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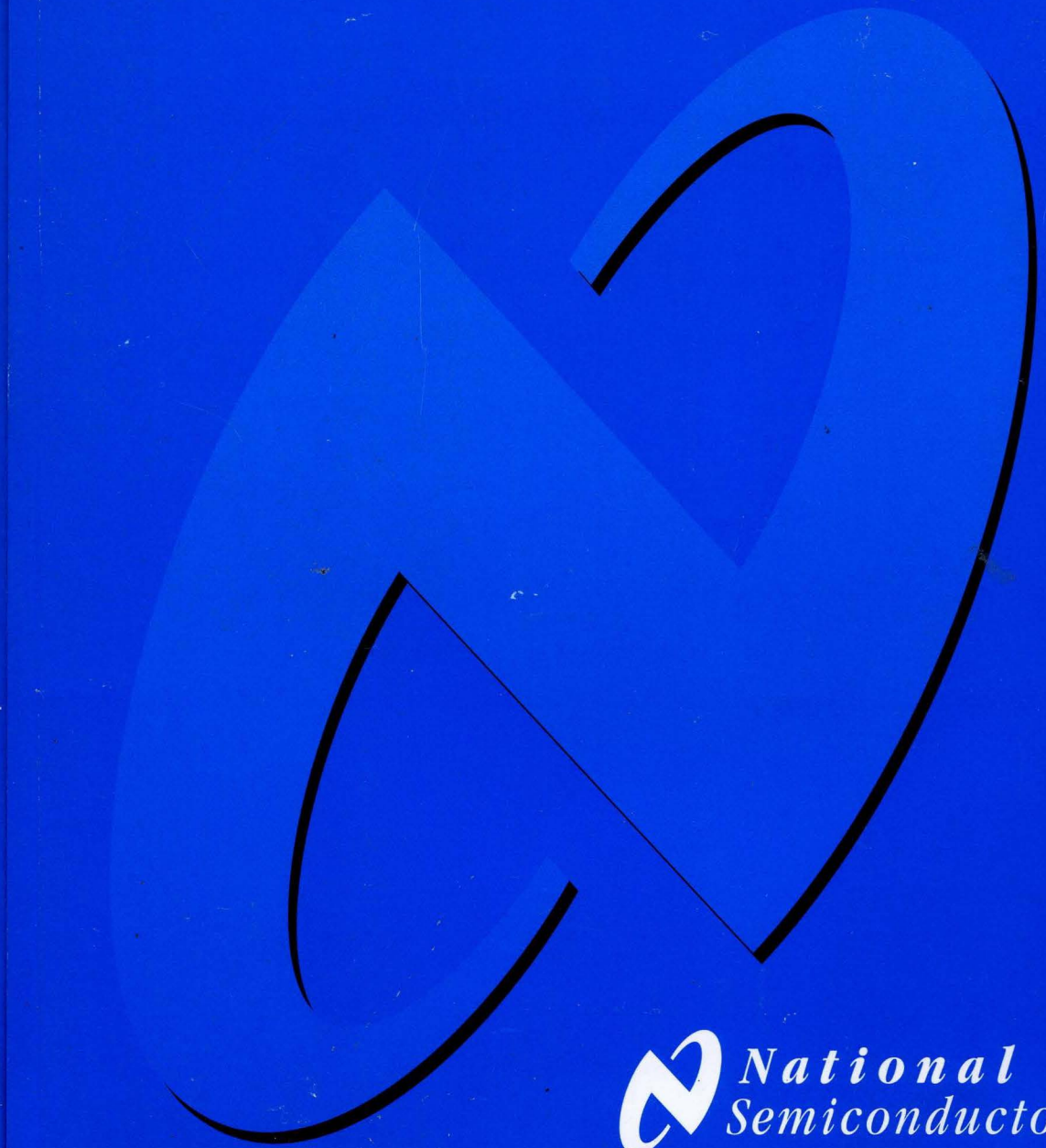
Linear Applications Handbook



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The Sight & Sound of Information

Linear Applications Handbook

2003

Linear Applications Handbook

2003 Edition

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Introduction

The purpose of this handbook is to provide a fully indexed and cross-referenced collection of analog integrated circuit applications using devices from National Semiconductor. The printed handbook includes application notes about analog/linear devices that are currently available from National.

Individual application notes are normally written to explain the operation and use of one particular device or to detail various methods of accomplishing a given function. The organization of this handbook takes advantage of this innate coherance by keeping each application note intact, arranging them by subject, then in alpha-numerical order. A detailed Subject Index and a Part Number to Application Note Crossreference are provided for quick reference, following the Alpha-Numeric Index of all analog/linear application notes.

Many of the application schematics refer to the generic family, identified by either the industrial/commercial temperature range version or the military temperature range version of the device. Generally, any device in the generic family will work in the circuit. For example, an amplifier indicated as an LM108 refers to any product contained in the LM108 family datasheet (such as LM208 or LM308), and does not imply that only military-grade devices will work in the application. Military and prime electrical ("A") grade devices need only be considered when their tighter electrical limits or wider temperature range warrants their use.

A CD is included with this handbook. It contains a complete set of all application notes available from National, as well as product information (datasheets, budgetary pricing, etc.) for the products referred to in this handbook. For updated information on these and any other National Semiconductor products, please consult our web site at http://www.national.com.

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Table of Contents

Table of Contents (Continued)

Table of Contents (Continued)

Table of Contents (Continued)

Table of Contents (Continued)

Table of Contents (Continued)

National Semiconductor

Alpha-Numeric Index

Alpha-Numeric Index (Continued)

Alpha-Numeric Index (Continued)

Alpha-Numeric Index (Continued)

Alpha-Numeric Index (Continued)

Alpha-Numeric Index (Continued)

Alpha-Numeric Index (Continued)

Alpha-Numeric Index (Continued)

Alpha-Numeric Index (Continued)

National Semiconductor

Device/Application Literature Cross-Reference

Products	Applications Documents
ADC0801-05	AN-274
ADC0801	AN-233, LB-53
ADC0804	AN-280, AN-281, AN-301
ADC0808	AN-247
ADC0809	AN-247
ADC0816	AN-193, AN-258
ADC0817	AN-258
ADC0833	AN-280, AN-281
ADC1001	AN-276
ADC1061	AN-804
ADC1210	AN-245
ADC3511	AN-200
ADC8711	AN-200
ADC10461	AN-769
ADC10662	AN-769
ADC12038	AN-929
ADC12040	AN-1261
ADC12441	AN-769
ADC12451	AN-769
ADC16071	AN-1002
ADC16471	AN-1002
ADD3501	AN-202
BPA200	AN-1192
BR100	AN-1192
CLC109	OA-18
CLC111	OA-18, OA-21, OA-27, OA-29
CLC205	OA-15
CLC221	OA-22
CLC400	OA-07, OA-13, OA-14, OA-18, OA-24, OA-31
CLC401	OA-07, OA-11, OA-14, OA-18, OA-22, OA-31
CLC402	OA-18, OA-31
CLC404	OA-11, OA-18, OA-31
CLC405	OA-18, OA-31
CLC406	OA-18, OA-24, OA-25, OA-31
CLC407	OA-18, OA-31
CLC409	OA-07, OA-18, OA-31
CLC410	OA-18, OA-31
CLC411	OA-18, OA-31

Device/Application Literature Cross-Reference (Continued)

Products	Applications Documents
CLC412	OA-18, OA-31
CLC414	OA-18, OA-31
CLC415	OA-18, OA-31
CLC420	OA-18, OA-31
CLC425	OA-18, OA-31
CLC426	OA-18, OA-31
CLC428	OA-18, OA-31
CLC430	OA-18, OA-24, OA-26, OA-31
CLC431	OA-18, OA-31
CLC432	OA-18, OA-26, OA-31
CLC440	OA-18, OA-31
CLC446	OA-21, OA-27, OA-28, OA-29, OA-31
CLC449	OA-18, OA-31
CLC450	AN-1244, OA-18, OA-31
CLC505	OA-19, OA-31
CLC520	OA-16, OA-31
CLC522	OA-31
CLC935	AD-01, AD-02
CLC949	AD-04
CLC5506	AN-1138
DAC0830	AN-271, AN-284
DAC1000	AN-271, AN-275, AN-277
DAC1006	AN-271, AN-275, AN-277
DAC1020	AN-263, AN-269, AN-293, AN-294, AN-299
DAC1208	AN-271
DAC1218	AN-293
DS14C88	AN-438
DS14C89A	AN-438
DS14C335	AN-914
DS26LS31	AN-805, AN-903
DS26LS32A	AN-903
DS36C278	AN-1057
DS36C279	AN-1057
DS36C280	AN-1031, AN-1057
DS78LS120	AN-214
DS96F172	AN-805
DS1691	AN-214
DS3362	AN-259
DS3595	AN-409
DS3596	AN-409
DS3662	AN-337

Device/Application Literature Cross-Reference (Continued)

Products	Applications Documents
DS3695	AN-454, AN-1057
DS3696	AN-759, AN-1057
DS7820	AN-22
DS7830	AN-22
DS8820	AN-22
DS8830	AN-22
DS8880	AN-84
DS8884A	AN-84
DS8911	AN-512
DS8921	AN-457
DS8922	AN-457
DS8923	AN-457
DS36276	AN-1031, AN-1057
DS36277	AN-915, AN-1057
DS36954	AN-904, AN-1057
DS37277	AN-1031
DS75176B	AN-915
DS76176B	AN-1057
LF155	AN-263
LF347	AN-256, AN-265, AN-262, LB-44
LF351	AN-240
LF353	AN-263
LF356	AN-260, AN-272, AN-447
LF357	AN-272, LB-42
LF398	AN-266, AN-294, AN-298, AN-776, LB-45
LF411	AN-272, AN-447
LF412	AN-299
LF441	AN-447
LF6197	AN-775
LF13006	AN-344
LF13007	AN-344
LF13509	AN-295
LH0002	AN-227
LH0024	AN-253
LH0032	AN-253
LH0033	AN-48, AN-227
LH0063	AN-227
LH0094	AN-637
LH0101	AN-261
LH1605	AN-343
LH4101	AN-480

Device/Application Literature Cross-Reference (Continued)

Products	Applications Documents
LH4117	AN-597
LH4118	AN-597
LH4200	AN-597
LH4860	AN-775
LM10	AN-211, AN-300, TP-14
LM11	AN-241, AN-242
LM12	AN-446, AN-446A, AN-446B
LM20	AN-1256
LM34	AN-460
LM35	AN-460
LM70	AN-1189
LM78S40	AN-711
LM85	AN-1260
LM88	AN-1262
LM101	AN-4, AN-20, AN-24
LM101A	AN-30, AN-31, AN-32, LB-2, LB-4, LB-8, LB-16
LM102	AN-31, AN-32, LB-1, LB-5, LB-6
LM104	AN-110
LM105	AN-110
LM105	AN-23
LM106	LB-6
LM107	AN-20, LB-1
LM108	AN-29, AN-30, AN-31, AN-32, AN-110, LB-14
LM108A	LB-15
LM109	AN-42, LB-15
LM110	LB-11, LB-42
LM111	AN-41, LB-12, LB-32, LB-39
LM113	AN-56
LM117	AN-178, AN-181, AN-182
LM118	AN-110, LB-17, LB-21, LB-23, LB-25
LM119	LB-23
LM121	AN-79, AN-260, LB-32
LM122	AN-97
LM125	AN-82
LM129	AN-173
LM134	LB-41
LM139	AN-74
LM143	AN-127
LM158/LM258/LM358	AN-116
LM163	AN-295
LM194	AN-222

Device/Application Literature Cross-Reference (Continued)

Products	Applications Documents
LM195	AN-110, AN-161, AN-184
LM211	AN-41, LB12, LB-39
LM239	AN-74
LM257x	AN-1229
LM267x	AN-1229
LM269x	AN-1229
LM305	AN-23
LM308	AN-184
LM311	AN-41, LB-12, LB-18, LB-39
LM317	AN-178, AN-181, AN-182, LB-35, LB-46, LB-47
LM321	LB-24
LM324	LB-44
LM329	AN-184, AN-225
LM331	AN-210, AN-240, AN-265, AN-285, AN-C, AN-D, LB-45
LM331	AN-265
LM334	AN-256
LM335	AN-225
LM336	AN-200
LM337	LB-46, LB-49
LM338	LB-49, LB-51
LM339	AN-74
LM340	AN-103
LM349	LB-42
LM359	AB-24, AN-278
LM360	AN-87
LM361	AN-87
LM378	AN-147
LM380	AN-69
LM382	AN-147
LM385	AN-715
LM391	AN-272
LM392	AN-286
LM394	AN-222, AN-263, AN-265, AN-299, AN-311, LB-52
LM395	LB-28
LM399	AN-184
LM555	AB-7
LM556	AB-7
LM565	AN-46, AN-146
LM566	AN-146
LM628	AN-693, AN-706
LM629	AN-868

Device/Application Literature Cross-Reference (Continued)

Products	Applications Documents
LM833	AN-346
LM1084	AN-1148
LM1800	AN-147
LM1823	AN-391
LM1830	AB-10
LM1894	AN-384, AN-386, AN-390
LM2576	AN-946
LM2577	AN-776, AN-777
LM2586	AN-1082
LM2587	AN-1061, AN-1095
LM2588	AN-1082
LM2593HV	AN-1197, AN-1207, AN-1246, AN-1253
LM2594	AN-1061
LM2595	AN-1118
LM2596	AN-1081
LM2611	AN-1203
LM2622	AN-1198, AN-1250
LM2623	AN-1221, AN-1258
LM2633	AN-1208
LM2635	AN-1145
LM2636	AN-1145
LM2637	AN-1145
LM2638	AN-1145
LM2639	AN-1146
LM2642	AN-1239
LM2650	AN-1071
LM2651	AN-1143
LM2653	AN-1133
LM2655	AN-1215
LM2661	AN-1142
LM2663	AN-1142
LM2664	AN-1142
LM2673	AN-1135, AN-1157
LM2675	AN-1120
LM2676	AN-1135
LM2678	AN-1135
LM2679	AN-1135
LM2698	AN-1202
LM2704	AN-1250
LM2727	AN-1247
LM2750	AN-1252

Device/Application Literature Cross-Reference (Continued)

Products	Applications Documents
LM2787	AN-1209
LM2791	AN-1218
LM2792	AN-1218, AN-1251
LM2794	AN-1218, AN-1251
LM2795	AN-1218, AN-1251
LM2825	AN-1038, AN-1061
LM2889	AN-402
LM2907	AN-162
LM2931	AB-11, AB-12
LM3089	AN-147
LM3352	AN-1144
LM3354	AN-1214, AN-1251
LM3355	AN-1214, AN-1251
LM3477	AN-1193
LM3478	AN-1204
LM3485	AN-1227
LM3488	AN-1204
LM3524	AN-272, AN-288, AN-292, AN-715
LM3525	AN-1249
LM3578A	AB-30, AN-1055, AN-1066
LM3622	AN-1249
LM3641	AN-1067
LM3645	AN-1068
LM3647	AN-1164, AN-1165
LM3820	AN-147
LM3876	AN-898
LM3900	AB-24, AN-72, LB-20
LM3909	AN-154
LM3914	LB-48
LM3940	AN-1061
LM4250	AN-71, LB-34
LM6181	AN-813, AN-840
LM6361/LM6364/LM6365	AN-549
LM6511	AN-1061
LM6622	AN-1255
LM8272	AN-1245
LM12454	AN-906, AN-949
LM12458	AN-906, AN-947, AN-949
LMC835	AN-435
LMC6484	AN-856
LMC6953	AN-1077

Device/Application Literature Cross-Reference (Continued)

Products	Applications Documents
LMD18200	AN-694, AN-828
LMF40	AN-779
LMF90	AN-779
LMF120	AN-779
LMH6642	AN-1244
LMH6643	AN-1240, AN-1255
LMH6672	AN-1255
LMX5600	LB-27
LP2952	AN-1061
LP2960	AN-1061
LP2980	AN-1148, AN-1172
LP2981	AN-1148, AN-1172
LP2982	AN-1148, AN-1172
LP2985	AN-1148, AN-1172
LP2989	AN-1148
LP2995	AN-1241, AN-1254
LP3985	AN-1219
MF8	AN-779
MF10	AN-307

National Semiconductor

Subject Index

Subject Index (Continued)

Subject Index (Continued)

Subject Index (Continued)

Subject Index (Continued)

Subject Index (Continued)

Subject Index (Continued)

Subject Index (Continued)

Subject Index (Continued)

Subject Index (Continued)

Subject Index (Continued)

Subject Index (Continued)

Subject Index (Continued)

Subject Index (Continued)

Subject Index (Continued)

Section 1

Amplifiers and Signal Conditioning: Device Information

Section 1 Contents

Monolithic Op Amp—The Universal Linear Component

National Semiconductor
Application Note 4
Robert J. Widlar

Introduction

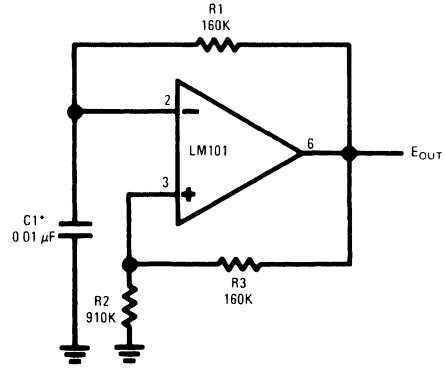
Operational amplifiers are undoubtedly the easiest and best way of performing a wide range of linear functions from simple amplification to complex analog computation. The cost of monolithic amplifiers is now less than $2.00, in large quantities, which makes it attractive to design them into circuits where they would not otherwise be considered. Yet low cost is not the only attraction of monolithic amplifiers. Since all components are simultaneously fabricated on one chip, much higher circuit complexities than can be used with discrete amplifiers are economical. This can be used to give improved performance. Further, there are no insurmountable technical difficulties to temperature stabilizing the amplifier chip, giving chopper-stabilized performance with little added cost.

Operational amplifiers are designed for high gain, low offset voltage and low input current. As a result, dc biasing is considerably simplified in most applications; and they can be used with fairly simple design rules because many potential error terms can be neglected. This article will give examples demonstrating the range of usefulness of operational amplifiers in linear circuit design. The examples are certainly not all-inclusive, and it is hoped that they will stimulate even more ideas from others. A few practical hints on preventing oscillations in operational amplifiers will also be given since this is probably the largest single problem that many engineers have with these devices.

Although the designs presented use the LM101 operational amplifier and the LM102 voltage follower produced by National Semiconductor, most are generally applicable to all monolithic devices if the manufacturer's recommended frequency compensation is used and differences in maximum ratings are taken into account. A complete description of the LM101 is given elsewhere;[1] but, briefly, it differs from most other monolithic amplifiers, such as the LM709,[2] in that it has a ±30V differential input voltage range, a +15V, −12V common mode range with ±15V supplies and it can be compensated with a single 30 pF capacitor. The LM102,[3] which is also used here, is designed specifically as a voltage follower and features a maximum input current of 10 nA and a 10 V/μs slew rate.

Operational-Amplifier Oscillator

The free-running multivibrator shown in *Figure 1* is an excellent example of an application where one does not normally consider using an operational amplifier. However, this circuit operates at low frequencies with relatively small capacitors because it can use a longer portion of the capacitor time constant since the threshold point of the operational amplifier is well determined. In addition, it has a completely-symmetrical output waveform along with a buffered output, although the symmetry can be varied by returning R2 to some voltage other than ground.



*Chosen for oscillation at 100 Hz

FIGURE 1. Free-Running Multivibrator

Another advantage of the circuit is that it will always self start and cannot hang up since there is more dc negative feedback than positive feedback. This can be a problem with many "textbook" multivibrators.

Since the operational amplifier is used open loop, the usual frequency compensation components are not required since they will only slow it down. But even without the 30 pF capacitor, the LM101 does have speed limitations which restrict the use of this circuit to frequencies below about 2 kHz.

The large input voltage range of the LM101 (both differential and single ended) permits large voltage swings on the input so that several time constants of the timing capacitor, C1, can be used. With most other amplifiers, R2 must be reduced to keep from exceeding these ratings, which requires that C1 be increased. Nonetheless, even when large values are needed for C1, smaller polarized capacitors may be used by returning them to the positive supply voltage instead of ground.

Level Shifting Amplifier

Frequently, in the design of linear equipment, it is necessary to take a voltage which is referred to some dc level and produce an amplified output which is referred to ground. The most straight-forward way of doing this is to use a differential amplifier similar to that shown in *Figure 2a.* This circuit, however, has the disadvantages that the signal source is loaded by current from the input divider, R3 and R4, and that the feedback resistors must be very well matched to prevent erroneous outputs from the common mode input signal.

Level Shifting Amplifier (Continued)

A circuit which does not have these problems is shown in *Figure 2b*. Here, an FET transistor on the output of the operational amplifier produces a voltage drop across the feedback resistor, R1, which is equal to the input voltage. The voltage across R2 will then be equal to the input voltage multiplied by the ratio, R2/R1; and the common mode rejection will be as good as the basic rejection of the amplifier, independent of the resistor tolerances. This voltage is buffered by an LM102 voltage follower to give a low impedance output.

An advantage of the LM101 in this circuit is that it will work with input voltages up to its positive supply voltages as long as the supplies are less than ±15V.

Voltage Comparators

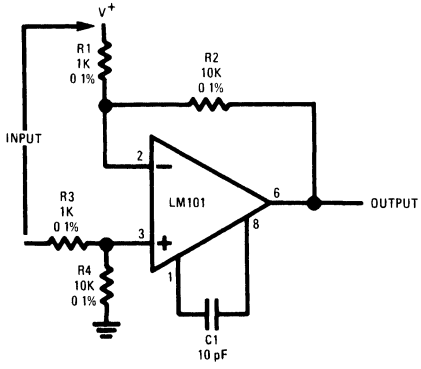
The LM101 is well suited to comparator applications for two reasons: first, it has a large differential input voltage range and, second, the output is easily clamped to make it compatible with various driver and logic circuits. It is true that it doesn't have the speed of the LM710[4] (10 µs versus 40 ns, under equivalent conditions); however, in many linear applications speed is not a problem and the lower input currents along with higher voltage capability of the LM101 is a tremendous benefit.

Two comparator circuits using the LM101 are shown in *Figure 3*. The one in *Figure 3a* shows a clamping scheme which makes the output signal directly compatible with DTL or TTL integrated circuits. An LM103 breakdown diode clamps the output at 0V or 4V in the low or high states, respectively. This particular diode was chosen because it has a sharp breakdown and low equivalent capacitance. When working as a comparator, the amplifier operates open loop so normally no frequency compensation is needed. Nonetheless, the stray capacitance between Pins 5 and 6 of the amplifier should be minimized to prevent low level oscillations when the comparator is in the active region. If this becomes a problem a 3 pF capacitor on the normal compensation terminals will eliminate it.

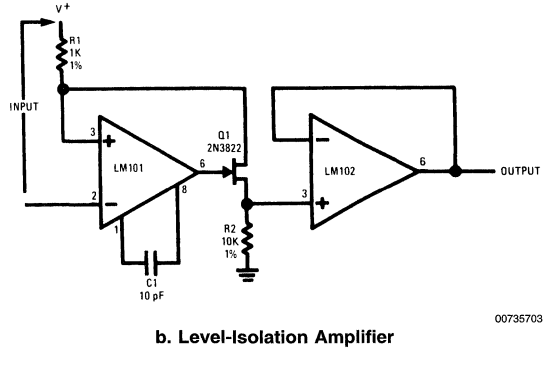
Figure 3b shows the connection of the LM101 as a comparator and lamp driver. Q1 switches the lamp, with R2 limiting the current surge resulting from turning on a cold lamp. R1 determines the base drive to Q1 while D1 keeps the amplifier from putting excessive reverse bias on the emitter-base junction of Q1 when it turns off.

More Output Current Swing

Because almost all monolithic amplifiers use class-B output stages, they have good loaded output voltage swings, delivering ±10V at 5 mA with ±15V supplies. Demanding much more current from the integrated circuit would require, for one, that the output transistors be made considerably larger. In addition, the increased dissipation could give rise to troublesome thermal gradients on the chip as well as excessive package heating in high-temperature applications. It is therefore advisable to use an external buffer when large output currents are needed.



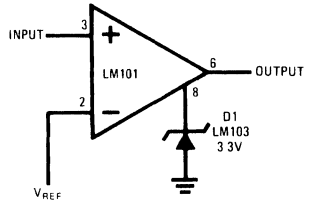
a. Standard Differential Amplifier



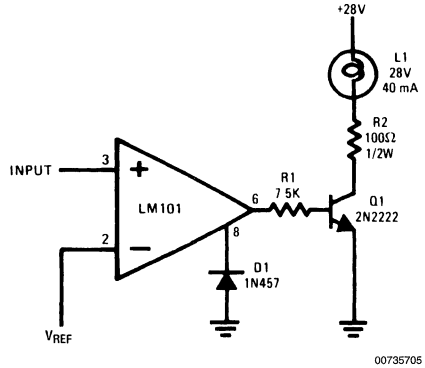
b. Level-Isolation Amplifier

FIGURE 2. Level-Shifting Amplifiers

More Output Current Swing (Continued)



a. Comparator for driving DTL and TTL integrated circuits



b. Comparator and Lamp Driver

FIGURE 3. Voltage Comparator Circuits

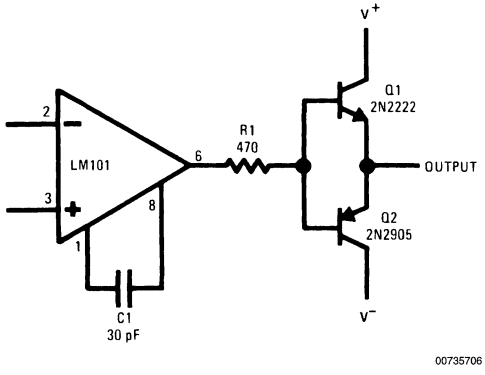


FIGURE 4. High Current Output Buffer

A simple way of accomplishing this is shown in *Figure 4.* A pair of complementary transistors are used on the output of the LM101 to get the increased current swing. Although this circuit does have a dead zone, it can be neglected at frequencies below 100 Hz because of the high gain of the amplifier. R1 is included to eliminate parasitic oscillations from the output transistors. In addition, adequate bypassing should be used on the collectors of the output transistors to insure that the output signal is not coupled back into the amplifier. This circuit does not have current limiting, but it can be added by putting 50Ω resistors in series with the collectors of Q1 and Q2.

A FET Amplifier

For ambient temperatures less than about 70°C, junction field effect transistors can give exceptionally low input currents when they are used on the input stage of an operational amplifier. However, monolithic FET amplifiers are not now available since it is no simple matter to diffuse high quality FET's on the same chip as the amplifier. Nonetheless, it is possible to make a good FET amplifier using a discrete FET pair in conjunction with a monolithic circuit.

Such a circuit is illustrated in *Figure 5.* A matched FET pair, connected as source followers, is put in front of an integrated operational amplifier. The composite circuit has roughly the same gain as the integrated circuit by itself and is compensated for unity gain with a 30 pF capacitor as shown. Although it works well as a summing amplifier, the circuit leaves something to be desired in applications requiring high common mode rejection. This happens both because resistors are used for current sources and because the FET's by themselves do not have good common mode rejection.

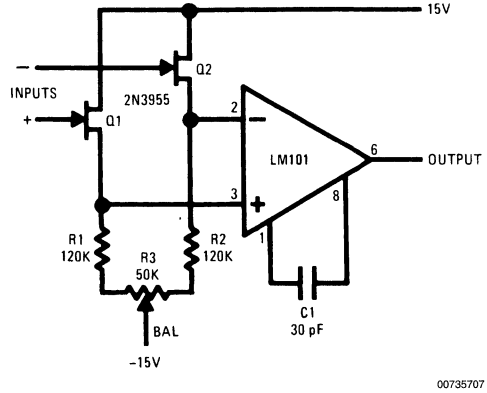
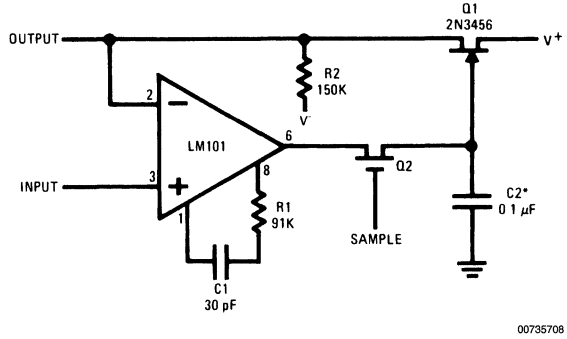


FIGURE 5. FET Operational Amplifier

Storage Circuits

A sample-and-hold circuit which combines the low input current of FET's with the low offset voltage of monolithic amplifiers is shown in *Figure 6.* The circuit is a unity gain amplifier employing an operational amplifier and an FET source follower. In operation, when the sample switch, Q2, is turned on, it closes the feedback loop to make the output equal to the input, differing only by the offset voltage of the LM101. When the switch is opened, the charge stored on C2 holds the output at a level equal to the last value of the input voltage.



*Polycarbonate-dielectric capacitor

FIGURE 6. Low Drift Sample and Hold

Some care must be taken in the selection of the holding capacitor. Certain types, including paper and mylar, exhibit a polarization phenomenon which causes the sampled voltage to drop off by about 50 mV, and then stabilize, when the capacitor is exercised over a 5V range during the sample interval. This drop off has a time constant in the order of seconds. The effect, however, can be minimized by using capacitors with teflon, polyethylene, glass or polycarbonate dielectrics.

Although this circuit does not have a particularly low output resistance, fixed loads do not upset the accuracy since the loading is automatically compensated for during the sample interval. However, if the load is expected to change after sampling, a buffer such as the LM102 must be added between the FET and the output.

A second pole is introduced into the loop response of the amplifier by the switch resistance and the holding capacitor, C2. This can cause problems with overshoot or oscillation if it is not compensated for by adding a resistor, R1, in series with the LM101 compensation capacitor such that the breakpoint of the R1C1 combination is roughly equal to that of the switch and the holding capacitor.

It is possible to use an MOS transistor for Q1 without worrying about the threshold stability. The threshold voltage is balanced out during every sample interval so only the short-term threshold stability is important. When MOS transistors are used along with mechanical switches, drift rates less than 10 mV/min can be realized.

Additional features of the circuit are that the amplifier acts as a buffer so that the circuit does not load the input signal.

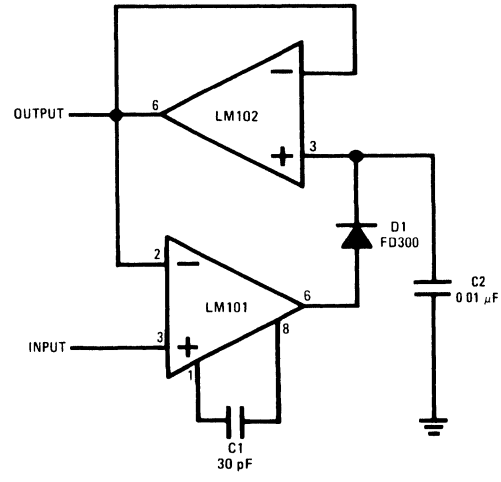


FIGURE 7. Positive Peak Detector with Buffered Output

Further, gain can also be provided by feeding back to the inverting input of the LM101 through a resistive divider instead of directly.

Storage Circuits (Continued)

The peak detector in *Figure 7* is similar in many respects to the sample-and-hold circuit. A diode is used in place of the sampling switch. Connected as shown, it will conduct whenever the input is greater than the output, so the output will be equal to the peak value of the input voltage. In this case, an LM102 is used as a buffer for the storage capacitor, giving low drift along with a low output resistance.

As with the sample and hold, the differential input voltage range of the LM101 permits differences between the input and output voltages when the circuit is holding.

Non-Linear Amplifiers

When a non-linear transfer function is needed from an operational amplifier, many methods of obtaining it present themselves. However, they usually require diodes and are therefore difficult to temperature compensate for accurate breakpoints. One way of getting around this is to make the output swing so large that the diode threshold is negligible by comparison, but this is not always practical.

A method of producing very sharp, temperature-stable breakpoints in the transfer function of an operational amplifier is shown in *Figure 8*. For small input signals, the gain is determined by R1 and R2. Both Q2 and Q3 are conducting to some degree, but they do not affect the gain because their current gain is high and they do not feed any appreciable current back into the summing mode. When the output voltage rises to 2V (determined by R3, R4 and V^-), Q3 draws enough current to saturate, connecting R4 in parallel with R2. This cuts the gain in half. Similarly, when the output voltage rises to 4V, Q2 will saturate, again halving the gain.

Temperature compensation is achieved in this circuit by including Q1 and Q4. Q4 compensates the emitter-base voltage of Q2 and Q3 to keep the voltage across the feedback resistors, R4 and R6, very nearly equal to the output voltage while Q1 compensates for the emitter base voltage of these transistors as they go into saturation, making the voltage across R3 and R5 equal to the negative supply voltage. A detrimental effect of Q4 is that it causes the output resistance of the amplifier to increase at high output levels. It may therefore be necessary to use an output buffer if the circuit must drive an appreciable load.

Servo Preamplifier

In certain servo systems, it is desirable to get the rate signal required for loop stability from some sort of electrical, lead network. This can, for example, be accomplished with reactive elements in the feedback network of the servo preamplifier.

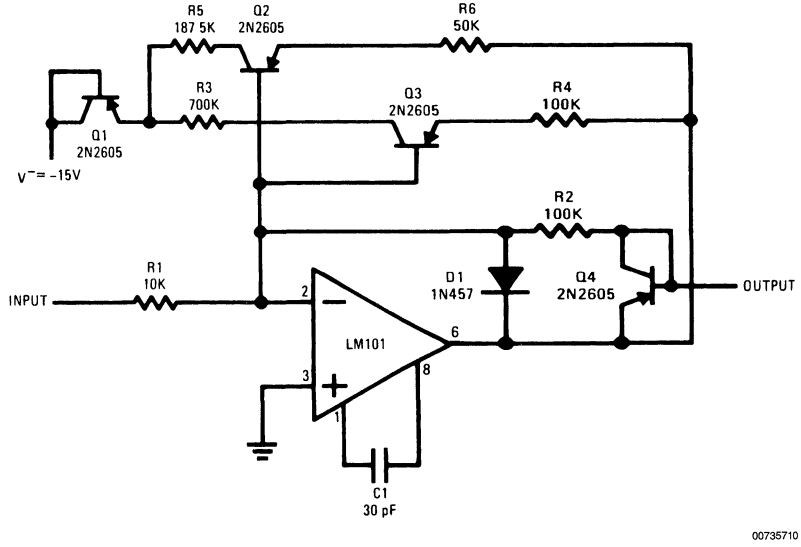


FIGURE 8. Nonlinear Operational Amplifier with temperature-compensated breakpoints

Many saturating servo amplifiers operate over an extremely wide dynamic range. For example, the maximum error signal could easily be 1000 times the signal required to saturate the system. Cases like this create problems with electrical rate networks because they cannot be placed in any part of the system which saturates. If the signal into the rate network saturates, a rate signal will only be developed over a narrow range of system operation; and instability will result when the error becomes large. Attempts to place the rate networks in front of the error amplifier or make the error amplifier linear over the entire range of error signals frequently gives rise to excessive dc error from signal attenuation.

These problems can be largely overcome using the kind of circuit shown in *Figure 9*. This amplifier operates in the linear mode until the output voltage reaches approximately 3V with 30 µA output current from the solar cell sensors. At this point the breakdown diodes in the feedback loop begin to conduct,

Servo Preamplifier (Continued)

drastically reducing the gain. However, a rate signal will still be developed because current is being fed back into the rate network (R1, R2 and C1) just as it would if the amplifier had remained in the linear operating region. In fact, the amplifier will not actually saturate until the error current reaches 6 mA, which would be the same as having a linear amplifier with a ±600V output swing.

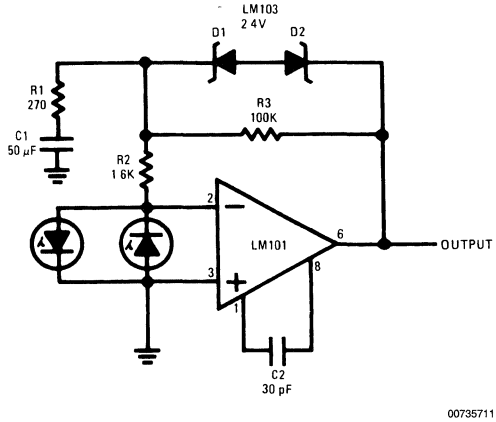


FIGURE 9. Saturating Servo Preamplifier with Rate Feedback

Computing Circuits

In analog computation it is a relatively simple matter to perform such operations as addition, subtraction, integration and differentiation by incorporating the proper resistors and capacitors in the feedback circuit of an amplifier. Many of these circuits are described in reference 5. Multiplication and division, however, are a bit more difficult. These operations are usually performed by taking the logarithms of the quantities, adding or subtracting as required and then taking the antilog.

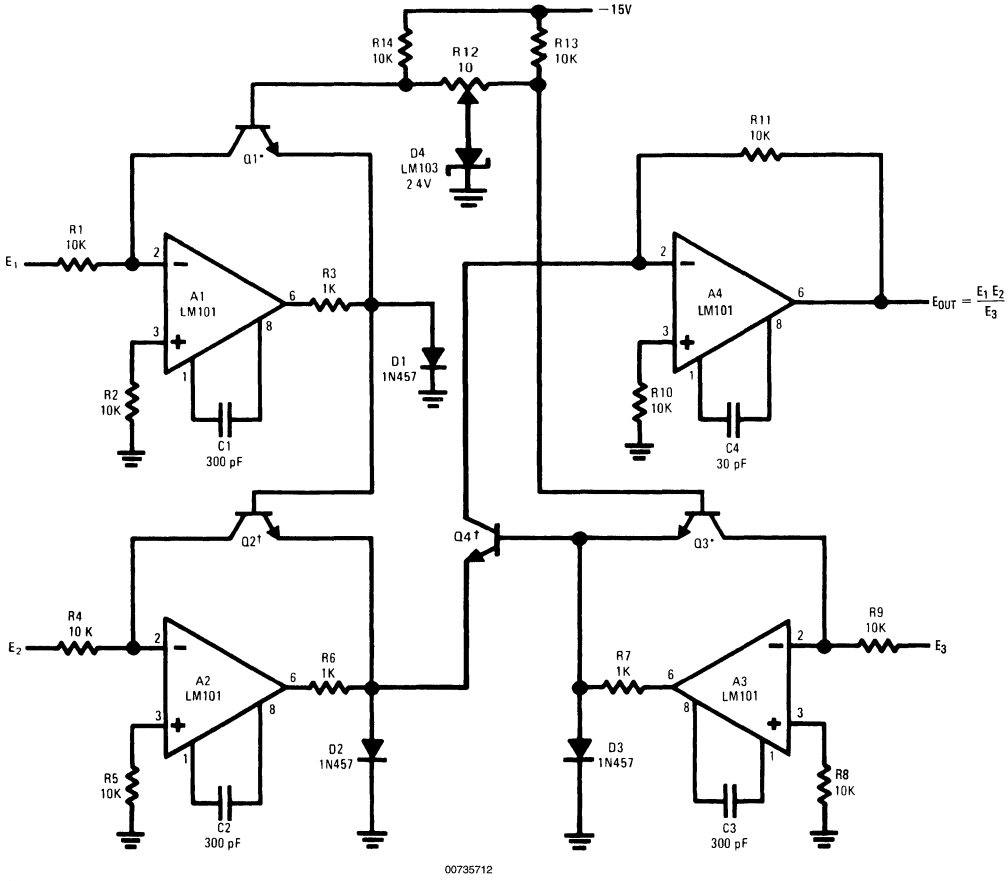
At first glance, it might appear that obtaining the log of a voltage is difficult; but it has been shown[6] that the emitter-base voltage of a silicon transistor follows the log of its collector current over as many as nine decades. This means that common transistors can be used to perform the log and antilog operations.

A circuit which performs both multiplication and division in this fashion is shown in *Figure 10*. It gives an output which is proportional to the product of two inputs divided by a third, and it is about the same complexity as a divider alone.

The circuit consists of three log converters and an antilog generator. Log converters similar to these have been described elsewhere,[7] but a brief description follows. Taking amplifier A1, a logging transistor, Q1, is inserted in the feedback loop such that its collector current is equal to the input voltage divided by the input resistor, R1. Hence, the emitter-base voltage of Q1 will vary as the log of the input voltage E1.

A2 is a similar amplifier operating with logging transistor, Q2. The emitter-base junctions of Q1 and Q2 are connected in series, adding the log voltages. The third log converter produces the log of E3. This is series-connected with the antilog transistor, Q4; and the combination is hooked in parallel with the output of the other two log convertors. Therefore, the emitter-base of Q4 will see the log of E3 subtracted from the sum of the logs of E1 and E2. Since the collector current of a transistor varies as the exponent of the emitter-base voltage, the collector current of Q4 will be proportional to the product of E1 and E2 divided by E3. This current is fed to the summing amplifier, A4, giving the desired output.

Computing Circuits (Continued)



*†LM394

FIGURE 10. Analog Multiplier/Divider

Computing Circuits (Continued)

This circuit can give 1-percent accuracy for input voltages from 500 mV to 50V. To get this precision at lower input voltages, the offset of the amplifiers handling them must be individually balanced out. The zener diode, D4, increases the collector-base voltage across the logging transistors to improve high current operation. It is not needed, and is in fact undesirable, when these transistors are running at currents less than 0.3 mA. At currents above 0.3 mA, the lead resistances of the transistors can become important (0.25Ω is 1-percent at 1 mA) so the transistors should be installed with short leads and no sockets.

An important feature of this circuit is that its operation is independent of temperature because the scale factor change in the log converter with temperature is compensated by an equal change in the scale factor of the antilog generator. It is only required that Q1, Q2, Q3 and Q4 be at the same temperature. Dual transistors should be used and arranged as shown in the figure so that thermal mismatches between cans appear as inaccuracies in scale factor (0.3-percent/°C) rather than a balance error (8-percent/°C). R12 is a balance potentiometer which nulls out the offset voltages of all the logging transistors. It is adjusted by setting all input voltages equal to 2V and adjusting for a 2V output voltage.

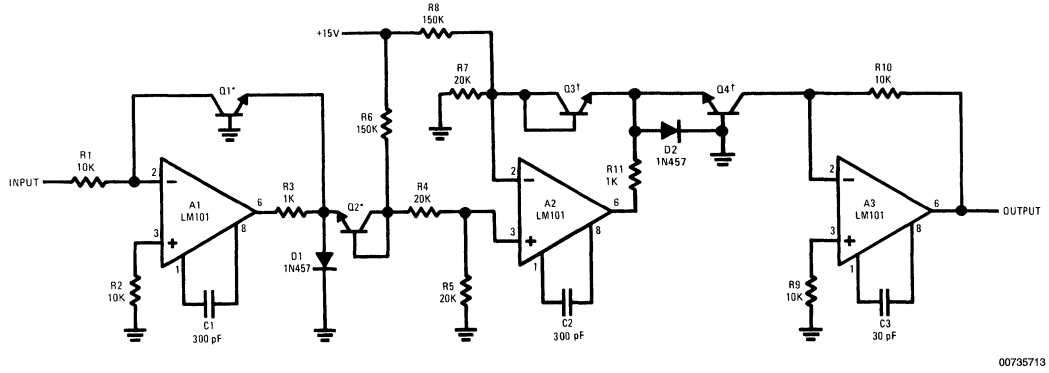
The logging transistors provide a gain which is dependent on their operating level, which complicates frequency compensation. Resistors (R3, R6 and R7) are put in the amplifier output to limit the maximum loop gain, and the compensation capacitor is chosen to correspond with this gain. As a result, the amplifiers are not especially designed for speed, but techniques for optimizing this parameter are given in reference 6.

Finally, clamp diodes D1 through D3, prevent exceeding the maximum reverse emitter-base voltage of the logging transistors with negative inputs.

Root Extractor*

Taking the root of a number using log converters is a fairly simple matter. All that is needed is to take the log of a voltage, divide it by, say ½ for the square root, and then take the antilog. A circuit which accomplishes this is shown in *Figure 11*. A1 and Q1 form the log converter for the input signal. This feeds Q2 which produces a level shift to give zero voltage into the R4, R5 divider for a 1V input. This divider reduces the log voltage by the ratio for the root desired and drives the buffer amplifier, A2. A2 has a second level shifting diode, Q3, its feedback network which gives the output voltage needed to get a 1V output from the antilog generator, consisting of A3 and Q4, with a unity input. The offset voltages of the transistors are nulled out by imbalancing R6 and R8 to give 1V output for 1V input, since any root of one is one.

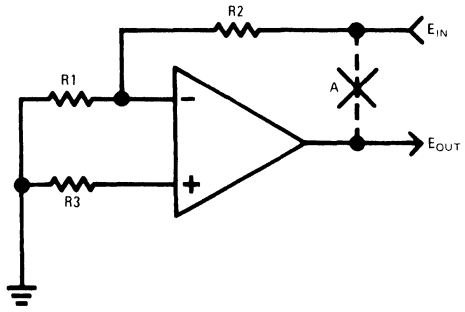
Note: *The "extraction" used here doubtless has origin in the dental operation most of us would fear less than having to find even a square root without tables or other aids



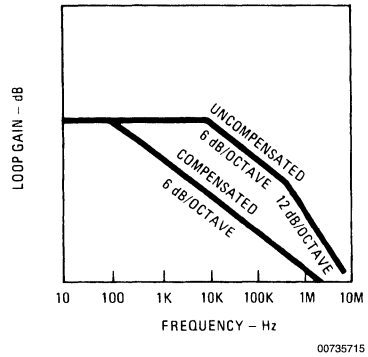
†LM394

FIGURE 11. Root Extractor

Root Extractor* (Continued)



a. Measuring loop gain



b. Typical response

FIGURE 12. Illustrating Loop Gain

Q2 and Q3 are connected as diodes in order to simplify the circuitry. This doesn't introduce problems because both operate over a very limited current range, and it is really only required that they match. R7 is a gain-compensating resistor which keeps the currents in Q2 and Q3 equal with changes in signal level.

As with the multiplier/divider, the circuit is insensitive to temperature as long as all the transistors are at the same temperature. Using transistor pairs and matching them as shown minimizes the effects of gradients.

The circuit has 1-percent accuracy for input voltages between 0.5 and 50V. For lower input voltages, A1 and A3 must have their offsets balanced out individually.

Frequency Compensation Hints

The ease of designing with operational amplifiers sometimes obscures some of the rules which must be followed with any feedback amplifier to keep it from oscillating. In general, these problems stem from stray capacitance, excessive capacitive loading, inadequate supply bypassing or improper frequency compensation.

In frequency compensating an operational amplifier, it is best to follow the manufacturer's recommendations. However, if operating speed and frequency response is not a consideration, a greater stability margin can usually be obtained by increasing the size of the compensation capacitors. For example, replacing the 30 pF compensation capacitor on the LM101 with a 300 pF capacitor will make it ten times less susceptible to oscillation problems in the unity-gain connection. Similarly, on the LM709, using 0.05 µF, 1.5 kΩ, 2000 pF and 51Ω components instead of 5000 pF, 1.5 kΩ, 200 pF and 51Ω will give 20 dB more stability margin. Capacitor values less than those specified by the manufacturer for a particular gain connection should not be used since they will make the amplifier more sensitive to strays and capacitive loading, or the circuit can even oscillate with worst-case units.

The basic requirement for frequency compensating a feedback amplifier is to keep the frequency roll-off of the loop gain from exceeding 12 dB/octave when it goes through unity gain. *Figure 12a* shows what is meant by loop gain. The feedback loop is broken at the output, and the input sources are replaced by their equivalent impedance. Then the response is measured such that the feedback network is included.

Figure 12b gives typical responses for both uncompensated and compensated amplifiers. An uncompensated amplifier generally rolls off at 6 dB/octave, then 12 dB/octave and even 18 dB/octave as various frequency-limiting effects within the amplifier come into play. If a loop with this kind of response were closed, it would oscillate. Frequency compensation causes the gain to roll off at a uniform 6 dB/octave right down through unity gain This allows some margin for excess rolloff in the external circuitry.

Some of the external influences which can affect the stability of an operational amplifier are shown in *Figure 13.* One is the load capacitance which can come from wiring, cables or an actual capacitor on the output. This capacitance works against the output impedance of the amplifier to attenuate high frequencies. If this added rolloff occurs before the loop gain goes through zero, it can cause instability. It should be remembered that this single rolloff point can give more than 6 dB/octave rolloff since the output impedance of the amplifier can be increasing with frequency.

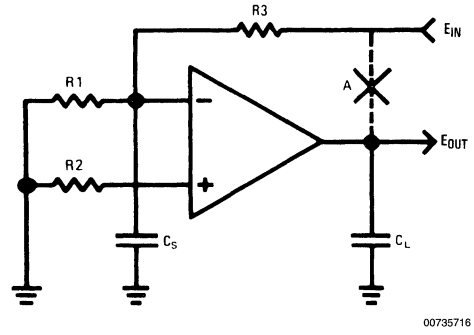


FIGURE 13. External Capacitances that Affect Stability

Frequency Compensation Hints

(Continued)

A second source of excess rolloff is stray capacitance on the inverting input. This becomes extremely important with large feedback resistors as might be used with an FET-input amplifier. A relatively simple method of compensating for this stray capacitance is shown in *Figure 14*: a lead capacitor, C1, put across the feedback resistor. Ideally, the ratio of the stray capacitance to the lead capacitor should be equal to the closed-loop gain of the amplifier. However, the lead capacitor can be made larger as long as the amplifier is compensated for unity gain. The only disadvantage of doing this is that it will reduce the bandwidth of the amplifier. Oscillations can also result if there is a large resistance on the non-inverting input of the amplifier. The differential input impedance of the amplifier falls off at high frequencies (especially with bipolar input transistors) so this resistor can produce troublesome rolloff if it is much greater than 10K, with most amplifiers. This is easily corrected by bypassing the resistor to ground.

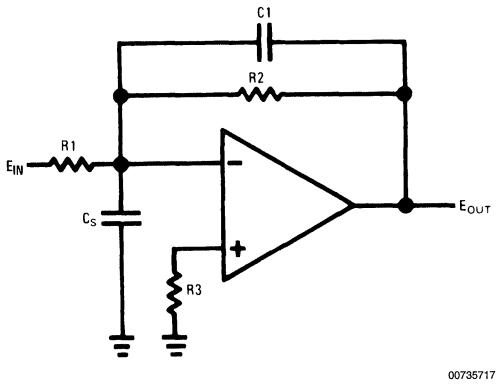


FIGURE 14. Compensating Stray Input Capacitance

When the capacitive load on an integrated amplifier is much greater than 100 pF, some consideration must be given to its effect on stability. Even though the amplifier does not oscillate readily, there may be a worst-case set of conditions under which it will. However, the amplifier can be stabilized for any value of capacitive loading using the circuit shown in *Figure 15*. The capacitive load is isolated from the output of the amplifier with R4 which has a value of 50Ω to 100Ω for both the LM101 and the LM709. At high frequencies, the feedback path is through the lead capacitor, C1, so that the lag produced by the load capacitance does not cause instability. To use this circuit, the amplifier must be compensated for unity gain, regardless of the closed loop dc gain. The value of C1 is not too important, but at a minimum its capacitive reactance should be one-tenth the resistance of R2 at the unity-gain crossover frequency of the amplifier.

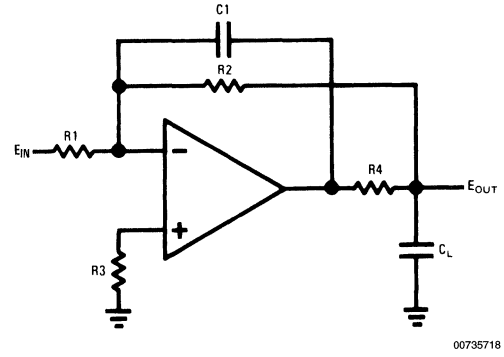


FIGURE 15. Compensating for Very Large Capacitive Loads

When an operational amplifier is operated open loop, it might appear at first glance that it needs no frequency compensation. However, this is not always the case because the external compensation is sometimes required to stabilize internal feedback loops.

The LM101 will not oscillate when operated open loop, although there may be problems if the capacitance between the balance terminal on pin 5 and the output is not held to an absolute minimum. Feedback between these two points is regenerative if it is not balanced out with a larger feedback capacitance across the compensation terminals. Usually a 3 pF compensation capacitor will completely eliminate the problem. The LM709 will oscillate when operated open loop unless a 10 pF capacitor is connected across the input compensation terminals and a 3 pF capacitor is connected on the output compensation terminals.

Problems encountered with supply bypassing are insidious in that they will hardly ever show up in a Nyquist plot. This problem has not really been thoroughly investigated, probably because one sure cure is known: bypass the positive and negative supply terminals of each amplifier to ground with at least a 0.01 µF capacitor.

For example, a LM101 can take over 1 mH inductance in either supply lead without oscillation. This should not suggest that they should be run without bypass capacitors. It has been established that 100 LM101's on a single printed circuit board with common supply busses will oscillate if the supplies are not bypassed about every fifth device. This happens even though the inputs and outputs are completely isolated.

Frequency Compensation Hints

(Continued)

The LM709, on the other hand, will oscillate under many load conditions with as little as 18 inches of wire between the negative supply lead and a bypass capacitor. Therefore, it is almost essential to have a set of bypass capacitors for every device.

Operational amplifiers are specified for power supply rejection at frequencies less than the first break frequency of the open loop gain. At higher frequencies, the rejection can be reduced depending on how the amplifier is frequency compensated. For both the LM101 and LM709, the rejection of high frequency signals on the positive supply is excellent. However, the situation is different for the negative supplies. These two amplifiers have compensation capacitors from the output down to a signal point which is referred to the negative supply, causing the high frequency rejection for the negative supply to be much reduced. It is therefore important to have sufficient bypassing on the negative supply to remove transients if they can cause trouble appearing on the output. One fairly large (22 µF) tantalum capacitor on the negative power lead for each printed-circuit card is usually enough to solve potential problems.

When high-current buffers are used in conjunction with operational amplifiers, supply bypassing and decoupling are even more important since they can feed a considerable amount of signal back into the supply lines. For reference, bypass capacitors of at least 0.1 µF are required for a 50 mA buffer.

When emitter followers are used to drive long cables, additional precautions are required. An emitter follower by itself—which is not contained in a feedback loop—will frequently oscillate when connected to a long length of cable. When an emitter follower is connected to the output of an operational amplifier, it can produce oscillations that will persist no matter how the loop gain is compensated. An analysis of why this happens is not very enlightening, so suffice it to say that these oscillations can usually be eliminated by putting a ferrite bead[8] between the emitter follower and the cable.

Considering the loop gain of an amplifier is a valuable tool in understanding the influence of various factors on the stability of feedback amplifiers. But it is not too helpful in determining if the amplifier is indeed stable. The reason is that most problems in a well-designed system are caused by secondary effects—which occur only under certain conditions of output voltage, load current, capacitive loading, temperature, etc. Making frequency-phase plots under all these conditions would require unreasonable amounts of time, so it is invariably not done.

A better check on stability is the small-signal transient response. It can be shown mathematically that the transient response of a network has a one-for-one correspondence with the frequency domain response.† The advantage of transient response tests is that they are displayed instantaneously on an oscilloscope, so it is reasonable to test a circuit under a wide range of conditions.

Exact methods of analysis using transient response will not be presented here. This is not because these methods are difficult, although they are. Instead, it is because it is very easy to determine which conditions are unfavorable from the overshoot and ringing on the step response. The stability margin can be determined much more easily by how much greater the aggravating conditions can be made before the circuit oscillates than by analysis of the response under given conditions. A little practice with this technique can quickly yield much better results than classical methods even for the inexperienced engineer.

Summary

A number of circuits using operational amplifiers have been proposed to show their versatility in circuit design. These have ranged from low frequency oscillators through circuits for complex analog computation. Because of the low cost of monolithic amplifiers, it is almost foolish to design dc amplifiers without integrated circuits. Moreover, the price makes it practical to take advantage of operational-amplifier performance in a variety of circuits where they are not normally used.

Many of the potential oscillation problems that can be encountered in both discrete and integrated operational amplifiers were described, and some conservative solutions to these problems were presented. The areas discussed included stray capacitance, capacitive loading and supply bypassing. Finally, a simplified method of quickly testing the stability of amplifier circuits over a wide range of operating conditions was suggested.

Note: †The frequency-domain characteristics can be determined from the impulse response of a network and this is directly relatable to the step response through the convolution integral

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IC Op Amp Beats FETs on Input Current

National Semiconductor
Application Note 29
Robert J. Widlar

Note: National Semiconductor recommends replacing 2N2920 and 2N3728 matched pairs with LM394 in all application circuits.

Abstract

A monolithic operational amplifier having input error currents in the order of 100 pA over a −55˚C to 125˚C temperature range is described. Instead of FETs, the circuit used bipolar transistors with current gains of 5000 so that offset voltage and drift are not degraded. A power consumption of 1 mW at low voltage is also featured.

A number of novel circuits that make use of the low current characteristics of the amplifier are given. Further, special design techniques required to take advantage of these low currents are explored. Component selection and the treatment of printed circuit boards is also covered.

Introduction

A year ago, one of the loudest complaints heard about IC op amps was that their input currents were too high. This is no longer the case. Today ICs can provide the ultimate in performance for many applications—even surpassing FET amplifiers.

FET input stages have long been considered the best way to get low input currents in an op amp. Low-picoamp input currents can in fact be obtained at room temperature. However, this current, which is the leakage current of the gate junction, doubles every 10˚C, so performance is severely degraded at high temperatures. Another disadvantage is that it is difficult to match FETs closely.[1] Unless expensive selection and trimming techniques are used, typical offset voltages of 50 mV and drifts of 50 µV/˚C must be tolerated.

Super gain transistors[2] are now challenging FETs. These devices are standard bipolar transistors which have been diffused for extremely high current gains. Typically, current gains of 5000 can be obtained at 1 µA collector currents. This makes it possible to get input currents which are competitive with FETs. It is also possible to operate these transistors at zero collector base voltage, eliminating the leakage currents that plague the FET. Hence they can provide lower error currents at elevated temperatures. As a bonus, super gain transistors match much better than FETs with typical offset voltages of 1 mV and drifts of 3 µV/˚C.

Figure 1 compares the typical input offset currents of IC op amps and FET amplifiers. Although FETs give superior performance at room temperature, their advantage is rapidly lost as temperature increases. Still, they are clearly better than early IC amplifiers like the LM709.[3] Improved devices, like the LM101A,[4] equal FET performance over a −55˚C to 125˚C temperature range. Yet they use standard transistors in the input stage. Super gain transistors can provide more than an order of magnitude improvement over the LM101A. The LM108 uses these to equal FET performance over a 0˚C to 70˚C temperature range.

In applications involving 125˚C operation, the LM108 is about two orders of magnitude better than FETs. In fact, unless special precautions are taken, overall circuit performance is often limited by leakages in capacitors, diodes, analog switches or printed circuit boards, rather than by the op amp itself.

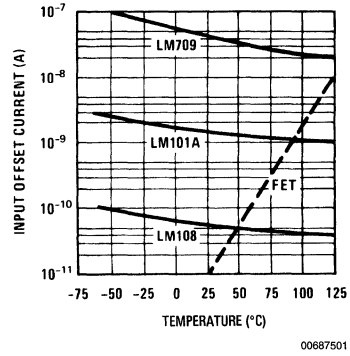


FIGURE 1. Comparing IC op Amps with FET-Input Amplifier

Effects of Error Current

In an operational amplifier, the input current produces a voltage drop across the source resistance, causing a dc error. This effect can be minimized by operating the amplifier with equal resistances on the two inputs.[5] The error is then proportional to the difference in the two input currents, or the offset current. Since the current gains of monolithic transistors tend to match well, the offset current is typically a factor of ten less than the input currents.

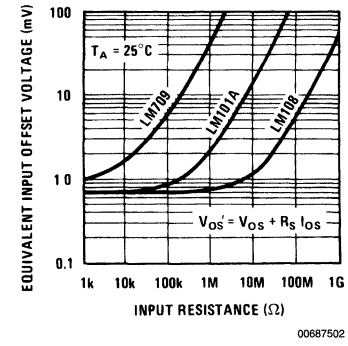


FIGURE 2. Illustrating the Effect of Source Resistance on Typical Input Error Voltage

Naturally, error current has the greatest effect in high impedance circuitry. *Figure 2* illustrates this point. The offset voltage of the LM709 is degraded significantly with source resistances greater than 10 kΩ. With the LM101A this is

Effects of Error Current (Continued)

extended to source resistances high as 500 kΩ. The LM108, on the other hand, works well with source resistances above 10 MΩ.

High source resistances have an even greater effect on the drift of an amplifier, as shown in *Figure 3*. The performance of the LM709 is worsened with sources greater than 3 kΩ. The LM101A holds out to 100 kΩ sources, while the LM108 still works well at 3 MΩ.

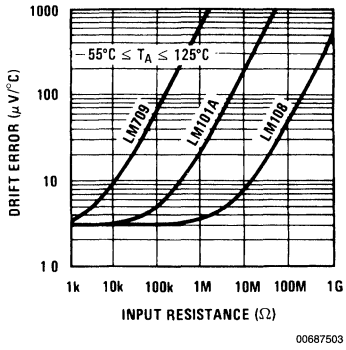


FIGURE 3. Degradation of Typical Drift Characteristics with High Source Resistances

It is difficult to include FET amplifiers in *Figure 3* because their drift is initially 50 μV/°C, unless they are selected and trimmed. Even though their drift may be well controlled (5 μV/°C) over a limited temperature range, trimmed amplifiers generally exhibit a much higher drift over a −55°C to 125°C temperature range. At any rate, their average drift rate would, at best, be like that of the LM101A where 125°C operation is involved.

Applications that require low error currents include amplifiers for photodiodes or capacitive transducers, as these usually operate at megohm impedance levels. Sample and hold circuits, timers, integrators and analog memories also benefit from low error currents For example, with the LM709, worst case drift rates for these kinds of circuits is in the order of 1.5 V/sec. The LM108 improves this to 3 mV/sec.—worst case over a −55°C to 125°C temperature range. Low input currents are also helpful in oscillators and active filters to get low frequency operation with reasonable capacitor values. The LM108 can be used at a frequency of 1 Hz with capacitors no larger than 0.01 μF. In logarithmic amplifiers, the dynamic range can be extended by nearly 60 dB by going from the LM709 to the LM108. In other applications, having low error currents often permits an entirely different design approach which can greatly simplify circuitry.

The LM108

Figure 4 shows a simplified schematic of the LM108. Two kinds of NPN transistors are used on the IC chip: super gain (primary) transistors which have a current gain of 5000 with a breakdown voltage of 4V and conventional (secondary) transistors which have a current gain of 200 with an 80V breakdown. These are differentiated on the schematic by drawing the secondaries with a wider base.

Primary transistors (Q_1 and Q_2) are used for the input stage; and they are operated in a cascode connection with Q_5 and Q_6. The bases of Q_5 and Q_6 are bootstrapped to the emitters of Q_1 and Q_2 through Q_3 and Q_4, so that the input transistors are operated at zero collector-base voltage. Hence, circuit performance is not impaired by the low breakdown of the primaries, as the secondary transistors stand off the common mode voltage. This configuration also improves the common mode rejection since the input transistors do not see variations in the common mode voltage. Further, because there is no voltage across their collector-base junctions, leakage currents in the input transistors are effectively eliminated.

The LM108 (Continued)

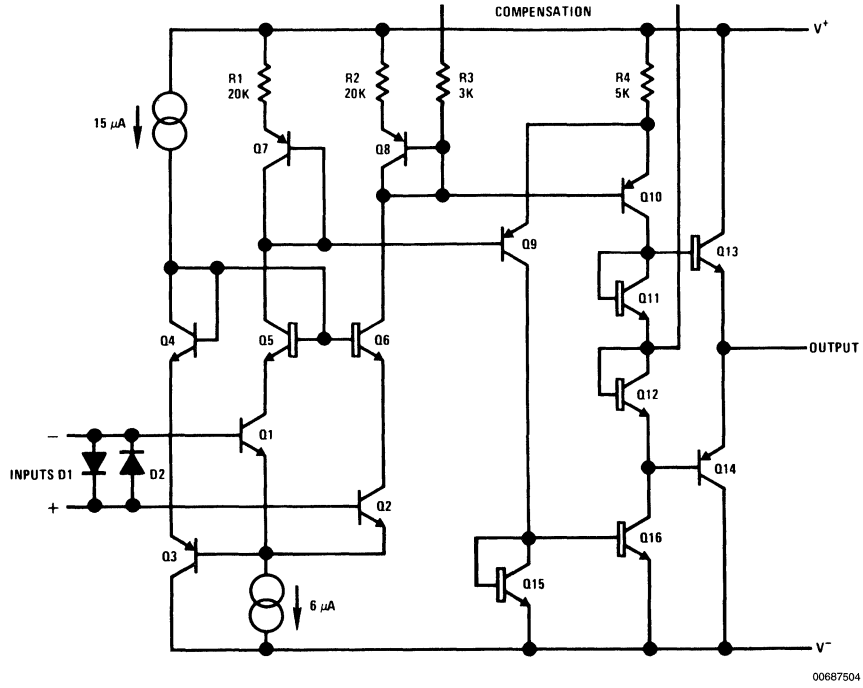


FIGURE 4. Simplified Schematic of the LM108

The second stage is a differential amplifier using high gain lateral PNPs (Q_9 and Q_{10}).[6] These devices have current gains of 150 and a breakdown voltage of 80V. R_1 and R_2 are the collector load resistors for the input stage. Q_7 and Q_8 are diode connected laterals which compensate for the emitter-base voltage of the second stage so that its operating current is set at twice that of the input stage by R_4.

The second stage uses an active collector load (Q_{15} and Q_{16}) to obtain high gain. It drives a complementary class-B output stage which gives a substantial load driving capability. The dead zone of the output stage is eliminated by biasing it on the verge of conduction with Q_{11} and Q_{12}.

Two methods of frequency compensation are available for the amplifier. In one a 30 pF capacitor is connected from the input to the output of the second stage (between the compensation terminals). This method is pin-compatible with the LM101 or LM101A. It can also be compensated by connecting a 100 pF capacitor from the output of the second stage to ground. This technique has the advantage of improving the high frequency power supply rejection by a factor of ten.

A complete schematic of the LM108 is given in the Appendix along with a description of the circuit. This includes such essential features as overload protection for the inputs and outputs.

Performance

The primary design objective for the LM108 was to obtain very low input currents without sacrificing offset voltage or drift. A secondary objective was to reduce the power consumption. Speed was of little concern, as long as it was comparable with the LM709. This is logical as it is quite difficult to make high-impedance circuits fast; and low power circuits are very resistant to being made fast. In other respects, it was desirable to make the LM108 as much like the LM101A as possible.

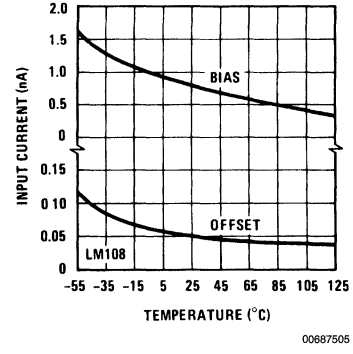


FIGURE 5. Input Currents

Figure 5 shows the input current characteristics of the LM108 over a –55°C to 125°C temperature range. Not only

Performance (Continued)

are the input currents low, but also they do not change radically over temperature. Hence, the device lends itself to relatively simple temperature compensation schemes, that will be described later.

There has been considerable discussion about using Darlington input stages rather than super gain transistors to obtain low input currents.[6,7] It is appropriate to make a few comments about that here.

Darlington inputs can give about the same input bias currents as super gain transistors—at room temperature. However, the bias current varies as the square of the transistor current gain. At low temperatures, super gain devices have a decided advantage Additionally, the offset current of super gain transistors is considerably lower than Darlingtons, when measured as a percentage of bias current. Further, the offset voltage and offset voltage drift of Darlington transistors is both higher and more unpredictable.

Experience seems to tell the real truth about Darlingtons. Quite a few op amps with Darlington input stages have been introduced. However, none have become industry standards. The reason is that they are more sensitive to variations in the manufacturing process. Therefore, satisfactory performance specifications can only be obtained by sacrificing the manufacturing yield.

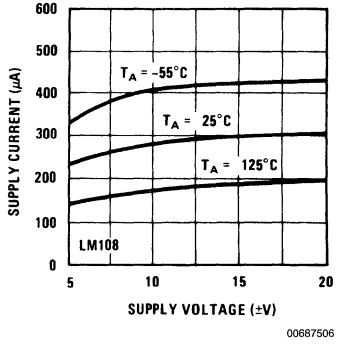


FIGURE 6. Supply Current

The supply current of the LM108 is plotted as a function of supply voltage in *Figure 6*. The operating current is about an order of magnitude lower than devices like the LM709. Furthermore, it does not vary radically with supply voltage which means that the device performance is maintained at low voltages and power consumption is held down at high voltages.

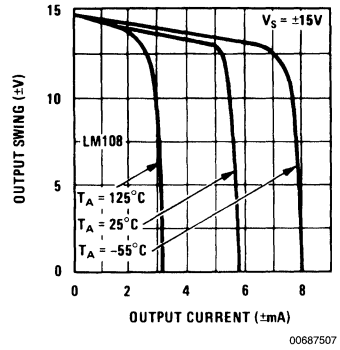


FIGURE 7. Output Swing

The output drive capability of the circuit is illustrated in *Figure 7*. The output swings to within a volt of the supplies, which is especially important when operating at low voltages. The output falls off rapidly as the current increases above a certain level and the short circuit protection goes into effect. The useful output drive is limited to about ±2 mA. It could have been increased by the addition of Darlington transistors on the output, but this would have restricted the voltage swing at low supply voltages. The amplifier, incidentally, works with common mode signals to within a volt of the supplies so it can be used with supply voltages as low as ±2V.

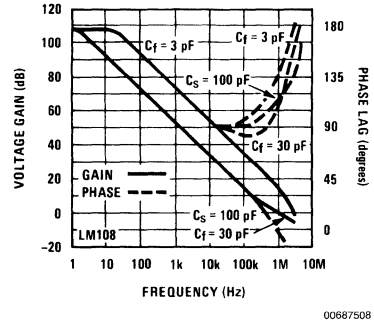
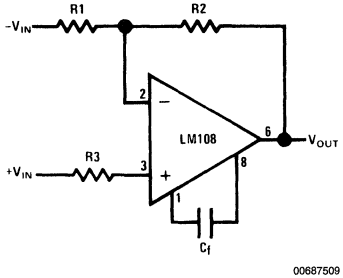


FIGURE 8. Open Loop Frequency Response

The open loop frequency response, plotted in *Figure 8*, indicates that the frequency response is about the same as

Performance (Continued)

that of the LM709 or the LM101A. Curves are given for the two compensation circuits shown in *Figure 9*. The standard compensation is identical to that of the LM101 or LM101A. The alternate compensation scheme gives much better rejection of high frequency power supply noise, as will be shown later.



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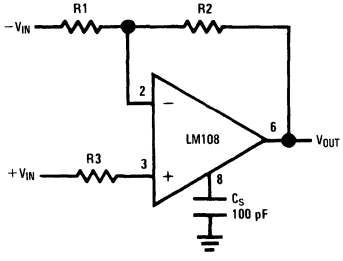
$$C_f \geq \frac{R1\ C_o}{R1 + R2}$$

C_o = 30 pF

a. Standard Compensation Circuit



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b. Alternate Compensation Circuit

FIGURE 9. Compensation Circuits

With unity gain compensation, both methods give a 75-degree stability margin. However, the shunt compensation has a 300 kHz small signal bandwidth as opposed to 1 MHz for the other scheme. Because the compensation capacitor is not included on the IC chip, it can be tailored to fit the application. When the amplifier is used only at low frequencies, the compensation capacitor can be increased to give a greater stability margin. This makes the circuit less sensitive to capacitive loading, stray capacitances or improper supply bypassing. Overcompensating also reduces the high frequency noise output of the amplifier.

With closed-loop gains greater than one, the high frequency performance can be optimized by making the compensation capacitor smaller. If unity-gain compensation is used for an amplifier with a gain of ten, the gain error will exceed 1-percent at frequencies above 400 Hz. This can be extended to 4 kHz by reducing the compensation capacitor to 3 pF. The formula for determining the minimum capacitor value is given in *Figure 9a*. It should be noted that the capacitor value does not really depend on the closed-loop gain. Instead, it depends on the high frequency attenuation in the feedback networks and, therefore, the values of R_1 and R_2. When it is desirable to optimize performance at high frequencies, the standard compensation should be used. With small capacitor values, the stability margin obtained with shunt compensation is inadequate for conservative designs.

The frequency response of an operational amplifier is considerably different for large output signals than it is for small signals. This is indicated in *Figure 10*. With unity-gain compensation, the small signal bandwidth of the LM108 is 1 MHz. Yet full output swing cannot be obtained above 2 kHz. This corresponds to a slew rate of 0.3 V/µs. Both the full-output bandwidth and the slew rate can be increased by using smaller compensation capacitors, as is indicated in the figure. However, this is only applicable for higher closed loop gains. The results plotted in *Figure 10* are for standard compensations. With unity gain compensation, the same curves are obtained for the shunt compensation scheme.

Classical op amp theory establishes output resistance as an important design parameter. This is not true for IC op amps: The output resistance of most devices is low enough that it can be ignored, because they use class-B output stages. At low frequencies, thermal feedback between the output and input stages determines the effective output resistance, and this cannot be accounted for by conventional design theories. Semiconductor manufacturers take care of this by specifying the gain under full load conditions, which combines output resistance with gain as far as it affects overall circuit performance. This avoids the fictitious problem that can be created by an amplifier with infinite gain, which is good, that will cause the open loop output resistance to appear infinite, which is bad, although none of this affects overall performance significantly.

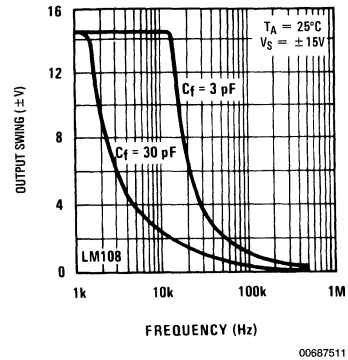

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FIGURE 10. Large Signal Frequency Response

Performance (Continued)

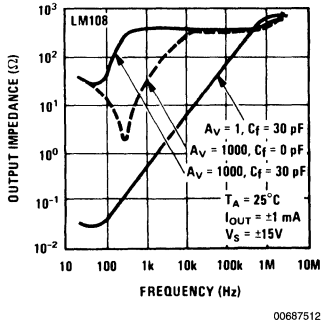


FIGURE 11. Closed Loop Output Impedance

The *closed loop* output impedance is, nonetheless, important in some applications. This is plotted for several operating conditions in *Figure 11*. It can be seen that the output impedance rises to about 500Ω at high frequencies. The increase occurs because the compensation capacitor rolls off the open loop gain. The output resistance can be reduced at the intermediate frequencies, for closed loop gains greater than one, by making the capacitor smaller. This is made apparent in the figure by comparing the output resistance with and without frequency compensation for a closed loop gain of 1000.

The output resistance also tends to increase at low frequencies. Thermal feedback is responsible for this phenomenon. The data for *Figure 11* was taken under large-signal conditions with ±15V supplies, the output at zero and ±1 mA current swing. Hence, the thermal feedback is accentuated more than would be the case for most applications.

In an op amp, it is desirable that performance be unaffected by variations in supply voltage. IC amplifiers are generally better than discretes in this respect because it is necessary for one single design to cover a wide range of uses. The LM108 has a power supply rejection which is typically in excess of 100 dB, and it will operate with supply voltages from ±2V to ±20V. Therefore, well-regulated supplies are unnecessary, for most applications, because a 20-percent variation has little effect on performance.

The story is different for high-frequency noise on the supplies, as is evident from *Figure 12*. Above 1 MHz, practically all the noise is fed through to the output. The figure also demonstrates that shunt compensation is about ten times better at rejecting high frequency noise than is standard compensation. This difference is even more pronounced with larger capacitor values. The shunt compensation has the added advantage that it makes the circuit virtually unaffected by the lack of supply bypassing.

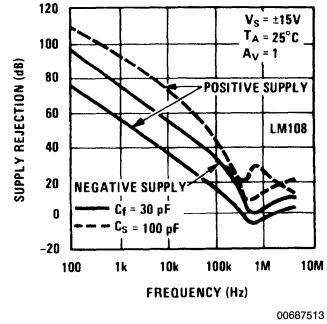


FIGURE 12. Power Supply Rejection

Power supply rejection is defined as the ratio of the change in offset voltage to the change in the supply voltage producing it. Using this definition, the rejection at low frequencies is unaffected by the closed loop gain. However, at high frequencies, the opposite is true. The high frequency rejection is increased by the closed loop gain. Hence, an amplifier with a gain of ten will have an order of magnitude better rejection than that shown in *Figure 12* in the vicinity of 100 kHz to 1 MHz.

The overall performance of the LM108 is summarized in *Table 1**. It is apparent from the table and the previous discussion that the device is ideally suited for applications that require low input currents or reduced power consumption. The speed of the amplifier is not spectacular, but this is not usually a problem in high-impedance circuitry. Further, the reduced high frequency performance makes the amplifier easier to use in that less attention need be paid to capacitive loading, stray capacitances and supply bypassing.

Note: *See Appendix Heading in This Application Note

Applications

Because of its low input current the LM108 opens up many new design possibilities. However, extra care must be taken in component selection and the assembly of printed circuit boards to take full advantage of its performance. Further, unusual design techniques must often be applied to get around the limitations of some components.

Sample and Hold Circuits

The holding accuracy of a sample and hold is directly related to the error currents in the components used. Therefore, it is a good circuit to start off with in explaining the problems involved. *Figure 13* shows one configuration for a sample and hold. During the sample interval, Q_1 is turned on, charging the hold capacitor, C_1, up to the value of the input signal.

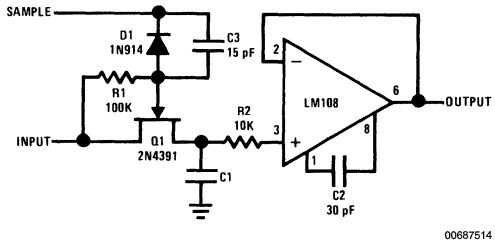


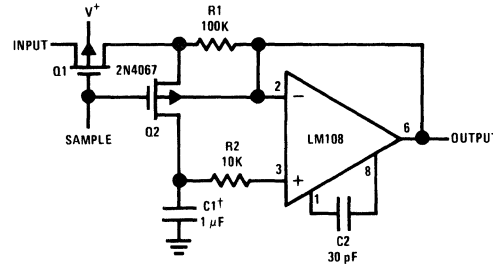
FIGURE 13. Sample and Hold Circuit

When Q_1 is turned off, C_1 retains this voltage. The output is obtained from an op amp that buffers the capacitor so that it is not discharged by any loading. In the holding mode, an error is generated as the capacitor looses charge to supply circuit leakages. The accumulation rate for error is given by

$$\frac{dV}{dt} = \frac{I_E}{C_1},$$

where dV/dt is the time rate of change in output voltage and I_E is the sum of the input current to the op amp, the leakage current of the holding capacitor, board leakages and the "off" current of the FET switch.

When high-temperature operation is involved, the FET leakage can limit circuit performance. This can be minimized by using a junction FET, as indicated, because commercial junction FETs have lower leakage than their MOS counterparts. However, at 125°C even junction devices are a problem. Mechanical switches, such as read relays, are quite satisfactory from the standpoint of leakage. However, they are often undesirable because they are sensitive to vibration, they are too slow or they require excessive drive power. If this is the case, the circuit in *Figure 14* can be used to eliminate the FET leakage.



†Teflon, polyethylene or polycarbonate dielectric capacitor

Worst case drift less than 3 mV/sec

FIGURE 14. Sample and Hold that Eliminates Leakage in FET Switches

When using P-channel MOS switches, the substrate must be connected to a voltage which is always more positive than the input signal. The source-to-substrate junction becomes forward biased if this is not done. The troublesome leakage current of a MOS device occurs across the substrate-to-drain junction. In *Figure 14*, this current is routed to the output of the buffer amplifier through R_1 so that it does not contribute to the error current.

The main sample switch is Q_1, while Q_2 isolates the hold capacitor from the leakage of Q_1. When the sample pulse is applied, both FETs turn on charging C_1 to the input voltage. Removing the pulse shuts off both FETs, and the output leakage of Q_1 goes through R_1 to the output. The voltage drop across R_1 is less than 10 mV, so the substrate of Q_2 can be bootstrapped to the output of the LM108. Therefore, the voltage across the substrate-drain junction is equal to the offset voltage of the amplifier. At this low voltage, the leakage of the FET is reduced by about two orders of magnitude.

It is necessary to use MOS switches when bootstrapping the leakages in this fashion. The gate leakage of a MOS device is still negligible at high temperatures; this is not the case with junction FETs. If the MOS transistors have protective diodes on the gates, special arrangements must be made to drive Q_2 so the diode does not become forward biased.

In selecting the hold capacitor, low leakage is not the only requirement. The capacitor must also be free of dielectric

Sample and Hold Circuits (Continued)

polarization phenomena.[8] This rules out such types as paper, mylar, electrolytic, tantalum or high-K ceramic. For small capacitor values, glass or silvered-mica capacitors are recommended. For the larger values, ones with teflon, polyethylene or polycarbonate dielectrics should be used.

The low input current of the LM108 gives a drift rate, in hold, of only 3 mV/sec when a 1 µF hold capacitor is used. And this number is worst case over the military temperature range Even if this kind of performance is not needed, it may still be beneficial to use the LM108 to reduce the size of the hold capacitor. High quality capacitors in the larger sizes are bulky and expensive. Further, the switches must have a low "on" resistance and be driven from a low impedance source to charge large capacitors in a short period of time.

If the sample interval is less than about 100 µs, the LM108 may not be fast enough to work properly. If this is the case, it is advisable to substitute the LM102A,[9] which is a voltage follower designed for both low input current and high speed. It has a 30 V/µs slew rate and will operate with sample intervals as short as 1 µs.

When the hold capacitor is larger than 0.05 µF, an isolation resistor should be included between the capacitor and the input of the amplifier (R_2 in *Figure 14*). This resistor insures that the IC will not be damaged by shorting the output or abruptly shutting down the supplies when the capacitor is charged. This precaution is not peculiar to the LM108 and should be observed on any IC op amp.

Integrators

Integrators are a lot like sample-and-hold circuits and have essentially the same design problems In an integrator, a capacitor is used as a storage element; and the error accumulation rate is again proportional to the input current of the op amp.

Figure 15 shows a circuit that can compensate for the bias current of the amplifier. A current is fed into the summing node through R_1 to supply the bias current. The potentiometer, R_2, is adjusted so that this current exactly equals the bias current, reducing the drift rate to zero.

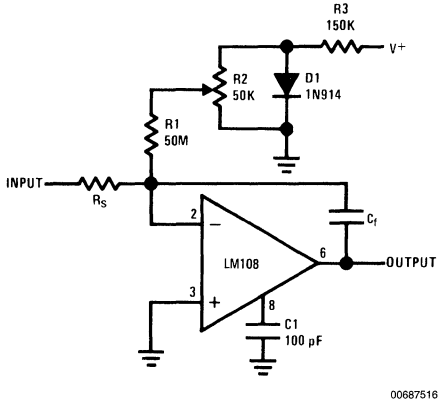
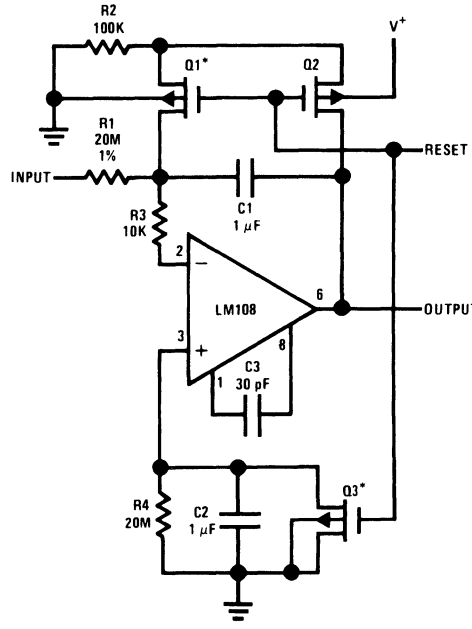


FIGURE 15. Integrator with Bias Current Compensation

The diode is used for two reasons. First, it acts as a regulator, making the compensation relatively insensitive to variations in supply voltage. Secondly, the temperature drift of diode voltage is approximately the same as the temperature drift of bias current. Therefore, the compensation is more effective if the temperature changes. Over a 0°C to 70°C temperature range, the compensation will give a factor of ten reduction in input current. Even better results are achieved if the temperature change is less.

Normally, it is necessary to reset an integrator to establish the initial conditions for integration. Resetting to zero is readily accomplished by shorting the integrating capacitor with a suitable switch. However, as with the sample and hold circuits, semiconductor switches can cause problems because of high-temperature leakage.

A connection that gets rid of switch leakages is shown in *Figure 16*. A negative-going reset pulse turns on Q_1 and Q_2, shorting the integrating capacitor. When the switches turn off, the leakage current of Q_2 is absorbed by R_2 while Q_1 isolates the output of Q_2 from the summing node. Q_1 has practically no voltage across its junctions because the substrate is grounded; hence, leakage currents are negligible.



*Q1 and Q3 should not have internal gate-protection diodes

FIGURE 16. Low Drift Integrator with Reset

The additional circuitry shown in *Figure 16* makes the error accumulation rate proportional to the offset current, rather than the bias current. Hence, the drift is reduced by roughly a factor of 10. During the integration interval, the bias current of the non-inverting input accumulates an error across R_4 and C_2 just as the bias current on the inverting input does across R_1 and C_1. Therefore, if R_4 is matched with R_1 and C_2 is matched with C_1 (within about 5 percent) the output will

Integrators (Continued)

drift at a rate proportional to the difference in these currents. At the end of the integration interval, Q_3 removes the compensating error accumulated on C_2 as the circuit is reset.

In applications involving large temperature changes, the circuit in *Figure 16* gives better results than the compensation scheme in *Figure 15*—especially under worst case conditions. Over a −55˚C to 125˚C temperature range, the worst case drift is reduced from 3 mV/sec to 0.5 mV/sec when a 1 µF integrating capacitor is used. If this reduction in drift is not needed, the circuit can be simplified by eliminating R_4, C_2 and Q_3 and returning the non-inverting input of the amplifier directly to ground.

In fabricating low drift integrators, it is again necessary to use high quality components and minimize leakage currents in the wiring. The comments made on capacitors in connection with the sample-and-hold circuits also apply here. As an additional precaution, a resistor should be used to isolate the inverting input from the integrating capacitor if it is larger than 0.05 µF. This resistor prevents damage that might occur when the supplies are abruptly shut down while the integrating capacitor is charged.

Some integrator applications require both speed and low error current. The output amplifiers for photomultiplier tubes or solid-state radiation dectectors are examples of this. Although the LM108 is relatively slow, there is a way to speed it up when it is used as an inverting amplifier. This is shown in *Figure 17*.

The circuit is arranged so that the high-frequency gain characteristics are determined by A_2, while A_1 determines the dc and low-frequency characteristics. The non-inverting input of A_1 is connected to the summing node through R_1. A_1 is operated as an integrator, going through unity gain at 500 Hz. Its output drives the non-inverting input of A_2. The inverting input of A_2 is also connected to the summing node through C_3. C_3 and R_3 are chosen to roll off below 750 Hz. Hence, at frequencies above 750 Hz, the feedback path is directly around A_2, with A_1 contributing little. Below 500 Hz, however, the direct feedback path to A_2 rolls off; and the gain of A_1 is added to that of A_2.

The high gain frequency amplifier, A_2, is an LM101A connected with feed-forward compensation.[10] It has a 10 MHz equivalent small-signal bandwidth, a 10V/µs slew rate and a 250 kHz large-signal bandwidth, so these are the high-frequency characteristics of the complete amplifier. The bias current of A_2 is isolated from the summing node by C_3. Hence, it does not contribute to the dc drift of the integrator. The inverting input of A_1 is the only dc connection to the summing junction. Therefore, the error current of the composite amplifier is equal to the bias current of A_1.

If A_2 is allowed to saturate, A_1 will then start towards saturation. If the output of A_1 gets far off zero, recovery from saturation will be slowed drastically. This can be prevented by putting zener clamp diodes across the integrating capacitor. A suitable clamping arrangement is shown in *Figure 17*. D_1 and D_2 are included in the clamp circuit along with R_5 to keep the leakage currents of the zeners from introducing errors.

In addition to increasing speed, this circuit has other advantages. For one, it has the increased output drive capability of the LM101A. Further, thermal feedback is virtually eliminated because the LM108 does not see load variations. Lastly, the open loop gain is nearly infinite at low frequencies as it is the product of the gains of the two amplifiers.

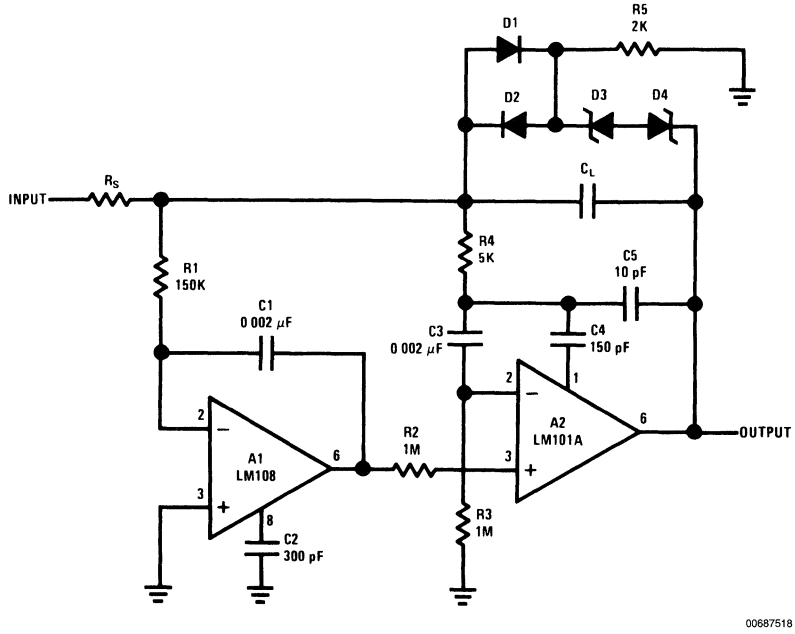


FIGURE 17. Fast Integrator

Integrators (Continued)

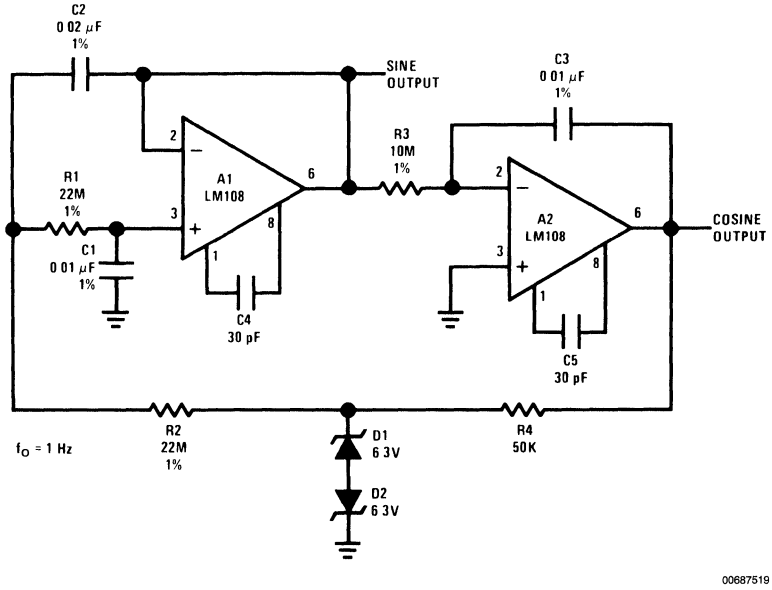


FIGURE 18. Sine Wave Oscillator

Sine Wave Oscillator

Although it is comparatively easy to build an oscillator that approximates a sine wave, making one that delivers a high-purity sinusoid with a stable frequency and amplitude is another story. Most satisfactory designs are relatively complicated and require individual trimming and temperature compensation to make them work. In addition, they generally take a long time to stabilize to the final output amplitude.

A unique solution to most of these problems is shown in *Figure 18*. A_1 is connected as a two-pole low-pass active filter, and A_2 is connected as an integrator. Since the ultimate phase lag introduced by the amplifiers is 270 degrees, the circuit can be made to oscillate if the loop gain is high enough at the frequency where the lag is 180 degrees. The gain is actually made somewhat higher than is required for oscillation to insure starting. Therefore, the amplitude builds up until it is limited by some nonlinearity in the system.

Amplitude stabilization is accomplished with zener clamp diodes, D_1 and D_2. This does introduce distortion, but it is reduced by the subsequent low pass filters. If D_1 and D_2 have equal breakdown voltages, the resulting symmetrical clipping will virtually eliminate the even-order harmonics. The dominant harmonic is then the third, and this is about 40 dB down at the output of A_1 and about 50 dB down on the output of A_2. This means that the total harmonic distortion on the two outputs is 1 percent and 0.3 percent, respectively.

The frequency of oscillation and the oscillation threshold are determined by R_1, R_2, R_3, C_1, C_2 and C_3. Therefore precision components with low temperature coefficients should be used. If R_3 is made lower than shown, the circuit will accept looser component tolerances before dropping out of oscillation. The start up will also be quicker. However, the price paid is that distortion is increased. The value of R_4 is not critical, but it should be made much smaller than R_2 so that the effective resistance at R_2 does not drop when the clamp diodes conduct.

The output amplitude is determined by the breakdown voltages of D_1 and D_2. Therefore, the clamp level should be temperature compensated for stable operation. Diode-connected (collector shorted to base) NPN transistors with an emitter-base breakdown of about 6.3V work well, as the positive temperature coefficient of the diode in reverse breakdown nearly cancels the negative temperature coefficient of the forward-biased diode. Added advantages of using transistors are that they have less shunt capacitance and sharper breakdowns than conventional zeners.

The LM108 is particularly useful in this circuit at low frequencies, since it permits the use of small capacitors. The circuit shown oscillates at 1 Hz, but uses capacitors in the order of 0.01 µF. This makes it much easier to find temperature-stable precision capacitors. However, some judgment must be used as large value resistors with low temperature coefficients are not exactly easy to come by.*

The LM108s are useful in this circuit for output frequencies up to 1 kHz. Beyond that, better performance can be realized by substituting and LM102A for A_1 and an LM101A with feed-forward compensation for A_2. The improved high-frequency response of these devices extend the operating frequency out to 100 kHz.

Note: *Large-value resistors are available from Victoreen Instrument, Cleveland, Ohio and Pyrofilm Resistor Co , Whippany, New Jersey

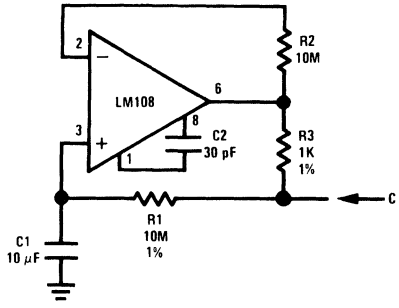
Capacitance Multiplier

Large capacitor values can be eliminated from most systems just by raising the impedance levels, if suitable op amps are available. However, sometimes it is not possible because the

Capacitance Multiplier (Continued)

impedance levels are already fixed by some element of the system like a low impedance transducer. If this is the case, a capacitance multiplier can be used to increase the effective capacitance of a small capacitor and couple it into a low impedance system.

Previously, IC op amps could not be used effectively as capacitance multipliers because the equivalent leakages generated due to offset current were significantly greater than the leakages of large tantalum capacitors. With the LM108, this has changed. The circuit shown in *Figure 19* generates an equivalent capacitance of 100,000 µF with a worst case leakage of 8 µA—over a –55˚C to 125˚C temperature range.



$$C = \frac{R1}{R3} C1$$

$$I_L = \frac{V_{OS} + I_{OS} R1}{R3}$$

$$R_S = R3$$

FIGURE 19. Capacitance Multiplier

The performance of the circuit is described by the equations given in *Figure 19*, where C is the effective output capacitance, I_L is the leakage current of this capacitance and R_S is the series resistance of the multiplied capacitance. The series resistance is relatively high, so high-Q capacitors cannot be realized. Hence, such applications as tuned circuits and filters are ruled out. However, the multiplier can still be used in timing circuits or servo compensation networks where some resistance is usually connected in series with the capacitor or the effect of the resistance can be compensated for.

One final point is that the leakage current of the multiplied capacitance is not a function of the applied voltage. It persists even with no voltage on the output. Therefore, it can generate offset errors in a circuit, rather than the scaling errors caused by conventional capacitors.

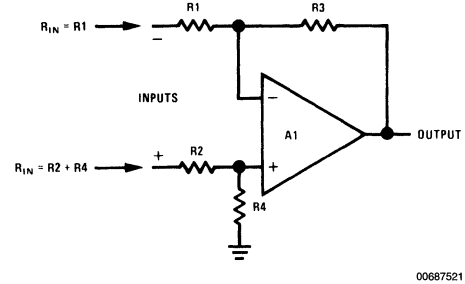
Instrumentation Amplifier

In many instrumentation applications there is frequently a need for an amplifier with a high-impedance differential input and a single ended output. Obvious uses for this are amplifiers for bridge-type signal sources such as strain gages, temperature sensors or pressure transducers. General purpose op amps have satisfactory input characteristics, but feedback must be added to determine the effective gain. And the addition of feedback can drastically reduce the input resistance and degrade common mode rejection.

Figure 20 shows the classical op amp circuit for a differential amplifier. This circuit has three main disadvantages. First, the input resistance on the inverting input is relatively low, being equal to R_1. Second, there usually is a large difference in the input resistance of the two inputs, as is indicated by the equations on the schematic. Third, the common mode rejection is greatly affected by resistor matching and by balancing of the source resistances. A 1-percent deviation in any one of the resistor values reduces the common mode rejection to 46 dB for a closed loop gain of 1, to 60 dB for a gain of 10 and to 80 dB for a gain of 100.

Clearly, the only way to get high input impedance is to use very large resistors in the feedback network. The op amp must operate from a source resistance which is orders of magnitude larger than the resistance of the signal source. Older IC op amps introduced excessive offset and drift when operating from higher resistances and could not be used successfully. The LM108, however, is relatively unaffected by the large resistors, so this approach can sometimes be employed.

With large input resistors, the feedback resistors, R_3 and R_4, can get quite large for higher closed loop gains. For example, if R_1 and R_2 are 1 MΩ, R_3 and R_4 must be 100 MΩ for a gain of 100. It is difficult to accurately match resistors that are this high in value, so common mode rejection may suffer. Nonetheless, any one of the resistors can be trimmed to take out common mode feedthrough caused either by resistors mismatches or the amplifier itself.



$$R1 = R2$$

$$R3 = R4$$

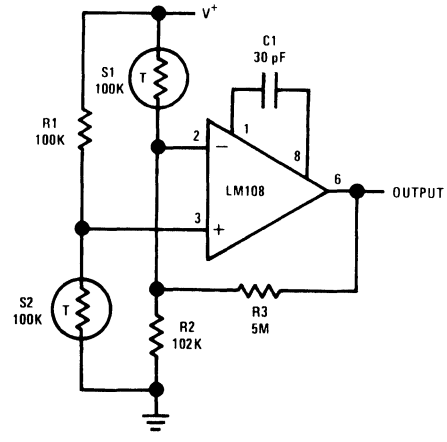
$$A_V = \frac{R3}{R1}$$

FIGURE 20. Feedback Connection for a Differential Amplifier

Another problem caused by large feedback resistors is that stray capacitance can seriously affect the high frequency common mode rejection. With 1 MΩ input resistors, a 1 pF mismatch in stray capacitance from either input to ground can drop the common mode rejection to 40 dB at 1500 Hz. The high frequency rejection can be improved at the expense of frequency response by shunting R_3 and R_4 with matched capacitors.

Instrumentation Amplifier (Continued)

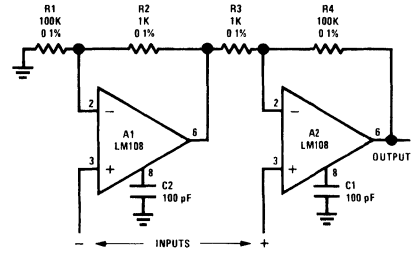
With high impedance bridges, the feedback resistances become prohibitively large even for the LM108, so the circuit in *Figure 20* cannot be used. One possible alternative is shown in *Figure 21*. R_2 and R_3 are chosen so that their equivalent parallel resistance is equal to R_1. Hence, the output of the amplifier will be zero when the bridge is balanced.



R1 = R2 || R3

FIGURE 21. Amplifier for Bridge Transducers

When the bridge goes off balance, the op amp maintains the voltage between its input terminals at zero with current fed back from the output through R_3. This circuit does not act like a true differential amplifier for large imbalances in the bridge. The voltage drops across the two sensor resistors, S_1 and S_2, become unequal as the bridge goes off balance, causing some non-linearity in the transfer function. However, this is not usually objectionable for small signal swings.



$R1 = R4$

$R2 = R3$

$A_V = 1 + \frac{R1}{R2}$

FIGURE 22. Differential Input Instrumentation Amplifier

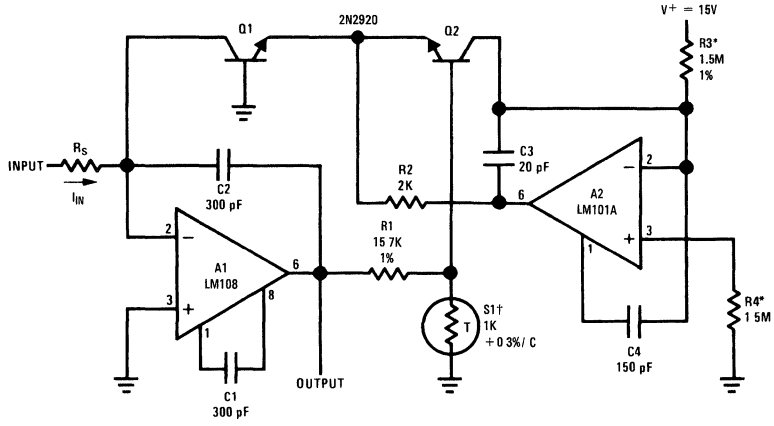
Figure 22 shows a true differential connection that has few of the problems mentioned previously. It has an input resistance greater than $10^{10}\Omega$, yet it does not need large resistors in the feedback circuitry. With the component values shown, A_1 is connected as a non-inverting amplifier with a gain of 1 01; and it feeds into A_2 which has an inverting gain of 100. Hence, the total gain from the input of A_1 to the output of A_2 is 101, which is equal to the non-inverting gain of A_2. If all the resistors are matched, the circuit responds only to the differential input signal—not the common mode voltage.

This circuit has the same sensitivity to resistor matching as the previous circuits, with a 1 percent mismatch between two resistors lowering the common mode rejection to 80 dB. However, matching is more easily accomplished because of the lower resistor values. Further, the high frequency common mode rejection is less affected by stray capacitances. The high frequency rejection is limited, though, by the response of A_1

Logarithmic Converter

A logarithmic amplifier is another circuit that can take advantage of the low input current of an op amp to increase dynamic range. Most practical log converters make use of the logarithmic relationship between the emitter-base voltage of standard double-diffused transistors and their collector current. This logarithmic characteristic has been proven true for over 9 decades of collector current. The only problem involved in using transistors as logging elements is that the scale factor has a temperature sensitivity of 0.3 percent/°C. However, temperature compensating resistors have been developed to compensate for this characteristic, making possible log converters that are accurate over a wide temperature range.

Logarithmic Converter (Continued)



10 nA < I_{IN} < 1 mA

Sensitivity is 1V per decade.

†1 kΩ (±1%) at 25°C, +3500 ppm/°C

Available from Vishay Ultronix, Grand Junction, CO, Q81 Series

*Determines current for zero crossing on output. 10 µA as shown

FIGURE 23. Temperature Compensated One-Quadrant Logarithmic Converter

Figure 23 gives a circuit that uses these techniques. Q_1 is the logging transistor, while Q_2 provides a fixed offset to temperature compensate the emitter-base turn on voltage of Q_1. Q_2 is operated at a fixed collector current of 10 µA by A_2, and its emitter-base voltage is subtracted from that of Q_1 in determining the output voltage of the circuit. The collector current of Q_2 is established by R_3 and V^+ through A_2.

The collector current of Q_1 is proportional to the input current through R_s and, therefore, proportional to the input voltage. The emitter-base voltage of Q_1 varies as the log of the input voltage. The fixed emitter-base voltage of Q_2 subtracts from the voltage on the emitter of Q_1 in determining the voltage on the top end of the temperature-compensating resistor, S_1.

The signal on the top of S_1 will be zero when the input current is equal to the current through R_3 at any temperature. Further, this voltage will vary logarithmically for changes in input current, although the scale factor will have a temperature coefficient of –0.3%/°C. The output of the converter is essentially multiplied by the ratio of R_1 to S_1. Since S_1 has a positive temperature coefficient of 0.3 %/°C, it compensates for the change in scale factor with temperature.

In this circuit, an LM101A with feedforward compensation is used for A_2 since it is much faster than the LM108 used for A_1. Since both amplifiers are cascaded in the overall feedback loop, the reduced phase shift through A_2 insures stability.

Certain things must be considered in designing this circuit. For one, the sensitivity can be changed by varying R_1. But R_1 must be made considerably larger than the resistance of S_1 for effective temperature compensation of the scale factor. Q_1 and Q_2 should also be matched devices in the same package, and S_1 should be at the same temperature as these transistors. Accuracy for low input currents is determined by the error caused by the bias current of A_1. At high currents, the behavior of Q_1 and Q_2 limits accuracy. For input currents approaching 1 mA, the 2N2920 develops logging errors in excess of 1 percent. If larger input currents are anticipated, bigger transistors must be used; and R_2 should be reduced to insure that A_2 does not saturate.

Transducer Amplifiers

With certain transducers, accuracy depends on the choice of the circuit configuration as much as it does on the quality of the components. The amplifier for photodiode sensors, shown in *Figure 24*, illustrates this point. Normally, photodiodes are operated with reverse voltage across the junction. At high temperatures, the leakage currents can approach the signal current. However, photodiodes deliver a short-circuit output current, unaffected by leakage currents, which is not significantly lower than the output current with reverse bias.

Transducer Amplifiers (Continued)

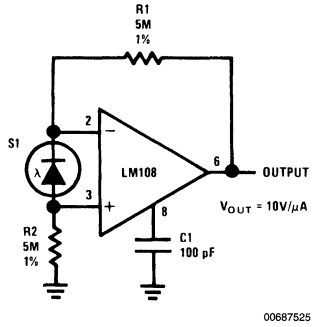


FIGURE 24. Amplifier for Photodiode Sensor

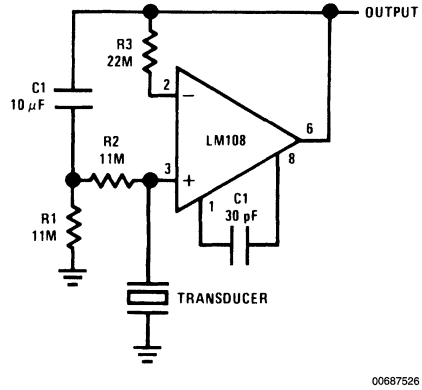


FIGURE 25. Amplifier for Piezoelectric Transducers

The circuit shown in *Figure 24* responds to the short-circuit output current of the photodiode. Since the voltage across the diode is only the offset voltage of the amplifier, inherent leakage is reduced by at least two orders of magnitude. Neglecting the offset current of the amplifier, the output current of the sensor is multiplied by R_1 plus R_2 in determining the output voltage.

Figure 25 shows an amplifier for high-impedance ac transducers like a piezoelectric accelerometer. These sensors normally require a high-input-resistance amplifier. The LM108 can provide input resistances in the range of 10 to 100 MΩ, using conventional circuitry. However, conventional designs are sometimes ruled out either because large resistors cannot be used or because prohibitively large input resistances are needed.

Using the circuit in *Figure 25*, input resistances that are orders of magnitude greater than the values of the dc return resistors can be obtained. This is accomplished by bootstrapping the resistors to the output. With this arrangement, the lower cutoff frequency of a capacitive transducer is determined more by the RC product of R_1 and C_1 than it is by resistor values and the equivalent capacitance of the transducer.

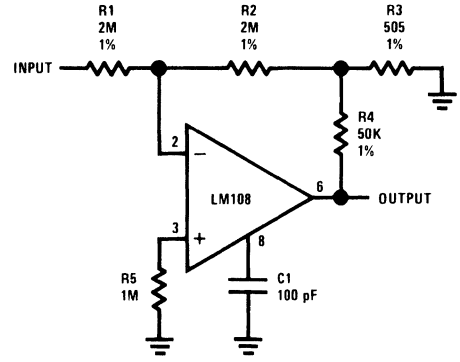
Resistance Multiplication

When an inverting operational amplifier must have high input resistance, the resistor values required can get out of hand. For example, if a 2 MΩ input resistance is needed for an amplifier with a gain of 100, a 200 MΩ feedback resistor is called for. This resistance can, however, be reduced using the circuit in *Figure 26*. A divider with a ratio of 100 to 1 (R_3 and R_4) is added to the output of the amplifier: Unity-gain feedback is applied from the output of the divider, giving an overall gain of 100 using only 2 MΩ resistors.

This circuit does increase the offset voltage somewhat. The output offset voltage is given by

$$V_{OUT} = \left(\frac{R_1 + R_2}{R_2}\right) A_V V_{os}.$$

The offset voltage is only multiplied by A_V +1 in a conventional inverter. Therefore, the circuit in *Figure 26* multiplies the offset by 200, instead of 101. This multiplication factor can be reduced to 110 by increasing R_2 to 20 MΩ and R_3 to 5.55k.



R2 > R1

R2 >> R3

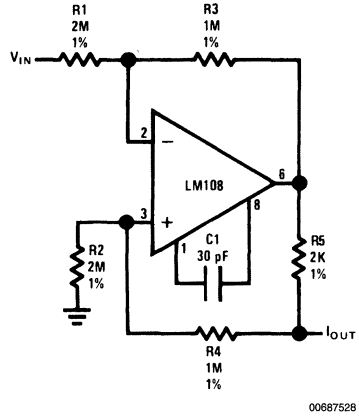
$$A_V = \frac{R2\,(R3 + R4)}{R1\,R3}$$

FIGURE 26. Inverting Amplifier with High Input Resistance

Another disadvantage of the circuit is that four resistors determine the gain, instead of two. Hence, for a given resistor tolerance, the worst-case gain deviation is greater, although this is probably more than offset by the ease of getting better tolerances in the low resistor values.

Current Sources

Although there are numerous ways to make current sources with op amps, most have limitations as far as their application is concerned. *Figure 27*, however, shows a current source which is fairly flexible and has few restrictions as far as its use is concerned. It supplies a current that is proportional to the input voltage and drives a load referred to ground or any voltage within the output-swing capability of the amplifier.



$$I_{OUT} = \frac{R3\ V_{IN}}{R1\ R5}$$

$R3 = R4 + R5$

$R1 = R2$

FIGURE 27. Bilateral Current Source

With the output grounded, it is relatively obvious that the output current will be determined by R_5 and the gain setting of the op amp, yielding

$$I_{OUT} = -\frac{R_3\ V_{IN}}{R_1\ R_5}.$$

When the output is not at zero, it would seem that the current through R_2 and R_4 would reduce accuracy. Nonetheless, if $R_1 = R_2$ and $R_3 = R_4 + R_5$, the output current will be independent of the output voltage. For $R_1 + R_3 \gg R_5$, the output resistance of the circuit is given by

$$R_{OUT} \cong R_5 \left(\frac{R}{\Delta R}\right)$$

where R is any one of the feedback resistors (R_1, R_2, R_3 or R_4) and ΔR is the incremental change in the resistor value from design center. Hence, for the circuit in *Figure 27*, a 1 percent deviation in one of the resistor values will drop the output resistance to 200 kΩ. Such errors can be trimmed out by adjusting one of the feedback resistors. In design, it is advisable to make the feedback resistors as large as possible. Otherwise, resistor tolerances become even more critical.

The circuit must be driven from a source resistance which is low by comparison to R_1, since this resistance will imbalance the circuit and affect both gain and output resistance. As shown, the circuit gives a negative output current for a positive input voltage. This can be reversed by grounding the input and driving the ground end of R_2. The magnitude of the scale factor will be unchanged as long as $R_4 \gg R_5$.

Voltage Comparators

Like most op amps, it is possible to use the LM108 as a voltage comparator. *Figure 28* shows the device used as a simple zero-crossing detector. The inputs of the IC are protected internally by back-to-back diodes connected between them, therefore, voltages in excess of 1V cannot be impressed directly across the inputs. This problem is taken care of by R_1 which limits the current so that input voltages in excess of 1 kV can be tolerated. If absolute accuracy is required or if R_1 is made much larger than 1 MΩ, a compensating resistor of equal value should be inserted in series with the other input.

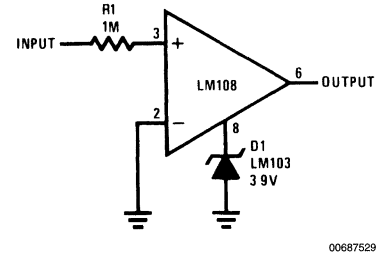


FIGURE 28. Zero Crossing Detector

In *Figure 28*, the output of the op amp is clamped so that it can drive DTL or TTL directly. This is accomplished with a clamp diode on pin 8. When the output swings positive, it is clamped at the breakdown voltage of the zener. When it swings negative, it is clamped at a diode drop below ground. If the 5V logic supply is used as a positive supply for the amplifier, the zener can be replaced with an ordinary silicon diode. The maximum fan out that can be handled by the device is one for standard DTL or TTL under worst case conditions.

As might be expected, the LM108 is not very fast when used as a comparator. The response time is up in the tens of microseconds. An LM103[11] is recommended for D_1, rather than a conventional alloy zener, because it has lower capacitance and will not slow the circuit further. The sharp breakdown of the LM103 at low currents is also an advantage as the current through the diode in clamp is only 10 µA.

Figure 29 shows a comparator for voltages of opposite polarity. The output changes state when the voltage on the junction of R_1 and R_2 is equal to V_{TH}. Mathematically, this is expressed by

$$V_{TH} = V_2 + \frac{R_2\ (V_1 - V_2)}{R_1 + R_2}.$$

Voltage Comparators (Continued)

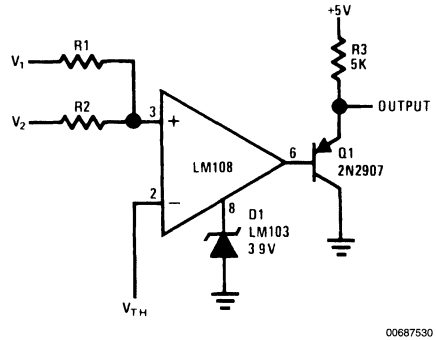


FIGURE 29. Voltage Comparator with Output Buffer

The LM108 can also be used as a differential comparator, going through a transition when two input voltages are equal. However, resistors must be inserted in series with the inputs to limit current and minimize loading on the signal sources when the input-protection diodes conduct. *Figure 29* also shows how a PNP transistor can be added on the output to increase the fan out to about 20 with standard DTL or TTL.

Power Booster

The LM108, which was designed for low power consumption, is not able to drive heavy loads. However, a relatively simple booster can be added to the output to increase the output current to ±50 mA. This circuit, shown in *Figure 30*, has the added advantage that it swings the output up to the supplies, within a fraction of a volt. The increased voltage swing is particularly helpful in low voltage circuits.

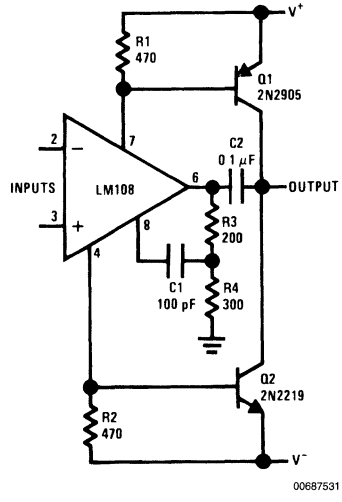


FIGURE 30. Power Booster

In *Figure 30*, the output transistors are driven from the supply leads of the op amp. It is important that R_1 and R_2 be made low enough so Q_1 and Q_2 are not turned on by the *worst case* quiescent current of the amplifier. The output of the op amp is loaded heavily to ground with R_3 and R_4.

When the output swings about 0.5V positive, the increasing positive supply current will turn on Q_1 which pulls up the load. A similar situation occurs with Q_2 for negative output swings.

Power Booster (Continued)

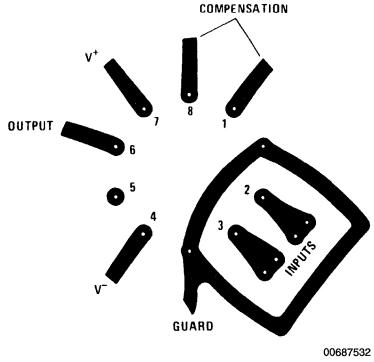
The bootstrapped shunt compensation shown in the figure is the only one that seems to work for all loading conditions. This capacitor, C_1, can be made inversely proportional to the closed loop gain to optimize frequency response. The value given is for a unity-gain follower connection. C_2 is also required for loop stability.

The circuit does have a dead zone in the open loop transfer characteristic. However, the low frequency gain is high enough so that it can be neglected. Around 1 kHz, though, the dead zone becomes quite noticeable.

Current limiting can be incorporated into the circuit by adding resistors in series with the emitters of Q_1 and Q_2 because the short circuit protection of the LM108 limits the maximum voltage drop across R_1 and R_2.

Board Construction

As indicated previously, certain precautions must be observed when building circuits that are sensitive to very low currents. If proper care is not taken, board leakage currents can easily become much larger than the error currents of the op amp. To prevent this, it is necessary to thoroughly clean printed circuit boards. Even experimental breadboards must be cleaned with trichloroethlene or alcohol to remove solder fluxes, and blown dry with compressed air. These fluxes may be insulators at low impedance levels—like in electric motors—but they certainly are not in high impedance circuits. In addition to causing gross errors, their presence can make the circuit behave erratically, especially as the temperature is changed.



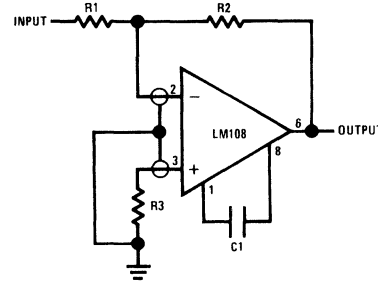
Bottom View

FIGURE 31. Printed Circuit Layout for Input Guarding with TO-5 Package

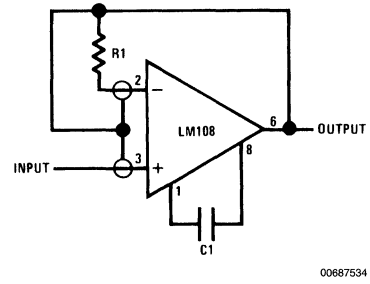
At elevated temperatures, even the leakage of clean boards can be a headache. At 125°C the leakage resistance between adjacent runs on a printed circuit board is about $10^{11}\Omega$ (0.05-inch separation parallel for 1 inch) for high quality epoxy-glass boards that have been properly cleaned. Therefore, the boards can easily produce error currents in the order of 200 pA and much more if they become contaminated. Conservative practice dictates that the boards be coated with epoxy or silicone rubber after cleaning to prevent contamination. Silicone rubber is the easiest to use. However, if the better durability of epoxy is needed, care must be taken to make sure that it gets thoroughly cured. Otherwise, the epoxy will make high temperature leakage much worse.

Care must also be exercised to insure that the circuit board is protected from condensed water vapor when operating in the vicinity of 0°C. This can usually be accomplished by coating the board as mentioned above.

a. Inverting Amplifier



b. Follower



c. Non-Inverting Amplifier

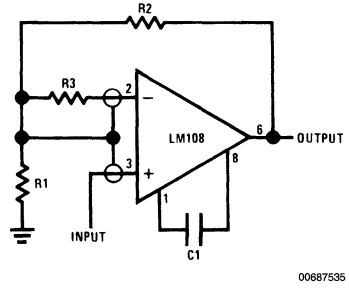


FIGURE 32. Connection of Input Guards

Guarding

Even with properly cleaned and coated boards, leakage currents are on the verge of causing trouble at 125°C. The standard pin configuration of most IC op amps has the input pins adjacent to pins which are at the supply potentials.

Guarding (Continued)

Therefore, it is advisable to employ guarding to reduce the voltage difference between the inputs and adjacent metal runs.

A board layout that includes input guarding is shown in *Figure 31* for the eight lead TO-5 package. A ten-lead pin circle is used, and the leads of the IC are formed so that the holes adjacent to the inputs are vacant when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is then connected to a low impedance point that is at the same potential as the inputs. The leakage currents from the pins at the supply potentials are absorbed by the guard. The voltage difference between the guard and the inputs can be made approximately equal to the offset voltage, reducing the effective leakage by more than three orders of magnitude. If the leads of the integrated circuit, or other components connected to the input, go through the board, it may be necessary to guard both sides.

Figure 32 shows how the guard is commited on the more-common op amp circuits. With an integrator or inverting amplifier, where the inputs are close to ground potential, the guard is simply grounded. With the voltage follower, the guard is bootstrapped to the output. If it is desirable to put a resistor in the inverting input to compensate for the source resistance, it is connected as shown in *Figure 32b*.

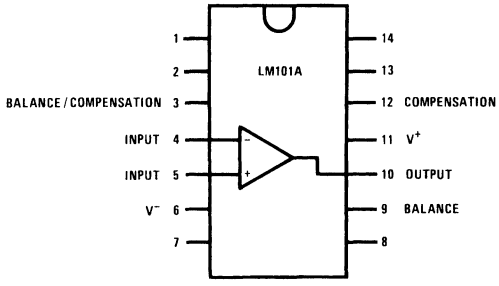
Guarding a non-inverting amplifier is a little more complicated. A low impedance point must be created by using relatively low value feedback resistors to determine the gain (R_1 and R_2 in *Figure 32c*). The guard is then connected to the junction of the feedback resistors. A resistor, R_3, can be connected as shown in the figure to compensate for large source resistances.

With the dual-in-line and flat packages, it is far more difficult to guard the inputs, if the standard pin configuration of the LM709 or LM101A is used, because the pin spacings on these packages are fixed. Therefore, the pin configuration of the LM108 was changed, as shown in *Figure 33*.

Conclusions

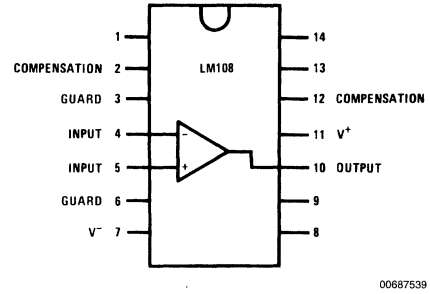
IC op amps are now available that equal the input current specifications of FET amplifiers in all but the most restricted temperature range applications. At operating temperatures above 85°C, the IC is clearly superior as it uses bipolar transistors that make it possible to eliminate the leakage currents that plague FETs. Additionally, bipolar transistors match better than FETs, so low offset voltage and drifts can be obtained without expensive adjustments or selection. Further, the bipolar devices lend themselves more readily to low-cost monolithic construction.

These amplifiers open up new application areas and vastly improve performance in others. For example, in analog memories, holding intervals can be extended to minutes, even where −55°C to 125°C operation is involved. Instrumentation amplifiers and low frequency waveform generators also benefit from the low error currents.



NOTE: Pin 6 connected to bottom of package

Top View



NOTE: Pin 7 connected to bottom of package

Top View

FIGURE 33. Comparing Connection Diagrams of the LM101A and LM108, Showing Addition of Guarding

When operating above 85°C, overall performance is frequently limited by components other than the op amp, unless certain precautions are observed It is generally necessary to redesign circuits using semiconductor switches to reduce the effect of their leakage currents. Further, high quality capacitors must be used, and care must be exercised in selecting large value resistors. Printed circuit board leakages can also be troublesome unless the boards are properly treated. And above 100°C, it is almost mandatory to employ guarding on the boards to protect the inputs, if the full potential of the amplifier is to be realized.

Appendix

A complete schematic of the LM108 is given in *Figure 34*. A description of the basic circuit is presented along with a simplified schematic earlier in the text. The purpose of this Appendix is to explain some of the more subtle features of the design.

The current source supplying the input transistors is Q_{29}. It is designed to supply a total input stage current of 6 µA at 25°C. This current drops to 3 µA at −55°C but increases to only 7.5 µA at 125°C. This temperature characteristic tends to compensate for the current gain falloff of the input transistors at low temperatures without creating stability problems at high temperatures.

The biasing circuitry for the input current source is nearly identical to that in the LM101A, and a complete description is given in Reference 4. However, a brief explanation follows.

Appendix (Continued)

A collector FET,[6] Q_{23}, which has a saturation current of about 30 µA, establishes the collector current of Q_{24}. This FET provides the initial turn-on current for the circuit and insures starting under all conditions. The purpose of R_{14} is to compensate for production and temperature variations in the FET current. It is a collector resistor (indicated by the T through it) made of the same semiconductor material as the FET channel. As the FET current varies, the drop across R_{14} tends to compensate for changes in the emitter base voltage of Q_{24}.

The collector-emitter voltage of Q_{24} is equal to the emitter base voltage of Q_{24} plus that of Q_{25}. This voltage is delivered to Q_{26} and Q_{29}. Q_{25} and Q_{24} are operated at substantially higher currents than Q_{26} and Q_{29}. Hence, there is a differential in their emitter base voltages that is dropped across R_{19} to determine the input stage current. R_{18} is a pinched base resistor, as is indicated by the slash bar through it. This resistor, which has a large positive temperature coefficient, operates in conjunction with R_{17} to help shape the temperature characteristics of the input stage current source.

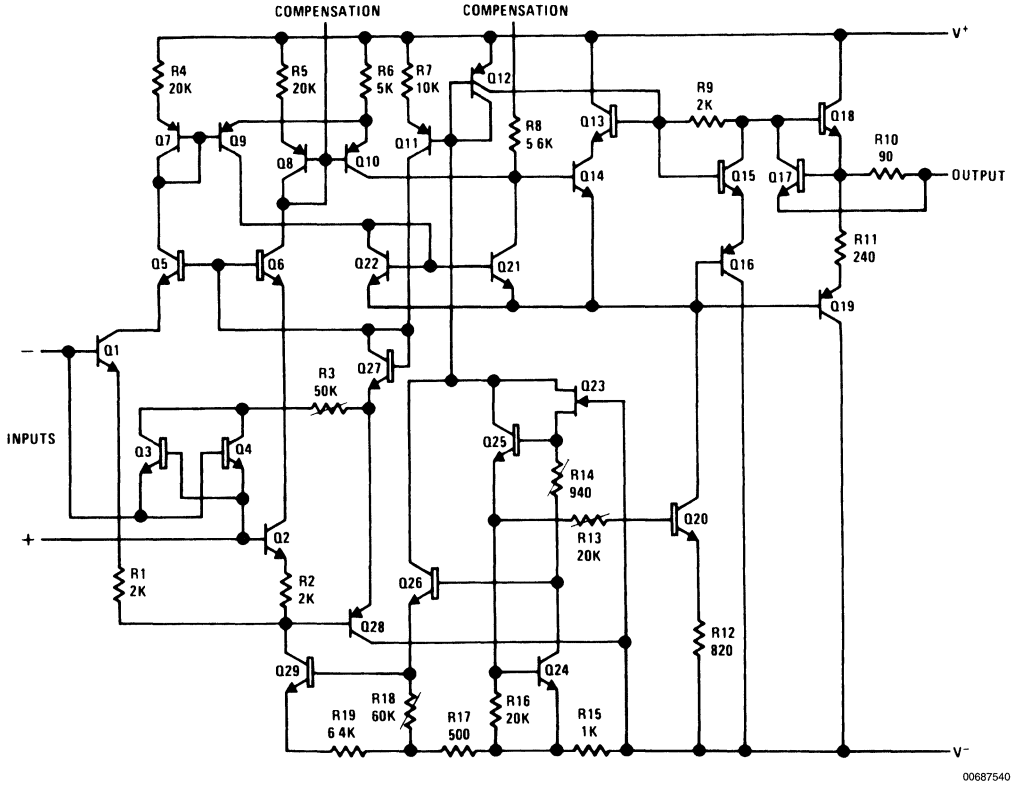


FIGURE 34. Complete Schematic of the LM108

The output currents of Q_{26}, Q_{25}, and Q_{23} are fed to Q_{12}, which is a controlled-gain lateral PNP.[6] It delivers one-half of the combined currents to the output stage. Q_{11} is also connected to Q_{12}, with its output current set at approximately 15 µA by R_7. Since this type of current source makes use of the emitter-base voltage differential between similar transistors operating at different collector currents, the output of Q_{11} is relatively independent of the current delivered to Q_{12}.[12] This current is used for the input stage bootstrapping circuitry.

Q_{20} also supplies current to the class-B output stage. Its output current is determined by the ratio of R_{15} to R_{12} and the current through R_{12}. R_{13} is included so that the biasing circuit is not upset when Q_{20} saturates.

One major departure from the simplified schematic is the bootstrapping of the second stage active loads, Q_{21} and Q_{22}, to the output. This makes the second stage gain dependent only on how well Q_9 and Q_{10} match with variations in output voltage. Hence, the second stage gain is quite high. In fact, the overall gain of the amplifier is typically in excess of 10^6 at dc.

The second stage active loads drive Q_{14}. A high-gain primary transistor is used to prevent loading of the second stage. Its collector is bootstrapped by Q_{13} to operate it at zero collector-base voltage. The class-B output stage is actually driven by the emitter of Q_{14}.

Appendix (Continued)

A dead zone in the output stage is prevented by biasing Q_{18} and Q_{19} on the verge of conduction with Q_{15} and Q_{16}. R_9 is used to compensate for the transconductance of Q_{15} and Q_{16}, making the output stage quiescent current relatively independent of the output current of Q_{12}. The drop across this resistor also reduces quiescent current.

For positive-going outputs, short circuit protection is provided by R_{10} and Q_{17}. When the voltage drop across R_{10} turns on Q_{17}, it removes base drive from Q_{18}. For negative-going outputs, current limiting is initiated when the voltage drop across R_{11} becomes large enough for the collector base junction of Q_{17} to become forward biased. When this happens, the base of Q_{19} is clamped so the output current cannot increase further.

Input protection is provided by Q_3 and Q_4 which act as clamp diodes between the inputs. The collectors of these transistors are bootstrapped to the emitter of Q_{28} through R_3. This keeps the collector-isolation leakage of the transistors from showing up on the inputs. R_3 is included so that the bootstrapping is not disrupted when Q_3 or Q_4 saturate with an input overload. Current-limiting resistors were not connected in series with the inputs, since diffused resistors cannot be employed such that they work effectively, without causing high temperature leakages.

TABLE 1. Typical Performance of the LM108 Operational Amplifier (T_A = 25°C and V_S = ±15V)

Input Offset Voltage	0.7 mV
Input Offset Current	50 pA
Input Bias Current	0.8 nA
Input Resistance	70 MΩ
Input Common Mode Range	±14V
Common Mode Rejection	100 dB
Offset Voltage Drift	3 µV/°C
Offset Current Drift	0.5 pA/°C
Voltage Gain	300V/mV
Small Signal Bandwidth	1.0 MHz
Slew Rate	0.3V/µs
Output Swing	±14V
Supply Current	300 µA
Power Supply Rejection	100 dB
Operating Voltage Range	±2V to ±20V

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Precision IC Comparator Runs from +5V Logic Supply

National Semiconductor
Application Note 41
Robert J. Widlar

Introduction

In digital systems, it is sometimes necessary to convert low level analog signals into digital information. An example of this might be a detector for the illumination level of a photo-diode. Another would be a zero crossing detector for a magnetic transducer such as a magnetometer or a shaft-position pickoff. These transducers have low-level outputs, with currents in the low microamperes or voltages in the low millivolts. Therefore, low level circuitry is required to condition these signals before they can drive logic circuits.

A voltage comparator can perform many of these precision functions. A comparator is essentially a high-gain op amp designed for open loop operation. The function of a comparator is to produce a logic "one" on the output with a positive signal between its two inputs or a logic "zero" with a negative signal between the inputs. Threshold detection is accomplished by putting a reference voltage on one input and the signal on the other. Clearly, an op amp can be used as a comparator, except that its response time is in the tens of microseconds which is often too slow for many applications.

A unique comparator design will be described here along with some of its applications in digital systems. Unlike older IC comparators or op amps, it will operate from the same 5V supply as DTL or TTL logic circuits. It will also operate with the single negative supply used with MOS logic. Hence, low level functions can be performed without the extra supply voltages previously required.

The versatility of the comparator along with the minimal circuit loading and considerable precision recommend it for many uses, in digital systems, other than the detection of low level signals. It can be used as an oscillator or multivibrator, in digital interface circuitry and even for low voltage analog circuitry. Some of these applications will also be discussed.

Circuit Description

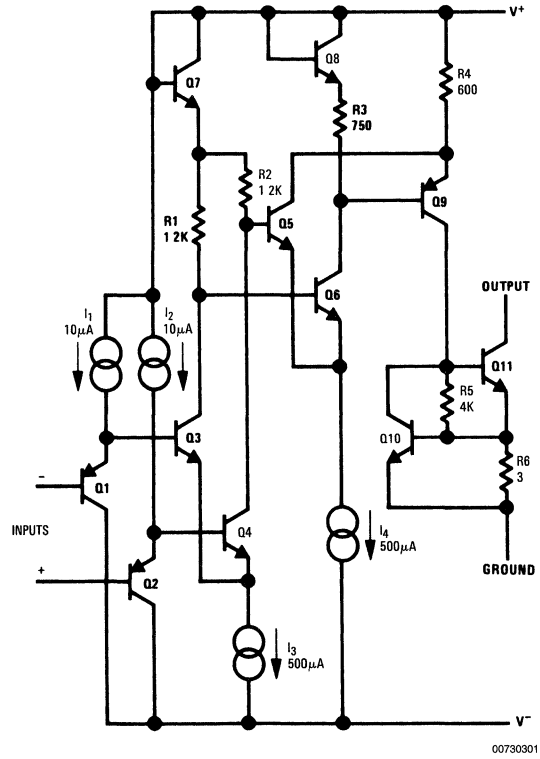


FIGURE 1. Simplified Schematic of the Comparator

In order to understand how to use this comparator, it is necessary to look briefly at the circuit configuration. *Figure 1* shows a simplified schematic of the device. PNP transistors buffer the differential input stage to get low input currents

Circuit Description (Continued)

without sacrificing speed. The PNP's drive a standard NPN differential stage, Q_3 and Q_4. The output of this stage is further amplified by the Q_5—Q_6 pair. This feeds Q_9 which provides additonal gain and drives the output stage. Current sources are used to determine the bias currents, so that performance is not greatly affected by supply voltages

The output transistor is Q_{11}, and it is protected by Q_{10} and R_6 which limit the peak output current. The output lead, since it is not connected to any other point in the circuit, can either be returned to the positive supply through a pull-up resistor or switch loads that are connected to a voltage higher than the positive supply voltage. The circuit will operate from a single supply if the negative supply lead is connected to ground. However, if a negative supply is available, it can be used to increase the input common mode range.

Table 1 summarizes the performance of the comparator when operating from a 5V supply. The circuit will work with supply voltages up to ±15V with a corresponding increase in the input voltage range. Other characteristics are essentially unchanged at the higher voltages.

TABLE 1. Important electrical characteristics of the LM111 comparator when operating from single, 5V supply (T_A = 25°C)

Parameter	Limits			Units
	Min	Typ	Max	
Input Offset Voltage		0.7	3	mV
Input Offset Current		4	10	nA
Input Bias Current		60	100	nA
Voltage Gain		100		V/mV
Response Time		200		ns
Common Mode Range	0.3		3 8	V
Output Voltage Swing			50	V
Output Current			50	mA
Fan Out (DTL/TTL)	8			
Supply Current		3	5	mA

Low Level Applications

A circuit that will detect zero crossing in the output of a magnetic transducer within a fraction of a millivolt is shown in *Figure 2*. The magnetic pickup is connected between the two inputs of the comparator. The resistive divider, R_1 and R_2, biases the inputs 0.5V above ground, within the common mode range of the IC. The output will directly drive DTL or TTL. The exact value of the pull up resistor, R_5, is determined by the speed required from the circuit since it must drive any capacitive loading for positive-going output signals. An optional offset-balancing circuit using R_3 and R_4 is included in the schematic.

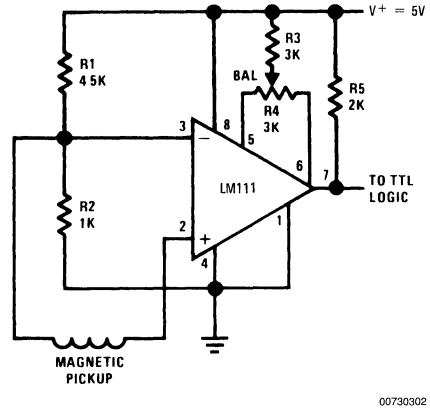


FIGURE 2. Zero Crossing Detector for Magnetic Transducer

Figure 3 shows a connection for operating with MOS logic. This is a level detector for a photodiode that operates off a −10V supply. The output changes state when the diode current reaches 1 µA. Even at this low current, the error contributed by the comparator is less than 1%.

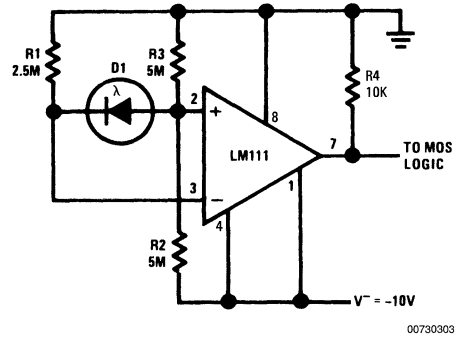


FIGURE 3. Level Detector for Photodiode

Higher threshold currents can be obtained by reducing R_1, R_2 and R_3 proportionally. At the switching point, the voltage across the photodiode is nearly zero, so its leakage current does not cause an error. The output switches between ground and −10V, driving the data inputs of MOS logic directly.

The circuit in *Figure 3* can, of course, be adapted to work with a 5V supply. At any rate, the accuracy of the circuit will

Low Level Applications (Continued)

depend on the supply-voltage regulation, since the reference is derived from the supply. *Figure 4* shows a method of making performance independent of supply voltage. D_1 is a temperature-compensated reference diode with a 1.23V breakdown voltage. It acts as a shunt regulator and delivers a stable voltage to the comparator. When the diode current is large enough (about 10 µA) to make the voltage drop across R_3 equal to the breakdown voltage of D_1, the output will change state. R_2 has been added to make the threshold error proportional to the offset current of the comparator, rather than the bias current. It can be eliminated if the bias current error is not considered significant.

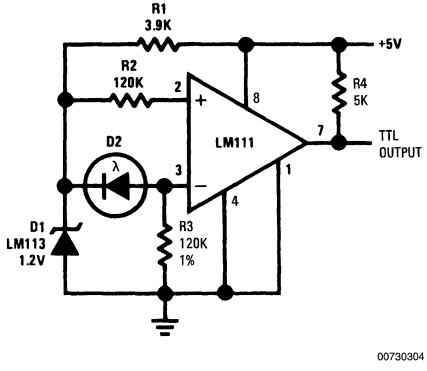


FIGURE 4. Precision Level Detector for Photodiode

A zero crossing detector that drives the data input of MOS logic is shown in *Figure 5*. Here, both a positive supply and the −10V supply for MOS circuits are used. Both supplies are required for the circuit to work with zero common-mode voltage. An alternate balancing scheme is also shown in the schematic. It differs from the circuit in *Figure 2* in that it raises the input-stage current by a factor of three. This increases the rate at which the input voltage follows rapidly-changing signals from 7V/µs to 18V/µs. This increased common-mode slew can be obtained without the balancing potentiometer by shorting both balance terminals to the positive-supply terminal. Increased input bias current is the price that must be paid for the faster operation.

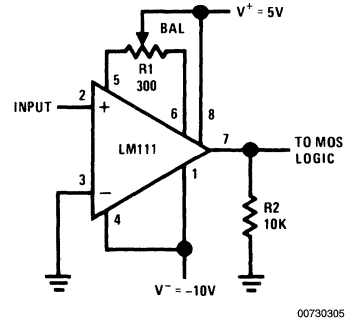


FIGURE 5. Zero Crossing Detector Driving MOS Logic

Digital Interface Circuits

Figure 6 shows an interface between high-level logic and DTL or TTL. The input signal, with 0V and 30V logic states is attenuated to 0V and 5V by R_1 and R_2. R_3 and R_4 set up a 2.5V threshold level for the comparator so that it switches when the input goes through 15V. The response time of the circuit can be controlled with C_1, if desired, to make it insensitive to fast noise spikes. Because of the low error currents of the LM111, it is possible to get input impedances even higher than the 300 kΩ obtained with the indicated resistor values.

The comparator can be strobed, as shown in *Figure 6*, by the addition of Q_1 and R_5. With a logic one on the base of Q_1, approximately 2.5 mA is drawn out of the strobe terminal of the LM111, making the output high independent of the input signal.

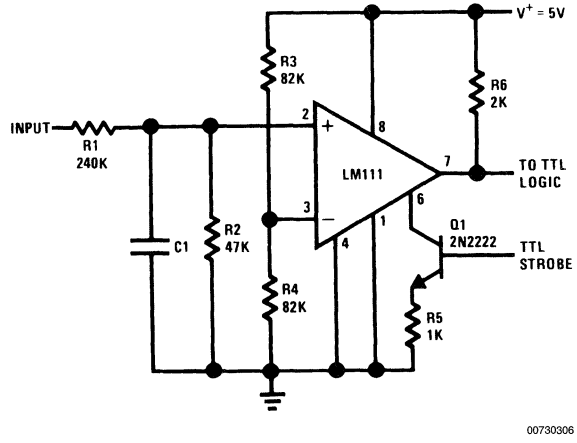


FIGURE 6. Circuit for Transmitting Data Between High-Level Logic and TTL

Digital Interface Circuits (Continued)

Sometimes it is necessary to transmit data between digital equipments, yet maintain a high degree of electrical isolation. Normally, this is done with a transformer. However, transformers have problems with low-duty-cycle pulses since they do not preseve the dc level.

The circuit in *Figure 7* is a more satisfactory method of obtaining isolation. At the transmitting end, a TTL gate drives a gallium-arsenide light-emitting diode. The light output is optically coupled to a silicon photodiode, and the comparator detects the photodiode output. The optical coupling makes possible electrical isolation in the thousands of Megohms at potentials in the thousands of volts.

The maximum data rate of this circuit is 1 MHz. At lower rates (~200 kHz) R_3 and C_1 can be eliminated.

Multivibrators and Oscillators

The free-running multivibrator in *Figure 8* is another example of the versatility of the comparator. The inputs are biased within the common mode range by R_1 and R_2 DC stability, which insures starting, is provided by negative feedback through R_3. The negative feedback is reduced at high frequencies by C_1. At some frequency, the positive feedback through R_4 will be greater than the negative feedback; and the circuit will oscillate. For the component values shown, the circuit delivers a 100 kHz square wave output. The frequency can be changed by varying C_1 or by adjusting R_1 through R_4, while keeping their ratios constant.

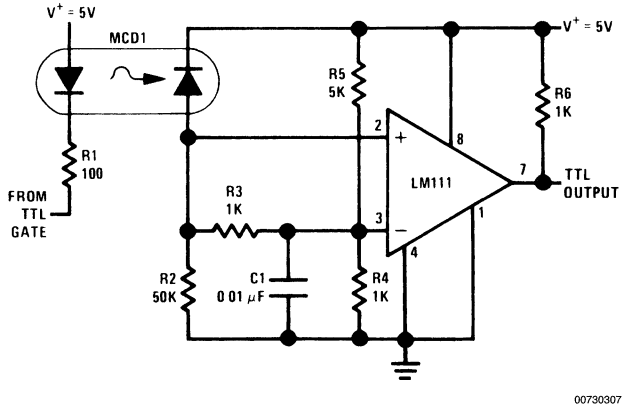
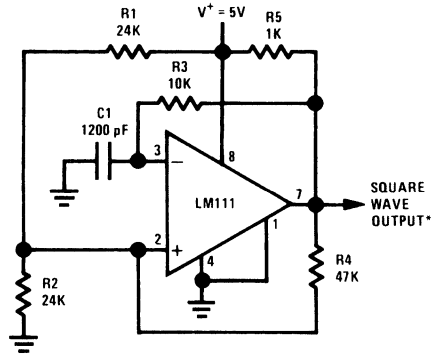


FIGURE 7. Data Transmission System with Near-Infinite Ground Isolation

Because of the low input current of the comparator, large circuit impedances can be used. Therefore, low frequencies can be obtained with relatively-small capacitor values: it is no problem to get down to 1 Hz using a 1 μF capacitor. The speed of the comparator also permits operation at frequencies above 100 kHz.



* TTL or DTL Fanout of two

FIGURE 8. Free-Running Multivibrator

Multivibrators and Oscillators

(Continued)

The frequency of oscillation depends almost entirely on the resistance and capacitor values because of the precision of the comparator. Further, the frequency changes by only 1% for a 10% change in supply voltage. Waveform symmetry is also good, but the symmetry can be varied by changing the ratio of R_1 to R_2.

A crystal-controlled oscillator that can be used to generate the clock in slower digital systems is shown in *Figure 9*. It is similar to the free running multivibrator, except that the positive feedback is obtained through a quartz crystal. The circuit oscillates when transmission through the crystal is at a maximum, so the crystal operates in its series-resonant mode. The high input impedance of the comparator and the isolating capacitor, C_2, minimize loading of the crystal and contribute to frequency stability. As shown, the oscillator delivers a 100 kHz square-wave output.

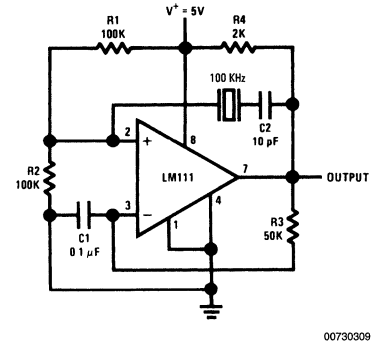
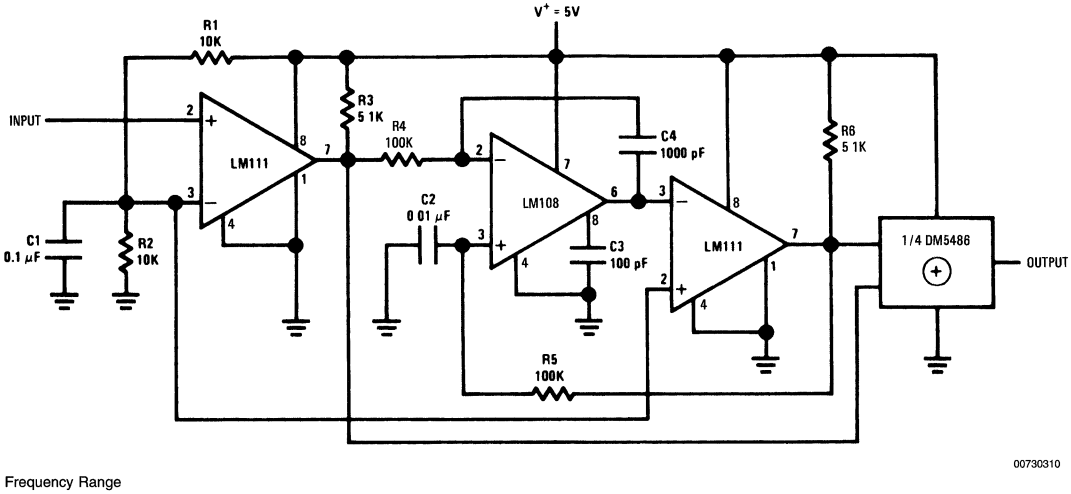


FIGURE 9. Crystal-controlled Oscillator

Frequency Doubler

In a digital system, it is a relatively simple matter to divide by any integer. However, multiplying by an integer is quite another story especially if operation over a wide frequency range and waveform symmetry are required.



Frequency Range
Input—5 kHz to 50 kHz
Output—10 kHz to 100 kHz

FIGURE 10. Frequency Doubler

A frequency doubler that satisfies the above requirements is shown in *Figure 10*. A comparator is used to shape the input signal and feed it to an integrator. The shaping is required because the input to the integrator must swing between the supply voltage and ground to preserve symmetry in the output waveform. An LM108 op amp, that works from the 5V logic supply, serves as the integrator. This feeds a triangular waveform to a second comparator that detects when the waveform goes through a voltage equal to its average value. Hence, as shown in *Figure 11*, the output of the second comparator is delayed by half the duration of the input pulse. The two comparator outputs can then be combined through an exclusive-OR gate to produce the double-frequency output.

Frequency Doubler (Continued)

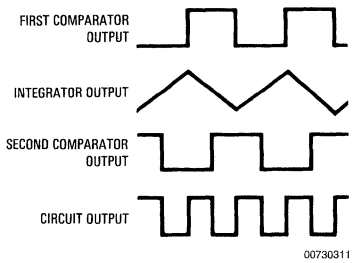


FIGURE 11. Waveforms for the Frequency Doubler

With the component values shown, the circuit operates at frequencies from 5 kHz to 50 kHz. Lower frequency operation can be secured by increasing both C_2 and C_4.

Application Hints

One of the problems encountered in using earlier IC comparators like the LM710 or LM106 was that they were prone to erratic operation caused by oscillations. This was a direct result of the high speed of the devices, which made it mandatory to provide good input-output isolation and low-inductance bypassing on the supplies. These oscillations could be particularly puzzling when they occurred internally, showing up at the external terminals only as erratic dc characteristics.

In general, the LM111 is less susceptible to spurious oscillations both because of its lower speed (200 ns response time vs 40 ns) and because of its better power supply rejection. Feedback between the output and the input is a lesser problem with a given source resistance. However, the LM111 can operate with source resistance that are orders of magnitude higher than the earlier devices, so stray coupling between the input and output should be minimized. With source resistances between 1 kΩ and 10 kΩ, the impedance (both capacitive and resistive) on both inputs should be made equal, as this tends to reject the signal feedback. Even so, it is difficult to completely eliminate oscillations in the linear region with source resistances above 10 kΩ, because the 1 MHz open loop gain of the comparator is about 80 dB. However, this does not affect the dc characteristics and is not a problem unless the input signal dwells within 200 μV of the transition level. But if the oscillation does cause difficulties, it can be eliminated with a small amount of positive feedback around the comparator to give a 1 mV hysteresis.

Stray coupling between the output and the balance terminals can also cause oscillations, so an attempt should be made to keep these leads apart. It is usually advisable to tie the balance pins together to minimize the effect of this feedback. If balancing is used, the same result can be accomplished by connecting a 0.1 μF capacitor between these pins.

Normally, individual supply bypasses on every device are unnecessary, although long leads between the comparator and the bypass capacitors are definitely not recommended. If large current spikes are injected into the supplies in switching the output, bypass capacitors should be included at these points.

When driving the inputs from a low impedance source, a limiting resistor should be placed in series with the input lead to limit the peak current to something less than 100 mA. This is especially important when the inputs go outside a piece of equipment where they could accidentally be connected to high voltage sources. Low impedance sources do not cause a problem unless their output voltage exceeds the negative supply voltage. However, the supplies go to zero when they are turned off, so the isolation is usually needed.

Large capacitors on the input (greater than 0.1 μF) should be treated as a low source impedance and isolated with a resistor. A charged capacitor can hold the inputs outside the supply voltage if the supplies are abruptly shut off.

Precautions should be taken to insure that the power supplies for this or any other IC never become reversed—even under transient conditions With reverse voltages greater than 1V, the IC can conduct excessive current, fusing internal aluminum interconnects. This usually takes more than 0.5A. If there is a possibility of reversal, clamp diodes with an adequate peak current rating should be installed across the supply bus.

No attempt should be made to operate the circuit with the ground terminal at a voltage exceeding either supply voltage. Further, the 50V output-voltage rating applies to the potential between the output and the V^- terminal. Therefore, if the comparator is operated from a negative supply, the maximum output voltage must be reduced by an amount equal to the voltage on the V^- terminal.

The output circuitry is protected for shorts across the load. It will not, for example, withstand a short to a voltage more negative than the ground terminal. Additionally, with a sustained short, power dissipation can become excessive if the voltage across the output transistor exceeds about 10V.

The input terminals can exceed the positive supply voltage without causing damage. However, the 30V maximum rating between the inputs and the V^- terminal must be observed. As mentioned earlier, the inputs should not be driven more negative than the V^- terminal.

Conclusions

A versatile voltage comparator that can perform many of the precision functions required in digital systems has been produced. Unlike older comparators, the IC can operate from the same supply voltage as the digital circuits. The comparator is particularly useful in circuits requiring considerable sensitivity and accuracy, such as threshold detectors for low level sensors, data transmission circuits or stable oscillators and multivibrators.

The comparator can also be used in many analog systems. It operates from standard ±15V op amp supplies, and its dc accuracy equals some of the best op amps. It is also an order of magnitude faster than op amps used as comparators.

The new comparator is considerably more flexible than older devices. Not only will it drive RTL, DTL and TTL logic; but also it can interface with MOS logic or deliver ±15V to FET analog switches. The output can switch 50V, 50 mA loads, making it useful as a driver for relays, lamps or light-emitting diodes. Further, a unique output stage enables it to drive loads referred to either supply or to ground and provide ground isolation between the comparator inputs and the load.

The LM111 is a plug-in replacement for comparators like the LM710 and LM106 in applications where speed is not of prime concern. Compared to its predecessors in other respects, it has many improved electrical specifications, more design flexibility and fewer application problems.

LM139/LM239/LM339 A Quad of Independently Functioning Comparators

National Semiconductor
Application Note 74
Robert J. Widlar

Introduction

The LM139/LM239/LM339 family of devices is a monolithic quad of independently functioning comparators designed to meet the needs for a medium speed, TTL compatible comparator for industrial applications. Since no antisaturation clamps are used on the output such as a Baker clamp or other active circuitry, the output leakage current in the OFF state is typically 0.5 nA. This makes the device ideal for system applications where it is desired to switch a node to ground while leaving it totally unaffected in the OFF state.

Other features include single supply, low voltage operation with an input common mode range from ground up to approximately one volt below V_{CC}. The output is an uncommitted collector so it may be used with a pull-up resistor and a separate output supply to give switching levels from any voltage up to 36V down to a $V_{CE\ SAT}$ above ground (approx. 100 mV), sinking currents up to 15 mA. In addition it may be used as a single pole switch to ground, leaving the switched node unaffected while in the OFF state. Power dissipation with all four comparators in the OFF state is typically 4 mW from a single 5V supply (1 mW/comparator).

Circuit Description

Figure 1 shows the basic input stage of one of the four comparators of the LM139. Transistors Q_1 through Q_4 make up a PNP Darlington differential input stage with Q_5 and Q_6 serving to give single-ended output from differential input with no loss in gain. Any differential input at Q_1 and Q_4 will be amplified causing Q_6 to switch OFF or ON depending on input signal polarity. It can easily be seen that operation with an input common mode voltage of ground is possible. With both inputs at ground potential, the emitters of Q_1 and Q_4 will be at one V_{BE} above ground and the emitters of Q_2 and Q_3 at 2 V_{BE}. For switching action the base of Q_5 and Q_6 need only go to one V_{BE} above ground and since Q_2 and Q_3 can operate with zero volts collector to base, enough voltage is present at a zero volt common mode input to insure comparator action. The bases should not be taken more than several hundred millivolts below ground; however, to prevent forward biasing a substrate diode which would stop all comparator action and possibly damage the device, if very large input currents were provided.

Figure 2 shows the comparator with the output stage added. Additional voltage gain is taken through Q_7 and Q_8 with the collector of Q_8 left open to offer a wide variety of possible applications. The addition of a large pull-up resistor from the collector of Q_8 to either $+V_{CC}$ or any other supply up to 36V both increases the LM139 gain and makes possible output switching levels to match practically any application. Several outputs may be tied together to provide an ORing function or the pull-up resistor may be omitted entirely with the comparator then serving as a SPST switch to ground.

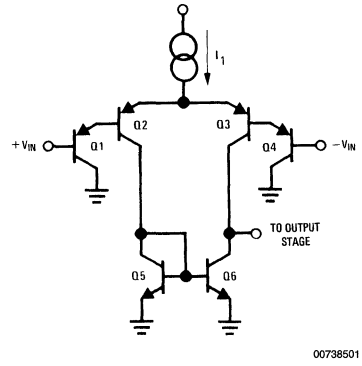


FIGURE 1. Basic LM139 Input Stage

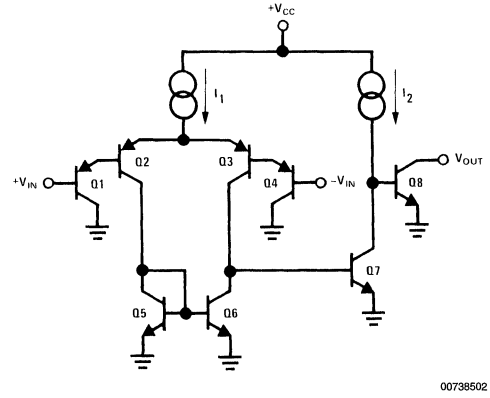


FIGURE 2. Basic LM139 Comparator

Output transistor Q_8 will sink up to 15 mA before the output ON voltage rises above several hundred millivolts. The output current sink capability may be boosted by the addition of a discrete transistor at the output.

The complete circuit for one comparator of the LM139 is shown in *Figure 3*. Current sources I_3 and I_4 are added to help charge any parasitic capacitance at the emitters of Q_1 and Q_4 to improve the slew rate of the input stage. Diodes D_1 and D_2 are added to speed up the voltage swing at the emitters of Q_1 and Q_2 for large input voltage swings.

Circuit Description (Continued)

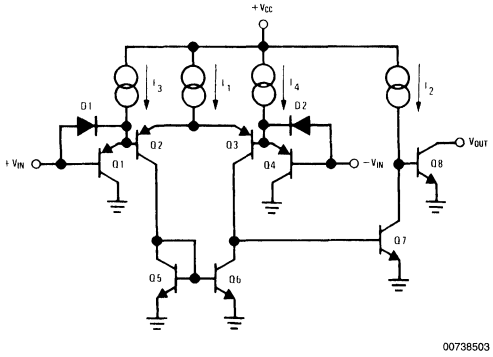


FIGURE 3. Complete LM139 Comparator Circuit

Biasing for current sources I_1 through I_4 is shown in *Figure 4.* When power is first applied to the circuit, current flows through the JFET Q_{13} to bias up diode D_5. This biases transistor Q_{12} which turns ON transistors Q_9 and Q_{10} by allowing a path to ground for their base and collector currents.

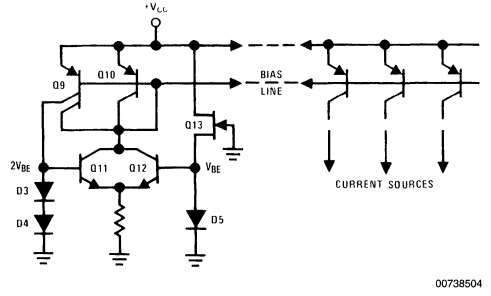


FIGURE 4. Current Source Biasing Circuit

Current from the left hand collector of Q_9 flows through diodes D_3 and D_4 bringing up the base of Q_{11} to 2 V_{BE} above ground and the emitters of Q_{11} and Q_{12} to one V_{BE}. Q_{12} will then turn OFF because its base emitter voltage goes to zero. This is the desired action because Q_9 and Q_{10} are biased ON through Q_{11}, D_3 and D_4 so Q_{12} is no longer needed. The "bias line" is now sitting at a V_{BE} below $+V_{CC}$ which is the voltage needed to bias the remaining current sources in the LM139 which will have a constant bias regardless of $+V_{CC}$ fluctuations. The upper input common mode voltage is V_{CC} minus the saturation voltage of the current sources (approximately 100 mV) minus the 2 V_{BE} of the input devices Q_1 and Q_2 (or Q_3 and Q_4).

Comparator Circuits

Figure 5 shows a basic comparator circuit for converting low level analog signals to a high level digital output The output pull-up resistor should be chosen high enough so as to avoid excessive power dissipation yet low enough to supply enough drive to switch whatever load circuitry is used on the comparator output. Resistors R_1 and R_2 are used to set the input threshold trip voltage (V_{REF}) at any value desired within the input common mode range of the comparator.

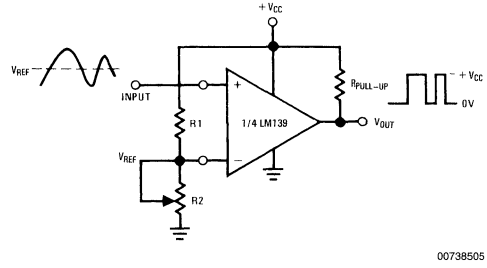


FIGURE 5. Basic Comparator Circuit

Comparators with Hysteresis

The circuit shown in *Figure 5* suffers from one basic drawback in that if the input signal is a slowly varying low level signal, the comparator may be forced to stay within its linear region between the output high and low states for an undesireable length of time. If this happens, it runs the risk of oscillating since it is basically an uncompensated, high gain op amp. To prevent this, a small amount of positive feedback or hysteresis is added around the comparator. *Figure 6* shows a comparator with a small amount of positive feedback. In order to insure proper comparator action, the components should be chosen as follows:

$$R_{PULL\text{-}UP} < R_{LOAD} \text{ and}$$

$$R_1 > R_{PULL\text{-}UP}$$

This will insure that the comparator will always switch fully up to $+V_{CC}$ and not be pulled down by the load or feedback. The amount of feedback is chosen arbitrarily to insure proper switching with the particular type of input signal used. If the output swing is 5V, for example, and it is desired to feedback 1% or 50 mV, then $R_1 \approx 100\ R_2$. To describe circuit operation, assume that the inverting input goes above the reference input ($V_{IN} > V_{REF}$). This will drive the output, V_O, towards ground which in turn pulls V_{REF} down through R_1. Since

Comparators with Hysteresis

(Continued)

V_{REF} is actually the noninverting input to the comparator, it too will drive the output towards ground insuring the fastest possible switching time regardless of how slow the input moves. If the input then travels down to V_{REF}, the same procedure will occur only in the opposite direction insuring that the output will be driven hard towards $+V_{CC}$.

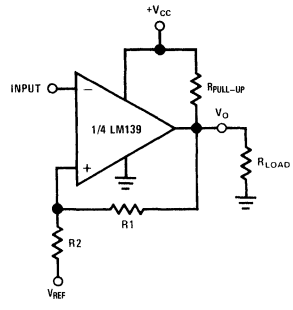


FIGURE 6. Comparator with Positive Feedback to Improve Switching Time

Putting hysteresis in the feedback loop of the comparator has far more use, however, than simply as an oscillation suppressor. It can be made to function as a Schmitt trigger with presettable trigger points. A typical circuit is shown in *Figure 7.* Again, the hysteresis is achieved by shifting the reference voltage at the positive input when the output voltage V_O changes state. This network requires only three resistors and is referenced to the positive supply $+V_{CC}$ of the comparator. This can be modeled as a resistive divider, R_1 and R_2, between $+V_{CC}$ and ground with the third resistor, R_3, alternately connected to $+V_{CC}$ or ground, paralleling either R_1 or R_2. To analyze this circuit, assume that the input voltage, V_{IN}, at the inverting input is less than V_A. With $V_{IN} \leq V_A$ the output will be high ($V_O = +V_{CC}$). The upper input trip voltage, V_{A1}, is defined by:

$$V_{A1} = \frac{+V_{CC}\, R_2}{(R_1 \parallel R_3) + R_2}$$

or

$$V_{A1} = \frac{+V_{CC}\, R_2\, (R_1 + R_3)}{R_1\, R_2 + R_1\, R_3 + R_2\, R_3} \quad (1)$$

When the input voltage V_{IN}, rises above the reference voltage ($V_{IN} > V_{A1}$), voltage, V_O, will go low (V_O = GND). The lower input trip voltage, V_{A2}, is now defined by:

$$V_{A2} = \frac{+V_{CC}\, R_2 \parallel R_3}{R_1 + R_2 \parallel R_3}$$

or

$$V_{A2} = \frac{+V_{CC}\, R_2\, R_3}{R_1\, R_2 + R_1\, R_3 + R_2\, R_3} \quad (2)$$

When the input voltage, V_{IN}, decreases to V_{A2} or lower, the output will again switch high. The total hysteresis, ΔV_A, provided by this network is defined by:

$$\Delta V_A = V_{A1} - V_{A2}$$

or, subtracting equation 2 from equation 1

$$\Delta V_A\, \Delta \frac{+V_{CC}\, R_1\, R_2}{R_1\, R_2 + R_1\, R_3 + R_2\, R_3} \quad (3)$$

To insure that V_O will swing between $+V_{CC}$ and ground, choose:

$$R_{PULL\text{-}UP} < R_{LOAD} \text{ and} \quad (4)$$

$$R_3 > R_{PULL\text{-}UP} \quad (5)$$

Heavier loading on $R_{PULL\text{-}UP}$ (i.e. smaller values of R_3 or R_{LOAD}) simply reduces the value of the maximum output voltage thereby reducing the amount of hysteresis by lowering the value of V_{A1}. For simplicity, we have assumed in the above equations that V_O high switches all the way up to $+V_{CC}$.

To find the resistor values needed for a given set of trip points, we first divide equation (3) by equation (2). This gives us the ratio:

$$\frac{\Delta V_A}{V_{A2}} = \frac{1 + \frac{R_1}{R_3} + \frac{R_1}{R_2}}{1 + \frac{R_3}{R_2} + \frac{R_3}{R_1}} \quad (6)$$

Comparators with Hysteresis (Continued)

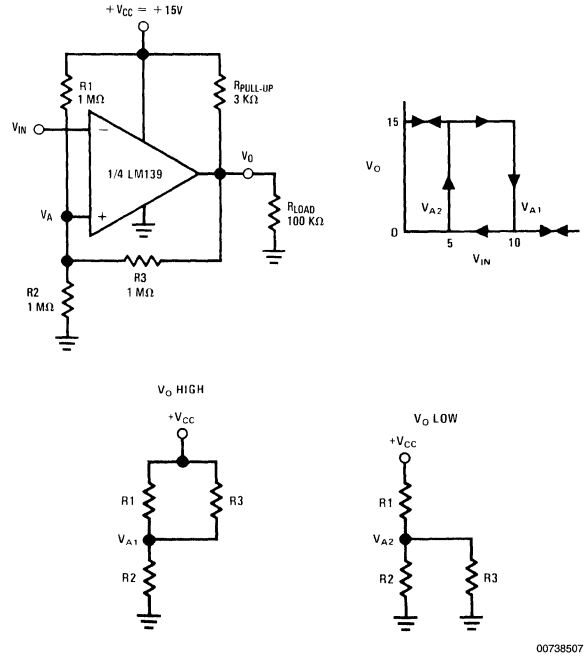


FIGURE 7. Inverting Comparator with Hysteresis

If we let $R_1 = n\ R_3$, *Equation (6)* becomes:

$$\frac{\Delta V_A}{V_{A2}} = n \tag{7}$$

We can then obtain an expression for R_2 from equation (1) which gives

$$R_2 = \frac{R_1 \parallel R_3}{\frac{+V_{CC}}{V_{A1}} - 1} \tag{8}$$

The following design example is offered:

Given: $V^+ = +15V$

$R_{LOAD} = 100\ k\Omega$

$V_{A1} = +10V$

$V_{A2} = +5V$

To find: R_1, R_2, R_3, $R_{PULL\text{-}UP}$

Solution:

From equation (4) $R_{PULL\text{-}UP} < R_{LOAD}$

$R_{PULL\text{-}UP} < 100\ k\Omega$

so let $R_{PULL\text{-}UP} = 3\ k\Omega$

From equation (5) $R_3 > R_{LOAD}$

$R_3 > 100\ k\Omega$

so let $R_3 = 1\ M\Omega$

From equation (7) $n = \frac{\Delta V_A}{V_{A2}} = \frac{10 - 5}{5} = 1$

and since $R_1 = n\ R_3$

this gives $R_1 = 1\ R_3 = 1\ M\Omega$

From equation (8) $R_2 = \frac{500\ k\Omega}{\frac{15}{10} - 1} = 1\ M\Omega$

These are the values shown in *Figure 7*.

The circuit shown in *Figure 8* is a non-inverting comparator with hysteresis which is obtained with only two resistors, R_1 and R_2. In contrast to the first method, however, this circuit requires a separate reference voltage at the negative input. The trip voltage, V_A, at the positive input is shifted about V_{REF} as V_O changes between $+V_{CC}$ and ground.

Comparators with Hysteresis

(Continued)

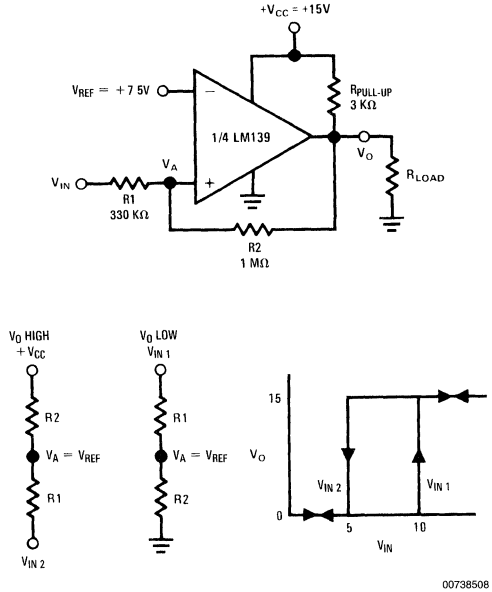


FIGURE 8. Non-Inverting Comparator with Hysteresis

Again for analysis, assume that the input voltage, V_{IN}, is low so that the output, V_O, is also low (V_O = GND). For the output to switch, V_{IN} must rise up to $V_{IN\ 1}$ where $V_{IN\ 1}$ is given by:

$$V_{IN\ 1} = \frac{V_{REF}\,(R_1 + R_2)}{R_2} \tag{9}$$

As soon as V_O switches to $+V_{CC}$, V_A will step to a value greater than V_{REF} which is given by:

$$V_A = V_{IN} + \frac{(V_{CC} - V_{IN\ 1})\,R_1}{R_1 + R_2} \tag{10}$$

To make the comparator switch back to its low state (V_O = GND) V_{IN} must go below V_{REF} before V_A will again equal V_{REF}. This lower trip point is now given by:

$$V_{IN\ 2} = \frac{V_{REF}\,(R_1 + R_2) - V_{CC}\,R_1}{R_2} \tag{11}$$

The hysteresis for this circuit, ΔV_{IN}, is the difference between $V_{IN\ 1}$ and $V_{IN\ 2}$ and is given by:

$$\Delta V_{IN} = V_{IN\ 1} - V_{IN\ 2} = \frac{V_{REF}\,(R_1 + R_2)}{R_2} - \frac{V_{REF}\,(R_1 + R_2) - V_{CC}\,R_1}{R_2}$$

or

$$\Delta V_{IN} = \frac{V_{CC}\,R_1}{R_2} \tag{12}$$

As a design example consider the following:

Given: R_{LOAD} = 100 kΩ

$V_{IN\ 1}$ = 10V

$V_{IN\ 2}$ = 5V

$+V_{CC}$ = 15V

To find: V_{REF}, R_1, R_2 and R_3

Solution:

Again choose $R_{PULL\text{-}UP} < R_{LOAD}$ to minimize loading, so let

$R_{PULL\text{-}UP}$ = 3 kΩ

From equation (12)

$$\frac{R_1}{R_2} = \frac{\Delta V_{IN}}{V_{CC}}$$

$$\frac{R_1}{R_2} = \frac{10 - 5}{15} = \frac{1}{3}$$

$$R_1 = \frac{R_2}{3}$$

From equation (9)

$$V_{REF} = \frac{10}{1 + \frac{R_1}{R_2}}$$

$$V_{REF} = \frac{V_{IN}}{1 + \frac{1}{3}} = 7.5V$$

To minimize output loading choose

$R_2 > R_{PULL\text{-}UP}$

or $R_2 > 3$ kΩ

so let $R_2 = 1$ MΩ

The value of R_1 is now obtained from equation (12)

$$R_1 = \frac{R_2}{3}$$

$$R_1 = \frac{1\ \text{M}\Omega}{3} \cong 330\ \text{k}\Omega$$

These are the values shown in *Figure 8.*

Limit Comparator with Lamp Driver

The limit comparator shown in *Figure 9* provides a range of input voltages between which the output devices of both LM139 comparators will be OFF.

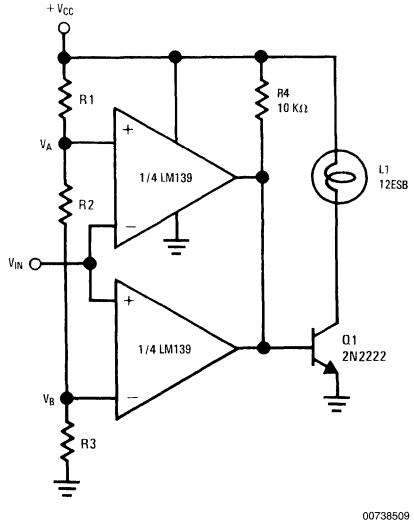


FIGURE 9. Limit Comparator with Lamp Driver

This will allow base current for Q_1 to flow through pull-up resistor R_4, turning ON Q_1 which lights the lamp. If the input voltage, V_{IN}, changes to a value greater than V_A or less than V_B, one of the comparators will switch ON, shorting the base of Q_1 to ground, causing the lamp to go OFF. If a PNP transistor is substituted for Q_1 (with emitter tied to $+V_{CC}$) the lamp will light when the input is above V_A or below V_B. V_A and V_B are arbitrarily set by varying resistors R_1, R_2 and R_3.

Zero Crossing Detector

The LM139 can be used to symmetrically square up a sine wave centered around zero volts by incorporating a small amount of positive feedback to improve switching times and centering the input threshold at ground (see *Figure 10*). Voltage divider R_4 and R_5 establishes a reference voltage, V_1, at the positive input. By making the series resistance, R_1 plus R_2 equal to R_5, the switching condition, $V_1 = V_2$, will be satisfied when $V_{IN} = 0$. The positive feedback resistor, R_6, is made very large with respect to R_5 ($R_6 = 2000\ R_5$). The resultant hysteresis established by this network is very small ($\Delta V_1 < 10$ mV) but it is sufficient to insure rapid output voltage transitions. Diode D_1 is used to insure that the inverting input terminal of the comparator never goes below approximately −100 mV. As the input terminal goes negative, D_1 will forward bias, clamping the node between R_1 and R_2 to approximately −700 mV. This sets up a voltage divider with R_2 and R_3 preventing V_2 from going below ground. The maximum negative input overdrive is limited by the current handling ability of D_1.

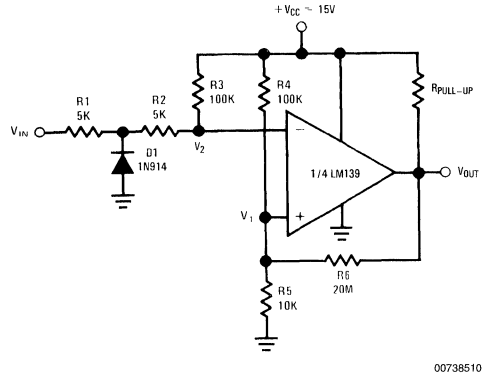


FIGURE 10. Zero Crossing Detector

Comparing the Magnitude of Voltages of Opposite Polarity

The comparator circuit shown in *Figure 11* compares the magnitude of two voltages, $V_{IN\ 1}$ and $V_{IN\ 2}$ which have opposite polarities. The resultant input voltage at the minus input terminal to the comparator, V_A, is a function of the voltage divider from $V_{IN\ 1}$ and $V_{IN\ 2}$ and the values of R_1 and R_2. Diode connected transistor Q_1 provides protection for the minus input terminal by clamping it at several hundred millivolts below ground. A 2N2222 was chosen over a 1N914 diode because of its lower diode voltage. If desired, a small amount of hysteresis may be added using the techniques described previously. Correct magnitude comparison can be seen as follows: Let $V_{IN\ 1}$ be the input for the positive polarity input voltage and $V_{IN\ 2}$ the input for the negative polarity. If the magnitude of $V_{IN\ 1}$ is greater than that of $V_{IN\ 2}$ the output will go low (V_{OUT} = GND). If the magnitude of $V_{IN\ 1}$ is less than that of $V_{IN\ 2}$, however, the output will go high ($V_{OUT} = V_{CC}$).

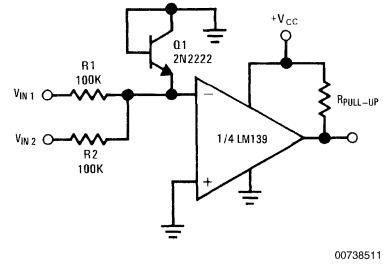


FIGURE 11. Comparing the Magnitude of Voltages of Opposite Polarity

Magnetic Transducer Amplifier

A circuit that will detect the zero crossings in the output of a magnetic transducer is shown in *Figure 12*. Resistor divider, R_1 and R_2, biases the positive input at $+V_{CC}/2$, which is well within the common mode operating range. The minus input is biased through the magnetic transducer. This allows large signal swings to be handled without exceeding the input voltage limits. A symmetrical square wave output is insured through the positive feedback resistor R_3. Resistors R_1 and R_2 can be used to set the DC bias voltage at the positive input at any desired voltage within the input common mode voltage range of the comparator.

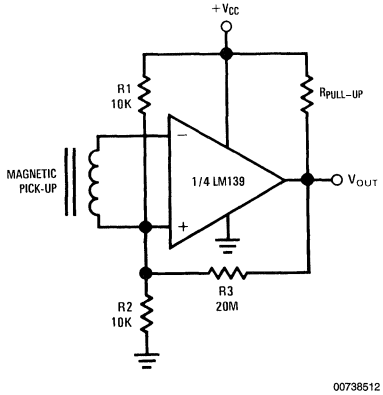


FIGURE 12. Magnetic Transducer Amplifier

Oscillators Using the LM139

The LM139 lends itself well to oscillator applications for frequencies below several megacycles. *Figure 13* shows a symmetrical square wave generator using a minimum of components. The output frequency is set by the RC time constant of R_4 and C_1 and the total hysteresis of the loop is set by R_1, R_2 and R_3. The maximum frequency is limited only by the large signal propagation delay of the comparator in addition to any capacitive loading at the output which would degrade the output slew rate.

To analyze this circuit assume that the output is initially high. For this to be true, the voltage at the negative input must be less than the voltage at the positive input. Therefore, capacitor C_1 is discharged. The voltage at the positive input, V_{A1}, will then be given by:

$$V_{A1} = \frac{+V_{CC}\, R_2}{R_2 + (R_1 \parallel R_3)} \tag{13}$$

where if $R_1 = R_2 = R_3$

then

$$V_{A1} = \frac{2\,V_{CC}}{3} \tag{14}$$

Capacitor C_1 will charge up through R_4 so that when it has charged up to a value equal to V_{A1}, the comparator output will switch. With the output V_O = GND, the value of V_A is reduced by the hysteresis network to a value given by:

$$V_{A2} = \frac{+V_{CC}}{3} \tag{15}$$

using the same resistor values as before. Capacitor C_1 must now discharge through R_4 towards ground. The output will return to its high state ($V_O = +V_{CC}$) when the voltage across the capacitor has discharged to a value equal to V_{A2}. For the circuit shown, the period for one cycle of oscillation will be twice the time it takes for a single RC circuit to charge up to one half of its final value. The period can be calculated from:

$$V_1 = V_{MAX} e^{-t_1/RC} \tag{16}$$

where

$$V_{MAX} = \frac{2\,V_{CC}}{3} \tag{17}$$

and

$$V_1 = \frac{V_{MAX}}{2} = \frac{V_{CC}}{3} \tag{18}$$

Oscillators Using the LM139 (Continued)

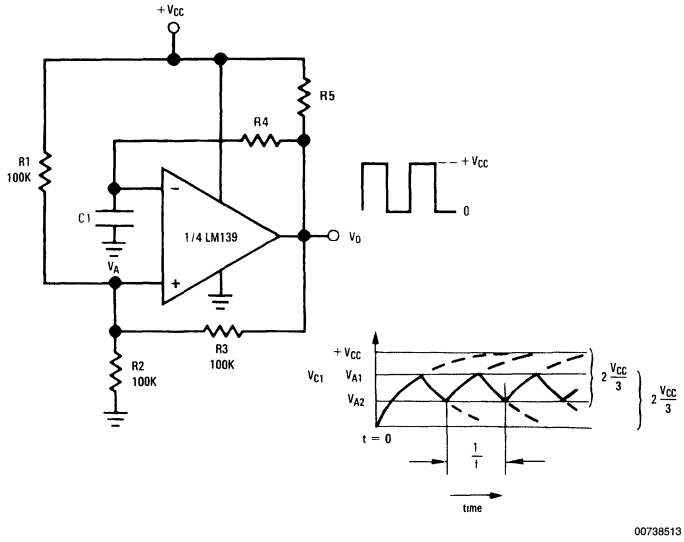


FIGURE 13. Square Wave Generator

One period will be given by:

$$\frac{1}{\text{freq.}} = 2t_1 \qquad (19)$$

or calculating the exponential gives

$$\frac{1}{\text{freq.}} = 2\,(0.694)\,R_4\,C_1 \qquad (20)$$

Resistors R_3 and R_4 must be at least 10 times larger than R_5 to insure that V_O will go all the way up to $+V_{CC}$ in the high state. The frequency stability of this circuit should strictly be a function of the external components.

Pulse Generator with Variable Duty Cycle

The basic square wave generator of *Figure 13* can be modified to obtain an adjustable duty cycle pulse generator, as shown in *Figure 14*, by providing a separate charge and discharge path for capacitor C_1. One path, through R_4 and D_1 will charge the capacitor and set the pulse width (t_1). The other path, R_5 and D_2, will discharge the capacitor and set the time between pulses (t_2). By varying resistor R_5, the time between pulses of the generator can be changed without changing the pulse width. Similarly, by varying R_4, the pulse width will be altered without affecting the time between pulses. Both controls will change the frequency of the generator, however. With the values given in *Figure 14*, the pulse width and time between pulses can be found from:

$$V_1 = V_{MAX}\,(1 - e^{-t_1/R_4C_1}) \quad \text{risetime} \qquad (21)$$

$$V_1 = V_{MAX}\,e^{-t_2/R_5C_1} \quad \text{falltime} \qquad (22)$$

where

$$V_{MAX} = \frac{2\,V_{CC}}{3} \qquad (23)$$

and

$$V_1 = \frac{V_{MAX}}{2} = \frac{V_{CC}}{3} \qquad (24)$$

which gives

$$\frac{1}{2} = e^{-t_1/R_4C_1} \qquad (25)$$

t_2 is then given by:

$$\frac{1}{2} = e^{-t_2/R_5C_1} \qquad (26)$$

These terms will have a slight error due to the fact that V_{MAX} is not exactly equal to $\frac{2}{3}\,V_{CC}$ but is actually reduced by the diode drop to:

$$V_{MAX} = \frac{2}{3}(V_{CC} - V_{BE}) \qquad (27)$$

therefore

$$\frac{1}{2\,(1 - V_{BE})} = e^{-t_1/R_4C_1} \qquad (28)$$

and

Pulse Generator with Variable Duty Cycle (Continued)

$$\frac{1}{2\,(1 - V_{BE})} = e^{-t_2/R_5C_1} \qquad (29)$$

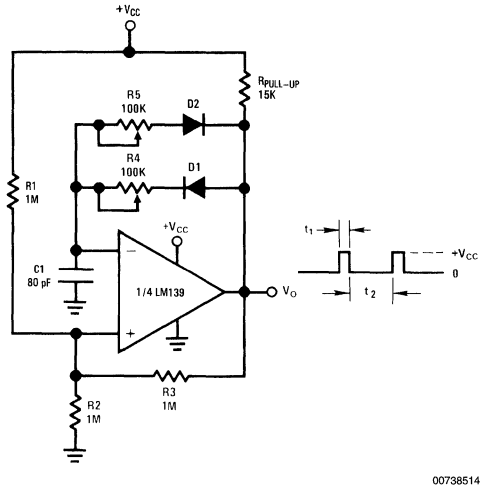


FIGURE 14. Pulse Generator with Variable Duty Cycle

Crystal Controlled Oscillator

A simple yet very stable oscillator can be obtained by using a quartz crystal resonator as the feedback element. *Figure 15* gives a typical circuit diagram of this. This value of R_1 and R_2 are equal so that the comparator will switch symmetrically about $+V_{CC}/2$. The RC time constant of R_3 and C_1 is set to be several times greater than the period of the oscillating frequency, insuring a 50% duty cycle by maintaining a DC voltage at the inverting input equal to the absolute average of the output waveform.

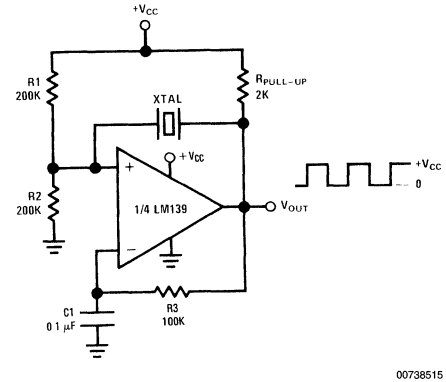


FIGURE 15. Crystal Controlled Oscillator

When specifying the crystal, be sure to order series resonant along with the desired temperature coefficient and load capacitance to be used.

MOS Clock Driver

The LM139 can be used to provide the oscillator and clock delay timing for a two phase MOS clock driver (see *Figure 16*). The oscillator is a standard comparator square wave generator similar to the one shown in *Figure 13*. Two other comparators of the LM139 are used to establish the desired phasing between the two outputs to the clock driver. A more detailed explanation of the delay circuit is given in the section under "Digital and Switching Circuits."

Wide Range VCO

A simple yet very stable voltage controlled oscillator using a mimimum of external components can be realized using three comparators of the LM139. The schematic is shown in *Figure 17a*. Comparator 1 is used closed loop as an integrator (for further discussion of closed loop operation see section on Operational Amplifiers) with comparator 2 used as a triangle to square wave converter and comparator 3 as the switch driving the integrator. To analyze the circuit, assume that comparator 2 is its high state ($V_{SQ} = +V_{CC}$) which drives comparator 3 to its high state also. The output device of comparator 3 will be OFF which prevents any current from flowing through R_2 to ground. With a control voltage, V_C, at the input to comparator 1, a current I_1 will flow through R_1 and begin discharging capacitor C_1, at a linear rate. This discharge current is given by:

$$I_1 = \frac{V_C}{2\,R_1} \tag{30}$$

and the discharge time is given by:

$$I_1 = C_1 \frac{\Delta V}{\Delta t} \tag{31}$$

ΔV will be the maximum peak change in the voltage across capacitor C_1 which will be set by the switch points of comparator 2. These trip points can be changed by simply altering the ratio of R_F to R_S, thereby increasing or decreasing the amount of hysteresis around comparator 2. With R_F = 100 kΩ and R_S = 5 kΩ, the amount of hysteresis is approximately ±5% which will give switch points of $+V_{CC}/2$ ±750 mV from a 30V supply (See "Comparators with Hysteresis")

As capacitor C_1 discharges, the output voltage of comparator 1 will decrease until it reaches the lower trip point of comparator 2, which will then force the output of comparator 2 to go to its low state (V_{SQ} = GND).

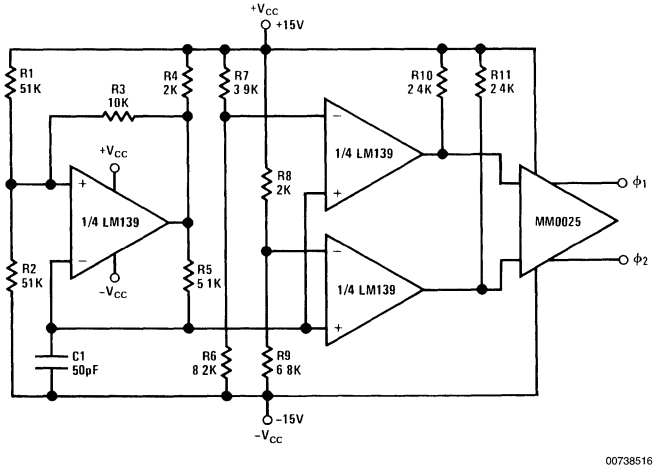


FIGURE 16. MOS Clock Driver

Wide Range VCO (Continued)

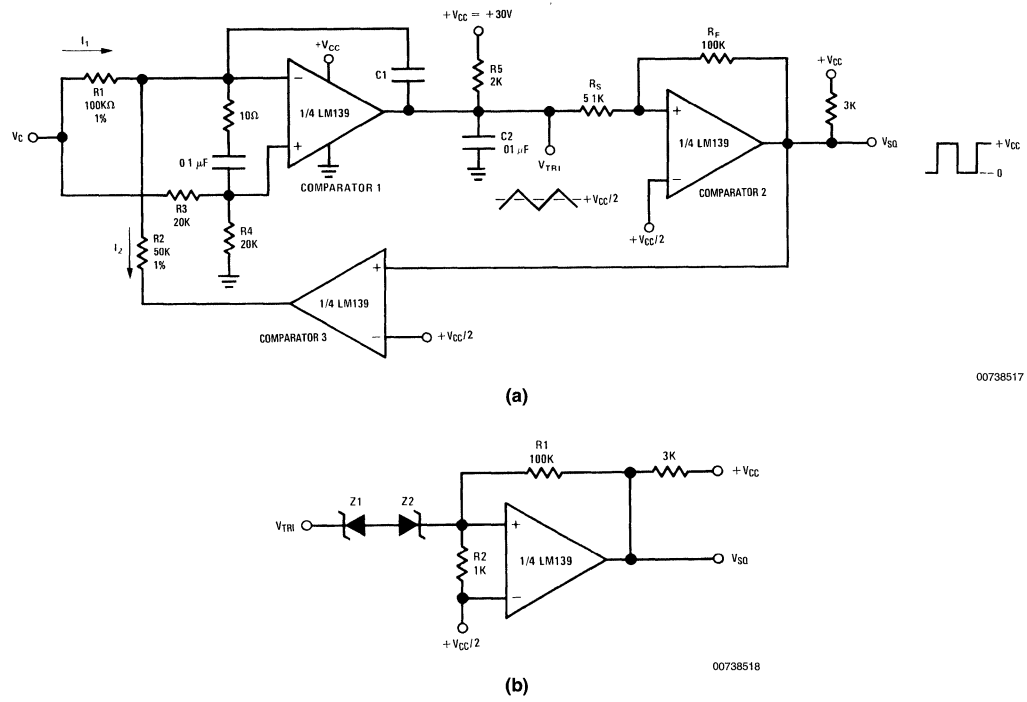


FIGURE 17. Voltage Controlled Oscillator

This in turn causes comparator 3 to go to its low state where its output device will be in saturation. A current I_2 can now flow through resistor R_2 to ground. If the value of R_2 is chosen as $R_1/2$ a current equal to the capacitor discharge current can be made to flow out of C_1 charging it at the same rate as it was discharged. By making $R_2 = R_1/2$, current I_2 will equal twice I_1. This is the control circuitry which guararantees a constant 50% duty cycle oscillation independent of frequency or temperature. As capacitor C_1 charges, the output of comparator 1 will ramp up until it trips comparator 2 to its high state ($V_{SQ} = +V_{CC}$) and the cycle will repeat.

The circuit shown in *Figure 17a* uses a +30V supply and gives a triangle wave of 1.5V peak-to-peak. With a timing capacitor, C_1 equal to 500 pF, a frequency range from approximately 115 kHz down to approximately 670 Hz was obtained with a control voltage ranging from 50V down to 250 mV. By reducing the hysteresis around comparator 2 down to ±150 mV (R_f = 100 kΩ, R_S = 1 kΩ) and reducing the compensating capacitor C_2 down to .001 μF, frequencies up to 1 MHz may be obtained. For lower frequencies ($f_o \leq 1$ Hz) the timing capacitor, C_1, should be increased up to approximately 1 μF to insure that the charging currents, I_1 and I_2, are much larger than the input bias currents of comparator 1.

Figure 17b shows another interesting approach to provide the hysteresis for comparator 2. Two identical Zener diodes, Z_1 and Z_2, are used to set the trip points of comparator 2. When the triangle wave is less than the value required to Zener one of the diodes, the resistive network, R_1 and R_2, provides enough feedback to keep the comparator in its proper state, (the input would otherwise be floating). The advantage of this circuit is that the trip points of comparator 2 will be completely independent of supply voltage fluctuations. The disadvantage is that Zeners with less than one volt breakdown voltage are not obtainable. This limits the maximum upper frequency obtainable because of the larger amplitude of the triangle wave. If a regulated supply is available, *Figure 17a* is preferable simply because of less parts count and lower cost.

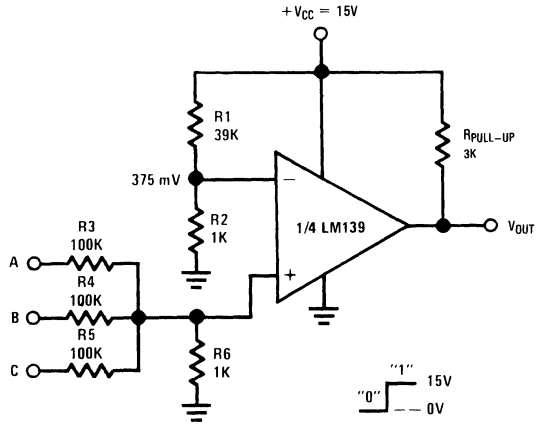
Both circuits provide good control over at least two decades in frequency with a temperature coefficient largely dependent on the TC of the external timing resistors and capacitors. Remember that good circuit layout is essential along with the 0.01 μF compensation capacitor at the output of comparator 1 and the series 10Ω resistor and 0.1 μF capacitor between its inputs, for proper operation. Comparator 1 is a high gain amplifier used closed loop as an integrator so long leads and loose layout should be avoided.

Digital and Switching Circuits

The LM139 lends itself well to low speed (<1 MHz) high level logic circuits. They have the advantage of operating with high signal levels, giving high noise immunity, which is highly desirable for industrial applications. The output signal level can be selected by setting the V_{CC} to which the pull-up resistor is connected to any desired level.

AND/NAND Gates

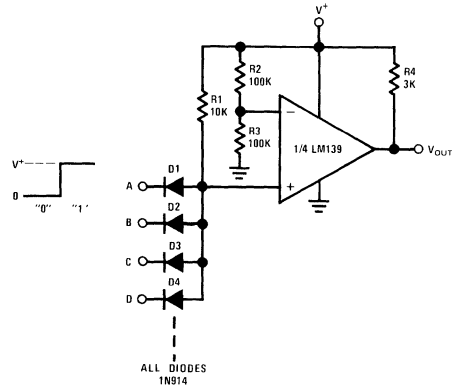
A three input AND gate is shown in *Figure 18*. Operation of this gate is as follows: resistor divider R_1 and R_2 establishes a reference voltage at the inverting input to the comparator. The non-inverting input is the sum of the voltages at the inputs divided by the voltage dividers comprised of R_3, R_4, R_5 and R_6. The output will go high only when all three inputs are high, causing the voltage at the non-inverting input to go above that at inverting input. The circuit values shown work for a "0" equal to ground and a "1" equal +15V. The resistor values can be altered if different logic levels are desired. If more inputs are required, diodes are recommended to improve the voltage margin when all but one of the inputs are the "1" state. This circuit with increased fan-in is shown in *Figure 19*.



$V_{OUT} = A \bullet B \bullet C$

FIGURE 18. Three Input AND Gate

To convert these AND gates to NAND gates simply interchange the inverting and non-inverting inputs to the comparator. Hysteresis can be added to speed up output transitions if low speed input signals are used.

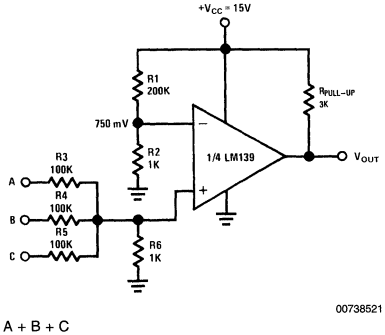


$V_{OUT} = A \bullet B \bullet C \bullet D$

FIGURE 19. AND Gate with Large Fan-In

OR/NOR Gates

The three input OR gate (positive logic) shown in *Figure 20* is achieved from the basic AND gate simply by increasing R_1 thereby reducing the reference voltage. A logic "1" at any of the inputs will produce a logic "1" at the output. Again a NOR gate may be implemented by simply reversing the comparator inputs. Resistor R_6 may be added for the OR or NOR function at the expense of noise immunity if so desired.



$V_{OUT} = A + B + C$

FIGURE 20. Three Input OR Gate

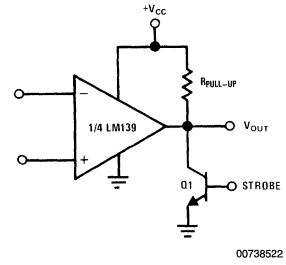


FIGURE 21. Output Strobing Using a Discrete Transistor

Output Strobing

The output of the LM139 may be disabled by adding a clamp transistor as shown in *Figure 21*. A strobe control voltage at the base of Q_1 will clamp the comparator output to ground, making it immune to any input changes.

If the LM139 is being used in a digital system the output may be strobed using any other type of gate having an uncommitted collector output (such as National's DM5401/DM7401). In addition another comparator of the LM139 could also be used for output strobing, replacing Q_1 in *Figure 21*, if desired. (See *Figure 22*.)

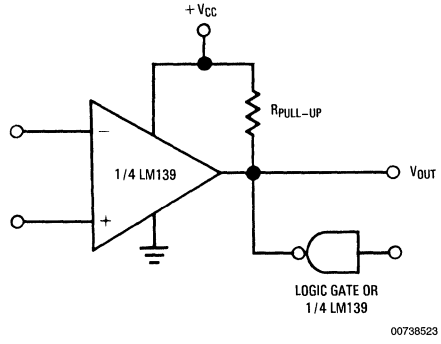


FIGURE 22. Output Strobing with TTL Gate

One Shot Multivibrators

A simple one shot multivibrator can be realized using one comparator of the LM139 as shown in *Figure 23*. The output pulse width is set by the values of C_2 and R_4 (with $R_4 > 10$ R_3 to avoid loading the output). The magnitude of the input trigger pulse required is determined by the resistive divider R_1 and R_2. Temperature stability can be achieved by balancing the temperature coefficients of R_4 and C_2 or by using components with very low TC. In addition, the TC of resistors R_1 and R_2 should be matched so as to maintain a fixed reference voltage of $+V_{CC}/2$. Diode D_2 provides a rapid discharge path for capacitor C_2 to reset the one shot at the end of its pulse. It also prevents the non-inverting input from being driven below ground. The output pulse width is relatively independent of the magnitude of the supply voltage and will change less than 2% for a five volt change in $+V_{CC}$.

One Shot Multivibrators (Continued)

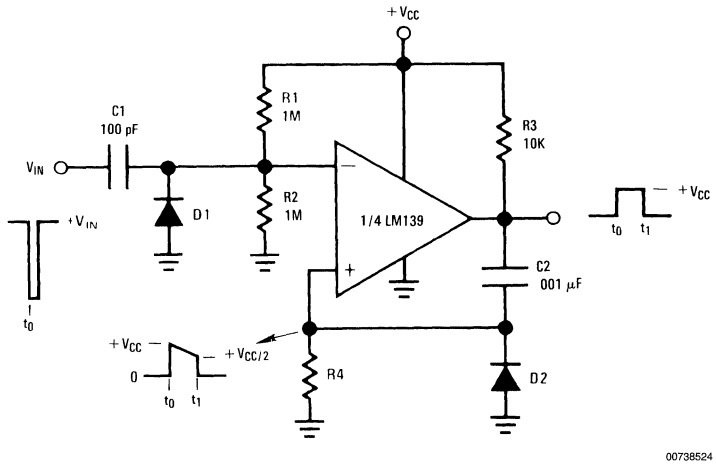


FIGURE 23. One Shot Multivibrator

The one shot multivibrator shown in *Figure 24* has several characteristics which make it superior to that shown in *Figure 23*. First, the pulse width is independent of the magnitude of the power supply voltage because the charging voltage and the intercept voltage are a fixed percentage of $+V_{CC}$. In addition this one-shot is capable of 99% duty cycle and exhibits input trigger lock-out to insure that the circuit will not re-trigger before the output pulse has been completed. The trigger level is the voltage required at the input to raise the voltage at point A higher than the voltage at point B, and is set by the resistive divider R_4 and R_{10} and the network R_1, R_2 and R_3. When the multivibrator has been triggered, the output of comparator 2 is high causing the reference voltage at the non-inverting input of comparator 1 to go to $+V_{CC}$. This prevents any additional input pulses from disturbing the circuit until the output pulse has been completed.

The value of the timing capacitor, C_1, must be kept small enough to allow comparator 1 to completely discharge C_1 before the feedback signal from comparator 2 (through R_{10}) switches comparator 1 OFF and allows C_1 to start an exponential charge. Proper circuit action depends on rapidly discharging C_1 to a value set by R_6 and R_9 at which time comparator 2 latches comparator 1 OFF. Prior to the establishment of this OFF state, C_1 will have been completely discharged by comparator 1 in the ON state. The time delay, which sets the output pulse width, results from C_1 recharging to the reference voltage set by R_6 and R_9. When the voltage across C_1 charges beyond this reference, the output pulse returns to ground and the input is again reset to accept a trigger.

Bistable Multivibrator

Figure 25 is the circuit of one comparator of the LM139 used as a bistable multivibrator. A reference voltage is provided at the inverting input by a voltage divider comprised of R_2 and R_3. A pulse applied to the SET terminal will switch the output high. Resistor divider network R_1, R_4, and R_5 now clamps the non-inverting input to a voltage greater than the reference voltage. A pulse now applied to the RESET Input will pull the output low. If both Q and $\overline{Q}$ outputs are needed, another comparator can be added as shown dashed in *Figure 25*.

Bistable Multivibrator (Continued)

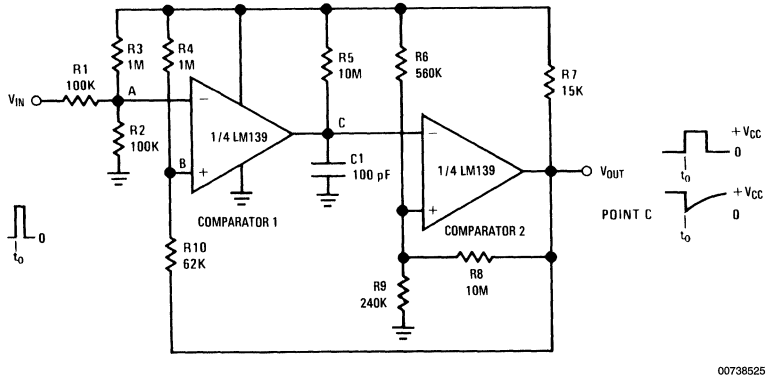


FIGURE 24. Multivibrator with Input Lock-Out

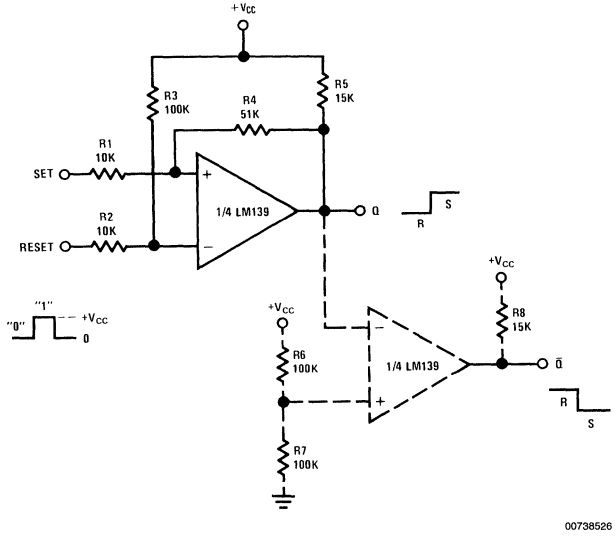


FIGURE 25. Bistable Multivibrator

Figure 26 shows the output saturation voltage of the LM139 comparator versus the amount of current being passed to ground. The end point of 1 mV at zero current along with an R_{SAT} of 60Ω shows why the LM139 so easily adapts itself to oscillator and digital switching circuits by allowing the DC output voltage to go practically to ground while in the ON state.

Bistable Multivibrator (Continued)

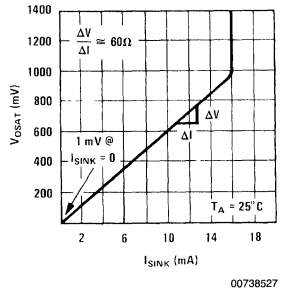


FIGURE 26. Typical Output Saturation Characteristics

Time Delay Generator

The final circuit to be presented "Digital and Switching Circuits" is a time delay generator (or sequence generator) as shown in *Figure 27*.

This timer will provide output signals at prescribed time intervals from a time reference t_o and will automatically reset when the input signal returns to ground. For circuit evaluation, first consider the quiescent state (V_{IN} = O) where the output of comparator 4 is ON which keeps the voltage across C_1 at zero volts. This keeps the outputs of comparators 1, 2 and 3 in their ON state (V_{OUT} = GND). When an input signal is applied, comparator 4 turns OFF allowing C_1 to charge at an exponential rate through R_1. As this voltage rises past the present trip points V_A, V_B, and V_C of comparators 1, 2 and 3 respectively, the output voltage of each of these comparators will switch to the high state (V_{OUT} = $+V_{CC}$). A small amount of hysteresis has been provided to insure fast switching for the case where the R_C time constant has been chosen large to give long delay times. It is not necessary that all comparator outputs be low in the quiescent state. Several or all may be reversed as desired simply by reversing the inverting and non-inverting input connections. Hysteresis again is optional.

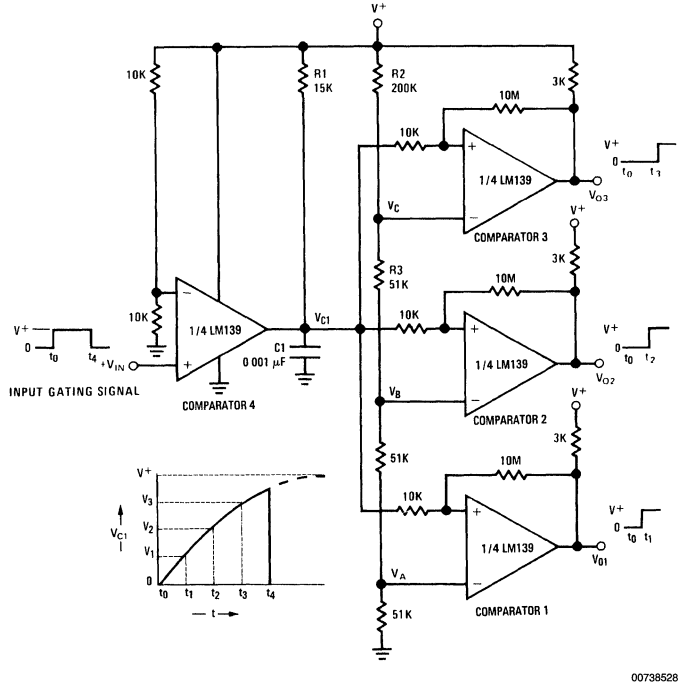


FIGURE 27. Time Delay Generator

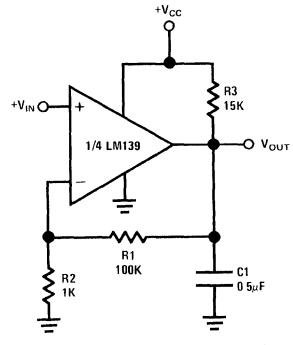
Low Frequency Operational Amplifiers

The LM139 comparator can be used as an operational amplifier in DC and very low frequency AC applications (≤100 Hz). An interesting combination is to use one of the comparators as an op amp to provide a DC reference voltage for the other three comparators in the same package.

Another useful application of an LM139 has the interesting feature that the input common mode voltage range includes ground even though the amplifier is biased from a single supply and ground. These op amps are also low power drain devices and will not drive large load currents unless current is boosted with an external NPN transistor. The largest ap-

Low Frequency Operational Amplifiers (Continued)

plication limitation comes from a relatively slow slew rate which restricts the power bandwidth and the output voltage response time.



$$A_V = 1 + \frac{R1}{R2} = 101$$

FIGURE 28. Non-Inverting Amplifier

The LM139, like other comparators, is not internally frequency compensated and does not have internal provisions for compensation by external components. Therefore, compensation must be applied at either the inputs or output of the device. *Figure 28* shows an output compensation scheme which utilizes the output collector pull-up resistor working with a single compensation capacitor to form a dominant pole. The feedback network, R_1 and R_2 sets the closed loop gain at $1 + R_1/R_2$ or 101 (40 dB). *Figure 29* shows the output swing limitations versus frequency. The output current capability of this amplifier is limited by the relatively large pull-up resistor (15 kΩ) so the output is shown boosted with an external NPN transistor in *Figure 30*. The frequency response is greatly extended by the use of the new compensation scheme also shown in *Figure 30*. The DC level shift due to the V_{BE} of Q_1 allows the output voltage to swing from ground to approximately one volt less than $+V_{CC}$. A voltage offset adjustment can be added as shown in *Figure 31*.

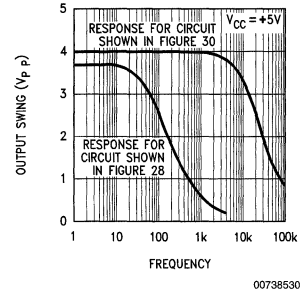


FIGURE 29. Large Signal Frequency Response

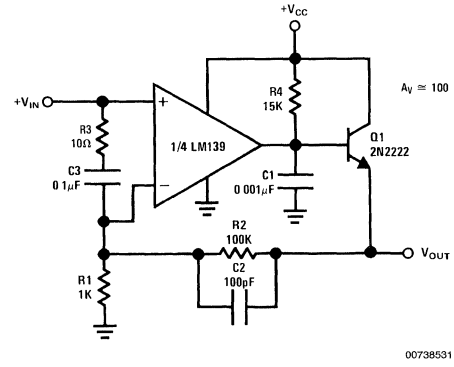
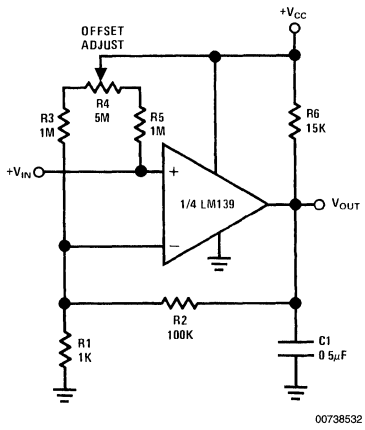


FIGURE 30. Improved Operational Amplifier

Low Frequency Operational Amplifiers (Continued)



$A_V \cong 100$

FIGURE 31. Input Offset Null Adjustment

Dual Supply Operation

The applications presented here have been shown biased typically between $+V_{CC}$ and ground for simplicity. The LM139, however, works equally well from dual (plus and minus) supplies commonly used with most industry standard op amps and comparators, with some applications actually requiring fewer parts than the single supply equivalent.

The zero crossing detector shown in *Figure 10* can be implemented with fewer parts as shown in *Figure 32*. Hysteresis has been added to insure fast transitions if used with slowly moving input signals. It may be omitted if not needed, bringing the total parts count down to one pull-up resistor.

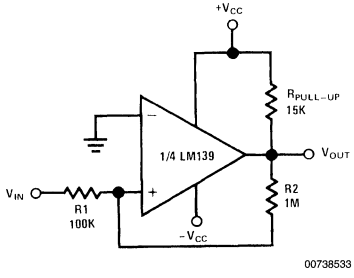


FIGURE 32. Zero Crossing Detector Using Dual Supplies

The MOS clock driver shown in *Figure 16* uses dual supplies to properly drive the MM0025 clock driver.

The square wave generator shown in *Figure 13* can be used with dual supplies giving an output that swings symmetrically above and below ground (see *Figure 33*). Operation is identical to the single supply oscillator with only change being in the lower trip point.

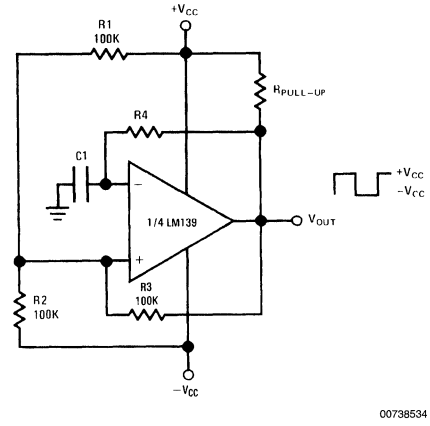


FIGURE 33. Squarewave Generator Using Dual Supplies

Figure 34 shows an LM139 connected as an op amp using dual supplies. Biasing is actually simpler if full output swing at low gain settings is required by biasing the inverting input from ground rather than from a resistive divider to some voltage between $+V_{CC}$ and ground.

All the applications shown will work equally well biased with dual supplies. If the total voltage across the device is increased from that shown, the output pull-up resistor should be increased to prevent the output transistor from being pulled out of saturation by drawing excessive current, thereby preventing the output low state from going all the way to $-V_{CC}$.

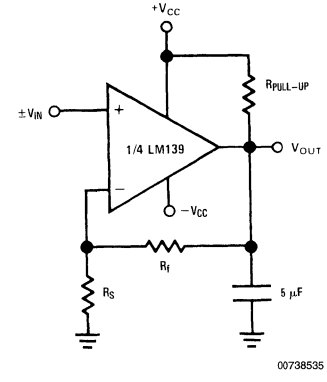


FIGURE 34. Non-Inverting Amplifier Using Dual Supplies

Miscellaneous Applications

The following is a collection of various applications intended primarily to further show the wide versatility that the LM139 quad comparator has to offer. No new modes of operation are presented here so all of the previous formulas and circuit descriptions will hold true. It is hoped that all of the circuits presented in this application note will suggest to the user a few of the many areas in which the LM139 can be utilized.

Remote Temperature Sensor/Alarm

The circuit shown in *Figure 35* shows a temperature over-range limit sensor. The 2N930 is a National process 07 silicon NPN transistor connected to produce a voltage reference equal to a multiple of its base emitter voltage along with temperature coefficient equal to a multiple of 2.2 mV/°C.

That multiple is determined by the ratio of R_1 to R_2. The theory of operation is as follows: with transistor Q_1 biased up, its base to emitter voltage will appear across resistor R_1. Assuming a reasonably high beta ($\beta \geq 100$) the base current can be neglected so that the current that flows through resistor R_1 must also be flowing through R_2. The voltage drop across resistor R_2 will be given by:

$$I_{R1} = I_{R2}$$

and

$$V_{R1} = V_{be} = I_{R1}\, R_1$$

so

$$V_{R2} = I_{R2}\, R_2 = I_{R1}\, R_2 = V_{be}\, \frac{R_2}{R_1} \qquad (32)$$

As stated previously this base-emitter voltage is strongly temperature dependent, minus 2.2 mV/°C for a silicon transistor. This temperature coefficient is also multiplied by the resistor ratio R_1/R_2.

This provides a highly linear, variable temperature coefficient reference which is ideal for use as a temperature sensor over a temperature range of approximately −65°C to +150°C. When this temperature sensor is connected as shown in *Figure 35* it can be used to indicate an alarm condition of either too high or too low a temperature excursion. Resistors R_3 and R_4 set the trip point reference voltage, V_B, with switching occuring when $V_A = V_B$. Resistor R_5 is used to bias up Q_1 at some low value of current simply to keep quiescent power dissipation to a minimum. An I_Q near 10 µA is acceptable.

Using one LM139, four separate sense points are available. The outputs of the four comparators can be used to indicate four separate alarm conditions or the outputs can be OR'ed together to indicate an alarm condition at any one of the sensors. For the circuit shown the output will go HIGH when the temperature of the sensor goes above the preset level. This could easily be inverted by simply reversing the input leads. For operation over a narrow temperature range, the resistor ratio R_2/R_1 should be large to make the alarm more sensitive to temperature variations. To vary the trip points a potentiometer can be substituted for R_3 and R_4. By the addition of a single feedback resistor to the non-inverting input to provide a slight amount of hysteresis, the sensor could function as a thermostat. For driving loads greater than 15 mA, an output current booster transistor could be used.

Four Independently Variable, Temperature Compensated, Reference Supplies

The circuit shown in *Figure 36* provides four independently variable voltages that could be used for low current supplies for powering additional equipment or for generating the reference voltages needed in some of the previous comparator applications. If the proper Zener diode is chosen, these four voltages will have a near zero temperature coefficient. For industry standard Zeners, this will be somewhere between 5.0 and 5.4V at a Zener current of approximately 10 mA. An alternative solution is offered to reduce this 50 mW quiescent power drain. Experimental data has shown that any of National's process 21 transistors which have been selected for low reverse beta ($\beta_R < .25$) can be used quite satisfactorily as a zero T.C. Zener. When connected as shown in *Figure 37*, the T.C. of the base-emitter Zener voltage is exactly cancelled by the T.C. of the forward biased base-collector junction if biased at 1.5 mA. The diode can be properly biased from any supply by adjusting R_S to set I_q equal to 1.5 mA. The outputs of any of the reference supplies can be current boosted by using the circuit shown in *Figure 30*.

Four Independently Variable, Temperature Compensated, Reference Supplies (Continued)

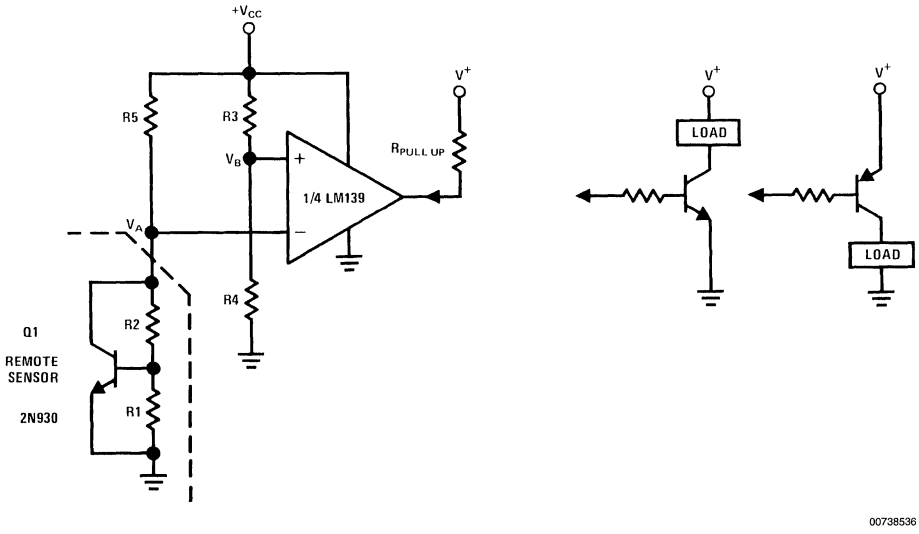


FIGURE 35. Temperature Alarm

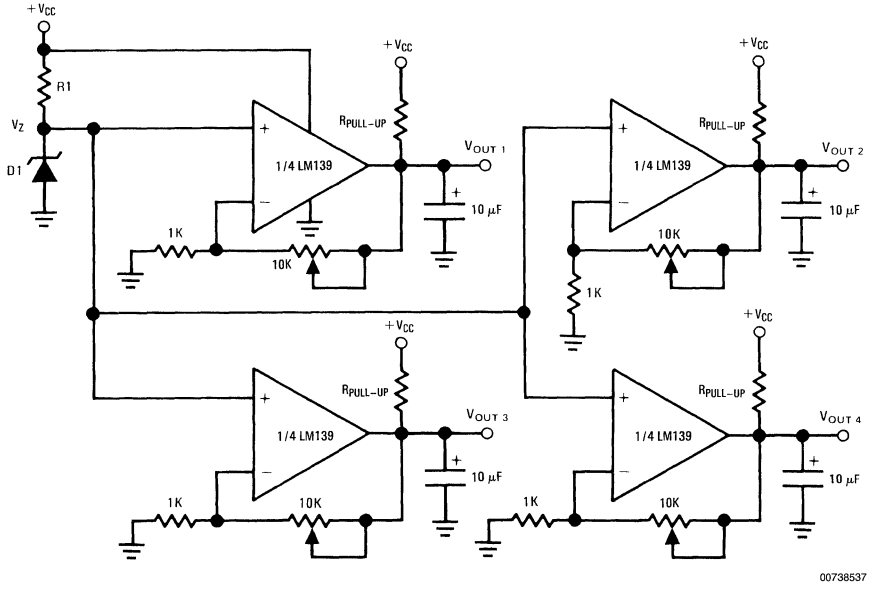
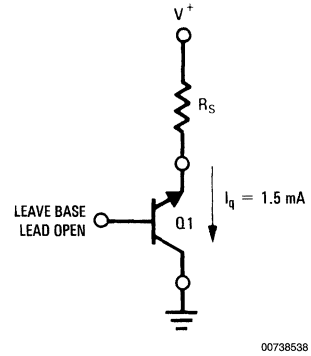


FIGURE 36. Four Variable Reference Supplies

Four Independently Variable, Temperature Compensated, Reference Supplies (Continued)



Q1 = National Process 21 Selected for Low Reverse β

FIGURE 37. Zero T.C. Zener

Digital Tape Reader

Two circuits are presented here–a tape reader for both magnetic tape and punched paper tape. The circuit shown in *Figure 38*, the magnetic tape reader, is the same as *Figure 12* with a few resistor values changed. With a 5V supply, to make the output TTL compatible, and a 1 MΩ feedback resistor, ±5 mV of hysteresis is provided to insure fast switching and higher noise immunity. Using one LM139, four tape channels can be read simultaneously.

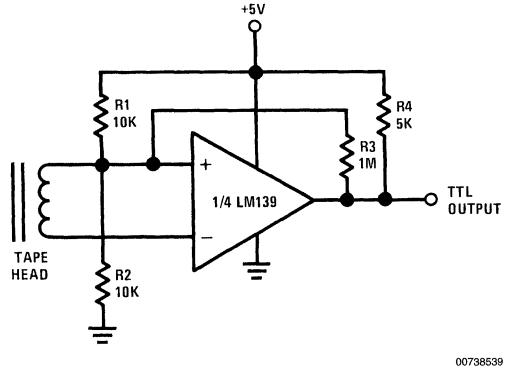


FIGURE 38. Magnetic Tape Reader with TTL Output

Digital Tape Reader (Continued)

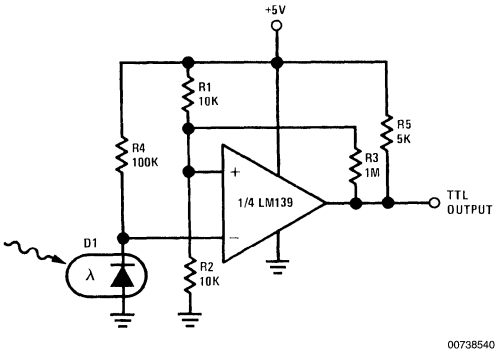


FIGURE 39. Paper Tape Reader With TTL Output

The paper tape reader shown in *Figure 39* is essentially the same circuit as *Figure 38* with the only change being in the type of transducer used. A photo-diode is now used to sense the presence or absence of light passing through holes in the tape. Again a 1 MΩ feedback resistor gives ±5 mV of hysteresis to insure rapid switching and noise immunity.

Pulse Width Modulator

Figure 40 shows the circuit for a simple pulse width modulator circuit. It is essentially the same as that shown in *Figure 13* with the addition of an input control voltage. With the input control voltage equal to $+V_{CC}/2$, operation is basically the same as that described previously. If the input control voltage is moved above or below $+V_{CC}/2$, however, the duty cycle of the output square wave will be altered. This is because the addition of the control voltage at the input has now altered the trip points. These trip points can be found if the circuit is simplified as in *Figure 41*. Equations 13 through 20 are still applicable if the effect of R_C is added, with equations 17 through 20 being altered for condition where $V_C \neq +V_{CC}/2$.

Pulse width sensitivity to input voltage variations will be increased by reducing the value of R_C from 10 kΩ and alternately, sensitivity will be reduced by increasing the value of R_C. The values of R_1 and C_1 can be varied to produce any desired center frequency from less than one hertz to the maximum frequency of the LM139 which will be limited by $+V_{CC}$ and the output slew rate.

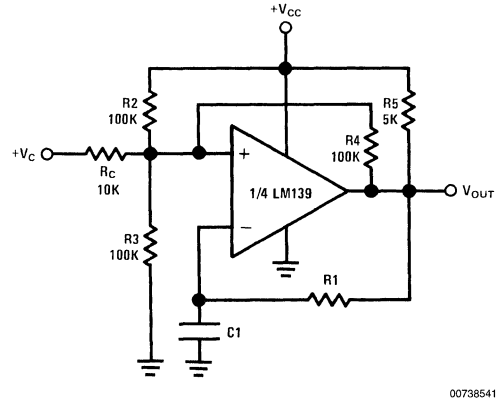
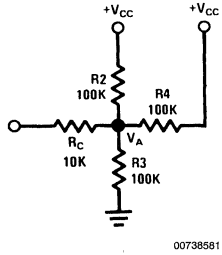
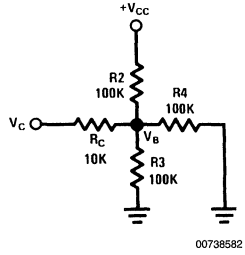


FIGURE 40. Pulse Width Modulator

Pulse Width Modulator (Continued)



V_A = UPPER TRIP POINT



V_B = LOWER TRIP POINT

FIGURE 41. Simplified Circuit For Calculating Trip Points of *Figure 40*

Positive and Negative Peak Detectors

Figures 42, 43 show the schematics for simple positive or negative peak detectors. Basically the LM139 is operated closed loop as a unity gain follower with a large holding capacitor from the output to ground. For the positive peak detector a low impedance current source is needed so an additional transistor is added to the output. When the output of the comparator goes high, current is passed through Q_1 to charge up C_1. The only discharge path will be the 1 MΩ resistor shunting C_1 and any load that is connected to V_{OUT}. The decay time can be altered simply by changing the 1 MΩ resistor higher or lower as desired. The output should be used through a high impedance follower to avoid loading the output of the peak detector.

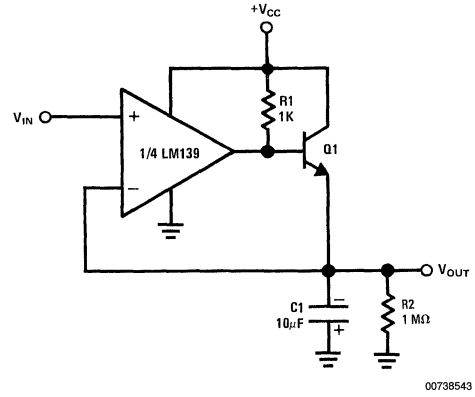


FIGURE 42. Positive Peak Detector

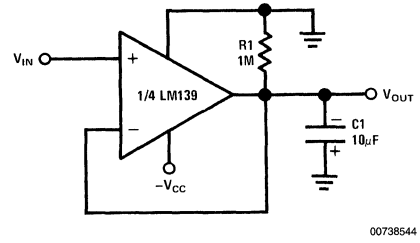


FIGURE 43. Negative Peak Detector

For the negative peak detector, a low impedance current sink is required and the output transistor of the LM139 works quite well for this. Again the only discharge path will be the 1 MΩ resistor and any load impedance used. Decay time is changed by varying the 1 MΩ resistor.

Conclusion

The LM139 is an extremely versatile comparator package offering reasonably high speed while operating at power levels in the low mW region. By offering four independent comparators in one package, many logic and other functions can now be performed at substantial savings in circuit complexity, parts count, overall physical dimensions, and power consumption.

For limited temperature range application, the LM239 or LM339 may be used in place of the LM139.

It is hoped that this application note will provide the user with a guide for using the LM139 and also offer some new application ideas.

IC Preamplifier Challenges Choppers on Drift

National Semiconductor
Application Note 79
Robert J. Widlar

Since the introduction of monolithic IC amplifiers there has been a continual improvement in DC accuracy. Bias currents have been decreased by 5 orders of magnitude over the past 5 years. Low offset voltage drift is also necessary in a high accuracy circuits. This is evidenced by the popularity of low drift amplifier types as well as the requests for selected low-drift op amps. However, until now the chopper stabilized amplifier offered the lowest drift. A new monolithic IC preamplifier designed for use with general purpose op amps improves DC accuracy to where the drift is lower than many chopper stabilized amplifiers.

Introduction

Chopper amplifiers have long been known to offer the lowest possible DC drift. They are not without problems, however. Most chopper amps can be used only as inverting amplifiers, limiting their applications. Chopping can introduce noise and spikes into the signal Mechanical choppers need replacement as well as being shock sensitive. Further, chopper amplifiers are designed to operate over a limited power supply, limited temperature range.

Previous low-drift op amps do not provide optimum performance either. Selected devices may only meet their specified voltage drift under restrictive conditions. For example, if a 741 device is selected without offset nulling, the addition of a offset null pot can drastically change the drift. Low drift op amps designed for offset balancing have another problem. The resistor network used in the null circuit is designed to null the drift when the offset voltage is nulled. The mechanism to achieve nulled drift depends on the difference in temperature coefficient between the internal resistors and the external null pot. Since the internal resistors have a non-linear temperature coefficient and may vary device to device as well as between manufacturers, it can only approximately null offset drift. The problem gets worse if the external null pot has a TC other than zero.

A new IC preamplifier is now available which can give drifts as low as 0.2 µV/°C. It is used with conventional op amps and eliminates the problems associated with older devices. As well as improving the DC input characteristics of the op amp, loop-gain is increased when an LM121 is used. This further improves overall accuracy since DC gain error is decreased.

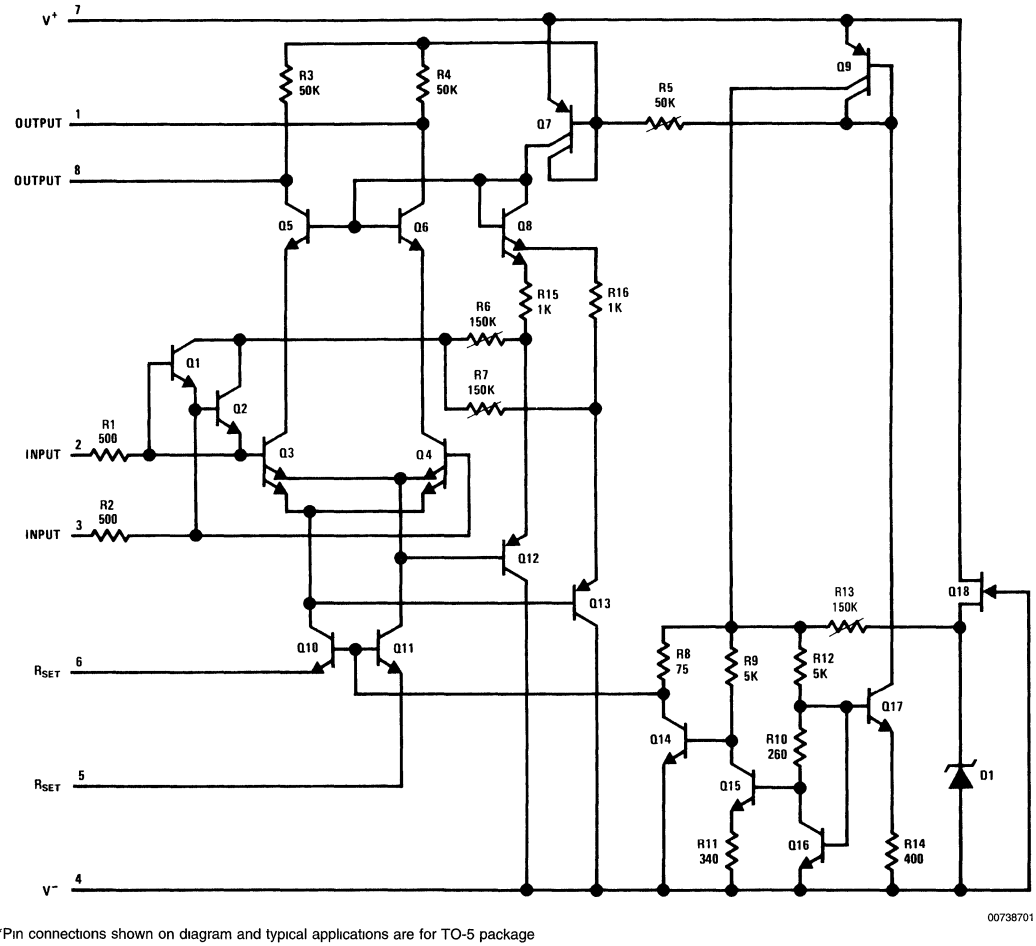
The LM121 preamp is designed to give zero drift when the offset voltage is nulled to zero. The operating current of the LM121 is programmable by the value of the null network resistors. The drift is independent of the value of the nulling network so it can be used over a wide range of operating currents while retaining low drift. The operating current can be chosen to optimize bias current, gain, speed, or noise while still retaining the low drift. Further, since the drift is independent of the match between external and internal resistors when the offset is nulled, lower and more predictable drifts can be expected in actual use. The input is fully differential, overcoming many of the problems with single ended chopper-amps. The device also has enough common mode rejection ratio to allow the low drift to be fully utilized.

Circuit Description

The LM121 is a well matched differential amplifier utilizing super-gain transistors as the input devices. A schematic is shown in *Figure 1*. The input signal is applied to the bases of Q_3 and Q_4 through protection resistors R_1 and R_2. Q_3 and Q_4 have two emitters to allow offset balancing which will be explained later. The operating current for the differential amplifier is supplied by current sources Q_{10} and Q_{11}. The operating current is externally programmed by resistors connected from the emitters of Q_{10} and Q_{11} to the negative supply. Input transistors Q_3 and Q_4 are cascoded by transistors Q_5 and Q_6 to keep the collector base voltage on the input stage equal to zero. This eliminates leakage at high operating temperatures and keeps the common mode input voltage from appearing across the low breakdown super-gain input transistors. Additionally, the cascode improves the common mode rejection of the differential amplifier. Q_1 and Q_2 protect the input against large differential voltages.

The ouput signal is developed across resistive loads R_3 and R_4. The total collector current of the input is then applied to the base of a fixed gain PNP, Q_7. The collector current of Q_7 sets the operating current of Q_8, Q_{12}, and Q_{13}. These transistors are used to set the operating voltage of the cascode, Q_5 and Q_6. By operating the cascode biasing transistors at the same operating current as the input stage, it is possible to keep collector base voltage at zero; and therefore, collector-base leakage remains low over a wide current range. Further, this minimizes the effects of V_{BE} variations and finite transistor current gain. At high operating currents the collector base voltage of the input stage is increased by about 100 mV due to the drop across R_{15} and R_{16}. This prevents the input transistors from saturating under worst case conditions of high current and high operating temperature.

Circuit Description (Continued)



*Pin connections shown on diagram and typical applications are for TO-5 package

FIGURE 1. Schematic Diagram of the LM121

The rest of the devices comprise the turn-on and regulator circuitry. Transistors Q_{14}, Q_{15}, and Q_{16} form a 1.2V regulator for the bases of the input stage current source. By fixing the bases of the current sources at 1.2V, their ouput current changes proportional to absolute temperature. This compensates for the temperature sensitivity of the input stage transconductance. Temperature compensating the transconductance makes the preamp more useful in some applications such as an instrumentation amplifier and minimizes bandwidth variations with temperature. The regulator is started by Q_{18} and its operating current is supplied by Q_{17} and Q_9, *Figure 2* shows the LM121 chip.

Offset Balancing

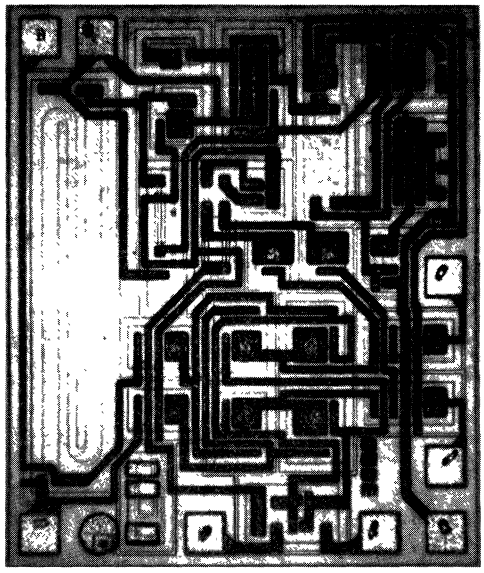
The LM121 was designed to operate with an offset balancing network connected to the current source transistors. The method of balancing the offset also minimizes the drift of the preamp. Unlike earlier devices such as the LM725, the LM121 depends only upon the highly predictable emitter base voltages of transistors to achieve low drift. Devices like the LM725 depend on the match between internal resistor temperature coefficient and the external null pot as well as the input stage transistors characteristics for drift compensation.

The input stage of the LM121 is actually two differential amplifiers connected in parallel, each having a fixed offset. The offset is due to different areas for the transistor emitters. The offset for each pair is given by:

$$\Delta V_{BE} = \frac{kT}{q} \ln \frac{A_1}{A_2}$$

where k is Boltzmann's constant, T is absolute temperature,

Offset Balancing (Continued)



00738702

FIGURE 2. LM121 Chip

q is the charge on an electron, and A_1 and A_2 are emitter areas. Because of the offset, each pair has a fixed drift. When the pairs are connected in parallel, if they match, the offsets and drift cancel. However, since matching is not perfect, the emitters of the pairs are not connected in parallel, but connected to independent current sources to allow offset balancing. The offset and drift effect of each pair is proportional to its operating current, so varying the ratio of the current from current sources will vary both the offset and drift. When the offset is nulled to zero, the drift is nulled to below 1 µV/°C.

The offset balancing method used in the LM121 has several advantages over conventional balancing schemes. Firstly, as mentioned earlier, it theoretically zeros the drift and offset simultaneously Secondly, since the maximum balancing range is fixed by transistor areas, the effect of null network variations on offset voltage is minimized. Resistor shifts of one percent only cause a 30 µV shift in offset voltage on the LM121, while a one percent shift in collector resistors on a standard diff amp causes a 300 µV offset change. Finally, it allows the value of the null network to set the operating current.

Achieving Low Drift

A very low drift amplifier poses some uncommon application and testing problems. Many sources of error can cause the apparent circuit drift to be much higher than would be predicted. In many cases, the low drift of the op amp is completely swamped by external effects while the amplifier is blamed for the high drift.

Thermocouple effects caused by temperature gradient across dissimilar metals are perhaps the worst offenders. Whenever dissimilar metals are joined, a thermocouple results. The voltage generated by the thermocouple is proportional to the temperature difference between the junction and the measurement end of the metal This voltage can range between essentially zero and hundred of microvolts per degree, depending on the metals used. In any system using integrated circuits a minimum of three metals are found: copper, solder, and kovar (lead material of the IC).

Nominally, most parts of a circuit are at the same temperature. However, a small temperature gradient can exist across even a few inches — and this is a big problem with low level signals. Only a few degrees gradient can cause hundreds of microvolts of error. The two places this shows up, generally are the package-to-printed circuit board interface and temperature gradients across resistors. Keeping package leads short and the two input leads close together help greatly.

For example, a very low drift amplifier was constructed and the output monitored over a 1 minute period. During the 1 minute it appeared to have input referred offset variations of ±5 µV. Shielding the circuit from air currents reduced this to ±0.5 µV. The 10 µV error was due to thermal gradients across the circuit from air currents.

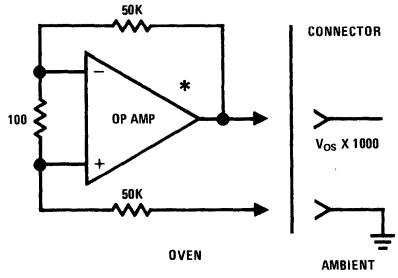
Resistor choice as well as physical placement is important for minimizing thermocouple effects. Carbon, oxide film and some metal film resistors can cause large thermocouple errors. Wirewound resistors of evenohm or managanin are best since they only generate about 2 µV/°C referenced to copper. Of course, keeping the resistor ends at the same temperature is important. Generally, shielding a low drift stage electrically and thermally will yield good results.

Resistors can cause other errors besides gradient generated voltages. If the gain setting resistors do not track with temperature a gain error will result. For example a gain of 1000 amplifier with a constant 10 mV input will have a 10V output. If the resistors mistrack by 0.5% over the operating temperature range, the error at the output is 50 mV Referred to input, this is a 50 µV error. Most precision resistors use different material for different ranges of resistor values. It is not unexpected that resistors differing by a factor of 1000, do not track perfectly with temperature. For best results insure that the gain fixing resistors are of the same material or have tracking temperature coefficients.

Testing low drift amplifiers is also difficult. Standard drift testing techniques such as heating the device in an oven and having the leads available through a connector, thermoprobe, or the soldering iron method — do not work. Thermal gradients cause much greater errors than the amplifier drift. Coupling microvolt signals through connectors is especially bad since the temperature difference across the connector

Achieving Low Drift (Continued)

can be 50°C or more. The device under test along with the gain setting resistor should be isothermal. The circuit in *Figure 3* will yield good results if well constructed.



*Op amp shown in *Figure 9.*

FIGURE 3. Drift Measurement Circuit

Performance

It is somewhat difficult to specify the performance of the LM121 since it is programmable over a wide range of operating currents. Changing the operating current varies gain, bias current, and offset current — three critical parameters in a high accuracy system. However, offset voltage and drift are virtually independent of the operating current.

Typical performance at an operating current of 20 µA is shown in *Table 1. Figures 4, 5* show how the bias current, offset current, and gain change as a function of programming current. Drift is guaranteed at 1 µV/°C independent of the operating current.

TABLE 1. Typical Performance at an Operating Current of 10 µA Per Side

Offset Voltage	Nulled
Bias Current	7 nA
Offset Current	0.5 nA
Offset Voltage Drift	0.3 µV/°C
Common Mode Rejection Ratio	125 dB
Supply Voltage Rejection Ratio	125 dB
Common Mode Range	±13V
Gain	20 V/V
Supply Current	0.5 mA

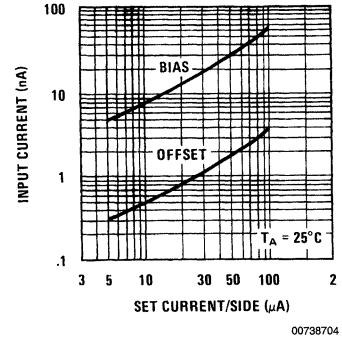


FIGURE 4. Bias and Offset Current vs Set Current

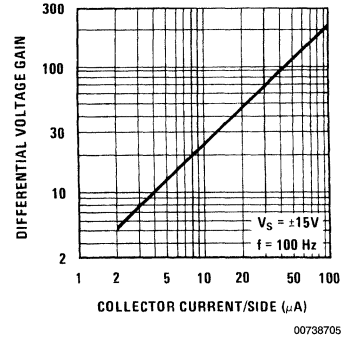


FIGURE 5. Gain vs Set Current

Over a temperature range of −55°C to +125°C the LM121 has less than 1 µV/°C offset voltage drift when nulled. It is important that the offset voltage is accurately nulled to achieve this low drift. The drift is directly related to the offset voltage with 3.8 µV/°C drift resulting from every millivolt of offset. For example, if the offset is nulled to 100 µV, about 0.4 µV/°C will result — or twice the typically expected drift. This drift is quite predictable and could even be used to cancel the drift elsewhere in a system. *Figure 6* shows drift as a function of offset voltage. For critical applications selected devices can achieve 0.2 µV/°C.

Figures 7, 8 show the bias current, offset current, and gain variation over a −55°C to +125°C temperature range. These

Performance (Continued)

performance characteristics do not tell the whole story. Since the LM121 is used with an operational amplifier, the op amp characteristics must be considered for overall amplifier performance.

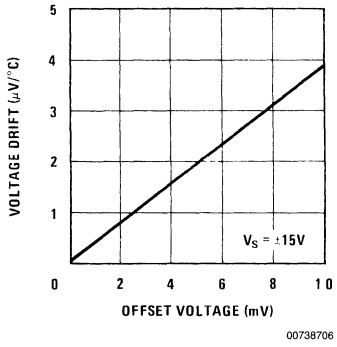


FIGURE 6. Drift vs Offset Voltage

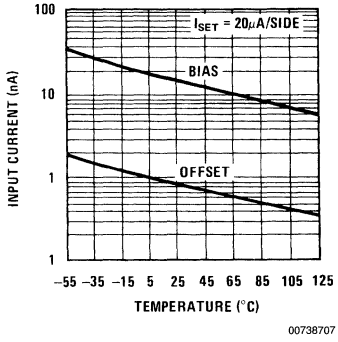


FIGURE 7. Bias and Offset Current vs Temperature

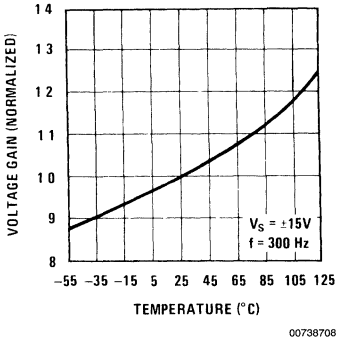


FIGURE 8. Gain vs Temperature for the LM121

Op Amp Effects

The LM121 is nominally used with a standard type of operational amplifier. The op amp functions as the second and ensuing stages of the amplifying system. When the LM121 is connected to an op amp, the two devices may be treated (and used) just as a single op amp. The inputs of the combination are the inputs of the LM121 and the output is from the op amp. Feedback, as with any op amp, is applied back to the inputs. *Figure 9* shows the general configuration of an amplifier using the LM121.

The offset voltage and drift of the op amp used have an effect on overall performance and must be considered. (The bias and offset currents of today's op amp are low enough to be ignored.) Although the exact effects of the op amp stage are difficult and tedious to calculate, a few approximations will show the sources of drift.

Op amp drift is perhaps the most important source of error. Drift of the op amp is directly reduced by the gain of the LM121. The drift referred to the input is given by:

$$\text{input drift} = \frac{\text{op amp drift}}{\text{LM121 gain}} + \text{LM121 drift.}$$

If the op amp has a drift of 10 μV/°C and the LM121 is operated at a gain of A_V = 50, there will be a 0.2 μV/°C component of the total drift due to the op amp. It is therefore important that the LM121 be operated at relatively high gain to minimize the effects of op amp drift. Lower gains for the LM121 will give proportionately less reduction in op amp drift. Of course, a moderately low drift op amp such as the LM108A eases the problem.

Op amp offset voltage also has an effect on total drift. For purpose of analysis assume the LM121 to be perfect with no offset or drift of its own. Then any offset seen when the LM121 is connected to an op amp is due to the op amp alone. The offset is equal to:

$$\text{offset voltage} = \frac{\text{op amp offset}}{\text{LM121 gain}}$$

or the offset is reduced by the gain of the LM121. For example, with a gain of 50 for the LM121, 2 mV of offset on the op amp appears as 40 μV of offset at the LM121 input. Unlike offset due to a mismatch in the LM121, this 40 μV of offset does not cause any drift. However, when the system is nulled so the offset at the input of the LM121 is zero, 40 μV of imbalance has been inserted into the LM121. The imbalance caused by nulling the offset induced by the op amp will cause a drift of about 0.14 μV/°C. With the system nulled the drift due to op amp will cause a drift of about 0.15 μV/°C. With the system nulled the drift due to op amp offset can be expressed as:

$$\text{drift } (\mu\text{V/°C}) = \frac{\text{op amp offset (mV)}}{\text{LM121 gain}} (3.6\ \mu\text{V/°C}).$$

In actual operation, drift due to op amp offsets will usually be better than predicted. This is because offset voltage and drift are not independent. With the LM121 there is a strong, predictable, correlation between offset and drift. Also, there

Op Amp Effects (Continued)

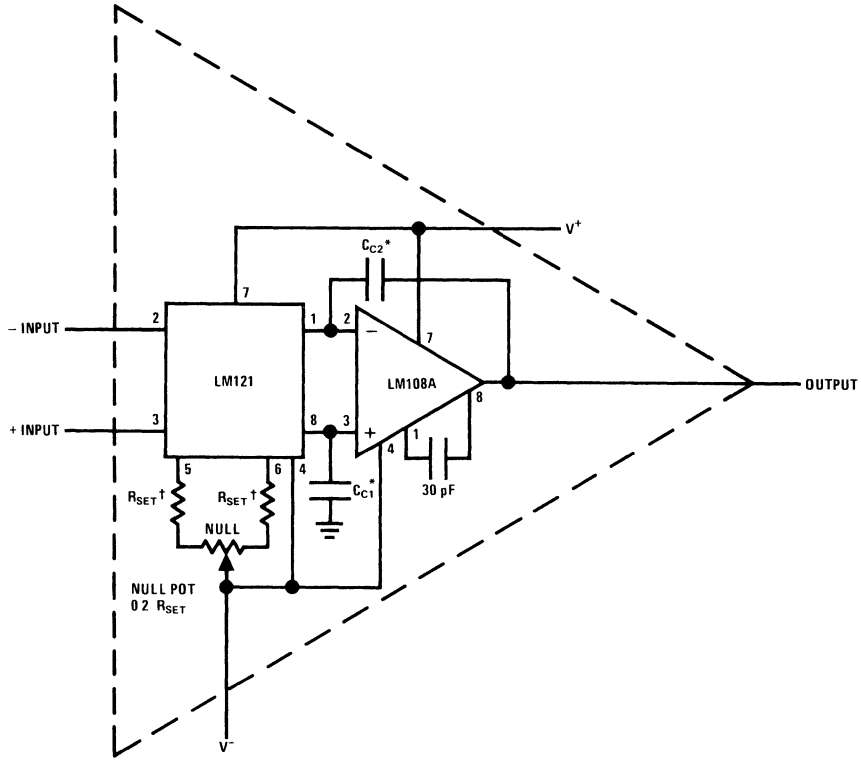
is a correlation with op amps, but it is not as strong. The drift of the op amp tends to cancel the drift induced in the LM121 when the system is nulled.

In the previous example the drift due to the op amp offset was 0.15 µV/°C. If the op amp has a drift of 3.6 µV/°C per millivolt of offset (like the LM121) it will have a drift of 7.2 µV/°C. This drift is reduced by the gain of the LM121 (A_V = 50) to 0.14 µV/°C. This 0.14 µV/°C will cancel the 0.14 µV/°C drift due to balancing the LM121. Since op amps do not always have a strong correlation between offset and drift, the cancellation of drifts is not total. Once again, high gain for the LM121 and a low offset op amp helps achieve low drifts.

Frequency Compensation

The additional gain of the LM121 preamplifier when used with an operational amplifier usually necessitates additional frequency compensation. This is because the additional gain introduced by the LM121 must be rolled-off before the phase shift through the LM121 and op amp reaches 180°. The additional compensation depends on the gain of the LM121 as well as the closed loop gain of the system. Two frequency compensation techniques are shown here that will operate with any op amp that is unity gain stable.

When the closed loop gain of the op amp with the LM121 is less than the gain of the LM121 alone, more compensation is needed. The worst case situation is when there is 100% feedback — such as a voltage follower or integrator — and the gain of the LM121 is high. When high closed loop gains are used — for example A_V = 1000 — and only an additional gain of 100 is inserted by the LM121, the frequency compensation of the op amp will usually suffice.



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*Frequency compensation — see text for values

$$\dagger I_{SET}\,(\mu A) \approx \frac{600}{R_{SET}\,(k\Omega)}$$

FIGURE 9. General Purpose Amplifier Using the LM121

The basic circuit of the LM121 in *Figure 9* shows two compensation capacitors connected to the op amp (disregarding the 30 pF frequency compensation for the op amp alone). The capacitor from pin 6 to pin 2 around the op amp acts as

Frequency Compensation (Continued)

an integrating capacitor to roll off the gain. Since the output of the LM121 is differential, a second capacitor is needed to roll off pin 3 of the op amp These capacitors are C_{C1} and C_{C2} in *Figure 9*.

With capacitors equal, the circuit retains good AC power supply rejection The approximate value of the compensation capacitors is given by:

$$C_C = \frac{8}{10^6 A_{CL} R_{SET}} \text{ farads}$$

where R_{SET} is the current set resistor from each current source and where A_{CL} is closed loop gain. *Table 2* shows typical capacitor values.

An alternate compensation scheme was developed for applications requiring more predictable and smoother roll off. This is useful where the amplifier's gain is changed over a wide range. In this case C_{C1} is made large and connected to V^+ rather than ground. The output of the LM121 is rendered single ended by a 0 01 µF bypass capacitor to V^+ Overall frequency compensation then is achieved by an integrating capacitor around the op amp·

$$\text{Bandwidth at unity gain} \cong \frac{12}{2\pi R_{SET} C}$$

$$\text{for 0 5 MHz bandwidth } C = \frac{4}{10^6 R_{SET}}$$

TABLE 2. Typical compensation capacitors for various operating currents and closed loop gains. Values given apply to LM101A, LM108, and LM741 type amplifiers.

Closed Loop Gain	Current Set Resistor				
	120 kΩ	60 kΩ	30 kΩ	12 kΩ	6 kΩ
A_V = 1	68 pF	130 pF	270 pF	680 pF	1300 pF
A_V = 5	15 pF	27 pF	50 pF	130 pF	270 pF
A_V = 10	10 pF	15 pF	27 pF	68 pF	130 pF
A_V = 50	1 pF	3 pF	5 pF	15 pF	27 pF
A_V = 100		1 pF	3 pF	5 pF	10 pF
A_V = 500			1 pF	1 pF	3 pF
A_V = 1000					

For use with higher frequency op amps such as the LM118 the bandwidth may be increased to about 2 MHz. If closed loop gain is greater than unity "C" may be decreased to:

$$C = \frac{4}{10^6 A_{CL} R_{SET}}$$

Applications

No attempt will be made to include precision op amp applications as they are well covered in other literature. The previous sections detail frequency compensation and drift problems encountered in using very low drift op amps. The circuit shown in *Figure 9* will yield good results in almost any op amp application. However, it is important to choose the operating current properly. From the curves given it is relatively easy to see the effects of current changes. High currents increase gain and reduce op amp effects on drift. Bias and offset current also increase at high current When the operating source resistance is relatively high, errors due to high bias and offset current can swamp offset voltage drift errors. Therefore, with high source impedances it may be advantageous to operate at lower currents

Another important consideration is output common mode voltage This is the voltage between the outputs of the LM121 and the positive power supply. Firstly, the output common mode voltage must be within the operating common mode range of the output op amp. At currents above 10 µA there is no problems with the LM108, LM101, and LM741 type devices. Higher currents are needed for devices with more limited common mode range, such as the LM118 As the operating current is increased, the positive common mode limit for the LM121 is decreased. This is because there is more voltage drop across the internal 50k load resistors The output common mode voltage and positive common mode limits are about equal and given by:

$$\begin{matrix}\text{Output common} \\ \text{mode voltage positive} \\ \text{common mode limit}\end{matrix} \approx V^+ - \left(0.6V + \frac{0.65 \times 50\ k\Omega}{R_{SET}}\right)$$

If it is necessary to increase the common mode output voltage (or limit), external resistors can be connected in parallel with the internal 50 kΩ resistors. This should only be done at high operating currents (80 µA) since it reduces gain and diverts part of the input stage current from the internal biasing circuitry. A reasonable value for external resistors is 50 kΩ.

The external resistors should be of high quality and low drift, such as wirewound resistors, since they will affect drift if they do not track well with temperature. A 20 ppm/°C difference in external resistor temperature coefficient will introduce an additional 0.3 µV/°C drift.

An unusually simple gain of 1000 instrumentation amplifier can be made using the LM121. The amplifier has a floating, full differential, high impedance input. Linearity is better than 1%, depending upon input signal level with maximum error at maximum input Gain stability, as shown in *Figure 10*, is about ±2% over a −55°C to +125°C temperature range. Finally, the amplifier has very low drift and high CMRR.

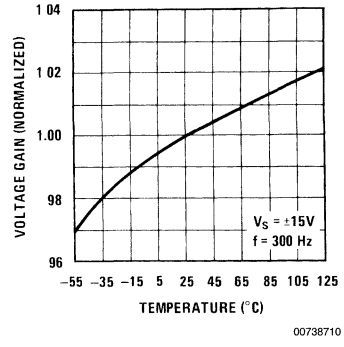
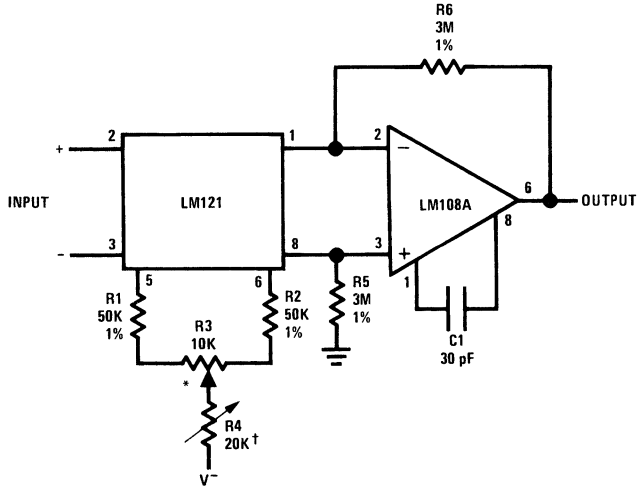


FIGURE 10. Instrumentation Amplifier Gain vs Temperature

Applications (Continued)

Figure 11 shows a schematic of the instrumentation amplifier. The LM121 is used as the input stage and operated open-loop. It converts an input voltage to a differential output current at pins 1 and 8 to drive an op amp. The op amp acts as a current to voltage converter and has a single-ended output.

Resistors R_1 and R_2 with null pot R_3 set the operating current of the LM121 and provide offset adjustment. R_4 is a fine trim to set the gain at 1000. There is very little interaction between the gain and null pots.



*Offset adjust

†Gain trim

‡Better than 1% linearity for input signals up to ±10 mV gain stability typical ±2% from −55°C to +125°C CMRR 110 dB

FIGURE 11. Gain of 1000 Instrumentation Amplifier

This instrumentation amplifier is limited to a maximum input signal of ±10 mV for good linearity. At high signal levels the transfer characteristic of the LM121 becomes rapidly non-linear, as with any differential amplifier. Therefore, it is most useful as a high gain amplifier.

Since feedback is not applied around the LM121, CMRR is not dependent on resistor matching. This eliminates the need for precisely matched resistor as with conventional instrumentation amplifiers. Although the linearity and gain stability are not as good as conventional schemes, this amplifier will find wide application where low drift and high CMRR are necessary.

A precision reference using a standard cell is shown in *Figure 12*. The low drift and low input current of the LM121A allow the reference amplifier to buffer the standard cell with high accuracy. Typical long term drift for the LM121 operating at constant temperature is less than 2 µV per 1000 hours.

To minimize temperature gradient errors, this circuit should be shielded from air currents. Good single-point wiring should also be used. When power is not applied, it is necessary to disconnect the standard cell from the input of the LM121 or it will discharge through the internal protection diodes.

Conclusions

A new preamplifier for operational amplifiers has been described. It can achieve voltage drifts as low as many chopper amplifiers without the problems associated with chopping. Operating current is programmable over a wide range so the input characteristics can be optimized for the particular application. Further, using a preamp and a conventional op amp allows more flexibility than a single low-drift op amp.

Conclusions (Continued)

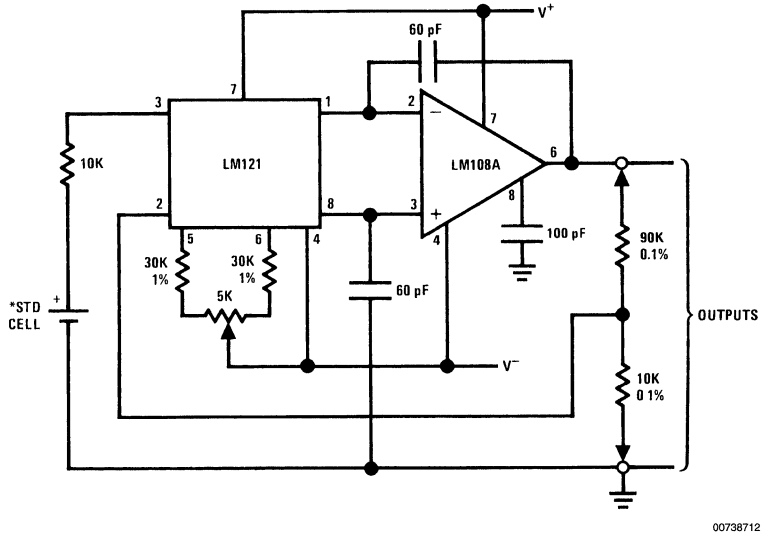


FIGURE 12. 10V Reference

Comparing the High Speed Comparators

National Semiconductor
Application Note 87

Introduction

Several integrated circuit voltage comparators exist which were designed with high speed and complementary TTL outputs as the main objectives. The more common applications for these devices are high speed analog to digital (A to D) converters, tape and disk-file read channels, fast zero-crossing detectors, and high speed differential line receivers. This note compares the National Semiconductor devices to similar devices from other manufacturers.

The product philosophy at National was to create pin-for-pin replacement circuits that could be considered as second-sources to the other comparators, while simultaneously containing the improvements necessary to make a more optimum device for the intended usage. Optimized parameters include speed, input accuracy and impedance, supply voltage range, fanout, and reliability. The LM160/LM260/LM360 are replacement devices for the µA760, while the LM161/LM261/LM361 replace the SE/NE529. *Tables 1, 2* compare the critical parameters of the National commercial range devices to their respective counterparts.

Speed

Throughout the universe the subject of speed must be approached with caution; the same holds true here. Speed (propagation delay time) is a function of the measurement technique. The earlier "standard" of using a 100 mV input step with 5.0 mV overdrive has given way to seemingly endless variations. To be meaningful, speed comparisons must be made with identical conditions. It is for this reason that the speed conditions specified for the National parts are the same as those of the parts replaced.

TABLE 1. LM360/µA760C Comparison

$0^\circ C \leq T_A \leq +70^\circ C$, $V^+ = +5.0V$, $V^- = -5.0V$

Parameter	LM360	µA760C	Units
Input Offset Voltage	5.0	6.0	mV max
Input Offset Current	3.0	7.5	µA max
Input Bias Current	20	60	µA max
Input Capacitance	4.0	8.0	pF typ
Input Impedance	17	5.0	kΩ typ @ 1 MHz 25°C
Differential Voltage Range	±5.0	±5.0	V typ
Common Mode Voltage Range	±4.0	±4.0	V typ
Gain	3.0	3.0	V/mV typ 25°
Fanout	4.0	2.0	74 Series TTL Loads
Propagation Delays:			
(1) 30 mVp-p 10 MHz Sinewave in	25	30	ns max 25°
(2) 2.0 Vp-p 10 MHz Sinewave in	20	25	ns max 25°
(3) 100 mV Step + 5.0 mV Overdrive	14	22	ns typ 25°

TABLE 2. LM261/NE529 Comparison

$0^\circ C \leq T_A \leq +70^\circ C$, $V^+ = +10V$, $V^- = -10V$, $V_{CC} = +5.0V$

Parameter	LM261	NE529	Units
Input Offset Voltage	3.0	10	mV max
Input Offset Current	3.0	15	µA max
Input Bias Current	20	50	µA max
Input Impedance	17	5.0	kΩ typ @ 1 MHz 25°C
Differential Voltage Range	±5.0	±5.0	V typ
Common Mode Voltage Range	±6.0	±6.0	V typ
Gain	3.0	4.0	V/mV typ 25°
Fanout	4.0	6.0	74 Series TTL Loads
Propagation Delay - 50 mV Overdrive	20	22	ns max 25°

Probably the most impressive speed characteristic of the six National parts is the fact that propagation delay is essentially independent of input overdrive (*Figure 1*); a highly desirable characteristic in A to D applications. Their delay typically varies only 3 ns for overdrive variations of 5.0 mV to 500 mV, whereas the other parts have a corresponding delay variation of two to one. As can be seen in *Tables 1, 2*, the National parts have an improved maximum delay specification. Further, the 20 ns maximum delay is meaningful since it is specified with a representative load: a 2.0 kΩ resistor to

Speed (Continued)

+5.0V and 15 pF total load capacitance. *Figure 2* shows typical delay variation with temperature.

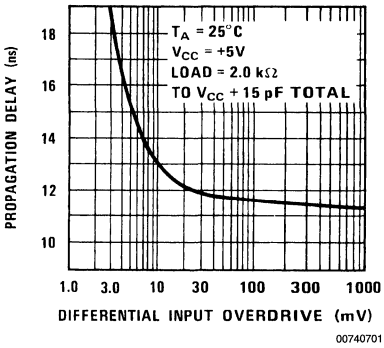


FIGURE 1. Delay vs Overdrive

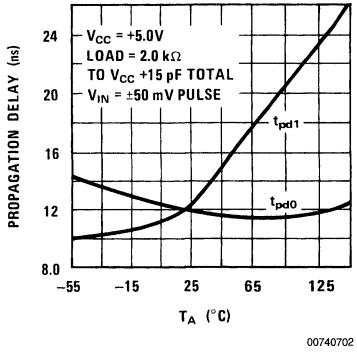


FIGURE 2. Delay vs Temperature

Input Parameters

The A to D, level detector, and line receiver applications of these devices require good input accuracy and impedance. In all these cases the differential input voltage is relatively large, resulting in a complete switch of input bias current as the input signal traverses the reference voltage level. This effect can give rise to reduced gain and threshold inaccuracy, dependent on input source impedances and comparator input bias currents. *Tables 1, 2* show that the National parts have a substantially lower maximum bias current to ease this problem. This was done without resorting to Darlington input stages whose price is higher offset voltages and longer delay times. The lower bias currents also raise input resistance in the threshold region. Lower input capacitance and higher input resistance result in higher input impedance at high frequencies.

Even with low source impedances, input accuracy is still dependent on offset voltage. Since none of the devices under discussion has internal offset null capability, ultimate accuracy was improved by designing and specifying lower maximum offset voltage. Refer to *Figure 3* for typical offset voltage drift with temperature.

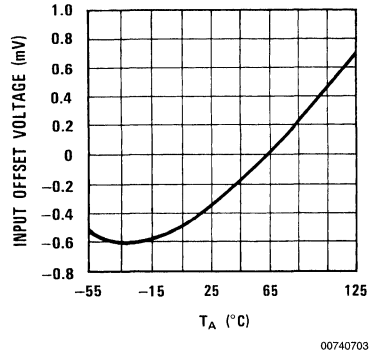


FIGURE 3. Offset Temperature Coefficient

Other Performance Areas

In the case of the LM160/LM260/LM360, fanout was doubled over the previous device. For the LM161/LM261/LM361, operating supply voltage range was extended to ±15V op amp supplies which are often readily available where such a comparator is used. *Figure 4* reveals the common mode range of the latter device.

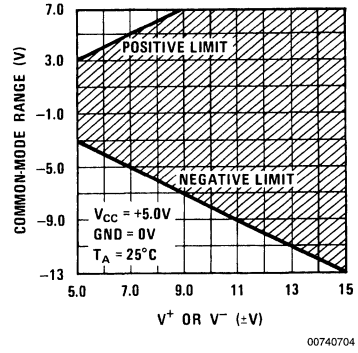


FIGURE 4. LM161 Common Mode Range

The performance improvements previously mentioned were a result of circuit design (*Figures 5, 6*) and device processing. Schottky clamping, which can give rise to reliability problems, was not used. Gold doping, which results in processing dependent speeds and low transistor beta, was not used. Instead a non-gold-doped process with high breakdown voltage, high beta, and high f_T (≈1.5 GHz) was selected which produced remarkably consistent performance independent of normal process variation. The higher breakdown voltage allows the LM161/LM261/LM361 to operate on ±15V supplies and results in lower transistor capacitance; higher beta provides lower input bias currents; and higher f_T helps reduce propagation time.

Other Performance Areas (Continued)

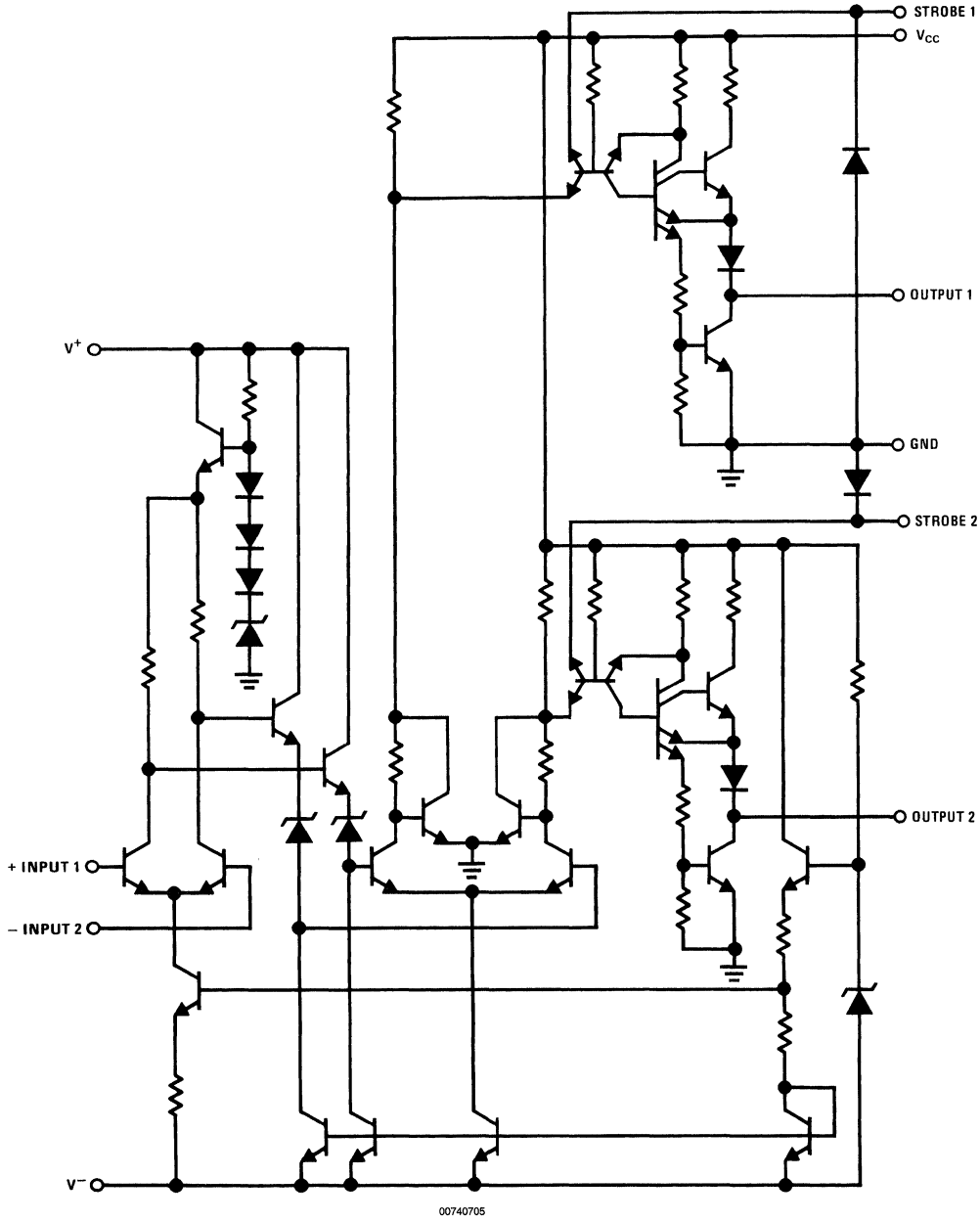


FIGURE 5. LM161 Schematic Diagram

Other Performance Areas (Continued)

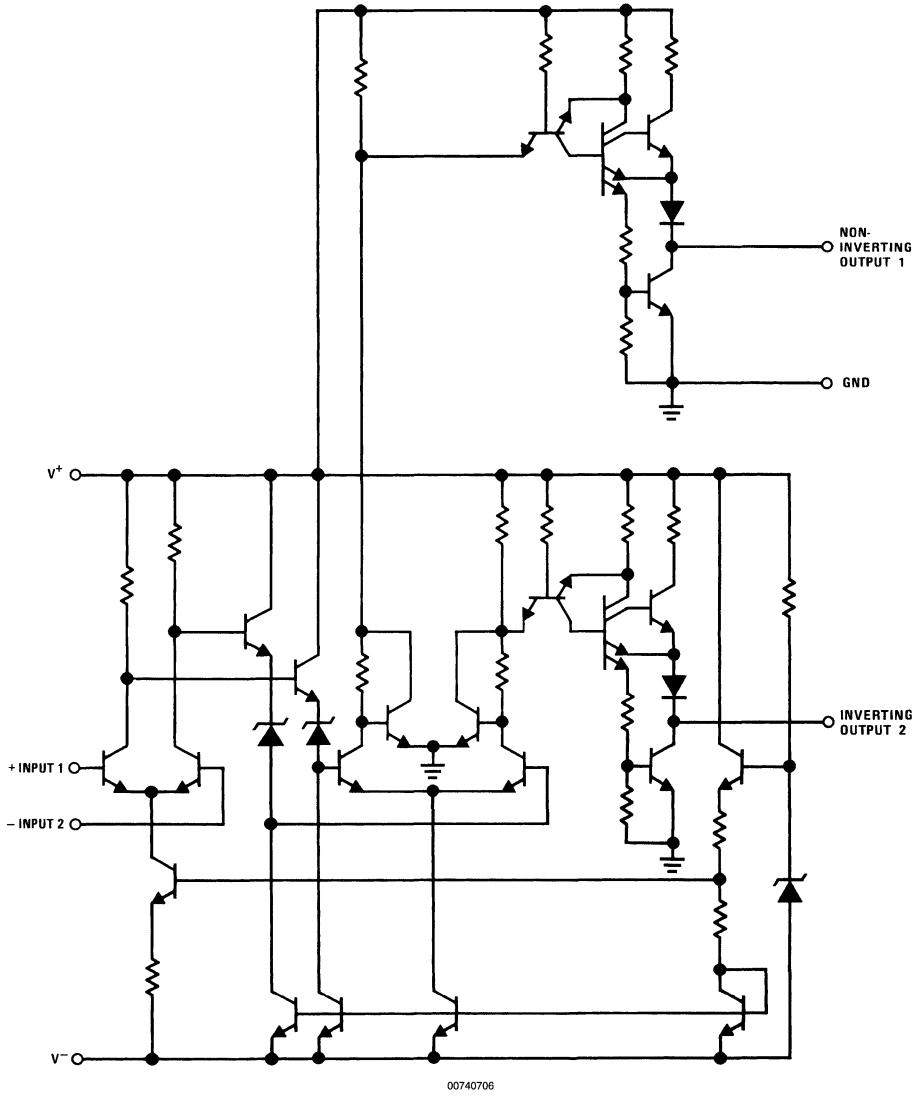


FIGURE 6. LM160 Schematic Diagram

Applications

Typical applications have been mentioned previously. The LM160 and LM161 may be combined as in *Figure 7* to create a fast, accurate peak detector for use in tape and disk-file read channels. A 3-bit A to D converter with 21 ns typical conversion time is shown in *Figure 8*. Although primarily intended for interfacing to TTL logic, direct connection may be made to ECL logic from the LM161 by the technique shown in *Figure 9*. When used this way the common mode range is shifted from that of the TTL configuration. Finally level detectors or line receivers may be implemented with hysteresis in the transfer characteristic as seen in *Figure 10*.

Applications (Continued)

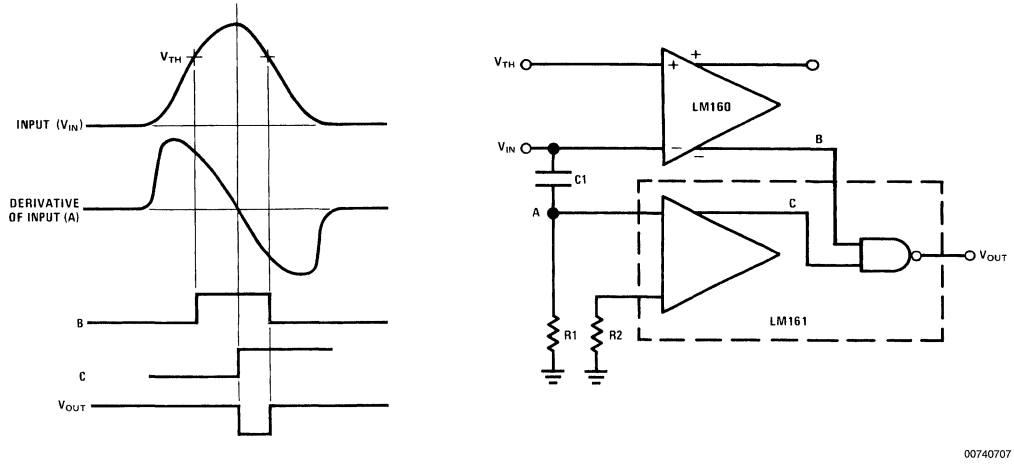


FIGURE 7. Peak Detector

Applications (Continued)

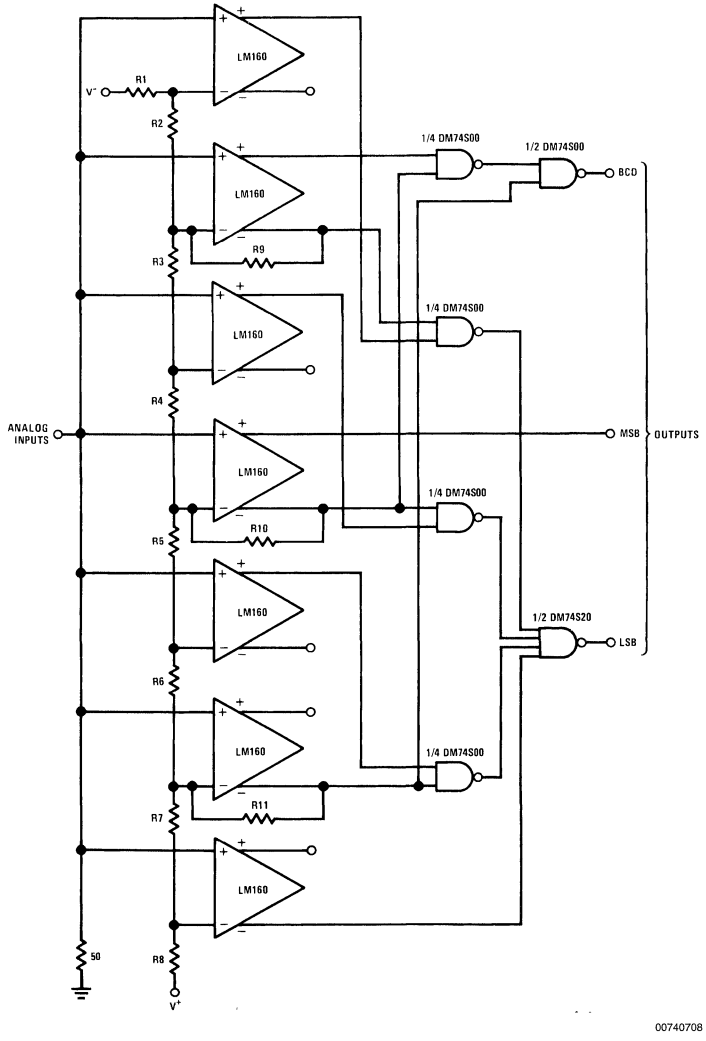


FIGURE 8. High Speed 3-bit A to D Converter

Applications (Continued)

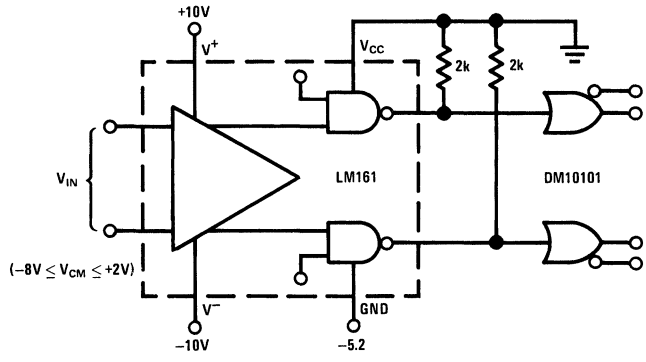
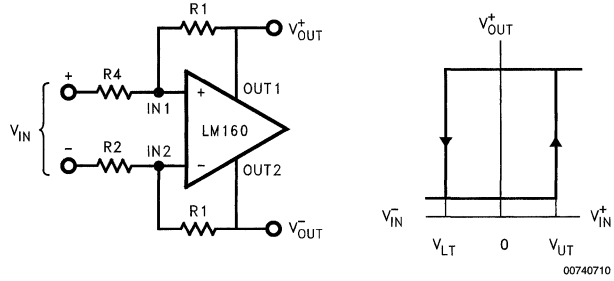


FIGURE 9. Direct Interfacing to ECL



$$V_{UT} = V_{OH}\left(\frac{R2}{R1}\right) - V_{OL}\left(\frac{R4}{R3}\right)$$

$$V_{LT} = V_{OL}\left(\frac{R2}{R1}\right) - V_{OH}\left(\frac{R4}{R3}\right)$$

FIGURE 10. Level Detector with Hysteresis

Use the LM158/LM258/LM358 Dual, Single Supply Op Amp

National Semiconductor
Application Note 116

Introduction

Use the LM158/LM258/LM358 dual op amp with a single supply in place of the LM1458/LM1558 with split supply and reap the profits in terms of:

a. Input and output voltage range down to the negative (ground) rail
b. Single supply operation
c. Lower standby power dissipation
d. Higher output voltage swing
e. Lower input offset current
f. Generally similar performance otherwise

The main advantage, of course, is that you can eliminate the negative supply in many applications and still retain equivalent op amp performance. Additionally, and in some cases more importantly, the input and output levels are permitted to swing down to ground (negative rail) potential. *Table 1* shows the relative performance of the two in terms of guaranteed and/or typical specifications.

In many applications the LM158/LM258/LM358 can also be used directly in place of LM1558 for split supply operation.

Single Supply Operation

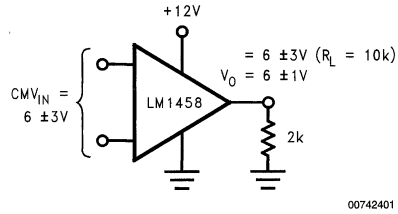
The LM1458/LM1558 or similar op amps exhibit several important limitations when operated from a single positive (or negative) supply. Chief among these is that input and output signal swing is severely limited for a given supply as shown in *Figure 1*. For linear operation, the input voltage must not reach within 3 volts of ground or of the supply, and output range is similarly limited to within 3–5 volts of ground or supply. This means that operation with a +12V supply could be limited as low as 2 Vp-p output swing. The LM358 however, allows a 10.5 Vp-p output swing for the same 12V supply. Admittedly these are worst case specification limits, but they serve to illustrate the problem.

TABLE 1. Comparison of Dual Op Amps LM1458 and LM358

Characteristic	LM1458	LM358
V_{IO}	6 mV Max	7 mV Max
CM V_I	24 Vp-p*	0–28.5V*
I_{IO}	200 nA	50 nA
I_{OB}	500 nA	−500 nA
CMRR	60 dB Min @ 100 Hz 90 dB Typ	85 dB Typ @ DC
$\bar{e}_n$ @ 1 kHz, R_{GEN} 10 kΩ	45 nV/$\sqrt{Hz}$ Typ	40 nV/$\sqrt{Hz}$ Typ**
Z_{IN}	200 MΩ Typ	Typ 100 MΩ
A_{VOL}	20k Min 100k Typ	100k Typ
f_c	1.1 MHz Typ	1 MHz Typ **
P_{BW}	14 kHz Typ	11 kHz Typ **
dV_o/dt	0.8V/μs Typ	0.5V/μs Typ**
V_o @ R_L = 10k/2k	24/20 Vp-p*	28.5 Vp-p
I_{SC}	20 mA Typ	Source 20 mA Min (40 Typ) Sink 10 mA Min (20 Typ)
PSRR @ DC	37 dB Min 90 dB Typ	100 dB Typ
I_D (R_L = ∞)	8 mA Max	2 mA Max

‡From laboratory measurement
*Based on V_S = 30V on LM358 only, or V_S = ±15V
**From data sheet typical curves

Single Supply Operation (Continued)



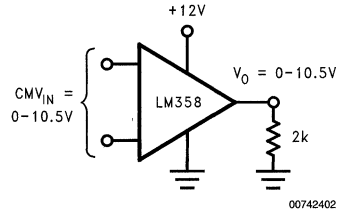
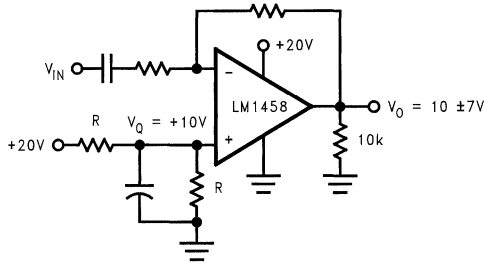


FIGURE 1. Worst Case Signal Levels with +12V Supply



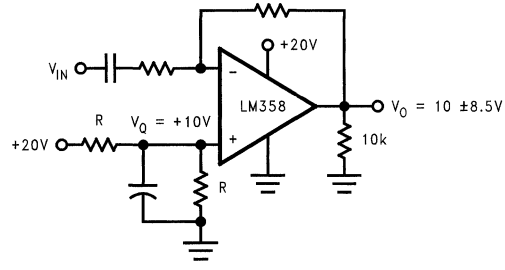


FIGURE 2. Operating with AC Signals

AC Gain

For AC signals the input can be capacitor coupled. The input common mode and quiescent output voltages are fixed at one-half the supply voltage by a resistive divider at the non-inverting input as shown in *Figure 2*. This quiescent output could be set at a lower voltage to minimize power dissipation in the LM358, if desired, so long as $V_Q \geq V_{IN}$ pk. For the LM1458 the quiescent output must be higher, VQ ≥ 3V + V_{IN} pk thus, for small signals, power dissipation is much greater with the LM1458. Example: Required $V_O = V_Q \pm 1V$ pk into 2k, V_{SUPPLY} = as required. Find quiescent dissipation in load and amplifier for LM1458 and LM358.

LM358

$V_Q = +1V$

$V_{SUPPLY} = +3.5V$

$$P_{LOAD} = \frac{E_L^2}{R_L} = \frac{1}{2k} = 0.5\,mW$$

$$P_D = V_S I_S{}^* + (V_S - V_Q) I_L$$

$$= 3.5V \times 0.7\,mA + (3.5 - 1)\frac{1V}{2k}$$

$P_D = 2.45 + 1.25 = 3.7\,mW$

$P_{TOTAL} = 3.7 + 0.5 = 4.2\,mW$

*From typical characteristics

LM1458

$V_Q = 4V$

$V_{SUPPLY} = 8V$

$$P_{LOAD} = \frac{4^2}{2k} = 8\,mW$$

$$P_D = P_D{}^* + (V_S - V_Q) I_L$$

$$= 22\,mW + (8 - 4)\frac{4V}{2k}$$

$P_D = 22 + 8 = 30\,mW$

$P_{TOTAL} = 30 + 8 = 38\,mW$

*From typical characteristics

The LM1458 requires over twice the supply voltage and nearly 10 times the supply power of the LM358 in this application.

Inverting DC Gain

Connections and biasing for DC inverting gain are essentially the same as for the AC coupled case. Note, of course, that the output cannot swing negative when operated from a single positive supply. *Figure 3* shows the connections and signal limitations.

Non-Inverting DC Gain

The non-inverting gain connection does not require the V_Q biasing as before; the inverting input can be returned to ground in the usual manner for gains greater than unity, (see *Figure 4*). A tremendous advantage of the LM358 in this connection is that input signals and output may extend all the way to ground; therefore DC signals in the low-millivolt range can be handled. The LM1458 still requires that V_{IN} = 3V–17V. Therefore maximum gain is limited to $A_V = (V_O–3)/3$, or A_V max = 5.4 for a 20V supply.

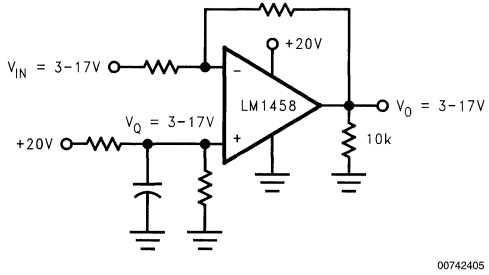
There is no similar limitation for the LM358.

Zero T.C. Input Bias Current

An interesting and unusual characteristic is that I_{IN} has a zero temperature coefficient. This means that matched resistance is not required at the input, allowing omission of one resistor per op amp from the circuit in most cases.

Balanced Supply Operation

The LM358 will operate satisfactorily in balanced supply operation so long as a load is maintained from output to the negative supply.



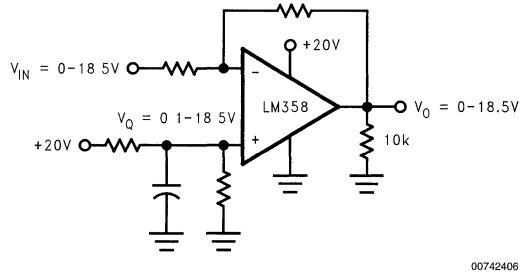
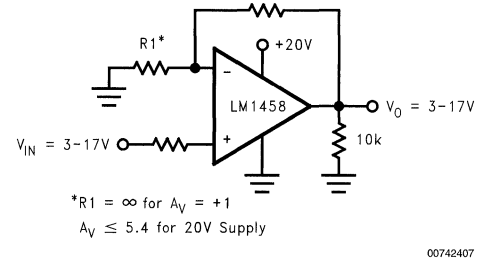


FIGURE 3. Typical DC Coupled Inverting Gain



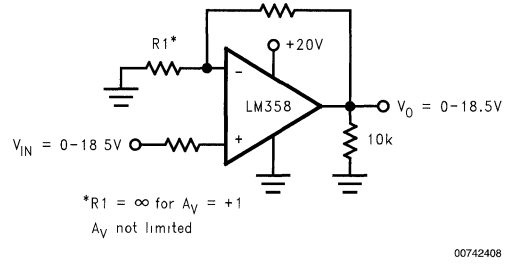


FIGURE 4. Typical DC Coupled Non-Inverting Gain

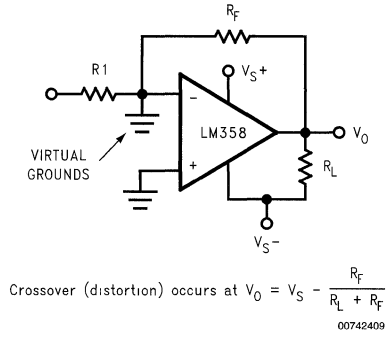


FIGURE 5. Split Supply Operation of LM358

The output load to negative supply forces the amplifier to source some minimum current at all times, thus eliminating crossover distortion. Crossover distortion without this load would be more severe than that expected with the normal op amp. Since the single supply design took notice of this normal load connection to ground, a class AB output stage

Balanced Supply Operation

(Continued)

was not included. Where ground referenced feedback resistors are used as in *Figure 5*, the required load to the negative supply depends upon the peak negative output signal level desired without exhibiting crossover distortion. R_L to the negative rail should be chosen small enough that the voltage divider formed by R_F and R_L will permit V_o to swing negative to the desired point according to the equation:

$$R_L = R_F \frac{V_S - V_o}{V_o}$$

R_L could also be returned to the positive supply with the advantage that V_o max would never exceed (V_{S^+} – 1.5V). Then with ±15V supplies $R_{L\ MIN}$ would be 0.12 R_F. The disadvantage would be that the LM358 can source twice as much current as it can sink, therefore R_L to negative supply can be one-half the value of R_L to positive supply.

The need for single or split supply is based on system requirements which may be other than op amp oriented. However if the only need for balanced supplies is to simplify the biasing of op amps, there are many systems which can find a cost effective benefit in operating LM358's from single supplies rather than standard op amps from balanced supplies. Of the usual op amp circuits, *Table 2* shows those few which have limited function with single supply operation. Most are based on the premise that to operate from a single supply, a reference V_Q at about one-half the supply be available for bias or (zero) signal reference. The basic circuits are those listed in AN-20.

TABLE 2. Conventional Op Amp Circuits Suitable for Single Supply Operation

Application	Limitations
AC Coupled amp‡	V_Q*
Inverting amp	V_Q
Non-inverting amp	OK*
Unity gain buffer	OK
Summing amp	V_Q
Difference amp	V_Q
Differentiator	V_Q
Integrator	V_Q
LP Filter	V_Q
I–V Connector	V_Q
PE Cell Amp	OK
I Source	$I_{O\ MIN} = \frac{1.5}{R1}$
I Sink	OK
Volt Ref	OK
FW Rectifier	V_Q or modified circuit
Sine wave osc	V_Q
Triangular generator	V_Q
Threshold detector	OK
Tracking, regulator PS	Not practical
Programmable PS	OK
Peak Detector	OK to V_{IN} = 0

‡See AN-20 for conventional circuits

*V_Q denotes need for a reference voltage, usually at about $\frac{V_S}{2}$

OK means no reference voltage required

IC Voltage Reference has 1 ppm per Degree Drift

National Semiconductor
Application Note 161

A new linear IC now provides the ultimate in highly stable voltage references Now, a new monolithic IC the LM199, out-performs zeners and can provide a 6.9V reference with a temperature drift of less than 1 ppm/° and excellent long term stability. This new IC, uses a unique subsurface zener to achieve low noise and a highly stable breakdown. Included is an on-chip temperature stabilizer which holds the chip temperature at 90°C, eliminating the effects of ambient temperature changes on reference voltage.

The planar monolithic IC offers superior performance compared to conventional reference diodes. For example, active circuitry buffers the reverse current to the zener giving a dynamic impedance of 0.5Ω and allows the LM199 to operate over a 0.5 mA to 10 mA current range with no change in performance. The low dynamic impedance, coupled with low operating current significantly simplifies the current drive circuitry needed for operation. Since the temperature coefficient is independent of operating current, usually a resistor is all that is needed.

Previously, the task of providing a stable, low temperature coefficient reference voltage was left to a discrete zener diode. However, these diodes often presented significant problems. For example, ordinary zeners can show many millivolts change if there is a temperature gradient across the package due to the zener and temperature compensation diode not being at the same temperature. A 1°C difference may cause a 2 mV shift in reference voltage. Because the on-chip temperature stabilizer maintains constant die temperature, the IC reference is free of voltage shifts due to temperature gradients. Further, the temperature stabilizer, as well as eliminating drift, allows exceptionally fast warm-up over conventional diodes. Also, the LM199 is insensitive to stress on the leads—another source of error with ordinary glass diodes. Finally, the LM199 shows virtually no hysteresis in reference voltage when subject to temperature cycling over a wide temperature range. Temperature cycling the LM199 between 25°C, 150°C and back to 25°C causes less than 50 µV change in reference voltage. Standard reference diodes exhibit shifts of 1 mV to 5 mV under the same conditions.

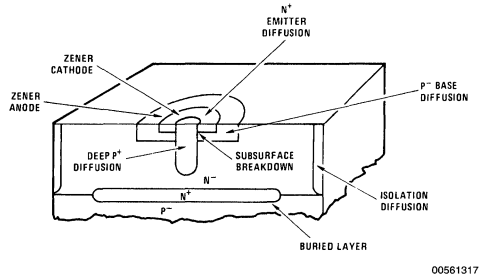


FIGURE 1. Subsurface Zener Construction

Sub Surface Zener Improves Stability

Previously, breakdown references made in monolithic IC's usually used the emitter-base junction of an NPN transistor as a zener diode. Unfortunately, this junction breaks down at the surface of the silicon and is therefore susceptible to surface effects. The breakdown is noisy, and cannot give long-term stabilities much better than about 0.3%. Further, a surface zener is especially sensitive to contamination in the oxide or charge on the surface of the oxide which can cause short-term instability or turn-on drift.

The new zener moves the breakdown below the surface of the silicon into the bulk yielding a zener that is stable with time and exhibits very low noise. Because the new zener is made with well-controlled diffusions in a planar structure, it is extremely reproducible with an initial 2% tolerance on breakdown voltage.

A cut-away view of the new zener is shown in *Figure 1.* First a small deep P^+ diffusion is made into the surface of the silicon. This is then covered by the standard base diffusion. The N^+ emitter diffusion is then made completely covering the P^+ diffusion. The diode then breaks down where the dopant concentration is greatest, that is, between the P^+ and N^+. Since the P^+ is completely covered by N^+ the breakdown is below the surface and at about 6.3V. One connection to the diode is to the N^+ and the other is to the P base diffusion. The current flows laterally through the base to the P^+ or cathode of the zener. Surface breakdown does not occur since the base P to N^+ breakdown voltage is greater than the breakdown of the buried device. The buried zener has been in volume production since 1973 as the reference in the LX5600 temperature transducer.

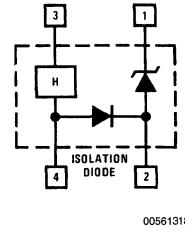


FIGURE 2. Functional Block Diagram

Circuit Description

The block diagram of the LM199 is shown in *Figure 2.* Two electrically independent circuits are included on the same chip—a temperature stabilizer and a floating active zener. The only electrical connection between the two circuits is the isolation diode inherent in any junction-isolated integrated circuit. The zener may be used with or without the tempera-

Circuit Description (Continued)

ture stabilizer powered. The only operating restriction is that the isolation diode must never become forward biased and the zener must not be biased above the 40V breakdown of the isolation diode.

The actual circuit is shown in *Figure 3*. The temperature stabilizer is composed of Q1 through Q9. FET Q9 provides current to zener D2 and Q8. Current through Q8 turns a loop consisting of D1, Q5, Q6, Q7, R1 and R2. About 5V is applied to the top of R1 from the base of Q7. This causes 400 µA to flow through the divider R1, R2. Transistor Q7 has a controlled gain of 0.3 giving Q7 a total emitter current of about 500 µA. This flows through the emitter of Q6 and drives another controlled gain PNP transistor Q5. The gain of Q5 is about 0.4 so D1 is driven with about 200 µA. Once current flows through Q5, Q8 is reverse biased and the loop is self-sustaining. This circuitry ensures start-up.

The resistor divider applies 400 mV to the base of Q4 while Q7 supplies 120 µA to its collector. At temperatures below the stabilization point, 400 mV is insufficient to cause Q4 to conduct. Thus, all the collector current from Q7 is provided as base drive to a Darlington composed of Q1 and Q2. The Darlington is connected across the supply and initially draws 140 mA (set by current limit transistor Q3). As the chip heats, the turn on voltage for Q4 decreases and Q4 starts to conduct. At about 90°C the current through Q4 appreciably increases and less drive is applied to Q1 and Q2. Power dissipation decreases to whatever is necessary to hold the chip at the stabilization temperature. In this manner, the chip temperature is regulated to better than 2°C for a 100°C temperature range.

The zener section is relatively straight-forward. A buried zener D3 breaks down biasing the base of transistor Q13. Transistor Q13 drives two buffers Q12 and Q11. External current changes through the circuit are fully absorbed by the buffer transistors rather than D3. Current through D3 is held constant at 250 µA by a 2k resistor across the emitter base of Q13 while the emitter-base voltage of Q13 nominally temperature compensates the reference voltage.

The other components, Q14, Q15 and Q16 set the operating current of Q13. Frequency compensation is accomplished with two junction capacitors.

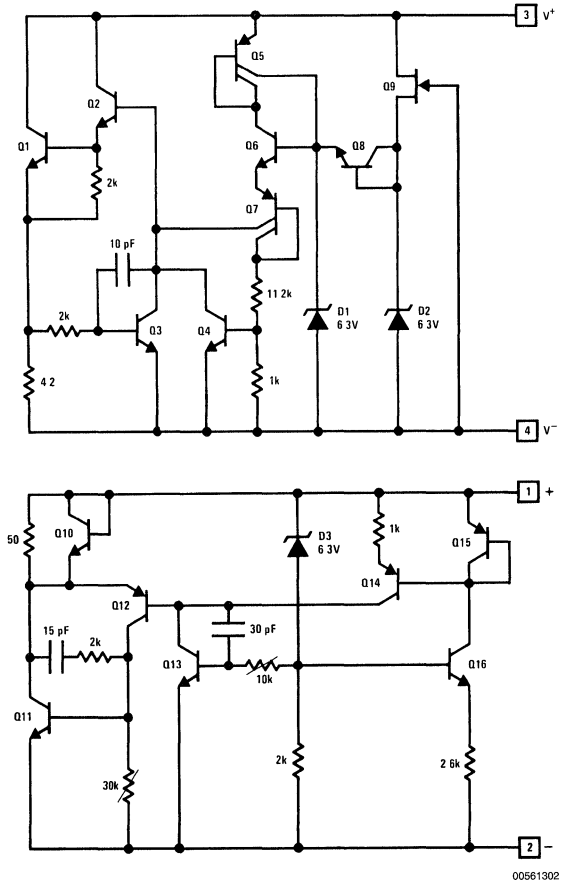


FIGURE 3. Schematic Diagram of LM199 Precision Reference

Performance

A polysulfone thermal shield, shown in *Figure 4*, is supplied with the LM199 to minimize power dissipation and improve temperature regulation. Using a thermal shield as well as the small, high thermal resistance TO-46 package allows operation at low power levels without the problems of special IC packages with built-in thermal isolation. Since the LM199 is made on a standard IC assembly line with standard assembly techniques, cost is significantly lower than if special techniques were used. For temperature stabilization only 300 mW are required at 25°C and 660 mW at −55°C.

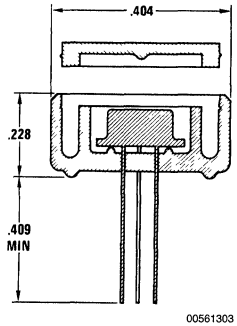


FIGURE 4. Polysulfone Thermal Shield

Temperature stabilizing the device at 90°C virtually eliminates temperature drift at ambient temperatures less than 90°C. The reference is nominally temperature compensated and the thermal regulator further decreases the temperature drift. Drift is typically only 0.3 ppm/°C. Stabilizing the temperature at 90°C rather than 125°C significantly reduces power dissipation but still provides very low drift over a major portion of the operating temperature range. Above 90°C ambient, the temperature coefficient is only 15 ppm/°C.

A low drift reference would be virtually useless without equivalent performance in long term stability and low noise. The subsurface breakdown technology yields both of these. Wideband and low frequency noise are both exceptionally low. Wideband noise is shown in *Figure 5* and low frequency noise is shown over a 10 minute period in the photograph of *Figure 6*. Peak to peak noise over a 0.01 Hz to 1 Hz bandwidth is only about 0.7 μV.

Long term stability is perhaps one of the most difficult measurements to make. However, conditions for long-term stability measurements on the LM199 are considerably more realistic than for commercially available certified zeners. Standard zeners are measured in ±0.05°C temperature controlled both at an operating current of 7.5 mA ±0.05 μA. Further, the standard devices must have stress-free contacts on the leads and the test must not be interrupted during the measurement interval. In contrast, the LM199 is measured in still air of 25°C to 28°C at a reverse current of 1 mA ±0.5%. This is more typical of actual operating conditions in instruments.

When a group of 10 devices were monitored for long-term stability, the variations all correlated, which indicates changes in the measurement system (limitation of 20 ppm) rather than the LM199.

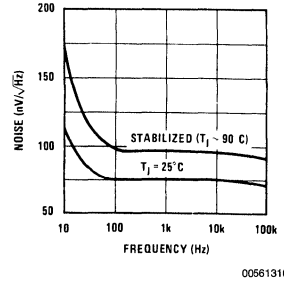


FIGURE 5. Wideband Noise of the LM199 Reference

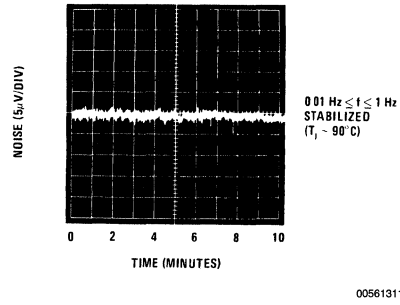


FIGURE 6. Low Frequency Noise Voltage

Because the planar structure does not exhibit hysteresis with temperature cycling, long-term stability is not impaired if the device is switched on and off.

The temperature stabilizer heats the small thermal mass of the LM199 to 90°C very quickly. Warm-up time at 25°C and −55°C is shown in *Figure 7*. This fast warm-up is significantly less than the several minutes needed by ordinary diodes to reach equilibrium. Typical specifications are shown in *Table 1*.

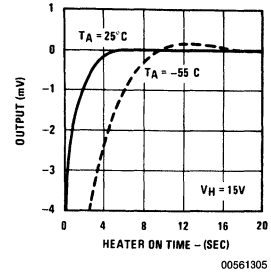


FIGURE 7. Fast Warmup Time of the LM199

Performance (Continued)

TABLE 1. Typical Specifications for the LM199

Reverse Breakdown Voltage	6.95V
Operating Current	0.5 mA to 10 mA
Temperature Coefficient	0.3 ppm/°C
Dynamic Impedance	0.5Ω
RMS Noise (10 Hz to 10 kHz)	7μV
Long-Term Stability	≤20 ppm
Temperature Stabilizer Operating Voltage	9V to 40V
Temperature Stabilizer Power Dissipation (25°C)	300 mW
Warm-up Time	3 Seconds

Applications

The LM199 is easier to use than standard zeners, but the temperature stability is so good—even better than precision resistors—that care must be taken to prevent external circuitry from limiting performance. Basic operation only requires energizing the temperature stabilizer from a 9V to 40V power source and biasing the reference with between 0.5 mA to 10 mA of current. The low dynamic impedance minimizes the current regulation required compared to ordinary zeners.

The only restriction on biasing the zener is the bias applied to the isolation diode. Firstly, the isolation diode must not be forward biased. This restricts the voltage at either terminal of the zener to a voltage equal to or greater than the V^-.

A dc return is needed between the zener and heater to insure the voltage limitation on the isolation diodes are not exceeded. *Figure 9* shows the basic biasing of the LM199.

The active circuitry in the reference section of the LM199 reduces the dynamic impedance of the zener to about 0.5Ω. This is especially useful in biasing the reference. For example, a standard reference diode such as a 1N829 operates at 7.5 mA and has a dynamic impedance of 15Ω. A 1% change in current (75 μA) changes the reference voltage by 1.1 mV. Operating the LM199 at 1 mA with the same 1% change in operating current (10 μA) results in a reference change of only 5 μV. *Figure 8* shows reverse voltage change with current.

Biasing current for the reference can be anywhere from 0.5 mA to 10 mA with little change in performance. This wide current range allows direct replacement of most zener types with no other circuit changes besides the temperature stabilizer connection. Since the dynamic impedance is constant with current changes regulation is better than discrete zeners. For optimum regulation, lower operating currents are preferred since the ratio of source resistance to zener impedance is higher, and the attenuation of input changes is greater. Further, at low currents, the voltage drop in the wiring is minimized.

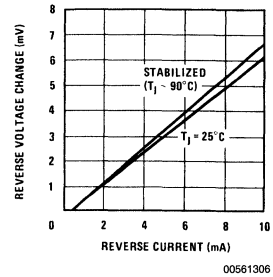


FIGURE 8. The LM199 Shows Excellent Regulation Against Current Changes

Mounting is an important consideration for optimum performance. Although the thermal shield minimizes the heat low, the LM199 should not be exposed to a direct air flow such as from a cooling fan. This can cause as much as a 100% increase in power dissipation degrading the thermal regulation and increasing the drift. Normal conviction currents do not degrade performance.

Applications (Continued)

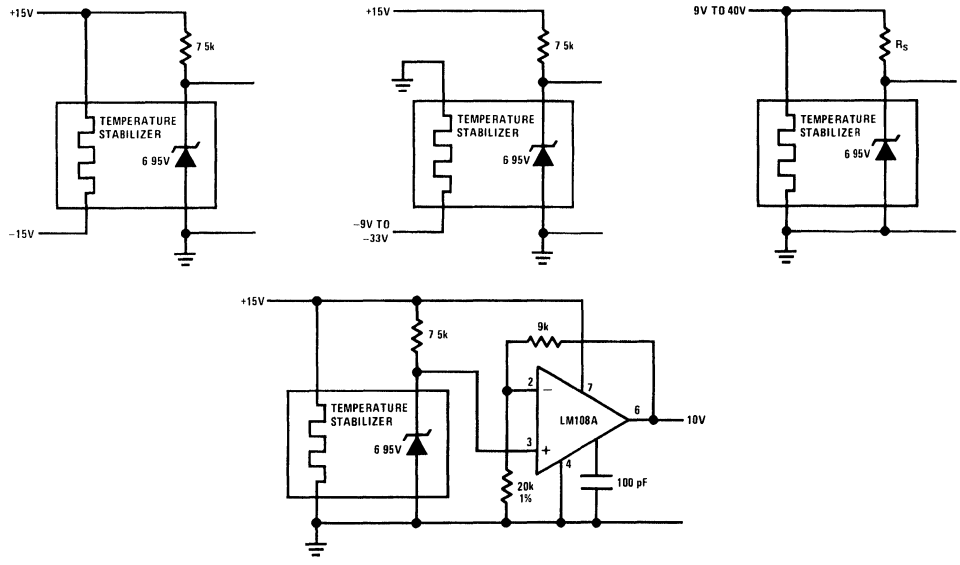


FIGURE 9. Basic Biasing of the LM199

Printed circuit board layout is also important. Firstly, four wire sensing should be used to eliminate ohmic drops in pc traces. Although the voltage drops are small the temperature coefficient of the voltage developed along a copper trace can add significantly to the drift. For example, a trace with 1Ω resistance and 2 mA current flow will develop 2 mV drop. The TC of copper is 0.004%/°C so the 2 mV drop will change at 8 µV/°C, an additional 1 ppm drift error. Of course, the effects of voltage drops in the printed circuit traces are eliminated with 4-wire operation. The heater current also should not be allowed to flow through the voltage reference traces. Over a −55°C to +125°C temperature range the heater current will change from about 1 mA to over 40 mA. These magnitudes of current flowing reference leads or reference ground can cause huge errors compared to the drift of the LM199.

Thermocouple effects can also use errors. The kovar leads from the LM199 package from a thermocouple with copper printed circuit board traces. Since the package of the 199 is heated, there is a heat flow along the leads of the LM199 package. If the leads terminate into unequal sizes of copper on the p.c. board greater heat will be absorbed by the larger copper trace and a temperature difference will develop. A temperature *difference* of 1°C between the two leads of the reference will generate about 30 µA. Therefore, the copper traces to the zener should be equal in size. This will generally keep the errors due to thermocouple effects under about 15 µV.

The LM199 should be mounted flush on the p.c. board with a minimum of space between the thermal shield and the boards. This minimizes air flow across the kovar leads on the board surface which also can cause thermocouple voltages. Air currents across the leads usually appear as ultra-low frequency noise of about 10 µV to 20 µV amplitude.

It is usually necessary to scale and buffer the output of any reference to some calibrated voltage. *Figure 10* shows a simple buffered reference with a 10V output. The reference is applied to the non-inverting input of the LM108A. An RC rolloff can be inserted in series with the input to the LM108A to roll-off the high frequency noise. The zener heater and op amp are all powered from a single 15V supply. About 1% regulation on the input supply is adequate contributing less than 10 µV of error to the output. Feedback resistors around the LM308 scale the output to 10V.

Although the absolute values of the resistors are not extremely important, tracking of temperature coefficients is vital. The 1 ppm/°C drift of the LM199 is easily exceeded by the temperature coefficient of most resistors. Tracking to better than 1 ppm is also not easy to obtain. Wirewound types made of Evenohm or Mangamin are good and also have low thermoelectric effects. Film types such as Vishay resistors are also good. Most potentiometers do not track fixed resistors so it is a good idea to minimize the adjustment range and therefore minimize their effects on the output TC. Overall temperature coefficient of the circuit shown in *Figure 10* is worst case 3 ppm/°C. About 1 ppm is due to the reference, 1 ppm due to the resistors and 1 ppm due to the op amp.

Figure 11 shows a standard cell replacement with a 1.01V output. LM321 and LM308 are used to minimize op amp drift to less than 1 µV/°C. Note the adjustment connection which minimizes the TC effects of the pot. Set-up for this circuit requires nulling the offset of the op amp first and then adjusting for proper output voltage.

Applications (Continued)

The drift of the LM321 is very predictable and can be used to eliminate overall drift of the system. The drift changes at 3.6 µV/°C per millivolt of offset so 1 mV to 2 mV of offset can be introduced to minimize the overall TC.

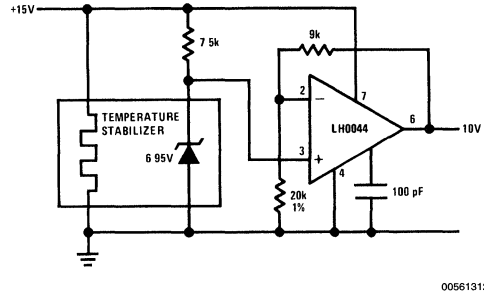


FIGURE 10. Buffered 10V Reference

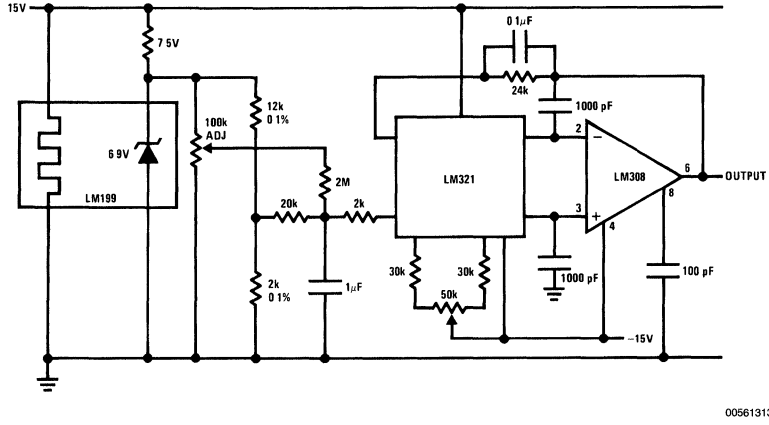


FIGURE 11. Standard Cell Replacement

For circuits with a wide input voltage range, the reference can be powered from the output of the buffer as is shown in *Figure 12*. The op amp supplies regulated voltage to the resistor biasing the reference minimizing changes due to input variation. There is some change due to variation of the temperature stabilizer voltage so extremely wide range operation is not recommended for highest precision. An additional resistor (shown 80 kΩ) is added to the unregulated input to insure the circuit starts up properly at the application of power.

A precision power supply is shown in *Figure 13*. The output of the op amp is buffered by an IC power transistor the LM395. The LM395 operates as an NPN power device but requires only 5 µA base current. Full overload protection inherent in the LM395 includes current limit, safe-area protection, and thermal limit.

A reference which can supply either a positive or a negative continuously variable output is shown in *Figure 14*. The reference is biased from the ±15 input supplies as was shown earlier. A ten-turn pot will adjust the output from $+V_Z$ to $-V_Z$ continuously. For negative output the op amp operates as an inverter while for positive outputs it operates as a non-inverting connection.

Op amp choice is important for this circuit. A low drift device such as the LM108A or a LM108-LM121 combination will provide excellent performance. The pot should be a precision wire wound 10 turn type. It should be noted that the output of this circuit is not linear.

Conclusions

A new monolithic reference which exceeds the performance of conventional zeners has been developed. In fact, the LM199 performance is limited more by external components than by reference drift itself. Further, many of the problems associated with conventional zeners such as hysteresis, stress sensitivity and temperature gradient sensitivity have also been eliminated. Finally, long-term stability and noise are equal of the drift performance of the new device.

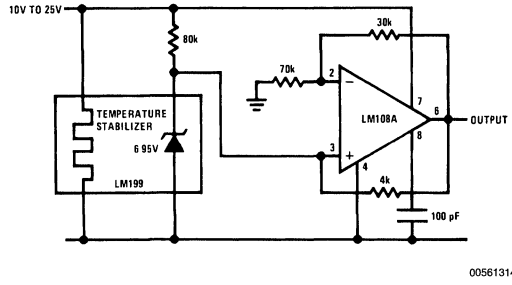


FIGURE 12. Wide Range Input Voltage Reference

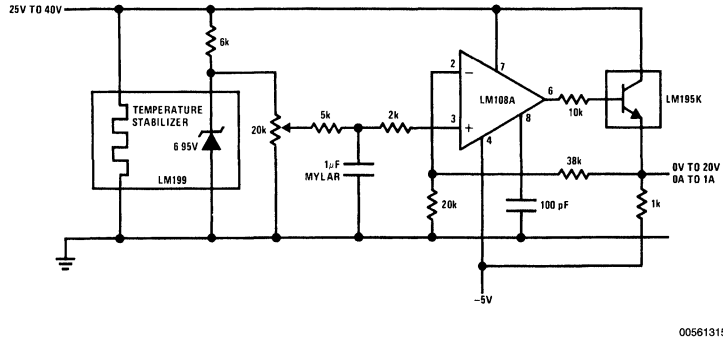


FIGURE 13. Precision Power Supply

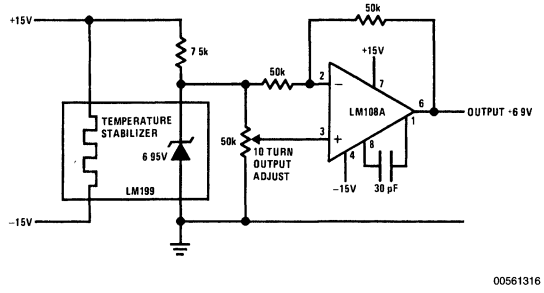


FIGURE 14. Bipolar Output Reference

IC Zener Eases Reference Design

National Semiconductor
Application Note 173

Description

A new IC zener with low dynamic impedance and wide operating current range significantly simplifies reference or regulator circuit design. The low dynamic impedance provides better regulation against operating current changes, easing the requirements of the biasing supply. Further, the temperature coefficient is independent of operating current, so that the LM129 can be used at any convenient current level. Other characteristics such as temperature coefficient, noise and long term stability are equal to or better than good quality discrete zeners.

The LM129 uses a new subsurface breakdown IC zener combined with a buffer circuit to lower dynamic impedance. The new subsurface zener has low noise and excellent long term stability since the breakdown is in the bulk of the silicon. Circuitry around the zener supplies internal biasing currents and buffers external current changes from the zener. The overall breakdown is about 6.9V with devices selected for temperature coefficients.

The zener is relatively straightforward. A buried zener D1 breaks down biasing the base of transistor Q1. Transistor Q1 drives two buffers Q2 and Q3. External current changes through the circuit are fully absorbed by the buffer transistors rather than by D1. Current through D1 is held constant at 250 µA by a 2k resistor across the emitter base of Q1 while the emitter-base voltage of Q1 nominally temperature compensates the reference voltage.

The other components, Q4, Q5 and Q6, set the operating current of Q1. Frequency compensation is accomplished with two junction capacitors.

All that is needed for biasing in most applications is a resistor as shown in *Figure 2*. Biasing current can be anywhere from 0.6 mA to 15 mA with little change in performance. Optimally, however, the biasing current should be as low as possible for the best regulation. The dynamic impedance of the LM129 is about 1 Ω and is independent of current. Therefore, the regulation of the LM129 against voltage changes is 1/Rs.

Lower currents or higher Rs give better regulation. For example, with a 15V supply and 1 mA operating current, the reference change for a 10% change in the 15V supply is 180 µV. If the LM129 is run at 5 mA, the change is 900 µV or 5 times worse. By comparison, a standard IN821 zener will change about 17 mV. All discrete zeners have about the same regulation since their dynamic impedance is inversely proportional to operating current.

If the zener does not have to be grounded, a bridge compensating circuit can be used to get virtually perfect regulation, as shown in *Figure 3*. A small compensating voltage is generated across R1, which matches the dynamic impedance of the LM129. Since the dynamic impedance of the LM129 is linear with current, this circuit will work even with large changes in the unregulated input voltage.

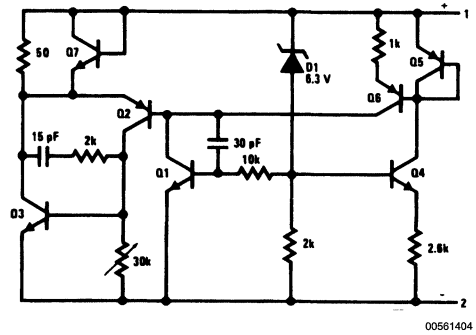


FIGURE 1. IC Reference Zener

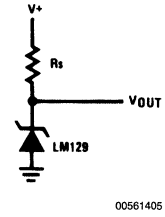


FIGURE 2. Basic Biasing

Other output voltages are easily obtained with the simple op-amp circuit shown in *Figure 4*. A simple non-inverting amplifier is used to boost and buffer the zener to 10V. The reference is run directly from the input power rather than the output of the op-amp. When the zener is powered from the op-amp, special starting circuitry is sometimes necessary to insure the output comes up in the right polarity. For outputs lower than the breakdown of the LM129 a divider can be connected across the zener to drive the op-amp.

An AC square wave or bipolarity output reference can easily be made with an op-amp and FET switch as shown in *Figure 5*. When Q1 is "ON", the LM108 functions as a normal inverting op-amp with a gain of −1 and an output of −6.9V. With Q1 "OFF" the op-amp acts as a giving 6.9V at the output. Some non-symmetry will occur from loading change on the LM129 in the different states and mismatch of R1 and R2. Trimming either R1 or R2 can make the output exactly symmetrical around ground.

Description (Continued)

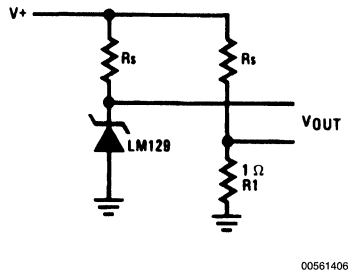


FIGURE 3. Bridge Compensation for Line Changes

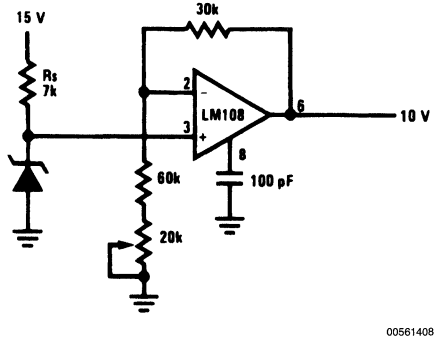


FIGURE 4. 10 Volt Buffered Output Reference

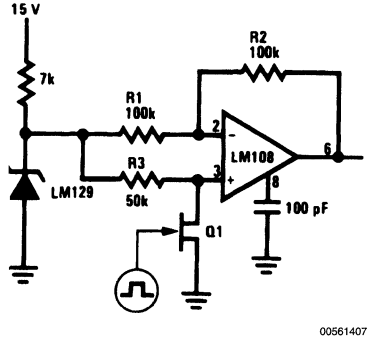


FIGURE 5. Bipolar Output Reference

Description (Continued)

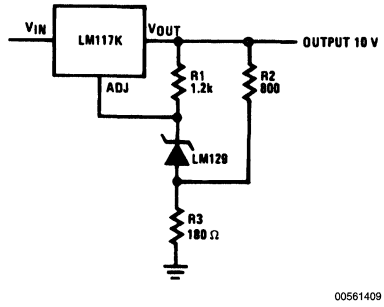


FIGURE 6. High Stability 10V Regulator

By combining the LM129 with an LM117 three-terminal regulator a high stability power regulator can be made. This is shown in *Figure 6*. Resistor R1 biases the LM129 at about 1 mA from the 1.25V reference in the LM117. The voltage of the LM129 is added to the 1.25V of the LM117 to make a total reference voltage of 8.1V. The output voltage is then set at 10V by R2 and R3. Since the internal reference of the LM117 contributes only about 20% of the total reference voltage, regulation and drift are essentially those of the external zener. The regulator has 0.2% load and line regulation and if a low drift zener such as the LM129A is used overall temperature coefficient is less than 0.002%/°C.

The new zener can be used as the reference for conventional IC voltage regulators for enhanced performance. Noise is lower, time stability is better, and temperature coefficient can be better depending on the device selected. Further, the output voltage is independent of power changes in the regulator.

Figure 7 shows an LM723 using an external LM129 reference. The internal 7V reference is not used and a single resistor biases the LM129 as the reference. The 5k resistor chosen provides sufficient operating current for the zener over the 10V to 40V input voltage range of the LM723. Since the dynamic impedance of the LM129 is so low, the reference regulation against line changes is only 0.02%/V. This is small compared to the regulation of 0.1%/V for the LM723; however, the resistor can be replaced by a 1 mA to 5 mA FET used as a constant current source for improved regulation. When the FET is used reference regulation is easily 0.001%/V. Output voltage is set in the standard manner except that for low output voltages sufficient current must be run through the zener to power the voltage divider supplying the reference to the LM723.

An overload protected power shunt regulator is shown in *Figure 8*. The output voltage is about 7.8V – the 7V breakdown of the LM129 plus the 0.8V emitter-base voltage of the LM395. The LM395 is an IC, 1.5 A power transistor with complete overload protection on the chip. Included on the chip are current limiting and thermal limiting, making the device virtually blowout-proof. Further, the base current is only 5 µA, making it easy to drive as a shunt regulator. As the input voltage rises, more drive is applied to the base of the LM395, turning it on harder and dropping more voltage across the series resistance. Should the input voltage rise too high, the LM395 will current limit or thermal limit, protecting itself.

The new IC zener can replace existing zeners in just about any application with improved performance and simpler external circuitry. As with any zener reference, devices are selected for temperature coefficient and operating temperature range. Since the devices are made by a standard integrated circuit process, cost is low and good reproducibility is obtained in volume production.

Finally, since the device is actually an IC, it is packaged in a rugged TO-46 metal can package or a 3-lead plastic transistor package.

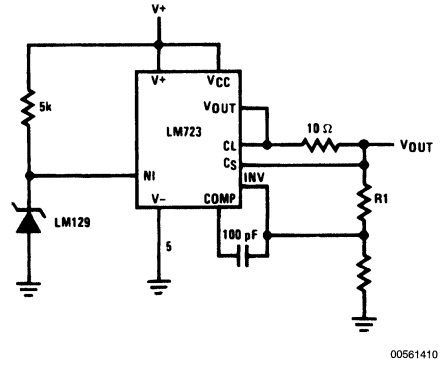


FIGURE 7. External Reference For IC

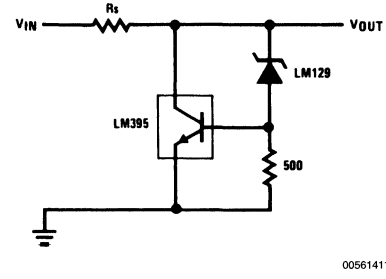


FIGURE 8. Power Shunt Regulator

Super Matched Bipolar Transistor Pair Sets New Standards for Drift and Noise

National Semiconductor
Application Note 222

Matched bipolar transistor pairs are a very powerful design tool, yet have received less and less attention over the last few years. This is primarily due to the proliferation of high-performance monolithic circuits which are replacing many designs previously implemented with discrete components. State-of-the-art circuitry, however, is still the realm of the discrete component, especially because of recent improvements in the components themselves.

It has become clear in the past few years that ultimate performance in monolithic transistor pairs was being limited by statistical fluctuations in the material itself and in the processing environment. This led to a matched transistor pair fabricated from many different individual transistors physically located in a manner which tended to average out any residual process or material gradients. At the same time, the large number of parallel devices would reduce random fluctuations by the square root of the number of devices.

The LM194 is the end result. It is a monolithic bipolar matched transistor pair which offers an order-of-magnitude improvement in matching properties and parasitic base and emitter resistance over conventional transistor pairs. This was accomplished without compromising breakdown voltage or current gain. The LM194 is specified at 40V minimum collector-to-emitter breakdown voltage and has a minimum h_{FE} of 500 at 1 mA collector current. Maximum offset voltage is 50 µV over a collector current range of 1 µA to 1 mA. Maximum h_{FE} mismatch is 2%. Common mode rejection of offset voltage (dV_{OS}/dV_{CB}) is 124 dB minimum. An added benefit of paralleling many transistors is the resultant drop in overall r_{bb} and r_{ee}, which are 40Ω and 0.4Ω respectively. This makes the logarithmic conformity of emitter-base voltage to collector current excellent even at higher current levels where other devices become non-theoretical. In addition, broadband noise is extremely low, especially at higher operating currents.

The key to the success of the LM194 is the nearly one-to-one correlation between measured parameters and those predicted by a theoretical bipolar transistor model. The relationship between emitter-base voltage and collector current, for instance, is perfectly logarithmic over an extremely wide range of collector currents, deviating in the pA range because of leakage currents and above several milliamperes due to the finite 0.4Ω emitter resistance. This gives the LM194 a distinct advantage in non-linear designs where true logarithmic behavior is essential to circuit accuracy. Of equal importance is the absolute nature of the logarithmic constant, both between the two halves of the device and from unit to unit. The relationship can be expressed as:

$$V_{BE_1} - V_{BE_2} = \frac{kT}{q} \ln \left(\frac{I_{C_1}}{I_{C_2}} \right)$$

This relationship holds true both within a single transistor where I_{C1} and I_{C2} represent two different operating currents and between the two halves of the LM194 where collector currents are unbalanced. Of particular importance is the fact that the kT/q logarithmic constant is an absolute quantity dependent only on Boltzman's constant (k), absolute temperature (T), and the charge on the electron (q). Since these values are independent of processing, there is virtually no variation from unit to unit at a fixed temperature. Lab measurements indicate that the logarithmic constant measured at a 10:1 collector current ratio does not vary more than ±0.5% from its theoretical value. Applications such as logarithmic converters, multipliers, thermometers, voltage references, and voltage-controlled amplifiers can take advantage of this inherent accuracy to provide adjustment-free precision circuits.

Approaching Theoretical Noise

In many low-level amplifier applications, the limiting factor on performance is noise. With bipolar transistors, the theoretical value for emitter-base voltage noise is a function only of absolute temperature and collector current.

$$e_n = kT \sqrt{\frac{2}{qI_C}} \quad \text{Volts}/\sqrt{\text{Hz}}$$

This formula indicates that voltage noise can be reduced to low levels by simply raising collector current. In fact, that is exactly what happens until collector current reaches a level where parasitic transistor noise limits any further reduction. This "noise floor" is usually created by and modeled as an equivalent resistor (r_{bb}') in series with the base of the transistor. Low parasitic base resistance is therefore an important factor in ultra-low-noise applications where collector current is pushed to the limits. The 40Ω equivalent r_{bb}' of the LM194 is considerably lower than that of other small-signal transistors. In addition, this device has no excess noise at lower current levels and coincides almost exactly with the predicted values. A low-noise design can be done on paper with a minimum of bench testing.

Another noise component in bipolar transistors is base current noise. For any finite source impedance, current noise must be considered as a quadrature addition to voltage noise.

$$\begin{matrix}\text{total equivalent} \\ \text{input voltage noise}\end{matrix} = e_N = \sqrt{e_n^2 + (i_n \bullet r_s)^2} \text{Volts}/\sqrt{\text{Hz}}$$

where r_s is the source impedance

In the LM194, base current noise is a well-defined function of collector current and can be expressed as:

$$i_n = \sqrt{\frac{2q \bullet I_C}{h_{FE}}} \quad \text{Amps}/\sqrt{\text{Hz}}$$

Approaching Theoretical Noise

(Continued)

To find the collector current which yields the minimum overall equivalent input noise with a given source impedance, the total noise formula can be differentiated with respect to I_C and set equal to zero for finding a minimum.

$$e_N^2 = e_n^2 + (i_n^2 \bullet r_s^2) + 4\,kT \bullet r_s$$

$$(4\,kT \bullet r_s = \text{noise}^2 \text{ of } r_s)$$

$$= \frac{2k^2 \bullet T^2}{q \bullet I_C} + \frac{2q \bullet I_C \bullet r_s^2}{h_{FE}} + 4kT \bullet r_s$$

$$\frac{d(V_N^2)}{d(I_C)} = \frac{-2k^2 \bullet T^2}{q \bullet I_C^2} + \frac{2q \bullet r_s^2}{h_{FE}} = 0$$

$$I_C\,(\text{optimum}) = \frac{kT}{q} \bullet \frac{\sqrt{h_{FE}}}{r_s}$$

For very low source impedances, the 40Ω r_{bb}' of the LM194 should be added to r_s in this calculation. A plot of noise figure versus collector current (see curve) shows that the formula does indeed predict the optimum value. The curves are very shallow, however, and actual current can be varied by 3:1 without losing more than 1 dB noise figure in most cases. This may be a worthwhile tradeoff if low bias current ($I_C < I_{opt}$) or wide bandwidth ($I_C > I_{opt}$) is also important. *Figure 1* is a plot of best obtainable noise figure versus source impedance for the LM194 and a very low noise junction FET (PF5102). Collector current for the LM194 is optimized for each source impedance and is also plotted on the graph using the right side scale. The PF5102 is operated at a constant 1 mA. It is obvious that the bipolar device gives significantly better noise figures for low source impedances and/or low frequencies. FETs are particularly poor at very low frequencies (< 10 Hz) and offer advantages only for very high source impedances.

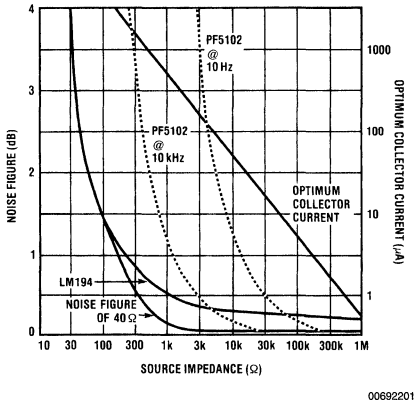


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FIGURE 1. Noise Figure vs Source Impedance

Reactive Sources

Calculations may also be done to derive an optimum collector current when the signal source is reactive. In this case, upper and lower frequencies (f_H and f_L) must be specified. Also, optimum current is different for an amplifier with a summing junction input ($Z_{IN} = 0$) as compared to a high impedance input ($Z_{IN} \gg X_C, X_L$). The formulas below give optimum collector current for noise within the frequency band f_L to f_H. For audio applications, lowest "perceived" noise may be somewhat different because of the variation in sensitivity of the ear to frequencies in the audio range (Fletcher-Munson effect).

Capacitive source into high impedance:

$$I_C\,(\text{opt}) = \frac{kT}{q} \bullet C \bullet 2\pi \bullet \sqrt{h_{FE}} \bullet \sqrt{f_H \bullet f_L}$$

Capacitive source into summing junction:

$$I_C\,(\text{opt}) = \frac{kT}{q} \times \frac{\sqrt{h_{FE}}}{R_f} \times \sqrt{\frac{4\pi^2 \bullet R_f^2 \bullet C^2 (f_L^2 + f_H^2 + f_L \bullet f_H)}{3} + \frac{4\pi \bullet R_f \bullet C \bullet (f_H + f_L)}{2} + 1}$$

Inductive source into high impedance:

$$I_C\,(\text{opt}) = \frac{\frac{kT}{q} \bullet \sqrt{h_{FE}}}{2\pi \bullet L} \sqrt{\frac{3}{f_L^2 + f_H^2 + f_L \bullet f_H}}$$

Keep in mind that the simple formula for total input-referred noise, though accurate in itself, does not take into account the effects of noise created in additional stages or noise injected from supply lines. In most cases voltage gain of the LM194 stage will be sufficient to swamp out second stage effects. For this to be true, first stage gain must be at least $3 \bullet v_{n2}/v_N$, where v_{n2} is the voltage noise of the second stage and v_N is the desired total input referred voltage noise. A simple formula for voltage gain of an LM194 stage, assuming no second stage loading, is given by:

$$A_V = \frac{(R_L)(I_C)}{kT/q} \text{ where } R_L \text{ is the load resistor}$$

Noise injected from power supplies is an often overlooked problem in low noise designs. This is probably in part due to the use of IC op amps with their high power supply rejection ratio and differential inputs. Many low-noise designs are single-ended and do not enjoy the inherent supply rejection of differential designs. For a single-ended amplifier with its load resistor tied directly to the power supply, noise on the supply must be no higher than $(R_L \bullet I_C \bullet v_N)/(3\ kT/q)$ or noise performance will be degraded. For a differential stage (see *Figure 2*) with the common emitter resistor tied to the negative supply and the collector resistors tied to the positive supply, supply noise is not generally a problem, at least at low frequencies. For this to be true at higher frequencies, the

Reactive Sources (Continued)

capacitance at the collector nodes must be kept low and balanced. In an unbalanced situation, noise from either supply will feed through unattenuated at higher frequencies where the reactance of the capacitor is much lower than the collector resistance.

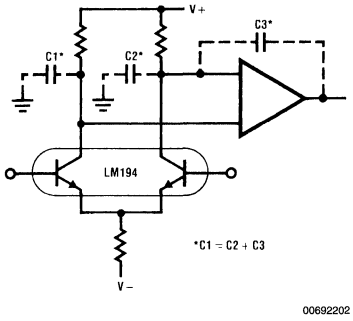


FIGURE 2. High Frequency Power Supply Rejection

Bandwidth Considerations

Because of its large area, the LM194 has capacitance-limited bandwidth. The $h_{fe} \bullet f$ product is roughly 0.08 MHz per microampere of collector current, yielding an f_t of 80 MHz at I_C = 1 mA and 800 kHz at I_C = 10 µA.

Collector-base capacitance on the LM194 is somewhat higher than ordinary small-signal transistors due to the large device geometry. C_{ob} is 17 pF at V_{CE} = 5V. For high gain stages with finite source impedance, the Millering effect of C_{ob} will usually be the limiting factor on voltage gain bandwidth. At I_C = 100 µA and R_L = 50 kΩ, for instance, DC voltage gain will be $(R_L)(I_C)/(kT/q)$ = 200, but bandwidth will be limited to

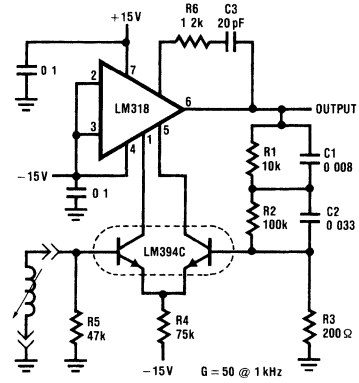
$$BW = \frac{kT/q}{(2\pi)(R_L)(I_C)(R_s)(C_{ob})} = 50 \text{ kHz}$$

for a source impedance (R_s) of 1 kΩ.

Low Noise Applications

Figure 3 and *Figure 4* represent two different approaches to low noise designs. In *Figure 3*, the LM194 is used to replace the input stage of an LM118 high speed operational amplifier to create an ultra-low-distortion, low-noise RIAA-equalized phono preamplifier. The internal input stage of the LM118 is shut off by tying the unused inputs to the negative supply. This allows the LM194 to be used in place of the internal input stage, avoiding the loop stability problems created when extra stages are added. The stability problem is especially critical in an RIAA circuit where 100% feedback is used at high frequencies. Performance of this circuit exceeds the ability of most test equipment to measure it. As shown in the accompanying chart, *Figure 3*, harmonic distortion is below the measurable 0.002% level over most of the operating frequency and amplitude range. Noise referred to a 10 mV input signal is 90 dB down, measuring 0.55 μV_{RMS} and 70 pA_{RMS} in a 20 kHz bandwidth. More importantly, the noise figure is less than 2 dB when the amplifier is used with standard phono cartridges, which have an equivalent wideband (20 kHz) noise of 0.7 µV[1]. Further improvements in amplifier noise characteristics would be of little use because of the noise generated by the cartridge itself.

A special test was performed to check for "Transient Intermodulation Distortion"[2]. 10 kHz and 11 kHz were mixed 1:1 at the input to give an RMS output voltage of 2V (input = 200 mV). The resulting 1 kHz intermodulation product measured at the output was 80 µV. This calculates to 0.004% distortion, an incredibly low level considering that the 1 kHz has 14 dB (5:1) gain with respect to the 10 kHz signal in an RIAA circuit. Of special interest also is the use of all DC coupling. This eliminates the overload recovery problems associated with coupling and bypass capacitors. Worst case DC output offset voltage is about 1V with a cartridge having 1 kΩ DC resistance.



NOTE Cartridge is assumed to have less than 5 kΩ DC resistance Do not capacitor couple the cartridge R1, R2, and R3 should be low noise metal film resistors

FREQUENCY (Hz)	TOTAL HARMONIC DISTORTION				
20	<0.002	<0.002	<0.002	<0.002	<0.002
100	<0.002	<0.002	<0.002	<0.002	<0.002
1k	<0.002	<0.002	<0.002	<0.002	<0.002
10k	<0.002	<0.002	<0.002	0.0025	<0.003
20k	<0.002	<0.002	0.004	0.004	0.007
	0.03	0.1	0.3	1.0	5.0

OUTPUT AMPLITUDE (V) RMS

FIGURE 3. Ultra Low Noise RIAA Phono Preamplifier

Low Noise Applications (Continued)

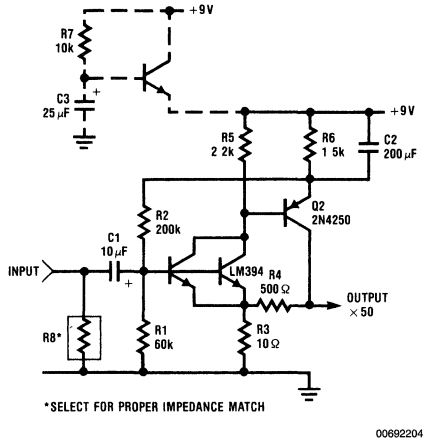


FIGURE 4. Ultra Low Noise Preamplifier

The single-ended amplifier shown in *Figure 4* was designed for source impedances below 250Ω. At this level, the LM194 should be biased at 2.5 mA (or higher) collector current. Unfortunately, r_{bb}', even at 40Ω, is the limiting factor on noise at these current levels. To achieve better performance, the two halves of the LM194 are paralleled to reduce r_{bb}' to 20Ω. Total input voltage noise for this design is given by:

$$e_N = \sqrt{4kT(r_{bb}' + R_3) + e_n^2}$$
$$= \sqrt{0.504 + 0.096} = 0.775\ nV/\sqrt{Hz}$$

The current noise is 1.2 $pA/\sqrt{Hz}$, and when this flows through a 250Ω source resistance, it causes an additional 0.30 $nV/\sqrt{Hz}$. Since the Johnson noise of a 250Ω resistor is 2.0 $nV/\sqrt{Hz}$, the noise figure is:

$$NF = 20 \log \frac{\sqrt{(2\ nV)^2 + (0.3\ nV)^2 + (0.775\ nV)^2}}{2nV} = 0.74\ dB$$

Several unique features of this circuit should be pointed out. First, it has only one internal capacitor which functions as an AC bypass for both stages. Second, no input stage load resistor bypassing is used, yet the circuit achieves 56 dB supply rejection referred to input. The optional supply filter shown in dotted lines improves this by an additional 50 dB and is necessary only if supply noise exceeds 20 $nV/\sqrt{Hz}$. Finally, the problem of AC coupling the 10Ω feedback impedance is eliminated by using a DC biasing scheme which biases both stages simultaneously without relying on feedback from the output.

Harmonic distortion is very low for a "simple" two stage design. At 300 mV output, total harmonic distortion measured 0.016%. For normal signal levels of 50 mV and below, distortion was lost in the noise floor. Small-signal bandwidth is 3 MHz.

An ideal application for this amplifier is as a head pre-amp for moving-coil phono cartridges. These cartridges have very low output impedance (< 50Ω at low frequencies) and have a full-output signal below 1 mV. Obviously, the preamp used for such a low signal level must have superb noise properties. The amplifier shown has a total RMS input noise of 0.11 µV in a 20 kHz bandwidth, yielding a signal-to-noise ratio of 70 dB when used with a 40Ω source impedance at a 0.5 mV signal level.

Low-Noise, Low-Drift Instrumentation Amplifier has Wide Bandwidth

The circuit in *Figure 5* is a high-performance instrumentation amplifier for low-noise, low-drift, wide-bandwidth applications. Input noise voltage is 2 $nV/\sqrt{Hz}$ up to 20 kHz, rising

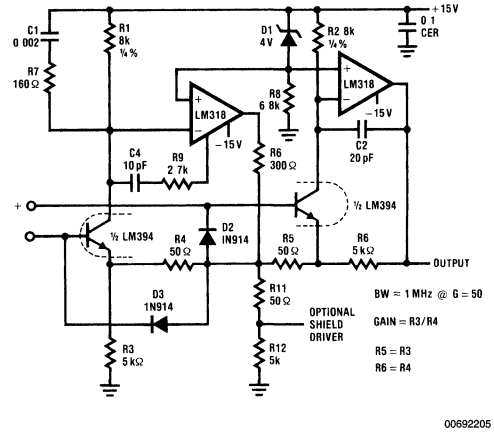


FIGURE 5. Low Drift-Low Noise Instrumentation Amplifier

to 3.5 $nV/\sqrt{Hz}$ at 100 kHz. Bandwidth at a gain of 50 is 1 MHz and gain can be varied over the range of 10–100 simply by changing the value of R_3 and R_6. Input offset voltage drift is determined by the LM194 and the tracking of the (R_1–R_2), (R_3–R_6), and (R_4–R_5) pairs. 20 ppm/°C mismatch on all pairs will generate 1.1 µV/°C referred to input, dominating the drift due to the LM194. Resistor pairs which track to 5 ppm/°C or better are recommended for very low drift applications. Input bias current is about 1 µA, rather high for general purpose use, but necessary in this case to achieve wide bandwidth and low noise. The tight matching of the LM194, however, reduces input offset current to 20 nA, and input offset current drift to 0.5 nA/°C. Input bias current drift is under 10 nA/°C. In terms of source impedance, total input referred voltage drift will be degraded 1 µV/°C for each 100Ω of unbalanced source resistance and 0.05 µV/°C for each 100Ω of balanced source resistance. DC common

Low-Noise, Low-Drift Instrumentation Amplifier has Wide Bandwidth (Continued)

mode rejection of this amplifier is extremely good, depending mostly on the match of the ratio of R_3/R_4 to R_5/R_6. 0.1% matching gives better than 90 dB. Rejection will improve with tighter matching and is not limited by the LM194 until CMRR approaches 120 dB. High frequency CMRR is also very good, measuring 80 dB at 20 kHz and 60 dB at 100 kHz. Settling time for a 10V output step is 1.5 µs to 0.1%, and 5 µs to 0.01%. Distortion with 10 V_{p-p} output is virtually unmeasurable (< 0.002%) at low frequencies, rising to 0.1% at 50 kHz, and 1% at 200 kHz.

Low Drift Designs

Offset voltage drive in the LM194 quite closely follows the theoretical value derived by differentiating the logarithmic formula. In other words it is a function only of the original offset voltage. If V_{OS} is the original room temperature offset voltage, drift of offset as given by differentiation yields:

$$\frac{d(V_{OS})}{dT} = \frac{\left(d\,kT/q \ln e^{\frac{V_{OS}}{kT/q}}\right)}{dT}$$

$$= \frac{V_{OS}}{T}$$

At room temperature (T = 297°K), 1 mV of offset voltage will generate 1 mV/297°K = 3.37 µV/°C drift. The LM194 with a maximum offset voltage of 50 µV could be expected to have a maximum offset voltage drift of 0.17 µV/°C. Lab measurements indicate that it does not deviate from this theoretical drift by more than 0.1 µV/°C. This means the LM194 can be specified at 0.3 µV/°C drift without an individual drift test on each device. In addition, if initial offset voltage is zeroed out, maximum drift will be less than 0.1 µV/°C. The zeroing, of course, must be done in a way that theoretically zeroes drift. This is best done as shown in *Figure 6* with a small trimpot used to unbalance collector load resistors. (See National's Application Note AN-3.)

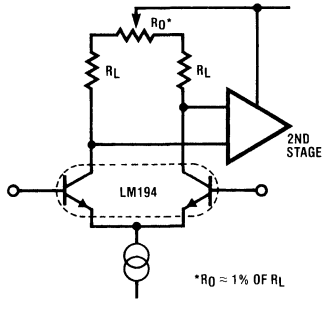


FIGURE 6. Zeroing Offset and Drift

To obtain optimum performance from such a low-drift device, strict attention must be paid to sources of drift external to the device itself. These include thermocouple effects, mismatch in load-resistor temperature coefficients, second-stage loading, collector leakage, and finite source impedance.

Thermocouple effects in ultra-low-drift amplifiers are often the limiting factor in performance. The copper-to-Kovar (LM194 leads) thermocouple will generate 35 µV/°C. This sounds extremely high, but is not a problem if all input leads on the LM194 are at the same temperature. For optimum drift performance, the differential lead temperature where copper connects to Kovar should not exceed 0.5 millidegrees per degree change in ambient. If the LM194 is mounted on a printed circuit board, emitter and base leads should be soldered to identical size pads and the package orientation should place emitter and base leads on isothermal lines if any significant power is being dissipated on the board. The board should be kept in a still-air environment to minimize the effects of circulating air currents. "Still" air is particularly important when the LM194 leads are soldered directly to wires and when low (< 10 Hz) noise is critical Individual wires in air can easily generate a differential end temperature of 10 millidegrees in an ordinary room ambient, even with the wires twisted together. This can cause up to 1 μV_{p-p} fluctuation in offset voltage. The 0.001 Hz to 10 Hz noise of the LM194 operating differentially at 100 µA is typically 40 nV_{p-p} (see *Figure 7*), so the thermally generated signal represents a 25:1 degradation of low frequency noise.

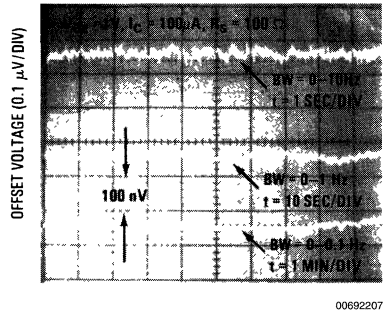


FIGURE 7. Low Frequency Noise of Differential Pair. Unit must be in still air environment so that differential lead temperature is held to less than 0.0003°C.

If the load resistors used to bias the LM194 do not have identical temperature coefficients, they will contribute to offset voltage drift. A 1 ppm/°C mismatch in resistor drift will generate 0.026 µV/°C drift in the LM194. Resistors with 10 ppm/°C differential drift will seriously degrade the drift of an otherwise perfect circuit design. Resistors specified to track better than 2 ppm/°C are available from several manufacturers including Vishay, Julie, RCL, TRW, and Tel Labs.

Source impedance must be considered in a low-drift amplifier since voltage drift at the output can result from drift of the base currents of the LM194. Base current changes at about −0.8%/°C. This is equal to 2 nA/°C at a collector current of 100 µA and an h_{FE} of 400. If drift error caused by the changing base current is to be kept to less than 0.05 µV/°C,

Low Drift Designs (Continued)

source unbalance cannot exceed 25Ω in this example. If a balanced condition exists, source impedance is still limited by the base current mismatch of the LM194. Worst case offset in the base current is 2%, and this offset can have a temperature drift of up to 2%/°C, yielding a change in offset current of up to

$$(2\%)(100\ \mu A)(2\%/^\circ C)/h_{FE} = 0.1\ nA/^\circ C$$

at a collector current of 100 µA. This limits balanced source impedances to 500Ω at collector currents of 100 µA if drift error is to be kept under 0.05 µV/°C. For higher source impedances, collector current must be reduced, or drift trimming must be used.

Collector-leakage effects on drift are generally very low for temperatures below 50°C. At higher temperatures, leakage can be a factor, especially at low collector currents. At 70°C, total collector leakage (to base and substrate) is typically 2 nA, increasing at 0.2 nA/°C. Assuming a 10% mismatch between collector leakages, input-referred drift will be 0.05 µV/°C at a collector current of 10 µA, and 0.005 µV/°C at 100 µA. At 125°C, input referred drift will be 1.5 µV/°C and 0.15 µV/°C respectively.

The amplifier used in conjunction with the LM194 may contribute significantly to drift if its own drift characteristics are poor. An LM194 operated with 2.5 V_{DC} across its load resistors has a voltage gain of approximately 100. If the second stage amplifier has a voltage drift of 20 µV/°C (normal for an amplifier with V_{OS} = 6 mV) the drift referred to the LM194 inputs will be 0.2 µV/°C, a significant degradation in drift. Amplifiers with low drift such as the LM108A or LM308A (5 µV/°C max) are recommended.

For the ultimate in low drift applications, the residual drift of the LM194 can be zeroed out. This is particularly easy because of the known relationship between a change in room-temperature offset and the resultant change in offset drift. The zeroing technique involves only one oven test to establish initial drift. The drift can then be reduced to below 0.03 µV/°C with a simple room-temperature adjustment. The procedure is as follows: (See *Figure 8.*)

1. Zero the offset voltage at room temperature (T_A).
2. Raise oven temperature to desired level (T_H) and measure offset voltage.
3. Bring circuit back to room temperature and adjust offset voltage to (V_{OS} at T_H) • (T_A)/(T_H − T_A). (T is in °K.)
4. Re-adjust offset voltage to zero with an external reference source by summing the two signals. (Do not re-adjust the offset of the LM194.)

This technique can be extended to include drift correction for source-generated drift as well since the basic correcting mechanism *is independent of the source of drift.*

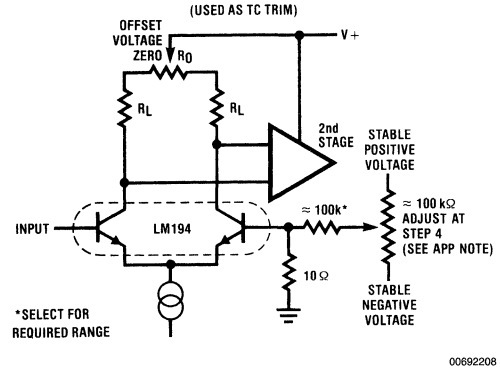


FIGURE 8. Correcting for Residual or Source Generated Drift

Voltage Reference

Voltage references utilizing the bandgap voltage of silicon were first used 8 years ago, and have since gained wide acceptance in such circuits as the LM109, LM113, LM340, LM117, µA7800, AD580, and REF 01. The theory has been well publicized and is not reiterated here.

The circuit in *Figure 9* is a micropower version of a bandgap technique first used by Analog Devices. It operates off a single 2.5V to 6V supply and draws only 25 µA idling current. Two AA penlight cells will power the reference for over a year of continuous operation. Maximum output current is 0.5 mA, with an output resistance of 0.2Ω. Line regulation is ~0.01%/V and output noise is 20 μV_{RMS} over a 10 kHz bandwidth. Temperature drift is less than ±50 ppm/°C when the output is trimmed to 1.21V. Much lower drift can be obtained by adjusting the output of each reference to the optimum value. A 1% shift in output voltage changes drift 33 ppm/°C. Temperature range is −25°C to +100°C.

The LM194 is the entire reference in this design, supplying both V_{BE} and ΔV_{BE} portions of the reference. One half LM114 delivers a constant bias current to the LM4250. The other half, in conjunction with the 2N4250 PNP, ensures startup of the circuit under worst cast (2.4k) load current. R_1–R_2 and R_4–R_5 should track to 50 ppm/°C. R_6 should have a TC of under 250 ppm/°C. The circuit is stable for capacitive loads up to 0.047 µF. C_2 is optional, for improved ripple rejection.

Strain Gauge Amplifier

The instrumentation amplifier shown in *Figure 10* is an example of an ultra-low-drift design specifically optimized for strain-gauge applications. A typical strain-gauge bridge has one end grounded and the other driven by a 3-to-10 volt precision voltage reference. The differential output signal of the bridge has a 1.5 to 5 volt common-mode level and a typical full-scale differential signal level of 5–50 mV. Source impedance is in the range of 100Ω to 500Ω, with an impedance imbalance of less than 2%. This amplifier has been specifically optimized for these types of signals. It has a +1V to +10V common mode range, a full scale input of 20 mV (1 mV to 100 mV is possible) and fully balanced inputs with a differential input impedance > 10 MΩ. Common mode input impedance is 100 MΩ. Common mode rejection ratio is 120 dB at 60 Hz, 114 dB at 1 kHz, and 94 dB at 10 kHz referred to input. Power supply rejection at DC is 114 dB on the V+ supply and 108 dB on the V− supply. Small signal bandwidth is > 50 kHz and slew rate is 0.1 V/µs. Gain error is determined by the accuracy of R_9, R_8, R_4, and R_3. For the values shown, gain is 500. R_3 can be varied to set gain as desired from 250 (800Ω) to 10,000 (20Ω). Gain non-linearity is < 0.05% for a 10V output and < 0.012% for a 5V output). R_7 is a +0.3%/°C positive-temperature-coefficient wirewound resistor for compensation of gain with temperature. Without this resistor, gain change with temperature is 0.007%/°C. If R_7 is omitted, replace R_9 with 12.4 kΩ.

Input offset voltage drift is determined primarily by resistor mismatches between R_1/R_2 and R_5/R_6. If either of these ratios drifts by 5 ppm/°C, an input offset voltage drift of 0.15 µV/°C will be created. Other resistor drifts contribute to gain error only. R_{12} is used to adjust room temperature offset voltage to zero.

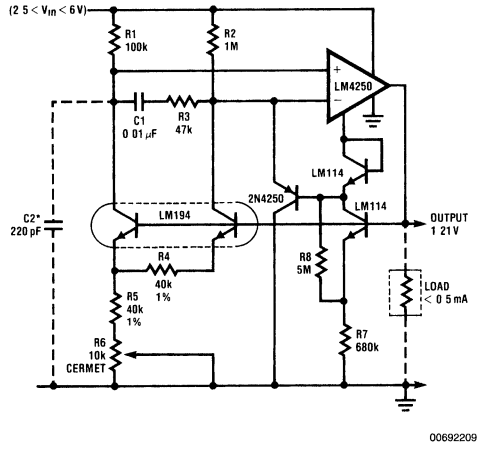


FIGURE 9. Micropower Reference

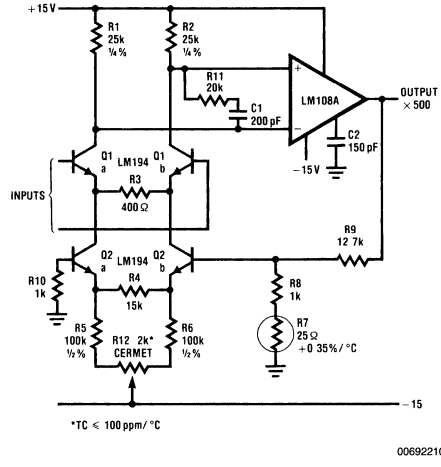


FIGURE 10. Strain Gauge Instrumentation Amplifier

Thermocouple Amplifier with Cold Junction Compensation

Thermocouple amplifiers need low offset voltage drift, good gain accuracy, low noise, and most importantly, cold-junction compensation. The amplifier in *Figure 11* does all that and more. It is specifically designed for ease of calibration so that repeated oven cycling is not required for calibration of gain and zero. Also, no mathematical calculations are required in the calibration procedure.

The circuit is basically a non-inverting amplifier with the gain set to give 10 mV/(°F or °C) at the output. This output sensitivity is arbitrary and can be set higher or lower. Cold-junction compensation is achieved by deliberately unbalancing the collector currents of the LM194 so that the resulting input offset voltage drift is just equal to the thermocouple output (α) at room temperature. By combining the formulas for offset voltage versus current imbalance and offset voltage drift, the required ratio of collector currents is obtained.

$$\frac{d(V_{os})}{dT} = \frac{V_{OS}}{T} = \frac{k}{q} \ln \frac{I_{C_1}}{I_{C_2}}$$

$$\ln \frac{I_{C_1}}{I_{C_2}} = \frac{q \bullet V_{OS}}{k \bullet T} = \frac{q \bullet \alpha}{k}$$

$$\frac{I_{C_1}}{I_{C_2}} = e^{\frac{q \bullet \alpha}{k}}$$

(α = thermocouple output in V/°C)

This technique does require that the LM194 be at the same temperature as the thermocouple cold junction. The thermocouple leads should be terminated close to the LM194.

The deliberate offset voltage created across the LM194 inputs must be subtracted out with an external reference which is also used to zero shift the output to read directly in °C or °F. This is done in a special way so that at some arbitrarily selected temperature (T_1), the gain adjustment has no effect on zero, vastly simplifying the calibration procedure. Design equations for the circuit are shown with the schematic in descending order of their proper use. Also shown is the calibration procedure, which requires only one oven trip for both gain and zero. Use of the nearest pocket calculator should yield all resistor values in a few minutes. The values shown on the schematic are for a 10 mV/°C output with a Chromel-Alumel thermocouple delivering 40 µV/°C, with T_1 selected at room temperature (297°K). All resistors except R_8 and R_{12} should be 1% metal film types for low thermocouple effects (resistors *do* generate thermocouple voltages if their ends are at different temperatures) and should have low temperature coefficients. R_9 and R_{10} should track to 10 ppm/°C. R_3, R_6, and R_{11} should not have a TC higher than 250 ppm/°C. R_1, R_2, and R_4 should track to 20 ppm/°C. C_2 can be added to reduce spikes and noise from long thermocouple lines.

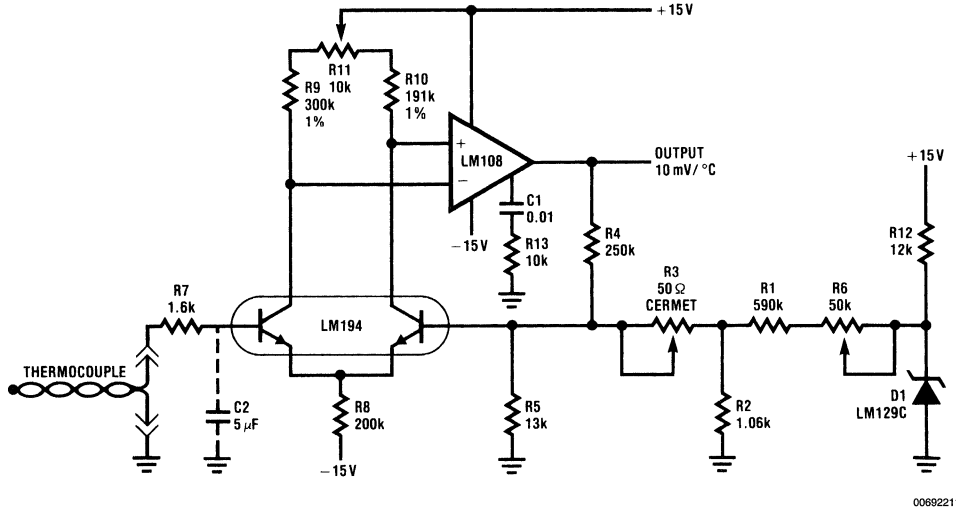


FIGURE 11. Thermocouple Amplifier with Cold-Junction Compensation

1. Select R9 = 300 kΩ
2. Set R10 equal to R9 • $e^{-\alpha(1\ 16 \times 104)}$
3. R8 = 200k
4. Select R4 in the range 50 kΩ to 250 kΩ

Thermocouple Amplifier with Cold Junction Compensation (Continued)

5.

$$R5 = \frac{(R4)(T_1)(\alpha)}{S(T_1 - T_0) - \alpha(T_1)}$$

6.

$$R2 = \frac{\alpha(R4)(R5)(1 - E^*/100)}{(S - \alpha)\left[R5 - \frac{\alpha(R4)}{S - \alpha}\right]}$$

7.

$$R1 = \frac{[(R2) \bullet V_Z - \alpha(T_1)]}{\alpha(T_1)} (0\ 95)$$

8.

$$R3 = \frac{(E)(R2)}{50}$$

9. R7 = (R9/R10)(R2)

10. R6 = R1/10

E= Gain error allowed for (≈2.5%)

T_1= Temperature in °K at which it is desired to have the gain control not interact with the zero control

T_0= Temperature in °K at which the desired temperature scale (°C or °F) is equal to zero

S= Required output scale factor. Use V/°C even though actual output may be in °F

V_Z= Zener reference voltage

α= Thermocouple output in V/°C

Values shown on schematic are for 10 mV/°C.

See below for 10 mV/°F values using a Chromel-Alumel thermocouple with room temperature for T_1.

R1 = 367k, R2 = 629Ω, R3 =Ω, R4 = 250k,

R5 = 4.08k, R6 = 50k, R7 = 1k, R10 = 191k

CALIBRATION: (Note 1)

a. Set oven to T_1 and adjust R6 to give proper output (zero adjust).

b. Raise (or lower) oven to T_2 and adjust R3 to give proper output at T_2 (gain adjust).

c. Return to room temperature and short thermocouple and D1 to ground. Adjust R11 to give proper output (room ambient) in °K or °R.

   For 10 mV/°C, this is 2.98V @ T_A = 25°C.

   For 10 mV/°F, this is 5.37V @ T_A = 77°F.

d. Remove shorts and re-adjust R6 if necessary to zero output.

   Note: Steps C and D can be eliminated if exact cold junction compensation is not required. R11 is simply shorted out. Compensation will be within ±5% without adjustment (≤0.05°C/°C).

Note 1: Thermocouple only in oven

Input impedance for this circuit is > 100 MΩ, so high thermocouple impedance will not affect scale factor. "Zero shift" due to input bias current is approximately 1°C for each 400Ω of thermocouple lead resistance with a 40 µV/°C thermocouple.

No provision is made for correction of thermocouple non-linearity. This could be accomplished with a slight non-linearity introduced into R_4 with additional resistors and diodes. Another possibility is to digitize the output and correct the nonlinearity digitally with a ROM programmed for a specific thermocouple type.

Power Meter

The power meter in *Figure 12* is a good example of minimum-parts-count design. It uses only one transistor pair to provide the complete (X) • (Y) function. The circuit is intended for 117 V_{AC} ± 50 V_{AC} operation, but can be easily modified for higher or lower voltages. It measures true (non-reactive) power being delivered to the load and requires no external power supply. Idling power drain is only 0.5W. Load current sensing voltage is only 10 mV, keeping load voltage loss to 0.01%. Rejection of reactive load currents is better than 100:1 for linear loads. Nonlinearity is about 1% full scale when using a 50 µA meter movement. Temperature correction for gain is accomplished by using a copper shunt (+0.32%/°C) for load-current sensing. This circuit measures power on negative cycles only, and so cannot be used on rectifying loads.

Low Cost Mathematical Functions

Many analog circuits require a mathematical function to be performed on one or more signals other than the standard addition, subtraction, or scaling which can be accomplished with resistor networks. The circuits shown in *Figure 13* through *Figure 15* are examples of low-cost function generating circuits using the LM394 with operational amplifiers. The logarithmic relationship of V_{BE} to I_C on the LM394 is utilized in each case to log-antilog the input signals so that addition and subtraction can be used to multiply, divide, square, etc. When transistors are used in this manner, matching is very critical. A 1 mV offset in V_{BE} appears as a *4% of signal* error even in the best case where operation is restricted to one quadrant. Parasitic emitter or base resistance (r_{ee}', r_{bb}'') can also seriously degrade accuracy. At I_C = 100 µA and h_{FE} = 100, each Ω of emitter resistance and each 100Ω of base resistance will cause 0.4% signal error. Most matched transistor pairs available today have significant parasitic resistances which severely limit their use in high-accuracy circuits. The LM394, with offset guaranteed below 0.15 mV and a typical emitter-referred total parasitic resistance of 0.4Ω gives an order of magnitude improvement in accuracy to nonlinear designs at all current levels.

Multiplier/Divider

The circuit in *Figure 13* will give an output proportional to the product of the (X) and (Y) inputs divided by the Z input. All inputs must be positive, limiting operation to one quadrant, but this restriction removes the large error terms found in 2- and 4-quadrant designs. In a large percentage of cases, analog signals requiring multiplication are of one polarity only and can be inverted if negative. A nice feature of this design is that all gain errors can be trimmed to zero at one point. R_5 is paralleled with 2.4 MΩ to drop its nominal value 2%. R_8 then gives a ±2% gain trim to account for errors in

Multiplier/Divider (Continued)

R_1, R_2, R_5, R_7, and any offset in Q_1 or Q_2. For very low level inputs, offset voltage in the LM308s may create large percentage errors referred to input. A simple scheme for offsetting any of the LM308s to zero is shown in dotted lines; the + input of the appropriate LM308 is simply tied to R_x instead of ground for zeroing. The summing mode of operation on all inputs allows easy scaling on any or all inputs. Simply set the input resistor equal to $(V_{IN(max)})/(200\ \mu A)$. V_{OUT} is equal to:

$$V_{OUT} = \frac{\left(\frac{X}{R_1}\right)\left(\frac{Y}{R_2}\right)(R_5)}{\frac{Z}{R_7}}$$

Input voltages above the supply voltage are allowed because of the summing mode of operation. Several inputs may be summed at "X", "Y," or "Z."

Proper scaling will improve accuracy by preventing large current imbalances in Q_1 and Q_2, and by creating the largest possible output swing. Keep in mind that any multiplier scheme must have a reference and this circuit is no different. For a simple (X) • (Y) or (X)/Z function, the unused input must be tied to a reference voltage. Perturbations in this reference will be seen at the output as scale factor changes, so a stable reference is necessary for precision work. For less critical applications, the unused input may be tied to the positive supply voltage, with $R = V^+/200\ \mu A$.

Square Root

The circuit in *Figure 14* will generate the square root function at low cost and good accuracy. The output is a current which may be used to drive a meter directly or be converted to a voltage with a summing junction current-to-voltage converter. The −15V supply is used as a reference, so it must be stable. A 1% change in the −15V supply will give a ½% shift in output reading. No positive supply is required when an LM301A is used because its inputs may be used at the same voltage as the positive supply (ground). The two 1N457 diodes and the 300 kΩ resistor are used to temperature compensate the current through the diode-connected ½ LM394.

Squaring Function

The circuit in *Figure 15* will square the input signal and deliver the result as an output current. Full scale input is 10V, but this may be changed simply by changing the value of the 100 kΩ input resistor. As in the square root circuit, the −15V supply is used as the reference. In this case, however, a 1% shift in supply voltage gives a 1% shift in output signal. The 150 kΩ resistor across the base-emitter of ½ LM394 provides slight temperature compensation of the reference current from the −15V supply. For improved accuracy at low input signal levels, the offset voltage of the LM301A should be zeroed out, and a 100 kΩ resistor should be inserted in the positive input to provide optimum DC balance.

Bibliography

1. See National's *Audio Handbook.*
2. *The Audio Amateur,* volume VIII, number 1, Feb. 1977.

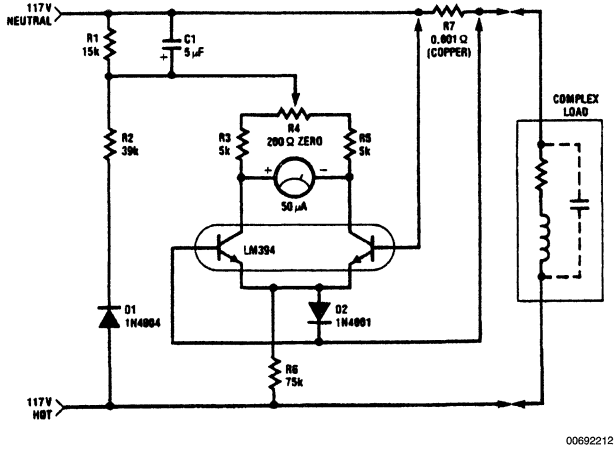
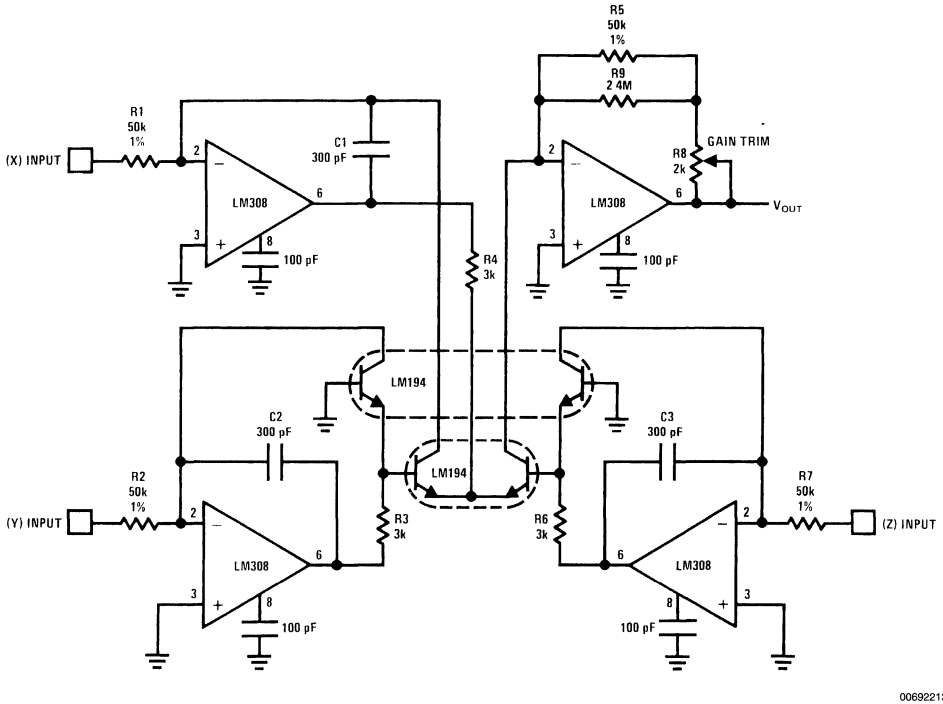


FIGURE 12. Power Meter (1 kW f.s.)



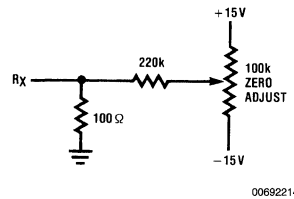
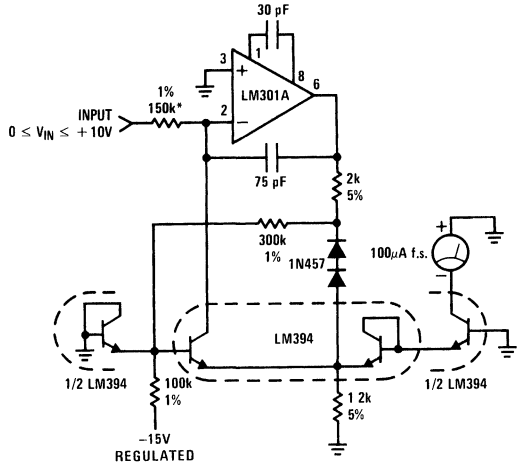
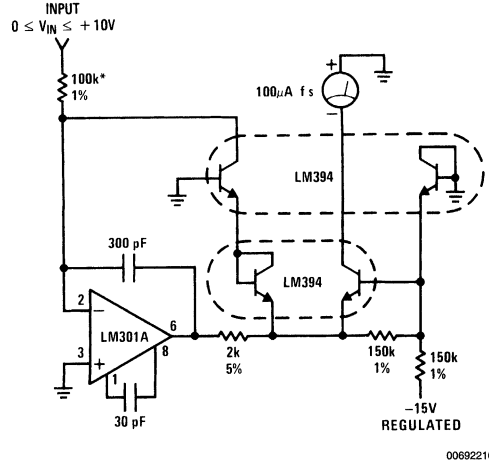


FIGURE 13. High Accuracy One Quadrant Multiplier/Divider



*Trim for full scale accuracy.

FIGURE 14. Low Cost Accurate Squaring Circuit
$I_{OUT} = 10^{-5}\sqrt{10\,V_{IN}}$



*Trim for full scale accuracy

FIGURE 15. Low Cost Accurate Squaring Circuit$I_{OUT} = 10^{-6}\,(V_{IN})^2$

Introducing the MF10: A Versatile Monolithic Active Filter Building Block

National Semiconductor
Application Note 307
Tim Regan

A unique alternative for active filter designs is now available with the introduction of the MF10. This new CMOS device can be used to implement precise, high-order filtering functions with no reactive components required.

Filter design takes one of two approaches: passive or active. Passive designs combine resistors, capacitors and inductors to perform specific frequency filtering in applications where precision is less important than mass producibility. For very high frequency applications, a passive approach is quite often the only way to go. Active filters combine op amps and discrete transistors, primarily with resistors and capacitors, to provide impedance buffering and filter parameter tunability. In precision filters, it is most desirable to have an independent "handle" for each of three basic filter parameters: resonant frequency (f_o), Q or quality factor, and the passband gain (H_o). As a general rule, the degree of tunability increases with the number of amplifiers used. The three op amp, state variable active filter, *Figure 1*, is most popular for 2nd order designs.

A major shortcoming of this type of filter is that resonant frequency accuracy is only as good as the capacitors used. In high volume production, to minimize filter tuning procedures, costly, low-tolerance, low-drift capacitors are required. Furthermore, these filters use a fair number of components; 3 op amps, 7 resistors and 2 capacitors for each 2nd order section. Even the best single amplifier 2nd order filter realizations require 3 to 5 resistors and 2 capacitors.

To offer designers an attractive alternative to these types of active filters, a device would have to:

1) eliminate critical capacitors entirely

2) minimize overall parts count

3) provide easy tunability of filter parameters

4) allow for the design of all five filter responses and,

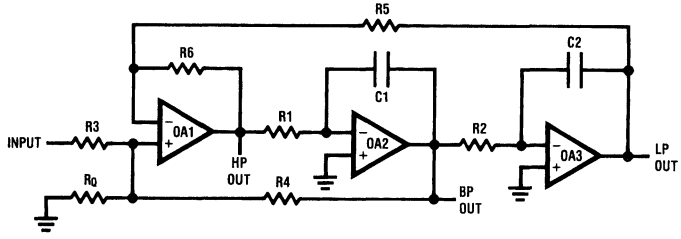
5) simplify design equations.

These are the design objectives behind the development of the MF10. Recent advances in sample-data techniques permit the construction of an op amp integrator on a monolithic substrate without the need for any external capacitors (see page 11 "The Switched Capacitor Integrator—How it Works"). The integrator is a key factor in filter designs for establishing the overall filter time constant and, therefore, its resonant frequency. The MF10 contains, in one 20-pin DIP package, all of the necessary active and reactive components to construct two complete 2nd order state variable type active filters, *Figure 2*. The only external requirements are for resistors to establish the desired filter parameters.

Basic Circuit Description

To keep the device as universal as possible, the outputs of each section of each filter are brought out. This allows designs for all five filtering functions: lowpass, bandpass, highpass, allpass and bandreject or notch filters. With two independent 2nd order sections in one package, cascading to achieve 4th order responses can easily be accomplished. Additionally, any of the classical filter response types such as Butterworth, Chebyshev, Bessel and Cauer can be implemented.

Between the output of the summing op amp and the input of the first integrator there is a unique 3-input summing stage where two of the inputs are subtracted from the third. One of the (–) inputs is brought out to serve as the signal input for some filter configurations. The other (–) input is connected through an internal switch to either the lowpass output or analog ground depending upon the desired filter implementation. The direction of this input connection is common to both halves of the MF10 and is controlled by the voltage level on the $S_{A/B}$ input terminal.



$$f_o = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}}\sqrt{\frac{1}{R1\ R2\ C1\ C2}}$$

$$Q = \left(\frac{1 + \frac{R4}{R3} + \frac{R4}{R0}}{1 + \frac{R6}{R5}}\right)\sqrt{\frac{R6\ R1\ C1}{R5\ R2\ C2}}$$

FIGURE 1. The Universal State Variable 2nd Order Active Filter (note the complexity of design equations and the number of critical external components)

Basic Circuit Description (Continued)

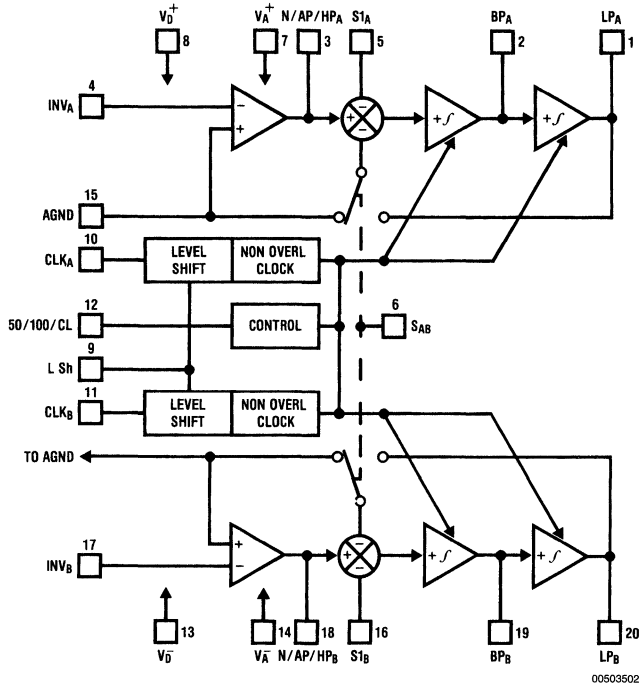


FIGURE 2. Block Diagram of the MF10

When tied to V_D^+ [the (+) supply], the switch connects the lowpass output, and when tied to V_D^- [the (–) supply], the connection to ground is made. In some applications one half of the MF10 may require that both of the (–) inputs to this summer be connected to ground, while the other side requires one to be connected to the lowpass output and the other to ground. For this, the $S_{A/B}$ control should be tied to the (–) supply and the connection to the lowpass output should be made externally to the $S1_A$ ($S1_B$) pin.

A clock with close to 50% duty cycle is required to control the resonant frequency of the filter. Either TTL or CMOS logic compatible clocks can be accommodated, whether the MF10 is powered from split supplies or a single supply, by simply grounding the level shift (L Sh) control pin.

The resonant frequency of each filter is directly controlled by its clock. A tri-level control pin sets the ratio of the clock frequency to the center frequency (the 50/100/CL pin) for both halves. When this pin is tied to V^+ the center frequency will be 1/50 of the clock frequency. When tied to mid-supply potential (i.e., ground, when biased from split supplies) provides 100 to 1 clock to center frequency operation. When this pin is tied to V^- a power saving supply current limiter shuts down operation and rolls back the supply current by 70%.

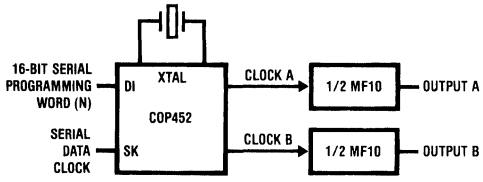
Filter center frequency accuracy and stability are only as good as the clock provided. Standard crystal oscillators, combined with digital counters, can provide very stable clocks for specific filter frequencies. A relatively new device from National's COPS™ family of microcontrollers and peripherals, the COP452 programmable frequency generator/counter, finds a unique use with the MF10, *Figure 3*. This low cost device can generate two independent 50% duty cycle clock frequencies. Each clock output is programmed via a 16-bit serial data word (N). This allows over 64,000 different clock frequencies for the MF10 from a single crystal.

The MF10 is intended for use with center frequencies up to 20 kHz, and is guaranteed to operate with clocks up to 1 MHz. This means that for center frequencies greater than 10 kHz, the 50 to 1 clock control should be used. The effect of using 100 to 1 or 50 to 1 clock to center frequency ratio manifests itself in the number of "stair-steps" apparent in the output waveform. The MF10 closely approximates the time and frequency domain response of continuous filters (RC active filters, for example) but does so using sampling techniques. The clock to center frequency control determines the number of samples taken (1 per clock cycle) in one cycle of the center frequency. Therefore, as shown in the photo of *Figure 4*, 100 to 1 clocking provides a smoother looking output as it has twice as many samples per cycle. For most audio applications, the audible effects of these step edges and the clock frequency component in the output are negligible as they are beyond 20 kHz. To obtain a cleaner output waveform, a simple passive RC lowpass can be added to the output to serve as a smoothing filter without affecting the MF10 filtering action.

Several of the modes of operation (discussed in a later section) allow altering of the clock to center frequency ratio by an external resistor ratio. This can be used to obtain

Basic Circuit Description (Continued)

center frequencies of values other than 1/50 or 1/100 of the clock frequency. In multiple stage, staggered tuned filters, the center frequency of each stage can be set independently with resistors to allow the overall filter to be controlled by just one clock frequency.



$$f_{CLK} = \frac{f_{XTAL}}{2(1+N)}$$

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FIGURE 3. A Programmable Dual Clock Generator

All of the rules of sampling theory apply when using the MF10. The sampling rate, or clock frequency, should be at least twice the maximum input frequency to produce the best equivalent to a continuous time filter. High frequency components in the input signal that approach the clock frequency will generate aliasing signals which appear at the output of the lower frequency filter and are indistinguishable from valid passband signals. Bandlimiting the input signal to attenuate these potential aliasing frequencies is the best preventative measure. In most applications, aliasing will not be a problem as the clock frequency is much higher than the passband of interest. In the event that a much higher clock frequency is required, the modes of operation which utilize external resistor ratios to increase the clock to center frequency ratio can extend the clock frequency to greater than 100 times the center frequency. By using a higher clock frequency, the aliasing frequencies are correspondingly higher. The limiting factor, with regard to increasing the clock to center frequency ratio, has to do with increased DC offsets at the various outputs.

The Basic Filter Configurations

There are six basic configurations (or modes of operation) for the 2nd order sections in the MF10 to realize a wide variety of filter responses. In all cases, no external capacitors are required. Design is a simple matter of establishing a few resistor ratios to set the desired passband gain and Q and generating a clock for the proper resonant frequency. Each 2nd order section can be treated in a modular fashion, with regard to individual center frequency, Q and gain, when cascading either the two sections within a package or several packages for very high order filters. This individuality of sections is important in implementing the various response characteristics such as Butterworth, Chebyshev, etc.

The following is a general summary of design hints common to all modes of operation.

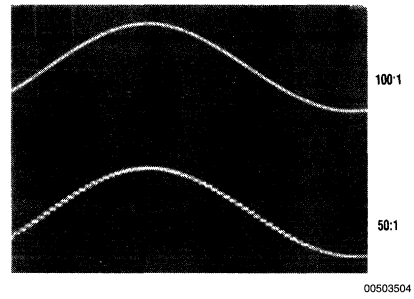

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FIGURE 4. The Sampled-Data Output Waveform

1. The maximum supply voltage for the MF10 is ±7V or just +14V for single supply operation. The minimum supply to properly bias the part is 8V.
2. The maximum swing at any of the outputs is typically within 1V of either supply rail.
3. The internal op amps can source 3 mA and sink 1.5 mA. This is an important criterion when selecting a minimum resistor value.
4. The maximum clock frequency is typically 1.5 MHz.
5. To insure the proper filter response, the f_oxQ product of each stage must be realizable by the MF10. For center frequencies less than 5 kHz, the f_oxQ product can be as high as 300 kHz (Q must be less than or equal to 150). A 3 kHz bandpass filter, for example, could have a Q as high as 100 with just one section. For center frequencies less than 20 kHz, the allowable f_oxQ product is limited to 200 kHz. A 10 kHz bandpass design using a single section should have a Q no larger than 20.
6. Center frequency matching from part to part for a given clock frequency is typically ±0.2%. Center frequency drift with temperature (excluding any clock frequency drift) is typically ±10 ppm/°C with 50:1 switching and ±100 ppm/°C for 100:1.
7. Q accuracy from part to part is typically ±2% with a temperature coefficient of ±500 ppm/°C.
8. The expressions for circuit dynamics given with each of the modes are important. They determine the voltage swing at each output as a function of the circuit Q. A high Q bandpass design can generate a significant peak in the response at the lowpass output at the center frequency.
9. Both sides of the MF10 are independent, except for supply voltages, analog ground, clock to center frequency ratio setting and internal switch setting for the three input summing stage.

The Basic Filter Configurations
(Continued)

In the following descriptions of the filter configurations, f_o is the filter center frequency, H_o is the passband gain and Q is the quality factor of the complex pole pair and is equal to f_o/BW where BW is the −3 dB bandwidth measured at the bandpass output.

MODE 1A: Non-Inverting Bandpass, Inverting Bandpass, Lowpass

This is a minimum external component configuration (only 2 resistors) useful for low Q lowpass and bandpass applications. The non-inverting bandpass output is necessary for minimum phase filter designs.

DESIGN EQUATIONS

$$f_o = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

$$Q = \frac{R3}{R2}$$

$$H_{OLP} = -1$$

$$H_{OBP_1} = -\frac{R3}{R2}$$

$$H_{OBP_2} = 1 \text{ (non-inverting)}$$

CIRCUIT DYNAMICS

$H_{OBP1} = -Q$ (this is the reason for the low Q recommendation)

$H_{OLP\ (peak)} = Q \times H_{OLP}$

MODE 1: Notch, Bandpass and Lowpass

With the addition of just one more external resistor, the output dynamics are improved over Mode 1A to allow bandpass designs with a much higher Q. The notch output features equal gain above and below the notch frequency.

DESIGN EQUATIONS

$$f_o = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

$$f_{notch} = f_o$$

$$Q = \frac{R3}{R2}$$

$$H_{OLP} = -\frac{R2}{R1}$$

$$H_{OBP} = -\frac{R3}{R1}$$

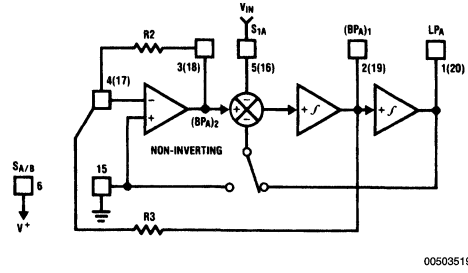
$$H_{ON} = -\frac{R2}{R1} \text{ as } f \longrightarrow 0 \text{ and as } f \longrightarrow \frac{f_{CLK}}{2}$$

CIRCUIT DYNAMICS

$H_{OBP} = H_{OLP} \times Q = H_{ON} \times Q$

$H_{OLP\ (peak)} = Q \times H_{OLP}$ (if the DC gain of the LP output is too high, a high Q value could cause clipping at the lowpass output resulting in gain non-linearity and distortion at the bandpass output).

MODE 1A



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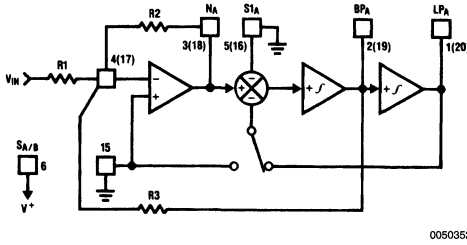
MODE 1



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MODE 2: Notch (with $f_n \leq f_o$), Bandpass and Lowpass

This configuration allows tuning of the clock to center frequency ratio to values greater than 100 to 1 or 50 to 1. The notch output is useful for designing elliptic highpass filters because the frequency of the required complex zeros (f_{notch}) is less than the frequency of the complex poles (f_o).

DESIGN EQUATIONS

$$f_o = \frac{f_{CLK}}{100}\sqrt{1+\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50}\sqrt{1+\frac{R2}{R4}}$$

$$f_n = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

$$Q = \frac{\sqrt{R_2/R_4+1}}{R_2/R_3}$$

$$H_{OLP} = \frac{-\frac{R2}{R1}}{1+\frac{R2}{R4}}$$

$$H_{OBP} = -\frac{R3}{R1}$$

$$H_{ON_1}\,(\text{as } f \rightarrow 0) = \frac{-\frac{R2}{R1}}{1+\frac{R2}{R4}}$$

$$H_{ON_2}\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}$$

CIRCUIT DYNAMICS

$$H_{OBP} = Q\sqrt{H_{OLP} \times H_{ON_2}} = Q\sqrt{H_{ON_1} \times H_{ON_2}}$$

MODE 3: Highpass, Bandpass and Lowpass

This configuration is the classical state variable filter (the circuit of *Figure 1*) implemented with only 4 external resistors. This is the most versatile mode of operation, since the clock to center frequency ratio can be externally tuned either above or below the 100 to 1 or 50 to 1 values. The circuit is suitable for multiple stage Chebyshev filters controlled by a single clock.

DESIGN EQUATIONS

$$f_o = \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R2}{R4}}$$

$$Q = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$$

$$H_{OHP} = -\frac{R2}{R1}$$

$$H_{OBP} = -\frac{R3}{R1}$$

$$H_{OLP} = -\frac{R4}{R1}$$

CIRCUIT DYNAMICS

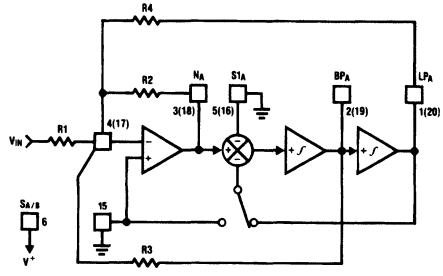
$$H_{OHP} = H_{OLP}\left(\frac{R2}{R4}\right)$$

$$H_{OLP\,(peak)} = Q \times H_{OLP}$$

$$H_{OBP} = Q\sqrt{H_{OHP} \times H_{OLP}}$$

$$H_{OHP\,(peak)} = Q \times H_{OHP}$$

MODE 2



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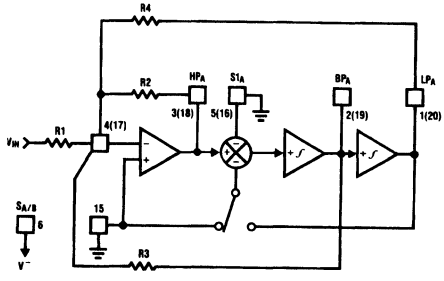
MODE 3



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MODE 3A: Highpass, Bandpass, Lowpass and Notch

A notch output is created from the circuit of Mode 3 by summing the highpass and lowpass outputs through an external op amp. The ratio of the summing resistors R_h and R_l adjusts the notch frequency independent of the center frequency. For elliptic filter designs, each stage combines a complex pole pair (at f_o) with a complex zero pair (at f_{notch}) and this configuration provides easy tuning of each of these frequencies for any response type. When cascading several stages of the MF10 the external op amp is needed only at the final output stage. The summing junction for the intermediate stages can be the inverting input of the MF10 internal op amp.

DESIGN EQUATIONS

$$f_o = \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R2}{R4}}$$

$$Q = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$$

$$f_{notch} = \frac{f_{CLK}}{100}\sqrt{\frac{R_h}{R_l}} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R_h}{R_l}}$$

$$H_{OHP} = -\frac{R2}{R1}$$

$$H_{OLP} = -\frac{R4}{R1}$$

$$H_{OBP} = -\frac{R3}{R1}$$

$$H_{ON}\,(\text{at } f = f_o) = \left| Q\left(\frac{R_g}{R_l}H_{OLP} - \frac{R_g}{R_h}H_{OHP}\right)\right|$$

$$H_{ON_l}\,(\text{as } f \rightarrow 0) = \frac{R_g}{R_l} \times H_{OLP}$$

$$H_{ON_h}\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = \frac{R_g}{R_h} \times H_{OHP}$$

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MODE 4: Allpass, Bandpass and Lowpass

Utilizing the $S1_A$ ($S1_B$) terminal as a signal input, an allpass function can be obtained. An allpass can provide a linear phase change with frequency which results in a constant time delay. This configuration restricts the gain at the allpass output to be unity.

DESIGN EQUATIONS

$$f_o = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

$$f_z \text{ (frequency of complex zero pair)} = f_o$$

$$Q = \frac{R3}{R2}$$

$$Q_z \text{ (Q of complex zero pair)} = \frac{R3}{R1}$$

$$H_{OAP} = -\frac{R2}{R1} = -1$$

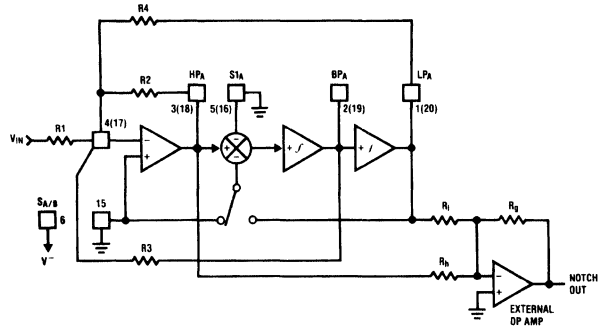
$$H_{OLP} = -\left(\frac{R2}{R1} + 1\right) = -2$$

$$H_{OBP} = -\left(1 + \frac{R2}{R1}\right)\frac{R3}{R2} = -2\frac{R3}{R2}$$

CIRCUIT DYNAMICS

$H_{OBP} = H_{OLP} \times Q = (H_{OAP} + 1)Q$

MODE 3A



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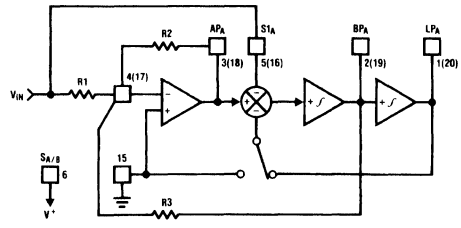
MODE 4: Allpass, Bandpass and Lowpass (Continued)

MODE 4



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MODE 5: Complex Zeros (C.z), Bandpass and Lowpass

This mode features an improved allpass design over that of Mode 4, in that it maintains a more constant amplitude with frequency at the complex zeros (C.z) output. The frequencies of the pole pair and zero pair are resistor tunable.

DESIGN EQUATIONS

$$f_o = \frac{f_{CLK}}{100}\sqrt{1+\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50}\sqrt{1+\frac{R2}{R4}}$$

$$f_z = \frac{f_{CLK}}{100}\sqrt{1-\frac{R1}{R4}} \text{ or } \frac{f_{CLK}}{50}\sqrt{1-\frac{R1}{R4}}$$

$$Q = \frac{R3}{R2}\sqrt{1+\frac{R2}{R4}}$$

$$Q_z = \frac{R3}{R1}\sqrt{1-\frac{R1}{R4}}$$

$$H_{O(C\,z)} \text{ as } f \longrightarrow 0 = \frac{R2(R4-R1)}{R1(R2+R4)}$$

$$H_{O(C\,z)} \text{ as } f \longrightarrow \frac{f_{CLK}}{2} = \frac{R2}{R1}$$

$$H_{OBP} = \frac{R3}{R2}\left(1+\frac{R2}{R1}\right)$$

$$H_{OLP} = \frac{R4}{R1}\left(\frac{R2+R1}{R2+R4}\right)$$

MODE 6A: Single Pole, Highpass and Lowpass

By using only one of the internal integrators, this mode is useful for creating odd-ordered cascaded filter responses by providing a real pole that is clock tunable to track the resonant frequency of other 2nd order MF10 sections. The corner frequency is resistor tunable.

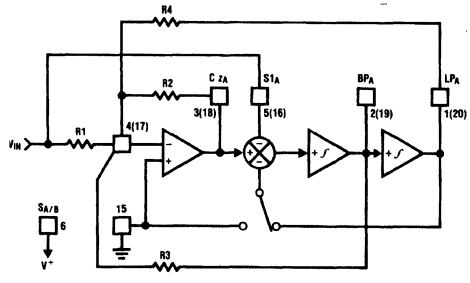
DESIGN EQUATIONS

$$f_c \text{ (cut-off frequency)} = \frac{f_{CLK}}{100}\left(\frac{R2}{R3}\right) \text{ or } \frac{f_{CLK}}{50}\left(\frac{R2}{R3}\right)$$

$$H_{OLP} = -\frac{R3}{R1}$$

$$H_{OHP} = -\frac{R2}{R1}$$

MODE 5



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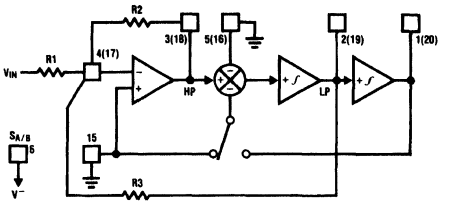
MODE 6A: Single Pole, Highpass and Lowpass (Continued)

MODE 6A



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MODE 6B: Single Pole Lowpass (Inverting and Non- Inverting)

This mode utilizes only one of the integrators for a single pole lowpass, and the input op amp as an inverting amplifier, to provide non-inverting lowpass output. Again, this mode is useful for designing odd-ordered lowpass filters.

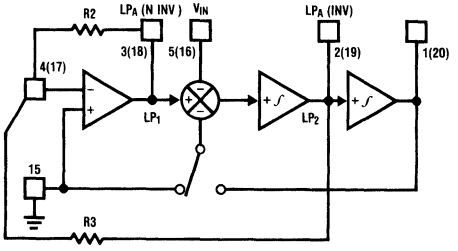
DESIGN EQUATIONS

$$f_c \text{ (cut-off frequency)} = \frac{f_{CLK}}{100}\left(\frac{R2}{R3}\right) \text{ or } \frac{f_{CLK}}{50}\left(\frac{R2}{R3}\right)$$

$$H_{OLP} \text{ (inverting output)} = -\frac{R3}{R2}$$

$$H_{OLP} \text{ (non-inverting output)} = +1$$

MODE 6B



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Some Specific Application Examples

For single-supply operation, it is important for several terminals to be biased to half supply. A single-supply design for a 4th order 1 kHz Butterworth lowpass (24 dB/octave or 80 dB/decade rolloff) is shown using Mode 1 in *Figure 5*. Note that the analog ground terminal (pin 15), the summer inputs $S1_A$ and $S1_B$ (pins 5 and 16) and the clock switching control pin (pin 12) are all biased to $V_{CC}/2$. For symmetrical split supply operation these pins would be grounded. An input coupling capacitor is optional, as it is needed only if the input signal is not also biased to $V_{CC}/2$. For a two-stage Butterworth response, both stages have the same corner frequency, hence the common clock for both sides. The resistor values shown are the nearest 5% tolerance values used to set the overall gain of the filter to unity and to set the required Q of the first stage (side A) to 0.504 and the second stage (side B) Q to 1.306 for a flat passband response.

A unique advantage of the switched capacitor design of the MF10 is illustrated in *Figure 6*. Here the MF10 serves double duty in a data acquisition system as an input filter for simple bandlimiting or anti-aliasing and, as a sample and hold to allow larger amplitude, higher frequency input signals. By gating OFF the applied clock, the switched capacitor integrators will hold the last sampled voltage value. The droop rate of the output voltage during the hold time is approximately 0.1 mV per ms.

A useful non-filtering application of the MF10 is shown in *Figure 7*. In this circuit, the MF10, together with an LM311 comparator, are used as a resonator to generate stable amplitude sine and cosine outputs without using AGC circuitry. The MF10 operates as a Q of 10 bandpass filter which will ring at its resonant frequency in response to a step input change. This ringing signal is fed to the LM311 which creates a square wave input signal to the bandpass to regenerate the oscillation. The bandpass output is the filtered fundamental frequency of a 50% duty cycle square wave. A 90° phase shifted signal of the same amplitude is available at the

Some Specific Application Examples (Continued)

lowpass output through the second integrator in the MF10. The frequency of oscillation is set by the center frequency of the filter as controlled by the clock and the 50:1/100: 1 control pin. The output amplitude is set by the peak to peak swing of the square wave input, which in this circuit is defined by the back to back diode clamps at the LM311 output.

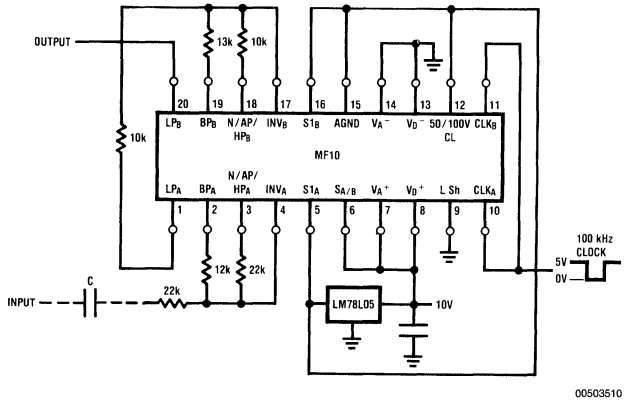


FIGURE 5. Only 6 resistors required for this 4th order, 1 kHz Butterworth lowpass filter. This example also illustrates single-supply biasing.

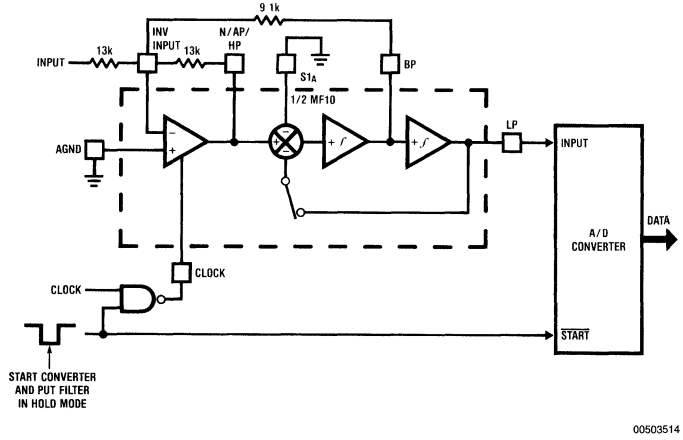


FIGURE 6. An MF10 as an Input Filter and Sample/Hold

Some Specific Application Examples (Continued)

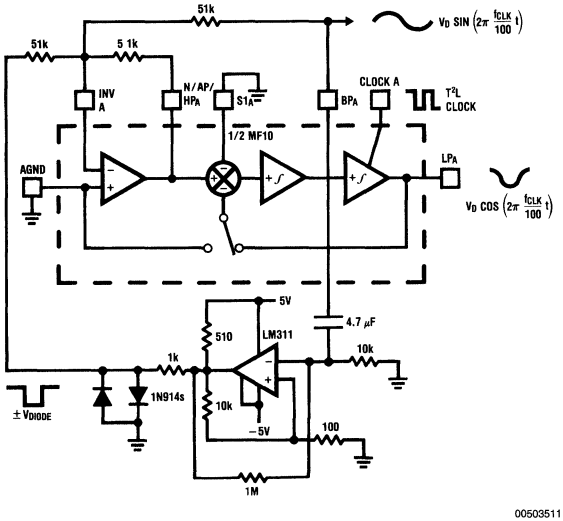


FIGURE 7. Generating Quadrature Sine Waves from a T^2L Clock

Finally, as a graphic illustration of the simplicity of filter implementation using the MF10, *Figure 8* is a complete 300 baud, full-duplex modem filter. The filter is an 8th order, 1 dB ripple Chebyshev bandpass which functions as both an 1170 Hz originate filter and a 2125 Hz answer filter. Control of answer or originate operation is set by the logic level at the 50/100/CL input so that only one clock frequency is required. The overall filter gain is 22 dB.

Construction of this filter on a printed circuit board would obviously be more compact than an RC active filter approach and much more cost effective for the level of precision required. An even more attractive implementation from a space savings point of view would be a hybrid circuit approach. A film resistor array connecting to two MF10 die could produce the entire filter in one package requiring only 7 external connections for input, output, supplies, etc.

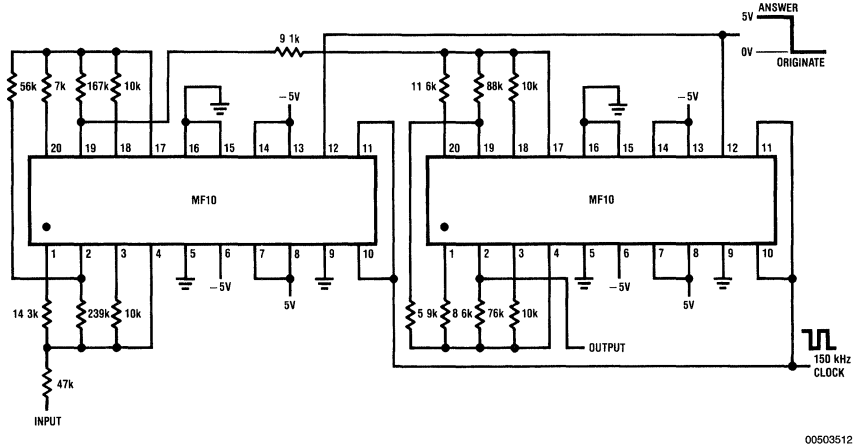


FIGURE 8. A Complete Full-Duplex 300 Baud Modem Filter

The Switched Capacitor Integrator—How it Works

The most important feature of the MF10 is that it requires no external capacitors, yet can implement filters over a wide range of frequencies. A clock is used to control the time constant of two non-inverting integrators. To feel comfortable with the operation of the MF10, it is important to understand how this control is accomplished.

It is easiest to discuss an inverting integrator (*Figure 9*) and how its input resistor can be replaced by 2 switches and a capacitor (*Figure 10*). In *Figure 9* the current which flows through feedback capacitor C is equal to V_{IN}/R and the circuit time constant is RC. This time constant accuracy depends on the absolute accuracy of two completely different discrete components. In *Figure 10*, switches S1 and S2 are alternately closed by the clock. When switch S1 is closed (S2 is opened), capacitor C1 charges up to V_{IN}. At the end of half a clock period, the charge on C1 (QC1) is equal to V_{IN}xC1. When the clock changes state, S1 opens and S2 closes. During this half of the clock period all of the charge on C1 gets transferred to the feedback capacitor C2.

The amount of charge transferred from the input, V_{IN}, to the summing junction [the (–) input] of the op amp during one complete clock period is $V_{IN}C1$. Recall that electrical current is defined as the amount of charge that passes through a conduction path during a specific time interval (1 ampere=1 coulomb per second). For this circuit, the current which flows through C2 to the output is:

$$I = \frac{\Delta Q}{\Delta t} = \frac{V_{IN}C1}{T} = V_{IN}C1\, f_{CLK}$$

where T is equal to the clock period.

The effective resistance from V_{IN} to the (–) input is therefore:

$$R = \frac{V_{IN}}{1} = \frac{1}{C1\, f_{CLK}}$$

This means that S1, S2 and C1, when clocked in *Figure 10*, act the same as the resistor in *Figure 9* to yield a clock tunable time constant of:

$$\tau = \frac{C2}{C1\, f_{CLK}}$$

Note that the time constant of the switched capacitor integrator is dependent on a *ratio* of two capacitor values, which, when fabricated on the same die, is very easy to control. This can provide precise filter resonant frequency control both from part to part and with changes in temperature.

The actual integrators used in the MF10 are non-inverting, requiring a slightly more elegant switching scheme, as shown in *Figure 11*. In this circuit, $S1_A$ and $S1_B$ are closed together to charge C1 to V_{IN}. Then $S2_A$ and $S2_B$ are closed to connect C1 to the summing junction with the capacitor plates reversed, to provide the non-inverting operation. If V_{IN} is positive, V_{OUT} will move positive as C2 acquires the charge from C1.

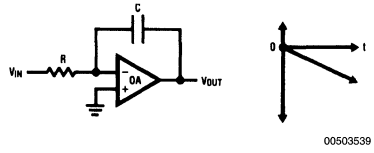


FIGURE 9.

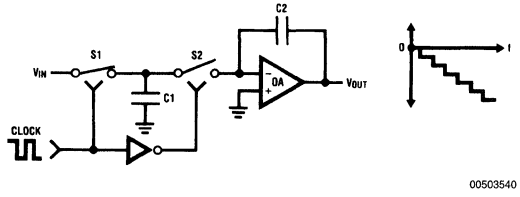


FIGURE 10.

The Switched Capacitor Integrator—How it Works (Continued)

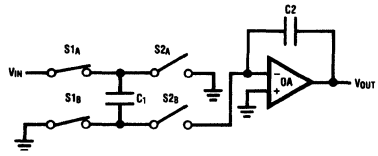


FIGURE 11. The Non-Inverting Integrator Used in the MF10

A SPICE Compatible Macromodel for CMOS Operational Amplifiers

National Semiconductor
Application Note 856
David Hindi

Abstract

A SPICE macromodel that captures the "personality" of National Semiconductor's CMOS op-amps has been developed. The salient features of the macromodel are a MOSFET input stage, Miller compensation, and a current-source output stage. A description of the model will be given along with correlation to actual device behavior.

Introduction

Recently, there has been a major thrust in lowering power dissipation and supply voltages for analog system level design. In response to this, National Semiconductor has developed a family of CMOS op-amps which feature rail-to-rail output swing, extremely low input bias current (10 fA typ.), single supply operation, low power consumption, and an input common-mode range that includes the negative supply rail [1]. Due to the unique topology that makes these features possible, a new SPICE macromodel was required in order to achieve accurate simulation results.

Macromodeling Philosophy

The philosophy used in creating this macromodel was a desire to design a model that would accurately simulate the typical behavior of a CMOS op-amp while executing much faster than a device level model (commonly referred to as a micromodel). The "personality" of an op-amp can be captured by individually hand crafting and thoroughly testing each model to ensure that it accurately simulates the behavior of the real device.

CMOS Macromodel Input Stage

The input stage performs several important functions including non-linear input transfer characteristics, offset voltage, input bias currents, second pole, and quiescent power supply current. The heart of the input stage consists of a differential amplifier which is made up of two simplified MOSFET models (see *Figure 1*) [2]. Input common-mode range can be modeled by properly setting the zero bias threshold voltage (V_{TO}) in the MOSFET model. In the case of the LMC6484, which has rail-to-rail input common-mode range, V_{TO} is left at its default value of zero Offset voltage is modeled with an ideal voltage source, E_{OS}, while input bias/offset currents are modeled by properly setting the leakage currents on the input protection diodes DP1–DP4. Quiescent current is modeled with the combination of I2 and the R8–R9 series resistors. As the supply voltage increases, the current through R8 and R9 will increase, effectively simulating that behavior in the real device. Resistors R8 and R9 also act as a voltage divider and establish a common-mode voltage (V_H) for the model directly between the rails. If the supply rails are symmetrical, i.e. ±5V, node 49 will be at 0V. Voltage-controlled voltage-source, EH, measures the voltage across R8 and subtracts an equal voltage from the positive supply rail to provide a stiff point between the rails (node 98) to which many other stages in the model are referenced. Voltage-controlled current-source G0 and resistor R0 model the gain of the input stage. The signal is then passed to the frequency shaping stages for further conditioning.

Frequency Shaping Stages

In keeping with the philosophy of providing a macromodel that is as accurate as possible, it has been determined that the model must be capable of easily accommodating as many poles and zeros that are necessary to precisely shape the magnitude and phase response of the model [3]. This is accomplished with telescopic frequency shaping stages that each have unity DC gain, making it easier to add poles and zeros without changing the low-frequency gain of the model. Each of the three types of frequency-shaping stages is shown in *Figure 1*.

Common-Mode Stage

Common-mode gain is modeled with a common-mode zero stage whose gain increases as a function of frequency. A voltage-controlled current-source, G4, is controlled with a polynomial equation which adds the voltage at each input (nodes 1 and 2) and divides the sum by two. This result is the input common-mode voltage. The DC gain of the stage is set to the reciprocal of the CMRR for the amplifier. An inductor, L2, increases the gain of the stage at 20 dB/decade to model the roll-off of CMRR that occurs in most amplifiers. The output of the common-mode zero stage (node 16) is reflected to the E_{OS} source to provide an input-referred common-mode error.

Characteristics of National Semiconductor's CMOS Operational Amplifiers

Common Characteristics	Rail-to-rail output swing, ultra-low input bias current (10 fA typ.), low drift (1.3 µV/°C), single supply operation, input common-mode range includes ground, low power consumption, and high voltage gain.
LMC660	Drives 600Ω load, high bandwidth (1.4 MHz), high slew rate (1.1 V/µs), comes in quad and dual (LMC662).
LPC660	Low power (215 µW/amp), comes in quad and dual (LPC662).
LMC6044	Low power (70 µW/amp), comes in quad, single (LMC6041) and dual (LMC6042).
LMC6062	High precision dual (V_{OS} = 100 µV), low power (80 µW/amp).
LMC6082	High precision dual (V_{OS} = 150 µV), drives 600Ω loads, high bandwidth (1.3 MHz).
LMC6484	Rail-to-rail input common-mode range, operates on 3V single supply, drives 600Ω loads, high bandwidth (1.3 MHz), comes in quad and dual (LMC6482).

Common-Mode Stage (Continued)

National's CMOS Op-Amp Macromodel

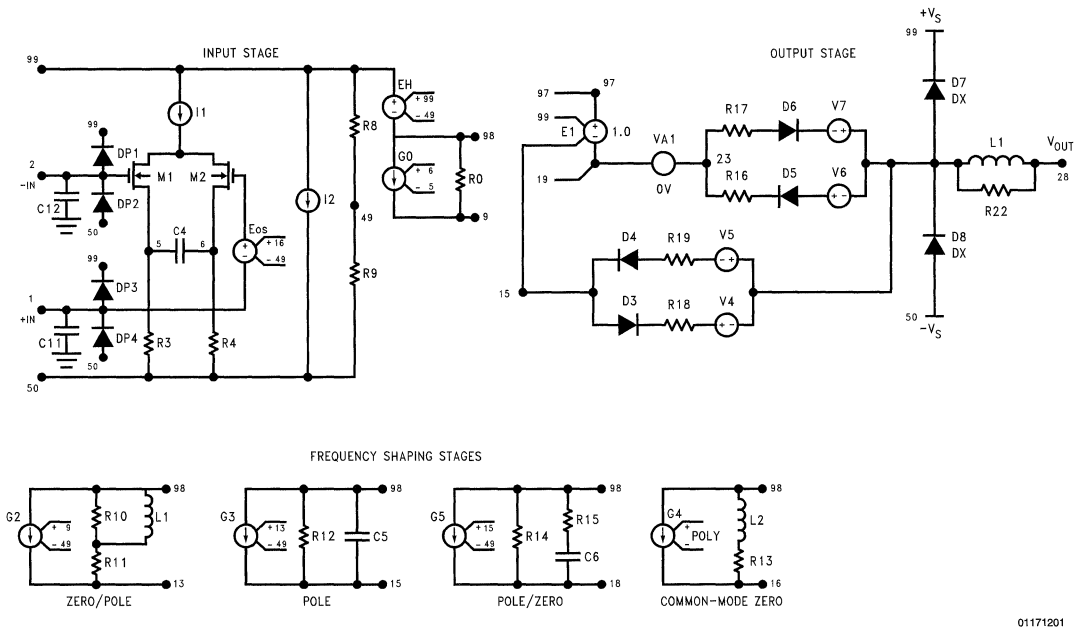


FIGURE 1.

Output Stage

After the last frequency-shaping stage, the intermediate signal is sent to the output stage. The output stage performs several important functions including dominant pole, slew rate limiting, dynamic supply current, short-circuit current limiting, the balance of the open-loop gain, output swing limiting, and output impedance. The output stage of the macromodel incorporates several new innovations in order to accommodate the unique topology of National's CMOS op-amps. To understand the unique features of this topology, a description of the actual amplifier output stage is in order.

The main feature of National's CMOS amplifiers is that the output can swing rail-to-rail. This is accomplished by removing the traditional output buffer and taking the output directly from the integrator. The output portion of the integrator is a common-source complementary push-pull gain stage which functions as a current source. Depending on load resistance, the output stage can have a considerable amount of gain. However, since the internal compensation capacitor is referenced to the output node, the slew rate does not significantly change as the output is loaded. Also, loading the output will reduce the open-loop gain of the amplifier so that the first pole will increase in frequency in order to maintain the gain-bandwidth product of the amplifier.

In the model, Miller compensation was used to obtain an additional degree of freedom in setting the open-loop gain, slew rate, and first pole. The slew rate is defined by:

$$SR = \frac{I1}{C3}$$

while the first pole is determined with the equation:

$$f_{p1} = \frac{1}{2 \times \pi \times R5 \times C3 \times (1 + A_{VOUT})}$$

where A_{VOUT} is the gain of the output stage. Note that the slew rate can be set with C3 while the first pole can be independently set with the gain of the output stage. A gain stage consisting of a voltage-controlled current-source G1 and resistor R5 takes the signal from the last frequency-shaping stage and amplifies it by the balance of the open-loop gain ($G1 \times R5 = A_{VOL} - A_{VIN} - A_{VOUT}$). A voltage clamp made of D1, V2, D2, and V3 limits the drive to the output current-source, G6, to provide short-circuit current limiting. Since the output stage has gain, output swing limiting is performed at the output node with a clamp consisting of D5, V4, D6, and V5. A resistor, R17, models the slight degradation in output swing as the amplifier is loaded.

Dynamic Supply Current

A behavior that is often not included in op-amp macromodels is dynamic supply current. If the output of the model is an ideal current source, the simulated output current of the

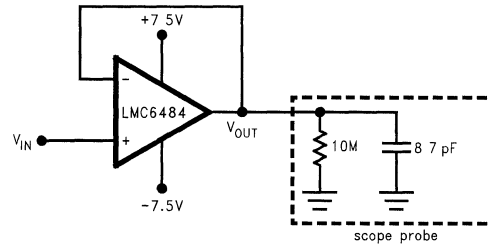
Dynamic Supply Current (Continued)

model appears to come from nowhere, i.e., the supply currents do not change. This apparent violation of the second law of thermodynamics has been solved with diodes D7–D8, current sources F5–F6, and associated circuitry. Since it is important to keep non-linear devices, such as diodes, out of the signal path, only an ideal ammeter, VA8, was inserted in the output driver to sense the sinking or sourcing of output current. Current-controlled current-source, F5, mirrors the current sensed by VA8 and forces an equal current through either D7 or D8 depending on its polarity. If current is being sourced into the load, the current flows from the positive rail through E1, VA8, and G6 to the output node and no supply current correction is necessary. However, if the output stage is sinking current from the load, the current flows from the output node up through G6, VA8 and E1 into the positive rail. To compensate for this, F5 forces an equal current through D7 and ammeter VA7. This current is then mirrored to current-source F6 which pulls an equal amount of current out of the positive rail and forces it into the negative rail. Therefore, if the output stage is sourcing current, it appears to come from the positive rail, whereas current that is sinking from the load appears to go into the negative rail. The net result of all these extra devices is an output stage which closely models the behavior of the real amplifier.

Simulation Accuracy

To ensure the accuracy of the macromodel, the simulation results are compared to lab data taken from an actual device. *Figure 2* shows a typical voltage follower transient response test circuit and *Figure 3* shows a SPICE netlist [4] for simulating the small-signal transient response of the LMC6484. Notice that the simulated response shown in *Figure 5* compares quite closely with the actual response shown in *Figure 4* with the correct amount of over-shoot and frequency of ringing.

Figures 6, 7 demonstrate the rail-to-rail input and ouput capabilities of the actual LMC6484 and the model respectively. The amplifier was configured as a voltage follower and powered from a 3V single supply. Then, a 3 V_{PP} square-wave was applied to the non-inverting input. The amplifier is clearly capable of handling this rail-to-rail input and reproducing it on the output while driving a 4.7 kΩ load. The simulation results show that the macromodel accurately models the slew rate and output swing of the amplifier.



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Note: It is very important to include a model of the scope probe on the output of the amplifier to obtain reasonable results from the simulation

FIGURE 2. Non-Inverting Amplifier (A_V = +1)

```
* LMC6484 S.S. Pulse Response. V(6)
* Cload = scope
*
XAR1 3 6 7 4 6 LMC6484
VP 7 0 7.5V
VN 4 0 -7.5V
VIN 3 0 PULSE (-.1V .1V 3U 20N 20N 5U)
Rout 6 0 10MEGohm
Cout 6 0 8.7pF
.LIB CMOSOA.LIB
.TRAN/OP .1N 10U
.PROBE
.END
```

FIGURE 3. Non-Inverting Amplifier Netlist to Simulate the Small-Signal Response of the LMC6484 [4]

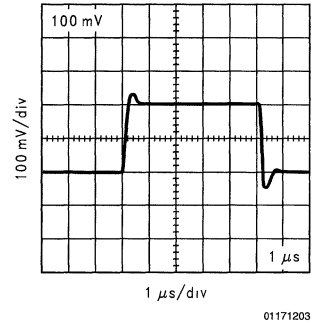

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FIGURE 4. LMC6484 Small-Signal Transient Response

Simulation Accuracy (Continued)

LMC6484 S.S. Pulse Response (V(6) C_{LOAD} = scope)

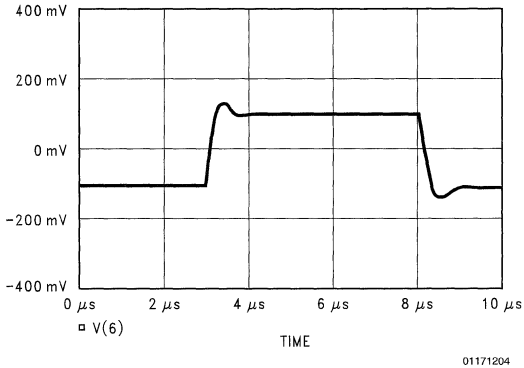
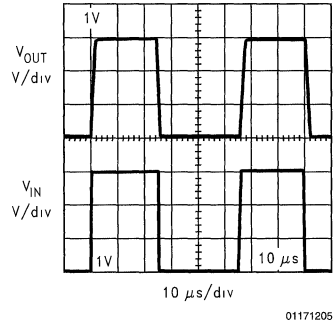


FIGURE 5. Simulated Small-Signal Transient Response



Note: This image demonstrates the rail-to-rail input/output capabilities of the LMC6484 while powered from a 3V single supply and driving a 4 7 kΩ load Don't try this with an ordinary op-amp

FIGURE 6. Large-Signal Transient Response

LMC6484 L.S. Pulse Response
(A_V = +1, V_{SUPP} = 0, +3, R1 = 4.7k)

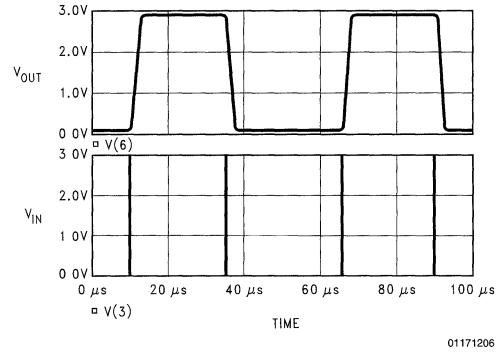


FIGURE 7. LMC6484 Simulated Large-Signal Transient Response

Conclusion

An accurate SPICE macromodel has been developed that captures the "personality" of National Semiconductor's CMOS operational amplifiers. The macromodel includes effects such as rail-to-rail output swing, input common-mode range, MOSFET input stage transfer characteristics, accurate frequency and transient response, slew rate and output short-circuit current. The model is not capable of simulating PSRR, thermal effects, or noise at this time.

Since the macromodels are much less complex and have fewer p-n junctions than a transistor level micromodel, simulation speed is much faster. For example, an LMC6484 macromodel simulation executed 34 times faster than its transistor level model. With accurate macromodels, the designer can quickly determine the dominant effects of a circuit and explore effects that are difficult to obtain with lab bench evaluation.

References

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3. Alexander, Mark: *AN-138 Spice-Compatible Op Amp Macromodels,* Precision Monolithics Inc., Application Note 138.
4. Tuinenga, Paul. *SPICE: A Guide to Circuit Simulation & Analysis Using PSpice®*, Prentice-Hall, 1992.

An IC Voltage Comparator for High Impedance Circuitry

National Semiconductor
Linear Brief 12
Robert J. Widlar

The IC voltage comparators available in the past have been designed primarily for low voltage, high speed operation. As a result, these devices have high input error currents, which limit their usefulness in high impedance circuitry. An IC is described here that drastically reduces these error currents, with only a moderate decrease in speed.

This new comparator is considerably more flexible than the older devices. Not only will it drive RTL, DTL and TTL logic; but also it can interface with MOS logic and FET analog switches. It operates from standard ±15V op amp supplies and can switch 50V, 50 mA loads, making it useful as a driver for relays, lamps or light-emitting diodes. A unique output stage enables it to drive loads referred to either supply or ground and provide ground isolation between the comparator inputs and the load.

Another useful feature of the circuit is that it can be powered from a single 5V supply and drive DTL or TTL integrated circuits. This enables the designer to perform linear functions on a digital-circuit card without using extra supplies. It can, for example, be used as a low-level photodiode detector, a zero crossing detector for magnetic transducers, an interface for high-level logic or a precision multivibrator.

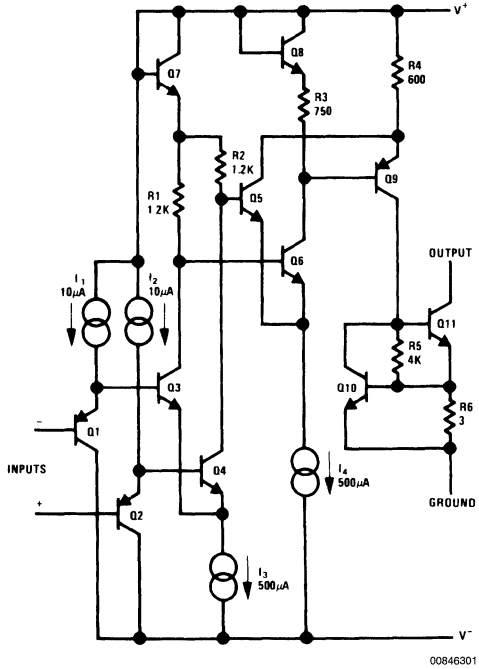


FIGURE 1. Simplified schematic of the LM111

Figure 1 shows a simplified schematic of this versatile comparator. PNP transistors buffer the differential input stage to get low input currents without sacrificing speed. Because the emitter base breakdown voltage of these PNPs is typically 70V, they can also withstand a large differential input voltage. The PNPs drive a standard differential stage. The output of this stage is further amplified by the Q_5-Q_6 pair. This feeds a lateral PNP, Q_9, that provides additional gain and drives the output stage.

The output transistor is Q_{11} which is driven by the level shifting PNP. Current limiting is provided by R_6 and Q_{10} to protect the circuit from intermittent shorts. Both the output and the ground lead are isolated from other points within the circuit, so either can be used as the output. The V^- terminal can also be tied to ground to run the circuit from a single supply. The comparator will work in any configuration as long as the ground terminal is at a potential somewhere between the supply voltages. The output terminal, however, can go above the positive supply as long as the breakdown voltage of Q_{11} is not exceeded.

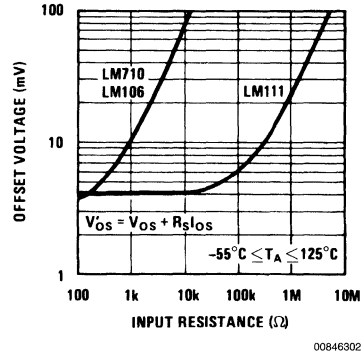


FIGURE 2. Illustrating the influence of source resistance on worst case, equivalent input offset voltage

Figure 2 shows how the reduced error currents of the LM111 improve circuit performance. With the LM710 or LM106, the offset voltage is degraded for source resistances above 200Ω. The LM111, however, works well with source resistances in excess of 30 kΩ *Figure 2* applies for equal source resistances on the two inputs. If they are unequal, the degradation will become pronounced at lower resistance levels.

Table 1 gives the important electrical characteristics of the LM111 and compares them with the specifications of older ICs.

A few, typical applications of the LM111 are illustrated in *Figure 3*. The first is a zero crossing detector driving a MOS analog switch. The ground terminal of the IC is connected to V^-; hence, with ±15V supplies, the signal swing delivered to the gate of Q_1 is also ±15V. This type of circuit is useful where the gain or feedback configuration of an op amp circuit must be changed at some precisely-determined signal level. Incidentally, it is a simple matter to modify the circuit to work with junction FETs.

TABLE 1. Comparing the LM111 with earlier IC comparators. Values given are worst case over a −55˚C to +125˚C temperature range, except as noted.

Parameter	LM111	LM106	LM710	Units
Input Offset Voltage	4	3	3	mV
Input Offset Current	0.02	7	7	μA
Input Bias Current	0.15	45	45	μA
Common Mode Range	±14	±5	±5	V
Differential Input Voltage Range	±30	±5	±5	V
Voltage Gain (Note 1)	200	40	1.7	V/mV
Response Time (Note 1)	200	40	40	ns
Output Drive				
Voltage	50	24	2.5	V
Current	50	100	1.6	mA
Fan Out (DTL/TTL)	8	16	1	
Power Consumption	80	145	160	mW

Note 1: Typical at 25˚C

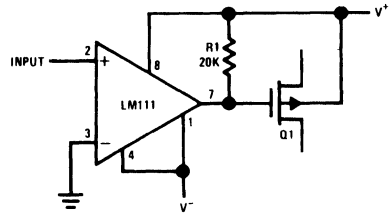
The second circuit is a zero crossing detector for a magnetic pickup such as a magnetometer or shaft-position pickoff. It delivers the output signal directly to DTL or TTL logic circuits and operates from the 5V logic supply. The resistive divider, R_1 and R_2, biases the inputs 0.5V above ground, within the common mode range of the device. An optional offset balancing circuit, R_3 and R_4, is included.

The next circuit shows a comparator for a low-level photodiode operating with MOS logic. The output changes state when the diode current reaches 1 μA. At the switching point, the voltage across the photodiode is nearly zero, so its leakage current does not cause an error. The output switches between ground and −10V, driving the data inputs of MOS logic directly.

The last circuit shows how a ground-referred load is driven from the ground terminal of the LM111. The input polarity is reversed because the ground terminal is used as the output. An incandescent lamp, which is the load here, has a cold resistance eight times lower than it is during normal operation. This produces a large inrush current, when it is switched on, that can damage the switch. However, the current limiting of the LM111 holds this current to a safe value.

The applications described above show that the output-circuit flexibility and wide supply-voltage range of the LM111 opens up new fields for IC comparators. Further, its low error currents permit its use in circuits with impedance levels above 1 kΩ. Although slower than older devices, it is more than an order of magnitude faster than op amps used as comparators.

The LM111 has the same pin configuration as the LM710 and LM106. It is interchangeable with these devices in applications where speed is not of prime concern.



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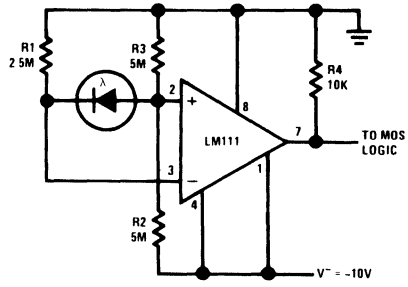
a. zero crossing detector driving analog switch



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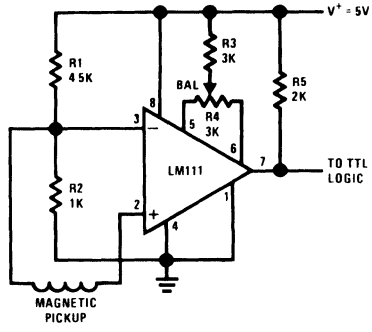
c. comparator for low level photodiode



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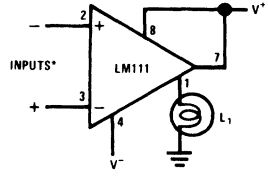
b. detector for magnetic transducer



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*Input polarity is reversed when using pin 1 as output

d. driving ground—referred load

FIGURE 3. Typical applications of the LM111

LM118
Op Amp Slews 70 V/µsec

National Semiconductor
Linear Brief 17
Robert J. Widlar

One of the greatest limitations of today's monolithic op amps is speed. With unity gain frequency compensation, general purpose op amps have 1 MHz bandwidth and 0.3 V/µs slew rate. Optimized compensation as well as feedforward compensation can improve op amp speed for some applications. Specialized devices such as fast, unity-gain buffers are available which provide partial solutions. This paper will describe a new high speed monolithic amplifier that offers an order of magnitude increase in speed with no loss in flexibility over general purpose devices.

The LM118 is constructed by the standard six mask monolithic process and features 15 MHz bandwidth and 70 V/µs slew rate. It operates over a ±5 to ±18V supply range with little change in speed. Additionally, the device has internal unity-gain frequency compensation and needs no external components for operation. However, unlike other internally compensated amplifiers, external feedforward compensation may be added to approximately double the bandwidth and slew rate.

Design Concepts

In general purpose amplifiers the unity-gain bandwidth is limited by the lateral PNP transistors used for level shifting. The response above 2 MHz is so poor that they cannot be used in a feedback amplifier. If the PNP transistors are used for level shifting only at DC or low frequencies and the signal is fed forward around the PNP transistors at high frequencies, wide bandwidth can be obtained without the excessive phase shift of the PNP transistors.

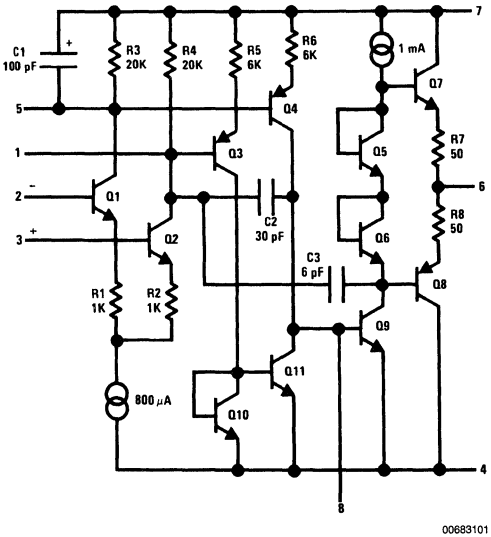


FIGURE 1. Simplified Circuit of the LM118

Figure 1 shows a simplified schematic of the LM118. Transistors Q_1 and Q_2 are a conventional differential input stage with emitter degeneration and resistive collector loads. Q_3 and Q_4 form the second stage which further amplify the signal and level shift the signal towards V^-. The collectors of Q_3 and Q_4 drive a current inverter, Q_{10} and Q_{11} to convert from differential to single ended. Q_9, which has a current source load for high gain, drives a class B output. The collectors of the input stage and the base of Q_9 are available for offset balancing and external compensation.

Frequency compensation is accomplished with three internal capacitors. C_1 rolls off on half the differential input stage so that the high frequency signal path is single-ended. Also, at high frequencies, the signal is fed forward around the lateral PNP transistors by a 30 pF capacitor, C_2. This eliminates the excessive phase shift. Overall frequency response is then set by capacitor, C_3, which rolls off the amplifier at 6 dB/octave. As previously mentioned feedforward compensation for inverting applications can be applied to the base of Q_9. *Figure 2* shows the open loop frequency response of an LM118. *Table 1* gives typical specifications for the new amplifier.

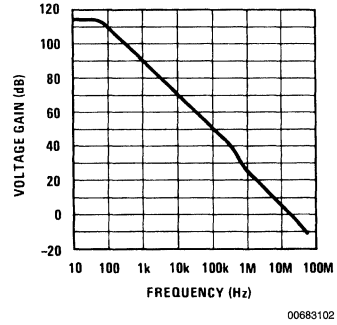


FIGURE 2. Open Loop Voltage Gain as a Function of Frequency for LM118

TABLE 1. Typical Specifications for the LM118

Input Offset Voltage	2 mV
Input Bias Current	200 nA
Offset Current	20 nA
Voltage Gain	200k
Common Mode Range	±11.5V
Output Voltage Swing	±13V
Small Signal Bandwidth	15 MHz
Slew Rate	70 V/µs

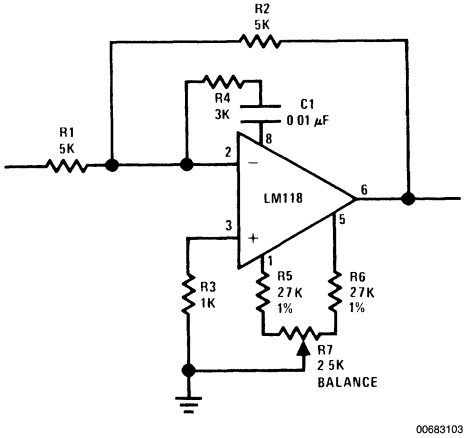
Operating Configuration

Although considerable effort was taken to make the LM118 trouble free, high frequency amplifiers are more prone to oscillations than low frequency devices such as the LM101A.

Operating Configuration (Continued)

Care must be taken to minimize the stray capacitance at the inverting input and at the output; however the LM118 will drive a 100 pF load. Good power supply bypassing is also in order—0.1 µF disc ceramic capacitors should be used within a few inches of the amplifier. Additionally, a small capacitor is usually necessary across the feedback resistor to compensate for unavoidable stray capacitance.

Figure 3 shows feedforward compensation of the LM118 for fast inverting applications. The signal is fed from the summing junction to the output stage driver by C_1 and R_4. Resistors R_5, R_6 and R_7 have two purposes: they increase the internal operating current of the output stage to increase slew rate and they provide offset balancing. The current boost is necessary to drive internal stray capacitance at the higher slew rate. Mismatch of the external resistors can cause large voltage offsets so offset balancing is necessary. For supply voltages other than ±15V, R_5 and R_6 should be selected to draw about 500 µA from Pins 1 and 5.



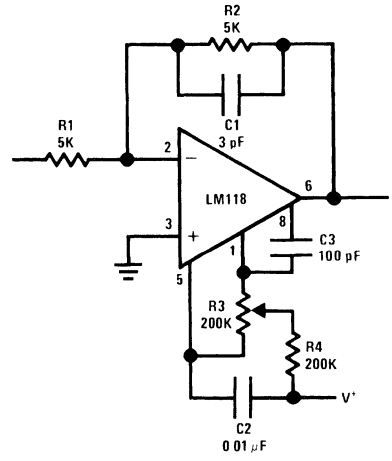
†Slew rate typically 120 V/µs

FIGURE 3. Feedforward Compensation for Greater Inverting Slew Rate†

When using feedforward resistor R_4 should be optimized for the application. It is necessary to have about 8 kΩ in the path from the output of the amplifier through the feedback resistor and through feedforward network to Pin 8 of the device. The series resistance is needed to limit the bandwidth and prevent minor loop oscillation.

At high gains, or with high value feedback resistors R_4 can be quite low—but not less than 100Ω. When the LM118 is used as a fast integrator, with a large feedback capacitor or with low values of feedback resistance, R_4 must be increased to 8 kΩ to ensure stability over a full −55°C to +125°C temperature range.

One of the more important considerations for a high speed amplifier is settling time. Poor settling time can cancel the advantages of having high slew rate and bandwidth. For example—an amplifier can have severe ringing after a step input. A relatively long time is then needed before the output voltage can be read accurately. Settling time is the time necessary for the output to slew through a defined voltage change and settle to within a defined error of its final output voltage. *Figure 4* shows optimized compensation for settling to within 0.1% error. Typically the settling time is 800 ns for a simple inverter circuit as shown. Settling time is, of course, subject to operating conditions external to the IC such as closed loop gain, circuit layout, stray capacitance and source resistance. An optional offset balancing circuit, R_3 and R_4 is included.



†Slew and settling time to 0 1% for a 10V step change is 800 ns

FIGURE 4. Compensation for Minimum Settling† Time

The LM118 opens up new fields for IC operational amplifiers It is more than an order of magnitude faster than general purpose amplifiers while retaining the ease of use features. It is ideally suited for analog to digital converters, active filters, sample and hold circuits and wide band amplification. Further, the LM118 has the same pin configuration as the LM101A or LM741 and is interchangeable with these devices when speed is of prime concern.

Specifying Selected Op Amps and Comparators

National Semiconductor
Linear Brief 26
Robert J. Widlar

It is not infrequent that commercially available standard IC components do not fit a particular application as they are specified. Often, however, a standard device selected to tighter limits will work. Thereupon, the IC manufacturer may be requested to supply a specially tested device.

The usual chain of events for a selected part is as follows: A specification is sent to the manufacturer with a request for quote. It is evaluated at the manufacturer for feasibility, yield, and testing requirements. Then price and delivery are quoted to the customer. (Sometimes this route is shortened by calling the manufacturer—but this does not always work.)

Some insight into the IC design and IC testing can help both the manufacturer and IC user with special selection. Proper specification helps the manufacturer test as well as reduce IC costs. Ambiguous or impossible specs will usually result in the return of the specification to the customer for clarification and delay the delivery of the required parts.

The manufacturer is usually familiar with the product and production spread of devices. Further, test equipment is available for measuring parameters specified by the data sheet. In general, tightening selected data sheet parameters causes no problems. Further, no additional test equipment is needed for these tests—only the limits need be changed.

Perhaps one of the largest problems is over-specification. Each tightened specification reduces the number of parts available to the specification. For example, tightening several specifications at once could result in a 1% or 0.1% yield; to supply 100 parts at this yield, between 10,000 and 100,000 parts might have to be tested, and that gets expensive.

Of course, spec limits cannot be tightened to any desired value. This is due to limitations on the IC design. For example, bias current, which depends on transistor H_{fe}; can not be tightened by a factor of 10. This would require beta's 10 times higher than normal. Also, some specifications are not independent, such as op amp bandwidth and slew-rate.

Op Amp and Comparators

These are the two most popular linear IC components requiring selection. Since many of the same specifications apply to both types of devices, they will be covered together. *Table 1* shows the most common parameters tested on these devices and the relative difficulty of testing on high speed equipment.

Selected offset voltage and drift are very commonly specified parameters. Offset voltage and drift depends on component matching. In general, drift is not usually tested on general purpose devices; although, it may be guaranteed. Offset voltage can be correlated to drift, and the offset limits are set to guarantee the standard drift specification. Of course, very low drift devices must be 100% tested for drift, making them relatively expensive. Drift testing requires measuring the offset voltage at three or more temperatures; then subtracting and dividing by the temperature change to obtain the drift—a long and tedious measurement.

In some cases tightened offset voltage specifications over the operating temperature range offer the same performance as a drift tested device, but are less expensive. This is because offset voltage measurement can be a go/no-go measurement. For example, 15 µV/°C can be guaranteed over a 100°C range by limiting the maximum offset voltage to ±0.75 mV or a 1.5 mV band. If the application has an error budget of ± "X" volts, it may be better to tighten the offset voltage rather than have the manufacturer to drift test. Drift testing a comparator is virtually impossible since they are not designed to operate closed loop.

Other parameters dependent upon matching are: offset current, common mode rejection, and supply rejections. These can be greatly tightened at the expense of yield.

Bias current, supply current, gain, slew rate, and response time are dependent upon both device design and processing. The limits for tighter parameters on these specifications are more restrictive. *Table 2* gives reasonable special selection limits. This is only a guideline and, of course, depends on the device.

Noise testing is in a class by itself. Op amp noise will vary between manufacturers of the same device. Further, noise will vary between different types of devices from the same manufacturer. Since noise on a particular device is mostly process dependent, it will be relatively consistant from a single IC producer.

Noise can be broken into two categories: white noise, and popcorn noise. Both of these noise sources can be either voltage or current noise. It is possible with advanced processing to make IC transistors as good as the best discrete low noise transistors. With good processing only a very small percentage of op amps will have any popcorn noise.

Noise measurements are time consuming and costly. Popcorn noise testing may take as much as 30 seconds per unit which limits production to about 100 devices per hour. This low production rate will increase costs. If not absolutely necessary—do not specify noise.

As a final note, some mention should be made of other special testing. Anything reasonable can be done; however, it should be kept in mind that accurate specification in terms of the IC parameters is necessary. It is unlikely a positive result will come from a specification showing a system schematic, system output, and stating "select devices to produce desired outputs." Although this is an exaggeration, it points out the type of specification to be avoided. Performance specification should apply to the IC not to a circuit using the IC. Many manufacturers have circuits available showing the various electrical tests and the way they are done.

Op Amp and Comparators (Continued)

TABLE 1. Relative Ease of Parameter Testing

Parameter	Op Amp	Comparator	Cost
Offset Voltage	Easy	Easy	Low
Offset Current	Easy	Easy	Low
Bias Current	Easy	Easy	Low
Supply Current	Easy	Easy	Low
Common Mode/Supply Rejection	Easy	Easy	Low
Gain	Moderate	Moderate	Low
Input Resistance	Guaranteed by Bias Current Measurement	Guaranteed by Bias Current Measurement	Not Tested
Slew Rate	Moderate	Moderate	Relatively Low
Bandwidth/Response Time	Difficult	Difficult	Moderate
Offset Voltage Drift	Very Difficult	Very Difficult	High
Offset Current Drift	Very Difficult	Very Difficult	High

TABLE 2. Guideline to Tightened Specifications

Parameters	Limit	Comments
Offset Voltage	0.1 mV	Matching
Offset Current	−50% of Nominal	Matching
Bias Current	−50% of Nominal	Depends on H_{fe}
Supply Current	−25% of Nominal	Depends on Various Process Parameters
Gain	+100% of Nominal	Set by Design
Common Mode/Supply Rejection	+200% of Nominal	Matching
Slew Rate	+30% of Nominal	Set by Design
Bandwidth	+30% of Nominal	Set by Design
Response Time	−30% of Nominal	Set by Design and Processing
Offset Voltage Drift	0.2 μV/°C to 5 μV/°C	Lower Limit May Not Apply to Many Op Amps
Offset Current Drift	Guarantee by Offset Current Limit	

Section 2

Amplifiers and Signal Conditioning: System Applications

Section 2 Contents

An Applications Guide for Op Amps

National Semiconductor
Application Note 20

Introduction

The general utility of the operational amplifier is derived from the fact that it is intended for use in a feedback loop whose feedback properties determine the feed-forward characteristics of the amplifier and loop combination. To suit it for this usage, the ideal operational amplifier would have infinite input impedance, zero output impedance, infinite gain and an open-loop 3 dB point at infinite frequency rolling off at 6 dB per octave. Unfortunately, the unit cost–in quantity–would also be infinite.

Intensive development of the operational amplifier, particularly in integrated form, has yielded circuits which are quite good engineering approximations of the ideal for finite cost. Quantity prices for the best contemporary integrated amplifiers are low compared with transistor prices of five years ago. The low cost and high quality of these amplifiers allows the implementation of equipment and systems functions impractical with discrete components. An example is the low frequency function generator which may use 15 to 20 operational amplifiers in generation, wave shaping, triggering and phase-locking.

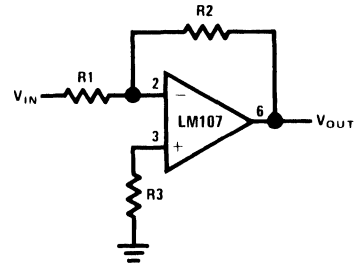
The availability of the low-cost integrated amplifier makes it mandatory that systems and equipments engineers be familiar with operational amplifier applications. This paper will present amplifier usages ranging from the simple unity-gain buffer to relatively complex generator and wave shaping circuits. The general theory of operational amplifiers is not within the scope of this paper and many excellent references are available in the literature.[1,2,3,4] The approach will be shaded toward the practical, amplifier parameters will be discussed as they affect circuit performance, and application restrictions will be outlined.

The applications discussed will be arranged in order of increasing complexity in five categories: simple amplifiers, operational circuits, transducer amplifiers, wave shapers and generators, and power supplies. The integrated amplifiers shown in the figures are for the most part internally compensated so frequency stabilization components are not shown; however, other amplifiers may be used to achieve greater operating speed in many circuits as will be shown in the text. Amplifier parameter definitions are contained in Appendix I.

The Inverting Amplifier

The basic operational amplifier circuit is shown in *Figure 1*. This circuit gives closed-loop gain of R2/R1 when this ratio is small compared with the amplifier open-loop gain and, as the name implies, is an inverting circuit. The input impedance is equal to R1. The closed-loop bandwidth is equal to the unity-gain frequency divided by one plus the closed-loop gain.

The only cautions to be observed are that R3 should be chosen to be equal to the parallel combination of R1 and R2 to minimize the offset voltage error due to bias current and that there will be an offset voltage at the amplifier output equal to closed-loop gain times the offset voltage at the amplifier input.



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$$V_{OUT} = \frac{R2}{R1} V_{IN}$$

$$R3 = R1 \parallel R2$$

For minimum error due to input bias current

FIGURE 1. Inverting Amplifier

Offset voltage at the input of an operational amplifier is comprised of two components, these components are identified in specifying the amplifier as input offset voltage and input bias current. The input offset voltage is fixed for a particular amplifier, however the contribution due to input bias current is dependent on the circuit configuration used. For minimum offset voltage at the amplifier input without circuit adjustment the source resistance for both inputs should be equal. In this case the maximum offset voltage would be the algebraic sum of amplifier offset voltage and the voltage drop across the source resistance due to offset current. Amplifier offset voltage is the predominant error term for low source resistances and offset current causes the main error for high source resistances.

In high source resistance applications, offset voltage at the amplifier output may be adjusted by adjusting the value of R3 and using the variation in voltage drop across it as an input offset voltage trim.

Offset voltage at the amplifier output is not as important in AC coupled applications. Here the only consideration is that any offset voltage at the output reduces the peak to peak linear output swing of the amplifier.

The gain-frequency characteristic of the amplifier and its feedback network must be such that oscillation does not occur. To meet this condition, the phase shift through amplifier and feedback network must never exceed 180° for any frequency where the gain of the amplifier and its feedback network is greater than unity. In practical applications, the phase shift should not approach 180° since this is the situation of conditional stability. Obviously the most critical case occurs when the attenuation of the feedback network is zero.

Amplifiers which are not internally compensated may be used to achieve increased performance in circuits where

The Inverting Amplifier (Continued)

feedback network attenuation is high. As an example, the LM101 may be operated at unity gain in the inverting amplifier circuit with a 15 pF compensating capacitor, since the feedback network has an attenuation of 6 dB, while it requires 30 pF in the non-inverting unity gain connection where the feedback network has zero attenuation. Since amplifier slew rate is dependent on compensation, the LM101 slew rate in the inverting unity gain connection will be twice that for the non-inverting connection and the inverting gain of ten connection will yield eleven times the slew rate of the non-inverting unity gain connection. The compensation trade-off for a particular connection is stability versus bandwidth, larger values of compensation capacitor yield greater stability and lower bandwidth and vice versa.

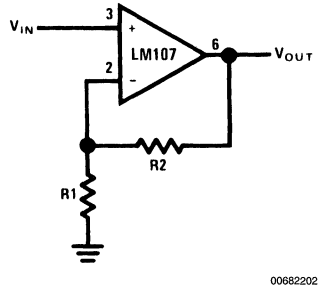
The preceding discussion of offset voltage, bias current and stability is applicable to most amplifier applications and will be referenced in later sections. A more complete treatment is contained in Reference 4.

The Non-Inverting Amplifier

Figure 2 shows a high input impedance non-inverting circuit. This circuit gives a closed-loop gain equal to the ratio of the sum of R1 and R2 to R1 and a closed-loop 3 dB bandwidth equal to the amplifier unity-gain frequency divided by the closed-loop gain.

The primary differences between this connection and the inverting circuit are that the output is not inverted and that the input impedance is very high and is equal to the differential input impedance multiplied by loop gain. (Open loop gain/Closed loop gain.) In DC coupled applications, input impedance is not as important as input current and its voltage drop across the source resistance.

Applications cautions are the same for this amplifier as for the inverting amplifier with one exception. The amplifier output will go into saturation if the input is allowed to float. This may be important if the amplifier must be switched from source to source. The compensation trade off discussed for the inverting amplifier is also valid for this connection.



$$V_{OUT} = \frac{R1 + R2}{R1} V_{IN}$$

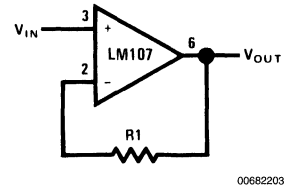
$R1 \parallel R2 = R_{SOURCE}$

For minimum error due to input bias current

FIGURE 2. Non-Inverting Amplifier

The Unity-Gain Buffer

The unity-gain buffer is shown in *Figure 3*. The circuit gives the highest input impedance of any operational amplifier circuit. Input impedance is equal to the differential input impedance multiplied by the open-loop gain, in parallel with common mode input impedance. The gain error of this circuit is equal to the reciprocal of the amplifier open-loop gain or to the common mode rejection, whichever is less.



$V_{OUT} = V_{IN}$

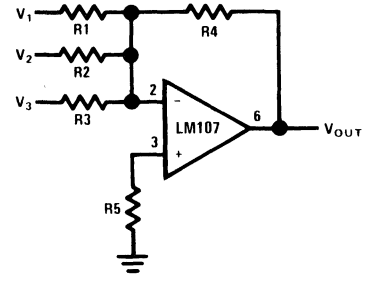
$R1 = R_{SOURCE}$

For minimum error due to input bias current

FIGURE 3. Unity Gain Buffer

Input impedance is a misleading concept in a DC coupled unity-gain buffer. Bias current for the amplifier will be supplied by the source resistance and will cause an error at the amplifier input due to its voltage drop across the source resistance. Since this is the case, a low bias current amplifier such as the LH102[6] should be chosen as a unity-gain buffer when working from high source resistances. Bias current compensation techniques are discussed in Reference 5.

The cautions to be observed in applying this circuit are three: the amplifier must be compensated for unity gain operation, the output swing of the amplifier may be limited by the amplifier common mode range, and some amplifiers exhibit a latch-up mode when the amplifier common mode range is exceeded. The LM107 may be used in this circuit with none of these problems; or, for faster operation, the LM102 may be chosen.



$$V_{OUT} = -R4\left(\frac{V_1}{R1} + \frac{V_2}{R2} + \frac{V_3}{R3}\right)$$

$R5 = R1 \parallel R2 \parallel R3 \parallel R4$

For minimum offset error due to input bias current

FIGURE 4. Summing Amplifier

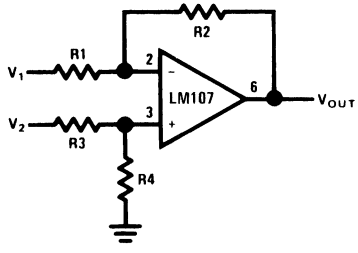
Summing Amplifier

The summing amplifier, a special case of the inverting amplifier, is shown in *Figure 4*. The circuit gives an inverted output which is equal to the weighted algebraic sum of all three inputs. The gain of any input of this circuit is equal to the ratio of the appropriate input resistor to the feedback resistor, R4. Amplifier bandwidth may be calculated as in the inverting amplifier shown in *Figure 1* by assuming the input resistor to be the parallel combination of R1, R2, and R3. Application cautions are the same as for the inverting amplifier. If an uncompensated amplifier is used, compensation is calculated on the basis of this bandwidth as is discussed in the section describing the simple inverting amplifier.

The advantage of this circuit is that there is no interaction between inputs and operations such as summing and weighted averaging are implemented very easily.

The Difference Amplifier

The difference amplifier is the complement of the summing amplifier and allows the subtraction of two voltages or, as a special case, the cancellation of a signal common to the two inputs This circuit is shown in *Figure 5* and is useful as a computational amplifier, in making a differential to single-ended conversion or in rejecting a common mode signal.



00682205

$$V_{OUT} = \left(\frac{R1 + R2}{R3 + R4}\right)\frac{R4}{R1}V_2 - \frac{R2}{R1}V_1$$

For R1 = R3 and R2 = R4

$$V_{OUT} = \frac{R2}{R1}(V_2 - V_1)$$

R1 || R2 = R3 || R4

For minimum offset error due to input bias current

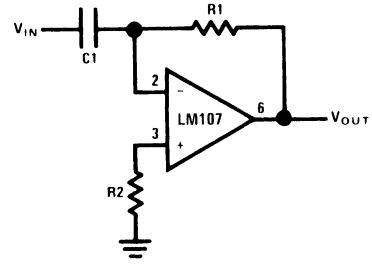
FIGURE 5. Difference Amplifier

Circuit bandwidth may be calculated in the same manner as for the inverting amplifier, but input impedance is somewhat more complicated. Input impedance for the two inputs is not necessarily equal, inverting input impedance is the same as for the inverting amplifier of *Figure 1* and the non-inverting input impedance is the sum of R3 and R4. Gain for either input is the ratio of R1 to R2 for the special case of a differential input single-ended output where R1 = R3 and R2 = R4. The general expression for gain is given in the figure. Compensation should be chosen on the basis of amplifier bandwidth.

Care must be exercised in applying this circuit since input impedances are not equal for minimum bias current error.

Differentiator

The differentiator is shown in *Figure 6* and, as the name implies, is used to perform the mathematical operation of differentiation. The form shown is not the practical form, it is a true differentiator and is extremely susceptible to high frequency noise since AC gain increases at the rate of 6 dB per octave. In addition, the feedback network of the differentiator, R1C1, is an RC low pass filter which contributes 90° phase shift to the loop and may cause stability problems even with an amplifier which is compensated for unity gain.



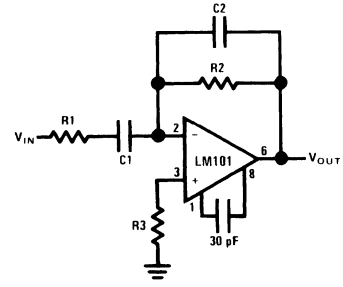
00682206

$$V_{OUT} = -R1C1\frac{d}{dt}(V_{IN})$$

R1 = R2

For minimum offset error due to input bias current

FIGURE 6. Differentiator



00682207

$$f_c = \frac{1}{2\pi R2C1}$$

$$f_h = \frac{1}{2\pi R1C1} = \frac{1}{2\pi R2C2}$$

$f_c \ll f_h \ll f_{unity\ gain}$

FIGURE 7. Practical Differentiator

A practical differentiator is shown in *Figure 7*. Here both the stability and noise problems are corrected by addition of two additional components, R1 and C2. R2 and C2 form a 6 dB per octave high frequency roll-off in the feedback network and R1C1 form a 6 dB per octave roll-off network in the input network for a total high frequency roll-off of 12 dB per octave to reduce the effect of high frequency input and amplifier noise. In addition R1C1 and R2C2 form lead networks in the

Differentiator (Continued)

feedback loop which, if placed below the amplifier unity gain frequency, provide 90° phase lead to compensate the 90° phase lag of R2C1 and prevent loop instability. A gain frequency plot is shown in *Figure 8* for clarity.

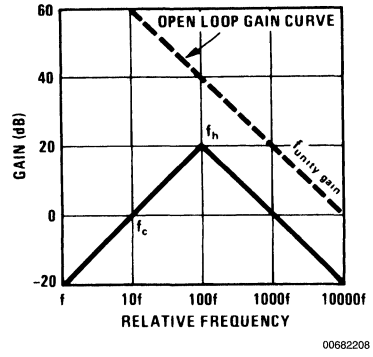
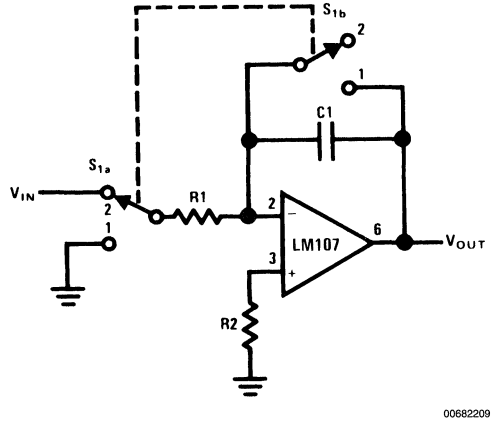


FIGURE 8. Differentiator Frequency Response

Integrator

The integrator is shown in *Figure 9* and performs the mathematical operation of integration. This circuit is essentially a low-pass filter with a frequency response decreasing at 6 dB per octave. An amplitude-frequency plot is shown in *Figure 10*.



$$V_{OUT} = \frac{1}{R1C1}\int_{t_1}^{t_2} V_{IN}\,dt$$

$$f_c = \frac{1}{2\pi R1C1}$$

$$R1 = R2$$

For minimum offset error due to input bias current

FIGURE 9. Integrator

Integrator (Continued)

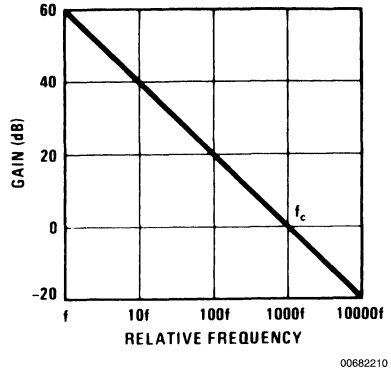


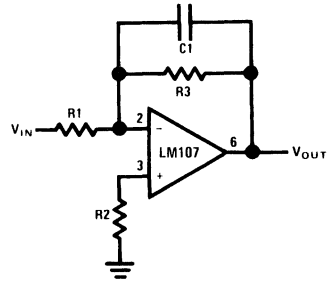
FIGURE 10. Integrator Frequency Response

The circuit must be provided with an external method of establishing initial conditions. This is shown in the figure as S_1. When S_1 is in position 1, the amplifier is connected in unity-gain and capacitor C1 is discharged, setting an initial condition of zero volts. When S_1 is in position 2, the amplifier is connected as an integrator and its output will change in accordance with a constant times the time integral of the input voltage.

The cautions to be observed with this circuit are two: the amplifier used should generally be stabilized for unity-gain operation and R2 must equal R1 for minimum error due to bias current.

Simple Low-pass Filter

The simple low-pass filter is shown in *Figure 11*. This circuit has a 6 dB per octave roll-off after a closed-loop 3 dB point defined by f_c. Gain below this corner frequency is defined by the ratio of R3 to R1. The circuit may be considered as an AC integrator at frequencies well above f_c; however, the time domain response is that of a single RC rather than an integral.



$$f_L = \frac{1}{2\pi R1C1}$$

$$f_c = \frac{1}{2\pi R3C1}$$

$$A_L = \frac{R3}{R1}$$

FIGURE 11. Simple Low Pass Filter

R2 should be chosen equal to the parallel combination of R1 and R3 to minimize errors due to bias current. The amplifier should be compensated for unity-gain or an internally compensated amplifier can be used.

Simple Low-pass Filter (Continued)

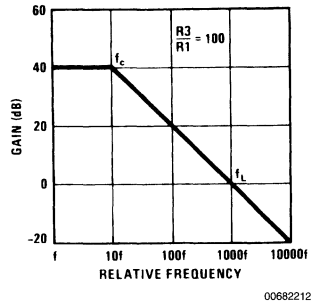


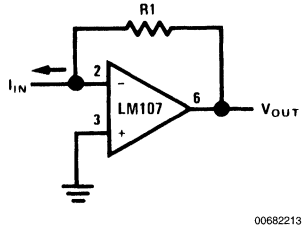
FIGURE 12. Low Pass Filter Response

A gain frequency plot of circuit response is shown in *Figure 12* to illustrate the difference between this circuit and the true integrator.

The Current-to-Voltage Converter

Current may be measured in two ways with an operational amplifier. The current may be converted into a voltage with a resistor and then amplified or the current may be injected directly into a summing node. Converting into voltage is undesirable for two reasons: first, an impedance is inserted into the measuring line causing an error; second, amplifier offset voltage is also amplified with a subsequent loss of accuracy. The use of a current-to-voltage transducer avoids both of these problems.

The current-to-voltage transducer is shown in *Figure 13*. The input current is fed directly into the summing node and the amplifier output voltage changes to extract the same current from the summing node through R1. The scale factor of this circuit is R1 volts per amp. The only conversion error in this circuit is I_{bias} which is summed algebraically with I_{IN}.



$V_{OUT} = I_{IN}\ R1$

FIGURE 13. Current to Voltage Converter

This basic circuit is useful for many applications other than current measurement. It is shown as a photocell amplifier in the following section.

The only design constraints are that scale factors must be chosen to minimize errors due to bias current and since voltage gain and source impedance are often indeterminate (as with photocells) the amplifier must be compensated for unity-gain operation. Valuable techniques for bias current compensation are contained in Reference 5.

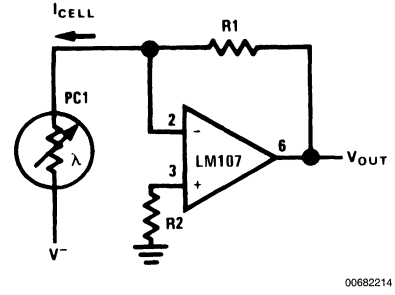
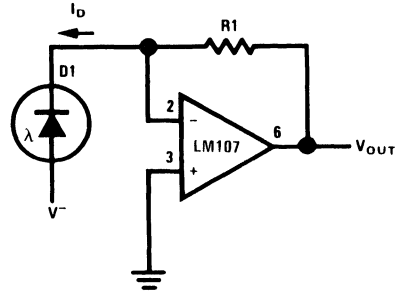


FIGURE 14. Amplifier for Photoconductive Cell

Photocell Amplifiers

Amplifiers for photoconductive, photodiode and photovoltaic cells are shown in *Figures 14, 15, 16* respectively.

All photogenerators display some voltage dependence of both speed and linearity. It is obvious that the current through a photoconductive cell will not display strict proportionality to incident light if the cell terminal voltage is allowed to vary with cell conductance. Somewhat less obvious is the fact that photodiode leakage and photovoltaic cell internal losses are also functions of terminal voltage. The current-to-voltage converter neatly sidesteps gross linearity problems by fixing a constant terminal voltage, zero in the case of photovoltaic cells and a fixed bias voltage in the case of photoconductors or photodiodes.

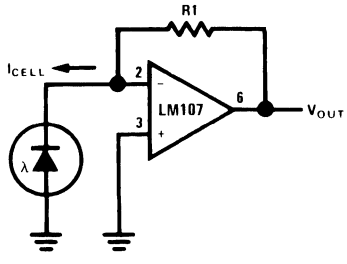


$V_{OUT} = R1\ I_D$

FIGURE 15. Photodiode Amplifier

Photocell Amplifiers (Continued)

Photodetector speed is optimized by operating into a fixed low load impedance. Currently available photovoltaic detectors show response times in the microsecond range at zero load impedance and photoconductors, even though slow, are materially faster at low load resistances.



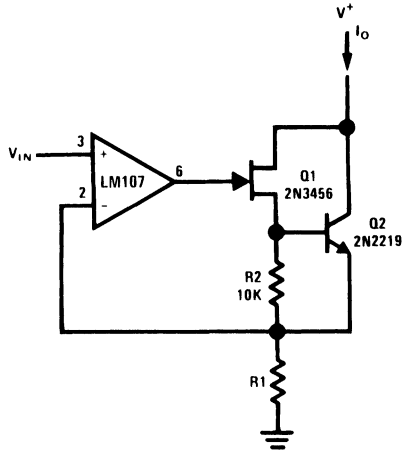
$V_{OUT} = I_{CELL}$ R1

FIGURE 16. Photovoltaic Cell Amplifier

The feedback resistance, R1, is dependent on cell sensitivity and should be chosen for either maximum dynamic range or for a desired scale factor. R2 is elective: in the case of photovoltaic cells or of photodiodes, it is not required in the case of photoconductive cells, it should be chosen to minimize bias current error over the operating range.

Precision Current Source

The precision current source is shown in *Figures 17, 18.* The configurations shown will sink or source conventional current respectively.



$$I_O = \frac{V_{IN}}{R1}$$

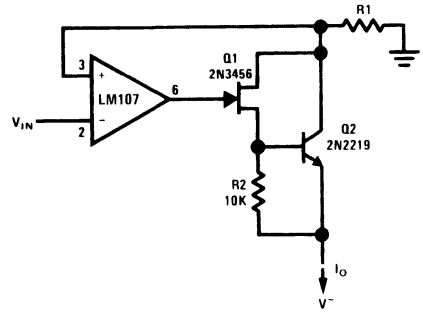
$V_{IN} \geq 0V$

FIGURE 17. Precision Current Sink

Caution must be exercised in applying these circuits. The voltage compliance of the source extends from BV_{CER} of the external transistor to approximately 1 volt more negative than V_{IN}. The compliance of the current sink is the same in the positive direction.

The impedance of these current generators is essentially infinite for small currents and they are accurate so long as V_{IN} is much greater than V_{OS} and I_O is much greater than I bias.

The source and sink illustrated in *Figures 17, 18* use an FET to drive a bipolar output transistor. It is possible to use a Darlington connection in place of the FET-bipolar combination in cases where the output current is high and the base current of the Darlington input would not cause a significant error.



$$I_O = \frac{V_{IN}}{R1}$$

$V_{IN} \leq 0V$

FIGURE 18. Precision Current Source

The amplifiers used must be compensated for unity-gain and additional compensation may be required depending on load reactance and external transistor parameters.

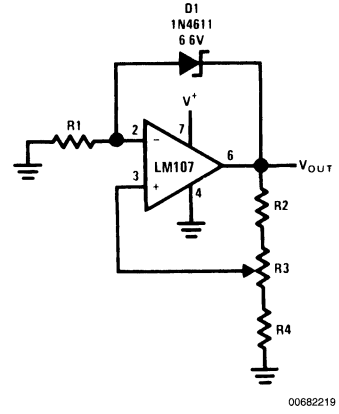


FIGURE 19. Positive Voltage Reference

Adjustable Voltage References

Adjustable voltage reference circuits are shown in *Figures 19, 20, 21, 22.* The two circuits shown have different areas of applicability. The basic difference between the two is that *Figures 19, 20* illustrate a voltage source which provides a voltage greater than the reference diode while *Figures 21, 22* illustrates a voltage source which provides a voltage lower than the reference diode. The figures show both positive and negative voltage sources.

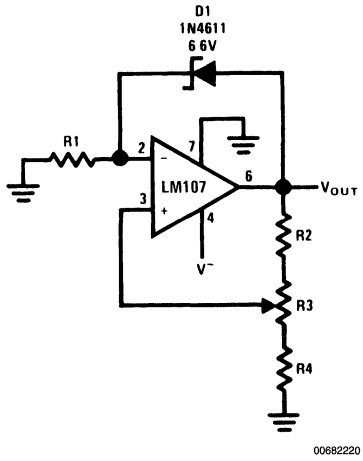


FIGURE 20. Negative Voltage Reference

High precision extended temperature applications of the circuit of *Figures 19, 20* require that the range of adjustment of V_{OUT} be restricted. When this is done, R1 may be chosen to provide optimum zener current for minimum zener T.C. Since I_Z is not a function of V^+, reference T.C. will be independent of V^+.

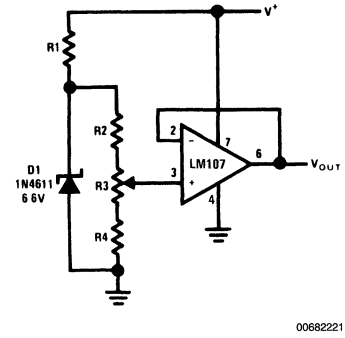


FIGURE 21. Positive Voltage Reference

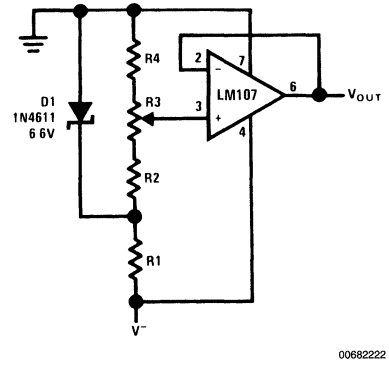


FIGURE 22. Negative Voltage Reference

The circuit of *Figures 21, 22* are suited for high precision extended temperature service if V^+ is reasonably constant since I_Z is dependent on V^+. R1, R2, R3, and R4 are chosen to provide the proper I_Z for minimum T.C. and to minimize errors due to I_{bias}.

The circuits shown should both be compensated for unity-gain operation or, if large capacitive loads are expected, should be overcompensated. Output noise may be reduced in both circuits by bypassing the amplifier input.

The circuits shown employ a single power supply, this requires that common mode range be considered in choosing an amplifier for these applications. If the common mode range requirements are in excess of the capability of the amplifier, two power supplies may be used. The LH101 may be used with a single power supply since the common mode range is from V^+ to within approximately 2 volts of V^-.

The Reset Stabilized Amplifier

The reset stabilized amplifier is a form of chopper-stabilized amplifier and is shown in *Figure 23.* As shown, the amplifier is operated closed-loop with a gain of one.

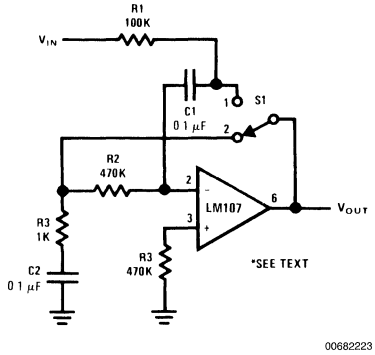
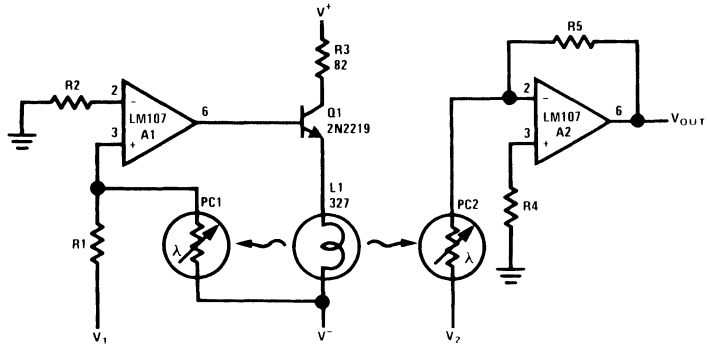


FIGURE 23. Reset Stabilized Amplifier

The connection is useful in eliminating errors due to offset voltage and bias current. The output of this circuit is a pulse whose amplitude is equal to V_{IN}. Operation may be understood by considering the two conditions corresponding to the position of S_1. When S_1 is in position 2, the amplifier is connected in the unity gain connection and the voltage at the output will be equal to the sum of the input offset voltage and the drop across R2 due to input bias current The voltage at the inverting input will be equal to input offset voltage. Capacitor C1 will charge to the sum of input offset voltage and V_{IN} through R1. When C1 is charged, no current flows through the source resistance and R1 so there is no error due to input resistance S_1 is then changed to position 1. The voltage stored on C1 is inserted between the output and inverting input of the amplifier and the output of the amplifier changes by V_{IN} to maintain the amplifier input at the input offset voltage. The output then changes from (V_{OS} + I_{bias}R2) to (V_{IN} + I_{bias}R2) as S_1 is changed from position 2 to position 1 Amplifier bias current is supplied through R2 from the output of the amplifier or from C2 when S_1 is in position 2 and position 1 respectively. R3 serves to reduce the offset at the amplifier output if the amplifier must have maximum linear range or if it is desired to DC couple the amplifier.

An additional advantage of this connection is that input resistance approaches infinity as the capacitor C1 approaches full charge, eliminating errors due to loading of the source resistance. The time spent in position 2 should be long with respect to the charging time of C1 for maximum accuracy.

The amplifier used must be compensated for unity gain operation and it may be necessary to overcompensate because of the phase shift across R2 due to C1 and the amplifier input capacity. Since this connection is usually used at very low switching speeds, slew rate is not normally a practical consideration and overcompensation does not reduce accuracy.



$$R5 = R1\left(\frac{V-}{10}\right)$$

$$V_1 > 0$$

$$V_{OUT} = \frac{V_1 V_2}{10}$$

FIGURE 24. Analog Multiplier

The Analog Multiplier

A simple embodiment of the analog multiplier is shown in *Figure 24.* This circuit circumvents many of the problems associated with the log-antilog circuit and provides three quadrant analog multiplication which is relatively temperature insensitive and which is not subject to the bias current errors which plague most multipliers.

The Analog Multiplier (Continued)

Circuit operation may be understood by considering A2 as a controlled gain amplifier, amplifying V_2, whose gain is dependent on the ratio of the resistance of PC2 to R5 and by considering A1 as a control amplifier which establishes the resistance of PC2 as a function of V_1. In this way it is seen that V_{OUT} is a function of both V_1 and V_2.

A1, the control amplifier, provides drive for the lamp, L1. When an input voltage, V_1, is present, L1 is driven by A1 until the current to the summing junction from the negative supply through PC1 is equal to the current to the summing junction from V_1 through R1. Since the negative supply voltage is fixed, this forces the resistance of PC1 to a value proportional to R1 and to the ratio of V_1 to V^-. L1 also illuminates PC2 and, if the photoconductors are matched, causes PC2 to have a resistance equal to PC1.

A2, the controlled gain amplifier, acts as an inverting amplifier whose gain is equal to the ratio of the resistance of PC2 to R5. If R5 is chosen equal to the product of R1 and V^-, then V_{OUT} becomes simply the product of V_1 and V_2. R5 may be scaled in powers of ten to provide any required output scale factor.

PC1 and PC2 should be matched for best tracking over temperature since the T.C. of resistance is related to resistance match for cells of the same geometry. Small mismatches may be compensated by varying the value of R5 as a scale factor adjustment. The photoconductive cells should receive equal illumination from L1, a convenient method is to mount the cells in holes in an aluminum block and to mount the lamp midway between them. This mounting method provides controlled spacing and also provides a thermal bridge between the two cells to reduce differences in cell temperature. This technique may be extended to the use of FET's or other devices to meet special resistance or environment requirements.

The circuit as shown gives an inverting output whose magnitude is equal to one-tenth the product of the two analog inputs. Input V_1 is restricted to positive values, but V_2 may assume both positive and negative values. This circuit is restricted to low frequency operation by the lamp time constant.

R2 and R4 are chosen to minimize errors due to input offset current as outlined in the section describing the photocell amplifier. R3 is included to reduce in-rush current when first turning on the lamp, L1.

The Full-Wave Rectifier and Averaging Filter

The circuit shown in *Figure 25* is the heart of an average reading, rms calibrated AC voltmeter. As shown, it is a rectifier and averaging filter. Deletion of C2 removes the averaging function and provides a precision full-wave rectifier, and deletion of C1 provides an absolute value generator.

Circuit operation may be understood by following the signal path for negative and then for positive inputs. For negative signals, the output of amplifier A1 is clamped to +0.7V by D1 and disconnected from the summing point of A2 by D2. A2 then functions as a simple unity-gain inverter with input resistor, R1, and feedback resistor, R2, giving a positive going output.

For positive inputs, A1 operates as a normal amplifier connected to the A2 summing point through resistor, R5. Amplifier A1 then acts as a simple unity-gain inverter with input resistor, R3, and feedback resistor, R5. A1 gain accuracy is not affected by D2 since it is inside the feedback loop. Positive current enters the A2 summing point through resistor, R1, and negative current is drawn from the A2 summing point through resistor, R5. Since the voltages across R1 and R5 are equal and opposite, and R5 is one-half the value of R1, the net input current at the A2 summing point is equal to and opposite from the current through R1 and amplifier A2 operates as a summing inverter with unity gain, again giving a positive output.

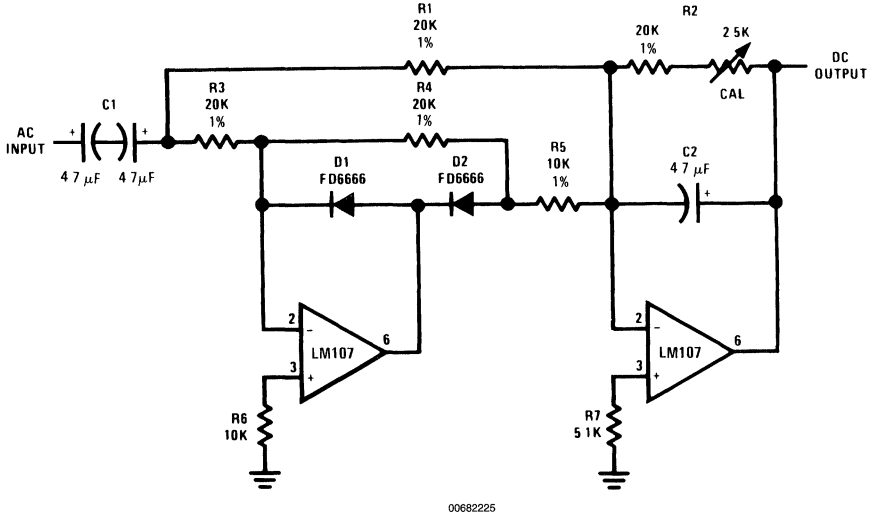


FIGURE 25. Full-Wave Rectifier and Averaging Filter

The Full-Wave Rectifier and Averaging Filter (Continued)

The circuit becomes an averaging filter when C2 is connected across R2. Operation of A2 then is similar to the Simple Low Pass Filter previously described. The time constant R2C2 should be chosen to be much larger than the maximum period of the input voltage which is to be averaged.

Capacitor C1 may be deleted if the circuit is to be used as an absolute value generator. When this is done, the circuit output will be the positive absolute value of the input voltage.

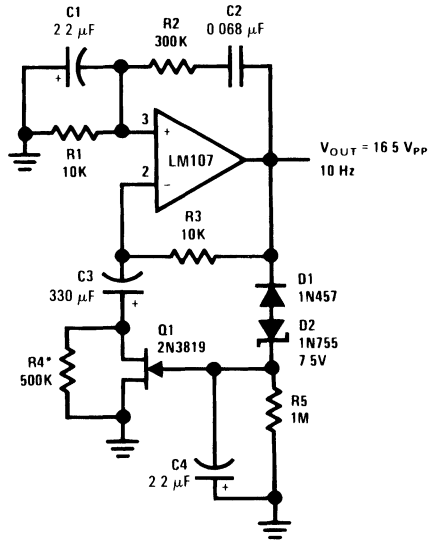
The amplifiers chosen must be compensated for unity-gain operation and R6 and R7 must be chosen to minimize output errors due to input offset current.

Sine Wave Oscillator

An amplitude-stabilized sine-wave oscillator is shown in *Figure 26.* This circuit provides high purity sine-wave output down to low frequencies with minimum circuit complexity. An important advantage of this circuit is that the traditional tungsten filament lamp amplitude regulator is eliminated along with its time constant and linearity problems.

In addition, the reliability problems associated with a lamp are eliminated.

The Wien Bridge oscillator is widely used and takes advantage of the fact that the phase of the voltage across the parallel branch of a series and a parallel RC network connected in series, is the same as the phase of the applied voltage across the two networks at one particular frequency and that the phase lags with increasing frequency and leads with decreasing frequency. When this network—the Wien Bridge—is used as a positive feedback element around an amplifier, oscillation occurs at the frequency at which the phase shift is zero. Additional negative feedback is provided to set loop gain to unity at the oscillation frequency, to stabilize the frequency of oscillation, and to reduce harmonic distortion.



*See Text

FIGURE 26. Wien Bridge Sine Wave Oscillator

The circuit presented here differs from the classic usage only in the form of the negative feedback stabilization scheme. Circuit operation is as follows: negative peaks in excess of −8.25V cause D1 and D2 to conduct, charging C4. The charge stored in C4 provides bias to Q1, which determines amplifier gain. C3 is a low frequency roll-off capacitor in the feedback network and prevents offset voltage and offset current errors from being multiplied by amplifier gain.

Distortion is determined by amplifier open-loop gain and by the response time of the negative feedback loop filter, R5 and C4. A trade-off is necessary in determining amplitude stabilization time constant and oscillator distortion. R4 is chosen to adjust the negative feedback loop so that the FET is operated at a small negative gate bias. The circuit shown provides optimum values for a general purpose oscillator.

Triangle-Wave Generator

A constant amplitude triangular-wave generator is shown in *Figure 27*. This circuit provides a variable frequency triangular wave whose amplitude is independent of frequency.

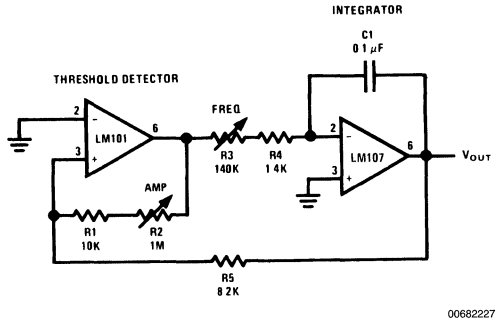


FIGURE 27. Triangular-Wave Generator

The generator embodies an integrator as a ramp generator and a threshold detector with hysterisis as a reset circuit. The integrator has been described in a previous section and requires no further explanation. The threshold detector is similar to a Schmitt Trigger in that it is a latch circuit with a large dead zone. This function is implemented by using positive feedback around an operational amplifier. When the amplifier output is in either the positive or negative saturated state, the positive feedback network provides a voltage at the non-inverting input which is determined by the attenuation of the feedback loop and the saturation voltage of the amplifier. To cause the amplifier to change states, the voltage at the input of the amplifier must be caused to change polarity by an amount in excess of the amplifier input offset voltage. When this is done the amplifier saturates in the opposite direction and remains in that state until the voltage at its input again reverses. The complete circuit operation may be understood by examining the operation with the output of the threshold detector in the positive state. The detector positive saturation voltage is applied to the integrator summing junction through the combination R3 and R4 causing a current I^+ to flow.

The integrator then generates a negative-going ramp with a rate of $I^+/C1$ volts per second until its output equals the negative trip point of the threshold detector. The threshold detector then changes to the negative output state and supplies a negative current, I^-, at the integrator summing point. The integrator now generates a positive-going ramp with a rate of $I^-/C1$ volts per second until its output equals the positive trip point of the threshold detector where the detector again changes output state and the cycle repeats.

Triangular-wave frequency is determined by R3, R4 and C1 and the positive and negative saturation voltages of the amplifier A1. Amplitude is determined by the ratio of R5 to the combination of R1 and R2 and the threshold detector saturation voltages. Positive and negative ramp rates are equal and positive and negative peaks are equal if the detector has equal positive and negative saturation voltages. The output waveform may be offset with respect to ground if the inverting input of the threshold detector, A1, is offset with respect to ground.

The generator may be made independent of temperature and supply voltage if the detector is clamped with matched zener diodes as shown in *Figure 28*.

The integrator should be compensated for unity-gain and the detector may be compensated if power supply impedance causes oscillation during its transition time. The current into the integrator should be large with respect to I_{bias} for maximum symmetry, and offset voltage should be small with respect to V_{OUT} peak.

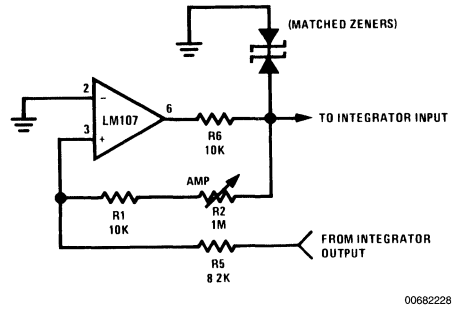
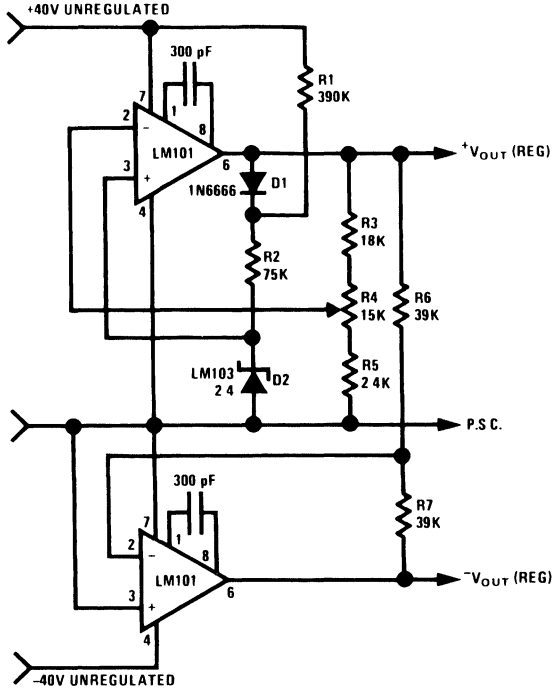


FIGURE 28. Threshold Detector with Regulated Output

Tracking Regulated Power Supply

A tracking regulated power supply is shown in *Figure 29*. This supply is very suitable for powering an operational amplifier system since positive and negative voltages track, eliminating common mode signals originating in the supply voltage. In addition, only one voltage reference and a minimum number of passive components are required.

Tracking Regulated Power Supply (Continued)



Output voltage is variable from ±5V to ±35V

Negative output tracks positive output to within the ratio of R6 to R7

FIGURE 29. Tracking Power Supply

Power supply operation may be understood by considering first the positive regulator. The positive regulator compares the voltage at the wiper of R4 to the voltage reference, D2. The difference between these two voltages is the input voltage for the amplifier and since R3, R4, and R5 form a negative feedback loop, the amplifier output voltage changes in such a way as to minimize this difference. The voltage reference current is supplied from the amplifier output to increase power supply line regulation. This allows the regulator to operate from supplies with large ripple voltages. Regulating the reference current in this way requires a separate source of current for supply start-up. Resistor R1 and diode D1 provide this start-up current. D1 decouples the reference string from the amplifier output during start-up and R1 supplies the start-up current from the unregulated positive supply. After start-up, the low amplifier output impedance reduces reference current variations due to the current through R1.

The negative regulator is simply a unity-gain inverter with input resistor, R6, and feedback resistor, R7.

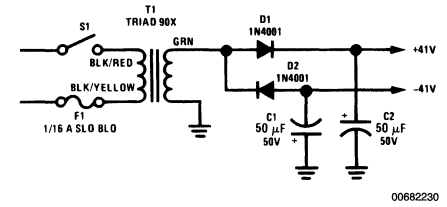
The amplifiers must be compensated for unity-gain operation.

The power supply may be modulated by injecting current into the wiper of R4. In this case, the output voltage variations will be equal and opposite at the positive and negative outputs. The power supply voltage may be controlled by replacing D1, D2, R1 and R2 with a variable voltage reference.

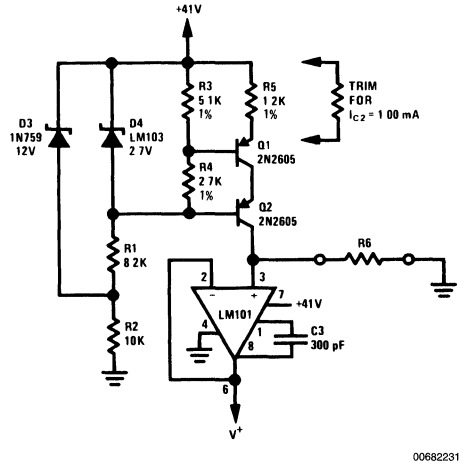
Programmable Bench Power Supply

The complete power supply shown in *Figure 30* is a programmable positive and negative power supply. The regulator section of the supply comprises two voltage followers whose input is provided by the voltage drop across a reference resistor of a precision current source.

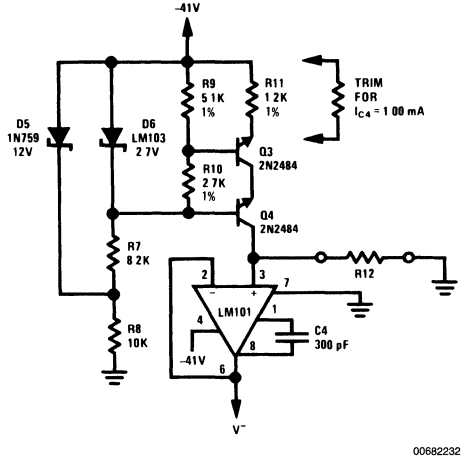
Programmable Bench Power Supply (Continued)



a.



b.



c.

FIGURE 30. Low-Power Supply for Integrated Circuit Testing

Programming sensitivity of the positive and negative supply is 1V/1000Ω of resistors R6 and R12 respectively. The output voltage of the positive regulator may be varied from approximately +2V to +38V with respect to ground and the negative regulator output voltage may be varied from −38V to 0V with respect to ground. Since LM107 amplifiers are

Programmable Bench Power Supply (Continued)

used, the supplies are inherently short circuit proof. This current limiting feature also serves to protect a test circuit if this supply is used in integrated circuit testing.

Internally compensated amplifiers may be used in this application if the expected capacitive loading is small. If large capacitive loads are expected, an externally compensated amplifier should be used and the amplifier should be overcompensated for additional stability. Power supply noise may be reduced by bypassing the amplifier inputs to ground with capacitors in the 0.1 to 1 0 µF range

Conclusions

The foregoing circuits are illustrative of the versatility of the integrated operational amplifier and provide a guide to a number of useful applications. The cautions noted in each section will show the more common pitfalls encountered in amplifier usage.

Appendix I

Definition of Terms

Input Offset Voltage: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

Input Offset Current: The difference in the currents into the two input terminals when the output is at zero.

Input Bias Current: The average of the two input currents.

Input Voltage Range: The range of voltages on the input terminals for which the amplifier operates within specifications.

Common Mode Rejection Ratio: The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output at zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Power Supply Rejection: The ratio of the change in input offset voltage to change in power supply voltage producing it.

Slew Rate: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

References

1. D.C. Amplifier Stabilized for Zero and Gain; Williams, Tapley, and Clark; AIEE Transactions, Vol. 67, 1948.
2. Active Network Synthesis; K. L. Su, McGraw-Hill Book Co., Inc., New York, New York.
3. Analog Computation; A. S. Jackson, McGraw-Hill Book Co., Inc., New York, New York
4. A Palimpsest on the Electronic Analog Art; H. M. Paynter, Editor. Published by George A. Philbrick Researches, Inc., Boston, Mass.
5. Drift Compensation Techniques for Integrated D.C. Amplifiers; R. J. Widlar, EDN, June 10, 1968.
6. A Fast Integrated Voltage Follower With Low Input Current; R J. Widlar, Microelectronics, Vol. 1 No. 7, June 1968.

Log Converters

National Semiconductor
Application Note 30

Note: National Semiconductor recommends replacing 2N2920 and 2N3728 matched pairs with LM394 in all application circuits.

One of the most predictable non-linear elements commonly available is the bipolar transistor. The relationship between collector current and emitter base voltage is precisely logarithmic from currents below one picoamp to currents above one milliamp. Using a matched pair of transistors and integrated circuit operational amplifiers, it is relatively easy to construct a linear to logarithmic converter with a dynamic range in excess of five decades.

The circuit in *Figure 1* generates a logarithmic output voltage for a linear input current. Transistor Q_1 is used as the non-linear feedback element around an LM108 operational amplifier. Negative feedback is applied to the emitter of Q_1 through divider, R_1 and R_2, and the emitter base junction of Q_2. This forces the collector current of Q_1 to be exactly equal to the current through the input resistor. Transistor Q_2 is used as the feedback element of an LM101A operational amplifier. Negative feedback forces the collector current of Q_2 to equal the current through R_3. For the values shown, this current is 10 µA. Since the collector current of Q_2 remains constant, the emitter base voltage also remains constant. Therefore, only the V_{BE} of Q_1 varies with a change of input current. However, the output voltage is a function of the difference in emitter base voltages of Q_1 and Q_2:

$$E_{OUT} = \frac{R_1 + R_2}{R_2}(V_{BE_2} - V_{BE_1}). \quad (1)$$

For matched transistors operating at different collector currents, the emitter base differential is given by

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{C_1}}{I_{C_2}}, \quad (2)$$

where k is Boltzmann's constant, T is temperature in degrees Kelvin and q is the charge of an electron. Combining these two equations and writing the expression for the output voltage gives

$$E_{OUT} = \frac{-kT}{q}\left[\frac{R_1 + R_2}{R_2}\right] \log_e \left[\frac{E_{IN} R_3}{E_{REF} R_{IN}}\right] \quad (3)$$

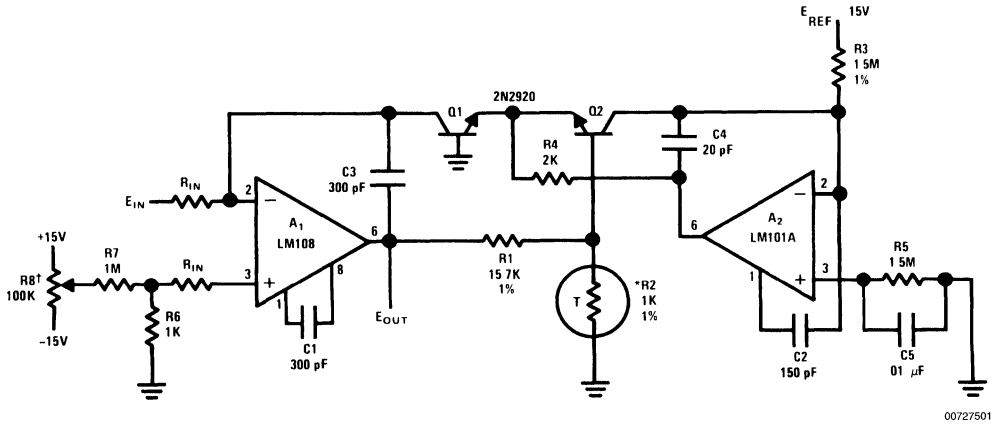
for $E_{IN} \geq 0$. This shows that the output is proportional to the logarithm of the input voltage. The coefficient of the log term is directly proportional to absolute temperature. Without compensation, the scale factor will also vary directly with temperature. However, by making R_2 directly proportional to temperature, constant gain is obtained. The temperature compensation is typically 1% over a temperature range of −25°C to 100°C for the resistor specified. For limited temperature range applications, such as 0°C to 50°C, a 430Ω sensistor in series with a 570Ω resistor may be substituted for the 1k resistor, also with 1% accuracy. The divider, R_1 and R_2, sets the gain while the current through R_3 sets the zero. With the values given, the scale factor is 1V/decade and

$$E_{OUT} = -\left[\log_{10}\left|\frac{E_{IN}}{R_{IN}}\right| + 5\right] \quad (4)$$

where the absolute value sign indicates that the dimensions of the quantity inside are to be ignored.

Log generator circuits are not limited to inverting operation. In fact, a feature of this circuit is the ease with which non-inverting operation is obtained. Supplying the input signal to A_2 and the reference current to A_1 results in a log output that is not inverted from the input. To achieve the same 100 dB dynamic range in the non-inverting configuration, an LM108 should be used for A_2, and an LM101A for A_1. Since the LM108 cannot use feedforward compensation, it is frequency compensated with the standard 30 pF capacitor.

The only other change is the addition of a clamp diode connected from the emitter of Q_1 to ground. This prevents damage to the logging transistors if the input signal should go negative.



*1 kΩ (±1%) at 25°C, +3500 ppm/°C

Available from Vishay Ultronix, Grand Junction, CO, Q81 Series

†Offset Voltage Adjust

FIGURE 1. Log Generator with 100 dB Dynamic Range

The log output is accurate to 1% for any current between 10 nA and 1 mA. This is equivalent to about 3% referred to the input. At currents over 500 µA the transistors used deviate from log characteristics due to resistance in the emitter, while at low currents, the offset current of the LM108 is the major source of error. These errors occur at the ends of the dynamic range, and from 40 nA to 400 µA the log converter is 1% accurate referred to the input. Both of the transistors are used in the grounded base connection, rather than the diode connection, to eliminate errors due to base current. Unfortunately, the grounded base connection increases the loop gain. More frequency compensation is necessary to prevent oscillation, and the log converter is necessarily slow. It may take 1 to 5 ms for the output to settle to 1% of its final value. This is especially true at low currents.

The circuit shown in *Figure 2* is two orders of magnitude faster than the previous circuit and has a dynamic range of 80 dB. Operation is the same as the circuit in *Figure 1*, except the configuration optimizes speed rather than dynamic range Transistor Q_1 is diode connected to allow the use of feedforward compensation[1] on an LM101A operational amplifier. This compensation extends the bandwidth to 10 MHz and increases the slew rate. To prevent errors due to the finite h_{FE} of Q_1 and the bias current of the LM101A, an LM102 voltage follower buffers the base current and input current. Although the log circuit will operate without the LM102, accuracy will degrade at low input currents. Amplifier A_2 is also compensated for maximum bandwidth. As with the previous log converter, R_1 and R_2 control the sensitivity; and R_3 controls the zero crossing of the transfer function. With the values shown the scale factor is 1V/decade and

$$E_{OUT} = -\left[\log_{10}\left|\frac{E_{IN}}{R_{IN}}\right| + 4\right] \quad (5)$$

from less than 100 nA to 1 mA.

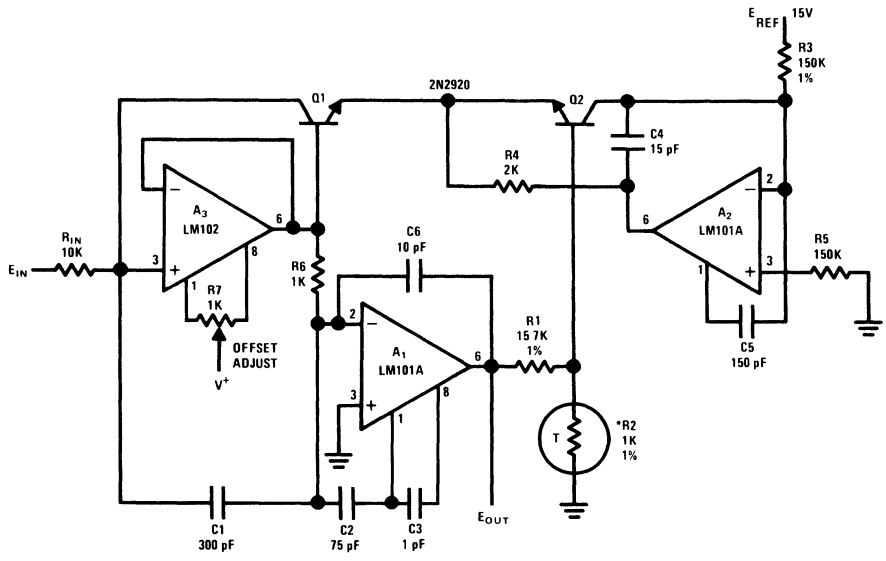
Anti-log or exponential generation is simply a matter of rearranging the circuitry. *Figure 3* shows the circuitry of the log converter connected to generate an exponential output from a linear input. Amplifier A_1 in conjunction with transistor Q_1 drives the emitter of Q_2 in proportion to the input voltage. The collector current of Q_2 varies exponentially with the emitter-base voltage. This current is converted to a voltage by amplifier A_2. With the values given

$$E_{OUT} = 10^{-[E_{IN}]}. \quad (6)$$

Many non-linear functions such as $X^{1/2}$, X^2, X^3, 1/X, XY, and X/Y are easily generated with the use of logs. Multiplication becomes addition, division becomes subtraction and powers become gain coefficients of log terms. *Figure 4* shows a circuit whose output is the cube of the input. Actually, any power function is available from this circuit by changing the values of R_9 and R_{10} in accordance with the expression:

$$E_{OUT} = E_{IN}^{\frac{16\,7\,R_9}{R_9 + R_{10}}}. \quad (7)$$

Note that when log and anti-log circuits are used to perform an operation with a linear output, no temperature compensating resistors at all are needed. If the log and anti-log transistors are at the same temperature, gain changes with temperature cancel. It is a good idea to use a heat sink which couples the two transistors to minimize thermal gradients. A 1°C temperature difference between the log and anti-log transistors results in a 0 3% error. Also, in the log converters, a 1°C difference between the log transistors and the compensating resistor results in a 0.3% error.



*1 kΩ (±1%) at 25˚C, +3500 ppm/˚C.

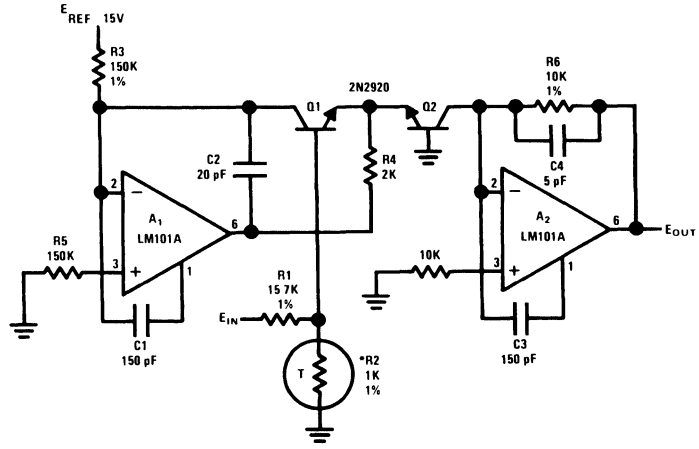
Available from Vishay Ultronix, Grand Junction, CO, Q81 Series

FIGURE 2. Fast Log Generator

Either of the circuits in *Figure 1* or *Figure 2* may be used as dividers or reciprocal generators. Equation 3 shows the outputs of the log generators are actually the ratio of two currents: the input current and the current through R_3. When used as a log generator, the current through R_3 was held constant by connecting R_3 to a fixed voltage. Hence, the output was just the log of the input. If R_3 is driven by an input voltage, rather than the 15V reference, the output of the log generator is the log ratio of the input current to the current through R_3. The anti-log of this voltage is the quotient. Of course, if the divisor is constant, the output is the reciprocal.

A complete one quadrant multiplier/divider is shown in *Figure 5*. It is basically the log generator shown in *Figure 1* driving the anti-log generator shown in *Figure 3*. The log generator output from A_1 drives the base of Q_3 with a voltage proportional to the log of E_1/E_2. Transistor Q_3 adds a voltage proportional to the log of E_3 and drives the anti-log transistor, Q_4. The collector current of Q_4 is converted to an output voltage by A_4 and R_7, with the scale factor set by R_7 at $E_1 E_3/10E_2$.

Measurement of transistor current gains over a wide range of operating currents is an application particularly suited to log multiplier/dividers. Using the circuit in *Figure 5*, PNP current gains can be measured at currents from 0.4 µA to 1 mA. The collector current is the input signal to A_1, the base current is the input signal to A_2, and a fixed voltage to R_5 sets the scale factor. Since A_2 holds the base at ground, a single resistor from the emitter to the positive supply is all that is needed to establish the operating current. The output is proportional to collector current divided by base current, or h_{FE}.



*1 kΩ (±1%) at 25°C, +3500 ppm/°C

Available from Vishay Ultronix, Grand Junction, CO, Q81 Series

FIGURE 3. Anti-Log Generator

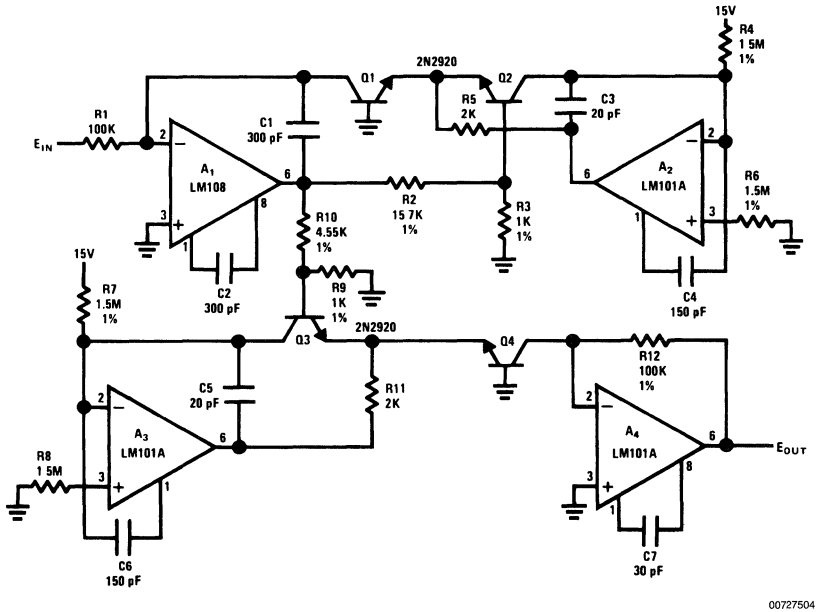


FIGURE 4. Cube Generator

In addition to their application in performing functional operations, log generators can provide a significant increase in the dynamic range of signal processing systems. Also, unlike a linear system, there is no loss in accuracy or resolution when the input signal is small compared to full scale. Over most of the dynamic range, the accuracy is a percent-of-signal rather than a percent-of-full-scale. For example, using log generators, a simple meter can display signals with 100 dB dynamic range or an oscilloscope can display a 10 mV and 10V pulse simultaneously. Obviously, without the log generator, the low level signals are completely lost.

To achieve wide dynamic range with high accuracy, the input operational amplifier necessarily must have low offset voltage, bias current and offset current. The LM108 has a maximum bias current of *3 nA* and offset current of *400 pA* over

a −55°C to 125°C temperature range. By using equal source resistors, only the offset current of the LM108 causes an error. The offset current of the LM108 is as low as many FET amplifiers. Further, it has a low and constant temperature coefficient rather than doubling every 10°C. This results in greater accuracy over temperature than can be achieved with FET amplifiers. The offset voltage may be zeroed, if necessary, to improve accuracy with low input voltages.

The log converters are low level circuits and some care should be taken during construction. The input leads should be as short as possible and the input circuitry guarded against leakage currents. Solder residues can easily conduct leakage currents, therefore circuit boards should be cleaned before use High quality glass or mica capacitors should be used on the inputs to minimize leakage currents. Also, when the +15V supply is used as a reference, it must be well regulated.

References

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2. R. J. Widlar, *"Monolithic Operational Amplifiers—The Universal Linear Component"*, National Semiconductor Corporation, AN-4, April, 1968.

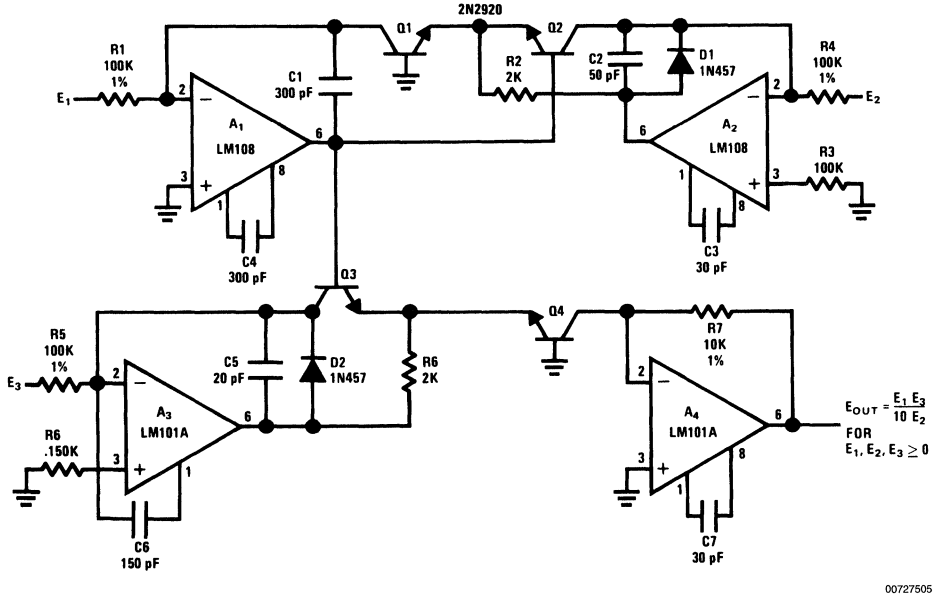


FIGURE 5. Multiplier/Divider

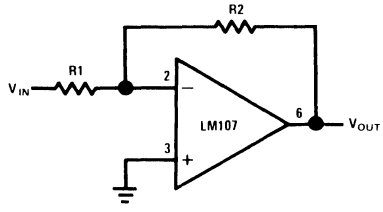
Op Amp Circuit Collection

National Semiconductor
Application Note 31

Note: National Semiconductor recommends replacing 2N2920 and 2N3728 matched pairs with LM394 in all application circuits.

Section 1—Basic Circuits

Inverting Amplifier

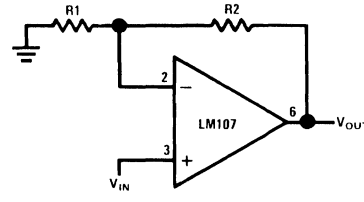


00705701

$$V_{OUT} = -\frac{R2}{R1} V_{IN}$$

$$R_{IN} = R1$$

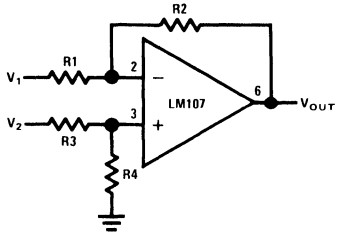
Non-Inverting Amplifier



00705702

$$V_{OUT} = \frac{R1 + R2}{R1} V_{IN}$$

Difference Amplifier



00705703

$$V_{OUT} = \left(\frac{R1 + R2}{R3 + R4}\right)\frac{R4}{R1} V_2 - \frac{R2}{R1} V_1$$

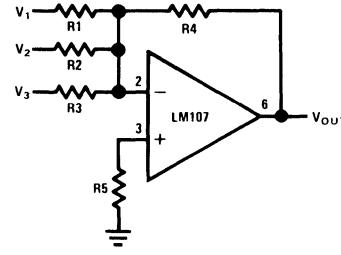
For R1 = R3 and R2 = R4

$$V_{OUT} = \frac{R2}{R1}(V_2 - V_1)$$

R1//R2 = R3//R4

For minimum offset error due to input bias current

Inverting Summing Amplifier



00705704

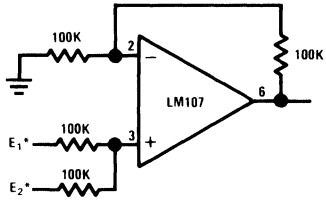
$$V_{OUT} = -R4\left(\frac{V_1}{R1} + \frac{V_2}{R2} + \frac{V_3}{R3}\right)$$

R5 = R1//R2//R3//R4

For minimum offset error due to input bias current

Section 1—Basic Circuits (Continued)

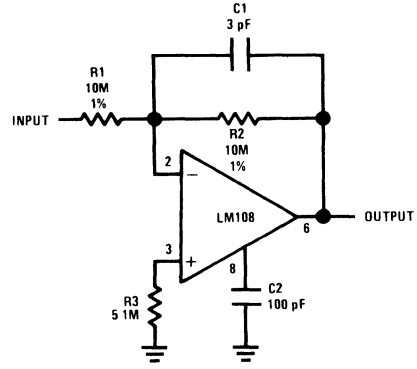
Non-Inverting Summing Amplifier



00705705

*R_S = 1k for 1% accuracy

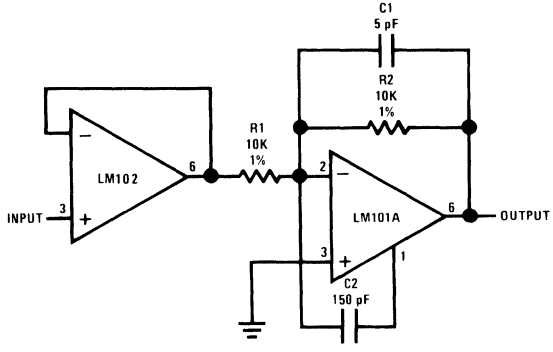
Inverting Amplifier with High Input Impedance



00705706

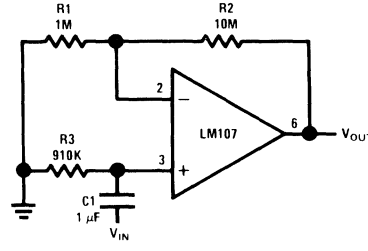
*Source Impedance less than 100k gives less than 1% gain error

Fast Inverting Amplifier with High Input Impedance



00705707

Non-Inverting AC Amplifier



00705708

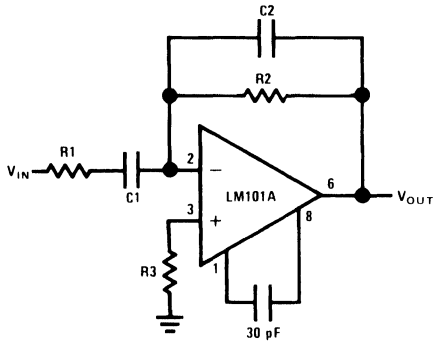
$$V_{OUT} = \frac{R1 + R2}{R1} V_{IN}$$

$R_{IN} = R3$

$R3 = R1 // R2$

Section 1—Basic Circuits (Continued)

Practical Differentiator



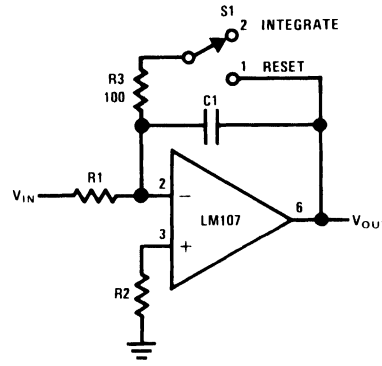
00705709

$$f_c = \frac{1}{2\pi R2C1}$$

$$f_h = \frac{1}{2\pi R1C1} = \frac{1}{2\pi R2C2}$$

$f_c \ll f_h \ll f_{unity\ gain}$

Integrator



00705710

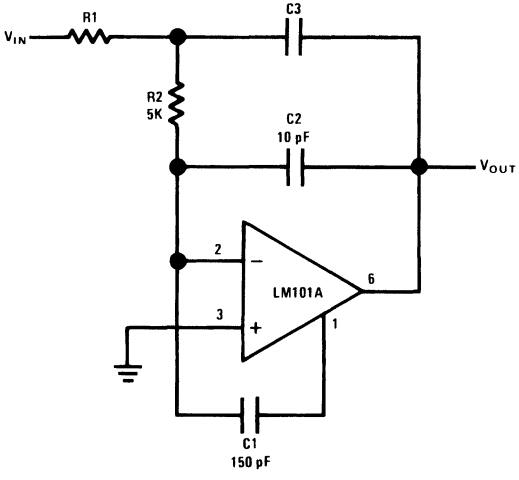
$$V_{OUT} = -\frac{1}{R1C1}\int_{t_1}^{t_2} V_{IN}\,dt$$

$$f_c = \frac{1}{2\pi R1C1}$$

R1 = R2

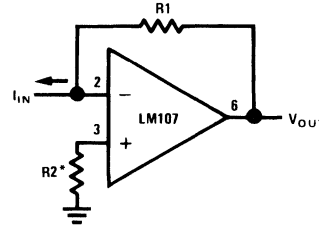
For minimum offset error due to input bias current

Fast Integrator



00705711

Current to Voltage Converter



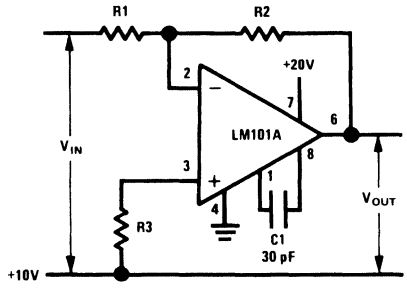
00705712

$V_{OUT} = I_{IN}\,R1$

*For minimum error due to bias current R2 = R1

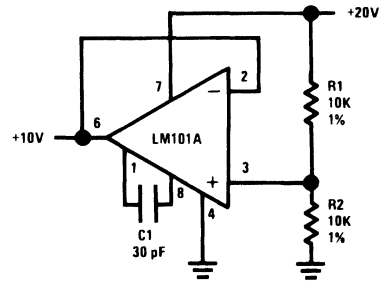
Section 1—Basic Circuits (Continued)

Circuit for Operating the LM101 without a Negative Supply



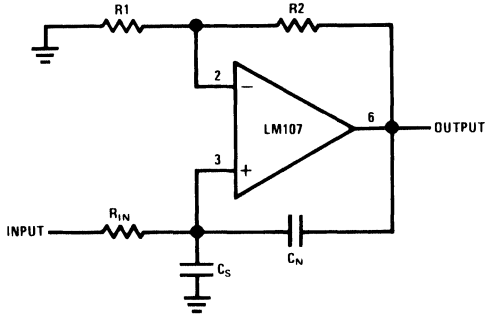
00705713

Circuit for Generating the Second Positive Voltage



00705714

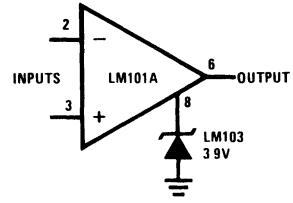
Neutralizing Input Capacitance to Optimize Response Time



00705715

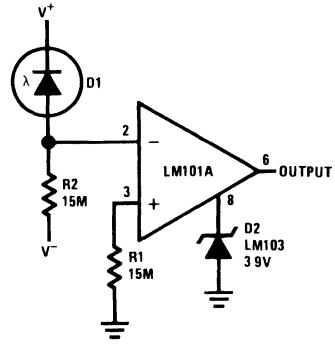
$$C_N \leq \frac{R1}{R2} C_S$$

Voltage Comparator for Driving DTL or TTL Integrated Circuits



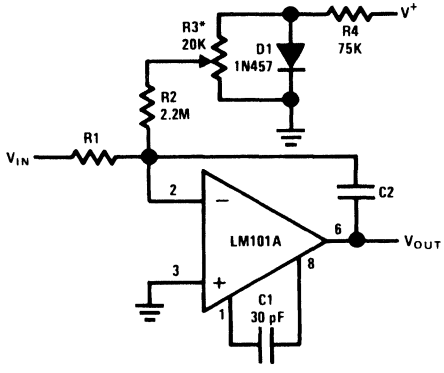
00705717

Threshold Detector for Photodiodes



00705718

Integrator with Bias Current Compensation



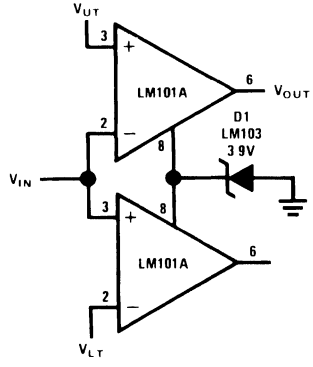
00705716

*Adjust for zero integrator drift

Current drift typically 0.1 n/A°C over −55°C to 125°C temperature range.

Section 1—Basic Circuits (Continued)

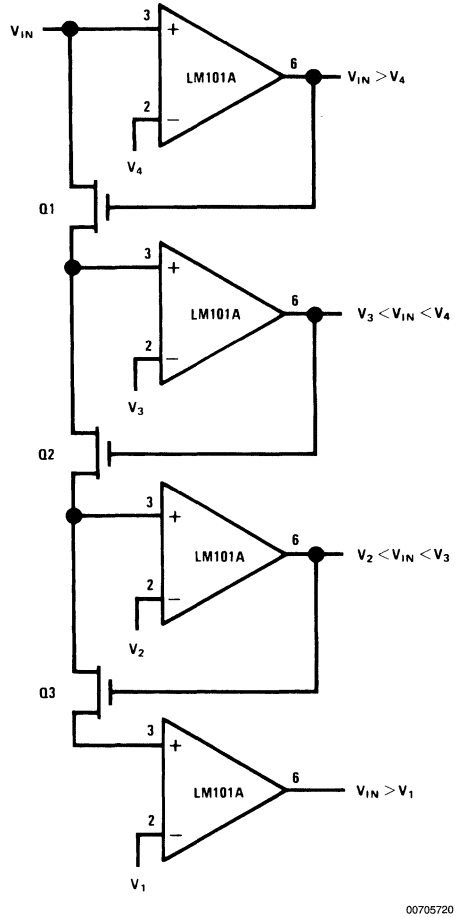
Double-Ended Limit Detector



00705719

V_{OUT} = 4.6V for $V_{LT} \leq V_{IN} \leq V_{UT}$
V_{OUT} = 0V for $V_{IN} < V_{LT}$ or $V_{IN} > V_{UT}$

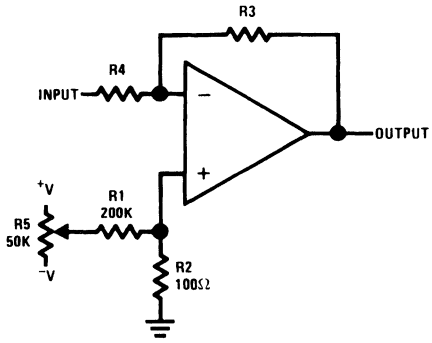
Multiple Aperture Window Discriminator



00705720

Section 1—Basic Circuits (Continued)

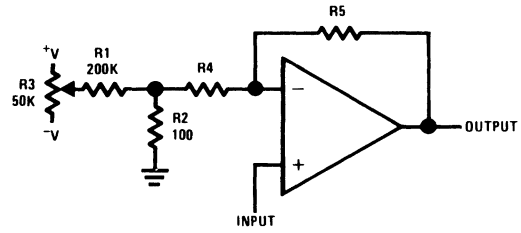
Offset Voltage Adjustment for Inverting Amplifiers Using Any Type of Feedback Element



00705721

$$\text{RANGE} = \pm V\left(\frac{R2}{R1}\right)$$

Offset Voltage Adjustment for Non-Inverting Amplifiers Using Any Type of Feedback Element

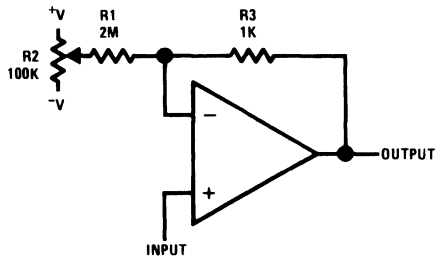


00705722

$$\text{RANGE} = \pm V\left(\frac{R2}{R1}\right)$$

$$\text{GAIN} = 1 + \frac{R5}{R4 + R2}$$

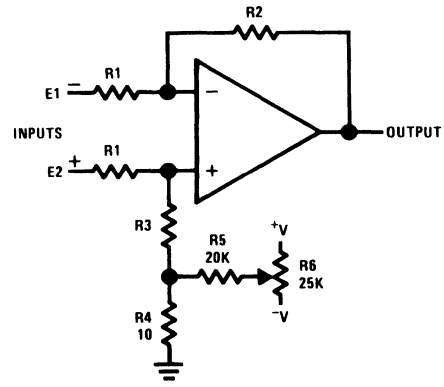
Offset Voltage Adjustment for Voltage Followers



00705723

$$\text{RANGE} = \pm V\left(\frac{R3}{R1}\right)$$

Offset Voltage Adjustment for Differential Amplifiers



00705724

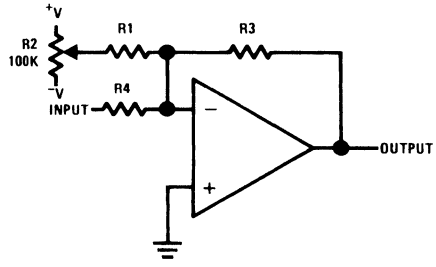
$$R2 = R3 + R4$$

$$\text{RANGE} = \pm V\left(\frac{R5}{R4}\right)\left(\frac{R1}{R1 + R3}\right)$$

$$\text{GAIN} = \frac{R2}{R1}$$

Section 1—Basic Circuits (Continued)

Offset Voltage Adjustment for Inverting Amplifiers Using 10 kΩ Source Resistance or Less



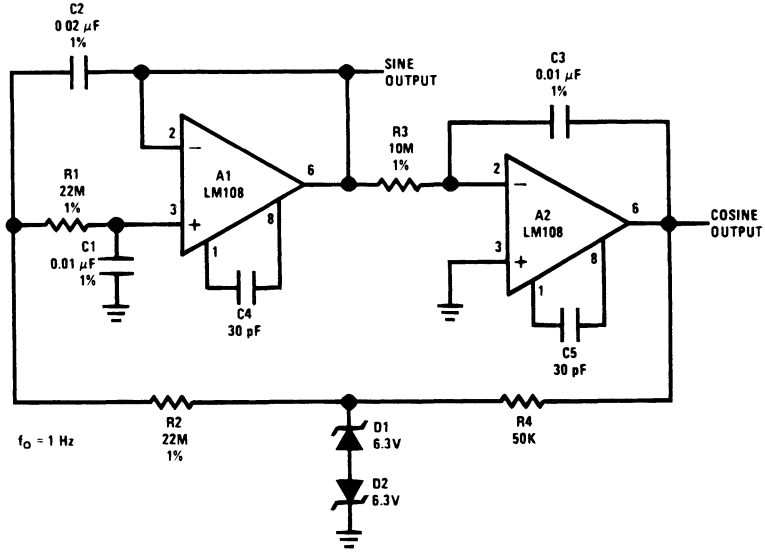
$R1 = 2000\ R3//R4$

$R4//R3 \leq 10\ k\Omega$

$$RANGE = \pm V\left(\frac{R3//R4}{R1}\right)$$

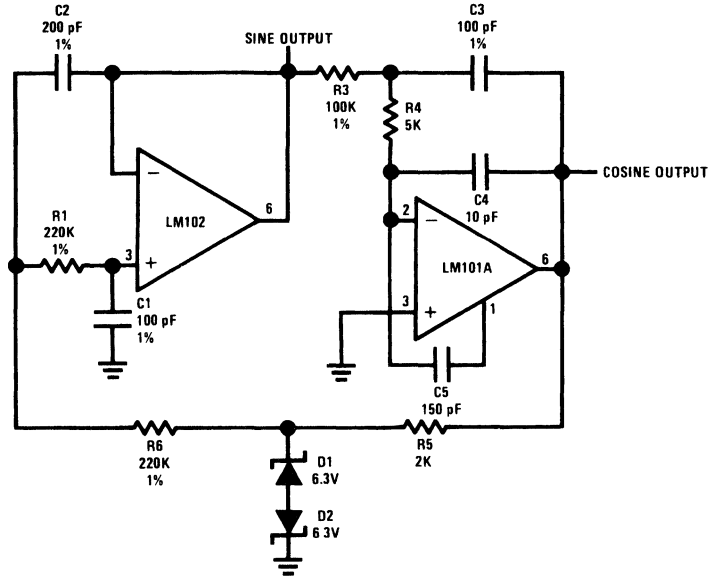
Section 2 — Signal Generation

Low Frequency Sine Wave Generator with Quadrature Output



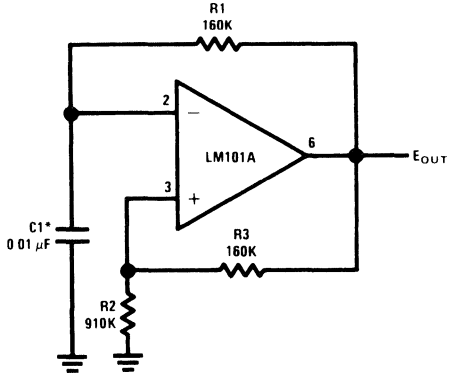
Section 2 — Signal Generation (Continued)

High Frequency Sine Wave Generator with Quadrature Output



00705727

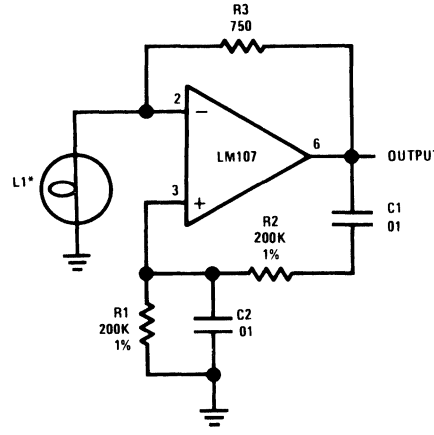
Free-Running Multivibrator



00705728

*Chosen for oscillation at 100 Hz

Wein Bridge Sine Wave Oscillator



00705729

$R1 = R2$

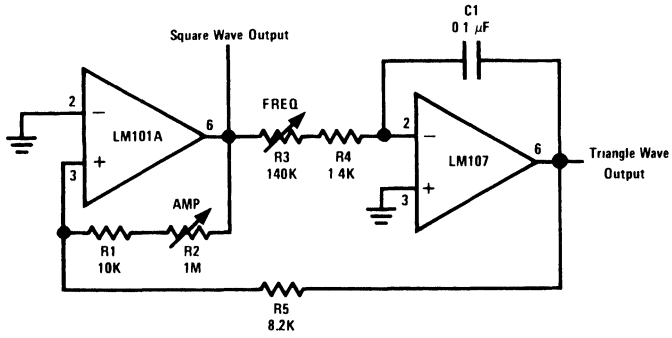
$C1 = C2$

$$f = \frac{1}{2\pi R1\ C1}$$

*Eldema 1869 10V, 14 mA Bulb

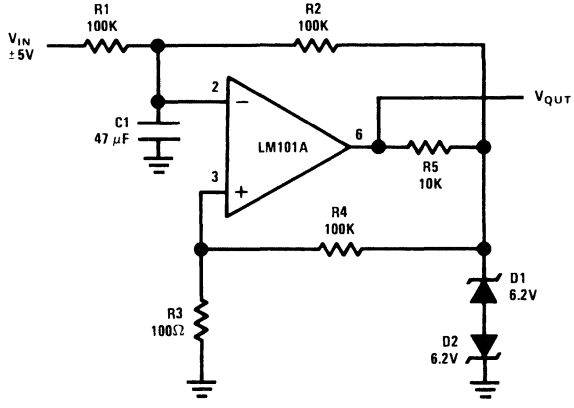
Section 2 — Signal Generation (Continued)

Function Generator



00705730

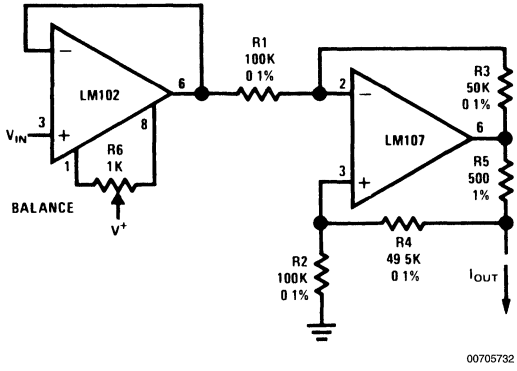
Pulse Width Modulator



00705731

Section 2 — Signal Generation (Continued)

Bilateral Current Source

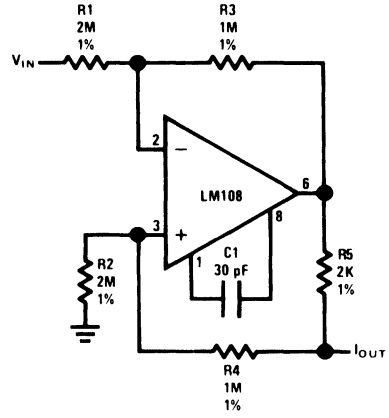


$$I_{OUT} = \frac{R3\ V_{IN}}{R1\ R5}$$

$R3 = R4 + R5$

$R1 = R2$

Bilateral Current Source



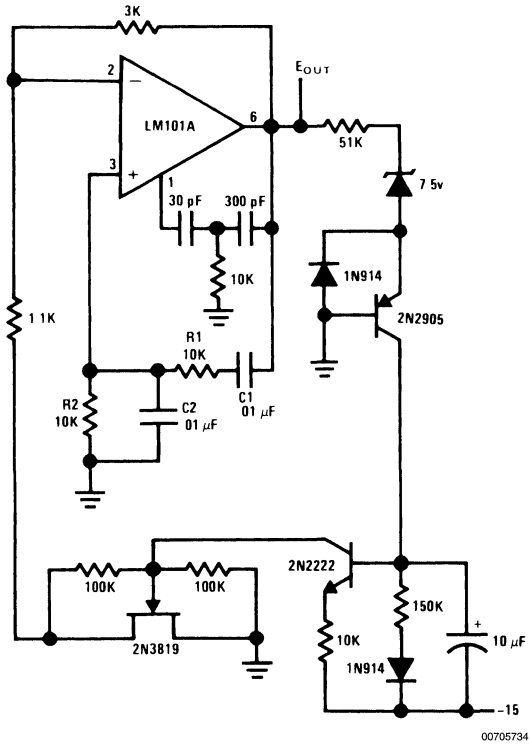
$$I_{OUT} = \frac{R3\ V_{IN}}{R1\ R5}$$

$R3 = R4 + R5$

$R1 = R2$

Section 2 — Signal Generation (Continued)

Wein Bridge Oscillator with FET Amplitude Stabilization



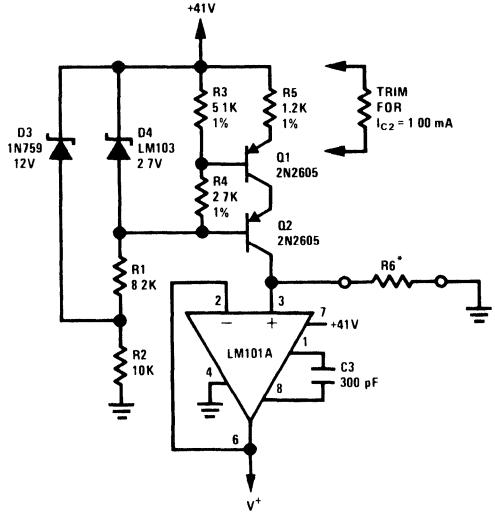
$R1 = R2$

$C1 = C2$

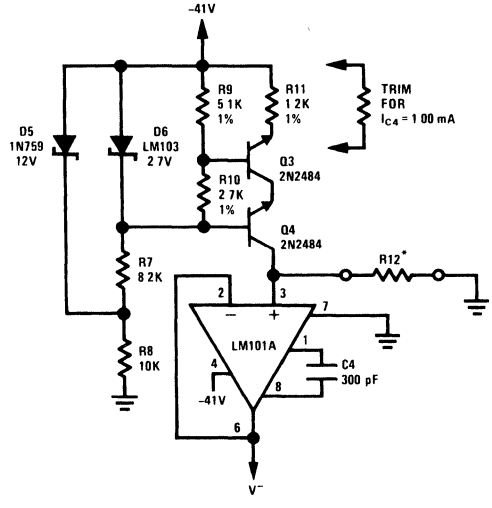
$$f = \frac{1}{2\pi R1\ C1}$$

Section 2 — Signal Generation (Continued)

Low Power Supply for Integrated Circuit Testing



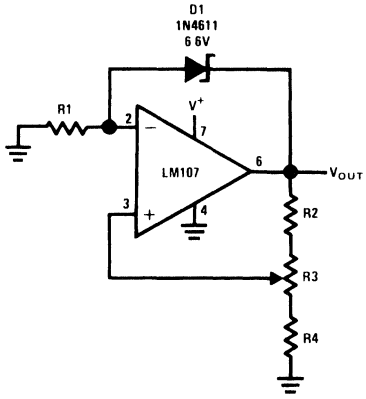
00705735



00705791

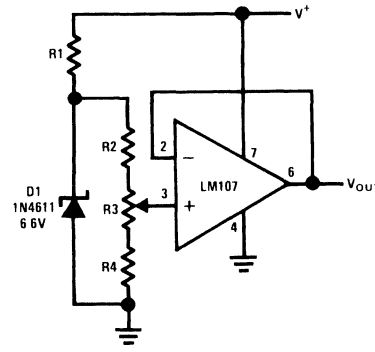
*V_{OUT} = 1V/kΩ

Positive Voltage Reference



00705736

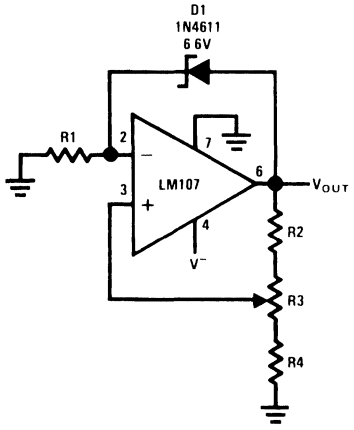
Positive Voltage Reference



00705737

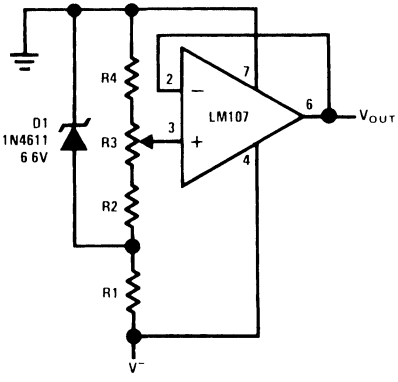
Section 2 — Signal Generation (Continued)

Negative Voltage Reference



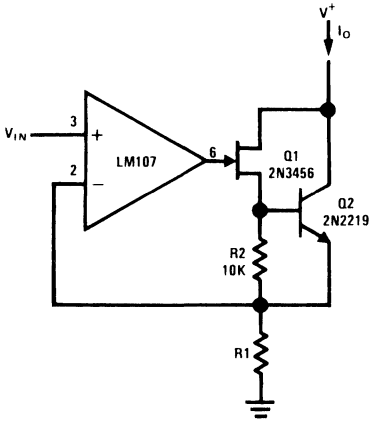
00705738

Negative Voltage Reference



00705739

Precision Current Sink

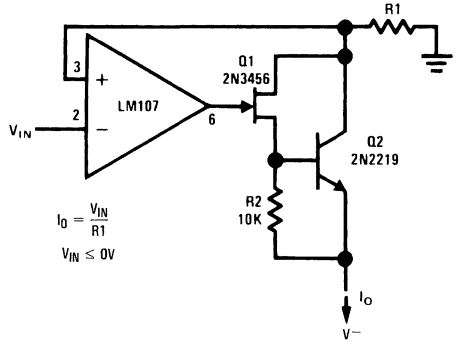


00705740

$$I_O = \frac{V_{IN}}{R1}$$

$V_{IN} \geq 0V$

Precision Current Source



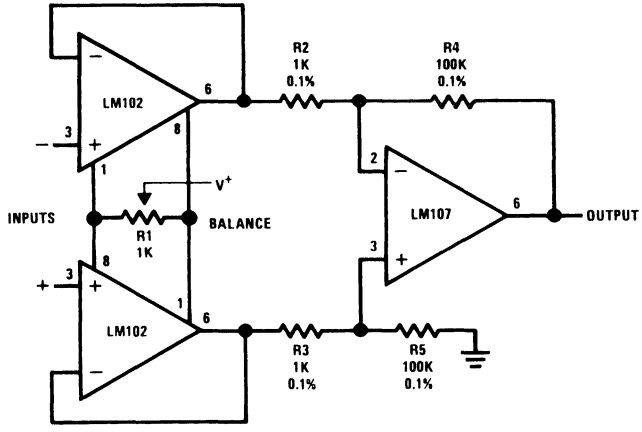
00705741

$$I_O = \frac{V_{IN}}{R1}$$

$V_{IN} \leq 0V$

Section 3 — Signal Processing

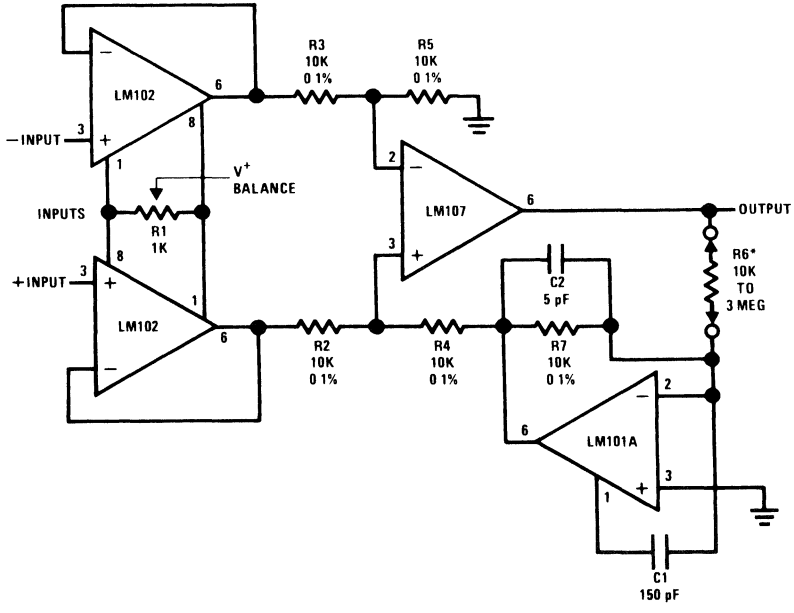
Differential-Input Instrumentation Amplifier



$$\frac{R4}{R2} = \frac{R5}{R3}$$

$$A_V = \frac{R4}{R2}$$

Variable Gain, Differential-Input Instrumentation Amplifier

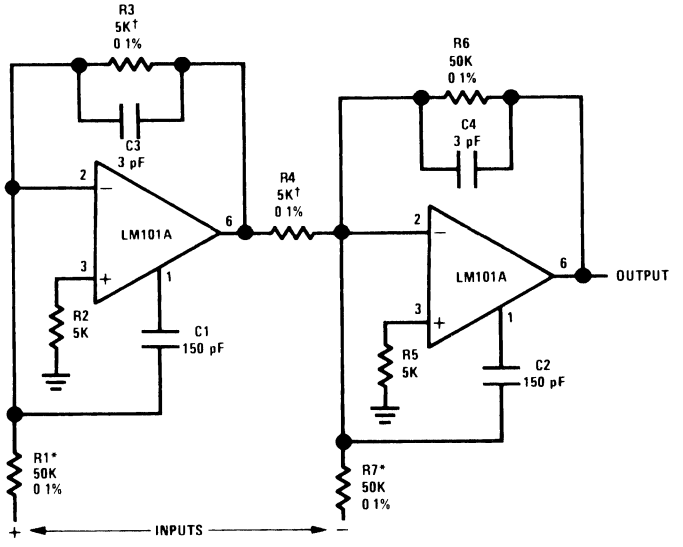


*Gain adjust

$A_V = 10^{-4}$ R6

Section 3 — Signal Processing (Continued)

Instrumentation Amplifier with ±100 Volt Common Mode Range

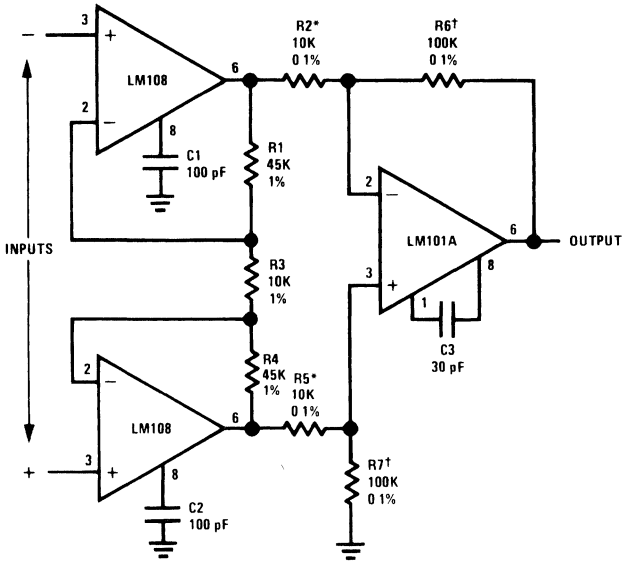


†Matching determines common mode rejection

$$R1 = R5 = 10R2$$
$$R2 = R3$$
$$R3 = R4$$
$$R1 = R6 = 10R3$$
$$A_V = \frac{R7}{R6}$$

Section 3 — Signal Processing (Continued)

Instrumentation Amplifier with ±10 Volt Common Mode Range



00705745

R1 = R4

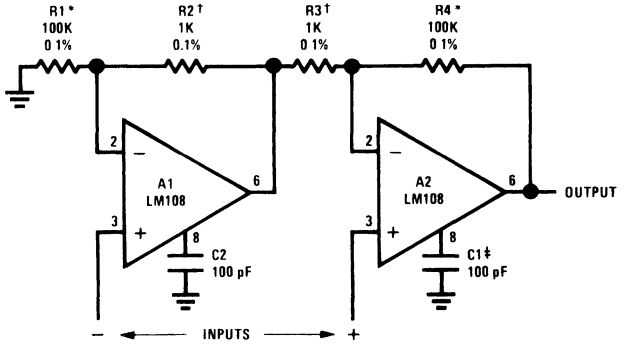
R2 = R5

R6 = R7

†*Matching Determines CMRR

$$A_V = \frac{R6}{R2}\left(1 + \frac{2R1}{R3}\right)$$

High Input Impedance Instrumentation Amplifier



00705746

R1 = R4; R2 = R3

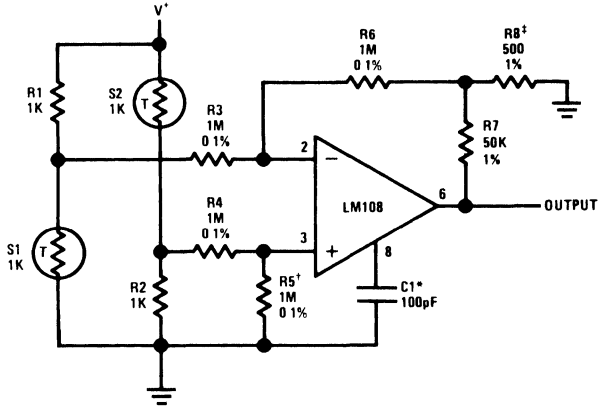
$$A_V = 1 + \frac{R1}{R2}$$

*†Matching Determines CMRR

‡May be deleted to maximize bandwidth

Section 3 — Signal Processing (Continued)

Bridge Amplifier with Low Noise Compensation



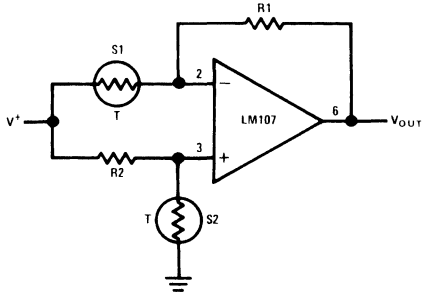
00705747

*Reduces feed through of power supply noise by 20 dB and makes supply bypassing unnecessary

†Trim for best common mode rejection

‡Gain adjust

Bridge Amplifier

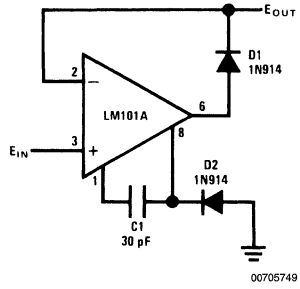


00705748

$$\frac{R1}{R_{S1}} = \frac{R2}{R_{S2}}$$

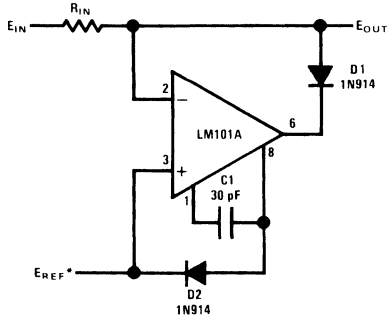
$$V_{OUT} = V+ \left(1 - \frac{R1}{R_{S1}}\right)$$

Precision Diode



00705749

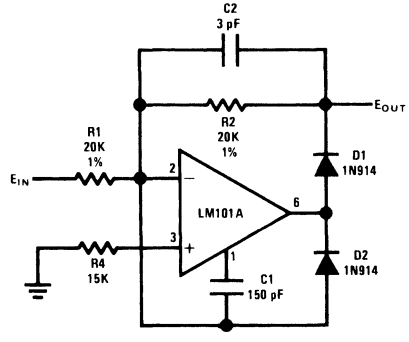
Precision Clamp



00705750

*E_{REF} must have a source impedance of less than 200Ω if D2 is used

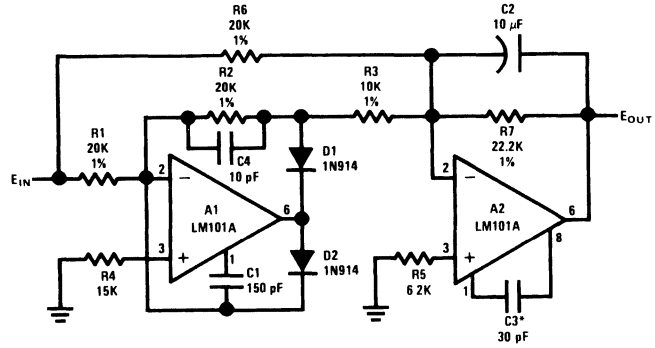
Fast Half Wave Rectifier



00705751

Section 3 — Signal Processing (Continued)

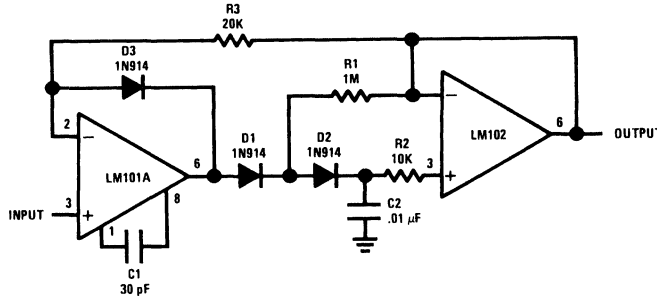
Precision AC to DC Converter



00705752

*Feedforward compensation can be used to make a fast full wave rectifier without a filter

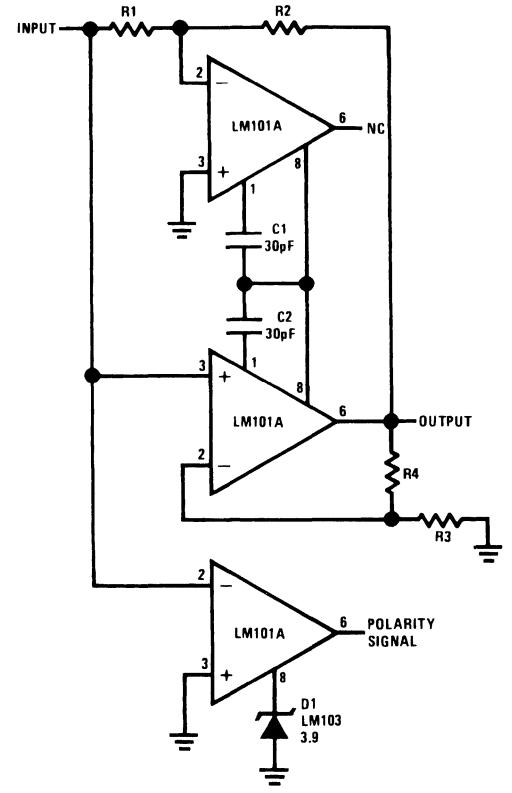
Low Drift Peak Detector



00705753

Section 3 — Signal Processing (Continued)

Absolute Value Amplifier with Polarity Detector

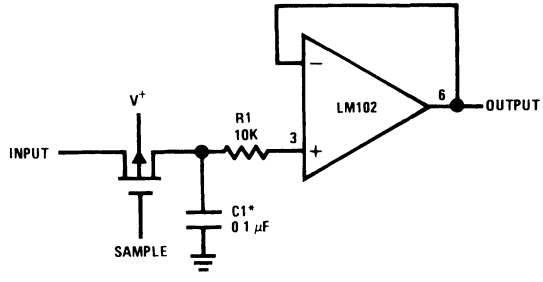


00705754

$$V_{OUT} = -|V_{IN}| \times \frac{R2}{R1}$$

$$\frac{R2}{R1} = \frac{R4 + R3}{R3}$$

Sample and Hold

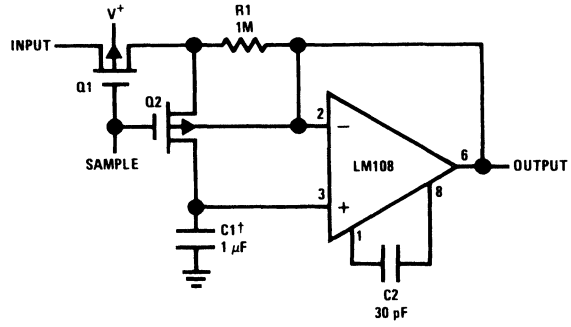


00705755

*Polycarbonate-dielectric capacitor

Section 3 — Signal Processing (Continued)

Sample and Hold

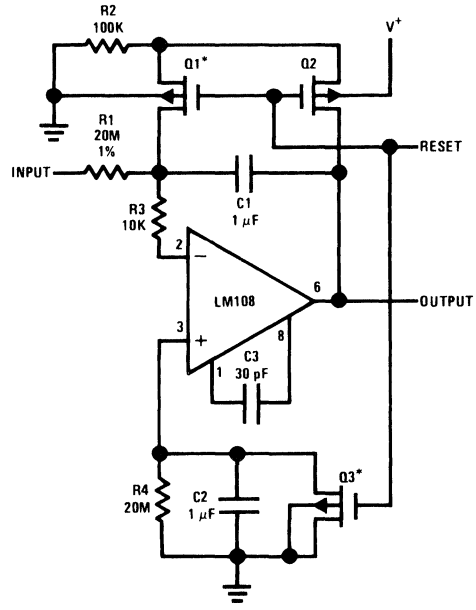


00705756

*Worst case drift less than 2 5 mV/sec

†Teflon, Polyethylene or Polycarbonate Dielectric Capacitor

Low Drift Integrator



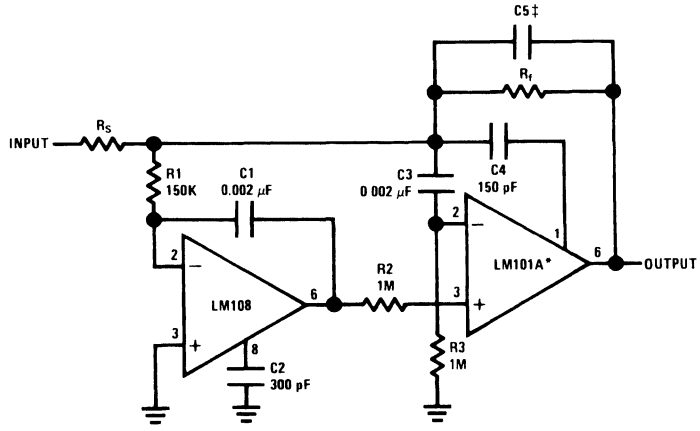
00705757

*Q1 and Q3 should not have internal gate-protection diodes

Worst case drift less than 500 μV/sec over −55°C to +125°C

Section 3 — Signal Processing (Continued)

Fast† Summing Amplifier with Low Input Current



00705758

*In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback

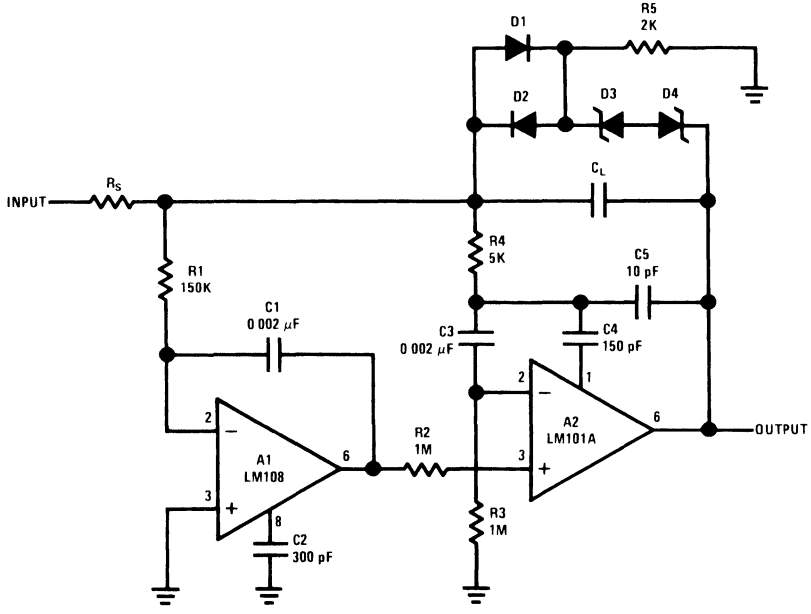
†Power Bandwidth 250 kHz

Small Signal Bandwidth 3 5 MHz

Slew Rate 10V/μs

$$\ddagger\ C5 = \frac{6 \times 10^{-8}}{R_f}$$

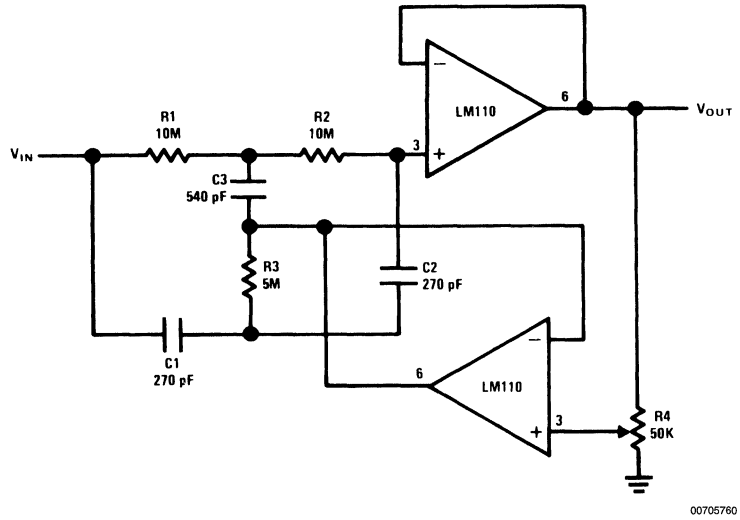
Fast Integrator with Low Input Current



00705759

Section 3 — Signal Processing (Continued)

Adjustable Q Notch Filter



00705760

$$f_O = \frac{1}{2\pi R1C1}$$

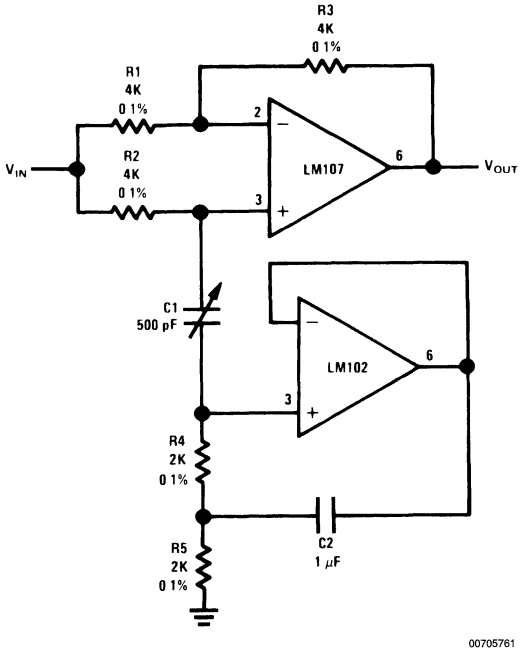
$= 60$ Hz

$R1 = R2 = R3$

$C1 = C2 = C23$

Section 3 — Signal Processing (Continued)

Easily Tuned Notch Filter

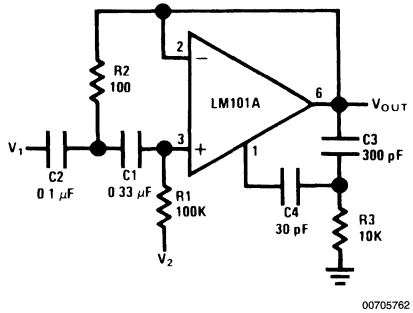


00705761

R4 = R5
R1 = R3
R4 = ½ R1

$$f_O = \frac{1}{2\pi R4\sqrt{C1C2}}$$

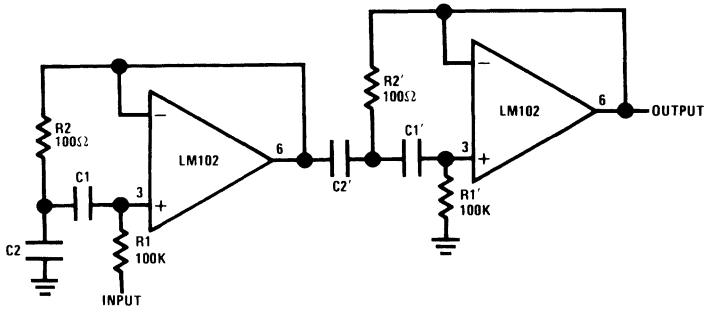
Tuned Circuit



00705762

$$f_O = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

Two-Stage Tuned Circuit

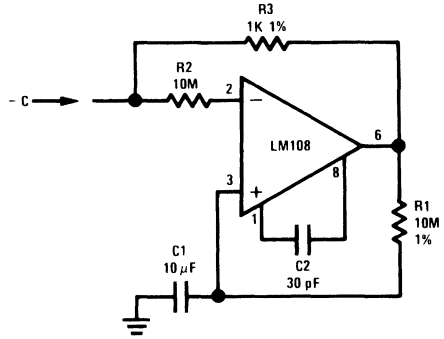


00705763

$$f_O = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

Section 3 — Signal Processing (Continued)

Negative Capacitance Multiplier



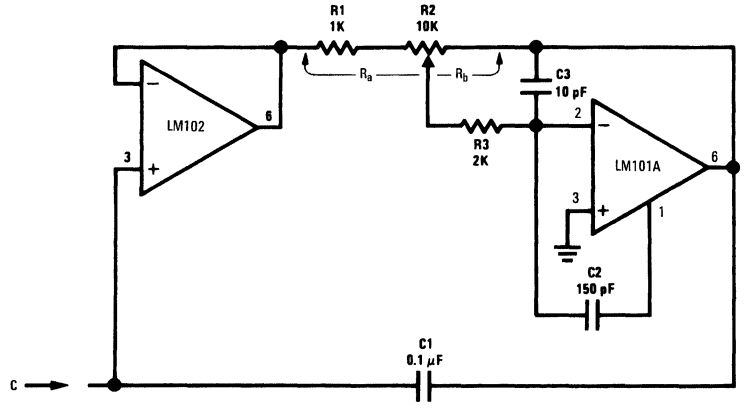
00705765

$$C = \frac{R2}{R3} C1$$

$$I_L = \frac{V_{OS} + R2\, I_{OS}}{R3}$$

$$R_S = \frac{R3(R1 + R_{IN})}{R_{IN}\, A_{VO}}$$

Variable Capacitance Multiplier

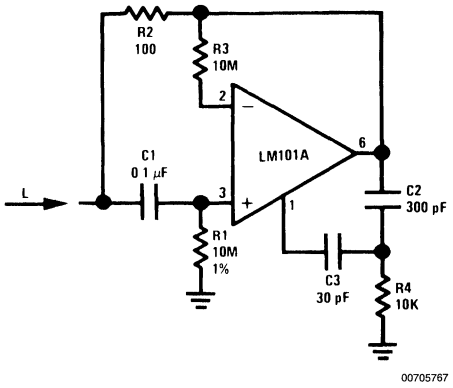


00705766

$$C = \left(1 + \frac{R_b}{R_a}\right) C_1$$

Section 3 — Signal Processing (Continued)

Simulated Inductor



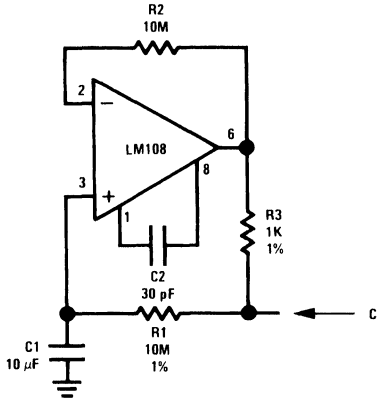
00705767

$L \geq R1\ R2\ C1$

$R_S = R2$

$R_P = R1$

Capacitance Multiplier



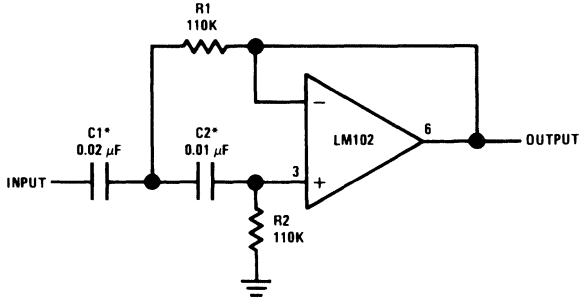
00705768

$$C = \frac{R1}{R3} C1$$

$$I_L = \frac{V_{OS} + I_{OS}\, R1}{R3}$$

$R_S = R3$

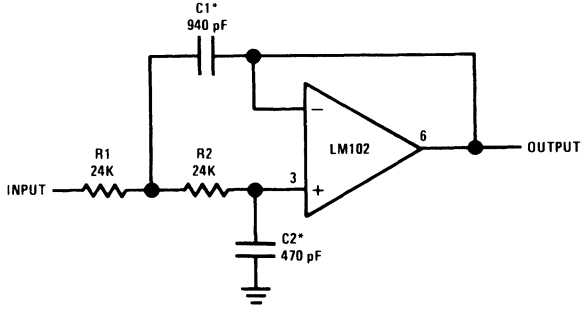
High Pass Active Filter



00705771

*Values are for 100 Hz cutoff Use metalized polycarbonate capacitors for good temperature stability

Low Pass Active Filter

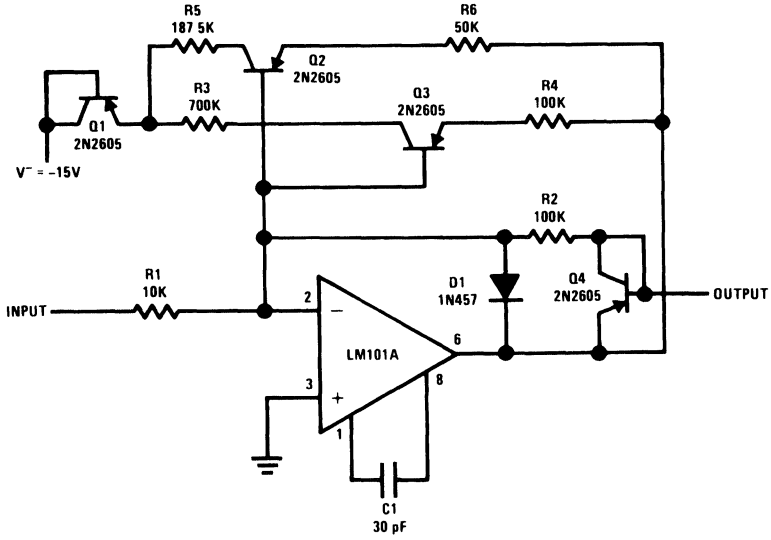


00705772

*Values are for 10 kHz cutoff Use silvered mica capacitors for good temperature stability

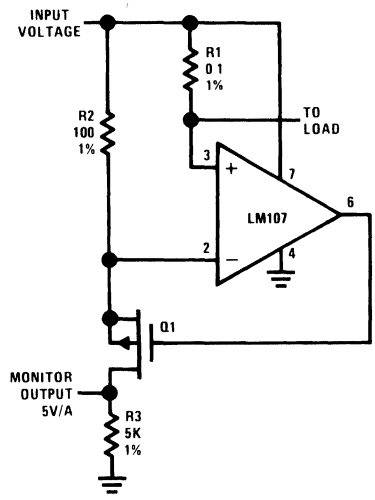
Section 3 — Signal Processing (Continued)

Nonlinear Operational Amplifier with Temperature Compensated Breakpoints



00705773

Current Monitor

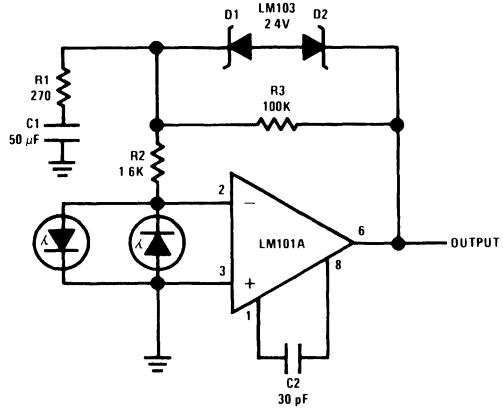


00705774

$$V_{OUT} = \frac{R1\ R3}{R2} I_L$$

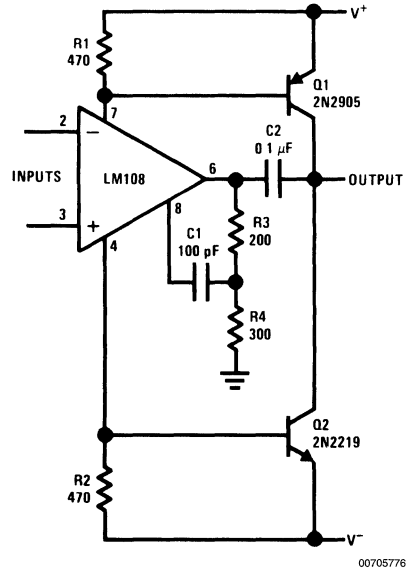
Section 3 — Signal Processing (Continued)

Saturating Servo Preamplifier with Rate Feedback



00705775

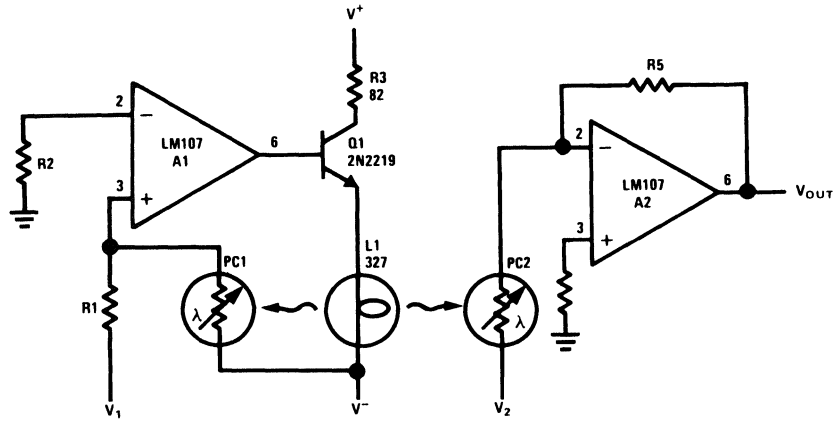
Power Booster



00705776

Section 3 — Signal Processing (Continued)

Analog Multiplier



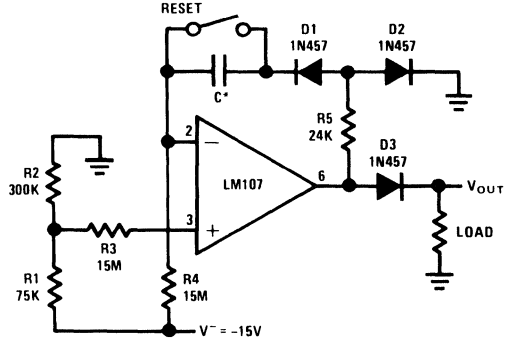
00705777

$$R5 = R1\left(\frac{V^-}{10}\right)$$

$$V_1 \geq 0$$

$$V_{OUT} = \frac{V_1 V_2}{10}$$

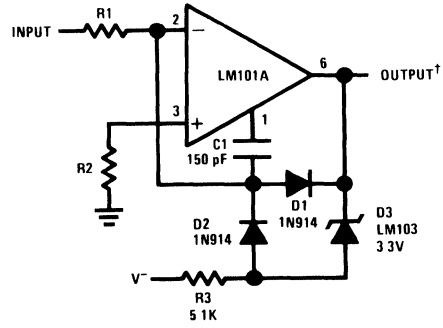
Long Interval Timer



00705778

*Low leakage −0 017 μF per second delay

Fast Zero Crossing Detector



00705779

Propagation delay approximately 200 ns

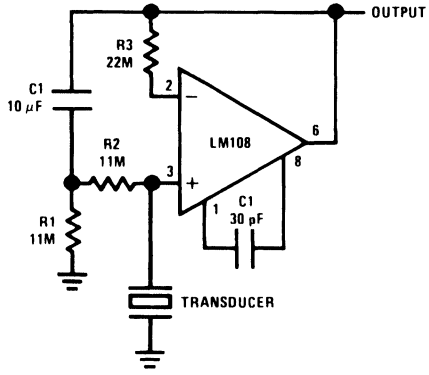
†DTL or TTL fanout of three

Minimize stray capacitance

Pin 8

Section 3 — Signal Processing (Continued)

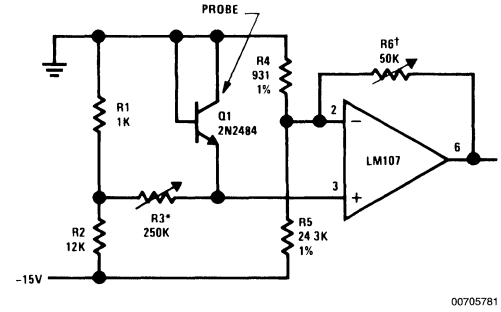
Amplifier for Piezoelectric Transducer



00705780

Low frequency cutoff = R1 C1

Temperature Probe

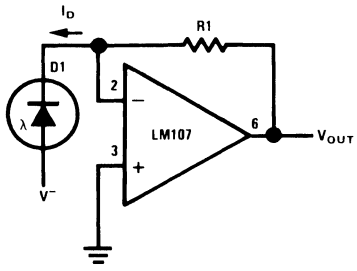


00705781

*Set for 0V at 0°C

†Adjust for 100 mV/°C

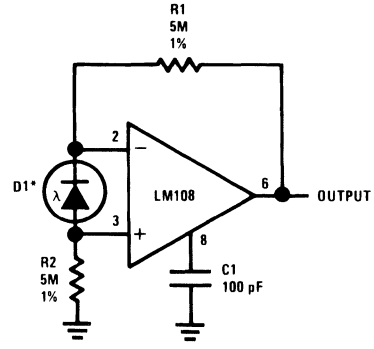
Photodiode Amplifier



00705782

$V_{OUT} = R1\ I_D$

Photodiode Amplifier

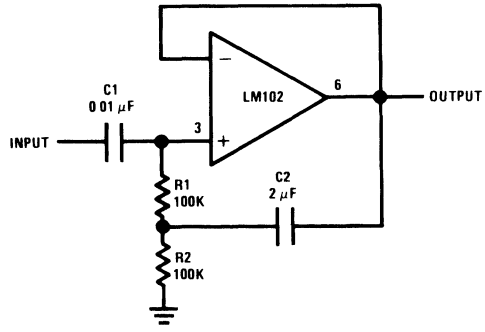


00705783

V_{OUT} = 10 V/μA

*Operating photodiode with less than 3 mV across it eliminates leakage currents

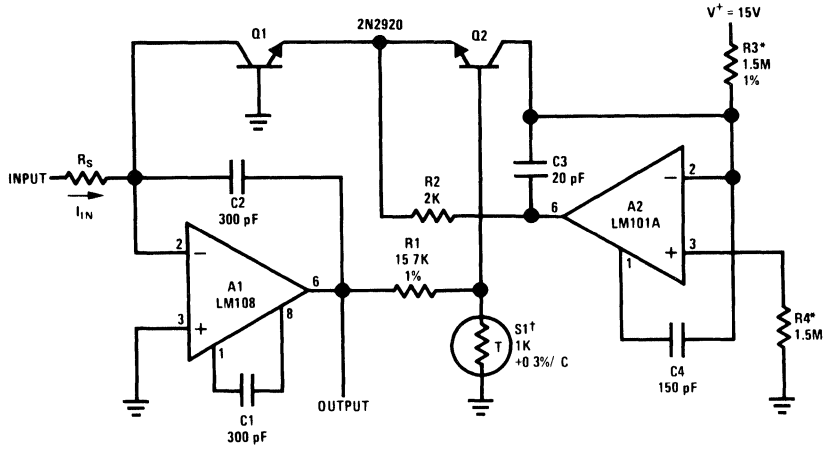
High Input Impedance AC Follower



00705784

Section 3 — Signal Processing (Continued)

Temperature Compensated Logarithmic Converter



00705785

10 nA < I_{IN} < 1 mA

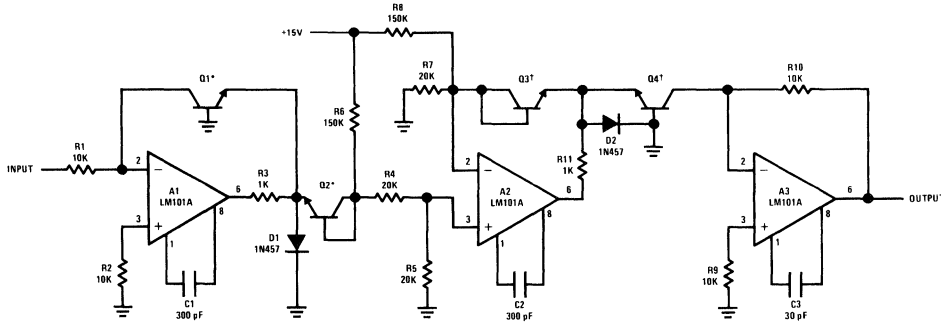
Sensitivity is 1V per decade

†1 kΩ (±1%) at 25°C, +3500 ppm/°C

Available from Vishay Ultronix, Grand Junction, CO, Q81 Series

*Determines current for zero crossing on output 10 µA as shown

Root Extractor

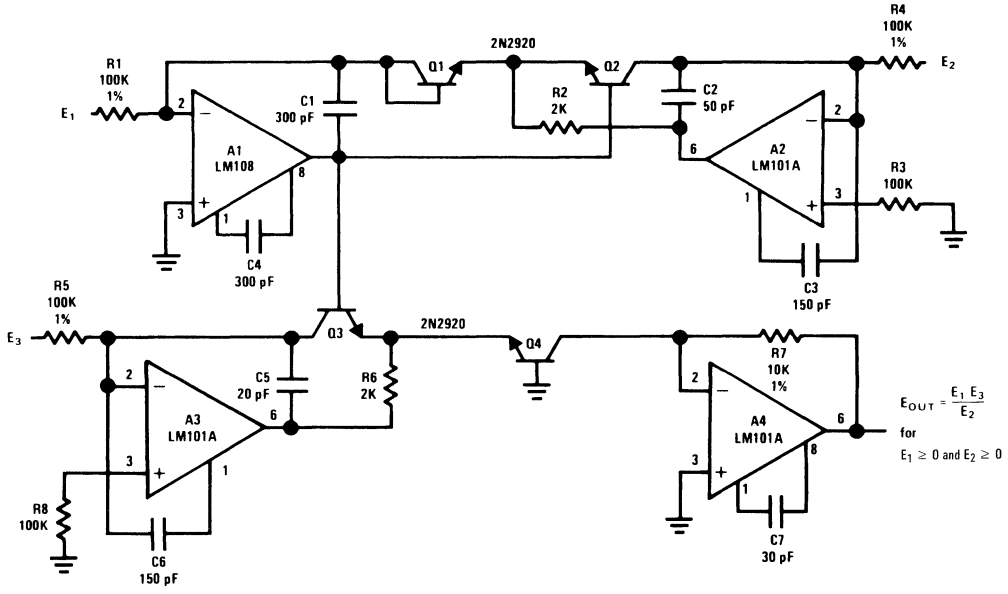


00705786

*†2N3728 matched pairs

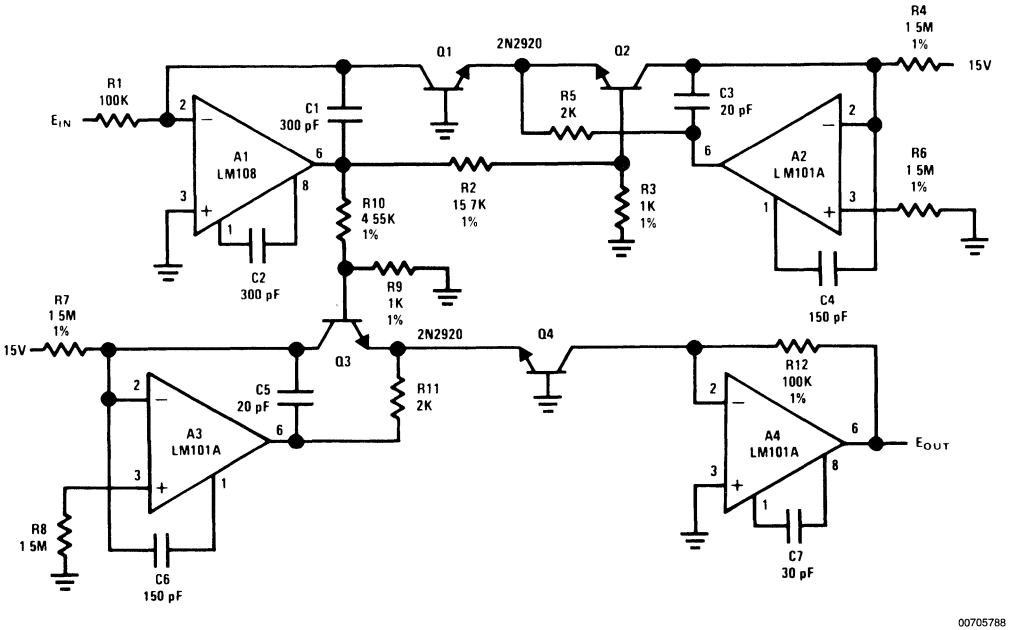
Section 3 — Signal Processing (Continued)

Multiplier/Divider



00705787

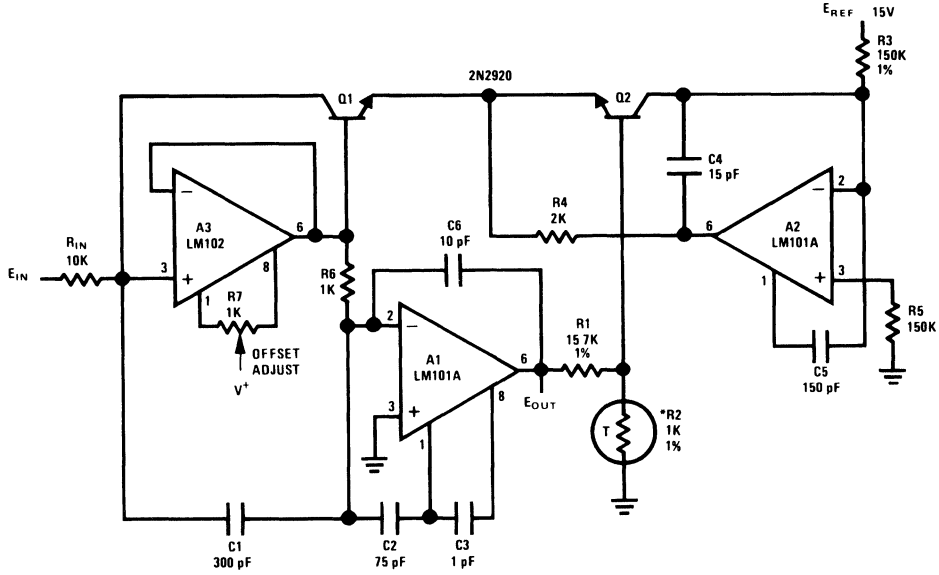
Cube Generator



00705788

Section 3 — Signal Processing (Continued)

Fast Log Generator

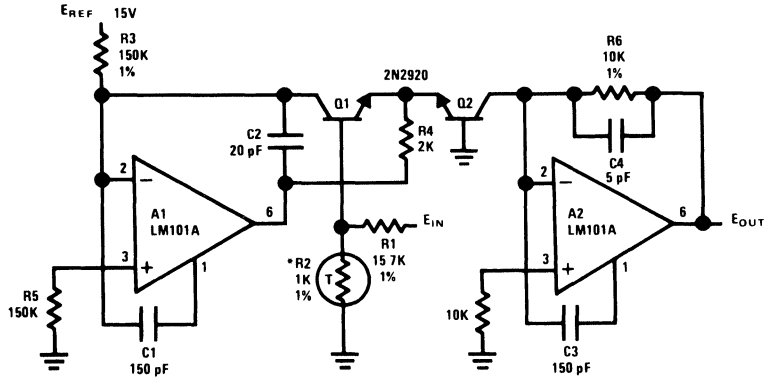


00705789

†1 kΩ (±1%) at 25°C, +3500 ppm/°C

Available from Vishay Ultronix, Grand Junction, CO, Q81 Series

Anti-Log Generator



00705790

†1 kΩ (±1%) at 25°C, +3500 ppm/°C

Available from Vishay Ultronix, Grand Junction, CO, Q81 Series

Micropower Circuits Using the LM4250 Programmable Op Amp

National Semiconductor
Application Note 71
George Cleveland

Introduction

The LM4250 is a highly versatile monolithic operational amplifier. A single external programming resistor determines the quiescent power dissipation, input offset and bias currents, slew rate, gain-bandwidth product, and input noise characteristics of the amplifier. Since the device is in effect a different op amp for each externally programmed set current, it is possible to use a single stock item for a variety of circuit functions in a system.

This paper describes the circuit operation of the LM4250, various methods of biasing the device, frequency response considerations, and some circuit applications exercising the unique characteristics of the LM4250.

Circuit Description LM4250

The LM4250 has two special features when compared with other monolithic operational amplifiers. One is the ability to externally set the bias current levels of the amplifiers, and the other is the use of PNP transistors as the differential input pair.

Referring to *Figure 1*, Q_1 and Q_2 are high current gain lateral PNPs connected as a differential pair. R_1 and R_2 provide emitter degeneration for greater stability at high bias currents. Q_3 and Q_4 are used as active loads for Q_1 and Q_2 to provide high gain and also form a current inverter to provide the maximum drive for the single ended output into Q_5. Q_5 is an emitter follower which prevents loading of the input stage by the succeeding amplifier stage.

One advantage of this lateral PNP input stage is a common mode swing to within 200 mV of the negative supply. This feature is especially useful in single supply operation with signals referred to ground. Another advantage is the almost constant input bias current over a wide temperature range. The input resistance R_{IN} is approximately equal to 2β (R_E + r_e) where β is the current gain, r_e is the emitter resistance of one of the input lateral PNPs, and R_E is the resistance of one of the 10 kΩ emitter resistor. Using a DC beta of 100 and the normal temperature dependent expression for r_e gives:

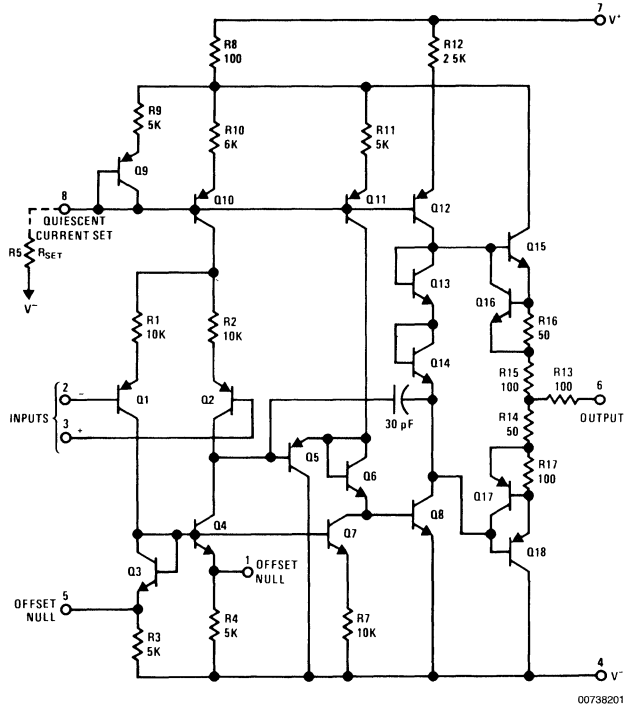


FIGURE 1. LM4250 Schematic Diagram

Circuit Description LM4250

(Continued)

$$R_{IN} \approx 2\,M\Omega + 2\frac{kT}{qI_B} \quad (1)$$

where I_B is input bias current. At room temperature this formula becomes:

$$R_{IN} \approx 2\,M\Omega + \frac{52\,mV}{I_B} \quad (2)$$

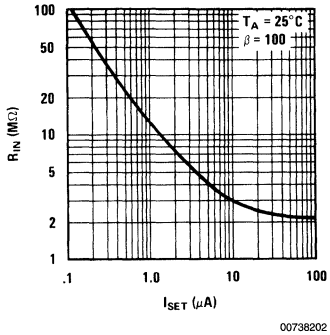


FIGURE 2. Input Resistance vs I_{SET}

Figure 2 gives a typical plot of R_{IN} vs I_{set} derived from the above equation.

Continuing with the circuit description, Q_6 level shifts downward to the base of Q_8 which is the second stage amplifier. Q_8 is run as a common emitter amplifier with a current source load (Q_{12}) to provide maximum gain. The output of Q_8 drives the class B complementary output stage composed of Q_{15} and Q_{18}.

The bias current levels in the LM4250 are set by the amount of current (I_{set}) drawn out of Pin 8. The constant current sources Q_{10}, Q_{11}, and Q_{12} are controlled by the amount of I_{set} current through the diode connected transistor Q_9 and resistor R_9. The constant collector current from Q_{10} biases the differential input stage. Therefore, the level Q_{10} is set at will control such amplifier characteristics as input bias current, input resistance, and amplifier slew rate. Current source Q_{11} biases Q_5 and Q_6. The current ratio between Q_5 and Q_6 is controlled by constant current sink Q_7. Current source Q_{12} sets the currents in diodes Q_{13} and Q_{14} which bias the output stage to the verge of conduction thereby eliminating the dead zone in the class B output. Q_{12} also acts as the load for Q_8 and limits the drive current to Q_{15}.

The output current limiting is provided by Q_{16} and Q_{17} and their associated resistors R_{16} and R_{17}. When enough current is drawn from the output, Q_{16} turns on and limits the base drive of Q_{15}. Similarly Q_{17} turns on when the LM4250 attempts to sink too much current, limiting the base drive of Q_{18} and therefore output current. Frequency compensation is provided by the 30 pF capacitor across the second stage amplifier, Q_8, of the LM4250. This provides a 6 dB per octave rolloff of the open loop gain.

Bias Current Setting Procedure

The single set resistor shown in *Figure 3a* offers the most straightforward method of biasing the LM4250. When the set resistor is connected from Pin 8 to ground the resistance value for a given set current is:

$$R_{SET} = \frac{V^+ - 0.5}{I_{SET}} \quad (3)$$

The 0.5 volts shown in Equation 3 is the voltage drop of the master bias current diode connected transistor on the integrated circuit chip. In applications where the regulation of the V^+ supply with respect to the V^- supply (as in the case of tracking regulators) is better than the V^+ supply with respect to ground the set resistor should be connected from Pin 8 to V^-. R_{SET} is then:

$$R_{SET} = \frac{V^+ + |V^-| - 0.5}{I_{SET}} \quad (4)$$

The transistor and resistor scheme shown in *Figure 3b* allows one to switch the amplifier off without disturbing the main V^+ and V^- power supply connections. Attaching C_1 across the circuit prevents any switching transient from appearing at the amplifier output. The dual scheme shown in *Figure 3c* has a constant set current flowing through R_{S1} and a variable current through R_{S2}. Transistor Q_2 acts as an emitter follower current sink whose value depends on the control voltage V_c on the base. This circuit provides a method of varying the amplifier's characteristics over a limited range while the amplifier is in operation. The FET circuit shown in *Figure 3d* covers the full range of set currents in response to as little as a 0.5V gate potential change on a low pinch-off voltage FET such as the 2N3687. The limit resistor prevents excessive current flow out of the LM4250 when the FET is fully turned on.

Bias Current Setting Procedure (Continued)

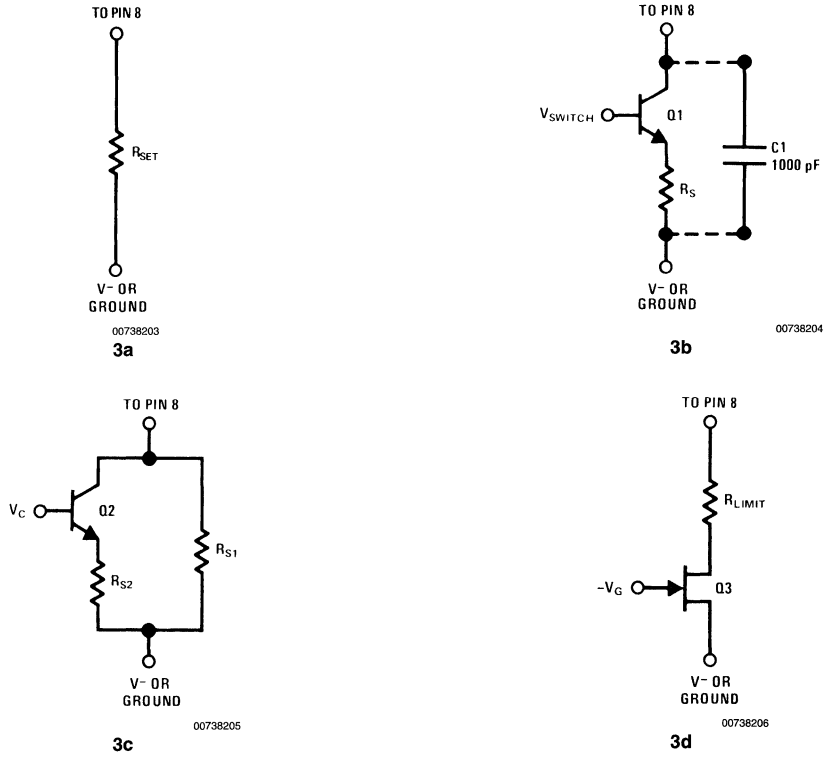


FIGURE 3. Biasing Schemes

Frequency Response of a Programmable Op Amp

This section provides a method of determining the sine and step voltage response of a programmable op amp. Both the sine and step voltage responses of an amplifier are modified when the rate of change of the output voltage reaches the slew rate limit of the amplifier. The following analysis develops the Bode plot as well as the small signal and slew rate limited responses of an amplifier to these two basic categories of waveforms.

Small Signal Sine Wave Response

The key to constructing the Bode plot for a programmable op amp is to find the gain bandwidth product, GBWP, for a given set current. Quiescent power drain, input bias current, or slew rate considerations usually dictate the desired set current. The data sheet curve relating GBWP to set current provides the value of GBWP which when divided by one yields the unity gain crossover of f_u. Assuming a set current of 6 µA gives a GBWP of 200,000 Hz and therefore an f_u of 200 kHz for the example shown in *Figure 4*. Since the device has a single dominant pole, the rolloff slope is –20 dB of gain per decade of frequency (–6 dB/octave). The dotted line shown on *Figure 4* has this slope and passes through the 200 kHz f_u point. Arbitrarily choosing an inverting amplifier with a closed loop gain magnitude of 50 determines the height of the 34 dB horizontal line shown in *Figure 4*. Graphically finding the intersection of the sloped line and the horizontal line or mathematically dividing GBWP by 50 determines the 3 dB down frequency of 4 kHz for the closed loop response of this amplifier configuration. Therefore, the amplifier will now apply a gain of –50 to all small signal sine waves at frequencies up to 4 kHz. For frequencies above 4 kHz, the gain will be as shown on the sloped portion of the Bode plot.

Small Signal Sine Wave Response

(Continued)

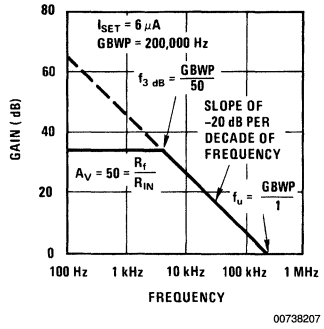


FIGURE 4. Bode Plot

Small Signal Step Input Response

The amplifier's response to a positive step voltage change at the input will be an exponentially rising waveform whose rise time is a function of the closed loop 3 dB down bandwidth of the amplifier. The amplifier may be modeled as a single pole low pass filter followed by a gain of 50 wideband amplifier. From basic filter theory*, the 10% to 90% rise time of a single pole low pass filter is:

$$t_r = \frac{0.35}{f_{3\ dB}} \tag{5}$$

For the example shown in *Figure 4* the 4 kHz 3 dB down frequency would give a rise time of 87.5 μs.

Note: *See reference

Slew Rate Limited Large Signal Response

The final consideration, which determines the upper speed limitation on the previous two types of signal responses, is the amplifier slew rate. The slew rate of an amplifier is the maximum rate of change of the output signal which the amplifier is capable of delivering. In the case of sinusoidal signals, the maximum rate of change occurs at the zero crossing and may be derived as follows:

$$V_O = V_p \sin 2\pi f t \tag{6}$$

$$\frac{d V_O}{d t} = 2\pi f V_p \cos 2\pi f t \tag{7}$$

$$\left.\frac{d V_O}{d t}\right|_{t=o} = 2\pi f V_p \tag{8}$$

$$S_r = 2\pi f_{MAX} V_P \tag{9}$$

where:

V_O = output voltage

V_p = peak output voltage

S_r = maximum $\frac{d V_O}{dt}$

The maximum sine wave frequency an amplifier with a given slew rate will sustain without causing the output to take on a triangular shape is therefore a function of the peak amplitude of the output and is expressed as:

$$f_{MAX} = \frac{S_r}{2\pi V_p} \tag{10}$$

Figure 5 shows a quick reference graphical presentation of this formula with the area below any V_{peak} line representing an undistorted small signal sine wave response for a given frequency and amplifier slew rate and the area above the V_{peak} line representing a distorted sine wave response due to slew rate limiting for a sine wave with the given V_{peak}.

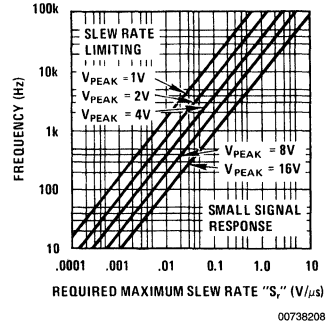


FIGURE 5. Frequency vs Slew Rate Limit vs Peak Output Voltage

Large signal step voltage changes at the output will have a rise time as shown in equation 5 until a signal with a rate of output voltage change equal to the slew rate of the amplifier occurs. At this point the output will become a ramp function with a slope equal to S_r. This action occurs when:

Slew Rate Limited Large Signal Response (Continued)

$$S_r \leq \frac{V_{step}}{t_r} \tag{11}$$

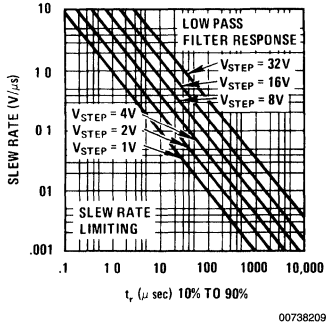


FIGURE 6. Slew Rate vs Rise Time vs Step Voltage

Figure 6 graphically expresses this formula and shows the maximum amplitude of undistorted step voltage for a given slew rate and rise time. The area above each step voltage line represents the undistorted low pass filter type response mode of the amplifier. If the intersection of the rise time and slew rate values of a particular amplifier configuration falls below the expected step voltage amplitude line, the rise time will be determined by the slew rate of the amplifier. The rise time will then be equal to the amplitude of the step divided by the slew rate S_r.

Full Power Bandwidth

The full power bandwidth often found on amplifier specification sheets is the range of frequencies from zero to the frequency found at the intersection on *Figure 5* of the maximum rated output voltage and the slew rate S_r of the amplifier. Mathematically this is:

$$f_{full\ power} = \frac{S_r}{2\pi V_{rated}} \tag{12}$$

The full power bandwidth of a programmable amplifier such as the LM4250 varies with the master bias set current.

The above analysis of sine wave and step voltage amplifier responses applies for all single dominant pole op amps such as the LM101A, LM1107, LM108A, LM112, LM118, and LM741 as well as the LM4250 programmable op amp.

500 Mano-Watt X10 Amplifier

The X10 inverting amplifier shown in *Figure 7* demonstrates the low power capability of the LM4250 at extremely low values of supply voltage and set current. The circuit draws 260 nA from the +1.0V supply of which 50 nA flows through the 12 MΩ set resistor. The current into the −1.0V supply is only 210 nA since the set resistor is tied to ground rather than V^-. Total quiescent power dissipation is:

$$P_D = (260\ nA)\ (1V) + (210\ nA)\ (1V) \tag{13}$$

$$P_D = 470\ nW \tag{14}$$

The slew rate determined from the data sheet typical performance curve is 1 V/ms for a .05 μA set current. Samples of actual values observed were 1.2 V/ms for the negative slew rate and 0.85 V/ms for the positive slew rate. This difference occurs due to the non-symmetry in the current sources used for charging and discharging the internal 30 pF compensation capacitor.

The 3 dB down (gain of −7.07) frequency observed for this configuration was approximately 300 Hz which agrees fairly closely with the 3.5 kHz GBWP divided by 10 taken from an extrapolation of the data sheet typical GBWP versus set current curve.

Peak-to-peak output voltage swing into a 100 kΩ load is 0.7V or ±0.35V peak. An increase in supply voltage to ±1.35V such as delivered by a pair of mercury cells directly increases the output swing by ±0.35V to 1.4V peak-to-peak. Although this increases the power dissipation to approximately 1 μW per battery, a power drain of 15 μW or less will not affect the shelf life of a mercury cell.

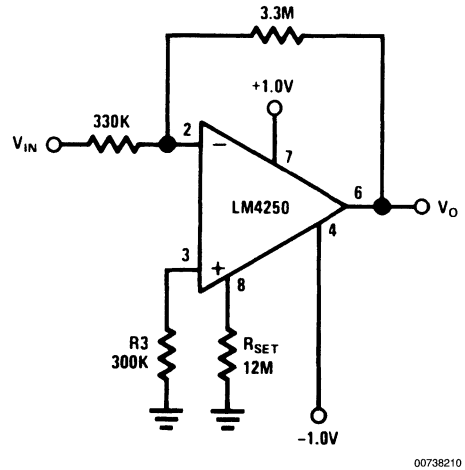


FIGURE 7. 500 nW x 10 Amplifier

Micro-Power Monitor with High Current Switch

Figure 8 shows the combination of a micro-power comparator and a high current switch run from a separate supply. This circuit provides a method of continuously monitoring an input voltage while dissipating only 100 μW of power and still being capable of switching a 500 mA load if the input exceeds a given value. The reference voltage can be any value between +8.5V and −8.5V. With a minimum gain of approximately 100,000 the comparator can resolve input voltage differences down into the 0.2 mV region.

Micro-Power Monitor with High Current Switch (Continued)

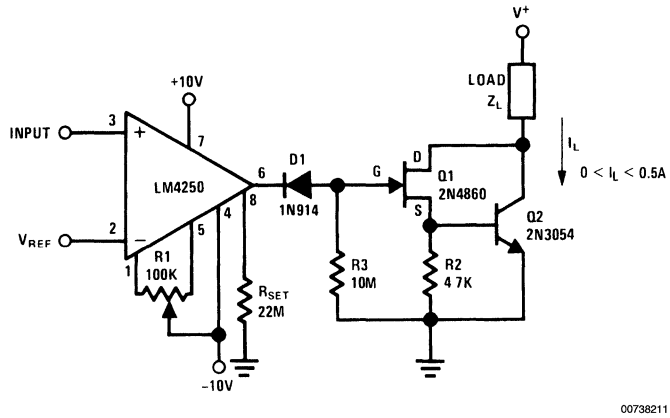


FIGURE 8. μ–Power Comparator with High Current Switch

The bias current for the LM4250 shown in *Figure 8* is set at 0.44 μA by the 200 MΩ R_{set} resistor. This results in a total comparator power drain of 100 μW and a slew rate of approximately 11 V/ms in the positive direction and 12.8 V/ms in the negative direction. Potentiometer R_1 provides input offset nulling capability for high accuracy applications. When the input voltage is less than the reference voltage, the output of the LM4250 is at approximately −9.5V causing diode D_1 to conduct. The gate of Q_1 is held at −8.8V by the voltage developed across R_3. With a large negative voltage on the gate of Q_1 it turns off and removes the base drive from Q_2. This results in a high voltage or open switch condition at the collector of Q_2. When the input voltage exceeds the reference voltage, the LM4250 output goes to +9.5V causing D_1 to be reverse biased. Q_1 turns on as does Q_2, and the collector of Q_2 drops to approximately 1V while sinking the 500 mA of load current.

The load denoted as Z_L can be resistor, relay coil, or indicator lamp as required; but the load current should not exceed 500 mA. For V^+ values of less than 15V and I_L values of less than 25 mA both Q_2 and R_2 may be omitted. With only the 2N4860 JFET as an output device the circuit is still capable of driving most common types of indicator lamps.

IC Meter Amplifier Runs on Two Flashlight Batteries

Meter amplifiers normally require one or two 9V transistor batteries. Due to the heavy current drain on these supplies, the meters must be switched to the OFF position when not in use. The meter circuit described here operates on two 1.5V flashlight batteries and has a quiescent power drain so low that no ON-OFF switch is needed. A pair of Eveready No. 950 "D" cells will serve for a minimum of one year without replacement. As a DC ammeter, the circuit will provide current ranges as low as 100 nA full-scale.

The basic meter amplifier circuit shown in *Figure 9* is a current-to-voltage converter. Negative feedback around the amplifier insures that currents I_{IN} and I_f are always equal, and the high gain of the op amp insures that the input voltage between Pins 2 and 3 is in the microvolt region. Output

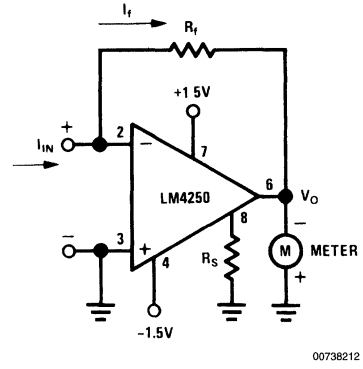


FIGURE 9. Basic Meter Amplifier

voltage V_o is therefore equal to $-I_fR_f$. Considering the ±1.5V sources (±1.2V end-of-life) a practical value of V_o for full scale meter deflection is 300 mV. With the master bias-current setting resistor (R_s) set at 10 MΩ, the total quiescent current drain of the circuit is 0.6 μA for a total power supply drain of 1.8 μW. The input bias current, required by the amplifier at this low level of quiescent current, is in the range of 600 pA.

The Complete Nanoammeter

The complete meter amplifier shown in *Figure 10* is a differential current-to-voltage converter with input protection, zeroing and full scale adjust provisions, and input resistor balancing for minimum offset voltage. Resistor R'_f (equal in value to R_f for measurements of less than 1 μA) insures that

The Complete Nanoammeter

(Continued)

the input bias currents for the two input terminals of the amplifier do not contribute significantly to an output error voltage. The output voltage V_o for the differential current-to-voltage converter is equal to $-2\ I_f R_f$ since the floating input current I_{IN} must flow through R_f and R'_f. R'_f may

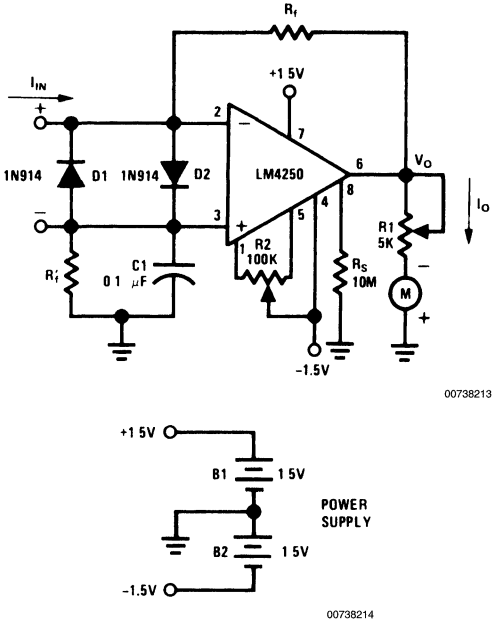


FIGURE 10. Complete Meter Amplifier

Resistance Values for DC Nano and Micro Ammeter

I FULL SCALE	$R_{f\ [\Omega]}$	$R'_{f\ [\Omega]}$
100 nA	1.5M	1.5M
500 nA	300k	300k
1 µA	300k	0
5 µA	60k	0
10 µA	30k	0
50 µA	6k	0
100 µA	3k	0

be omitted for R_f values of 500 kΩ or less, since a resistance of this value contributes an error of less than 0.1% in output voltage. Potentiometer R_2 provides an electrical meter zero by forcing the input offset voltage V_{os} to zero. Full scale meter deflection is set by R_1. Both R_1 and R_2 only need to be set once for each op amp and meter combination. For a 50 microamp 2 kΩ meter movement, R_1 should be about 4 kΩ to give full scale meter deflection in response to a 300 mV output voltage. Diodes D_1 and D_2 provide full input protection for overcurrents up to 75 mA.

With an R_f resistor value of 1.5M the circuit in *Figure 10* becomes a nanommeter with a full scale reading capability of 100 nA. Reducing R_f to 3 kΩ in steps, as shown in *Figure 10* increases the full scale deflection to 100 µA, the maximum for this circuit configuration. The voltage drop across the two input terminals is equal to the output voltage V_o divided by the open loop gain. Assuming an open loop gain of 10,000 gives an input voltage drop of 30 µV or less.

Circuit for Higher Current Readings

For DC current readings higher than 100 µA, the inverting amplifier configuration shown in *Figure 11* provides the required gain. Resistor R_A develops a voltage drop in response to input current I_A. This voltage is amplified by a factor equal to the ratio of R_f/R_B. R_B must be sufficiently larger than R_A, so as not to load the input signal. *Figure 11* also shows the proper values of R_A, R_B and R_f for full scale meter deflections of from 1 mA to 10A.

Resistance Values for DC Ammeter

I FULL SCALE	$R_A\ [\Omega]$	$R_B\ [\Omega]$	$R_f\ [\Omega]$
1 mA	3.0	3k	300k
10 mA	.3	3k	300k
100 mA	.3	30k	300k
1A	.03	30k	300k
10A	.03	30k	30k

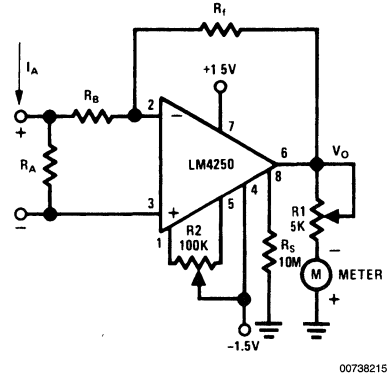


FIGURE 11. Ammeter

A 10 mV to 100V Full-Scale Voltmeter

A resistor inserted in series with one of the input leads of the basic meter amplifier converts it to a wide range voltmeter circuit, as shown in *Figure 12*. This inverting amplifier has a gain varying from −30 for the 10 mV full scale range to −0.003 for the 100V full scale range. *Figure 12* also lists the proper values of R_v, R_f, and R'_f for each range. Diodes D_1 and D_2 provide complete amplifier protection for input overvoltages as high as 500V on the 10 mV range, but if overvoltages of this magnitude are expected under continuous operation, the power rating of R_v should be adjusted accordingly.

A 10 mV to 100V Full-Scale Voltmeter (Continued)

Resistance Values for a DC Voltmeter

V FULL SCALE	R_V [Ω]	R_f [Ω]	R'_f [Ω]
10 mV	100k	1.5M	1.5M
100 mV	1M	1.5M	1.5M
1V	10M	1.M	1.5M
10V	10M	300k	0
100V	10M	30k	0

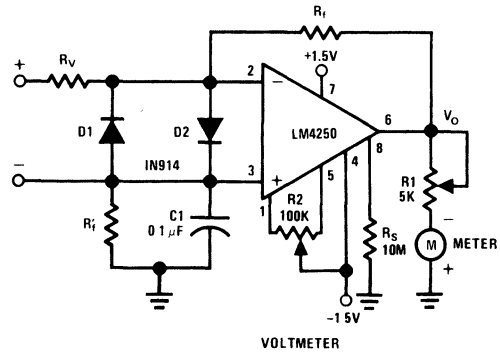


FIGURE 12. Voltmeter

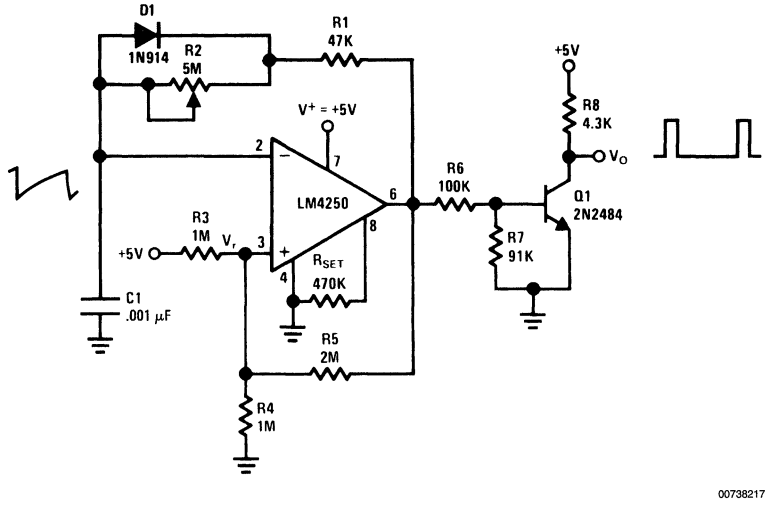


FIGURE 13. Pulse Generator

Low Frequency Pulse Generator Using a Single +5V Supply

The variable frequency pulse generator shown in *Figure 13* provides an example of the LM4250 operated from a single supply. The circuit is a buffered output free running multivibrator with a constant width output pulse occurring with a frequency determined by potentiometer R_2.

The LM4250 acts as a comparator for the voltages found at the upper plate of capacitor C_1 and at the reference point denoted as V_r on *Figure 13*. Capacitor C_1 charges and discharges with a peak-to-peak amplitude of approximately 1V determined by the shift in reference voltage V_r at Pin 3 of the op amp. The charge path of C_1 is from the amplifier output, which is at its maximum positive voltage V_{HIGH} (approximately $V^+ - 0.5V$), through R_1 and through the potentiometer R_2. Diode D_1 is reverse biased during the charge period. When C_1 charges to the V_r value determined by the net result of V_{HIGH} through resistor R_5 and V^+ through the voltage divider made up of resistors R_3 and R_4 the amplifier swings to its lower limit of approximately 0.5V causing C_1 to begin discharging. The discharge path is through the forward biased diode D_1, through resistor R_1, and into Pin 6 of the op amp. Since the impedance in the discharge path does not vary for R_2 settings of from 3 kΩ to 5 MΩ, the output pulse maintains a constant pulse width of 41 μs ±1.5 μs over this range of potentiometer settings. *Figure 14* shows the output pulse frequency variation from 6 kHz down to 360 Hz as R_2 places from 100 kΩ up to 5 MΩ of additional resistance in the charge path of C_1. Setting R_2 to zero ohms will short out diode D_1 and cause a symmetrical square wave output at a frequency of 10 kHz. Increasing the value of C_1 will lower the range of frequencies available in response to the R_2 variation shown on *Figure 14*. Electrolytic capacitors may be used for the larger values of C_1 since it has only positive voltages applied to it.

The output buffer Q_1 presents a constant load to the op amp output thereby preventing frequency variations caused by

Low Frequency Pulse Generator Using a Single +5V Supply (Continued)

V_{HIGH} and V_{LOW} voltages changing as a function of load current. The output of Q_1 will interface directly with a standard TTL or DTL logic device. Reversing diode D1 will invert the polarity of the generator output providing a series of negative going pulses dropping from +5V to the saturation voltage of Q_1.

The change in output frequency as a function of supply voltage is less than ±4% for a V^+ change of from 4V to 10V. This stability of frequency versus supply voltage is due to the fact that the reference voltage V_r and the drive voltage for the capacitor are both direct functions of V^+.

The power dissipation of the free running multivibrator is 300 µW and the power dissipation of the buffer circuit is approximately 5.8 mW.

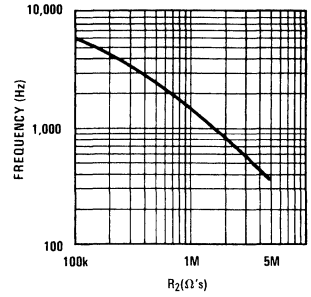
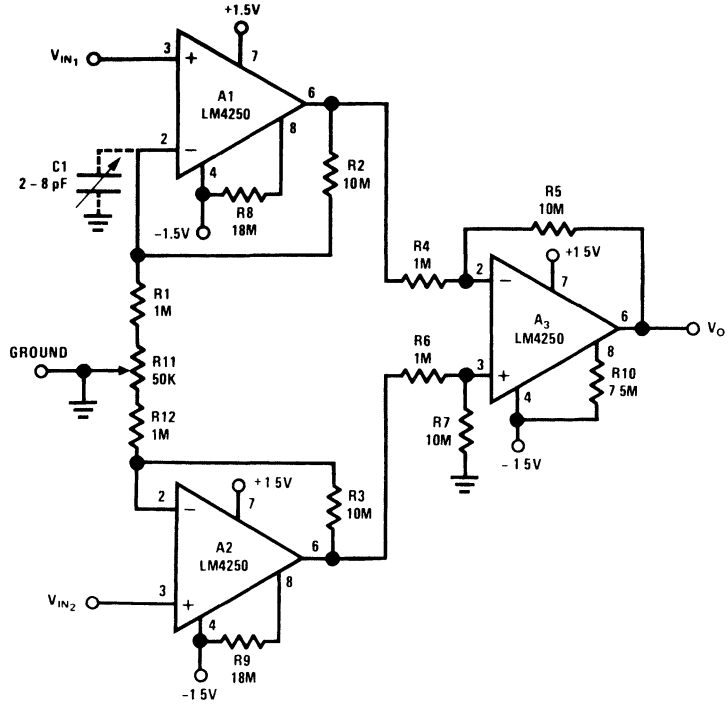


FIGURE 14. Pulse Frequency vs R_2



Notes:

Quiescent P_D = 10 µW

R2, R3, R4, R5, R6 and R7 are 1% resistors

R11 and C1 are for DC and AC common mode rejection adjustments

FIGURE 15. x 100 Instrumentation Amplifier

X100 Instrumentation Amplifier

The instrumentation amplifier circuit shown in *Figure 15* has a full differential input center tapped to ground. With the bias current set at approximately 0.1 µA, the impedance looking into either V_{IN1} or V_{IN2} is 100 MΩ with respect to ground, and the input bias current at either terminal is 0.2 nA. The two non-inverting input stages A_1 and A_2 apply a gain of 10 to the input signal, and the differential output stage applies an additional gain of −10 for a net amplifier gain of −100:

$$V_O = -100(V_{IN1} - V_{IN2}). \quad (15)$$

The entire circuit can run from two 1.5V batteries connected directly (no power switch) to the V^+ and V^- terminals. With a

X100 Instrumentation Amplifier

(Continued)

total current drain of 2.8 µA the quiescent power dissipation of the circuit is 8.4 µW. This is low enough to have no significant effect on the shelf life of most batteries.

Potentiometer R_{11} provides a means for matching the gains of A_1 and A_2 to achieve maximum DC common mode rejection ratio CMRR. With R_{11} adjusted to its null point for DC common mode rejection the small AC CMRR trimmer capacitor C_1 will normally give an additional 10 to 20 dB of CMRR over the operating frequency range. Since C_1 actually balances wiring capacitance rather than amplifier frequency characteristics, it may be necessary to attach it to Pin 2 of either A_1 or A_2 as required. *Figure 16* shows the variation of CMRR (referred to the input) with frequency for this configuration. Since the circuit applies a gain of 100 or 40 dB to an input signal, the actual observed rejection ratio

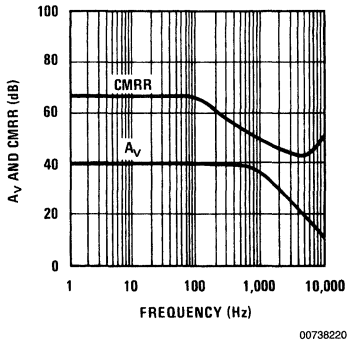


FIGURE 16. A_V and CMRR vs Frequency

is the difference between the CMRR curve and A_V curve. For example, a 60 Hz common mode signal will be attenuated by 67 dB minus 40 db or 27 dB for an actual rejection ratio of V_{IN}/V_O equal to 22.4.

The maximum peak-to-peak output signal into a 100 kΩ load resistor is approximately 1.8V. With no input signal, the noise seen at the output is approximately 0.8 mV_{RMS} or 8 μV_{RMS} referred to the input. When doing power dissipation measurements on this circuit, it should be kept in mind that even a 1 MΩ oscilloscope probe placed between +1.5V and −1.5V will more than double the power drawn from the batteries.

5V Regulator for Cmos Logic Circuits

The ideal regulator for low power CMOS logic elements should dissipate essentially no power when the CMOS devices are running at low frequencies, but be capable of delivering full output power on demand when the CMOS devices are running in the 0.1 MHz to 10 MHz region. With a 10V input voltage, the regulator shown in *Figure 17* will dissipate 350 µW in the stand-by mode but will deliver up to 50 mA of continuous load current when required.

The circuit is basically a boosted output voltage-follower referenced to a low current zener diode. The voltage divider consisting of R_2 and R_3 provides a 5V tap voltage from the 6.5V reference diode to determine the regulator output. Since a standard 6.5V zener diode does not exhibit good regulation in the 2 µA to 60 µA reverse current region, Q_2 must be a special device. An NPN transistor with its collector and base terminals grounded and its emitter tied to the junction of R_1 and R_2 exhibits a well-controlled base emitter reverse breakdown voltage. A National Semiconductor process 25 small signal NPN transistor sorted to a 2N registration such as 2N3252 has a BV_{EBO} at 10 µA specified as 5.5V minimum, 6.5V typical, and 7.0V maximum. Using a diode connected 2N3252 as a reference, the regulator output voltage changed 78 mV in response to an 8V to 36V change in the input voltage. This test was done under both no load and full load conditions and represents a line regulation of better than 1.6%.

A load change from 10 µA to 50 mA caused a 1 mV change in output voltage giving a load regulation value of 0.05%. When operating the regulator at load currents of less than 25 mA, no heat sink is required for Q_1. For load currents in excess of 50 mA, Q_1 should be replaced by a Darlington pair with the 2N3019 acting as a driver for a higher power device such as a 2N3054.

References

Millman, J. and Halkias, C.C.: *"Electronic Device and Circuits,"* pp. 465–466, McGraw-Hill Book Company, New York, 1967.

References (Continued)

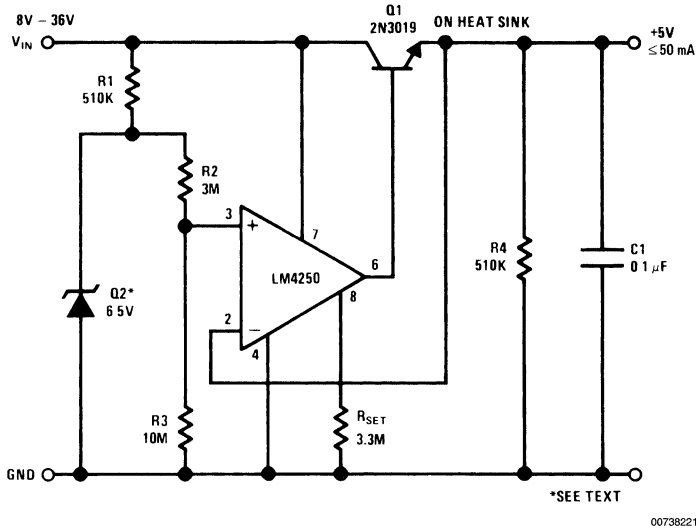


FIGURE 17. 350 µW Quiescent Drain 5 Volt Regulator

Noise Specs Confusing?

National Semiconductor
Application Note 104
George Cleveland

It's really all very simple—once you understand it. Then, here's the inside story on noise for those of us who haven't been designing low noise amplifiers for ten years.

You hear all sorts of terms like signal-to-noise ratio, noise figure, noise factor, noise voltage, noise current, noise power, noise spectral density, noise per root Hertz, broadband noise, spot noise, shot noise, flicker noise, excess noise, I/F noise, fluctuation noise, thermal noise, white noise, pink noise, popcorn noise, bipolar spike noise, low noise, no noise, and loud noise. No wonder not everyone understands noise specifications.

In a case like noise, it is probably best to sort it all out from the beginning. So, in the beginning, there was noise; and then there was signal. The whole idea is to have the noise very small compared to the signal; or, conversely, we desire a high signal-to-noise ratio S/N. Now it happens that S/N is related to noise figure NF, noise factor F, noise power, noise voltage $\bar{e}_n$, and noise current $\bar{i}_n$. To simplify matters, it also happens that any noisy channel or amplifier can be completely specified for noise in terms of two noise generators $\bar{e}_n$ and $\bar{i}_n$ as shown in *Figure 1*.

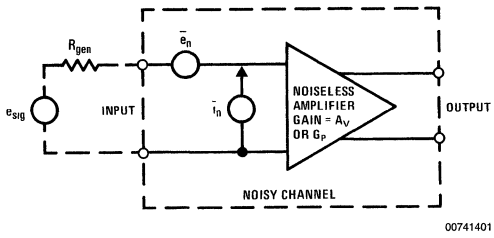


FIGURE 1. Noise Characterization of Amplifier

All we really need to understand are NF, $\bar{e}_n$, and $\bar{i}_n$. So here is a rundown on these three.

NOISE VOLTAGE, $\bar{e}_n$, or more properly, EQUIVALENT SHORT-CIRCUIT INPUT RMS NOISE VOLTAGE is simply that noise voltage which would appear to originate at the input of the noiseless amplifier if the input terminals were shorted. It is expressed in nanovolts per root Hertz $nV/\sqrt{Hz}$ at a specified frequency, or in microvolts in a given frequency band. It is determined or measured by shorting the input terminals, measuring the output rms noise, dividing by amplifier gain, and referencing to the input. Hence the term, equivalent noise voltage. An output bandpass filter of known characteristic is used in measurements, and the measured value is divided by the square root of the bandwidth $\sqrt{B}$ if data is to be expressed per unit bandwidth or per root Hertz.

The level of $\bar{e}_n$ is not constant over the frequency band; typically it increases at lower frequencies as shown in *Figure 2*. This increase is 1/f NOISE.

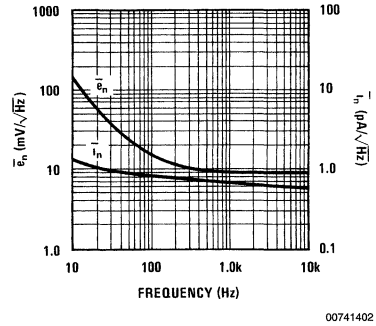


FIGURE 2. Noise Voltage and Current for an Op Amp

NOISE CURRENT, $\bar{i}_n$, or more properly, EQUIVALENT OPEN-CIRCUIT RMS NOISE CURRENT is that noise which occurs apparently at the input of the noiseless amplifier due only to noise currents. It is expressed in picoamps per root Hertz $pA/\sqrt{Hz}$ at a specified frequency or in nanoamps in a given frequency band. It is measured by shunting a capacitor or resistor across the input terminals such that the noise current will give rise to an additional noise voltage which is $\bar{i}_n \times R_{in}$ (or X_{cin}). The output is measured, divided by amplifier gain, referenced to input, and that contribution known to be due to $\bar{e}_n$ and resistor noise is appropriately subtracted from the total measured noise. If a capacitor is used at the input, there is only $\bar{e}_n$ and $\bar{i}_n X_{cin}$. The $\bar{i}_n$ is measured with a bandpass filter and converted to

$$pA\sqrt{Hz}$$

if appropriate; typically it increases at lower frequencies for op amps and bipolar transistors, but increases at higher frequencies for field-effect transistors.

NOISE FIGURE, NF is the logarithm of the ratio of input signal-to-noise and output signal-to-noise.

$$NF = 10 \text{ Log } \frac{(S/N)_{in}}{(S/N)_{out}} \quad (1)$$

where: S and N are power or (voltage)^2 levels

This is measured by determining the S/N at the input with no amplifier present, and then dividing by the measured S/N at the output with signal source present.

The values of R_{gen} and any X_{gen} as well as frequency must be known to properly express NF in meaningful terms. This is because the amplifier $\bar{i}_n \times Z_{gen}$ as well as R_{gen} itself produces input noise. The signal source in *Figure 1* contains some noise. However e_{sig} is generally considered to be noise free and input noise is present as the THERMAL NOISE of the resistive component of the signal generator impedance R_{gen}. This thermal noise is WHITE in nature as it contains constant NOISE POWER DENSITY per unit bandwidth. It is easily seen from Equation 2 that the $\bar{e}_n^2$ has the units V^2/Hz and that $(\bar{e}_n)$ has the units $V/\sqrt{Hz}$

$$\bar{e}_R^{\,2} = 4kTRB \qquad (2)$$

where: T is the temperature in °K

R is resistor value in Ω

B is bandwidth in Hz

k is Boltzman's constant

Relation Between $\bar{e}_n$, $\bar{i}_n$, NF

Now we can examine the relationship between $\bar{e}_n$ and $\bar{i}_n$ at the amplifier input. When the signal source is connected, the $\bar{e}_n$ appears in series with the e_{sig} and $\bar{e}_R$. The $\bar{i}_n$ flows through R_{gen} thus producing another noise voltage of value $\bar{i}_n \times R_{gen}$. This noise voltage is clearly dependent upon the value of R_{gen}. All of these noise voltages add at the input in rms fashion; that is, as the square root of the sum of the squares. Thus, neglecting possible correlation between $\bar{e}_n$ and $\bar{i}_n$, the total input noise is

$$\bar{e}_N^{\,2} = \bar{e}_n^{\,2} + \bar{e}_R^{\,2} + + \bar{i}_n^{\,2}\, R_{gen}^{\,2} \qquad (3)$$

Further examination of the NF equation shows the relationship of $\bar{e}_N$, $\bar{i}_n$, and NF.

$$NF = 10 \log \frac{S_{in} \times N_{out}}{S_{out} \times N_{in}}$$

$$= 10 \log \frac{S_{in}\, G_p\, \overline{e_N^2}}{S_{in}\, G_p\, \overline{e_R^2}}$$

where: G_p = power gain

$$= 10 \log \frac{\overline{e_N^2}}{\overline{e_R^2}}$$

$$= 10 \log \frac{\overline{e_n^2} + \overline{e_R^2} + \overline{i_n^2}\, R_{gen}^2}{\overline{e_R^2}}$$

$$NF = 10 \log \left(1 + \frac{\overline{e_n^2} + \overline{i_n^2}\, R_{gen}^2}{\overline{e_R^2}}\right) \qquad (4)$$

Thus, for small R_{gen}, noise voltage dominates; and for large R_{gen}, noise current becomes important. A clear advantage accrues to FET input amplifiers, especially at high values of R_{gen}, as the FET has essentially zero $\bar{i}_n$. Note, that for an NF value to have meaning, it must be accompanied by a value for R_{gen} as well as frequency.

Calculating Total Noise, $\bar{e}_N$

We can generate a plot of $\bar{e}_N$ for various values of R_{gen} if noise voltage and current are known vs frequency. Such a graph is shown in *Figure 3* drawn from *Figure 2*. To make this plot, the thermal noise $\bar{e}_R$ of the input resistance must be calculated from Equation 2 or taken from the graph of *Figure 4*. Remember that each term in Equation 3 must be squared prior to addition, so the data from *Figure 4* and from *Figure 2* is squared. A sample of this calculation follows:

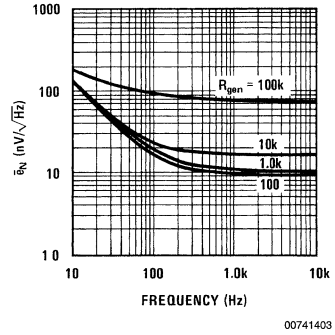


FIGURE 3. Total Noise for the Op Amp of *Figure 2*

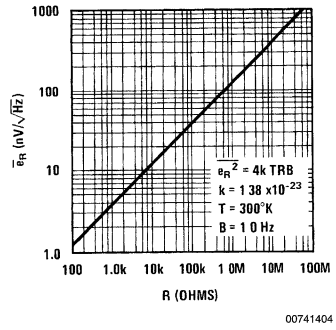


FIGURE 4. Thermal Noise of Resistor

Example 1: Determine total equivalent input noise per unit bandwidth for an amplifier operating at 1 kHz from a source resistance of 10 kΩ. Use the data from *Figures 2, 4.*

1. Read $\bar{e}_R$ from *Figure 4* at 10 kΩ; the value is

$$12.7\ nV/\sqrt{Hz}.$$

2. Read $\bar{e}_n$ from *Figure 2* at 1 kHz; the value is

$$9.5\ nV/\sqrt{Hz}.$$

Calculating Total Noise, $\bar{e}_N$ (Continued)

3. Read $\bar{i}_n$ from *Figure 2* at 1 kHz; the value is
   Multiply by 10 kΩ to obtain

$$0.68\ pA/\sqrt{Hz}.$$

$$6.8\ nV/\sqrt{Hz}.$$

4. Square each term individually, and enter into Equation 3.

$$\bar{e}_N = \sqrt{\overline{e_n^2} + \overline{e_R^2} + \overline{i_n^2}\,R_{gen}^2}$$

$$= \sqrt{9.5^2 + 12^2 + 6.8^2} \quad = \sqrt{279}$$

$$\bar{e}_N = 17.4\ nV/\sqrt{Hz}$$

This is total rms noise at the input in one Hertz bandwidth at 1 kHz. If total noise in a given bandwidth is desired, one must integrate the noise over a bandwidth as specified. This is most easily done in a noise measurement set-up, but may be approximated as follows:

1. If the frequency range of interest is in the flat band; i e., between 1 kHz and 10 kHz in *Figure 2*, it is simply a matter of multiplying $\bar{e}_N$ by the square root of the bandwidth. Then, in the 1 kHz–10 kHz band, total noise is

$$\bar{e}_N = 17.4\sqrt{9000}$$
$$= 1.65\ \mu V$$

2. If the frequency band of interest is not in the flat band of *Figure 2*, one must break the band into sections, calculating average noise in each section, squaring, multiplying by section bandwidth, summing all sections, and finally taking square root of the sum as follows:

$$\bar{e}_N = \sqrt{\overline{e_R^2}B + \sum_{1}^{i} (\overline{e_n^2} + \overline{i_n^2}\,R_{gen}^2)_i\,B_i} \qquad (5)$$

where: i is the total number of sub-blocks.

For most purposes a sub-block may be one or two octaves. Example 2 details such a calculation.

Example 2: Determine the rms noise level in the frequency band 50 Hz to 10 kHz for the amplifier of *Figure 2* operating from R_{gen} = 2k.

1. Read $\bar{e}_R$ from *Figure 4* at 2k, square the value, and multiply by the entire bandwidth. Easiest way is to construct a table as shown on the next page.
2. Read the median value of $\bar{e}_n$ in a relatively small frequency band, say 50 Hz–100 Hz, from *Figure 2*, square it and enter into the table.
3. Read the median value of $\bar{i}_n$ in the 50 Hz–100 Hz band from *Figure 2*, multiply by R_{gen} = 2k, square the result and enter in the table.
4. Sum the squared results from steps 2 and 3, multiply the sum by Δf = 100–50 = 50 Hz, and enter in the table.
5. Repeat steps 2–4 for band sections of 100 Hz–300 Hz, 300 Hz–1000 Hz and 1 kHz–10 kHz. Enter results in the table.
6. Sum all entires in the last column, and finally take the square root of this sum for the total rms noise in the 50 Hz–10,000 Hz band.
7. Total $\bar{e}_n$ is 1.62 μV in the 50 Hz–10,000 Hz band.

Calculating S/N and NF

Signal-to-noise ratio can be easily calculated from known signal levels once total rms noise in the band is determined. Example 3 shows this rather simple calculation from Equation 6 for the data of Example 2.

$$S/N = 20 \log \frac{e_{sig}}{\bar{e}_N} \qquad (6)$$

Example 3: Determine S/N for an rms e_{sig} = 4 mV at the input to the amplifier operated in Example 2.

1. RMS signal is e_{sig} = 4 mV
2. RMS noise from Example 2 is 1.62 μV
3. Calculate S/N from Equation 6

$$S/N = 20 \log \frac{4\ mV}{1.62\ \mu V}$$

$$= 20 \log (2.47 \times 10^3)$$
$$= 20 (\log 10^3 + \log 2.47)$$
$$= 20 (3 + 0.393)$$
$$S/N = 68\ dB$$

It is also possible to plot NF vs frequency at various R_{gen} for any given plot of $\bar{e}_n$ and $\bar{i}_n$. However there is no specific all-purpose conversion plot relating NF, $\bar{e}_n$, $\bar{i}_n$, R_{gen} and f. If either $\bar{e}_n$ or $\bar{i}_n$ is neglected, a reference chart can be constructed. *Figure 5* is such a plot when only $\bar{e}_n$ is considered. It is useful for most op amps when R_{gen} is less than about 200Ω and for FETs at any R_{gen} (because there is no significant $\bar{i}_n$ for FETs), however actual NF for op amps with R_{gen} > 200Ω is higher than indicated on the chart. The graph of *Figure 5* can be used to find spot NF if $\bar{e}_n$ and R_{gen} are known, or to find $\bar{e}_n$ if NF and R_{gen} are known. It can also be used to find max R_{gen} allowed for a given max NF when $\bar{e}_n$ is known. In any case, values are only valid if $\bar{i}_n$ is negligible and at the specific frequency of interest for NF and e_n, and for 1 Hz bandwidth. If bandwidth increases, the plot is valid so long as $\bar{e}_n$ is multiplied by $\sqrt{B}$.

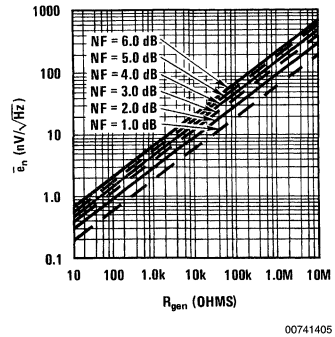


FIGURE 5. Spot NF vs R_{gen} when Considering *Only* $\bar{e}_n$ and $\bar{e}_R$ (not valid when $\bar{i}_n$ R_{gen} is significant)

The Noise Figure Myth

Noise figure is easy to calculate because the signal level need not be specified (note that e_{sig} drops out of Equation 4) Because NF is so easy to handle in calculations, many designers tend to lose sight of the fact that signal-to-noise ratio $(S/N)_{out}$ is what is important in the final analysis, be it an audio, video, or digital data system One can, in fact, choose a high R_{gen} to reduce NF to near zero if $\bar{i}_n$ is very small. In this case e_R is the major source of noise, overshadowing $\bar{e}_n$ completely. The result is very low NF, but very low S/N as well because of very high noise. Don't be fooled into believing that low NF means low noise *per se*!

Another term is worth considering, that is optimum source resistance R_{OPT} This is a value of R_{gen} which produces the lowest NF in a given system. It is calculated as

$$R_{OPT} = \frac{\bar{e}_n}{\bar{i}_n} \qquad (7)$$

This has been arrived at by differentiating Equation 4 with respect to R_{gen} and equating it to zero (see Appendix). *Note that this does not mean lowest noise.*

For example, using *Figure 2* to calculate R_{OPT} at say 600 Hz,

$$R_{OPT} = \frac{10\ nV}{0\ 7\ pA} = 14\ k\Omega$$

TABLE 1. Noise Calculations for Example 2

B (Hz)	Δf (Hz)	$\bar{e}_n2$ (nV/Hz)	+ $\bar{i}_n2\ R_{gen}2$			SUM x Δf	=	(nV^2)
50–100	50	$(20)^2 = 400$	$(8.7 \times 2.0k)^2$	=	302	702* x 50		35,000
100–300	200	$(13)^2 = 169$	$(8 \times 2.0k)^2$	=	256	425 x 200		85,000
300–1000	700	$(10)^2 = 100$	$(7 \times 2.0k)^2$	=	196	296 x 700		207,000
1.0k–10k	9000	$(9)^2 = 81$	$(6 \times 2\ 0k)^2$	=	144	225 x 9000		2,020,000
50–10,000	9950	$\bar{e}_R2 = (5.3)^2 = 28$				28 x 9950		279,000
Total $\bar{e}_N = \sqrt{2,626,000}$		= 1620 nV = 1.62 μV						

*The units are as follows $(20\ nV/\sqrt{Hz})^2 = 400\ (nV)^2/Hz$
$(8\ 7\ pA/\sqrt{Hz} \times 2.0\ k\Omega)^2 = (17\ 4\ nA/\sqrt{Hz})^2 = 302\ (nV)^2/Hz$
Sum = 702 $(nV)^2/Hz$ x 50 Hz = 35,000 $(nV)^2$

Then note in *Figure 3*, that $\bar{e}_N$ is in the neighborhood of 20 $nV/\sqrt{Hz}$ for R_{gen} of 14k, while $\bar{e}_N$ = 10 $nV/\sqrt{Hz}$ for R_{gen} = 0–100Ω. STOP! Do not pass GO. Do not be fooled. Using $R_{gen} = R_{OPT}$ does not guarantee lowest noise UNLESS $e_{sig}^2 = kR_{gen}$ as in the case of transformer coupling. When $e_{sig}^2 > kR_{gen}$, as is the case where signal level is proportional to R_{gen} ($e_{sig} = kR_{gen}$), it makes sense to use the highest practical value of R_{gen}. When $e_{sig}^2 < kR_{gen}$, it makes sense to use a value of $R_{gen} < R_{OPT}$. These conclusions are verified in the Appendix.

This all means that it does not make sense to tamper with the R_{gen} of existing signal sources in an attempt to make $R_{gen} = R_{OPT}$. Especially, do not add series resistance to a source for this purpose. It does make sense to adjust R_{gen} in transformer coupled circuits by manipulating turns ratio or to design R_{gen} of a magnetic pick-up to operate with pre-amps where R_{OPT} is known. It does make sense to increase the design resistance of signal sources to match or exceed R_{OPT} so long as the signal voltage increases with R_{gen} in at least the ratio $e_{sig}^2 < 5°C\ R_{gen}$. It does not necessarily make sense to select an amplifier with R_{OPT} to match R_{gen} because one amplifier operating at $R_{gen} = R_{OPT}$ may produce lower S/N than another (quieter) amplifier operating with $R_{gen} \neq R_{OPT}$.

With some amplifiers it is possible to adjust R_{OPT} over a limited range by adjusting the first stage operating current (the National LM121 and LM381 for example). With these, one might increase operating current, varying R_{OPT}, to find a condition of minimum S/N. Increasing input stage current decreases R_{OPT} as $\bar{e}_n$ is decreased and $\bar{i}_n$ is simultaneously increased.

Let us consider one additional case of a fairly complex nature just as a practical example which will point up some factors often overlooked.

Example 4: Determine the S/N *apparent to the ear* of the amplifier of *Figure 2* operating over 50-12,800 Hz when driven by a phonograph cartridge exhibiting R_{gen} = 1350Ω, L_{gen} = 0.5H, and average e_{sig} = 4.0 mVrms. The cartridge is to be loaded by 47k as in *Figure 7*. This is equivalent to using a Shure V15, Type 3 for average level recorded music.

1. Choose sectional bandwidths of 1 octave each, listed in the following table.
2. Read $\bar{e}_n$ from *Figure 2* as average for each octave and enter in the table.
3. Read $\bar{i}_n$ from *Figure 2* as average for each octave and enter in the table.
4. Read $\bar{e}_R$ for the R_{gen} = 1350Ω from *Figure 4* and enter in the table.
5. Determine the values of Z_{gen} at the midpoint of each octave and enter in the table.
6. Determine the amount of $\bar{e}_R$ which reaches the amplifier input; this is

$$\bar{e}_R \frac{R1}{R1 + Z_{gen}}$$

7. Read the noise contribution $\bar{e}_{47k}$ of R1 = 47k from *Figure 4*.
8. Determine the amount of $\bar{e}_{47K}$ which reaches the amplifier input; this is

$$\bar{e}_{47k} \frac{Z_{gen}}{R1 + Z_{gen}}$$

The Noise Figure Myth (Continued)

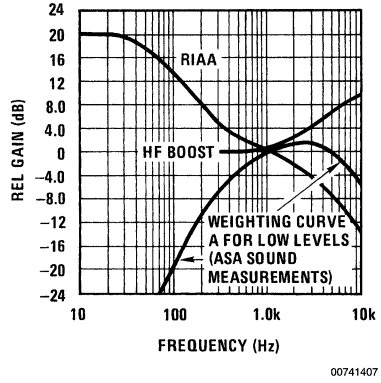


FIGURE 6. Relative Gain for RIAA, ASA Weighting A, and H-F Boost Curves

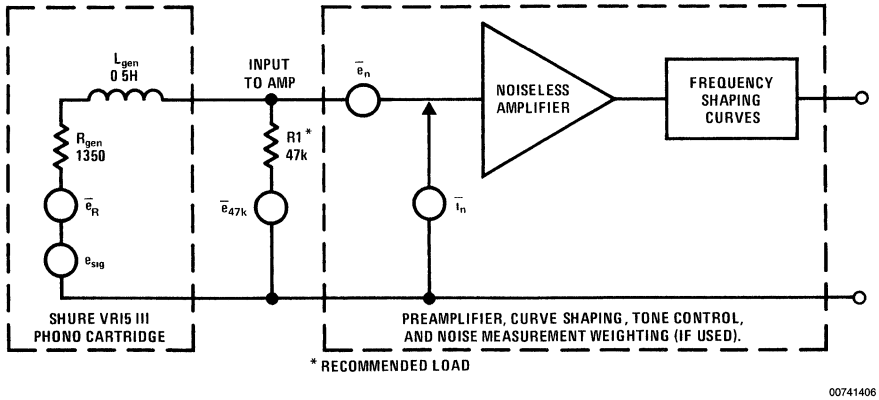


FIGURE 7. Phono Preamp Noise Sources

9. Determine the effective noise contributed by $\bar{i}_n$ flowing through the parallel combination of R1 and Z_{gen}. This is

$$\bar{i}_n \frac{Z_{gen}\, R1}{Z_{gen} + R1}$$

10. Square all noise voltage values resulting from steps 2, 6, 8 and 9; and sum the squares.
11. Determine the relative gain at the midpoint of each octave from the RIAA playback response curve of *Figure 6*.
12. Determine the relative gain at these same midpoints from the A weighted response curve of *Figure 6* for sound level meters (this roughly accounts for variations in human hearing).
13. Assume a tone control high frequency boost of 10 dB at 10 kHz from *Figure 6*. Again determine relative response of octave midpoints.
14. Multiply all relative gain values of steps 11-13 and square the result.
15. Multiply the sum of the squared values from step 10 by the resultant relative gain of step 14 and by the bandwidth in each octave.
16. Sum all the values resultant from step 15, and find the square root of the sum. This is the total audible rms noise apparent in the band.
17. Divide e_{sig} = 4 mV by the total noise to find S/N = 69.4 dB.

Steps for Example

1	Frequency Band (Hz)	50–100	100–200	200–400	400–800	800–1600	1.6–3.2k	3.2–6.4k	6.4–12.8k
	Bandwidth, B (Hz)	50	100	200	400	800	1600	3200	6400
	Bandcenter, f (Hz)	75	150	300	600	1200	2400	4800	9600
5	Z_{gen} at f (Ω)	1355	1425	1665	2400	4220	8100	16k	32k
	Z_{gen} R1 (Ω)	1300	1360	1600	2270	3900	6900	11 9k	19k
	$Z_{gen}(R1 + Z_{gen})$	0.028	0.030	0.034	0.485	0.082	0.145	0.255	0.400
	$R1/(R1 + Z_{gen})$	0.97	0.97	0.97	0.95	0.92	0.86	0.74	0.60
11	RIAA Gain, A_{RIAA}	5.6	3.1	2.0	1.4	1	0.7	0.45	0.316
12	Corr for Hearing, A_A	0.08	0.18	0.45	0.80	1	1.26	1	0.5
13	H-F Boost, A_{boost}	1	1	1	1	1.12	1.46	2 3	3.1
14	Product of Gains, A	0.45	0.55	0.9	1.12	1.12	1.28	1.03	0.49
	A^2	0.204	0.304	0.81	1.26	1.26	1.65	1.06	0.241
4	$\bar{e}_R$ (nV/√Hz)	4.74	4.74	4.74	4.74	4.74	4.74	4.74	4.74
7	$\bar{e}_{47k}$ (nV/√Hz)	29	29	29	29	29	29	29	29
3	$\bar{i}_n$ (pA/√Hz)	0.85	0.80	0.77	0.72	0.65	0.62	0.60	0.60
2	$\bar{e}_n$ (nV/√Hz)	19	14	11	10	9.5	9	9	9
9	$\bar{e}_1 = \bar{i}_n (Z_{gen}\ R1)$	1.1	1.09	1.23	1.63	2.55	4.3	7.1	11.4
6	$\bar{e}_2 = \bar{e}_R\ R1/(R1 + Z_{gen})$	4.35	4.35	4.35	4.25	4.15	3.86	3.33	2.7
8	$\bar{e}_3 = \bar{e}_{47k}\ Z_{gen}/(R1 + Z_{gen})$	0.81	0.87	0.98	1.4	2.4	4.2	7.4	11.6
10	$\bar{e}_n^2$	360	195	121	100	90	81	81	81
	$\bar{e}_1^2$ (from $\bar{i}_n$)	1 21	1.2	1.5	2.65	6.5	18.5	50	150
	$\bar{e}_2^2$ (from $\bar{e}_R$)	19	19	19	18	17	15	11	7.2
	$\bar{e}_3^2$ (from $\bar{e}_{47k}$)	0.65	0.76	0.96	2	5.8	18	55	135
	$\Sigma\bar{e}_n^2$ (nV²/Hz)	381	216	142	122	120	133	147	373
15	BA^2 (Hz)	10.2	30.4	162	504	1010	2640	3400	1550
	$BA^2\Sigma\bar{e}^2$ (nV²)	3880	6550	23000	61500	121000	350000	670000	580000

16 $\Sigma(\bar{e}_{ni}^2 + \bar{e}_{1i}^2 + \bar{e}_{2i}^2 + \bar{e}_{3i}^2)\ B_iA_i2 = 1{,}815{,}930\ nV^2$

$\bar{e}_N = \sqrt{\Sigma} = 1.337\ \mu V$

17 S/N = 20 log (4.0 mV/1.337 μV) = 69.4 dB

Note the significant contributions of $\bar{i}_n$ and the 47k resistor, especially at high frequencies. Note also that there will be a difference between calculated noise and that noise measured on broadband meters because of the A curve employed in the example. If it were not for the A curve attenuation at low frequencies, the $\bar{e}_n$ would add a very important contribution below 200 Hz. This would be due to the RIAA boost at low frequency. As it stands, 97% of the 1.35 μV would occur in the 800–12.8 kHz band alone, principally because of the high frequency boost and the A measurement curve. If the measurement were made without either the high frequency boost or the A curve, the $\bar{e}_n$ would be 1.25 μV. In this case, 76% of the total noise would arise in the 50 Hz–400 Hz band alone. If the A curve were used, but the high-frequency boost were deleted, $\bar{e}_n$ would be 0.91 μV; and 94% would arise in the 800–12,800 Hz band alone.

The three different methods of measuring would only produce a difference of +3.5 dB in overall S/N, however the prime sources of the largest part of the noise and the frequency character of the noise can vary greatly with the test or measurement conditions. It is, then, quite important to know the method of measurement in order to know which individual noise sources in *Figure 7* must be reduced in order to significantly improve S/N.

Conclusions

The main points in selecting low noise preamplifiers are:

1. Don't pad the signal source; live with the existing R_{gen}.
2. Select on the basis of low values of $\bar{e}_n$ and especially $\bar{i}_n$ if R_{gen} is over about a thousand Ω.
3. Don't select on the basis of NF or R_{OPT} in most cases. NF specs are all right so long as you know precisely how to use them and so long as they are valid over the frequency band for the R_{gen} or Z_{gen} with which you must work.
4. Be sure to (root) sum all the noise sources $\bar{e}_n$, $\bar{i}_n$ and $\bar{e}_R$ in your system over appropriate bandwidth.
5. The higher frequencies are often the most important unless there is low frequency boost or high frequency attenuation in the system.
6. Don't forget the filtering effect of the human ear in audio systems. Know the eventual frequency emphasis or filtering to be employed.

Appendix I

Derivation of R_{OPT}:

$$NF = 10 \log \frac{\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2} R_{gen}^2}{\overline{e_R^2}}$$

$$10 \log \left(1 + \frac{\overline{e_n^2} + \overline{i_n^2} R_{gen}^2}{\overline{e_R^2}}\right)$$

$$\frac{\delta NF}{\delta R} = \frac{0.435}{(4\ kTRB)^2} \frac{4\ kTRB\ (2R\ \overline{i_n^2}) - (\overline{e_n^2} + \overline{i_n^2} R^2) 4\ kTB}{1 + (\overline{e_n^2} + \overline{i_n^2} R^2)/4\ kTRB}$$

where: $R = R_{gen}$

Set this = 0, and

$$4\ kTRB(2R\ \overline{i_n^2}) = 4\ kTB\ (\overline{e_n^2} + \overline{i_n^2} R^2)$$

$$2\ \overline{i_n^2} R^2 = \overline{e_n^2} + \overline{i_n^2} R^2$$

$$\overline{i_n^2} R^2 = \overline{e_n^2}$$

$$R^2 = \overline{e_n^2}/\overline{i_n^2}$$

$$R_{OPT} = \frac{\overline{e_n}}{\overline{i_n}}$$

Appendix II

Selecting R_{gen} for highest S/N.

$$S/N = \frac{e_{sig}^2}{B(\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2} R^2)}$$

For S/N to increase with R,

$$\frac{\delta S/N}{\delta R} > 0$$

$$\frac{\delta S/N}{\delta R} = \frac{2e_{sig}\ (\delta e_{sig}/\delta R)\ (\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2} R^2) - e_{sig}^2\ (4\ kT + 2\ \overline{i_n^2} R)}{B(\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2} R^2)^2}$$

If we set > 0, then

$$2\ (\delta e_{sig}/\delta\ R)\ (\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2} R^2) > e_{sig}\ (4\ kT + 2\ \overline{i_n^2} R)$$

For $e_{sig} = k_1 \sqrt{R}$, $\delta e_{sig}/\delta R = \frac{k_1}{2\sqrt{R}}$

$$(2\ k_1/2\sqrt{R})\ (\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2} R2) > k_1\sqrt{R}\ (4\ kT + 2\ \overline{i_n^2} R)$$

$$\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2} R^2 > 4\ kTR + 2\ \overline{i_n^2} R^2$$

$$\overline{e_n^2} > \overline{i_n^2} R^2$$

$$R < \overline{e_n}/\overline{i_n}$$

Appendix II (Continued)

Therefore S/N increases with R_{gen} so long as $R_{gen} \leq R_{OPT}$

For $e_{sig} = k_1 R$, $\delta e_{sig}/\delta R = k_1$

$$2 k_1 (\bar{e}_R^{\,2} + \bar{e}_n^{\,2} + \bar{i}_n^{\,2} R^2) > k_1 R (4 kT + 2 \bar{i}_n^{\,2} R)$$

$$2 \bar{e}_R^{\,2} + 2 \bar{e}_n^{\,2} + 2 \bar{i}_n^{\,2} R^2 > 4 kTR + 2 \bar{i}_n^{\,2} R^2$$

$$\bar{e}_R^{\,2} + 2 \bar{e}_n^{\,2} > 0$$

Then S/N increases with R_{gen} for any amplifier.

For any e_{sig} an optimum R_{gen} may be determined. Take, for example, $e_{sig} = k_1 R^{0.4}$, $\delta e_{sig}/\delta R = 0.4 k_1 R^{-0.6}$

$$(0.8 k_1/R^{0.6}) (\bar{e}_R^{\,2} + \bar{e}_n^{\,2} + \bar{i}_n^{\,2} R^2) > k_1 R^{0.4} (4 kT + 2 \bar{i}_n^{\,2} R)$$

$$0.8 \bar{e}_R^{\,2} + 0.8 \bar{e}_n^{\,2} + 0.8 \bar{i}_n^{\,2} R^2 > 4 kTR + 2 \bar{i}_n^{\,2} R^2$$

$$0.8 \bar{e}_n^{\,2} > 0.2 \bar{e}_R^{\,2} + 1.2 \bar{i}_n^{\,2} R^2$$

Then S/N increases with R_{gen} until

$$0.25 \bar{e}_R^{\,2} + 1.5 \bar{i}_n^{\,2} R^2 = \bar{e}_n^{\,2}$$

New Op Amp Ideas

National Semiconductor
Application Note 211
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Abstract

An op amp and voltage reference capable of single supply operation down to 1.1V is introduced. Performance is uncompromised and compares favorably with standard, state-of-the-art devices. In a departure from conventional approaches, the circuit can operate in a floating mode, powered by residual voltages, independent of fixed supplies. A brief description of the IC design is given, but emphasis is on applications. Examples are given for a variety of remote comparators and two-wire transmitters for analog signals. Regulator designs with outputs ranging from a fraction of a volt to several hundred volts are discussed. In general, greater precision is possible than with existing ICs. Designs for portable instruments are also looked into. These applications serve to emphasize the flexibility of the new part and can only be considered a starting point for new designs.

Introduction

Integrated circuit operational amplifiers have reached a certain maturity in that there no longer seems to be a pressing demand for better performance. Devices are available at low cost for all but the most exacting needs. Of course, there is always room for improvement, but even substantial changes in specifications cannot be expected to cause much excitement.

A new approach to op amp design and application has been taken here. First, the amplifier has been equipped to function in a floating mode, independent of fixed supplies. This, however, in no way restricts conventional operation. Second, it has been combined with a voltage reference, since these two functions are often interlocked in equipment design. Third, the minimum operating voltage has been reduced to nearly one volt. It will be seen that these features open broad new areas of application.

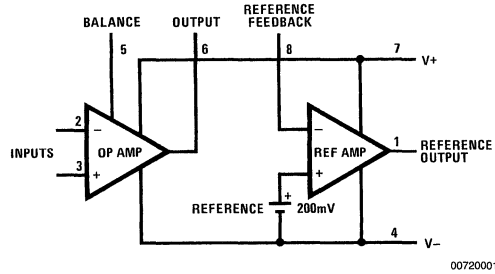

FIGURE 1. Functional diagram of the new IC

A functional diagram of the new device is shown in *Figure 1*. Even though a voltage reference and a reference amplifier have been added, it can still be supplied in an eight-pin TO-5 or mini-DIP. The pin connections for the op amp are the same as the industry standards. And offset balancing that tends to minimize drift has been provided. Both the op amp and the reference amplifier are internally compensated for unity-gain feedback.

Table 1 shows that, except for bias current, the general specifications are much as good as the popular LM108. But the new circuit has a common mode range that includes V^- and the output swings within 50 mV of the supplies with 50 µA load, or within 0.4V with 20 mA load. These parameters are specified in *Table 1* as the conditions under which gain and common-mode rejection are measured. *Table 2* indicates that the reference compares favorably with the better ICs on the market today.

TABLE 1. Typical Performance of the Operational Amplifier at 25°C

Parameter	Conditions	Value
Input Offset Voltage		0.3 mV
Offset Voltage Drift	$-55°C \le T_A \le 125°C$	2 µV/°C
Input Offset Current		0.25 nA
Offset Current Drift	$-55°C \le T_A \le 125°C$	2 pA/°C
Input Bias Current		10 nA
Bias Current Drift	$-55°C \le T_A \le 125°C$	40 pA/°C
Common-Mode Rejection	$V^- \le V_{CM} \le V^+ - .85V$	102 dB
Supply-Voltage Rejection	$1.2V \le V_S \le 40V$	96 dB
Unloaded Voltage Gain	$V_S = \pm 20V$, $V_O = \pm 19.95V$, $I_O \le 50\ \mu A$	400V/mV
Loaded Voltage Gain	$V_S = \pm 20V$, $V_O = \pm 19.6V$, $R_L = 980\Omega$	130V/mV

TABLE 1. Typical Performance of the Operational Amplifier at 25°C (Continued)

Parameter	Conditions	Value
Unity-Gain Bandwidth	$1.2V \leq V_S \leq 40V$	0.3 MHz
Slew Rate	$1.2V \leq V_S \leq 40V$	0.15V/μs

TABLE 2. Typical Performance of the Reference at 25°C

Parameter	Conditions	Value
Line Regulation	$1.2V \leq V_S \leq 40V$	0.001%/V
Load Regulation	$0 \leq I_O \leq 1$ mA	0.01%
Feedback Sense Voltage		200 mV
Temperature Drift	$-55°C \leq T_A \leq 125°C$	0.002%/°C
Feedback Bias Current		20 nA
Amplifier Gain	$0.2V \leq V_O \leq 35V$	75V/mV
Total Supply Current	$12.V \leq V_S \leq 40V$	270 μA

Since worst-case internal dissipation can easily exceed 1W under overload conditions, thermal overload protection is included. Thus at higher ambient temperatures, this circuit is better protected than conventional op amps with lesser output capabilities

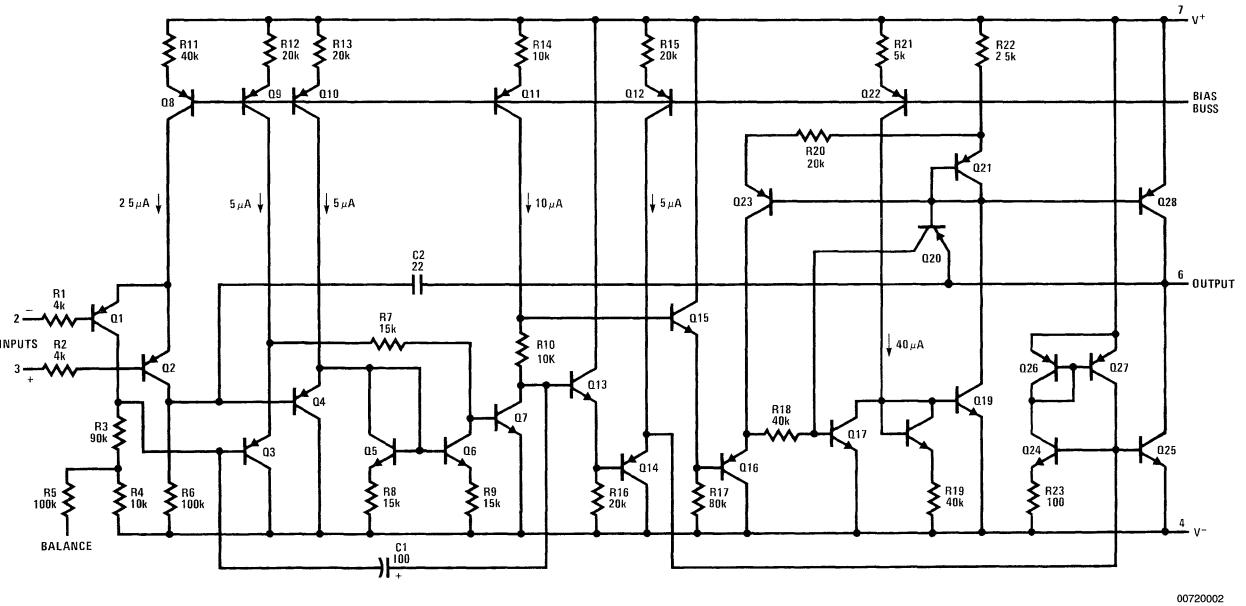

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FIGURE 2. Essential details of the Op Amp

Figure 2 and *Figure 5* are simplified schematics of the op amp, the reference and the internal current regulator. A complete circuit description is a subject in itself and is covered in detail elsewhere [1]. However, a brief run through the circuit is in order to give some understanding of the details that affect application

The Op Amp

Referring to *Figure 2*, lateral PNPs are used for the op amp input because this was the only reasonable way to get V^- included in the common-mode range while meeting the minimum-voltage requirement. These transistors typically have $h_{FE} > 100$ at $I_C = 1\ \mu A$ and appear to match better than their NPN counterparts. Current gain is less affected by temperature, resulting in a fairly flat bias current over temperature (*Figure 3*). At elevated temperature the sharp decrease in bias current for $V_{CM} > V^-$ is caused by the same substrate leakage that affects bi-FET op amps.

Protective resistors have been included in the input leads so that current does not become excessive when the inputs are forced below the negative supply, forward biasing the base tubs of the lateral PNPs.

Offset nulling is accomplished by connecting the balance terminal to a variable voltage derived from the reference output, as shown in *Figure 4*. Both the input stage collector voltage and the reference are well regulated and have a low temperature drift. The resistance of the adjustment potentiometer can be made very much lower than the resistance looking back into the balance pin. Therefore, no matching of temperature coefficients is required and offset nulling will tend to produce a minimum-drift condition.

With 200 mV on the balance control, the balance range is asymmetrical. Standard parts are trimmed to bring them into the −1 mV to 8 mV adjustment range. Null sensitivity can be reduced for low-offset premium parts by adding a resistor on the top end of R1.

Proceeding through the circuit, the input stage is buffered by vertical PNP followers, Q3 and Q4. From here, the differential signal is converted to single ended and fed to the base of the second stage amplifier, Q7.

This configuration is not inherently balanced in that the emitter-base voltage of the PNP transistors is required to match that of the NPNs. The final design includes circuitry to correct for the expected variations.

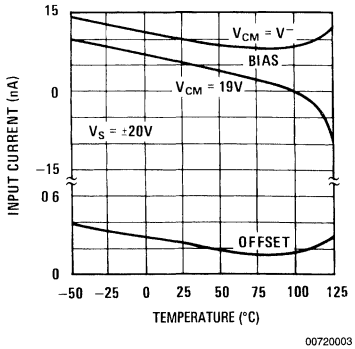


FIGURE 3. Variation of input current with temperature

From the collector of Q7, the signal splits, driving separate halves of the complementary class-B output stage The NPN output transistor, Q25, is driven through Q13 and Q14

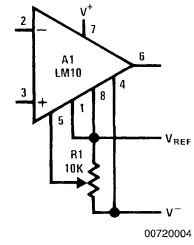


FIGURE 4. Op Amp offset adjustment

This complementary emitter follower arrangement provides the necessary current gain without requiring the extra bias voltage of the Darlington connection.

Base drive for the NPN output transistor is initially supplied by Q12, but a boost circuit has also been added to increase the available drive as a function of load current. This is accomplished by Q24 in conjunction with a current inverter.

Drive for the PNP half of the output is somewhat more complicated. Again, a compound buffer, Q15 and Q16, is used, although to maintain circuit balance rather than for current gain. The signal proceeds through two inverters, Q17 and Q19, to obtain the correct phase relationship and DC level shift before it is fed to the PNP output transistor, Q28.

This path has three common-emitter stages and, potentially, much higher gain than the NPN side. The gain is equalized, however, by the shunting action of Q18–R19 and Q21–R22 as well as negative feedback through Q23.

When the output PNP saturates, Q20 serves to limit its base overdrive with a feedback path to the base of Q17. As will be seen, Q20 is also important to floating-mode operation in that it disables the PNP drive circuitry when the op-amp output is shorted to V^+

The Reference

A simplified version of the reference circuitry and internal current regulator is shown in *Figure 5*. The design of the band-gap reference is unconventional both in its configuration and because it compensates for the second-order nonlinearities in the emitter-base voltage as well as those introduced by resistor drift. Thus, the bowed characteristic of conventional designs is eliminated, with better temperature stability resulting.

The reference element iself is formed by Q40 and Q41, with the output on the emitter of Q41 The V_{BE} component of the output is developed across R30, while the ΔV_{BE} component is obtained by operating Q41 at a much lower current density than Q40. The output is made less sensitive to variations in biasing current by the action of R29. Curvature correction results from the different temperature coefficients of bias current for the two transistors.

The 200 mV reference voltage is fed to both the reference amplifier and the internal current regulator. The reference amplifier design is straight-forward, consisting of two stages with an emitter follower output. Unlike the op amp, the output can only swing within 0.8V of the positive supply. This should be kept in mind when designing low-voltage circuitry.

The Reference (Continued)

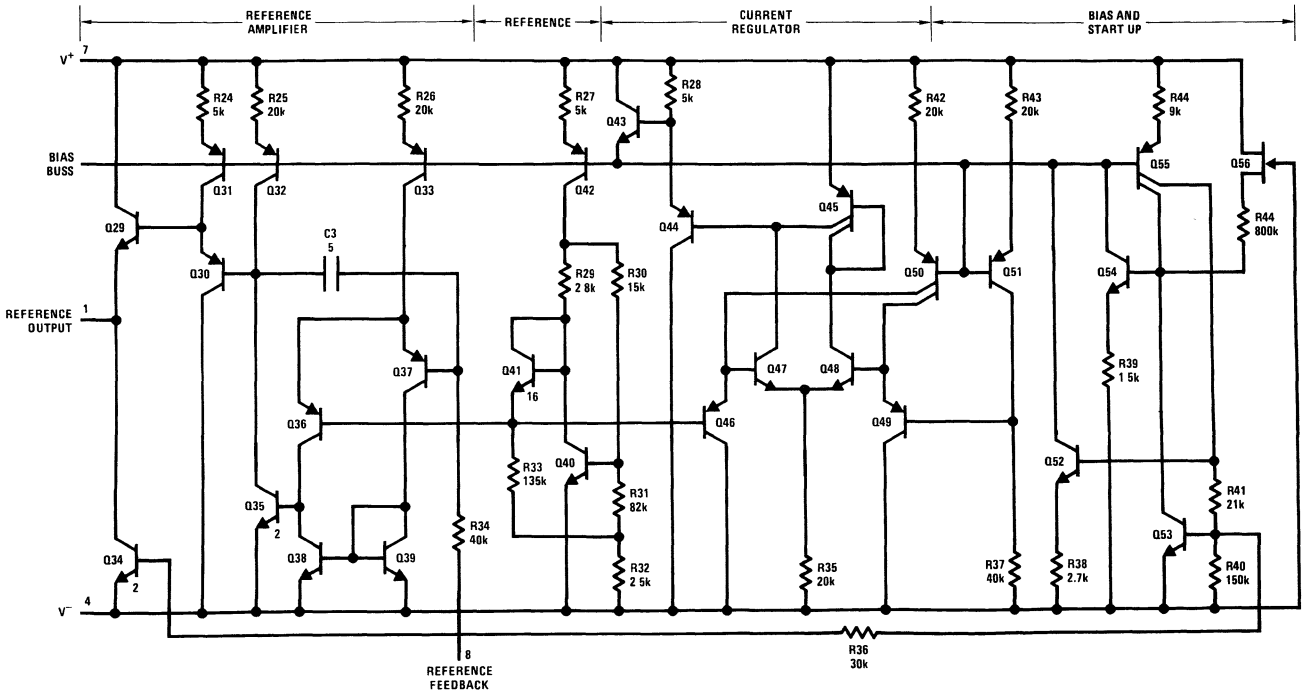


FIGURE 5. Simplified Schematic of the Reference and Internal Current Regulator

The Reference (Continued)

A minimal sink current (~20 µA) is supplied by Q34. And since the reference is not included in the thermal protection control loop, conventional current limit is included on the final circuit to limit maximum output current to about 3 mA.

The current regulator is also relatively uncomplicated. A control loop drives the current source bias bus so that the output of one current source (Q51) is proportional to the reference voltage. The remaining current sources are slaved into regulation by virtue of matching.

The remaining circuitry generates a trickle current for start-up and biases internal circuitry.

An analysis of the complete circuit would serve only to bring into focus a multitude of detail such as second-order DC compensation terms, minor-loop frequency stabilization, clamps, overload protection, etc. Although necessary, these particulars tend to obscure the principles being put forward. So, having gained some insight into circuit operation, it is appropriate to proceed to some of the novel applications made possible with this new IC.

Floating Comparators

The light-level detector in *Figure 6* illustrates floating-mode operation of the IC. Shorting the op-amp outut to V^+ disables the PNP half of the class-B output stage, as mentioned earlier. Thus, with a positive input signal, neither half of the output conducts and the current between the supply terminals is equal to the quiescent supply current. With negative input signals, the NPN portion of the output begins to turn on, reaching the short circuit current for a few hundred microvolts overdrive. This is shown in *Figure 7*.

Figure 7 also shows the terminal characteristics for the case where the output is shorted to V^- so that only the PNP side can be activated. This mode of operation has not been so thoroughly investigated, but it gives a slightly lower ON voltage at moderate currents and the gain is generally higher below 70°C. With ON currents less than about 1 mA, the terminal voltage drops low enough to disrupt the internal regulators and the reference, producing some hysteresis. Further, there is a tendency to oscillate over about a 50 µV range of input voltage in the linear region of comparator operation.

The above is not intended to preclude operation with the output connected to V^-, if there is a good reason for doing so. It is meant only to draw attention to the problems that might be encountered.

In *Figure 6*, the internal reference supplies the bias that determines the transition threshold. At crossover, the voltage across the photodiode is equal to the offset voltage of the op amp, so leakage is negligible. The circuit can directly drive such loads as logic circuits or silicon controlled rectifiers. The IC can be located remotely with the sensor, with the output transmitted along a twisted-pair line. Alternatively, a common ground can be used if there is sufficient noise immunity; and the signal can be transmitted on a single line.

It should be remembered that this particular design is fully compensated as a feedback amplifier. As such it is not particularly fast in comparator applications. With low-level signals, delays a few hundred microseconds can be expected; and once in the linear region, the maximum change of terminal voltage is 0.15/µs. This is illustrated in the plots of *Figure 8* and *Figure 9*. In general, high accuracy cannot be obtained with switch frequencies above 100 Hz.

Hysteresis can be provided as shown in *Figure 6* by feedback to the balance terminal. About 1 mV of hysteresis is obtained for a 5V output swing. However, this disappears near 10 Hz operating frequency because of gain loss.

Figure 10 shows a flame detector that can drive digital circuitry directly. The platinum-rhodium thermocouple gives an 8 mV output at 800°C. This threshold is established by connecting the balance pin to the reference output

Linear Operation

The IC can also operate linearly in the floating mode. The simplest examples of this are the shunt voltage regulator in *Figure 11* and the current regulator in *Figure 12*. The voltage regulator is straightforward, but the current regulator is a bit unusual in that the supply current of the IC flows through the sense resistor and does not affect accuracy as long as it is less than the desired output current.

It is also possible to use remote amplifiers with two-wire signal transmission, as was done with the comparators. Remote sensors can be particularly troublesome when low-level analog signals are involved. Transmission problems include induced noise, ground currents, shunting from cable capacitance, resistance drops and thermoelectric potentials. These problems can be largely eliminated by amplifying the signal at the source and altering impedances to levels more suitable for transmission.

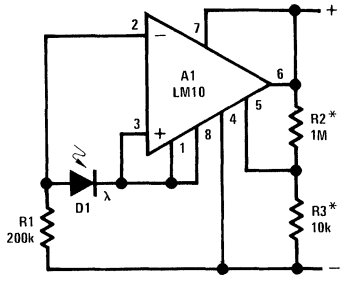
Figure 13 is an example of a remote amplifier. It boosts the output of a high-impedance crystal transducer and provides a low impedance output. No extra wires are needed because DC power is fed in on the signal line.

Figure 14 is a remote signal conditioner that operates in the current mode. A modification of the current source in *Figure 12*, it delivers an output current inversely proportional to sensor resistance. The output can be transmitted over a twisted pair for maximum noise immunity or over a single line with common ground if the signal is slow enough that sufficient noise bypass can be put on the line.

A current-mode signal conditioner for a thermocouple is shown in *Figure 15*. A thermocouple is in reality a two-junction affair that measures temperature differential. Absolute temperature measurements are made by controlling the temperature of one junction, usually by immersing it in an ice bath. This complication can be avoided with cold-junction compensation, which is an absolute thermometer that measures cold-junction temperature and corrects for any deviation from the calibration temperature.

In *Figure 15*, the IC temperature sensor (S1) generates an output proportional to absolute temperature. This current flows through R2, which is chosen so that its voltage drop has the same temperature coefficient as the thermocouple. Thus, changes in cold-junction temperature will not affect calibration as long as it is at the same temperature as S1.

Linear Operation (Continued)



*provides hysteresis

FIGURE 6. Two Terminal Light-Level Detector with Hysteresis

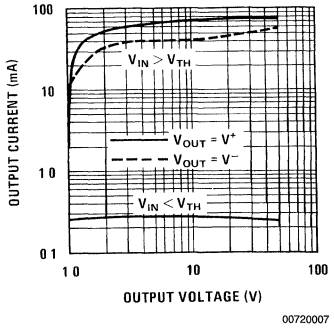


FIGURE 7. Terminal Characteristics Above and Below Threshold

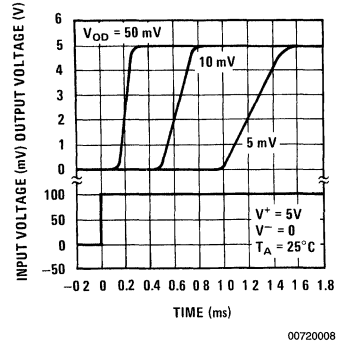


FIGURE 8. Comparator Response Times for Various Input Overdrives

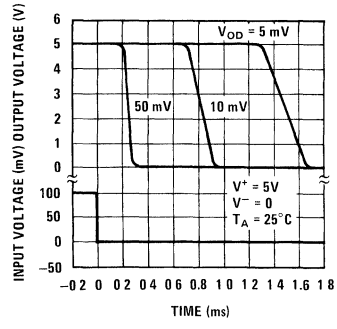
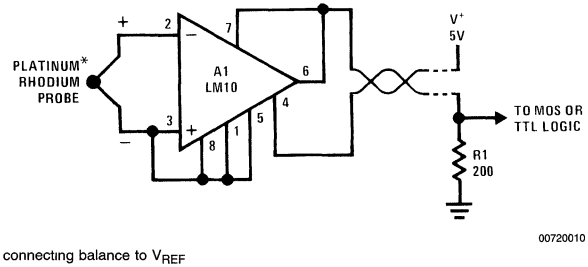


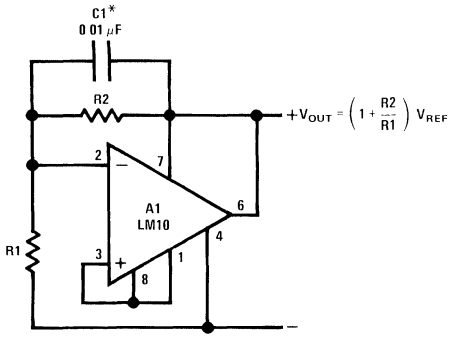
FIGURE 9. Comparator Response Times for Various Input Overdrives



*800 C threshold is established by connecting balance to V_{REF}

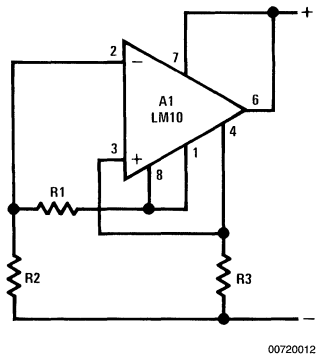
FIGURE 10. Flame Detector

Linear Operation (Continued)



*required for capacitive loading

FIGURE 11. Shunt Voltage Regulator



$$I_{OUT} = \frac{(R2 + R3)\, V_{REF}}{R1R3}$$

FIGURE 12. Current Regulator

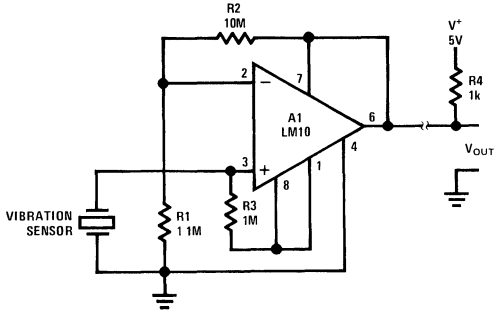


FIGURE 13. Remote Amplifier

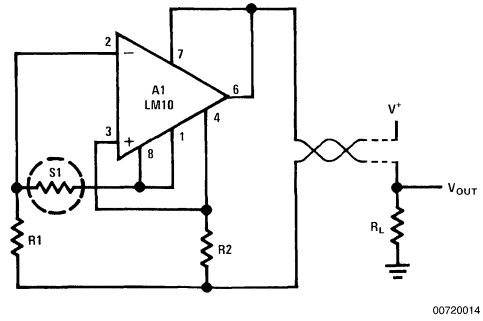
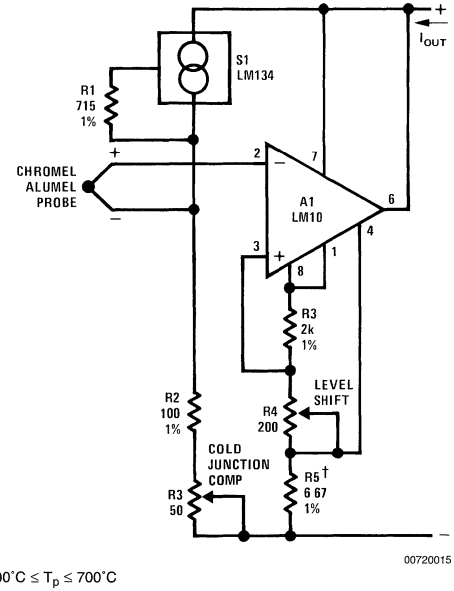


FIGURE 14. Two-Wire Transmitter for Variable-resistance Sensor



200°C ≤ T_p ≤ 700°C
1 mA ≤ I_{OUT} ≤ 5 mA
†gain trim

FIGURE 15. Current Transmitter for Thermocouple Including Cold Junction Compensation

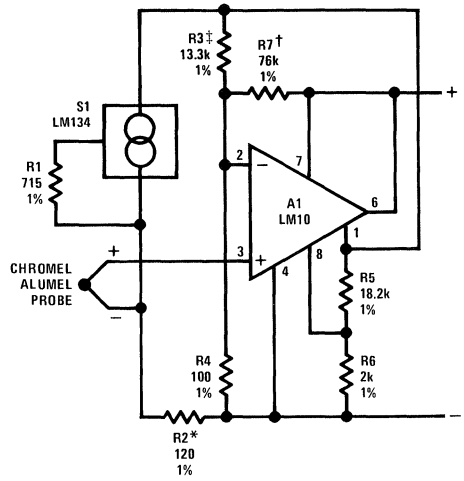
In addition to powering S1, the reference is used to generate an offset voltage such that the output current is within operating limits for temperatures of interest. It is important that the reference be stable because drift will show up as signal.

The indicated output-current range was chosen because it is one of the standards for two-wire transmission. With the new IC, the dynamic range can be increased by a factor of five in some cases (0.8 mA–20 mA) because the supply current is low. This could be used to advantage with a unidirectional signal where zero must be preserved: the less the offset required to put zero on scale, the less the offset-drift error.

Linear Operation (Continued)

The circuit in *Figure 16* is the same thermocouple amplifier operating in the voltage mode. The output voltage range was chosen arbitrarily in that there are no set standards for voltage-mode transmission.

The choice between voltage- and current-mode operation will depend on the peculiarities of the application, although current mode seems to be favored overall. If there is sufficient supply voltage, the dynamic range of both approaches is about equal, provided the transmitter is capable of working at both low voltage and current. This situation could be modified by the voltage and current requirements of the sensor or conditioning circuitry.



$4V \leq V_{OUT} \leq 20V$

$200°C \leq T_p \leq 700°C$

†span trim

‡level-shift trim

*cold-junction trim

FIGURE 16. Voltage Transmitter for Thermocouple, Including Cold Junction Compensation

With voltage-mode operation, the line resistance can cause error because the DC current that powers the amplifier and sensor circuitry must flow through it. Ground potentials, if they cannot be swamped out with signal swing, would require that twisted pair lines be used. This is not so with current mode.

An important consideration is that cable capacitance does not affect the loop stability of the current-mode amplifier. However, large-amplitude noise appearing across the output can give problems. *Figure 17* shows the noise rejections of the LM10. The negative supply rejection applies in current-mode operations with the output connected to V^+. The rejection in this mode is not overly impressive, but transmission can be reduced by bypassing the load resistor. This done, noise slew limiting is the restricting factor in that excessive slew can give rise to a DC error. The maximum noise amplitude that can be tolerated for a 100 µV input-referred DC error is plotted in *Figure 18*. These limits are not to be pushed as error increases rapidly above them.

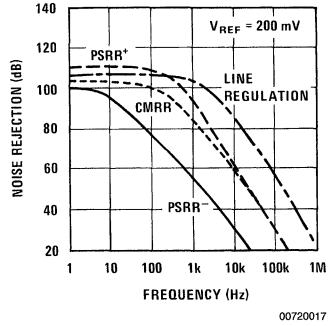


FIGURE 17. Noise Rejection for the Various Elements of the Circuit

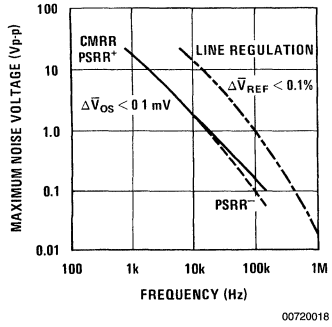


FIGURE 18. Noise Frequency and Amplitude Required to give Indicated Error

With voltage-mode, the circuit reacts to capacitive loading like any other op amp. If there are problems, the load should be isolated with a resistor, taking DC feedback from the load and AC feedback from the op amp output. With the LM10, it is also possible to bypass the output with a single, large capacitor (20 µF electrolytic) if speed is no consideration.

With bridge sensors, these techniques not only reduce noise problems but only require two leads to both power the bridge and retrieve the signal.

The relevant circuit is shown in *Figure 19*. The op amp is wired for a high-impedance differential input so as not to load the bridge. The reference supplies the offset to put the amplifier in the center of its operating range when the bridge is balanced. It also powers the bridge. The low voltage available from the reference regulator is ideal for driving wire strain gauges that usually have low resistances.

Another form of remote signal processing is shown in *Figure 20*. A logarithmic conversion is made on the output current of a photodiode to compress a four-decade, light-intensity variation into a standard transmission range. The circuit is balanced at mid-range, where R3 should be chosen so that the current through it equals the photodiode current. The log-conversion slope is temperature compensated with R6. Setting the reference output to 1.22V gives a current through R2 that is proportional to absolute temperature, because of D1, so that this level-shift voltage matches the temperature

Linear Operation (Continued)

coefficient of R6. C1 has been added so that large area photodiodes with high capacitance do not cause frequency instabilities.

Figure 21 shows a setup that optically measures the temperature of an incandescent body. It makes use of the shift in the emission spectrum of a black body toward shorter wavelengths as temperature is increased. Optical filters are used to split the emission spectrum, with one photodiode being illuminated by short wavelengths (visible light) and the other by long (infrared). The photocurrents are converted to logarithms by Q1 and Q2. These are subtracted to generate an output that varies as the log of the ratio of the illumination intensities. Thus, the circuit is sensitive to changes in spectral distribution, but not intensity. Otherwise, the circuit is quite similar to that in *Figure 20*.

The laws of physics dictate that the output is not a simple function of temperature, so point-by-point calibration is necessary. Sensitivity for a particular temperature range is optimized with the crossover point of the optical filter, longer wavelengths giving lower temperatures.

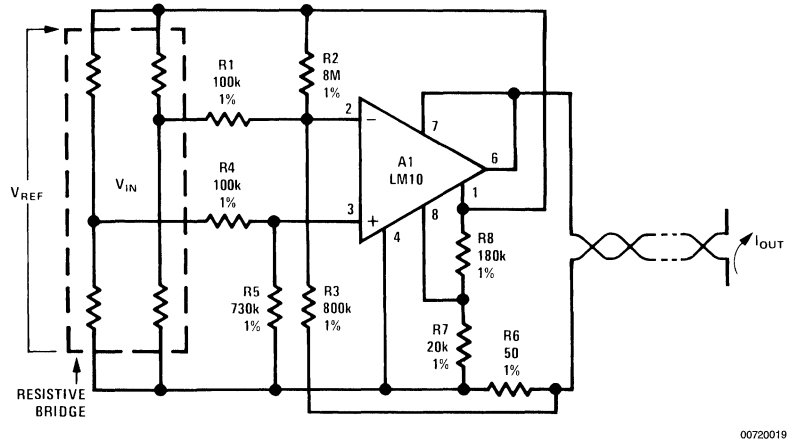
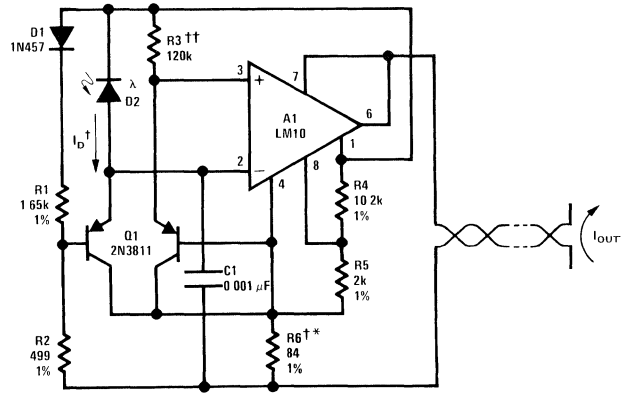


FIGURE 19. Two-Wire Transmitter for Resistive Bridge

Linear Operation (Continued)



$$1\ mA \leq I_{OUT} \leq 5\ mA$$

$$0.01 \leq \frac{I_{D2}}{I_{D1}} \leq 100$$

‡50 μA ≤ I_D ≤ 500 μF
††Center scale trim
†Scale factor trim
*Copper wire wound

FIGURE 20. Log Converter/Transmitter for a Photodiode

$$1\ mA \leq I_{OUT} \leq 5\ mA$$

$$0\ 01 \leq \frac{I_{D2}}{I_{D1}} \leq 100$$

00720040

$$V_{OUT} = \frac{R2}{R1} V_{REF}$$

††Level-shift trim
*Scale factor trim
†Copper wire wound

FIGURE 21. Optoelectric Pyrometer with Transmitter

Linear Operation (Continued)

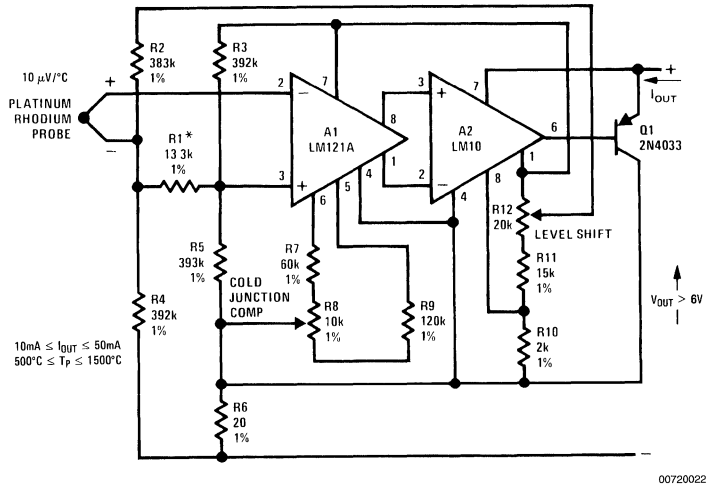


FIGURE 22. Precision Thermocouple Amplifier/Transmitter

Figure 22 shows how a low-drift preamplifier can be added to improve the measurement resolution of a thermocouple. The preamp is powered from the reference regulator, and bridge feedback is used to bias the preamp input within its common-mode range. Cold-junction compensation is provided with the offset voltage set into A1, it being directly proportional to absolute temperature.

The maximum drift specification for the preamp is 0.2 μV/°C. For this particular circuit, an equal drift component would result for 0.004%/°C on the reference, 0.001%/°C mismatch on the bridged-feedback resistors (R2–R4) or 3 μV/°C on the op amp offset voltage. The op amp drift might be desensitized by raising the preamp gain (lowering R7–R9), but this would require raising the output voltage of the reference regulator and the minimum terminal voltage.

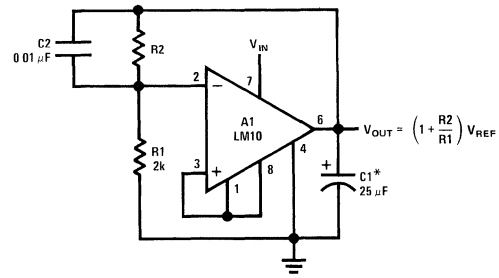
In this application, the preamp is run at a lower voltage than standard parts are tested with, and the maximum supply current specified is high. However, there should be no problem with the voltage; and a lower, maximum supply current can be expected at the lower voltage. Even so, some testing may be in order.

Regulators

The op amp and voltage reference are combined in *Figure 23* to make a positive voltage regulator. The output can be set between 0.2V and the breakdown voltage of the IC by selecting an appropriate value for R2. The circuit regulates for input voltages within a saturation drop of the output (typically 0.4V @ 20 mA and 0.15V @ 5 mA). The regulator is protected from shorts or overloads by current limiting and thermal shutdown.

Typical regulation is about 0.05% load and 0.003%/V line. A substantial improvement in regulation can be effected by connecting the op amp as a follower and setting the reference to the desired output voltage. This has the disadvantage that the minimum input-output differential is increased to a little more than a diode drop. If the op amp were connected for a gain of 2, the output could again saturate. But this requires an additional pair of precision resistors.

The regulator in *Figure 23* could be made adjustable to zero by connecting the op amp to a potentiometer on the reference output. This has the disadvantage that the regulation at the lower voltage settings is not as good as it might otherwise be.



*electrolytic

FIGURE 23. Adjustable Positive Regulator

It is also possible to make a negative regulator with this device, as can be seen from *Figure 24*. A discrete transistor is used to level shift the reference current. This increases the minimum operating voltage to about 1.8V.

Output voltage cannot be reduced below 0.85V because of the common-mode limit of the op amp. The minimum input-output differential is equal to the voltage across R1 plus the saturation voltage of Q1, about 400 mV.

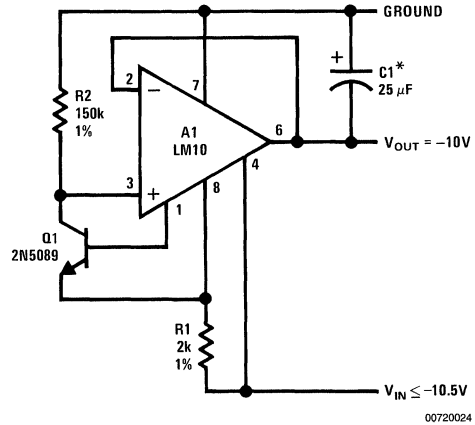
It is necessary that Q1 has a high current gain, or line regulation and thermal drift will be degraded. For example, with a nominal current gain of 100, a 1% drift will be intro-

Regulators (Continued)

duced between −55°C and 125°C. With the device specified, drift contribution should be less than 0.3% over the same range; but operation is limited to 30V on the input.

Floating-mode operation can also be useful in regulator applications. In *Figure 25*, the op amp controls the turn-on voltage of the pass transistor in such a way that it does not see either the output voltage or the supply voltage. Therefore, maximum voltages are limited only by the external transistors.

A three-stage emitter follower is used for the pass transistor primarily to insure adequate bias voltage for the IC under worst-case, high-temperature conditions. With lower output currents Q2 and R4 could be replaced with a diode.



*electrolytic

FIGURE 24. Negative Regulator

Load regulation is better than 0.01%. Worst-case line regulation is better than ±0.1% for a ±10V change in input voltage. If the op amp output were buffered with a discrete PNP, load and line regulation could be made essentially perfect, except for thermal drift.

Current limiting, although not shown, could easily be provided by the addition of a sense resistor and an NPN transistor. A foldback characteristic could be obtained with two more resistors.

A fully adjustable voltage and current regulator is shown in *Figure 26*. A second IC (A2) is added to provide regulation in the current-limit mode. Both the regulated voltage and the current can be adjusted close to zero.

The circuit has a tendency to overshoot when a short circuit is removed. This is suppressed with Q2, R5 and C3, which limit the rate at which the output can rise. Low-level oscillations at the dropout threshold are eliminated with C2 and R4.

The current-limit amplifier takes about 100 μs to respond to a shorted output. Therefore, Q6 has been added to limit the peak current during this interval.

Regulators (Continued)

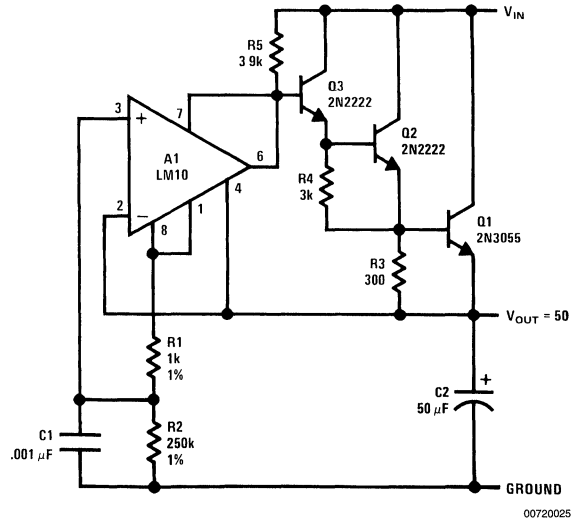
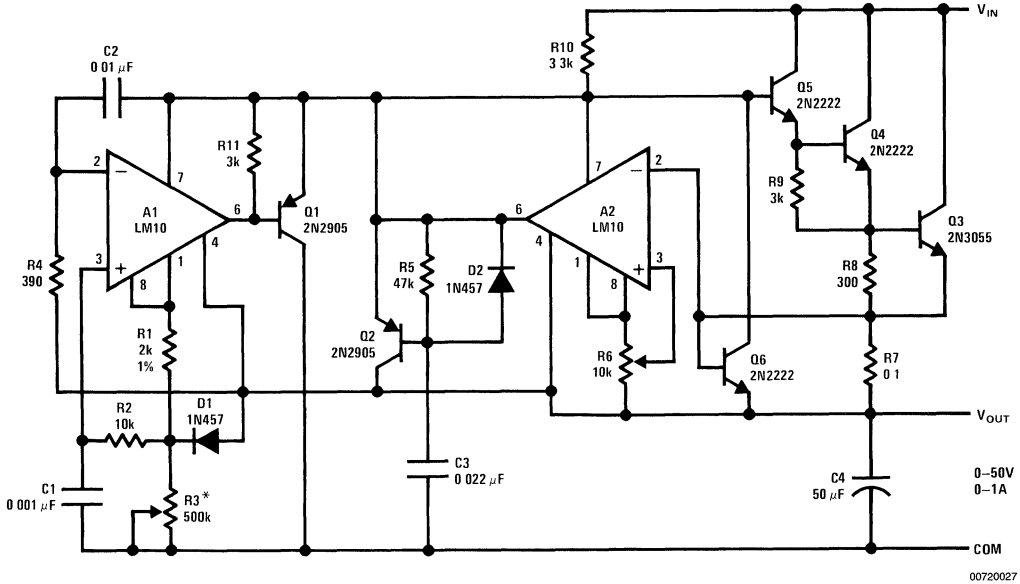


FIGURE 25. Bootstrapped Regulator



*$V_{OUT} = 10^{-4}$ R3

FIGURE 26. Detailed Schematic of an Adjustable Voltage and Current Regulator

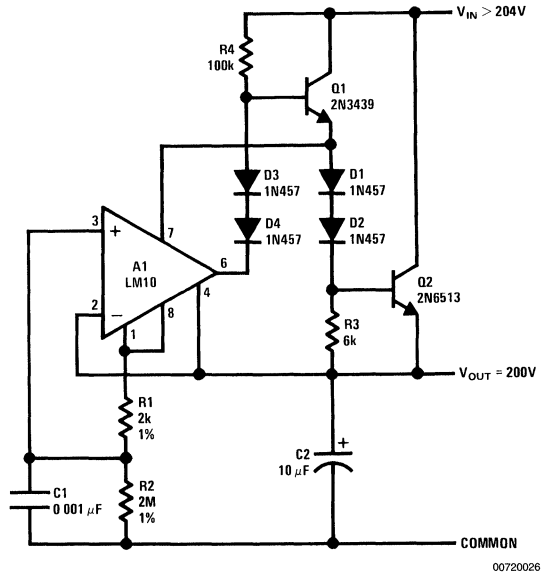
With high-voltage regulators, powering the IC through the drive resistor for the pass transistors can become quite inefficient. This is avoided with the circuit in *Figure 27*. The supply current for the IC is derived from Q1. This allows R4 to be increased by an order of magnitude without affecting the dropout voltage.

Selection of the output transistors will depend on voltage requirements. For output voltages above 200V, it may be more economical to cascade lower-voltage transistors.

Figure 28 shows a more detailed circuit for a high-voltage regulator. Foldback current limiting has been added to protect the pass transistors from blowout caused by excessive

Regulators (Continued)

heating or secondary breakdown. This limiting must be fairly precise to obtain reasonable start-up characteristics while conforming to worst case specifications for the transistors. This accounts for the complexity of the circuit.



$$V_{OUT} = \frac{R2}{R1} V_{REF}$$

FIGURE 27. High-Voltage Regulator

Regulators (Continued)

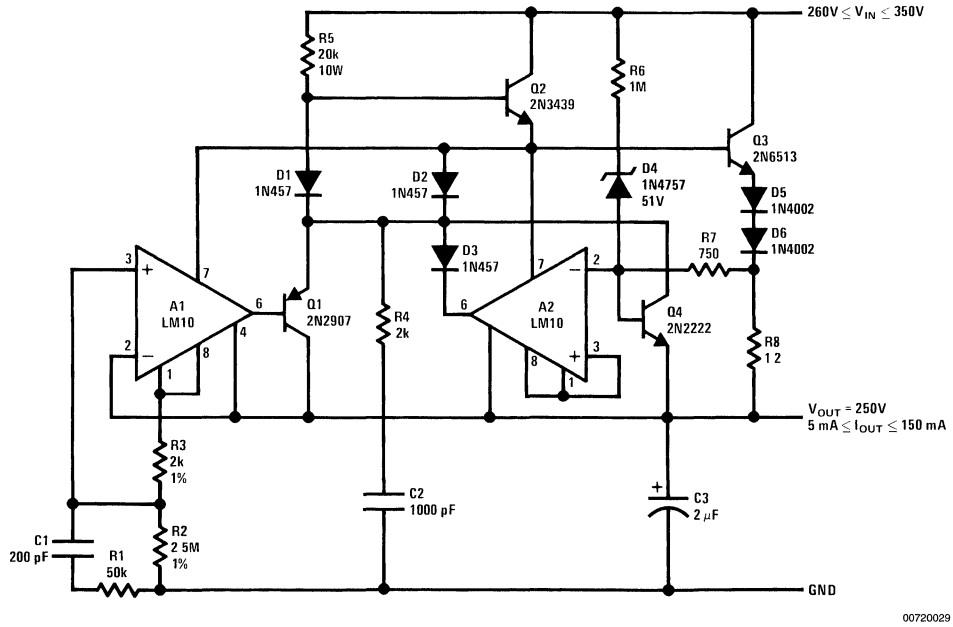


FIGURE 28. High Voltage Regulator with Foldback Current Limit

The output current is sensed across R8. This is delivered to the current limit amplifier through R7, across which the foldback potential is developed by R6 with a threshold determined by D4. The values given limit the peak power below 20W and shut off the pass transistors when the voltage across them exceeds 310V. With unregulated input voltages above this value, start-up is initiated solely by the current through R5 Q4 is added to provide some control on current before A2 has time to react.

The design could be considered overly conservative, but this may not be inappropriate considering the start of the art for high-voltage power transistors. Their maximum operating current is in the tens of milliamperes at maximum voltage. Cutting off the power transistor before the maximum input-output voltage differential is reached can cause start-up problems, depending on the nature of the load (those that tend toward a constant-current characteristic being worst).

If a tighter design is required for start-up, the values of R6 and D4 can be altered. In addition, R5 can be lowered, although it may be necessary to add a PNP buffer to A2 in place of D3.

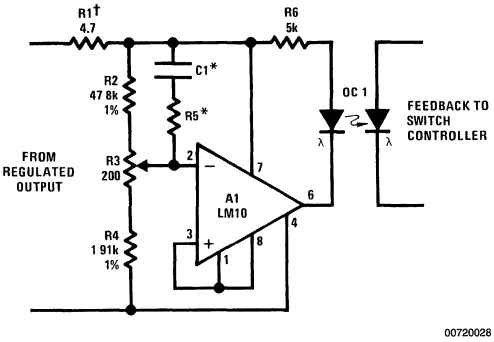
The leakage current of Q3 can be more than several milliamperes. That is why a hard turn-off is provided with D2.

The circuit is stable with an output capacitor greater than about 2 μF. Spurious oscillations in current limit are suppressed by C2 and R4, while a strange, latch-mode oscillation coming out of current limit is killed with C1 and R1.

Switching regulators operating directly from the power lines are seeing increased usage not only because of the reduced weight and size when compared to a 60 Hz transformer but also because they operate over a wide voltage range giving a regulated output with reasonable efficiency. Electrical isolation of the load is generally required in these applications for reasons of safety. Therefore, if precise regulation is needed on the secondary, there must be some way of transmitting the error signal back to the primary.

Figure 29 shows a design that provides this function. The IC serves as a reference and error amplifier, transmitting the error signal through an optical coupler. The loop gain may be controlled by the addition of R1, and C1 and R5 may be added to develop the phase lead that is helpful in frequency stabilizing the feedback.

Regulators (Continued)



†controls "loop gain"

*optional frequency shaping

FIGURE 29. Isolated Sensor for an Off-Line Switching Regulator

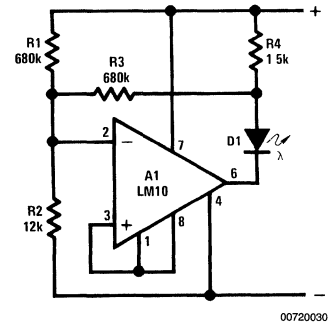
Voltage Level Indicators

In battery-powered circuitry, there is some advantage to having an indicator to show when the battery voltage is high enough for proper circuit operation. This is especially true for instruments that can produce erroneous data.

The battery status indicator drawn in *Figure 30* is designed for a 9V source. It begins dimming noticeably below 7V and extinguishes at 6V. If the warning of incipient battery failure is not desired, R3 can be removed and the value of R1 halved.

A second circuit that also regulates the current through the light-emitting diode is shown in *Figure 31*. This is important so that adequate current is available at minimum voltage, but excessive current is not drawn at maximum voltage. Current regulation is accomplished by using the voltage on the balance pin (5) as a reference for the op amp. This is controlled at approximately 23 mV, independent of temperature, by an internal regulator. When the voltage on the reference-feedback terminal (8) drops below 200 mV, the reference output (1) rises to supply the feedback voltage to the op amp through D2, so the LED current drops to zero.

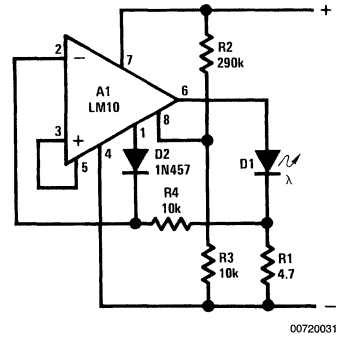
The minimum threshold voltage for these circuits is basically limited by the bias voltage for the LEDs. Typically, this is 1.7V for red, 2V for green and 2.5V for yellow. These two circuits can be made to operate satisfactorily for threshold voltages as low as 2V if a red diode is used. However, the circuit in *Figure 31* is preferred in that difficulties caused by voltage change across the diode biasing resistor are eliminated.



V_{TH} = 6V

LED dims below 7V

FIGURE 30. Battery Status Indicator



V_{TH} = 6V

I_{D1} = 5 mA

FIGURE 31. Battery Level Indicator with Regulated LED Current

When operating with a single cell, it is necessary to incorporate switching circuitry to develop sufficient voltage to drive the LED. A circuit that accomplishes this is drawn in *Figure 32*. Basically, it is a voltage-controlled asymmetrical multivibrator with a minimum operating threshold given by

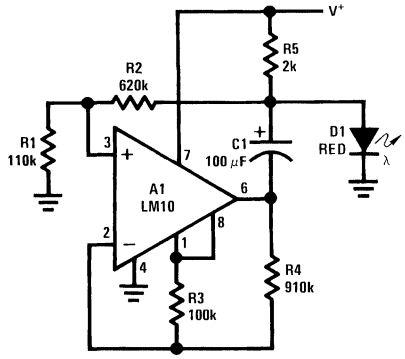
$$V_{TH} = \frac{R4\,(R1 + R2)}{R1\,(R3 + R4)} V_{REF} \quad (1)$$

Above this threshold, the flash frequency increases with voltage. This is a far more noticeable indication of a deteriorating battery than merely dimming the LED. In addition, the indicator can be made visible with considerably less power drain. With the values shown, the flash rate is 1.4 sec^{-1} at 1.2V with a 300 µA drain and 5.5 sec^{-1} at 1.55V with 800 µA drain. Equivalent visibility for continuous operation would require more than 5 mA drain.

The maximum threshold voltage of this circuit is limited because the LED can be turned on directly through R5. Once this happens, the full supply voltage is not delivered to R2, which is how the threshold is determined. This problem can be overcome with the circuit illustrated in *Figure 33*. This

Voltage Level Indicators (Continued)

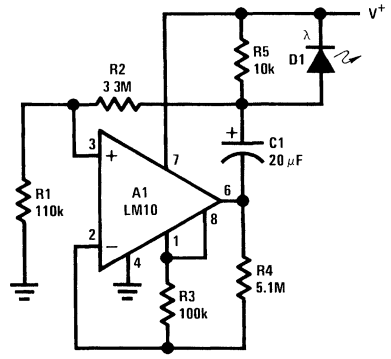
design repositions the indicator diode, requiring an input voltage somewhat greater than the diode bias voltage needed.



00720032

flashes about 1 2V, rate increases with voltage

FIGURE 32. Undervoltage Indicator for Single Call



00720033

V_{TH}' = 15V

V_{TH} = 6V

flash rate increases above 6V and below 15V

FIGURE 33. Double-Ended Voltage Monitor

This circuit has the added feature that it can sense an overvoltage condition. The lower activation threshold is given by equation (1), but above a threshold,

$$V_{TH}' = \frac{R4\,(R1 + R2)\,V_{REF}}{R1\,(R3 + R4) - R3\,(R1 + R2)'} \quad (2)$$

oscillation again ceases. (Below V_{TH} the op amp output is saturated negative while above V_{TH}' it is saturated positive.) The flash rate approaches zero near either limit.

The minimum/maximum limits possible with this circuit along with the possibility of estimating the proximity to the limit and the low power drain (~ 500 µA) make it attractive for a variety of simple, low-cost test equipment. This could include everything from the measurement of power-line voltage to in-circuit testers for digital equipment.

Meter Circuits

One obvious application for this IC is a meter amplifier. Accuracy can be maintained over a 15°C to 55°C range for a full-scale sensitivity of 10 mV and 100 nA using the design in *Figure 34.* In fact, initial tests indicate negligible zero drift with 1 mV and 10 nA sensitivities, although balancing is troublesome with low-cost potentiometers. Offset voltage error is nulled with R5, and the bias current can be balanced

Meter Circuits (Continued)

out with R4. The zeroing circuits operates from the reference output and are essentially unaffected by changes in battery voltage, so frequent adjustments should not be necessary.

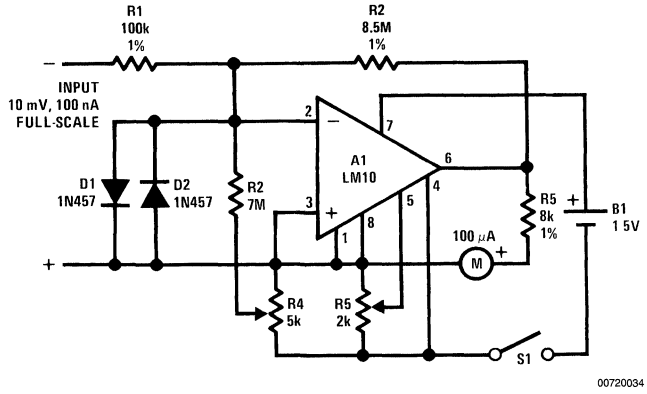


FIGURE 34. Meter Amplifier

Under overload conditions, the current delivered to the meter is kept well in hand by the limited output swing of the op amp. The same is true for polarity reversals. Input clamp diodes protect the circuit from gross overloads.

Total current drain is under 0.5 mA, giving an approximate life of 3–6 months with an "AA" cell and over a year with a "D" cell. With these lifetimes an ON/OFF switch may be unnecessary. A test switch that converts to a battery-test mode may be of greater value.

If the meter amplifier is used in building a multimeter, the internal reference can also be used in measuring resistance. This would make the usual frequent recalibration with falling cell voltage unnecessary.

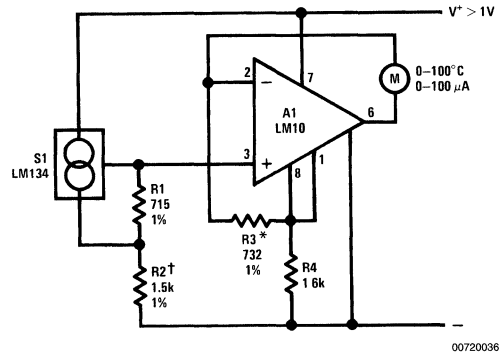
A portable light-level meter with a five-decade dynamic range is shown in *Figure 36.* The circuit is calibrated at mid-range with the appropriate illumination by adjusting R2 such that the amplifier output equals the reference and the meter is at center scale. The emitter-base voltage of Q2 will vary with supply voltage; so R4 is included to minimize the effect on circuit balance. If photocurrents less than 50 nA are to be measured, it is necessary to compensate the bias current of the op amp.

The logging slope is not temperature compensated. With a five-decade response, the error at the scale extremes will be about 40% (a half stop in photography) for a ±18°C temperature change.

If temperature compensation is desired, it is best to use a center-zero meter to introduce the offset, rather than the reference voltage. This done, temperature compensation can be obtained by making the resistor in series with the meter a copper wire-wound unit.

If this design is to be used for photography, it is important to remember that silicon photodiodes are sensitive to near infrared, whereas ordinary film is not. Therefore, an infrared-stop filter is called for. A blue-enhanced photodiode or an appropriate correction filter would also give best results.

An electronic thermometer design, useful in the range of −55°C to 150°C, is shown in *Figure 35.* The sensor, S1, develops a current that is proportional to absolute temperature. This is given the required offset and range expansion by the reference and op amp, resulting in a direct readout in either °C or °F.



*trim for span

†trim for zero

FIGURE 35. Electronic Thermometer

Meter Circuits (Continued)

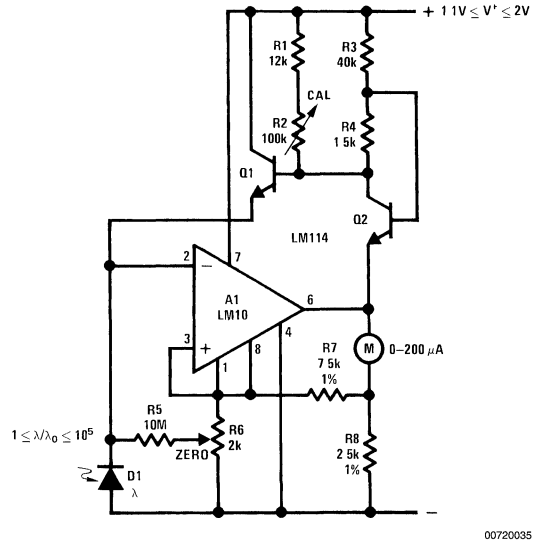


FIGURE 36. Logarithmic Light-Level Meter

Although it can operate down to 1V with better than 0.5°C accuracy, the LM134 is not tested below 1.5V. Maverick units were observed to develop a 1°C error going from 1.5V to 1.2V. This should be kept in mind for high-accuracy applications.

The thermocouple transmitter in *Figure 15* can easily be modified to work with a meter if a broader temperature range is of interest. It would likewise be no great problem adapting resistance or thermistor sensors to this function.

Audio Circuits

As mentioned earlier, the frequency response of the LM10 is not as good as might be desired. The frequency-response curve in *Figure 37* shows that only moderate gains can be realized in the audio range. However, considering the reference, there are two independent amplifiers available, so that reasonable overall performance can be obtained.

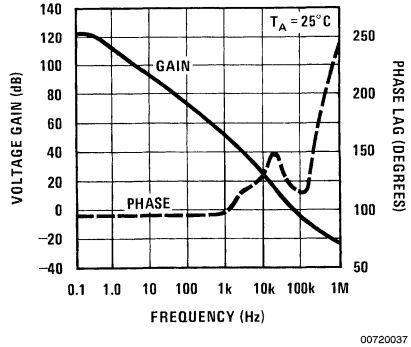


FIGURE 37. Open Loop Frequency Response

Audio Circuits (Continued)

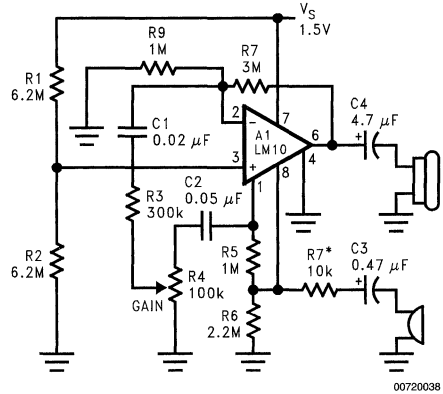
This is illustrated with the microphone amplifier shown in *Figure 38*. The reference, with a 500 kHz unity-gain bandwidth, is used as a preamplifier with a gain of 100. Its output is fed through a gain-control potentiometer to the op amp which is connected for a gain of 10. The combination gives a 60 dB gain with a 10 kHz bandwidth, unloaded, and 5 kHz loaded at 500Ω. Input impedance is 10 kΩ.

Potentially, using the reference as a preamplifier in this fashion can cause excess noise. However, because the reference voltage is low, the noise contribution, which adds root-mean-square, is likewise low. The input noise voltage in this connection is 40–50 nV/$\sqrt{\text{Hz}}$, about equal to that of the op amp.

One point to observe with this connection is that the signal swing at the reference output is strictly limited. It cannot swing much below 150 mV nor closer than 800 mV to the supply. Further, the bias current at the reference feedback terminal lowers the output quiescent level and generates an uncertainty in this level. These facts limit the maximum feedback resistance (R5) and require that R6 be used to optimize the quiescent operating voltage on the output. Even so, the fact that limited swing on the preamplifier can reduce maximum output power with low settings on the gain control must be considered.

In this design, no DC current flows in the gain control. This is perhaps an arbitrary rule, designed to insure long life with noise-free operation. If violations of this rule are acceptable, R5 can be used as the gain control with only the bias current for the reference amplifier (<75 nA) flowing through the wiper. This simplifies the circuit and gives more leeway on getting sufficient output swing from the preamplifier.

The circuit in *Figure 38* can also be modified to provide two-wire transmission for a microphone output.



Z_{OUT} ~ 680Ω, @5 kHz, $A_V \leq$ 1k, f_1 ~ 100 Hz, f_2 ~ 5 kHz, R_L ~ 500, *max gain trim

FIGURE 38. Microphone Amplifier

Conclusions

The applications described here show that some truly unique functions can be performed by the LM10 because of the low-voltage capability and floating mode operation. Among these are accurate, two-terminal comparators that interface directly with most logic forms. They can also drive SCRs in control circuits using low-level sensors like photodiodes or thermocouples, although this was not explored here.

Two-wire transmitters for analog signals were shown to work with a variety of transducers, even to the extent of remotely performing computational functions. These might be used for anything from a microphone preamplifier to a strain gauge measuring stress at some remote location in an aircraft. The power requirements of this IC are modest enough to insure a wide dynamic range and permit operation with lower-voltage supplies.

The IC also proves to be quite useful in regulator circuits, as might be expected from a combined op amp and voltage reference. It makes an efficient series regulator at low voltages. And as a low-level, on-card regulator, it offers greater precision than existing devices. It is also easily applied as a shunt regulator or current regulator.

In the floating mode, it operates with the precision required of laboratory supplies, as either a voltage or current regulator. Maximum output voltage is limited only by discrete pass transistors, because the control circuit sees, at most, a couple volts. Therefore, output voltages of several hundred volts are entirely practical.

A few examples were given of amplifiers and signal conditioners for portable instruments. Emphasis was placed on single-cell operation as this gives the longest life at lowest cost from the smallest power source. The IC is well suited to single-supply operation, where it can be used in any number of standard applications. This can be put to use in digital systems where some linear functions must be performed. The availability of a reference allows precise level shifting or comparisons even when the supply is poorly regulated. The reference can also be used to create an elevated pseudo-ground so that split-supply techniques can be used.

Even when split supplies are available, the increased output capability (40V @ 20 mA) coupled with lower power consumption could well recommend the LM10. This is combined with the more satisfactory fault protection provided by thermal limiting.

Acknowledgement

The authors would like to thank Dick Wong for his assistance in building and checking out the applications described here.

References

1. R. J. Widlar, "Low Voltage Techniques," *IEEE J. Solid-State Circuits*, Dec 1978.

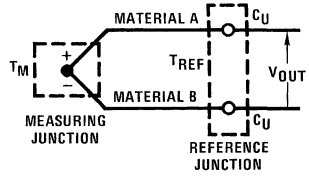
***See Addendum in Application Note TP-14.**

IC Temperature Sensor Provides Thermocouple Cold-Junction Compensation

National Semiconductor
Application Note 225
Michael X. Maida

Introduction

Due to their low cost and ease of use, thermocouples are still a popular means for making temperature measurements up to several thousand degrees centigrade. A thermocouple is made by joining wires of two different metals as shown in *Figure 1*. The output voltage is approximately proportional to the temperature difference between the measuring junction and the reference junction. This constant of proportionality is known as the Seebeck coefficient and ranges from 5 µV/°C to 50 µV/°C for commonly used thermocouples.



$V_{OUT} \cong \alpha(T_M - T_{REF})$

FIGURE 1. Thermocouple

Because a thermocouple is sensitive to a temperature *difference*, the temperature at the reference junction must be known in order to make a temperature measurement. One way to do this is to keep the reference junction in an ice bath. This has the advantage of zero output voltage at 0°C, making thermocouple tables usable. A more convenient approach, known as cold-junction compensation, is to add a compensating voltage to the thermocouple output so that the reference junction appears to be at 0°C independent of the actual temperature. If this voltage is made proportional to temperature with the same constant of proportionality as the thermocouple, changes in ambient temperature will have no effect on output voltage.

An IC temperature sensor such as the LM135/LM235/LM335, which has a very linear voltage vs. temperature characteristic, is a natural choice to use in this compensation circuit. The LM135 operates by sensing the difference of base-emitter voltage of two transistors running at different current levels and acts like a zener diode with a breakdown voltage proportional to absolute temperature at 10 mV/°K. Furthermore, because the LM135 extrapolates to zero output at 0°K, the temperature coefficient of the compensation circuit can be adjusted at room temperature without requiring any temperature cycling.

Sources of Error

There will be several sources of error involved when measuring temperature with thermocouples. The most basic of these is the tolerance of the thermocouple itself, due to varying composition of the wire material. Note that this tolerance states how much the voltage vs. temperature characteristic differs from that of an ideal thermocouple and has nothing to do with nonlinearity. Tolerance is typically ±¾% of reading for J, K, and T types or ±½% for S and R types, so that a measurement of 1000°C may be off by as much as 7.5°C. Special wire is available with half this error guaranteed.

Additional error can be introduced by the compensation circuitry. For perfect compensation, the compensation circuit must match the output of an ice-point-referenced thermocouple at ambient. It is difficult to match the thermocouple's nonlinear voltage vs. temperature characteristic with a linear absolute temperature sensor, so a "best fit" linear approximation must be made. In *Figure 2* this nonlinearity is plotted as a function of temperature for several thermocouple types. The K type is the most linear, while the S type is one of the least linear. When using an absolute temperature sensor for cold-junction compensation, compensation error is a function of both thermocouple nonlinearity and also the variation in ambient temperature, since the straight-line approximation to the thermocouple characteristic is more valid for small deviations.

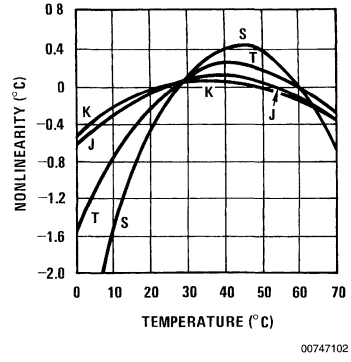


FIGURE 2. Thermocouple Nonlinearity

Of course, increased error results if, due to component inaccuracies, the compensation circuit does not produce the ideal output. The LM335 is very linear with respect to absolute temperature and introduces little error. However, the complete circuit must contain resistors and a voltage reference in order to obtain the proper offset and scaling. Initial tolerances can be trimmed out, but the temperature coefficient of these external components is usually the limiting factor (unless this drift is measured and trimmed out).

Circuit Description

A single-supply circuit is shown in *Figure 3*. R3 and R4 divide down the 10 mV/°K output of the LM335 to match the Seebeck coefficient of the thermocouple. The LM329B and its associated voltage divider provide a voltage to buck out the 0°C output of the LM335. To calibrate, adjust R1 so that

Circuit Description (Continued)

V1 = <5°C T, where <5°C is the Seebeck coefficient (Note 1) and T is the ambient temperature in degrees *Kelvin*. Then, adjust R2 so that V1–V2 is equal to the thermocouple output voltage at the known ambient temperature.

To achieve maximum performance from this circuit the resistors must be carefully chosen. R3 through R6 should be precision wirewounds, Vishay bulk metal or precision metal film types with a 1% tolerance and a temperature coefficient of ±5 ppm/°C or better. In addition to having a low TCR, these resistors exhibit low thermal emf when the leads are at different temperatures, ranging from 3 µV/°C for the TRW MAR to only 0.3 µV/°C for the Vishay types. This is especially important when using S or R type thermocouples that output only 6 µV/°C. R7 should have a temperature coefficient of ±25 ppm/°C or better and a 1% tolerance. Note that the potentiometers are placed where their absolute resistance is not important so that their TCR is not critical. However, the trim pots should be of a stable cermet type. While multi-turn pots are usually considered to have the best resolution, many modern single-turn pots are just as easy to set to within ±0.1% of the desired value as the multi-turn pots.

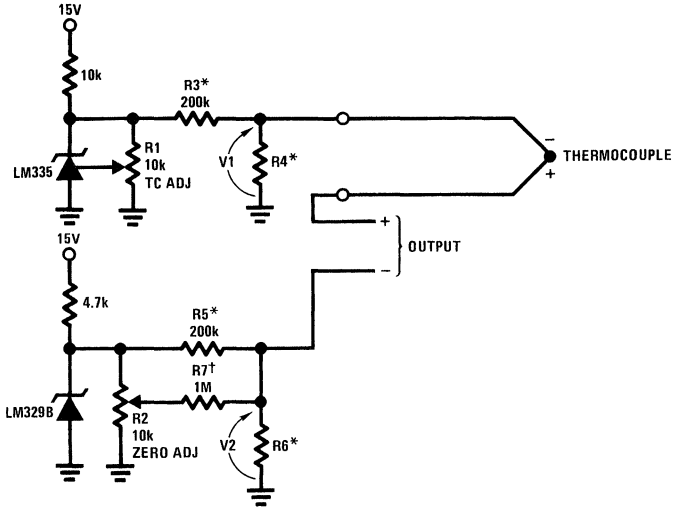
Also single-turn pots usually have superior stability of setting, versus shock or vibration. Thus, good single-turn cermet pots (such as Allen Bradley type E, Weston series 840, or CTS series 360) should be considered as good candidates for high-resolution trim applications, competing with the more obvious (but slightly more expensive) multi-turn trim pots such as Allen Bradley type RT or MT, Weston type 850, or similar.

With a room temperature adjustment, drift error will be only ±½°C at 70°C and ±¼°C at 0°C. Thermocouple nonlinearity results in additional compensation error. The chromel/alumel (type K) thermocouple is the most linear. With this type, a compensation accuracy of ±¾°C can be obtained over a 0°C–70°C range. Performance with an iron-constantan thermocouple is almost as good. To keep the error small for the less linear S and T type thermocouples, the ambient temperature must be kept within a more limited range, such as 15°C to 50°C. Of course, more accurate compensation over a narrower temperature range can be obtained with any thermocouple type by the proper adjustment of voltage TC and offset.

Standard metal-film resistors cost substantially less than precision types and may be substituted with a reduction in accuracy or temperature range. Using 50 ppm/°C resistors, the circuit can achieve ½°C error over a 10°C range. Switching to 25 ppm resistors will halve this error. Tin oxide resistors should be avoided since they generate a thermal emf of 20 µV for 1°C temperature difference in lead temperature as opposed to 2 µV/°C for nichrome or 4.3 µV/°C for cermet types. Resistor networks exhibit good tracking, with 50 ppm/°C obtainable for thick film and 5 ppm/°C for thin film. In order to obtain the large resistor ratios needed, one can use series and parallel connections of resistors on one or more substrates.

Note 1: See Appendix A for calculation of Seebeck coefficient

Circuit Description (Continued)



Thermocouple Type	Seebeck Coefficient (μV/°C)	R4 (Ω)	R6 (Ω)
J	52.3	1050	385
T	42.8	856	315
K	40.8	816	300
S	6.4	128	46.3

*R3 thru R6 are 1%, 5 ppm/°C. (10 ppm/°C tracking.)
†R7 is 1%, 25 ppm/°C.

$$\text{choose R4} = \frac{\alpha}{10\ \text{mV/°C}} \bullet \text{R3}$$

$$\text{choose R6} = \frac{-T_o \bullet \alpha}{V_Z} \bullet (0\ 9R5)$$

$$\text{choose R7} = 5 \bullet \text{R5}$$

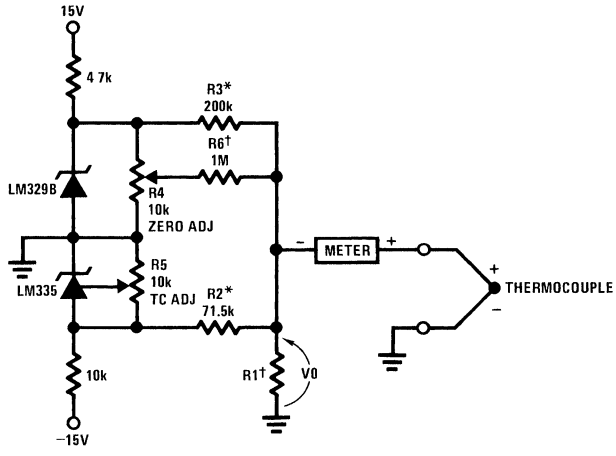
where T_o is absolute zero (−273 16°C)
V_Z is the reference voltage (6 95V for LM329B)

FIGURE 3. Thermocouple Cold-Junction Compensation Using Single Power Supply

A circuit for use with grounded thermocouples is shown in *Figure 4.* If dual supplies are available, this circuit is preferable to that of *Figure 3* since it achieves similar performance with fewer low TC resistors. To trim, short out the LM329B and adjust R5 so that V_o = <5°C T, where <5°C is the Seebeck coefficient of the thermocouple and T is the absolute temperature. Remove the short and adjust R4 so that V_o equals the thermocouple output voltage at ambient. A good grounding system is essential here, for any ground differential will appear in series with the thermocouple output.

An electronic thermometer with a 10 mV/°C output from 0°C to 1300°C is seen in *Figure 5.* The trimming procedure is as follows: first short out the LM329B, the LM335 and the thermocouple. Measure the output voltage (equal to the input offset voltage times the voltage gain). Then apply a 50 mV input voltage and adjust the GAIN ADJUST pot until the output voltage is 12.25V above the previously measured value. Next, short out the thermocouple again and remove the short across the LM335. Adjust the TC ADJUST pot so that the output voltage equals 10 mV/°K times the absolute temperature. Finally, remove the short across the LM329B and adjust the ZERO ADJUST pot so that the output voltage equals 10 mV/°C times the ambient temperature in °C.

Circuit Description (Continued)



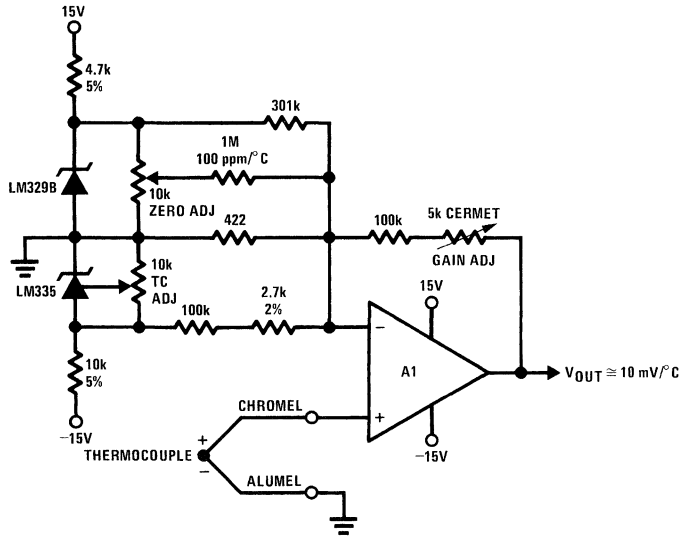
Thermocouple Type	R1 (Ω)	Seebeck Coefficient (μV/°C)
J	377	52.3
T	308	42.8
K	293	40.8
S	45.8	6.4

*R2 and R3 are 1%, 10 ppm/°C. (20 ppm/°C tracking.)

†R1 and R6 are 1%, 50 ppm/°C.

FIGURE 4. Cold-Junction Compensation for Grounded Thermocouple

Circuit Description (Continued)



All fixed resistors ±1%, 25 ppm/°C unless otherwise indicated

A1 should be a low drift type such as LM308A or LH0044C See text

FIGURE 5. Centigrade Thermometer with Cold-Junction Compensation

The error over a 0°C to 1300°C range due to thermocouple nonlinearity is only 2.5% maximum. *Table 1* shows the error due to thermocouple nonlinearity as a function of temperature. This error is under 1°C for 0°C to 300°C but is as high as 17°C over the entire range. This may be corrected with a nonlinear shaping network. If the output is digitized, correction factors can be stored in a ROM and added in via hardware or software.

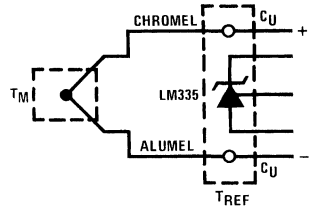
The major cause of temperature drift will be the input offset voltage drift of the op amp. The LM308A has a specified maximum offset voltage drift of 5 µV/°C which will result in a 1°C error for every 8°C change in ambient. Substitution of an LH0044C with its 1 µV/°C maximum offset voltage drift will reduce this error to 1°C per 40°C. If desired, this temperature drift can be trimmed out with only one temperature cycle by following the procedure detailed in Appendix B.

Construction Hints

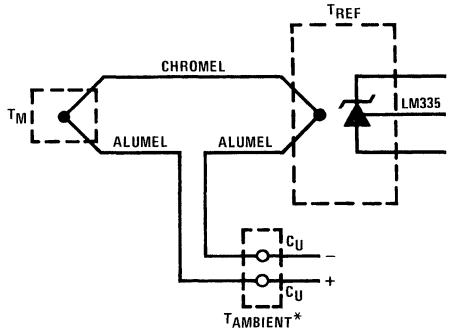
The LM335 must be held isothermal with the thermocouple reference junction for proper compensation. Either of the techniques of *Figure 6a* or *Figure 6b* may be used.

Hermetic ICs use Kovar leads which output 35 µV/°C referenced to copper. In the circuit of *Figure 5*, the low level thermocouple output is connected directly to the op amp input. To avoid this from causing a problem, both input leads of the op amp must be maintained at the same temperature. This is easily achieved by terminating both leads to identically sized copper pads and keeping them away from thermal gradients caused by components that generate significant heat.

Construction Hints (Continued)



a



*Has no effect on measurement

b

FIGURE 6. Methods for Sensing Temperature of Reference Junction

TABLE 1. Nonlinearity Error of Thermometer Using Type K Thermocouple (Scale Factor 25.47°C/μV)

°C	Error (°C)	°C	Error (°C)
10	–0.3	200	–0.1
20	–0.4	210	–0.2
30	–0.4	220	–0.4
40	–0.4	240	–0.6
50	–0.3	260	–0.5
60	–0.2	280	–0.4
70	0	300	–0.1
80	0 2	350	1.2
90	0 4	400	2.8
100	0.6	500	7.1
110	0.8	600	11.8
120	0.9	700	15.7
130	0.9	800	17 6
140	0.9	900	17.1
150	0.8	1000	14.0
160	0.7	1100	8.3
170	0.5	1200	–0.3
180	0.3	1300	–13
190	0.1		

Construction Hints (Continued)

Before trimming, all components should be stabilized. A 24-hour bake at 85°C is usually sufficient. Care should be taken when trimming to maintain the temperature of the LM335 constant, as body heat nearby can introduce significant errors. One should either keep the circuit in moving air or house it in a box, leaving holes for the trimpots.

Conclusion

Two circuits using the LM335 for thermocouple cold-junction compensation have been described. With a single room temperature calibration, these circuits are accurate to ±¾°C over a 0°C to 70°C temperature range using J or K type thermocouples. In addition, a thermocouple amplifier using an LM335 for cold-junction compensation has been described for which worst case error can be as low as 1°C per 40°C change in ambient.

Appendix A Determination of Seebeck Coefficient

Because of the nonlinear relation of output voltage vs. temperature for a thermocouple, there is no unique value of its Seebeck coefficient <5°C. Instead, one must approximate the thermocouple function with a straight line and determine <5°C from the line's slope for the temperature range of interest. On a graph, the error of the line approximation is easily visible as the vertical distance between the line and the nonlinear function. Thermocouple nonlinearity is not so gross, so that a numerical error calculation is better than the graphical approach.

Most thermocouple functions have positive curvature, so that a linear approximation with minimum mean-square error will intersect the function at two points. As a first cut, one can pick these points at the ⅓ and ⅔ points across the ambient temperature range. Then calculate the difference between the linear approximation and the thermocouple. (Note 2) This error will usually then be a maximum at the midpoint and endpoints of the temperature range. If the error becomes too large at either temperature extreme, one can modify the slope or the intercept of the line. Once the linear approximation is found that minimizes error over the temperature range, use its slope as the Seebeck coefficient value when designing a cold-junction compensator.

An example of this procedure for a type S thermocouple is shown in *Table 2*. Note that picking the two intercepts (zero error points) close together results in less error over a narrower temperature range.

Note 2: A collection of thermocouple tables useful for this purpose is found in the Omega Temperature Measurement Handbook published by Omega Engineering, Stamford, Connecticut

TABLE 2. Linear Approximations to Type S Thermocouple

Centigrade Temperature	Type S Thermocouple Output (μV)	Approximation #1 Zero Error at 25°C and 60°C			Approximation #2 Zero Error at 30°C and 50°C		
		Linear Approx.	Error μV	Error °C	Linear Approx.	Error μV	Error °C
0°	0	−17	−17	−2.7°	−16	−16	−2.8°
5°	27	15	−12	−1.9°	16	−11	−1.7°
10°	55	46	−9	−1.4°	47	−8	−1.3°
15°	84	78	−6	−0.9°	78	−6	−0.9°
20°	113	110	−3	−0.5°	110	−3	−0.5°
25°	142	142	0	0	142	−1	−0.2°
30°	173	174	1	0.2°	173	0	0
35°	203	206	3	0.5°	204	1	0.2°
40°	235	238	3	0.5°	236	1	0.2°
45°	266	270	4	0.6°	268	2	0.3°
50°	299	301	2	0.3°	299	0	0
55°	331	333	2	0.3°	330	−1	−0.2°
60°	365	365	0	0	362	−3	−0.5°
65°	398	397	−1	−0.2°	394	−4	−0.6°
70°	432	429	−3	−0.5°	425	−7	−1.1°
		<5°C = 6.4 μV/°C			<5°C = 6.3 μV/°C		
		0.6°C error for 20°C < T < 70°C			0.3°C error for 25°C < T < 50°C		

Note 3: Error is the difference between linear approximation and actual thermocouple output in μV To convert error to °C, divide by Seebeck coefficient.

Appendix B Technique for Trimming Out Offset Drift

Short out the thermocouple input and measure the circuit output voltage at 25˚C and at 70˚C. Calculate the output voltage temperature coefficient, β as shown.

$$\beta = \frac{V_{OUT\,(70°C)} - V_{OUT(25°C)}}{45°K} \text{ in mV/°K}$$

Next, short out the LM329B and adjust the TC ADJ pot so that V_{OUT} = (20 mV/˚K − β) x 298˚K at 25˚C. Now remove the short across the LM329B and adjust the ZERO ADJUST pot so that V_{OUT} = 246 mV at 25˚C (246 times the 25˚C output of an ice-point-referenced thermocouple).

This procedure compensates for all sources of drift, including resistor TC, reference drift (±20 ppm/˚C maximum for the LM329B) and op amp offset drift. Performance will be limited only by TC nonlinearities and measurement accuracy.

References

R. C. Dobkin, "Low Drift Amplifiers," National Semiconductor LB-22, June 1973.

Carl T. Nelson, "Super Matched Bipolar Transistor Pair Sets New Standards for Drift and Noise," National Semiconductor AN-222, February 1979.

Circuitry for Inexpensive Relative Humidity Measurement

National Semiconductor
Application Note 256
Michael X. Maida

Of all common environmental parameters, humidity is perhaps the least understood and most difficult to measure. The most common electronic humidity detection methods, albeit highly accurate, are not obvious and tend to be expensive and complex (See Box). Accurate humidity measurement is vital to a number of diverse areas, including food processing, paper and lumber production, pollution monitoring and chemical manufacturing. Despite these and other applications, little design oriented material has appeared on circuitry to measure humidity. This is primarily due to the small number of transducers available and a generally accepted notion that they are difficult and expensive to signal condition.

Although not as accurate as other methods, the sensor described by the response curve (*Figure 1*) is inexpensive and provides a direct readout of relative humidity. The curve reveals a close exponential relationship between the sensor and relative humidity spanning almost 4 decades of resistance. Linearization of this curve may be accomplished by taking the logarithm of the resistance value and utilizing breakpoint approximation techniques to minimize the residual non-linearities. A further consideration in signal conditioning is that the manufacturer specifies that no significant DC current component may pass through the sensor. This device must be excited with an unbiased AC waveform to preclude detrimental electrochemical migration. In addition, it has a 0.36 RH unit/°C positive temperature coefficient. The sensor is a chemically treated styrene copolymer which has a surface layer whose resistivity varies with relative humidity. Because the humidity sensitive portion of the sensor is at its surface, time response is reasonably rapid and is on the order of seconds.

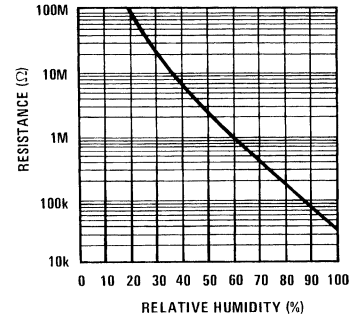


FIGURE 1. Phys-Chemical Research Corp. Model PCRC-55 Humidity Sensor

A block diagram of the concept chosen to instrument the sensor appears in *Figure 2*. An amplitude stabilized square wave which is symmetrical about zero volts is used to provide a precision alternating current through the sensor, satisfying the requirement for a zero DC component drive. The current through the sensor is fed into a current sensitive (e.g. the input is at virtual ground) logarithmic amplifier, which linearizes sensor response. The output of the logarithmic amplifier is scaled, rectified and filtered to provide a DC output which represents relative humidity. Residual non-linearity due to the sensors non-logarithmic response below RH = 40% is compensated by breakpoint techniques in this final stage.

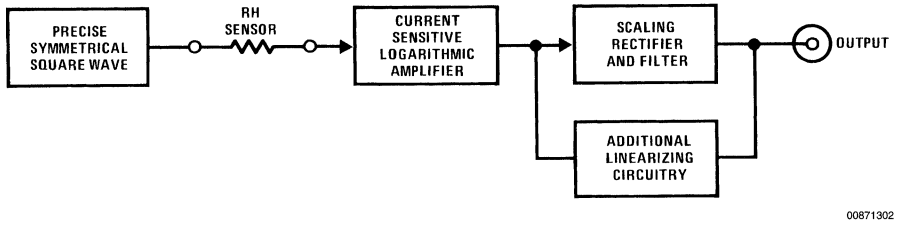
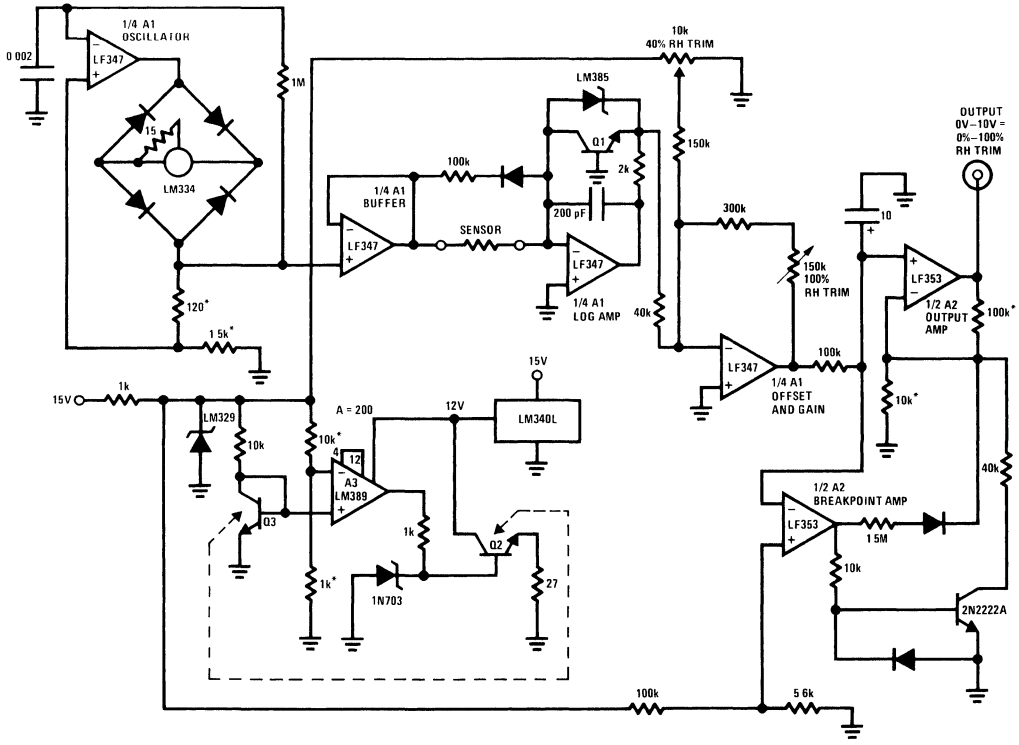


FIGURE 2.

The detailed circuitry appears in *Figure 3*. It is worth noting that the entire function described in *Figure 2* requires a small number of inexpensive ICs. This is accomplished by novel circuitry approaches, especially in the design of the logarithmic amplifier. The stabilized symmetrical square wave is generated by A1, ¼ of an LF347 quad amplifier. A1 is set up in a positive feedback configuration, causing it to oscillate. The output of A1 is current limited and clamped to ground for either polarity output by the LM334 current source diode bridge combination. The LM334 is programmed by the 15Ω resistor to current limit at about 5 mA. This forces the voltage across the 120Ω–1.5 kΩ resistor string to stabilize at about ±8V. Each time A1's output changes state the charging current into the 0.002 µF capacitor reverses, causing the amplifier to switch again when the capacitor reaches a threshold established by the 120Ω–1.5 kΩ divider (waveforms, *Figure 4*). This circuit's output is buffered by the A1 follower. The amplitude stability of the waveform is dependent upon the +0.33%/°C temperature coefficient of the LM334. This T.C. has been intentionally designed into the LM334 so that it may be used in temperature sensing and compensation applications. Here, the negative 0.3%/°C temperature dependence of the humidity sensor is reduced by more than an order of magnitude by the LM334's T.C. and

thermally induced inaccuracy in the humidity sensor's response drops out as an error term. In practice, the LM334 should be mounted in proximity to the humidity sensor. The residual −0.03%/°C temperature coefficient is negligibly small compared to the sensors ±1% accuracy specification.

The output square wave is used to drive current through the sensor and into the summing junction of another ¼ of A1, which is connected as a logarithmic amplifier. On negative cycles of the input waveform the transistor (Q1) in the feedback loop provides logarithmic response, due to the well known relationship between V_{BE} and collector current in transistors. During positive excursions of the input waveform the diode provides feedback to the amplifier's summing junction. In this manner the summing junction always remains at virtual ground while the input current is expressed in logarithmic form by the negative going square wave at the transistor emitter. Since the summing junction is always at ground potential the sensor sees the required symmetrical drive (waveforms, *Figure 5*).



LF347 and LF353 run on ±15V supply
Q1, Q2, Q3 are on LM389 chip
* = 1% Metal Film
▶| = 1N4148

Sensor = PCRC-55 - Phys-Chemical Research Corporation
A1 = LF347
A2 = LF353

00871303

FIGURE 3.

The output of this stage is fed to another ¼ of A1. This amplifier is used to sum in the 40% RH trim and provide adjustable gain to set the 100% RH trim. The output is filtered to DC and routed to one half of A2, an LF353, which unloads the filter and provides additional gain and the final output.

The other ½ of A2 is used to compensate the sensor departure from logarithmic conformity below 40% RH (*Figure 1*). This is accomplished by changing the gain of the output amplifier for RH readings below 40%. The input to the output amplifier is sensed by the breakpoint amplifier. When this input goes below RH = 40% (about 0.36V at the output amplifiers "+" terminal) the breakpoint amplifier swings positive. This turns on the 2N2222A, causing the required gain change to occur at the output amplifier. For RH values above 40% the transistor is off and the circuits linearizing function is determined solely by the logarithmic amplifier.

In logarithmic configurations such as this, Q1's DC operating point will vary wildly with temperature and the circuit normally requires careful attention to temperature compensation, resulting in the expense associated with logarithmic amplifiers. Here, A3, an LM389 audio amplifier IC which also contains three discrete transistors, is used in an unorthodox configuration to eliminate all temperature compensation requirements. In addition, the cost of the log function is reduced by an order of magnitude compared to available ICs

and modules. Q3 functions as a chip temperature sensor while Q2 serves as a heater. The amplifier senses the temperature dependent V_{BE} of Q3 and drives Q2 to servo the chip temperature to the set-point established by the 10 kΩ–1 kΩ divider string. The LM329 reference ensures power supply independence of the temperature control. Q1 operates in this tightly controlled thermal environment (typically 50˚C) and is immune to ambient temperature shifts. The LM340L 12V regulator ensures safe operation of the LM389, a 12V device. The zener at the base of Q2 prevents servo lock-up during circuit start-up. Because of the small size of the chip, warm-up is quick and power consumption low. *Figure 6* shows the thermal servo's performance for a step function of 7˚C change in set-point. The step is shown in trace A while the LM389 output appears in trace B. The output responds almost instantaneously and complete settling to the new set-point occurs within 100 ms.

To adjust this circuit, ground the base of Q2, apply circuit power and measure the collector potential of Q3, at known room temperature. Next, calculate what Q3's collector potential will be at 50˚C, allowing –2.2 mV/˚C. Select the 1k value to yield a voltage close to the calculated 50˚C potential at the LM389's negative input. This can be a fairly loose trim, as the exact chip temperature is unimportant so long as it is stable. Finally, unground Q2's base and the circuit will servo. This may be functionally checked by reading Q3's collector voltage and noting stability within 100 µV (0.05˚C) while blowing on A3.

To calibrate the circuit for RH, place a 35 kΩ resistor in the sensor position and trim the 150 kΩ pot for an output of 10V. Next, substitute an 8 MΩ resistor for the sensor and trim the 10k potentiometer for an output of 4V. Repeat this procedure until the adjustments do not interfere with each other. Finally, substitute a 60 MΩ resistor for the sensor and select the nominal 40 kΩ value in the breakpoint amplifier for a reading of RH = 24%. It may be necessary to select the 1.5 MΩ value to minimize "hop" at the circuit output when the breakpoint is activated. The circuit is now calibrated and will read ambient relative humidity when the PCRC-55 sensor is connected.

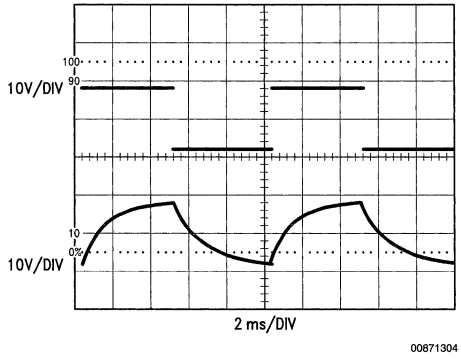


FIGURE 4.

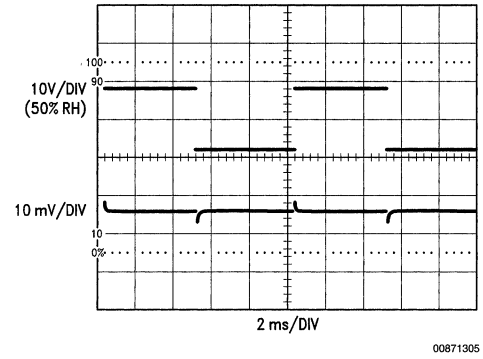


FIGURE 5.

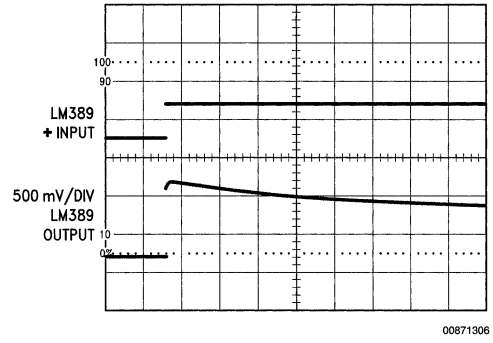


FIGURE 6.

Humidity

Humidity is simply water gas. In air the humidity may vary from zero percent for 90˚F dry air to as much as 4.5 percent for heavily water laden air at 90˚F. The amount of water air will hold is dependent upon temperature. *Relative* humidity is an expression denoting the ratio of water vapor in the air to the amount possible in saturated air at the same temperature.

Some of the more common ways of expressing humidity related information include wet bulb temperature, dew point and frost point. Wet bulb temperature refers to the minimum temperature reached by a wetted thermometer bulb in a stream of air. The dew point is the point at which water saturation occurs in air It is evidenced by water condensation. When temperatures below 0˚C are required to produce this phenomenon it is called the frost point.

Other measurements and ways of expressing humidity exist and are useful in a variety of applications. For additional information consult the bibliography.

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2. "Humidity Measurement"—*Instrumentation Technology*, reprint P. R. Wiederhold. Available from General Eastern Corp.; Watertown, Mass.
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4. "Electric Hygrometers"—Wexler, A.; NBS Circular 586; NBS Washington, D.C. 1957.
5. "An elegant 6-IC circuit gauges relative humidity"—Williams, James M.; *EDN Magazine*, June 5, 1980.

Applying Dual and Quad FET Op Amps

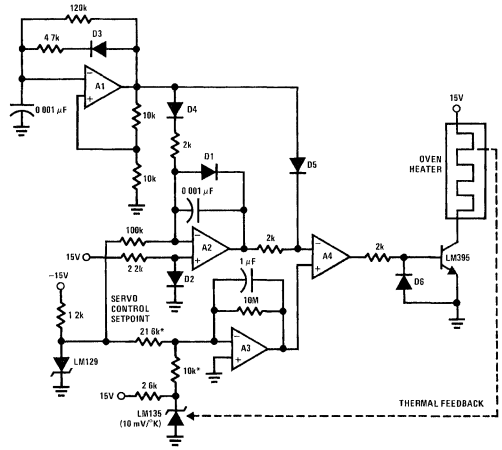
National Semiconductor
Application Note 262
Michael X. Maida

The availability of dual and quad packaged FET op amps offers the designer all the traditional capabilities of FET op amps, including low bias current and speed, and some additional advantages. The cost-per-amplifier is lower because of reduced package costs. This means that more amplifiers are available to implement a function at a given cost, making design easier. At the same time, the availability of more amplifiers-per-dollar means that relatively self contained and sophisticated functions can be designed around a single FET dual or quad package. In addition, duals and quads require less board space, fewer bypass capacitors and less power supply bussing. An inventive designer can capitalize on all of these advantages to produce complex circuit functions at low cost. An example is shown in *Figure 1*.

High Efficiency Precision Oven Temperature Controller

In this circuit, a complete, high efficiency pulse width modulating temperature controller is built around a single LF347 package. In *Figure 1*, A1 functions as an oscillator whose output (Trace A, *Figure 2*) periodically resets the A2 integrator output (Trace B, *Figure 2*) back to zero volts. Each time A1's output goes high, a large positive current is forced into A2's summing junction, overcoming the negative current that flows through the 100 kΩ resistor into the LM129 reference. This forces A2's output to head in a negative-going direction ultimately limited by the diode feedback-bound. Another diode provides bias at A2's "+" input to compensate the bound diode and A2's output settles very near zero volts. When the positive output pulse from A1 ends, the positive current into A2's summing junction ceases and A2's output ramps linearly until the next reset pulse.

A3 functions as a current summing servo-amplifier which compares the currents derived from the LM135 temperature sensor and the LM129 reference. In this example A3 operates at a gain of 1000 with a 1 µF capacitor providing 0.1 Hz servo response. A3's output represents the amplified difference between the LM135's temperature and the desired control setpoint, which may be varied by altering the 21.6k value. In this circuit the 21.6k resistor provides a setpoint of 49°C. A3's output is compared to the ramp output of A2 and A4, which is set up as a comparator. A4's output will only be high during the time A3's output is greater than the ramp voltage. The ramp reset pulse is diode-summed with the ramp output (Trace C, *Figure 2*) at A4 to prevent A4's output from going high during the period of the reset pulse. A4's output biases the LM395 power transistor which switches power to the heater (Trace D, *Figure 2*). If the LM135 sensor is tightly coupled to the heater and the oven is well insulated, this controller will easily hold 0.05°C over wide excursions of ambient temperature.



01258701

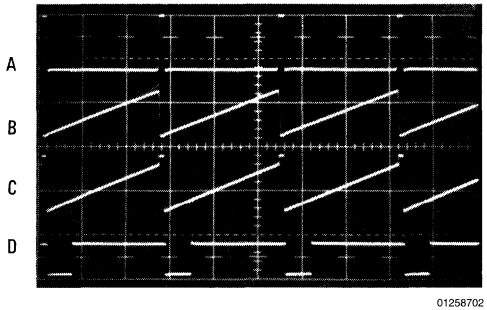
All diodes = 1N4148

* = Low TC, metal-film types

A1-A4 = LF347 quad

FIGURE 1. Connecting appropriate components to an LF347 quad FET op amp IC produces a high efficiency precision oven temperature controller. This design can hold a temperature within 0.05°C despite wide ambient temperature fluctuations.

High Efficiency Precision Oven Temperature Controller (Continued)



01258702

Trace	Vertical	Horizontal
A	20V/Div	
B	10V/Div	50 µs/Div
C	10V/Div	
D	20V/Div	

FIGURE 2. Oven-controller waveforms from *Figure 1* circuit show A1's oscillator output (Trace A) and A2's integrator output (B) as the latter resets periodically to 0V. Trace C displays A4's ramp input, and (D) indicates the LM395's power input to the oven heater.

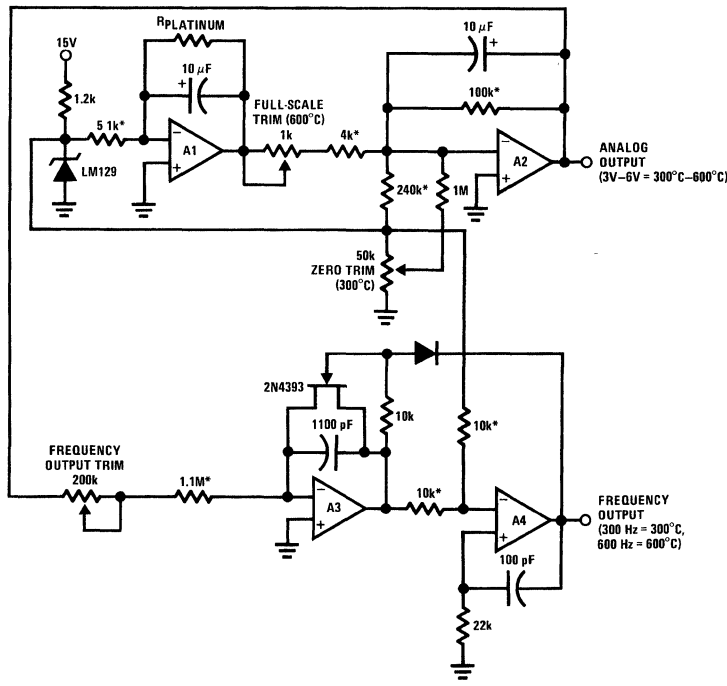
Platinum RTD High Temperature Thermometer with Analog and Digital Outputs

Another temperature related circuit appears in *Figure 3* In this circuit an LF347 is used to signal condition a Platinum RTD and provide simultaneous analog and frequency outputs. These outputs are accurate to ±1°C over a range of 300°C–600°C (572°F–1112°F). Although the circuit maintains linearity over a much wider range the non-linear response of the RTD over wide range is the limitation to accurate, wide range operation (see graph, *Figure 4*).

A1 functions as a negative gain inverter to drive a constant current through the platinum sensor. The LM129 and the 5.1k resistor provide the current reference. Because A1 operates at negative gain the voltage across the sensor is extremely low and self-heating induced errors are eliminated. A1's output potential, which varies with the platinum sensor's temperature, is fed to A2. A2 provides scaled gain and offsetting so that its output will swing from 3.00V to 6.00V for a 300°C to 600°C temperature swing at the platinum sensor.

A3 and A4 form a voltage-to-frequency converter which generates a 300 Hz to 600 Hz output from A2's 3V to 6V analog output. A3 integrates in a negative-going direction at a slope which is linearly dependent upon A2's output voltage. A4 compares A3's negative ramp to the LM129's positive reference voltage by current summing in the 10 kΩ resistors. When the negative value of the ramp just exceeds the LM129 voltage A4's output goes positive, turning on the 2N4393 FET and resetting the A3 integrator. AC feedback at A4 causes it to "hang up" in the positive state long enough to completely discharge the integrator capacitor.

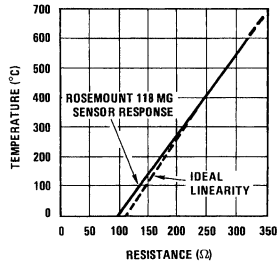
Platinum RTD High Temperature Thermometer with Analog and Digital Outputs (Continued)



RPLATINUM = Rosemount 118 MG
= 214 2Ω at 300°C (572°F)
= 318 2Ω at 600°C (1112°F)
All diodes = 1N4148
A1-A4 = LF347 quad
* = Low TC, metal-film types

FIGURE 3. Generate simultaneous analog level and frequency outputs using one LF347 package by signal-conditioning a platinum RTD sensor. You can calibrate this high temperature (300°C to 600°C) measuring circuit to ±1°C by using three trimming pots.

Platinum RTD High Temperature Thermometer with Analog and Digital Outputs (Continued)



01258704

Temperature(°C)	Resistance(Ω)
600	318.2
500	284.7
400	249.8
300	219.2
200	177.3
100	139.2
0	100.0

FIGURE 4. A platinum RTD sensor's resistance decreases linearly from 600°C to 300°C. Then, from 300°C to 0°C, the sensor's resistance deviates from a straight line slope and degrades the *Figure 3* circuit's accuracy beyond ±1°C.

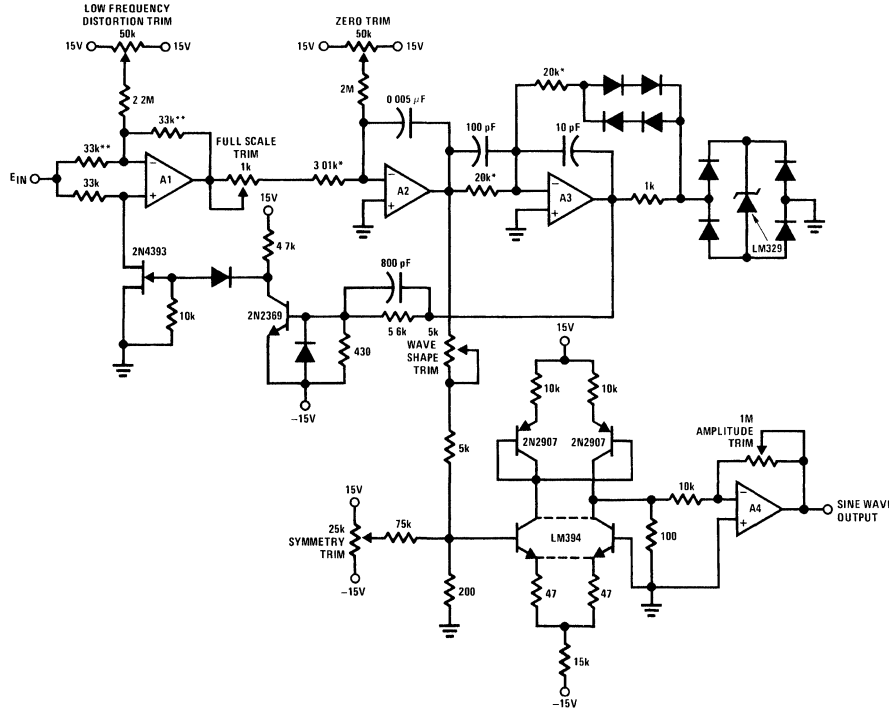
To calibrate this circuit, substitute a high quality decade box (e.g., General Radio #1432-K) for the sensor. Alternately adjust the zero (300°C) and full-scale (600°C) potentiometers for the resistance values noted in *Figure 4* until A2's output is calibrated. Next, adjust the 200 kΩ frequency output trim so the frequency output corresponds to the analog value at A2's output.

Voltage Controlled Sine Wave Oscillator

Figure 5 diagrams a very high performance voltage controlled sine wave oscillator which uses a single LF347 package. For a 0V–10V input the circuit produces sine wave outputs of 1 Hz to 20 kHz with better than 0.2% linearity. In addition, distortion is about 0.4% and the sine wave output frequency and amplitude settle instantaneously to a step input change. The circuit's sine wave output is achieved by non-linearly shaping the triangle wave output of a voltage-to-frequency converter.

Assume the 2N4393 FET is on and A1's output has just gone low. With the FET on, A1's "+" input is grounded and A1 functions as a unity gain inverter. In this state its output will be equal to $-E_{IN}$ (Trace A, *Figure 6*). This negative voltage is applied to the A2 integrator which responds by ramping in a positive direction (Trade B, *Figure 6*). This positive-going ramp is compared by A3 to the LM329 7V reference which is contained within its symmetrically bounded positive feedback loop. The paralleled diodes compensate the diodes in the bridge. When the positive-going ramp voltage just nulls out the –7V produced by the LM329, diode bound A3's output goes positive (Trace D, *Figure 6*). The 100 pF capacitor provides a frequency adaptive trim to A3's trip point, aiding V/F linearity at high frequencies by compensating A3's relatively slow response time when used as a comparator. The 10 pF capacitor provides AC positive feedback to A3's positive input (Trace C, *Figure 6*). The positive output of A3 is inverted by the 2N2369 transistor which also has the effect of further shortening A3's response time. It does this by using a heavy feed-forward capacitor in its base drive line. This allows the transistor to complete switching just barely after the A3 output has begun to move! (Trace E, *Figure 6*). The 2N2369's negative output turns off the 2N4393 FET. This lifts A1's "+" input from ground and causes A1 to become a unity gain follower. This forces A1's output to immediately slew to the value of E_{IN}. This causes the A2 integrator to reverse in direction, forming a triangle wave. When A2 ramps far enough negative A3 will again switch and the entire cycle will repeat. The triangle output at A2 is fed to the discrete transistors which form a sine shaper. This configuration uses the logarithmic relationship between collector current and V_{BE} in transistors to smooth the triangle wave. The last amplifier in the quad package provides gain and buffering and furnishes the sine wave output (Trace F, *Figure 6*).

Voltage Controlled Sine Wave Oscillator (Continued)



* = 1% metal-film resistors

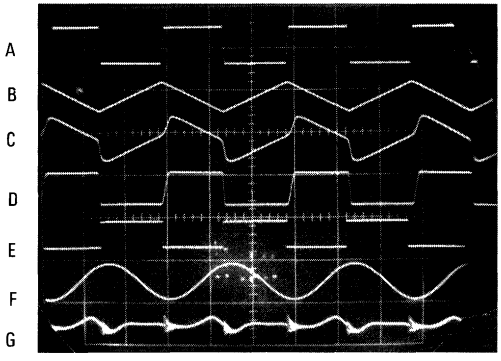
** = Match to 0 1%

All diodes = 1N4148

A1–A4 = LF347 quad

FIGURE 5. An LF347-based voltage-controlled sine wave oscillator combines high performance with versatility. For 0V to 10V inputs, this circuit generates 1 Hz to 20 kHz outputs with better than 0.2% linearity and only 0.4% distortion.

Voltage Controlled Sine Wave Oscillator (Continued)



Trace	Vertical	Horizontal
A	20V/Div	
B	20V/Div	
C	10V/Div	
D	20V/Div	20 µs/Div
E	50V/Div	
F	2V/Div	
G	0.2VDiv	

FIGURE 6. Waveforms from the oscillator shown in *Figure 5* show that upon receiving A1's negative voltage (Trace A), A2 ramps in a positive direction (B). This ramp joins the AC feedback delivered to A3's positive input (C); Trace D depicts A3's positive-going output. This output in turn is inverted by the 2N2369 transistor (E), which turns off the 2N4393 and drives A1's positive input above ground. A2's triangle output also connects to four sine-shaper transistors and A4 and finally emerges as the circuit's sine wave output (F). A distortion analyzer's output (G) shows the circuit's minimum distortion products after trimming.

To calibrate the circuit apply 10V to the input and adjust the wave shape trim and symmetry trim for minimum distortion on a distortion analyzer. Next, adjust the input voltage for an output frequency of 10 Hz and trim the low frequency distortion potentiometer for minimum indication on the distortion analyzer. Finally, alternately adjust the zero and full-scale potentiometers so that inputs of 500 µV and 10V yield respective outputs of 1 Hz and 20 kHz. Distortion products are shown in Trace G, *Figure 6*.

This circuit provides an unusually clean and wide ranging response to rapidly changing inputs, something most sine wave oscillators cannot do. *Figure 7* shows the circuit's response to a 10V ramp applied to the input. The output is singularly clean, with no untoward dynamics, even during or following the high speed reset of the ramp.

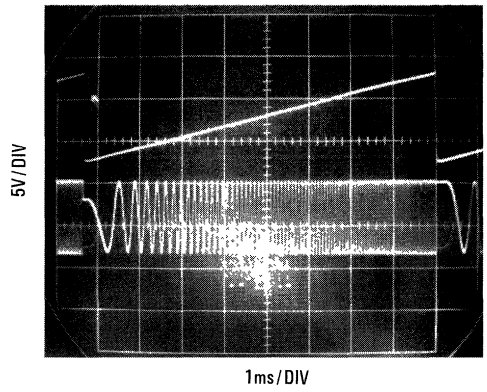


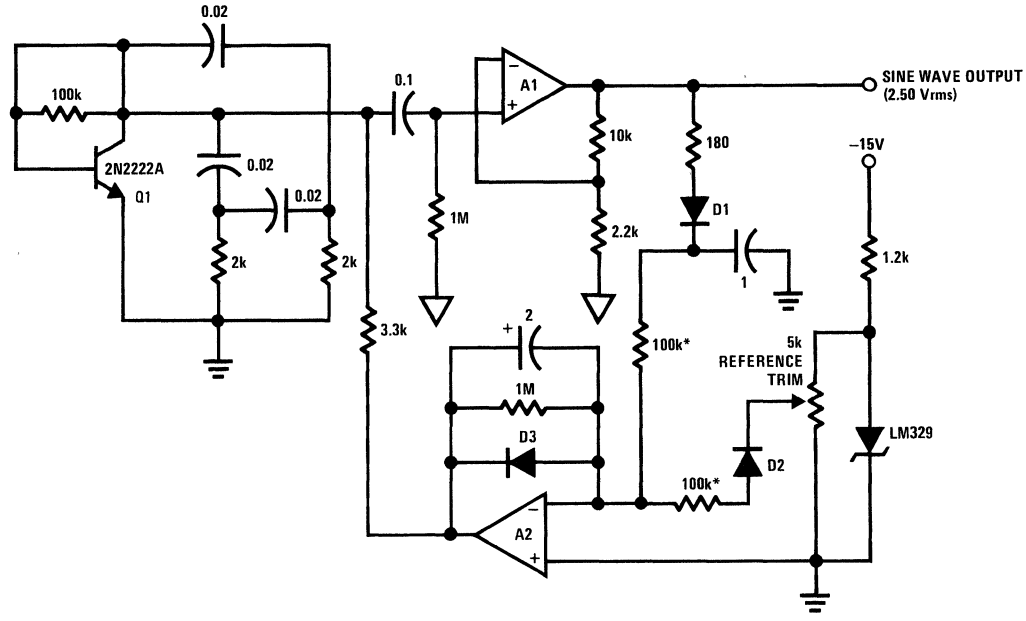
FIGURE 7. Applying a 10V ramp input (top trace) to the *Figure 5* circuit's input produces an extremely clean output (bottom trace) with no glitches, ringing or overshoot, even during or after the ramp's high speed reset.

Sine Wave Voltage Reference

Figure 8 depicts a simple and economical sine wave circuit which provides a fixed 1 kHz output with a precise 2.50 Vrms amplitude. The circuit may be used as inexpensive AC calibration source or anywhere an amplitude stabilized AC source is required. Q1 is set up in a phase shift oscillator configuration and oscillates at 1 kHz. The sine wave at Q1's collector is AC coupled to A1, which has a closed loop gain of about 5. A1's output, which is the circuit's output, is half-wave rectified by the diode and a DC potential appears across the 1 µF capacitor.

This positive voltage is compared by A2 to a voltage derived from the LM329 reference. The diode in the potentiometer wiper arm compensates the rectifying diode. The diode in A2's feedback loop prevents negative voltages from being applied to Q1 (and the feedback capacitor, an electrolytic) on start-up. A2 amplifies the difference of the reference and output signals at a gain of 10. The output of A2 is used to provide collector bias for Q1, completing an amplitude stabilizing feedback loop around the oscillator. The 2 µF electrolytic provides stable loop compensation. The 5 kΩ potentiometer is adjusted so that the circuit output is exactly 2.50V. This output will show less than 1 mV shift for ±5V variation in either supply. Drift is typically 250 µV/°C and distortion is inside 1%.

Sine Wave Voltage Reference (Continued)



All diodes = 1N4148
All capacitors in μF
* = 1% metal-film types
A1, A2 = LF353 dual

FIGURE 8. Reduce parts count and save money by basing this precision sine wave voltage reference on an LF353 dual FET op amp IC. This circuit generates a 1 kHz sine wave at 2.50 Vrms. The 2N2222A transistor functions as a phase-shift oscillator. The A1, A2 combination amplifies and amplitude stabilizes the circuit's sine wave output.

Analog-to-Digital Converter

An extremely versatile integrating analog-to-digital converter appears in *Figure 9.* A single LF347 quad implements the A/D converter which can be either internally or externally triggered. As shown, the converter provides a 10-bit serial output word with a 10 ms full-scale conversion time.

To understand this circuit assume the mode select switch is in the "free run with delay" position and the 2N4393 FET has just been turned off. The A2 integrator, biased from the LM129 reference, begins to ramp in a negative-going direction (Trace B, *Figure 10*). The 2N2222A transistor provides a −0.6V or a +7V feedback output bound for A4, keeping its output from saturating and aiding high speed response. AC positive feedback assures clean transitions. A3 is set up as a 100 kHz oscillator. The LM329 and the diodes provide a temperature compensated bipolar switching threshold reference for the oscillator. During the time A4 is low the pulses from A3's output are passed by the 2N3904 transistor. When A4 goes high the 2N3904 is biased on and no more pulses appear (Trace D, *Figure 10*). Since A2's output ramp is linear the length of time A4 spends low is directly proportional to the value of E_{IN}. The number of pulses at the 2N3904 output provides a digital indication of this information. A2's ramp continues to run after A4 goes high and the actual conversion ends. When the time constant associated with the "free run with delay" mode charges to 2V A1's output goes high (Trace A, *Figure 10*), turning on the 2N4393 FET, which resets the integrator. A1 stays high until the AC feedback provided by the 150 pF capacitor decays below 2V. At this point A1 goes low, A2 begins to ramp and a new conversion cycle starts. False data at the converter output is prevented during the time A1 is high by resistor diode gating at the 2N3904 base.

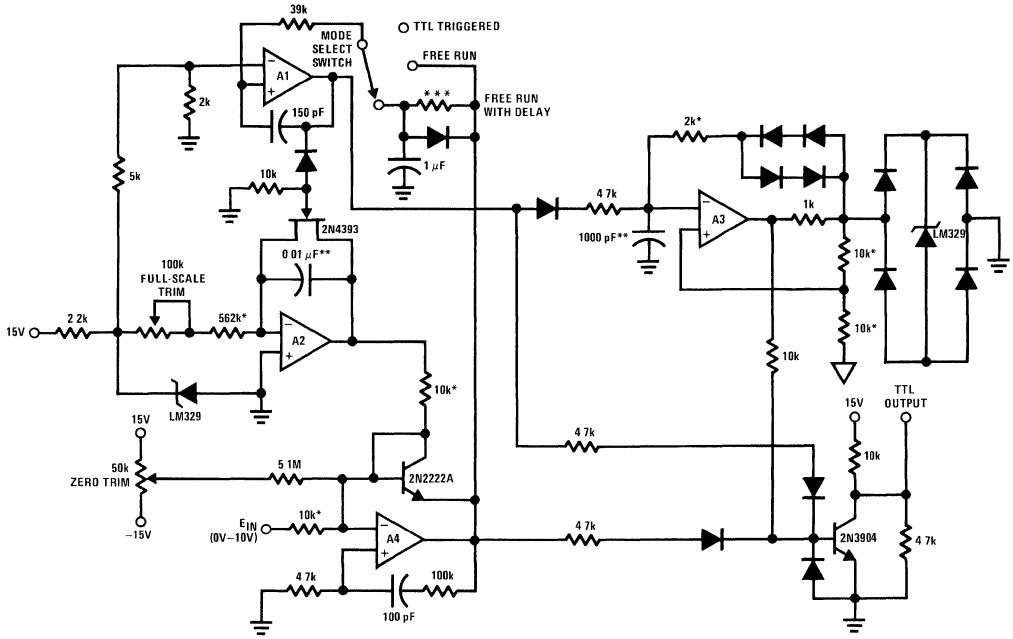
Normally, a ±1 count uncertainty at the output will be introduced because the 100 kHz clock runs asynchronously with the conversion cycle. This problem is eliminated by the diode and 4.7k resistor which run between A1's output and the A3 negative input. These components force the oscillator to synchronize to the conversion cycle at each falling edge of A1's output. The length of time between conversions in the "free run with delay" mode is adjustable by varying the RC combination associated with this switch position. The converter may be triggered externally by any source with a greater than 2V amplitude. In the "free run" mode the converter self triggers immediately after A4 goes high. Thus, the conversion time will vary with the input voltage.

This is graphically illustrated in the photo of *Figure 11.* Here, a positive biased sine wave (Trace B, *Figure 11*) is fed into

Analog-to-Digital Converter

(Continued)

the A/D input. Because the A/D resets and self triggers immediately after converting, the A2 ramp output shapes a ramp constructed envelope of the input signal (Trace C, *Figure 11*). Trace A shows this in time expanded form. Note that the −120 ppm/°C temperature coefficients of the Polystyrene capacitors in the integrator and oscillator will tend to track, aiding drift performance in this circuit. From 15°C to 35°C this circuit achieves 10-bit absolute accuracy. To calibrate this circuit apply 10.00V to the input and adjust the FS trim for 1000 pulses out per conversion. Next, apply 0.05V and adjust zero trim for 5 pulses out per conversion. Repeat this procedure until the adjustments converge.



All diodes = 1N4148

*** = 2 kΩ to 20 MΩ typ for delays up to 20 sec

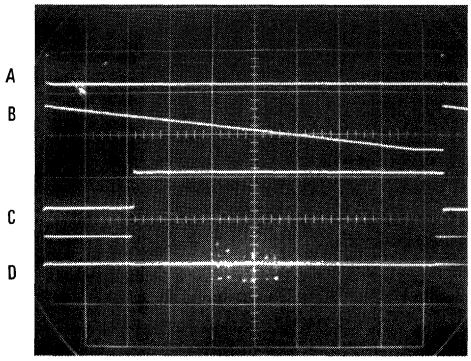
** = Polystyrene types

* = Metal-film types A1–A4 = LF347 quad

FIGURE 9. Three mode select switch positions offer a choice of internal or external trigger conditions for this integrating A/D converter. Over 15°C to 35°C, this trimmable converter provides a 10-bit serial output, converts in 10 ms and accepts 0V to 10V inputs.

Analog-to-Digital Converter

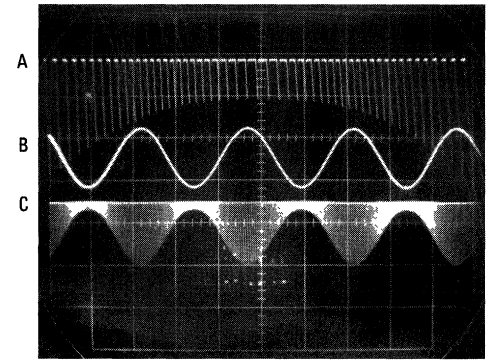
(Continued)



01258710

Trace	Vertical	Horizontal
A	5V/Div	
B	10V/Div	1 ms/Div
C	10V/Div	
D	5V/Div	

FIGURE 10. Depicting the operation of *Figure 9* A/D circuit in "free run with delay" mode, Trace A shows A1's output low. In this state, integrator A2 starts to ramp in a negative-going direction (Trace B). When A2's ramp potential barely exceeds the input voltage's negative value, A4's output goes high (C). This transition turns on the 2N3904 transistor, which shuts off the TTL output pulse train (D).



01258711

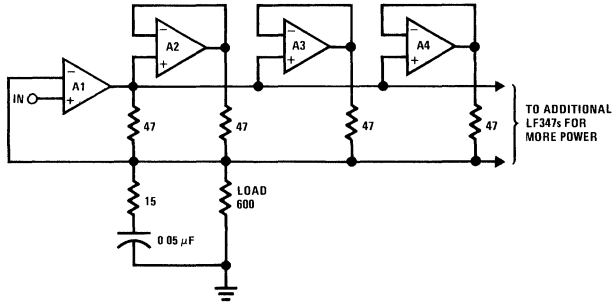
Trace	Vertical	Horizontal
A	1V/Div	2 ms/Div
B	5V/Div	20 ms/Div
C	5V/Div	20 ms/Div

FIGURE 11. Illustrating the A/D converter's operation in the "free run" mode, Trace B shows a positively biased sine wave input. Because reset and self trigger occur instantly after conversion. A2's output produces a ramp-constructed envelope of the input (Trace C). Trace A shows a time expanded form of the envelope waveform.

High Output Current Amplifier

Figure 12 shows a scheme for obtaining high output current into a load by using all 4 amplifiers in an LF347 to supply output power. It operates on the principle that all the amplifiers have to supply the same current as A1, whether that current is plus, minus or zero. A single LF347 can be used to drive a 600Ω load to ±11V in this fashion. Two LF347 packages permit ±40 mA of output current. The series RC damper prevents oscillations. The circuit of *Figure 13* is similar but features a gain of 10 and output to a floating load. A1 amplifies the signal and A2 helps it drive the load. A3 operates as a unity gain inverter and A4 helps it to drive the load. This circuit will easily drive a 2000Ω floating load to ±20V.

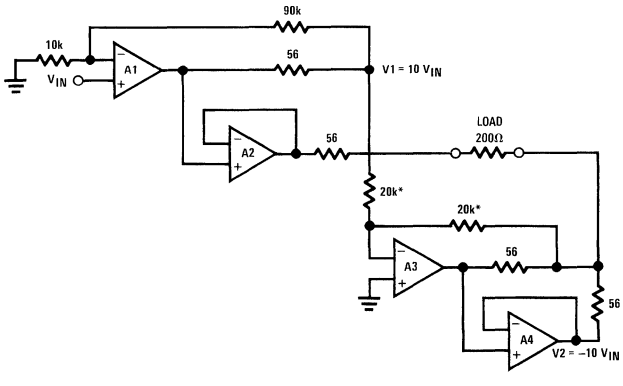
High Output Current Amplifier (Continued)



01258712

A1–A4 = LF347 quad

FIGURE 12. Utilizing current-amplifying capabilities, one LF347 can drive a 600Ω load to ±11V. For additional power, two LF347's can supply an output current of ±40 mA.



01258713

*= 1% types

A1–A4 = LF347 quad

FIGURE 13. Configured as a high output current amplifier with a gain of 10, this LF347 circuit can drive a 200Ω floating load to ±20V.

Sine Wave Generation Techniques

National Semiconductor
Application Note 263
Michael X. Maida

Producing and manipulating the sine wave function is a common problem encountered by circuit designers. Sine wave circuits pose a significant design challenge because they represent a constantly controlled linear oscillator. Sine wave circuitry is required in a number of diverse areas, including audio testing, calibration equipment, transducer drives, power conditioning and automatic test equipment (ATE). Control of frequency, amplitude or distortion level is often required and all three parameters must be simultaneously controlled in many applications.

A number of techniques utilizing both analog and digital approaches are available for a variety of applications. Each individual circuit approach has inherent strengths and weaknesses which must be matched against any given application (see table).

Phase Shift Oscillator

A simple inexpensive amplitude stabilized phase shift sine wave oscillator which requires one IC package, three transistors and runs off a single supply appears in *Figure 1*. Q2, in combination with the RC network comprises a phase shift configuration and oscillates at about 12 kHz. The remaining circuitry provides amplitude stability. The high impedance output at Q2's collector is fed to the input of the LM386 via the 10 µF-1M series network. The 1M resistor in combination with the internal 50 kΩ unit in the LM386 divides Q2's output by 20. This is necessary because the LM386 has a fixed gain of 20. In this manner the amplifier functions as a unity gain current buffer which will drive an 8Ω load. The positive peaks at the amplifier output are rectified and stored in the 5 µF capacitor. This potential is fed to the base of Q3. Q3's collector current will vary with the difference between its base and emitter voltages. Since the emitter voltage is fixed by the LM313 1.2V reference, Q3 performs a comparison function and its collector current modulates Q1's base voltage. Q1, an emitter follower, provides servo controlled drive to the Q2 oscillator. If the emitter of Q2 is opened up and driven by a control voltage, the amplitude of the circuit output may be varied. The LM386 output will drive 5V (1.75 Vrms) peak-to-peak into 8Ω with about 2% distortion. A ±3V power supply variation causes less than ±0.1 dB amplitude shift at the output.

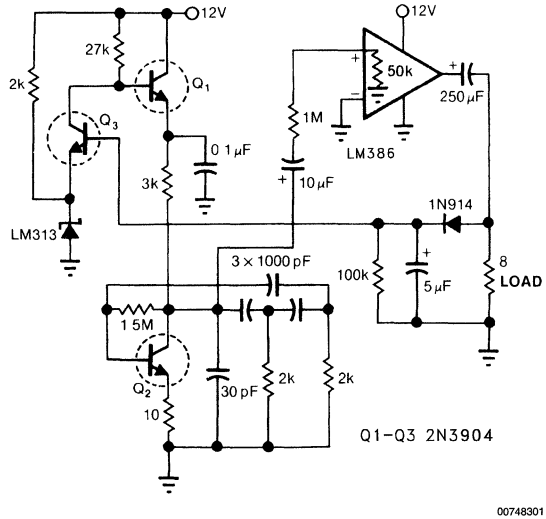


FIGURE 1. Phase-shift sine wave oscillators combine simplicity with versatility. This 12 kHz design can deliver 5 Vp-p to the 8Ω load with about 2% distortion.

Sine-Wave-Generation Techniques

Type	Typical Frequency Range	Typical Distortion (%)	Typical Amplitude Stability (%)	Comments
Phase Shift	10 Hz–1 MHz	1–3	3 (Tighter with Servo Control)	Simple, inexpensive technique. Easily amplitude servo controlled. Resistively tunable over 2:1 range with little trouble. Good choice for cost-sensitive, moderate-performance applications. Quick starting and settling.
Wein Bridge	1 Hz–1 MHz	0.01	1	Extremely low distortion. Excellent for high-grade instrumentation and audio applications. Relatively difficult to tune—requires dual variable resistor with good tracking Take considerable time to settle after a step change in frequency or amplitude.
LC Negative Resistance	1 kHz–10 MHz	1–3	3	Difficult to tune over wide ranges. Higher Q than RC types. Quick starting and easy to operate in high frequency ranges.
Tuning Fork	60 Hz–3 kHz	0.25	0.01	Frequency-stable over wide ranges of temperature and supply voltage. Relatively unaffected by severe shock or vibration. Basically untunable.
Crystal	30 kHz–200 MHz	0.1	1	Highest frequency stability. Only slight (ppm) tuning possible. Fragile.
Triangle-Driven Break-Point Shaper	< 1 Hz–500 kHz	1–2	1	Wide tuning range possible with quick settling to new frequency or amplitude.
Triangle-Driven Logarithmic Shaper	< 1 Hz–500 kHz	0.3	0.25	Wide tuning range possible with quick settling to new frequency or amplitude. Triangle and square wave also available. Excellent choice for general-purpose requirements needing frequency-sweep capability with low-distortion output.
DAC-Driven Logarithmic Shaper	<1 Hz–500 kHz	0.3	0.25	Similar to above but DAC-generated triangle wave generally easier to amplitude-stabilize or vary. Also, DAC can be addressed by counters synchronized to a master system clock.
ROM-Driven DAC	1 Hz–20 MHz	0.1	0.01	Powerful digital technique that yields fast amplitude and frequency slewing with little dynamic error. Chief detriments are requirements for high-speed clock (e.g., 8-bit DAC requires a clock that is 256 x output sine wave frequency) and DAC glitching and settling, which will introduce significant distortion as output frequency increases.

Low Distortion Oscillation

In many applications the distortion levels of a phase shift oscillator are unacceptable. Very low distortion levels are provided by Wein bridge techniques. In a Wein bridge stable oscillation can only occur if the loop gain is maintained at unity at the oscillation frequency. In *Figure 2a* this is achieved by using the positive temperature coefficient of a small lamp to regulate gain as the output attempts to vary. This is a classic technique and has been used by numerous circuit designers* to achieve low distortion. The smooth limiting action of the positive temperature coefficient bulb in combination with the near ideal characteristics of the Wein network allow very high performance. The photo of *Figure 3* shows the output of the circuit of *Figure 2a*. The upper trace is the oscillator output. The middle trace is the downward slope of the waveform shown greatly expanded. The slight aberration is due to crossover distortion in the FET-input LF155. This crossover distortion is almost totally responsible for the sum of the measured 0.01% distortion in this oscillator. The output of the distortion analyzer is shown in the bottom trace. In the circuit of *Figure 2b*, an electronic equivalent of the light bulb is used to control loop gain. The zener diode determines the output amplitude and the loop time constant is set by the 1M-2.2 µF combination.

Low Distortion Oscillation (Continued)

The 2N3819 FET, biased by the voltage across the 2.2 µF capacitor, is used to control the AC loop gain by shunting the feedback path. This circuit is more complex than *Figure 2a* but offers a way to control the loop time constant while maintaining distortion performance almost as good as in *Figure 2.*

Note: * Including William Hewlett and David Packard who built a few of these type circuits in a Palo Alto garage about forty years ago

High Voltage AC Calibrator

Another dimension in sine wave oscillator design is stable control of amplitude. In this circuit, not only is the amplitude stabilized by servo control but voltage gain is included within the servo loop.

A 100 Vrms output stabilized to 0.025% is achieved by the circuit of *Figure 4.* Although complex in appearance this circuit requires just 3 IC packages. Here, a transformer is used to provide voltage gain within a tightly controlled servo loop. The LM3900 Norton amplifiers comprise a 1 kHz amplitude controllable oscillator. The LH0002 buffer provides low impedance drive to the LS-52 audio transformer. A voltage gain of 100 is achieved by driving the secondary of the transformer and taking the output from the primary. A current-sensitive negative absolute value amplifier composed of two amplifiers of an LF347 quad generates a negative rectified feedback signal. This is compared to the LM329 DC reference at the third LF347 which amplifies the difference at a gain of 100. The 10 µF feedback capacitor is used to set the frequency response of the loop. The output of this amplifier controls the amplitude of the LM3900 oscillator thereby closing the loop. As shown the circuit oscillates at 1 kHz with under 0.1% distortion for a 100 Vrms (285 Vp-p) output. If the summing resistors from the LM329 are replaced with a potentiometer the loop is stable for output settings ranging from 3 Vrms to 190 Vrms (542 Vp-p!) with no change in frequency. If the DAC1280 D/A converter shown in dashed lines replaces the LM329 reference, the AC output voltage can be controlled by the digital code input with 3 digit calibrated accuracy.

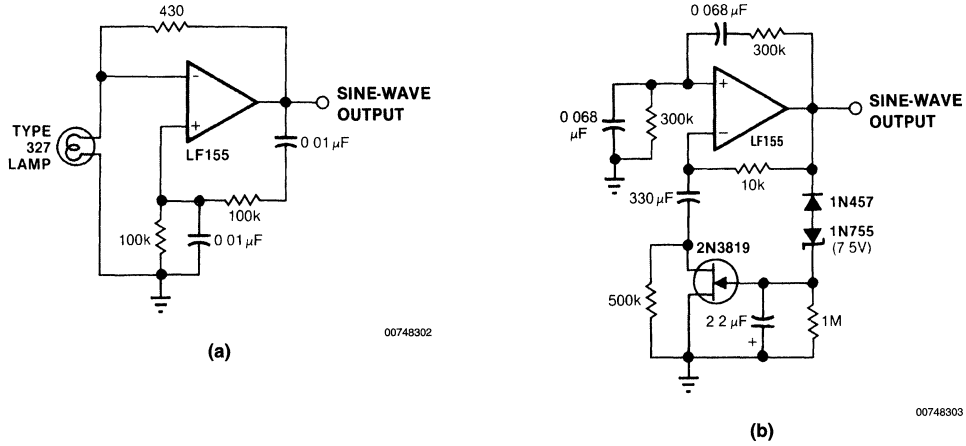
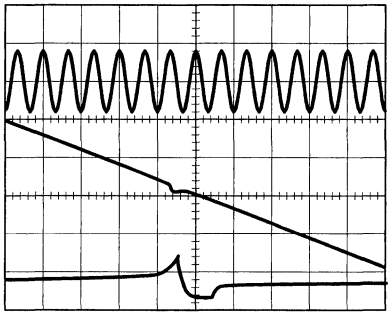


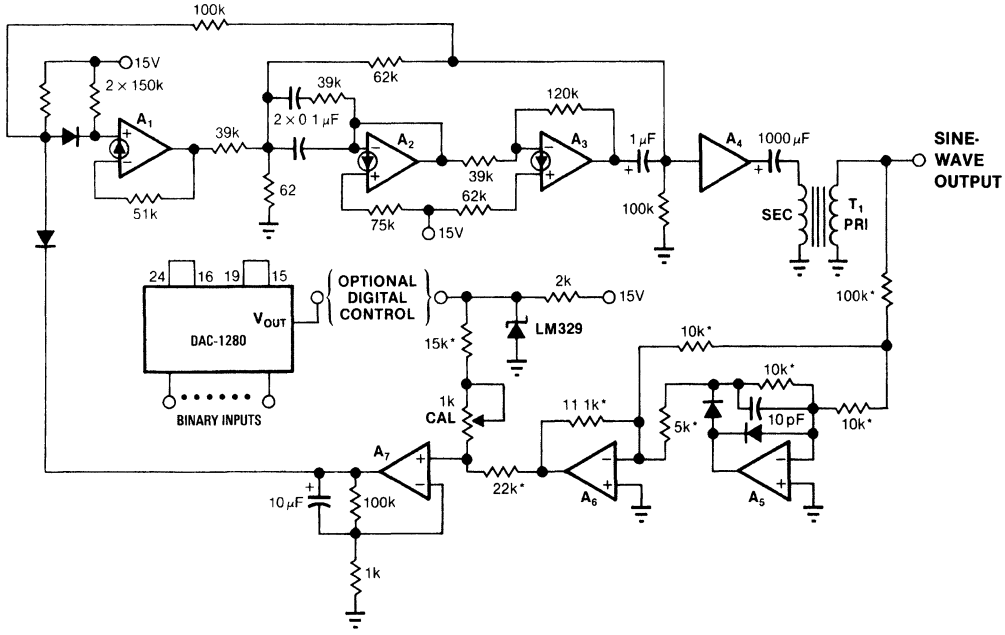
FIGURE 2. A basic Wein bridge design (a) employs a lamp's positive temperature coefficient to achieve amplitude stability. A more complex version (b) provides the same feature with the additional advantage of loop time-constant control.

High Voltage AC Calibrator (Continued)



Trace	Vertical	Horizontal
Top	10V/DIV	10 ms/DIV
Middle	1V/DIV	500 ns/DIV
Bottom	0.5V/DIV	500 ns/DIV

FIGURE 3. Low-distortion output (top trace) is a Wein bridge oscillator feature. The very low crossover distortion level (middle) results from the LF155's output stage. A distortion analyzer's output signal (bottom) indicates this design's 0.01% distortion level.



A1–A3 = ¼ LM3900
A4 = LH0002
A5–A7 = ¼ LF347
T1 = UTC LS-52
All diodes = 1N914
* = low-TC, metal-film types

FIGURE 4. Generate high-voltage sine waves using IC-based circuits by driving a transformer in a step-up mode. You can realize digital amplitude control by replacing the LM329 voltage reference with the DAC1287.

Negative Resistance Oscillator

All of the preceding circuits rely on RC time constants to achieve resonance. LC combinations can also be used and offer good frequency stability, high Q and fast starting.

In *Figure 5* a negative resistance configuration is used to generate the sine wave. The Q1-Q2 pair provides a 15 µA current source. Q2's collector current sets Q3's peak collector current. The 300 kΩ resistor and the Q4-Q5 LM394 matched pair accomplish a voltage-to-current conversion that decreases Q3's base current when its collector voltage rises. This negative resistance characteristic permits oscillation. The frequency of operation is determined by the LC in the Q3-Q5 collector line. The LF353 FET amplifier provides gain and buffering. Power supply dependence is eliminated by the zener diode and the LF353 unity gain follower. This circuit starts quickly and distortion is inside 1.5%.

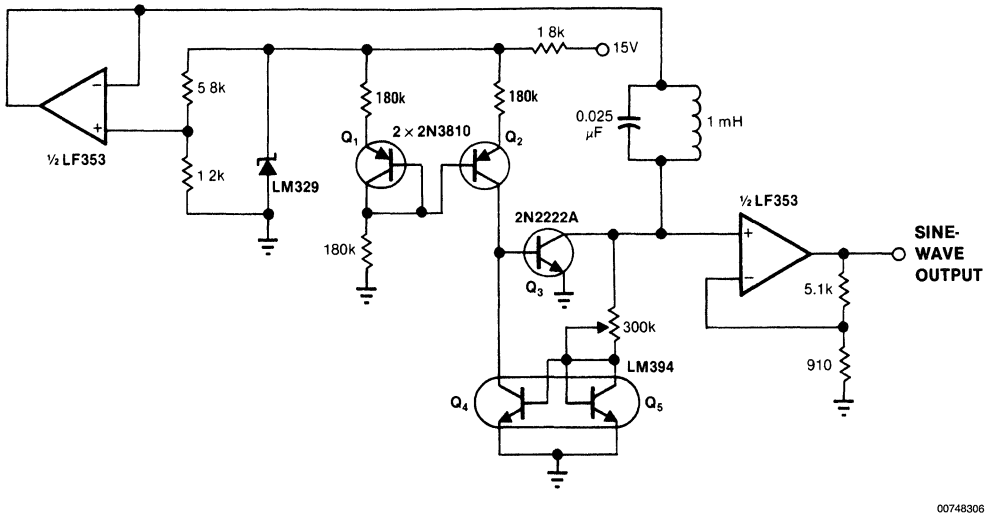


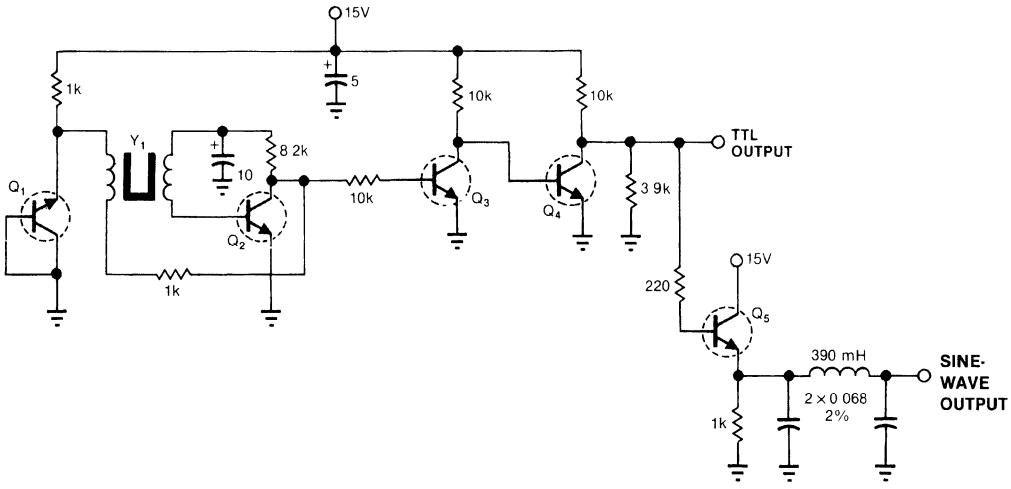
FIGURE 5. LC sine wave sources offer high stability and reasonable distortion levels. Transistors Q1 through Q5 implement a negative-resistance amplifier. The LM329, LF353 combination eliminates power-supply dependence.

Resonant Element Oscillator—Tuning Fork

All of the above oscillators rely on combinations of passive components to achieve resonance at the oscillation frequency. Some circuits utilize inherently resonant elements to achieve very high frequency stability. In *Figure 6* a tuning fork is used in a feedback loop to achieve a stable 1 kHz output. Tuning fork oscillators will generate stable low frequency sine outputs under high mechanical shock conditions which would fracture a quartz crystal.

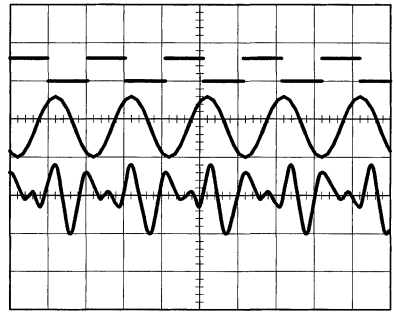
Because of their excellent frequency stability, small size and low power requirements, they have been used in airborne applications, remote instrumentation and even watches. The low frequencies achievable with tuning forks are not available from crystals. In *Figure 6*, a 1 kHz fork is used in a feedback configuration with Q2, one transistor of an LM3045 array. Q1 provides zener drive to the oscillator circuit. The need for amplitude stabilization is eliminated by allowing the oscillator to go into limit. This is a conventional technique in fork oscillator design. Q3 and Q4 provide edge speed-up and a 5V output for TTL compatibility. Emitter follower Q5 is used to drive an LC filter which provides a sine wave output. *Figure 7*, trace A shows the square wave output while trace B depicts the sine wave output. The 0.7% distortion in the sine wave output is shown in trace C, which is the output of a distortion analyzer.

Resonant Element Oscillator—Tuning Fork (Continued)



Q1–Q5 = LM3045 array
Y1 = 1 kHz tuning fork, Fork Standards Inc
All capacitors in µF

FIGURE 6. Tuning fork based oscillators don't inherently produce sinusoidal outputs. But when you do use them for this purpose, you achieve maximum stability when the oscillator stage (Q1, Q2) limits. Q3 and Q4 provide a TTL compatible signal, which Q5 then converts to a sine wave.



Trace	Vertical	Horizontal
Top	5V/DIV	
Middle	50V/DIV	500 µs/DIV
Bottom	0.2V/DIV	

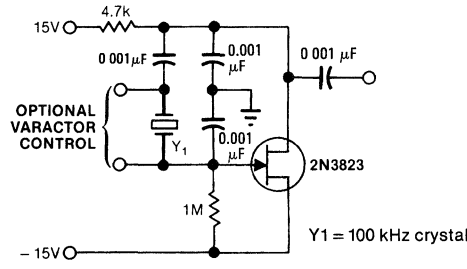
FIGURE 7. Various output levels are provided by the tuning fork oscillator shown in *Figure 6.* This design easily produces a TTL compatible signal (top trace) because the oscillator is allowed to limit. Low-pass filtering this square wave generates a sine wave (middle). The oscillator's 0.7% distortion level is indicated (bottom) by an analyzer's output.

Resonant Element Oscillator—Quartz Crystal

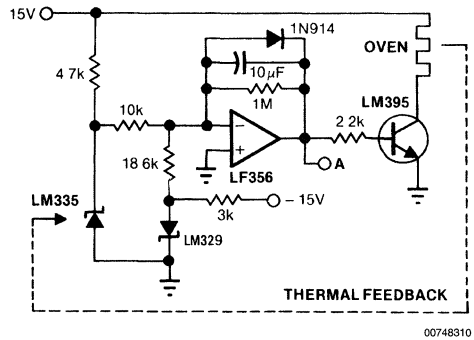
Quartz crystals allow high frequency stability in the face of changing power supply and temperature parameters. *Figure 8a* shows a simple 100 kHz crystal oscillator. This Colpitts class circuit uses a JFET for low loading of the crystal, aiding stability. Regulation will eliminate the small effects (~ 5 ppm for 20% shift) that supply variation has on this circuit. Shunting the crystal with a small amount of capacitance allows very fine trimming of frequency. Crystals typically drift less than 1 ppm/°C and temperature controlled ovens can be used to eliminate this term (*Figure 8b*). The RC feedback values will depend upon the thermal time constants of the oven used. The values shown are typical. The temperature of the oven should be set so that it coincides with the crystal's zero temperature coefficient or "turning point" temperature which is manufacturer specified. An alternative to temperature control uses a varactor diode placed across the crystal. The varactor is biased by a temperature dependent voltage from a circuit which could be very similar to *Figure 8b* without the output transistor. As ambient temperature varies the circuit changes the voltage across the varactor, which in turn changes its capacitance. This shift in capacitance trims the oscillator frequency.

Approximation Methods

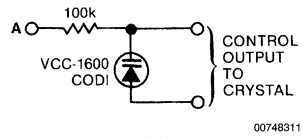
All of the preceding circuits are *inherent* sine wave generators. Their normal mode of operation supports and maintains a sinusoidal characteristic. Another class of oscillator is made up of circuits which *approximate* the sine function through a variety of techniques. This approach is usually more complex but offers increased flexibility in controlling amplitude and frequency of oscillation. The capability of this type of circuit for a digitally controlled interface has markedly increased the popularity of the approach.



(a)



(b)

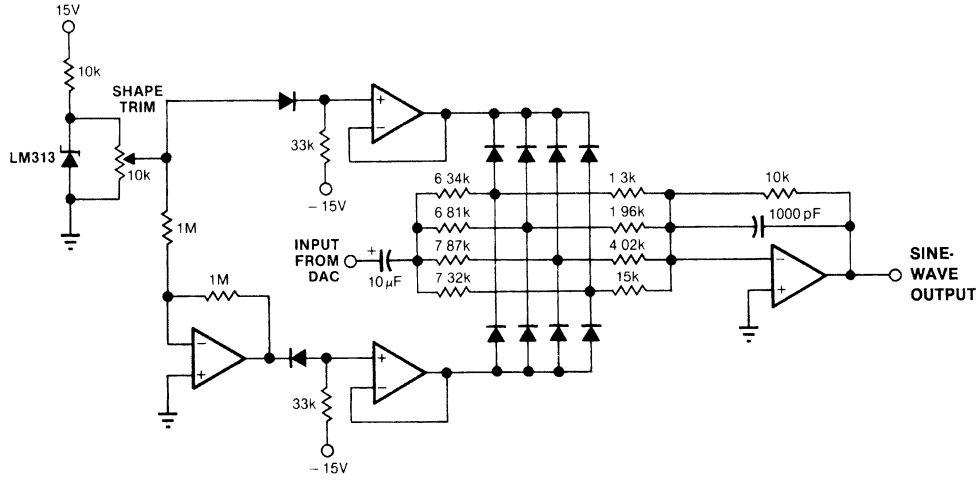


(c)

FIGURE 8. Stable quartz-crystal oscillators can operate with a single active device (a). You can achieve maximum frequency stability by mounting the oscillator in an oven and using a temperature-controlling circuit (b). A varactor network (c) can also accomplish crystal fine tuning. Here, the varactor replaces the oven and retunes the crystal by changing its load capacitances.

Sine Approximation—Breakpoint Shaper

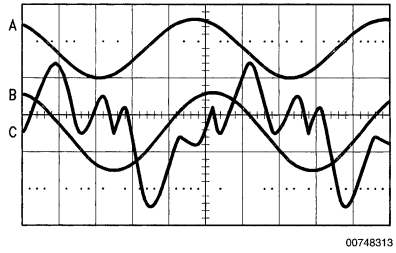
Figure 9 diagrams a circuit which will "shape" a 20 Vp-p wave input into a sine wave output. The amplifiers serve to establish stable bias potentials for the diode shaping network. The shaper operates by having individual diodes turn on or off depending upon the amplitude of the input triangle. This changes the gain of the output amplifier and gives the circuit its characteristic non-linear, shaped output response. The values of the resistors associated with the diodes determine the shaped waveform's appearance. Individual diodes in the DC bias circuitry provide first order temperature compensation for the shaper diodes. *Figure 10* shows the circuit's performance. Trace A is the filtered output (note 1000 pF capacitor across the output amplifier). Trace B shows the waveform with no filtering (1000 pF capacitor removed) and trace C is the output of a distortion analyzer. In trace B the breakpoint action is just detectable at the top and bottom of the waveform, but all the breakpoints are clearly identifiable in the distortion analyzer output of trace C. In this circuit, if the amplitude or symmetry of the input triangle wave shifts, the output waveform will degrade badly. Typically, a D/A converter will be used to provide input drive. Distortion in this circuit is less than 1.5% for a filtered output. If no filter is used, this figure rises to about 2.7%.



All diodes = 1N4148

All op amps = ¼ LF347

FIGURE 9. Breakpoint shaping networks employ diodes that conduct in direct proportion to an input triangle wave's amplitude. This action changes the output amplifier's gain to produce the sine function.

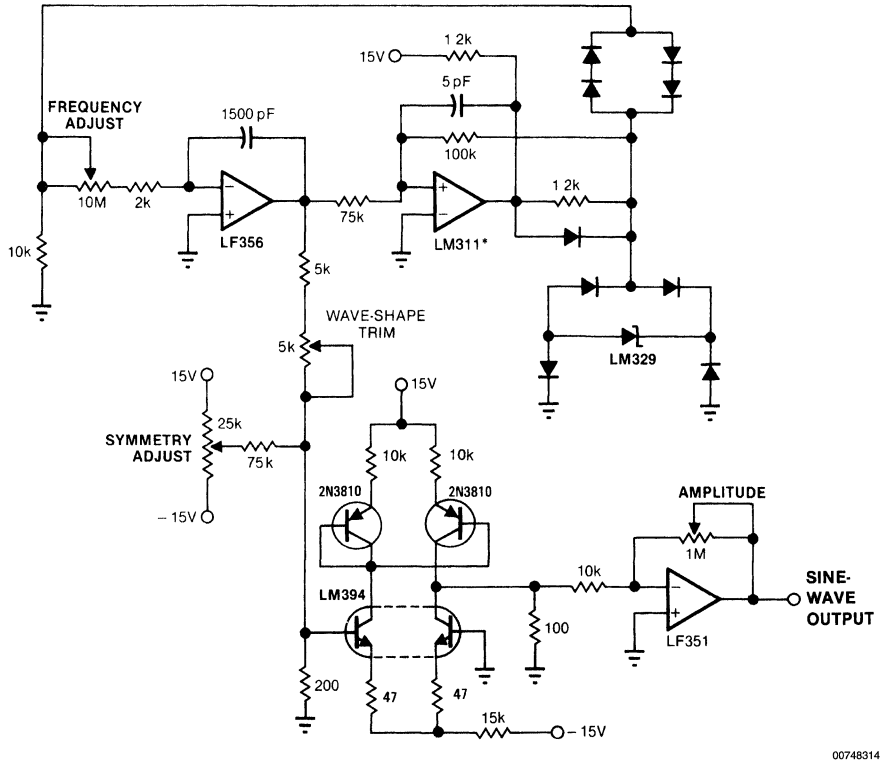


Trace	Vertical	Horizontal
A	5V/DIV	
B	5V/DIV	20 μs/DIV
C	0.5V/DIV	

FIGURE 10. A clean sine wave results (trace A) when *Figure 9* circuit's output includes a 1000 pF capacitor. When the capacitor isn't used, the diode network's breakpoint action becomes apparent (trace B). The distortion analyzer's output (trace C) clearly shows all the breakpoints.

Sine Approximation—Logarithmic Shaping

Figure 11 shows a complete sine wave oscillator which may be tuned from 1 Hz to 10 kHz with a single variable resistor. Amplitude stability is inside 0.02%/°C and distortion is 0.35%. In addition, desired frequency shifts occur instantaneously because no control loop time constants are employed. The circuit works by placing an integrator inside the positive feedback loop of a comparator. The LM311 drives symmetrical, temperature-compensated clamp arrangement. The output of the clamp biases the LF356 integrator. The LF356 integrates this current into a linear ramp at its output. This ramp is summed with the clamp output at the LM311 input. When the ramp voltage nulls out the bound voltage, the comparator changes state and the integrator output reverses. The resultant, repetitive triangle waveform is applied to the sine shaper configuration. The sine shaper utilizes the non-linear, logarithmic relationship between V_{be} and collector current in transistors to smooth the triangle wave. The LM394 dual transistor is used to generate the actual shaping while the 2N3810 provides current drive. The LF351 allows adjustable, low impedance, output amplitude control. Waveforms of operation are shown in *Figure 14*.



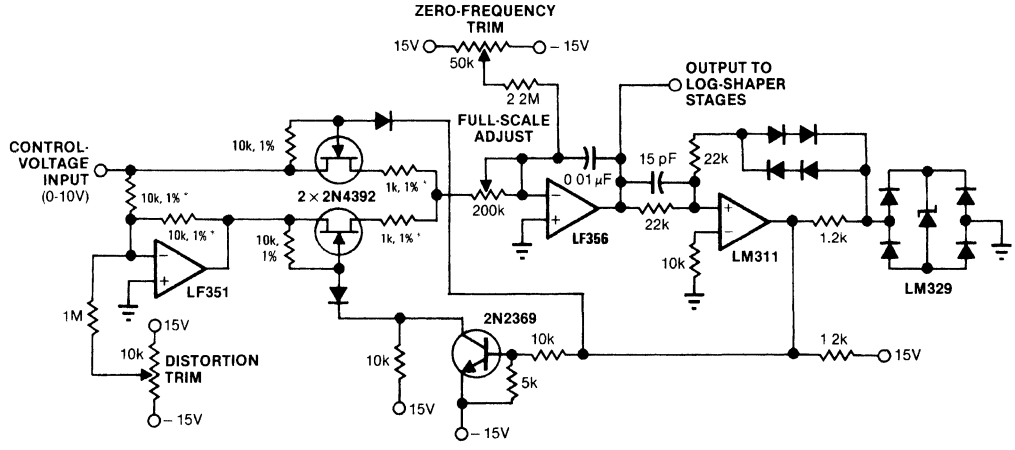
All diodes = 1N4148
Adjust symmetry and wave-shape controls for minimum distortion
* LM311 Ground Pin (Pin 1) at −15V

FIGURE 11. Logarithmic shaping schemes produce a sine wave oscillator that you can tune from 1 Hz to 10 kHz with a single control. Additionally, you can shift frequencies rapidly because the circuit contains no control-loop time constants.

Sine Approximation—Voltage Controlled Sine Oscillator

Figure 12 details a modified but extremely powerful version of *Figure 11*. Here, the input voltage to the LF356 integrator is furnished from a control voltage input instead of the zener diode bridge. The control input is inverted by the LF351. The two complementary voltages are each gated by the 2N4393 FET switches, which are controlled by the LM311 output. The frequency of oscillation will now vary in direct proportion to the control input. In addition, because the amplitude of this circuit is controlled by limiting, rather than a servo loop, response to a control step or ramp input is almost instantaneous. For a 0V–10V input the output will run over 1 Hz to 30 kHz with less than 0.4% distortion. In addition, linearity of control voltage vs output frequency will be within 0.25%. *Figure 13* shows the response of this circuit (waveform B) to a 10V ramp (waveform A).

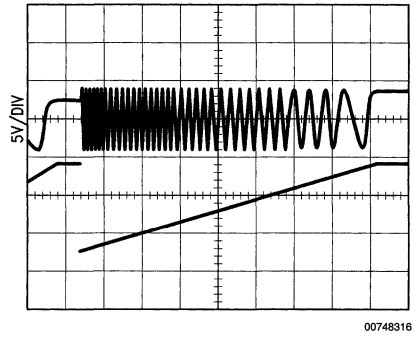
Sine Approximation—Voltage Controlled Sine Oscillator (Continued)



00748315

Adjust distortion for
minimum at 1 Hz to 10 Hz
Adjust full-scale for 30 kHz
at 10V input
All diodes = 1N4148
* Match to 0 1%

FIGURE 12. A voltage-tunable oscillator results when *Figure 11's* design is modified to include signal-level-controlled feedback. Here, FETs switch the integrator's input so that the resulting summing-junction current is a function of the input control voltage. This scheme realizes a frequency range of 1 Hz to 30 kHz for a 0V to 10V input.



00748316

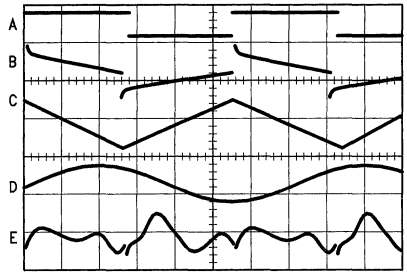
FIGURE 13. Rapid frequency sweeping is an inherent feature of *Figure 12's* voltage-controlled sine wave oscillator. You can sweep this VCO from 1 Hz to 30 kHz with a 10V input signal; the output settles quickly.

Sine Approximation—Digital Methods

Digital methods may be used to approximate sine wave operation and offer the greatest flexibility at some increase in complexity. *Figure 15* shows a 10-bit IC D/A converter driven from up/down counters to produce an amplitude-stable triangle current into the LF357 FET amplifier. The LF357 is used to drive a shaper circuit of the type shown in *Figure 11*. The output amplitude of the sine wave is stable and the frequency is solely dependent on the clock used to drive the counters. If the clock is crystal controlled, the output sine wave will reflect the high frequency stability of the crystal. In this example, 10 binary bits are used to drive the DAC so the output frequency will be 1/1024 of the clock frequency. If a sine coded read-only-memory is placed between the counter

Sine Approximation—Digital Methods (Continued)

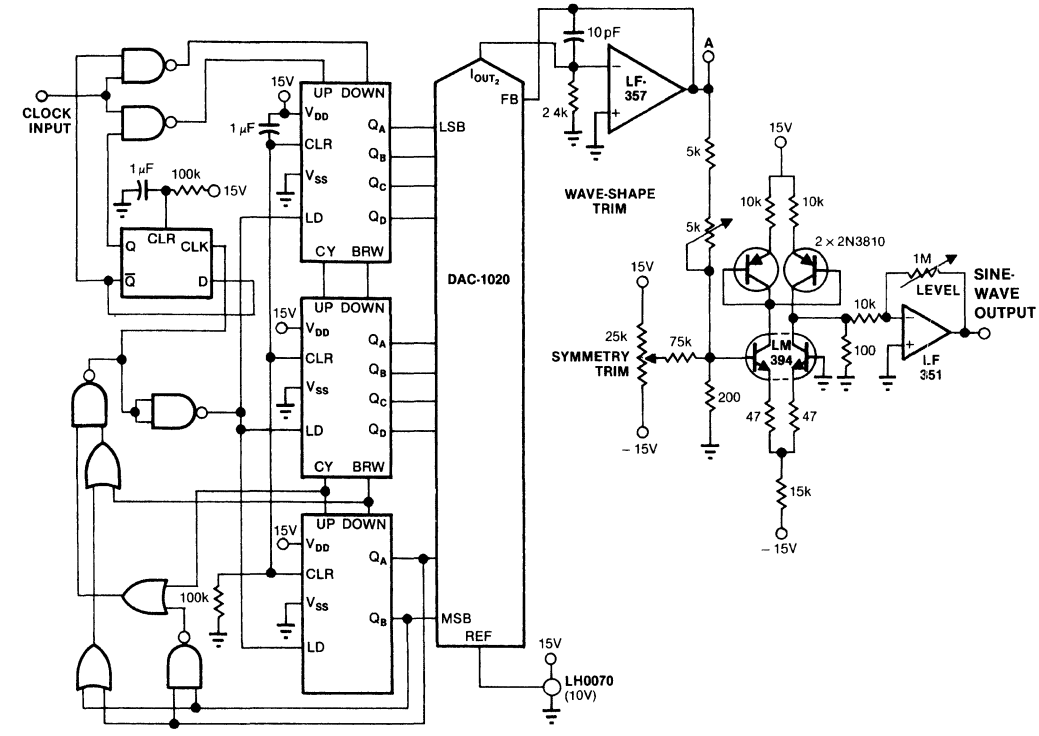
outputs and the DAC, the sine shaper may be eliminated and the sine wave output taken directly from the LF357. This constitutes an extremely powerful digital technique for generating sine waves. The amplitude may be voltage controlled by driving the reference terminal of the DAC. The frequency is again established by the clock speed used and both may be varied at high rates of speed without introducing significant lag or distortion. Distortion is low and is related to the number of bits of resolution used. At the 8-bit level only 0.5% distortion is seen (waveforms, *Figure 16*; graph, *Figure 17*) and filtering will drop this below 0.1%. In the photo of *Figure 16* the ROM directed steps are clearly visible in the sine waveform and the DAC levels and glitching show up in the distortion analyzer output. Filtering at the output amplifier does an effective job of reducing distortion by taking out these high frequency components.



Trace	Vertical	Horizontal
A	20V/DIV	
B	20V/DIV	20 µs/DIV
C	10V/DIV	
D	10V/DIV	
E	0.5V/DIV	

FIGURE 14. Logarithmic shapers can utilize a variety of circuit waveforms. The input to the LF356 integrator (*Figure 11*) appears here as trace A. The LM311's input (trace B) is the summed result of the integrator's triangle output (C) and the LM329's clamped waveform. After passing through the 2N3810/LM394 shaper stage, the resulting sine wave is amplified by the LF351 (D). A distortion analyzer's output (E) represents a 0.35% total harmonic distortion.

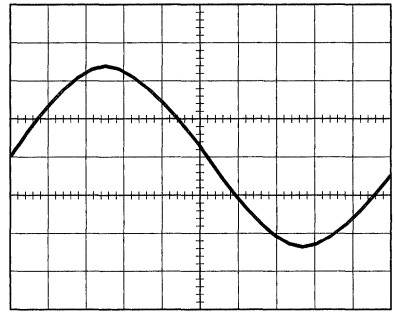
Sine Approximation—Digital Methods (Continued)



MM74C00 = NAND
MM74C32 = OR
MM74C74 = D flip-flop
MM74193 = counters

FIGURE 15. Digital techniques produce triangular waveforms that methods employed in *Figure 11* can then easily convert to sine waves. This digital approach divides the input clock frequency by 1024 and uses the resultant 10 bits to drive a DAC. The DAC's triangular output—amplified by the LF357—drives the log shaper stage. You could also eliminate the log shaper and place a sine-coded ROM between the counters' outputs and the DAC, then recover the sine wave at point A.

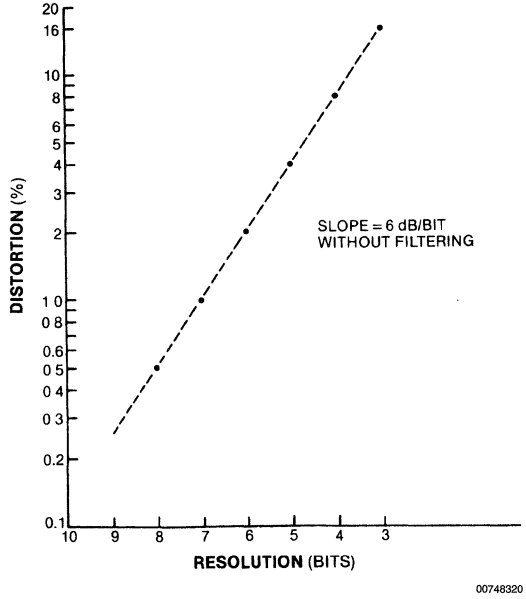
Sine Approximation—Digital Methods (Continued)



00748319

Trace	Vertical	Horizontal
Sine Wave	1V/DIV	200 µs/DIV
Analyzer	0.2V/DIV	

FIGURE 16. An 8-bit sine coded ROM version of *Figure 15's* circuit produces a distortion level less than 0.5%. Filtering the sine output—shown here with a distortion analyzer's trace—can reduce the distortion to below 0.1%.



00748320

FIGURE 17. Distortion levels decrease with increasing digital word length. Although additional filtering can considerably improve the distortion levels (to 0.1% from 0.5% for the 8-bit case), you're better off using a long digital word.

Circuit Applications of Sample-Hold Amplifiers

National Semiconductor
Application Note 266
Michael X. Maida

Most designers are familiar with the sample-hold amplifier as a *system* component which is utilized in high speed data acquisition work. In these applications, the sample-hold amplifier is used to store analog data which is then digitized by a relatively slow A/D converter. In this fashion, high speed or multiplexed analog data can be digitized without resorting to complex and expensive ultra-high speed A/D converters.

The use of sample-hold amplifiers as *circuit* oriented components is not as common as the class of application described above. This is unfortunate, because sampling techniques allow circuit functions which are sophisticated, low cost and not easily achieved with other approaches. An excellent example is furnished by the fiber optic data link intrusion alarm of *Figure 1*.

Fiber Optic Data Link Intrusion Alarm

The circuit of *Figure 1* will detect an attempt to tap a fiber optic data link. It may be used with any fiber optic communication system which transmits data in pulse coded form. The circuit works by detecting any short-term change in the loss characteristics of the fiber optic line. Long term changes due to temperature and component aging do not affect the circuit. The amplitude of the pulses at the LH0082 fiber optic receiver IC (A6) will depend upon the characteristics of the photocomponents and the losses in the optical line. Any attempt to tap the fiber optic will necessitate removal of some amount of light energy. This will cause an instantaneous drop in the pulse amplitude at A6's output. The amplitude of each of A6's output pulses is sampled by the LF398 sample-hold amplifier (A3), A1 and A2 provide a delayed sample-hold control pulse to A3, which insures that A6's output is sampled well after its output has settled. Under normal conditions, the pulse-to-pulse amplitude variations at A6's output will be negligible, and the output of A3 will be at a DC level. A4 is AC coupled and its output will be zero. During an intrusion attempt, energy will be removed from the line and A6's output will shift, causing A3 to jump to a new DC level. This shift will be AC amplified by A4 and the A5 comparator will trip, activating the latch circuitry.

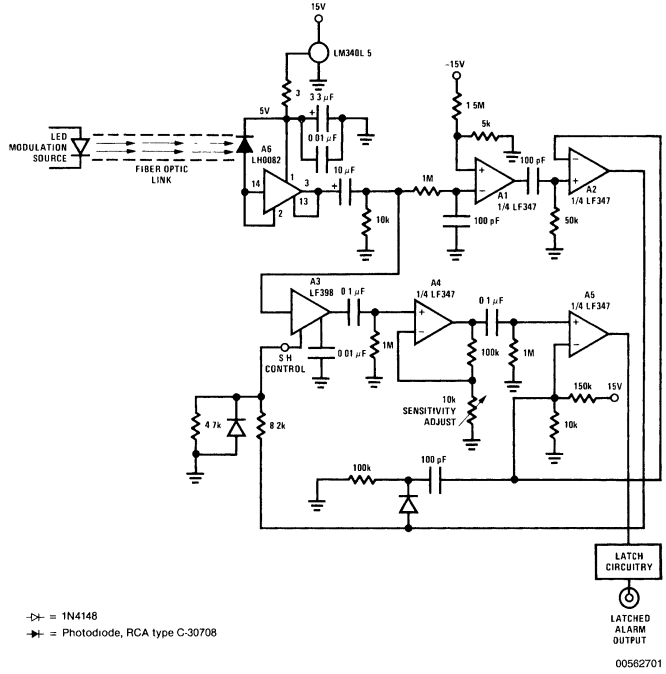
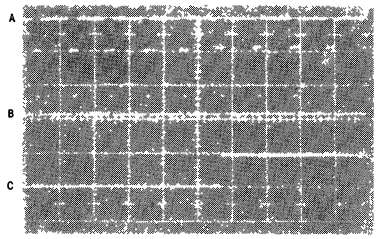


FIGURE 1. Fiber optic link eavesdropping attempts are immediately detected by this design. Working on a pulse-by-pulse comparison basis, A3 samples each input pulse and holds its output amplitude value at a DC level. Anything that disturbs the next input's amplitude causes a jump in this level; because A4 is an AC-coupled amplifier, the comparator and latch then activate.

Fiber Optic Data Link Intrusion Alarm (Continued)

Note that the circuit is not affected by slow drifts in circuit components over time and temperature because it is only sensitive to AC disturbances on the line. In addition, the frequency and pulse widths of the data may vary over wide ranges. The photo of *Figure 2* shows the circuit in operation. Trace A is A6's output. Trace B is the sample-hold control pin at A3 and Trace C is the latch-alarm output. In this figure, a disturbance on the fiber optic line has occurred just past the midpoint of the photo. This is reflected by the reduced amplitude of A6's output at this point. The latch-alarm output goes high just after the sample command rises, due to the sample-hold amplifier jumping to the new value at A6's output. In the photo, the disturbance has been made large (≅10%) for viewing purposes. In practice, the circuit will detect an energy removal as small as 0.1% from the line.



00562702

TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	1 mSEC/DIV
B	10V/DIV	1 mSEC/DIV
C	10V/DIV	1 mSEC/DIV

FIGURE 2. An intrusion attempt occurring just past the midpoint of Trace A is immediately detected by *Figure 1*'s circuit. The photodetector's amplifier output (A) shows a slight amplitude drop. The next time the S-H amplifier samples this signal (B), the alarm latch sets (C).

Proportional Pulse Stretcher

The circuit of *Figure 3* allows high accuracy measurement of short width pulse durations. The pulses may be either repetitive or single-shot events. Using digital techniques, a 1% width measurement of a 1 µs event requires a 100 MHz clock. This circuit gets around this requirement by linearly amplifying the width of the input pulse with a time multiplying factor of 1000 or more. Thus, a 1 µs input event will yield a 1 ms output pulse which is easy to measure to 1%. This measurement capability is useful in high energy physics and nuclear instrumentation work, where short pulse width signals are common.

Figure 4, Trace A shows a 350 ns input pulse applied to the circuit of *Figure 3*. The A1 comparator output goes low (*Figure 4*, Trace B), triggering the DM74121 one shot, which resets the 100 pF capacitor to 0V via Q1 with a 50 ns pulse (Trace C). Concurrently, Q2 is turned off, allowing the A3 current source to charge the 100 pF capacitor in a linear fashion (*Figure 4*, Trace C). This charging continues until the circuit input pulse ends, causing A1's output to return high and cutting off the current source. The voltage across the 100 pF capacitor at this point in time is directly proportional to the width of the circuit input pulse. This voltage is sampled by the LF398 sample-hold amplifier (A2) which receives its sample-hold command from A3 (*Figure 4*, Trace E—note horizontal scale change at this point). A3 is fed from a delay network which is driven by A1's inverting output. The output of A2 is a DC voltage, which represents the width of the most recently applied pulse to the circuit's input. This DC potential is applied to A4, which along with A5 comprises a voltage controlled pulse width modulator. A5 ramps positive (*Figure 4*, Trace G) until it is reset by a pulse from A6, which goes high for a short period (*Figure 4*, Trace F) each time A3's output (*Figure 4*, Trace E) goes low. The ramps at A6's output are compared to A2's output voltage by A4, which goes high for a period linearly dependent on A2's output value (*Figure 4*, Trace H). This pulse is the circuit's output.

In this particular circuit, the time amplification factor is about 2000 with a 1 µs full-scale width giving a 1.4 ms output pulse. Absolute accuracy of the time expansion is 1% (10 ns) referred to input with resolution down to 2 ns. The 50 ns DM74121 reset pulse limits the minimum pulse width the circuit can measure.

Proportional Pulse Stretcher (Continued)

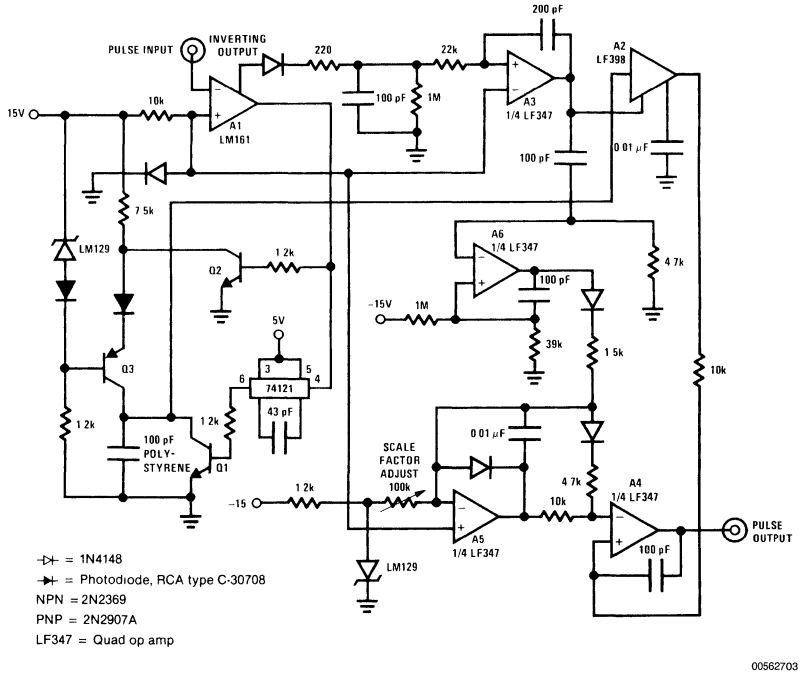
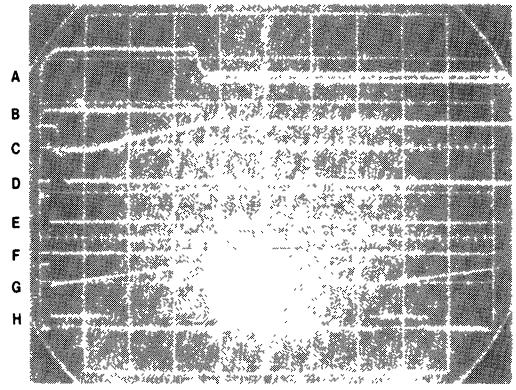


FIGURE 3. Pulse width measurement accuracy is enhanced by this pulse stretching circuit. A short input pulse triggers the 74121 one-shot and (via Q1) discharges the 100 pF capacitor while concurrently turning on the recharging current source, Q3. So long as the input pulse is present, the capacitor charges; when the pulse ends, the capacitor's voltage is proportional to the pulse's width. S-H amplifier A2 samples this voltage, and the resultant DC level controls the ON duration of the A4/A5 pulse width modulator.

Proportional Pulse Stretcher (Continued)



00562704

TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	100 nSEC/DIV
B	5V/DIV	100 nSEC/DIV
C	5V/DIV	100 nSEC/DIV
D	5V/DIV	100 nSEC/DIV

TRACE	VERTICAL	HORIZONTAL
E	50V/DIV	500 µSEC/DIV
F	50V/DIV	500 µSEC/DIV
G	20V/DIV	500 µSEC/DIV
H	100V/DIV	500 µSEC/DIV

FIGURE 4. A sequence of events in *Figure 3*'s circuit stretches a 350 ns input pulse (A) by a factor of 2000. When triggered, comparator A1 goes low (B). This action starts the recharging of a capacitor (C) after its previously stored charge has been dumped (D). When the input pulse ends, the capacitor's voltage is sampled under control of a delayed pulse (E) derived from the input amplifier's inverting output (F). The sampled and held voltage then turns off a voltage controlled pulse width modulator (G), and a stretched output pulse results (H).

Controlled Amplitude Pulser

Figure 5 depicts a circuit which converts an input pulse train into an amplitude stabilized pulse output which will drive a 20Ω load. The output pulse amplitude is adjustable from 0V to 10V and is stable over time, temperature and load changes. This circuit function is useful in automatic test equipment and general laboratory applications.

The circuit works by storing the sampled amplitude of the output pulse as a DC level, and supplying this information to a feedback loop which controls the voltage applied to the output switch. Each time a pulse is applied at the circuit input, the Q2-Q3 combination turns on and drives the load.

Simultaneously, the A1 sample-hold amplifier is placed in the sample mode. When the pulse ends, A1's output is at a DC level equal to the amplitude of the output pulse. This level is compared to the amplitude set DC reference by A2, whose output drives Q1. Q1's emitter provides the DC supply level to the Q2-Q3 switch. This servo action forces the amplitude of the output pulse to be the same as the DC potential at the amplitude set potentiometer wiper, regardless of Q3 switch losses or loading. In *Figure 6*, Trace A is the circuit output. Traces B and C detail the rising and falling edges of the output (note horizontal sweep time change for B and C) with clean 50 ns transitions into the 20Ω load.

Controlled Amplitude Pulser (Continued)

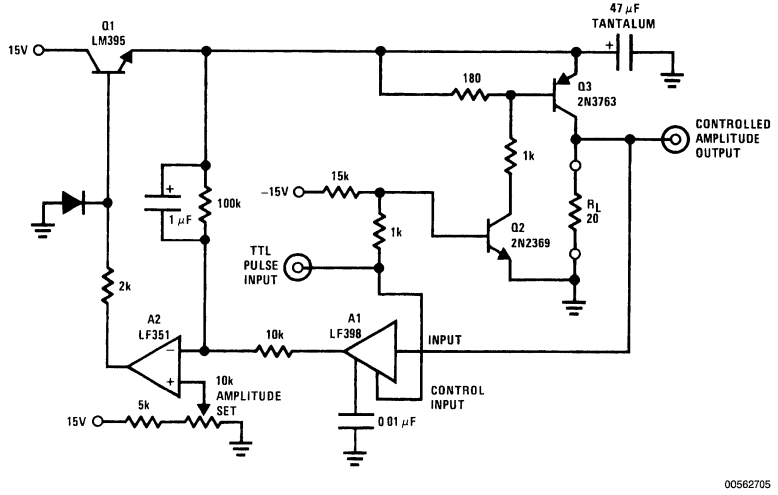
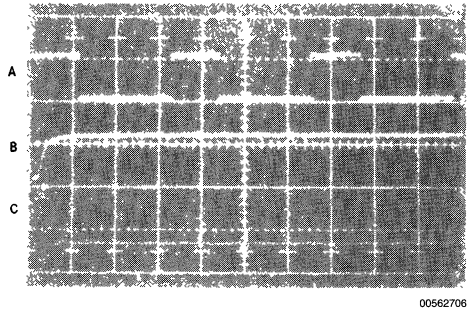


FIGURE 5. Pulse amplitude control results when this circuit samples an output pulse's amplitude and compares it with a preset reference level. When the output exceeds this reference, A2 readjusts switching transistor Q3's supply voltage to the correct level.



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	1 mSEC/DIV
B	10V/DIV	100 nSEC/DIV
C	10V/DIV	100 nSEC/DIV

FIGURE 6. A 10V, 0.5A pulse (A) is amplitude stabilized by the S-H technique depicted in *Figure 5*. Note the clean 50 ns rise (B) and fall (C) times.

Isolated Input Signal Conditioning Amplifier

Figure 7 is a logical and very powerful extension of the controlled amplitude pulser shown in *Figure 5*. This circuit permits measurement of a small amplitude signal, e.g., thermocouples, in the presence of common-mode noise or voltages as high as 500V. This is a common requirement in industrial control systems. Despite the fact that the input terminals are fully galvanically isolated from the output, a transfer accuracy of 0.1% may be expected. With the optional low-level pre-amplifier shown, inputs as low as 10 mV full-scale may be measured.

The circuit works by converting the input signal into a pulse train whose amplitude is linearly dependent on the input signal value. This pulse train drives a transformer which provides total galvanic isolation of the input circuitry from ground. The transformer output is then demodulated back to a DC level to provide the circuit's system ground referenced

Isolated Input Signal Conditioning Amplifier (Continued)

output. The amplitude of the pulse train which drives the transformer is controlled by a loop very similar to the one described in *Figure 5*. The amplitude set potentiometer has been deleted, and the servo amplifier's "+" input becomes the circuit input. A1, a low drift *X1000* amplifier, may be employed for boosting low-level inputs. The pulse train is supplied by A2, which is set up as an oscillator (A2 output shown in *Figure 8*, Trace A). The feedback to the pulse amplitude stabilizing loop is taken from an isolated secondary of the transformer, which insures high accuracy amplitude information transfer. The amplitude coded information at the transformer's secondary (*Figure 8*, Trace B) is demodulated back to a DC level by sample-hold amplifier, A7. A5 (output, *Figure 8*, Trace C) and A6 ("+" input, *Figure 8*, Trace D; output, *Figure 8*, Trace E) provide a delayed sample command to A7, ensuring accurate acquisition of the transformer's output pulse amplitude. A8 provides gain trimming and filtering capability.

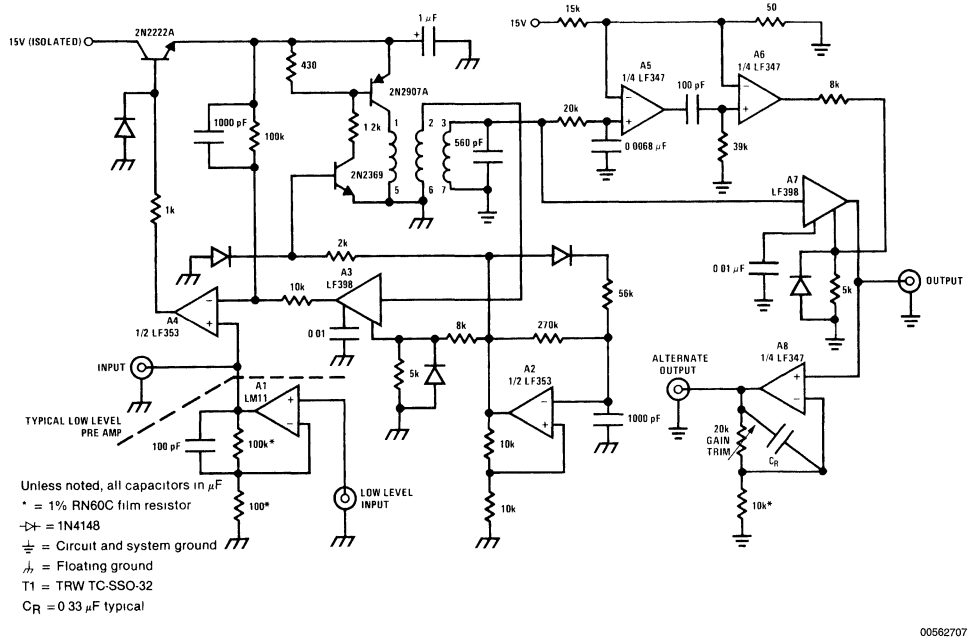
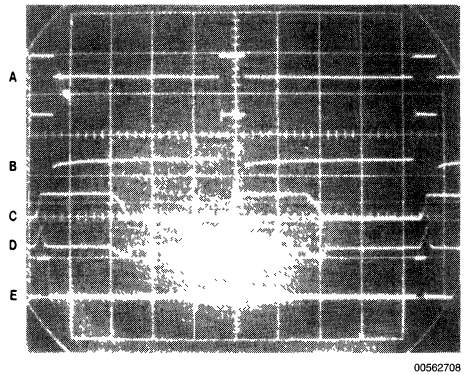


FIGURE 7. Obtain input signal isolation using this circuit's dual S-H scheme. Analog input signals amplitude modulate a pulse train using a technique similar to that employed in *Figure 5*'s design. This modulated data is transformer coupled, and thereby isolated, to a DC filter stage, where it is resampled and reconstructed.

Isolated Input Signal Conditioning Amplifier (Continued)



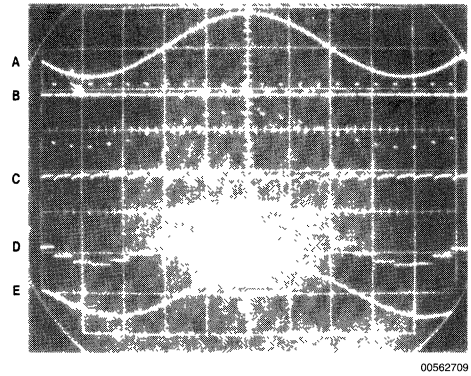
TRACE	VERTICAL	HORIZONTAL
A	50V/DIV	100 µSEC/DIV
B	1V/DIV	100 µSEC/DIV
C	50V/DIV	100 µSEC/DIV
D	10V/DIV	100 µSEC/DIV
E	5V/DIV	100 µSEC/DIV

FIGURE 8. *Figure 7*'s in-circuit oscillator (A2) generates both the sampling pulse (A) and the switching transistor's drive. Modulated by the analog input signal, Q2's (and therefore T1's) output (B) is demodulated by S-H amplifier A7. A5's output (C) and A6's input (D) and output (E) provide a delayed sample command.

Figure 9 provides very graphic evidence of the circuit at work. Here, a DC biased sine wave (*Figure 9*, Trace A) is fed into the circuit input. Trace B is the clock from A2's output. Trace C is the transformer secondary (input of A7 sample-hold amplifier) and Trace D is A7's output. Trace E shows the filter's output at A8.

Precision, High Efficiency Temperature Controller

The sample-hold amplifier in *Figure 10* is used to provide very high stability in an oven temperature control circuit. In this circuit, the output signal of the pulse driven thermistor-bridge is ten times greater than the usual DC driven bridge. In thermistor-bridges, power dissipation in the resistors and thermistor is the limiting factor in how much DC bridge drive may be used. However, if the bridge drive is applied in the form of high voltage pulses at very low duty cycle, average power dissipation will be low and a high bridge output signal will result.



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	100 mSEC/DIV
B	100V/DIV	
C	5V/DIV	
D	5V/DIV	
E	5V/DIV	

FIGURE 9. Completely input-to-output isolated, *Figure 7*'s circuit's analog input signal (A) is sampled by a clock pulse (B) and converted to a pulse amplitude modulated format (C). After filtering and resampling, the reconstructed signal (D) is available smoothed (E).

Precision, High Efficiency Temperature Controller (Continued)

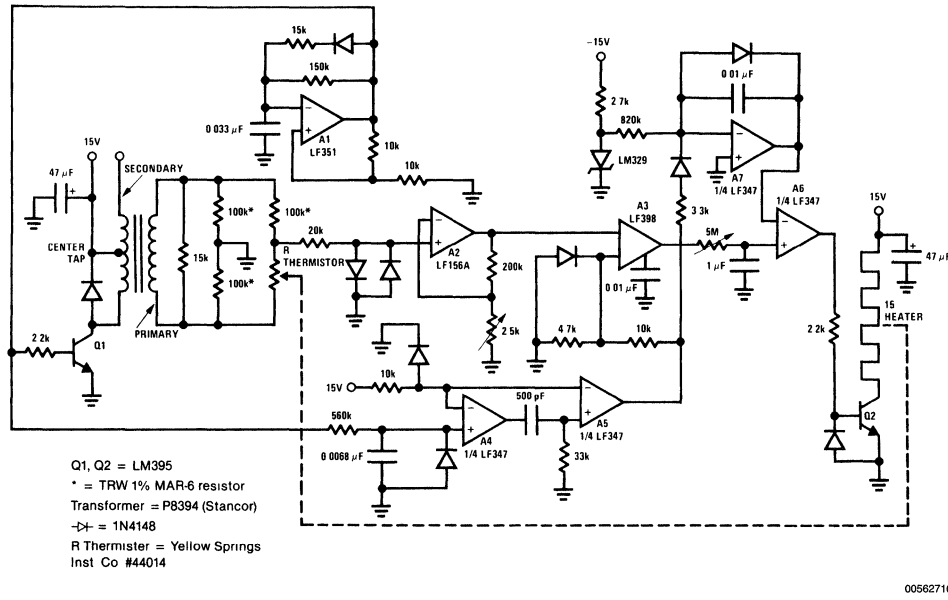


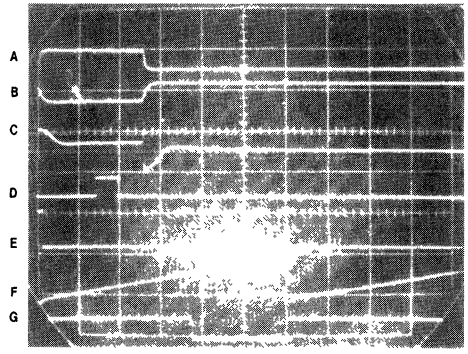
FIGURE 10. Tight temperature control results when high voltage pulses synchronously drive a thermistor-bridge—a trick that increases signal level—and are then sampled and used to control a pulse width modulated heater driver.

In *Figure 10*, this operation is implemented by having the A1 oscillator drive Q1 to energize a common 24V transformer used "backwards". The transformer's floated output is a 100V pulse which is applied directly across the thermistor-bridge. With one side of the bridge output grounded, the bridge drive with respect to ground appears as complementary 50V pulses (*Figure 11*, Traces A and B). A2 provides amplification of the bridge's pulsed output (*Figure 11*, Trace C). A3, a sample-hold amplifier, samples the middle of A2's output pulses and has a DC output equal to the amplitude of these pulses. Proper timing for A3's sample command (*Figure 11*, Trace D) is provided by the A4-A5 pair and their associated RC networks. The DC output of A3 is low-pass filtered and fed to A6, which combines with A7 to form a simple pulse width modulator. The output of A7 is a ramp (*Figure 11*, Trace F—note horizontal scale change) which is periodically reset by A5's output (*Figure 11*, Trace E). This ramp is compared at A6 to A3's output, and the resultant pulse at A6's output (*Figure 11*, Trace G) is used to drive the Q2 heater control switch. In this fashion, the ON time of the pulse applied to the heater will be proportional to the sensed offset at the thermistor-bridge. Thermal feedback from the heater to the thermistor completes a loop around the circuit. The 5 MΩ potentiometer is used to adjust the time constant of this loop, and the 2.5k potentiometer at A2 sets the gain.

In operation, with the thermistor and heater tightly coupled, the time constant of the loop is adjusted by applying small step changes in the temperature setpoint. This is done by alternately opening and closing a switch across a 100Ω resistor in series with one of the bridge resistors. For the thermistor shown, this represents a 0.02°C step. The response of the loop to these steps can be monitored at A3's output. With the loop time constant and gain properly adjusted, A3's output will settle in a minimum amount of time in

Precision, High Efficiency Temperature Controller (Continued)

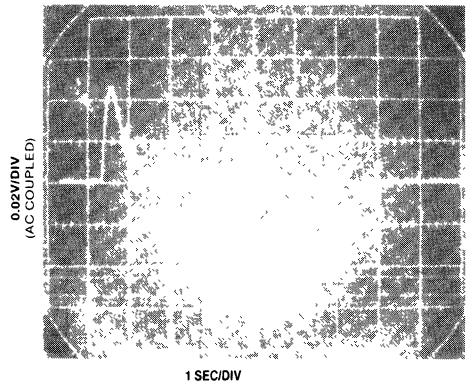
response to the steps. *Figure 12* shows settling for both "+" and "–" steps, with settling inside 2 seconds for either polarity step.



00562711

TRACE	VERTICAL	HORIZONTAL
A	100V/DIV	200 µSEC/DIV
B	100V/DIV	200 µSEC/DIV
C	5V/DIV	200 µSEC/DIV
D	10V/DIV	200 µSEC/DIV
E	5V/DIV	1 mSEC/DIV
F	10V/DIV	1 mSEC/DIV
G	50V/DIV	1 mSEC/DIV

FIGURE 11. Driving a thermistor-bridge with complementary high voltage pulses (A and B) permits high gain amplification without drift problems (C). Driven by a delayed sample command (D), a S-H amplifier converts the bridge's error signal to a DC level (E) that controls a pulse width modulated heater driver (F and G).



00562712

FIGURE 12. Tight heater to thermistor coupling and careful calibration can provide rapid temperature restabilization. Here the controlled oven recovers within 2 seconds after ±0.002°C steps.

Once adjusted, and driving a well insulated and designed oven, the circuit's control stability can be monitored. The high output signal levels from the bridge, in combination with the gain provided by A2, yield extremely good performance.

Sample-Hold Amplifier Terms

Acquisition Time: The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Aperture Time: The delay required between hold command and an input analog transition, so that the transition does not affect the held output.

Dynamic Sampling Error: The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Gain Error: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Hold Settling Time: The time required for the output to settle within 1 mV of final value after the hold logic command.

Hold Step: The voltage step at the output of the sample-hold when switching from sample mode to hold mode with a steady (DC) analog input voltage. Logic swing is specified, usually 5V.

Sample-Hold Amplifier Terms (Continued)

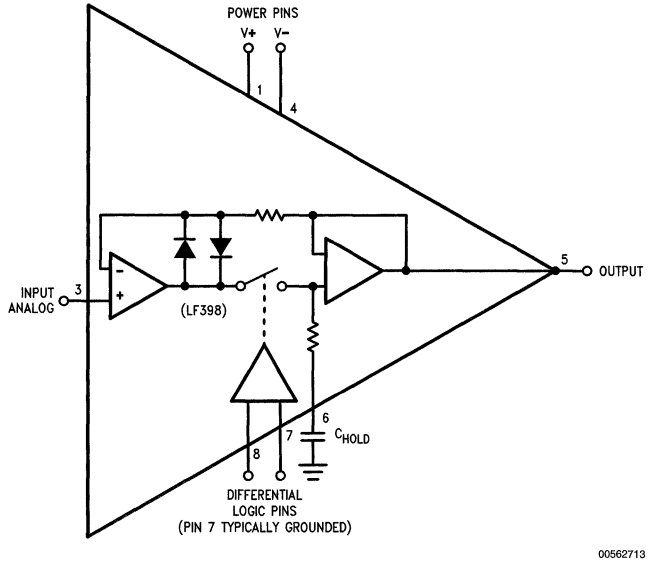


FIGURE 13. Typical Sample-Hold IC Amplifier

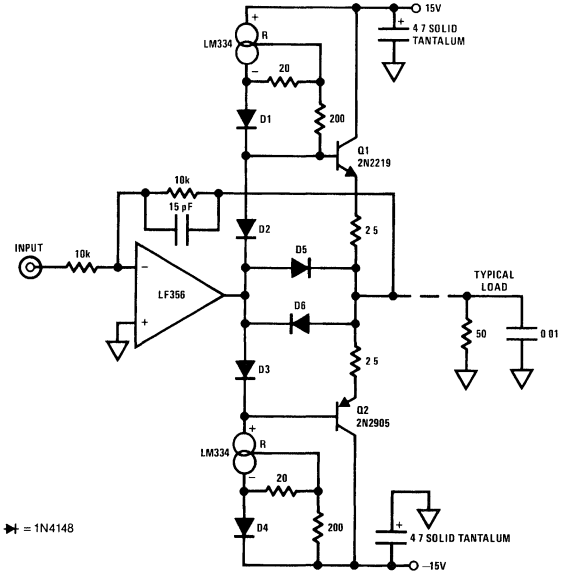
Op Amp Booster Designs

National Semiconductor
Application Note 272
Michael X. Maida

Although modern integrated circuit operational amplifiers ease linear circuit design, IC processing limits amplifier output power. Many applications, however, require substantially greater output voltage swing or current (or both) than IC amplifiers can deliver. In these situations an output "booster," or post amplifier, is required to achieve the needed voltage or current gain. Normally, this stage is placed within the feedback loop of the operational amplifier so that the low drift and stable gain characteristics of the amplifier are retained. Because the booster is a gain stage with its own inherent AC characteristics, the issues of phase shift, oscillation, and frequency response cannot be ignored if the booster and amplifier are to work well together. The design of booster stages which achieve power gain while maintaining good dynamic performance is a difficult challenge. The circuitry for boosters will change with the application's requirements, which can be very diverse. A typical current gain stage is shown in *Figure 1*.

200 mA Current Booster

The circuit of *Figure 1* boosts the LF356 unity gain inverter amplifier's output current to a ±200 mA level while maintaining a full ±12V output swing. The LM334 current sources are used to bias complementary emitter-followers. The 200Ω resistors and D1-D4 diodes associated with the LM334s provide temperature compensation for the current sources, while the 20Ω resistor sets the current value at 3.5 mA. Q1 provides drive for positive LF356 output swings, while Q2 sinks current for negative amplifier outputs. Crossover distortion is avoided by the D2-D3 diodes which compensate the V_{BE}s of Q1 and Q2. For best results, D2 and D3 would be thermally coupled to the TO-5 type heat sinks used for Q1 and Q2. Amplifier feedback is taken from the booster output and returned to the LF356 summing junction. D5 and D6 achieve short circuit protection for the output by shunting drive from Q1 or Q2 when output current exceeds about 275 mA. This value is derived from the output 2.5Ω resistors value divided by the 0.7V drop across the diodes. The 15 pF-10k feedback values provide a roll-off above 2 MHz. *Figure 2* shows the circuit at work driving a 100 kHz 20 Vp-p sine wave into a 50Ω load paralleled by 10,000 pF. Trace A is the input, while Trace B is the output. Despite the heavy load, response is clean below and quick with overall circuit distortion 0.05% (Trace C).

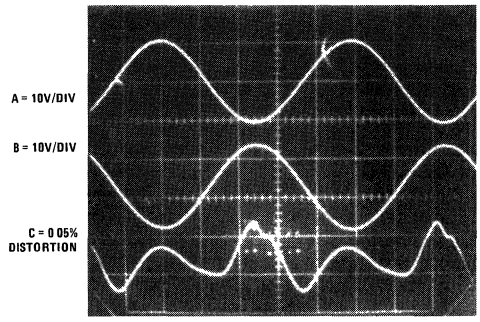


Use TO-5 heat sinks on transistors

All capacitor values in µF unless otherwise noted

FIGURE 1.

200 mA Current Booster (Continued)

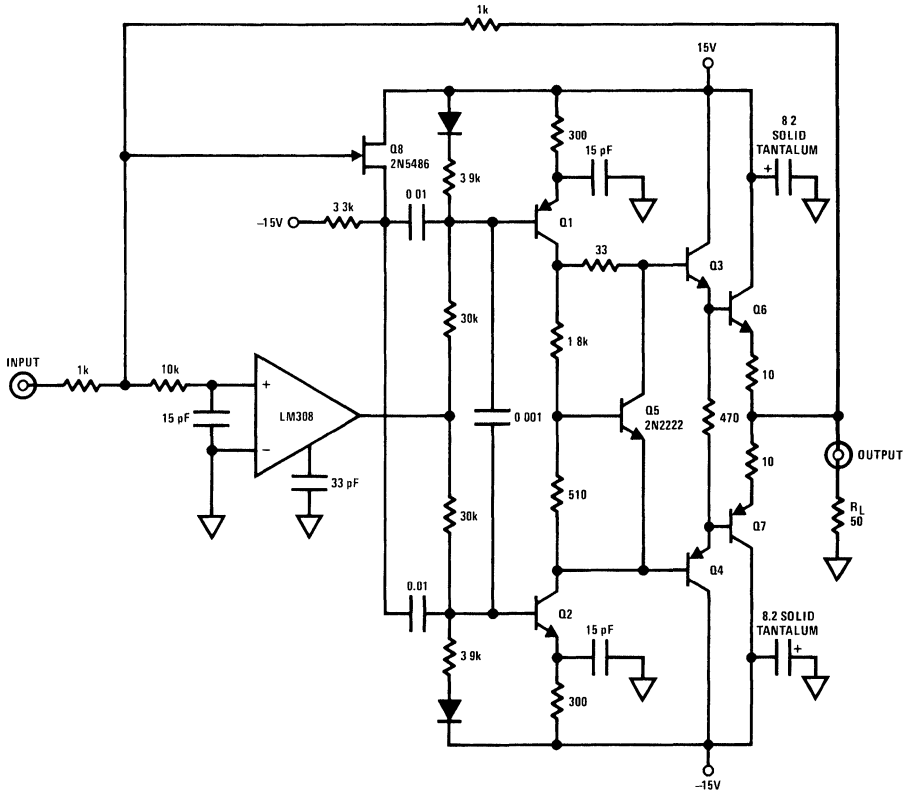


00563002

FIGURE 2.

Ultra High Speed Fed-Forward Current Booster

The schematic of *Figure 3* features the same output specifications as the previous current booster, but provides much greater speed. The speed of the booster in *Figure 1* is limited by the response of the op amp which drives it. Because that booster resides in the op amp's feedback loop, it cannot go any faster than the op amp, even though it has inherently greater bandwidth. In *Figure 3* we employ a feed-forward network which allows AC signals to bypass the LM308 op amp and directly drive a very high bandwidth current boost stage. At DC and low frequencies the LM308 provides the signal path to the booster. In this fashion, a very high speed, high current output is achieved without sacrificing the DC stability of the op amp. The output stage is made up of the Q1 and Q2 current sources which bias complementary emitter-followers, Q3-Q6 and Q4-Q7. Because the stage inverts, feedback is returned to the non-inverting input of the LM308. The actual summing junction for the circuit is the meeting point of the 1k resistors and the 10k unit at the LM308. The 10k-15 pF combination prevents the LM308 from seeing high frequency inputs. Instead, these inputs are source-followed by the Q8 FET and fed directly to the output stage via the two 0.01 µF capacitors. The LM308, therefore, is used to maintain loop stability only at DC and low frequencies. Although this arrangement is substantially more complex than *Figure 1*, the result is a breathtaking increase in speed. This boosted amplifier features a slew rate of 750V per microsecond, a full power bandwidth over 6 MHz and a 3 dB point beyond 11 MHz while retaining a ±12V, 200 mA output. *Figure 4* shows the amplifier-booster at work. Trace A is the input, while Trace B is the output. The booster drives a 10V pulse into 50Ω, with rise and fall times inside 15 ns and clean settling characteristics.



PNP=2N2905
NPN=2N2219 unless noted
TO-5 heat sinks for Q6-Q7

FIGURE 3.

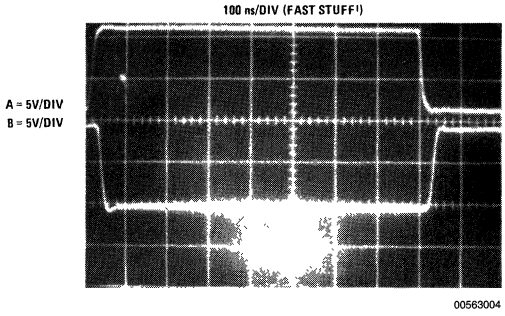


FIGURE 4.

Voltage-Current Booster

In many applications it is desirable to obtain voltage gain from a booster stage. Most monolithic amplifiers will only swing ±12V, although some types, such as the LM143, can swing ±35V. The circuit of *Figure 5* shows a simple way to effectively double the voltage swing across a load by stacking or "bridging" amplifier outputs. In the circuit shown, LF0002 current amplifiers are included in each LF412 output to provide current drive capability. Because one amplifier inverts and the other does not, the load sees 24V across it for ±12V swings from each amplifier. With the LH0002 current buffers, 24V can be placed across a 250Ω load. Although this circuit is simple and no high voltage supplies are needed, it requires that the load float with respect to ground.

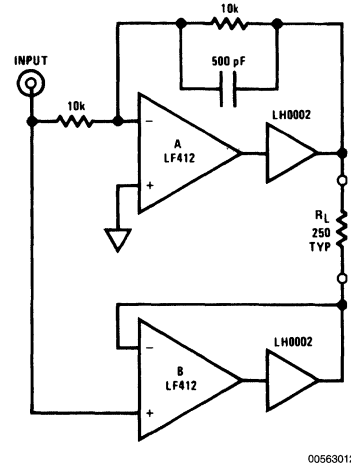
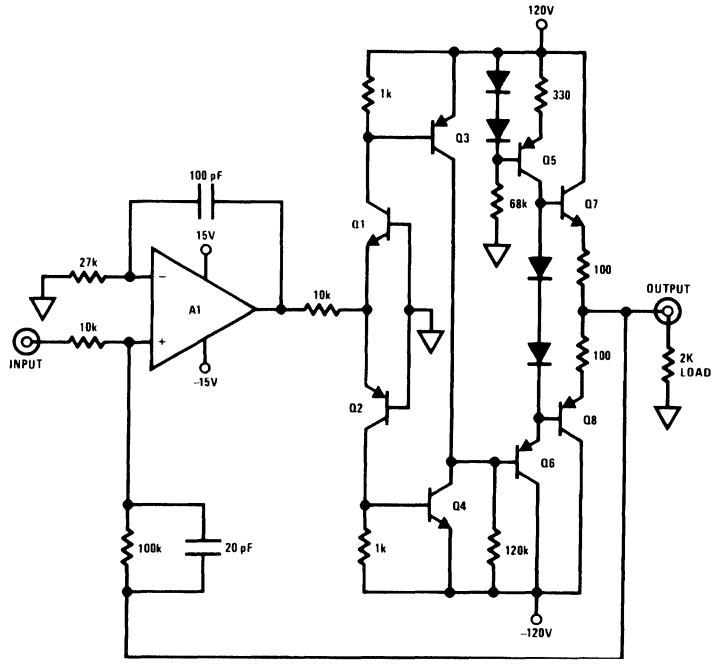


FIGURE 5.

±120V Swing Booster

In *Figure 7* the load does not have to float from ground to be driven at high voltage. This booster will drive a 2000Ω load to ±100V with good speed. In this circuit, voltage gain is obtained from the complementary common base stage, Q1-Q2. Q3 and Q4 provide additional gain to the Q7-Q8 complementary emitter-follower output stage. Q5 and Q6 provide bias, and crossover distortion is minimized by the diodes in Q5's collector line. For ±10V input signals, A1 must operate at a minimum gain of 10 to achieve a ±100V swing at the output. In this case, 10k-100k feedback values are used for a gain of ten, and the 20 pF capacitor provides loop roll-off. Because the booster contains an inverting stage (Q3-Q4), overall feedback is returned to A1's positive input. Local AC feedback at A1's negative input provides circuit dynamic stability. With its ±50 mA output, this booster yields currents as well as voltage gain. In many applications, such as CRT deflection plate driving, this current capability is not required. If this is the case, Q5 through Q8 and their associated components can be eliminated and the output and feedback taken directly from the Q3-Q4 collector line. Under these conditions, resistive output loading should not exceed 1 MΩ or significant crossover distortion will appear. Since deflection plates are a pure capacitive load, this is usually not a problem. *Figure 7* shows the boosted amplifier driving a ±100V square wave into a 2000Ω load at 30 kHz.

±120V Swing Booster (Continued)



A1 = LF357
PNP = 2N5415
NPN = 2N3440

FIGURE 6.

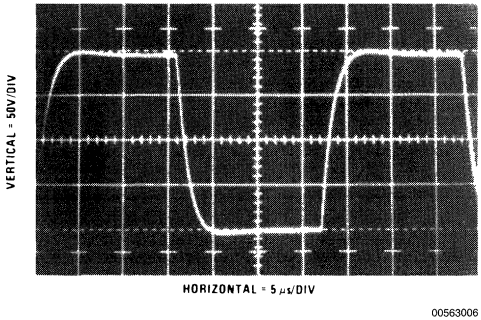
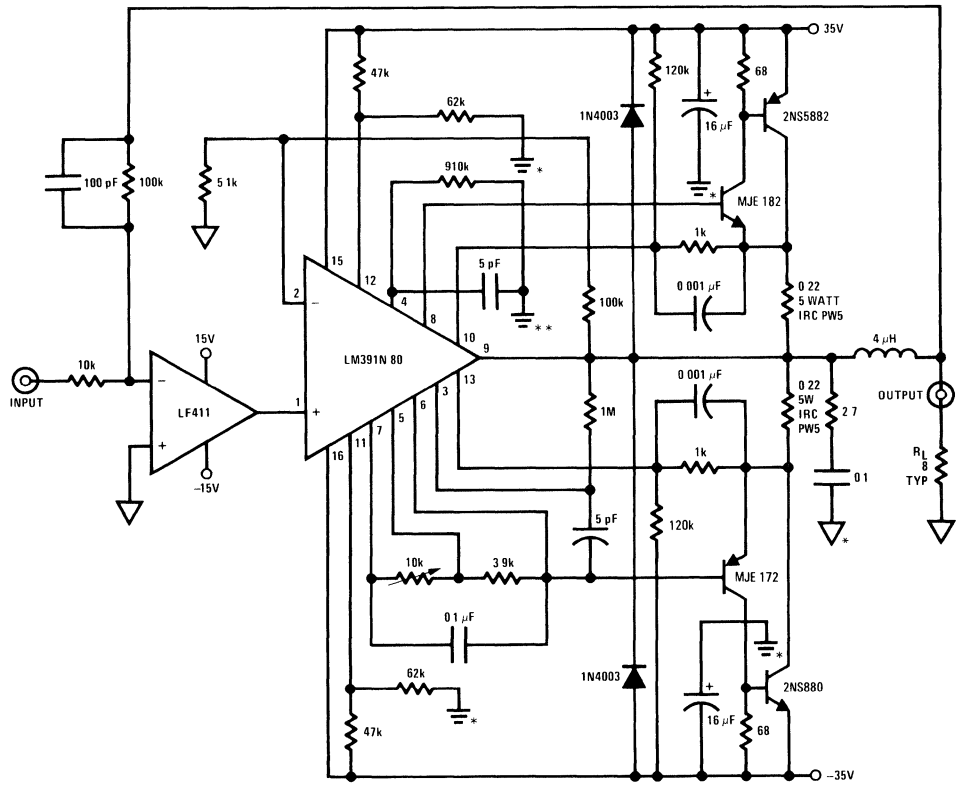


FIGURE 7.

High Current Booster

High current loads are well served by the booster circuit of *Figure 8*. While this circuit does provide voltage gain, its ability to drive 3A of current into an 8Ω load at 25V peak makes it useful as a current booster. In this circuit, the LM391-80 driver chip and its associated power transistors are placed inside the LF411's feedback loop. The 5 pF capacitor at pin 3 of the LM391-80 sets the booster bandwidth well past 250 kHz. The 100k-10k feedback resistors set a gain of ten, and the 100 pF feedback capacitor rolls off the loop gain at 100 kHz to insure stability for the amplifier-booster combination. The 2.7Ω-0.1 µF damper network and the 4 µH inductor prevent oscillations. The zero signal current of the output stage is set with the 10k potentiometer (pins 6-7 at the LM391) while a DVM is monitored for 10 mV across the 0.22Ω output resistors.

High Current Booster (Continued)



Adjust 10k pot
for 25 mA zero signal
current through the
0 22Ω resistors

* High frequency ground

** Input Ground

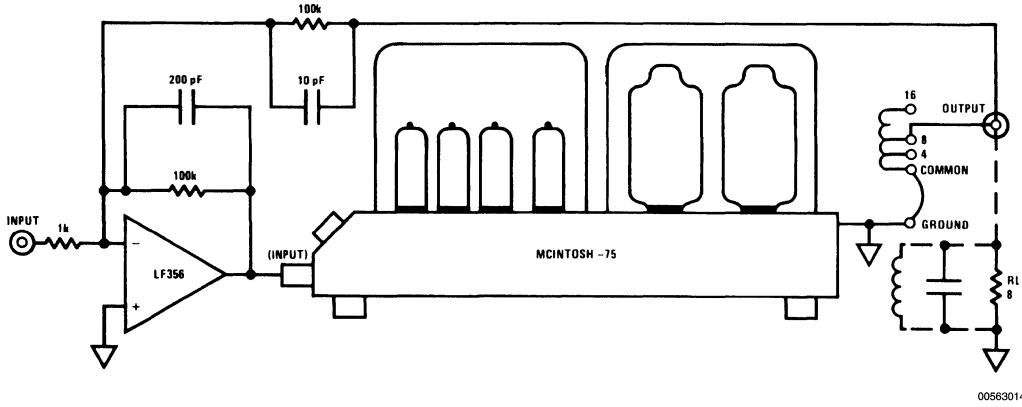
Note: All grounds should be tied together
only at power supply ground.
5 0° C/W heat sink on BD348 and BD349
3.0° C/W heat sink on BD360 and BD361

FIGURE 8.

Indestructible, Floating Output Booster

Figure 9 shows how a high quality audio amplifier can be used as a current-voltage booster for AC signals. The audio amplifier, specified as the booster, is a venerable favorite in research labs, due to its transformer isolated output and clean response. The LF356 op amp's loop is closed locally at a DC gain of 100, and rolled off at 50 kHz by the 200 pF capacitor. The audio amplifier booster's output is fed back via the 100k resistor for an overall AC gain of 100 with respect to the booster amplifier output. The arrangement is ideal for laboratory use because the vacuum tube driven transformer isolated output is extremely forgiving and almost indestructible. AC variable frequency power supplies, shaker table drives, motors and gyro drives, as well as other difficult inductive and active loads, can be powered by this booster. Power output is 75W into 4Ω-16Ω, although loads of 1Ω can be driven at reduced power output.

Indestructible, Floating Output Booster (Continued)



Phase Shift — Less than ±8° 20-20 kHz
Power Output — 75 watts RMS 16 Hz-60 kHz
Output Impedance — Less than 10% of rated output load Z
Frequency Response — 10 Hz-100 kHz-1 dB
16 Hz-40 kHz-0.1 dB
16 Hz-60 kHz-0 5 dB

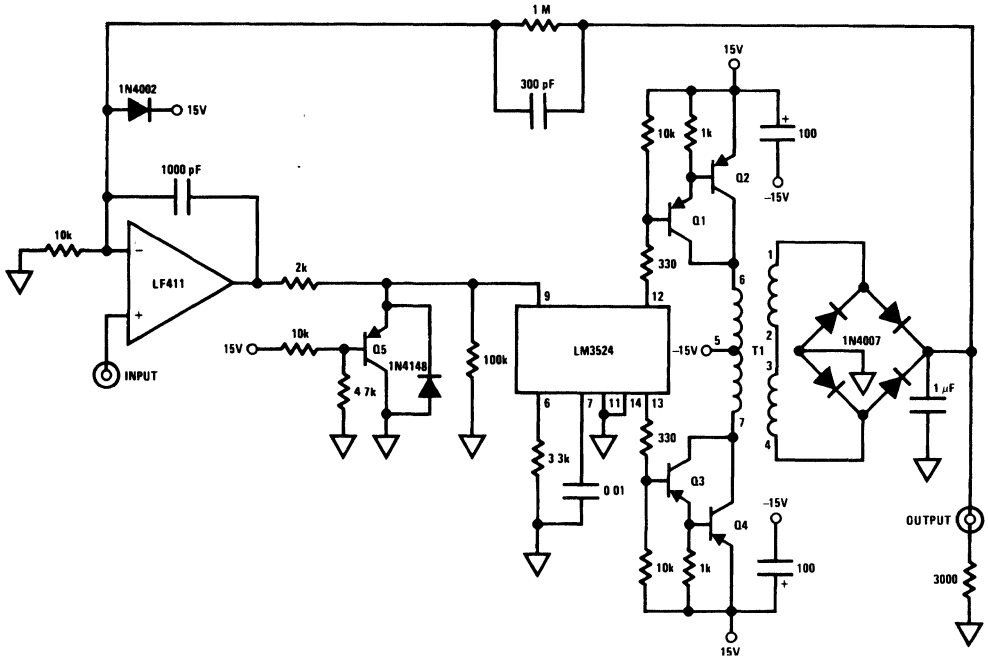
FIGURE 9.

1000V-300 mA Booster

Figure 10 diagrams a very high voltage, high current booster which will allow an op amp to control up to 300W for positive outputs up to a staggering 1000V. This performance is achieved without sacrificing efficiency because this booster, in contrast to all the others shown, operates in a switching mode. In addition, this booster runs off ±15V supplies and has the highly desirable property of *not* requiring a high voltage power supply to achieve its high potential outputs. The high voltage required for the output is directly generated by a switching DC-DC converter which forms an integral part of the booster. The LM3524 switching regulator chip is used to pulse width modulate the transistors which provide switched 20 kHz drive to the TY-85 step-up transformer. The transformer's rectified and filtered output is fed back to the LF411, which controls the input to the LM3524 switching regulator. In this manner, the high voltage booster, although operating switched mode, is controlled by the op amp's feedback action in a similar fashion to all the other designs. Q5 and the diode act as clamps to prevent the LF411's output swing from damaging the LM3524's 4V input on start-up. The diode at the LF411 swing junction prevents high voltage transients coupled through the feedback capacitor from destroying the amplifier The 1 MΩ-10k feedback resistors set the gain of the amplifier at 100 so that a 10V input will give a 1000V output. Although the 20 kHz torroid switching rate places an upper limit on how fast information can be transmitted around the loop, the 1 µF filter capacitor at the circuit output restricts the bandwidth. For the design shown, full power sine wave output frequency is 55H. *Figure 11* shows the response of the boosted LF411 when a 10V pulse (Trace A) is applied to the circuit input. The output (Trace B) goes to 1000V in about 1 ms, while fall time is about 10 ms because of capacitor discharge time. During the output pulse's rise time the booster is slew rate limited and the switching action of the torroid is just visible in the leading edge of the pulse.

The reader is advised that the construction, testing and use of this circuit must be approached with the greatest care. The output potentials produced are many times above the level which will kill. Repeating, the output of this circuit is lethal.

1000V-300 mA Booster (Continued)



T1 = Triad TY-85
Q1, Q3 = 2N3468
Q2, Q4 = 2N4399
Q5 = 2N2907

CAUTION:
LETHAL OUTPUT POTENTIALS

FIGURE 10. Son of Godzilla Booster

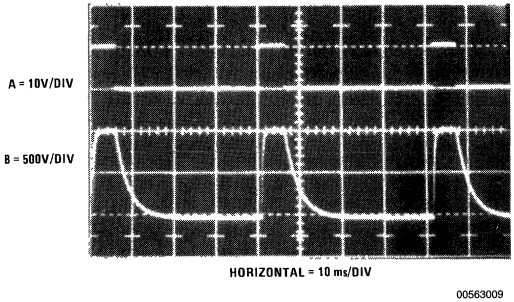


FIGURE 11.

300V Output Booster

The circuit of *Figure 12* is another high voltage booster, but will only provide 10 mA of output current. This positive-output-only circuit will drive 350V into a 30k load, and is almost immune to load shorts and reverse voltages. A solid state output requires substantial protection against these conditions. Although the circuit shown has a 350V limit, tubes (remember them?) with higher plate voltage ratings can extend the output capacity to several kilovolts. In this circuit, our thermionic friends are arranged in a common cathode (V2B) loaded-cathode-follower (V2A) output, driven from a common cathode gain stage (V1). The booster output is fed back to the LF357 via the 1 MΩ resistor. Local feedback is used to stabilize the LF357, while the pF-1 MΩ pair rolls off the loop at 1 MHz. Because the V1 stage inverts, the feedback summing junction is placed at the LF357 positive input. The parallel diodes at the summing junction prevent

300V Output Booster (Continued)

high voltage from destroying the amplifier during circuit start-up and slew rate limiting. Tubes are inherently much more tolerant of load shorts and reverse voltages than transistors, and are much easier to protect. In this circuit, an LM335 temperature sensor is in contact with V2. This sensor's output is compared with another LM335 which senses ambient temperature. Under normal operating conditions, V2 operates about 45°C above ambient and the "+" input of the LF311 is about −100 mV, causing its output to be low. When a load fault occurs, V2's plate dissipation increases, causing its associated LM335's output to rise with respect to ambient temperature. This forces the LF311's output high, which makes the LF357 output go low, shutting down the output stage. Adequate hysteresis is provided by the thermal time constant of V2 and the 10 MΩ-1 µF delay in the LF311 input line. *Figure 13* shows the response of this amplifier booster at a gain of about 25. With a 15V input pulse (Trace A), the output (Trace B) goes to 350V in 1 µs, and settles within 5 µs. The falling edge slews equally fast and settling occurs within 4 µs.

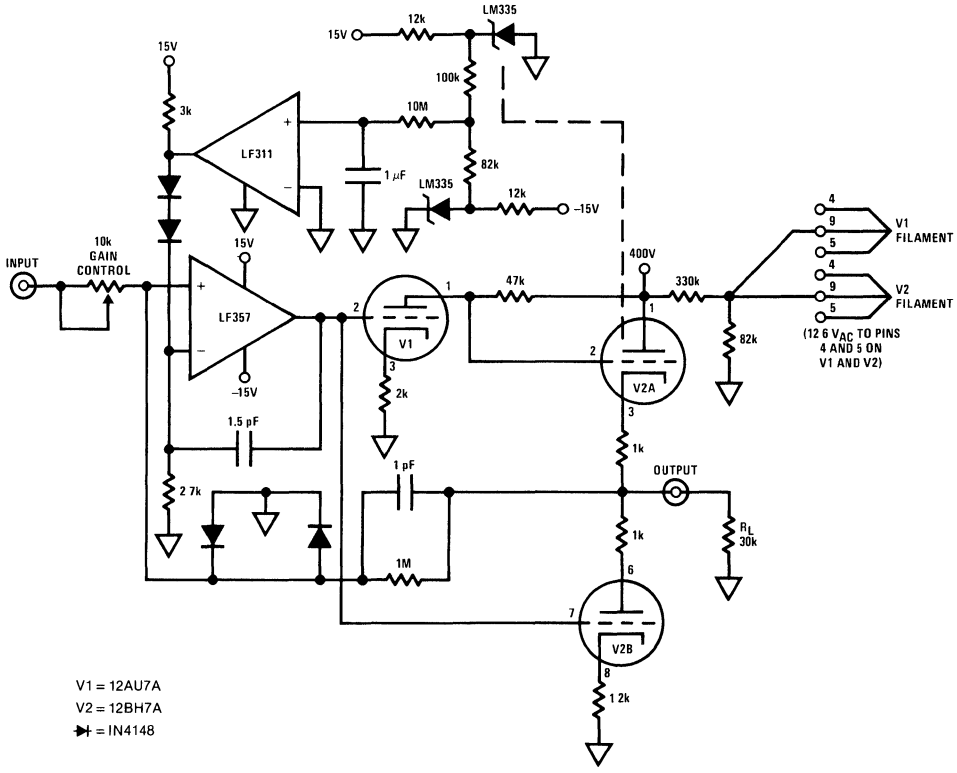


FIGURE 12.

300V Output Booster (Continued)

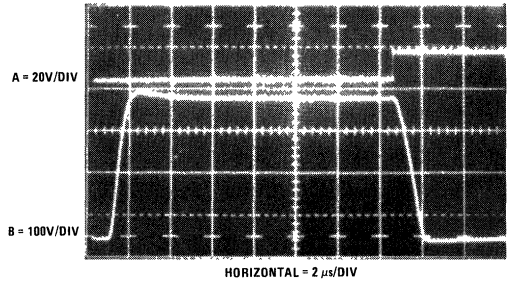


FIGURE 13.

Figure 14 is a table which summarizes the information in this article and will help you to pick the right booster for your particular application.

Figure	Voltage Gain	Current Gain	Bandwidth	Comments
1	No	Yes—200 mA	Depends on op amp. Typical 1 MHz	Full "+" and "–" output swing. Stable into 50Ω-10,000 pF load. Inverting or non-inverting operation. Simple.
3	No	Yes—200 mA	Full output to 5 MHz-3dB. Point at 11 MHz.	Ultra fast. 750V/μs. Full bipolar output. Inverting operation only.
5	Yes—24V swing	No	Depends on op amp.	Requires that load float from ground.
6	Yes—±100V	Yes—50 mA	50 kHz typical.	Full "+" and "–" output swing. Allows inverting or non-inverting operation. Simplified version ideal for CRT deflection plate driving. More complex version drives full 200V swing into 2 kΩ and 1000 pF.
8	Yes—±30V	Yes—3A	50 kHz	Full "+" and "–" output swing. Allows inverting or non-inverting operation.
9	Yes—70V swing	Yes—3A	100 kHz	Output extremely rugged. Well suited for driving difficult loads in lab. Set-ups. Full bipolar output. AC only.
10	Yes—1000V	Yes—300 mA	50 Hz	High voltage at high current. Switched mode operation allows operation from ±15V supplies with good efficiency. Limited bandwidth with asymmetrical slewing. Positive outputs only.
12	Yes—350V	No	500 kHz	Output very rugged. Good speed. Positive outputs only.

FIGURE 14.

Applications of the LM392 Comparator Op Amp IC

National Semiconductor
Application Note 286
Michael X. Maida

The LM339 quad comparator and the LM324 op amp are among the most widely used linear ICs today. The combination of low cost, single or dual supply operation and ease of use has contributed to the wide range of applications for these devices.

The LM392, a dual which contains a 324-type op amp and a 339-type comparator, is also available. This device shares all the operating features and economy of 339 and 324 types with the flexibility of both device types in a single 8-pin mini-DIP. This allows applications that are not readily implemented with other devices but retain simplicity and low cost. *Figure 2* provides an example.

Sample-Hold Circuit

The circuit of *Figure 2* is an unusual implementation of the sample-hold function. Although its input-to-output relationship is similar to standard configurations, its operating principle is different. Key advantages include simplicity, no hold step, essentially zero gain error and operation from a single 5V supply. In this circuit the sample-hold command pulse (Trace A, *Figure 1*) is applied to Q3, which turns on, causing current source transistor Q4's collector (Trace B, *Figure 1*) to go to ground potential. Amplifier A1 follows Q4's collector voltage and provides the circuit's output (Trace C, *Figure 1*). When the sample-hold command pulse falls, Q4's collector drives a constant current into the 0.01 µF capacitor. When the capacitor ramp voltage equals the circuit's input voltage, comparator C1 switches, causing Q2 to turn off the current source. At this point the collector voltage of Q4 sits at the circuit's input voltage. Q1 insures that the comparator will not self trigger if the input voltage increases during a "hold" interval. When a DC biased sine wave is applied to the circuit (Trace D, *Figure 1*) the sampled output (Trace E, *Figure 1*) is available at the circuit's output. The ramping action of the Q4 current source during the "sample" states is just visible in the output.

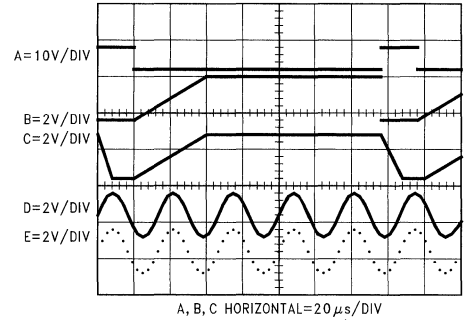
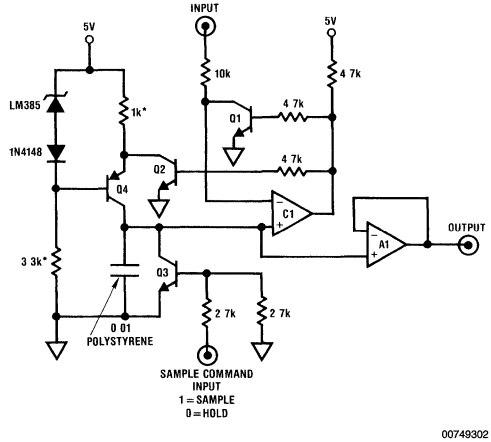


FIGURE 1.



Q1, Q2, Q3 = 2N2369

Q4 = 2N2907

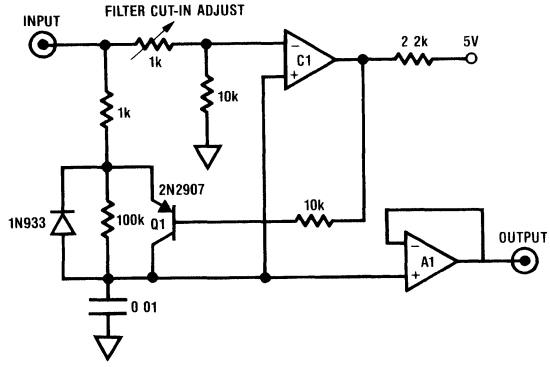
C1, A1 = LM392 amplifier-comparator dual

*1% metal film resistor

FIGURE 2.

"Fed-Forward" Low-Pass Filter

In *Figure 3* the LM392 implements a useful solution to a common filtering problem. This single supply circuit allows a signal to be rapidly acquired to final value but provides a long filtering constant. This characteristic is useful in multiplexed data acquisition systems and has been employed in electronic infant scales where fast, stable readings of infant weight are desired despite motion on the scale platform. When an input step (Trace A, *Figure 4*) is applied, C1's negative input will immediately rise to a voltage determined by the 1k pot-10 kΩ divider. C1's "+" input is biased through the 100 kΩ-0.01 µF time constant and phase lags the input. Under these conditions C1's output will go low, turning on Q1. This causes the capacitor (Waveform B, *Figure 1*) to charge rapidly towards the input value. When the voltage across the capacitor equals the voltage at C1's positive input, C1's output will go high, turning off Q1. Now, the capacitor can only charge through the 100k value and the time constant will be long. Waveform B clearly shows this. The point at which the filter switches from short to long time constant is adjustable with the 1 kΩ potentiometer. Normally, this is adjusted so that switching occurs at 90%–98% of final value, but the photo was taken at a 70% trip point so circuit operation is easily discernible. A1 provides a buffered output. When the input returns to zero the 1N933 diode, a low forward drop type, provides rapid discharge for the capacitor.



A1, C1 = LM392 amplifier-comparator dual

FIGURE 3.

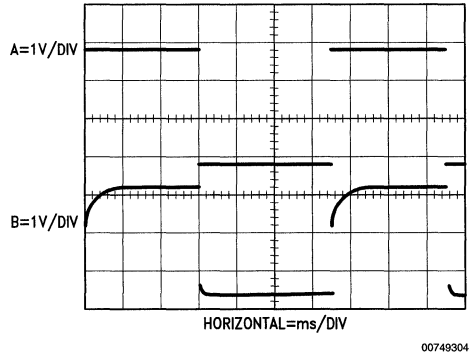


FIGURE 4.

Variable Ratio Digital Divider

In *Figure 5* the circuit allows a digital pulse input to be divided by any number from 1 to 100 with control provided by a single knob. This function is ideal for bench type work where the rapid set-up and flexibility of the division ratio is highly desirable. When the circuit input is low, Q1 and Q3 are off and Q2 is on. This causes the 100 pF capacitor to accumulate a quantity of charge (Q) equal to

$Q = CV$

where C = 100 pF

and V = the LM385 potential (1.2V) minus the $V_{CE(SAT)}$ of Q2.

When the input goes high (Trace A, *Figure 6*) Q2 goes off and Q1 turns on Q3. This causes Q3 to displace the 100 pF capacitor's charge into A1's summing junction. A1's output responds (Waveform B, *Figure 6*) by jumping to the required

Variable Ratio Digital Divider

(Continued)

value to maintain the summing junction at 0V. This sequence is repeated for every input pulse. During this time A1's output will form the staircase shape shown in Trace B as the 0.02 µFfeedback capacitor is pumped up by the charge dispensing action into A1's summing junction. When A1's output is great enough to just bias C1's "+" input below ground, C1's output (Trace C, *Figure 6*) goes low and resets A1 to 0V. Positive feedback to C1's "+" input (Trace D, *Figure 6*) comes through the 300 pF unit, insuring adequate reset time for A1. The 1 MΩ potentiometer, by setting the number of steps in the ramp required to trip C1, controls the circuit input-output division ratio. Traces E–G expand the scale to show circuit detail. When the input (Trace E) goes high, charge is deposited into A1's summing junction (Trace F) and the resultant staircase waveform (Trace G) takes a step.

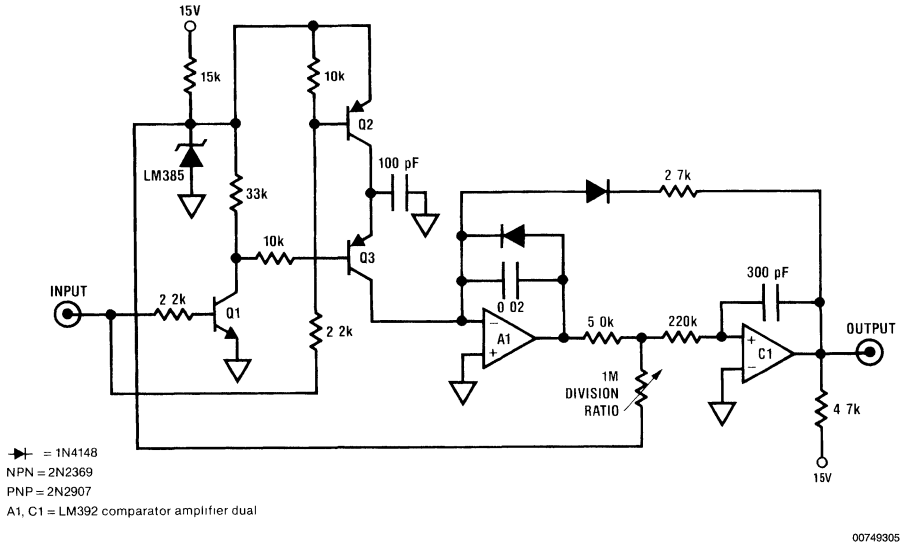


FIGURE 5.

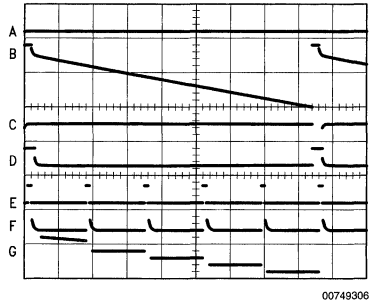


FIGURE 6.

Trace	Vertical	Horizontal
A	10V	500 µs
B	1V	500 µs
C	50V	500 µs
D	50V	500 µs
E	10V	50 µs

Trace	Vertical	Horizontal
F	10 mA	50 µs
G	0.1V	50 µs

Exponential V/F Converter for Electronic Music

Professional grade electronic music synthesizers require voltage controlled frequency generators whose output frequencies are exponentially related to the input voltages. *Figure 7* diagrams a circuit which performs this function with 0.25% exponential conformity over a range from 20 Hz to 15 kHz using a single LM392 and an LM3045 transistor array. The exponential function is generated by Q1, whose collector current will vary exponentially with its base-emitter voltage in accordance with the well known relationship between BE voltage and collector current in bipolar transistors. Normally, this transistor's operating point will vary wildly with temperature and elaborate and expensive compensation is required. Here, Q1 is part of an LM3045 transistor array. Q2 and Q3, located in the array, serve as a heater-sensor pair for A1, which servo controls the temperature of Q2. This causes the entire LM3045 array to be at constant temperature, eliminating thermal drift problems in Q1's operation. Q4 acts as a clamp, preventing servo lock-up during circuit start-up.

Exponential V/F Converter for Electronic Music (Continued)

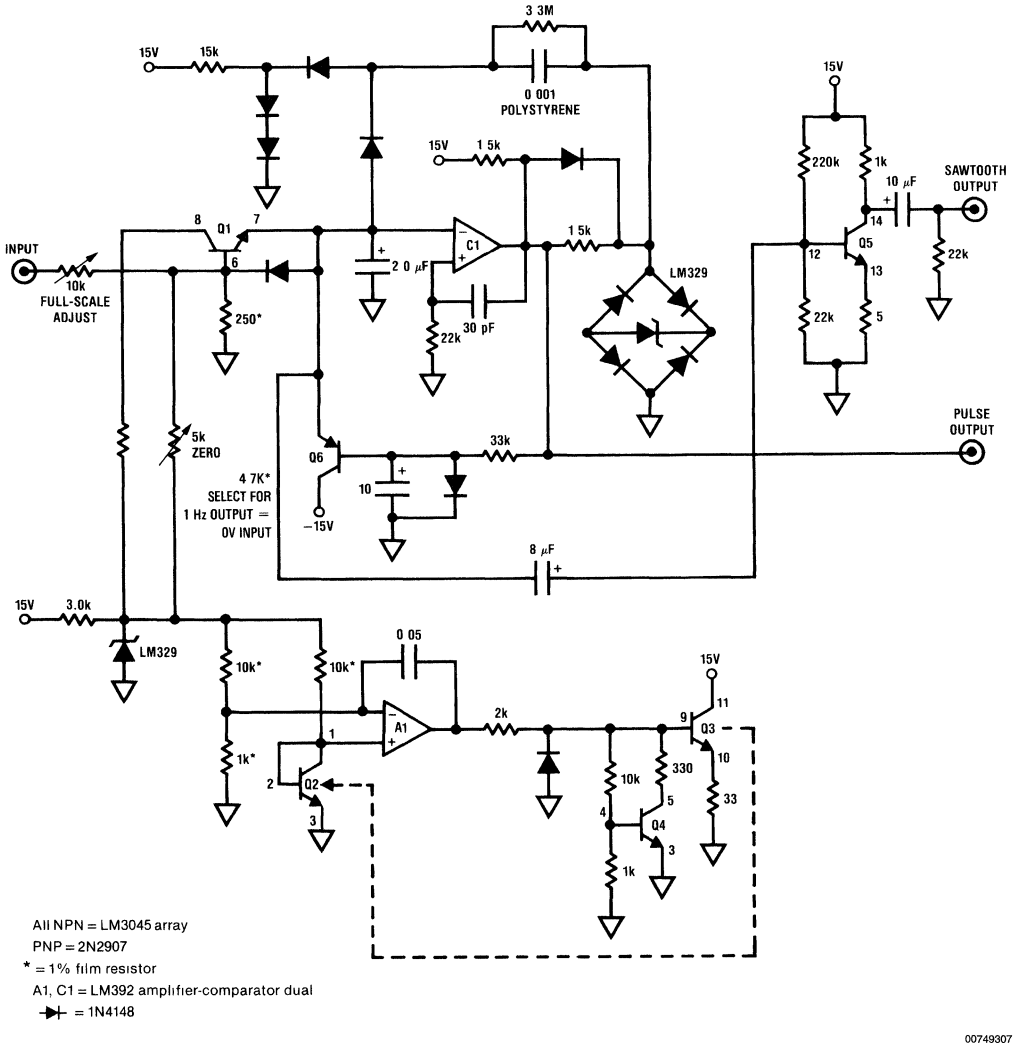


FIGURE 7.

Q1's current output is fed into the summing junction of a charge dispensing I/F converter. C1's output state is used to switch the 0.001 µF capacitor between a reference voltage and C1's "−" input. The reference voltage is furnished by the LM329 zener diode bridge. The comparator's output pulse width is unimportant as long as it permits complete charging and discharging of the capacitor. In operation, C1 drives the 30 pF-22k combination. This RC provides regenerative feedback which reinforces the direction of C1's output. When the 30 pF-22k combination decays, the positive feedback ceases. Thus, any negative going amplifier output will be followed by a positive edge after an amount of time governed by the 30 pF-22k time constant (Waveforms A and B, *Figure 8*). The actual integration capacitor in the circuit is the 2 µF electrolytic. This capacitor is never allowed to charge beyond 10 mV–15 mV because it is constantly being reset by charge dispensed from the switching of the 0.001 µF capacitor (Waveform C, *Figure 8*). Whenever the amplifier's output goes negative, the 0.001 µF capacitor dumps a quantity of charge (Waveform D) into the 2 µF capacitor, forcing it to a lower potential. The amplifier's output going negative also causes a short pulse to be transferred through the 30 pF capacitor to the "+" input. When this negative pulse decays out so that the "+" input is higher than the "−" input, the 0.001 µF capacitor is again able to receive a charge and the entire process repeats. The rate at which this sequence occurs is directly related to the current into C1's summing junction from Q1. Since this current is exponentially related to the

Exponential V/F Converter for Electronic Music (Continued)

circuit's input voltage, the overall I/F transfer function is exponentially related to the input voltage. This circuit can lock-up under several conditions. Any condition which would allow the 2 µF electrolytic to charge beyond 10 mV–20 mV (start-up, overdrive at the input, etc) will cause the output of the amplifier to go to the negative rail and stay there. The 2N2907A transistor prevents this by pulling the "–" input towards –15V. The 10 µF-33k combination determines when the transistor will come on. When the circuit is running normally, the 2N2907 is biased off and is effectively out of the circuit. To calibrate the circuit, ground the input and adjust the zero potentiometer until oscillations just start. Next, adjust the full-scale potentiometer so that frequency output exactly doubles for each volt of input (e.g., 1V per octave for musical purposes). Repeat these adjustments until both are fixed. C1 provides a pulse output while Q5 AC amplifies the summing junction ramp for a sawtooth output.

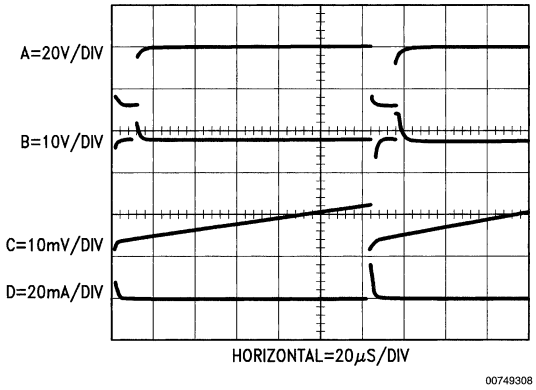
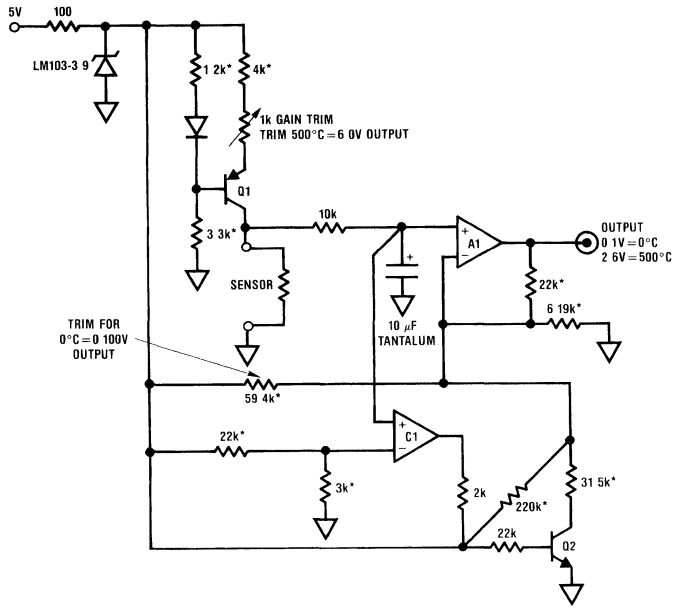


FIGURE 8.

Linearized Platinum RTD Thermometer

In *Figure 9* the LM392 is used to provide gain and linearization for a platinum RTD in a single supply thermometer circuit which measures from 0°C to 500°C with ±1°C accuracy. Q1 functions as a current source which is slaved to the LM103-3.9 reference. The constant current driven platinum sensor yields a voltage drop which is proportionate to temperature. A1 amplifies this signal and provides the circuit output. Normally the slight nonlinear response of the RTD would limit accuracy to about ±3 degrees. C1 compensates for this error by generating a breakpoint change in A1's gain for sensor outputs above 250°C. When the sensor's output indicates 250°C, C1's "+" input exceeds the potential at the "–" input and C1's output goes high. This turns on Q2 whose collector resistor shunts A1's 6.19k feedback value, causing a gain change which compensates for the sensor's slight loss of gain from 250°C to 500°C. Current through the 220k resistor shifts the offset of A1 so no "hop" occurs at the circuit output when the breakpoint is activated. A precision decade box is used to calibrate this circuit. With the box inserted in place of the sensor, adjust 0°C for 0.10V output for a value of 1000Ω. Next dial in 2846Ω (500°C) and adjust the gain trim for an output of 2 60V. Repeat these adjustments until both zero and full-scale are fixed at these points.

Linearized Platinum RTD Thermometer (Continued)



Sensor = Rosemount
118 MF-1000-A
1000Ω at 0°C

Q1 = 2N2907

Q2 = 2N2222A

A1, C1 = LM392 amplifier-comparator dual

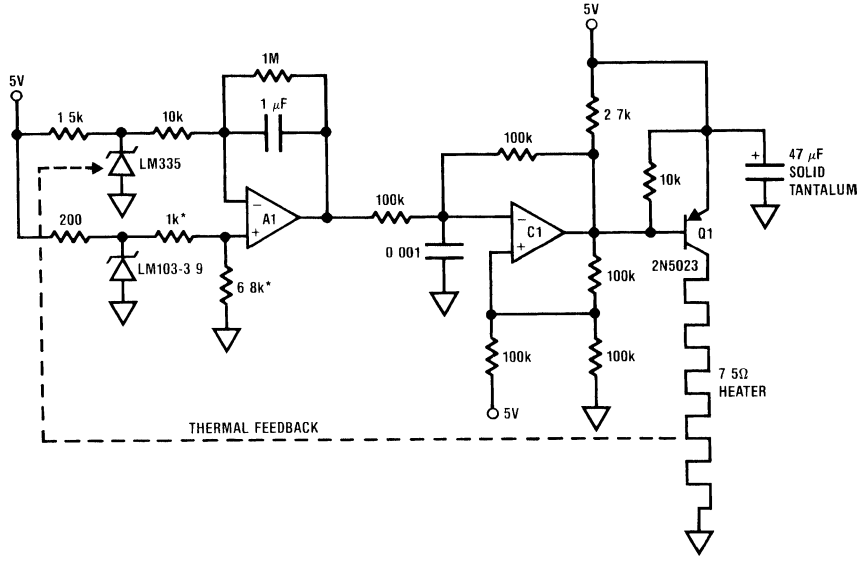
*metal film resistor

FIGURE 9.

Temperature Controller

Figure 10 details the LM392 in a circuit which will temperature-control an oven at 75°C. This is ideal for most types of quartz crystals. 5V single supply operation allows the circuit to be powered directly from TTL-type rails. A1, operating at a gain of 100, determines the voltage difference between the temperature setpoint and the LM335 temperature sensor, which is located inside the oven. The temperature setpoint is established by the LM103-3.9 reference and the 1k–6.8k divider. A1's output biases C1, which functions as a pulse width modulator and biases Q1 to deliver switched-mode power to the heater. When power is applied, A1's output goes high, causing C1's output to saturate low. Q1 comes on and delivers DC to the heater. When the oven warms to the setpoint, A1's output falls and C1 begins to pulse width modulate the heater in servo control fashion. In practice the LM335 should be in good thermal contact with the heater to prevent servo oscillation.

Temperature Controller (Continued)



A1, C1 = LM392 amplifier-comparator dual

FIGURE 10.

References

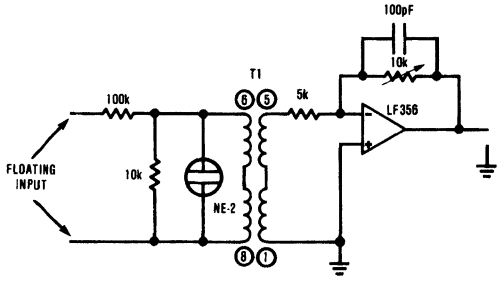
1. *Transducer Interface Handbook,* pp. 220–223, Analog Devices, Inc.

2. "A New Ultra-Linear Voltage-to-Frequency Converter", Pease, R. A.; *1973 NEREM Record* Volume 1, page 167.

Isolation Techniques for Signal Conditioning

National Semiconductor
Application Note 298
Michael X. Maida

Industrial environments present a formidable challenge to the electronic system designer. In particular, high electrical noise levels and often excessive common mode voltages make safe, precise measurement difficult. One of the best ways to overcome these problems is by the use of isolated measurement techniques. Typically, these approaches utilize transformers or opto isolators to galvanically isolate the input terminals of the signal conditioning amplifier from its output terminal. This breaks the common ground connection and eliminates noise and dangerous common mode voltages. The conflicting requirements for good accuracy and total input/output galvanic isolation requires unusual circuit techniques. A relatively simple isolated signal conditioner appears in *Figure 1*.



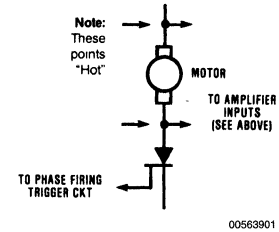
OUTPUT= INPUT ÷100 & ISOLATED T1=UTC #P2

To AC Line From Full Wave Bridge

FIGURE 1.

Floating Input High Voltage Motor Monitor

In this inexpensive circuit, a wideband audio transformer permits safe, ground referenced monitoring of a motor which is powered directly from the 115VAC line. *Figure 2* details the measurement arrangement. The floating amplifier inputs are applied directly across the brush-type motor. The 100k-10k string, in combination with the transformer ratio, provides a nominal 100:1 division in the observed motor voltage while simultaneously allowing a ground referenced output. The NE-2 bulb suppresses line transients while the 10k potentiometer trims the circuit for a precise 100:1 scale factor. To calibrate the circuit, apply a 10-volt RMS 1kHz sine wave to the floating inputs, and adjust the potentiometer for 100 millivolts RMS output. Full power bandwidth extends from 15Hz to 45kHz ± .25dB with the –3dB point beyond 85kHz. Risetime is about 10 microseconds. *Figure 3* shows the motor waveform at the ground referenced circuit output. The isolated, wideband response of the circuit permits safe monitoring of the fast rise SCR turn-on as well as the motor's brush noise.



AC Line From Full Wave Bridge

FIGURE 2.

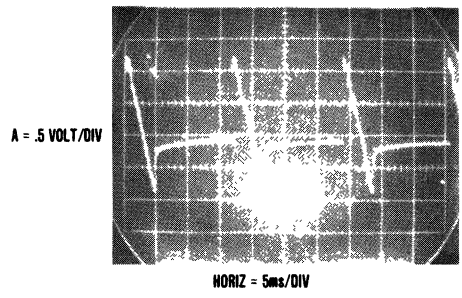


FIGURE 3.

Isolated Temperature Measurement

Figure 4 shows a scheme which allows an LM135 temperature sensor to operate in a fully floating fashion. In this circuit, the LM311 puts out a 100 microsecond pulse at about 20Hz. This signal biases the PNP transistor, whose collector load is composed of the 1kΩ unit and the primary of T1. The voltage that develops across T1's primary (waveform A, *Figure 5*) will be directly dependent upon the value that the LM135 temperature sensor clamps the secondary at. Waveform B, *Figure 5* details the transformer primary current.

Isolated Temperature Measurement (Continued)

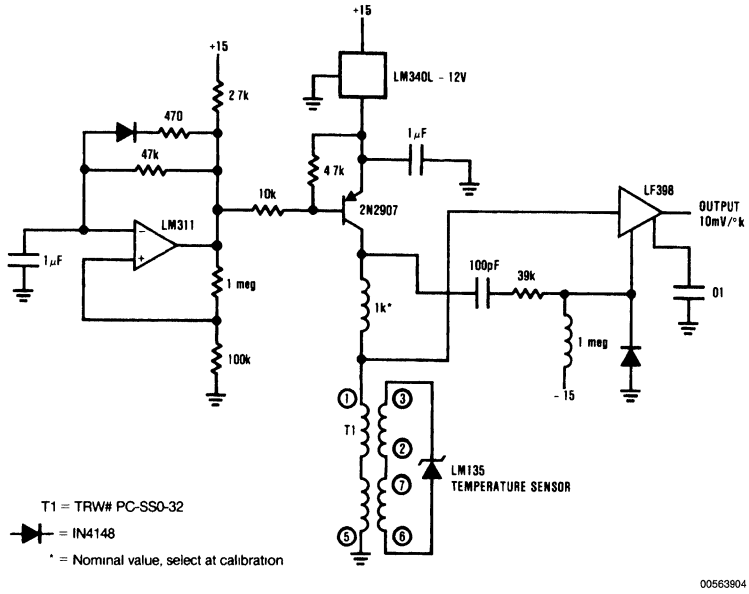


FIGURE 4.

This voltage value, of course, varies with the temperature of the LM135 in accordance with its normal mode of operation. The LF398 sample-and-hold IC is used to sample the transformer primary voltage and presents the circuit output as a DC level. The 100 pF-39k-1MΩ combination presents a trigger pulse (waveform C, *Figure 5*) to the LF398, so that the sampling period does not finish until well after the LM135 has settled. The LM340 12-volt regulator provides power supply rejection for the circuit. To calibrate, replace the LM135 with an LM336 2.5-volt diode of known breakdown potential. Next, select the 1kΩ valve until the circuit output is the same as the LM336 breakdown voltage. Replace the LM336 with the LM135 and the circuit is ready for use.

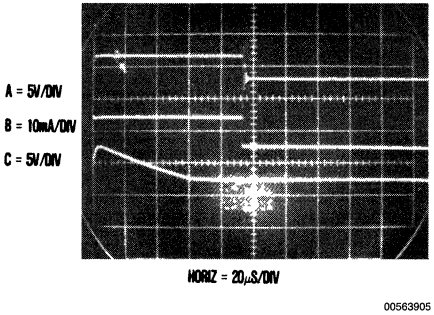


FIGURE 5.

Fully Isolated Pressure Transducer Measurement

Strain gauge-based transducers present special difficulties if total isolation from ground is required. They need excitation power in addition to their output signal. Some industrial measurement situations require that the transducer must be physically connected to a structure which is floating at a high common mode voltage. This means that the signal conditioning circuitry must supply fully floating drive to the strain gauge bridge, while also providing isolated transducer output signal amplification. *Figure 6* details a way to accomplish this. Here, the strain bridge is excited by a transformer which generates a pulse of servo-controlled amplitude. The pulse is generated by storing the sampled amplitude of the output pulse as a DC level, and supplying this information to a feedback loop which controls the voltage applied to the output switch. A2 functions as an oscillator which simultaneously drives Q2-Q3 and the LF398 (A3) sample mode pin. When A2's output pulse ends, A3's output is a DC level equal to the amplitude of the output pulse which drives the strain bridge. The dual secondary of T1 allows accurate magnetic sampling of the strain bridge output pulse without sacrificing electrical isolation. A3's output is compared to the LH0070 10-volt reference by A4, whose output drives Q1. Q1's emitter provides the DC supply level to the Q2-Q3 switch. This servo action forces the pulses applied to the strain gauge transducer (waveform A, *Figure 7*) to be of constant amplitude and equal to the 10-volt LH0070 reference output. Some amount of the pulse's energy is stored in the 100μF capacitor and used to power the LM358 dual (A1) followers.

Fully Isolated Pressure Transducer Measurement (Continued)

These devices unload the output of the transducer bridge and drive the primary of T2. T2's secondary output amplitude (waveform B, *Figure 7*) represents the transducer output value. This potential is amplified by A5 and fed to A6, a sample-and-hold circuit. A6's sample command is a shortened version of the A2 oscillator pulse. The 74C221 generates this pulse (waveform C, *Figure 7*).

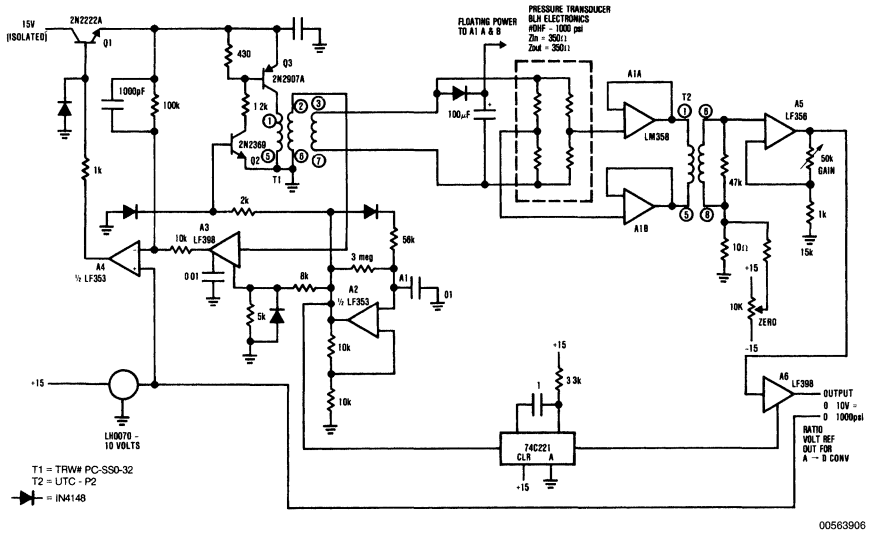


FIGURE 6.

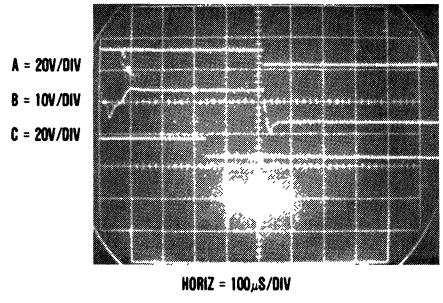


FIGURE 7.

Because the A6 sample command falls during the settled section of T2's output pulse, A6's output will be a DC representation of the amplified strain gauge pressure transducer output. The LH0070 output may be used to ratiometrically reference a monitoring A/D converter. To calibrate this circuit, insert a strain bridge substitution box (e.g., BLH model 625) in place of the transducer and dial in the respective values for zero and full-scale output (which are normally supplied with the individual transducer). Adjust the circuit "zero" and "gain" potentiometers until a 0- to 10-volt output corresponds to a 0 to 1000psi pressure input.

1.5-Volt Powered Isolated Pressure Measurement

Figure 8 diagrams another pressure measurement circuit. This circuit presents a frequency output which is fully isolated by the transformer indicated. The entire circuit may be powered from a 1.5-volt supply, which may be derived from a battery or solar cells. The potentiometer output of the pressure transducer used is fed to a voltage-to-frequency converter circuit. In this V-F circuit, an LM10 op amp acts as an input amplifier, and forces the collector current of Q1 to be linearly proportional to V_{IN} for a range of 0 to +400 millivolts. Likewise, the reference amplifier of the LM10 causes Q2's output current to be stable and constant under all conditions. The transistors Q3-Q10 form a relaxation oscillator, and every time the voltage across C1 reaches 0.8-volt, Q6 is commanded to reset it to zero volts differential. This basic circuit is not normally considered a very accurate technique, because the dead time, while Q6 is saturated, will cause a large (1%) nonlinearity in the V-to-F transfer curve. However, the addition of R_X causes the reference current flowing through Q2 to include a term which is linearly proportional to the signal, which corrects the transfer nonlinearity.

1.5-Volt Powered Isolated Pressure Measurement (Continued)

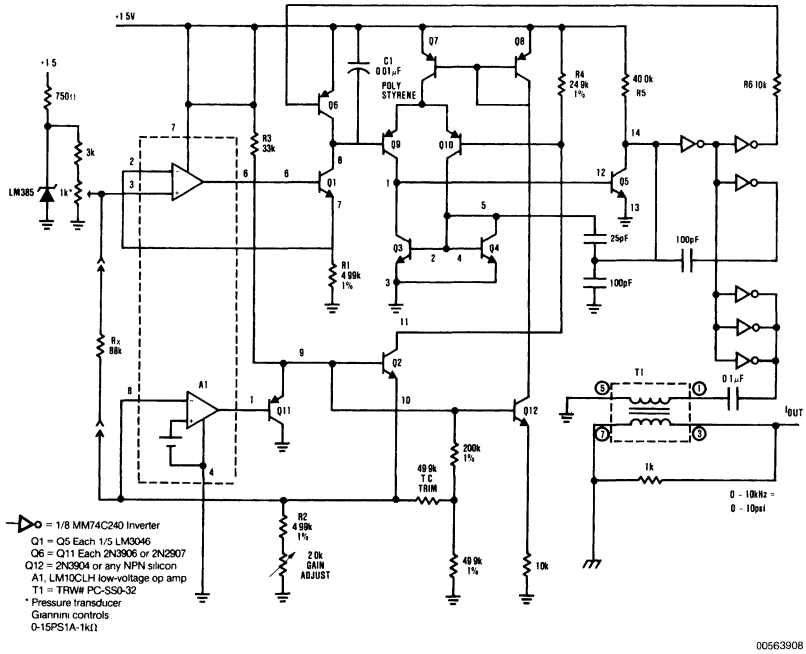


FIGURE 8.

The NSC MM74C240 inverters are employed because this IC has the only uncommitted inverters with such a low (0.6 to 0.8V) threshold that they can operate on a supply as low as 1.2 volts.

The 49.9k resistors which feed into Q2's emitter act as a gain tempco trim, as Q12's Vbe is used as a temperature sensor. If the output frequency is 100ppm/C too fast/hot, you can cut the resistor to 20k. If f is too slow/hot, add more resistance in series with the 49 9k. Total current drain for this circuit is about 1 milliampere.

Fully Isolated "Zero Power" Complete A/D Converter

Figure 9 shows a complete 8-bit A/D converter, which has all input and output lines fully floating from system ground. In addition, the A/D converter requires *no* power supply for operation! Circuit operation is initiated by applying a convert-command pulse to the "convert-command" input (trace A, *Figure 11*). This pulse simultaneously forces the "Data Output" line low (trace B, *Figure 11*) and propagates across the isolation transformer. The pulse appears at the transformer secondary (*Figure 10*, trace A) and charges the 100 μF capacitor to five volts. This potential is used to supply power to the floating A/D conversion circuitry. The pulse appearing at the transformer secondary is also used to start the A/D conversion by biasing comparator A's negative input low. This causes comparator A's output to go low, discharging the .06μF capacitor (waveform B, *Figure 10*) Simultaneously, the 10kHz oscillator (*Figure 10*, trace D), formed by comparator D and its associated components, is forced off via the 22k diode path. A second diode path also forces comparator D's output low (*Figure 10*, trace E). Note the cessation of oscillation during the time the convert command pulse is high. When the convert command pulse falls, the Q1-Q2 current source begins to charge the .06 μF capacitor. During this time, the 10 kHz comparator C oscillator runs, and comparator D's output is a stream of 10 kc clock pulses. When the ramp (trace B, *Figure 10*) across the .06 μF capacitor exceeds the circuit input voltage, comparator B's output goes high (trace C, *Figure 10*), forcing comparator D's output low. The number of pulses which appeared at comparator D's output is directly proportional to the value of the circuit's input voltage. These pulses are amplified by the two NPN transistors which are used to modulate the data pulse stream back across the transformer. The six series diodes insure that the modulated data does not appear at comparator A's input and trigger it. The pulses appear at the primary (*Figure 11*, trace A) as small amplitude spikes and are then amplified by the data output transistor, whose collector waveform is trace B or *Figure 11*. In this example a 0- to 3-volt input produces 0- to 300 pulses at the output. The 22k diode path averts a +1 count uncertainty error by synchronizing the 10kHz clock to the conversion sequence at the beginning of each conversion. The 500k potentiometer in the current source adjusts the scale factor. The circuit drifts less than 1LSB over 25°C±20°C and requires 45 milliseconds to complete a full scale 300 count conversion.

Fully Isolated "Zero Power" Complete A/D Converter (Continued)

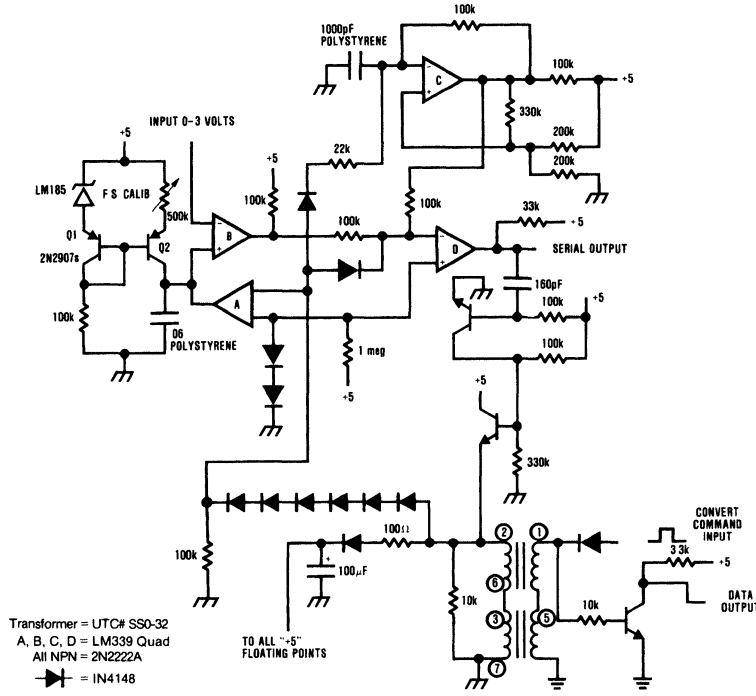


FIGURE 9.

Fully Isolated "Zero Power" Complete A/D Converter (Continued)

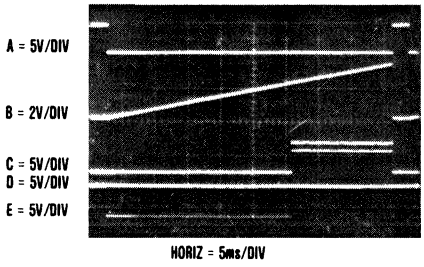


FIGURE 10.

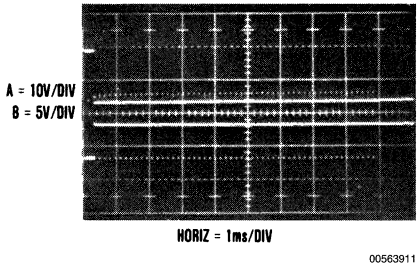


FIGURE 11.

Complete, Floating Multiplexed Thermocouple Temperature Measurement

Figure 12 shows a complete, fully floating multiplexed thermocouple measurement system. Power to the floating system is supplied via T2, which runs in a self oscillating DC-DC converter configuration with the 2N2219 transistors. T2's output is rectified, filtered, and regulated to ±15 volts. An eight channel LF13509 multiplexer is used to sequentially switch 7 inputs and a ground reference into the LM11 amplifier. The LM11 provides gain and cold junction compensation for the thermocouples. The multiplexer is switched from the 74C93 counter, which is serially addressed via the 4N28 opto isolator. The ground referenced channel prevents monitoring instrumentation from losing track of the multiplexer state The LM11's output is fed into a unity gain isolation amplifier. Oscillator drive for the isolation amplifier is derived by dividing down T2's pulsed output, and shaping the 74C90's output with A4 and its associated components. This scheme also prevents unwanted interaction between the T2 DC-DC converter and the isolation amplifier. This circuit, similar to the servo-controlled amplitude pulser described in *Figure 6*, puts a pulse across T1's primary. The amplitude of the pulse is directly dependent on the LM11's output value. T1's secondary receives the pulse and feeds into an LF398 sample-hold-amplifier. The LF398 is supplied with a delayed trigger pulse, so that T1's output is sampled well after settling occurs. The LF398 output equals the value of the LM11. In this fashion, the fully floating thermocouple information may be connected to grounded test equipment or computers. Effective cold-junction compensation results when the thermocouple leads and the LM335 are held isothermal. To calibrate the circuit, first adjust R3 for an LM11 gain of 245.7. Next, short the "+" input of the LM11 and the LM329 to floating common, and adjust R1 so that the circuit output is 2.982 volts at 25°C. Then, remove the short across the LM329 and adjust R2 for a circuit output of 246 millivolts at 25°C. Finally, remove the short at the LM11 input, and the circuit is ready for use.

Complete, Floating Multiplexed Thermocouple Temperature Measurement

(Continued)

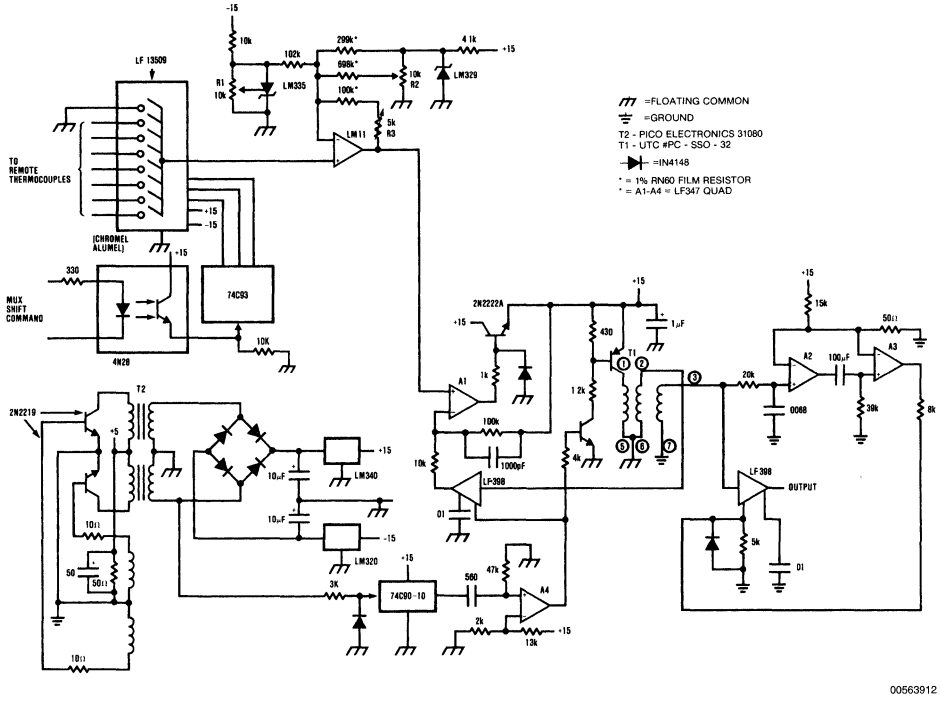


FIGURE 12.

Simple Circuit Detects Loss of 4-20 mA Signal

National Semiconductor
Application Note 300
Robert A. Pease

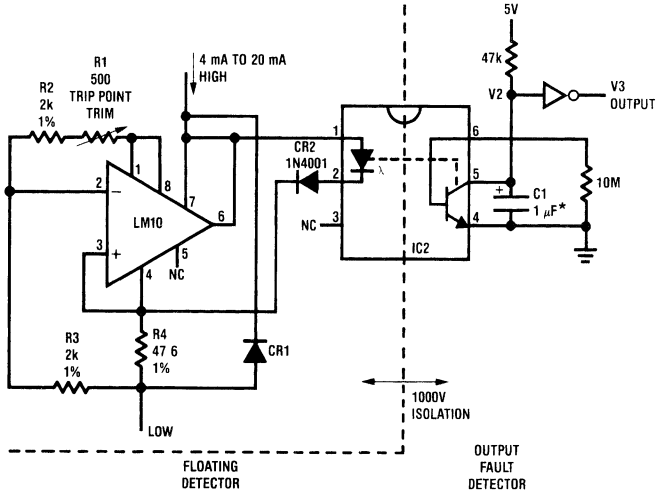
Four-to-twenty milliampere current loops are commonly used in the process control industry. They take advantage of the fact that a remote amplifier can be powered by the same 4-20 mA current that it controls as its output signal, thus using a single pair of wires for signal and power Circuits for making 4-20 mA transmitters are found in the LM10, LM163, and LH0045 data sheets

In general, an expensive isolation amplifier would be required to detect the case of a 4 mA signal falling out of spec (e.g , 3.7 mA) without degrading the isolation of the 4-20 mA current loop

But this new circuit (*Figure 1*) can detect a loss or degradation of signal below 4 mA, with simplicity and low cost The LM10 contains a stable reference at pins 1 and 8, 200 mV positive referred to pin 4 As long as the loop current is larger than 4 mA, the I x R drop across the 47.6Ω resistor, R4, is sufficient to pull the LM10's amplifier input (pin 2) below pin 3 and keep its output (pin 6) turned *OFF*.

The 4-20 mA current will flow through the LED in the optoisolator and provide a *LOW* output at pin 5 of the optoisolator.

When the current loop falls below 3.7 mA, the LM10's input at pin 2 will rise and cause the pin 6 output to fall and steal all the current away from the LED in the optoisolator. Pin 5 of the 4N28 will rise to signify a *fault* condition This *fault* flag will fly for any loop current between 3 7 mA and 0.0 mA (and also in case of reversal or open-circuit). R1 is used to trim the threshold point to the desired value. CR2 is added in series with the LED to make sure it will turn OFF when the LM10's output goes *LOW*. (While the LM10 is guaranteed to saturate to 1.2V, the forward drop of the LED in the 4N28 may be as low as 1.0V, so a diode is added in series with the LED, to insure that it can be shut off.) Note that most operational amplifiers will not respond in a reasonable way if the output pin (6) is connected to the positive supply pin (7), but the LM10 was specifically designed and is specified to perform accurately in this "shunt" mode (Refer to AN-211 application note, TP-14 technical paper, and the LM10 data sheet.)



CR1 = 1N4001, optional, in case of signal reversal
LM10 = NSC LM10CLN or LM10CLH amp/reference
IC2 = 4N28 or similar, optoisolator
V2 = Normally low, high signifies fault (I < 3 7 mA)
V3 = Normally high, low signifies fault (I < 3 7 mA) (buffered output)
*C1 = 1 μF optional, to avoid false output when large AC current is superimposed on 4 0 mA
Disconnect this capacitor when using with circuit of *Figure 2*
▷o = 1/6 MM74C04 or similar, CMOS inverter

00564001

FIGURE 1. Current Loop Fault Detector

While you could manually adjust R1 while observing the status of V3 output, this would be a coarse and awkward trim procedure *Figure 2* shows an improved test circuit which servos the current through the detector circuit, forcing it to be at the threshold value. Then that current can be monitored continuously, and the circuit can be trimmed easily. If the current through R107 starts out too small, the output of the 4N28 will be *HIGH* too much of the time, and the op amp

output will integrate upwards until the current is at the actual threshold of the detector. The integrator's output will stop at the value where the duty cycle of the 4N28 output is exactly 50%. This occurs when the current through R107 is straddling the threshold value.

The positive feedback via R108 assures that the loop oscillates at approximately 50 cycles per second, with a small, well-controlled sawtooth wave at its output. This mode of operation was chosen to insure that the loop does not oscillate at some high, uncontrolled frequency, as it would be difficult in that case to be sure the duty cycle was exactly 50%. This test circuit is advantageous, because you can measure the trip point directly.

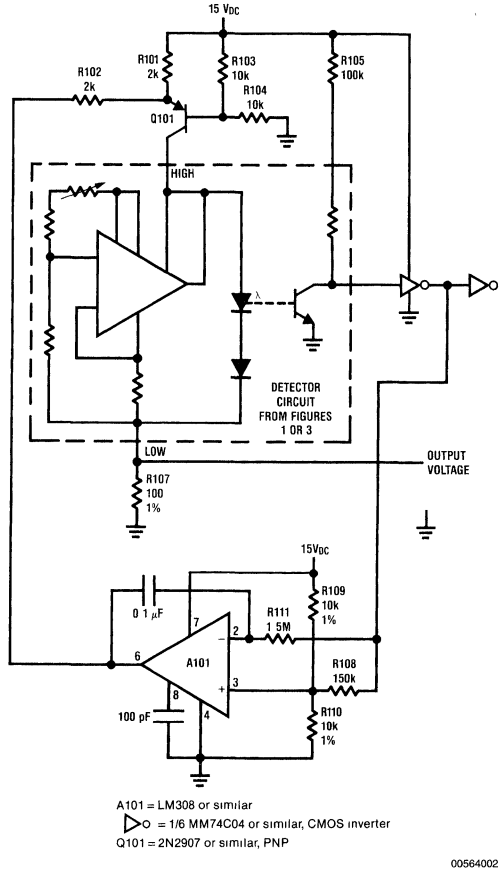


FIGURE 2. Test Circuit for Threshold Detector

The test circuit of *Figure 2* is necessary for trimming the detector in *Figure 3*. This circuit does not have a trim pot, and thus avoids the problem of someone mis-adjusting the circuit after it is once trimmed correctly. It also avoids the compromises between good but expensive trim pots and cheap but unreliable, drifty trim pots. By opening one or more of the links, L1–L4, according to the following procedure, it is easy to trim the threshold level to be within 1% of 3.70 mA (or as desired).

- Observe the DC current through R107 in *Figure 2*
- If $I_{THRESHOLD}$ is larger than 3.950 mA, open link L1;
  —if not, don't
- If $I_{THRESHOLD}$ is larger than 3.830 mA, open link L2;
  —if not, don't
- If $I_{THRESHOLD}$ is larger than 3.760 mA, open link L3;
  —if not, don't
- Then, if $I_{THRESHOLD}$ is larger than 3.720 mA, open link L4;
  —if not, don't

This procedure provides a circuit trimmed to much better than 1% of 3.70 mA, without using any trim pots. Of course, this circuit can be used to detect drop-out of regulation of other floating signals, while maintaining high isolation from ground, good accuracy, low power dissipation (2 mA x 2.5V typical) and low cost.

Other standard values of current loop are 1 mA–5 mA and 10 mA–50 mA. The version shown in *Figure 4* uses higher

resistance values to trip at 0.85 mA. The circuit in *Figure 5* has an additional transistor, to accommodate currents as large as 50 mA without damage or loss of accuracy, and provide an 8.5 mA threshold.

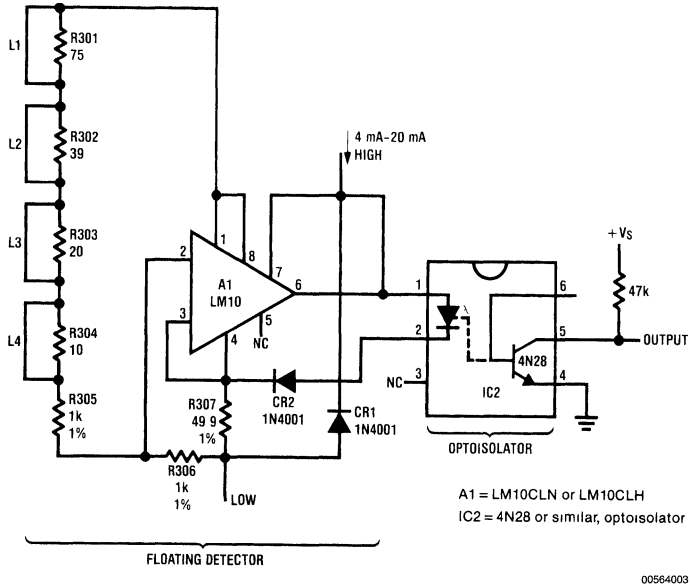


FIGURE 3. Fault Detector with Low-Cost Trim Scheme (To be trimmed in the circuit of *Figure 2*)

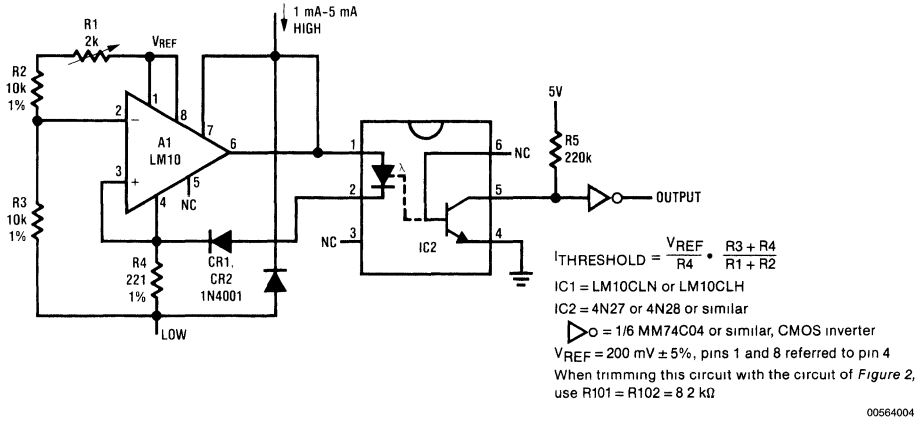
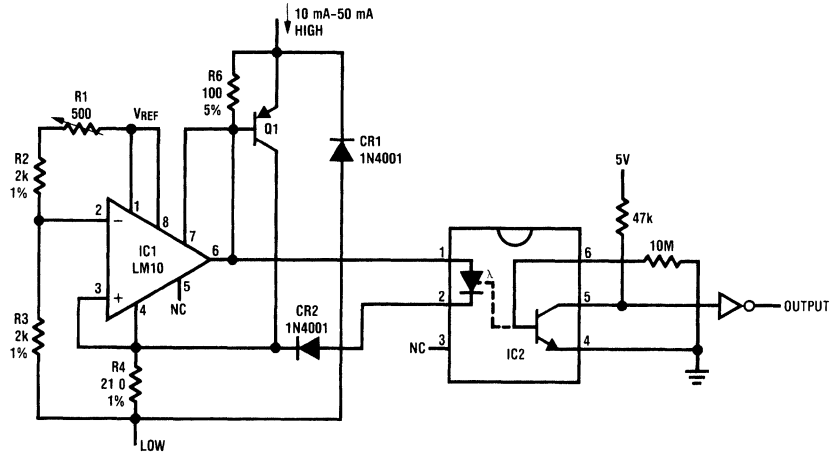


FIGURE 4. Current Loop Fault Detector ($I_{THRESHOLD}$ = 0.85 mA for 1 mA–5 mA Current Loops)



$$-I_{THRESHOLD} = \frac{V_{REF}}{R4} \bullet \frac{R3 + R4}{R1 + R2}$$

IC1 = LM10CLH or LM10CLN op amp and reference

V_{REF} = 200 mV ± 5%, pins 1 and 8 referred to pin 4

IC2 = 4N28 or similar, optoisolator

▷o = 1/6 MM74C04 or similar, CMOS inverter

Q1 = 2N2904 or 2N2907, any silicon PNP

When trimming this circuit with the circuit of *Figure 2*, use R101 = R102 = 820Ω

00564005

FIGURE 5. Current Loop Fault Detector ($I_{THRESHOLD}$ = 8.5 mA, for 10 mA–50 mA Current Loops)

Signal Conditioning for Sophisticated Transducers

National Semiconductor
Application Note 301
Robert A. Pease

A substantial amount of information is available on signal conditioning for common transducers Fortunately, most of these devices, which are used to sense common physical parameters, are relatively easy to signal condition. Further, most transducer-based measurement requirements are well served by standard transducers and signal conditioning techniques.

Some situations, however, require sophisticated transduction techniques with their attendant special signal conditioning requirements This application note details signal conditioning and applications information for a diverse group of sophisticated and unusual tranducers. Because these devices are unusual or somewhat difficult to signal condition, relatively little material has appeared on how to design circuitry for them. Many of these devices permit measurements which cannot be accomplished in any other way. For this reason it is worthwhile to have a basic familiarity with their capabilities and what is required to signal condition them. The circuits shown are intended as instructive examples only, although each one has been constructed and tested. Every individual transducer application has a set of specifications and constraints which will require modification or revision of the circuits presented. Sources of additional information which feature more vigorous treatment are presented in a reference section at the end of the application note.

Photomultiplier Tube (PMT)

Perhaps the most versatile light detector available is the photomultiplier tube (PMT). These sensors allow single photon detection, sub-nanosecond rise time, bandwidths approaching 1 GHz and linearity of response over a range of 10^7. In addition, they feature extremely low noise, stable characteristics and very long life. *Figure 1* details a typical PMT along with a signal conditioning circuit. The tube is composed of a photosensitive cathode, an anode, a focusing electrode and ten dynode stages. In operation, the photocathode, which is high voltage biased with respect to the dynodes, emits photoelectrons when it is struck by light. These are focused into a beam and directed to the first dynode stage by the focus electrode. These arriving electrons impinge on the dynode, causing secondary emission to occur. As a result, a greater number of electrons leave the dynode and are then directed to the second dynode. In this fashion, a number (e.g.,10) of dynode stages are used to achieve overall gains of 10^6 to 10^8. The electrons from the final dynode are collected by the anode, which provides the output current of the tube. In contrast to other vacuum tubes, the PMT does not use a filament to thermionically generate electrons. Instead, the photocathode, in combination with incident light, initiates the electrons. The absence of a filament means there are no degradation, heat or outgassing problems and the life of a PMT is very long.

Signal conditioning involves generating a stable high voltage supply and accomplishing a low noise current-to-voltage conversion at the anode. In this example, a DC-DC converter is used to supply the dynode potentials to the tube. The supply is stabilized by the LF412 amplifier which drives the Q3-Q5 combination to complete a feedback loop around the Q1-Q2 driven transformer The LM329 provides a stable servo reference In general, the regulation of a PMT supply should be at least ten times greater than the required measurement gain stability because of the relationship between a PMT's gain slope and the high voltage applied. The cathode and dynodes are biased from the high voltage supply via divider resistors. The resistors distribute the dynode potentials in proportion to a ratio which is specified for each tube type. To prevent non-linear response, the current through the divider string should be at least ten times the maximum expected current out of the tube. Some high speed pulse applications can generate transient high tube currents which may require the small capacitors shown in dashed lines. The anode is the tube output and appears as an almost ideal current source. The LF412 amplifier performs a current-to-voltage conversion with the 1 MΩ resistor setting the output scale factor.

The PMT's combination of high speed and extreme sensitivity suits it to a variety of difficult light measurement chores. The remarkable photograph of *Figure 2* shows the actual rise and fall time characteristics (inverted) of a fast pulse of light produced by an LED. This photo was taken with a high speed PMT which was terminated directly into a 1 GHz bandwidth, 50Ω sampling oscilloscope.

Another PMT application exchanges speed for sensitivity in a nuclear medical instrument, the Gamma camera.

The Gamma camera operates by using the scintillation properties of special crystals which are placed in front of an array of PMTs. Small quantities of radioactive isotopes are introduced into the patient either by oral ingestion or injection. Specific isotopes collect at certain organs within the body. As the radioactive isotopes decay, gamma rays are emitted from the isotope concentration area. These rays are collimated by a lead plate containing many small holes which forms the front of the camera (*Figure 3*). This collimator allows only those rays which are at right angles to pass through the plate. The rest are absorbed in the lead In this fashion the geometric shape of the gamma source is preserved and is presented to the scintillation crystal. The array of PMTs is located behind the crystal. The individual tubes respond to any given scintillation anywhere in the crystal with a distribution of signal strengths. This distribution is used by a processor to determine the precise point of scintillation in the crystal. Each of these scantillation locations is recorded on a CRT After a length of time, this counting-integration process produces a picture of the organ on the CRT. *Figure 4* shows 7 such pictures of a pair of human lungs, taken 30 seconds apart over a 150 second period In photo A, the administered radioactive isotope begins to collect in the lungs. In photo B, the lungs are saturated. During photos C, D, E, F and G, the isotope progressively decays. Normally, human lungs will clear after 120 seconds. This particular sequence shows evidence of an obstructive pulmonary disease which is most pronounced in the lower right lung.

Photomultiplier Tube (PMT) (Continued)

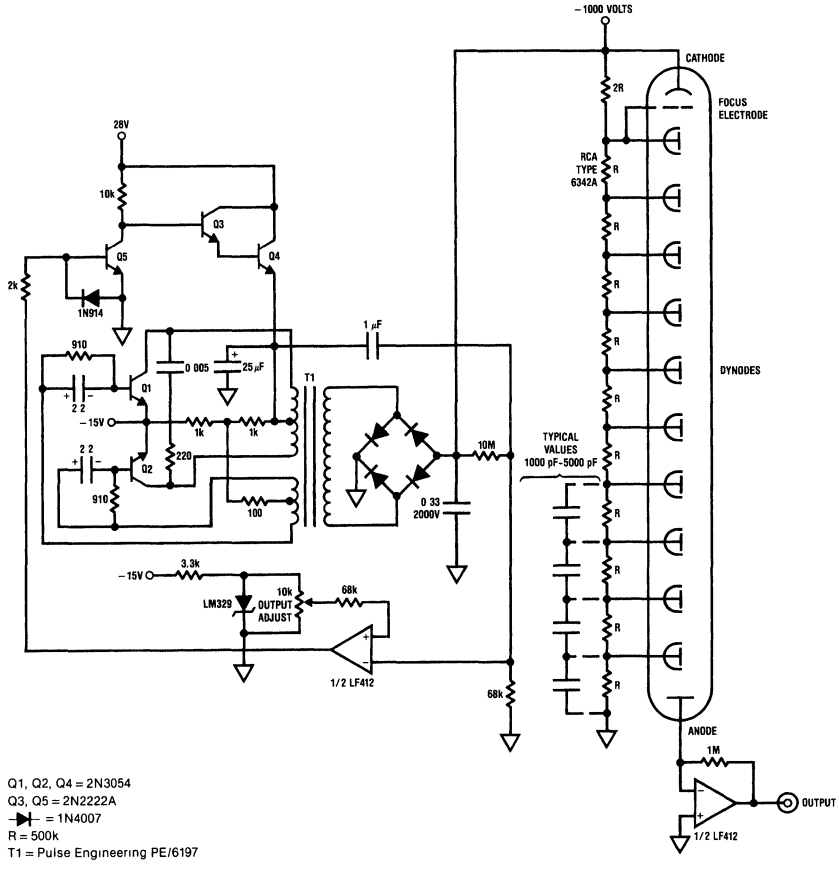


FIGURE 1.

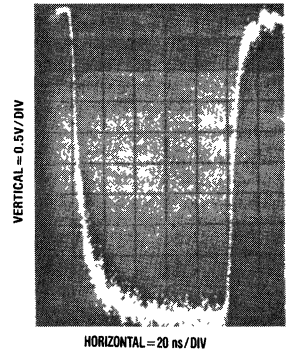


FIGURE 2.

Photomultiplier Tube (PMT)

(Continued)

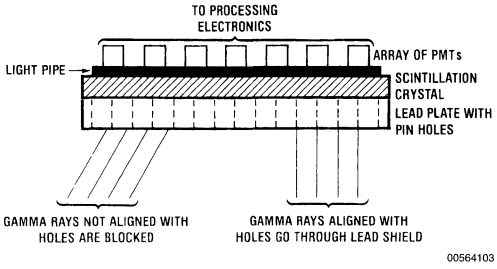


FIGURE 3.

Pyroelectric Detector

The pyroelectric detector represents another class of sophisticated photodetector. These ceramic-based radiation detectors feature an extraordinary light sensitivity range from microwatts to watts with excellent linearity. Their bandwidth is flat from the ultraviolet to the far infrared. Response is sub-nanosecond and the devices may be operated at room temperature; no cooling is required. A major difficulty and source of confusion with signal conditioning pyroelectrics is that they do not respond at DC. This limitation, which is in keeping with all ceramic-based transducers, is surmounted by using a light chopper in front of the detector. In this fashion, DC light inputs to the detector appear as a modulated carrier. These devices are used in industrial temperature measurement, spectroscopy and laser power meters They are also used to measure high speed laser pulse characteristics.

For signal conditioning purposes, pyroelectrics can be modeled as either a current source with parallel capacitance or a voltage source with series capacitance Because there is no resistive component, there is no resistive Johnson noise. *Figure 5a* shows a simple voltage mode set-up which can be used for fast pulses of high energy. In this circuit, the detector is terminated directly into a high speed 50Ω oscilloscope. In *Figure 5b*, a slower detector terminates into 1 MΩ and is unloaded by the LH0052 low bias FET amplifier. For response time much longer than a few milliseconds, the optical chopper provides a modulated light signal to the detector. The amplifier output may be rectified to recover the DC component of the signal. *Figure 5c* shows a current mode signal conditioning circuit. The optical chopper is retained, but the detector is loaded directly into the summing junction of a low bias op amp composed of an LF411 and a pair of sub-picoamp bias FETs. The low bias current allows low energy light measurement.

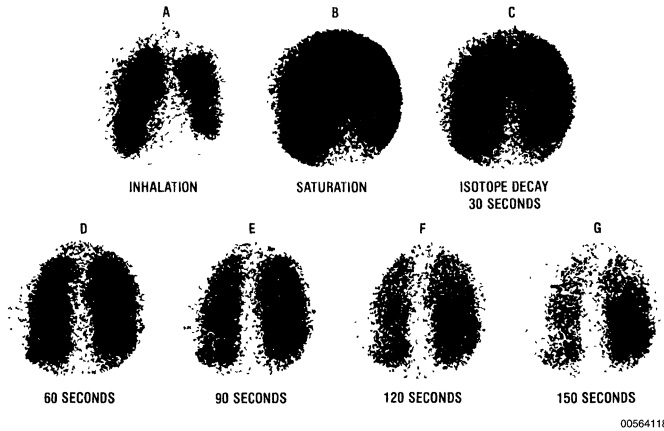
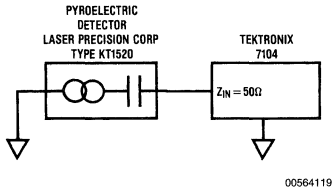
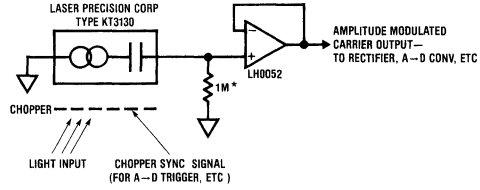


FIGURE 4.

Pyroelectric Detector (Continued)

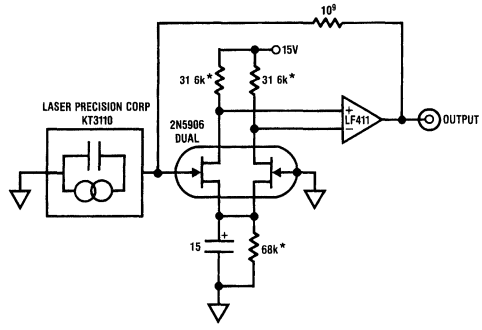


a



*TRW MAR 6 resistor, 1%

b



*TRW MAR 6 resistor, 1%

c

FIGURE 5.

Piezoelectric Ultrasonic Resonators

Piezoelectric ultrasonic tranducers are generically related to pyroelectrics in that they are also ceramic-based. These devices are used for both generation and reception of narrow band ultrasonic information. The characteristic resonance of these transducers, in a similar fashion to quartz crystals, is extremely narrow, allowing high Q, noise rejecting systems to be built around them. As transmitters, they are often driven very hard by steps several hundred volts high at low duty cycles. This permits substantial ultrasonic power to be generated and eases the burden of the receiver in the system (which could be the same transducer as the transmitter). Ultrasonic resonators are used in a wide variety of applications including liquid level detection, intrusion alarms, automatic camera focusing, cardiac ultrasonic profiling (echocardiography) and distance measuring equipment. *Figure 6* shows a signal conditioning circuit which capitalizes on the high Q, noise rejection characteristics and fast response of ultrasonic transducers to accomplish a difficult thermal measurement. This circuit is similar to a type developed to measure high speed temperature shifts in a gas medium.

In contrast to almost all other temperature sensors, it does not rely on its sensing element to come into thermal equality with the measurand. Instead, the relationship between the speed of sound and the temperature of the medium in which the sound is propagating is utilized to determine temperature. The speed of response is therefore very fast and the measurement is also non-invasive. The relationship between the speed of sound in any medium and temperature may be described by equations. As an example, the relationship in dry air is:

$$C = 331.5\sqrt{\frac{T}{273}} \text{ meters/second,}$$

where C = speed of sound.

For any given value of C the absolute temperature is:

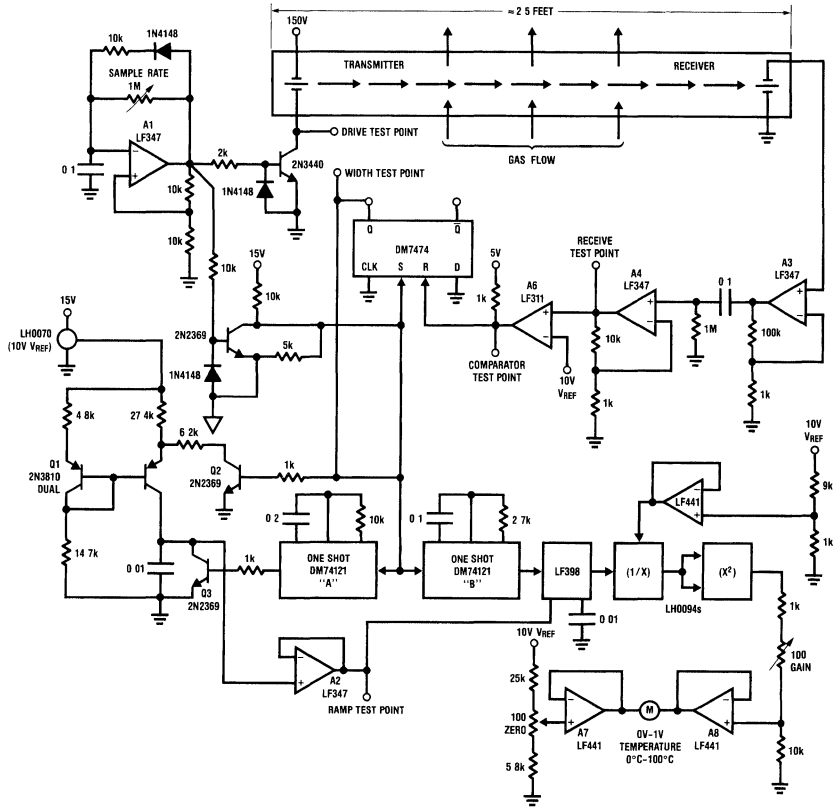
$$T = \frac{273}{(331.5)^2} \times C^2.$$

It is clear that because sound speed and the medium in which it travels have a predictable relationship, a temperature transducer can be composed of the medium itself. If the characteristics of the medium can be defined (e.g., its make up) the transmit time of a sonic pulse through it can be used to determine its temperature. If narrow band ultrasonic transducers are used, they will reject sonic noise that may be occurring in the medium.

Piezoelectric Ultrasonic Resonators (Continued)

A1 periodically generates a short pulse (waveform A, *Figure 7*) that drives the 2N3440 into conduction, forcing the ultrasonic 40 kHz transducer to emit a short burst at its resonant frequency. The 150V pulse amplitude allows substantial ultrasonic energy to be coupled into the medium. As this pulse is generated, the DM7474 flip-flop is set low (waveform C, *Figure 7*). After a length of time, determined by the distance between the ultrasonic transducers and the temperature of the gas, the sonic pulse arrives at the receiving transducer and is amplified by A3 and A4 (A4's output is waveform B, *Figure 7*) This amplified output triggers A6, which resets the flip-flop high. During the time the flip-flop was low, the 2N3810 current source was allowed to charge the 0.01 µF capacitor (waveform D, *Figure 7*). When the flip-flop is reset high, Q2 comes on and the charging ceases. The A2 follower output sits at the capacitor's DC potential, which is related to the sonic transit time in the gas stream. The LF398 sample-hold is triggered by the "B" DM74121 one shot and samples A2's output. The LF398's output feeds two LH0094 multi-function non-linear converters which are arranged to linearize the speed of sound versus temperature relationship. The output of this configuration is the gas temperature which is displayed on the meter. Gain and zero trims are provided via the A7 and A8 networks When A1 issues another pulse, the DM74121 "A" one shot resets the 0.01 µF capacitor to 0V and the entire process repeats.

It is worth noting that no bandwidth limiting of any kind is employed at the A3-A4 receiver despite their compound gain of 1000. This would seem to invite noise sensitivity problems in a sonic system, but the high Q ultrasonic transducer provides almost ideal noise rejection *Figure 8* shows the amplified output of the received pulse superimposed on the output of a boardband microphone placed in the sonic path. Boardband noise 100 dB greater than the 40 kHz pulse is pumped into the sonic path. Virtually complete noise rejection occurs and signal integrity is maintained.



Ultrasonic transducers = Massa MK-109

FIGURE 6.

Piezoelectric Ultrasonic Resonators (Continued)

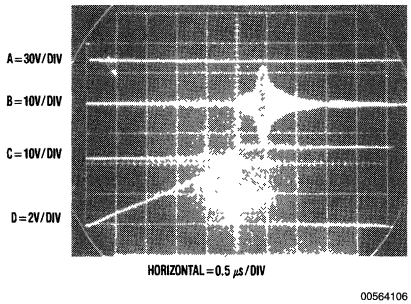


FIGURE 7.

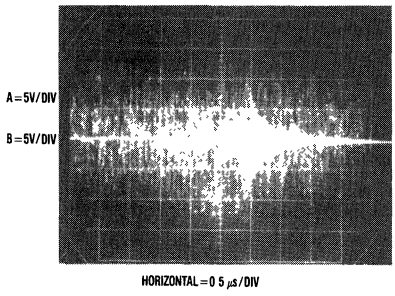


FIGURE 8.

Piezoelectric Accelerometer

Another piezoelectric-based transducer is the piezoelectric accelerometer. These devices utilize the property of certain ceramic materials to produce charge when subject to mechanical excitation. These accelerometers use a mass coupled to the piezoelectric element to generate a force on the element in response to an acceleration's frequency and amplitude. Calibration and sensitivity can be varied by selecting the piezoelectric materal and altering the configuration and amount of the mass. The best way to signal condition these devices is to employ an amplifier configuration that is directly sensitive to their charge-type output. Charge amplifiers use low bias current op amps with capacitive feedback. Output voltage will depend upon the charge out of the accelerometer which is related to the applied acceleration.

In *Figure 9*, the transducer looks directly into the ground potential summing junction of an op amp. Because of this, there is no voltage difference between the interconnecting cable center conductor and its shield. This eliminates cable capacitance effects on the transducer output and allows long cable runs. It is advisable to use cable specified for low triboelectric charge effects for best performance, although this is usually only a factor with relatively low output devices. The $10^{11}\Omega$ resistor provides a DC feedback path, while the variable capacitor sets the sensitivity of the charge-to-voltage conversion. When the accelerometer shown is mounted on a hand-held voltmeter and dropped on the floor, the instantaneous acceleration to which the voltmeter is subjected can be determined. In *Figure 10*, the stored trace display shows an instantaneous force of almost 1000G with smaller forces generated as the voltmeter bounces 3 times over 60 ms. (It is recommended that this experiment be performed with a borrowed voltmeter.)

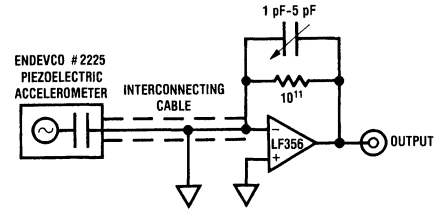


FIGURE 9.

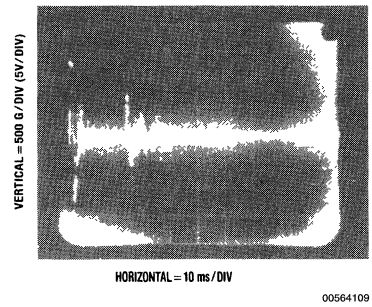


FIGURE 10.

Linear Variable Differential Transformer (LVDT)

The linear variable differential transformer (LVDT) offers zero-friction position sensing with good precision. Although potentiometers are easy to signal condition and allow high precision they cannot match the nearly infinite life and zero-friction of the LVDT approach. LVDTs are available in both rotary and stroke mechanical configurations. The LVDT is basically a transformer (*Figure 11*) with a movable core. The primary is driven with a sine wave which is usually amplitude stabilized. The two matched secondaries are connected in series-opposed fashion. When the movable core is positioned in the magnetic (and usually geometric) center of the transformer, the secondaries' outputs cancel and no net secondary voltage appears. This is called the null position.

Linear Variable Differential Transformer (LVDT) (Continued)

As the core is moved from null, the differential in flux coupled to the two secondaries produces a net voltage difference across them.

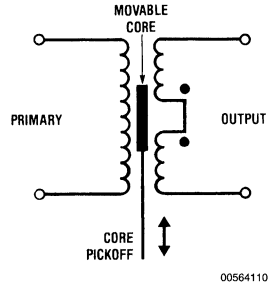


FIGURE 11.

This is the output of transducer. Good transducer performance (e.g., null cancellation characteristics, linearity, etc.) requires manufacturer attention to winding techniques, magnetic shielding, material choices and other issues. Rectifying and filtering the output signal will yield only amplitude information. Optimum signal conditioning requires a phase sensitive demodulation scheme. This gives the amplitude and also polarity information necessary to determine on which side of null the LVDT core is.

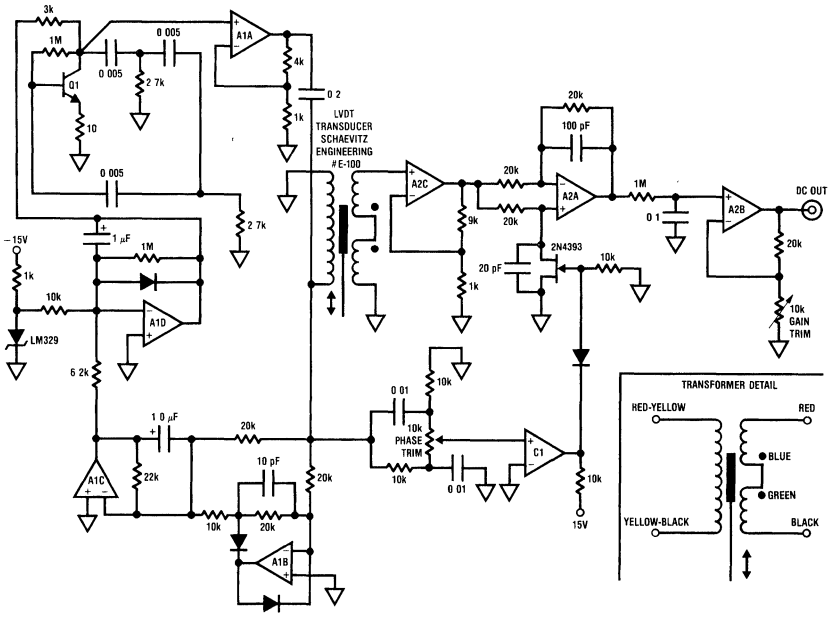
Figure 12 shows a circuit which does this. Waveforms of operation are given in *Figure 13*. In this circuit, Q1 and its associated components from a phase shift oscillator which runs at 2.5 kHz, the manufacturer's specified transducer operating frequency. A1A amplifies and buffers Q1's output and drives the LVDT (waveform A, *Figure 13*). Since the transducer's output will vary with drive level, feedback is used to stabilize the 2.5 kHz amplitude. A1C and A1D full wave rectify a sample of the drive waveform. A1C's filtered output is applied to A1D, a servo amplifier. A1D compares A1C's output to the LM329 reference and drives the Q1 oscillator to complete an amplitude stabilization loop. The LVDT's output is amplified by A2C and fed to A2A. A2A is a unity gain ampilifer whose sign alternates between "+" and "–". Synchronous switching for A2A comes from C1 (waveform B, *Figure 13*), which is driven by the modulation sine wave output via a phase shift network. The phase trim network compensates phase shift in the LVDT and ensures that C1 switches at the zero crossings relative to A2A's output. When C1's output is low, the 2N4393 FET is off and A2A's positive input (waveform C, *Figure 13*) receives signal. When the sine wave reverses polarity, C1's output goes high, turning on the FET, which grounds A2A's "+" input. Under these conditions A2A is always switching its amplification's sign from "+" to "–" in synchronism with the sine wave output from the LVDT. A2A's phase sensitive output, in this case positive, appears in trace D, *Figure 13*. A2B provides a scaled and filtered DC output. To trim the circuit, set the LVDT to at least ½ physical displacement and adjust the phase trim for maximum output indication. Next, adjust the gain trim for the desired circuit output at full-scale LVDT displacement.

Force-Balanced Pendulous Accelerometer

The operating principles of the LVDT are applied in the force-balanced pendulous accelerometer. Transducers of this type feature wide dynamic range, high linearity and very high accuracy. *Figure 14* shows one form of a conceptual force-balanced pendulous accelerometer. The device operates by using an LVDT-type pick-off to determine the position of the pendulum. The DC output of the LVDT is fed to a servo amplifier which drives the torque coil. The magnetic output of the torque coil completes a servo loop around the pendulum, forcing it to become immobile. Because the torque coil's field can attract only the pendulum, a second bias coil provides a steady force for the torque coil to work against. When an input acceleration occurs along the sensitive axis, the servo applies the necessary current to the torque coil to keep the pendulum from moving. The amount of current required is directly proportional to the value of the input acceleration. Because the pendulum never moves, transducer linearity and accuracy can be very high. In addition, wide dynamic range is possible. Force-balanced accelerometers are widely applied in aircraft inertial guidance systems, aerospace applications, seismic monitoring, shock and vibration studies, oil drilling platform stabilization and similar applications. In recent years these accelerometers have become available in complete signal conditioned packages, although there are a number of applications where it is desirable to independently signal condition the transducer. *Figure 15* shows a detailed schematic of such signal conditioning. The pick-off circuitry is similar to the LVDT shown in *Figure 12* and does not require further comment. The bias coil is driven by the LH0002 boosted LF347 (A1A) which is in a current sensing feedback configuration. For the accelerometer shown, the manufacturer specifies

60 mA of bias coil current. Torque pulses are applied by servo amplifier A3B, which is biased from the LVDT demodulator output. The output of the circuit is taken across the 100Ω resistor in series with the torque coil. Servo gain is set at A3B while damping for the loop is provided by the 1 µF unit in A3B's feedback loop. In addition, accelerometer damping is controlled by stabilizing the temperature of the mechanical assembly. This is accomplished by A3C, which is set up as a simple on-off temperature controller. The interior of the accelerometer is filled at manufacture with a liquid whose viscosity provides appropriate damping characteristics at a specified temperature, in this case 180°F. Accelerometers of this type routinely yield 100ppm accuracy from ranges of 20 mG to 100G.

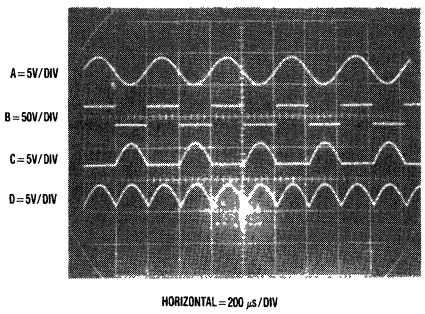
Force-Balanced Pendulous Accelerometer (Continued)



00564125

= N914 = N914
A1 = LF347
A2 = LF347
C1 = LM311
Q1 = 2N2222

FIGURE 12.



00564112

FIGURE 13.

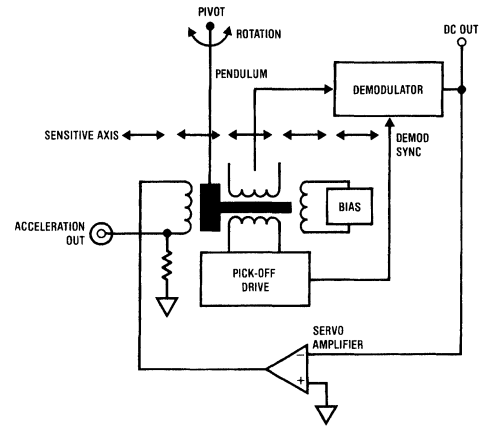


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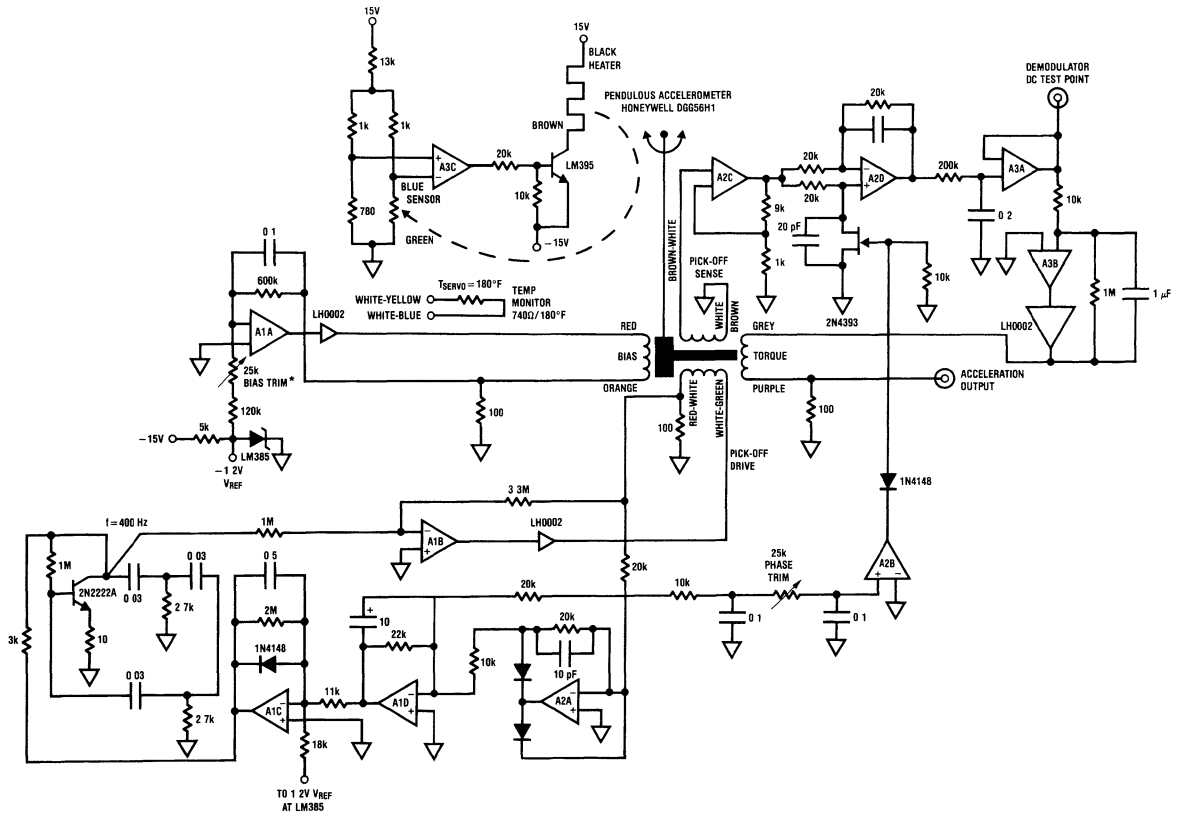
FIGURE 14.

Force-Balanced Pendulous Accelerometer (Continued)



00564113

*Adjust to 60 mA bias loop current

A1, A2, A3 = LF347

FIGURE 15.

Rate Gyro

The rate gyro is another form of high performance inertial measuring transducer. It consists of an electrically driven gyroscope with a captive spin axis. Normal gyros are free of restraint and maintain position when moved. The rate gyro is held captive and forced to move with the physical input. By measuring the force generated as the gyro opposes its restraining mechanism, rate-of-angle change information can be deduced. *Figure 16* shows signal conditioning for a typical rate gyro. An LVDT-type pick-off is used and synchronous demodulation-type circuitry very similar to *Figure 15* is employed. Note the high voltage drive to the gyro motor (26 Vrms) supplied by the boosted LM143. Because of their long life and high precision rate, gyros are frequently employed in inertial guidance systems, drilling platform stabilization systems and other critical applications.

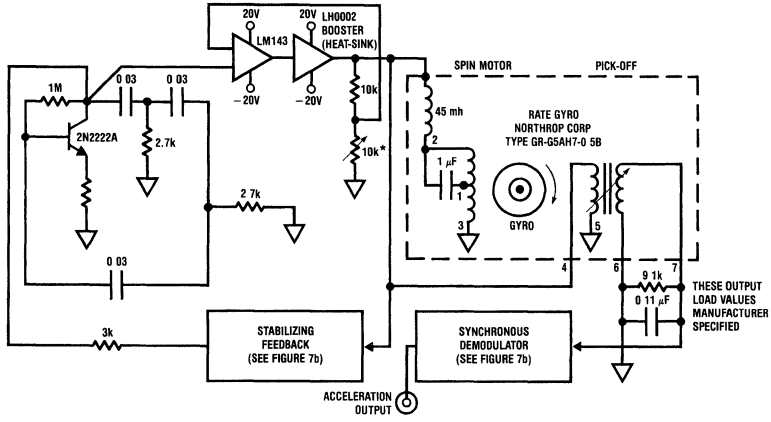
Flux Gate

A flux gate transducer converts an external magnetic field (such as that of the earth's) into an electric output. A variety of flux gate configurations exist, the simplest being a piece of easily saturable ferrous material wrapped around a cylinder (*Figure 17*). An alternating current is passed along the axis of the cylinder which periodically saturates the material, first clockwise and then counter-clockwise.

A pick-up winding is wrapped around the cylinder. While the ferrous material is between saturation extremes, it maintains a certain average permeability. While in saturation, this permeability (μ = dB/dH) becomes one (an increase in driving field H produces the same increase in flux B). If there is no component of magnetic field along the axis of the cylinder, the flux change seen by the pick-up winding is zero since the excitation flux is normal to the axis of the winding. If, on the other hand, a field component is present along the cylindrical axis, then each time the ferrous material goes from one saturation extreme to the other it produces a pulse output on the signal pick-up winding that is proportional to the external magnetic field and the average permeability of the material. Since this saturation-to-saturation transition occurs twice each excitation period (fundamental), the frequency of signal out of the pick-up windings is twice the excitation frequency.

These transducers find use in metal detectors, submarine locating gear, electronic compasses, oil surveys, and other areas where measurement of the strength or locally caused disturbance of the earth's magnetic field is of interest. Flux gate transducers are capable of measuring variations in the earth's magnetic field within one gamma (10^{-5} oersteds). Two axis flux gates can be used to construct an electronic compass. More recent flux gate design employs a core-shaped transducer, which is essentially two cylinder types bent together at the ends to form a closed magnetic path. This permits lower driving power and allows the use of commercially available tape-wound cores to be used to construct the transducer. A simple flux gate and its signal conditioning appears in *Figure 18*. Excitation to the flux gate is provided by the complementary signal output from the CD4047s. The transistor drives a transformer which is tuned for resonance. This converts the square wave output of the CMOS oscillator into a sinusoidal waveform. This sinusoidal excitation voltage is then converted by the transformer into a high level AC drive current at the excitation frequency which is used to drive the sensor.

The output of the sensor signal winding is an AC signal at twice the excitation frequency and is directly proportional in amplitude to the external axial magnetic field. This second-harmonic of the excitation frequency is then phase detected with a circuit similar to the demodulators shown in *Figures 12, 15*. A portion of the DC output signal may be fed back (shown in dashed lines) to the signal winding to provide a closed loop negative feedback system. This feedback signal produces a field in the sensor which opposes the signal being measured. The high forward gain of the signal channel along with the closed loop negative feedback system ensure good stability and linearity of the output signal.



*Adjust for 26 Vrms output

FIGURE 16.

Flux Gate (Continued)

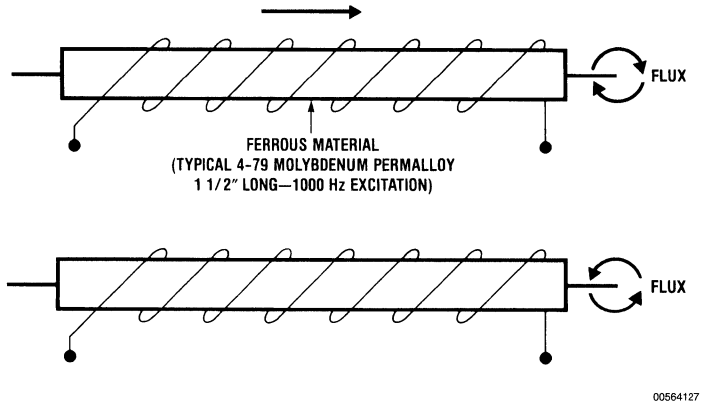


FIGURE 17.

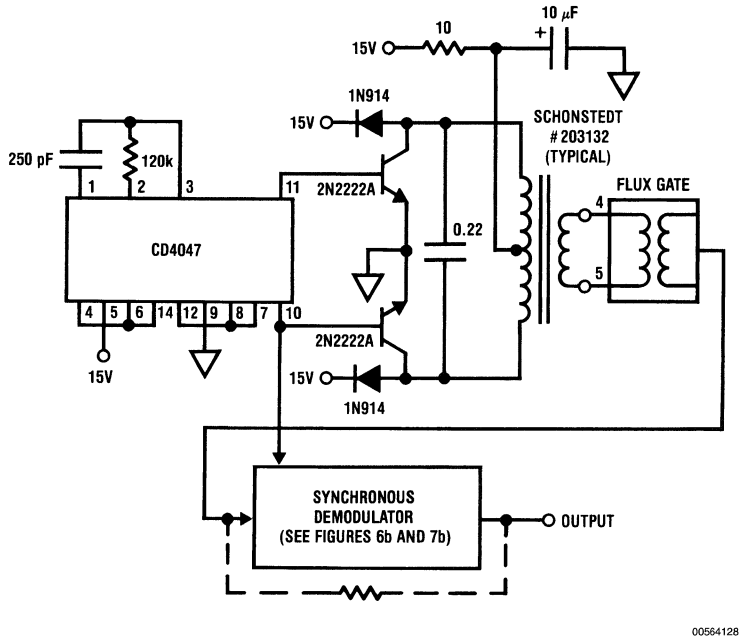


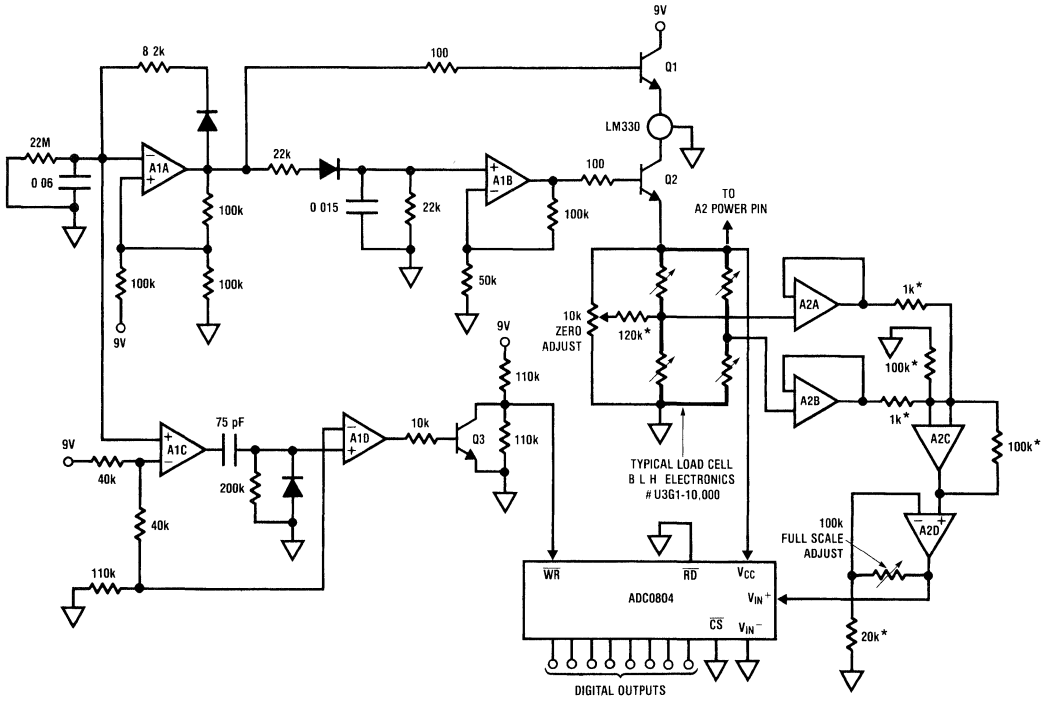
FIGURE 18.

Low Power Strain Gauge Bridge Signal Conditioning

In most cases, strain gauge bridges do not require unusual signal conditioning techniques. When low power consumption is necessary, special circuitry must be employed to eliminate the high current consumption of strain gauge-based transducers. Normally, the 350Ω input impedance of these devices requires substantial drive to achieve a usable output. For a typical 10V drive level, 35 mA are required; hardly compatible with low power or battery operation. The circuit shown in *Figure 19* provides complete signal conditioning for strain gauge transducers while using only 1.8 mA average current out of a 9V transistor radio battery. The output of the circuit is an 8-bit word produced by an A-D converter. The key to achieving low power operation is to pulse power at low duty cycles to the transducer and its signal conditioning circuitry. In *Figure 20*, A1A oscillates at

Low Power Strain Gauge Bridge Signal Conditioning (Continued)

about 1 Hz. Each time A1A's output goes high (waveform A, *Figure 20*), Q1 comes on, turning on the LM330 5V regulator. This places 5V at Q2's collector. Concurrently, A1B amplifies the output of the pulse-edge shaping network at its input and provides voltage overdrive to emitter-follower Q2, forcing it into saturation. This causes an edge shaped pulse to be applied to the strain gauge bridge (waveform B, *Figure 20*). This pulse is also used to power A2 and the ADC0804 A-D converter. The slow edge shaping limits the DV/DT seen by the transducer as it is pulsed. This eliminates possible deleterious effects on transducer performance over time, due to the continuous abrupt step functions being applied. The transducer bridge output is monitored by the A2 quad, which serves as a differential input (A2A and A2B), single-ended output (A2C and A2D) amplifier. A2D's output (waveform C, *Figure 20*) feeds the ADC0804 A-D converter. The A-D is triggered by a delayed pulse generated by the A1C and A1D pair (waveform D, *Figure 20*). This pulse is positioned so that it occurs after A2D's output has settled to final value. To calibrate the circuit, apply zero physical load to the transducer shown and adjust the zero trim so the A-D converter is just below indicating 1 LSB output. Next, apply (or electrically simulate) 10,000 lbs. and adjust the gain trim for a full output code at the A-D converter.



* 1% metal film resistor
A1, A2 = LM324 quad
Q1, Q2, Q3 = 2N2222A
= 1N4148

00564116

FIGURE 19.

Low Power Strain Gauge Bridge Signal Conditioning (Continued)

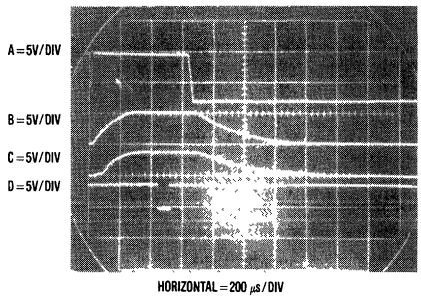


FIGURE 20.

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Short Form Catalog; ENDEVCO Corporation; San Juan Capistrano, CA

Bulletin 31, MK109 Ultrasonic Transducer; Massa Corporation; Hungham, MA

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Laser Precision Corporation

Schonstedt Instrument Company

Schaevitz Engineering Company

Northrop Corporation, Precision Products Division

RCA Electro-Optics Division

Lancaster Radiology Associates

Theory and Applications of Logarithmic Amplifiers

National Semiconductor
Application Note 311
Robert A. Pease

A number of instrumentation applications can benefit from the use of logarithmic or exponential signal processing techniques. The design and use of logarithmic/exponential circuits are often associated with involved temperature compensation requirements and difficult to stabilize feedback loops. For these considerations and others, designers tend to avoid these circuits. Hybrid and modular logarithmic/exponential devices are available commercially, but are quite expensive and earn very high profits for their manufacturers.

The theory and construction of these circuits are actually readily understood. *Figure 1* shows an amplifier which provides a logarithmic output for a linear input current or voltage. For input currents, the circuit will maintain 1% logarithmic conformity over almost 6 decades of operation. This circuit is based, as are most logarithmic circuits, on the inherent logarithmic relationship between collector current and V_{BE} in bipolar transistors. Q1A functions as the logging transistor in this circuit and is enclosed within A1A's feedback loop, which includes the 15.7 kΩ-1 kΩ divider. The circuit's input will force A1A's output to achieve whatever value is required to maintain its summing junction at zero potential. Because Q1A's response is dictated by the logarithmic relationship between collector current and V_{BE}, the output of A1A will be the logarithm of the circuit input. A1B and Q1B provide compensation for Q1A's V_{BE} temperature dependence. A1B servos Q1B's collector current to equal the 10 µA current established by the LM329 reference diode and the 700 kΩ resistor. Since Q1B's collector current cannot vary, its V_{BE} is also fixed. Under these conditions only Q1A's V_{BE} will be affected by the circuit's input. The circuit's output is a function of:

$$E_{OUT} = \frac{15.7k + 1k}{1k}(V_{BE}Q1B - V_{BE}Q1A)$$

For Q1A and Q1B operating at different collector currents, the V_{BE} difference is:

$$\Delta V_{BE} = \frac{KT}{q} \log_e \frac{I_{CQ1A}}{I_{CQ1B}}$$

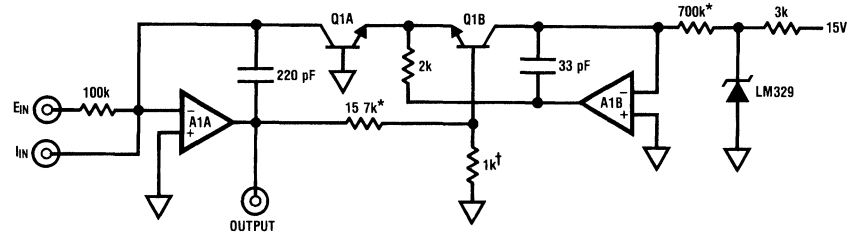
where K=Boltzmann's constant
T=temperature °K
q=charge of an electron.

If both equations are combined, the circuit output for a voltage input is:

$$E_{OUT} = \frac{-KT}{q} \frac{15.7k + 1k}{1k} \log_e \frac{E_{IN} \bullet 700k}{6.9V \bullet 100k}$$

where 6.9V=V_Z of LM329
100k=input resistor
$E_{IN} \geq 0$.

This confirms that the circuit output voltage is logarithmically related to the circuit's input. Without some form of compensation, the scale factor will change with temperature. The simplest way to avoid this is to have the 1 kΩ value vary with temperature. For the device shown, compensation is within 1% over −25°C to +100°C. The circuit's gain is set by the 15.7 kΩ-1 kΩ divider to a factor of 1V/decade.



*1% film resistor
†1 kΩ (±1%) at 25°C, +3500 ppm/°C
Available from Vishay Ultronix,
Grand Junction, CO, Q81 Series
A1A, A1B = LF412 dual
Q1A, Q1B = LM394 dual

FIGURE 1.

This circuit may be easily turned around to generate exponentials. In *Figure 2*, Q1A is driven from the input via the 15.7 kΩ divider. Q1B's collector current varies exponentially with its V_{BE}, and A1B provides a voltage output representation of this action.

These circuits are easy to construct and use if a few considerations are kept in mind. Because of the V_{BE} and scale factor temperature dependences, it is important that Q1A, Q1B and the 1 kΩ resistor be kept at the same temperature. Since Q1 is a dual monolithic device, both halves will track. The resistor should be mounted as closely as possible to Q1, and these components should be kept away from air currents or drafts The KT/q factor for which the resistor compensates varies at about 0.3%/°C, so a few degrees difference between Q1 and the resistor will introduce significant error.

Once the theory and construction techniques are understood, the circuits can be applied. *Figure 3* shows a way to achieve very precise control of a rotary pump, used to feed a biochemical fermentation process. In this example, the exponentiator, composed of Q1 and A1A, is driven from input amplifier A1D. Q1B's collector current, instead of biasing a voltage output amplifier as in *Figure 2*, pulls current from the A1B integrator which ramps up (trace A, *Figure 4*) until it is reset by level triggered A1C (A1C output is trace B, *Figure 4*). The 100 pF capacitor provides AC positive feedback to A3C's "+" input (trace C, *Figure 4*). The magnitude of the current that Q1B's collector pulls from A1B's summing junction will set the frequency of operation of this oscillator. Note that the operation of the exponentiator is similar to the basic circuit in *Figure 3* because A1B's summing junction is always at virtual ground. A1C's output drives the MM74C76 flip-flop to bias the output transistors with 4-phase drive for a stepper motor which runs the pump head. In practice, the exponentiator allows very fine and predictable control for very slow pump rates (e.g., 0.1 rpm-10 rpm of the stepper motor), aiding tight feedback control of the fermentation process. When high pump rates are required, such as during process start-up or when a wide feedback control error exists, the exponentiator can be voltage directed to the top of its range. To calibrate the circuit, ground V_{IN} and adjust the 0.1 Hz trim until oscillation just ceases. Next, apply 7.5V at V_{IN} and adjust the 600 Hz trim for 600 Hz output frequency. *Figure 5* shows a circuit similar to *Figure 3*, except that a more accurate V-F converter is used. This circuit is intended for laboratory and audio studio applications requiring an oscillator whose frequency changes exponentially with an applied input sweep voltage. Applications include swept distortion measurements (where this circuit's output is used to drive a sine coded ROM-DAC combination or analog shaper) and music synthesizers. The V-F converter employed allows better than 0.15% total conformity over a range of 10 Hz-30 kHz. The voltage reference used to drive A1A's input resistor is derived from the LM331A's internal reference and is scaled by A1B, which also biases the zero trim setting. The DM74C74 provides a square wave output for applications requiring a waveform with substantial fundamental frequency content. The 0.15% conformity performance achieved by this circuit will meet almost any synthesizer or swept distortion measurement and the scale factor may be easily varied. To trim, apply OV to the input and adjust zero until oscillation (typically 2 Hz-3 Hz) just starts. Next, apply −8V and adjust the 5k unit for an output frequency of 30 kHz. For the values given, the K factor of the exponentiator will yield a precise doubling in frequency for each volt of input (e.g., 1V in per octave out).

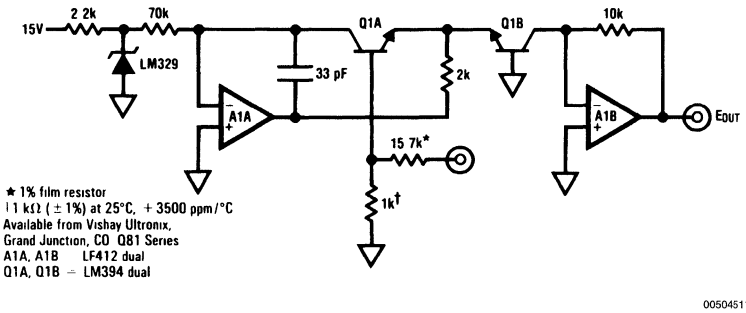


FIGURE 2.

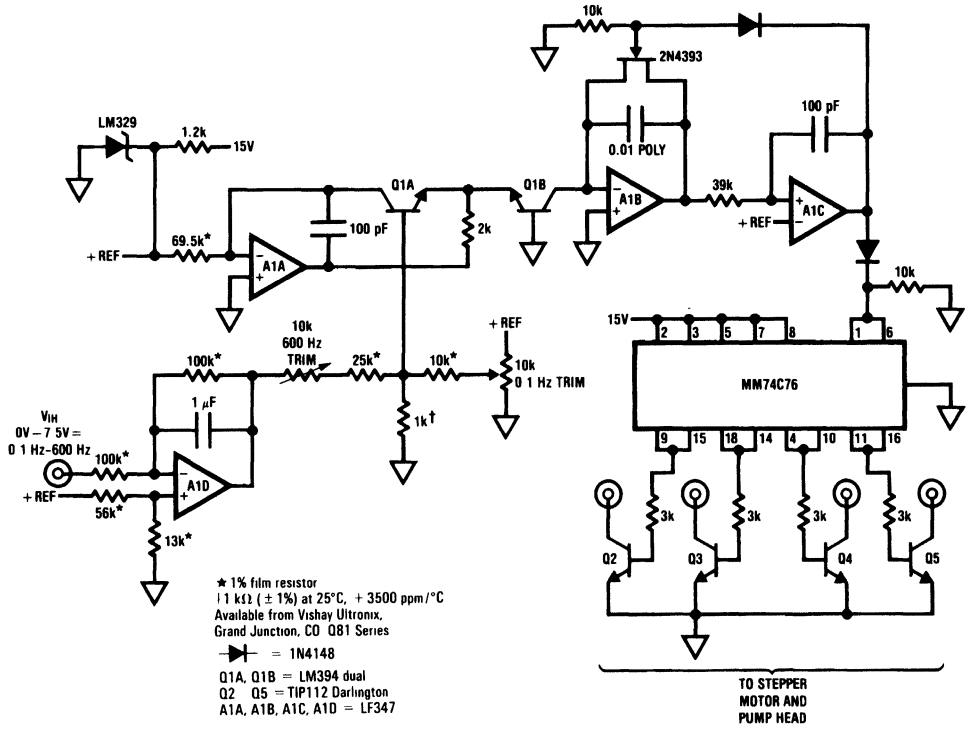


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FIGURE 3.

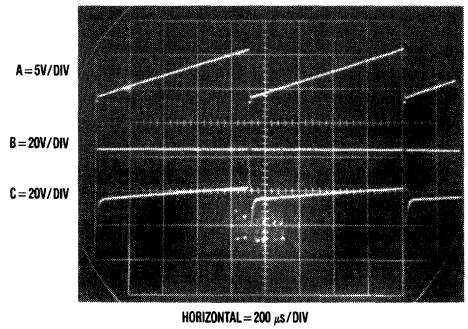

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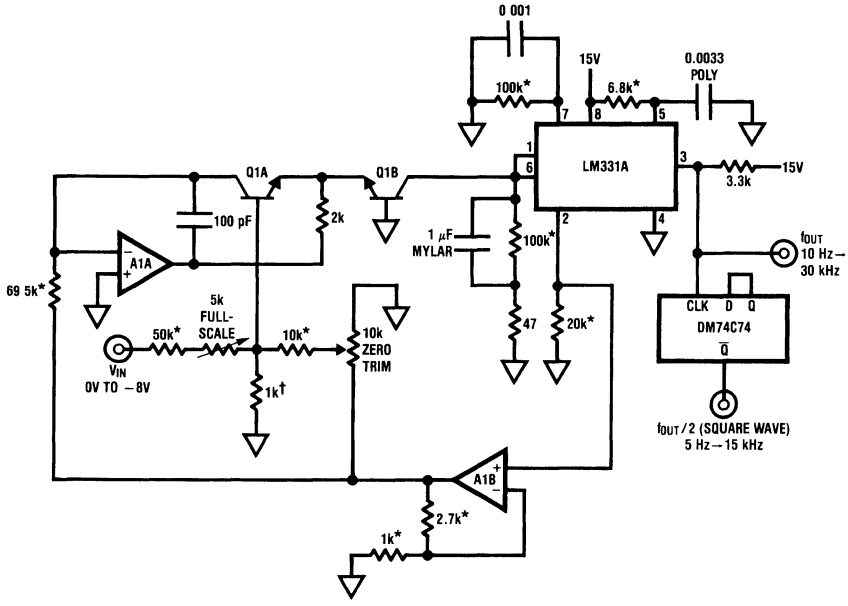
FIGURE 4.



*1% film resistor

†1 kΩ (±1%) at 25°C, +3500 ppm/°C
Available from Vishay Ultronix,
Grand Junction, CO, Q81 Series

A1A, A1B = LF412 dual

Q1A, Q1B = LM394 dual

FIGURE 5.

Figure 6 shows a way to use the exponentiator circuit in a non-invasive, high reliability gas gauge which was designed for use in irrigation pump arrangements in remote locations. The application calls for a highly reliable gas gauge to be retrofitted to large fuel tanks which supply pump motors. It is desirable to run the gas tanks down as closely to empty as possible to eliminate condensation build-up without running out of fuel. This acoustically-based scheme operates by bouncing an ultrasonic pulse off the liquid level surface and using the elapsed time to determine the fuel remaining. This time is converted to a voltage, which is exponentiated to provide a readout with high resolution for nearly empty tanks. The 60 Hz derived clock pulse (trace A, *Figure 7*) drives the transistor pair to bias the ultrasonic transducer with a 100V pulse. Concurrently, the DM74C74 flip-flop is set high (trace C, *Figure 7*) and the DM74C221 one-shot (trace D, *Figure 7*) is used to disable the output of the receiver amplifier. The acoustic pulse bounces off the gasoline's surface and returns to the transducer. By this time, the disable pulse has gone low and the A1A, A1B, A1C and C1 receiver responds (trace B, *Figure 7*) to the transducer's output. C1's output resets the flip-flop low via the DM74C04 inverter. The width of the 60 Hz flip-flop output pulse represents the transit time and the fuel remaining. This width is voltage clamped and integrated at A1D, whose output drives the exponentiator. The 1V/decade scale factor of the exponentiator means that the last 20% of the meter scale corresponds to a tank with only 2% fuel remaining. The first 10% of the meter indicates 80% of the tank's capacity.

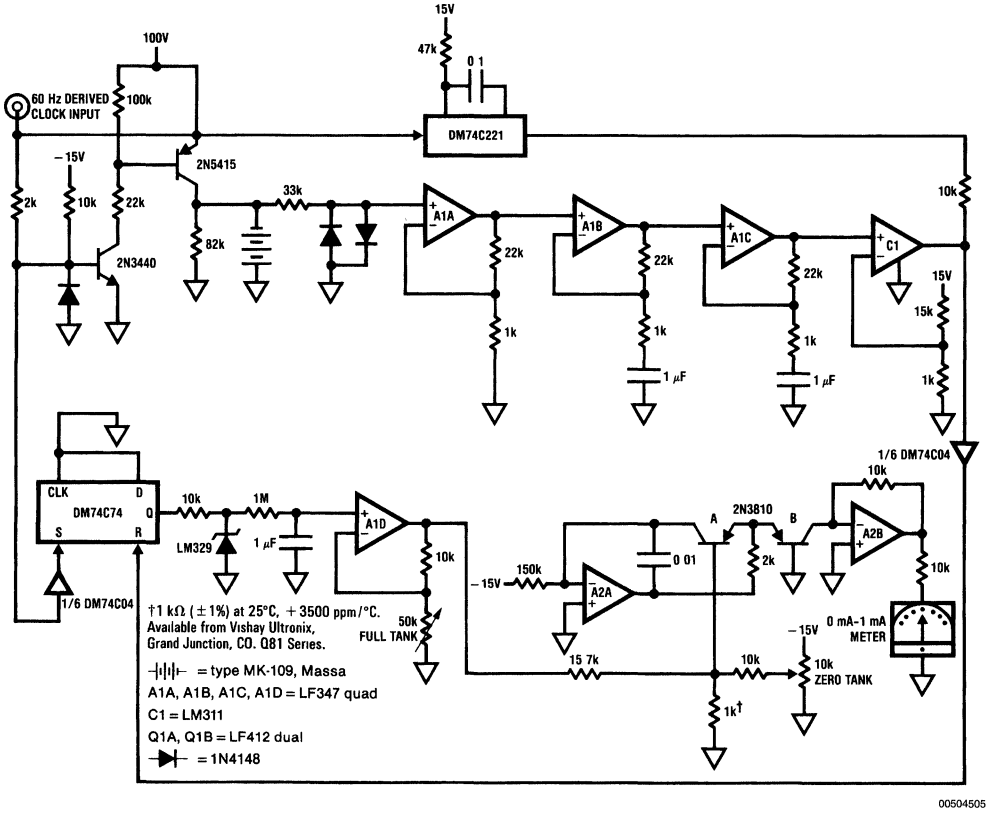


FIGURE 6.

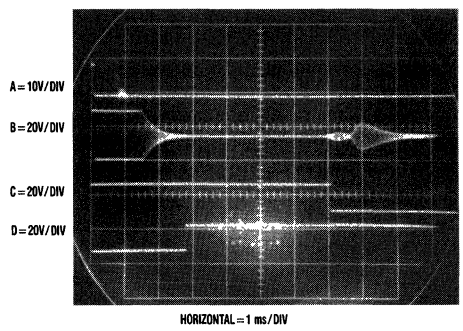


FIGURE 7.

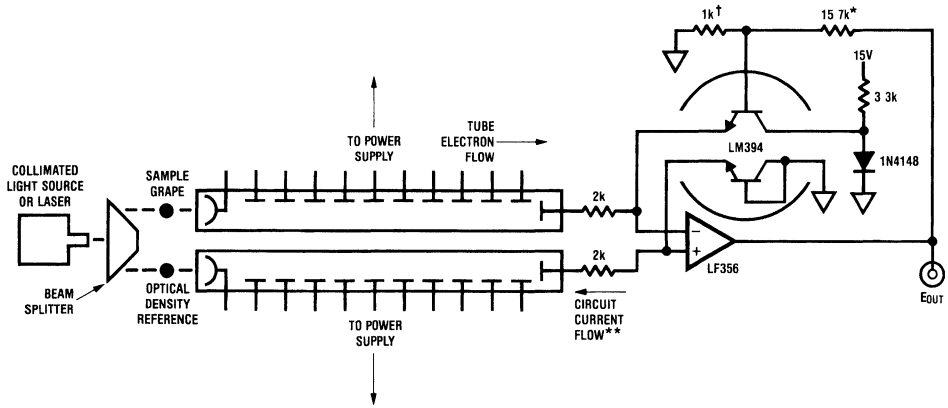
The last application determines density by using photometry. In this arrangement, a light source is optically split (*Figure 8*) and the resultant two beams drive light through a sample and an optical density reference. In this case, the optical sample is a grape, and the photometric set-up is used to correlate the optical density of the grape with its ripeness. Two photomultiplier tubes detect the light passed by the sample and the reference. The ratio of the photomultiplier outputs, which may vary over a wide range, is dependent upon the optical density difference of the sample and the reference. The tubes' output feed a log *ratio* amplifier. This configuration dispenses with the fixed current reference nor-

mally employed, and substitutes the output of the reference channel photomultiplier. In this fashion, the log amplifier's output represents the ratio between the densities of the sample and reference channels over a wide dynamic range. Variations in the light source intensity have no effect. Strictly speaking, the LF356 inputs are not at virtual ground, and an imperfect current-to-voltage conversion should result. In fact, the output impedance of the photomultipliers is so high that errors are minimal. The most significant log conformance error source in this simple log circuit is the fact that the transistor's collectors are at slightly different potentials. For the application shown, this uncertainty is not significant.

References

Non-Linear Circuits Handbook; Analog Devices, Inc.

Logarithmic Converters, Application Note AN-30;
R. C. Dobkin; National Semiconductor Corporation.



00504507

*1% film resistor†1 kΩ (±1%) at 25˚C, +3500 ppm/˚C
Available from Vishay Ultronix,
Grand Junction, CO, Q81 Series
**≈ 10 µA nominal but may vary from
10^{-4}A to 10^{-9}A

FIGURE 8.

Unlimited Capacitive Load Drive Op Amp Takes Guess Work Out of Design

National Semiconductor
Application Note 1245
Hooman Hashemi

Whether or not an Op Amp circuit is capable of driving a capacitive load successfully, depends on several factors:

1. Op Amp internal architecture (e.g. R_{OUT}, Phase Margin, Compensation, etc.)
2. Closed loop gain and output loading
3. Load capacitance value

Driving a capacitor also entails the Op Amp's output current capability since changing the voltage across a capacitor requires an adequate supply of current from the Op Amp. This article will present a lab method to measure amplifier stability under closed loop condition. In addition, a new Op Amp architecture will be presented that would ease this class of applications by using an internal mechanism to improve stability.

Closed Loop Phase Margin Measurement

One of the internal Op Amp parameters which effects cap load drive performance is R_{OUT}, output impedance. In fact, an ideal Op Amp with zero output impedance will be able to drive "any" capacitance with no Phase Margin degradation. However, in reality, for almost all cases, R_{OUT} cannot be ignored. By using a Network Analyzer (HP4195A or equivalent) and the circuit shown in *Figure 1*, it is possible to measure closed loop performance under capacitive loading:

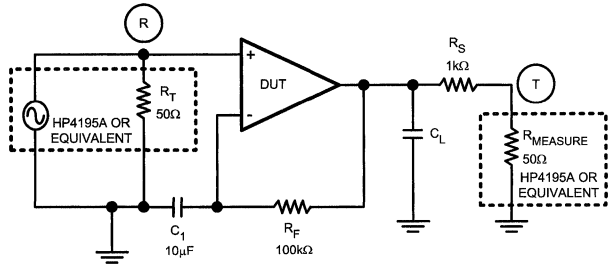


FIGURE 1. Circuit to Measure PM Under Capacitive Loading

The DUT (device under test) will operate under closed loop DC and open loop AC conditions. Therefore, the measured results will be a true representation of Loop Gain including the effect of CL. The resultant T/R measurement (magnitude and phase) will aid in determining the PM for a given CL. One such plot done for LM8272, unlimited capacitance load drive Op Amp, is shown in *Figure 2*:

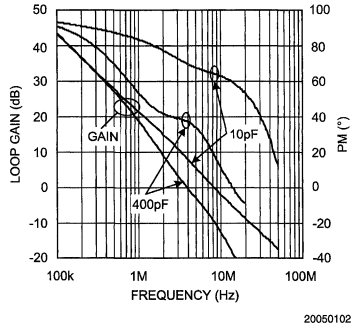


FIGURE 2. LM8272 Loop Gain vs. Frequency

This plot has been corrected for 26dB gain loss through R_S and the RHS axis is made to read Phase Margin directly. In fact, with the LM8272, the PM stays positive for any and all capacitors, as can be seen from *Figure 3* plot below:

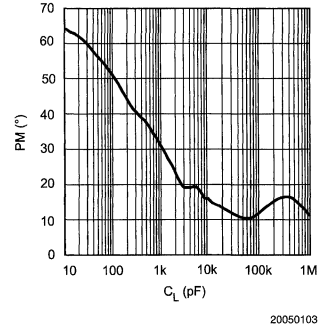


FIGURE 3. LM8272 PM vs. CL

It can be shown that the PM degradation for LM8272 with the chosen capacitor values is less than what would be expected if the Op Amp open loop parameters (i.e. dominant

Closed Loop Phase Margin Measurement (Continued)

pole frequency) stayed fixed. The LM8272 has specifically been designed such that a heavy capacitive load will internally shift the dominant pole frequency higher. This feature is intended to keep the phase shift around the loop to less than 180° under any capacitive load The LM8272 architecture is explained further below.

However, it is important to remember that as in most Op Amps, addition of a series isolation resistor between the output and the load improves the settling and overshoot performance

LM8272 Architecture

To understand how LM8272 achieves "unlimited capacitive load" drive capability, its internal block diagram is shown in *Figure 4* below:

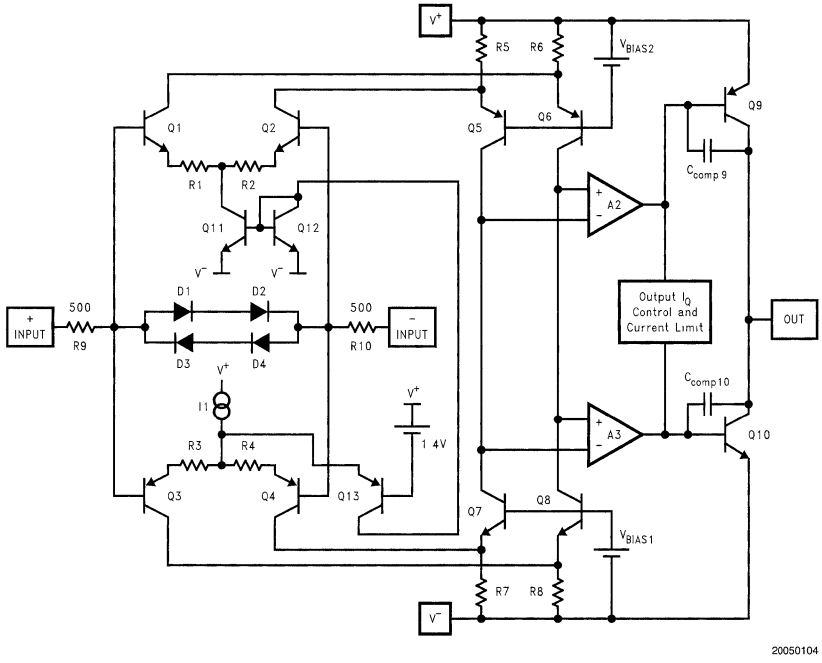


FIGURE 4. LM8272 Simplified Schematic

The output stage is comprised of complementary NPN and PNP common-emitter stages to permit voltage swing to within a V_{CE} (sat) of either supply rail. Q9 supplies the sourcing and Q10 supplies the sinking current load. Output current limiting is achieved by limiting the V_{CE} of Q9 and Q10. The frequency compensation circuit includes Miller capacitors from collector to base of each output transistor (C_{comp9} and C_{comp10}). At light capacitive loads, the high frequency gain of the output transistors is high, and the Miller effect increases the effective value of the capacitors thereby stabilizing the Op Amp. Large capacitive loads greatly decrease the high frequency gain of the output transistors thus lowering the effective internal Miller capacitance. The internal pole frequency increases at the same time a low frequency pole is created at the Op Amp output due to the large load capacitor. In this fashion, the internal dominant pole compensation, which works by reducing the loop gain to less than OdB when the phase shift around the feedback loop is more than 180°, varies with the amount of capacitive load and becomes less dominant when the load capacitor has increased enough Hence, the Op Amp is very stable even at high values of load capacitance resulting in the uncharacteristic feature of stability under all capacitive loads.

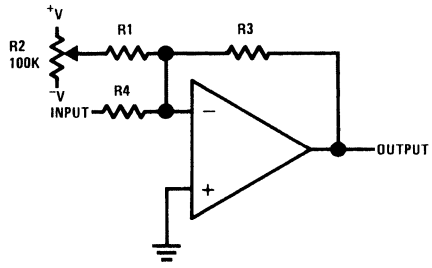
Conclusion

Readily available Op Amp's have always suffered from inability to drive capacitive loads and instabilities associated with that. A new Op Amp design, LM8272 (Dual) and LM8261 (Single) have mostly alleviated this problem to the extent that these devices can even be used as voltage buffers with heavy capacitors sitting right at their output.

Universal Balancing Techniques

National Semiconductor
Linear Brief 9
Hooman Hashemi

IC op amps are widely accepted as a universal analog component. Although the circuit designs may vary, most devices are functionally interchangeable. However, offset voltage balancing remains a personality trait of the particular amplifier design. The techniques shown here allow offset voltage balancing without regard to the internal circuitry of the amplifier.



R1 = 2000 R3 ‖ R4

R4 ‖ R3 ≤ 10 kΩ

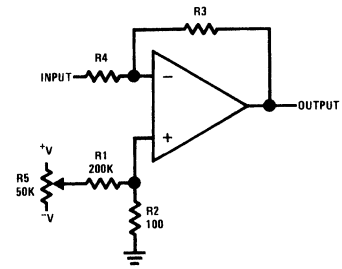
$$\text{RANGE} = \pm V\left(\frac{R3 \parallel R4}{R1}\right)$$

FIGURE 1. Offset Voltage Adjustment for Inverting Amplifiers Using 10 kΩ Source Resistance or Less

The circuit shown in *Figure 1* is used to balance out the offset voltage of inverting amplifiers having a source resistance of 10 kΩ or less. A small current is injected into the summing node of the amplifier through R_1. Since R_1 is 2000 times as large as the source resistance the voltage at the arm of the pot is attenuated by a factor of 2000 at the summing node. With the values given and ±15V supplies the output may be zeroed for offset voltages up to ±7.5 mW.

If the value of the source resistance is much larger than 10 kΩ, the resistance needed for R_1 becomes too large. In this case it is much easier to balance out the offset by supplying a small voltage at the non-inverting input of the amplifier. *Figure 2* shows such a scheme. Resistors R_1 and R_2 divide the voltage at the arm of the pot to supply a ±7.5 mW adjustment range with ±15V supplies.

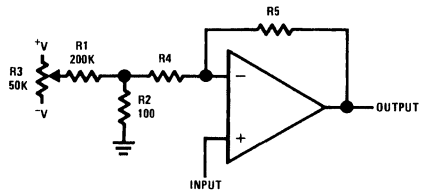
This adjustment method is also useful when the feedback element is a capacitor or non-linear device.



$$\text{RANGE} = \pm V\left(\frac{R2}{R1}\right)$$

FIGURE 2. Offset Voltage Adjustment for Inverting Amplifiers Using Any Type of Feedback Element

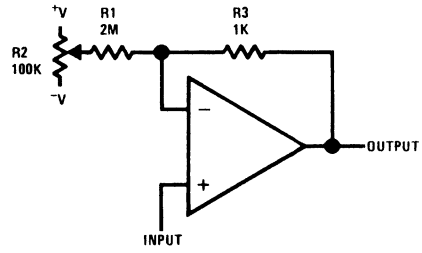
This technique of supplying a small voltage effectively in series with the input is also used for adjusting non-inverting amplifiers. As is shown in *Figure 3*, divider R_1, R_2 reduces the voltage at the arm of the pot to ±7.5 mW for offset adjustment. Since R_2 appears in series with R_4, R_2 should be considered when calculating the gain. If R_4 is greater than 10 kΩ the error due to R_2 is less than 1%.



$$\text{RANGE} = \pm V\left(\frac{R2}{R1}\right)$$

$$\text{GAIN} = 1 + \frac{R5}{R4 + R2}$$

FIGURE 3. Offset Voltage Adjustment for Non-Inverting Amplifiers

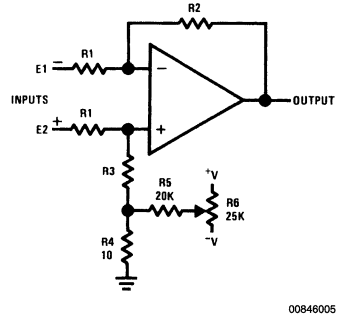


$$\text{RANGE} = \pm V\left(\frac{R3}{R1}\right)$$

FIGURE 4. Offset Voltage Adjustment for Voltage Followers

A voltage follower may be balanced by the technique shown in *Figure 4*. R_1 injects a current which produces a voltage drop across R_3 to cancel the offset voltage. The addition of the adjustment resistors causes a gain error, increasing the gain by 0.05%. This small error usually causes no problem. The adjustment circuit essentially causes the offset voltage to appear at full output, rather than at low output levels, where it is a large percentage error.

Differential amplifiers are somewhat more difficult to balance. The offset adjustment used for a differential amplifier can degrade the common mode rejection ratio. *Figure 5* shows an adjustment circuit which has minimal effect on the common mode rejection. The voltage at the arm of the pot is divided by R_4 and R_5 to supply an offset correction of ±7.5 mV. R_4 and R_5 are chosen such that the common mode rejection ratio is limited by the amplifer for values of R_3 greater than 1 kΩ. If R_3 is less than 1k the shunting of R_4 by R_5 must be considered when choosing the value of R_3.



$$R2 = R3 + R4$$

$$\text{RANGE} = \pm V\left(\frac{R5}{R4}\right)\left(\frac{R1}{R1 + R3}\right)$$

$$\text{GAIN} = \frac{R2}{R1}$$

FIGURE 5. Offset Voltage Adjustment for Differential Amplifiers

The techniques described for balancing offset voltage at the input of the amplifier offer two main advantages: First, they are universally applicable to all operational amplifiers and allow device interchangeability with no modifications to the balance circuitry. Second, they permit balancing without interfering with the internal circuitry of the amplifier. The electrical parameters of the amplifiers are tested and guaranteed without balancing. Although it doesn't usually happen, balancing could degrade performance.

Predicting Op Amp Slew Rate Limited Response

National Semiconductor
Linear Brief 19
Hooman Hashemi

The following analysis of sine and step voltage responses applies to all single dominant pole op amps such as the LM101A, LM107, LM108A, LM112, LM118 and the LM741. Each of these op amps has an open loop response curve with a shape similar to the one shown in *Figure 1*. The distinguishing feature of this curve is the single low frequency turnover from a flat response to a uniform –20 dB per decade of frequency (–6 dB/octave) drop in gain, at least until the curve passes through the 0 dB line. Closing the loop to 40 dB (X100) as shown with a dotted line on *Figure 1* does not change the shape of the curve, but it does move the turnover to a higher frequency. These open loop and closed loop response curves determine the gain applied to small signal inputs. The logical question then arises as to when a signal can no longer be treated as a small signal and the amplifier response begins to deviate from this curve.

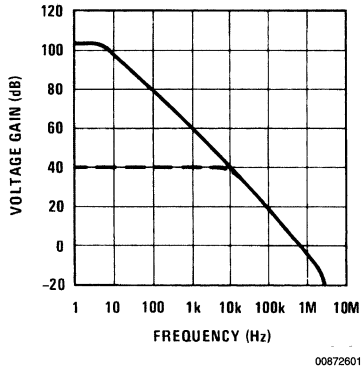


FIGURE 1. Open and Closed Loop Frequency Response

The answer lies in the slew rate limit of the op amp. The slew rate limit is the maximum rate of change of the amplifier's output voltage and is due to the fact that the compensation capacitor inside the amplifier only has finite currents[1] available for charging and discharging. A sinusoidal output signal will cease being a small signal when its maximum rate of change equals the slew rate limit S_r of the amplifier. The maximum rate of change for a sine wave occurs at the zero crossing and may be derived as follows:

$$v_o = V_P \sin 2\pi ft \quad (1)$$

$$\frac{dv_o}{dt} = 2\pi f V_P \cos 2\pi ft \quad (2)$$

$$\left.\frac{dv_o}{dt}\right|_{t=0} = 2\pi f V_p \quad (3)$$

$$S_r = 2\pi f_{max} V_p \quad (4)$$

where:

v_o = output voltage

V_p = peak output voltage

where: v_o = output voltage

v_p = peak output voltage

S_r = maximum $\frac{dv_o}{dt}$

The maximum sine wave frequency an amplifier with a given slew rate will sustain without causing the output to take on a triangular shape is therefore a function of the peak amplitude of the output and is expressed as:

$$f_{max} = \frac{S_r}{2\pi V_p} \quad (5)$$

Equation (5) demonstrates that the borderline between small signal response and slew rate limited response is not just a function of the peak output signal but that by trading off either frequency or peak amplitude one can continue to have a distortion free output. *Figure 2* shows a quick reference graphical presentation of *Equation (5)* with the area above any V_{PEAK} line representing an undistorted small signal response and the area below a given V_{PEAK} line representing a distorted sine wave response due to slew rate limiting.

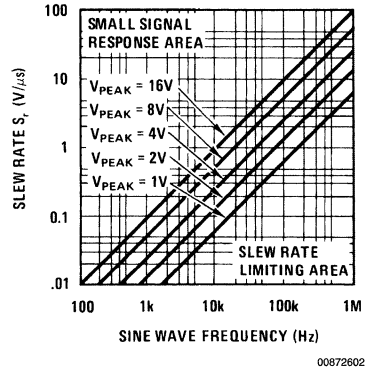


FIGURE 2. Sine Wave Response

As a matter of convenience, amplifier manufacturers often give a "full-power bandwidth" or "large signal response" on their specification sheets.

This frequency can be derived by inserting the amplifier slew rate and peak rated output voltage into *Equation (5)*. The bandwidth from DC to the resulting f_{max} is the full-power bandwidth or "large signal response" of the amplifier. For example the full-power bandwidth of the LM741 with a 0.5V

μs S_r is approximately 6 kHz while the full-power bandwidth of the LM118 with an S_r of 70 V/μs is approximately 900 kHz.

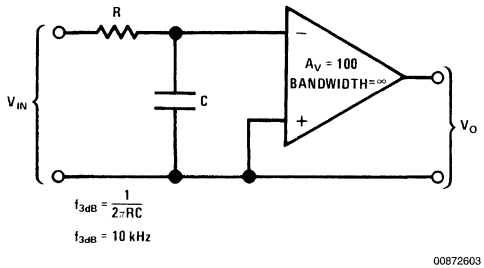


FIGURE 3. Small Signal Op Amp Model

The step voltage response at the output of an op amp can also be divided into a small signal response and a slew rate limited response. The signal turnover and uniform −20 dB/decade slope shown in the small signal frequency response curve of *Figure 1* are also characteristic of a low pass filter and one can in fact model an op amp as a low pass RC filter followed by a very wideband amplifier. *Figure 3* shows a model of a X100 circuit with a 3 dB down rolloff frequency of 10 kHz. From basic filter theory[2] the 10% to 90% rise time of single pole low pass filter is:

$$t_r = \frac{0.35}{f_{3dB}} \qquad (6)$$

which for this example would be 35 μs. Again this small signal or low pass filter response ceases when the required rate of change of the output voltage exceeds the slew rate limit S_r of the amplifier. Mathematically stated:

$$\frac{V_{STEP}}{t_r} \geq S_r \qquad (7)$$

This means that as soon as the amplitude of the output step voltage divided by the rise time of the circuit exceeds the S_r of the amplifier, the amplifier will go into slew rate limiting. The output will then be a ramp function with a slope of S_r and a rise time equal to:

$$t'_r = \frac{V_{STEP}}{S_r} \qquad (8)$$

Subsituting *Equation (6)* into *Equation (7)* gives the critical value of V_{STEP} directly in terms of f_{3dB}:

$$\frac{V_{STEP}\, f_{3db}}{0.35} \geq S_r \qquad (9)$$

which can be graphed as shown in *Figure 4*. Any point in the area above a V_{STEP} line represents an undistorted low pass filter type response and any point in the area below a given V_{STEP} line represents a slew rate limited response.

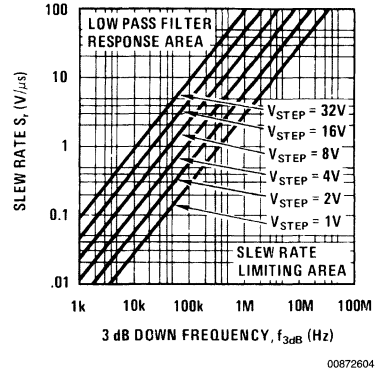


FIGURE 4. Step Voltage Response

The above equations and graphs should allow one to avoid the pitfalls of slew rate limiting and also provide a means of using engineering tradeoffs to extend the response of the single dominant pole type of amplifier.

References

1. Solomon, J. E.; Davis, W. R.; and Lee, P. L.: *"A Self-Compensated Monolithic Operational Amplifier With Low Input Current and High Slew Rate"*, pp. 14–15, ISSCC Digest Tech. Papers, February 1969.
2. Millman, J. and Hawkias, C. C.: *"Electronic Devices and Circuits"*, pp. 465–466, McGraw-Hill Book Company, New York, 1967.

Instrumentational Amplifiers

National Semiconductor
Linear Brief 21
Hooman Hashemi

Introduction

One of the most useful analog subsystems is the true instrumentation amplifier. It can faithfully amplify low level signals in the presence of high common mode noise. This aspect of its performance makes it especially useful as the input amplifier of a signal processing system. Other features of the instrumentation amplifier are high input impedance, low input current, and good linearity.

It has never been easy to design a high performance instrumentation amplifier; however, the availability of high performance IC's considerably simplifies the problem. IC op amps are available today that can give very low drifts as well as low bias currents; however, most of the circuits have some drawbacks.

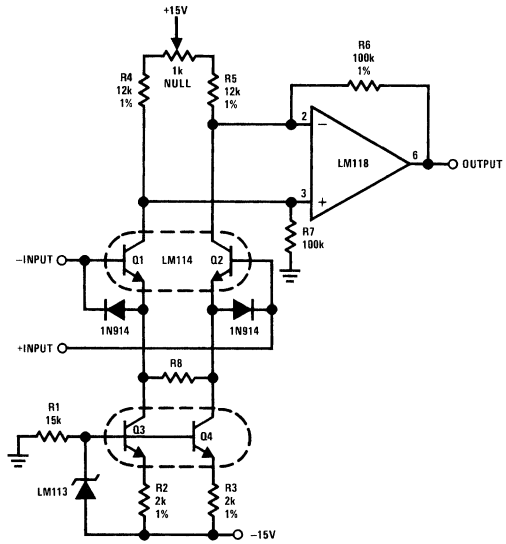
The most commonly used instrumentation amplifier designs utilize either 2 or 3 op amps and several precision resistors. These are capable of excellent performance; however, for high performance they require very precisely matched resistors. The common mode rejection of these designs depends on resistor matching and overall gain. Since op amps are now available with exceedingly high CMRR, this is no longer a problem. The CMRR of the instrumentation amplifier is approximately equal to half resistor mismatch plus the gain. For a 1% resistor mismatch the CMRR is limited to 46 dB plus the gain—referred to the input.

Referred to the output, the common mode error is independent of gain and fixed by the resistor mismatch. For 1% match the error is 0.5%, and for 0.1% match the error is 0.05%. These errors are not trivial in high precision systems.

An instrumentation amplifier is shown here that compares favorably with multiple op amp designs, yet does not require precisely matched resistors. Further, the design allows a single resistor to adjust the gain. In comparing this instrumentation amp to multiple op amp types there are of course some drawbacks. The gain linearity and accuracy are not as good as the multiple op amp circuits.

The errors appearing in multiple op amp circuits are independent of the output signal level. For example, a common mode error at the output of 0.5% of full scale is a 33% error if the desired output signal is only 1.5% of full scale. With the new circuit maximum errors at full scale output and the percentage of output error decreases at lower output levels.

Figure 1 shows a general purpose instrumentation amplifier optimized for wide bandwidth. It can provide gains from under 1 to over 1000 with a single resistor adjustment. Gain linearity is worst for unity-gain at 0.4%, and gain stability is better than 1.5% from −55˚C to +125˚C. Typically over a 0˚C to +70˚C range gain stability is 0.2%. Common mode rejection ratio is about 100 dB—independent of gain.



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Note: Since the LM114 is an obsolete part, substitution of the LM194 is recommended, along with the removal of the two LM194 diodes This circuit has not been tested with the LM194 included.

Also, the LM185-1 2 could be substituted for the LM113.

FIGURE 1. Instrumentation Amplifier

Transistor pair, Q1 and Q2, are operated open-loop as the input stage to give a floating, fully differential input. Current sources, Q3 and Q4, set the operating current of the input pair. To obtain good linearity the output current of Q3 and Q4 are set at about twice the current in R8 at full differential voltage. The temperature sensitivity of the transconductance of Q1 and Q2 is compensated by making their operating current directly proportional to absolute temperature. It has been shown that by biasing the base of transistor current sources at 1.22V, the output current varies as absolute temperature. The LM113 diode provides a constant 1.22V to the current sources. Both the compensated gm of Q1 and Q2 and the large degeneration from R8 give the amplifier stable gain over a wide temperature range.

In operation, transistors Q1 and Q2 convert a differential input voltage to a differential output current at their collectors. This is fed into a standard differential amplifier to obtain a single ended output voltage. Since the diff amp does not see the common mode input voltage, 1% resistors are adequate. Gain is set by the ratio of R8 (plus the r_e of Q1 and Q2) to the sum of R6 and R7.

As mentioned previously this circuit is optimized for wide bandwidth: however, it is easily modified for other applications. If low bias current is needed, all resistors can be increased by a factor of 100 and an LM108 substituted for the LM318. Other possible improvements are cascaded current sources and a modified Darlington input stage.

Low Drift Amplifiers

National Semiconductor
Linear Brief 22
Hooman Hashemi

Introduction

Since the introduction of the monolithic IC amplifier, there has been a continued improvement in DC accuracy. Bias currents have been decreased by five orders of magnitude over the past five years. Low offset voltage drift is also necessary in high-accuracy circuits. This is evidenced by the popularity of low-drift amplifier types as well as requests for selected low-drift op amps. However, little has been written about the problems associated with handling microvolt signals with a minimum of errors.

A very low drift amplifier poses some uncommon application and testing problems. Many sources of error can cause the apparent circuit drift to be much higher than would be predicted. In many cases, the low drift of the op amp is completely swamped by external effects while the amplifier is blamed for the high drift.

Thermocouple effects caused by temperature gradient across dissimilar metals are perhaps the worst offenders. Whenever dissimilar metals are joined, a thermocouple results. The voltage generated by the thermocouple is proportional to the temperature difference between the junction and the measurement end of the metal. This voltage can range between essentially zero and hundreds of microvolts per degree, depending on the metals used. In any system using integrated circuits, a minimum of three metals are found: copper, solder, and kovar (lead material of the IC).

Nominally, most parts of the circuit are at the same temperature. However, a small temperature gradient can exist across even a few inches—and this is a big problem with the low level signals. Only a few degrees gradient can cause hundreds of microvolts of error. Two places where this shows up, generally, are the package-to-printed-circuit-board interface and temperature gradients across resistors. Keeping package leads short and the two input leads close together help greatly.

For example, a very low drift amplifier was constructed and the output monitored over a 1-minute period. During the one minute it appeared to have input referred offset variations of ±5.0 µV. Shielding the circuit from air currents reduced this to ±0.5 µV. The 10 µV error was due to thermal gradients across the circuit from air currents.

Resistor choice as well as physical placement is important for minimizing thermocouple effects. Carbon, oxide film, and some metal-film resistors can cause large thermocouple errors. Wirewound resistors of evenohm or managanin are best since they only generate about 2.0 µV/°C referenced to copper. Of course, keeping the resistor ends at the same temperature is important. Generally, shielding a low-drift stage electrically and thermally yields good results.

Resistors can cause other errors besides gradient generated voltages. If the gain setting resistors do not track with temperature, a gain error will result. For example, a gain-of-1000 amplifier with a constant 10 mV input will have 10V output. If the resistors mistrack by 0.5% over the operating temperature range, the error at the output is 50 mV. Referred to input, this is a 50 µV error. Most precision resistors use different material for different ranges of resistor values. It is not unexpected that a resistor differing by a factor of 1000 does not track perfectly with temperature. For best results, ensure that the gain fixing resistors are of the same material or have tracking temperature coefficients.

It is appropriate to mention offset balancing as this can have a large effect on drift. Theoretically, the drift of a transistor differential amplifier depends on the offset voltage. For every millivolt of offset voltage the drift is 3.6 µV/°C. Therefore, if the offset is nulled, the drift should be zero. When working with IC op amps, this is not the case. Other effects, such as second stage drift and internal resistor TC, make the drift nontheoretical.

Certain types of amplifiers are optimized to have lower drift with offset balancing such as the LM121 and LM725. With this type of device offset, nulling improves the drift, and offset nulling should be used. Other types of devices, such as selected LM741's or LM308's, are selected for the drift without offset nulling connected to the device. The addition of a balancing network changes the internal currents and thus changes the drift—probably for the worse—so any offset balancing should be done at the input.

No matter which null network is applied, highly stable resistors must be used. They should have low TC and track. Wirewound pots are usually a good choice. Finally, when the null network reduces a drift, the balancing of the amplifier as close to zero offset as possible minimizes the drift.

Testing low-drift amplifiers is also difficult. Standard drift testing techniques such as heating the device in an oven and having the leads available through a connector, thermoprobe, or the soldering iron method do not work. Thermal gradients can cause much greater errors than the amplifier drift. Coupling microvolt signal through connectors is especially bad since the temperature difference across the connector can be 50°C or more. The device under test, along with the gain setting resistor, should be isothermal. The circuit in *Figure 1* will yield good results if well constructed.

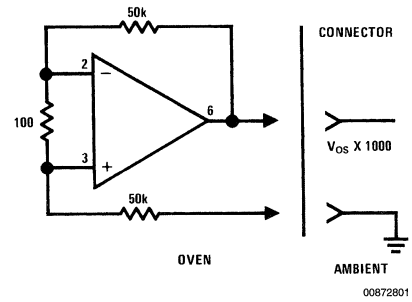


FIGURE 1. Drift Measurement Circuit

Conclusion

Low-drift amplifiers need extreme care to achieve reproducable low drift. Thermal and electrical shielding minimize thermocouple effects. Resistor choice is also important as they can introduce large errors. Careful attention to circuit layout offset balancing circuitry is also necessary

Precise Tri-Wave Generation

National Semiconductor
Linear Brief 23
Hooman Hashemi

Introduction

The simple Tri-wave generator has become an often used analog circuit. Tri-wave oscillators are more easily designed, require less circuitry, and are more easily stabilized than sine wave oscillators. Further, the highly linear output of today's Tri-wave generators make them useful in many "sweep" circuits and test equipment.

This article describes a triangle wave generator with an easily controlled peak-to-peak amplitude. The positive and negative peak amplitude is controllable to an accuracy of about ±0.01V by a DC input. Also, the output frequency and symmetry are easily adjustable.

Circuit Description

The Tri-wave oscillator consists of an integrator and two comparators—one comparator sets the positive peak and the other the negative peak of the Tri-wave. To understand the operation, assume that the output of the comparator is low (–5V). Then –5.0V is applied through R1 to the input of the integrator. The LM118 will integrate positive until its output is equal to the positive reference on pin 9 of the LM119. Since the comparator outputs are low, D1 is reverse biased and the full output of the integrator is applied to the non-inverting input of comparator A. As the integrator output crosses the positive reference, comparator A switches "plus" and latches "plus" from positive feedback through D1 and R4. Now the polarity of the current to the integrator has changed and the integrator starts ramping negative. When the output reaches the negative reference voltage, comparator B swings negative. This forces the output of comparator A negative, also, and stops the positive feedback through D1 from holding the comparator's outputs positive. Once the positive feedback loop is broken, the outputs of the comparators stay low. With the comparator's outputs low, the integrator ramps positive again.

The frequency of operation is dependent upon R1, C1 and the reference voltages. Frequency is given by:

$$F = \frac{5.0V}{2R1\ C1\ (V_{REF}{}^{+} - V_{REF}{}^{-})}$$

The maximum frequency of operation is limited by the circuit delay to about 200 kHz. Also, the maximum difference in reference voltages is 5.0V.

Applications

Regular or op amp testing is made easier with precise triangle waves. For example, IC voltage regulators are usually specified to operate over a certain input voltage range such as 7.0V to 25V. The Tri-wave generator can be set to deliver a 0.7V to 2.5V output. This output is then amplified by a factor of 10 by an op amp and used to sweep the regulator input over its operating range. With op amps, the generator can be used to sweep common mode voltages, power supply voltages, or even to test output swing. The output of the device can be displayed on an oscilloscope and performance monitored over the entire operating range.

Another application is a voltage controlled oscillator. Since the frequency depends on the input reference voltage, varying the reference varies the frequency. The useful VCO range is about 2 decades. The output is then taken from the comparators as the Tri-wave changes in amplitude.

Many sine wave oscillators use a non-linear network to convert triangle wave to sines. It is usually necessary to set triangle amplitude precisely for minimum distortion. If R1 is replaced by a pot, frequency can be varied over at least 10 to 1 range without affecting amplitude.

Symmetry is also easily adjustable. Current can be injected into the inverting input of the LM118 to change ramp time. The easiest way to achieve this is to connect a 50 kΩ resistor from the inverting input of the LM118 to the arm of a 1 kΩ pot. The ends of the pot are connected across the supplies. Current from the resistor either adds or subtracts from the current through R1, changing the ramp time.

Applications (Continued)

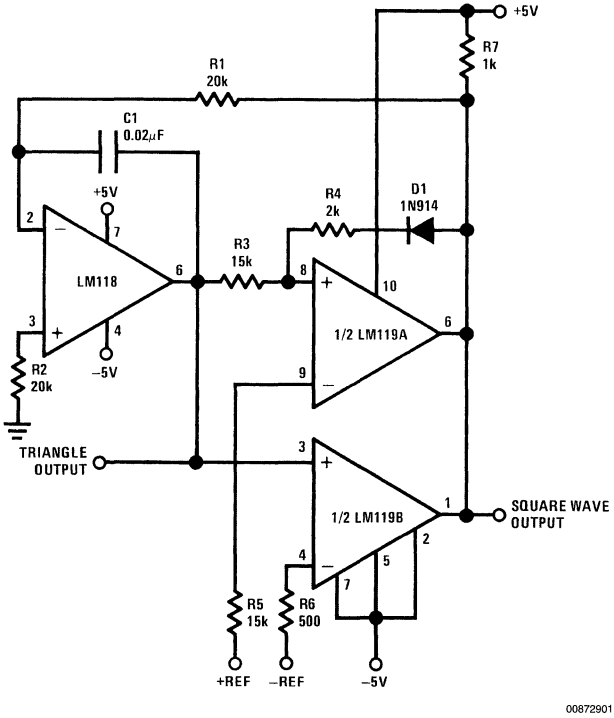


FIGURE 1. Precision Tri-Wave Generator

Versatile IC Preamplifier Makes Thermocouple Amplifier with Cold Junction Compensation

National Semiconductor
Linear Brief 24
Hooman Hashemi

Introduction

Accurate electronic temperature measurements are not simple. There exists a large array of temperature sensors; each with its own peculiarities. The major sensors are thermistors, resistance sensors, and thermocouples. (Diodes and transistors have been used but they are not normally sold for this purpose.) Thermistors are highly non-linear, making wide range measurements difficult. Resistance sensors are large, require a bridge, and tend to be relatively costly. Thermocouples are small, relatively linear, inexpensive, but require reference junction temperature compensation.

Thermocouples are made when wires of different metals are joined. A voltage is produced proportional to the temperature *difference* between the junction and the output ends of the wire. This voltage is the Seebeck coefficient and is usually specified in volts (or microvolts) per degree. Commercially available thermocouples produce an output of between 10 µV/°C and 50 µV/°C.

Since the output voltage of thermocouples is proportional to temperature difference, the ambient temperature or measurement end of the thermocouple must be known. Alternatively, compensation can be applied for temperature changes. This is done either by terminating the thermocouple in a temperature controlled environment or with electrical compensation circuitry. The amplifier shown here provides a direct reading output of 10 mV/°C and automatically compensates for reference junction temperature changes. Further, calibration is relatively simple.

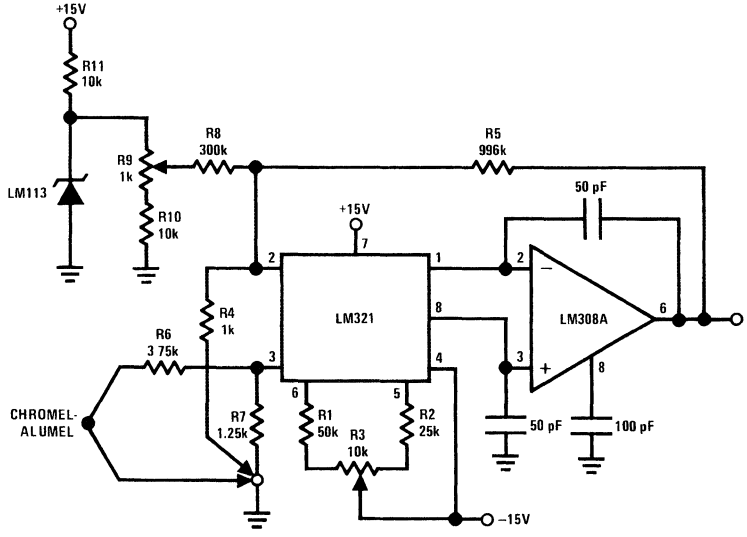
Circuit Description

An LM321 preamp is used in conjunction with an LM308A op amp to form a precision, low-drift, operational amplifier. The LM321 is specifically designed for use with general purpose op amps to obtain drifts of 1 µV/°C. When the offset voltage is nulled, the drift is also nulled. There is a theoretical relationship between the offset voltage and drift when the offset is not nulled to zero. The drift of the amplifier is then used to compensate the thermocouple for ambient temperature variations. Drift given by:

$$\frac{d\,V_{OS}}{dT} = \frac{V_{OS}}{T}$$

where T is in degrees Kelvin.

Resistors R1, R2, and R3 set the operating current of the preamp, and R3 is used to adjust the offset. The offset and drift are amplified by the ratio of the feedback resistors R4 and R5 and appear at the output. R6 and R7 attenuate the thermocouple's output to 10 µV/°C to match the amplifier drift and set the scale factor at 10 mV/°C. The LM113 provides a temperature stable reference for offsetting the output to read directly in degrees centigrade.



Calibration

Calibration is independent of thermocouple type; however, circuit values are for chromel alumel. R6 and R7 must be changed for different thermocouples. First, the thermocouple is replaced by a short of copper wire and the LM113 is shorted to ground. Then the offset is adjusted so the output reads the ambient temperature at 10 mV/°k—for 25°C this is 2.98V. The short across the LM113 is removed and R9 is adjusted for the correct output in degrees centigrade. Connect the thermocouple, and it's ready to go.

Performance

It should be mentioned that for stable performance, good construction techniques are necessary. Resistors R4, R6, and R7 should be wirewound so they contribute a minimum of error due to thermocouple effects from temperature gradients across the circuit. The entire circuit should be enclosed in a box with the end of the thermocouple terminated in the box near the LM321. This will minimize temperature gradients across the circuit and insure close thermal coupling between the LM321 and the reference end of the thermocouple.

Typically, the LM321 will track temperature changes with less then 0.03°C error per degree change. Self-heating of the LM321 will change its temperature by about 2°C; this is calibrated out initially. Reference and resistor drift can be expected to contribute about 0.02°C/°C. Of course, no compensation is made for nonlinearities of the thermocouple output voltage as a function of temperature. Over a wide measurement range with relatively stable ambient temperature, thermocouple error will be the major inaccuracy.

True RMS Detector

National Semiconductor
Linear Brief 25
Hooman Hashemi

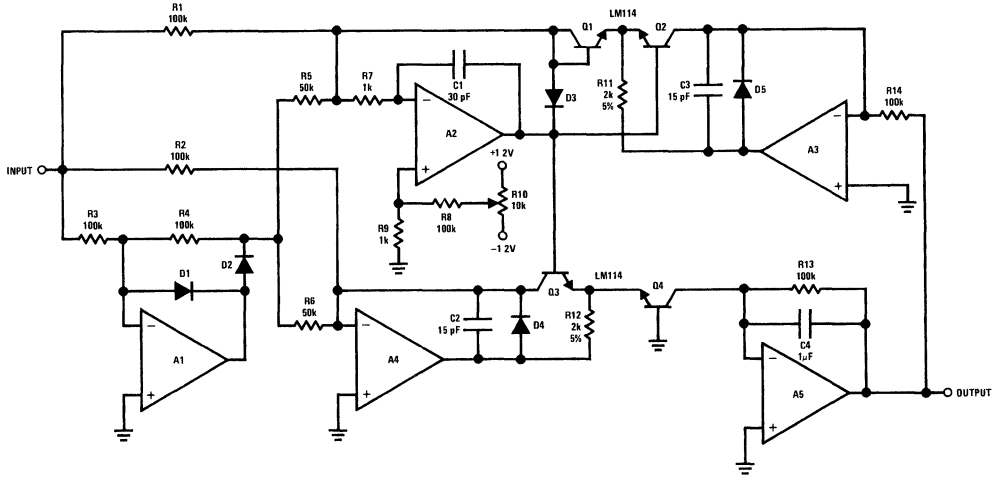
Introduction

The op amp precision rectifier circuits have greatly eased the problems of AC to DC conversion. It is possible to measure millivolt AC signal with a DC meter with better than 1% accuracy. Inaccuracy due to diode turn-on and nonlinearity is eliminated, and precise rectification of low level signals is obtained.

Once the signal is rectified, it is normally filtered to obtain a smooth DC output. The output is proportional to the average value of the AC input signal, rather than the root mean square. With known input waveforms such as a sine, triangle, or square; this is adequate since there is a known proportionality between rms and average values. However, when the waveform is complex or unknown, a direct readout of the rms value is desirable.

The circuit shown will provide a DC output equal to the rms value of the input. Accuracy is typically 2% for a 20 V_{p-p} input signal from 50 Hz to 100 kHz, although it's usable to about 500 kHz. The lower frequency is limited by the size of the filter capacitor. Further, since the input is DC coupled, it can provide the true rms equivalent of a DC and AC signal.

Basically, the circuit is a precision absolute value circuit connected to a one-quadrant multiplier/divider. Amplifier A1 is the absolute value amplifier and provides a positive input current to amplifiers A2 and A4 independent of signal polarity. If the input signal is positive, A1's output is clamped at −0.6V, D2 is reverse biased, and no signal flows through R5 and R6. Positive signal current flows through R1 and R2 into the summing junctions of A2 and A4. When the input is negative, an inverted signal appears at the output of A1 (output is taken from D2). This is summed through R5 and R6 with the input signal from R1 and R2. Twice the current flows through R5 and R6 and the net input to A2 and A4 is positive.



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Notes:

All operational amplifiers are LM118. All resistors are 1% unless otherwise specified All diodes are 1N914 Supply voltage ±15V.

Amplifiers A2 through A5 with transistors Q1 through Q4 form a log multiplier/divider. Since the currents into the op amps are negligible, all the input currents flow through the logging transistors. Assuming the transistors to be matched, the V_{be} of Q4 is:

$$V_{be}\ (Q4) = V_{be}\ (Q1) + V_{be}\ (Q3) - V_{be}\ (Q2)$$

The V_{be}'s of these transistors are logarithmically proportional to their collector currents so

$$\log (I_{C4}) = \log (I_{C1}) + \log (I_{C3}) - \log (I_{C2})$$

$$\text{or } I_{C4} = \frac{I_{C1} I_{C3}}{I_{C2}}$$

where I_{C1}, I_{C2}, I_{C3}, and I_{C4} are the collector currents of transistors Q1–Q4.

Since I_{C1} equal I_{C3} and is proportional to the input, the square of the input signal is generated. The square of the input appears as the collector current of Q4. Averaging is done by C4, giving a mean square output. The filtered output of Q4 is fed back to Q2 to perform continuous division where the divisor is proportional to the output signal for a true root mean square output.

Due to mismatches in transistors, it is necessary to calibrate the circuit. This is accomplished by feeding a small offset into amplifier A2. A 10V DC input signal is applied, and R10 is adjusted for a 10V DC output. The adjustment of R10 changes the gain of the multiplier by adding or subtracting voltage from the log voltages generated by the transistors. Therefore, both the resistor inaccuracies and V_{be} mismatches are corrected.

For best results, transistors Q1 through Q4 should be matched, have high beta, and be at the same temperature. Since dual transistors are common, good results can be obtained if Q1, Q2 and Q3, Q4 are paired. They should be mounted in close proximity or on a common heat sink, if possible. As a final note, it is necessary to bypass all op amps with 0.1 µF disc capacitors.

Microvolt Comparator

National Semiconductor
Linear Brief 32
Hooman Hashemi

Introduction

Comparison of dc signal levels within microvolts of each other can be made by using an LM121A pre-amp and an LM111 comparator IC. Implementing this with two separate IC's decreases noise, eliminates troublesome thermal effects, and achieves a maximum offset drift of 0.22 µV/°C (*Figure 1*).

Designing a practical comparator with a voltage gain of 10 million involves protecting the *input* stage from temperature changes or gradients, and avoiding problems of including the noise filter within the positive feedback loop. The circuit as shown has a 5 µV hysteresis which can be trimmed to 1 µV under certain conditions. Further, delays *decrease* with increasing overdrive (see chart) due to elimination of input stage thermal effects, saturating stages, and dielectric soak or polarization effects on signal filter capacitors *Table 1*.

Designing with a Pre-Amp

With the bias network shown, the LM121A input stage has an open-loop temperature stable voltage gain of close to 100. The 100k output impedance of the LM121A is shunted by C_S to filter out pickup and internally generated noise. No feedback to the inputs of the pre-amp is employed to avoid degrading common-mode rejection of the system.

The separate pre-amp with a gain of 100 provides two major advantages over single comparator designs. First, V_{OS} and other small errors attributed to the LM111 are reduced by the 100 gain factor. More important, temperature gradient changes which occur within the LM111 when switching any output load, are completely isolated by the separate packages and do not affect the pre-amp. If the entire microvolt comparator were on a single silicon chip, a temperature variation of as little as 1/1000°C across the input stage could have a significant effect.

This effect is a major reason for designing circuits sensitive and stable to microvolt dc signals with a *separate* pre-amplifier. Further, the special 4-transistor input stage, when adjusted to zero offset with the "balance" control between pins 5 and 6, automatically reduces V_{OS} change with temperature to almost zero.

TABLE 1. Typical Overdrive Delays

Hyst. Set	R_H	R_S	C_S	Delays with Various Overdrives			
				25%	100%	1000%	100 mV
5 µV	75 kΩ	10 kΩ Max.	6800 pF	2 ms	1.8 ms	600 µs	560 µs

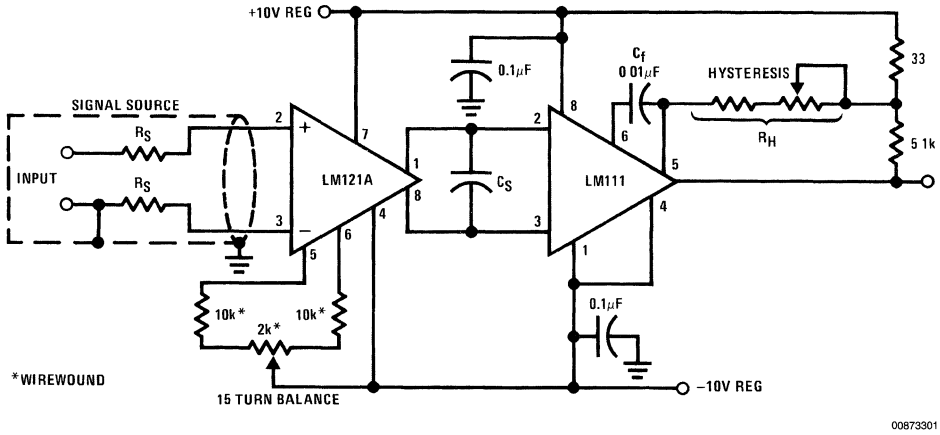


FIGURE 1. Schematic Diagram

Filtering

The pre-amp/comparator system generates a continuous stream of very fast pulses if assembled without a filter, even with positive feedback for hysteresis. This is caused by both stray output-input feedback, and noise. The noise is both thermal and pickup from the environment, including power switching transients and fluorescent light hash. To cure this, shunt filter capacitor C_S is used.

Placing this capacitor outside the positive feedback loop has two advantages. It eliminates a tendency for the comparator

Filtering (Continued)

to oscillate during slow transitions. Also, response time to small signals is halved since the positive hysteresis feedback signal is not stored on the filter capacitor.

A higher frequency filter (C_f) is needed to provide a low impedance shunt to any high frequency noise and stray feedback that may be picked up between LM111 terminals 5 and 6. These two terminals have almost the same voltage sensitivity as the normal input terminals. The positive feedback to terminal 5, as described below, is only delayed slightly by this filter.

Feedback

The positive feedback provided by the 5.1k/33Ω voltage divider with R_H is needed to insure clean, rapid changes of state. It is applied to one of the "balance" terminals (pin 5) of the LM111 to simplify the circuit over a balanced feedback network, and to minimize signal stored on C_S as previously described. The current fed back to terminal 5 is single ended with respect to the balance adjust network between these terminals, and hence injects a dc offset of the desired polarity and amplitude for a few microvolts of latching.

Performance

A tabulation is shown for one of the many possible combinations of input circuits, filters, etc. For large amplitude signals, C_S can be decreased and hysteresis increased for greater speed. Conversely, to obtain hysteresis as low as 1 µV, trim R_H (to about 300k) use a C_S of 0.01 µF to 0.1 µF and have a low impedance source of signals.

For reduced ambient range and drift specifications, an LM321 can be paired with the LM311 for a cost saving while maintaining the same comparison sensitivity.

Design Tips for Microvolt Signals

Even with high performance devices such as the LM121, microvolts of error can occur from thermocouple effects, common-mode signals, "microphonics," or unbalances in the input or nulling circuits. As pointed out in Application Note AN-79, Kovar lead to copper circuit board thermocouple effects can cause a 3.5 µV offset voltage for only 0.1°C difference across the input leads. A compact layout of input connections and shielding from air currents will minimize this problem.

Although the LM121A has excellent common-mode rejection (> 120 dB), a 1V change in common-mode voltage can induce up to 1 µV of error voltage. For this reason common-mode voltage changes should be kept to a minimum. Also, common-mode voltages allow mechanical vibrations in the probe cable to induce "microphonic" noise signals Short, stiff, low capacitance and symmetrical input shielded wires are recommended.

If it is possible to have a signal source balanced with regard to ground, it will help decrease errors due to bias currents, and noise due to common-mode and microphonic effects. Matched, low temperature coefficient parts should be used in the balance network, and care should be exercised in shielding input circuits and eliminating ground-loops.

Applications

The microvolt comparator is particularly well suited to controllers or test equipment having thermocouples or strain gauges as inputs. This includes wind speed indicators, RMS to dc converters, vacuum gauges, gas analysis equipment, conductivity gauges, and hot wire controls. The strain gauges can be used in materials testing, electronic weighing, pressure transducers, and load limiting sensors for cranes, hoists, and rolling mills.

As a temperature controller, ⅛ degree or less on-off differential can be obtained using thermocouple types E, J, T or K. Other microvolt signals used for control may come from Hall effect sensors, Bolometers, slide-wires, and heat-flow thermopiles. A microvolt comparator will be useful in "Go/No-Go" testing of low resistances such as switch and relay contacts, RTDs, coil and fuse resistances, and pressure-sensitive-plastic conductors.

A Micropower Voltage Reference

National Semiconductor
Linear Brief 34
Hooman Hashemi

A low-drift voltage reference can be easily made by converting a zero temperature coefficient current to a voltage. JFETs biased slightly below pinch-off exhibit a zero temperature coefficient drain current (I_D) as shown in *Figure 1*. With the above property and a micropower operational amplifier, used to convert the drain current to a voltage, a low power consumption voltage reference can be built as shown in *Figure 2*. The consumption of LM4250 op amp is programmed through resistor R_{SET}. Potentiometer P1 should be adjusted for low output (V_{REF}) temperature coefficient. Actually, it can be trimmed for positive, negative or zero temperature coefficient. The output voltage is trimmed through P2 and it is expressed by:

$$V_{REF} = I_{D1}(P'_2 + R1 + R2),$$

$$R2 = R3, I_{D1} \cong I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

With the values shown in *Figure 2*, the temperature coefficient of the output is 0.002%/°C and the overall standby current less than 100 µA. The characteristics of the LM4250 are a function of its supply current, which depends on R_{SET}, and V^+. V^+ can be provided by V_{REF} through the addition of a second FET, J2, shown in *Figure 3*. This way the parameters of the op amp will be independent of the unregulated input. The reference voltage can be taken from the wiper of the potentiometer P2 ($V_{REF} = V^+$) or from the source of J2 ($V_{REF} > V^+$). In the first case, the output impedance of the circuit is quite high and buffering may be required according to the application. The output impedance in the second case is low, essentially the 1/gm of (J2) divided by the loop gain of the circuit. In this case, a small temperature coefficient due to the supply current of the LM4250 is going to be added and be compensated for by an additional trimming of P1. V_{REF} is computed by:

$$V_{REF} \cong I_{D1}[P2 + R1 + R2] + P''_2[I_S + I_{D1}],$$

$$R2 = R3, I_S \cong \frac{6(V^+ - V_{BE})}{R_{SET}}$$

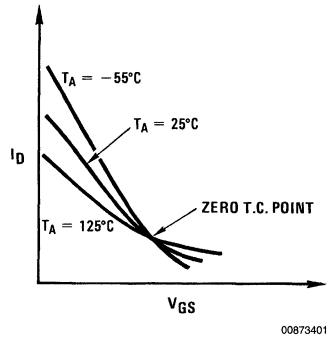
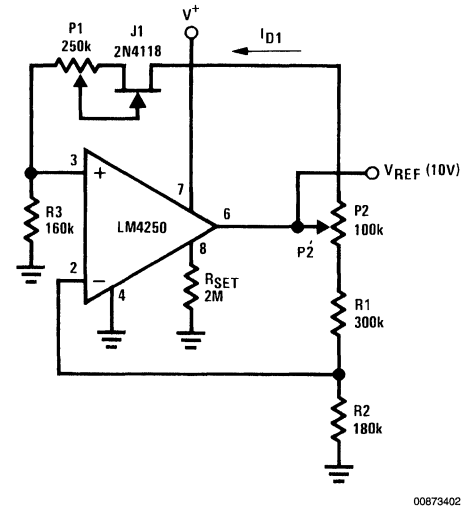


FIGURE 1. FET Transfer Characteristics



P1 = Drift Adjust

P2 = V_{REF} Adjust

FIGURE 2. Basic Voltage Reference

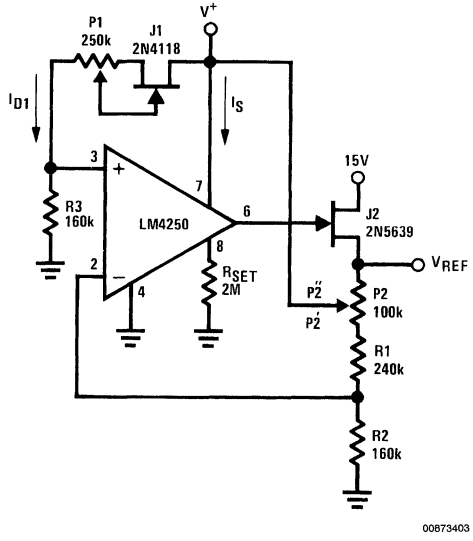


FIGURE 3. Improved Voltage Reference

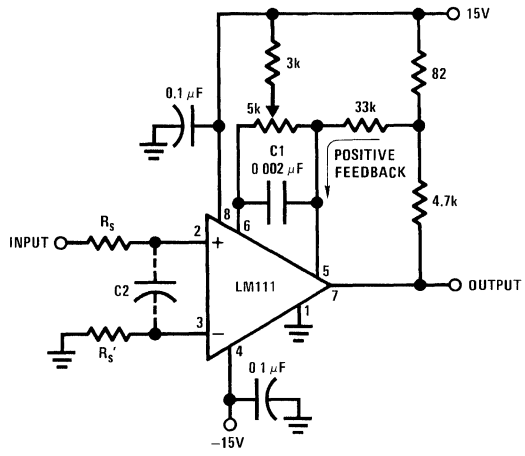
Circuit Techniques for Avoiding Oscillations in Comparator Applications

National Semiconductor
Linear Brief 39
Hooman Hashemi

When a high-speed comparator such as the LM111 is used with fast input signals and low source impedances, the output response will normally be fast and stable, assuming that the power supplies have been bypassed (with 0.1 µF disc capacitors), and that the output signal is routed well away from the inputs (pins 2 and 3) and also away from pins 5 and 6.

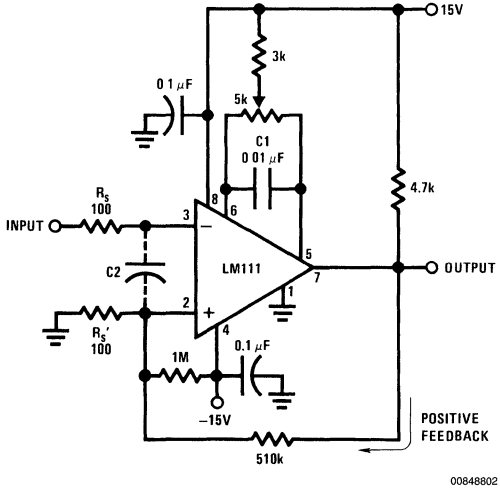
However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM111. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in *Figure 1* below.

1. The trim pins (pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trimpot, they should be shorted together. If they are connected to a trim-pot, a 0.01 µF capacitor C1 between pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if pin 5 is used for positive feedback as in *Figure 1*.
2. Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor C2 is connected directly across the input pins.
3. When the signal source is applied through a resistive network, R_s, it is usually advantageous to choose an R_s' of substantially the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used successfully in comparator input circuitry. Inductive wirewound resistors are not suitable.
4. When comparator circuits use input resistors (e.g. summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words there should be very little lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R_s = 10 kΩ, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to damp. Twisting these input leads tightly is the only (second best) alternative to placing resistors close to the comparator.
5. Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM111 circuitry, for example, one side of a double-layer circuit card. Ground foil (or, positive supply or negative supply foil) should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any high-level signals (such as the output). If pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located, at most, a few inches away from the LM111, and the 0.01 µF capacitor should be installed. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM111. (Some other comparators require the power-supply bypass to be located immediately adjacent to the comparator.)
6. It is a standard procedure to use hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier for its own noise. In the circuit of *Figure 2*, the feedback from the output to the positive input will cause about 3 mV of hysteresis. However, if the value of R_s is larger than 100Ω, such as 50 kΩ, it would not be reasonable to simply increase the value of the positive feedback resistor above 510 kΩ. The circuit of *Figure 3* could be used, but it is rather awkward. See paragraph 7, below, for the alternative.
7. When both inputs of the LM111 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM111 so that positive feedback would be disruptive, the circuit of *Figure 1* is ideal. The positive feedback is to pin 5 (one of the offset adjustment pins). It is sufficient to cause 1 to 2 mV hysteresis and ensure sharp output transitions with input triangle waves from a few Hz to hundreds of kHz. The positive feedback signal across the 82Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at pin 5, so this feedback does not add to the V_{OS} of the comparator. As much as 8 mV of V_{OS} can be trimmed out, using the 5 kΩ pot and 3 kΩ resistor as shown.
8. These application notes apply specifically to the LM111, LM211, LM311, and LF111 families of comparators, and are applicable to all high-speed comparators in general, (with the exception that not all comparators have trim pins).



Pin connections shown are for LM111H in 8-lead TO-5 hermetic package

FIGURE 1. Improved Positive Feedback



Pin connections shown are for LM111H in 8-lead TO-5 hermetic package

FIGURE 2. Conventional Positive Feedback

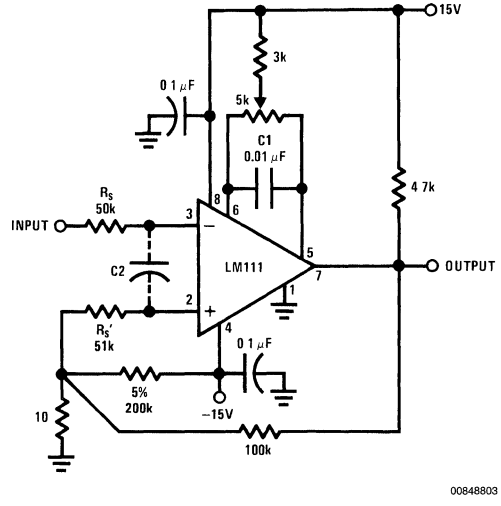


FIGURE 3. Positive Feedback with High Source Resistance

Precision Reference Uses Only Ten Microamperes

National Semiconductor
Linear Brief 41
Hooman Hashemi

Increasing interest in battery-operated analog and digital circuitry in recent years has created the need for a micro-power voltage reference. In particular, the reference should draw 10 µA or less and operate from a single 5V supply. These requirements eliminate zener diodes which tend to have unpredictable temperature drift and are noisy at low currents and low voltages. One possibility is the LM103 series of punch-through diodes which have break-down voltages of 1.8V to 5.6V and operate well at 10 µA. Unfortunately, these devices drift at −5 mV/°C and extra circuitry must be added to create a low-drift reference. Non-linearity in the drift characteristic limits usable drift compensation to about 50 ppm/°C. Variations in slope from device to device can be up to ±0.5 mV/°C, so each reference must be individually corrected for temperature drift in an oven test.

The LM134 current source can provide an interesting solution to the low-power-drain reference problem. This device is a 3-terminal current source which has a compliance of 1V to 40V and is programmable over a current range of 1 µA to 10 mA. Current is determined by an external resistor. With a zero drift resistor, the LM134 current is directly proportional to absolute temperature (°K). Untrimmed accuracy of the current is ±3%, but the key to the success of the LM134 is that initial errors are gain errors which are trimmed to zero when the external resistor is adjusted. Independent of initial current, if the current is adjusted to 298 µA at T = 25°C (298°K), all devices will have a current dependence of 1 ±0.01 µA/°C.

A voltage reference can be made by combining the positive temperature coefficient of the LM134 with the negative TC of a forward-biased diode. The IC terminology for such a reference is "bandgap reference" because the total voltage of the reference is equal to the extrapolated (0°K) bandgap voltage of silicon. An important characteristic of bandgap references is that the zero TC voltage is independent of diode current even though the diode voltage and TC are not. This means that by adjusting the total voltage of the reference to a fixed value, T.C. will be adjusted to near zero at the same time. The zero TC voltage for most bandgap references falls between 1.20V and 1.28V.

The circuit in *Figure 1* is a micropower reference using the LM134 and an MPSA43 transistor connected as a diode with collector-base shorted. A transistor is used in place of a diode because the transistor characteristics as a double-diffused structure are more consistent than a diode. In particular, the emitter-biased voltage drift of wide-base high-voltage transistors connected as diodes is very linear with temperature.

In *Figure 1*, the LM134 controls the voltage between its R and V^- terminals to ≈ 64 mV. About 5.5% of the current out of the R terminal flows out of the V^- terminal. The total current flowing through R2 is then determined by 67.7 mV/R1. Output voltage is the sum of the diode voltage, plus the voltage across R2, plus 64 mV. The voltage TC across R2 and the 64 mV is positive and directly proportional to absolute temperature while the diode TC is negative. The overall TC of the output will be near zero (< 50 ppm/°C) when the output is adjusted to 1.253V by trimming R2. To obtain this level of performance, R1 and R2 must track well over temperature. 1% metal film resistors are suggested.

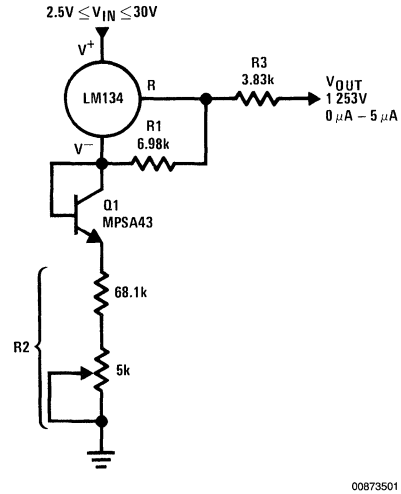


FIGURE 1.

For optimum results with a single point adjustment of voltage and temperature coefficient, an additional error term must be accounted for. Internal to the LM134 are low I_{dss} FETs used for starting the control loop. This FET current adds directly to the V^- pin current and therefore creates an additional output voltage equal to $(I_{dss})(R2)$. Typical I_{dss} is 200 nA, causing V_{OUT} to be 14 mV high. Temperature coefficient of I_{dss} is low, typically 0.1%/°C. For best results in a single point adjustment, V_{OUT} should be adjusted to 1.253V + I_{dss} (R2). I_{dss} can be easily measured by open circuiting R1 and measuring the drop across R2. The resulting voltage must be divided by 2 due to an internal action which causes 2 I_{dss} to flow when no current flows from the R pin. Example: with R1 open, 32 mV is measured across R2. Set V_{OUT} equal to 1.253V + 32 mV/2 ≙ 1.269V. Even lower TC can be obtained by measuring the output at 2 temperatures and using the following formula to calculate the exact zero TC output voltage for each reference.

$$V_{OUT}\,(0\ TC) = V1 - \frac{T1\,(V2 - V1)}{T2 - T1}$$

Where:

V1 = Output voltage at T1

V2 = Output voltage at T2

T = Absolute temperture (°K)

The limitation on temperature drift after a 2 point calibration is non-linearity This reference circuit has a non-reducible bow error of ≈ 10 ppm/°C over a temperature range of −25°C to +100°C and ≈5 ppm/°C from 0°C to +70°C. At 125°C, leakage creates significant error, causing the output voltage to droop about 5 mV.

Noise of the reference consists primarily of theoretical shot noise current from the LM134. At the 10 µA level, this is about $6\ pA/\sqrt{Hz}$ rms from 10 Hz to 10 kHz. Total output noise would be $0.4\ \mu V/\sqrt{Hz}$ rms over this frequency range, except that C1 bypasses most of the noise above 2 kHz. Measured output noise was 25 µVrms over a 10 Hz to 10 kHz bandwidth with C1 = 1000 pF. Larger values of C1 may be used if lower broadband noise is needed Low frequency noise is about 25 µV peak-to-peak from 0.1 Hz to 10 Hz.

The LM134 has a negative output resistance at the R pin when resistance is inserted in series with the V^- pin. The value of this negative resistance is approximately $-R_X/19$, where R_X is the equivalent resistance from V^- to ground. In this reference circuit R_X is 72 kΩ, yielding a negative output resistance of 3.8 kΩ. Resistor R2 sums with this resistance to give the reference a net zero output resistance (±400Ω). Loading should be limited to about 5 µA. Line regulation for the reference is typically less than 0.5 mV with an input voltage of 5V ±2V. Minimum input voltage for a 2 mV drop in output voltage is 2.5V at −55°C, 2.4V at 25°C and 2.3V at 125°C.

Although this reference was designed for ultra-low operating current, there is no reason that it cannot be used at higher current levels as well. All resistor values are simply scaled downward. Higher operating current will give lower output resistance, more drive capability, less sensitivity to FET I_{dss}, lower noise, and less droop at 125°C.

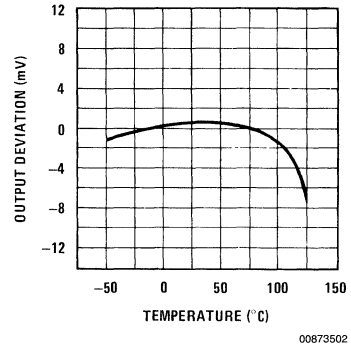


FIGURE 2. Output Voltage Drift

Get Fast Stable Response From Improved Unity-Gain Followers

National Semiconductor
Linear Brief 42
Robert A. Pease

In many applications, a unity-gain follower (e.g. any operational amplifier with tight feedback to the inverting input) may oscillate or exhibit bad ringing when required to drive heavy load capacitance. For example, the LM110 follower will normally drive a 50 pF load capacitor, but will not drive 500 pF, because the open-loop output impedance is lagged by such a large capacitive load. The frequency at which this lag occurs is comparable to the gain-bandwidth product of the amplifier, and when the phase margin is decreased to zero, oscillation occurs.

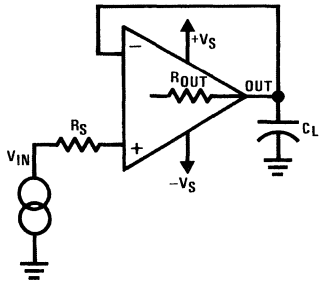


FIGURE 1. Unity-Gain Follower Attempting to Drive Capacitive Load

While the solution to this problem is not widely known, an analysis of the general problem shown in *Figure 2* can lead to a useful approach. It is generally known that increasing the noise gain of an op amp's feedback network will improve tolerance of capacitive load. In *Figure 2*, adding a resistor R2 $\cong R_F/10$ will do this. (A moderate capacitor C2 is usually inserted in series with R2, to prevent the DC noise gain from increasing also—to avoid degrading DC offset, drift and inaccuracy.) If the op amp has a 1 MHz gain bandwidth product, and R1 = R_F, the closed-loop frequency response will be ½ MHz. Adding R2 = $R_F/10$ will drop the closed-loop frequency response to 90 kHz, where the amplifier can usually tolerate a much larger C_L;

$$\text{Noise Gain} = \frac{R_F}{R1} + \frac{R_F}{R2} + 1 \text{ (AC)}$$

$$\text{Noise Gain} = \frac{R_F}{R1} + 1 \text{ (DC)}$$

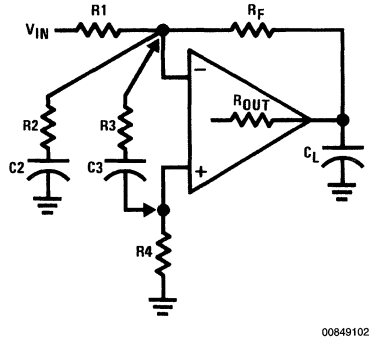


FIGURE 2. Stabilizing an Operational Amplifier for Capacitive Load

A similar result will occur if you install R3 and C3, instead of R2. Now the (AC) noise gain will be:

$$1 + \frac{R4}{R3} + \frac{R_F}{R3} + \left(\frac{R_F}{R1}\right)\left(\frac{R3 + R4}{R3}\right)$$

As a simplification, if R1 is an open circuit, the AC noise gain will be: $(R4/R3 + R_F/R3 + 1)$. Now it can be seen that noise gain can be raised by having a low value of R3 and a high value of R4 or R_F (or both).

In particular, where R_F is required to be 0Ω, as in a follower, the noise gain can be raised by adding a large R4 and a

small R5, as shown in *Figure 3*. If R_S is low, the AC noise gain will be R4/R5 + 1. (If R_S is large and constant, R4 may be unnecessary, and the noise gain would then be R_S/R5 + 1.) For LM110/LM310's R4 = 10 kΩ is recommended and when R5 = 3.3 kΩ, C5 = 200 pF, the LM110 will stably drive C_L up to 600 pF.

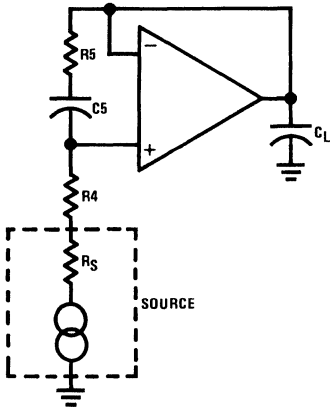


FIGURE 3. Stabilizing a Unity-Gain Follower for Capacitive Load

Another application of this technique is for making a fast follower with a high slew rate. An LF356 is specified as a follower, but an LF357 must be applied at an "A_V = 5" minimum, because it has been "decompensated" with a smaller internal capacitor. Most people do not realize how easy it is to apply an LF357 as a follower. In *Figure 4*, an LF357 will have fast, stable response just like an LF356 does, when R_S is < 1 kΩ, but it will have a 50V/μs slew rate (typical) vs. 12V/μs for an LF356.

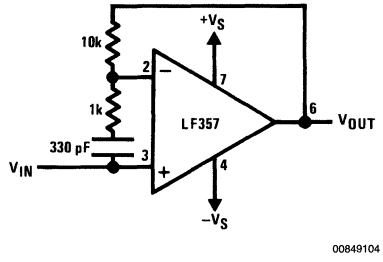


FIGURE 4. Unity-Gain Follower With Fast Slew Rate

Similarly, an LM348 is a fast decompensated quad op amp. Its bipolar input stage has a finite bias current, 200 nA max. For best results, the resistance which makes up the noise gain should be put equally in the **plus** and **minus** input circuits, as shown in *Figure 5*. The LM349 can slew at 2V/μs typical, and is much faster for handling audio signals without distortion than the LM348 (which at 0.5V/μs is only as fast as an ordinary LM741). The same approach can be used for an LM101 with a 5 pF damping capacitor. While these circuits give faster slewing, the bandwidth may degrade if the source impedance R_S increases. Also, when the AC noise gain is raised, the AC noise will also be increased. While most modern op amps have low noise, a noise gain of 10 may make a significant increase in output noise, which the user should check to insure it is not objectionable.

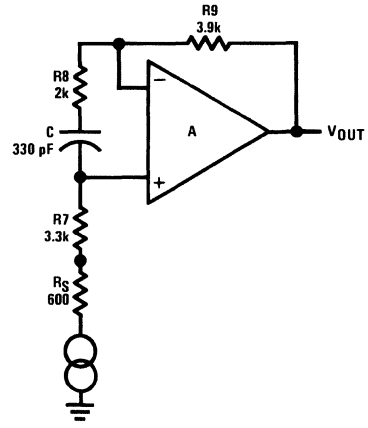


FIGURE 5. Application of Fast Follower With Balanced Resistors, R9 = R7 + R_S, A = 1/4 LM349 (or LM101 with 5 pF Capacitor)

If the series capacitor is much larger than necessary, noise will be increased more than necessary. In general, choose the C5 for *Figure 3*, (e.g.) per these guidelines: (where f_V = unity-gain bandwidth of op amp)

$$\text{C5 Min} = \frac{4 \bullet \left(1 + \frac{R4}{R5}\right)}{2\pi R5 \bullet f_V} = \frac{R4 + R5}{\frac{\pi}{2} \bullet f_V \bullet (R5)^2}$$

For best results, choose the design center value of C5 to be 2 or 3 times C5 min.

Get More Power Out of Dual or Quad Op-Amps

National Semiconductor
Linear Brief 44
Bob Pease

Although simple brute-force paralleling of op-amps is a bad scheme for driving heavy loads, here is a good scheme for dual op-amps. It is fairly efficient, and will not overheat if the load is disconnected. It is *not* useful for driving active loads or nonlinear loads, however.

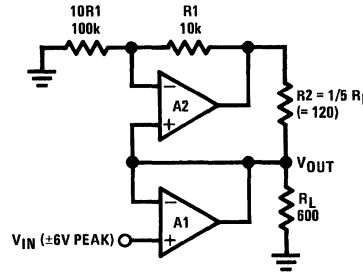
In *Figure 1*, an LF353N mini-DIP can drive a 600Ω load to ±9V typical (±6V min guaranteed) and will have only a 47°C temperature rise above free air. If the load R is removed, the chip temperature will rise to +50°C above free air. Note that A2's task is to drive half of the load. A1 could be applied as a unity-gain follower *or* inverter, or as a high-gain or low-gain amplifier, integrator, etc.

While *Figure 1* is suitable for sharing a load between 2 amplifiers, it is not suitable for 4 or more amplifiers, because the circuit would tend to go out of control and overheat if the load is disconnected.

Instead, *Figure 2* is generally recommended, as it is capable of driving large output currents into resistive, reactive, nonlinear, passive, or active loads. It is easily expandable to use as many as 2 or 4 or 8 or 20 or more op-amps, for driving heavier loads.

It operates, of course, on the principle that every op-amp has to put out the same current as A1, whether that current is plus, minus, or zero. Thus if the load is removed, all amplifiers will be unloaded together. A quad op-amp can drive 600Ω to ±11 or 12 volts. Two quads can put out ±40 mA, but they get only a little warm. A series R-C damper of 15Ω in series with 0.047 µF is useful to prevent oscillations (although LM324's do not seem to need any R-C damper).

Of course, there is no requirement for the main amplifier to run only as a unity-gain amplifier. In the example shown in *Figure 3*, A1 amplifies a signal with a gain of +10. A2 helps it drive the load. Then A3 operates as a unity-gain inverter to provide V2 = –V1, and A4 helps it drive the load. This circuit can drive a floating 2000Ω load to ±20V, accurately, using a slow LM324 or a quick LF347.



A1, A2 = 1/2 LM747 or 1/2 LF353 or any op-amp

FIGURE 1. A1 and A2 Share the Load

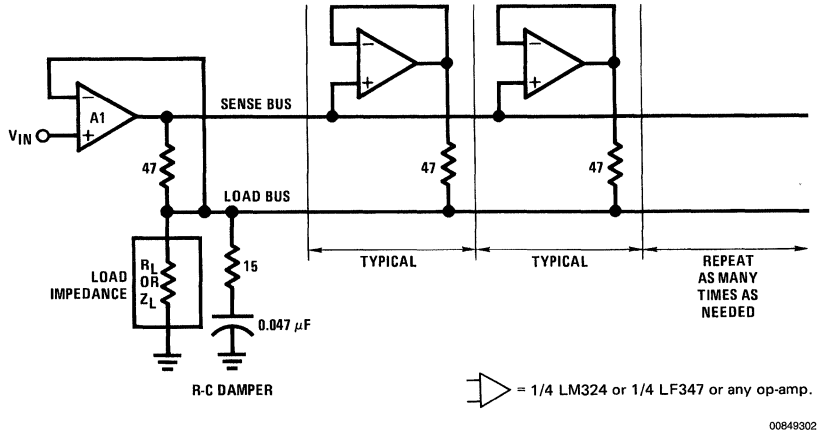


FIGURE 2. Improved Load-Sharing Circuit

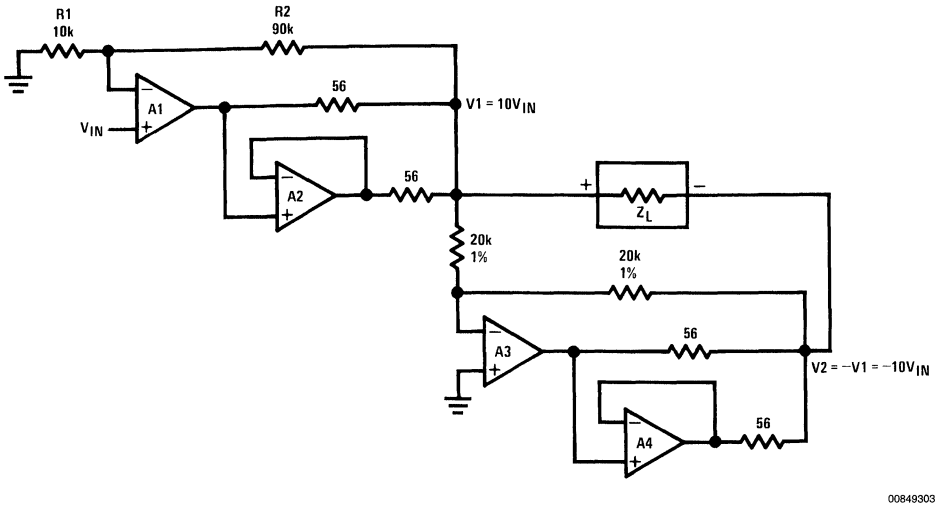


FIGURE 3. Typical Application of Load-Sharing

Simple Voltmeter Monitors TTL Supplies

National Semiconductor
Linear Brief 48
Michael Maida

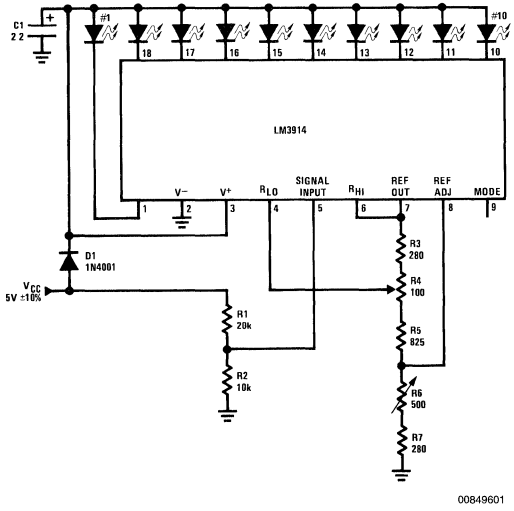
Using a National Semiconductor LM3914 bar/dot display driver chip, a few resistors and some LEDs, a simple expanded-scale voltmeter is easily constructed. Furthermore, it runs from the same single 5V ± 10% supply it monitors and can provide TTL-compatible undervoltage and overvoltage warning signals.

The complete circuit is shown in *Figure 1* Resistors R1 and R2 attenuate V_{CC} by a factor of three at the LM3914 signal input, ensuring proper biasing of the IC with V_{CC} as low as 4V The IC's internal reference sets the voltage across the series combination of R3, R4 and R5 at 1.25V, establishing a reference load current of about 1 mA. This current is joined by the small, constant current from the reference adjust pin (75 µA, typ) and flows to ground through R6 and R7, developing a voltage drop. Adjusting R6 varies this voltage drop and, consequently, the voltage at pin 7, nominally 1.803V (= 5.41V/3).

Pin 7 is connected to the top of the LM3914's internal ten-step voltage divider (pin 6) The bottom of this divider (pin 4) is connected to the center tap of potentiometer R4. By varying the pot setting this voltage can be set to 1.47V (= 4.41V/3) without significantly affecting the potential at pin 7. The optional diode D1 protects against damaging the IC by connecting the leads backwards

In operation, the LM3914's ten internal voltage comparators compare the signal input, $V_{CC}/3$, to the reference voltage on the divider, lighting each successive LED for every 100 mV increase in V_{CC} above 4.5V as shown The LM3914 regulates the LED currents at 10 times the reference load current, here about 10 mA, so external current-limiting resistors are not required. With pin 9 left open circuit, the LM3914 functions in Dot mode (only one LED on at a time). If desired, a Bar mode display could be obtained by connecting pin 9 to V_{CC}, but the dot display seems more suitable in this application.

To calibrate, set V_{CC} at 5.41V and adjust R6 until LED #9 and LED #10 are equally illuminated (A built-in overlap of about 1 mV ensures all LEDs won't go out at a threshold point) There's no need to vary the system supply voltage to perform this adjustment Instead, disconnect R1 from V_{CC} and connect it to an accurate reference. Then, at 4.5V, adjust R4 until LED #1 just barely turns on. There is a slight interaction caused by the finite resistance (10k, typ) of the LM3914's voltage divider, so that repeating the above procedure once is advised.



V_{CC}(V)	LED Illuminated
4.51-4.60	#1
4.61-4.70	#2
4.71-4.80	#3
4.81-4.90	#4
4.91-5.00	#5
5 01-5.10	#6
5.11-5.20	#7
5.21-5.30	#8
5.31-5.40	#9
5.41-up	#10

All fixed resistors are ± 1% tolerance

All potentiometers are ± 20%

C1: 2.2 µF tantalum or 10 µF aluminum electrolytic

FIGURE 1. 5V Power Supply Monitor

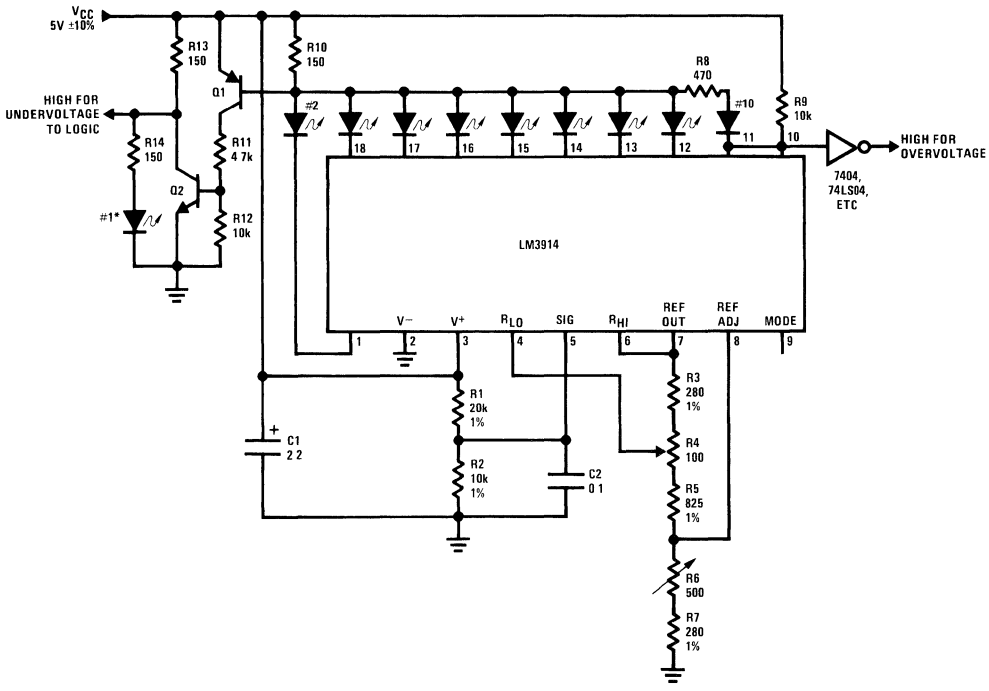
The LED driver outputs can directly drive a TTL gate, so that the LED #1 and LED #10 outputs may be used for undervoltage and overvoltage warning signals. These may be used to initiate a soft shutdown or summon an operator, for example. The interfacing circuitry is shown in *Figure 2*. The 470Ω resistor R8 ensures that the LM3914 output will saturate to provide the proper TTL low level. Pull-up resistor R9 provides the logic high level.

In the previous circuit the undervoltage LED goes out when V_{CC} is less than 4.51V, a deficiency that is corrected here, Transistors Q1 and Q2 shut off LED #1 whenever any other LED is turned on by the LM3914. Q2's output will directly drive TTL.

Calibration procedure is the same as before. The LM3914 output thresholds have been shifted up by 100 mV and

output #10 is or-tied with output #9 Other outputs may be wire-or'd together if 100 mV resolution is not necessary If desired, the outputs can be color coded by making LED #1 and LED #10 red, LED #2 and LED #9 amber, and the rest of the LEDs green to ease interpretation

This circuit is useful where quick and easy voltage adjustments must be made, such as in the field or on the production line. The circuit's low cost makes it feasible to incorporate it into the system, where the overvoltage and undervoltage warning signals provide an attractive extra. Of course, these techniques can be used to monitor any higher voltages, positive or negative.



[1]LED #1 is illuminated for 3V ≤ V_{CC} ≤ 4 51V

Q1 2N3906, 2N2907 or similar

Q2 2N3904, 2N2222 or similar

FIGURE 2. Power Supply Monitor with TTL Interface and Extended Undervoltage Range

A Low-Noise Precision Op Amp

National Semiconductor
Linear Brief 52
Robert A. Pease

It is well known that the voltage noise of an operational amplifier can be decreased by increasing the emitter current of the input stage. The signal-to-noise ratio will be improved by the increase of bias, until the base current noise begins to dominate. The optimum is found at:

$$I_{e(optimum)} = \frac{KT}{q} \frac{\sqrt{h_{FE}}}{r_s}$$

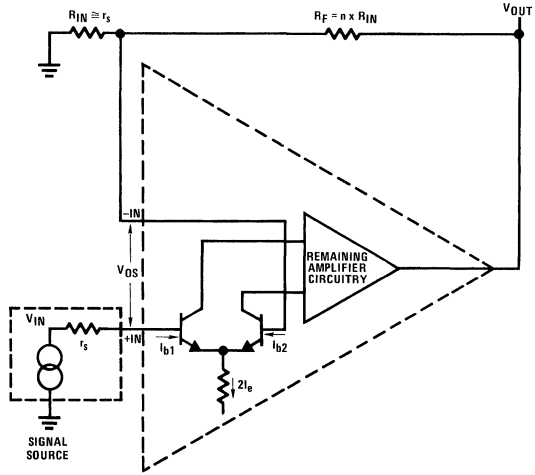
where r_s is the output resistance of the signal source. For example, in the circuit of *Figure 1*, when r_s = 1 kΩ and h_{FE} = 500, the I_e optimum is about 500 µA or 560 µA. However, at this rich current level, the DC base current will cause a significant voltage error in the base resistance, and even after cancellation, the DC drift will be significantly bigger than when I_e is smaller. In this example, I_b = 1 µA, so $I_b \times r_s$ = 1 mV. Even if the I_b and r_s are well matched at each input, it is not reasonable to expect the $I_b \times r_s$ to track better than 5 or 10 µV/°C versus temperature.

A new amplifier, shown in *Figure 2*, operates one transistor pair at a rich current, for low noise, and a second pair at a much leaner current, for low base current. Although this looks like the familiar Darlington connection, capacitors are added so that the noise will be very low, and the DC drift is very good, too. In the example of *Figure 2*, Q2 runs at I_e = 500 µA and has very low noise. Each half of Q1 is operated at 11 µA = I_e. It will have a low base current (20 nA to 40 nA typical), and the offset current of the composite op amp, I_{b1}–I_{b2}, will be very small, 1 nA or 2 nA. Thus, errors caused by bias current and offset current drift vs. temperature can be quite small, less than 0.1 µV/°C at r_s = 1000Ω.

The noise of Q1A and Q1B would normally be quite significant, about 6 $nV/\sqrt{Hz}$, but the 10 µF capacitors completely filter out the noise. At all frequencies above 10 Hz, Q2A and Q2B act as the input transistors, while Q1A and Q1B merely buffer the lowest frequency and DC signals.

For audio frequencies (20 Hz to 20 kHz) the voltage noise of this amplifier is predicted to be 1.4 $nV/\sqrt{Hz}$, which is quite small compared to the Johnson noise of the 1 kΩ source, 4.0 $nV/\sqrt{Hz}$. A noise figure of 0.7 dB is thus predicted, and has been measured and confirmed. Note that for best DC balance R6 = 976Ω is added into the feedback path, so that the total impedance seen by the op amp at its negative input is 1 kΩ. But the 976Ω is heavily bypassed, and the total Johnson noise contributed by the feedback network is below ½ $nV/\sqrt{Hz}$.

To achieve lowest drift, below 0.1 µV/°C, R1 and R2 should, of course, be chosen to have good tracking tempco, below 5 ppm/°C, and so should R3 and R4. When this is done, the drift referred to input will be well below 0.5 µV/°C, and this has been confirmed, in the range +10°C to +50°C.



$$V_{OUT} \cong (n+1)\, V_{IN} + V_{OS} \times (n+1) + (I_{b2} - I_{b1}) \times r_s \times (n+1) + V_{noise} \times (n+1) + I_{noise} \times (r_s + R_{IN}) \times (n+1)$$

FIGURE 1. Conventional Low-Noise Operational Amplifier

Overall, we have designed a low-noise op amp which can rival the noise of the best audio amplifiers, and at the same time exhibits drift characteristics of the best low-drift amplifiers. The amplifier has been used as a precision pre-amp (gain = 1000), and also as the output amplifier for a 20-bit DAC, where low drift and low noise are both important.

To optimize the circuit for other r_s levels, the emitter current for Q2 should be proportional to $1/\sqrt{r_s}$. The emitter current of Q1A should be about ten times the base current of Q2A. The base current of the output op amp should be no more than 1/1000 of the emitter current of Q2 The values of R1 and R2 should be the same as R7.

Various formulae for noise:

Voltage noise of a transistor,

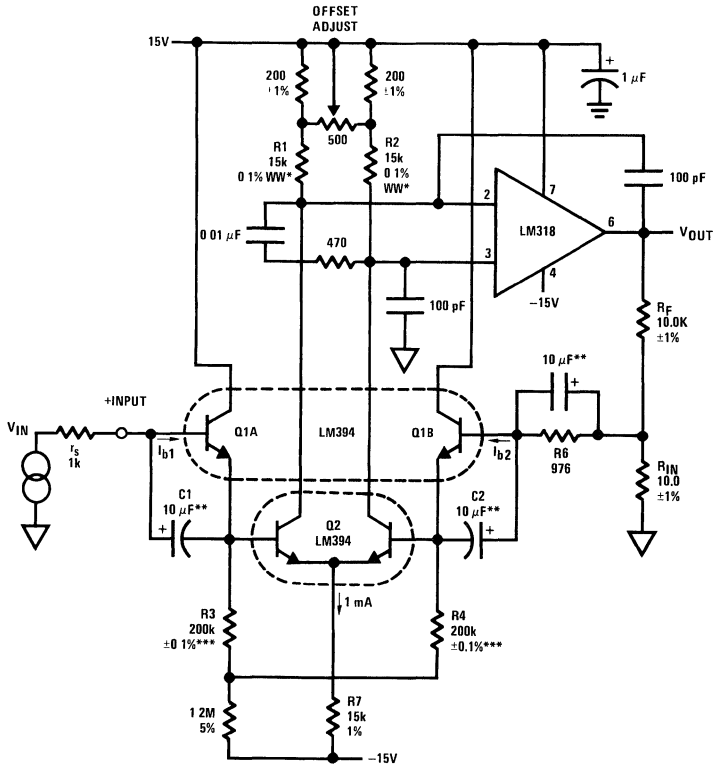
$$\text{per } \sqrt{\text{Hz}},\ e_n = KT\sqrt{\frac{2}{qI_C}}$$

Current noise of a transistor,

$$\text{per } \sqrt{\text{Hz}},\ i_n = \sqrt{\frac{2qI_C}{h_{FE}}}$$

Voltage noise of a resistor, per $\sqrt{\text{Hz}}$, $e_n = \sqrt{4\,KTR_s}$

For a more complete analysis of low-noise amplifiers, see AN-222, "Super Matched Bipolar Transistor Pair Sets New Standards for Drift and Noise", Carl T. Nelson.



*Tracking TC < 5 ppm/°C

**Solid tantalum

***Tracking TC < 5 ppm/°C, Beckman 694-3-R100K-D or similar

FIGURE 2. New Low-Noise Precision Operational Amplifier as Gain-of-1000 Pre-Amp

Section 3

High Speed Amplifiers and Signal Conditioning: Device Information

Section 3 Contents

National Semiconductor

CLC to LMH Conversion Table

The following table shows the list of LMH products already released For the complete conversion roadmap please visit www.national.com/see/LMH2CLC.

* Replacement Device column shows closest equivalent to CLC NSIDs

CLC NSIDs	Replacement Device*	Pin Compatible?	Key Features
CLC109	LMH6559	YES	Single Closed Loop Buffer
CLC110	LMH6559	YES	Single Closed Loop Buffer
CLC111	LMH6559	YES	Single Closed Loop Buffer
CLC114	LMH6560	YES	Quad Closed Loop Buffer
CLC115	LMH6560	YES	Quad Closed Loop Buffer
CLC400	LMH6714	NO	No offset adjustment
CLC401	LMH6714	YES	Single Current Feedback Amplifier
CLC402	LMH6714	YES	Single Current Feedback Amplifier
CLC404	LMH6714	YES	Single Current Feedback Amplifier
CLC405	LMH6720	YES	Single Current Feedback Amplifier + Shutdown
CLC406	LMH6714	YES	Single Current Feedback Amplifier
CLC407	LMH6559	NO	Programmable Gain Buffer vs. Opamp or Buffer
CLC409	LMH6702	YES	Single Current Feedback Amplifier
CLC410	LMH6720	YES	Single Current Feedback Amplifier + Shutdown
CLC411	LMH6720	YES	Single Current Feedback Amplifier + Shutdown
CLC412	LMH6715	YES	Dual Current Feedback Amplifier
CLC414	LMH6722	YES	Quad Current Feedback
CLC415	LMH6722	YES	Quad Current Feedback
CLC416	LMH6715	YES	Dual Current Feedback Amplifier
CLC417	LMH6718	YES	Dual Programmable Gain Buffer
CLC425	LMH6624	YES	Single VFB, No Adjustable Current Pin on SOIC-8
CLC428	LMH6628	YES	Dual Voltage Feedback Amplifier
CLC430	LM6181 or LM7171	NO	Single Current Feedback Amplifier
CLC431	LM7372	NO	No Disables, different package
CLC432	LM7372	YES	Dual Current Feedback Amplifier
CLC446	LMH6705	YES	Single Current Feedback Amplifier
CLC449	LMH6705	YES	Single Current Feedback Amplifier
CLC505	LMH6732	YES	Single Current Feedback Amplifier + Shutdown
CLC5612	LMH6718	YES	Dual Programmable Gain Buffer
CLC5623	LMH6683	YES	Voltage vs. Current Feedback
CLC5632	LMH6718	YES	Dual Programmable Gain Buffer
CLC5633	LMH6683	YES	Voltage vs. Current Feedback
CLC5644	LMH6722	YES	Quad Current Feedback Amplifier
CLC5654	LMH6722	YES	Quad Current Feedback Amplifier
CLC5665	LM6181 or LM7171	NO	Single Current Feedback Amplifier
CLC5801	LMH6624	YES	Single Voltage Feedback Amplifier
CLC5802	LMH6628	YES	Dual Voltage Feedback Amplifier
LM7131	LMH6642	YES	Single Voltage Feedback Amplifier

LM6361/LM6364/LM6365 Fast VIP™ Op Amps Offer High Speed at Low Power Consumption

National Semiconductor
Application Note 549
Wanda Garrett

The LM6361/LM6364/LM6365 family of op amps are wide-bandwidth monolithic amplifiers which offer improved speed and stability over many other op amps, at low cost, with little-to-no penalty in power supply consumption.

These advantages are due to a new process, developed by National Semiconductor, which provides lateral PNP transistors with nearly the gain and speed characteristic of NPN transistors—while the NPNs maintain their usual high performance. This allows the use of both NPN and PNP transistors in the signal path, where previously the PNP transistors severely limited the speed of linear devices. (Standard lateral PNPs have 1/10th the gain and 1/200th the bandwidth of standard NPN transistors.)

Traditional high-speed op amps often either used all-NPN circuitry (which usually severely limits the input, output, and power supply voltage ranges); used feed-forward techniques (which reduce stability); or resorted to costly hybrid design. Amplifiers made from this new process (dubbed VIP, for "Vertically-Integrated PNP") operate from a 5V to 30V (total) supply voltage, and have standard input and output voltage ranges. In addition, they require comparatively little supply current, and are available in standard 8-pin dual-in-line packages.

The first devices produced with this process are three op amps—each with the same basic design but compensated to different degrees. The schematic of the unity-gain-stable LM6361 (see *Figure 1*) has a simple but effective form. The VIP transistors can now be used in the signal path, so a fairly traditional NPN differential input stage can be followed by a folded cascode wide-bandwidth gain stage. The input stage uses emitter-degeneration resistors to reduce its transconductance (G_m). The bandwidth of the amplifiers is then set by the ratio of G_m to compensation capacitance. This also determines the stability of the amplifier.

The compensation capacitance is stray capacitance (about 0.5 pF) which is seen lumped together at the front of the output stage. This output stage has a classic AB design, but since it contains a VIP transistor it has the speed necessary for a high speed amplifier. Additional capacitance on the output effectively increases the total compensation capacitance, increasing the stability of the amplifier but also reducing the bandwidth. This "compensation" is not ideal, however, so transient response may be degraded.

The step response (*Figure 2*) demonstrates the stability of the LM6361. The amplifier was set up as a unity-gain follower, with a 6V input step. The output has a small overshoot and settles quickly to its final value. This well-behaved response is due to the simplicity of the compensation, which can be seen in the frequency response (*Figure 3*). It shows a smooth one-pole rolloff beyond 50 MHz, where the gain has dropped to unity, with a phase margin of 45°; the next pole is introduced after 100 MHz

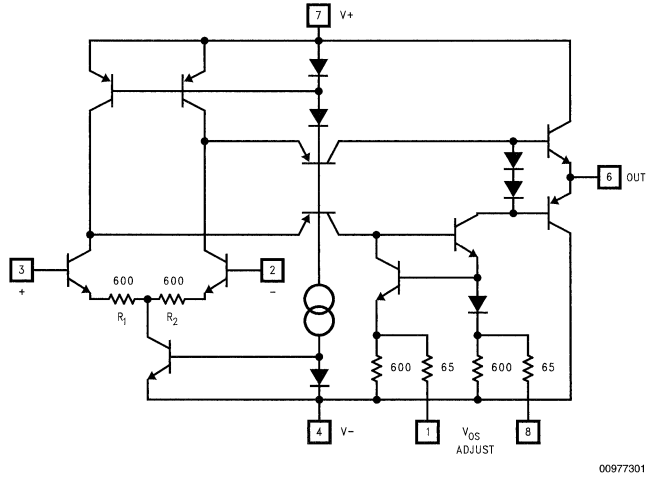


FIGURE 1. LM6361 Simplified Schematic. For LM6364, R1 and R2 are 150Ω; for LM6365, R1 and R2 are Omitted.

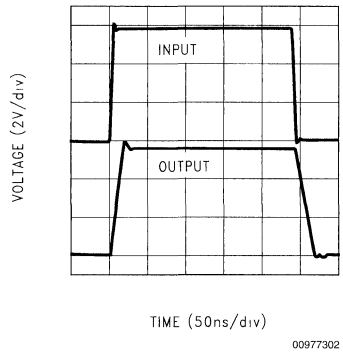


FIGURE 2. Step Response of LM6361 in Unity-Gain (Follower) Configuration

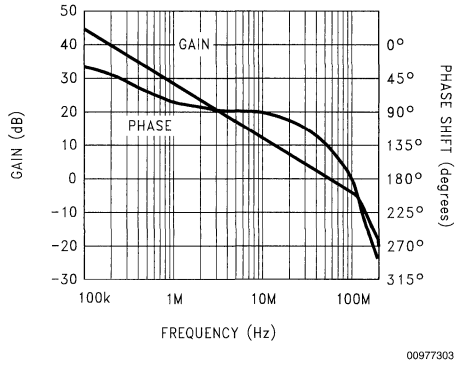


FIGURE 3. Frequency Response of LM6361 (Closed Loop Gain = 45 dB)

The LM6364 and LM6365 are based on the LM6361 design The LM6361's 600Ω emitter degeneration resistors are reduced to 150Ω in the 6364 to produce an op amp with gain-bandwidth product of 175 MHz, stable to a minimum gain of 5 In the 6365 the resistors are eliminated altogether, for a GBW of 725 MHz and minimum gain of 25. All three devices have slew rates guaranteed (and 100% tested) to be over 200 V/µs (the slew rates are typically 300 V/µs)

Since the emitter degeneration resistors contribute to offset voltage and input voltage noise, the device with the widest bandwidth also has the best DC specs. The high gain of the transistors used in the common design, combined with the configuration used, give these op amps their high speed without consuming a lot of power Supply current is guaranteed to be less than 6.8 mA (with ±15V supplies) for each of the three devices.

The LM6361, LM6364, and LM6365 are guaranteed for operation over the commercial temperature range (0°C to 70°C). In addition, there are two other versions of each amplifier available· LM62XX, rated for operation over the industrial –25°C to +85°C range, and delivering improved DC input specifications over the LM63XX parts; and LM61XX, which is rated for the military temperature range (–55°C to +125°C), with the same improved DC specifications as the industrial versions

These VIP amplifiers were optimized for high AC performance at low power consumption, while offering an ease of use previously found only in low speed parts They are expected to bring a new level of performance and affordability to applications such as filtering, 8-bit data acquisition, video and communications, and general high frequency signal processing

General High-Speed Circuit Design Techniques

The LM6361/LM6364/LM6365 op amp family can tolerate circuit-building techniques appropriate for op amps of much lower bandwidth However, for best performance, any high-speed circuit (and many DC precision circuits) should be built using what is often called "good RF design." Power supply bypassing is very important: most op amps will require 0 01 µF to 0.1 µF good ceramic capacitors at each power supply pin, and an additional 2.2 µF to 10 µF tantalum nearby for extra noise reduction These VIP op amps do not require as much bypassing as other op amps in their speed class, for most applications, 0.01 µF bypass capacitors are adequate. However, their stability (especially that of the wider gain-bandwidth LM6365) is enhanced when good bypassing is used.

Power supply bypassing is added to negate the effects of lead inductance from the power supply wires. This inductance causes "glitches" on the power supply lines every time the op amp has to deliver power to a transient load, these glitches normally work their way into other sensitive parts of your circuit. In addition, the inductance can create small tank circuits with stray capacitance, which often will cause a marginally stable circuit to oscillate

For these reasons, keep all leads short (especially to the input pins), and make sure the ground paths are low-impedance, especially where larger currents will be flowing Minimize stray capacitance (especially in the forms of sockets and parallel board traces) Stray capacitance allows signal coupling from one pin or input or lead to another, which can cause noise and/or oscillation.

All of the circuits shown here were built on copper-clad board (used as a ground plane), with the op amps in sockets for convenience—except for the input and output pins, which were soldered directly into the circuits

1 MHz Voltage-to-Frequency Converter

The classic charge-pump voltage-to-frequency converter is limited in maximum frequency by the integrator amplifier. For example, op amps with 1 MHz gain-bandwidth products limit converters to a maximum frequency of about 10 kHz (for 0 1% accuracy or better). Higher-speed converters (500 kHz and up) must either incorporate the very-high-speed (usually hybrid) op amps, or turn to another, more complex, design

The LM6365 can be used in the charge-pump V-to-F to produce a 1 MHz (at 10V) output signal, as shown in *Figure 4.* Offset and full-scale trims allow more than two-decade operation with 0.1% linearity, as shown in *Figure 5.* Careful

1 MHz Voltage-to-Frequency Converter (Continued)

power supply bypassing and layout are important to reduce noise and stray capacitance which will degrade performance.

The wide-bandwidth nature of the LM6365 provide the fast switching necessary for 1 MHz operation, with little degradation in accuracy for inputs up to 11V (10% overrange). Likewise, the 0.1% linearity holds for inputs down to 50 mV.

The circuit gain is described by the equation:

$$\frac{f}{V_{IN}} = 1/(2 \cdot V_z \cdot R_{in} \cdot C_{fb})$$
$$= 100\ kHz/V$$

where V_Z is the output clamp voltage, 3.5V, and R_{in} and C_{fb} are the components noted on the schematic (*Figure 4*).

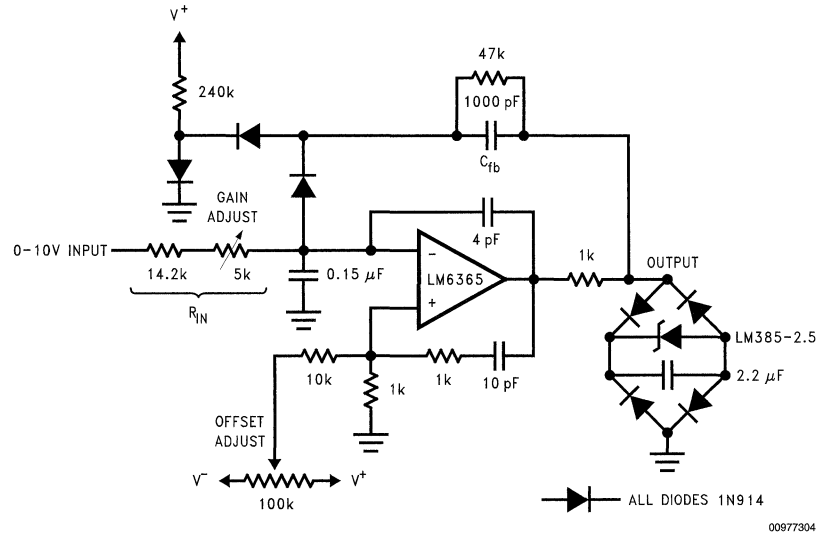


FIGURE 4. 1 MHz V-to-F Converter

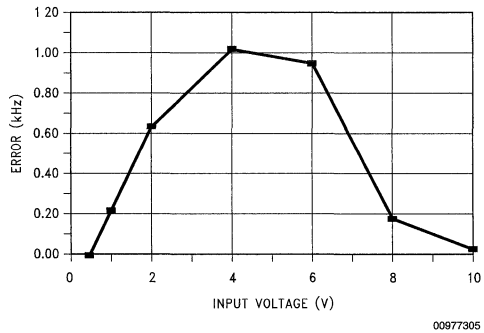


FIGURE 5. Nonlinearity of LM6365 Voltage-to-Frequency Converter (of *Figure 4*) is 0.1%

To calibrate the circuit, first adjust the gain potentiometer until a 10.00V input produces a 1.000 MHz output. Then adjust the offset potentiometer until a 50 mV input produces a 5.0 kHz signal. Repeat adjustments until both ends of the input range produce the correct output frequencies. The 0.15 µF input capacitance improves the linearity of the circuit.

All leads must be kept very short, especially those connected to the inputs of the LM6365, to minimize stray capacitance which affects the gain and linearity. In addition, the LM6365 power supply pins must be bypassed with 4.7 µF tantalum and 0.01 µF ceramic capacitors to keep lead inductance from affecting the circuit's stability.

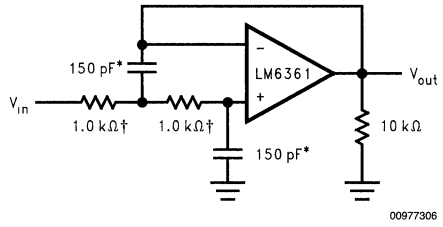
High-Frequency Active Filters

The LM6361 can be used in active filters at frequencies which often require special designs to achieve even adequate performance. For example, even though a 1 MHz low-pass filter could be constructed taking advantage of the natural bandwidth of an op amp such as a 741, the designer would find the cutoff varying with the unit-to-unit variation of 741 bandwidths, and the filter would only have a one-pole slope. A two-pole active filter with good performance at this frequency is difficult to realize with most standard op amps. Either the amplifier's own bandwidth is too low, or in the case of many decompensated fast op amps, the low gain needed for the wide bandwidth may render the amplifier unstable.

High-Frequency Active Filters

(Continued)

However, the LM6361 can easily be used to provide a 1 MHz cutoff with a 2-pole rolloff, as shown in *Figure 6*. And because the cutoff frequency is not set by amplifier bandwidth, but by the R-C network, it can be trimmed for accuracy.



†1% tolerance

*matching determines filter precision

FIGURE 6. 1 MHz Low-Pass Filter

Figure 7 shows the frequency response of the low-pass filter. The gain rolls off at a steady 12 dB/octave until 6 MHz, where the gain is down 35 dB.

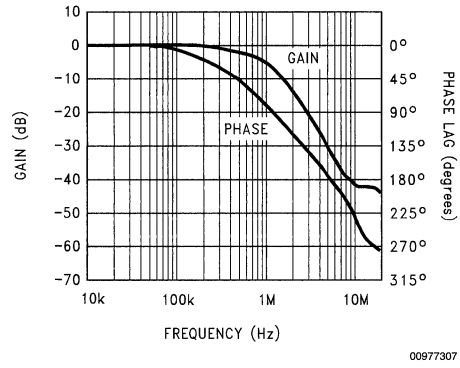


FIGURE 7. Frequency Response of Low-Pass Filter (Reference *Figure 6*)

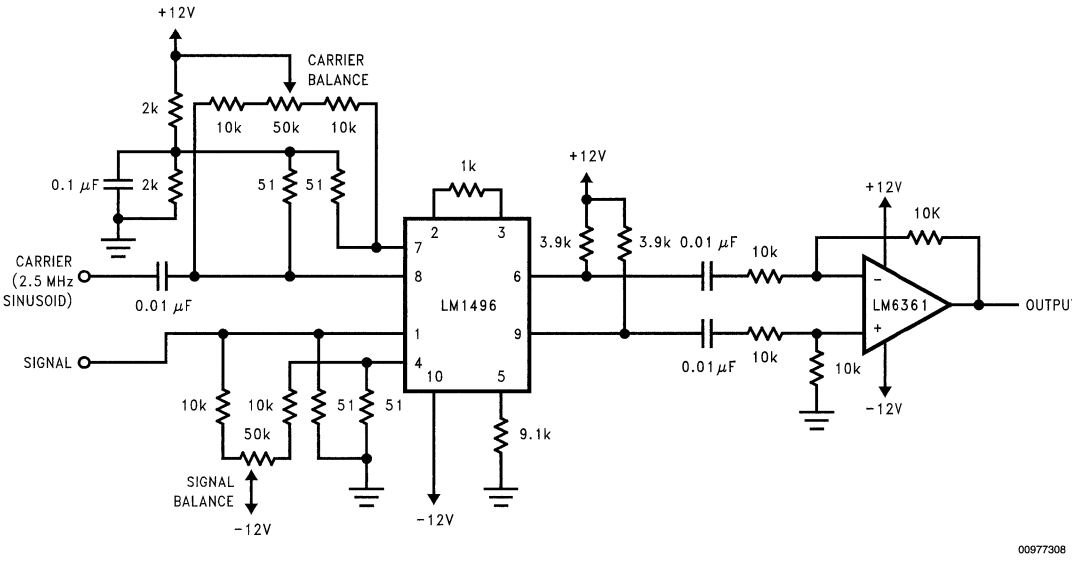


FIGURE 8. Modulator with Single-Ended Output Centered about Ground

Video/Communications Applications

In systems such as some local area networks, where a signal is modulated onto a carrier for transmission, and is demodulated for use, an amplifier may have to pass this multiplexed signal. The carrier frequency depends on the system in which it's used—some LANs have 10 MHz basebands, and radio and other broadcasting systems often use carriers of 10 MHz or less. Signals transmitted may be AM-audio, or perhaps some analog information from a transducer or sensor.

Special video circuits which are often used in these systems, such as the LM1496 modulator/demodulator and LM733/LM592 differential amplifiers, have differential outputs with common-mode voltage several volts above ground. This differential signal may be fine for transmitting on a twisted pair, but for sending through coax or for observation/monitoring, it would be better if it were single-ended. To convert the outputs to a signal which is single-ended, referenced to ground, requires a wide-bandwidth amplifier. Unity-gain stability is helpful if no additional gain is needed, but a less stable amplifier could be used if it is allowed sufficient

Video/Communications Applications (Continued)

noise gain. The LM6361 works well in this circuit, having a bandwidth of 50 MHz at unity gain. When higher gain is required, the LM6364 may be used.

In the circuit of *Figure 8*, an LM1496 is used to modulate an analog signal (lower trace, *Figure 9*) with a 2.5 MHz sine-wave carrier. The output of the LM1496 is a differential signal with a common-mode voltage of 8V. An LM6361 is used to convert this signal to a single-ended one centered about ground (upper trace, *Figure 9*).

The LM1496 requires quite a bit of balancing, using the two potentiometers shown, to obtain the lowest possible distortion. The LM1496 is the dominant source of distortion, which is caused by the application of an unbalanced carrier or modulating signal to the LM1496. The balance of the system can be checked on a scope, but for most accurate measurements a spectrum analyzer should be used.

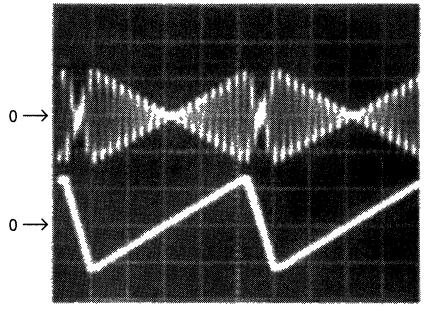


FIGURE 9. Bottom Trace: Signal Input to Multiplexer of *Figure 8* (200 mV/div)
Top Trace: Output of Multiplexer (2 V/div)

Video Amplifier

The LM6361/LM6364/LM6365 series of amplifiers is also suitable for use in video amplifier systems. A key parameter of any amplifier used in video applications, especialy NTSC color television systems, is the differential gain and phase it adds to the circuit (Note 1). An NTSC Vectorscope can be used to check these parameters, analyzing the output of an amplifier whose input is from an NTSC signal generator.

Note 1: Differential gain, in an NTSC color television system, is a change in color subcarrier amplitude due to a change in the luminance signal while hue and saturation of the original signal are held constant In an amplifier, it relates to the variation of closed-loop gain with common-mode input voltage It should be (ideally) zero.

Differential phase is a phase change of the chrominance signal by the luminance signal while the original chrominance signal is held constant. In an amplifier, it relates to the variation of phase shift with common-mode input voltage. It should also be (ideally) zero.

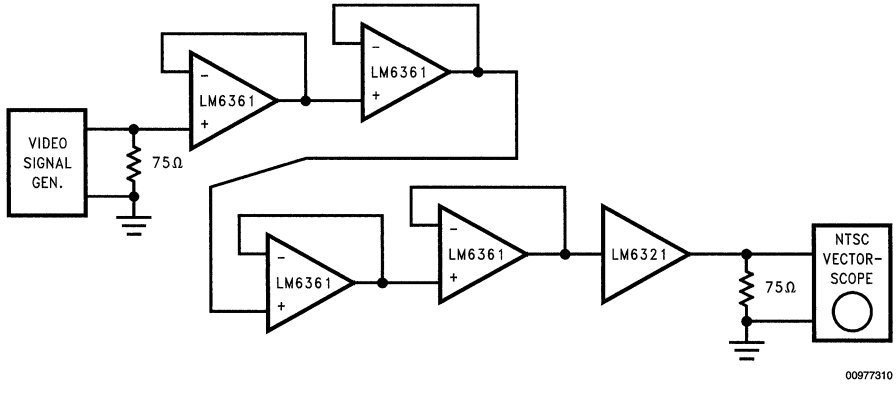
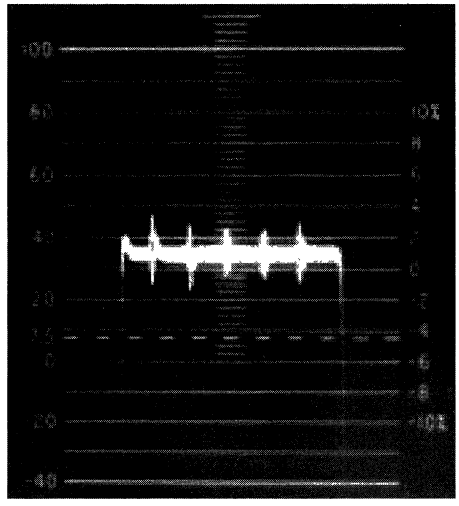


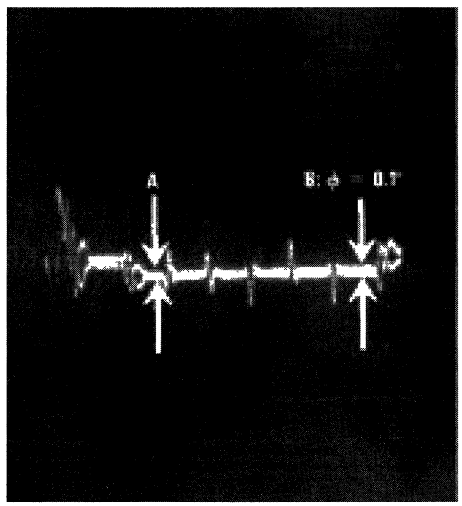
FIGURE 10. Test Circuit for Differential Gain, Differential Phase Measurements

Video Amplifier (Continued)



00977311

FIGURE 11. Differential gain of four cascaded LM6361s plus buffer (see *Figure 10*). Differential gain, measured by change in level from the 1st (leftmost) horizontal bar to the 6th (rightmost), is less than 0.5% for the network.



00977312

FIGURE 12. Differential phase of four cascaded LM6361s plus buffer (see *Figure 10*). Differential phase, based on the spread in the two lines at point B when the spread at point A is nulled, is 0.1° for the network.

To adequately measure the differential gain and phase of these op amps, the error produced by four LM6361 voltage followers, connected in series (see *Figure 10*), was measured. A Tektronix 144 NTSC Signal Generator provided the input signal, and a Tektronix 520 NTSC Vectorscope was used to monitor the error. Since the Vectorscope input needed 75Ω termination, an LM6321 buffer was added to prevent loading of the LM6361s. The LM6321 added less than 0.1% differential gain, and less than 0.02° differential phase, to the measurement.

Figure 11 shows the differential gain of the four LM6361 followers (plus buffer) of *Figure 10* to be less than 0.5%, or an average of less than 0.12% for each LM6361. The differential phase measurement for the same circuit is made with the Vectorscope displaying the picture of *Figure 12*, with one

Video Amplifier (Continued)

side of the display zeroed as shown (point A). The spread of lines at point B represents the differential phase, which is 0.1° for the network (0.02° for each follower), as measured with the Vectorscope. These measurements indicate that a video signal will suffer very little degradation when amplied with one of these devices.

References

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"Intuitive IC Op Amps," by Thomas M. Frederiksen. *National Semiconductor Technology Series,* RR Donnelley & Sons, 1984.

Tektronix Type 520/R520 NTSC Vectorscope Instruction Manual, 1969. Pages 2.2–2.20.

Topics on Using the LM6181—A New Current Feedback Amplifier

National Semiconductor
Application Note 813
Wanda Garrett

Use your imagination . . . that's what jazz is all about. If you make a mistake, make it loud so you won't make it next time.—**Art Blakey**

Introduction

High-speed analog system design can often be a daunting task Typically, after the initial system definition and the design approach is established, the task of component selection commences. Unfortunately, simple reliance on data sheet parameters provides only a partial feel for the device's actual operating nuances. This is unfortunately true no matter how complete a high-speed amplifier data sheet is written Only by experimenting i e , spending some time on the bench with the part, will the requisite experience be obtained for reliably using high-speed amplifiers. The high-speed demonstration board, described herein, can be effectively used to accelerate this process. In developing the LM6181 application program, the key focus areas for making high-speed design a little easier included:

- Designing a product that is more forgiving—for example it can directly drive backmatched cables (a heavy dc load), and significant capacitive loads (without oscillating).
- Developing a high-speed demonstration board that is easily reconfigurable for either inverting or non-inverting amplifier operation.
- Incorporate a highly accurate SPICE macromodel of the LM6181 into National's macromodeling library. This macromodel can be used in conjunction with bench results to more quickly converge on a reliable high-speed design.

Although it may seem that evaluation of high-speed circuit operation can be more quickly performed with computer simulation, full bench evaluation cannot be supplanted. By integrating *both* of these complementary tools, the cycle time from component selection to finalized design can be reduced.

Some Background Information on the LM6181

The LM6181 is a high-speed current feedback amplifier with typical slew rates of 2000 V/µs, settling time of 50 ns for 0.1%, and is fully specified and characterized for ±5V, and ±15V operation. Current feedback operational amplifiers, like the LM6181, offer two significant advantages over the more popular voltage feedback topology. These advantages include a bandwidth that is relatively independent of closed-loop gain (see *Figure 1*), and a large signal response that is closer to ideal. "Ideal" specifically means that the large signal response is not overtly dominated by non-linear slewing behavior (Ref. 1), as is typically found for voltage feedback amplifiers. An obvious consequence is dramatic improvement in distortion performance versus the signal amplitude, and settling time

The high-speed demonstration board can be used to either examine the time domain, or frequency domain. However, the discussion will focus on using this board for the purpose of compensating the time domain response of the LM6181 for popular applications.

LM6181 Closed-Loop Frequency Response
V_S = ±15V; R_f = 820Ω; R_L = 1 kΩ

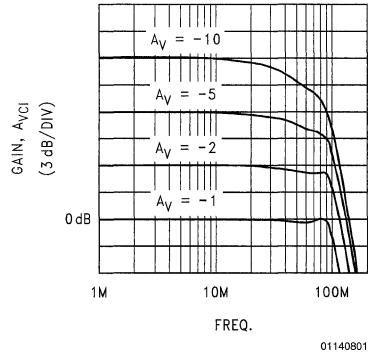

FIGURE 1. Unlike voltage feedback amplifiers which directly trade bandwidth for gain, current feedback amplifiers provide consistently wideband performance regardless of moderate closed-loop gain levels.

Examples of this includes driving cables, dealing with capacitive loads, and generally obtaining a user specified fidelity to the pulse response. Essentially, the demonstration board simplifies the evaluation of high speed operational amplifiers in either the inverting, or the non-inverting circuit configurations. Appendix A includes the board schematic with the associated configuration options Layout of the board included a host of mandatory high speed design considerations. These principles have been summarized in Appendix B (also see Ref. 2 to 4).

A popular application for high speed amplifiers includes driving backmatched cables as illustrated in *Figure 2.* Due to loading and typical bandwidth requirements this particular application places heavy demands on an amplifier. The LM6181 output stage incorporates a high-current-gain output stage that provides a lower output impedance into heavy loads, such as 100Ω and 15Ω. This enhances the amplifier's ability to drive backmatched cables (±10V, into 100Ω) since the internal current drive to the amplifiers output stage is used more efficiently. Additionally, the benefits of the current feedback topology of the LM6181 allows for wideband operation of 100 MHz, even when configured in closed-loop gain configuration of +2.

Some Background Information on the LM6181 (Continued)

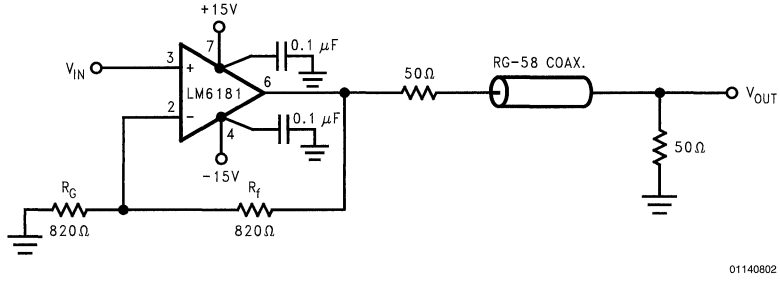

FIGURE 2. Backmatching of a cable is a clean way of terminating the source to the characteristic impedance. The LM6181 can deliver ±10V into the resulting dc load of 100Ω, at 100 MHz, typically.

Experimenting with the Time Domain

Some consideration needs to be addressed for the test signal chosen to evaluate the transient response of a linear system. By the properties of Laplace transforms, if a unit impulse input is used and the measured output response is integrated, the result of applying an inverse Laplace transform will yield the systems frequency response This approach is not typically useful since pulse generators do not generate impulses and the integration becomes unduly complex. Additionally, this technique does not serve to establish an intuitive feel. Alternatively, if a slowly time-varying input signal is used as the test input, the high-frequency components in the system are not significantly excited. The step response often provides a meaningful evaluation of amplifier performance, and represents a more practical signal. Other advantages of using a step response is that it directly provides the dc gain, and the high-frequency nature of the step excites the high-frequency poles in the amplifier's system transfer function.

When evaluating step response performance of wideband amplifiers it is important to use a pulse generator that provides a sufficiently fast risetime. A step response, in relation to the system that is being evaluated, must have a risetime relationship of:

$$t_{risetime} < \frac{0.35}{(\text{Bandwidth of Amplifier})}$$

Therefore, evaluating the step response of the LM6181 amplifier, where the typical bandwidth for gains of +2 is 100 MHz, will require a step input signal with a maximum risetime of 3.5 ns. Since there will always be a certain amount of risetime degradation due to the oscilloscope probe and the oscilloscope, use the same measurement equipment for evaluating both the integrity of the input signal and for measuring the output response of the system. *Figure 3* illustrates a satisfactory input pulse for evaluating the LM6181.

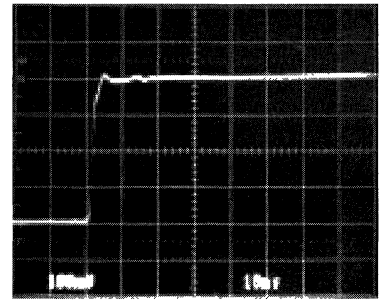

FIGURE 3. Always start the dynamic characterization of high-speed amplifiers with an input signal that maintains adequate speed, with little aberration. Measuring the input signal, from a fast pulse generator, (a Hewlett-Packard 8082A pulse generator was used), also provides a check of correct terminations of the probe—oscilloscope combination.

Probably the largest area of difficulty in high-speed design is when amplifiers drive capacitive loads. Unfortunately, many amplifiers on the marketplace are specified to handle a maximum of a meager 20 pF of capacitive load before oscillation occurs. This maximum limitation equivalently implies that the amplifiers pulse response will be sensitive to typical oscilloscope capacitance—the probe becomes an integral part of the overall circuit, which makes meaningful judgements on measurements very difficult.

Although direct capacitive loading should typically be minimized in general practice, *Figure 4* illustrates that for moderate values of capacitive load, due to the oscilloscope probe, the LM6181 is still very well behaved. *Figure 5* illustrates the simulation using SPICE and the LM6181 macromodel. The LM6181 SPICE macromodel has superb ac and transient response characteristics. For availability information concerning the complete macromodeling library, including the LM6181, along with an outline of the model's capabilities, refer to Appendix C.

Experimenting with the Time Domain (Continued)

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FIGURE 4. Output response of a real LM6181, A_V = +2, $R_f = R_G$ = 820Ω. Output load is oscilloscope probe, Tektronix P6106A, 10 MΩ, 8.7 pF.

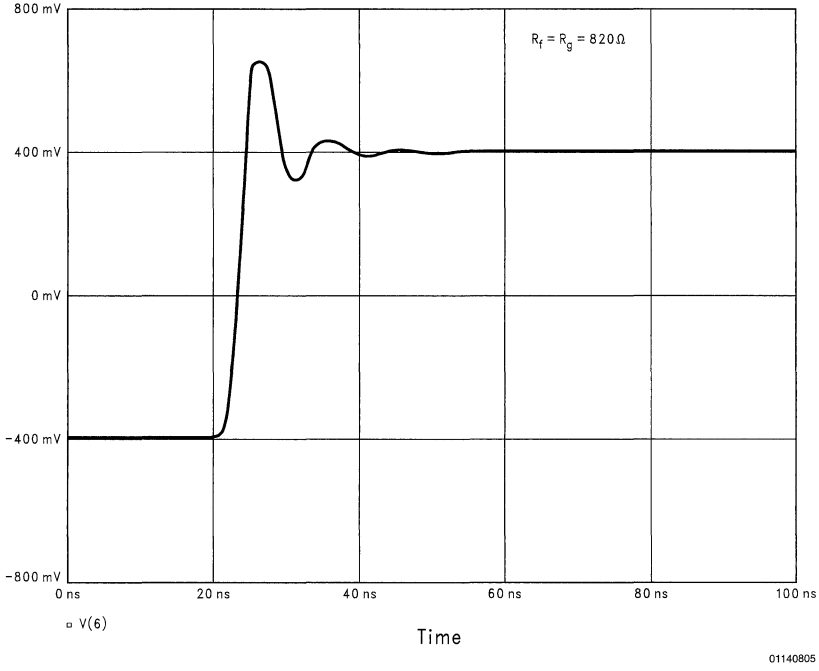

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FIGURE 5. Simulated output response of the circuit in *Figure 3* using the LM6181 macromodel. See Appendix C for more information regarding the LM6181 macromodel and National's Macromodel library.

Compensating the Pulse Response

Degradation in the phase margin, due to direct capacitive loading of high-speed amplifiers can potentially induce oscillation. The output impedance of the amplifier, coupled with the load capacitance, forms a lag network in the loop transmission of the amplifier. Since this network delays the feedback, phase margin is reduced such that even when a system is not oscillating excessive ringing can occur, as illustrated in *Figure 6* where the capacitive load is 48 pF.

A direct solution to reducing the ringing for driving capacitive loads is to indirectly drive the load i.e., isolate the load with a real impedance, such as a moderately small value of resistance. In *Figure 7* a 47Ω resistor was used to isolate the capacitor's complex impedance from the amplifier's output, thereby preserving the amplifier's phase margin. An obvious trade-off exists between taming the time domain response, and maintaining the amplifier's bandwidth, since this form of compensation directly slows down the amplifier's response.

Compensating the Pulse Response (Continued)

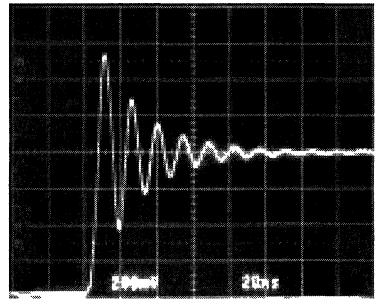

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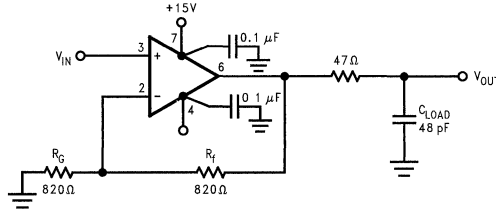
FIGURE 6. Direct capacitive loading will reduce the phase margin and resulting pulse fidelity of any amplifier. A pole is created by the combination of the op amp's output impedance and the capacitive load. This results in delaying the feedback or loop transmission. In this example the LM6181 is directly driving a 48 pF load. High-speed current-feedback amplifiers can handle capacitive loads, and maintain pulse fidelity, by indirectly driving them. This is illustrated in *Figure 7*.



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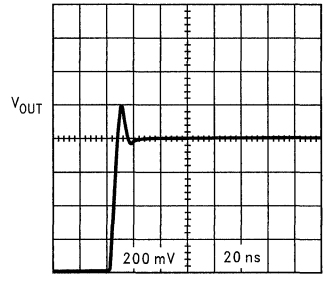

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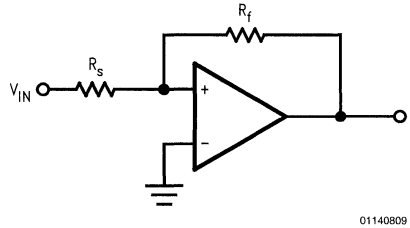
FIGURE 7. A small resistor can be used, such as 47Ω, at the output of the amplifier to indirectly drive capacitive loads.

For general applications of the LM6181, the suggested feedback resistance, R_f, is 820Ω. However, a characteristic unique to current-feedback amplifiers is that they will have different bandwidths depending on the feedback resistor R_f. This results in current-feedback amplifiers maintaining a net closed-loop bandwidth that remains (this is of course an approximation; second order effects do take their toll, of course) the same for moderate variations of closed-loop gain. This feature of current feedback amplifiers actually makes them relatively easy to compensate. By simply scaling the gain setting and the feedback impedance, the appropriate bandwidth can be obtained at the desired value of closed-loop gain. *Figure 8* was cut from the LM6181 data sheet, and describes this relationship.

Compensating the Pulse Response (Continued)



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Bandwidth vs R_F and R_S
A_V = −1, R_L = 1 kΩ

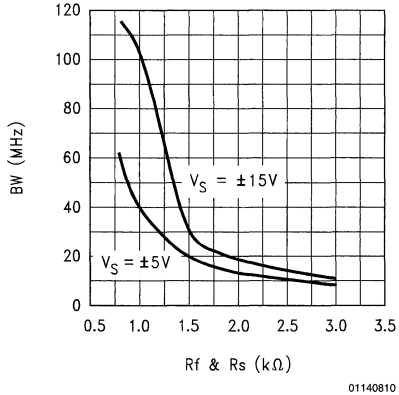

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FIGURE 8. By scaling both R_F and R_S the closed-loop gain stays constant but the bandwidth changes.

A practical application of using altered feedback values for compensating the LM6181 when driving a 100 pF capacitive load is illustrated in *Figure 9*. By reducing the open-loop bandwidth of the amplifier, the resulting degradation of phase margin is reduced, thereby improving the pulse response fidelity.

Compensating the Pulse Response (Continued)

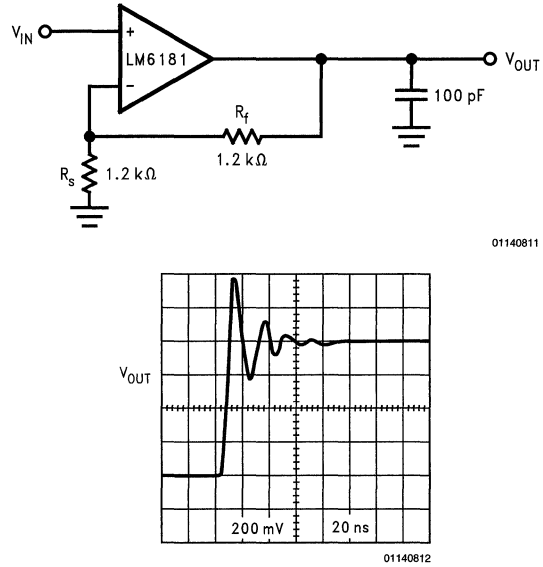


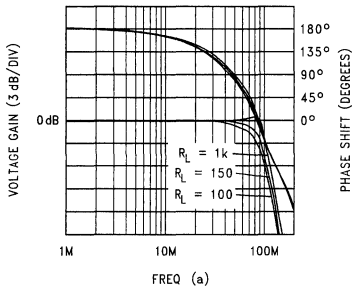
FIGURE 9. Normally, if $R_F = R_S = 820\Omega$, the LM6181 would oscillate with 100 pF of capacitive load. In this example the feedback, R_F and R_S values are scaled to 1.2 kΩ so that the closed-loop gain is $A_V = +2$, but the open-loop band width decreases, maintaining adequate phase margin.

An often overlooked factor in dynamically understanding high-speed amplifiers is the effect that dc loading has on amplifier speed. When driving backmatched cables, for example, the Thevenin equivalent load is usually either 100Ω, or 150Ω. *Figure 10* (from the LM6181 data sheet) provides bandwidth versus dc load information. *Figure 11* illustrates the step response for the LM6181 in a gain of +2, with a dc equivalent load of 100Ω. When the step response is compared against *Figure 4* it is obvious that dc loading will affect amplifier bandwidth. Additionally, since amplifier dynamics is also affected by supply voltage, the LM6181 is fully characterized for both ±5V and ±15V operation.

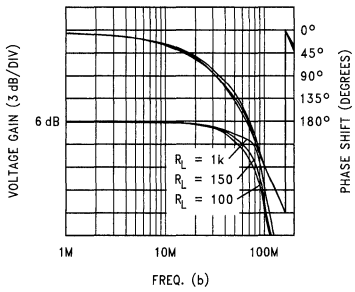
Compensating the Pulse Response

(Continued)

Inverting Gain Frequency Response
V_S = ±15V; A_V = −1; R_F = 820Ω



Non-Inverting Gain Frequency Response
V_S = ±15V; A_V = +2; R_f = 820Ω



Inverting Gain Frequency Response
V_S = ±15V; A_V = −10; R_F = 820Ω

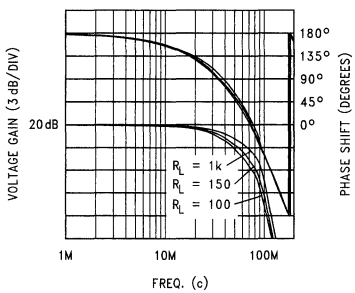


FIGURE 10. DC loading of a high-speed amplifier will affect bandwidth. (Refer to the LM6181 data sheet for ±5V bandwidth vs loading characteristic curves.)

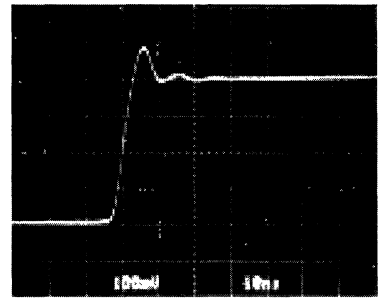
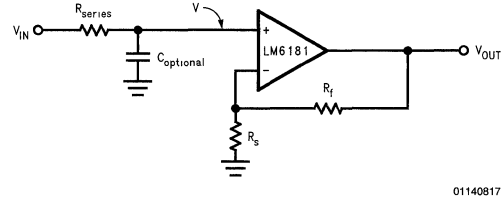


FIGURE 11. Output step response of LM6181 when driving backmatched cables. Comparing this step response to *Figure 4* illustrates the bandwidth reduction due to the 100Ω resistive load.

Compensating Non-Inverting CF Amplifiers

Often, for the inverting amplifier configuration, simply scaling the feedback and gain setting resistor is the easiest way of compensating for peaking and overshoot in the step response. The non-inverting configuration, however, can alternatively be compensated by adding a series input resistor, as shown in *Figure 12*. This resistor, in combination with the input and stray input capacitances of the amplifier bandwidth limit the input step response, and accordingly reduce peaking in the output response. This effect is equivalent to increasing the risetime of the leading edge of the input pulse (some pulse generators have this adjustment).



$$f_{-3\,dB} \text{ of } V \cong \frac{1}{2\pi(C_{optional} + 3\,pF) \cdot R_{series}}$$

FIGURE 12. Peaking and ringing for non-inverting amplifier configurations can be reduced by adding a series input resistor, R_{series}. This resistor interacts with the amplifiers input capacitance to provide a low pass bandwidth limit for the input pulse. If more bandwidth reduction is required $C_{optional}$ can be used.

Compensating Non-Inverting CF Amplifiers (Continued)

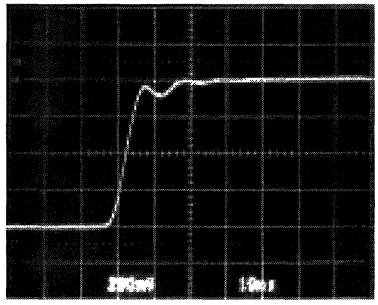


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FIGURE 13. Resulting pulse response for LM6181 using R_{series} = 680Ω, A_V = +2, R_S = R_F = 820Ω, C_{LOAD} ≈ 8.7 pF. Compare this response with *Figure 4*, overshoot and ringing has been dramatically reduced.

Snake Oil and Spice Macromodels Cure All Evils

Not all amplifier macromodels are created equal. For example, driving capacitive loads with high-speed amplifiers is a good way of evaluating and comparing op-amp macromodels. Capacitive loading directly affects the loop dynamics of a closed-loop amplifier system. And since this capacitive load interacts with the output impedance of the amplifier to delay the feedback (or loop transmission), the phase margin is reduced, as stated earlier.

Simulating high-speed systems when driving capacitive loads places a demand on the amplifier's macromodel. Constructing an accurate macromodel is not simple. Unfortunately, parameterized models (an efficient method of using a computer to generate many inaccurate models per a typical workday) lack the extensive software testing and bench measurement analysis required for sophisticated simulation work. The amplifier's output stage, the frequency response, and the input parasitic structures need to be carefully measured on the bench, then accurately mimicked in the macromodel. The moral is to be aware, and:

ALWAYS TEST YOUR MACROMODEL!

Compare the similarity between results in *Figure 14* with the bench results of *Figure 6*. Increased confidence in using a specific high-speed amplifier macromodel can be obtained by corresponding bench results of driving capacitive loads with simulation results.

Driving reactive loads, such as capacitive loads, can be used not only to indicate limitations for the associated SPICE macromodel, but also to reveal some of the amplifier's high-speed personality. Never assume that a macromodel of an operational amplifier includes characteristics that are germane to your particular simulation.

Summing Things Up

The focus has been on high-speed analog design methodology, as opposed to generating a plethora of varied application circuits. By establishing a foundation—understanding the amplifier, referring to the typical characterization curves, using correct high-speed layout techniques, knowing the SPICE macromodels limitations, and adopting some basic compensation techniques, a large fraction of everyday high-speed design challenges can be addressed confidently.

Summing Things Up (Continued)

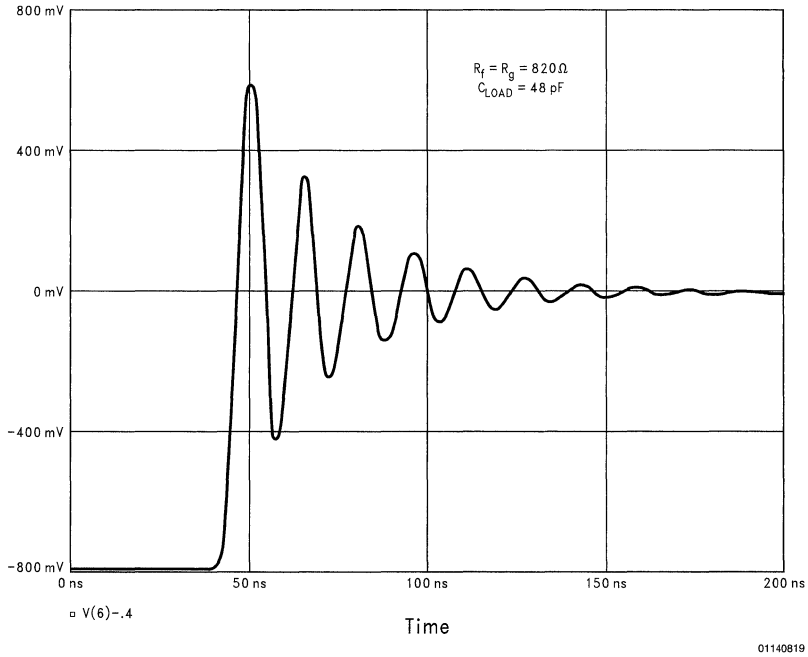
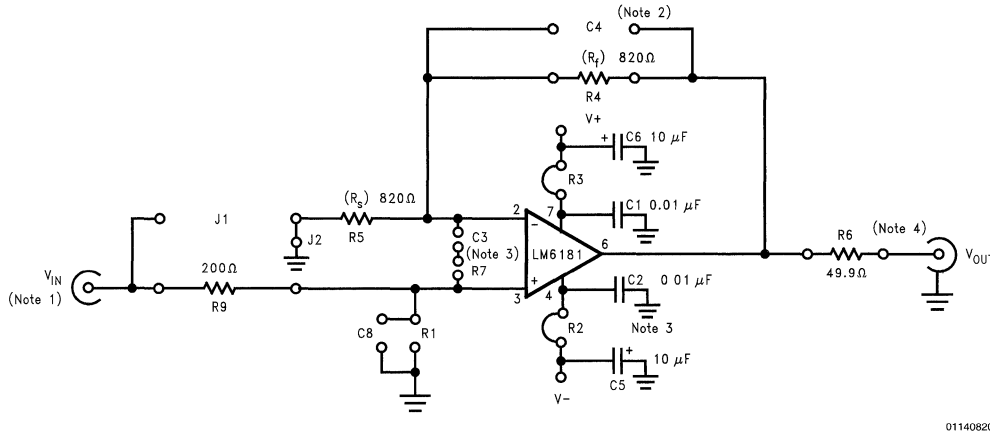


FIGURE 14. Simulation of LM6181 step response with A_V = +2, $R_F = R_S$ = 820Ω, and C_{load} = 48 pF.

Appendix A



The LM6181 high speed demonstration board can be configured for either inverting or non-inverting amplifier configurations. This board was intentionally embellished with options so that it can be used as a general-purpose 8-pin op-amp evaluation board.

Note 1: Terminate this BNC connection with the appropriate connector Otherwise ringing due to high-frequency reflections will occur

Note 2: Do not lead compensate current feedback amplifiers — oscillation will result Lead compensation uses a feedback capacitor, C_4

Note 3: C3 and R7 are optional lag-compensation network points

Note 4: R6 is for back matched driving of cables

Appendix B: High Speed Board Design Caveats

1. Good high frequency termination is always required for the input signal. It is important, for evaluating any amplifier, to check the integrity of the input signal.
2. RF quality, ceramic capacitors are used for bypassing and are placed close to the amplifiers supply pins.
3. The feedback network is placed in close proximity to the amplifier.
4. The entire top side of the board is ground planed. This lowers the high-frequency impedance for ground return signals.
5. The amplifier inputs have ground plane voids since these amplifier nodes are sensitive to parasitic stray capacitance. This is specifically a key issue for the non-inverting amplifier configuration.
6. All leads are kept as short as possible, using the most direct point-point wiring techniques.

Appendix C: Features Modeled For LM6181 Macromodel

Supply-Voltage-Dependent Input Offset Voltage (V_{OS})

Temperature-Dependent Input Offset Voltage (TCV_{OS})

Supply-Voltage-Dependent Input Bias Current (I_{b+} & I_{b-} PSR)

Temperature-Dependent Input Bias Current (TCI_{B+} & TCI_{B-})

Input-Voltage-Dependent Input Bias Current (I_{b-} CMRR)

Non-Inverting Input Resistance

Asymmetrical Output Swing

Output Short Circuit Current (I_{SC})

Supply-Voltage-Dependent Supply Current

Quiescent and Dynamic Supply Current

Input-Voltage-Dependent Input Slew Rate

Input-Voltage-Dependent Output Slew Rate

Multiple Poles and Zeroes in Open-Loop Transimpedance (Z_t)

Supply-Voltage-Dependent Input Buffer Impedance

Supply-Voltage-Dependent Open-Loop Voltage Gain (A_{VOL})

Feedback-Resistance-Dependent Bandwidth

Accurate Small-Signal Pulse Response

Large-Signal Pulse Response

DC and AC Common Mode Rejection Ratio (CMRR)

DC and AC Power Supply Rejection Ratio (PSRR)

White and 1/f Voltage Noise (e_n)

White and 1/f Current Noise (i_n)

For information related to obtaining National's SPICE macromodeling library, including the LM6181, call a National sales office.

References

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2 K Lacanette, K Hoskins, "Preserving and Verifying the LF400's Fast Settling Time", AN-428, National Semiconductor Linear Applications Handbook

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Development of an Extensive SPICE Macromodel for "Current-Feedback" Amplifiers

National Semiconductor
Application Note 840

Abstract

A current-feedback amplifier macromodel has been developed which simulates the more common small-signal effects such as small-signal transient response and frequency response as well as temperature effects, noise, and power supply rejection ratio. Also modeled are large-signal effects such as non-linear input transfer characteristics and input/output slew rate limiting.

Detailed descriptions of each stage in the model will be presented with examples of model performance and correlation to actual device behavior.

Introduction

With the increasing complexity and shorter design cycles of today's designs, computer modeling with SPICE (Simulation Program with Integrated Circuit Emphasis) is becoming more popular. This is especially true with high-speed designs utilizing the latest in current-feedback amplifiers. However, an accurate, detailed macromodel for current-feedback amplifiers with good convergence characteristics has not yet been available.

Macromodeling Philosophy

The philosophy used in creating this macromodel was a desire to design a model that would simulate the typical behavior of a current-feedback amplifier to within 10% of typical parameters while executing much faster than a device level model Also, the macromodel would act as a development platform for effects not normally included in other models such as temperature effects, noise, and many of the other second and third order effects that are characteristic in current-feedback amplifiers such as the LM6181.

The LM6181

National Semiconductor's monolithic current-feedback amplifier, the LM6181, offers the designer an amplifier with the high-performance advantages of current-feedback topology without the high cost associated with hybrid devices. The LM6181 has a bandwidth of 100 MHz, slew rate of 2000 V/µs, settling time of 50 ns (0.1%), and 100 mA of output current drive. A special output stage allows the LM6181 to directly drive a 50Ω or 75Ω back-terminated coax cable. To understand how this device functions, a description of current-feedback amplifiers is in order.

Current-Feedback Amplifiers

Figure 1 shows the block diagram for the current-feedback amplifier The main difference when compared to voltage-feedback amplifiers (VFA's) is that in the current-feedback topology, a unity gain buffer drives the inverting input. Since this is an inherently low impedance, the feedback error signal is treated as a current rather than a voltage. During input transients, an error current will flow into or out of the input buffer. This current is then mirrored to a current-to-voltage converter (Zt(s)) which consists of a large (≈ 2 MΩ) transimpedance and an output buffer. Since the large transimpedance is analogous to the large voltage gain of VFA's, the output voltage is servo'ed to a value which causes the current through Rf and Rg to cancel the current in the input buffer.

Current-Feedback Amplifiers (Continued)

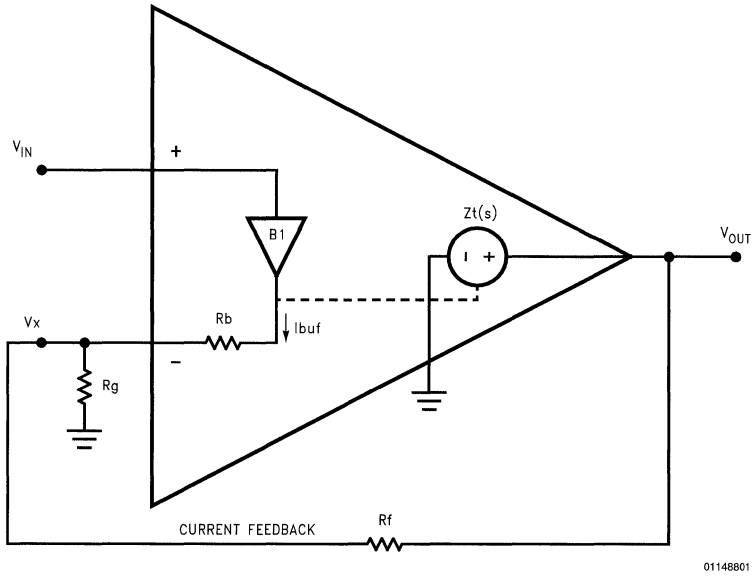


FIGURE 1. Block Diagram of a Current-Feedback Amplifier

Analysis of Current-Feedback Topology

From the simplified current-feedback amplifier schematic in *Figure 2*, it can be observed that the inverting (–IN) terminal is driven by a unity gain buffer stage. Transistors Q3 and Q4 make up the high-impedance input (+IN) to the buffer while Q5 and Q9 comprise a push-pull stage whose low output impedance is determined by $V_T/(I_C Q5 + I_C Q9) = V_T/(I1 + I2)$ assuming I1 and I2 are equal. The function of the input buffer is to drive the inverting input to the same voltage as the non-inverting input much like a voltage-feedback amplifier does via negative feedback. Transistors Q6, Q7, Q8, Q10, Q11 and Q12 form a pair of Wilson current mirrors which transfer the output current of the input buffer to a high-impedance (Zt) node. The equivalent capacitance (C_C) at this node is charged to the value of the output voltage. This voltage is then conveyed to a second buffer made up of Q14, Q15, Q17 and Q18 which drives the output pin of the amplifier. Short-circuit current limiting is performed by transistors Q19 and Q20. Back on the input of the amplifier, Q1 and Q2 provide a slew rate enhancement effect. For low closed-loop gains and large input steps these transistors turn on and increase the current available to the input buffer. This causes a transient increase in the current available to charge the compensation capacitor via the current mirrors, resulting in a faster slew rate for low gains. Now that the simplified circuit has been described, it will be informative to analyze the block diagram for the model.

By summing the currents at node Vx in *Figure 1* and using the fact that $V_O = I_{buf} \times Zt(s)$, the transfer function of the non-inverting configuration can be determined to be:

$$\frac{V_o}{V_{in}} = \left(1 + \frac{Rf}{Rg}\right) \times \left[\frac{1}{1 + \dfrac{Rf + \left[1 + \dfrac{Rf}{Rg}\right] \times Rb}{Zt(s)}}\right] \quad (1)$$

where Zt(s) is the open-loop transimpedance as a function of complex frequency. Notice, in *Equation (1)*, the 1 + Rf/Rg term on the left is the standard closed-loop voltage gain equation for non-inverting amplifiers while the term on the right is an error term. The 1 + Rf/Rg in the error term is the noise gain of the amplifier and Rb is the input buffer's quiescent output impedance (≈ 30Ω for the LM6181). If Zt(s) is assumed to be large, the error term goes to 1. The closed-loop bandwidth is defined as the frequency at which the magnitude of the error term equals $1/\sqrt{2}$ (–3 dB). If Zt(s) is approximated to be a single pole function, then:

$$Zt(s) = \frac{Zt(dc)}{1 + s \times Zt(dc) \times C_C} \quad (2)$$

where C_C is the value of the internal compensation capacitor in *Figure 2*. By substituting *Equation (2)* for Zt(s) in *Equation (1)* and assuming Zt(dc) is much larger than Rf, the closed-loop bandwidth can now be found to be:

$$bw = \frac{1}{2 \times \pi \times C_C \left[Rf + \left(1 + \dfrac{Rf}{Rg}\right) \times Rb\right]} \quad (3)$$

Analysis of Current-Feedback Topology (Continued)

If the input buffer output resistance (Rb) times the noise gain of the amplifier (1 + Rf/Rg) is assumed to be small compared to Rf, *Equation (3)* reduces to:

$$bw = \frac{1}{2 \times \pi \times C_C \times Rf} \tag{4}$$

Notice that the ideal closed-loop bandwidth in *Equation (4)* is dependent only on the value of the internal compensation capacitor (C_C) and the feedback impedance (Rf). A recommended value for Rf is usually specified in the manufacturer's datasheet (Rf = 820Ω for the LM6181). Therefore, if the above assumptions are valid, there is theoretically no reduction in bandwidth as Rg is decreased to increase closed-loop gain.

Another special feature of the current-feedback amplifier is the theoretical absence of slew-rate limiting. Since the total output current of the input buffer is available to charge the compensation capacitor (C_C), the slew rate is proportional to the output voltage [4].

$$SR = \frac{I_{buf}}{C_C} = \frac{V_{OUT}}{C_C \times Rf} \tag{5}$$

This simplified analysis is adequate for small closed-loop gains; however, since Rb is typically several tens of ohms, the bandwidth and slew rate will be less than ideal for large gains. Also, there are slew-rate characteristics associated with the input buffer that are dominated by the slew-rate enhancement transistors (Q1 and Q2 in *Figure 2*) and stray package capacitances. All these second order effects are included in the macromodel input stage to achieve accurate simulation results.

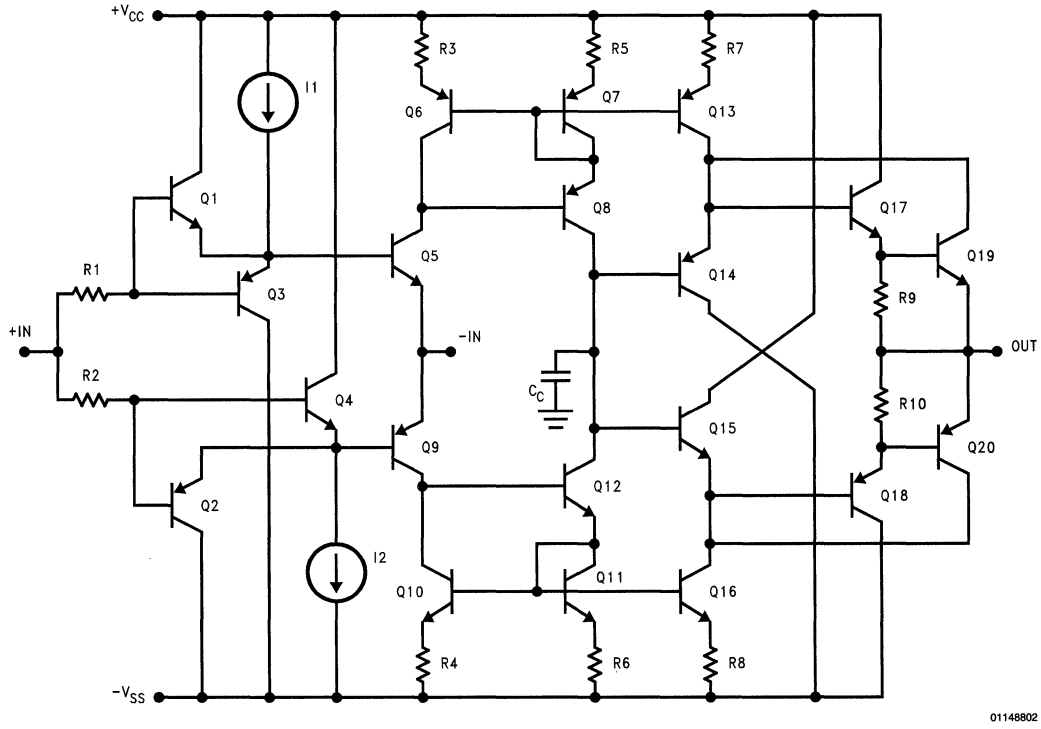


FIGURE 2. LM6181 Simplified Circuit

The Input Stage

Figure 3 shows the macromodel input stage which performs many important functions such as the simulation of input buffer output impedance, input/output slew rate, supply voltage dependent input bias current and offset voltage, input capacitance, CMRR and noise [2]. Voltage-controlled current-sources GI1 and GI2 establish the input buffer's output impedance depending on supply voltage. For a given supply voltage, these current-sources can be determined by rearranging the standard bipolar transistor output resistance equation:

The Input Stage (Continued)

$$I1 = I2 = \frac{k \times T}{2 \times q \times Rb} \tag{6}$$

Rb is the output impedance of the input buffer and may be approximated with

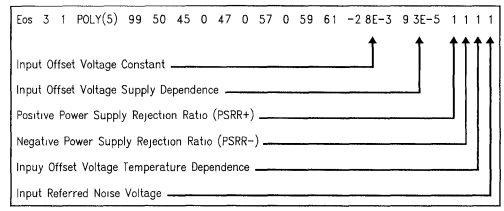
$$Rb = \frac{Zt}{A_{VOL}} \tag{7}$$

where A_{VOL} is the differential open-loop voltage gain of the amplifier from input to output. *Equation (7)* can be derived by shorting Rg and solving the transfer function in *Equation (1)*

The input stage slew rate is controlled by R1, R2, C1 and C2. The total current available to charge the capacitors C1 and C2 determines the maximum slew rate of the input stage. To reduce the number of PN junctions in the model, the slew rate enhancement transistors were modeled with diodes DS1 and DS2 and current-sources FI1 and FI2.

Input bias currents are simulated with polynomial-controlled current-sources Gb1 and Gb2 which are dependent on both supply voltage and temperature. Current-source Gb2 also models the residual input current (Ib) caused by imbalances in the input buffer as well as the error current caused by the input common mode voltage. The latter is called Inverting Input Bias Current Common Mode Rejection and is designated IbCMR on most datasheets Fn1 and Fn2 transfer the current from the noise-current sources to the inputs of the amplifier

The offset voltage-source, Eos, provides a supply voltage dependent input offset voltage and reflects the error voltages from the power supply rejection ratio stage, the thermal effect stage, and the noise-voltage source. Below is a diagram of the Eos polynomial-source and the effects that correspond to each term.



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Stray capacitance at the inputs of the amplifier modeled by $C_{in}1$ and $C_{in}2$ has a dramatic effect on the peaking in the amplifier's high frequency response. Common Mode Rejection Ratio can be modeled in the input stage by properly setting the early voltage (Vaf) of the input transistor models A good starting point for the value of the early voltage is given by:

$$Vaf = \frac{2 \times V_T}{10^{\left[\frac{CMRR(dB)}{20}\right]}} \tag{8}$$

Also, in the transistor model, a value for beta (BF) should be chosen. It should be large enough so that the base currents do not interfere with the input bias currents of the model, but not so large as to cause convergence problems during simulation.

The output of the input stage is the sum of the currents flowing through R3 and R4 The voltage across R3 and R4 is softly clamped by the V1, RE1, D1 and V2, RE2, D2 strings respectively. This effectively limits the current to the second stage yet still allows the second stage slew rate to increase for large input signals.

The Input Stage (Continued)

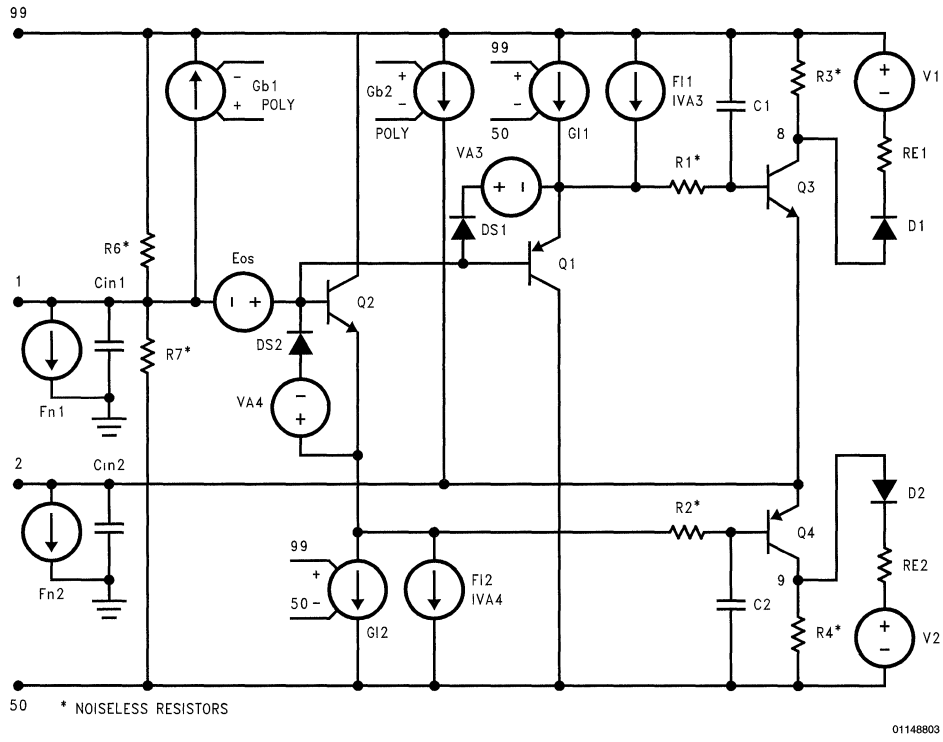

FIGURE 3. Macromodel Input Stage. Simulates Input Impedance, Input Errors, CMRR, Input/Output Slew Rate, Input Capacitance, and Noise.

The Second Stage

The second stage of the macromodel (*Figure 4*) provides the open-loop transimpedance, the first pole, output clamping and supply dependent quiescent supply current. The voltage-controlled current-source G1 is controlled by a second order polynomial equation which calculates the current through R3 and R4 and reflects the sum directly into the second stage. By making the polynomial coefficients equal to the reciprocal of R3 and R4, the DC transimpedance of the model is simply equal to the value of R5. The dominant pole and output slew rate is established with capacitor C3 which is comparable in function to C_C in the LM6181 simplified circuit. Output clamping is performed with two diodes (D3–D4) each in series with a voltage-source (V3–V4). Clamping should be done here at the gain stage to prevent node 15 from reaching several thousands of volts which could cause convergence problems during simulation. Quiescent current is modeled with the combination of I3 and the R8–R9 series resistors. As the supply voltage increases, the current through R8 and R9 will increase effectively simulating that behavior in the real device. The value for resistors R8 and R9 can be calculated by dividing the change in supply voltage by the change in supply current ($\Delta V_S/\Delta I_S$) anywhere within the operating range of the amplifier. Current-source I3 is evaluated by taking the total supply current at a given voltage and subtracting off the current through all other significant supply loads. These loads are R8, GI1, GI2, and R3 so that:

$$I3 = Ivs\ @\ 15V - \frac{15}{R8} - 3 \times I1 \qquad (9)$$

The 3 x I1 comes from the fact that the currents through GI1, GI2 and R3 are equal. Resistors R8 and R9 also act as a voltage divider and establish a common-mode voltage (V_H) for the model directly between the rails. If the supply rails are symmetrical, i.e., ±15V, node 49 will be at zero volts. Voltage-controlled voltage-source EH measures the voltage across R8 and subtracts an equal voltage from the positive supply rail to provide a stiff point between the rails (node 98) to which many other stages in the model are referenced.

The Second Stage (Continued)

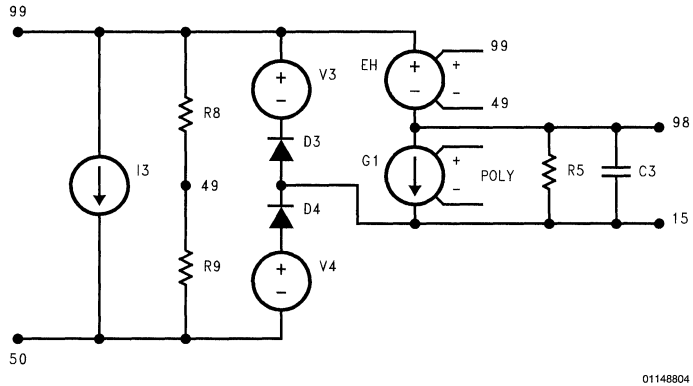

FIGURE 4. The Macromodel Second Stage Models Open-Loop Transimpedance, First Pole, Output Swing Limiting, and Quiescent Supply Current.

Frequency-Shaping Stages

In keeping with the philosophy of providing a macromodel that is as accurate as possible, it has been determined that the model must be capable of easily accommodating as many poles and zeros that are necessary to precisely shape the magnitude and phase response of the model [5]. This is accomplished with telescopic frequency-shaping stages that each have unity DC gain making it easier to add poles and zeros without changing the DC gain of the model. The LM6181 macromodel has four high frequency pole stages and no zero stages, however, each of the three types of frequency-shaping stages will be discussed in detail should the reader wish to develop macromodels for other amplifiers.

The first type of frequency-shaping stage is a pole. In *Figure 5* (a), resistor R14 is set to 1 kΩ. This value is chosen to reduce the thermal noise associated with this resistor and to simplify the calculations for the other components in the stage. Current-source G2 is controlled by the output voltage from the previous stage and its g_m is set to the reciprocal of R14 or 10^{-3} to maintain unity DC gain of the stage. Capacitor C4 rolls off the gain at high frequencies and is set with the standard pole equation: C = 1/(2 x π x fp x R) where fP is the −3 dB frequency of the pole in Hz.

Even though SPICE will attempt to process a bare zero stage, in the real world, such a circuit is actually non-causal and SPICE may not converge because an ideal inductor can generate an infinite voltage if the current though it changes instantaneously. To introduce a zero in the frequency response of the model, a pole must be combined with the zero to form a zero/pole or a pole/zero stage. The circuit for the zero/pole stage is shown in *Figure 5* (b). This stage will have unity DC gain if the g_m of G5 is set to the reciprocal of R19. As the frequency increases, L1's impedance starts to increase until R18 dominates causing the gain to level off.

The last type of frequency-shaping stage is the pole/zero circuit shown in *Figure 5* (c). As the frequency increases, the gain starts at unity and decreases until the impedance of the capacitor is negligible compared to its series resistor. For more information on poles and zeros, see references [7] and [8].

Frequency-Shaping Stages

(Continued)

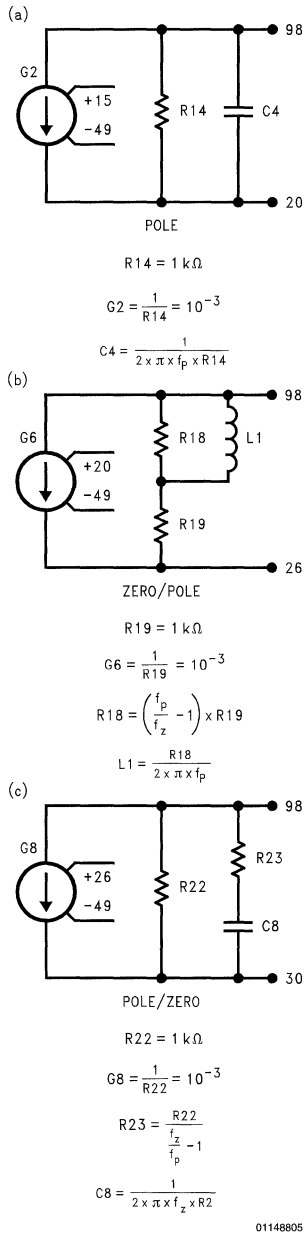

FIGURE 5. Macromodel Frequency-Shaping Stages

PSRR Stage

Power supply rejection ratio is a parameter that many vendors have previously neglected in their SPICE models. Since AC power supply impedance is extremely critical in high-speed amplifier designs, both DC and AC PSRR were included in this model so that the designer can explore the effects of supply bypassing. The PSRR stage (see *Figure 6*) consists of two attenuation circuits controlled by the voltage from each rail to ground whose gains increase at 20 dB per decade.

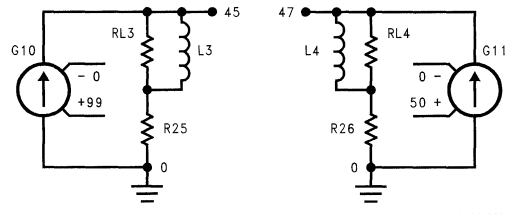

FIGURE 6. Macromodel PSRR Stage

The signals generated at nodes 45 and 47 are directly reflected to the input of the amplifier via the second and third terms of the Eos polynomial-controlled source. Since the PSRR stages are referenced to ground, a large offset voltage will be developed if the model is operated from asymmetrical supplies. This compromise was necessary in order to include the PSRR effects; however, if operation on asymmetrical supplies is required, the PSRR effects can be disabled by changing the second and third polynomial terms in Eos from 1 to 0. For example, change:

Eos 3 1 POLY(5) 99 50 45 0 47 0 57 0 59 61 –2.8E-3 9.3E-5 1 1 1 1

to·

Eos 3 1 POLY(5) 99 50 45 0 47 0 57 0 59 61 –2.8E-3 9.3E-5 0 0 1 1

To set the component values in the PSRR stages, R25 and R26 are arbitrarily chosen to be 10Ω. The g_m's of the current sources are set so that the DC gain of each stage is equal to the DC value of the PSRR or:

$$G10 = 10^{\frac{PSRR}{20}} \times \left[\frac{1}{R25}\right] \quad (10)$$

where PSRR is the typical DC rejection ratio in dB. The inductors, L3 and L4, determine the 3 dB frequency of each stage and can be set with:

$$L = \frac{R}{2 \times \pi \times f_{3dB}} \quad (11)$$

Resistors RL3 and RL4 cancel the zeros associated with the inductors at a frequency above the unity gain frequency of the amplifier. This helps with transient convergence when simulating inductive or resistive power supply lines.

Thermal Effects

The predominant thermal effects of a current-feedback amplifier are the change in offset voltage and input bias current as a function of temperature. The macromodel stages in *Figure 7* are used to simulate these effects by utilizing the SPICE temperature dependent resistor model which is controlled with the *Equation (9)*:

Thermal Effects (Continued)

$$R(\Omega) = \text{<value>} \times (1 + TC1 \times (T - Tnom) + TC2 \times (T - Tnom)^2) \quad (12)$$

where <value> is the value of the resistor at Tnom (usually 27°C), T is the temperature in °C, TC1 is the linear temperature coefficient, and TC2 is the quadratic temperature coefficient The equation will fit a quadratic curve through three points in a temperature graph by solving three equations with three unknowns Since SPICE will give an error message if a resistor goes negative at any temperature, an offset bias is added to the resistor value whose voltage is then subtracted from the respective input error source (Gb1, Gb2, or Eos)

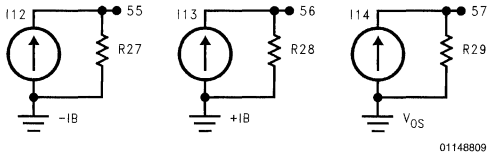

FIGURE 7. Macromodel Thermal Effect Stages

The voltages generated at nodes 55, 56, and 57 are scaled and used to control the input error sources Gb2, Gb1, and Eos respectively. The simulated results compare quite closely to the typical curves for the actual device as can be seen in *Figures 16, 17*

Noise Stages

The addition of noise effects to any macromodel is similar to the techniques used for input offset voltage and drift. The total amplifier noise is lumped together and referred to the input of the model. Before noise sources are added, however, the model has to be rendered essentially noiseless. This is easier than it sounds, though, because noise adds vectorially. The total contribution of several noise sources can be found by:

$$En_{total} = \sqrt{(En1)^2 + (En2)^2 + (En3)^2 \ldots}$$

So, a latent noise source within the model will have to be reduced to only ¼ of the desired noise level to maintain an accuracy of less than 3% ($\sqrt{1 + 0.25^2} = 1.03$). Most of the latent amplifier model noise comes from thermal noise generated by large-value resistors commonly used in macromodels. To reduce this noise, the resistor values are scaled so their thermal noise is negligible compared to the desired noise of the amplifier. If resistor scaling is not possible, as was the case with several resistors in the input stage of the LM6181 macromodel, a *noiseless resistor* can be used. A noiseless resistor is created by utilizing a voltage-controlled current-source (G device) with the same input and output terminals whose gm is set to the reciprocal of the required value of resistance (see *Figure 3* and the LM6181 netlist). The only caveat with using noiseless resistors is that a current- source is considered an open circuit when SPICE calculates the initial bias point of the circuit. Therefore, at least one other device must be connected to the nodes of the noiseless resistor to avoid "floating node" errors.

Now that the macromodel is rendered essentially noiseless, lumped noise sources can be added and referred to the input sources. *Figure 8* shows the equivalent noise model which consists of an ideal noiseless amplifier, two noise-current generators (I_{n+} and I_{n-}), from each input to ground and a noise-voltage generator (e_n) in series with non-inverting input.

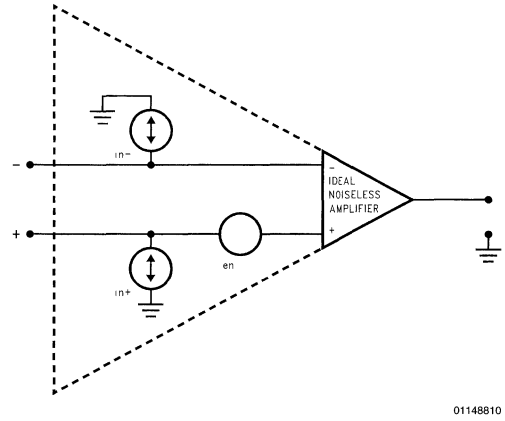

FIGURE 8. Equivalent Amplifier Noise Model

The noise-current generators are called Fn1 and Fn2 in the macromodel input stage (*Figure 3*), while the noise-voltage generator is included in the Eos polynomial-controlled source. The noise voltage or current which is actually referred to the input generators comes from separate noise source stages in the macromodel.

The noise-voltage circuit (*Figure 9*) generates both 1/f and white noise by using a 0.1V voltage-source which lightly biases a diode-resistor series combination. White noise is simply the thermal noise-current generated in the resistor which follows the spectral power density (per unit bandwidth) equation below:

$$i_n^2 = \frac{4 \times k \times T}{\text{Resistance}} \quad (13)$$

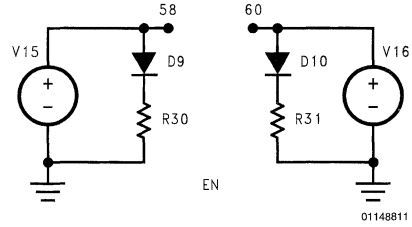

FIGURE 9. Macromodel Noise Voltage Stage

where in is the noise-current through the resistor, k is Boltzmann's constant (1 381 x 10^{-23}), and T is the temperature in °K (°C + 273.2°). By taking the square root of both

Noise Stages (Continued)

sides of the equation and multiplying by resistance, the required value of resistance can be found for a given noise-voltage spectral density with:

$$R = \frac{e_n^2}{2 \times 4 \times k \times T} \tag{14}$$

where e_n is the white noise voltage of the amplifier per $\sqrt{Hz}$. The "2" in the denominator comes from the fact that the voltage is taken differentially across two identical circuits of the noise-voltage source (nodes 58 and 60). The reason for using two identical circuits is so that a DC voltage would not be created which would be seen as an offset voltage on the input.

Flicker noise or 1/f noise-voltage comes from the SPICE diode model. By setting the flicker noise exponent (AF) to 1 and properly setting the flicker noise coefficient (KF), the resulting noise voltage will accurately simulate the 1/f noise-voltage spectral density with the correct "corner frequency". *Equation (15)* shows the noise-current that results from the SPICE diode model where Id is the DC diode current and the 2 x q x Id term is negligible compared to the 1/f noise of the amplifier.

$$i_n^2 = 2 \times q \times Id + KF \times \frac{Id^{AF}}{FREQUENCY} \tag{15}$$

To determine the value for KF in the macromodel, the following equation can be used:

$$KF = \frac{Ea^2}{R^2 \times Id \times 2} \tag{16}$$

where Ea is the noise-voltage spectral density of the amplifier at 1 Hz and Id is the DC current through the diode which can be determined with the standard Schottky diode equation. Again, the "2" in the denominator comes from the fact that the noise output is taken differentially across two identical circuits.

The white portion of the amplifier's noise current is modeled by utilizing the thermal noise current of a resistor in series with a zero volt voltage-source (see *Figure 10*).

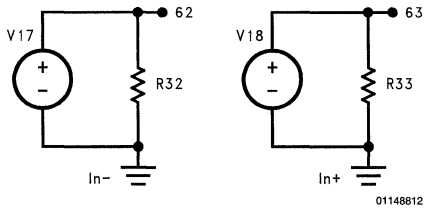

FIGURE 10. Macromodel White Noise-Current Generators

Since the noise-current through each of the resistors is measured with the voltage-sources and directly referred to the respective current-controlled current-source on the input, the value for each resistor can be found by rearranging *Equation (13)* or:

$$R = \frac{4 \times k \times T}{i_n^2} \tag{17}$$

The in term is the broad-band or white noise-current spectral density at the respective input of the amplifier.

To simulate the 1/f component of the noise-current, the flicker noise coefficient (KF) in the model for each pair of input transistors is set to obtain the correct corner frequency. In the LM6181 macromodel, KF is set to 4.13×10^{-13} for Q1 and Q2 while KF is set to 6.7×10^{-14} for Q3 and Q4. The flicker noise exponent (AF) is left at its default value of 1.

The macromodel's noise curves are compared to the actual amplifier's curves in *Figures 18, 19, 20, 21*. The simulation results are quite close to the actual noise characteristics of the amplifier. For more information on calculating and modeling amplifier noise, see references [3] and [9].

Output Stage

After the input signal is amplified and frequency shaped, it is further processed by the output stage shown in *Figure 11*. The output stage performs three important functions, namely, simulation of output impedance, short-circuit current limiting, and dynamic supply current.

The intermediate output signal appears at the output of the last frequency-shaping stage as a high-source-impedance voltage referenced to V_H. Voltage-controlled voltage-source, E1, level shifts the intermediate output signal down from the positive rail and provides the output drive for the model. Output impedance is modeled with the combination of R35 and L5. Resistor R35 simulates the DC output impedance which determines the behavior of the model when driving heavy loads. Additionally, inductor L5 models the characteristic rise in output impedance as a function of frequency which is common to the emitter-follower output stage found in many amplifiers. Since an ideal inductor as modeled by SPICE has infinite Q, a bare inductor in the signal path can cause convergence problems if the current through it can change instantaneously. To lower the Q of the inductor and prevent convergence problems during simulation, a large value resistor, RL5, is placed across L5. Capacitor CF1 models stray capacitance across the feedback resistor which dramatically affects the high frequency response of the amplifier.

Short-circuit current limiting is also a necessary feature of any good amplifier macromodel. The diodes D5 and D6 each in series with a voltage-source V5 and V6 accomplish this function by effectively clamping the maximum voltage across R35. The value of the voltage-sources can be set with the following equation which was derived with the Schottky diode equation and summing the currents at node 40 assuming the output is shorted to ground.

$$V = R35 \times I_{SC} - \ln\left[\frac{V_{CC} - R35 \times I_{SC}}{I_S \times Zofr} + 1\right] \times V_T \tag{18}$$

Output Stage (Continued)

The term Zofr is the output impedance of the last frequency shaping stage (1 kΩ in this case), I_S is the saturation current of the diode, and V_T is the thermal voltage k x T/q. Although it appears that the appropriate parameters are included in the equation, no attempt was made to model the dependence of short-circuit current on supply voltage or temperature.

Another behavior that is often not included in op-amp macromodels is dynamic supply current. If the output of the model is driven by an ideal voltage-source, the simulated output current of the model appears to come from nowhere, i.e , the supply currents do not change This apparent violation of the second law of thermodynamics has been solved with diodes D7–D8, current-sources F5–F6, and associated circuitry. Since it is important to keep non-linear devices, such as diodes, out of the signal path, only an ideal ammeter, VA8, was inserted in the output driver to sense the sinking or sourcing of output current. Current-controlled current-source F5 mirrors the current sensed by VA8 and forces an equal current through either D7 or D8 depending on its polarity. If current is being sourced into the load, the current flows from the positive rail through E1 and VA8 to the output node and no supply current correction is necessary However, if the output stage is sinking current from the load, the current flows from the output node up through VA8 and E1 into the positive rail. To compensate for this, F5 forces an equal current through D7 and ammeter VA7. This current is then mirrored to current-source F6 which pulls an equal amount of current out of the positive rail and forces it into the negative rail. Therefore, if the output stage is sourcing current, it appears to come from the positive rail, whereas current that is sinking from the load appears to go into the negative rail. The net result of all these extra devices is an output stage which closely models the behavior of the real amplifier

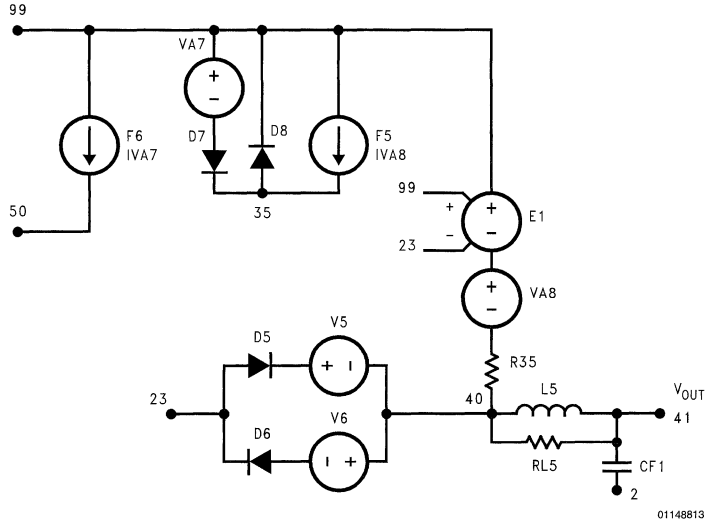

FIGURE 11. Macromodel Output Stage

LM6181 Macromodel Netlist

```
*****************************************
*LM6181 CURRENT FEEDBACK OP-AMP MACRO-MODEL
*****************************************
*
*connections:     non-inverting input
*                 | inverting input
*                 | | positive power supply
*                 | | |  negative power supply
*                 | | |  |  output
*                 | | |  |  |
*                 | | |  |  |
.SUBCKT LM6181    1 2 99 50 41
*
*Features:             (TYP.)
*High bandwidth =      100 MHz
*High slew rate =      2000 V/microseconds
*Current Feedback Topology
```

LM6181 Macromodel Netlist (Continued)

```
*NOTE: Due to the addition of PSRR effects, model must be operated
*      with symmetrical supply voltages. To avoid this limitation
*      and disable the PSRR effects, see Eos below.
*
********** INPUT STAGE **********
*
GI1 99  5 POLY(1) 99 50 243.75U 2.708E-6
GI2  4 50 POLY(1) 99 50 243.75U 2.708E-6
FI1 99  5 VA3 100
FI2  4 50 VA4 100
Q1 50 3 5 QPN
Q2 99 3 4 QNN
GR1  5 6 5 6 2.38E-4
*^4.2K noiseless resistor
C1  6 99 .468P
GR2 4 7 4 7 2.38E-4
*^4.2K noiseless resistor
C2  7 50 .468P
GR3 99 8 99 8 1.58E-3
*^633ohm noiseless resistor
V1 99 10 .3
RE1 10 30 130
D1 30 8 DX
GR4 50  9 50 9 1.58E-3
*^633ohm noiseless resistor
V2  11 50 .3
RE2 11 31 150
D2  9 31 DX
Q3  8 6 2 QNI
Q4  9 7 2 QPI
DS1 3 12 DY
VA3 12 5 0
DS2 13 3 DY
VA4 4 13 0
GR6 1 99 1 99 5E-8
*^20MEG noiseless resistor
GR7  1 50 1 50 5E-8
*^20MEG noiseless resistor
GB1  1 99 POLY(2) 99 50 56 0 -1.2E-6 4E-8 1E-3
FN1  1  0 V18 1
GB2 99  2 POLY(3) 99 50 1 49 55 0 18.5E-6 -1.5E-7 -1E-7 -1E-6
FN2  2  0 V17 1
EOS 3  1 POLY(5) 99 50 45 0 47 0 57 0 59 61 -2.8E-3 9.3E-5 1 1 1 1
*To run on asymmetrical supplies, change to 0..... ^ ^
CIN1 1 0 2P
CIN2 2 0 5.75P
*
******** SECOND STAGE **********
*
I3 99 50 4.47M
R8 99 49 7.19K
R9 49 50 7.19K
V3 99 16 1.7
D3 15 16 DX
D4 17 15 DX
V4 17 50 2.0
EH 99 98 99 49 1
G1 98 15 POLY(2) 99 8 50 9 0 1.58E-3 1.58E-3
*Fp1 = 27.96 KHz
R5 98 15 2.372MEG
C3 98 15 2.4P
*
********* POLE STAGE ***********
*
*Fp = 250 MHz
```

LM6181 Macromodel Netlist (Continued)

```
G2 98 20 15 49 1E-3
R14 98 20 1K
C4 98 20 .692P
*
********* POLE STAGE ***********
*
*Fp = 250 MHz
G3 98 21 20 49 1E-3
R15 98 21 1K
C5 98 21 .692P
*
********* POLE STAGE ***********
*
*Fp = 275 MHz
G4 98 22 21 49 1E-3
R16 98 22 1K
C6 98 22 .5787P
*
********* POLE STAGE ***********
*
*Fp = 500 MHz
G5 98 23 22 49 1E-3
R17 98 23 1K
C7 98 23 .3183P
*
********* PSRR STAGE ***********
*
G10 0 45 99 0 1.413E-4
L3 44 45 26.53U
R25 44 0 10
RL3 44 45 10K
G11 0 47 50 0 1.413E-4
L4 46 47 2.27364U
R26 46 0 10
RL4 46 47 10K
*
******** THERMAL EFFECTS **********
*
I12 0 55 1
R27 0 55 10 TC = 3.453E-3 7.93E-5
I13 0 56 1E-3
R28 0 56 1.5 TC = 9.303E-4 8.075E-5
I14 0 57 1E-3
R29 0 57 3.34 TC = 3.111E-3
*
********* NOISE SOURCES ***********
*
V15 58  0 .1
D9  58 59 DN
R30 59  0 726.4
V16 60  0 .1
D10 60 61 DN
R31 61  0 726.4
V17 62  0 0
R32 62  0 73.6
V18 63  0 0
R33 63  0 1840
*
********* OUTPUT STAGE ***********
*
F6 99 50 VA7 1
F5 99 35 VA8 1
D7 36 35 DX
VA7 99 36 0
D8 35 99 DX
```

LM6181 Macromodel Netlist (Continued)

```
E1 99 37 99 23 1
VA8 37 38 0
R35 38 40 50
V5 33 40 5.3V
D5 23 33 DX
V6 40 34 5.3V
D6 34 23 DX
CF1 41 2 2.1P
L5 40 41 31N
RL5 40 41 100K
*
********* MODELS USED ***********
*
.MODEL QNI NPN(IS = 1E-14 BF = 10E4 VAF = 62.9 KF = 6.7E-14)
.MODEL QPI PNP(IS = 1E-14 BF = 10E4 VAF = 62.9 KF = 6.7E-14)
.MODEL QNN NPN(IS = 1E-14 BF = 10E4 VAF = 62.9 KF = 4.13E-13)
.MODEL QPN PNP(IS = 1E-14 BF = 10E4 VAF = 62.9 KF = 4.13E-13)
.MODEL DX D(IS = 1E-15)
.MODEL DY D(IS = 1E-17)
.MODEL DN D(KF = 1.667E-9 AF = 1 XTI = 0 EG = .3)
.ENDS
```

Simulation Accuracy

The real test of a macromodel is how the simulation results compare with the real-world device. The table below shows some of the amplifier parameters and how the simulation compares to actual device behavior. As can be seen, the goal of a 10% match between the model and the actual device was achieved.

A good figure of merit for a macromodel is the accuracy of its small-signal transient response. *Figures 14, 15* show the small-signal response of the real LM6181 and the simulation output. Notice that the simulated over-shoot and frequency of ringing closely match that of the actual device. This is due to the accurate modeling of the frequency response and output impedance capabilities of the model

romodel includes effects such as accurate input transfer response, accurate AC response, temperature effects, DC and AC PSRR, and noise. Even with the addition of all these features, the macromodel's simulation speed is still more than twice as fast as a device level micromodel. The speed advantage of this macromodel mainly comes from the fact that it converges extremely well. Since careful attention was paid to convergence during the development of the model, there is no difficulty establishing a bias point or dealing with large input signals. With detailed and accurate vendor supplied macromodels such as the one described in this paper, the designer can easily verify the effects of strays and amplifier limitations in his circuit.

Conclusion

A truly comprehensive SPICE compatible macromodel for current-feedback amplifiers has been developed. The mac-

Parameter	Typical Value	Simulation Results	% Error
$Z_{t(dc)}$ RI = 1 k Ω	127 dBΩ	126.6 dBΩ	4.5%
$BW_{3\ dB}$ A_V = −1 RI = 1 kΩ	100 MHz	103 9 MHz	3.9%
I_{B+}	1.5 µA	1.5 µA	0.0%
I_{B-}	−4.0 µA	−4.0 µA	0.0%
V_{OS}	−3.4 mV	−3.3 mV	1.2%
I_{supp}	7.5 mA	7.7 mA	2.7%
Pulse Resp. Overshoot	35%	34.8%	0.6%
Slew Rate V_{IN} = ±10V	1400 V/µs	1468 V/µs	4.8%
I_{SC}	130 mA	136.8 mA	5.2%
e_n	5 nV/√Hz	4.9 nV/√Hz	2.0%
I_{n+}	3 pA/√Hz	2.96 pA/√Hz	1.3%
i_{n-}	16 pA/√Hz	15.1 pA/√Hz	5.6%

Conclusion (Continued)

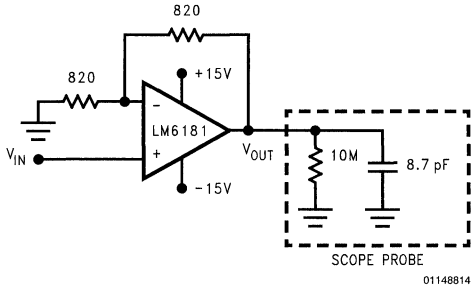

FIGURE 12. Non-inverting amplifier. A_V = +2. It is very important to include a model of the scope probe on the output of the amplifier to obtain reasonable results from the simulation.

```
*LM6181 Small-Signal Response. Av = +2.
*Rf = Rg = 820ohm.
*
XAR1 3 2 7 4 6 LM6181
VP 7 0 15V
VN 4 0 -15V
VIN 3 0 PULSE (-.2V .2V 40N .2N .2N)
RF 6 2 820ohm
RI 2 0 820ohm
RL 6 0 10MEG
CL 6 0 8 7pF
.LIB CF.LIB
.OPTIONS RELTOL = .0001 CHGTOL = 1E-20
.TRAN/OP .1N 200N
.PROBE
.END
```

FIGURE 13. Non-Inverting Amplifier Netlist [9]

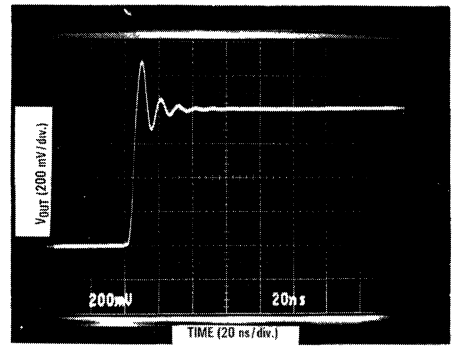

FIGURE 14. LM6181 Small-Signal Transient Response

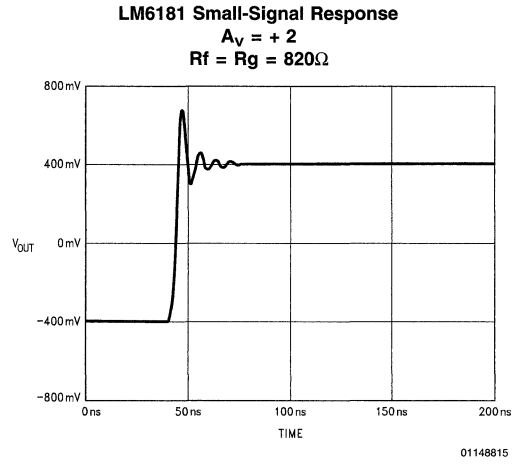

FIGURE 15. LM6181 SimulatedTransient Response

Conclusion (Continued)

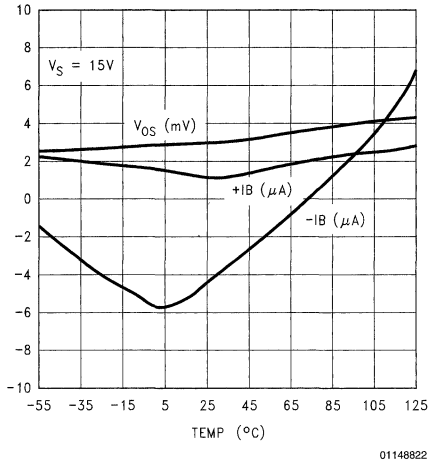

FIGURE 16. LM6181 Temperature Effects

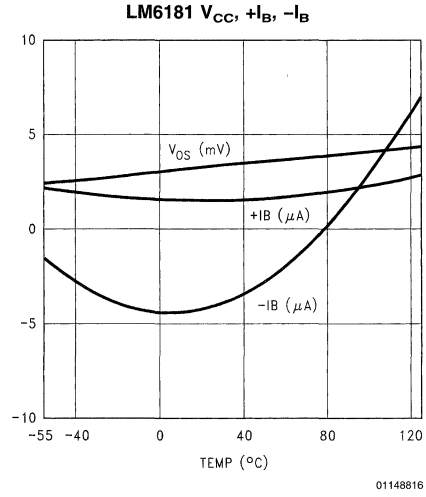

FIGURE 17. LM6181 Simulated Temperature Effects

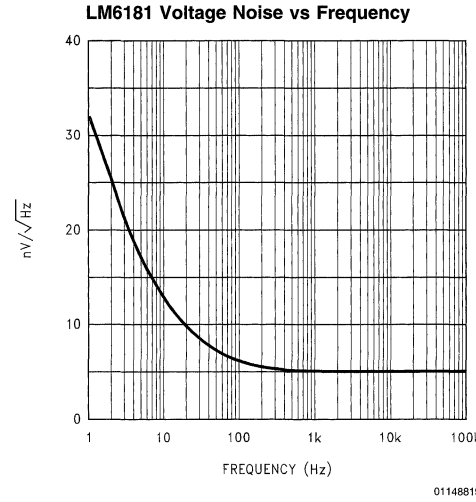

FIGURE 18. LM6181 Voltage-Noise Response

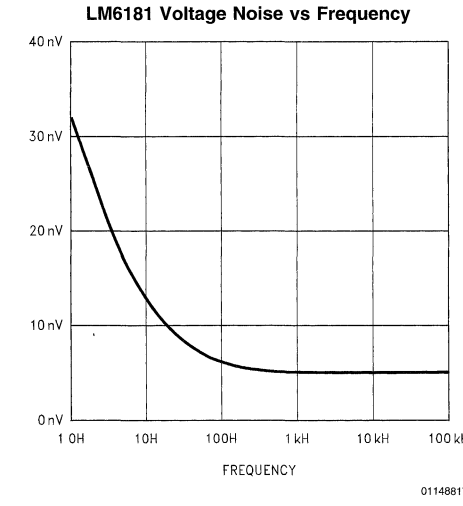

FIGURE 19. LM6181 Simulated Voltage-Noise Response

Conclusion (Continued)

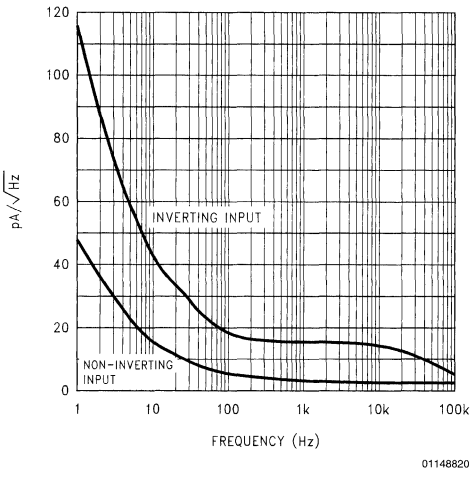

FIGURE 20. LM6181 Current-Noise Response

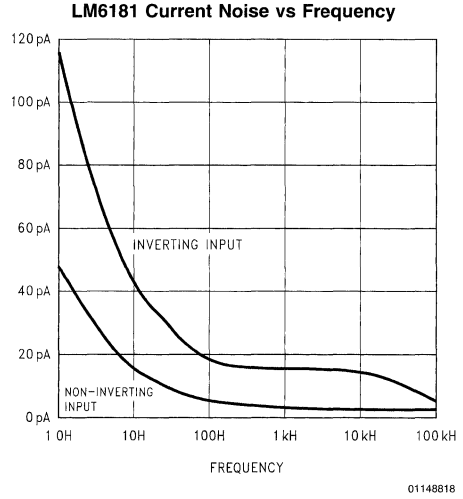

FIGURE 21. LM6181 Simulated Current-Noise Response

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CLC5506 Evaluation Board

National Semiconductor
Application Note 1138

The CLC5506PCASM is a fully assembled and tested evaluation module for CLC5506 Gain Trim Amplifier. The evaluation module simplifies the task of making frequency response and noise figure performance evaluation of the CLC5506 Gain Trim Amplifier (GTA).

The evaluation circuit is carefully designed and laid out on an FR4 printed circuit board (part number: CLC730102). Refer to *Figure 1* for the schematic diagram of the CLC5506PCASM.

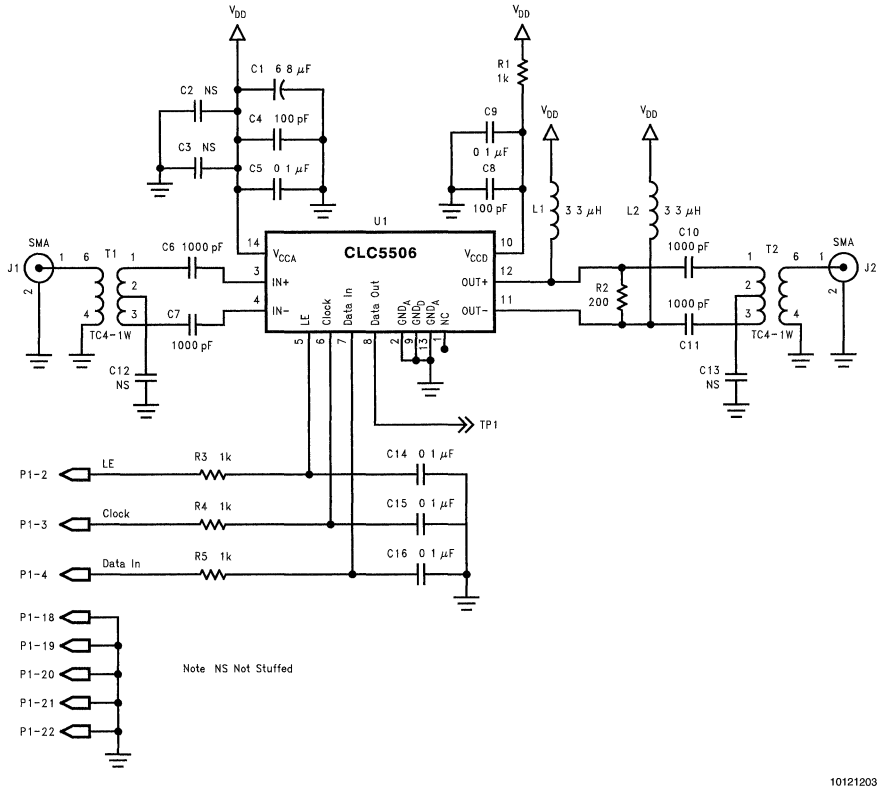

FIGURE 1. CLC5506PCASM Schematic Diagram

The differential input impedance of CLC5506 between pins IN^+ and IN^- is 200Ω. The differential output impedance between pins OUT_+ and OUT_- is set to 200Ω by resistor R2. Two 4:1 impedance ratio transformers (T1 and T2) are used for wide band matching to a single ended 50Ω system to simplify evaluation. The 3.3µH inductor at L1 and L2 are used as RF chokes for the open collector outputs. Resistor R1 and V_{CCD} is used to reduce noise cross-talk between the V_{CCA} and V_{CCD}. The low pass RC networks (R3, R4, R5 and C14, C15, C16) at LE, Clock and Data In pins are used to reduce AC feed-through to the RF circuitry.

Windows-95/98/NT GTA control software, developed by National Semiconductor can be used to send control data to the CLC5506 Gain Trim Amplifier. This software along with the CLC5506 Datasheet can be downloaded from National Semiconductor Corporation Web site at http://www.national.com.

Figure 2, shows the typical test setup block diagram for the measurement of frequency response parameters.

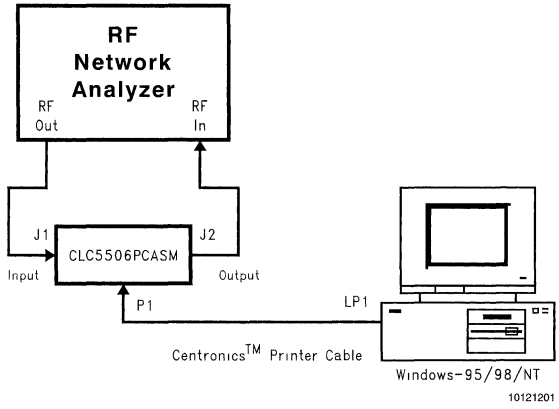

FIGURE 2. Test Setup Block Diagram for Frequency Response Measurement

Figure 3, shows the typical test setup block diagram for the measurement of noise figure parameter. A RF noise source was used. During the noise figure measurement, the Centronics™ printer cable connected to P1 should be disconnected from the evaluation module and removed from the measurement area to reduce PC EMI noise pick-up.

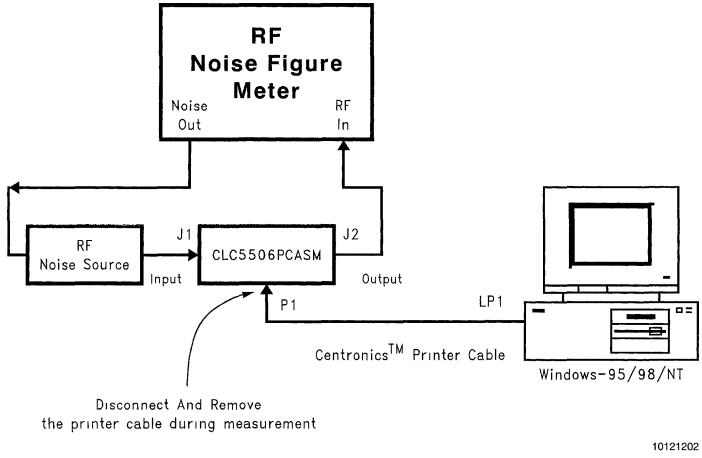

FIGURE 3. Test Setup Block Diagram for Noise figure Measurement

RF transformers T1 and T2 have intrinsic losses, the actual RF performance of the CLC5506 per se, could be calculated by accounting for T1 and T2 losses in the evaluation module.

Refer to *Table 1* for correction factor for gain measurement and noise figure measurement based on typical losses measured on the transformers specified in *Table 2*.

TABLE 1. Gain and Noise Figure Correction Factor

Frequency (MHz)	Gain Measurement Correction Factor (dB)	Noise Figure Measurement Correction Factor (dB)
50	1.6	0.8
60	1.6	0.8
70	1.6	0.8
80	1.7	0.85
90	1.7	0.85
100	1.7	0.85
110	1.7	0.85
120	1.8	0.9
130	1.8	0.9
140	1.8	0.9
150	1.8	0.9
160	1.8	0.9
170	1.8	0.9
180	1.9	0.95
190	1.9	1.9
200	1.9	1.9
210	1.9	0.95
220	2.0	1.0
230	2.0	1.0
240	2.0	1.0
250	2.0	1.0
260	2.1	1.05
270	2.1	1.05
280	2.2	1.1
290	2.2	1.1
300	2.2	1.1
310	2.2	1.1
320	2.3	1.15
330	2.3	1.15
340	2.3	1.15
350	2.4	1.2
360	2.4	1.2
370	2.5	1.25
380	2.5	1.25
390	2 5	1.25
400	2.5	1.25
500	3.8	1.9
600	4.4	2.2

TABLE 2. Bill of Materials for CLC5506PCASM

Reference	Description	Part No. or Note	Distributor	Qty.
T1,2	Transformer	Mini-Circuits TC4-1W	Mini-Circuits	2
P1	Connector	Norcomp, TT57-LE40360	DigiKey/ 1036RF-ND	1
J1,2	SMA connector	Femal Right Angle PCB Mount	DigiKey/ ARFX1232-ND	2
C4,8	Cap, 100pF, 5%	0805 SMD package	Generic	3
C6,7,10,11	Cap, 1000pF, 10%	1206 SMD package	Generic	4
C5,9,14,15,16	Cap, 0.1µF, 20%	0805 SMD Package	Generic	6
C1	Cap, 6.8µF, Tant., 16V	3528 SMD package	Generic	1
R1.3,4,5	Res 1K, 5%, 1/8W	1206 SMD Package	Generic	4
R2	REs, 200, 5%, 1/8W	1206 SMD Package	Generic	1
L1,2	Inductor, 3 3µH	1008 SMD Package	CoilCraft	2
VCC, GND	Single Header	0.1" header	Generic	2
U1	CLC5506IM PCB	14-PIN SOIC CLC730102	National Semiconductor National Semiconductor	1 1

For insertion gain measurement of the frequency response, the correction factor is the total insertion loss of T1 and T2. This correction factor shall be added back to the insertion gain reading of network analyzer to get the actual gain performance of CLC5506.

For the noise figure measurement, the correction factor is the insertion loss of T1 (or half the total loss of T1 and T2). This correction factor shall be deducted from the noise figure reading of noise figure meter.

Figure 4 and *Figure 5* on the following page, illustrate the top and bottom side layout of the CLC730102. *Figure 6*, also on the following page, is the assembly drawing of CLC5506PCASM.

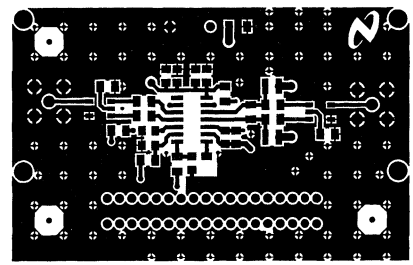

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FIGURE 4. CLC730102 (Top Side)

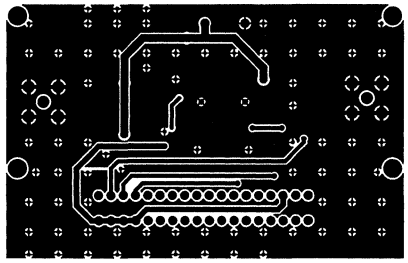

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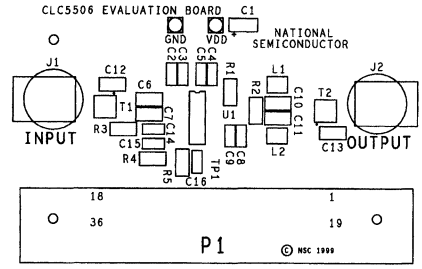
FIGURE 5. CLC730102 PCB (Bottom Side)



10121204

FIGURE 6. CLC5506PCASM Component Layout (Top Side)

In order to achieve the same performance as specified in the CLC5506 datasheet, components should be chosen from the bill of material attached and installed per *Figure 6*.

Note: The circuits included in this application note have been tested with National Semiconductor parts that may have been obsoleted and/or replaced with newer products. Please refer to the CLC to LMH conversion table to find the appropriate replacement part for the obsolete device.

An OrCAD PSPICE Library for the VIP10 High-Speed Op Amp

National Semiconductor
Application Note 1255
Barry Yuen

Creating the op amp SPICE model from ground-up for simulation is esoteric and often time consuming.

National Semiconductor Corporation has an OrCAD Capture library (**nationalhighspeed.olb**) and PSPICE (**nationalhighspeed.lib**) model library for the industry-leading VIP10™ process high-speed operational amplifiers. These libraries contain behavior models of the LMH series high-speed operational amplifiers and the schematic symbols of op amp. These libraries are available for download from **amplifiers.national.com**. Libraries are created from OrCAD PSPICE A/D version 9.1 and have been verified to match the performance in the datasheet

The VIP10 is a high-speed, dielectrically-isolated, complementary bipolar IC process that utilizes deep trench technology on a bonded wafer for complete dielectric isolation and optimal high-speed amplifier performance. Trench technology with bonded wafers helps minimize parasitic capacitance for optimal power-to-bandwidth performance, lower distortion and decreased die size.

When doing the simulation, the path of **nationalhighspeed.lib** needs to be added under either the "Include Files" option or the "Libraries" option in the "Simulation Profile".

The ADSL Analog Front End for Customer Premises Equipment

One of the very popular applications for LMH high-speed operational amplifiers is the DSL analog front end in the customer premises equipment side. The new LMH6643 rail-to-rail output, LMH6672 line driver, and LMH6622 low-noise op amps form a robust chipset solution that maximizes the ADSL baseband DSP performance as shown in *Figure 1*.

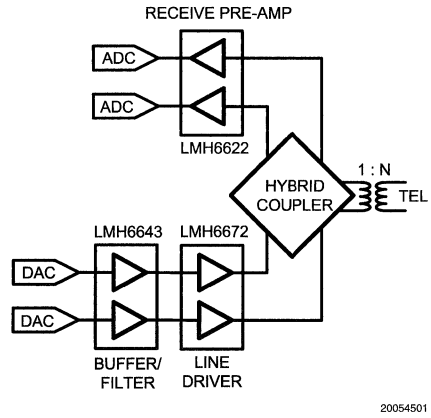


FIGURE 1. Block Diagram of ADSL CPE Analog Front End

The LMH6643 as a Buffer Amplifier for the D/A Converter

A pair of LMH6643 is used as a differential buffer amplifier at the outputs of digital-to-analog converter for providing impedance matching, isolation, and driving capability to an optional low pass filter between the LMH6643 and the LMH6672. *Figure 2* shows the OrCAD schematic to demonstrate the use of SPICE model. The voltage gain of this inverting buffer amplifier is simply defined as $-R_{B1+}/R_{B2+}$ and $-R_{B1-}/R_{B2-}$.

The LMH6643 as a Buffer Amplifier for the D/A Converter (Continued)

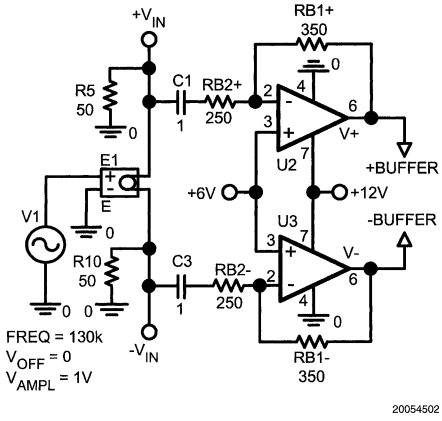


FIGURE 2. LMH6643 as an ADC Buffer in ADSL CPE Analog Front End

The LMH6672 as an Upstream Line Driver

The LMH6672 is used as an upstream DSL line driver because of its high-output drive with low distortion and single supply features. When connected as a differential output driver, the LMH6672 can drive a 50Ω load to 16.8 V_{PP} swing with only −93 dBc distortion and fully supports the peak upstream power levels for full-rate ADSL. *Figure 3* is a typical line driver circuit driving the 100Ω twisted-pair transmission line through a 1:2 transformer. The voltage gain of this non-inverting driver amplifier is simply defined as $(1+2*R_F+/R_G)$ or $(1+2*R_F-/R_G)$. The capacitor C_G is inserted to set a DC gain of 1 V/V.

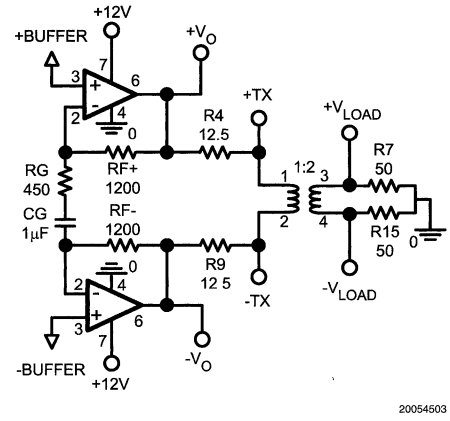


FIGURE 3. LMH6672 as a Differential Driver to a 50Ω Differential Load

The LMH6622 as a Downstream Low-Noise Pre-Amp

The LMH6622 is used as a low-noise pre-amp in the downstream link because of its low noise and low-distortion performance. This twin personality ensures the receiving path has high dynamic range to meet the stringent linearity and noise requirements of the ADSL standard.

In *Figure 4*, the LMH6622 is used as an inverting summing amplifier to provide both receive pre-amp channel gain and driver echo signal cancellation. In order to cancel the unwanted driver echo signal in the receive path, R_{1+} is set to be $2*R_{2+}$ and R_{1-} is set to be $2*R_{2-}$.

In reality, the hybrid rejection is about 12 dB due to imperfect matching. The resistors values in the simulation can be adjusted to experience the real performance of the receive circuit.

The LMH6622 as a Downstream Low-Noise Pre-Amp (Continued)

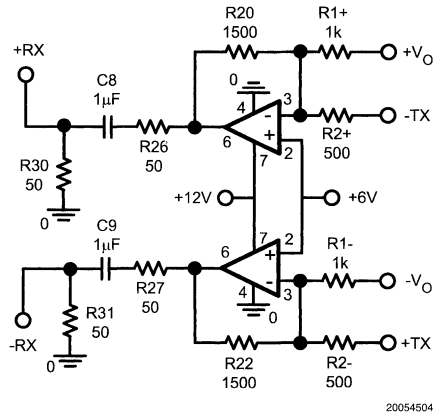


FIGURE 4. LMH6622 as a Low-noise Pre-amp in the ADSL Downstream

Figure 5 shows the differential output voltage across the twisted-pair-transmission line and the unwanted echo signal at the pre-amp's outputs. Perfect cancellation of the unwanted echo signal is possible only if perfect matching is achieved.

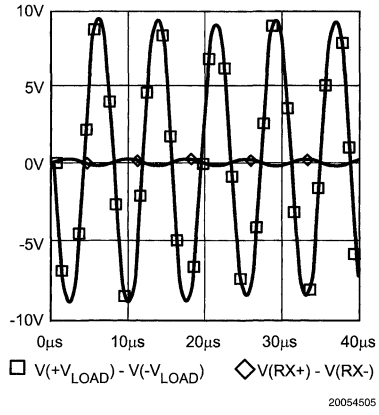


FIGURE 5. Simulation Results at the Transmission Line and Pre-amp's Output

In conclusion, PSPICE models and Capture symbols for National's high-speed op amps can be downloaded from **amplifiers.national.com** and used for simulation.

Simulation SPICE Models for Comlinear's Op Amps

National Semiconductor Corporation is a manufacturer and supplier of high-performance analog signal processing components. National's broad signal conditioning product line includes high-speed hybrid and monolithic operational amplifiers, buffers, video amplifiers, multiplexers, automatic gain control integrated circuits, track/hold amplifiers, and analog-to-digital converters. National continues as a leader in developing products offering exceptional performance, speed, quality, reliability and service.

Introduction

This is a collection of PSpice compatible models for National Semiconductor Corporation amplifiers. For additional information about SPICE Models supporting existing or new products, customers can visit National's web site at *http://www.national.com*. These SPICE Models are created for use on an IBM compatible computer using analysis programs that accept Spice formats. National assumes no responsibility for designs created from these SPICE Models. These SPICE Model files model typical performance at room temperature. AC response is dominated by board layout and package parasitics at frequencies above 500MHz. Before designs are released to production, National suggests that topologies be verified by prototyping the circuit. The part-to-part and over-temperature performance variations of National amplifiers are specified in current data sheets found on National's web site. The changes from the last SPICE Model version are listed in this table:

TABLE 1. Updates to Spice Models

File Name	Description
CLC405.CIR	A new SPICE Model.
CLC406.CIR	A revised SPICE Model.
CLC407.CIR	A new SPICE Model.
CLC412.CIR	A new SPICE Model.
CLC430.CIR	A revised SPICE Model that improves disabled output response.
CLC440.CIR	A new SPICE Model.
CLC449.CIR	A new SPICE Model.
CLC450.MOD	A new SPICE Model.

TABLE 2. Spice Model Subcircuit Files

File Name	Description
CLC109.CIR	A Low-Power, Wideband, Closed-Loop Buffer.
CLC111.CIR	A Very Wideband, Ultra-High Slew Rate, Closed-Loop Buffer.
CLC400.CIR	A Wideband, Low-Gain Monolithic Current Feedback Op Amp with Fast Settling (0.05% in 12 ns), Low Power, and an Input Offset Adjustment Pin.
CLC401.CIR	A Wideband, High-Gain Monolithic Current Feedback Op Amp with Fast Settling (0.01% in 10 ns) and Low Power.
CLC402.CIR	A Low-Gain Monolithic Current Feedback Op Amp with Fast 14-bit Settling (0.0025% in 25 ns) and Low Power.
CLC404.CIR	A Wideband Monolithic Current Feedback Op Amp with High Slew Rate.
CLC405.CIR	A Low-Cost, Low Power, and 110 MHz Op Amp with Disable.
CLC406.CIR	A Wideband, Low-Cost, Low-Power Monolithic Current Feedback Op Amp.
CLC407.CIR	A Low-Cost, Low Power, Programmable Gain Buffer with Disable.
CLC409.CIR	A Very Wideband, Low Distortion Monolithic Current Feedback Op Amp.
CLC410.CIR	A Video Monolithic Current Feedback Op Amp with disable, Fast Settling (0.05% in 12 ns) and an Input Offset Adjust Pin.
CLC412.CIR	A Dual Wideband Video Op Amp.
CLC414.CIR	A Quad, Low-Power Monolithic Current-Feedback Op Amp.
CLC415.CIR	A Quad Wideband Monolithic Current Feedback Op Amp.
CLC420.CIR	A High-Speed, Unity Gain Stable Monolithic Voltage Feedback Op Amp.
CLC425.CIR	An Ultra Low-Noise, Wideband Monolithic Voltage Feedback Op Amp with Current Supply Adjust.
CLC426.CIR	An Ultra Low-Noise, Wideband Monolithic Voltage Feedback Op Amp with Current Supply Adjust and External Compensation.
CLC428.CIR	An Ultra Low-Noise, Wideband, Dual Monolithic Voltage Feedback Op Amp.
CLC430.CIR	A Wideband Monolithic Current Feedback Op Amp with disable and ±5V to ±15V supply capability.
CLC431.CIR	A Dual, Wideband Monolithic Current Feedback Op Amp with High Slew Rate.
CLC432.CIR	A Dual, Wideband Monolithic Current Feedback Op Amp with Disable and ±5V to ±15V Supply Capability.

Introduction (Continued)

TABLE 2. Spice Model Subcircuit Files (Continued)

File Name	Description
CLC440.CIR	A High-Speed, Low-Power Voltage Feedback Op Amp.
CLC449.CIR	A 1.2 GHz Ultra-Wideband Monolithic Op Amp.
CLC450.MOD	A Single Supply, Low Power, High Output, Current Feedback Amplifier.
CLC501.CIR	A High-Speed Output Clamping Monolithic Current Feedback Op Amp for High Gains.
CLC502.CIR	A High-Speed Output Clamping Monolithic Current Feedback Op Amp with Fast 14-bit Settling (0.0025% in 25 ns) for Low Gain.
CLC505.CIR	A High-Speed, Programmable-Supply Current, Monolithic Current Feedback Op Amp.
CLC520.CIR	A Monolithic Amplifier with Voltage Controlled Gain (AGC).
CLC522.CIR	A Monolithic Wideband Variable Gain Amplifier.
CLC532.CIR	A High-Speed, 2:1 Analog Multiplexer with fast 12-bit settling (0.01% in 17 ns), Low Noise, Low Distortion, and Adjustable Noise Bandwidth.
CLC5644.CIR	A Quad, Low-Power Monolithic Current-Feedback Op Amp.
CLC5655.CIR	A Quad Wideband Monolithic Current Feedback Op Amp.
CLC5665.CIR	A Wideband Monolithic Current Feedback Op Amp with Disable and ±5V to ±15V Supply Capability.
CLC5801.CIR	An Ultra Low-Noise, Wideband Monolithic Voltage Feedback Op Amp with Current Supply Adjust.
CLC5802.CIR	An Ultra Low-Noise, Wideband, Dual Monolithic Voltage Feedback Op Amp.

Start Up Instructions

Download all SPICE Model files of interest to a library on the hard disk. If the library directory is not in the SPICE program's path, the user should set that path in the autoexec-.bat for easier excess. The .INC statement in PSpice should be used in the simulation file to include the SPICE Models subcircuit.

Example: ".INC CLC400.CIR"

Amplifier Spice Models

These SPICE Model files are written in ASCII file format for IBM-compatible PC's. They are compatible with PSpice and other Spice 2G simulators. For additional detailed information about using PSpice please contact MicroSim (See Reference below). National amplifier SPICE Models are written in a subcircuit format for easy incorporation into larger circuits. A listing of any amplifier subcircuit may be obtained by printing its CLC*.CIR file to a local printer. The subcircuit node assignments match the device pin-outs as shown in the individual device data sheets. An example is an 8 pin op amp.

- Connections: NON-INVERTING INPUT PIN
- | INVERTING INPUT PIN
- | | OUTPUT
- | | | $+V_{CC}$
- | | | | $-V_{CC}$
- | | | | |
- SUBCKT (NAME) 3 2 6 7 4

Some schematic capture software packages require a different pin connection other than what National uses. Changing the pin order in the .SUBCKT statement will not affect the SPICE Model performance.

Performance Results

When substitutions of current feedback op amps are made for voltage feedback op amps, results may not be acceptable. Refer to National 's application note OA-13 for a tutorial on current feedback op amp design.

Parameters Modeled

The following typical performance parameters are modeled by the SPICE Models.

DC EFFECTS

- VIO, IBI, IBN
- Supply current vs. supply voltages
- Common mode input/output voltage range
- Load current from supplies
- CMRR

AC EFFECTS < 500 MHz

- Frequency response vs. gain & load
- Open loop gain & phase
- Noise
- Small signal input/output impedance

TIME DOMAIN

- Rise/fall times
- Slew rates

SPECIAL FEATURES (WHERE APPLICABLE)

- Output clamping
- Supply current adjustment
- Offset voltage adjust
- Disable/enable times
- External compensation

Parameters Not Modeled

- Differential gain and phase
- PSRR
- Harmonic distortion
- Fine scale settling performance
- Thermal tail

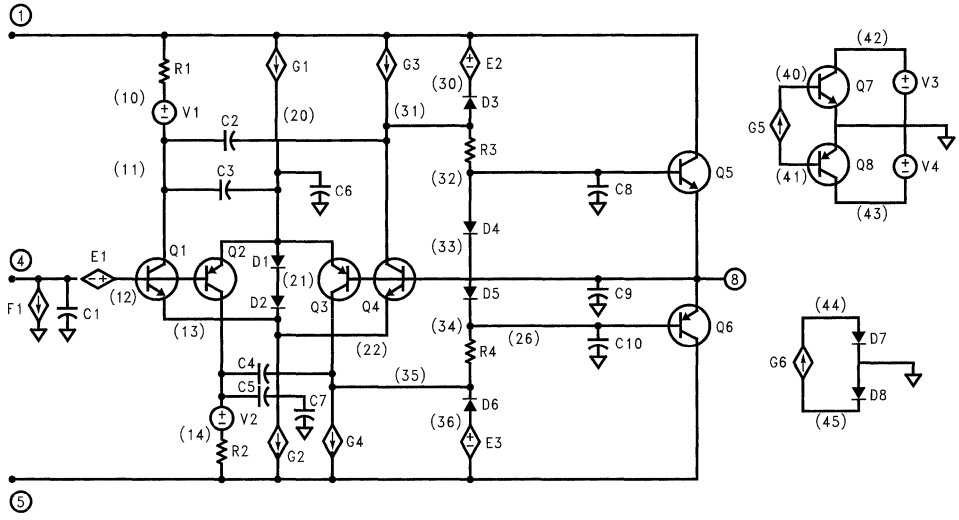
Parameters Not Modeled (Continued)

- Overdrive recovery time (Except for the CLC501and the CLC502)
- Variation in performance vs. temperature
- Part-to-part performance variation

Notice

The information provided within these files and documents is believed to be reliable and correct. National assumes no responsibility for alterations, omissions or inaccuracies. National assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. National does not grant licenses or patent rights to any of the circuits described within this document.

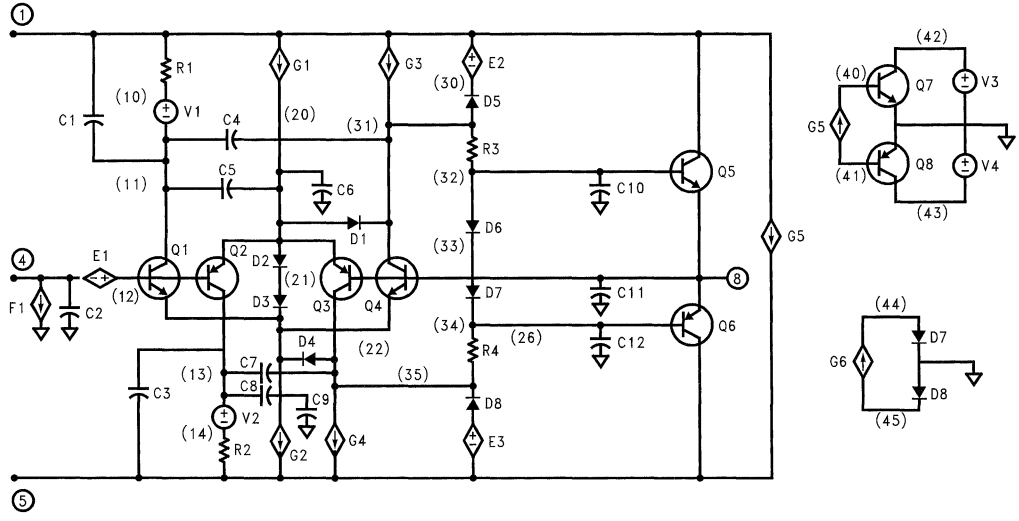
CLC109



01278401

Note: Circled number denotes PIN number and number in parenthesis denotes NODE number

CLC111



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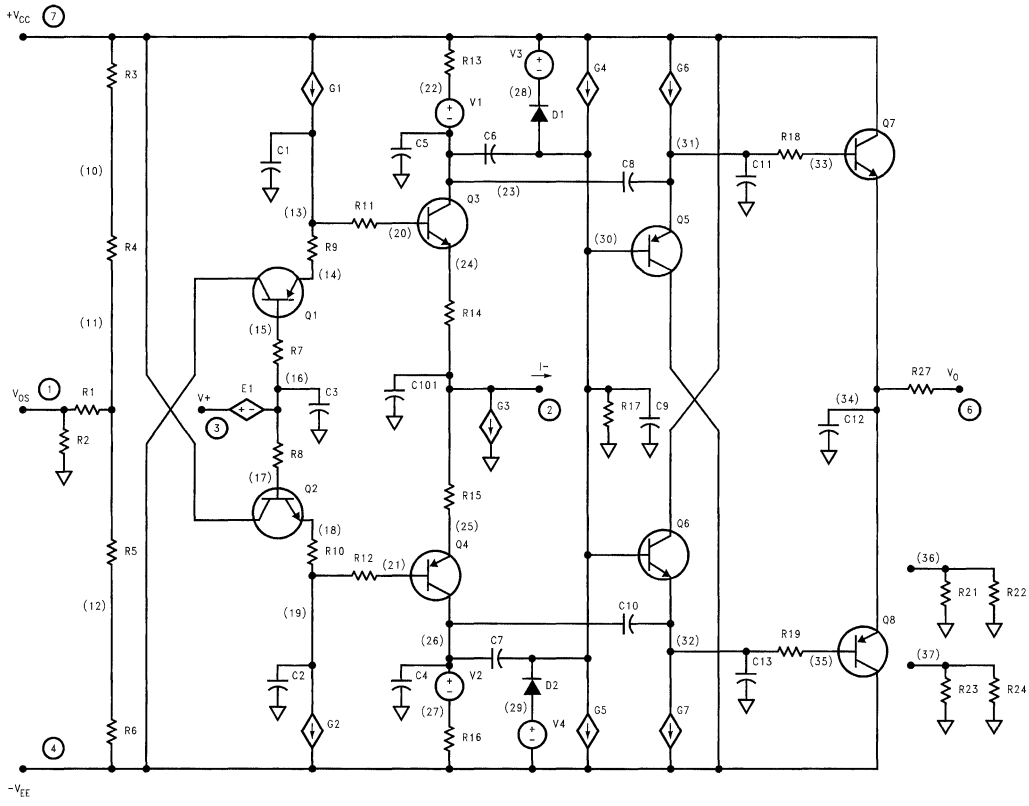
Note: Circled number denotes PIN number and number in parenthesis denotes NODE number

CLC400



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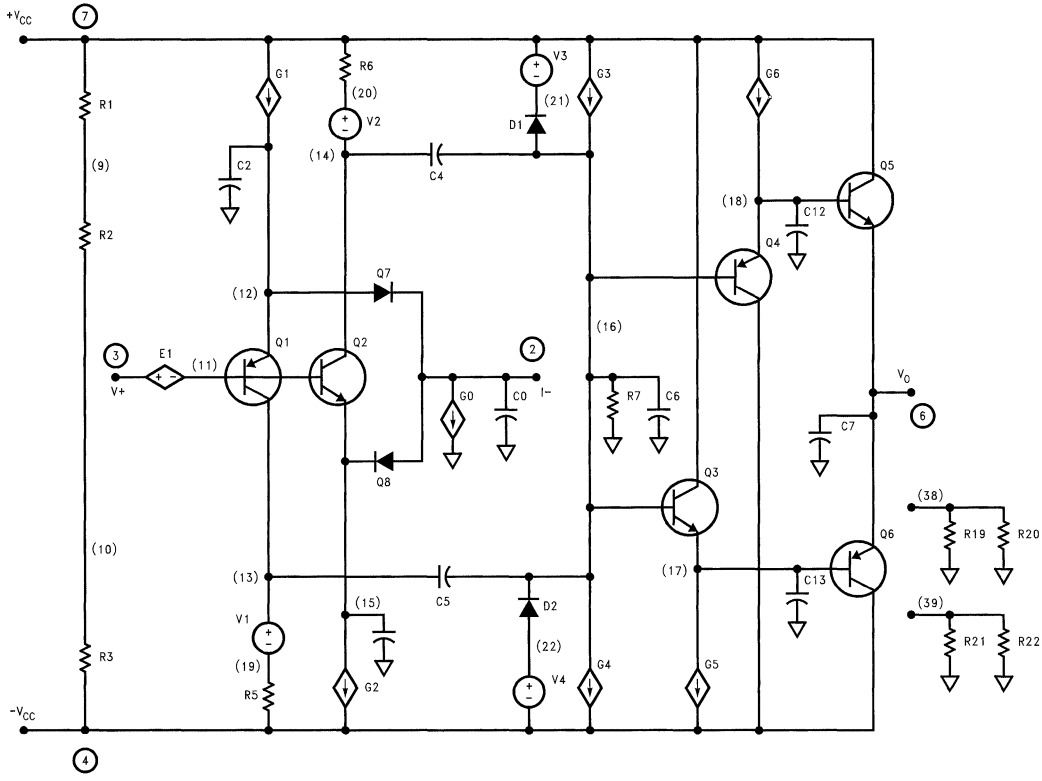
Note: Circled number denotes PIN number and number in parenthesis denotes NODE number

CLC401



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Note: Circled number denotes PIN number and number in parenthesis denotes NODE number

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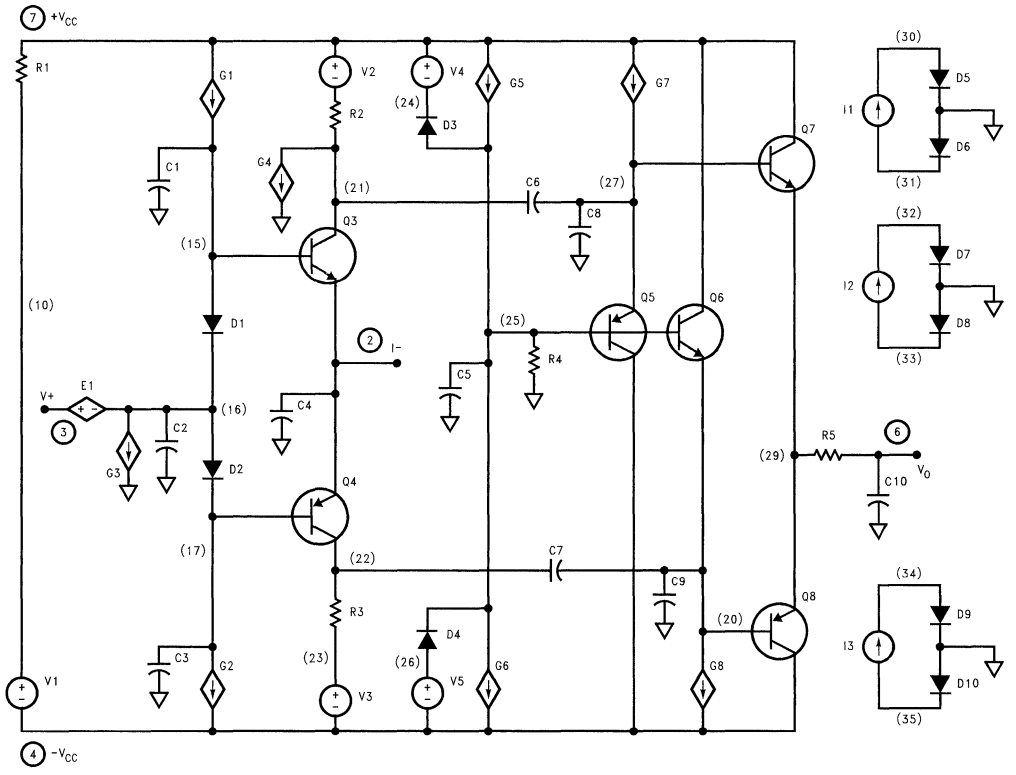
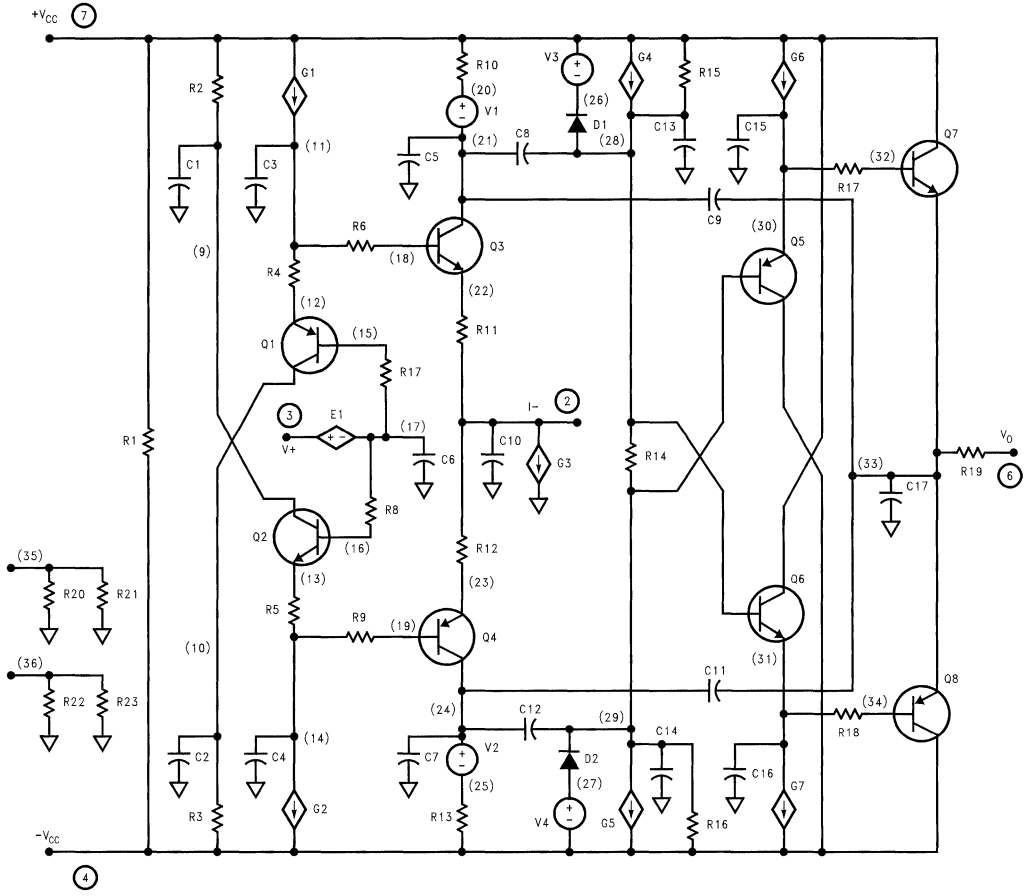


Note: Circled number denotes PIN number and number in parenthesis denotes NODE number

CLC404



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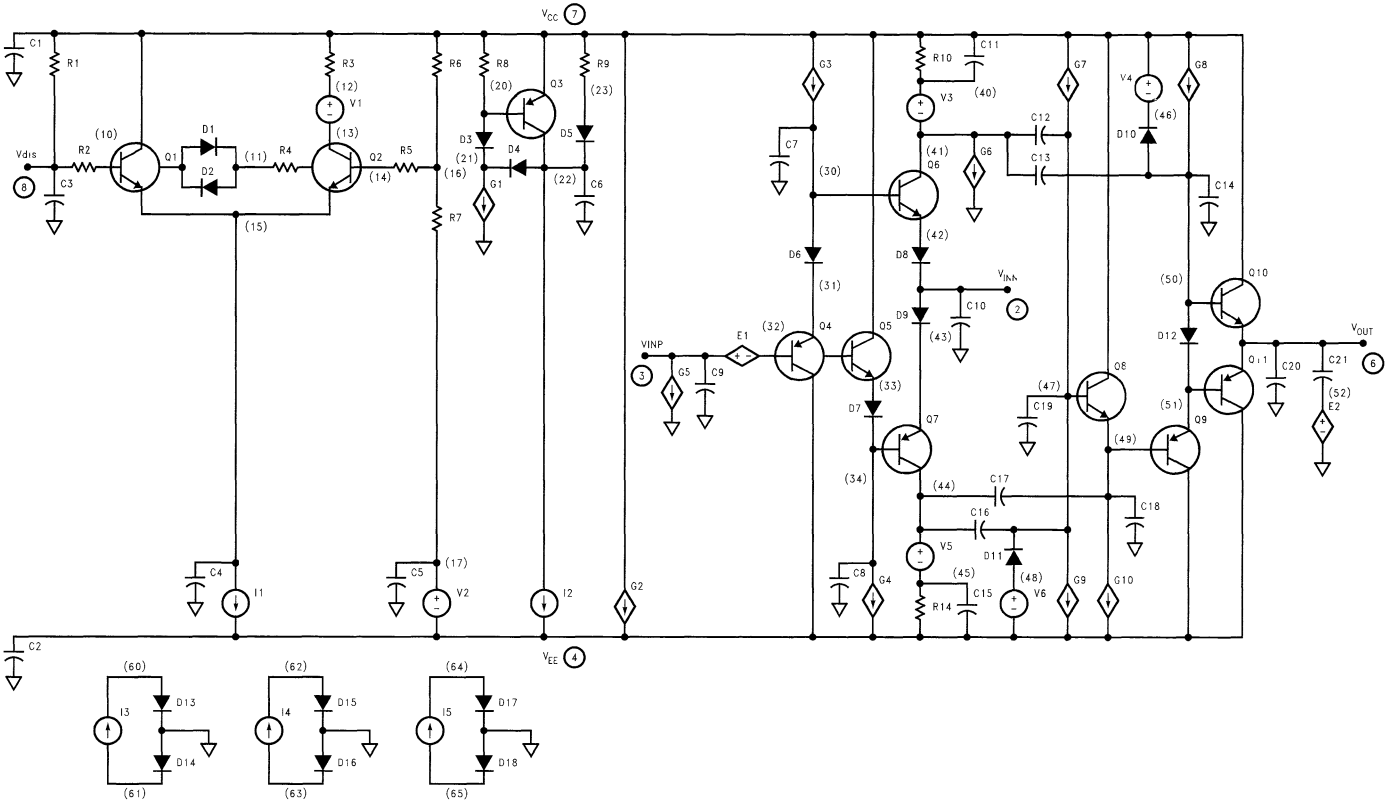

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Note: Circled number denotes PIN number and number in parenthesis denotes NODE number

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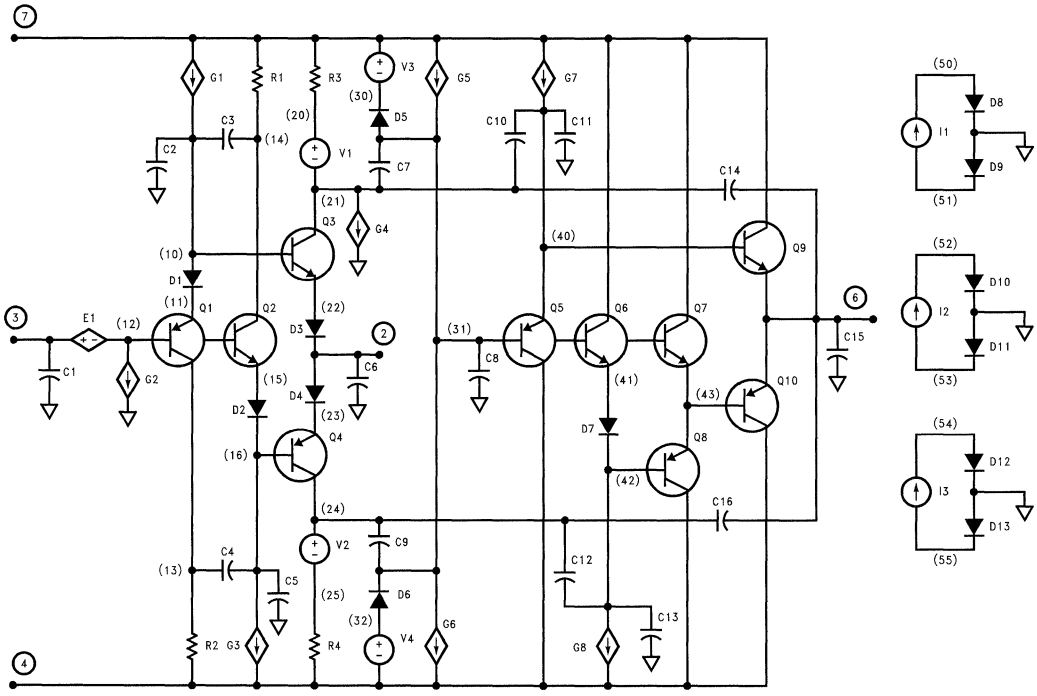

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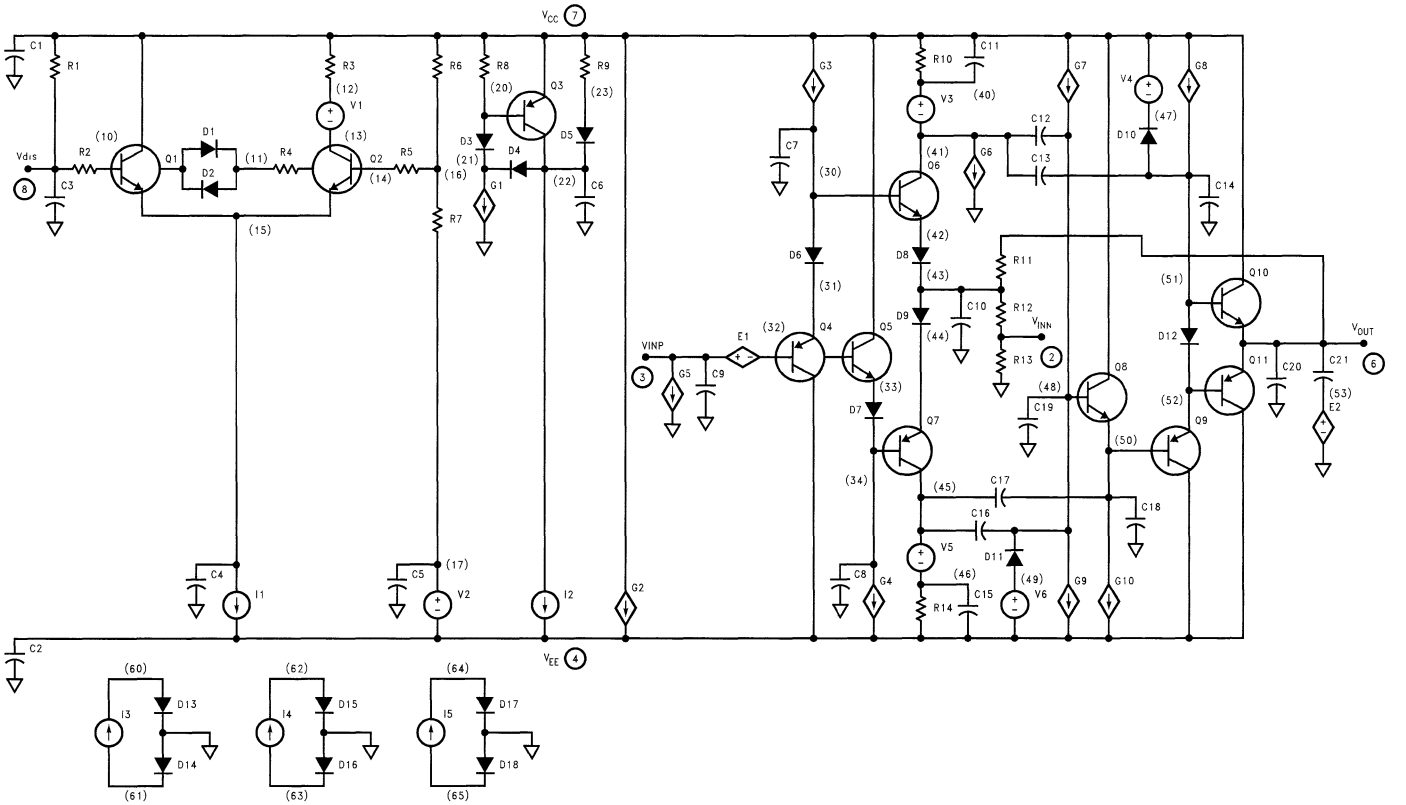
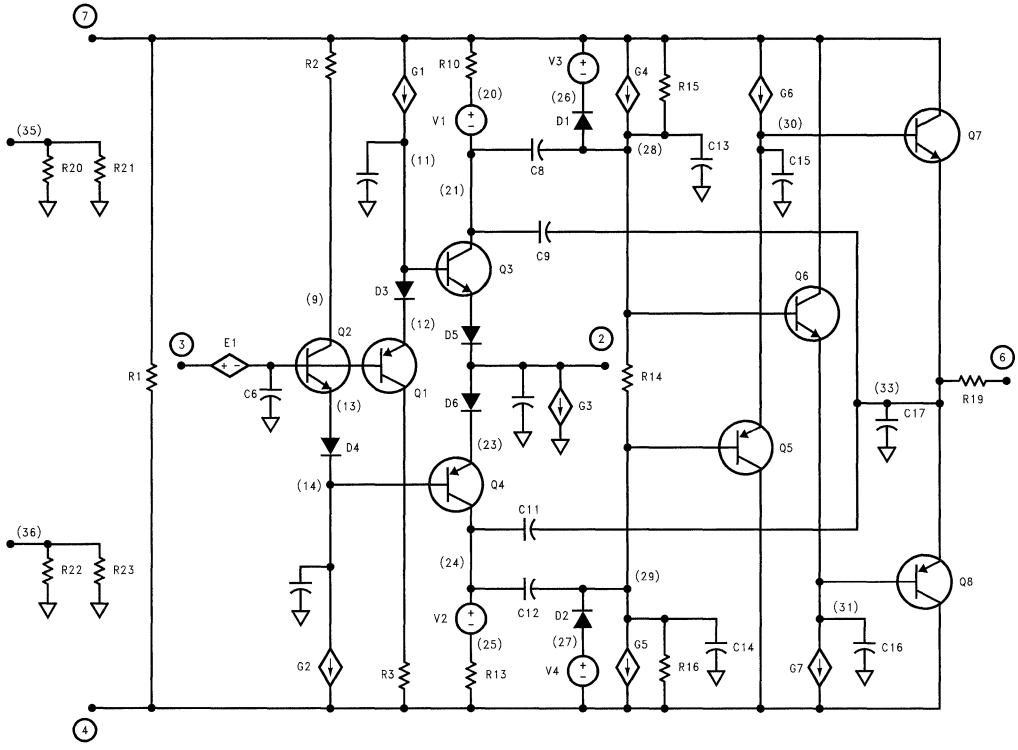


Note: Circled number denotes PIN number and number in parenthesis denotes NODE number

CLC409



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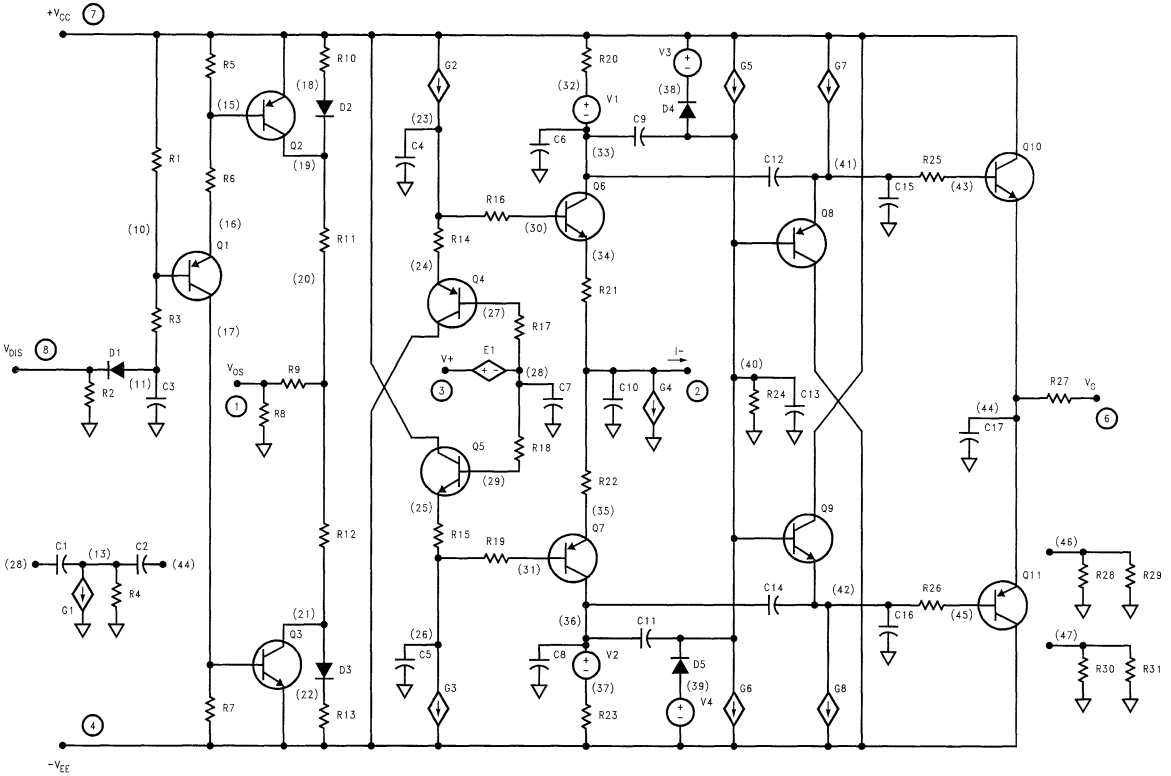
Note: Circled number denotes PIN number and number in parenthesis denotes NODE number



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Note: Circled number denotes PIN number and number in parenthesis denotes NODE number

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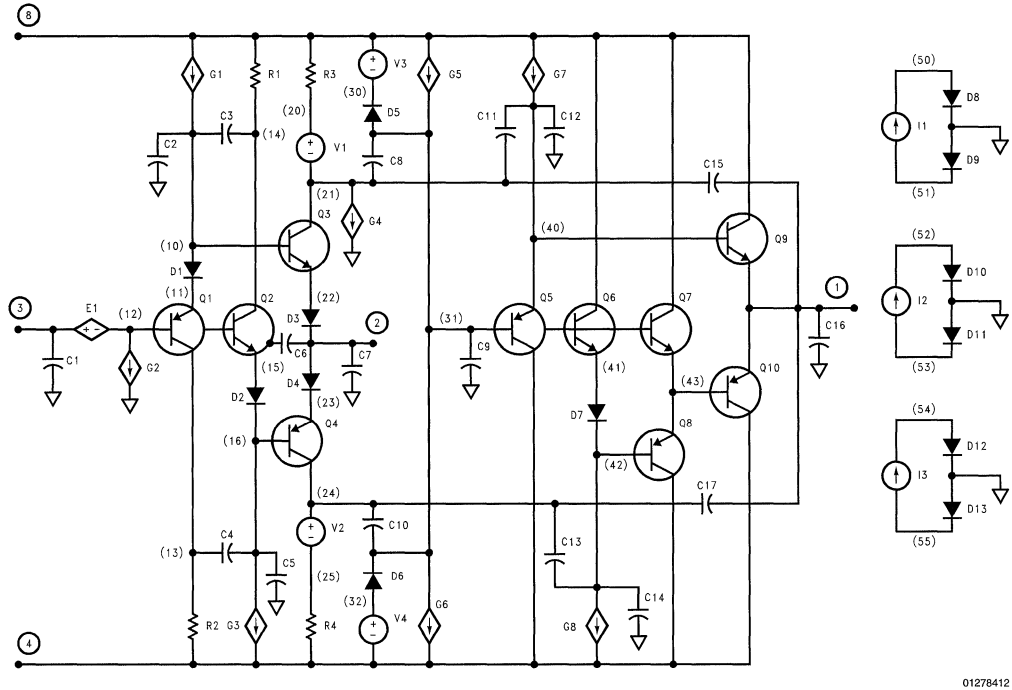

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Note: Circled number denotes PIN number and number in parenthesis denotes NODE number

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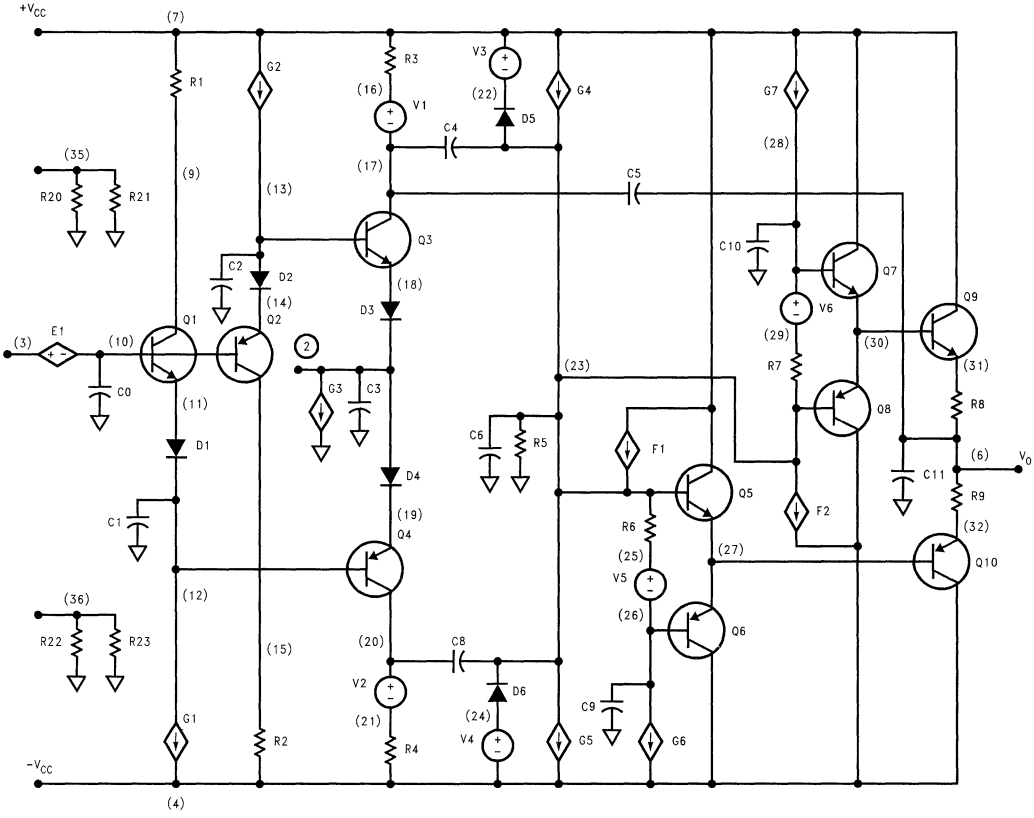

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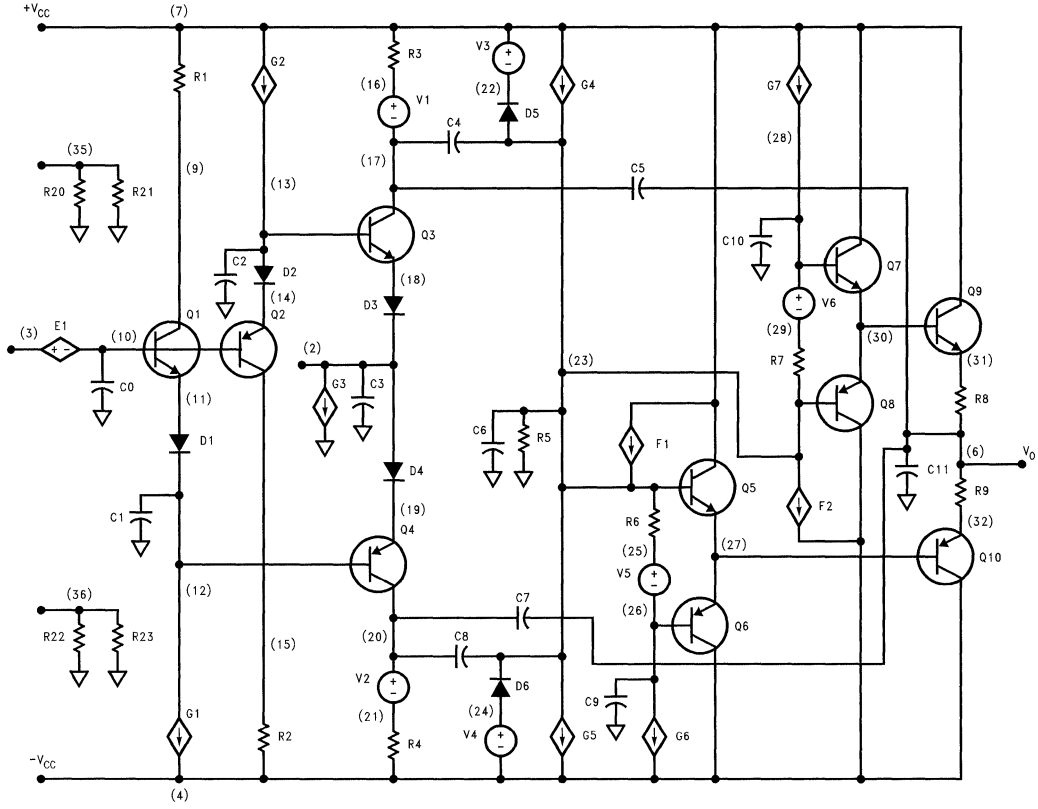

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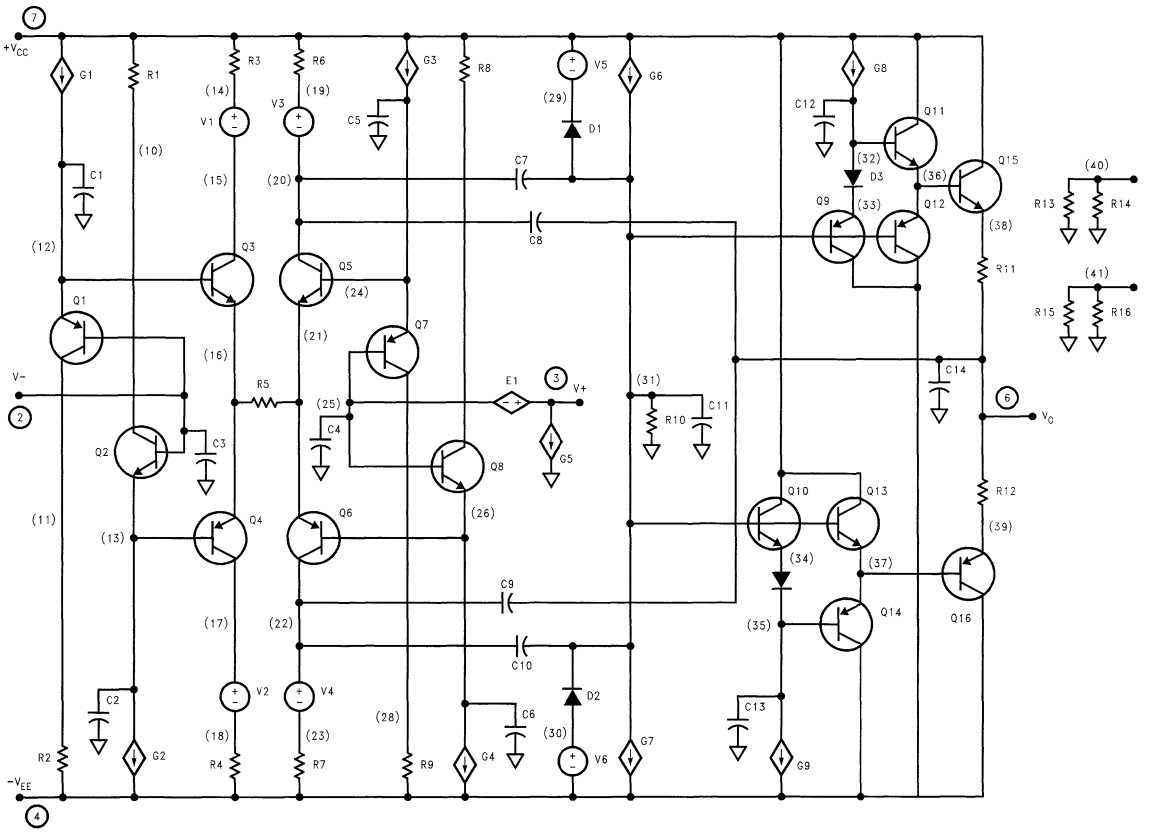

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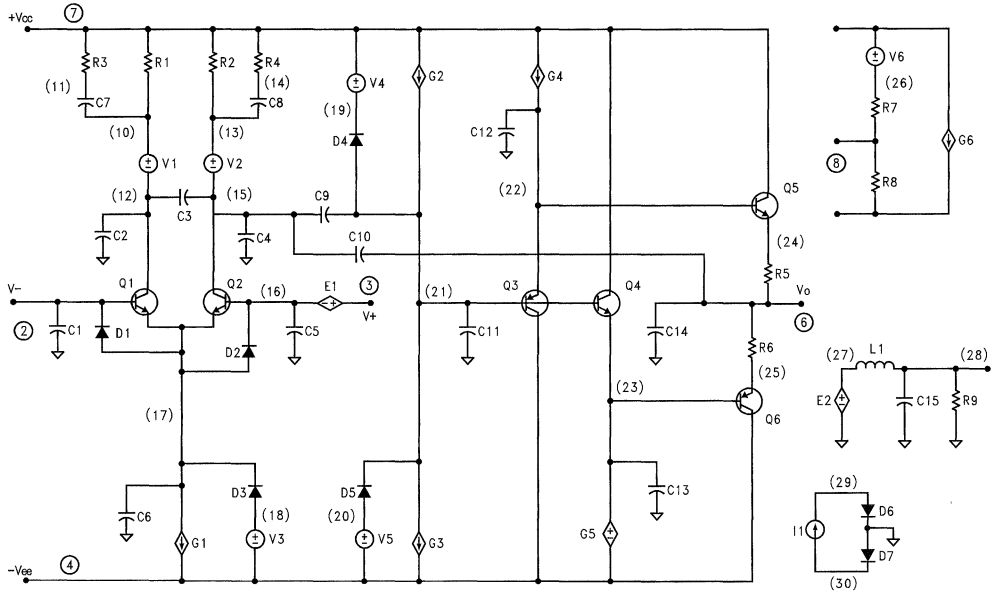

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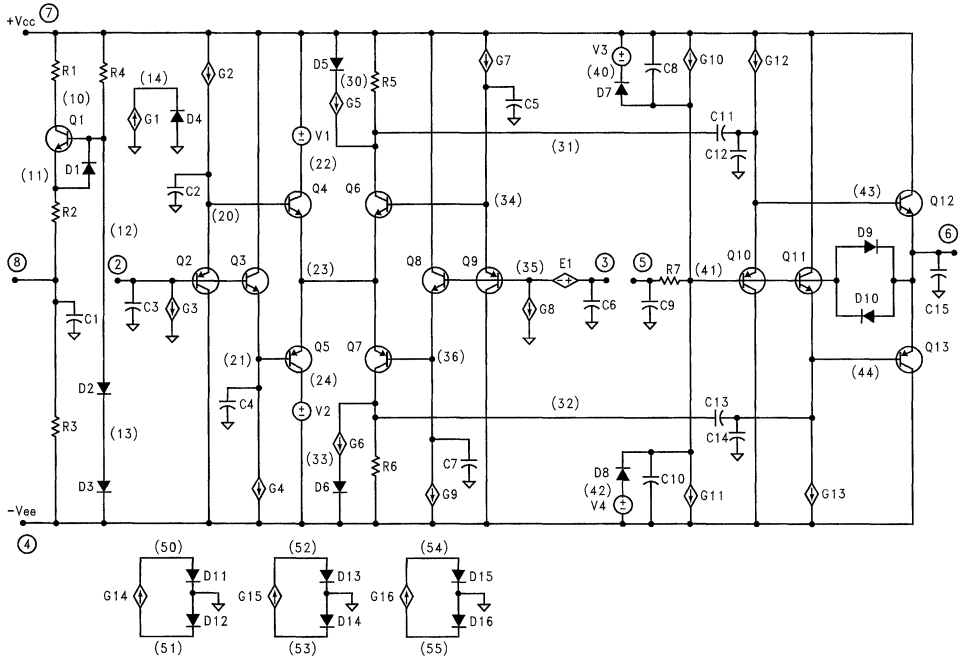

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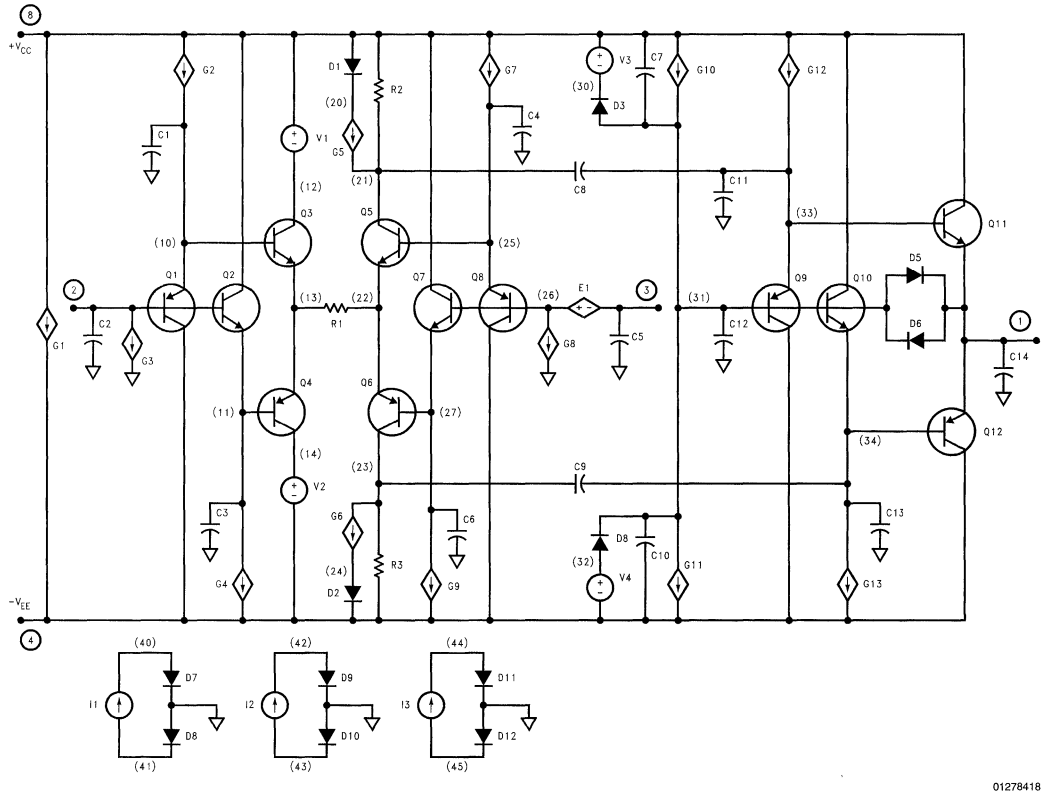

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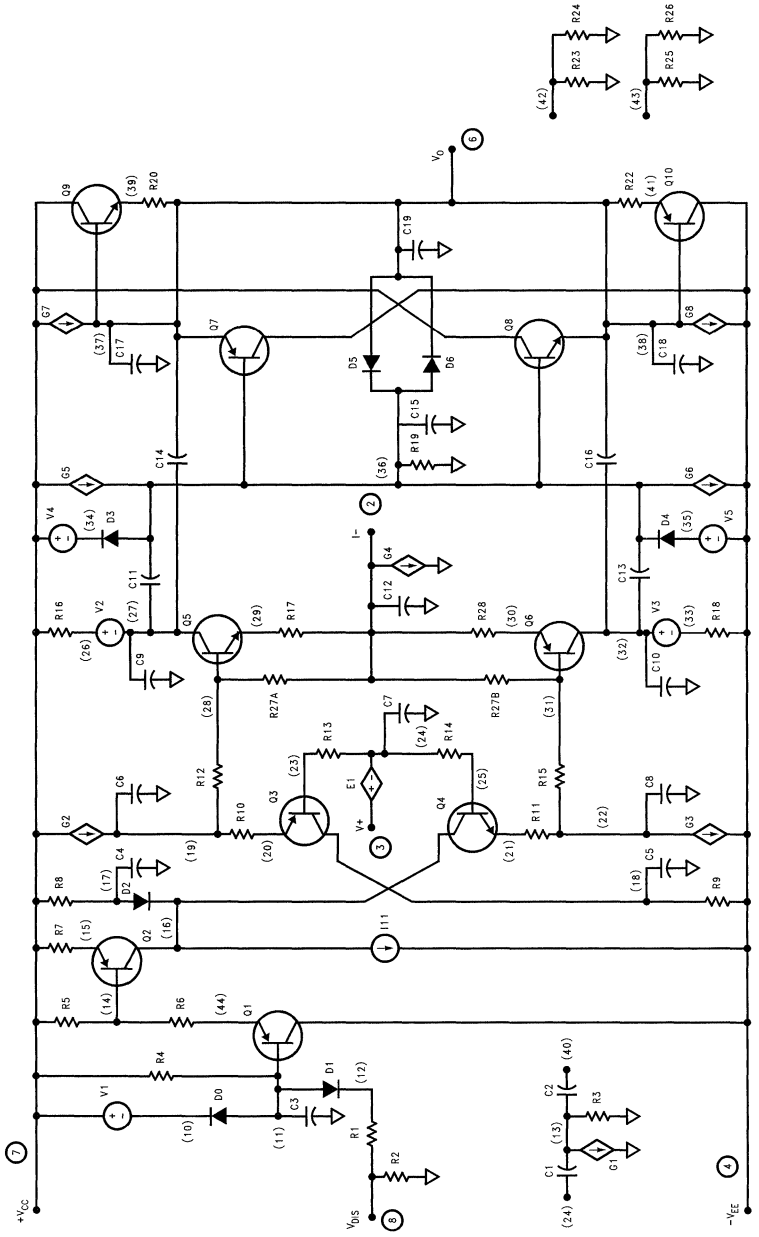
Note: Circled number denotes PIN number and number in parenthesis denotes NODE number

CLC430



Note: Circled number denotes PIN number and number in parenthesis denotes NODE number

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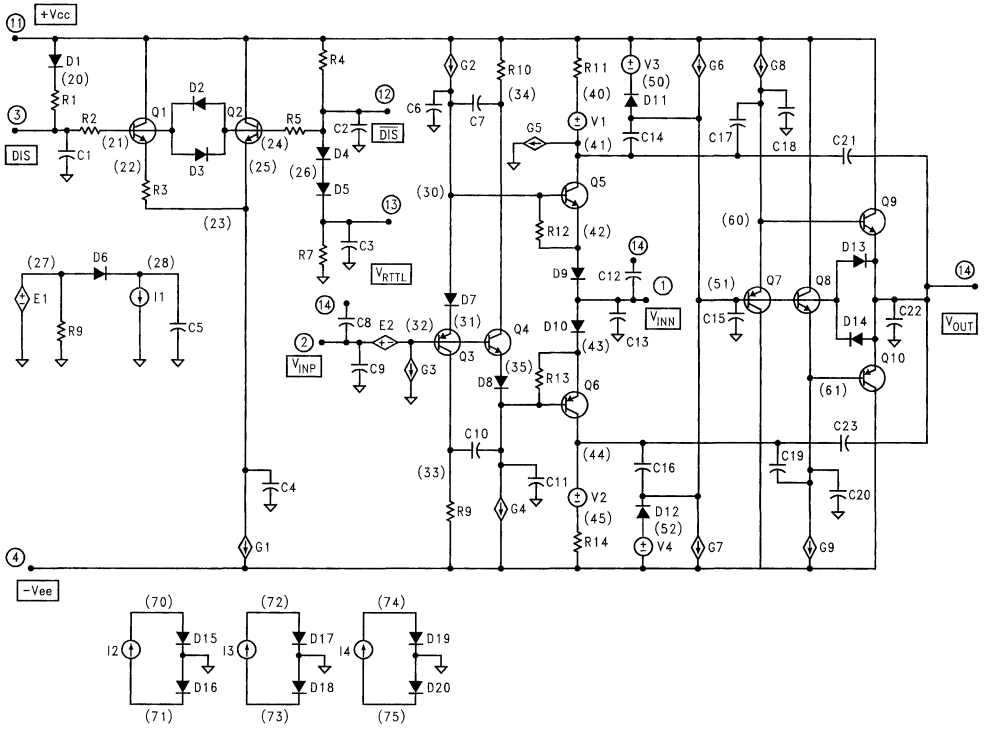

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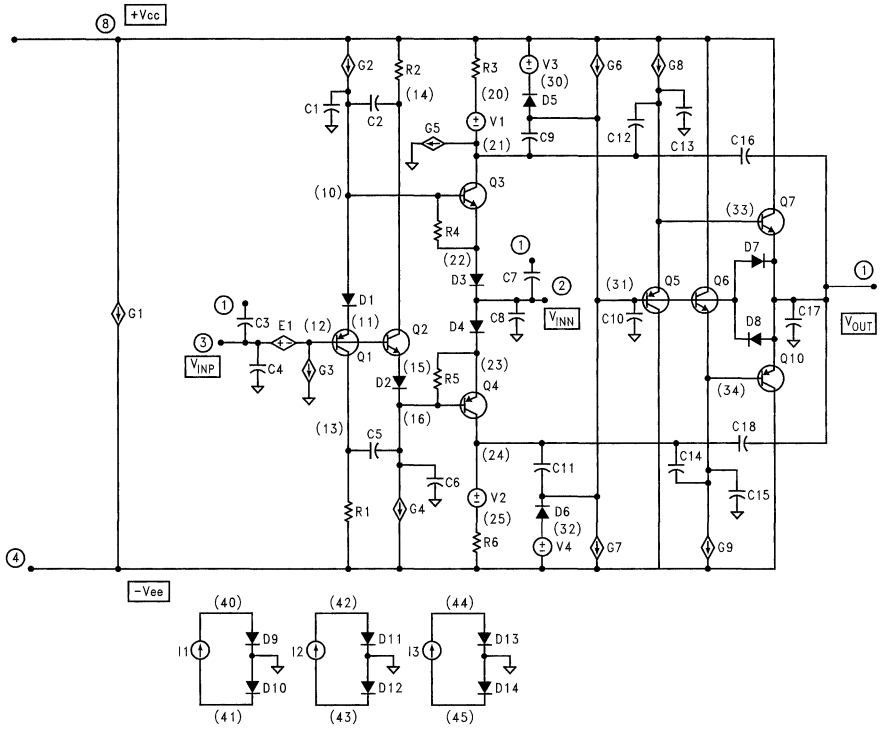
Note: Circled number denotes PIN number and number in parenthesis denotes NODE number

CLC432



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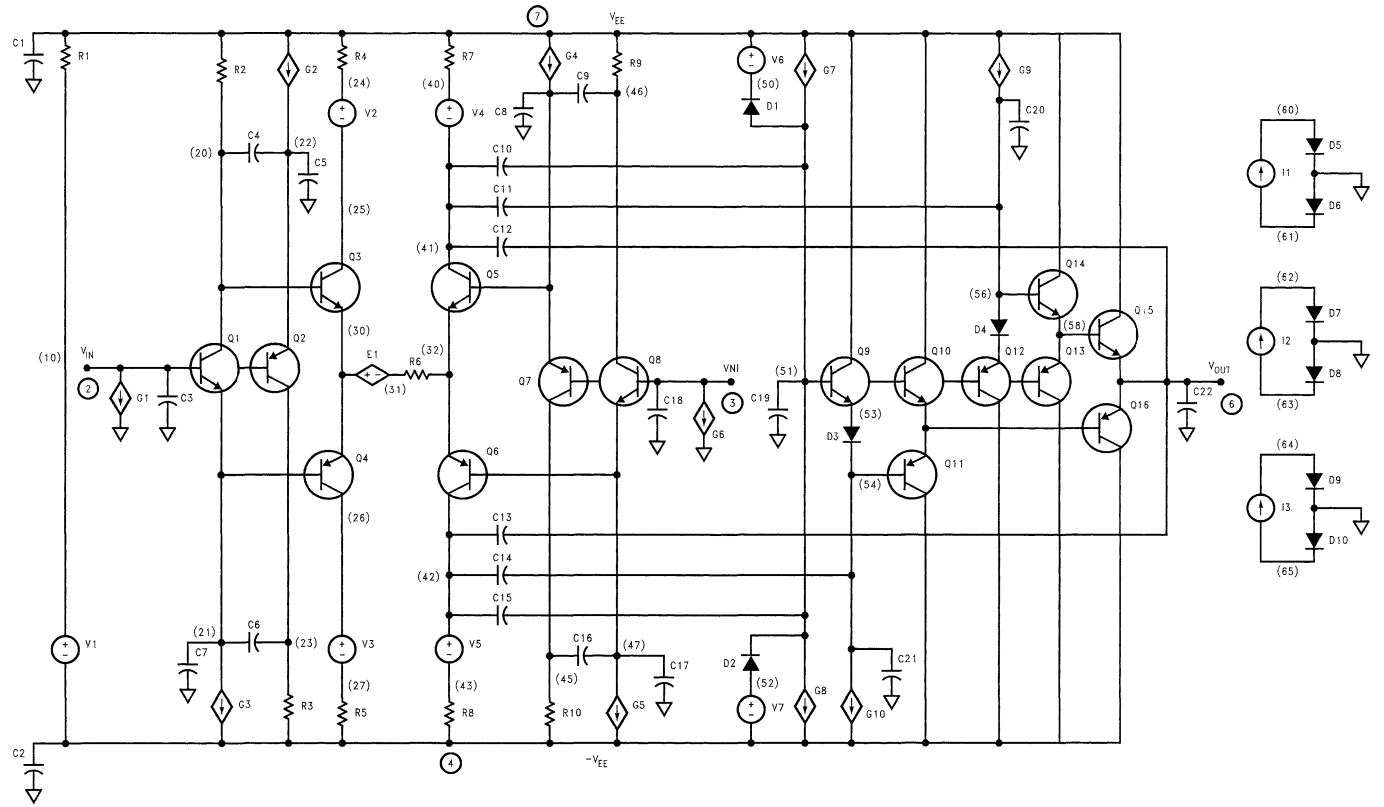
CLC440



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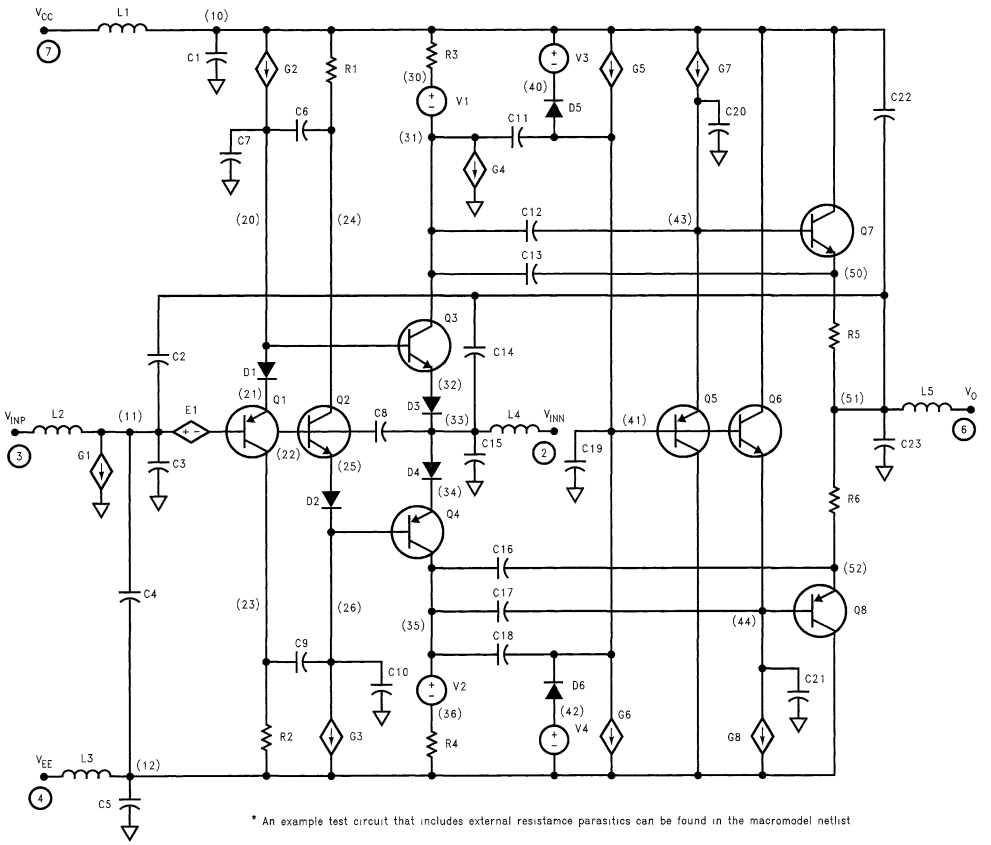
Note: Circled number denotes PIN number and number in parenthesis denotes NODE number

CLC449

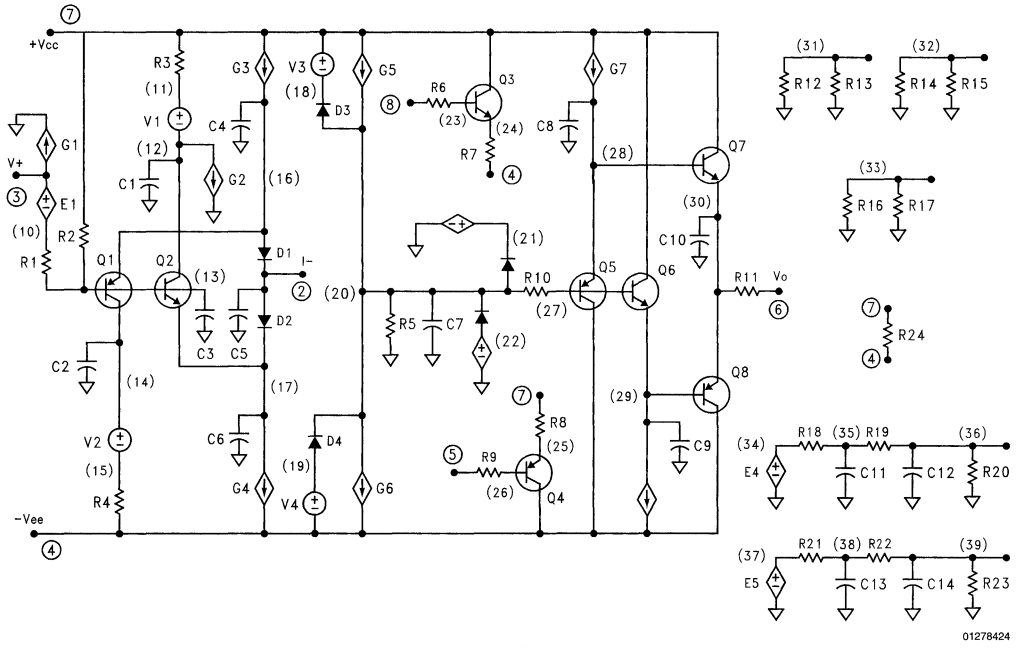


* An example test circuit that includes external resistance parasitics can be found in the macromodel netlist

01278423

Note: Circled number denotes PIN number and number in parenthesis denotes NODE number

CLC501



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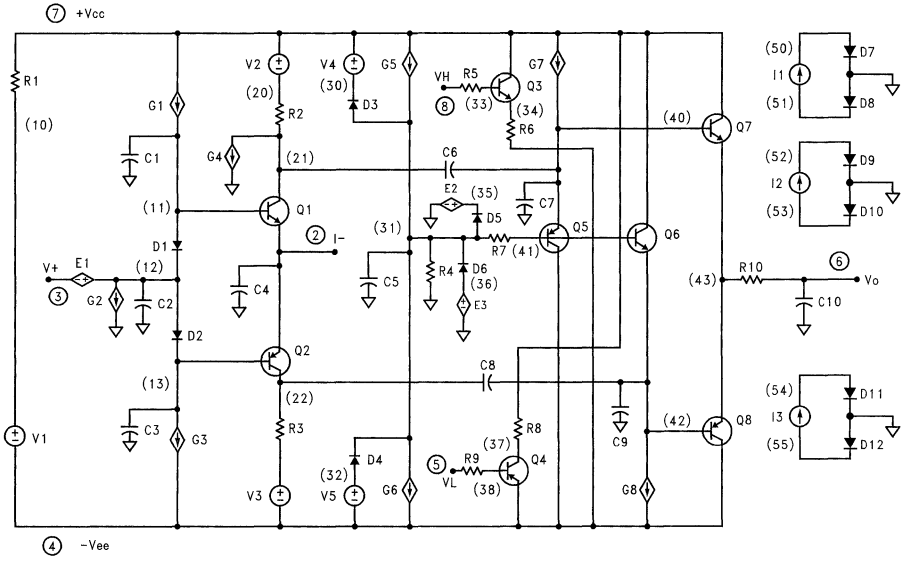

Note: Circled number denotes PIN number and number in parenthesis denotes NODE number

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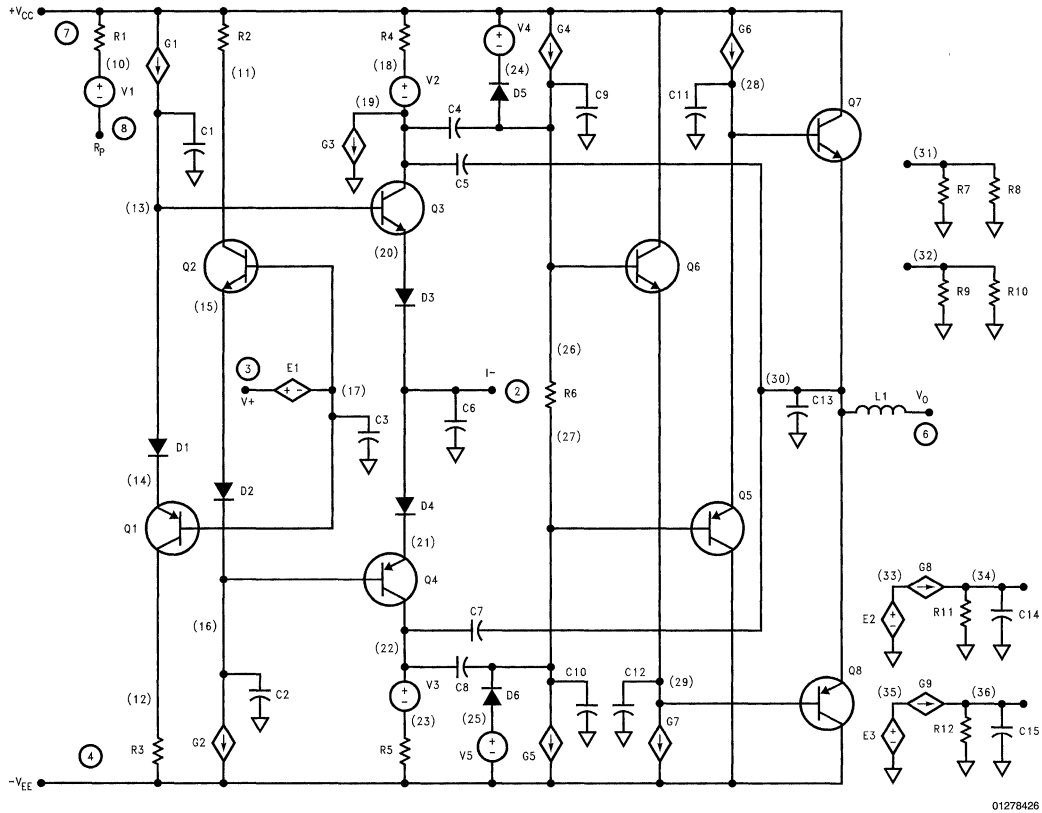

Note: Circled number denotes PIN number and number in parenthesis denotes NODE number

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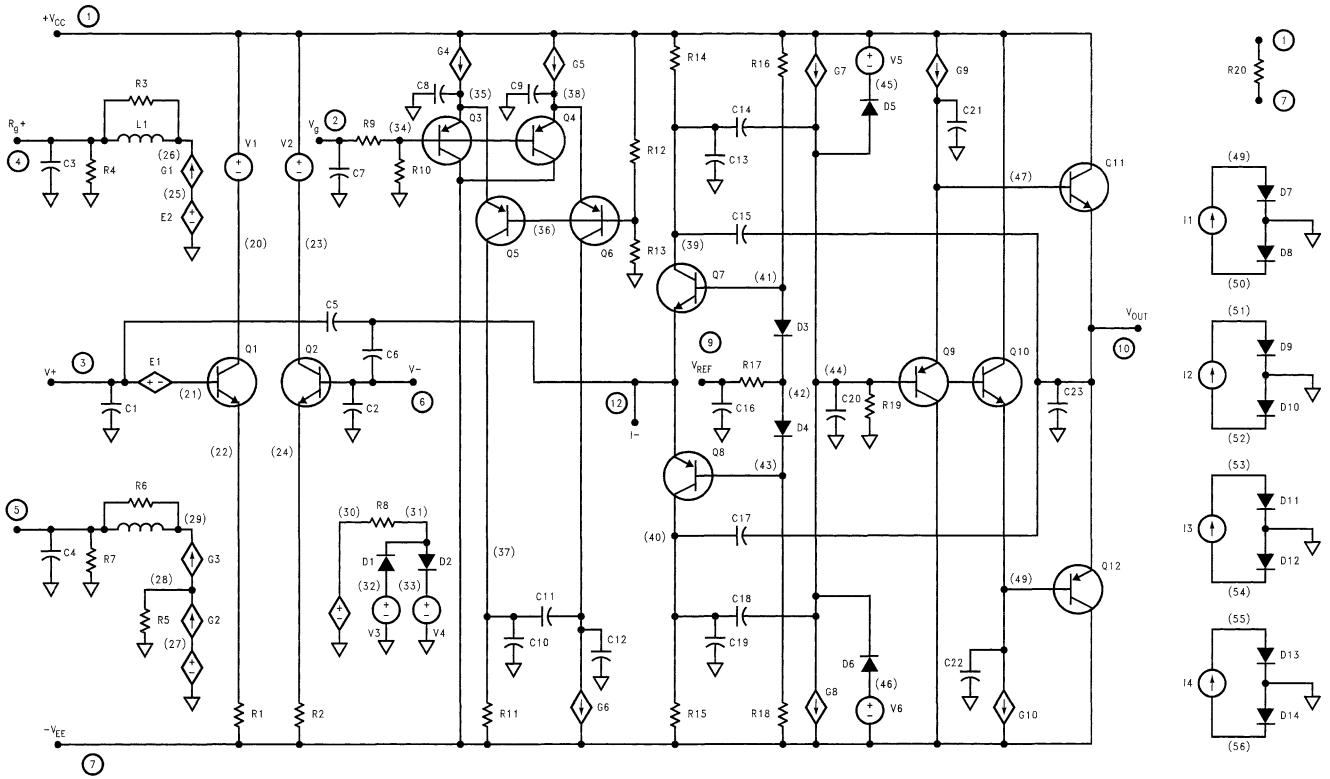

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Note: Circled number denotes PIN number and number in parenthesis denotes NODE number

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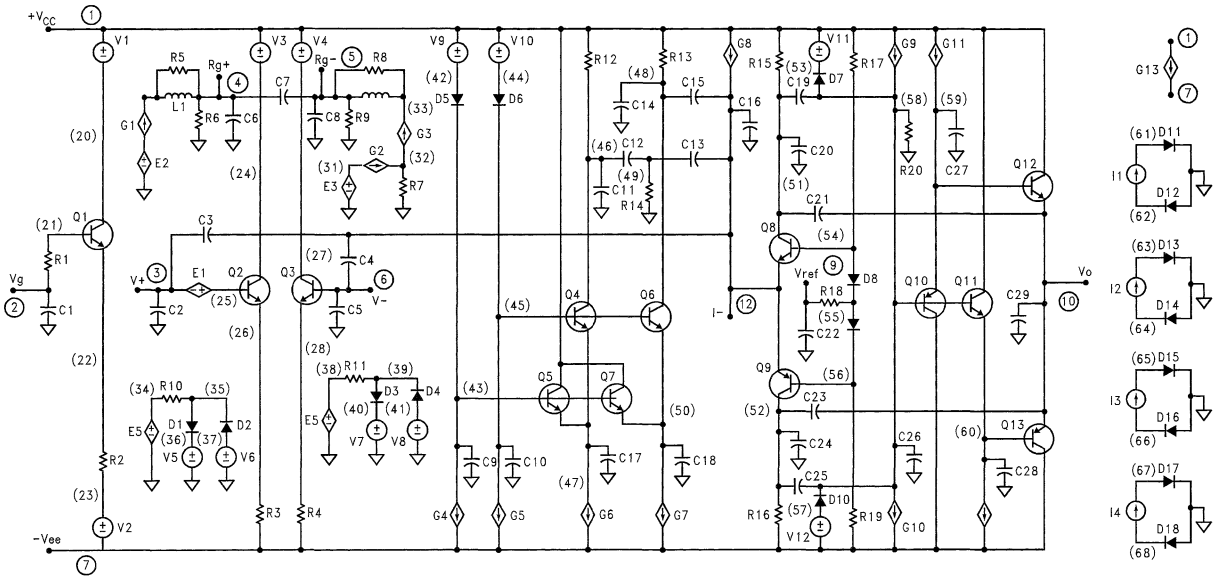

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Note: Circled number denotes PIN number and number in parenthesis denotes NODE number

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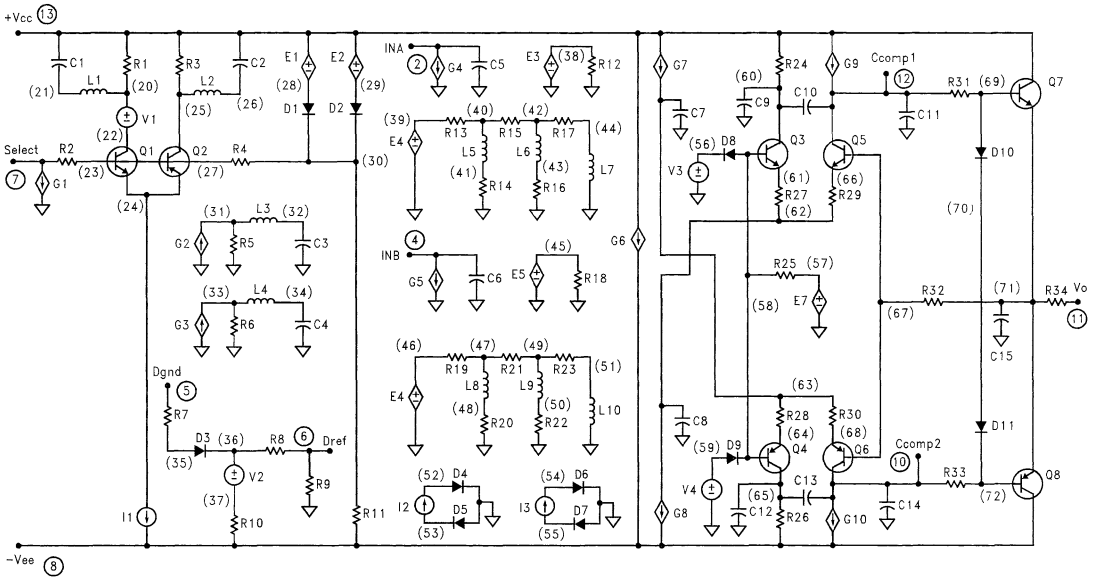

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Note: Circled number denotes PIN number and number in parenthesis denotes NODE number

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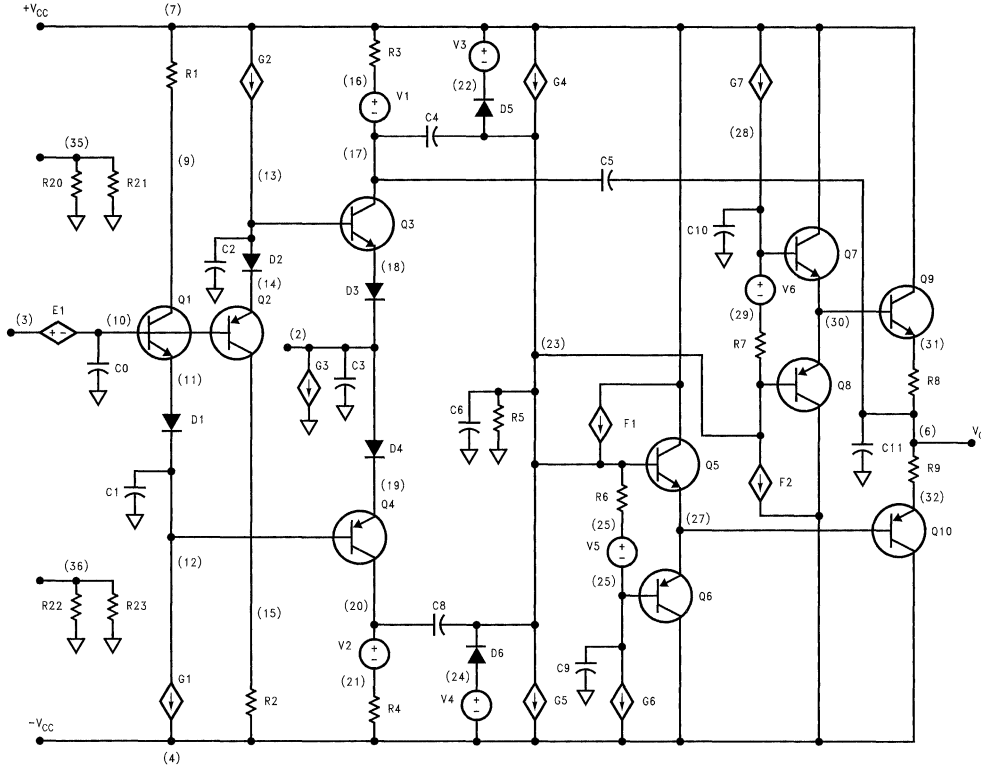
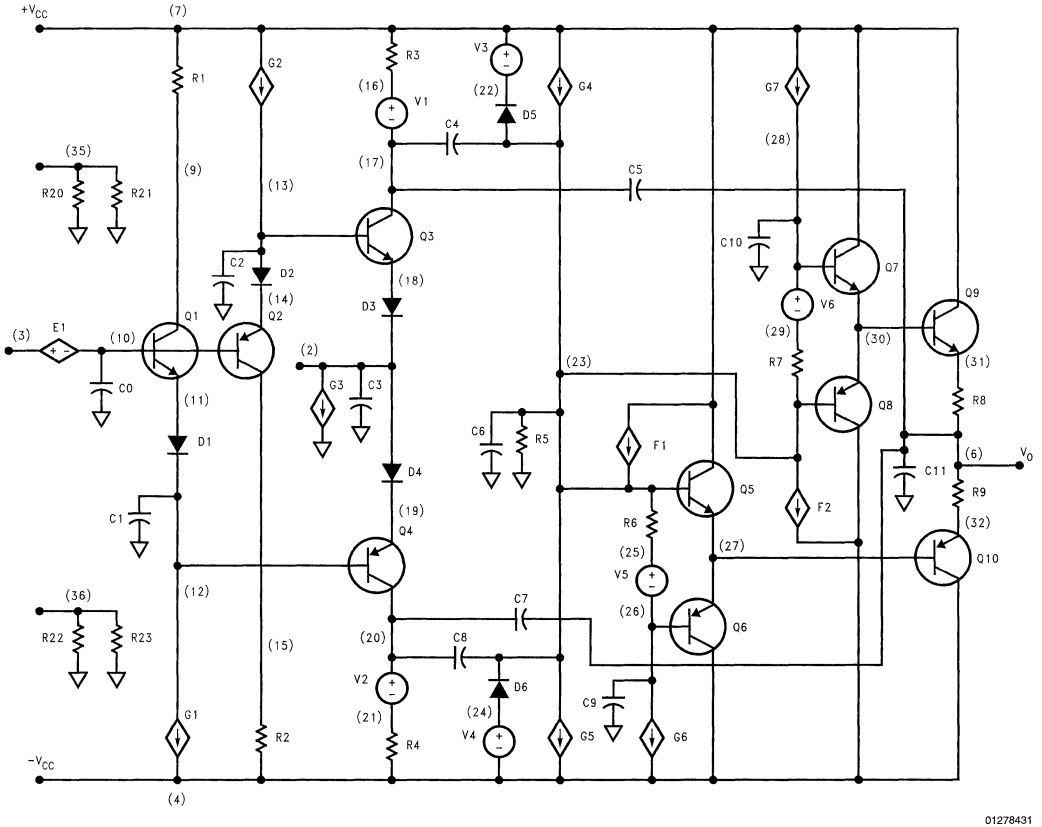


01278430

Note: Circled number denotes PIN number and number in parenthesis denotes NODE number

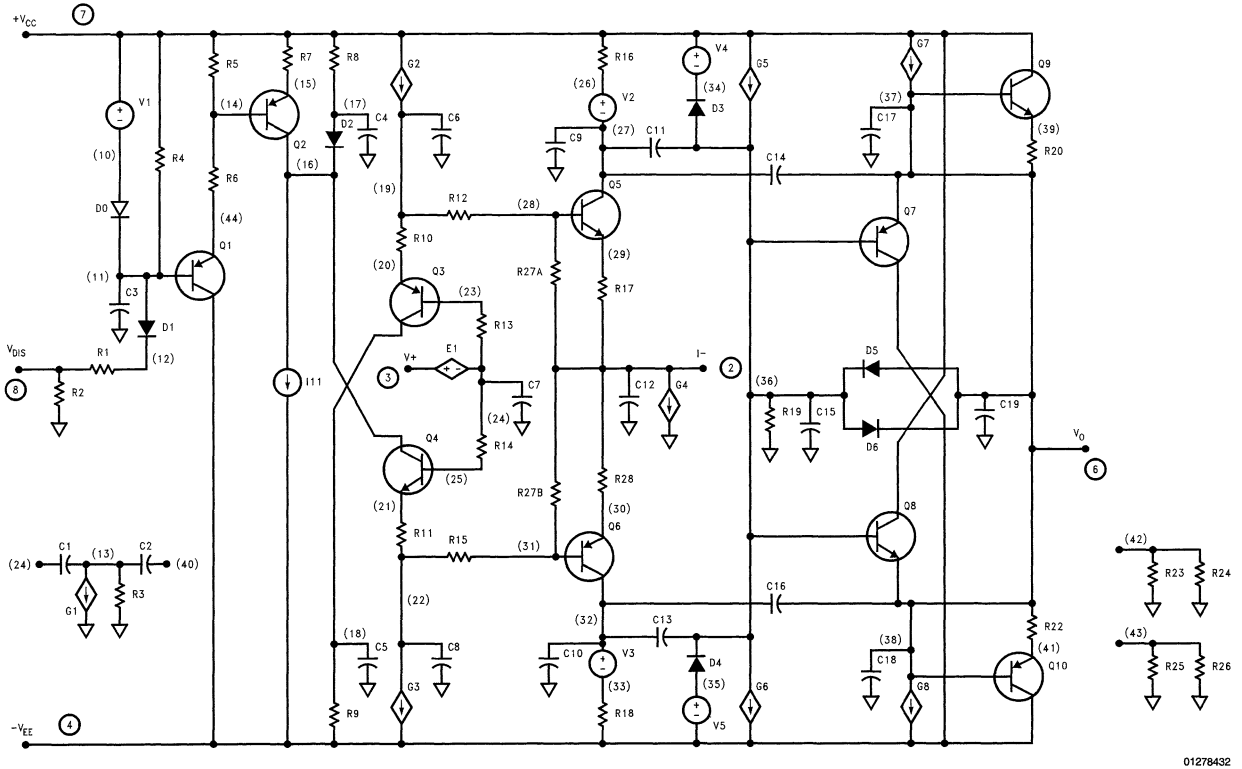
CLC5654



01278431

Note: Circled number denotes PIN number and number in parenthesis denotes NODE number

CLC5665



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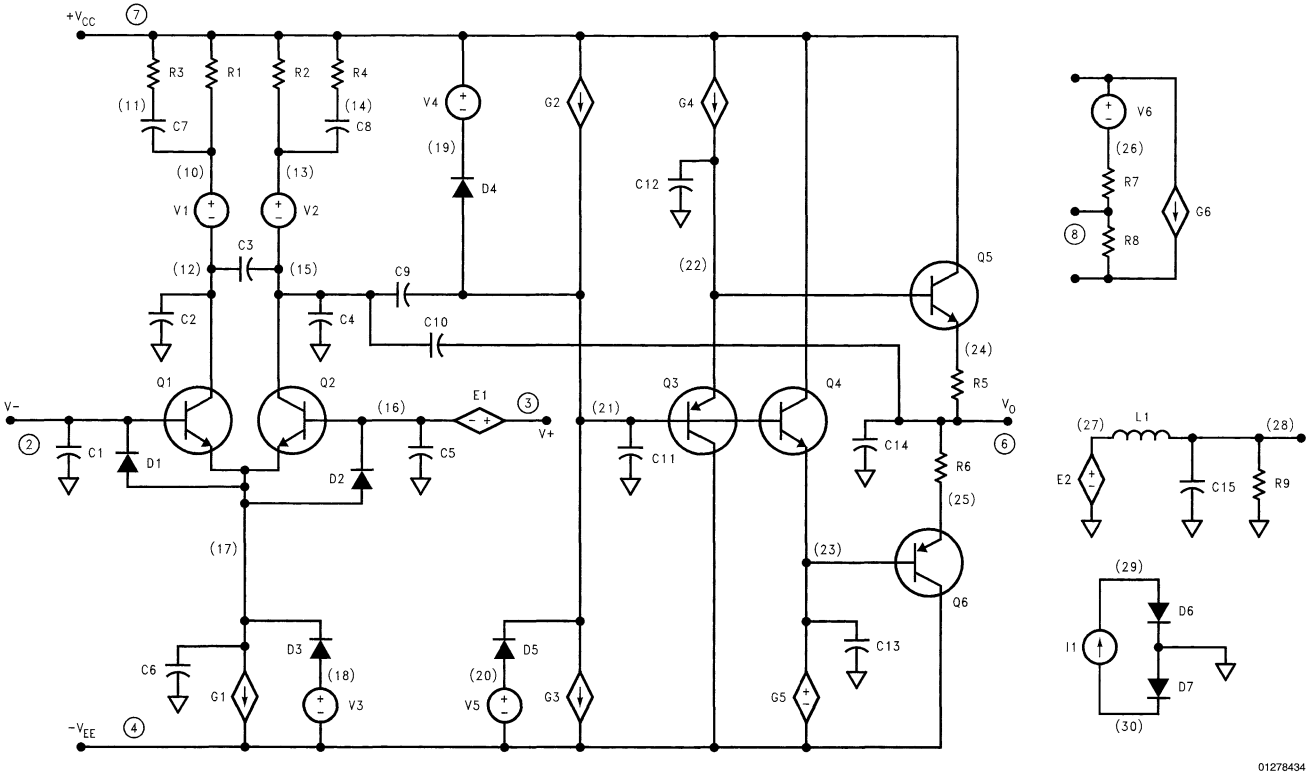
Note: Circled number denotes PIN number and number in parenthesis denotes NODE number



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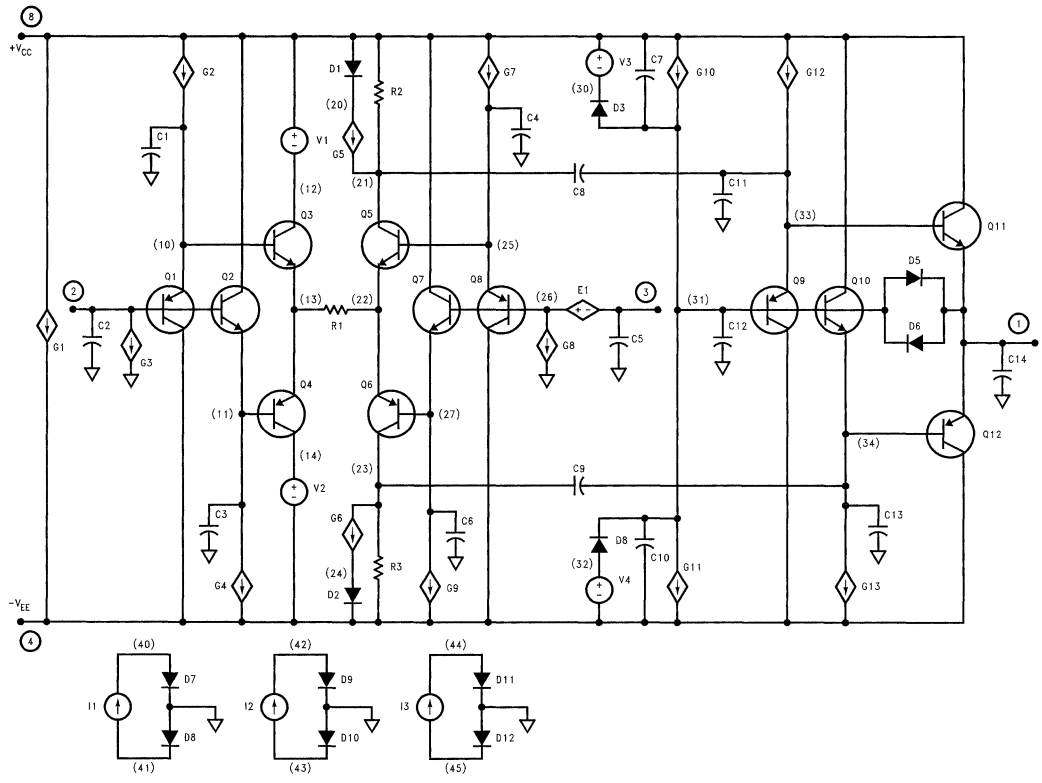
Note: Circled number denotes PIN number and number in parenthesis denotes NODE number



Note: Circled number denotes PIN number and number in parenthesis denotes NODE number.

The circuits included in this application note have been tested with National Semiconductor parts that may have been obsoleted and/or replaced with newer products. Please refer to the CLC to LMH conversion table to find the appropriate replacement part for the obsolete device.

References

1. National's 1993/1994 Databook and 1995 Databook Supplement of standard products.
2. MicroSim Corporation, 20 Fairbanks, Irvine, CA 92718 USA, (714) 770-3022, (800) 245-3022.

Wideband Op Amp Capable of µPower Operation

National Semiconductor
OA-19

The CLC505 is a current-feedback operational amplifier with an externally-adjustable supply current whose AC performance can be tuned to meet the precise requirements of many high-speed applications. The CLC505 provides a small-signal bandwidth of 150MHz (A_v = +6) while drawing 9mA supply current from ±5V power supplies. Reducing the supply current to 1mA decreases the bandwidth by only a third; 50MHz (A_v = +6). Please refer to the CLC505 data sheet for a full performance description over the 1mA to 9mA supply current range. The following application note is intended to supplement the CLC505 data sheet describing its operation with quiescent supply currents at or below 1mA.

Frequency Response Dependence on Supply Current

Application note OA-13 describes the internal topology of a current-feedback amplifier and the dependence of its loop gain (and hence bandwidth) on the inverting-input impedance. For an ideal current-feedback amplifier, this impedance is zero and the amplifier's frequency response is completely independent of the signal gain. As the supply current of the CLC505 is reduced below the 1mA region, the inverting-input impedance increases to such a degree that its effect on the loop-gain begins to dominate. To understand the impact of this impedance, as well as a similar increase in the output impedance (R_o) at low supply currents, the amplifier's internal block diagram, *Figure 1*, and resulting transfer function are shown. This analysis considers only the non-inverting op amp configuration but a similar result is obtained for the inverting configuration.

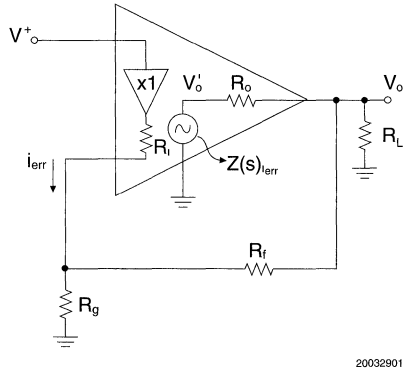


FIGURE 1. Low Current CLC505 Analysis Topology

An understanding of the transfer function given in Equation 1 is the central point of this discussion. The supply current's dependence enters into this equation through the three internal terms, R_i, R_o, and Z(s). R_i represents the output impedance of the unity-gain buffer found between the amplifier's inputs, while R_o represents the output impedance of the output voltage buffer. Z(s) is the frequency-dependent transimpedance gain which converts the error current (I_{err}), flowing through the inverting input, to a voltage which is buffered to the output.

Both the inverting input and the output pins are voltage-output structures consisting of symmetric (PNP and NPN)

$$\frac{V_o}{V^+} = \left(1+\frac{R_f}{R_g}\right)\left(\frac{1+\dfrac{R_o}{\left(1+\frac{R_f}{R_g}\right)z(s)}}{1+\dfrac{\left(R_f+R_i\left(1+\frac{R_f}{R_g}\right)\right)\left(1+\frac{R_o}{R_L}\right)+R_o\left(1+\frac{R_i}{R_g}\right)}{z(s)}}\right) \quad (1)$$

where

$1+\frac{R_f}{R_g}$ → desired noninverting signal gain

$\frac{R_o}{\left(1+\frac{R_f}{R_g}\right)z(s)}$ → will set a limit to the high frequency attenuation as the forward transimpedance gain, Z(s), become very small.

$$\frac{\left(R_f+R_i\left(1+\frac{R_f}{R_g}\right)\right)\left(1+\frac{R_o}{R_L}\right)+R_o\left(1+\frac{R_i}{R_g}\right)}{z(s)} = \frac{1}{\text{Loop Gain}}$$

emitter followers (ref. 1), very similar to a Class AB power buffer (ref. 2, p 293). Emitter-follower outputs show an output impedance that is directly proportional to the operating temperature (K) and inversely proportional to the transistor's quiescent current ($R_e = V_t/I_c$, $V_t = kT/q$, ref. 2, p 398). As the supply current decreases, the portion of the supply current allocated to these stages also decreases causing an increase in both the inverting input impedance, R_i, and the output impedance, R_o. Decreasing the supply current will also increase the DC open-loop gain, Z_{OL}, while decreasing the dominant pole frequency, W_o. However, the product of Z_{OL}*W_o remains relatively constant over supply current and temperature.

From the transfer function shown in Equation 1

Rewriting Equation 1 in these terms

Manipulating this into standard form

Frequency Response Dependence on Supply Current (Continued)

Let $1+\frac{R_f}{R_g} = A_V^+$ desired signal gain

$$z(s) = \frac{z_{OL}\omega_o}{s+\omega_o} \text{ single pole, forward transimpedance gain}$$

$$z_t = \left(R_f + R_i\left(1+\frac{R_f}{R_g}\right)\right)\left(1+\frac{R_o}{R_L}\right) + R_o\left(1+\frac{R_i}{R_g}\right)$$

feedback transimpedance, this is the inverting error current, i_{err} resulting from V_o

$$\text{Loop gain} \equiv \frac{z(s)}{z_t} \qquad (2)$$

$$\frac{V_o}{V^+} = A_V^+\left(\frac{1+\frac{R_o\left(s+\omega_o\right)}{A_V^+\left(z_{OL}\omega_o\right)}}{1+\frac{z_t\left(s+\omega_o\right)}{z_{OL}\omega_o}}\right)$$

$$\frac{V_o}{V^+} = \frac{R_o}{z_t}\left(\frac{s+\omega_o\left(\frac{A_V^+ z_{OL}}{R_o}+1\right)}{s+\omega_o\left(\frac{z_{OL}}{z_t}+1\right)}\right) \quad \text{Let} \quad \frac{A_V^+ z_{OL}}{R_o} >> 1, \quad \frac{z_{OL}}{z_t} >> 1$$

then

$$\frac{V_o}{V^+} = \frac{R_o}{z_t}\left(\frac{s+\left(\frac{A_V^+}{R_o}\right)z_{OL}\omega_o}{s+\frac{z_{OL}\omega_o}{z_t}}\right)$$

as $s \rightarrow 0$, DC gain, $\frac{V_o}{V^+} = A_V^+$

as $s \rightarrow \infty$, high frequency gain, $\frac{V_o}{V^+} = \frac{R_o}{z_t} \equiv A_{min}$

(3)

Note that the zero frequency shown in Equation 3 is at a significantly higher frequency than the pole frequency. Once the operating frequency approaches this zero frequency, Equation 3 predicts a minimum gain, A_{min}. This is generally not observed in practice, since the zero frequency of Equation 3 is typically much higher than the frequencies at which R_i and R_o start to show a normal emitter-follower inductive characteristic. To simplify this analysis, the inductive characteristics of R_i and R_o have been neglected. It should be noted that the inductive characteristics will continue to roll off the closed-loop response with attenuations much greater than that predicted by A_{min} at high frequencies. The zero shown in the transfer function of Equation 3 will be neglected with the rest of this discussion focused on the closed-loop pole frequency.

Looking at equation 3 again, the closed-loop response pole will be set by $(Z_{OL}{}^*W_o)/Zt$. As the supply current is changed, the $Z_{OL}{}^*W_o$ product remains relatively constant. *Figure 2* shows the typical open-loop forward transimpedance gain, (20*log(|Z(s)|)), plotted over frequency as the supply current is varied. *Figure 3* shows this same forward open-loop gain at 1mA supply current plotted over the full military temperature range. As long as these forward gain responses fall on the same line in the 20dB/decade roll-off region, the $Z_{OL}{}^*W_o$ product remains constant.

With a constant $Z_{OL}{}^*W_o$ term, the only element setting the bandwidth in the transfer function of equation 3 is the Z_t expression, equation 2. In general, it is advantageous to make Z_t as small as possible which will increase the loop gain and as a result improve harmonic distortion and extend the bandwidth. The limit to the reduction of Z_t comes when higher order poles of Z(s) degrade the phase margin at the unity-gain crossover of the loop gain. For a given supply current and desired gain, decreasing R_f and increasing R_L will decrease Z_t. An important limitation on decreasing R_f is the available output current drive. For the non-inverting configuration, R_f+R_g appears as an additional load in parallel with R_L, while for the inverting configuration, only R_f appears as an additional load in parallel with R_L.

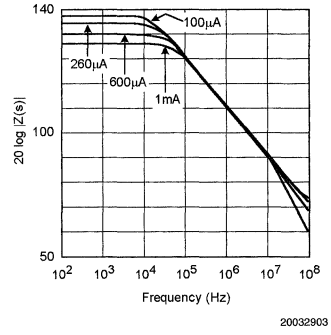


FIGURE 2. 20log|Z(s)| at Deferent Supply Currents

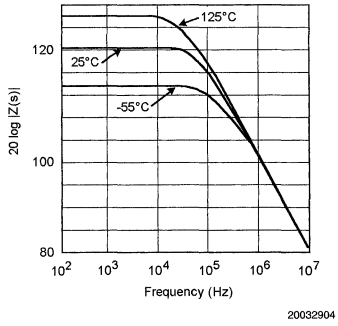


FIGURE 3. 20log|Z(s)| at 1mA = I_{CC} Over Temperature

Letting $1+\frac{R_f}{R_g} = A_V^+$, and $R_g = \frac{R_f}{A_V^+ - 1}$

Z_t can be rewritten as

$$z_t = A_V^+ R_i\left(1+\frac{R_o}{R_L \| R_f}\right) + R_f + R_o\left(1+\frac{R_f}{R_L}-\frac{R_i}{R_f}\right) \qquad (4)$$

Equation 4 emphasizes the gain dependence of Z_t. At low supply currents, R_i becomes so large (500Ω at 1mA) as to cause the first term of Equation 4 to dominate. This part of the feedback transimpedance expression is directly related to the desired signal gain, A^+_v. As the gain is increased, Z_t increases, decreasing the bandwidth. This bandwidth de-

Frequency Response Dependence on Supply Current (Continued)

pendence on gain is analogous to that observed with voltage-feedback amplifiers. As such, for configurations which set the first term of equation 4 to be the dominant contributor to Z_t, a gain-bandwidth (GBW) product characteristic will be observed. *Figure 4* shows a test circuit used to measure the GBW as the supply current is decreased from 1mA to 100mA over gains of +5, +10, and +20. At very low supply currents, slight DC-output currents due to offsets can change the AC performance. For this reason, the output DC-blocking capacitor was used to limit output DC currents.

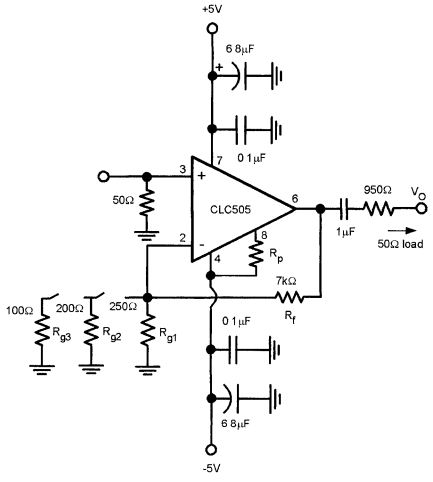


FIGURE 4. Test Circuit for Gain Bandwidth Product Measurement

For the 1mA case, Equations 2 and 3 were used to predict the small-signal −3dB bandwidth at the three gains of +5,+10, &+20. With R_p = 300kΩ, $I_{cc} \approx$ 1mA, $R_i \approx$500Ω, $R_o \approx$ 50Ω and approximate Z_{OL}*W_o product = 2π120E9. Compute Z_t from Equation 2 and expected −3dB bandwidth from Equation 3.

The computed and measured results are shown in Table 1. *Figure 5* shows the small-signal frequency responses for each of these gains normalized to enter the graph at the same point on the y-axis.

TABLE 1.

Gain	Computed Z_t	Expected −3dB BW	Measured −3dB BW	Measured GBW
A_V^+ = 5	3.78kΩ	32MHz	57MHz	285MHz
A_V^+ = 10	650kΩ	18.5MHz	26MHz	260MHz
A_V^+ = 20	11.9kΩ	10MHz	11.5MHz	230MHz

The test results are in good agreement with the simplified analysis of *Figure 5* at the highest gain tested, A_v = +20. At lower gains, several effects combine to extend the bandwidth beyond that predicted by this simplified analysis. Specifically, all of the additional higher frequency poles of the open loop response can come into play at lower gains. These include both the inductive characteristics of the two output impedances and higher order poles for Z(s). This has the effect of decreasing the phase margin from the theoretical 90° assumed by the single pole analysis Phase margins less than 90° but greater than 60° will extend the closed-loop bandwidth without peaking.

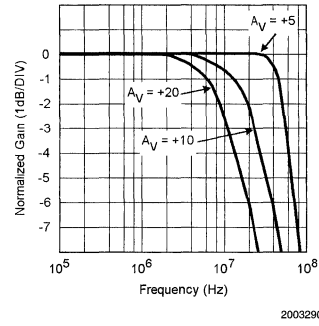


FIGURE 5. Small Signal Frequency Response vs. Gain (I_{cc} = 1mA)

An additional effect serves to increase the measured bandwidth as the desired signal level is increased. As the frequency of operation increases (or as fast rise time signals are applied), an increase in the steady-state inverting-stage current is observed due to the increased I_{err} required when operating at these higher frequencies with reduced loop gain. This increasing error current, as the input is swept over higher frequencies, decreases the inverting input impedance. This frequency and signal level dependence of R_i will decrease the value for Z_t, increasing the loop gain and extending the bandwidth. This effect is particularly pronounced when the R_i*A_v term becomes a large part of the total Z_t expression, at relatively high non-inverting or inverting gains. Under these conditions, the bandwidth actually increases as the signal level is increased. *Figure 6* shows this effect for the A_v = +20 case of *Figure 4* with I_{cc} = 1mA.

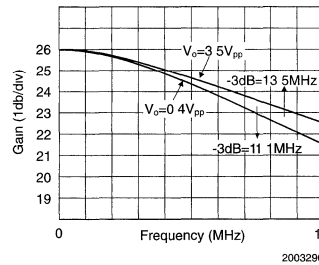


FIGURE 6. Frequency Response vs. Signal Level

For a given desired supply current, load impedance and signal gain, a close inspection of the feedback transimpedance expression of Equation 4 shows that an optimum R_f can be found that will minimize Z_t, maximizing the bandwidth and loop gain. This is a relatively shallow minimum with the

Frequency Response Dependence on Supply Current (Continued)

resulting –3dB bandwidth not significantly different than for a fixed 1kΩ = R_f. Nevertheless, solving for this optimum R_f yields the following.

Table 2 on page 6 shows the required information to predict a gain-bandwidth product vs. supply current. At each supply current, the internal parameters (R_i, R_o, and Z_{OL}*W_o) are shown. From this, an optimum R_f can be calculated using Equation 5. The measured small-signal bandwidth and GBW are then recorded. The measured –3dB bandwidths shown in table 2 agree very closely with those predicted from Z_{OL}*W_o/Z_t (evaluating this expression from the data given in this table and Equation 2 for Z_t).

$$\text{Optimum } R_f = \sqrt{\frac{R_i R_o (A_V^+ - 1)}{1 + \frac{R_o}{R_L}}} \qquad (5)$$

This estimate of GBW vs. supply current represents a very conservative estimate. As the signal gain is decreased from A_v = +20V/V, the GBW will increase as shown in Table 1. In addition, the measured bandwidth would increase as signal level is increased, as discussed earlier, up to the point that output-stage drive current and slew limits come into consideration. The supply current and resulting GBW of Table 2 are plotted in *Figure 7*. This GBW should be taken as a minimum achievable value and a good starting point for estimating the bandwidth capability of the CLC505 at very low supply currents. A PSPICE simulation macromodel available from National can be used to test the performance under different operating conditions. This macromodel reasonably simulates most of the effects discussed earlier. Transient simulation will even show the improved rise times at higher gains as the signal swing is increased.

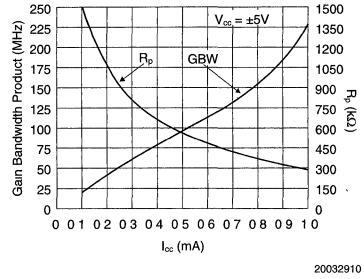


FIGURE 7. Gain Bandwidth Product and Current Set Resistor vs. I_{CC}

A common way to illustrate the wideband capability of low-power amplifiers is through a MHz-per-mA figure of merit. *Figure 8* shows the same data as *Figure 7* with boundary regions for decades of MHz/mA shown. Two low-power Maxim op amps are also shown that claim superior MHz/ mA performance. Although certainly capable parts, the Maxim amplifiers are about a decade lower in performance than the CLC505. The CLC505, along with several other National wideband current-feedback amplifiers (such as the CLC406), push strongly above the 100MHz/mA barrier. The discussion thus far has assumed ±5 volt supplies. As will be discussed later, single supply operation is also possible.

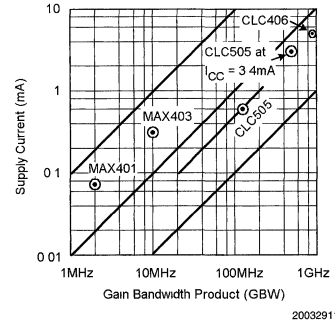


FIGURE 8. GBW vs. Supply Current

TABLE 2. Performance vs. Supply Current (V_{cc} = ±5V, T_A = 25°C, R_L = 1kΩ)

R_p	I_{cc}	R_i	R_o	Z_{OL}	W_o	$Z_{OL}W_o$	A_v = +20 Optimum R_f	A_v = +20 –3d BW	GBW
300kΩ	1mA	500Ω	47Ω	1.93MΩ	2π62kHz	2π120E9	653Ω	11.4MHz	228MHz
400kΩ	800µA	620Ω	64Ω	2.46MΩ	2π49kHz	2π121E9	842Ω	7.9MHz	158MHz
500kΩ	600µA	920Ω	81Ω	2.92MΩ	2π42kHz	2π123E9	1.14kΩ	60MHz	120MHz
600kΩ	480µA	1.16kΩ	100Ω	3.35vMHz	2π38kHz	2π127E9	1.42kΩ	4.6MHz	92MHz
900kΩ	260µA	1.97kΩ	139Ω	1.76MΩ	2π26kHz	2π123E9	2.14kΩ	2.7MHz	54MHz
1MΩ	260µA	2.27kΩ	185Ω	5.13MΩ	2π25kHz	2π128E9	260kΩ	2.6MHz	46MHz
1.3MΩ	160µA	3.27kΩ	258Ω	6.80MΩ	2π20kHz	2π136E9	3.57kΩ	1.6MHz	32MHz
1.6mΩ	100µA	4.30kΩ	333Ω	7.50KΩ	2π17.5kHz	2π131E9	4.52kΩ	1.1MHz	22MHz

Secondary Effects of Low Supply Current Operation

Besides having a profound effect on the small signal AC performance, low supply current operation of the CLC505 will also modify most other performance characteristics. The most drastic effect is on the available output current. At 1mA supply current, the CLC505 data sheet guarantees ±5mA at 25°C. This specification should be scaled down proportionately for operation below 1mA. The non-inverting slew rate is retained with very low power levels due to a slew enhancement circuitry in the input buffer stage (e.g. at 1mA supply current, SR = 500V/µs for the particularly demanding condition of A_v = +2) Both of the input bias currents will decrease with supply current but the input offset voltage and temperature drift will become more pronounced. Recall that, for a current-feedback topology, the two input bias current terms are unrelated in both magnitude and polarity. Bias current cancellation to an offset-current specification is therefore ineffective. Please refer to the CLC505 data sheet for more information on these DC error terms at 1mA.

The most subtle effect is perhaps found with the noise performance. As I_{cc} is reduced, all of the amplifier's input referred noise terms show an increase in their 1/f noise corner frequencies. Also, an additional gain term for the inverting noise current becomes appreciable. Specifically, the inverting input impedance acts as an additional impedance gain for the inverting bias current noise. The noise model discussed in application note OA-12 (Noise Analysis for National's Current-Feedback Amplifier's) does not consider this effect and would therefore understate the total output noise. The simulation macromodel will, however, show the correct output noise including this effect.

Taking Advantage of Voltage Feedback Characteristics

Most of the design techniques developed for voltage-feedback amplifiers are applicable to the CLC505 operating at or below 1mA supply current. One of the standard applications for a voltage-feedback amplifier, that is not directly possible with a current-feedback part, is a simple integrator with direct capacitive feedback. Changing the feedback resistor to a capacitor and moving to the inverting integrator configuration will result in the following circuit, *Figure 9*, and transfer function.

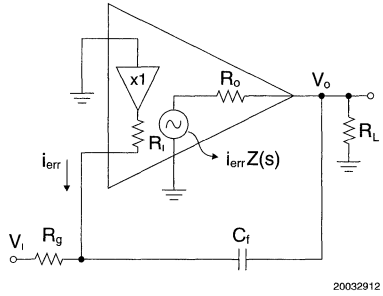


FIGURE 9. Analysis Circuit for Inverting Integrator

Neglecting the high frequency zero due to R_o. Should set feedback transimpedance zero < higher order poles of Z(s).

Also, high frequency feedback impedance should be > 1kΩ *Figure 10* shows a test circuit to demonstrate this integrator operation, while *Figure 11* shows the resulting integration of a square wave (100kHz) input to an output triangle wave.

Again the simulation macromodel for the CLC505 is very effective for analyzing the performance of these types of circuits.

$$\frac{V_o}{V_i} = \frac{-1}{sR_gC_f} \left(\frac{1}{1+\frac{1}{z(s)}\left(R_i\left(\frac{R_o}{R_L \| R_g}+1\right)+R_o\right)\left(\frac{s+\frac{1}{C_f\left(R_i \| R_g + R_o \| R_L\right)}}{s}\right)} \right)$$

$$\frac{1}{C_f\left(R_i \| R_g + R_o \| R_L\right)} < 2\pi(10 \rightarrow 20\text{MHz}) \text{ for } I_{cc} \leq 1\text{mA}$$

$$R_i\left(\frac{R_o}{R_L \| R_g}+1\right)+R_o > 1\text{k}\Omega$$

Figure 12 shows the simulated gain and phase for the integrator shown in *Figure 10*. Note that the DC gain of 66dB is comparable to other high-speed voltage-feedback amplifiers (such as the CLC420) while the supply current for this integrator is a very low 500µA.

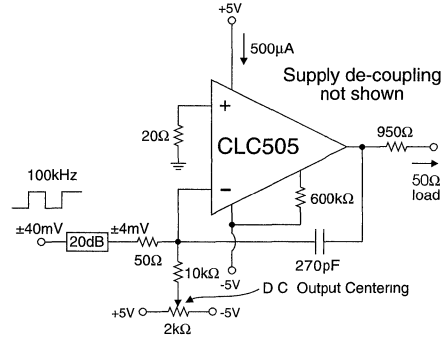


FIGURE 10. Low Power Integrator Test Circuit

Taking Advantage of Voltage Feedback Characteristics (Continued)

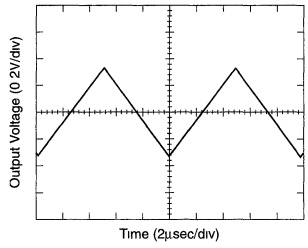


FIGURE 11. Integrator Output to Square Wave Input

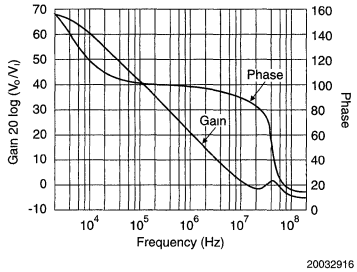


FIGURE 12. Integrator Frequency Response

To implement the Sallen-Key type of active filters, it is generally desirable to have an amplifier bandwidth at least twenty times the desired cutoff frequency. It is also desirable to operate the amplifier at relatively low gains. *Figure 13* shows a test circuit used to demonstrate the CLC505's capability of implementing very low-power single-supply high-frequency active filters

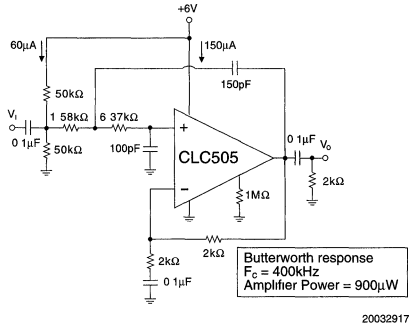


FIGURE 13. Single Supply µPower Active Filter

For low-power single-supply operation, all of the signal nodes need to be AC coupled. The three 0.1µF capacitors provide this function. This allows the non-inverting input pin to be biased at a midpoint between the supply pins, +3V in this case. The capacitors also prevent any DC currents from flowing in the output pin and reduce the DC amplifier gain to 1, which will hold the output pin DC operating point equal to the non-inverting input (centered between the supply pins.)

At least 6 volts across the part's supply pins is required to give some signal swing capability at the input stage from common-mode input range considerations. The amplifier's AC gain has been set for +2 and the filter components have been adjusted to allow for the amplifier's bandwidth (ref. 3).

Figure 14 shows the frequency response for just the amplifier. At this very low power and gain some peaking due to a loss of phase margin is observed. This will not effect the filter performance however. The 9MHz bandwidth is more than adequate to implement the desired 400kHz Butterworth low-pass filter. *Figure 15* shows the measured filter frequency response. The desired cutoff was achieved precisely. The loss in rolloff at higher frequencies arises from a direct signal coupling to the output through the filter components after the amplifier has stopped controlling the output voltage.

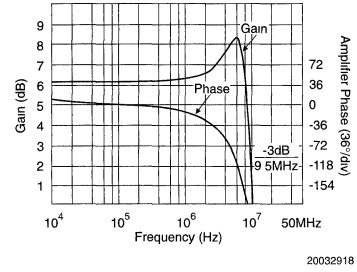


FIGURE 14. Very Low Power, Single Supply, Amplifier Frequency Response

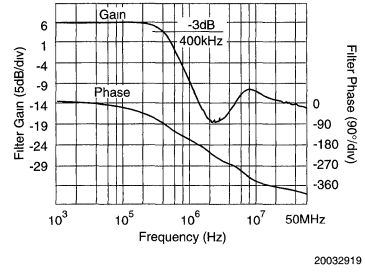


FIGURE 15. Very Low Power, Single Supply, Active Filter Frequency Response

Conclusions and Caveats

The CLC505 adjustable supply current op amp offers one of the highest MHz-per-mA performance levels available in a monolithic amplifier. A simplified analysis can do a good job of predicting the gain-bandwidth product under a variety of supply current, gain, feedback resistor, and loading conditions. A PSPICE simulation model available from National does an even better job of predicting performance over a wide variety of conditions. Although the internal topology of the CLC505 uses a current-feedback approach, at very low

Conclusions and Caveats (Continued)

supply currents this part may be treated more like a voltage-feedback amplifier having a gain-bandwidth product. Very high-speed integrators and active filters may be implemented at exceptionally low supply currents.

Due to leakage effects, the part-to-part tolerance on supply current for a fixed R_p becomes greater as the desired nominal supply current is decreased. At R_p = 300kΩ, National guarantees a maximum 1.3mA supply current at 25˚C from a nominal 1mA value. If a closer tolerance at this, or lower, supply currents is required, please contact National for further information.

References:

1. "Current Feedback Amplifiers", National Application Note OA-31.
2. "Analysis and Design of Analog Integrated Circuits", Gray & Meyer, Wiley 1977.
3. "Simplified Component Value Pre-Distortion for High Speed Active Filters", National Application Note OA-21.

Note: The circuits included in this application note have been tested with National Semiconductor parts that may have been obsoleted and/or replaced with newer products. Please refer to the CLC to LMH conversion table to find the appropriate replacement part for the obsolete device.

Current vs. Voltage Feedback Amplifiers

National Semiconductor
OA-30
Debbie Brandenburg

One question continuously troubles the analog design engineer: "Which amplifier topology is better for my application, current feedback or voltage feedback?" In most applications, the differences between current feedback (CFB) and voltage feedback (VFB) are not apparent. Today's CFB and VFB amplifiers have comparable performance, but there are certain unique advantages associated with each topology. In general, VFB amplifiers offer:

- Lower Noise
- Better DC Performance
- Feedback Freedom

Aside from the well-known attribute of CFB amplifiers, gain-bandwidth independence, CFB amplifiers also tend to offer:

- Faster Slew Rates
- Lower Distortion
- Feedback Restrictions

With these common attributes known, the design engineer may still ask: "Why?" This article will examine the basics of the CFB amplifier in comparison with the VFB amplifier. The following aspects of each topology will be examined:

- Closed loop characteristics
- Open loop characteristics
- Input stage differences and advantages

Once these aspects are examined, it will become apparent why VFB amplifiers have better DC specifications and why CFB amplifiers have higher bandwidths for the same power and better linear phase performance over wider bands. Finally, an internal look at the CFB amplifier will explain why distortion and slew rate are enhanced by its topology.

Closed Loop Characteristics

The basic amplifier design schematics and their equations hold true for both amplifier topologies. *Figure 1* shows the basic circuit topologies and transfer functions for inverting and non-inverting gain configurations. These hold true for both CFB and VFB amplifiers. One point to remember is that the value of the feedback resistor is limited for CFB amplifiers. The CFB amplifier data sheet will provide the recommended R_f value.

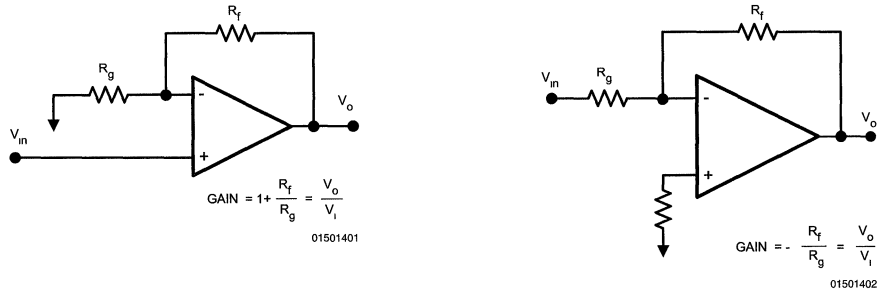


FIGURE 1. Basic Inverting and Non-Inverting Gain Topologies Hold True for CFB and VFB Amplifiers

These transfer functions assume ideal conditions. Under ideal conditions, the open loop gain A(s) of a VFB amplifier and the open loop transimpedance gain Z(s) of a CFB amplifier are infinite. Therefore, the ideal transfer function, for the non-inverting topology, is generated as follows:

$$\frac{V_{in}}{R_g} = \frac{V_o - V_{in}}{R_f}$$

$$\frac{V_o}{V_{in}} = \frac{R_f + R_g}{R_g}$$

$$\frac{V_o}{V_{in}} = 1 + \frac{R_f}{R_g}$$

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or

$$\text{LET } G = \frac{R_f + R_g}{R_g}$$

$$V_o = V_{in} G$$

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The output is equal to the input multiplied by the gain, G.

VFB Open Loop Characteristics

The fundamental differences between VFB and CFB amplifiers begin to show when comparing their open-loop characteristics. *Figure 2* illustrates the open-loop characteristics of a VFB amplifier.

VFB Open Loop Characteristics

(Continued)

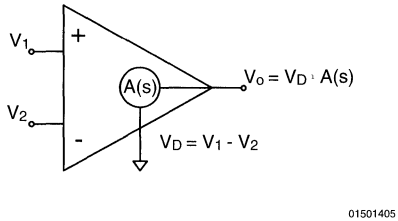

FIGURE 2. VFB Open-loop Characteristics

The ideal open-loop terminal characteristics are:

- Infinite non-inverting and inverting input impedances
- Zero output impedance

The output is a voltage source that is controlled by the potential difference between the two input terminals of the amplifier, also called the error voltage ($V_D = V_1 - V_2$). The output is equal to this error voltage multiplied by the open loop gain, A(s). Once the loop is closed, feedback will attempt to drive the error voltage to zero, hence the term voltage feedback.

Gain Bandwidth Product

Refer to the non-inverting gain topology of *Figure 1*. Remember that the open loop gain of a non-ideal amplifier is finite. Reevaluating, the non-ideal transfer function for a VFB amplifier becomes:

$$\frac{V_{in} - V_D}{R_g} = \frac{V_o - (V_{in} - V_D)}{R_f}$$

$$V_D = \frac{V_o}{A(s)}$$

$$R_f\left(V_{in} - \frac{V_o}{A(s)}\right) = R_g\left(V_o - V_{in} + \frac{V_o}{A(s)}\right)$$

$$R_f V_{in} - \frac{R_f V_o}{A(s)} = V_o\left(R_g + \frac{R_g + R_f}{C}\right)$$

$$\text{Let } G = \frac{R_f + R_g}{R_g}$$

$$V_o = V_{in}\left(\frac{G}{1 + \frac{G}{A(s)}}\right)$$

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As long as A>>G then the denominator becomes 1 and the amplifier behaves as it did in the ideal case.

The actual open loop gain is large at DC and rolls off at a rate of 6dB per octave, through most of the frequency range. As the frequency increases, the value of A(s) decreases. When A(s) = G, the overall gain of the circuit will be half its DC value. This is commonly referred to as the -3dB bandwidth of the amplifier. The rate at which the bandwidth decreases is proportional to 1/G. For most of the frequency range, the product of gain and bandwidth becomes constant. This is referred to as the gain-bandwidth product (GBP). GBP prevents VFB amplifiers from obtaining high gain and high bandwidths simultaneously. This is illustrated in *Figure 3*.

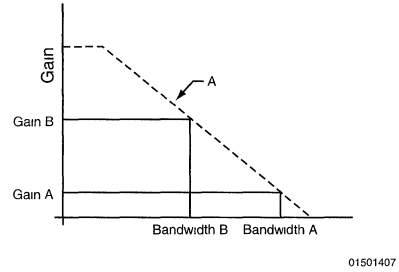

FIGURE 3. Open-Loop Gain A(s) and Illustration of the GBP for VFB Amplifiers

CFB Open-Loop Characteristics

Figure 4 illustrates the open-loop characteristics of a CFB amplifier

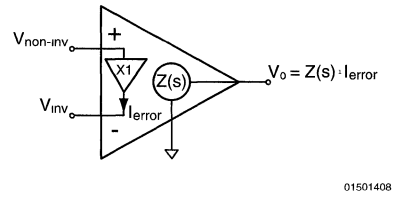

FIGURE 4. CFB Open-Loop Characteristics

There is a unity-gain buffer between the two inputs of the CFB amplifier. Ideally, this buffer has infinite input impedance and zero output impedance. Therefore, the ideal open-loop terminal characteristics are.

- Infinite non-inverting input impedance
- Zero inverting input impedance
- Zero output impedance

The output is a voltage source controlled by the error current, I_{error}, out of the inverting input. Once the loop is closed, feedback will attempt to drive the error current to zero, hence the term current feedback.

Gain Bandwidth Independence

CFB amplifiers are known for their gain-bandwidth independence. The reason for this attribute is explained by calculating the transfer function of a non-ideal CFB amplifier. The evaluation of the transfer function for non-inverting configu-

Gain Bandwidth Independence

(Continued)

ration is shown. The transfer function for an inverting configuration also illustrates the gain-bandwidth independence.

$$I_{error} = \frac{V_{in} - V_o}{R_f} + \frac{V_{in}}{R_g}$$

$$V_o = Z(s)\, I_{error}$$

$$\frac{V_o}{Z(s)} = \frac{V_{in} - V_o}{R_f} + \frac{V_{in}}{R_g}$$

$$\frac{V_o}{V_{in}} = \frac{\frac{1}{R_f} + \frac{1}{R_g}}{\frac{1}{Z(s)} + \frac{1}{R_f}}$$

$$\frac{V_o}{V_{in}} = \frac{R_g}{\frac{Z(s) + R_f}{Z(s)}}$$

$$\text{Let } G = \frac{R_f + R_g}{R_g}$$

$$V_o = V_{in} \frac{G}{1 + \frac{R_f}{Z(s)}}$$

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The CFB transfer function looks very similar to the VFB transfer function. As long as $Z >> R_f$ then the amplifier behaves as in the ideal case. Once Z(s) drops to where it equals R_f, then the gain is lowered to 1/2 its DC value. This differs from the VFB case where gain is determined by both R_f and R_g . For CFB amplifiers, if the gain is increased by lowering R_g, rather than increasing R_f , then the bandwidth is independent of gain.

This expression explains the importance of R_f for CFB amplifiers. CFB amplifier data sheets provide the recommended R_f values for various gain settings. An excessively large or small R_f will compromise stability. Within reason, the feedback resistor can be used to adjust the frequency response. As a rule of thumb, if the value of the recommended R_f is doubled, then the bandwidth will be cut in half.

An Internal look at the VFB Topology

By observing the open-loop characteristics of both amplifier topologies, the differences begin to become apparent. However, a closer look at the input stages will shed more insight into the battle, CFB vs. VFB. A typical VFB amplifier input stage is shown in *Figure 5.* It is a common fact that VFB amplifiers tend to have better DC specifications than CFB amplifiers. Most VFB amplifiers have:

- Low input offset voltage (V_{io})
- Matched input bias currents (I_b)
- High power supply rejection ratio (PSRR)
- Good common mode rejection ratio (CMRR)

A close look at the input stages of both topologies will explain why VFB amplifiers tend to have better DC specifications.

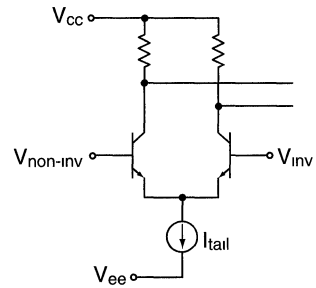

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FIGURE 5. Typical VFB Input Stage

The structure of the VFB input stage is the reason for better DC specifications. A VFB input stage is often a simple differential pair, two identical bipolar transistors at the same bias current and voltage. This configuration is often called a balanced circuit because of the symmetry between the two inputs. Because of this symmetry, there will be no input offset voltage unless the devices do not match.

The inputs are the bases of the two transistors. Although the absolute base currents, or input bias currents, may vary considerably due to process variation and temperature, again unless the devices are not identical, the input bias currents will match.

When either the supply voltage or the common mode input voltage is altered, the change in the collector to emitter voltages is matched for both of the input transistors. Changes in the devices bias point could effect offset, but again due to the balanced topology, the bias currents match and offset voltage is little effected. The result of this is good CMRR and PSRR.

An Internal Look at the CFB Topology

The input stage of a CFB amplifier will also describe a few inherent DC traits of the CFB amplifier:

- Nonzero V_{io}
- Unmatched I_b

The input stage of a typical CFB amplifier is illustrated in *Figure 6.* It is a voltage buffer. For the offset voltage to be zero, the V_{ee} of the NPN transistors would have to match the V_{ee} of the PNP. Since these devices are constructed differently, there is no reason why they would inherently match. Bias currents in CFB amplifiers are also fundamentally mismatched. The non-inverting bias current is the difference between two base currents where the inverting bias current depends on the errors produced in the next stage.

An Internal Look at the CFB Topology (Continued)

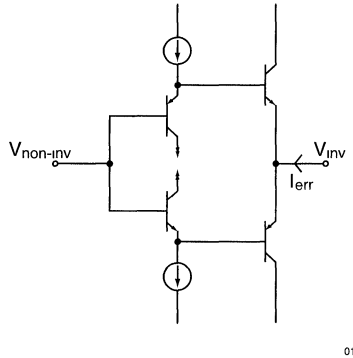


FIGURE 6. Typical CFB Amplifier Input Stage

Advantages of the CFB Topology

One hidden advantage of current feedback amplifiers is that they usually require fewer internal gain stages than their voltage feedback counterparts. Often a current feedback amplifier consists of merely an input buffer, one gain stage and an output buffer. Having fewer stages means less delay through the open-loop circuit. This translates into higher bandwidths for the same power.

The basic CFB topology in *Figure 7* is a single-stage amplifier. The only high impedance node in the circuit is at the input to the output buffer. VFB amplifiers usually require two or more stages for sufficient loop-gain. These additional stages add delay and yield lower stable bandwidths.

Distortion

The distortion of an amplifier is impacted by the open-loop distortion of the amplifier and the overall speed of the closed-loop circuit. The amount of open-loop distortion contributed by a CFB amplifier is small due to the basic symmetry of the topology. *Figure 7* illustrates a typical CFB topology. For every NPN transistor, there is a complimentary PNP transistor. Speed is the other main contributor to distortion. In many gain configurations, a CFB amplifier has a greater bandwidth than its VFB counterpart. So at a given signal frequency, the faster part has greater loop-gain and therefore lower distortion

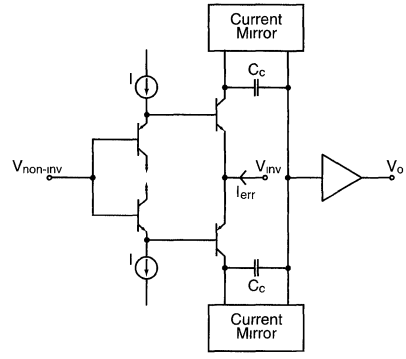


FIGURE 7. Basic CFB Topology

Slew Rate

Slew rate performance is also enhanced by the CFB topology. Refer to the typical CFB topology of *Figure 7*. The slew rate is determined by the rate at which the second two transistors can charge the compensation capacitors, C_c. The current that can be sourced by these transistors is dynamic. It is not limited to any fixed value as is often the case in VFB topologies. With a step input or overload condition, the current flowing through the transistors is increased and the overdriven condition is quickly removed. To the first order, there is no slew rate limit in this architecture. Some VFB amplifiers have input structures similar to CFB amplifiers in order to take advantage of the higher slew rate possibilities. The combination of higher bandwidths and slew rate allows CFB devices to have respectable distortion performance while doing so at a lower power.

The basic current feedback amplifier has no fundamental slew-rate limit. Limits only come about by parasitic transistor capacitances and many strides have been made to reduce even their effects.

The availability of high-speed operational amplifiers in both CFB and VFB topologies allows design engineers to select the best amplifier to fit his/her needs. A CFB amplifier compliments an application that requires high slew rates, low distortion, or the ability to set gain and bandwidth independently. While a VFB amplifier compliments an application where low offset voltage or low noise specifications are required.

Current Feedback Amplifiers

National Semiconductor
OA-31

In their effort to approximate the ideal op amp, manufacturers must not only maximize the open-loop gain and minimize input-referred errors such as offset voltage, bias current, and noise, but must also ensure adequate band-width and settling-time characteristics. Amplifier dynamics are particularly important in applications like high-speed DAC buffers, subranging ADCs, S/H circuits, ATE pin drivers, and video and IF drivers. *(Reference 1)*

Being basically voltage-processing devices, op amps are subject to the speed limitations inherent to voltage-mode operation, stemming primarily from the stray capacitances of nodes and the cutoff frequencies of transistors. Particularly severe is the effect of the stray capacitances between the input and output nodes of high-gain inverting stages because of the Miller effect which multiplies the stray capacitance by the voltage gain of the stage.

On the other hand, it has long been recognized that current manipulation is inherently faster than voltage manipulation. The effect of stray inductances in a circuit is usually less severe than that of its stray capacitances, and BJTs can switch currents much more rapidly than voltages. These technological reasons form the basis of emitter-coupled logic, bipolar DACs, current conveyors, and the high-speed amplifier topology know as *current-feedback*. *(Reference 2)*

For true current-mode operation, all nodes in the circuit should ideally be kept at fixed voltages to avoid the slow-down effect by their stray capacitances. However, since the output of the amplifier must be a voltage, some form of high-speed voltage-mode operation must also be provided at some point. This is achieved by employing gain configurations that are inherently immune from the Miller effect, such as the common-collector and the cascode configurations, and by driving the nodes with push-pull stages to rapidly charge/discharge their stray capacitances.

To ensure symmetric rise and fall times, the npn and pnp transistors must have comparable characteristics in terns of cutoff frequency f_t. Traditionally, monolithics pnp's have been plagued by much poorer performance characteristics than their npn counterparts. However, the recent development of truly complementary high-speed processes makes it possible to achieve monolithics speeds that were hitherto available only in hybrid form.

The advantages of the current-feedback topology are best appreciated by comparing it against that of the conventional op amp. *(Reference 3, Reference 4)*

The Conventional Op Amp

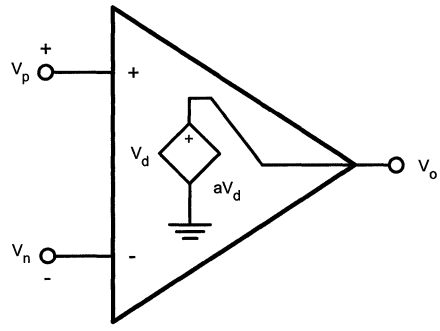
The conventional op amp consists of a high input-impedance differential stage followed by additional gain stages, the last of which is a low output-impedance stage. As shown in the circuit model of Figure 1A, the op amp transfer characteristic is

$$V_O = a(jf)\, V_d \qquad (1)$$

where V_O is the output voltage; $V_d = V_p - V_n$ is the differential input voltage; and a (jf), a complex function of frequency f_t, is the open-loop gain.

Connecting an external network as in Figure 1B creates a feedback path along which a signal in the form of a voltage is derived from the output and applied to the non-inverting input. By inspection.

$$V_d = V_i - \frac{R_1}{R_1 + R_2} V_o \qquad (2)$$



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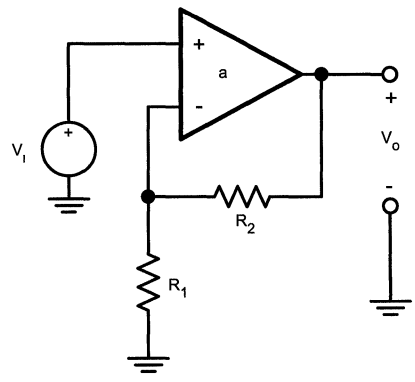


(b)

FIGURE 1. Circuit model of the conventional op amp, and connection as a non-inverting amplifier.

Substituting into Eq. (1), collecting, and solving for the ratio V_O/V_I yields the familiar non-inverting amplifier transfer characteristic

$$A(jf) \triangleq \frac{V_o}{V_i} = \left(1 + \frac{R_2}{R_1}\right) \frac{1}{1 + 1/T(jf)} \qquad (3)$$

The Conventional Op Amp (Continued)

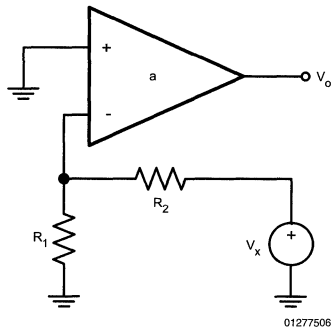
where A (jf) represents the closed-loop gain, and

$$T(jf) = \frac{a(jf)}{1 + R_2/R_1} \tag{4}$$

represents the loop gain.

The designation loop gain stems from the fact that if we break the loop as in Figure 2a and inject a test signal V_x with V_i suppressed, the circuit will first attenuate V_x to produce $V_n = V^x/(1 + R_2/R_1)1$ and then amplify V_n to produce $V_o = -aV_n$ Hence, the gain experienced by a signal in going around the loop is $V_o/V_x = -a/(1 + R_2/R_1)$. The negative of this ratio represents the loop gain , $T \equiv -(V_o/V_x)$. Hence, Eq. (4).

The loop gain gives a measure of how close A is to the ideal value $1 + R_2/R_1$, also called the noise gain of the circuit By Eq. (3), the larger T, the better. To ensure substantial loop gain over a wide range of closed-loop gains, op amp manufacturers strive to make a as large as possible. Consequently, V_d will assume extremely small values since $V_d = V_o/a$. In the limit $a \to \infty$ we obtain $V_d \to 0$, that is, $V_n \to V_p$. This forms the basis of the familiar op amp rule: when operated with negative feedback, an op amp will provide whatever output voltage and current are needed to ideally force V_n to follow V_p.



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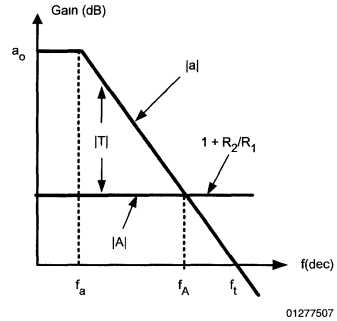


(b)

FIGURE 2. Test circuit to find the loop gain, and grapnical method to determine the closed-loop bandwidth f_A.

Gain Bandwidth Tradeoff

Large open-loop gains can physically be realized only over a limited frequency range. Past this range, gain rolls off with frequency. Most op amps are designed for a constant rolloff of –20dB/dec, so that the open-loop response can be expressed as

$$a(jf) = \frac{a_o}{1 + j(f/f_a)} \tag{5}$$

where a_o represents the dc gain, and f_a is the –3dB frequency of the open-loop response. Both parameters can be found from the data sheets. For example, the 741 op amp has $a_o \cong 2 \times 10^5$ and $f_a \cong 5$Hz.

Substituting Eq. (5) into Eq. (4) and then into Eq. (3), and exploiting the fact that $(1 + R_2/R_1)\ a_o <<$, we obtain

$$A(jf) = \frac{1 + R_2/R_1}{1 + j(f/f_A)} \tag{6}$$

where

$$f_A = \frac{f_t}{1 + R_2/R_1} \tag{7}$$

represents the closed-loop bandwidth, and $f_t = a_o f_a$ represents the open-loop unity-gain frequency, that is the frequency at which $|a| = 1$. For instance, the 741 op amp has $f_t = 2 \times 10^5 \times 5 = 1$ MHz.

Equation (7) reveals a gain-bandwidth tradeoff. As we raise the R_2/R_1 ratio to increase the closed-loop gain, we also decrease its bandwidth in the process. Moreover, by Eq. (4), the loop-gain is also decreased, thus leading to a greater closed-loop gain error.

The above concepts can also be visualized graphically. Since Eq. (4) implies $|T|_{dB} \equiv 20 \log |T| = 20 \log |a| - 20 \log (1 + R_2/R_1) \equiv |a|_{dB} - (1 + R_2/R_1)_{dB}$, it follows that the loop gain can be found graphically as the difference between the open-loop gain and the noise gain. This is shown in Figure 2b. The frequency at which the two curves meet is called the crossover frequency. At this frequency we have $T = -j$, that is, $|A| = (1 + R_2/R_1)/\sqrt{2}$. Thus, the crossover frequency represents the – 3dB frequency of the closed-loop response, that is, the closed-loop bandwidth f_A.

We now see that increasing the closed-loop gain shifts the noise-gain curve upward, thus reducing the loop gain, and causes the crosspoint to move up the |a| curve, thus decreasing the closed-loop bandwidth. Clearly, the circuit with the widest bandwidth and the highest loop gain is also the one with the lowest closed-loop gain. This is the voltage follower, for which $R_2/R_1 = 0$, so that $A = 1$ and $f_A = f_t$.

Slew-Rate Limiting

To fully characterize the dynamic behavior of an op amp, we also need to know its transient response. If an op amp with the response of Eq. (5) is operated as a unity-gain voltage follower and is subjected to a suitably small voltage step, its dynamic behavior will be similiar to that of an RC network. Applying an input step ΔV_i will cause the output to undergo an exponential transition with magnitude $\Delta V_o = \Delta V_i$, and with time-constant $\tau = 1/(2\pi f_t)$. For the 741 op amp we have $\tau = 1/(2\pi \times 10^6) \cong 170$ns.

The rate at which the output changes with time is highest at the beginning of the exponential transition, when its value is $\Delta V_o/\tau$. Increasing the step magnitude increases this initial rate of change, until the latter will saturate at a value called the slew-rate (SR). This effect stems from the limited ability of the internal circuitry to charge/discharge capacitive loads, especially the compensation capacitor responsible for open-loop bandwidth f_a.

To illustrate, refer to the circuit model of Figure 3, which is typical of many op amps *(Reference 4)*. The input stage is a transconductance block consisting of differential pair Q_1–Q_2 and current mirror Q_3–Q_4. The remaining stages are lumped together as an integrator block consisting of an inverting amplifier and the compensation capacitor C. Slew-rate limiting occurs when the transconductance stage is driven into saturation, so that all the current available to charge/discharge C is the bias current / of this stage. For example, the 741 op amp has I = 20μA and C = 30 pF, so that SR = I/C = 0.67 V/μs.

The step magnitude corresponding to the onset of slew-rate limiting is such that $\Delta V_i/\tau$ = SR, that is, ΔV_i = SR x τ = (0.67 V/μs) x (170ns) = 116mV. As long as the step is less than 116 mV, a 741 voltage follower will respond with an exponential transition governed by $\tau \cong 170$ ns, whereas for a greater input step the output will slew at a constant rate of 0.67 V/μs.

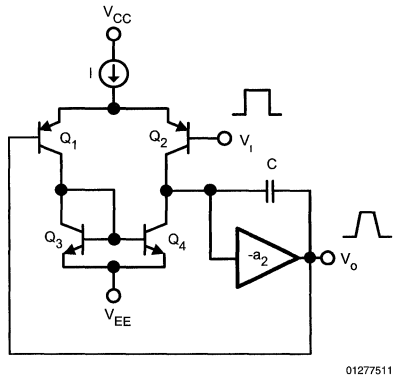


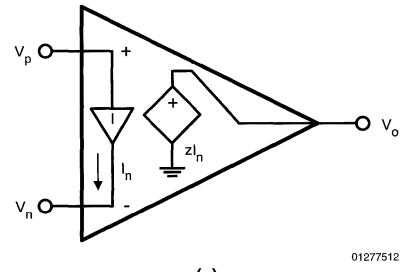
FIGURE 3. Simplified slew-rate model of a conventional op amp

In many applications the dynamic parameter of greatest concern is the settling time, that is, the time it takes for the output to settle and remain within a specified band around its final value, usually for a full-scale output transition. Clearly, slew-rate limiting plays an important role in the settling-time characteristic of the device.

The Current-Feedback Amplifier

As shown in the circuit model of Figure 4, the architecture of the current-feedback amplifier (CF amp) differs from the conventional op amp in two respects: *(Reference 2)*

1. The input stage is a unity-gain voltage buffer connected across the inputs of the op amp. Its function is to force V_n to follow V_p, very much like a conventional op amp does via negative feedback. However, because of the low output impedance of this buffer, current can easily flow in or out of the inverting input, though we shall see that in normal operation this current is extremely small.



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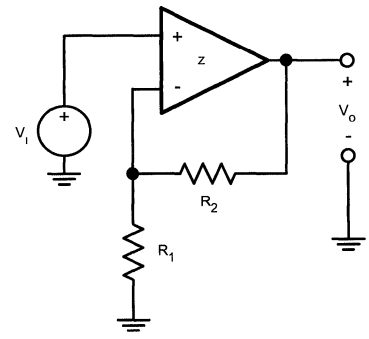


(b)

FIGURE 4. Circuit model of the current -feedback amplifier, and connection as a non-inverting amplifier

2. Amplification is provided by a transimpedance amplifier which senses the current delivered by the buffer to the external feedback network, and produces an output voltage V_o such that

$$Vo = z(jf)I_n \qquad (8)$$

where A z(jf) represents the transimpedance gain of the amplifier, in V/A or Ω, ind I_n is the current out of the inverting input.

The Current-Feedback Amplifier

(Continued)

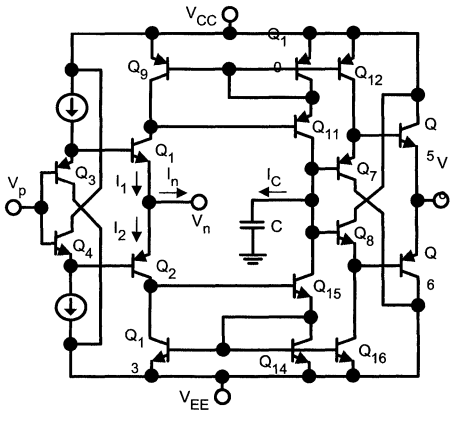
To fully appreciate the inner workings of the CF amp, it is instructive to examine the simplified circuit diagram of Figure 5a. The input buffer consists of transistors Q_1 through Q_4. While Q_1 and Q_2 form a low output-impedance push-pull stage, Q_3 and Q_4 provide V^{BE} compensation for the push-pull pair, as well as a Darlington function to raise the input impedance.

Summing currents at the inverting node yields $I_1 - I_2 = I_n$, where I_1 and I_2 are the push-pull transistor currents. Two Wilson current mirrors, consisting of transistors Q_9–Q_{10}–Q_{11} and Q_{13}–Q_{14}–Q_{15}, reflect these currents and recombine them at a common node, whose equivalent capacitance to ground has been designated as C. By mirror action, the current through this capacitance is $I_c = I_1 - I_2$, that is

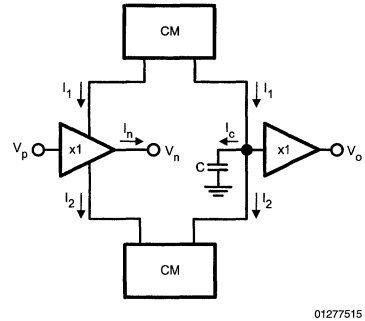
$$I_c = I_n \qquad (9)$$

The voltage developed by C in response to this current is then conveyed to the output via a second buffer, consisting of Q_5 through Q_8. The salient features of the CF amp are summarized in block diagram form in Figure 5b.

When the amplifier loop is closed as in Figure 4b, and whenever an external signal tries to imbalance the two inputs, the input buffer will begin sourcing (or sinking) an imbalance current I_n to the external resistances. This imbalance is the conveyed by the Wilson mirrors to capacitor C, causing V_o to swing in the positive (or negative) direction until the original imbalance I_n is neutralized via the negative feedback loop. thus, I_n plays the role of error signal in the system.



(a)



(b)

FIGURE 5. Simplified circuit diagram and block diagram of a current-feedback amplifier

To obtain the closed-loop transfer characteristic, refer again to Figure 4b. Summing currents at the inverting node yields

$$I_n = \frac{V_n}{R_1} - \frac{V_o - V_n}{R_2} \qquad (10)$$

since the buffer ensures V_n V_p V_i we can rewrite as

$$I_n = \frac{V_i}{R_1 \,||\, R_2} - \frac{V_o}{R_2} \qquad (11)$$

confirming that the feedback signal V_o/R_2 is now in the form of a current. Substituting into Eq. (8), collecting and solving for the ratio V_o/V_i yields

$$A(jf) \triangleq \frac{V_o}{V_i} = \left(1 + \frac{R_2}{R_1}\right) \frac{1}{1 + 1/T(jf)} \qquad (12)$$

where A (jf) represents the closed-loop gain of the circuit, and

$$T(jf) = \frac{z(jf)}{R_2} \qquad (13)$$

represents the loop gain. This designation stems again from the fact that if we break the loop as in Figure 6a, and inject a test voltage V_x with the input V_i suppressed, the circuit will first convert V_x to the current $I_n = -V_x/R_2$, and then convert I_n to the voltage $V_o = zI_n$, so that $T \equiv -(V_o/V_x) = z/R_2$, as expected.

In an effort to ensure substantial loop gain to reduce the closed-loop gain error, manufacturers strive to make z as large as possible relative to the expected values of R_2. Consequently, since $I_n = V_o/z$, the inverting-input current will be very small, though this input is a low-impedance node because of the buffer. In the limit $z \to \infty$ we obtain $I_n \to 0$, indicating that a CF amp will provide whatever output voltage and current are needed to ideally drive I_n to zero. Thus, the conventional op amp conditions $V_n = V_p$ and $I_n = I_p = 0$ hold for CF amps as well.

The Current-Feedback Amplifier (Continued)

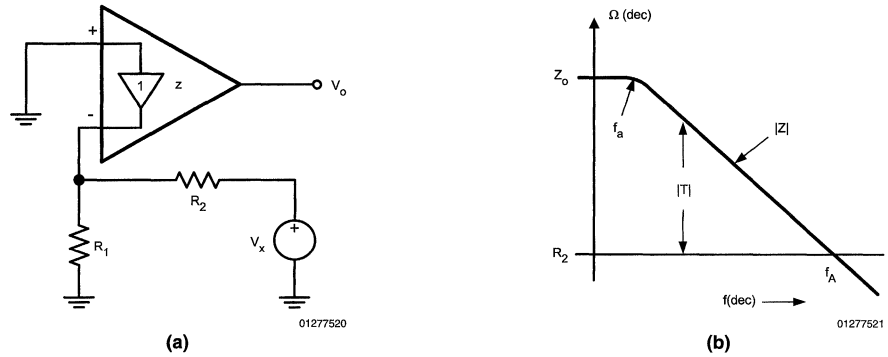


FIGURE 6. Test circuit to find the loop gain, and graphical method to determine the close-loop bandwidth f_A

No Gain-Bandwidth Tradeoff

The transimpedance gain of a practical CF amp rolls off with frequency according to

$$z(jf) = \frac{z_o}{1 + j(f/f_a)} \qquad (14)$$

where z_o is the dc value of the transimpedance gain, and f_a is the frequency at which rolloff begins. For instance, from the data sheets of the CLC401 CF amp (Comlinear Co.) we find z_o = 710 kΩ, and f_a = 350 kHz.

Substituting Eq. (14) into Eq. (13) and then into Eq. (12), and exploiting the fact that $R^2/z_o << 1$, we obtain

$$A(jf) = \frac{1 + R_2/R_1}{1 + j(f/f_A)} \qquad (15)$$

where

$$f_A = \frac{z_o f_a}{R_2} \qquad (16)$$

represents the closed-loop bandwidth, for R_2 in the kΩ range, f_A is typically in the 100MHz. Retracing previous reasoning, we see that the noise-gain curve is now R_2, and that f_A can be found graphically as the frequency at which this curve meets the | z | curve, see Figure 6b.

Comparing with Eq. (6) and (7), we note that the closed-loop gain expressions are formally identical.

However, the bandwidth now depends only on R_2 rather than on the closed-loop gain 1 + R_2/R_1. Consequently, we can use R_2 to select the bandwidth, and R_1 to select the gain. The ability to control gain independently of bandwidth constitutes a major advantage of CF amps over conventional op amps, especially in automatic gain control applications. This important difference is highlighted in Figure 7.

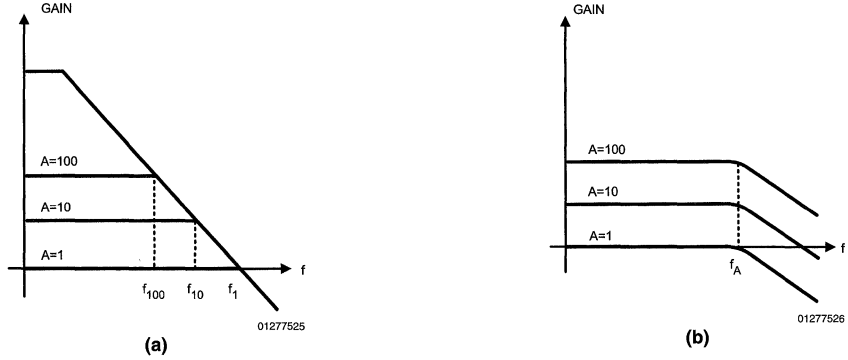


FIGURE 7. Comparing the gain-bandwidth relationship of conventional op amps and current-feedback amplifiers.

Absence of Slew-Rate Limiting

The other major advantage of CF amps is the inherent absence of slew-rate limiting. This stems from the fact that the current available to charge the internal capacitance at the onset of a step is proportional to the step regardless of its size. Indeed, applying a step ΔV_i induces, by Eq. (11), an initial current imbalance $I_n = \Delta V_i/(R_1 \parallel R_2)$, which the Wilson mirrors then convey to the capacitor. The initial rate of charge is, therefore, $I_c/C = I_n/C = \Delta V_i/[(R_1 \parallel R_2)C] = [\Delta V_i(1 + R_2/R_1)] / (R_2C) = \Delta V_o/(R_2C)$, indicating an exponential output transition with time-constant $\tau = R_2C$ Like the frequency response, the transient response is governed by R_2 alone, regardless of the closed-loop gain. With R_2 in the kΩ range and C in the pF range, τ comes out in the ns range.

The rise time is defined as the amount of time t_r it takes for the output to swing from 10% to 90% of the step size For an exponential transition, $t_r = \tau \times \ln(0.9/0.1) = 2.2\tau$.

For example, the CLC401 has t_r = 2.5 ns for a 2V output step, indicating an effective τ of 1.14 ns. The time it takes for the output to settle within 0.1% of the final value is $t_s = \tau \ln 1000 \cong 7\tau$. For the CLC401, this yields $t_s \cong 8$ ns, in reasonable agreement with the data sheet value of 10 ns.

The absence of slew-rate limiting not only allows for faster settling times, but also eliminates slew-rate related nonlinearities such as intermodulation distortion. this makes CF amps attractive in high-quality audio amplifier applications.

Second-Order Effects

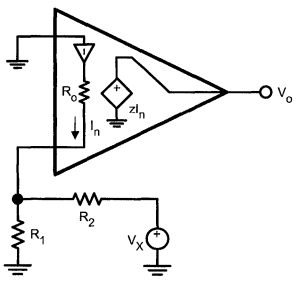
The above analysis indicates that once R_2 has been set, the dynamics of the amplifier are unaffected by the closed-loop gain setting In practice it is found that bandwidth and rise time do vary with gain somewhat, though not as drastically as with conventional op amps.

The main cause is the non-zero output impedance of the input buffer, whose effect is to alter the loop gain and, hence, the closed-loop dynamics.

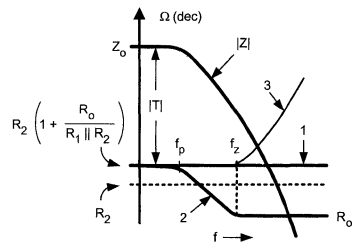
Referring to Figure 8a and denoting this impedance as R_o, we note that the circuit first converts V_x to a current $I_{R2} = V_x/(R_2 + R_1 \parallel R_o)$, then it divides I_{R2} to produce $I_n = I_{R2}R_1/(R_1 + R_o)$, and finally it converts I_n to the voltage $V_o = zI_n$. Eliminating I_{R2} and I_n and letting $T = -V_o/V_x$ yields $T = z/Z_2$, where

$$Z_2 = R_2\left(1 + \frac{R_o}{R_1 \parallel R_2}\right) \qquad (17)$$

Thus, the effect of R_o is to increase the noise gain from R_2 to $R_2[1 + R_o/(R_1 \parallel R_2)]$, see Figure 8b, curve 1. Consequently, both bandwidth and rise time will be reduced by a proportional amount.



(a)



(b)

FIGURE 8. Test circuit to investigat the effect of R_o, and noise-gain curves for the case of: (1) purely resistive feedback, (2) a capacitance in parallel with R_2, and (3) the same capacitance in parallel of R_1.

Replacing R_2 with Z_2 in Eq. (16) yields, after simple manipulation,

$$f_A = \frac{f_t}{1 + \frac{R_o}{R_2}\left(1 + \frac{R_2}{R_1}\right)} \qquad (18)$$

where $f_t = z_o f_a/R_2$ represents the extrapolated value of f_A in the limit $R_o \rightarrow 0$. This equation indicates that bandwidth reduction due to R_o will be more pronounced at high closed-loop gains. As an example, suppose a CF amp has R_o = 50Ω. R_2 = 1.5 kΩ, and f_t = 100MHz, so that $f_A = 10^8/[1 + (50/1500)A^o] = 10^8/(1 + A_o/30)$, where $A_o = 1 + R_2/R_1$. Then, the bandwidths corresponding to A_o = 1, 10, and 100 are, respectively, f_1 = 96.8 MHz, f_{10} = 75.0 MHz, and f_{100} = 23.1 MHz. Note that these values still compare favorably with a conventional op amp, whose bandwidth would be reduced, respectively, by 1, 10, and 100

If so desired, the external resistance values can be predistorted to compensate for the bandwidth reduction at high gains. turning Eq. (18) around yields the required value of R_2 for a given bandwidth f_A and gain A_o.

$$R_2 = \frac{z_o f_a}{f_A} - R_o A_o \qquad (19)$$

while the required value of R_1 for the given gain A_o is

$$R_1 = \frac{R_2}{A_o - 1} \qquad (20)$$

As an example, suppose we want the above amplifier to retain its 100 MHz bandwidth at a closed-loop gain of 10. Since with R_2 = 1.5kΩ this device has $z_o f_a/R_2$ = 100 MHz, it

Second-Order Effects (Continued)

follows that $z_o f^a = 10^8 \times 1500 = 1.5 \times 10^{11}\ \Omega \times Hz$. Then, the above equations yield $R_2 = 1.5 \times 10^{11} / 10^8 - 50 \times 10 = 1\ k\Omega$, and $R_1 = 1000/(10 - 1) = 111\ \Omega$.

Besides the dominant pole at f_a, the open-loop response of a practical amplifier presents additional poles above the crossover frequency. As shown in Figure 8b, the effect of these poles is to cause a stepper gain rolloff at this frequency, further reducing the closed-loop bandwidth.

Moreover, the additional phase-shift due to these poles decreases the phase margin somewhat, thus causing a small amount of peaking in the frequency response, and ringing in the transient response.

Finally, it must be said that the rise time of a practical CF amp does increase with the step size somewhat, due primarily to transistor current gain degradation at high current levels. For instance, the rise time of the CLC401 changes from 2.5 ns to 5 ns as the step size is changed from 2V to 5V. In spite of second-order limitations, CF amps still provide superior dynamics.

CF Applications Considerations

Although, the above treatment has focused on the noninverting configuration, the CF amp will work as well in most other resistive feedback configurations, such as the inverting amplifier, the summing and differencing amplifier, I-V and V-I converters, and KRC active filters *(Reference 4)*. In fact, the derivation of the transfer characteristic of any of these circuits proceeds along the same lines as conventional op amps. Special consideration, however, require the cases in which the feedback network includes reactive elements, either intentional or parastic.

Consider first the effect of a feedback capacitance C_2 in parallel with R_2 in the basic circuit of Figure 8a. Letting $Z = R_2 || (1/sC_2)$, the noise gain, becomes $Z_2 = Z\,[1 + R_o/(R_1 || Z)]$. After expanding, it is readily seen that the noise-gain curve has a pole at $f_p = 1/(2\pi R_2 C_2)$ and a zero at $f_z = 1/[2\pi(R_o || R_1 || R_2)C_2]$, as shown in Figure 8b, curve 2. Consequently, the crossover frequency will be pushed into the region of substantial phase shift due to the higher-order poles of z. If the overall shift reaches -180° at this frequency then $T = -1$ there, indicating that A will become infinite by Eq. (12), and the circuit will oscillate. Even if the phase shift fails to reach -180°, the closed-loop response may still exhibit intolerable peaking and ringing. Hence, capacitive feedback must be avoided with CF amps. To minimize the effect of stray feedback capacitances, manufacturers often provide R_2 internally.

CF Integrators

To synthesize the integrator function in CF form, which provides the basis for dual-integrator-loop filters and oscillators as well as other popular circuits, we must use configurations that avoid a direct capacitance between the output and the inverting input. One possibility is offered by the Deboo integrator *(Reference 4)*, which belongs to the class of KRC filters and is therefore amenable to CF realization. Its drawback is the need for tightly matched resistances, if lossless integration is desired. The alternative of Figure 9 not only meets the given constraint, but also provides active compensation, a highly desirable feature to cope with Q-enhancement problems in dual-integrator-loop filters *(Reference 4)*. Using standard op amp analysis techniques, it is readily seen that the unity-gain frequency of this integrator is $f_o = (R_2/R_1) / (2\pi RC)$.

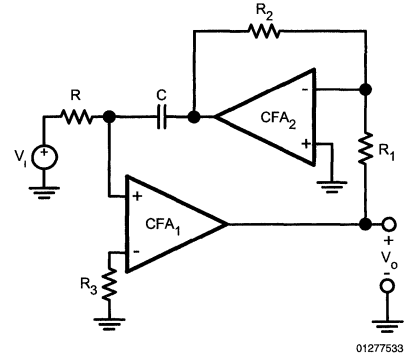


FIGURE 9. Actively-compensated CF integrator.

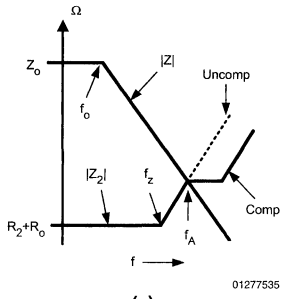
Stray Input-Capacitance Compensation

Next, consider the effect of an input capacitance C_1 in parallel with R_1 in the basic circuit of Figure 8a. Letting $Z = R_1 || (1/sC_1)$, the noise gain is now $Z_2 = R_2[1 + R_o/(Z || R_2)]$. After expanding, it is readily seen that the noise-gain curve has a zero at $f_z = 1/[2\pi(R_o || R_1 || R_2)\,C_1]$, as shown in Figure 8b, curve 3. If C_1 is sufficiently large, the phase of T at the crossover frequency will again approach -180°, bringing the circuit on the verge of instability. This is of particular concern in current-mode DAC output buffering, where C_1 is the output capacitance of the DAC, typically in the range of a few tens to a few hundreds of picofarads, depending on the DAC type.

Like a conventional op amp, the CF amp can be stabilized by using a feedback capacitance C_2 to introduce sufficient phase-lead to compensate for the phase-lag due to the input capacitance C_1. For a phase margin of 45°, choose the value of C_2 so that the noise-gain pole $f_p = 1/(2\pi R_2 C_2)$ coincides with the crossover frequency f_A, as shown in Figure 10a. Using asymptotic Bode-plot reasoning *(Reference 4)*, it is easily seen that $f_A = [z_o f_a f_z/(R_o + R_2)]^{1/2}$, where $f_z = 1/[2\pi(R_o || R_2)C_1]$. Imposing $f_p = f_A$ yields

$$C_2 = \left(\frac{R_o}{2\pi R_2 z_o f_a} C_1\right)^{1/2} \qquad (21)$$

Stray Input-Capacitance Compensation (Continued)



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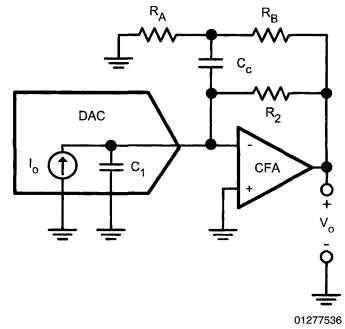

(b)

FIGURE 10. DAC output capacitance compensation.

To cope with impractically low values of C_2, it is convenient to drive C_2 with a voltage divider as in Figure 10b, since this will scale the value of C_2 to the more practical value.

$$C_c = \left(1 + \frac{R_B}{R_A}\right) C_2 \qquad (22)$$

It can be shown that for this technique to be effective we must choose $R_B << R_2$. As an example, suppose a DAC having C_1 = 100 pF feeds the CF amp considered earlier. Then, Eq. (21) yields $C_2 = [50 \times 100 \times 10^{-12} / (2\pi \times 1\ 5 \times 10^3 \times 1.5 \times 10^{11})]^{1/2} = 1.88$ pF. To scale it to a more practical value use *(Reference 5)* $R_A = 50\Omega$ and $R_B = 500\Omega$ Then, C_C = (1 + 500/50) 1.88 ≅ 21 pF. This estimate may require some fine tuning to optimize the transient response.

Additional useful application hints can be found in *(Reference 5).*

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Section 4

High Speed Amplifiers and Signal Conditioning: System Applications

Section 4 Contents

Designing with a New Super Fast Dual Norton Amplifier

National Semiconductor
Application Note 278
Timothy T Regan

Why Another Norton Amplifier?

The current differencing Norton amplifier has been widely applied over the last 5 years because of the versatility and availability of quad Norton amplifiers (the LM3900) These low cost quads are found today in a wide variety of analog systems, but primarily in medium frequency and single supply AC applications Today, a brand new dual current differencing amplifier, the LM359, offers spectacular speed improvements which can be used in circuits operating well beyond the video frequencies

HOW THE SPEED IS IMPROVED

The speed improvement of the new Norton amplifier is due to the cascode circuit (*Figure 1*). Cascode circuits are used in high frequency single-ended amplifier designs because there is no Miller effect on the collector-to-base capacitance of the input transistor Also, there is no collector-to-emitter parasitic feedback in the common base configured transistor, Q2, so the high frequency signal appearing at the output of the cascode does not reflect back into the input. Furthermore, note that band-limiting PNP transistors are eliminated from the signal path, here PNPs are used only for collector loads, so not only is high speed maintained, but high gain is also obtained without additional amplification stages.

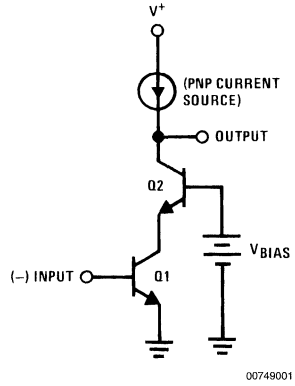


FIGURE 1. Basic Cascode Circuit

ADDING A MIRROR TO GET DIFFERENTIAL INPUTS

To make the high frequency single-ended amplifier more versatile differential inputs should be provided. An easy way is to add a current mirror across the negative (inverting) input terminal (*Figure 2*). This method provides current differencing, as the current entering the non-inverting input is extracted from the inverting input current The LM359 is then a current differencing, as opposed to a voltage differencing, op amp.

THE PROGRAMMABLE FEATURES EXTEND VERSATILITY

An additional feature of the LM359 is the programmability of its speed, its input impedance, and its output current sinking capability for line driver applications and for control of overall power consumption (*Figure 3*). An internal compensation capacitor is adequate compensation for all inverting applications where the gain is 10 or higher. An additional compensation capacitor can be added externally to reduce undesired bandwidth or to fit any particular application, as will be discussed later The following sections illustrate some new design ideas using this fast Norton amplifier.

A New High Frequency Active Filter Structure

Multiple op amp active filter building blocks are very popular because of their low sensitivities and their tunability. The basic element of such a filter is the inverting integrator Usually two inverting integrators are cascaded and a third inverter allows closing the overall loop with the proper phase. This is the idea behind the state variable and bi-quad filter structures which today are fully available in low cost hybrid forms

A New High Frequency Active Filter Structure (Continued)

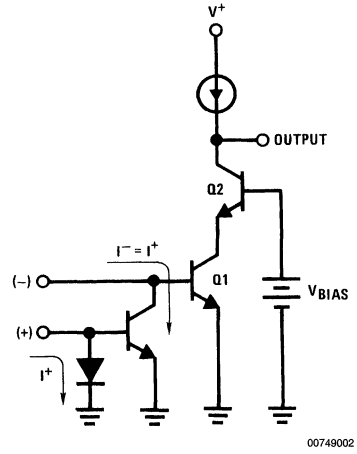


FIGURE 2. Adding a Current Mirror to Provide Current Differencing Inputs

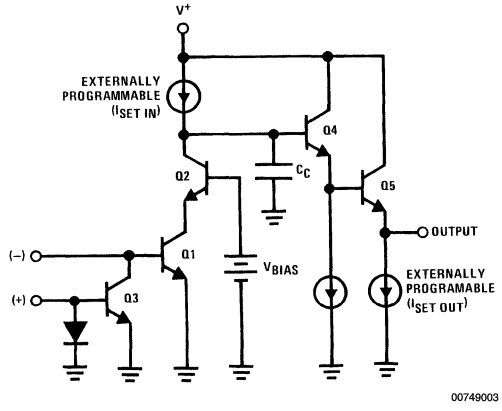


FIGURE 3. A Simplified Schematic of the LM359, a High Speed, Current Differencing Amplifier. The Input, Output and Speed Characteristics are Externally Programmable.

The op amp count in these filters could be reduced by one (allowing use of a dual op amp instead of 3 op amps or a quad) if a true non-inverting integrator could be built with a single op amp. Unfortunately, this cannot be done with standard op amps but is a trivial task with current differencing amplifiers (*Figure 4*). Combining a non-inverting integrator with an inverting one, a new high frequency and low sensitivity active filter building block can be made (*Figure 5*). *Table 1* shows the 3 particular filter structures, together with their design equations, which are derived from *Figure 5*. The frequency compensation for the 2 amplifiers is asymmetric to optimize performance. Also, since the LM359 is a wide bandwidth amplifier, high frequency circuit layout is strongly recommended. The circuit works with a single supply, and the output DC biasing of each filter type is provided with 2 resistors, R1 and R_b, which should be chosen according to *Table 2*.

A New High Frequency Active Filter Structure (Continued)

TABLE 1. Analysis and Design Equations

Type	V_{O1}	V_{O2}	C_I	R_{I2}	R_{I1}	f_o	Q_o	f_Z (Notch)	H_o (LP)	H_o (BP)	H_o (HP)
I	BP	LP	O	R_{I2}	∞	$\frac{1}{2\pi RC}$	$\frac{R_Q}{R}$	–	$\frac{R}{R_{I2}}$	$\frac{R_Q}{R_{I2}}$	–
II	HP	BP	C_I	∞	∞	$\frac{1}{2\pi RC}$	$\frac{R_Q}{R}$	–	–	$\frac{R_Q C_I}{RC}$	$\frac{C_I}{C}$
III	Notch or Band-Reject	–	C_I	∞	R_{I1}	$\frac{1}{2\pi RC}$	$\frac{R_Q}{R}$	$\frac{1}{2\pi RR_I CC_I}$	–	–	$\frac{C_I}{C}$ as f $\rightarrow \infty$ $\frac{R}{R_1}$ as f $\rightarrow 0$

TABLE 2. DC Biasing Equations for V_{O1} (DC) $\cong V_{O2}$ (DC) $\cong V^+/2$

Type I	$\frac{2V_{IN}(DC)}{V^+(R_{I2})} + \frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}$; R1 = 2R
Type II	$\frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}$, R1 = 2R
Type III	$\frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}; \frac{1}{R1} = \frac{V_{IN}(DC)}{V^+(R_{I1})} + \frac{1}{2R}$

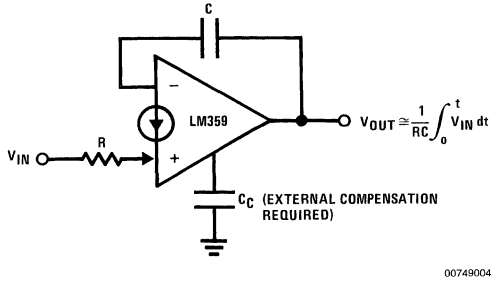
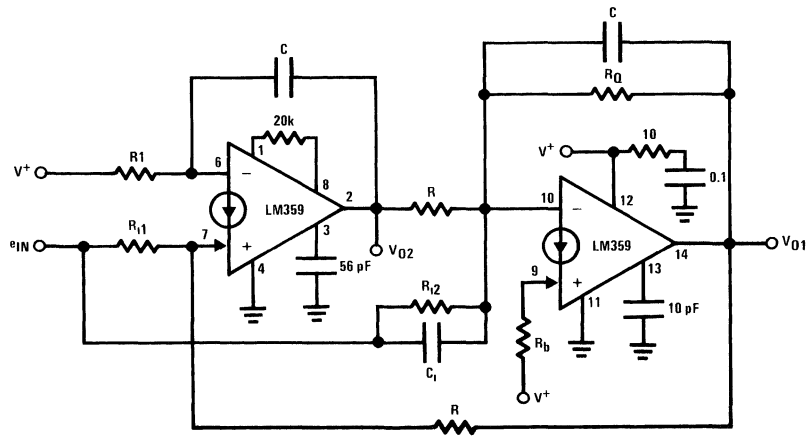


FIGURE 4. A True Non-Inverting Integrator

A New High Frequency Active Filter Structure (Continued)



Tables 1, 2 relate to *Figure 5*

FIGURE 5. High Performance 2 Amplifier Bi-Quad Filter. Half of the LM359 Acts as a Non-Inverting Integrator and the Other Half Acts as an Inverting One. No Extra Inversion is Necessary to Provide Proper Phase.

The operating range of an active filter can be estimated by comparing its Q_o, center frequency product (f_o x Q_o), with the gain bandwidth product (GBW) of its active elements. The f_o x Q_o should be less than the active element GBW by a factor of at least 20; a higher factor will yield less sensitive filters. For instance, with a 5 MHz op amp, the f_o x Q_o product of the filter should not exceed 250 kHz, and in reality should be even less. The filters tested with the LM359 could extend their f_o x Q_o product up to 2 MHz.

Voltage-Controlled Low Pass Filter

A most unique feature of the LM359 is that it provides the user with complete control of its frequency response over a very wide range. The combination of both programmable input stage current and external compensation capability is the key to this flexibility.

One of the most simple, yet illustrative, examples of the usefulness of this capability is the voltage-controlled low pass filter shown in *Figure 6*. The corner frequency of this filter is determined by the closed loop corner frequency of the inverting, gain of 100 amplifier. This frequency is directly controlled by the frequency of the dominant pole of the amplifier's open loop response, which can be approximated by the expression:

$$f_p \cong \frac{3\, I_{SET\ IN}}{2\,\pi\, C_{COMP}\, A_{VOL}\, V_T}$$

where A_{VOL} is the amplifier's DC open loop gain, V_T is equal to KT/q or 0.026V at room temperature, $I_{SET\ IN}$ is the input stage programming current, and C_{COMP} is the total compensation capacitance.

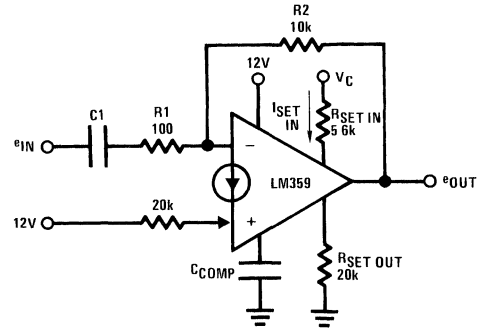


FIGURE 6. Voltage-Controlled Low Pass Filter. Minimum Input Frequency is Determined by C1 and R1.

The closed loop corner frequency, which, as stated is also the corner frequency of the filter, is:

$$f_c = \beta \bullet GBW = \beta \bullet A_{VOL} \bullet f_p$$

where β is the feedback factor, R1/(R1+R2), and a single pole open loop frequency response is assumed. Combining these two expressions, the corner frequency is:

$$f_c = \frac{3\, I_{SET\ IN} \bullet \beta}{2\,\pi\, C_{COMP}\, V_T}.$$

Voltage-Controlled Low Pass Filter

(Continued)

The simplest method to dynamically control f_c is to vary $I_{SET\ IN}$ through a control voltage, V_C, where:

$$I_{SET\ IN} = \frac{V_C - V_{BE}}{R_{SET\ IN} + 500\Omega}.$$

In this manner, C_{COMP} should be chosen for the highest desired corner frequency at maximum $I_{SET\ IN}$. Two curves illustrating the dependence of the corner frequency on $I_{SET\ IN}$ for two different compensation capacitors are shown in *Figure 7*.

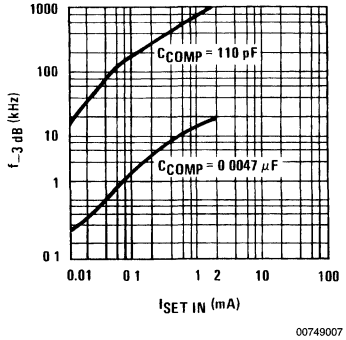


FIGURE 7. Amplifier Closed Loop Corner Frequency vs $I_{SET\ IN}$

It should be noted that as the compensation capacitor is increased, or $I_{SET\ IN}$ is decreased, the maximum slew rate of the amplifier is decreased. To prevent slew rate induced distortion of sinusoidal input signals, the following restriction applies:

$$\text{Slew rate max} = \frac{3\ I_{SET\ IN}}{C_{COMP}} \geq \omega\ V_o\ \text{peak},$$

where V_o peak is the peak output voltage of the filter and ω is $2\ \pi\ f_{IN}$, where f_{IN} is the signal frequency. The output voltage for signal frequencies less than the corner frequency of the filter (within the passband) should then be restricted to:

$$V_o\ \text{peak} \leq \frac{V_T}{\beta}.$$

Video Amplifiers

The basic principle behind the design of the LM359 is to provide amplification of high frequency signals with the ease of using standard operational amplifiers. The most obvious application area for this amplifier is in the video area where a fair amount of gain is required at frequencies much higher than monolithic op amps can provide.

A specific application is the amplification or buffering of a composite video signal for a distributed monitor system.

Figure 8 shows a typical connection for a non-inverting video amplifier whose signal source may be either detected video from a receiver, or possibly a camera signal. The output stage of the LM359 can be programmed, as shown, to drive a terminated 75Ω cable to 4 Vp-p for use as a video line driver. For color signals, the differential phase error and differential gain error at 3.58 MHz are desirably low, as noted in *Table 3*.

TABLE 3. Typical Video Amplifier Performance

A_V = 20 dB	
−3 dB Bandwidth →	2.5 Hz to 25 MHz
Differential Phase Error <1°	at 3.58 MHz
Differential Gain Error < 2%	at 3.58 MHz
Amplifier Output Swing =	4 Vp-p Max

For general purpose wideband amplifiers, the availability of two amplifiers in a single package allows cascading two gain stages to achieve very high gain bandwidth products as shown in *Figure 9*.

Disc and Magnetic Tape Memory Sensing

In digital data recovery from a magnetic storage medium, such as a disc or magnetic tape, there exists a need for high gain bandwidth amplifiers to convert the low level voltage transients from the output of the playback head (caused by a magnetic flux reversal on the tape or disc) to digital pulses that can be processed by data separating or decoding circuitry. The two amplifiers in a single LM359 package can be combined in a variety of ways to provide the basic blocks of a playback channel.

a) For very high bit rates and low level signals they can be cascaded to optimize overall gain bandwidth product, as already shown in *Figure 9*.

b) For single-ended playback signals (non center-tapped head), one amplifier can be used as a gain stage and the other as a differentiating stage to convert recovered signal peaks into bi-directional zero crossing signals, and then properly drive a comparator with regard to direction of flux changes on the disc or tape; this simplifies decoding of phase-encoded data.

c) For differential playback signals (center-tapped head), one amplifier can be used to provide gain for each output signal individually to retain the differential signal, or a single amplifier difference amp can perform a differential to single-ended conversion and the other amplifier can perform differentiation of the single-ended signal. For multi-channel, parallel recorded data, the overall component count of the playback system can be minimized by using one amplifier of the LM359 per channel.

Disc and Magnetic Tape Memory Sensing (Continued)

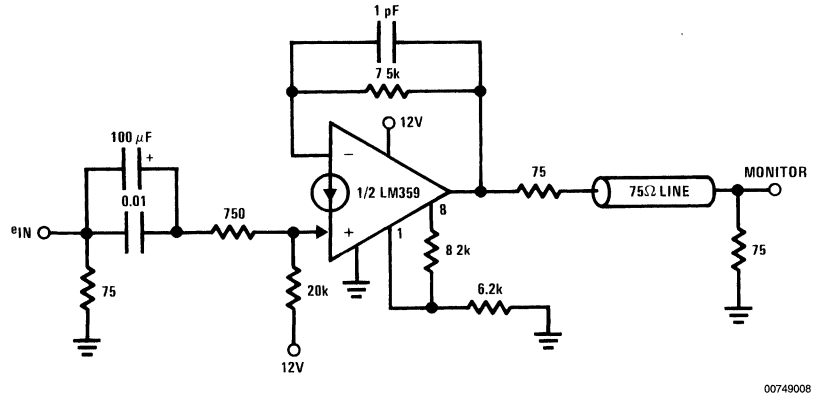
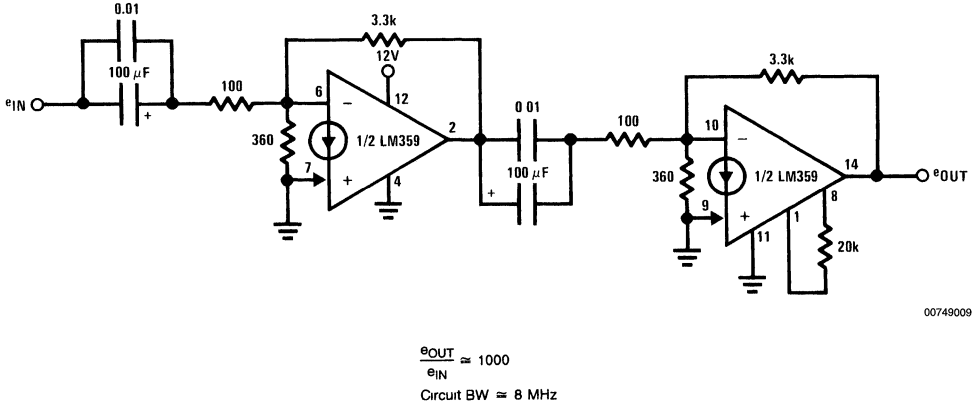


FIGURE 8. A Typical Application of this Fast Norton Amplifier as a High Perfomance Video Amplifier Driving a 75Ω Line



$$\frac{e_{OUT}}{e_{IN}} \cong 1000$$

Circuit BW ≅ 8 MHz

FIGURE 9. General Purpose, High Gain, Wideband Amplifiers Can Be Obtained by Cascading the 2 Norton Amplifiers Available on a Single Chip

Combining gain with constant delay filtering: Another important application of the LM359 in data recovery systems is that of filtering. It is most desirable to prevent high frequency noise spikes from being coupled through the sensing stage causing erroneous readings, but the low pass filter used must not induce time delays to valid data signals which will be decoded by their time relationship to each other. This immediately implies a constant group delay low pass filter or a Bessel filter approximation which, if implemented with active components, can also provide signal gain. *Figure 10* shows a fourth order, 250 kHz, gain of 100 Bessel filter. Here, because of the low Q_o requirements of the Bessel filter, a simple (Sallen-Key) filter structure has been chosen over the previously discussed higher performance structures. Note, however, that constant group delay filtering and amplification are performed with a single package.

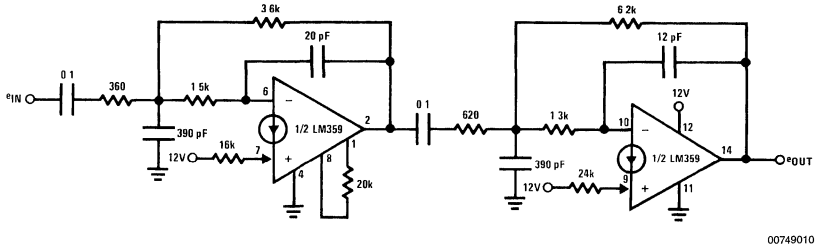
A Handle on Input Noise

The programmability of the amplifier's input stage current and the ability to "shut off" the non-inverting input current mirror allows significant improvements of the noise characteristics. For an inverting application where the non-inverting input would only be used for DC biasing purposes, an alternate biasing scheme, the nV_{BE}biasing, can be used, as shown in *Figure 11*. This allows "shutting off" the input current mirror which, in itself, will reduce the input noise by a factor of two.

In addition, the input stage programming current can be increased to further reduce the noise voltage at the expense of an increase in input noise current and low frequency 1/f

A Handle on Input Noise (Continued)

noise, which are not a problem in low input impedance, wideband amplifiers. The typical effect on noise vs input stage current is illustrated in *Figure 12*.



$\frac{e_{OUT}}{e_{IN}} = 100$

f_O = 250 kHz

Time delay = 636 ns

for f ≤ 250 kHz

FIGURE 10. A Fourth Order, 250 kHz Bessel Filter for Data Recovery Systems. The Filtering Function is Done with a Single Package.

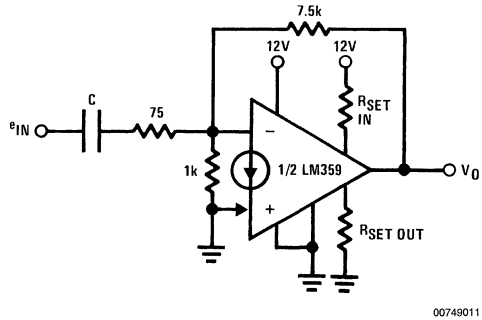
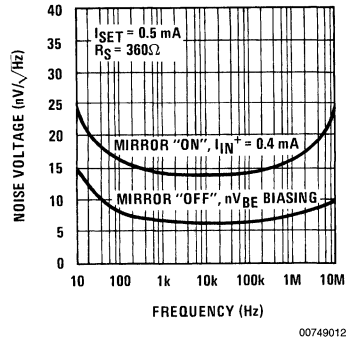
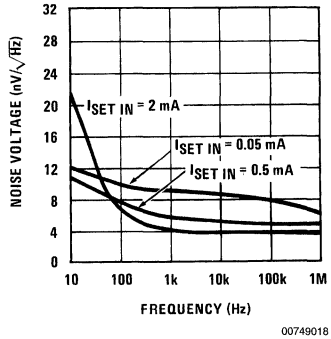


FIGURE 11. nV_{BE} Biasing Can Reduce Input Noise Voltage

A Handle on Input Noise (Continued)



a) Effect of "Shutting Off" the Input Mirror



b) Noise Performance of *Figure 11*

FIGURE 12. Programmability Provides a Handle on Input Noise

Making a Fast JFET Input Op Amp

The current mirror input stage of the LM359 can be used as an active load for a differential JFET stage to form a super fast op amp (*Figure 13*). This circuit combines the high frequency performance and programmability of the LM359 with the high input impedance and low bias currents of a discrete JFET input stage. External compensation of the LM359 is generally required to accommodate any additional phase shift of the input stage, and the "pole-splitting" configuration shown works quite well. The speed performance is shown in *Table 4*. Note that this op amp should be mainly used for very high speed, single supply AC coupled circuits. This is because the op amp DC input offset voltage depends mainly on the matching of 2 discrete JFETs.

Making a Fast JFET Input Op Amp

(Continued)

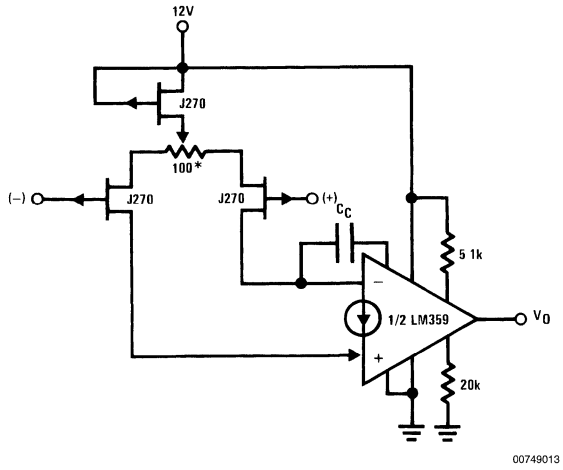
TABLE 4. Typical Amplifier Performance

A_V	BW	Sr	C_C
1	40 MHz	60 V/µs	51 pF
10	24 MHz	130 V/µs	5 pF
100	4 5 MHz	150 V/µs	2 pF

A High Common-Mode Input Voltage Difference Amplifier

An inherent feature of a current differencing input stage is that the voltages from which the input currents are derived are limited only by the maximum input current (or mirror current) of the amplifier and the size of the input resistors. An application that takes advantage of this is a high common-mode voltage difference amplifier (*Figure 14*). In this circuit, the LM359 will amplify the difference in voltage between inputs V1 and V2, but both inputs can be riding on a common-mode level as high as approximately 250 V_{DC} without exceeding the maximum mirror current of 10 mA.

The addition of resistor R1 in *Figure 14* allows an adjustment of the common-mode rejection ratio by adjusting the inverting input bias current, via the programmable input stage current, $I_{SET\ IN}$. This bias current error is most significant at lower common-mode input voltage levels. By making the bias current directly proportional to the input level, a 20 dB CMRR improvement is possible by adjusting R1 for maximum CMRR at the maximum input common-mode voltage.



*V_{OS} null (V_{OS} is typically < 25 mV)
I_{BIAS} < 50 pA

FIGURE 13. Combining the Norton Amplifier with Discrete P-Channel JFETs to Make a Fast Voltage Mode Op Amp

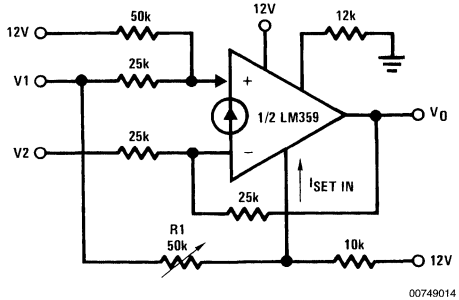


FIGURE 14. A High Input Common-Mode Voltage Difference Amplifier

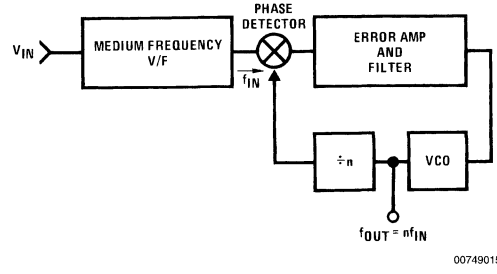
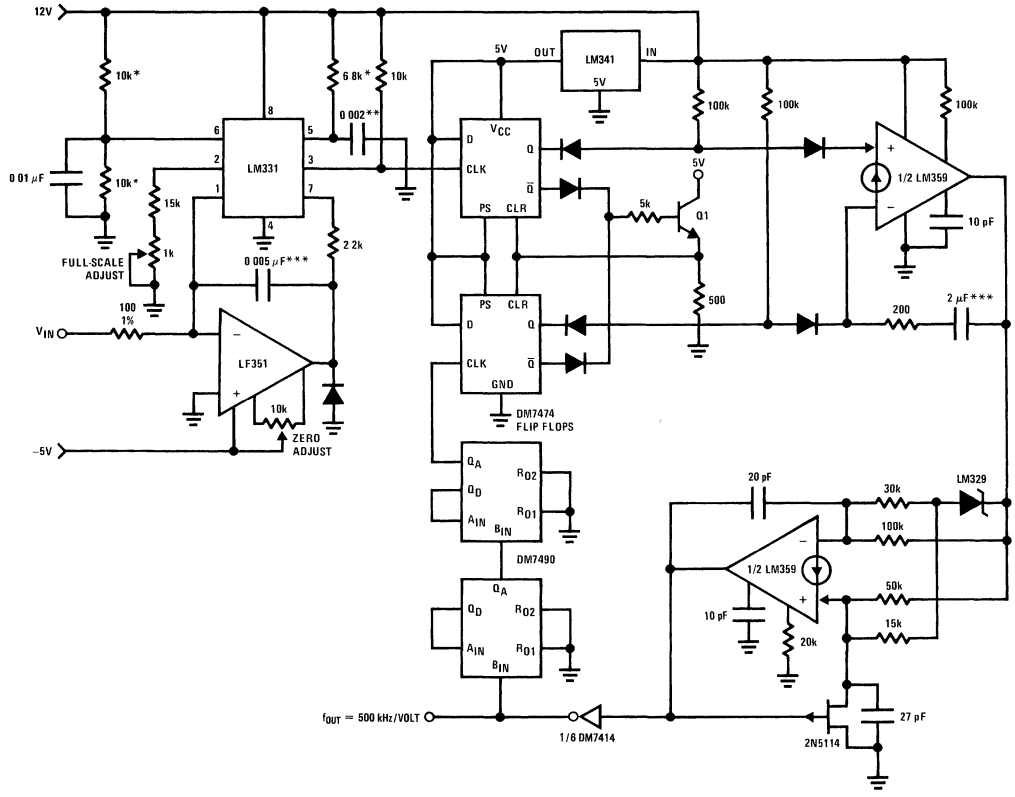


FIGURE 15. Using a Fast PLL to Make a High Frequency, Ultra Linear V/F

A High Common-Mode Input Voltage Difference Amplifier (Continued)



All diodes 1N914
*Metal film, 1%
**Polypropylene
***Mylar
Q1→2N5038
Full-scale adjust made with V_{IN} = −10V
Zero adjust made with V_{IN} = −0 1V

FIGURE 16. Complete Schematic of an Ultra Linear, Two Decade (50 kHz→5 MHz) VCO

Building a Fast and Ultra Linear V/F Converter

Linear and fast voltage-to-frequency (V/F) converters are very difficult to build, especially when standard V/F design techniques are used. A solution to this problem is the use of a fast phase locked loop (PLL) which is driven by a medium frequency and ultra linear V/F IC (the LM331), *Figure 15.* This high frequency operation is obtained via a frequency divider inserted into the loop, and the linearity of the overall circuit closely approximates the linearity of the medium frequency input V/F. The high frequency, quasi linear VCO, and the error amplifier of the PLL are designed by using the 2 sections of the LM359. The output frequency of the VCO, which is also the output of the system, is divided by 100 and is compared with the output of the driving V/F via a digital phase detector. The overall circuit is shown in *Figure 16.* Following a zero and a full-scale adjust, the V/F works well over 2 decades of frequency and its non-linearity is below 0.03%, as shown in *Figure 17.*

Building a Fast and Ultra Linear V/F Converter (Continued)

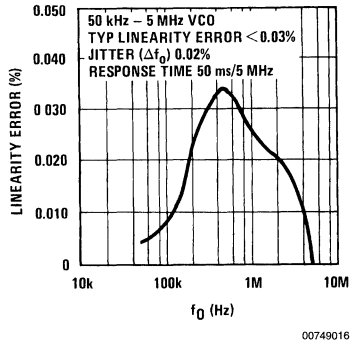


FIGURE 17. Typical Performance

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Fredericksen, T.M.; Howard, W.M., Sleeth, R.S., "The LM3900—A New Current-Differencing Quad of ± Input Amplifiers" AN-72, National Semiconductor Corporation.

Nortronics Design Digest on Digital Recording, Application Factors to Consider for Magnetic Heads, 1976.

Pease, R.A., "New Phase-Locked-Loops Have Advantages as Frequency to Voltage Converters (and more)" AN-210, National Semiconductor Corporation.

Video Transmission Over Twisted Pair Wire

National Semiconductor
Application Note 1240
John Bittner

The circuits in *Figure 1* and *Figure 2* transmit NTSC video signals over twisted pair wire. They were designed and tested for transmitting video on inexpensive CAT-3 twisted pair wire. Even when transmitting on 1000 feet of wire, good quality color video was displayed on a monitor with an NTSC input. Both the transmit and receive circuits use the LMH6643 dual op-amp which has the proper bandwidth and slew rate for this application.

The Video Driver is shown in *Figure 1*. It converts a single-ended input signal from a camera or DVD player into a differential signal that drives the twisted-pair line. The input receives an NTSC composite video signal with $1V_{PP}$ amplitude, and the output drives the twisted-pair with a $2V_{PP}$ differential signal. A 50Ω source resistor is in series with the outputs of both op-amps, matching the Video Driver output resistance to the twisted-pair characteristic impedance.

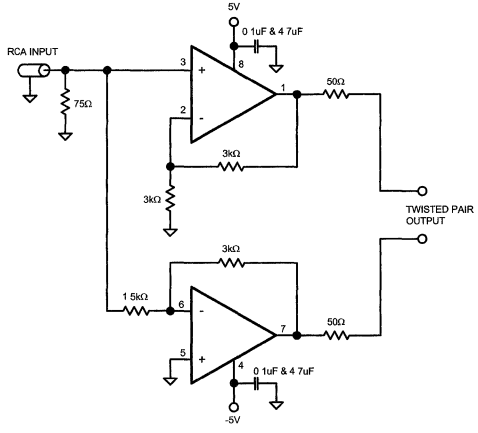


FIGURE 1. Twisted Pair Video Driver

In the receiver circuit of *Figure 2*, R2 is adjusted so that the overall gain of the system is unity (gain of the last op-amp is greater than one to compensate for signal loss). C1 and R1 provide a zero-pole function that compensates for attenuation of higher frequency signals in the twisted pair. The proper values for R1, C1, and R2 can be set by transmitting a $1V_{PP}$ square wave with a frequency of about 300KHz, and adjusting these components for an optimized square wave at the output. This can be done with the following procedure. First, adjust R2 so that the square wave at the receiver output has an amplitude of $1V_{PP}$ (with the output driving a 75Ω load). Next, set C1 and R1 to optimize the risetime/falltime and damping of this square wave. In the demonstration circuit that transmits video on 1000 feet of wire, R1 = 3.9k, C1 = 68pF, and R2 = 3.6k.

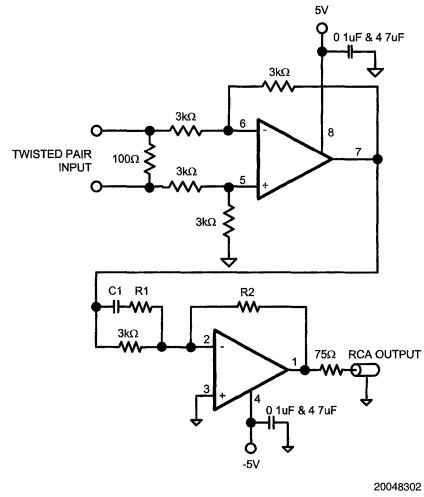


FIGURE 2. Twisted Pair Video Receiver

Figure 3 shows the response of this system when transmitting a square wave. The transitions of the output signal have rise and fall times of 160ns with about 5% of overshoot. Note that 1,000 feet of twisted pair wire delays the input signal by 1.4µs.

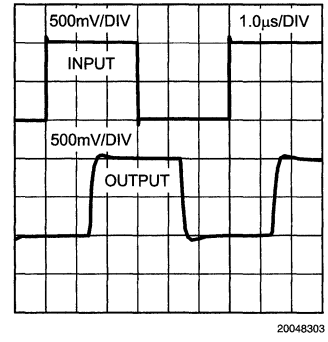


FIGURE 3. System Square Wave Response

Differential gain and phase of the system was measured with an HP3577A Network Analyzer. A $0.55V_{PP}$ sinewave test signal was applied to the input, and the gain and phase were measured at 3.58MHz (NTSC reference frequency). When the DC offset of the test signal changed from 0 to 1V, the gain changed -0.028dB (differential gain), and phase changed 0.23° (differential phase).

Photo-Diode Current-to-Voltage Converters

National Semiconductor
Application Note 1244
Hooman Hashemi

Converting the small output current of a photo-diode transducer to a fast responding voltage is often challenging. Here are some ways to use high-speed Current Feedback and Voltage Feedback op amps to do the job

Current Feedback Amplifier Solution

Current Feedback Amplifiers (CFA) are especially suited to implement this function, as shown in *Figure 1*. With an effective internal buffer on the inverting node of the op amp, the output impedance R_O (internal to U1, not shown) and the photo-diode's output capacitance C_{IN} (typically 10-200pF) introduce a zero in the noise gain at approximately $1/2\pi \times (R_O \times C_{IN})$. In comparison, the zero produced by a Voltage Feedback op amp in a similar configuration $[1/2\pi \times (R_{IN}||R_F||R_{BIAS}) \times C_{IN}]$ tends to be much lower in frequency and more troublesome. This being the case, C_{IN} has less of an effect on reduction of the converter bandwidth, and achieving stability is easier when using a CFA.

If C_{IN} is sufficiently large, the closed loop phase shift will approach – 180° at the cross-over frequency (where open loop transimpedance gain crosses the noise gain function). As with Voltage Feedback Amplifiers, the closed loop amplifier can be compensated by adding a small capacitor (C_F) across R_F. In the case of *Figure 1*, using the CLC450 CFA, C_F was experimentally determined to be around 2pF for about 10% overshoot in the step response. C_F improves stability by counteracting the effect of the zero discussed in the paragraph above by introducing a low frequency pole $(1/2\pi \times R_F \times C_F)$ and an inconsequential zero $(1/2\pi \times R_O \times C_F)$.

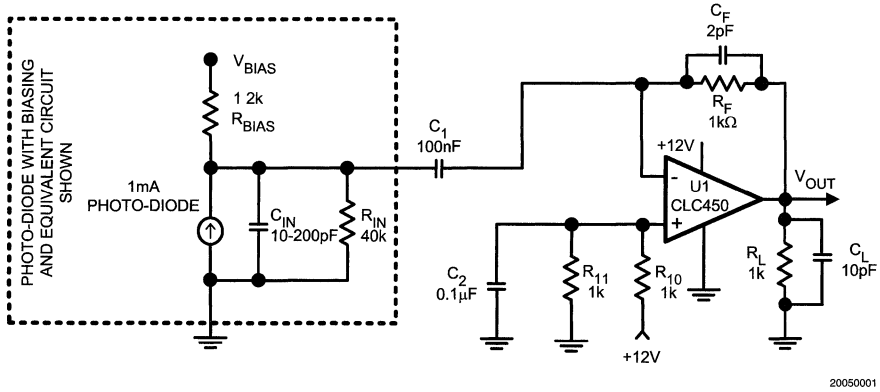


FIGURE 1. Single-Supply Photo-Diode Amplifier Using CLC450 Current-Feedback Amplifier

It is possible to change the required 2pF compensation capacitor to a more practical value, by adding R_A and R_B in a voltage divider, as shown in *Figure 2* The new value of C'_f is $(1+R_B/R_A) \times C_F$. This relationship holds true as long as $R_B << R_F$.

For this example, select $R_A = 50\Omega$, and $R_B = 500\Omega$. Therefore, $C'_f = (1+500/50)$ x2pF = ~22pF which is a much more practical component value. This value needs to be "fine tuned" in the real application for proper step response.

Current Feedback Amplifier Solution (Continued)

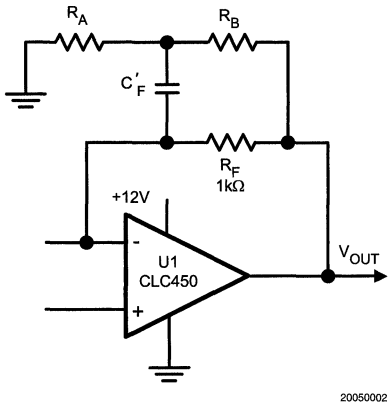


FIGURE 2. R_A -R_B Resistor Divider Allows Use of Practical Value for C'$_f$

Voltage Feedback Amplifier Solution

It's more difficult to design a good current-to-voltage converter using a Voltage Feedback Amplifier (VFA). As discussed above, phase shift caused by photo-diode capacitance is often a source of instability. Furthermore, wide bandwidth usually comes at the expense of supply currents and higher supply voltage. However, the new LMH6642 high-speed low-voltage VFA op amp has excellent performance in a transimpedance gain block, as shown in *Figure 3*. This device can operate down to 2.7V single supply and its −3dB BW (A_V = +1) is more than 100MHz (with a supply current of only 2.7mA)! Because of the "Dielectric Isolation" process this device is based on, the traditional supply voltage vs. speed trade-off has been alleviated to a great extent allowing low power consumption and operation at lower supply voltages. In addition, the device has Rail-to-Rail output swing capability to maximize the output swing, and is capable of driving ±50mA into the load.

With 5V single supply, the device common mode voltage is shifted to near half-supply using R_{10}-R_{11} as a voltage divider from V_{CC}. The common-base transistor stage (Q1) isolates the photo-diode's capacitance from the inverting terminal, allowing wider bandwidth and easing the compensation required. Note that the collector of Q1 does not have any voltage swing, so the Miller effect is minimized. The diode on the base of Q1 is for temperature compensation of its bias point. Q1 bias current was set to be large enough to handle the peak-to-peak photo-diode excitation, yet not too large as to shift the U1 output too far from mid-supply. The overall circuit draws about 4.5mA from the +5V power supply and achieves about 35MHz of closed loop bandwidth @1V_{PP}. *Figure 4* shows the output large signal step response. C_F can be increased to reduce the overshoot, at the expense of bandwidth.

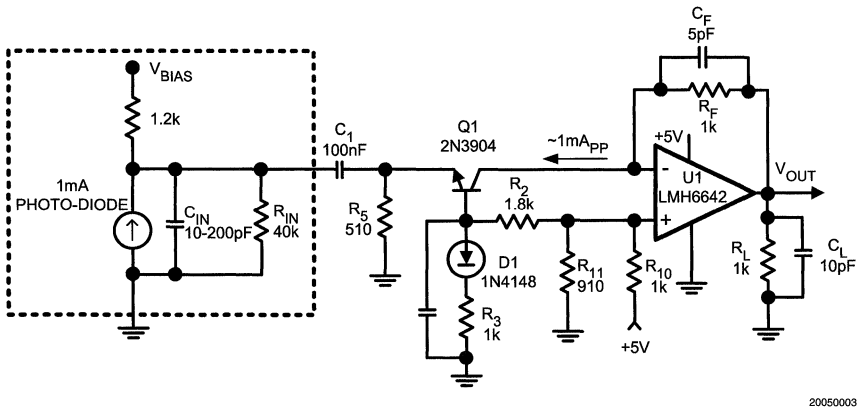


FIGURE 3. Single-Supply Photo-Diode Amplifier Using LMH6642 Voltage-Feedback Op Amp

Voltage Feedback Amplifier Solution (Continued)

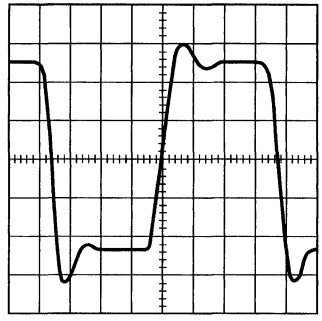


FIGURE 4. Output Step Response 20ns/div, 0.2V/div

Current Feedback Op Amp Applications Circuit Guide

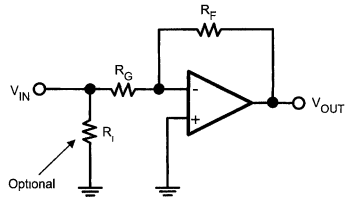
National Semiconductor
OA-07
David Potson

Introduction

No two high-speed application are the same – or at least it seems that way. Nonetheless, while every system has its particular requirements, many of the design techniques are common among different designs. This application note illustrates design techniques utilizing current-feedback op amps and the practical circuits where they are used. The circuits should work well with any Comlinear op amp if appropriate adjustments are made for different feedback resistance values.

Inverting Gain

As with voltage-feedback op amps, the ratio of the feedback resistor to the gain-setting resistor determines the voltage gain in current-feedback op amp circuits. With current feedback, however, dynamic performance is largely independent of the voltage gain. (See application note AN300-1 for a technical discussion of current-feedback.) Also, the optimum feedback resistor value for a current-feedback op amp is indicated in the datasheet

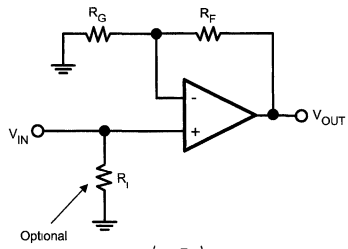


$$V_{OUT} = \frac{R_F}{R_G} V_{IN}$$

For input impedance of 50Ω, select $R_I \parallel R_G$ equal to 50Ω

01278101

Non-Inverting Gain



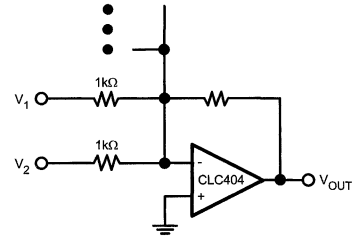
$$V_{OUT} = \left(1 + \frac{R_F}{R_G}\right) V_{IN}$$

R_I set the input impedance

01278102

Summing Amplifier

Current-feedback op amps are the natural choice in summing applications since the bandwidth and other key specs are relatively unaffected by high gain setting. (The parallel combination off all the input resistors yields a small effective gain-setting resistance and hence a large effective gain setting.)

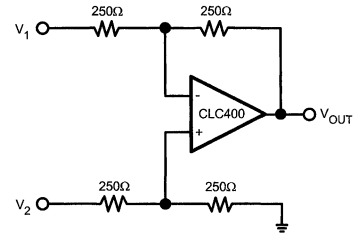


$$V_{OUT} = -\left(V_1 + V_2 \cdots\right)$$

01278103

Differential Amplifier

Be sure to obey common-mode input voltage limits shown in the op amp datasheet. If large, saturating input signals are expected, use an overdrive-protected op amp and appropriate protection circuitry.

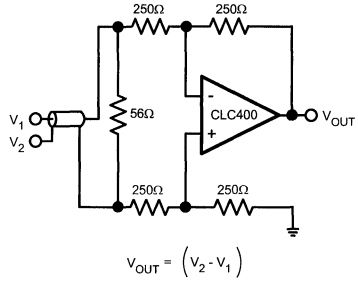


$$V_{OUT} = \left(V_2 - V_1\right)$$

01278104

Differential Line Receiver

This circuit provides good common mode rejection and 50Ω termination for signals which need to be transmitted through coaxial lines.



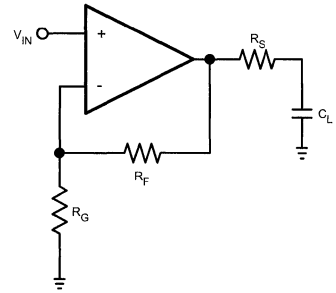
$$V_{OUT} = \left(V_2 - V_1\right)$$

Differential input resistance is 50Ω

01278105

Driving Capacitive Loads

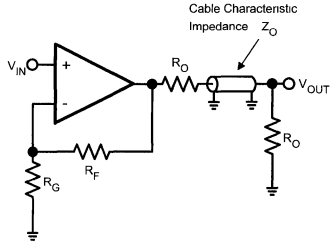
The damping resistor, R_S, reduces pulse-response overshoot and frequency-response peaking caused by the load capacitance. The value of R_S may be found on some of the op amp datasheet or may be found experimentally.



01278108

Coaxial Cable Driver

Proper transmission line driving techniques are important when high-speed signals have to travel more than a few inches. The back-matching and terminating resistor, R_O, are chosen to match the characteristic impedance of the coaxial line. If the load is well-matched to the transmission line impedance, the back-matching resistor may be omitted for greater voltage swing. (Remember that back matching creates a voltage divider which attenuates the output signal by 50%.)

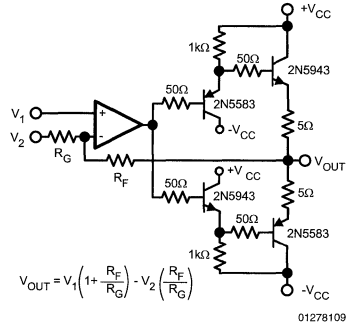


$$R_O = Z_O$$

01278106

Output Current Booster

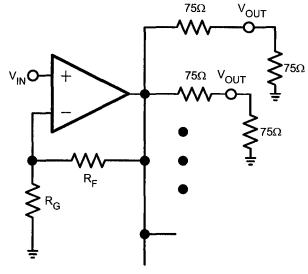
This circuits provides up to 400mA of output current. Since the output buffer circuit introduces additional phase lag, the feedback resistor, R_F, may have to be increased above the datasheet recommendation to decrease loop gain and thus improve stability. The gain-setting resistor, R_G, is then chosen for the desired gain.



$$V_{OUT} = V_1\left(1 + \frac{R_F}{R_G}\right) - V_2\left(\frac{R_F}{R_G}\right)$$

01278109

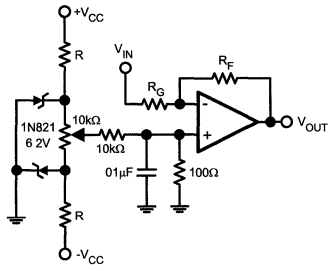
Distribution Amplifier



01278107

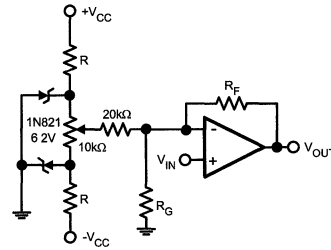
Simple Offset Adjustment

The Zener diode biasing resistor, R, should be chosen to provide a diode current of 7.5mA.



Inverting

01278110

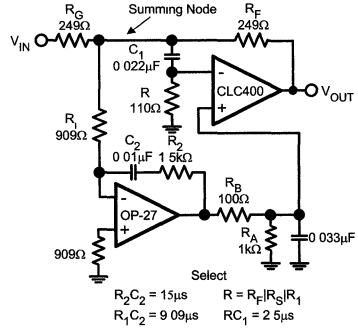


Non-Inverting

01278111

Composite Amplifier for Low Offset and Drift (#1)

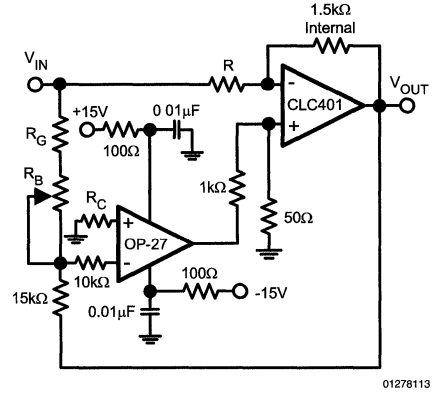
This composite circuit provides both high speed and good DC performance and unlike most composite circuits, it provides good settling performance (17ns to 0.1%). In operation, the OP-27 op amp drives its output such that the summing node is driven to 0V(which is the normal case for an inverting gain circuits). Thus, the circuit output takes on the high performance DC characteristics of the OP-27. At high frequencies, the high-speed op amp takes over to provide good AC performance.



01278112

Composite Amplifier for Low Offset and Drift (#2)

This composite circuit is useful with those products which have the feedback resistor connected internally to both the input and output. R_B is adjusted for minimum output voltage at the OP-27 when V_{OUT} is a 70kHz square wave of $10V_{PP}$ centered at 0V.



01278113

$$V_{OUT} = -\left(\frac{1500}{R}\right) V_{IN}$$

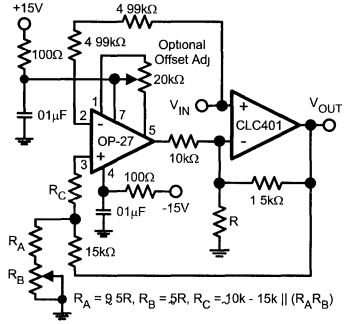
$R_A \cong 9\ 5R$

$R_B \cong 0\ 5R$

$R_C \cong 10K - 15K \parallel (R_A + R_B)$

Non-Inverting Composite Amplifier

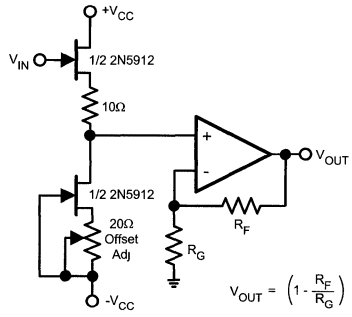
As with the previous circuit, R_B is chosen for minimum output voltage at the OP-27 when V_{OUT} is a 70kHZ square wave of $10V_{PP}$ center at 0V.



01278115

FET-Input Circuit

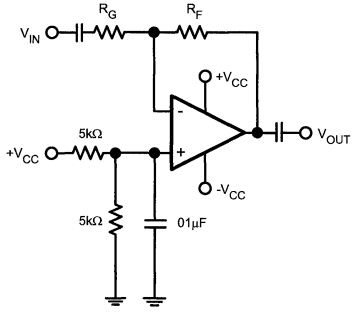
A FET-input circuit is useful when a greater input impedance is desired or when bias currents or noise current need to be reduced.



01278116

AC-coupled Amplifier (with Single-Supply Biasing)

The voltage divider circuit at the non-inverting input biases the op amp input and output at the supply midpoint. For those op amps having a bias pin, these pins should also connect to the supply midpoint bias circuit.

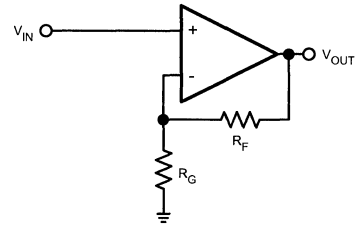


01278117

Reducing Bandwidth

Bandwidth and loop stability is controlled by R_F. Increasing R_F reduces bandwidth according to the approximate relationship:

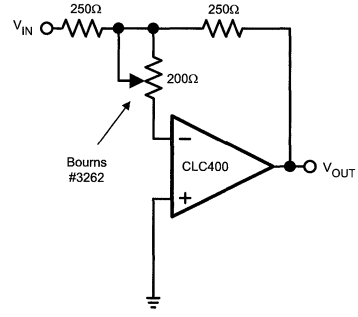
$$\frac{BW_2}{BW_1} \cong \frac{R_{F1}}{R_{F2}}$$



01278118

Adjustable Bandwidth

By increasing the inverting input impedance (which is normally very low) of a current feedback op amp, the bandwidth of the op amp can be reduced. The bandwidth of the circuit below can be varied over a range of 60MHz to 160MHz.



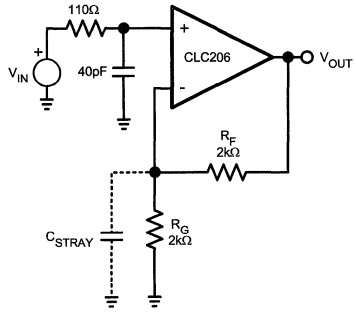
01278119

Reducing Frequency-Response Peaking

(due to stray capacitance in parallel with R_G)

The low-pass filter at the non-inverting input cancels the frequency-response zero caused by C_{STRAY}. At low non-inverting gains, the CLC231 or CLC400 will provide a flatter frequency response without the need for the low-pass filter (because they can be used with lower feedback resistor values).

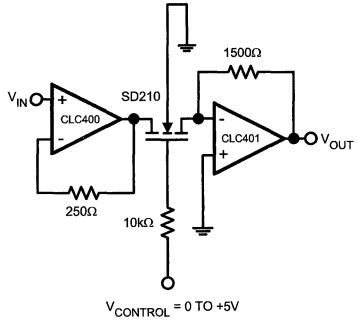
Reducing Frequency-Response Peaking (Continued)



01278120

Adjustable Gain Using a FET

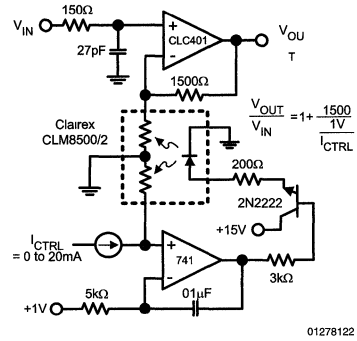
This circuit provides a 26dB adjustment range and a gain flatness of 1dB from DC to 50MHz. An SD210 FET provides low on-resistance with minimal capacitive loading.



01278121

Adjustable Gain Using a Photoresistor

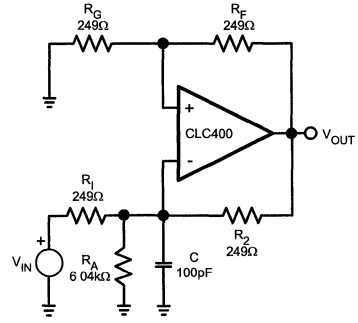
This circuit provides a 12dB adjustment range and a gain flatness of 1dB from DC to 20MHz. The 741 circuit improves temperature stability and repeatability of the photoresistor circuit.



01278122

Integrator (#1)

With current-feedback op amps, it is importance to keep large capacitance values out of the inverting feedback loop in order to maintain stability.



01278123

For stable operation,

$$\frac{R_2}{R_1 \| R_A} \geq \frac{R_F}{R_G}$$

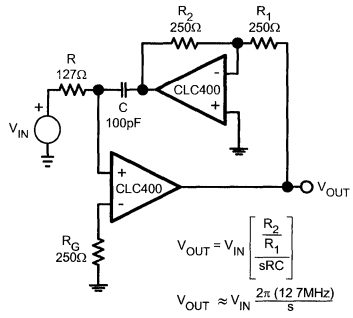
All resistors are 1%

$$V_{OUT} = V_{IN}\left[\frac{1 + \frac{R_F}{R_G}}{sR_1C}\right]$$

$$V_{OUT} \backsim V_{IN}\,\frac{2\pi\,(12\,8MHz)}{s}$$

Integrator (#2)

This integrator provides higher DC gain than #1. For values shown, the DC gain is 55dB. Higher values can be obtained by reducing R_G, however, the ratio of R_G to R_1 should remain constant for adequate loop stability. Much of the output noise is directly proportional to R_1 so that the higher DC gain is obtained at the expense of higher noise. This circuit does not have the stability problem that is related to resistor matching as does integrator #1.



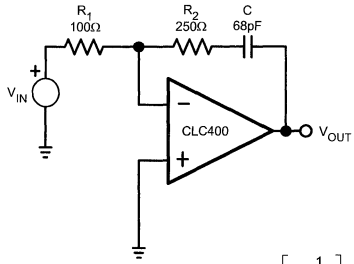
$$V_{OUT} = V_{IN}\left[\frac{\frac{R_2}{R_1}}{sRC}\right]$$

$$V_{OUT} \approx V_{IN}\frac{2\pi\,(12.7\text{MHz})}{s}$$

01278125

Integrator with Zero

In this circuit, feedback capacitance is acceptable because the op amp relies upon the value of the feedback resistor for stability.



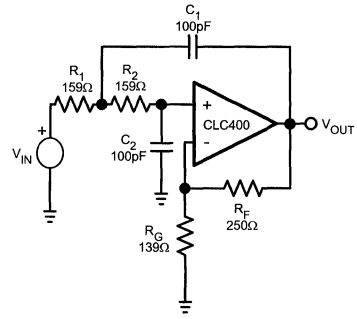
$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_2}{R_1}\left[\frac{s + \frac{1}{R_2C}}{s}\right]$$

01278126

Active Filter Circuits

The following five circuits illustrate how current feedback op amps provide high-performance active filter functions. The "KRC" realization is used (see references at the end of the app note) since it does not require reactive elements in the (negative) feedback path, which would compromise stability. When the filter cutoff frequency is small relative to the amplifier bandwidth, the transfer functions shown will provide good accuracy. However, as with any active filter circuit, the group delay through the op amp becomes significant for cutoff frequencies greater than about 10% of the op amp bandwidth. For such designs, computer analysis tools and an iterative design approach is helpful.

Low-Pass Filter (10MHz, Q = 5)



01278127

$$\frac{V_{OUT}}{V_{IN}} = \frac{s\frac{K_0}{R_1C_1}}{s^2 + s\left(\frac{1}{R_1C_1} + \frac{1}{R_3C_2} + \frac{1}{R_3C_1} + \frac{1-K_0}{R_2C_1}\right) + \frac{R_1+R_2}{R_1R_2R_3C_1C_2}}$$

$$K_0 = 1 + \frac{R_F}{R_G} \qquad \omega_0^2 = \frac{1}{R_1R_2C_1C_2}$$

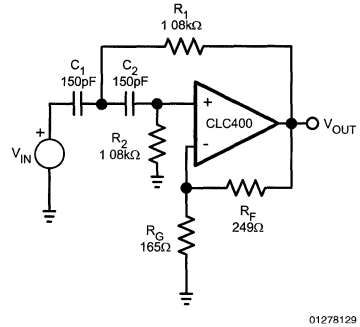
$$Q = \frac{1}{\sqrt{\frac{R_1C_2}{R_2C_1}} + \sqrt{\frac{R_2C_2}{R_1C_1}} + (1-K_0)\sqrt{\frac{R_1C_1}{R_2C_2}}}$$

$R_1 = R_3 = R, \quad C_1 = C_2 = C$

$$\omega_0 = \frac{\sqrt{2}}{RC}$$

$$Q = \frac{\sqrt{2}}{4-K_0}$$

High-Pass Filter (1MHz, Q = 2)



01278129

$$\frac{V_{OUT}}{V_{IN}} = \frac{K_0s^2}{s^2 + s\left(\frac{1}{R_2}\left(\frac{1}{C_1} + \frac{1}{C_2}\right) + \frac{1-K_0}{R_1C_1}\right) + \frac{1}{R_1R_2C_1C_2}}$$

$$K_0 = 1 + \frac{R_F}{R_G} \qquad \omega_0^2 = \frac{1}{R_1R_2C_1C_2}$$

$$Q = \frac{1}{\sqrt{\frac{R_1}{R_2}}\left(\sqrt{\frac{C_2}{C_1}} + \sqrt{\frac{C_1}{C_2}}\right) + \sqrt{\frac{R_2C_2}{R_1C_1}}(1-K_0)}$$

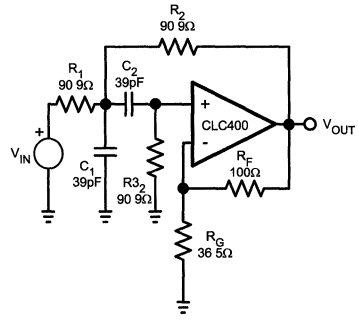
$R_1 = R_3 = R, \quad C_1 = C_2 = C$

$$\omega_0 = \frac{1}{RC}$$

$$Q = \frac{1}{3-K_0}$$

Band-Pass Filter (40MHz, Q = 4)

The component values shown are "predistorted" from the nominal design values to account for the 1.6ns op amp group delay, which is significant relative to the filter cutoff frequency.



01278131

$$\frac{V_{OUT}}{V_{IN}} = \frac{s\frac{K_0}{R_1C_1}}{s^2 + s\left(\frac{1}{R_1C_1} + \frac{1}{R_3C_2} + \frac{1}{R_3C_1} + \frac{1-K_0}{R_2C_1}\right) + \frac{R_1+R_2}{R_1R_2R_3C_1C_2}}$$

$$K_0 = 1 + \frac{R_F}{R_G} \qquad \omega_0^2 = \frac{R_1+R_2}{R_1R_2R_3C_1C_2}$$

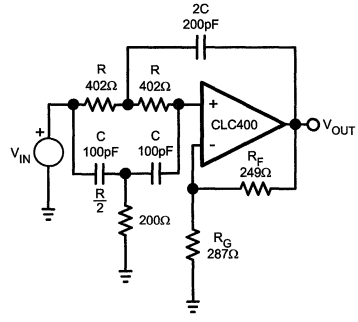
$$Q = \frac{\sqrt{\frac{R_2C_1}{R_1R_3C_2}\,(R1+R2)}}{1 + \frac{R_1}{R_2} + \frac{R_2}{R_3}\left(1 + \frac{C_1}{C_2}\right) - K_0}$$

$R_1 = R_3 = R, \quad C_1 = C_2 = C$

$$\omega_0 = \frac{\sqrt{2}}{RC}$$

$$Q = \frac{\sqrt{2}}{4 - K_0}$$

Band-Stop Filter (4MHz, Q = 4)



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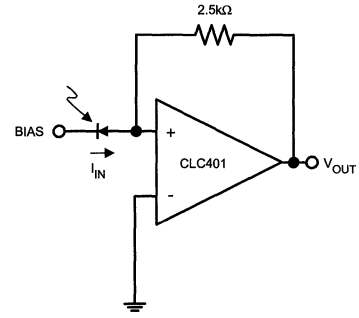
$$\frac{V_{OUT}}{V_{IN}} = \frac{K_0\left(s^2 + \frac{1}{R^2C^2}\right)}{s^2 + 2\frac{s}{RC}\left(2 - K_0\right) + \frac{1}{R^2C^2}}$$

$$K_0 = 1 + \frac{R_F}{R_G} \qquad \omega_{0POLE}^2 = \omega_{0ZERO}^2 = \frac{1}{R^2C^2}$$

$$Q_{POLE} = \frac{1}{2(2 - K_0)}$$

Photodiode Amplifier

The circuit below provides a transimpedance gain of −2.5kΩ to convert the protodiode current into a voltage.



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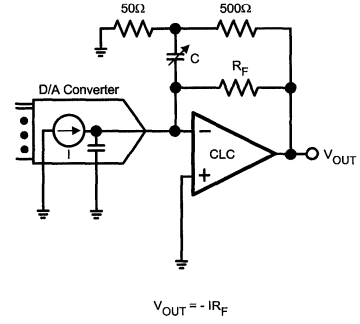
D/A Converted Buffer Amplifier

Most high-speed, current-output D/A converters provide the best performance when driving little or no load impedance. The circuit below meets this requirement while also providing a transimpedance gain which converts the D/A output current into a Voltage. The variable capacitor in the feedback loop should be adjusted for desired pulse response to compensate for the D/A output capacitance, which otherwise caused frequency-response peaking or instability. The 50Ω and 500Ω resistors reduce the effective value of the feedback capacitance so that a reasonable value capacitor may be used.



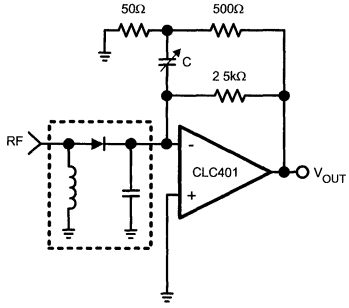
$$V_{OUT} = -IR_F$$

01278136

For example, with the CLC401, R_F = 2.5kΩ and a D/A output capacitance of 20pF, C ≅ 5pF.

Tunnel Diode Detector Amplifier

See the D/A converter buffer circuit for circuit highlights.



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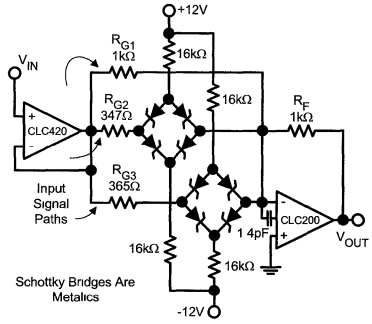
Non-Linear Transfer Functions

Current-feedback op amps are particularly useful in non-linear transfer function circuits. Since bandwidth and other key specifications are independent of gain-the dynamic performance is relatively independent of signal level.

In analyzing the circuit, it is useful to identify the three input signal paths that contribute to the output voltage (the 1kΩ resistor and the two diode bridges). Each of these paths terminates at the inverting input–a point that is at virtual ground. Due to feedback, the current through the feedback resistor is equal to the sum of these input currents. The output voltage, therefore, is the product of the feedback resistor and the sum of the input current.

The individual input currents are equal to the input voltage divided by the respective gain-setting resistor. However, in the signal paths containing the bridges, the current follows this linear relationship until it limits at 12V/16kΩ. This is what leads to the non-linear gain. A more accurate analysis requires that the diode bulk and dynamic resistance be included.



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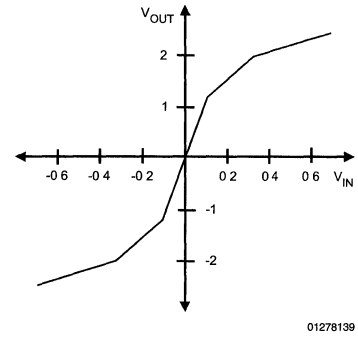

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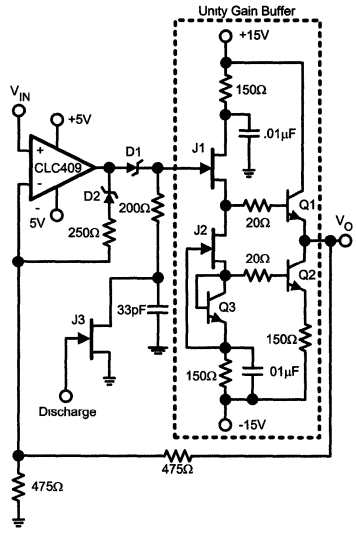
Peak Detector

The circuit shown in the next column can capture 50ns pulses over a 20mV to 1.5V input range. The circuit consists of three basic blocks: the op amp and diodes, the storage capacitor and discharge circuit, and the unity-gain buffer. The peak detecting action is caused by the conduction or non-conduction of the two diodes in the feedback loop.

When $V_{OUT} > V_{IN}$, the op amp output swings in the negative direction until D2 conducts and the feedback path is completed and the op amp does not saturate.

When $V_{OUT} > V_{IN}$, the op amp swings in the positive direction causing D1 to conduct and the storage capacitor voltage to be charge through the 200Ω isolating resistor. This action continues until $V_{OUT} > V_{IN}$ and equilibrium is established.

Peak Detector (Continued)



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50ns pulses over a
20mV to 1.5V input range.

D1, 2	1N5711
Q1, 2, 3	MPSH10
J1, 2	2N5911
J3	2N4391

References:

A. Budak, Passive and *Active Network Analysis and Synthesis*, Houghton Mifflin Company, Boston, 1974.

IEEE Transactions on Circuits and Systems, Volume CAS-27, "Optimum Configurations for Single Amplifier Biquadratic Filters," number 12, pages 1155-1163, December 1980.

Note: The circuits included in this application note have been tested with National Semiconductor parts that may have been obsoleted and/or replaced with newer products. Please refer to the CLC to LMH conversion table to find the appropriate replacement part for the obsolete device.

A Tutorial on Applying Op Amps to RF Applications

National Semiconductor
OA-11
David Potson

With operating frequencies exceeding 300MHz, National's line of monolithic and hybrid current feedback operational amplifiers have become an attractive option for the RF (and IF) design engineer Typical operational amplifier specifications do not, however, include many of the common specifications familiar to RF engineers. To help the designer exploit the many advantages these amplifiers can offer, this application note will define the RF specifications of most interest to designers, detail what determines each of these particular performance characteristics for National's current feedback op amps, and, where possible, discuss performance optimization techniques. To apply op amps to RF applications, questions in three general areas must be addressed:

1. Setting the op amp's operating conditions
2. Small signal AC performance in an RF context
3. Typical limits to RF amplifier dynamic range applied to op amps

Wherever possible, tested performance using the CLC404 will be used to demonstrate performance. The CLC404 is a ±5V power supply monolithic amplifier intended for use over a voltage gain range of ±1 to ±10. At its optimum gain of +6, the CLC404 offers a DC to 175MHz frequency range while delivering 12dBm power into a 50Ω load while dissipating only 110mΩ quiescent power. National offers a wide range of additional monolithic op amps, as well as higher supply voltage (and hence higher power output) hybrid amplifiers. The best amplifier for a particular application will depend upon the desired gain, power output, frequency range and dynamic range.

Operation of National's Current Feedback Op Amps

The current feedback op amp, developed by National Semiconductor Corporation, provides a very wideband, DC coupled op amp that has the distinct advantage of being relatively gain-bandwidth independent. As with all op amps using a closed loop negative feedback structure, the frequency response for the National op amps is set by the loop gain characteristics. The key development of the National amplifiers is to de-couple the signal gain from the loop gain part of the transfer function.

This de-coupling allows the desired signal gain to be changed without radically impacting the frequency response. If compared to voltage feedback amplifiers, which are constrained to a gain-bandwidth product operation, the current feedback topology offers truly impressive equivalent gain-bandwidth products (e.g. the CLC401 at a gain of 20 yields a flat response with a -3dB bandwidth of 150MHz. To match this, a voltage feedback op amp would require 20*150MHz = 3GHz gain bandwidth product). Please refer to National application note OA-13 for a description of the current feedback op amp topology and transfer function.

One of the big changes in going from a classical RF amplifier to using an op amp is the exceptional flexibility offered by the op amps The designer is now charged with setting up the proper operating conditions for the op amp, defining the gain, and determining the I/O impedances with external components. Op amps allow the designer the option of running either a non-inverting or an inverting gain path. For RF applications, the 180° phase shift provided by the inverting mode is often incidental. There are, however, advantages and disadvantages to each mode, depending on the desired performance, and both will be considered at each stage in this development.

Most of this discussion on applying op amps to RF applications applies to any type of op amp. The unique advantages of the current feedback topology are its higher frequency capabilities and its intrinsically low distortion at low operating currents. If not specifically stated as being unique to the current feedback topology, the items considered here apply equally as well to a voltage feedback op amp.

As a starting point for describing op amps for RF applications, it is useful to summarize some of the standard operating assumptions for typical RF amplifiers. Although there are certainly exceptions to the typical conditions shown here, RF amplifiers generally have:

1. AC coupled input and output. A DC voltage generally has little meaning in RF applications.
2. Input and output impedances nominally set to 50Ω (AC) over the frequency range of operation. This is seldom a physical 50Ω resister, but rather a combination of active element I/O impedances along with passive matching networks.
3. Fixed signal gain operations over a certain band of frequencies. Any particular RF amp is purchased to provide a particular gain and is not user adjustable. A two decade range of operating frequencies seems typical.
4. Single power supply operation. Since both input and output are AC coupled, bipolar power supplies, balanced around ground, are not needed The DC bias point is maintained internally with minimal user adjustment possible.

Operation of National's Current Feedback Op Amps (Continued)

Figure 1 shows a typical RF amplifier connection, while *Figure 2* and *Figure 3* show an ideal op amp, either current or voltage feedback, connected for non-inverting and inverting gains, respectively.

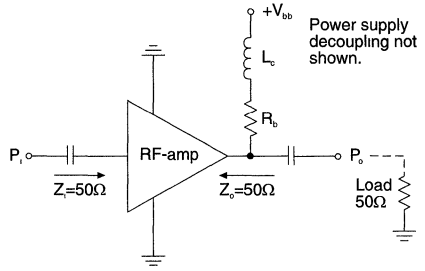

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FIGURE 1. Typical RF Amplifier Connection

For the RF amplifier, both input and output are AC coupled, while a single power supply biases the part through R_b. L_C chokes off the AC output signal from seeing the power supply as a load. The RF amplifier signal gain is specified with the output driving a 50Ω load and is defined as 10*log (power gain)

The two ideal op amp circuits assume that the source is coming from a ground referenced, zero impedance voltage source while their outputs are intended to act as ideal (zero ohm output impedance) voltage sources to a ground referenced load. The non-inverting configuration ideally presents an infinite input impedance, a zero ohm output impedance, and a voltage gain, as shown in *Figure 2*, from the plus input to the output pin.

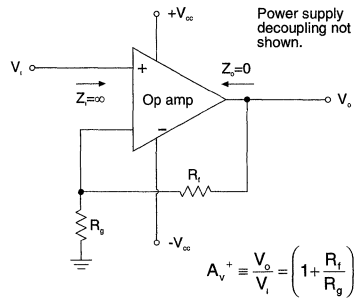

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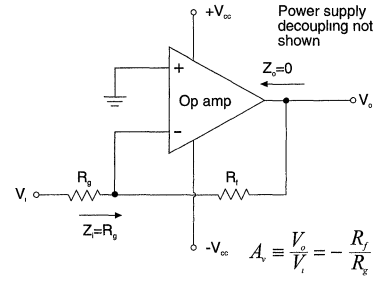
FIGURE 2. Ideal Non-Inverting Op Amp

The ideal inverting op amp differs in several respects from the non-inverting. The output voltage is ideally 180° out of phase from the input, which accounts for the signal inversion. The op amp's (-) input ideally presents a virtual ground, while drawing minimal current, for either voltage or current feedback op amps. This leaves R_g as the ideal input impedance seen by the source, while the voltage gain from the input of R_g to the output is simply $-R_f/R_g$. This signal inversion is usually of no consequence in an RF application, and most of this discussion will deal only with the magnitude of the inverting gain.



01501803

FIGURE 3. Ideal Inverting Op Amp

When using op amps as RF amplifiers, we must first satisfy the I/O impedance matching requirements, recast the gain from a voltage gain to a power gain (in dB), and possibly configure for operation from a single power supply. *Figure 4* and *Figure 5* show the op amps of *Figure 2* and *Figure 3* set up to provide I/O impedance matching with the resulting power gain equations, but still using bipolar supplies. The bipolar power supplies allow operation to be maintained all the way down to DC. Single supply operation is possible and will be considered next

For the non-inverting case, setting Z_i = 50Ω simply requires a 50Ω termination resistor to ground on the non-inverting input, R_T . Getting Z_o = 50Ω simply requires a series 50Ω resistor in the output, R_O.

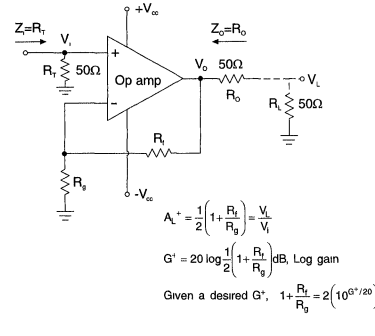


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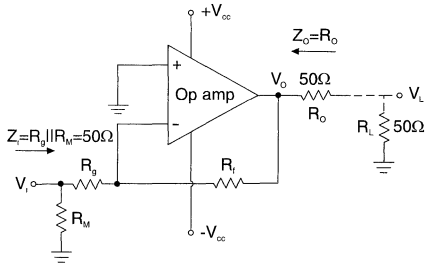
FIGURE 4. Non-Inverting Op Amp Configured for RF Application

For the inverting mode of op amp operation, the (+) input is ground referenced, while the signal channel input impedance becomes the parallel combination of R_g and R_M. As OA-13 describes, the current feedback topology depends on the value of the feedback resistor to determine the frequency response. With each particular op amp calling out a particu-

Operation of National's Current Feedback Op Amps (Continued)

lar optimum R_f , R_g can then be used to set the gain and R_M, along with R_g, will set the input impedance. Setting R_g to yield the desired gain and then setting R_M to satisfy $Z_I = 50\Omega$ will work until the required $R_g < 50\Omega$. Having fixed R_f to satisfy the amplifier's stability requirements, going to higher and higher inverting gains will eventually yield R_g's $< 50\Omega$. Non-inverting operation should be used if this limitation is reached R_f can, however, be increased beyond the recommended value for a current feedback op amp in order to allow an $R_g = 50$ at higher gains, but only at the expense of decreasing bandwidth.



$$A_L^- = -\frac{1}{2}\frac{R_f}{R_g} = \frac{V_L}{V_I}\text{; neglecting the signal inversion}$$

$$G^- = 20\log\left(\frac{1}{2}\frac{R_f}{R_g}\right)\text{dB, Log gain}$$

$$\text{Given a desired } G^-,\ \frac{R_f}{R_g} = 2\,(10^{G-/20})$$

01501805

FIGURE 5. Inverting Op Amp Configured for RF Application

Note that for both topologies the gain to the matched load has been cut in half (-6dB), from the earlier ideal case, through the voltage divider action of $R_O = R_L$. It is a simple, but critical, conversion from any description of output voltage swing to and from a power (in dBm) defined at the load. *Figure 6* shows these conversions for a purely sinusoidal signal. Basically, for whatever initial description of voltage swing given, we need to convert that into an RMS voltage, square it and divide by the load ($R_L = 50\Omega$ normally) to get the absolute power in watts. This is then divided by 0.001 to reference that power to 1mW and 10*log of that expression is taken to yield the power in dBm.

$$P_o = 10\log\frac{\left(\frac{V_{L_{pp}}}{2\sqrt{2}}\right)^2}{50\Omega\,(1\text{mW})} = 20\log(8(50\,\Omega)(0.001))$$
$$= 20\log V_{L_{pp}} + 4\,\text{dBm}$$

Conversely, for a given P_o (in dBm)

$$V_{L_{pp}} = 10^{(P_o - 4)/20}$$

Peak – Peak voltage swing at load

$$V_{O_{pp}} = 2^{*}10^{(P_o - 4)/20}$$

Peak – Peak voltage swing at output pin

01501806

FIGURE 6. Converting Between Voltage Swings and Power

Every op amp has a specified maximum output voltage swing that is generally shown as a peak excursion from ground. This type of specification, for balanced bipolar power supplies, is really inferring how close the output may come to the supply voltages before non-linear limiting occurs. For AC coupled RF applications, it is always best to hold the output pin DC level centered between the two supply pins in order to provide the maximum output V_{pp} . Application note OA-15 discusses in more detail input and output voltage range considerations.

Most of National's op amps do not require a ground reference for proper operation and can be easily operated from a single supply Generally, all that is required is to keep the DC voltage on the (+) input and the output pin centered between the voltages appearing on the two supply pins. For a single supply operation (with one supply pin held at ground) this translates into the (+) input and V_O being held at V_{cc} /2. For those amplifiers requiring a ground pin, that pin should also be driven with a low source impedance voltage midway between the supply pins.

There are many possible implementations of single power supply op amp operation. *Figure 7* and *Figure 8* show two simple ways to operate non-inverting and inverting op amps as AC coupled RF amplifiers using a single power supply.

In the non-inverting case, the input termination is still DC coupled, while the (+) input bias is set by the two R_b 's to yield V_{cc} /2. R_b should be large enough to limit excessive quiescent current in the bias path, but not so large as to generate excessive DC errors due to the amplifier's input bias current. The gain setting resistor, R_g , is also AC coupled to limit the DC gain to 1. Hence, the (+) input DC

Operation of National's Current Feedback Op Amps (Continued)

bias voltage also appears at the output pin. The output should be AC coupled in both circuits to limit the DC current that would be required if a grounded load were driven.

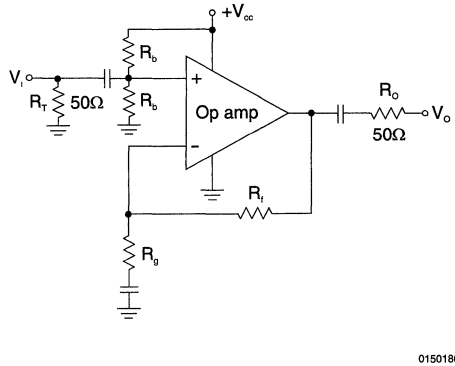


FIGURE 7. Single Supply, Non-Inverting Op Amp Operation

Single Supply, Non-Inverting Op Amp Operation For the single supply inverting amplifier of *Figure 8*, we still require the midpoint reference to be brought in on the (+) input. A de-coupling capacitor on that node is also suggested to decrease the AC source impedance for the non-inverting input noise current. The gain for this non-inverting input reference voltage is again AC coupled to yield a unity DC gain to get $V_{cc}/2$ at the output pin. The inverting input impedance goes from R_M at DC to 50Ω at higher frequencies. R_M, as well as R_T in *Figure 7*, could also be AC coupled to avoid DC loading on the source.

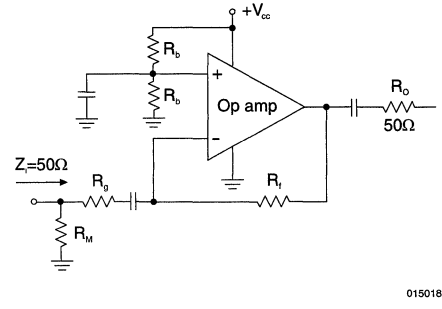


FIGURE 8. Single Supply, Inverting Op Amp Operation

For both of these single supply circuits, we have given up the DC coupling for the signal path. The low frequency limits to operation will now be set by the AC coupling capacitors, along with impedances in each part of the circuit. All of the subsequent discussions assume balanced bipolar supplies, but apply equally as well to single supply operation.

Small Signal AC Performance Characteristics

All of the typical small signal AC parameters specified for RF amplifiers are derived from the S-parameters (reference 1). These are:

Scattering Parameters	RF Amplifier Specification
S_{11} Input reflection	Input VSWR
S_{22} Output reflection	Output VSWR
S_{21} Forward transmission	Amplifier gain and bandwidth
S_{12} Reverse transmission	Reverse isolation

These frequency dependent specifications are measured using a network analyzer and an S-parameter test set. A full 2-port calibration should be performed prior to any device measurements. The HP8753A, used for the measurements reported here, incorporates full 12 term error correction in its 2-port calibration. This basically normalizes all measurement errors due to imperfections in the cabling and test hardware (reference 2).

Figure 9 and *Figure 10* show the two configurations for the CLC404 used in demonstrating the small signal AC performance parameters listed above. In each case, the S-parameter test set places the device into a 50Ω input and output environment. Both configurations achieve a voltage gain of 6 to the output pin and 3 to the 50Ω load. This yields a gain of 20*log(3) = 9.54dB measured by the network analyzer. Recall that one of the advantages to using op amps in RF applications is the exceptional flexibility in setting the gain. A wide range of gains could have been selected for the test circuits of *Figure 9*. and *Figure 10*. ±6 was selected to allow easy comparisons to the CLC404's data sheet specifications, which are all defined at a gain of +6.

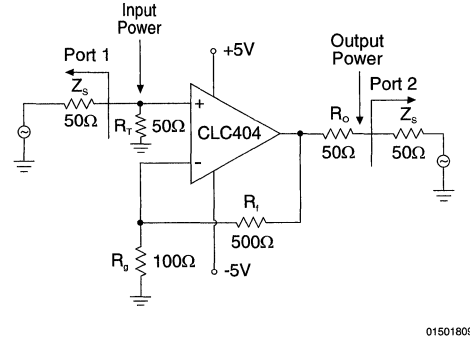


FIGURE 9. Non-Inverting Amplifier S-parameter Test Circuit

Small Signal AC Performance Characteristics (Continued)

For the inverting gain configuration, R_M along with R_g sets the input impedance to 50Ω. An R_T of 50Ω is retained on the non-inverting input to limit the possibility of self-oscillation in the non-inverting input transistors (See application note OA-15).

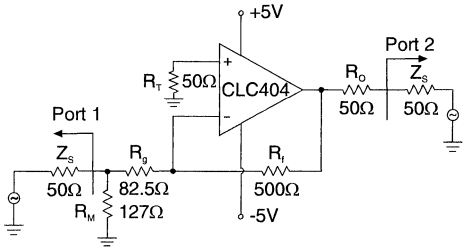


FIGURE 10. Inverting Amplifier S-parameter Test Circuit

Input/Output VSWR

The Voltage Standing Wave Ratio (VSWR) is a measure of how well the input and output impedances are matched to the source impedance. (It is assumed throughout that the transmission line characteristic impedance is also equal to the source impedance of both ports-50Ω in this case). It is desirable that the input and output impedances be as closely matched as possible to the source for maximum power transfer and minimum reflections.

$$VSWR = \frac{Z_l}{Z_s} \text{ or } \frac{Z_S}{Z_l} \quad \text{whichever} > 1$$

$Z_l \rightarrow$ amplifier input or output impedance

$Z_S \rightarrow$ test system source impedance

$$\text{Return loss} = 20\log\left(\frac{VSWR+1}{VSWR-1}\right) = 10\log(S_{11})^2 \text{ input}$$

$$\text{or } 10\log(S_{22})^2 \text{ output}$$

Ideal VSWR = 1

Typically, VSWR = 1.5, for RF-amps over their operating frequency range

Measuring the input VSWR is simply a matter of measuring the ratio of the reflected power vs. incident power on Port 1 of *Figure 9* and *Figure 10* (S_{11}). A perfect match will reflect no power. Output VSWR is measured similarly at Port 2 (S_{22}).

As described earlier, an op amp's input and output impedances are determined by external components selected by the designer. For this reason, I/O VSWR is never shown on an op amp's data sheet. Excellent VSWR can, nevertheless, be achieved using the components shown in *Figure 4* and *Figure 5.*

An op amp's gain polarity has minimal effect on the output VSWR. At low frequencies, R_O by itself will determine the output VSWR. Setting this resistor to 50Ω will yield excellent output VSWR to reasonably high frequencies. As the test frequency increases, however, the op amp's output impedance will begin to increase as the loop gain rolls off (reference 3, page 237). This inductive characteristic can be partially compensated by a small shunt capacitance across R_O. *Figure 11* shows this, for either gain polarity, along with tested output VSWR with and without this shunt capacitance. The value of this capacitance will depend on the amplifier and, to some extent, on the gain setting, and was determined empirically for this test by using a small adjustable cap (5-20pF) directly across R_O.

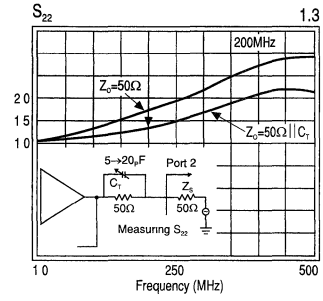


FIGURE 11. Measuring and Tuning CLC404 Output VSWR

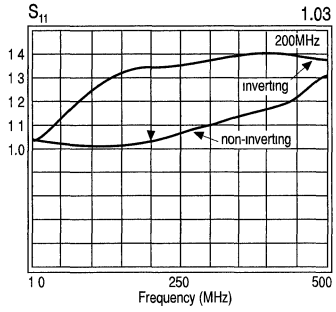
The marker at 200MHz indicates an output VSWR of 1.3:1 when CT is tuned optimally. Tuning CT also extends the frequency response (S_{21}) lightly and will be left in place for the remainder of the tests.

The input impedance match of the non-inverting topology *Figure 9* is principally set by R_T. As the frequency increases, the input capacitance of the op amp will eventually degrade the input VSWR. This effect is so negligible over the expected operating frequency range, however, that no tuning is required.

The input impedance match of the inverting topology *Figure 10* is, at low frequencies, set by the parallel combination of R_g and R_M. This holds very well as long as the amplifier's inverting input acts like a low impedance over frequency. For current feedback amplifiers, the inverting input is actually a driven, low impedance buffer. It's impedance will, however, increase with frequency. A voltage feedback amplifier's apparent inverting input impedance will also increase with frequency as its loop gain rolls off. In the voltage feedback case, the increase in inverting input impedance will be seen at a lower frequency than for a current feedback amplifier and will depend strongly on the amplifier gain setting.

Input/Output VSWR (Continued)

Figure 12 shows the tested input VSWR for the two gain polarities of *Figure 9* and *Figure 10*. In this case, we are measuring S_{11} and allowing the HP8753A to convert the measurement and display VSWR directly.



01501813

FIGURE 12. CLC404 Input VSWR

Note carefully the change in scale for the input VSWR vs. the output VSWR plot. The marker on the non-inverting test trace shows an exceptional input VSWR of 1.03:1 at 200MHz, while the inverting, though higher, remains under 1.4:1 through this range.

Forward Gain and Bandwidth

Typical RF amplifier specifications show a fixed gain, as defined in *Figure 1*, with a specified frequency range for 0.5dB gain flatness, along with -3dB cutoff frequencies. For the designer using a current feedback op amp, a wide range of possible gains are easily obtainable. With the CLC404's specified voltage gain range of ±1 to ±10, and including the additional 6dB loss from the output to the load, -6dB to 14dB gains may be achieved using the CLC404. Higher gains can be achieved with this, or any other current feedback amplifier, with some sacrifice in bandwidth (see application note OA-13). For example, the CLC401, specified over a ±7 to ±50 voltage gain range, translates into an 11dB to 28dB gain range for RF applications.

The forward gain over frequency (commonly called the frequency response and measured as S_{21}) always appear in the National data sheets over a range of gains. Small signal -3dB bandwidth and gain flatness are also guaranteed at a particular gain for each amplifier. Rarely does a voltage feedback op amp show the S_{21} characteristics, since it so strongly depends upon the gain setting. Rather, these amplifiers show an open loop gain and phase plot and leave it to the designer to predict closed loop gain and phase. The frequency response plots for the National op amps are normalized to show each gain coming in at the same grid on the plot for easier comparisons of frequency response shape over a wide range of gains. Another advantage of the excellent loop gain control of the current feedback topology is exceptional forward gain phase linearity. This phase is also shown on the frequency response plot. A maximum deviation from linear phase is guaranteed at a particular gain setting in the data sheet specifications.

The part to part variation in the frequency response is minimal for the hybrid amplifiers from National, with more variation seen for the monolithic op amps. As application note OA-13 describes, the current feedback topology allows an easy, resistive trim for the frequency response shape that has no impact on the forward gain. This frequency response flatness trim has the same effect for either non-inverting or inverting topologies. *Figure 13* shows this adjustment added to the circuit of *Figure 9*, along with the measured S_{21} with and without this trim. As OA-13 describes, this resistive trim inside the feedback loop has the effect of adjusting the loop gain, and hence the frequency response, without adjusting the signal gain, which would still be set by only R_f and R_g. This particular test achieved a flatness of ±.1dB from DC to 110MHz at a gain of 9.54dB for the non-inverting test circuit shown (with identical results for an inverting configuration).

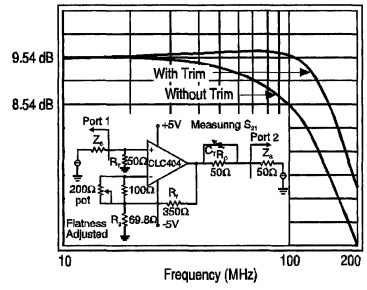


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FIGURE 13. Measuring and Adjusting the Frequency Response S_{21}

Note that the values for R_f and R_g have been reduced from those used in the circuit of *Figure 9*, although their ratio and hence the gain, have remained the same. With the adjustment pot set to zero ohms, this lower R_f value ensures that the frequency response will be peaked for any particular CLC404 used in the circuit. Then, by increasing the resistance into the inverting input, the amplifier can be compensated and S_{21} adjusted to the excellent flatness shown above.

The part to part variation in frequency response becomes more pronounced as the desired operating frequencies and signal gains increase Operation of the CLC404 through 50MHz at 9.54dB gain would, for example, have minimal variation relative to operation through 100MHz and 14dB gain. For ±.1dB flatness, and considering the rapid degradation in distortion performance at higher frequencies, 100MHz is probably a reasonable upper limit for the operation of National op amps (available at the time of publication) in RF (or IF) applications. Higher frequency operation can be achieved if the degraded flatness and distortion characteristics are acceptable to the application. New product introductions can be expected to extend this operating frequency.

Reverse Isolation

This small signal AC characteristic is a measure of how much signal injected into the output port makes it back into the input source. The magnitude of S_{12} is the measure of

Reverse Isolation (Continued)

reverse isolation. National's current feedback op amps exhibit excellent reverse isolation relative to most RF amplifiers. This results from both the output and inverting input being driven, low impedance, nodes. To the extent that the output of the op amp and its inverting input both present very low impedances over wide frequency ranges, significant signal attenuation can be expected in taking a signal voltage applied to the output matching resistor and tracing it back to either an inverting or non-inverting input signal. Slightly more attenuation can be expected for the non-inverting vs. inverting configurations, since the signal must also get from the inverting to non-inverting pin in the non-inverting case.

The circuit of *Figure 13*, along with the inverting circuit of *Figure 14* were used to measure the reverse isolation for both gain polarities, as shown in *Figure 15*. Although reverse isolation is generally specified as a positive number, this is simply the negative of the log gain in going backwards through the amplifier. Hence, the plot of *Figure 14* shows a rising "gain" that would be interpreted as a decreasing reverse isolation as we go to higher frequencies. As *Figure 15* shows, isolations in excess of 30dB are easily obtainable through frequencies far higher than the operating frequency range, with very high isolations observed at low frequencies.

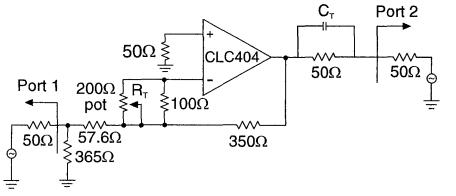

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FIGURE 14. Inverting Reverse Isolation Test Circuit

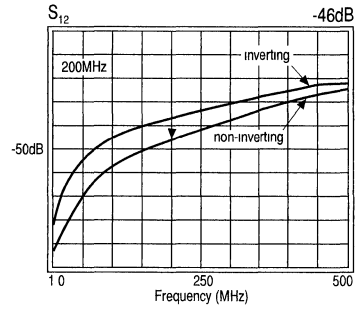

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FIGURE 15. Reverse Gain for the Circuits of Figures 13 and 14

Dynamic Range Limiting Characteristics

The final area of concern in applying op amps to RF applications are the limits to dynamic range familiar to RF amplifier users. These are generally limited to:

-1dB Compression Point

2-Tone, 3rd Order, Intermodulation Intercept

Noise Figure

The -1dB Compression Point is a measure of the maximum output power capability of the amplifier. The 2-Tone Intercept allows the prediction of spurious signals caused by amplifier non-linearities when two input signals closely spaced in frequency are applied to the input. The noise figure is a measure of how much noise is added by the amplifier and will set a limit to the minimum detectable signal.

Dynamic Range Limiting Characteristics (Continued)

Although each of these can certainly be measured for any particular op amp configuration, their interpretation for op amps may vary from RF amplifiers depending on the op amp being used and the specification. Each of these will be described generally and developed, and/or measured, for the CLC404 with any anomalies in interpretation noted.

-1dB Compression Point

Briefly stated, this is the expected output power, at a fixed input frequency, where the amplifier's actual output power is 1dBm less than expected. As *Figure 16* shows, it can also be interpreted as the ideal output power at which the actual amplifier gain has been reduced by 1dB from its value at lower output powers. With both the X and Y axis of *Figure 16* a dBm scale, the output power vs. the input power will have a slope of 1. If we shift the X-axis by the amplifier's low power gain (a 20dB gain was used arbitrarily in *Figure 16*), the amplifier's input to output transfer would ideally be a unity slope line through the origin.

An additional interpretation of *Figure 16* is that beyond the -1dB compression point the output power remains fixed as the input power is increased. If S_{21} were measured at a fixed frequency, with a swept input power, we would get a horizontal line, showing the low power gain, that eventually transitions to a -1 slope line as the output power becomes fixed while the input power continues to increase.

The -1dB compression power is commonly used as a maximum output power limit when computing an amplifier's dynamic range. Standard AC coupled RF amplifiers show a relatively constant -1dB compression power over their operating frequency range.

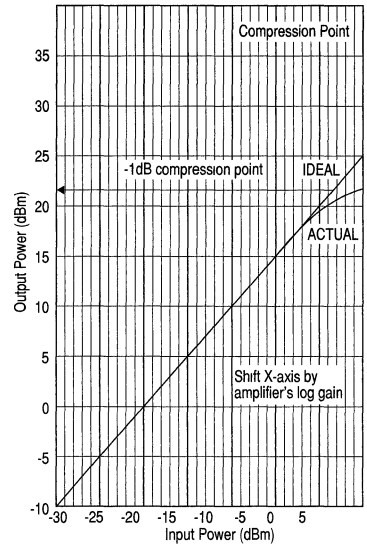

FIGURE 16. Illustration of -1dB Compression

For an operational amplifier, the maximum output power depends strongly on the input frequency. The two op amp specifications that serve a similar purpose to -1dB compression are output voltage range and slew rate. At low frequen-

-1dB Compression Point (Continued)

cies, increasing the power of a fixed frequency input will eventually drive the output "into the rails" - a saturation limit typically some number of diode drops below the supply voltages. In addition, as the input frequency increases, all op amps will reach a limit on how fast the output can transition. This is typically specified as a slew rate indicating the maximum dV/dT at the output pin voltage. Half this slew rate is available at the matched load when an output series matching resistor is used. For a sinusoidal signal, the maximum slew rate occurs at the 0 crossing. This maximum dV/dT is simply the peak voltage exursion times the radian frequency. Given a slew rate in Volts/sec (SR) and a frequency, the maximum peak amplitude before slew limited operation is experienced is predicted to be SR/(2*π*frequency). However, this peak amplitude, which can be converted to a dBm power at the load using the expressions developed earlier, does not relate directly to the measured -1dB compression.

Figure 17 shows the measured -1dB compression powers vs. frequency for the CLC404 in the circuits of *Figure 13* and *Figure 14*. Since the maximum output power is principally a function of the output stage, there is very little difference between the non-inverting and inverting -1dB compression points. For the National amplifiers that show a higher inverting slew rate than non-inverting (e.g. CLC400), a higher -1dB compression power at higher frequencies in inverting configurations would be expected. The low frequency value, however, should be similar between polarities, since it is determined by the maximum output voltage swing (principally set by the power supply voltages and the headroom requirements in the output stage).

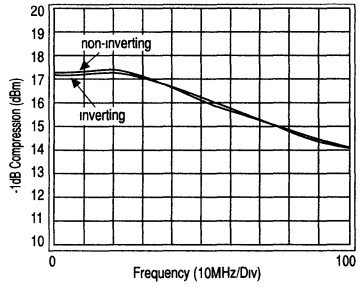

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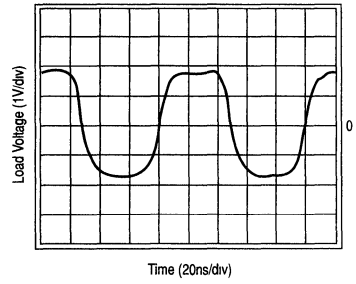
FIGURE 17. 1dB Compression for the CLC404

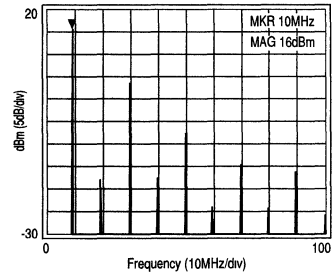
Although *Figure 17* shows the -1dB compression as defined in *Figure 16*, it is also very useful to look at the output waveforms and spectrums to gain an understanding of what is setting the measured -1dB compression power.

Figure 18 and *Figure 19* show the time waveform and the spectrum at the load for the input power that yields the -1dB compression point for the CLC404 operating at 10MHz.



01501819

FIGURE 18. Output Waveform at 10MHz - 1dB Compression



01501820

FIGURE 19. Output Spectrum at 10MHz - 1dB Compression

At this low frequency, we are clearly running into an output voltage swing limitation. With a 17.3dBm -1dB compression (as shown at 10MHz in *Figure 17*), we would expect the fundamental amplitude in the spectrum to be at 16.3dBm. The observed 16dBm in the spectrum of *Figure 19* is a reasonable match to this expected fundamental power. It is, however, incorrect to directly convert this fundamental power at -1dB compression into a sinusoid and expect that the amplifier can deliver a sinusoid of this amplitude. For the 16.3dBm fundamental power predicted by the -1dB compression measurement, we might expect that the output is delivering an approximately $4V_{pp}$ sinusoidal swing at the load, or ±4V swing at the output pin. Although this would

-1dB Compression Point (Continued)

exceed the maximum output swing specification for the CLC404 operating at ±5 volt supplies, this amplitude of sinusoid is in fact available if a zero loss filter is used to pass on only the fundamental harmonic.

Notice that a considerable portion of the output power has been spread into the odd order harmonics. This is typical of the square wave output observed in the time domain trace of *Figure 18*. The fundamental (10MHz) power can be related to the output time waveform amplitude through the Fourier series expansion of the output waveform. If the output were a perfect square wave, under conditions of output voltage limited operation, a peak square wave amplitude of A would generate a fundamental frequency amplitude of $4*A/\pi$. Going from the measured peak amplitude of the output time waveform, the anticipated -1dB compression would be calculated as the power in a sinusoid $4/\pi$ times the square wave amplitude +1dBm. Doing this for the measured ±1.8V swing of *Figure 18* would predict 15.1dBm (peak-peak square wave amplitude converted to dBm) + 2.1dBm ($20*\log(4/\pi)$) + 1dBm (reported -1dBm output power is 1dBm higher than measured power) = 18.3dBm. This is 1dBm higher than measured. This can be explained by the less than perfect square wave shape shown in the time waveform of *Figure 18*. This less than perfect square wave will yield a coefficient for the fundamental term in the Fourier expansion that is actually less than the predicted $A*4/\pi$.

As the operating frequency increases, the slew limit for the op amp will eventually restrict the achievable output swing to something less than the output voltage swing limit of the amplifier. This can be observed in *Figure 11* at approximately 30MHz for the CLC404. Again, it is instructive to look at the time waveform and resulting spectrum when operating at an input power that yielded a -1dB compression in measured gain at the these higher frequencies. *Figure 20* and *Figure 21* show this for the non-inverting circuit (*Figure 13*) operating at the input power necessary to produce the measured -1dB compression with a 50MHz sinusoidal input signal (From *Figure 17*, this input power would be 16.3dBm - 9.54 (gain) = 6.8dBm)

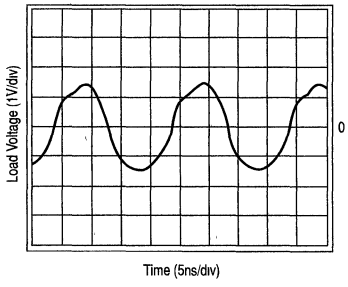


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FIGURE 20. Measured Output Waveform at 50MHz -1dB Compression

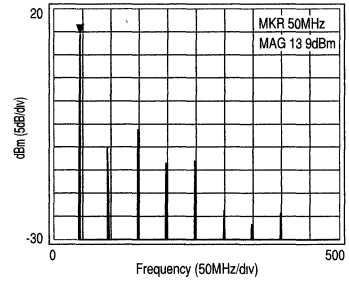

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FIGURE 21. Measured Output Spectrum at 50MHz -1dB Compression

The measured -1dB compression power under slew limited conditions is dependent on the amount of power in the fundamental frequency generated by the time waveform shown in *Figure 20*. Although we can say that the -1dB compression must be related to the amplifier's slew rate, it would be very difficult to relate the slew rate to the waveform shape and then, through the Fourier series, to the fundamental power and hence -1dB compression. The exact distribution of power into the fundamental and harmonics is changing over frequency. All that can really be said is that at these higher frequency -1dB compressions, a significantly distorted waveform with a peak to peak excursion less than that seen at lower frequencies is being generated.

At low frequencies, the -1dB compression power can be predicted approximately using the analysis shown earlier by assuming a square wave output set by the output voltage swing limits shown in the op amp data sheet. Remember that the output voltage range specified in the data sheet is twice what can be delivered through the 6dB loss taken from the matching resistor to the load. It is not, however, possible to easily predict the higher frequency -1dB compression from the slew rate specification. As will become apparent in the next section, it is also not possible to relate the -1dB compression to the third order intercept. Typical RF amplifiers will show a 3rd order intercept 10dBm higher than the -1dB compression point. National op amps, if they show an intercept characteristic, have an intercept considerably higher than what would be predicted by adding 10dBm to the -1dB compression.

2-Tone, 3rd Order Intermodulation Intercept

This specification is directed at predicting the 3rd order intermodulation distortion powers for any combination of two closely spaced (in frequency) input signals. Any amplifier can be modeled to have a polynomial approximation to its transfer function from input to output. When two input signal frequencies are present, the 3rd order term of this polynomial approximation will give rise to distortion terms at frequencies that can be very near the input signal frequencies.

2-Tone, 3rd Order Intermodulation Intercept (Continued)

These closely spaced distortions are considerably more troublesome to narrowband IF channels than the simple harmonic distortion terms that appear in integer increments away from the input signal frequency.

Appendix B expands all of the spurious frequency locations and distortion coefficients for two input signals at frequencies of f_O-Δf and f_O+Δf when passed through a 5th order polynomial. With this simple definition of equal deviations from a center frequency (an average frequency), all of the spurious frequency locations become very simple algebraic expressions of f_O and Δf. Using this approach to defining the test frequency locations also allows a clear illustration of the symmetric clusters of spurious terms around integer multiples of f_O. From appendix B, the 3rd order inter-modulation terms fall at $f_O \pm \Delta Df_O$. With an input signal defined as V_I = $A\cos(2\Delta(f_O-\Delta f)t) + B\cos(2\Delta(f_O+\Delta f)t)$, and an input to output voltage gain transfer function of $V_O = K_0 + K_1 V_I + K_2 V_I^2 + K_3 V_I^3$ (ignoring the higher order terms for now), a lower 3rd order spurious term at $f_O - 3\Delta f$ with an amplitude of $(3/4)*K_3*A*B_2$ and an upper spurious at $f_O + 3\Delta f$ with an amplitude of $(3/4)*K_3*A_2*B$ will result.

If equal amplitude signals were applied to the input (A = B), and if these were increased in an equal fashion, the two spurious amplitudes would increase in a cubic fashion. In dBm terms, if the two input, and hence output, powers were increased by 1dBm, this model predicts that the two output third order spurious powers will increase by 3dBm. It is interesting to note the effect of adjusting just one of the input frequency power's. Changing the lower test frequency power by 1dBm will change the lower spurious by 1dBm and the upper spurious by 2dBm. Conversely, changing the upper test frequency power by 1dBm will change the lower spurious by 2dBm and the upper by 1dBm. The dependence of the 3rd order spurious power to output test frequency power (assuming equal powers for each test frequency) is shown graphically in *Figure 22*.

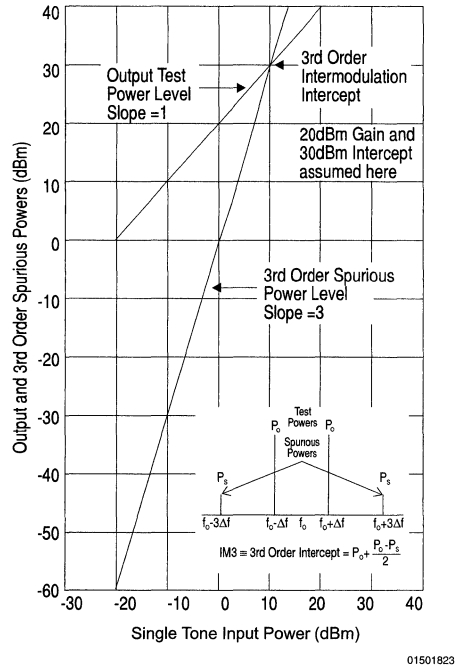


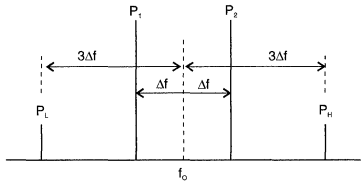
FIGURE 22. Output and 3rd Order Spurious Power vs. Input Power

As shown in *Figure 22*, the 3rd order spurious powers, increasing at a 3X rate vs. the input power, will, at some output power, "intercept" the desired output powers that are increasing at a 1X rate vs. the input power. Another way of

2-Tone, 3rd Order Intermodulation Intercept (Continued)

saying this is that there is a 2X closure rate between the desired output powers and the undesired 3rd order intermodulation spurious powers. The graph of *Figure 22* was arbitrarily set up for an amplifier gain of 20dB (the x-axis has been shifted to yield 0dBm output power for -20dBm input power) and for a 30dBm 3rd order intercept. No actual amplifier will be able to reach the intercept point from an output power standpoint since this intercept typically exceeds the -1dB compression power by at least 10dBm. The intercept is intended as a mathematical construct to allow the prediction of the spurious power level for a given output signal power. For an amplifier that shows a 3rd order intermodulation intercept characteristic, a single measurement of output powers and spurious levels are sufficient to solve for the intercept point as shown by the equation in *Figure 22*.

Figure 22 assumes equal output power levels for the two desired output signals. A more general approach, with unequal test power levels, shows that, from one set of measurements, two estimates for the 3rd order intercept can be made. *Figure 23* steps through this analysis and concludes with the predictive equations for each of the two 3rd order spurious levels. The graphical representation shown in *Figure 23* is modeling what would be observed for a spectrum analyzer measurement of the test and spurious powers.



1^{st} estimate of intercept $IM3_1 = P_1 + \frac{P_2 - P_L}{2}$

2^{nd} estimate of intercept $IM3_2 = P_2 + \frac{P1 - P_H}{2}$

Averaging these $IM3_{AVG} = \frac{P_1 + P_2}{2} + \frac{P_2 - P_L}{4} + \frac{P_1 - P_H}{4}$

If $P_1 = P_2 = P_T$ and $P_L = P_H$, define $\Delta dB_c = P_O - P_L = P_O - P_H$

$IM3 = P_O + \frac{\Delta dB_c}{2}$

Solving the two intercept estimates for P_L and P_H

$P_L = P_2 - 2\,(IM3 - P_1)$

$P_H = P_1 - 2\,(IM3 - P_2)$

or, for $P_1 = P_2 = P_O$

$P_L = P_H = 2\left(\frac{3}{2}P_O - IM3\right)$

01501824

FIGURE 23. 3rd Order Intermodulation intercept Calculations

Typical RF amplifiers closely approximate this 3rd order intermodulation spurious model with an intercept that is relatively constant over the specified operating frequency range of the amplifier. Op amps, however, show significant deviations from this simple model. The principal difference is that all op amps will show a strongly frequency dependent 2-tone, 3rd order spurious performance. The observed intermodulation spurious levels will be a function of the intrinsic distortion in the forward path of the amplifier corrected by whatever loop gain the amplifier has at that frequency. All op amps show a loop gain that decreases with frequency. Hence, the 3rd order spurious levels will, in general, increase with frequency for fixed output test powers (reference 4 discusses this loop gain dependence in detail).

An additional concern is at what point in the circuit to define the 3rd order intercept. In order to make direct comparisons to RF amplifiers, National defines the 3rd order intercept to be at a 50Ω load when driving from a 50Ω output impedance. Some of the earlier National data sheets (e.g. CLC220, CLC221) defined the intercept for a voltage swing at the output pin converted into a power (as if it were driving 50Ω) while actually applying that output swing to the series 50Ω into a 50Ω load. This has the effect of defining an intercept that is 6dBm higher than what is actually available at the load. This can be seen from the equation shown above for IM3. Recall that IM3, for equal test power levels for the two test frequencies, is simply the test power level +1/2 the difference between the test power levels and the spurious power levels. This difference does not change in going from the output pin to the matched load. However, the output voltage swing will drop by 6dB and, since the output pin power was erroneously defined as being a particular voltage swing across a 50Ω load (when it in fact sees a 100Ω load), this will translate into a 6dBm drop in the test power level to the matched 50Ω load Therefore, the usable intercept at the matched load is 6dBm lower than specified in those earlier data sheets that call for an output power calculation at the output pin.

Given that the test power level is being defined at the matched load, it is important to consider the amplifier limitations on the maximum power and frequency of test. For a two tone test of equal powers and closely spaced frequencies, the available peak to peak voltage swing for each test frequency at the load is 1/4 the peak to peak output voltage available at the amplifier's output pin while the available slew rate for each test tone can be estimated as 1/8 the amplifier's specified slew rate. For a 2-tone test signal being generated at a matched load, twice the peak to peak swing is being generated in the envelope (and twice the slew rate). Going back through the matching resistor to the output pin will double this swing and slew rate again. In addition, empirical testing has revealed that an overall maximum slew rate at the output pin that is 1/2 the specified op amp slew rate will show low spurious performance. As the slew rate of the output pin waveform exceeds this limit, additional nonlinearities come into play rapidly increasing the 3rd order spurious powers.

Using the circuit of *Figure 13* and the typical specifications for the CLC404, the maximum test power level at the load for each test tone, from an output swing standpoint, would be (1/4)*6V_{pp} = 1.5V_{pp} . This translates into a maximum test power level for each tone of approximately 8dBm. At this maximum output swing, the available slew rate of (1/8)*2000Vμmsec = 250V/μsec will limit the frequency of operation to less than (SR/(2*π*V_{pp}/2) = 250E6/(2*π*.75V) = 53MHz. As the test or operation powers decrease, this upper frequency limit set by the slew rate limit will increase. For example, dropping the power 6dB to 2dBm will push this limit out to 106MHz.

Although some of the National current feedback amplifiers (e.g. CLC400, CLC401, CLC560) show a good approximation to the 3rd order intercept model, the CLC404, used in

2-Tone, 3rd Order Intermodulation Intercept (Continued)

the example circuits shown thus far, shows a spurious power vs. test power characteristic that deviates significantly from the simple model of *Figure 22*. *Figure 24* shows the difference between the test and spurious powers plotted as a function of single tone test power at the load. Note that the independent variable axis is output power; not the input power shown in *Figure 22*. Ideally, this would, at each frequency, yield a straight line with a slope of +2 (instead of the +3 slope shown in *Figure 22*). A similar plot for the CLC401, which more closely approximates this ideal, is shown in *Figure 25* If an op amp closely approximated the 3rd order intercept model, a single measurement at one operating power would be adequate to predict the intercept at that frequency.

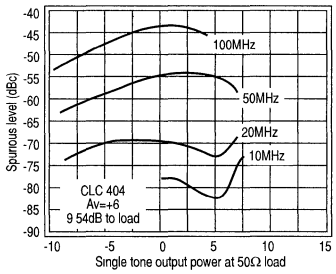


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FIGURE 24. Measured 3rd Order Spurious for the CLC404

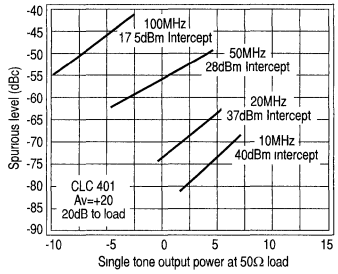

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FIGURE 25. Measured 3rd Order Spurious for the CLC401

The 3rd order spurious plot for the CLC404 is clearly showing some additional mechanism that is holding the spurious levels down as the output power level moves above 0dBm. At lower power levels, it appears that the spurious characteristic is moving towards a linear slope of 2 as predicted by the simple intercept model. Looking again at the 5th order expansion of the 2-tone coefficients shown in appendix B, an additional 5th order term contributes to the spurious powers observed at the 3rd order intermodulation frequencies. Normally, it would be expected that the K5 coefficient is so much lower than the K3 value that this 5th order contribution can be neglected. However, in the case of the CLC404, the K3 coefficient is so low as to make this second term significant at higher operating powers. Note that the contribution of this 5th order term increases as the 5th power of the two test powers vs. the more slowly increasing 3rd order term. It can be theorized that the 5th order coefficient is of opposite sign to the 3rd order coefficient. Then, as the test powers increase to the level that this 5th order term becomes significant in magnitude vs. the 3rd order, the spurious levels actually decrease for increasing output power.

The projected intercept at very low power levels can still be used to predict the spurious free dynamic range. In *Figure 24*, the intercept at low output powers may be estimated for a particular frequency as the output power minus 1/2 the y-axis value. However, it should be realized that wideband op amps like the CLC404 actually provide better spurious performance at high powers than would be predicted by this low power intercept model

The 3rd order intercept performance is typically very similar between inverting and non-inverting topologies. As discussed in reference 4, anything that changes the loop gain of the op amp will have an effect on the 3rd order spurious performance. Increasing loop gain, either by going to low feedback resistor values for current feedback op amps or low signal gains for voltage feedback op amps, will decrease the spurious powers. In both cases, however, increasing the loop gain by changing the external operating point is constrained by closed loop stability considerations. 3rd order distortions and intermodulations can be further reduced by operating any op amp at higher quiescent currents (if possible) and/or driving the output into a higher impedance load for those situations not requiring a 50Ω matched impedance environment.

Noise Figure

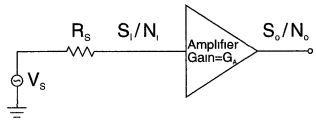
Unlike the compression point and 3rd order intermodulation intercept, the noise figure for an op amp is always usable in the same way that it is for an RF amp. It is important to remember that, like compression and intercept, a noise figure is generally developed at a particular frequency and may change over frequency. Normally, however, a single value can be used above the op amp's 1/f noise corner frequency (see application note OA-12 for an additional noise discussion and its appendices for 1/f noise corner discussion and tabulated op amp input noise terms for National op amps).

The noise figure can be accurately calculated from the equivalent input noise terms for an op amp and the resistor values used to achieve the desired gain and input impedance. Unlike an RF amplifier with a fixed gain and noise figure, an op amp's noise figure will be strongly dependent on the gain setting We can, however, easily predict the noise figure with the equations developed here.

A very general development for an op amp's non-inverting noise figure will be performed in order to allow easy comparison to noise figure expressions found in earlier National data sheets. The inverting op amp's noise figure will, however, proceed with the assumption normally used – that the input impedance is to be matched to the source impedance.

Noise Figure (Continued)

An idealized schematic illustrating the definition of noise figure is shown in *Figure 26.*



$$\text{Noise Figure} = NF = 10\log\left[\frac{S_i/N_i}{S_o/N_o}\right] = 10\log\left[\frac{S_i N_o}{S_o N_i}\right]$$

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FIGURE 26. Noise Figure Definition

All of the input and output noise and signal terms in the equation for noise figure (NF) are considered to be powers. N_I is the noise power delivered by the source resistor to the input of the amplifier. All other noise sources are considered to be part of the amplifier and contribute to the noise power, N_o , seen at the output.

Looking at the two parts of the NF expression (inside the log function) yields:

$S_i/S_o \rightarrow$ Inverse of the power gain provided by the amplifier

$N_o/N_i \rightarrow$ Total output noise power, including the contribution of R_S , divided by the noise power at the input due to R_S

To simplify this, consider Na as the noise power added by the amplifier (reflected to its input port):

$S_i/S_o \rightarrow$ 1/G

$N_o/N_i \rightarrow$ $G^*(N_i+N_a)/N_i$ (where $G^*(N_i+N_a) = N_o$)

Substituting these two expressions into the NF expression:

$$NF = 10\log\left[\frac{1}{G}\left(\frac{G[N_i+N_a]}{N_i}\right)\right] = 10\log\left(1+\frac{N_a}{N_i}\right) \quad (1)$$

The noise figure expression has simplified to depend only on the ratio of the noise power added by the amplifier at its input (considering the source resistor to be in place but noiseless in getting Na) to the noise power delivered by the source resistor (considering all amplifier elements to be in place but noiseless in getting N_i). Generally, the definition for NF also constrains the input impedance for the amplifier to be conjugate matched to the source resistor (this yields $N_i = k_T$ with this constraint). We will, however, relax this constraint initially to allow comparison to the NF expressions found in National's earlier datasheets.

The NF of *Equation (1)* is specified in terms of a power ratio. The individual noise terms for the op amp are, however, expressed as spot noise voltages or currents (Spot means in a 1Hz bandwidth, as opposed to integrated over some noise power bandwidth. See OA-12). Combining separately contributing noise sources is a matter of adding noise powers. This can be done by converting all current noises to a voltage through the appropriate impedance, then summing all of the squared noise voltage terms. Any impedance (normally needed to define a power) or noise power bandwidth (used to convert from spot to integrated noise) will normalize out since we are developing the ratio of two powers at the same point in the circuit. Getting to the total spot noise power is then simply a matter of summing all the relevant squared noise voltages.

Figure 27 below shows an op amp in the non-inverting configuration with all of the individual resistor and amplifier input noise terms detailed.

Where;

e_n = op amp input voltage noise

in_i = op amp non-inverting input current noise

i_i = op amp inverting input current noise

$R_T \rightarrow$ input terminating resistor

e_T = R_T's voltage noise

e_f = R_f's voltage noise

i_g = R_g's current noise

e_S = R_S's voltage noise

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FIGURE 27. Non-Inverting Op Amp Noise Figure Analysis Circuit

Recall that the noise of a resistor (Johnson Noise) can be defined as either a spot current or voltage noise. For a resister of value R, these two possible expressions are:

$$\text{voltage noise, } e_R = \sqrt{4kTR}$$

$$\text{current noise, } i_R = \sqrt{\frac{4kT}{R}}$$

where;

$k \rightarrow$ Boltzman's constant

k = 1.38E-23 Joules/°Kelvin

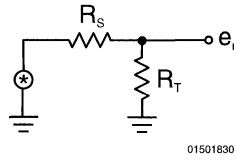
$T \rightarrow$ °Kelvin = 290° in this analysis

4kT = 16E-21 Joules at T = 290°K

The 3 amplifier noise terms are available for most of National's amplifiers in appendix 2 of OA-12. If the spot noise Figure below the 1/f noise corner is of interest, appendix I of OA-12 also shows how to approximate the low frequency spot noise from the high frequency flat band value and the 1/f noise corner frequency.

Using the circuit of *Figure 27*, the NF expression can be developed by generating an expression for N_i and N_a . N_i is the noise power delivered by the source resistor noise to the input of the amplifier. This analysis simply proceeds by considering the noise voltages as sources in normal linear circuit analysis, but eventually squaring the resulting noise voltage delivered to RT from es. *Figure 28* shows the equivalent circuit and the resulting N_i . This is considering the amplifier to have an infinite non-inverting input impedance, with all other noise sources neglected for now (superposition of noise voltage contributions are used throughout this analysis).

Noise Figure (Continued)



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$$e_i = \frac{R_T}{R_S + R_T}\sqrt{4kTR_S}$$

$$N_i = e_i^2 = \frac{R_T{}^2\, 4kTR_S}{(R_s \div R_T)^2}$$

$$\text{define} \quad R_p = R_s \,||\, R_T = \frac{R_S R_T}{R_S + R_T}$$

$$N_i = \frac{4kTR_pR_T}{R_S + R_T} = \frac{4kTR_p}{1 + R_T / R_S}$$

01501831

FIGURE 28. Input Noise Power calculation

To get an expression for N_a , all other noise voltages and currents are referred to the non-inverting input and summed as voltages squared. For the noise terms on the inverting side of the amplifier, it is best to find each term's gain to the output voltage, then reflect back to the non-inverting input by dividing by the non-inverting voltage gain of the amplifier. At this point, since we are dealing with linear voltage gains, define this gain as $A_v + = 1 + R_f / R_g$. Table 1 tabulates each individual voltage and current noise and its "gain" to the input of *Figure 27*. Note that all current noise terms have an impedance in their gain expression to yield all voltage noise terms at the input of the amplifier.

TABLE 1. Noise Terms Contributing to N_a for the Non-inverting Op Amp Configuration

Noise Source	Value	Voltage Gain to Input
Non-inverting input voltage noise	e_n	1
Non-inverting input current noise	in_i	R_n|| $R_T \rightarrow (R_P)$
Inverting input current noise	I_i	R_f/A_v^+
Input terminating resistor voltage noise	$\sqrt{4kT/R_g}$	R_S/R_S+R_T
Gain setting resistor current noise	$\sqrt{4kT/R_g}$	R_f/A_v^+
Feedback resistor voltage noise	$\sqrt{4kT/R_g}$	$1/A_v^+$

One point of possible confusion is that, although we are trying to develop the total noise power at the input of the op amp, what relation does this have to the input voltage noise term that already appears in the op amp model, en. As described in OA-12, the noise model for an op amp attempts to lump all the internal noise sources of the actual amplifier into an equivalent input noise voltage at the non-inverting input and two input noise currents. The intent is to provide a means of predicting the noise performance over a wide range of external operating conditions. The en shown in the analysis model of *Figure 27* is associated only with the internal characteristics of the op amp itself. The total amplifier output noise includes this and contributions from all of the other noise sources shown there. Having gotten to an expression for the total output noise voltage, an equivalent input noise voltage may be derived by simply dividing by the voltage gain of the op amp. This step of input referring each noise source is performed for each term in Table 1.

To form an expression for N_a, we need only to sum the squared product of each noise source and its associated gain, as shown in Table 1.

$$N_a = e_n^2 + (I_{ni}R_p)^2 = \left(I_i \frac{R_f}{A_v^+}\right)^2 + \frac{4kTR_TR_S^2}{(R_S + R_T)^2} + \frac{4kTR_f{}^2}{R_g(A_v^+)^2} + \frac{4kTR_f}{(A_v^+)^2}$$

This will simplify to.

$$N_a = e_n^2 + (I_{ni}R_p)^2 + \left(I_i \frac{R_f}{A_v^+}\right)^2 + \frac{4kTR_p}{1 + R_T/R_S} + \frac{4kTR_f}{+A_v}$$

op amp noise terms + input terminating + combined feedback resistor noise term and gain setting resistor noise terms

(2)

Noise Figure (Continued)

An expression for the non-inverting noise Figure (N+) may now be derived by substituting the equation in *Figure 28* and *Equation (2)* back into *Equation (1)*.

$$NF^{+} = 10\log\left[1 + \frac{e_n^{\,2} + (i_{ni}R_p)^2 + \left(i_i\frac{R_i}{A_v^{+}}\right)^2 + \frac{4kTR_p}{1+R_T/R_S} + \frac{4kTR_f}{A_v^{+}}}{\frac{4kTR_p}{1+R_S/R_T}}\right]$$

This will further simplify to

$$NF = 10\log\left[1 + \frac{1+R_s/R_T}{1+R_T/R_S} + \frac{(1+R_s/R_T)R_p^{\,2}}{4kTR_p}\left(\left(\frac{e_{ni}}{R_p}\right)^2 + i_{ni}^{\,2} + \left(\frac{i_iR_f}{R_pA_v^{+}}\right)^2 + \frac{4kTR_f}{R_p^{\,2}A_v^{+}}\right)\right] \quad (3)$$

Simplifying two of these terms:

$$\frac{1+\frac{R_S}{R_T}}{1+\frac{R_T}{R_S}} = \frac{\frac{R_T+R_S}{R_T}}{\frac{R_S+R_T}{R_S}} = \frac{R_S}{R_T}$$

Recall that $R_p = \frac{R_SR_T}{R_S+R_T}$

$$\text{then } \frac{\left(1+\frac{R_S}{R_T}\right)R_p^{\,2}}{4kTR_p} = \frac{\frac{R_T+R_S}{R_T}\,\frac{R_SR_T}{R_S+R_T}}{4kT} = \frac{R_S}{4kT}$$

Putting these simplifications back into Equation 4 yields:

$$NF^{+} = 10\log\left[1 + \frac{R_S}{R_T} + \frac{R_S}{4kT}\left(\left(\frac{e_{ni}}{R_p}\right)^2 + i_{ni}^{\,2} + \left(\frac{i_iR_f}{R_pA_v^{+}}\right)^2 + \frac{4kTR_f}{A_v^{+}R_p^{\,2}}\right)\right] \quad (4)$$

This expression for the non-inverting noise Figure closely matches the equation shown in the CLC205 and CLC206 data sheets. *Equation (4)* differs only in some of the variable names and in the addition of a term due to the R_f and R_g noise, which the CLC205 and CLC206 equations neglected.

If we were to let $R_T \rightarrow \infty$, driving the signal directly into the non-inverting input with no input termination and neglect any noise contribution from i_{ni}, R_f and R_g, *Equation (4)* will reduce to:

$$NF^{+}_{est} \approx 10\log\left[1 + \frac{e_{ni}^{\,2} + \left(i_iR_f/A_v^{+}\right)^2}{4kTR_S}\right] \quad (5)$$

This expression for NF matches that appearing in several of the National hybrid amplifier data sheets (e.g. CLC200, CLC201, CLC103, CLC203, CLC220 and CLC221), where the Δf term has been replaced by a 1 in *Equation (5)* to consider only spot noise figure.

Equation (4) above is the most general expression for an op amp's non-inverting spot noise figure, considering an arbitrary input termination resister R_T and all possible contributing terms (even though some may prove negligible). The simplified *Equation (5)* assumes no input terminating resister and neglects any noise contribution of the op amps non-inverting input bias current noise and the feedback and gain setting resister noises. The expression found in the CLC205 and CLC206 data sheets include an arbitrary R_T , but still neglected the noise contribution of R_f and R_g.

Having labored through all of this to clarify where some of the earlier noise figure expressions published by National came from, we can now step to the most useful form of the noise figure expression where $R_S = R_T$. Doing this in *Equation (4)* yields:

$$NF^{+} = 10\log\left[2 + \frac{e_{ni}^{\,2} + \left(i_{ni}\frac{R_S}{2}\right)^2 + \left(\frac{i_iR_f}{A_v^{+}}\right)^2 + \frac{4kTR_f}{A_v^{+}}}{kTR_S}\right]$$

With $R_S = R_T$ (6)

This is probably the most useful formulation of the noise figure for the non-inverting op amp. The "2" arises from the signal attenuation we take in getting from the source to the input by using an external, noisy, resister matched to R_S (e.g. R_T). Note that the noise figure will decrease as the signal gain is increased due to the two numerator terms showing an A_v + in their denominators. Also note that for current feedback amplifiers, the feedback resister R_f is fixed to satisfy the amplifier's loop gain phase margin requirements (application note OA-13 discusses relaxing this requirement somewhat). Hence, the latter two terms in *Equation (6)*'s numerator do indeed decrease with increasing gain. If R_f were not particularly constrained in value, as with voltage feedback amplifiers, the R_f/A_v + term appearing in the last two terms of *Equation (6)* would probably make more sense if replaced by an $R_f \| R_g$ term.

Inverting Op Amp Noise Figure

In this case, the discussion will be simplified by constraining the input impedance of the op amp to be equal to R_S. *Figure 29* shows the circuit for analysis with all of the contributing noise sources:

RT has been retained on the non-inverting input, along with its noise voltage source, for complete generality. R_g's noise now appears as a voltage source instead of the current noise term used in the non-inverting analysis. Again, developing the noise figure expression for the inverting amplifier configuration is simply a matter of resolving N_a and N_i and placing these expressions into *Equation (1)*. Knowing that the input impedance is matched to R_S, 1/2 of the noise voltage attributed to R_S will be delivered to the input port of the amplifier. This yields a (voltage) 2 at the input.

Inverting Op Amp Noise Figure

(Continued)

$$e_I^2 = \left(\frac{1}{2}e_S\right)^2 = \frac{1}{4}4kTR_S = kTR_S \quad (7)$$

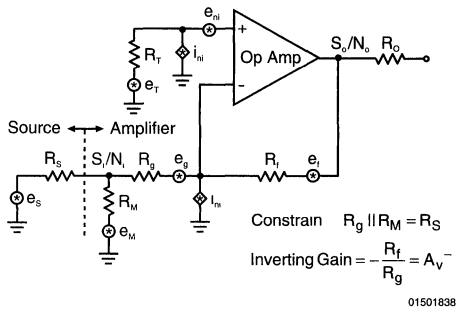

FIGURE 29. Inverting Op Amp Noise Figure Analysis

Table II shows each individual noise terms, except e_s, with each term's "gain" to the inverting input. The noise terms on the non-inverting input have a gain of A_t to the inverting input. This represents the non-inverting gain to the output divided by the inverting gain back to the inverting input. The two resistor noise terms for R_M and R_g are taken to have a voltage gain to the inverting input defined simply by the resistor divider networks and simplified with the constraint on R_M that it is to be set to yield $R_g \| R_M = R_S$. It is, perhaps, easiest to confirm the gain equations for R_g 's and R_M 's noise by computing the current those voltages generate into R_g , taking this current to the output by multiplying by R_f and then reflecting back to the inverting input by dividing by A_v - = R_f /R_g . Doing this and then substituting in for R_M , as shown in Table II, will (with some manipulation) yield the simple gain expressions found in Table II. The inverting noise current and R_f noise voltage are taken to the output then reflected back to the inverting input by dividing by the inverting gain.

TABLE 2. Noise Terms Contributing to N_a for the Inverting Op Amp Configuration

Noise Source	Value	Voltage Gain to Input
Non-inverting input voltage noise	e_n	A_T
Non-inverting input current noise	in_i	$R_T A_T$
Non-inverting input source resistor noise	$\sqrt{4kT/R_T}$	A_T
Inverting input current noise	i_i	$\frac{R_f}{A_V^-}$
Inverting input impedance matching resistor noise	$\sqrt{4kT/R_M}$	$\frac{1}{2}\left[1 - \frac{R_f}{A_V^-}\right]$
Gain setting resistor	$\sqrt{4kT/R_g}$	$1 - \frac{1}{2}\frac{R_s}{R_g}$
Feedback resistor voltage noise	$\sqrt{4kT/R_f}$	$\frac{1}{A_V^-}$

where:

$$A_v^- = \frac{R_f}{R_g} \text{ and } A_T = \frac{1 + A_v^- \left(1 - \frac{1R_S}{2R_g}\right)}{A_v^-}$$

$$\text{For } A_v^- > \sqrt{\frac{2R_f}{R_S}}, A_{T<1}$$

$$R_M = \frac{R_g R_S}{R_g - R_S} \text{ to get } R_M \| R_g = R_S$$

The noise terms on the non-inverting side of the op amp have a gain of A_T to the inverting input. As A_v^- increases, this gain drops to < 1, which contributes to the lower noise figure achievable using the inverting amplifier configuration. Again, an expression for a noise (voltage) 2 at the input may be obtained by taking the sum of the squared product of each noise source and associated gain shown in Table II.

$$e_a^2 (e_n A_T)^2 + (i_m R_T A_T)^2 + 4kTR_T A_T^2 + \left(\frac{i_I R_f}{A_v}\right)^2 +$$

$$4kTR_m \left(\frac{1}{2}\left(1 - \frac{R_S}{R_g}\right)\right)^2 + 4kTR_g \left(1 - \frac{1R_S}{2R_g}\right)^2 + \frac{4kTR_f}{(A_v^-)^2}$$

Combining the two noise powers attributed to the input matching network will allow considerable simplification in the final inverting noise figure expression. Substituting in for R_M with the expression shown as part of Table II and expanding the squared gain expressions.

$$\frac{4kTR_g R_S}{R_g - R_S}\left[\frac{1}{4}\frac{(R_g - R_S)^2}{R_g^2}\right] + 4kTR_g \frac{1}{4}\left(2 - \frac{R_S}{R_g}\right)^2 =$$

$$kTR_S\left(1 - \frac{R_S}{R_g}\right) + kTR_S\left[4\frac{R_g}{R_S} - 4 + \frac{R_S}{R_g}\right] = kT\left(4R_g - 3R_S\right)$$

Putting this back into the inverting e_a^2 expression and grouping the non-inverting input noise terms together yields:

$$e_a^2 = \left(e_n^2 + (i_{ni}R_T)^2 + 4kTR_T\right)A_T^2 + \left(\frac{i_I R_f}{A_v^-}\right)^2 + kTR_S\left(4\frac{R_g}{R_S} - 3\right) + \frac{4kTR_f}{\left(A_v^-\right)^2} \quad (8)$$

Putting the expressions for inverting e_a^2 and e_i^2 (*Equation (8)* and *Equation (9)*) back into the noise figure expression (Equation 1), and recognizing that dividing each term by R_S will yield N_a and N_i respectively, shows that the kTR_s term that arose in e_a^2 from the R_M and R_g resistor noises will collapse to a simple term, not including kTR_s (very reminiscent of the "2" appearing in the NF+ expression). One difference is that this part of the expression includes the contribution of both R_M and R_g, while the non-inverting equation kept the R_g noise as part of the equivalent input noise. This arises since R_g is now constrained by the input impedance matching requirement and can, therefore, be taken into this simplified form. The inverting noise figure NF- is then:

$$NF^- = 10\log\left(2\left(2\frac{R_g}{R_S} - 1\right) + \frac{(e_n^2 + (i_{ni}R_T)^2 + 4kTR_T)A_T^2 + \left(\frac{i_I R_f}{A_v^-}\right)^2 + \frac{4kTR_f}{(A_v^-)^2}}{kTR_S}\right) \quad (9)$$

To compare the non-inverting noise figure expression (*Equation (7)*) to the inverting expressions (*Equation (9)*), note that noise terms on the non-inverting input side have a gain of 1 for the non-inverting configuration but a gain of A_t for the inverting. Also note that the term associated with the feedback resistor noise is divided by simply A_v^+ in the non-inverting case. This arises because it also includes the R_g noise in the non-inverting expression. However, it is divided by $(A_v^-)2$ in the inverting case. This arises from the R_g noise term being considered part of the input termination. In this case, R_g and R_M's noise, appears in $2*(2*R_g/R_s - 1)$ as part of the noise figure expression. Note that this collapses to simply equal 2 when $R_g = R_s$ similar to the NF+ case.

At low inverting gain, the non-inverting input noise terms have a larger impact for the inverting configuration than for an equivalent non-inverting gain, yielding a higher noise figure. As A_v^- increases, however, the non-inverting noise terms will be attenuated in going to the inverting signal input reference point, yielding a lower inverting noise figure than for an equivalent gain non-inverting configuration.

Figure 30 compares the noise figures over gain for the non-inverting vs. inverting configurations using the CLC404. For this comparison, R_f is assumed fixed at 500Ω, R_T for the non-inverting case = 50Ω; but is set to 25Ω for the inverting case. With these constraints, R_g and R_M will be set by the desired gain and the requirement that $R_g \| R_M = R_S$ in the inverting mode. R_S is assumed = 50Ω throughout. The inverting noise figure plot simply stops at the point where R_g = 50Ω, since higher gains are not possible (with a fixed R_f) while retaining the input impedance matching requirement. Also note that log gains are shown on the x-axis to the matched load, while the voltage gains used in the noise figure calculations are the linear voltage gains to the output pin.

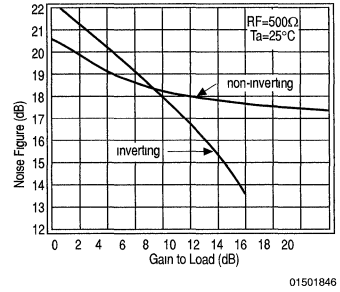

FIGURE 30. Noise Figure vs. Gain For the CLC404

Dynamic Range Calculation

Having developed the 3 limits to dynamic range commonly used in describing RF amplifiers as they apply to op amps, it is now possible to combine them into a single dynamic range number. The usable dynamic range is typically described in terms of the difference between the minimum detectable signal at the amplifier output and either the -1dB compression or the output power that would bring the 3rd order spurious up to this minimally detectable level. As described in reference 5 (page 175) the minimally detectable signal at the output of an amplifier is:

$Po_{MDS} = kTG_A(NF)BX$

Dynamic Range Calculation

(Continued)

where:

kT →	Noise power delivered to matched input in dBm
GA →	Power gain in dB
NF →	Noise Figure
B →	Noise bandwidth
X →	Additional margin above the noise floor for detectability; typically 3dBm

Note that the kTGA(NF) term solves to yield the spot output noise power Substituting for NF and recalling that k_T = noise power delivered to the input matching resistor = N_I.

$$kTG_A(NF) = N_I G_A \left[\frac{S_I/N_I}{S_O/N_O}\right] = N_O G_A \frac{S_I}{S_O} = N_O$$

Adding 10*log(B) will then show the integrated noise floor at the output of the amplifier. It is important to remember that this bandwidth need not be the bandwidth of the amplifier itself It is advantageous to bandlimit the response as narrowly as possible at some point after the amplifier immediately prior to the desired signal extraction. It is this later bandlimiting bandwidth that would be used in the equation for determining the minimum detectable signal

As an example, consider the CLC404 circuit used throughout this discussion with a post-filter to yield a bandwidth of interest from 10MHz to 20MHz. The non-inverting, gain of 9.54dB topology would yield a minimum detectable power level at the output:

$$Po_{MDS} = 10\log(kT) + 10\log(G_A) + NF + 10\log(10MHz) + 3db = -174dBm + 9.54dB + 18dB + 70dB + 3dB = -73.5dBm$$

Where the noise figure was read off of *Figure 30* and

$$10\log\left(\frac{kT}{.001}\right) = 10\log(1000(4E-21)) = -174dBm.$$

Having determined the minimally detectable signal, at the output, a maximum output signal set by some constraint will determine the dynamic range Typically, a simple dynamic range specification uses the -1dB compression power as the maximum output power From the earlier discussion on -1dB compression, we know that the actual output power at the fundamental frequency is -1dBm less than the reported -1dB compression point, and, that the true achievable sinusoidal power is approximately 2.1dBm less than this due to increase in power showing in the fundamental when the output is approaching a square wave. With these considerations, it would seem more realistic to use a maximum output power 3dBm less than the measured -1dB compression power. Going to *Figure 17* and subtracting 3dBm from the measured -1dB compression at the maximum operating frequency will yield a maximum usable output power at the matched, load of 14.5dBm. Subtracting the minimum detectable signal at the output from this shows a 14.5 – (-73.5) = 88dB dynamic range.

An alternative approach is to define a spurious free dynamic range. This approach sets the maximum output power to yield a 3rd order spurious level equal to the minimum detectable signal At this point, the amplifier generated spurious is just equalling what can be detected from a noise floor consideration. From *Figure 23*, the 3rd order spurious levels are:

$$P_S = 2\left(\frac{3}{2}P_O - IM3\right)$$

Setting this equal to the minimum detectable signal and solving for P_O –

$$P_S = 2\left(\frac{3}{2}P_o - IM3\right) = -174dBm + 10\log G_A + 10\log(B) + 3dB$$

$$P_{O\,max} = \frac{1}{3}\left[-174dBm + 10\log G_A + NF + 10\log(B) + 3dB + 2(IM3)\right]$$

Putting in the previously develop minimum detectable signal and pulling the 20MHz intercept from *Figure 24* shows a maximum spurious free output power of –

$$P_{O_{max}} = \frac{1}{3}\left[-73.5 + 2(28)\right] = -5.8\,dBM$$

and a spurious free dynamic range of:

DRf = -5.8dBm – (-73.5dBm) = 67.7dB

An additional check on this spurious free dynamic range is to recall that the total output power for the equal power 2-tone condition (that will generate the spurious level at the minimum detectable signal) is actually a voltage envelope that is twice the individual signals, or, 6dBm higher in power. This would imply a 0dBm total output power when the spurious is just rising above the noise floor. This is well below the dynamic range set by the -1dB compression limit.

Another way to interpret the 3rd order spurious plot of *Figure 24* is to compute the absolute spurious power level as the output power is swept higher and simply compare that to the minimum detectable signal power at the output. The absolute spurious power can be derived from the data of *Figure 24* as simply the x-axis value minus the y-axis value, (P_O -(P_O - P_S)) = P_S . When the measured spurious free range is in a region of -1 slope (2→4dBm on the 20MHz line), P_S is remaining constant as the output power increases. Using the actual measured data, as opposed to an intercept, can become a more appropriate way to compare the spurious power to the noise floor when the spurious level begins to level out and become constant (for a part like the CLC404) just below the minimum detectable signal.

For example, if the minimum detectable signal were actually -68dBm in the example considered earlier, the 3rd order spurious would equal this level at 4dBm output power instead of the -4dBm level that would be predicted from the equation used above with the low power estimate of a 28dBm intercept. Increasing the amplifier gain by 6dB would raise the output noise floor to -67.5 to take advantage of this improved spurious performance at higher output powers. Doing this would actually yield a 72dB spurious free dynamic range vs. the 68dB calculated earlier.

The primary determinants to dynamic range are noise power bandwidth, noise figure, -1dB compression, and 2- tone, 3rd order spurious. To maximize dynamic range, the following steps may be taken –

Dynamic Range Calculation
(Continued)

1. Limit the noise power bandwidth after the amplifier as much as possible.
2. To reduce noise figure, run the amplifier at as high a gain as possible consistent with bandwidth limitations and/or use the amplifier at high inverting gains. Alternatively, using a transformer coupled non-inverting amplifier configuration as described in National application note OA-14 can typically reduce the noise figure to the 6dB level.
3. If the -1dB compression limits are inadequate, use a higher supply voltage amplifier (such the hybrid amplifiers offered by National), or, increase the power supply voltage above the recommended value. National's low voltage monolithic amplifier's specify a maximum voltage across the supply pins of 14 volts. Increasing the supplies from ±5V to ±6V (or using a single 12V supply and the single supply circuits described earlier) will typically increase the maximum usable output power by 2dBm.
4. Be sure to consider the actual spurious performance if an intercept characteristic is not followed. Increasing the supply current (if possible) or increasing the load impedance can dramatically drop the 3rd order distortion terms. Recall that the feedback network remains as an upper limit on the output loading. Reference 4 describes an additional technique of loop gain shaping that can be used to further improve the distortion performance.

Conclusions

High speed current feedback amplifier's can offer considerable performance advantages when used in IF and RF applications. The flexible gain and I/O impedance capability can be used to the designers benefit in tailoring the amplifier to the specific requirement. Last minute gain changes can be accommodated with resistor value changes as opposed to requiring a new amplifier. Exceptional I/O VSWR and reverse isolation are easily attainable using wideband op amps. Although somewhat different, the dynamic range can be calculated, or measured, and compared between op amps and more typical RF amplifiers.

One of the most significant advantages of wideband current feedback amplifiers is the low 3rd order spurious level for their relatively low quiescent power dissipation. Most of National's monolithic amplifier's dissipate less than 150mW while delivering in excess of 40dBm intercepts below 10MHz. The primary drawback to the closed loop op amps are their rapid rolloff in distortion performance as the loop gain decreases at higher frequencies. Another area for improvement are the relatively high noise figures using standard op amp topologies. Using an input transformer can reduce the overall noise figure to around 6dB (see National application note OA-14). Additional external circuit techniques, along with a new low noise op amp (the CLC425), show a potential for noise figures as low as 2dB. For IF and RF applications below 100MHz, and particularly below 50MHz (when a high spurious free dynamic range is required), a wideband op amp solution can probably offer significant performance, power dissipation, and price advantages over more typical fixed gain amplifiers. Appendix A summarizes the comparison between RF amplifiers and wideband op amps.

References:

1. Hewlett Packard Application Note 154 "S-Parameter Design".
2. "Error Models for Systems Measurement", Jim Fitzpatrick, MicroWave Journal, May, 1978.
3. Passive and Active Network Analysis and Synthesis, Aram Budak; Houghton, Miflin, 1974.
4. "Pushing Low Quiescent Power Op Amps to Greater than 55dBm 2-Tone Intercept, and an Automated, Very Wide Dynamic Range System to Measure these Exceptionally Low Spurious Levels.", Michael Steffes, National Application Note, OA-22.
5. Microwave Transistor Amplifiers: Analysis and Design, Guillermo Gonzalez; Prentice Hall, Inc., 1984.

The circuits included in this application note have been tested with National Semiconductor parts that may have been obsoleted and/or replaced with newer products. Please refer to the CLC to LMH conversion table to find the appropriate replacement part for the obsolete device.

Note: The circuits included in this application note have been tested with National Semiconductor parts that may have been obsoleted and/or replaced with newer products. Please refer to the CLC to LMH conversion table to find the appropriate replacement part for the obsolete device.

Appendix A
Amplifier Comparison Table

Parameter	RF Amplifiers	National Semiconductor Op Amps
Gain	Almost always fixed gain	Easily adjustable over wide range
Bandwidth	Limited capacity < 1MHz. Can be very high frequency. Generally, 2 decade range .	DC capability. Upper limit around 100MHz to match RF amp flatness specs
I/O VSWR	Typically 1.5:1	Can be tuned to much better match through 100MHz than RF amps
Reverse Isolation	20 to 30dB considered good. Not too frequency dependent.	Much better isolation possible degrades at high frequencies. Better non-inverting than inverting.
Noise Figure	Can be very low 2 to 5dB typical	Varies with gain setting. Higher gains better but bottoming out about 12dB for typical op amp. Circuit can be improved to < 5dB

Appendix A
Amplifier Comparison Table (Continued)

Parameter	RF Amplifiers	National Semiconductor Op Amps
3rd Order	Moderate levels, needs high I_{cc} for excellent numbers. Relatively frequency independent.	Very good intercepts for quiescent power. Strong frequency dependent-degrading rapidly at Can be improved at low frequencies. See App. Note OA-22.
−1dB Compression	Good levels for voltage supplies. Relatively frequency independent. -1dB + 3rd intercept are order related.	Requires more head room for available output power. Drops rapidly with frequency due to slew rate -1dB and 3rd order not related.
Supply Current	Usually single polarity supply. High quiescent current vs. PoCapability.	Bi-polar supplies Almost all can be run single supply. Much lower quiescent currents for PoCapability.

Appendix B
Harmonic & Intermodulation Terms for a 5th Order Polynomial Transfer Function

For an input signal that is two sinusoidal signals

$V_i = A\cos 2\pi f_1 t + B\cos 2\pi f_1 t$

$f_1 = f_o - \Delta f$

$f_2 = f_o - \Delta f$

Processed through a 5th order polynomial transfer function

$V_o = K_o + K_1 V_i + K_2 V_i^2 + K_3 V_i^3 + K_4 V_i^4 + K_5 V_i^5$

yields the following frequencies and coefficients:

Frequency terms and coefficients in order of ascending frequency

Frequency	Coefficient	
DC	$K_O + K_2 (A^2/2 + B^2/2) + K_4 (3/8 * A^4 + 3/8 * B^4 + 3/2 * A^2B^2)$	
$2\Delta f$	$(K^2 + AB/2) + 2K_4 (A_3B + AB^3) + 5/4 * K_5 (A^4B + AB^4)$	2nd Order Intermod
f_0	$K_5 * 10/16 * A^3B^2$	5th Order Intermod
$f_0 - 3\Delta f$	$K_3 * 3/4 * AB^2 + 30/16 * K_5A^2B^3$	3rd Order Intermod
$f_0 - \Delta f (=f_1)$	$K_1 + K_3 (3/4 * A_3 + 3/2 * A^2B) + K_5 (5/8 * A^5 + 30/8 * A^3B^2 + 15/8 * AB^4)$	Lower Test Tone f_1
f_0	No coefficient	
$f_0 - \Delta f (=f_2)$	$K_1 + K_3 (3/4 * B_3 + 3/2 * AB^2) + K_5 (5/8 * B^5 + 30/8 * A^2B^3 + 15/8 * A^4B)$	Upper Test Tone f_2
$f_0 + 3\Delta f$	$K_3 * 3/4 * A^2B + 30/16 * K_5A^3B^2$	3rd Order Intermod
$f_0 + 5\Delta f$	$K_5 * 10/16 * A^2B^3$	5th Order Intermod
$2f_0 + 4\Delta f$	$2K_4A^3B$	4th Order Intermod
$2f_0 + 2\Delta f (=2f_1)$	$K_2 * A_2/2 + K_4 * A^4/2 + 3/2 * K_4A^2B^2$	2nd Harmonic for f_1
$2f_0$	$K_2 * AB/2 + 2K_4 (A^3B + AB^3) + K^5 * 5/4 * (A^4B + AB^4)$	2nd Order Intermod
$2f_0 + 2\Delta f (=2f_2)$	$K_2 * B^2/2 + K_4 * B^4/2 + 3/2K_4A^2B_2$	2nd Harmonic for f_2
$2f_0 + 4\Delta f$	$2K_4AB^3$	4th Order Intermod
$3f_0 - 5\Delta f$	$5/16 * K_5A^4B$	5th Order Intermod
$3f_0 - 3\Delta f (=3f_1)$	$K3/4 * A^3 + K_5/16 * A^5$	3rd Harmonic for f_1
$3f_0 - \Delta f$	$3/4 * K_3AB^2 + 30/16 * K_5A^2B^3$	Higher 3rd Order Intermod
$3f_0$	No Coefficient	
$3f_0 - \Delta f$	$3/4 * K_3A^2B + 30/16 * K_5A^3B^2$	Higher 3rd Order Intermod
$3f_0 - 3\Delta f (=3f_2)$	$K3/4 * B^3 + K_5/16 * B^5$	3rd Harmonic for f_2
$3f_0 - 5\Delta f$	$5/16 * K_5AB^4$	5th Order Intermod
$4f_0 - 4\Delta f (=4f_1)$	$1/8 * K_4A_4$	4th Harmonic for f_1
$4f_0 - 2\Delta f$	$2K_4A^3B$	4th Order Intermod
$4f_0$	No Coefficient	

Appendix B
Harmonic & Intermodulation Terms for a 5th Order Polynomial Transfer Function (Continued)

$4f_0 - 2\Delta f$	$2K_4AB^3$	4th Order Intermod
$4f_0 - 4\Delta f$ (=$4f_2$)	$1/8 * K_4B^4$	4th Harmonic for f_2
$5f_0 - 5\Delta f$ (=$5f_1$)	$1/16 * K_5A^5$	5th Harmonic for f_1
$5f_0 - 3\Delta f$	$5/16 * K_5A^4B$	5th Order Intermod
$5f_0$	No Coefficient	
$5f_0 - 3\Delta f$	$5/16 * K_5AB^4$	5th Order Intermod
$5f_0 - 5\Delta f$ (=$5f_2$)	$1/16 * K_5B^5$	5th Harmonic for f_2

Noise Analysis for Comlinear Amplifiers

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OA-12
Kumen Blake

Abstract

This App Note covers the noise model for all current-feedback op amps, simple design techniques and useful approximations. This is a frequency-domain model to simplify circuit analysis and design. This information simplifies the selection of a low-noise current-feedback op amp.

This revision obsoletes the previous revision of this App Note, and covers additional material.

Contents

The subjects covered are:

- The noise model for current-feedback op amps
- Converting noise densities to integrated noise
- Interpreting integrated noise as SNR
- Output noise improvement
- 1/f noise calculations
- SPICE models
- A design example
- A derivation of the Noise Power Bandwidth approximation (Appendix A)
- A bibliography (Appendix B)

Scope of Noise Analysis

The noise analysis in this App Note deals with random noise generated by the devices and components in a circuit. Noise analysis gives the greatest benefit when:

- The signal level is low
- The signal to noise ratio (SNR) is high
- The signal sees a substantial gain

Noise analysis will not help:

- Identify and eliminate oscillation or instability problems
- Reduce EMI (Electro-Magnetic Interference)
- Reduce cross talk

Noise Model

Three input-referred noise density (spot noise) sources model the noise generated by current-feedback (CFB) op amps. Noise power density (en^2 or in^2) is the power measured in a narrow bandwidth, normalized to the load resistance, in units of V^2/Hz or A^2/Hz. Voltage noise density (e_n) and current noise density (I_n) are the square-root of noise power density in units of $V/\sqrt{Hz}$ or $A/\sqrt{Hz}$. Notice that these noise densities are functions of frequency.

Figure 1 shows the three input noise density sources, e_{ni}^2 , i_{bn}^2 and I_{bi}^2 , in a standard amplifier circuit. The specifications give densities that are constant over frequency (white noise). Ground R_T for inverting gain circuits, and ground R_g for non-inverting gain circuits

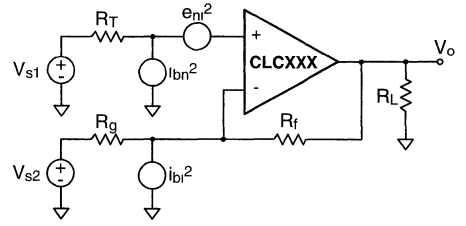

FIGURE 1. CFB Noise Model

The equation for the output voltage noise density is (1)

$$e_{no}^2 = G_n^2 \cdot \left(e_{ni}^2 + \left(i_{bn} R_T \right)^2 + 4kT\left(R_T + \left(R_f \,\|\, R_g \right) \right) \right) + \left(i_{bi} R_f \right)^2 + \left(e_{ns1} G_n \right)^2 + \left(e_{ns2} \left(G_n - 1 \right) \right)^2$$

where:

- $G_n = 1 + \frac{R_f}{R_g}$
- e_{no} is the voltage noise density ($V/\sqrt{Hz}$) seen at V_o
- e_{ni} is the op amp's input voltage noise density ($V/\sqrt{Hz}$)
- i_{bn} and i_{bi} are the op amp's input current noise densities ($A/\sqrt{Hz}$)
- $4kT = \left(16.0 \times 10^{-21} J \right) \cdot \frac{T}{290°K}$, T is the temperature in K
- e_{ns1} and e_{ns2} are the voltage noise densities ($V/\sqrt{Hz}$) produced by V_{S1} and V_{S2}

The load resistor (R_L) has a negligible contribution to the noise because the output resistance of the op amp is very small.

The system transfer function will shape the output noise. See **References [1 & 2]** in **Appendix B** for information on how to generate noise transfer functions. The *1/f Noise* section covers excess noise (noise that exceeds the white noise specifications).

Integrated Noise

Convert the output voltage noise density to the integrated output voltage noise by integrating over frequency:

$$E_{no} = \sqrt{\int_0^{\infty} e_{no}^2 \left| H_{eno}(jf) \right|^2 df} = e_{no} \cdot \sqrt{NPBW}$$

$$NPBW \approx 1.3 \cdot f_2 - 0.8 \cdot f_1$$

where:

- H_{eno} (jf) is the noise transfer function for e_{no}
- f_1 is the lower -3dB corner frequency for AC-coupled systems, or the lowest frequency that affects your system's performance
- f_2 is the upper -3dB corner frequency
- The NPBW (Noise Power Bandwidth) approximation holds when:
- there is ≤ 3dB of gain peaking
- $f_1 << f_2$
- If the NPBW approximation does not hold, use numerical integration instead

The integrated output noise, E_{no} , is the standard deviation of the output noise in units of V_{rms} . It is also a measure of the lower end of the useful dynamic range. Because integrated output noise depends on the circuit architecture, component values and the op amp, **it is best to compare op amps based on the input noise densities**

To see how each noise source contributes to E_{no} , integrate

$$E_{no}^2 = \int_0^{\infty} G_n^2 e_{ni}^2 \left| H_{eni}(jf) \right|^2 df + \int_0^{\infty} G_n^2 i_{bn}^2 R_f^2 \left| H_{ibn}(jf) \right|^2 df + \ldots$$

This information is useful for improving the amplifier's SNR.

Dynamic Range

Signal to noise ratio (SNR) describes how much dynamic range a signal has. It compares the lower end of the useful dynamic range (E_{no}) to the signal magnitude (in units of V_{rms}). The input and output signal to noise ratios are:

$$SNR_{in} = 20\log\left(\frac{V_{in(rms)}}{E_{nin}}\right), dB$$

$$SNR_o = 10\log\left(\frac{V_{o(rms)}^2/R_L}{E_{no}^2/R_L}\right) = 20\log\left(\frac{V_{o(rms)}}{E_{no}}\right), dB$$

where:

- $V_{in(rms}$ is the signal voltage at the input (V_{S1} or V_{S2}), V_{rms}
- E_{nin} is the integrated voltage noise at the input (at V_{S1} or V_{S2}), V_{rms}
- $V_{o(rms)}$ is the signal voltage at the output, V_{rms}
- E_{no} is the integrated voltage noise at the output, V_{rms}

Improving Output Noise

To reduce output noise, do the following:

- Band-limit the signal after the op amp to limit the final output noise
- AC couple when possible
- Use a low-pass filter, or a band-pass filter
- Reduce gain peaking to lower the NPBW
- Reduce resistor values to lower thermal noise, but keep in mind that:
- R_f values smaller than that recommended in the datasheet will cause gain peaking and increased bandwidth; **the NPBW may increase faster than the intended noise reduction**
- Smaller loads at the op amp's output increase distortion and power consumption
- Resistors connected to the input of current-sensing amplifiers act as current noise sources; **increase these resistor values to reduce thermal noise**

For those op amps with an adjustable supply current, the input noise sources change with supply current. As the supply current increases, the input voltage noise decreases, the input current noises increase, the distortion improves and the bandwidth increases. For the best voltage noise performance, use the highest supply current. For the best current noise performance, use the lowest supply current.

1/f Noise

At low frequencies, the three input noise density terms are larger than predicted by the specifications. The dominant source of this excess noise is 1/f (or flicker) noise. Burst noise also contributes to excess noise, but is not covered in this App Note. The input noise sources, with both the 1/f noise and white noise terms included, are:

$$e_{ni}^2(f) = e_{ni}^2\left(1 + \frac{f_{c(eni)}}{f}\right)$$

$$i_{bn}^2(f) = i_{bn}^2\left(1 + \frac{f_{c(ibn)}}{f}\right)$$

$$i_{bi}^2(f) = i_{bi}^2\left(1 + \frac{f_{c(ibi)}}{f}\right)$$

where:

- $e_{ni}^2(f)$ is the sum of the white noise term, e_{ni}^2, and the 1/f noise term, $e_{ni}^2 \frac{f_{c(eni)}}{f}$
- $f_{c(eni)}$ is the corner frequency of the 1/f noise for $e_{ni}^2(f)$; this is the point where $e_{ni}^2(f)$ doubles its white noise value
- the other input noise terms are defined similarly

Notice that flicker noise power density is proportional to 1/f; flicker voltage noise density and flicker current noise densities are proportional to 1/√f.

To integrate both white noise and 1/f noise, evaluate individual noise terms separately. For each term we obtain:

$$E_n^2 = \int_0^{\infty} e_n^2\left(1 + \frac{f_c}{f}\right)\left| H_{en}(jf) \right|^2 df = e_n^2 \ NPBW$$

$$NPBW \approx (1.3 \cdot f_2 - 0.8 \cdot f_1) + NPBW_{1/f}$$

$$NPBW_{1/f} \approx f_c \ \ln\left(\frac{f_2}{f_1}\right)$$

The 1/f noise contribution is negligible when $f_2 >> f_c$. f_1 is the largest frequency that does not affect your system's performance when the amplifier is DC-coupled.

Use metal-film resistors to minimize 1/f noise.

SPICE Models

SPICE models are available for most of Comlinear's amplifiers. These models support AC noise simulations at room temperature. We recommend simulating with Comlinear's SPICE models to:

- Predict a better value for NPBW
- Support quicker design cycles

To verify your simulations, we recommend breadboarding your circuit. Evaluation boards are available for building and testing Comlinear's amplifiers.

Design Example

This design example demonstrates the noise design of a simple circuit. The CFB op amp in this example is not an actual product; **the parameter values shown are arbitrary** and are for illustration purposes only.

This example uses the non-inverting gain amplifier in *Figure 2*. The components shown are:

- V_{S1} is the input voltage source (with very low output impedance). The signal at V_{S1} is $100mV_{rms}$, and the voltage noise e_{ns1} (at V_{S1}) is $3.0nV/\sqrt{Hz}$.
- A 50Ω coax cable is placed between the source and the amplifier
- R_{T1} = 50Ω to match the coax cable's impedance and prevent reflections
- R_{T2} prevents gain peaking, and filters the input signal with CT
- C_T filters the input signal (this reduces the signal's slew rate)
- R_f and R_g set the gain; the recommended R_f is 250Ω for a gain of 10
- R_L is 100Ω
- The op amp noise terms are:
- e_{nI} = $3.0nV/\sqrt{Hz}$ and $f_{c(enI)}$ = 1.0kHz
- i_{bn} = $2.0pA/\sqrt{Hz}$ and $f_{c(ibn)}$ = 5.0kHz
- i_{bI} = $12pA/\sqrt{Hz}$ and $f_{c(ibI)}$ = 10kHz
- Ambient temperature (T) is 25˚C
- Power dissipation of the op amp causes a 15˚C junction temperature rise

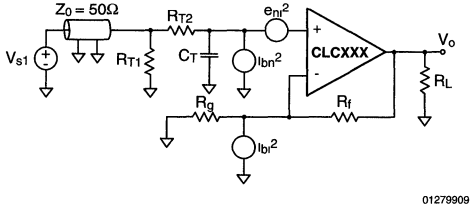

FIGURE 2. Non-Inverting Gain Amplifier

The design goals are:

- Provide a gain of 10 (= G_n for non-inverting gains)
- DC-couple the signal; the lowest frequency that affects system performance is 10Hz (f_1)
- Set an upper 3dB corner frequency of 10MHz (f_2)
- Achieve an output SNR of 74dB

The initial design choices we made are:

- 20MHz pole at the input set by C_T and R_{T2} (this will cause reflections in the coax cable for any signal above this pole)
- 10MHz filter after this amplifier (not shown); this will set f 2 (NPBW)
- R_{T2} = 1.0kΩ
- C_T = 8pF
- R_f = 250Ω, its recommended value, to avoid gain peaking
- R_g = 27.8Ω to set the gain to G_n = 10

The resulting junction temperature of the op amp, input integrated noise and input SNR are:

$$T = 25°C + 15°C = 40°C = 313°K$$

$$E_{ns1} = e_{ns1}\sqrt{NPBW}$$

$$\approx \left(3.0nV/\sqrt{Hz}\right)\sqrt{13MHz - 8Hz}$$

$$\approx \left(10.8\mu V_{rms}\right)^2$$

$$SNR_{in} \approx 79.3dB$$

R_{T1} does not contribute to the output noise; $V_{S1}$is a nearly ideal voltage source.

The input source produces an output noise of: The individual white noise contributions of the op amp to the output noise are:

$$G_n^2 \cdot e_{ns1}^2 \cdot NPBW \approx \left(108\mu V_{rms}\right)^2$$

The individual white noise contributes of the op amp to output noise are:

$$G_n^2\ e_{nI}^2\ NPBW \approx \left(108\mu V_{rms}\right)^2$$

$$G_n^2\ i_{bn}^2\ R_{T2}^2\ NPBW \approx \left(72\mu V_{rms}\right)^2$$

$$i_{bI}^2\ R_f^2 \cdot NPBW \approx \left(11\mu V_{rms}\right)^2$$

The individual 1/f noise contributions of the op amp to the output noise are:

$$G_n^2\ e_{nI}^2\ NPBW_{1/f} \approx (10)^2\left(3.0nV/\sqrt{Hz}\right)^2\left((1kHz)\ \ln\left(\frac{10MHz}{10Hz}\right)\right)$$

$$\approx \left(3.5\mu V_{rms}\right)^2$$

$$G_n^2\ i_{bn}^2\ R_{T2}^2\ NPBW_{1/f} \approx \left(5.3\mu V_{rms}\right)^2$$

$$i_{bI}^2\ R_f^2 \cdot NPBW_{1/f} \approx \left(1.1\mu V_{rms}\right)^2$$

The contributions of the other components to the output noise are:

$$G_n^2\ 4kTR_{T2}\ NPBW \approx (10)^2\left(4.2nV/\sqrt{Hz}\right)^2(13MHz - 8Hz)$$

$$\approx \left(150\mu V_{rms}\right)^2$$

$$G_n^2 \cdot 4kT\left(R_f \,||\, R_g\right) \cdot NPBW \approx \left(24\mu V_{rms}\right)^2$$

Design Example (Continued)

The resulting output integrated noise, output signal and output SNR are:

$$E_{no} \approx 227\mu V_{rms}$$
$$V_{o(rms)} = G_n V_{in(rms)} \approx 1.00V_{rms}$$
$$SNR_o \approx 72.9dB$$

Reduce R_{T2} to improve SNR; this has little impact on other performance parameters. Changing R_{T2} to 200Ω gives:

$$C_T = 40pF$$
$$E_{no} \approx 169\mu V_{rms}$$
$$SNR_o \approx 75.4dB$$

In an actual design, the next step would be SPICE simulations, then breadboarding the circuit.

Conclusions

The important points to remember when designing low noise circuits are:

- Employ noise analysis where small signals are present
- Select correct resistor values to reduce thermal noise
- Select op amps based on their input noise densities (integrated noise is circuit-dependent)
- Reduce NPBW and gain peaking to minimize integrated output noise
- Estimate your signal's dynamic range using SNR
- Simulate with Comlinear's SPICE models to estimate noise performance
- Build and measure your circuit to verify the design
- Refer to the **Bibliography** in **Appendix B** for additional background information

Appendix A

(derivation of Noise Power Bandwidth formula)

The goal is to estimate NPBW using common, easy to measure parameters: the -3dB bandwidth and gain peaking. We assume a second-order transfer function for the op amp circuit's high-frequency behavior:

$$H(s) = \frac{H_o}{1 + \frac{1}{Q}\cdot\frac{s}{\omega_o} + \frac{s^2}{\omega_o^2}}$$

$$|H(jf)| = \frac{H_o}{\sqrt{1 + \left(\frac{1}{Q^2} - 2\right)\left(\frac{f}{f_o}\right)^2 + \left(\frac{f}{f_o}\right)^4}}$$

$$s = j\omega = j2\pi f$$

where $\omega o = 2\pi f_o$ is the natural frequency of this transfer function.

Integrating the magnitude squared of the transfer function gives:

$$NPBW = \int_0^\infty |H(jf)|^2 df$$
$$= \frac{\pi}{2} Q\, f_o$$

Solving for the upper -3dB corner frequency (f_2), and substituting the result in the equation above, gives:

$$NPBW = \frac{\frac{\pi}{2}\cdot Q\, f_2}{\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}}$$

Gain peaking is easy to measure, and is a strong function of Q for large Q. It is easy to show that:

$$Q = \frac{H_{max}}{H_o}\,\frac{\sqrt{1 + \sqrt{1 - \frac{H_o^2}{H_{max}^2}}}}{\sqrt{2}},\ \frac{1}{\sqrt{2}} \le Q$$

where H_{max} is the peak gain magnitude.

These results support the following approximations:

$$NPBW \approx (1.3)\ f_2,\ \frac{H_{max}}{H_o} \le 1.5$$
$$\approx \frac{H_{max}}{H_o}\ f_2,\ 1.0 < \frac{H_{max}}{H_o}$$

with a 20% maximum error. This translates to a 0.8dB maximum error in the estimated SNR.

If the amplifier transfer function has a single pole response, it is easy to show that:

$$NPBW = (\pi/2)\cdot f_2,\ \text{Single pole transfer function}$$

High-order filters will have:

$$NPBW \approx f_2,\ \text{high-order filters}$$

The approximation formula includes both of these cases.

The above results hold for the lower corner -3dB frequency (f_1) with minor modifications. When the corner -3dB frequencies do not interact ($f_1 << f_2$), we obtain:

$$NPBW \approx (1\,3 \bullet f_2 - 0\,8 \bullet f_1),\ \frac{H_{max}}{H_o} \le 3.0dB$$

It is easy to extend this result when there is more than 3.0dB of peaking, but it is better to reduce the peaking, or to numerically integrate the output noise.

Appendix B (Bibliography)

[1] C. D. Motchenbacher and J. A. Connelly, **Low-Noise Electronic System Design, New York:** John Wiley & Sons, 1993.

[2] P. R. Gray and R. G. Meyer, **Analysis and Design of Analog Integrated Circuits,** 2nd Ed. New York: John Wiley & Sons, 1984.

[3] J. D. Gibson, **Principles of Digital and Analog Communications,** New York: Macmillan, 1989.

[4] A. B. Carlson, **Communication Systems: An Introduction to Signals and Noise in Electrical Communication,** 3rd Ed. New York: McGraw-Hill, 1986.

Appendix B (Bibliography) (Continued)

[5] P. Antognetti and G. Massobrio (Editors), **Semiconductor Device Modeling with SPICE,** New York: McGraw-Hill, 1988.

Note: The circuits included in this application note have been tested with National Semiconductor parts that may have been obsoleted and/or replaced with newer products. Please refer to the CLC to LMH conversion table to find the appropriate replacement part for the obsolete device.

Current Feedback Loop Gain Analysis and Performance Enhancement

National Semiconductor
OA-13
Michael Steffes

With the introduction of commercially available amplifiers using the current feedback topology by Comlinear Corporation in the early 1980's, previously unattainable gain and bandwidths in a DC coupled amplifier became easily available to any design engineer. The basic achievement realized by the current feedback topology is to de-couple the signal gain from the loop gain part of the overall transfer function. Commonly available voltage feedback amplifiers offer a signal gain expression that appears identically in the loop gain expression, yielding a tight coupling between the desired gain and the resulting bandwidth. This historically has led to the gain-bandwidth product idea for voltage feedback amplifiers. The current feedback topology transcends this limitation to offer a signal bandwidth that is largely independent of gain. This application note develops the current feedback transfer function with an eye towards manipulating the loop gain.

Current Feedback Amplifier Transfer Function Development

The equivalent amplifier circuit of *Figure 1* will be used to develop the non-inverting transfer function for the current feedback topology. The current feedback topology is also perfectly suitable for inverting mode operation, especially inverting summing applications. The non-inverting transfer function will be developed, in preference to the inverting, since the inverting transfer function development is a subset of the non-inverting.

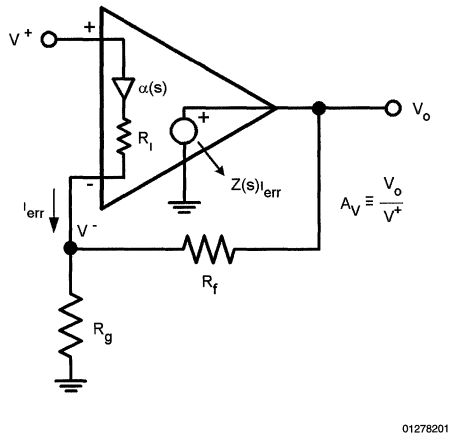

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FIGURE 1. Current Feedback Amplifier Internal Elements

The amplifier's non-inverting input presents a high impedance to the input voltage, V^+, so as to not load the driving source. Any voltage appearing at the input node is passed through an open loop, unity gain, buffer that has a frequency dependent gain, $\alpha(s)$. $\alpha(s)$ is very neatly equal to 1 at DC (typically .996 or higher, but always < 1.00) and typically has a −3dB point beyond 500MHZ. The output of the buffer ideally presents a 0Ω output impedance at the inverting input, V^-. It actually shows a frequency dependent impedance, Z_I, that is relatively low at DC and increases inductively at high frequencies. For this development, we will only consider that Z_I is a small valued resistive impedance, R_I. The intent of the buffer is to simultaneously force the inverting node voltage to follow the non-inverting input voltage while also providing a low impedance path for an error current to flow. Any small signal error current flowing in the inverting node, i_{err}, is passed through the buffer to a high transimpedance gain stage and on to the output pin as voltage. This transimpedance gain, Z(s), senses i_{err} and generates an output voltage proportional to it. Z(s) has a very high DC value, a dominant low frequency pole, and higher order poles. When the loop is closed, the action of the feedback loop is to drive i_{err} to zero much like a voltage feedback amplifier will drive the delta voltage across its inputs to zero. Z(s) ideally transforms the error current into a 0Ω output impedance voltage source.

Figure 2 steps through the transfer function development including the effect of R_I. This analysis neglects the impact of a finite output impedance from Z(s) to the output, output loading interactions with that output impedance, and the effect of stray capacitance shunting R_g.

Start by summing current at the V^- node of *Figure 1*

$$I_{err} + \frac{V_o - V^-}{R_f} = \frac{V^-}{R_g} \qquad \text{Eq 1}$$

We also know that,

$$V^- = \alpha(s)V^+ - I_{err} R_I$$

and, $I_{err} Z(s) = Vo$ then, $I_{err} = \frac{V_o}{Z(s)}$

Multiply equation 1 through by R_f and isolate V^-

$$R_f I_{err} + V_o = V^-(1 + R_f/R_g)$$

Now substitute in for I_{err} and V^- from above

$$\frac{R_f V_o}{Z(s)} + V_o = \left(\alpha(s)V^+ - \frac{R_I V_o}{Z(s)}\right)\left(1 + \frac{R_f}{R_g}\right)$$

Gather V_o terms and solve for V_o/V^+

$$\frac{V_o}{V^+} = \frac{\alpha(s)\left(1 + \frac{R_f}{R_g}\right)}{1 + \frac{R_f + R_I(1 + R_f/R_g)}{Z(s)}} \qquad \text{Eq 2}$$

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FIGURE 2. Current Feedback Amplifier Transfer Function

It is instructive to consider the separate part of Equation 2 separately.

$\alpha(S.) \rightarrow$ Frequency dependent buffer gain. Normally consider = 1

Current Feedback Amplifier Transfer Function Development

(Continued)

$1 + R_f/R_g \rightarrow$ Desired signal gain. Identical to voltage feedback non-inverting amplifier gain.

$$\frac{R_f + R_I\left(1 + \frac{R_f}{R_g}\right)}{Z(s)} = \frac{1}{\text{Loop Gain}}$$

$$\text{Hence, Loop Gain (LG)} = \frac{Z(s)}{R_f + R_I\left(1 + \frac{R_f}{R_g}\right)}$$

$$= \frac{\text{internal forward transimpedance}}{\text{feedback transimpedance}}$$

The loop gain expression is of particular interest here. If Z(s), the forward transimpedance, is much greater than $R_f + R_I$ (1 + R_f/R_g), the feedback transimpedance, (as it is at low frequencies) then this term goes to zero leaving just the numerator terms for the low frequency transfer function. As frequency increases, Z(s) rolls off to eventually equal the feedback transimpedance expression. Beyond this point, at higher frequencies, this term increases in value rolling off the overall closed loop response.

The key thing to note is that the elements external to the amplifier that determine the loop gain, and hence the closed loop frequency response, do not exactly equal the desired signal gain expression in the transfer function numerator. **The desired signal gain expression has been de-coupled from the feedback expression in the loop gain.**

If the inverting input impedance were zero, the loop gain would depend externally only on the feedback resistor value. Even with small R_I, the feedback resistor dominantly sets the loop gain and every current feedback amplifier has a recommended R_f for which Z(s) has been optimized. As the desired signal gain becomes very high, the $R_f(1 + R_f/R_g)$ term in the feedback transimpedance can come to dominate, pushing the amplifier back into a gain bandwidth type operation.

Understand the Loop Gain

It is very useful, and commonly done for voltage feedback amplifiers, to look at the gain graphically. *Figure 3* shows this for the CLC400, a low gain part offering DC to 200MHz performance What has been graphed is 20*log(|Z(s)|), the forward transimpedance gain, along with its phase, and 20 log(Z_t). **This Z, is the feedback transimpedance, $R_f + R_f(1 + R_f/R_g)$, and where it crosses the forward transimpedance curve is the frequency at which the loop gain has dropped to 1.** Note that the forward transimpedance phase starts out with a 180° phase shift, indicating a signal inversion through the part, and could have plotted as continuing to 360° or, shown, going to zero. Using these axis allows a direct reading of the phase margin at unity gain crossover.

As with any negative feedback amplifier, the key determinant of the closed loop frequency response is the phase margin at unity gain crossover. If the phase has shifted completely around to 360°, or dropped to zero on the axis used above when the loop gain has decreased to 1, unity gain crossover - (where the 20 log(Z_t) line intersects the 20 log(|Z(s)|) curve), the denominator in closed loop expression will become (1-1), or infinity (For the axis used above, the closed loop expression (Eq. 2) would have a 1-1/LG in the denominator. The form developed as Equation 2 accounted for the inversion with the sign convention for I_{err} and V_o).

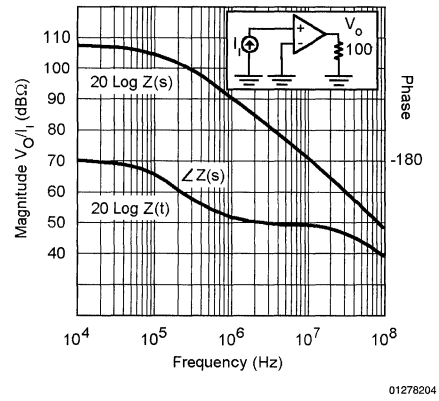


FIGURE 3.

It is critical for stable amplifier operation to maintain adequate phase margin at the unity gain crossover frequency. The feedback transimpedance that is plotted in *Figure 3* is $R_t + R(1 + R_f/R_g)$ evaluated at the specifications setup point for the CLC400. This yields:

$R_f = 250\Omega$	then
$A_V \equiv 1 + (R_f/R_g) = 2$	$Z_I = 250\Omega + 500\Omega(2) = 350\Omega$
	and
$Z_I = 50\Omega$	$20\log(350\Omega) = 50.9\text{dB}$

Looking at the unity gain crossover near 100MHz, we see somewhere in the neighborhood of a 60° phase margin. This is Comlinear's targeted phase margin at the gain and R_f used to specify any particular current feedback part. This phase margin, for simple 2 pole Z(s), yields a maximally flat Butterworth filter shape for the closed loop amplifier response (Q = .707). Note that the design targets reasonable flatness over a wide range of process tolerances and temperatures. This typically yields a nominal part that is somewhat overcompensated (phase margin > 60°) at room temperature.

Note that the closed loop bandwidth will only equal the open loop unity gain crossover frequency for 90° phase margins (single pole forward gain response). As the open loop phase margin decreases from 90°, with the impact of higher frequency poles in the forward transimpedance gain, the closed loop poles move off the negative real axis (in the s-plane) peaking the response up and extending the bandwidth. The actual bandwidth achieved by Comlinear's amplifiers is considerably beyond the unity gain crossover frequency due to these open loop phase effects

Controlling the Loop Gain

One of the key insights provided by the loop gain plot is what happens when Z_t is changed Decreasing Z_t (dropping the horizontal line of 20 log (Z_t)), will extend the unity gain crossover frequency but will sacrifice phase margin. This commonly seen in current feedback amplifiers when an er-

Controlling the Loop Gain (Continued)

roneously low R_f value is used yielding an extremely peaked frequency response. In fact a very reliable oscillator can be generated with any current feedback amplifier by using R_f = 0 in a unity gain configuration. Conversely, increasing Z_t (raising the horizontal line of 20 log(Z_t)) will drop the unity gain crossover frequency and increase phase margin. Increasing R_f is in fact a very effective means of over compensating a current feedback amplifier. Increasing R_f will decrease the closed loop bandwidth and/or decrease peaking in the frequency response.

Computing Z_t for the design point used in setting the specifications for any particular current feedback part indicates an optimum targeted feedback transimpedance under any condition.

In design, the internal Z(s) has been set up to yield a maximally flat closed loop response with the gain and R_f used to develop the performance specifications. if we then try to hold the same feedback transimpedance under different gain conditions, an option not possible with voltage feedback topologies, this optimum unity gain crossover for the open loop response can be maintained.

If we designate this optimum feedback transimpedance as Z_t*,

We would like to hold $R_f + R_i (1 + R_f/R_g) = Z_t$*

(where R_f and $1 + R_f/R_g$ are those values shown at the top of the part performance specification).

Substituting $A_v = 1 + R_f/R_g$, we get, $R_f = Z_t$* - R_iA_v (where R_f is a new value to be used at a gain other than the design point.) **Eq. 4**

This is a design equation for holding optimum unity gain crossover. Having computed R_f to hold $Z_t = Z_t$* $R_g/R_f/(A_v$ - 1) **Eq.5**

The Benefits of Controlling Z_t

As an example of adjusting R_f to hold a constant Z_t as the desired signal gain is changed, consider a CLC404 at gains of +2, +6 and +11.*Figure 4* shows test results over these gains for a fixed R_f very similar to low the CLC404 datasheet plots were generated.

Using the CLC404 design and specifications points (see Appendix 1)

A_v = +6

R_f = 500Ω

R_i = 30Ω

Z_t* = 500 + 30*6 = 680Ω

Figure 5 shows the same part operated with R_f adjusted as indicated by Equation 4. R_g in both cases is set using Equation 5.

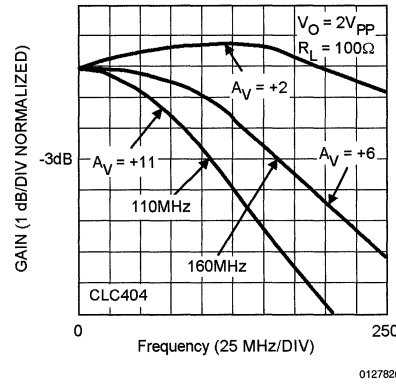


FIGURE 4. Frequency Response vs. Gain for R_f Fixed = 500Ω

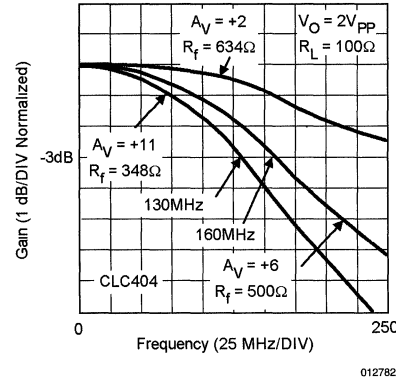


FIGURE 5. Frequency Response vs. Gain for Fixed Z_t = Z_t* = 680Ω

The results of *Figure 5* vs. *Figure 4* show that adjusting R_f does indeed hold a more constant frequency response over gain than a simple fixed R_f. The low gain response has flattened out while the high gain response has been extended.

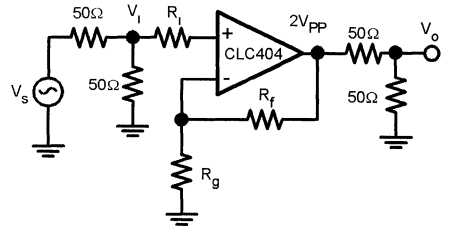
The remaining variability in frequency response can be attributed to 2nd order effects that have not yet been considered. As described in application Note OA-15, parasitic capacitance shunting the gain setting resistor, R_g, will introduce a response zero for non-inverting gain operation. This zero location can be easily located by substitution $R_g||C_g$ into the numerator part of the transfer function, Equation 2. This yields a zero at $1/(R_f||R_g)/C_g$ in radians. This

The Benefits of Controlling Z_t

(Continued)

effect would not be observed in inverting mode operation yielding a much more consistent response over gains, especially with R_f adjusted as shown above.

If we assume equal parasitic capacitances on the two inputs, we can cancel this zero by introducing a series impedance into the non-inverting input that equals $R_f||R_g$. *Figure 6* shows the test circuit and table of values used to test this for the same CLC404 used above. Note that we must include the equivalent source impedance of the source matching and termination resistors in (25Ω here). Note that the table shows actual standard values used, rather than the exact calculated values.



$R_f = 680 - A_V(30)$
$R_g = R_f / (A_V - 1)$
$R_I = (R_f || R_g) - 25\Omega$

A_V	R_f	R_g	R_I
+2	634	634	287
+6	500	100	56 2
+11	348	34	6

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FIGURE 6.

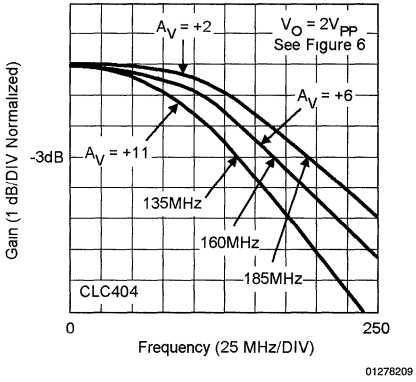

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FIGURE 7.

Figure 7 shows the measured frequency responses under the conditions tabulated in *Figure 6*.

Clearly, adding R_I has brought the low gain response to be much more consistent with the higher gains. Little effect was observed by adding R_I at gains of 6 and 11. Generally, adding R_I is particularly effective at flattening out the frequency response for higher gain parts, which are designed using high value of feedback resistors, when they are operated at low gains.

An alternative to adding R_I is simply to continue to increase R_f until the loop gain is overcompensated enough to cancel the zero. This is increasingly ineffective as the resistor values get larger but was developed empirically for the CLC414 and CLC415 quad amplifiers (Refer to datasheet for details). An alternative approach with those part would be to adjust R_f using the data from Appendix 1 and then add an R as described above.

Note that Equation 3 will predict negative R_f values as the desired gain exceeds Z_t^*/R_I. From a loop gain standpoint, this is exactly correct. However, additional concerns (particularly distortion and output current limits) will come in to limit the applicable range of gains for Equation 3. Generally, the total loading on the amplifiers should not be allowed to drop below 65Ω. This is the actual load in parallel with $R_f + R_g$ for the non-inverting configuration. For a 100Ω load, this limits the minimum $R_f + R_g$ to about 200Ω. Lower values can be used if R_L is greater. For inverting mode, which has exactly the same loop gain expression as non-inverting, R_f alone appears in parallel with R_L as an additional load. This would limit R_f to a minimum of 200Ω in inverting mode operation. This does not, of course, limit the amplifier's maximum gain. When a minimum R_f has been reached, R_g can continue to decrease, yielding higher gains, with a gain bandwidth characteristic eventually developing as the R_I (1 + R_f/R_g) part of Z_t comes to dominate.

Special Considerations for Variable Supply Current

The inverting input impedance, R_I, is essentially the output impedance of parallel/series combinations of emitter followers for most Comlinear amplifiers. Thus, R_I is some fraction or integer multiple of V_t/I_c, where V_t = kT/q and I_c is the bias current in those transistors. For lower power parts, and parts with adjustable supply current, R_I can get very large, as I_c decreases quickly putting the parts into a gain bandwidth type operation. Appendix 1 shows the nominal design point I_c, along with a room temperature R_I, and, for the adjustable supply current, I_{cc}. Anything that adjusts the total quiescent supply current from its nominal design point, changing power supply voltage, using the bias adjust pins on some parts, etc., will scale the I_c listed in Appendix 1 in direct proportion to I_{cc}.

Additional Loop Gain Control Applications

Recognizing that the inverting input impedance provides an opportunity to adjust the loop gain, without having any impact on the signal gain, we can add a resistor inside the loop that can act as an independent frequency response compensation element. This is very useful if a fine control over the frequency response shape is desired.

Using the same CLC404 used in the earlier tests (a part that is nominally overcompensated as shown by the rolloff at its gain of +6 condition in *Figure 4*), the circuit of *Figure 8* show an adjustment technique for the frequency response. Since we are intentionally adding R_I to the feedback transimped-

Additional Loop Gain Control Applications (Continued)

ance expression, Z_t, it is recommended to approximately set R_f to yield Z_t* when the adjustment to R_i is at midrange. This will yield a lower R_f as shown in*Figure 8. Figure 9* shows the original gain of +6 response of *Figure 4*, along with the response achieved with the circuit of *Figure 8* with R_p adjusted to yielded maximally flat frequency response. This circuit shows a ±.1dB gain flatness to beyond 100MHz.

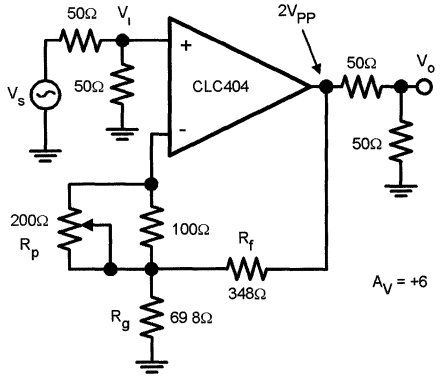


FIGURE 8. Adjustable Frequency Response

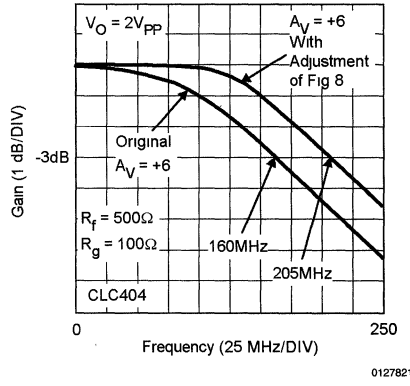


FIGURE 9. Frequency Response with Loop Gain Response

In inverting applications there is often times a conflict between the required gain setting resistors from an input impedance and signal gain standpoint, and what the amplifier would like to see from a loop gain phase margin standpoint. In a similar fashion to voltage feedback, in this case, an additional resistor to ground on the inverting input can be used to tune the loop gain independently of the inverting signal gain requirements. The drawback of this, is that, like voltage feedback, this increases the noise gain for the non-inverting input voltage noise.

Figure 10 shows an example of a transimpedance application using a CLC401 with a 1kΩ feedback resistor. In this case, the value of the feedback resistor is set by the desired signal gain, while R_g is used to satisfy the loop gain phase margin by setting the feedback transimpedance to Z* = 2.5k.

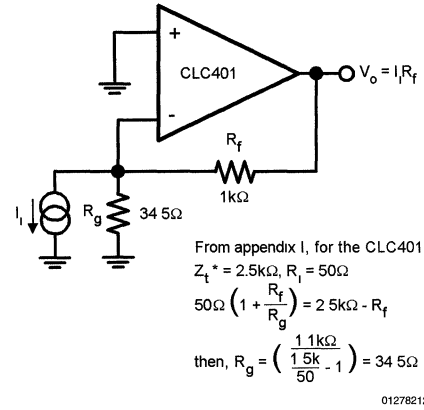


FIGURE 10.

Similarly, in an inverting summing application, once the desired gain and input impedance conditions are set, the loop gain can be independently controlled through the use of an additional resistor to ground on the inverting input. *Figure 11* shows an example of this using the CLC401 summing 5 channels, at a gain of −1 for each channel, using 1kΩ input resistors.

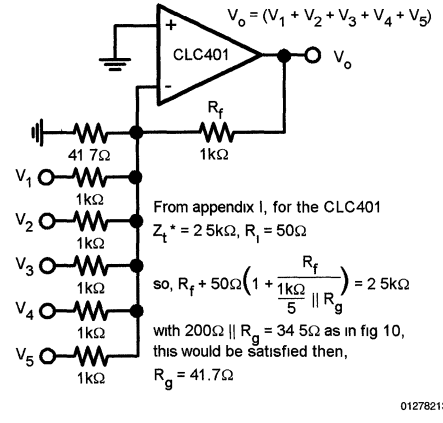


FIGURE 11. Loop Gain Adjusted in Inverting Summing Application

Conclusions

The current feedback topology has allowed us to de-couple the signal gain from the loop gain expressions. This provides ample opportunity for independent control of both the signal gains and the frequency response by using only resistive elements. A thorough understanding of the loop gain mechanisms provides the designer with a flexibility unavailable to the voltage feedback op amp

Appendix 1

The data tabulated here provide the necessary information to hold a constant feedback transimpedance over a wide range of closed loop signals gains for the current feedback amplifiers available from Comlinear at the time of this application note's publication. The data is broken into a set for the monolithic amplifiers, which generally have a higher R_i due to their lower quiescent bias current, and a set of data for the hybrid amplifier products.

The table entries show

1. $A_v \geq$ Non-inverting voltage gain used to set device specs
2. $R_f \geq$ Feedback resistor value used to set the device specs.
3. $R_i \geq$ Nominal inverting input impedance

These 3 items are used to compute the optimum feedback transimpedance for the particular part. This is given by

$$Z_t^* = R_f + RA_v$$

This information is used to compute a more optimum R_f as the desired closed loop gain moves away from the design point A_v.

It is important to note that, given any feedback R_f and any closed loop non-inverting signal gain, a feedback transimpedance can be computed using the equation for $Z_t = R_f + R_iA_v$. Z_t^* is the optimum value for open loop phase margin and closed loop response flatness found by evaluating the expression at the specific R_f and gain used in designing and specifying the part.

$I_c \geq$ Approximate collector current for the emmitter followers seen looking into the inverting input. The inverting inputs do not necessarily present an integer number of series/parallel emmitter followers. The approximate scale factors can be computed by solving for n in the following expression

$$R_i = n\ V_t/I_c \text{ with } V_t = kT/q \text{ (=26mV at room temperature)}$$

$I_c/I_{cc} \geq$ Ratio of inverting input stage bias current to the total device quiescent current. With n determined from above, the adjusted value for R_i may be determined for a part that is being operated at a different quiescent current than is normally specified.

The data presented here represent a good approximation to the device characteristics. Several second order effects have been neglected for the sake of simplicity.

The CLC505, an adjustable supply current op amp, was optimized at 9mA supply current. No attempt was made in this table, or in the datasheet, to reset the optimum R_g as the supply current is decreased. At very low supply current, the CLC505's inverting input impedance dominates the feedback transimpedance expression. To compensate for this with a reduce R_f, as has been suggested in this document, would require such low values as to excessively load the limited output drive current available. The CLC505 at 1mA supply current shows a gain bandwidth product performance due to the dominance of R_i in the loop gain equation.

Note: The circuits included in this application note have been tested with National Semiconductor parts that may have been obsoleted and/or replaced with newer products. Please refer to the CLC to LMH conversion table to find the appropriate replacement part for the obsolete device.

TABLE 1. Comlinear Monolithic, Current Feedback, Amplifier Optimum Feedback Transimpedance and Operating Point Information

Part #	Design Point Information				Operating Current		comments
	A_v	R_f (Ω)	R_i (Ω)	Z_t* (Ω)	I_c (mA)	I_c/I_{cc}	
CLC400	+2	250	40	330	.67	.045	
CLC401	+20	1500	50	2500	.52	.035	
CLC402	+2	250	16	282	.82	.055	
CLC404	+6	500	30	680	.87	.080	
CLC406	+6	500	60	860	.43	.09	
CLC409	+2	250	25	300	1.05	.08	
CLC410	+2	250	35	320	.74	.05	disable left open
CLC411	+2	301	50	400	.52	.05	disable left open
CLC414	+6	500	250	2000	.105	.05	each amplifier of quad
CLC415	+6	500	60	860	.43	.09	each amplifier of quad
CLC430	+2	750	60	870	.43	.04	disable left open
CLC500	+2	250	32	314	.82	.05	
CLC501	+20	1500	30	2100	.86	.05	see (Note 3)
CLC505	+6	1000	50	1300	.52	.06	I_{cc} = 9.0mA R_p = 33kΩ
CLC505	+6	1000	150	1900	.175	.06	I_{cc} = 3.3mA R_p = 33kΩ
CLC505	+6	1000	490	3950	.053	.06	I_{cc} = 1.0mA R_p = 33kΩ

Note 1: Power supplies at ±5V

Note 2: 25°C temperature assumed. yields kT/q = .26V

Note 3: CLC501 specification point at A_v = +32, R_f = 1500Ω Design point, however is at A_v = +20, R_f = 1500Ω

TABLE 2. Comlinear Hybrid, Current Feedback, Amplifier Optimum Feedback Transimpedance and Operating Point Information

Part #	Design Point Information				Operating Current		comments
	A_v	R_f (Ω)	R_i (Ω)	Z_t* (Ω)	I_c (mA)	I_c/I_{cc}	
CLC103	20	1500	8.5	1670	1.57	.054	fixed internal R_f. See (Note 6)
CLC203	20	1500	11.8	1736	2.21	.072	fixed internal R_f. See (Note 6)
CLC200	20	2000	8.5	2170	1.54	.053	See (Note 7)
CLC201	20	2000	17	2340	1.54	.053	See (Note 7)
CLC205	20	2000	23Ω	2460	.74	.037	see (Note 8)
CLC206	20	2000	15Ω	2300	1.10	.038	see (Note 8)
CLC207	20	2000	23Ω	2460	.74	.030	see (Note 8)
CLC220	20	1500	8.5	1670	1.54	.053	see (Note 7)
CLC221	20	1500	17	1840	1.54	.053	see (Note 7)

TABLE 2. Comlinear Hybrid, Current Feedback, Amplifier Optimum Feedback Transimpedance and Operating Point Information (Continued)

Part #	Design Point Information				Operating Current		comments
	A_v	R_f (Ω)	R_i (Ω)	Z_t* (Ω)	I_c (mA)	I_c/I_{cc}	
CLC231	2	250	15	280	1.78	.093	
CLC232	2	250	15	280	1.78	.071	
CLC300A	20	1500	7.5	1650	1.73	0.70	see (Note 7)

Note 4: Power supplies at ±15V

Note 5: 25°C temperature assumed, yields kT/q = 26V

Note 6: CLC103 & CLC203 have fixed internal R_f Cannot, therefore increase the R_f value or insert additional R_i for loop gain control

Note 7: These parts include an optional internal feedback resistor that may or may not be used in applying the part Not using this internal R_f allows adjusting the R_f over gain and/or inserting additional R_i

Note 8: CLC205, CLC206, & CLC207 use a small shunting capacitance across the internal R_f to extend the bandwidth Using a standard RN55D external R_f, with lower shunt capacitance, will require a large nominal design point value for Z_t* to hold optimum loop gain At A_v = +20, an external R_f = 2 74kΩ yields the desired Z_t

Improving Amplifier Noise for High 3rd Intercept Amplifiers

National Semiconductor
OA-14
Michael Steffes

Abstract

Wide spurious-free dynamic range certainly the goal for any IF amplifier. This is particularly true for OTH radar as well as other systems using high resolution digitizers. Recently introduced current feedback amplifiers offer exceptional 3rd order intermodulation intercepts at very low quiescent power levels, but have been plagued by relatively poor noise figures. Teaming these op amps with a simple transformer input coupling yields noise figures less than 7dB with 3rd order intercepts greater than 40dBm (for frequencies < 10MHz).

Although not commonly considered for IF amplifiers, wideband, DC coupled operational amplifiers can offer considerable performance advantages at the lower IF (or HF) over standard AC coupled amplifiers. Particularly suitable from a distortion standpoint are a family of recently introduced monolithic current feedback operational amplifiers. Similar to the more common voltage feedback op amps, these parts offer very high non-inverting input impedance, very low output impedance, and a very high open loop gain that is controlled through the use of external resistors to set a well controlled closed loop gain. These amplifiers are unique in that the inverting node presents a low impedance through which the amplifier senses a feedback current as opposed to the more common feedback voltage. (Reference 1)

The current feedback topology, as implemented in National's CLC400 and CLC401 amplifiers, is also exceptionally symmetric. This yields intrinsically low distortion mechanisms internal to the amplifier which are then divided by the loop gain to yield the closed loop distortion. As described in Reference 1, the loop gain for a current feedback amplifier is principally set by the feedback resistor value. The loop gain will, of course, show a frequency dependence yielding a continued improvement in distortion down to the dominant open loop pole frequency (at approximately 350kHz for these parts). Conversely, the distortion will worsen moving to higher frequencies as the open loop gain rolls off. Measuring the 3rd order intermodulation intercept at 10MHz yields between 40 and 45dBm for these two parts. Although theory indicates a continued improvement below this frequency, accurate measurements are difficult to perform for intercepts above 45dBm for output power levels within the capability of these two devices.

Taking advantage of this exceptional intercept performance has, however, been impaired by noise figures ranging from 11 to 20dB depending on the device and the gain setting used. Reflecting all op amp noise sources to the non-inverting input typically yields an equivalent input spot noise voltage (at frequencies above the 1/f noise corner) that range from 2.4nV/√Hz to well over 5nV/√Hz (for the CLC401 operated at low gains.) Aside from the intrinsic noise voltage at the non-inverting input, the effect of the inverting noise current also contributes strongly to this result. (See the appendix and Application Note OA-12 for a discussion of calculating the equivalent input noise voltage.)

As suggested in the literature (Reference 2), transformer coupling can sometimes be used to reduce an amplifier's noise figure. This is possible when the equivalent input noise voltage is much greater than the noise voltage generated by the input noise current through the source impedance. Reference 2 suggests an optimum source impedance for noise figure given by the ratio of noise voltage to noise current. If this ideal impedance is much greater than the typical 50Ω source impedance seen in IF strips (as it is for the two amplifiers considered here), a significant improvement in the noise figure can be achieved using transformer coupling. Conceptually, the transformer will provide a noiseless voltage gain at the expense of increasing the source impedance for the input noise current.

Using this technique with the current feedback op amps will sacrifice the DC coupling, with the transformer setting the low frequency limit of operation. Depending on the amplifier to set the high frequency limit will yield poor distortion performance near the amplifier's -3dB frequency. The amplifier's -3dB point is largely determined by the frequency at which the loop gain has dropped to unity. With negligible loop gain, the internal distortion mechanisms are no longer corrected yielding poor distortion performance. Hence, it is preferable to have the transformer also limit the high frequency performance. Both amplifiers considered here offer -3dB bandwidths exceeding 100MHz. A transformer offering good performance up through 50MHz maximum and down to as low a frequency as is desired would probably be a suitable choice

Figure 1 shows the topology to be considered

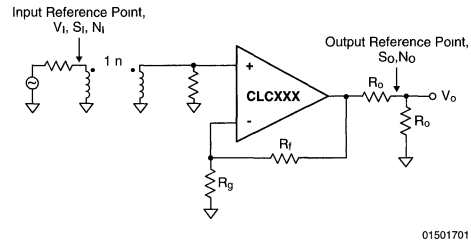


FIGURE 1.

The transformer will provide a noiseless voltage gain from the voltage applied to its input to the non-inverting input of the amplifier. This is done at the expense of increasing the AC source impedance looking back out of the amplifier's non-inverting input. Increasing the turns ratio of the transformer (i.e. picking up voltage gain) will decrease the noise figure until the noise term due to the non-inverting input noise current times the source impedance equals the equivalent non-inverting input noise voltage.

Constraints and Assumptions

1. Input impedance matching to the source impedance (R_s) at the transformer input is desired. Therefore, $R_1 = n^2R_s$. With this assumption, going to the output side of the transformer, the source impedance for the non-inverting input noise current will equal $R_1/2$ or, in terms of Rs will be $n^2R_s/2$. R_1 will also introduce a noise voltage term into the analysis.

Constraints and Assumptions

(Continued)

2. Since the op amp offers a low output impedance, a separate matching resistor must be added to drive into a matched load as would be typical in an IF application (normally, $R_o = 50\Omega$). If we assume the resistor noise of the output matching network is negligible compared to the noise at the output, no change in the S/N ratio will be seen in going from the output pin of the amplifier to the load point. Therefore, the noise figure and gain will be calculated to the load point neglecting any noise added by the output matching resistor, R_o.
3. The various noise contributors for the amplifier are considered to be uncorrelated. This allows equivalent total noise powers to be developed as the sum of the separate noise powers. The noise voltage and currents are taken to be the spot noise values yielding a spot noise figure value For transformer low frequency rolloff corners < 100kHz, some increase in spot noises at the low frequencies will be observed due to the 1/f noise corners for the amplifiers. (Refer to the individual op amp data sheets or Application Note OA-12 for detailed noise data).

Noise Figure Computation

To develop an expression of the noise figure for the circuit of *Figure 1*, the most elementary definition shown as Equation 1 will be used

$$NF = 10 \log \frac{S_i / N_i}{S_o / N_o} \tag{1}$$

This definition states that the noise figure is 10 times the log of the ratio of the signal/noise ratio at the input to the signal/noise ratio at the output. These ratios are for the signal and noise powers available at the input and output. The noise power available at the input is taken to be that delivered by R_s to a conjugate matched load where the noise of that load is separated out as being added by the system. Since some noise will always be added, the signal/noise ratio at the output will be degraded from that at the input yielding a noise figure always > 0.

To evaluate the noise figure expression, the circuit of Figure 1 is redrawn in a more idealized form in Figure 2.

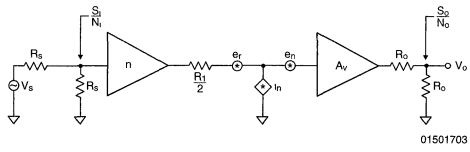


FIGURE 2.

In this circuit, the transformer has been replaced by its equivalent elements; an input terminating impedance (R_s), a noiseless voltage gain given by the turns ratio (n), and an equivalent output impedance taken as the parallel combination of R_1 and R_s reflected through the transformer. ($R_1/2$). Note that R_1 has been reflected to the input side as a noiseless terminating resistor, R_s . R_1 's noise contribution is retained as e_r on the output side of the transformer since this needs to be considered as part of the noise added by the system.

The amplifier has been replaced by an infinite input impedance gain block (A_v) with its two equivalent noise sources brought out as e_n , and i_n . Note that en includes the noise contributions of the inverting input noise current and the feedback and gain setting resistor noises (This analysis is described in the appendix.)

Although the gain and noise terms of *Figure 2* have thus far been expressed as voltage gains with noise voltage and current terms, the noise figure development deals only with power gains and noise powers. Therefore, the gains and noises shown on *Figure 2* will be modified to get the power gain from input to output and the noise powers delivered at the input and output.

Looking at the separate parts of the argument in Equation 1, we can separate them as.

$\frac{S_i}{S_o}$ → inverse of the power gain through the path

$$= \frac{V_i^2 / R_s}{\left(\frac{nA_v V_i}{2}\right)^2 / R_o} = \frac{4}{(nA_v)^2} \frac{R_o}{R_s}$$

$\frac{N_o}{N_i}$ → output noise power over input noise power

The output noise power can be developed by taking each contributing noise voltage term through to the output then developing the power of that voltage across R_o and adding all the terms. The separate noise voltage terms at the output are:

Source noise voltage → $\sqrt{4KTR_s}\ \frac{1}{2}\ nA_v\ \frac{1}{2}$

Terminating resistor noise (e_r) → $\sqrt{4KTR_1}\ \frac{1}{2}\ A_v\ \frac{1}{2}$

where K → Boltzman's constant
= 1.38E – 23 Joules / °Kelvin
T → °Kelvin = 290° in this analysis
then 4kT = 16E - 21J

Amplifier current noise → $i_n \frac{R_1}{2} A_v \frac{1}{2}$

Amplifier voltage noise → $e_n A_v \frac{1}{2}$

Note that both noise voltages intrinsic to R_s and R_1 are attenuated by 1/2 due to the impedance matching present on both sides of the transformer (i.e. R_1 reflects to the source side as R_s to ground, and R_s reflects to the secondary side as the driving impedance for the non-inverting input terminating impedance, R_1).

Noise Figure Computation (Continued)

Substituting with $R_1 = n^2R_s$, and adding each noise voltage term squared divided by the output terminating impedance, R_o, will yield the total output noise power.

$$N_o = \left[KTR_s\left(\frac{nA_v}{2}\right)^2 + KTn^2R_s\left(\frac{A_v}{2}\right)^2 + i_n^2\left(\frac{n^2R_s}{2}\right)\left(\frac{A_v}{2}\right)^2 + e_n^2\left(\frac{A_v}{2}\right)^2\right]/R_o$$

The input noise power may be derived as the power delivered to the source matching resistor from the source resistor noise voltage. This is:

$$N_i \rightarrow \left[\frac{1}{2}\sqrt{4KTR_s}\right]^2/R_s = KT$$

Pulling an $(nAv/2)^2R_S$ out of the N_o expression, the ratio of input to output noise power may be rewritten as:

$$\frac{N_o}{N_i} = \frac{(nA_v)^2R_s}{4R_o}\,\frac{KT + KT + i_n^2n^2\frac{R_s}{4} + \frac{e_n^2}{n^2R_s}}{KT}$$

Combining the expressions for noise power ratios and the inverse of the power gain through the channel, developed above, yields:

$$\frac{S_i}{S_o}\frac{N_o}{N_i} = \frac{4R_o}{(nR_v)^2R_s}\,\frac{(nR_v)^2R_s}{4R_o}\left(2 + \frac{i_n^2n^2\frac{R_s}{4} + \frac{e_n^2}{n^2R_s}}{KT}\right) =$$

$$\frac{S_i}{S_o}\frac{N_o}{N_i} = \left(2 + \frac{i_n^2n^2\frac{R_s}{4} + \frac{e_n^2}{n^2R_s}}{KT}\right)$$

Multiplying the fraction through, top and bottom, by R_s and going back to the log form for noise figure yields:

$$NF = 10\log\left(2 + \frac{\left(i_nn\frac{R_s}{2}\right) + \left(\frac{e_n}{n}\right)^2}{KTR_s}\right) \qquad (2)$$

Looking at the component parts of this expression, the "2" in the log argument arises from our terminating with a discrete (noisy) matching resistor, R_1. This increases the minimum achievable noise figure from 0dB to 10 • log (2) = 3dB.

The $\dfrac{\left(i_nn\frac{R_s}{2}\right) + \left(\frac{e_n}{n}\right)^2}{R_s}$ parts of the fraction

represents the 2 noise voltages (the total equivalent input noise voltage and the voltage generated by the noise current through the source impedance) at the input of the amplifier reflected to the transformer input and added as powers across R_s. The kT term in the denominator is simply the noise power available from the source at the input to the network. From this, as the turns ratio increases, the contribution of the noise current increases while that due to the noise voltage decreases As reported in Reference 1, the minimum value will occur when these two terms are equal.

Solving for the optimum turns ratio to minimize the noise figure:

$$n_{opt} = \sqrt{\frac{e_n}{i_n\frac{R_s}{2}}}$$

Substituting this in Equation 2 yields a minimum noise figure:

$$NF_{min} = 10\log\left(2 + \frac{e_ni_n}{KT}\right)$$

Recognizing that transformer turns ratios are actually only available in integer steps, the optimum turns ratio is somewhat academic. However, for a given n, it can be recognized that anything that will reduce i_n or e_n will improve the noise figure.

Little can be done to reduce the noise current at the amplifier's non-inverting input. The equivalent input noise voltage can, however, be reduced as the amplifier is operated at higher gains. The results in the appendix show that equivalent input noise terms due to the inverting noise current and resistor noises are reduced as the gain increases. However, once these noise terms have been reduced below the intrinsic non-inverting input noise voltage, further improvements through increased gain are minimal.

Design Procedure and Test Results

To illustrate the design procedure and the resulting performance using this input transformer coupling, two possible designs using the CLC400 and CLC401 will be developed. The designs will proceed with the assumption that the maximum gain consistent with broad bandwidth and good 3rd order intermod intercept is desired. Enough information is presented to allow a design to proceed from a targeted gain as well.

The CLC400 is a broadband DC coupled monolithic amplifier intended for relatively low gain operation. Typical specifications show a 200MHz bandwidth (-3dB) at a gain of +2. Both parts pull a nominal no load current of 15mA when operated from their recommended ±5 volt power supplies. For the current feedback topology, a low gain part corresponds to a part that has been optimized for a lower value of feedback resistor as opposed to a high gain part such as the CLC401. Hence, the nominal N at a gain of + 2 for the CLC400 is shown on the data sheet as 250Ω, while the CLC401 is optimized to use a 1.5k feedback at a gain of +20. Most of the requisite information for the design can be found in National Application Notes OA-12 (Noise Analysis) and OA-13 (Current Feedback Loop Gain Analysis).

Non-inverting input intrinsic noise voltage	e_{ni} = 2.5nV/√Hz
Inverting input noise current	i_i = 14pA/√Hz
Non-inverting input noise current	i_{ni} = 3.2pA/√Hz
Inverting input impedance	Z i ≅ 50Ω
Nominal feedback transimpedance for maximally flat frequency response	Z_t = 350Ω

Using these numbers, and equation F in the appendix, a maximum amplifier gain for reduced equivalent input noise voltage may be derived as (this assumes an ** of 1/9) G = 4.3

Rounding this off to a gain of +4 yields a feedback resistor value of:

$R_f = Z_t - GZ_1 = 150\Omega$ **(Eq. D In Appendix)**

Note that taking the gain too high will eventually yield very low R_f values from this equation. For very low values of R_f, a significant degradation in both bandwidth and 3rd order intercept will be observed due to the added output stage loading presented by the feedback network. Generally, $R_f + R_g = 200\Omega$ should be taken as a lower limit to R_f.

Computing the equivalent input noise voltage for G = 4 using Eq. E of the appendix yields

$$e_n = \sqrt{(2\ 5nV)^2 + [(14pA)(37\ 5\Omega)]^2 + 16E-21(37\ 5\Omega)} = 2\ 67\ \frac{nV}{\sqrt{Hz}}$$

As hoped, this total equivalent input noise voltage is nearly equal to the intrinsic noise voltage listed above. From these results, and assuming a 50Ω source impedance, an optimum transformer turns ratio would be:

$$n_{opt} = \sqrt{\frac{e_n}{i_n \frac{R_s}{2}}} = \sqrt{\frac{6.67nV}{3.2pA(25\Omega)}} = 5.78$$

This yields a best case noise figure equal to

$$NF_{min} = 10\log\left(2 + \frac{2.67nV}{4E-21}\right) = 6.2dB$$

It is, however, difficult to maintain broadband performance through the transformer with a turns ratio this high. For test, a 1:4 turns ratio transformer from Mini-Circuits was selected as a reasonable compromise between best noise figure and broadband performance (part #T16-6T)

The resulting test circuit for the CLC400 is shown in *Figure 3.*

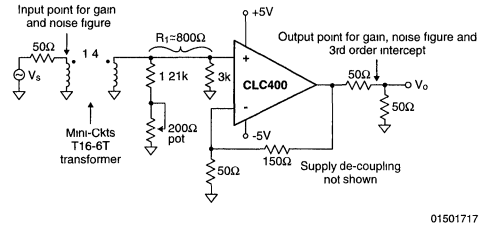


FIGURE 3.

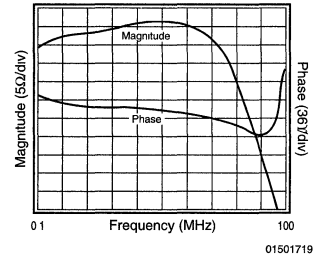
$$NF = 10\log\left(2 + \frac{\left(4(3.2pA)25\Omega\right)^2 + \left(\frac{2.67nV}{4}\right)^2}{(4E-21)(50\Omega)}\right) = 6.2dB$$

Using this test circuit, the anticipated performance can be calculated to be:

Overall gain A_v = 4 • 4 • 1/2 = + 8 (18dB)

Noise Figure (from Eq.2)

In test, the first step was to tune the input impedance matching to provide a good 50Ω match over the frequency range of interest, after which the transfer function (S_{21}) was measured. These results are shown in *Figure 4.*



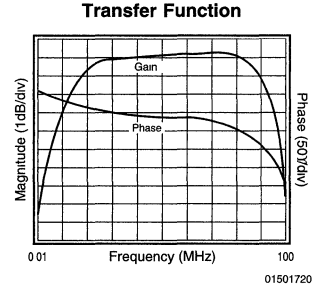


FIGURE 4.

These results show excellent input impedance matching over a broad frequency range with a very flat passband gain from about 60kHz to 30MHz.

The noise figure for this circuit was measured using an HP8970A with an HP346B noise source. *Figure 4* tabulates those results along with the 3rd order intercept.

Frequency	Noise Figure	3rd Order Intercept
10MHz	6.8dB	44dB
20MHz	6.8dB	38dB
30MHz	7.1dB	33dB
40MHz	7.1dB	30dB

FIGURE 5.

The measured noise figure shows excellent agreement with the predicted value, while the 3rd order intercept parallels the CLC400 data sheet plots. Note that the data sheets typically show intercept defined for a power level at the output pin as opposed to the 6dB lower value if defined at the matched load. Adding 6dB to the results shown above gets us back to the data sheet plots. This indicates that the intercept has not been degraded by the transformer input coupling.

Note that the noise figure for just the CLC400, configured as shown in Figure 3 without the transformer, may be derived by simply letting n = 1 in the noise figure equation (Equation 2). Doing this yields a noise figure of 15.8dB for the CLC400 by itself (assuming only a 50Ω non-inverting input impedance matching resistor). Hence, the transformer not only provides us with more gain but with greatly improved noise figure.

In summary, this circuit shows a 50Ω in/50Ωout, 18dB gain block with very flat frequency response from 60kHz to 30MHz offering an approximate 7dB noise figure with a 3rd order intercept greater than 33dBm over that frequency range, while dissipating only 150mW quiescent power!

Design and Test Results for the CLC401

The CLC401 is a monolithic, DC coupled, wideband current feedback amplifier optimized for higher closed loop gains. Typical specifications show a 150MHz -3dB bandwidth at a gain of +20 using a 1.5k feedback resistor while drawing only 15mA no load current from the specified ±5 volt supplies. Getting the requisite design information from Application Notes OA-12 and OA-13,

Non-inverting input intrinsic noise voltage	e_{ni} = 2.4nV/√Hz
Inverting input noise current	i_i = 17pA/√Hz
Non-inverting input noise current	i_{ni} = 2.SpA/√Hz
Inverting input impedance	Z i ≅ 50Ω
Nominal feedback transimpedance for maximally flat frequency response	Z_t = 2.5kΩ

Using these numbers, and Eq. F of the Appendix, yields a maximum amplifier gain for minimal equivalent input noise voltage of (assuming α = 1/9) G = 32.5

Building up the circuit at this gain and using the same transformer as for the CLC400 test circuit resulted in a 3dB response peaking at the higher frequency limits.

This seemed to arise from a gain dependent non-inverting input impedance resonating with the transformer. Reducing the amplifier gain ameliorated this effect, Since the amplifier gain was being determined somewhat arbitrarily to reduce the noise figure, backing away from this gain to improve frequency response seemed reasonable. For test, an amplifier gain of G = +25 was selected. Using Eq. E of the appendix shows an equivalent input noise voltage with again of +25 given by:

$$e_n = \sqrt{(2.4nV)^2 + [(17pA)(37.5\Omega)]^2 + 16E-21(50\Omega)} = 2.70\,\frac{nV}{\sqrt{Hz}}$$

With this result, an optimum turns ratio for the transformer and a theoretical best noise figure may be calculated to be:

$$n_{opt} = \sqrt{\frac{2.70nV}{(2.8pA)(25\Omega)}} = 6.2$$

and

$$NF_{min} = 10\log\left(2 + \frac{2.70nV\,(2.8pA)}{4E-21}\right) = 5.9dB$$

Again, the high transformer turns ratio required for optimum noise figure would result in an unnecessarily limited bandwidth. Backing off to a 1:4 turns ratio transformer yielded the test circuit shown in *Figure 6.*

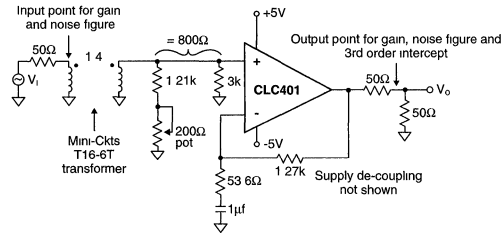


FIGURE 6.

Note that for this test, the amplifier's gain setting resistor has been AC coupled with a 1mf capacitor. This is intended to reduce the DC gain for the amplifier's input offset voltage to 1, holding the output DC as close to 0 as possible. The capacitor value was chosen to yield a transfer function pole well below the transformer low frequency cutoff. The feedback resistor value is set using Equation D of the Appendix. The anticipated midband gain and noise figure performance can be calculated to be:

Overall Gain A_v = 4 • 25 • 1/2 = + 50 (34dB)

Noise Figure (from Eq. 2)

$$NF = 10\log\left(2 + \frac{\left(4(2.8pA)25\Omega\right)^2 + \left(\frac{2.70nV}{4}\right)^2}{4E-21(50\Omega)}\right) = 6.7dB$$

As with the CLC400, the test sequence was to the input matching impedance network to yield a good 50Ω match over as wide a frequency range as possible. After this, the input to output transfer function was measured (S21). *Figure 7* show these results:

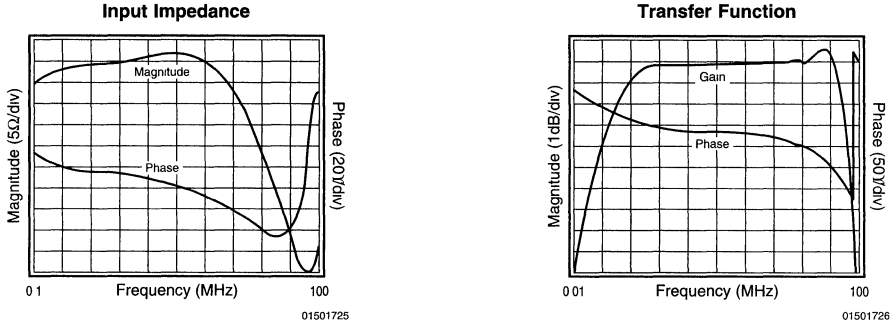


FIGURE 7.

This circuit doesn't do quite as well in holding up the input impedance to higher frequencies but it does provide a reasonably flat frequency response from 70kHz to 50MHz (passband with < ± 0.5dB ripple).

A measure of the noise performance was obtained using an HP3585 spectrum analyzer along with a CLC100 low noise wideband amplifier as a preamp to the analyzer input. Although accurate noise figure measurements are difficult to achieve in this fashion, this approach indicated noise figures between 7 and 8dB. *Figure 8* tabulates the measured 3rd order intercept results and this estimated noise figure.

Frequency	Estimated NF	3rd Order Intercept
10MHz	7-8dB	38dB
20MHz	7-8dB	33dB
30MHz	7-8dB	29dB
40MHz	7-8dB	25dB
50MHz	7-8dB	23dB

FIGURE 8.

Calculating the noise figure of just the CLC401 without the transformer coupling (by letting n = 1 in the noise figure equation) yields 15.9dB for just the amplifier by itself with a 50Ω non-inverting termination resistor. So, again, the transformer has added signal gain while greatly improving the noise figure.

The results of *Figure 7* and *Figure 8* show a 50Ω in/50Ω out, 34dB gain block with reasonably flat frequency response from 70kHz to 50MHz offering an approximate 7dB noise figure with 3rd order intercepts greater than 25dBm for operation below 40MHz dissipating only 150mW! The intercept performance improves rapidly at lower frequencies with continued improvement observed below 10MHz.

Comparisons and Conclusions

Clearly, the transformer coupling offers the potential for some real improvement in noise figures for the amplifiers considered here. Having given up the DC coupling in the process, however, we are now looking to compare these parts to the more classical AC coupled IF amplifiers.

Those parts generally use a Class A output stage as opposed to the Class AB structure used in most of National's amplifier products. This, along with the high loop gain at lower frequencies, allows exceptional distortion performance to be achieved at a fraction of the quiescent power dissipation vs. the more classical Class A output. This advantage narrows as we move to frequencies over 100MHz with the op amp's loop gain dropping below unity at these higher frequencies

Generally, for the lower frequency applications, the circuits described here, or similar circuits using different National amplifiers can offer considerable advantages in the areas of power dissipation, size, and cost.

The transformer coupling offers additional flexibility through potential signal inversion, by reversing the dot convention, output DC shifting, by inserting a DC voltage in place of the ground on the secondary, and potential narrowband filtering. If higher output power levels are desired, this same approach could be used with one of National's hybrid op amps offering higher supply voltages and greater output power capability. The CLC232, for low gains, and the CLC207 for higher gains, are particularly low harmonic distortion parts that would also benefit, from a noise figure standpoint, from transformer coupling.

This approach to noise figure improvement is applicable to any op amp with an optimum source resistance greater than the actual source resistance. With the total equivalent input noise voltage at the non-inverting input decreasing as the closed loop gain is increased (as shown in the appendix), it is advantageous to operate the op amps at high gains. The current feedback topology, pioneered by National, is particularly suitable for wideband, high gain applications.

As described in Application Notes 300-1 and OA-13, the current feedback op amp topology largely eliminates the gain-bandwidth performance limitations plaguing earlier voltage feedback designs. Therefore, running the amplifiers to higher gains, in an effort to drive down the non-inverting input voltage noise, will not sacrifice broadband performance as it would using a voltage feedback part.

Acknowledgments

Ralph Carfi, General Electric, Syracuse, N.Y. for measuring the noise figure on the CLC400 test circuit and many useful discussions on this application.

Alan Baker, R & D, National Semiconductor Corp., for review and discussion of the noise figure equation development.

Steve Smith, R & D, National Semiconductor Corp., for automating the 3rd order intercept measurement procedure.

References

1. "Current-Feedback Amplifiers," Sergio Franco EDN, Jan. 5, 1989, page 161 (in Comlinear Corporation 1989/ 1991 Databook). Also, National Application Note 300-1 and Application Note OA-14.
2. "Low-Noise Electronic Design," Motchenbacher and Fitchen; Wiley 1973, pp. 10, 34, and 127.

Appendix:

Computing the equivalent Input noise voltage, the gain, and feedback resistor values for noise figure reduction with current feedback op amps.

The equations for determining the equivalent input noise voltage for use in the noise figure calculations will be developed. Since the external resistors around the amplifier, R_f and R_g, play a large role in setting that noise, the amplifiers transfer function, which is also determined by these resistors, will be given and used to set the gain

Figure 9 shows the necessary information to develop both the transfer function from V_i to V_o and the equivalent input noise voltage expression. As described in Reference 1, a current feedback amplifier uses a unity gain buffer from the + input to the inverting node, X_1, with the inverting node current (i_{err}) acting as the feedback signal sensed and passed on to the output through a transimpedance gain, Z_s

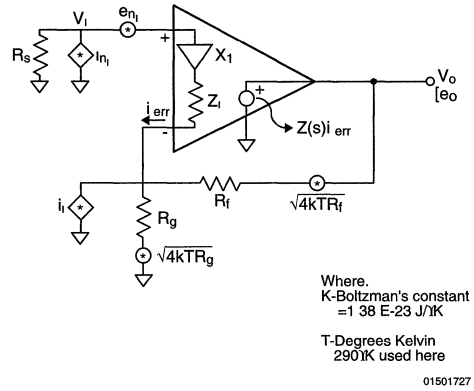


FIGURE 9.

The goal here is to develop an equivalent non-inverting input noise voltage source to place at the non-inverting input for noise figure calculations. Normally, a noise generator for the non-inverting termination resistor would be included in this analysis. In the context of using an input transformer coupling, however, this resistor will be set by impedance matching concerns removing it as a variable for equivalent input noise voltage reduction. The effect of this resistor's noise is included in the development for noise figure. The 3 noise sources on the inverting side of the circuit must be reflected to the non-inverting side and combined with the intrinsic noise voltage, e_{ni}, already present in the model. Neglecting i_{ni}, which is left separate for later use in the noise figure equations, each noise voltage or current will develop an output voltage noise. With the non-inverting signal gain defined to be $G = (1 + R_f/R_g)$, the separate output noise voltages are:

intrinsic non-inverting input noise voltage $\rightarrow e_{ni}\, G$

inverting input noise current $\rightarrow i_i\, R_f$

combined resistor noise terms $\rightarrow \sqrt{4KTR_fG}$

Combining terms as the root sum of squared elements, and reflecting this to the non-inverting input yields

$$\text{equivalent input noise voltage} \rightarrow \sqrt{(e_{n_i})^2 + \left(\frac{i_iR_f}{G}\right)^2 + \frac{4KTR_f}{G}} \qquad \textbf{Eq. C}$$

As is apparent from this expression, both the gain and the resistor values can be used to reduce the input noise voltage. Increasing the gain and/or reducing the resistor values will both decrease the apparent input noise voltage. This effort is bounded by the intrinsic input noise voltage, e_{ni}.

Setting the gain and the resistor values needs to be done in the context of maintaining adequate phase margin for the closed loop amplifier response. Analyzing the circuit of Figure A for the V_o/V_i transfer function yields (see Application Note OA-13 for a more complete development);

where: $Z_{(s)} \rightarrow$ Forward transimpedance gain of the

$$\frac{V_o}{V_i} = \frac{1+R_f/R_G}{1+\dfrac{R_f+Z_i\left(1+R_f/R_G\right)}{Z_{(s)}}} = \frac{G}{1+\dfrac{R_f+GZ_i}{Z_{(s)}}}$$

amplifier (frequency dependent)

$Z_i \rightarrow$ Inverting input impedance (considered noiseless and real)

The inverting node current is the feedback signal with an output voltage to inverting input current transfer gain given by $Z_t = R_f + Z_iG$

Every current feedback amplifier has an internal forward transimpedance gain function ($Z_{(s)}$) optimized for a certain value of Z_t. Typically, this optimization yields a 60° phase margin at the gain and feedback resistor value specified on the data sheet for guaranteed performance specs. To a first approximation, this Z_t can be held constant (maintaining maximum closed loop bandwidth with no peaking) as the desired closed loop signal gain is changed from the nominal design point. This is done by adjusting R_f vs. gain. Solving for this from the above expression for Z_t yields:

$$R_f = Z_t - Z_iG \qquad \textbf{Eq. D}$$

Appendix: (Continued)

If this expression for R_f is placed into the equivalent input noise expression developed above, Eq. C, we get

$$e_n = \sqrt{\left(e_{n_i}\right)^2 + i_i^2\left(\frac{Z_t}{G} - Z_i\right)2 + 4KT\left(\frac{Z_t}{G} - Z_i\right)} \quad \textbf{Eq. E}$$

The only variable left at this point is the desired closed loop gain. The absolute resistor values have been removed with the assumption that a maximally flat frequency response is desired as the closed loop gain is changed. Again we see that increasing the gain will decrease the equivalent input noise voltage. This approach is decreasingly effective as those terms involving G become less than the non-inverting input noise voltage e_{ni}. If we target a desired ratio of the two squared terms involving G to the intrinsic non-inverting input noise voltage squared, we can develop a targeted maximum gain beyond which minimal noise reduction is achieved through further gain increases. If we call that ratio of the noise powers cc we can solve for:

$$\left(\frac{Z_t}{G} - Z_i\right) = \frac{2KT}{i_i\,2}\left[\sqrt{1+\alpha\left(\frac{e_{n_i}\,i_i}{2KT}\right)^2} - 1\right] \quad \textbf{Eq. F}$$

From this expression, and a knowledge of Z_t and Z_i , a maximum desired gain may be derived. This yields a somewhat arbitrary upper limit on amplifier gain in that we are only trying to increase the gain until negligible improvements in the noise figure are seen. The amplifier can, of course, be operated at lower gains, with an increase in noise, or at higher gains, with little noise improvement but an eventual bandwidth limitation. If we set α to be 1/9 (saying that the reflected equivalent noise power terms at the non-inverting input are 1/9 the intrinsic input noise power due to the non-inverting input noise voltage) those terms increase the equivalent input noise voltage by only 5%. This will be the initial targeted design criteria used in the example developments.

See Application Note OA-13 for a complete development of adjusting R_f to hold a constant loop gain, and hence bandwidth, as the desired signal gain is changed.

Note: The circuits included in this application note have been tested with National Semiconductor parts that may have been obsoleted and/or replaced with newer products. Please refer to the CLC to LMH conversion table to find the appropriate replacement part for the obsolete device.

Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers

National Semiconductor
OA-15
Michael Steffes

As op amp operating speeds have moved to ever higher frequencies, a whole new set of design concerns have come into play for linear op amp applications. With the development of the current feedback topology, design concerns unique to that topology must also be considered if optimal performance is to be achieved from devices offering over 200 MHz –3 dB bandwidths. This discussion will review some of the considerations common to all wideband linear op amp applications as well as topics unique to the current feedback topology pioneered by Comlinear Corporation. These design guidelines are intended to help the designer get the full potential out of Comlinear's high performance, current feedback, operational amplifiers.

Since there are quite disparate areas to consider here, the approximate order of discussion will follow a perceived frequency of occurrence ranking. Those considered first seem to impact every designer, with more particular concerns dealt with later.

Parasitic Capacitance Effects and What to do About Ground and Power Planes in a PC Board Layout.

The sensitivity of the Comlinear amplifiers to parasitic capacitance arises solely from their wide bandwidth characteristics and not from the current feedback aspect of their design. With parts showing a loop gain that does not drop to unity until the 100 MHz region, a few picofarad capacitance to ground in the loop can have a profound effect on the phase margin at the unity gain crossover frequency. *Figure 1* shows a typical non-inverting gain op amp, including the internal structure for the current feedback topology (Note 1), along with the two most critical external parasitic capacitances.

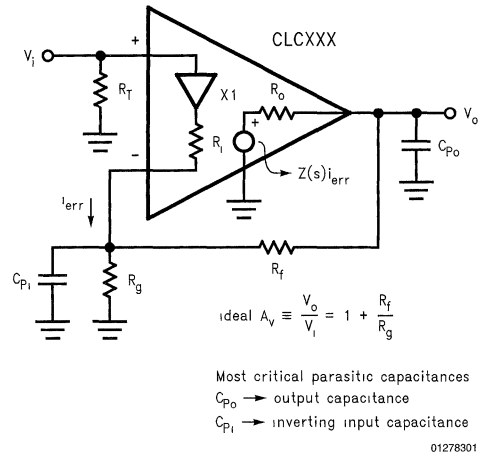


FIGURE 1. Non-inverting Gain with Internal Current Feedback Topology

Note 1: See Application Note OA-13 or OA-31 for a development of the current feedback transfer function

Parasitic, or loading, capacitance directly on the output is particularly effective at transforming amplifiers into oscillators. Closed loop stability for any negative feedback amplifier is determined by the open loop phase margin. In tracing the signal around the loop it is always desirable to have significantly less than 180 degrees phase shift around the loop at the unity gain crossover frequency. Adding a capacitor directly on the output will cause additional signal phase shift

Parasitic Capacitance Effects and What to do About Ground and Power Planes in a PC Board Layout. (Continued)

due to the additional pole introduced by the open loop output impedance, R_o, driving the output pin capacitance, C_{po}. Even small capacitances and low R_o's can cause significant phase shifts with unity gain crossovers in the 100 MHz region (a typical unity gain crossover frequency for Comlinear amplifiers).

Several design and test guidelines can be suggested to keep this sensitivity to C_{po} under control.

a. Always clear ground and power planes away from the output pin net. This includes opening up a little wider than standard clearance to ground and power inner planes to any through hole or trace carrying the output signal.

b. Never probe directly with a high impedance probe or a DVM on the output pin (passive divider probes are okay) If probing, always probe through a series resistor > = 100Ω since this will decouple the effect of the probe capacitance from the output pin. This also holds for adding PC board test points. If needed, connect the test points through a series resistor located as close as possible to the device pin being brought out.

c. If a capacitive load must be driven, such as flash ADC's most of the Comlinear amplifier data sheets include a plot of a recommended series resistor to put at the output prior to the load capacitance Adding a resistor prior to the load (or parasitic) capacitance, changes the load's effect from a pole to a pole-zero pair. This causes a phase dip in the loop phase response that has recovered prior to unity gain crossover.

d. Driving into another amplifier stage, or actually almost any other high input impedance active device, can also present enough capacitance to cause problems. Again, a small series resistor right at the output prior to going off to this device will defuse the situation.

Figures 2, 3 show the effect of an output capacitance on the small signal frequency response of the CLC205, a hybrid current feedback op amp intended for higher gains. The plot shows the SPICE simulated gain, in dB, vs. linear frequency under several loading conditions Similar plots may be generated using the small signal macromodels of Application Note OA-09. Initially, a 200Ω load is driven, then just a 20 pF load, and finally, the 20 pF load with a series 30Ω resistor (R_s in *Figure 2*). Clearly, getting into a series resistor prior to the capacitive load can dramatically improve the frequency response flatness, and hence pulse response capabilities for the amplifier simulated here. Recall that this approach is applicable for both current and voltage feedback amplifiers.

Generally, it is suggested to get the output voltage through a resistor as soon as possible before running it over any significant length of trace or cable. If a matched impedance load is to be driven, source match right at the output pin with a discrete resistor equal to the transmission line's characteristic impedance, and terminate the line similarly. Although short trace runs do not need to be impedance matched, using just the series resistor will isolate the trace capacitance when no terminating resistor is used.

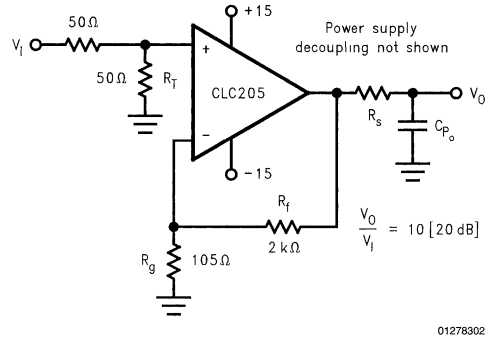


FIGURE 2. Simulation Circuit for Capacitive Loading Test

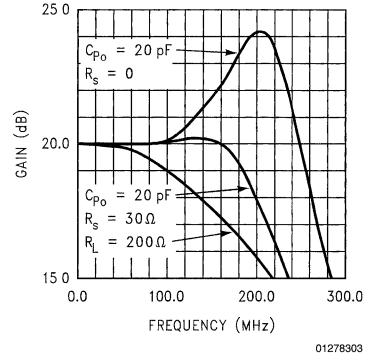


FIGURE 3. Frequency Response for Various Loadings

Parasitic capacitance on the inverting node is a considerably more complex, but not nearly as troublesome, phenomena. Capacitance on this input affects both the non-inverting signal gain, by appearing in shunt with the gain setting resistor, and the loop gain phase margin in a 2nd order sense. Two types of pulse response characteristics can be observed due to this parasitic. If the dominant effect is simply shunting R_g in the ideal gain expression, neglecting loop gain effects for now, a single overshoot with a decay will be observed. If this capacitance is large enough to effect the phase margin, considerable ringing in the pulse response will also be observed.

Again, minimize ground and power planes around the inverting node net. The single overshoot and decay will most often be observed when a current feedback part intended for higher gains, and hence designed to use a relatively high feedback resistor value, is used at low non-inverting gains. The relatively high R_g required to get a low non-inverting gain will bring the impact of whatever parasitic is present down in frequency into the passband of the amplifier. The solution here, beyond simply limiting C_{pi}, is to run inverting mode if possible, or switch to a part intended for lower gain

Parasitic Capacitance Effects and What to do About Ground and Power Planes in a PC Board Layout. (Continued)

operation, and hence designed to use lower resistor values. Given a fixed C_{pi}, operating with lower R_f and R_g will move the zero frequency out beyond the amplifier passband. Application Note OA-14 discusses in more detail the gain range considerations for current feedback amplifiers.

Figures 4, 5, 6 shows a test circuit and simulation results demonstrating the effect of inverting node capacitance for the CLC205 operated at relatively low non-inverting gain.

The effect of increasing C_{pi} from 0.5 pF to 5 pF in the circuit of *Figure 4* can be seen as a considerable peaking in the frequency response of *Figure 5*. This is not, in this case, a loss of phase margin peaking, but simply a zero coming into the non-inverting transfer function due to C_{pi} shunting R_g. This zero frequency is at (C_{pi} • (R_g||R_f) / (2 • pi)) Hz. Note in the pulse response of *Figure 6* that C_{pi} causes a single overshoot with negligible ringing.

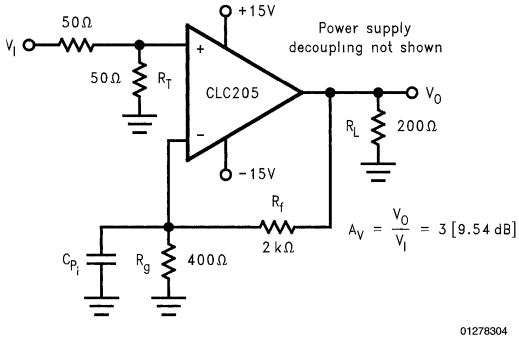


FIGURE 4. Simulation Circuit for Inverting Input Capacitive Test

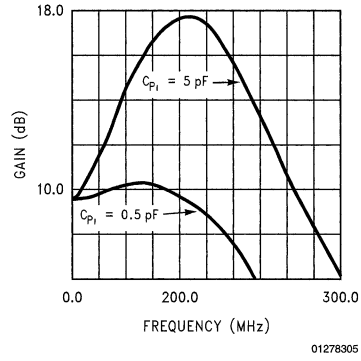


FIGURE 5. Frequency Response vs. C_{pi}

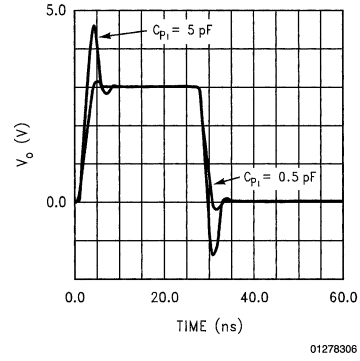


FIGURE 6. Pulse Response vs. C_{pi}

If ringing is observed in the pulse response, this is more likely due to capacitance on the output pin. However, larger parasitic capacitances on the inverting node (>10 pF) can

Parasitic Capacitance Effects and What to do About Ground and Power Planes in a PC Board Layout. (Continued)

also cause loop gain phase margin problems, particularly for parts intended for high gains. Again, the discussion about avoiding parasitic capacitances on the output pin applies equally well here. *Figure 7* shows the difference in pulse response behavior between C_{po} and C_{pi} effects. The upper trace, which was plotted with a 1V offset for clarity, shows the ringing pulse response for the most peaked response of *Figure 3*. This is typical of output pin capacitance effects. The lower trace is a repeat of the C_{pi} = 5 pF pulse response of *Figure 6*.

Parasitic capacitance to an AC ground on the non-inverting input, including the capacitance of the high impedance non-inverting input itself, will generally only introduce an additional response pole, depending on the source impedance driving the input capacitance. For low source impedances, this pole comes in well beyond the passband of the amplifier. However, when the parasitic capacitance on the non-inverting and inverting nodes are approximately equal, intentionally adding non-inverting source impedance equal to $R_g||R_f$ can be very effective at cancelling the response zero coming in through C_{pi} shunting R_g.

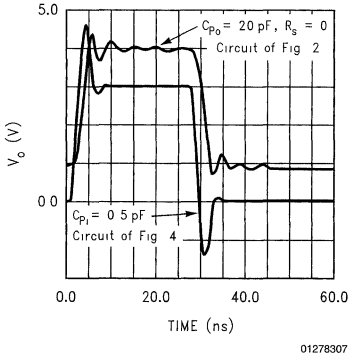


FIGURE 7. Contrasting Pulse Responses for C_{po} and C_{pi}

Figure 8 shows this approach with the C_{pi} = 5 pF case considered earlier in *Figure 4*. Note that we have intentionally matched the capacitance at the non-inverting input and added R_{ni} = 300 to bring the frequency response back to flatness. The signal gain is not changed by the addition of R_p. This approach simply cancels the zero apparent in the upper trace of *Figure 9*, significantly decreasing the pulse overshoot as shown in *Figure 10*.

Although it is critical to remove ground plane from the signal input and output nodes, a good, low inductance, ground return path must be provided for the AC load current. This is typically provided by putting small-valued ceramic capacitors directly on the power supplies, connected to a good adjacent ground plane. These conflicting goals of good power supply grounding with no parasitic capacitance on the I/O pins can be achieved by opening a window around the part for the ground and power planes with the high frequency decoupling capacitors connecting into this ground plane. The layout drawing of the 730013 evaluation board (in the product accessories section of the catalog), shows a good high frequency layout for the 8-pin DIP monolithic amplifier products offered by Comlinear.

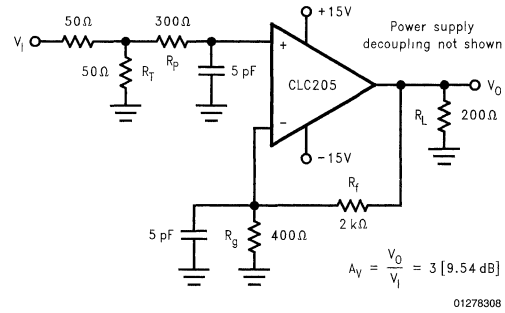


FIGURE 8. Simulation Circuit of C_{pi} Peaking Cancellation

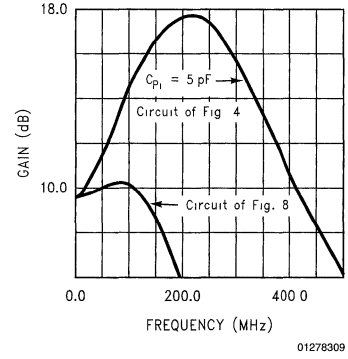


FIGURE 9. Frequency Response Demonstrating Zero Cancellation

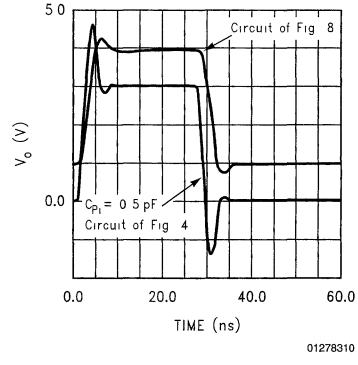


FIGURE 10. Pulse Response with Zero Cancellation

Parasitic Capacitance Effects and What to do About Ground and Power Planes in a PC Board Layout. (Continued)

Figure 11 shows the same amplifier as *Figure 1* with the suggestions for handling parasitic capacitances incorporated.

The circuit of *Figure 11* includes every fix for the possible problems arising from parasitic capacitance discussed thus far. Very rarely would all of these be required for the same application. If test points are to be brought out, always come out through at least 100Ω resistors with the body of those resistors as close as possible to the amplifier pins. Probing at these test points can still radically alter the signal path frequency response. The amplifier should, however, remain stable with at least 100Ω isolating resistors. If inverting node parasitic capacitance seems to be a problem, R_p can be very effective at cancelling it out (except when C_{pi} is so large as to cause phase margin problems). If a parasitic or load capacitance must be driven, R_s may be used very effectively to improve the frequency response flatness. And, always get the high frequency capacitors on the power supplies as close to the part as possible into a good ground plane.

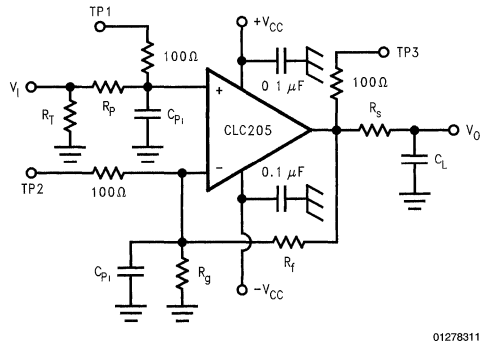


FIGURE 11. Non-Inverting Amplifier Featuring Several Suggested Protections from Parasitic Capacitance Effects

The Importance of the Feedback Resistor

The feedback resistor value becomes of paramount importance in the current feedback topology used by most of the Comlinear amplifiers. As discussed in detail in Application Note OA-14, the feedback resistor is the single most important element in setting the overall frequency response for the current feedback amplifier topology. Briefly, since we are looking for a feedback current from the output voltage to the inverting input, the feedback impedance plays the dominant role in determining what this will be. This, in turn, will determine the amplifier's loop gain and phase margin. Achieving adequate phase margin is critical to the success of any operational amplifier application.

Every current feedback amplifier is optimized for a particular value of feedback resistor. This value is typically noted at the heading of the specifications listing. Always select a value near this as the starting point for any design. Lower values may be used at the risk of lower phase margin and greater frequency response peaking. Higher values may be used at the expense of lower amplifier bandwidth. In fact, increasing the feedback resistor value is a very effective means of overcompensating the amplifier. Unlike voltage feedback amplifiers, a unity gain follower application requires the recommended feedback resistor to be in place from the output to the inverting input. Although having no influence on the low frequency signal gain in the unity follower application, the feedback element is still needed to determine the loop gain for the current feedback topology.

Using reactive elements in the feedback path, either intentionally or unintentionally, can play havoc with the loop gain phase margin. Generally, this should be avoided unless done with extreme care. The small signal macromodels in Application Note OA-9 are very useful for predicting what will happen with different feedback configurations. Using direct capacitive feedback, to implement an integrator, will generally cause oscillations with a current feedback amplifier. Integrators can be implemented, however, using the alternative topologies shown in Application Note OA-7. Also, the CLC420, a wideband voltage feedback op amp, can be used to implement classical integrator topologies.

Returning to the feedback resistor itself, never use a wirewound type for this, or any other, resistor in a broadband application. Also, trying to compensate the amplifier by using shunt capacitance across R_f will typically yield oscillations with the current feedback topology. It is much more fruitful to compensate by increasing the value of the feedback resistor, although a pot in the feedback path is not recommended.

Non-Inverting Source Impedance Considerations

The impedance seen looking out of the non-inverting input can play a strong role in determining an amplifier's overall performance. For very broadband applications, significant resistive source impedance, in conjunction with the part's input capacitance, can become the bandlimiting point in the system. This is normally not a problem for 50Ω terminations driven from a 50Ω source.

When running the amplifier in inverting mode, the non-inverting input would typically be grounded, either directly, or through an approximately 25Ω resistor. No attempt at source impedance matching on the two inputs for bias current cancellation should be made since the two bias currents for a current feedback amplifier are totally unrelated in both magnitude and polarity. Hence, unlike a voltage feedback op amp, there is no meaning to an offset current specification.

Generally, taking the non-inverting input to ground through a 25Ω resistor (for inverting amplifier applications) will eliminate any oscillations that might be seen due to negative input impedance effects at very high frequencies for the non-inverting input. It is oftentimes sufficient to simply ground the non-inverting input. But a careful check for low level oscillations above 500 MHz should be made, particularly for the faster amplifiers, if direct grounding is desired. If oscillations are observed, going to a 25Ω, or higher, resistor to ground will kill this self oscillation in the non-inverting input transistors.

When it is desired to AC couple the non-inverting input signal, as shown in *Figure 12*, particular attention must be paid to the effect the terminating resistor has on the DC operating point of the amplifier. Oftentimes, in an effort to achieve very low pole frequencies for the AC coupling (with-

Non-Inverting Source Impedance Considerations (Continued)

out an inordinately large coupling capacitor, C_t), R_t is made very large or, in some cases, not included.

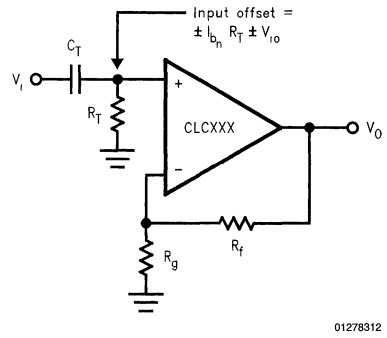


FIGURE 12. Effect of R_t on DC Input Offset Voltage

R_t, however, provides the DC current path for the non-inverting input bias current. Wideband amplifiers with a purely bipolar construction, as Comlinear's amplifiers typically are, have an input bias current ranging into the 10's of µA's. It is critical, therefore, to consider the effect a large R_t has on the input offset voltage (as shown in *Figure 12*). It is very easy, with large R_t, for this bias current requirement to have driven the input and output into saturation precluding proper high frequency operation. The effect of high R_t on the non-inverting noise current gain should also be considered. This noise current will add as an input noise voltage term dependent on the frequency dependent source impedance looking back out the non-inverting input.

Input and Output Voltage Range Considerations

The common mode input voltage range specification (CMIR) shown in the Comlinear data sheets indicates how near the specified supply voltages the non-inverting input voltage may be for proper operation. When operating properly, the inverting node voltage simply follows the non-inverting even for differential amp applications. For current feedback, this is due to the unity gain buffer from V^+ to V^-, while for voltage feedback, this is due the feedback loop.

Since all of the amplifiers are specified with balanced bipolar supply voltages, the CMIR and output voltage ranges are given as an allowed bipolar swing around ground. Both specifications are, however, indicating the required voltage headroom to the supplies on the non-inverting input and output pins respectively. Recasting these specifications as a required voltage headroom would allow input and output voltage ranges to be set for non-standard supply voltages.

In almost all cases, the maximum output voltage swing will be the limiting factor. Only at very low non-inverting gains, or for single amplifier differential operation, will the CMIR limit operation. The crossover non-inverting gain where the limiting point will change from input to output can be found by dividing the output voltage range by the input voltage range.

Operation that can cause the amplifier to exceed its output voltage range should be handled with special caution. Except for devices including an output limiting or clamping function (CLC500, CLC501, CLC502), exceeding the output voltage range will result in saturation internal to the amplifier. In all cases, this will result in very slow recovery time from overdrive. Since the error signal, for current feedback, is a current back to the inverting input, saturating the output voltage so that it no longer fully supplies the current being set up in the gain setting resistor will cause a current to build up in the inverting input. This is analogous to a voltage developing across the inputs of a voltage feedback amplifier when overdriven. This inverting input current can also limit recovery time from saturation effects internal to the amplifier.

All of the monolithic amplifiers from Comlinear can handle this saturation without damage. Extreme overdrives at the inputs can, however, exceed the current handling capability of the inverting node at which point a voltage will start to build across the inputs. This can, if large enough, break down some internal junctions leading to an increase in noise and possibly a shift in the DC characteristics of the amplifier.

Unless specifically indicated as overdrive protected (CLC205, CLC206, CLC207, CLC560, CLC561), special care should be taken not to drive any of the hybrid amplifiers into output saturation. Intended for the widest band, high power operation, these parts have enough internal drive capability to potentially damage themselves under a saturated output condition. Although not noted in the data sheets, the CLC231 and CLC232 low gain hybrid amplifiers can also be output stage saturated without damage. Even with an output saturable capability, all of the hybrid amplifiers need a careful analysis of junction temperatures to ensure that they do not exceed the rated maximum of 175°C.

From these considerations, it is not recommended that these unprotected hybrid amps be used as comparators—with the output intentionally forced from supply rail to supply rail. (The fast recovery clamping of the CLC501 does, however, offer an excellent opportunity for a very flexible high speed comparator function.) It is also not recommended to increase the value of the output stage collector resistors, for those parts bringing the output transistor collectors out separately, to act as a current limit since this will only saturate the output stage sooner. Generally, these resistors are intended only to de-couple high speed load current transients from the rest of the amplifier to enhance high speed settling times. It is possible, however, to use these resistors as an output short ckt current limit for those parts indicated as being overdrive protected. And finally, when using adjustable gain circuits, particularly with switching FETs, take care to keep the amplifiers out of an open loop situation during gain adjust.

For situations requiring a robust output overdrive capability, the clamping amplifiers are by far the best choice.

Cascaded Amplifier Considerations

High gain, cascaded amplifier applications require particular attention to a number of parasitic and operational effects. *Figure 13* shows an example circuit of 3-CLC401's configured for an overall gain of 1000 (60 dB) that will be used to demonstrate the suggestions developed here.

Several opportunities exist to develop an oscillator with very high gain, wideband circuits. The most common is direct output to input parasitic coupling. The output signal path should be physically isolated and, if necessary, shielded from the input signal path. When the final output is driving a relatively heavy AC load, either capacitive or, in this case,

Cascaded Amplifier Considerations (Continued)

resistive (100Ω), high frequency load currents through the supplies can couple back into early stages completing an oscillatory feedback loop. High frequency de-coupling directly on the supply pins of each stage are required at a minimum.

Interstage ferrite beads on the supply rails, as shown in *Figure 13*, can also be used to attenuate this feedback path. The power supply connections of *Figure 13* bring in the supplies at the final gain stage with LC PI filter stages used as it connects into earlier amplifier stages.

This provides increasing high frequency attenuation as we go to amplifier stages earlier on in the gain path. This is very desirable from both a PSRR standpoint and in breaking any feedback path through the power supplies from the output to input.

For close physically coupled amplifier stages, interstage matched impedances are probably not necessary. The two interstage 40Ω resistors of *Figure 13* are intended to isolate the input capacitance of the next stage from the output of the previous stage as suggested earlier in the discussion of parasitic load capacitance effects.

One key concern in a very high gain path is the build-up of DC errors. The circuit of *Figure 13* AC couples the gain setting resistors which reduces the DC gain to 1 for each amplifier stage. With only 1 mV input offset voltage at the first stage, the final amplifier output, (prior to the 6 dB matching loss), would be at 2V for this gain of 2000 if the 1 µF capacitors had not been used in the gain setting networks. If DC coupling at high gains is desired, some sort of composite correction loop (as described in Application Note OA-07) should be considered.

As a general rule, the highest gain stage should be used as the first stage to limit the impact on the overall input noise of the noise contribution of succeeding stages. Here, the equivalent input noise of the 2nd two stages would be divided by the gain of +20 in the first stage in adding to overall equivalent input noise. The total equivalent input noise for the circuit of *Figure 13* is 3 nV/$\sqrt{\text{Hz}}$. See Application Notes OA-12 for a noise calculation discussion and OA-14 for reducing the input noise for AC coupled applications.

Figure 14 shows the measured broadband gain and phase response for the circuit of *Figure 13*. Note that the measured −3 dB bandwidth, extending from 3 kHz to 200 MHz, achieves an equivalent 200 GHz Gain-Bandwidth product.

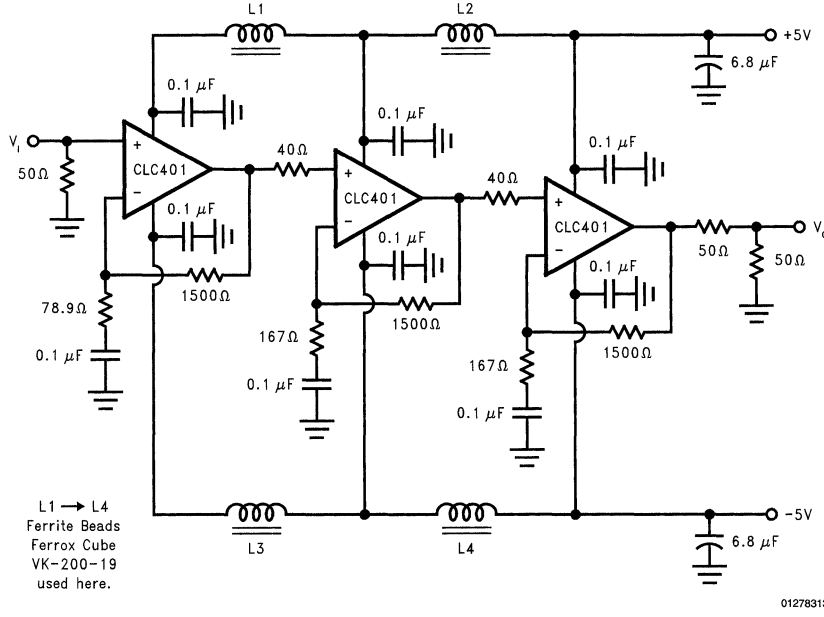


FIGURE 13. Wideband, High Gain, Cascaded Amplifiers

Cascaded Amplifier Considerations (Continued)

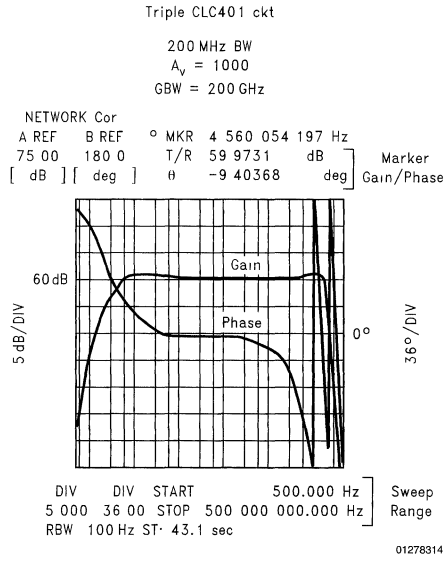


FIGURE 14. Measured Gain and Phase for High Gain Cascaded Circuit

The circuits included in this application note have been tested with National Semiconductor parts that may have been obsoleted and/or replaced with newer products. Please refer to the CLC to LMH conversion table to find the appropriate replacement part for the obsolete device.

Wideband AGC Amplifier as a Differential Amplifier

National Semiconductor
OA-16
Kern Wong

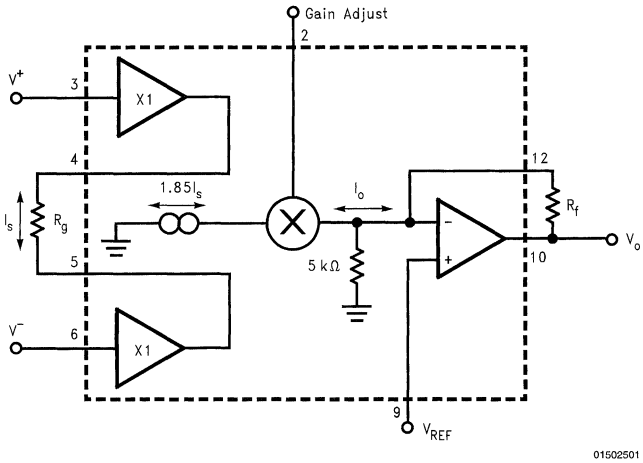


FIGURE 1. CLC520 Internal Block Diagram

The CLC520 is a very flexible DC-coupled Automatic Gain Control amplifier (AGC). Unique features include two closely-matched differential inputs, a wideband gain control channel (100 MHz), and a ground referenced DC-coupled output signal driven from a low output impedance amplifier. *Figure 1* illustrates the internal block diagram and pin assignments of the CLC520.

As shown in *Figure 1*, two unity-gain closed-loop input buffers on pins 3 and 6 are used to force the two input voltages to appear across the external resistor, R_g. The differential voltage across R_g generates a signal current which is amplified by a factor of 1.85 and fed into a two quadrant multiplier stage. The gain-adjustment voltage on pin 2 determines how much of this signal current makes it through the multiplier stage, with the remainder of the signal current being shunted to ground. The multiplier's output current then flows through the transimpedance amplifier formed by the external feedback resistor, R_f, and the internal amplifier. If the non-inverting input of this output amplifier, V_{REF}, is tied to ground then a ground-referenced DC-coupled replica of the differential voltage across R_g appears at the output of the op amp. The values of R_f and R_g, along with the gain-adjust voltage, determine the gain. Refer to the CLC520 data sheet for a more complete operational and performance discussion.

In order to implement a fixed-gain differential amplifier, the CLC520 will rely on R's very well-matched input buffers and it's differential-to-single-ended voltage conversion. For the purposes of this discussion, the gain-control input will be held at a fixed level to yield the maximum gain given by $1.85*R_f/R_g$. Thus, the differential signal gain depends only on the ratio of two external resistors and the internal current-mirror gain. Both R_f and R_g can be adjusted to yield a wide range of differential gains. As an example, the circuit of *Figure 2* is used to demonstrate the performance of the CLC520 in a fixed-gain differential amplifier configuration.

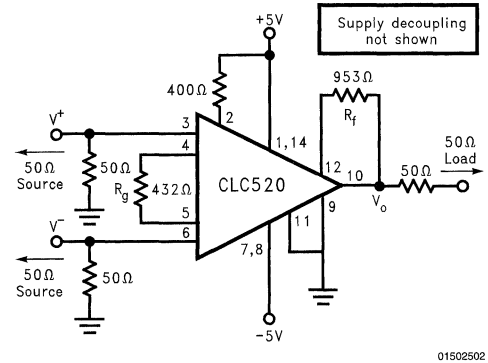


FIGURE 2. CLC520 Fixed-Gain Differential Amplifier Configuration

To demonstrate this application, the CLC520 is set up for a gain of 4.08V/V. The 50Ω impedance-matching resistor at the output effectively halves the differential gain to 2.04V/V (6.2 dB) at the 50Ω load. *Figure 3* shows the single-ended gain and phase response for both inputs on a linear frequency scale through 200 MHz. Note the 180° phase offset for the inverting-signal gain, indicating signal inversion. The slightly quicker roll-off of the inverting-gain response is consistent from part to part. This broadband performance is maintained as the part is operated at higher gain settings. It is the close, broadband, gain match of the inputs that allows the CLC520 to provide this wideband differential amplifier with very good common-mode signal rejection.

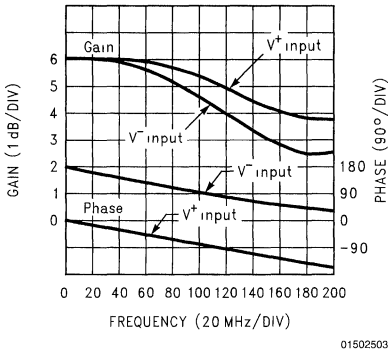


FIGURE 3. Single-Ended Gain and Phase

One measure of a good differential amplifier is its ability to reject common-mode signals. The common approach in describing this rejection is as a Common Mode Rejection Ratio (CMRR). The definition of CMRR is structured to allow the common-mode input signal to be placed in series with one of the differential inputs, (divided by CMRR), as an equivalent error term. With the following definition of CMRR, an equivalent input error term is placed at one of the inputs as shown in *Figure 4*.

Ad: Diff gain

Ac. Common-mode gain

$$CMRR \equiv \frac{Ad}{Ac}$$

$$CMRR = 20\log(Ad) - 20\log(Ac) \quad \text{Eq. 1}$$

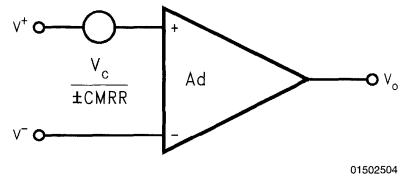


FIGURE 4. Input-Referred Common-Mode Error Model

V^+, V^-: pure differential signals

V_C: Common mode signal element

$$Vo = Ad(V^+ - V^-) \pm \frac{Vc}{CMRR} Ad$$

$$= Ad(V^+ - V^-) \pm \frac{Vc}{Ad/Ac} Ad$$

$$= Ad(V^+ - V^-) \pm VcAc$$

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This definition of CMRR essentially input refers an output signal due to a common-mode input signal which effectively holds the common-mode gain constant as the differential gain is changed. In computing the actual input-to-output signal gain due to a common-mode input voltage, simply use Ac Note, with Ac << 1, the logarithmic form of CMRR yields a large positive value. However, in computing the output common-mode signal, as shown in *Figure 4*, a linear (V/V) gain must be used and the error must be considered bipolar.

To measure the CMRR as defined in *Figure 4*, a measure of the pure differential gain must first be made. This measurement can be accomplished with the circuit of *Figure 5*. This circuit uses a transformer with a center tapped secondary to generate a pure differential input signal. The center tap also provides a DC path to ground supplying a DC-bias current to each of the inputs. It is necessary, in all cases, to carefully consider the source of these DC-bias currents. The transformer's frequency response was normalized prior to the gain and phase response measurement. Although using this transformer effectively AC couples the differential gain, it is important to recognize that the CLC520 is a truly DC-coupled device. The measured gain and phase for the circuit of *Figure 5* are shown in *Figure 6*. In order to maintain compatibility with the common-mode gain measurement, this *figure* is represented with a logarithmic frequency sweep from 100 kHz to 100 MHz. This circuit offers an exceptional gain-flatness with only 0.5 dB roll-off to 100 MHz.

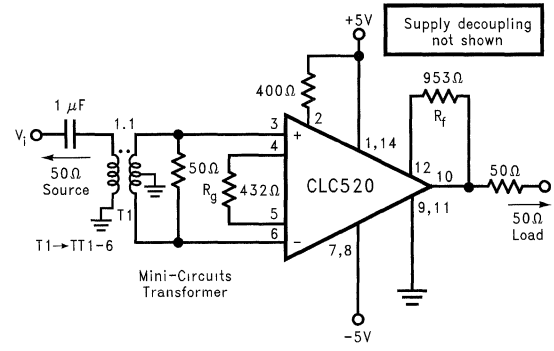


FIGURE 5. Differential Gain Test Circuit

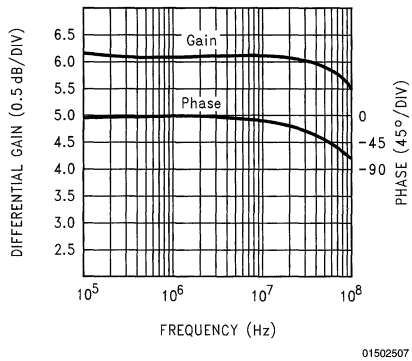


FIGURE 6. Differential Gain and Phase

The common-mode gain is measured by replacing each of the 50Ω input resistors of *Figure 2* with 100Ω while connecting the two inputs together. Tying the inputs together forces the input signals to be exactly the same while the resistor replacement retains the 50Ω input impedance match. In an actual application, connecting the two inputs together is impractical. In most cases the common-mode gain is not set by the amplifier, but by the mismatch of signal attenuations arising from each signal-source's impedance into the single-ended input impedance of each of the differential amplifier's inputs. A careful attention to the signal-source impedance match is necessary in order for the CMRR performance to be dominated by the amplifier and not by the deleterious effects of signal-source impedance mismatches. The common-mode gain measurement made here sidesteps those issues by simply tying the two inputs together. *Figure 7* shows the CMRR using the measured differential gain, the measured common-mode gain and the logarithmic form of CMRR (Eq.1).

The upper limit of CMRR at low-frequencies (below 100 kHz) is approximately 70 dB. This limit is set by the differential-to-single-ended conversion that takes place internal to the CLC520. At higher frequencies, the divergence in single-ended gains results in a 40 dB roll-off of CMRR at 10 MHz (shown in *Figure 3*). The CLC520's two high-impedance inputs with its internal wideband differential-to-single ended conversion combine to form a very wideband, high CMRR, differential amplifier.

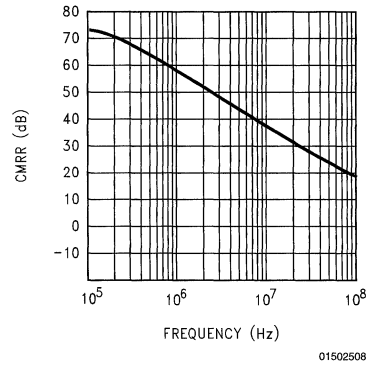


FIGURE 7. Common-Mode Rejection Ratio of the Circuit in *Figure 2*

Application Hints

IMPROVING CMRR

Several elements combine to set the frequency response of the CLC520. On the input side, parasitic capacitance to ground on either of the buffer outputs (pins 4 & 5) can cause high-frequency peaking. It is essential to keep the PC trace capacitance small and balanced when connecting R_g. For the tests shown here, R_g was soldered directly across the pins of the DIP while those pins were lifted from the board. On the output side, R_f will determine the frequency response of the output amplifier. Since this amplifier uses the current-feedback topology, R_f is the dominant element determining R_s frequency response. Increasing the value of R_f can be used to roll-off any peaking caused by parasitic capacitance on the output of the input buffers. However, it is preferable (from a noise standpoint) to minimize this parasitic on pins 4

Application Hints (Continued)

& 5 and use lower values of R_f (and therefore lower values of R_g for any particular gain). The CLC520 is designed for use with a 1 kW feedback resistor. Decreasing this value will cause the frequency response to peak, while increasing it will roll the response off. Most designs should start by first selecting a value for R_f and then determine the required R_g using the design equations found in the CLC520 data sheet. An additional constraint on lower values of R_g for good linear operation is that the maximum current supplied by the buffers through R_g should be kept within ±1.35 mA. This will set a maximum differential input voltage based on this current limit and the value of R_g.

Once the parasitic capacitance to ground on pins 4 & 5 has been minimized, a frequency response similar to that shown in *Figure 3* can be achieved for each of the two inputs separately. It is possible to take advantage of a parasitic gain imbalance in order to bring the inverting gain, at higher frequencies, into a closer match with the non-inverting gain. A closer gain match over a wider frequency range will improve the CMRR at high frequencies.

Although the equivalent circuit of *Figure 1* shows an output that depends only on the current through R_g, any additional current driven in to or out of the buffers will also generate an output signal. Therefore, by adding an AG coupled path to ground on the output of the inverting buffer, its response can be matched to that of the noninverting buffer. The circuit of *Figure 8* shows the original test circuit with the addition of this frequency-response matching network (R_T and C_T).

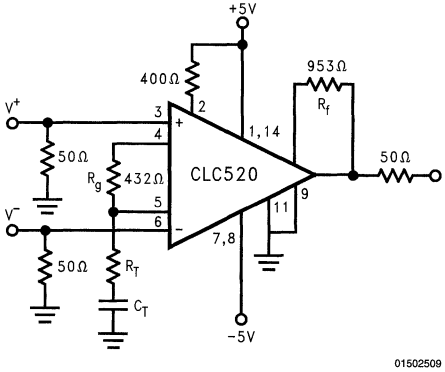


FIGURE 8. Differential Amplifier with Inverting Response Compensation

The single-ended frequency responses shown in *Figure 3* show a lower bandwidth for the inverting gain path vs. the non-inverting. This bandwidth mismatch is consistent from part to part and is set by the internal gain path. The buffer bandwidths are considerably higher and do not play a role determining this response. The following analysis will show how to select the appropriate values for R_T and C_T such that the frequency response of the inverting gain path can be matched to that of the non-inverting gain path.

$\omega+$: Non-inverting response pole

$\omega-$: Inverting response pole

Non-inverting frequency response:

$$A^+ = Ad\left(\frac{\omega^+}{s+\omega^+}\right)$$

Inverting frequency

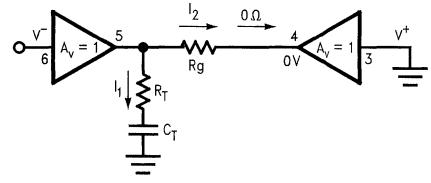
$$A^- = Ad\left(\frac{\omega^-}{s+\omega^-}\right)$$

Assuming $\omega- < \omega+$

Compensate A^- to achieve the following

$$A^+ = Ad\left(\frac{\omega^+}{s+\omega^+}\right)$$
$$= Ad\left(\frac{\omega^-}{s+\omega^-}\right)\left(\frac{s+\omega^-}{s+\omega^+}\right)\left(\frac{\omega^+}{\omega^-}\right)$$
$$= Ad\left(\frac{\omega^+}{s+\omega^+}\right)$$

The single-ended gain response of either input may be analyzed by grounding one input in order to determine the current generated at the output of the active buffer channel. Adding the R_T-C_T series combination will then provide a means of canceling the internal inverting-path pole with a zero, and replacing it with a pole that matches that seen by the single-ended non-inverting gain path. Note, adding this network will not impact the non-inverting response as long as it is assumed the buffers have zero output-impedance. The following analysis provides a method for computing the required values of R_T and C_T given R_g and the initial single-ended frequency response of each input as shown in *Figure 3*. Note: the input-to-output gain from the current produced in the compensation path is 1/2 that of the gain of the current produced through R_g.



Application Hints (Continued)

The output voltage due to an inverting input voltage is:

$$V_o = -\left[\left(1.85(I_2)R_f + \frac{1}{2}(1.85)I_1R_f\right)\right]\left(\frac{\omega^-}{s+\omega^-}\right)$$

$$I_1 = \left(\frac{V^-}{R_T + \frac{1}{sC_T}}\right) \text{ and } I_2 = \frac{V^-}{R_g};\ \omega^- \equiv \text{single-pole response}$$

Solving this for the gain to the output:

$$\frac{V_o}{V^-} = -1.85\,\frac{R_f}{R_g}\left(1+\frac{\frac{1}{2}R_g}{R_T}\right)\left(\frac{s+\frac{1}{\left(R_T+\frac{R_g}{2}\right)C_T}}{s+\frac{1}{R_TC_T}}\right)\left(\frac{\omega^-}{s+\omega^-}\right)$$

The non-inverting path has a gain of:

$$\frac{V_o}{V^+} = 1.85\,\frac{R_f}{R_g}\left(\frac{\omega^+}{s+\omega^+}\right),\ \omega^+ \equiv \text{single-pole response}$$

Equating these two gains requires a cancelling of the ω^- pole with the zero developed by the R_TC_T netrwork while placing the R_TC_T pole at ω^+.

Solving for R_T and C_T

$$R_T = \left(\frac{\frac{1}{2}R_g}{\frac{\omega^+}{\omega^-}-1}\right),\ C_T = \left(\frac{1}{R_T\omega^+}\right)$$

Estimating ω^+ and ω^- from the −1 dB roll-off frequencies of *Figure 3* and using

$\omega_{-3\ dB} = 1.97\ \omega_{-1\ dB}$ for a 1-pole response roll-off

$\omega^- = 2\pi$ (176 MHz)

$\omega^+ = 2\pi$ (240 MHz)

R_T and C_T therefore,

$$R_T = \left(\frac{216}{\frac{240}{176}-1}\right) = 595\Omega$$

$$C_T = \frac{1}{(595\Omega)2\pi(240\ \text{MHz})} = 1.12\ \text{pF}$$

Figures 9, 10 show the resulting single-ended frequency responses and the CMRR achieved through this compensation. Comparing *Figure 9* to *Figure 3* shows a much closer match over frequency. A significant improvement in the high-frequency CMRR has been achieved with this simple approach. C_T should be tuned for best CMRR at these higher frequencies. Note: when using different values of R_f and R_g, a remeasurement of the single-ended gains is required in order to provide the single ended gain poles necessary for this compensation analysis.

SETTING THE DIFFERENTIAL GAIN

To use the CLC520 at a fixed gain, it is best (from a temperature stability standpoint) to operate at its maximum gain, determined by R_f and R_g. The adjustable portion of the CLC520's gain is set by a two-transistor internal differential stage which compares the voltage seen on pin 2 to an internal reference voltage developed as a resistor divider from the positive supply to ground. With approximately 750W internally to ground on pin 2, the 400Ω external resistor shown on the circuits above will develop approximately 3.3V at pin 2, insuring the internal gain stage is fully switched to maximum gain.

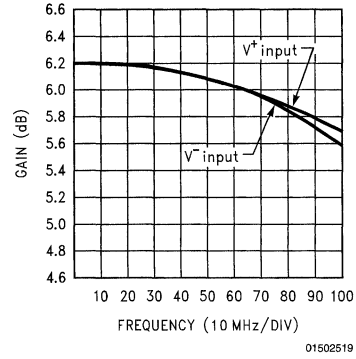


FIGURE 9. Single-Ended Gains With Inverting Path Compensation

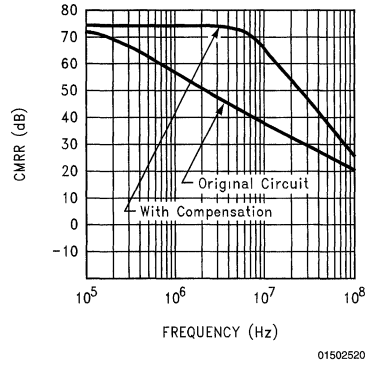


FIGURE 10. Improved CMRR with Better Response-Match Over Frequency

Note that the signal gain is also dependent on an internal current-mirror gain from the current developed in R_g to the multiplier stage. This nominal 1.85 factor will show some part-to-part tolerance and a slight temperature dependence.

Application Hints (Continued)

A ±3% part-to-part tolerance in this current gain along with a +80 ppm/°C temperature drift over 0°C–70°C may by used in the design of the CLC520 circuits.

USING THE GAIN ADJUST PIN

The fixed-gain differential amplifiers shown above can also be disabled with an open-collector pull-down device on pin 2 Once pin 2 is pulled below 0.4V, the gain will be attenuated by greater than 60 dB. Again, refer to the CLC520 data sheet for a full discussion of signal attenuation vs. gain-adjust voltage. Although the forward path can be shut down in this fashion, the output pin remains a low impedance driver· it will not be tri-stated. However, when driving several of these differential stages into an n:l MUX, shutting down the CLC520's gain will significantly improve the overall signal isolation at the MUX output.

An adjustable-gain differential amplifier can also be implemented with the CLC520. As discussed in the data sheet, the CLC520's gain adjustment is intended for operation inside an AGC loop. The gain-adjust accuracy and temperature stability of the CLC520 does not support open loop operation. A companion part, the CLC522, should be used if absolute gain accuracy and gain temperature stability is desired in an open loop (no feedback to the gain adjust pin), adjustable-gain differential-amplifier application.

INPUT NOISE

The equivalent input noise of the CLC520 is set largely by the value of R_g. As shown in the data sheet, a model for the input noise voltage due to R_g is simply R_g*I 8pA/√Hz. For any given gain setting, scaling down the values of R_f and R_g will reduce this input noise. Since R_f controls the output-amplifier stability, it cannot be made too small. For a fixed R_f, decreasing R_g will increase the signal gain. Since the input noise decreases at the same rate as the gain increases, the output noise remains nearly constant as R_g is decreased.

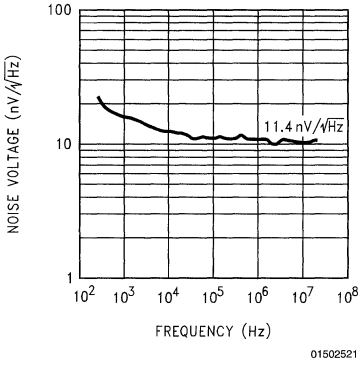


FIGURE 11. Input Noise Voltage

Figure 11 shows the measured input-referred spot noise voltage for the differential amplifier circuit of *Figure 5*.

APPLICATION SUGGESTION: WIDEBAND DIFFERENTIAL COAX LINE RECEIVER

It is often necessary to transfer high-speed signals from point to point via a matched-impedance coaxial line. *Figure 12* illustrates one receiver implementation using the CLC520 at a fixed gain. Since both buffers have high impedance inputs, a simple termination across the center conductor and properly terminate the cable allowing the differential signal to be picked-off and amplified by the CLC520. This circuit ties the coax shield into the local ground through a high-frequency blocking ferrite bead. This will help prevent coupling of high-frequency common-mode noise from the coaxial line onto the local ground, while at the same time setting the DC voltage and current operating point for the CLC520 inputs. This will also act to break high-frequency ground loops between different pieces of equipment

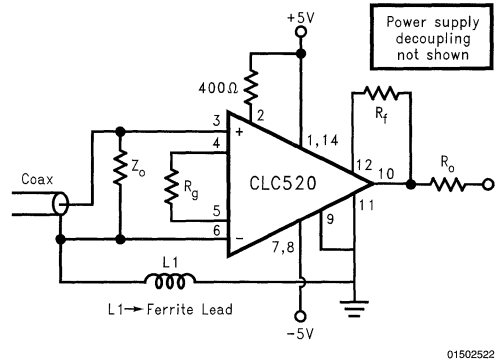


FIGURE 12. Differential Coax Line Receiver

APPLICATION SUGGESTION: VIDEO LOOP-THROUGH AMPLIFIER

The loop-through connection is one alternative to the impedance-matching approach of high-speed signals. For this approach, a high-input-impedance differential amplifier is simply placed across the center conductor and shield with minimal loading and no characteristic impedance-matching. Good high-frequency common mode rejection and good wideband differential amplification are essential for this application. The final destination of this daisy-chained connection terminates the cable in it's characteristic impedance.

An implementation of this loop-through connection using the CLC520 is shown in *Figure 13*. This circuit is a replication the circuit of *Figure 2* with some additional input resistors and a shutdown control gate.

The 20Ω resistors to ground will insure a DC-bias path for the input-stage bias currents. If it is absolutely certain that a DC path through both the center conductor and the shield will be maintained, the 20kΩ resistors can be eliminated with an overall improvement of VSWR. With only the 20kΩ termination, the CLC520's input offset current drift will generate a nominal input offset-voltage drift of 100mV/°C. It is desirable

Application Hints (Continued)

considering common mode rejection and offset-current drift, to keep these input termination resistors as large as possible. Ideally, the termination resistors should be eliminated if the bias current can be supplied by the cable. Remember, any mis-match in the single-ended attenuations from the center conductor's and shields source impedances into the CLC520's input impedances will degrade the CMRR.

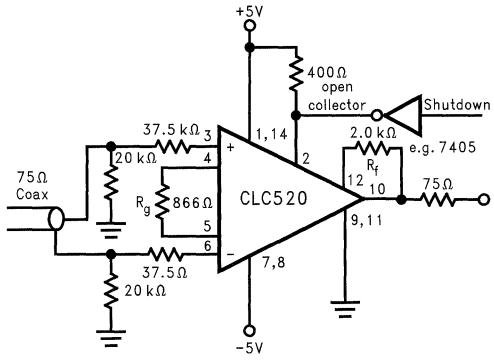


FIGURE 13. Video Loop-Through Connection Using A Wideband Differential Amplifier

The two series 37.5Ω resistors into pins 3 and 6 act to isolate the inputs from the cable reactance helping to maintain high-frequency input stability. These resistors, included with the parasitic input-capacitance to ground, will also form a matched-impedance termination for the cable at very high frequencies (>500 MHz): well beyond the signal frequencies of interest. The full signal level would be available to downstream stages using this wideband differential amplifier as a loop-through connection.

APPLICATION SUGGESTION: A VERY WIDEBAND PULSE-DIFFERENCING AMPLIFIER

With the addition of several frequency-response trims, the basic circuit *Figure 2* can be used to implement a very wideband pulse-differencing amplifier. Targeting a gain of +1V/V into a matched 50Ω load, bandwidths in excess of 300 MHz are achievable. *Figure 9* shows a typical single-sided pulse response. The input rise time for this test is approximately 800 ps. With a 1.15 ns output rise time and a 08 ns input rise time, the amplifiers actual rise time is approximately 0.8 ns for this 0.9V step at the load. Very similar and well-matched results can be achieved for both the inverting and non-inverting inputs.

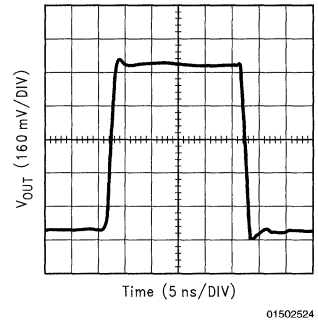


FIGURE 14. Very Wideband Single Input Pulse Response

APPLICATION SUGGESTION: ALTERNATIVE WIDEBAND DIFFERENTIAL AMPLIFIERS

Although the classical single op amp differential amplifier has found wide usage, several intrinsic problems limit it's performance. Both signal inputs are looking into relatively low and not necessarily well-matched impedances causing unbalanced signal-source attenuation, having the effect of degraded CMRR. Most simplified analysis assume a 0W source impedance in order to circumvent this problem. Furthermore, resistor inaccuracies, instead of the amplifier itself, will typically dominate the CMRR. These resistors and the amplifier's open-loop gain will determine the differential-to-single ended conversion carried out so well by the CLC520.

However, a classical single-amp differential amplifier combined with a pair of wideband, low-output-impedance buffers can be made to approach the performance of the CLC520. This approach may be preferred if lower input noise, lower power dissipation and improved DC-drift characteristics are worth a higher number of parts, lower differential bandwidth and the necessary precise resistor matching. *Figure 15* pro-

Application Hints (Continued)

vides an example of a single-amp differential amplifier using two buffers from a CLC114 quad buffer and a low-gain op amp with a differential gain of +1V/V.

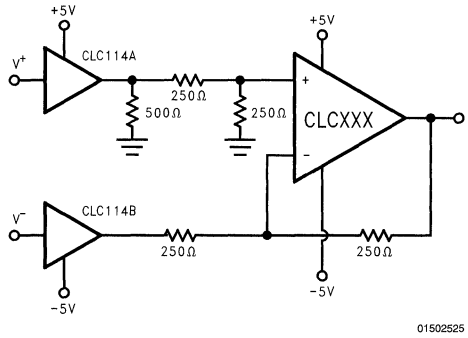


FIGURE 15. Single Amplifier Differential Amplifier With Input Buffering

The two input-barriers provide many of the same advantages found with the CLC520 inputs. Any of the input terminations described for the CLC520 may be used here as well. The optional 500Ω resistor to ground on the output of the non-inverting buffer provides a means of matching the loads seen by both buffer outputs. This load matching will improve the high frequency response-match. The four 250Ω resistors should be matched as closely as possible since any mismatch will degrade the CMRR. The recommended low-gain differencing amplifier may be chosen from the following selection of National's wideband low-gain amplifiers.

CLC402 Low-gain high-accuracy current-feed back amplifier

Lower CMRR than the CLC420 with wider bandwidth and better fine-scale, pulse-settling accuracy.

CLC409 Very wideband, low-gain, current-feed back amplifier.

CLC410 Intermediate performance, low-gain, current-feedback amplifier. This part also includes a shutdown feature and provides the best dG/d_ for composite video applications.

CLC420 Unity-gain stable voltage feedback amplifier. This part will provide the best CMRR and DC accuracy

CLC502 Similar to the CLC402 but with an output-clipping feature

All of these parts are optimized for the 250Ω feedback resistor shown in the circuit of *Figure 15*.

Conclusion

As operating speeds have increased, the need for a wide-bandwidth high-CMRR differential amplifiers has increased. National's CLC520 & CLC522 provide all of the required building blocks integrated into one part. Although intended for adjustable gain requirements, operating the CLC520 at a fixed gain is perfectly acceptable and preferable in a differential receiver application. Signal bandwidths in excess of 150 MHz over a wide range of gains, along with CMRR exceeding 60 dB through 10 MHz, and two matched high-impedance inputs provide all the essential requirements for wideband differential amplification. In some applications using wideband, low power buffers and a standard single op amp differential amplifier topology offers certain advantages over the CLC520 approach.

The circuits included in this application note have been tested with National Semiconductor parts that may have been obsoleted and/or replaced with newer products. Please refer to the CLC to LMH conversion table to find the appropriate replacement part for the obsolete device.

Current-Feedback Myths Debunked

National Semiconductor
OA-20
Arne Buck

Introduction

Mystery needlessly surrounds the operation and use of current feedback operational amplifiers. Many engineers refuse to design with these op amps due to misunderstandings which are easily rectified.

Much has been written to date on the internal circuitry of current feedback op amps. These open-loop "tutorials" obfuscate how current feedback works in a closed-loop circuit. Practical op amp circuits are closed-loop feedback systems which yield to classical control theory analysis. Analog circuit designers are comfortable with voltage feedback op amps in a closed-loop circuit and with the familiar ideal op amp approximations feedback affords. It will be shown that current feedback op amps can be analyzed in an analogous fashion. Once this closed-loop similarity is appreciated, it is easy to see that most circuits commonly built with voltage feedback op amps can be realized with a current feedback op amp, and with better results at high frequencies.

Refer to *Figure 1* to review the open-loop terminal characteristics of a voltage feedback amplifier. Ideally the non-inverting input impedance is infinite, as is the inverting input impedance. The output is a voltage source, the output impedance of which is zero. This voltage source is controlled by the potential difference between the two op amp input terminals. This is the error voltage, hence the term voltage feedback. Feedback will drive the error voltage to zero. The open-loop dynamics are contained in A(s). This A(s) is a dimensionless gain, often represented in units of volts per volt or decibels.

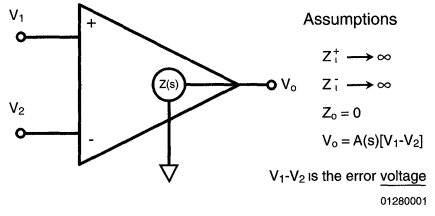


FIGURE 1. Voltage Feedback Op Amp

A typical voltage feedback circuit is shown in *Figure 2*, the inverting amplifier. The transfer function is developed from the following equations:

$$V_1 = 0,\ V_o = -A(s)V_2,\ (V_i - V_2)/R_1 = (V_2 - V_o)/R_2.$$

As A(s) approaches infinity, the closed-loop gain is $-(R_2/R_1)$. The frequency response of the closed-loop circuit is determined by the denominator of the transfer function. Both the noise gain $(1 + R_2/R_1)$ of the circuit and the frequency-dependent source (A(s)) appear in the denominator, linking the closed-loop gain and bandwidth.

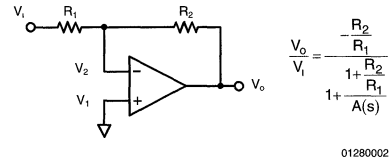


FIGURE 2. Voltage Feedback Op Amp Inverting Gain

The familiar Bode plot of this circuit is shown in *Figure 3*. The amplifier is typically compensated with a dominant low-frequency pole to ensure stability down to a specified minimum gain, often unity. In the region where the one-pole approximation of the open-loop response is valid, the phase is around −90°. This is the gain-bandwidth product region. The intersection of the zero-slope noise gain line and the open-loop gain curve determines the closed-loop system −3 dB bandwidth. A high gain circuit will have less bandwidth than a lower gain circuit. As the circuit moves to lower gains, bandwidth increases, phase margin is lost and stability suffers.

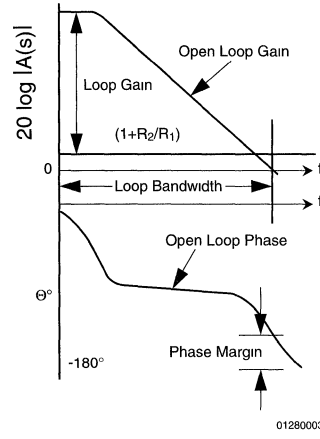


FIGURE 3. Bode Plot

The open-loop terminal characteristics of a current feedback amplifier are depicted in *Figure 4*. There is a unity-gain buffer between the two op amp inputs. This buffer ideally has infinite input impedance and zero output impedance. Thus the non-inverting input impedance of the current feedback op amp is infinite, and the inverting input impedance is zero. The output is a voltage source, so the output impedance is

zero. This voltage source is controlled by the current out of the inverting input. This is the error current, hence current feedback. Feedback forces the error current to zero. The open-loop dynamics are determined by Z(s). This Z(s) is a current controlled voltage source which has units of transimpedance, ohms.

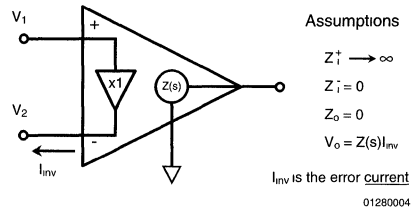


FIGURE 4. Current Feedback Op Amp

The inverting amplifier employing a current feedback op amp is shown in *Figure 5*. The transfer function is derived from the following equations:

$$V_1 = 0,\ V_o = Z(s)I_{inv},\ (V_i/R_1) + I_{inv} = -(V_o/R_2)$$

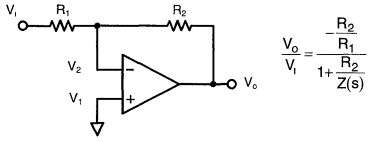


FIGURE 5. Current Feedback Op Amp Inverting Gain

As Z(s) approaches infinity, the closed-loop gain is $-(R_2/R_1)$. Notice that only the feedback resistor appears in the characteristic equation, in the term with Z(s). The closed-loop gain has been decoupled from the frequency response determining term of the transfer function. Only the feedback resistor affects the closed-loop frequency response.

A Bode plot for the circuit is shown in *Figure 6*. A current feedback amplifier is also compensated with a dominant low-frequency pole. This pole is usually at a higher frequency than that of a voltage feedback op amp. A current feedback op amp is commonly compensated for maximally flat response at a specified closed-loop gain and with a specified feedback resistor. The phase is approximately –90° where this one-pole approximation is valid. The ideal current feedback op amp does not have a gain-bandwidth product. The closed-loop bandwidth is determined by the feedback resistor, not the closed-loop gain. One could entertain the idea of a "feedback-resistor-bandwidth" product. The intersection of the zero-slope feedback resistor line and the open-loop transimpedance curve yields the closed-loop –3dB bandwidth. A circuit with a higher feedback resistor will have reduced bandwidth. This is a good way to over-compensate the current feedback op amp. A feedback resistor of twice the manufacturer's recommended value will cut the circuit bandwidth in half. As the feedback resistance, or impedance, is reduced to a lower value, there is a loss of phase margin. As can be seen from the transfer function in *Figure 5*, if the negative of the loop transmission, $(R_2/(Z)s)$, equals –1 the loop is unstable.

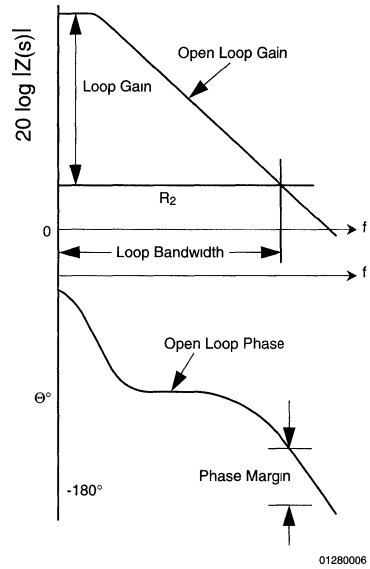


FIGURE 6. Bode Plot

The design trade-offs between current feedback and voltage feedback differ. Voltage feedback allows freedom of choice of the feedback resistor (or impedance) at the expense of sacrificing bandwidth for gain. Current feedback maintains high bandwidth over a wide range of gains at the cost of limiting the feedback impedance.

For example, a common error in using a current feedback op amp is to short the inverting input to the output in an attempt to build a voltage follower. This circuit will oscillate. The circuit is perfectly stable if the recommended feedback resistor is used in place of the short. Similarly, an integrator is commonly accomplished by placing a capacitor between the inverting input and output. At high frequencies a capacitor has a low impedance and can easily have an impedance less than that required for stability. The proper feedback resistor in series with the feedback capacitor will stabilize the amplifier, and introduce a high frequency zero into the integrator transfer function.

Another aspect of current feedback op amps which causes much consternation is the low open-loop inverting input impedance. This feature, which causes the decoupling of closed-loop gain and bandwidth, is often viewed as making current feedback op amps unsuitable for use as differential amplifiers. In fact, the low inverting input impedance can result in a better high-frequency differential amplifier than a similar circuit built with a voltage feedback op amp.

First consider the closed-loop driving-point impedance of an op amp, regardless of the nature of the error signal. The circuit and equations to find this closed-loop impedance are shown in *Figure 7*. The resistor, R, is the open-loop inverting input impedance. Note that R is simply a resistance. A

voltage feedback amplifier will have an R approaching infinity; in a current feedback op amp R approaches zero. A test current, I_T, is applied to the inverting input and the inverting node currents are summed. To find the closed-loop inverting input impedance of either amplifier simply substitute the proper form of the output voltage, V_o.

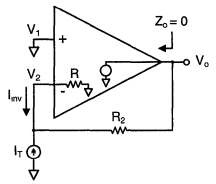


FIGURE 7. Closed-Loop Inverting Input Impedance

In the case of the voltage feedback op amp, $V_o = -V_2A(s)$ for this circuit. The result, $Z_{inv}(s)$, is in *Figure 8*. The familiar result is that when A(s) approaches infinity, the incremental inverting impedance approaches zero. This is the incremental or virtual ground on which much first-order op amp analysis is based.

$$\text{Traditional Op Amp } V_o = -V_2A(s)$$

$$Z_{inv}(s) = R \,||\left(\frac{R_2}{1+A(s)}\right) \xrightarrow{A(s)\to\infty} 0$$

$$\text{Current Feedback Op Amp } V_o = -V\left(\frac{Z(s)}{R}\right)$$

$$Z_{inv}(s) = R \,||\left(\frac{R_2}{1+\frac{Z(s)}{R}}\right) \xrightarrow{R\to 0} 0$$

$$\text{or } \xrightarrow{Z(s)\to\infty} 0$$

01280008

FIGURE 8. Inverting Input Impedance Comparison

The output voltage is derived differently in the current feedback op amp. When $V_o = -V_2(Z(s)/R)$ is substituted, the result is in *Figure 8* also. It can be seen that two mechanisms force the inverting input impedance to a low value, ideally zero. When Z(s) is very large, $Z_{inv}(s)$ goes to zero. In addition, as R goes to zero so does the closed-loop inverting input impedance. The topology of the input buffer keeps R small to very high frequencies. Thus a current feedback op amp can have a better virtual ground at the inverting input than a voltage feedback amp, especially at high frequencies.

A summary of the above discussion is tabulated in *Figure 9*. The voltage difference between the input terminals is zero. Voltage feedback drives this difference to zero. The current feedback amplifier input buffer forces the two input terminals to equal voltages. Both amplifier types have a high non-inverting input impedance, so the non-inverting current is small. A voltage feedback op amp has a high open-loop inverting input impedance, thus the inverting current approaches zero. Current feedback forces the inverting current to zero. Both op amps display similar input voltage and current characteristics. Only the mechanism forcing these to zero differs.

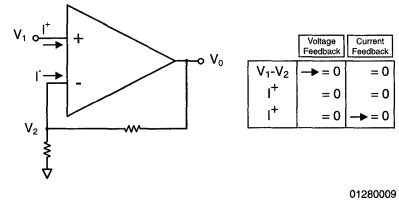


FIGURE 9. Op Amp Comparison Closed-Loop Operation

It can now be seen that from a closed-loop standpoint both current and voltage feedback op amps allow the same ideal op amp assumptions to be made. Voltage feedback has a gain-bandwidth product which limits the lowest stable gain. Current feedback displays a "feedback-resistor-bandwidth" product which limits the lowest stable feedback impedance.

The inverting input impedance of an ideal voltage feedback op amp in a closed-loop circuit is zero. Feedback accomplishes this by dividing a high open-loop impedance by a high loop gain. The open-loop inverting input impedance of an ideal current feedback op amp is zero. A practical current feedback op amp has a finite inverting input impedance, less than 100Ω. Feedback reduces this further by dividing the initially low open-loop inverting input impedance by the loop transmission. The result is a better incremental ground at the inverting input to very high frequencies.

As both amplifier types are used in closed-loop topologies, the same methods of analysis are equally applicable. Now that this is seen, current feedback op amps can easily be designed into amplifiers of any arbitrary gain (inverting and non-inverting), integrators, differential amplifiers (*Figure 10*), and current-to-voltage converters, commonly known as transimpedance amplifiers (*Figure 11*).

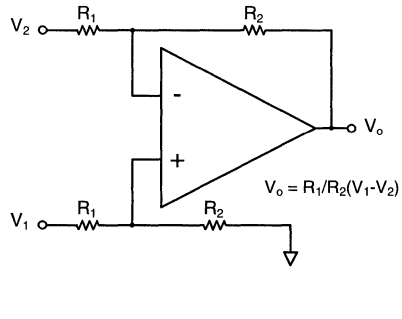


FIGURE 10. Difference

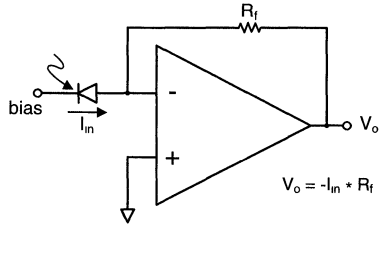


FIGURE 11. Transimpedance Amplifier with a Current Feedback Op Amp

Component Pre-distortion for Sallen Key Filters

National Semiconductor
OA-21
Kumen Blake

Introduction

This revision obsoletes the previous revision of this Application Note, and covers additional material.

This Application Note shows a simple component pre-distortion method that works for many popular Sallen-Key (also called KRC or VCVS [voltage-controlled, voltage-source]) filter sections. This method compensates for voltage-feedback and current-feedback op amps. Several examples illustrate this method.

KRC active filter sections use an op amp and two resistors to set a non-inverting gain of K. resistors and capacitors placed around this amplifier provide the desired transfer function. The op amp's finite bandwidth causes K to be a function of frequency. For this reason, KRC filters typically operate at frequencies well below the op amp's bandwidth ($f << f_{3dB}$).

"Pre-distortion" compensates for the op amp's finite bandwidth by modifying the nominal resistor and capacitor values. The pre-distortion method in the Application Note compensates for the op amp's group delay which is approximately constant when $f << f_{3dB}$.

One possible design sequence for KRC filters is:

1. Design the filter assuming an ideal op amp (K is assumed constant over frequency)
   - Select components for low sensitivities
   - Do a worst case analysis
   - Do a temperature analysis
1. Pre-distort the resistors and capacitors to compensate for the op amp's group delay
2. Compensate for parasitic elements

Filter Component Pre-Distortion

This section outlines a simple pre-distortion method that works for many popular Sallen-Key filters using current-feedback or voltage-feedback op amps. Other more general pre-distortion methods are available (see reference [4]) which require more design effort.

To pre-distort your filter components:

1. Calculate the op amp's delay:

$$\tau_{oa} \approx -\frac{1}{f_c} \bullet \frac{\phi(f_c)}{360°}$$

where $\phi(f)$ is the op amp phase response in degrees, and f_c is the cutoff frequency (passband edge frequency) of your filter

- Subtract the phase shift caused by your measurement jig from any measured value of $\phi(f_c)$
- The group delay is specified at f_c because it has the greatest impact on the filter response near the frequency.
- Other less accurate estimates of the op amp delay at f_c are:
  - Step response propagation delay
  - $1/(2\pi f_{3dB})$

2. The time delay around the filter feedback loop ("electrical loop delay") adds to the op amp delay.

   For this reason,

   - Make the filter feedback loop as physically short as possible.
   - If you need greater accuracy in the following calculation, use the electrical loop delay (τ_{eld}) instead of the op amp delay (τ_{oa}):

$$\tau_{eld} \leftarrow \tau_{oa}$$

   See *Appendix B* for information on calculating τ_{eld}.

3. Replace K in the filter transfer function with a simple approximation to the op amp's frequency response
   - Start with a simple, single pole approximation:

$$K \leftarrow K/(1 + \tau_{oa}s)\ ,\ s = j\omega$$

   - Alter the approximation to K and simplify:
   - *Do not create new terms* (a coefficient times a new power of s) in the transfer function *after simplifying*
   - Convert $(1 + \tau_{oa}s)$ to the exponential form (a pure time delay) when it multiplies, or divides, the entire transfer function
   - Do not change the gain at $\omega \approx \omega_p$ in allpass sections
   - The most useful alterations to K are:

$$\frac{K}{1 + \tau_{oa}s} \approx K \bullet \frac{1 - (\tau_{oa}/2)s}{1 + (\tau_{oa}/2)s}$$

$$\approx K(1 - \tau_{oa}s)$$

$$\approx Ke^{-\tau_{oa}s}$$

   All of these approximations are valid when: $\omega << 1/\tau_{oa}$

4. Use an op amp with adequate bandwidth (f_{3db}) and slew rate (SR):

$$f_{3db} \geq 10 f_H$$

$$SR > 5 f_H V_{peak}$$

Where f_H is the highest frequency in the passband of the filter, and V_{peak} is the largest peak volage. This increases the accuracy of the pre-distortion algorithm. It also reduces the filter's sensitivity to op amp performance changes over temperature and process. Make sure the op amp is stable at the gain of $A_V = K$.

Appendix A contains examples using transfer functions. The next section will apply the results from *Appendix A*.

KRC Lowpass Biquad

The biquad shown in *Figure 1* is a Sallen-Key lowpass biquad. V_{in} needs to be a voltage source with low output impedance. R_1 and R_2 attenuate V_{in} to keep the signal within the op amp's dynamic range. Using Example 2 in *Appendix A*, we can show:

KRC Lowpass Biquad (Continued)

$$\frac{V_o}{V_{in}} \approx \frac{H_o}{1 + \left(1/(\omega_p Q_p)\right)s + \left(1/\omega_p^2\right)s^2} \bullet e^{-\tau_{oa}s}$$

$\omega, \omega_p << 1/\tau_{oa}$

where

$\alpha = R_2/(R_1 + R_2)$

$K = 1 + R_f/R_g$

$H_o = \alpha K$

$R_{12} = (R_1 \parallel R_2)$

$1/(\omega_p Q_p) = R_{12}C_5(1 - K) + R_3C_4 + R_{12}C_4$

$1/\omega_p^2 = R_{12}R_3C_4C_5 + K\tau_{oa}R_{12}C_5$

After selecting α and R_{12}, calculate R_1 and R_2 as:

$R_1 = R_{12}/\alpha$

$R_2 = R_{12}/(1 - \alpha)$

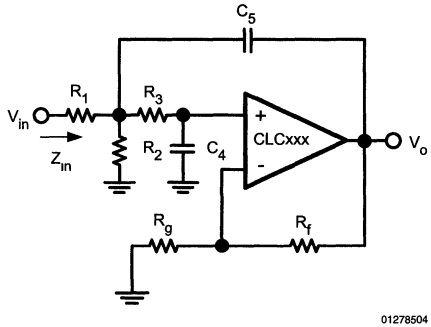


FIGURE 1. Lowpass Biquad

To pre-distort this filter:

1. Design the filter assuming K constant ($\tau_{oa} = 0$). Use low values for K so that:
   — τ_{oa} will have less impact on the biquad's response.
   — For voltage-feedback op amps, τ_{oa} will be smaller ($\tau_{oa} \approx$ K divided by the gain-bandwidth products).
2. Recalculate the resistors and capacitors using the pre-distorted values of ω_p and Q_p ($\omega_{p(pd)}$ and $Q_{p(pd)}$ that will compensate for τ_{oa}:

$1/\omega_{p(pd)}^2 = 1/\omega_{p(nom)}^2 - K\tau_{oa}R_{12}C_5$

$= R_{12}R_3C_4C_5$

$1/(\omega_{p(pd)}Q_{p(pd)}) = 1/(\omega_{p(nom)}Q_{p(nom)})$

$= R_{12}C_5(1 - K) + R_3C_4 + R_{12}C_4$

where $\omega_{p(nom)}$ and $Q_{p(nom)}$ are the nominal values of ω_p and Q_p

3. Repeat step 2 until $\omega_p \approx \omega_{p(nom)}$ and $Q_p \approx Q_{p(nom)}$, where:

$1/\omega_p^2 = 1/\omega_{p(pd)}^2 + K\tau_{oa}R_{12}C_5$

$1/(\omega_p Q_p) = 1/(\omega_{p(pd)}Q_{p(pd)})$

Design Example

The circuit shown in fig 2 is a 3rd-order Chebyshev lowpass filter. Section A is a buffered single pole section, and Section B is a lowpass biquad. Use a voltage source with low output impedance, such as the CLC111 buffer, for V_{in}.

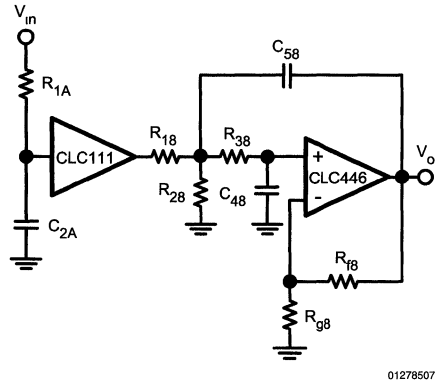


FIGURE 2. Lowpass Filter

The nominal filter specification are:

f_c = 50MHz (passband edge frequency)

f_s = 100MHz (stopband edge frequency)

A_p = 0.5dB (maximum passband ripple)

A_s = 19dB (minimum stopband attenuation)

H_o = 0dB (DC voltage gain)

The 3rd-order Chebyshev filter meets our specifications (see References [1-4]. The resulting -3dB frequency is 58.4MHz. The pole frequencies and quality factors are:

Design Example (Continued)

Section	A	B
$\omega_p/2\pi$ [MHz]	53.45	31.30
Q_p [ ]	1.706	–

Overall Design:

1. Use the CLC111 for section A. This is a closed loop buffer
   - f_{3dB} = 800MHz > $10f_c$ = 500MHz
   - SR = 3500V/µs, while a 50MHz, $2V_{pp}$ sinusoid requires more than 250V/µs
   - $\tau oa \approx$ 0.28ns at 50MHz
   - $C_{ni(111)}$ = 1.3pF (input capacitance)
2. Use the CLC446 for section B. This is a current feedback op amp
   - f_{3dB} = 400MHz ≈ $10f_c$ = 500MHz
   - SR = 2000V/µs > 250V/µs (see item #1)
   - $\tau_{oa} \approx$ 0.56ns at 50MHz
   - $C_{ni(446)}$ = 10pF (non-inverting capacitance)
3. Use 1% resistors (chip metal film, 1206 SMD, 25ppm/°C)
4. Use 1% capacitors (ceramic chip, 1206 SMD, 100ppm/°C)
5. Use standard resistor and capacitor values
6. See Reference [6] for the low-sensitivity design of this biquad.

Section A Pre-distortion:

We selected R_{1A} for noise, distortion and to properly isolate the CLC111's output and C_{2A}. The pole is then set by C_{2A}. The pre-distorted value of R_{1A}, that also compensates for $C_{ni(111)}$, is (see Example 1 in *Appendix A*):

$$R_{1A} = (1/\omega_p - \tau_{oa})/(C_{2A} + C_{ni(111)})$$

The resulting components are in the table below:

- The Initial Value column shows the values before pre-distortion
- The Adjusted Value column shows the values after pre-distortion, and adjusting C_{2A} for $C_{ni(111)}$
- The Standard Value column shows the nearest available standard 1% resistor and capacitor values

Component	Value		
	Initial	Adjusted	Standard
R_{1A}	108Ω	100Ω	100Ω
C_{2A}	47pF	47pF	47pF
$C_{ni(111)}$	–	1.3pF	1.3pF

Section B Pre-distortion:

1. The design started with these values:

$$\omega_{p(nom)} = 2\pi\ (53.45\text{MHz})$$
$$Q_{p(nom)} = 1.706$$
$$K_B = 1.50$$
$$\alpha_B = 0.667$$
$$C_{4B} + C_{ni(446)} = 4.7\text{pF}$$
$$C_{5B} = 47\text{pF}$$

2. Iteration 0 shows the initial design results. Iterations 1-3 pre-distort R_{12B} and R_{3B} to compensate for the CLC446's group delay:

Iteration	0	1	2	3
$\omega_{p(pd)}/2\pi$ [MHz]	53.45	63.21	60.65	61.21
$Q_{p(pd)}$ [ ]	1.706	1.443	1.503	1.490
R_{12B} [Ω]	64.00	50.17	53.32	52.63
R_{3B} [Ω]	627.0	571.9	584.9	581.9
$K\tau_{oa}R_{12B}C_{5B}$ [ns^2]	2.527	1.981	2.105	2.078
$\omega_p/2\pi$ [MHz]	47.15	55.18	53.08	53.53
Q_p [ ]	1.934	1.653	1.718	1.703

3. The resulting components are:

Component	Value		
	Initial	Adjusted	Standard
R_{1B}	96.0Ω	78.9Ω	78.7Ω
R_{2B}	192Ω	158Ω	158Ω
R_{3B}	627Ω	582Ω	576Ω
C_{4B}	4.7pF	3.7pF	3.6pF
$C_{ni(446)}$	–	1.0pF	1.0pF
C_{5B}	47pF	47pF	47pF
R_{fB}	348Ω	348Ω	348Ω
R_{gB}	696Ω	696Ω	698Ω

Figure 3 and *Figure 4* show simulated gains for the following conditions:

1. Ideal (Initial Values, $\tau_{oa} = 0$)
2. Without Pre-distortion (Initial Values, $\tau_{oa} \neq 0$)
3. Without Pre-distortion (Standard Values, $\tau_{oa} \neq 0$)

Design Example (Continued)

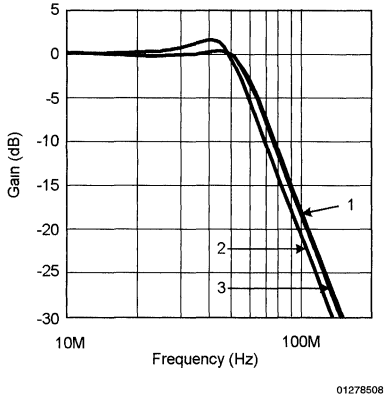


FIGURE 3. Simulated Filter Magnitude Response

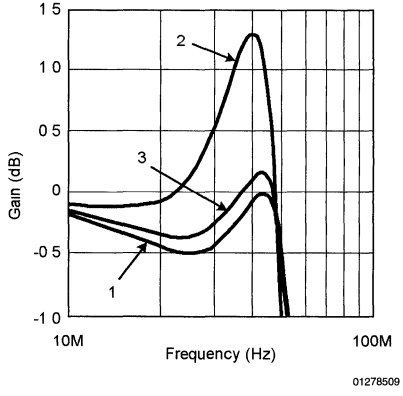


FIGURE 4. Simulated Filter Magnitude Response

SPICE Models

SPICE models are available for most of Comlinear's amplifiers. These models support nominal DC, AC, AC noise and transient simulations at room temperature.

We recommend simulating with Comlinear's SPICE models to:

- Predict the op amp's influence on filter response
- Support quicker design cycles

Include board and component parasitics to obtain a more accurate prediction of the filter's response, and to further improve your design.

To verify your simulations, we recommend bread-boarding your circuit.

Summary

This Application Note demonstrates a component pre-distortion method that:

- Works for popular Sallen-Key filter sections
- Is quick and simple to use
- Shows the op amp's effect on the filter response
- Gives reasonable op amp selection criteria

Appendix A and the *Design Example* section contain illustrations of this method.

Appendix A – Transfer Function Examples

Example 1:

Single pole section, K in the numerator:

$$\frac{V_o}{V_{in}} \approx \frac{K}{1 + (1/\omega_p)s}$$

$$1/\omega_p = \tau_1$$

where τ_1 is a time constant set by resistors and capacitors.

To include the op amp's group delay, substitute for K and simplify:

$$\frac{V_o}{V_{in}} \approx \frac{1}{1 + (\tau_1)s} \bullet \frac{K}{1 + (\tau_{oa})s}$$

$$\approx \frac{K}{1 + (1/\omega_p)s} \; ; \quad \omega, \omega_p << 1/\tau_{oa}$$

$$1/\omega_p = \tau_1 + \tau_{oa}$$

Notice that:

- There are no new powers of s in the transfer function
- Changing the resistor and capacitor values can compensate for τ_{oa}
- The approximation is reasonably accurate when f << f_{3dB}

  To pre-this filter section, recalculate the resistors and capacitors using the equation:

$$\tau_1 = 1/\omega_p - \tau_{oa}$$

Example 2:

Single pole allpass section, K times the numerator:

$$\frac{V_o}{V_{in}} \approx \frac{1 - (1/\omega_z)s}{1 + (1/\omega_p)s} \bullet K$$

$$1/\omega_p = \tau_1$$

$$1/\omega_z = \tau_2$$

where τ_1 and τ_2 are time constants set by resistors and capacitors. This section operates as an allpass filter when:

$$\tau_1 = \tau_2$$

Appendix A – Transfer Function Examples (Continued)

To include the op amp's group delay, substitute for K and simplify. Since this is an allpass transfer function, the approximation to K does not change gain at $\omega = \omega_p$:

$$\frac{V_o}{V_{in}} \approx \frac{1 - (\tau_2)s}{1 + (\tau_1)s} \bullet \frac{1 - (\tau_{oa}/2)s}{1 + (\tau_{oa}/2)s} \bullet K$$

$$\approx \frac{1 - (1/\omega_z)s}{1 + (1/\omega_p)s} \bullet K$$

$$\omega, \omega_p, \omega_z << 1/\tau_{oa}$$

$$1/\omega_z = \tau_2 + \tau_{oa}/2$$

$$1/\omega_p = \tau_1 + \tau_{oa}/2$$

Notice that:

- There are no new powers of s in the transfer function
- The gain at ω_p does not change (this is an allpass section)
- Changing the resistor and capacitor values can compensate for τ_{oa}
- The approximation is reasonably accurate when $f << f_{3dB}$

To pre-distort this filter, recalculate the resistor and capacitors using the equations:

$$\tau_2 = /\omega_z - \tau_{oa}/2$$
$$\tau_1 = /\omega_p - \tau_{oa}/2$$

Example 3:

Biquad section, s term in the denominator that includes K:

$$\frac{V_o}{V_{in}} \approx \frac{1}{1 + (1/(\omega_p Q_p))s + (1/\omega_p^2)s^2}$$

$$1/(\omega_p Q_p) = \tau_1 + K\tau_2$$

$$1/\omega_p^2 = \tau_3^2$$

where τ_1, τ_2 and τ_3 are time constants set by resistors and capacitors.

To include the op amp's group delay, substitute for K and simplify:

$$\frac{V_o}{V_{in}} \approx \frac{1}{1 + (\tau_1 + K(1 - \tau_{oa}s) \bullet \tau_2)s + (\tau_3^2)s^2}$$

$$\approx \frac{1}{1 + (1/(\omega_p Q_p))s + (1/\omega_p^2)s^2}$$

$$\omega, \omega_p, << 1/\tau_{oa}$$

$$1/(\omega_p Q_p) = \tau_1 + K\tau_2$$

$$1/\omega_p^2 = \tau_3^2 - K\tau_2\tau_{oa}$$

Notice that:

- There are no new powers of s in the transfer function
- Changing the resistor and capacitor values can compensate for τ_{oa}
- The approximation is reasonably accurate when $f << f_{3dB}$

To pre-distort this filter:

1. Design the filter assuming K constant ($\tau_{oa} = 0$).
2. Recalculate the resistors and capacitors using the pre-distorted values of ω_p and Q_p ($\omega_{p(pd)}$ and $Q_{p(pd)}$ that will compensate for τ_{oa}:

$$1/\omega_{p(pd)}^2 = 1/\omega_{p(nom)}^2 + K\tau_2\tau_{oa}$$
$$= \tau_3^2$$

$$1/(\omega_{p(pd)}Q_{p(pd)}) = 1/(\omega_{p(nom)}Q_{p(nom)})$$
$$= \tau_1 + K\tau_2$$

where $\omega_{p(nom)}$ and $Q_{p(nom)}$ are the nominal values of ω_p and Q_p

3. Repeat step 2 until $\omega_p \approx \omega_{p(nom)}$ and $Q_p \approx Q_{p(nom)}$, where:

$$1/\omega_p^2 = 1/\omega_{p(pd)}^2 - K\tau_2\tau_{oa}$$

$$1/(\omega_p Q_p) = 1/(\omega_{p(pd)}Q_{p(pd)})$$

Example 4:

Biquad section, s^2 term in the denominator multiplied by K:

$$\frac{V_o}{V_{in}} \approx \frac{1}{1 + (1/(\omega_p Q_p))s + (1/\omega_p^2)s^2}$$

$$1/(\omega_p Q_p) = \tau_1$$

$$1/\omega_p^2 = K\tau_2^2$$

where τ_1 and τ_2 are time constants set by resistors and capacitors.

To include the op amp's group delay, substitute for K and simplify:

$$\frac{V_o}{V_{in}} \approx \frac{1}{1 + (\tau_1)s + (\tau_2^2 \bullet K/(1 + \tau_{oa}s))s^2}$$

$$\approx \frac{e^{\tau_{oa}s}}{1 + (1/\omega_p Q_p))s + (1/\omega_p^2)s^2}$$

$$\omega, \omega_p << 1/\tau_{oa}$$

$$1/(\omega_p Q_p) = \tau_1 + \tau_{oa}$$

$$1/\omega_p^2 = K\tau_2^2 + \tau_1\tau_{oa}$$

Notice that:

- The $(1 + \tau_{oa}s)$ factor in the numerator was converted to the exponential form, which represents a constant group delay
- There are no new powers of s in the transfer function
- Changing the resistor and capacitor values can compensate for τ_{oa}
- The approximation is reasonably accurate when $f << f_{3dB}$

To pre-distort this filter:

1. Design the filter assuming K constant ($\tau_{oa} = 0$).

Appendix A – Transfer Function Examples (Continued)

2. Recalculate the resistors and capacitors using the pre-distorted values of ω_p and Q_p ($\omega_{p(pd)}$ and $Q_{p(pd)}$) that will compensate for τ_{oa}:

$$1/\omega^2_{p(pd)} = 1/\omega^2_{p(nom)} - \tau_1\tau_{oa}$$
$$= K\tau_2^2$$
$$1/(\omega_{p(pd)} Q_{p(pd)}) = 1/(\omega_{p(nom)} Q_{p(nom)}) - \tau_{oa}$$
$$= \tau_1$$

where $\omega_{p(nom)}$ and $Q_{p(nom)}$ are the nominal values of ω_p and Q_p

3. Repeat step 2 until $\omega_p \approx \omega_{p(nom)}$ and $Q_p \approx Q_{p(nom)}$, where:

$$1/\omega_p^2 = 1/\omega^2_{p(pd)} + \tau_1\tau_{oa}$$
$$1/(\omega_p Q_p) = 1/(\omega_{p(pd)} Q_{p(pd)}) + \tau_{oa}$$

Appendix B – Electrical Loop Delay

τ_{eld} can be calculated as:

$$\tau_{eld} = x \bullet \sqrt{\varepsilon_r \mu_r}/c + \tau_{oa}$$

where:

- x is the distance around the filter feedback loop, excluding the op amp
- ε_r is the equivalent relative permittivity of the PCB trace
- μ_r is the equivalent relative permeability of the PCB trace
- **c** is the speed of light in free space (3.00×10^8 m/s)
- τ_{oa} is the op amp group delay at f_c

For a typical printed circuit board, $\sqrt{\varepsilon_r \mu_r} \approx 20$. This gives:

$$\tau_{eld} \approx x \cdot (0.067\text{ns/cm}) + \tau_{oa}$$

where x is in centimeters, and τ_{oa} is in nanoseconds.

Appendix C – Bibliography

[1] R. Schaumann, M. Ghausi and K. Laker, *Design of Analog Filters: Passive, Active RC, and Switched Capacitor.* New Jersey: Prentice Hall, 1990.

[2] A. Zverev, *Handbook of FILTER SYNTHESIS.* John Wiley & Sons, 1967

[3] A. Williams and F. Taylor, *Electronic Filter Design Handbook.* McGraw Hill, 1995.

[4] S. Natarajan, *Theory and Design of Linear Active Networks.* Macmillan, 1987

[5] M Steffes, "Simplified Component Value Pre-distortion for High Speed Active Filters," Comlinear Application Note, QA-21, Rev. A, March 1993 (no longer available).

[6] K Blake, "Low-Sensitivity, Lowpass Filter Design," *Comlinear Application Note*, OA-27, July 1996.

Note: The circuits included in this application note have been tested with National Semiconductor parts that may have been obsoleted and/or replaced with newer products. Please refer to the CLC to LMH conversion table to find the appropriate replacement part for the obsolete device.

Pushing Low Quiescent Power Op Amps to Greater than 55dBM 2-Tone Intercept

National Semiconductor
OA-22

Abstract

It is commonly expected that very low distortion amplifiers must dissipate considerable quiescent power to achieve their high linearity. With the advent of intrinsically low distortion current feedback op amps, along with the linearity improvements achieved by the negative feedback used in these devices, wideband low distortion amplifiers have become available at much lower quiescent power levels. This discussion will focus on the 2-tone, 3rd order intermodulation distortion of current feedback amplifiers. Following a brief review the harmonic distortion mechanisms of current feedback op amps, a simple means to further improve an already high intercept will be described. Having pushed the 3rd order spurious levels into the noise, an automated means of measuring these very low distortion levels will be described.

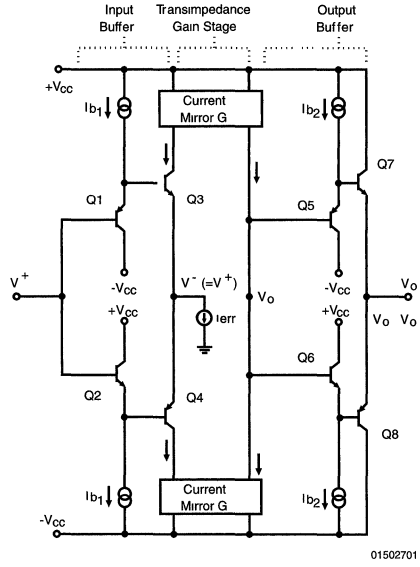


FIGURE 1. Simplified Current Feedback Topology

Harmonic Distortion in a Current Feedback Amplifier

Figure 1 shows a simplified internal circuit for a current feedback operational amplifier. Note that the structure is very symmetric with complementary NPN and PNP devices. The input buffer stage, Q1-Q4, forms an open loop voltage buffer from the non-inverting input to the inverting pin. Transistors Q3 and Q4 provide a means to simultaneously drive the inverting node voltage and cascode an error current signal through their collectors to a current mirror stage. The outputs of the two symmetric current mirror stages are fed back together to form the high transimpedance node for the amplifier. This is the high gain node for the amplifier. Small changes in the error current (fed back through Q3 and Q4) will have a significant transimpedance gain to a voltage at the outputs of the two current mirrors. This voltage (V_o') is buffered to the output pin by another open loop voltage buffer, transistors Q5-Q8. This buffer's high input impedance contributes to achieving a high forward transimpedance gain through the amplifier while providing a low impedance output drive. Both the input buffer and the output buffer are essentially Class AB buffer stages *(see ref. 1 for a more complete description of a current feedback op amp).*

To this point, the amplifier's internal elements have been treated from an open loop standpoint. When the output is connected back to the inverting input through a feedback resistor, with a gain setting resistor to ground on the inverting node, we get the closed loop op amp configuration. *Figure 2* shows the closed loop current feedback op amp block diagram along with the resulting transfer function.

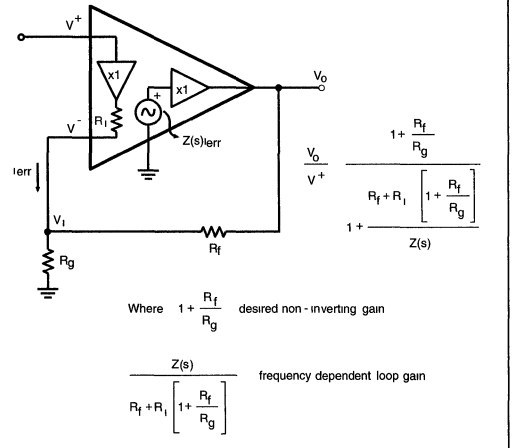


FIGURE 2. Closed-Loop Transfer Function

Looking at the transfer function, the numerator expression is our desired signal gain in Volts/Volts. While the denominator expression represents the error terms due to a finite forward gain in the amplifier. If the forward transimpedance gain, Z(s), were infinite, this error term would drop out and the amplifier would produce exactly the gain shown in the numerator. The forward transimpedance is, however, a frequency dependent gain, having a very large value at DC with a dominant low frequency pole along with higher frequency poles (see National op-amp data sheets for open loop transimpedance plots). When the magnitude of Z(s) has rolled off to equal the value of the feedback transimpedance ($R_f + R_i * (1 + R_f / R_g)$), the loop gain has dropped to one and the

Harmonic Distortion in a Current Feedback Amplifier (Continued)

overall amplifier frequency response begins to roll off. The R_t * (1+ R_f /R_g) part of the feedback transimpedance is the principal parasitic effect limiting the amplifier's bandwidth as higher closed loop (1+ R_f /R_g) gains are desired (R_t is the output impedance of the buffer driving out of the inverting node). For the remainder of this discussion this R_t term will be set to zero leaving the feedback transimpedance set by only R_f.

One of the basic advantages offered by the current feedback topology is that, with the loop gain, and hence the frequency response, set externally by R_f , the desired signal gain may be set by R_g with minimal impact on the frequency response. It is through this mechanism that the current feedback op amp is said to offer a Gain-Bandwidth product "independence". Please see National application note OA-14 for a more complete discussion of the current feedback transfer function and frequency response control.

Distortion Mechanism's in Current Feedback Amplifiers

From an open loop standpoint, harmonic distortion arises from any non-linearities in going from the inverting error current signal to the output voltage. Although we have shown this transimpedance gain to be a frequency dependent linear gain, Z(s), at any particular frequency, Z can actually be represented by a polynomial expression from the error current to the output voltage. This polynomial will have a very high linear gain term (at low frequencies) with relatively small coefficients for the higher order terms.

The signal path from the inverting input to the output follows two symmetric paths as shown in *Figure 1*. The open loop 2nd order coefficient is set by any transfer mismatches between the upper and lower signal paths to the output. The open loop 3rd order coefficient is principally set by the 3rd order curvature (crossover distortion) in the transfer function of the Class AB output buffer. (See reference 2, page 694 for a discussion of Class AB buffer distortion).

With the 2nd order distortion arising from mismatch effects, it is often observed that this distortion is strongly dependent on the DC operating point at the output. Changing the relative voltages across the two halves of the forward gain path will effect the balance of the parasitic effects (voltage dependent base-collector capacitance and output impedances) that give rise to this non-linearity. Similarly, for a ground centered, sinusoidal, output swing, inbalancing the power supplies can be used to null the 2nd harmonic at a specific frequency.

The magnitude of the open loop 3rd harmonic distortion term, at a given frequency, is principally a function of the output load current vs. the biasing current, I_{b2} , in the output stage. Hence, as signal swings go up, load resistors go down, or quiescent biasing current goes down, this third order distortion will increase. Conversely, as the load impedance increases, the signal swing decreases, or the quiescent biasing current increases, this 3rd order distortion will be decreased.

The intrinsic symmetry of the forward gain path, with well matched PNP and NPN signal paths, along with the fully complementary Class AB output buffer, yields low open loop distortion. This distortion is further reduced by the action of the negative feedback when the loop is closed (as shown in *Figure 2*). At a particular frequency, Z(s) can be taken to have specific values for the coefficients of a polynomial approximation to the transimpedance gain from the inverting error current to the output voltage. *Figure 3* steps through a transfer function development using a polynomial expression for the forward transimpedance gain. Although this approach does not yield a closed form solution for the output voltage polynomial vs. an input signal, it does illustrate the loop gain dependence of the higher order terms.

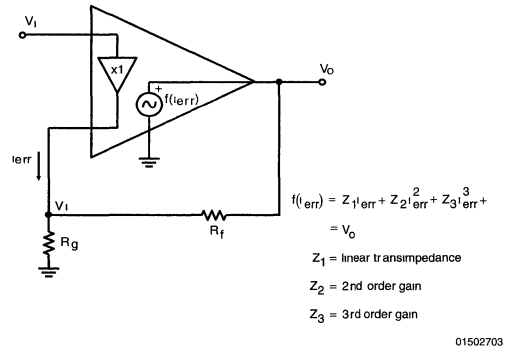


FIGURE 3. Loop Gain Effect on Non-Linearity

Summing currents at the inverting node

$$\left[\frac{V_I}{R_g} = i_{err} + \frac{V_o - V_I}{R_f}\right] R_f \quad \text{, multiplying through by } R_f \text{ and grouping terms}$$

$$V_I\left[1 + \frac{R_f}{R_g}\right] + R_f I_{err} + V_o$$

From the above expression for V_O (using the first three terms)

$$i_{err} = \frac{V_o}{Z_1} \quad \frac{Z_2}{Z_1} i_{err}^2 \quad \frac{Z_3}{Z_1} i_{err}^3$$

Should isolate and solve for i_{err} polynomial here, but this doesn't yield a very clear result. Simply putting this i_{err} expression into the above expression

$$V_I\left[1 + \frac{R_f}{R_g}\right] = V_o\left[1 + \frac{R_f}{Z_1}\right] - R_f \frac{Z_2}{Z_1} i_{err}^2 - R_f \frac{Z_3}{Z_1} i_{err}^3$$

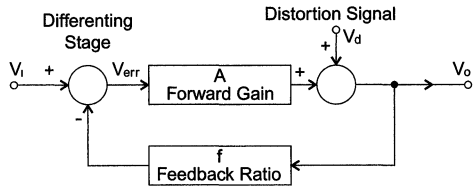
Then, solving for V_O

$$V_o = V_I \frac{1 + \frac{R_f}{R_g}}{1 + \frac{R_f}{Z_1}} + \frac{Z_2}{Z_1 / R_f} i_{err}^2 + \frac{Z_3}{Z_1 / R_f} i_{err}^3 \quad \text{where } \frac{Z_1}{R_f} = \text{Loop gain}$$

A more common way to show the effect of negative feedback on forward gain distortion effects is to introduce an error signal at the output of the forward gain block. *Figure 4* shows this control theory approach with a similar result to *Figure 3* - open loop distortion effects are reduced by the loop gain in

Distortion Mechanism's in Current Feedback Amplifiers (Continued)

a negative feedback closed loop configuration. This approach also does not reach a closed form solution for V_o, (V_d should actually depend on V_i).



$$V_o = A * V_{err} + V_d$$

$$V_{err} = V_i - f * V_o$$

$$V_o = A * V_i - A * f * V_o + V_d$$

$$(1 + A * f) * V_o = A * V_i + V_d$$

$$V_o = A * \frac{V_i}{1 + A * f} + \frac{V_d}{1 + A * f}$$

$$A * f \equiv \text{Loop Gain}$$

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FIGURE 4. Control Theory Model of Distortion

For a single frequency input, it is the loop gain at the fundamental frequency that is applicable to determining the loop gain's impact on the distortion. Some of the literature seems to imply that it is the loop gain at the harmonics that is acting to linearize the closed loop performance to decrease the distortion (reference 2, page 418). However, testing with a loop gain tailored to be higher at the fundamental than at the harmonics has shown a direct dependence on the loop gain at the fundamental, but not at the harmonics.

For the 3rd order terms, the achievable harmonic and 2-tone, intermod, distortion levels are set by the intrinsic 3rd order distortion of the output buffer and the loop gain at the fundamental frequency of operation. *Figure 5* shows a Bode plot of the frequency dependent forward transimpedance, 20*log(|Z(s)|), for a typical current feedback amplifier. The solid horizontal line intersecting this plot at about 100MHz is 20*log(R_f), the feedback transimpedance. The vertical distance between the forward Z(s) and this solid horizontal line is the loop gain, $|Z(s)|/R_f$.

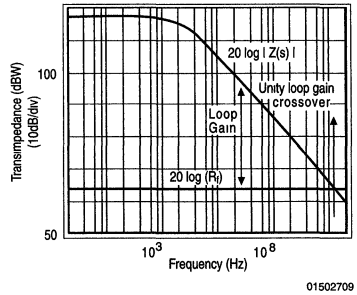

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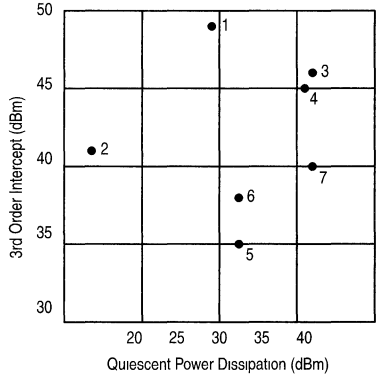
FIGURE 5. Forward and Feedback Transimpedance

As is apparent from *Figure 5*, this loop gain decreases with increasing frequency as the forward transimpedance gain rolls off. The intersection of Z(s) and the feedback transimpedance is of critical importance in determining the closed loop frequency response flatness. This decreasing loop gain with frequency is the dominant cause for an increase in

Distortion Mechanism's in Current Feedback Amplifiers (Continued)

harmonic distortion with increasing frequency for negative feedback amplifiers. One of the key contributions of the current feedback amplifier is the ability to use higher loop gains to higher frequencies than for equivalent voltage feedback parts Typically, however, we still see the 3rd order distortion terms starting to increase, for a given output power level and gain, for frequencies above 5MHz. Conversely, as operating frequencies go below about 5MHz, the distortion performance typically reaches a minimum value in the region of the dominant open loop pole.

As a point of comparison, this discussion will focus on the 2-tone 3rd order intermodulation distortion at 10MHz. *Figure 6* shows a plot of 3rd order intercept (at 10MHz) vs. quiescent power dissipation (in dBm) for two current feedback amplifiers along with several other high linearity amplifiers. Many of these other amplifiers use a Class A output which requires significantly higher quiescent power to achieve low distortion. Also, minimal feedback, and hence minimal distortion improvement due to loop gain, is generally used in these other parts. This yields a distortion performance that is not nearly as frequency dependent Basically, these Class A output amplifiers have driven the forward path non-linearities down with high quiescent currents and used minimal feedback to keep their distortion performance constant over a wider frequency range.



1.	National	CLC221
2	National	CLC401
3	Advancd Millwave Lab	ARO1003252
4.	Adams Russell	AM-109
5.	Avantek	UTO-509
6.	Watkins Johnson	WJ-A59
7.	Q-Bit	QB-210

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FIGURE 6. 2-tone, 3rd Order Intercept vs. Quiescent Power (dBm)

The data of *Figure 6* shows that, for HF frequencies, considerably higher intercepts per mW of quiescent dissipation can be achieved with current feedback op amps through the use of a very linear forward gain path and high loop gain in the feedback network. The principal drawbacks to using the current feedback op amp in an HF or RF application is a steadily decreasing intercept above 5MHz, usable bandwidths limited to about 100MHz, and relatively poor noise performance. Intercepts have typically dropped to below 30dBm by 50MHz for the National op amps shown in *Figure 6* (note 1)

Improving Distortion by Shaping the Loop Gain

Since a current feedback amplifier allows the loop gain to be set separately from the signal gain, it should be possible to adjust the loop gain to yield an improved distortion performance without changing the signal gain. The simplest way to do this would be to scale the resistor values down, keeping the same ratio for R_f /R_g. Decreasing R_f will increase the loop gain over the full frequency range, but runs the risk of inadequate phase margin at the crossover, where $|Z(s)| = R_f$. It would be preferable to decrease the feedback transimpedance at lower frequencies but return to the nominal design value for R_f where this feedback R is intended to equal Z(s).

Figure 7 shows one possible circuit that achieves this loop gain shaping. This circuit was originally reported in the literature as a means to improve the equivalent input noise (reference 3). At low closed loop gain settings, the relatively large inverting input current noise for a current feedback amplifier can dominate the overall noise performance. This noise current shows up at the output pin multiplied by the feedback resistor. The circuit of *Figure 7* reduces the feedback resistor by using a parallel combination of the two feedback resistors as the low frequency gain for this noise current. The coupling inductor is set to remove this parallel

Improving Distortion by Shaping the Loop Gain (Continued)

feedback path for the unity loop gain crossover frequency (where Z(s) = R_{f1}) with approximately 60 degree phase margin.

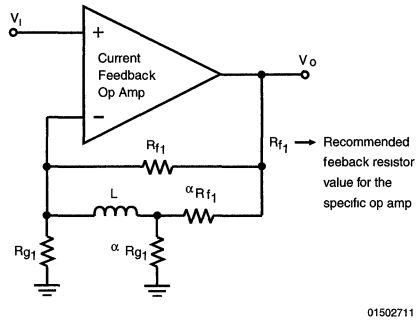

FIGURE 7. Loop Gain Shaping Network

Figure 8 shows a generalized transfer function for the circuit of *Figure 7*. In general, this circuit could be used to shape both the loop gain and the forward signal gain. At low frequencies, the gain is set by the parallel combination of the two R_f's divided by the parallel combination of the two R_g's. At high frequencies, once the inductor has opened up the connection between the two feedback's, the gain is simply (1 + R_{f1}/R_{g1}). Similarly, the feedback transimpedance at low frequencies is the parallel combination of the two feedback R's while at high frequencies it has increased to equal R_{f1}. In going from low to high frequencies, this circuit shows a zero/pole pair for both the signal gain and the feedback transimpedance.

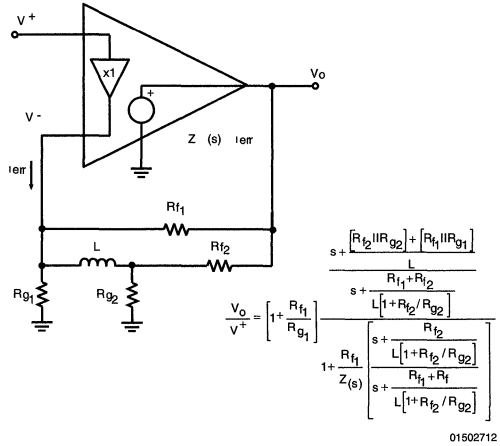

FIGURE 8. Transfer Function for Parallel and Inductor Coupled Feedback

For this loop gain shaping application, we will take the ratio of $R_{f1}/R_{g1} = R_{f2}/R_{g2}$. Under this condition, the numerator of the transfer function in *Figure 8* simplifies to equal 1+ R_{f1}/R_{g1} indicating a flat frequency response up to the roll-off frequency. The principle concern here is the frequency dependence of the feedback transimpedance. The loop gain has been increased due to the decreased feedback transimpedance at low frequencies which should provide an improved harmonic distortion performance. The feedback transimpedance now shows a zero/pole pair due to the inductor coupling the two feedback paths together. *Figure 9* shows an analysis of the loop gain for this parallel, inductor coupled, feedback to set the pole and zero frequencies.

With $1+\frac{R_{f_1}}{R_{g_1}} = 1+\frac{R_{f_2}}{R_{g_2}} = A_v$,

Let $R_{f_2} = \alpha R_{f_1}$; Normally $\alpha \leq 1$

Rewriting the Loop Gain in terms of α and A_v

Loop gain $\frac{Z(s)}{R_{f_1}\frac{s+\frac{R_{f_1}\alpha}{L A_v}}{s+\frac{R_{f_1}(1+\alpha)}{L A_v}}}$ $\frac{\text{forward transimpedance}}{\text{feedback transimpedance}}$

At high frequencies, the feedback transimpedance = R_{f_1}.

Define the ratio of this high frequency feedback transimpedance to the DC feedback transimpedance as $\beta = \frac{R_{f_1}}{R_{f_1}\|R_{f_2}} = 1+\frac{R_{f_1}}{R_{f_2}}$.

20 log (β) is then the increase in low frequency loop gain in dB from the high frequency value of R_{f_1}.

The resulting feedback transimpedance $\frac{\text{zero}}{\text{pole}}$ ratio $= \frac{\alpha}{\alpha+1} = \frac{1}{\beta}$

Typically we would target the pole frequency to occur at a lower frequency than the nominal crossover frequency for R_{f_1} (recommended value for amplifier)

Then $L = \frac{R_{f_1}\alpha}{\text{Pole frequency} * A_v}$

This will set the zero frequency to $\frac{\text{pole frequency}}{\beta}$

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FIGURE 9. Loop Gain Analysis for Parallel and Inductor Coupled Feedback

To use this approach to increasing the low frequency loop gain the following steps would be followed:

1. The desired signal gain would be set.
2. A current feedback amplifier appropriate for this gain range would be selected.
3. R_{f1} is set to the selected op amp's nominal recommended value (note 2).

Improving Distortion by Shaping the Loop Gain (Continued)

4. The pole frequency for the feedback transimpedance is set to be less than nominal unity loop gain crossover frequency for the selected op amp.
5. The desired reduction in feedback transimpedance at low frequencies is set. This will also determine the zero frequency.

The pole/zero ratio is equal to $\beta \left(=1+\frac{R_{f_1}}{R_{f_2}}\right)$

6 The coupling inductor (L) is solved from the equation in *Figure 9*.

7. R_{f2} and R_{g2} are solved using _ and the desired signal gain.
8. The additional loading on the output due to the additional feedback network (R_{f2} + R_{g2}) should be checked to see that it is not significantly lowering the intended load.

Figure 10 shows a Bode plot of the same forward transimpedance gain of *Figure 6* with a 4·1 reduction in the DC feedback transimpedance using this paralleled, inductor coupled, feedback. Note that the targeted pole frequency was 80MHz which forces the zero frequency to be at 20MHz. This yields a 12dB (4 times) increase in the low frequency loop gain. This loop gain has decreased by 3dB at 20MHz and continues on up to only a 3dB improvement from the nominal R_{f1} value at 80MHz. The goal here was to be approximately back to an R_{f1} feedback impedance by the 100MHz unity loop gain crossover point on the forward transimpedance curve. This 12dB improvement in the loop gain at 10MHz should translate directly into a 6dB increase in the 2-tone, 3rd order intermodulation intercept (one half of a 12dB decrease in the spurious levels for a given output power level will yield a 6dB increase in intercept).

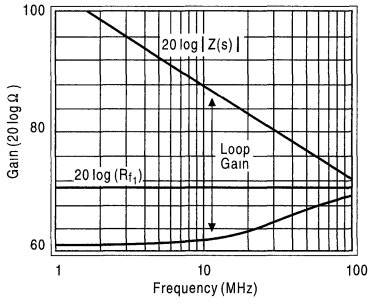


FIGURE 10. Forward Transimpedance with Shaped Feedback Showing Increased Loop Gain

Figure 11 shows an example circuit using the paralleled feedback approach to increasing the loop gain at low frequencies. This circuit also uses a 1:4 step up transformer at the input to improve the Noise Figure (reference 4). This input stage presents a 50Ω input impedance in the passband of the transformer and reduces the overall Noise Figure to 7.2dB for this test circuit. Although this transformer will AC couple the signal path, it is important to remember that the amplifier itself is a true DC coupled device. Since the input is already AC coupled, a 1µF blocking capacitor at the output has been added to strip off any amplifier DC offsets that may be present. The op amp itself presents a very low output impedance. To get into a 50Ω system, a series, discrete, 50Ω resistor must be added The defined measurement point for both gain and intercept is at the 50Ω load.

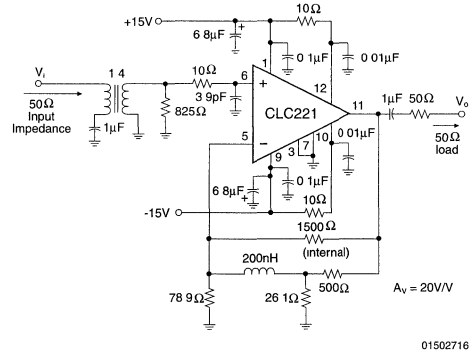


FIGURE 11. Test Circuit for Increasing Loop Gain

The overall gain for this circuit is 40V/V (32dB). *Figure 12* shows the measured frequency response for this test circuit. Although the CLC221 is specified to provide >165MHz -3dB bandwidth in the gain of +20 configuration used here, the transformer and the input RC filter limit the bandwidth to approximately 90MHz. Significant latitude in trading off gain, bandwidth, and noise are possible when using op amps in these types of applications. Please see National application note OA-11 for additional discussion of interpreting and using op amp specifications in RF applications.

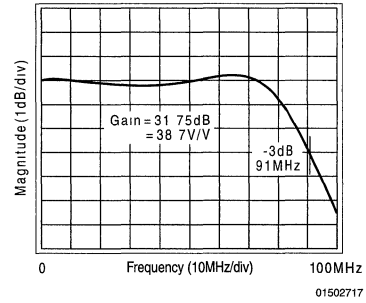


FIGURE 12. Measured Frequency Response for Wide Dynamic Range Test Circuit Using a CLC221

At 10MHz, the CLC221, without any loop gain shaping, has a 49dBm 3rd order intercept while dissipating only 900mW quiescent power. Using ±15 volt supplies, the full scale output pin voltage swing is approximately ±5 volts in order to satisfy the 50mA maximum output current into the 100Ω load. For 2-tone, 3rd order intercept testing, this translates into a maximum 12dBm test power level for each of the two

Improving Distortion by Shaping the Loop Gain (Continued)

test frequencies at the 50Ω load. Given a maximum peak to peak swing at the amplifier output, from either a voltage swing or current limit standpoint, the maximum single tone power level at the load is for a voltage swing 1/4 this level. This accounts for the 6dB loss in going through the matching network and the fact that the full voltage envelope for a two tone test is the sum of the peak to peak swings for the individual test frequencies.

Pushing a full 12dBm in each test tone at the load puts the amplifier into a slightly higher distortion mode. The 49dBm intercept for the amplifier by itself is not observed until the single tone power at the load has dropped to 8dBm. Using this as a test condition will yield a $3V_{pp}$ swing for the voltage envelope at the load.

This test circuit shows bipolar supplies for the amplifier. True DC coupled devices typically use balanced bipolar supplies. However, since most current feedback amplifiers don't actually use a ground reference in their design, single supply operation is perfectly acceptable. National application note OA-11 describes this in detail.

Measuring 2-Tone, 3rd Order Intercepts above 50dBm

The 3rd order spurious levels for 8dBm test power levels and 50dBm intercept would be −74dBm (note 3). This 82dB dynamic range requirement is right at the edge of what most spectrum analyzers can measure. *Figure 13* shows a typical test setup for measuring intercepts where the dynamic range requirement is less than 90dB. One of the principle requirements for this measurement are to provide clean input test tones, with no intermodulation of the sources. The amplifiers following the sources and the hybrid power combiner achieve this quite well. These amplifiers, the CLC142, can provide 27dBm output power through 100MHz and are particularly useful in getting enough power to the DUT for testing low gain devices. They also isolate any leveling loops in the output stage of the sources from mixing together and can themselves provide in excess of 50dBm intercepts through 10MHz (although their intercept performance does not limit this test).

The 2nd primary requirement for the test setup of *Figure 13* is to attenuate the fundamental power levels at the input of the spectrum analyzer mixer to a low enough power level to eliminate any analyzer produced inter-modulation products. This typically translates into a −36 to −40dBm power level at the mixer.

The test set up of *Figure 13* would begin to have trouble making this measurement as the required dynamic range extends beyond 85dB. This would occur as the test power level is decreased (to evaluate if intercept performance is observed) or if higher intercepts were to be measured. The anticipated 55dBm intercept for the test circuit described earlier would exceed the measurement range for the test configuration of *Figure 13*. With 8dBm test power levels at the load, the anticipated spurious power levels would be at −86dBm for a 55dBm intercept. This 94dB dynamic range is probably beyond most spectrum analyzers. Averaging could be used to lower the noise floor in an attempt to pull this very low spurious out of the noise. As the test power is decreased, the required averaging would significantly extend the test time. An alternative technique would be to filter out one or both of the two test frequencies after the DUT and before the signal is applied to the analyzer. This realistically requires a relatively broad spacing of the test input frequencies (to avoid filtering the spurious frequencies) and is not particularly useful for swept frequency measurements.

Figure 14 shows a modification to the basic test setup of *Figure 13* to extend the dynamic range of this intermodulation measurement system. In this approach a 3rd signal source, phase locked to one of the other two input signal sources, is used to null out one test frequency at the output of the DUT. The same type of power combiner used at the input is used here to combine the output signal with a nulling signal from a 3rd signal generator. The Fluke 6080A sources offer a programmable phase capability that allows the nulling source to be tuned to very nearly 180 degrees out of phase with one of the test signals at the DUT output. The output of this 2nd power combiner will then have one of the test frequencies plus the original intermodulation tones at the output of the DUT. This allows the system to use less attenuation to the analyzer mixer since no intermodulation terms will be generated in the analyzer. This technique also offers the advantage of being fully programmable over a wide range of frequencies and test powers.

Low Frequency (100KHz to 10MHz) 3rd Order Intermodulation Intercept Test Setup Template

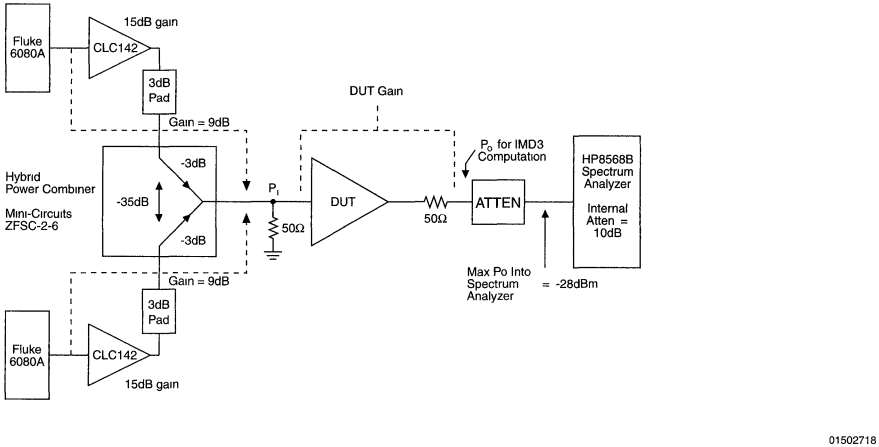


FIGURE 13. Intermod Test Setup

Measuring 2-Tone, 3rd Order Intercepts above 50dBm (Continued)

Low Frequency (100KHz to 10MHz) 3rd Order Intermodulation Intercept Test Setup Template with Output Single Tone Cancellation

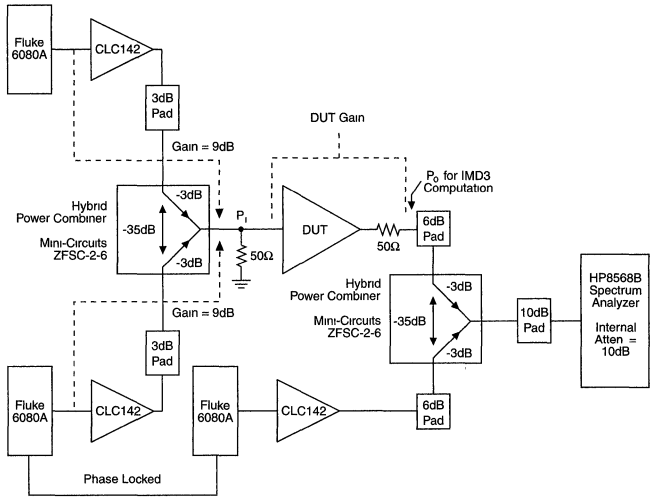


FIGURE 14. Improved Dynamic Range Intermod Test Setup

Test Results for the Improved Intercept Amplifier

The intermodulation intercept for the circuit of *Figure 11* was first measured using the basic setup of *Figure 13*. This measurement resulted in approximately a 52dBm intercept. *Figure 15* shows the test signals at 100kHz around 10MHz. Note that the measured power is –27dBm or –37dBm at the mixer considering the analyzer's internal 10dB attenuator.

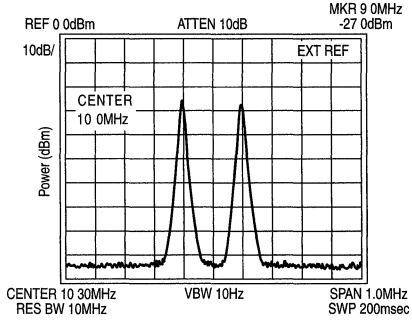


FIGURE 15. Test Power Levels for 10MHz Test

Figure 16 shows the measurement for the upper spurious signal at 10.3MHz. Note the very narrow resolution bandwidth, video bandwidth, and span to make this measurement. The low phase noise of the sources and phase locking all of the sources and the analyzer together are critical to this measurement.

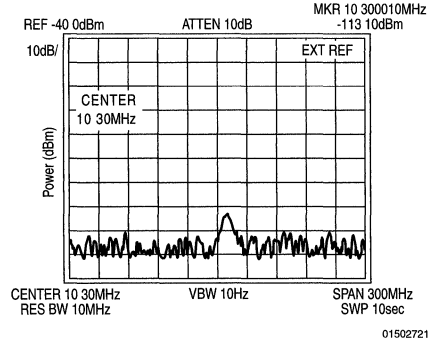


FIGURE 16. Spurious Measurement at 10.3MHz

Continuing on to the same measurement with the test set up of *Figure 14* did allow a slightly increased measurement range. After nulling out the lower test frequency, the test signal plot of *Figure 17* shows the widely disparate power levels going into the analyzer. It is important to remember that equal test power levels are still being generated at the DUT output. Note that the measured power on the uncancelled test tone has increased to approximately –11dBm from the earlier –27dBm level. This reflects the reduced

Test Results for the Improved Intercept Amplifier (Continued)

(19dB) attenuation used at the output signal path. Also note that the lower test tone has been attenuated by 40dB from the upper tone with this cancelling technique. Although the mixer is seeing a fairly high absolute power level for the upper tone, −21dBm, since the lower tone is significantly lower, no analyzer generated intermodulation terms should interfere with this measurement.

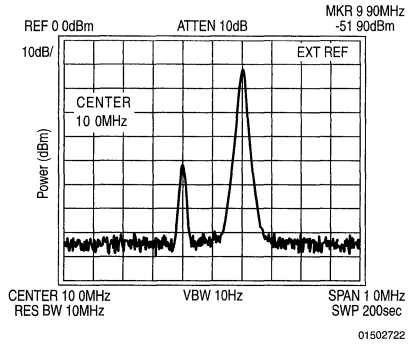


FIGURE 17. Test Power Levels at the Analyzer with Single-Tone Cancellation

Figure 18 shows the measured lower spurious at 9.7MHz using the test setup of *Figure 14*. This measured spurious level is about 8dB more out of the noise than the earlier measurement. However, the noise floor has clearly come up along with this reduced attenuation from the DUT output to the analyzer input. This indicates that the DUT output noise is a significant part of the total noise at the analyzer. Taking the measured test tone power to be at −11dBm, while the DUT output power at the load was 8dBm, this yields a (−11-(−98.5)) / 2 +8 = 51.75dBm intercept.

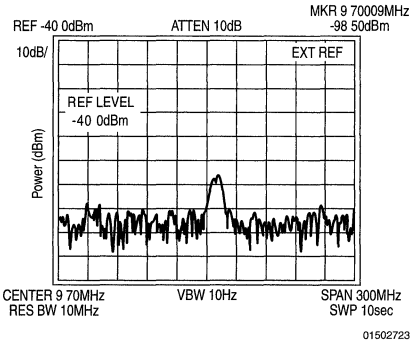


FIGURE 18. Spurious Measurement with Single Test Tone Cancellation

The loop gain shaping network of *Figure 11* appears to have improved the intercept by only 3dBm instead of the 6dBm expected. Further investigation revealed that this can be attributed to the non-zero inverting input impedance of the current feedback amplifier. With this impedance >0, some of the feedback error signal splits off and is wasted through the gain setting resistors. This reduces the loop gain. Simulations including this effect revealed only a 6dB improvement in loop gain at 10MHz which is consistent with the 3dBm increase in intermodulation intercept.

However, the intercept does continue to improve as the test frequency is decreased. The following tables shows the measured intercepts from 5MHz to 10MHz for the circuit of *Figure 11* using the test setup of *Figure 14*.

Frequency	Intercept
5MHz	55.8dBm
6MHz	54.9dBm
7MHz	54.0dBm
8MHz	52 8dBm
9MHz	52.4dBm
10MHz	51.5dBm

Below 5MHz a 56dBm intercept is achieved.

Conclusions:

High speed current feedback amplifiers can offer exceptional 2-tone 3rd order intercept performance at relatively low quiescent powers. This intercept performance does decrease with frequency due to the decreasing loop gain as frequency is increased. Although the example device used here, the CLC221, is a high performance hybrid amplifier, similar results at lower maximum output power levels can be achieved with monolithic current feedback amplifiers (such as the CLC409, CLC401 and CLC404 particularly). A simple loop gain shaping network can be used to further increase the intercept at low frequencies. And finally, a simple means to extend the measurement dynamic range through output test signal cancellation has been described and demonstrated. This approach offers the principle advantage of being easily programmable over a wide range of frequencies.

References:

1. "Current Feedback Amplifiers", Sergio Franco, reprinted in National 1993 Databook as Application Note AN 2.
2. Integrated Electronics· Analog and Digital Circuits and Systems, Millman & Halkias; McGraw/Hill 1972
3. "T Network Quiets Current-Feedback Op Amps", Howard Bandell; EDN, Aug. 20, 1990 page 152
4. "Improving Amplifier Noise Figure for High 3rd Order Intercept Amplifiers", National Semiconductor Application Note OA-14

Notes:

1. The 49dBm intercept shown for the CLC221 does not agree with the data sheet plot showing 55dBm at 10MHz. The data in *Figure 6* was taking the signal power at a 50Ω load through a series 50Ω output matching resistor. The CLC221 data sheet plot was taking the test power at the output pin which yields a 6dBm higher intercept. More recent data sheets, and all of this discussion, are taking the signal power to be at the matched load.

2. See National Semiconductor Application note OA-13 for a discussion of setting R_f for various signal gains.
3. Equal test powers $P_{spurious}$ = 2 [1.5P_{test} -Intercept] in dBm. At 8dBm test and 49dBm intercept, $P_{spurious}$ = 2 [1.5(8) $-P_{test}$ -49] = −74dBm

Note: The circuits included in this application note have been tested with National Semiconductor parts that may have been obsoleted and/or replaced with newer products. Please refer to the CLC to LMH conversion table to find the appropriate replacement part for the obsolete device.

Measuring and Improving Differential Gain and Differential Phase for Video

National Semiconductor
OA-24
Arne Buck and Jim Riphahn

Differential gain (DG) and differential phase (DP) are two specifications that designers of composite video systems use everyday. We will define them here just to be sure we are all speaking the same language, and to ensure understanding of the rationale of the test technique used by National.

Composite video encodes brightness (luminance), timing (sync), and color (chrominance) into one channel. Luminance is the voltage offset from a reference, or "black", level. Sync appears at a level defined as "blacker than black." Chrominance is encoded as a high-frequency (with respect to the luminance signal) subcarrier. The average value (midpoint) of the chrominance is the luminance. The color has two "dimensions": amplitude which determines the saturation, and phase relative to a reference chrominance burst which encodes the hue. For example, pink has the same relative phase as red, but of a lower amplitude, hence a less saturated red. Red in NTSC is shifted 103.7° from the reference, green 241.3°.

DG and DP are measured at one of two chrominance subcarrier frequencies. NTSC (National Television Systems Committee, 1953) uses a 3.579545MHz color subcarrier. Phase Alternation Line (PAL) alternates the phase of the reference burst with every scan line. The PAL subcarrier frequency is 4.433619MHz.

Differential phase is a change in chrominance (high-frequency) phase with luminance level. This manifests itself in the picture as a color hue shift as the illumination changes. A blue parrot indoors does not become a purple parrot in the sun. Differential gain is a change in chrominance gain with luminance level. The saturation changes in the viewed scene as the brightness varies. A red shirt at noon must not turn pink at night. Both are distortions which, if sufficiently large, can be perceived by the eye.

Another way to think of DG error in a signal channel or amplifier is a magnitude variation of a high-frequency sinusoid (the subcarrier) as its offset changes. This offset can be, at its simplest and crudest, a DC offset. It can also take the form of a low-frequency sinusoid or ramp. Similarly, an alternative way to view DP is as a change in the carrier phase shift of the channel over the range of offset simulating the luminance (see *Figure 1*).

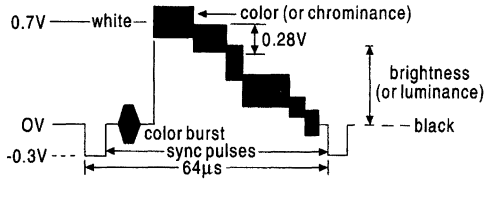


FIGURE 1.

The traditional way of measuring the DG and DP of broadcast video equipment such as a switcher or a distribution amplifier, DA, is with a vectorscope. A distribution amp can have several integrated or discrete amplifiers between the input and output. Vectorscopes can measure such high-level systems to <1% DG and <1°DP. Newer video test equipment based on digital technology, such as the Tektronix ©VM700, can make measurements to <0 03% and <0.03°. This resolution results after the DG and DP errors of the video test signal generator have been calibrated out. This equipment is adequate to measure a complete video system, but cannot measure an individual operational amplifier to the required resolution.

Video designers usually take a worst-case approach when selecting a video op-amp. Consider, for example, the design of a DA with five amplifiers between the input and output. The desired overall system specification for this DA board is to be 0.05% DG and 0.05° DP. One then assumes each of the five op-amps will contribute "+0.01%" and "+0.01°" of DG and DP, respectively. These errors will then add "in phase" for the total of "+0.05." There is not usually a sign associated with DG and DP, rather, the absolute value is used The VM700 measures signed DG and DP for each step in a modulated staircase. The overall DG and DP, however, are displayed as an unsigned peak-to-peak magnitude. Modern video test equipment can measure the final DA but cannot measure the individual op-amps with the required resolution. Imagine, as well, the design of a system with better than 0.05 numbers. If it were possible to select one op-amp with +0.01% DG and another with –0.01%, the two would cancel to zero. Some state-of-the-art video test equipment is built this way.

Another concern, especially with advanced video test equipment, is squeezing the most out of an op-amp

Refer to *Figure 1*, a positive video waveform. The video information is at voltages above 0V (positive video); the sync information is below 0V (negative sync). Video equipment must conform to a standard such as this at the input and output. What happens to the signal in between these external ports is only the designer's business. She may choose to invert the video (negative video, or positive sync) for gamma correction with an inverting summing circuit. Another compelling reason to work with inverted video is that a particular amplifier may have better DG, DP or both, with negative video. The "polarity" of DG and DP may change in a predictable way between negative and positive video. This feature (not a bug) may then be exploited to improve the system DG and DP specifications. It is not easy, using current industry-standard test equipment, to measure negative video DG and DP.

How We Do It

Comlinear uses an HP4195 network analyzer to make DG, DP measurements of its devices and customer circuits There are many good reasons to choose this particular machine. The network analyzer has the gain and phase measuring capability to resolve significantly less than the

How We Do It (Continued)

0.01% and 0.01° target specifications in the device under test, DUT. This particular analyzer has a built-in DC source which can be used as an independent sweep variable; single-frequency, CW, gain and phase can be measured and displayed parametrically on the DC source voltage. This allows the behavior of the amplifier over the entire luminance range, both positive and negative video, to be observed and characterized in detail. A qualitative, as well as quantitative, measurement of DG and DP can be made.

Trends in amplifiers can easily be seen. This is not possible with a box which only delivers numbers. Since network analyzers measure gain in V/V or dB, the trace mathematics of the HP4195 enable conversion to percentages. Finally the internal programming capability of this analyzer yields a self-contained DG and DP measurement system, which does not require an external computer and interface hardware/software yet still can be used for other purposes.

The machine needs a few ancillary items to make this specialized measurement. The CLC400 with ±6V supplies boosts the HP4195's DC sourcing ability. The DC source has limited drive current. The measurement of a unity gain buffer requires twice the input signal level, relative to a DUT with a gain of two, in order to maintain the correct output amplitudes. Operating the CLC400 with ±6V supplies increases the maximum output voltage of the device ±3.5V. The lowpass filter, with the CLC400, guarantees a 50W output impedance over frequency and DC level from the DC source into the power combiner. The power splitter sums the DC swept source (luminance) and AC oscillator (chrominance) passively, so no DG or DP is introduced into the input test signal. The R/T test set is needed for a controlled impedance throughout the test system. Comlinear uses a 50Ω test set for a 50Ω environment. A video designer would most likely have a 75Ω R/T test set at his disposal. In this case the 50Ω resistor on the output of the CLC400 would be 75Ω, the power combiner and filter would be 75Ω, etc.

The DUT, in a 50Ω system, would have a series 100Ω resistor between the DUT output and the 50Ω, 14dB attenuator. Thus the total driven load is the proper 150Ω for a 75Ω environment. With a 75Ω test set, a series resistor of 75Ω and a 14dB 75Ω pad would be used instead. Multiple video loads can be simulated by adding additional 150Ω resistors between the DUT output pin and earth. The AC test signal and the T2 analyzer input are capacitively coupled to isolate the DC from the source oscillator and from the analyzer receiver. The 14dB attenuator ensures that the test signal to be measured is of sufficiently low amplitude so as not to cause overload and distortions in the analyzer front end.

The software is straightforward. Previously, in Application Note OA-08 [Comlinear 1993-1994 data book, pages 11-27], we did a through calibration and subtracted this from the subsequent DUT measurement. This proved unnecessary once the lowpass filter, described above, was added. It is the change in gain and phase being measured here. The absolute gain or phase at any point on the DC sweep is irrelevant. The measurement to be made is S21. The straight amplitude-ratio measurement format is required here, not decibels. Averaging dB and converting to percent is problematic. The mathematics is easy to understand and program if non-dB measurements are made. The AC source is set to CW mode, the frequency to that of the desired color subcarrier for the system requirements. The amplitudes of the DC and AC sources are set.

Once the instrument has been set up, the measurement can begin. A sweep is triggered over the DC source sweep range. It is not necessary to have a large number of measurement points over the sweep. We measure a total of twenty-one points for clarity in the plotted data— 10 negative video, 10 positive video, and one reference black level. For the required resolution a number of measurements are averaged. We have found an average of 30 sweeps to be a good compromise between measurement time and resolution for most op-amps. Some, like the CLC400 and CLC410 with DG, DP ≤0.01, require an average of 50 measurements. There comes a point where further averaging does not enhance resolution.

After the raw data are collected, they are scaled and displayed. The gain data are converted to percentages. The percent gain and the phase data are scaled to fit on the screen. The trace mathematics built into the programming language find the maximum deviation, or peak-to-peak change in gain and phase, over the luminance sweep. Minimum and maximum DG and DP are found along the trace, and can be displayed as does the VM700. The final DG and DP numbers are displayed in addition to the sweep graph. A vectorscope also gives DG and DP as peak-to-peak magnitude. This is in accordance with NTSC standards.

There is one small problem with the programming language in this machine. Oscillator and DC source levels must be hard-coded and cannot be stored as variables for easy experimentation with different circuit gains and attenuations. This isn't too inconvenient, as most op-amps will be tested at a gain of two. The exact hardware chosen will have differing insertion losses which must be taken into account. The AC coupling may necessitate changing the oscillator level slightly between NTSC and PAL subcarrier frequencies. In current practice, engineers use the PAL 4.43MHz frequency, as it is considered to be the more demanding test condition. Also, a piece of equipment is often sold to countries with different broadcast standards. If a product meets the more stringent specification, one size fits all. Often a current feedback amplifier with 200MHz bandwidth at a gain of two displays little difference in DG and DP between the NTSC and PAL frequencies.

The practical upshot of this is that one must determine the appropriate oscillator amplitude and DC sweep range of each individual hardware assemblage empirically, with an oscilloscope. NTSC levels can be found as follows:

- Set the oscillator frequency to 3.58MHz
- To find the necessary DC sweep range, the AC source oscillator amplitude is first manually set to 1mV, as zero is not allowed by the HP4195 software
- Adjust the DC level from the front panel to yield 0.714V at the equivalent 75Ω load, or 1.424V the DUT output
- When the DC sweep range numbers have been found, these are then entered into the program. It is the programmed start- and stop-sweep voltages which are displayed on the HP4195 screen.

How We Do It (Continued)

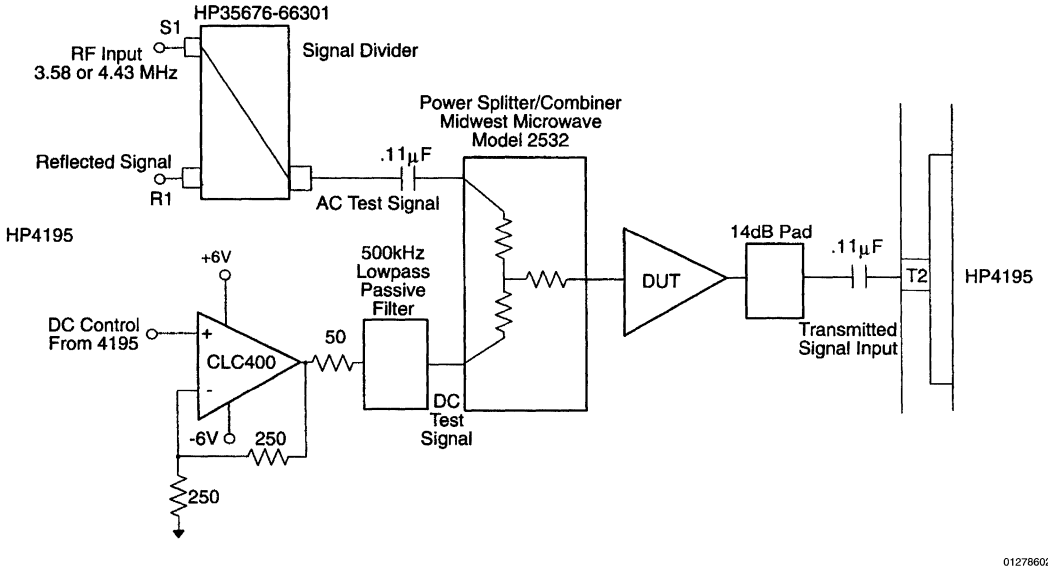


FIGURE 2. R/T Test Set

For example, one of our test setups results in 0.95V at the maximum luminance level. When the HP4195 DC source is set to 0.95V, a DUT at a gain of two has an output of 1.424V. To set the AC oscillator, begin by manually resetting the DC source to 0V. From the front panel, adjust the oscillator amplitude to yield 286mV$_{PP}$ at the equivalent 75Ω load, or 572mV$_{PP}$ at the DUT output. Note the oscillator setting and edit this into the test program (see *Figure 2*).

Look Carefully at How DG, DP are Specified In Datasheets

It is much easier to make measurements than it is to know exactly what you are measuring. — J.W.N. Sullivan, physicist, 1928

Figure 3 shows the measurement results of this test system. A CLC406 is shown. DG and DP are measured for both positive and negative sync (negative and positive video, respectively). The marked points show the specified DG and DP, (peak-to-peak) that is quoted in Comlinear's data sheet. Notice that we would get better numbers if we just took the delta between the endpoints of the sweep range, essentially a DC test at only two luminance levels. This is neither what the video standards delineate, or what vectorscopes or the VM700 report. Another interpretation of these standards implies an RMS value of the error. Neither Comlinear or Tektronix do this.

The VM700 display shows the DP/DG as the largest peak-to-peak delta over the luminance range. Simply giving the endpoint delta between black level and the white level can be misleading. DG and DP do not behave linearly with luminance. The VM700 gives signed DG, DP numbers to each step of the modulated staircase, similar to the HP4195 program. Both pieces of equipment can be used for device characterization and screening for best system performance. The final DG, DP number is the worst-case, peak-to-peak magnitude measured over the entire, continuous, luminance range.

Some manufacturers measure gain and phase at 0V and 0.714V and then tell you the difference. With elan, they call this DG and DP in the data sheet discussion. This would only make sense if the amplifier's DG and DP errors were perfectly linear with respect to luminance. Comlinear has never measured such a device from any manufacturer. When represented graphically, as in *Figure 3*, DG and DP are not represented by a straight line, but appear more like a quadratic or even cubic function.

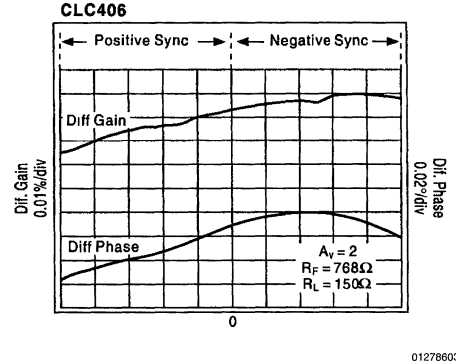


FIGURE 3.

Look Carefully at How DG, DP are Specified In Datasheets (Continued)

Let's take a closer look at the endpoint measurement. If we could change the intercepts or the shape of this "parabola," we could come up with just about any number for DG and DP we wished (see *Figure 3*). If one could change the bias current in a typical complementary emitter follower output stage (*Figure 4*), this can be accomplished.

Even complementary bipolar processes leave something to be desired in PNP and NPN matching. The PNP is better than a lateral PNP, but still worse than the NPN. Beta, for one thing, and Early voltage, for another, are not as good as in the NPN. The PNP is the limitation in the output stage. Many Comlinear amplifiers specify the maximum output voltage and current capabilities based on PNP. Often the device is significantly better than this especially when the output is sourcing current from the NPN. The PNP simply cannot sink an equal magnitude of current without compromising other device performance specifications. Some devices, like the CLC406, specify two output voltage ranges, e.g. +3.1, -2.7 (see *Figure 4*).

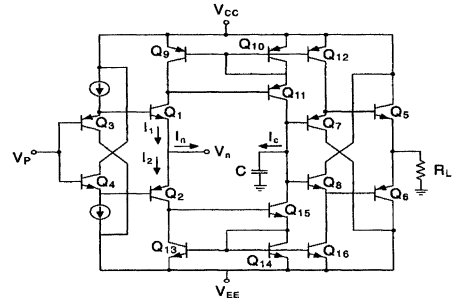


FIGURE 4.

An old trick which can improve the situation (at the expense of burning more circuit power) is to place a "pull-down" resistor on the output. This increases the collector current in the NPN and relieves the burden on the feeble PNP. Notice the effect of this pulldown resistor on DG and DP. Increasing the output stage NPN collector current flattens the DG, DP curves. It is possible to reduce the peak-to-peak DG, DP and force it to zero at the end-points. *Figure 5* shows the CLC430 driving two video loads (total R_L = 75Ω). After adding a pulldown resistor, the DG, DP went from 0.04%, 0.1° to 0.01%, 0.02°.

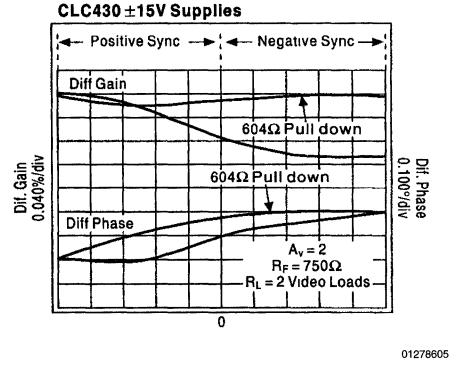


FIGURE 5.

Another test method used in an attempt to measure DG and DP of individual op-amps employs a vectorscope, in spite of its limited resolution. If you assume that five amplifiers in a row each have +0.2 DG and DP, you could theoretically estimate the accumulated error of this chain. We have already seen that amps can be selected to cancel DG, DP errors, so this method is highly suspect (see *Figure 6*).

Careful reading of the data sheets from other manufacturers will reveal anomalous devices' test conditions for DG and DP. A frequent dodge is to specify a 500Ω or even a 1000Ω load. Most video designers need to know DG and DP into a 150Ω load. DG and DP frequently are not the best at a gain of two. The DUT may be "measured" in a gain of three, or another gain where DG/DP are best. Always look for the amplitude of the test signal. It is rarely specified. The proper luminance may be stated in the test conditions, but the chrominance will not (or vice versa). It should come as no surprise that an amplifier will have better DG and DP when delivering 100mV at 3.58MHz into 1kΩ.

If a manufacturer's DG, DP specifications appear to meet the required test conditions for carrier frequency, luminance levels, load and gain, there is still the question of whether the RMS, peak-to-peak or endpoint delta error is measured. This is rarely, if ever, stated. Finally, you may wish to ask for maximum guarantees on DG and DP.

National guarantees DG and DP, others offer only typical (see *Figure 7*).

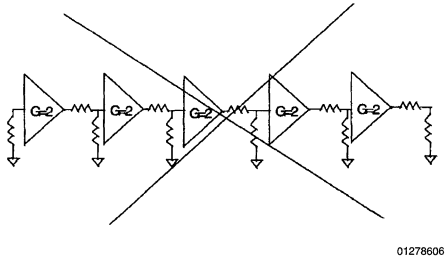


FIGURE 6.

Summary

Please read all data sheets carefully. DG and DP may not be "measured" as you expect. Consider the measurement technique, the test conditions and the guaranteed specifications. Does the data sheet really specify what you need to know?

References

1. *More Random Walks Through Science,* Robert L. Weber, editor, The Institute of Physics, Bristol, England.
2. *Television Measurements,* NTSC Systems, Margaret Craig.
3. *Video Technology Tutorial,* May 1992, Dennis Brunnenmeyer, Cedar Ridge Systems, Cedar Ridge.
4. *Operational Amplifiers, Theory and Practice,* J. K. Roberge.
5. *Solutions* with Speed 1993-1994, Comlinear Corporation.
6. *Raster Graphics Handbook*, Second Edition, Conrac Division, Conrac Corporation.

Video - Differential Gain/Phase Comparison

	1 Load		2 Load		3 Load		4 Load	
Part #	DG	Df	DG	Df	DG	Df	DG	Df
CLC231	.005	.09	.006	.10	.007	.11	.008	.14
CLC400	.025	.01	.025	.015	.025	.015	.025	.015
CLC404	.05	.03	.05	.06	05	.10	.06	.13
CLC406	.03	.02	.03	.025	.04	.03	.04	.03
CLC409	.02	.02	.015	.025	.02	.025	.015	.03
CLC410	.02	.015	.02	.02	.03	.03	.02	.03
CLC411	.02	.05	.05	.10	.06	.19	.08	.26
CLC412	.02	.02	.02	.02	.025	.05	.03	.075
CLC414	.02	.16	.02	.18	.03	.20	.04	.20
CLC415	.02	.07	.02	.08	.02	.09	.02	.10
CLC420	.02	.14	.02	.15	.025	.15	.025	.17
CLC430	.02	.02	.02	.09	.015	.18	.02	.30
CLC431	.1	.1	.2	.2	.35	.35	.45	.45
CLC432	.1	.1	.2	.2	.35	.35	.45	.45
CLC522	.03	.07	.04	.08	.045	.09	.05	.10
CLC532	.05	.01	.11	.08	.19	.15	.34	.24
CLC533	.03	.01	.11	.09	.19	.15	.34	.24

FIGURE 7.

Note: The circuits included in this application note have been tested with National Semiconductor parts that may have been obsoleted and/or replaced with newer products. Please refer to the CLC to LMH conversion table to find the appropriate replacement part for the obsolete device.

Stability Analysis of Current Feedback Amplifiers

National Semiconductor
OA-25
Rea Schmid

Introduction

High frequency current-feedback amplifiers (CFA) are finding a wide acceptance in more complicated applications from dc to high bandwidths. Often the applications involve amplifying signals in simple resistive networks for which the data sheets provide adequate information to complete the task. Too often the CFA application involves amplifying signals that have a complex load or parasitic components at the external nodes that creates stability problems.

This application note covers the discussion of using Bode analysis to determine the gain and phase margin while including external parameters. It discusses how to determine the input buffer gain and its effect on the closed-loop gain. A more appropriate mathematical model is developed for a clearer understanding of the poles and zeros of the CFA amplifier. Finally a summary of how parasitic components influence the frequency and time domain response.

Stability Review

Bode analysis is one of the more useful methods for determining stability for an amplifier. When an engineer selects a unity gain stable voltage-feedback amplifier, the internal compensation of the amplifier is transparent to the end user of the amplifier. If the VFA is connected to a complex load and it alters the phase margin then often the part will oscillate or peak the frequency response. Adding external compensation networks with capacitors and resistors will generally stabilize the amplifier. Of course, this is done at the expense of additional components and cost. With a CFA amplifier, stabilization is accomplished by adjusting the feedback resistor. Thus one component, the feedback resistor, controls the phase and gain margin of the amplifier. The most practical way to determine stability of current-feedback amplifier is by Bode plots generated from computer simulations.

Review of Bode Analysis

Bode analysis is the easiest predictor for determining amplifier stability. The measurement is based upon creating an open-loop magnitude and phase plot to arrive at the closed-loop stability, indicators of gain and phase margin. The phase margin is derived by finding the intersection of the closed-loop unity gain frequency response curve to the open-loop response curve as shown in *Figure 1*. At this frequency the phase is read from the phase plot. This value is subtracted from 180° to arrive at the desired phase margin. Similarly the frequency at 180° is used to determine the gain margin in the magnitude plot shown in *Figure 1*. A recommended phase margin is at least 60° with gain margin of 12 dB.

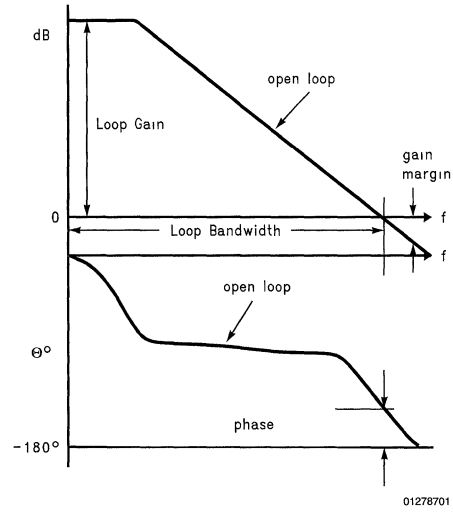


FIGURE 1. Bode Analysis

A Better Model

A practical voltage follower has output resistance which creates a need for a more comprehensive model. That model is developed in *Figure 2* and allows us to mathematically model the effects of critical parameters. For example, if an application consists of amplifying continuous waveforms, then this model allows us to determine gain-accuracy, stability, impedances, frequency response and output swing for a particular load requirement.

A Better Model (Continued)

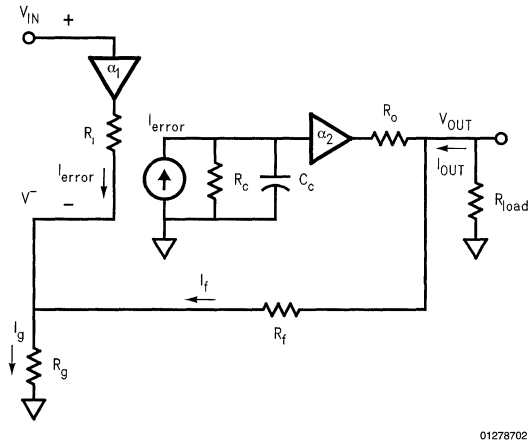


FIGURE 2. Practical Model

Mathematical Justification

Our first task is to derive a transfer function by nodal analysis for an infinite load condition.

$$I_{error} = I_g - I_f$$

$$I_{error} = \frac{V^-}{R_g} - \frac{V_{OUT} - V^-}{R_f}$$

$$V_{OUT} = I_{error}(\alpha_2 \cdot Z(s)) - I_f \cdot R_o$$

$$V^- = \alpha_1 \cdot V_{IN} - I_{error} \cdot R_i$$

Equation 1

After combining and eliminating the terms V^- and I_{error} in Equation 1, a transfer function is derived by dividing V_{OUT} by V_{IN} as seen in Equation 2.

$$\frac{V_{OUT}}{V_{IN}} = \frac{\alpha_1 \cdot A_v \left(1 + \frac{R_o}{A_v \cdot \alpha_2 \cdot Z(s)}\right)}{1 + \frac{R_f + R_i \cdot A_v + R_o\left(1 + \frac{R_i}{R_g}\right)}{\alpha_2 \cdot Z(s)}}$$

$$A_v = 1 + \frac{R_f}{R_g}$$

Equation 2

The Z(s) in Equation 2 is the open-loop transimpedance gain and its value is derived by dividing the output voltage V_{OUT} by the current through V_{IN}, shown in the schematic of *Figure 3.* The terms "α_1 and α_2" are the buffer gains while R_o is the open loop output resistance.

Although this equation has many variables, most of the terms are reduced by the open-loop response Z(s). The gain bandwidth independence for CFA is still true when Z(s) approaches infinity and the gain A_v remains small. The denominator term, "R_i" is multiplied by closed-loop gain A_v, and is small with a range of 16Ω to 490Ω for current feedback amplifiers. For a CLC406 R_i is 60Ω. The series output resistance R_o in the denominator is scaled by the ratio of the R_i and gain setting resistor R_g. While the R_o in the numerator is divided by the gain A_v, α_2, and Z(s). Typically, the open-loop R_o will vary from 5Ω to 25Ω.

The closed-loop output resistance approaches zero at dc, and is a function of the open-loop Z(s) frequency response. This is an important point when matching an output impedance by a back matching resistor. Typically back matching consists of placing a resistor that matches the characteristic impedance of a coaxial cable or specific devices input impedance, such as 50Ω.

The denominator term:

$$\frac{\alpha_2 \cdot Z(s)}{R_f + R_i \cdot A_v + R_o\left(1 + \frac{R_i}{R_g}\right)}$$

is referred to as the loop gain, and its closed-loop bandwidth is determined by denominator:

$$R_f + R_i \cdot A_v + R_o\left(1 + \frac{R_i}{R_g}\right)$$

As you increase gain A_v, you need to decrease R_f to maintain the largest possible –3 dB bandwidth. Manufacturers of CFA amplifiers specify a gain of 1 or 2 at a recommended R_f in the data sheet. For large gain changes the designer can select a value that best fits the desired new closed-loop gain A_v. This maximizes the bandwidth and maintains the same stability based upon maintaining the same ratio used to

Mathematical Justification (Continued)

select the original R_f in the datasheet. For small changes in gain, using the recommended R_f while changing the gain by R_g is acceptable unless stability becomes an issue.

As R_f decreases, a fundamental limit is reached by the approximate parallel combination of R_{load} and R_f. At this new load, the output voltage limit is set by the output current capability or the maximum output voltage swing into a no load condition. An alternative is to increase R_{load} or increase R_f. A bandwidth reduction in the ratio of the open-loop to closed-loop will result. This ratio decrease results in secondary effects such as a decrease in distortion, noise, gain accuracy, etc. Therefore, small changes are acceptable and large ratio changes are not recommended.

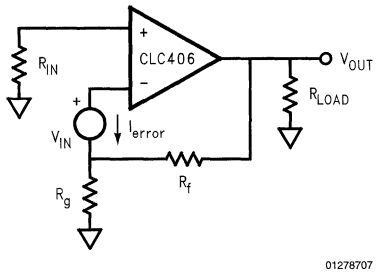


FIGURE 3. Simulation Method

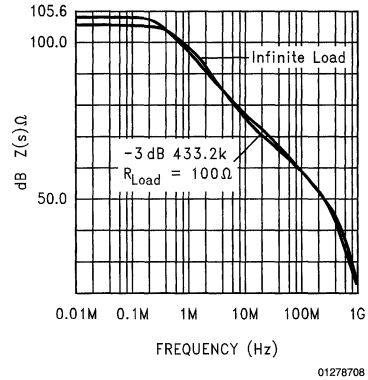
Open Loop Transimpedance Plot

At first it may seem strange to determine Z(s) by placing the voltage source in the inverting node of *Figure 3*. But this simplifies the simulation steps and has advantages for deriving the stability plot for investigating loads at the output pin.

The circuit in *Figure 3* simulates the open-loop transimpedance response Plot 1, while looking at 2 conditions:

1. Infinite load.
2. 100Ω load.

This plot helps explain the accuracy of our spice model and its effects for a practical application. Later this transimpedance gain Z(s) is normalized to an open-loop magnitude function.



Plot 1: Open Loop Transimpedance

The open loop transimpedance gain Plot 1 has axis in dB ohms versus frequency, and shows an approximate first order roll off function

$$Z(s) = \frac{R_c}{sR_cC_c + 1}$$

that includes secondary poles at the higher frequencies. To derive the value of R_c you take the inverse log of the axis:

$$10^{Z(s)/20}$$

at low frequencies while the 3 dB bandwidth gives C_c by the following:

$$\frac{1}{2\pi R_c f_{-3\,dB}}$$

Equation 3:

$$T(s) = \frac{Z(s) \cdot A_v}{R_f + R_i \cdot A_v}$$

where Z(s) is:

$$\frac{V_{OUT}}{I(V_{IN})}$$

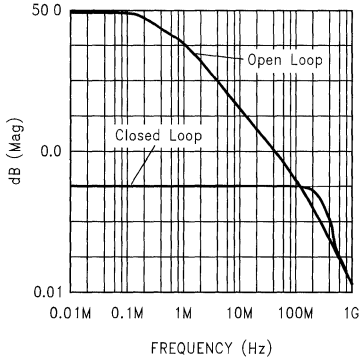
and I is the current in V_{IN}.

Open Loop Transimpedance Plot

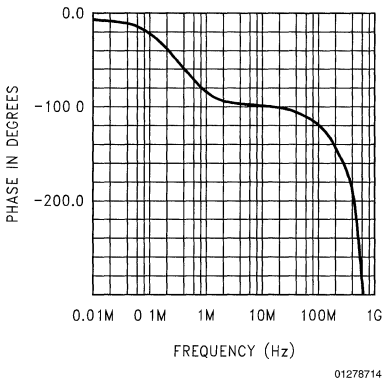
(Continued)

If we plot this transfer function for a CLC406 at an $A_V = 1$ with an $R_f = 768\Omega$ and $R_g = \infty$, the magnitude and phase information is shown in Plot 2 and 3. The output R_o term is ignored since R_l is low. The gain and phase margin is now available for determining the stability of our CLC406 Current Feedback Amplifier

With Plot 2, you find the unity gain crossover frequency point. This frequency point determines the phase of the amplifier on Plot 3 and it is subtracted from a 180° to derive the Phase Margin The value at 0 dB is at a frequency of 108 MHz and infers a phase margin of 62° The gain margin is measured from the −180° phase point and is the difference between the open-loop gain intersection and the 0 dB gain line in Plot 2, which is approximately 12 dB From control theory, these values are the indicators for optimum amplifier performance, although many designers will set the phase margin to 45° and 9 dB of gain margin. This results in 3 dB of frequency peaking or in the time domain signal preshoot and undershoot. Yet, we will still have a difference in the unity gain −3 dB frequency response of 220 MHz in simulation versus 200 MHz in an actual part The explanation for the difference will be explained later



Plot 2: Open and Closed Loop Magnitude



Plot 3: Open Loop Phase

Including Z(s)

The transfer function derived in Equation 2 has little meaning when looking at the poles and zeros for the amplifier without including transimpedance gain Z(s) At first let's substitute the first order pole of Z(s) into Equation 2. After some mathematical manipulation we discover a pole plus a zero as shown in. This is not intuitively obvious until you think about the amplifier's independent and dependent source and the inclusion of R_o to produce this zero.

$$\frac{V_{OUT}}{V_{IN}} = \frac{\alpha_1 \cdot A_V \left(1 + \frac{R_o}{A_V \cdot R_c}\right)}{1 + \frac{R_t}{R_c}} \cdot \frac{1 + s\left(\frac{R_o \cdot C_c}{A_V}\right)}{1 + s(R_t \| R_c \cdot C_c)}$$

Equation 3

Where the term.

$$R_t \cong R_f + A_V \cdot R_i + \left(1 + \frac{R_i}{R_g}\right) \cdot R_o ,$$

$$s = j\omega, \text{ and } \omega = 2\pi f.$$

At $s = 0$ the open-loop R_c reduces the terms in Equation 3 to the gain A_v times α_1 The zero in the numerator is an order of magnitude higher than the pole in denominator, while the pole has a new value of R_t times C_c where $R_c >> R_t$ Yet, we have not considered the effects of "Parasites" and their influences upon the stability of the amplifier.

External Parasites and Complex Loads

Connecting multiple circuits that have complex values (capacitance or inductance) at the nodes often results in stability issues for all types of amplifiers Recall the bandwidth of the CLC406 model indicated its −3 dB bandwidth to be higher than the measured unity-gain frequency This increase bandwidth is largely the result of parasitic components of the package and evaluation board layout [1] This adds additional zeros and poles to the equation that peaks the frequency response. Adding complex loads to various pins of our model causes stability questions that are probably more easily answered through simulation analysis rather than mathematical analysis

If a capacitance is in parallel with the load resistance, a decrease in phase margin will result. Capacitance in parallel with R_g decreases the loop gain, while capacitance in parallel with R_f increases the loop gain. All of these effects are seen in simulations for an amplifier

A common designed circuit is a transimpedance amplifier. The circuit in *Figure 4* shows replacing the R_g resistor with the equivalent photo-diode capacitance to simulate closed-loop stability for the CFA. Using the earlier spice simulation method to generate a Bode plot that determines the stability of the design. Adding an independent current source in parallel with the diode capacitance provides a method to simulate the transimpedance gain versus frequency.

External Parasites and Complex Loads (Continued)

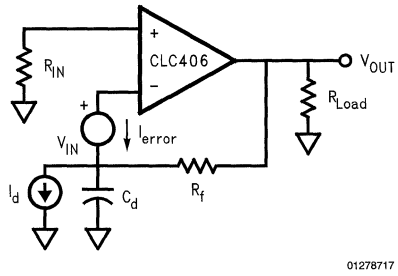


FIGURE 4. Photo Diode Analysis

Summary

Models are available from Comlinear Corporation for modeling many of the important parameters for high speed op amps. Application Note OA-18 "Simulation SPICE Models For Comlinear's Op Amps", details the schematics and parameters that are modeled. Ask for Comlinear's latest spice model diskette.

[1]R. Schmid, "Technique targets board parasites", EDN April 14, 1994 page 147.

Designing Active High Speed Filters

National Semiconductor
OA-26
Mark Sauerwald

Filters built from resistors (R), inductors (L) and capacitors (C) are known as RLC or passive filters and are the dominant type of filter for high frequency applications. The performance of these filters is typically limited by the inductors which are large, expensive and far from ideal in an electrical sense. By using amplifiers and feedback, the same filter characteristics can be achieved without the use of inductors, these filters are known as "active filters". An active filter will perform well only to the extent that the amplifiers in it behave in an ideal sense, so traditionally active filters have been limited to applications at frequencies below 1MHz. With the advent of low cost, very high speed operational amplifiers, it is now feasible to realize active filters with frequency ranges in the tens of MHz. With some of the newer high speed amplifiers such as the CLC449 – a 1.2GHz bandwidth amplifier, filters with corner frequencies above 100MHz have been built.

This application note will provide a recipe to realize active filters using low cost, high speed operational amplifiers. The filter topology that is used is the Sallen-Key Filter which uses the operational amplifier as a fixed gain block. This filter topology can be used with current feed-back or voltage feedback amplifiers, and you will be shown how to design low pass, high pass and band pass filters using this filter topology. This application note discusses a printed circuit board which will allow you to prototype active filters of up to 8 pole complexity. This is not a complete treatment of the subject of active filters, there are several good books published on that topic, some of which are listed in the bibliography. This is a simple method of getting a circuit that will work for most applications. The topics covered are:

1) Filter Types
2) Introduction to the second order, low pass Sallen-Key Filter
3) RC:CR Transformations to realize second order, high pass Sallen-Key Filters.
4) Cascading filter sections to achieve higher order filters and Band Pass Filters
5) Sensitivities to component values
6) How to select an Op-amp for use in an active filter
7) Compensation for finite Bandwidth Amplifiers
8) The National active filter evaluation boards

Filter Types

There are a large number of different types of filter responses. In this application note, we will concern ourselves with the three which I have found to be the most useful.

Butterworth Response

The Butterworth response maximizes the flatness in the pass band of the filter. The response is very flat near DC then begins to slowly roll off so that it is at -3dB at the cutoff frequency, and approaches an ultimate rolloff rate of -20ndB/decade where n is the order of the filter. Butterworth filters are used it is very important to maintain gain flatness, especially at low frequencies.

Bessel Response

In addition to altering the magnitude of the input signal depending upon its frequency, filters introduce a delay into the signal which is dependent upon frequency. This introduces a frequency dependent phase shift which distorts non-sinusoidal signals. Just as the Butterworth response maximizes the amplitude flatness through the passband, a Bessel Response minimizes the phase non-linearity in the passband.

Chebyshev Response

In some applications, the most important factor is how fast the filter cuts off the unwanted signal. Faster rolloff than what is seen by the Butterworth filter can be achieved if you are willing to accept some ripple in the passband.

Appendix A contains tables with the parameters required to design filters up to order 8 with Butterworth, Bessel, and Chebyshev responses. There are two tables for the Chebyshev response: one for 0.1dB maximum ripple in the passband, and one for 1dB of ripple in the passband.

Introduction to the Second Order, Low Pass Sallen-Key Filter

The circuit shown in figure 1 is a two pole, Sallen-Key Low Pass Filter. This filter (and any two pole filter) can be characterized by three parameters: K, ω_0 and Q. K is the DC gain of the filter. ω_0 is a measure of the corner frequency of the filter, while Q is a measure of how closely spaced the two poles are in the S plane. The values of K, Q and ω_0 are given by:

$$K = 1 + \frac{R_f}{R_g} \quad Q = \frac{m}{1+m^2} \quad \omega_0 = \frac{1}{mRC}$$

Q, K are unitless

ω_0 is in units of radians/sec. Divide ω_0 by 2π to get it in Hz.

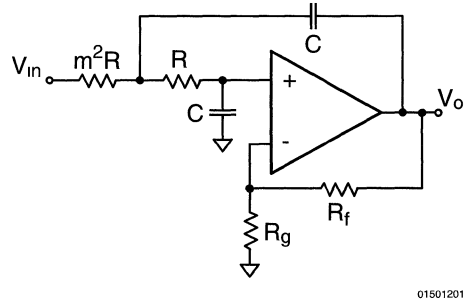


FIGURE 1. Sallen-Key Low Pass Filter with Equal C_S

The methodology to design a particular filter is to select the desired values for K, Q and ω_0 and then to use the above equations to determine the component values required. Q

Introduction to the Second Order, Low Pass Sallen-Key Filter (Continued)

can be obtained from the filter table in appendix A. ω_0 is your cutoff frequency and will be given to you from the design specification. In most filters, the actual value of ω_0 that you design for must be adjusted by the factor found in the filter table to get the proper -3dB frequency. K is another parameter that will be provided as part of the filter specification.

Since these three parameters are not completely independent, it may not be possible to meet all three points simultaneously. In this case, you should select another value of K, and then use an amplifier before or after the filter to make the overall gain meet the system requirements. For example if a Butterworth filter is desired (Q = 0.707) with a DC gain of 4, then we find that there is no positive value of m which will provide the required filter. Since a negative value of m implies the use of a negative value resistor, we need to find another solution. If however we select K = 1.5, then by using an m of 0.707 we obtain the required Q, and to obtain the proper overall gain, we can place an amplifier with a gain of 2.66 in front of the filter.

Even doing these things, it is possible that there will not be a solution to the desired filter, especially for high Q sections. In this case, see the methodology for a filter with non equal C_S shown in appendix B. This is a much more versatile circuit, but somewhat more difficult to design.

The methodology to use in selecting component values is outlined below:

1) Select R_f and R_g to obtain the desired K. If the amplifier that you are using is a current feedback amplifier, follow the guidelines in the datasheet to select appropriate values of R_f and R_g
2) Determine the value of m required using the following equation and the value of Q found in the design table:

$$m = \frac{1 \pm \sqrt{1 - 4Q^2(2-K)}}{2Q(2-K)}$$

3) If you cannot get a positive real solution for m, then select another value of K and go back to step 1. For $Q < 1.3$ select $K = 1$, for $1.3 < Q < 5$ select $K = 2$, for $Q > 5$ select $K \approx \sqrt{Q}$. If this still does not work, then see appendix B.
4) Arbitrarily select a value for C.
5) Determine the value of ω_0 to use by multiplying your desired cutoff frequency by the value of μ found in the filter design table. If your frequency specification is in Hz, remember to multiply it by 2π to get it into radians/sec.
6) Determine the value of R required using the equation below:

$$R = \frac{1}{\omega_0 mC}$$

7) If R turns out to be too large or too small for practical purposes, select another value for C (if R is too big, select a larger value for C, if R is too small select a smaller value of C) then go back to step 6.

Example:

Design a Butterworth filter, with a cutoff frequency of 10MHz, and a DC gain of 1.5. The CLC430 will be used in this

Introduction to the Second Order, Low Pass Sallen-Key Filter (Continued)

example.

1) Select R_f = 700Ω, R_g = 1.4kΩ as per the CLC430 data sheet.
2) Find Q from table: 0.707, use this to determine m = 0.707
3) Not required
4) No Arbitrarily select C = 0 1µF
5) ω_0 = 62.8E6 for a 10MHz filter
6) Calculate R. R turns out to be 0.23Ω
7) R is too small, therefore try a smaller C, and return to step 6. Select C = 100pF.
8) R = 225Ω, much better.

Figure 2 illustrates the final filter topology.

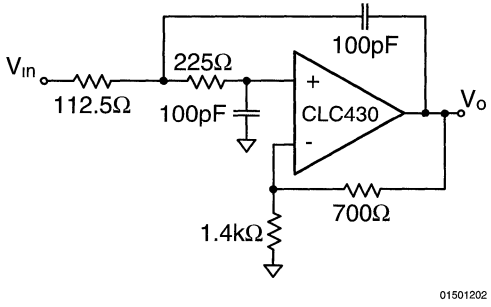


FIGURE 2. Example of Low Pass Filter

With slight modifications, the CLC430's evaluation board, CLC730013, can be used to test this circuit.

In some cases, it may be difficult to realize the desired filter with the constraint of equal valued capacitors. If this is the case, see appendix B to obtain expressions for Q and ω_0 where the capacitors can take on different values. This is most often necessary when trying to realize a filter with a high Q.

Transform a Low Pass Filter into a High Pass Filter

By changing capacitors into resistors, and resistors into capacitors, a low pass filter can be changed into a high pass filter. To make a high pass filter from a lowpass filter, replace each capacitor of value C with a resistor of value $1/\omega_0$ C, and each resistor with a capacitor of value $1/\omega_0$ R. For example the 100pF capacitors in the example circuit from the previous section should be replaced with 159Ω resistors, the 225Ω resistor should be replaced with a 71pF capacitor, and the 112Ω resistor should be replaced with a 142pF cap.

Alternately you can calculate component values using a method similar to that shown in the previous section. *Figure 3* is a second order Sallen-Key High pass filter. Q and ω0 are given by

$$Q = \frac{1}{2n + \frac{1}{n}(1-K)} \quad \text{and} \quad \omega_0 = \frac{1}{nRC}$$

01501215

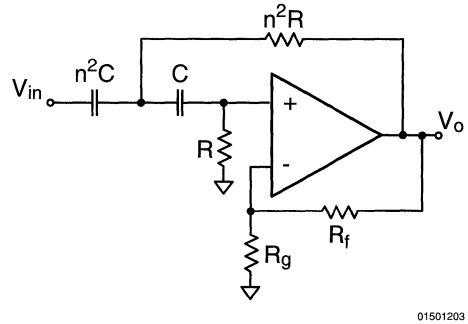


FIGURE 3. Sallen-Key High Pass Filter

Cascading Filter Sections

Higher order filters can be realized by cascading lower order filters. A filter of order n can be realized by cascading n/2 second order sections. Note that to obtain a fourth order Butterworth filter you do not cascade two second order Butterworth filter sections. The pole locations for the fourth order filter are all different and different values of Q and ω_0 will need to be used for each section. Cascading active filters of the Sallen-Key topology is easy. Since the output impedances of the filters are very small, cascading them consists of just connecting one section to the next (each filter section is designed assuming 0 source impedance.)

If a filter of odd order is desired, the last pole can be added with a simple passive filter at the output of the active filter as shown in *Figure 4*.

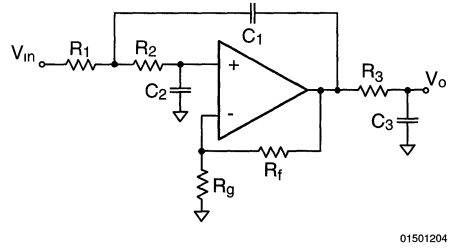


FIGURE 4. Order Sallen-Key Filter

Cascading Filter Sections (Continued)

When cascading filters, one question that arises is what order the sections should be placed. The answer to this is the same as the answer to all filter questions – "it depends". Two factors that need to be considered when cascading filter sections are "Am I liable to have intermediate signals that might clip or distort?" and "How important is noise to me?"

In filters with sections where there are large Qs, the maximum amplitude of the signal in between stages may be larger than the input or the output amplitude. This can lead to undue distortion of the signal. This will most likely be an issue if there are filter sections with large Qs, and the input signals are large. Strategies that can be used to combat this effect are to put the stages with the lowest Qs and gains first, and cascade the higher gain sections later. Another way that the dynamic range could be increased would be to use an op-amp with larger dynamic range. The CLC432 is a dual, current feedback op-amp that is well suited to active filter applications and has an output voltage swing of $28V_{PP}$ when driving a light load.

In order to minimize the broadband noise that is present in an active filter, stages should be cascaded with the highest Q, and highest gain sections first, then followed by lower gain sections. Other strategies that should be considered when trying for low noise are using the lowest possible value resistors to reduce thermal noise and to select low noise op amps such as the CLC428, dual, voltage feedback op amp.

As you can see from the previous two paragraphs, the order in which to place the filter stages is dependent upon the requirements of your application. There is no best way to cascade your filter stages.

Component Value Sensitivities

If the component values used in realizing the filter are not exactly what the calculations arrive at, and they won't be, then the filter characteristics will be different from what was desired. Even if time is spent trimming components to the exact desired value, variations caused by temperature shifts, aging and other external and internal sources will cause the filter characteristics to vary. A good design will result in minimal variation in the filter characteristics as a result of the component value variations that might be expected. To estimate the effect on the filter characteristics as component values vary, sensitivity figures are used.

A sensitivity figure tells how much variation there will be in one characteristic when a parameter is changed. Hence S_R^ω refers to the incremental change in ω for an incremental change in R. If is S_R^ω 2 then there will be a 2% variation in ω for a 1% variation in R. The two parameters with which we are most concerned in our filter designs are Q and $\omega 0$, therefore it would be useful to look at what component variations have an effect on these parameters, and to determine what these sensitivities are. S_x^A is defined as:

$$S_x^A = \frac{d(\ln A)}{d(\ln x)} = \frac{x}{A}\frac{dA}{dx}$$

In the lowpass filter of *Figure 1*, the equation that describes Q, has n and K as its variables, hence Q is only sensitive to the ratio of resistor values and to K which is determined by R_f and R_g . For this filter the sensitivity that we have worry the most about is the sensitivity to K, which is very large for high Q sections.

Selecting an Op Amp for Use in an Active Filter

Although there are many factors that go into selecting an op amp for use in any application, most filter applications can be satisfied by looking at a just four parameters: Bandwidth Recommended Gain range Noise Dynamic Range

- Bandwidth
- Recommended Gain Range
- Noise
- Dynamic Range

Bandwidth

As a general rule, when selecting an op amp for a filter, make certain that it has a bandwidth of at least 10x the intended filter frequency, and preferably 20x. As an example to design a 10MHz low pass filter, use an op amp with at least 100MHz of bandwidth. If designing a high pass filter, make certain that the bandwidth of the op amps will be sufficient to pass all of your signal. Another point to watch is that your op amp must have this band-width under the conditions that you intend to use it, for example, the same gain, signal level and power supply voltage. An op amp that is specified as a 100MHz op amp because it has 100MHz bandwidth with ±15V supplies, 50mV output level and a gain of 1 is not likely to be useful in a 10MHz filter application. If in doubt, configure the amplifier that you are considering at the gain that you are intending to use (K) and measure its bandwidth.

Recommended Gain Range

Your filter design will be dictating to you the gains at which you will be setting your op amps. If the chosen op amp is a voltage feedback op amp, use at gains outside the recommended gain range is liable to lead to lower than expected bandwidth at best and oscillation at worst. For a current feedback op amp, operation at gains outside of the recommended range is liable to force you to use resistor values for R_f and R_g which are way too small or large for practical realization.

Noise

The input voltage and current noises of the op amp will contribute to the noise at the output of the filter. In applications where noise is a major concern, you will need to calculate these contributions (as well as the contributions of the thermal noise of the resistors in the circuit) to determine if the added noise encountered with an active filter is acceptable. Noise can be reduced by selecting low noise, high speed op amps such as the CLC425 or CLC428.

Dynamic Range

In filters which have high Q sections, it is possible that there will be intermediate signals that are larger than either the input signal or the output signal. For the filter to operate properly, all of these signals must be passed without clipping or excessive distortion.

Secondary Specifications

In addition to the four primary specifications above, there are several secondary parameters that you may want to take into consideration. These would include phase linearity (this

Secondary Specifications (Continued)

is generally better in current feedback op amps), packaging (duals, quads available?), power dissipation, price and availability of technical support.

Summary of High Speed Dual Op Amps

	Bandwidth (with 500mV output, A_V = 2) (MHz)	Recommended Gain Range in Filter Applications	Noise Voltage (nV√Hz)	Noise Current (pA√Hz)	Output Dynamic Range (100Ω Load (V)
CLC412	250	1-8	3	12/2	+3.1/–2.9
CLC416	80	1-5	2	2	+3.5/–3.5
CLC428	80	1-5	2	2	+3.5/–3.5
LM6172	50	1-5	12	1	+9/–8.5
LM6182	100	1-5	4	16/3	±11
CLC5602	120	1-5	3	8.5/6.9	±3.8
CLC5622	150	1-5	2.8	10/7.5	±3.8
CLC432	62 (V_O = 4V)	1-20	3.3	13/2	+6/–6

Compensation for Finite Bandwidth Amplifiers

In all of the analysis that we have done, we have assumed that the op amps are ideal op amps with infinite bandwidth. Unfortunately, price and delivery of these op amps makes them a poor choice for actual realizable filters. The effect of using a real op amp in place of an ideal one is to slightly lower the corner frequency of the filter, and if we are somewhat clever, we can compensate for this by pre-distorting the component values of the components so that the final filter is much closer to what we wanted. The mathematical background for this is explained in application note *OA-21*. Since the goal of this application note is to make the design of active filters easy, we are going to skip all of the development work, and go directly to the final result. To make use of this method there is a parameter that you will need to know for the op amp that you intend to use, and this is the time delay through the amplifier, called T. The value of T can be obtained in a few different ways: one is to look at the frequency response plots for the op amp that you are considering using. Find the frequency at which the phase delay is 180°, multiply this frequency by 2 and take the reciprocal to obtain the time delay through the amplifier. In the case of the CLC412, the 180° frequency is about 300MHz, multiplying by two and taking the reciprocal yields a time delay, T, of 1.7ns. Another way that you can get a value for T with a National op amp is to use the spice model, and provide the amplifier, configured as you want it, with a pulse, and measure the delay between the input edge and the output edge.

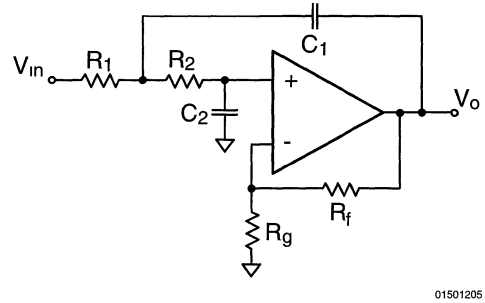


FIGURE 5. Low Pass Sallen-Key Filter

For the filter shown in *Figure 5*, you can calculate the values of R_1 and R_2 in the following way: Calculate R_2 by solving:

$$R_2^2 - bR_2 - d = 0$$

where

$$b = \frac{1}{\omega_0 C_2}\left[\frac{1}{Q} - \omega_0 KT\right] \quad d = \left(\frac{1}{\omega_0 C_2}\right)^2 \left(\frac{KT\omega_0}{Q} + K - 1 - \frac{1}{\alpha}\right)$$

$$\alpha = \frac{C_1}{C_2}$$

Once you have R_2, you can get R_1 with:

$$R_1 = \frac{R_2 - \frac{1}{\omega_0 C_2 Q}}{\alpha(K-1)-1}$$

Compensation for Finite Bandwidth Amplifiers (Continued)

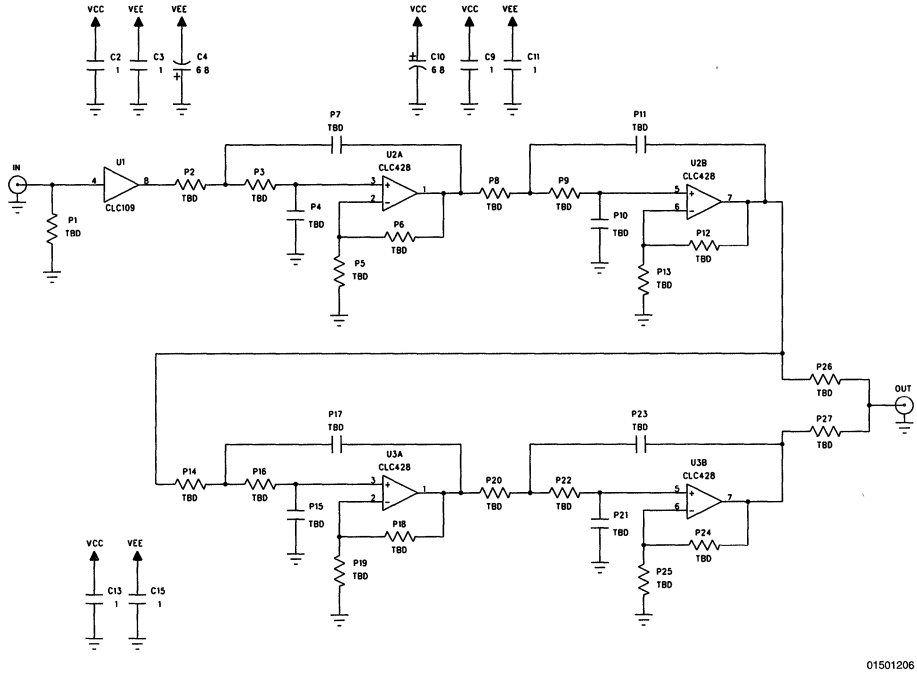


FIGURE 6. Schematic for Active Filter Board

The Active Filter Boards

To make prototyping active filters easier, Comlinear has designed two different active filter evaluation boards. A schematic of the first board is shown in *Figure 6.* It consists of a CLC109 (or CLC111) input buffer, followed by four cascaded Sallen Key filter sections, realized with two dual op amps. The board was designed using surface mount components, so the resistors and capacitors are interchangeable. This board is available from National Semiconductor as the CLC730061 board and is shipped as a bare PCB. The top and bottom views of the evaluation board are shown in *Figure 7.* The other board also allows for up to four cascaded biquad sections but restricts the user to designs using K = 1 since rather than op amps, this board uses a quad, unity gain buffer. The board can be ordered as part number CLC730023 and is fully documented in the CLC114 evaluation board datasheet, available as National Semiconductor Literature #660114-001 or in the 1997 Comlinear Databook.

Conclusion

Using the principles outlined in this application note, an active filter design need not be a daunting task. You can feel free to impress your friends at a cocktail party by whipping out pencil and paper and doing a design for a 5MHz low pass filter. You don't have to tell them how easy it really is, just wow them and bask in their awed looks.

Conclusion (Continued)

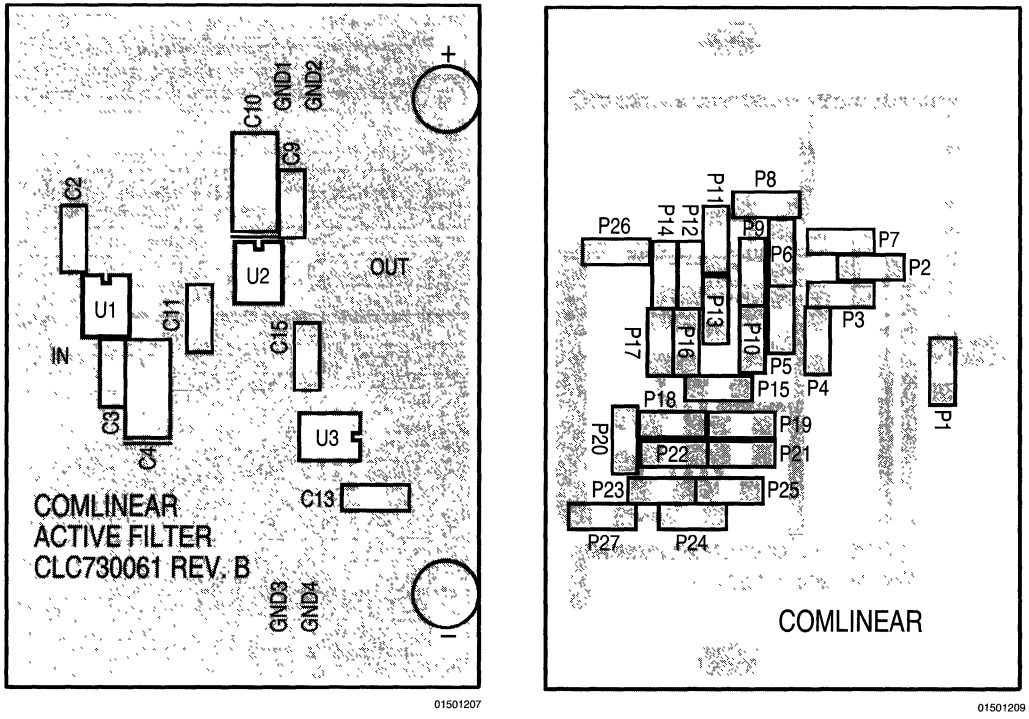


FIGURE 7. Top & Bottom Views of Active Filter Evaluation Board

Appendix A
Filter Design Tables

Butterworth Low Pass Filter

n	ω_1	Q_1	ω_2	Q_2	ω_3	Q_3	ω_4	Q_4	Attenuation at $2f_C$(dB)
2	1	0.707	1						15
3	1	1.000	1						21
4	1	0.541	1	1.306					27
5	1	0.618	1	1.620	1				33
6	1	0.518	1	0.707	1	1.932			39
7	1	0.555	1	0.802	1	2.247	1		45
8	1	0.510	1	0.601	1	0.900	1	2.563	51

Bessel Low Pass Filter

n	ω_1	Q_1	ω_2	Q_2	ω_3	Q_3	ω_4	Q_4
2	1.274	0.577						
3	1.453	0.691	1.327					
4	1.419	0.522	1.591	0.806				
5	1.561	0.564	1.760	0.917	1.507			
6	1.606	0.510	1.691	0.611	1.907	1.023		

Appendix A
Filter Design Tables (Continued)

Bessel Low Pass Filter (Continued)

7	1.719	0.533	1.824	0.661	2.051	1.127	1.685	
8	1.784	0.506	1.838	0.560	1.958	0.711	2.196	1.226

dB Ripple Chebyshev Filter

n	ω_1	Q_1	ω_2	Q_2	ω_3	Q_3	ω_4	Q_4	Attenuation at $2f_c$(dB)
2	1.82	0.767							3.31
3	1.300	1.341	0.969						12.24
4	1.153	2.183	0.789	0.619					23.43
5	1.093	3.282	0.797	0.915	0.539				34.85
6	1.063	4.633	0.834	1.332	0.513	0.599			46.29
7	1.045	6.233	0.868	1.847	0.575	0.846	0.377		57.72
8	1.034	8.082	0.894	2.453	0.645	1.183	0.382	0.593	69.16

1.00dB Ripple Chebyshev Filter

n	ω_1	Q_1	ω_2	Q_2	ω_3	Q_3	ω_4	Q_4	Attenuation at $2f_c$(dB)
2	0.050	0.957							11.36
3	0.997	2.018	0.494						22.46
4	0.993	3.559	0.529	0.785					33.87
5	0.994	5.556	0.655	1.399	0.289				45.31
6	0.995	8.004	0.747	2.198	0.353	0.761			56.74
7	0.996	10.899	0.808	3.156	0.480	1.297	0.205		68.18
8	0.997	14.240	0.851	4.266	0.584	1.956	0.265	0.753	79.62

Appendix B
Non-Equal C Sallen-Key Filter Methodology

The circuit shown in *Figure 8* is a two pole, Sallen-Key low pass filter similar to the one seen in the body of this application note. The difference is that in this figure we have removed the constraint that the two capacitors remain equal by adding the "n" as an additional degree of freedom. Like the filter from *Figure 1*, this filter can be characterized three parameters: K, ω_0 and Q. K is the DC gain of the filter. ω_0 is a measure of the corner frequency of the filter, while Q is a measure of how closely spaced the two poles are in the S plane. The values of K, Q and ω_0 are given by:

$$K = 1 + \frac{R_f}{R_g}$$

$$Q = \frac{mn}{1 + m^2 + (mn)^2(1-K)}$$

$$\omega_0 = \frac{1}{mnRC}$$

Q,K are unitless

ω_0 is in units of radians/sec. Divide ω_0 by 2π to get it in Hz.

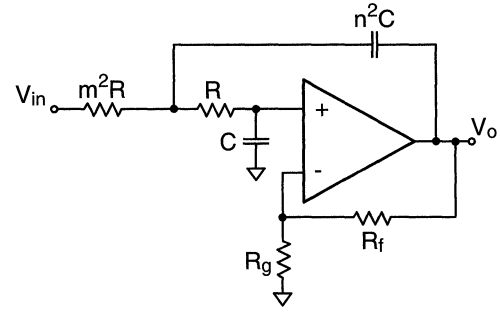


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FIGURE 8. Pole Sallen-Key Low Pass Filter with Unequal Capacitors

The methodology to design a particular filter is to select the desired values for K, Q and $\omega_0$and then to use the above equations to determine the component values required. Q can be obtained from the filter table in appendix A. ω_0 is your cutoff frequency and will be given to you from the design

Appendix B
Non-Equal C Sallen-Key Filter Methodology (Continued)

specification. In most filters, the actual value of ω_0 that you design for must be adjusted by the factor found in the filter table to get the proper -3dB frequency. K is another parameter that will be provided as part of the filter specification.

The methodology to use in selecting component values is outlined below:

1) Select R_f and R_g to obtain the desired K. If the amplifier that you are using is a current feedback amplifier, follow the guidelines in the data sheet to select appropriate values of R_f and R_g
2) Arbitrarily select a value for n. This value should be small for low Q filters and should be larger for higher Q filters. Remember that the standard values for capacitors are limited, and n should be chosen with this in mind.
3) Determine the value of m required using the following equation and the value of Q found in the design table:

$$m = \frac{\frac{n}{Q} \pm \sqrt{\left(\frac{n}{Q}\right)^2 - 4\left(1+n^2(1-K)\right)}}{2\left(1+n^2(1-K)\right)}$$

4) If you cannot get a positive real solution for m, then select another value of K or n and go back to step 1.
5) Arbitrarily select a value for C.
6) Determine the value of ω_0 to use by multiplying your desired cutoff frequency by the value of ω found in the filter design table. If your frequency specification is in Hz, remember to multiply it by 2π to get it into radians/sec.
7) Determine the value of R required using the equation below:

$$R = \frac{1}{\omega_0 m C}$$

8) If R turns out to be too large or too small for practical purposes, select another value for C (if R is too big, select a larger value for C, if R is too small select a smaller value of C) then go back to step 7.

Appendix C
Transfer Functions for Some of the Filters

Transfer function for filter in *Figure 5*:

$$\frac{V_o}{V_{in}} = \frac{\frac{K}{R_1R_2C_1C_2}}{s^2 + s\left(\frac{1}{C_2R_2} - \frac{K}{C_2R_2} + \frac{1}{R_2C_1} + \frac{1}{R_1C_1}\right) + \frac{1}{R_1R_2C_1C_2}}$$

Transfer function for filter in *Figure 3*:

$$\frac{V_o}{V_{in}} = \frac{s^2K}{s^2 + \frac{s}{RC}\left[2 + \frac{1}{n^2}(1-K)\right] + \frac{1}{C^2R^2n^2}}$$

Appendix D Bibliography

S. Franco: *Design with Operational Amplifiers and Analog Integrated Circuits*, McGraw Hill, 1988

K. Lacanette, ed.: *Switched Capacitor Filter Handbook*, National Semiconductor, April 1985

G. Temes and S. Mitra: *Modern Filter Theory and Design*, Wiley, 1973

M. Steffes: *Simplified Component Value Pre-Distortion For High Speed Active Filters OA-21*, Comlinear, March 1993

A.B. Williams, F.J. Taylor: *Electronic Filter Design Handbook*, McGraw Hill 1988

Note: The circuits included in this application note have been tested with National Semiconductor parts that may have been obsoleted and/or replaced with newer products. Please refer to the CLC to LMH conversion table to find the appropriate replacement part for the obsolete device.

Low-Sensitivity, Lowpass Filter Design

National Semiconductor
OA-27
Kumen Blake

Introduction

This Application Note covers the design of a Sallen-Key (also called KRC or VCVS [voltage-controlled, voltage-source]) lowpass biquad with low component and op amp sensitivities. This method is valid for either voltage-feedback or current-feedback op amps. Basic techniques for evaluating filter sensitivity performance are included. A filter design example illustrates the method.

Changes in component values over process, environment and time affect the performance of a filter. To achieve a greater production yield, we need to make the filter insensitive to these changes. This Application Note presents a design algorithm that results in low sensitivity to component variation.

Lowpass biquad filter sections have the transfer function:

$$\frac{V_O}{V_{IN}} \approx \frac{H_0}{1 + \left(1/(\omega_p Q_p)\right) s + (1/\omega_p^2) s^2}$$

where s=jω, H_o is the DC gain, ω_p is the pole frequency, and Q_p is the pole quality factor. Both ω_p and Q_p affect the filter phase response, ω_p the filter cutoff frequency, Q_p the peaking, and H_o the gain. For these reasons, we will minimize the sensitivities of H_o, ω_p and Q_p to all of the components (see *Appendix A*).

To achieve the best production yield, the nominal filter design must also compensate for component and board parasitics. For information on filter component pre-distortion, see Reference [5]. SPICE simulations, with good component and board models, help adjust the nominal design point to compensate for parasitics.

See *Appendix A* for an overview of sensitivity analysis, with applications to filter design. See *Appendix B* for useful sensitivity properties and formulas. See the references listed in *Appendix C* for a more complete discussion of sensitivity functions, their applications, and other approaches to improving the manufacturing yield of your filter.

KRC Lowpass Biquad

The biquad shown in *Figure 1* is a Sallen-Key lowpass biquad. V_{IN} needs to be a voltage source with low output impedance. R_1 and R_2 attenuate V_{IN} to keep the signal within the op amp's dynamic range. The Thevenin equivalent of V_{IN}, R_1 and R_2 is a voltage source αV_{IN}, with an output impedance of R_{12}, where:

$\alpha = R_2/(R_1 + R_2)$

$R_{12} = (R_1 \parallel R_2)$

The input impedance in the passband is:

$Z_{IN} = R_1 + R_2, \quad \omega << \omega_p$

The transfer function is:

$$\frac{V_O}{V_{IN}} \approx \frac{H_0}{1 + \left(1/(\omega_p Q_p)\right) s + (1/\omega_p^2) s^2}$$

where:

$$K = 1 + R_f/R_g$$

$$H_0 = \alpha K$$

$$1/(\omega_p Q_p) = R_{12} C_5 (1 - K) + R_3 C_4 + R_{12} C_4$$

$$1/\omega_p^2 = R_{12} R_3 C_4 C_5$$

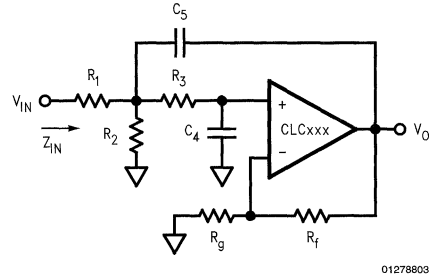

FIGURE 1. Lowpass Biquad

To achieve low sensitivities, use this design algorithm:

1. Partition the gain for good Q_p sensitivity and dynamic range performance:
   - — Use a low noise amplifier before this biquad if you need a large gain
   - — Select K for good sensitivity with this empirical formula:

$$K = \begin{cases} 1 & , \ 0.1 \le Q_p \le 1.1 \\ \dfrac{2.2 Q_p - 0.9}{Q_p + 0.2} & , \ 1.1 < Q_p < 5 \end{cases}$$

   - — These values also reduce the op amp bandwidth's impact on the filter response, and increase the bandwidth for voltage-feedback op amps. When $Q_p \ge 5$, the sensitivities of this biquad are very high
   - — Set α as close to 1 as possible while keeping the signal within the op amp's dynamic range

KRC Lowpass Biquad (Continued)

2. Select an op amp with adequate bandwidth ($f_{3\ dB}$) and slew rate: (SR):

   $f_{3\ dB} \geq 10 f_c$

   $SR > 5 f_c\ V_{peak}$

   where f_c is the corner frequency of the filter, and V_{peak} is the largest peak voltage. Make sure the op amp is stable at a gain of $A_v = K$.
3. Select R_f and R_g so that:

   $K = 1 + R_f/R_g$

   For current-feedback op amps, use the recommended value of R_f for a gain of $A_v = K$. For voltage-feedback op amps, select R_f for noise and distortion performance.
4. Initialize the resistance level ($R = \sqrt{R_{12} R_3}$). This value is a compromise between noise performance, distortion performance, and adequate isolation between the op amp outputs and the capacitors.
5. Initialize the capacitance level ($C = \sqrt{C_4 C_5}$), the resistor ratio ($r^2 = R_{12} / R_3$), the capacitor ratio ($c^2 = C_4/C_5$) and the capacitors:

   $C = 1/(R\omega_p)$

   $r^2 = 0.10$

$$c^2 = \max\left(\left(\frac{1 + \sqrt{1 + 4Q_p^2(1+r^2)(K-1)}}{2 \cdot Q_p \cdot (1+r^2)/r}\right)^2,\ 0.10\right)$$

   $C_4 = cC$

   $C_5 = C/c$
6. Set the capacitors C_4 and C_5 to the nearest standard values.
7. Recalculate C, c^2, R and r^2:

   $C = \sqrt{C_4 C_5}$

   $c^2 = C_4/C_5$

   $R = 1/(C\omega_p)$

$$r^2 = \left(\frac{2 \cdot cQ_p}{1 + \sqrt{1 + 4Q_p^2(K - 1 - c^2)}}\right)^2$$

8. Calculate R_{12} and the resistors:

   $R_{12} = rR$

   $R_1 = R_{12}/\alpha$

   $R_2 = R_{12}/(1-\alpha)$

   $R_3 = R/r$

V_{IN} can represent a source driving a transmission line, with R_1 and R_2 the source and terminating resistances. For this type of application, make these modifications to the design algorithm:

- Select R_1 and R_2 to properly terminate the transmission line (R_1 includes the source resistance)
- Calculate α and R_{12}
- Adjust C and R so that $R_{12} = rR$

To evaluate the sensitivity performance of this design, follow these steps:

1. Calculate the resulting sensitivities:

α_i	$S_{\alpha_i}^{H_o}$	$S_{\alpha_i}^{\omega_p}$	$S_{\alpha_i}^{Q_p}$
K	1	0	$\left(K \cdot Q_p \cdot \frac{r}{c}\right)$
R_1	$-(1-\alpha)$	$-\frac{\alpha}{2}$	$(\alpha) \cdot \left(Q_p \cdot \frac{c}{r} - \frac{1}{2}\right)$
R_2	$(1-\alpha)$	$-\frac{1-\alpha}{2}$	$(1-\alpha) \cdot \left(Q_p \cdot \frac{c}{r} - \frac{1}{2}\right)$
R_3	0	$-\frac{1}{2}$	$-\left(Q_p \cdot \frac{c}{r} - \frac{1}{2}\right)$
R_f	$\frac{K-1}{K}$	0	$\left((K-1) \cdot Q_p \cdot \frac{r}{c}\right)$
R_g	$-\frac{K-1}{K}$	0	$-\left((K-1) \cdot Q_p \cdot \frac{r}{c}\right)$
C_4	0	$-\frac{1}{2}$	$-\left((K-1) \cdot Q_p \cdot \frac{r}{c} + \frac{1}{2}\right)$
C_5	0	$-\frac{1}{2}$	$\left((K-1) \cdot Q_p \cdot \frac{r}{c} + \frac{1}{2}\right)$

Reducing $\left|S_K^{Q_p}\right|$ lowers the biquad's sensitivity to the op amp bandwidth.

KRC Lowpass Biquad (Continued)

2. Calculate the relative standard deviations of H_o, ω_p and Q_p:

$$\left(\frac{\sigma_x}{X}\right)^2 \approx \sum_i \left(\left|S_{\alpha_i}^X\right| \cdot \frac{\sigma_{\alpha_i}}{\alpha_i}\right)^2$$

In this formula, use:

— The nominal values of H_o, ω_p and Q_p for X

— The nominal values of R_1, R_2, R_3, R_f, R_g, C_4 and C_5 for α_i (*do not use* K since it is not a component)

— The capacitor and resistor standard deviations for σ_{α_i}. For parts with a uniform probability distribution,

$$\sigma_{\alpha_i} = \frac{\max(\alpha_i) - \min(\alpha_i)}{\sqrt{12}}$$

3. If temperature performance is a concern, then estimate the change in nominal values of H_o, ω_p and Q_p over the design temperature range:

$$X(T) \approx X\left(1 + \sum_i \left(S_{\alpha_i}^X \cdot \frac{\alpha_i(T) - \alpha_i}{\alpha_i}\right)\right)$$

In this formula, use:

— The nominal values, at room temperature, of H_o, ω_p and Q_p for X

— The nominal values, at room temperature, of R_1, R_2, R_3, R_f, R_g, C_4 and C_5 for α_i (*do not use* K since it is not a component)

— The nominal resistor and capacitor values at temperature T for $\alpha_i(T)$

4. Estimate the probable ranges of values for H_o, ω_p and Q_p:

$X \geq (1-3 \bullet \sigma_x/X) \bullet \min(X(T))$

$X \leq 1+3 \bullet \sigma_x/X) \bullet \max(X(T))$

where X is H_o, ω_p and Q_p.

Design Example

The circuit shown in *Figure 2* is a 3rd-order Chebyshev lowpass filter. Section A is a buffered single pole section, and Section B is a lowpass biquad. Use a voltage source with low output impedance, such as the CLC111 buffer, for V_{IN}.

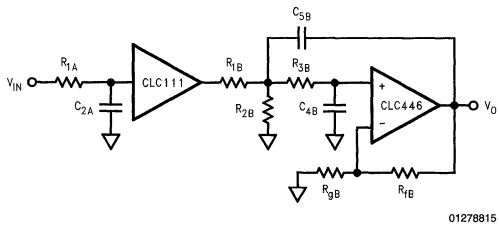

FIGURE 2. Lowpass Filter

The nominal filter specifications are:

f_c = 500 MHz (passband edge frequency)

f_s = 100 MHz (stopband edge frequency)

A_p = 0.5 dB (maximum passband ripple)

A_s = 19 dB (minimum stopband attenuation)

H_o = 0 dB (DC voltage gain)

The 3rd-order Chebyshev filter meets our specifications (see References [1–4]). The resulting –3 dB frequency is 58.4 MHz. The pole frequencies and quality factors are:

Section	A	B
$\omega_p/2\pi$ [MHz]	53:45	31:30
Q_p [ ]	1.706	—

Overall Design:

1. Restrict the resistor and capacitor ratios to:
   $0.1 \leq r^2 \leq 10$
   $0.1 \leq c^2 \leq 10$
2. Use 1% resistors (chip metal film, 1206 SMD, 25 ppm/°C)
3. Use 1% capacitors (ceramic chip, 1206 SMD, 100 ppm/°C)
4. Use standard resistor and capacitor values
5. The temperature range is –40°C to 85°C, and room temperature is 25°C

Section A Design:

1. Use the CLC111. This is a closed-loop buffer.
   — $f_{3\ db}$ = 800 MHz > 10 f_c = 500 MHz
   — SR = 3500V/µs, while a 50 MHz, $2V_{pp}$ sinusoid requires more than 250V/µs
   — $C_{ni(111)}$ = 1.3 pF (input capacitance)
2. We selected R_{1A} for noise, distortion and to properly isolate the CLC111's output and C_{2A}. The capacitor C_{2A} then sets the pole frequency:
   $1/\omega_p = R_{1A}C_{2A}$
   The results are in the table below:
   — The Initial Value column shows values from the calculations above
   — The Adjusted Value column shows the component values that compensate for $C_{ni(111)}$ and for the CLC111's finite bandwidth (see Comlinear's Application Note on filter component pre-distortion [5])
   — The Standard Value column shows the nearest available standard 1% resistors and capacitors

Component	Value		
	Initial	Adjusted	Standard
R_{1A}	108Ω	100Ω	100Ω
C_{2A}	47 pF	47 pF	47 pF
$C_{ni(111)}$	—	1.3 pF	1.3 pF

Design Example (Continued)

Section B Design:

1. The recommended value of K_B for $Q_p = 1.706$ is:

$$K_B = \frac{2.2(1.706) - 0.9}{(1.706) + 0.2} = 1.50$$

Set $\alpha_B = H_o/K_B = 0.667$.

2. Use the CLC446. This is a current-feedback op amp
   — $f_{3\ dB} = 400\ MHz \approx 10\ f_c = 500\ MHz$
   — SR = 2000V/μs > 250V/μs (see Item #1 in "Section A Design")
   — $C_{ni(446)} = 1.0\ pF$ (non-inverting input capacitance)
3. Set R_{fB} to the CLC446's recommended R_f at $A_V = +15$:
   $R_{fB} = 348\Omega$
   Then set $R_{gB} = 696\Omega$ so that $K_B = 1.50$.
4. Initialize the resistor level for noise and distortion performance:
   $R \approx 200\Omega$
5. Initialize the capacitor level, resistor and capacitor ratios, and the capacitors:

$$C \approx \frac{1}{(200\Omega) \cdot (2\pi(53.45\ MHz))} = 15\ pF$$

$r^2 \approx 0.10$
$c^2 \approx \max(0.0983, 0.10) = 0.1000$
$C_{4B} \approx 4.7\ pF$
$C_{5B} \approx 4.7\ pF$

6. Set the capacitors to the nearest standard values:
   $C_{4B} = 4.7\ pF$
   $C_{5B} = 4.7\ pF$
7. Recalculate the capacitor level and ratio, and the resistor level and ratio:

$$C = \sqrt{(4.7\ pF) \cdot (47\ pF)} = 14.86\ pF$$

$$c^2 = (4.7\ pF)/(47\ pF) = 0.1000$$

$$R = \frac{1}{(14.86\ pF) \cdot (2\pi(53.45\ MHz))} = 200.4\Omega$$

$$r^2 = 0.1020$$

8. Calculate R_{12B} and the resistor values:
   $R_{12B} = 64.0\Omega$
   $R_{1B} = 96.0\Omega$
   $R_{2B} = 192\Omega$
   $R_{3B} = 627\Omega$
   The resulting component values are:

Component	Value		
	Initial	Adjusted	Standard
R_{1B}	96.0Ω	78.9Ω	78.7Ω
R_{2B}	192Ω	158Ω	158Ω
R_{3B}	627Ω	582Ω	576Ω
C_{4B}	4.7 pF	3.7 pF	3.6 pF

Component	Value		
	Initial	Adjusted	Standard
$C_{ni(446)}$	—	1.0 pF	1.0 pF
C_{5B}	47 pF	47 pF	47 pF
R_{fB}	348Ω	348Ω	348Ω
R_{gB}	696Ω	696Ω	698Ω

9. The sensitivities for this design are:

α_i	H_o S_{α_i}	ω_p S_{α_i}	Q_p S_{α_i}
K	1.00	0.00	2.58
R_{1B}	−0.33	−0.33	0.79
R_{2B}	0.33	−0.17	0.40
R_{3B}	0.00	−0.50	−1.19
R_{fB}	0.33	0.00	0.86
R_{gB}	−0.33	0.00	−0.86
C_{4B}	0.00	−0.50	−1.36
C_{5B}	0.00	−0.50	1.36

10. The relative standard deviations of H_o, ω_p and Q_p are:
    $\sigma_{H_o}/H_o \approx 0.38\%$
    $\sigma_{\omega_p}/\omega_p \approx 0.55\%$
    $\sigma_{Q_p}/Q_p \approx 1.58\%$
    These standard deviations are based on a uniform distribution, with all resistors and capacitor values being independent:

$$\frac{\sigma_R}{R} \approx \frac{\sigma_C}{C} \approx \frac{1.00\% - (-1.00\%)}{\sqrt{12}} \approx 0.58\%$$

11. The nominal values of H_o, ω_p and Q_p over the design temperature range are:

T [°C]	−40	25	85
H_o [V/V]	1.000	1.000	1.000
$\omega_p/2\pi$ [MHz]	53.88	53.45	53.00
Q_p [ ]	1.706	1.706	1.706

12. The probable ranges of values for H_o, ω_p and Q_p, over the design temperature range, are:
    $0.99 \le H_o \le 1.01$
    $52.1\ MHz \le (\omega_p/2\pi) \le 54.8\ MHz$
    $1.63 \le Q_p \le 1.79$
13. Based on the results in #10 and #12, we can conclude that:
    — The DC gain and cutoff frequency change little with component value and temperature changes
    — Q_p has the greatest sensitivity to fabrication changes
    — The greatest filter response variation is in the peaking near the cutoff frequency

Figure 3 shows the results of a Monte-Carlo simulation at room temperature, with 100 cases simulated. These simulations used the "Standard Values" of the components. The gain curves are:

1. Lower 3-sigma limit (mean minus 3 times the standard deviation)
2. Mean value

Design Example (Continued)

3. Upper 3-sigma limit (mean plus 3 times the standard deviation)

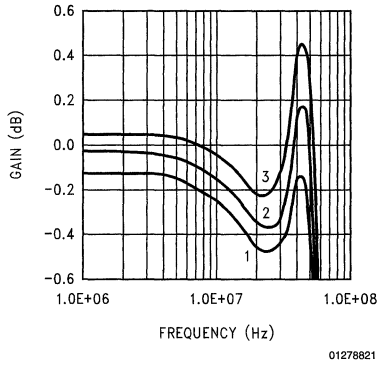

FIGURE 3. Monte-Carlo Simulation Results

SPICE Models

SPICE models are available for most of Comlinear's amplifiers. These models support nominal DC, AC, AC noise and transient simulations at room temperature.

We recommend simulating with Comlinear's SPICE models to:

- Predict the op amp's influence on filter response
- Support quicker design cycles

Include board and component parasitic models to obtain a more accurate prediction of the filter's response.

To verify your simulations, we recommend bread-boarding your circuit.

Summary

This Application Note contains an easy to use design algorithm for a low sensitivity, Sallen-Key lowpass biquad, which works for $Q_p < 5$. It also shows the basics of evaluating filter sensitivity performance.

Designing for low ω_p and Q_p sensitivities gives:

- Reduced filter variation over process, temperature and time
- Higher manufacturing yield
- Lower component cost

A low sensitivity design is not enough to produce high manufacturing yields. The nominal design must also compensate for any component parasitics, board parasitics, and op amp bandwidth (see Comlinear's Application Note on filter component pre-distortion [5]). The components must also have low enough tolerance and temperature coefficients.

Appendix A

Sensitivity Analysis Overview

The classic logarithmic sensitivity function is:

$$S_{\alpha_i}^{X} = \frac{\partial(\ln X)}{\partial(\ln \alpha_i)}; \quad \alpha_i, X \neq 0$$

$$= \frac{\alpha_i}{X} \cdot \frac{\partial X}{\partial \alpha_i}$$

$$\approx \frac{\Delta X / X}{\Delta \alpha_i / \alpha_i}$$

where α_i is a component value, and X is a filter performance measure (in the most general case, this is a complex-value function or frequency). The sensitivity function is a dimensionless figure of merit used in filter design.

We can approximate the relative change in X caused by the relative changes in the components α_i as:

$$\frac{\Delta X}{X} \approx \sum_i S_{\alpha_i}^{X} \cdot \frac{\Delta \alpha_i}{\alpha_i}$$

where:

$$\alpha_i, X \neq 0$$

$$\left|\frac{\Delta \alpha_i}{\alpha_i}\right|, \left|\frac{\Delta X}{X}\right| << 1$$

The relative standard deviation of X is calculated using:

$$\left(\frac{\sigma_X}{X}\right)^2 \approx \sum_i \left(\left|S_{\alpha_i}^{X}\right| \cdot \frac{\sigma_{\alpha_i}}{\alpha_i}\right)^2$$

where:

- The summation is over all component values (α_i) that affect X
- All component values (α_i) are physically independent (no statistical correlation)

Appendix A (Continued)

The nominal value of X is a function of temperature

$$X(T) = X\left(1 + \frac{X(T) - X}{X}\right)$$

$$\approx X\left(1 + \sum_i \left(S_{\alpha_i}^X \cdot \frac{\alpha_i(T) - \alpha_i}{\alpha_i}\right)\right)$$

where:

- X is the nominal value of X at room temperature
- α_i (T) is the nominal value of α_i at temperature T
- X(T) is the nominal value of X at temperature T

To help reduce variation in filter performance:

- Reduce the sensitivity function magnitudes ($\left|S_{\alpha_i}^X\right|$), where X is H_o, ω_p and Q_p, and α_i is any of the component values, the gain K, or operating conditions (such as temperature or supply voltage)
- Use components with smaller tolerances
- Use components with lower temperature coefficients

Appendix B

Handy Sensitivity Formulas

Notation:

1. k, m, n = constants
2. α, β = [non-zero] component parameters
3. X, Y = [non-zero] performance measures

Formulas:

1. $S_\alpha^{k\alpha^n} = n$
2. $S_\alpha^{kX} = S_{k\alpha}^X = S_\alpha^X$
3. $S_{\alpha^k}^{X^m Y^n} = \frac{m}{k} \cdot S_\alpha^X + \frac{n}{k} \cdot S_\alpha^Y$
4. $S_\alpha^X = 1/S_X^\alpha$
5. $S_\alpha^{Y(X(\alpha))} = S_X^Y S_\alpha^X$
6. $S_\gamma^{X(\alpha,\beta)} = S_\alpha^X S_\gamma^\alpha + S_\beta^X S_\gamma^\beta$
7. $S_\alpha^X = \mathrm{Re}\left(S_\alpha^X\right) + j\,\mathrm{Im}\left(S_\alpha^X\right)$

   where:

   $$\mathrm{Re}\left(S_\alpha^X\right) = S_\alpha^{|X|}$$

   $$\mathrm{Im}\left(S_\alpha^X\right) = \arg(X) \cdot S_\alpha^{\arg(X)} = \alpha \cdot \frac{\partial(\arg(X))}{\partial(\alpha)}$$

Appendix C

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Low-Sensitivity, Bandpass Filter Design with Tuning Method

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Introduction

This Application Note covers the design of a Sallen-Key bandpass biquad. It gives a design with low component and op amp sensitivities. Then it gives a filter tuning method to compensate for parasitics. A design example illustrates these methods. These biquads are also called KRC or VCVS [voltage-controlled, voltage-source].

Changes in component values over process, environment and time affect the performance of a filter. To achieve a greater production yield, the filter needs to be insensitive to these changes. This Application Note presents a design algorithm that results in low sensitivity to component variation. See [6] for information on evaluating the sensitivity performance of your filter.

To achieve the best production yield, the nominal filter design must also compensate for component and board parasitics. This Application Note gives a method to empirically tune your filter. See [5, 7] for the background theory.

Filter Tuning Overview

This section shows a simple tuning method that compensates for the parasitic elements in your filter.

To minimize the impact of parasitics:

- Keep signal paths as short as possible
- Minimize the length of all feedback loops
- Use components with small parasitics
- Use good PCB layout techniques
- Use an op amp with adequate bandwidth ($f_{3\ dB}$) and slew rate (SR):

  $f_{3\ dB} \geq 10\ f_H$

  $SR > 5\ f_H\ V_{PEAK}$

  where f_H is the highest frequency in the passband of the filter, and V_{PEAK} is the largest peak voltage. Make sure the op amp is stable at the chosen gain.

To compensate for the parasitic elements:

1. Start with a low sensitivity, low parasitic design
2. Calculate the sensitivities of the filter response parameters to the resistors and capacitors [6]
3. Measure the filter's response. The important parameters to extract are:
   - — Maximum passband gain (H_p)
   - — Pole frequency (ω_p)
   - — Pole quality (Q_p)

   The *Design Example* section gives a simple extraction method. Use accurate component values for the prototype filter so that the nominal design point will be near the center of the possible component values
4. Use the information in steps 2 and 3 to adjust the resistor and capacitor values:
   - — Set up the linear equations relating the relative change in filter response parameters ($\Delta H_p/H_p$, $\Delta\omega_p/\omega_p$ and $\Delta Q_p/Q_p$) to the relative change in the components to be adjusted
   - — The number of components to change is the same as the number of filter response parameters
   - — The coefficients of these linear equations are the component sensitivities [6]
   - — Solve for the relative change in component values
   - — Calculate the new component values
5. Repeat steps 3 and 4 until the nominal response is close enough to the desired response.

KRC Bandpass Biquad Design

The biquad shown in *Figure 1* is a Sallen-Key bandpass biquad. V_{IN} needs to be a voltage source with low output impedance.

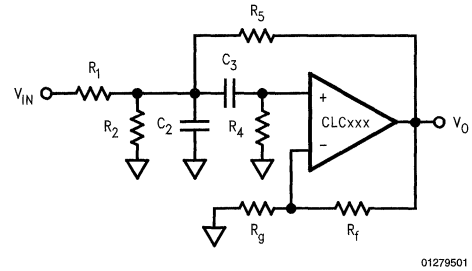


FIGURE 1. Bandpass Biquad

R_2 attenuates the input signal for low gains. V_{IN}, R_1 and R_2 can be replaced with their Thévenin equivalent voltage (αV_{IN}) and impedance (R_{12}):

$\alpha = R_2/(R_1 + R_2)$

$R_{12} = R_1 \parallel R_2$

The transfer function is:

$$\frac{V_O}{V_{IN}} \approx \frac{H_p(\omega_p/Q_p)s}{s^2 + (\omega_p/Q_p)s + (\omega_p^2)}, \quad s = j\omega$$

where:

$$\omega_p/Q_p = \left(\frac{1}{R_{12}} + \frac{1}{R_4} - \frac{K-1}{R_5}\right) \cdot \frac{1}{C_2} + \frac{1}{R_4 C_3}$$

$$\omega_p^2 = \frac{1}{R_4 C_2 C_3}\left(\frac{1}{R_{12}} + \frac{1}{R_5}\right)$$

$$K = 1 + R_f/R_g$$

$$H_p = \frac{\alpha K}{R_{12} C_2} \cdot \frac{Q_p}{\omega_p}$$

KRC Bandpass Biquad Design

(Continued)

To achieve low sensitivities, use this design algorithm:

1. Use this biquad when:

   $$0.5 \le Q_p < 50$$

   Steps 2 and 3 assume this condition to be true.

2. Partition the gain:
   - — Use a low noise amplifier before this biquad if you need a large gain
   - — Initialize the peak passband gain in 1 of 3 ways:
   - — For the best sensitivity performance, use:

     $$H_p \approx 1.0$$

   - — For reasonable sensitivity performance and reduced component spreads, use:

     $$H_p \approx \max\{1.0, Q_p\}$$

   - — For dynamic range performance, scale H_p as needed. Limit the peak gain to:

     $$H_p < 10.0$$

3. Set the input attenuation:

   $$\alpha = \min\{1.0, H_p\}$$

4. Initialize one of the resistor spreads ($r^2 = R_{12}/R_4$) and the op amp gain (K):

   $$A_1 = 0.0381Q_p^{1.51}(H_p/\alpha)^{-1.27}$$

   $$A_2 = 0.00206Q_p^{-1.92}(H_p/\alpha)^{1.39}$$

   $$r^2 \approx \max\{0.1, A_1 + A_2\}$$

   $$B_1 = 0.456(\max\{1, Q_p\})^{-1.22}(H_p/\alpha)^{1.22}$$

   $$B_2 = 0.0260(\max\{1, Q_p\})^{1.76}(H_p/\alpha)^{-1.51}$$

   $$K \approx 1.0 + \max\{0.1, B_1 + B_2\}$$

5. Select an op amp with adequate bandwidth ($f_{3\,dB}$) and slew rate (SR):

   $$f_{3\,dB} \ge 10\, f_H$$

   $$SR > 5\, f_H\, V_{PEAK}$$

   where f_H is the highest frequency in the passband, and V_{PEAK} is the largest peak voltage. Make sure the op amp is stable at a gain of $A_v = K$.

6. For current-feedback op amps, use the recommended value of R_f for a gain of $A_v = K$. For voltage-feedback op amps, select R_f for noise and distortion performance. Then set R_g for the correct gain:

   $$R_g = R_f/K - 1)$$

7. Calculate the capacitor spread ($c^2 = C_2/C_3$), and the other resistor spread ($\beta^2 = R_{12}/R_5$):

   $$A_0 = (K - 1)(\alpha K Q_p/H_p)^2$$

   $$A_1 = r^2 + K(1 - \alpha/H_p)$$

   $$c^2 = \frac{1}{r^2} \cdot \frac{2A_0}{A_1 + \sqrt{A_1^2 + 4A_0}}$$

   $$\beta^2 = \left(\frac{\alpha K Q_p}{H_p}\right)^2 \left(\frac{1}{c^2 r^2}\right) - 1$$

8. Initialize the resistance level ($R = \sqrt{R_{12} R_4}$).
   Increasing R will:
   - — Increase the output noise
   - — Improve the distortion performance
   - — Improve the isolation between the op amp outputs and C_2 and C_3
   - — Make the parasitic capacitances a larger fraction of C_2 and C_3

9. Calculate the capacitance level ($C = \sqrt{C_2 C_3}$):

   $$C = \sqrt{1 + \beta^2}/(\omega_p R)$$

10. Calculate the resistors and capacitors:

    $R_{12} = rR$

    $R_1 = R_{12}/\alpha$

    $R_2 = R_{12}/(1 - \alpha)$

    $R_4 = R/r$

    $R_5 = R_{12}/\beta^2$

    $C_2 = cC$

    $C_3 = C/c$

11. Set the resistors and capacitors to the nearest standard values.

The component sensitivity formulas are in the table below. The sensitivities to $\alpha_i = K$ are a measure of this biquad's sensitivity to the op amp group delay [5]. To evaluate this biquad's sensitivity performance, see [6]. To manually pre-distort this filter, and compensate for parasitic capacitances, see [5] and [7].

α_i	$S_{\alpha_i}^{H_p}$	$S_{\alpha_i}^{\omega_p}$	$S_{\alpha_i}^{Q_p}$
R_1	$\frac{H_p}{K} - 1$	$\frac{-\alpha}{2(1+\beta^2)}$	$S_{R_1}^{H_p} + S_{R_1}^{\omega_p} + 1$
R_2	$\frac{(1-\alpha)H_p}{\alpha K}$	$\frac{-(1-\alpha)}{2(1+\beta^2)}$	$S_{R_2}^{H_p} + S_{R_2}^{\omega_p}$
R_4	$\frac{H_p(1+c^2)r^2}{\alpha K}$	$-\frac{1}{2}$	$S_{R_4}^{H_p} + S_{R_4}^{\omega_p}$
R_5	$\frac{-H_p(K-1)\beta^2}{\alpha K}$	$\frac{-\beta^2}{2(1+\beta^2)}$	$S_{R_5}^{H_p} + S_{R_5}^{\omega_p}$
C_2	$\frac{-H_p c^2 r^2}{\alpha K}$	$-\frac{1}{2}$	$S_{C_2}^{H_p} + S_{C_2}^{\omega_p} + 1$
C_3	$-S_{C_2}^{H_p}$	$-\frac{1}{2}$	$-S_{C_2}^{Q_p}$
R_f	$\left(\frac{H_p\beta^2}{\alpha} + 1\right) \cdot \frac{K-1}{K}$	0	$S_{R_f}^{H_p} + S_{R_f}^{\omega_p} - \frac{K-1}{K}$
R_g	$-S_{R_f}^{H_p}$	0	$-S_{R_f}^{Q_p}$
K	1	0	$\frac{H_p\beta^2}{\alpha}$

KRC Bandpass Biquad Tuning Method

To tune this filter, use this algorithm:

1. Start with a low-sensitivity design.
2. Calculate the sensitivities of H_p, ω_p and Q_p to the components.

KRC Bandpass Biquad Tuning Method (Continued)

3. Set up the linear equations:
   — Choose the 3 components α_i that will be changed to adjust H_P, ω_p and Q_p
   — Create this sensitivity matrix using the formulas (see *Appendix A* for a simple method that uses measurement or simulation results):

$$M_3 = \begin{bmatrix} S_{\alpha_1}^{H_p} & S_{\alpha_2}^{H_p} & S_{\alpha_3}^{H_p} \\ S_{\alpha_1}^{\omega_p} & S_{\alpha_2}^{\omega_p} & S_{\alpha_3}^{\omega_p} \\ S_{\alpha_1}^{Q_p} & S_{\alpha_2}^{Q_p} & S_{\alpha_3}^{Q_p} \end{bmatrix}$$

   — Invert the sensitivity matrix (M_3^{-1})
4. Measure the filter response, and then extract H_p, ω_p and Q_p:
   — Find the maximum gain magnitude:

$$H_p = \max\{|H(j\omega)|\}$$

   — Find the –3 dB corner frequencies f_1 and f_2, where $f_2 > f_1$
   — Calculate ω_p and Q_p:

$$\omega_p = 2\pi\sqrt{f_1 f_2}$$

$$Q_p = \sqrt{f_1 f_2}/(f_2 - f_1)$$

5. Calculate the needed changes in H_p, ω_p and Q_p (X):

$$\Delta X/X = 1 - X_{meas}/X_{nom}$$

where X_{nom} and X_{meas} are the nominal and measured values of X. Limit the relative changes in X:

$$\Delta X/X \leftarrow \max\{-0.5, \min\{1.0, \Delta X/X\}\}$$

6. Calculate the needed component values:
   — Estimate the relative changes in α_i, and then limit them:

$$\begin{bmatrix} \Delta\alpha_1/\alpha_1 \\ \Delta\alpha_2/\alpha_2 \\ \Delta\alpha_3/\alpha_3 \end{bmatrix} = M_3^{-1} \cdot \begin{bmatrix} \Delta H_p/H_p \\ \Delta\omega_p/\omega_p \\ \Delta Q_p/Q_p \end{bmatrix}$$

$$\frac{\Delta\alpha_i}{\alpha_i} \leftarrow \max\left\{-0.5, \min\left\{1.0, \frac{\Delta\alpha_i}{\alpha_i}\right\}\right\}$$

   — Calculate the new α_i:

$$\alpha_i \leftarrow \alpha_i(1 + \Delta\alpha_i/\alpha_i)$$

   — Change the filter components to these new values; *use accurate component values when building the prototype filter* so that the nominal design point will be near the center of the possible component values
7. Repeat steps 4–6 until the nominal response is close enough to the desired response.

Design Example

The circuit shown in *Figure 2* is a 4th-order bandpass filter. This filter cascades two bandpass biquads: sections A and B. Use a voltage source with low output impedance, such as the CLC111 buffer, for V_{IN}.

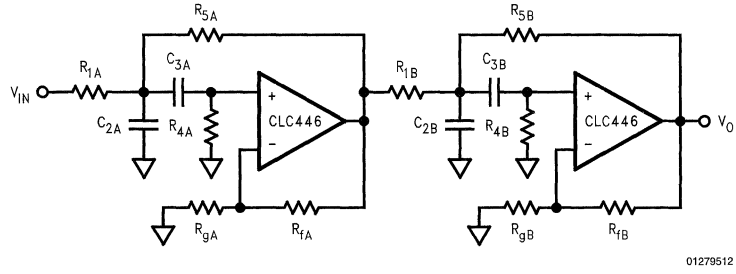


FIGURE 2. Bandpass Filter

The nominal filter specifications are:

f_{sl} = 15 MHz (lower stopband edge frequency)
f_{cl} = 40 MHz (lower passband edge frequency)
f_{cu} = 60 MHz (upper passband edge frequency)
f_{su} = 135 MHz (upper stopband edge frequency)
A_p = 3.0 dB (maximum passband ripple)
A_s = 30 dB (minimum stopband attenuation)
H_p = 0 dB (passband voltage gain)

Design Example (Continued)

The 2nd-order Butterworth lowpass prototype filter meets these specifications [1–4]. The H_p values shown below give a maximum gain of 1 00 from V_{IN} to each biquad output The transformed filter is:

Section		A	B
$\omega_p/2\pi$	[MHz]	42.36	56.65
Q_p	[ ]	3.501	3.501
H_p	[V/V]	1.000	2.043

Overall Design:

1. Restrict the resistor and capacitor ratios to.
$$0.1 \le c^2, r^2, \beta^2 \le 10$$
2. Use 1% resistors (chip metal film, 1206 SMD)
3 Use 5% capacitors (ceramic chip, 1206 SMD)
4 Use standard resistor and capacitor values
5. Use the same H_p in both sections to simplify the design Also set the overall gain to 1.00:
$$H_p = \sqrt{(1.000)(2.043)} = 1.429$$

Section A Design:

1. Q_p (3.501) meets the required limits
2. H_p (1.429) is between the first two criteria in step 2 of the design algorithm; the sensitivity performance and component spreads should be reasonable
3. Initialize α to 1.00; R_{2A} is an open circuit
4. Initialize r^2 & K:
   $A_1 = 0.1606 \quad A_2 = 0.0003$
   $r^2 = 0\ 1609$
   $B_1 = 0.1528 \quad B_2 = 0.1376$
   K = 1.290
5 The CLC446 is a current-feedback op amp:
   — $f_{3\ dB} = 400$ MHz < 10 $f_H = 600$ MHz ($f_{H\ =\ f_{cu}}$); the op amp strongly affects the filter
   — SR = 2000 V/µs, while a 60 MHz, 2 V_{pp} sinusoid requires more than 300 V/µs
6. Set R_{fA} to the CLC446's recommended R_f at A_V = +1.290, then calculate R_{gA}:
   $R_{fA} = 392\Omega$
   $R_{gA} = R_{fA}/(K - 1) = 1352\Omega$
7. Calculate c^2 and β^2:
   $A_0 = 2.897 \quad A_1 = 0.5482$
   $c^2 = 9.011$
   $\beta^2 = 5.889$
8. Initialize R = 300Ω
9. Calculate C:
$$C = \frac{\sqrt{1 + 5.889}}{2\pi(42.36\ \text{MHz}) \cdot (300\Omega)} = 32.87\ \text{pF}$$
10. The initial values are in the table below

Section B Design:

H_p and Q_p are the same as in section A, but ω_p is different. To change the pole frequency, scale the resistors R_{1B}, R_{4B} and R_{5B}:

$$R_{xB} \leftarrow R_{xA} \bullet (\omega_{pA}/\omega_{pB}) = R_{xA} \bullet 0.7477$$

The initial component values are:

Component		Initial Value	
		Section A	Section B
R_1	[Ω]	120	90 0
R_4	[Ω]	748	559
R_5	[Ω]	20.4	15.3
C_2	[pF]	98.7	98 7
C_3	[pF]	11.0	11.0
R_f	[Ω]	392	392
R_g	[Ω]	1352	1352

Filter Tuning:

This section uses simulated results; different layout and component parasitics will change the tuning results. Simulations used the following parasitics:

- 0.2 pF across all resistors
- 1.0 pF to ground at CLC446 non-inverting inputs
- A group delay of 0.56 ns for the CLC446 at 50 MHz, using a good simulation model

1. The sensitivities for sections A and B are equal since they are not functions of ω_p. They are:

α_i	H_p S_{α_i}	ω_p S_{α_i}	Q_p S_{α_i}
R_1	0.11	–0.07	1.04
R_4	1 78	–0.50	1.28
R_5	–1.89	–0.43	–2.32
C_2	–1.61	–0.50	–1.11
C_3	1.61	–0.50	1.11
R_f	2.12	0.00	1.89
R_g	–2.12	0.00	–1.89
K	1.00	0.00	8.42

2. To tune the filter, change R_1, R_4 and R_g:
$$\begin{bmatrix} \Delta R_1/R_1 \\ \Delta R_4/R_4 \\ \Delta R_g/R_g \end{bmatrix} = M_3^{-1} \cdot \begin{bmatrix} \Delta H_p/H_p \\ \Delta\omega_p/\omega_p \\ \Delta Q_p/Q_p \end{bmatrix}$$

where:

$$M_3 = \begin{bmatrix} 0.11 & 1.78 & -2.12 \\ -0.07 & -0.50 & 0.00 \\ 1.04 & 1.28 & -1.89 \end{bmatrix}$$

$$M_3^{-1} = \begin{bmatrix} -0.91 & -0.62 & 1.02 \\ 0.13 & -1.91 & -0.14 \\ -0.41 & -1.64 & -0.07 \end{bmatrix}$$

Design Example (Continued)

3. The results of tuning section A are:

Iteration #		1	2	3	4
R_1	[Ω]	120	98.7	89.3	90.8
R_4	[Ω]	748	496	488	492
R_g	[Ω]	1352	676	708	700
H_p	[V/V]	0.736	1.625	1.373	1.433
$\omega_p/2\pi$	[MHz]	34.62	41.76	42.57	42.32
Q_p	[ ]	2.212	4.226	3.335	3.504
$\Delta H_p/H_p$	[%]	48.5	−13.7	3.92	−0.28
$\Delta\omega_p/\omega_p$	[%]	18.3	1.42	−0.50	0.09
$\Delta Q_p/Q_p$	[%]	36.8	−20.7	4.74	−0.09
$\Delta R_1/R_1$	[%]	−17.9	−9.52	1.58	—
$\Delta R_4/R_4$	[%]	−33.8	−1.59	0.79	—
$\Delta R_g/R_g$	[%]	−50.0	4.75	−1.13	—

4. The results of tuning section B are:

Iteration #		1	2	3	4
R_1	[Ω]	90.0	66.5	62.9	63.3
R_4	[Ω]	559	363	357	360
R_g	[Ω]	1352	740	784	779
H_p	[V/V]	0.993	1.663	1.384	1.428
$\omega_p/2\pi$	[MHz]	45.66	55.94	56.95	56.62
Q_p	[ ]	3.029	4.174	3.391	3.496
$\Delta H_p/H_p$	[%]	30.5	−16.4	3.15	0.07
$\Delta\omega_p/\omega_p$	[%]	19.4	1.25	−0.53	0.05
$\Delta Q_p/Q_p$	[%]	13.5	−19.2	3.14	0.14
$\Delta R_1/R_1$	[%]	−26.1	−5.48	0.67	—
$\Delta R_4/R_4$	[%]	−35.0	−1.83	0.98	—
$\Delta R_g/R_g$	[%]	−45.3	6.00	−0.64	—

Figures 3 and 4 show the simulated filter gain. The curve numbers are:

1. The ideal gain
2. The gain for the initial design (Iteration 1)
3. The gain for the tuned filter (Iteration 4)

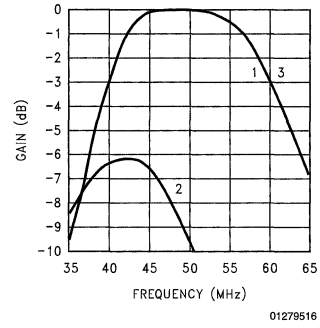


FIGURE 3. Simulated Filter Magnitude Response

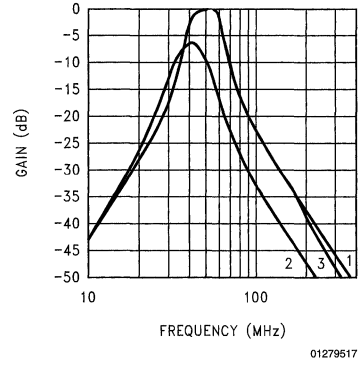


FIGURE 4. Simulated Filter Magnitude Response

The final standard component values are:

Component		Standard Tuned Value	
		Section A	Section B
R_1	[Ω]	90.9	63.4
R_4	[Ω]	487	357
R_5	[Ω]	20.5	15.4
C_2	[pF]	100	100
C_3	[pF]	11	11
R_f	[Ω]	392	392
R_g	[Ω]	698	787

SPICE Models

SPICE models are available for most of Comlinear's amplifiers. These models support nominal DC, AC, AC noise and transient simulations at room temperature.

We recommend simulating with Comlinear's SPICE models to:

- Predict the op amp's influence on filter response
- Support quicker design cycles

Include board and component parasitic models to obtain a more accurate prediction of the filter's response.

To verify your simulations, we recommend bread-boarding your circuit.

Summary

This Application Note contains an easy to use design algorithm for a low sensitivity, Sallen-Key bandpass biquad. Designing for low H_p, ω_p and Q_p sensitivities gives:

- Reduced filter variation over process, temperature and time
- Higher manufacturing yield
- Lower component cost

A low sensitivity design is not enough to produce high manufacturing yields. This Application Note shows how to tune the filter to compensate for parasitics; no assumptions about the parasitics are necessary. The components must also have low tolerance, small parasitics and low temperature coefficients.

Appendix A

Estimating the Sensitivity Matrix

For filters where the sensitivity formulas are not readily available, this appendix gives a simple method to estimate the entries in the sensitivity matrix.

To estimate the sensitivity matrix entries using measurement or simulation results, use this algorithm:

1. Choose the 3 components α_i that will be changed to adjust H_p, ω_p and Q_p (X)
2. Calculate the sensitivities of H_p, ω_p and Q_p to the chosen components:
   - — Extract the parameters H_p, ω_p and Q_p at the nominal values of α_i
   - — Extract the parameters H_p, ω_p and Q_p when only one α_i is different from its nominal value; this results in 3 sets of 3 modified performance parameters
   - — Estimate the sensitivities (X is H_p, ω_p or Q_p):

$$S_{\alpha_1}^{X} \approx \frac{\Delta X}{X} \cdot \frac{\alpha_1}{\Delta \alpha_1}\Bigg|_{\Delta\alpha_2 = \Delta\alpha_3 = 0}$$

$$S_{\alpha_2}^{X} \approx \frac{\Delta X}{X} \cdot \frac{\alpha_2}{\Delta \alpha_2}\Bigg|_{\Delta\alpha_1 = \Delta\alpha_3 = 0}$$

$$S_{\alpha_3}^{X} \approx \frac{\Delta X}{X} \cdot \frac{\alpha_3}{\Delta \alpha_3}\Bigg|_{\Delta\alpha_1 = \Delta\alpha_2 = 0}$$

3. From the sensitivity matrix:

$$M_3 = \begin{bmatrix} S_{\alpha_1}^{H_p} & S_{\alpha_2}^{H_p} & S_{\alpha_3}^{H_p} \\ S_{\alpha_1}^{\omega_p} & S_{\alpha_2}^{\omega_p} & S_{\alpha_3}^{\omega_p} \\ S_{\alpha_1}^{Q_p} & S_{\alpha_2}^{Q_p} & S_{\alpha_3}^{Q_p} \end{bmatrix}$$

4 Invert the sensitivity matrix (M_3^{-1})

Example:

As an example, suppose that the following measurements result from the 4 conditions in Step 2 (italicized numbers are changed from nominal):

Condition #		1	2	3	4
R_1	[Ω]	120	*115*	120	120
R_4	[Ω]	748	748	*715*	748
R_g	[Ω]	1352	1352	1352	*1300*
H_p	[V/V]	0.736	*0.729*	*0.681*	*0.792*
$\omega_p/2\pi$	[MHz]	34.62	*34.84*	*35.51*	*34.54*
Q_p	[ ]	2.212	*2.110*	*2.096*	*2.368*

where the Condition # means:

1. Nominal values
2. $\Delta R_1 \neq 0$, and $\Delta R_2 = \Delta R_3 = 0$
3. $\Delta R_2 \neq 0$, and $\Delta R_1 = \Delta R_3 = 0$
4. $\Delta R_3 \neq 0$, and $\Delta R_1 = \Delta R_2 = 0$

The sensitivity of H_p to R_1 is estimated as:

$$S_{R_1}^{H_p} = \frac{0.729 - 0.736}{0.736} \cdot \frac{120}{115 - 120} \approx 0.23$$

Estimating the other sensitivities produces these sensitivity matrices:

$$M_3 \approx \begin{bmatrix} 0.23 & 1.69 & -1.98 \\ -0.15 & -0.58 & 0.06 \\ 1.11 & 1.19 & -1.83 \end{bmatrix}$$

$$M_3^{-1} \approx \begin{bmatrix} -0.95 & -0.70 & 1.00 \\ 0.20 & -1.70 & -0.27 \\ -0.45 & -1.53 & -0.11 \end{bmatrix}$$

Appendix B

Bibliography

[1] R. Schaumann, M. Ghausi and K. Laker, *Design of Analog Filters: Passive, Active RC, and Switched Capacitor.* New Jersey: Prentice Hall, 1990.

[2] A. Zverev, *Handbook of FILTER SYNTHESIS.* John Wiley & Sons, 1967.

[3] A. Williams and F. Taylor, *Electronic Filter Design Handbook.* McGraw Hill, 1995.

[4] S. Natarajan, *Theory and Design of Linear Active Networks.* Macmillan, 1987.

[5] K. Blake, "Component Pre-distortion for Sallen-Key Filters," *Comlinear Application Note*, OA-21, Rev. B, July 1996.

[6] K. Blake, "Low-Sensitivity, Lowpass Filter Design," *Comlinear Application Note*, OA-27, July 1996.

[7] K. Blake, "Low-Sensitivity, Highpass Filter Design with Parasitic Compensation," *Comlinear Application Note*, OA-29, Oct. 1996.

Note: The circuits included in this application note have been tested with National Semiconductor parts that may have been obsoleted and/or replaced with newer products. Please refer to the CLC to LMH conversion table to find the appropriate replacement part for the obsolete device.

Low-Sensitivity, Highpass Filter Design with Parasitic Compensation

National Semiconductor
OA-29
Kumen Blake

Introduction

This Application Note covers the design of a Sallen-Key highpass biquad. This design gives low component and op amp sensitivities. It also shows how to compensate for the op amp's bandwidth (pre-distortion) and parasitic capacitances. A design example illustrates this method. These biquads are also called KRC or VCVS [voltage-controlled, voltage-source]

Changes in component values over process, environment and time affect the performance of a filter. To achieve a greater production yield, the filter needs to be insensitive to these changes. This Application Note presents a design algorithm that results in low sensitivity to component variation. See [6] for information on evaluating the sensitivity performance of your filter.

To achieve the best production yield, the nominal filter design must also compensate for component and board parasitics. The components are pre-distorted [5] to compensate for the op amp bandwidth. This Application Note expands the pre-distortion method in [5] to include compensation for parasitic capacitances. This method is valid for either voltage-feedback or current-feedback op amps.

Parasitic Compensation

To pre-distort your filter components and compensate for parasitic capacitances:

1. Use the method in [5] to include the op amp's effect on the filter response. The result is a transfer function of the same order whose coefficients include the op amp group delay (τ_{oa}) evaluated at the passband edge frequency (f_c)
2. For all parasitic capacitances in parallel with capacitors:
   - — Add the capacitors together
   - — Simplify the resulting coefficients
   - — Use the sum of time constants form for the coefficients when possible
3. For all parasitic capacitances in parallel with resistors:
   - — Replace the resistor R_x in the filter transfer function with the parallel equivalent of R_x and C_p.

$$\frac{R_x \leftarrow R_x}{(1+R_xC_ps)}, s = j\omega$$

   - — Alter this impedance to a convenient form and simplify:
   - — *Do not create new terms* (a coefficient times a new power of s) in the transfer function *after simplifying*
   - — The most useful approximations are:

$$\frac{R_x}{(1+R_xC_ps)} \approx R_x(1-R_xC_ps)$$

$$\approx R_x e^{-R_xC_ps}$$

These approximations are valid when:

$$\frac{\omega << 1}{(R_xC_p)}$$

   - — Convert $(1 + R_xC_ps)$ to the exponential form (a pure time delay) when it multiplies, or divides, the entire transfer function
   - — Do not change the gain at $\omega \approx \omega_p$ in allpass sections
   - — When simplifying, discard any terms that are products of the error terms ($k\tau_{oa}$ and R_xC_p); they are negligible
   - — Use the sum of time constants form for the coefficients when possible

Use an op amp with adequate bandwidth (f_{3dB}) and slew rate (SR):

$$f_{3dB} \geq 10f_H$$

$$SR > 5f_HV_{peak}$$

where f_H is the highest frequency in the passband of the filter, and V_{peak} is the largest peak voltage. This increases the accuracy of the pre-distortion algorithm. It also reduces the filter's sensitivity to op amp performance changes over temperature and process. Make sure the op amp is stable at a gain of $A_V = K$.

KRC Highpass Biquad Design

The biquad shown in *Figure 1* is a Sallen-Key highpass biquad. V_{in} needs to be a voltage source with low output impedance.

The transfer function is:

$$\frac{V_o}{V_{in}} \approx \frac{H_\infty\left(\frac{1}{\omega_p^2}\right)s^2}{1+\left(\frac{1}{(\omega_pQ_p)}\right)s+\left(\frac{1}{(\omega_p^2)}\right)s^2}$$

KRC Highpass Biquad Design

(Continued)

$$K = 1 + \frac{R_f}{R_g}$$

$$H_\infty = K$$

$$\frac{1}{(\omega_p Q_p)} = R_5C_1 + R_5C_3 - R_4C_3(K-1)$$

$$\frac{1}{\omega_p^2} = R_4R_5C_1C_3$$

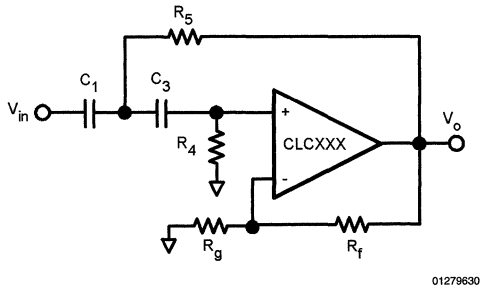


FIGURE 1. Highpass Biquad

To achieve low sensitivities, use this design algorithm:

1. Partition the gain for good Q_p sensitivity and dynamic range performance:
   — Use a low noise amplifier before this biquad if you need a large gain
   — Select K with this empirical formula:

$$K = \begin{cases} 1, & 0.1 \le Q_p \le 1.1 \\ \dfrac{2.2Q_p - 0.9}{Q_p + 0.2}, & 1.1 < Q_p < 5 \end{cases}$$

   These values also reduce the op amp bandwidth's impact on the filter response. This biquad's sensitivities are too high when $Q_p \ge 5$

2. Select an op amp with adequate bandwidth (f_{3dB}) and slew rate (SR):

$$f_{3dB} \ge f_H$$

$$f_{3dB} \ge 10f_c$$

$$SR > 5f_H V_{peak}$$

   where f_H is the highest signal frequency, f_c is the corner frequency of the filter, and V_{peak} is the largest peak voltage. Make sure the op amp is stable at a gain of $A_v = K$.

3. For current-feedback op amps, use the recommended value of R_f for a gain of $A_V = K$. For voltage-feedback op amps, select R_f for noise and distortion performance. Then set R_g for the correct gain:

$$R_g = \frac{R_f}{(K-1)}$$

4. Initialize the resistance level $\left(R = \sqrt{R_4R_5}\right)$.
   Increasing R will:
   — Increase the output noise
   — Reduce the distortion
   — Improve the isolation between the op amp outputs and C_1 and C_3
   — Make the parasitic capacitances a larger fraction of C_1 and C_3

5. Initialize the capacitance level $s_{\alpha_i}^{H_\infty}$, and the component ratios

$$\left(c^2 = \frac{C_3}{C_1} \text{ and } r^3 = \frac{R_5}{R_4}\right):$$

$$c = \frac{1}{(\omega_p R)}$$

$$c^2 = 0.10$$

$$r^2 = \max\left\{0.10, \left(\frac{1 + \sqrt{1 + 4Q_p^2}\left(1 + c^2\right)(K-1)}{2 \cdot Q_p \cdot \left(1 + c^2\right)/c}\right)\right.$$

6. Recalculate C^2 and initialize the capacitors:

$$c^2 = \left(\frac{2 \cdot r \cdot Q_p}{1 + \sqrt{1 + 4Q_p^2}\left(K - 1 - r^2\right)}\right)^2$$

$$C_1 = \frac{C}{c}$$

$$C_3 = cC$$

7. Set C_1 and C_3 to the nearest standard values.

KRC Highpass Biquad Design

(Continued)

8. Recalculate C, C^2, R and r^2:

$$C = \sqrt{C_1 C_3}$$

$$c^2 = \frac{C_3}{C_1}$$

$$R = \frac{1}{(\omega_p C)}$$

$$r^2 = \left(\frac{1 + \sqrt{1 + 4Q_p^2 (1 + c^2)(K-1)}}{2 \cdot Q_p \cdot (1 + c^2)/c} \right)^2$$

9. Calculate the resistors:

$$R_4 = \frac{R}{r}$$

$$R_5 = rR$$

The component sensitivity formulas are in the table below. The sensitivities formulas are in the table below. The sensitivities to $\alpha_1 = K$ are a measure of this biquad's sensitivity to the op amp group delay [5]. To evaluate this biquad is sensitivity performance, use the method in [6].

α_1	$S_{\alpha_1}^{H_{\infty}}$	$S_{\alpha_1}^{\omega_p}$	$S_{\alpha_1}^{Q_p}$
C_1	0	$-\frac{1}{2}$	$-\left(Q_p \frac{r}{c} - \frac{1}{2}\right)$
C_3	0	$-\frac{1}{2}$	$\left(Q_p \frac{r}{c} - \frac{1}{2}\right)$
R_4	0	$-\frac{1}{2}$	$\left((K-1)\ Q_p \frac{c}{r} + \frac{1}{2}\right)$
R_5	0	$-\frac{1}{2}$	$-\left((K-1)\ Q_p \frac{c}{r} + \frac{1}{2}\right)$
R_f	$\frac{K-1}{K}$	0	$\left((K-1)\ Q_p \frac{c}{r}\right)$
R_f	$-\frac{K-1}{K}$	0	$-\left((K-1)\ Q_p \frac{c}{r}\right)$
K	1	0	$\left(K\ Q_p \frac{c}{r}\right)$

KRC Highpass Biquad Parasitic Compensation

To pre-distort this biquad, and compensate for the [parasitic] non-inverting input capacitance of the op amp (C_{n_i}), do the following (see *Appendix A* for the derivation of the formulas):

1. Start the iterations by ignoring the parasitics:

$$\tau^2 = 0$$

$$\tau^2_4 = 0$$

2. Estimate the pre-distorted values of ω_p and Q_p ($\omega_{p(pd)}$ and $Q_{p(pd)}$ that will compensate for τ_{oa} and C_{n_i}:

$$\frac{\omega_{p(pd)} = \omega_{p(nom)}}{\sqrt{1 - \tau_4^2 \omega_{p(nom)}^2}}$$

$$\frac{Q_{p(pd)} = Q_{p(nom)}}{\left(\frac{\omega_{p(pd)}}{\omega_{p(nom)}} - Q_{p(nom)} \tau_2 \omega_{p(pd)} \right)}$$

Where $\omega_{p(nom)}$ and $Q_{p(nom)}$ are the nominal values of ω_p and Q_p

3 Recalculate the resistors and capacitors using $\omega_{p(pd)}$ and $Q_{p(pd)}$:

$$\frac{1}{\omega_{p(pd)}^2} = R_4 R_5 C_1 C_3$$

$$\frac{1}{(\omega_{p(pd)} Q_{p(pd)})} = R_5 C_1 + R_5 C_3 - R_4 C_3 (K-1)$$

The *Design Example* accomplishes this by recalculating R and r^2, then R_4 and R_5:

$$R = \frac{1}{(\omega_{p(pd)} C)}$$

$$r^2 = \left(\frac{1 + \sqrt{1 + 4Q_{p(pd)}^2 (1 + c^2)(K-1)}}{2 \cdot Q_{p(pd)} \cdot (1 + c^2)/c} \right)^2$$

$$R_4 = \frac{R}{r}$$

$$R_5 = rR$$

4. Calculate the resulting parasitic correction factors:

$$\tau^2 = R_4 C_{n_i}$$

$$\tau^2_4 = K \tau_{oa} R_4 C_3 + R_4 R_5 (C_1 + C_3) C_{n_i}$$

5 Calculate the resulting filter response parameters ω_p and Q_p

$$\frac{\omega_p = \omega_{p(pd)}}{\sqrt{1 + \tau_4^2 \omega_{p(pd)}^2}}$$

$$Q_p = \frac{Q_{p(pd)}}{\left(\frac{\omega_p}{\omega_{p(pd)}} + Q_{p(pd)} \tau_2 \omega_p \right)}$$

6. Repeat steps 2-5 until:

$$\omega_p = \omega_{p(nom)}$$

$$Q_p = Q_{p(nom)}$$

KRC Highpass Biquad Parasitic Compensation (Continued)

7. Estimate the high frequency gain:

$$\frac{H_\infty \approx K}{\left(1+\tau_4^2\omega_{p(pd)}^2\right)}$$

If this reduces the gain too much, then repartition the gain

Design Example

The circuit shown in *Figure 2* is a 3rd-order Butterworth highpass filter. Section A is a buffered single pole section, and Section B is a highpass biquad. Use a voltage source with low output impedance, such as the CLC111 buffer, for V_{in}:

The nominal filter specifications are:

f_c = 50MHz (passband edge frequency)
f_s = 10MHz (stopband edge frequency)
f_H = 200MHz (highest signal frequency)
A_p = 3.0dB (maximum passband ripple)
A_s = 40dB (minimum stopband attenuation)
H_∞ = 0dB (passband voltage gain)

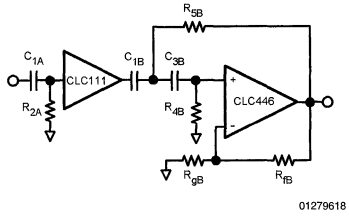


FIGURE 2. Highpass Filter

The 3rd-order Butterworth filter [1-4] meets our specifications. The pole frequencies and quality factors are:

Section	A	B
$\omega_p/2\pi$ [MHz]	50.00	50.00
Q_p [ ]	–	1.000

Overall Design

1. Restrict the resistor and capacitor ratios to:
2. $$0.1 \le c^2, r^2 \le 10$$
3. Use 1% resistors (chip metal film, 1206 SMD)
4. Use 5% capacitors (ceramic chip, 1206 SMD)
5. Use standard resistor and capacitor values

Section A Design and Pre-distortion:

1. Use the CLC111. This is a close-loop buffer.
   — f_{3dB} = 800MHz > f_H = 200MHz
   — f_{3dB}= 800MHz > $10f_c$= 500MHz
   — SR = 3500V/µs, while a 200MHz, $2V_{pp}$ sinusoid requires more than 100V/µs
   — $\tau_{oa} \approx$ 0.28ns at 10MHz
   — $C_{ni(111)}$ = 1.3pF (input capacitance)
2. Select R_{2A} for noise, distortion and to properly isolate the CLC111's output and C_{1A}. The pre-distorted value of R_{2A}, that also compensates for $C_{ni(111)}$, is [5]:

$$R_{2A} = \frac{\left(\frac{1}{\omega_p - \tau_{oa}}\right)}{\left(C_{1A}+C_{ni(111)}\right)}$$

The results are in the table below:

— The Initial Value column shows ideal values that ignore any parasitic effect
— The Adjusted Value column shows the component values that compensate for $C_{ni(111)}$ and CLC111 is group delay (τ_{oa})
— The Standard Value column shows the nearest standard 1% resistors and 5% capacitors

Component	Initial	Value Adjusted	Standard
C_{1A}	30pF	30pF	30pF
R_{2A}	106Ω	92.8Ω	93.1Ω
$C_{ni(111)}$	–	1.3pF	1 3pF

Section B Design:

1. Since Q_p = 1.000, set K_B to 1.00
2. Use the CLC446. This is a current-feedback op amp
   — f_{3dB} = 400MHz > f_H = 200MHz
   — f_{3dB} < $10f_c$ = 500MHz; the design will be sensitive to the op amp group delay
   — SR = 2000V/µs > 1000V/µs (see Item #1 in "Section A Design")
   — $\tau_{oa} \approx$ 0.56ns at 10MHz
   — $C_{ni(446)}$ = 1.0pF (input capacitance)
3. Use the CLC446's recommended R_f at A_v = 1.0:
   R_{fB} = 453Ω
   Then leave R_{gB} open so that K_B = 1.00
4. Initialize the resistor level:
   R ≈ 100Ω
5. Initialize the capacitor level, and the component ratios:

$$C \approx \frac{1}{2\pi(50.00\text{MHz})\cdot(100\Omega)} = 31.83\text{pF}$$

$$c^2 \approx 0.1000$$

$$r^2 \approx \max\{0.10, 0.0826\} = 0.1000$$

6. Recalculate C^2 and initialize the capacitors:
   $C^2 \approx 0.127$ $C_{1B} \approx 89.3$pF $C_{3B} \approx 11.3$pF
7. Set the capacitors to the nearest standard values:
   $C_{1B} \approx 91$pF $C_{3B} \approx 11$pF
8. Recalculate the capacitor level and ratio, and the resistor level and ratio:

Design Example (Continued)

9. Calculate the resistors:

$$R_{4B} = 324\Omega \quad R_{3B} = 31.2\Omega$$

10. The sensitivities for this design are:

$$C = \sqrt{(91pF)\ (11pF)} = 31.64pF$$

$$c^2 = \frac{(11pF)}{(91pF)} = 0.1209$$

$$R = \frac{1}{2\pi(50.00MHz)\cdot(31.64pF)}$$

$$= 100.6\Omega$$

$$r^2 = 0.1056$$

αi	$S_{\alpha_i}^{H_\infty}$	$S_{\alpha_i}^{\omega_p}$	$S_{\alpha_i}^{Q_p}$
C_{1B}	0.00	−0.50	−0.39
C_{3B}	0.00	−0.50	0.39
R_{4B}	0.00	−0.50	0.50
R_{5B}	0.00	−0.50	−0.50
R_{fB}	0.00	0.00	0.00
R_{gB}	0.00	0.00	0.00
K	1.00	0.00	1.12

Section B Pre-distortion:

1. The design gives these values:

$\omega_{p(nom)} = 2\pi(50.00MHz)$

$Q_{p(nom)} = 1.000$

$K_B = 1\ 00$

$C_{1B} = 91pF$

$C_{3B} = 11pF$

2. Iteration 1 shows the initial design results. Iterations 2-4 pre-distort R_{4B} and R_{5B} to compensate for the CLC446's group delay, and for $C_{ni(446)}$:

Iteration #		1	2	3	4
$\frac{\omega_{p(pd)}}{2\pi}$	[MHz]	50.00	59.73	56.81	57.54
$Q_{p(pd)}$	[ ]	1.000	0.9320	0 9561	0.9505
R	[Ω]	10.6	84.22	88.54	87.42
r^2	[Ω]	0.0962	0.1108	0.1053	0.1065
R_{4B}	[Ω]	324.3	253.0	272.9	267.9
R_{5B}	[Ω]	31.21	28.03	28.73	28.53
τ_2	[ns]	0.324	0.253	0.273	0.268
τ_4	[ns]	1.741	1.511	1.575	1.559

Iteration #		1	2	3	4
$\frac{\omega_p}{2\pi}$	[MHz]	43.87	51.96	49.52	50 13
Q_p	[ ]	1.034	0.984	1 003	0.999

The midband gain estimate is:

$H_\infty \approx 0.770$[/V/V]. Iteration 1

≈ 0.759 [V/V]. Iteration 4

The simulations gave a lower value for H_∞. Increasing K could help overcome this loss, but would also increase the sensitivities.

3 The resulting components are

Component	Initial	Value Adjusted	Standard
C_{1B}	91pF	91pF	91pF
C_{3B}	11pF	11pF	11pF
$C_{ni(446)}$	–	1 0pF	1 0pF
R_{4B}	324Ω	268Ω	267Ω
R_{5B}	31.2Ω	28.5Ω	28.7Ω
R_{fB}	453Ω	453Ω	453Ω
R_{gB}	∞	∞	∞

Figure 3 and *Figure 4* show simulated gains. The curve numbers are:

1. Ideal (Initial Design Values, $\tau_{oa} = 0$, C_{ni} 0)
2. Without pre-distortion (Initial Design Values, $\tau_{oa} \neq 0$, C_{ni} = 0)
3. With pre-distortion (Pre-distorted Values, $\tau_{oa} \neq 0$, C_{ni} = 0)

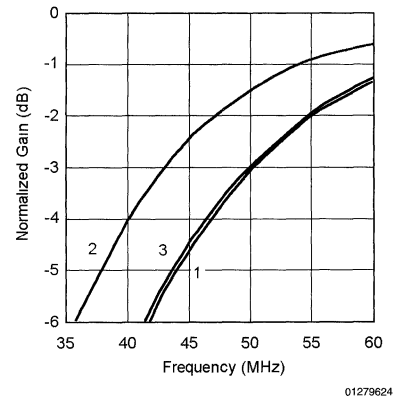


FIGURE 3. Simulated Filter Magnitude Response

Design Example (Continued)

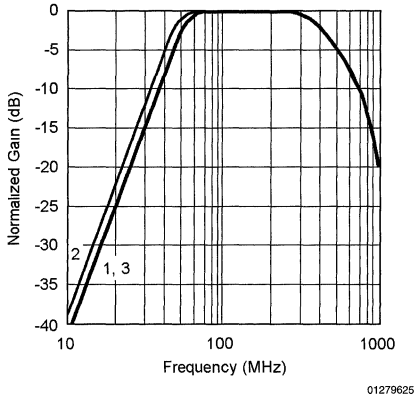


FIGURE 4. Simulated Filter Magnitude Response

SPICE Models

SPICE Models are available for most of Comlinear's amplifiers. These models support nominal DC, AC, AC noise and transient simulations at room temperature.

We recommend simulating with Comlinear's SPICE model to:

- Predict the op amp's influence on filter response
- Support quicker design cycles

Include board and component parasitic models to obtain a more accurate prediction of the filter's response.

To verify your simulations, we recommend bread-boarding your circuit.

Summary

This application Note contains an easy to use design algorithm for a low sensitivities Sallen-Key highpass biquad. Designing for low ω_p and Q_p sensitivities gives:

- Reduced filter variation over process, temperature and time
- High manufacturing yield
- Lower component cost

A low sensitivity design is not enough to produce high manufacturing yields. This Application Note shows how to compensate for the op amp bandwidth, and for the [parasitic] input capacitance of the op amp. This method also applies to any other component or board parasitics. The components must also have low enough tolerance and temperature coefficients.

Appendix A – Derivation of Pre-distortion and Parasitic Capacitance Compensation Formulas

To pre-distort this filter, and compensate for the [parasitic] input capacitance of the op amp C_{ni}):

1. Use the method in [5] to include the op amp's effect on the filter response. The result is:

$$\frac{V_o}{V_{in}} \approx \frac{H_\infty \left(\frac{1}{\omega_p^2}\right) s^2}{1 + \left(\frac{1}{(\omega_p Q_p)}\right) s + \left(\frac{1}{\omega_p^2}\right) s^2} e^{-\tau_{oa} s}$$

where the op amp group delay (τ_{oa}) is evaluated at the passband edge frequency (f_c), and:

$$\frac{1}{(\omega_p Q_p)} = R_5C_1 + R_5C_3 - R_4C_3(K-1)$$

$$\frac{1}{\omega_p^2} = R_4R_5C_1C_3 + K\tau_{oa}R_4C_3$$

$$K = \frac{1+R_f}{R_g}$$

$$H_\infty = K$$

Appendix A – Derivation of Pre-distortion and Parasitic Capacitance Compensation Formulas (Continued)

2. Since C_{ni} is in parallel with R_4, replace R_4 with the parallel equivalent of R_4 and C_{ni}:

$$\frac{R_4 \leftarrow R_4}{(1+R_4C_{ni}s)}$$

$$\frac{V_o}{V_{in}} \approx \frac{H_\infty\left(\frac{R_4C_3(R_5C_1+K\tau_{oa})}{1+R_4C_{ni}s}\right)s^2 \cdot e^{-\tau_{oa}s}}{\left(1+\left(\frac{R_4C_3(1-K)}{1+R_4C_{ni}s}+R_5(C_1+C_3)\right)s + \left(\frac{R_4C_3(R_5C_1+Kt_{oa})}{1+R_4C_{ni}s}\right)s^2\right)}$$

3. After simplifying, we obtain:

$$\frac{V_o}{V_{in}} \approx \frac{H_\infty\left(\frac{1}{\omega_p^2}\right)s^2}{1+\left(\frac{1}{(\omega_pQ_p)}\right)s+\left(\frac{1}{\omega_p^2}\right)s^2} \cdot e^{-\tau_{oa}s}$$

where:

$$\frac{1}{(\omega_pQ_p)} = t_1 + t_2$$

$$\tau_1 = R_5C_1 + R_5C_3 - R_4C_3(K-1)$$

$$\tau_2 = R_4C_{ni}$$

$$\frac{1}{\omega_p^2} = \tau_3^2 + \tau_4^2$$

$$\tau_3^2 = R_4R_5C_1C_3$$

$$\tau_4^2 = K\tau_{oa}R_4C_3 + R_4R_5(C_1+C_3)C_{ni}$$

$$K = \frac{1+R_f}{R_g}$$

$$H_\infty = \frac{K\left(\tau_3^2\right)}{\left(\tau_3^2+\tau_4^2\right)}$$

Appendix B– Bibliography

1. R. Schaumann, M Ghausi and K. Laker, *Design of Analog Filters: Passive, Active RD, and Switched Capacitor.* New Jersey: Prentice Hall, 1990.
2. A. Zverev, *Handbook of FILTER SYNTHESIS.* John Wiley & Sons, 1967.
3. A. Williams and F. Taylor, *Electronic Filter Design Handbook.* McGraw Hill, 1995.
4. S. Natarajan, *Theory and Design of Linear Active Networks.* Macmillan, 1987.
5. K Blake, "Component Pre-distortion for Sallen-Key Filters, " *Comlinear Application Note*, OA-21, Rev. B, July 1996.
6. K. Blake, "Low-Sensitivity, Lowpass Filter Design," *Comlinear Application Note*, OA-27, July 1996.
7. K. Blake, "Low-Sensitivity, Bandpass Filter Design With Tuning Method," *Comlinear Application Note*, OA-28, Oct. 1996

Note: The circuits included in this application note have been tested with National Semiconductor parts that may have been obsoleted and/or replaced with newer products. Please refer to the CLC to LMH conversion table to find the appropriate replacement part for the obsolete device.

Section 5
Audio

Section 5 Contents

High-Performance Audio Applications of The LM833

National Semiconductor
Application Note 346
Kerry Lacanette

Designers of quality audio equipment have long recognized the value of a low noise gain block with "audiophile performance". The LM833 is such a device: a dual operational amplifier with excellent audio specifications. The LM833 features low input noise voltage ($4.5\ nV/\sqrt{Hz}$ typical), typical), large gain-bandwidth product (15 MHz), high slew rate (7V/μSec), low THD (0.002% 20 Hz-20 kHz), and unity gain stability. This Application Note describes some of the ways in which the LM833 can be used to deliver improved audio performance.

1. Two Stage RIAA Phono Preamplifier

A phono preamplifier's primary task is to provide gain (usually 30 to 40 dB at 1 kHz) and accurate amplitude and phase equalization to the signal from a moving magnet or a moving coil cartridge. (A moving coil device's output voltage is typically around 20 dB lower than that of a moving magnet pickup, so this signal is usually amplified by a step-up device—either an active circuit or a transformer—before being applied to the input of the phono preamplifier). In addition to the amplification and equalization functions, the phono preamp must not add significant noise or distortion to the signal from the cartridge.

Figure 1 shows the standard RIAA phono preamplifier amplitude response. Numerical values relative to the 1 kHz gain are given in *Table 1*. Note that the gain rolls off at a 6 dB/octave rate above 2122 Hz. Most phono preamplifier circuits in commercially available audio products, as well as most published circuits, are based on the topology shown in *Figure 2(a)*. The network consisting of R_1, R_2, C_1, and C_2 is not unique, and can be replaced by any of several other networks that give equivalent results. R_0 is generally well under 1k to keep its contribution to the input noise voltage below that of the cartridge itself. The 47k resistor shunting the input provides damping for moving-magnet phono cartridges. The input is also shunted by a capacitance equal to the sum of the input cable capacitance and C_p. This capacitance resonates with the inductance of the moving magnet cartridge around 15 kHz to 20 kHz to determine the frequency response of the transducer, so when a moving magnet pickup is used, C_p should be carefully chosen so that the total capacitance is equal to the recommended load capitance for that particular cartridge.

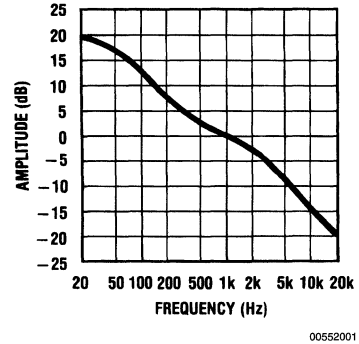


FIGURE 1. Standard RIAA phonograph preamplifier frequency response curve.Gain continues to roll off at a 6 dB/octave rate above 20 kHz.

TABLE 1. RIAA standard response referred to gain at 1 kHz.

FREQUENCY (Hz)	AMPLITUDE (dB)	FREQUENCY (Hz)	AMPLITUDE (dB)
20	+19.3	800	+0.7
30	+18.6	1000	0.0
40	+17.8	1500	−1.4
50	+17.0	2000	−2.6
60	+16.1	3000	−4.8
80	+14.5	4000	−6.6
100	+13.1	5000	−8 2
150	+10.3	6000	−9.6
200	+8.2	8000	−11.9
300	+5.5	10000	−13.7
400	+3.8	15000	−17.2
500	+2.6	20000	−19.6

The circuit of *Figure 2(a)* has a disadvantage· it cannot accurately follow the curve in *Figure 1*, no matter what values are chosen for the feedback resistors and capacitors. This is because the non-inverting amplifier cannot have a gain of less than unity, which means that the high frequency gain cannot roll off continuously above the 2122 Hz breakpoint as it is supposed to. Instead, a new breakpoint is introduced at the unity gain frequency.

In addition to the amplitude response errors (which can be made small through careful design), the lack of a continued rolloff can cause distortion in later stages of the audio system by allowing high frequency signals from the pickup cartridge to pass through the phono equalizer without sufficient attenuation. This is generally not a problem with moving magnet cartridges, since they are usually severely band-limited above 20 kHz due to the electrical resonance of

1. Two Stage RIAA Phono Preamplifier (Continued)

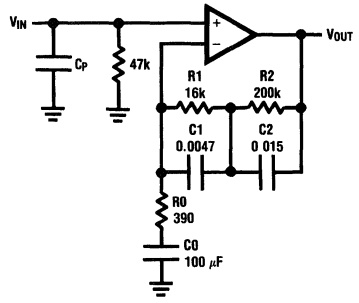
cartridge inductance and preamp input capacitance. Moving coil cartridges, however, have very low inductance, and can produce significant output at frequencies as high as 150 kHz. If a subsequent preamplifier stage or power amplifier suffers from distortion caused by slew-rate limitations, these ultrasonic signals can cause distortion of the audio signal even though the signals actually causing the distortion are inaudible.

Preamplifers using the topology of *Figure 2(a)* can suffer from distortion due to input stage nonlinearities that are not corrected by the feedback loop. The fact that practical amplifiers have non-infinite common mode rejection ratios means that the amplifier will have a term in its gain function that is dependent on the input voltage level. Since most good operational amplifiers have very high common mode rejection ratios, this form of distortion is usually quite difficult to find in opamp-based designs, but it is very common in discrete amplifiers using two or three transistors since these circuits generally have poor common mode performance. Another source of input stage distortion is input impedance nonlinearity. Since the input impedance of an amplifier can vary depending on the input voltage, and the signal at the amplifier input will be more strongly affected by input impedance if the source impedance is high, distortion will generally increase as the source impedance increases. Again, this problem will typically be significant only when the amplifier is a simple discrete design, and is not generally troublesome with good op amp designs.

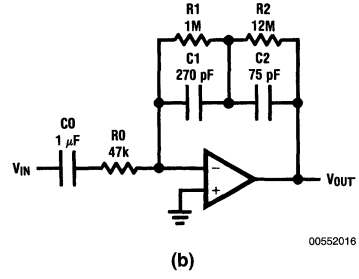
The disadvantages of the circuit configuration of *Figure 2(a)* have led some designers to consider the use of RIAA preamplifiers based on the inverting topology shown in *Figure 2(b)*. This circuit can accurately follow the standard RIAA response curve since the absolute value of its gain can be less than unity. The reduced level of ultrasonic information at its output will sometimes result in lower perceived distortion (depending on the design of the other components in the audio system). Since there is no voltage swing at the preamplifier input, distortion will be lower in cases where the gain block has poor common-mode performance. (The common-mode distortion of the LM833 is low enough that it exhibits essentially the same THD figures whether it is used in the inverting or the non-inverting mode.)

The primary handicap of the inverting configuration is its noise performance. The 47k resistor in series with the source adds at least 4 µV of noise (20 Hz to 20 kHz) to the preamplifier's input. In addition to 4 µV of thermal noise from the 47k resistor, the high impedance in series with the preamp input will generally result in a noise increase due to the preamplifier's input noise current, especially when the series impedance is made even larger by a moving magnet cartridge at resonance. In contrast, the 47k damping resistor in *Figure 2(a)* is in parallel with the source, and is a significant noise contributor only when the source impedance is high. This will occur near resonance, when the source is a moving magnet cartridge. Since the step-up devices used with moving coil cartridges present a low, primarily resistive source impedance to the preamplifier input, the effects of cartridge resonance and input noise current are virtually eliminated for moving coil sources. Therefore, the circuit of *Figure 2(a)* has a noise advantage of about 16 dB with a moving coil source, and from about 13 dB to about 18 dB (depending on the source impedance and on the input noise current of the amplifier) with a moving magnet source. Using the component values shown, the circuit in *Figure 2(a)* follows the RIAA characteristic with an accuracy of better than 0.5 dB (20–20 kHz) and has an input-referred noise voltage equal to 0.33 µV over the Audio frequency range.

Even better performance can be obtained by using the two-amplifier approach of *Figure 3*. The first operational amplifier takes care of the 50 Hz and 500 Hz breakpoints, while the 2122 Hz rolloff is accomplished by the passive network R_3, R_6, and C_3. The second amplifier supplies additional gain—10 dB in this example. Using two amplifiers results in accurate conformance to the RIAA curve without reverting to the noisy inverting topology, as well as lower distortion due to the fact that each amplifier is operating at a lower gain than would be the case in a single-amplifier design. Also, the amplifiers are not required to drive capacitive feedback networks with the full preamplifier output voltages, further reducing distortion compared to the single-amplifier designs.



(a)



(b)

FIGURE 2. Two typical operational amplifier-based phonograph preamplifier circuits. (a) Non-inverting. (b) Inverting.

The design equations for the preamplifier are:

$R_1 = 8.058\ R_0A_1$, where A_1 is the 1 kHz voltage gain of the first amplifier. (1)

1. Two Stage RIAA Phono Preamplifier (Continued)

$$C_1 = \frac{3.18 \times 10^{-3}}{R_1} \quad (2)$$

$$R_2 = \frac{R_1}{9} - R_0 \quad (3)$$

$$C_3 = 7.5 \times 10^{-5} \frac{(R_3 + R_6)}{R_3 R_6} = \frac{7.5 \times 10^{-5}}{R_P} \quad (4)$$

$$C_4 = \frac{1}{2\pi f_L (R_3 + R_6)} \quad (5)$$

where f_L is the low-frequency −3 dB corner of the second stage. For standard RIAA preamplifiers, f_L should be kept well below the audible frequency range. If the preamplifier is to follow the IEC recommendation (IEC Publication 98, Amendment #4), f_L should equal 20.2 Hz.

$$A_{V2} = 1 + \frac{R_5}{R_4} \quad (6)$$

where A_{V2} is the voltage gain of the second amplifier.

$$C_0 \approx \frac{1}{2\pi f_0 R_0} \quad (7)$$

where f_0 is the low-frequency −3 dB corner of the first amplifier. This should be kept well below the audible frequency range.

A design procedure is shown below with an illustrative example using 1% tolerance E96 components for close conformance to the ideal RIAA curve. Since 1% tolerance capacitors are often difficult to find except in 5% or 10% standard values, the design procedure calls for re-calculation of a few component values so that standard capacitor values can be used.

RIAA PHONO PREAMPLIFIER DESIGN PROCEDURE

1. Choose R_0. R_0 should be small for minimum noise contribution, but not so small that the feedback network excessively loads the amplifier.
   Example: Choose $R_0 = 500$.
2. Choose 1 kHz gain, A_{V1} of first amplifier. This will typically be around 20 dB to 30 dB.
   Example: Choose $A_{V1} = 26$ dB = 20.
3. Calculate $R_1 = 8.058 R_0 A_{V1}$
   Example: $R_1 = 8.058 \times 500 \times 20 = 80.58$k.
4. $$\text{Calculate } C_1 = \frac{3.18 \times 10^{-3}}{R_1}$$
   $$\text{Example: } C_1 = \frac{3.18 \times 10^{-3}}{8.058 \times 10^4} = 0.03946\ \mu F$$
5. If C_1 is not a convenient value, choose the nearest convenient value and calculate a new R_1 from
   $$R_1 = \frac{3.18 \times 10^{-3}}{C_1}$$
   Example: New $C_1 = 0.039\ \mu F$.
   $$\text{New } R_1 = \frac{3.18 \times 10^{-3}}{3.9 \times 10^{-8}} = 81.54k$$
   Use $R_1 = 80.6$k
6. Calculate a new value for R_0 from $R_0 = \frac{R_1}{8.058 A_{V1}}$
   $$\text{Example: New } R_0 = \frac{8.06 \times 10^4}{8.058 \times 20} = 498.8.$$
   Use $R_0 = 499$.
7. $$\text{Calculate } R_2 = \frac{R_1}{9} - R_0$$
   $$\text{Example: } R_2 = \frac{8.06 \times 10^4}{9} - 499 = 8456.56$$
   Use 8.45k.
8. Choose a convenient value for C_3 in the range from 0.01 µF to 0.05 µF.
   Example: $C_3 = 0.033\ \mu F$.
9. $$\text{Calculate } R_P = \frac{7.5 \times 10^{-5}}{C_3}$$
   $$\text{Example: } R_P = \frac{7.5 \times 10^{-5}}{3.3 \times 10^{-8}} = 2.273k.$$
10. Choose a standard value for R_3 that is slightly larger than R_P.
    Example: $R_3 = 2.37$k.
11. Calculate R_6 from $1/R_6 = 1/R_P - 1/R_3$
    Example: $R_6 = 55.36$k
    Use 54.9k.
12. Calculate C_4 for low-frequency rolloff below 1 Hz from design *Equation (5)*.
    Example: $C_4 = 2\ \mu F$. Use a good quality mylar, polystyrene, or polypropylene.

1. Two Stage RIAA Phono Preamplifier (Continued)

13. Choose gain of second amplifier.
    Example: The 1 kHz gain up to the input of the second amplifier is about 26 dB for this example. For an overall 1 kHz gain equal to about 36 dB we choose:
    A_{V2} = 10 dB = 3.16.
14. Choose value for R_4.
    Example: R_4 = 2k.
15. Calculate $R_5 = (A_{V2} - 1)\, R_4$
    Example: R_5 = 4.32k.
    Use R_5 = 4.3k
16. Calculate C_0 for low-frequency rolloff below 1 Hz from design *Equation (7)*.
    Example: C_0 = 200 µF.

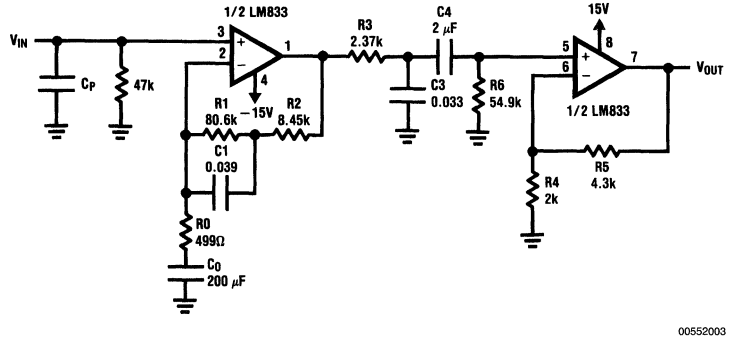


FIGURE 3. Two-amplifier RIAA phono preamplifier with very accurate RIAA response.

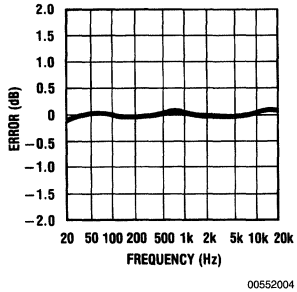


FIGURE 4. Deviation from ideal RIAA response for circuit of *Figure 3* using 1% resistors. The maximum observed error for the prototype was 0.1 dB.

The circuit of *Figure 3* has excellent performance: Conformance to the RIAA curve is within 0.1 dB from 20 Hz to 20 kHz, as illustrated in *Figure 4* for a prototype version of the circuit. THD and noise data are reproduced in *Figure 5* and *Table 2*, respectively. If a "perfect" cartridge with 1mV/cm/s sensitivity (higher than average) is used as the input to this preamplifier, the highest recorded groove velocities available on discs (limited by the cutting equipment) will fall below the 1V curve except in the 1 kHz to 10 kHz region, where isolated occurances of 2V to 3V levels can be generated by one or two of the "superdiscs". (See reference 4). The distortion levels at those frequencies and signal levels are essentially the same as those shown on the 1V curve, so they are not reproduced separately here. It should be noted that most real cartridges are very limited in their ability to track such large velocities, and will not generate preamplifier output levels above 1Vrms even under high groove velocity conditions.

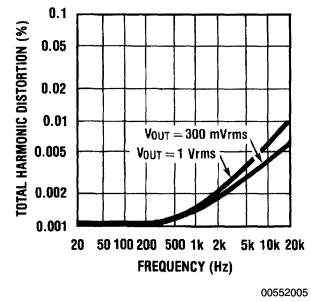


FIGURE 5. THD of circuit in *Figure 3* as a function of frequency. The lower curve is for an output level of 300mVrms and the upper curve is for an output level of 1Vrms.

1. Two Stage RIAA Phono Preamplifier (Continued)

TABLE 2. Equivalent input noise and signal-to-noise ratio for RIAA preamplifier circuit of *Figure 3*. Noise levels are referred to gain at 1 kHz.

NOISE WEIGHTING	CCIR/ARM	"A"	FLAT
Noise voltage	0.26 μV	0.23 μV	0.37 μV
S/N referred to 5 mV input at 1 kHz	86 dB	87 dB	82 dB

2. Active Crossover Network for Loudspeakers

A typical multi-driver loudspeaker system will contain two or more transducers that are intended to handle different parts of the audio frequency spectrum. Passive filters are usually used to split the output of a power amplifier into signals that are within the usable frequency range of the individual drivers. Since passive crossover networks must drive loudspeaker elements whose impedances are quite low, the capacitors and inductors in the crossovers must be large in value, meaning that they will very likely be expensive and physically large. If the capacitors are electrolytic types or if the inductors do not have air cores, they can also be significant sources of distortion. Futhermore, many desirable filter characteristics are either impossible to realize with passive circuitry, or require so much attenuation to achieve passively that system efficiency is severely reduced.

An alternative approach is to use low-level filters to divide the frequency spectrum, and to follow each of these with a separate power amplifier for each driver or group of drivers. A two-way (or "bi-amped") system of this type is shown in *Figure 6*. This basic concept can be expanded to any number of frequency bands. For accurate sound reproduction, the sum of the filter outputs should be equal to the crossover input (if the transducers are "ideal"). While this seems to be an obvious requirement, it is very difficult to find a commercial active dividing network that meets it. Consider an active crossover consisting of a pair of 2nd-order Butterworth filters, (one is a low-pass; the other is a high-pass). The transfer functions of the filters are of the form:

$$\frac{V_L(s)}{V_{IN}(s)} = \frac{1}{s^2 + \sqrt{2}s + 1}$$

$$\frac{V_H(s)}{V_{IN}(s)} = \frac{s^2}{s^2 + \sqrt{2}s + 1}$$

and their sum is:

$$\frac{V_L(s)}{V_{IN}(s)} + \frac{V_H(s)}{V_{IN}(s)} = \frac{1 + s^2}{s^2 + \sqrt{2}s + 1}$$

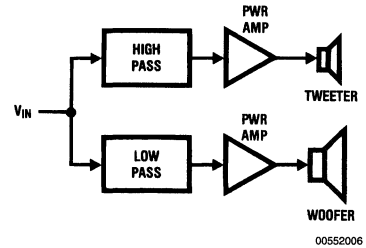


FIGURE 6. Block diagram of a two-way loudspeaker system using a low level crossover network ahead of the power amplifiers.

The output will therefore never exactly equal the input signal (except in the trivial case of a DC input). *Figure 7* shows the response of this crossover to a square wave input, and the amplitude and phase response of the crossover to sinusoidal steady state inputs can be seen in *Figure 8*. Higher-order filters will yield similarly dissatisfying results when this approach is used.

A significant improvement can be made by the use of a constant voltage crossover like the one shown in *Figure 9*. The term "constant voltage" means that the outputs of the high-pass and low-pass sections add up to produce an exact replica of the input signal. The rolloff rate is 12 dB/octave. The input impedance is equal to R/2, or 12 kΩ in the circuit of *Figure 9*. The LM833 is especially well-suited for active filter applications because of its high gain-bandwidth product. The transfer functions of this crossover network are of the form

$$\frac{V_L(s)}{V_{IN}(s)} = \frac{a_1 s + 1}{a_3 s^3 + a_2 s^2 + a_1 s + 1}$$

and

$$\frac{V_H(s)}{V_{IN}(s)} = \frac{a_3 s^3 + a_2 s^2}{a_3 s^3 + a_2 s^2 + a_1 s + 1}$$

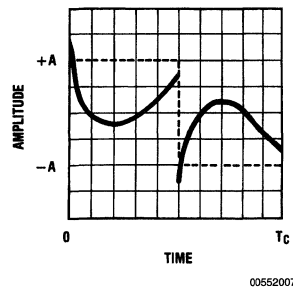


FIGURE 7. Response of second-order Butterworth crossover network (high-pass and low-pass outputs summed) to a square wave input (dashed line) at the crossover frequency. Period is $T_C = 1/f_C$.

2. Active Crossover Network for Loudspeakers (Continued)

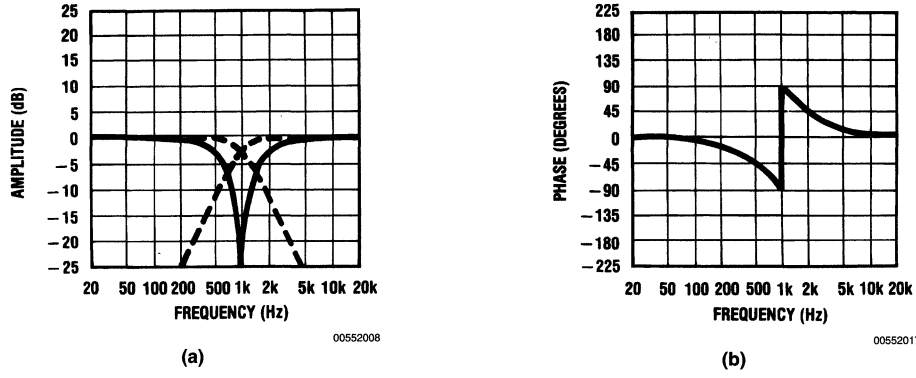


FIGURE 8. Magnitude (a) and phase (b) response of a second-order, 1 kHz Butterworth crossover network with the high-pass and low-pass outputs summed. The individual high-pass and low-pass outputs are superimposed (dashed lines).

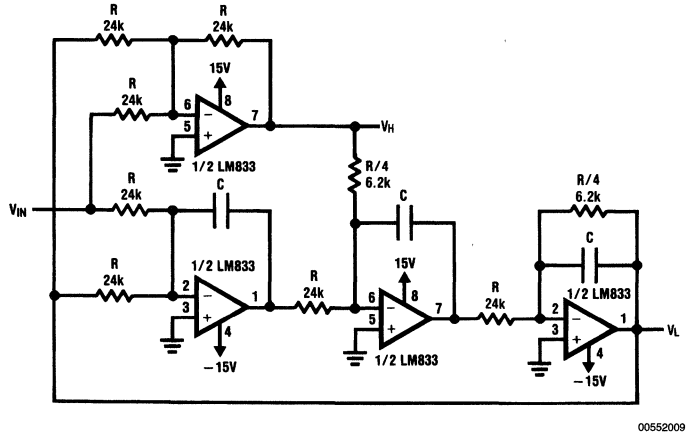


FIGURE 9. Constant-voltage crossover network with 12 dB/octave slopes. The crossover frequency is equal to $\frac{1}{2\pi RC}$.

The low-pass and high-pass constant voltage crossover outputs are plotted in *Figure 10*. The square-wave response (not shown) of the summed outputs is simply an inverted square-wave, and the phase shift (also not shown) is essentially 0° to beyond 20 kHz.

2. Active Crossover Network for Loudspeakers (Continued)

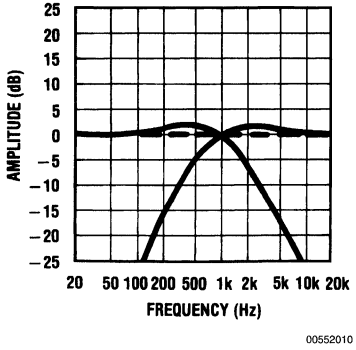


FIGURE 10. Low-pass and high-pass responses of constant-voltage crossover network in *Figure 9* with crossover frequency of 1 kHz. For the circuit of *Figure 9*, a_1=4, a_2=4, and a_3=1. Note that the summed response (dashed lines) is perfectly flat.

It is important to remember that even a constant voltage crossover transfer function does not guarantee an ideal overall system response, because the transfer functions of the transducers will also affect the overall response. This can be minimized to some extent by using drivers that are "flat" at least two octaves beyond the crossover frequency.

3. Infrasonic and Ultrasonic Filters

In order to ensure "perfectly flat" amplitude response from 20 Hz to 20 kHz, many audio circuits are designed to have bandwidths extending far beyond the audio frequency range. There are many high-fidelity systems, however, that can be audibly improved by reducing the gain at frequencies above and below the limits of audibility

The phonograph arm/cartridge/disc combination is the most significant source of unwanted low-frequency information. Disc warps on 33⅓ rpm records can cause large-amplitude signals at harmonics of 0.556 Hz. Other large low-frequency signals can be created at the resonance frequency determined by the compliance of the pickup cartridge and the effective mass of the cartridge/arm combination. The magnitude of undesireable low-frequency signals can be especially large if the cartridge/arm resonance occurs at a warp frequency. Infrasonic signals can sometimes overload amplifiers, and even in the absence of amplifier overload can cause large woofer excursions, resulting in audible distortion and even woofer damage.

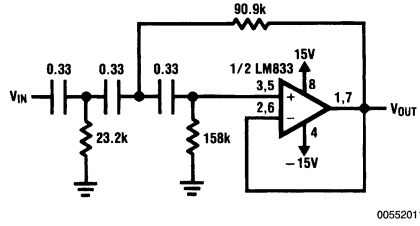


FIGURE 11. Filter for rejection of undersireable infrasonic signals. Filter characteristic is third-order Butterworth with −3 dB frequency at 15 Hz. Resistor and capacitor values shown are for 1% tolerance components. 5% tolerance units can be substituted in less critical applications.

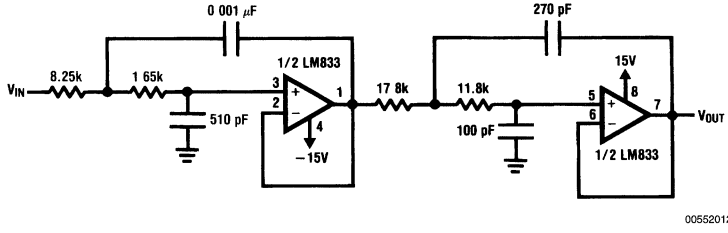


FIGURE 12. Ultrasonic rejection filter with fourth-order Bessel low-pass characteristic. The filter gain is down 3 dB at about 40 kHz. As with the infrasonic filter, 1% tolerance components should be used for accurate response.

3. Infrasonic and Ultrasonic Filters

(Continued)

Ultrasonic signals tend to cause problems in power amplifiers when the amplifiers exhibit distortion mechanisms due to slew rate limitations and other high frequency nonlinearities. The most troublesome high-frequency signals come principally from moving-coil cartridges and sometimes from tape recorders if their bias oscillator outputs manage to get into the audio signal path. Like the infrasonic signals, ultrasonic signals can place distortion products in the audio band even though the offending signals themselves are not audible.

The circuits in *Figure 11* and *Figure 12* attenuate out-of-band signals while having minimal effect on the audio program. The infrasonic filter in *Figure 11* is a third-order Butterworth high-pass with its –3 dB frequency at 15 Hz. The attenuation at 5 Hz is over 28 dB, while 20 Hz information is reduced by only 0.7 dB and 30 Hz information by under 0.1 dB.

The ultrasonic filter in *Figure 12* is a fourth-order Bessel alignment, giving excellent phase characteristics. A Bessel filter approximates a delay line within its passband, so complex in-band signals are passed through the filter with negligible alteration of the phase relationships among the various in-band signal frequencies. The circuit shown is down 0.65 dB at 20 kHz and –3 dB at about 40 kHz. Rise time is limited to about 8.5 µSec.

The high-pass and low-pass filters exhibit extremely low THD, typically under 0.002%. Both circuits must be driven from low impedance sources (preferably under 100 ohms). 5% components will often yield satisfactory results, but 1% values will keep the filter responses accurate and minimize mismatching between the two channels. The amplitude response of the two filters in cascade is shown in *Figure 13*. When the two filters are cascaded, the low-pass should precede the high-pass.

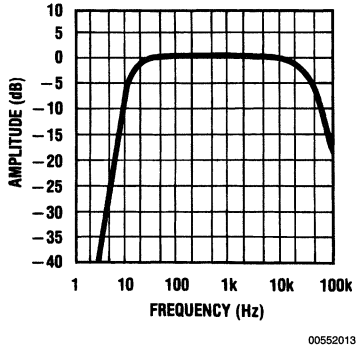


FIGURE 13. Amplitude response of infrasonic and ultrasonic filters connected in series.

4. Transformerless Microphone Preamplifiers

Microphones used in professional applications encounter an extremely wide dynamic range of input sound pressure levels, ranging from about 30 dB SPL (ambient noise in a quiet room) to over 130 dB SPL. The output voltage of a low impedance (200 ohm) microphone over this range of SPLs might typically vary from 20 µV to 2V rms, while its self-generated output noise would be on the order of 0.25 µV over a 20 kHz bandwidth. Since the microphone's output dynamic range is so large, a preamplifier for microphone signals should have an adjustable gain so that it can be optimized for the signal levels that will be present in a given situation. Large signals should be handled without clipping or excessive distortion, and small signals should not be degraded by preamplifier noise.

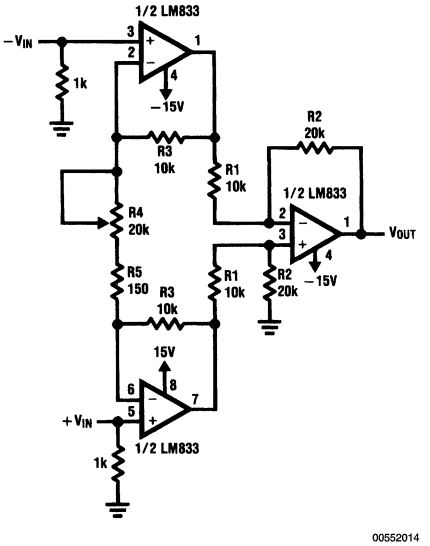


FIGURE 14. Simple transformerless microphone preamplifier using LM833. R_1, R_2, and R_3 are 0.1% tolerance units (or R_2 can be trimmed).

For a conservative low noise design, the preamplifier should contribute no more noise to the output signal than does the resistive portion of the source impedance. In practical applications, it is often reasonable to allow a higher level of input noise in the preamplifier since ambient room noise will usually cause a noise voltage at the microphone output terminals that is on the order of 30 dB greater than the microphone's intrinsic (due to source resistance) noise floor.

When long cables are used with a microphone, its output signal is susceptable to contamination by external magnetic fields—especially power line hum. To minimize this problem, the outputs of most professional microphones are balanced, driving a pair of twisted wires with signals of opposite polarity. Ideally, magnetic fields will induce equal voltages on each of the two wires, which can then be cancelled if the signals are applied to a transformer or differential amplifier at the preamplifier input.

The circuits in *Figure 14* and *Figure 15* are transformerless differential input microphone preamplifiers. Avoiding transformers has several advantages, including lower cost, smaller physical size, and reduced distortion. The circuit of *Figure 14* is the simpler of the two, with two LM833s amplifying the input signal before the common-mode noise is cancelled in the differential amplifier. The equivalent input noise is about 760 nV over a 20 Hz to 20 kHz frequency band (–122 dB referred to 1V), which is over 26 dB lower

4. Transformerless Microphone Preamplifiers (Continued)

than a typical microphone's output from the 30 dB SPL ambient noise level in a quiet room. THD is under .01% at maximum gain, and .002% at minimum gain. For more critical applications with lower sensitivity microphones, the circuit of *Figure 15* uses LM394s as input devices for the LM833 gain stages. The equivalent input noise of this circuit is about 2.4 nv/√Hz, at maximum gain, resulting in a 20 Hz to 20 kHz input noise level of 340 nV, or −129 dB referred to 1V.

In both circuits, potentiometer R_4 is used to adjust the circuit gain from about 4 to 270. The maximum gain will be limited by the minimum resistance of the potentiometer. If R_1, R_2, and R_3 are all 0.1% tolerance units, the rejection of hum and other common-mode noise will typically be about 60 dB, and about 44 dB worst case. If better common-mode rejection is needed, one of the R_2s can be replaced by an 18k resistor and a 5k potentiometer to allow trimming of CMRR. To prevent radio-frequency interference from getting into the preamplifier inputs, it may be helpful to place 470 pF capacitors between the inputs and ground.

References:

1) S. P. Lipshitz, J. Audio Eng. Soc., "On RIAA Equalization Networks", June 1979.

2) P. J. Baxandall, J. Audio Eng. Soc., Letter, pp47–52, Jan 1981.

3) Ashley and Kaminsky, J. Audio Eng. Soc., "Active and Passive Filters as Loudspeaker Crossover Networks", June 1971.

4) T. Holman, Audio, "Dynamic Range Requirements of Phonographic Preamplifiers", July 1977.

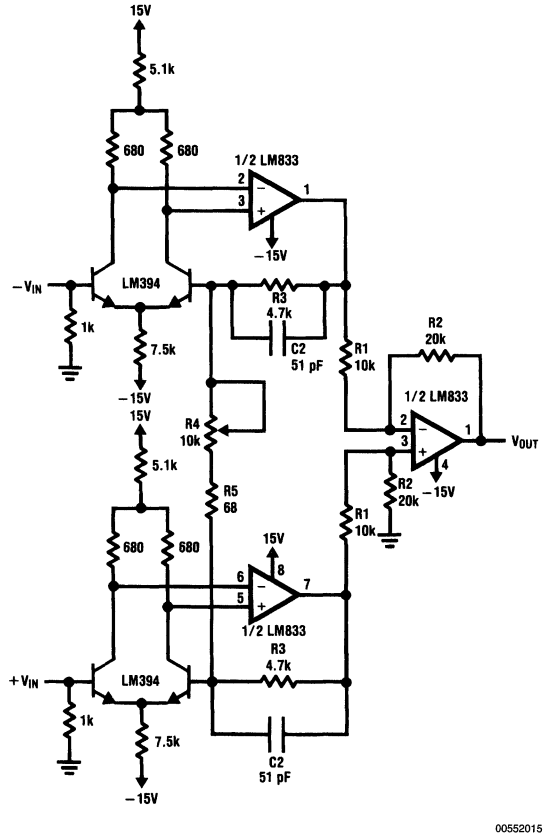


FIGURE 15. Transformerless microphone preamplifier similar to that of *Figure 14*, but using LM394s as low-noise input stages.

Appendix I: Derivation of RIAA Phono Preamplifier Design *Equations (8), (9), (10).*

The first three design equations on the third page are derived here. The derivations of the others should be apparent by observation. The purpose of the preamplifier's first stage is to produce the transfer function:

$$A_V(s) = A_V(dc)\,\frac{(3.18 \times 10^{-4} + 1)}{(3.18 \times 10^{-3} + 1)} \tag{8}$$

where $A_V(dc)$ is the dc gain of the first stage.

The actual first stage transfer function is (ignoring C_0):

$$A_V(s) = \frac{sC_1(R_0R_1 + R_1R_2) + R_0 + R_1 + R_2}{sC_1R_0R_1 + R_0}$$

$$= \left[\frac{R_0 + R_1 + R_2}{R_0}\right]\left[\frac{sC_1\dfrac{(R_0R_1 + R_1R_2)}{R_0 + R_1 + R_2} + 1}{sC_1R_1 + 1}\right] \tag{9}$$

Equating terms, we have:

$$\frac{C_1(R_0R_1 + R_1R_2)}{R_0 + R_1 + R_2} = 3.18 \times 10^{-4} \tag{10}$$

$$C_1R_1 = 3.18 \times 10^{-3} \tag{11}$$

$$A_V(dc) = \frac{R_0 + R_1 + R_2}{R_0} \tag{12}$$

Note that *Equation (11)* is quivalent to *Equation (2)* on page three.

From *Equation (10)* and *Equation (11)* we have:

$$\frac{C_1R_1(R_0 + R_2)}{R_0 + R_1 + R_2} = \frac{C_1R_1}{10} \tag{13}$$

Therefore:

$$\frac{R_0 + R_1 + R_2}{R_0 + R_2} = 10 \tag{14}$$

$$\frac{R_1}{R_0 + R_2} = 9 \tag{15}$$

$$\text{and } R_2 = \frac{R_1}{9} - R_0 \tag{16}$$

Equation (16) is equivalent to design *Equation (3)* on page three.

Combining *Equation (12)* and *Equation (16)*,

$$A_V(dc) = \frac{R_0 + R_1 + R_2}{R_0} = \frac{R_1(1 + 1/9)}{R_0} \tag{17}$$

Finally, solving for R_1 and using $A_V(dc) = 8.9535A_V$ (1 kHz) yields:

$$R_1 = \frac{R_0A_V(dc)}{10/9} = 0.9R_0A_V(dc) = 8.058A_V(1\text{ kHz})R_0\,, \tag{18}$$

which is equivalent to *Equation (1)* on page three.

Appendix II: Standard E96 (1%) Resistor Values

Standard Resistor Values (E-96 Series)							
10.0	13.3	17.8	23.7	31.6	42.2	56.2	75.0
10.2	13.7	18.2	24.3	32.4	43.2	57.6	76.8
10.5	14.0	18.7	24.9	33.2	44.2	59.0	78.7
10.7	14.3	19.1	25.5	34.0	45.3	60.4	80.6
11.0	14.7	19.6	26.1	34.8	46.4	61.9	82.5
11.3	15.0	20.0	26.7	35.7	47.5	63.4	84.5
11.5	15.4	20.5	27.4	36.5	48.7	64.9	86.6
11.8	15.8	21.0	28.0	37.4	49.9	66.5	88.7
12.1	16.2	21.5	28.7	38.3	51.1	68.1	90.9
12.4	16.5	22.1	29.4	39.2	52.3	69.8	93.1
12.7	16.9	22.6	30.1	40.2	53.6	71.5	95.3
13.0	17.4	23.2	30.9	41.2	54.9	73.2	97.6

Audio Noise Reduction and Masking

National Semiconductor
Application Note 384
Martin Giles

Introduction

Audio noise reduction systems can be divided into two basic approaches. The first is the complementary type which involves compressing the audio signal in some well-defined manner before it is recorded (primarily on tape). On playback, the subsequent complementary expansion of the audio signal which restores the original dynamic range, at the same time has the effect of pushing the reproduced tape noise (added during recording) farther below the peak signal level—and hopefully below the threshold of hearing.

The second approach is the single-ended or non-complementary type which utilizes techniques to reduce the noise level already present in the source material—in essence a playback only noise reduction system. This approach is used by the LM1894 integrated circuit, designed specifically for the reduction of audible noise in virtually any audio source.

While either type of system is capable of producing a significant reduction in audible noise levels, compandors are inherently capable of the largest reduction and, as a result, have found the most favor in studio based equipment. This would appear to give compandors a distinct edge when it comes to translating noise reduction systems from the studio or lab to the consumer marketplace. Compandors are not, unfortunately, a complete solution to the audio noise problem. If we summarize the major desirable attributes of a noise reduction system we will come up with at least eight distinct things that the system must do—and no system as yet does all of them perfectly.

1) The reproduced signal (now free of noise) is audibly identical to the original signal in terms of frequency response, transient response and program dynamics. The stereo image is stable and does not wander.
2) Overload characteristics of the system are well above the normal peak signal level.
3) The system electronics do not produce additional noise (including perturbations produced by the control signal path).
4) Proper response of the system does not depend on phase/frequency or gain accuracy of the transmission medium.
5) System operation does not cause audible modulation of the noise level.
6) The system enables the full dynamic range of the source to be utilized without distortion.
7) The recorded signal sounds natural on playback—even when decoding is not used. This means that the system is compatible with existing equipment.
8) Finally, the system is universal and can be used with any medium; disc, FM broadcast, television broadcast, audio and video tapes.

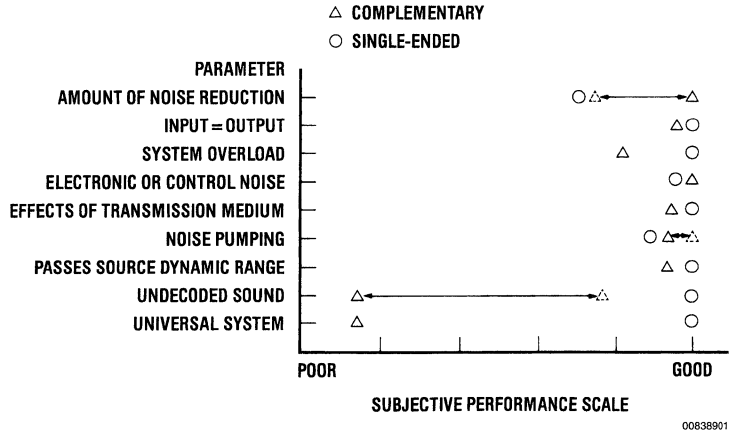


FIGURE 1. Comparison of Noise Reduction Systems

Although no system presently meets all these requirements—and the performance level they do reach is often judged subjectively—they provide a useful set of performance standards by which to judge the n.r. systems that are available. In particular, in the consumer field items 7) and 8) are significant. The most popular n.r. system, Dolby B Type, got that way in part because pre-recorded and encoded tapes could be played back on tape-decks that did not have Dolby B decoders (Dolby B uses a relatively small amount of compression and that only for low level higher frequency signals). Similarly, DNR™, which uses the LM1894, is gaining in popularity because it does not require any encoding and, in addition, can work with any audio source, including Dolby B encoded tapes.

DNR is a non-complementary noise reduction system which can give up to 14 dB noise reduction in stereo program material. The operation of the LM1894 is dependent on two

Introduction (Continued)

principles; that the audible noise is proportional to the system bandwidth—decreasing the bandwidth decreases the noise—and that the desired signal is capable of "masking" the noise when the signal to noise ratio is sufficiently high. DNR automatically and continuously changes the system bandwidth in response to the amplitude and frequency content of the program. Restricting the bandwidth to less than 1 kHz reduces the audible noise by up to 14 dB (weighted) and a special spectral weighting filter in the control path ensures that the bandwidth is always increased sufficiently to pass any music that may be present. Because of this ability to analyze the auditory masking qualities of the program material, DNR does not require the source to be encoded in any special way for noise reduction to be obtained.

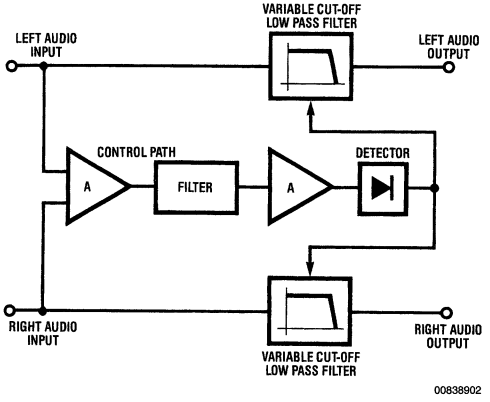


FIGURE 2. Stereo Noise Reduction System (DNR)

Noise Reduction by Bandwidth Restriction

The first principle upon which DNR is based—that a reduction in system bandwidth is accompanied by a reduction in noise level—is rather easy to show. If our system noise is assumed to be caused solely by resistive sources then the noise amplitude will be uniform over the frequency bandwidth. The total or aggregate noise level $\overline{e_{NT}}$ is given by the familiar formula

$$\overline{e_{NT}} = \sqrt{4KTBR} \qquad (1)$$

K = Boltzmanns cons't

T = absolute temp.

B = bandwidth

R = source resistance

At any single frequency, the noise amplitude measured in a bandwidth of 1 Hz is $\overline{e_n}$, and therefore

$$\overline{e_{NT}} = \overline{e_n}\sqrt{B} \qquad (2)$$

This shows that the total noise, and hence the S/N ratio, is directly proportional to the square root of the system bandwidth. For example, if the system bandwidth is changed from 30 kHz to 1 kHz, the aggregate S/N ratio changes by $20 \log_{10} \sqrt{1 \times 10^3} - 20 \log_{10} \sqrt{30 \times 10^3} = -14.8$ dB

This result, although mathematically correct, is not exactly what will occur in practice for several reasons. Most audio systems will have a generally smooth noise spectrum similar to white noise, but the amplitude is not necessarily uniform with frequency. In audio cassette systems where the dominant noise source is the tape itself, the frequency response often falls off rapidly beyond 12 kHz anyway. For video tapes with very slow longitudinal audio tracks, the frequency response is well below 10 kHz, depending on the recording mode. Disc noise generally increases towards the low frequency end of the audio spectrum whereas FM broadcast noise decreases below 2 kHz. On the other hand, the frequency range of the noise spectrum is not always indicative of its obtrusiveness. The human ear is most sensitive to noise in the frequency range from 800 Hz to just above 8 kHz. Because of this, a weighting filter inserted into the measurement system which gives emphasis to this frequency range, produces better correlation between the S/N "number" and the subjective impression of noise audibility. Generally speaking, a typical tape noise spectrum and a weighting filter such as CCIR/ARM will yield noise reduction numbers between 10–14 dB when a single pole low pass filter is used to restrict the audio bandwidth to less than 1 kHz. Up to 18 dB noise reduction is possible with a two pole low pass filter. Consistent with the many reported experiments on ear sensitivity (Fletcher-Munson, Robinson-Dadson etc.) we see that decreasing the bandwidth below 800 Hz is not particularly beneficial, and that once the bandwidth is above 8 kHz, there is little perceived increase in the audible noise level.

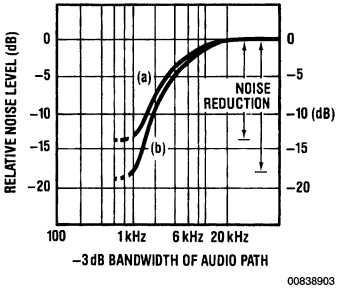


FIGURE 3. Reduction in Noise Level with Decreasing Bandwidth Audio Cassette Tape Noise Source—CCIR/ARM Weighted a) single pole low pass filter; b) two pole low pass filter

Auditory Masking

Obviously restricting the system bandwidth to less than 1 kHz in order to reduce the noise level will not be very satisfactory if the program material is similarly restricted, and this is where the second operating principle of DNR comes into play—whenever a sound is being heard it reduces the ability of the listener to hear another sound. This is known as auditory masking and is not a newly discovered phenomenon. It has been investigated for many years, primarily in connection with noise masking the ability of the listener to hear tones. The measurements have been made under steady state conditions and are summarized in the curves of *Figure 4.* Before discussing the shape of the curves and the conclusions that can be drawn it is worth looking at the scales employed. One difficulty that occurs in evaluating electronic equipment for audio is to be able to relate a

Auditory Masking (Continued)

quantity measured in electrical terms to the subjective stimulus (hearing) that it produces. For audio we are most interested in the conversion of electrical power into acoustic power. Since neither sound power nor sound intensity can be measured directly, we must use a related quantity known as sound pressure level (SPL) as our reference scale in *Figure 4*. The reference sound pressure, which approximates the threshold of hearing at 1 kHz is 0.0002 μBars (10^6 μBars = 1 Bar = 1 atmosphere). For this sound pressure scale, the level at which noise spectra will appear depends on the degree of amplification we are giving the desired signal to produce the maximum anticipated sound pressure. Typically a maximum preferred listening level is +90 dB (SPL) and the assumption is made that the total audio system, including speakers, is producing this SPL at the listener's ear when the recorded level (on tape, for example) corresponds to OVU. By comparing the amplitude of noise spectra with this OVU level signal we obtain the tape noise curves of *Figure 4* and can compare them with the audible noise threshold. Increasing the volume level by 10 dB (say), to compensate for a lower recording level will raise all the *noise spectra curves* by 10 dB. The audible noise threshold curve *does not change* with changes in SPL produced by twiddling the volume control (except after prolonged listening at high levels) since it depends on the characteristics of the ear and partly upon the masking effects of room noise.

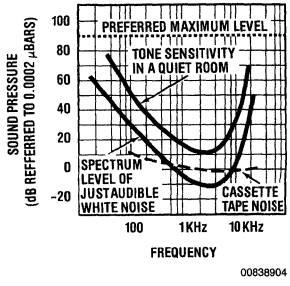


FIGURE 4. Relating the Spectral Sensitivity of the Ear to Tones and Audible Noise with the Noise Output Level from an Electric Source

The upper solid curve in *Figure 3* shows the sensitivity of the ear to pure tones in a typical room environment. Notice that tones at very low frequencies and at very high frequencies must be much louder than tones at mid-frequencies in order to be heard. The lower solid curve shows the spectrum level of just audible white noise. This curve is some 20 dB–30 dB below the tone spectrum because, unlike a single tone, noise has spectral components at all frequencies. Noise spectra at frequencies either side of a specific frequency contribute to the auditory sensation and thus can be heard at a lower threshold level. The two curves also imply that noise at or above the lower curve is able to completely mask single tones on the upper curve. Also sources with noise spectra above the lower curve are going to be audible. Clearly for cassette tapes we need to push the noise level down by another 10 dB if it is to be inaudible at preferred listening levels. If the tape is under-recorded and the volume level increased to compensate, yet more noise reduction is needed.

Reversing these conclusions to determine the ability of tones to mask the noise is not as easy. The hearing mechanism in the ear involves the basilar membrane which is approximately 30 mm long by 0.5 mm wide. The nerve endings giving the sensation of hearing are spaced along this membrane so that the ability to hear at one frequency is not masked at another frequency when the frequencies are well separated. White noise can excite the entire basilar membrane since it has spectral components at all frequencies. For any single frequency therefore, there will be a band of noise spectra capable of simultaneously exciting the nerve endings that are responding to the single frequency—and masking occurs. Conversely, a single tone at the upper curve level is quite incapable of masking noise spectra at the lower curve level snce it can only excite nerve endings at one particular point on the membrane. Noise spectra at frequencies on either side of the tone will still excite different parts of the membrane—and will be heard. Extremely high SPL's are required if single tones are to raise the audible noise threshold level and provide masking. As might be expected, the most effective tone frequencies are near the natural resonance of the ear—between 700 Hz and 1 kHz—and even then SPL's higher than 75 dB are needed for masking noise at 16 dBSPL. Fortunately for n.r. systems in general, including compandors, this applies only to pure tones. As soon as the tone acquires distortion, frequency modulation or transient qualities, or a mixture of tones is present, the masking abilities change dramatically. Typically music and speech, with high energy concentration around 1 kHz, can be regarded as excellent noise masking sources—up to 30 dB more effective than single tones. Therefore, recorded signals at an average level of 40–45 dB SPL will allow a full audio bandwidth to be used without the noise becoming audible. Signal levels lower than this can provide adequate masking, particularly if the source has employed dynamic range compression (FM broadcast for example), but speech and solo musical instruments are likely to betray noise modulation. These conclusions can apply equally to complementary noise reduction systems with the noise modulation effects depending on the degree of compression/expansion and the threshold level at which compression begins in the record chain.

Control Path Filtering and Transient Characteristics

If the signal source always maintained a relatively high SPL, then there wouldn't be any need for an n.r. system. However, when the program material SPL momentarily drops, the noise is unmasked and becomes audible. Much of the design effort involved in n.r. systems is in making the system track the program dynamics so that unmasking does not occur—at least not audibly. Similarly when the program material increases abruptly following a quiet passage, the n.r. system must respond quickly enough that the audio material is not distorted. For DNR, this means that the −3 dB corner frequency of the low pass filters inserted in each audio channel must increase quickly enough to pass all the music yet decrease back to around 1 kHz in the absence of music to reduce the noise. Matching low pass filters are used

Control Path Filtering and Transient Characteristics (Continued)

with a flat response below the cut-off frequency, and a smoothly decreasing response (–6 dB/octave) above the cut-off frequency, which can be varied from 800 Hz to over 30 kHz by the control signal.

A first approach to generating this control signal might be to use a filter and a gain block, driving a peak detector circuit. Since the amplitude spectra of musical instruments falls off with increasing frequency, and the characteristics of the ear are such that masking is most effective with sounds around 1 kHz, a reasonable filter for the control path might be low pass. This turns out *not* to be the case. To take a worse case situation (from the viewpoint of masking), when a French Horn is the dominant source, most of the energy is at frequencies below 1 kHz. If we were detecting this energy through a low pass filter, the control path would respond to the high amplitude and cause the audio filters to open to full bandwidth. Noise in the 2 kHz and above region would be promptly unmasked and audible. To avoid this, DNR uses a *highpass* filter in the control path. Below 1.6 kHz, the response falls at an 18 dB/octave rate. Above 1.6 kHz the filter response increases at a 12 dB/octave rate until a –3 dB corner frequency around 6 kHz is reached. After this the response is allowed to drop again and may include notches at 15.734 kHz (for television sound), or at 19 kHz to suppress the subcarrier pilot signal in FM stereo broadcasts. Returning to the case of the French Horn, the absence of high amplitude higher frequency harmonics means that the control signal will generate only a small increase in the audio bandwidth (depending on the sound level) and the noise will remain filtered out.

Contrasted with this, multiple instruments, or solo instruments such as the violin or trumpet, can have significant energy levels above 1 kHz which not only provide masking at higher frequencies but also require wider audio bandwidths for fidelity transmission in the audio path. Put another way, when the presence of high frequencies is detected in the control path we know that the audio bandwidth must be increased and that simultaneously large levels of signal energy are present in the critical masking frequency range. Since the harmonic amplitude can decrease rapidly with increase in frequency, the control sensitivity is raised at a 12 dB/octave rate up to 6 kHz to ensure that an adequate audio bandwidth is always maintained.

The attack and release times of the control path signal are also based on typical program dynamics and the characteristics of the human ear. If the detector cannot respond to the leading edge transient in the music, then distortion in the audio path will result from the initial loss of high frequency components. As might be expected, the rise time of any musical selection will depend on the instruments that are being played. An English Horn is capable of reaching 60% of its peak amplitude in 5 ms. For other instruments, rise-times can vary from 50 ms to 200 ms whereas a hand-clap can be as fast as 0.5 ms With this data in mind, DNR has been designed with an attack time of 0.5 ms. A distinction should be made in the effects of longer attack times for DNR compared to a companding noise reducer. If the compander does not respond immediately to an input transient, then instantaneous overload of the audio path can occur, with an overshoot amplitude as much as the maximum compression capability. If the system does not have adequate headroom, this overshoot can cause audible effects that last for longer than the period of the overshoot. The DNR filters simply cannot produce such an overshoot by failure to respond to the input rise-time. Since the ear has difficulty registering sounds of less than 5 ms duration, and can tolerate severe distortion if it lasts less than 10 ms, DNR has considerable flexibility in the choice of detector attack time.

Attack time is only half the story. Once the detector has responded to a musical transient, it needs to decay back to the quiescent output level at the cessation of the transient. A slow decay time would mean that for a period following the end of the transient, the system audio bandwidth would still be relatively wide. The noise in this bandwidth would be unmasked and a noise "burst" heard at the end of each musical transient. Conversely, if the release time is short to ensure a rapid decrease in bandwidth, a loss in musical "ambience" will occur with the suppression of harmonics at the end of a large signal transient. To avoid this, DNR uses a natural decay to within 10% of the final value in 60 ms. The inability of the ear to recover for 100 ms to 150 ms following a loud sound prevents the noise that is present (until the bandwidth is closed down) from being heard. Again a contrast with compander action is appropriate As the DNR detector control voltage decays, the bandwidth starts to diminish, Initially only high frequencies are affected and since the harmonic amplitude of the signal is also decaying rapidly, the audio is unaffected by this decrease in bandwidth. For a compander however, as the control voltage decays, the system gain is altered—which also affects the signal mid-band and low frequency components. Thus, as with attack times, DNR is substantially less affected by the choice of release times, permitting a high tolerance in component values.

Control Path Filtering and Transient Characteristics (Continued)

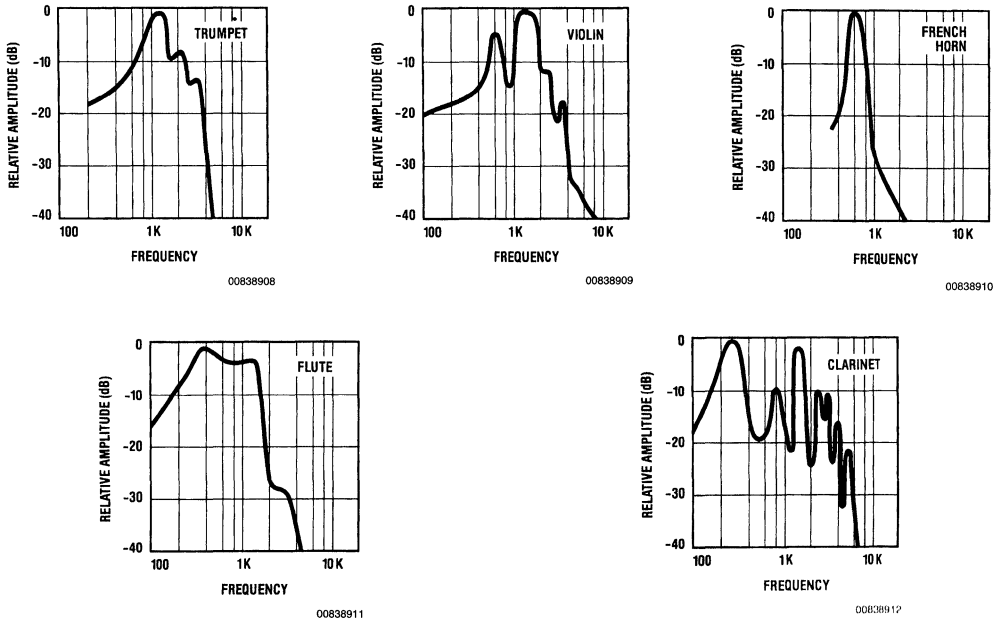


FIGURE 5. With Most Musical Instruments, As Well As Speech, Energy Is Concentrated around 1 kHz with a Rapid Fall-Off in Level above 6 kHz

Circuit Operation

The entire DNR system is contained within a single I/C and consists of two main functional signal paths. The audio path includes two low distortion low pass filters for a stereo audio source and the control path has a summing amplifier, variable gain filter amplifier and a peak detector. These functions are combined as shown in *Figure 7* which also shows the typical external components required for a complete n.r. system. By low distortion, we mean a filter that maintains the same cut-off slope and does not peak at the corner frequency as this frequency is changed. A 6 dB/octave filter slope was chosen since this provides a reasonable amount of noise reduction when the −3 dB frequency is less than 2 kHz and does not audibly affect the program material when the control path threshold is correctly set. It is possible to cascade the two audio filters—with a corresponding reduction in the size of the feedback capacitors to maintain the same operating frequency range—for a 12 dB/octave slope and up to 18 dB noise reduction. However, this steeper roll-off characteristic is better suited for program material that is relatively deficient in high frequency content, early recordings or video tapes for example.

Each audio filter consists of a variable transconductance stage driving an amplifier with capacitative feedback. For a fixed capacitor value, as the transconductance is changed by the control signal, the open loop unity gain frequency is changed correspondingly, giving a variable corner frequency low-pass filter. Of particular importance in the design is the need to avoid voltage offsets at the filter output caused by control action, and the ability of the input stage to accommodate large signal swings without introducing distortion. Output offset voltages are not necessarily proportional to the change in control voltage but will, in any case, be accompanied by a significant change in the program level. Extensive listening tests have shown that offset voltages 26 dB or more below the nominal signal input level will not be heard. Overload capability is dependent on the input stage current level and the available supply voltage, but even with an 8 VDC supply the LM1894 can handle signals more than 20 dB over the nominal input level without increased distortion.

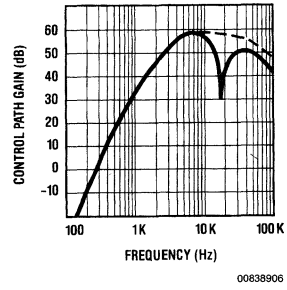


FIGURE 6. Control Path Characteristic (Including Optional 19 kHz Notch)

Circuit Operation (Continued)

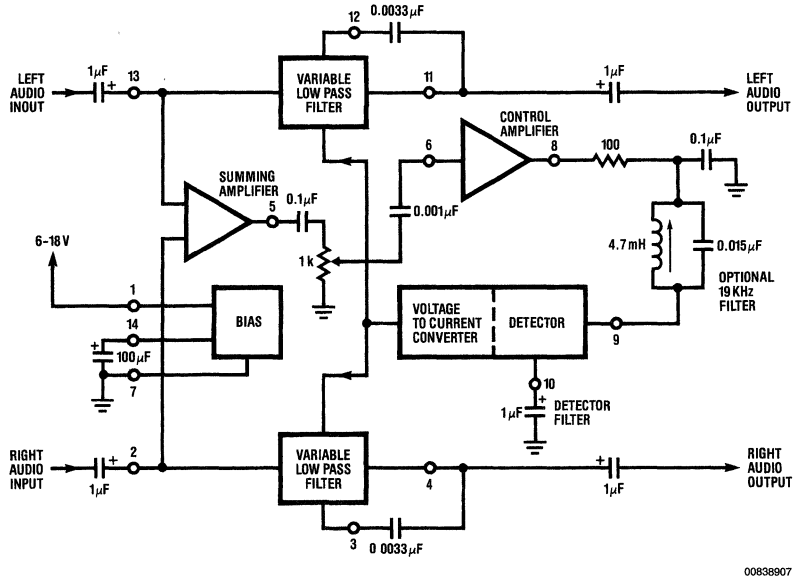


FIGURE 7. The DNR System with Recommended Circuit Values

A summing amplifier is used at the input to the control path so that both left and right audio channels contribute to the control signal. Both audio filters are controlled with the same signal yielding matched audio bandwidths and maintaining a stable stereo image. From the summing amplifier the signal passes through a high-pass filter formed by the coupling capacitor and a 1 kΩ potentiometer. These components produce an amplitude roll-off below 1.6 kHz to avoid control path overload and help prevent high level, low frequency signals (drum beats for example) from activating the detector unnecessarily. The potentiometer provides a means to adjust the overall gain of the control path such that the input source noise level is able to just cross the detector threshold and begin opening the audio bandwidth. The correct adjustment point is one that permits alternate use and bypass of the DNR system with no audible change in the program material—other than reduction of background noise. Also, on more difficult program material where the S/N ratio is so poor that masking is not completely effective, the potentiometer can be set to limit the maximum audio bandwidth so that noise pumping is avoided. For systems with a predictable noise level such as cassette recorders, the potentiometer can be replaced by two suitable fixed resistors. Further filtering of the control signal is done at the input to the gain stage and at the input to the detector stage. The input capacitors to these stages form high pass filters with internal resistors and are cascaded for a combined corner frequency (−3 dB) of around 6 kHz. Finally the detector attack and release times are set to the previously described values by an external capacitor connected to the peak detector output.

This paper has described the DNR non-complementary noise reduction system in terms of the functional blocks and the psychocoustic background necessary to understand the operating principles. For a more complete circuit description and practical details on the use of the LM1894, see the data sheet and AN386. Note that DNR is a trademark of National Semiconductor Corporation and that use of the DNR logo is by license agreement only.

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1) "Speech and Hearing in Communication", Fletcher, Von Nostrand, 1953.
2) "Absolute Amplitudes and Spectra of Certain Musical Instruments and Orchestras", Sixian et al, JASA, Vol. 2, #1.
3) "The Masking of Pure Tones and Speech by White Noise", Hawkins and Stevens, JAES, Vol. 22, #1.
4) "Loudness, Masking, and Their Relation to the Hearing Process and the Problem of Noise Measurement", Fletcher, JASA, Vol. 9, #4.
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8) A "Best Buy Denoiser", High Fidelity, May, 1981.
9) "On-chip Stereo Filter Cuts Noise Without Pre-processing Signal", Giles, Electronics, Aug., 1981.
10) "A Non-Complementary Audio Noise Reduction System", Giles and Wright, IEEE Trans on Consumer Electronics, Vol. CE-27, #4.

A Non-Complementary Audio Noise Reduction System

National Semiconductor
Application Note 386
Martin Giles

Introduction

The popularity of companding or complementary noise reduction systems is self-evident. Nearly all medium to high quality cassette tape decks include either Dolby®B or Dolby C type noise reduction. A scant few have different systems such as dbx or Hi-Com. The universal appeal of compandors to n.r system designers is the amount of noise reduction they can offer, yet one of the major reasons the Dolby B system gained dominance in the consumer marketplace is because it offered only a limited degree of noise reduction — just 10 dB. This was sufficient to push cassette tape noise down to the level where it became acceptable in good-quality applications, yet wasn't enough that undecoded playback on machines not equipped with a Dolby B system was unsatisfactory — quite the contrary, in fact. The h.f. boost on Dolby B encoded tapes when reproduced on systems with modest speakers was frequently preferred. Since companding systems are so popular, it is not unreasonable to ask, "why do we need another noise reduction system?"

For many of the available audio sources today, compandors are not a solution for audio noise. When the source material is not encoded in any way and has perceptible noise, complementary noise reduction is not possible. This includes radio and television broadcasts, the majority of video tapes and of course, older audio tape recordings and discs. The DNR™ single-ended n.r. system has been developed specifically to reduce noise in such sources A single-ended system, able to provide noise reduction where non previously existed, and which avoids compatability restraints or the imposition of yet another recording standard for consumer equipment, is therefore attractive.

The DNR system can be implemented by either of two integrated circuits, the LM1894 or the LM832, both of which can offer between 10 and 14 dB noise reduction in stereo program material. Although differing in some details (the LM832 is designed for low-signal, low-supply voltage applications) the operation of the integrated circuits is essentially the same. Two basic principles are involved; that the noise output is proportional to the system bandwidth, and that the desired program material is capable of "masking" the noise when the signal-to-noise ratio is sufficiently high. DNR automatically and continuously changes the system bandwidth in response to the amplitude and frequency content of the program. Restricting the signal bandwidth to less than 1 kHz reduces the audible noise and a special spectral weighting filter in the control path ensures that the audio bandwidth in the signal path is always increased sufficiently to pass any music that may be present. Because of this ability to dynamically analyze the auditory masking qualities of the program material, DNR does not require the source to be encoded in any special way for noise reduction to be obtained. This paper deals with the design and operating characteristics of the LM1894. For a more complete description of the principles behind the DNR system, refer to AN-384.

The DNR System Format

A block diagram showing the basic format of the LM1894 is shown in *Figure 1*. This is a stereo system with the left and right channel audio signals each being processed by a controlled cut-off frequency ($f_{-3\ dB}$) low-pass filter. The filter cut-off frequency can be continuously and automatically adjusted between 800 Hz and 35 kHz by a signal developed in the control path. Both audio inputs contribute to the control path signal and are used to activate a peak detector which, in turn, changes the audio filters' cut-off frequency. The audio path filters are controlled by the same signal for equally matched bandwidths in order to maintain a stable stereo image.

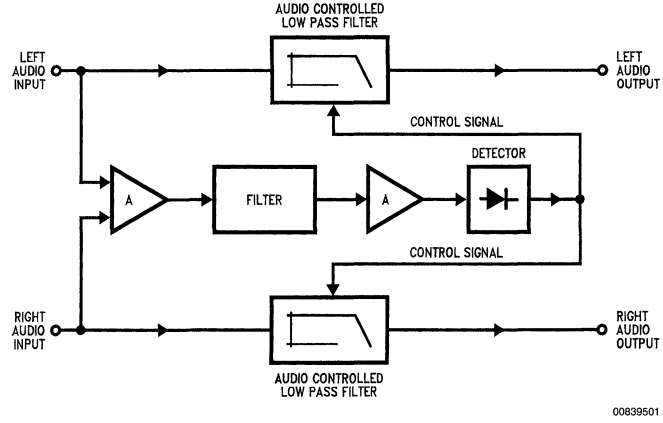
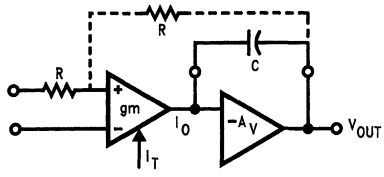
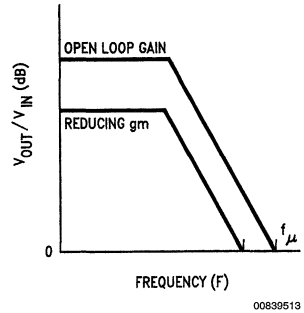


FIGURE 1. Stereo Noise Reduction System (DNR)

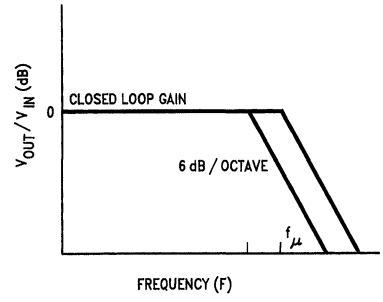
The DNR System Format (Continued)



(a) Variable Lowpass Filter



(b) Open Loop Response



(c) Closed Loop Response

FIGURE 2.

Variable Cut-Off Low Distortion Filters

By low distortion we mean a filter that has a flat response below the cut-off frequency, a smooth, constant attenuation slope above the cut-off frequency and does not peak at the cut-off frequency as this frequency is changed.

The circuit topology is shown in *Figure 2* (a) and is, in fact, very similar to the pole-splitting frequency compensation technique used on many integrated circuit operational amplifiers (see pp. 24–26 of "Intuitive I/C Op Amps" by T. M. Fredericksen). A variable transconductance (g_m) stage drives an amplifier configured as an integrator. The transconductance stage output current I_O is given by

$$I_o = g_m V_{in} \quad (1)$$

and if the second amplifier is considered ideal, then the voltage V_{out} is the result of I_o flowing through the capacitative reactance of C. Therefore we can write

$$V_{out} = \frac{I_o}{2\pi fC} \quad (2)$$

Combining *Equation (1)* and *Equation (2)* we have

$$\frac{V_{out}}{V_{in}} = \frac{g_m}{2\pi fC} \quad (3)$$

At some frequency, the open loop gain will fall to unity ($f=f_u$) given by

$$f_u = \frac{g_m}{2\pi C} \quad (4)$$

For a fixed value of capacitance, when the transconductance changes, then the unity gain frequency will change correspondingly as shown in *Figure 2* (b).

If we put dc feedback around both stages for unity closed loop gain, the amplitude response will be flat (or unity gain) until $f_u$is reached, and then will follow the open loop gain curve which is falling at 6 dB/octave. Since we control g_m, we can make $f_u$any frequency we desire and therefore have a controlled cut-off frequency low pass filter.

A more detailed schematic is given in *Figure 3* and shows the resistors R_f and R_i which provide dc feedback around the circuit for unity closed-loop gain (i.e. at frequencies below f_u). The transconductance stage consists of a differential pair T_1 and T_2 with current mirrors replacing the more conventional load resistors. The output current I_o to the integrator stage is the difference between $T_1$and T_2 collector currents.

For a differential pair, as long as the input differential voltage is small — a few millivolts — the g_m is dependent on the tail current I_T and can be written

$$g_m = \frac{q}{kT} \times \frac{I_T}{2}$$

$$\text{where } \frac{q}{kT} = \frac{1}{26\text{ mV}} \text{ @25°C} \quad (5)$$

Variable Cut-Off Low Distortion Filters (Continued)

For frequencies below the cut-off frequency, the amplifier is operating closed loop, and the dc feedback via Rf will keep the input differential voltage very small. However, as the input signal frequency approaches cut-off, the loop gain decreases and larger differential voltages will start to appear across the bases of T_1 and T_2. When this happens, the g_m is no longer linearly dependent on the tail current I_T and signal distortion will occur. To prevent this, two diodes D_1 and D_2 biased by current sources are added to the input stage. Now the signal current is converted to a logarithmically related voltage at the input to the differential pair T_1 and T_2. Since the diodes and the transistors have identical geometries and temperature excursions, this conversion will exactly compensate for the exponential relationship between the input voltage to T_1 and T_2 and the output collector currents. As long as the signal current is less than the current available to the diodes, the transconductance amplifier will have a linear characteristic with very low distortion.

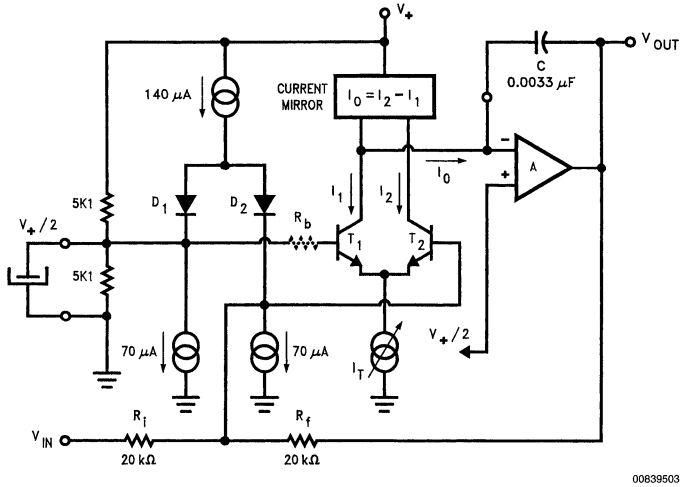


FIGURE 3. Variable Lowpass Filter with Distortion Correcting Diodes and Control Voltage Offset Compensation

Variable Cut-Off Low Distortion Filters (Continued)

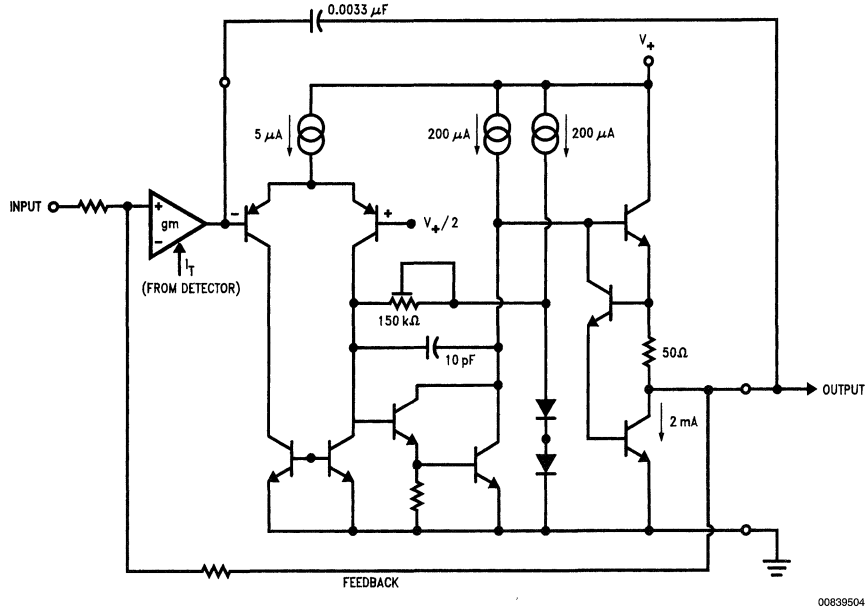


FIGURE 4. The OP AMP Output Stage of the LM1894

For the entire circuit, if $R_i = R_f = R$ and the diode dynamic resistance is r_e, we can write the transfer characteristic as

$$\frac{V_{out}}{V_{in}} = \frac{-1}{\left(1 + \frac{4\pi f C K\, 26 \times 10^{-3}}{I_T}\right)}$$

$$\text{where } K = \left(2 + \frac{R}{2r_e}\right) \qquad (6)$$

Therefore the pole frequency for C = 0.0033 μF is

$f_u = I_T/4\,\pi\, 26 \times 10^{-3} CK = I_T \times 33.2 \times 10^6$

for f_u = 1 kHz, I_T = 33.2 μA

for f_u = 35 kHz, I_T = 1.1 mA

In operation, the transconductance stage current I_T for the LM1894 will vary between the levels given above in response to the control path detected voltage. Notice that with the circuit values given in *Figure 3* the maximum output voltage swing at the cut-off frequency is about IV_{rms} (use equation 2 and put $I_O = I_T$ = 33 μA) and this is specified in the LM1894 data sheet as the input voltage for 3% THD. This is, of course, the condition for minimum bandwidth when noise only is normally present at the input. When signals are simultaneously present causing the audio bandwidth to increase out to 35 kHz, the transconductance stage current is over 1 mA, allowing signal swings at 1 kHz (theoretically) of over 34 Vrms. Practically, at maximum bandwidth the output swing is determined by the output stage saturation voltages which are dependent on the supply voltage (see *Figure 4*). With a 15 V_{DC} supply, the LM1894 can handle well over 4 Vrms.

Variable Cut-Off Low Distortion Filters (Continued)

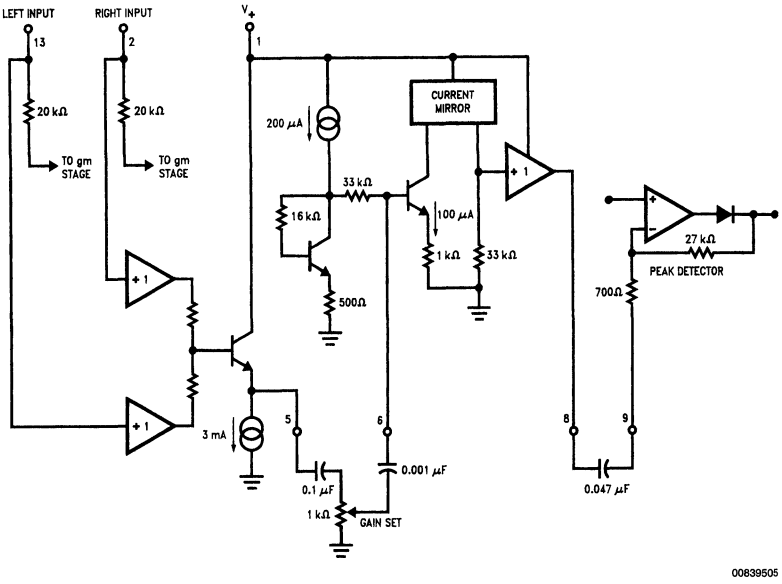


FIGURE 5. Control Path Amplifiers and Filters

While there are other circuit topologies that can be used to obtain a variable cut-off low pass filter, this design has certain advantages, especially when it comes to avoiding control feedthrough. Control feedthrough is the name given to voltage offsets that can occur in the audio path as the transconductance stage current changes. The audible effect is a low level "bacon frying" noise or pops as the bandwidth changes. To prevent such voltage offsets occurring, the differential stage T_1 and T_2, the current mirrors and the diodes are arranged to provide good tracking over the entire range of the bandwidth control current I_T. Because the transconductance stage is driving the inverting input to an operational amplifier — a virtual ground — there will be no voltage swing at this node. This eliminates possible offset voltages from output impedance changes in the current mirror and T_1 collector caused by different operating currents. Last, but not least, a source of offset voltages are the base currents of T_1 and T_2. Because the transistors have a finite current gain, when the tail current I_T is increased, these base currents must increase slightly. T_1base current is provided by the reference voltage ($V_+/2$), but T_2 base current must come via the feedback resistor R_f. This current is not normally available from D_2 because the feedback loop is holding T_1 and T_2 base voltages equal. By adding the resistor R_b in series with T_1 base, a compensating offset voltage is produced across the input diodes. This reduces the current in D_1 slightly and increases the current in D_2 correspondingly, allowing it to supply the increased base current requirement of T_2.

The Control Path

The purpose of the control path is to ensure that the audio bandwidth is always sufficiently wide to pass the desired signal, yet in the absence of this signal will decrease rapidly enough that the noise also present does not become audible. In order to do this, the control path must recognize the masking qualities of the signal source and the detector stage must be able to take advantage of the characteristics of the human ear so that audible signal distortion or un-masking does not occur.

Figure 5 shows a block diagram of the control path including the external components. A straight-forward summing amplifier combines the left and right channel inputs and acts as a buffer amplifier for the gain control. Because the noise level for signal sources can be different — cassette tapes are between −50 dB and −65 dB (depending on whether Dolby B encoding is employed) and FM broadcast noise is around −45 dB to over −75 dB (depending on signal strength) — the control path gain is adjusted such that a noise input is capable of just increasing the audio bandwidth from its minimum value. This ensures that any program material above the noise level increases the audio bandwidth so that the material is passed without distortion. Setting the potentiometer (or an equivalent pair of resistors) will be described in more detail later.

The gain control potentiometer is also part of the DNR filter characteristic derived from auditory masking considerations — see AN384. Combined with a 0.1 μF coupling capacitor, the total resistance of the potentiometer will cause a signal attenuation below 1.6 kHz.

$$\text{i.e. } f_1 = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 10^3 \times 0.1 \times 10^{-6}} = 1.6 \text{ kHz}$$

This helps to prevent signals with a high amplitude but no high frequency content above 1 kHz — such as a bass drum — from activating the control path detector and unnecessarily opening the audio bandwidth. For signals that do have

The Control Path (Continued)

a significant high frequency content (predominantly harmonics), the control path sensitivity is increased at a 12 dB/octave rate. This rapid gain in sensitivity is important since the harmonic content of program material typically falls off quickly with increasing frequency. The 12 dB/octave slope is provided by cascading two RC high pass filters composed of the coupling capacitors to the control path gain stage and detector stage and the internal input resistors to these stages. Individual corner frequencies of 5.3 kHz and 4.8 kHz respectively are used, with a combined corner frequency around 6 kHz. Above 6 kHz the gain can be allowed to decrease again since the signal energy content between 1 kHz and 6 kHz (the critical masking frequency range) will have already caused the audio bandwidth to extend beyond 30 kHz, allowing passage of any high frequency components in the audio path.

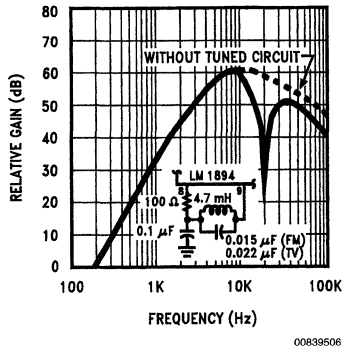


FIGURE 6. Control Path Frequency Response

Under some circumstances, not normal to music or speech, the source can contain relatively high level, high frequency components which are not necessarily accompanied by large levels of low frequency signal energy providing noise masking. These are spurious components such as the line scan frequency in a television receiver (15.734 kHz) or subcarrier signals such as the 19 kHz pilot tone in FM stereo broadcasting. Although both these components should be low enough to be inaudible in the audio path, their presence in the control path could cause a change in the minimum bandwidth and hence the amount of available noise reduction. Since these unwanted components are at frequencies higher than the desired control path frequency range, they are easily accommodated by including a notch filter in the control path at the specified frequency. A resonant L-C circuit with a Q of 30 will attenuate 19 kHz by over 28 dB. If a 10% tolerance 0.015µF capacitor is used, the coil can be a fixed 4.7 mH inductance. For 15.734 kHz a 0.022 µF capacitor is needed. When those frequency components are not present (i.e. in cassette tapes) the L-C circuit is eliminated and the gain amplifier and detector stage are coupled together with a single 0.047 µF capacitor.

Apart from providing the proper frequency response the control path gain must be enough to ensure that the detector threshold can be reached by very low noise input levels. The summing amplifier has unity gain to the sum of the left and right channel inputs and the necessary signal gain of 60 dB is split between the following gain amplifier and the detector stage. For the gain amplifier

$$A_V = 33 \times 10^3/(r_e + 10^3) = 26.2$$
$$= 28.4 \text{ dB}$$

For the detector stage, the gain to negative signal swings is

$$A_V = 27 \times 10^3/700 = 38.6 = 31.7 \text{ dB}$$

With over 60 dB gain and typical source input noise levels, the gain potentiometer will normally be set with the wiper arm close to the ground terminal.

The Detector Stage

The last part of the LM1894 to be described is the detector stage which includes a negative peak detector and a voltage to current converter. As noted earlier, the input resistance of the detector, together with the input coupling capacitor, forms part of the control path filter. Similarly the output resistance from the detector and the gain setting feedback resistor help to determine the detector time constants. With a pulse or transient input signal, the rise time is 200 µs to 90% of the final detected voltage level. Actual rise-times will normally be longer with the detector tracking the envelope of the combined left and right channel signals after they have passed through the control path filter.

An interesting difference to compandor performance can be demonstrated with a 10 kHz tone burst. Since the LM1894 detector responds only to negative signal peaks, it will take about four input cycles to reach 90% of the final voltage on the detector capacitor (this is the 500 µs time constant called out in the data sheet). After the first two cycles the audio bandwidth will have already increased past 10 kHz and a comparison of the input and output tone bursts will show only a *slight* loss in amplitude in these initial cycles. A compandor, however, usually cannot afford a fast detector time constant since the rapid changes in system gain that occur when a transient signal is processed can easily cause modulation products to be developed which may not be treated complementarily on playback, Therefore there is a time lag before the system can change gain, which may be to the maximum signal compression (as much as 30 dB depending on the compandor type). Failure to compress immediately at the start of the tone burst means that an *overshoot* is present in the signal which can be up to 30 dB higher than the final amplitude. To prevent this overshoot from causing subsequent amplifier overload (which can last for several times the period of the overshoot), clippers are required in the signal path, limiting the dynamic range of the system. Obviously, the LM1894 does not need clippers since no signal overshoots in the audio path are possible.

When the input signal transient decays, the diode in the detector stage is back biassed and the capacitor discharges primarily through the feedback resistor and takes about 60 ms to reach 90% of the final value.

$$T = RC \times 2.3 = 27 \times 10^3 \times 1 \times 10^{-6} \times 2.3$$
$$= 62.1 \text{ ms}$$

The decay time constant is required to protect the reverberatory or "ambience" qualities of the music. For material with a limited high frequency content or a particularly poor S/N ratio, some benefit can be obtained with a faster decay time—a resistor shunted across the detector capacitor will do this. Resistors less than 27 kΩ should not be used since

The Detector Stage (Continued)

very fast decay times will permit the detector to start tracking the signal frequency. For signal amplitudes that are not producing the full audio bandwidth, this will cause a rapid and audible modulation of the audio bandwidth.

Bypassing the System

Sometimes it is necessary or desirable to bypass the n.r. system. This will allow a direct and instantaneous comparison of the effect that the system is having on the program material and will assist in arriving at the correct setting for the control path gain potentiometer. This facility is not practical with compandors unless unencoded passages occur in the program material. Also, should the action of the compandor become more objectionable than the noise in the original material, there is no way of switching the n.r. system off.

One way of bypassing is to simply use a double pole switch to route the signals around the LM1894. This physically ensures complete bypassing but does present a couple of problems. First, there may be a level change caused by the different impedances presented to the following audio stages when switching occurs. Second, the signal now has to be routed to the front panel where the switch is located, perhaps calling for shielded cable.

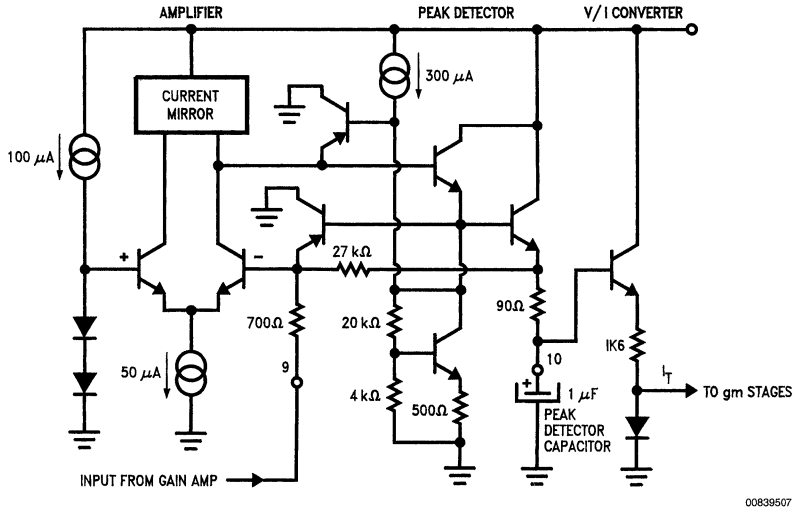
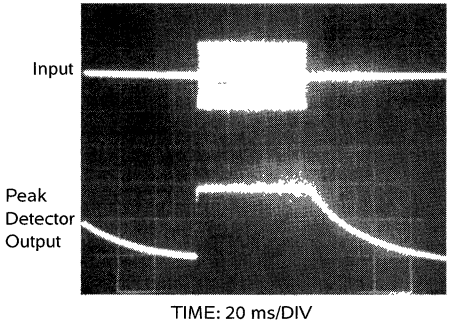


FIGURE 7. Peak Detector and Voltage to Current Converter

Peak Detector Response, 500 mV/Div



Audio Output Response, 10 kHz Tone Burst

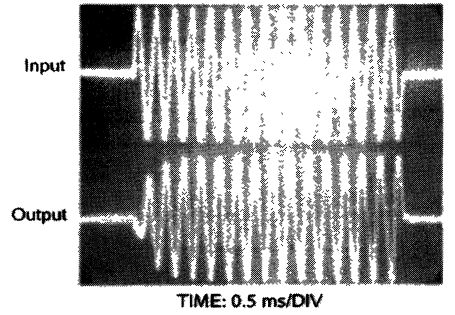


FIGURE 8.

A different technique, which avoids these problems, is to switch the LM1894 permanently into the full audio bandwidth mode. Since this provides a high S/N ratio path and low distortion the impact on the signal is minimal. Two methods can be used to switch the LM1894 audio bandwidth fully open, both with a single pole switch that is not in the audio path. Simply grounding the input of the peak detector amplifier will generate the maximum bandwidth control current

Bypassing the System (Continued)

and simultaneously prevent any control signals reaching the detector. Usually this is more than adequate since the maximum audio bandwidth is 34 kHz, but in some cases the 1 dB loss at 17 kHz produced by the single pole audio filters may not be desired. *Figure 9* shows a way to increase the audio bandwidth to 50 kHz (−1 dB at 25 kHz) by pulling up the detector capacitor to the reference voltage level ($V_+/2$) through a 1 kΩ resistor. This method is useful only for higher supply voltage applications. To increase the bandwidth significantly the detector capacitor must be pulled up to around 5V (V_+ >10V). Although a separate voltage source other than the reference pin could be used when $V_+$is less than 10V, this can cause an internal circuit latch-up if the voltage on the detector increases faster than the reference voltage at initial turn-on.

General System Measurements and Precautions

For most applications the external components shown in *Figure 9* will be required. In fact, the only recommended deviation from these values is the substitution of an equivalent pair of fixed resistors for the gain setting potentiometer. Location of the LM1894 in the audio path is important and should be prior to any tone or volume controls. In tape systems, right after the playback head pre-amplifier is the best place, or at the stereo decoder output (after de-emphasis and the multiplex filter) in an FM broadcast receiver. The LM1894 is designed for a nominal input level of 300 mVrms and sources with a much lower pre-amplifier output level will either require an additional gain block or substitution of the LM832 which is designed for 30 mVrms input levels.

The same circuit as *Figure 9* can be used for measurements on the I/C performance but, as with any other n.r. system, care in intepretation of the results may be necessary. For example, while the decay time constant for a tone burst signal is pretty constant, the attack time will depend on the tone frequency.

Sometimes separation of the audio path input and the control path is required, particularly when the frequency response or the THD with low input signal levels is being measured. If the audio and control paths are not separated then a typical audio system measurement of the frequency response will not appear as expected. This is because the control path frequency response is non-linear, exhibiting low sensitivity at low frequencies. When a low level input signal is swept through the audio frequency range, at low frequencies the audio −3 dB bandwidth will be held at 1 kHz, and the audio path signal will fall in amplitude as the signal goes above 1 kHz. As the signal frequency gets yet higher, the increasing sensitivity of the control path will allow the detector to be activated and the audio path −3 dB frequency starts to overtake the signal frequency. This causes the output signal amplitude to increase again giving the appearance that there is a dip in the audio frequency response around 1–2 kHz. It is worth remembering at this point that the audio path frequency response is always flat below some corner frequency and rolls off at 6 dB/octave above this frequency. In normal operation this corner frequency is the result of the aggregrate control path signals in the 1 kHz to 6 kHz region and not the result of a single input frequency. To properly measure the frequency response of the audio path at a particular signal input frequency and amplitude, the control path input is separated by disconnecting C_5 from Pin 5 and injecting the signal through C_5 only. Then, a separate swept frequency response measurement can be made in the audio path. Similarly measurements of THD should include separation of the audio and control path inputs.

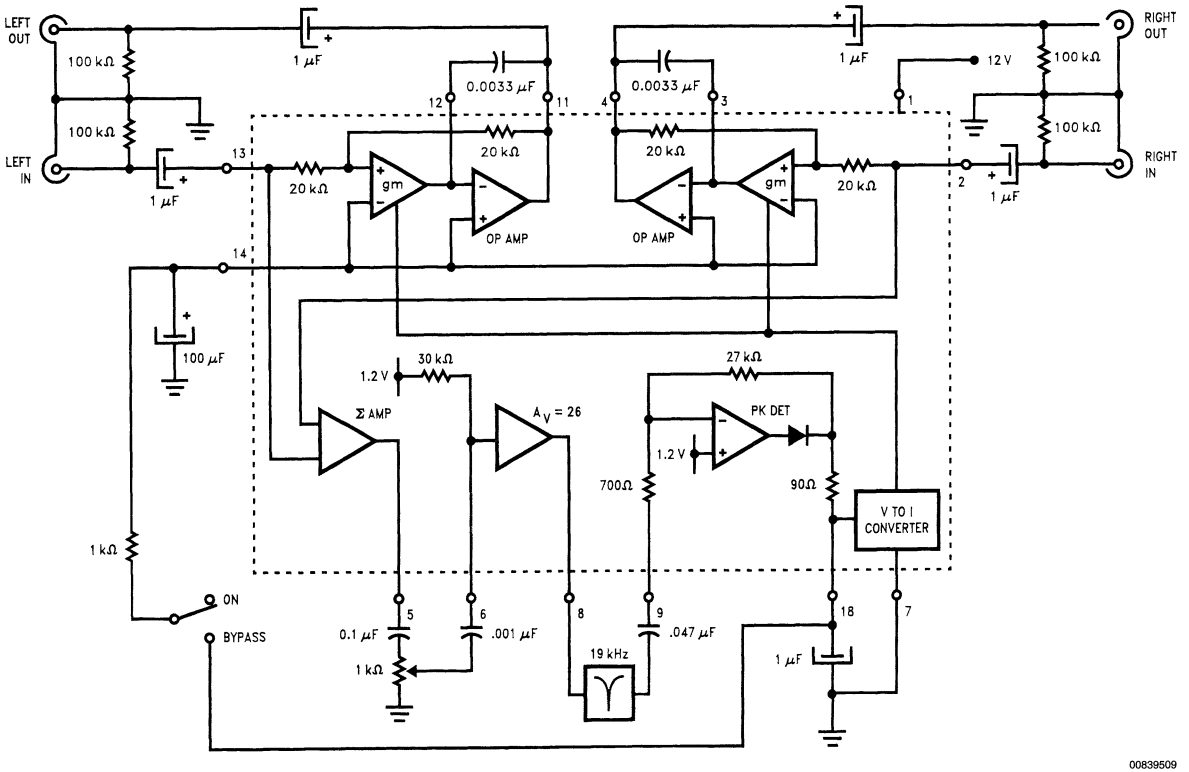


FIGURE 9. Complete Stereo Noise Reduction System

Pitfalls - Or What to Listen For

Many people are understandably wary of non-complementary n.r. systems since there is no perfect means for distinguishing between the desired signal and noise. A thorough understanding of the psycho-acoustic basis for noise masking will go a long way to allaying these fears, but a much simpler method is to listen to a variety of source material with a DNR system being switched in and out. Even so, improper implementation of the LM1894—wrong location in the audio path changing either the level or frequency response of the source—or incorrect external component values, or the wrong sensitivity setting, can all strongly affect the audio in an undesired way. Sometimes, unhappily, the source is really beyond repair and some compromise must be made. Phonograph discs with bad scratches may require special treatment (a click and pop remover) and some older tape recordings may show some or all of the following problems.

1. Pumping:

   Incorrect selection of the control path bandwidth external components can result in an audible increase in noise as the input level changes. This is most likely to be heard on solo instruments or on speech. Sometimes the S/N rate is too poor and masking will not be completely effective - i.e., when the bandwidth is wide enough to pass the program material, the increase in noise is audible. Cutting down on the pumping will also affect the program material to some extent and judgement as to which is preferable is required. Sometimes a shorter decay time constant in the detector circuit will help, especially for a source which always shows these characteristics, but for better program material a return to the recommended detector characteristics is imperative.

2. High Frequency Loss:

   This can be caused by an improper control path gain setting—perhaps deliberate because of the source S/N ratio as described above—or incorrect values for the audio path filter capacitors. Capacitors larger than the recommended values will scale the operating bandwidth lower, causing lower −3 dB corner frequencies for a given control path signal. Return to the correct capacitor values and the appropriate control path gain setting will *always* ensure that the h.f. content of the signal source is preserved.

3. Apparent High Frequency Loss:

   The ability to instantaneously A/B the source with and without noise reduction can sometimes exhibit an apparent loss of h.f. signal content as the DNR system operates. This is most likely to happen with sources having an S/N ratio of less than 45 dB and is a subjective effect in that the program material probably does not have any significant h.f. components. It has been reported several times elsewhere that adding high frequency noise (hiss) to a music signal with a limited frequency range will seem to add to the h.f. content of the music. Trying sources with a higher S/N ratio that do not demonstrate this effect can re-assure the listener that the DNR system is operating properly. Alternatively a control path sensitivity can be used that leaves the audio bandwidth slightly wider, preserving the "h.f. content" at the expense of less noise reduction in the absence of music.

4. Sensitivity Setting:

   Since this is the only adjustment in the system, it is the one most likely to cause problems. Improper settings can cause any of the previously described problems. Factory pre-sets can (and are) used, but only when the source is well defined with known noise level. For the user who intends to noise reduce a variety of sources, the control path gain potentiometer is required and should be adjusted for each application. A bypass switch is helpful in this respect since it allows rapid A/B comparison. Another useful aid is a bandwidth indicator, shown in *Figure 10*. This is simply an LED display driver, the LM3915, operating from the voltage on the detector filter capacitor at Pin 10 of the LM1894. The LM3915 will light successive LEDs for each 3 dB increase in voltage. The resistor values are chosen such that the capacitor voltage when the LM1894 is at minimum audio bandwidth, is just able to light the first LED, and a full audio bandwidth control signal will light the upper LED. Experience will show that adjusting the sensitivity so that the noise in the source (no signal is present) is just able to light the second LED, will produce good results. This display also provides constant reassurance that the system audio bandwidth really is adequate to process the music. A simpler detector, using a dual comparator and a couple of LEDs can be constructed instead, with threshold levels selected to show the correct sensitivity setting, minimum bandwidth, maximum bandwidth or some intermediate bandwidth as desired.

Pitfalls - Or What to Listen For (Continued)

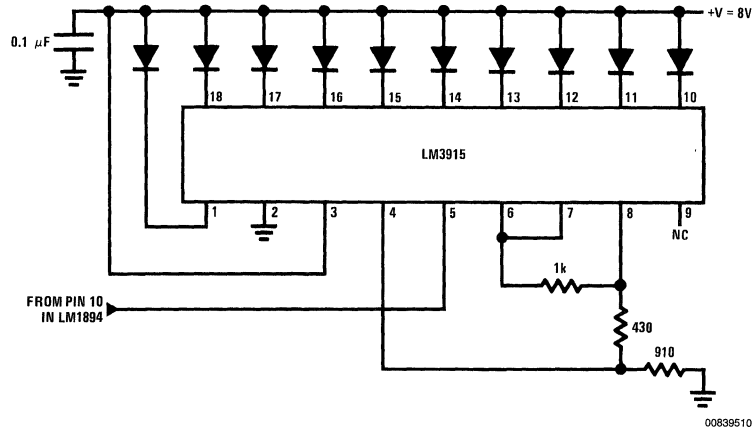


FIGURE 10. Bar Graph Display of Peak Detector Voltage

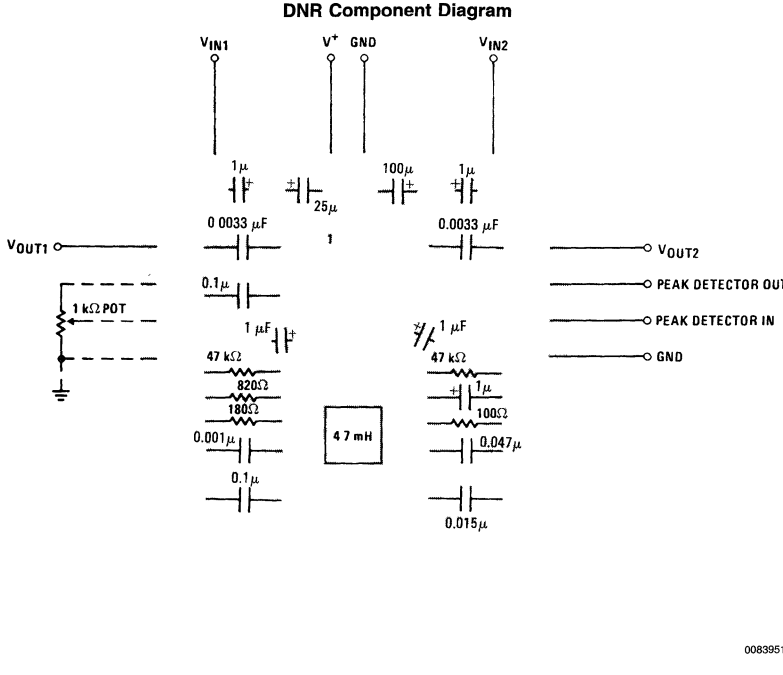


FIGURE 11. Printed Circuit Layout

DNR™ Applications of the LM1894

National Semiconductor
Application Note 390
Martin Giles
Kerry Lacanette

Introduction

The operating principles of a single-ended or non-complementary audio noise reduction system, DNR, have been covered extensively in a previous application note AN384, Audio Noise Reduction and Masking. Although the system was originally implemented with transconductance amplifiers (LM13600) and audio op-amps (LM387), dedicated I/Cs have since been developed to perform the DNR function. The LM1894 is designed to accommodate and noise reduce the line level signals encountered in video recorders, audio tape recorders, radio and television broadcast receivers, and automobile radio/cassette receivers. A companion device, the LM832, is designed to handle the lower signal levels available in low voltage portable audio equipment. This note deals chiefly with the practical aspects of using the LM1894, but the information given can also be applied to the LM832.

The Basic DNR Application Circuit

At the time of writing, the LM1894 has already found use in a large variety of applications. These include:

AUTOMOTIVE RADIOS
TELEVISION RECEIVERS
HOME MUSIC CENTERS
PORTABLE STEREOS (BOOM BOXES)
SATELLITE RECEIVERS
AUDIO CASSETTE PLAYERS
AVIONIC ENTERTAINMENT SYSTEMS
HI-FI AUDIO ACCESSORIES
BACKGROUND MUSIC SYSTEMS
ETC.

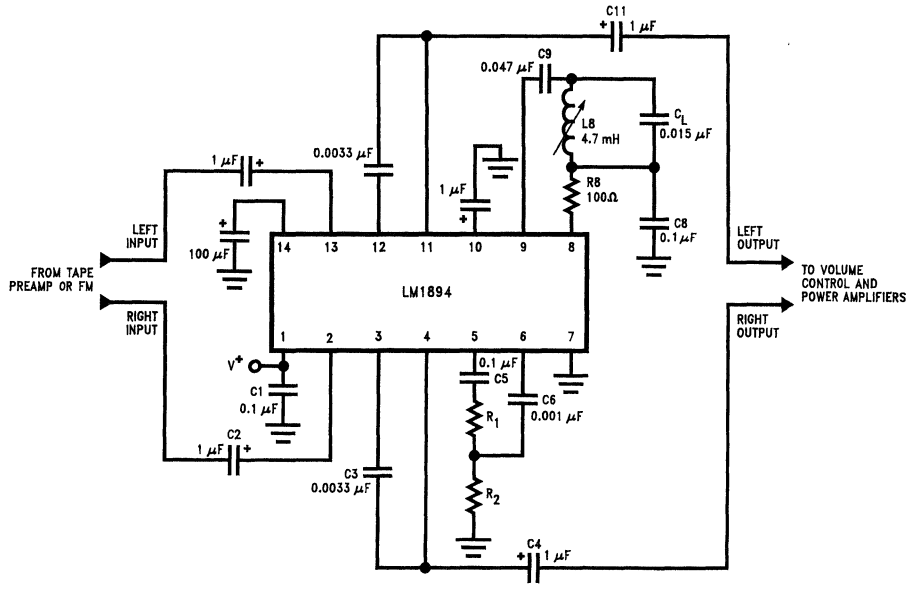
In the majority of these applications the circuit used is identical to that shown in *Figure 1*, and this is the basic stereo Dynamic Noise Reduction System. Although a split power supply can be used, a single positive supply voltage is shown, with ac coupled inputs and outputs common in many consumer applications. This supply voltage can be between 4.5 V_{DC} and 18 V_{DC} but operation at the higher end of the range (above 8 V_{DC}) is preferred, since this will ensure adequate signal handling capability. The LM1894 is optimized for a nominal input signal level of 300 mVrms but with an 8 V_{DC} supply it can handle over 2.5 Vrms at full audio bandwidth. Smaller nominal signal levels can be processed but below 100 mVrms there may not be sufficient gain in the control path to activate the detector with the source noise. In this instance, and where battery powered operation is desired, the LM832 is a better choice. The LM832 has identical operating principles and a similar (but not identical) pin-out. It is optimized for input levels around 30 mVrms and a supply voltage range from 1.5 V_{DC} to 9.0 V_{DC}.

The capacitors connected at Pins 12 and 3 determine the range of –3 dB cut off frequencies for the audio path filters. Increasing the capacitor value scales the range downward – the minimum frequency becomes lower and the maximum or full bandwidth frequency will decrease proportionally. Similarly, smaller capacitors will raise the range.

$$f_{-3\ dB} = I_T/9.1C\ (I_T = 33\ \mu A\ MIN)\ (= 1.05\ mA\ MAX) \quad (1)$$

For normal audio applications the recommended value of 0.0033 µF should be adhered to, producing a frequency range from 1 kHz to 35 kHz.

The Basic DNR Application Circuit (Continued)



R1 + R2 = 1 kΩ total

FIGURE 1. Complete DNR Application Circuit

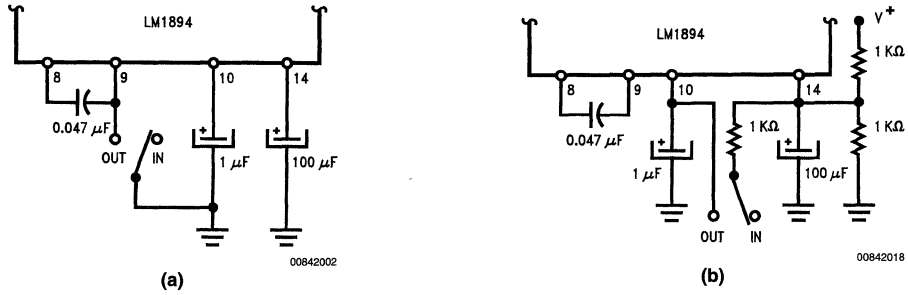


FIGURE 2. Two Methods of DNR IN/OUT Switching

The two resistors connected at Pin 5 set the overall control path gain, and hence the system sensitivity. A lower tap point will decrease the sensitivity for high signal level sources, and a higher tap point will accommodate lower level sources. For purposes of initial calibration it is best to replace the resistors with a 1 kΩ potentiometer (the wiper arm connecting through C_6 to Pin 6), and follow the procedures outlined below. Once the correct adjustment point has been found, the position of the wiper arm is measured and an equivalent pair of resistors are used to replace the potentiometer. This, of course, can be done only if the source has a relatively fixed noise floor—the output from an audio cassette tape for example. For an add-on audio accessory the potentiometer should be retained as a front panel control to allow adjustment for individual sources. Use of DNR with multiple sources is described later.

System Calibration

System calibration can be performed in a number of ways. With the source connected play a blank but biased section of the cassette tape. Set the potentiometer so that the wiper arm is at ground and then steadily rotate it until a slight increase in the output noise level is heard. Alternatively, with source program material present, set the potentiometer with the wiper arm connected to the Pin 5 end of the slider and again rotate until the high frequency content of the program material appears to begin to be attenuated. Then return the potentiometer wiper slightly towards Pin 5 so that the music is unaffected.

A third method of adjustment can be done with an oscilloscope monitoring the voltage on the control path detector filter capacitor, Pin 10. This will show a steady dc voltage around 1V while the wiper arm of the potentiometer is at ground. As the wiper arm is rotated, this voltage will start to increase. About 200 mV above the quiescent value will usually be the right point. Note that this will not be a steady dc voltage but a random peak, low amplitude sawtooth waveform caused by peak detection of the source noise in the control path.

Whatever method is used to determine the potentiometer setting, this setting should be confirmed by listening to a variety of programs and comparing the audio quality while switching DNR in and out of the circuit. This is easily accomplished by grounding Pin 9 which will disable the control path and force the audio filters to maximum bandwidth, *Figure 2(a)*. Also shown is a second method of ON/OFF switching that gives an increased maximum bandwidth over that obtained in normal operation. Although the switch is not a required front panel control it can be an important feature. Unlike compander systems, DNR can be switched out leaving the source completely unprocessed in any way. With a switch, the user can always be assured that the noise reduction is not affecting the program material.

Apart from the basic circuit shown in *Figure 1*, all applications of the DNR system have another feature in common–the location of the LM1894 in the signal chain. As *Figure 3* shows, the LM1894 is *always* placed right after the signal source pre-amplifier and *before* any circuit that includes user adjustable controls for volume or frequency response. The reasons for this are obvious. If the gain of the signal amplifier preceding DNR is changed arbitrarily, the noise input level to the LM1894 will not be at the correct point to begin activation of the audio path filters. Either reduced noise reduction will be obtained, or the high frequency content of the program material will be affected. A change in system gain prior to the LM1894 requires a corresponding change in the control path threshold sensitivity. Similarly modifying the frequency response, by heavy boost or cut of the mid to high frequencies, will have the same effect of changing the required threshold setting—apart from modifying the masking qualities of the program material.

How Much Noise Reduction?

The actual sensitivity setting that is finally used, and the amount of noise reduction that is obtained, will depend on a number of factors. As the data sheet for the LM1894 and other application notes have explained in some detail, the noise reduction effect is obtained by audio bandwidth restriction with a pair of matched low-pass filters. A CCIR/ARM (Note 1) weighted noise measurement is used so that the measured improvement obtained with DNR correlates well to the subjective impression of reduced noise. This is another way of stating that the source noise spectrum level versus frequency characteristic can have a large impact on how "noisy" we judge a source to be—and concomitantly how much of the "noisiness" can be reduced by decreasing the audio bandwidth. Fortunately most of the audio noise sources we deal with are smooth although not necessarily flat, resembling white noise. The weighting characteristic referred to above generally gives excellent correlation. For example, if the source –3 dB upper frequency limit is only 2 kHz (an AM radio), reducing the audio path bandwidth down to 800 Hz will improve the S/N ratio by only 5 to 7 dB. On the other hand, if the source bandwidth exceeds at least 8 kHz then from 10 dB to 14 dB noise reduction can be obtained. Of course, it is always worth remembering that this is the reduction in the source noise—any noise added in circuits *after* the LM1894 may contribute to the audible output and prevent the full noise reduction effect. To see how easily this can happen, we will consider the noise levels at various points in a typical automotive radio using an I/C tone and volume control, and an I/C power amplifier, both with and without noise reduction of the cassette player.

Note 1: See pp 2–9 to 2–10, Audio Handbook, National Semiconductor 1980

How Much Noise Reduction? (Continued)

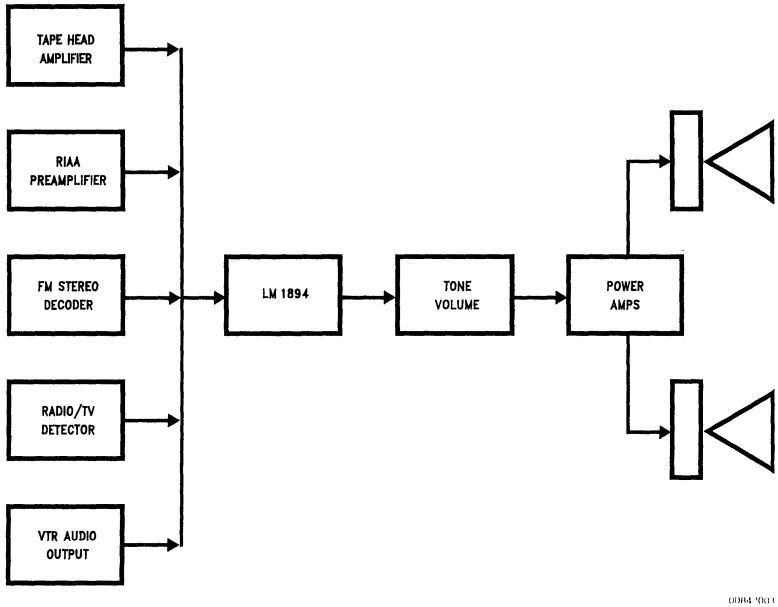
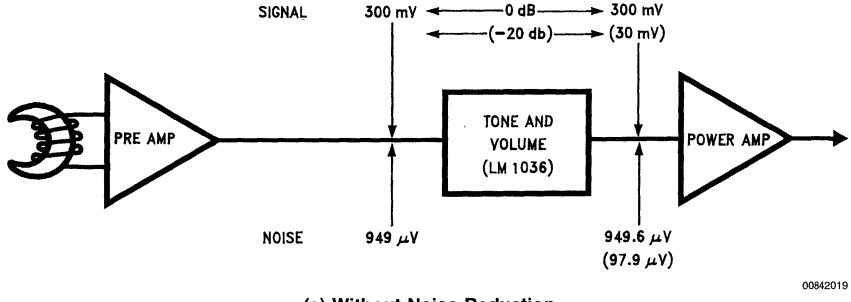
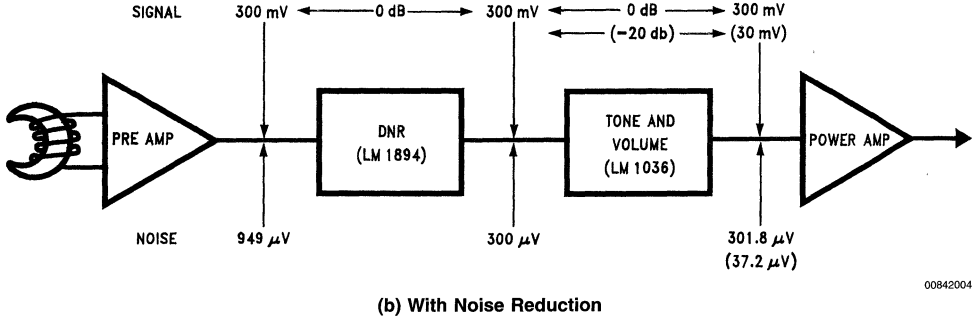


FIGURE 3. Location of DNR in Audio Systems



(a) Without Noise Reduction



(b) With Noise Reduction

FIGURE 4. Signal and Noise Levels in the Audio Path

How Much Noise Reduction?

(Continued)

If we assume that the tape head pre-amplifier gain is such that the nominal output level (corresponding to O"VU") is 300 mVrms, then for a typical cassette tape the noise will be 50 dB lower, or 949 µV. The gain of the tone and volume control (an LM1036) is unity or 0 dB at maximum volume setting, with an output noise level of 33 µV with no signal applied. With the tape pre-amplifier connected, the output noise from the LM1036 will be V_n where

$$V_n = 10^{-6}\sqrt{(33)^2 + (949)^2} = 949.6\ \mu V \quad (2)$$

Clearly, the LM1036 has caused an insignificant increase in the background noise level (0.006 dB). Even when the volume control is set at –20 dB overall gain, the LM1036 intrinsic noise level is 22 µV. The tape noise level is now 94.9 µV (–20 dB) and the output noise V_n is

$$V_n = 10^{-6}\sqrt{(22)^2 + (94.9)^2} = 97.4\ \mu V \quad (3)$$

Once more an insignificant contribution on the part of the LM1036 (0.23 dB).

Now we add noise reduction between the tape head amplifier and the LM1036. Usually this will mean over 10 dB reduction in the tape noise so that the input of the LM1036 sees 300 µV noise At 0 dB gain we have

$$V_n = 10^{-6}\sqrt{(33)^2 + (300)^2} = 301.8\ \mu V \quad (4)$$

But at –20 dB

$$V_n = 10^{-6}\sqrt{(22)^2 + (30)^2} = 37.2\ \mu V \quad (5)$$

When we compare the results of *Equation (3)* and *Equation (5)* we see that at –20 dB gain setting we are getting only 8.4 dB noise reduction compared to 10 dB at maximum gain! Since the volume control is not normally set to maximum, this is a significant loss.

Active tone and volume controls are not the only circuits that can contribute to a loss in noise reduction. Most modern automotive radios use I/C power amplifiers delivering in excess of 6 watts into 4Ω loads—and even more if bridge amplifiers are employed. With a 12 V_{DC} supply, the output signal swing is limited to less than 4 Vrms if clipping is avoided. Typical amplifiers have an input referred noise level of 2 µVrms, and with a gain of 40 dB (a typical value) the intrinsic output noise level is 200 µVrms, or 86 dB below clipping. For a normal listening level, the signal amplitude will be 20 dB below clipping which yields a S/N ratio of only 66 dB—which is just better than the noise reduced input to the amplifier.

Many manufacturers recommend using I/C power amplifiers with gains of 60 dB. This will always result in unacceptable noise performance at moderate listening levels since the amplifier generated noise is now over 2 mV. For a signal 20 dB below clipping the output S/N ratio is only 46 dB!

It is interesting to note that the inclusion of just 10 dB noise reduction is sufficient to put pressure on the performance standards of the remaining circuits in the audio path of an automotive radio. If more noise reduction is available, such as a combination of Dolby B and DNR, or Dolby C, then the subsequent gain distribution must be considered even more carefully. The power amplifier gain may have to be reduced to 20 dB to avoid degrading the noise performance. In fact it may be impractical to realize the full noise performance capability of systems providing high levels of noise reduction in many automotive stereo radios.

Modifications to the Standard Applications Circuit

1. TAPE DECKS WITH EQUALIZATION SWITCHES:

Many modern cassette tape decks and automotive radio cassette players offer at least two types of equalization in the head-preamplifier in order to optimize the frequency response of various tape formulations. These are often identified on the equalization switch as "Normal" and "CrO_2" corresponding to 120 µs and 70 µs time constants in the equalization network. This difference in time constants can mean that the noise floor from a cassette tape in the "CrO_2" mode can be up to 4 dB lower than for a tape requiring the "Normal" mode, *Figure 5.*

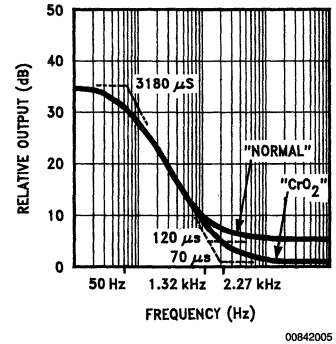


FIGURE 5. Tape Playback Equalization Including Integration

Although a compromise setting can be found for the DNR threshold setting to accommodate both types of tape, a single pole, double throw switch ganged to the equalization switch will optimize performance for each mode. In the example given in *Figure 6*, the resistor values shown are from an application that yielded a 400 mVrms input to the LM1894 when the tape flux density was 200 nW/m. For different tape-head amplifiers the resistors R_1 and R_2 are selected using a "Normal" tape as a source, and then R_3 is selected according to the relationship given in *Equation (5).*

Modifications to the Standard Applications Circuit (Continued)

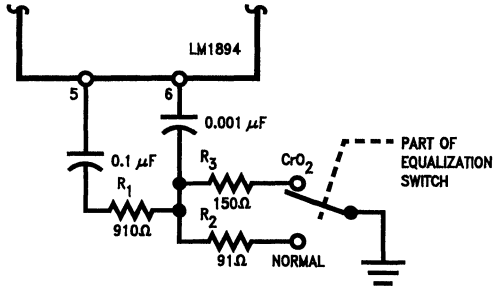


FIGURE 6. Optimizing the Control Path Threshold for Different Tape Formulations

Notice that only one additional resistor is required over the standard application, and it is easy to substitute transistor switching in place of the spdt switch.

$$R_1/(R_1 + R_2) = 0.63\ R_3/(R_1 + R_3) \quad (6)$$

2. TAPE DECKS WITH COMPLEMENTARY NOISE REDUCTION:

Most cassette decks available today employ some form of complementary (companding) noise reduction system, usually Dolby B Type. DNR can be used in conjunction with these noise reduction systems as a means to provide yet more noise reduction on decoded tapes and still provide noise reduction for unencoded tapes. The LM1894 is located after the companding system and provision must be made for the drop in noise level when the compandor is being used. The DNR threshold sensitivity is increased by the appropriate amount so that the lower noise levels are still able to activate the audio filters. For example, the circuit in *Figure 7* shows a switching arrangement to compensate for the 9 dB lower noise floor from a Dolby B decoded tape. Notice the change in resistor values R_1through R_3 to raise the sensitivity (yet keeping the sum of $R_1$and R_2 to 1k) and the 9 dB pad formed by the 3 kΩ resistor and the 1.5 kΩ resistor in parallel with the control path input Pin 6, for use when the compandor is switched off. Since the output level from the compandor is usually around 580 mV for a flux density of 200 nW/m, the ratio of R_1 to R_2 and R_3 is changed by only 5.6 dB compared to that shown in the previous Figure where the input level was 400 mVrms.

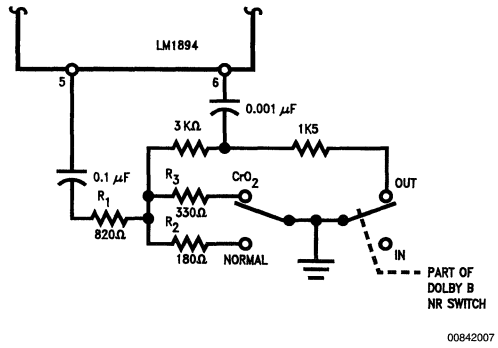


FIGURE 7. Switching with Other NR Systems

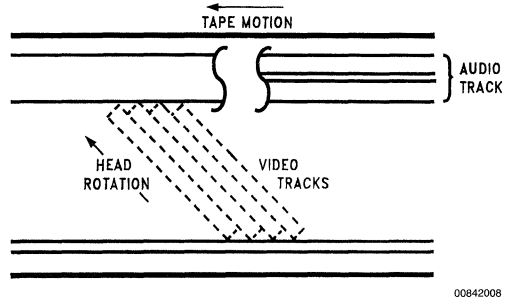


FIGURE 8. Video Magnetic Tape Format

3. VIDEO TAPE RECORDERS:

The audio track of a video cassette tape is similar to an audio cassette and appears along one edge of the tape. Although provision is made for two tracks, each 0.35 mm wide, a large number of recordings are monaural with a track width of 1 mm (0.04 inches).

Unlike the video heads, which are mounted on a rotating drum and angled to the direction of tape travel in order to give a much higher recording speed, the audio is recorded longitudinally with a separate head at 33.35 mm/sec for standard play, 16.88 mm/sec for long play, and 11.12 mm/sec for the very long play mode (VHS format tape machines). The noise spectrum is similar to an audio cassette but with a couple of differences. The typical frequency response from the head pre-amplifier does not extend beyond

Modifications to the Standard Applications Circuit (Continued)

10 kHz in the SP mode and is less in the LP and VLP modes. Even so, this bandwidth is enough to ensure the presence of the familiar tape "hiss" when played through modest or better Hi-Fi systems. Although the mono track width (twice as wide as an audio cassette stereo track) should help the S/N ratio, the slower tape speed does not, as shown in the curves of *Figure 9*. For the SP mode the S/N ratio is approximately 5 to 10 dB lower than the audio cassette and worsens by 3 to 5 dB in the extended play modes. Some "spurs" or "spikes" may be observed at harmonics of the video field frequency (60 Hz) and at the video line scan frequency of 15.734 kHz. The low frequency spikes will not affect DNR operation since the control path sensitivity decreases sharply below 1 kHz, but the presence of the 15.734 kHz component could cause improper sensitivity settings to be obtained. If this is the case, the pilot frequency notch filter for FM, described later, can be retuned by changing the capacitor from 0.015 µF to 0.022 µF.

Figure 9 also shows the noise spectrum with the new Beta Hi-Fi format. This is clearly superior to both the standard format and audio cassette tapes and is realized by using the two video record/play heads simultaneously for audio, thus taking advantage of the substantially higher relative tape speed. The audio is added in the form of four FM carriers, *Figure 10*. Four carriers are necessary for two audio channels since the azimuth loss between the normal video heads (reducing crosstalk between the heads at video frequencies) is not enough at the lower audio carrier frequencies. Each head therefore uses different carriers for the left and right channel signals.

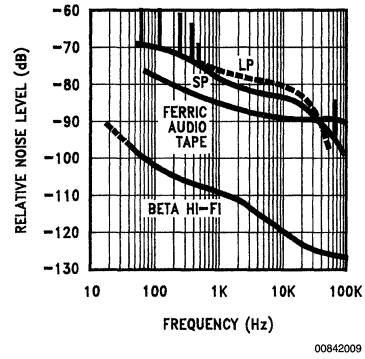


FIGURE 9. Video Tape Noise Spectrum Levels

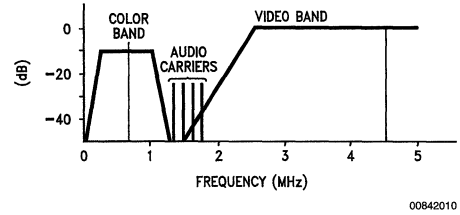


FIGURE 10. Beta Hi-Fi Carrier Frequencies

A quite different technique is used for VHS Hi-Fi, which is similar to that for 8 mm video. Separate audio heads are mounted on the same rotating drum that is carrying the video heads, but with a much larger azimuth angle compared to the video heads. The sound signal is written deep into the tape coating and then written over by the video signal which causes partial erasure of the audio—about a 10 dB to 15 dB loss. The difference in azimuth angle prevents crosstalk and the much greater writing speed still yields an S/N of over 80 dB.

Both Hi-Fi formats provide excellent sound quality with hardly any need for noise reduction but DNR can still play a role. Conventionally recorded tapes are and will be popular for quite a while, and even with Hi-Fi recording capability much recording will be done with television sound as a source—and the source noise will dominate now instead of the tape noise. As discussed later, DNR can be very effective in dealing with television S/N ratios, allowing much of the benefit of improved recording techniques to be enjoyed.

Modifications to the Standard Applications Circuit (Continued)

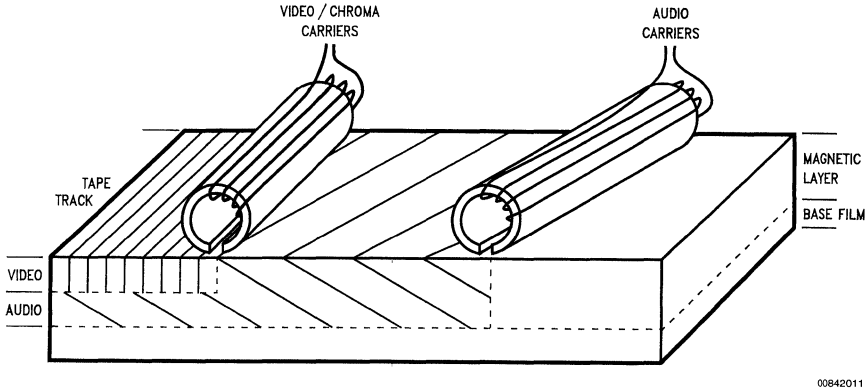


FIGURE 11. VHS Hi-Fi Recording Format

4. FM RADIOS:

FM sources can present special problems to DNR users. The presence of the 19 kHz stereo pilot tone can be detected in the DNR control path and cause improper threshold settings (the problem is not so much that the 19 kHz tone gives the wrong setting, but that if the threshold is adjusted with the tone present, then the threshold is wrong when the tone is absent—as in a monaural broadcast). Secondly, for FM broadcasts the noise level at the receiver detector output is dependent on the r.f field strength when this field strength is under 100 µV/meter at the antenna terminal. With a fixed DNR threshold, as the noise level increases with decreasing field strength, the minimum audio bandwidth becomes wider and a loss in noise reduction is perceived. This latter problem occurs primarily with automobile radios where the signal strength can vary dramatically as the radio moves about For the home receiver, re-adjustment of the DNR threshold setting for an individual station will compensate for the weaker signals.

To understand how much the pilot tone can affect the DNR control path, we can take a look at some typical signal levels. For an FM broadcast in the U.S., the maximum carrier deviation is limited to ±75 kHz with a pilot deviation that is 10% of this value. A high quality FM I/C such as the LM1865 will produce a 390 mVrms output at the detector with this peak deviation, so the pilot level at 19 kHz will be 39 mVrms. If the receiver does not include a multiplex filter, after de-emphasis 4 mV will appear at the inputs to the LM1894. Typically for FM signal noise floors, the resistive divider at Pin 5 will attenuate the pilot by 20 dB leaving 0.4 mVrms at Pin 6. This input level to the LM1894 control path is sufficient to cause the audio bandwidth to increase by over 1 kHz compared to the monaural minimum bandwidth. Of course, if the receiver does have a multiplex filter, which is common in high quality equipment or receivers that include Dolby B Type noise reduction, this problem will not happen, but otherwise we require an extra 15 dB to 20 dB attenuation at 19 kHz. This is obtained with a notch filter tuned to the pilot frequency connected between Pins 8 and 9 of the LM1894 Although a tuned inductor is shown, a fixed coil of similar inductance and Q can be used since with normal component value tolerances (±7% inductance, ±10% capacitance) the pilot tone will be attenuated by at least 15 dB.

Handling the signal strength dependence of the FM signal noise floor is not quite as easy – at least if pre-set DNR sensitivity settings are used. A look at the quieting curves for an FM radio will show why. At strong signal levels, greater than 1 mV/meter field strength at the antenna, the IF amplifier of the radio is in full limiting and the noise floor is between 60 dB and 80 dB below the audio signal. However, as the field strength starts to decrease below 1 mV/meter, the noise level begins to increase, even though the IF amplifier is still in limiting. Worse yet, since the demodulated output includes the noise from the stereo difference signal channel (L-R), the noise level is increasing more rapidly in the stereo mode than in the monaural mode. By the time the field strength has fallen to 100 µV/m the stereo noise is over 20 dB higher than the equivalent mono noise. If the DNR sensitivity is pre-set such that noise at the –45 dB to –55 dB level is activating the control path detector, when weaker stations are tuned in the noise level will increase and less noise reduction will be obtained. On the other hand, for stronger stations the noise level will drop below the detector threshold and a possibility exists that high frequency signals will be attenuated. Fortunately this latter occurrence is unlikely with commercial FM broadcasts since substantial signal compression is common, and the relatively high mid-band signals will be adequate enough to open the audio

Modifications to the Standard Applications Circuit (Continued)

bandwidth sufficiently. In any event, with very strong r.f. signals, the need for noise reduction is minimal and DNR can be switched out.

	FM	TV
L	4.7 mH	4.7 mH
C	0.015 µF	0.022 µF

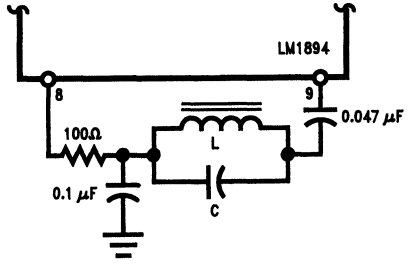


FIGURE 12. Control Path Notch Filter

Recognizing that a fixed threshold setting is necessarily a compromise for FM, the designer can still elect to use a pre-set adjustment for convenience. The set-up procedure is a little more complicated than for an audio tape source and involves the use of an FM signal generator. The carrier frequency from the generator (between 88 MHz and 108 MHz) is unmodulated except for the stereo pilot tone, and the receiver is tuned to this carrier frequency. Then the carrier level is increased until the stereo demodulator output S/N ratio is that desired for the DNR threshold setting. For example, if the recovered audio output is 390 mVrms for 75 kHz deviation of the carrier frequency, the stereo noise level is 2.2 mVrms for a 45 dB S/N ratio. The generator level is increased until this noise voltage is measured at the demodulator output and the resistive divider at Pin 5 of the LM1894 adjusted correspondingly. A multiplex filter should be inserted between the decoder output and the S/N meter to prevent the pilot tone from giving an erroneous reading. At no time should the pilot tone be switched off since this will allow the decoder to switch into the nomaural mode, decreasing the noise level −65 dB instead. A S/N ratio of 45 dB is chosen since many modern receivers incorporate blending stereo demodulators. As the dashed curve of *Figure 13* shows, when the stereo S/N ratio falls to 45 dB, the decoder starts to blend into monaural operation, thus keeping a constant S/N ratio. The loss in stereo separation that inevitably accompanies this blending is far less objectionable than abrupt switching from stereo to mono operation at weak signal levels.

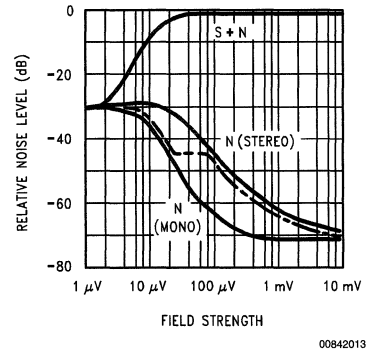


FIGURE 13. FM Radio Quieting Curves

5. TELEVISION RECEIVERS:

At first it might be thought that television broadcast signals, with an FM sound carrier located 4.5 MHz above the picture carrier frequency, will present the same difficulties as FM radio broadcasts to a DNR system with a pre-set threshold. This conclusion is modified by two considerations. First the TV receiver is unlikely to be mobile and the received signal strength will be relatively constant from an individual broadcast station. Secondly another subjective factor, the picture quality, will largely determine whether the signal strength is adequate enough for the viewer to stay tuned to that station. A representative television receiver will have a VHF Noise Figure between 6 dB and 7 dB such that, with a 75Ω antenna impedance, the picture will be judged noise-free at an input signal level of just above 0.5 mVrms – i.e. a picture signal to noise ratio of 43 dB. Noise will become perceptible to most viewers at a S/N ratio of 38 dB and become objectionable at 28 dB to 30 dB. Therefore 13 dB below 1 mVrms the picture noise is objectionable, and at −25 dB to −30 dB it will probably be totally unacceptable to the majority of viewers. For off-air broadcasts, the audio carrier amplitude is 7 dB to 10 dB below the picture carrier amplitude and for cable services the typical sound/picture carrier ratio is −15 dB. However, due to the FM improvement factor (45.4 dB for equal amplitude carriers compared to the AM picture carrier) audio S/N ratios do not degrade as rapidly as the picture S/N—even with the lower audio carrier amplitudes. *Figure 14* shows the increase in audio noise level as both carrier amplitudes are reduced from the picture carrier level that produces a noise-free picture. When the picture noise is already objectionable the audio noise level has remained virtually unchanged, even for an audio carrier 30 dB below the picture carrier. By the time an unacceptable picture noise level has been reached, the audio noise has increased by less than 3 dB for sound carriers at −10 dB and −20 dB relative to the picture carrier. Therefore it is unlikely

Modifications to the Standard Applications Circuit (Continued)

that a perceptible increase in noise compared to a strong channel will occur before the viewer switches to another channel.

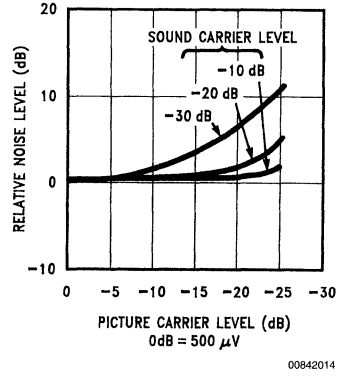


FIGURE 14. Increase in Audio Noise with Decreasing Carrier Levels

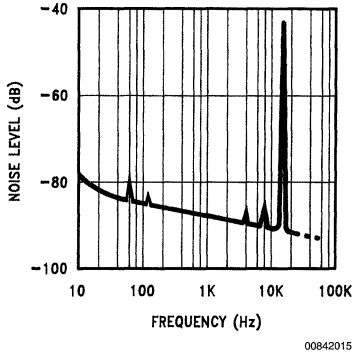


FIGURE 15. TV Noise Spectrum Level

Figure 15 shows the noise spectrum level of a strong audio carrier (1 mVrms) referred to 7.5 kHz carrier deviation. The standard peak deviation in the U.S. is 25 kHz so that the spectrum level will be 10 dB lower when referred to the peak audio level, meaning that the noise is not much better than the cassette tape noise levels shown previously. Only the relatively small power capability and limited bandwidth of audio amplifiers and speakers in conventional receivers has made this noise level acceptable. Unfortunately for the listener who hooks up the audio to his Hi-Fi system, or buys a new receiver with wider audio bandwidth and high output power (in anticipation of the proposed BTSC stereo audio broadcasts for television), TV sound will exhibit this noise.

Because the noise floor will be relatively constant, a pre-set threshold can be used for the LM1894 control path (although broadcast of older movies with unprocessed and noisy optical soundtracks might increase the received noise), and the only modification to the standard application circuit is to shift the control path notch filter down to 15.734 kHz. This is done with sufficient accuracy simply by changing the 0.015 μF tuning capacitor to 0.022 μF.

Note: The introduction of a stereo audio broadcast (the BTSC-MCS proposal) does not substantially modify the above conclusions, even though dbx noise processing is used The dbx-TV noise reduction is applied only to the new stereo difference signal channel (L-R) to decrease the *additional* noise intrinsic in the use of an AM subcarrier along with the normal (L+R) monaural channel This means that the new stereo signal should have roughly the same characteristics as the present monaural signal

6. MULTIPLE SOURCES:

Multiple sources are best accommodated by keeping the potentiometer in the LM1894 control path and allowing the user to optimize each source. Nevertheless, for convenience, pre-sets are often desired and these can be done in two ways.

1. If the sources have widely different S/N ratios, the resistive divider at Pin 5 should be tapped at the appropriate point for each source noise level. This assumes that the source signal levels have been matched at the input to the LM1894 for equal volume levels.
2. If the source S/N ratios are not too far different, then the input levels can be trimmed individually to produce the same noise level in the LM1894 control path. A single sensitivity setting is used, and an additional switch pole ganged to the source selector switch is avoided

Examples of both arrangements are shown in *Figure 16*(a) and *(b)*. To set up the multiple source system of *16(b)* , the DNR control path sensitivity is adjusted for the source with the *lowest* noise floor. Measure the peak detector voltage (Pin 10) produced by this noise source and then switch to the next source. Adjust (attenuate) the input level of the new source to match the previous Pin 10 detector voltage and repeat this procedure for each subsequent source.

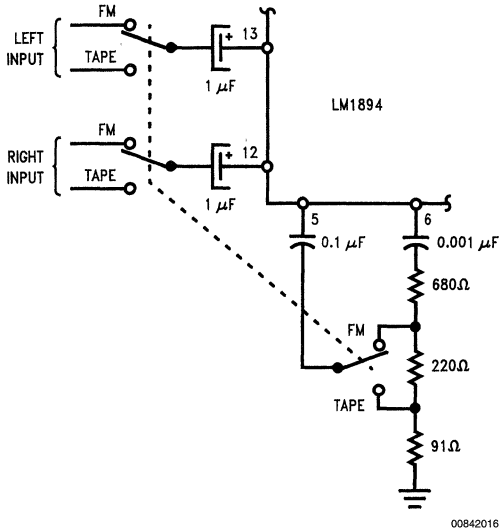
7. CASCADING THE LM1894 AUDIO FILTERS

The LM1894 has two matched audio lowpass filters which can be cascaded, providing a single channel filter per I/C with a 12 dB/octave roll-off. This produces slightly more noise reduction (up to 18 dB) but because the steeper filter slope may in some cases produce audible effects on high frequency material, cascaded filters are best used for sources with a relatively restricted h.f. content. When the filters are cascaded the combined corner frequency decreases by 64% according to *Equation (7)*), for n = 2

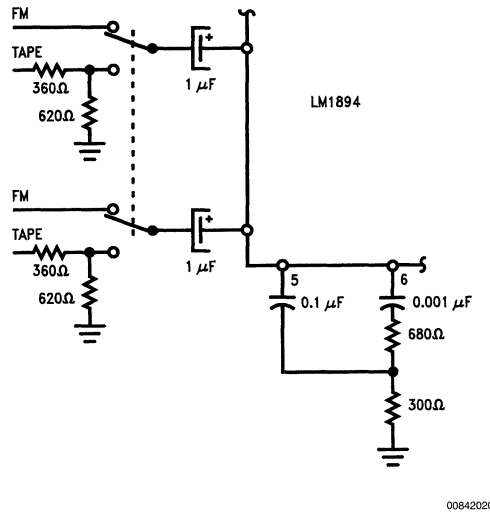
$$f_C = f_0 \sqrt{10^{0.3/n} - 1} \qquad (7)$$

Therefore, to retain the original frequency range, the capacitor values must be reduced by the same factor to 0.0022 μF. One of the audio outputs is connected over to the other audio filter input and the summing amplifier in the control path is by-passed by moving the 0.1 μF coupling capacitor from Pin 5 over to the single audio input. If the audio source is unable to drive the 1 kΩ impedance of the control path input network, this can be scaled up by using a 0.01 μF capacitor and a 10 kΩ potentiometer.

Modifications to the Standard Applications Circuit (Continued)



(a) Input and Control Path Switching for Two Sources



(b) Eliminating the Control Path Switch

FIGURE 16. Multiple Programme Source Switching

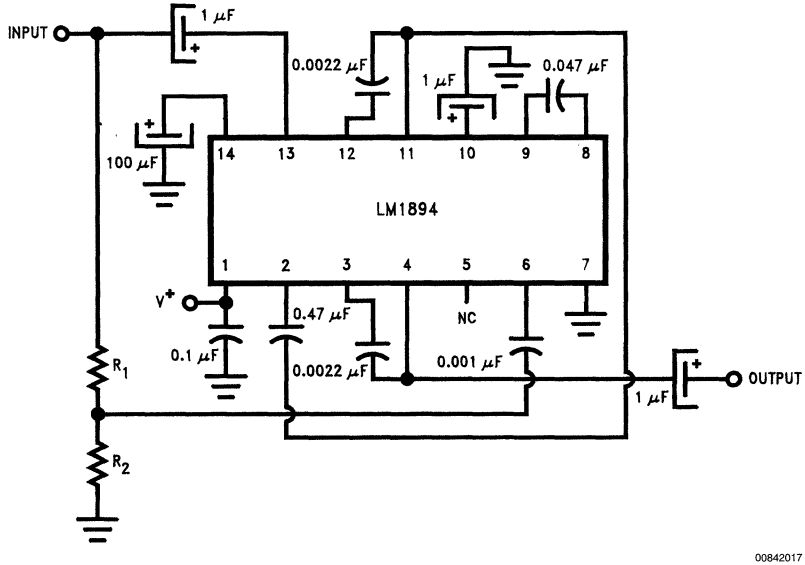


FIGURE 17. Cascading the Audio Filters of the LM1894

Audio Amplifiers Utilizing: SPiKe™ Protection

National Semiconductor
Application Note 898
John DeCelles

Introduction

As technology develops, integrated circuits continue to provide an advantage to consumers requiring products with more functionality and reliability for their money. It's been less than fifty years since the first transistor began to provide audio amplification to consumers. Technology changed, bringing to the market higher power discretes and hybrids with the later development of lower powered monolithics. Today with the development of IC technologies, high-performance monolithic audio amplifiers arrive, allowing consumers to experience high-power, high-fidelity audio systems in compact packages.

The Overture™ Audio Power Amplifier Series possesses a unique protection system that saves audio amplifier designers components, size, and cost of their systems. This translates into higher-power, more functional, more reliable, compact audio amplification systems.

These advantages, generally provided only in high-end discrete amplifiers, are accomplished by providing a protection mechanism within a monolithic power package. Since audio amplifier designers generally need to provide some sort of protection to the output transistors in order to keep product failures to a minimum, National Semiconductor's Audio Group has designed SPiKe (Self Peak Instantaneous Temperature (°Ke)) Protection. This is a protection mechanism designed to safeguard the amplifier's output from overvoltages, undervoltages, shorts to ground or to the supplies, thermal runaway, and instantaneous temperature peaks.

The following pages will explain in detail each of the protections provided by SPiKe protected audio amplifiers, the advantages they bring to audio designers, and why they are necessary.

Each of the protection sections on the following pages will refer to *Figure 1.* (Amplifier Equivalent Schematic with Simplified SPiKe Protection Circuitry) when its functionality is described.

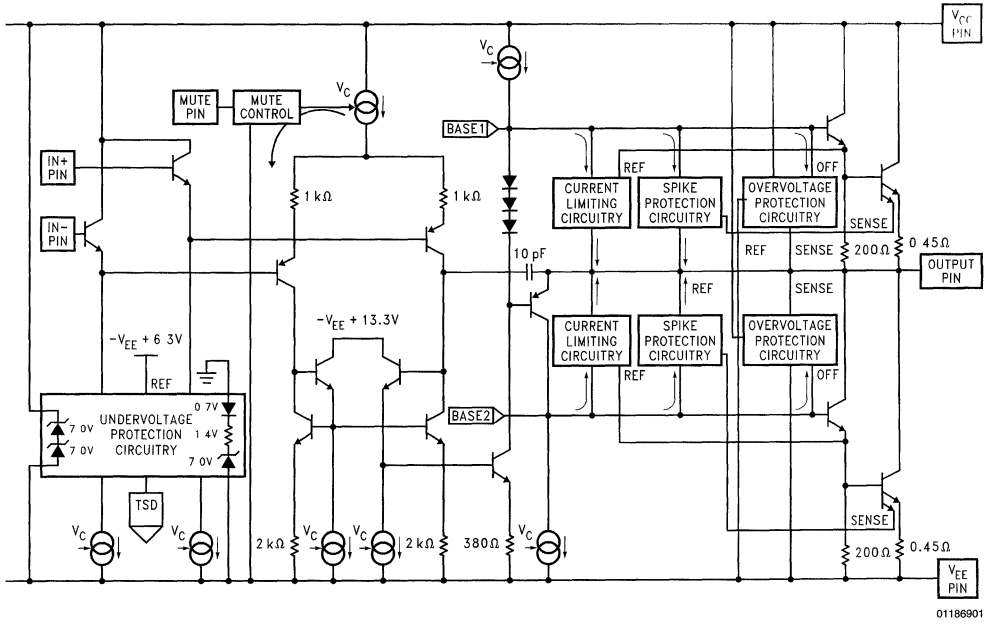


FIGURE 1. Amplifier Equivalent Schematic with Simplified SPiKe Protection Circuitry

Self Peak Instantaneous Temperature Limiting (SPiKe)

SPiKe Protection is a "uniquely-smart" protection mechanism that will adjust its output drive capability according to its output operating conditions, thus safeguarding itself against the most stringent power limiting conditions.

Other power amplifiers on the market provide SOA protection by calculating external resistances for adjustable current limiting whose primary function is to keep the amplifier within its safe operating area. Not only do these amplifiers require external components, but they aiso have a design conflict between fault protection and maximum output current drive capability. In order to keep the device from self-destructing against output shorts to either supply rail, the adjustable current limit must be significantly lowered, thus limiting the device's current drive capability.

SPiKe protected audio amplifiers provide extensive fault protection without sacrificing output current drive capability. Its circuitry functions by sensing the output transistor's temperature, enabling itself when the temperature reaches approximately 250°C. Depending upon the amplifier's present operating conditions, the device will reduce the output drive transistor's base current, as shown in *Figure 1*, keeping the transistor within its safe operating area.

The uniqueness of SPiKe protected audio amplifiers is its abillty to monitor the output drive transistor's safe operating area dynamically, regardless of an output to ground short, an output to supply short, or the reaching of its power limit by any pulse within the audio spectrum.

As can be seen from *Figure 2*, *Figure 3* and *Figure 4*, the safe operating area is reduced for all pulse widths as the case temperature increases. This indicates that good heatsinking is required for optimal operation of the power amplifier. *Figure 5*, *Figure 6* and *Figure 7* illustrate the reduction of the safe operating area by the increasing effect of enabling SPiKe Protection on a 100 Hz sine wave due to increasing case temperatures.

As seen in the Current Limiting section, a short to ground with an input pulse applied to the amplifier will be current limited by the conventional current limiting circuitry for a few hundred microseconds. When the junction temperature reaches its limit, SPiKe protection takes over, limiting the output current further, as the junction temperature tries to rise above 250°C.

This protection scheme results in the power capabilities being dependent upon the case temperature, the transistor operating voltages, V_{CE}, and the power dissipation versus time.

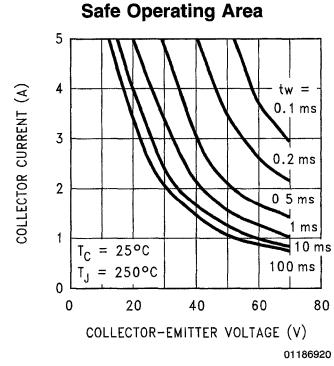


FIGURE 2. T_C = 25°C

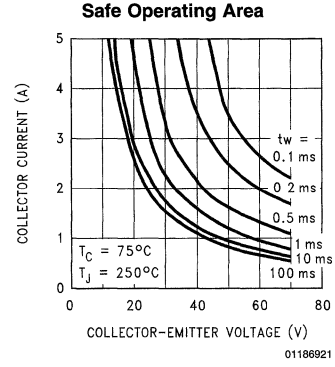


FIGURE 3. T_C = 75°C

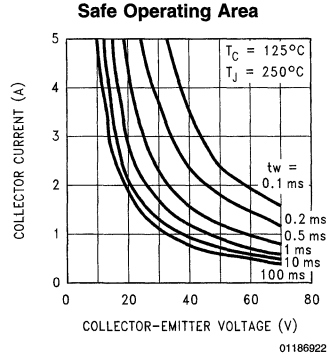


FIGURE 4. T_C = 125°C

Self Peak Instantaneous Temperature Limiting (SPiKe)

(Continued)

SPiKe Protection Response

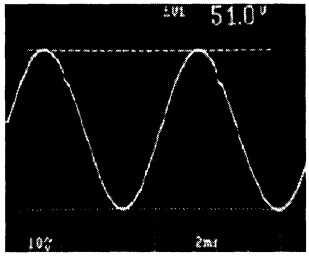


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FIGURE 5. T_C = 75˚C

SPiKe Protection Response

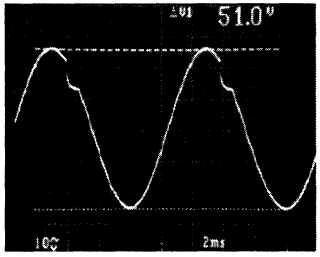

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FIGURE 6. T_C = 80˚C

SPiKe Protection Response

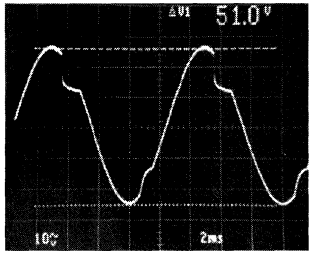

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FIGURE 7. T_C = 85˚C

Figure 8 and *Figure 9* are provided for each SPiKe Protected audio power amplifier and should be used to determine the power transistor's peak dissipation capabilities and the power required to activate the power limit. This information may help a designer to determine the maximum amount of power that SPiKe protected amplifiers may deliver into different loads before enabling SPiKe protection.

Figure 8 shows the peak power dissipation capabilities of the output drive transistor at increasing case temperatures for various output pulse widths.

Figure 9 shows the power required to activate SPiKe circuitry at increasing case temperatures over the operating voltage range.

Again, it is evident that good heatsinking and ventilation within the system are important to the design in order to achieve maximum output power from the amplifier.

SPiKe protected amplifiers provide the capability of regulating temperature peaks that may be caused by reaching the power limit of the safe operating area. The reaching of power limits may result from increased case temperatures while heavily driving a load or by conventional current limiting, resulting from the output being shorted to ground or to the supplies.

Pulse Power Limit

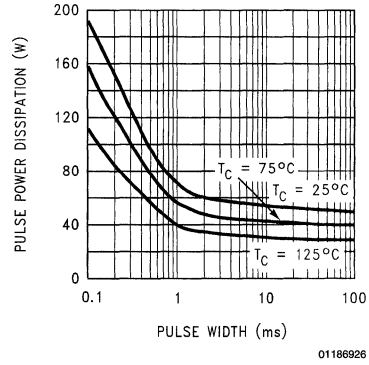

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FIGURE 8. Pulse Power Dissipation vs Pulse Width

Pulse Power Limit

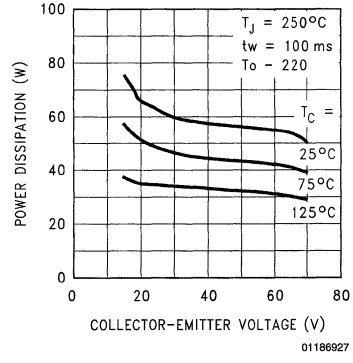

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FIGURE 9. Pulse Power Dissipation vs V_{CE}

Overvoltage—Output Voltage Clamping

One of the most important protection schemes of an audio amplifier is the protection of the output drive transistors against large voltage flyback spikes. These spikes are created by the sudden attempt to change the current flow in an inductive load, such as a speaker. When a push-pull amplifier goes into power limit (i.e., reaching the SOA limit) while driving an inductive load, the current present in the inductor drives the output beyond the supplies. This large voltage spike may exceed the breakdown voltage rating of a typical audio amplifier and destroy the output drive transistor. In general, the amplifier should not be stressed beyond its *Absolute Maximum* (No Signal) Voltage Supply Rating and should be protected against any condition that may lead to this type of voltage stress level. This type of protection generally requires the use of costly zener or fast recovery Schottky diodes from the output of the device to each supply rail.

However, SPiKe protected audio amplifiers possess a unique overvoltage protection scheme that allows the device to sustain overvoltages for nominally rated speaker loads. Referring to *Figure 1*, the protection mechanism functions by first sensing that the output has exceeded the supply rail, then immediately turns the driving output transistor off so that its breakdown voltage is not exceeded. The circuitry continues to monitor the output, waiting to turn the output drive transistor back on when the overvoltage fault has ceased.

While monitoring the output, the IC also provides SPiKe protection if needed. Finally, SPiKe protected audio amplifiers possess an internal supply-clamping mechanism; a zener plus a diode drop from the output to the positive supply rail and an intrinsic diode drop from the output to the negative rail. This equates to clamping of approximately 8V on the positive rail and 0.8V on the negative rail as can be seen in *Figure 10* and *Figure 11*, respectively.

Figure 12 and *Figure 13* model the output stage for each overvoltage condition exemplifying how the voltage waveforms are clamped to their respective values for high frequency waveforms. As shown in the Self Peak Instantaneous Temperature Limiting (SPiKe) section, *Figure 2*, *Figure 3* and *Figure 4*, the safe operating area for lower frequency waveforms is much smaller than for higher frequency waveforms. Therefore, the power limits of low frequency waveforms may be reached much more easily than for high frequency waveforms. It is due to this fact that more extreme and more frequent overvoltages may occur at lower frequencies, as shown in *Figure 14*, *Figure 15*, *Figure 16* and *Figure 17*. The peak output voltage spikes may increase beyond the described clamping values due to extreme power conditions, however, the waveforms will decrease to the clamping values with the discharge of the output inductor current, as shown in *Figure 14*.

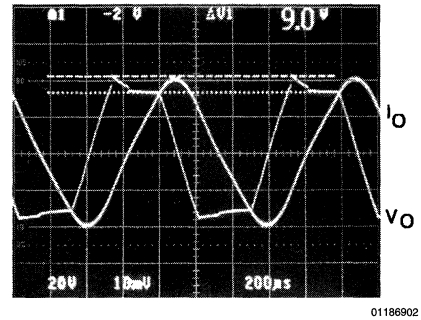

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FIGURE 10. Positive Output Voltage Clamping Waveform

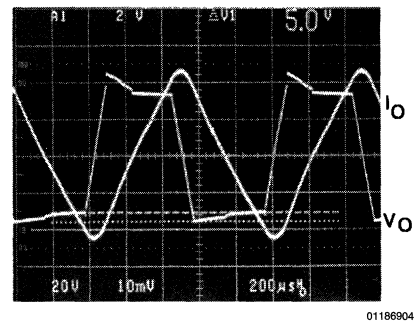

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FIGURE 11. Negative Output Voltage Clamping Waveform

Overvoltage—Output Voltage Clamping (Continued)

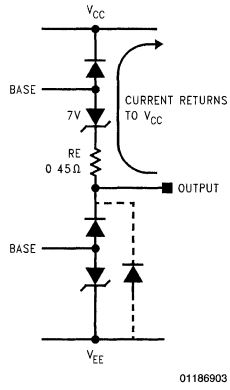

FIGURE 12. Output Stage Overvoltage Model (V_{CC})

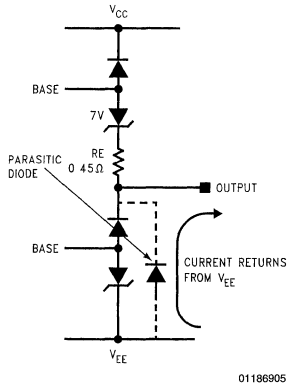

FIGURE 13. Output Stage Overvoltage Model ($-V_{EE}$)

The lower output stage has the advantage of an intrinsic diode from the negative rail to the output which can replace the usual external clamping diode in an audio amplifier. This intrinsic diode is an advantage of the monolithic IC, capable of handling the large current flowing through the load at the time of the power limit.

The system is not protected against all reactive loads since these clamping diodes will dissipate large amounts of power that cannot be controlled by the peak temperature limiting circuitry if the fault is sustained for a long period of time. It should also be noted that for purely reactive loads, all of the power is dissipated in the amplifier and none in the load. This implies that if the load is more reactive than resistive, at those frequencies, more power will be dissipated in the amplifier than delivered to the speaker. Since the impedance characteristics of a speaker change over frequency, it is very important to know what types of loads the amplifier can and cannot drive in order to not only match the amplifier and speaker for optimum performance, but also to protect the amplifier from trying to outperform itself. It is the mismatching of components or low dips in the resistive component of a complex speaker that can cause an amplifier to go into power limit. The likelihood of reaching the amplifier's power limit is greatly reduced when the minimum impedance that the amplifier can drive is known.

Figure 14, *Figure 15*, *Figure 16* and *Figure 17* are examples of the LM3876 reaching its power limit, experiencing large flyback voltages from an inductive load, for various input signals and loads.

The test conditions for *Figure 14*, *Figure 15*, *Figure 16* and *Figure 17* are as follows:

- Using an LM3876
- No external compensation components
- V_{CC} = ±35V
- Av_{CL} = 20
- I_O/Div. = 2.0A/div
- Z_L = 7.5 mH + 4Ω for *Figure 14*
- Z_L = 7.5 mH + 2Ω for *Figure 15*, *Figure 16* and *Figure 17*
- f = 100 Hz for *Figure 14*, *Figure 15* and *Figure 17*
- f = 70 Hz for *Figure 16*

In *Figure 14*, the 4.5Vpk input signal applied to the amplifier with a closed-loop gain of 20, produces the severely clipped 34V output voltage waveform, as shown. The sharp 48.5V overvoltage spike that occurs at the crossover point is due to the amplifier output stage reaching the SOA (Safe Operating Area) limit. For this waveform, the collector-emitter voltage is quite large, while the output current is also quite large (4A) Referring to *Figure 2*, *Figure 3* and *Figure 4*, it is easily understood that the SOA power limit has been reached.

When the SOA limit is reached, the SPiKe protection circuitry tries to limit the output current while the inductor tries to continuously supply the current it has stored. Since the current in an inductor can't change instantaneously, the current is driven back into the output up through the upper drive transistor, as shown in *Figure 12*.

It is this current that causes the large flyback voltage spike on the output waveform. The peak of the voltage spike can be found by taking the current going through the output at the time of the power limit multiplied by the 0.45Ω emitter resistor and adding it to the zener-diode combination. In *Figure 10* this would be (2A)(0.45Ω) + 8V which is approximately 9V, as shown by the cursors. For the lower output stage, the clamping voltage is controlled by an intrinsic diode that replaces costly output clamping diodes.

In *Figure 14*, when the current reaches close to zero, the voltage at the output tends to move towards the output voltage that it would have been if the power limit had not been reached. This is typical for all overvoltage occurrences. It should be noted that when the overvoltage fault occurs, the device is no longer functioning in the closed-loop mode.

In *Figure 15*, one waveform is actually a sinewave with SPiKe protection enabled, as in *Figure 5*, *Figure 6* and *Figure 7* with the same overvoltage spikes as in *Figure 14* and the other waveform is the output current. In the middle of the response, the current is rising toward 6A when SPiKe is enabled, causing a "bite" to be taken out of the sinewave. The device is just trying to limit the output current at this point, as explained in the SPiKe Protection section. The overvoltage flyback spike then occurs while the output current discharges to zero. However, this time when the current

Overvoltage—Output Voltage Clamping (Continued)

reaches zero, the current and voltage must make up for what it had lost and try to return to its position on the amplified input waveform. The voltage jumps up to its value, but the current must slowly and continuously charge up to its place on the current waveform, then continue downward as the lower output stage starts sinking current. It must be remembered that the current waveform would have been a sinewave if the SOA power limit hadn't been reached.

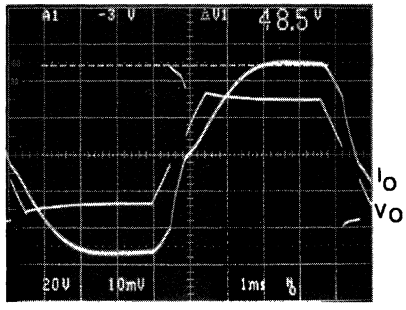

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FIGURE 14. Overvoltage Exceeding Clamping Level

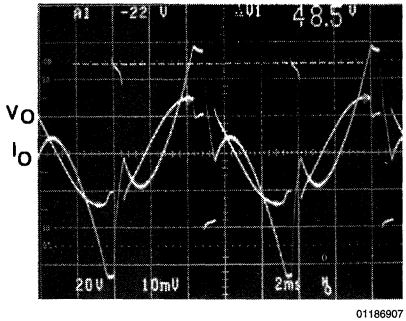

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FIGURE 15. Reaching the SOA Power Limit, f = 100 Hz, SPiKe Enabled

Multiple SOA power limits on the output waveform are the difference between *Figure 15* and *Figure 16*. *Figure 16* is intended to show that multiple SOA power limits can occur under extreme loading conditions. The amplifier is trying to drive a 70 Hz sinewave into a 7.5 mH inductor in series with a 2Ω resistor. As the signal frequency decreases, with a low resistance load, the number of SOA power limits will increase. The frequency of reaching power limits will depend upon the size of the reactance as the load.

Figure 17 is intended to exemplify the large current overdrive that can occur when the output waveform is driven hard into the rails. Notice that the current is over 6Apk for each voltage swing.

It must be remembered that it is the large voltage across the output drive transistors that would normally exceed a discrete output transistor's breakdown voltage. A discrete power transistor that is not protected with output clamping diodes would be destroyed if its breakdown voltage was exceeded. SPiKe protected audio amplifiers clearly show the ability to withstand overvoltages created by low impedance loads.

The integration of output overvoltage protection within monolithic audio amplifiers provides the advantage of eliminating expensive fast-recovery Schottky diodes that would be used in a discrete design, thus resulting in fewer external components and a lower system cost.

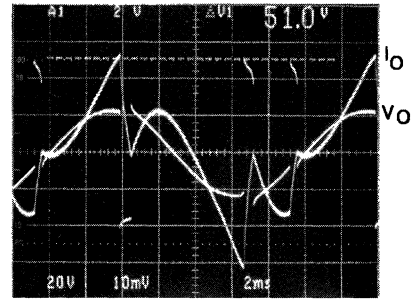

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FIGURE 16. Multiple SOA Power Limits

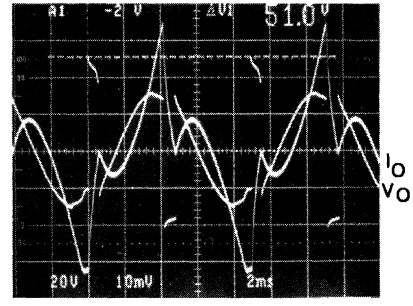

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FIGURE 17. Output Saturation Causing Extreme Overvoltage

Undervoltage—Popless Power-On/Off

SPiKe protected audio amplifiers possess a unique undervoltage protection circuit that eliminates the annoying and destructive pops that occur at the output of many amplifiers during power-up/down. SPiKe's undervoltage protection was designed because all DC voltage shifts or "pops" at the output should be avoided in any audio amplifier design, due to their destructive capability on a speaker. These pops are generally a result of the unstable nature of the output as internal biasing is established while the power supplies are coming up.

SPiKe Protection accomplishes this by disabling the output, placing it in a high impedance state, while its biasing is established. This function is achieved through the disabling

Undervoltage—Popless Power-On/Off (Continued)

of all current sources within the device as denoted by control signal V_C, in *Figure 1*. For the LM2876, LM3876, and LM3886, the control signal will not allow the current sources to function until 1) the total supply voltage, from the positive rail to the negative rail, is greater than 14V and 2) the negative voltage rail exceeds –9V. The LM3875 is undervoltage protected with the relative 14V total supply voltage condition only. Thus for the "6"-series, the amplifiers will not amplify audio signals until both of these conditions are met. It is this –9V protection that causes the undervoltage protection scheme to disable the output up to 18V between the positive and negative rail, assuming that both supply rails come up simultaneously. This can be seen in *Figure 18*. The –9V undervoltage protection is ground referenced to eliminate the possibility of large voltage spikes, that occur on the supplies, which may enable the relative 14V undervoltage protection momentarily.

It should be noted that the isolation from the input to the output, when the output is in its high-impedance state, is dependent upon the interaction of external components and traces on the circuit board.

As can be seen in *Figure 18* and *Figure 19*, the transition from ground to $\pm V_{CC}$ and from $\pm V_{CC}$ to ground upon power-on/off is smooth and free of "pops". It can also be seen from the magnification of *Figure 18* in *Figure 20*, that the amplifier doesn't start amplifying the input signal until the supplies reach ±9V. It is also evident that there is no feedthrough from 0V to ±9V. It must be noted that the sinewave being amplified is clipped initially as the supplies are coming up, but after the supplies are at their full values, the output sinewave is actually below the clipping level of the amplifier.

It should also be noted that the waveforms were obtained with the mute pin of the LM3876 sourcing 0.5 mA, its 0 dB attenuation level. If the mute pin is sourcing less than 0.5 mA, the nonlinear attenuation curve may induce crossover distortion or signal clipping. The Mute Attenuation curves vs. Mute Current in the datasheets of the LM2876, LM3876, and LM3886 show this nonlinear characteristic. The LM3875 is the sister part to the LM3876 and does not have a mute function.

For optimum performance, the mute function should be either enabled or disabled upon power-up/down. Although the undervoltage protection circuitry is not dependent upon the mute pin and its external components, the mute function can be used in conjunction with the undervoltage function to provide a longer turn-on delay. It should be noted that the mute function is also popless. Of the multiple ways to set the mute current and utilize the mute function, the use of a regulator can continuously control the amount of current out of the mute pin. This regulation concept keeps the attenuation level from dropping below 0 dB when the supply is sagging. More information about mute circuit configurations will be provided later in a future application note.

The advantages of undervoltage protection in SPiKe protected audio amplifers are that no pops occur at the output upon power-up/down. Customers can also be assured that their speakers are protected against DC voltage spikes when the amplifier is turned on or off.

Current Limiting—Output Short to Ground

Whether in the lab or inside a consumer's home, the possibility of an amplifier output short to ground exists. If current limiting is not provided within the amplifier, the output drive transistors may be damaged. This means one of two things, either sending the unit to customer service for repair or if you're in the lab, throwing the discrete drive transistor or hybrid unit away and replacing it with a new one. SPiKe protected audio amplifiers eliminate this costly, time-consuming hassle by providing current limiting capability internally.

This also means that the multiple components required to provide current limiting capability in a discrete design are eliminated with the monolithic audio amplifier solution, once again, reducing the system size and cost.

The value of the current limit will vary for each particular audio amplifier and its output drive capability. Please refer to each amplifier's datasheet Electrical Characteristics section for particular current limits.

As can be seen in *Figure 21*, the value of current limiting for the LM3876 is typically 6 Apk when V_{CC} = ±35V and R_L = 1Ω. From the scope cursors at the top of the waveform I_{LIMIT} = Vo/R_L. This test was performed with a closed-loop gain of 20 and an input signal of 2V (t_w = 10 ms).

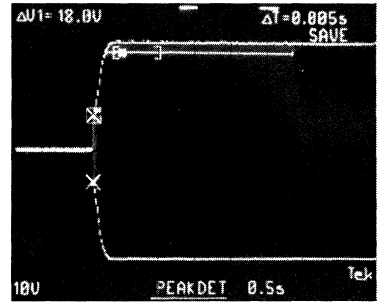

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FIGURE 18. Output Waveform Resulting from Power-On Undervoltage Protection

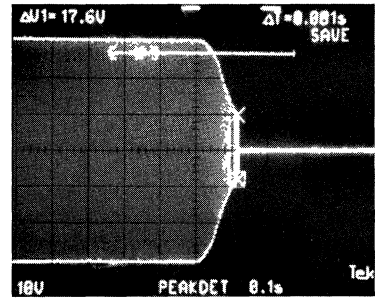

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FIGURE 19. Output Waveform Resulting from Power-Off Undervoltage Protection

Current Limiting—Output Short to Ground (Continued)

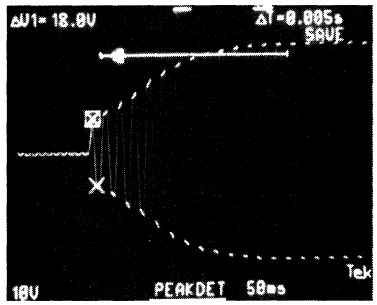

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FIGURE 20. Output Waveform Resulting from Power-Off Undervoltage Protection

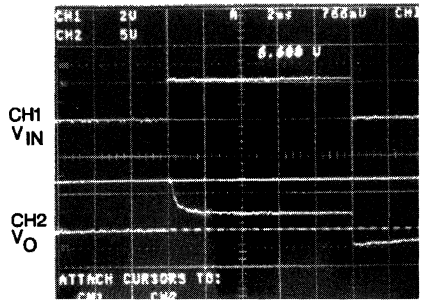

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FIGURE 21. LM3876 Typical Current Limiting with SPiKe Protection ON

Notice that the initial current limit is at its peak value of approximately 6A, but as time increases, the final current limit decreases. This is due to the enabling of the instantaneous temperature limiting circuitry or SPiKe protection. When the IC is in current limiting, the temperature of the output drive transistor array increases to its limit of 250°C, at which time SPiKe protection is enabled, reducing the amount of output drive current. It is this further reduction of its drive current that prevents the output drive transistor from exceeding the safe operating area.

As shown in *Figure 22*, *Figure 23* and *Figure 24* as the input pulses' time increases, the level of SPiKe protection imposed on the waveform increases. It should be noted that SPiKe protection was enabled after 200 µs of current limiting in *Figure 23* and *Figure 24*, but is in general dependent upon the case temperature, the transistor operating current and voltage, and its power dissipation versus time.

The internal current limiting circuitry functions by monitoring the output drive transistor current. The sensing of an increase in this current signals the circuitry to pull away drive current from the base of the output drive transistor as shown in *Figure 1*. The harder the input tries to drive the output, the more current is pulled away from the output drive transistor, thus internally limiting the output current.

Another point worth mentioning is that with increasing supply voltages, the turn-on point of SPiKe protection, when in current limiting, will decrease. Since the internal power dissipation is greater, it will take a shorter amount of time before the temperature of the output drive transistor increases to the SOA limit.

Once again, SPiKe protected audio amplifiers save design time and external component count by integrating system solutions within the IC, translating into more cost reduction.

Current Limiting—Output Short to Supply

One feature of SPiKe Protection which can prevent costly mistakes from occurring in the lab when prototyping Overture audio amplifiers is its protection from output shorts to the supply rails. The device is protected from momentary shorts from the output to either supply rail by limiting the current flow through the output transistors.

Although accidents such as this one occur infrequently, accidents do happen and if one were to happen with Overture audio amplifiers they would be protected for a limited amount of time. Normally when an accident like this would occur in a discrete design with no current limiting protection, the output transistor would be subjected to the full output swing plus a large current draw from the supply. This type of stress would destroy an output stage discrete transistor whereas with SPiKe protected amplifiers, the current is internally limited, thus preventing its output transistors from being destroyed.

One note to make about this protection scheme is that the current limitation is not sustained indefinitely. In essence, the output shorts to either supply rail should not be sustained for any period of time greater than a few seconds. Frequent temporary shorts from the output to either supply rail will be protected, however, continued testing of the circuitry in this manner is not guaranteed and is likely to cause degradation to the functionality and long-term reliability of the device.

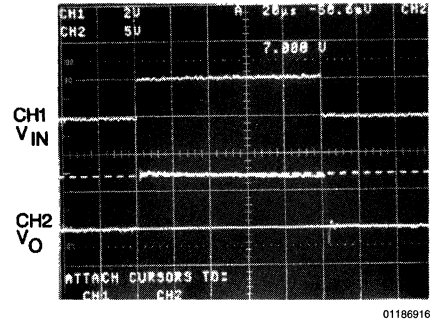

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FIGURE 22. t_w = 100 µs, t_{SPIKe} (Not Enabled)

Current Limiting—Output Short to Supply (Continued)

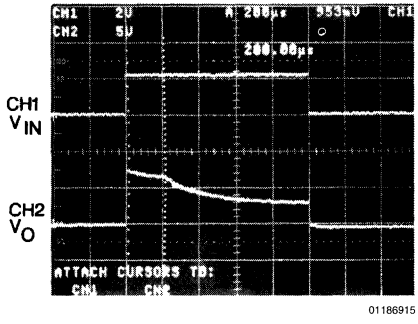

FIGURE 23. t_w = 1 ms, t_{SPIKe} = 200 µs

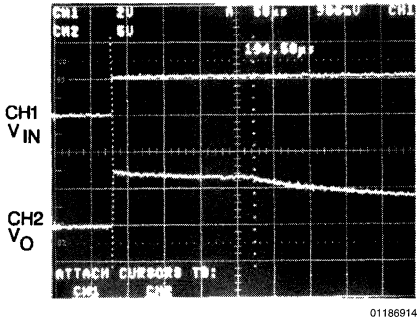

FIGURE 24. t_w = 10 ms, t_{SPIKe} = 195 µs

Thermal Shutdown—Continuous Temperature Rise

An audio system designer's design cycle time is reduced by eliminating the need for designing tricky thermal matching between discrete output transistors and their biasing counterparts which are physically located some distance from each other. Complex thermal sensing and control circuitry provided from the legendary Bob Widlar, and the ability of integrating it onto a monolithic amplifier, eliminates the external circuitry and long design time required in a discrete amplifier design.

SPiKe protected audio amplifiers are safeguarded from Thermal runaway, an area of concern for any complementary-symmetry amplifier. Thermal runaway is an excessive amount of heating and power dissipation of the output transistor from an increased collector current caused by the two complementary transistors not having the same characteristics or from an uncompensated V_{BE} being reduced by high temperatures.

If proper heatsinking is not utilized, the die will heat up due to the poor dissipation of power when the amplifier is being driven hard for a long period of time. Once the die reaches its upper temperature limit of approximately 165˚C, the thermal shutdown protection circuitry is enabled, driving the output to ground. A pseudo "pop" at the output may occur when this point is reached, due to the sudden interruption of the flow of music to the speaker. The device will remain off until the temperature of the die decreases about 10˚C to its lower temperature limit of 155˚C. It is at this point that the device will turn itself on, again amplifying the input signal.

As can be seen in *Figure 25* and *Figure 26*, the junction temperature vs time graph and the response to the activation of the thermal shutdown circuitry perform in a Schmitt trigger fashion, turning the output on and off, thus regulating the temperature of the die over time when subjected to high continuous powers with improper heatsinking.

The intention of the protection circuitry is to prevent the device from being subjected to short-term fault conditions that result in high power dissipation within the amplifier and thus transgressing into thermal runaway. If the conditions that cause the thermal shutdown are not removed, the amplifier will perform in this Schmitt trigger fashion indefinitely, reducing the long-term reliability of the device.

The fairly slow-acting thermal shutdown circuitry is not intended to protect the amplifier against transient safe operating area violations. SPiKe protection circuitry will perform this function.

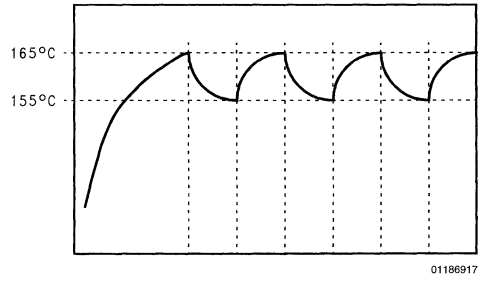

FIGURE 25. Junction Temperature vs Time

Thermal Shutdown—Continuous Temperature Rise (Continued)

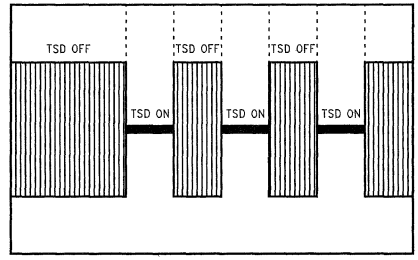

FIGURE 26. Thermal Shutdown Waveform

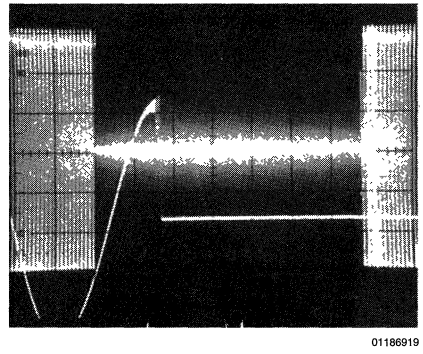

FIGURE 27. Actual Thermal Shutdown Waveform

Overture™ Series High-Power Solutions

National Semiconductor
Application Note 1192
John DeCelles and Troy Huebner

Table of Contents

1.0 Introduction

National Semiconductor has a broad portfolio of monolithic power integrated circuits covering power levels from a few hundred milliwatts up to 60W of non-clipped continuous average power. These ICs cover most audio applications by themselves, however, for really high-power applications, other methods need to be employed because IC packages have limited power dissipation capabilities.

There are many different ways of obtaining over 100W of output power. Most high-end power amplifier manufacturers utilize discrete circuits which allows them to market their amplifiers as "specially designed,..." However, there is a price to be paid for discrete amplifier designs; they are complex, difficult to design, require many components, lack the comprehensive protection mechanisms of integrated circuits and are not as reliable.

Other methods of obtaining output power greater than 100W include the use of power ICs as drivers for discrete power transistors. There are a number of these types of circuits, but they too possess all of the same flaws as discrete circuits, including a lack of comprehensive output stage protection.

2.0 Objective

The objective is to provide simple high-power solutions that are conservatively designed, highly reliable and have low part count. This document provides three specific, but not unique, application circuits that provide output power of 100W, 200W, and above. These circuits are the parallel, bridged, and bridged/paralleled configurations.

These three circuits are simple to understand, simple to build and require very few external components compared to discrete power amplifier designs. Simplicity of design and few components make this solution much more reliable than discrete amplifiers. In addition, these circuits inherently possess the full protection of each individual IC that is very difficult and time consuming to design discretely. Finally, these circuits are well known and have been in industry for years.

3.0 Conclusion

The BR100 (100W Bridged Circuit), PA100 (100W parallel circuit), and the BPA200 (200W Bridged/Paralleled Circuit) are high-power solutions that can be used in many applications, but they are primarily targeted for Home Theater Amplifier applications such as powered subwoofers, self-powered speakers, and surround sound amplifiers.

While bridged amplifier configurations are able to provide high power levels, they also consume four times more power than a conventional single-ended solution. However, it is feasible to conservatively design a 100W bridged amplifier

3.0 Conclusion (Continued)

solution, as will be shown here. The bridged solution is designed to drive an 8Ω nominal load for self-powered speaker or powered subwoofer applications.

The parallel amplifier is another configuration that can be used to obtain higher output power levels by combining two IC outputs and doubling output current drive capability. The parallel amplifier using Overture ICs is ineffective in obtaining higher output power levels with 8Ω loads because the ICs are voltage supply limited. However, the parallel topology provides a great way of achieving higher power levels while keeping within IC power dissipation limits by driving low impedance loads, which is the case for many self-powered speaker and powered subwoofer designs. The main advantage of the parallel configuration is its ability to divide total power dissipation between ICs, since each amplifier is providing half of the load current. Another advantage of the parallel design is that unlike the bridge design, more than two ICs can be used. In fact, any number of ICs can be used in a parallel design and when configured the same will share the power dissipation equally. For example, using four ICs to drive a 1Ω load means that each IC dissipates ¼ of the total power dissipation. In other words, the load to each IC looks like a 4Ω load (Number Of ICs in Parallel * Load Impedance = Load Impedance seen by each individual IC.) Odd numbers of ICs can also be used.

If the bridged and parallel configurations are combined, the outcome is a very high-power amplifier solution that far exceeds the capabilities of one IC alone, while maintaining reasonable power dissipation levels within each IC. The bridged portion doubles the output voltage swing and quadruples the total power dissipation while the parallel portion halves the current between each IC set and divides the total power dissipation between each of the four ICs. The result is higher system output power with each IC not exceeding its individual power dissipation capabilities. Higher output power levels are attained, while the ICs run at a normal temperature, keeping long-term reliability high. The schematic of the Bridged/Paralleled Amplifier is shown in *Figure 13.*

The data in the following sections will exemplify that the parallel, bridged, and bridged/paralleled solutions using multiple power ICs can meet high fidelity specifications while providing output power from 100W up to 400W. The low noise and excellent linearity traits of the monolithic IC are transferred to the high-power solution, making the circuit even more attractive. In addition, the protection mechanisms within the IC, which are not easily designed discretely, are inherently designed into the circuit, making the solution priceless.

While the data show what specs can be achieved by the configurations, as always, good design practices need to be followed to achieve the stated results. In addition to good electrical and layout design practices, the thermal design is equally critical with Overture ICs. The following section will expand on the thermal design aspects of Overture ICs. This concept of "design by power dissipation" is applicable to all types of high power solutions.

The PA100, BR100, and BPA200 schematics and test results exemplify what can be achieved with proper component selection, thermal design, and layout techniques. The PA100, BR100, and BPA200 demoboards are available from your regional National Semiconductor Business Center.

4.0 Thermal Background

The voltage and current ratings of a power semiconductor are typically the first specs considered in designing high power amplifiers. The same is true for an integrated monolithic power amplifier. However, power dissipation ratings are equally important to the long-term reliability of the power amplifier design. When using a monolithic IC in its intended application and within its specified capabilities, the thermal design is relatively straightforward. When an IC is used beyond is capabilities, as in high power circuits, power dissipation issues become more critical and not as straightforward. Therefore, the designer must understand the IC's power dissipation capabilities before using the IC in a booster configuration.

4.1 TYPICAL CHARACTERISTIC DATA

The power dissipation capabilities of a power IC are either specified in the datasheet or can be derived from its guaranteed output power specification. While the power dissipation rating for the LM3886T is 125W, this number can be misleading. Its power dissipation specification is derived from the IC's junction-to-case thermal resistance, θ_{JC} = 1˚C/W, the maximum junction temperature, T_J = 150˚C, and the ambient air, T_A = 25˚C. As stated in the datasheet, the device must be derated based on these parameters while operating at elevated temperatures. The heatsinking requirements for the application are based on these parameters so that the IC will not go into Thermal Shutdown (TSD). The real problem for Overture ICs, however, comes from the sensitivity of the output stage's unique SPiKe™ Protection which dynamically monitors the output transistor's temperature. While the thermal shutdown circuitry is enabled at T_J = 150˚C, SPiKe circuitry is enabled at T_J = 250˚C for instantaneous power spikes in the output stage transistor. As the overall temperature of the IC increases, SPiKe circuitry becomes even more sensitive causing it to turn on before the 125W limit is reached. TSD circuitry will continue to function globally for the IC in conjunction with the SPiKe circuitry. However, protection circuitry should not be activated under normal operating conditions. The question then becomes, what is the power dissipation limit for the IC such that SPiKe circuitry is not enabled? Knowing the power dissipation limit and keeping the case temperature of the IC as cool as possible will expand the output power capability without activating SPiKe Protection.

The other way to determine IC power dissipation capabilities is to analyze the output power specification in the datasheet. In the case of the LM3886T, there are two output power specification guarantees: 60W (min) into a 4Ω load using ±28V supplies and 50W(typ) into an 8Ω load from ±35V supplies. Using these two conditions and the theoretical maximum power dissipation equation shown below, results in the following maximum power dissipations:

4.2 SINGLE-ENDED AMPLIFIER Pdmax EQUATION:

$$P_{dmax} = V_{CCtot}^2/2\pi^2R_L$$

Non-Isolated LM3886T:

1. V_{CC} = ±28V, R_L = 4Ω

$$P_{dmax} = V_{CCtot}^2/2\pi^2R_L = (\pm 28V)^2/2\pi^2(4\Omega) = 39.7W$$

2. V_{CC} = ±35V, R_L = 8Ω

$$P_{dmax} = V_{CCtot}^2/2\pi^2R_L = (\pm 35V)^2/2\pi^2(8\Omega) = 31.0W$$

4.0 Thermal Background (Continued)

These results show that the IC can handle a maximum of ≈ 40W of continuous power dissipation without SPiKe Protection being turned on under continuous sinusoidal input with proper heat-sinking. The same theory applies to other Overture ICs as well, like the LM3876T, which is capable of dissipating 31W with proper heatsinking. It should be noted that the results shown above are for the Non-Isolated Power Package, where the back of the package is tied to the silicon substrate, or −Vee. The Isolated Power Package has overmolded plastic on the back keeping the package electrically isolated from the silicon substrate. This extra amount of plastic increases the package thermal resistance from 1˚C/W for the non-isolated version to ≈ 2˚C/W for the isolated version. The result of increased thermal resistance is higher die temperature under the same conditions.

Comparing the above maximum power dissipation in single-ended mode to the bridged-mode under the same electrical conditions shows that the IC's electrical conditions would need to be derated to keep within its power dissipation capabilities. Using the bridged-output Pdmax equation shown below, gives us the following results:

4.3 BRIDGED-OUTPUT AMPLIFIER Pdmax EQUATION

$$Pdmax = 4V_{cctot}^2/2\pi^2R_L = 2V_{cctot}^2/\pi^2R_L$$

The bridged-output Pdmax equation represents the bridged amplifier solution. If a dual amplifier IC is used like the LM1876T, then the total Pdmax would need to be dissipated in the single IC package. However, if two individual ICs are used, like two LM3886Ts, then the total power dissipation is divided between each IC.

Two Non-Isolted LM3886Ts:

1. $V_{cc} = \pm 28V$, $R_L = 4\Omega$

$$Pdmax = 4V_{cctot}^2/2\pi^2R_L = 4(\pm 28V)^2/2\pi^2(4\Omega) = 158.8W$$

$$Pdmax = 158.8W$$

$$Pdmax/IC = 79.4W$$

Therefore, using a bridged configuration, V_{cc} would have to be equal to ±20V to keep the IC's power dissipation within 40W when driving a 4Ω load! This equates to about 110W of output power in bridged-mode driving a 4Ω load. When driving an 8Ω load, and using the same bridged pdmax equation and a maximum of 40W of power dissipation, the supply voltages would have to be ±28V. This equates to about 120W of output power!

There are two major points to note here:

1. The maximum power dissipation analysis was taken into account using regulated power supplies. The IC for the whole analysis is being tested at the worst case power dissipation point for a constant full-load power supply voltage. When using an unregulated power supply, the no-load voltage will be somewhat higher (15%–35%) causing the overall maximum power dissipation to be higher than expected.
2. In the real "audio" application, the average music power dissipation is much less than the maximum power dissipation created by a sinusoidal input. Therefore, the IC will run cooler than expected due to the power dissipation.

However, when you put these two points together, they cancel out, but only for music stimulus. Most product qualifications go through worst case power dissipation scenarios which implies that sinusoids will be used with unregulated power supplies. Therefore, when doing the thermal portion of the design, the higher supply voltages will increase the IC power dissipation and must be taken into account.

4.4 THERMAL CONCLUSION

Because of National's portfolio of products and the capabilities of the bridged/paralleled circuit, the bridged solution is applicable for a power output window between 80W and 120W. Trying to exceed this power level without a rigorous thermal design will be difficult to achieve. More caution needs to be applied along with better thermal management for bridged circuit designs. The proposed bridged/paralleled solution is a more robust design than the bridged circuit, allowing higher output power levels to be obtained. By paralleling the two bridged sets of ICs, the amount of output power attainable is essentially limitless.

In addition to better heatsinking, the application of a small fan can substantially increase the IC's continuous power dissipation capabilities. While the air flow of the fan used to take the data is not known, its air flow seemed to be consistent with a typical computer fan. The IC maximum power dissipation data for an individual LM3886 is summarized below in *Table 1* The data shown below should only be used as a guideline of possible IC power dissipation capability. Your electrical design parameters and thermal management may be different, changing the achievable results. As always, lab testing is recommended to verify any solution.

TABLE 1. Power Dissipation Results

Power IC	Pdmax (No Fan)	Pdmax (With Fan)
LM3886T	40W	60W
LM3886TF	30W	45W

4.5 THERMAL TESTING CONDITIONS

The data summarized in *Table 1* was obtained by using the bridged/paralleled configuration and the following conditions: The system was warmed up for an hour using a power dissipation of 30W per device with a 4Ω load. Four different temperature points were measured after stabilizing, then the supply voltages were incremented while insuring that SPiKe Protection was not enabled during each test by monitoring each amplifier output. The supply voltages continued to be incremented until SPiKe protection or thermal shutdown was enabled, providing the IC's power dissipation limits under those operating conditions.

The input stimulus was a 20Hz sinewave with an amplitude corresponding to the worst case power dissipation for the given load and supply voltage. The ICs were evenly spread out along the heatsink with dimensions of: 3.25" high x 13.25" long x 1.3125" deep. The main body of the heatsink is 0.25" thick with (10) 1.0625" deep fins and the heatsink is black anodized. (See Appendix B, section 10.2 for detailed

4.0 Thermal Background (Continued)

drawing.) Unfortunately, the fins ran horizontally, which hindered heat radiation without a fan, but helped with air flow and heat dissipation when a fan was used.

This same testing procedure can be used for any number of booster circuits, including variations of the bridged/paralleled circuit. Another variation would be to add more ICs in parallel to further reduce power dissipation, allowing low impedance loads to be driven to obtain even higher output power levels.

5.0 BR100—100W Bridge Circuit

5.1 AUDIO TESTING

The following graphs represent the performance level attainable from the bridged circuit found in Figure 3 with a well designed PCB and properly heat sinked. The testing focused on maximum output power capabilities and amplifier linearity. The low THD+N plots shown on the following page exemplify the high degree of linearity of the bridged circuit which directly translates into a cleaner sounding more transparent amplifier. Other bridged circuit topologies that use the output of one amplifier as the input to the second inverting amplifier inherently possess higher THD and noise that will degrade the solution's sound quality.

5.1.1 LINEARITY TESTS

The linearity of the amplifier is represented by the low THD+N values shown in *Figures 1, 2. Figure 1* represents the THD+N vs Frequency for 1W, 56W, and 100W power levels. The 20kHz THD+N is less than 0.02% for 1W and about 0.008% for 56W and above. For normal listening levels, the THD+N is about 0.004% for most of the audio band. *Figure 2* represents the THD+N vs Output Power Level for 20Hz, 1kHz, and 20kHz. The THD+N between 20Hz and 1kHz is less than 0.004% from 1W to the clipping point. The 20kHz THD+N is less than 0.02% from 1W to the clipping point. The continuous clipping point power is around 105W while the power at 10% THD is about 140W. These THD graphs were obtained using relative THD units, which indicates that the noise level for the amplifier is quite low. Typically, the noise level becomes a significant THD+N contributor at low power levels and shows up as a linearly decreasing function of increasing input signal amplitude. The low power level THD+N for this amplifier is more than acceptable for home entertainment applications.

Figure 3 represents the bridged amplifier schematic. The design is extremely simple, consisting of a non-inverting power op amp configuration and an inverting power op amp configuration. The input to the amplifier solution goes to each individual configuration. While closed-loop gain matching is not critical, it is recommended to have fairly close values. The main functional point to note about this solution is that for a positive going input signal, amplifier U1 will have a positive changing output signal while U2 will have a negative changing output signal. The final voltage across the load is two times the peak amplitude of each individual amplifier output. Since output power is based on the square of the output voltage, the output power is theoretically quadrupled. This document will not go further into the functionality of the circuit as it is widely known in industry.

BR100 THD+N vs Freq R_i = 8Ω V_{CC} ±25.5V BW <80kHz P_O = 1W, 56W, 100W

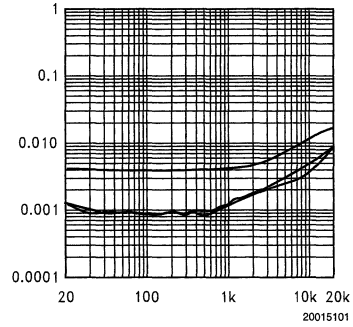

FIGURE 1. THD+N vs Frequency

BR100 THD+N(%) vs P_O @ f = 20Hz, 1 kHz, 20kHz R_i = 8Ω V_{CC} = ±25.5V BW <80kHz

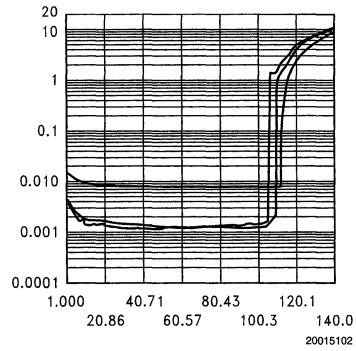

FIGURE 2. THD+N vs Output Power

5.0 BR100—100W Bridge Circuit

(Continued)

5.2 SCHEMATICS

5.2.1 Bridged Amplifier Schematic

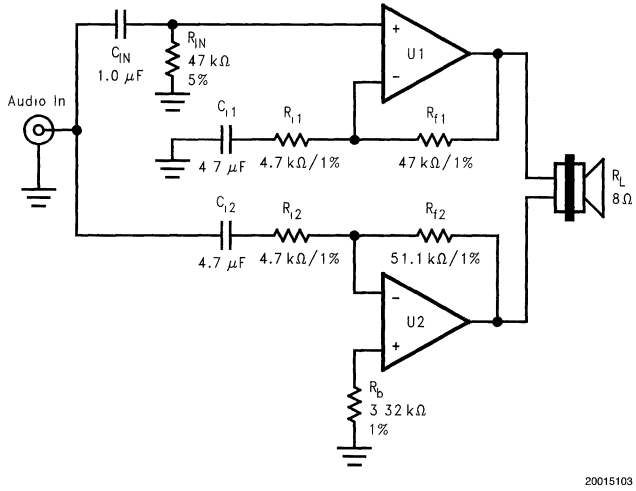

FIGURE 3. Bridged Amplifier Schematic

5.2.2 Electrical Design Notes

The following electrical design notes will aid in making the bridged amplifier design go more smoothly while also helping to achieve the highest level of performance.

- The input impedance of the inverting amplifier is essentially resistor, R_i. The value of this resistance affects the gain setting of the amplifier as well as the low frequency rolloff in conjunction with C_i. There is a tradeoff between having a low frequency rolloff, a high input impedance and a small capacitor size and value. It is critical to have a flat band response down to 20Hz while it is equally important to have a high enough input impedance so that heavy loading does not occur from the preamp stage. Using large valued low-cost capacitors implies the use of leaky electrolytics which affect the output offset voltage. Electrolytic capacitors are also less linear than other premium caps and should not be used in the signal path when not necessary. This tradeoff issue is the toughest portion of the design. The amplifier gain setting is just as one would expect for an inverting op amp. Of course, the input impedance issue can be quickly resolved by using a voltage follower as an input buffer, but it was omitted from this design to minimize cost and simplify the design. The values provided in the bridged schematic are at a good tradeoff point. There is sufficient input impedance for practically all audio op amps, the closed-loop gain setting is 11 for each amplifier, (gain of 22 overall) while the capacitor value of 4.7μF sets the low frequency −3dB rolloff at about 7Hz.
- The non-inverting input resistance, R_b, is used to create a voltage drop at the non-inverting terminal to offset the voltage at the inverting input terminal due to the input bias current flowing from the output to the inverting input. Generally, the value of this resistor equals the value of the feedback resistor so that the output offset voltage will be minimized close to zero. However, if this value is too large, noise can easily be picked up which will be amplified and seriously affect the THD+N performance. If the resistor is eliminated and the terminal is grounded, the THD+N performance will be much better, but it will not necessarily be optimized. By connecting the non-inverting input directly to a ground reference, any noise on that ground will be directly injected into the amplifier, amplified and thus will also affect the THD+N performance. The best solution is to use a value of resistance not too large to pick up stray noise and not too small as to be affected by ground noise fluctuations. The value used in the previous plots was a 3.32kΩ resistor. It should be noted that this is not necessarily the optimized value and can change with varying circuit layouts
- Low leakage signal path capacitors should be used where possible to reduce output offset voltages. This is not too big of an issue since each gain stage has only unity gain at DC. This is another reason why 1% resistor tolerances are not necessarily required. To obtain the highest quality amplifier, polypropylene capacitors should be employed in the signal path and supply bypassing.

5.0 BR100—100W Bridge Circuit

(Continued)

- As always, the better the supply bypassing, the better the noise rejection and hence higher performance.

6.0 PA100—100W Parallel Circuit

6.1 AUDIO TESTING

The following graphs are the same format as those presented in the BR100 analysis, namely THD+N verses Frequency at 1W, 56W and 100W and THD verses Output Power with plots at 20Hz, 1kHz, and 20kHz. Each IC uses a 2.2°C/W passive heat sink shown in Appendix B, section 10.1 and the demo board show in Appendix A, section 9.2.

6.1.1 Linearity Test

The linearity of the amplifier is represented by the low THD+N values shown in Figures 4, 5. Figure 4 represents the THD+N vs Frequency for 1W, 56W and 100W power levels. The 20kHz THD+N is less than 0.05% for all power levels. Figure 5 represents the THD+N vs Output Power Level for 20Hz, 1kHz, and 20kHz. The THD+N between 20Hz and 1kHz is less than 0.01% for power levels above 1W up to the clipping point. The 20kHz THD+N is 0.04% from 0.1W to the clipping point. The 1% THD power point is around 110W while the 10% THD power point is near 150W. These THD graphs were obtained using relative THD units, which indicates that the noise level for the amplifier is very low. Typically, the noise level becomes a significant THD+N contributor at lower power levels and shows up as a linearly decreasing function of increasing input signal amplitude. The low power level THD+N for this amplifier configuration is more than acceptable for home entertainment applications.

Figure 6 represents the parallel amplifier schematic. The design is extremely simple, consisting of two power op amps configured identically and tied in parallel to the load each through a 0.1Ω/3W resistor. The closer matched the gain of each IC the more equal the current sharing between them as well as the temperature of each IC due to power dissipation being near equal. This document will not go further into the functionality of the circuit as it is well known in industry.

PA100 THD+N vs Freq R_L = 4Ω, V_{CC} = ±35V BW < 80kHz, P_O = 1W, 56W, 100W

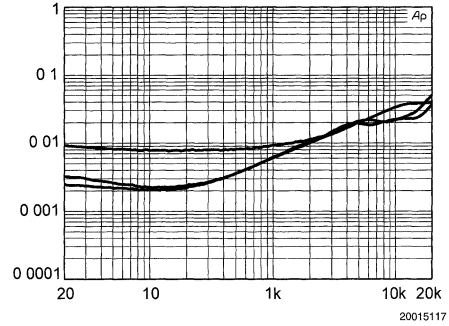

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FIGURE 4. THD+N vs Frequency

PA100 THD+N vs P_O @ f = 20Hz, 1kHz, 20kHz, R_L = 4Ω, V_{CC} = ±35V BW < 80kHz

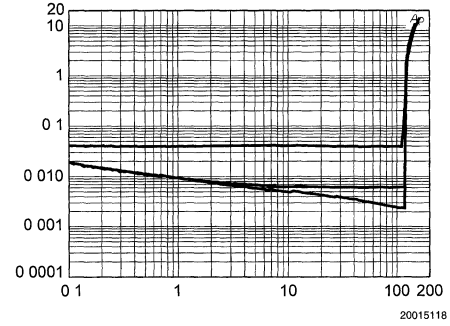

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FIGURE 5. THD+N vs Output Power

6.0 PA100—100W Parallel Circuit

(Continued)

6.2 SCHEMATICS

6.2.1 Parallel Amplifier Schematic

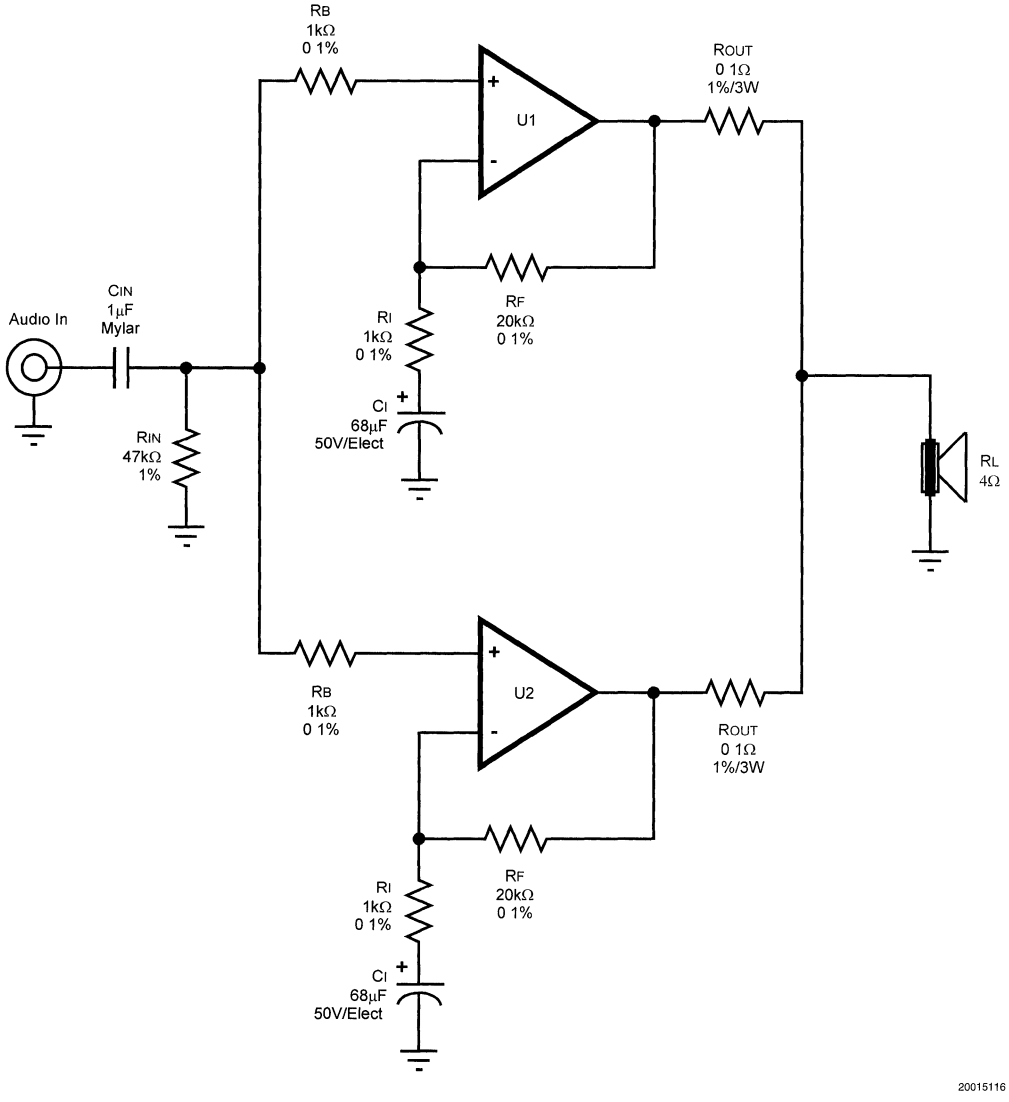


FIGURE 6. Parallel Amplifier Schematic

6.2.2 Electrical Design Notes

The following electrical design notes will aid in making the parallel amplifier design go more smoothly while also helping to achieve the highest level of performance.

- The input resistance is equal to R_{IN}.The value of R_{IN} should be high enough to eliminate any loading placed on the previous stage (i.e. pre-amplifier). The DC blocking input capacitor value should be calculated on the value of Rin to be sure the correct size is used so low frequency signals will be coupled in without severe attenuation. $f_{IN} = 1/(2\pi R_{IN} C_{IN})$.

6.0 PA100—100W Parallel Circuit

(Continued)

- 1% gain setting resistors (R_i and R_f) will give good results but it is recommended 0.1% tolerance resistors be used for setting the gain of each op amp for closer matched gain and equal output current and power dissipation.
- The output resistors, R_{OUT}, wattage rating is based on the load impedance and the output current or maximum output power. As the load impedance is increased or reduced the output current is reduced or increased, respectively. The wattage rating of R_{OUT} should increase as output current increases and decrease as output current decreases. A very conservative design will use peak output current to calculate the needed wattage rating of R_{OUT} ($P = I^2R$).
- As always, the better the supply bypassing, the better the noise rejection and hence higher performance.

7.0 BPA200—200W Bridged/Paralleled Circuit

7.1 AUDIO TESTING

The following graphs represent the performance level attainable from the bridge/paralleled circuit found in Figure 10 with a well designed PCB and properly heatsinked. The testing focused on maximum output power capabilities, amplifier linearity and noise level.

7.1.1 Linearity Tests

The linearity of the amplifier is represented by the low THD+N values shown in *Figures 7, 8. Figure 7* represents the THD+N vs Frequency for 1W, 56W, and 200W power levels. *Figure 8* represents the THD+N vs Output Power Level for 20Hz, 1kHz, and 20kHz. The THD+N between 20Hz and 1 kHz is less than 0.004% from 1W to the clipping point. The 20kHz THD+N is less than 0.02% from 1W to the clipping point, The continuous clipping point power is around 210W while the power at 10% THD is 300W. These THD graphs were obtained using relative THD units, which indicates that the noise level for the amplifier is quite low. Typically, the noise level becomes a significant THD+N contributor at low power levels and shows up as a linearly decreasing function of increasing input signal amplitude. In *Figure 8*, the THD+N decreases from 0.004% to 0.001% from 1W to the clipping point for frequencies between 20Hz and 1kHz. The THD+N with a 20kHz input decreases from 0.02% to 0.009% from 1W to 50W and rises thereafter up to about 0.015%.

BPA200 THD+N vs Frequency P_O = 1W, 56W, 200W R_i = 8Ω BW < 80 kHz 9/16/97

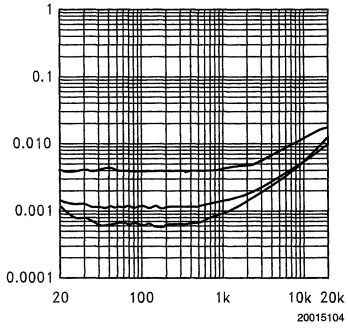


FIGURE 7. THD+N vs Frequency

BPA200 THD+N(%) vs P_O @ f = 20Hz, 1kHz, 200kHz R_i = 8Ω BW < 80kHz 9/16/97

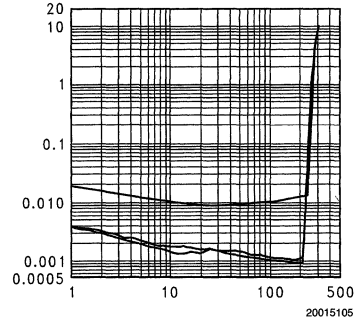


FIGURE 8. THD+N vs Output Power

7.1.2 Output Power Tests

Although the amplifier was deigned based on thermal dissipation capabilities using continuous sinusoidal inputs, the output power levels attainable are significantly greater with pulsed waveforms that more accurately reflect music material. The continuous clipping point power and burst power levels are shown in *Table 2* below:

TABLE 2. BPA200 Maximum Output Power Levels

Load Impedance	Continuous Clipping Point Power	Burst Clipping Point Power
8Ω	225W	295W
4Ω	335W	450W

The burst power levels were obtained using a 20Hz sinewave with two cycles on and twenty cycles off. The output power capability of the BPA200 is further substantiated by the power bandwidth measurement. The amplifier is capable of producing 200W continuously into an 8Ω load up to f = 90.5kHz with little change in THD+N. The graph in *Figure 9* shows the power bandwidth measurement. Also notice that the low frequency power in the graph is not rolled

7.0 BPA200—200W Bridged/Paralleled Circuit (Continued)

off as would normally occur with a DC blocking capacitor. The servo circuits allow the low frequency power to remain constant down to DC without high output offset voltage.

BPA200 Power Bandwidth @ P_o = 200W R_i = 8Ω BW > 500kHz 9/16/97

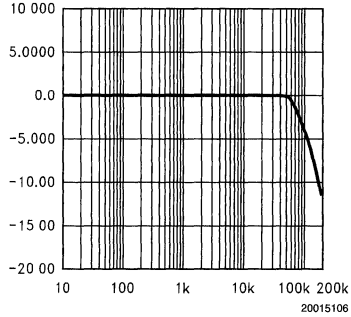


FIGURE 9. Power Bandwidth

7.1.3 Noise Floor Tests

The following plots exemplify the low-noise aspects of the BPA200. *Figure 10* was obtained using an 8k FFT relative to 1dBV with a measurement bandwidth of 22kHz. *Figure 11* is the same measurement as *Figure 10*, but shown in a logarithmic scale.

BPA200 Spot Noise Floor (dBV) R_i = 8Ω BW < 22kHz 9/16/97

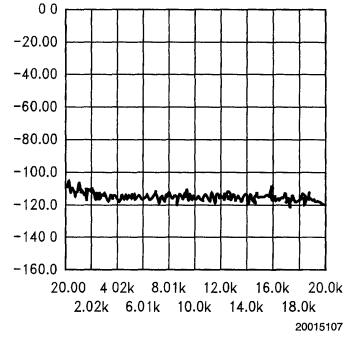


FIGURE 10. Linear-Scale Noise Floor

BPA200 Noise Floor (dBV) R_i = 8Ω BW < 22 kHz 9/16/97

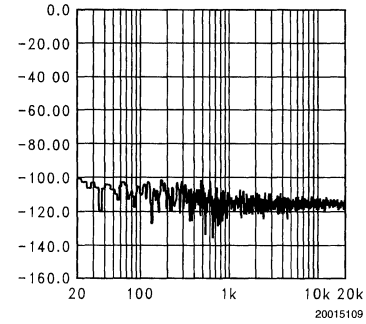


FIGURE 11. Log-Scale Noise Floor

An FFT analyzer is extremely handy in determining the noise culprit when debugging a new circuit and its layout, as well as evaluating the coupling effects of the 60Hz component and its harmonics. As shown in *Figure 12*, the noise level is quite low and the influence of the power supply is relatively small. The highest 60Hz components reach −105dBV, while the noise floor sits around −120dBV.

BPA200 Noise Floor (dBV) R_i = 8Ω BW < 22 kHz 9/16/97

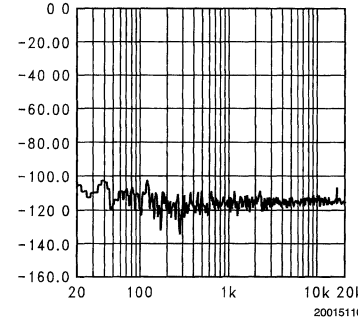


FIGURE 12. Log-Scale 60 Hz Noise Floor

Even with the limited number of graphs shown, the quality of this amplifier from a measurement perspective is quite good. However, with all audio equipment, nothing is really better than doing a listening test. It is recommended that listening test be done to confirm the audio quality of the different configurations presented.

7.0 BPA200—200W Bridged/Paralleled Circuit (Continued)

7.2 SCHEMATICS

7.2.1 Detailed Bridged/Paralleled Amplifier Schematic

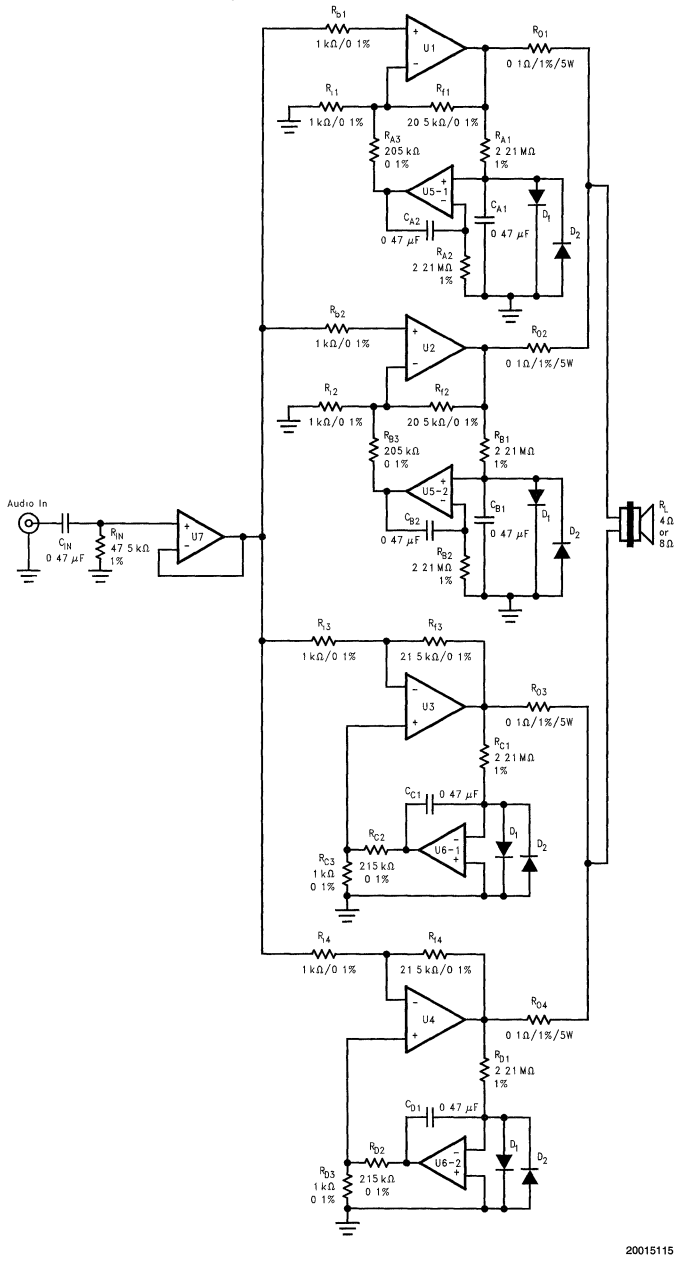


FIGURE 13. Detailed Bridged/Paralleled Amplifier Schematic

7.0 BPA200—200W Bridged/Paralleled Circuit (Continued)

7.2.2 Servo Circuits

While output ballast resistors in the basic bridge/paralleled circuit work well to keep separately biased IC outputs from fighting each other, the addition of servo circuits will minimize output offset voltages that cause output voltage inequalities. Different output offset voltages cause a constant current to flow between outputs that increases IC power dissipation. By minimizing output offset voltages, all of the ICs will run cooler, expanding the IC's long-term reliability and output power capability without activating sensitive protection circuits.

Typically, offset voltages are compensated for by using input and output coupling capacitors. Power amplifiers used in a single-supply configuration, utilize large value, large size electrolytic or polypropylene capacitors. This is because the load impedance is 4Ω or 8Ω and the RC combination creates a highpass filter that can rolloff audio frequencies. Since these output coupling capacitors have nonlinearities and are quite large, many designers choose to employ split power supplies. While split power supplies don't use these capacitors, a DC blocking capacitor is needed somewhere in the circuit to protect speakers. This capacitor is typically, C_{i1}, C_{i2}, C_{i3}, and C_{i4} as shown in *Figure 13*. With the application of a servo circuit, this capacitor can also be eliminated as shown in *Figures 14, 15*.

Servo circuits are essentially integrator op amp circuits that integrate offset voltage changes from the power op amp's output and feed back the integrated voltage to the opposite input of the power op amp. A servo circuit is required at each IC output of the bridge/paralleled circuit to keep currents from flowing between IC outputs. Without each output compensated, one offset voltage will cause current to flow between ICs increasing power dissipation. If gain setting resistors are 0.1% and closely matched, the servo circuit may be left out, but DC blocking capacitors will be required.

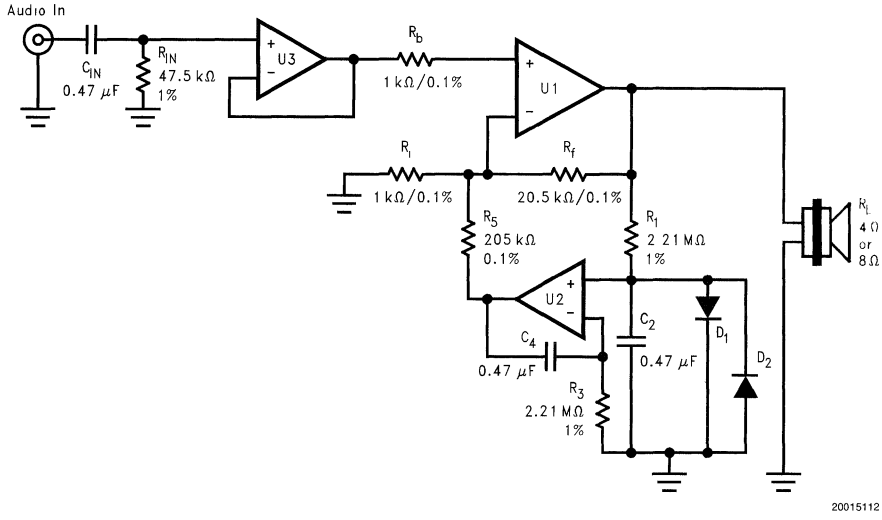


FIGURE 14. Non-Inverting Servo Amplifier Schematic

The inverting type servo amplifier applied to the inverting amplifier portion of the bridge/paralleled circuit is shown in *Figure 15*. The non-inverting type servo circuit could be applied to the inverting input of U1 to achieve the same result, however, it uses an extra RC network that can be eliminated with the inverting type servo.

If a different power amplifier gain is desired, other component values can be used under the following conditions: In *Figure 14*, resistor R5 should be about 10 times the value of R_f, while R_i and R_b should be equal. In , *Figure 15*, resistor R3 should be about 10 times the value of R_f, while R_4 and R_i should be equal. For both the Non-Inverting and Inverting Servo solutions, the input clamping diodes should be low-leakage, with low-leakage film capacitors having a high-quality dielectric such as polypropylene or polystyrene (mylar), and metal-film resistors.

7.0 BPA200—200W Bridged/Paralleled Circuit (Continued)

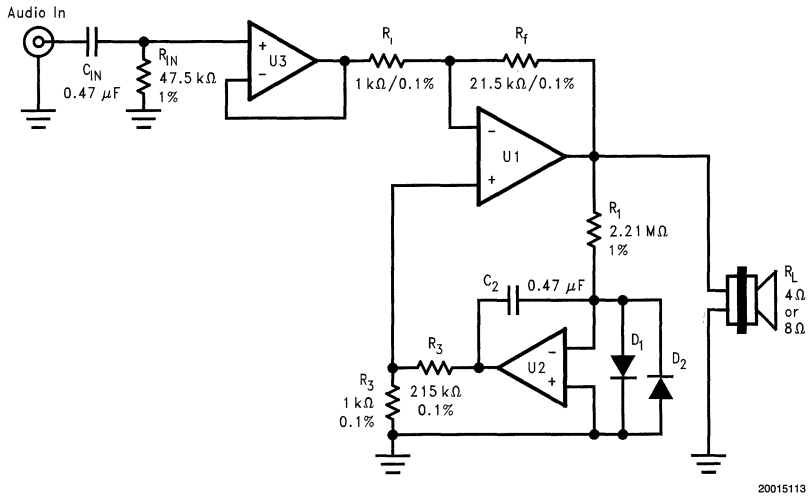


FIGURE 15. Inverting Servo Amplifier Schematic

7.2.3 Power Supply Circuit

The power supply portion of the amplifier is made up of a typical unregulated bipolar power supply. The supply is comprised of an input AC line filter, surge protecting MOVs, a separate 385VA toroidal transformer for each channel, and 40,000µF of supply reservoir capacitance for each supply voltage rail.

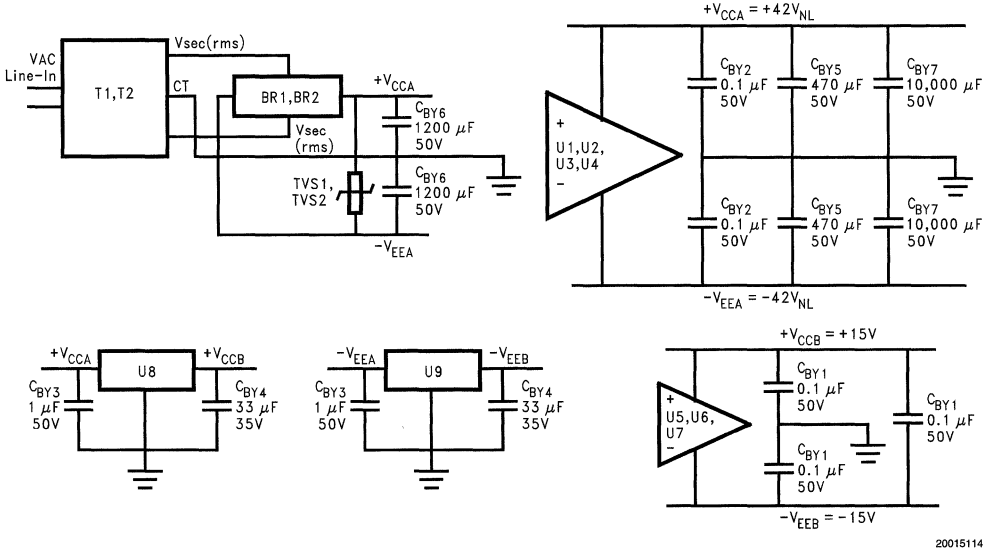


FIGURE 16. Power Supply Schematic

7.0 BPA200—200W Bridged/Paralleled Circuit (Continued)

7.2.4 Basic Bridged/Parallel Amplifier Schematic

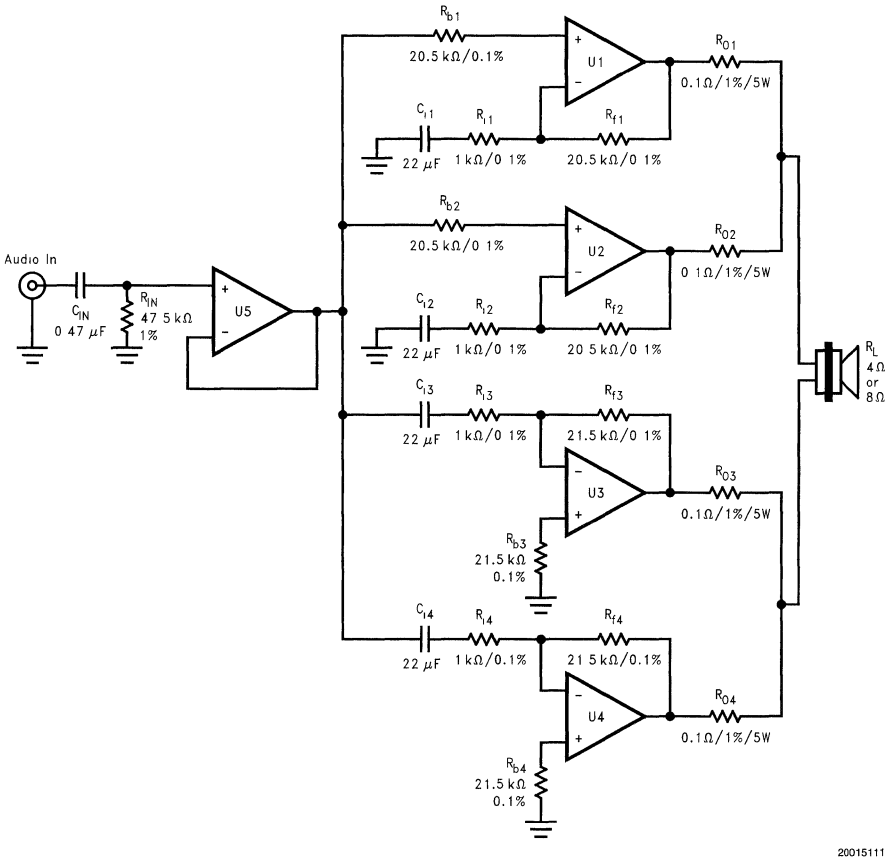


FIGURE 17. Basic Bridged/Paralleled Amplifier Schematic

8.0 Parts List And Vendors

8.1 BUILD OF MATERIALS FOR BR100 AMPLIFIER

(See Figure 3 Bridged Amplifier Schematic)

Description	Designator	Manufacturer's or Example Part Number
1.0µF/100V Metallized Polyester Fim Capacitor	C_{IN}	Panasonic,ECQ-E1105KF
4.7µF/35V/Electrolytic Capacitor	Ci1, Ci2	Panasonic, ECE-A1VN4R7U
47kΩ/1/4W/5% Resistor	RIN	
4.7kΩ/1/4W/1% Resistor	Ri1, Ri2	
46.4kΩ/1/4W/1% Resistor	Rf1	
51.1kΩ/1/4W/1% Resistor	Rf2	
3.32kΩ/1/4W/1% Resistor	RB	
Additional Externals on Demo Board Not Shown on Schematic		
Description	**Designator**	**Functional Description and Example Part Number**
0.1µF/50V/Monolithic Ceramic Capacitor	CB1	IC Supply Bypass Capacitor
47µF/50V/Electrolytic Capacitor	CB2	IC Supply Bypass Capacitor Panasonic, EEU-FC1H470
4,700µF/50V/Electrolytic Capacitor	CB3	IC Supply Bypass Capacitor Panasonic,ECO-S1HP472BA
10µF/35V/Electrolytic Capacitor	CM	Turn on Mute
15kΩ/1/4W/5% Resistor	RM1	Turn on Mute
8.2kΩ/1/4W/5% Resistor	RM2	Turn on Mute
2.7Ω/1/4W/5% Resistor	RG	Signal GND to Power GND

8.2 BUILD OF MATERIALS FOR PA100 AMPLIFIER

(See Figure 6 Parallel Amplifier Schematic)

Description	Designator	Manufacturer's or Example Part Number
1.0µF/100V Metallized Polyester Film Capacitor	CIN	Panasonic, ECQ-E1105KF
68µF/50V Electrolytic Capacitor	Ci	Panasonic, EEU-FC1H680
47kΩ/1/4W/1% Resistor	RIN	
1.0kΩ/1/4W/0.1% Resistor	Ri	
20.0kΩ/1/4W/0.1% Resistor	RF	
1.0kΩ/1/4W/1% Resistor	RB	
0.1Ω/1/3W/1% Resistor	ROUT	
Additional Externals on Demo Board Not Shown on Schematic		
Description	**Designator**	**Functional Description and Example Part Number**
0.1µF/50V/Monolithic Ceramic Capacitor	C1	IC Supply Bypass Capacitor
47µF/50V/Electrolytic Capacitor	C2	IC Supply Bypass Capacitor Panasonic, EEU-FC1H470
2,200µF/50V/Electrolytic Capacitor	C3	IC Supply Bypass Capacitor Panasonic,EEU-FC1H222
0.1µF/50V/Monolithic Ceramic Capacitor	CSN	Snubber Network on Output
2.7Ω/1/4W/5% Resistor	RSN	Snubber Network on Output
LM340T5, Fixed +5V Regulator	LM340L-5	5V PCB Supply
10µF/25V/Electrolytic Capacitor	CM1	5V Output Bypass Capacitor
0.1µF/50V/Monolithic Ceramic Capacitor	CM2	5V Input Bypass Capacitor

8.0 Parts List And Vendors (Continued)

Description	Designator	Manufacturer's or Example Part Number
470Ω/1/2W/5% Resistor	RREG	Voltage Reducer for LM340 Input Voltage
20kΩ/1/4W/5% Resistor	RM1	Mute Circuit
1MΩ/1/4W/5% Resistor	RM2	Mute Circuit
120Ω/1/4W/5% Resistor	RLED	Current Limit for LED Indicators
2.7Ω/1/4W/5% Resistor	RG	Signal GND to Power GND
Ultra Bright LED Lamp, T-1 ¾ Standard Size, Green	LED	Indicator LED

8.0 Parts List And Vendors

(Continued)

8.3 BUILD OF MATERIALS FOR BPA200 AMPLIFIER

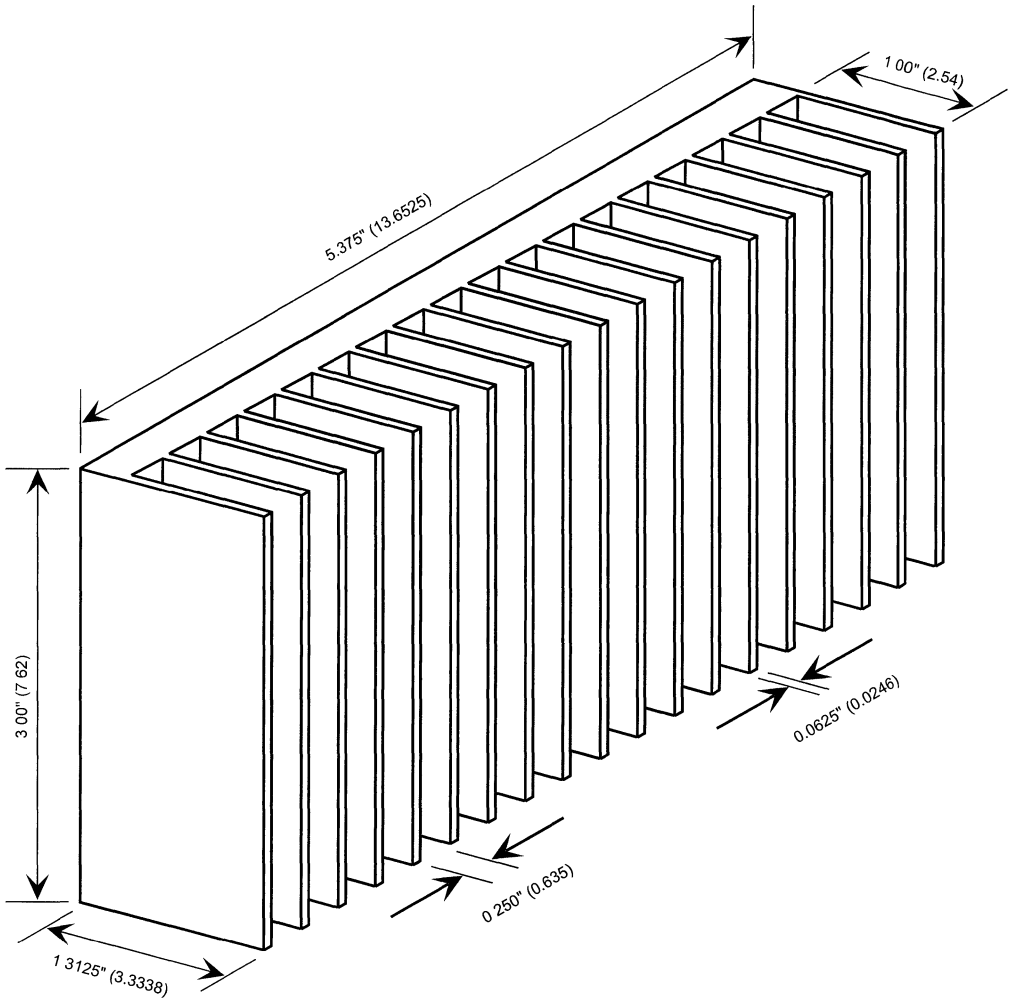
(See Figures 13 and 16, Detailed Bridged/Paralled Amplifier Schematic and Power Supply Schematic)

Description	Designator	Manufacturer's Part Number
PASSIVE COMPONENTS		
0.47µF/100V Mylar Capacitor	C_{A1}, C_{A2}, C_{B1}, C_{B2}, C_{C1}, C_{D1}, C_{IN}	Electrocube, 230B-0.47µF-100V-JB
0.1Ω/5W/1% Power Ballast Resistor	R_{O1}, R_{O2}, R_{O3}, R_{O4}	Dale, RS-5-0.1-1%
1kΩ/0.1% Metal Film Resistor	R_{b1}, R_{b2}, R_{i1}, R_{i2}, R_{i3}, R_{i4}, R_{C3}, R_{D3}	Dale, RN-55D-1000-B
47kΩ/1% Metal Film Resistor	R_{in}	Dale, RN-55D-4702
20.5kΩ/0.1% Metal Film Resistor	R_{f1}, R_{f2}	Dale, CMF-55-20.5k-.1%-T2
21.5kΩ/0.1% Metal Film Resistor	R_{f3}, R_{f4}	Dale, MF-55-21.5k-.1%-T2
205kΩ/0.1% Metal Film Resistor	R_{A3}, R_{B3}	Dale, CMF-55-205k-.1%-T2
215kΩ/0.1% Metal Film Resistor	R_{C2}, R_{D2}	Dale, CMF-55-215k-.1%-T2
2.21MΩ/1% Metal Film Resistor	R_{A1}, R_{A2}, R_{B1}, R_{B2}, R_{C1}, R_{D1}	Dale, CMF-55-2.21M-.5%-T9
1N456A Low Leakage Diodes	D_1, D_2	National Semiconductor (NSC) 1N456A
INTEGRATED COMPONENTS		
LM3886T, 50W Monolithic Power IC	U1, U2, U3, U4	NSC, LM3886T
LF412ACN, Dual JFET Input Op Amp	U5, U6	NSC, LF412ACN
LF411ACN, JFET Input Op Amp	U7	NSC, LF411ACN
LM78L15ACZ, +15V Linear Regulator	U8	NSC, LM78L15ACZ
LM79L15ACZ, −15V Linear Regulator	U9	NSC, LM79L15ACZ
POWER SUPPLY COMPONENTS		
385V A, 60 V_{rms} Sec. Transformer	T1, T2	Toroid Corp. of Maryland, #738.302
Bridge Rectifier	B_{R1}, B_{R2}	General Instrument, KBU8B
100V, 1.5kΩ Metal Oxide Varistor (Transient Voltage Surpressor)	TVS1, TVS2	Digikey, 1.5KE100CACT-ND
0.1µF/50V Ceramic Capacitor	C_{BY1}	Sprague, 1C25Z5U104M050B
0.1µF/50V Polypropylene	C_{BY2}	Panasonic, ECQ-P1H104GZ
1µF/50V Electrolytic Capacitor	C_{BY3}	
33µF/35V Electrolytic Capacitor	C_{BY4}	
470µF/50V Electrolytic Capacitor	C_{BY5}	Mallory, SKR471M1HJ21V
1200µF/50V Electrolytic Capacitor	C_{BY6}	Mallory, LP122M050A1P3
10,000µF/50V Electrolytic Capacitor	C_{BY7}	Panasonic, ECE-S1HU103U
AC Line Connector		Schurter, 34.3124
Power Switch (Bowden Cable)		Schurter, 886.0101
MISCELLANEOUS HARDWARE		
IC 11-Pin Sockets		Yamaichi, SMT-15420

9.0 Appendix A

9.1 BR100 AND PA100 HEAT SINK DRAWING

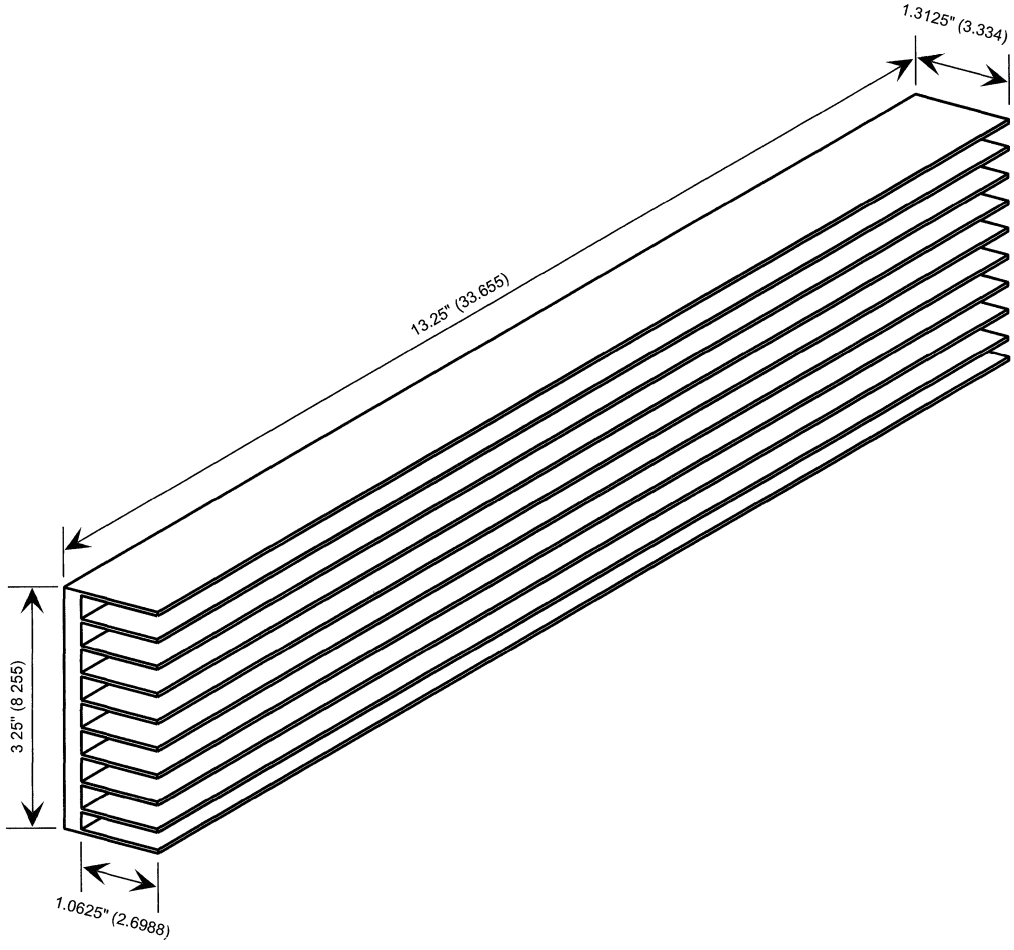
Inches (centimeters) unless otherwise noted



9.0 Appendix A (Continued)

9.2 BPA200 HEAT SINK DRAWING

Inches (centimeters) unless otherwise noted



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Section 6
Data Conversion

Section 6 Contents

Specifying A/D and D/A Converters

National Semiconductor
Application Note 156

The specification or selection of analog-to-digital (A/D) or digital-to-analog (D/A) converters can be a chancey thing unless the specifications are understood by the person making the selection. Of course, you know you want an accurate converter of specific resolution; but how do you ensure that you get what you want? For example, 12 switches, 12 arbitrarily valued resistors, and a reference will produce a 12-bit DAC exhibiting 12 quantum steps of output voltage. In all probability, the user wants something better than the expected performance of such a DAC. Specifying a 12-bit DAC or an ADC must be made with a full understanding of accuracy, linearity, differential linearity, monotonicity, scale, gain, offset, and hysteresis errors.

This note explains the meanings of and the relationships between the various specifications encountered in A/D and D/A converter descriptions. It is intended that the meanings be presented in the simplest and clearest practical terms. Included are transfer curves showing the several types of errors discussed. Timing and control signals and several binary codes are described as they relate to A/D and D/A converters.

Meaning of Performance Specs

Resolution describes the smallest standard incremental change in output voltage of a DAC or the amount of input voltage change required to increment the output of an ADC between one code change and the next adjacent code change. A converter with n switches can resolve 1 part in 2^n. The least significant increment is then 2^{-n}, or one least significant bit (LSB) In contrast, the most significant bit (MSB) carries a weight of 2^{-1}. Resolution applies to DACs and ADCs, and may be expressed in percent of full scale or in binary bits. For example, an ADC with 12-bit resolution could resolve 1 part in 2^{12} (1 part in 4096) or 0.0244% of full scale. A converter with 10V full scale could resolve a 2.44mV input change. Likewise, a 12-bit DAC would exhibit an output voltage change of 0.0244% of full scale when the binary input code is incremented one binary bit (1 LSB). Resolution is a design parameter rather than a performance specification; it says nothing about accuracy or linearity.

Accuracy is sometimes considered to be a non-specific term when applied to D/A or A/D converters. A linearity spec is generally considered as more descriptive. An accuracy specification describes the worst case deviation of the DAC output voltage from a straight line drawn between zero and full scale; it includes all errors. A 12-bit DAC could not have a conversion accuracy better than ±½ LSB or ±1 part in 2^{12+1} (±0.0122% of full scale) due to finite resolution. This would be the case in *Figure 1* if there were no errors. Actually, ±0.0122% FS represents a deviation from 100% accuracy; therefore accuracy should be specified as 99.9878%. However, convention would dictate 0.0122% as being an accuracy spec rather than an inaccuracy (tolerance or error) spec.

Accuracy as applied to an ADC would describe the difference between the actual input voltage and the full-scale weighted equivalent of the binary output code; included are quantizing and all other errors. If a 12-bit ADC is stated to be ±1 LSB accurate, this is equivalent to ±0.0245% or twice the minimum possible quantizing error of 0.0122%. An accuracy spec describes the maximum sum of all errors including quantizing error, but is rarely provided on data sheets as the several errors are listed separately

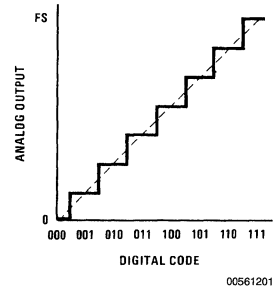


FIGURE 1. Linear DAC Transfer Curve Showing Minimum Resolution Error and Best Possible Accuracy

Quantizing Error is the maximum deviation from a straight line transfer function of a perfect ADC. As, by its very nature, an ADC quantizes the analog input into a finite number of output codes, only an infinite resolution ADC would exhibit zero quantizing error. A perfect ADC, suitably offset ½ LSB at zero scale as shown in *Figure 2*, exhibits only ±½ LSB maximum output error. If not offset, the error will be −1/+0 LSB as shown in *Figure 3*. For example, a perfect 12-bit ADC will show a ±½ LSB error of ±0.0122% while the quantizing error of an 8-bit ADC is ±½ part in 2^8 or ±0.195% of full scale. Quantizing error is not strictly applicable to a DAC, the equivalent effect is more properly a resolution error.

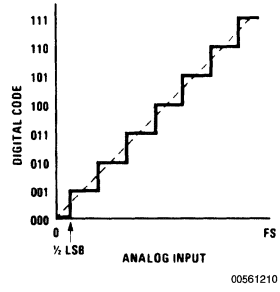


FIGURE 2. ADC Transfer Curve, ½ LSB Offset at Zero

Meaning of Performance Specs

(Continued)

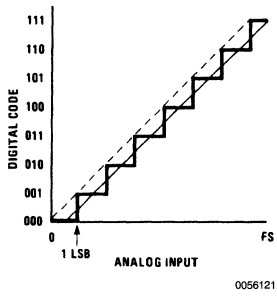


FIGURE 3. ADC Transfer Curve, No Offset

Scale Error (full scale error) is the departure from design output voltage of a DAC for a given input code, usually full-scale code. (See *Figure 4.*) In an ADC it is the departure of actual input voltage from design input voltage for a full-scale output code. Scale errors can be caused by errors in reference voltage, ladder resistor values, or amplifier gain, *et. al.* (See **Temperature Coefficient**.) Scale errors may be corrected by adjusting output amplifier gain or reference voltage. If the transfer curve resembles that of *Figure 6*, a scale adjustment at ¾ scale could improve the overall ± accuracy compared to an adjustment at full scale.

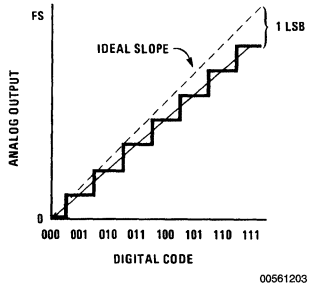


FIGURE 4. Linear, 1 LSB Scale Error

Gain Error is essentially the same as scale error for an ADC. In the case of a DAC with current and voltage mode outputs, the current output could be to scale while the voltage output could exhibit a gain error. The amplifier feedback resistors would be trimmed to correct the gain error.

Offset Error (zero error) is the output voltage of a DAC with zero code input, or it is the required mean value of input voltage of an ADC to set zero code out. (See *Figure 5.*) Offset error is usually caused by amplifier or comparator input offset voltage or current; it can usually be trimmed to zero with an offset zero adjust potentiometer external to the DAC or ADC. Offset error may be expressed in % FS or in fractional LSB.

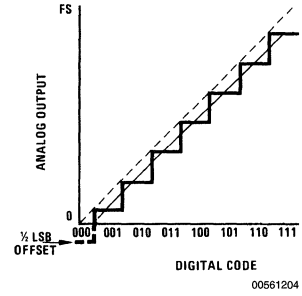


FIGURE 5. DAC Transfer Curve, ½ LSB Offset at Zero

Hysteresis Error in an ADC causes the voltage at which a code transition occurs to be dependent upon the direction from which the transition is approached. This is usually caused by hysteresis in the comparator inside an ADC. Excessive hysteresis may be reduced by design; however, some slight hysteresis is inevitable and may be objectionable in converters if hysteresis approaches ½ LSB.

Linearity, or, more accurately, non-linearity specifications describe the departure from a linear transfer curve for either an ADC or a DAC. Linearity error does not include quantizing, zero, or scale errors. Thus, a specification of ± ½ LSB linearity implies error in addition to the inherent ±½ LSB quantizing or resolution error. In reference to *Figure 2*, showing no errors other than quantizing error, a linearity error allows for one or more of the steps being greater or less than the ideal shown.

Figure 6 shows a 3-bit DAC transfer curve with no more than ±½ LSB non-linearity, yet one step shown is of zero amplitude. This is within the specification, as the maximum deviation from the ideal straight line is ±1 LSB (½ LSB resolution error plus ½ LSB non-linearity). With any linearity error, there is a differential non-linearity (see below). A ±½ LSB linearity spec guarantees monotonicity (see below) and ≤±1 LSB differential non-linearity (see below). In the example of *Figure 6*, the code transition from 100 to 101 is the worst possible non-linearity, being the transition from 1 LSB high at code 100 to 1 LSB low at 110. Any fractional non-linearity beyond ±½ LSB will allow for a non-monotonic transfer curve. *Figure 7* shows a typical non-linear curve; non-linearity is 1¼ LSB yet the curve is smooth and monotonic.

Meaning of Performance Specs

(Continued)

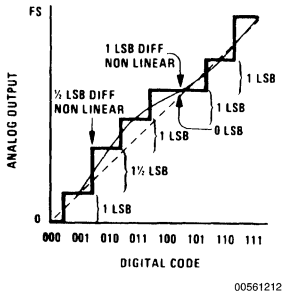


FIGURE 6. ±½ LSB Non-Linearity (Implies 1 LSB Possible Error), 1 LSB Differential Non-Linearity (Implies Monotonicity)

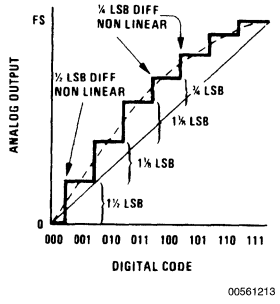


FIGURE 7. 1¼ LSB Non-Linear, ½ LSB Differential Non-Linearity

Linearity specs refer to either ADCs or to DACs, and do not include quantizing, gain, offset, or scale errors. Linearity errors are of prime importance along with differential linearity in either ADC or DAC specs, as all other errors (except quantizing, and temperature and long-term drifts) may be adjusted to zero. Linearity errors may be expressed in % FS or fractional LSB.

Differential Non-Linearity indicates the difference between actual analog voltage change and the ideal (1 LSB) voltage change at any code change of a DAC. For example, a DAC with a 1.5 LSB step at a code change would be said to exhibit ½ LSB differential non-linearity (see *Figure 6* and *Figure 7*). Differential non-linearity may be expressed in fractional bits or in % FS.

Differential linearity specs are just as important as linearity specs because the apparent quality of a converter curve can be significantly affected by differential non-linearity even though the linearity spec is good. *Figure 6* shows a curve with a ±½ LSB linearity and ±1 LSB differential non-linearity while *Figure 7* shows a curve with +1¼ LSB linearity and ±½ LSB differential non-linearity. In many user applications, the curve of *Figure 7* would be preferred over that of *Figure 6* because the curve is smoother. The differential non-linearity spec describes the smoothness of a curve; therefore it is of great importance to the user. A gross example of differential non-linearity is shown in *Figure 8* where the linearity spec is ±1 LSB and the differential linearity spec is ±2 LSB. The effect is to allow a transfer curve with grossly degraded resolution; the normal 8-step curve is reduced to 3 steps in *Figure 8*. Similarly, a 16-step curve (4-bit converter) with only 2 LSB differential non-linearity could be reduced to 6 steps (a 2 6-bit converter?) The real message is, "Beware of the specs." Do not ignore or omit differential linearity characteristics on a converter unless the linearity spec is tight enough to guarantee the desired differential linearity. As this characteristic is impractical to measure on a production basis, it is rarely, if ever, specified, and linearity is the primary specified parameter Differential non-linearity can always be as much as twice the non-linearity, but no more.

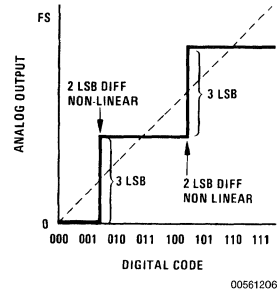


FIGURE 8. ±1 LSB Linear, ±2 LSB Differential Non-Linear

Monotonicity. A monotonic curve has no change in sign of the slope; thus all incremental elements of a monotonically increasing curve will have positive or zero, but never negative slope. The converse is true for decreasing curves. The transfer curve of a monotonic DAC will contain steps of only positive or zero height, and no negative steps. Thus a smooth line connecting all output voltage points will contain no peaks or dips. The transfer function of a monotonic ADC will provide no decreasing output code for increasing input voltage.

Figure 9 shows a non-monotonic DAC transfer curve. For the curve to be non-monotonic, the linearity error must exceed ±½ LSB no matter by how little. The greater the linearity error, the more significant the negative step might be. A non-monotonic curve may not be a special disadvantage is some systems; however, it is a disaster in closed-loop servo systems of any type (including a DAC-controlled ADC). A ±½ LSB maximum linearity spec on an n-bit converter guarantees monotonicity to n bits. A converter exhibiting more than ±½ LSB non-linearity may be monotonic, but is not necessarily monotonic. For example, a 12-bit DAC with ±½ bit linearity to 10 bits (not ±½ LSB) will be mono-

Meaning of Performance Specs

(Continued)

tonic at 10 bits but may or may not be monotonic at 12 bits unless tested and guaranteed to be 12-bit monotonic.

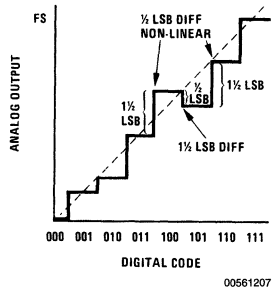
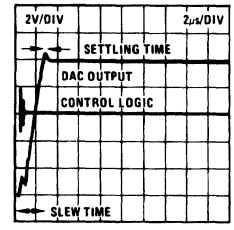


FIGURE 9. Non-Monotonic (Must be > ±½ LSB Non-Linear)

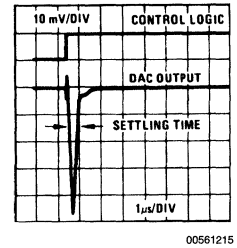
Settling Time is the elapsed time after a code transition for DAC output to reach final value within specified limits, usually ±½ LSB. (See also **Conversion Rate** below.) Settling time is often listed along with a slew rate specification; if so, it may not include slew time. If no slew rate spec is included, the settling time spec must be expected to include slew time. Settling time is usually summed with slew time to obtain total elapsed time for the output to settle to final value. *Figure 10* delineates that part of the total elapsed time which is considered to be slew and that part which is settling time. It is apparent from this figure that the total time is greater for a major than for a minor code change due to amplifier slew limitations, but settling time may also be different depending upon amplifier overload recovery characteristics.

Slew Rate is an inherent limitation of the output amplifier in a DAC which limits the rate of change of output voltage after code transitions. Slew rate is usually anywhere from 0.2 to several hundred volts/μs. Delay in reaching final value of DAC output voltage is the sum of slew time and settling time as shown in *Figure 10.*

Overshoot and Glitches occur whenever a code transition occurs in a DAC. There are two causes. The current output of a DAC contains switching glitches due to possible asynchronous switching of the bit currents (expected to be worst at half-scale transition when all bits are switched). These glitches are normally of extremely short duration but could be of ½ scale amplitude. The current switching glitches are generally somewhat attenuated at the voltage output of the DAC because the output amplifier is unable to slew at a very high rate; they are, however, partially coupled around the amplifier via the amplifier feedback network and seen at the output. The output amplifier introduces overshoot and some non-critically damped ringing which may be minimized but not entirely eliminated except at the expense of slew rate and settling time.



(a) Full-Scale Step



(b) 1 LSB Step

FIGURE 10. DAC Slew and Settling Time

Temperature Coefficient of the various components of a DAC or ADC can produce or increase any of the several errors as the operating temperature varies. Zero scale offset error can change due to the TC of the amplifier and comparator input offset voltages and currents. Scale error can occur due to shifts in the reference, changes in ladder resistance or non-compensating RC product shifts in dual-slope ADCs, changes in beta or reference current in current switches, changes in amplifier bias current, or drift in amplifier gain-set resistors. Linearity and monotonicity of the DAC can be affected by differential temperature drifts of the ladder resistors and switches. Overshoot, settling time, and slew rate can be affected by temperature due to internal change in amplifier gain and bandwidth. In short, every specification except resolution and quantizing error can be affected by temperature changes.

Long-Term Drift, due mainly to resistor and semiconductor aging can affect all those characteristics which temperature change can affect. Characteristics most commonly affected are linearity, monotonicity, scale, and offset. Scale change due to reference aging is usually the most important change.

Meaning of Performance Specs

(Continued)

Supply Rejection relates to the ability of a DAC or ADC to maintain scale, offset, TC, slew rate, and linearity when the supply voltage is varied. The reference must, of course, remain constant unless considering a multiplying DAC. Most affected are current sources (affecting linearity and scale) and amplifiers or comparators (affecting offset and slew rate). Supply rejection is usually specified only as a % FS change at or near full scale at 25°C

Conversion Rate is the speed at which an ADC or DAC can make repetitive data conversions. It is affected by propagation delay in counting circuits, ladder switches and comparators; ladder RC and amplifier settling times; amplifier and comparator slew rates; and integrating time of dual-slope converters. Conversion rate is specified as a number of conversions per second, or conversion time is specified as a number of microseconds to complete one conversion (including the effects of settling time). Sometimes, conversion rate is specified for less than full resolution, thus showing a misleading (high) rate.

Clock Rate is the minimum or maximum pulse rate at which ADC counters may be driven. There is a fixed relationship between the minimum conversion rate and the clock rate depending upon the converter accuracy and type. All factors which affect conversion rate of an ADC limit the clock rate.

Input Impedance of an ADC describes the load placed on the analog source.

Output Drive Capability describes the digital load driving capability of an ADC or the analog load driving capacity of a DAC; it is usually given as a current level or a voltage output into a given load.

Codes

Several types of DAC input or ADC output codes are in common use. Each has its advantages depending upon the system interfacing the converter. Most codes are binary in form; each is described and compared below.

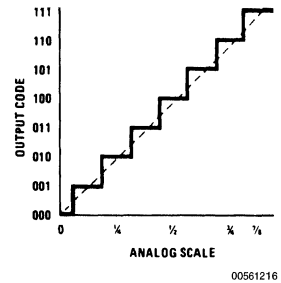
Natural Binary (or simply Binary) is the usual 2^n code with 2, 4, 8, 16, . . . , 2^n progression. An input or output high or "1" is considered a signal, whereas a "0" is considered an absence of signal. This is a positive true binary signal Zero scale is then all "zeros" while full scale is all "ones."

Complementary Binary (or Inverted Binary) is the negative true binary system. It is identical to the binary code except that all binary bits are inverted. Thus, zero scale is all "ones" while full scale is all "zeros."

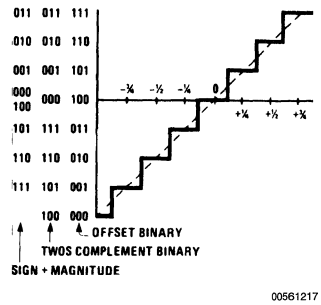
Binary Coded Decimal (BCD) is the representation of decimal numbers in binary form. It is useful in ADC systems intended to drive decimal displays. Its advantage over decimal is that only 4 lines are needed to represent 10 digits. The disadvantage of coding DACs or ADCs in BCD is that a full 4 bits could represent 16 digits while only 10 are represented in BCD. The full-scale resolution of a BCD coded system is less than that of a binary coded system. For example, a 12-bit BCD system has a resolution of only 1 part in 1000 compared to 1 part in 4096 for a binary system. This represents a loss in resolution of over 4:1.

Offset Binary is a natural binary code except that it is offset (usually ½ scale) in order to represent negative and positive values. Maximum negative scale is represented to be all "zeros" while maximum positive scale is represented as all "ones." Zero scale (actually center scale) is then represented as a leading "one" and all remaining "zeros." The comparison with binary is shown in *Figure 11.*

Two's Complement Binary is an alternate and more widely used code to represent negative values. With this code, zero and positive values are represented as in natural binary while all negative values are represented in a twos complement form. That is, the twos complement of a number represents a negative value so that interface to a computer or microprocessor is simplified. The twos complement is formed by complementing each bit and then adding a 1; any overflow is neglected. The decimal number –8 is represented in twos complement as follows: start with binary code of decimal 8 (off scale for ± representation in 4 bits so not a valid code in the ± scale of 4 bits) which is 1000; complement it to 0111; add 0001 to get 1000. The comparison with offset binary is shown in *Figure 11.* Note that the offset binary representation of the ± scale differs from the twos complement representation only in that the MSB is complemented. The conversion from offset binary to twos complement only requires that the MSB be inverted.



(a) Zero to + Full-Scale



(b) ± Full-Scale

FIGURE 11. ADC Codes

Sign Plus Magnitude coding contains polarity information in the MSB (MSB = 1 indicates a negative sign); all other bits represent magnitude only. This code is compared to offset binary and twos complement in *Figure 11.* Note that one code is used up in providing a double code for zero. Sign plus magnitude code is used in certain instrument and audio systems; its advantage is that only one bit need be changed

Codes (Continued)

for small scale changes in the vicinity of zero, and plus and minus scales are symmetrical. A DVM might be an example of its use.

Control

Each ADC must accept and/or provide digital control signals telling it and/or the external system what to do and when to do it. Control signals should be compatible with one or more types of logic in common use. Control signal timing must be such that the converter or connected system will accept the signals. Common control signals are listed below.

Start Conversion (SC) is a digital signal to an ADC which initiates a single conversion cycle. Typically, an SC signal must be present at the fall (or rise) of the clock waveform to initiate the cycle. A DAC needs no SC signal; however, such could be provided to gate digital inputs to a DAC.

End of Conversion (EOC) is a digital signal from an ADC which informs the external system that the digital output data is valid. Typically, an EOC output can be connected to an SC input to cause the ADC to operate in continuous conversion mode. In non-continuous conversion systems, the SC signal is a command from the system to the ADC. A DAC does not supply an EOC signal.

Clock signals are required or must be generated within an ADC to control counting or successive approximation registers. The clock controls the conversion speed within the limitations of the ADC. DACs do not require clock signals.

Conclusion

Once the user has a working knowledge of DAC or ADC characteristics and specifications, he should be able to select a converter to suit a specific system need. The likelihood of overspecification, and therefore an unnecessarily high cost, is likewise reduced. The user will also be aware that specific parameters, test conditions, test circuits, and even definitions may vary from manufacturer to manufacturer. For practical production reasons, parameters may not be tested in the same manner for all converter types, even those supplied by the same manufacturer. Using information in this note, the user should, however, be able to sort out and understand those specifications (from any manufacturer) pertinent to his needs.

References for A/D Converters

National Semiconductor
Application Note 184

Interfacing between digital and analog signals is becoming increasingly important with the proliferation of digital signal processing. System accuracy is often limited by the accuracy of the converter and a limitation of the converter is the voltage reference. Design can be difficult if the reference is external.

The accuracy of any converter is limited by the temperature drift or long term drift of the voltage reference, even if conversion linearity is perfect. Assuming that the voltage reference is allowed to add 1/2 least significant bit error (LSB) to the converter, it is surprising how good the reference must be when even small temperature excursions are considered. When temperature changes are large, the reference design is a major problem. *Table 1* shows the reference requirements for different converters while *Table 2* shows how the same problems exist with digital panel meters.

The voltage reference circuitry is required to do several functions to maintain a stable output. First, input power supply changes must be rejected by the reference circuitry. Secondly, the zener used in the reference must be biased properly, while other parts of circuitry scale the typical zener voltage and provides a low impedance output. Finally, the reference circuitry must reject ambient temperature changes so that the temperature drift of the reference circuitry plus the drift of the zener does not exceed the desired drift limit.

While zener temperature coefficient is obviously critical to reference performance, other sources of drift can easily add as much error as zener — even in voltage references with modest performance of 20 ppm/°C temperature drift. Zener drift and op amp drift add directly to the drift error, while resistor error is only a function of how well the scaling resistors track. Resistors which have a high TC can be used if they track.

For a 10V output with a 6.9V zener, the drift contribution of resistor mistracking is about 0.4 since the gain is 1.4. The range of temperature coefficient errors for different components used to make a 10V reference from a 6.9V zener are shown in *Table 3*. Another potential source of error, input supply variations, are negligible if the input is 1% regulated, and the resistor feeding the zener is stable to 1%.

Less frequently specified sources of error in voltage reference zeners are hysteresis and stress sensitivity. Stress on either a zener-diode junction or the series-temperature-compensating junction will cause voltage shifts. The axial leads on discrete devices can transmit stress from outside the package to the junction, causing 1 mV to 5 mV shifts.

Temperature cycling is the discrete zener can also induce non-reversible changes in zener voltage. If a zener is heated from 25°C to 100°C and then back to 25°C, the zener voltage may not return to its original value. This is because the temperature cycle has permanently changed the stress in the die, changing the voltage. This effect can be as high as 5 mV in some diodes and may be cumulative with many temperature cycles. The new planar IC zeners, such as the LM199 (temperature stabilized) or the LM129 are insensitive to stress and show only about 50 µV of hysteresis for a 150°C temperature cycle since the package does not stress the silicon chip.

Designing the Reference

If moderate temperature performance such as 20 ppm/°C is all that is needed, 2 different approaches can be used in the reference design. In the first, the temperature drift error is split equally between the zener and the amplifier or scaling resistors. This requires a moderately low drift zener and op amp with 10 ppm resistors.

TABLE 1. Maximum Allowable Reference Drift for 1/2 Least Significant Bits Error of Binary Coded Converter

TEMP CHANGE	BITS					
	6	8	10	12	14	
25°C	310	80	20	5	1.25	ppm/°C
50°C	160	40	10	2.5	0.6	ppm/°C
100°C	80	20	5	1.2	0.3	ppm/°C
125°C	63	16	3	1	0.2	ppm/°C

TABLE 2. Maximum Allowable Reference Drift for 1/2 Digit Error of Digital Meters

TEMP CHANGE	DIGITS								
	2	2½	3	3½	4	4½	5	5½	
25°C	200	100	20	10	2	1	0.2	0.1	ppm/°C
5°C			100	50	10	5	1	0.5	ppm/°C

Note 1: 0 01%/°C=100 ppm/°C, 0 001%/°C=10 ppm/°C, 0 0001%/°C=1 ppm/°C

Designing the Reference (Continued)

TABLE 3. Drift Error Contribution From Reference Components for a 10V Reference

DEVICE	ERROR	10V OUTPUT DRIFT
Zener	**Zener Drift**	
LM199A	0.5 ppm/°C	0.5 ppm/°C
LM199, LM399A	1 ppm/°C	1 ppm/°C
LM399	2 ppm/°C	2 ppm/°C
1N829, LM3999	5 ppm/°C	5 ppm/°C
LM129, 1N823A, 1N827A, LM329A	10–50 ppm/°C	10–50 ppm/°C
LM329, 1N821, 1N825	20–100 ppm/°C	20–100 ppm°C
Op Amp	**Offset Voltage Drift**	
LM725, LH0044, LM121	1 µV/°C	0.15 ppm/°C
LM108A, LM208A, LM308A	5 µV/°C	0.7 ppm/°C
LM741, LM101A	15 µV/°C	2 ppm/°C
LM741C, LM301A, LM308	30 µV/°C	4 ppm/°C
Resistors	**Resistance Ratio Drift**	
1% (RN55D)	50–100 ppm	20–40 ppm/°C
0.1% (Wirewound)	5–10	2–4 ppm
Tracking 1 ppm Film or Wirewound	—	0.4 ppm/°C

The second approach uses a very low drift zener and allows the buffer amplifier or scaling resistor to cause most of the drift error. This type of design is now made economical by the availability of low cost temperature stabilized IC zeners with virtually no TC. Further, the temperature coefficient of this reference is easily upgraded, if necessary. The 2 reference circuits are shown in *Figure 1* and *Figure 2*.

In *Figure 1*, an LM308 op amp is used to increase the typical zener output to 10V while adding a worst-case drift of 4 ppm/°C to the 10 ppm/°C of the zener. Resistors R3 and R4 should track to better than 10 ppm bringing the total error so far to 18 ppm. Since the output must be adjusted to eliminate the initial zener tolerance, a pot, R5 and R2 have been added. The loading on the pot by R2 is small, and there is no tracking requirement between the pot and R2. It is necessary for R2 to track R3 and R4 within 50 ppm.

In *Figure 2*, a low drift reference and op amp are used to give a total drift, exclusive of resistors of 3 ppm/°C. Now the resistor tracking requirement is relaxed to about 50 ppm, allowing ordinary 1% resistors to be used. The circuit in *Figure 2* is modified easily for applications requiring 3 ppm/°C to 5 ppm/°C overall drift by tightening the tracking of the resistors. For more accurate applications, the Kelvin sensing for both output and ground should be used. For even lower drifts, substituting a 1 µV/°C op amp, 1 ppm tracking resistors and an LM199A zener, overall drifts of 1 ppm/°C can be achieved. In both of the circuits, it is important to remember that the tracking of resistors can, at worst-case, be twice temperature drift of either resistance.

In both circuits, the zener is biased by a single resistor from the supply, rather than from the reference output. This eliminates possible start-up problems and, because of the 1Ω dynamic impedance of the IC zeners, only adds about 20 µV of error. Compensation for input changes is shown in *Figure 2*. Conventional zeners do not allow this biasing. A conventional 5 ppm reference such as the 1N829 has a dynamic impedance of about 15Ω. If it is biased from a resistor from a 1% regulated 15V supply, the operating current can change by 1.7% or 127 µA. This will shift the zener voltage by 1.9 mV or 60 ppm. With the IC zeners operating at 1 mA, a 1% shift in the supply will change the reference by 20 µV or 3 ppm. Further, power dissipation in the IC is only 7 mW, giving low warm-up drift compared to 7.5 mA zeners. The biasing resistor for the IC zener need not be any better than an ordinary 1% resistor since performance is independent of current.

When output voltages less than the zener voltage are desired, the IC zeners significantly simplify circuit design since no auxiliary regulator is needed for biasing. *Figure 3* shows a 5V reference circuit for use with a 15V input. In this case, zener drift contributes proportionally to the output drift while op amp offset drift adds a greater rate. With the 10V reference, 15 µV/°C from the op amp contributed 2 ppm/°C drift, but for the 5V reference, 15 µV/°C adds 3 ppm/°C. This makes op amp choice more important as the output voltage is lowered. Of course, if a high output impedance is tolerable, the op amp can be eliminated.

Designing the Reference (Continued)

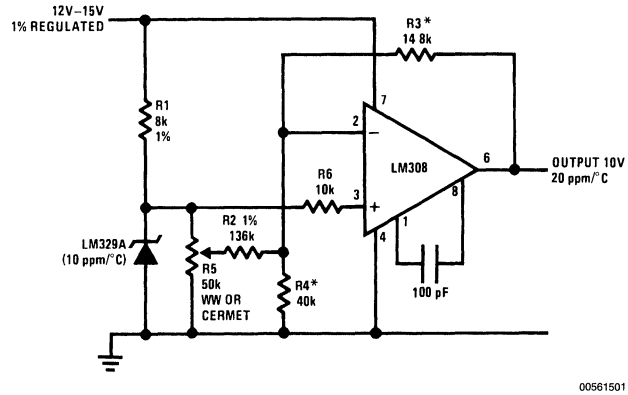
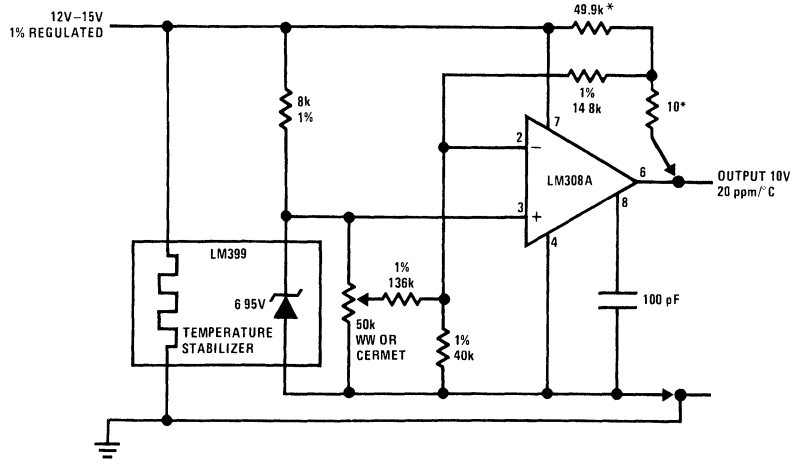


FIGURE 1. 10V, 20 ppm Reference Using a Low Cost Zener and Low Drift Resistors



*Optional — improves line regulation

FIGURE 2. 10V Reference has Low Drift Reference and Standard 1% Resistors. Kelvin Sensing is Shown with Compensation for Line Changes.

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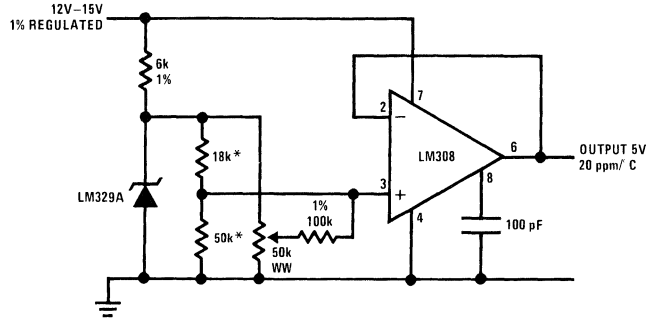
Designing the Reference (Continued)

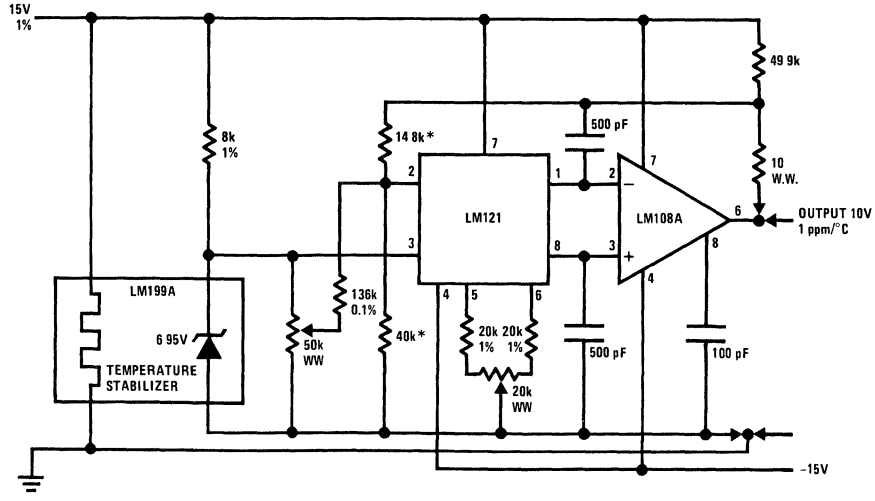


*20 ppm tracking

FIGURE 3. Low Voltage Reference

Approaching the Ultimate Drift

To obtain the lowest possible drifts, temperature coefficient trimming is necessary. With discrete zeners, the operating current can sometimes be trimmed to change the TC of the reference; however, the temperature coefficient is not always linear or predictable. With the new IC zeners, TC is independent of operating current so trimming must be done elsewhere in the circuit. The lowest drift components should be used since trimming can only remove a linear component of drift. High TC devices can have a highly non-linear drift, making trimming difficult. *Figure 4* shows a circuit suitable for trimming. An LM199A reference with 0.5 ppm/°C drift is used with a 121/108 op amp. Resistors should be 1 ppm tracking to give overall untrimmed drifts of about 0.9 ppm. The 121/108 is a low drift amplifier combination where drift is predictably proportional to offset voltage. An offset can be set for the 108/121 combination to cancel the measured drift with 1 pass calibration.



*1 ppm tracking

FIGURE 4. Ultra Low Drift Reference

Trimming procedure is as follows: the zener is disconnected and the input of the op amp grounded. Then the offset of the op amp is nulled out to zero. Reconnecting the zener, the output is adjusted to precisely 10V. A temperature run is made and the drift noted. The op amp will drift 3.6 µV/°C for every 1 mV of offset, so for every 5 µV/°C drift at the output,

Approaching the Ultimate Drift
(Continued)

the offset of the op amp is adjusted 1 mV (1.4 mV measured at the output) in the opposite direction. The output is readjusted to 10V and the drift checked.

Although this trimming scheme was chosen since only a single adjustment is usually required, compensation is not always perfect. Hysteresis effects can appear in resistors or op amps as well as zeners. Best results can be obtained by cycling the circuit to temperature a few times before taking data to relieve assembly stresses on the components. Also, oven testing can sometimes cause thermal gradients across circuits, giving 50 µV to 100 µV of error. However, with careful layout and trimming, overall reference drifts of 0.1 ppm/°C to 0.2 ppm/°C can be achieved.

There are 2 other possible problem areas to be considered before final layout. Good single point grounding is important. Traces on a PC board can easily have 0.1Ω and only 10 mA will cause a 1 mV shift. Also, since these references are close to high-speed digital circuitry, shielding may be necessary to prevent pick-up at the inputs of the op amp. Transient response to pick-up or rapid loading changes can sometimes be improved by a large capacitor. (1 µF—10 µF) directly on the op amp output; but this will depend on the stability of the op amp.

New Phase-Locked-Loops Have Advantages as Frequency to Voltage Converters (and more)

National Semiconductor
Application Note 210
Robert Pease

A phase-locked-loop (PLL) is a servo system, or, in other words, a feedback loop that operates with frequencies and phases. PLL's are well known to be quite useful (powerful, in fact) in communications systems, where they can pluck tiny signals out of large noises. Here, however, we will discuss a new kind of PLL which cannot work with low-level signals immersed in noise, but has a new set of advantages, instead. It does require a clean noise-free input frequency such as a square wave or pulse train.

This PLL can operate over a wide frequency range, not just 1 or 2 octaves but over 1 or 2 or 3 decades. It naturally provides a voltage output which responds quickly to frequency changes, yet does not have any inherent ripple. Thus, it can be used as a frequency-to-voltage (F-to-V) converter which does not have any of the classical limitations or compromises of (large ripple) vs (slow response), which most F-to-V converters have (Note 1). The linearity of this F-to-V converter will be as good as the linearity of the V-to-F converter used, and this linearity can easily be better than 0.01%. Other advantages will be apparent as we study the circuit further.

The basic circuit shown in *Figure 1* has all the functional blocks of a standard PLL. The frequency and phase detection do not consist of a quadrature detector, but of a standard dual-D flip-flop. When the frequency input is larger than F_2, Q1 will be forced high a majority of the time, and provide a positive error signal (via CR3, 4, 5, and 6) to the integrator.

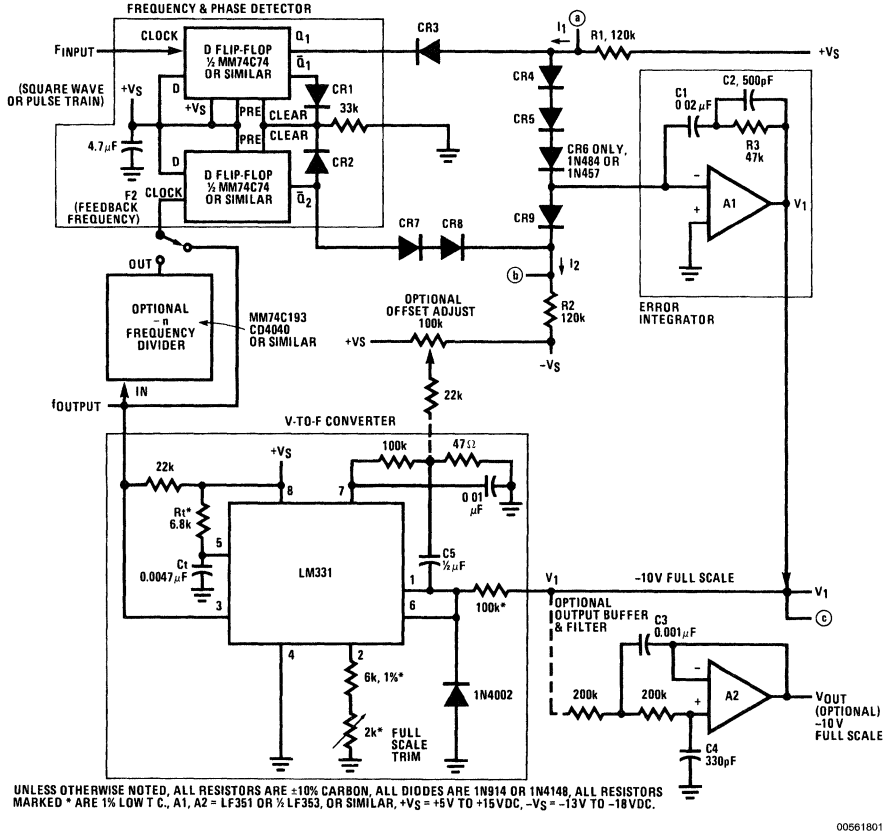


FIGURE 1. Basic Wide-Range Phase-Locked Loop

Note 1: See application note AN-C, "V/F Converter ICs Handle Frequency-to-Voltage Needs"

If F input and F_2 are the same, but the rising edges of F input lead the rising edges of F_2, the duty cycle of Q1=HI will be proportional to the phase error. Thus, the error signal fed to the integrator will decrease to nearly zero, when the loop has achieved phase-lock, and the phase error between F_{IN} and F_2 is zero. Actually, in this condition, Q1 will put out 30 nanosecond positive pulses, at the same time that Q2 puts out 30 nanosecond negative pulses, and the net effect as seen by the integrator is zero net charge. The 30 nanosecond pulses at Q1 and Q2 enable both flip-flops to be CLEARED, and prepared for the next cycle. This phase-detector action is substantially the same as that of an MC4044 Phase-Detector, but the MM74C74 is cheaper and uses less power. It is fast enough for frequencies below 1 MHz. (At higher frequencies, a DM74S74 can be used similarly, with very low delays.)

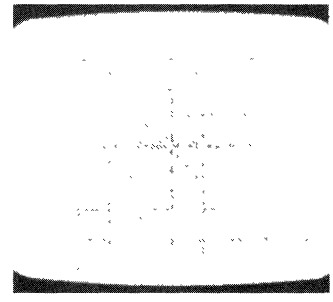
The error integrator takes in the current from R1 or R2, as gated by the Q1 and $\overline{Q2}$ outputs of the flip-flop. For example, when F_{IN} is higher, and Q1 is HIGH, I_1 will flow through CR4, 5, and 6 and cause the integrator's output to go more negative. This is the direction to make the V-to-F converter run faster, and bring F_2 up to F input. Note that A1 does not merely integrate this current in C1 (a mistake which many amateur PLL designers make). The resistor R3 in series with C1 makes a phase *lead* in the loop response, which is essential to loop stability. The small capacitor C2 across R3 is not essential, but has been observed to offer improved settling at the voltage output.

The output of the integrator, V1, is fed to a voltage-to-frequency (V-to-F) converter. The example shown here utilizes a LM331. This converter runs on a single supply, and responds quickly with nonlinearity better than 0.05% (even though an op-amp is not used nor needed). The output of the VFC is fed back to F_2, as a feedback frequency, either directly or through an (optional) frequency divider. Any number of standard frequency dividers such as MM74C193, CD4029, or CD4018, can be used, subject to reasonable limits. A divider of 2, 3, 10, or 16 is often used. The output voltage of the integrator will be proportional to the F input, as linearly as the V-to-F can make it. Thus, the integrator's output voltage V1 can be used as the output of an ultralinear F-to-V converter. However during the brief pulses when the flip-flop is CLEARing itself, there will be small glitches found on the output of A1. The RMS value of this noise may be very small, typically 0.5 to 5mV, but the peak amplitude, sometimes 10 to 100mV, can be annoying in some systems. And, no additional filtering can be added in the main loop's path, for any further delay in the route to the VFC would cause loop instability. Instead, the output may be obtained from a separate filter and buffer which operates on a branch path. A2 provides a simple 2-pole active filter (as discussed in Reference 1) which cuts the steady-state ripple and noise down below 1mV peak-to-peak, an excellent level for such a quick F-to-V (as we shall see).

What is not obvious about A2 is that its output can settle (within a specified error-band such as ±10 millivolts from the final DC value) earlier and more quickly than A1's output. The waveforms in *Figures 2, 3* show F_{IN} stepping up instantly from 5 kHz to 10 kHz; it also shows F_2 stepping up very quickly. The error signal at Q1 is also shown. The critical waveforms are shown in *Figures 4, 5*, the outputs of A1 and A2. While A1 puts out large spikes (caused by I1 flowing through R3), these large spikes cause the V-to-F converter to jump from 5 kHz to 10 kHz without any delay. There is, as shown in *Figures 2, 3*, a significant phase error between F_{IN} and F_2, but an inspection of these frequencies shows that frequency lock has been substantially instantaneous. Not one cycle has been lost. The phase lock and settling takes longer to achieve. Still, we know that if the frequency out of the VFC is 10 kHz, its input voltage must be −10 VDC. If there is noise on it, all we have to do is filter it in A2. *Figures 4, 5* shows that A2 settles very quickly — actually, in 2.0 milliseconds, which is just 20 cycles of the new frequency. A2's output has settled (i.e., the frequency has settled). While A1's output error (which is indicative of phase error being servo'ed out) continues to settle out for another 12 ms. Thus, this filter permits its output voltage to settle faster than its input, and it is responsible for the remarkable quickness of this circuit as an F-to-V converter. The waveforms of *Figures 4, 5* can be compared to the response (shown in *Figures 6, 7, 8, 9, 10*) of a conventional F-to-V converter. The upper trace is the output of a conventional FVC after a 4-pole filter (Note 2), and the lower trace is the output of the circuit of *Figure 1*. The phase-locked-loop F-to-V converter is quicker yet quieter.

Note 2: AN-207, V-to-F and F-to-V Converter Applications

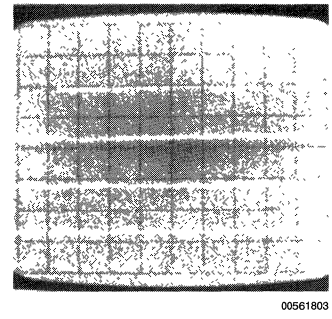
Vertical sensitivity=10 V/DIV (CMOS logic levels)
Horizontal sensitivity=0.5 ms/DIV



00561802

FIGURE 2. F output steps up from 5 kHz to 10 kHz as quickly as the input, never missing a beat.
Top Trace = input "F_{IN}" to PLL.
Bottom Trace = output "F_{OUT}" from PLL.

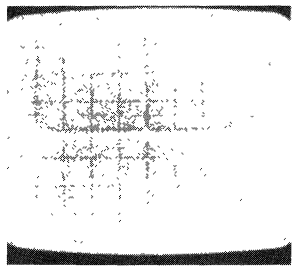
Vert=10 V/DIV, Horiz=2 ms/DIV



00561803

FIGURE 3. Error Signal. Top Trace = error signal at Q1.
Bottom Trace = output "F_{OUT}" from PLL.

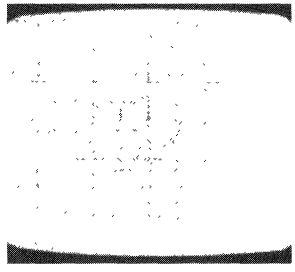
Vert = 2 V/DIV, Horiz = 2 ms/DIV



00561804

FIGURE 4. Settling waveforms, as F_{IN} goes from 5 kHz to 10 kHz and back again, using circuit of *Figure 1*. Top Trace = output of integrator (V1). Bottom Trace = output of filter (V_{OUT}).

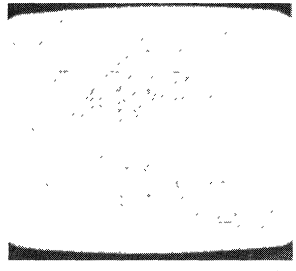
Vert = 2 V/DIV, Horiz = 0.5 ms/DIV



00561805

FIGURE 5. PLL Settling Waveforms. The same waveform as in *Figure 4*, but time base is expanded to 0.5 ms/DIV to show fine detail of settling.

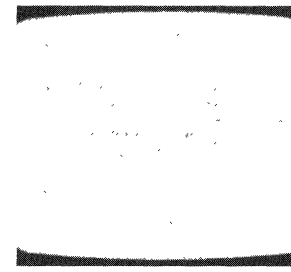
Vert = 2 V/DIV, Horiz = 20 ms/DIV



00561806

FIGURE 6. FVC Response vs PLL Response. The PLL can settle rather more quickly than a conventional F-to-V converter. Top Trace = conventional F-to-V converter with 4-pole active filter, responding to a 5 kHz to 10 kHz step. Bottom Trace = PLL FVC, with the same input, circuit of *Figure 1*.

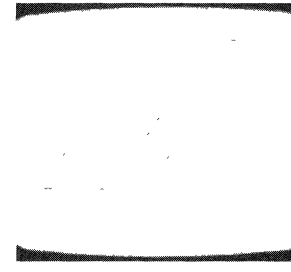
Vert = 2 V/DIV, Horiz = 20 ms/DIV



00561807

FIGURE 7. FVC Step Response. This waveform is similar to that in *Figure 6* but the frequency change covers a 10:1 ratio, from 10 kHz to 1 kHz and back to 10 kHz. For this waveform, the adaptive current sources of *Figure 11* connect to *Figure 1* (whereas for *Figure 6* R1 = R2 = 120k).

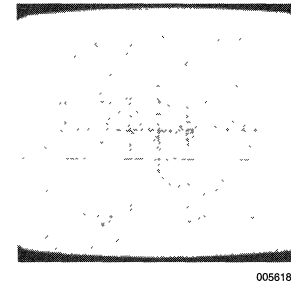
Vert = 2 V/DIV, Horiz = 5 ms/DIV



00561808

FIGURE 8. FVC Response. The same as *Figure 7*, but time base expanded to 5 ms/DIV, to show detail of rise time. Top Trace = conventional FVC. Bottom Trace = PLL FVC.

Vert = 2 V/DIV, Horiz = 5 ms/DIV



00561809

FIGURE 9. FVC Response The same as *Figure 7*, but expanded to 5 ms/DIV to show details of fall time. Top Trace = conventional FVC. Bottom Trace = PLL FVC.

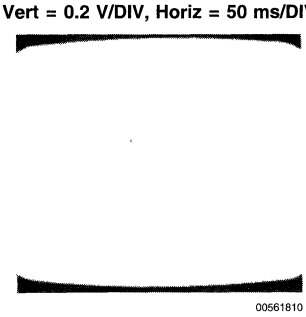


FIGURE 10. PLL Settling Waveforms at Low Frequencies. The same idea as in *Figure 7*, but 10 x slower, from 1.0 kHz to 100 Hz (and back). The settling to 1 kHz is still distinctly faster for the PLL, but at 100 Hz, it is a bit slower. Still, the PLL is faster than the FVC at all speeds from 200 Hz to 10 kHz.

So far we have shown a PLL which operates nicely over a frequency range of about 3:1. If the frequency is decreased below 3 kHz, the loop gain becomes excessive, and the currents I1 and I2 are large enough to cause loop instability. The loop gain increases at lower frequencies, because a given initial phase error will cause the fixed current from R1 or R2 to be integrated for a *longer* time, causing a *larger* output change at the integrator's output, and a *larger* change of frequency. When the frequency is thus corrected, and the period of one cycle is changed, at a low frequency it may be *over-corrected*, and the phase error on the next cycle may be as large as (or larger than) the initial phase error, but with reversed sign (Note 3). To avoid this and to maintain loop stability at lower frequencies, e.g. 0.5 to 1 kHz, R1 and R2 can be simply raised to 1.5 MΩ. However, response to a step will be proportionally slower. To achieve a wide frequency range (20:1), and optimum quickness at all frequencies, it is necessary to servo I1 and I2 to be *proportional to the frequency*. Fortunately, as V1 is normally proportional to F, it is easy to generate current sources I1' and I2' which are proportional to F. The circuit of *Figure 11* can be connected to the basic PLL, instead of R1 and R2, and provides good, quick loop stability over a 30:1 frequency range, from 330 Hz to 10 kHz. For best results over a 30:1 frequency range, change R3, the damping resistor in *Figure 1*, from 47k to 100k. However, if the frequency range is smaller (such as 2:1 or 3:1), constant resistors for R1 and R2 or very simple current sources may give adequate response in many systems. (To cover wider frequency ranges than 30.1 with optimum response, the circuits in the precision phase-locked-loop, below, are much more suitable.)

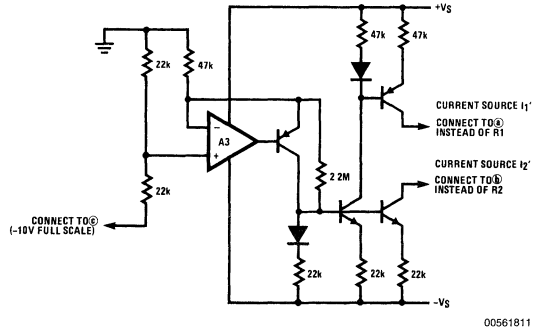
Often a frequency multiplier is needed, to provide an output frequency 2 or 3 or 10 or n times higher than the input. By inserting a ÷n frequency divider in the feedback loop, this is easily accomplished. [Of course, a ÷m frequency divider can be inserted ahead of the frequency input, to provide correct scaling, and the output frequency then will be $F_{IN}(n/m)$.]

To obtain good loop stability in a frequency multiplier with n = 2, remember that a 20 kHz V-to-F converter followed by a ÷2 circuit has exactly the same loop response and stability needs as a 10 kHz V-to-F converter, because it *is* a 10 kHz V-to-F converter, even though it provides a useful 20 kHz output. Thus, the frequency of the F_2 (minimum and maximum) will determine what loop gains and loop damping components are needed.

To accommodate a 1 kHz V-to-F loop, simply make C1 and C2 10 times bigger than the values of *Figure 1*; treating C3, C4, C5 and Ct similarly is used. To accommodate a 100 Hz V-to-F, increase them by another factor of 10.

If the PLL is to be used primarily as a frequency multiplier, it may be necessary to use stable, low-temperature-coefficient components, because the accuracy of V_{OUT} will not be important. The parts cost can be cut considerably. (Make sure that the VFC does not run out of range to handle all frequencies of interest.) On the other hand, the damping components will be chosen quite a bit differently if slow, stable jitter-free response is needed or if quick response is required. The circuits shown are just a starting place, to start optimizing your own circuit.

Note 3: Optimize phase-lock loops to meet your needs or determine why you can't Andrzej B Przedpelski, Electronic Design, September 13, 1978

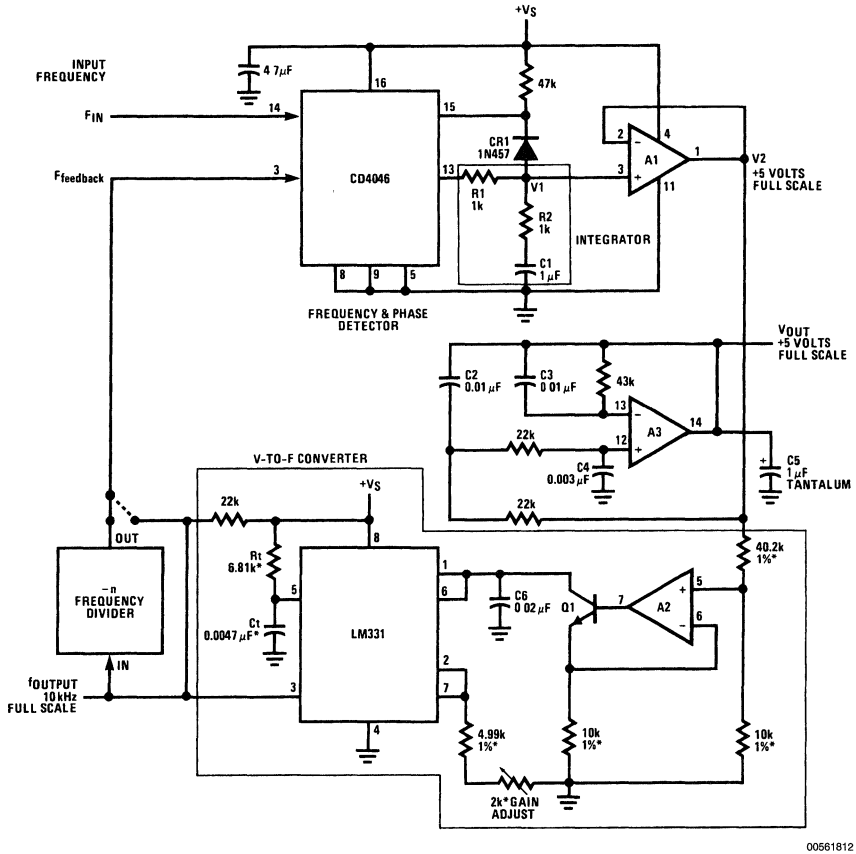


A3 — LF351, LM741 OR ANY NPN TRANSISTOR — 2N3904, 2N2222 OR ANY SILICON NPN , PNP TRANSISTOR — 2N3906, 2N2907 OR ANY SILICON PNP , ALL RESISTORS ±10%
ALL DIODES 1N914 OR 1N4148 OR SIMILAR

FIGURE 11. Proportional Current Source for Basic PLL

A Single-Supply PLL

The single-supply PLL is shown in *Figure 12* as an example of a simple circuit which is effective when battery operation or single-supply operation is necessary. This circuit will function accurately over a 10:1 frequency range from 1 kHz to 10 kHz, but will not respond as quickly as the basic PLL of *Figure 1*. The reason is the use of the CD4046 frequency detector. When an F_{IN} edge occurs ahead of a F feedback pulse, pin 13 of the CD4046 pulls up on C1 via R1 = 1 kΩ. This current cannot be controlled or manipulated over as wide a range as "I1" in *Figure 1*. As a consequence, the response of this PLL is never as smooth nor fast-settling as the basic PLL, but it is still better behaved than most F-to-V converters. As with the basic PLL, the detector feeds a current to be integrated in C1 (and R2 provides the necessary "lead"). A1 acts simply as a buffer for the R1, C1 integrator. A3, optional, can provide a nicely filtered output. And A2 servos Q1, drawing a current out of C6 which is proportional to V2. Here the LM331 acts as a current-to-frequency converter, and F output is precisely proportional to the collector current of Q1. As with the basic circuit, this PLL can be used as a quick and/or quiet F-to-V converter, or as a frequency multiplier. One of the most important uses of an F-to-V is to demodulate the frequency of a V-to-F converter, which may be situated at a high common-mode voltage, isolated by photoisolators, or to recover a telemetered signal. An F-to-V converter of this sort can provide good bandwidth for demodulating such a signal.



00561812

— Q1 = 2N3565 OR 2N3904 HIGH BETA NPN
— A1, A2, A3 = ¼ LM324
— ON CD4046, PINS 1, 2, 4, 6, 7, 10, 11, 12 ARE NO CONNECTION
— USE STABLE, LOW-T C PARTS FOR COMPONENTS MARKED*
—$+V_S$ = +7 TO +15 VDC

FIGURE 12. Single Supply Phase Locked Loop

A Single-Supply PLL (Continued)

The precision PLL in *Figure 13* acts very much the same as the basic PLL, with refinements in various places.

- The flip-flops in the detector have a gate G1 to CLEAR them, for quicker response.
- The currents which A1 integrates are steered through Q1, Q2 and Q3, Q4 because transistors are quicker then diodes, yet have much lower leakage
- The V-to-F converter uses A2 as an op-amp integrator, to get better than 0.01% nonlinearity (max).
- G2 is recommended as an inverter, to invert the signal on the LM331's pin 3, avoid a delay, and improve loop stability. (However, we never found any *real* improvement in loop stability, despite theories that insist it must be there Comments are invited.)

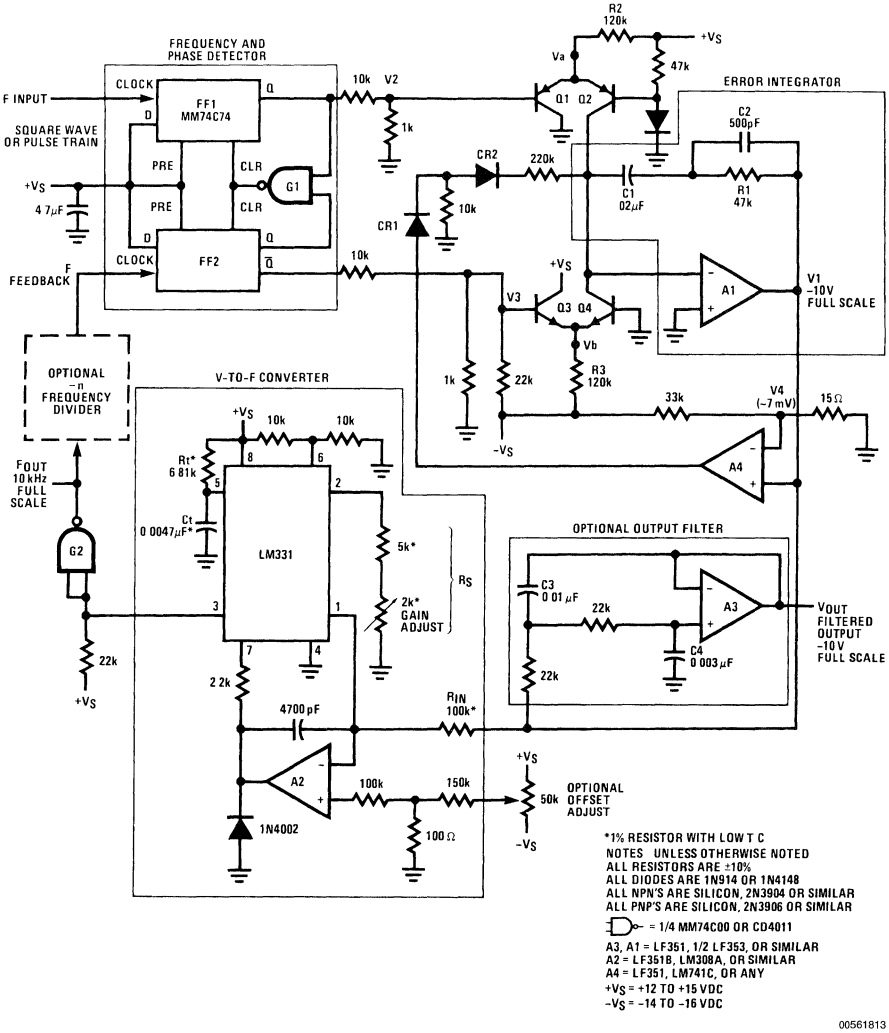


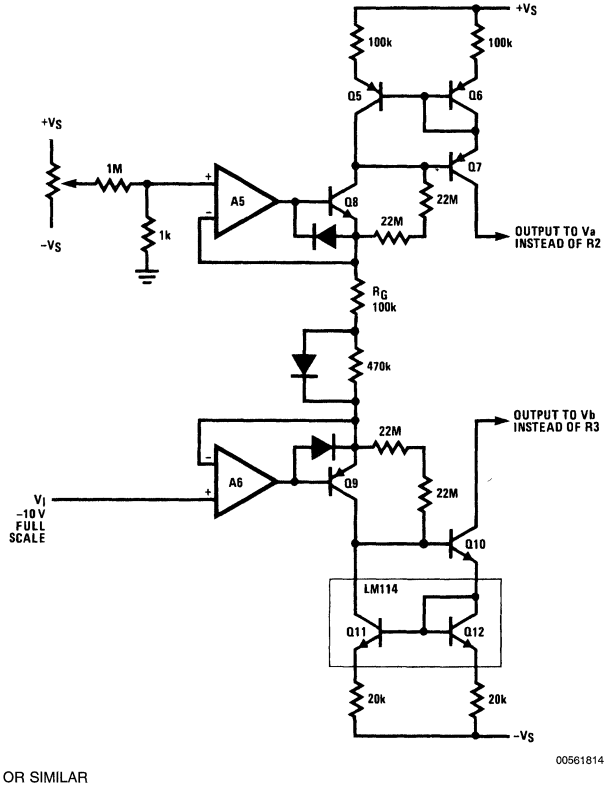
FIGURE 13. Precision PLL

A Single-Supply PLL (Continued)

- A4 is included as an (optional) limiter, to prevent V1 from ever going positive. This will facilitate quick startup and recovery from overdrive conditions.

Also, in *Figure 14*, the wide-range current pump for the precision PLL is a "semiprecision" circuit, and provides an output current proportional to −V1, give or take 10 or 15%, over a 3-decade range. The 22 MΩ resistors prevent the current from shutting off in case −V becomes positive (probably unnecessary if A4 is used). For best results over a full 3-decade range (11 kHz to 9 Hz), do use A4, delete the four 22 MΩ resistors, and insert the (diode parallel to the 470 kΩ) in series with the R_G as shown. This will give good stability at all frequencies (although stability cannot be extended below 1/1500 of full scale without extra efforts).

This PLL has been widely used in testing of VFCs, as it can force the LM331 to run at a crystal-controlled frequency (established as the F input), and the output voltage at V_{OUT} is promptly measured by a 6-digit (1 ppm nonlinearity, max) digital voltmeter, with much greater speed and precision than can be obtained by forcing a voltage and trying to read a frequency. While at 10 kHz, the advantages are clearcut; at 50 Hz it is even more obvious. Measuring a 50 Hz signal with ±0.01 Hz resolution cannot be done (even with the most powerful computing counter-timer) as accurately, quickly, and conveniently as the PLL's voltage output settles.



A5, A6, ARE LF351 OR ½LF353 OR SIMILAR

Q5, Q6, Q7, Q9 ARE 2N2907 OR 2N3906 OR SIMILAR

Q8, Q10 ARE Q8 IS 2N3565 OR 2N3904 OR SIMILAR

FIGURE 14. Wide Range Current Pumps for Precision PLL of *Figure 13*

One final application of this PLL is as a wide-range sine generator. The VFC in *Figure 15* puts out an adequate sine-shaped output, but does not have good V-to-F linearity, and its frequency stability is not much better than 0.2%. An LM331 makes an excellent linear stable V-to-F converter, with a pulse output; but it can not make sines. But it can command, via a PLL, to force the sine VFC to run at the correct frequency. Simply connect the sine VFC of *Figure 15* into one of the PLLs, instead of the LM331 VFC circuit. Then use a precise linear low-drift VFC based on the LM331 to establish the F_{IN} to the PLL. If the voltage needed by the sine VFC to put out a given frequency drifts a little, that is okay, as the integrator will servo and make up the error. The use of a controlled sine-wave generator in a test system was the first of many applications for a wide-range phase-locked-loop.

A Single-Supply PLL (Continued)

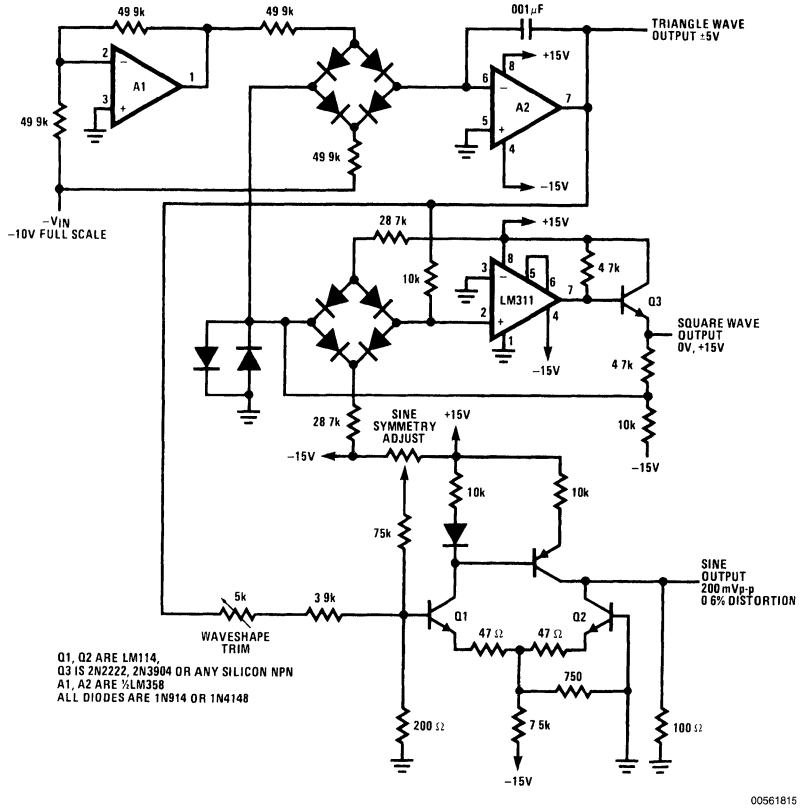


FIGURE 15. Sine-Wave VFC to Use with PLL

The A/D Easily Allows Many Unusual Applications

National Semiconductor
Application Note 233
Robert Pease

Accommodation of Arbitrary Analog Inputs

Two design features of the ADC0801 series of A/D converters provide for easy solutions to many system design problems. The combination of differential analog voltage inputs and a voltage reference input which can range from near zero to $5V_{DC}$ are key to these application advantages.

In many systems the analog signal which has to be converted does not range clear to ground (0.00 V_{DC}) nor does it reach up to the full supply or reference voltage value. This presents two problems: 1) a "zero-offset" provision is needed—and this may be volts, instead of the few millivolts which are usually provided; and 2) the "full scale" needs to be adjusted to accommodate this reduced span. ("Span" is the actual range of the analog input signal, from $V_{IN\ MIN}$ to $V_{IN\ MAX}$.) This is easily handled with the converter as shown in *Figure 1.*

Note that when the input signal, V_{IN}, equals $V_{IN\ MIN}$ the "differential input" to the A/D is zero volts and therefore a digital output code of zero is obtained. When V_{IN}equals $V_{IN\ MAX}$, the "differential input" to the A/D is equal to the "span" (for reference applications convenience, there is an internal gain of two to the voltage which is applied to pin 9, the $V_{REF}/2$ input), therefore the A/D will provide a digital full scale. In this way a wide range of analog input voltages can be easily accommodated.

An example of the usefulness of this feature is when operating with ratiometric transducers which do not output the complete supply voltage range. Some, for example, may output 15% of the supply voltage for a zero reading and 85% of the supply for a full scale reading. For this case, 15% of the supply should be applied to the $V_{IN(-)}$ pin and the $V_{REF}/2$ pin should be biased at one-half of the span, which is ½ (85%–15%) or 35% of the supply. This properly shifts the zero and adjusts the full scale for this application. The $V_{IN(-)}$ input can be provided by a resistive divider which is driven by the power supply voltage and the $V_{REF}/2$ pin should be driven by an op amp. This op amp can be a unity-gain voltage follower which also obtains an input voltage from a resistive divider. These can be combined as shown in *Figure 2.*

This application can allow obtaining the resolution of a greater than 8-bit A/D. For example, 9-bit performance with the 8-bit converter is possible if the span of the analog input voltage should only use one-half of the available 0V to 5V span. This would be a span of approximately 2.5V which could start anywhere over the range of 0V to $2.5V_{DC}$.

The RC network on the output of the op amp of *Figure 2* is used to isolate the transient displacement current demands of the $V_{REF}/2$ input from the op amp.

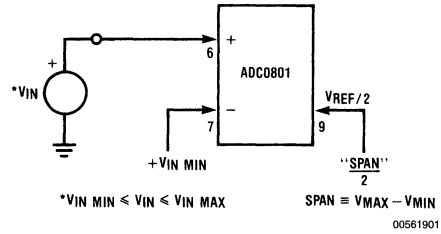


FIGURE 1. Providing Arbitrary Zero and Span Accommodation

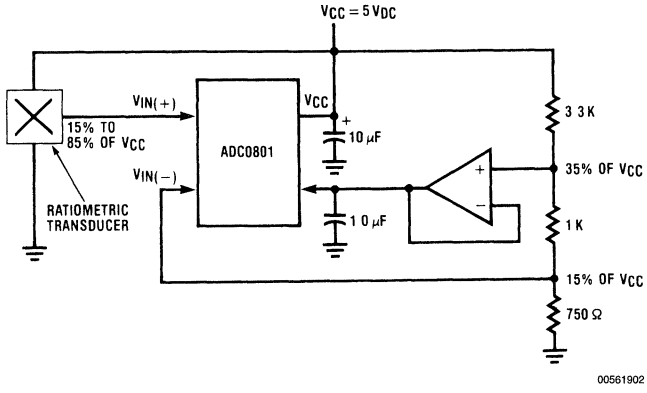


FIGURE 2. Operating with a Ratiometric Transducer which Outputs 15% to 85% of V_{CC}

Limits of $V_{REF}/2$ Voltage Magnitude

A question arises as to how small in value the span can be made. An ADC0801 part is shown in *Figure 3* where the $V_{REF}/2$ voltage is reduced in steps: from A), 2.5V (for a full scale reading of 5V); to B), 0.625V (for a full scale reading of 1.25V—this corresponds to the resolution of a 10-bit con-

Limits of $V_{REF}/2$ Voltage Magnitude

(Continued)

verter over this restricted range); to C), 0.15625V (for a full scale reading of 0.3125V—which corresponds to the resolution of a 12-bit converter). Note that at 12 bits the linearity error has increased to ½ LSB.

For these reduced reference applications the offset voltage of the A/D has to be adjusted as the voltage value of the LSB changes from 20 mV to 5 mV and finally to 1.25 mV as we go from A) to B) to C). This offset adjustment is easily combined with the setting of the $V_{IN\ MIN}$ value at the $V_{IN(-)}$ pin.

Operation with reduced $V_{REF}/2$ voltages increases the requirement for good initial tolerance of the reference voltage (or requires an adjustment) and also the allowed changes in the $V_{REF}/2$ voltage over temperature are reduced.

An interesting application of this reduced reference feature is to directly digitize the forward voltage drop of a silicon diode as a simple digital temperature sensor.

A 10-Bit Application

This analog flexibility can be used to increase the resolution of the 8-bit converter to 10 bits. The heart of the idea is shown in *Figure 4*. The two extra bits are provided by the 2-bit external DAC (resistor string) and the analog switch, SW1.

Note that the $V_{REF}/2$ pin of the converter is supplied with ⅛ V_{REF} so each of the four spans which are encoded will be:

$$2\times\frac{1}{8}V_{REF}=\frac{1}{4}V_{REF}$$

In actual implementation of this circuit, the switch would be replaced by an analog multiplexer (such as the CD4066 quad bilateral switch) and a microprocessor would be programmed to do a binary search for the two MS bits. These two bits plus the 8 LSBs provided by the A/D give the 10-bit data. For a particular application, this basic idea can be simplified to a 1-bit ladder to cover a particular range of analog input voltages with increased resolution. Further, there may exit a *priori* knowledge by the CPU which could locate the analog signal to within the 1 or 2 MSBs without requiring a search algorithm.

A Microprocessor Controlled Voltage Comparator

In applications where set points (or "pick points") are set up by analog voltages, the A/D can be used as a comparator to determine whether an analog input is greater than or less than a reference DC value. This is accomplished by simply grounding the $V_{REF}/2$ pin (to provide maximum resolution) and applying the reference DC value to the $V_{IN(-)}$ input. Now with the analog signal applied to the $V_{IN(+)}$input, an all zeros code will be output for $V_{IN(+)}$ less than the reference voltage and an all ones code for $V_{IN(+)}$ greater than the reference voltage. This reduces the computational loading of the CPU Further, using analog switches, a single A/D can encode some analog input channels in the "normal" way and can provide this comparator operation, under microprocessor control, for other analog input channels.

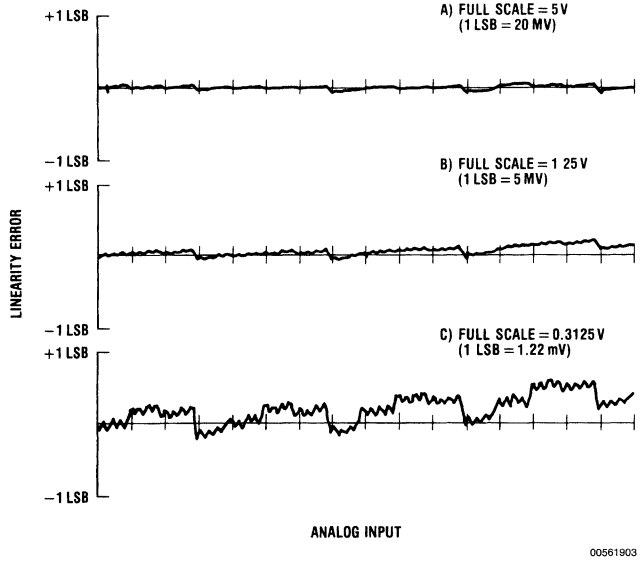


FIGURE 3. Linearity Error for Reduced Analog Input Spans

DACs Multiply and A/Ds Divide

Computation can be directly done with converter components to either increase the speed or reduce the loading on a CPU. It is rather well known that DACs multiply—and for this reason many are actually called "MDACs" to signify "multiplying DAC." An analog product voltage is provided as an output signal from a DAC for a hybrid pair of input signals—one is analog (the V_{REF} input) and the other is digital.

The A/D provides a digital quotient output for two analog input signals. The numerator or the dividend is the normal analog input voltage to the A/D and the denominator or the divisor is the V_{REF} input voltage.

High speed computation can be provided external to the CPU by either or both of these converter products. DACs are available which provide 4-quadrant multiplications (the MDACs and MICRO-DACs™), but A/Ds are usually limited to only one quadrant.

Combine Analog Self-Test with Your Digital Routines

A new innovation is the digital self-test and diagnostic routines which are being used in equipment. If an 8-bit A/D converter and an analog multiplexer are added, these testing routines can then check all power supply voltage levels and other set point values in the system. This is a major application area for the new generation converter products.

Control Temperature Coefficients with Converters

The performance of many systems can be improved if voltages within the system can be caused to change properly with changes in ambient temperature. This can be accomplished by making use of low cost 8-bit digital to analog converters (DACs) which are used to introduce a "dither" or small change about the normal operating values of DC power supplies or other voltages within the system. Now, a single measurement of the ambient temperature and one A/D converter with a MUX can be used by the microprocessor to establish proper voltage values for a given ambient temperature. This approach easily provides non-linear temperature compensation and generally reduces the cost and improves the performance of the complete system.

Save an Op Amp

In applications where an analog signal voltage which is to be converted may only range from, for example, $0V_{DC}$ to 500 mV_{DC}, an op amp with a closed-loop gain of 10 is required to allow making use of the full dynamic range ($0V_{DC}$ to $5V_{DC}$) of the A/D converter. An alternative circuit approach is shown in *Figure 5*. Here we, instead, attenuate the magnitude of the reference voltage by 10:1 and apply the 0 to 500 mV signal directly to the A/D converter. The $V_{IN(-)}$ input is now used for a V_{OS} adjust, and due to the "sampled-data" operation of the A/D there is essentially no V_{OS} drift with temperature changes.

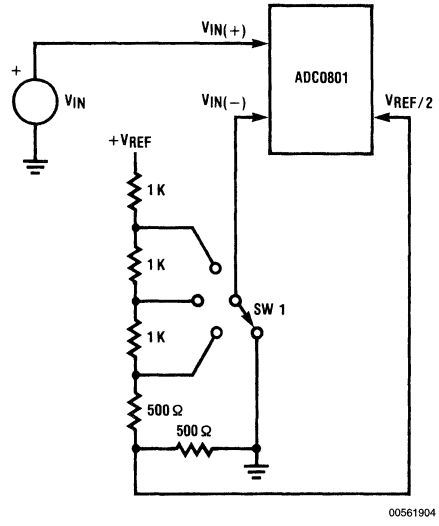


FIGURE 4. 10-Bit A/D Using the 8-Bit ADC801

Save an Op Amp (Continued)

As shown in *Figure 5*, all zeros will be output by the A/D for an input voltage (at the $V_{IN(+)}$ input) of $0V_{DC}$ and all ones will be output by the A/D for a $500mV_{DC}$ input signal. Operation of the A/D in this high sensitivity mode can be useful in many low cost system applications.

Digitizing a Current Flow

In system applications there are many requirements to monitor the current drawn by a PC card or a high current load device. This typically is done by sampling the load current flow with a small valued resistor. Unfortunately, it is usually desired that this resistor be placed in series with the V_{CC} line. The problem is to remove the large common-mode DC voltage, amplify the differential signal, and then present the ground referenced voltage to an A/D converter.

All of these functions can be handled by the A/D using the circuit shown in *Figure 6*. Here we are making use of the differential input feature and the common-mode rejection of the A/D to directly encode the voltage drop across the load current sampling resistor. An offset voltage adjustment is provided and the $V_{REF}/2$ voltage is reduced to 50 mV to accommodate the input voltage span of 100 mV. If desired, a multiplexer can be used to allow switching the $V_{IN(-)}$ input among many loads

Conclusions

At first glance it may appear that the A/D converters were mainly designed for an easy digital interface to the microprocessor. This is true, but the analog interface has also been given attention in the design and a very useful converter product has resulted from this combination of features.

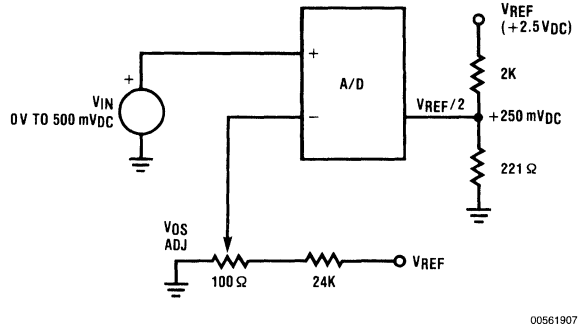


FIGURE 5. Directly Encoding a Low Level Signal

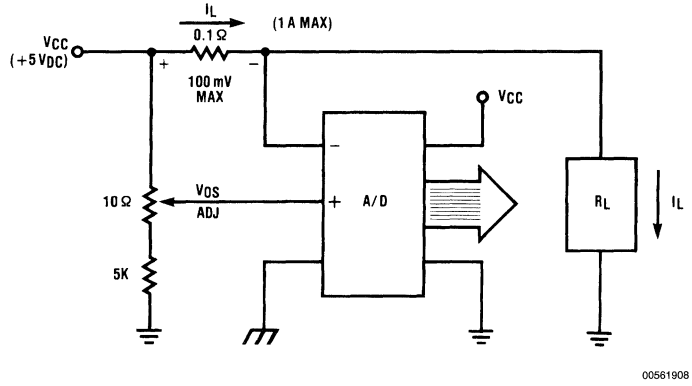


FIGURE 6. Digitizing a Current Flow

An Introduction to the Sampling Theorem

National Semiconductor
Application Note 236
Robert Pease

An Introduction to the Sampling Theorem

With rapid advancement in data acquistion technology (i.e. analog-to-digital and digital-to-analog converters) and the explosive introduction of micro-computers, selected complex linear and nonlinear functions currently implemented with analog circuitry are being alternately implemented with sample data systems.

Though more costly than their analog counterpart, these sampled data systems feature programmability. Additionally, many of the algorithms employed are a result of developments made in the area of signal processing and are in some cases capable of functions unrealizable by current analog techniques.

With increased usage a proportional demand has evolved to understand the theoretical basis required in interfacing these sampled data-systems to the analog world.

This article attempts to address the demand by presenting the concepts of aliasing and the sampling theorem in a manner, hopefully, easily understood by those making their first attempt at signal processing. Additionally discussed are some of the unobvious hardware effects that one might encounter when applying the sampled theorem.

With this. . . let us begin.

An Intuitive Development

The sampling theorem by C.E. Shannon in 1949 places restrictions on the frequency content of the time function signal, f(t), and can be simply stated as follows:

> In order to recover the signal function f(t) exactly, it is necessary to sample f(t) at a rate greater than twice its highest frequency component.

Practically speaking for example, to sample an analog signal having a maximum frequency of 2Kc requires sampling at greater than 4Kc to preserve and recover the waveform exactly.

The consequences of sampling a signal at a rate below its highest frequency component results in a phenomenon known as *aliasing*. This concept results in a frequency mistakenly taking on the identity of an entirely different frequency when recovered. In an attempt to clarify this, envision the ideal sampler of *Figure 1*(a), with a sample period of T shown in *Figure 1*(b), sampling the waveform f(t) as pictured in *Figure 1*(c). The sampled data points of f'(t) are shown in *Figure 1*(d) and can be defined as the sample set of the continuous function f(t). Note in *Figure 1*(e) that another frequency component, a'(t), can be found that has the same sample set of data points as f'(t) in *Figure 1*(d). Because of this it is difficult to determine which frequency a'(t), is truly being observed. This effect is similar to that observed in western movies when watching the spoked wheels of a rapidly moving stagecoach rotate backwards at a slow rate. The effect is a result of each individual frame of film resembling a discrete strobed sampling operation flashing at a rate slightly faster than that of the rotating wheel. Each observed sample point or frame catches the spoked wheel slightly displaced from its previous position giving the effective appearance of a wheel rotating backwards. Again, aliasing is evidenced and in this example it becomes difficult to determine which is the true rotational frequency being observed.

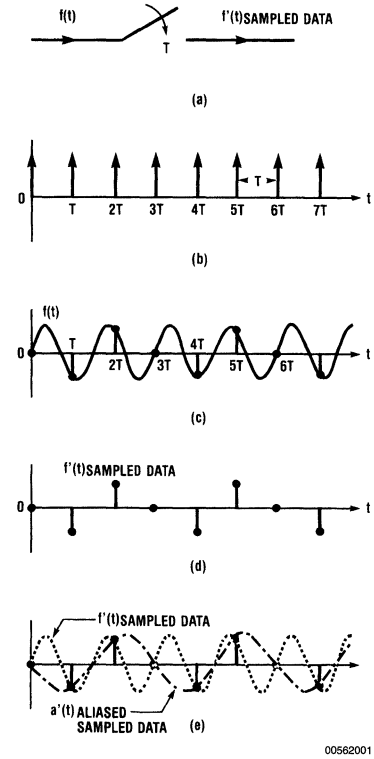


FIGURE 1. When sampling, many signals may be found to have the same set of data points. These are called aliases of each other.

An Intuitive Development (Continued)

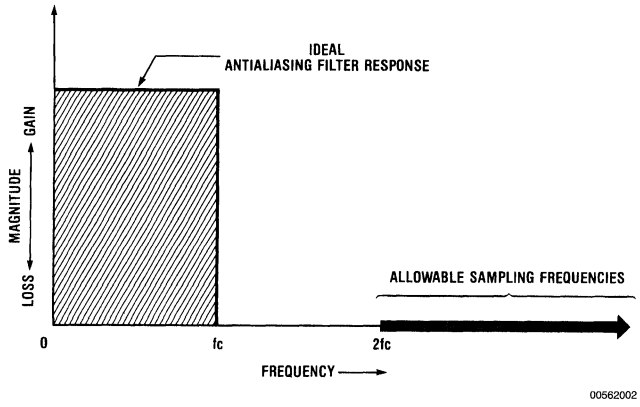


FIGURE 2. Shown in the shaded area is an ideal, low pass, anti-aliasing filter response. Signals passed through the filter are bandlimited to frequencies no greater than the cutoff frequency, fc. In accordance with the sampling theorem, to recover the bandlimited signal exactly the sampling rate must be chosen to be greater than 2fc.

On the surface it is easily said that anti-aliasing designs can be achieved by sampling at a rate greater than twice the maximum frequency found within the signal to be sampled. In the real world, however, most signals contain the entire spectrum of frequency components; from the desired to those present in white noise. To recover such information accurately the system would require an unrealizably high sample rate.

This difficulty can be easily overcome by preconditioning the input signal, the means of which would be a band-limiting or frequency filtering function performed prior to the sample data input. The prefilter, typically called anti-aliasing filter guarantees, for example in the low pass filter case, that the sampled data system receives analog signals having a spectral content no greater than those frequencies allowed by the filter. As illustrated in *Figure 2*, it thus becomes a simple matter to sample at greater than twice the maximum frequency content of a given signal.

A parallel analog of band-limiting can be made to the world of perception when considering the spectrum of white light. It can be realized that the study of violet light wavelengths generated from a white light source would be vastly simplified if initial band-limiting were performed through the use of a prism or white light filter.

The Sampling Theorem

To solidify some of the intuitive thoughts presented in the previous section, the sampling theorem will be presented applying the rigor of mathematics supported by an illustrative proof. This should hopefully leave the reader with a comfortable understanding of the sampling theorem.

Theorem: If the Fourier transform $F(\omega)$ of a signal function f(t) is zero for all frequencies above $|\omega| \geq \omega_c$, then f(t) can be uniquely determined from its sampled values

$$f_n = f(nT) \qquad (1)$$

These values are a sequence of equidistant sample points spaced $\frac{1}{2fc} = \frac{Tc}{2} = T$ apart. (f)t is thus given by

$$f(t) = \sum_{n=-\infty}^{\infty} f(nT) \frac{\sin \omega_c (t - nT)}{\omega_c (t - nT)} \qquad (2)$$

Proof: Using the inverse Fourier transform formula:

$$f(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} F(\omega) \epsilon^{j\omega t} \, d\omega \qquad (3)$$

the band limited function, f(t), takes the form, *Figure 3a*,

$$f(t) = \frac{1}{2\pi} \int_{-\omega_c}^{\omega_c} F(\omega) \epsilon^{j\omega t} \, d\omega \qquad (4)$$

$f_n = f\left(n \frac{\pi}{\omega_c}\right)$ is then given as

$$f_n = \frac{1}{2\pi} \int_{-\omega_c}^{\omega_c} F(\omega) \epsilon^{j\omega \frac{n\pi}{\omega_c}} \, d\omega \qquad (5)$$

See *Figure 3c* and *Figure 3e*.

Expressing $F(\omega)$ as a Fourier series in the interval $-\omega_c \leq \omega \leq \omega_c$ we have

$$f_n = \frac{1}{2\pi} \int_{-\omega_c}^{\omega_c} F(\omega) \epsilon^{j\omega \frac{n\pi}{\omega_c}} \, d\omega \qquad (6)$$

The Sampling Theorem (Continued)

Where,

$$C_n = \frac{1}{2\omega_c}\int_{-\omega_c}^{\omega_c} F(\omega)\epsilon^{j\omega\frac{n\pi}{\omega_c}}\,d\omega \tag{7}$$

Further manipulating *Equation (7)*

$$C_n = \frac{2\pi}{2\omega_c}\frac{1}{2\pi}\int_{-\omega_c}^{\omega_c} F(\omega)\epsilon^{j\omega\frac{n\pi}{\omega_c}}\,d\omega \tag{8}$$

C_n can be written as

$$C_n = \frac{\pi}{\omega_c} f_n \tag{9}$$

Substituting *Equation (9)* into *Equation (6)* gives the periodic Fourier Transform

$$F_P(\omega) = \sum_{n=-\infty}^{\infty} \frac{\pi}{\omega_c} f_n \epsilon^{-j\omega\frac{n\pi}{\omega_c}} \tag{10}$$

of *Figure 3f.* Using Poisson's sum formula (Note 1) $F(\omega)$ can be stated more clearly as

$$F(\omega) = \sum_{n=-\infty}^{\infty} F(\omega - 2n\omega_c) \tag{11}$$

Interestingly for the interval $-\omega_c \le \omega \le \omega_c$ the periodic function $F_p(\omega)$ and *Figure 3f.* equals $F(\omega)$ and *Figure 3b.* respectively. Analogously if $F_p(\omega)$ were multiplied by a rectangular pulse defined,

$$H(\omega) = 1 \qquad -\omega_c \le \omega \le \omega \tag{12}$$

and

$$H(\omega) = 0 \qquad |\omega| \ge \omega_C \tag{13}$$

then as pictured in *Figure 4b, d,* and *f,*

$$F(\omega) = H(\omega) \bullet F_P(\omega) = H(\omega) \sum_{n=-\infty}^{\infty} \frac{\pi}{\omega_c} f_n \epsilon^{-j\omega\frac{n\pi}{\omega_c}} \tag{14}$$

Solving for f(t) the inverse Fourier transform *Equation (3)* is applied to *Equation (14)*

$$f(t) = \frac{1}{2\pi}\int_{-\omega_c}^{\omega_c} F(\omega)\epsilon^{j\omega t}\,d\omega \tag{15}$$

$$= \frac{1}{2\pi}\int_{-\omega_c}^{\omega_c}\left[H(\omega)\sum_{n=-\infty}^{\infty}\frac{\pi}{\omega_c} f_n \epsilon^{-j\omega\frac{n\pi}{\omega c}}\right]\epsilon^{j\omega t}\,d\omega$$

$$= \sum_{n=-\infty}^{\infty} fn\frac{1}{2\omega_c}\int_{-\omega_c}^{\omega_c}\epsilon^{j\omega\left(t-\frac{n\pi}{\omega}\right)}\,d\omega$$

Note 1: Poisson's sum formula

$$\frac{1}{T}\sum_{n=-\infty}^{\infty} F(\omega - n\omega_s) = \sum_{n=-\infty}^{\infty} f(nT)\epsilon^{-j\omega nT}$$

where $T = \frac{1}{f_s}$ and f_s is the sampling frequency giving

$$f(t) = \sum_{n=-\infty}^{\infty} f_n \frac{\sin\omega_c\left(t-\frac{n\pi}{\omega_c}\right)}{\omega_c\left(t-\frac{n\pi}{\omega_c}\right)} \tag{16}$$

Equation (16) is equivalent to *Equation (2)* as is illustrated in *Figure 4e* and *Figure 3a* respectively.

As observed in *Figure 3* and *Figure 4,* each step of the sampling theorem proof was also illustrated with its Fourier transform pair. This was done to present alternate illustrative proofs.

Recalling the convolution (Note 2) theorem, the convolution of $F(\omega)$, *Figure 3b,* with a set of equidistant impulses, *Figure 3d,* yields the same periodic frequency function $F_p(\omega)$, *Figure 3f,* as did the Fourier transform of f_n, *Figure 3e,* the product of f(t), *Figure 3a,* and its equidistant sample impulses, *Figure 3c.*

In the same light the original time function f(t), *Figure 4e,* could have been recovered from its sampled waveform by convolving f_n, *Figure 4a,* with h(t), *Figure 4c,* rather than multiplying $F_p(\omega)$, *Figure 4b,* by the rectangular function $H(\omega)$, *Figure 4d,* to get $F(\omega)$, *Figure 4f,* and finally inverse transforming to achieve f(t), *Figure 4e,* as done in the mathematic proof.

Note 2: The convolution theorem allows one to mathematically convolve in the time domain by simply multiplying in the frequency domain. That is, if f(t) has the Fourier transform $F(\omega)$, and x(t) has the Fourier transform $X(\omega)$, then the convolution f(t)*x(t) has the Fourier transform $F(\omega)\bullet X(\omega)$

$f(t) * x(t) \leftrightarrow F(\omega) \bullet X(\omega)$

$f(t) \bullet x(t) \leftrightarrow F(\omega) * X(\omega)$

The Sampling Theorem (Continued)

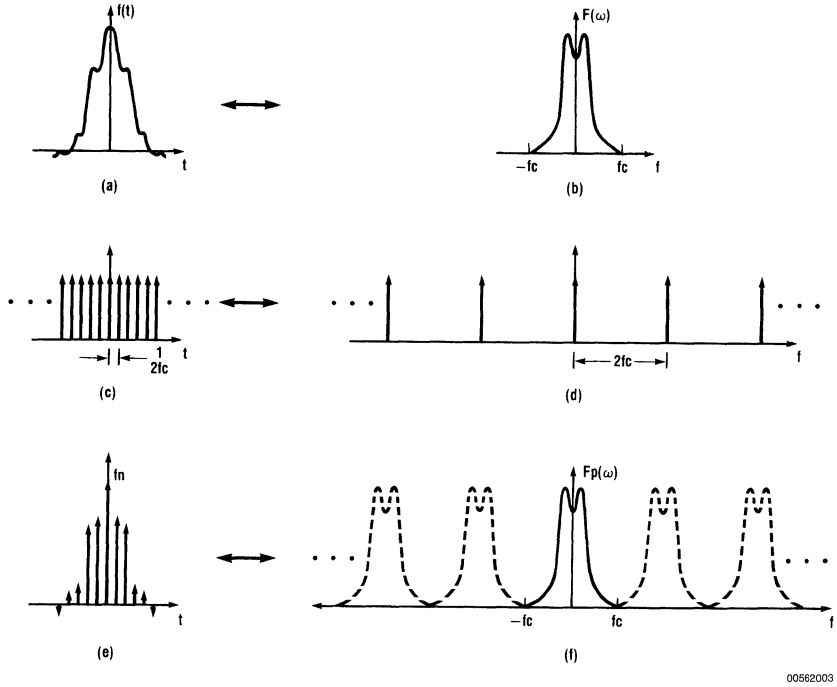


FIGURE 3. Fourier transform of a sampled signal.

The Sampling Theorem (Continued)

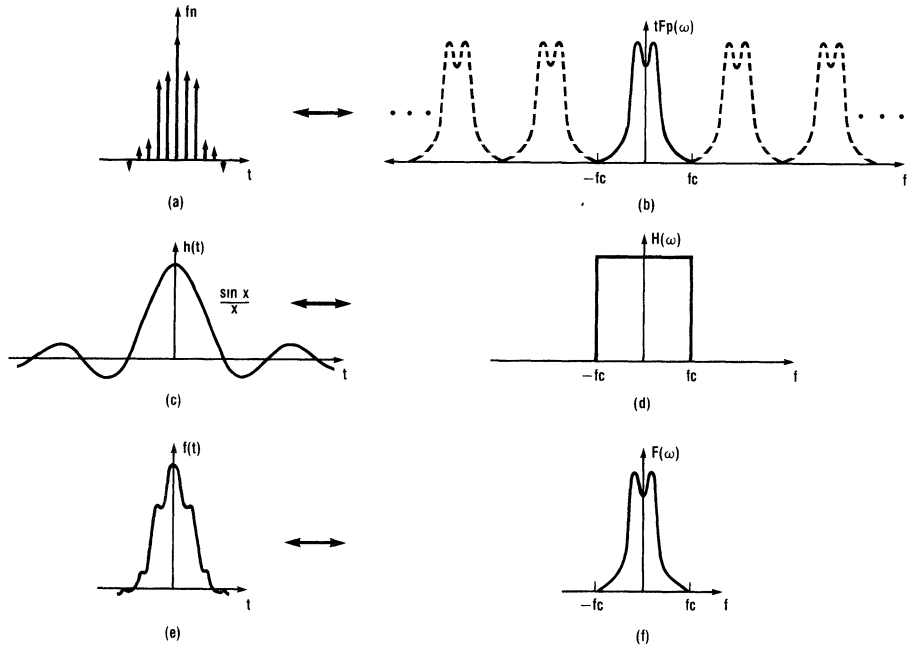


FIGURE 4. Recovery of a signal f(t) from sampled data information.

Some Observations and Definitions

If *Figure 3f* or *Figure 4b* are re-examined it can be noted that the original spectrum $F_p(\omega)$, $|\omega| \leq \omega_c$, and its images $F_p(\omega)$, $|\omega| \geq \omega_c$, are non-overlapping. On the other hand *Figure 5* illustrates spectral folding, overlapping or aliasing of the spectrum images into the original signal spectrum. This aliasing effect is, in fact, a result of undersampling and further causes the information of the original signal to be indistinguishable from its images (i.e. *Figure 1e*). From *Figure 6* one can readily see that the signal is thus considered non-recoverable.

The frequency |fc| of *Figure 3f* and *Figure 4b* is exactly one half the sampling frequency, fc=fs/2, and is defined as the Nyquist frequency (after Harry Nyquist of Bell Laboratories). It is also often called the aliasing frequency or folding frequency for the reasons discussed above. From this we can say that in order to prevent aliasing in a sampled-data system the sampling frequency should be chosen to be greater than twice the highest frequency component f_c of the signal being sampled.

By definition

$$f_s \geq 2f_c \qquad (17)$$

Note, however, that no mention has been made to sample at precisely the Nyquist rate since in actual practice it is impossible to sample at $f_s = 2f_c$ unless one can guarantee there are absolutely no signal components above f_c. This can only be achieved by filtering the signal prior to sampling with a filter having infinite rolloff... a physical impossibility, see *Figure 2*.

Some Observations and Definitions (Continued)

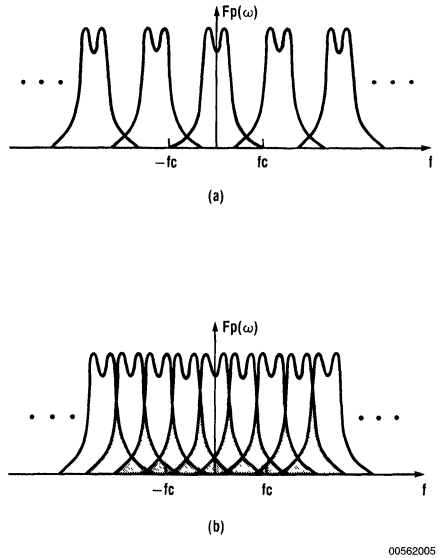


FIGURE 5. Spectral folding or aliasing caused by:
(a) under sampling
(b) exaggerated under sampling.

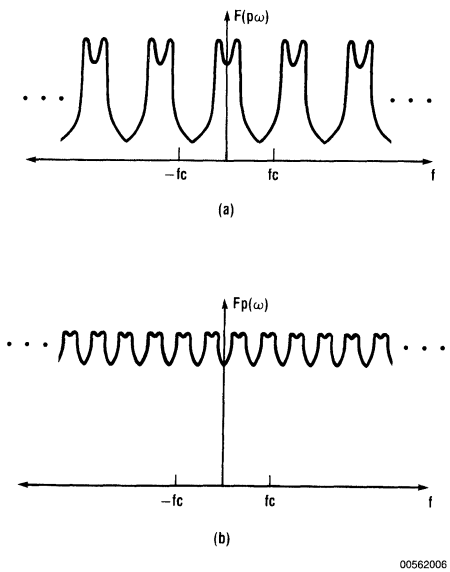


FIGURE 6. Aliased spectral envelope (a) and (b) of *Figure 5a* and *Figure 5b* respectively.

Some Observations and Definitions (Continued)

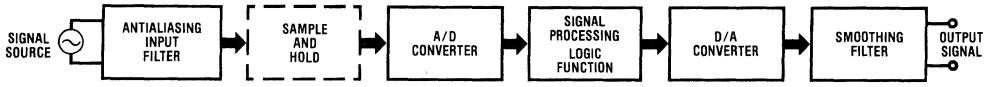


FIGURE 7. Generalized single channel sample data system.

The Sampling Theorem and Its Hardware

IMPLICATIONS

Though there are numerous sophisticated techniques of implementation, it is appropriate to re-emphasize that the intent of this article is to give the first time user a basic and fundamental approach toward the design of a sampled-data system. The method with which to achieve this goal will be to introduce a few of the common perils encountered when implementing such a system. We begin by considering the generalized block diagram of *Figure 7.*

As shown in *Figure 7*, prior to any signal processing manipulation the analog input signal must be preconditioned to prevent aliasing and thereafter digitized to logic signals usable by the logic function block. The antialiasing and digitizing functions are performed by an input filter and analog-to-digital converter respectively. Once digitized the signal can then be altered or processed and upon completion, reconstructed back to a continuous analog signal via a digital-to-analog converter followed by a smoothing filter.

To this point no mention has been made concerning the sample and hold circuit block depicted in *Figure 7.* In general the analog-to-digital converter can operate as a stand alone unit. In many high speed operations however, the converter speed is insufficient and thus requires the assistance of a sample and hold circuit. This will be discussed in detail further in the article.

The Antialiasing Input Filter

As indicated earlier in the text, the antialiasing filter should band-limit the input signal's spectrum to frequencies no greater than the Nyquist frequency. In the real world however, filters are non-ideal and have typical attenuation or band-limiting and phase characteristics as shown in *Figure 8* (Note 3). It must also be realized that true band-limiting of a specific frequency spectrum is not possible. In the sample data system band-limiting is achieved by attenuating those frequencies greater than the Nyquist frequency to a level undetectable or invisible to the system analog-to-digital (A/D) converter. This level would typically be less than the rms quantization (Note 4) noise level defined by the specific converter being used.

Note 3: In order not to disrupt the flow of the discussion a list of filter terms has been presented in Appendix A

Note 4: For an explanation of quantization refer to section IV B of this article

As an example of how an antialiasing filter would be applied, assume a sample data system having within it an 8-bit A/D converter. Eight bits translates to $2^n=2^8=256$ levels of resolution. If a 2.56 volt reference were used each quantization level, q, would represent the equivalent of 2.56 volts/256=10 millivolts. Realizing this the antialiasing filter would be designed such that frequencies in the stopband were attenuated to less than the rms quantization noise level of $q/2\sqrt{3}$ and thus appearing invisible to the system. More specifically

$$-20 \log_{10} \frac{V \text{ full scale}}{V_{q/2\sqrt{3}}} \cong -59 \text{ dB} = A_{MIN}$$

It can be seen, for example in the Butterworth filter case (characterized as having a maximally flat pass-band) of *Figure 9a* that any order of filter may be used to achieve the −59 dB attenuation level, however, the higher the order, the faster the roll off rate and the closer the filter magnitude response will approach the ideal.

Referring back to *Figure 8* it is observed that those frequencies greater than ω_a are not recognized by the A/D converter and thus the sampling frequency of the sample data system would be defined as $\omega_s \geq 2\omega_a$. Additionally, the frequencies present within the filtered input signal would be those less than ω_a. Note however, that the portion of the signal frequencies least distorted are those between ω=O and ω_p and those within the transition band are distorted to a substantial degree, though it was originally desired to limit the signal to frequencies less than the cutoff ω_p, because of the non-ideal frequency response the true Nyquist frequency occurred at ω_a. We see then that the sampled-data system could at most be accurate for those frequencies within the antialiasing filter passband.

From the above example, the design of an antialiasing filter appears to be quite straight forward. Recall however, that all waveforms are composed of the sums and differences of various frequency components and as a result, if the response of the filter passband were not flat for the desired signal frequency spectrum, the recovered signal would be an inaccurate summation of all frequency components altered by their relative attenuations in the pass-band.

Additionally the antialiasing filter design should not neglect the effects of delay. As illustrated in *Figure 8* and *Figure 9b*, delay time corresponds to a specific phase shift at a particular frequency. Similar to the flat pass-band consideration, if the phase shift of the filter is not exactly proportional to the frequency, the output of the filter will be a waveform in which the summation of all frequency components has been altered by shifts in their relative phase. *Figure 9b* further indicates that contrary to the roll off rate, the higher the filter order the more non-ideal the delay becomes (increased delay) and the result is a distorted output signal.

A final and complex consideration to understand is the effects of sampling. When a signal is sampled the end effect is the multiplication of the signal by a unit sampling pulse train as recalled from *Figure 3a, c* and *e.* The resultant waveform has a spectrum that is the convolution of the signal spectrum and the spectrum of the unit sample pulse train, i.e. *Figure 3b, d,* and *f.* If the unit sample pulse has the classical sin X/X

The Sampling Theorem and Its Hardware (Continued)

spectrum (Note 5) of a rectangular pulse, see *Figure 13*, then the convolution of the pulse spectrum with the signal spectrum would produce the non-ideal sampled signal spectrum shown in *Figure 10a*, *b*, and *c*.

It should be realized that because of the band-limiting or filtering and delay response of the Sin X/X function combined with the effects of the non-ideal antialiasing filter (i e non-flat pass-band and phase shift) certain of the sum and difference frequency components may fall within the desired signal spectrum thereby creating aliasing errors, *Figure 10c*.

When designing antialiasing filters it will be found that the closer the filter response approaches the ideal the more complex the filter becomes. Along with this an increase in delay and pass-band ripple combine to distort and alias the input signal. In the final analysis the design will involve trade offs made between filter complexity, sampling speed and thus system bandwidth.

Note 5: This will be explained more clearly in Section IV of this article

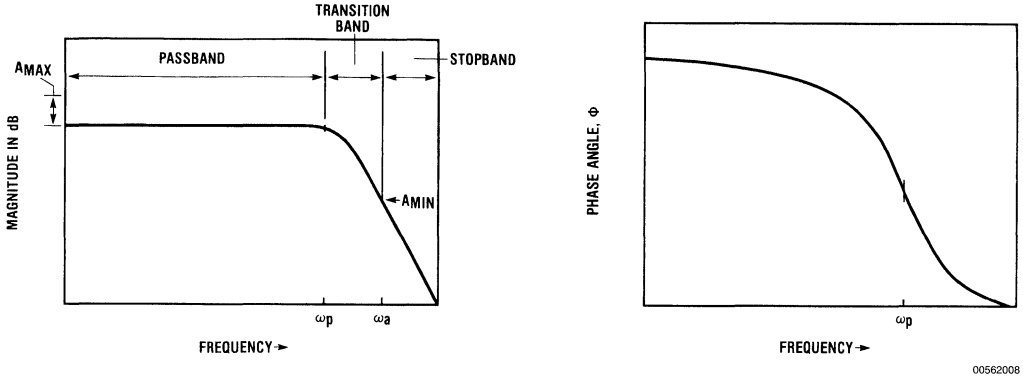
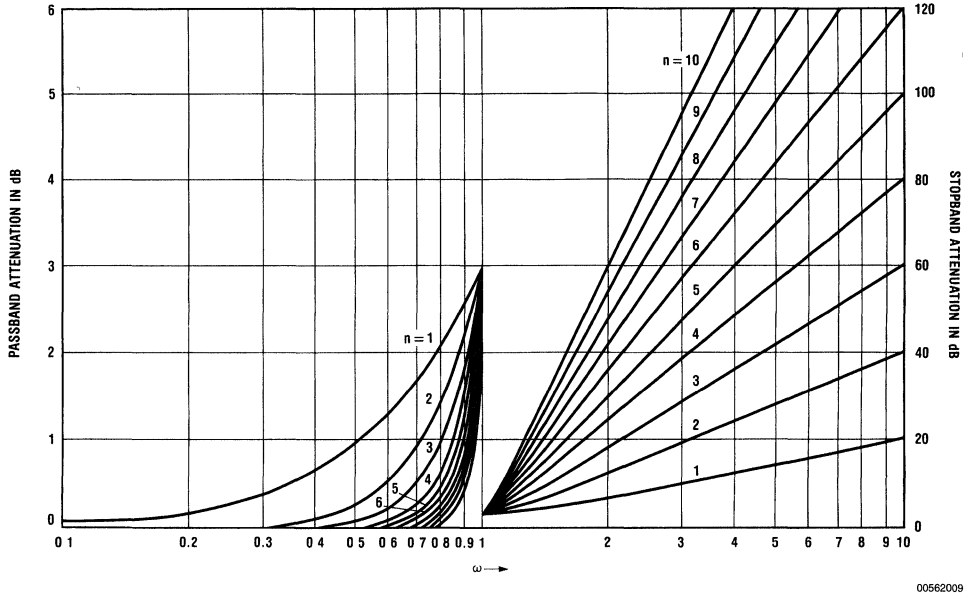


FIGURE 8. Typical filter magnitude and phase versus frequency response.

The Sampling Theorem and Its Hardware (Continued)



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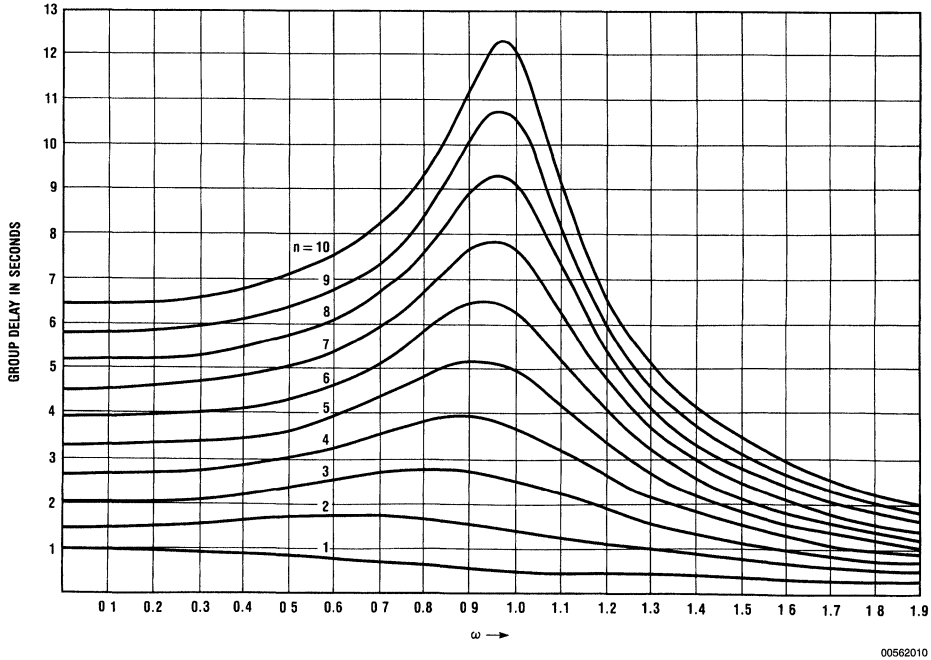
a) Attenuation characteristics of a normalized Butterworth filter as a function of degree n.



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b) Group delay performances of normalized Butterworth lowpass filters as a function of degree n.

FIGURE 9.

The Sampling Theorem and Its Hardware (Continued)

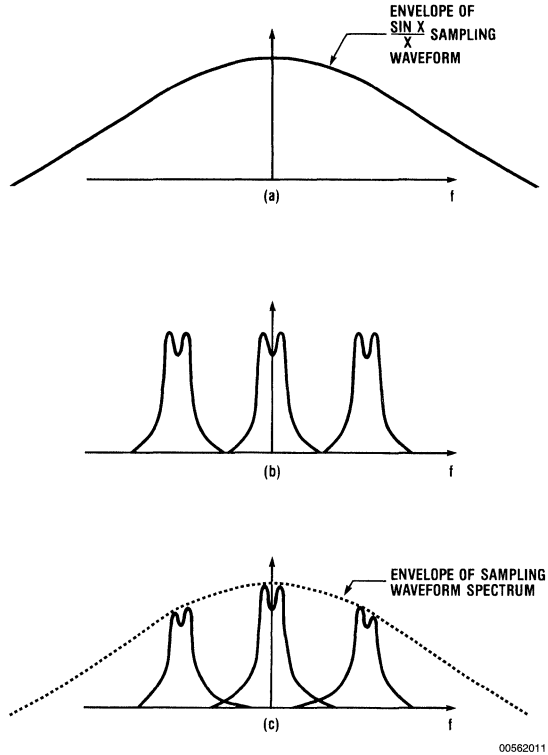


FIGURE 10. (c) equals the convolution of (a) with (b).

The Analog-to-Digital Converter

Following the antialiasing filter is the A/D converter which performs the operations of quantizing and coding the input signal in some finite amount of time. *Figure 11* shows the quantization process of converting a continuous analog input signal into a set of discrete output levels. A quantization, q, is thus defined as the smallest step used in the digital

representation of $f_q(n)$ where f(n) is the sample set of an input signal f(t) and is expressed by a finite number of bits giving the sequence $f_q(n)$. Digitally speaking q is the value of the least significant code bit. The difference signal $\epsilon(n)$ shown in *Figure 11* is called quantization noise or error and can be defined as $\epsilon(n) = f(n) - f_q(n)$. This error is an irreducible one and is a function of the quantizing process. Its error amplitude is dependent on the number of quantization levels or quantizer resolution and as shown, the maximum quantization error is |q/2|.

Generally $\epsilon(n)$ is treated as a random error when described in terms of its probability density function, that is, all values of $\epsilon(n)$ between q/2 and −q/2 are equally probable, then for the average value $\epsilon(n)_{avg}=0$ and for the rms value $\epsilon(n)_{rms} = q/2\sqrt{3}$.

As a side note it is appropriate at this point to emphasize that all analog signals have some form of noise corruption. If for example an input signal has a finite signal-to-noise ratio of 40dB it would be superfluous to select an A/D converter with a high number of bits. It may be realized that the use of a large number of bits does not give the digitized signal a higher signal-to-noise ratio than that of the original analog input signal. As a supportive argument one may say that though the quantization steps q are very small with respect to the peak input signal the lower order bits of the A/D converter merely provide a more accurate representation of the noise inherent in the analog input signal.

Returning to our discussion, we define the conversion time as the time taken by the A/D converter to convert the analog input signal to its equivalent quantization or digital code. The conversion speed required in any particular application depends upon the time variation of the signal to be converted and the amount of resolution or bits, n, required. Though the antialiasing filter helps to control the input signal time rate of change by band-limiting its frequency spectrum, a finite amount of time is still required to make a measurement or conversion. This time is generally called the aperture time and as illustrated in *Figure 12* produces amplitude measurement uncertainty errors. The maximum rate of change detectable by an A/D converter can simply be stated as

$$\left.\frac{dv}{dt}\right|_{\substack{\text{maximum resolvable}\\ \text{rate of change}}} = \frac{\text{V full scale}}{2^n T_{\text{conversion time}}} \qquad (18)$$

The Sampling Theorem and Its Hardware (Continued)

If for example V full scale = 10.24 volts, T conversion time = 10 ms, and n = 10 or 1024 bits of resolution then the maximum rate of change resolvable by the A/D converter would be 1 volt/sec. If the input signal has a faster rate of change than 1 volt/sec, 1 LSB changes cannot be resolved within the sampling period.

In many instances a sample-and-hold circuit may be used to reduce the amplitude uncertainty error by measuring the input signal with a smaller aperture time than the conversion time aperture of the A/D converter. In this case the maximum rate of change resolvable by the sample-and-hold would be

$$\left.\frac{dv}{dt}\right|_{\substack{\text{maximum resolvable}\\ \text{rate of change}}} = \frac{V \text{ full scale}}{t \text{ aperture}} \tag{19}$$

Note also that the actual calculated rate of change may be limited by the slew rate specification fo the sample-and-hold in the track mode. Additionally it is very important to clarify that this does not imply violating the sampling theorem in lieu of the increased ability to more accurately sample signals having a fast time rate of change.

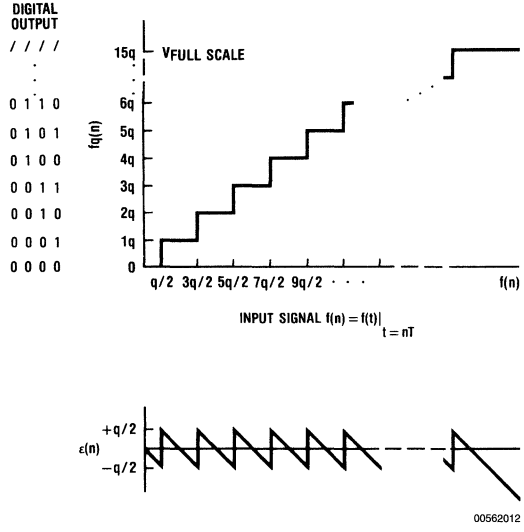
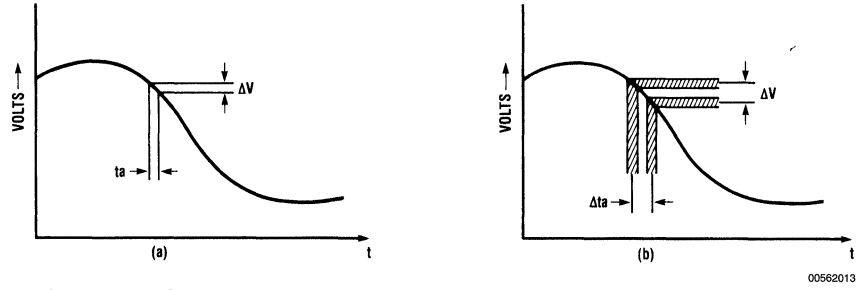


FIGURE 11. Quantization error.



ΔV AMPLITUDE UNCERTAINTY ERROR
ta APERTURE TIME
Δta APERTURE TIME UNCERTAINTY

FIGURE 12. Amplitude uncertainty as a function of (a) a nonvarying aperture and(b) aperture time uncertainty.

The Sampling Theorem and Its Hardware (Continued)

An ideal sample-and-hold effectively takes a sample in zero time and with perfect accuracy holds the value of the sample indefinitely. This type of sampler is also known as a zero order hold circuit and its effect on a sample data system warrants some discussion

It is appropriate to recall the earlier discussion that the spectrum of a sampled signal is one in which the resultant spectrum is the product obtain by convolving the input signal spectrum with the sin X/X spectrum of the sampling waveform. *Figure 13* illustrates the frequency spectrum plotted from the Fourier transform

$$F(\omega) = AT \frac{\sin \frac{\omega T}{2}}{\frac{\omega T}{2}} \tag{20}$$

of a rectangular pulse. The sin X/X form occurs frequently in modern communication theory and is commonly called the sampling function

The magnitude and phase of a typical zero order hold sampler spectrum

$$H(\omega) = A\left[\tau \frac{\sin \omega\tau}{\omega\tau} + j\frac{1}{\omega}(\cos \omega - 1)\right] \tag{21}$$

is shown in *Figure 14* and *Figure 15* illustrates the spectra of various sampler pulse-widths. The purpose of presenting this illustrative information is to give insight at to what effects cause the aliasing described in *Figure 10.* From *Figure 15* it is realized that the main lobe of the sin X/X function varies inversely proportional with the sampler pulse-width. In other words a wide pulse-width, or in this case the aperture window, acts as a low pass filtering function and limits the amount of information resolvable by the sample data system. On the other hand a narrow sampler pulse-width or aperture window has a broader main lobe or band-width and thus when convolved with the analog input signal produces the least amount of distortion. Understandably then the effect of the sampler's spectral phase and main lobe width must be considered when developing a sampling system so that no unexpected aliasing occurs from its convolution with the input signal spectrum

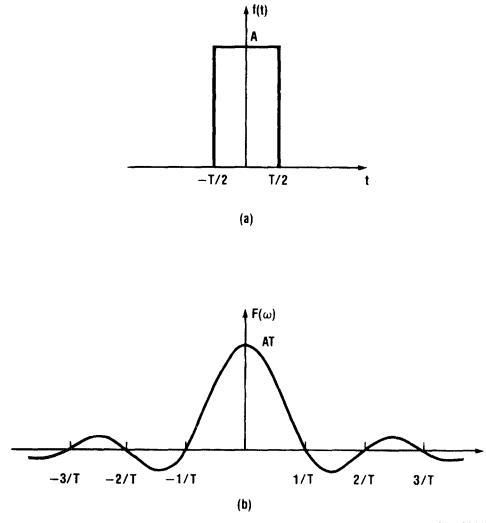


FIGURE 13. The Fourier transform of the rectangular pulse (a) is shown in (b).

The Sampling Theorem and Its Hardware (Continued)

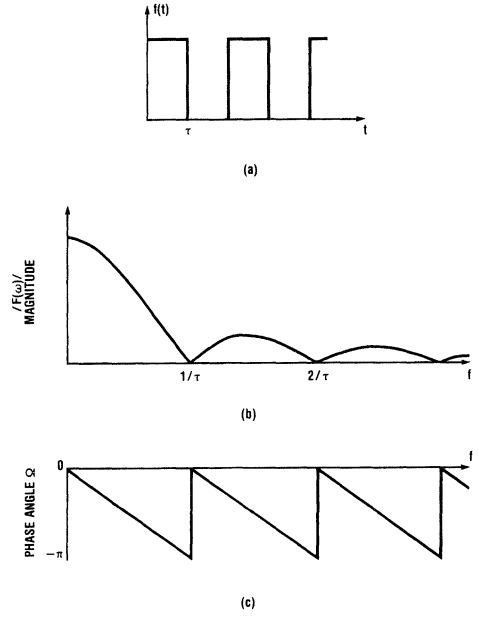


FIGURE 14. Sampling Pulse (a), its Magnitude (b) and Phase Response (c).

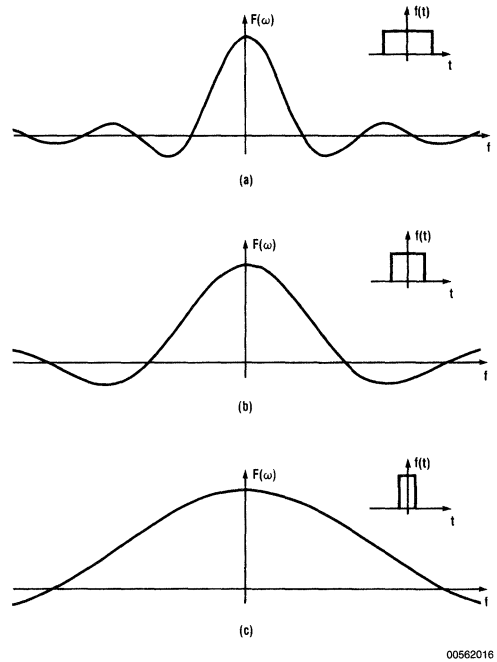


FIGURE 15. Pulse width and how it effects the sin X/X envelop spectrum (normalized amplitudes).

The Sampling Theorem and Its Hardware (Continued)

The Digital-to-Analog Converter and Smoothing Filter

After a signal has been digitally conditioned by the signal processing unit of *Figure 7*, a D/A converter is used to convert the sampled binary information back in to an analog signal. The conversion is called a zero order hold type where each output sample level is a function of its binary weight value and is held until the next sample arrives, see *Figure 16*. As a result of the D/A converter step function response it is apparent that a large amount of undesirable high frequency energy is present. To eliminate this the D/A converter is usually followed by a smoothing filter, having a cutoff frequency no greater than half the sampling frequency. As its name suggests the filter output produces a smoothed version of the D/A converter output which in fact is a convolved function. More simply said, the spectrum of the resulting signal is the product of a step function sin X/X spectrum and the band-limited analog filter spectrum. Analogous to the input sampling problem, the smoothed output may have aliasing effects resulting from the phase and attenuation relations of the signal recovery system (defined as the D/A converter and smoothing filter combination).

As a final note, the attenuation due to the D/A converter sin X/X spectrum shape may in some cases be compensated for in the signal processing unit by pre-processing using a digital filter with an inverse response X/sin X prior to D/A conversion. This allows an overall flat magnitude signal response to be smoothed by the final filter.

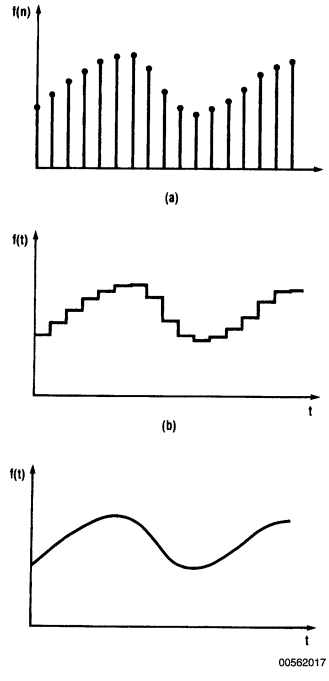


FIGURE 16. (a) Processed signal data points (b) output of D/A converter (c) output of smoothing filter.

A Final Note

This article began by presenting an intuitive development of the sampling theorem supported by a mathematical and illustrative proof. Following the theoretical development were a few of the unobvious and troublesome results that develop when trying to put the sampling theorem into practice. The purpose of presenting these thought provoking perils was to perhaps give the beginning designer some insight or guidelines for consideration when developing a sample data system's interface.

Acknowledgements

The author wishes to thank James Moyer and Barry Siegel for their encouragement and the time they allocated for the writing of this article.

Appendix A

BASIC FILTER CONCEPTS

A filter is a network used for separating signal waves on the basis of their frequency and is usually composed of passive, reactive and active elements such as resistors, capacitors, inductors, and amplifiers, or combinations thereof.

There are basically five types of filters used to pass or reject such signals and they are defined as follows:

1. A low-pass filter passes a band of frequencies called the *passband*, ranging from zero frequency or DC to a certain *cutoff frequency*, ω_c (Note 6), and in addition has a maximum attenuation or ripple level of A_{MAX} within the passband. See *Figure 17*.

   Frequencies beyond the ω_c may have an attenuation greater than A_{MAX} but beyond a specific frequency ω_s defined as the *stopband frequency*, a minimum attenuation of A_{MIN} must prevail. The band of frequencies higher than ω_s and maintaining attenuation greater than or equal to A_{MIN} is called the *stopband*. The transition region or *transition band* is that band of frequencies between ω_c and ω_s.

Note 6: Recall that the radian frequency $\omega=2\pi f$

Appendix A (Continued)

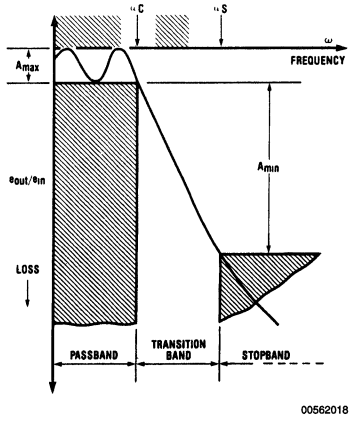


FIGURE 17. Common Low Pass Filter Response

A high-pass filter allows frequencies above the passband frequency, ω_c, to pass and rejects frequencies below this point. A_{MAX} must be maintained in the passband and frequencies equal to and below the stopband frequency, ω_s, must have a minimum attenuation of A_{MIN}. See *Figure 18*.

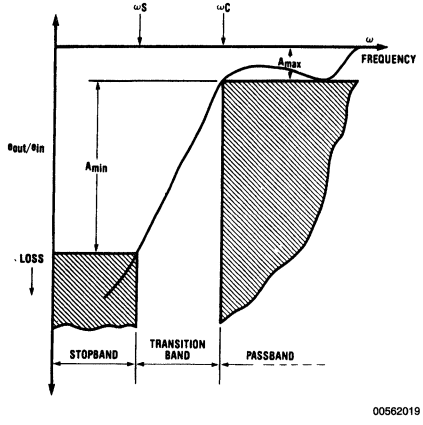


FIGURE 18. Common High Pass Filter Response

A bandpass filter performs the function of passing a specific band of frequencies while rejecting those frequencies above and below ω_{c2} and lower, ω_{c1} cutoff frequency limits. See *Figure 19*.

As in the previous two cases the passband is required to sustain an attenuation of A_{MAX}, and the stopband of frequencies above and below ω_{s2} and ω_{s2} respectively, must have a minimum attenuation of A_{MIN}.

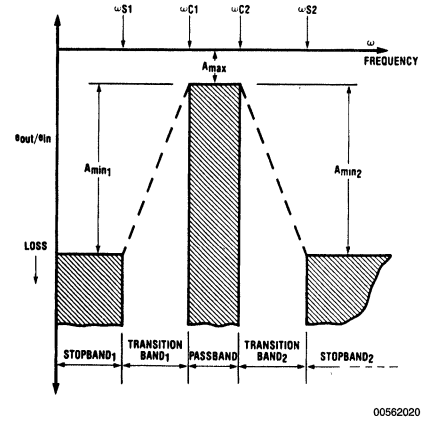


FIGURE 19. Common Band-pass Filter Response

A band-reject filter or notch filter allows all but a specific band of frequencies to pass. As shown in *Figure 4*, those frequencies between ω_{s1} and ω_{s2} are filtered out and those frequencies above and below ω_{c2} and ω_{c1} respectively are passed. The attenuation requirements of the stopband A_{MIN} and passband A_{MAX} must still hold.

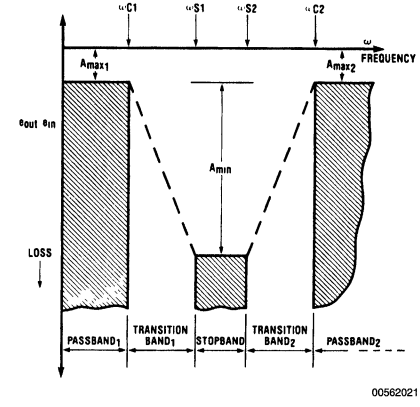


FIGURE 20. Common Band-Reject Filter Response

An all-pass or phase shift filter allows all frequencies to pass without any appreciable attenuation. It further introduces a predictable phase shift to all frequencies passed, though not

Appendix A (Continued)

restricting the entire range of frequencies to a specific phase shift (i.e., a phase shift may be imposed upon a selected band of frequencies and appear invisible to all others).

Appendix B

ARTICLE REFERENCES

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Wide-Range Current-to-Frequency Converters

National Semiconductor
Application Note 240
Robert A. Pease

Does an analog-to-digital converter cost you a lot if you need many bits of accuracy and dynamic range? Absolute accuracy better than 0.1% is likely to be expensive. But a capability for wide dynamic range can be quite inexpensive. Voltage-to-frequency (V-to-F) converters are becoming popular as a low-cost form of A-to-D conversion because they can handle a wide dynamic range of signals with good accuracy.

Most voltage-to-frequency (V-to-F) converters actually operate with an input current which is proportional to the voltage input:

$$I_{IN} = \frac{V_{IN}}{R_{IN}}$$

(*Figure 1*). This current is integrated by an op amp, and a charge dispenser acts as the feedback path, to balance out the average input current. When an amount of charge Q=I•T (or Q=C•V) per cycle is dispensed by the circuit, then the frequency will be:

$$f = \left(\frac{V_{IN} - V_{OS}}{R_{IN}} + I_b\right) \times \frac{1}{Q}.$$

When V_{IN} is large:

$$f \cong \frac{V_{IN}}{R_{IN}} \times \frac{1}{Q}.$$

When V_{IN} covers a wide dynamic range, the V_{OS} and I_b of the op amp must be considered, as they greatly affect the usable accuracy when the input signal is very small. For example, when the full-scale input is 10V, a signal which is 100 dB below full-scale will be only 100 µV. If the op amp has an offset drift of ± 100 µV, (whether caused by time or temperature), that would cause a ±100% error at this signal level. However, a current-to-frequency converter can easily cover a 120 dB range because the voltage offset problem is not significant when the input signal is actually a current source. Let's study the architecture and design of a current-to-frequency converter, to see where we can take advantage of this.

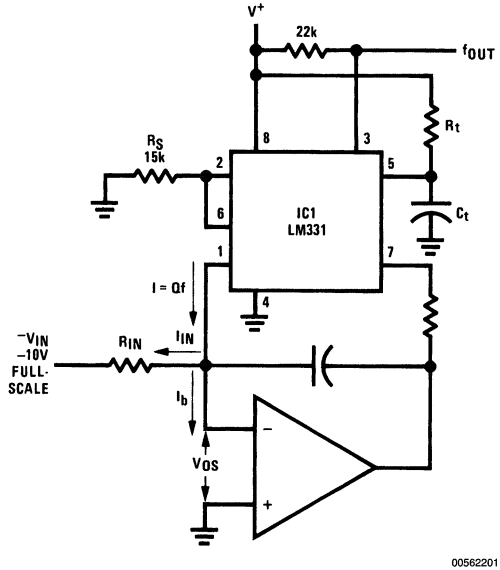


FIGURE 1. Typical Voltage-to-Frequency Converter

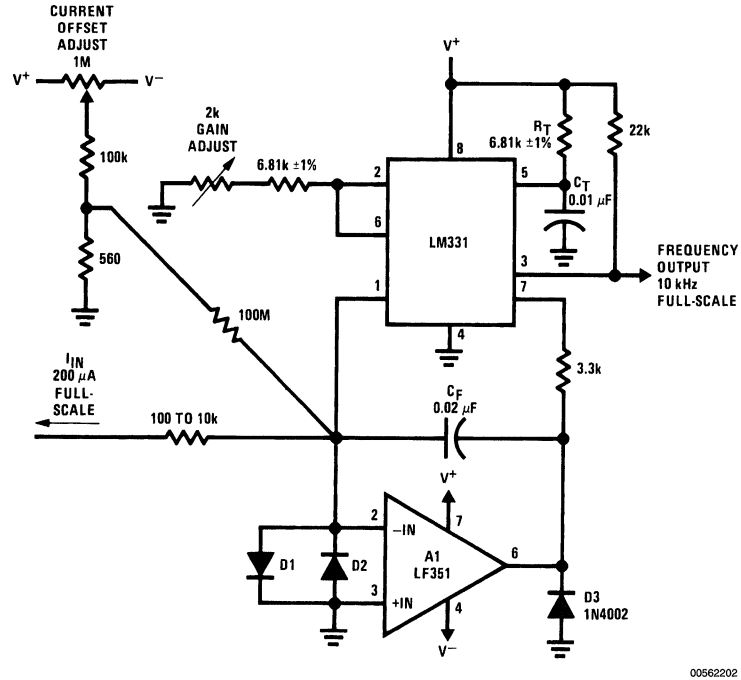
When the input signal is a current, the use of a low-voltage-drift op amp becomes of no advantage, and low bias current is the prime specification. A low-cost BI-FET™ op amp such as the LF351A has I_b <100 pA, and temperature coefficient of I_b less than 10 pA/°C, at room temperature. In a typical circuit such as *Figure 2*, the leakage of the charge dispenser is important, too. The LM331 is only specified at 10 nA max at room temperature, because that is the

smallest current which can be measured economically on high-speed test equipment. The leakage of the LM331's current-source output at pin 1 is usually 2 pA to 4 pA, and is always less than the 100 pA mentioned above, at 25°C.

The feedback capacitor C_F should be of a low-leakage type, such as polypropylene or polystyrene. (At any temperature above 35°C, mylar's leakage may be excessive.) Also, low-leakage diodes are recommended to protect the circuit's input from any possible fault conditions at the input. (A 1N914 may leak 100 pA even with only 1 millivolt across it, and is unsuitable.)

After trimming this circuit for a low offset when I_{IN} is 1 nA, the circuit will operate with an input range of 120 dB, from 200 µA to 100 pA, and an accuracy or linearity error well below (0.02% of the signal plus 0.0001% of full-scale).

The zero-offset drift will be below 5 or 10 pA/°C, so when the input is 100 dB down from full-scale, the zero drift will be less than 2% of signal, for a ±5°C temperature range. Another way of indicating this performance is to realize that when the input is 1/1000 of full-scale, zero drift will be less than 1% of that small signal, for a 0°C to 70°C temperature range.



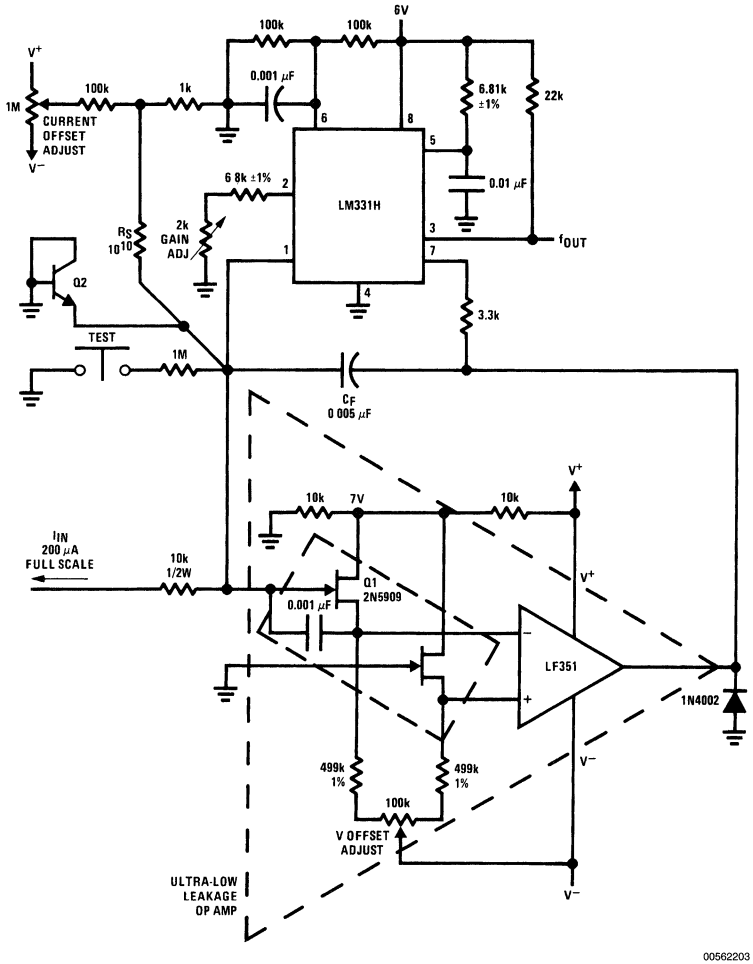
D1, D2=1N457, 1N484, or similar low-leakage planar diode

FIGURE 2. Practical Wide-Range Current-to-Frequency Converter

What if this isn't good enough? You *could* get a better op amp. For example, an LH0022C has 10 pA max I_b. But it is silly to pay for such a good op amp, with low V offset errors, when only a low input current specification is needed. The circuit of *Figure 3* shows the simple scheme of using FET followers ahead of a conventional op amp. An LF351 type is suitable because it is a cheap, quick amplifier, well suited for this work. The 2N5909s have a maximum I_b of 1.0 pA, and at room temperature it will drift only 0.1 pA/°C. Typical drift is 0.02 pA/°C.

The voltage offset adjust pot is used to bring the summing point within a millivolt of ground. With an input signal big enough to cause f_{OUT}=1 second per cycle, trim the V offset adjust pot so that closing the *test* switch makes no effect on the output frequency (or, output period). Then adjust the input current offset pot, to get f_{OUT}=1/1000 of full-scale when I_{IN} is 1/1000 of full-scale. When I_{IN} covers the 140 dB range, from 200 µA to 20 pA, the output will be stable, with very good zero offset stability, for a limited temperature range around room temperature. Note these precautions and special procedures:

1. Run the LM331 on 5V to 6V to keep leakage down and to cut the dissipation and temperature rise, too.
2. Run the FETs with a 6V drain supply.
3. Guard all summing point wiring away from all other voltages.



Q1 - 2N5909 or similar
1G<1 pA
Q2 - 2N930 or 2N3565

FIGURE 3. Very-Wide-Range Current-to-Frequency Converter

An alternate approach, shown in *Figure 4*, uses an LM11C as the input pre-amplifier. The LM11C has much better voltage drift than any of the other amplifiers shown here (normally less than 2 µV/°C) and excellent current drift, less than 1 pA/°C by itself, and typically 0.2 pA/°C when trimmed with the 2N3904 bias current compensation circuit as shown. Of course, the LM331's leakage of 1 pA/°C will still double every 10°C, so that having an amplifier with excellent I_b characteristics does not solve the whole problem, when trying to get good accuracy with a 100 pA signal. For that job, even the leakage of the LM331 must be guarded out!

What if even lower ranges of input current must be accepted? While it might be possible to use a current-to-voltage converter ahead of a V-to-F converter, offset voltage drifts would hurt dynamic range badly. Response and zero-drift of such an I-V will be disappointing. Also, it is not feasible to starve the LM331 to an arbitrary extent.

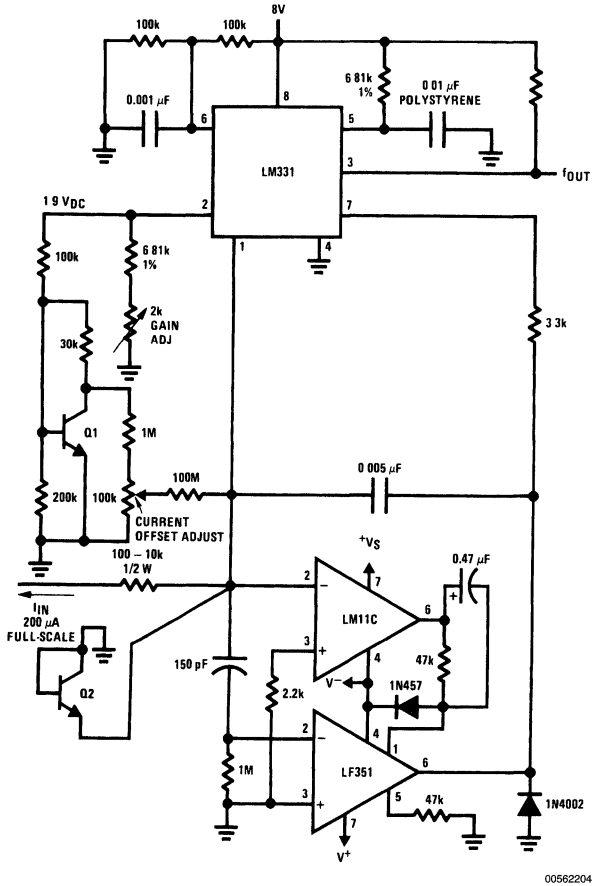
For example, while its I_{OUT} (full-scale) of 280 µA DC can be cut to 10 µA or 28 µA, it cannot be cut to 1 µA or 2.8 µA with good accuracy at 10 kHz, because the internal switches in the integrated circuit will not operate with best speed and precision at such low currents.

Instead, the output current from pin 1 of the LM331 can be fed through a current attenuator circuit, as shown in *Figure 5*. The LM334 (temperature-to-current converter IC) causes −120 mV bias to appear at the base of Q2. When a current flows out of pin 1 of the LM331, 1/100 of the current will flow out of Q1's collector, and the rest will go out of Q2's collector.

As the LM334's current is linearly proportional to Kelvin temperature, the −120 mV at Q2's base will change linearly with temperature so that the Q1/Q2 current divider stays at 1:100, invariant of temperature, according to the equation:

$$i_1/i_2 = e^{\frac{q(Vb1 - Vb2)}{kT}}$$

This current attenuator will work stably and accurately, even at high speeds, such as for 4 µS current pulses. Thus, the output of Q1 is a charge pump which puts out only 10 picocoulombs per pulse, with surprisingly good accuracy. Note also that the LM331's leakage is substantially attenuated also, by a factor of 100 or more, so that source of error virtually disappears. When Q1 is off, it is really *OFF*, and its leakage is typically 0.01 pA if the summing point is within a millivolt or two of ground.



Q1, 2N3904 or any silicon NPN

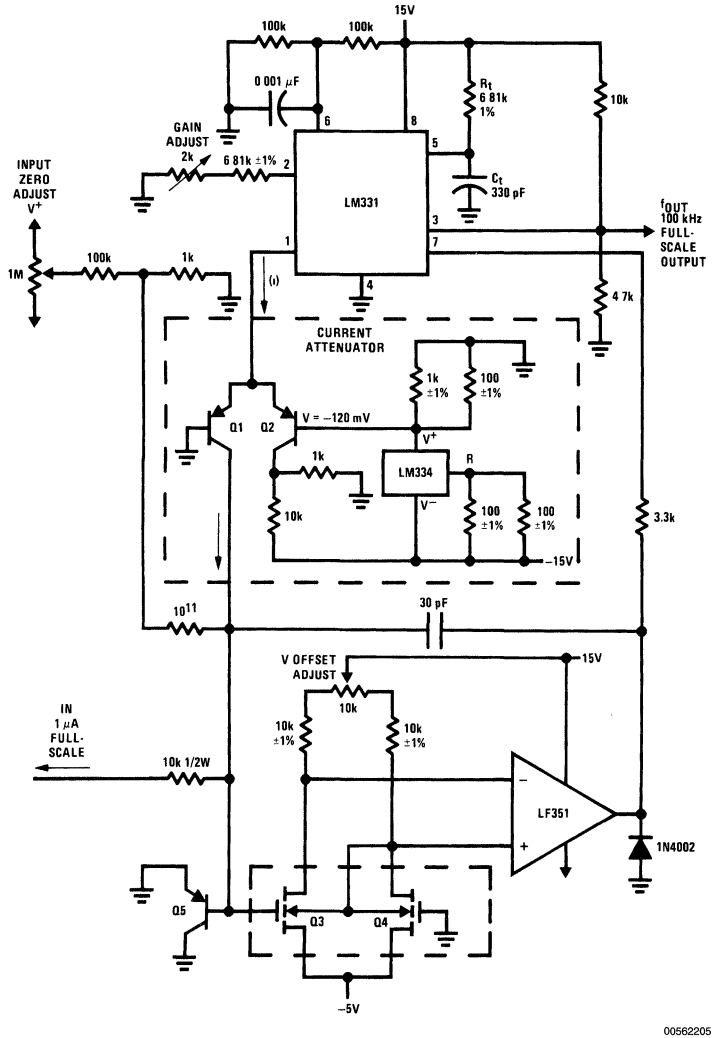
Q2, 2N930 or 2N3565

FIGURE 4. Very-Wide-Range I-to-F Converter with Low Voltage Drift

To do justice to this low leakage of the VFC, the op amp should be made with MOSFETs for Q3 and Q4, such as the Intersil 3N165 or 3N190 dual MOSFET (with no gate-protection diodes). When MOSFETs have relatively poor offset voltage, offset voltage drift, and voltage noise, this circuit does not care much about these characteristics, but instead takes advantage of the MOSFET's superior current leakage and current drift.

Now, with an input current of 1 µA, the full-scale output frequency will be 100 kHz. At a 1 nA input, the output frequency will be 100 Hz. And, when the input current is 1 pA, the output frequency will drop to 1 cycle per 10 seconds or 100 mHz. When the input current drops to zero, frequencies as small as 500 µHz have been observed, at 25°C and also as warm as 35°C. Here is a wide-range data converter whose zero drift is *well* below 1 ppm per 10°C! (Rather more

like 0.001 ppm per°C.) The usable dynamic range is better than 140 dB, with excellent accuracy at inputs between 100% and 1% and 0.01% and 0.0001% of full-scale.



Q1, Q2, Q5 - 2N3906, 2N4250 or similar
Q3, Q4 - 3N165, 3N190 or similar See text
Keep Q1, Q2 and LM334 at the same temperature

FIGURE 5. Picoampere-to-Frequency Converters

If a positive signal is of interest, the LM331 can be applied with a current reflector as in *Figure 6*. This current reflector has high output impedance, and low leakage. Its output can go directly to the summing point, or via a current attenuator made with NPN transistors, similar to the PNP circuit of *Figure 5*. This circuit has been observed to cover a wide (130 dB) range, with 0.1% of signal accuracy.

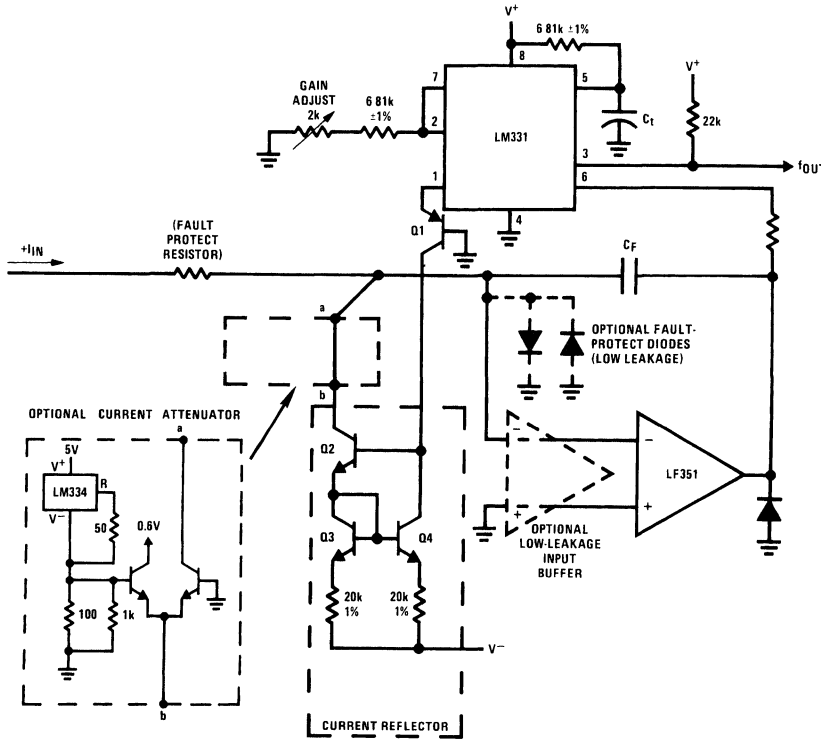
What is the significance of this wide-range current-to-frequency converter? In many industrial systems the question of using an inexpensive 8-bit converter instead of an expensive 12-bit data converter is a battle which is decided everyday. But if the signal source is actually a current source, then you can use a V-to-F converter to make a cheap 14-bit converter or an inexpensive converter with 18 bits of dynamic range. The choice is yours.

Why use an I-to-F converter?

- It is a natural form of A-to-D conversion.
- It naturally facilitates integration, as well.
- There are many signals in the world, such as photospectrometer currents, which like to be digitized and integrated as a standard part of the analysis of the data.
- Similarly: photocurrents, dosimeters, ionization currents, are examples of currents which beg to be integrated in a current-to-frequency meter.
- Other signal sources which provide output currents are:
  - —Phototransistors
  - —Photo diodes
  - —Photoresistors (with a fixed voltage bias)
  - —Photomultiplier tubes
  - —Some temperature sensors
  - —Some IC signal conditioners

Why have a fast frequency out?

- A 100 kHz output full-scale frequency instead of 10 kHz means that you have 10 times the resolution of the signal. For example, when I_{IN} is 0.01% of full-scale, the f will be 10 Hz. If you integrate or count that frequency for just 10 seconds, you can resolve the signal to within 1% – a factor of 10 better than if the full-scale frequency were slower.



Q1 - 2N4250 or 2N3906

Q2, Q3, Q4 - 2N3904 or 2N3565

FIGURE 6. Current-to-Frequency Converter For Positive Signals

Using the ADC0808/ADC0809 8-Bit µP Compatible A/D Converters with 8-Channel Analog Multiplexer

National Semiconductor
Application Note 247
Larry Wakeman

Introduction

The ADC0808/ADC0809 Data Acquisition Devices (DAD) implement on a single chip most the elements of the standard data acquisition system. They contain an 8-bit A/D converter, 8-channel multiplexer with an address input latch, and associated control logic. These devices provide most of the logic to interface to a variety of microprocessors with the addition of a minimum number of parts.

These circuits are implemented using a standard metal-gate CMOS process. This process is particularly suitable to applications where both analog and digital functions must be implemented on the same chip.

These two converters, the ADC0808 and ADC0809, are functionally identical except that the ADC0808 has a total unadjusted error of ±½ LSB and the ADC0809 has an unadjusted error of ±1 LSB. They are also related to their big brothers, the ADC0816 and ADC0817 expandable 16 channel converters. All four converters will typically do a conversion in ~100 µs when using a 640 kHz clock, but can convert a single input in as little as ~50 µs.

Functional Description

The ADC0808/ADC0809, shown in *Figure 1*, can be functionally divided into 2 basic subcircuits. These two subcircuits are an analog multiplexer and an A/D converter. The multiplexer uses 8 standard CMOS analog switches to provide for up to 8 analog inputs. The switches are selectively turned on, depending on the data latched into a 3-bit multiplexer address register.

The second function block, the successive approximation A/D converter, transforms the analog output of the multiplexer to an 8-bit digital word. The output of the multiplexer goes to one of two comparator inputs. The other input is derived from a 256R resistor ladder, which is tapped by a MOSFET transistor switch tree. The converter control logic controls the switch tree, funneling a particular tap voltage to the comparator. Based on the result of this comparison, the control logic and the successive approximation register (SAR) will decide whether the next tap to be selected should be higher or lower than the present tap on the resistor ladder. This algorithm is executed 8 times per conversion, once every 8 clock periods, yielding a total conversion time of 64 clock periods.

When the conversion cycle is complete the resulting data is loaded into the TRI-STATE® output latch. The data in the output latch can then be read by the host system any time before the end of the next conversion. The TRI-STATE capability of the latch allows easy interface to bus oriented systems.

The operation of these converters by a microprocessor or some control logic is very simple. The controlling device first selects the desired input channel. To do this, a 3-bit channel address is placed on the A, B, C input pins; and the ALE input is pulsed positively, clocking the address into the multiplexer address register. To begin the conversion, the START pin is pulsed. On the rising edge of this pulse the internal registers are cleared and on the falling edge the start conversion is initiated.

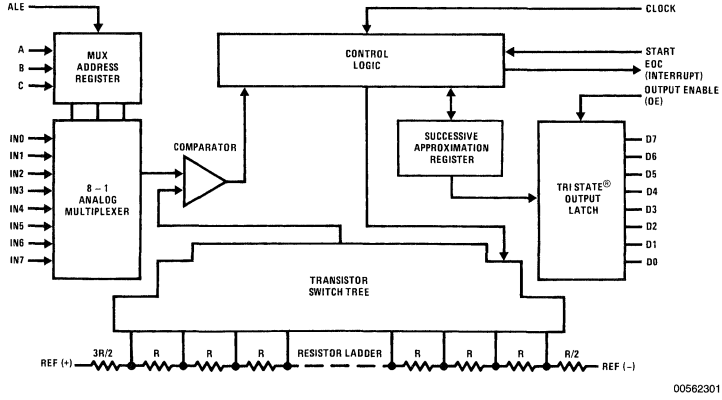


FIGURE 1. ADC0808/ADC0809 Functional Block Diagram

Functional Description (Continued)

As mentioned earlier, there are 8 clock periods per approximation. Even though there is no conversion in progress the ADC0808/ADC0809 is still internally cycling through these 8 clock periods. A start pulse can occur any time during this cycle but the conversion will not actually begin until the converter internally cycles to the beginning of the next 8 clock period sequence. As long as the start pin is held high no conversion begins, but when the start pin is taken low the conversion will start within 8 clock periods.

The EOC output is triggered on the rising edge of the start pulse. It, too, is controlled by the 8 clock period cycle, so it will go low within 8 clock periods of the rising edge of the start pulse One can see that it is entirely possible for EOC to go low before the conversion starts internally, but this is not important, since the positive transition of EOC, which occurs at the end of a conversion, is what the control logic is looking for.

Once EOC does go high this signals the interface logic that the data resulting from the conversion is ready to be read. The output enable (OE) is then raised high. This enables the TRI-STATE outputs, allowing the data to be read. *Figure 3* shows the timing diagram.

Analog Inputs

RATIOMETRIC INPUTS

The arrangement of the REF(+) and REF(−) inputs is intended to enable easy design of ratiometric converter systems. The REF inputs are located at either end of the 256R resistor ladder and by proper choice of the input voltages several applications can be easily implemented.

Figure 2 shows a typical input connection for ratiometric transducers. A ratiometric transducer is a conversion device whose output is proportional to some arbitrary full-scale value. In other words, the transducer's absolute output value is of no particular concern but the ratio of the output to the full-scale is of great importance. For example, the potentiometric displacement transducers of *Figure 2* have this feature. When the wiper is at midscale, the output voltage is $V_O = V_F \times$ (Wiper Displacement) $= V_F \times 0.5$. This enables the use of much less accurate and less expensive references. The important consideration for this reference is noise. The reference must be "glitch free" because a voltage spike during a conversion cycle could cause conversion inaccuracies.

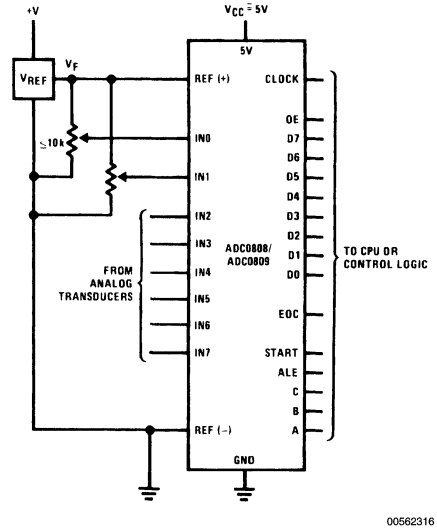


FIGURE 2. Ratiometeric Converter with Separate Reference

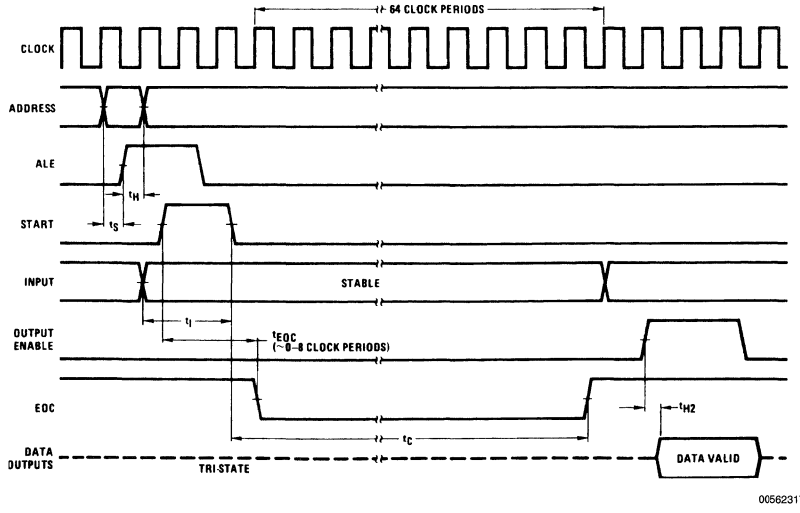


FIGURE 3. ADC0808/ADC0809 Timing Diagram

Analog Inputs (Continued)

Since highly accurate references aren't required it is possible to use the system power supply as a reference, as shown in *Figure 4*. If the power supply is to be used in this manner supply noise must be kept to a minimum to preserve conversion accuracy. If possible the supply should be well bypassed and separate reference and supply PC board traces, originating as close as possible to the power supply or regulator, should be used. This is illustrated in *Figure 4*. External accessibility of both ends of the resistor ladder enables several variations on these basic connections, and are shown in *Figures 5, 6*. The magnitude of the reference voltage, V_{REF} = REF(+) – REF(–), can be varied from about –0.5V to V_{CC}, but the center voltage must be maintained within ±0.1V of $V_{CC}/2$. This constraint is due to the design of the transistor switch tree, which could malfunction if the offset from center scale becomes excessive. Variation of the reference voltage can sometimes eliminate the need for external gain blocks to scale the input voltage to a full-scale range of 5V.

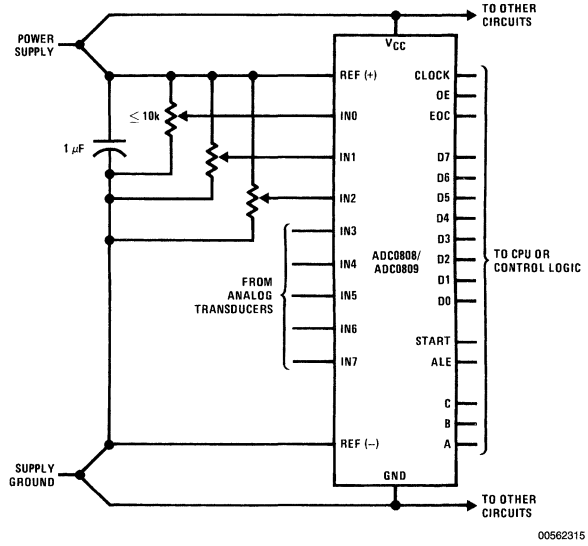


FIGURE 4. Ratiometric Converter with Power Supply Reference

Analog Inputs (Continued)

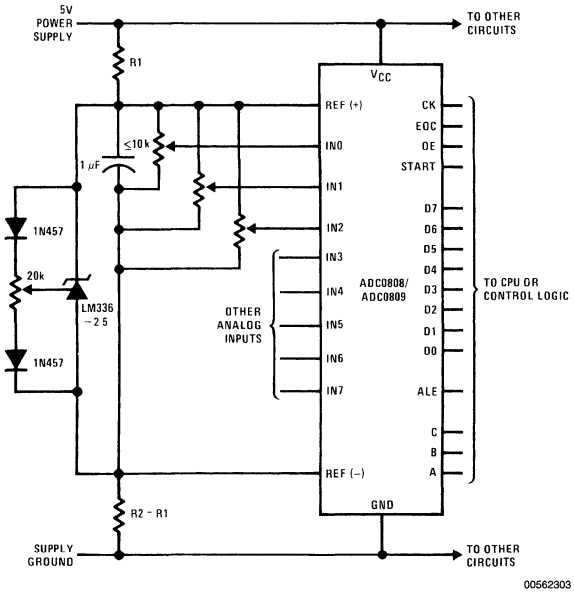


FIGURE 5. Mid-Supply Centered Reference Using LM336 2.5V Reference

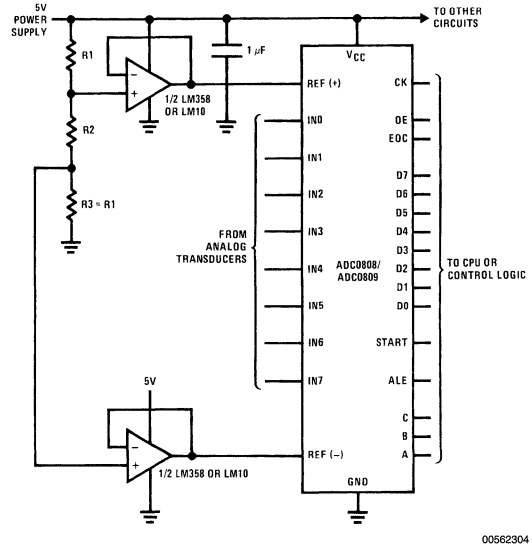


FIGURE 6. Mid-Supply Centered Reference Using Buffered Resistors

Figure 5 shows a center referencing technique, using two equal resistors to symmetrically offset an LM336 2.5V reference, from both supplies. The offset from either supply is:

$$V_{OFF} = \frac{V_{CC} - V_{REF}}{2} = 1.25V$$

Analog Inputs (Continued)

These resistors should be chosen so that they limit current through the LM336 to a reasonable value, say 5 mA. The total resistor current is:

$$I_R = I_{REF} + I_{LADDER} + I_{TRAN}$$

where I_{LADDER} is the 256R ladder current, I_{TRAN} is the current through all the transducers, and I_{REF} is the current through the reference. R1 and R2 should be well matched and track each other over temperature.

For odd values of reference voltage, the reference could be replaced by a resistor, but due to loading and temperature problems, these resistors should be buffered to the REF(+) and REF(−) inputs, *Figure 6*. The power supply must be well bypassed as supply glitches would otherwise be passed to the reference inputs. The reference voltage magnitude is:

$$V_{REF} = V_{DD}\left(\frac{R2}{2R1 + R2}\right) \text{ For } R3 = R1$$

There are several op amps that can be used for buffering this ladder. Without adding another supply, an LM358 could be used if the REF(+) input is not to be set above 3.5V. The LM10 can swing closer to the positive supply and can be used if a higher $V_{REF(+)}$ voltage is needed.

As the REF(+) to REF(−) voltage decreases the incremental voltage step size decreases. At 5V one LSB represents ~20 mV, but at 1V, one LSB represents ~4 mV.

As the reference voltage decreases, system noise will become more significant so greater precaution should be enforced at lower voltages to compensate for system noise; i.e., adequate supply and reference bypassing, and physical as well as electrical isolation of the inputs.

ABSOLUTE ANALOG INPUTS

The ADC0808/ADC0809 may have been designed to easily utilize ratiometric transducers, but this does not preclude the use of non-ratiometric inputs. A second type of input is the absolute input. This is one which is independent of the reference. This implies that its *absolute* numerical voltage value is very critical, and to accurately measure this voltage the accuracy of the reference voltage becomes equally critical. The previous designs can be modified to accommodate absolute input signals by using a more accurate reference. In *Figure 4* the power supply reference could be replaced by LM336-5.0 reference. R1 and R2 of *Figure 6*, and R1 and R3 of *Figure 7* may have to be made more accurately equal.

In some small systems it is possible to use the precision reference as the power supply as shown in *Figure 7*. An unregulated supply voltage >5V is required, but the LM336-5.0 functions as both a regulator and reference. The dropping resistor R must be chosen so that, for the whole range of supply currents needed by the system, the LM336-5.0 will stay in regulation. As in *Figure 4* separate supply and reference traces should be used to maintain a noiseless supply.

If the system requires more power, an op amp can be used as shown in *Figure 8* to isolate the reference and boost the supply current capabilities. Here again, a single unregulated supply is required.

DIFFERENTIAL INPUTS

Differential measurements can be obtained by playing a little software trick. This simply involves sequentially converting two channels then subtracting the two results. For example, if the difference voltage between channel 1 and 2 is required, merely convert channel 1 and read the result. Then convert channel 2, input the result, and subtract it from the first result. (See *Figure 9*.) When using this procedure, both input signals must be stable throughout both conversion times or the end result will be incorrect. One way to get around this is to use two sample/holds which are sampled at the same time.

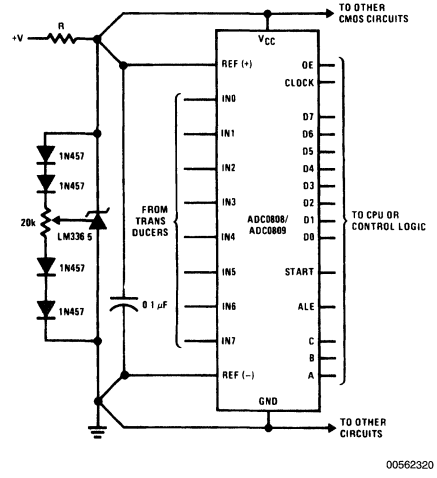


FIGURE 7. Precision Reference used as a Power Supply

Analog Inputs (Continued)

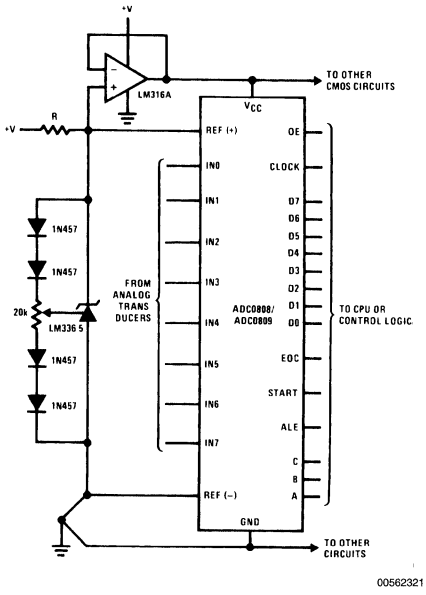


FIGURE 8. Precision Reference Buffered for Power Supply

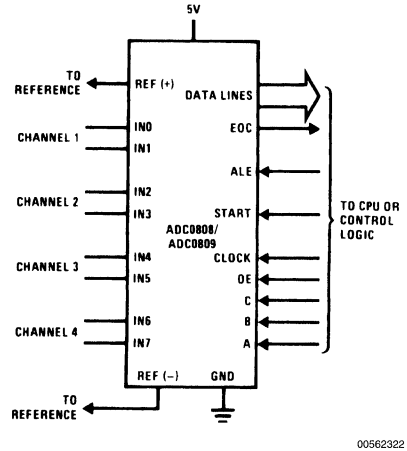


FIGURE 9. Software Controlled Differential Converter

A second method is to use two chips to convert a differential channel, *Figure 10*. Typically each channel 1 would be connected to opposite sides of the differential input. Both converters are started simultaneously. When both converters' EOC outputs go high the output of the AND gate will go high indicating that the data is ready to be read.

The circuit in *Figure 10* can be slightly modified to provide increased data throughput by using two converters in a parallel data acquisition scheme. *Figure 11* shows this circuit in which all the input channels are connected in pairs through LF398 monolithic sample/holds. Under normal operation a sample/hold is accessed through an MM74C42 which will pulse an MM74C221, generating a sample pulse. After a sample/hold is done sampling the signal, the appropriate channel is started. If this process is alternated between two converters the sample rate can be doubled.

Analog Inputs (Continued)

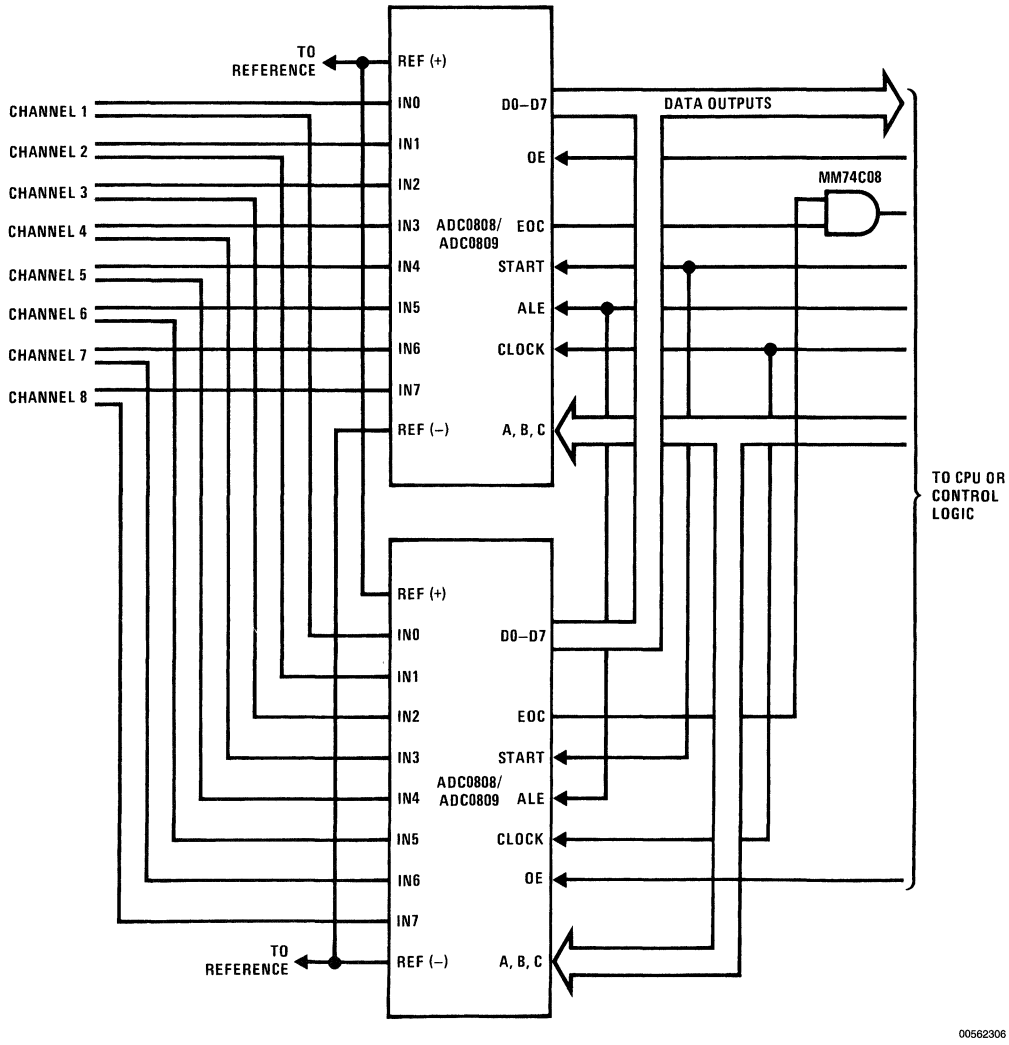


FIGURE 10. Dual Converter Differential Circuit

Analog Inputs (Continued)

ANALOG INPUT CONSIDERATIONS

Analog inputs into the ADC0808/ADC0809 can handle any input signal that is maintained within the supply limits, but some careful consideration must be given to the output impedance of the transducer or buffer. Using transducers with large source impedances can cause errors due to comparator input currents.

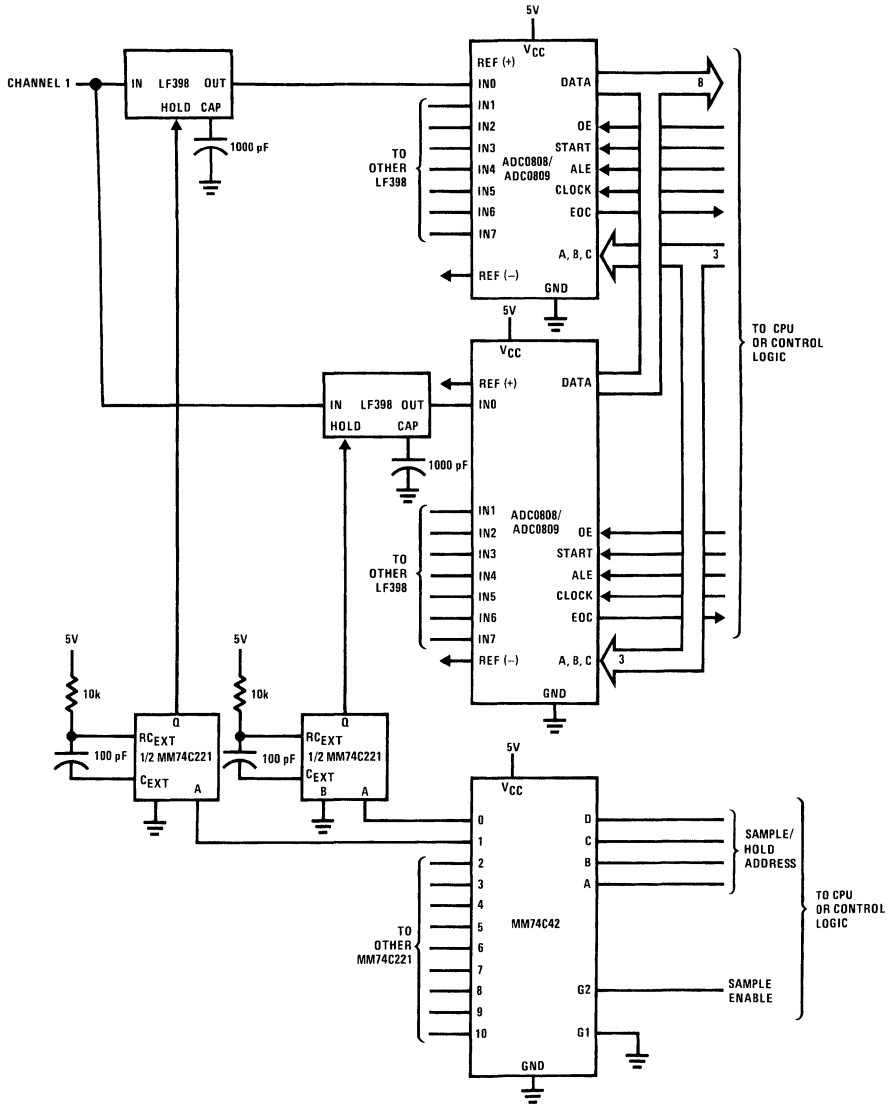


FIGURE 11. Parallel Data Acquisition with Sample/Holds

Analog Inputs (Continued)

To understand the nature of these currents a short discussion of comparator operation is required. *Figure 12* shows a simplified model of the comparator and multiplexer. This comparator alternately samples the input voltage and the ladder voltage. As it samples the input, C_C and C_P are charged up to the input voltage. It then samples the ladder and discharges the capacitor. The net charge difference is determined by a modified inverter chain and results in a 1 or 0 state at the output.

Eight samples are made per conversion, resulting in eight spikes of varying magnitude on the input.

If the source resistance is large, it adds to the RC time constant of the switched capacitor which will inhibit the input from settling properly, causing errors. As one might expect, the maximum source resistance allowable for accurate conversions is inversely proportional to clock frequency. This resistance should be ≤1 kΩ at 1.2 MHz and ≤2 kΩ at 640 kHz. If a potentiometer-type ratiometric transducer is used it should be ≤5 kΩ at 1.2 MHz and ≤10 kΩ at 640 kHz.

If large source impedances are unavoidable (≥2 kΩ at 640 kHz), the transient errors can be reduced by placing a bypass capacitor ≥0.1 µF from the analog inputs to ground. This will reduce the spikes to a small average current which will cause some error as well, but this can be much less than the error otherwise incurred. The maximum voltage error for a potentiometer input with a bypass capacitor added is:

$$V_{ERR} \approx \left[\frac{R_{POT}}{5}(I_{IN})\frac{Ck}{640\ kHz}\right] V$$

where R_{POT} = total potentiometer resistance; I_{IN} = maximum input current at 640 kHz, 2 µA; and Ck=clock frequency.

For standard buffer source impedance the maximum error is:

$$V_{ERR} = \left[I_{IN}R_S\left(\frac{Ck}{640\ kHz}\right)\right] V$$

where R_S = buffer source resistance; I_{IN} = the maximum input current at 640 kHz, 2 µA; and Ck = clock frequency.

Microprocessor Interfacing

The ADC0808/ADC0809 converters were designed to interface to most standard microprocessors with very little external logic, but there are a few general requirements which must be considered to ensure proper converter operation. Most microprocessors are designed to be TTL compatible and, due to speed and drive requirements, incorporate many TTL circuits. The data outputs of the ADC0808/ADC0809 are capable of driving one standard TTL load which is adequate for most small systems, but for larger systems extra buffering may be necessary. The EOC output is not quite as powerful as the data outputs, but normally it is not bussed like the data outputs.

The converter inputs are standard CMOS compatible inputs. When TTL outputs are connected to any of the digital inputs a pull-up resistor should be tied from the TTL output to V_{CC}, ~ 5 kΩ. This will ensure that the TTL will pull-up above 3.5V.

Usually the converter clock will be derived from the microprocessor system clock. Some slower microprocessor clocks can be used directly, but at worst a few divider stages may be necessary to divide microprocessor clock frequencies above 1.2 MHz to a usable value.

The timing of the START and ALE pulses relative to channel selection and signal stability can be critical. The simplest approach to microprocessor interfaces usually ties START and ALE together. When these lines are strobed the address is strobed into the address register and the conversion is started. The propagation delay from ALE to comparator input of the selected input signal is about ~3.0 µs (input source resistance $<<1$ kΩ). If the start pulse is very short the comparator can sample the analog input before it is stable. When using a slow clock ≤500 kHz the sample period of the comparator input is long enough to allow this delay to settle out.

If the ADC0808/ADC0809 clock is >500 kHz, a delay between the START and ALE pulses is required. There are three basic methods to accomplish this. The first possibility is to design the microprocessor interface so that the START and ALE inputs are separately accessible. This is simple if some extra address decoding is available. Separate accessibility of the START and ALE pins allows the microprocessor, via software, to set the delay time between the START and ALE pulses.

If extra decoding is not available, then START and ALE could be tied together. To obtain the proper delay, the microprocessor would cause START/ALE to be strobed twice by executing the load and start instruction twice. The first time this instruction is executed, the new channel address is loaded and the conversion is started. The second execution of this instruction will reload the same channel address and restart the conversion. But since the multiplexer address register contents are unchanged the selected analog input will have already settled by the time the second instruction is issued. Actual implementations of these ideas are shown in following sections.

Microprocessor Interfacing (Continued)

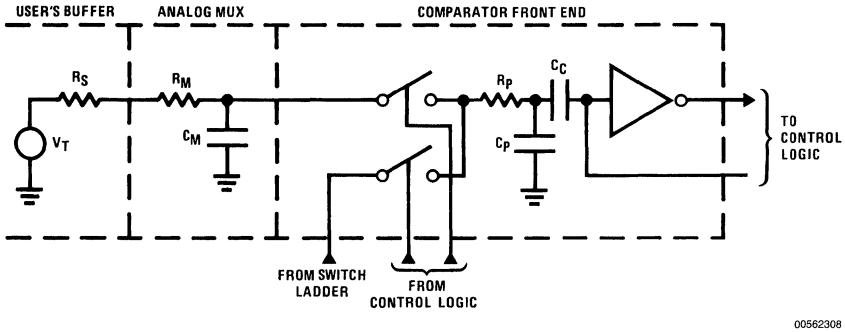


FIGURE 12. Analog Multiplexer and Comparator Input Model

A third possibility when ALE and START are tied together is to stretch the microprocessor derived ALE/START pulse by inserting a one-shot at these inputs and creating a positive pulse >3 µs. Since ALE loads the multiplexer register on the positive going edge of the pulse and START begins the conversion on the falling edge, the width of the pulse sets the ALE to START delay time.

Most microprocessor interfaces would be designed such that a START pulse is issued by a memory or I/O write instruction, although a memory or I/O read can be used. The ALE strobe on the other hand, requires a write by the CPU when A, B, and C are connected to the data bus, and could use a read instruction if A, B, and C are connected to the address bus, but the software could get confusing. The logic to derive the OE strobe must be connected to the microprocessor so that a memory or I/O read instruction will cause OE to be pulsed. A read is required since the ADC0808/ADC0809 data must be read.

Interfacing to the 8080

The simplest interface would contain no address decoding, which may seem unreasonable; but if the system ports are I/O mapped, up to 8 of them can be connected to the CPU with no decoding. Each of the 8 I/O address lines would serve as a simple port enable line which would be gated with read and write strobes to select a particular port. This scheme is shown in *Figure 13*. A7 is the address line used and, whenever it is zero and an I/O read or write is low, the port is accessed. This implementation shows A, B, C connected to D0, D1, D2 causing the information on the data bus to select the channel, but A, B, and C could be connected to the address bus, with a loss of only 3 ports. Both decoding schemes are tabulated in *Figure 14*. (Remember A, B, C inputs are only valid when selecting a channel to convert, and are not used to read data.)

Interfacing to the 8080 (Continued)

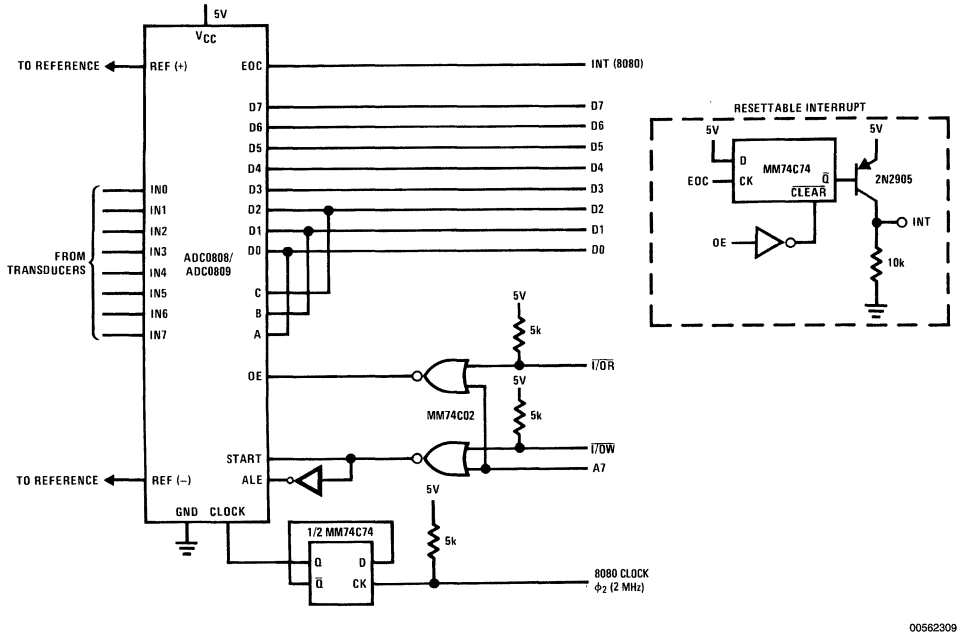


FIGURE 13. Minimum 8080/8224/8228 Interface

A7	A6	A5	A4	A3	A2	A1	A0	D2	D1	D0	Output Port Description
1	1	1	1	1	1	1	0	X	X	X	Spare Port
1	1	1	1	1	1	0	1	X	X	X	Spare Port
1	1	1	1	1	0	1	1	X	X	X	Spare Port
1	1	1	1	0	1	1	1	X	X	X	Spare Port
1	1	1	0	1	1	1	1	X	X	X	Spare Port
1	1	0	1	1	1	1	1	X	X	X	Spare Port
1	0	1	1	1	1	1	1	X	X	X	Spare Port
0	1	1	1	1	1	1	1	0	0	0	Channel 0 Port
0	1	1	1	1	1	1	1	0	0	1	Channel 1 Port
0	1	1	1	1	1	1	1	0	1	0	Channel 2 Port
0	1	1	1	1	1	1	1	0	1	1	Channel 3 Port
0	1	1	1	1	1	1	1	1	0	0	Channel 4 Port
0	1	1	1	1	1	1	1	1	0	1	Channel 5 Port
0	1	1	1	1	1	1	1	1	1	0	Channel 6 Port
0	1	1	1	1	1	1	1	1	1	1	Channel 7 Port

FIGURE 14. Write Address Decoding for 8080 Output Ports (A, B, C Connected to D0, D1, D2)

Interfacing to the 8080 (Continued)

A7	A6	A5	A4	A3	A2	A1	A0	Output Port Description
0	1	1	1	1	0	0	0	Channel 0 Port
0	1	1	1	1	0	0	1	Channel 1 Port
0	1	1	1	1	0	1	0	Channel 2 Port
0	1	1	1	1	0	1	1	Channel 3 Port
0	1	1	1	1	1	0	0	Channel 4 Port
0	1	1	1	1	1	0	1	Channel 5 Port
0	1	1	1	1	1	1	0	Channel 6 Port
0	1	1	1	1	1	1	1	Channel 7 Port
1	1	1	1	0	X	X	X	Spare Port
1	1	1	0	1	X	X	X	Spare Port
1	1	0	1	1	X	X	X	Spare Port
1	0	1	1	1	X	X	X	Spare Port

X = don't care

FIGURE 15. Modified Write Address Decoding for 8080 Output Ports (A, B, C Connected to A0, A1, A2)

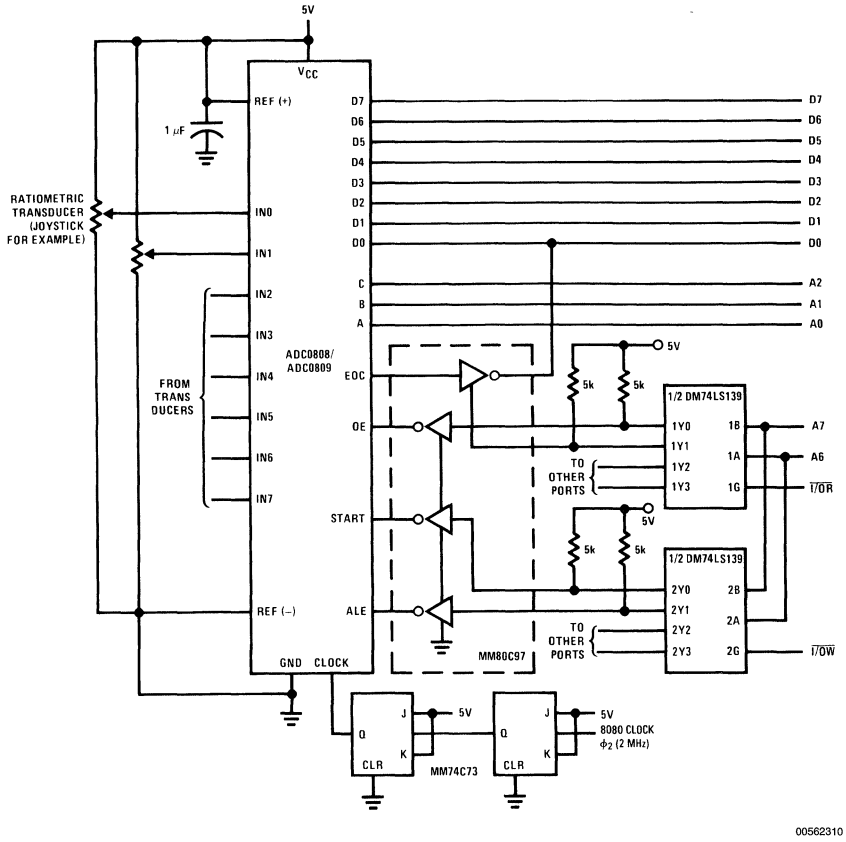
Two LSTTL NOR gates are used to generate the ADC0808/ADC0809 read/write strobes. When the 8080 writes to the ADC0808/ADC0809 the ALE and START inputs are strobed, loading and starting the conversion. When the CPU reads the ADC0808/ADC0809 the OE input is taken high, and the data outputs are enabled.

Figure 13 implements a simple interrupt concept where EOC is tied directly to the 8080 interrupt input. When the INS8228 is used and the INTA pin is tied high through a 1 kΩ resistor, the interrupt will cause a restart, RST, instruction to be executed, which will then cause a jump to a restart vector and execution of the interrupt routine. If a very simple multi-interrupt system is desired, a wire OR'ed configuration employing resettable latches as shown in *Figure 13's* inset can be used. In this simple design the MM74C74 is reset when the ADC0808/ADC0809 data is read. If more complicated interrupt structures are required, then an interrupt controller is usually the best solution.

The I/O port address structure for *Figure 13's* implementation is shown in *Figure 14*. If the A, B, C inputs are tied to A0, A1, A2 inputs the port structure is as shown in *Figure 15*. The latter method makes each channel look like a separate port address, whereas if A, B, C are tied to the data bus the ADC0808/ADC0809 looks like one start conversion port address whose channel is selected by the 3-bit status word written to it on the data bus.

Figure 16 shows a slightly more complex interface, where the address is partially decoded by a DM74LS139, dual 2-4 line decoder which creates the read and write strobes to operate the converter. This design interfaces to the processor in a polled type of interface. An MM80C97 TRI-STATE buffer is used to buffer the EOC line to the data bus, as well as provide the correct level for the START, ALE, and OE pulses. The converter clock is a divided 8080 system clock.

Interfacing to the 8080 (Continued)



Address A7–A0								Description
0	0	X	X	X	X	X	X	Write-Start Conv.
0	0	X	X	X	X	X	X	Read-Input Data
0	1	X	X	X	0	0	0	Channel 1 Select
0	1	X	X	X	0	0	1	Channel 2 Select
0	1	X	X	X	0	1	0	Channel 3 Select
0	1	X	X	X	0	1	1	Channel 4 Select
0	1	X	X	X	1	0	0	Channel 5 Select
0	1	X	X	X	1	0	1	Channel 6 Select
0	1	X	X	X	1	1	0	Channel 7 Select
0	1	X	X	X	1	1	1	Channel 8 Select
0	1	X	X	X	X	X	X	Read-Input $\overline{EOC}$

FIGURE 16. 8080/8224/8228 Interface Using Partial Decoding

Interfacing to the 8080 (Continued)

Typically, the software to use *Figure 16* would first select the desired channel by writing the channel address to the ALE port address, 01XXXCBA, where X=don't care, and CBA is the channel address. Next the conversion is started by writing to the START address, 00XXXXXX. Now the processor must wait a few instruction cycles to allow EOC to fall. Once EOC falls, its status can be checked by reading the EOC line, address 01XXXXXX. When the EOC line is detected high again (a low on DO), the data can be read by accessing the OE port, address 00XXXXXX. As in the previous example the A, B, C inputs can be tied to D0, D1, D2 rather than A0, A1, A2, so that the information on the data bus selects the channel to be converted. *Figure 16* can be connected in an interrupt mode by incorporating the interrupt flip-flop of *Figure 13*.

A few typical utility routines to operate the ADC0808/ADC0809 application in *Figure 13* are shown in *Figure 17*. These routines assume that the resettable interrupt flip-flop is used. *Figure 18* illustrates some typical polled I/O routines for *Figure 16*. Notice that in *Figure 17* the OUT START1 instruction is executed twice to allow the analog input signal to settle as discussed earlier.

```
;
;
; START CONVERSION (A, B, C CONNECTED TO D0, D1, D2)
;
CHANN1          EQU     7
START1          EQU     7FH
DATA            EQU     7FH
;
START:          LDA     CHANN1      ; LOAD CHANNEL ADDRESS INTO ACE
                OUT     START1      ; STORE IT TO ADC0808/ADC0809 AND START
                OUT     START1      ; RESTART ADC0808/ADC0809 TO ACCOUNT FOR
;                                   ; MULTIPLEXER DELAY
                EI                  ; ENABLE INTERRUPTS IF NOT ALREADY
                —       —           ; PROCESS PROGRAM
;
; INTERRUPT HANDLER ROUTINE
;
INTRP:          IN      DATA        ; READ DATA AND RESET INTERRUPT
                —       —           ; PROCESS DATA
                EI                  , ENABLE INTERRUPTS IF DESIRED
                RET                 ; RETURN TO MAIN PROGRAM
```

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FIGURE 17. Typical 8080 Resettable Interrupt I/O Routines

Interfacing to the 8080 (Continued)

```
;
; START CONVERSION (A, B, C CONNECTED TO A0, A2, A3) AND POLL EOC
; (FIGURE 15)
SELECT          EQU     40H     ; SELECT CHANNEL 0
START           EQU     00H     , START CONVERTER
EOCIN           EQU     40H     ; READ EOC
DATA            EQU     00H     ; READ DATA
START:          OUT     SELECT  ; SELECT CHANNEL
                OUT     START   ; START CONVERSION
                NOP             ; INSERT INSTRUCTIONS TO WAIT 0-8
                NOP             ; CLOCK PERIODS OF ADC0808/ADC0809 CLOCK
                NOP             ; FOR EOC TO DROP (8NOPs MINIMUM)
                NOP
                NOP
;
; READ AND TEST EOC
;
STATUS:         IN      EOCIN   ; INPUT EOC BIT
                ANI     01H     ; MASK OUT OTHER BITS
                JZ      READY   ; IF INPUT BIT IS ZERO JUMP READY
                —       —       ; ELSE CONTINUE EXECUTING PROGRAM
; OR
; CONTINUOUS POLLING ROUTINE
;
STAT 2:         IN      EOCIN   ; INPUT EOC STATUS BIT
                ANI     01H     ; MASK OUT ALL BITS BUT D0
                JNZ     STAT 2  ; JUMP TO TRY AGAIN IF NOT READY
READY:          IN      DATA    ; IF READY INPUT DATA
                —       —       ; CONTINUE EXECUTING PROGRAM
```

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FIGURE 18. Typical Polled I/O Routines for ADC0808/ADC0809

Interfacing to the 8080 (Continued)

The application in *Figure 19* uses a 6-bit bus comparator and a few gates to decode a read and write strobe. Viewed from the CPU this interface looks like a bidirectional data port whose address is set by the logic levels on the T_n inputs of the DM8131 comparator. When data is written to the ADC0808/ADC0809 the 3 least significant bits on the address bus define the channel to be converted. The rest of the bits are decoded to provide the START and ALE strobes. When the conversion is completed EOC sets the interrupt flip-flop, and when the data is read the interrupt is reset.

Both the decoder and the bus comparator methods of address decoding have their own advantages. Bus comparators will more completely decode addresses but are capable of only a limited number of port strobes. Decoders, on the other hand, provide less decoding but more port strobes. There is a trade off for minimum parts systems as far as which route to go, and it will depend on the CPU and type of system.

INTERFACING TO THE 6800

The ADC0808/ADC0809 easily interface to more than one microprocessor. The 6800 can also be used to control the converter. The 6800 has no separate I/O address space so all I/O transfers must be memory mapped. In general more address decoding logic is required to ensure that the I/O ports don't overlap existing memory. For small systems a partial address decoding scheme is shown in *Figure 20*. Generally, if several ports are desired, a small block of memory would be set aside, as is accomplished by the DM8131. *Figure 20* also illustrates a typical 6800 interrupt scheme using a flip-flop and open collector transistor. The interrupt is reset when the data is read. If more ports are needed, a decoder could be added as shown in *Figure 21*. *Figure 21* also illustrates a polled I/O mode using TRI-STATE buffer to gate EOC onto the data bus. As with the INS8080 the A, B, C inputs of the ADC0808/ADC0809 can be connected to the address bus or the data bus.

The 6800 differs from the INS8080 in that the 6800 has a single read/write (R/$\overline{W}$) strobe and a valid memory address (VMA), whereas the INS8080 has separate read and write strobes ($\overline{I/OR}$ and $\overline{I/OW}$). Normally, to obtain a read pulse, VMA, R/$\overline{W}$ and ϕ_2 are gated together and, for a write R/$\overline{W}$ is inverted. ϕ_2 is the 6800 phase 2 system clock. Also notice that the 6800 $\overline{INT}$ interrupt input is active low. This enables a standard wired-OR open collector design to be implemented.

Figure 22 illustrates some typical 6800 software utility routines for either polled or interrupt interfaces. Again notice double start instructions.

Z80 INTERFACE

Interfacing the Z80 to the ADC0808 is much the same as interfacing to an 8080/8224/8228 CPU group. CPU instruction timing is very similar, except the read/write control signals are slightly different. Instead of the $\overline{I/OW}$ write strobe there is the $\overline{IOREQ}$ and $\overline{WR}$ and instead of $\overline{I/OR}$, $\overline{IOREQ}$ and $\overline{RD}$ are supplied.

Interfacing to the 8080 (Continued)

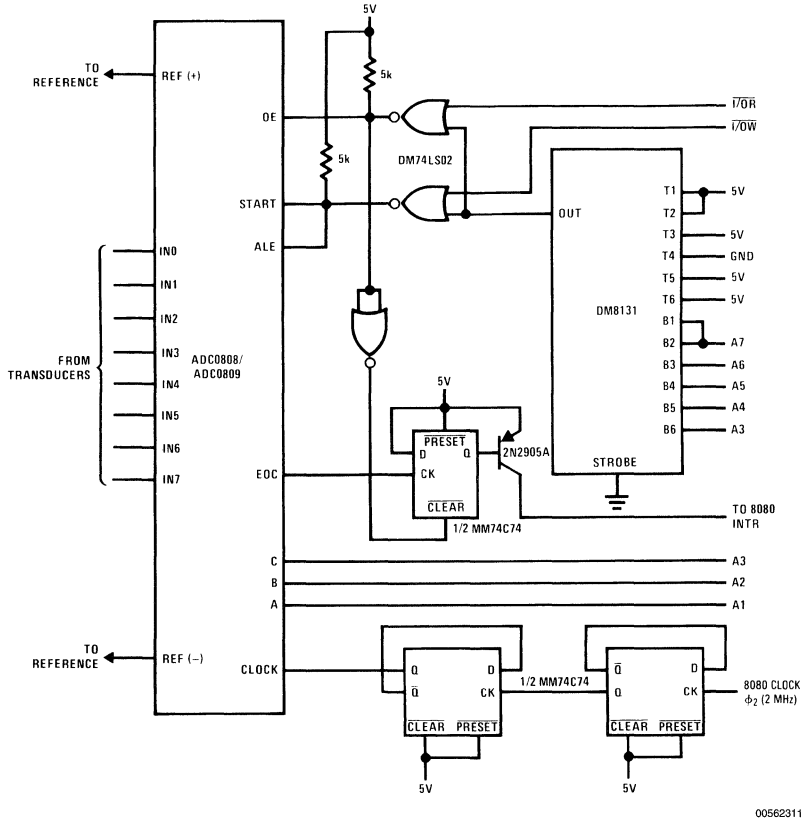

FIGURE 19. Interrupt-Type 8080/8224/8228 Interface Using 6-Bit Bus Comparator

Interfacing to the 8080 (Continued)

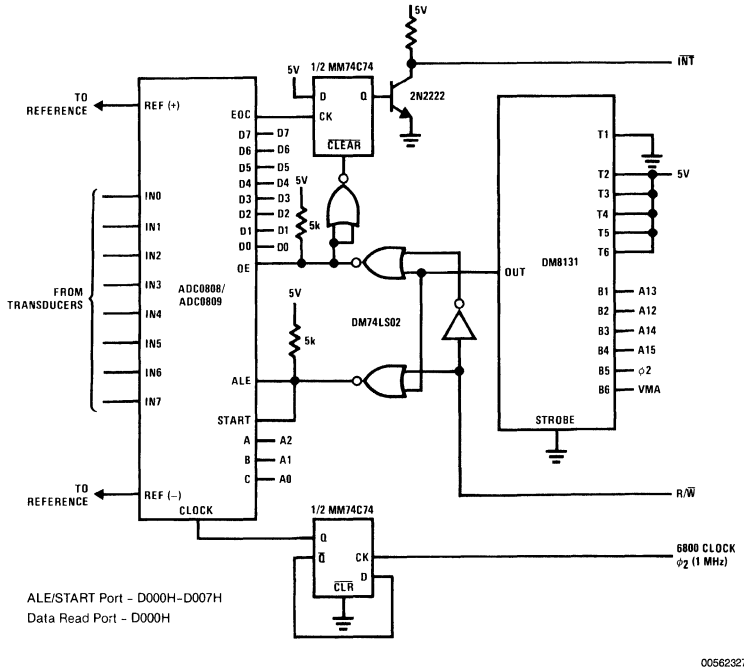

FIGURE 20. Typical 6800 Interface with Partial Address Decoding

Interfacing to the 8080 (Continued)

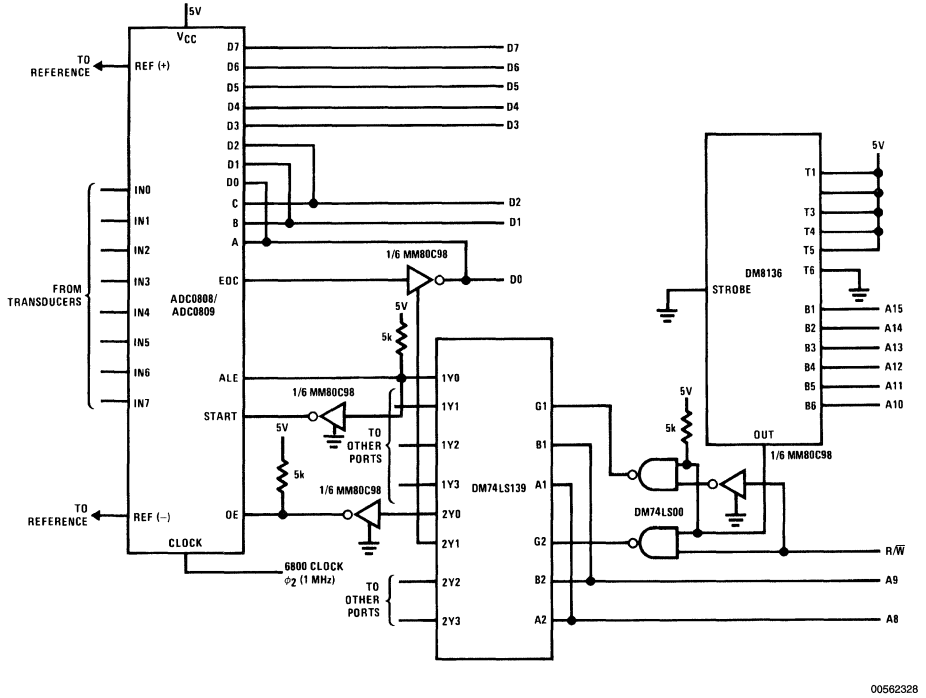

FIGURE 21. Full Decoded 6800 Interface Address

Interfacing to the 8080 (Continued)

```
        *
*UTILITY ROUTINES FOR ADC0808/ADC0809 INTERFACE
        *
        *
*LOAD AND START CONVERSION (FIGURE 18)
        *
STATUS      EQU     $D800     START ADDRESS FOR CHANNEL 0
DATA        EQU     $D800     CONVERTER DATA ADDRESS
        *
        *
        *
START       STA     STATUS    SELECT CHANNEL 0 AND START
            STA     STATUS    DO AGAIN TO LET INPUTS SETTLE
            LDX     #VECTOR   LOAD INTERRUPT VECTOR ADDRESS
            STX     $FFF8     STORE IT
            — —               EXECUTE MISC PROGRAM
            — —
            — —
            CLI               ENABLE INTERRUPT IF NOT ALREADY
            — —               EXECUTE MISC PROGRAM
            WAI               WAIT FOR INTERRUPT
        *
*INTERRUPT HANDLER (FIGURE 18)
        *
VECTOR      LDAA    DATA      LOAD DATA RESET INTERRUPT
            CLI               ENABLE INTERRUPTS (OPTION)
            — —               EXECUTE PROGRAM
            RTI               RETURN TO MAIN PROGRAM
        *
*START AND TEST CONVERSION POLLED MODE (FIGURE 19)
        *
DATA2       EQU     $F800     CONVERTER DATA ADDRESS
CHANN2      EQU     02        CHANNEL 2 ADDRESS
EOCIN       EQU     $F900     EOC INPUT PORT
START2      LDAA    CHANN2    LOAD A ACCUMULATOR
            STAA    STATUS    LOAD ADDRESS AND START
            NOP               WAIT
            STAA    STATUS    RESTART TO LET MUX SETTLE
            NOP               8 NOPS TO WAIT FOR EOC
            — —               TO GO LOW
            LDAA    EOCIN     LOAD EOC STATUS BIT
            ANDA    01        MASK BITS 1–7
            BEQ     READY     IF A = 0 THEN CONVERTER DONE
        *
        *
            — —               EXECUTE MISC PROGRAM
        *
*CONTINUOUS POLLING OF EOC (FIGURE 19)
        *
        *
POLLIT      LDAA    EOCIN     LOAD EOC STATUS
            ANDA    CHANN2    MASK MSBs
            BNE     POLL IT   IT ACC≠0 NOT READY, LOOP
READY LDAA          DATA      ELSE READ DATA
            — —               CONTINUE PROGRAM
            — —
```

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FIGURE 22. Typical I/O Routines for ADC0808/ADC0809 and 6800 Interface

Figure 23 shows a very simple Z80 interface, which is similar to the INS8080 interface of *Figure 13*, except that the inter-

Interfacing to the 8080 (Continued)

rupt flip-flop design is closer to the 6800 designs. This is because the Z80 $\overline{INT}$ is active low as is the 6800, but the INS8080 INT is active high.

Figure 24 shows a fully decoded bus comparator design where the DM8131 decodes 5 address bits and the $\overline{IOREQ}$ I/O request strobe. Two NOR gates gate the $\overline{RD}$ and $\overline{WR}$ strobes for ALE, START and OE inputs.

Conclusion

Both the ADC0808 and the ADC0809 can be easily used in microprocessor controlled environments. Many sophisticated medium throughput applications can be handled with a minimum of extra hardware, but additional hardware can increase flexibility and simplify software. Putting both the multiplexer and A/D on the same chip frees the designer from matching multiplexers and A/Ds to implement a 7 or 8-bit accurate system. Design time and overall system cost can be reduced by using these low cost converters.

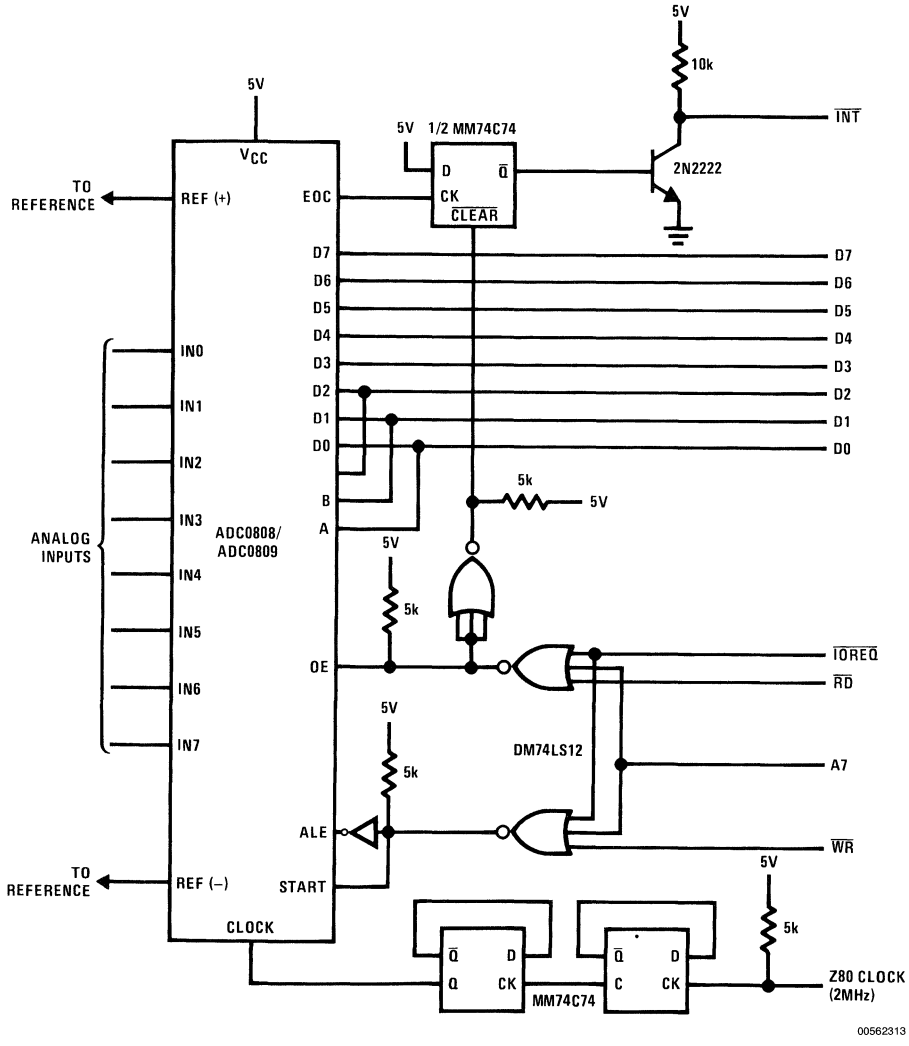


FIGURE 23. Simple Z80 Interface

Conclusion (Continued)

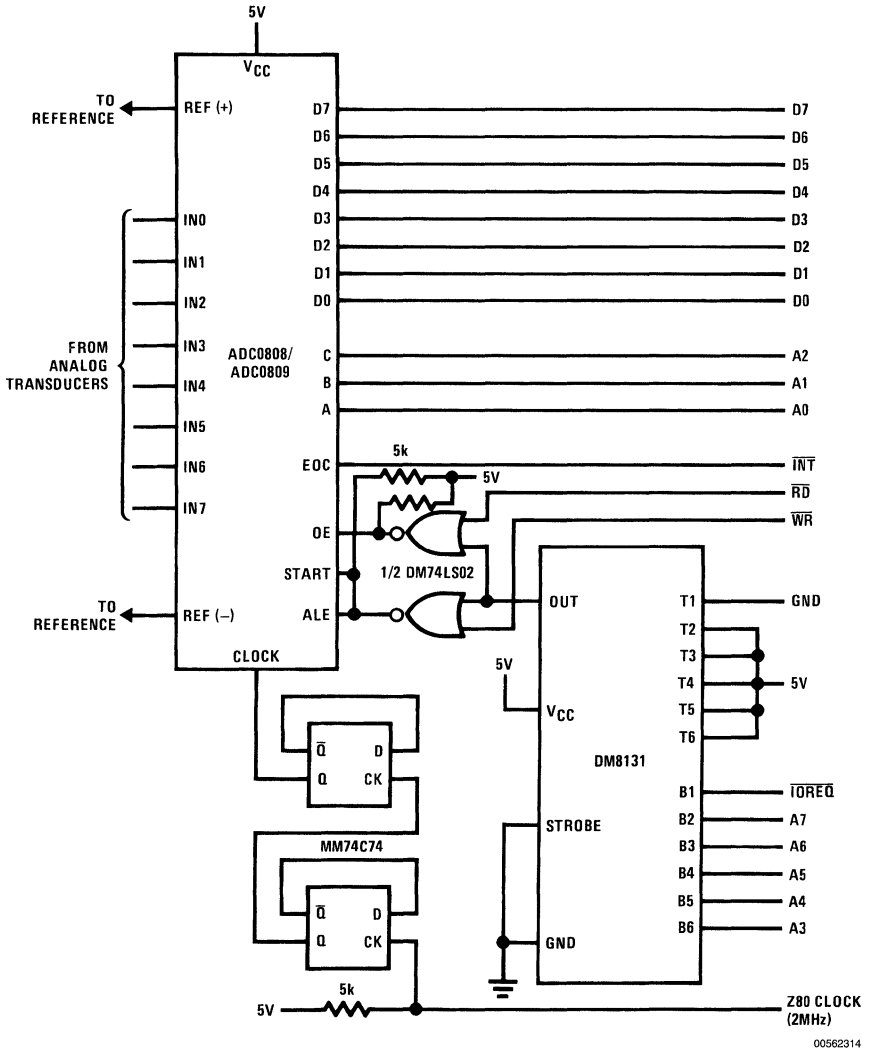


FIGURE 24. Z80 Partial Decoding Interface

A 20-Bit (1 ppm) Linear Slope-Integrating A/D Converter

National Semiconductor
Application Note 260
Larry Wakeman

By combining an "inferior", 20 year old A/D conversion technique with a microprocessor, a developmental A/D converter achieves 1 part-per-million (20-bit) linearity. The absolute accuracy of the converter is primarily limited by the voltage reference available. The precision achieved by the unlikely combination of technologies surpasses conventional approaches by more than an order of magnitude. The approach used points the way towards a generation of "smart" converters, which would feature medium to high resolution (12 bits and above) with high accuracy over extended temperature range. The conversion technique employed, while slow speed, suits transducer based measurement systems which require high resolution over widely varying conditions of time and temperature. In addition, extensions of the basic converter have achieved 15-bit digitization of signal inputs of only 30 mV full-scale with no sacrifice in linearity or stability. This offers the prospect of an "instrumentation converter" which could interface directly with low level analog signals.

One of the many A/D techniques utilized in the late 50's and early 60's was the single-slope-integrating converter. One form of this circuit compares a linear reference ramp to the unknown voltage input (see About Integrating Converters and Capacitors). When the ramp potential crosses the unknown input voltage a comparator changes state. The length of time between the start of the ramp and the comparator changing state is proportional to the input voltage. This length of time is measured digitally and presented as the converter output. The inherent strengths of this type of converter are simplicity and high linearity. Although single-slope-integrators were used in early A/Ds and voltmeters their dependence on an integrating capacitor for stability was considered an intolerable weakness. The advent of the dual-slope converter (see About Integrating Converters and Capacitors) solved the problem of integrating capacitor drift with time and temperature by error cancellation techniques. In a dual-slope converter the output represents the ratio of the time required to integrate the unknown voltage for a fixed time and then, using a reference voltage of opposing polarity, measures the amount of time required to get back to the original starting point (see About Integrating Converters and Capacitors). The technique eliminates capacitor drift as an error term.

Limitations of Dual-Slope Converters

The dual-slope converter, and variants on it, have been refined to a point where 16 and 17-bit resolution units are available. A primary detriment to linearity in these converters is a parasitic effect in capacitors called dielectric absorption. Dielectric absorption can be conceptualized as a slight hysteresis of response by the capacitor to charging and discharging. It is influenced by the recent history of current flow in the capacitor, including the magnitude, duration and direction of current flow (see About Integrating Converters and Capacitors).

The nature of operation of dual-slope and related converters requires the instantaneous reversal of current in the integrating capacitor. This puts a substantial burden on the dielectric absorption characteristics of the capacitor. Although dual-slope and related techniques go far to cancel zero and full-scale drifts, residual non-linearity exists due to the effects of dielectric absorption. In addition to non-linearity, dielectric absorption can also cause the converter to give different outputs with a fixed input as the conversion rate is varied over any significant range. Various compensation arrangements are employed to partially offset these effects in present converters. What is really needed for high precision, however, is a conversion scheme which inherently acts to cancel the effects of dielectric absorption, while simultaneously correcting for zero and full-scale drifts.

Overcoming Dual-Slope Limitations

Figure 1 diagrams a converter which meets the requirement noted previously. In this arrangement a microprocessor is used to sequentially switch zero, full-scale reference and EX signals into one input of a comparator. The other comparator input is driven from the ramp output of an operational amplifier integrator. With no convert command applied to the microprocessor, the circuit is at quiescence. In this state the microprocessor sends a continuous, regularly spaced signal to the integrator reset switch. This results in a relatively fixed frequency, period and height ramp at the amplifier's output. This relationship never changes, regardless of the converter's operating state. In addition, the time between ramps is lengthy, resulting in an effective and repeatable reset for the capacitor. When a convert command is applied, the microprocessor switches the comparator input to the zero position, waits for the next available ramp and then measures the amount of time required for the ramp to cross zero volts. This information is stored in memory. The microprocessor then repeats this procedure for the full-scale reference and EX switch positions. With all this information, and the assumption that the integrator ramps are highly linear, the absolute value of EX is determined by the processor according to the following equation.

$$EX = \frac{[C_{EX} - C_{ZERO}]}{[C_{FULL\text{-}SCALE} - C_{ZERO}]} \times K\,\mu V$$

where C = count obtained

and K = a constant, typically 10^7

After this equation is solved and the answer presented as the converter's output, the conversion is complete and the microprocessor is ready to receive the next convert command.

Overcoming Dual-Slope Limitations (Continued)

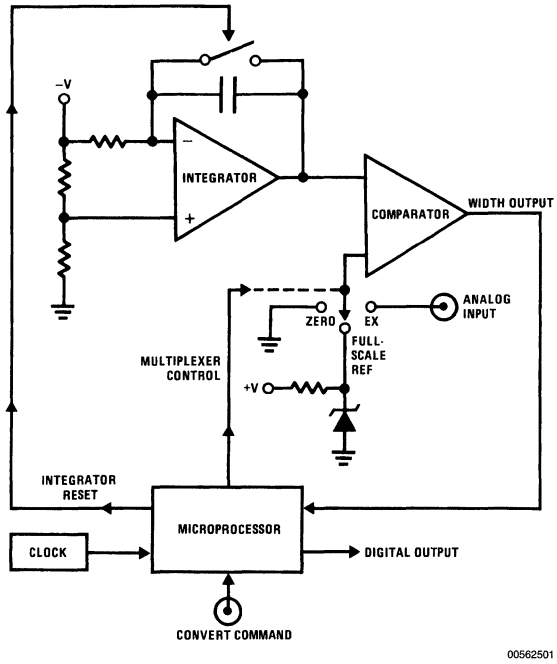


FIGURE 1.

The converter arrangement shares many of the characteristics of a dual-slope type and also provides some significant advantages. The key operating features are as follows:

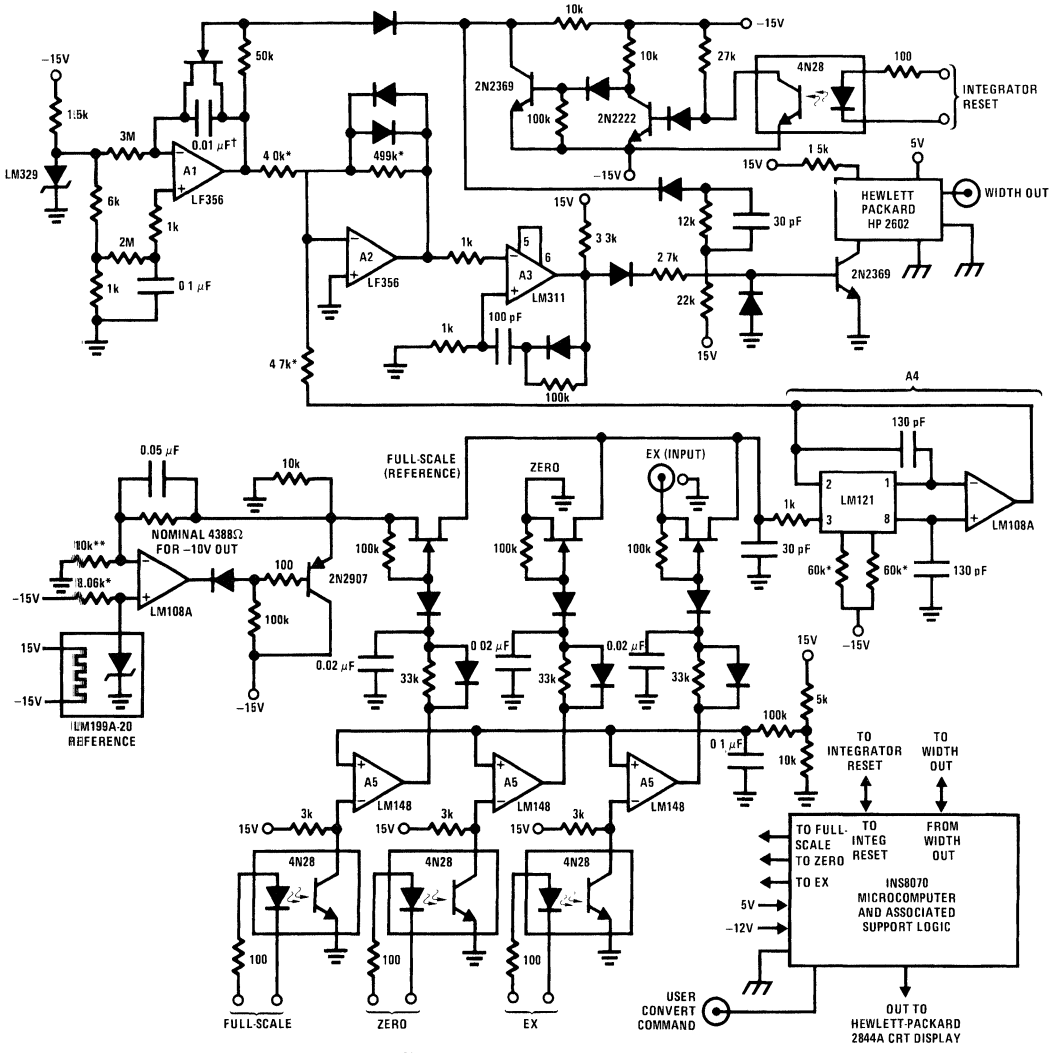
1. It continuously corrects for zero and full-scale drift in all components in the A/D circuit, regardless of changes in time or temperature. The primary limitation on accuracy is the stability of the full-scale reference. The zero signal is derived through conventional high quality grounding technique. These features are similar to a dual-slope converter.
2. Because the integrating capacitor is always charged in a continuous pattern and in the same direction, the dielectric absorption induced error will be relatively small, constant, and will appear as an offset term. This offset term will be removed during the microprocessor's calibration cycle. This feature is unique to this converter and is the key to high linearity.
3. The comparator always sees the ramp voltage approaching the trip point from the same direction and at the same slew rate, regardless of operating conditions. This helps maintain repeatability at the trip point in the face of noise and gain-bandwidth limitations in the comparator.
4. Unlike a dual-slope, this converter has no inherent noise rejection capability. The EX input signal is directly coupled to the comparator input with no filtering. This is a decided disadvantage because most "real world" signals require some smoothing. If a filter was placed at the input substantial time lag due to settling requirements would occur. This is unacceptable because the converter relies on short time intervals between multiplexer states to effectively cancel drift. The solution is to use the microprocessor to filter the signal digitally, using averaging techniques.

Filling out the Blocks

The detailed schematic diagram of the prototype 20-bit linear A/D conveter is shown in *Figure 2.* For clarity, the details of the INS8070 microprocessor and its associated logic are shown in block from. Note that the entire analog section of the converter is fully floating from the digital section to eliminate noise due to digital current spiking and clock noise. The analog and digital circuits communicate via opto-isolators. The full-scale reference for the converter is provided by the LM199A-20-LM108A combination. This circuit, using the components specified, will typically deliver 0.25 ppm/°C performance with drift of several ppm per year. The accuracy to which this reference can be maintained is the primary limitation on absolute accuracy in this converter. The output of this reference is fed to an FET-switched multiplexer which also receives the EX and zero signals. Because all these sources are at low impedance, and only one is switched on at a time, the leakage and ON resistances do not contribute significant error. The A4 combination provides a low bias current unity gain follower with greater than 1,000,00:1 (120 dB) of CMRR, preserving converter linearity. Drifts in this follower are not significant because they will be cancelled out by the microprocessor's calibration cycle. The microprocessor's digital commands to the FET switches are received by the 4N28 opto-isolators. The LM148 quad op-amp (A5) is

Filling out the Blocks (Continued)

used to generate the voltage swing necessary to control the FET switches. The discrete components at each amplifier output are used to generate one-way time delays to give the FET switches break-before-make action. This prevents cross talk between the zero, full-scale reference and EX sources.



Notes

All ⊣⊢ = 2N4393

± 15V for analog circuitry is fully floating

** Vishay S-102 precision resistor

* Metal film resistor—RN60C

† Teflon—Component Research Corp

⊣▶⊢ = 1N4148

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FIGURE 2.

Another FET is used to reset the integrator and is biased by a "brute-force" level shifting-edge speed-up network formed by the 2N2222-2N2369 pair. A 4N28 opto-isolator biases this network when it receives the reset signal from the INS8070

Filling out the Blocks (Continued)

processor. A1, an LF356, has its "+" input biased at about negative 1V, ensuring that the ramp will start far enough below ground to determine a true zero signal.

The requirement for a comparator with 1 ppm (1 LSB at 20 bits=1 ppm) of trip point noise cannot be met by any standard device. At 10V full-scale this is only a 10 µV LSB. The 50 ms-10V ramp's relatively slow slew rate means that the gain-bandwidth and noise characteristics of a standard differential input comparator will cause considerable un- certainty at the trip point. Also, as the common-mode volt- age at which the ramp vs EX crossing occurs changes, the trip point of the comparator will shift, introducing overall non-linearity.

These problems are addressed by the A2-A3 configuration, which forms a high precision comparator. A4's negative output is resistively summed with the positive output of the A1 ramp at A2. A2 normally operates at a low gain due to the diode bounding in its feedback loop. When the currents produced by the ramp potential and A4's output very nearly balance the potential at A2's summing junction will go low enough so that A2 comes out of bound and operates at a gain determined by the 499k feedback resistor (about 100). A2 remains in this high-gain state as long as the ramp and A4 output caused currents are nearly equal. As the ramp continues in its positive going direction the current into A2's summing junction will go to zero and then move positive until the A2 output bounds negative. The output of A2 drives A3, an LM311 comparator which is set up as a zero crossing detector. The components in the positive feedback path at A3 insure a sharp transition. *Figure 3* shows the waveforms of operation. The ramp (a) is shown in highly expanded form. The A2 output (b) can be seen to come cleanly out of diode-bound just before the ramp balances A4's output and then return to bound after the crossing occurs. Waveform (c) is A3's output. The A2 pre-amplifier makes the A3 comparator's job much easier in a number of ways. It amplifies the voltage difference of the two signals to be compared by a factor of 100. This knocks down the effect of A3's input uncertainties. It also produces an apparent 100 fold increase in the ramp slew rate at the trip point. This means A3 spends that much less time with its inputs nearly balanced in an uncertain and noise sensitive condition. Finally, A2 presents the difference signal as a single ended zero crossing signal. This eliminates errors due to changing common-mode voltages that a differential comparator's input would face. Such errors would manifest themselves as overall converter non-linearity.

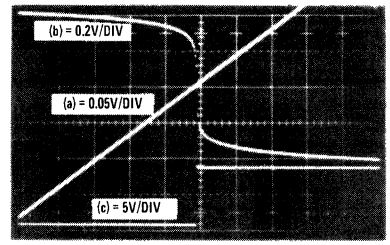


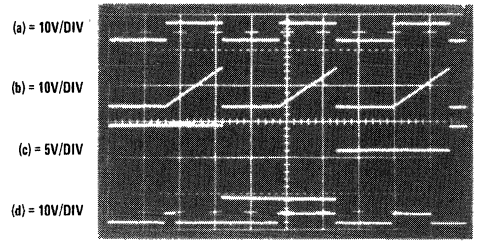
FIGURE 3.

The output of the A3 comparator feeds a 2N2369 transistor, which functions as a level shifter-gate. This transistor gates out that portion of the width output pulse which would be due to the length of the integrator reset pulse. The 2N2369, a low storage capacitance device, provides high speed, even in the relatively slow common emitter configuration. The HP-2602 high speed opto-coupler transmits the width information to the digital circuitry.

Converter Performance and Testing

Figure 4 shows the convert at work. A complete conversion cycle is captured in the photograph. Waveform (a) is the integrator reset out of the INS8070. (b) is the ramp at A1's output. Waveform (c) is the multiplexer output at A4, showing the zero, full-scale reference and EX states. For each state ample time is allowed before the ramp begins. The width output is shown in waveform (d).

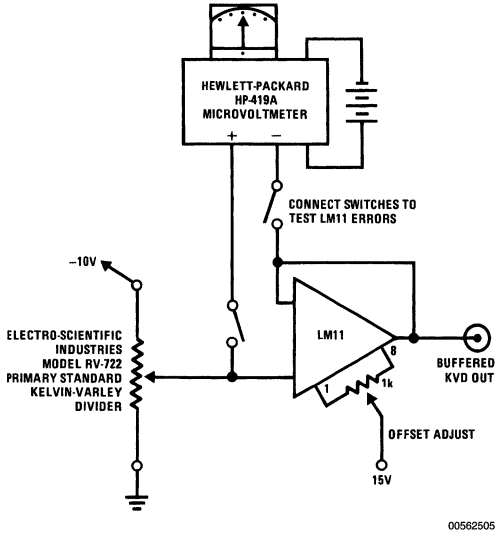
Converter Performance and Testing (Continued)



00562504

FIGURE 4.

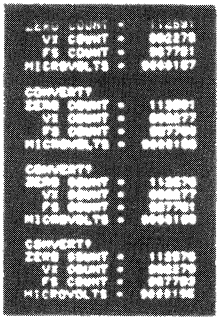
The converter was tested with the arrangement shown in *Figure 5*. The Kelvin-Varley voltage divider, a primary standard type, has a guaranteed linearity of within 1 ppm. The LM11 op amp provides a low bias current, low drift follower to unload the Kelvin divider's output impedance. Because the LM11 gives greater than 120 dB common-mode rejection, its voltage output should track the linearity of the Kelvin divider. To test this the LM11 was adjusted for offset null and a battery-powered µV meter connected between its inputs. 20-bit linear (1 ppm) transfer characteristics were verified by running the Kelvin divider through its range and noting less than 10 µV (1 LSB at 10V full-scale) shift under all conditions. Then, the converter reference was used to drive the Kelvin divider input and the LM11 output to the EX input of the A/D converter.



00562505

FIGURE 5.

A typical output on the Hewlett-Packard 2644A CRT terminal display is shown in *Figure 6*. For each convert command to the INS8070 the number of counts of zero, full-scale reference and EX are shown along with the final computed answer. Note that the final count is computed to one part in ten million and the last digit is insignificant. Note also that the 4 final counts are all within ± 1 ppm . . . despite the fact that they were individually spaced almost 1 hour apart in a varying thermal environment. Linearity of the converter over a 10V range was verified at 10 points by varying the MSB of the Kelvin divider. Although the prototype converter takes 300 ms to complete a cycle, faster speed is attainable by increasing the 20 MHz clock rate. Perhaps more practically, higher conversion speeds at lower resolutions are easily attainable by simply shortening the ramp time. The converter output word length and conversion time may be varied over a wide dynamic range by juggling clock speed and ramp time.



00562506

FIGURE 6.

Although demonstrating a 20-bit converter is useful, there are other applications which do not require this degree of precision. The basic technique is readily adaptable to the practical solution of common transducer and other low-level interface problems. *Figure 7* shows the block diagram of the converter used to generate a 15-bit output directly from a 30 mV full-scale input. In this application the converter input is a differential input amplifier with a nominal gain of 300. Note that the amplifier's offset and gain drift will be cancelled by the microprocessor's calibration loop. The EX signal is the output of the transducer bridge. The full-scale reference signal is derived by measuring across the middle resistor of a string which has the same voltage across it as the nominal bridge output for a given bridge drive level. In this manner, even if the bridge drive varies, the gain of the system remains calibrated by ratiometric error cancellation. The zero signal is derived by shorting both amplifier inputs to the common-mode voltage at the bridge output. This system has been built and has maintained 15-bit accuracy over a 75°F temperature range.

Prospective constructors of this converter are advised that construction technique is extremely critical. In order for the converter to operate properly, the greatest care must be taken in grounding, guarding and shielding techniques. Useful sources of information are listed in the References

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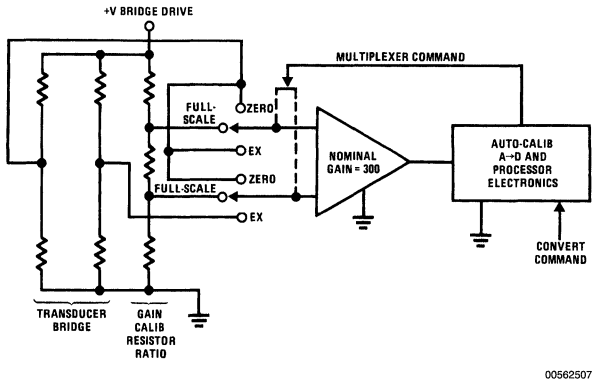


FIGURE 7.

About Integrating Converters and Capacitors

The simplest form of integrating converter is the single-slope type (*Figure 8*). In the single-slope unit shown, a linear reference ramp is compared against the unknown input, EX. When the switch across the integrator capacitor is opened, the ramp begins. The time interval between the opening of the integrator reset switch and the comparator changing state (when E_{RAMP}=EX) is directly proportional to the value of EX. This converter requires that the integrating capacitor and the clock used to measure the time interval be stable over time and temperature . . . a significant drawback under normal circumstances.

The dual-slope integrator (*Figure 9*) overcomes these problems by effectively normalizing the capacitor value and clock rate each time a conversion is made. It does this by integrating the EX input for a pre-determined time. Then, the voltage reference is switched to the integrator input which proceeds to integrate in a negative going direction from the EX slope. The length of time the reference slope requires to get back to zero is proportionate to the EX signal value. These slopes are both established with the same integrating capacitor and measured with the same clock, so both parameters need only be stable over one conversion cycle.

Both of these converters are dependent to varying degrees on capacitor characteristics. The single-slope type requires stability in the capacitor over time and temperature while the dual-slope gets around this limitation. The effects of a phenomenon in capacitors called dielectric absorption, however, have direct impact on dual-slope performance. Dielectric absorption is due to the capacitor dielectric's unwillingness to accept or give up charge instantaneously. It is commonly and simply modeled as a parasitic series RC (*Figure 10*) across the terminals of the main capacitor.

If a charged capacitor is discharged, even through a dead short, some degree of time will be required to remove all of the charge in the parasitic capacitance due to the parasitic series resistance. Conversely, some amount of charge will be absorbed by the parasitic capacitor after a charging of the main capacitor has ceased unless the charge source is maintained for many parasitic RC time constants. Various dielectrics offer differing performance with respect to dielectric absorption. Teflon, polystyrene and polypropylene are quite good, while paper, mylar and glass are relatively poor. Electrolytics are by far the worst offenders. Anyone who has received a shock after discharging a high voltage electrolytic in a television set has experienced the effect of dielectric absorption.

About Integrating Converters and Capacitors (Continued)

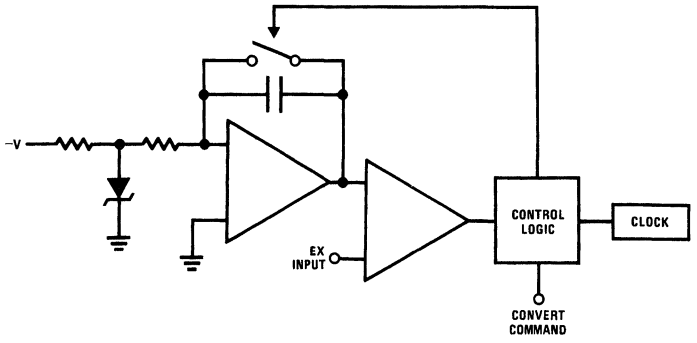


FIGURE 8.

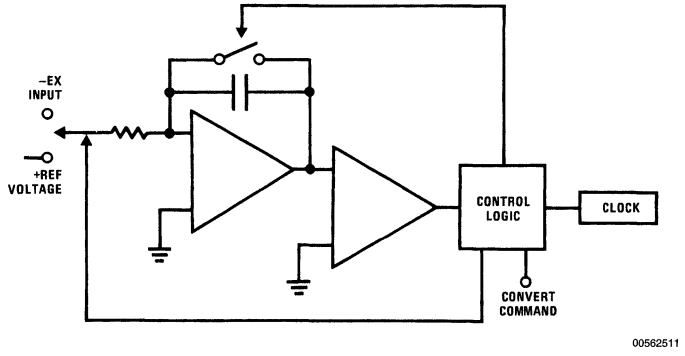


FIGURE 9.

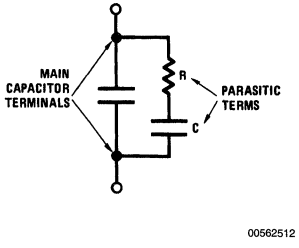


FIGURE 10.

CMOS A/D Converter Interfaces Easily with Many Microprocessors

National Semiconductor
Application Note 274
Larry Wakeman

With a span accommodation down to 180 mV, this 8-bit unit can also replace a 12-bit analog-to-digital device in some applications

To help meet the rising demand for easier interfacing between analog-to-digital converters and microprocessors, the complementary MOS, 8-bit ADC0801-05 has been designed to accommodate almost all of today's popular microprocessors. It requires only a single 5V supply and is low power to boot.

Housed in a 20-pin dual-in-line package, the successive approximation device includes a Schmitt trigger circuit that allows it to be driven from a system clock, as well as an external RC network. At a clock frequency of 640 kHz, conversion time is 100 μs. What's more, its guaranteed linearity error of ±¼ least significant bit (typically ±1/16 LSB) can encode an analog signal span as small as 180 mV—a performance that allows it to replace 9, 10, and even 12-bit converters in many applications.

Constantly decreasing converter prices raise the comparative cost of the interface electronics and increase the demand for simplicity of interfacing. The growing emphasis on simpler systems for higher levels of reliability has also pushed this demand, as has a trend toward lower levels of power dissipation. And with the success of the 5V power supply standard of logic circuits, linear circuits have been pressed for 5V operation. Supporting the ADC0801-05 A/D converter are such special operational amplifiers as the LM358 dual and the LM324 and LM3900 quad op amps that run off 5V supplies, also useful are voltage comparators such as the LM393 dual and LM339 quad devices. Perhaps the most versatile of such 5V linear devices is the LM392, comprising an op amp and a comparator.

More Complications

Complicating the interfacing are the ever higher levels of resolution in monolithic converters, with 8 and 10-bit types readily available and 12-bit devices ready to emerge soon. Yet, despite their greater resolution, 10 and 12-bit monolithic A/D converters are not only more expensive than 8-bit designs, but also require more careful attention to system noise problems and management of grounding.

For simple interfacing, an A/D converter must operate directly with the signals available on a microprocessor control bus. The converter is generally given an address that can be mapped into memory or input/output space, depending on the type of microprocessor employed. On 6800 microprocessors and their derivatives, no special input/output addressing or strobes are available, so the converter must appear as a memory location to these processors. Z80® microprocessors, on the other hand, not only provide special I/O interfacing, but also automatically insert a wait state during I/O selection to increase the width of the read and write strobe signals. This eases interface requirements considerably, since slower I/O devices can operate with much faster microprocessor units. The automatic wait state for I/O devices will loom larger in importance as the next generation of higher speed microprocessors evolves.

Compatibility Criteria Differ

Microprocessor compatibility has a wide range of meanings—at least according to the various converter data sheets. True compatibility, however, involves meeting electrical specifications like proper logic voltage levels with adequate loading capability. For example, true TTL compatibility means the ability to maintain a 0.4V low potential (or less) at the A/D converter logic outputs while sinking 1.6 mA of current. And the high state must be maintained at a minimum of 2.4V while supplying at least 360 μA.

Furthermore, all interface protocols must be met. This not only means operating with the proper signals, but also meeting all necessary timing requirements, so the converter must have valid data on the microprocessor bus within the access time of the memory system with which it happens to be working.

The protocols for interfacing are not at all standardized. Some A/D converters make use of the standard chip select signal ($\overline{CS}$) to start a conversion. But decoding voltage glitches can cause an A/D converter to begin conversion when it is not desirable. Both the standard $\overline{CS}$ signal and a write strobe signal ($\overline{WR}$) must therefore be used, so that the former signal qualifies the latter and prevents unwanted conversions due to address decoding glitches. Care must also be taken when using some A/D converters that are designed to act as bus controllers, problems can arise when the central processor is not in control of the bus.

Different Standards

The 8080 and 6800 microprocessors (and their derivatives) use different control bus standards. Microprocessors based on the 8080, for example, make use of read and write strobe signals to specify the operation (read or write) requested. Working with these microprocessors, A/D converters start the conversion cycle upon the microprocessor's issuance of a chip select signal (decoded from the address bus) and a write strobe signal. At the end of conversion (EOC), the converter issues an EOC signal. When dealing with older A/D converters where the EOC signal is typically low during the conversion process and high at the end of it, microprocessors have difficulty because the EOC signal is not available on the data bus. Furthermore, the EOC signal does not reset when the converter is serviced by the central processing unit (that is, when data has been read).

Complications can also occur when microprocessors interface with older A/D devices during read operations. For proper interfacing, such converters must have valid data on the bus within the memory access time.

Interfacing requirements differ for 6800-type microprocessors, like the 6502 and 68000, which use read/write (R/$\overline{W}$) control lines instead of read and write strobe signals and obtain timing information from the system clock signal. In addition, they include a valid memory address signal to qualify the address that is placed on the bus. Such features make interfacing for these microprocessors different from that for earlier 8080 types.

Different Standards (Continued)

For an A/D converter to be most useful in a microprocessor-based system, it must have such desirable analog features as differential inputs, and it should adjust to accommodate various analog input signal ranges. The ADC0801-05 offers differential analog inputs, but it is the converter's span accommodation that allows many unusual and useful analog applications.

The availability of differential analog voltage inputs eliminates the problem of poor analog grounds, since both inputs can be connected directly across the analog signal source.

The negative (normally grounded) analog input lead can be referenced to any desired DC offset voltage to accommodate an input signal range that does not swing down to ground. A DC offset can thus be used at this input to cause a digital output of all 0s at any desired input voltage.

Flexible Span

Finally, the ability to accommodate an arbitrary span or input dynamic voltage range is desirable in an A/D converter. This can easily be achieved in the ADC0801-05 by selecting the magnitude of the converter's reference input.

An example might be to permit an analog input voltage range of 0.5V to 3.5V. This is accomplished by tying the converter's negative input lead to a 0.5 V_{DC} offset voltage and supplying a reference voltage that is equal to half the 3V span. This application provides the 00 output code for V_{IN} = 0.5 V_{DC} and the FF output code for V_{IN} = 3.5 V_{DC}.

In many applications (such as weighing cans on a production line), 14, or even 16-bit converters are often called upon for the needed high levels of resolution. For those reduced-span applications, an 8-bit A/D converter can be used instead—at considerable savings.

A Sampled-Data Input

The ADC0801-05 makes use of a sampled-data comparator. Sampled-data circuits cancel the offset voltage, provide essentially temperature-independent performance, and cancel low frequency MOS 1/f noise. They do, however, provide some differences in application, since there is an input stray capacitance to ground, as shown in *Figure 1.*

When switch S1 is closed, stray input capacitance, C_{IN}, is charged to the input analog potential, V_{ANALOG}. Note that with a stray capacitance of approximately 12 pF and a 5 kΩ MOS switch resistance, the time constant, τ, is only 60 ns. Thus, C_{IN} becomes charged to the necessary accuracy level (within ±¼ LSB) in 6.9τ, or about 0.4 μs. Since the input switches are operating at one eighth the input clock frequency of 640 kHz, there is ample time for C_{IN} to settle, as comparisons are made only at the end of the clock period. Note that the switch at the (–) analog input discharges the stray capacitance; this event causes input displacement currents to flow.

Input bypass capacitors, when placed directly at the analog inputs, cause full-scale errors, since they average the current which will flow through the source resistance of the analog input signal generator. Input capacitors are not required; but if they are used, a full-scale adjustment will eliminate any system errors.

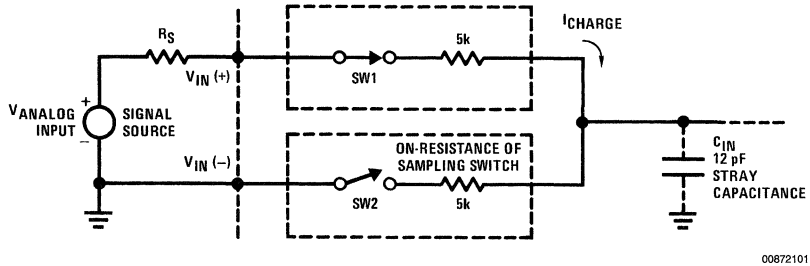


FIGURE 1. Equivalent. Because it has a sampled-data comparator input, the 8-bit ADC0801-05 monolithic analog-to-digital converter looks capacitive to an input signal source. The sampling switches operate at one eighth the rate of the clock frequency.

The ADC0801-05 monolithic 8-bit CMOS A/D converter can be operated with a wide range of $V_{REF}/2$ voltages that facilitates its use in many different circuit applications. Inexpensive ratiometric transducers, such as potentiometers, can be tied across the converter's 5V supply voltage with the wiper fed directly to the converter's V_{IN}+ input pin. The $V_{REF}/2$ pin, which will now bias at 2.5V, can be tied to a second potentiometer that is also hooked across the supply voltage to provide a full-scale adjustment.

When the $V_{REF}/2$ is grounded, the converter then functions as a comparator, yielding a digital output of all 1s when V_{IN}+ is greater than V_{IN}–, and of all 0s when V_{IN}+ is less than V_{IN}–. The $V_{REF}/2$ feature is also useful for low level analog voltage systems where an operational amplifier is normally used to boost the input signal prior to digitization. In a circuit with an analog input voltage of 250 mV maximum, for example, the signal can be fed directly to the A/D device, saving the cost of the amplifier. The $V_{REF}/2$ pin would thus be biased at 125 mV.

Careful Grounding

A minor drawback is that this extra analog resolution leaves the circuit more susceptible to noise, and the $V_{REF}/2$ voltage requires a low initial tolerance and must be stable over temperature changes. Grounding problems become more critical and careful grounding is a must.

The ADC0801-05 can also be used as a logarithmic converter to extend the input voltage dynamic range to cover three decades. Three input logging circuits (*Figure 2*) are

Careful Grounding (Continued)

provided by the NPN transistors in the feedback loops of operational amplifiers. With these at the same temperature (all three on a common chip), there are no thermal problems with this circuit. To keep costs at their lowest, the three transistors in the LM389 audio amplifier IC can be used.

The fourth operational amplifier in *Figure 2* is used to supply the proper $V_{REF}/2$ voltage to the A/D converter. Its DC output voltage is half that of the logarithmically compressed analog input voltage span.

Offset Adjusting

Yet another application for the ADC0801-05 is in automatically adjusting the offset voltage of an op amp under microprocessor control. This is useful in transducer bridge networks where a pair of amplifiers is normally used to amplify the differential signal. Such an output signal can be fed directly to the A/D converter's inputs without requiring a more costly instrumentation amplifier. The bridge network's arms will thus be biased at approximately $V_{CC}/2$.

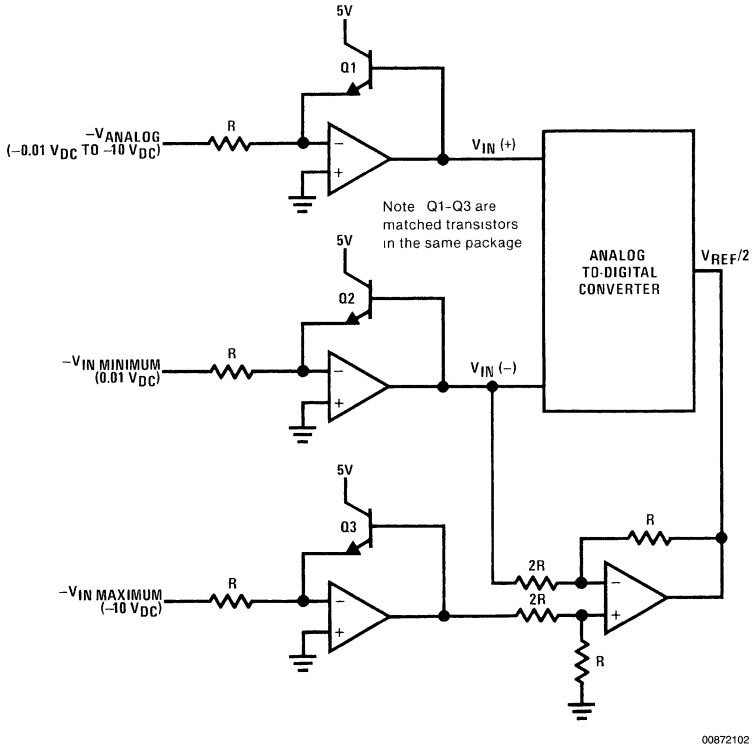


FIGURE 2. Logarithmic. The ADC0801-05 monolithic A/D converter's $V_{REF}/2$ pin allows its use as a three-decade logarithmic circuit. The three NPN transistors in the feedback loops of the operational amplifiers give better accuracy with changing temperature than the diodes normally used.

Figure 3 shows such a circuit, where the microprocessor takes the digital output of the A/D device and automatically adjusts the output voltage of operational amplifier 2. This amplifier is used to isolate the bridge network from the offset adjustment circuit. The INS8255 programmable peripheral interface controls the offset voltage adjustment and analog switches 1 and 2. The CMOS buffer provides ideal analog level swings of either 0V or 5V to the binary resistor network. The binary resistor network extracts and injects a current from and into op amp 3, causing a small voltage drop across R_S. This corrects for offset voltage that is introduced anywhere in the system.

Auto Adjustment

Electrically actuated switches 1 and 2 allow the automatic adjustment of the offset voltage. It should be noted that op amp 1 is referenced to one side of the bridge network in order to cancel any common-mode offset voltage effects.

The A/D converter acts as a high gain comparator because a 0V $V_{REF}/2$ is provided by the voltage follower (amplifier 4) and switch 1 circuits. This allows the microprocessor to perform a successive approximation routine to null the offset

Auto Adjustment (Continued)

voltage of the system. Resolution is thus considerably better than the normal + 1LSB obtainable with a conventional A/D converter.

The ADC0801-05 combines linear and digital features in an A/D converter that is flexible and easy to tie to microprocessor-based systems. The benefits of a sampled-data comparator and an unusual ladder now make an A/D converter actually easier to fabricate than a digital-to-analog converter.

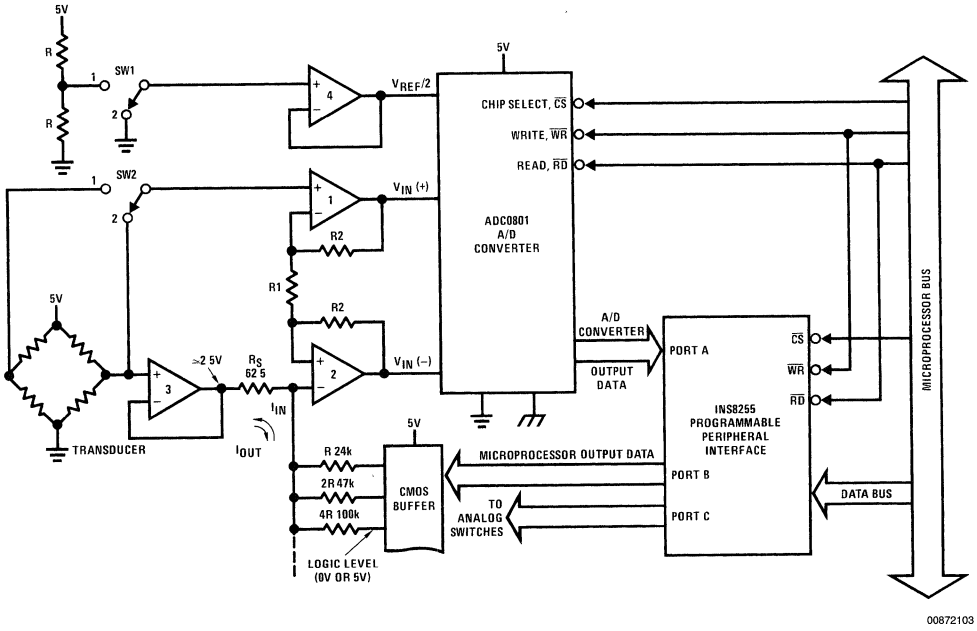


FIGURE 3. Automatic. Adjusting the offset voltage of a differential amplifier pair in a transcript bridge network can be done automatically. A microprocessor provides this adjustment through a programmable peripheral interface and a buffer integrated circuit.

Single-Supply Applications of CMOS MICRODACs

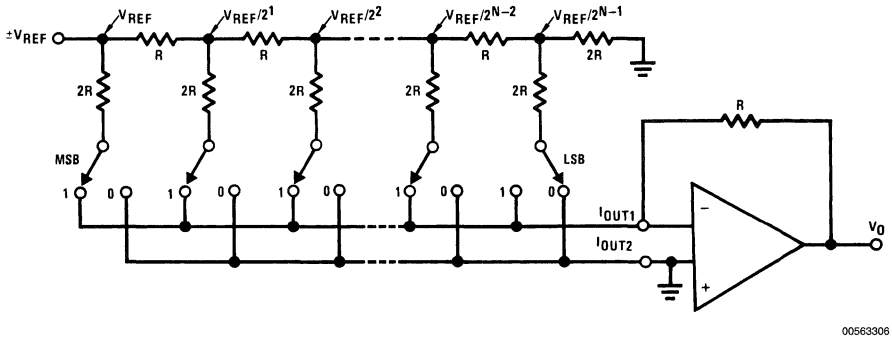
National Semiconductor
Application Note 284
Tim Regan

CMOS data acquisition and conversion products are becoming the ideal choice for microprocessor controlled analog systems. The use of CMOS allows the addition of more digital logic functionality on to the same die as the analog circuitry to minimize external parts requirements. The inherently low power consumption is also a big factor for battery operation and low heat generation in large scale systems.

National's MICRODAC™ family of 8, 10 and 12-bit D to A converters all feature on-chip data latches to permit direct interface to 8 or 16-bit data busses. These devices were designed to provide the most versatility from an analog standpoint. By utilizing a current switching R-2R ladder network (*Figure 1*), the applied reference voltage can be either a stable DC voltage or an AC voltage within the wide range of ±10V. However, output linearity requires that the two current output terminals be biased to 0V. This is accomplished by using an external op amp to serve as a current-to-voltage converter. Negative feedback via the feedback resistor included in the DAC keeps the I_{OUT1} terminal at a virtual ground potential A drawback to this technique is that the output amplifier inverts and outputs a voltage of the opposite polarity of the applied reference. This then requires the output amplifier to have a negative supply voltage if the reference were positive. To operate with only a single-supply by biasing the ground pin of the DAC and the inputs of the op amp to ½ the supply does not work, as the digital inputs are no longer TTL compatible.

All hope is not lost, however, if single-supply operation is essential. By taking a somewhat backwards view of the DAC ladder network, only a single positive supply is necessary. In *Figure 2* the R-2R ladder network is used to switch voltages rather than currents.[1] By applying the reference to the normal current output terminal (I_{OUT1}) and grounding I_{OUT2} the voltage at the reference terminal will be a fraction of the reference voltage and a function of the applied digital input code.

There are two important considerations when using this voltage-switching approach. The applied reference voltage must be positive since there are internal parasitic diodes from the I_{OUT} terminals to ground which would turn on if the reference were to be negative. This, of course, is of no concern with single-supply applications. There is also a dependence of converter linearity and gain error on the voltage difference between the DAC's V_{CC} supply and the applied reference voltage. This is a result of the voltage drive requirement of the CMOS ladder switches. To ensure that all of the switches can turn on sufficiently (so as not to add significant resistance to any leg of the ladder and thereby introduce additional linearity and gain errors) an 8-bit DAC should not have a reference greater than 5V and the V_{CC} supply should be at least 9V more positive than the reference. This would keep linearity and gain error degradation less than 0.1%. A 10-bit DAC is a bit more stringent. For a 0.005% or less error degradation, the reference should be less than 3 V_{DC} and V_{CC} should be 10V more positive. The typical effects of bringing V_{REF} and V_{CC} closer together, are well as temperature performance, are shown graphically in *Figure 3* for the 8-bit DAC0830 series



N = Number of bits of resolution

FIGURE 1. The Standard Current-Switching R-2R Ladder Network

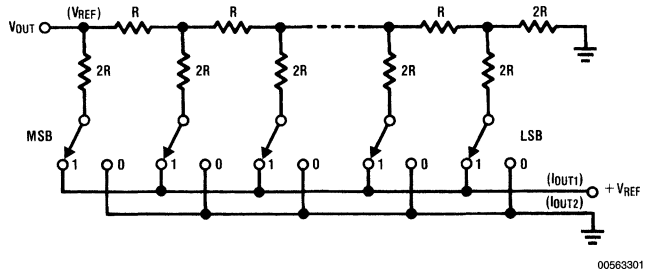


FIGURE 2. Operating the Ladder "Backwards" to Serve as a Voltage-Switching Network

Since the output is now a voltage rather than a current, an output op amp is not necessarily required, but the DAC's output impedance is fairly high (equal to its specified reference input resistance of 10k to 20k), so an op amp may be required for buffering purposes. *Figure 4* shows a single-supply DAC with an output amplifier providing buffering and gain for a more useful 0V to 10V output from a 2.5V reference. The LM336 reference diode is biased through the internal feedback resistor between the I_{OUT1} pin and the R_{fb} pin. The zero-code output voltage is limited by the lower output saturation voltage of the LM358 op amp. The 2k pull-down load resistor helps to reduce this voltage to 10 mV or ¼ of an output LSB. Even with a 15V DAC supply, the digital inputs remain T^2L compatible.

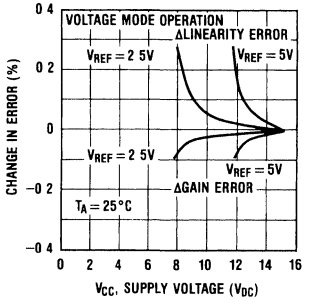
Closer inspection of *Figure 2* shows that both I_{OUT1} and I_{OUT2} drive the ladder network in an identical manner. Each leg is connected to either I_{OUT1} or I_{OUT2} as controlled by the logic state of each digital input. If each I_{OUT} terminal is biased to separate reference potentials, the circuit of *Figure 5* results. This is a single-supply DAC with an adjustable zero-code output offset voltage and adjustable output span to reserve the full resolution of the DAC for a range of voltages other than 0V to full-scale. An important point to note is that for an all ones code applied, only the voltage at I_{OUT1} is connected to the ladder and sets the output to 255/256 times the voltage of I_{OUT1}. With an all zeros code applied, only the voltage at I_{OUT2} drives the ladder, setting the output to 255/256 times this voltage. This non-interaction of the two inputs at the end-points makes calibration a breeze. The incremental analog output steps are automatically set to $(V_{MAX}-V_{MIN})/256$.

The buffers at the two reference inputs in *Figure 5* isolate the code-dependent resistance to ground at I_{OUT1} and I_{OUT2} from the resistive string used to set V_{MAX} and V_{MIN}. The output responds in accordance to the following expression.

$$V_{OUT} = D/256\ (V_{MAX} - V_{MIN}) + 255/256\ V_{MIN} \quad (1)$$

Where D is the decimal equivalent of the 8-bit binary control word.

Gain and Linearity Error Variation vs Supply Voltage



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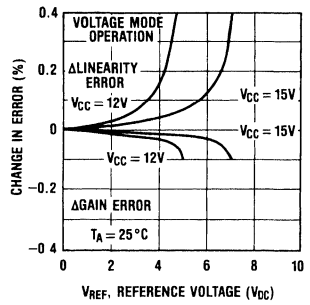
Gain and Linearity Error Variation vs Reference Voltage



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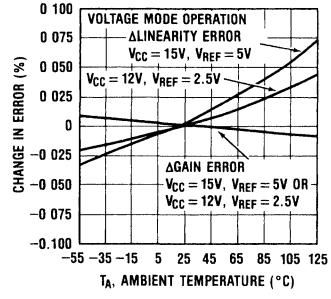
Gain and Linearity Error Variation vs Temperature



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Note: For these curves, V_{REF} is the voltage applied to the I_{OUT1} terminal and I_{OUT2} is grounded.

FIGURE 3. The Effects of Bringing the V_{CC} Supply and V_{REF} Closer Together and Temperature Performance Using the DAC in the Voltage-Switching Mode

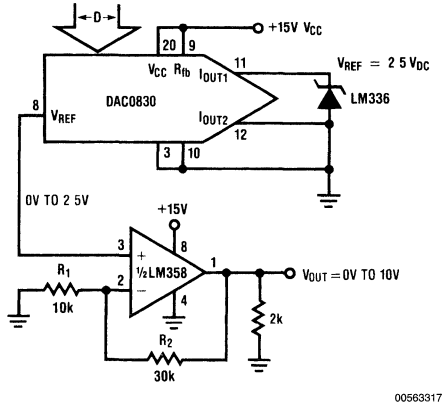

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FIGURE 4. Obtaining 0V to 10V Output from a 2.5V Reference

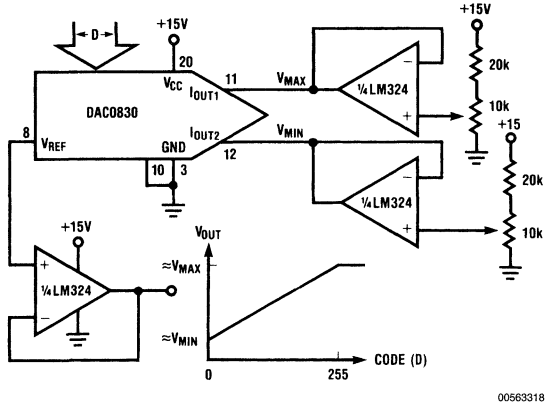

FIGURE 5. A Single-Supply DAC with Level Shift and Span Adjustable Output

A common requirement of single-supply systems is that the outputs of signal-conditioning amplifiers must be DC biased, typically to ½ of the V_{CC} supply, to provide maximum unclipped AC signal swing. The circuit of *Figure 6* shows how this dual-input voltage-switching DAC configuration can allow the digital input code to control the attenuation of an AC signal without significantly affecting the DC biasing level. If the voltage at I_{OUT2} is set to the DC level of the voltage at I_{OUT1}, then the term in *Equation (1)* which is controlled by the digital input code, D, reduces to just the AC signal at I_{OUT1}. The DC level at the output is 255/256 times the DC level at the input.

The circuit of *Figure 7* combines the advantages of low power consumption of the CMOS MICRODACs together with the non-interactive zero and full-scale adjustability of this voltage-switching technique. This circuit is an isolated 4 mA-20 mA current loop controller where the DAC sets the amount of current that flows through the loop, yet receives its own power from the very same loop.

Digital control and isolation are provided by a single optoisolator and a CMOS counter. The controlling processor must generate a clock and keep track of the number of clock pulses issued to the circuit to know what the loop current is at any time. On power-up the counter is reset to all zeros to give the processor a starting point, as well as to inherently provide a calibration point. When calibrating, potentiometer P1 would be set for the zero-code loop current of 4 mA. The processor would then issue exactly 255 clock pulses to the opto-isolator. Potentiometer P2 can then adjust the full-scale current value to 19.92 mA. If one more clock pulse is issued, the DAC input code returns to all zeros and the previously set value of 4 mA will flow, as this setting was unaffected by the full-scale adjustment.

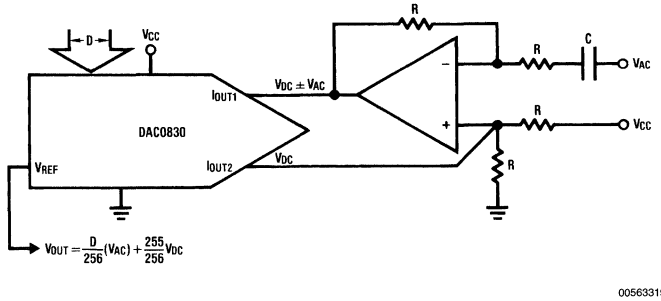

FIGURE 6. Single-Supply DAC where the Digital Input Word Affects the Attenuation of an AC Signal without Significantly Altering its DC Biasing Level

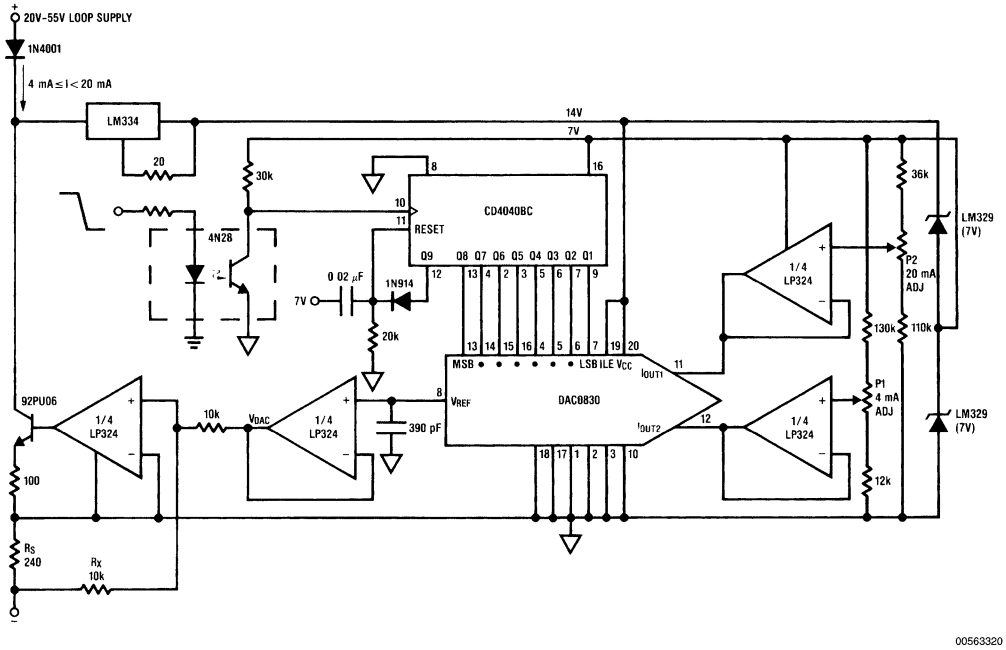

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FIGURE 7. Easily Calibrated, Isolated 4 mA-20 mA Current Loop Controller

The NPN emitter-follower will conduct whatever level of current necessary to keep the voltage across resistor R_S equal to the voltage across resistor R_X. This voltage is equal to the output voltage at the V_{REF} pin of the DAC which can be determined from *Equation (1)*. The actual loop current is:

$$I_{LOOP}=V_{DAC}(1/R_S+1/R_X) \qquad (2)$$

The second LM329 reference diode is used to bias the DAC V_{CC} supply higher than the voltages at I_{OUT1} and I_{OUT2} to preserve linearity.

Finally, what if a D to A function is required, but only a single 5V supply is available and minimal supply current is a primary concern (battery powered instrumentation is a good example)? The voltage-switching techniques previously described are not suitable because not enough voltage is available to properly bias the DAC. A CMOS DAC is still attractive for its low supply current requirements and if it can be operated in the standard current switching configuration, a single 5V supply is sufficient. But how about the voltage inversion and the requirement for negative supply potential?

By taking advantage of an age-old technique of clocking a diode-capacitor network connected as a DC to DC voltage inverter, a low current negative supply can be generated. In the circuit of *Figure 8*, 2 diodes and 2 capacitors are clocked by a CMOS Schmitt trigger oscillator and connected in such a fashion as to generate a −3.8V supply potential. This negative supply is used only to bias a low current LM385-2.5V reference diode to provide the DAC with a stable negative reference. Now the inversion of the output current-to-voltage converter will generate a positive output ranging from 0V to 2.5V as a function of the digital input code.

The amount of ripple that may appear at the reference input is a function of the dynamic impedance of the LM385, the clock frequency and the size of the switching capacitors. For the component values shown, the clock frequency is approximately 1 kHz and the ripple on the reference is 7 mV peak to peak. This ripple is cleanly filtered by the bypass cap around the feedback resistor of the output amplifier. The output op amp is part of a new low power quad, the LP324, which is ideal for its ability to common-mode to ground on the inputs and swing very close to ground at its output. If an extra CMOS Schmitt inverter is not readily available, the oscillator function can be implemented with another of the amplifiers in the op amp package. The total supply current of this single-supply DAC is on the order of 1.5 mA with no output load.

With this technique even the 12-bit DAC1230 can be used with no linearity degradation which would be apparent in the voltage-switching techniques.

Reference

1. Sevastopoulos, N.; Cecil, J.; and Fredericksen, T., *"An Unusual Circuit Configuration Improves CMOS-MDAC Performance"*, EDN Magazine, March 5, 1979, pg. 77.

Reference (Continued)

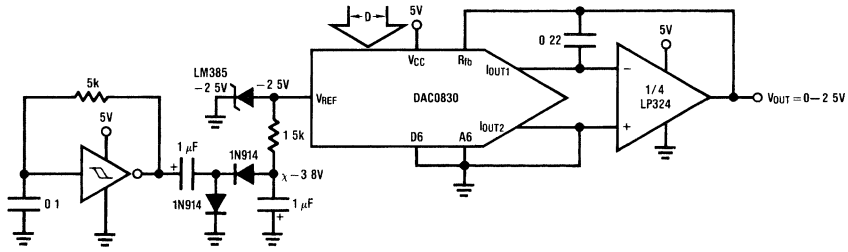


FIGURE 8. Single 5V Supply, 8-Bit CMOS DAC

LM34/LM35 Precision Monolithic Temperature Sensors

National Semiconductor
Application Note 460
Tim Regan

Introduction

Most commonly-used electrical temperature sensors are difficult to apply. For example, thermocouples have low output levels and require cold junction compensation. Thermistors are nonlinear. In addition, the outputs of these sensors are not linearly proportional to any temperature scale. Early monolithic sensors, such as the LM3911, LM134 and LM135, overcame many of these difficulties, but their outputs are related to the Kelvin temperature scale rather than the more popular Celsius and Fahrenheit scales. Fortunately, in 1983 two I.C.'s, the LM34 Precision Fahrenheit Temperature Sensor and the LM35 Precision Celsius Temperature Sensor, were introduced. This application note will discuss the LM34, but with the proper scaling factors can easily be adapted to the LM35.

The LM34 has an output of 10 mV/°F with a typical nonlinearity of only ±0.35°F over a −50 to +300°F temperature range, and is accurate to within ±0.4°F typically at room temperature (77°F). The LM34's low output impedance and linear output characteristic make interfacing with readout or control circuitry easy. An inherent strength of the LM34 over other currently available temperature sensors is that it is not as susceptible to large errors in its output from low level leakage currents. For instance, many monolithic temperature sensors have an output of only 1 µA/°K. This leads to a 1°K error for only 1 µ-Ampere of leakage current. On the other hand, the LM34 may be operated as a current mode device providing 20 µA/°F of output current. The same 1 µA of leakage current will cause an error in the LM34's output of only 0.05°F (or 0.03°K after scaling).

Low cost and high accuracy are maintained by performing trimming and calibration procedures at the wafer level. The device may be operated with either single or dual supplies. With less than 70 µA of current drain, the LM34 has very little self-heating (less than 0.2°F in still air), and comes in a TO-46 metal can package, a SO-8 small outline package and a TO-92 plastic package.

Forerunners to the LM34

The making of a temperature sensor depends upon exploiting a property of some material which is a changing function of temperature. Preferably this function will be a linear function for the temperature range of interest. The base-emitter voltage (V_{BE}) of a silicon NPN transistor has such a temperature dependence over small ranges of temperature.

Unfortunately, the value of V_{BE} varies over a production range and thus the room temperature calibration error is not specified nor guaranteeable in production. Additionally, the temperature coefficient of about −2 mV/°C also has a tolerance and spread in production. Furthermore, while the tempo may appear linear over a narrow temperature, there is a definite nonlinearity as large as 3°C or 4°C over a full −55°C to +150°C temperature range.

Another approach has been developed where the difference in the base-emitter voltage of two transistors operated at different current densities is used as a measure of temperature. It can be shown that when two transistors, Q1 and Q2, are operated at different emitter current densities, the difference in their base-emitter voltages, ΔV_{BE}, is

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = \frac{kT}{q} \ln \frac{(J_{E1})}{J_{E2}} \quad (1)$$

where k is Boltzman's constant, q is the charge on an electron, T is absolute temperature in degrees Kelvin and J_{E1} and J_{E2} are the emitter current densities of Q1 and Q2 respectively. A circuit realizing this function is shown in *Figure 1.*

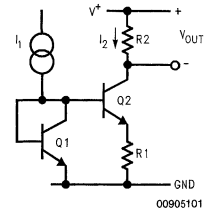


FIGURE 1.

Equation (1) implies that as long as the ratio of I_{E1} to I_{E2} is held constant, then ΔV_{BE} is a linear function of temperature (this is not exactly true over the whole temperature range, but a correction circuit for the nonlinearity of V_{BE1} and V_{BE2} will be discussed later). The linearity of this ΔV_{BE} with temperature is good enough that most of today's monolithic temperature sensors are based upon this principle.

An early monolithic temperature sensor using the above principle is shown in *Figure 2.* This sensor outputs a voltage which is related to the absolute temperature scale by a factor of 10 mV per degree Kelvin and is known as the LM135. The circuit has a ΔV_{BE} of approximately

$$(0.2 \text{ mV/°K}) \times (T)$$

developed across resistor R. The amplifier acts as a servo to enforce this condition. The ΔV_{BE} appearing across resistor R is then multiplied by the resistor string consisting of R and the 26R and 23R resistors for an output voltage of (10 mV/°K) x (T). The resistor marked 100R is used for offset trimming. This circuit has been very popular, but such Kelvin temperature sensors have the disadvantage of a large constant output voltage of 2.73V which must be subtracted for use as a Celsius-scaled temperature sensor.

Forerunners to the LM34 (Continued)

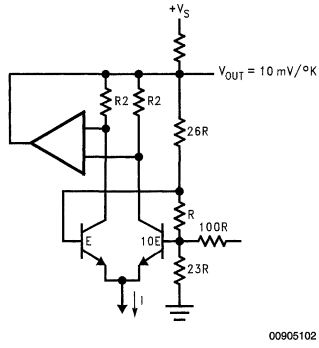


FIGURE 2.

Various sensors have been developed with outputs which are proportional to the Celsius temperature scale, but are rather expensive and difficult to calibrate due to the large number of calibration steps which have to be performed. Gerard C.M. Meijer[4] has developed a circuit which claims to be inherently calibrated if properly trimmed at any one temperature. The basic structure of Meijer's circuit is shown in *Figure 3*. The output current has a temperature coefficient of 1 µA/°C. The circuit works as follows: a current which is proportional to absolute temperature, I_{PTAT}, is generated by a current source. Then a current which is proportional to the V_{BE} drop of transistor Q4 is subtracted from I_{PTAT} to get the output current, I_O. Transistor Q4 is biased by means of a PNP current mirror and transistor Q3, which is used as a feedback amplifier. In Meijer's paper it is claimed that the calibration procedure is straightforward and can be performed at any temperature by trimming resistor R4 to adjust the sensitivity, dI_O/dT, and then trimming a resistor in the PTAT current source to give the correct value of output current for the temperature at which the calibration is being performed.

Meijer's Celsius temperature sensor has problems due to its small output signal (i.e., the output may have errors caused by leakage currents). Another problem is the trim scheme requires the trimming of two resistors to a very high degree of accuracy. To overcome these problems the circuits of *Figure 4* (an LM34 Fahrenheit temperature sensor) and *Figure 5* (an LM35 Celsius temperature sensor) have been developed to have a simpler calibration procedure, an output voltage with a relatively large tempco, and a curvature compensation circuit to account for the non-linear characteristics of V_{BE} versus temperature. Basically, what happens is transistors Q1 and Q2 develop a ΔV_{BE} across resistor R1. This voltage is multiplied across resistor nR1. Thus at the non-inverting input of amplifier A2 is a voltage two diode drops below the voltage across resistor nR1. This voltage is then amplified by amplifier A2 to give an output proportional to whichever temperature scale is desired by a factor of 10 mV per degree.

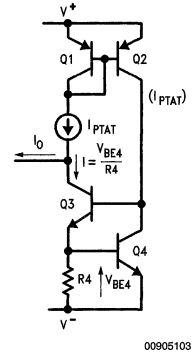


FIGURE 3.

Circuit Operation

Since the two circuits are very similar, only the LM34 Fahrenheit temperature sensor will be discussed in greater detail. The circuit operates as follows:

Transistor Q1 has 10 times the emitter area of transistor Q2, and therefore, one-tenth the current density. From *Figure 4*, it is seen that the difference in the current densities of Q1 and Q2 will develop a voltage which is proportional to absolute temperature across resistor R_1. At 77°F this voltage will be 60 mV. As in the Kelvin temperature sensor, an amplifier, A1, is used to insure that this is the case by servoing the base of transistor Q1 to a voltage level, V_{PTAT}, of ΔV_{BE} x n. The value of n will be trimmed during calibration of the device to give the correct output for any temperature.

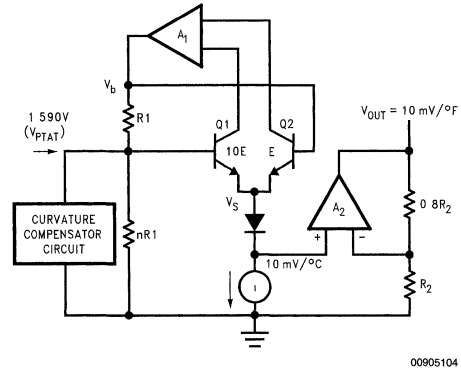


FIGURE 4.

Circuit Operation (Continued)

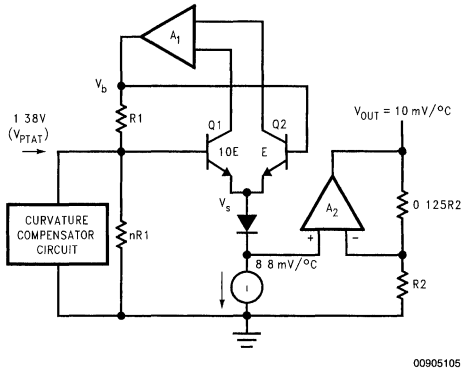


FIGURE 5.

For purposes of discussion, suppose that a value of V_{PTAT} equal to 1.59V will give a correct output of 770 mV at 77°F. Then n will be equal to $V_{PTAT}/\Delta V_{BE}$ or 1.59V/60 mV = 26.5, and V_{PTAT} will have a temperature coefficient (tempco) of:

$$\frac{nk}{q} \ln \frac{I_1}{I_2} = 5.3 \text{ mV/°C}.$$

Subtracting two diode drops of 581 mV (at 77°F) with tempcos of −2.35 mV/°C each, will result in a voltage of 428 mV with a tempco of 10 mV/°C at the non-inverting input of amplifier A2. As shown, amplifier A2 has a gain of 1.8 which provides the necessary conversion to 770 mV at 77°F (25°C). A further example would be if the temperature were 32°F (0°C), then the voltage at the input of A2 would be 428 mV−(10 mV/°C) (25°C) = 0.178, which would give V_{OUT} = (0.178) (1.8) = 320 mV—the correct value for this temperature.

Easy Calibration Procedure

The circuit may be calibrated at any temperature by adjusting the value of the resistor ratio factor n. Note that the value of n is dependent on the actual value of the voltage drop from the two diodes since n is adjusted to give a correct value of voltage at the output and not to a theoretical value for PTAT. The calibration procedure is easily carried out by opening or shorting the links of a quasi-binary trim network like the one shown in *Figure 6*. The links may be opened to add resistance by blowing an aluminum fuse, or a resistor may be shorted out of the circuit by carrying out a "zener-zap". The analysis in the next section shows that when the circuit is calibrated at a given temperature, then the circuit will be accurate for the full temperature range.

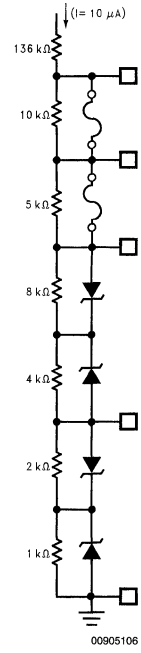


FIGURE 6.

How the Calibration Procedure Works

Widlar[5] has shown that a good approximation for the base-emitter voltage of a transistor is:

$$V_{BE} = V_{G0}\left(1 - \frac{T}{T_0}\right) + V_{beo}\left(\frac{T}{T_0}\right) + \frac{nkT}{q} \ln\left(\frac{T_0}{T}\right) + \frac{kT}{q} \ln \frac{I_C}{I_{co}} \quad (2)$$

where T is the temperature in °Kelvin, T_0 is a reference temperature, V_{GO} is the bandgap of silicon, typically 1.22V,

How the Calibration Procedure Works (Continued)

and V_{beo} is the transistor's base-emitter voltage at the reference temperature, T_0. The above equation can be re-written as

$$V_{BE} = (\text{sum of linear temp terms}) + (\text{sum of non-linear temp terms}) \quad (3)$$

where the first two terms of *Equation (1)* are linear and the last two terms are non-linear. The non-linear terms were shown by Widlar to be relatively small and thus will be considered later.

Let us define a base voltage, V_b, which is a linear function of temperature as: $V_b = C_1 \cdot T$. This voltage may be represented by the circuit in *Figure 1*. The emitter voltage is $V_e = V_b - V_{be}$ which becomes:

$$V_e = C_1T - V_{G0}\left(1 - \frac{T}{T_0}\right) - V_{beo}\left(\frac{T}{T_0}\right).$$

If V_e is defined as being equal to C_2 at $T = T_0$, then the above equation may be solved for C_1. Doing so gives:

$$C_1 = \frac{V_{beo} + C_2}{T_0} \quad (4)$$

Using this value for C_1 in the equation for V_e gives:

$$V_e = C_2\frac{T}{T_0} + V_{G0}\left(\frac{T - T_0}{T_0}\right) \quad (5)$$

If V_e is differentiated with respect to temperature, T, *Equation (4)* becomes $dV_e/dT = (C_2 + V_{G0})/T_0$.

This equation shows that if V_b is adjusted at T_0 to give $V_e = C_2$, then the rate of change of V_e with respect to temperature will be a constant, independent of the value of V_b, the transistor's beta or V_{be}. To proceed, consider the case where $V_e = C_2 = 0$ at $T_0 = 0°C$. Then

$$\frac{dV_e}{dT} = \frac{V_{G0}}{273.7} = 4.47\ mV/°C$$

Therefore, if V_e is trimmed to be equal to (4.47 mV) T (in °C) for each degree of displacement from 0°C, then the trimming can be done at ambient temperatures.

In practice, the two non-linear terms in *Equation (1)* are found to be quadratic for positive temperatures. Tsividis[6] showed that the bandgap voltage, V_0, is not linear with respect to temperature and causes nonlinear terms which become significant for negative temperatures (below 0°C). The sum of these errors causes an error term which has an approximately square-law characteristic and is thus compensated by the curvature compensation circuit of *Figure 7*.

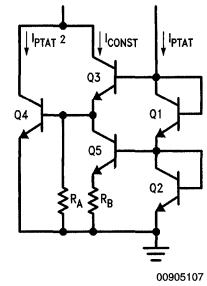


FIGURE 7.

A Unique Compensation Circuit

As mentioned earlier, the base-emitter voltage, V_{BE}, is not a linear function with respect to temperature. In practice, the nonlinearity of this function may be approximated as having a square-law characteristic. Therefore, the inherent non-linearity of the transistor and diode may be corrected by introducing a current with a square-law characteristic into the indicated node of *Figure 4*. Here's how the circuit of *Figure 7* works: transistors Q1 and Q2 are used to establish currents in the other three transistors. The current through Q1 and Q2 is linearly proportional to absolute temperature, I_{PTAT}, as is the current through transistor Q5 and resistor R_B. The current through resistor R_A is a decreasing function of temperature since it is proportional to the V_{BE} of transistor Q4. The emitter current of Q3 is equal to the sum of the current through Q5 and the current through R_A, and thus Q3's collector current is a constant with respect to temperature. The current through transistor Q4, I_{C4}, will be used to compensate for the V_{BE} nonlinearities and is found with the use of the following equation:

$$I_{C4} = I_S\left(e^{\frac{qV_{BE4}}{KT}} - 1\right) \cong I_S\, e^{\frac{qV_{BE4}}{KT}}$$

where $V_{BE4} = V_{BE1} + V_{BE2} - V_{BE3}$.

From the above logarithmic relationship, it is apparent that I_{C4} becomes

$$I_{C4} = \frac{I_{C1}\, I_{C2}}{I_{C3}} = \frac{I_{PTAT}{}^2}{I_{CONST}}.$$

A Unique Compensation Circuit

(Continued)

Thus, a current which has a square law characteristic and is $PTAT^2$, is generated for use as a means of curvature correction.

Processing and Layout

The sensor is constructed using conventional bipolar epitaxial linear processing. SiCr thin-film resistors are used in place of their diffused counterparts as a result of their better tempco matching, an important consideration for resistors which must track over temperature. Such resistors include R1 and nR1 of the bandgap circuit.

Another point of interest in the construction of the device centers around transistors Q1 and Q2 of *Figure 4*. In order for the circuit to retain its accuracy over temperature, the leakage currents of each transistor, which can become quite significant at high temperatures, must be equal so that their effects will cancel one another. If the geometries of the two transistors were equivalent, then their leakage currents would be also, but since Q1 has ten times the emitter area of Q2, the accuracy of the device could suffer. To correct the problem, the circuit is built with Q1 and Q2 each replaced by a transistor group consisting of both Q1 and Q2. These transistor groups have equivalent geometries so that their leakage currents will cancel, but only one transistor of each group, representing Q1 in one group and Q2 in the other pair is used in the temperature sensing circuit. A circuit diagram demonstrating this idea is shown in *Figure 8.*

Using the LM34

The LM34 is a versatile device which may be used for a wide variety of applications, including oven controllers and remote temperature sensing. The device is easy to use (there are only three terminals) and will be within 0.02˚F of a surface to which it is either glued or cemented. The TO-46 package allows the user to solder the sensor to a metal surface, but in doing so, the GND pin will be at the same potential as that metal. For applications where a steady reading is desired despite small changes in temperature, the user can solder the TO-46 package to a thermal mass. Conversely, the thermal time constant may be decreased to speed up response time by soldering the sensor to a small heat fin.

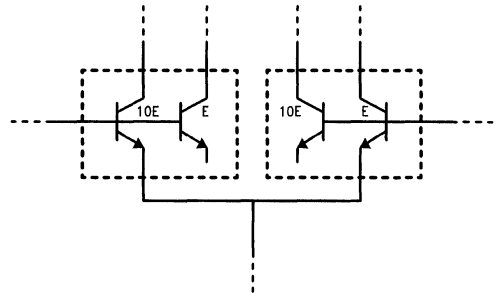


FIGURE 8.

Fahrenheit Temperature Sensors

As mentioned earlier, the LM34 is easy to use and may be operated with either single or dual supplies. *Figure 9* shows a simple Fahrenheit temperature sensor using a single supply. The output in this configuration is limited to positive temperatures. The sensor can be used with a single supply over the full −50˚F to +300˚F temperature range, as seen in *Figure 10*, simply by adding a resistor from the output pin to ground, connecting two diodes in series between the GND pin and the circuit ground, and taking a differential reading. This allows the LM34 to sink the necessary current required for negative temperatures. If dual supplies are available, the sensor may be used over the full temperature range by merely adding a pull-down resistor from the output to the negative supply as shown in *Figure 11*. The value of this resistor should be $|-V_S|/50\ \mu A$.

For applications where the sensor has to be located quite a distance from the readout circuitry, it is often expensive and inconvenient to use the standard 3-wire connection. To overcome this problem, the LM34 may be connected as a two-wire remote temperature sensor. Two circuits to do this are shown in *Figure 12* and *Figure 13*. When connected as a remote temperature sensor, the LM34 may be thought of as a temperature-dependent current source. In both configurations the current has both a relatively large value,

Fahrenheit Temperature Sensors

(Continued)

$$(20\ \mu A/^{\circ}F) \times (T_A + 3^{\circ}F),$$

and less offset when compared to other sensors. In fact, the current per degree Fahrenheit is large enough to make the output relatively immune to leakage currents in the wiring.

Temperature to Digital Converters

For interfacing with digital systems, the output of the LM34 may be sent through an analog to digital converter (ADC) to provide either serial or parallel data outputs as shown in *Figure 14* and *Figure 15*. Both circuits have a 0 to +128°F scale. The scales are set by adjusting an external voltage reference to each ADC so that the full 8 bits of resolution will be applied over a reduced analog input range. The serial output ADC uses an LM385 micropower voltage reference diode to set its scale adjust (V_{REF} pin) to 1.28V, while the parallel output ADC uses half of an LM358 low power dual op amp configured as a voltage follower to set its $V_{REF}/2$ pin to 0.64V. Both circuits are operated with standard 5V supplies.

Basic Fahrenheit Temperature Sensor (+5° to +300°F)

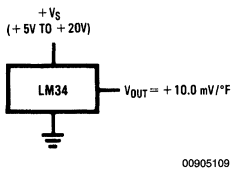


FIGURE 9.

Temperature Sensor, Single Supply, -50° to +300°F

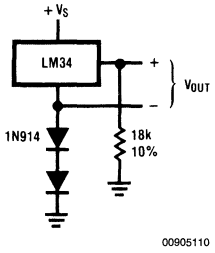


FIGURE 10.

Full-Range Fahrenheit Temperature Sensor

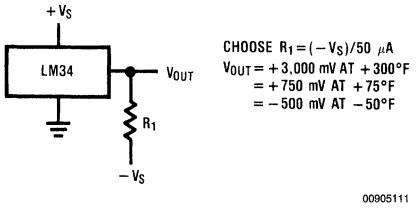
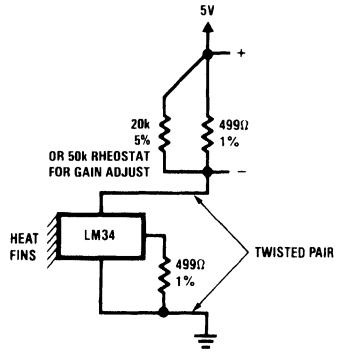


FIGURE 11.

Temperature to Digital Converters (Continued)

Two-Wire Remote Temperature Sensor
(Grounded Sensor)



V_{OUT} = 10 mV/°F (T_A + 3°F)
from +3°F to +100°F

FIGURE 12.

Two-Wire Temperature Sensor
(Output Referred to Ground)

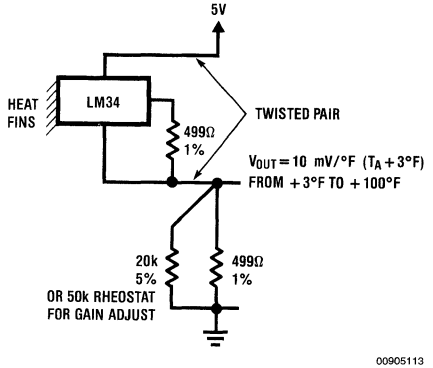


FIGURE 13.

Temperature to Digital Converters (Continued)

Temperature-to-Digital Converter (Serial Output, +128°F Full Scale)

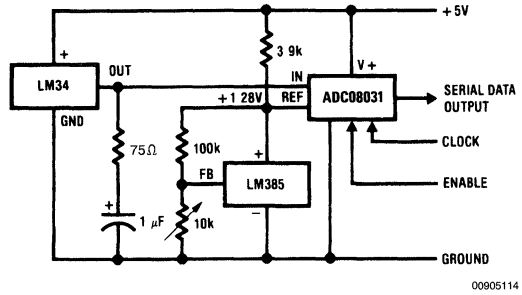


FIGURE 14.

Temperature-to-Digital Converter (Parallel TRI-STATE Outputs for Standard Data Bus to μP Interface, 128°F Full Scale)

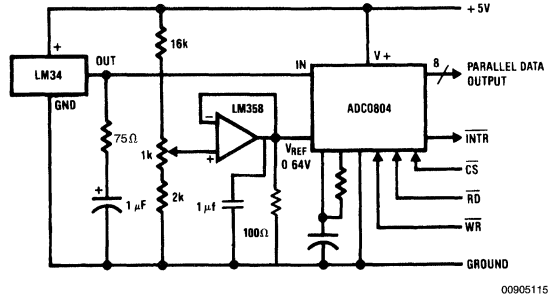


FIGURE 15.

LM34 with Voltage-to-Frequency Converter and Isolated Output (3°F to +300°F; 30 Hz to 3000 Hz)

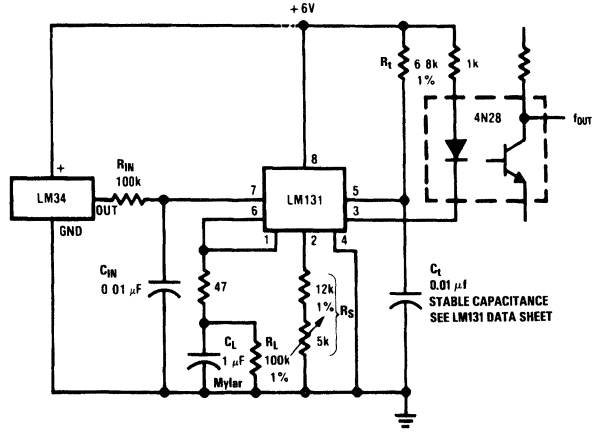
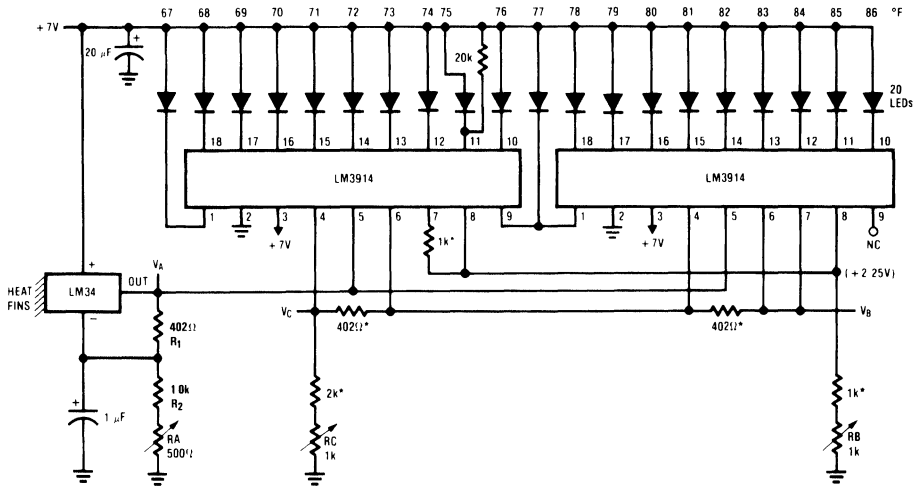


FIGURE 16.

Temperature to Digital Converters (Continued)

Bar-Graph Temperature Display (Dot Mode)



• = 1% or 2% film resistor
—Trim R_B for V_B = 3.525V
—Trim R_C for V_C = 2.725V
—Trim R_A for V_A = 0.085V + 40 mV/°F x $T_{Ambient}$
—Example V_A = 3.285V at 80°F

FIGURE 17.

Temperature-to-Frequency Converter for Remote Sensing

If a frequency proportional to temperature is needed, then the LM34 can be used in conjunction with an LM131 voltage-to-frequency converter to perform the desired conversion from temperature to frequency. A relatively simple circuit which performs over a +3°F to +300°F temperature range is shown in *Figure 16*. The output frequency of this circuit can be found from the equation:

$$f_{OUT} = \left(\frac{V_{IN}}{2.09V}\right)\left(\frac{R_S}{R_L}\right)\left(\frac{1}{R_t\, C_t}\right)$$

where resistor R_S is used to adjust the gain of the LM131. If R_S is set to approximately 14.2 kΩ, the output frequency will have a gain of 10 Hz/°F. Isolation from high common mode levels is provided by channeling the frequency through a photoisolator. This circuit is also useful for sending temperature information across long transmission lines where it can be decoded at the receiving station.

LED Display for Easy Temperature Reading

It is often beneficial to use an array of LED's for displaying temperature. This application may be handled by combining the LM34 with an LM3914 dot/display driver. The temperature may then be displayed as either a bar of illuminated LED's or as a single LED by simply flipping a switch. A wide range of temperatures may be displayed at once by cascading several LM3914's as shown in *Figure 17*.

Without going into how the LM3914 drivers function internally, the values for V_A, V_B, and V_C can be determined as follows:

V_A is the voltage appearing at the output pin of the LM34. It consists of two components, 0.085V and (40 mV/°F) (T_A).

The first term is due to the LM34's bias current (approximately 70 μA) flowing through the 1 kΩ resistor in series with R_A. The second term is a result of the multiplication of the LM34's output by the resistive string composed of R_1, R_2, and R_A, where R_A is set for a gain factor of 4 (i.e.; 40 mV/°F).

V_B represents the highest temperature to be displayed and is given by the equation V_B = 0.085V + (40 mV/°F) (T_{HIGH}). For the circuit in *Figure 17*, V_B = 0.085V + (40 mV/°F) (86°F) = 3.525V.

V_C represents the lowest temperature to be displayed minus 1°F. That is, V_C = 0.085V + (T_{LOW} −1°F) (40 mV/°F) which in this case becomes V_C = 0.085V + (67°F −1°F) (40 mV/°F) = 2.725V.

With a few external parts, the circuit can change from dot to bar mode or flash a bar of LED's when the temperature sensed reaches a selected limit (see LM3914 data sheet).

Indoor/Outdoor Thermometer

An indoor/outdoor thermometer capable of displaying temperatures all the way down to −50°F is shown in *Figure 18*.

Indoor/Outdoor Thermometer

(Continued)

Two sensor outputs are multiplexed through a CD4066 quad bilateral switch and then displayed one at a time on a DVM such as Texmate's PM-35X. The LMC555 timer is run as an astable multivibrator at 0.2 Hz so that each temperature reading will be displayed for approximately 2.5 seconds. The RC filter on the sensors outputs are to compensate for the capacitive loading of the cable. An LMC7660 can be used to provide the negative supply voltage for the circuit.

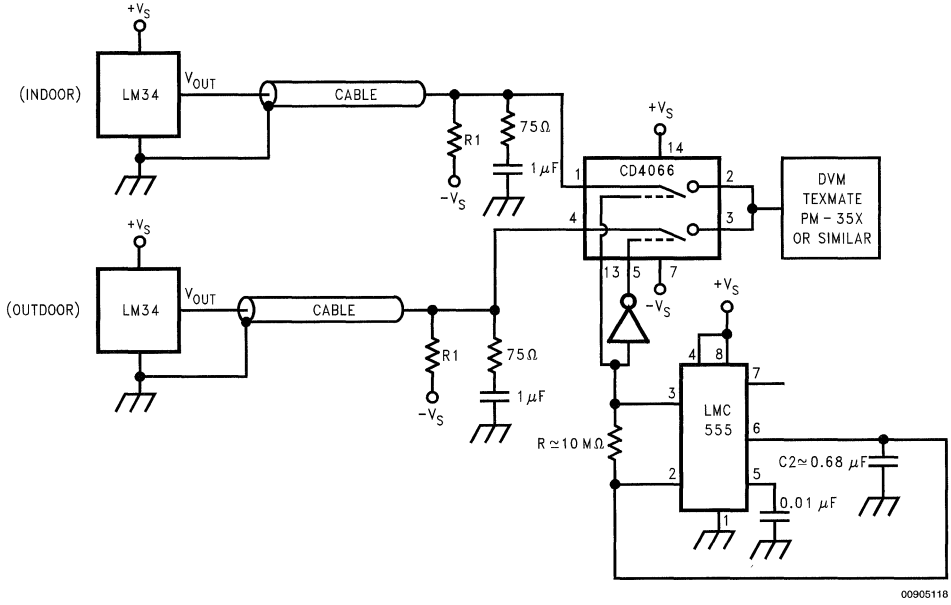


FIGURE 18.

Temperature Controller

A proportional temperature controller can be made with an LM34 and a few additional parts. The complete circuit is shown in *Figure 19*. Here, an LM10 serves as both a temperature setting device and as a driver for the heating unit (an LM395 power transistor). The optional lamp, driven by an LP395 Transistor, is for indicating whether or not power is being applied to the heater.

When a change in temperature is desired, the user merely adjusts a reference setting pot and the circuit will smoothly make the temperature transition with a minimum of overshoot or ringing. The circuit is calibrated by adjusting R2, R3 and C2 for minimum overshoot. Capacitor C2 eliminates DC offset errors. Then R1 and C1 are added to improve loop stability about the set point. For optimum performance, the temperature sensor should be located as close as possible to the heater to minimize the time lag between the heater application and sensing. Long term stability and repeatability are better than 0.5°F.

Differential Thermometer

The differential thermometer shown in *Figure 20* produces an output voltage which is proportional to the temperature difference between two sensors. This is accomplished by using a difference amplifier to subtract the sensor outputs from one another and then multiplying the difference by a factor of ten to provide a single-ended output of 100 mV per degree of differential temperature.

Differential Thermometer (Continued)

Temperature Controller

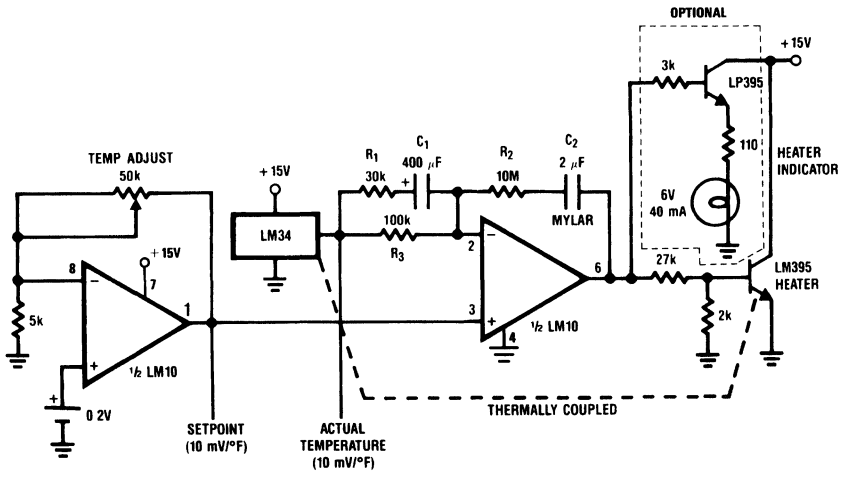


FIGURE 19.

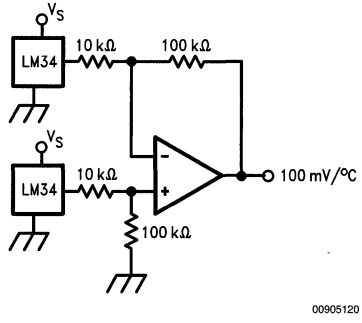
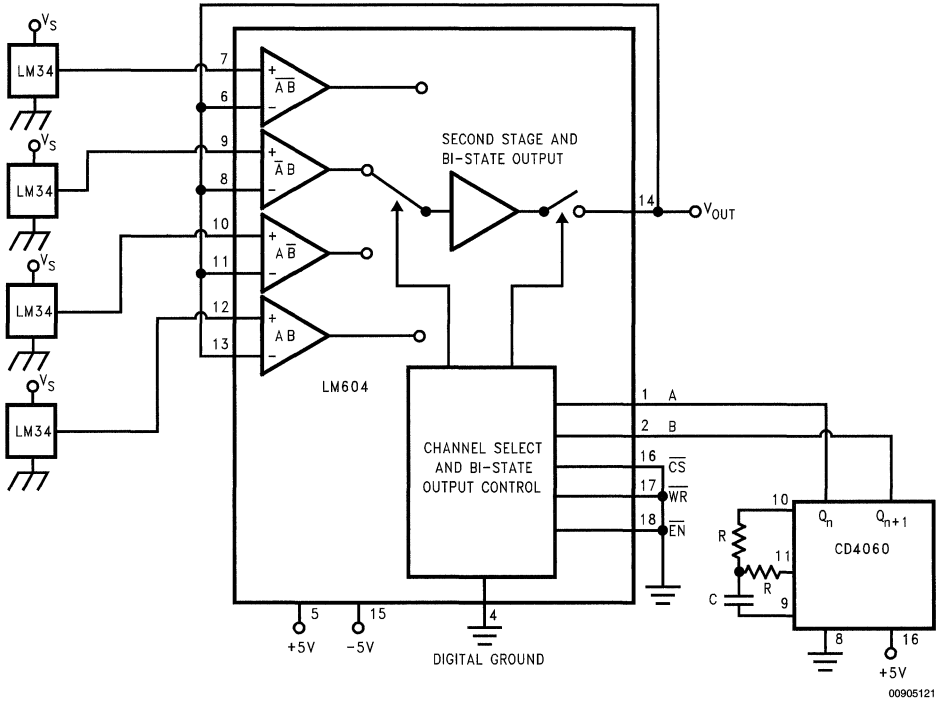


FIGURE 20.

Differential Thermometer (Continued)



Temperature monitoring

$$\text{rate} = \frac{0.56}{RC}\left(\frac{1}{2^{n-1}}\right)$$

If Q_4 and Q_5 are used with R = 13k and C = 510 pF the rate will be 10 kHz

FIGURE 21.

Temperature Scanner

In some applications it is important to monitor several temperatures periodically, rather than continuously. The circuit shown in *Figure 21* does this with the aid of an LM604 Mux Amp. Each channel is multiplexed to the output according to the AB channel select. The CD4060 ripple binary counter has an on-board oscillator for continuous updating of the channel selects.

Conclusion

As can be seen, the LM34 and LM35 are easy-to-use temperature sensors with excellent linearity. These sensors can be used with minimal external circuitry for a wide variety of applications and do not require any elaborate scaling schemes nor offset voltage subtraction to reproduce the Fahrenheit and Celsius temperature scales respectively.

References

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2. R.A. Pease, "A New Celsius Temperature Sensor", National Semiconductor Corp., 1983.
3. Robert Dobkin, "Monolithic Temperature Transducer", in *Dig. Tech. Papers,* Int. Solid State Circuits Conf., 1974, pp. 126, 127, 239, 240.
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5. R.J. Widlar, "An Exact Expression for the Thermal Variation of the Emitter—Base Voltage of Bipolar Transistors", *Proc. IEEE,* January 1967.
6. Y.P. Tsividis, "Accurate Analysis of Temperature Effects in $I_C - V_{BE}$ Characteristics with Application to Bandgap Reference Sources", *IEEE Journal of Solid-State Circuits,* December 1980, pp. 1076–1084.
7. Michael P. Timko, "A Two-Terminal IC Temperature Transducer", *IEEE Journal of Solid-State Circuits,* December 1976, pp. 784–788.

Microcontroller Interface to the ADC12038 Families

National Semiconductor
Application Note 929
Emmy Denton

1.0 General Overview

The ADC12038 families are 12-bit plus sign sampling ADC converters with serial I/O. These devices have configurable analog multiplexers with 2, 4, or 8 input channels. On request, these A/Ds perform a self calibration routine that minimizes linearity, zero, and full-scale errors. To minimize power consumption these devices have a power down mode that can be accessed by hardware (PD pin) or by a software instruction.

The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ and HPC families of controllers, and can easily interface with standard shift registers and microprocessors. The conversion resolution can be selected by a software instruction to be 8-bits, 8-bits+sign, 12-bits or 12-bits+sign. 8-bit and 8-bit+sign conversions take less time than 12-bit and 12-bit+sign conversions (21 clock periods versus 44). In addition, selection of the output data format can be software programmable to be:

1. 8-bits, 8-bits+sign, 12-bits, 12-bits+sign, 16-bits or 16-bits+sign in length
2. MSB or LSB first
3. Left or Right justified

There are three ADC12038 families: Low voltage, High speed and standard. Each family includes four different combinations of analog inputs and features as summarized in *Table 1*.

TABLE 1. Summary of the Differences of the Devices in the Three ADC12038 Families

Device Number	Operating Supply Voltage and Power Dissipation	Maximum Clock Frequency (MHz)	Maximum Sampling Rate (kHz)	Number of MUX Inputs	MUX OUT and A/D IN Pins	Hardware Power Down Control (PD Pin)	Package Size and Type
ADC12030	5V ±10% 33 mW (max) @5V	5 MHz	73 kHz	2	NO	NO	16-pin DIP & SO
ADC12032				2	YES	NO	20-pin DIP & SO
ADC12034				4	YES	YES	24-pin DIP & SO
ADC12038				8	YES	YES	28-pin DIP & SO
ADC12L030	3.3V ±10% 15 mW (max) @3.3V			2	NO	NO	16-pin DIP & SO
ADC12L032				2	YES	NO	20-pin DIP & SO
ADC12L034				4	YES	YES	24-pin DIP & SO
ADC12L038				8	YES	YES	28-pin DIP & SO
ADC12H030	5V ±10% 36 mW (max) @5V	8 MHz	116 kHz	2	NO	NO	16-pin DIP & SO
ADC12H032				2	YES	NO	20-pin DIP & SO
ADC12H034				4	YES	YES	24-pin DIP & SO
ADC12H038				8	YES	YES	28-pin DIP & SO

Throughout this application note we will refer to the ADC12038. Any of this information will also apply to all the devices in the ADC12038 families. The device data sheets should be used in conjunction with this application note to help you understand the operation of these devices. The scope of this application note will focus on the digital interface. A brief overview of the digital functionality of these devices is included.

1.1 THE SERIAL INTERFACE

The ADC12038 families of analog-to-digital converters can be programmed for many modes of operation through their serial digital interface. The serial interface for the ADC12038 is comprised of the digital control lines SCLK, $\overline{CS}$, DO, DI, EOC, $\overline{DOR}$, PD and $\overline{CONV}$. *Table 2* gives a brief pin description for each of these control lines.

1.0 General Overview (Continued)

TABLE 2. Digital Control Pin Descriptions

Pin Name	Description
SCLK	This is the serial data clock input. The clock applied to this input controls the rate at which the serial data exchange occurs. With $\overline{CS}$ low the rising edge of SCLK loads the information on the DI pin into the multiplexer address and mode select shift register. This address controls which channel of the analog input multiplexer (MUX) is selected and the mode of operation for the ADC. With $\overline{CS}$ low the falling edge shifts of SCLK the data resulting from the previous ADC conversion out on DO, with the exception of the first bit of data. When $\overline{CS}$ is low continuously, the first bit of the data is clocked out on the rising edge of EOC (end of conversion). When $\overline{CS}$ is toggled the falling edge of $\overline{CS}$ always clocks out the first bit of data. $\overline{CS}$ should be brought low when SCLK is low.
$\overline{CS}$	This is the chip select pin. When a logic low is applied to this pin the device is selected, activating the DO, DI, and SCLK serial interface lines. The falling edge of $\overline{CS}$ resets a conversion in progress and starts the sequence for a new conversion. When $\overline{CS}$ is brought low during a conversion in progress, the conversion is prematurely ended and the data in the output latches may be corrupted, requiring the data output at this time to be ignored. $\overline{CS}$ should be brought low when SCLK is low.
DI	The data input pin. The data applied to this pin is shifted by the rising edge of SCLK into the multiplexer address and mode select register. *Tables 4, 5, 6, 7* show the assignments of the multiplexer address and the mode select data.
DO	The data output pin. This pin is an active push/pull output when $\overline{CS}$ is Low. When $\overline{CS}$ is High this output is in TRI-STATE. The ADC conversion result and converter status data are clocked out by the falling edge of SCLK on this pin.
EOC	This pin is an active push/pull output and indicates the status of the device. When Low, it signals that the ADC is busy with a conversion, auto-calibration, auto-zero or power down cycle. The rising edge of EOC signals the end of one of these cycles.
$\overline{DOR}$	This is the data output ready pin. This pin is an active push/pull output. It is useful only when $\overline{CS}$ is toggled.
$\overline{CONV}$	A logic Low is required on this pin to program any mode or change the ADC's configuration (12-bit conversion, 8-bit conversion, Auto Cal, Auto Zero etc.) as listed in the Mode Programming Table (*Table 4*). When this pin is high the ADC is placed in the read data only mode. While in the read data only mode, bringing $\overline{CS}$ low and Pulsing SCLK will only clock out on DO any data stored in the ADCs output shift register. The data on DI will be neglected. A new conversion will not be started and the ADC will remain in the mode and/or configuration previously programmed. Read data only cannot be performed while a conversion, Auto-Cal or Auto-Zero are in progress.
PD	This is the power down pin. When PD is high, the ADC is powered down; when PD is low, the ADC is powered up.

1.0 General Overview (Continued)

The interplay of these lines can be graphically seen in the timing diagram of *Figure 1*.

The chip select pin ($\overline{CS}$) enables the logic inputs and DO output Eight bits of data that control the ADC are clocked in on the digital input pin (DI) by the rising edge of the serial clock (SCLK) when $\overline{CS}$ is low. Taking $\overline{CS}$ will output the first bit of data (DBO) on DO. While $\overline{CS}$ is low, the falling edge of SCLK clocks the data out on the digital output pin (DO). $\overline{CS}$ should only be brought low when SCLK is low The functions of the convert input ($\overline{CONV}$), data output ready ($\overline{DOR}$) and end of conversion output (EOC) pins are covered in more detail in the data sheet. The simplest interface to the ADC12038 requires only 4 control lines: DO, DI, SCLK and $\overline{CS}$ For this case $\overline{CONV}$ and PD are grounded and EOC and $\overline{DOR}$ outputs are not used

1.2 THE SERIAL OUTPUT WORD FORMAT

The diagram in *Figure 2* shows a 16-bit serial output word. The ADC12038 family can be programmed to provide unsigned output data in 8-bit, 12-bit, or 16-bit word lengths or signed data in 9-bit, 13-bit, or 17-bit word lengths The data format can be right- or left-justified, MSB or LSB first. *Table 3* summarizes the available serial output data formats. *Table 4* describes the serial input word required to select the available serial output data formats.

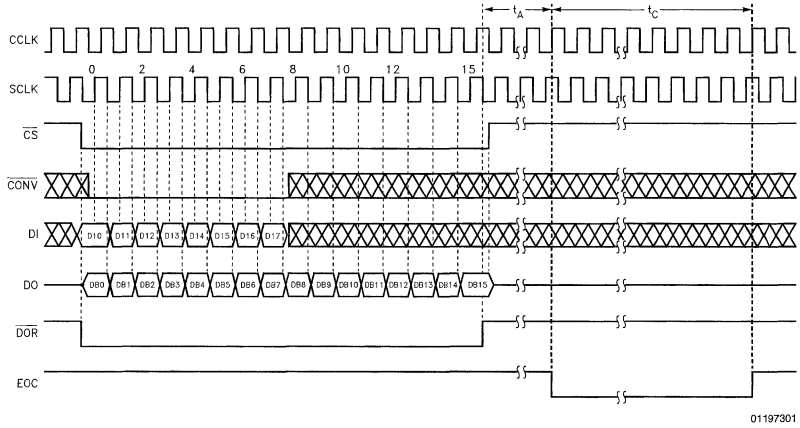


FIGURE 1. Timing Diagram for a 12-Bit Plus Sign Conversion with a 16-Bit Serial Output Word Format on DO

1.0 General Overview (Continued)

TABLE 3. Data Out Formats

DO Formats			DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8	DB9	DB10	DB11	DB12	DB13	DB14	DB15	DB16
with Sign	MSB First	17 Bits	Sign	Sign	Sign	Sign	Sign	MSB	10	9	8	7	6	5	4	3	2	1	LSB
		13 Bits	Sign	MSB	10	9	8	7	6	5	4	3	2	1	LSB				
		9 Bits	Sign	MSB	6	5	4	3	2	1	LSB								
	LSB First	17 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB	Sign	Sign	Sign	Sign	Sign
		13 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB	Sign				
		9 Bits	LSB	1	2	3	4	5	6	MSB	Sign								
without Sign	MSB First	16 Bits	0	0	0	0	MSB	10	9	8	7	6	5	4	3	2	1	LSB	
		12 Bits	MSB	10	9	8	7	6	5	4	3	2	1	LSB					
		8 Bits	MSB	6	5	4	3	2	1	LSB									
	LSB First	16 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB	0	0	0	0	
		12 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB					
		8 Bits	LSB	1	2	3	4	5	6	MSB									

The falling edge of SCLK strobes out the digital word on DO when $\overline{CS}$ is low. The digital word length will vary in accord with the digital word format. Thus for 8-bits + sign resolution 9 clock cycles are required.

As shown in the timing diagram (*Figure 1*), the acquisition time (the period of time during which the analog input is being sampled) starts on the falling edge of the last data clock cycle. For 16 bits of data that would be the 16th clock; for 8 bits of data that would be the 8th clock. The length of the acquisition time may be programmed by the user with an instruction, (see *Table 4*). The acquisition time can be set to 6, 10, 18, or 34 CCLK cycles.

1.3 SELECTING OUTPUT WORD FORMAT AND MODE

While $\overline{CS}$ is low, the rising edge of SCLK strobes in the data bits DI0–DI7 on the DI control line. For the ADC12038, the values of DI0–DI7 determine the digital output word format, mode select, and multiplexer configuration. For the ADC12034, 7 bits of data (DI0–DI6) are required. The ADC12032, and ADC12030 require only 6 bits of data (DI0–DI5). Mode Select determines the number of clock periods for the acquisition time (t_A), software power up/down, Auto Cal, Auto Zero and other functions as shown in *Table 4*.

1.0 General Overview (Continued)

TABLE 4. Mode Programing

ADC12038	DI0	DI1	DI2	DI3	DI4	DI5	DI6	DI7	Mode Select (Current)	DO Format (next Conversion Cycle)
ADC12034	DI0	DI1	DI2		DI3	DI4	DI5	DI6		
ADC12030 and ADC12032	DI0	DI1			DI2	DI3	DI4	DI5		
	MUX Address see *Tables 5, 6* or *Table 7*				L	L	L	L	12-Bit Conversion	12- or 13-Bit MSB First
	MUX Address see *Tables 5, 6* or *Table 7*				L	L	L	H	12-Bit Conversion	16-Bit MSB First
	MUX Address see *Tables 5, 6* or *Table 7*				L	L	H	L	8-Bit Conversion	8- or 9-Bit MSB First
	L	L	L	L	L	L	H	H	12-Bit Conversion of Full-Scale	12- or 13-Bit MSB First
	MUX Address see *Tables 5, 6* or *Table 7*				L	H	L	L	12-Bit Conversion	12- or 13-Bit LSB First
	MUX Address see *Tables 5, 6* or *Table 7*				L	H	L	H	12-Bit Conversion	16-Bit LSB First
	MUX Address see *Tables 5, 6* or *Table 7*				L	H	H	L	8-Bit Conversion	8- or 9-Bit LSB First
	L	L	L	L	L	H	H	H	12-Bit Conversion of Offset	12- or 13-Bit LSB First
	L	L	L	L	H	L	L	L	Auto Cal	No Change
	L	L	L	L	H	L	L	H	Auto Zero	No Change
	L	L	L	L	H	L	H	L	Power Up	No Change
	L	L	L	L	H	L	H	H	Power Down	No Change
	L	L	L	L	H	H	L	L	Read Status Register (LSB First)	No Change
	L	L	L	L	H	H	L	H	Data Out without Sign	No Change
	H	L	L	L	H	H	L	H	Data Out with Sign	No Change
	L	L	L	L	H	H	H	L	Acquisition Time—4 CCLK Cycles	No Change
	L	H	L	L	H	H	H	L	Acquisition Time—8 CCLK Cycles	No Change
	H	L	L	L	H	H	H	L	Acquisition Time—16 CCLK Cycles	No Change
	H	H	L	L	H	H	H	L	Acquisition Time—32 CCLK Cycles	No Change
	L	L	L	L	H	H	H	H	User Mode	No Change
	H	L	L	L	H	H	H	H	Test Mode (CH1–CH7 become Active Outputs)	No Change

Note: The A/D powers up with No CAL, No Auto-Zero, 10 CCLK Cycles Acquisition time, sign bit on, 13-bit MSB First format, power up, and user mode

1.0 General Overview (Continued)

1.4 MULTIPLEXER ADDRESSING

The analog input channel configuration is selected during mode programming using the "MUX address" bits in *Table 4*. These bits and their effects are defined in *Tables 5, 6, 7.*

TABLE 5. ADC12038 Multiplexer Addressing

MUX Address				Analog Channel Addressed and Assignment with A/D IN1 tied to MUXOUT1 and A/D IN2 tied to MUXOUT2									A/D Input Polarity Assignment		Multiplexer Output Channel Assignment		Mode
DI0	DI1	DI2	DI3	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM	A/D IN1	A/D IN2	MUXOUT1	MUXOUT2	
L	L	L	L	+	−								+	−	CH0	CH1	
L	L	L	H			+	−						+	−	CH2	CH3	
L	L	H	L					+	−				+	−	CH4	CH5	
L	L	H	H							+	−		+	−	CH6	CH7	Differential
L	H	L	L	−	+								−	+	CH0	CH1	
L	H	L	H			−	+						−	+	CH2	CH3	
L	H	H	L					−	+				−	+	CH4	CH5	
L	H	H	H							−	+		−	+	CH6	CH7	
H	L	L	L	+								−	+	−	CH0	COM	
H	L	L	H			+						−	+	−	CH2	COM	
H	L	H	L					+				−	+	−	CH4	COM	
H	L	H	H							+		−	+	−	CH6	COM	Single-Ended
H	H	L	L		+							−	+	−	CH1	COM	
H	H	L	H				+					−	+	−	CH3	COM	
H	H	H	L						+			−	+	−	CH5	COM	
H	H	H	H								+	−	+	−	CH7	COM	

TABLE 6. ADC12034 Multiplexer Addressing

MUX Address			Analog Channel Addressed and Assignment with A/D IN1 tied to MUXOUT1 and A/D IN2 tied to MUXOUT2					A/D Input Polarity Assignment		Multiplexer Output Channel Assignment		Mode
DI0	DI1	DI2	CH0	CH1	CH2	CH3	COM	A/D IN1	A/D IN2	MUXOUT1	MUXOUT2	
L	L	L	+	−				+	−	CH0	CH1	
L	L	H			+	−		+	−	CH2	CH3	Differential
L	H	L	−	+				−	+	CH0	CH1	
L	H	H			−	+		−	+	CH2	CH3	
H	L	L	+				−	+	−	CH0	COM	
H	L	H			+		−	+	−	CH2	COM	Single-
H	H	L		+			−	+	−	CH1	COM	Ended
H	H	H				+	−	+	−	CH3	COM	

1.0 General Overview (Continued)

TABLE 7. ADC12032 and ADC12030 Multiplexer Addressing

MUX Address		Analog Channel Addressed and Assignment with A/D IN1 tied to MUXOUT1 and A/D IN2 tied to MUXOUT2			A/D Input Polarity Assignment		Multiplexer Output Channel Assignment		Mode
DI0	DI1	CH0	CH1	COM	A/D IN1	A/D IN2	MUXOUT1	MUXOUT2	
L	L	+	−		+	−	CH0	CH1	Differential
L	H	−	+		−	+	CH0	CH1	
H	L	+		−	+	−	CH0	COM	Single-
H	H		+	−	+	−	CH1	COM	Ended

Note: MUXOUT1, MUXOUT2, A/D IN1 and A/D IN2 pins are not available on the ADC12030 A/D IN1 is tied internally to MUXOUT1 A/D IN2 is tied internally to MUXOUT2

As can be seen in the tables, 4, 3 or 2 bits of the serial digital input word control the channel selection. These bits are part of an 8-, 7-, or 6-bit serial word that controls the function of the devices.

1.5 STATUS REGISTER DEFINITION

On request, the ADC12038 provides status information indicating power up or power down status, output data format, Auto-Cal status, and User/Test Mode status. *Table 8* defines the digital output data obtained after requesting a "Status Read".

When $\overline{CS}$ is used it is not necessary to clock all the status bits out. $\overline{CS}$ may be brought high at any time to restart a new serial data communication.

1.6 PROGRAMMING PROCEDURE

The example in *Figure 2* shows a typical sequence of events after power is applied to the ADC12038:

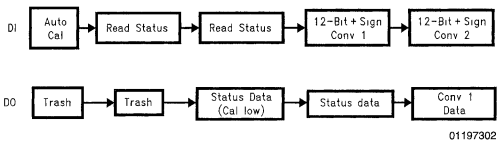


FIGURE 2. Typical Instruction Sequence after Power Up

The first instruction to the ADC via DI initiates Auto Cal. The data output on DO at that time is meaningless and is completely random. To obtain the specified accuracy of the device it is necessary to issue an Auto Cal instruction after the power supply and reference voltage to the device have been given enough time to stabilize. The Auto Cal instruction initiates an internal calibration sequence without which the specified accuracy of the device would be unattainable. To determine whether the Auto Cal has been completed, a Read Status instruction is issued to the device Again, the data obtained while issuing the Read Status instruction has no significance since the Auto Cal instruction modifies the data in the output shift register. To retrieve the status information an additional read status instruction is issued to the ADC. At this time the status data is available on DO. If the Cal signal in the status word is low, Auto Cal has been completed. Therefore, the next instruction issued can start a conversion. The data output, while clocking in the "start conversion request", is again status information. Status can not be read during a conversion. To preserve the integrity of the A/D conversion, there is no end of conversion bit in the status word. If $\overline{CS}$ is brought low during a conversion, that conversion is stopped and never completed. EOC can be used to determine the end of a conversion or the A/D controller can keep track in software of when it would be appropriate to communicate to the A/D again. Once it has been determined that the A/D has completed a conversion another instruction can be transmitted to the A/D. The data from this conversion can be accessed when the next instruction is issued to the A/D

1.0 General Overview (Continued)

TABLE 8. Status Register

Status Bit Location	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8
Status Bit	PU	PD	Cal	8 or 9	12 or 13	16 or 17	Sign	Justification	Test Mode
Function	Device Status			DO Output Format Status					
	"High" indicates a Power Up State	"High" indicates a Power Down State	"High" indicates an Auto-Cal Sequence is in progress	"High" indicates an 8- or 9-bit format	"High" indicates a 12- or 13-bit format	"High" indicates a 16- or 17-bit format	"High" indicates that the sign bit is included. When "Low", the sign bit is not included.	When "High", the conversion result will be output MSB first. When "Low", the result will be output LSB first.	When "High", the device is in test mode. When "Low", the device is in user mode.

2.0 General Flow Chart for a Microcontroller Interface

Below is a flow chart that can be used for a microcontroller interface to the ADC12038. The data required by the ADC12038 is given in parentheses.

The timing diagrams shown to the right are suggested for each instruction issued to the ADC.

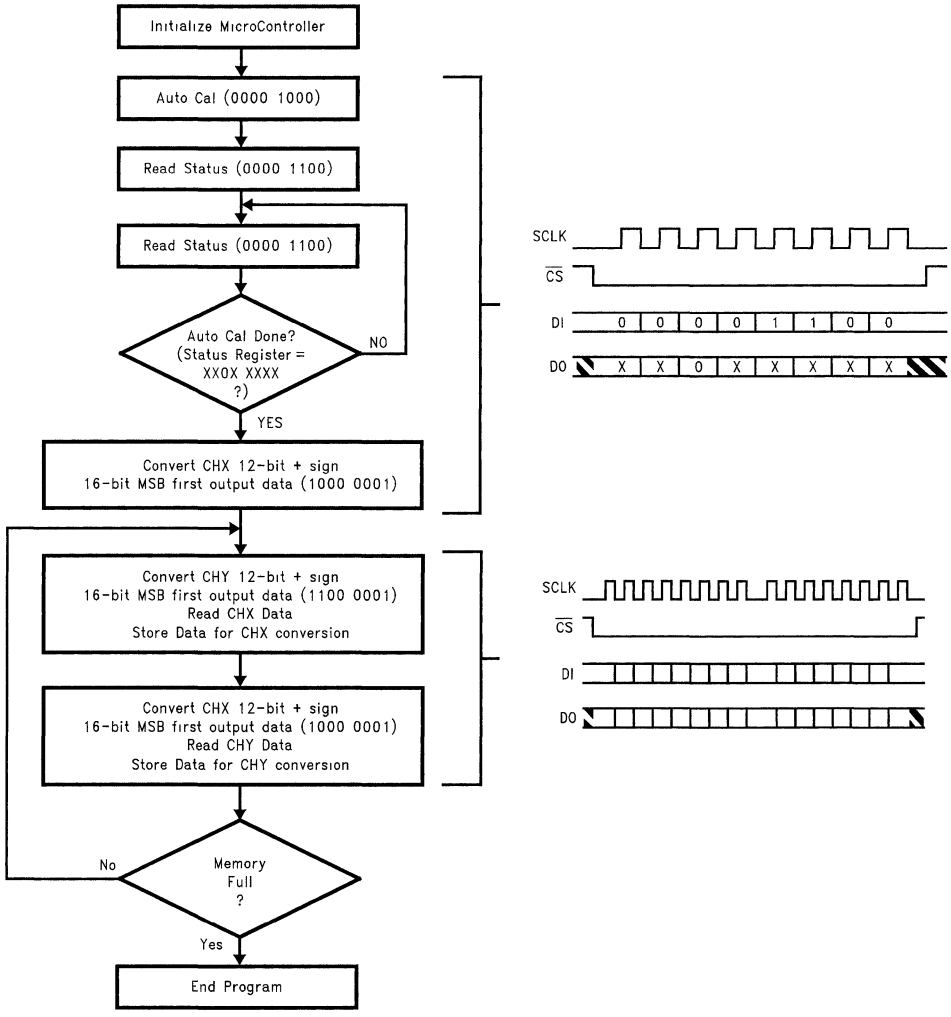


FIGURE 3. ADC12038 Program Flow Chart and Timing

3.0 Examples of Microcontroller Hardware Implementations

3.1 THE 68HC11

Figure 4 shows the hardware interface to a Motorola M68HC11 microcontroller. Motorola's SPI (Serial Peripheral Interface) SCK, MISO, and MOSI lines are directly tied to the SCLK, DO and DI of the ADC12038. Port B bit 0 is used to generate the $\overline{CS}$ to the ADC.

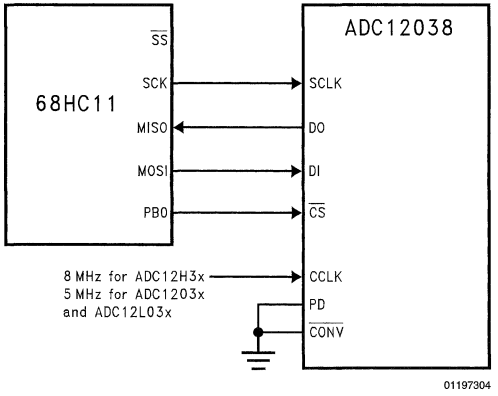


FIGURE 4. 68HC11 ADC12038 Hardware Interface

3.2 NATIONAL'S HPC AND COP

The serial I/O for these devices is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ and HPC™ families of controllers. The output data format is software-programmable, making the serial interface extremely flexible and an ideal choice for many applications. Shown in *Figure 5* is an implementation of an National Semiconductor HPC microcontroller interface. The SK (Serial clocK), SI (Serial Input data) and SO (Serial Output data) lines of the HPC, used in Nationals MICROWIRE interface, are tied directly to the ADC12038. Port B, bit 6 is used to generate a $\overline{CS}$ for the ADC.

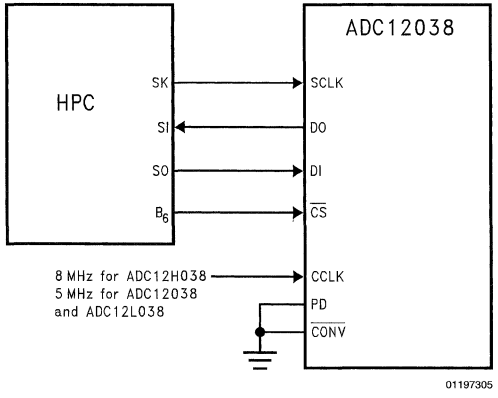


FIGURE 5. HPC to ADC12038 Hardware Interface

3.3 THE 8051

Figure 6 shows the ADC12038 connected to an Intel 8051. The 8051 serial interface does not support the protocol of the serial interface for this device. Therefore three port lines from the 8051 (P1.0, P1.1 and P1.2) can be used to talk to the ADC. The software toggles these lines directly to form the signals necessary to control the ADC.

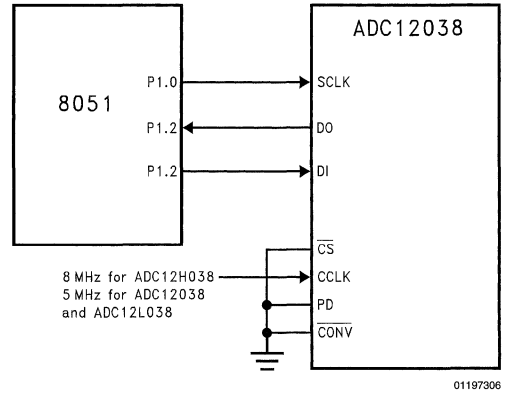


FIGURE 6. 8051 ADC12038 Hardware Interface

4.0 68HC11 SPI Interface

This section will describe in detail an SPI interface to the ADC12038. *Figure 7*, shown below, is a detailed schematic of the interface. The Motorola M68HC11EVB evaluation board was used to verify the program included at the end of this section. Therefore, the schematic shown here shows the connections required to the 68HC11 evaluation board.

4.1 68HC11 SPI PORT AND REGISTER INITIALIZATION FOR THE ADC12038

The 68HC11 SPI (Serial Peripheral Interchange) interface is ideal for driving the ADC12038. The SCK, MISO, and MOSI lines of the SPI tie directly to the SCLK, DO and DI lines of the ADC. $\overline{CS}$ for the ADC is generated using a line of the 68HC11's output port B. Here is a brief overview of the 68HC11 ports and registers used by the SPI.

The 68HC11 has four I/O ports. Port D can be set up as a general purpose I/O port or it can be used for the SPI interface and SCI (Serial Control Interface). The signal assignments for port D when used for SPI or SCI follow:

PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
X	X	SS	SCK	MOSI	MISO	TXD	RXD

SS (Slave Select), SCK (Serial ClocK), MOSI (Master Output Slave Input), MISO (Master Input Slave Output) are used for the SPI. SCI uses TXD and RXD.

There are two registers in the 68HC11 that need to be initialized: the DDRD (Data Direction Register for port D) and the SPCR (Serial Peripheral Control Register).

4.0 68HC11 SPI Interface (Continued)

4.1.1 DDRD

If ones are placed in the locations corresponding to the signal assignments for port D, those signals will be selected as outputs (except for the SS location). A one placed in the SS location disables that function. The SS input can be used for synchronizing master/slave communications between 68HC11s on the SPI bus. If SS is enabled and the 68HC11 is set as master then the SS input should be hard wired to a logical "high" for our case. Shown below is the data required to initialize DDRD for the ADC12038 interface. SS is disabled; SCK and MOSI are set as outputs, MISO is set as an input. TXD and RXD are not used but are set as input and output.

PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
X	X	1	1	1	0	1	0

DDRD resides at address i009. On the 68HC11 development board this address is 1009. All register addresses on the development board start at 1000. 0000 through 0FFF are used by the software that controls the development board. In an actual system the registers can be remapped to any 4k boundary by software

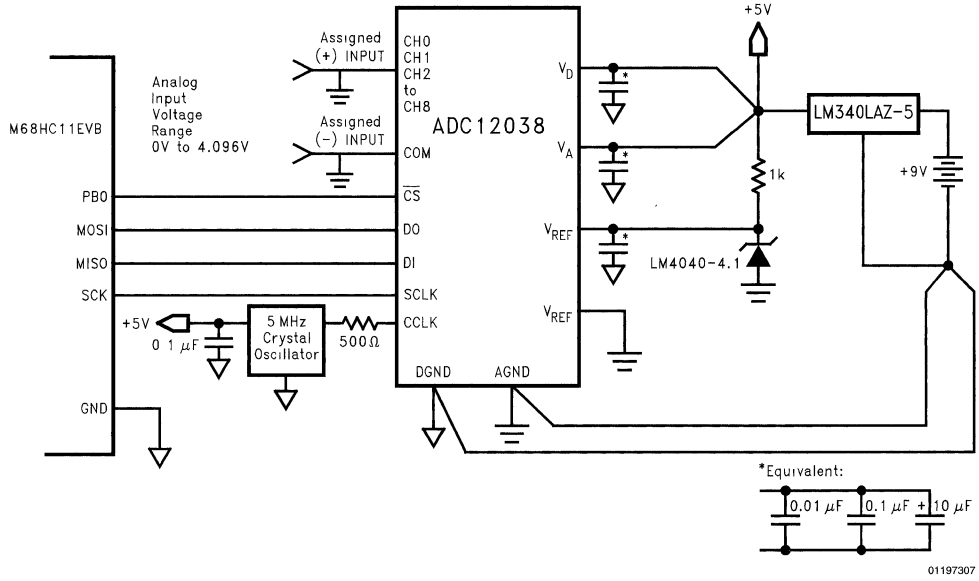


FIGURE 7. Detailed Schematic of ADC12038 to M68HC11EVB Interface

4.1.2 SPCR

On power up the SPI is disabled. The data stored in the SPCR (Serial Peripheral Control Register) controls how the SPI functions. SPCR resides at address 1028 for the development board. The table below summarizes the functions of the bits in this register. The SPIE (Serial Peripheral Interrupt Enable) bit when set to 1 allows the use of an interrupt to signal when an I/O exchange has completed. The SPE (Serial Peripheral Enable) bit when set to 1 enables the SPI. DWOM bit when set to 1 sets the outputs of port D to open drain. When this bit is low port D has totem pole outputs. MSTR bit controls whether this 68HC11 is a master or slave. When set to a 1 the 68HC11 is set as a master. In the slave mode SCK is an input. The CPOL and CPHA control the inactive level of the SCK output as well as which edge of the SCK output strobes the data out or in on the MISO or MOSI pins of port D. With both these bits set low the timing is as shown in *Figure 8*.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
0	1	0	1	0	0	0	0

The 68HC11 clocks in the data on MISO using the rising edge of SCK. Data on MOSI changes on the falling edge of SCK. This timing matches what the ADC12038 expects. SPR1 and SPR2 control the frequency of SCK as shown in *Table 9*.

4.0 68HC11 SPI Interface (Continued)

TABLE 9. SCK Frequency Control

XTAL Frequency	Internal Processor Clock	SCK Frequency	Internal Processor Clock Divide by	SPR1	SPR0
8 MHz	2 MHz	1 MHz	2	0	0
8 MHz	2 MHz	500 kHz	4	0	1
8 MHz	2 MHz	250 kHz	8	1	0
8 MHz	2 MHz	125 kHz	16	1	1

The SPSR (SPI Status Register) logs the status of the SPI I/O interchange. The only bit that is of concern is the SPIF which when set signals that the SPI interchange is complete.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
SPIF							

SPDR (SPI Data Register) is an 8-bit register used to exchange input and output data on the SPI. A write to this register will initiate an SPI exchange. The data input to the 68HC11 after an SPI exchange will reside in this register. This register resides at address 1029 for the development system.

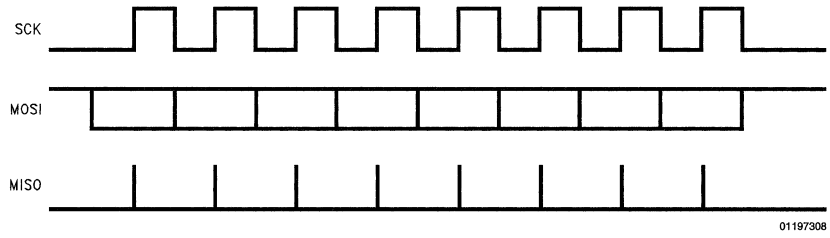


FIGURE 8. SPI Timing Diagram Required for the ADC12038

4.0 68HC11 SPI Interface (Continued)

4.2 68HC11 Program Listing

The following program listing follows the flow chart given in Section 2.0.

```
0001*****************************************************************************************
0002                        *       Emmy Denton                 3/4/93
0003                        *
0004                        *       ADC12'38 MC68HC11 SPI Interface
0005                        *
0006                        *
0007                        *       This program
0008                        *               1. Initializes the SPI interface
0009                        *               2. Starts a self calibration
0010                        *               3. Fills memory locations C200-C2FF with
0011                        *                conversions of CH0 and CH1 set up as single ended,
0012                        *                12-bit +sign MSB first
0013                        *
0014*****************************************************************************************
0015                        *
0016 0081                   CH0CONV EQU     %10000001       ADC DI FOR CH0 CONVERSION
0017 00c1                   CH1CONV EQU     %11000001       ADC DI FOR CH1 CONVERSION
0018 0008                   CAL     EQU     $08             ADC DI FOR CALIBRAITON
0019 000c                   STATUS  EQU     $0C             ADC DI FOR STATUS READ
0020 c1ff                   STARTDATA EQU   $C1FF           START ADDRESS - 1 FOR CONVERSION RESULTS
0021 c2ff                   ENDDATA EQU     $C2FF           END ADDRESS FOR CONVERSION RESULTS
0022 1009                   DDRD    EQU     $1009           DATA DIRECTION REGISTER ADDRESS
0023 1028                   SPCR    EQU     $1028           SPI CONTROL REGISTER ADDRESS
0024 1029                   SPSR    EQU     $1029           SPI STATUS REGISTER ADDRESS
0025 102a                   SPDR    EQU     $102A           SPI DATA REGISTER ADDRESS
0026 1004                   PORTB   EQU     $1004           PORT B ADDRESS
0027 1008                   PORTD   EQU     $1008           PORT D ADDRESS (SPI OUTPUT)
0028
0029
0030 c000                           ORG     $C000           STARTING ADDRESS OF PROGRAM*
0031
0032
0033
0034
0035
0036                        *******
0037                        *       INITIALIZE SPI INTERFACE PORT
0038                        *******
0039 c000 86 20                     LDAA    #$20
0040 c002 b7 10 08                  STAA    PORTD           SET SCK TO 0, MISO TO 0, SS TO 1
0041
0042 c005 86 3a                     LDAA    #$3A            SET DDRD: DISABLE SS; SCK, MOSI, TXD - OUTPUTS;
0043 c007 b7 10 09                  STAA    DDRD                      MISO,RXD - INPUTS.
0044                        *
0045 c00a 86 50                     LDAA    #$50            SET SPCR
0046 c00c b7 10 28                  STAA    SPCR
0047
0048
0049
0050
0051
0052                        *******
0053                        *       INITIALIZE PORT B AND X INDEX REGISTER
0054                        *******
0055 c00f f6 10 04                  LDAB    PORTB           PLACE PORT B DATA INTO ACC B
0056 c012 ca 01                     ORAB    #$01            (BIT 0 OF PORT B IS ADC CS) SET CS OF ADC HIGH
0057 c014 f7 10 04                  STAB    PORTB
0058 c017 ce c1 ff                  LDX     #STARTDATA      SET X INDEX REGISTER TO START OF ADC DATA
0059                        *
0060
0061
0062
0063                        *
```

01197309

4.0 68HC11 SPI Interface (Continued)

```
0064                    *******
0065                    *       ADC MAIN PROGRAM
0066                    *******
0067                    *
0068
0069 c01a 86 08         MAIN    LDAA    #CAL
0070 c01c bd c0 53              JSR     EBWRADC         ACC A JUNK START CALIBRATION
0071 c01f 86 0c                 LDAA    #STATUS         READ STATUS
0072 c021 bd c0 53              JSR     EBWRADC         JUNK IN ACCUMULATOR
0073                    *
0074 c024 86 0c         CALWAIT LDAA    #STATUS
0075 c026 bd c0 53              JSR     EBWRADC         READ ADC STATUS
0076 c029 84 20                 ANDA    #$20            MASK STATUS BIT
0077 c02b 26 f7                 BNE     CALWAIT         IF Z=1 JUMP TO CALWAIT
0078                    *
0079 c02d 86 81                 LDAA    #CH0CONV
0080 c02f bd c0 53              JSR     EBWRADC         START CH0 CONVERSION DO IS JUNK
0081                    *
0082                    *
0083 c032 86 c1         CONV    LDAA    #CH1CONV        START CH1 CONVERSION
0084 c034 bd c0 6e              JSR     SBWRADC
0085
0086 c037 08                    INX
0087 c038 a7 00                 STAA    0,X             STORE CH0 DATA
0088 c03a 08                    INX
0089 c03b e7 00                 STAB    0,X
0090
0091 c03d 86 81                 LDAA    #CH0CONV        START CH0 CONVERSION
0092 c03f bd c0 6e              JSR     SBWRADC
0093
0094 c042 08                    INX
0095 c043 a7 00                 STAA    0,X             STORE CH1 DATA
0096 c045 08                    INX
0097 c046 e7 00             STAB 0,X
0098
0099 c048 8c c2 ff              CPX     #ENDDATA        IS MEMORY FOR DATA FULL
0100 c04b 26 e5                 BNE     CONV            IF NOT DO ANOTHER 2 CONVERSIONS
0101 c04d ce c1 ff              LDX     #STARTDATA
0102 c050 01                    NOP
0103 c051 01                    NOP
0104 c052 01                    NOP
0105                    *
0106                            END
0107
0108
0109
0110
0111                    *******
0112                    *       EBWRADC - Subroutine to Output/Input 8 bits to/from ADC (SPI port)
0113                    *       UPON ENTERING SUBROUTINe - ACCUMULATOR A HAS DATA TO OUTPUT TO ADC
0114                    *       UPON EXITING SUBROUTINE - ACCUMULATOR A HAS DATA FROM ADC
0115                    *******
0116 c053 f6 10 04      EBWRADC LDAB    PORTB           READ PREVIOUSE SETTING OF PORTB
0117 c056 c4 fe                 ANDB    #$FE            SET CS LOW (BIT 0 OF PORTB)
0118 c058 f7 10 04              STAB    PORTB
0119 c05b b7 10 2a              STAA    SPDR            WRITE ACCUMULATOR A TO SPI PORT AND READ SPI
0120
0121 c05e b6 10 29      SPIWTA  LDAA    SPSR            WAIT FOR SPI INTERFACE
0122 c061 84 80                 ANDA    #$80            AND RESET SPI FOR ANOTHER TIMING SEQUENCE
0123 c063 27 f9                 BEQ     SPIWTA
0124
0125 c065 b6 10 2a              LDAA    SPDR            LOAD SPI DATA INTO ACCUMULATOR A
0126 c068 ca 01                 ORAB    #$01            SET CS HIGH
0127 c06a f7 10 04              STAB    PORTB
0128 c06d 39                    RTS
0129
0130
0131
0132
```

01197310

4.0 68HC11 SPI Interface (Continued)

```
0133                    *
0134                    *******
0135                    *       SBWRADC - Subroutine to Output/Input 16 bits to/from ADC (SPI port)
0136                    *       UPON ENTERING SUBROUTINE - ACCUMULATOR A and B HAVE DATA TO OUTPUT TO ADC
0137                    *       UPON EXITING SUBROUTINE - ACCUMULATOR A AND B HAVE DATA FROM ADC
0138                    *******
0139
0140
0141 c06e f6 10 04      SBWRADC LDAB    PORTB           READ PREVIOUS SETTING OF PORTB
0142 c071 c4 fe                 ANDB    #$FE            SET CS LOW (BIT 0 OF PORTB)
0143 c073 f7 10 04              STAB    PORTB
0144 c076 b7 10 2a              STAA    SPDR            WRITE ACCUMULATOR A TO SPI PORT AND READ BYTE 1
0145
0146 c079 b6 10 29      SPIWTB  LDAA    SPSR            WAIT FOR SPI INTERFACE
0147 c07c 84 80                 ANDA    #$80            AND RESET SPI FOR ANOTHER TIMING SEQUENCE
0148 c07e 27 f9                 BEQ     SPIWTB
0149
0150 c080 f6 10 2a              LDAB    SPDR            LOAD SPI DATA (BYTE 1) INTO ACCUMULATOR B
0151 c083 b7 10 2a              STAA    SPDR            WRITE ACCUMULATOR A TO SPI PORT AND READ BYTE 2
0152
0153 c086 b6 10 29      SPIWTC  LDAA    SPSR            WAIT FOR SPI INTERFACE
0154 c089 84 80                 ANDA    #$80            AND RESET SPI FOR ANOTHER TIMING SEQUENCE
0155 c08b 27 f9                 BEQ     SPIWTC
0156
0157 c08d b6 10 04              LDAA    PORTB           SET CS HIGH
0158 c090 8a 01                 ORAA    #$01
0159 c092 b7 10 04              STAA    PORTB
0160 c095 b6 10 2a              LDAA    SPDR            LOAD SPI DATA (BYTE 2) INTO ACCUMULATOR A
0161
0162 c098 39                    RTS
0163                    *
```

01197311

5.0 References

National Serniconductor Microcontroller Databook

Motorola MC68HC11 Reference Manual
#M68HC11RM/AD

Motorola MC68HC11A8/1/0 Data Sheet

"Design with Microcontrollers" John B. Peatman

Intel 8051 Databook

Tiny Temperature Sensors for Portable Systems

National Semiconductor
Application Note 1256

The last year has seen the introduction of silicon temperature sensors in revolutionary small packages, ideal for portable systems. This brief will discuss trade-offs in accuracy, as well as how to choose between thermistors and analog output IC temperature sensors. *Figure 1* shows the output voltage transfer function of various analog output temperature sensors. These sensors are available in tiny packages like the SC70 and the 4-bump micro SMD. The LM20 is the smallest, lowest power (10µA max) analog output temperature sensor National Semiconductor has released and is available in the SC70 and micro SMD packages. The LM70 and LM74 are MICROWIRE/SPI compatible digital temperature sensors and are available in the LLP and 8-bump micro SMD packages, respectively. The LM70 and LM74 have resolutions of 0.125°C and 0.0625°C, respectively. The LM74 is the most accurate of the two, with an accuracy of better than ±1.25°C.

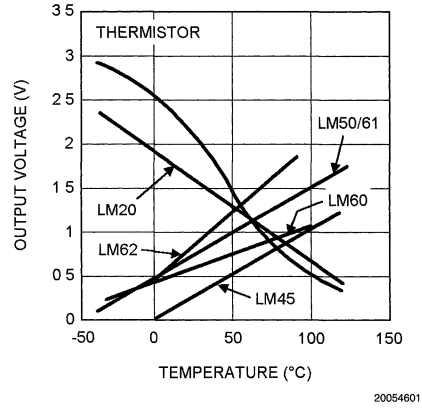


FIGURE 1. Comparison of analog temperature sensors to thermistors

The curves shown in *Figure 1* compare the temperature-to-voltage transfer functions of silicon temperature sensors with that of an NTC thermistor.

Thermistors come in a variety of packages ranging from probes to beads. However ICs have surface mount packaging equivalent to thermistors, as in the LM20 micro SMD.

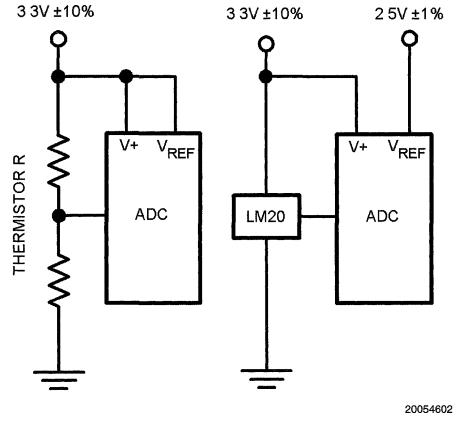


FIGURE 2. Connecting a thermistor or an LM20 to an ADC

Thermistors, when biased ratiometrically (as shown in *Figure 2*), have the advantage of not requiring an accurate or stable voltage reference in the system. In ratiometric operation, the error introduced by the reference is cancelled out. If ratiometric operation is not possible, for instance when the ADC reference voltage is in an ASIC and is not pinned out, using ICs like the LM20 will result in better total system accuracy. The LM20 draws only 10µA of current while the current drawn by the thermistor circuit depend on the value of R.

We analyzed a specific thermistor, the Murata NTH5G10P/16P33B103F. This thermistor has an accuracy of 1% at 25°C. The evaluation used ADCs with various resolutions to examine the overall system accuracy which depends on the resolution of the ADC, the ADC's errors (gain, offset and nonlinearity or TUE, total unadjusted error) and the resolution of the compensation table.

Figure 3 shows the voltage applied at the ADC input for the thermistor circuit shown in *Figure 2*. Note that the ADC input voltage decreases logarithmically with increasing temperature. The 97.6k resistor optimizes the power dissipation

(30µA) in the thermistor. It allows the thermistor to operate at a power level not exceeding its maximum power rating while maintaining specified accuracy.

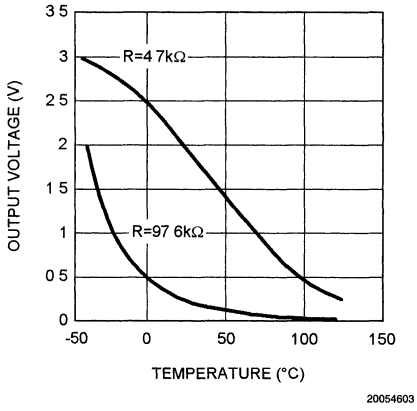


FIGURE 3. Thermistor output voltage vs. temperature for different values of R

Lowering the value of R will increase the temperature range over which the thermistor's transfer function is linear. With a 4.7k bias resistor, the slope at higher temperatures increases, providing more resolution, at the cost of greater power consumption (600µA)

Figure 4 compares the overall system accuracy when using a thermistor with an 8-bit ADC and R=100k, a thermistor with a 10-bit ADC and R=33k, or an LM20 with an 8-bit ADC. The quantization error and ADC Total Unadjusted Error (a combination of offset, gain and linearity errors) was considered to determine the overall system accuracy. The black lines show the min/max system performance of the LM20 superimposed over the blue min/max performance of the thermistor. Overall system accuracy for the LM20 remains constant over temperature. At temperatures above 60˚C the LM20 wins big when compared to the performance of the thermistor and 8-bit ADC!

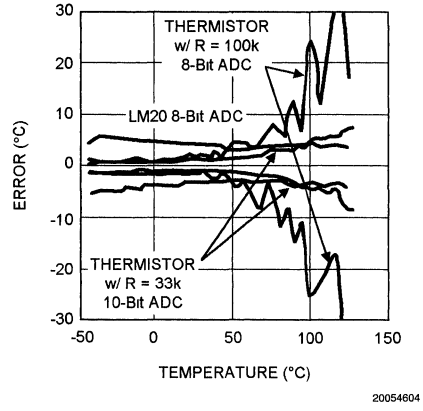


FIGURE 4. Comparison of Thermistor to LM20 System Performance

Increasing the ADC resolution and decreasing the value of R in the thermistor circuit decreases the overall system error. Improving the accuracy of the voltage reference will bring the LM20 system accuracy closer to that of the specifications found on the LM20 data sheet of ±2.5˚C at +130˚C and −55˚C, and ±1.5˚C at +30˚C. Since the output slope of the LM20 is negative, the gain error introduced by the reference voltage plays less of a role in the overall accuracy as the temperature increases, thus the slight negative slope of the LM20 performance.

Designers have numerous options for sensing temperature. Most common are thermistors, RTDs, thermocouples, and active silicon sensors. IC sensors have major advantages when the temperatures to be measured fall within the normal operating temperature range of silicon ICs. Among these advantages are low system cost, small size, and fast design time (because external signal conditioning circuitry is either minimal or not required). ICs can include extensive additional functions, such as built-in trip-point comparators or digital I/O. Since they include on-chip linearity correction when needed, there is no need for lookup tables to correct linearity errors.

Autonomous Fan Control for Processor Systems Using the LM85

National Semiconductor
Application Note 1260
Emmy Denton

To lower cost, many embedded processor systems include a hardware monitor for rudimentary system diagnostics. This helps ensure that the right person is sent to fix the problem with proper replacement parts. The system diagnostics include detection of power supply over/under voltage, system fan malfunction, and system component overheating.

Many processor systems require fans because of the heat produced by the processor and other components. The noise from these fans can be a nuisance to users. Many methods can be used to control noise level, the most obvious being controlling the fan speed.

The LM85 hardware monitor includes three PWM outputs that can be used to control fan drive circuitry. In addition, the LM85 features the ability to monitor five different power supply voltages, four fan tachometer outputs, and one set of processor voltage regulator module VID outputs.

The PWM outputs can be automatically controlled using three different temperature zones. The temperature of two of these zones is sensed by two remote thermal diode connected transistors, while the third zone is the LM85 die temperature.

A system error can be determined by polling the LM85's status registers. The LM85 includes high and low-limit registers for all measured values. Comparison of a measured value with its high and low-limit automatically sets or clears a bit in the status register.

Figure 1 shows the typical connection of an LM85 in a system. The LM85 communicates with the system using a simple 2-wire serial interface that is compatible with the SMBus 2.0 interface. Note that one of the remote thermal diodes is on the processor die. This diode is the parasitic PNP found in all CMOS processes. This particular one has been characterized to work with the LM85. The diode thermal sensor can be implemented on any CMOS ASIC and made to work after careful characterization of the thermal diode.

For more information on the error sources when using diode thermal sensors see the archived seminar titled "Thermal Management for High-Performance Processor Systems" found at: **http://www.national.com/onlineseminar/.**

The PWM fan drive uses a simple 2N2222 NPN transistor. Since the LM85 has four tach inputs and only three PWM outputs, PWM3 is shared by two fans.

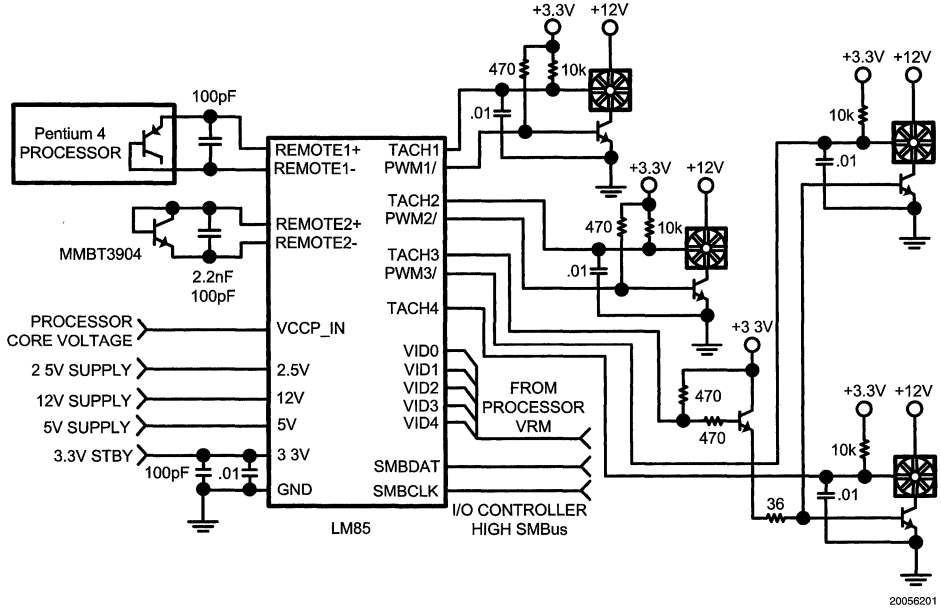


FIGURE 1. Typical LM85 Connection

The only drawback of this circuit is that the voltage drop across the 2N2222 in saturation will cause a lower maximum speed on the fan because the fan will not see a full 12V. This can be improved by replacing the bipolar transistor with a MOSFET, but then the cost goes up. Placing a slightly larger fan in the system is another solution, and it will also lower the noise generated by the fan. Another issue crops up when trying to monitor the speed when using the fan's tachometer output. Chopping the power supply of the fan with the PWM output can also distort the tach signal, particularly at the high PWM frequencies and/or low duty cycles. Since the GND will be going to a very high impedance when the 2N2222 is turned off, at high PWM frequencies and/or low duty cycle the tachometer signal will get distorted. *Figure 2* shows what happens when the PWM frequency is too high. The top trace shows the PWM collector base drive of the 2N2222. The bottom trace is the fan's tachometer output.

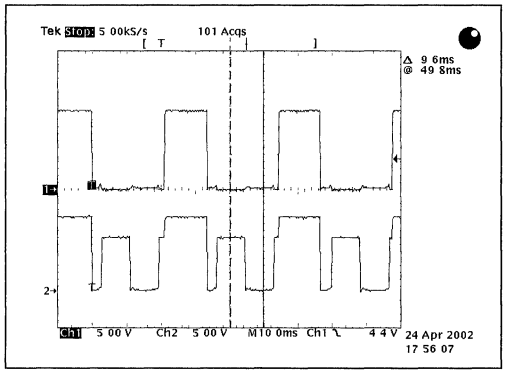


FIGURE 2. Fan Tachometer Output with PWM Fan Speed Control

The LM85 has two techniques for overcoming this problem. For example, when using a 30 Hz PWM frequency the minimum accurate speed that can be measured is approximately 2500 RPM. With the LM85's special circuitry, this is extended much lower, to approximately 420 RPM.

The LM85's autonomous fan control is based on a linear relationship between the measured temperature and a PWM output. The registers that are used for fan control are shown in *Figure 3.* The Fan Temp Limit sets the temperature at which the PWM output will start to increase. The Range sets the temperature at which 100% PWM is achieved. The PWM will change linearly from a minimum (set at Fan Temp Limit) to 100% (at Fan Temp Limit + Range). As temperature decreases, the PWM output will be at the minimum setting when the temperature reading is less than (Fan Temp Limit – Hysteresis). The minimum PWM can be set to any level. When the Absolute Limit is exceeded, the other two PWM outputs will be set to 100% duty cycle. Each PWM output can be assigned to any temperature zone, the hottest of one, two, or all three.

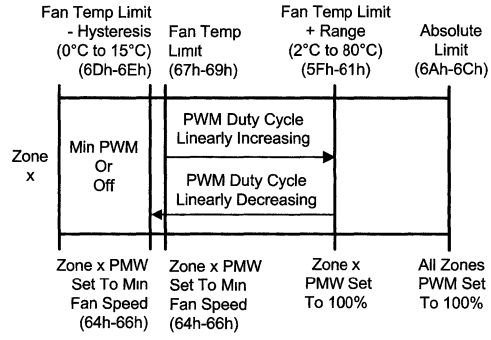


FIGURE 3. LM85 Fan Control Registers

Power Supply Effects on Noise Performance

National Semiconductor
Application Note 1261
Nicholas Gray

Understanding the PSRR (Power Supply Rejection Ratio) of analog circuits is an important step to improving overall mixed-signal system performance. Once you know the effects of PSRR, you can compensate for them. The fact is that the PSRR of analog circuits, including ADCs (Analog-to-Digital Converters), DACs (Digital-to-Analog Converters) and op amps, is usually much worse at high frequencies than the DC PSRR generally seen on data sheets.

Why the Apparent Discrepancy?

The reason for the apparent discrepancy is the fact that most products' PSRR specification indicates the variation in a particular parameter for a given change in DC power supply voltage. For example, an ADC may specify the PSRR as the ratio of the change in full-scale gain or offset error with a given change in the DC supply voltage, usually expressed in dB. If a change in supply voltage from 4.75V to 5.25V (a 500mV delta) results in a change in the full-scale ADC gain error of 0.6mV, the PSRR is found to be

$$\text{PSRR} = 20 \bullet \log\left(\frac{\Delta \text{ Gain Error}}{\Delta \text{ Supply}}\right) = 20 \bullet \log\left(\frac{0\,6}{500}\right) = -58\text{dB}$$

That is, the difference in gain error is determined by taking two gain error measurements. One reading is taken with a stable, noise-free supply of 4.75V and the other is with a stable, noise-free supply of 5.25V. This information only shows how this one specified parameter can be expected to change with individual power supply variations. However, other parameters may have more or less sensitivity to noise on the power supply, so the usefulness of such a specification is questionable.

Generally, the PSRR of an active component will be worse with an AC signal riding on its supply than it will be with a change of the power supply's DC level.

Why the Low AC PSRR

Any signal or noise on the supply lines will couple into the active circuitry through the stray capacitances and gain of the bias network and be amplified by the active circuitry on the die. These unwanted signals are noise and, therefore, degrade the device's noise performance. *Figure 1* shows a simplified amplifier stage with stray capacitances. Actual circuits use many techniques to improve PSRR, but no analog circuit is totally immune to supply noise.

One source of power supply noise comes from the output switching of an ADC. The change of output states will cause supply current transients as the output drivers charge the capacitance on the output pins.

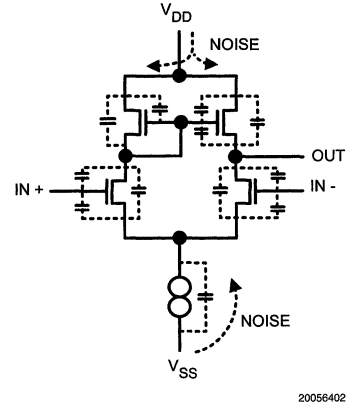


FIGURE 1. Supply noise can couple into the active circuitry of a device and degrade its performance

Without adequate supply bypassing, these current transients will cause voltage fluctuations on the supply line. The resulting high frequency noise on the supply line causes noise in the bias circuitry, which further degrades the SNR of the ADC.

PSRR Variation with Frequency

Figure 2 shows a plot of AC PSRR for the ADC12040 (a 12-bit, 40Msps ADC) vs. supply noise frequency. The test data for this plot was gathered by injecting 200mV_{P-P} of the noise at various frequencies onto the power supply lines of the ADC and using an FFT plot to measure the magnitude of this signal at the output of the ADC.

With 38dB AC PSRR at 30MHz, the ADC12040's performance is actually quite good. Analog components often have PSRRs in the 10 to 20 dB range at these frequencies.

PSRR Variation with Frequency

(Continued)

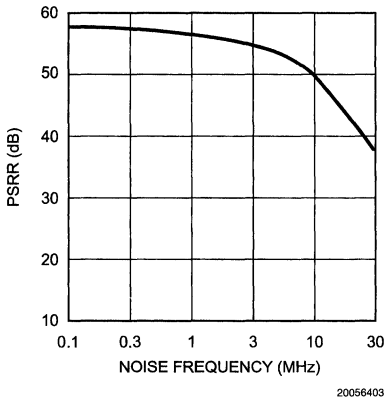


FIGURE 2. Plot of PSRR vs. supply noise frequency for the ADC12040

Minimizing Noise Problems

To minimize the effects of noise on the power supply, the analog and digital supply pins should be separately decoupled for both high and low frequencies. Typically, a parallel combination of a 10µF capacitor and a 0.1µF monolithic capacitor will suffice. The optimum values may vary with the particular IC selected and the frequency of operation, so be sure to follow the manufacturer's recommendations. Additionally, for mixed-signal products such as ADCs, it is good practice to bring the power directly to the analog supply pins first, then to the digital supply pins through a choke. For high-speed ADCs, a ferrite choke with 2.5 turns will do well. The choke usually only needs to isolate the output driver pins from the other supply pins. If the output driver supply pins are not explicitly shown on the data sheet, isolate all of the digital supply pins. In any case, the analog and digital supply pins of a mixed signal device should have separate bypass capacitors as shown in *Figure 3*.

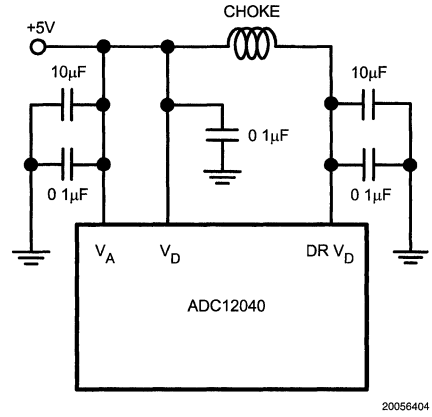


FIGURE 3. Separately bypass the power supply at both low and high frequencies. Isolate digital output driver supply line with a small choke. A ferrite choke with 2.5 turns will do well.

Power supply noise can be further reduced by keeping the analog power plane over the analog ground plane, when a split ground plane is used, or by routing the power trace away from any digital components when a single ground plane is used.

Finally, as popular as they are for their efficiency, the noise generated by switching power supplies can wreak havoc with mixed signal components. If it is necessary to have a switching supply in the system, be sure to lay it out for minimum RFI/EMI and keep it as far away from analog and mixed signal areas of the system as possible.

Four-Speed Fan Control Using Simple Remote Diode Temperature Sensor

National Semiconductor
Application Note 1262

The circuit shown in *Figure 1*controls the speed of a 12V DC fan using an LM88 Remote Diode Temperature Sensor (RDTS) IC. The LM88 is a dual remote diode temperature sensor with 3 digital comparators and has 3 open-drain outputs (O_SP0, O_SP1 and O_CRIT) that can be used as interrupts or to signal system shutdown. The digital comparators can be programmed independently to make a greater than or less than comparison. When programmed for a greater than comparison:

• O_SP0 and O_SP1 activate when the temperatures measured by D0 or D1 exceed the associated setpoints of T_SP0 or T_SP1.

• O_CRIT activates when the temperature measured by either D0 or D1 exceeds set point T_CRIT.

T_CRIT can be set at 1°C intervals from -40°C to +125°C. T_SP0 and T_SP1 can be set at 4°C intervals in the range of T_CRIT, ±100°C.

In the circuit shown in *Figure 1* the two D+ inputs have been wired in parallel to allow all three set points to be evaluated against a single temperature measurement. The hysteresis of each comparator is internally set to 1°C, allowing the set point values to be placed very close together without any interaction. The three outputs of the LM88 are connected to resistors forming a crude 2-bit DAC. The output of this DAC is fed to a PNP emitter follower, controlling the voltage on the negative pin of the fan from 1.25V to 5.7V. The output voltage (V_{OUT}) decreases as the temperature reading increases, when SP0<SP1<CRIT.

The equations shown in *Figure 1* describe the behavior of V_{OUT} . The maximum speed of the fan is dependent on the minimum V_{OUT} . The minimum V_{OUT} is dependent on the drain to source on resistance (Rds) of the O_CRIT output, the MPSW51's beta and base emitter voltage when R5 is set to 0Ω (as shown in *Figure 1*). The MPSW51 beta variation will introduce an error term that cannot be accounted for. Therefore, it is tempting to make the current through the resistors as high as possible. Increasing this current is a "Catch 22", because the minimum V_{OUT} level will increase as the current increases, because of O_CRIT's Rds that is typical 100Ω and worst case .4V/3 mA = 133Ω. A compromise would be to set this current 10 times the MPSW51 base current.

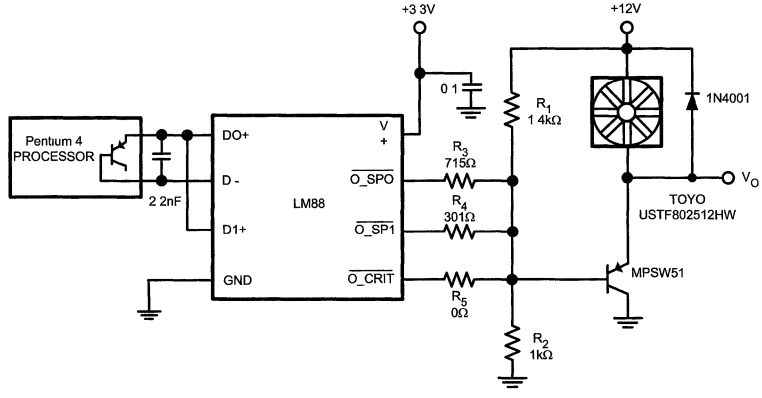
O_SP0, O_SP1 and O_CRIT have a maximum voltage limit of 5V. This sets the ratio of R2/(R2+R1) = 5/12 = 0.41666.

The current through R1 and R2 should be set such that the base current of the MPSW51 is negligible. The current through the fan with (12 - 5.7) 6.3V is about 65mA or so. That makes the base current about 65mA/130 = 0.5 mA. Since the beta will vary slightly as the collector current changes, it's best to set the current through R1/R2 ten times greater than 0.5 mA. Therefore:

(R1+R2)= 12V/5mA = 2400Ω

Since R2/(R2+R1)=5/12

R2= (5/12)*(2400)=1000Ω and R1=1400Ω



If TD < SP0 V_{OUT}min = 5 7V (fan min on)

If TD < SP1 V_{OUT}int1 = ((Rp23/(R1+Rp23))12V)+0 7V=3.61V

If TD < CRIT V_{OUT}int2 = ((Rp234/(R1+Rp234))12V)+0 7V=2 28V

If TD < CRIT V_{OUT}max = ((Rp2345/(R1+Rp2345))12V)+0 7V=1 25V

where SP0<SP1<CRIT and TD=diode temperature, see text for values of Rp23, Rp234 and Rp2345

FIGURE 1. Low Cost Remote Diode Temperature Fan Speed Control

When the temperature of the diode is less than the SP0, SP1 and T_CRIT set points, all of the LM88's outputs will be deactivated. Therefore, V_{OUT} will be set to approximately 5.7V. This will set the slowest speed of the fan.

The first intermediate fan speed will be set when only O_SP0 is activated. This happens when the temperature measured is greater than the SP0 set point but less than the SP1 and CRIT set points. For this case the following equations set V_{OUT}:

Rp23 = (R3+Rds)||R2 = 1/(1/(R3+Rds)+1/R2)

V_{OUT}int1 = ((Rp23/(R1+Rp23))12V)+0.7V

Therefore, If Rds = 100Ω typical, then with R3 = 715Ω, V_{OUT}= 3.614V making the voltage across the fan equal to 12V - 3.614V = 8.386V.

The second intermediate speed of the fan will be set when both O_SP0 and O_SP1 are activated. This happens when the temperature measured is greater than both the SP0 and SP1 set points but less than the CRIT set point. For this case the following equations set V_{OUT} :

Rp234=(R3+Rds)||(R4+Rds)||R2 =

1/(1/(R3+Rds)+1/(R4+Rds)+1/R2)

V_{OUT}int2 = ((Rp234/(R1+Rp234))12V)+0.7V. If R3 = 715Ω and Rds = 100Ω (typical) setting R4 to 301Ω will give a V_{OUT}= 2.277 V making the voltage across the fan equal to 12V-2.277V= 9.723V.

The fourth, and maximum, speed of the fan will be set when all three outputs O_CRIT, O_SP0 and O_SP1 are activated. This happens when the temperature measured is greater than all three set points. For this case the following equations set V_{OUT}:

Rp2345 = (R5+Rds)||(R4+Rds)||(R3+Rds)||R2 =

1/(1/(R5+Rds)+1/(R4+Rds)+1/(R3+Rds)+1/R2)

V_{OUT}max = ((Rp2345/(R1+Rp2345))12V)+0.7V. If R3 = 715Ω, R4 = 301Ω and Rds = 100Ω (typical) setting R5 to 0Ω will give V_{OUT} = 1.255V making the maximum voltage across the fan equal to 12V-1.255V=10.775V.

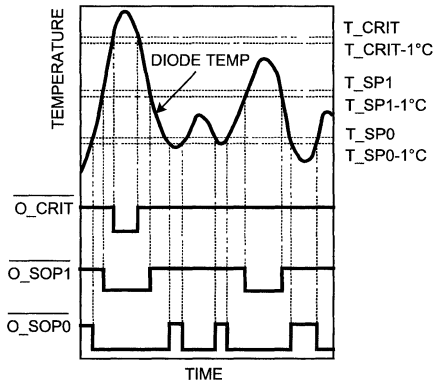


FIGURE 2. Temperature Response Diagram Of The LM88's Outputs

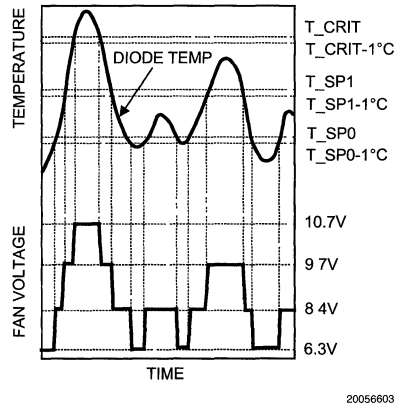


FIGURE 3. Fan Voltage Temperature Response

Using 1% resistor values measurements were made and the measured V_{OUT} was within 3% of the calculated V_{OUT} voltage.

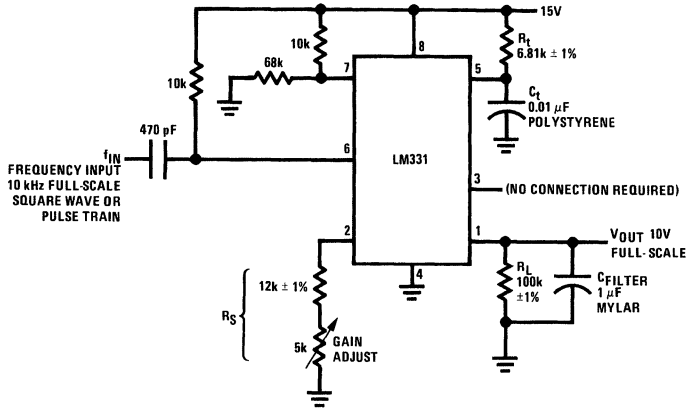
Figures 2 and 3 show the temperature response diagram of the LM88's outputs and the fan voltage. As the temperature increases the sequential activation of O_SP0 followed by O_SP1 and finally O_CRIT cause the voltage across the fan to increase.

Frequency-to-Voltage Converter Uses Sample-and-Hold to Improve Response and Ripple

National Semiconductor
Linear Brief 45

Most frequency-to-voltage (F-to-V) converters suffer from the classical tradeoff of ripple versus speed of response. For example, the basic F-to-V converter shown below has 13 mVp-p of ripple, and a rather slow 0.6 second settling time, when C_{FILTER} is 1 µF. If you want less ripple than that, the response time will be even slower. If you want quicker response, it is easy to decrease C_{FILTER}, but the ripple will increase by the same factor.

The improved circuit in *Figure 2* makes an end-run around these compromises. A low-cost sample-and-hold circuit such as LF398 can sample the F-to-V's output at the peak of its ripple, and hold it until the next cycle. The LF398 has fairly low output ripple (rms) but it does have some short duration noise spikes and glitches which can be removed easily with a simple output filter. The ripple at the output of the active filter V6 is smaller than 1 mV peak, but the settling time for a step change of input frequency is only 60 ms, or ten times quicker than the "basic" FVC with C_{FILTER} = 1 µF.



$$V_{OUT} = f_{IN} \times \left(\frac{R_L}{R_S}\right) \times (1.9V) \times (1.1R_tC_t)$$

$$\left(\begin{matrix}\text{output}\\ \text{ripple}\\ \text{p-p}\end{matrix}\right) = \left(\frac{1}{C_{FILTER}}\right) \times \frac{(1.9V) \times (1.1R_tC_t)}{R_S}$$

FIGURE 1. Basic Frequency-to-Voltage Converter

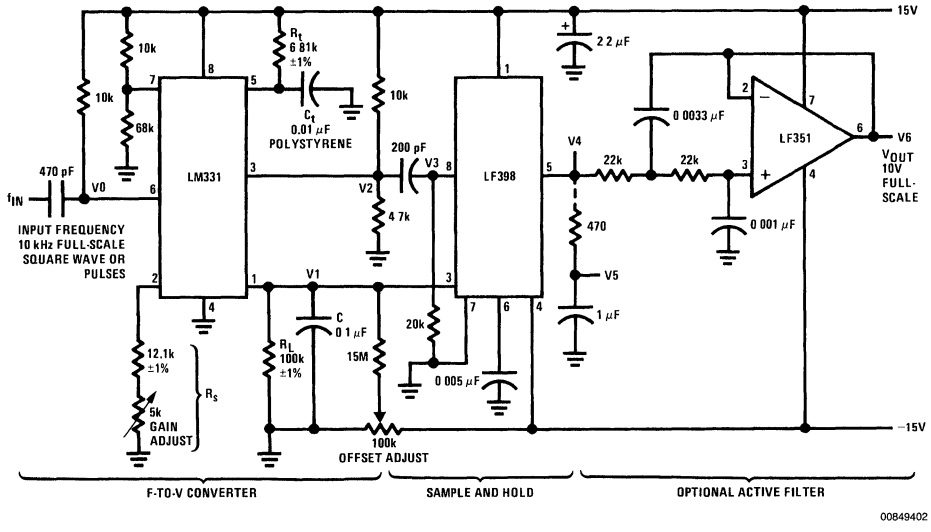


FIGURE 2. Improved F-to-V Converter Using Sample-and-Hold

Details of Operation

(Refer to *Figure 3*, Waveforms)

When the input frequency waveform has a negative-going transition, pin 6 of the LM331 is driven momentarily lower than the 13V threshold voltage at pin 7. This initiates a timing cycle controlled by the R_t and C_t at pin 5, and also causes a transition from +5V to 0V at pin 3, (the normal VFC logic output) which is usually left unused in F-to-V operation.

During the timing cycle ($t = 1.1 \times R_t \times C_t = 75$ μs, for the example shown) a precision current source $i = 1.9\ V/R_S$ flows out of pin 1 of the LM331, and charges V1 up to a value slightly higher than the average DC value of V1. At the end of the timing cycle, V1 stops charging up, and also V2 rises. The 10 kΩ pull-up resistor is coupled (through the 200 pF capacitor) to V3, and causes the LF398 to *sample* for about 5 μs. Then the LF398 goes back into *hold*. This entire operation is repeated at the same frequency as f_{IN}. The average voltage at V1 will be the same 10V full scale, according to the same formula of *Figure 1*. And the peak-to-peak ripple can be computed as 65 mV peak, 130 mVp-p, using the appropriate formula.

Now, the input to the sample-and-hold at pin 3 may have a 10.000V average DC value, but the output will be at 10.065V, because the sample occurs at the peak value of V1. Thus, to get an output with low offset, a 15 MΩ resistor is used to offset the V1 signal to a lower level. Trim the offset adjust pot to get V_{OUT} = 1V at 1 kHz, and trim the gain adjust pot to get V_{OUT} = 10V at 10 kHz (the interaction is minor), as measured at V4, V5, or V6. The rms value of the ripple at V4 is rather small, but the peak-to-peak ripple (spikes and glitches) may be excessive. A simple R-C filter can provide a filtered output at V5; or a simple active filter using an inexpensive LF351, will give sub-millivolt (peak) ripple at V6, with improved settling time and low output impedance.

This F-to-V converter will have a good linearity, better than 0.1%, but only from 10 kHz down to 500 Hz. Between 200 Hz and 20 Hz, V_{OUT} is not very proportional to f_{IN}. And at 0 Hz, the output will be indeterminate, because the sample-and-hold will never sample! However, there are many F-to-V applications where a 20.1 frequency range is adequate.

Details of Operation (Continued)

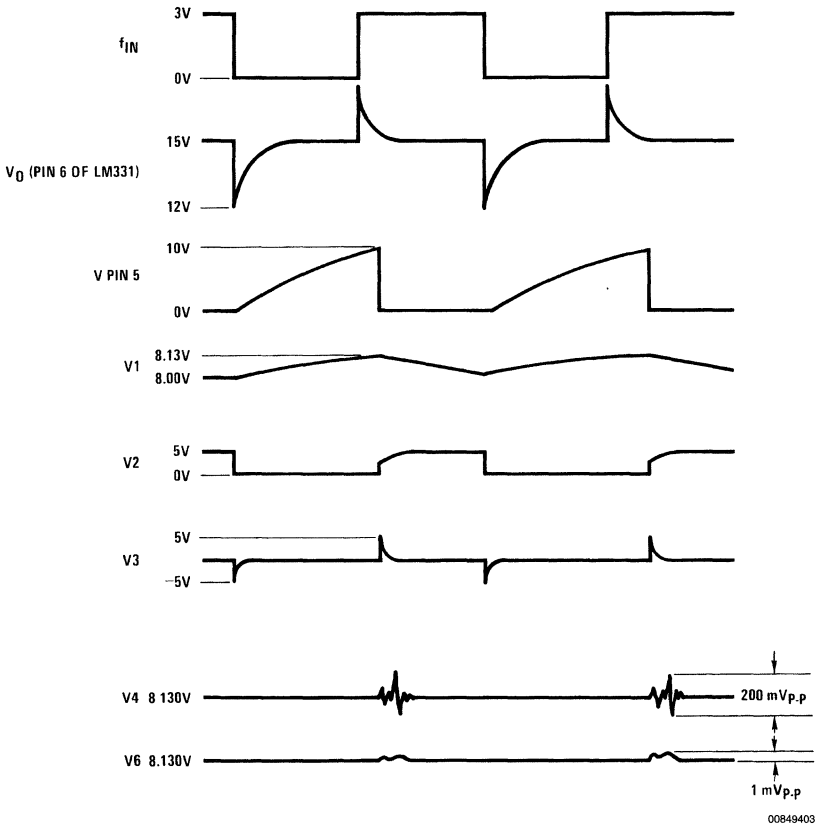


FIGURE 3. Waveforms, Improved F-to-V Converter

µP Interface for a Free-Running A/D Allows Asynchronous Reads

National Semiconductor
Linear Brief 53

In many data acquisition applications it is necessary to have an A to D converter operate as its maximum conversion rate. The controlling microprocessor would then be able to read the most current input data at *any* point in time as required by software To minimize program execution time, a DATA READ may not be synchronous to the completion of a conversion, and herein lies a problem. It is entirely possible that the processor could assert a READ command right at the instant the A/D converter is updating its output register. The data read would be the value of the converter's output lines in transition from the result of the previous conversion to the latest result, and would very likely be in error.

The addition of a simple binary counter to the A/D interface circuitry can be used to generate a READY signal to the microprocessor that will prevent a READ during a data update. The circuit of *Figure 1* shows a CD4024BC7-stage ripple carry binary counter used in conjunction with an ADC0801, 8-bit microprocessor compatible A to D converter. Circuit operation relies on two basic properties of the A/D converter. First of all, the free-running conversion time of the A/D must be a constant number of clock cycles; and secondly, the output latches must be updated prior to the end of conversion signal. The ADC0801 fulfills both of these requirements. The output data latches are updated one A/D clock period before the $\overline{INTR}$ falls low, and the free-running conversion time is always 72 clock periods long.

As part of the system power-up initialization sequence, a logic low must be temporarily applied to the $\overline{SYSTEM\ RESET}$ input to the A/D to force the converter to start. At the end of a conversion, the $\overline{INTR}$ output goes low, and both resets the counter outputs to all zeros and signals another conversion to start by pulling $\overline{WR}$ low. The length of time that the $\overline{INTR}$ output stays low is normally only a few internal gate propagation delays (approximately 300 ns) and is independent of the A/D clock frequency. The 1000 pF capacitor on this output extends this time to approximately 1 µs to insure adequate reset time for the counter.

A conversion is started on the low to high transition of the $\overline{INTR}$ and $\overline{WR}$ pins. The next data update will occur 71 clock periods after this edge occurs. The counter will signal that a data update is about to occur after 64 clock periods. If the processor attempts a DATA READ within an 8 clock period time frame around the data update time, its READY input line will remain low, signifying a NOT READY condition. The processor would then extend the READ cycle time until it receives a READY indication created by the counter being reset by $\overline{INTR}$. This insures that the latches have already been updated and proper data will be read.

If a READ is attempted during the 64 clock period interval after the start of a conversion, the READY IN line to the processor will go high to permit a normal READ cycle, and the data output by the A/D will be the result of the previous conversion. The processor READY IN logic, as shown, requires that all system devices that may need special READ or WRITE timing provide a NOT READY (a Logic 0 on their READY OUT lines) indication until selected to be read from or written to.

The chance of having the processor extend its READ cycle time is 1 in 9 (8 clock periods out of 72) and the maximum length of time a READ would be extended is 8 A/D clock periods. These two timing considerations are insignificant trade-offs to take to insure that proper A/D data is always read.

Timing Diagram

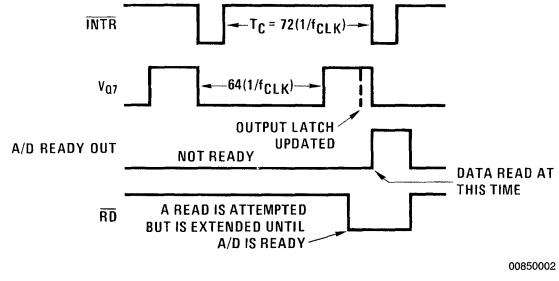
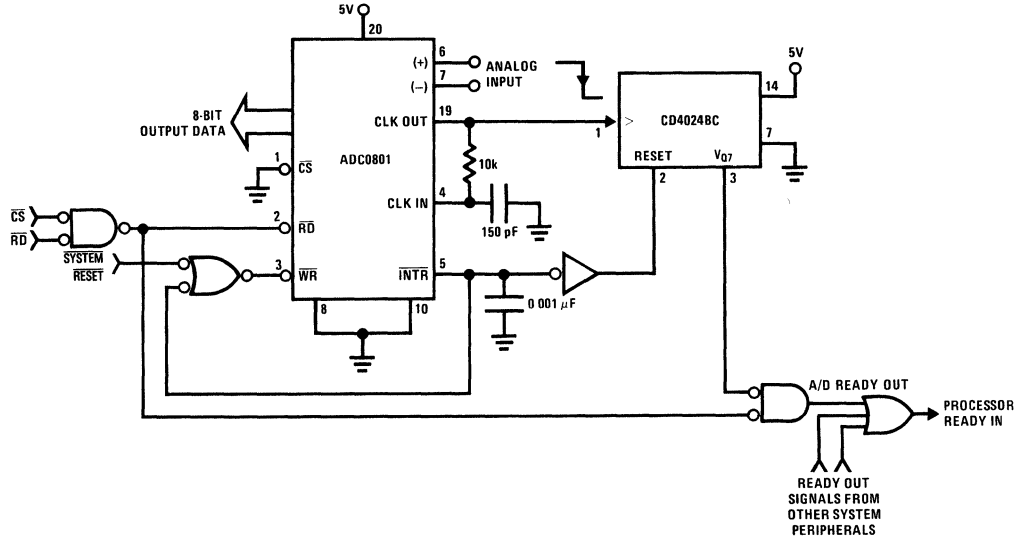


FIGURE 1.


5V
20
6
(+)
7
(−)
ANALOG
INPUT
8-BIT
OUTPUT DATA
CLK OUT
19
1
ADC0801
CS
1
10k
CLK IN
4
150 pF
RD
2
WR
3
INTR
5
8
10
0 001 μF
CS
RD
SYSTEM
RESET
CD4024BC
RESET
Q7
14
7
2
3
5V
A/D READY OUT
PROCESSOR
READY IN
READY OUT
SIGNALS FROM
OTHER SYSTEM
PERIPHERALS

00850001

V/F Converter ICs Handle Frequency-to-Voltage Needs

National Semiconductor
Application Note C
Robert A. Pease

Simplify your F/V converter designs with versatile V/F ICs. Starting with a basic converter circuit, you can modify it to meet almost any application requirement. You can spare yourself some hard labor when designing frequency-to-voltage (F/V) converters by using a voltage-to-frequency IC in your designs. These ICs form the basis of a series of accurate, yet economical, F/V converters suiting a variety of applications.

Figure 1 shows an LM331 IC (or LM131 for the military temperature range) in a basic F/V converter configuration (sometimes termed a stand-alone converter because it requires no op amps or other active devices other than the IC). (Comparable V/F ICs, such as RM4151, can take advantage of this and other circuits described in this article, although they might not always be pin-for-pin compatible).

This circuit accepts a pulse-train or square wave input amplitude of 3V or greater. The 470 pF coupling capacitor suits negative-going input pulses between 80 µs and 1.5 µs, as well as accommodating square waves or positive-going pulses (so long as the interval between pulses is at least 10 µs).

IC Handles the Hard Part

The LM331 detects an input-signal change by sensing when pin 6 goes negative relative to the threshold voltage at pin 7, which is nominally biased 2V lower than the supply voltage. When a signal change occurs, the LM331's input comparator sets an internal latch and initiates a timing cycle. During this cycle, a current equal to V_{REF}/RS flows out of pin 1 for a time $t = 1.1\ R_tC$. The 1 µF capacitor filters this pulsating current from pin 1, and the current's average value flows through load resistor R_L. As a result, for a 10 kHz input, the circuit outputs 10 V_{DC} across R_L with good (0.06% typical) nonlinearity.

Two problems remain, however: the output at V1 includes about 13 mVp-p ripple, and it also lags 0.1 second behind an input frequency step change, settling to 0.1% of full-scale in about 0.6 second. This ripple and slow response represent an inherent tradeoff that applies to almost every F/V converter

The Art of Compromise

Increasing the filter capacitor's value reduces ripple but also increases response time. Conversely, lowering the filter capacitor's value improves response time at the expense of larger ripple. In some cases, adding an active filter results in faster response and less ripple for high input frequencies.

Although the circuit specifies a 15V power supply, you can use any regulated supply between 4 V_{DC} and 40 V_{DC}. The output voltage can extend to within 3 V_{DC} of the supply voltage, so choose R_L to maintain that output range.

Adding a 220 kΩ/0.1 µF postfilter to the circuit slows the response slightly, but it also reduces ripple to less than 1 mVp-p for frequencies from 200 Hz to 10 kHz. The reduction in ripple achieved by adding this passive filter, while not as good as that obtainable using an active filter, could suffice in some applications.

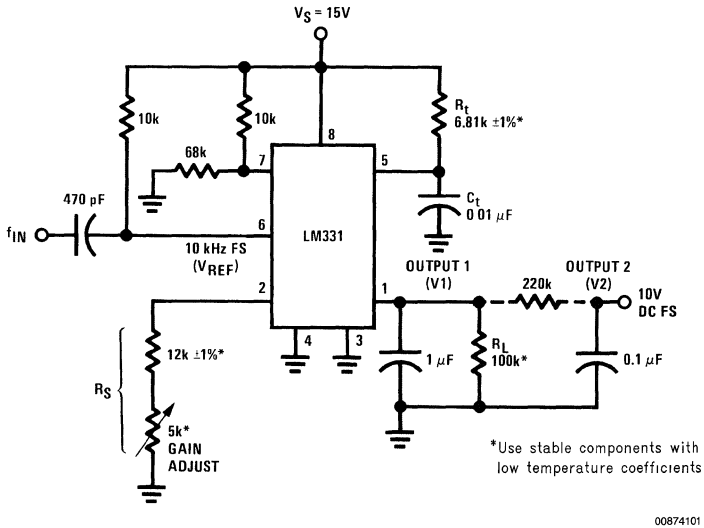


FIGURE 1. A Simple Stand-Alone F/V Converter Forms the Basis for Many Other Converter-Circuit Configurations

Improving the Basic Circuit

Further modifications and additions to the basic F/V converter shown in *Figure 1* can adapt it to specific performance requirements. *Figure 2* shows one such modification, which improves the converter's nonlinearity to 0.006% typical.

Reconsideration of the basic stand-alone converter shows why its nonlinearity falls short of this improved version's. At low input frequencies, the current source feeding pin 1 in the LM331 is turned off most of the time. As the input frequency increases, however, the current source stays on more of the time, and its own impedance attenuates the output signal for an increasing fraction of each cycle time. This disproportionate attenuation at higher frequencies causes a parabolic change in full-scale gain rather than the desired linear one.

In the improved circuit, on the other hand, the PNP transistor acts as a cascade, so the output impedance at pin 1 sees a constant voltage that won't modulate the gain. Also, with an alpha ranging between 0.998 and 0.990, the transistor exhibits a temperature coefficient of between 10 ppm/°C and 40 ppm/°C—a fairly minor effect. Thus, this circuit's nonlinearity does not exceed 0.01% maximum for the 10V output range shown and is normally not worse than 0.01% for any supply voltage between 4V and 40V.

Add an Output Buffer

The circuit in *Figure 3* adds an output buffer (unity-gain follower) to the basic single-supply F/V converter. Either an LM324 or LM358 op amp functions well in a single-supply circuit because these devices' common-mode ranges extend down to ground. But if a negative supply is available, you can use any op amp; types such as the LF351B or LM308A, which have low input currents, provide the best accuracy.

The output buffer in *Figure 3* also acts as an active filter, furnishing a 2-pole response from a single op amp. This filter provides the general response

$$V_{OUT}/I_{OUT} = R_L/(1 + K1p + K2p^2).$$

(p is the differential operator d/dt.) As shown, R_L controls the filter's DC gain. The high frequency response rolls off at 12 dB/octave. Near the circuit's natural resonant frequency, you can choose the damping to give a little overshoot—or none, as desired.

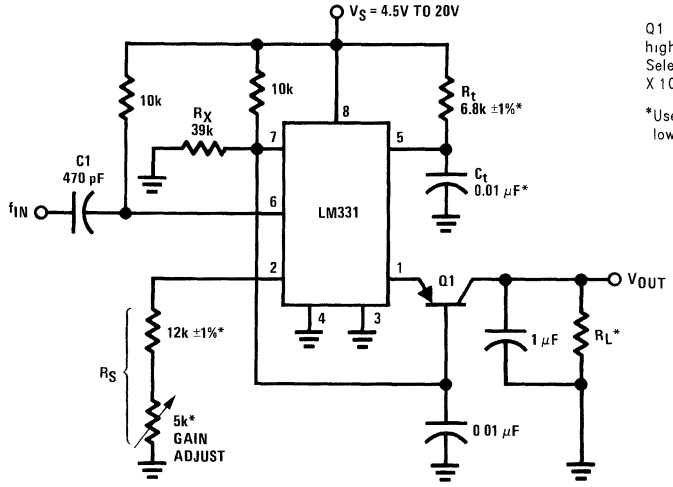


FIGURE 2. Adding a Cascade Transistor to the LM331's Output Improves Nonlinearity to 0.006%

Add an Output Buffer (Continued)

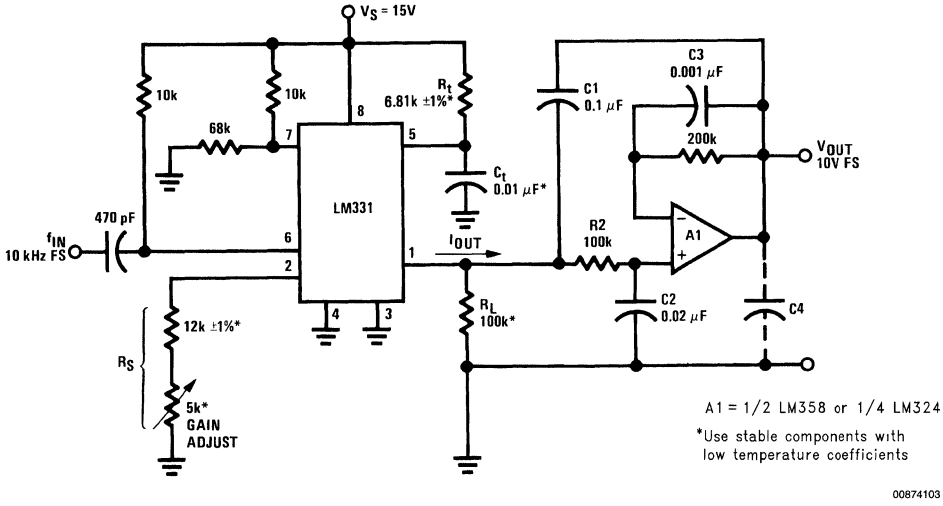


FIGURE 3. The Op Amp on This F/V Converter's Output Acts as a Buffer as Well as a 2-Pole Filter

Dealing with F/V Converter Ripple

Voltage ripple on the output of F/V converters can present a problem, and the chart shown in *Figure 4* indicates exactly how big a problem it is. A simple, slow, RC filter exhibits low ripple at all frequencies. Two-pole filters offer the lowest ripple at high frequencies and provide a 30-times-faster step response than RC devices.

To reduce a circuit's ripple at moderate frequencies, however, you can cascade a second active-filter stage on the F/V converter's output. That circuit's response also appears in *Figure 4* and shows a significant improvement in low-ripple bandwidth over the single-active-filter configuration, with only a 30% degradation of step response.

Figure 5 and *Figure 6* show filter circuits suitable for cascading. The inverting filter in *Figure 5* requires closely matched resistors with a low TC over their temperature range for best accuracy. For lowest DC error, choose R5 = R2 + (R_{IN}|R_F). This circuit's response is

$-V_{OUT}/V_{IN} = n/(1 + (R_F + R2 + nR2)C4p + R_FR2C3C4p^2)$.

where n = DC gain. If $R_{IN} = R_F$ and n = 1,

$-V_{OUT}/V_{IN} = 1/(1 + (R_F + 2R2)C4p + R_FR2C3C4p^2)$.

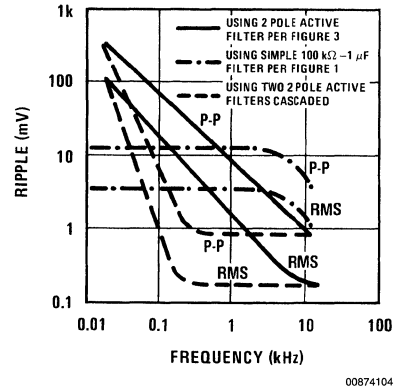


FIGURE 4. Output-Ripple Performance of Several Different F/V Converter Configurations Illustrates the Effect of Voltage Ripple

Dealing with F/V Converter Ripple

(Continued)

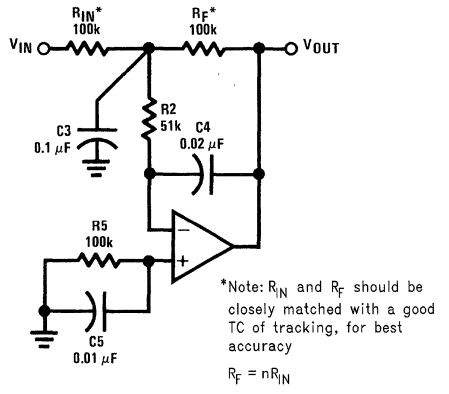


FIGURE 5. You Can Cascade This 2-Pole Inverting Filter onto an F/V Converter's Output

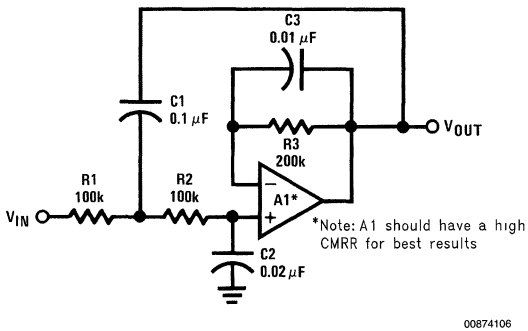


FIGURE 6. This 2-Pole Noninverting Filter Suits Cascade Requirements on F/V Converter Outputs

The circuit shown in *Figure 6* does not require precision passive components, but for best accuracy, choosing an A1 with a high CMRR is critical. An LM308A op amp's 96 dB minimum CMRR suits this circuit well, but an LM358B's 85 dB typical figure also proves adequate for many applications. Circuit response is

$V_{OUT}/V_{IN} = 1/(1 + (R1 + R2)\ C2p + R1R2C1C2p^2)$.

For best results, choose R3 = R1 + R2.

Components Determine Response

The specific response of the circuit in *Figure 3* is

$V_{OUT}/I_{OUT} = R_L/(1 + (R_L + R2)C2p + R_LR2C1C2C2p^2)$.

Making C2 relatively large eliminates overshoot and sine peaking. Alternatively, making C2 a suitable fraction of C1 (as is done in *Figure 3*) produces both a sine response with 0 dB to 1 dB of peaking and a quick real-time response having only 10% to 30% overshoot for a step response. By maintaining *Figure 3*'s ratio of C1:C2 and R2:R_L, you can adapt its 2-pole filter to a wide frequency range without tedious computations.

This filter settles to within 1% of a 5V step's final value in about 20 ms. By contrast, the circuit with the simple RC filter shown in *Figure 1* takes about 900 ms to achieve the same response, yet offers no less ripple than *Figure 3*'s op amp approach.

As for the other component in the 2-pole filter, any capacitance between 100 pF and 0.05 µF suits C3 because it serves only as a bypass for the 200 kΩ resistor. C4 helps reduce output ripple in single positive power-supply systems when VOUT approaches so close to ground that the op amp's output impedance suffers. In this circuit, using a tantalum capacitor of between 0.1 µF and 2.2 µF for C4 usually helps keep the filter's output much quieter without degrading the op amp's stability.

Avoid Low-Leakage Limitations

Note that in most ordinary applications, this 2-pole filter performs as well with 0.1 µF and 0.02 µF capacitors as the passive filter in *Figure 1* does with 1 µF. Thus, if you require a 100 Hz F/V converter, the circuit in *Figure 3* furnishes good filtering with C1 = 10 µF and C2 = 2 µF, and eliminates the 100 µF low-leakage capacitor needed in a passive filter.

Note also that because C1 always has zero DC voltage across it, you can use a tantalum or aluminum electrolytic capacitor for C1 with no leakage-related problems; C2, however, must be a low-leakage type. At room temperature, typical 1 µF tantalum components allow only a few nanoamperes of leakage, but leakage this low usually cannot be guaranteed.

Compensating for Temperature Coefficients

F/V converters often encounter temperature-related problems usually resulting from the temperature coefficients of passive components. Following some simple design and manufacturing guidelines can help immunize your circuits against loss of accuracy when the temperature changes.

Capacitors fabricated from Teflon or polystyrene usually exhibit a TC of −110 ±30 ppm/°C. When you use such a component for the timing capacitor in an F/V converter (such as C_t in the *figure*) the circuit's output voltage—or the gain in terms of volts per kilohertz—also exhibits a −110 ppm/°C TC.

But the resistor-diode network (R_X, D1, D2) connected from pin 2 to ground in the *figure* can cancel the effect of the timing capacitor's large TC. When R_X = 240 kΩ, the current flowing through pin 1 will then have an overall TC of 110 ppm/°C, effectively canceling a polystyrene timing capacitor's TC to a first approximation. Thus, you needn't find a zero-TC capacitor for C_t, so long as its temperature coefficient is stable and well established. As an additional advantage, the resistor-diode network nearly compensates to zero the TC of the rest of the circuit.

Bake it for a While

After the circuit has been built and checked out at room temperature, a brief oven test will indicate the sign and the size of the TC for the complete F/V converter. Then you can add resistance in series with R_X, or add conductance in parallel with it, to greatly diminish the TC previously observed and yield a complete circuit with a lower TC than you could obtain simply by buying low TC parts.

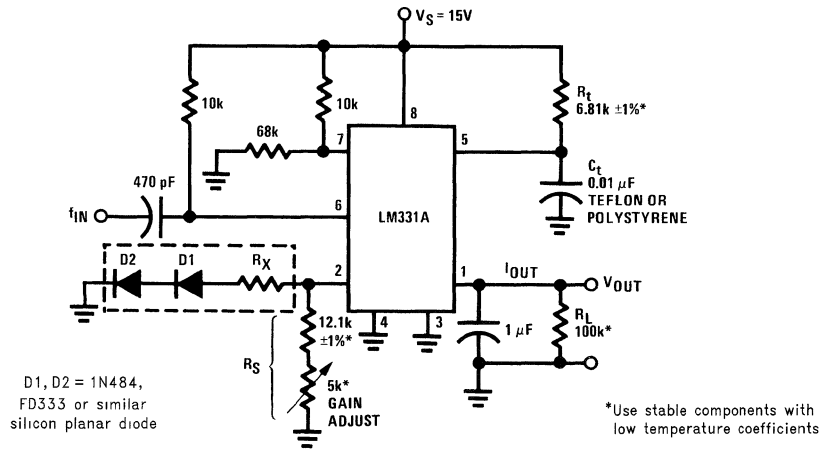
For example, if the circuit increases its full-scale output by 0.1% per 30°C (33 ppm/°C) during the oven test, adding 120 kΩ in series with R_X = 240 kΩ cancels the temperature-caused deviation. Or, if the full-scale output decreases by −0.04% per 20°C (−20 ppm/°C), just add 1.2 MΩ in parallel with R_X.

Note that to allow trimming in both directions, you must start with a finite *fixed* TC (such as the −110 ppm/°C of C_t), which then nominally cancels out by the addition of a finite *adjustable* TC. Only by using this procedure can you compensate for whatever polarity of TC is found by the oven test.

You can utilize this technique to obtain TCs as low as 20 ppm/°C, or perhaps even 10 ppm/°C, if you take a few passes to zero-in on the best value for R_X. For optimum results, consider the following guidelines:

- Use a good capacitor for C_t; the cheapest polystyrene capacitors can shift value by 0.05% or more per temperature cycle. In that case, you would not be able to distinguish the actual temperature sensitivity from the hysteresis, and you would also never achieve a stable circuit.
- After soldering, bake or temperature-cycle the circuit (at a temperature not exceeding 75°C in the case of polystyrene) for a few hours to stabilize all components and to relieve the strains of soldering.
- Do not rush the trimming. Recheck the room temperature value before *and* after you take the high temperature data to ensure a reasonably low hysteresis per cycle.
- Do not expect a perfect TC at −25°C if you trim for ±5 ppm/°C at temperatures from +25°C to 60°C. None of the components in the *figure's* circuit offer linearity much better than 5 ppm/°C or 10 ppm/°C cold, if trimmed for a zero TC at warm temperatures. Even so, using these techniques you can obtain a data converter with better than 0.02% accuracy and 0.003% linearity, for a ±20°C range around room temperature.
- Start out the trimming with R_X installed and its value near the design-center value (e.g., 240 kΩ or 270 kΩ), so you will be reasonably close to zero TC; you will usually find the process slower if you start without any resistor, because the trimming converges more slowly.
- If you change R_X from 240 kΩ to 220 kΩ, do not pull out the 240 kΩ part and put in a new 220 kΩ resistor—you will get much more consistent results by adding a 2.4 MΩ resistor in parallel. The same admonition holds true for adding resistance in series with R_X.
- Use reasonably stable components. If you use an LM331A (±50 ppm/°C maximum) and RN55D film resistors (each ±100 ppm/°C) for R_L, R_t and R_S, you probably won't be able to trim out the resulting ±350 ppm/°C worst-case TC. Resistors with a TC specification of 25 ppm/°C usually work well. Finally, use the same resistor value (e.g., 12.1 kΩ ±1%) for both R_S and R_t; when these resistors come from the same manufacturer's batch, their TC tracking will usually rate at better than 20 ppm/°C.

Whenever an op amp is used as a buffer (as in *Figure 3*), its offset voltage and current (±7.5 mV maximum and ±100 nA, respectively, for most inexpensive devices) can cause a ±17.5 mV worst-case output offset. If both plus and minus supplies are available, however, you can easily provide a symmetrical offset adjustment. With only one supply, you can add a small positive current to each op amp input and also trim one of the inputs.



Two Diodes and a Resistor Help Decrease an F/V Converter's Temperature Coefficient

Need a Negative Output?

If your F/V converter application requires a negative output voltage, the circuit shown in *Figure 7* provides a solution with excellent linearity (±0.003% typical, ±0.01% maximum). And because pin 1 of the LM331 always remains at 0 V_{DC}, this

Need a Negative Output? (Continued)

circuit needs no cascade transistor. (Note, however, that while the circuit's nonlinearity error is negligible, its ripple is not.)

The circuit in *Figure 7* offers a significant advantage over some other designs because the offset adjust voltage derives from the stable 1.9 V_{DC} reference voltage at pin 2 of the LM331; thus any supply voltage shifts cause no output shifts. The offset pot can have any value between 200 kΩ and 2 MΩ.

An optional bypass capacitor (C2) connected from the op amp's positive input to ground prevents output noise arising from stray noise pickup at that point; the capacitance value is not critical.

A Familiar Response

The circuit in *Figure 7* exhibits the same 2-pole response—with heavy output ripple attenuation—as the noninverting filter in *Figure 3*. Specifically,

$$V_{OUT}/I_{OUT} = R_F/(1 + (R4 + R_F)C4p + R4R_FC3C4p^2).$$

Here also, R5 = R4 + R_F = 200 kΩ provides the best bias current compensation.

The LM331 can handle frequencies up to 100 kHz by utilizing smaller-value capacitors as shown in *Figure 8*. This circuit increases the current at pin 2 to facilitate high-speed switching, but, despite these speed-ups, the LM331's 500 ppm/°C TC at 100 kHz causes problems because of switching speed shifts resulting from temperature changes.

To compensate for the device's positive TC, the LM334 temperature sensor feeds pin 2 a current that decreases linearly with temperature and provides a low overall temperature coefficient. An Ry value of 30 kΩ provides first-order compensation, but you can trim it higher or lower if you need more precise TC correction.

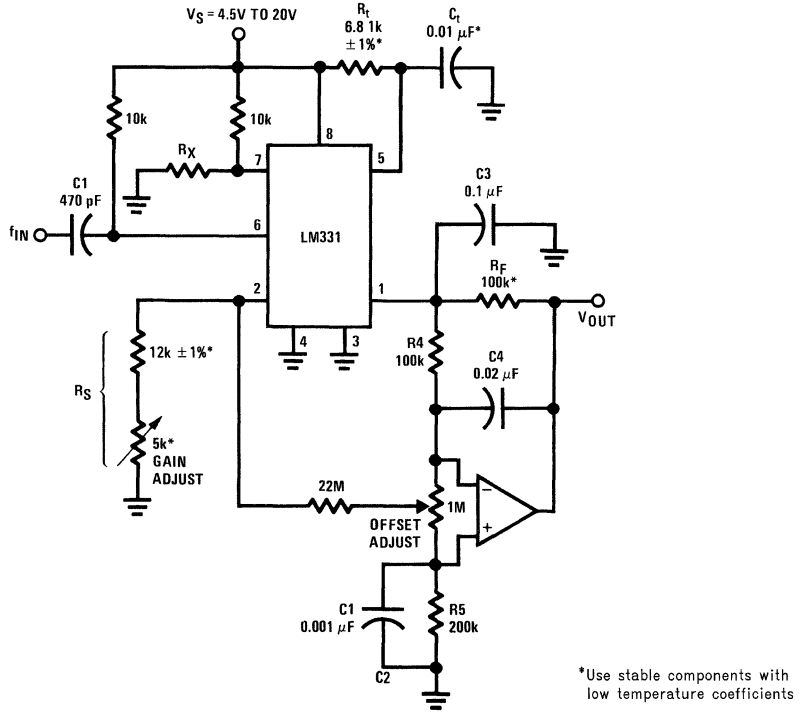


FIGURE 7. In This F/V Circuit, the Output-Buffer Op Amp Derives its Offset Voltage from the Precision Voltage Source at Pin 2 of the LM331

A Familiar Response (Continued)

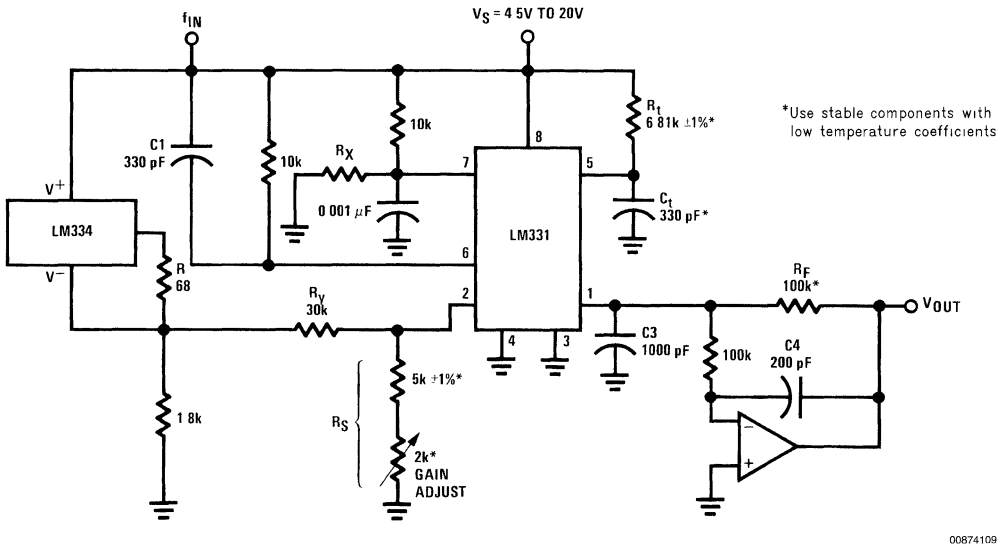


FIGURE 8. An LM334 Temperature Sensor Compensates for the F/V Circuit's Temperature Coefficient

Detect Frequencies Accurately

Using an F/V converter combined with a comparator as a frequency detector is an obvious application for these devices. But when the F/V converter is utilized in this way, its output ripple hampers accurate frequency detection, and the slow filter frequency response causes delays.

If a quick response is not important, though, you can effectively utilize an LM331-based F/V converter to feed one or more comparators, as shown in *Figure 9*. For an input frequency drop from 1.1 kHz to 0.5 kHz, the converter's output responds within about 20 ms. When the input falls from 9 kHz to 0.9 kHz, however, the output responds only after a 600 ms lag, so utilize this circuit only in applications that can tolerate F/V circuits' inherent delays and ripples.

Detect Frequencies Accurately (Continued)

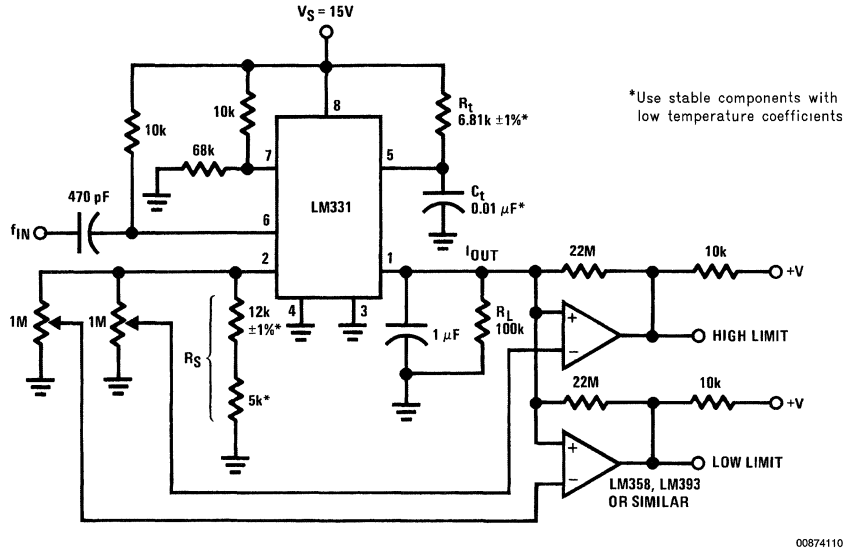


FIGURE 9. Combining a V/F IC with Two Comparators Produces a Slow-Response Frequency Detector

Author's Biography

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Versatile Monolithic V/Fs can Compute as Well as Convert with High Accuracy

National Semiconductor
Application Note D

The best of the monolithic voltage-to-frequency (V/F) converters have performance that's so good it equals or exceeds that of modular types. Some of these ICs can be designed into quite a variety of circuits because they're notably versatile. Along with versatility and high performance come the advantages that are characteristic of all V/F converters, including good linearity, excellent resolution, wide dynamic range, and an output signal that's easy to transmit as well as couple through an isolator.

One of the recently introduced monolithic types, the LM131, has both high performance and a design that's rather flexible. For instance, it can compute and convert at the same time; the computation is a part of the conversion. Among other functions, it can provide the product, ratio and square root of analog inputs.

This IC has an internal reference for its conversion circuitry that's also brought out to a pin, so it's available to external circuits associated with the converter. Not surprisingly, it turns out that any deviations of the reference, due to process variations and temperature changes have equal and opposite effects on the scale factors of the converter and the external circuitry. (This presumes, of course, that the scale factor of the external circuitry is a linear function of voltage.)

Precision Relaxation Oscillator

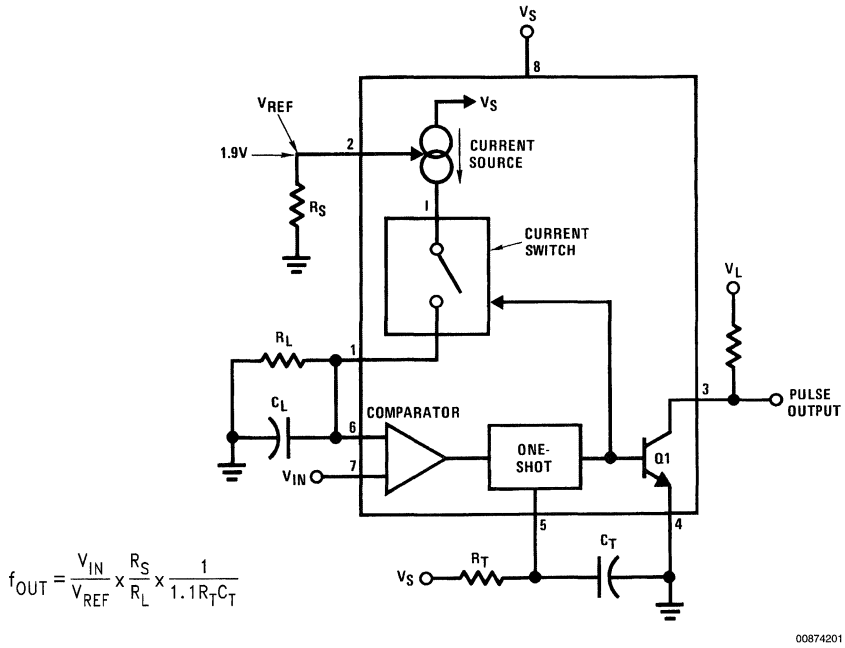
Before looking at some applications, quickly take a look at the basic circuit of an LM131 V/F converter (*Figure 1*). Basically, this IC, like any V/F converter, is a precision relaxation oscillator that generates a frequency linearly proportional to the input voltage. As might be expected, the circuit has a capacitor, C_L, with a sawtooth voltage on it. Generally speaking, the circuit is a feedback loop that keeps this capacitor charged to a voltage very slightly higher than the input voltage, V_{IN}. If V_{IN} is high, C_L discharges relatively quickly through R_L, and the circuit generates a high frequency. If V_{IN} is low, C_L discharges slowly, and the converter puts out a low frequency.

When C_L discharges to a voltage equal to the input, the comparator triggers the one-shot The one-shot closes the current switch and also turns on the output transistor. With the switch closed, current from the current source recharges C_L to a voltage somewhat higher than the input. Charging continues for a period determined by R_T and C_T. At the end of this period, the one-shot returns to its quiescent state and C_L resumes discharging.

Resistor R_S sets the amount of current put out by the current source. In fact, the current in pin 1, with the switch on, is identical to the current in pin 2. The latter pin is at a constant voltage (nominally 1.90V), so a given resistor value can set the operating currents. When connected to a high impedance buffer, this pin provides a stable reference for external circuits.

The open-collector output at pin 3 permits the output swing to be different from the converter's supply voltage, if the load circuit requires. The supplies don't have to be separate, however, and both the converter and its load can use the same voltage.

Precision Relaxation Oscillator (Continued)



$$f_{OUT} = \frac{V_{IN}}{V_{REF}} \times \frac{R_S}{R_L} \times \frac{1}{1.1 R_T C_T}$$

FIGURE 1. A voltage-to-frequency converter such as this is a relaxation oscillator with a frequency proportional to the input voltage. Current pulses keep C_L's average voltage slightly greater than the input voltage.

Steady as She Goes

By far the simplest of the circuits that make use of the reference output voltage from the LM131 is one that simply ties this output pin right back to the signal input. This connection is just a V/F converter with a constant input, which makes it a constant-frequency oscillator. Even with this simple circuit (*Figure 2*), variations in the reference voltage have two opposite effects that cancel each other out, so the circuit is particularly stable. In this type of circuit, the temperature-dependent internal delays tend to cancel as well, which isn't true of relaxation oscillators based on op amps or comparators.

Steady as She Goes (Continued)

$$f_{OUT} = \frac{1.90V}{1.90V} \times \frac{R_S}{R_L} \times \frac{1}{1.1R_TC_T}$$

$$= \frac{1}{2.2R_TC_T}$$

$$C_L \approx 10 \times C_T$$

*Stable components with low tempco

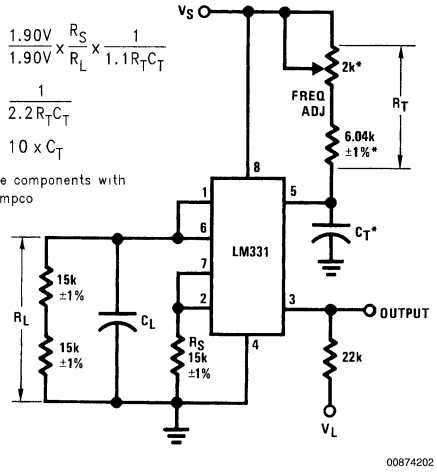


FIGURE 2. A V/F converter is a stable-frequency oscillator if its input is connected to its reference output. If the reference voltage changes, the effects of the change cancel out, so the frequency doesn't change. With low tempco components for R_T and C_T, frequency stability vs temperature can be as good as ±25 ppm/°C.

Resistors R_L and R_S are best taken from the same batch. (R_L must be larger than R_S, so it's made up of two resistors.) By doing this, the tempco tracking, which is the critical parameter, is five to ten times better than it would be if R_L were a single 30.1 kΩ resistor.

Although the reference output, pin 2, can't be loaded without affecting the converter's sensitivity, the comparator input, pin 7, has a high impedance so this connection does no harm.

Frequency stability is typically ±25 ppm/°C, even with an LM331, which as a V/F converter is specified only to 150 ppm/°C maximum. From 20 Hz to 20 kHz, stability is excellent, and the circuit can generate frequencies up to 120 kHz.

Although the simplest way of using the reference output is to tie it back to the input, the reference can also be buffered and amplified to supply such external circuitry as a resistive transducer, which might be a strain gauge or a pot (*Figure 3*). As in the stable oscillator already described, deviations of the internal reference voltage from the ideal cause the transducer's and the converter's sensitivities to change equally in opposite directions, so the effects cancel

In this circuit, op amp A2 buffers and amplifies the constant voltage at pin 2 of the converter to provide the 5V excitation for the strain gauge. Amplifier A1, connected as an instrumentation amplifier, raises the output of the strain gauge to a usable level while rejecting common-mode pickup.

A potentiometer-type transducer works just as well with this circuit. Its wiper output takes the place of A1's output as shown at the X.

The reference terminal is both a constant voltage output and a current programming input. So far, it's been shown simply with one or two resistors going to ground It is, however, a full-fledged signal input that accepts a signal from a current source quite well.

*Stable components with low tempco
A1 should have low offset; LM308A, 1/2 LM358A, LF351B, or similar
A2 General purpose, such as LF351, 1/2 LM358A or LM741

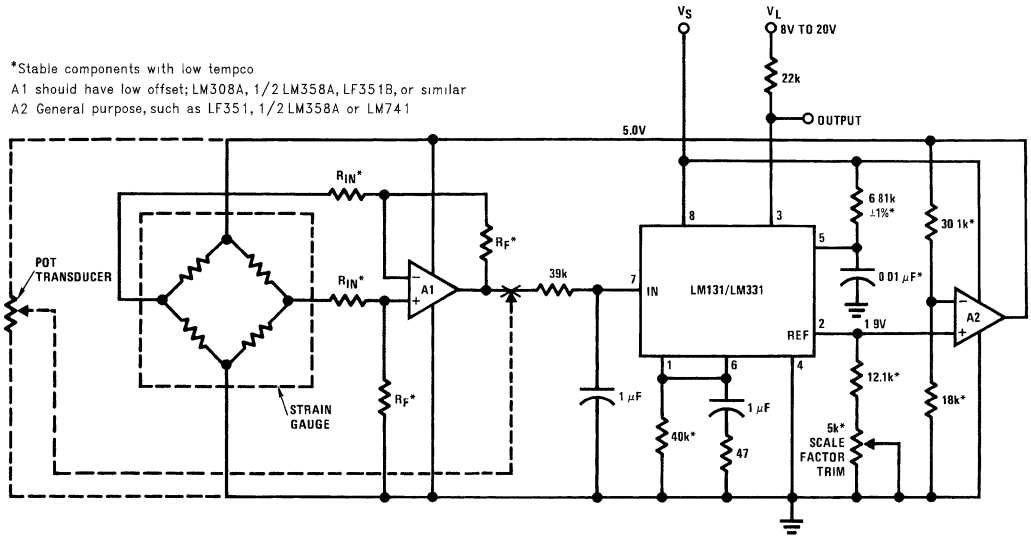
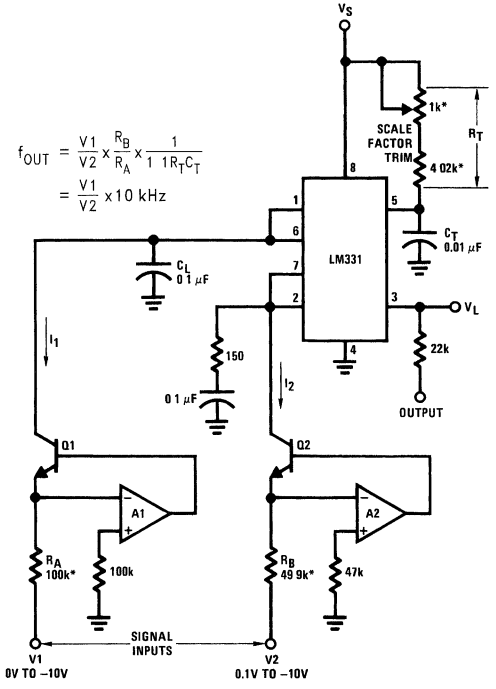


FIGURE 3. In this strain-to-frequency converter, the converter's reference excites the strain gauge (or the optional pot) through buffer amp A2. This makes the circuit insensitive to changes in the reference voltage.

Steady as She Goes (Continued)

This extra input is what enables the LM131 to compute while converting. For instance, it will convert the ratio of two voltages to a frequency proportional to the ratio (*Figure 4*). The circuit is still a V/F converter, but has two signal inputs, both of them going to rather unorthodox places at that. The inputs, shown as voltages, are converted to currents by two current pumps (voltage-to-current converters). Of course, if currents of the proper ranges are available, the current pumps aren't needed. The left current pump, which includes Q1 and A1, determines how fast capacitor C_L discharges between output pulses. The other pump sets the current in the reference circuit to control the amount of recharge current when the one-shot fires. Tying the comparator input, pin 7, to the reference pin sets the comparator's trip point at a constant voltage.



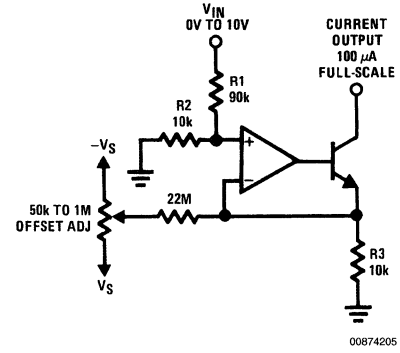
*Stable components with low tempco

A1, A2 should have low offset and low bias current LM351B, LM358A, LF353B, or similar Q1, Q2· 2N3565, 2N2484, or similar high β

FIGURE 4. This circuit converts the ratio of two voltages to an equivalent frequency without a separate analog divider. Full-scale output is 15 kHz. The two op amp circuits convert the inputs to proportional currents.

To get an idea of how the circuit works, consider first the effect of, for instance, tripling the input voltage, V1. This make C_L discharge to the comparator trip point three times as fast, so the frequency triples. Next, consider a given change, such as doubling the voltage at the other input, V2. This doubles the recharge current to C_L during the fixed-width output pulse, which means C_L's voltage increases twice as much during recharging. Since the discharge into Q1 is linear (for V1 constant), it takes twice as long for C_L to discharge—the frequency becomes half of what it was before.

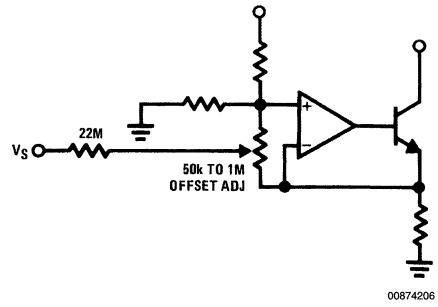
Although the current pumps in *Figure 4* must have negative inputs, rearranging the op amps according to *Figure 5* makes them accept positive inputs instead. Trimming out the offset in the op amp gives the ratio converter better linearity and accuracy. The trim circuit in *Figure 5a* needs stable positive and negative supplies for the offset trimmer, while the one in *Figure 5b* needs only a stable positive supply. Unmarked components in *Figure 5b* are the same as in *Figure 5a*.



R1, R2, R3 Stable components with low tempco

Q1 β ≥ 330

a



b

FIGURE 5. These current pumps adapt the converter circuits in *Figure 4* and *Figure 6* to positive input voltages. Optional offset trimming improves linearity and accuracy, especially with input signals that have a wide dynamic range.

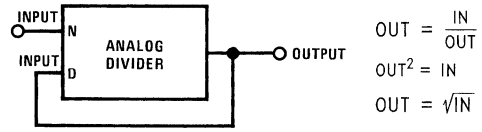
Note that the full-scale range of the current pumps can be changed by varying the value of the input resistor(s). If either of these pump circuits is used with a single positive supply,

Steady as She Goes (Continued)

the op amp should be a type such as 1/2 LM358 or 1/4 LM324, which has a common-mode range that includes the negative-supply bus.

Computing Square Roots Implicitly

An analog divider computes the square root of a signal when the signal is fed to the divider's numerator input, and the output is fed back to the divider's denominator input.



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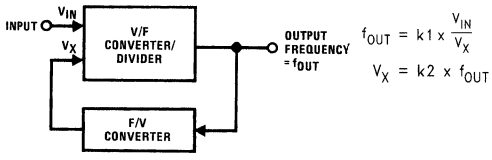
This type of computation is called implicit, because the end result of the computation is only implied, not explicitly stated by the equation that defines the computation.

In the implicit square root computing loop described in the text, a V/F converter serves as a divider. Since it's a converter, its inputs are voltages (or currents), but its output is a frequency. To connect its output back to one of its inputs so it will compute a square root means that its output frequency must be converted back to a voltage. This is taken care of by the frequency-to-voltage converter.



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Doing some algebraic substitution shows that:

$$f_{OUT} = k3 \times \sqrt{V_{IN}}$$

where

$$k3 = \sqrt{k1/k2}$$

It'll Take Reciprocals

Taking the ratio of two inputs—in other words, doing division—is only one of the mathematical operations that can be combined with converting. Another one is a special case of division, which is taking reciprocals. In this instance, the numerator (V1 in *Figure 4*) is held constant, and the denominator, V2, changes over a wide range such as one or two decades. In this case, since the frequency is the reciprocal of the input, the period of the output is proportional to the input. When operated this way, the V2 current pump should have an offset trimmer. A constant current circuit is still needed to discharge capacitor C_L.

Nonlinearity (that is, deviation from the ideal law) with an LM331 is a little better than 1% for 10 kHz full-scale. Increasing C_T to 0.1 µF reduces the nonlinearity to below 0.2% while decreasing full-scale output to 1 kHz.

Two inputs can also be multiplied while converting to a frequency. The multiplying converter circuit (*Figure 6*) that does this has a more elaborate current pump than the ratio circuit of *Figure 4*. This pump is really two cascaded circuits; it includes op amps A2 and A3 as well as transistors Q2 and Q3. Current from this pump goes to pin 5 to control the one-shot's pulse width. (This current ranges from 13.3 µA to 1.33 µA.)

As in the ratio circuit, the left current pump controls the discharge rate of C_L. The other pump, however, controls the one-shot's pulse width to vary the amount that C_L charges during the pulse. If the V2 input is close to zero, the current from the pump into pin 5 is small, and the one-shot develops a wide pulse. This allows C_L to charge quite a bit. It takes a relatively long time for C_L to discharge to the comparator threshold, so the resulting frequency is low. As V2 goes negative (a greater absolute magnitude), the output frequency rises. Op amp A3 must have a common-mode range that extends to the positive supply voltage, which the specified types do.

Multiplying, dividing and converting can all be done at the same time by combining the V2 input current pump of *Figure 4* with the circuit of *Figure 6*. If a scale-factor trimmer is needed, R4 in *Figure 6* is a good choice, better than input resistors such as R1 or R2. Using the latter as trimmers would make the input impedance of the circuit change with trim setting.

Two V/F converter ICs along with some extra circuitry will take the square root of a voltage input. Square root functions are used mostly to simulate natural laws, but also to linearize functions that have a natural square-law relationship. One of the latter is converting differential pressure to flow, where flow is proportional to the square root of differential pressure.

It'll Take Reciprocals (Continued)

*Stable components with low tempco

$$f_{OUT} = \frac{V1}{10V} \times \frac{V2}{10V} \times 10\ kHz$$

V_S = 15V, regulated and stable

$$R3 = \left(\frac{15.00V}{+V_S} \times 750\Omega \text{ with } \pm 1\% \text{ tolerance}\right.$$

A, A2: Each is 1/2 LM158/LM358A or 1/2 LF353B
A3: LM301A, LM307, or LF13741 only
Q1, Q2: High β such as 2N2484, 2N3565 or similar
Q3: High β such as 2N4250, 2N3906 or similar

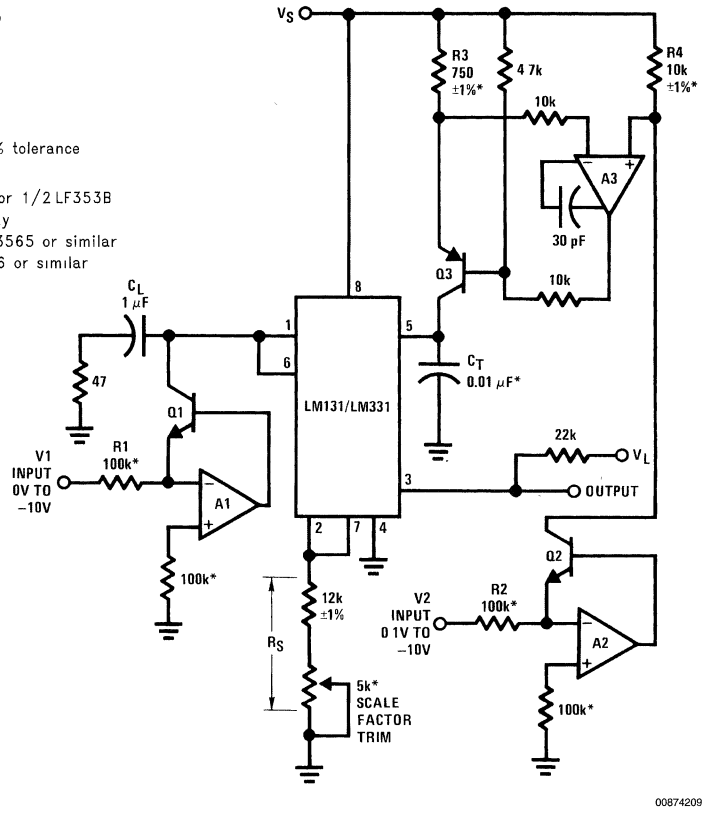


FIGURE 6. The product of two input voltages becomes an equivalent frequency in this converter. A current pump that includes op amps A2 and A3 controls the pulse duration of the converter's internal one-shot.

Versatile Pin Functions Give Design Flexibility

Two features—the reference and the one-shot—of the LM131/LM331 V/F converter deserve a closer look because they are the key to its versatility. The simplified schematic of the chip, shown here along with a transducer and the components needed for a basic V/F converter, will help to illustrate how these features work.

The reference circuit, connected to pin 2, is both a constant voltage output and a current setting, scale-factor control input. The constant voltage can supply external circuitry, such as the transducer, that feeds the converter's input.

One great advantage of using the converter's internal reference to supply the external circuitry is that any variation in the reference voltage affects the sensitivities of the converter and the external circuitry by equal and opposite amounts, so the effects of the variation cancel.

While providing a constant voltage output, pin 2 also provides scale-factor, or sensitivity control for the converter. Current supplied to an external circuit by this terminal comes from the supply (V_S) through the current mirror and the transistor. The op amp drives this transistor to hold pin 2 at a constant voltage equal to the internal reference, which is nominally 1.9V.

The current mirror provides a current to the switch that's essentially identical to that in pin 2. This means that a resistor to ground or a signal from a current source will set the current that is switched to pin 1. In most circuits, a capacitor goes from pin 1 to ground, and the switched current from this pin recharges the capacitor during the pulse from the one-shot.

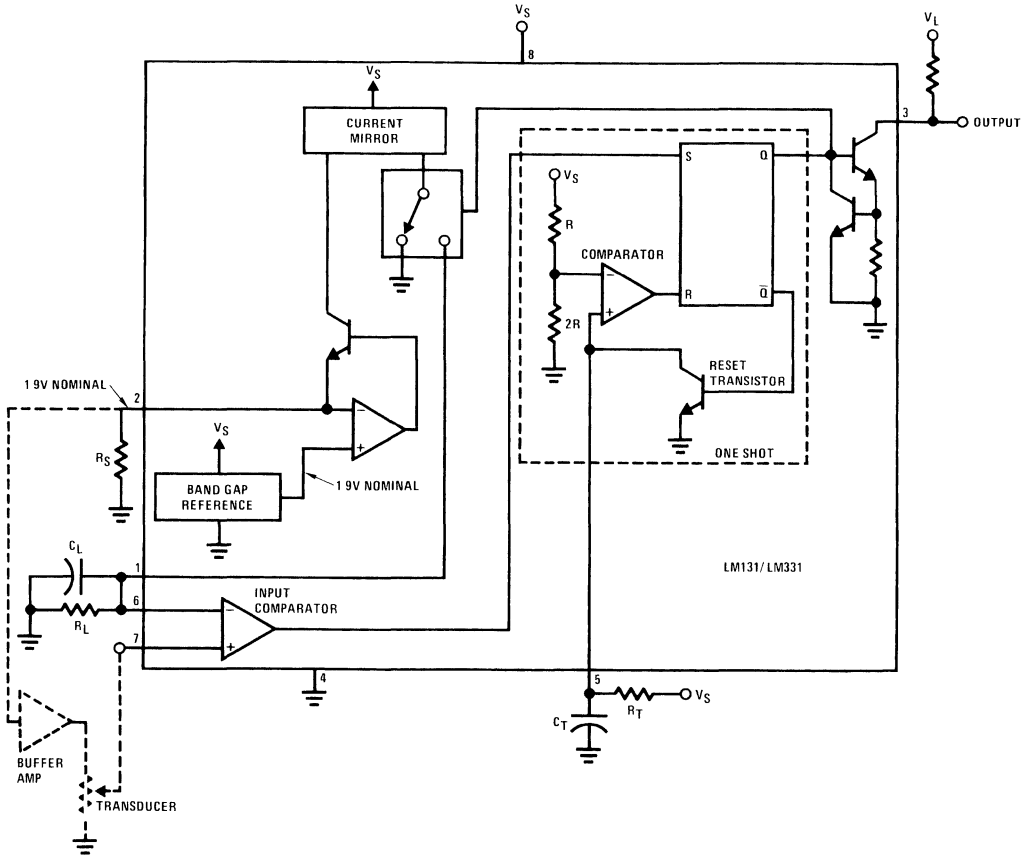
The one-shot circuit is somewhat like the well known 555 timer's circuit. In the quiescent state, the reset transistor is on and holds pin 5 near ground. When pin 7 becomes more positive than pin 6 (or pin 6 falls below pin 7), the input comparator sets the flip-flop in the one-shot.

The flip-flop turns on the current limited output transistor (pin 3) and switches the current coming from the current mirror to pin 1. The flip-flop also turns off the reset transistor, and the timing capacitor C_T starts to charge toward V_S. This charge is exponential, and C_T's voltage reaches 2/3 of V_S in about

Versatile Pin Functions Give Design Flexibility (Continued)

1.1 R_TC_T time constants. (The quantity 1.1 is –ln 0.333...) When pin 5 reaches this voltage, the one-shot's comparator resets the flip-flop which turns off the current to pin 1, discharges C_T, and turns off the output transistor.

If the voltages at pins 6 and 7 still call for setting the flip-flop after pin 5 has reached 2/3 V_S, internal logic not shown in this simplified diagram overrides the reset signal from the one-shot's own comparator, and the flip-flop stays set. In this instance, C_T continues charging past 2/3 V_S.



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Root Loop Computes

The circuit in *Figure 7* is an implicit loop (see "Computing Square Roots Implicitly") that uses IC1 as a voltage-to-frequency converter and divider, and IC2 as a frequency-to-voltage converter. The F/V converter, IC2, and the current pump that includes A1 and the transistor return the output of IC1 to its denominator input. A relatively elaborate feedback circuit like this is needed to convert IC1's frequency output back to a current for its denominator input.

Looking at the circuit in more detail, IC1 puts out a frequency proportional to V_{IN} divided by the feedback voltage, V_X. The current I_1 is generated by a current pump that has V_X as its input (*Figure 5a*). To develop the feedback IC2 converts the pulse output from IC1 into standard width precision current pulses that charge capacitor C1. This capacitor integrates them into the voltage V_X, thus closing the loop.

Op amp A2, serving as a comparator, ensures that the circuit will always start and continue running. If V_{IN} suddenly jumps to a higher voltage, one pulse from the one-shot in IC1 may not be enough to recharge C_L to a voltage higher than the input. In such a case, the IC's internal logic keeps its internal current switch turned on, and the voltage on C_L ramps up until it exceeds the input. During this time, however, IC1's output hasn't changed state. (Such a temporary hang-up isn't unique to this circuit, and equivalent things happen to other V/Fs besides the LM131/LM331.) What is worse here, though, is that the lack of pulses to IC2 means that V_X and I_1 decay. The recharging current, I_2, is the same as I_1, so it not only becomes progressively harder for the voltage on C_L to catch up with the input, it may even fail to catch up entirely if ($I_2 \times R_L$) is less than the input voltage.

Root Loop Computes (Continued)

As a sign of this condition, when the converter hangs up, the one-shot's timing node, pin 5, continues to charge well beyond its normal peak of 2/3 V_S. As soon as the comparator A2 detects this rise, it pulls up voltage V_X, current I_1 increases, and the loop catches its breath again.

After all these nonlinear computations, this last circuit is about as linear as it can be. It's a precision, ultralinear V/F converter based on an LM331A (*Figure 8*) that has several detail refinements over previous V/F converter circuits. Choosing the proper components and trimming the tempco give less than 0.02% error and 0.003% nonlinearity for a ±20°C range around room temperature.

This circuit has an active integrator, which includes the op amp and the integrating feedback capacitor, C_F. The integrator converts the input voltage, which is negative, into a positive-going ramp. When the ramp reaches the converter IC's comparator threshold, the one-shot fires and switches a pulse of current to the integrator's summing junction. This current makes the integrator's output ramp down quickly. When the one-shot times out, the cycle repeats.

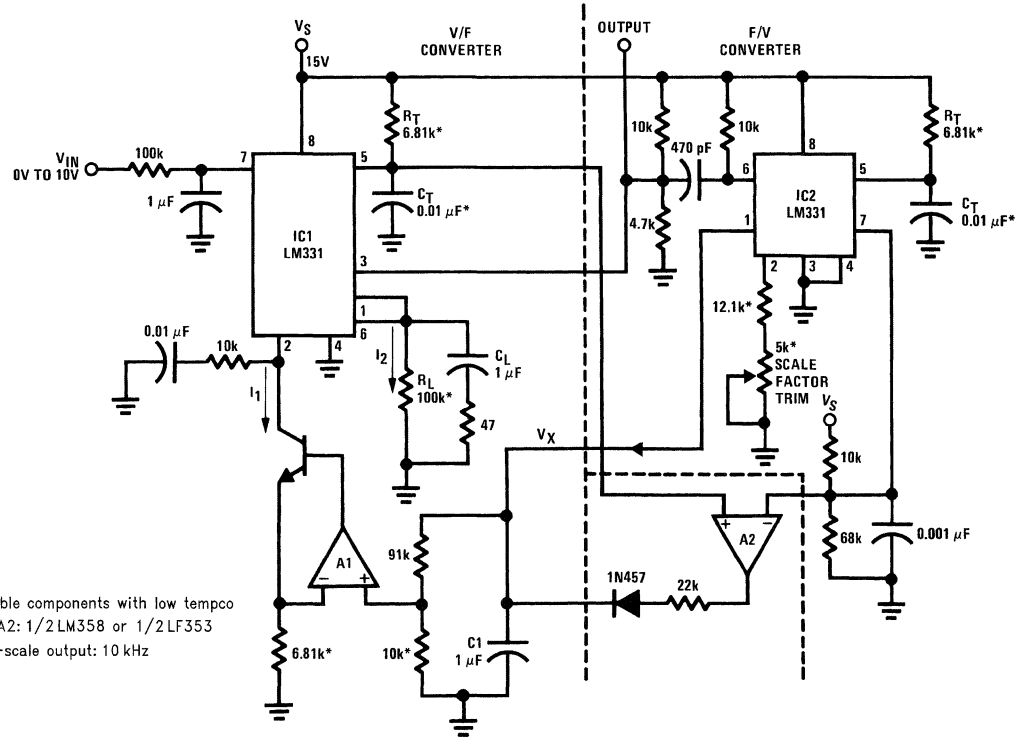


FIGURE 7. Two converter ICs generate an output frequency proportional to the square root of the input voltage. The circuit is an implicit loop in which IC1 serves as a divider and V/F converter. This IC's output goes back to its denominator input through F/V converter IC2 to make the circuit output equal the input's square root.

Root Loop Computes (Continued)

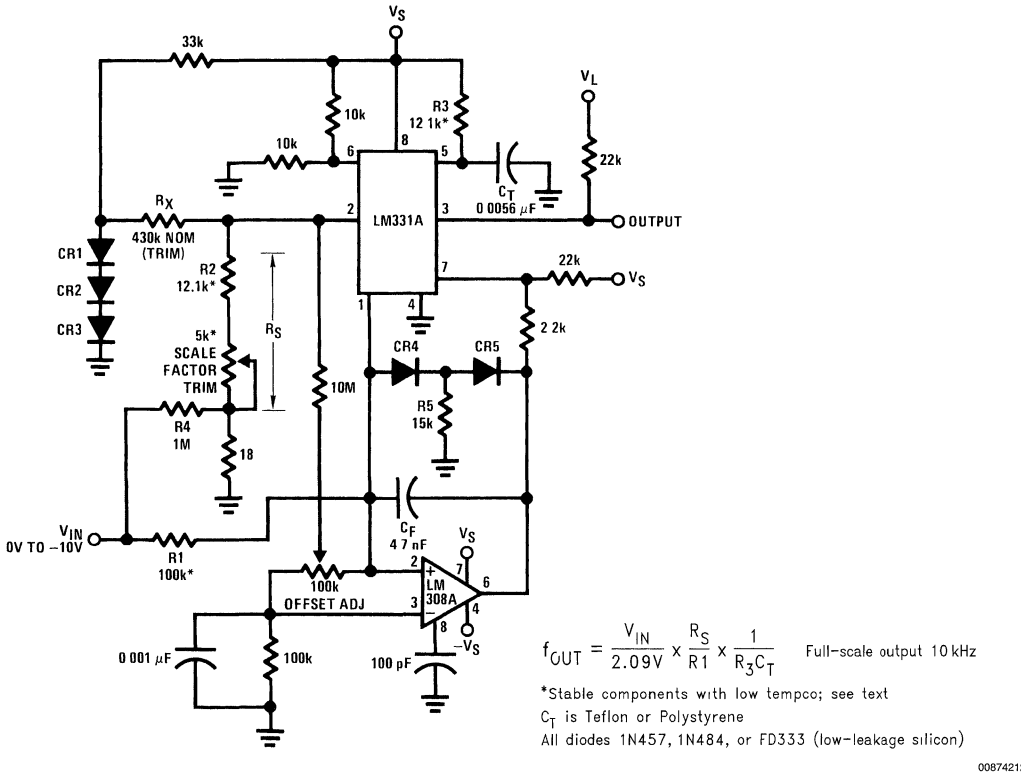


FIGURE 8. An ultraprecision V/F converter, capable of better than 0.02% error and 0.003% nonlinearity for a ±20°C range about room temperature, augments the basic converter with an external integrator.

There are several reasons this converter circuit gives high performance:

- A feedback limiter prevents the op amp from driving pin 7 of the LM331A negative. The limiter circuit arrangement bypasses the leakage through CR5 to ground via R5, so it won't reach the summing junction. Bypassing leakage this way is especially important at high temperatures.
- The offset trimming pot is connected to the stable 1.9V reference at pin 2 instead of to a power supply bus that might be unstable and noisy.
- A small fraction (180 μV, full-scale) of the input voltage goes via R4 to the R_S network, which improves the non-linearity from 0.004% to 0.002%
- Resistors R2 and R3 are the same value, so that resistors such as Allen-Bradley type CC metal-film types can provide excellent tempco tracking at low cost. (This tracking is very good when equal values come from the same batch.) Resistor R1 should be a low tempco metal-film or wirewound type, with a maximum tempco of ±10 ppm/°C or ±25 ppm/°C.

In addition, C_T should be a polystyrene or Teflon type. Polystyrene is rated to 80°C, while Teflon goes to 150°C. Both types can be obtained with a tempco of −110 ±30 ppm/°C. Choosing this tempco for C_T makes the tempco, due to C_T, of the full-scale output frequency 110 ppm/°C.

Using tight tolerance components results in a total tempco between 0 ppm/°C and 220 ppm/°C, so the tempco will never be negative. The voltage at CR1 and R_X has a tempco of −6 mV/°C, which can be used to compensate the tempco of the rest of the circuit. Trimming R_X compensates for the tempco of the V/F IC, the capacitor, and all the resistors.

A good starting value for selecting R_X is 430 kΩ, which will give the 135 μA flowing out of pin 2 a slope of 110 ppm/°C. If the output frequency increases with temperature, a little more conductance should be added in parallel with R_X.

When doing a second round of trimming, though, note that a resistor of, say, 4.3 MΩ, has about the same effect on tempco when shunted across a 220 kΩ resistor that it does when shunted across one of 430 kΩ, namely, −11 ppm/°C. This technique can give tempcos below ±20 ppm/°C or even ±10 ppm/°C.

Root Loop Computes (Continued)

Some precautions help this procedure converge:

1. Use a good capacitor for C_T. The cheapest polystyrene capacitors will shift in value by 0.05% or more per temperature cycle. The actual temperature sensitivity would be indistinguishable from the hysteresis, and the circuit would never be stable.
2. After soldering, bake and/or temperature-cycle the circuit (at a temperature not exceeding 75˚C if C_T is polystyrene) for a few hours, to stabilize all components and to relieve the strains from soldering.
3. Don't rush the trimming. Recheck the room temperature value, before and after the high temperature data are taken, to ensure that hysteresis per cycle is reasonably low.
4. Don't expect a perfect tempco at −25˚C if the circuit is trimmed for ±5 ppm/˚C between 25˚C and 60˚C. If it's been trimmed for zero tempco while warm, none of its components will be linear to much better than 5 ppm/˚C or 10 ppm/˚C when it's cold.

The values shown in this circuit are generally optimum for ±12V to ±16V regulated supplies but any stable supplies between ±4V and ±22V would be usable, after changing a few component values.

Section 7
Interface

Section 7 Contents

Integrated Circuits for Digital Data Transmission

National Semiconductor
Application Note 22

Introduction

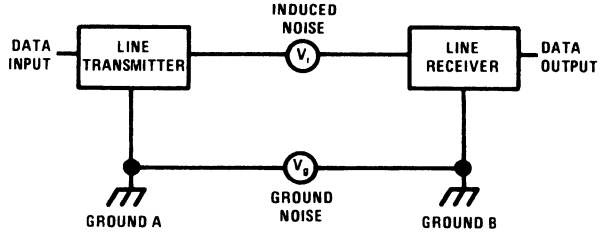
It is frequently necessary to transmit digital data in a high-noise environment where ordinary integrated logic circuits cannot be used because they do not have sufficient noise immunity. One solution to this problem, of course, is to use high-noise-immunity logic. In many cases, this approach would require worst case logic swings of 30V, requiring high power-supply voltages. Further, considerable power would be needed to transmit these voltage levels at high speed. This is especially true if the lines must be terminated to eliminate reflections, since practical transmission lines have a low characteristic impedance.

A much better solution is to convert the ground referred digital data at the transmission end into a differential signal and transmit this down a balanced, twisted-pair line. At the receiving end, any induced noise, or voltage due to ground-loop currents, appears equally on both ends of the twisted-pair line. Hence, a receiver which responds only to the differential signal from the line will reject the undesired signals even with moderate voltage swings from the transmitter.

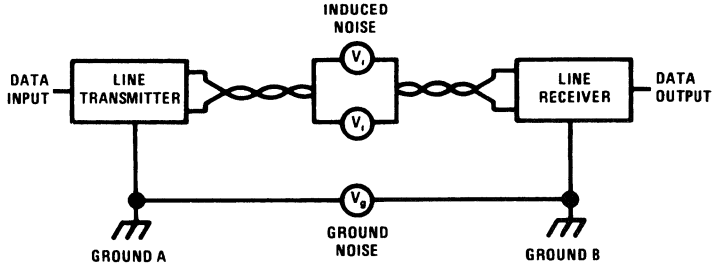
Figure 1 illustrates this situation more clearly. When ground is used as a signal return as in *Figure 1*, the voltage seen at the receiving end will be the output voltage of the transmitter plus any noise voltage induced in the signal line. Hence, the noise immunity of the transmitter-receiver combination must be equal to the maximum expected noise from both sources.

The differential transmission scheme diagrammed in *Figure 1* solves this problem. Any ground noise or voltage induced on the transmission lines will appear equally on both inputs of the receiver. The receiver responds only to the differential signal coming out of the twisted-pair line and delivers a single-ended output signal referred to the ground at the receiving end. Therefore, extremely high noise immunities are not needed; and the transmitter and receiver can be operated from the same supplies as standard integrated logic circuits.

This article describes the operation and use of a line driver and line receiver for transmission systems using twisted-pair lines. The transmitter provides a buffered differential output from a DTL or TTL input signal. A four-input gate is included on the input so that the circuit can also perform logic. The receiver detects a zero crossing in the differential input voltage and can directly drive DTL or TTL integrated circuits at the receiving end. It also has strobe capability to blank out unwanted input signals. Both the transmitter and the receiver incorporate two independent units on a single silicon chip.



a Single-Ended System



b Difference System

FIGURE 1. Comparing Differential and Single-Ended Data Transmission

Line Driver

Figure 2 shows a schematic diagram of the line transmitter. The circuit has a marked resemblance to a standard TTL buffer. In fact, it is possible to use a standard dual buffer as a transmitter. However, the DS7830 incorporates additional features. For one, the output is current limited to protect the driver from accidental shorts in the transmission lines. Secondly, diodes on the output clamp sever voltage transients that may be induced into the transmission lines. Finally, the circuit has internal inversion to produce a differential output signal, reducing the skew between the outputs and making the output state independent of loading.

As can be seen from the upper half of *Figure 2*, a quadruple-emitter input transistor, Q9, provides four logic inputs to the transmitter. This transistor drives the inverter stage formed by Q10 and Q11 to give a NAND output. A low state logic input on any of the emitters of Q9 will cause the base drive to be removed from Q10, since Q9 will be saturated by current from R8, holding the base of Q10 near ground. Hence, Q10 and Q11 will be turned off; and the output will be in a high state. When all the emitters of Q9 are at a one logic level, Q10 receives base drive from R8 through the forward biased collector-base junction of Q9. This saturates Q10 and also Q11, giving a low output state. The input voltage at which the transition occurs is equal to the sum of the emitter-base turn on voltages of Q10 and Q11 minus the saturation voltage of Q9. This is about 1.4V at 25°C.

A standard "totem-pole" arrangement is used on the output stage. When the output is switched to the high state, with Q10 and Q11 cut off, current is supplied to the load by Q13 and Q14 which are connected in a modified Darlington configuration. Because of the high compound current gain of these transistors, the output resistance is quite low and a large load current can be supplied. R10 is included across the emitter-base junction of Q13 both to drain off any collector-base leakage current in Q13 and to discharge the collector-base capacitance of Q13 when the output is switched to the low state. In the high state, the output level is approximately two diode drops below the positive supply, or roughly 3.6V at 25°C with a 5.0V supply.

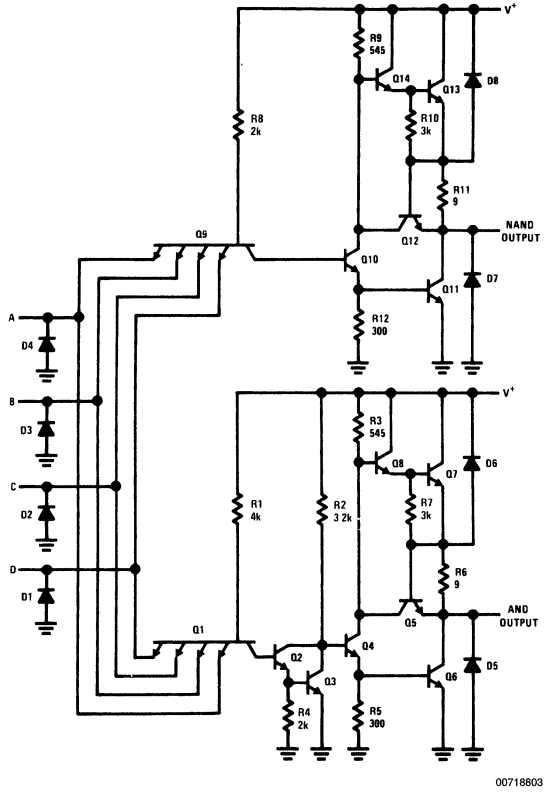


FIGURE 2. Schematic Diagram of the DS7830 Line Driver

With the output switched into the low state, Q10 saturates, holding the base of Q14 about one diode drop above ground. This cuts off Q13. Further, both the base current and the collector current of Q10 are driven into the base of Q11 saturating it and giving a low-state output of about 0.1V. The circuit is designed so that the base of Q11 is supplied 6 mA, so the collector can drive considerable load current before it is pulled out of saturation.

Line Driver (Continued)

The primary purpose of R12 is to provide current to remove the stored charge in Q11 and charge its collector-base capacitance when the circuit is switched to the high state. Its value is also made less than R9 to prevent supply current transients which might otherwise occur (Note 1) when the power supply is coming up to voltage.

The lower half of the transmitter in *Figure 2* is identical to the upper, except that an inverter stage has been added This is needed so that an input signal which drives the output of the upper half positive will drive the lower half negative, and vice versa, producing a differential output signal. Transistors Q2 and Q3 produce the inversion. Even though the current gain is not necessarily needed, the modified Darlington connection is used to produce the proper logic transition voltage on the input of the transmitter. Because of the low load capacitance that the inverter sees when it is completely within the integrated circuit, it is extremely fast, with a typical delay of 3 ns This minimizes the skew between the outputs.

One of the schemes used when dual buffers are employed as a differential line driver is to obtain the NAND output in the normal fashion and provide the AND output by connecting the input of the second buffer to the NAND output Using an internal inverter has some distinct advantages over this: for one, capacitive loads which slow down the response of the NAND output will not introduce a time skew between the two outputs; secondly, line transients on the NAND output will not cause an unwanted change of state on the AND output.

Clamp diodes, D1 through D4, are added on all inputs to clamp undershoot. This undershoot and ringing can occur in TTL systems because the rise and fall times are extremely short.

Output-current limiting is provided by adding a resistor and transistor to each of the complementary outputs. Referring again to *Figure 2*, when the current on the NAND output increases to a value where the voltage drop across R11 is sufficient to turn on Q12, the short circuit protection comes into effect This happens because further increases in output current flow into the base of Q12 causing it to remove base drive from Q14 and, therefore, Q13. Any substantial increase in output current will then cause the output voltage to collapse to zero. Since the magnitude of the short circuit depends on the emitter base turn-on voltage of Q12, this current has a negative temperature coefficient. As the chip temperature increases from power dissipation, the available short circuit current is reduced. The current limiting also serves to control the current transient that occurs when the output is going through a transition with both Q11 and Q13 turned on.

Note 1: Kalb, "Design Considerations for a TTL Gate", National Semiconductor TP-6, May, 1968

The AND output is similarly protected by R6 and Q5, which limits the maximum output current to about 100 mA, preventing damage to the circuit from shorts between the outputs and ground.

The current limiting transistors also serve to increase the low state output current capability under severe transient conditions. For example, when the current into the NAND output becomes so high as to pull Q11 out of saturation, the output voltage will rise to two diode drops above ground. At this voltage, the collector-base junction of Q12 becomes forward biased and supplies additional base drive to Q11 through Q10 which is saturated. This minimizes any further increase in output voltage.

When either of the outputs are in the high state, they can drive a large current towards ground without a significant change in output voltage. However, noise induced on the transmission line which tries to drive the output positive will cut it off since it cannot sink current in this state. For this reason, D6 and D8 are included to clamp the output and keep it from being driven much above the supply voltage, as this could damage the circuit.

When the output is in a low state, it can sink a lot of current to clamp positive-going induced voltages on the transmission line However, it cannot source enough current to eliminate negative-going transients so D5 and D7 are included to clamp those voltages to ground.

It is interesting to note that the voltage swing produced on one of the outputs when the clamp diodes go into conduction actually increases the differential noise immunity For example with no induced common mode current, the low-state output will be a saturation voltage above ground while the high output will be two diode drops below the positive supply voltage. With positive-going common mode noise on the line, the low output remains in saturation; and the high output is clamped at a diode drop above the positive supply. Hence, in this case, the common mode noise increases the differential swing by three diode drops.

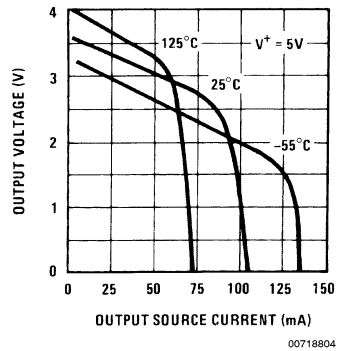


FIGURE 3. High State Output Voltage as a Function of Output Current

Having explained the operation of the line driver, it is appropriate to look at the performance in more detail. *Figure 3* shows the high-state output characteristics under load. Over the normal range of output currents, the output resistance is about 10Ω. With higher output currents, the short circuit protection is activated, causing the output voltage to drop to

Line Driver (Continued)

zero. As can be seen from the figure, the short-circuit current decreases at higher temperatures to minimize the possibility of over-heating the integrated circuit.

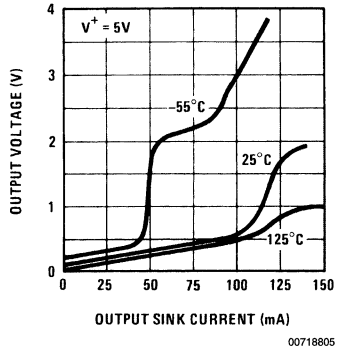


FIGURE 4. Low-State Output Current as a Function of Output Current

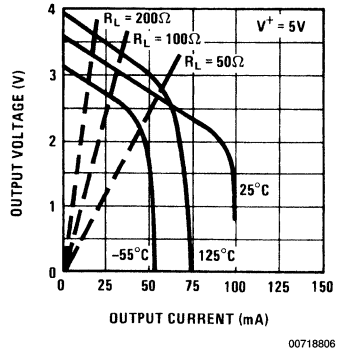


FIGURE 5. Differential Output Voltage as a Function of Differential Output Current

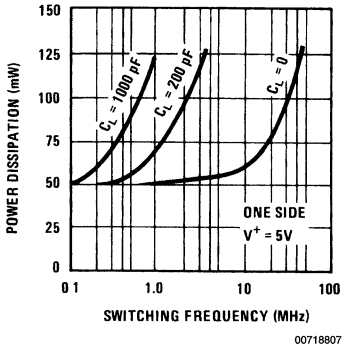


FIGURE 6. Power Dissipation as a Function of Switching Frequency

Figure 4 is a similar graph of the low-state output characteristics. Here, the output resistance is about 5Ω with normal values of output current. With larger currents, the output transistor is pulled out of saturation; and the output voltage increases. This is more pronounced at −55°C where the transistor current gain is the lowest. However, when the output voltage rises about two diode drops above ground, the collector-base junction of the current-limit transistor becomes forward biased, providing additional base drive for the output transistor. This roughly doubles the current available for clamping positive common-mode transients on the twisted-pair line. It is interesting to note that even though the output level increases to about 2V under this condition, the differential noise immunity does not suffer because the high-state output also increases by about 3V with positive going common-mode transients.

It is clear from the figure that the low state output current is not effectively limited. Therefore, the device can be damaged by shorts between the output and the 5V supply. However, protection against shorts between outputs or from the outputs to ground is provided by limiting the high-state current.

The curves in *Figure 3* and *Figure 4* demonstrate the performance of the line driver with large, capacitively-coupled common-mode transients, or under gross overload conditions. *Figure 5* shows the ability of the circuit to drive a differential load: that is, the transmission line. It can be seen that for output currents less than 35 mA, the output resistance is approximately 15Ω. At both temperature extremes, the output falls off at high currents. At high temperatures, this is caused by current limiting of the high output state. At low temperatures, the fall off of current gain in the low-state output transistor produces this result.

Load lines have been included on the figure to show the differential output with various load resistances. The output swing can be read off from the intersection of the output characteristic with the load line. The figure shows that the driver can easily handle load resistances greater than 100Ω.

This is more than adequate for practical, twisted-pair lines.

Figure 6 shows the no load power dissipation, for one-half of the dual line driver, as a function of frequency. This information is important for two reasons. First, the increase in power dissipation at high frequencies must be added to the excess power dissipation caused by the load to determine the total package dissipation. Second, and more important, it is a measure of the "glitch" current which flows from the positive supply to ground through the output transistors when the circuit is going through a transition. If the output stage is not properly designed, the current spikes in the power supplies can become quite large; and the power dissipation can increase by as much as a factor of five between 100 kHz and 10 MHz. The figure shows that, with no capacitive loading, the power increases with frequencies as high as 10 MHz is almost negligible. However, with large capacitive loads, more power is required.

The line receiver is designed to detect a zero crossing in the differential output of the line driver. Therefore, the propagation time of the driver is measured as the time difference between the application of a step input and the point where the differential output voltage crosses zero. A plot of the propagation time over temperature is shown in *Figure 7* . This delay is added directly to the propagation time of the transmission line and the delay of the line receiver to determine the total data-propagation time. However, in most cases, the delay of the driver is small, even by comparison to the uncertainties in the other delays.

Line Driver (Continued)

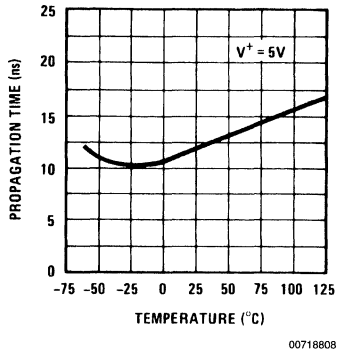


FIGURE 7. Propagation Time as a Function of Temperature

To summarize the characteristics of the DS7830 line driver, the input interfaces directly with standard TTL circuits. It presents a load which is equivalent to a fan out of 3 to the circuit driving it, and it operates from the 5.0V, ±10% logic supplies. The output can drive low impedance lines down to 50Ω and capacitive loads up to 5000 pF. The time skew between the outputs is minimized to reduce radiation from the twisted-pair lines, and the circuit is designed to clamp common mode transients coupled into the line. Short circuit protection is also provided. The integrated circuit consists of two independent drivers fabricated on a 41 x 53 mil-square die using the standard TTL process. A photomicrograph of the chip is shown in *Figure 8* .

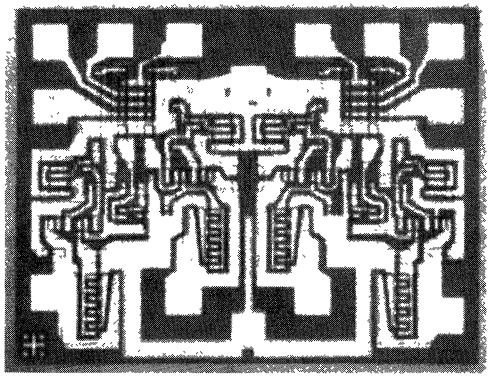


FIGURE 8. Photomicrograph of the DS7830 Dual Line Driver

Line Receiver

As mentioned previously, the function of the line receiver is to convert the differential output signal of the line driver into a single ended, ground-referred signal to drive standard digital circuits on the receiving end. At the same time it must reject the common mode and induced noise on the transmission line.

Normally this would not be too difficult a task because of the large signal swings involved. However, it was considered important that the receiver operate from the +5V logic supply without requiring additional supply voltages, as do most other line receiver designs. This complicates the situation because the receiver must operate with ±15V input signals which are considerably greater than the operating supply voltage.

The large common mode range over which the circuit must work can be reduced with an attenuator on the input of the receiver. In this design, the input signal is attenuated by a factor of 30. Hence, the ±15V common mode voltage is reduced to ±0.5V, which can be handed easily by circuitry operating from a 5V supply. However, the differential input signal, which can go down as low as ±2.4V in the worst case, is also reduced to ±80 mV. Hence, it is necessary to employ a fairly accurate zero crossing detector in the receiver.

System requirements dictated that the threshold inaccuracy introduced by the zero crossing detector be less than 17 mV. In principle, this accuracy requirement should not pose insurmountable problems because it is a simple matter to make well matched parts in an integrated circuit.

Figure 9 shows a simplified schematic diagram of the circuit configuration used for the line receiver The input signal is attenuated by the resistive dividers R1-R2 and R8-R3. This attenuated signal is fed into a balanced DC amplifier, operating in the common base configuration. This input amplifier, consisting of Q1 and Q2, removes the common mode component of the input signal. Further, it delivers an output signal at the collector of Q2, which is nearly equal in amplitude to the original differential input signal. this output signal is buffered by Q6 and drives an output amplifier, Q8. The output stage drives the logic load directly.

An understanding of the circuit can be obtained by first considering the input stage. Assuming high current gains and neglecting the voltage drop across R3, the collector current of Q1 will be:

$$I_{C1} = \frac{V^+ - V_{BE1} - V_{BE3} - V_{BE4}}{R11} \quad (1)$$

With equal emitter-base voltages for all transistors, this becomes:

$$I_{C1} = \frac{V^+ - 3V_{BE}}{R11} \quad (2)$$

The output voltage at the collector of Q2 will be:

$$V_{C2} = V+ - I_{C2}R12 \quad (3)$$

Line Receiver (Continued)

When the differential input voltage to the receiver is zero, the voltages presented to the emitters of Q1 and Q2 will be equal. If Q1 and Q2 are matched devices, which is easy to arrange when they are fabricated close together on a single silicon chip, their collector currents will be equal with zero input voltage. Hence, the output voltage from Q2 can be determined by substituting (2) into (3):

$$V_{C2} = V^+ - \frac{R12}{R11}(V^+ - 3V_{BE}) \quad (4)$$

For R11 = R12, this becomes:

$$V_{C2} = 3V_{BE}$$

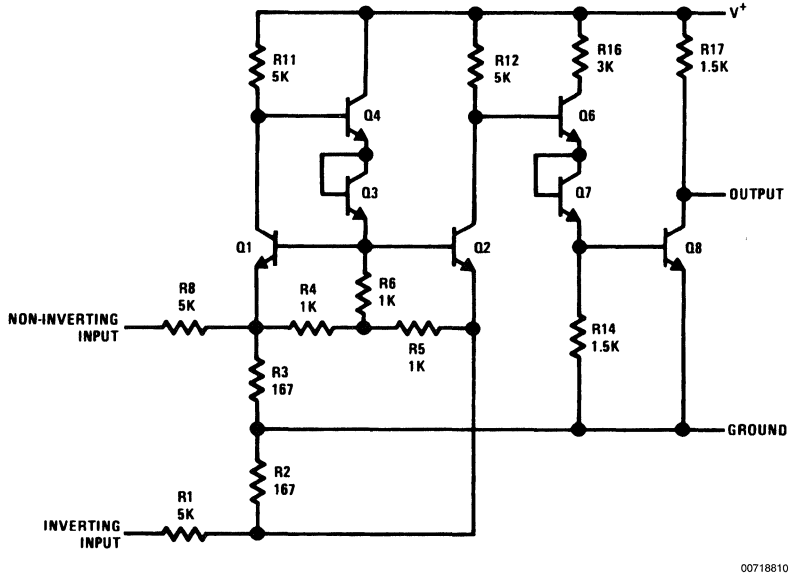


FIGURE 9. Simplified Schematic of the Line Receiver

The voltage on the base of Q6 will likewise be $3V_{BE}$ when the output is on the verge of switching from a zero to a one state. A differential input signal which causes Q2 to conduct more heavily will then make the output go high, while an input signal in the opposite direction will cause the output to saturate.

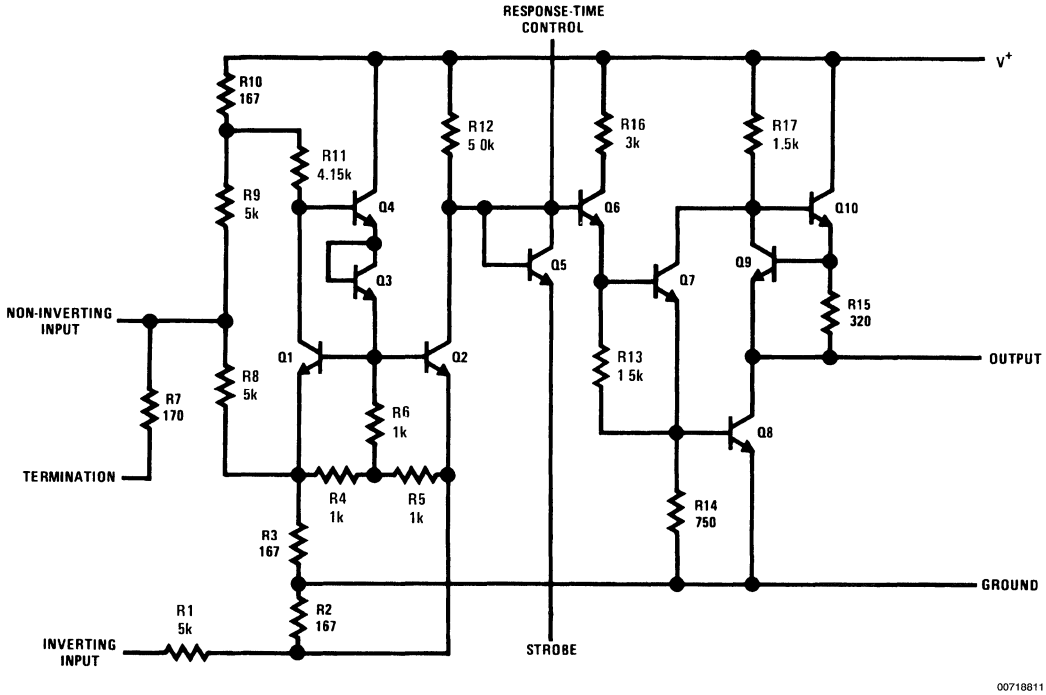
It should be noted that the balance of this circuit is not affected by absolute values of components—only by how well they match. Nor is it affected by variations in the positive supply voltage, so it will perform well with standard logic supply voltages between 4.5V and 5.5V. In addition, component values are chosen so that the collector currents of Q4 and Q6 are equal. As a result, the base currents of Q4 and Q6 do not upset the balance of the input stage. This means that circuit performance is not greatly affected by production or temperature variations in transistor current gain.

A complete schematic of the line receiver, shown in *Figure 10*, shows several refinements of the basic circuit which are needed to secure proper operation under all conditions. For one, the explanation of the simplified circuit ignores the fact that the collector current of Q1 will be affected by common mode voltage developed across R3. This can give a 0.5V threshold error at the extremes of the ±15V common mode range. To compensate for this, a separate divider, R9 and R10, is used to maintain a constant collector current in Q1 with varying common mode signals. With an increasing common mode voltage on the non-inverting input, the voltage on the emitter of Q1 will increase. Normally, this would cause the voltage across R11 to decrease, reducing the collector current of Q1. However, the increasing common mode signal also drives the top end of R11 through R9 and R10 so as to hold the voltage drop across R11 constant.

In addition to improving the common mode rejection, R9 also forces the output of the receiver into the high state when nothing is connected to the input lines. This means that the output will be in a pre-determined state when the transmission cables are disconnected.

A diode connected transistor, Q5, is also added in the complete circuit to provide strobe capability. With a logic zero on the strobe terminal, the output will be high no matter what the input signal is. With the strobe, the receiver can be made immune to any noise signals during intervals where no digital information is expected. The output state with the strobe on is also the same as the output state with the input terminals open.

Line Receiver (Continued)



DM7820 dual line receiver (one side)

FIGURE 10. Complete Schematic of One Half of the DS7820 Line Receiver

The collector of Q2 is brought out so that an external capacitor can be used to slow down the receiver to where it will not respond to fast noise spikes. This capacitor, which is connected between the response-time-control terminal and ground, does not give exactly-symmetrical delays. The delay for input signals which produce a positive-going output will be less than for input signals of opposite polarity. This happens because the impedance on the collector of Q2 drops as Q6 goes into saturation, reducing the effectiveness of the capacitor.

Another difference in the complete circuit is that the output stage is improved both to provide more gain and to reduce the output resistance in the high output state. This was accomplished by adding Q9 and Q10. When the output stage is operating in the linear region, that is, on the verge of switching to either the high or the low state, Q9 and Q10 form sort of an active collector load for Q8. The current through R15 is constant at approximately 2 mA as the output voltage changes through the active region. Hence, the percentage change in the collector current of Q8 due to the voltage change across R17 is made smaller by this pre-bias current; and the effective stage gain is increased.

With the output in the high state (Q8 cut off), the output resistance is equal to R15, as long as the load current is less than 2 mA. When the load current goes above this value, Q9 turns on; and the output resistance increases to 1.5k, the value of R17.

This particular output configuration gives a higher gain than either a standard DTL or TTL output stage. It can also drive enough current in the high state to make it compatible with TTL, yet outputs can be wire OR'ed as with DTL.

Remaining details of the circuit are that Q7 is connected as an emitter follower to make the circuit even less sensitive to transistor current gains. R16 limits the base drive to Q7 with the output saturated, while R17 limits the base drive to the output transistor, Q8. A resistor, R7, which can be used to terminate the twisted-pair line is also included on the chip. It is not connected directly across the inputs. Instead, one end is left open so that a capacitor can be inserted in series with the resistor. The capacitor significantly reduces the power dissipation in both the line transmitter and receiver, especially in low-duty-cycle applications, by terminating the line at high frequencies but blocking steady-state current flow in the terminating resistor.

Since line receivers are generally used repetitively in a system, the DS7820 has been designed with two independent receivers on a single silicon chip. The device is fabricated on a 41 x 49 mil-square die using the standard six mask planar-epitaxial process. The processing employed is identical to that used on TTL circuits, and the design does not impose any unusual demands on the processing. It is only required that various parts within the circuit match well, but

Line Receiver (Continued)

this is easily accomplished in a monolithic integrated circuit without any special effort in manufacturing. A photomicrograph of the integrated circuit chip is shown in *Figure 11.*

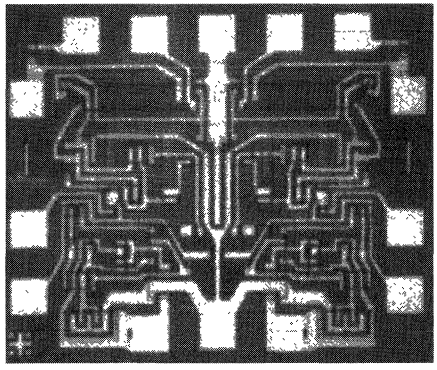


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FIGURE 11. Photomicrograph of the DS7820 Dual Line Receiver

The only components in the circuit which see voltages higher than standard logic circuits are the resistors used to attenuate the input signal. These resistors, R1, R7, R8 and R9, are diffused into a separate, floating, N-type isolation tub, so that the higher voltage is not seen by any of the transistors. For a ±15V input voltage range, the breakdown voltages required for the collector-isolation and collector-base diodes are only 15V and 19V, respectively. These breakdown voltages can be achieved readily with standard digital processing.

The purpose of the foregoing was to provide some insight into circuit operation. A more exact mathematical analysis of the device is developed in Appendix A.

Receiver Performance

The characteristics of the line receiver are described graphically in *Figures 12, 13, 14, 15, 16, 17, 18. Figure 12* illustrates the effect of supply voltage variations on the threshold accuracy. The upper curve gives the differential input voltage required to hold the output at 2.5V while it is supplying 200 µA to the digital load. The lower curve shows the differential input needed to hold the output at 0.4V while it sinks 3.5 mA from the digital load. This load corresponds to a worst case fanout of 2 with either DTL or TTL integrated circuits. The data shows that the threshold accuracy is only affected by ±60 mV for a ±10% change in supply voltage. Proper operation can be secured over a wider range of supply voltages, although the error becomes excessive at voltages below 4V.

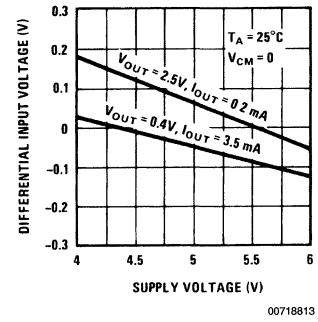

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FIGURE 12. Differential Input Voltage Required for High or Low Output as a Function of Supply Voltage

Figure 13 is a similar plot for varying common mode input voltage. Again the differential input voltages are given for high and low states on the output with a worst case fanout of 2. With precisely matched components within the integrated circuit, the threshold voltage will not change with common mode voltage. The mismatches typically encountered give a threshold voltage change of ±100 mV over a ±20V common mode range. This change can have either a positive slope or a negative slope.

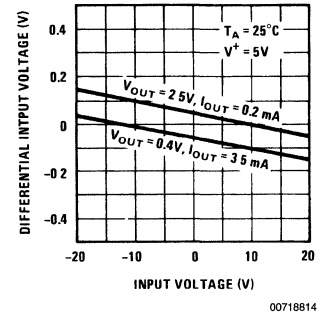

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FIGURE 13. Differential Input Voltage Required for High or Low Output as a Function of Common Mode Voltage

Receiver Performance (Continued)

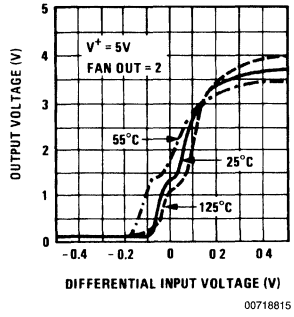


FIGURE 14. Voltage Transfer Function

The transfer function of the circuit is given in *Figure 14*. The loading is for a worst case fanout of 2. The digital load is not linear, and this is reflected as a non-linearity in the transfer function which occurs with the output around 1.5V. These transfer characteristics show that the only significant effect of temperature is a reduction in the positive swing at −55°C. However, the voltage available remains well above the 2.5V required by digital logic.

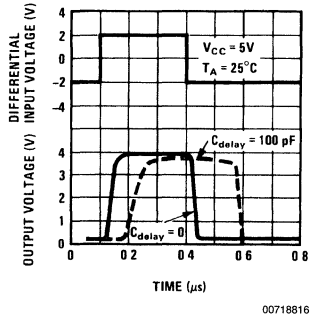


FIGURE 15. Response Time with and without an External Delay Capacitor

Figure 15 gives the response time, or propagation delay, of the receiver. Normally, the delay through the circuit is about 40 ns. As shown, the delay can be increased, by the addition of a capacitor between the response-time terminal and ground, to make the device immune to fast noise spikes on the input. The delay will generally be longer for negative going outputs than for positive going outputs.

Under normal conditions, the power dissipated in the receiver is relatively low. However, with large common mode input voltages, dissipation increases markedly, as shown in *Figure 16*. This is of little consequence with common mode transients, but the increased dissipation must be taken into account when there is a DC difference between the grounds of the transmitter and the receiver It is important to note that *Figure 16* gives the dissipation for one half the dual receiver. The total package dissipation will be twice the values given when both sides are operated under identical conditions.

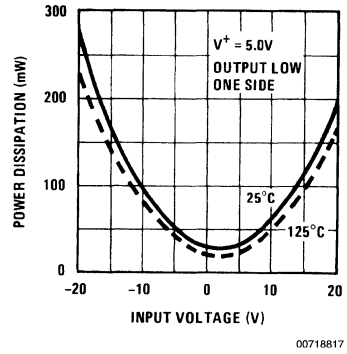


FIGURE 16. Internal Power Dissipation as a Function of Common Mode Input Voltage

Figure 17 shows that the power supply current also changes with common mode input voltage due to the current drawn out of or fed into the supply through R9. The supply current reaches a maximum with negative input voltages and can actually reverse with large positive input voltages. The figure also shows that the supply current with the output switched into the low state is about 3 mA higher than with a high output.

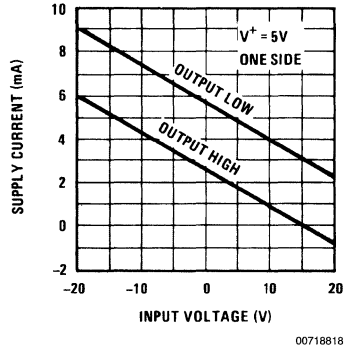


FIGURE 17. Power Supply Current as a Function of Common Mode Input Voltage

The variation of the internal termination resistance with temperature is illustrated in *Figure 18*. Taking into account the initial tolerance as well as the change with temperature, the termination resistance is by no means precise. Fortunately, in most cases, the termination resistance can vary appreciably without greatly affecting the characteristics of the transmission line. If the resistor tolerance is a problem, however, an external resistor can be used in place of the one provided within the integrated circuit.

Receiver Performance (Continued)

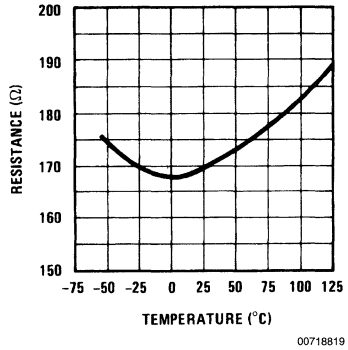
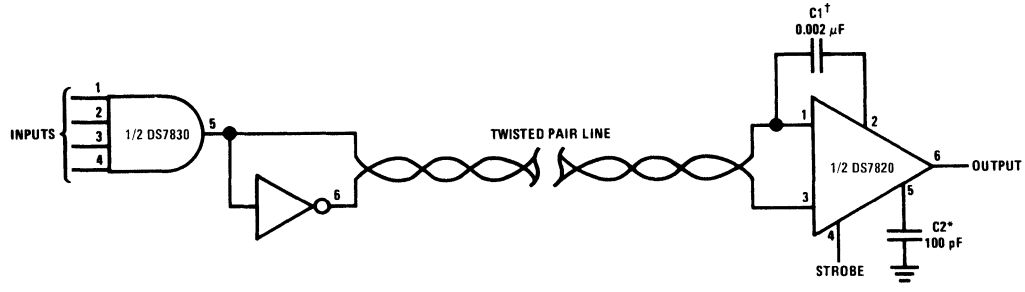


FIGURE 18. Variation of Termination Resistance with Temperature

Data Transmission

The interconnection of the DS7830 line driver with the DS7820 line receiver is shown in *Figure 19*. With the exception of the transmission line, the design is rather straightforward. Connections on the input of the driver and the output or strobe of the receiver follow standard design rules for DTL or TTL integrated logic circuits. The load presented by the driver inputs is equal to 3 standard digital loads, while the receiver can drive a worst-case fanout of 2. The load presented by the receiver strobe is equal to one standard load.

The purpose of C1 on the receiver is to provide DC isolation of the termination resistor for the transmission line. This capacitor can both increase the differential noise immunity, by reducing attenuation on the line, and reduce power dissipation in both the transmitter and receiver. In some applications, C1 can be replaced with a short between Pins 1 and 2, which connects the internal termination resistor of the DS7820 directly across the line. C2 may be included, if necessary, to control the response time of the receiver, making it immune to noise spikes that may be coupled differentially into the transmission lines.



LINE DRIVER AND RECEIVER‡

†Exact value depends on line length

‡V+ is 4 5V to 5 5V for both the DS720 and DS7830

*Optional to control response time

FIGURE 19. Interconnection of the Line Driver and Line Receiver

Data Transmission (Continued)

The effect of termination mismatches on the transmission line is shown in *Figure 20*. The line was constructed of a twisted pair of No. 22 copper conductors with a characteristic impedance of approximately 170Ω. The line length was about 150 ns and it was driven directly from a DS7830 line driver. The data shows that termination resistances which are a factor of two off the nominal value do not cause significant reflections on the line. The lower termination resistors do, however, increase the attenuation.

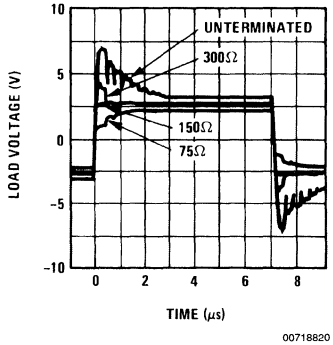


FIGURE 20. Transmission Line Response with Various Termination Resistances

Figure 21 gives the line-transmission characteristics with various termination resistances when a DC isolation capacitor is used. The line is identical to that used in the previous example. It can be seen that the transient reponse is nearly the same as a DC terminated line. The attenuation, on the other hand, is considerably lower, being the same as an unterminated line. An added advantage of using the isolation capacitor is that the DC signal current is blocked from the termination resistor which reduces the average power drain of the driver and the power dissipation in both the driver and receiver.

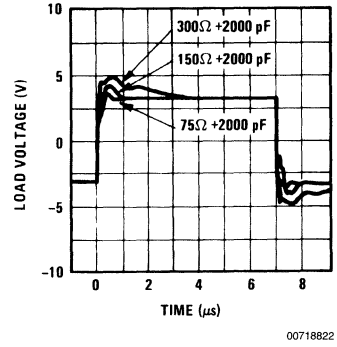


FIGURE 21. Line Response for Various Termination Resistances with a DC Isolation Capacitor

The effect of different values of DC isolation capacitors is illustrated in *Figure 22*. This shows that the RC time constant of the termination resistor/isolation capacitor combination should be 2 to 3 times the line delay. As before, this data was taken for a 150 ns long line.

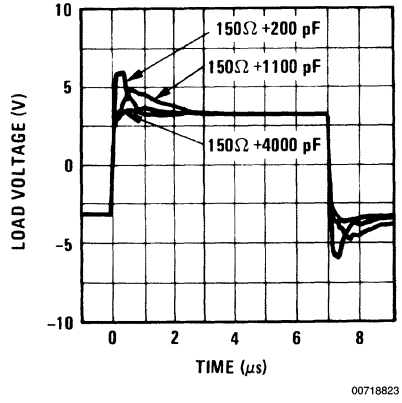
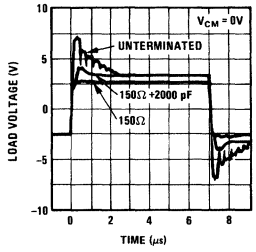
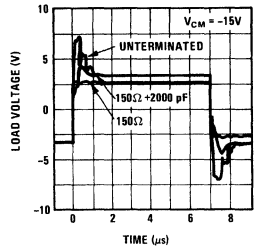


FIGURE 22. Response of Terminated Line with Different DC Isolation Capacitors

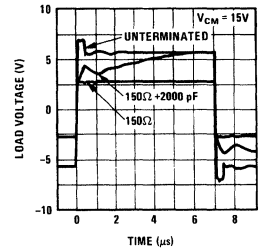
Data Transmission (Continued)



a. V_{CM} = 0V



b V_{CM} = -15V



c V_{CM} = 15V

FIGURE 23. Line Response With Different Terminations and Common Mode Input Voltages

In *Figure 23*, the influence of a varying ground voltage between the transmitter and the receiver is shown. The difference in the characteristics arises because the source resistance of the driver is not constant under all conditions. The high output of the transmitter looks like an open circuit to voltages reflected from the receiving end of the transmission line which try to drive it higher than its normal DC state. This condition exists until the voltage at the transmitting end becomes high enough to forward bias the clamp diode on the 5V supply. Much of the phenomena which does not follow simple transmission-line theory is caused by this. For example, with an unterminated line, the overshoot comes from the reflected signal charging the line capacitance to where the clamp diodes are forward biased. The overshoot then decays at a rate determined by the total line capacitance and the input resistance of the receiver.

When the ground on the receiver is 15V more negative than the ground at the transmitting end, the decay with an unterminated line is faster, as shown in *Figure 23*. This occurs because there is more current from the input resistor of the receiver to discharge the line capacitance. With a terminated line, however, the transmission characteristics are the same as for equal ground voltages because the terminating resistor keeps the line from getting charged.

Figure 23 gives the transmission characteristics when the receiver ground is 15V more positive than the transmitter ground. When the line is not terminated, the differential voltage swing is increased because the high output of the driver will be pulled against the clamp diodes by the common mode input current of the receiver. With a DC isolation capacitor, the differential swing will reach this same value with a time constant determined by the isolation capacitor and the input resistance of the receiver. With a DC coupled termination, the characteristics are unchanged because the differential load current is large by comparison to the common mode current so that the output transistors of the driver are always conducting.

The low output of the driver can also be pulled below ground to where the lower clamp diode conducts, giving effects which are similar to those described for the high output. However, a current of about 9 mA is required to do this, so it does not happen under normal operating conditions.

To summarize, the best termination is an RC combination with a time constant approximately equal to 3 times the transmission-line delay. Even though its value is not precisely determined, the internal termination resistor of the integrated circuit can be used because the line characteristics are not greatly affected by the termination resistor.

The only place that an RC termination can cause problems is when the data transmission rate approaches the line delay and the attenuation down the line (terminated) is greater than 3 dB. This would correspond to more than 1000 ft. of twisted-pair cable with No. 22 copper conductors. Under these conditions, the noise margin can disappear with low-duty-cycle signals. If this is the case, it is best to operate the twisted-pair line without a termination to minimize transmission losses. Reflections should not be a problem as they will be absorbed by the line losses.

Conclusion

A method of transmitting digital information in high-noise environments has been described. The technique is a much more attractive solution than high-noise-immunity logic as it has lower power consumption, provides more noise rejection, operates from standard 5V supplies, and is fully compatible with almost all integrated logic circuits. An additional advantage is that the circuits can be fabricated with integrated circuit processes used for standard logic circuits.

Appendix A

LINE RECEIVER

Design Analysis

The purpose of this appendix is to derive mathematical expressions describing the operation of the line receiver. It will be shown that the performance of the circuit is not greatly affected by the absolute value of the components within the integrated circuit or by the supply voltage. Instead, it depends mostly on how well the various parts match.

The analysis will assume that all the resistors are well matched in ratio and that the transistors are likewise matched, since this is easily accomplished over a broad temperature range with monolithic construction. However, the effects of component mismatching will be discussed

Appendix A (Continued)

where important. Further, large transistor current gains will be assumed, but it will be pointed out later that this is valid for current gains greater than about 10.

A schematic diagram of the DS7820 line receiver is shown in *Figure 24*. Referring to this circuit, the collector current of the input transistor is given by

$$I_{C1} = \frac{V^+ - V_{BE1} - V_{BE3} - V_{BE4}}{R9//R10 + R11 + R3//R8} - \frac{\frac{R3}{R4 + 2R6 + R3} V_{BE1} - \frac{R3//R11}{R8 + R3//R1} V_{IN}}{R9//R10 + R11 + R3//R8} + \frac{(V_{IN} - V^+)\frac{R10//R11}{R9 + R10//R11}}{R9//R10 + R11 + R3//R8} \quad (5)$$

where V_{IN} is the common mode input voltage and $R_a//R_b$ denotes the parallel connection of the two resistors. In *Equation (5)*, R8 = R9, R3 = R10, R10 $\ll$ R11, R9 $\gg$ R10, R3 $\ll$ R11, R8 $\gg$ R3 and

$$\frac{R3}{R4 + 2R6 + R3} \ll 3$$

so it can be reduced to

$$I_{C1} = \frac{V^+ - 3V_{BE} - \frac{R10}{R9} V^+}{R10 + R11 + R3} \quad (6)$$

which shows that the collector current of Q1 is not affected by the common mode voltage.

The output voltage on the collector of Q2 is

$$V_{C2} = V+ - I_{C2}R12 \quad (7)$$

For zero differential input voltage, the collector currents of Q1 and Q2 will be equal so *Equation (7)* becomes

$$V_{C2} = V^+ - \frac{R12\left(V^+ - 3V_{BE} - \frac{R10}{R9} V^+\right)}{R10 + R11 + R3} \quad (8)$$

It is desired that this voltage be $3V_{BE}$ so that the output stage is just on the verge of switching with zero input. Forcing this condition and solving for R12 yields

$$R12 = (R10 + R11 + R3)\frac{V^+ - 3V_{BE}}{V^+ - 3V_{BE} - \frac{R10}{R9} V^+} \quad (9)$$

This shows that the optimum value of R12 is dependent on supply voltage. For a 5V supply it has a value of 4.7 kΩ. Substituting this and the other component values into (*Equation (8)*),

$$V_{C2} = 2.83V_{BE} + 0.081V+, \quad (10)$$

which shows that the voltage on the collector of Q2 will vary by about 80 mV for a 1V change in supply voltage.

The next step in the analysis is to obtain an expression for the voltage gain of the input stage.

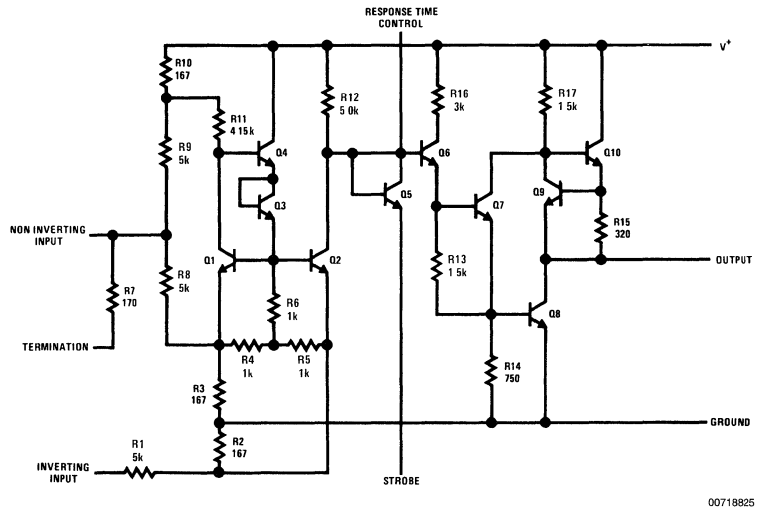


FIGURE 24. Schematic Diagram of One Half of the DS7820 Line Receiver

An equivalent circuit of the input stage is given in *Figure 25*. Noting that R6 = R7 = R8 and R2 ≅ 0.1 (R6 + R7[D]R8), the change in the emitter current of Q1 for a change in input voltage is

$$\Delta I_{E2} = \frac{0.9\,R2}{R1\,(0.9\,R2 + R_{E2})} \Delta V_{IN} \quad (11)$$

Appendix A (Continued)

Hence, the change in output voltage will be

$$\Delta V_{OUT} = \alpha I_{E2} R12 = \frac{0.9\,\alpha\,R2\,R12}{R1\,(0.9\,R2 + R_{E2})}\,\Delta V_{IN} \quad (12)$$

Since $\alpha \cong 1$, the voltage gain is

$$A_{V1} = \frac{0.9\,R2\,R12}{R1\,(0.9\,R2 + R_{E2})} \quad (13)$$

The emitter resistance of Q2 is given by

$$R_{E2} = \frac{kT}{qI_{C2}} \quad (14)$$

$$I_{C2} = \frac{V^+ - 3V_{BE}}{R12} \quad (15)$$

$$R_{E2} = \frac{kT\,R12}{q\,(V^+ - 3V_{BE})} \quad (16)$$

Therefore, at 25°C where V_{VE} = 670 mV and kT/q = 26 mV, the computed value for gain is 0.745. The gain is not greatly affected by temperature as the gain at −55°C where V_{BE} = 810 mV and kT/q = 18 mV is 0.774, and the gain at 125°C where V_{BE} = 480 mV and kT/q = 34 mV is 0.730.

With a voltage gain of 0.75, the results of *Equation (10)* show that the input referred threshold voltage will change by 0.11V for a 1V change in supply voltage. With the standard ±10-percent supplies used for logic circuits, this means that the threshold voltage will change by less than ±60 mV.

Finally, the threshold error due to finite gain in the output stage can be considered. The collector current of Q7 from the bleeder resistor R14, is large by comparison to the base current of Q8, if Q8 has a reasonable current gain. Hence, the collector current of Q7 does not change appreciably when the output switches from a logic one to a logic zero. This is even more true for Q6, an emitter follower which drives Q7. Therefore, it is safe to presume that Q6 does not load the output of the first-stage amplifier, because of the compounded current gain of the three transistors, and that Q8 is driven from a low resistance source.

It follows that the gain of the output stage can be determined from the change in the emitter-base voltage of Q8 required to swing the output from a logic one state to a logic zero state. The expression

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{C1}}{I_{C2}} \quad (17)$$

describes the change in emitter-base voltage required to vary the collector current from one value, I_{C1}, to a second, I_{C2}. With the output of the receiver in the low state, the collector current of Q8 is

$$I_{OL} = \frac{V^+ - V_{OL} - V_{BE9} - V_{BE10}}{R17} + \frac{V_{BE9}}{R15} - \frac{V_{BE8}}{R14} + \frac{V_{BE7}}{R13} + I_{SINK}, \quad (18)$$

where V_{OL} is the low state output voltage and I_{SINK} is the current load from the logic that the receiver is driving. Noting that R13 = 2R14 and figuring that all the emitter-base voltages are the same, this becomes

$$I_{OL} = \frac{V^+ - V_{OL} - 2V_{BE}}{R17} + \frac{V_{BE}}{R15} - \frac{V_{BE}}{2R14} + I_{SINK} \quad (19)$$

Similarly, with the output in the high state, the collector current of Q8 is

$$I_{OH} = \frac{V^+ - V_{OH} - V_{BE9} - V_{BE10}}{R17} + \frac{V_{BE9}}{R15} - \frac{V_{BE8}}{R14} + \frac{V_{BE7}}{R13} - I_{SOURCE}, \quad (20)$$

where V_{OH} is the high-level output voltage and I_{SOURCE} is the current needed to supply the input leakage of the digital circuits loading the comparator.

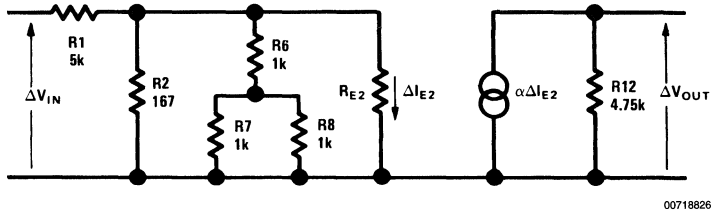


FIGURE 25. Equivalent Circuit Used to Calculate Input Stage Gain

Appendix A (Continued)

With the same conditions used in arriving at (*Equation (19)*), this becomes

$$I_{OH} = \frac{V^+ - V_{OH} - 2V_{BE}}{R17} + \frac{V_{BE}}{R15} - \frac{V_{BE}}{2R14} - I_{SOURCE} \quad (21)$$

From (*Equation (17)*) the change in the emitter-base voltage of Q8 in going from the high output level to the low output level is

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{OL}}{I_{OH}} \quad (22)$$

providing that Q8 is not quite in saturation, although it may be on the verge of saturation.

The change of input threshold voltage is then

$$\Delta V_{TH} = \frac{kT}{qA_{v1}} \log_e \frac{I_{OL}}{I_{OH}} \quad (23)$$

where A_{v1} is the input stage gain. With a worst case fanout of 2, where V_{OH} = 2.5V, V_{OL} = 0 4V, I_{SOURCE} = 40 µA and I_{SINK} = 3.2 mA, the calculated change in threshold is 37 mV at 25°C, 24 mV at −55°C and 52 mV at 125°C.

The measured values of overall gain differ by about a factor of two from the calculated gain. This is not too surprising because a number of assumptions were made which introduce small errors, and all these errors lower the gain. It is also not too important because the gain is high enough where another factor of two reduction would not cause the circuit to stop working.

The main contributors to this discrepancy are the non-ideal behavior of the emitter-base voltage of Q8 due to current crowding under the emitter and the variation in the emitter base voltage of Q7 and Q8 with changes in collector-emitter voltage (h_{RE}).

Although these parameters can vary considerably with different manufacturing methods, they are relatively fixed for a given process. The ΔV_{BE} errors introduced by these quantities, if known, can be added directly into *Equation (22)* to give a more accurate gain expression.

The most stringent matching requirement in the receiver is the matching of the input stage divider resistors: R1 with R8 and R2 with R3. As little as 1% mismatch in one of these pairs can cause a threshold shift of 150 mV at the extremes of the ±15V common mode range. Because of this, it is necessary to make the resistors absolutely identical and locate them close together. In addition, since R1 and R8 do dissipate a reasonable amount of power, they have to be located to minimize the thermal gradient between them. To do this, R9 was located between R1 and R8 so that it would heat both of these resistors equally. There are not serious heating problems with R2 and R3; however, because of their low resistance value, it was necessary even to match the lengths of the aluminum interconnects, as the resistance of the aluminum is high enough to cause intolerable mismatches. Of secondary importance is the matching of Q1 and Q2 and the matching of ratios between R11 and R12. A 1 mV difference in the emitter-base voltages of Q1 and Q2 causes a 30 mV input offset voltage as does a 1% mismatch in the ratio of R11 to R12.

The circuit is indeed insensitive to transistor current gains as long as they are above 10. The collector currents of Q4 and Q6 are made equal so that their base currents load the collectors of Q1 and Q2 equally. Hence, the input threshold voltage is affected only by how well the current gains match. Low current gain in the output transistor, Q8, can cause a reduction in gain. But even with a current gain of 10, the error produced in the input threshold voltage is less than 50 mV.

Transmission Line Drivers and Receivers for TIA/EIA Standards RS-422 and RS-423

National Semiconductor
Application Note 214
John Abbott
John Goldie

Introduction

With the advent of the microprocessor, logic designs have become both sophisticated and modular in concept. Frequently the modules making up the system are very closely coupled on a single printed circuit board or cardfile. In a majority of these cases a standard bus transceiver will be adequate. However because of the distributed intelligence ability of the microprocessor, it is becoming common practice for the peripheral circuits to be physically separated from the host processor with data communications being handled over cables (e.g. plant environmental control or security system). And often these cables are measured in hundreds or thousands of feet as opposed to inches on a backplane. At this point the component wavelengths of the digital signals may become shorter than the electrical length of the cable and consequently must be treated as transmission lines. Further, these signals are exposed to electrical noise sources which may require greater noise immunity than the single chassis system.

It is the object of this application note to underscore the more important design requirements for balanced and unbalanced transmission lines, and to show that National's DS1691 driver and DS78LS120 receiver meet or exceed all of those requirements.

The Requirements

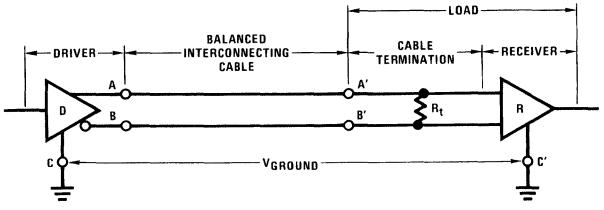
The requirements for transmission lines and noise immunity have been adequately recognized by National Semiconductor's application note AN-108 and TIA/EIA standards TIA/EIA-422-B (balanced) and TIA/EIA-423-B (unbalanced). In this application note the generic terms of RS-422 and RS-423 will be used to represent the respective TIA/EIA standards. A summary review of these notes will show that the controlling factors in a voltage digital interface are:

1. The cable length
2. The data signaling rate
3. The characteristic of the interconnection cable
4. The rise time of the signal

RS-422 and RS-423 contain several useful guidelines relative to the choice of balanced circuits versus unbalanced circuits. *Figure 1* and *Figure 2* are the digital interface for balanced *(1)* and unbalanced *(2)* circuits.

Even though the unbalanced interface circuit is intended for use at lower modulation rates than the balanced circuit, its use is not recommended where the following conditions exist:

1. The interconnecting cable is exposed to noise sources which may cause a voltage sufficient to indicate a change of binary state at the load.
2. It is necessary to minimize interference with other signals, such as data versus clock.
3. The interconnecting cable is too long electrically for unbalanced operation (*Figure 3*).



Legend

R_t = Transmission line termination and/or receiver input impedance

V_{GROUND} = Ground potential difference

A, B = Driver interface

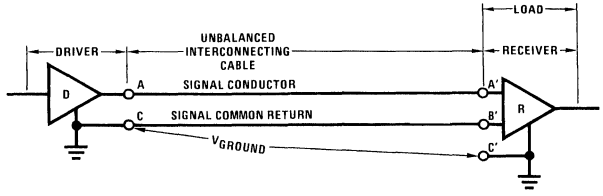
A', B' = Load interface

C = Driver circuit ground

C' = Load circuit ground

FIGURE 1. Balanced Digital Interface Circuit

The Requirements (Continued)



Legend

R_t = Transmission line termination and/or receiver input impedance

V_{GROUND} = Ground potential difference

A, C = Driver interface

A', B' = Load interface

C = Driver circuit ground

C' = Load circuit ground

FIGURE 2. Unbalanced Digital Interface Circuit

Cable Length

While there is no maximum cable length specified, guidelines are given with respect to conservative operating distances as a function of data signaling rate. *Figure 3* is a composite of the guidelines provided by RS-422 and RS-423 for data signaling rate versus cable length. The data is for 24 AWG twisted pair cable terminated for worst case (due to IR drop) in a 100Ω load, with rise and fall times equal to or less than one half unit interval at the applied data rate.

The maximum cable length between driver and load is a function of the data signaling rate. But it is influenced by:

1. A maximum common noise range of ±7 volts
   - A. The amount of common-mode noise
     Difference of driver and receiver ground potential plus driver offset voltage and coupled peak random noise.
   - B. Ground potential differences between driver and load.
   - C. Cable balance
     Differential noise caused by imbalance between the signal conductor and the common return (ground)
2. Cable termination
   At rates above 200 kbps or where the rise time is 4 times the one way propagation delay time of the cable
3. Tolerable signal distortion

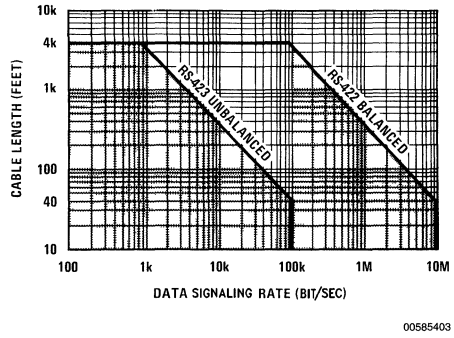


FIGURE 3. Data Signaling Rate vs Cable Length

Data Signaling Rate

The TIA/EIA Standards recommend that the unbalanced voltage interface will normally be utilized on data, timing or control circuits where the data signaling rate on these circuits is below 100 kbps, and balanced voltage digital inter-

Data Signaling Rate (Continued)

face on circuits up to 10 Mbps. The voltage digital interface drivers and receivers meeting the electrical characteristics of this standard need not meet the entire data signaling range specified. They may be designed to operate over narrower ranges to more economically satisfy specific applications, particularly at the lower data signaling rates.

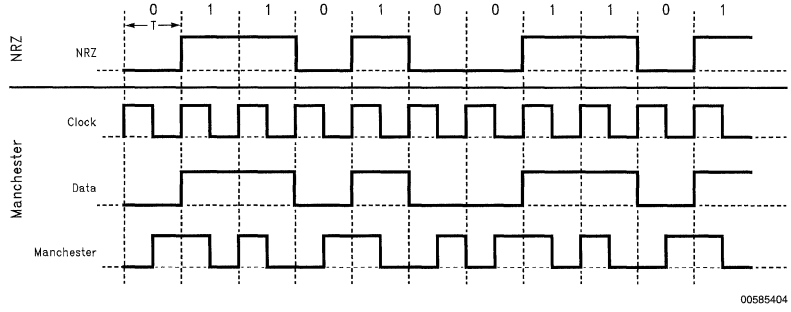
As pointed out in AN-108, the duty cycle of the transmitted signal contributes to the distortion. The effect is the result of rise time. Due to delay and attenuation caused by the cable, it is possible due to AC averaging of the signal, to be unable to reach one binary level before it is changed to another. If the duty cycle is ½ (50%) and the receiver threshold is midway between logic levels, the distortion is small. However if the duty cycle were ⅛ (12.5%) the signal would be considerably distorted.

Characteristics

DRIVER UNBALANCED (RS-423)

The unbalanced driver characteristics as specified by RS-423 are as follows:

1. A driver circuit should be a low impedance (50Ω or less) unbalanced voltage source that will produce a voltage applied to the interconnecting cable in the range of 4V to 6V.
2. With a test load of 450Ω connected between the driver output terminal and the driver circuit ground, the magnitude of the voltage (VT) measured between the driver output and the driver circuit ground shall not be less than 90% of the open circuit voltage magnitude (≥ 3.6V) for either binary state.
3. During transitions of the driver output between alternating binary states, the signal measured across a 450Ω test load connected between the driver output and circuit ground should be such that the voltage monotonically changes between 0.1 and 0.9 of V_{SS}. Thereafter, the signal shall not vary more than 10% of V_{SS} from the steady state value, until the next binary transition occurs, and at no time shall the instantaneous magnitude of VT and $\overline{VT}$ exceed |6V|, nor be less than |3.6V|. V_{SS} is defined as the voltage difference between the two steady state values of the driver output.



	Baud	Bits per Second	Hertz		Baud	Bits per Second	Hertz
CLOCK	—	—	1/T	Manchester	2/T	1/T	—
NRZ	1/T	1/T	—				

Note: bps (bits per second) - Data Information Rate "the number of bits passed along in one second."
baud-Modulation Rate "the reciprocal of the minimum pulse width."
For NRZ bps = bauds

FIGURE 4. Definition of Baud, Bits per Second (bps), Hertz (Hz) for NRZ and Manchester Coding

Characteristics (Continued)

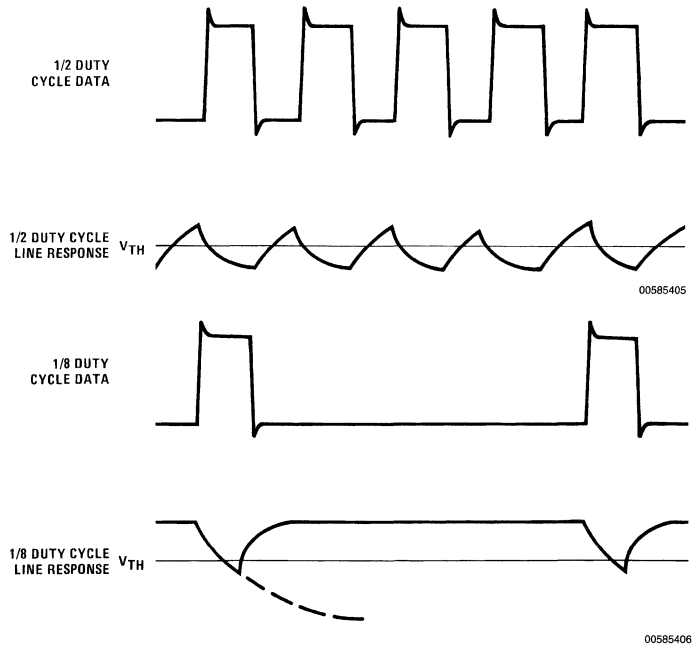
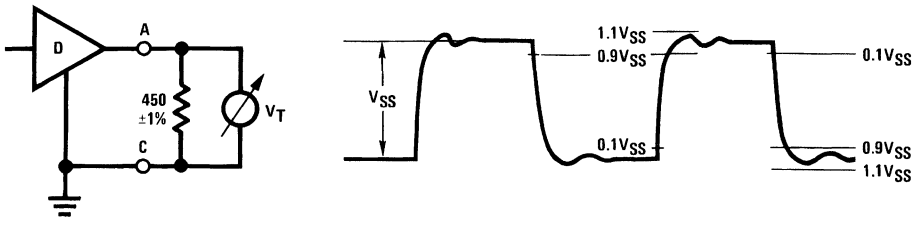


FIGURE 5. Signal Distortion Due to Duty Cycle



$V_{SS} = |V_t - V_t|$

V_{SS} = Difference in steady state voltages

FIGURE 6. Unbalanced Driver Output Signal Waveform

7

Characteristics (Continued)

DRIVER BALANCED (RS-422)

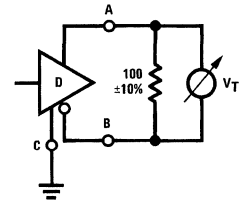
The balanced driver characteristics as specified by RS-422 are as follows:

1. A driver circuit should result in a low impedance (100Ω or less) balanced voltage source that will produce a differential voltage applied to the interconnecting cable in the range of 2V to 10V.
2. With a test load of 2 resistors, 50Ω each, connected in series between the driver output terminals, the magnitude of the differential voltage (VT) measured between the 2 output terminals shall not be less than either 2.0V or 50% of the magnitude of V_O, whichever is greater. For the opposite binary state the polarity of VT shall be reversed ($\overline{VT}$). The magnitude of the difference in the magnitude of VT and $\overline{VT}$ shall be less than 0.4V. The magnitude of the driver offset voltage (V_{OS}) measured between the center point of the test load and driver circuit ground shall not be greater than 3.0V. The magnitude of the difference in the magnitude of V_{OS} for one binary state and $\overline{V_{OS}}$ for the opposing binary state shall be less than 0.4V.
3. During transitions of the driver output between alternating binary states, the differential signal measured across a 100Ω test load connected between the driver output terminals shall be such that the voltage monotonically changes between 0.1 and 0.9 of V_{SS} within 10% of the unit interval or 20 ns, whichever is greater. Thereafter the signal voltage shall not vary more than 10% of V_{SS} from the steady state value, until the next binary transition occurs, and at no time shall the instantaneous magnitude of VT or $\overline{VT}$ exceed 6V, nor less than 2V.

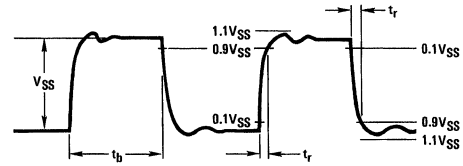
INTERCONNECTING CABLE

The characteristics of the interconnecting cable should result in a transmission line with a characteristic impedance in the general range of 100Ω to frequencies greater than 100 kHz, and a DC series loop resistance not exceeding 240Ω. The cable may be composed of twisted or untwisted pair (flat cable) and is not further specified within the standards.

1. Conductor size of the 2 wires 24 AWG or larger, and wire resistance not to exceed 30Ω per 1000 feet per conductor.
2. Mutual pair capacitance between 1 wire in the pair to the other should be less than 20 pF/ft.



00585408



00585409

t_b = Time duration of the unit interval at the applicable modulation rate

$t_r \leq 0.1\ t_b$ when $t_b \geq 200$ ns

$t_r \leq 20$ ns when $t_b < 200$ ns

V_{SS} = Difference in steady state voltages

$V_{SS} = |V_t - V_t|$

FIGURE 7. Balanced Driver Output Signal Waveform

RECEIVER

The receiver characteristics are identical for both balanced (RS-422) and unbalanced (RS-423) circuits. The electrical characteristics of a single receiver without termination or optional fail-safe provisions are specified as follows:

1. Over an entire common-mode voltage range of −7V to +7V, the receiver shall not require a differential input voltage of more than 200 mV to correctly assume the intended binary state. The common-mode voltage (V_{CM}) is defined as the algebraic mean of the 2 voltages appearing at the receiver input terminals with respect to the receiver circuit ground. Reversing the polarity of VT shall cause the receiver to assume the opposite binary state. This allows for operations where there are ground differences caused by IR drop and noise of up to ±7V.
2. To maintain correct operation for differential input signal voltages ranging between 200 mV and 6V in magnitude.
3. The maximum voltage present between either receiver input terminal and receiver circuit ground shall not exceed 10V (3V signal plus 7V common-mode) in magnitude nor cause the receiver to operationally fail. Additionally, the receiver shall tolerate a maximum differential signal of 12V applied across its input terminals without being damaged.
4. The total load including up to 10 receivers shall not have a resistance less than 90Ω for balanced, and 450Ω for unbalanced at its input points and shall not require a differential input voltage of greater than 200 mV for all receivers to assume the correct binary state.

Characteristics (Continued)

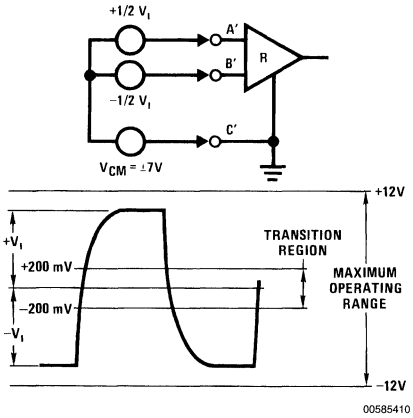


FIGURE 8. Receiver Input Sensitivity Measurement

Signal Rise Time

The signal rise time is a high frequency component which causes interference (near end cross-talk) to be coupled to adjacent channels in the interconnecting cable. The near-end crosstalk is a function of both rise time and cable length, and in considering wave shaping, both should be considered. Since in the balanced voltage digital interface the output is complementary, there is practically no cross-talk coupled and therefore wave shaping is limited to unbalanced circuits.

Per RS-423 the rise time of the signal should be controlled so that the signal has reached 90% of V_{SS} between 10% and 30% of the unit interval at the maximum data signaling rate. Below 1 kbps the time to reach 90% V_{SS} shall be between 100 µs and 300 µs. If a driver is to operate over a range of data signaling rates and employ a fixed amount of wave shaping which meets the specification for the maximum data signaling rate of the operating range, the wave shaping is considered adequate for all lesser modulation rates.

However a major cause of distortion is the effect the transmission line has on the rise time of the transmitted signal. *Figure 9* shows the effect of line attenuation and delay to a voltage step as it progresses down the cable. The increase of the rise time with distance will have a considerable effect on the distortion at the receiver Therefore in fixing the amount of wave shaping employed, caution should be taken not to use more than the minimum required.

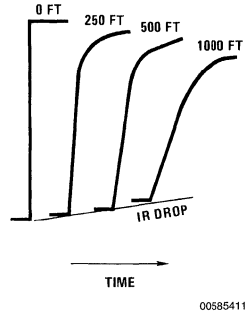


FIGURE 9. Signal Rise Time on Transmission Line vs Line Length

DS1691A/DS78LS120

THE DRIVER

The DS1691A/DS3691 are low power Schottky TTL line drivers designed to meet the above listed requirements of both standards. They feature 4 buffered outputs with high source and sink current capability with internal short circuit protection. The DS1691/DS3691 employ a mode selection pin which allows the circuit to become either a pair of balanced drivers (*Figure 10*) or 4 independent unbalanced drivers (*Figure 11*) When configured for unbalanced operation (*Figure 12*) a rise time control pin allows the use of an external capacitor to control rise time for suppression of near end cross-talk to adjacent channels in the interconnect cable. *Figure 13* is the typical rise time vs external capacitor used for wave shaping. Note that the rise time control capacitors are connected betwen the control pins and the respective outputs.

The DS3691 configured for RS-422 is connected V_{CC} = 5V V_{EE} = 0V, and configured for RS-423 is connected V_{CC} = 5V V_{EE} = −5V. For applications with greater cable lengths the DS1691/DS3691 may be connected with a V_{CC} of 5 volts and V_{EE} of −5 volts. This will create an output which is symmetrical about ground, similar to Mil Standard 188-114.

DS1691A/DS78LS120 (Continued)

This mode is also allowed by the "B" revision of RS-422 (TIA/EIA-422-B) which relaxed to open circuit voltage from 6V to 10V in magnitude.

When configured as balanced drivers (*Figure 10*), each of the drivers is equipped with an independent TRI-STATE® control pin. By use of this pin it is possible to force the driver into its high impedance mode for applications using party line techniques. If the driver is used in multi-point applications (multiple drivers) the use of the response control capacitors is not allowed.

If the common-mode voltage, between driver 1 and all other drivers in the circuit, is small then several line drivers (and receivers) may be incorporated into the system. However, if the common-mode voltage exceeds the TRI-STATE common-mode range of any driver, then the signal will become attenuated by that driver to the extent the common-mode voltage exceeds its common-mode range (see *Figure 14*, top waveform).

It is important then to select a driver with a common-mode range equal to or larger than the common-mode voltage requirement of the system. In the case of RS-422 and RS-423 the minimum common-mode range would be ±7V. The DS1691/DS3691 driver is tested to a common-mode range of ±10V and will operate within the requirements of such a system (see *Figure 14*, bottom waveform).

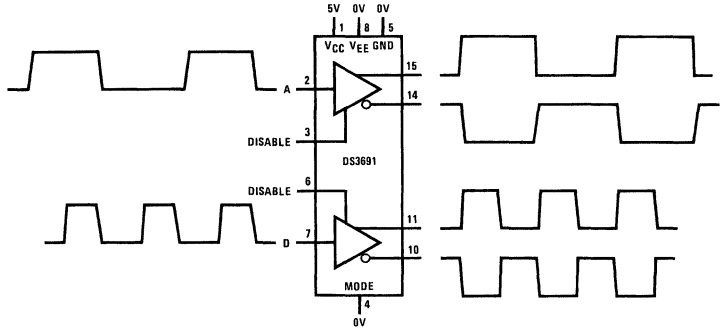


FIGURE 10. DS3691 Connected for Balanced Mode Operation

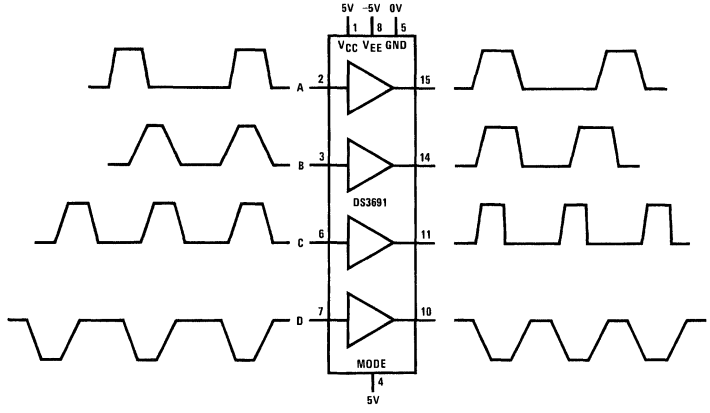


FIGURE 11. DS3691 Connected for Unbalanced Mode Operation (Non-inverting)

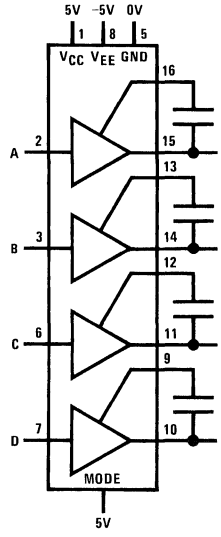


FIGURE 12. Using an External Capacitor to Control Rise Time of DS3691

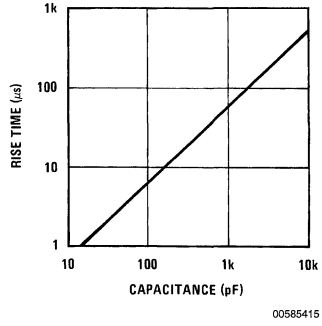


FIGURE 13. DS3691 Rise Time vs External Capacitor

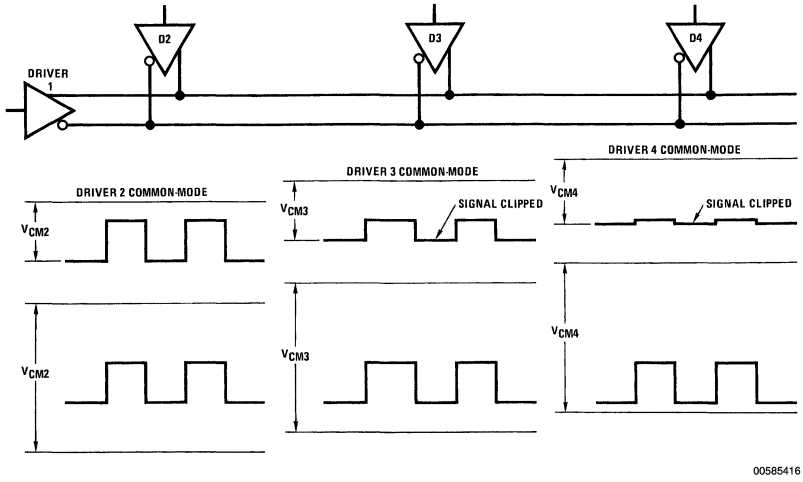
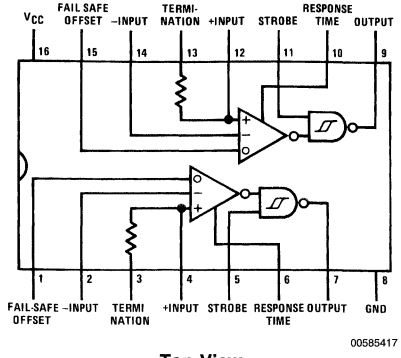


FIGURE 14. Comparison of Drivers without TRI-STATE Common-Mode Output Range (top waveforms) to DS3691 (bottom waveforms)



Top View

FIGURE 15. DS78LS120/DS88LS120 Dual Differential Line Receiver

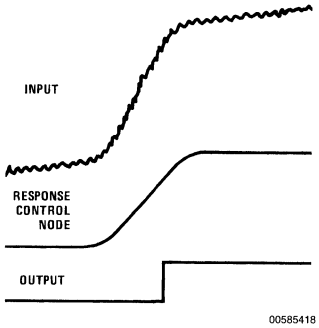
DS78LS120/DS88LS120

THE RECEIVER

The DS78LS120/DS88LS120 are high peformance, dual differential TTL compatible line receivers which meet or exceed the above listed requirements for both balanced and unbalanced voltage digital interface.

The line receiver will discriminate a ±200 millivolt input signal over a full common-mode range of ±10 volts and a ±300 millivolt signal over a full common-mode range of ±15 volts.

The DS78LS120/DS88LS120 include response control for applications where controlled rise and fall times and/or high frequency noise rejection are desirable. Switching noise which may occur on the input signal can be eliminated by the 50 mV (referred to input) of hysteresis built into the output gate (*Figure 16*). The DS78LS120/DS88LS120 makes use of a response control pin for the addition of an external capacitor, which will not affect the line termination impedance of the interconnect cable. Noise pulse width rejection versus the value of the response control capacitor is shown in *Figure 17* . The combination of the filter followed by hysteresis will optimize performance in a worst case noise environment. The DS78C120/DS88C120 is identical in performance to the DS78LS120/DS88LS120, except it's compatible with CMOS logic gates.



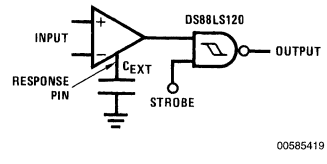
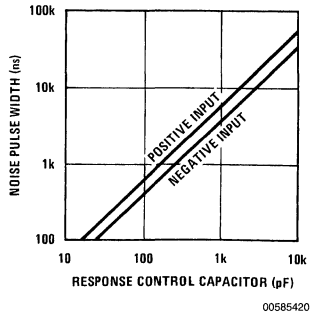


FIGURE 16. Application of DS88LS120 Receiver Response Control and Hysteresis



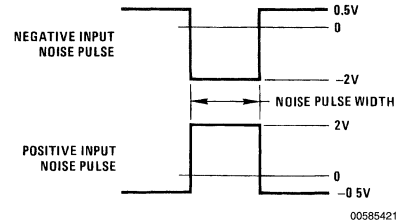


FIGURE 17. Noise Pulse Width vs Response Control Capacitor

Fail-Safe Operation

Some communication systems require elements of a system to detect the loss of signals in the transmission lines. And it is desirable to have the system shut-down in a fail-safe mode if the transmission line is open or short. To facilitate the detection of input opens or shorts, the DS78LS120/DS88LS120 incorporates an input threshold voltage offset. This feature will force the line receiver to a specific logic state if presence of either fault condition exists.

The receiver input threshold is ±200 mV and an input signal greater than ±200 mV insures the receiver will be in a specific logic state. When the offset control input is connected to a V_{CC} = 5V, the input thresholds are offset from 200 mV to 700 mV, referred to the non-inverting input, or −200 mV to −700 mV, referred to the inverting input. Therefore, if the input is open or short, the input will remain in a specific state (see *Figure 18*).

It is recommended that the receiver be terminated in 500Ω or less to insure it will detect an open circuit in the presence of noise.

For unbalanced operation, the receiver would be in an indeterminate logic state if the offset control input was open. Connecting the offset to +5V, offsets the receiver threshold 0.45V. The output is forced to a logic zero state if the input is open or short.

For balanced operation with inputs short or open, receiver C will be in an indeterminate logic state. Receivers A and B will be in a logic zero state allowing the NOR gate to detect the short or open fault condition. The "strobe" input will disable the A and B receivers and therefore may be used to "sample" the fail-safe detector (see *Figure 19*).

Fail-Safe Operation (Continued)

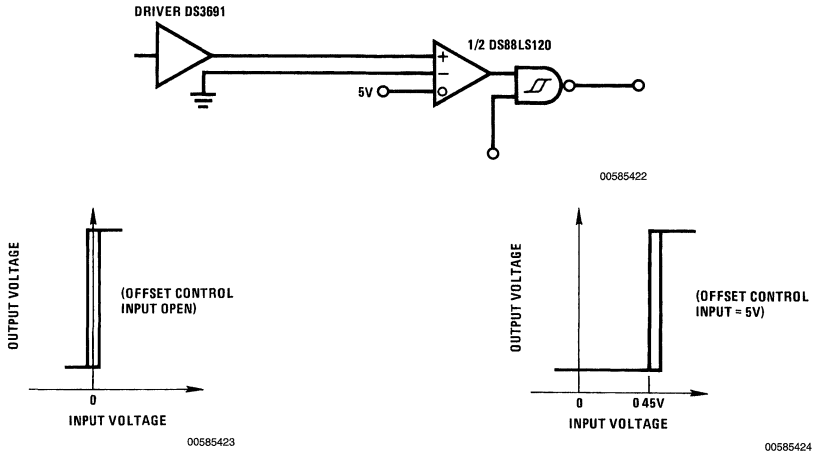


FIGURE 18. Fail-Safe Using the DS88LS120 Threshold Offset for Unbalanced Lines

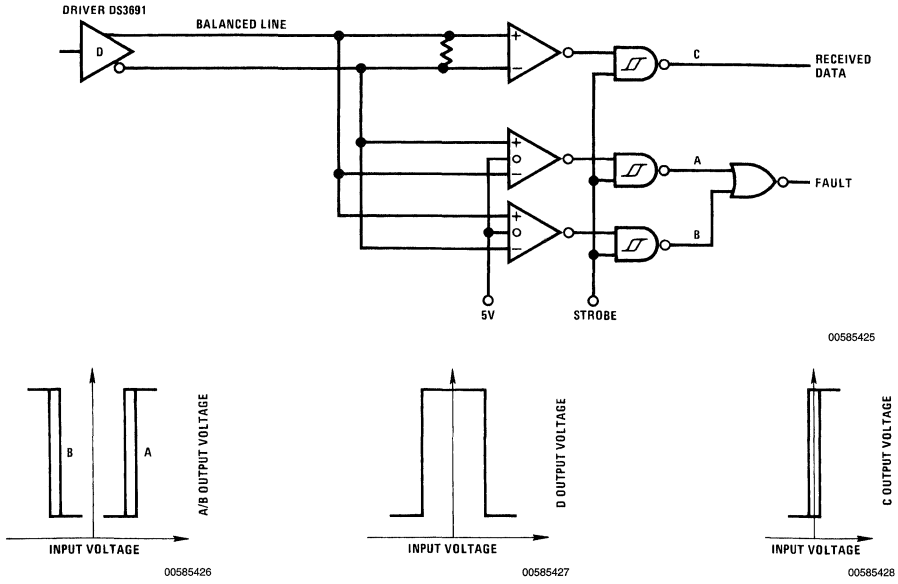


FIGURE 19. Fail-Safe Using the DS88LS120 Threshold Offset for Balanced Lines

Conclusion

This application note provides a brief overview of TIA/EIA-422-B and TIA/EIA-423-B. At the time of publication of this application note the Rev. B standards were draft standard proposals only. For complete/current information on the respective standards the reader is referenced to the respective standards, as minor differences may exist between this document and the final versions.

Summary of Well Known Interface Standards

National Semiconductor
Application Note 216
John Goldie

Forward

Designing an interface between systems is not a simple or straight-forward task. Parameters that must be taken into account include: data rate, data format, cable length, mode of transmission, termination, bus common mode range, connector type, and system configuration. Noting the number of parameters illustrates how complex this task actually is Additionally, the interface's compatibility with systems from other manufacturers is also critically important Thus, the need for standardized interfaces becomes evident. Interface Standards resolve both the compatibility issue, and ease the design through the use of non-custom standardized Drivers and Receivers.

Introduction

This application note provides a short summary of popular Interface Standards. In most cases, a table of the major electrical requirements and a typical application is illustrated. Interface Standards from the following standardization organizations are covered in this application note

- TIA/EIA Telecommunications Industry Association/ Electronics Industry Association
- ITU International Telecommunications Union
- CCITT International Telegraph and Telephone Consultative Committee—now replaced by the ITU
- MIL-STD United States Military Standards
- FED-STD Federal Telecommunications Standard Committee
- Other selected interface standards

There are two basic modes of operation for line drivers (generators) and receivers The two modes are Unbalanced (Single-ended) and Balanced (Differential).

Unbalanced (Single-Ended) Data Transmission

Unbalanced data transmission uses a single conductor, with a voltage referenced to signal ground (common) to denote logical states. In unbalanced communication only one line is switched. The advantage of unbalanced data transmission is when multiple channels are required, a common ground can be used (see *Figure 1*). This minimizes cable and connector size, which helps to minimize system cost. The disadvantage of unbalanced data transmission is in its inability to reliably send data in noisy environments. This is due to very limited noise margins. The sources of system noise can include externally induced noise, cross talk, and ground potential differences.

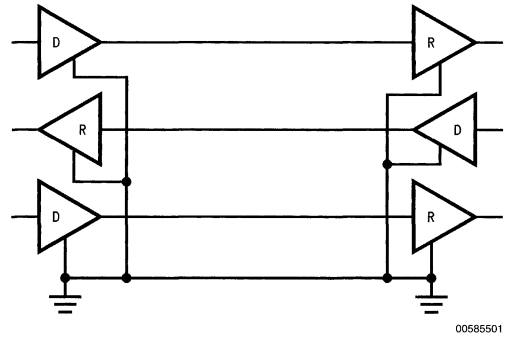


FIGURE 1. Unbalanced Data Transmission- 3 Channel, 4 Line

Balanced (Differential) Data Transmission

Balanced data transmission requires two conductors per signal. In balanced communication two lines are switched. The logical states are referenced by the difference of potential between the lines, not with respect to ground. This fact makes differential drivers and receivers ideal for use in noisy environments (See *Figure 2*). Differential data transmission nullifies the effects of coupled noise and ground potential differences. Both of these are seen as common mode voltages (seen on both lines), not differential, and are rejected by the receivers. In contrast to unbalanced drivers, most balanced drivers feature fast transition times allowing for operation at higher data rates.

Balanced (Differential) Data Transmission (Continued)

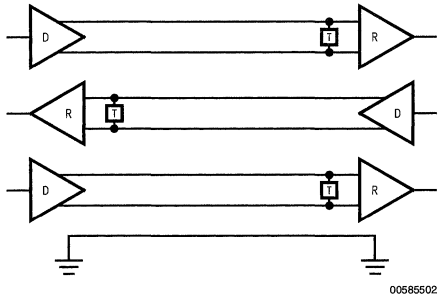


FIGURE 2. Balanced Data Transmission- 3 Channel, 7 Line and Ground

TIA/EIA Data Transmission Standards

The Electronic Industry Association (EIA) and the Telecommunications Industry Association (TIA) are industry trade associations that have developed standards to simplify interfaces in data communication systems. The standards are intended for use in Data Terminal Equipment/Data Circuit-terminating Equipment (DTE/DCE) Interfaces. The classic example of the DTE/DCE interface is the "terminal to modem serial interface". However, the standards are not limited to use in DTE/DCE interfaces alone. In fact, many of the standards are commonly used in a wide variety of applications. Examples include Hard Disk Drive Interfaces, Factory Control Busses, and generic I/O Busses. Previously, EIA labeled the standards with the prefix "RS", which stood for recommended standard. This has been replaced with "TIA/EIA", to help in identifying the source of the standard. The letter suffix represents the revision level of the standard. For example, TIA/EIA-232-E represents the fifth revision of RS-232.

TIA/EIA Data Transmission Standards cover the following areas: Complete Interface Standards, Electrical Only Standards, and Signal Quality Standards. Complete standards define functional, mechanical, and electrical specifications. Electrical only standards, as their name implies only defines electrical specifications. They are intended to be referenced by complete standards. Signal Quality Standards define terms and methods for measuring signal quality. Examples of each type are listed below.

- Complete DTE/DCE Interface Standards
  - TIA/EIA-232-F
  - TIA/EIA-530-A
  - TIA/EIA-561
  - TIA/EIA-574
  - TIA/EIA-613
  - TIA/EIA-687
  - TIA/EIA-688
  - TIA/EIA-723
- Electrical Only Standards
  - Unbalanced Standards
    - TIA/EIA-232-F (Section 2)
    - TIA/EIA-423-B
    - TIA/EIA-562
    - TIA/EIA-694
  - Balanced Standards
    - TIA/EIA-422-B
    - TIA/EIA-485-A
    - TIA/EIA-612
    - TIA/EIA-644
- Signal Quality Standards
  - EIA-334-A
  - EIA-363
  - EIA-404-A

TIA/EIA—Unbalanced (Single-Ended) Standards

TIA/EIA-232-F (RS-232)

TIA/EIA-232-F is the oldest and most widely known DTE/DCE Interface Standard. It is a complete standard specifying the mechanical (connector(s)), electrical (driver/receiver characteristics), and functional (definition of circuits) requirements for a serial binary DTE/DCE Interface. Under the electrical section, the standard specifies an unbalanced, unidirectional, point-to-point interface. The drivers feature a controlled slew rate, this allows the cable to be seen as a lumped load, rather than a transmission line. This is due to the fact that the driver's transition time is substantially greater than the cable delay (velocity x length). The maximum capacitive load seen by the driver is specified at 2,500 pF. The standard allows for operation up to 20 kbps (19.2 kbps). For higher data rates TIA/EIA-562 or TIA/EIA-423-B are recommended. *Figure 3* illustrates a typical application, and *Table 1* lists the major electrical requirements.

Key Features of the standard are:

- Single-Ended
- Point-to-Point Interface
- Large Polar Driver Output Swing
- Controlled Driver Slew Rate
- Fully Defined Interface
- 20 kbps Maximum Data Rate

TABLE 1. TIA/EIA-232-F Major Electrical Specifications

Parameter	Limit & Units
Driver Loaded Output Voltages (3 kΩ)	≥ | 5.0V |
Driver Open Circuit Voltage	≤ | 25V |
Driver Short Circuit Current	≤ | 100 mA |
Maximum Driver Slew Rate	≤ 30 V/μs
Driver Output Resistance (Power Off)	≥ 300Ω
Receiver Input Resistance	3 kΩ to 7 kΩ
Maximum Receiver Input Voltage	±25V
Receiver Thresholds	±3V

TIA/EIA—Unbalanced (Single-Ended) Standards (Continued)

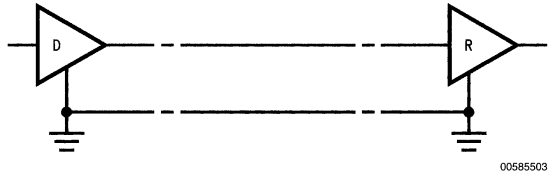


FIGURE 3. Typical TIA/EIA-232-F Application

TIA/EIA-423-B

TIA/EIA-423-B while similar to TIA/EIA-232-F features a reduced driver output swing, and supports higher data rates. This standard specifies an unbalanced driver and a balanced receiver. It is an electrical standard, specifying driver and receiver requirements only. The receivers' requirements are identical to the receivers' requirements specified in TIA/EIA-422-B standard. TIA/EIA-423-B is intended to be referenced by complete standards, such as TIA/EIA-530-A. TIA/EIA-423-B specifies a unidirectional, multidrop (up to ten receivers) interface. Advantages over TIA/EIA-232-F include: multiple receiver operation, faster data rates, and common power supplies (typically ±5V). *Figure 4* illustrates a typical application, and *Table 2* lists the major electrical requirements.

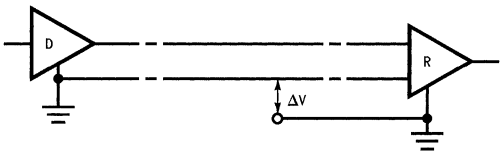


FIGURE 4. Typical TIA/EIA-423-B Application

Key Features of the standard are:

- Unbalanced Driver and Balanced Receivers
- Multi-Drop (multiple receivers)
- Wave Shape Control (Driver Output)
- ±7V Receiver Common Mode Range
- ±200 mV Receiver Sensitivity
- 100 kbps Maximum Data Rate (@40 feet)
- 4000 Foot Maximum Cable Length (@ 1 kbps)

TABLE 2. TIA/EIA-423-B Major Electrical Specifications

Parameter	Limit & Units
Driver Output Voltage (450Ω Load)	≥ |3.6V|
Driver Open Circuit Voltage	≥ |4.0V| & ≤ |6.0V|
Driver Short Circuit Current	≤ |150 mA|
Transition Time	Controlled
Driver Output Leakage Current	≤ |100 μA|
Receiver Specifications	See TIA/EIA-422-B

TIA/EIA-562

TIA/EIA-562 is a electrical standard which is very similar to TIA/EIA-232-F, but supports higher data rates (64 kbps). It is an electrical only standard, which is intended to be referenced by complete standards, such as TIA/EIA-561. TIA/EIA-562 specifies an unbalanced, unidirectional, point-to-point interface. This standard supports inter-operability with TIA/EIA-232-F devices. *Figure 5* illustrates a typical application, and *Table 3* lists the major electrical requirements.

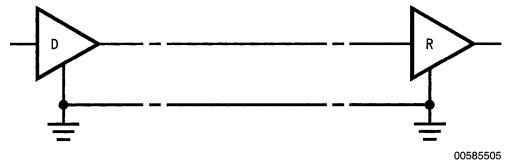


FIGURE 5. Typical TIA/EIA-562 Application

Key Features of the standard are:

- Unbalanced Driver and Receiver
- Point-to-Point
- Inter-Operability with TIA/EIA-232-F Devices
- 64 kbps Maximum Data Rate

TIA/EIA—Unbalanced (Single-Ended) Standards (Continued)

TABLE 3. TIA/EIA-562 Major Electrical Specifications

Parameter	Limit & Units
Driver Loaded Output Voltage (Min. Level)	≥ ∣ 3.3V ∣
Driver Open Circuit Output Voltage	≤ ∣ 13.2V ∣
Driver Loaded Output Voltage (3 kΩ)	≥ ∣ 3.7V ∣
Driver Short Circuit Current	≤ ∣ 60 mA ∣
Driver Transition Time	Controlled
Maximum Driver Slew Rate	≤ 30 V/μs
Driver Output Resistance (Power Off)	≥ 300Ω
Receiver Input Resistance	3 kΩ to 7 kΩ
Maximum Receiver Input Voltage	±25V
Receiver Thresholds	±3V

TIA/EIA-694

TIA/EIA-694 is a new electrical standard which is very similar to TIA/EIA-232-F, but supports higher data rates (512 kbps). It is an electrical only standard, which is intended to be referenced by complete standards, such as TIA/EIA-723. TIA/EIA-694 specifies an unbalanced, unidirectional, point-to-point interface. This standard supports inter-operability with TIA/EIA-232-F devices. *Figure 6* illustrates a typical application, and *Table 4* lists the major electrical requirements.

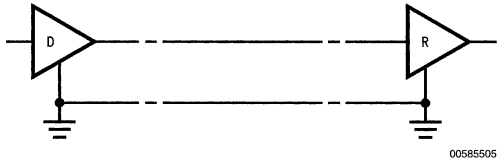


FIGURE 6. Typical TIA/EIA-694 Application

Key Features of the standard are:

- Unbalanced Driver and Receiver
- Point-to-Point
- Inter-Operability with TIA/EIA-232-F Devices
- 512 kbps Maximum Data Rate

TABLE 4. TIA/EIA-694 Major Electrical Specifications

Parameter	Limit & Units
Driver Open Circuit Output Voltage	≤ ∣ 5.5V ∣
Driver Loaded Output Voltage (3 kΩ)	≥ ∣ 3.0V ∣
Driver Short Circuit Current	≤ ∣ 100 mA ∣
Driver Transition Time	Controlled
Receiver Input Resistance	≥ 3 kΩ
Maximum Receiver Input Voltage	±12V
Receiver Thresholds	±2V

TIA/EIA Balanced (Differential) Standards

TIA/EIA-422-B

TIA/EIA-422-B is an electrical standard, specifying a balanced driver and balanced receivers. The receivers' requirements are identical to the receivers' requirements specified in TIA/EIA-423-B. This standard specifies a unidirectional, single driver, multiple receivers, terminated, balanced interface. *Figure 7* illustrates a point-to-point typical application with termination located at the receiver input (end of cable). *Figure 8* illustrates a fully loaded TIA/EIA-422-B interface. Again termination is located at the end of the cable, also stub length should be minimized to limit reflections. *Table 5* lists the major electrical requirements of the TIA/EIA-422-B Standard.

Key Features of the standard are:

- Balanced Interface
- Multi-Drop (Multiple Receiver Operation)
- 10 Mbps Maximum Data Rate (@ 40 feet)
- 4000 Foot Maximum Cable Length (@ 100 kbps)

TIA/EIA Balanced (Differential) Standards (Continued)

TABLE 5. TIA/EIA-422-B Major Electrical Specifications

Parameter	Limit & Units
Driver Open Circuit Voltage	≤ | 10V |
Driver Loaded Output Voltage	≥ | 2.0V |
Balance of Loaded Output Voltage	≤ 400 mV
Driver Output Offset Voltage	≤ 3.0V
Balance of Offset Voltage	≤ 400 mV
Driver Short Circuit Current	≤ |150 mA |
Driver Leakage Current	≤ | 100 µA |
Driver Output Impedance	≤ 100Ω
Receiver Input Resistance	≥ 4 kΩ
Receiver Thresholds	±200 mV
Receiver Internal Bias	≤ 3.0V
Maximum Receiver Input Current	3.25 mA
Receiver Common Mode Range	±7V (±10V)
Receiver Operating Differential Range	±200 mV to ±6V
Maximum Differential Input Voltage	±12V

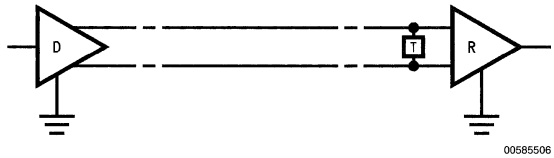


FIGURE 7. Typical TIA/EIA-422-B Point-to-Point Application

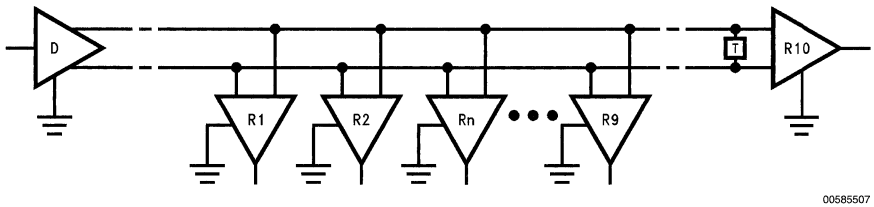


FIGURE 8. Typical TIA/EIA-422-B Multidrop Application

TIA/EIA-485-A

TIA/EIA-485-A is an electrical standard, specifying balanced drivers and receivers. It provides all the advantages of TIA/EIA-422-B along with supporting multiple driver operation. TIA/EIA-485-A is the only TIA/EIA standard that allows for multiple driver operation at this time. This fact allows for multipoint (party line) configurations. The standard specifies a bi-directional (half duplex), multipoint interface. *Figure 9* illustrates a typical multipoint application, and *Table 6* lists the major electrical requirements. For additional applications information, refer to the TIA System Bulletin (TSB89).

Key Features are:

- Balanced Interface
- Multipoint Operation
- Operation From a Single +5V Supply
- −7V to +12V Bus Common Mode Range
- Up to 32 Transceiver Loads (Unit Loads)
- 10 Mbps Maximum Data Rate (@ 40 feet)
- 4000 Foot Maximum Cable Length (@ 100 kbps)

TIA/EIA Balanced (Differential) Standards (Continued)

TABLE 6. TIA/EIA-485-A Major Electrical Specifications

Parameter	Limit & Units
Driver Open Circuit Voltage	≤ | 6.0V |
Driver Loaded Output Voltage	≥ | 1.5V |
Balance of Driver Loaded Output Voltage	≤ | 200 mV |
Maximum Driver Offset Voltage	3.0V
Balance of Driver Offset Voltage	≤ | 200 mV |
Driver Transition Time	≤ 30% Tui
Driver Short Circuit Current (–7V to +12V)	≤ | 250 mA |
Receiver Thresholds	±200 mV
Maximum Bus Input Current +12V/–7V	≤1.0 mA/≤ 0.8 mA
Max. Unit Loads	32

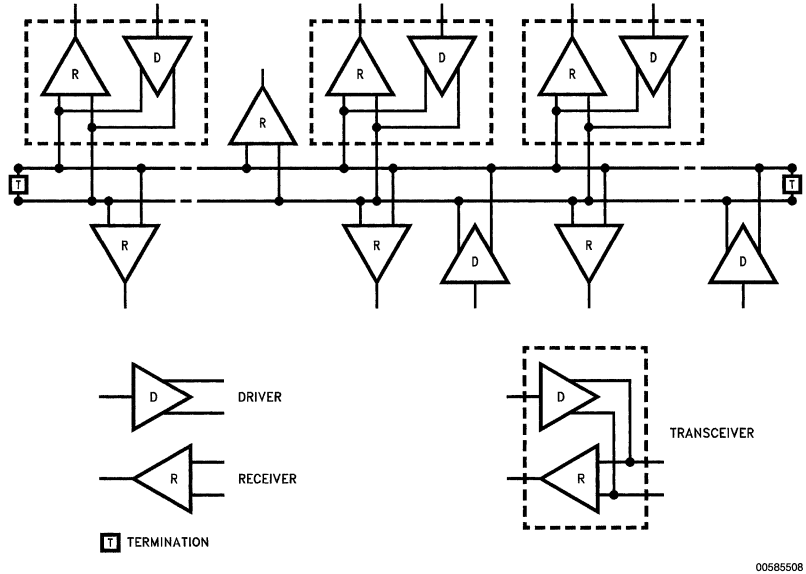


FIGURE 9. Typical TIA/EIA-485-A Application

TIA/EIA Balanced (Differential) Standards

TIA/EIA-612

TIA/EIA-612 is an electrical standard, specifying a balanced driver and balanced receiver. This standard specifies data rates up to 52 Mbps using ECL technology. This standard specifies a unidirectional, point-to-point interface. *Figure 10* illustrates a typical application with termination located at the receiver input (end of cable). *Table 7* lists the major electrical requirements of the TIA/EIA-612 Standard. This Standard is referenced by TIA/EIA-613, and together implement a HSSI (High Speed Serial Interface).

TIA/EIA Balanced (Differential) Standards (Continued)

TABLE 7. TIA/EIA-612 Major Electrical Specifications

Parameter	Limit and Units
Driver Open Circuit Voltage	≤ |1.5V|
Driver Loaded Output Voltage	≥ |590 mV|
Balance of Loaded Output Voltage	≤ |100 mV|
Driver Output Offset Voltage	≤ 0V and ≥ −1.6V
Balance of Offset Voltage	≤ |100 mV|
Driver Short Circuit Current	≤ 50 mA
Receiver Thresholds	±150 mV
Receiver Input Range	−0.5V to −2.0V
Receiver Input Current	≤ 350 µA
Maximum Differential Input Voltage	≤ 1.5V

TIA/EIA-644 (LVDS)

TIA/EIA-644 is an electrical standard, specifying a balanced driver and a balanced receiver(s). This standard specifies data rates up to 655 Mbps (application / device dependent, higher is possible) using LVDS (Low Voltage Differential Signaling) technology. This standard specifies a unidirectional, point-to-point interface. Multiple receivers are supported under certain application limitations. *Figure 10* illustrates the typical point-to-point application with termination (required) located at the receiver input (end of cable). *Table 8* list the major electrical requirements of the TIA/EIA-644 Standard. This Standard is intended to be referenced by other standards which specify the complete interface.

TABLE 8. TIA/EIA-644 LVDS Major Electrical Specifications

Parameter	Limit and Units
Driver Output Voltage	247 mV ≤ Vdiff ≤ 454 mV
Driver Offset Voltage	1.125V ≤ V_{OS} ≤ 1.375
Driver Short Circuit Current	≤ 24 mA
Receiver Thresholds	±100 mV
Receiver Input Range	0V to +2.4V
Receiver Differential Input Range	100 mV to 600 mV
Receiver Input Current	±20 µA

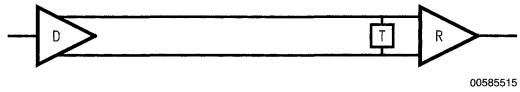


FIGURE 10. Typical TIA/EIA-612 and TIA/EIA-644 Point-to-Point Application

Other TIA/EIA Standards

TIA/EIA-232-F

TIA/EIA-232-F is a standard specifying a DTE/DCE serial interface. It is a complete standard specifying the function of the lines (Data, Timing, & Control) and a 25 position connector. The standard supports data rates up to 20 kbps. Two connector options are provided; a common 25 position D connector, and a smaller 26 position connector.

EIA-334-A

EIA-334-A defines signal quality terms for synchronous serial DTE/DCE interfaces. This standard is referenced by the complete synchronous standards.

EIA-363

EIA-363 defines signal quality terms for non-synchronous serial DTE/DCE interfaces. This standard is referenced by the complete non-synchronous standards.

EIA-404-A

EIA-404-A defines signal quality for start-stop non-synchronous DTE/DCE interfaces.

EIA-449

EIA-449 was a standard specifying a general purpose DTE/DCE serial interface. It was a complete standard specifying the function of the lines (Data, Timing, & Control) and a 37 position connector. This standard referenced 422 and 423 standards for line driver and receiver requirements and characteristics. The standard supports data rates up to 2 Mbps. The size of the specified connector has prevented wide spread acceptance of this standard. New designs are utilizing TIA/EIA-530-A instead of EIA-449 (RS-449).

TIA/EIA-530-A

TIA/EIA-530-A is a complete standard specifying a high speed DTE/DCE serial interface. It is a complete standard specifying the function of the lines (Data, Timing, & Control) and a 25 position connector. This standard references TIA/EIA-422-B and TIA/EIA-423-B standards for line driver and receiver requirements and characteristics. The standard supports data rates up to 2.1 Mbps. Two connector options are provided; a common 25 position D connector, and a smaller 26 position connector.

Note: Connector pinout differences exists between EIA-530 and TIA/EIA-530-A

Other TIA/EIA Standards (Continued)

TIA/EIA-561

TIA/EIA-561 is a complete standard specifying a non-synchronous DTE/DCE serial interface. It is a complete standard specifying the function of the lines (Data, Timing & Control) and a small 8 position connector (MJ8). This standard references TIA/EIA-562 standard for line driver and receiver requirements and characteristics. The standard supports data rates up to 38.4 kbps.

TIA/EIA-574

TIA/EIA-574 is a complete standard specifying a non-synchronous DTE/DCE serial interface. It is a complete standard specifying the function of the lines (Data, Timing, & Control) and a 9 position connector. This standard references TIA/EIA-562 standard for line driver and receiver requirements and characteristics. The standard supports data rates up to 38.4 kbps.

TIA/EIA-613

TIA/EIA-613 is a complete standard specifying a general purpose DTE/DCE interface for data rates up to 52 Mbps. This standard specifies functional and connector specifications and references TIA/EIA-612 for electrical characteristics. Together TIA/EIA-612 and TIA/EIA-613 implement a HSSI interface.

TIA/EIA-687

TIA/EIA-687 is a medium speed standard specifying a DTE/DCE serial interface. It is a complete standard specifying the function of the lines (Data, Timing, & Control) and a 25 or 26 position connector. This standard references TIA/EIA-423-B standard for line driver and receiver requirements and characteristics.

TIA/EIA-688

TIA/EIA-688 is a standard specifying a DTE/DCE serial interface for Digital Cellular Equipment. It is a complete standard specifying the function of the lines (Data, Timing, & Control) and a 12 position (plus coax) connector. This standard references TIA/EIA-694 standard for line driver and receiver requirements and characteristics. The standard supports data rates up to 512 kbps.

TIA/EIA-723

TIA/EIA-723 is a complete standard specifying a high speed DTE/DCE serial interface. It is a complete standard specifying the function of the lines (Data, Timing, & Control) and a 25 or 26 position connector. This standard references TIA/EIA-694 standard for line driver and receiver requirements and characteristics. The standard supports data rates up to 512 kbps.

CCITT RECOMMENDATIONS / ITU-T RECOMMENDATIONS

CCITT (International Telegraph and Telephone Consultative Committee) creates and maintains standards which are intended to help standardize international telecommunication services. These standards are recommended technical practices and approaches, however, in some countries they can be considered mandatory. CCITT reviews its standards on a 4 year cycle. Many of the Interface standards are located in volume eight of the CCITT "V" series. This volume is titled "Data Communication over the Telephone Network". Some of the Interface standards are also covered in the "X" series. The CCITT prefix has been replaced by ITU for International Telecommunications Union and the term CCITT will eventually be phased out. A cross reference is provided in *Table 9*.

TABLE 9. V and X Series Cross Reference

V Series	X Series
V.10	X.26
V.11	X.27

RECOMMENDATION V.10

Recommendation V.10 defines the electrical characteristics for an unbalanced interface. This recommendation specifies an unbalanced driver and a balanced receiver. With the exception of generator (driver) open circuit output voltage specification, V.10 generator (driver) requirements are very similar to the TIA/EIA-423-B standard. In V.10 the driver is loaded with a 3.9 kΩ resistor to ground, while in the TIA/EIA-423-B standard the driver is unloaded. The V.10 receiver is specified with ±300 mV thresholds, while the TIA/EIA-423-B receiver supports a tighter specification of ±200 mV. Other smaller differences also exist. Therefore, for exact conditions and requirements consult the respective standards.

RECOMMENDATION V.11

Recommendation V.11 defines the electrical characteristics for a balanced Interface. V.11 specifies a balanced driver and balanced receivers. With the exception of generator (driver) open circuit output voltage specification, V.11 generator (driver) requirements very similar to the TIA/EIA-422-B standard. V.11 requires a 3.9 kΩ differential load for the driver's open circuit output, while TIA/EIA-422-B test conditions require no load (open circuit) The Receiver specifications are also very similar, with the exception of the input threshold specification. Recommendation V.11 requires thresholds of ±300 mV while TIA/EIA-422-B requires a tighter specification of ±200 mV. Other smaller differences also exist. Therefore, for exact conditions and requirements consult the respective standards.

RECOMMENDATION V.24

Recommendation V.24 defines the function of interchange circuits for DTE/DCE interfaces. Circuit class (Data, Timing, or Control), direction, and definition are all defined in this recommendation. V.24 is intended to be referenced by other recommendations.

RECOMMENDATION V.28

Recommendation V.28 defines the electrical characteristics for an unbalanced Interface. This standard specifies driver output and receiver input characteristics. The standard is very similar to the Electrical section (2) of the TIA/EIA-232-F standard. The one notable exception in the generator (driver) requirements is the slew rate specification. The TIA/EIA-232-F lower limit for slew rate is 3 V/µs (@20 kbps), (measured between the +3V and −3V level), while in V.28 the lower limit is 4 V/µs (@20 kbps). Both standards specify the same upper limit of 30 V/µs under light loading conditions. TIA/EIA-232-F defines the complete interface, while V.28 only defines the electrical section of TIA/EIA-232-F. The complete interface standard is covered by CCITT Recommendations V.28 (electrical), V.24 (functional), and ISO 2110 & 4902 (mechanical). For complete specifications refer to CCITT Recommendation V.28.

Other TIA/EIA Standards (Continued)

RECOMMENDATION V.35

Recommendation V.35 is actually a modem standard that also defines a balanced interface. While many applications operate at data rates substantially higher than 48 kbps (typically > 1 Mbps), the interface is only defined to operate up to 48 kbps. For low speed control lines the standard recommends the use of V.28 generators (drivers) and receivers. For use on high speed data and timing lines the standard recommends the use of unique V.35 balanced generators (drivers). The drivers feature a small swing of ±0.55V across a termination load of 100Ω. The generator is also specified to have polar swings around ground, yielding a 0V offset voltage. Most implementations use differential current mode drivers with external resistors to implement V.35 balanced generators. V.35 has been rescinded, and V.10 and V.11 generators are recommended as replacements.

US Military Standards

MIL STD 188C (LOW LEVEL)

Military Standard 188C (MIL-STD-188C) is similar to TIA/EIA-232-F in the fact that it specifies an unbalanced point-to-point interface. However, the driver's requirements are slightly different. The driver is still required to develop a | 5V | level. The maximum driver output level is specified at | 7V |, and the match between V_{OL} and V_{OH} levels must be within 10% of each other. The driver's slew rate is specified to be between 5% and 15% of the applicable modulation rate. Most drivers require an external capacitor to control the slew rate. *Figure 11* illustrates a typical application, and *Table 10* lists the major electrical specification of MIL-STD-188C.

TABLE 10. MIL-STD-188C Major Electrical Specifications

Parameter	Limit & Units
Unloaded Driver Output Level	±5V Min., ±7V Max.
Driver Output Resistance (Power ON) ($I_O \leq 10$ mA)	100Ω Max.
Driver Output Short Circuit Current	±100 mA
Driver Output Slew Rate	5% to 15% of Modulation Rate
Receiver Input Resistance	≥6 kΩ
Receiver Input Thresholds	±100 µA

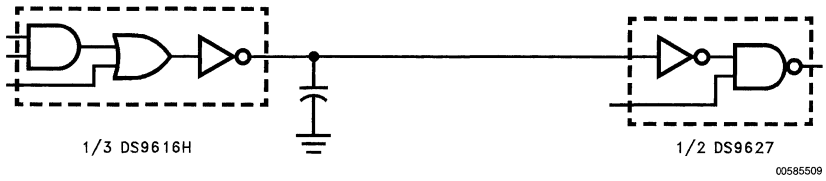


FIGURE 11. Typical MIL-STD-188C Application

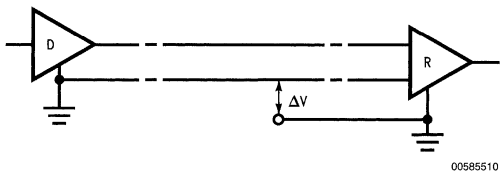


FIGURE 12. MIL STD 188-114A Unbalanced Typical Application

MIL STD 188-114A

Military Standard 188-114 specifies four different interfaces; three balanced and one unbalanced. The balanced interfaces are divided into three types, two of which are voltage mode, and one of which is current mode. See *Figure 12*, *Figure 13* and *Figure 14* . Voltage mode, type 1, defines an interface for data rates up to 100 kbps. An additional requirement of type 1 is a polar (around ground) output swing. This provides a zero offset output voltage. Voltage mode, type 2, drivers operate up to 10 Mbps and require the same parameters as TIA/EIA-422-B drivers. Additionally, type 2, drivers can have an output offset up to 3V. Current mode, type 3, drivers operate beyond 10 Mbps. The receiver specified for type 1 & 2 balanced, and unbalanced drivers are identical to the receivers specified in TIA/EIA-422-B and TIA/EIA-423-B standards.

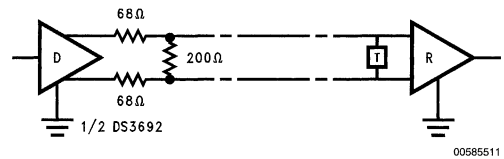


FIGURE 13. MIL STD 188-114A Balanced, Type 1 Typical Application

US Military Standards (Continued)

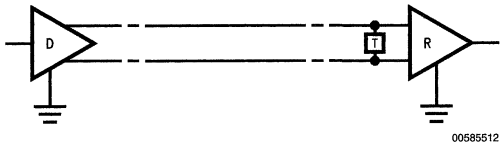


FIGURE 14. MIL STD 188-114A Balanced, Type 2 Typical Application

MIL STD 1397

Military Standard 1397 specifies two interfaces. These are termed "slow" and "fast". The slow interface operates up to 42 kbps, while the fast interface is defined to operate up to 250 kbps. Comparators and/or discretes components are used to implement drivers and receivers.

Federal Telecommunications Standards

Federal Standards are from the Federal Telecommunications Standards Committee, which is an advisory committee that adopts TIA/EIA interface standards.

FED STD 1020A

The FEDSTD 1020A is identical to TIA/EIA-423-B. It is intended for United States, non-military government use.

FED STD 1030A

The FEDSTD 1030A is identical to TIA/EIA-422-B. It is intended for United States, non-military government use.

Other Standards

IEEE488

The IEEE (Institute of Electrical and Electronics Engineers) also has a standard developing arm. Generally the IEEE standards deal with complete Bus specifications. IEEE488 is a complete Bus standard covering the electrical, mechanical, and functional specification of a parallel instrumentation bus. The bus is commonly used for communication of lab test equipment and machinery control. The standard allows for 15 devices to be connected together, over cable lengths up to 60 feet. The standard defines 16 lines composed of 3 control, 5 management, and 8 data lines. The major electrical specifications are summarized in *Table 11*.

TABLE 11. Major IEEE488 Electrical Requirements

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Driver Output Voltage	I_{OH} = −5.2 mA	2.4		V
V_{OL}	Driver Output Voltage	I_{OL} = 48 mA		0.4	V
I_{OZ}	Driver Output Leakage Current	V_O = 2.4V		±40	µA
I_{OH}	Driver Output Current Open Collector	V_O = 5.25V		250	µA
V_{IH}	Receiver Input Voltage		2.0		V
V_{IL}	Receiver Input Voltage			0.8	V
I_{IH}	Receiver Input Current	V_{IN} = 2.4V		40	µA
I_{IL}	Receiver Input Current	V_{IN} = 0.4V		−1.6	mA
I_{CL}	Receiver Clamp Current	V_{IN} = −1.5V		12	mA
RL_1	Termination Resistor	V_{CC} = 5V ±5%	2850	3150	Ω
RL_2	Termination Resistor	V = GND	5890	6510	Ω

GA-22-6974-0

IBM specification GA-22-6974-0 specifies the electrical characteristics, format of information, and the control scheme of an unbalanced interface. This interface is mainly used on 360/370 equipment and allows up to 10 I/O ports. This unbalanced interface employs 95Ω terminated coax cable. Drivers normally feature open-emitter designs, and short-circuit limiting. Receivers normally feature hysteresis to prevent output oscillations for slow rising inputs in noisy environments. Care should be taken to limit cable lengths such that noise is limited to less than 400 mV. *Figure 15* illustrates a typical application, and *Table 12* lists the major electrical requirements.

Other Standards (Continued)

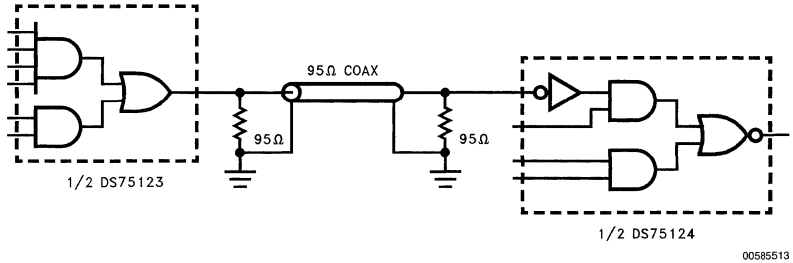


FIGURE 15. GA-22-6974-0 Typical Application

TABLE 12. Major Electrical Requirements of GA-22-6974-0

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Driver Output Voltage	I_{OH} = 123 mA		7	V
V_{OH}		I_{OH} = 30 µA		5.85	V
V_{OH}		I_{OH} = 59.3 mA	3.11		V
V_{OL}		I_{OL} = −240 µA		0.15	V
V_{IH}	Receiver Input Threshold			1.7	V
V_{IL}			0.7		V
I_{IH}	Receiver Input Current	V_{IN} = 3.11V		−0.42	mA
I_{IL}		V_{IN} = 0.15V	0.24		mA
	Receiver Input Voltage Range				
V_{IN}	Power ON		−0.15	7	V
V_{IN}	Power OFF		−0.15	6	V
R_{IN}	Receiver Input Impedance	0.15V ≤ V_{IN} ≤ 3.9V	7.4		kΩ
I_{IN}	Receiver Input Current	V_{IN} = 0.15V		240	µA
Z_O	Cable Impedance		83	101	Ω
R_O	Cable Termination	PD ≤ 390 mW	90	100	Ω
	Noise (Signal and Ground)			400	mV

Conclusion

This application note provides a brief overview of various interface standards from several standardization organizations. It is only intended to point out the major requirements of each standard and to illustrate a typical application. When selecting or designing a standardized interface it is highly recommended to carefully review the complete standard.

Standards can be ordered from the respective organizations or from:

Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112-5704 USA
USA and Canada 1-800-854-7179
International 303-397-7956
http://global.ihs.com/

Low Power RS-232C Driver and Receiver in CMOS

National Semiconductor
Application Note 438
Gordon W. Campbell

This article sets out to describe the new innovative low power CMOS RS-232C driver and receiver IC's introduced by National Semiconductor with particular reference to the EIA RS-232C standard. Comparison will also be made with existing bipolar driver and receiver circuits.

The DS14C88 and DS14C89A are monolithic MOS circuits utilizing a standard CMOS process. Important features are a wide operating voltage range (4.5V–12.6V), together with ESD and latch up protection and proven reliability.

The Electronics Industries Association released Data Terminal Equipment (DTE) to Data Communications Equipment (DCE) interface standards to cover the electrical, mechanical and functional interface between/among terminals (i.e. teletypewriters, CRT's etc.) and communications equipment (i.e. modems, cryptographic sets etc.).

The EIA RS-232C is the oldest and most widely known DTE/DCE standard. Its European version is CCITT V.24 specification. It provides for one-way/non-reversible, single ended (unbalanced) non-terminated line, serial digital data transmission.

The DS14C88 quad CMOS driver and its companion circuit, the DS14C89A quad CMOS receiver, combine to provide an efficient low power system for RS-232C or CCITT V.24 applications.

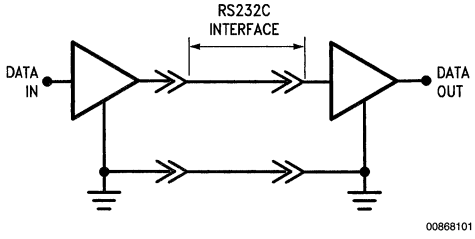


FIGURE 1. EIA RS-232C Application

The Driver

The DS14C88 quad CMOS line driver is a pin replacement of the existing bipolar circuit DS1488/MC1488.

The DS14C88 is fabricated in CMOS technology and therefore has an inherent advantage over the bipolar DS1488/MC1488 line driver in terms of current consumption. Under worst case static conditions, the DS14C88 is a miser when it comes to current consumption. In comparison with the DS1488/MC1488 line driver, a current consumption reduction to 500 µA max versus 25 mA can be achieved.

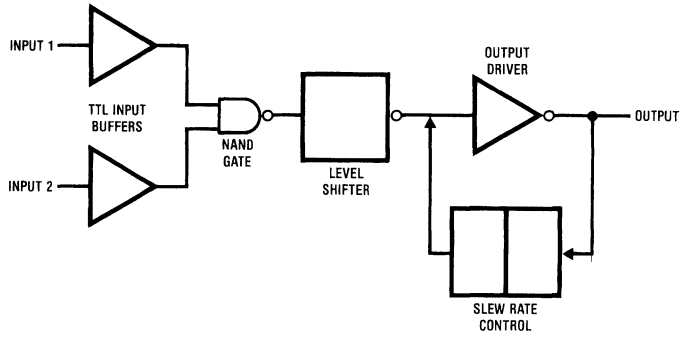
The RS-232C specification states that the required driver output voltage is defined as being between +5V and +15V and is positive for a logic "0" (+5V to +15V) and negative for a logic "1" (–5V to –15V). These voltage levels are defined when driver is loaded ($3000\Omega < R_L < 7000\Omega$). The DS14C88 meets this voltage requirement by converting HC or TTL/LSTTL levels into RS-232C levels through one stage of inversion.

In applications where strict compliance to RS-232C voltage levels is not essential, a ±5V power supply to the driver may be used. The output voltage of the DS14C88 will be high enough to be recognized by either the 1489 or 14C89A receiver as valid data.

The RS-232C specification further states that, during transitions, the driver output slew rate must not exceed 30V/µs. The inherent slew rate of the equivalent bipolar circuit DS1488/MC1488 is much too fast and requires the connection of one external capacitor (330–400 pF) to each driver output in order to limit the slew rate to the specified value. However, the DS14C88 does not require any external components. The DS14C88 has a novel feature in that unique internal slew rate control circuitry has been incorporated which eliminates the need for external capacitors; to be precise, a saving of four capacitors per package. The 14C88 minimizes RFI and transition noise spikes by typically setting the slew rate at 5V–6V/µs. This will enable optimum noise performance, but will restrict data rates to below 40k baud.

The DS14C88 can also withstand an accidental short circuit from a conductor in the interconnecting cable to any one of four outputs in a package without sustaining damage to itself or its associated equipment.

The Driver (Continued)



(¼ circuit shown)

FIGURE 2. DS14C88 Line Driver Block Diagram

The Receiver

The DS14C89A quad CMOS line receiver is a pin replacement of the existing bipolar circuit DS1489/MC1489/DS1489A/MC1489A.

The DS14C89A is fabricated in CMOS technology giving it an inherent advantage over the bipolar DS1489/MC1489/DS1489A/MC1489A circuits in terms of power consumption. Under worst case static conditions a power consumption reduction of 97% (900 µA against 26 mA) is achieved.

The RS-232C specification states that the required receiver input impedance as being between 3000Ω and 7000Ω for input signals between 3.0V and 25.0V. Furthermore, the receiver open circuit bias voltage must not be greater than +2V.

The DS14C89A meets these requirements and is able to level shift voltages in the range of −30V to +30V to HC or TTL/LSTTL logic levels through one stage of inversion. A voltage of between −3.0V and −25.0V is detected as a logic "1" and a voltage of between +3.0V and +25.0V is detected as logic "0".

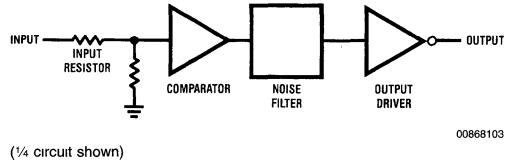
The RS-232C specification states that the receiver should interpret an open circuit or power off condition (source impedance of driver must be 300Ω or more to ground) as an OFF condition. In order to meet this requirement the input threshold of the DS14C89A is positive with respect to ground resulting in an open circuit or "power off" condition being interpreted as a logic "0" at the input.

Although the DS14C89A is pin replacement for the bipolar circuits DS1489/MC1489/DS1489A/MC1489A, its performance characteristics are modeled on the DS1489A/MC1489A.

The response control input on each of the bipolar circuits facilitates the rejection of noise signals by means of an external capacitor between each response control pin and ground.

When communicating between components of a data processing system in a hostile environment, spurious data such as ground shifts and noise signals may be introduced and it can become difficult to distinguish between a valid data signal and those signals introduced by the environment.

The DS14C89A eliminates the need for external response control capacitors and overcomes the effects of spurious data by means of unique internal noise filtering circuitry. *Figure 4* shows typical turn on threshold versus response control capacitance for existing bipolar devices. Note the curve for the DS14C89A CMOS device. The DS14C89A will not recognize any input signal whose pulse width is less than 1 µs, regardless of the voltage level of that input signal. Noise rejection in the bipolar parts depends on the voltage level of the noise transients. Therefore, in hostile environments the CMOS parts offer improved noise rejection properties. The DS14C89A has an internal comparator which provides input hysteresis for noise rejection. The DS14C89A has a typical turn-on voltage of 2.0V and a typical turn-off voltage of 1.0V resulting in 1.0V of hysteresis.



(¼ circuit shown)

FIGURE 3. DS14C89A Line Receiver Block Diagram

The Receiver (Continued)

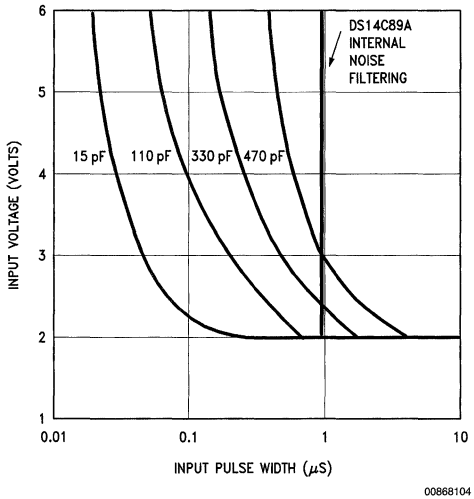


FIGURE 4.

Typical Applications

Obviously the major advantage of these CMOS devices is that with the large reduction of operating current, it is now possible to implement the "FULL" RS-232 interface in remote or portable equipment. Imagine that previously a designer, using a CMOS µP, RAM, ROM, and peripherals, could implement a complete system that consumes between 200 and 300 mW, but just adding the RS-232 interface (one driver, and one receiver) would add another 450 to 700 mW to the total system power consumption. This would severely shorten the battery life. The CMOS driver and receiver would only add about 40–50 mW.

In addition, the CMOS devices provide better noise rejection in harsh EMI environments, thus better data integrity. At the same time the internal slew rate limiting of the driver reduces the output transition time along the cable interface, hence reducing RFI emission, and easing the ability for portable (or non-portable) systems to meet FCC noise emission regulations. Also, since space is a premium in remote and portable systems, by integrating the function of the external capacitors on-chip (eliminating 8 capacitors), and designing these into S.O. packages, significant reduction in board space can be achieved.

For example, *Figure 5* shows a small CMOS system utilizing a CMOS NSC800 microprocessor, NSC858 CMOS UART, CMOS RAM/ROM, and a clock timer. This system runs off a 9V battery so a DC–DC converter is used to generate –9V for the RS-232 interface. In this design a standard DC–DC convert IC is used to generate a –9V supply from the single +9V battery.

As a second example, a "cheater" RS-232 interface is sometimes implemented. This interface is compatible with the current RS-232 driver/receiver products, but rather than using a ±(9–15)V supply, a ±5V supply is used. The drivers will not meet the RS-232 output voltage level specifications, but will correctly drive either the CMOS or bipolar receivers. The DC–DC converter circuit in *Figure 5* may be used to implement this. While for non-portable applications this can be done with the old bipolar 1488/89s, the DC–DC converter is somewhat simpler with the CMOS parts due to the much reduced current consumption.

The RS-232 driver/receivers are also useful in non-power sensitive multi-user computers. Imagine a 16 terminal cluster controller for a multi-user computer system, *Figure 6*. This controller would require 16 drivers and 16 receivers with a total power of 8 watts when using the bipolar devices. The CMOS devices need only 400 mW.

Also proper noise rejection for receivers and slew rate limiting for the driver would require 128 capacitors for the bipolar parts, but they are unnecessary in the CMOS implementation.

Typical Applications (Continued)

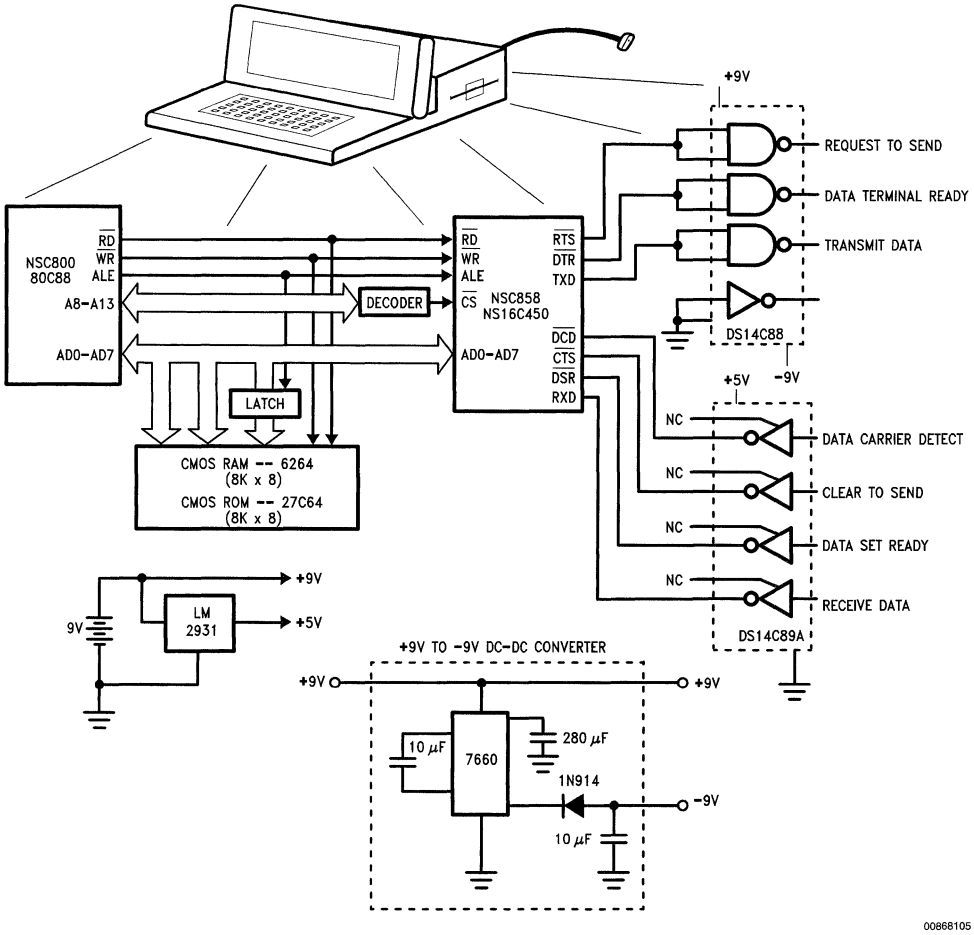


FIGURE 5. Typical portable system application using CMOS μP, ROM, RAM, and UART. RS-232 interface is shown using 7660 supply inverter and CMOS Receiver/Driver.

Typical Applications (Continued)

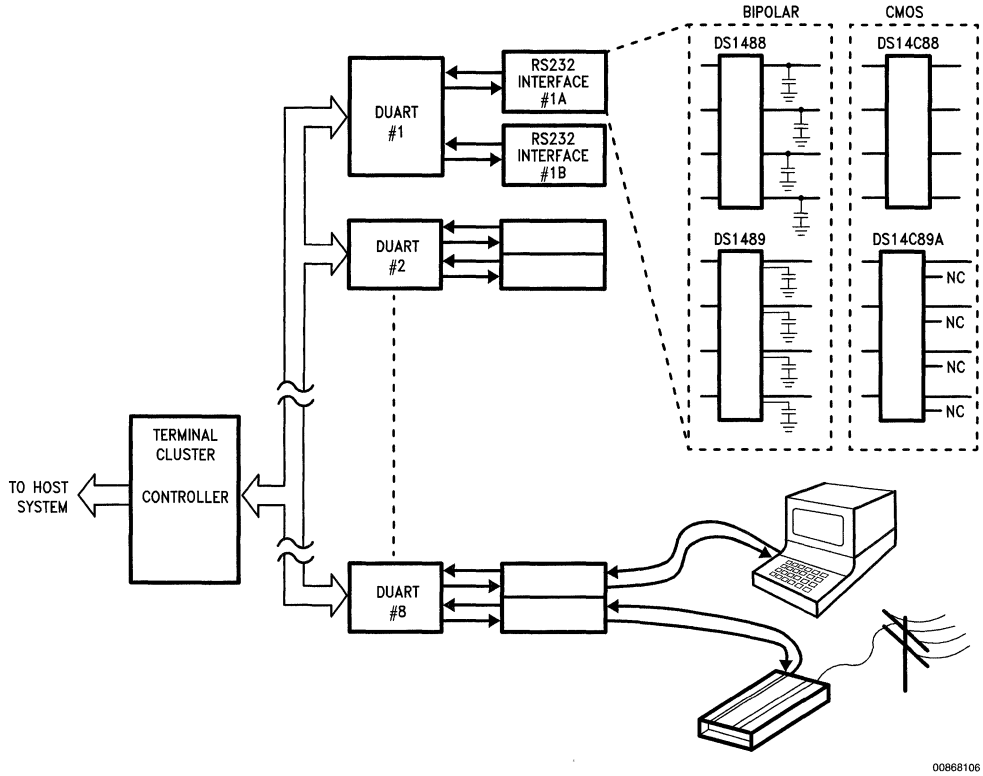


FIGURE 6. A multi-terminal application showing a comparison of Bipolar vs CMOS solutions.

High Speed, Low Skew RS-422 Drivers and Receivers Solve Critical System Timing Problems

National Semiconductor
Application Note 457
Toan Tran
Larry Kendall

In system design, due to the distributed intelligence ability of the microprocessor, it is a common practice to have the peripheral circuits physically separated from the host processor with data communications being handled over cables. Usually, these cables are measured in hundreds or thousands of feet. Signals transmitted on these lines (or cables) are exposed to electrical noise sources which may require large noise immunity. The requirements for transmission lines and noise immunity are covered in E.I.A. standard RS-422.

The object of this application note is to describe the design requirement of RS-422 standard and to show that National's DS8921, DS8922 and DS8923 Differential Driver and Receiver pair meet all of those requirements. Special circuit design techniques are used to achieve small skew on complementary signals of the driver outputs. In fact, these devices are designed specifically for applications which must meet stringent timing constraints including the ESDI Disk Drive standard. Additionally, the DS8921 series meet the requirement of ST506 and ST412HP standards.

Balanced Voltage Digital Interface Circuits (RS-422) Requirement

Balanced circuits are normally used in data, timing, or control applications where the data signaling rate approaches speeds of 10 Mbit/s In addition, balanced data transmission techniques should be used whenever the following conditions exist:

1. The interconnecting cable is too long for effective unbalanced operation.
2. The interconnecting cable is exposed to a noise source which may cause a voltage sufficient to indicate a change of binary state at the load.
3. It is necessary to minimize interference with other signals.

Figure 2 below is a balanced circuit connection.

There are three major controlling factors in balanced voltage digital interface:

1. The cable length
2. The modulation rate
3. The characteristics of the Driver and Receiver

Cable Length

There is no maximum cable length specified in the RS-422 standard. Guidelines are given with respect to conservative operating distances as a function of modulation rate. *Figure 1* below is the guideline provided by RS-422 for data modulation rate versus cable length.

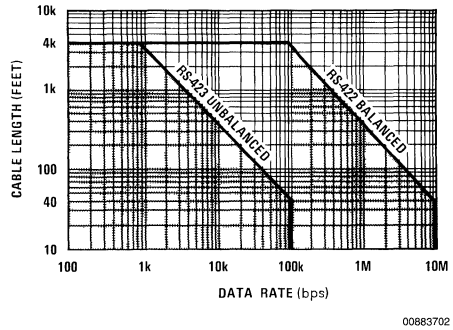
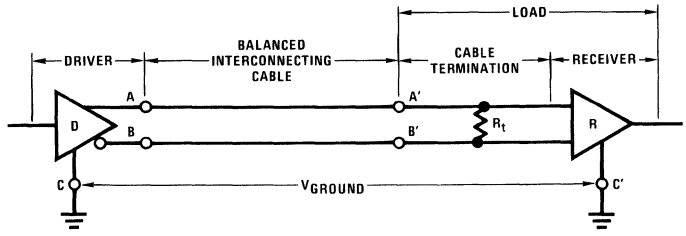


FIGURE 1. Data Modulation Rate vs Cable Length

The curve is based on empirical data using a 24 AWG, copper conductor, twisted pair cable terminated for worst case in a 100Ω load, with rise and fall time equal or less than one half unit interval at the applied modulation rate.

Even though the maximum cable length between driver and load is a function of data signaling rate, it is also influenced by the tolerable signal distortion, the amount of longitudinally coupled noise and ground potential difference introduced between the generator and load circuit grounds.

Cable Length (Continued)



Legend

R_t = Optional cable transmission resistance/receiver input impedance.

V_{GROUND} = Ground potential difference

A, B = Driver interface

A', B' = Load Interface

C = Driver circuit ground

C' = Load circuit ground

FIGURE 2. RS-422 Balanced Digital Interface Circuit

Modulation Rate

The balanced (or differential) voltage mode interface will normally be utilized on data, timing or control circuits operating at up to 10 Mbps. The voltage digital interface devices meeting the electrical characteristics of this standard need not meet the entire modulation range specified. They may be designed to operate over narrower ranges to more economically satisfy specific applications, particularly at the lower modulation rates. The DS8921 family of devices meets or exceeds all of the recommended RS-422 performance specifications.

RS-422 Characteristics

A. The Driver

The balanced driver characteristics are specified in RS-422 as follows:

1. A driver circuit should result in a low impedance (100Ω or less) balanced voltage source that will produce a differential voltage to the interconnecting cable in the range of 2V to 6V.
2. With a test load of 2 resistors, 50Ω each, connected in series between the driver output terminals, the magnitude of the differential voltage (VT) measured between the two output terminals shall be equal to or greater than 2V, or 50% of the magnitude of V_O, whichever is greater. For the opposite binary state the polarity of VT is reversed ($\overline{VT}$).
3. During transitions of the driver output between alternating binary states, the differential voltage measured across 100Ω load shall monotonically change between 0.1 and 0.9 of V_{SS} within 0.1 of the unit interval or 20 ns, whichever is greater. Thereafter, the signal voltage shall not change more than 10% of V_{SS} from the steady state value until the binary state occurs.

B. The Receiver

The electrical characteristics of the receiver are specified in RS-422 as follows:

1. The receiver shall not require a differential input voltage more than 200 mV to correctly assume the intended binary state, over an entire common-mode voltage range of −7 to +7V. The common-mode voltage (V_{CM}) is defined as the algebraic mean of the 2 voltages appearing at the receiver input terminals with respect to the receiver circuit ground. This allows for operations where there are ground differences caused by IR drop and noise of up to ±7V.
2. The receiver shall maintain correct operation for a differential input signal ranging between 200 mV and 6V in magnitude.
3. The maximum voltage between either receiver input terminal and receiver circuit ground shall not exceed 10V (3V signal +7V common-mode) in magnitude. Also, the receiver shall tolerate a maximum differential signal of 12V applied across its input terminals without being damaged.
4. The total load (up to 10 receivers) shall not have a resistance more than 90Ω at its input points.

DS8921, DS8922 andDS8923

The DS8921 is a single differential line driver and receiver pair. Whereas, the DS8922 and DS8923 are dual differential line driver and receiver pairs. The difference between the DS8922 and DS8923 is in the TRI-STATE® control (*Figure 3*).

These devices are designed to meet the full specifications of RS-422. The driver features high source and sink current capability.

The receiver will discriminate a ±200 mV input signal over a full common-mode range of ±7V. Switching noise which may occur on input signal can be eliminated by the built-in hysteresis (50 mV typical, and 15 mV min.). An input fail-safe circuit is provided so that if the receiver inputs are open, the output will assume the logical one state.

DS8921, DS8922 andDS8923

(Continued)

These devices have power up/down circuitry that will TRI-STATE the outputs and prevent erroneous glitches on the transmission lines during system power up or down operation.

The most attractive feature of these devices is the small skew beween the complementary outputs of the driver, typically about 0.5 ns. This small skew specification is often necessary to meet tight system timing requirements.

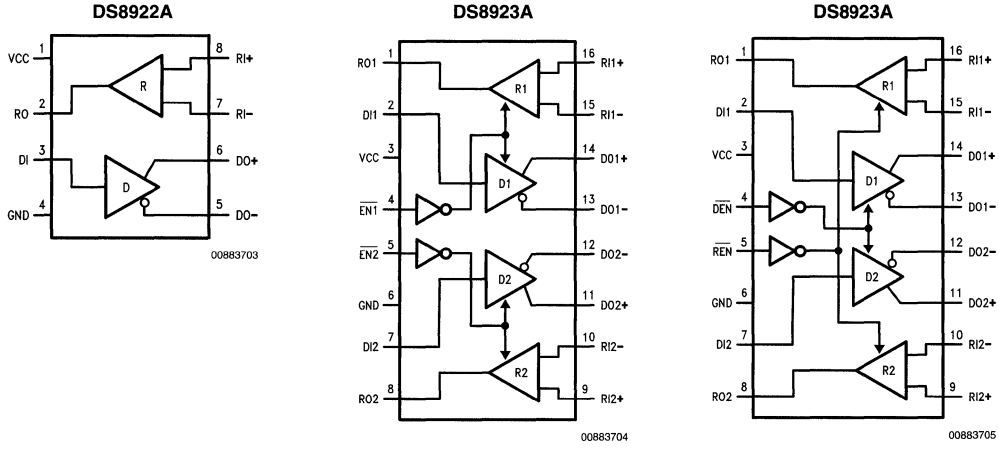
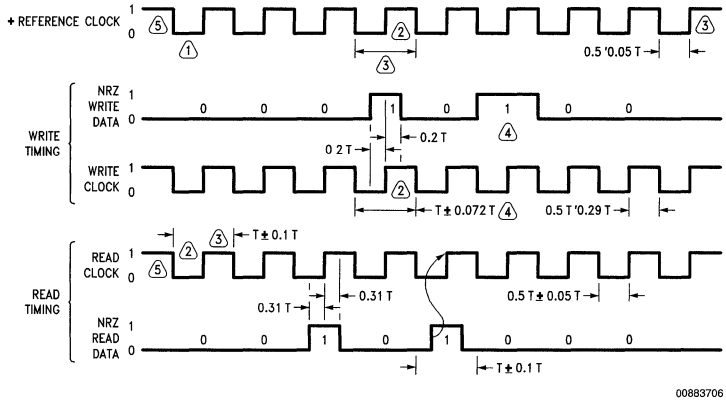


FIGURE 3. DS8921A, DS8922A and DS8923A Connection Diagrams



Note 1: All times in ns measured at I/O connector of the drive T is the period of the clock signals and is the inverse of the reference or read clock frequency

Note 2: Similar period symmetry shall be in ±4 ns between any two adjacent cycles during reading and writing

Note 3: Except during a head change or PLO synchronization the clock variances for spindle speed and circuit tolerances shall not vary more than −5 5% to +5 0% Phase relationship between reference clock and NRZ write data or write clock is not defined

Note 4: The write clock must be the same frequency as the drive supplied reference clock (i e , the write clock is the controller received and retransmitted drive reference clock)

Note 5: Reference clock is valid when read gate is inactive. Read clock is valid when read gate is active and PLO synchronization has been established.

FIGURE 4. ESDI Timing Diagrams

DS8921, DS8922 andDS8923 (Continued)

DM74AS74 Switching Characteristics

over recommended operating free air temperature range (Note 1). All typical values are measured at V_{CC}= 5V, T_A= 25°C.

Parameter	From	To	Conditions	DM74AS74			Units
				Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V	105			MHz
T_{PLH}	Preset	Q or	R_L = 500Ω	3.3		7.5	ns
T_{PHL}	or clear	Q	C_L = 50 pF	3.5		10.5	ns
T_{PLH}	Clock	Q or		3.5		8	ns
T_{PHL}		Q		4.5		9	ns

FIGURE 5. 1 ns Clock Skew

ESDI Enhanced Small Device Interface

The ESDI specification requires that the read and Reference Clock must meet the symmetry shown in *Figure 4*. This necessitates the use of National's DS8921A/22A/23A series of transceivers.

All specifications are in % T, where

$$T = \frac{1}{F}$$

the ESDI specification is assumed to be a 10 Mbits/second standard, T = 100 ns.

Given this, the negative pulse width measured at the drive connector must equal 0.5T ±0.05T (50 ns ±5 ns). The best available RS-422 driver, other than the DS8921A Family, is specified at ±4 ns differential skew. If the clock is from a high speed 74AS74 device, shown in *Figure 5*, it will have a typical skew of 1 ns.

This combination of 4 ns +1 ns uses all of the ESDI specified 5 ns and leaves no margin for noise. Use of the DS8921A, 22A, or 23A, specified at ±2.75 ns max. differential skew would allow up to ±2.25 ns for clock skew and noise. This is as close a guarantee to meeting the ±5 ns spec. of ESDI, as is possible with todays advanced testing systems.

One other consideration is the relationship between Read Clock and Read Data. *Figure 4* shows that the positive edge of Read Clock must be 0.31T (31 ns) after the leading edge of Read Data, and 0.31T (31 ns) before the trailing edge of Read Data.

The Read Clock positive edges will be used to strobe Read Data into the controller after both signals go through their respective cable lines and receivers. Use of the DS8922A/23A assures minimum skew between these two signals. Because both drivers, or both receivers, are on the same piece of silicon an optimum match is achieved.

The above is applicable to an ESDI controller as well as the Drive itself. The controller receives the Reference Clock and uses both positive and negative edges to generate WRITE CLOCK. The negative edge of WRITE CLOCK is used to strobe out WRITE DATA and the positive edge will strobe WRITE DATA into the Drive.

The WRITE CLOCK positive edge has to be centered within WRITE DATA after it is received by the Drive. The transmitted WRITE CLOCK and WRITE DATA must be as closely matched as possible.

National's DS8921A, 22A, and DS8923A devices offer the combination of tightly spec'd parameters and drivers and receivers on one chip to meet various system timing constraints.

Comparing EIA-485 and EIA-422-A Line Drivers and Receivers in Multipoint Applications

National Semiconductor
Application Note 759
John Goldie

Introduction

EIA-485 is a unique interface standard because, of all the EIA Standards, only EIA-485 allows for multiple driver operation. At first glance EIA-485 and EIA-422-A appear to be very similar. Thus, EIA-485 is commonly confused with EIA-422-A. EIA-485 components (drivers and receivers) are backward compatible with EIA-422-A devices and may be interchanged. However, EIA-422-A drivers should not be used in EIA-485 applications. This application note describes the differences between EIA-422-A and EIA-485 devices.

EIA-422-A drivers face three major problems if they are used in multipoint (multiple driver) applications. The first deals with the common mode range of the drivers. The TRI-STATE® common mode range for a EIA-422-A driver is −250 mV to +6V. If a ground potential difference exists between drivers as shown in *Figure 1*, the disabled driver can come out of its high impedance state and clamp the line to one diode drop below ground The second problem deals with contention between active drivers. Faults may occur that cause two drivers to be enabled at the same time. If this happens and the drivers are in opposite states, high currents will flow between devices. The maximum package power dissipation ratings for the devices can be easily exceeded, thermally damaging the devices. The third problem deals with drive current. For bi-directional data flow, the line should be terminated with a resistor at both ends of the cable. Therefore drivers are required to source/sink twice the current required by an EIA-422-A termination (single resistor).

Problem #1—Common Mode Range

A typical bipolar EIA-422-A output structure is shown in *Figure 2*. Associated with the classical totem pole output structure is the parasitic substrate diode formed between the EPI layer and the substrate. This parasitic diode limits the negative common mode range of the driver's output. Given the case when the driver on the left is disabled (high impedance state), the driver on the right is active, and the two drivers are referenced to local grounds a fault can occur. If a ground potential difference exists between the two grounds (V_{CM}), the disabled driver can clamp the line. An example of this occurs when the disabled driver's ground is two volts higher in potential than the active driver's ground. If the output voltage goes below its ground by one diode drop, the parasitic diode becomes forward biased. For this example, assume a V_{OL} of 0.5V, and a V_{CM} of +2V. The active driver's V_{OL} is 0.5V, but with respect to the disabled driver's ground it becomes −1.5V. Clearly the EPI/SUB diode is forward biased and the line is clamped to −0.7V instead of the driven level. Data flow is not guaranteed, if the line is clamped. EIA-485 driver output structures, shown in *Figure 3*, include a Schottky diode in both the source and sink side of the output structure. This diode isolates the EPI/SUB diode from the output pin, and eliminates the possibility of the parasitic diode from turning on and clamping the data line. The common mode range is now −7V to +12V (7V from either rail). The adverse affects of this diode are minimal. The driver's V_{OL} is a Schottky diode drop higher, and V_{OH} is one diode drop lower However, the driver's output will remain in a high impedance state for applied voltages between −7V and +12V.

Problem #2—Contention Between Drivers

If by hardware or software error two drivers are enabled at the same time, a fault occurs. In applications that use multiple drivers, protection from this fault should be considered. This fault can be more damaging to the drivers if the two active drivers are separated by a large ground potential difference. For example, transceiver one (T1) shown in *Figure 3* is referenced to earth ground GND1 (0V). While T2's ground potential (GND2) is 7V higher in magnitude with respect to GND1. If the two drivers are in opposite states, then a 12V difference exists between the drivers (12V = V_{CM} + V_{CC}). A large current will flow, and the maximum package power dissipation rating would be exceeded. EIA-422-A drivers do not have contention protection built in, since they are intended for use in single driver/multiple receiver applications. Power dissipation increases if multiple drivers are involved. EIA-485 line drivers are protected from this contention problem through the use of short circuit current limiting over a wide common mode range. Most EIA-485 drivers have a thermal shutdown feature (although not required by EIA-485). If an active EIA-485 driver output is shorted to any voltage between −7V and +12V, the resulting current will be less than 250 mA. Realizing that drivers can be thermally damaged, ALL National Semiconductor's EIA-485 drivers feature thermal shutdown protection (TS). For example, a worse case fault occurs if the driver is shorted to +12V, and the resulting current is 250 mA. The power dissipated on the device is simply current multiplied by voltage (P=IV): 12V (250 mA) = 3W. Three watts clearly exceeds the rated maximum package power dissipation speci fication for all common packages. However, the thermal shutdown feature senses this fault and disables the drivers output. Hence, the 250 mA current drops to 0 mA; the device cools down and is automatically reset. If the fault is still present, the device will cycle into and out of thermal shutdown until the fault is removed. Some of National's devices feature an open collector pin that reports the occurrence of a thermal shutdown (DS3696 for example). EIA-422-A drivers would commonly incur damage when this fault occurs.

Problem #2—Contention Between Drivers (Continued)

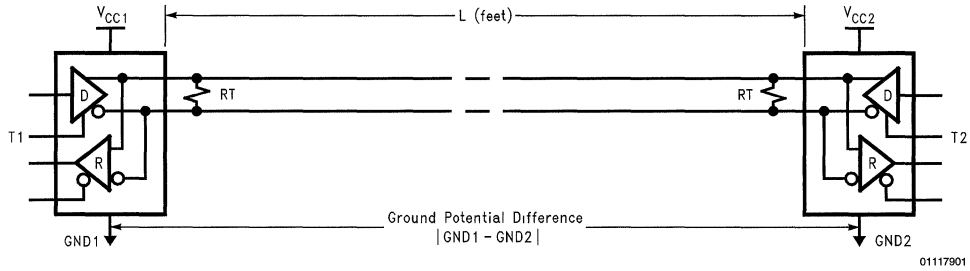


FIGURE 1. Typical Multiple Driver Application

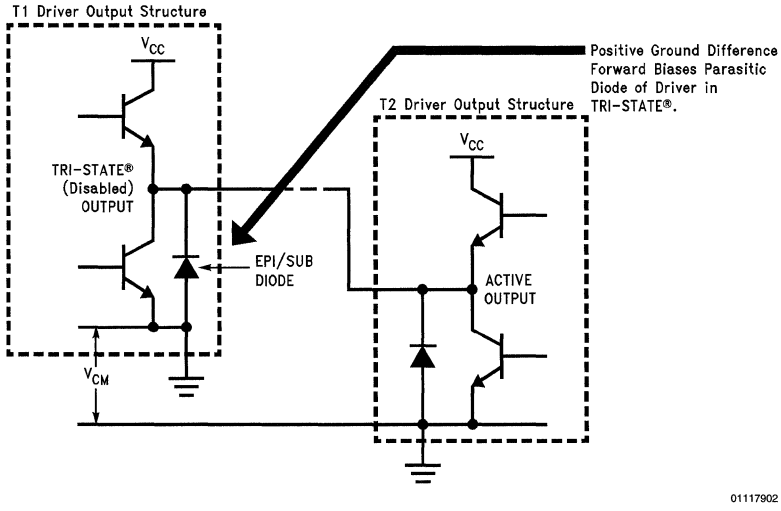


FIGURE 2. EIA-422-A Driver Output Structures Have A Limited Common Mode Range

Problem #2—Contention Between Drivers (Continued)

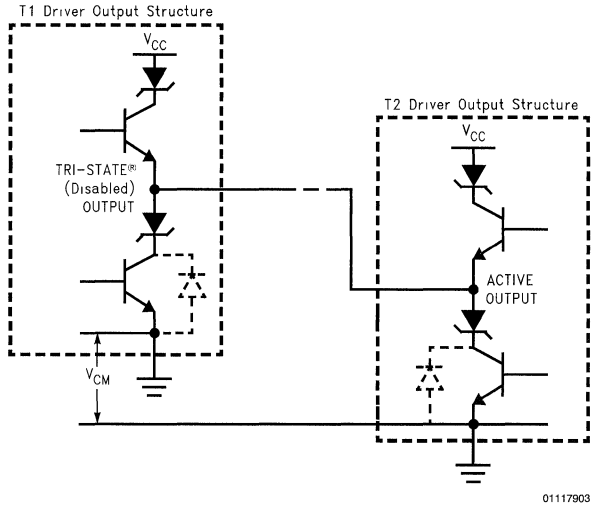


FIGURE 3. EIA-485 Driver Output Supports –7V to +12V Common Mode Range

Problem #3—Drive Current

The third problem deals with the drivers load current capability. EIA-422-A drivers are rated at ±20 mA minimum, while EIA-485 devices have ±55 mA minimum drive capability. Current sourced by the driver either flows through the termination resistor(s), or into receiver input structures. In multiple driver applications, two termination resistors (RT) are required (one at each end of the cable), a driver would see these two resistors in parallel, resulting in a 60Ω load (assuming the termination resistors are 120Ω each). Receiver input structures are also seen in parallel by the driver, and the EIA-422-A receiver input impedance is also too low to be used in applications requiring a high number of receivers. To overcome these problems EIA-485 drivers have roughly three times the drive capability of EIA-422-A drivers. In addition EIA-485 receivers feature a higher input impedance, which is typically three times the EIA-422-A limit of 4 kΩ.

Conclusions

EIA-485 drivers are the best choice for multipoint (multiple driver) applications as shown in *Figure 4*. They can tolerate ground potential differences of up to 7V from either rail. They are contention safe and thermally protected. Finally, the drivers can handle up to 32 transceiver loads compared to EIA-422-A's limit of ten receivers. National offers a wide range of EIA-485 devices: Transceivers, Repeaters, Quad Drivers, Quad Receivers and Quad Transceivers are all offered. Select devices are available in the Industrial and Military temperature ranges. National also offers MIL-883C qualified Quad Drivers, Quad Receivers and Transceiver (see the selection guide located in the front of chapter one of the Interface Databook for a complete listing of all EIA-485 Devices).

References

1. EIA Standard EIA-485 (RS-485), Standard for Electrical Characteristics of Generators and Receivers for use in a Balanced Digital Multipoint Systems, EIA, Washington, D.C.
2. EIA Standard EIA-422-A (EIA RS-422-A), Electrical Characteristics of Balanced Voltage Digital Interface Circuits, EIA, Washington, D.C.
3. Application Note 409, Transceivers and Repeaters Meeting the EIA RS-485 Interface Standard, Interface Databook, National Semiconductor, Santa Clara, CA.

EIA Standards can be obtained for a fee from:

Electronic Industries Association

EIA Engineering Department/Standard Sales Office

2001 Pennsylvania Avenue, N.W.

Washington, D.C. 20006

Tel: (202) 457-4988

References (Continued)

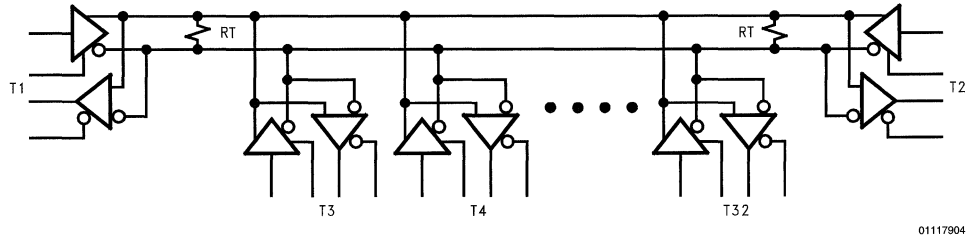


FIGURE 4. Typical EIA-485 Multipoint Application

Calculating Power Dissipation for Differential Line Drivers

National Semiconductor
Application Note 805
Joe Vo

Introduction

In many board and system level designs, it is often necessary to determine the total power dissipated by the individual components of that application. This determination of total device power dissipation is important for two reasons. First, it can be used to select the power supply best suited to satisfy the needs of the application. And second, a power dissipation calculation facilitates the analysis of how the board or system's operating conditions might adversely affect the reliability of, or otherwise damage, the on board components.

The purpose of this application note is to provide end users with a sample power dissipation calculation for typical TIA/EIA-422 and TIA/EIA-485 differential line drivers. Other topics which will be addressed by this application note include worst case power dissipation, and packaging/thermal considerations.

Contributions to Total Device Power Dissipation

Under normal operating conditions, the total device power dissipation is determined primarily by output load current and quiescent current. These current terms are modified by external loading conditions, device switching frequency, power supply voltage and ambient operating temperature. The following discussion of device power dissipation will take all these factors into consideration.

The power dissipated by a device in its quiescent state and that dissipated by the outputs when the device is switching constitute the primary contributions to total device power dissipation. Quiescent power dissipation is defined as the product of power supply voltage (V_{CC}) and power supply current (I_{CC}).

$$PD_{QUIESCENT} = (V_{CC})\,(I_{CC}) \quad (1)$$

The power dissipation by the outputs, takes into account the power dissipated by the output structures of the device when the outputs are driving a load. When the device output is in the LOW state, the output sinks a sufficient amount of load current to develop a V_{OL} with respect to ground. Conversely, when the device output is in the HIGH state, the output sources a load current sufficient to develop a V_{OH} with a respect to ground. The power dissipated, then, by a single channel is:

$$PD_{OUTPUT} = I_{OH}(V_{CC} - V_{OH}) + I_{OL}(V_{OL}) \quad (2)$$

where, I_{OH}= HIGH level output current

I_{OL} = LOW level output current

The general expression to describe the dissipated power for all outputs is:

$$PD_{OUTPUTS} = (\#\text{ of channels})\,[I_{OH}(V_{CC} - V_{OH} + I_{OL}(V_{OL}))] \quad (3)$$

Together, the sum of quiescent power dissipation and power dissipation at the device outputs approximates the total power dissipated by the device.

$$PD_{TOTAL} = PD_{QUIESCENT} + PD_{OUTPUTS} \quad (4)$$

A more comprehensive total device power dissipation calculation, however, might also incorporate the contribution to device power dissipation from the device's switching frequency. Therefore, *Equation (4)* could be changed to look like the following.

$$PD_{TOTAL} = PD_{QUIESCENT} + PD_{OUTPUTS} + C_{OUT}(V_{CC})^2(f) \quad (5)$$

where, C_{OUT} = device output capacitive load

f= device switching frequency

For this application note, the last term of *Equation (5)* was intentionally omitted. These are several reasons for this omission. First, switching frequency does not lend itself well to this general discussion of power dissipation since it varies from application to application. Second, in terms of the quiescent and output power dissipation components, the magnitude of the CV^2f term on total device power dissipation is negligibly small for most line drivers. And third, *Figure 1* demonstrates that switching frequency will not heavily impact quiescent device power dissipation (see *Equation (1)*) since the magnitude of the change in I_{CC} due to switching frequency is small.

Contributions to Total Device Power Dissipation (Continued)

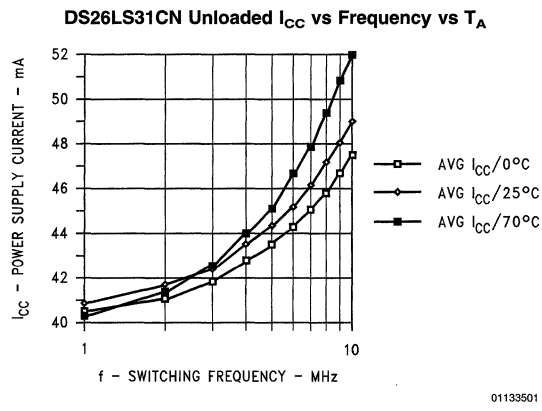


FIGURE 1. Supply Current vs Switching Frequency vs Temperature

Typical Power Dissipation Calculations Using the DS26LS31CN

To better illustrate a total power dissipation calculation in a typical TIA/EIA-422 application, consider the DS26LS31CN (molded DIP package) Quad Differential Line Driver operating under following conditions:

V_{CC} = 5.0V

Ambient Operating Temperature = 25˚C

Switching Frequency = 1 MHz

Duty Cycle = 50%

Measured V_{OH} = 3.2V

Measured V_{OL} = 0.3V

Termination Resistor = 100Ω

Figure 2 indicates that the I_{CC} typically associated with a V_{CC} of 5.0V, at room temperature, is approximately 39 mA. *Figure 1* indicated that a device, operating at room temperature, switching at 1 MHz will generate an I_{CC} of approximately 41 mA. Note in both *Figure 1* and *Figure 2* that the change in I_{CC} with respect to switching frequency and the change in I_{CC} with respect to V_{CC}, respectively, is rather small. Also note that in both figures there is little I_{CC} dependence on temperature.

For this typical calculation, 41 mA will be used for $I_{CCtypical}$ since it is a better representation of actual device operating conditions.

From (1), the static power dissipation is:

$$PD_{QUIESCENT} = (V_{CCtypical}\ (I_{CCtypical})$$
$$= (5.0V)\ (41.0\ mA)$$
$$= 205.0\ mW$$

Given that the measured V_{OH} is 3.2V, one can extract the corresponding I_{OH} from *Figure 3*. The I_{OH} required to develop a V_{OH} of 3.2V is approximately 30 mA.

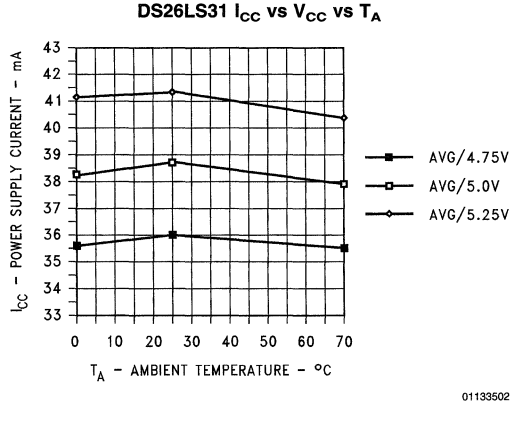


FIGURE 2. Supply Current vs Supply Voltage vs Temperature

Typical Power Dissipation Calculations Using the DS26LS31CN (Continued)

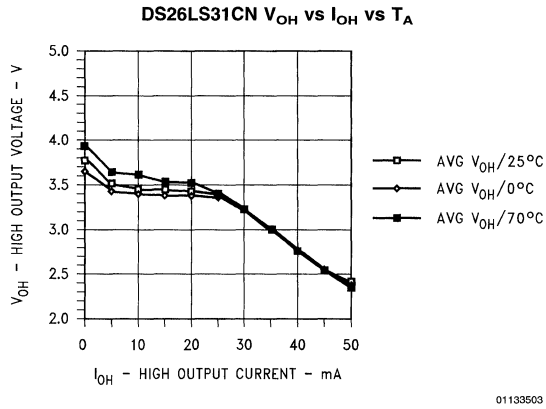


FIGURE 3. High Output Voltage vs High Output Current vs Temperature

From *Figure 4*, one can likewise obtain an I_{OL} of approximately 30 mA given a measured V_{OL} of 0.3V.

The outputs, then, of the DS26LS31CN dissipate power according to the following relationship:

$$PD_{OUTPUTS} = (\#\ \text{of Channels})\ [I_{OH}\ (V_{CC} - V_{OH}) + I_{OL}\ (V_{OL})]$$
$$= (4)\ [30\ \text{mA}\ (5.0V - 3.2V) + 30\ \text{mA}\ (0.3V)]$$
$$= (4)\ [54.0\ \text{mW} + 0.9\ \text{mW}]$$
$$= 252.0\ \text{mW}$$

From the given typical operating conditions, the total power dissipated by the DS26LS31CN is:

$$PD_{TOTAL} = PD_{QUIESCENT} + PD_{OUTPUTS}$$
$$= 205.0\ \text{mW} + 252.0\ \text{mW}$$
$$= 457\ 0\ \text{mW}$$

Worst Case Power Dissipation Calculations

While a typical power dissipation calculation is informative, a board or system level designer will invariably be forced to also perform a worst case calculation. With the exception of several minor changes, the same procedure is followed for both typical and worst case power dissipation calculations.

Starting with static power dissipation, this calculation must now use the maximum values for both power supply voltage (V_{CCmax}) and power supply current (I_{CCmax}). The I_{CCmax} used is normally that specified by the data sheet. However, if the application were to force the device beyond its 10 MHZ operating window, the I_{CCmax} could exceed the data sheet specifications of 60 mA (see *Figure 1*). In either case, the larger current value must be used for I_{CCmax} in the worst case quiescent power calculation.

The next step is to calculate the power dissipation from the device outputs. To do so, place the device under the worst case board or system conditions, and measure the resulting V_{OH} and V_{OL} levels. Given these worst case V_{OH} and V_{OL} values, one can extract the corresponding worst case I_{OH} and I_{OL} values with the help of *Figure 3* and *Figure 4*, respectively. A substitution of these values into *Equation (3)* will then yield the worst case power dissipation due to the device outputs.

An alternative method to calculate the power dissipated by the device outputs requires that a differential output voltage versus output current (V_{OD} vs I_O) curve be generated. Keeping in mind that $V_{OD} \equiv V_{OH} - V_{OL}$, a V_{OD} vs I_O curve can be developed by "subtracting" the V_{OL} vs I_{OL} curve from the V_{OH} vs I_{OH} curve. On the resulting V_{OD} vs I_O curve, draw a load line corresponding to the worst case loading conditions. This will then yield the output differential voltage and output currents being sourced and sunk by the device under a worst case loading condition. A substitution of these quantities into *Equation (6)* will yield the power being dissipated by the device outputs.

$$PD_{DIFFERENTIAL\ OUTPUTS} = (\#\ \text{of channels})\ [I_O(V_{CC} - V_{OD})] \quad (6)$$

As an example, consider the output voltage versus output current curves previously given for the DS26LS31CN (*Figure 3* and *Figure 4*). The V_{OD} vs I_O curve for the DS26LS31CN, as illustrated in *Figure 5*, can be drawn by "subtracting" *Figure 4* from *Figure 3*.

Worst Case Power Dissipation Calculations (Continued)

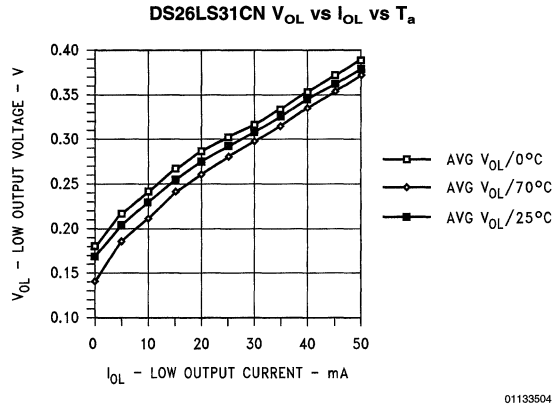


FIGURE 4. Low Output Voltage vs Low Output Current vs Temperature

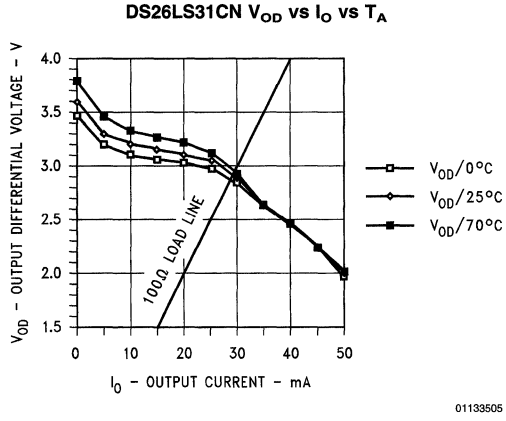


FIGURE 5. Output Differential Voltage vs Output Current vs Temperature

A sample worst case load line of 100Ω superimposed upon *Figure 5* reveals the corresponding worst case operating point for the DS26LS31CN; that is, it reveals the device's output differential voltage and output current given a sample worst case output load. When substituted into *Equation (6)*, these voltage and current quantities will yield the worst case power dissipation at the device outputs.

The sum of the worst case quiescent and output power dissipation components will approximate the total worst case device power dissipation.

Power Calculation for TIA/EIA-485 Differential Line Drivers

Let's first compare a typical TIA/EIA-422 output structure to a typical TIA/EIA-485 output structure. As shown in *Figure 6*, the presence of Schottky diodes in the output stage of an TIA/EIA-485 device clearly differentiates it from a similar TIA/EIA-422 device. The addition of the Schottky diodes to the TIA/EIA-485 output stage enable it to safely operate in multipoint (multiple driver) applications over a –7V to +12V common mode range versus the –250 mV to +6V common mode range of TIA/EIA-422. However, the Schottky diodes in the TIA/EIA-485 outputs have the net effect of raising the value of V_{OL} by one diode drop and decreasing the value of V_{OH} by the same amount. This change in output voltage levels will, in turn, affect the amount of power being dissipated in the output stage.

Despite the fact that the output structure of an TIA/EIA-422 line driver differs from that of the TIA/EIA-485 line driver, the procedure outlined earlier to calculate power dissipation is applicable for both TIA/EIA-422 devices and TIA/EIA-485 devices. Quiescent and output power dissipation calculations for an TIA/EIA-485 line driver will again employ *Equations (1), (3)* respectively.

As with the sample power calculation for the TIA/EIA-422 device, the sum of the quiescent and output power components will yield the total approximated power dissipated by the TIA/EIA-485 device.

Power Calculation for TIA/EIA-485 Differential Line Drivers (Continued)

As an example, consider the worst case power dissipation of the DS96F172CJ (ceramic DIP package). Other than the fact that the DS96F172CJ is an TIA/EIA-485 device, it is pin for pin compatible with the DS26LS31CN. As outlined earlier, the first step is to calculate the quiescent power dissipation. From *Equation (1)*, the worst case quiescent power dissipation is:

$$PD_{QUIESCENTmax} = (V_{CCmax})\,(I_{CCmax})$$
$$= (5.25V)\,(50\ mA)$$
$$= 262.5\ mW$$

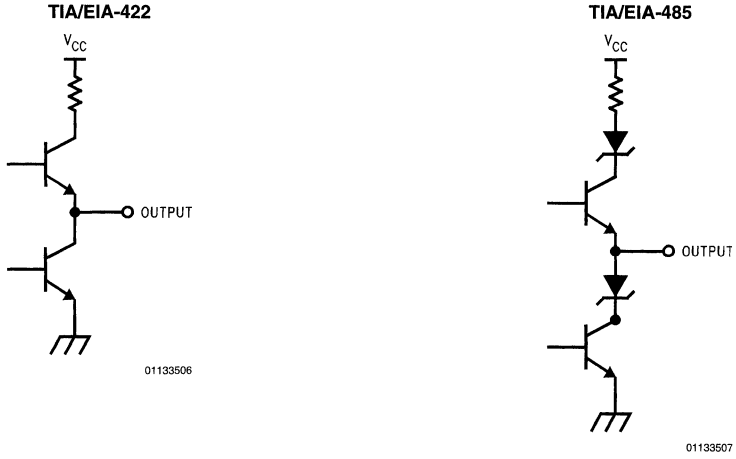


FIGURE 6. TIA/EIA-422 and TIA/EIA-485 Output Structures

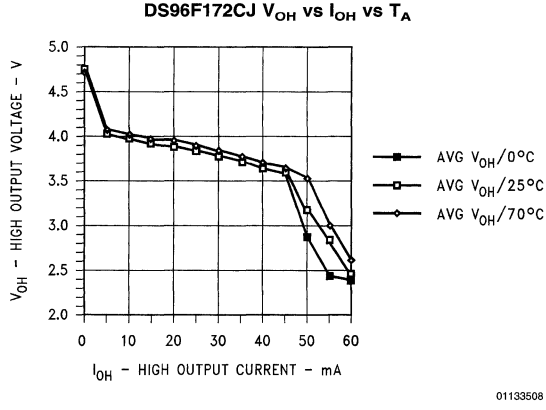


FIGURE 7. High Output Voltage vs High Output Current vs Temperature

Power Calculation for TIA/EIA-485 Differential Line Drivers (Continued)

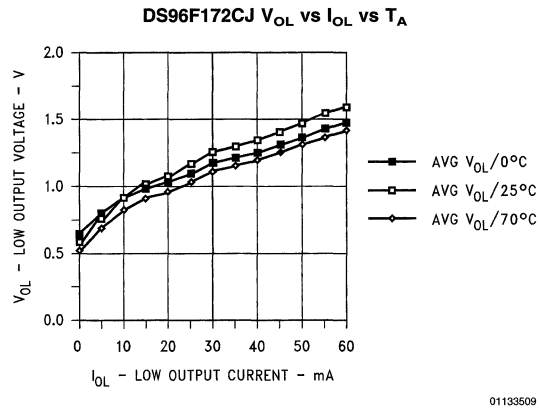


FIGURE 8. Low Output Voltage vs Low Output Current vs Temperature

The next step is to calculate the power dissipated at the device outputs under a worst case load condition. Again, there are two ways to do this. First, one can measure the worst case output voltage levels and reference them with *Figure 7* and *Figure 8* to extract the corresponding worst case output currents.

A substitution of these resulting quantities into *Equation (3)* will yield the power dissipated at the device outputs given a worst case load. The second method to calculate output power dissipation involves drawing a worst case load line on the differential output voltage versus output current curve. In the case of the DS96F172CJ, the worst case load line is assumed to be 60Ω. This assumption was made because in a typical TIA/EIA-485 application, both ends of the transmission line are terminated with 120Ω and so the TIA/EIA-485 driver is effectively loaded with 60Ω. In *Figure 9* a 60Ω load line has been superimposed upon the differential output versus output current curve and consequently, worst case values of output current and differential output voltage (under the given load) have been obtained.

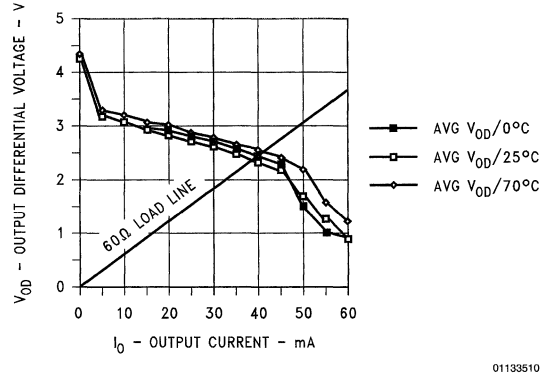


FIGURE 9. Output Differential Voltage vs Output Current vs Temperature

At room temperature, the worst case power dissipation at the device outputs is (from *Equation (6)*):

$PD_{DIFFERENTIAL\ OUTPUTS}$

= (# of channels) [I_O (V_{CC} – V_{OD})]

= (4) [39 mA (5.25V – 2.4V)]

= 444.6 mW

The only remaining task is to sum together the quiescent and output power dissipation terms to obtain a total worst case power dissipation. From (4), the DS96F172CJ operating at room temperature, under a worst case load of 60Ω, will dissipate:

Power Calculation for TIA/EIA-485 Differential Line Drivers (Continued)

$$PD_{TOTAL} = PD_{QUIESCENT} + PD_{OUTPUTS}$$
$$= 262.5 \text{ mW} + 444.6 \text{ mW}$$
$$= 707.1 \text{ mW}$$

Packaging and Thermal Considerations

Having calculated the total power dissipated by the device, the next logical step is to ascertain that the power dissipated does not thermally damage the device. To do so, the following equation is used:

$$T_J = [PD_{TOTAL}(\theta_{JA})] + T_A \quad (7)$$

where, θ_{JA} = Thermal Resistance from Junction to Ambient (°C/W)

PD_{TOTAL} = Total Power Dissipated by Device (W)

T_J = Junction Temperature (°C)

T_A = Ambient Temperature (°C)

The only variable which remains unknown is θ_{JA}. θ_{JA} information for the available package types of most devices can be found in the respective device's data sheet. Keep in mind that the data sheet often refers to θ_{JA} in terms of derate factors. Determining θ_{JA} involves taking the inverse of the derate factor.

$$\theta_{JA} = 1/\text{Derate Factor} \quad (8)$$

For example, all the information is now available for a sample calculation of the DS26LS31CN's junction temperature using the operating conditions specified earlier. The data sheet of the DS26LS31CN specifies a derate factor, for the plastic DIP package, of 11.9 mW/°C. From (8), the θ_{JA} is:

$$\theta_{JA} = 1/\text{Derate Factor}$$
$$= 1/(0.0119 \text{ W/°C})$$
$$= 84.0 \text{ °C/W}$$

The thermal resistance from junction to ambient for the DS26LS31CN is now known. Also known are the ambient operating temperature and the total power dissipated (obtained earlier). From (7), the junction temperature is:

$$T_J = [(PD_{TOTAL})\ (\theta_{JA})] + T_A$$
$$= [(0.457\text{W})\ (84.0\text{°C/W})] + 25\text{°C}$$
$$= 63.4\text{°C}$$

The maximum allowable junction temperature for plastic DIP packages is 150°C. The junction temperature of the DS26LS31CN operating under the conditions specified earlier, by the typical power dissipation calculation, is well within the allowed maximum. Applications where the maximum allowable junction temperature is exceeded should be avoided since this condition may thermally damage the device and package.

Looking at this thermal analysis from a slightly different perspective, *Equation (7)* can be rewritten as:

$$PD_{PACKAGEmax} = (T_{Jmax} - T_A)/\theta_{JA} \quad (9)$$

Packaging and Thermal Considerations (Continued)

By substituting 150˚C for the maximum allowable junction temperature, the maximum allowable package power dissipation at 25˚C can be calculated using the θ_{JA} for the DS26LS31CN plastic DIP (N) package.

$$PD_{PACKAGEmax\ @\ 25^\circ C} = (T_{Jmax} - T_A)/\theta_{JA}$$
$$= (150^\circ C - 25^\circ C)/84.0^\circ C/W$$
$$= 1.48W$$

To calculate the maximum allowable package power dissipation at 70˚C, the 1.48W maximum at 25˚C must be derated using the following procedure:

$$PD_{PACKAGEmax\ @\ 70^\circ C} =$$
$$PD_{PACKAGEmax\ @\ 25^\circ C} - (\text{Derate})\ (\Delta T_A)$$
$$= 1.48W - (0.0119W/^\circ C)$$
$$(45^\circ C) = 0.94W \qquad (10)$$

This sample calculation illustrates that as ambient temperature increases, the DS26LS31CN is able to dissipate less power before the maximum allowable junction temperature specification is violated. Keep in mind that this thermal analysis also applies to TIA/EIA-485 devices such as the DS96F172CJ.

It should be noted that this general thermal analysis is applicable to all other packages and device types assuming that the maximum power dissipation and θ_{JA} are known.

Summary

A method for calculating the total power dissipated by an TIA/EIA-422 driver was presented. This method is also applicable to similar devices conforming to the TIA/EIA-485 standard. Samples calculations for the DS26LS31CN and the DS96F172CJ were presented. Worst case considerations were also discussed. And finally, the relationship between power dissipation and thermal/packaging limitations was introduced.

Special Notes

Figure 1:	Ten samples from three data codes.
Figure 2:	Ten samples from three data codes. Outputs unloaded and V_{CC} = 5.0V.
Figure 3, *Figure 4*, *Figure 5*:	Ten samples from three date codes. V_{CC} = 5.0V
Figure 7, *Figure 8*, *Figure 9*:	Ten samples from two date codes. V_{CC} = 5.0V

The graphical data referenced in this application note are not intended to guarantee performance as they only represent typical values.

References

HC-CMOS Power Dissipation, K. Karakotsios, National Semiconductor, 1988 CMOS Logic Data Book, Application Note AN-303.

Understanding Integrated Circuit Package Power Capabilities, C. Carinalli and J. Huljev, National Semiconductor, 1990 Interface Data Book, Application Note AN-336.

Data Transmission Lines and Their Characteristics

National Semiconductor
Application Note 806
Kenneth M True

Overview

This application note discusses the general characteristics of transmission lines and their derivations. Here, using a transmission line model, the important parameters of characteristics impedance and propagation delay are developed in terms of their physical and electrical parameters. This application note is a revised reprint of section two of the Fairchild Line Driver and Receiver Handbook This application note, the first of a three part series (see AN-807 and AN-808), covers the following topics.

- Transmission Line Model
- Input Impedance of a Transmission Line
- Phase Shift and Propagation Velocity for the Transmission Line
- Summary—Characteristics Impedance and Propagation Delay

Introduction

A data transmission line is composed of two or more conductors transmitting electrical signals from one location to another. A parallel transmission line is shown in *Figure 1*. To show how the signals (voltages and currents) on the line relate to as yet undefined parameters, a transmission line model is needed.

Transmission Line Model

Because the wires A and B could not be ideal conductors, they therefore must have some finite resistance. This resistance/conductivity is determined by length and cross-sectional area. Any line model, then, should possess some series resistance representing the finite conductivity of the wires. It is convenient to establish this resistance as a per-unit-length parameter.

Similarly, the insulating medium separating the two conductors could not be a perfect insulator because some small leakage current is always present. These currents and dielectric losses can be represented as a shunt conductance per unit length of line To facilitate development of later equations, conductance is the chosen term instead of resistance.

If the voltage between conductors A and B *is not variable* with time, any voltage present indicates a static electric field between the conductors. From electrostatic theory it is known that the voltage V produced by a static electric field E is given by

$$V = \int E \bullet dl \tag{1}$$

This static electric field between the wires can only exist if there are free charges of equal and opposite polarity on both wires as described by Coulomb's law

$$E = \frac{q}{4\pi\epsilon r^2} \tag{2}$$

where E is the electric field in volts per meter, q is the charge in Coulombs, ϵ is the dielectric constant, and r is the distance in meters. These free charges, accompanied by a voltage, represent a capacitance (C = q/V), so the line model must include a shunt capacitive component. Since total capacitance is dependent upon line length, it should be expressed in a capacitance per-unit-length value.

It is known that a current flow in the conductors induces a magnetic field or flux This is determined by either Ampere's law

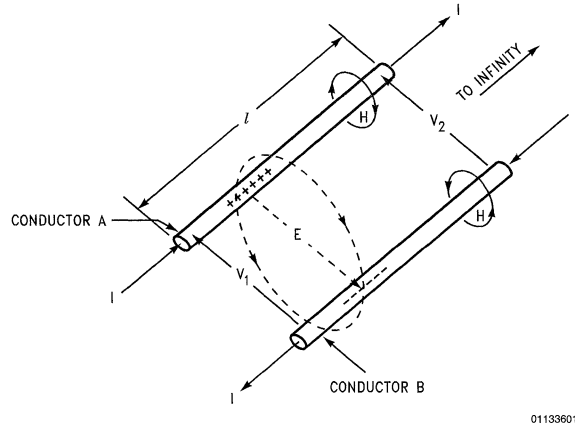
$$\int H \bullet dl = I \tag{3}$$

or the Biot-Savart law

$$dB = \frac{\mu I dl \times r}{4\pi r^3} \tag{4}$$

where r = radius vector (meters)
ℓ = length vector (meters)
I = current (amps)
B = magnetic flux density (Webers per meter)
H = magnetic field (amps per meter)
μ = permeability

Transmission Line Model (Continued)



I = CURRENT FLOW
ℓ = LINE LENGTH
E = ELECTRIC FIELD
H = MAGNETIC FIELD

FIGURE 1. Infinite Length Parallel Wire Transmission Line

If the magnetic flux (ϕ) linking the two wires *is variable* with time, then according to Faraday's law

$$V = \frac{d\phi}{dt} \tag{5}$$

A small line section can exhibit a voltage drop—in addition to a resistive drop—due to the changing magnetic flux (ϕ) within the section loop. This voltage drop is the result of an inductance given as

$$V = L\frac{di}{dt} \tag{6}$$

Therefore, the line model should include a series inductance per-unit-length term. In summary, it is determined that the model of a transmission line section can be represented by two series terms of resistance and inductance and two shunt terms of capacitance and conductance.

From a circuit analysis point of view, the terms can be considered in any order, since an *equivalent* circuit is being generated. *Figure 2* shows three possible arrangements of circuit elements.

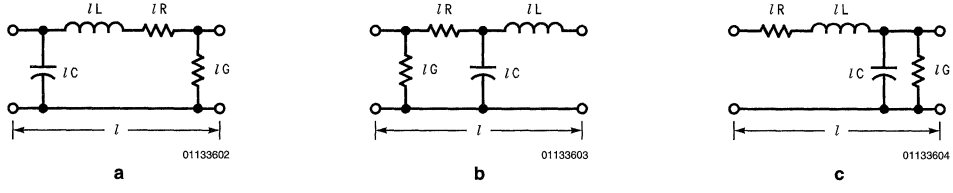


FIGURE 2. Circuit Elements

For consistency, the circuit shown in *Figure 2* will be used throughout the remainder of this application note. *Figure 3* shows how a transmission line model is constructed by series connecting the short sections into a ladder network.

Before examining the pertinent properties of the model, some comments are necessary on applicability and limitations. A *real* transmission line does not consist of an infinite number of small lumped sections—rather, it is a distributed network. For the lumped model to accurately represent the transmission line (see *Figure 3*), the section length must be quite small in comparison with the shortest wavelengths (highest frequencies) to be used in analysis of the model. Within these limits, as differentials are taken, the section length will approach zero and the model should exhibit the same (or at least very similar) characteristics as the actual distributed parameter transmission line. The model in *Figure*

Transmission Line Model (Continued)

3 does not include second order terms such as the increase in resistance due to skin effect or loss terms resulting from non-linear dielectrics. These terms and effects are discussed in the references rather than in this application note, since they tend to obscure the basic principles under consideration. For the present, assume that the signals applied to the line have their minimum wavelengths a great deal longer than the section length of the model and ignore the second order terms.

Input Impedance of a Transmission Line

The purpose of this section is to determine the input impedance of a transmission line; i e., what amount of input current I_{IN} is needed to produce a given voltage V_{IN} across the line as a function of the LRCG parameters in the transmission line, (see *Figure 4*).

Combining the series terms IR and IL together simplifies calculation of the series impedance (Z_s) as follows

$$Z_s = \ell(R + j\omega L) \tag{7}$$

Likewise, combining IC and IG produces a parallel impedance Z_p represented by

$$Z_p = \frac{1}{Y_p} = \frac{1}{\ell(G + j\omega C)} \tag{8}$$

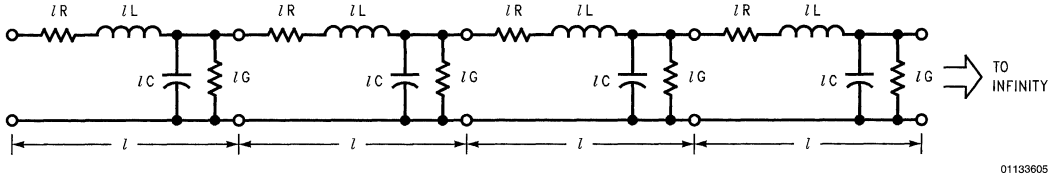


FIGURE 3. A Transmission Line Model Composed of Short, Series Connected Sections

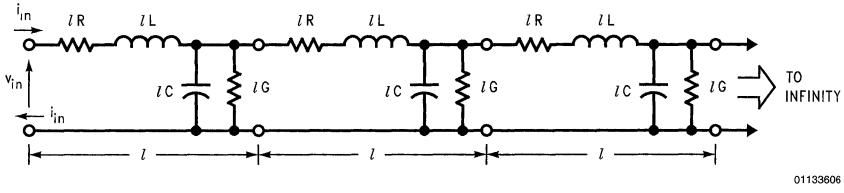


FIGURE 4. Series Connected Sections to Approximate a Distributed Transmission Line

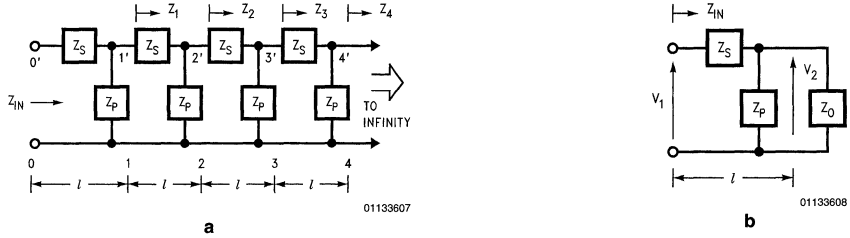


FIGURE 5. Cascaded Network to Model Transmission Line

Since it is assumed that the line model in *Figure 5* is infinite in length, the impedance looking into any cross section should be equal, that is $Z_1 = Z_2 = Z_3$, etc. So *Figure 5* can be simplified to the network in *Figure 5* where Z_0 is the characteristic impedance of the line and Z_{in} must equal this impedance ($Z_{in} = Z_0$). From *Figure 5*,

$$Z_{in} = Z_s + \frac{Z_0 Z_p}{Z_0 + Z_p} = Z_0 \tag{9}$$

Input Impedance of a Transmission Line (Continued)

Multiplying through both sides by $(Z_0 + Z_p)$ and collecting terms yields

$$Z_0 2 - Z_s Z_0 - Z_s Z_p = 0 \quad (10)$$

which may be solved by using the quadratic formula to give

$$Z_0 = \frac{Z_s \pm \sqrt{Z_s^2 + 4Z_s Z_p}}{2} \quad (11)$$

Substituting in the definition of Z_s and Z_p from *Equation (7)* and *Equation (8)*, *Equation (11)* now appears as

$$Z_0 = \frac{l(R + j\omega L)}{2} \pm \frac{1}{2}\sqrt{l^2 (R + j\omega L)^2 + 4\frac{R + j\omega L}{G + j\omega C}} \quad (12)$$

Now, as the section length is reduced, all the parameters (IR, IL, IG, and IC) decrease in the same proportion. This is because the per-unit-length line parameters R, L, G, and C are constants for a given line. By sufficiently reducing ℓ, the terms in *Equation (12)* which contain I as multipliers will become negligible when compared to the last term

$$\frac{R + j\omega L}{G + j\omega C}$$

which remains constant during the reduction process. Thus *Equation (12)* can be rewritten as

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} = \sqrt{Z_s Z_p} \quad (13)$$

particularly when the section length ℓ is taken to be very small. Similarly, if a high enough frequency is assumed,

$$\frac{\omega}{2\pi} > 100\ \text{kHz}$$

such that the ωL and ωC terms are much larger respectively than the R and G terms, $Z_s = j\omega \ell L$ and $Z_p = 1/j\omega \ell C$ can be used to arrive at a lossless line value of

$$Z_0 = \sqrt{\frac{L}{C}} \quad (14)$$

In the lower frequency range,

$$\frac{\omega}{2\pi} \cong 1\ \text{kHz}$$

the R and G terms dominate the impedance giving

$$Z_0 = \sqrt{\frac{R}{G}} \quad (15)$$

A typical twisted pair would show an impedance versus applied frequency curve similar to that shown in *Figure 6*. The Z_0 becomes constant above 100 kHz, since this is the region where the ωL and ωC terms dominate and *Equation (13)* reduces to *Equation (14)*. This region above 100 kHz is of primary interest, since the frequency spectrum of the fast rise/fall time pulses sent over the transmission line have a fundamental frequency in the 1-to-50 MHz area with harmonics extending upward in frequency. The expressions for Z_0 in *Equation (13)*, *Equation (14)* and *Equation (15)* do not contain any reference to line length, so using *Equation (14)* as the normal characteristic impedance expression, allows the line to be replaced with a resistor of $R_0 = Z_0\ \Omega$ neglecting any small reactance. This is true when calculating the initial voltage step produced on the line in response to an input current step, or an initial current step in response to an input voltage step.

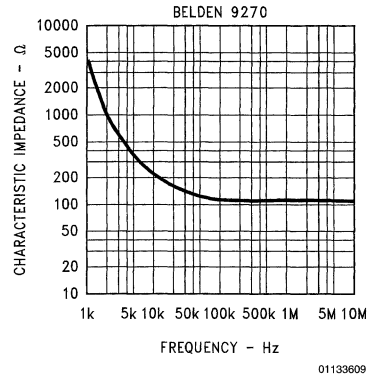


FIGURE 6. Characteristics Impedance versus Frequency

Figure 7 shows a 2V input step into a 96Ω transmission line (top trace) and the input current required for line lengths of 150, 300, 450, 1050, 2100, and 3750 feet, respectively (second set of traces). The lower traces show the output voltage waveform for the various line lengths. As can be seen, maximum input current is the same for all the different line lengths, and depends only upon the input voltage and the characteristic resistance of the line. Since $R_0 = 96\Omega$ and $V_{IN} = 2V$, then $I_{IN} = V_{IN}/R_0 \cong 20$ mA as shown by *Figure 7*.

A popular method for estimating the input current into a line in response to an input voltage is the formula

$$C(dv/dt) = i$$

where C is the total capacitance of the line (C = C per foot x length of line) and dv/dt is the slew rate of the input signal. If the 3750-foot line, with a characteristic capacitance per unit length of 16 pF/ft is used, the formula $C_{total} = (C \times \ell)$ would yield a total lumped capacitance of 0.06 µF. Using this C(dv/dt) = *i* formula with (dv/dt = 2V/10 ns) as in the scope photo would yield

$$I = \frac{2V}{10\ \text{ns}} \times 0.06\ \mu F = 12A$$

This is clearly not the case! Actually, since the line impedance is approximately 100Ω, 20 mA are required to produce 2V across the line. If a signal with a rise time long enough to encompass the time delay of the line is used ($t_r \gg \tau$), then the C(dv/dt) = *i* formula will yield a resonable estimate of the peak input current required. In the example, if the dv/dt is 2V/20 µs (t_r = 20 µs > τ = 6 µs), then *i* = 2V/20 µs x 0.06 µF = 6 mA, which is verified by *Figure 8*.

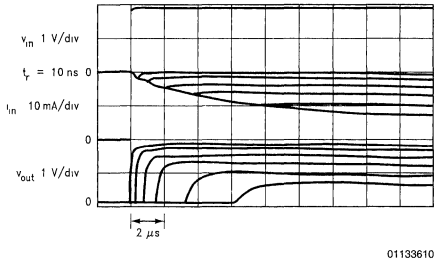
Figure 8 shows that C(dv/dt) = *i* only when the rise time is greater than the time delay of the line ($t_r \gg \tau$). The maximum input current requirement will be with a fast rise time step,

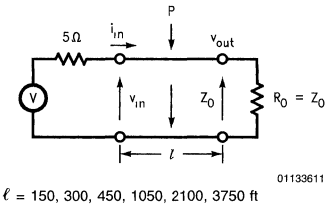
Input Impedance of a Transmission Line (Continued)

but the line is essentially resistive, so $V_{IN}/I_{IN} = R_0 = Z_0$ will give the actual drive current needed These effects will be discussed later in Application Note 807.

Phase Shift and Propagation Velocity for the Transmission Line

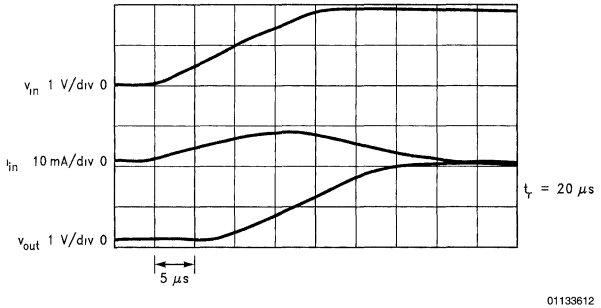
There will probably be some phase shift and loss of signal v_2 with respect to v_1 because of the reactive and resistive parts of Z_s and Z_p in the model (*Figure 5*). Each small section of the line (ℓ) will contribute to the total phase shift and amplitude reduction if a number of sections are cascaded as in *Figure 5*. So, it is important to determine the phase shift and signal amplitude loss contributed by each section.

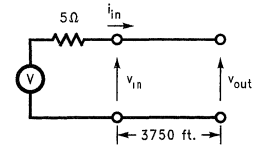




ℓ = 150, 300, 450, 1050, 2100, 3750 ft
24 AWG TWISTED PAIR $R_0 \equiv 96\Omega$

FIGURE 7. Input Current Into a 96Ω Transmission Line for a 2V Input Step for Various LIne Lengths





$R_0 = 96\Omega$, δ = 1 6 ns/ft

FIGURE 8. Input Current Into Line with Controlled Rise Time $t_r > 2\pi$

Phase Shift and Propagation Velocity for the Transmission Line

(Continued)

Using *Figure 5*, v_2 can be expressed as

$$v_2 = v_1 \frac{Z_p Z_0}{Z_p + Z_0} \quad \frac{1}{Z_s + Z_p Z_0/(Z_p + Z_0)} \tag{16}$$

or

$$\frac{v_1}{v_2} = \frac{Z_s(Z_p + Z_0) + Z_p Z_0}{Z_p Z_0} \tag{17}$$

and further simplification yields

$$\frac{v_1}{v_2} = 1 + Z_s \left[\frac{1}{Z_0} + \frac{1}{Z_p} \right] \tag{18}$$

Remember that a per-unit-length constant, normally called γ is needed. This shows the reduction in amplitude and the change in the phase per unit length of the sections.

$$\gamma_\ell = \alpha_\ell = j\beta_\ell \tag{19}$$

Since

$$v_2 = v_1 \, ^{-\gamma\ell} = v_1 \, ^{-\alpha\ell} + v_\ell \, ^{-j\beta\ell} \tag{20}$$

where $v_1^{\alpha\ell}$ is a signal attenuation and $v_1 - j\beta_\ell$ is the change in phase from v_1 to v_2,

$$ln \left[\frac{v_1}{v_2} \right] = ln \, (\alpha_l + j\beta_l) = \alpha_l + j\beta_l = \gamma_l \tag{21}$$

Thus, taking the natural log of both sides of *Equation (18)*

$$ln \left[\frac{v_1}{v_2} \right] = ln \left[1 + Z_s \left(\frac{1}{Z_0} + \frac{1}{Z_p} \right) \right] \tag{22}$$

Substituting *Equation (13)* for Z_0 and $Y_p$for ℓ/Z_p

$$\gamma_l = ln \left[1 + Z_s \left(\sqrt{\frac{Y_p}{Z_s}} + Y_p \right) \right] \tag{23}$$

Now when allowing the section length ℓ to become small,

$$Y_p = \ell(G + j\omega C)$$

will be very small compared to the constant

$$\sqrt{Y_p/Z_s} = 1/Z_0,$$

since the expression for Z_0 does not contain a reference to the section length ℓ. So *Equation (23)* can be rewritten as

$$\gamma_l = ln \left(1 + Z_s \sqrt{\frac{Y_p}{Z_s}} \right) = ln \, (1 + \sqrt{Y_p Z_s}) \tag{24}$$

By using the series expansion for the natural log:

$$ln \, (1 + \zeta) = \zeta - \frac{\zeta^2}{2} + \frac{\zeta^3}{3} \ldots \text{ etc.} \tag{25}$$

and keeping in mind the

$$\sqrt{Z_s Y_p}$$

value will be much less than one because the section length is allowed to become very small, the higher order expansion terms can be neglected, thereby reducing *Equation (24)* to

$$\gamma_l = \sqrt{Z_s Y_p} = l \sqrt{(R + j\omega L)(G + j\omega C)} \tag{26}$$

If *Equation (26)* is divided by the section length,

$$\gamma = \frac{\gamma_l}{l} = \sqrt{(R + j\omega L)(G + j\omega C}} \tag{27}$$

the propagation constant per unit length is obtained. If the resistive components R and G are further neglected by assuming the line is reasonably short, *Equation (26)* can be reduced to read

$$\gamma_l = j\beta_l = j\omega l \sqrt{LC} \tag{28}$$

Equation (28) shows that the lossless transmission line has one very important property: signals introduced on the line have a constant phase shift per unit length with no change in amplitude. This progressive phase shift along the line actually represents a wave traveling down the line with a velocity equal to the inverse of the phase shift per section. This velocity is

$$v = \frac{\omega}{\beta} = \frac{1}{\sqrt{LC}} \tag{29}$$

for lossless lines. Because the LRCG parameters of the line are independent of frequency except for those upper frequency constraints previously discussed, the signal velocity given by *Equation (29)* is also independent of signal frequency. In the practical world with long lines, there is in fact a frequency dependence of the signal velocity. This causes sharp edged pulses to become rounded and distorted. More on these long line effects will be discussed in Application Note 807.

Summary—Characteristic Impedance and Propagation Delay

Every transmission line has a characteristic impedance Z_0, and both voltage and current at any point on the line are related by the formula

$$Z_0 = \frac{v}{i}$$

In terms of the per-unit-length parameters LRCG,

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

Since $R \ll j\omega L$ and $G \ll j\omega C$ for most lines at frequencies above 100 kHz, the characteristic impedance is best approximated by the lossless line expression

Summary—Characteristic Impedance and Propagation Delay

(Continued)

$$Z_0 \cong \sqrt{\frac{L}{C}}$$

The propagation constant, γ, shows that signals exhibit an amplitude loss and phase shift with the latter actually a velocity of propagation of the signal down the line. For lossless lines, where the attenuation is zero, the phase shift per unit length is

$$\beta = \frac{\beta l}{l} = \omega \sqrt{LC}$$

This really represents a signal traveling down the line with a velocity

$$v = \frac{\omega}{\beta} = \frac{1}{\sqrt{LC}}$$

This velocity is independent of the applied frequency.

The larger the LC product of the line, the slower the signal will propagate down the line. A time delay per unit length can also be defined as the inverse of v

$$\delta = \frac{1}{v} = \sqrt{LC} \tag{30}$$

and a total propagation delay for a line of length ℓ as

$$\tau = l\delta = l\sqrt{LC} \tag{31}$$

For a more detailed discussion of characteristic impedances and propagation constants, the reader is referred to the references below.

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Hamsher, D.H. (editor); *Communications System Engineering Handbook;* Chapter 11, McGraw-Hill, New York, 1967.

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Matrick, R.F.; *Transmission Lines for Digital and Communications Networks;* McGraw-Hill, New York, 1969.

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Reflections: Computations and Waveforms

National Semiconductor
Application Note 807
Kenneth M. True

Overview

In this application note, the logical progression from the ideal transmission line to the real world of the long transmission line with its attendant losses and problems is made; specifically, the methods to determine the practicality of a certain length of line at a given data rate is discussed. Transmission line effects on various data formats are examined as well as the effects of several types of sources (drivers) on signal quality. A practical means is given to measure signal quality for a given transmission line using readily available test equipment This, in turn, leads to a chart that provides the designer a way to predict the feasibility of a proposed data-transmission circuit when twisted-pair cable is used. This application note is a revised reprint of section three of the Fairchild Line Driver and Receiver Handbook. This application note, the second of a three-part series (see AN-806 and AN-808), covers the following topics:

- The Initial Wave
- Cut Lines and a Matched Load
- Kirchoff's Laws and Line-Load Boundary Conditions
- Fundamental Principles
- Tabular Method for Reflections—The Lattice Diagram
- Limitations of the Lattice Diagram Method
- Reflection Effects for Voltage-Source Drivers
- Reflection Effects for Matched-Source Drivers
- Reflection Effects for Current-Source Drivers
- Summary—Which are the Advantageous Combinations?
- Effect of Source Rise Time on Waveforms

Introduction

In AN-806 it was determined that transmission lines have two important properties: one, a characteristic impedance relating instantaneous voltages and currents of waves traveling along the line and, two, a wave propagation velocity or time delay per unit length. In this chapter, both Z_0 and δ are used to compute the line voltages and currents at any point along the line and at any time after the line signal is applied. Also, concepts of reflections and reflection coefficients are explored along with calculating methods for voltages and currents.

The Initial Wave

Application Note AN-806 also showed that for most practical purposes, where fast rise and fall time signals are concerned, the characteristic impedance of the line actually behaves as a pure resistance ($R_0 = \sqrt{L/C}$) .

Figure 1 shows a generator comprised of a voltage source (magnitude V), a source resistance of R_S ohms, and a switch closing at time t = 0 connected to a lossless, infinite length transmission line having a characteristic resistance, R_0. Because the relationship of V_{IN} to I_{IN} is known as $V_{IN} = R_0 I_{IN}$, the lossless transmission line can be replaced with a resistor as shown in *Figure 2*. The loop equation is.

$$I_{IN} (R_S + R_0) = V \quad (1)$$

Substituting V_{IN}/R_0 for $I_{IN}$and collecting terms shows

$$V_{IN} = V\left(\frac{R_0}{R_0 + R_S}\right) \quad (2)$$

This shows that both source and characteristic resistances act as voltage dividers for the source voltage V. *Figure 3* shows voltage and current steps for the various source resistances. Source resistances of less than R_0 produce initial voltage steps on the line which are greater than half the compliance of the source voltage, V. A matched source ($R_S = R_0$) produces voltage steps exactly half of V and source resistances greater than R_0 produce an initial voltage step less than one half V in magnitude. Generators can be classified into three categories:

- Voltage source types where $R_S < R_0$
- Matched source types where $R_S = R_0$
- Current source types where $R_S > R_0$

Waveforms of these types will be discussed more fully in AN-808 on long line effects. Suffice to say that initial voltage wave amplitude depends greatly on source resistance. Voltage source type drivers produce higher amplitude initial voltage waves in the line than either matched source or current source type drivers.

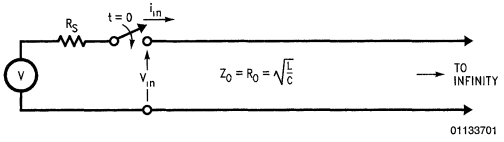


FIGURE 1. Generator Driving an Infinite Transmission Line

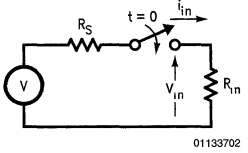


FIGURE 2. Thevenin Equivalent for Initial Wave

The Initial Wave (Continued)

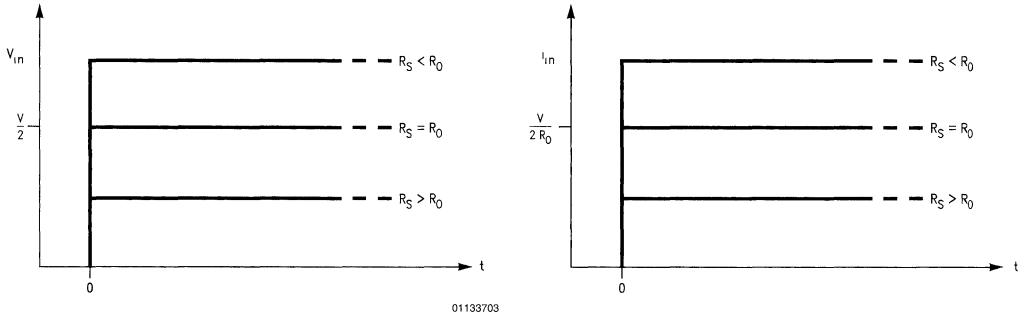


FIGURE 3. Voltage/Current Steps for Three Source Resistances

Cut Lines and a Matched Load

In examining an infinite, lossless line (*Figure 4*), it is already known that the ratio of line voltage to current is equal to the characteristic resistance of that line. The line is lossless, and the same voltages and currents should appear at point x down the line after a time delay of $x\delta$. If the line at point x is cut, and a resistor of value R_0 is inserted, there would not be a difference between the cut, terminated finite line and the infinite line. The v_x and I_x waves see the same impedance (R_0) they were launched into at time t = 0, and indeed, the waves are absorbed into R_L (= R_0) after experiencing a time delay of $\tau = x\delta$ So, from an external viewpoint, an infinite-length lossless line behaves as a finite-length lossless line terminated in its characteristic resistance.

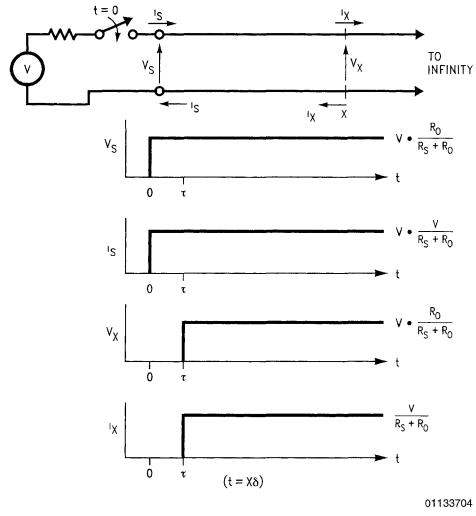


FIGURE 4. Voltages and Current on an Infinite Length Line

Kirchoff's Laws and Line-Load Boundary Conditions

The principle of energy conservation, widely known and accepted in the sciences, applies as well to transmission line theory; therefore, energy (as power) must be conserved at boundaries between line and load. This is expressed in an English language equation as follows.

$$\left[\begin{array}{c}\text{Power available at}\\ \text{the line end}\end{array}\right] = \left[\begin{array}{c}\text{Power absorbed}\\ \text{by the load}\end{array}\right] + \left[\begin{array}{c}\text{Power not absorbed}\\ \text{by the load}\end{array}\right]$$

Figure 5 shows power available at the line end is derived by the following formula. (This is assuming in-phase current and voltage.)

$$P_x = i_x \bullet v_x = \frac{v_x^2}{R_0} \tag{3}$$

The power *absorbed* by the load will be

$$P_L = v_L \bullet i_L = \frac{v_L^2}{R_L} \tag{4}$$

while power *not absorbed* by the load is represented by

$$P_r = v_r \bullet i_r = \frac{v_r^2}{R_0} \tag{5}$$

Here, the r subscript stands for reflected (not absorbed) power, voltage or current, respectively.

Applying Kirchoff's laws to point x in *Figure 5*, the current to the load is

$$i_L = i_x - i_r \tag{6}$$

and voltage across the load is

$$v_L = i_L R_L = v_x + v_r \tag{7}$$

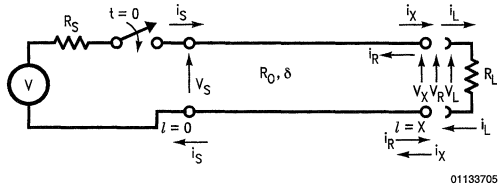


FIGURE 5. Boundary Conditions at the Line/Load Interface

To find the ratio of v_r to v_x so that it can be ascertained how much power is absorbed by the load, and how much is not absorbed (therefore, reflected), substitute v_x/R_0 for i_x and v_r/R_0 for i_r into *Equation (6)*.

$$i_L = \frac{v_x}{R_0} - \frac{v_r}{R_0} \tag{8}$$

Rearranging *Equation (7)* and substituting for i_L in *Equation (8)* yields

$$\frac{v_x + v_r}{R_L} = \frac{v_x}{R_0} - \frac{v_r}{R_0} \tag{9}$$

The minus sign associated with v_r/R_0 means, in this case, that the reflected voltage wave v_r travels in the –x direction toward the generator.

Collecting like terms of *Equation (9)* yields

$$v_x\left(\frac{1}{R_0} - \frac{1}{R_L}\right) = v_r\left(\frac{1}{R_0} - \frac{1}{R_L}\right) \tag{10}$$

So,

$$v_r = v_x \frac{\left(\frac{R_L - R_0}{R_0 R_L}\right)}{\left(\frac{R_L + R_0}{R_0 R_L}\right)} = v_x\left(\frac{R_L - R_0}{R_0 + R_L}\right) \tag{11}$$

and the desired relation for v_r/v_x is

$$\frac{v_r}{v_x} = \frac{R_L - R_0}{R_0 + R_L} \tag{12}$$

This ratio is defined as the voltage reflection coefficient of the load ρ_{VL}

$$\rho_{VL} \equiv \frac{v_r}{v_x} = \frac{R_L - R_0}{R_0 + R_L} \tag{13}$$

A similar derivation for currents shows

$$\rho_{IL} = -\frac{R_L - R_0}{R_L + R_0} = -\rho_{VL} \tag{14}$$

For the remainder of this application note and AN-808, the v or ı subscript on the reflection coefficient is dropped, and ρ_L is assumed to be the *voltage* reflection coefficient of the load. Similarly, applying Kirchoff's laws to the source-line interface, the voltage reflection coefficient of the source is

$$\rho_S = \frac{R_S - R_0}{R_S + R_0} \tag{15}$$

The current reflection coefficient of the source has the same magnitude as ρ_S, but is opposite in algebraic sign.

When a traveling wave v_x, i_x meets a boundary such as the line load interface, a reflected wave is instantaneously generated so that Kirchoff's laws are satisfied at the boundary conditions. This is the direct result of the conservation of energy principle. Referring again to *Figure 5*, the effects of three different termination resistance R_L values are shown.

Case 1, $R_L = R_0$

In this case, R_L is equal to the characteristic resistance of the line. Using *Equation (13)*, the voltage reflection coefficient of the load ρ_L is

$$\rho_L = \frac{R_0 - R_0}{R_0 + R_0} = \frac{0}{2R_0} = 0 \tag{16}$$

Kirchoff's Laws and Line-Load Boundary Conditions (Continued)

Since $v_r/v_x = \rho_L$, then $v_r = \rho_L v_x = 0$ and no reflection is generated. This agrees with the discussion of cut lines and matched load where a line terminated in its characteristic impedance behaves the same as an infinite line. All power delivered by the line is absorbed into the load. The waveforms appear as shown in *Figure 6*. The wave starting at the source at time t = 0 is reproduced at point x down the line after a time delay of $t = x\delta = \tau$.

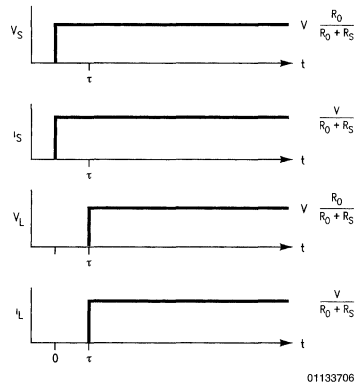


FIGURE 6. Waveforms for $R_L = R_0$

Case 2, $R_L > R_0$

To simplify this case, assume that $R_S = R_0$. This means that the initial voltage is

$$V\frac{R_0}{R_0 + R_0} = \frac{V}{2} \tag{17}$$

Also assume $R_L = 3\ R_0$, then the load voltage reflection coefficient is

$$\rho_L = \frac{3R_0 - R_0}{3R_0 + R_0} = +\frac{1}{2} \tag{18}$$

The voltage wave arriving at point x at time $t = x\delta$ generates a reflected voltage wave of magnitude

$$v_r = \rho_L v_x = \left(+\frac{1}{2}\right)\left(\frac{V}{2}\right) = \frac{V}{4} \tag{19}$$

and the load voltage is

$$v_L = v_x + v_r = \frac{V}{2} + \frac{V}{4} = \frac{3V}{4} \tag{20}$$

The reflected voltage wave v_r generated at $t = x\delta = \tau$ travels back down the line toward the source arriving at the source at time $t = 2x\delta = 2\tau$. This wave will be absorbed without generating another reflection because R_S was picked to equal R_0, making ρ_S equal to zero. The source voltage is now

$$v_S + v_r = \frac{V}{2} + \frac{V}{4} = \frac{3V}{4} \tag{21}$$

and equilibrium is achieved.

If the circuit in *Figure 5* is analyzed using simple circuit theory and neglecting the transmission line effects, it is easily seen that

$$v_S = v_L = V\frac{R_L}{R_0 + R_L} = \frac{3V}{4} \tag{22}$$

This agrees exactly with *Equation (21)* and will always be the case. After all reflections cease and the circuit reaches equilibrium, the steady state voltages and currents on the line are the same as those produced using simple dc circuit analysis. Waveforms for $R_L > R_0$ (specifically $R_L = 3\ R_0$) appear in *Figure 7*.

In general, the case where $R_L > R_0$ is viewed in the following manner. Because the line is capable of delivering more power than can be instantaneously absorbed by the load, the excess power is returned to the source and absorbed in the source resistor (assuming $R_S = R_0$).

An upper limit on the voltage reflection coefficient is found by allowing R_L to go to infinity. In this case, *Equation (13)* goes to +1.

Case 3, $R_L < R_0$

In this case, again set $R_S = R_0$ and allow R_L to equal $R_0/3$. The initial wave, as before, is

$$v_S = V\frac{R_0}{R_0 + R_S} = \frac{V}{2} \tag{23}$$

and the load voltage reflection coefficient is

$$\rho_L = \frac{R_L - R_0}{R_L + R_0} = \frac{\frac{R_0}{3} - R_0}{\frac{R_0}{3} + R_0} = -\frac{1}{2} \tag{24}$$

Therefore, the reflected voltage wave v_r is

$$v_r = \rho_L\frac{V}{2} = -\frac{V}{4} \tag{25}$$

which starts propagating back toward the source at time $t = \tau$. The load voltage at time $t = \tau$ is

$$v_x + v_r = \frac{V}{2} + -\frac{V}{4} = +\frac{V}{4} \tag{26}$$

Kirchoff's Laws and Line-Load Boundary Conditions (Continued)

The (−V/4) reflected wave arrives back at the source at time $t = 2\tau$. Because R_S is set equal to R_0, ρ_S is, then, equal to zero and no reflected wave will be generated. The voltage at the source is now

$$v_S + v_r + \rho_S v_r = \frac{V}{2} + -\frac{V}{4} + 0 = \frac{V}{4} \tag{27}$$

From a dc circuit analysis, the steady state voltage is

$$V_{SS} = V\frac{R_L}{R_L + R_0} = \frac{V}{4} \tag{28}$$

This agrees with the result of *Equation (27)*. The waveforms for Case 3 ($R_L < R_0$) appear in *Figure 8*.

An interpretation of the actions occurring when load resistance is less than the characteristic line resistance is as follows: when power available at the line end is less than the power the load can absorb, a signal is sent back to the source saying, in essence, "send more power".

It has been shown that a ratio of line and load resistance (ρ) can be used to calculate the voltages and currents in terms of a wave arriving at the boundary, possibly generating a reflected, reverse-traveling wave to satisfy the conservation of energy principle at the line-to-load boundary. This ratio is

$$V_{SS} = V\frac{R_L}{R_L + R_0} = \frac{V}{4} \tag{29}$$

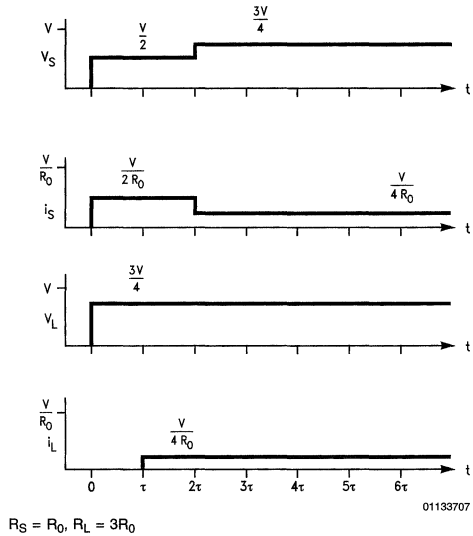
where R_B represents the resistance into the boundary, R_B is R_S when considering the source-to-line interface and R_B would be R_L when considering the line-to-load interface. It is obvious that if discussing impedances, then $Z_S$would be substituted for R_S in *Equation (29)*, and there may be some phase angle between the voltage and current waves.

The forward traveling wave, v_x, plus the reflected wave, v_r, is equal to the load voltage (V_L). Since v_r is $\rho_L\, v_x$, this can be expressed as

$$v_x(1 + \rho_L) = v_L \tag{30}$$

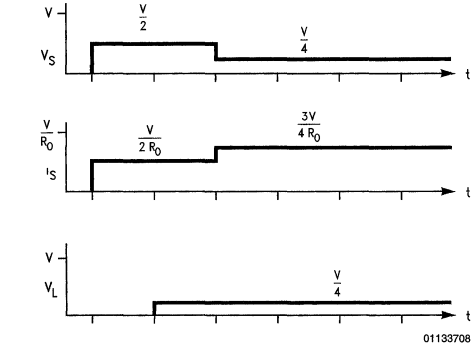
This quantity $(1 + \rho)$ can be defined as the voltage *transmission* coefficient of the load and it is known that

$$\frac{v_L}{v_x} = (1 + \rho_L) \tag{31}$$



$R_S = R_0$, $R_L = 3R_0$

FIGURE 7.



$$R_L = \frac{R_0}{3}$$

FIGURE 8.

Kirchoff's Laws and Line-Load Boundary Conditions (Continued)

The cases with various load resistances can be summarized.

	Condition		Circuit at time t = τ (one line delay time)
1.	$R_L = R_0$	$\rho_L = 0$	No reflection is produced—circuit reaches steady state immediately.
2.	$R_L > R_0$	$\rho_L > 0$	Positive voltage reflection—wave is sent back toward source. Voltage at load is higher than steady stage voltage (overshoot).
3.	$R_L < R_0$	$\rho_L < 0$	Negative voltage reflection—wave is sent back toward source. Voltage at load is lower than steady state voltage (undershoot).

Fundamental Principles

Before examining the algorithm for keeping track of reflections, there are two principles to keep in mind.

- Energy (as power) is conserved at boundary conditions (as explored previously)
- The principle of linear superposition applies. This means any arbitrary excitation function can be broken down into step functions, or ramps. The reaction of the circuit to each part can be analyzed, and the results can be added together when finished. This means that a positive pulse of duration t is examined by superimposing two step functions, one positive and one negative, starting after a delay of t (*Figure 9*). It also means the voltage at any point on the line is the sum of initial voltage plus the sum of all voltage waves that have arrived at or passed through the point up to and including the time of examination. Also, the current on the line is, at any point, the sum of initial current plus any forward or reverse traveling currents passing the point up to and including the time the current is examined.

It has also been established that the steady state solution for voltages and currents on the line can be found by simple dc circuit analysis.

In examining reflection effects for the remainder of this application note, the following conventions are used.

A voltage or current wave traveling *toward* the point of interest will have the subscript "i" for *incident* wave,

A voltage or current wave traveling *away* from the point of interest will have the subscript "r" for *reflected* wave,

The subscript "S" means the parameter applied to the *source* ($v_S$for the voltage at the source, etc.), and

The subscript "L" means the parameter applied to the *load* (v_L for the voltage at the load, etc.)

Sign conventions for voltage waves and their associated currents are shown in *Figure 10*.

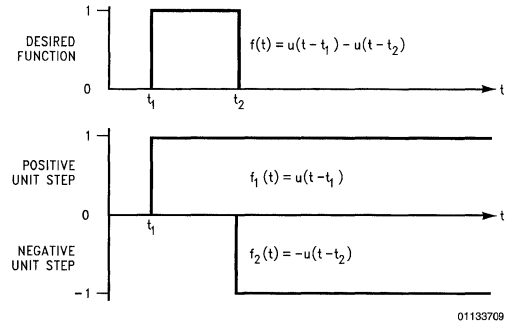


FIGURE 9. Superposition of Simple Waveforms to Form More Complex Excitations

Tabular Method for Reflections—the Lattice Diagram

The waves going up and down the line can be monitored by drawing a time scale, as a vertical line with time increasing in the down direction, to represent the location on the line under examination. Because voltages at the source and load ends of the transmission line are normally of primary interest, two time scales are necessary. Drawing arrows from one time scale to the other as in *Figure 10* shows the direction of travel of the waves during a specific time interval. Since the main concern is only with the waveforms at the line ends, time scales are ruled off in multiples of the time delay of the line τ. If a unit-step type wave is launched from the source at time t = 0+, it is known that the magnitude of the wave will persist unchanged until a wave arrives back from the load after a round trip delay time of two line delays. The source time scale then is incremented in multiples of 2 mτ where m = 0, 1, 2, 3,... Likewise, the first wave arrives at the load after a single time delay, so the first increment ruling on the load time scale is τ, or one time delay of the line. Because the subsequent waves arrive back at the load in increments of 2τ, the load time scale is ruled off in multiples of (2m + 1)τ where m = 0, 1, 2, 3,... The operation of the lattice diagram is discussed using the example in *Figure 11* which is the lattice diagram for the associated circuit.

time t = 0– (just before the switch closes)

The voltages at the source and load are equal with a magnitude of $v_{initial}$. Assume that no initial voltage is present. So, in this case, the voltage at the source and load equals zero.

$$V_{initial} = v_S(0-) = V_L(0-) = 0$$

time t = 0+ (just after the switch has closed)

Tabular Method for Reflections— the Lattice Diagram (Continued)

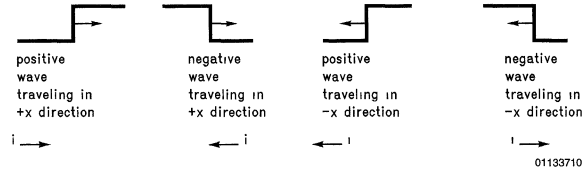
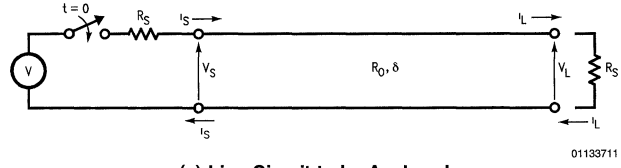
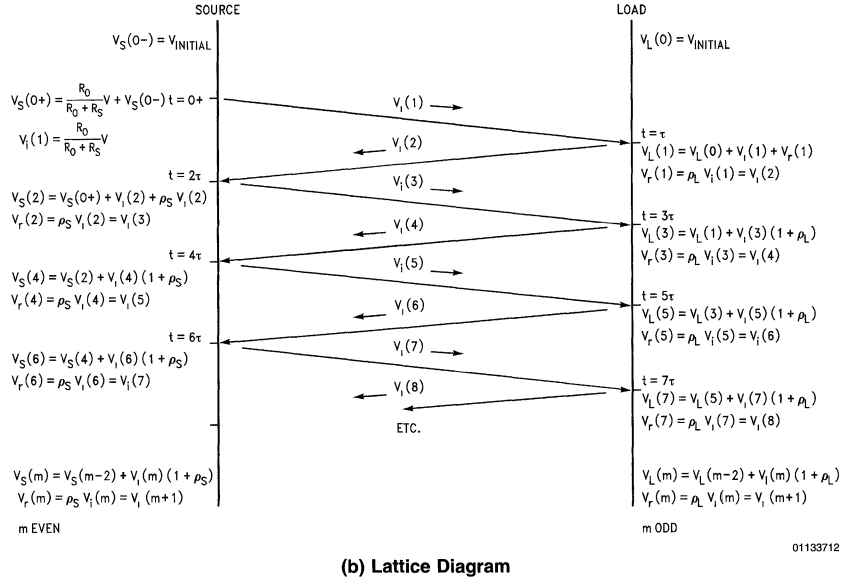


FIGURE 10. Sign Conventions for Waves



(a) Line Circuit to be Analyzed



(b) Lattice Diagram

FIGURE 11. Reflection Bookkeeping with the Lattice Diagram

The first wave $v_i(1)$ is launched at the source and begins to travel toward the load end of the line. As previously mentioned, a voltage divider action between R_S and R_0 is used to derive the magnitude of the initial voltage wave.

$$v_i(1) = V \frac{R_0}{R_0 + R_S}$$

At this time, the voltage at the source is the sum of the initial voltage plus the voltage wave $v_i(1)$ just generated.

$$v_S(0+) = v_S(0-) + v_i(1) = 0 + V \frac{R_0}{R_0 + R_S}$$

Tabular Method for Reflections—the Lattice Diagram (Continued)

Because the switch closure represents a step function, the source voltage remains at this level until a wave returns after reflecting from the load at time t = 2τ.

time t = τ

The incident voltage wave $v_i(1)$ now arrives at the load and generates a reflected voltage wave

$$v_r(1) = \rho_L v_i(i);\ \rho_L = \frac{R_L - R_0}{R_L + R_0}$$

where ρ_L is the voltage reflection coefficient of the load. The reflected voltage wave $v_r(1)$ immediately starts traveling back toward the source becoming the incident voltage wave $v_i(2)$ which arrives back at the source at t = 2τ. The voltage at the load is now the sum of the initial voltage plus the incident voltage wave $v_i(1)$ that just arrived plus the reflected voltage wave that is just departing.

$$\begin{aligned} v_L(1) &= v_L(0-) + v_i(1) + v_r(1) \\ &= 0 + v_i(1) + \rho_L v_i(1) \\ &= v_i(1)\,(1 + \rho_L) \end{aligned}$$

Again, because of the step function excitation, the load voltage remains unchanged until the new wave arrives at time t = 3τ.

time t = 2τ

$v_i(2)$ now arrives at the source and generates a reflected voltage wave $v_r(2)$ of magnitude

$$v_r(2) = \rho_S v_i(2);\ \rho_S = \frac{R_S - R_0}{R_S + R_0}$$

where ρ_S is the source voltage reflection coefficient.

The reflected voltage wave $v_r(2)$ starts back toward the load end of the line and becomes the incident voltage wave $v_i(3)$ arriving at the load at time t = 3τ. The voltage at the source is now the sum of the voltage that was there plus the incident voltage wave just arrived plus the reflected voltage wave just departed for the load.

$$\begin{aligned} v_S(2) &= v_S(0+) + v_i(2) + v_r(2) \\ &= v\frac{R_0}{R_0 + R_S} + v_i(2) + \rho_S v_i(2) \\ &= v\frac{R_0}{R_0 + R_S} + v_i(2)\,(1 + \rho_S) \end{aligned}$$

time t = 3τ

$v_i(3)$ arrives at the load generating $v_r(3)$

$$v_r(3) = \rho_L v_i(3)$$

$v_r(3)$ departs back toward the source becoming $v_i(4)$ to the source. The load voltage is now

$$v_L(3) = v_L(1) + v_i(3)\,(1 + \rho_L)$$

time t = 4τ

When $v_i(4)$ arrives at the source and generates $v_r(4)$, then

$$v_r(4) = \rho_S v_i(4)$$

starts back toward the load to become $v_i(5)$ to the load. The load voltage is now

$$v_L(4) = v_L(2) + v_i(4)\,(1 + \rho_L)$$

This process can continue ad infinitum or until no measurable changes are detected. The reflection process at that time is considered complete and the line assumes a steady state condition. Steady state conditions can be found by applying simple dc circuit theory to source load circuits.

Summarizing this lattice diagram method, any time t = mτ and m > 1, the following relationships exist:

If m is odd, the $v_i(m)$ wave is arriving at the load and generates a reflected wave

$$v_r(m) = \rho_L v_i(m)$$

This becomes $v_i(m + 1)$ as it starts toward the source. The voltage at the load at time t = mτ will be

$$v_L(m) = v_L(m - 2) + v_i(m)\,(1 + \rho_L)$$

This is the sum of the voltage that was there before the wave arrived, i.e., $v_L(m - 2)$, plus the wave arriving $v_i(m)$ and the reflected wave $v_r(m)$ departing.

If m is even, the $v_i(m)$ wave is arriving at the source and generates a reflected wave

$$v_r(m) = \rho_S v_i(m)$$

This becomes $v_i(m + 1)$ as it starts toward the load. The voltage at the source is now

$$v_S(m) = v_S(m - 2) + v_i(m)\,(1 + \rho_S)$$

This is the sum of the voltage that was present $v_S(m - 2)$ plus the incident wave arriving $v_i(m)$ plus the reflected wave departing $v_r(m)$.

The voltage and current at the source end of the line for a lossless line can be expressed as a summation.

$$v_S(t) = \frac{R_0}{R_S + R_0} \bullet \left[e(t)u(t) + \left(1 + \frac{1}{\rho_S}\right) \sum_{n=1}^{\infty} \rho_S^n \rho_L^n e(t - 2n\tau)u(t - 2n\tau) \right] \tag{32}$$

$$i_S(t) = \frac{1}{R_S + R_0} \bullet \left[e(t)u(t) + \left(1 - \frac{1}{\rho_S}\right) \sum_{n=1}^{\infty} \rho_S^n \rho_L^n e(t - 2n\tau)u(t - 2n\tau) \right] \tag{33}$$

where e(t) is the generator voltage as a function of time, and u(t) is the unit step function.

Likewise, the load voltage and load current for the lossless line can be expressed as a summation.

$$v_L(t) = \frac{R_0}{R_S + R_0} \bullet (1 + \rho_L)\left[\sum_{n=0}^{\infty} \rho_S^n \rho_L^n e(t-(2n+1)\tau)u(t-(2n+1)\tau) \right] \tag{34}$$

Tabular Method for Reflections—the Lattice Diagram (Continued)

$$i_L(t) = \frac{1}{R_S + R_0} \bullet (1 - \rho_L)\left[\sum_{n=0}^{\infty} \rho_S^n \rho_L^n e(t-(2n+1)\tau)u(t-(2n+1)\tau)\right] \quad (35)$$

A similar expression of summation can be developed for the voltage (or current) at any point along the line at any time.

Because the lattice diagram is tabular in method, a computer program can be written relieving the designer of bookkeeping and repetitive calculations. A BASIC computer program for lattice diagrams appears in >*Figure 12*.

Limitations of the Lattice Diagram Method

Before using the lattice diagram to explore reflection effects with various source and load characteristics, it is necessary to pause at this point and examine the models used by the lattice diagram.

First, both the line driver and receiver are simulated either by a constant input or output resistance. The source has two voltage sources and a switch representing the internal source voltage at a time less than zero and equal to (or greater than) zero. The receiver is represented by a single resistor shunting the line end opposite the driver site. The line itself is represented by its characteristic resistance R_0 and its total one-way time delay (τ). This is equal to length times propagation delay per unit length. This model is shown in *Figure 12*.

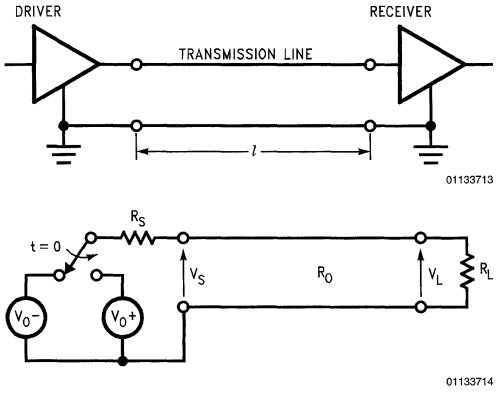


FIGURE 12. Model Used for Lattice Diagram Method

Because most data communication circuits are voltage types, that is, the receiver senses the line voltage to decide if a logic One or logic Zero is present, the primary interest is in voltages at the source and load as a function of time. Major exceptions include the current loops used in teletypewriters, telegraphs, and burglar alarm systems. The majority of data communications circuits used in computers, peripherals, and general controllers are voltage types.

The lattice diagram method cannot easily use source or receiver current/voltage relationships that are non-linear; i.e., not purely resistive. For non-linear current/voltage characteristics such as found in diodes, a graphic method can be used called the reflection diagram or the Bergeron method.

Note: A French hydraulic engineer, L J B Bergeron developed the method to study the propagation of water hammer effects in hydraulics See references, AN-806

Signals exchanged using lattice diagrams are of the unit step variety. When ramps or more complex waves are exchanged, the complexity of the bookkeeping increases dramatically. Additionally, the lines are presumed to be lossless, although a constant line attenuation factor could be accommodated without excessive bookkeeping. These limitations should be kept in mind when examining various source and load resistance combinations and their reflection characteristics.

There are three classes of source resistance, $R_S < R_0$, $R_S = R_0$ and $R_S > R_0$. There are also three classes of load resistance, $R_L < R_0$, $R_L = R_0$ and $R_L > R_0$. This gives nine types of single driver, single receiver line circuits. Each circuit will be examined in turn to determine reflection effects for these combinations with evaluations of each combination for voltage type communications.

Reflection Effects for Voltage Source Drivers

Initial waves launched by a voltage source type driver ($R_S < R_0$) are greater than one-half the magnitude of the internal voltage source. Referring to *Figure 12*, the initial voltage wave is derived as follows.

$$v_i(1) = (V_{0+} - V_{0-}) \bullet \frac{R_0}{R_0 + R_S} \quad (36)$$

while the voltage at the source at t = 0+ is

$$v_S(0+) = v_S(0-) + v_i(1) = V_{0-} \bullet \frac{R_L}{R_L + R_S} + v_i(1) \quad (37)$$

If the receiver switching point is at the mean of the driver voltage swing, the initial wave always has sufficient magnitude to indicate the correct logic state as it passes the receiver site. This maximizes the noise margins of the receiver.

Since $R_S < R_0$, the source voltage reflection coefficient ρ_S is less than zero. Any voltage waves, then, arriving back at the source are changed in sign, reduced in amplitude (assuming $R_S > 0\Omega$), and sent back toward the load. If the load resistance equals the characteristic line resistance ($R_L = R_0$), the voltage reflection coefficient of the load is

$$\rho_L = \frac{R_L - R_0}{R_L + R_0} = \frac{0}{2R_0} = 0$$

No reflections, therefore, are generated at the load. The voltage wave produced at the source is reproduced at the load after a time delay of $\tau = \ell\delta$, and the line assumes a steady state condition. *Figure 16* illustrates the source and load voltage waveforms for this case.

If R_L is greater than R_0, ρ_L is positive. Waves arriving at the load generate the same polarity reflections as the arriving

Reflection Effects for Voltage Source Drivers (Continued)

waves. ρ_S and ρ_L are of opposite signs, so a dampened oscillatory behavior of the load voltage is expected. The oscillation period or *ringing* is 4τ. The overshoot of v_L from t = τ to 3τ may cause breakdown of the input circuitry of a receiver, depending on the receiver voltage rating. The undershoot at t = 3τ or 5τ can reduce the noise immunity of a receiver or even cause a logic level misinterpretation—an error in the data. These waveforms are shown in *Figure 16*.

If R_L is less than R_0, then ρ_L is negative and a wave arriving at the load generates a reflection opposite in polarity to the incident wave. This causes the voltage at the source to overshoot steady state voltage at t = 0. Each reflection returning from the load causes the source voltage to continually step down toward the steady state voltage V_{SS}. These steps last for 2τ, or one round trip delay. Load voltage starts an increasing step-up waveform towards V_{SS} at time t = τ, with steps again taking one round trip delay, 2τ. A line receiver placed in the middle of the line sees an entirely different waveform—dampened oscillations much like the load voltage in *Figure 16*. This is caused by the negative signs of both source and load voltage reflection coefficients. Each time an incident wave arrives at either source or load, the reflected wave generated at that time has a sign opposite to the sign of the incident voltage wave. The voltage at a distance half way down the line is composed of these forward and reverse traveling waves arriving at that point commencing at time t = 0.5τ, and with each new wave passing that point after one line delay (τ). These waveforms are shown in *Figure 16*.

The optimum load resistance for voltage signal communications on transmission lines driven by a low impedance source ($R_S < R_0$) is equal to the characteristic line resistance. Large signal line voltages are produced and there are no reflection effects complicating the waveforms *Figure 14*.

However, a matched load ($R_L = R_0$) is a dc load on the driver, thus it increases system power dissipation. But, it does preserve signal fidelity and amplitude allowing use of multiple bridging receivers ($R_{in} \gg R_0$) along the line.

The unterminated case ($R_L > R_0$) reduces dc driver loading and also reduces system power dissipation over the matched load case. The unterminated case does, however, allow the load signal to exhibit pronounced overshoot and undershoot around the steady state voltage. If the load signal undershoot places the receiver in its threshold uncertainty region, data errors result. There is a way to "civilize" the voltage waveform of the unterminated line load by trading off signal rise time versus line time delay This is discussed later.

The final case of $R_S < R_0$ and $R_L < R_0$ is not generally useful in terms of voltage signals produced (*Figure 16*). Systems using this case consume more power than the previous two cases and have no particular advantage for voltage mode communications

Reflection Effects for Voltage Source Drivers (Continued)

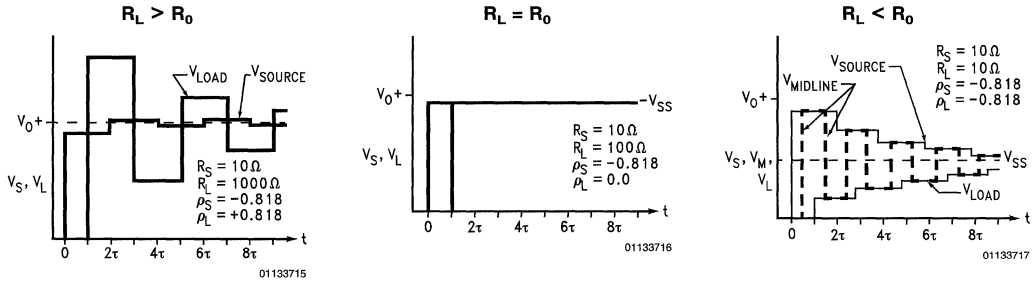


FIGURE 13. $R_S < R_0$

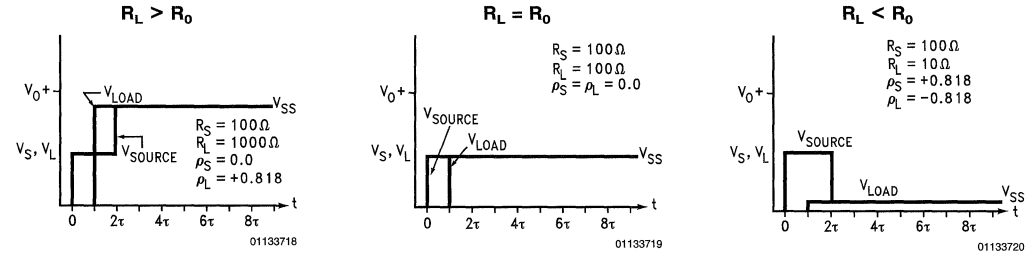


FIGURE 14. $R_S = R_0$

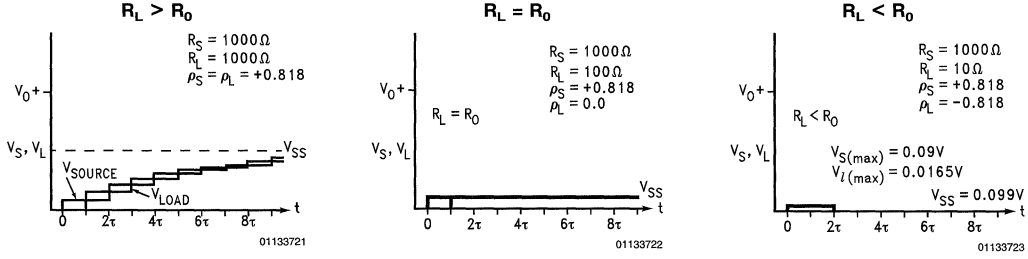


FIGURE 15. $R_S > R_0$

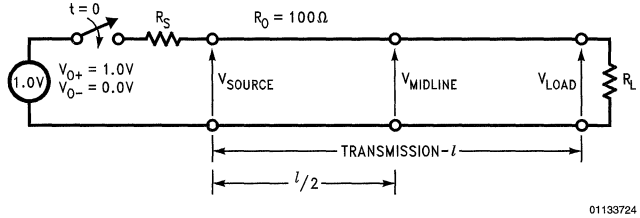


FIGURE 16. Source and Load Voltage Waveforms for Various R_S and R_L

Reflection Effects for Matched-Source Drivers

In all three cases under discussion here, the initial voltage produced by the driver onto the line is

$$v_i(1) = (V_{0+} - V_{0-})\frac{R_0}{R_0 + R_S} = \frac{1}{2}(V_{0+} + V_{0-}) \quad (38)$$

since $R_S = R_0$. The voltage at the source at time t = 0+ is

$$v_S(0+) = v_S(0-) + v_i(1) = V_{0-} \bullet \frac{R_L}{R_L + R_S} + v_i(1) \quad (39)$$

Assume, for clarity, that initial voltage (V_{0-}) is zero, thus *Equation (39)* simplifies to

$$v_S(0+) = \frac{V_{0+}}{2} \quad (40)$$

Since $R_S = R_0$, ρ_S is equal to zero. This means that load-generated reflections due to load mismatch are absorbed at the source when, at time t = 2τ, the reflected wave arrives back at the source. The line then assumes a steady state throughout. This back match or series termination effect of a matched source allows a wide latitude in choice of load resistance without sacrificing the signal fidelity of the load voltage waveform.

If the load resistance equals the characteristic line resistance $R_L = R_0$, then ρ_L equals zero and no load site reflections are generated The initial voltage wave arrives at the load at time t = τ (one line delay) and voltages (and currents) on the line immediately assume steady state conditions (see *Figure 16*). The optimum receiver threshold here is one-half the steady state voltage or $V_{0+}/4$. The main advantage over the voltage source type driver with matched load case ($R_S < R_0$, $R_L = R_0$) is that $R_S$and R_L resistance tolerances may be relaxed without incurring much signal *ringing*. This effect is due primarily to the termination provided by both line ends, rather than just one line end. Any reflected voltage wave on either system is attenuated by the product of ρ_S and ρ_L for each round trip line delay time. Since the $\rho_S\rho_L$ product for the fully matched case is smaller than the $\rho_S\rho_L$product for the single matched case, the reflections are attenuated and die out in fewer round trips. For example, if 20% tolerance resistors are used in both cases, ρ_S and ρ_L values for the fully matched case become 0.0 ±0.0909, which is a $\rho_S\rho_L$ product of ±0 0033. This means that after one round trip (2τ), the reflection amplitude starting back toward the load would be less than 0.33% of the initial wave.

Using $R_S = 10\Omega$, $R_L = 100\Omega$, and $R_0 = 100\Omega$ as for *Figure 16*, shows the same 20% tolerances applied to the single matched case

$$-0.8519 \le \rho_S \le -0.7857$$
$$-0.0909 \le \rho_L \le +0.0909$$

and

$$|\rho_S \le \rho_L| \le 0.0909$$

The voltage reflection amplitude after one round trip is a maximum of 7.7% of the initial wave.

The choice between using the single and fully matched system should be carefully considered because the fully matched system does sacrifice signal voltage magnitude to get a decreased dependence on absolute resistor values.

If the load resistance for a matched driver circuit is made much greater than the line resistance, the initial wave arriving at the load at time t = τ will be almost double since ρ_L will be close to +1.0 Because source resistance is set equal to line resistance, ρ_S becomes zero, the reflected voltage wave from the load is absorbed by the source at time t = 2τ, and steady state conditions prevail. Waveforms for this case are shown in *Figure 16*. This is called *back matching* or *series termination*.

The main advantage of series termination is a great reduction in steady state power consumption when compared with the parallel terminated case ($R_S \ll R_0$, $R_L = R_0$) At the same time, series termination provides the same signal fidelity to a receiver placed at the line end. Compare the load voltage waveforms for the two cases in and *Figure 16*. The main disadvantage to series termination is that receivers placed along the line see a waveform similar to that shown for the source in *Figure 16*. That is, receivers along the line see the $V_{0+}/2$ initial wave as it passes that point on the line, and do not see a full signal swing until the load end reflection passes that point. Consequently, receivers along the line do not see a signal sufficient to produce the valid logic state output until the load reflection returns. Depending on actual line length and receiver characteristics, the receiver may even oscillate, having been placed in its linear operation region. With the benefit, then, of reducing system power, the series termination method has a constraint of allowing only one line receiver located at the line load end. The parallel termination method should be used if other receivers along the line are required.

The final case of matched source drivers is with the use of a load resistance less than the characteristic line resistance. The waveforms for this case are shown in *Figure 16*. A line receiver with a threshold of $V_0/4$ placed at the source responds like a positive, edge triggered one-shot and produces a pulse in response to a +V/2 initial wave of 2τ duration. Aside from its use as a one-shot, this circuit doesn't seem to offer any advantages for voltage mode communications.

Reflection Effects for Current-Source Drivers

The name *current source drivers* is somewhat of a misnomer, and might be more properly called *current-limited voltage source drivers*. True *current source* drivers such as the DS75110A are normally used in conjunction with parallel termination resistors to create a matched source.

The *current source* drivers ($R_S > R_0$) discussed resemble true current sources in the respect that their output resistance is usually much greater than the characteristic line resistance. The initial voltage step produced on the line is thus usually small $v_i(1) = (i_S(1)R_0)$. This is due to the voltage divider action of the driver source resistance and the characteristic line resistance.

Voltage waveforms for a current source type driver either step up to V_{SS}, reach steady state after 2τ, or execute a dampened oscillation around V_{SS}, depending on whether the load resistance R_L is greater, equal, or less than R_0, respectively. The second case $R_L = R_0$ provides signals much the same as the other two cases where $R_L = R_0$, that is, the source voltage steps immediately to V_{SS}, with the load voltage following after one line time delay. Here the amplitude of the signal is much smaller than previous matched load cases. Since the current source type drivers (DS75110A)

Reflection Effects for Current-Source Drivers (Continued)

have high off-state impedances, they allow multiple drivers on the line to produce data bus or party line. Waveforms for the matched load case are shown in *Figure 16*.

The case $R_L < R_0$ really provides no useful advantage for voltage mode communications. The negative sign for ρ_L and the positive sign for ρ_S lead to dampened oscillatory behavior, or ringing. The maximum perturbation takes place at the source end of the line. Waveforms for this case are similar to those shown in *Figure 16*, and are shown to scale in *Figure 16*. With the given values used to produce the figure, the maximum amplitude ringing appears at the source line end.

The $R_L > R_0$ case is of interest because it is representative of DTL driving a transmission line with the output going from LOW to HIGH. DTL has a high value R_S, (2 kΩ or 6 kΩ) in the HIGH logic state. Since both R_S and R_L are greater than R_0, both ρ_S and ρ_L are positive. A small voltage step starts from the source at t = 0+; its magnitude is

$$v_i(1) = V\frac{R_0}{R_0 + R_S}$$

Note: Since the input diode is not represented, the representation of DTL input as a single resistor to ground is not strictly correct For purposes of approximation, this simple representation is used Treatment of non-linear current/voltage sources and loads is covered by Metzger & Vabre. (op cit)

Upon arrival at the load at time $t = \tau$, this initial wave generates a positive voltage reflection since $\rho_L > 0$. The voltage reflection arrives back at the source site at time $t = 2\tau$. Since ρ_S is also positive, another positive voltage reflection is launched back toward the load. The process repeats, and the source and load voltages both execute a step-up approach toward steady state voltage V_{SS}. These waveforms are shown in *Figure 16*.

In examining voltage at the line midpoint ($x = \ell/2$), a step-up type waveform is seen which is the sum of all the incident voltage waves passing the line midpoint up to the time of examination. The midpoint voltage is expressed as follows.

$$v_m(t) = V_{SS}(1 - \exp[-(t + 0.5\tau)/T]) \qquad (41)$$

Note: This equation is presented without derivation, but a procedure similar to that used by Matick (Ref 2, AN-806) can be used

for $t = n + 0.5\tau$ with n = 0, 1, 2, 3, etc. V_{SS} in *Equation (41)* is the steady state line voltage

$$V_{SS} = V_{0+} \bullet \frac{R_L}{R_S + R_L}$$

and T is a time constant given by

$$T = -\frac{2\tau}{\ell\, n(\rho_S \rho_L)} \qquad (42)$$

with τ being one line delay ($\tau = \ell\delta$).

Note: This equation is presented without derivation, but a procedure similar to that used by Matick (Ref 2, AN-806) can be used

Equation (41) provides an exact solution for odd multiples of n (n = 1, 3, 5..., so $t = 1.5\tau, 3.5\tau, 5.5\tau...$), while it approximates $v_m(t)$ for even multiples of n (n = 0, 2, 4..., so $t = 0.5\tau$, 2.5τ, 4.5τ...). The closer the $\rho_S\rho_L$ product is to 1, the better *Equation (41)* predicts $v_m(t)$, particularly for even multiples of n. To illustrate the fitting, *Table 1* and *Table 2* are generated by the BASIC language computer program *Table 3* and their data is plotted in *Figure 18*.

Designers familiar with DTL circuits should quickly recognize that the waveforms shown in *Figure 18* are very similar to the rising edge waveforms found when a DTL gate output goes from the LOW to HIGH state. This characteristic waveform has usually been attributed to the series RC circuit (a gate output resistance driving a lumped transmission line capacitance). The time constant for this approach, based on the C(dv/dt) = i rule from simple circuit theory, provides only an approximation. The actual cause of the waveform shape, however, is due to reflection effects. Unfortunately, the only way to speed up the rising edge is to reduce source resistance, (providing an initial step greater than the receiving threshold) and terminate the line to eliminate the load reflections.

DTL inability to drive transmission lines at high repetition rates is the direct result of the signal rise time limitation caused by positive reflection coefficients for both the source and load. A transmitted positive pulse may be missed if its duration is less than the time required for the load signal to reach the receiver threshold.

The $R_S > R_0$ and $R_L > R_0$ case provides no definite advantages as voltage mode communication is concerned. This case, in fact, poses a definite hazard to high speed data communications because the reflections cause, in effect, a slow, exponential signal transition. Because line delay is a factor, longer lines will only increase the effect.

TABLE 1. (R_S = 2000Ω, R_0 = 100Ω, R_L = 4000Ω)
RHOS = 0.904762 RHOL = 0.951220 TAU = −13.3250 V1(1) = 4.76190H-C2 V_{SS} = 0.666667

TIME	VM(T)	VAPPX	%DIFF
0.5	0.04762	0.04820	+1.220%
1.5	0.09292	0.09292	+0.000%
2.5	0.13390	0.13440	+0.373%
3.5	0.17288	0.17288	+0.000%
4.5	0.20815	0.20858	+0.207%
5.5	0.24170	0.24170	+0.000%
6.5	0.27206	0.27243	+0.136%
7.5	0.30093	0 30093	+0.000%
8.5	0.32705	0.32737	+0.097%
9.5	0.35190	0.35190	+0.000%
10.5	0.37439	0.37466	+0.073%
11.5	0.39577	0.39577	+0.000%
12.5	0.41512	0.41536	+0.057%
13.5	0.43353	0.43353	+0.000%
14.5	0.45018	0.45038	+0.045%
15.5	0.46602	0.46602	+0.000%
16.5	0.48035	0.48053	+0.036%
17.5	0.49399	0.49399	+0.000%
18.5	0.50632	0.50647	+0.030%
19.5	0.51805	0.51805	+0.000%
20.5	0.52867	0.52880	+0.024%
21.5	0.53877	0.53877	+0.000%

Reflection Effects for Current-Source Drivers (Continued)

TABLE 2. (R_S = 500Ω, R_0 = 75Ω, R_L = 10 kΩ)
RHOS = 0.739130 RHOL = 0.985112 TAU = −6.30356 V1(1) = 1.30435 V_{SS} = 0.952381

TIME	VM(T)	VAPPX	%DIFF
0.5	0.13043	0.13971	+7.112%
1.5	0.25893	0.25893	+0.000%
2.5	0.35390	0.36066	+1.909%
3 5	0.44746	0.44746	+0.000%
4.5	0.51661	0.52153	+0.952%
5.5	0.58473	0.58473	+0.000%
6.5	0.63509	0.63867	+0.564%
7.5	0.68469	0.68469	+0.000%
8.5	0.72135	0.72396	+0.361%
9.5	0.75747	0.75747	+0.000%

RHOS = 0.739130 RHOL = 0.985112 TAU = −6.30356 V1(1) = 1.30435 V_{SS} = 0.952381

TIME	VM(T)	VAPPX	%DIFF
10.5	0.78416	0.78606	+0.242%
11.5	0.81046	0.81046	+0.000%
12.5	0.82990	0.83128	+0.167%
13.5	0.84904	0.84904	+0.000%
14.5	0.86320	0.86420	+0.117%
15.5	0.87714	0.87714	+0.000%
16.5	0.88744	0.88818	+0.083%
17.5	0.89759	0.89759	+0.000%
18.5	0.90510	0.90563	+0.059%
19.5	0.91249	0.91249	+0.000%
20.5	0.91795	0.91834	+0.042%
21.5	0.92334	0.92334	+0.000%

Reflection Effects for Current-Source Drivers (Continued)

TABLE 3. BASIC Program Listing

```
100   PRINT'ENTER RS, R0, RL'1
110   INPUT R1, R0, R2
120   P1=(R1-R0)/R1+R0)
130   P2=(R2-R0)/R2+R0)
140   V1=R0/R1+R0)
150   K1=2./LOG(P1*P2)
160   V9=R2/(R1+R2)
170   PRINT'RHOS='; P1;'RHOL=';PS;'TAU=';K1
180   PRINT 'V1(1)=';V1;'VSS=';V9
190   V=V1
200   PRINT'TIME VM(T) VAPPX %DIFF'
210   FOR T=0.5 TO 20.5 STEP 2.
220   V2=V9*(1.-EXP((T+.5)/KL))
230   P=100.*(V2-V)/V
240   PRINT USING 250,T,V,V2,P
250   :##.# -#.##### -#.##### +###.###%
260   V1=V1*P2
270   V=V+V1
280   REM SOURCE END
290   V2=V9*(1.-EXP( (T+1.5)/k1 ) )
300   P=100.*(V2-V)/V
310   PRINT USING 250,T+1.,V,V2,P
320   V1=P1*V1
330   V=V+V1
340   NEXT T
350   PRINT
360   PRINT
370   PRINT
380   GOTO 100
390   END
```

FIGURE 17. Comparison of v_m Formula to Computed Midline Voltage

Reflection Effects for Current-Source Drivers (Continued)

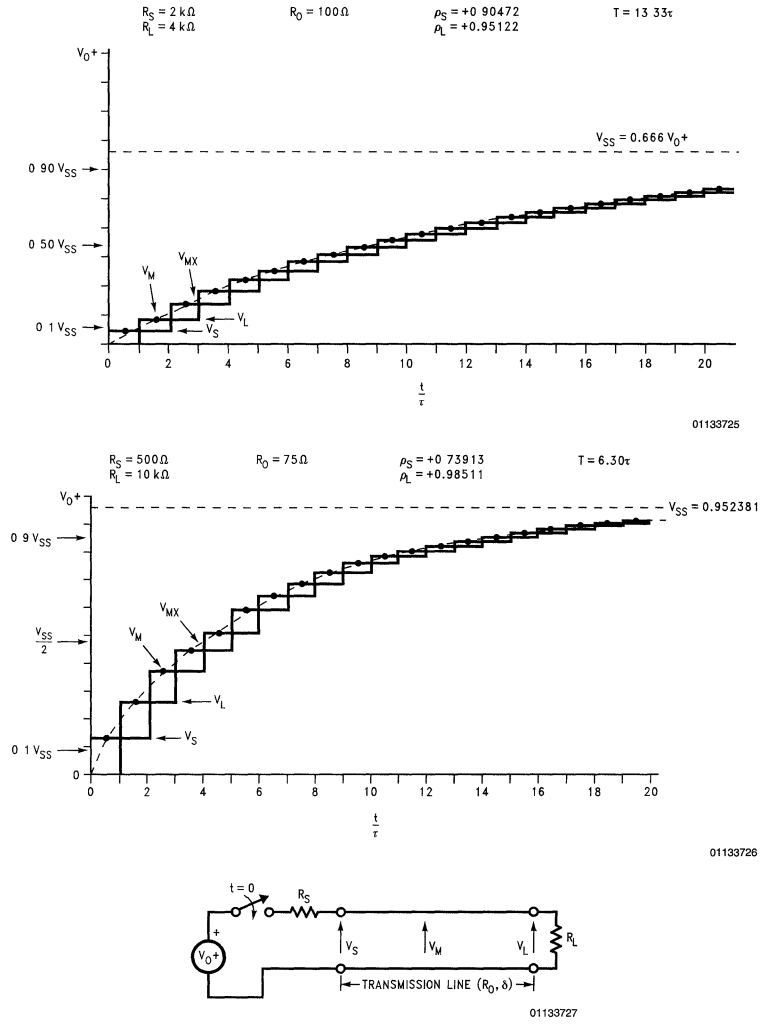


FIGURE 18. Approximation of Midline Voltage with $R_S > R_0$ and $R_L > R_0$

$$v_{MX}(t) = V_{SS}\left(1 - \exp[-(t + 0\,5\tau)/T]\right)$$

$$t = \frac{-2\tau}{\ell n\,(\rho_S\,\rho_L)}$$

Summary—Which are the Advantageous Combinations?

In examining the basic combinations of source, line and load resistances, and typical waveforms characteristic of each case, advantageous combinations can be determined. The primary results are tabulated in *Figure 19.* those combinations generally used in voltage mode communications circuits are as follows.

1. Unterminated case ($R_S \ll R_0$, $R_L \gg R_0$). This situation provides low steady state power dissipation and large signal levels, but also shows pronounced "ringing" effects. The "ringing" can be reduced by controlling signal rise/fall time versus τ, or by clamping diodes to limit load signal excursions. This case is representative of TTL circuits and is thus widely employed.
2. The parallel terminated case ($R_S \ll R_0$, $R_L = R_0$) provides large signal levels, and excellent signal fidelity. However, it is power consuming with most of that power dissipated in the load resistor. This case is useful for cleaning up the reflection effects of Case 1 but, at the same time, does require a driver circuit to have its internal current limits set at greater values than those required to produce the desired signal level into the minimum line resistance used. Thus, this case requires specific line driver devices such as the DS75114/DS9614. Ordinary TTL, except for the above mentioned circuits, has too low a current limit point to adequately drive 50Ω lines.
3. The series terminated or backmatched driver case $R_S = R_0$, $R_L \gg R_0$ provides a low steady state power dissipation system for use with one receiver located at the load end of the line. The positive reflection coefficient of the load is used to approximately double the initial wave arriving at the load. Setting $R_S = R_0$ terminates the reflected wave when it arrives back at the source site after two line delays, and the line then assumes steady state conditions. The use of other receivers located along the line is not recommended, because they will not see the full driver signal swing until the reflection from the load passes their particular bridging points Such receivers could malfunction, as they would see a voltage very close to their threshold, and perhaps even place the line receiver in its linear operating region. This could make the line receiver sensitive to oscillatory, parasitic feedback. If these constraints are acceptable, the series termination method can be used to good advantage in providing the same signal fidelity and signal amplitude as with the parallel termination method, while at the same time, contributing a significant savings in steady state power consumption.
4. The fully matched case $R_S = R_0$, $R_L = R_0$ not only provides excellent signal fidelity all along the line, but also has reduced signal amplitude over that of the parallel terminated case. Additionally, the power consumption is somewhat less than the parallel termination case and the power is divided equally by the source and load. The primary advantage of the fully matched system is that termination resistor tolerances can be relaxed somewhat without incurring large amounts of ringing. This is because both the source and load act as line terminations.

Summary—Which are the Advantageous Combinations? (Continued)

Configuration Name (if any)	(Driver) Source Resistance	(Receiver) Load Resistance	Signal Characteristics	Optimum Receiver Threshold	Line Receivers Allowed at Other Than Load End of Line?	Comments
Unterminated	$\ll R_0$	$\gg R_0$	Ringing Pronounced	0.5 V_{SS}	Yes	Undershoot May Cause Errors
Parallel Terminated	$\ll R_0$	$= R_0$	Excellent Fidelity	0.5 V_{SS}	Yes	Load Resistor Consumes Power $P_L = \frac{(V_{SS})^2}{R_L}$
	$\ll R_0$	$\ll R_0$	Awful—Different Signals at Each Point on the Line	NA	No	Not Generally Useful
Series Terminated or Backmatched Driver	$= R_0$	$\gg R_0$	Load Signal Excellent	0.5 V_{SS}	No	Reduced Power Consumption Over Parallel Termination
Fully Matched	$= R_0$	$= R_0$	Excellent Fidelity	0.25 V_{SS}	Yes	Greater Tolerances on Resistors Allowed for Same Fidelity as Parallel Termination
	$= R_0$	$< R_0$	Load Signal Like a One-Shot	NA	NA	Not Generally Useful for Data, is Useful as Pulse Generator
	$\gg R_0$	$\gg R_0$	Exponential Like Signal Waveforms	0.5 V_{SS}	Yes	Low Power Consumption. Increased Delay due to Signal "Rise" Times.
	$\gg R_0$	$= R_0$	Small Signal Amplitude and Excellent Fidelity	0.5 V_{SS}	Yes	Produces Only Small Signal Voltages Compared with Other Methods. Uses Current Sinking Drivers such as the 75110A.
	$\gg R_0$	$< R_0$	Very Small Signal Amplitudes, also Ringing	NA	NA	Not Generally Useful

FIGURE 19. Summary of Effects

Effect of Source Rise Time on Waveforms

Previously, it was assumed that the source-produced signal rise time was always much less than the line time delay (τ). Because the waveforms for the source and load voltage were the superposition of incident and reflected waves occurring at their proper times, and because the shape of each wave was a square edged step function, the resultant source and load waveforms were thus also square edged, or *ideal* in nature. In many practical cases, particularly when line length is short, the source excitation possesses a finite, and non-negligible, rise time. Therefore, depending on the ratio of rise time to line delay, it is possible to have a new wave start arriving at the point of interest *before* the previous wave can reach its final value. The net waveform for voltage or current at that point, then, would consist of the superposition of two or more waves during their time of overlap. To study the superposition effect on signal waveforms, the source excitation is represented as a simple linear ramp rise to its final value of V_{0+}, so

$e(t) = 0$ for $t < 0$

$e(t) = V_{0+} \cdot t/t_r$ for $0 \le t \le t_r$

$e(t) = V_{0+}$ for $t > t_r$

and where t_r represents the 0-to-100% source rise time. The circuit model and its lattice diagram are shown in *Figure 20*. The values of R_S, R_0 and R_L were chosen to equal those of an actual circuit on hand, allowing the theoretical waveforms, obtained by graphical superposition, to be compared with the measured response of an actual circuit.

Figure 21 shows the load voltage v_L, source voltage v_S and source current i_S waveforms versus time for a circuit with a source rise time very much less than τ. The actual waveforms for v_L, v_S and i_S are composed of the superposition of both incident and reflected waves in their proper time sequence. In the figures, these waves are shown as dotted lines. Each wave represents the sum of the incident wave plus its reflection. The resultant v_L, v_S and i_S waveforms (shown as solid lines) are the superposition of the waves represented by the dotted lines. With the exception of a slight rounding of the edges, the actual waveforms for the circuit, shown in the oscilloscope photograph in *Figure 21*, closely approximate the waveforms predicted by theory.

Source					Load				
t in (τ)	$v_i + v_r$ (V)	$i_i + i_r$ (mA)	v_S (V)	i_S (mA)	t in (τ)	$v_i + v_r$ (V)	$i_i + i_r$ (mA)	v_L (V)	i_L (mA)
0	0.9400	12.53	0.9400	12.53	1	1.8500	0.40	1.8500	0.40
2	0.1224	−22.64	1.0624	−10.10	3	−1.5500	−0.34	0.3000	0.06
4	−0.1026	18.97	0.9599	8.87	5	1.2986	0.28	1.5986	0.35
6	0.0859	−15.90	1.0458	−7.03	7	− 1.0881	−0.24	0.5106	0.11
8	−0.0720	13.32	0.9738	6.29	9	0.9116	0.20	1.4222	0.31
10	0.0603	−11.17	1.0341	−4.87	11	−0.7638	−0.17	0.6584	0.14
12	−0.0505	9.36	0.9836	4.48	13	0.6399	0.14	1.2983	0.28
14	0.0424	−7.84	1.0259	−3.36	15	−0.5362	−0.12	0.7622	0.16
16	0.0355	6.57	0.9904	3.21	17	0.4492	0.10	1.2114	0.26

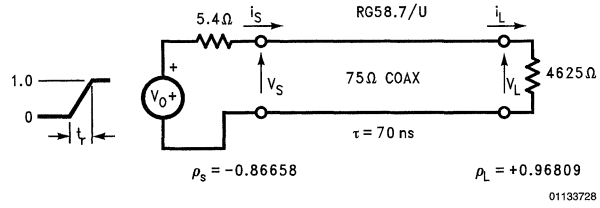
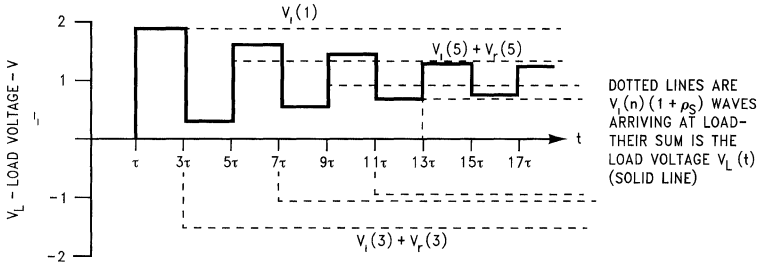
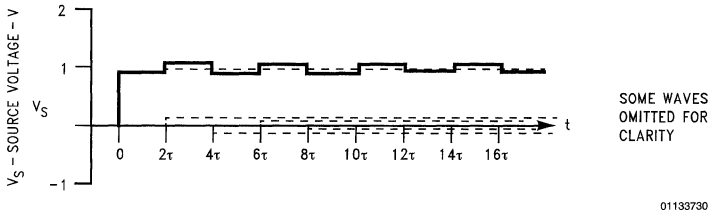
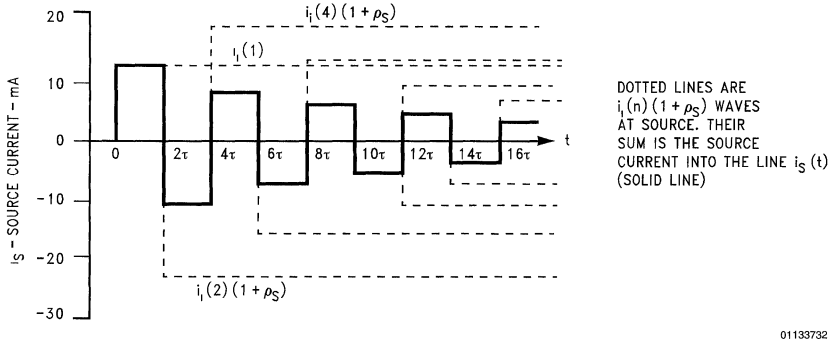


FIGURE 20. Transmission Line Model and Its Lattice Diagram

Effect of Source Rise Time on Waveforms (Continued)







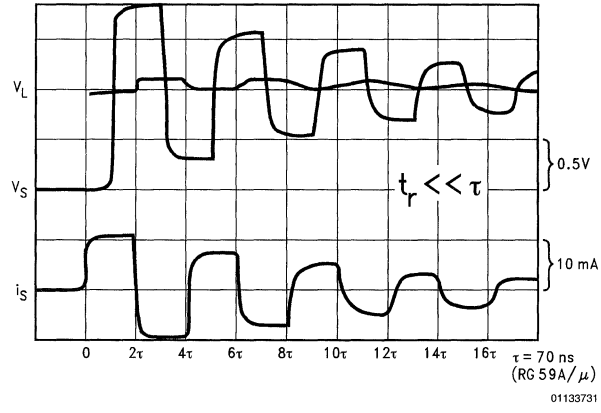


FIGURE 21. Waveforms for $t_r = 2 \ll \tau$

Effect of Source Rise Time on Waveforms (Continued)

If the source excitation is adjusted so that its 0-to-100% rise time t_r is equal to 2τ, each of the $v_i + v_r$ and $i_i + i_r$ waveforms must be modified to include this rise time. The waves will have the same final value as predicted by the lattice diagram, but they now require two line time delays to reach this final value. The v_L, v_S and i_S waveforms consist of the superposition of these linear ramps. Because each wave reaches its final value just as a new wave arrives, their superposition converts the square edged v_L, v_S and i_S waveforms into triangular waveforms. This is shown in *Figure 22*. The accompanying oscilloscope plot shows the close correspondence between the actual and theoretical waveforms whereas an additional oscilloscope photograph in *Figure 22* shows the actual waveforms for the case where $t_r = \tau$. Not surprisingly, the $t_r = \tau$ case changes the v_L, v_S and i_S waveforms of the $t_r \ll \tau$ case into trapeziodal forms because each arriving wave reaches its final value well before a new wave arrives.

If the source excitation is adjusted such that its rise time equals three line delays $t_r = 3\tau$, the $v_i + v_r$ and $i_i + i_r$ waves overlap for a period of time equal to τ. That is, each wave reaches only ⅔ of its final value when a new wave starts arriving. Considering the waveform, the load voltage from time τ to 3τ is

$$v_i(1)\ (1 + \rho_L)\ e\ (t - \tau)$$

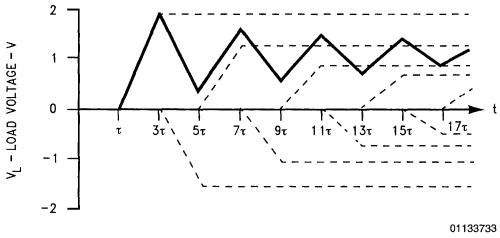
Starting at $t = 3\tau$, the wave

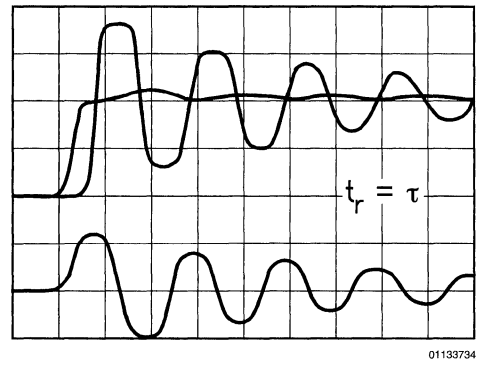
$$v_i(3) = v_i(1)\rho_S\rho_L\ e(t - 3\tau).$$

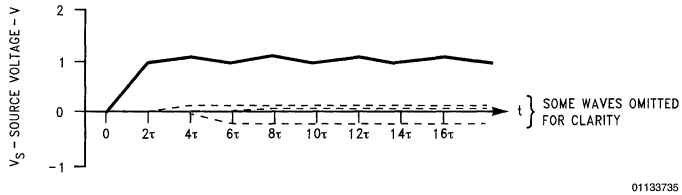
begins arriving from the source, and the load voltage then is the superposition of these two waves. Because $v_i(3)$ is a negative wave ($\rho_S < 0$), the algebraic sum of the last third of the first wave and the first third of the second wave $v_i(3)$ arriving at the load causes the load voltage to reduce in amplitude from the ($t_r \ll \tau$) case. Likewise, the source voltage and source current show reduced amplitudes over the ideal case, due to the overlap period of the waves arriving at the source.

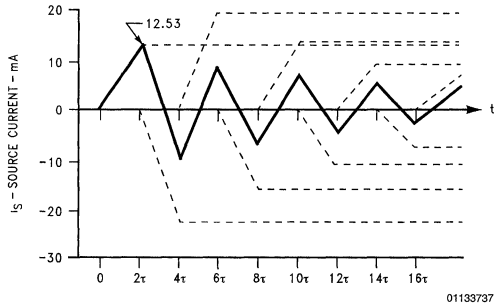
Theoretical and actual waveforms for the $t_r = 3\tau$ case are shown in *Figure 23*. Notice that load voltage perturbations and source current i_S requirements are reduced from those of the $t_r \ll \tau$ case. Similarly, the ratio of t_r to τ can be successively increased. This results in reduced ringing on the load voltage and reduced source current due to the overlapping of more and more $v_i + v_r$ (or $i_i + i_r$) waves. Actual and theoretical waveforms for t_r equal to 4τ, 6τ, and 8τ are shown in *Figure 24*, *Figure 25* and *Figure 26*, respectively. In each case, as the t_r to τ ratio is increased, the instantaneous source and load voltages become more equal. The source current is also reduced so that the circuit exhibits fewer reflection effects and the transmission line itself can be considered as a simple interconnection from dc circuit theory.

Effect of Source Rise Time on Waveforms (Continued)









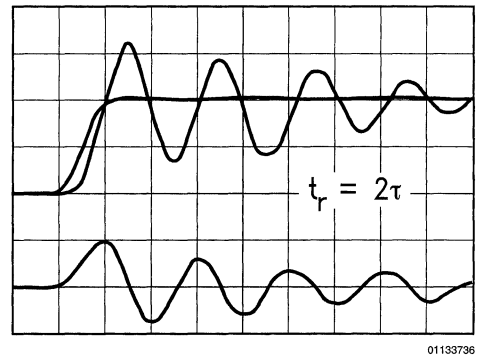
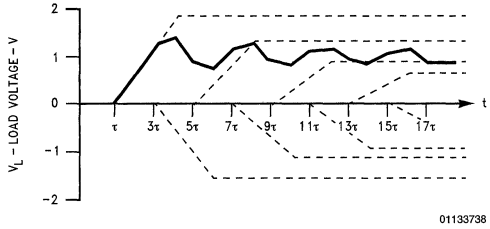


FIGURE 22. Waveforms for $t_r = 2\tau$

Effect of Source Rise Time on Waveforms (Continued)



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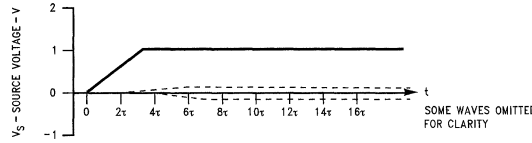

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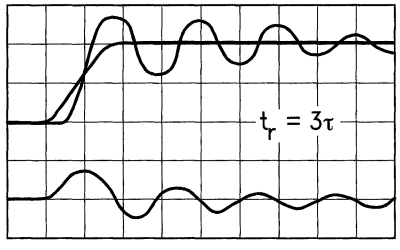

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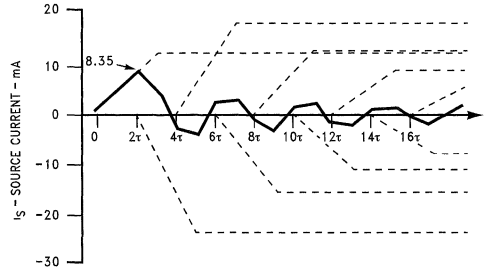

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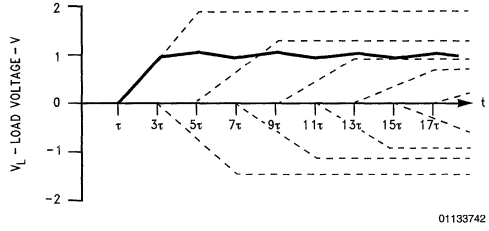
FIGURE 23. Waveforms for $t_r = 3\tau$



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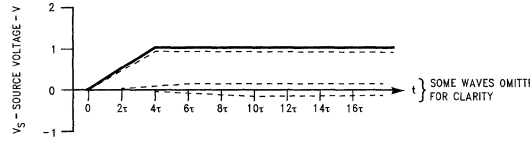

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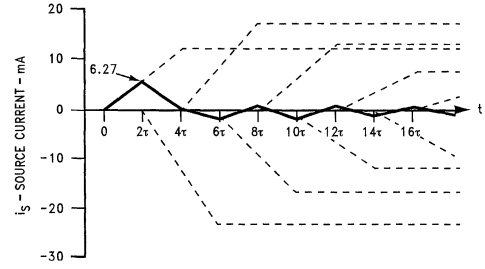

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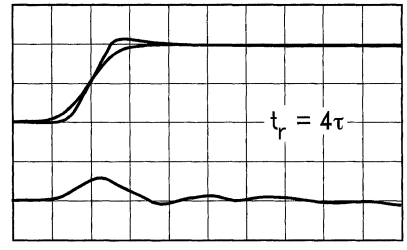

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FIGURE 24. Waveforms for $t_r = 4\tau$

Effect of Source Rise Time on Waveforms (Continued)

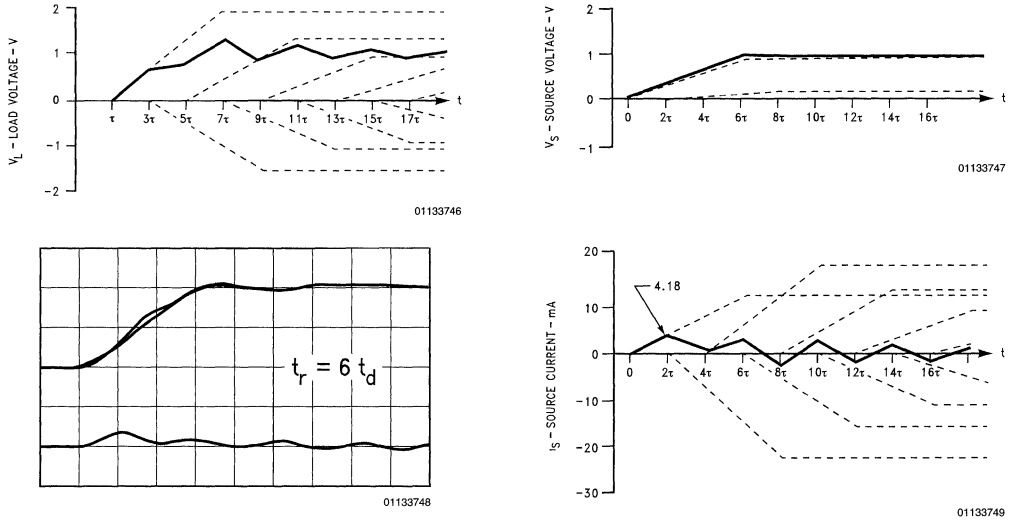


FIGURE 25. Waveforms for $t_r = 6\tau$

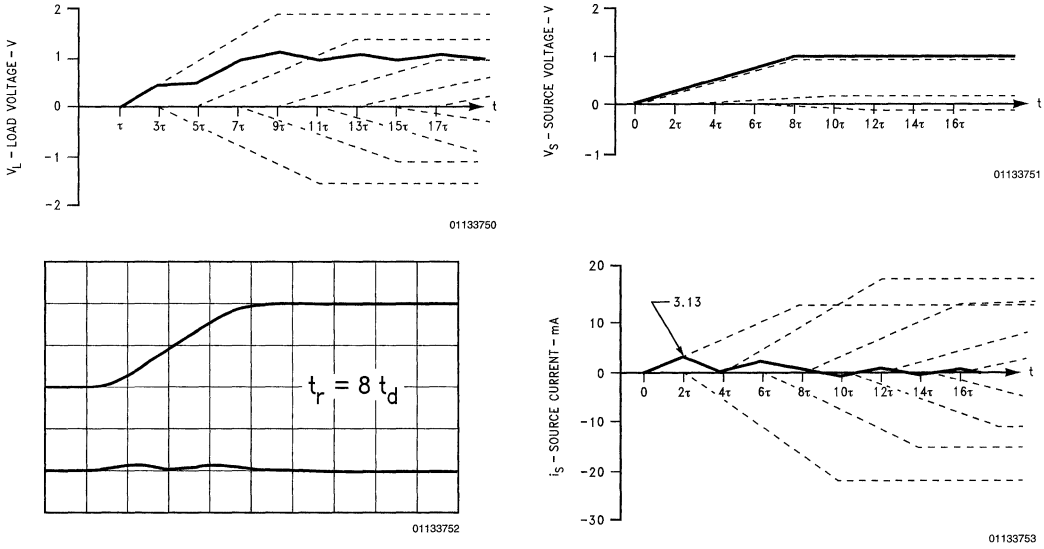


FIGURE 26. Waveforms for $t_r = 8\tau$

Using the t_r to τ ratio to reduce reflection effects has many practical advantages in digital design. The low source and high input resistance of TTL or ECL circuits allows one gate to drive many receiving gates. The reflection effects of this unterminated combination, however, can cause data errors or at least lead to reduced noise immunity due to the pronounced load voltage undershoot. Since the rise and fall times of these devices are easily measured, a maximum line length can be set such that the resulting t_r to τ ratio provides the desired reduction in ringing. This is the primary basis for the wiring rules of each logic family and, usually, the t_r to τ ratio is chosen somewhere between 3:1 and 4:1. As an example, the rise and fall time for normal TTL is $t_{10\%-90\%}$ = 6 ns. When this is converted to an equivalent linear 0% to 100% time, t_r = 8 ns. A common propagation delay of 1.7 ns/ft, in combination with the requirement that $t_r = 3\tau$, gives the maximum line length of approximately 18 inches. This corresponds with the published recommenda-

Effect of Source Rise Time on Waveforms (Continued)

tion of the various manufacturers for the 74 series TTL circuits. A similar computation of the rise and fall times for other logic families yields their respective line length recommendations. The faster families require shorter line lengths for the same t_r to τ ratio, and slower logic families allow relatively longer line length. This ratio can also be used to make stubs or taps on lines "disappear". In other words, if the stub's time delay is made very short when compared to the t_r of the signal at the stub line location, the stub reflections will have a minimal effect on the line signals. A stub length to generate a t_r to τ ratio of greater than 8:1 is usually considered adequate to negate the stub reflections.

The third primary application of the t_r to τ ratio for controlling reflection effects is that used in some standard data communications interfaces such as EIA/TIA-232-E (RS-232). Here, driver slew rate is explicitly controlled. This, along with the implied maximum interconnect cable length serves to produce a t_r to τ ratio of 3:1 or greater. This, in turn, reduces the reflection effects inherent in a voltage source driver, unterminated line system. The main disadvantage of using the t_r to τ ratio to control reflection effects is in the overall time for the signal representing the data to rise above the receiver threshold level. With the parallel terminated method, the minimum time delay was τ or one line delay. When the t_r to τ ratio is used, an additional delay time of approximately 0.5 t_r is added to the line delay yielding, therefore, a greater effective signal propagation delay. This increased delay may or may not be acceptable in the desired system so the trade-off between ease of usage of the unterminated case must be weighed against the increased effective signal delay over that delay obtainable with the terminated case.

Long Transmission Lines and Data Signal Quality

National Semiconductor
Application Note 808
Kenneth M. True

Overview

This application note explores another important transmission line characteristic, the reflection coefficient. This concept is combined with the material in AN-806 to present graphical and analytical methods for determining the voltages and currents at any point on a line with respect to distance and time. The effects of various source resistances and line termination methods on the transmitted signal are also discussed This application note is a revised reprint of section four of the Fairchild Line Driver and Receiver Handbook. This application note, the third of a three part series (See AN-806 and AN-807), covers the following topics:

- Factors Causing Signal Wave-Shape Changes
- Influence of Loss Effects on Primary Line Parameters
- Variations in Z_0, $\alpha(\omega)$ and Propagation Velocity
- Signal Quality—Terms
- Signal Quality Measurement—The Eye Pattern
- Other Pulse Codes and Signal Quality

Introduction

Transmission lines as discussed in AN-806 and AN-807 have always been treated as ideal lossless lines. As a consequence of this simplified model, the signals passing along the lines did not change in shape, but were only delayed in time. This time delay is given as the product of per-unit-length delay and line length ($\tau = \ell\delta$). Unfortunately, real transmission lines always possess some finite resistance per unit length due to the resistance of the conductors composing the line. So, the lossless model only represents *short* lines where this resistance term can be neglected. In AN-806 the per-unit-length line parameters, L, R, C, G, were assumed to be both constant and independent of frequency (up to the limits mentioned, of course). But with real lines, this is not strictly correct as four effects alter the per-unit-length parameters, making some of them frequency dependent. These four effects are skin effect, proximity effect, radiation loss effect, and dielectric loss effect. These effects and how they influence the intrinsic line parameters are discussed later in this application note Since these effects make simple ac analysis virtually impossible, operational (Laplace) calculus is usually applied to various simplified line models to provide somewhat constrained analytical solutions to line voltages and currents. These analytical solutions are difficult to derive, perhaps even more difficult ot evaluate, and their accuracy of prediction depends greatly on line model accuracy Analytical solutions for various lines (primarily coaxial cables) appear in the references, so only the salient results are examined here.

Engineers designing data transmission circuits are not usually interested in the esoterica of lossy transmission line theory. Instead, they are concerned with the following question: given a line length of x feet and a data rate of n bps, does the system work—and if so—what amount of transition jitter is expected? To answer this question using analytical methods is quite difficult because evaluation of the expressions representing the line voltage or current as a function of position and time is an involved process. The references at the end of this application note provide a starting point to generate and evalute analytical expressions for a given cable

The effects on the LRCG line parameters, the variations in Z_0, $\alpha(\omega)$, and propagation velocity as a function of applied frequency are discussed later in this application note. Using an empirical approach to answer the "how far—how fast" question involves only easily made laboratory measurements on that selected cable. This empirical approach, using the binary eye pattern as the primary measurement tool, enables the construction of a graph showing the line length/data rate/signal quality trade-offs for a particular cable. The terms describing *signal quality* are discussed later in this application note. The technique of using actual measurements from cables rather than theoretical predictions is not as subject to error as the analytical approach. The only difficulties in the empirical method are the requirements for a high quality, real time (or random sampling) oscilloscope and, of course, the requisite amount of transmission line to be tested.

Also discussed in this application note are commonly used pulse codes.

Factors Causing Signal Wave Shape Changes

In AN-806 and AN-807, it was assumed that the transmission lines were ideal so the step functions propagated along the lines without any change in wave shape. Because a single pulse is actually composed of a continuous (Fourier) spectrum, the phase velocity independence on an applied frequency, and the absence of attenuation (R = 0, G = 0) of the ideal line always allows the linear addition of these frequency components to reconstruct the original signal without alteration. For real lines, unfortunately, the series resistance is not quite zero, and the phase velocity is slightly dependent on the applied frequency. The latter results in *dispersion, i.e.*, the propagation velocity will differ for the various frequencies, while the former results in signal *attenuation* (reduction in amplitude). This attenuation may also be a function of frequency. Attenuation and dispersion cause the frequency components of a signal, at some point down the line, to be quite different from the frequency components of the signal applied to the input of the line. Thus, at some point down the line, the frequency components add together to produce a wave shape that may differ significantly from the input signal wave shape. In many ways, then, a real transmission line may be thought of as a distributed lowpass filter with loss. The fast rise and fall times of the signals become progressively "rounded" due to attenuation and dispersion of the high frequency signal components.

It should be noted that there is a theoretical condition where attenuation is independent of frequency and dispersion is zero. This results in a line causing signal amplitude reduction, but no change in signal wave shape. This condition was first discussed by Heavyside and is called the *distortionless* line. To make a line distortionless, the primary line parameters must satisfy the relation (R/L) = (G/C). Because for real lines (R/L) > (G/C), the distortionless line is only of historical

Factors Causing Signal Wave Shape Changes (Continued)

interest, and it is not possible to satisfy the (R/L) = (G/C) condition over a sufficiently wide bandwidth to allow a proper transmission of short duration pulses. Over a limited frequency range such as that encountered in telephony (0 kHz–4 kHz), the L term can be increased by either adding lumped inductances at fixed intervals along the line or by winding a magnetic material (as a thin tape) around the conductors of the line throughout its length. Lumped loading is commonly applied to long telephone circuits to reduce the signal attenuation over a narrow frequency range; however this linearity is at the expense of in-band attenuation and non-linear delay distortion. The distributed loading method has been tried, but the mechanical characteristics of the magnetic materials have made the winding process very difficult. In any event, neither method allows short pulses to retain their wave shapes. The interest in line loading to produce the Heavyside condition for pulse transmission is therefore largely academic.

The following sections discuss the origins of the second-order effects—skin effect, proximity effect, radiation loss effect, and dielectric loss effect—and their influence on the LRCG transmission line parameters.

- Skin Effect: The phenomenon is based on two facts: a current flow in any real conductor produces an electric field given by Ohm's Law; the current distribution and/or magnetic field distribution in a conductor is frequency dependent. For dc current in a single isolated conductor, the current density is uniform across the conductor. When alternating current is used, the current density is not uniform across the conductor. Instead, the current tends to concentrate on the conductor surface. Current density continuously increases from the conductor center to its surface, but for practical purposes, the current *penetration depth*, d, is assumed as a dividing line for current density. The current is assumed to flow in a imaginary cylinder of thickness d with a constant current density throughout the cylinder thickness. Distribution of current densities for both actual and assumed models is shown in *Figure 1.*

  It can be seen that for *classical* skin effects, the penetration depth is given by

$$d = K\frac{1}{\sqrt{f}} \qquad (1)$$

  where

$$K = 1/\sqrt{\pi\mu\sigma},$$

  μ = magnetic permeability of the conducting material expressed in henries per unit length, and Σ = conductivity of the conducting material. For MKS (SI) units and for a copper conductor

$$\Sigma = 5.85 \times 10^{7} (\Omega \text{ meter})^{-1}$$

$$\mu = 4\pi \times 10^{-7} \text{ (H/meter)}$$

  in which case, d would be the penetration depth expressed in meters.

  Because the skin effect reduces the equivalent conductor cross-sectional area, increasing frequencies cause an increase in the effective resistance per unit length of the line. This in turn leads to signal attenuation increasing with frequency. If the frequency response of a cable is plotted on log-log graph paper, log dB, or Nepers vs log frequency, the curve slope will be 0.5 if the cable losses are primarily governed by *classical* skin effects. The slope of the attenuation curve, along with the attenuation at a particular frequency, can be used to estimate coaxial cable transient response as a function of length.[2, 4]

Note: *See Reference 2 and 4

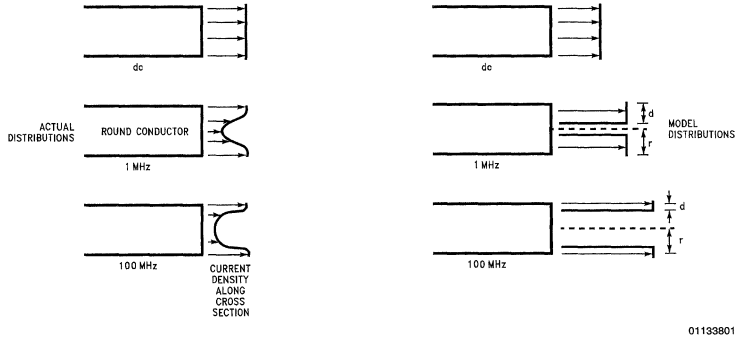


FIGURE 1. Current Distributions Across and Conductor for Several Frequencies

Factors Causing Signal Wave Shape Changes (Continued)

- Proximity Effect: This is a current density redistribution in a conductor due to the mutual repulsion (or attraction) generated by currents flowing in nearby conductors. The current density at those points on the conductor close to neighboring conductors varies from the current density when the conductor is isolated from other conductors. This current density redistribution reduces the effective cross-sectional area of the conductor, thereby increasing the per-unit-length line resistance. This effect is a function of the conductor diameters, the separation of the conductors from each other, and frequency. The analytical evaluation of the proximity effect is quite complicated and except for certain limited cases*, no general rule of thumb expressions have been proposed. The proximity effect is not present in coaxial cables because of their circular symmetry. The proximity effect is a significant contributor to signal losses particularly in cases of a twisted pair or parallel wire lines.
- Radiation Loss: Radiation losses cause an apparent rise in resistance per unit length increasing with frequency. The mechanism of radiation loss is energy dissipation either as heat or magnetization via eddy currents in nearby metallic or magnetic masses, with the eddy currents induced by line currents. Coaxial cables do not exhibit this effect because the signal magnetic field is confined between the shield and the outside of the center conductor. Ideally, the magnetic field produced by shield current cancels the field produced by current in the center conductor (for points outside the shield).

  Both twisted pair and parallel wire lines exhibit radiation losses and these losses contribute to the effective per-unit-length line resistance. Radiation loss is dependent to a large extent on the characteristics of the materials close to the line; so radiation loss is quite difficult to calculate, but can be measured if necessary.
- Dielectric Loss Effect: Dielectric losses result from leakage currents through the dielectric material. This causes an increase in the shunt conductance per unit length and produces signal attenuation. Fortunately, for most dielectric materials in common use, this loss is very small particularly for frequencies below 250 MHz. For most practical purposes, then, dielectric losses may be neglected as they are usually overshadowed by skin effect losses.

Influence of Loss Effects on Primary Line Parameters

Resistance Per Unit Length, R. It is composed of a basic dc resistance term R_{dc} plus the contributions of skin effect, proximity effect and radiation loss effect. For coaxial lines, the proximity and radiation loss effects are negligible in most cases, so the primary contribution is made by the skin effect. Thus the resistance per unit length becomes

$$R = R_{dc} + Ks^m \qquad (2)$$

where $0 < m < 1$.

Note: *See References Arnold[11] and Dwight[12] **See References 5 and 6

For 2-wire lines (twisted pair, parallel wire), the resistance per unit length is increased by the skin effect. For closely spaced wires, however, the proximity effect also contributes significantly to a resistance increase. Radiation loss should also be included, but is very difficult to calculate because it depends on the surroundings of the line.

Inductance Per Unit Length, L. It can be shown** that, as the frequency is increased, the skin effect, proximity effect, and radiation loss effect cause a reduction in the effective per-unit-length self-inductance of the line.

Capacitance Per Unit Length, C. This depends primarily on the dielectric constant of the insulating medium and conductor geometry. This term is constant over a wide range of frequencies for most dielectrics (Teflon®, Polyethylene). For Polyvinylchloride (PVC) insulation, the relative dielectric constant shows a decrease as frequency increases ($\epsilon_r \approx 4.7$ @ 1 kHz, $\epsilon_r \approx 2.9$ @ 100 MHz). The capacitance per unit length, therefore, will show a decrease corresponding with increasing frequency for PVC insulation and little change for most other dielectrics.

Conductance Per Unit Length, G. Because resistance per unit length usually has a much greater magnitude, this value is negligible. When this term cannot be neglected, it is represented as

$$G = \omega C \tan\phi \qquad (3)$$

where C is capacitance per unit length, ω is the angular frequency ($= 2\pi f$) and $\tan\phi$ is a dielectric material coefficient. The angle ϕ is called the dielectric loss angle. This angle is usually quite small (< 0.005 radians) for the majority of dielectrics up to several hundred megahertz.

Variations in Z_0, $\alpha(\omega)$, and Propagation Velocity

The variations in the primary line parameters as a function of frequency shown by *Figure 2* have a profound influence on the three secondary line parameters of characteristic impedance, attenuation, and velocity of propagation.

In the expression for the characteristic impedance of a line,

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

at low frequencies, $j\omega L$ is small compared to R, and G is small compared to $j\omega C$. So the characteristic impedance is

$$\sqrt{R/j\omega C}.$$

At high frequencies, the increase in R is overshadowed by $j\omega L$ even though L is being reduced. With G still much smaller than $j\omega C$, the characteristic impedance is almost a pure resistance

$$R_0 = \sqrt{L/C}.$$

Variations in Z_0, $\alpha(\omega)$, and Propagation Velocity (Continued)

The behavior of the characteristic impedance as a function of frequency ($Z_0 = R_0 - jX_0$) is shown in *Figure 3.*

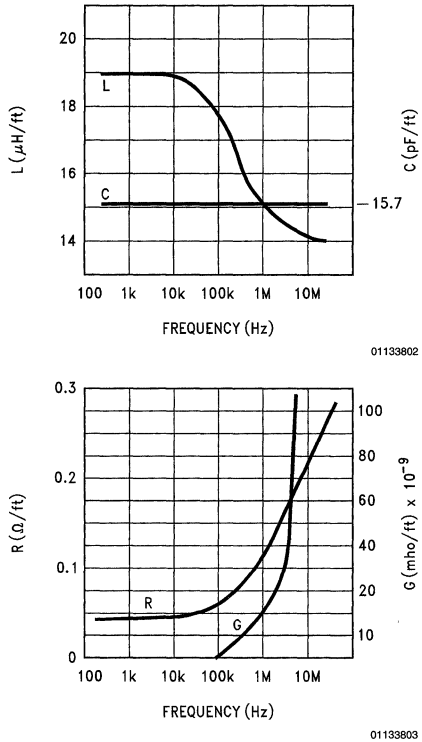


FIGURE 2. Variations in Primary Parameters as a Function of Frequency (22 AWG Polyethylene Insulated Twisted Pair)

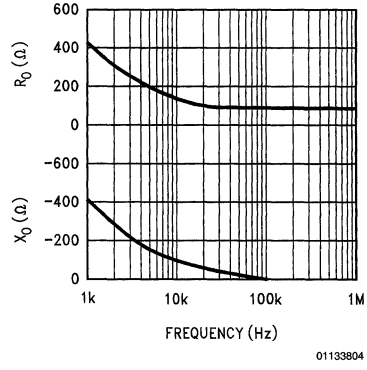


FIGURE 3. Typical Variation in Z_0 as a Function of Frequencies

Typical behavior of the line attenuation as a function of frequency is shown in *Figure 4.* This line attenuation is the real part of the equation

$$\gamma(\omega) = \sqrt{(R + j\omega L)(G + j\omega C)}.$$

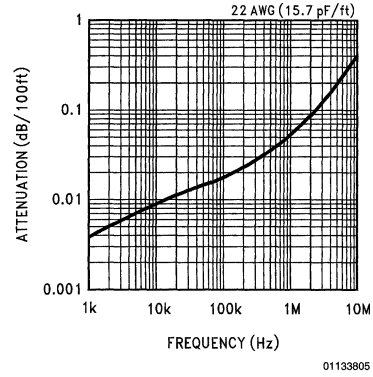


FIGURE 4. Attenuation vs Frequency

The change in resistance is the primary contributor to the attenuation increase as a function of frequency. For coaxial cables, this resistance increase is due primarily to the skin effect ($R_{SK} = Kf^m$). The slope of the attenuation curve on a log-log graph (log dB vs log frequency), therefore, is essentially linear and, at the same time, equal to m. For twisted pair and parallel wire lines, proximity effects and radiation losses make the curves less linear, but for high frequencies (over 100 kHz), the attenuation expressed in nepers per unit length is approximated by

$$\alpha \cong \frac{R}{2}\sqrt{\frac{C}{L}} \qquad (4)$$

The R term is, of course, the sum of the dc resistance, plus the incremental resistance due to skin, proximity and radiation loss effects. This R term usually varies as follows.

$$R_{SK} = Kf^m$$

where $0.6 \leq m < 1.0$

The signal velocity propagation ($v = \omega/\beta$) is given by the imaginary part of the propagation constant γ. As shown in AN-807, v is a constant given by

$$v = \sqrt{LC}$$

for lossless lines. For real lines, this value is approached at high frequencies. At low frequencies, however, (when ω is small compared to R/L or G/C), then

$$v_{LF} \cong (C/2)\sqrt{R/G}$$

and the velocity is reduced. The propagation velocity as a function of frequency is shown in *Figure 5.* This variation in signal velocity as a function of signal frequency is *dispersion* which was previously discussed.

Variations in Z_0, $\alpha(\omega)$, and Propagation Velocity (Continued)

The signal at a point down the line represents the sum of that original signal's Fourier spectrum. Because both the attenuation and propagation velocity of these Fourier components increase with frequency, the resultant signal shape at that point down the line depends greatly on the winners of the race to get to that point. The high frequency components, with their faster propagation velocities, arrive first, but the increased attenuation minimizes their effect. The low frequency signals arrive later, but the reduced attenuation allows them a greater influence on the resultant signal. In general, the output signal from the line should show a relatively fast rise up to some signal value (20% to 50% of the final value). This is due to arrival of the high frequency components, followed by a more leisurely rise to the final value as the slower, low frequency components arrive.

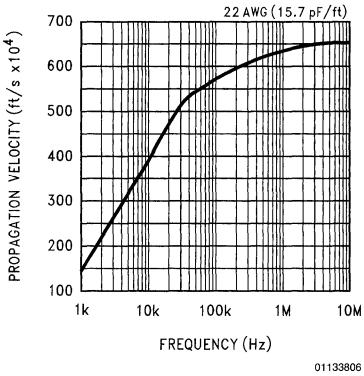


FIGURE 5. Propagation Velocity vs Frequency

Signal Quality—Terms

Before the concepts presented in the previous sections can be used to answer the "how far—how fast" question, some familiarity with the terms describing data and signal quality is necessary.

The primary objective of data transmission is the transfer of *information* from one location to another. The information here is *digital* in nature; i.e., a finite number of separate states or choices. This is in contrast to *analog* which has an infinite number of separate states or a continuous range of choices. The digital information is *binary* or two-valued; thus two different, recognizable electrical states/levels are used to symbolize the digital information. A binary symbol is commonly called a binary-digit or *bit*. A single binary symbol or bit, by itself, can represent only one of two possible things. To represent alphabetic or numeric characters, a group of bits is arranged to provide the necessary number of unique combinations. This arrangement of bits which is then considered an information unit is called a *byte*. In the same manner that a group of bits can be called a byte, a collection of bytes, considered as a unit, is called a *word*. Selective arrangement of seven bits will provide 2^7 (or 128) distinct character combinations (unique bytes). The American Standard Code for Information Interchange (ASCII) is an excellent example of just such an arrangement—upper and lower case alphabetic, zero to nine numeric, punctuation marks, and miscellaneous information-code control functions.

Now with the means for representing information as bits or bytes, and the means for transmission of the bits (symbols) from one location to another (transmission line), the remaining task is to ensure that a particular bit arriving at its destination is interpreted in the proper context. To achieve this, both the sender and receiver of the data must accomplish the five following requirements.

1. Agree upon the nominal rate of transmission; or how many bits are to be emitted per second by the sender.
2. Agree upon a specified information code providing a one-to-one mapping ratio of information-to-bit pattern and vice versa.
3. Establish a particular scheme whereby each bit can be properly positioned within a byte by the receiver of the data (assuming that bit-serial transmission is used).
4. Define the protocol (handshaking) sequences necessary to ensure an orderly flow of information.
5. Agree to the electrical states representing the logic values of each bit and the particular pulse code to be used.

These are by no means all of the points that must be agreed upon by sender and receiver—but these are probably the most important. Items 2, 3 and 4 are more or less "software" type decisions, because the actual signal flow along the transmission line is usually independent of these decisions. Because items 1 and 5 are much more dependent on the characteristics of line drivers, line receivers, and transmission lines, they are the primary concern here.

Figure 6 represents the components of a typical data transmission system. The *information source* can be a computer terminal or a digitized transducer output, or any device emitting a stream of bits at the rate of one bit every t_B seconds. This establishes the *information rate* of the system at $1/t_B$ bits per second. The information source in the figure feeds a *source encoder* which performs logic operations not only on the data, but also on the associated clock and, perhaps, the past data bits. Thus, the source encoder produces a binary data stream controlling the *line driver*. The line driver interfaces the source internal logic levels (TTL, CMOS, etc.) with transmission line current/voltage requirements. The transmission line conveys signals produced by the line driver to the line receiver. The line receiver makes a decision on the signal logic state by comparing the received signal to a decision threshold level, and the *sink decoder* performs logic operations on the binary bit stream recovered by the line receiver. For example, the sink decoder may extract the clock rate from the data or perhaps detect and correct errors in the data. From the optional sink decoder, the recovered binary data passes to the *information sink*—the destination for the information source data.

Assume for the moment that the source encoder and sink decoder are "transparent"; that is, they will not modify the binary data presented to them in any way. Line driver signals, then, have the same timing as the original bit stream. The data source emits a new bit every t_B seconds. The *pulse code* produced by the source encoder and line driver is called Non-Return to Zero (NRZ), a very common signal in TTL logic systems. A sample bit pattern with its NRZ repre-

Signal Quality—Terms (Continued)

sentation is shown in *Figure 7*. The arrows at the top represent the *ideal instants*, or the times the signal can change state. The term *unit interval* is used to express the time duration of the shortest signaling element. The shortest signaling element for NRZ data is one bit time t_B, so the unit interval for NRZ data is also t_B. The rate at which the signal changes is the *modulation rate* (or signaling speed), and *baud* is the unit of modulation rate. A modulation rate of one baud corresponds to the transmission of one unit interval per second. Thus the modulation rate, in baud, is just the reciprocal of the time for one unit interval. A unit interval of 20 ms, therefore, means the signaling speed is 50 baud. The reason for differentiating between the *information rate* in bits per second (bps) and the *modulation rate* in baud will be clarified after examining some of the other pulse codes later in this application note.

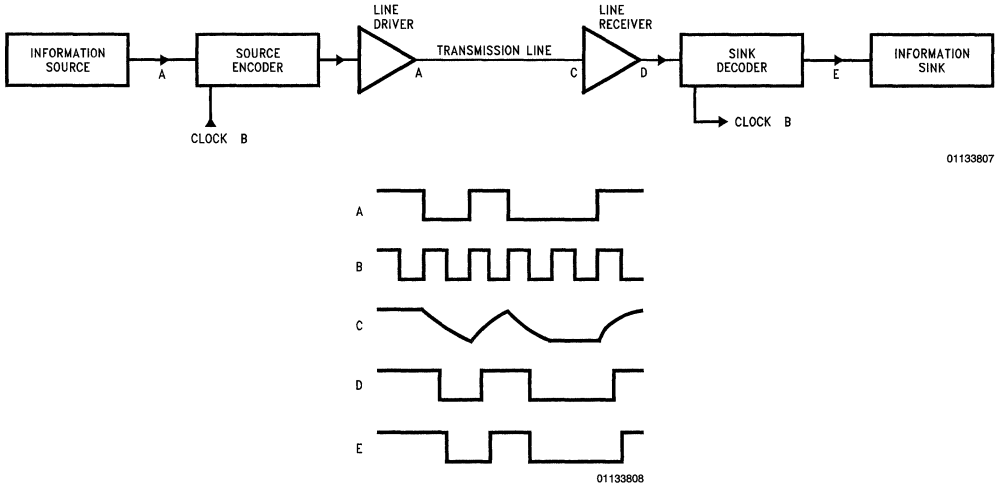


FIGURE 6. Data Transmission System

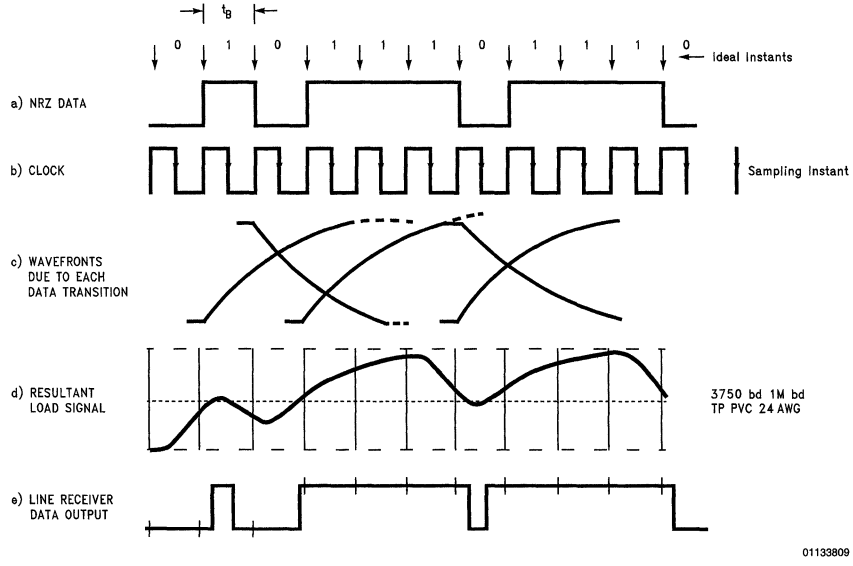


FIGURE 7. NRZ Signaling

Signal Quality—Terms (Continued)

NRZ data should always be accompanied by a clock signal, *Figure 7*, which tells the receiver when to sample the data signal and thus determine the current logic state. For the example in *Figure 7*, the falling edge of the clock corresponds to the middle of the data bits, so it could be used to transfer the line receiver data output into a binary latch. The falling edge of the clock is thus the *sampling instant* for the data. The line receiver does have a *decision threshold* or slicing point so that voltages above that threshold level produce one logic state output, while voltages below the threshold produce the other logic state at the receiver output. The receiver may incorporate positive feedback to produce *hysteresis* in its transfer function. This reduces the possibility of oscillation in response to slow rise or fall time signals applied to the receiver inputs.

Previously in this application note, it was stated that the fast rise and fall times of signals, corresponding to the transisions between data bits, are rounded out and slowed down by a real transmission line. Each transition of the signal applied to the line by the line driver is transformed to a rounded out transition by the dispersion and attenuation of the transmission line. The resultant signal at the load end of the line consists of the superposition of these transformed transitions. The waves arriving at the load end of the line are shown in *Figure 7* and their superposition is shown in *Figure 7*. It is assumed that the line is terminated in its characteristic resistance so that reflections are not present. The receiver threshold level is shown here, superimposed on the resultant load signal, and the re-converted data output of the line receiver is shown in *Figure 7* along with the ideal instants for the data transitions (tick marks).

Comparing the original data (*Figure 7*) to the recovered data (*Figure 7*) shows that the actual recovered data transitions may be displaced from their ideal instants (tic marks on *Figure 7*). This time displacement of the transitions is due to a new wave arriving at the receiver site before the previous wave has reached its final value. Since the wave representing a previous data bit is *interfering* with the wave representing the present data bit, this phenomenon is called *intersymbol interference* (in telegraphy it is called *characteristic distortion*). The intersymbol interference can be reduced to zero by making the unit interval of the data signal quite long in comparison to the rise/fall time of the signal at the receiver site. This can be accomplished by either reducing the modulation rate for a given line length, or by reducing the line length for a given modulation rate.

Signal quality is concerned with the variance between the ideal instants of the original data signal and the actual transition times for the recovered data signal.

For synchronous signaling, such as NRZ data, the *isochronous distortion* of the recovered data is the ratio of the unit interval to the maximum measured difference irrespective of sign between the actual and theoretical significant instants. The isochronous distortion is, then, the peak-to-peak time jitter of the data signal expressed as a percentage of the unit interval. A 25% isochronous distortion means that the peak-to-peak time jitter of the transition is 0.25 unit interval (max).

Another type of received-signal time distortion can occur if the decision threshold point is misplaced from its optimum value. If the receiver threshold is shifted up toward the *One signal level*, then the time duration of the One bits shortens with respect to the duration of the *Zero bits*, and vice versa. This is called *bias distortion* in telegraphy and can be due to receiver threshold offset (bias) and/or asymmetrical output levels of the driver. These effects are shown in *Figure 8*.

Bias distortion and characteristic distortion (intersymbol interference) together are called systemic distortion, because their magnitudes are determined by characteristics within the data transmission system. Another variety of time distortion is called *fortuitous distortion* and is due to factors outside the data transmission system such as noise and crosstalk, which may occur randomly with respect to the signal timing.

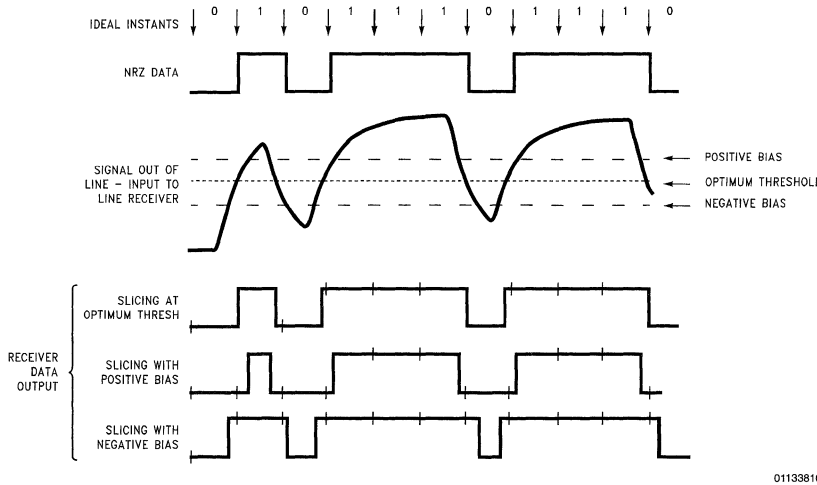


FIGURE 8. Bias Distortion

Signal Quality Measurement—The Eye Pattern

To examine the relative effects of intersymbol interference on random NRZ data and a "dotting"* pattern, see *Figure 9.* The top two waveforms represent the NRZ data and dotting pattern as outputs into two identical long transmission lines. The middle two traces illustrate the resultant signals at the line outputs and the bottom two traces show the data output of the line receivers. The respective thresholds are shown as dotted lines on the middle two traces. The arrows indicate the ideal instants for both data and dotting signals.

Notice that the dotting signal (D) is symmetrical, i.e., every One is preceded by a Zero and vice versa, while the NRZ data is random. The resultant dotting signal out of the line is also symmetrical. Because, in this case, the dotting halfcycle time is less than the rise/fall time of the line, the resultant signal out of the line (E) is a *partial response* —it never reaches its final level before changing. The dotting signal, due to its symmetry, does not show intersymbol interference in the same way that a random NRZ signal does. The intersymbol interference in the dotting signal shows up as a uniform displacement of the transitions as shown in *Figure 9.*

The NRZ data shows intersymbol interference, in its worst light, due to its unpredictable bit sequence. Thus, whenever feasibility of a data transmission system is to be tested, a random data sequence should be used. This is because a symmetrical dotting pattern or clock signal cannot always show the effects of possible intersymbol interference.

Note: *The term dotting pattern is from telegraphy and means an alternating sequence of 1 bits and 0 bits (the "dot dot dot" etc). Note that an NRZ dotting pattern generates a signal which has a 50% duty cycle and a frequency of $\frac{1}{2}\ t_B$ (Hz)

A very effective method of measuring time distortion through a data transmission system is based on the eye pattern. The eye pattern, displayed on an oscilloscope, is simply the superposition—over one unit interval—of all the Zero-to-One and One-to-Zero transitions, each preceded and followed by various combinations of One and Zero, and also constant One and Zero levels. The name *eye pattern* comes from the resemblance of the open pattern center to an eye. The diagramatic construction of an eye pattern is shown in *Figure 10.* The data sequence can be generated by a pseudo-random sequence generator (PRSG), which is a digital shift register with feedback connected to produce a maximum length sequence.

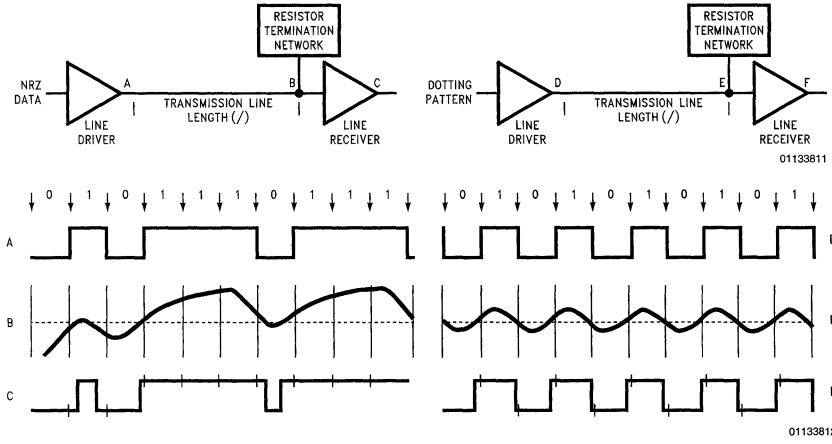


FIGURE 9. Comparison of NRZ Random Data and "Dotting" Signals

Signal Quality Measurement—The Eye Pattern (Continued)

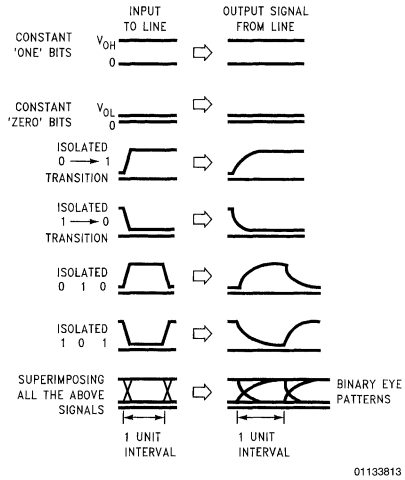
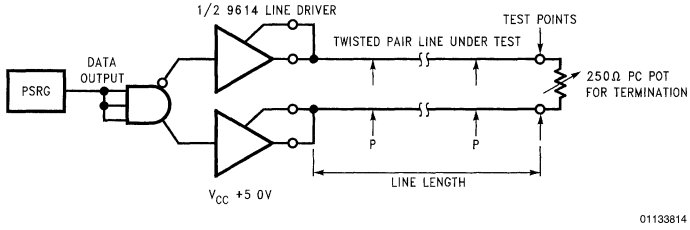


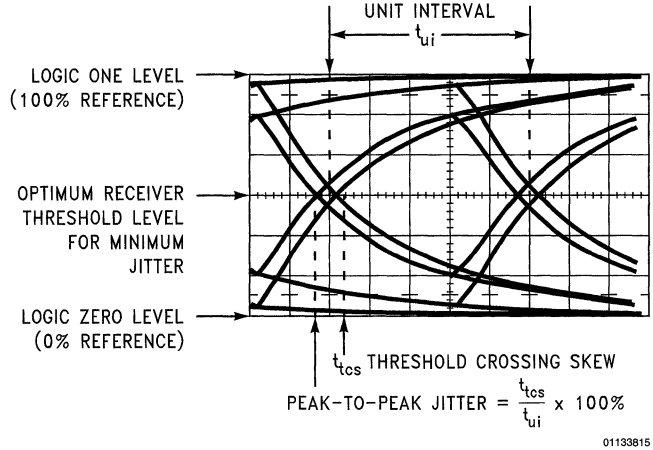
FIGURE 10. Formation of an Eye Pattern by Superposition



USE DIFFERENTIAL PROBE ACROSS TEST POINTS AND WIDE BANDWIDTH DIFFERENTIAL INPUT OSCILLOSCOPE TO DISPLAY EYE PATTERN

FIGURE 11. Bench Set-Up to Measure Data Signal Quality

Signal Quality Measurement—The Eye Pattern (Continued)



2100 ft—Terminated
24 AWG Twisted Pair
Cable—PVC Insulation

FIGURE 12. NRZ Data Eye Pattern

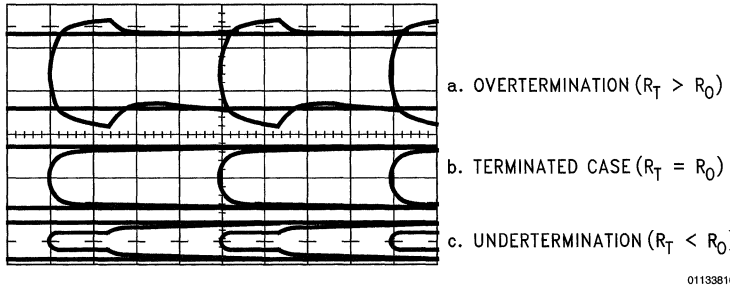


FIGURE 13. Using Eye Pattern to Determine Characteristic Resistance of Line

Several features of the eye pattern make it a useful tool for measuring data signal quality. *Figure 13* shows a typical binary eye pattern for NRZ data. The spread of traces crossing the receiver threshold level (dotted line) is a direct measure of the peak-to-peak transition jitter—isochronous distortion in a synchronous system—of the data signal. The rise and fall time of the signal can be conveniently measured by using the built-in 0% and 100% references produced by long strings of Zeros and Ones. The height of the trace above or below the receiver threshold level at the sampling instant is the noise margin of the system. If no clear transition-free space in the eye pattern exists, the eye is closed. This indicates that error-free data transmission is not possible at the data rate and line length with that particular transmission line without resorting to equalizing techniques. In some extreme cases, error-free data recovery may not be possible even when using equalizing techniques.

The eye pattern can also be used to find the characteristic resistance of a transmission line. The 250Ω printed circuit-type potentiometer termination resistor (*Figure 11*) can be adjusted to yield the minimum overshoot and undershoot of the data signal. *Figure 14* shows the NRZ data eye patterns for $R_T > R_O$, $R_T = R_O$ and $R_T < R_O$. The 100% and 0% reference levels are again provided by long strings of Ones and Zeros, and any overshoot or undershoot is easily discernible. The termination resistor is adjusted so that the eye pattern transitions exhibit the minimum perturbations (*Figure 13*). The resistor is then removed from the transmission line, and its measured value is the characteristic resistance of the line.

By using the eye pattern to measure signal quality at the load end of a given line, a graph can be constructed showing the tradeoffs in signal quality—peak-to-peak jitter—as a function of line length and modulation rate for a specific pulse code. An example graph for NRZ data is shown in *Figure 14*. The graph was constructed using eye pattern measurements on a 24 AWG twisted pair line (PVC insulation) driven by a differential voltage source driver (75114/9614) with the line parallel-terminated in its characteristic resistance (96Ω). The oscilloscope plots in *Figure 15* show the typical eye

Signal Quality Measurement—The Eye Pattern (Continued)

patterns for NRZ data with various amounts of isochronous distortion. The straight lines represent a "best fit" to the actual measurement points. Since the twisted pair line used was not specifically constructed for pulse service, the graph probably represents a reasonably good worst-case condition insofar as signal quality vs line length is concerned. Twisted pair lines with polyethylene or Teflon insulation have shown better performance at a given length than the polyvinyl chloride insulation. Likewise, larger conductors (20 AWG, 22 AWG) also provide better performance at a given length. Thus, the graph in *Figure 14* can be used to estimate feasibility of a data transmission system when the actual cable to be used is unavailable for measurement purposes. The arbitrary cutoff of 4000 feet on the graph was due to the observed signal amplitude loss of 6 dBV (½ voltage) of the 24 AWG line at that distance. The cutoff of 10 Mbaud is based on the propagation delays of the typical TTL line drivers and receivers. Field experience has shown that twisted pair transmission systems using TTL drivers and receivers have operated essentially error-free when the line length and modulation rate are kept to within the recommended operating region shown in *Figure 14*. This has not precluded operation outside this region for some systems, but these systems must be carefully designed with particular attention paid to defining the required characteristics of the line, the driver, and the receiver devices. The use of coaxial cable instead of twisted pair lines almost always yields better performance, i.e , greater modulation rate at a given line length and signal quality. This is because most coaxial cable has a wider bandwidth and reduced attenuation at a given length than twisted pair line (one notable exception is RG 174/U cable).

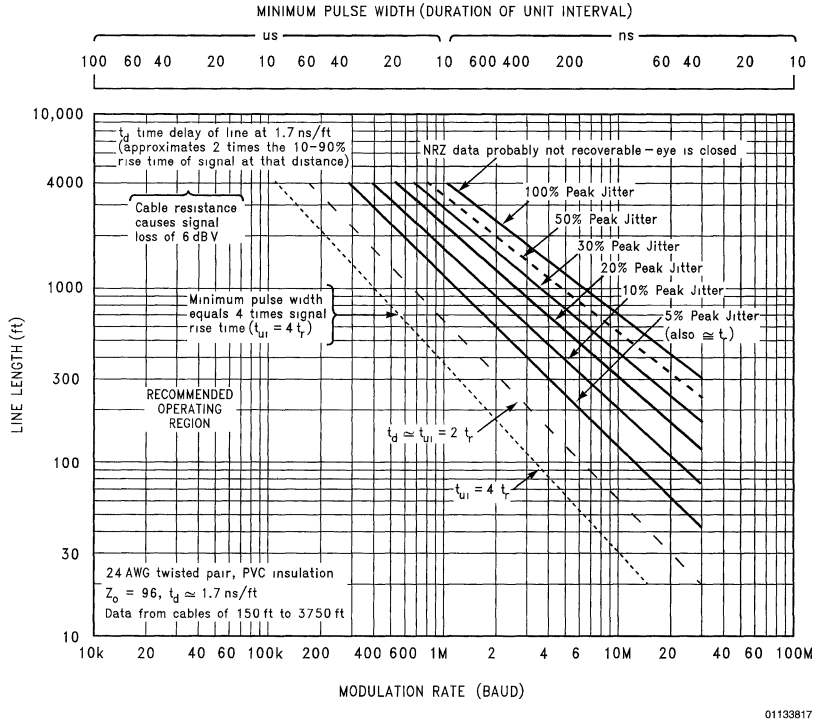


FIGURE 14. Signal Quality as a Function of Line Length and Modulation Rate for Terminated 24 AWG Twisted Pair (PVC Insulation)

7

Signal Quality Measurement—The Eye Pattern (Continued)

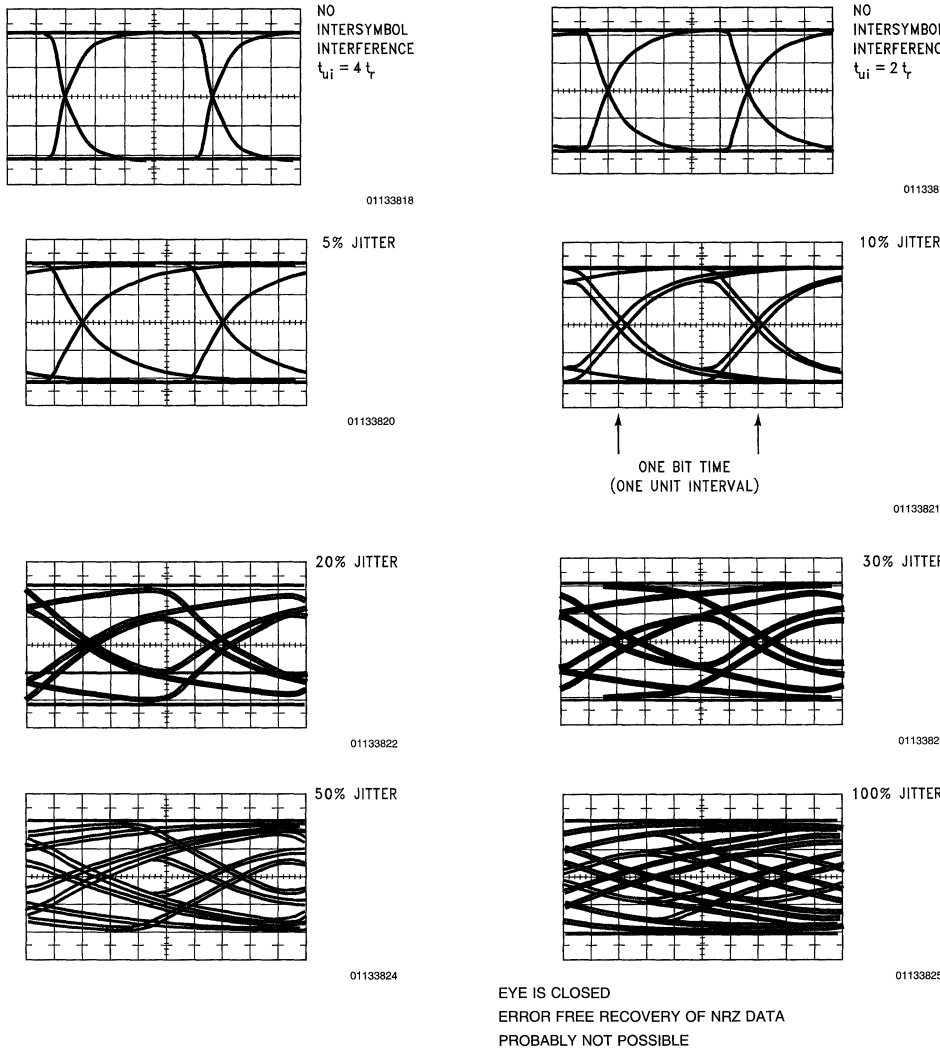


FIGURE 15. Eye Patterns for NRZ Data Corresponding to Various Peak-to-Peak Transition Jitter

It should be remembered that, in some ways, the eye pattern gives the *minimum* peak-to-peak transition jitter for a given line length, type, pulse code, and modulation rate. This is because the eye pattern transition spread is the result of intersymbol interference and reflection effects (if present) and this minimum jitter is only obtainable if the following conditions are met.

- The One and Zero signal levels produced by the line driver are symmetrical, and the line receiver's decision threshold (for NRZ signaling) is set to coincide with the mean of those two levels.
- The line is perfectly terminated in its characteristic resistance to prevent reflections from altering the signal threshold crossings.
- The time delays through driver and receiver devices for both logic states is symmetrical and there is no relative skew in the delays (difference between t_{plh} and t_{phl} propagation delays = 0). This is especially important when the device propagation delays become significant fractions of the unit interval for the applicable modulation rate.

Signal Quality Measurement—The Eye Pattern (Continued)

If any one of these conditions is not satisfied, the signal quality is reduced (more distortion). The effects of receiver bias or threshold ambiguity and driver offset can be determined by location of the decision threshold(s) on the oscillograph of the eye pattern for that driver/cable modulation rate combination. For eye patterns displaying more than 20% isochronous distortion, the slope of the signal in the transition region is relatively small. Therefore, a small amount of bias results in a large increase in net isochronous distortion. See *Figure 16* for a graphic illustration of this effect. In the interest of conservative design practices, systems should always be designed with less than 5% transition spread in the eye pattern. This allows the detrimental effects due to bias to be minimized, thus simplifying construction of line drivers and receivers.

Other Pulse Codes and Signal Quality

In the preceding sections, the discussion of signal quality has been centered around the use of NRZ signaling, because it represents the simplest and most commonly used pulse code. Other pulse codes have been developed which provide one or more of the following desirable features:

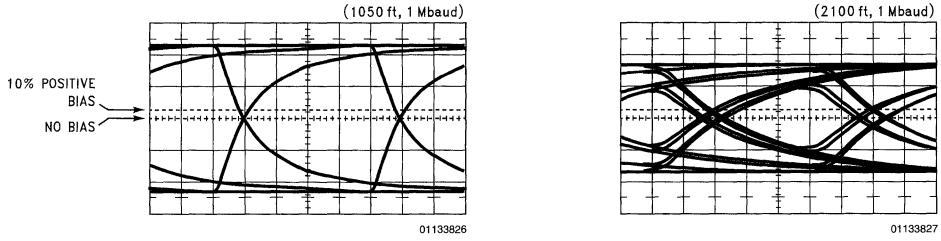
- Compress the overall bandwidth normally required to adequately transmit the signal yet still ensure recovery of the binary data.
- Eliminate the need for a dc response in the transmission medium so that transformer coupling can be used for phantom power distribution on repeated lines. (The elimination of a dc characteristic of the pulse code also allows ac coupling of amplifier circuits).
- Provide a clocking scheme within the signal so that no separate clock channel is required for synchronization.
- Provide built-in error detection.

The following discussion is restricted to the binary class of baseband signals. This simply means that each decision by the line receiver yields one bit of information. The *M*-ary schemes ($M \geq 3$) can encode more than one bit of information per receiver decision*, but these schemes are seldom applied to baseband signaling due to the complexities of the driver and receiver circuits (especially for $M > 3$). *M*-ary schemes, however, are applied to high speed non-baseband data transmission systems using modems. The price to be paid for the increased bit-packing with multi-level signaling is decreased immunity to noise relative to a binary system. This is because a smaller relative threshold displacement (or amount of noise) is required to produce a signal representing another logic state in the *M*-ary schemes.

Note: *It can be shown that, for *M* levels, the information per receiver decision will be $S = \log_2 M$ bits/decision. Thus, three levels theoretically yield 1.58 bits, four levels yield 2 bits of information, eight levels yield 3 bits, etc.

In general, the binary class of pulse codes can be grouped into four categories:

- Non-Return to Zero (NRZ)
- Return to Zero (RZ)
- Phase Encoded (PE) (sometimes called Split Phase)
- Multi-Level Binary (MLB). (The MLB scheme uses three levels to convey the binary data, but each decision by the line receiver yields only one bit of information.)



$$\text{ISOCHRONOUS DISTORTION (ID)} = \frac{t_{tcs}}{t_{ui}} \times 100\%$$

01133848

BIAS	1050 ft	2100 ft
0%	5% ID	20% ID
10%	12% ID	36% ID

FIGURE 16. Receiver Bias Effect on Total Isochronous Distortion

A secondary differentiation among the pulse codes in concerned with the algebraic signs of the signal levels. If the signal levels have the same algebraic sign for their voltages (or currents) and differ only in their magnitudes, the signaling is called *unipolar*. A very common example of unipolar signaling is TTL or ECL logic. TTL uses two positive voltages to represent its logic states, while ECL uses two negative voltages for its logic states. The complement of unipolar signaling is *polar* signaling. Here, one logic state is represented by a signal voltage or current having a positive sign and the other logic state is represented by a signal with a negative sign. For binary signals, the magnitude of both signals

Other Pulse Codes and Signal Quality (Continued)

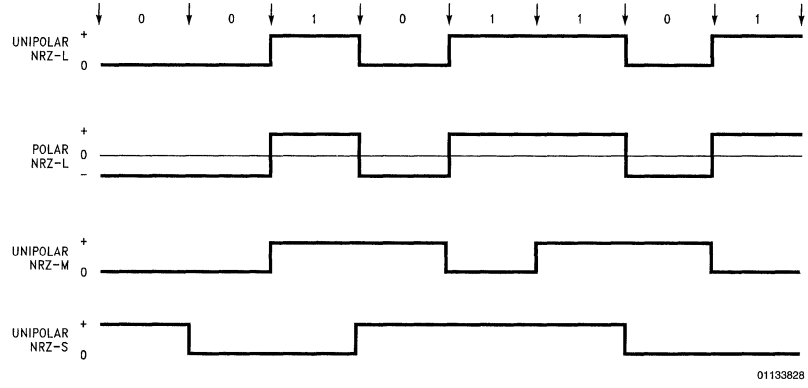
should be equal, ideally. Their only difference should be in the algebraic signs. This allows the receiver to use ground as its decision thershold reference.

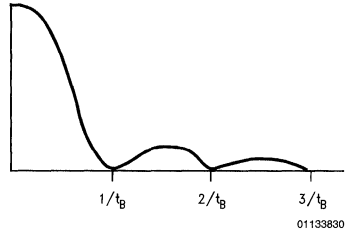
NON-RETURN TO ZERO (NRZ) PULSE CODES

There are three NRZ pulse codes: NRZ-Level (NRZ-L), NRZ-Mark (NRZ-M), and NRZ-Space (NRZ-S). NRZ-L is the same pulse code as previously discussed. In NRZ-L signaling, data is represented by a constant signal level during the bit time interval, with one signal level corresponding to one logic state, and the other signal level corresponding to the opposite logic state. In NRZ-M or NRZ-S signaling, however, a change in signal level at the start of a bit interval corresponds to one logic state and no change in signal level at the start of a bit interval corresponds to the opposite logic state. For NRZ-M pulse codes, a change in signal level at the start of the bit interval indicates a logic One (Mark), while no change in signal level indicates a logic Zero (Space). NRZ-S is a logical complement to NRZ-M. A change in signal level means a logic Zero and no change means logic One. With NRZ-M and NRZ-S pulse codes, therefore, there is no direct correspondence between signal levels and logic states as there is with NRZ-L signaling. Any of the NRZ pulse codes may, of course, be used in unipolar or polar form. The NRZ codes are shown in *Figure 17*, along with their generation algorithm*, signal levels vs time, and their general power density spectrum.

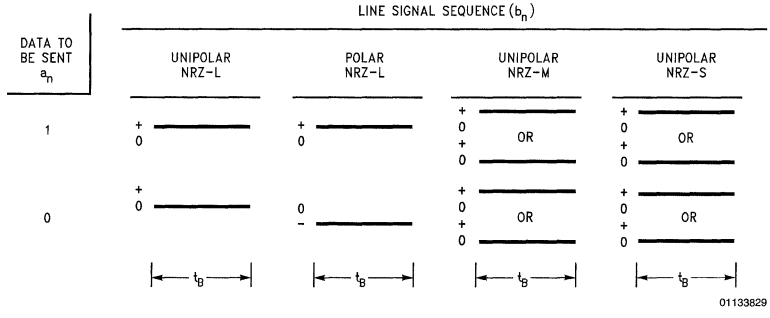
Note: *The generation algorithm showing the sequence of signal levels on the line, represented by the set $\{b_n\}$, is determined by the sequence of input logic states, represented by the set $\{a_n\}$ See Bennet[14] for detailed usage of this notation

Other Pulse Codes and Signal Quality (Continued)





GENERAL POWER SPECTRUM
FOR NRZ CODES



t_{ui}	t_B	t_B	t_B	t_B
$a_n = 1$	$b_n = +$	$b_n = +$	$b_n = (-)\ b_n - 1$	$b_n = b_n - 1$
$a_n = 0$	$b_n = 0$	$b_n = -$	$b_n = b_n - 1$	$b_n = (-)b_n - 1$

FIGURE 17. Non-Return to Zero (NRZ) Pulse Codes

Other Pulse Codes and Signal Quality (Continued)

The degradation in signal quality caused by intersymbol interference for NRZ-L signaling was discussed earlier. Since the minimum signaling element (unit interval) for all three NRZ pulse codes is equal to t_B, the previous signal quality discussion for NRZ-L also applies equally to NRZ-M and NRZ-S pulse codes. The following is a capsule summary of the previous discussion on NRZ signal quality.

- When t_B is less than the 0%–50% rise or fall time of the signal at the line end, the open space in the eye pattern closes, thereby indicating error-free data transmission is unlikely.
- When t_B is less than the 10%–90% rise or fall time of the line end signal, some intersymbol interference is present and thus, some time jitter in the transitions of the recovered data will be present.

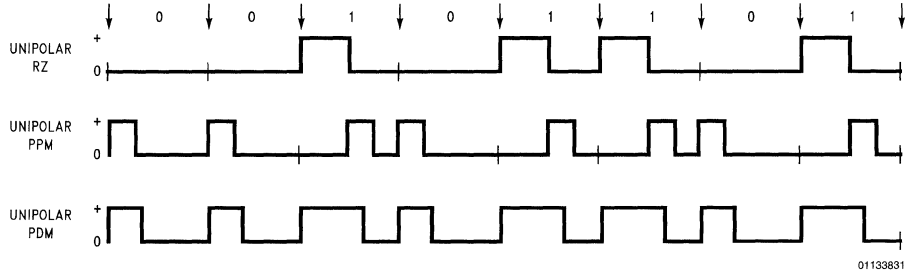
NRZ codes are simple to generate and decode because no precoding or special treatment is required. This simplicity makes them probably the most widely used pulse codes, with NRZ-L the leader by far. NRZ-M has been widely used in digital magnetic recording where it is usually called NRZI for Non-Return to Zero, Invert-on-Ones. In terms of the four desirable features for a pulse code listed at the start of this section, however, non of the NRZ codes are all that great—NRZ codes do possess a strong dc component, and have neither intrinsic clocking, nor error detection features. Even so, their power frequency spectra are used as references for comparison with other pulse codes.

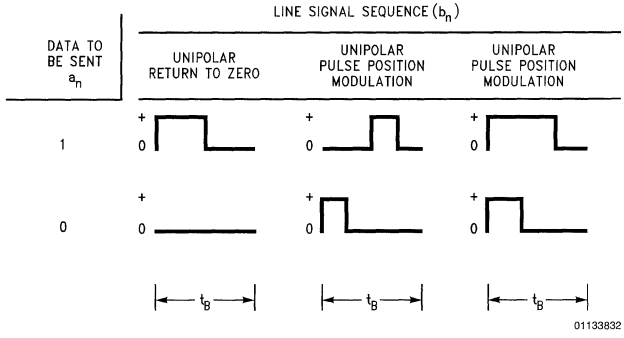
RETURN TO ZERO (RZ) PULSE CODES

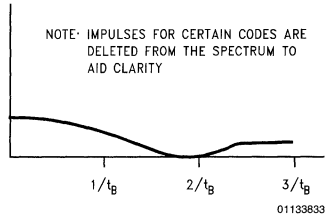
The RZ group of pulse codes are usually simple combinations of NRZL data and its associated single or double frequency clock. By combining the clock with data, all RZ codes possess some intrinsic synchronization feature. Three representative RZ pulse codes are shown in *Figure 18*. Unipolar RZ is formed by performing a logic AND between the NRZ-L data and its clock. Thus a logic Zero is represented by the absence of a pulse during the bit time interval, and a logic One is represented by a pulse as shown. Pulse Position Modulation (PPM) uses a pulse of $t_B/4$ duration beginning at the start of the bit interval to indicate a logic Zero, and a $t_B/4$ pulse beginning at the middle of the bit interval to indicate a logic One. Pulse Duration Modulation (PDM) uses a $t_B/3$ duration pulse for a logic Zero and a (⅔) t_B pulse for a logic One, with the rising edge of both pulses coinciding with the start of the bit interval. PDM with $t_B/4$ pulse widths is also used but better results are usually obtained with the $t_B/3$, 2 $t_B/3$ scheme.

The reason for differentiating between information rate and modulation rate can now be further clarified. Each of the RZ pulse codes in *Figure 18* has the same information rate; i.e., $1/t_B$ bits per second. Their respective minimum signaling elements (unit intervals) however, are all less than t_B so the *modulation rate* for the RZ pulse code is greater than the *information rate*. Remember that with NRZ signaling, the unit interval and the bit time interval are equal in duration, so the information rate in bps is equal to the modulation rate in bauds. For isochronous NRZ signaling, the measures bps and baud are both synonymous and interchangeable.

Other Pulse Codes and Signal Quality (Continued)







GENERAL POWER SPECTRUM FOR RZ CODES

t_{ui}	$t_B/2$	$t_B/4$	$t_B/3$
$a_n = 1$	$b_n = (+)$ $\{0 \le t < t_B/2$ $b_n = (0)$ $\{t_B/2 \le t < t_B$	$b_n = (+)$ $\{t_B/2 \le t \le 3t_B/4$ $b_n = (0)$ $\begin{cases} 0 \le t < t_B/2 \\ 3t_B/4 < t < t_B \end{cases}$	$b_n = (+)$ $\{0 \le t \le 2t_B/3$ $b_n = (0)$ $\{ 2t_B/3 \le t < t_B$
$a_n = 0$	$b_n = (0)$	$b_n = (+)$ $\{0 \le t \le t_B/4$ $b_n = (0)$ $\{t_B/4 < t < t_B$	$b_n = (+)$ $\{0 \le t \le t_B/3$ $b_n = (0)$ $\{t_B/3 \le t_B$

FIGURE 18. Return to Zero (RZ) Pulse Codes

Inspection of unipolar RZ signaling reveals that the unit interval is ½ bit interval ($t_{ui} = t_B/2$). When this unit interval is less than the 0%–50% rise or fall time of the line, the data is likely to be unrecoverable. With a fixed modulation rate, the price paid to include clocking information into unipolar RZ is reduced information rate over that for NRZ signaling. Likewise, for PPM with its unit interval of $t_B/4$, the information rate reduces to ¼ that of NRZ data under the same conditions. This is because the maximum modulation rate is determined by the 50% rise time of the line which is constant for a given length and type of line. PDM has a unit interval of $t_B/3$ so, for a given maximum modulation rate, the resulting information rate is ⅓ that of NRZ data.

The preceding argument should not be taken as strictly correct—since the actual intersymbol interference patterns for the three RZ codes discussed differ somewhat from the pattern with NRZ codes. A random sequence of NRZ data can easily consist of a long sequence of Zeros followed by a single One and then a long sequence of Zeros, so the $t_{50\%}$

Other Pulse Codes and Signal Quality (Continued)

limit can be accurately applied. Unipolar RZ, in response to the same long data sequence, produces a $t_B/2$ pulse, so the $t_{50\%}$ argument can be applied here too. With PPM and PDM, the maximum time that the line signal can be in one state is quite reduced from the NRZ case. For PPM, this time is 1.25 t_B (010 data sequence) while for PDM, it is 0.67 t_B (see *Figure 18*). With PPM and PDM, then, the line signal may never reach the final signal levels that it does with NRZ data. So, the PPM and PDM signals have a head start, so to speak, in reaching the threshold crossing of the receiver. Because of the reduced time that PDM and PPM signal levels are allowed to remain at one signal level, their signaling may still operate at a modulation rate slightly above that where the NRZ data shows 100% transition jitter. Even with this slight correction to the previous discussion, the RZ group of pulse codes still sacrifice information rate in return for synchronization. The PPM scheme appears to be a poor trade in this respect, since PDM allows a greater information rate while retaining the self-clocking feature. Unipolar RZ, because it provides no clocking for a logic Zero signal, is not generally as useful as PDM for baseband data transmission. However, unipolar RZ is used in older digital magnetic tape recorders.

Examination of RZ codes shows only one more desirable feature than NRZ codes: clocking. RZ codes still have a dc component in their power density spectrum (*Figure 18*) and their bandwidth is extended (first null at $2/t_B$) over that of NRZ (first null $1/t_B$). RZ codes do not have any intrinsic error detection features.

PHASE ENCODED (PE) PULSE CODES

The PE group of pulse codes uses signal level transitions to carry both binary data and synchronization information. Each of the codes provides at least one signal level transition per bit interval aiding synchronous recovery of the binary data. Simply stated, Biphase-Level (Biϕ-L) code is binary phase shift keying (PSK) and is the result of an Exclusive-OR logic function performed on the NRZ-L data and its clock; it is further required that the resultant signal be phase coherent (i.e., no glitches). Biphase—Mark (Biϕ-M) and Biphase-Space (Biϕ-S) codes are essentially phase coherent, binary frequency shift keying (FSK). In Biϕ-M, a logic One is represented by a constant level during the bit interval (one-half cycle of the lower frequency $1/(2\ t_B)$, while a logic Zero is represented by one-half cycle of the higher frequency $1/t_B$. In Biϕ-S, the logic states are reversed from those in Biϕ-M. Another way of thinking of Biϕ-M or Biϕ-S is as follows.

- Change signal level at the end of each bit interval regardless of the logic state of the data.
- Change signal level at the middle of each bit interval to mean a particular logic state.

In Biϕ-M (sometimes call diphase), a mid-bit interval change in signal level indicates a logic One (Mark), while no change indicates a logic Zero. For Biϕ-S, no signal level change in the middle of the bit interval means a logic One, while a change means a logic Zero.

In Biϕ-L (also called Manchester Code), a positive-going transition at the middle of the bit interval means a logic Zero, while a negative-going transition there indicates a logic One.

The fourth member of the PE family is Delay Modulation (DM)[15, 16] sometimes referred to as Miller code. Here logic One is represented by a mid-bit interval signal level change, and a logic Zero is represented by a signal level change at the end of the bit interval if the logic Zero is followed by another logic Zero. If the logic Zero is immediately followed by a logic One, no signal level transition at the end of the first bit interval is used. The waveforms encoding algorithms, and general power density spectra for the PE pulse code family are shown in *Figure 19*.

Note: *Delay Modulation[15, 16] has a maximum of 2 t_B without a signal level transition

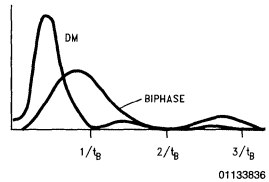
A brief inspection of the signal waveforms for the three Biphase pulse codes reveals that their minimum signaling element has a duration of one-half bit interval ($t_{ui} = t_B/2$); the longest duration of either signal level is one bit interval Similarly, DM is seen to have a minimum signaling element of one bit interval ($t_{ui} = t_B$) and the maximum duration of either signal level is two bit intervals (produced by a 101 pattern). Biphase codes should exhibit eye closure (they would not be recoverable without equalization) when $t_{ui} \leq t_{0\%-50\%}$. So, a 50% jitter on NRZ signaling approximately corresponds to the Biphase codes non-operation point. Biphase codes, therefore, provide one-half the information rate of NRZ signals at a given maximum modulation rate. This is in exchange for synchronization information and a dc-free spectrum when used in polar form.

DM should have essentially the same intersymbol interference characteristics as NRZ, since the unit interval is the same for both codes. DM may perform slightly better than NRZ, because the maximum duration of either signal level is two bit intervals. Overall, DM is better coding scheme than the Biϕ. It does not require as much bandwidth as Biϕ and still possesses the desirable dc response and synchronization qualities.

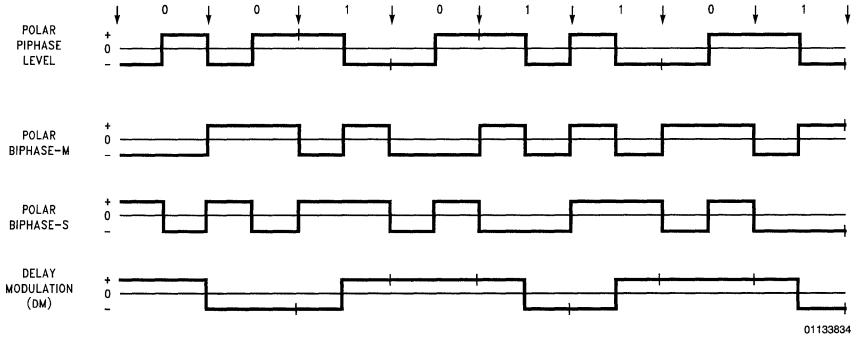
Both Biϕ and DM are good choices for digital magnetic recording[16]; Biϕ is widely used in disc memory equipment, and DM is rapidly gaining acceptance where high bit packing densities are desired. Overall scoring, in terms of the four desirable characteristics, shows the PE pulse codes with three primary features; bandwidth compression, no dc, and intrinsic synchronization.

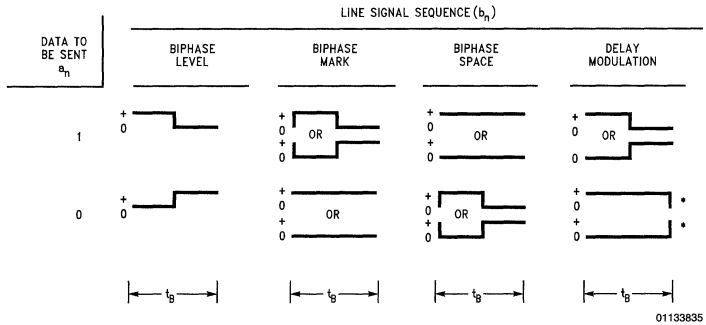
Th Biϕ family does not possess any intrinsic error detection scheme. DM does possess the capability of detecting some—but not all—single bit errors. This detection process is accomplished by checking to see if a single level persists longer than two bit intervals, in which case, an error is indicated. DM detection requires two samples per bit interval.

Other Pulse Codes and Signal Quality (Continued)



GENERAL POWER SPECTRUM
FOR SPLIT PHASE CODES





*Transition only if followed by another "0" ($a_{k+1} = 0$)

FIGURE 19. Phase Encoded (PE) Pulse Codes

Other Pulse Codes and Signal Quality (Continued)

t_{ui}	$t_B/2$	t_B2	$t_B/2$	t_B
			$b_n = (-)\, b_{n-1}$*	if final value of $b_{n-1} = (+)$
	$b_n = (+)\{0 < t < t_B/2$		*complement of	then $b_n = (+)\{0 < t < t_B/2$
$a_n = 1$	$b_n = (-)\ \{t_B/2 \le t \le t_B$	‡	final level of	and $b_n = (-)\ \{ t_B/2 \le t \le t_B$
			last b_n	else, compliment above b_n
				values for times shown
				if final value of $b_{n-1} = (+)$
		$b_n = (-)\, b_{n-1}$*		then $b_n = (+)\ \{ 0 \le t < t_B$
$a_n = 0$	$b_n = (-)\ \{ 0 < t < t_B/2$	*complement of	‡	if $a_{n+1} = (0)$ then $b_n = (-)\ \{ t = t_B$
	$b_n = (+)\ \{ t_B/2 \le t \le t_B$	final level of		else $b_n = (+)\ \{ t = t_B$
		last b_n		if final value of $b_{n-1} = (-)$
				then complement b_n values above

‡ If b_{n-1} final level = (+), then $\begin{cases} b_n = (-)\ \{ 0 \le t < t_B/2 \\ b_n = (+)\ \{ t_B/2 \le t < t_B \end{cases}$

If b_{n-1} final level = (−), then $\begin{cases} b_n = (+)\ \{ 0 \le t < t_B/2 \\ b_n = (-)\ \{ t_B/2 \le t < t_B \end{cases}$

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MULTI-LEVEL BINARY (PLB) PULSE CODES

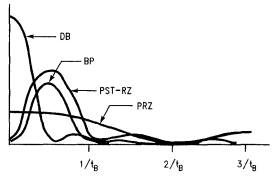
The pulse codes in the MLB groupd discussed have a common characteristic of using three signal levels (expressed in shofthand notation as +, 0, –) to represent the binary information, but each receiver decision yields only one bit of information. These are sometimes called *pseudoternary* codes to distinguish them from true ternary codes wherein each receiver decision can yield 1.58 information bits.

The most straightforward pulse code in the MLB group is polar RZ (*Figure 20*). Some authors place PRZ in the RZ group, but since PRZ uses three signal levels, it is placed in the MLB group here. A logic One is represented by a positive polarity pulse, and a logic Zero is represented by a negative polarity pulse. Each pulse lasts for one-half bit interval. PRZ has excellent synchronization properties since there is a pulse present during every bit interval.

Bipolar (BP)[17, 18] uses a $t_B/2$ duration pulse to signify a logic One, and no pulse during the bit interval to signify a logic Zero. The polarity of the pulses for a logic One is alternated as shown in *Figure 20*. Bipolar coding is also known as Alternate Mark Inversion. BP is widely used in Bell Systems T1–PCM carrier systems as a pulse code transmitted along a regenerative repeated transmission line. Since BP has no dc component, the regenerative repeaters along the span line may be transformer coupled and powered by a phantom constant current power loop from the central office. The synchronization properties of BP are excellent if the number of Zero bits transmitted in series is constrained. This constraint on the number of sequential Zeros allows clock circuits in each repeater to remain in synchronization. A scheme called Binary with 6 Zeros Substitution (B6ZS) was developed to replace 6 Zeros with a given signal sequence to offset this loss of synchronization[18]. Bipolar coding has a limited capability to detect single errors, all odd errors, and certain even error combinations which violate the mark alternation rule. Another scheme called High Density Bipolar with 3 Zeros substitution (HDB-3) replaces four successive Zeros (no pulses) with three Zeros followed by a pulse whose polarity violates the Mark alternation rule[19]. Subsequent detection of this pattern (three Zeros and pulse violating the polarity coding rule) causes the receiver to substitute four Zeros for the received 0001 pattern.

In Dicode (DI)[20, 21], a polar pulse (either t_B for DI-NRZ or $t_B/2$ for DI-RZ) is sent for every input data transition. The limiting constraint is that the successive pulses must alternate in sign (*Figure 19*). As in NRZ-M and NRZ-S, the actual polarity of the pulses does not necessarily correspond to the logic state of the data (a positive pulse may represent either a Zero-to-One or a One-to-Zero transition of the input data). The power spectrum for DI is the same as for BP (no dc component). Bit synchronization for DI can be obtained in the same manner as for BP, but with DI, the number of bits of the same logic state must be controlled in order for the receiver to maintain bit synchronization. DI also has the intrinsic capability of detecting single bit errors (via two successive positive or negative signal levels), all odd, and some even numbers of errors.

Other Pulse Codes and Signal Quality (Continued)



GENERAL POWER DENSITY SPECTRUM
RANDOM SEQUENCE
P(0) = P(1) = 0 5

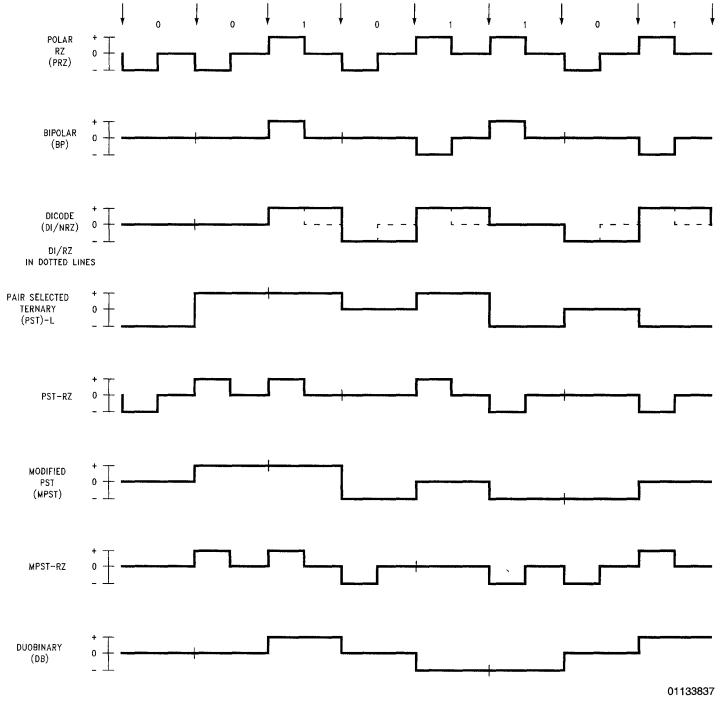


FIGURE 20. Multilevel Binary (MLB) or Pseudoternary Pulse Codes

Pair Selected Ternary (PST)[18, 22] and Modified PST (MPST)[22] were proposed to minimize the disadvantages of BP coding: loss of synchronization with long strings of Zeros and timing jitter. PST/MPST maintains the strong features of BP: dc free spectrum, single error detection. To produce PST or MPST, the incoming bits are grouped into pairs, and the signal produced on the line is governed by a coding table. Two modes are also used in the coding table with a change in mode occurring after a certain bit pair is transmitted. The features of PST/MPST thus include:

- No dc spectral component,
- No loss of synchronization with long strings of Zeros,
- Intrinsic error detection,
- Simplification of requirements for timing extraction circuits with respect to BP.

MPST coding was developed primarily to speed up the framing process, i.e., selecting which two successive pulses constitute a valid pair, when the probability for a Zero and a One are not equal.

Duobinary[23, 24] is an example of a correlative level coding technique, wherein a correlation exists between successive signal levels. Duobinary uses three signal levels with the middle level corresponding to a logic Zero, and the other two levels corresponding to a logic One. The pseudoternary signal is generated by precoding the input data, which results in constraining the line signal to change only to the neighboring level, i.e., the (+) to (−) and (−) to (+) level changes are not allowed. This precoding process uses controlled intersymbol interference as part of the coding scheme. The benefit is an effective doubling of the bit rate for

Other Pulse Codes and Signal Quality (Continued)

a given bandwidth and concentration of the power spectrum toward dc (*Figure 20*). Duobinary has the capability to detect single errors which violate the encoding rules. In terms of bandwidth utilization, Duobinary ranks first among all the binary and MLB codes[20], but its strong dc component prohibits the use of ac-coupled transmission media. Synchronization properties are similar to NRZ, thus external clocking must be used to recover the data.

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A Comparison of Differential Termination Techniques

National Semiconductor
Application Note 903
Joe Vo

Introduction

Transmission line termination should be an important consideration to the designer who must transmit electrical signals from any point A to any point B Proper line termination becomes increasingly important as designs migrate towards higher data transfer rates over longer lengths of transmission media. However, the subject of transmission line termination can be somewhat confusing since there are so many ways in which a signal can be terminated. Therefore, the advantages and disadvantages of each termination option are not always obvious

The purpose of this application note is to remove some of the confusion which may surround signal termination. This discussion, however, will focus attention upon signal termination only as it applies to differential data transmission over twisted pair cable. Common differential signal termination techniques will be presented and the advantages and disadvantages of each will be discussed.

Each discussion will also include a sample waveform generated by a setup consisting of a function generator whose signals are transmitted across a twisted pair cable by a differential line driver and sensed at the far end by a differential line receiver. This application note will specifically address the following differential termination options:

- Unterminated
- Series/Backmatch
- Parallel
- AC
- Power (Failsafe)
- Alternate Failsafe
- Bi-Directional

For the purposes of discussion, popular TIA/EIA-422 drivers and receivers, such as the DS26LS31 and DS26LS32A, will be used to further clarify differential termination.

Unterminated

The selection of one termination option over another is oftentimes dictated by the performance requirements of the application. The selection criteria may also hinge upon other factors such as cost. From this cost perspective the option of not terminating the signal is clearly the most cost effective solution. Consider *Figure 1*, where a DS26LS31 differential driver and a DS26LS32A differential receiver have been connected (using a twisted pair cable) together without a termination element. Because there is no signal termination element, the DS26LS31 driver's worst case load is the DS26LS32A receiver's minimum input resistance.

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FIGURE 1. Unterminated Configuration

Since, TIA/EIA-422-A (RS-422) standard defines the DS26LS32A's minimum input resistance to be 4 kΩ, the driver's worst case load, as seen in *Figure 1*, is then 4 kΩ

In the unterminated configuration, the DS26LS31 driver is only required to source a minimal amount of current in order to drive a signal to the receiver. This minimal DC current sourcing requirement in turn minimizes the driver's on chip power dissipation. In addition, the 4 kΩ driver output load results in a higher driver output swing (than if the driver was loaded with 100Ω) which in turn increases DC noise margin. This increase in noise margin further diminishes the possibility that system noise will improperly switch the receiver. To be sure that there is no confusion, noise margin is defined as the difference between the minimum driver output swing and the maximum receiver sensitivity. On the other hand, if a receiver was used which complies to TIA/EIA-485 (RS-485), the resulting noise margin would be even greater. This is because the minimum input resistance of an RS-485 receiver must be greater than 12 kΩ as compared to 4 kΩ for an RS-422 receiver.

The absence of a termination element at the DS26LS32A's inputs also guarantees that the receiver output is in a known logic state when the transmission line is in the idle or open line state (receiver dependent). This condition is commonly referred to as open input receiver failsafe. This receiver failsafe (Note 1) bias is guaranteed by internal pull up and pull down resistors on the positive and negative receiver inputs, respectively. These pull up and pull down resistors bias the input differential voltage (V_{ID}) to a value greater than 200 mV when the line is, for example, idle (un-driven). This bias is significant in that it represents the minimum guaranteed V_{ID} required to switch the receiver output into a logic high state.

Note: A complete discussion of receiver failsafe can be found in Application Note 847 (AN-847)

There are, however, some disadvantages with an unterminated cable. The most significant effect of unterminated data transmission is the introduction of signal reflections onto the transmission line. Basic transmission line theory states that a signal propagating down a transmission line will be reflected back towards the source if the outbound signal encounters a mismatch in line impedance at the far end. In the case of *Figure 1*, the mismatch occurs between the characteristic impedance of the twisted pair (typically 100Ω) and the 4 kΩ input resistance of the DS26LS32A. The result is a signal reflection back towards the driver. This reflection then encounters another impedance mismatch at the driver outputs which in turn generates additional reflections back toward the receiver, and so on. The net result is a number of reflections propagating back and forth between the driver and receiver. These reflections can be observed in *Figure 2*.

Unterminated (Continued)

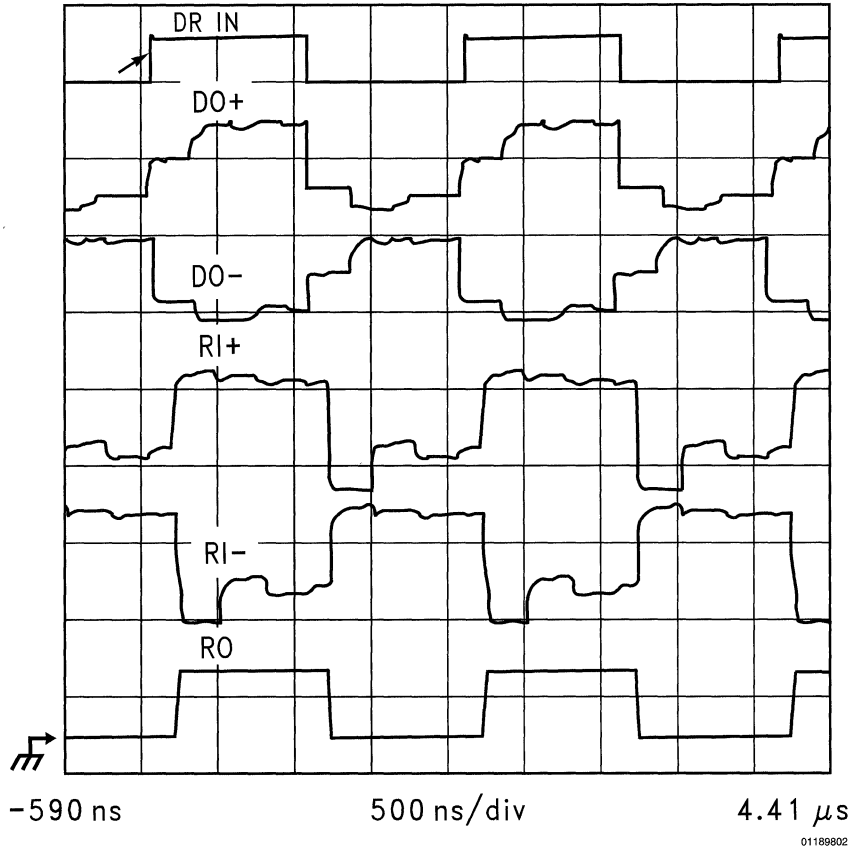

FIGURE 2. Unterminated Waveforms

The main limitation of unterminated signals can be clearly seen in *Figure 2*. A positive reflection is generated when the signal encounters the large input resistance of the receiver. These reflections propagate back and forth until a steady state condition is reached after several round trip cable delays. The delay is a function of the cable length and the cable velocity. *Figure 2* shows that the reflections settle after three round trips. To limit the effect of these reflections, unterminated signals should only be used in applications with low data rates and short driving distances.

The data being transmitted should, therefore, not make any transitions until after this steady state condition has been reached. A low data rate ensures that reflections have sufficient time to settle before the next signal transition. At the same time, a short cable length ensures that the time required for the reflections to settle is kept to a minimum. The low data rate and short cable length dictated by the lack of termination is probably the most significant shortcoming of the unterminated option.

Low speed is generally characterized to be either signalling rates below 200 kbits/sec or when the cable delay (the time required for an electrical signal to transverse the cable) is substantially shorter than the bit width (unit interval) or when the signal rise time is more than four times the one way propagation delay of the cable (i.e., not a transmission line). As a general rule, if the signal rise time is greater than four times the propagation delay of the cable, the cable is no longer considered a transmission line.

It should be mentioned that most differential data transmission applications provide for some kind of signal termination. This is because most differential applications transmit data at relatively high transfer rates over relatively long distances. In these type of applications, signal termination is critically important. If the application only requires low speed operation over short distances, an unterminated transmission line may be the simplest solution.

Series Termination

Another termination option is popularly known as either series or backmatch termination. *Figure 3* illustrates this type of termination. The termination resistors, R_S, are chosen such that their value plus the impedance of the driver's output equal the characteristic impedance of the cable. Now as the

Series Termination (Continued)

driven signal propagates down the transmission line an impedance mismatch is still encountered at the far end of the cable (receiver inputs).

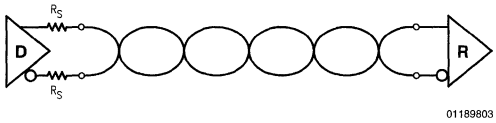

FIGURE 3. Series Termination Configuration

However, when that signal propagates back to the driver the reflection is terminated at the driver output. There is only one reflection before the driven signal reaches a steady state condition. How long it takes for the driven signal to reach steady state is still dependent upon the length of cable the signal must traverse. As with the unterminated option the driver power dissipation is still minimized due to the light loading presented by the 4 kΩ receiver input resistance. The driver loading remains unchanged from the unterminated option. In both cases the driver is effectively loaded with the receiver's input impedance. DC noise margin has again increased and the open input receiver failsafe feature is still supported for idle and open line conditions.

There are three major disadvantages in using series termination. First, the driver output impedances can vary, due to normal process variations, from one manufacturer to another and from one driver load to another. Should there be a problem which involves replacing line drivers, there is a chance that the designer might have to rework the board in order to ensure that the R_S matches the new driver's output impedance.

Second, series termination is commonly limited to only point to point applications. Consider the following example. If a second receiver (multidrop application) was located halfway between the driver and receiver at the far end of the cable, the noise margin seen by the middle receiver would change between the incident signal and the reflected signal. Such a problem would not exist in a point to point application where only one receiver is used with one driver.

Third, there is still an impedance mismatch at the receiver inputs. Again, this mismatch is caused by a signal propagating down a 100Ω cable suddenly encountering a 4 kΩ receiver input resistance. This impedance mismatch will continue to cause reflections on the transmission line as illustrated in *Figure 4*.

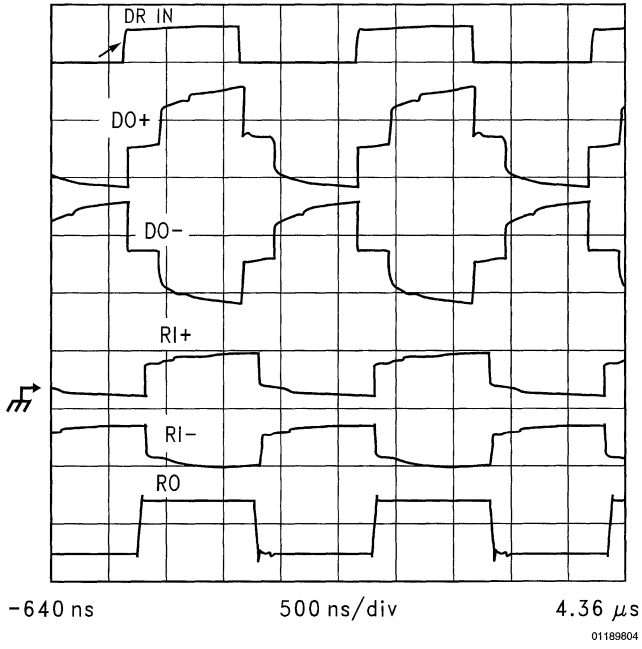

FIGURE 4. Series Termination Waveforms

Notice the reflections which result when the driven signal encounters an impedance mismatch at the receiver input. The reflection propagates back to the driver and is somewhat terminated by the driver's output impedance. The reflected signal is terminated because the combined impedance of the series resistor (R_S) and the driver's output impedance comes close to matching the characteristic impedance of the cable. In contrast with *Figure 2*'s unterminated signal waveform, the waveform seen in *Figure 4* is characterized by only one reflection.

In all it will take the signal one round trip cable delay to be reflected back towards the signal source. Since all reflections should be allowed to settle before the next data tran-

Series Termination (Continued)

sition (to maintain data integrity), it is imperative that the round trip cable delay be kept much less than the time unit interval (TUI—defined to be the minimum bit width or the "distance" between signal transitions). In other words, series termination should be limited to applications where the cable lengths are short (to minimize round trip cable delays) and the data rate is low (to maximize the TUI). And to a lesser degree, the series termination option may not be the ideal choice from a cost perspective in that it requires two additional external components.

Parallel Termination

Parallel termination is arguably one of the most prevalent termination schemes today. In contrast to the series termination option, parallel termination employs a resistor across the differential lines at the far (receiver) end of the transmission line to eliminate all reflections. See *Figure 5*.

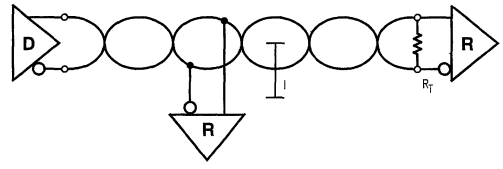

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FIGURE 5. Parallel Termination Configuration

Eliminating all reflections requires that R_T be selected to match the characteristic impedance (Z_O) of the transmission line. As a general rule, however, it is usually better to select $R_T$such that it is slightly greater than Z_O. Over-termination tends to be more desirable than under-termination since over-termination has been observed to improve signal quality. R_T is typically chosen to be equal to Z_O. When over-termination is used R_T is typically chosen to be up to 10% larger than Z_O. The elimination of reflections permits higher data rates over longer cable lengths. Keep in mind, however, that there is an inverse relationship between data rate and cable length. That is, the higher the data rate the shorter the cable and conversely the lower the data rate the longer the cable. Higher data rates and longer cable lengths translate simply into smaller TUI's and longer cable delays. Unlike series termination where high data rates and long cable lengths can negatively impact data integrity, parallel termination can effectively remove all reflections; thereby removing all concerns about reflections interfering with data transitions. See *Figure 6*.

Parallel Termination (Continued)

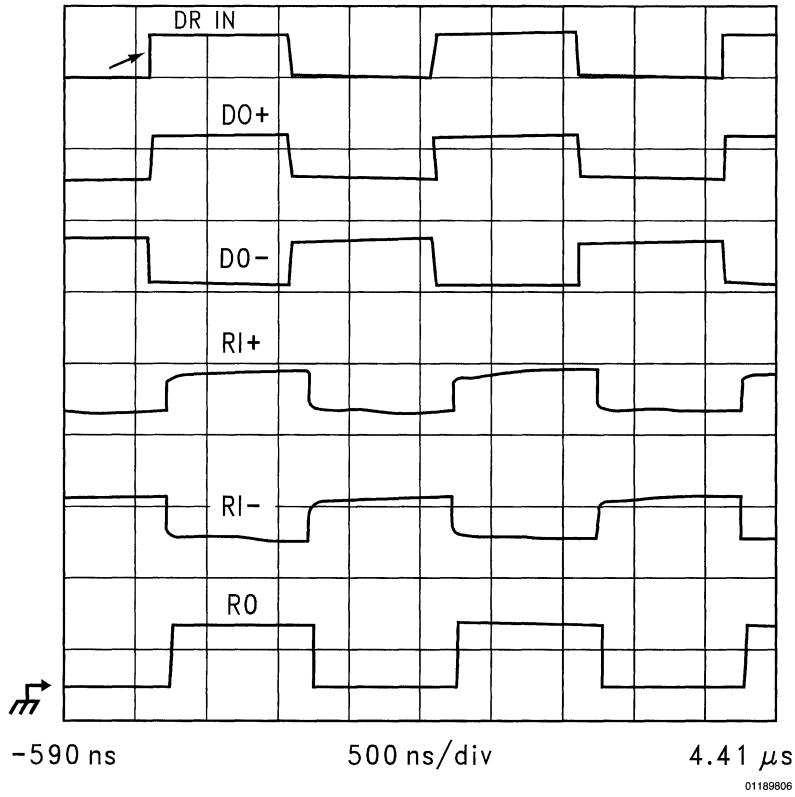

FIGURE 6. Parallel Termination Waveforms

As seen in *Figure 6* both driver output and receiver input signals are free of reflections. Such results make parallel termination optimal for use in either high speed (10 Mb/s), or long cable length (up to 4000 feet), applications.

Another benefit the parallel termination provides is that both point to point and multidrop applications are supported. Recall that multidrop is defined as a distribution system composed of one driver and up to ten receivers spread out along the cable as defined in the TIA/EIA-422 standard. The parallel termination is located at the far end (opposite the driver) of the cable and effectively terminates the signal at that location, preventing reflections.

There are also disadvantages to parallel termination. Let's examine these disadvantages as they pertain to multidrop configurations. An intrinsic assumption to multidrop operation is that stub lengths, as measured by "l" in *Figure 5*, are minimized. Despite the fact that all receivers are effectively terminated with R_T, long stub lengths will once again reintroduce impedance mis-matches and reflections. So while parallel termination may remove reflections and permit multidrop configurations, it does place a restriction upon the stub lengths associated with these other receivers. Typically stubs should be kept to less that ¼ of the drivers rise time in length to minimize transmission line effects, and reflections.

TIA/EIA-422-A standard does recommend a 100Ω resistor to be used when the differential line is parallel terminated. Therefore, applications which use a TIA/EIA-422-A driver such as the DS26LS31 or DS26C31 are commonly terminated with 100Ω at the far end of the twisted pair cable. While the 100Ω parallel termination eliminates all reflections, the power dissipated by the driver will increase substantially with the addition of this resistor. This increased driver power dissipation is a major disadvantage of parallel termination. The absence of this termination resistor keeps driver power dissipation low for unterminated and series terminated drivers and is a major advantage of these two termination options.

Noise margin will also decrease with parallel termination. The relatively light loading (4 kΩ) of unterminated and series terminated drivers led to larger driver output swings. The heavier driver load (typically 100Ω) brought on by parallel termination reduces the driver's output signal swing. However, even with this reduction, there is ample noise margin left to ensure that the receiver does not improperly switch.

Recall the discussion earlier about receiver failsafe with the unterminated and series options. In both cases, open input receiver failsafe operation was guaranteed because of internal circuitry (receiver dependent) which biases the differen-

Parallel Termination (Continued)

tial input voltage (V_{ID}) to a value greater than its differential threshold. Since the resulting bias voltage at the receivers inputs (V_{ID}), is greater than +200 mV, the output of the DS26LS32A receiver remains in a stable HIGH state. Unlike unterminated and series options, parallel termination cannot support open input receiver failsafe when the transmission line is in the idle state. This shortcoming of parallel termination is discussed in much greater detail later in the section which describes power and alternate failsafe termination (see AN-847 for more of information on failsafe biasing differential buses).

AC Termination

The effectiveness of parallel termination is oftentimes countered by increased driver power dissipation and receiver failsafe concerns. The DC loop current required by the termination resistor, R_T (see *Figure 5*), is often too large in order to be useful for power conscious applications or for seldomly switched control lines. In asynchronous applications, parallel termination's is not able to guarantee receiver failsafe during idle bus states which in turn makes the system susceptible to errors such as false start bits and framing errors. The primary reason for the AC termination, however, grew out of the need for effective transmission line termination with minimal DC loop current.

A representation of an AC terminated differential line is shown in *Figure 7*.

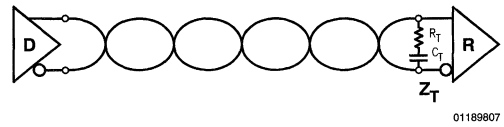

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FIGURE 7. AC Termination Configuration

The value of R_T generally ranges from 100Ω–150Ω (cable Z_O dependent) and is selected to match the characteristic impedance (Z_O) of the cable. C_T, on the other hand, is selected to be equal to the round trip delay of the cable divided by the cable's Z_O.

EQ1: $C_T \leq$ (Cable round trip delay) / Z_O

For this example:

Cable Length = 100 feet

Velocity = 1.7 ns/foot

Char. Impedance = 100Ω

Therefore,

$C_T \leq$ (100 ft x 2 x 1.7 ns/ft)/100Ω or ≤ 3,400 pF.

Further, the resulting R_C time constant should be less than or equal to 10% of the unit interval (TUI). In the example provided the maximum switching rate therefore should be less than 300 kHz. This termination should now behave like a parallel termination during transitions, but yield the expanded noise margins during steady state conditions. See *Figure 8*.

Figure 8 illustrates the tradeoff between parallel terminated and unterminated signals. There are no major reflections and driver power dissipation is reduced at the expense of a low pass filtering effect which essentially limits the application of AC termination to low speed control lines. Note that the frequency of the driven signal in *Figure 8* is 300 kHz whereas it was 500 kHz for the other plots. This was done to maintain the ratio between bit time and the R_C time constant. The draft revision of RS-422-A will include AC termination as an alternative to parallel termination.

AC Termination (Continued)

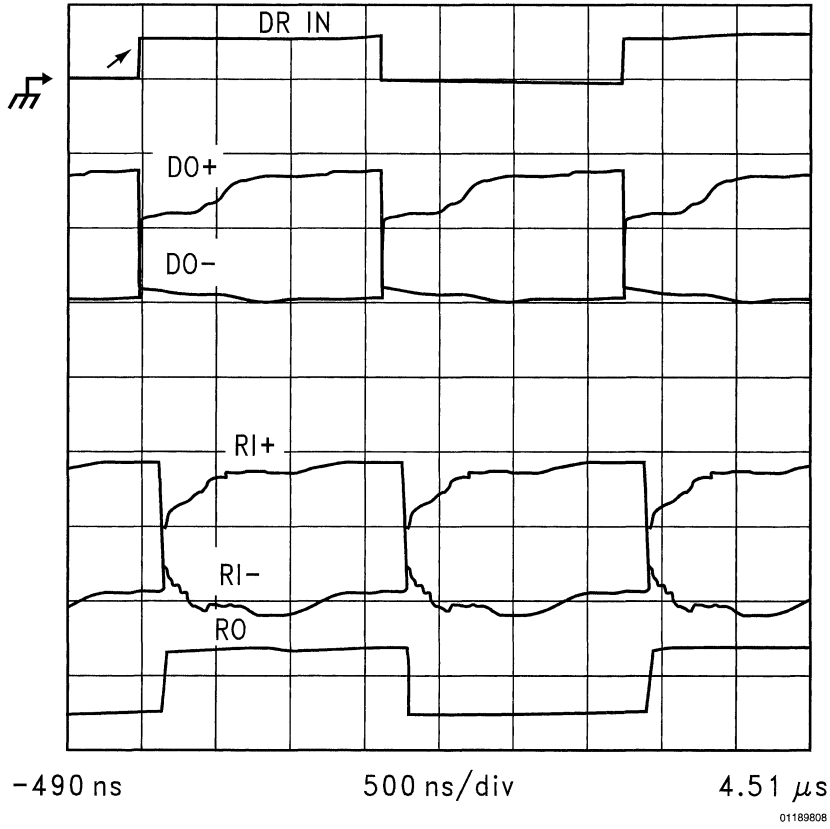


FIGURE 8. AC Termination Waveforms

The waveforms in *Figure 8* should be viewed together with the following brief explanation of how AC termination works. When the driven signal transitions from one logic state to another, the capacitor C_T behaves as a short circuit and consequently, the load presented to the driver is essentially R_T. However, once the driven signal reaches its intended levels, either a logic HIGH or logic LOW, C_T will behave as an open circuit. DC loop current is now blocked. The driver power dissipation will then decrease. The load presented to the driver also decreases. This is due to the fact that the driver is now loaded with a large receiver input resistance typically greater than 4 kΩ; versus the typical R_T of 100Ω–120Ω. This reduced loading condition increases the signal swing of the driver and results in increased noise margin. The idle bus state also forces C_T into the open circuit mode. Once this takes place, the receiver's internal pull up and pull down resistors will bias the output into a known state. Therefore, besides minimizing DC loop current, preventing line reflections, and increasing noise margin, AC termination also supports open input receiver failsafe.

As with all the previously discussed termination options, there are disadvantages in using AC termination. AC termination introduces a low pass filtering effect on the driven signal which tends to limit the maximum data rate of the application. This data rate limitation is the result of the impact that R_T and C_T, together, have upon the driven signal's rise time. How much the data rate is limited is dependent upon the selection of R_T and C_T. Long R_C time constants will have a greater impact upon the driven signal's maximum data rate, and vice versa. Because of of these data rate limitations, the transmission lines best suited for AC termination are typically low speed control lines where level sensitivity is desired over edge sensitivity. Finally, the part count required by AC termination can put it at a disadvantage in cost conscious applications.

Power Termination

Recall that AC termination is intended primarily to eliminate the large DC loop current inherent in parallel termination. The power termination, on the other hand, addresses parallel termination's inability to support receiver failsafe during the idle bus state. See *Figure 9* for an illustration of a transmission line terminated using the power option.

Power Termination (Continued)

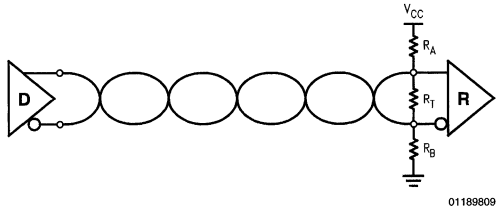


FIGURE 9. Power Termination Configuration

The lack of R_A and R_B, when the bus is idle, almost assures that the receiver output will not be in a known state. This is due to the insufficient voltage across R_T (on the order of 1 mV–5 mV) as caused by the receiver's internal high value pull up and pull down resistors. The presence of these internal pull up and pull down resistors will guarantee receiver failsafe only for the open input condition. In order to switch the receiver into the logic high state, regardless of whether the bus is open or idle, a minimum of +200 mV (with respect to the inverted receiver input) must be developed across R_T. The sole purpose, then, of R_A and R_B is to establish a voltage divider whereby at least +200 mV will be dropped across R_T. A complete explanation of selection criteria for resistor values (R_A and R_B) can be found in AN-847.

The addition of external receiver failsafe biasing resistors, however, does pose some concerns. The primary drawback relates to the increased driver loading with the addition of R_A and R_B. The increased driver loading decreases the driver's output swing and, in turn, reduces the noise margin. Higher driver power dissipation is also symptomatic of the increased driver loading since the driver must source the additional current required by the external failsafe network. One last concern is that the extra cost and subsequent handling of two additional resistors (excluding R_T) might outweigh power termination's advantages in some applications.

Alternate-Failsafe Termination

This version of failsafe termination is essentially an extension of power termination. The addition of R_C and R_D greatly enhances the receiver's ability to operate in harsher environments. See *Figure 10.*

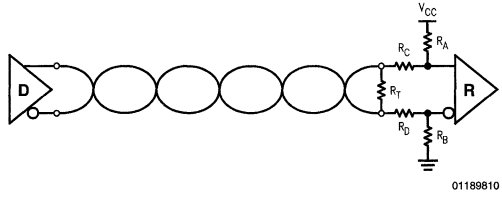


FIGURE 10. Alternate Failsafe Termination Configuration

The advantages of this failsafe termination point directly to this increased ruggedness. A transmission line terminated using the failsafe option will be able to withstand larger common mode voltages. A careful selection of R_C and R_D will determine how much more common mode voltage a line can endure. This is because R_C and $R_D$act as a voltage dividers between the receivers input resistance. The TIA/EIA-422-A standard allows for common mode shifting up to 7V in magnitude, however most integrated circuits support absolute maximum rating that exceed the ±7V limit. The DS26LS32A supports a ±25V ABS MAX input rating. Careful selection of resistors can allow common mode voltages in the 35V–45V range on the cable, while still honoring the 25V limit in the receiver input pins. R_C and R_D are typically 4.7 kΩ, while R_A and R_B are 47 kΩ. This provides 9.5 kΩ between the receiver input pins, and also allows the pull up and pull down resistors to be increased in value to 47 kΩ. This capability lends itself well to applications, such as factory control and building to building data transmission, where the common mode range can occasionally exceed ±7V.

Failsafe termination also guarantees receiver failsafe for open, idle, as well as shorted line conditions. Of all the terminations options discussed, the failsafe option is the only one for which receiver failsafe can be guaranteed for shorted differential lines. Shorting the differential lines together merely shorts out R_T. In this short condition, the receiver will still see the series combination of R_C and R_D across its inputs. Receiver failsafe can, therefore, still be supported. The short condition just described yields another benefit of failsafe termination. The increased impedance between V_{CC} and ground, with the addition of R_C and R_D, also results in increased fault or short circuit current limiting.

While the addition of R_C and R_D improves the transmission line's ability to withstand larger common mode voltages, it might also negatively impact the receiver's sensitivity. Consider, for example, a TIA/EIA-422 receiver. The minimum differential input signal (V_{ID}) required to switch the receiver is normally |200 mV|. Depending on the values of R_C and R_D, it may be necessary to develop a minimum of +400 mV across R_T in order to ensure that there is at least 200 mV across the receiver input terminals. The other significant disadvantage with failsafe termination may be the number of resistors required to implement it. Five resistors per line may prove too costly.

Bi-Directional Termination

The last type of termination which will be discussed is known as bi-directional termination. *Figure 11* illustrates a typically multipoint application composed of drivers, receivers, and transceivers. Bi-directional termination is parallel termination carried one step further. Bi-directional termination now permits multiple drivers (multipoint configuration) to be connected to the same twisted pair. With multiple drivers connected to the same twisted pair, data can now be transmitted in two directions. Keep in mind, however, that while data transmission can now take place in two directions, only half duplex transmission is allowed (as defined by TIA/EIA-485 standard). Multiple TIA/EIA-485 drivers cannot simultaneously drive the line since this would result in line contention. It should be mentioned that system timing should be

Bi-Directional Termination (Continued)

carefully inspected to ensure that line contention does not occur. The advantages in using bi-directional termination are almost identical to those with parallel termination.

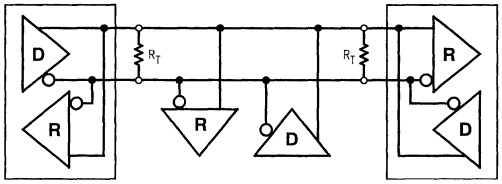


FIGURE 11. Bi-Directional Termination Configuration

These advantages include the prevention of signal reflections, and the ability to drive long transmission lines at high data rates As with parallel termination, R_T should be selected so that it matches the characteristic impedance (Z_O) of the twisted pair cable.

The disadvantages in using parallel termination also extend to bi-directional termination. Receiver failsafe cannot be guaranteed due to the interaction between R_T and the receiver's open circuit failsafe network. Stub lengths must be minimized and an R_T must each be placed at both extreme ends of the line in order to minimize transmission line effects. However, when two termination resistors are placed at the far ends of the cable, the effective load of the driver is now 60Ω (since R_T is typically 120Ω). This "doubling" of the driver load, using bidirectional termination, has two effects. First, it places a greater demand upon the driver's ability to source current. As described above, a multipoint driver must be able to source approximately twice the amount of current that is required from a multidrop driver. A driver expected to meet this increased current demand naturally experiences greater power dissipation. And second, noise margin tends to be reduced since the driver's output levels tend to decrease with increased loading.

Conclusion

The advantages and disadvantages of unterminated lines and those with series, parallel, AC, power, failsafe, and bi-directional terminations were contrasted. It should now be clear that there is no one termination scheme which is suited for all applications. *Table 1* provides a summary of the differential termination options discussed in this application note.

TABLE 1. Termination Summary

Termination	Signal Quality	Data Rate	Comments
Unterminated	Poor	Low	Low Power
Series	Good	Low	Low Power
Parallel	Excellent	High	Single Resistor
AC	Good	Med.	Ideal for use on control lines
Power	Excellent	High	Failsafe bias for idle line
Alt. Failsafe	Excellent	High	Failsafe for open, shorted, and idle lines
Bi-Directional	Excellent	High	Ideal for bidirectional half duplex operation

The termination scheme used will essentially be dictated by the needs of the system. Specifically, the choice of termination will depend upon the system's data transmission requirements.

Special Notes

The waveforms illustrated in this application note were acquired from laboratory testing of TIA/EIA-422 (RS-422) Drivers, and Receivers under the following conditions:

- DS26LS31 Quad Differential Driver
- DS26LS32A Quad Differential Receiver
- Cable = 100', 24AWG, 100Ω, twp cable (Berk-Tek #520382)
- Driver input signal with f = 500 kHz, V_{IH} = 3.0V, V_{IL} = 0V, Duty cycle = 50%
- V_{CC}= 5.0V
- T_A= 25°C

The cable selected for this testing was supplied by Berk-Tek Inc. and represents a typical twisted pair cable commonly used in TIA/EIA-422 applications. Additional information on cables can be obtained from:

Berk-Tek Inc.
132 White Oak Road
New Holland, PA 17557
(717) 354-6200

The RS-422-A standard was developed by the Technical Recommendation (TR30.2) TIA/EIA committee on DTE-DCE Interfaces. Since publication of the revision A, the EIA (Electronic Industries Association) has aligned with the TIA (Telecommunications Industry Association), and future revisions and new standards carry the TIA/EIA prefix, replacing the familiar "RS" (for Recommended Standard) prefix. Revision "B" of RS-422-A is expected in late 1993, and will become TIA/EIA-422-B.

References

Transmission Line Characteristics,
B. Fowler, National Semiconductor, Application Note AN-108.

Data Transmission Lines and Their Characteristics,
K. True, National Semiconductor, Application Note AN-806.

Reflections: Computations and Waveforms, K. True,
National Semiconductor, Application Note AN-807.

FAILSAFE Biasing of Differential Buses,
J. Goldie, National Semiconductor, Application Note AN-847.

Common Data Transmission Parameters and their Definitions

National Semiconductor
Application Note 912
John Goldie

Overview

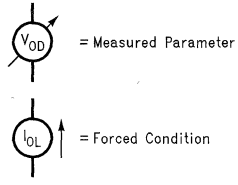
The scope of this application note is to introduce common data transmission parameters and to provide their definitions. This application note is subdivided into five sections, which are:

- Voltage Parameters
- Current Parameters
- Timing Parameters
- Miscellaneous Parameters
- Truth Table Explanations

Each parameter definition typically includes the following information: symbol, full name, description of measurement, measurement diagram, and a list of alternate names where applicable. Due to historical reasons (Fairchild origin, National origin, second sourcing, etc.) some devices use alternate symbols for the same parameters. Whenever possible, a list of common alternate symbols is provided for cross reference. New and future devices from National's Data Transmission Products Group will use the parameters as described in this application note for consistency and clarity reasons and to limit confusion.

This application note will be revised to add new parameters as required by new product definition.

In this application note the following symbols are used in test circuit diagrams. The measured parameter symbol represents a PMU—Precision Measurement Unit located at the test points illustrated in the test circuit. The PMU symbol also includes the parameter's name that is under test. The forced condition represents a forced voltage or current which is required to make the parameter measurement. Once again, it includes the parameter symbol that is being forced.



Voltage Parameters

INPUT VOLTAGE PARAMETERS

V_{CL}—Input Clamp Voltage. An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

V_{CM}—Common Mode Voltage. The algebraic mean of the two voltages applied to the referenced terminals, for example the receiver's input terminals. This voltage is referenced to circuit common (ground). This parameter is illustrated in *Figure 1* along with its mathematical equation.

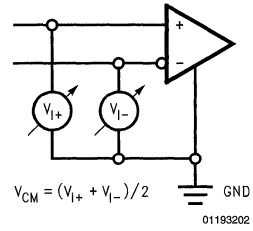


FIGURE 1. Common Mode Voltage

V_{DIFF}—Differential Input Voltage. The potential difference between the input terminals of the device (receiver) with respect to one of the inputs (typically the inverting input terminal). This parameter may be a positive or negative voltage, and commonly specifies the minimum operating voltage and the absolute maximum differential input voltage. See *Figure 2*. V_{DIFF} is also known as V_{ID} for input differential voltage.

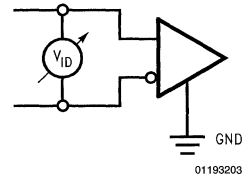


FIGURE 2. Differential Input Voltage

V_{IH}—High-Level Input Voltage. An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables. For example an input voltage between 2.0V and 5.0V in the case of standard TTL logic.

Note: A minimum is specified that is the least positive value of the high-level input voltage for which operation of the logic element within specification limits is guaranteed

V_{IL}—Low-Level Input Voltage. An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables. For example an input voltage between 0.0V and 0.8V in the case of standard TTL logic.

Note: A maximum is specified that is the most positive value of the low-level input voltage for which operation of the logic element within specification limits is guaranteed

V_{TH}—Positive-Going Threshold Voltage. The voltage level at a transition-operated input that causes operation of the logic element according to specification, as the input voltage rises from a level below the negative-going threshold voltage, V_{TL}. See *Figure 3*. Note that V_{TH} has also been

Voltage Parameters (Continued)

used in the past to specifiy both thresholds in one parameter. In this case, V_{TH} represents the Threshold Voltages and supports a minimum and maximum limit, for example, ±200 mV.

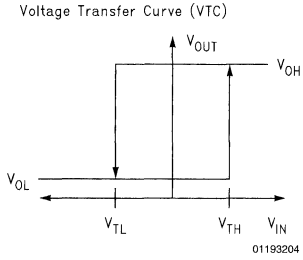


FIGURE 3. Threshold Voltages

V_{TL}—Negative-Going Threshold Voltage. The voltage level at a transition-operated input that causes operation of the logic element according to specification, as the input voltage falls from a level above the positive-going threshold voltage, V_{TH}. See *Figure 3* above

V_{HYS}—Hysteresis. The absolute difference in voltage value between the positive going threshold and the negative going threshold. See *Figure 4*. Hysteresis is the most widely symbolized parameter Alternate symbols include: V_{HY}, $V_{T+}-V_{T-}$, V_{HYST}, ΔV_{TH}, $V_{TH}-V_{TL}$, and V_{HST}.

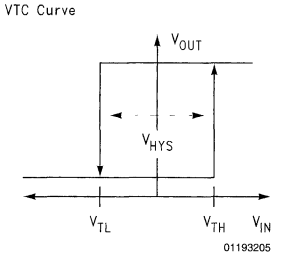


FIGURE 4. Hysteresis Voltage

Output Voltage Parameters

V_{OD}—Output Differential Voltage. The output voltage between the output terminals of a differential driver with input conditions applied that, according to the product specification, will establish a voltage level at the output. This voltage is measured with respect to the inverting output of the differential driver. V_{OD} is defined as the voltage at true output (A, $D_{OUT}+$, or DO) minus the voltage at the inverting output (B, $D_{OUT}-$, or DO*). Commonly an alpha-numeric suffix is added to designate specific test conditions. For example the case of different resistive loads. Also a star "*" or over-score bar is used with the parameter to designate the parameters' value with the opposite input state applied. This parameter has also been designated Terminated Output Voltage (V_T) in some datasheets.

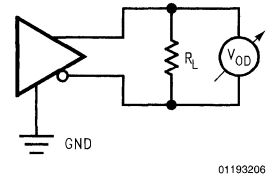


FIGURE 5. V_{OD} Test Circuit

ΔV_{OD}—Output Voltage Unbalance. The change in magnitude of the differential output voltage between the output terminals of a differential driver with opposite input conditions applied ΔV_{OD} is defined as: $\Delta V_{OD}=|V_{OD}|-|V_{OD}{}^*|$.

V_{OH}—High Level Output Voltage. The output voltage at an output terminal with input conditions applied that, according to the product specification, will establish a logic high level at the output. This voltage is measured with respect to circuit common (ground) See *Figure 6*.

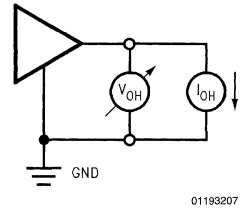


FIGURE 6. V_{OH} Test Circuit

V_{OL}—Low Level Output Voltage. The output voltage at an output terminal with input conditions applied that, according to the product specification, will establish a logic low level at the output. This voltage is measured with respect to circuit common (ground). See *Figure 7*

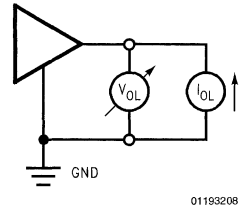


FIGURE 7. V_{OL} Test Circuit

V_{OS}—Offset Voltage. The center point output voltage between the output terminals of a differential driver with input conditions applied that, according to the product specification, will establish a voltage level at the output. This voltage

Output Voltage Parameters

(Continued)

is measured with respect to the driver's circuit common (ground). Commonly a star "*" or over-score bar is used with the parameter to designate the parameter's value with the opposite input state applied (see *Figure 8*). This parameter is also referred to as V_{OC}—Common Mode Voltage.

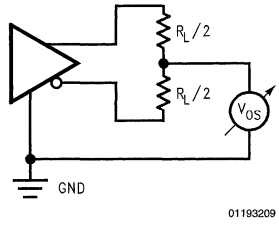


FIGURE 8. V_{OS} Test Circuit

ΔV_{OS}—Offset Voltage Unbalance. The change in magnitude of the offset voltage at the output terminals of a differential driver with opposite input conditions applied. ΔV_{OS} is defined as:

$$\Delta V_{OS}=|V_{OS}|-|V_{OS}^*|.$$

V_{SS}—Steady State Output Voltage. The steady state differential output voltage is defined as $|V_{OD}|+|V_{OD}^*|$. This is typically a calculated parameter only, based on the formula shown above. The V_{OD} parameter is defined above and illustrated in *Figure 5*. V_{SS} is equal to twice the magnitude of V_{OD} and is shown in *Figure 9*.

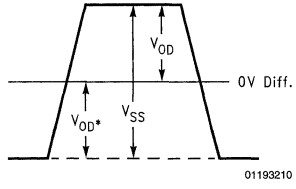


FIGURE 9. Differential Output Steady State Voltage

V_T—Terminated Output Voltage. The output voltage at an output terminal with input conditions applied that, according to the product specification, will establish a known logic level at the output. This voltage is measured with respect to circuit common (ground) with a stated resistance, and may be a positive or negative voltage. This parameter is typically used in conjunction with single-ended (unbalanced) line drivers. See *Figure 10*.

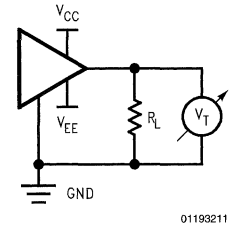


FIGURE 10. V_T Test Circuit

ΔV_T—Terminated Output Voltage Unbalance. The change in magnitude of the terminated output voltage at the output terminal of a single-ended line driver with opposite input conditions applied. ΔV_T is defined as:

$$\Delta V_T=|V_T|-|V_T^*|.$$

Current Parameters

Note: Current is specified as magnitude value only, with the sign denoting the current direction only A negative sign defines current flowing out of a device pin, while a positive sign defines current flowing into a device pin The largest current limit is specified as a maximum, and zero (0) by default is the smallest minimum All future DTP datasheets will follow this convention, and only some existing datasheets follow this convention

I_{IH}—High-Level Input Current. The current into (out of) an input when a high-level voltage is applied to that input. Note that current out of a device pin is given as a negative value. Typically this parameter specifies a positive maximum value for bipolar devices.

I_{IL}—Low-Level Input Current. The current into (out of) an input when a low-level voltage is applied to that input. Note that current out of a device pin is given as a negative value.

I_I—Maximum Input Current. The current into (out of) an input when the maximum specified input voltage is applied to that input. Note that current out of a device pin is given as a negative value.

I_{IN}—Input Current. The current into (out of) a receiver input when a specified input voltage, or voltage range is applied to that input. Note that current out of a device pin is given as a negative value. This parameter is typically tested at the maximum voltage specified for the input. For differential receivers the other input (not under test) is held at 0V (in the case of RS-422/3 and 485 receivers).

I_{ING}—Input Current, Power Up Glitch. The current into (out of) an input when a specified input voltage, or voltage range is applied to that input. Note that current out of a device pin is given as a negative value. This parameter applies to transceivers (RS-485) only, and is actually specifying the driver's performance at a specific power supply

Current Parameters (Continued)

level. Additionally the driver is biased such that it is enabled, with the specified power supply voltage applied. This parameter assures that the driver is disabled by an internal circuit at the specified power supply level, even though the enable pin is active. If the driver was enabled, I_{OS} current would be observed, instead of the combined measured current of driver TRI-STATE® leakage (I_{OZ}) plus receiver input current (I_{IN}). For example V_{CC}=3.0V is commonly referenced to represent a single point in a power up/down cycle (See AN-905 for more information on this parameter).

I_{OS}—Output Short Circuit Current. The current into (out of) an output when that output is short-circuited to circuit common (ground) or any other specified potential, with input conditions as noted, typically such that the output logic level is the furthest potential from the applied voltage. This parameter commonly includes an identifying suffix. For example I_{OSD} represents the output short circuit current of a driver, while I_{OSR} represents the receiver's output short circuit current. Output short circuit current is also designated by the following symbols: I_{O+}, I_{SC}, and I_S. See *Figure 11.*

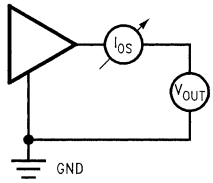


FIGURE 11. I_{OS} Test Circuit

I_{OZ}—TRI-STATE Output Current. The current into (out of) a TRI-STATE output having input (control) conditions applied that, according to the product specification, will establish a high impedance state at the output. This parameter commonly includes an identifying suffix. For example, I_{OZD} represents the TRI-STATE output current of a driver, while I_{OZR} represents the receiver's TRI-STATE output current. In addition I_{OZH} and I_{OZL} are also commonly used and denote the forced voltage (logic) level. See *Figure 12.*

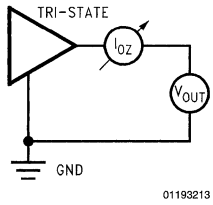


FIGURE 12. I_{OZ} Test Circuit

I_{OX}—Power Off Leakage Current. The current flowing into (out of) an output with input conditions applied that, according to the product specification, will establish a high impedance state at the output. Commonly a known state is required on the power supply pin as an input condition. For example, power supply terminal (V_{CC}) equal to zero volts may be a required condition of an I_{OX} parameter. See *Figure 13.*

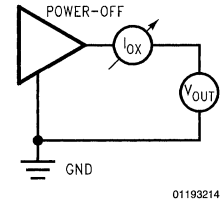


FIGURE 13. I_{OX} Test Circuit

I_{OD}—Differential Output Current. The current flowing between the output terminals of a differential line driver with an external differential load applied that, according to the product specification, will establish a known state at the output. See *Figure 14.*

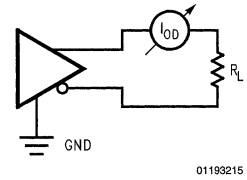


FIGURE 14. Differential Output Current

I_{OH}—High-Level Output Current. The current into (out of) an output terminal with input conditions applied that, according to the product specification, will establish a logic high level at the corresponding output. Note that current out of a terminal is given as a negative value.

I_{OL}—Low-Level Output Current. The current into (out of) an output terminal with input conditions applied that, according to the product specification, will establish a logic low level at the corresponding output. Note that current out of a terminal is given as a negative value.

I_{CC}—Supply Current. The current into the V_{CC} supply terminal of the integrated circuit. Normally the parameter is measured with all loads removed. It may also include a suffix that denotes that state of the device. For example:

I_{CCD}= Power Supply Current
(drivers enabled, receivers disabled)

I_{CCR}= Power Supply Current
(receivers enabled, drivers disabled)

I_{CCZ}= Power Supply Current
(drivers and receivers disabled)

I_{CCX}= Power Supply Current
(sleep or shutdown mode)

I_{EE}—Supply Current. The current into the V_{EE} supply terminal of the integrated circuit. Normally the parameter is measured with all loads removed. It may also include a suffix that denotes that state of the device. Note that current out of

Current Parameters (Continued)

a terminal is given as a negative value. For example:

I_{EED}= Power Supply Current
(drivers enabled, receivers disabled)

I_{EER}= Power Supply Current
(receivers enabled, drivers disabled)

I_{EEZ}= Power Supply Current
(drivers and receivers disabled)

I_{EEX}= Power Supply Current
(sleep or shutdown mode)

Timing Parameters

t_{PLH}—Propagation Delay Time, Low-to-High-Level Output. The time between specified reference points on the input and output voltage waveforms with the output changing from a logic low level to a logic high level.

t_{PHL}—Propagation Delay Time, High-to-Low-Level Output. The time between specified reference points on the input and output voltage waveforms with the output changing from a logic high level to a logic low level.

t_{SK}—Propagation Delay Skew. The magnitude difference between complementary propagation delays. Skew is defined as $|t_{PLH}-t_{PHL}|$. This specification is a per channel parameter unless specified otherwise.

t_{PLHD}—Differential Propagation Delay Time, Low-to-High-Level Output. The time between specified reference points on the input and output differential voltage waveforms with the output changing from a logic low level to a logic high level.

t_{PHLD}—Differential Propagation Delay Time, High-to-Low-Level Output. The time between specified reference points on the input and output differential voltage waveforms with the output changing from a logic high level to a logic low level.

t_{SKD}—Differential Propagation Delay Skew. The magnitude difference between complementary differential propagation delays. Skew is defined as $|t_{PLHD}-t_{PHLD}|$. This specification is a per channel parameter unless specified otherwise.

t_{PZH}—Output Enable Time. The propagation delay time between the specified reference points on the input (control) and output voltage waveforms with the TRI-STATE output changing from a high impedance (off) state to a logic high level.

t_{PZL}—Output Enable Time. The propagation delay time between the specified reference points on the input (control) and output voltage waveforms with the TRI-STATE output changing from a high impedance (off) state to a logic low level.

t_{PHZ}—Output Disable Time. The propagation delay time between the specified reference points on the input (control) and output voltage waveforms with the TRI-STATE output changing from logic high level to a high impedance (off) state.

t_{PLZ}—Output Disable Time. The propagation delay time between the specified reference points on the input (control) and output voltage waveforms with the TRI-STATE output changing from logic low level to a high impedance (off) state.

t_{PSH}—Propagation Delay Time, Sleep-to-High-Level Output. The propagation delay time between the specified reference points on the input (control) and output voltage waveforms with the output changing from an off state to a logic high level.

t_{PSL}—Propagation Delay Time, Sleep-to-Low-Level Output. The propagation delay time between the specified reference points on the input (control) and output voltage waveforms with the output changing from an off state to a logic low level.

t_{PHS}—Propagation Delay Time, High-Level Output to Sleep. The propagation delay time between the specified reference points on the input (control) and output voltage waveforms with the output changing from logic high level to an off state.

t_{PLS}—Propagation Delay Time, Low-Level Output to Sleep. The propagation delay time between the specified reference points on the input (control) and output voltage waveforms with the output changing from logic low level to an off state.

t_r—Rise Time. The time between two specified reference points on an input waveform, normally between the 10% and 90% or the 20% and 80% points, that is changing from low to high. Note, also commonly specified as transition time (t_{TLH}).

t_f—Fall Time. The time between two specified reference points on an input waveform, normally between the 10% and 90% or the 20% and 80% points, that is changing from high to low. Note, also commonly specified as transition time (t_{THL}).

t_{TLH}—Transition Time Low to High. The time between two specified reference points on an input waveform, normally between the 10% and 90% or the 20% and 80% points, that is changing from low to high. Note, also commonly specified as rise time (t_r).

t_{THL}—Transition Time High to Low. The time between two specified reference points on an output waveform, normally between the 10% and 90% or the 20% and 80% points, that is changing from high to low. Note, also commonly specified as fall time (t_f).

t_{NW}—Noise Pulse Width. The width in time of a pulse applied to a device. The parameter is commonly specified with receivers that feature low pass noise filters. t_{NW} is the pulse width assumed to be noise and guaranteed to be rejected.

Miscellaneous Parameters

SR—Slew Rate. The time between two specified reference points on an output waveform, normally between the ±3V level for TIA/EIA-232 (RS-232) drivers, divided by the voltage difference. Note, this parameter is normally specified in Volts per microsecond (V/µs). A suffix may be added to denote different loading conditions.

R_{IN}—Input Resistance. The slope of the input voltage vs. input current curve of an input when a specified voltage range is applied to that input and the current is measured. Note, that two points must be measured for the parameter to be calculated correctly as R_{IN} is defined as $\Delta V/\Delta I$ not V/I.

R_{OUT}—Output Impedance. The resulting output impedance calculated from measured currents at applied voltages.

Truth Table Explanantions

Symbols generally associated with functional truth tables are listed below:

H or 1 = Logic High Level (steady state)

Truth Table Explanantions (Continued)

L or 0 = Logic Low Level (steady state)

Z = TRI-STATE® (high impedance off state)

X = irrelevant (input, including transitions)

References

ALS/AS IC Device Testing, ALS/AS Logic Databook. National Semiconductor Corp., 1990

Glossary of Terms, ALS/AS Logic Databook. National Semiconductor Corp., 1990

Understanding Power Requirements in RS-232 Applications

National Semiconductor
Application Note 914
Syed Huq

Introduction

As the popularity of asynchronous serial communication became widely accepted by the industry, the RS-232 standard gained very wide acceptance. The use of this standard is visible in almost all Industrial, Portable, Desktop, Data Acquistion and Test Measurement applications using a serial port for communication. Even though the standard specifies a maximum data rate for RS-232 of 20 kbps, some applications need for higher speed is overwhelming. More and more applications today require at least 120 kbps to support Laplink®, a popular communication software used by Laptop/Desktop computers for fast file transfer between two computers. RS-232 type Drivers and Receivers must also support this higher data rate to be Laplink compatible.

This application note covers the RS-232 circuit functions, an explanation of hardware handshaking, a step by step analysis of the hardware handshaking between a local and remote terminal, and power requirements/dissipation of the DS14C335.

RS-232 Handshaking Circuits

In a Terminal (DTE-Data Terminal Equipment) to Modem (DCE-Data Circuit Terminating Equipment) application, as shown in *Figure 2*, commonly only eight dedicated lines are required. Even though the standard defines a 25 pin connection, the de-facto 9 pin connector is very popular. These lines are DCD, RXD, TXD, DTR, DSR, RTS, CTS, RI and GND and are shown in *Figure 1*. Lets take a quick look at these dedicated lines along with their respective functions. Note that ON is defined as a positive voltage and OFF is a negative voltages on the cable.

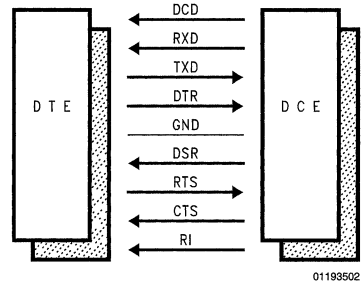


FIGURE 1. Direction of Flow from DTE/DCE

DCD: Data Carrier Detect (DCE to DTE)

When this circuit is OFF locally, it indicates to the local terminal that the remote DTE has not switched its RTS circuit ON yet and the local terminal can gain control over the carrier line if needed. When this circuit is ON locally, it indicates to the local terminal that the remote modem has received a RTS ON condition from its terminal and the remote DTE is in control over the carrier line.

RXD: Receive Data (DCE to DTE)

Receive data circuit from modem to DTE.

TXD: Transmit Data (DTE to DCE)

Transmit data circuit from DTE to modem.

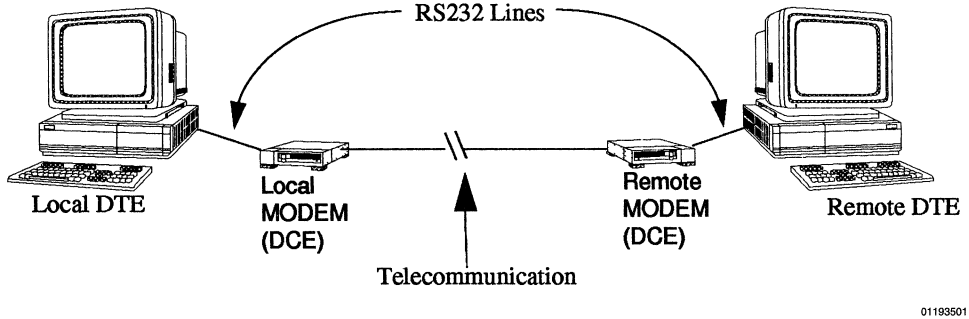


FIGURE 2. DTE to DCE Interface

DTR: Data Terminal Ready (DTE to DCE)

The DTR pin is generally ON when the terminal is ready to establish communication channel through its modem. By keeping the DTR circuit ON the DTE lets an *"auto answer"* modem accept the call unattended. The DTR circuit is OFF, only when the DTE does not want its modem to accept calls from remote locations. This is known as *local mode.*

DSR: Data Set Ready (DCE to DTE)

Both modems switch their DSR circuit ON when a communication path has been established between the two sites (local and remote modem).

RTS: Request To Send (DTE to DCE)

When a terminal is ready to transmit data, it switches the RTS circuit ON, indicating to the local modem that it is ready to transmit data. This information also gets passed to the remote modem. The RTS line controls the direction of data transmission. During transmit mode, the line is ON and during receive mode it's OFF.

CTS: Clear To Send (DCE to DTE)

When CTS switches ON, the local modem is ready to receive data from its DTE and the local modem has control over the telephone lines for data transmission.

RI: Ring Indicator (DCE to DTE)

When the modem receives a call, the RI circuit switches ON/OFF in sequence with the phone ringing informing the DTE that a call is coming in. This indicates that a remote modem is requesting a dial-up connection.

GND

Ground, signal common.

Hardware Handshake Flow

A step by step analysis of handshaking illustrates how each circuit is used to establish communication between a local and a remote site. To keep the subject simple, assumption has been made that transmission is from Local to Remote only.

1. Local DTE switches DTR ON and local modem dials the phone number of the remote modem.
2. If DTR at remote location is ON, the remote modem's RI turns ON/OFF in sequence with the phone ringing, indicating a call coming in.
3. The remote modem returns an answer-back tone to the local modem Upon detection of this tone, the local modem and the remote modem establishes the on-line connection. At this point both modems switch their DSR pins ON indicating that a connection has been established.
4. The local DTE switches RTS ON indicating that it is ready to send data. This signal gets passed on to the remote modems DCD circuit.
5. The local modem checks to make sure that local DCD is OFF, which indicates that the remote modem is not in control of the carrier line.
6. The local modem then switches CTS ON to the local DTE to inform that it can start sending data. Locally the DCD circuit stays OFF. On the remote modem DCD stays ON. RTS is held ON by the local DTE throughout the duration of the connection.
7. The local DTE sends data through TXD to modem for transmittal.
8. The remote modem receives the data and sends the data to its terminal via the RXD circuit.
9. When data transmittal is finished, local DTE drops RTS, which drops the DCD at remote modem and CTS at local modem. Transmission of data can be discontinued by hanging up the phone line, by the DTE dropping its DTR circuit, by disconnecting the modem cable from the DTE.
10. Now, either DTE is ready to start all over again and gain control of the telecommunication line.

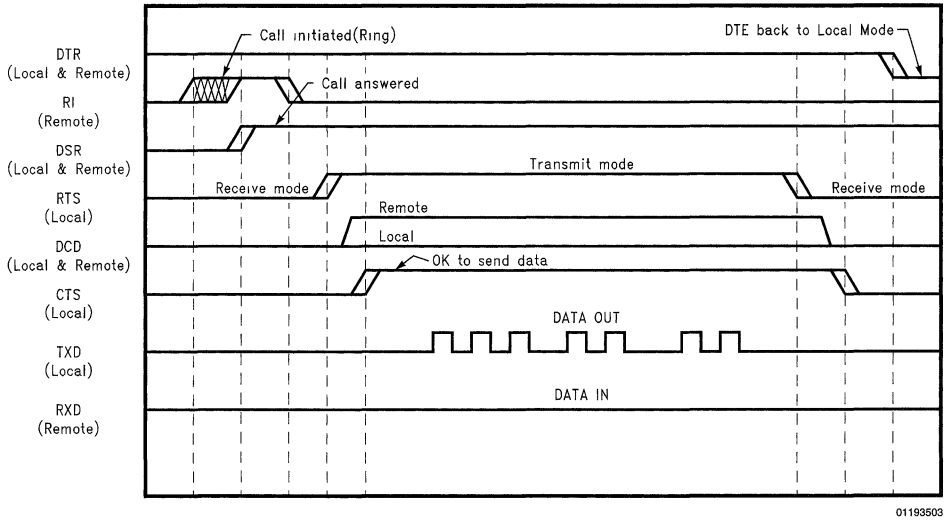


FIGURE 3. Graphical Illustration of Hardware Handshaking

Hardware Handshake Flow (Continued)

From the above explanations, in half-duplex communication, we can derive that in transmit mode, only one driver (TXD) is switching (up to 120 kbps) while the other drivers/receivers are at some known steady state (not switching). Similarly, on a receive mode, only one receiver (RXD) is switching while other lines maintain known steady state levels.

Power Consumption

Based on the above observations, lets determine how I_{CC}, frequency, internal/external capacitance and load resistance play a role in power consumption for the DS14C335. Total power consumption is the static and the dynamic power combined. CMOS devices typically consume minimal power in a static condition. This can be calculated simply by multiplying I_{CC} with V_{CC}.

Under a loaded condition, the external loading of the driver directly effects the power dissipation of the device and application. The RS-232 driver is normally connected to a cable and a receiver at the far end. Since the transition time of the driver is set to be substantially longer than the cable delay, the cable load represents a lumped capacitive load and a series resistance. The series resistance on short cables (< 200 feet) can be neglected since it is very small compared to the receiver input resistance. This means the cable may be modeled as a lumped capacitive load equal to the capacitance per unit length multiplied by the length of the cable. 1000 pF is commonly used to represent a 20 foot cable, and 2500 pF is used as the maximum specified cable load. The receiver input resistance is specified to be between 3 kΩ and 7 kΩ, 5 kΩ is used as a typical, and 3 kΩ is the worst case from a power point of view. This equivalent load is illustrated in *Figure 4.*

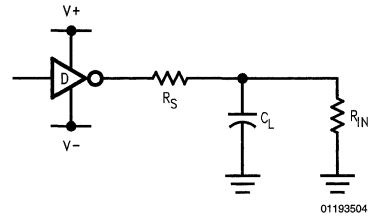


FIGURE 4. Load Seen by the Driver

Where: R_S = Cable series resistance.

C_L = Cable load capacitance.

R_{IN} = Input resistance of the Receiver.

A channel that is in a steady state is loaded by the receivers input impedance since the cable capacitance has charged up. The output current of the driver is determined by the output voltage of the driver (V_{OH} or V_{OL}) divided by the input resistance of the receiver. For example, a 7V level, across the 3 kΩ load, requires 2.3 mA.

Dynamic power consumption has three major components. The switching current (spike current, also commonly called Conduction Overlap Current) during transitions, external load resistance and external load capacitance transient dissipation.

When the voltages to an NMOS/PMOS pair are in transition, both transistors turn on partially, creating a relatively low impedance path between the supply rails (V+ and V−). This is known as simultaneous conduction and is illustrated in *Figure 5.* As input frequency increases, the period decreases. At some point the output transistors fail to charge and discharge fully causing both upper and lower output transistor to stay on momentarily. This simultaneous conduction increases I_{CC} as the input signal's frequency is increased.

The charging and discharging of the large load capacitance C_L contributes to power consumption as well. The external load capacitance increases power in the same manner as the internal capacitance. A channel that is switching at speed is affected by all the components described previously. These new components contribute to the increased output current sourced or sunk by the driver to charge or discharge the capacitive load. This component of the load current will increase if the external capacitance is increased and also if the switching rate of the device is increased.

Power Consumption (Continued)

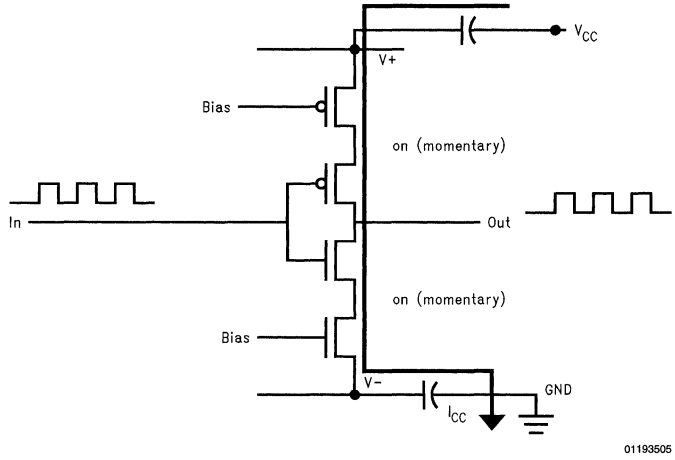


FIGURE 5. Simultaneous Conduction and I_{CC}

DS14C335 and Power Consumption

National's DS14C335 is a 3 X 5 Driver/Receiver combination providing a one-chip solution for a 9 pin RS-232 DTE application. *Figure 6* shows a worst case situation where all 3 drivers and 5 receivers are switching under different loading conditions. Under this worst case condition, at 10 kHz (20 kbps), supply current is 30 mA (2500 pF). Under a no load condition, supply current stays relatively flat. *Figure 7* shows a true RS-232 application where one driver (TXD) is switching while the other two are driver (DTR and RTS) remain High (loaded) as shown in *Figure 3*. At 10 kHz, supply current reads 26 mA (2500 pF), under this real world RS-232 application. Decreasing the capacitive load also decreases the supply current as shown in *Figure 7*. *Figure 8* illustrates one receiver (RXD) switching. Supply current is almost constant under this operating condition.

DS14C335 and Power Consumption (Continued)

DS14C335 Supply Current vs Frequency vs Driver Loads

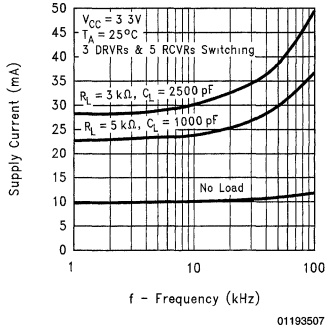


FIGURE 6. All Driver and Receiver Switching

DS14C335 Supply Current vs Frequency vs Driver Loads

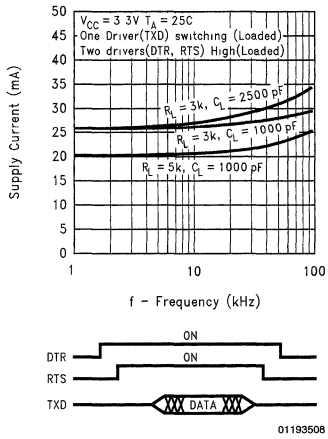


FIGURE 7. One Driver (TXD) Switching

DS14C335 Supply Current vs Frequency (Receiver)

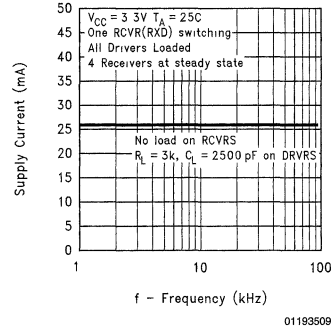


FIGURE 8. One Receiver (RXD) Switching

Looking at the Supply Power vs Data Rate (*Figure 9*) we can see that under multiple driver switching and at a maximum data rate of 120 kbps, the supply power is 120 mW (2500 pF load). With one driver switching and the other two driver output at High (RS-232 Application), the supply power at maximum data rate of 120 kbps drops to 103 mW (2500 pF load).

DS14C335 Supply Power vs Data Rate

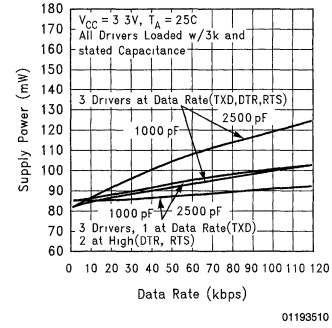


FIGURE 9. Supply Power vs Data Rate

The DS14C335 also offers a SHUTDOWN (SD) feature where the device can be de-activated by applying a logic High on the SD pin. This will lower the supply current to less than 1 µA (typical). In addition, in this mode one receiver (R5) remains active to monitor RI (Ring Indicator). This active receiver can sense incoming calls and inform the power management circuit to activate the device. SHUTDOWN mode saves battery life when the serial port is not used. In this mode, power dissipation is only 3.3 µW allowing battery charge to be used by other active circuitry.

Other Industry Standards (RS-232)

RS-562 is another standard that is gaining popularity in the Industry. RS-562 is compatible to RS-232, however, there are some trade-offs. *Table 1* illustrates a comparison and the major differences between the two standards.

Other Industry Standards (RS-232) (Continued)

TABLE 1. Comparison and Major Differences between RS-232 and RS-562

Specifications	RS-232	RS-562
Mode of Operation	Single-ended	Single-ended
Receiver Input Resistance (Ω)	3 kΩ to 7 kΩ	3 kΩ to 7 kΩ
Receiver Sensitivity	±3V	±3V
Driver Output Current (Powered Off, ±2V)	±6.67 mA (300Ω)	±6.67 mA (300Ω)
Driver Output Short Circuit Current Limit	**≤100 mA**	**≤60 mA**
Number of Drivers and Receivers Allowed	1 Driver 1 Receiver	1 Driver 1 Receiver
Max Cable Length	~50' (2500 pF)	2500 pF (20 kbps) 1000 pF (64 kbps)
Max Data Rate	**20 kbps**	**64 kbps**
Driver Output	**±5V Min** **±15V Max**	**±3.7V Min** **±13.2V Max**
Driver Load	3 kΩ to 7 kΩ	3 kΩ to 7 kΩ
Driver Slew Rate	≤30 V/μs	≤30 V/μs

Even though RS-562 standard specifies data rates greater than RS-232, the DS14C335 (RS-232) far exceeds the 64 kbps of RS-562. The most significant difference between the two standards is the noise margin. As shown in *Figure 10*, RS-232 devices have a noise margin of 2V or greater. Typically for DS14C335, the noise margin is 4.5V (7.5V – 3V) whereas RS-562 has a noise margin as low as 700 mV (3.7V – 3V). A lower noise margin (RS-562) means limited rejection of external noise, crosstalk and ground potential differences which can all commonly occur in RS-232 type communication.

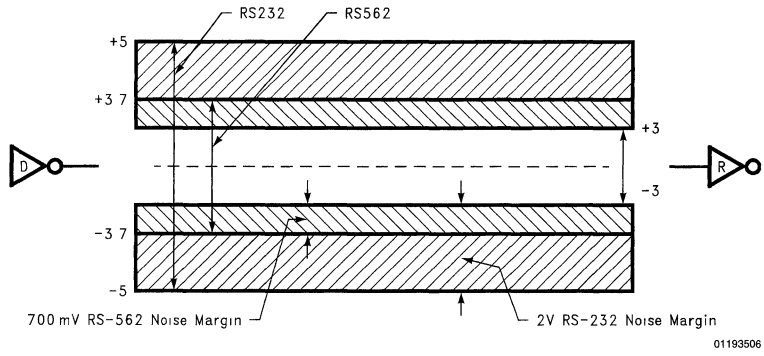


FIGURE 10. Noise Margin Comparison

Conclusion

Design Engineers are plagued with ground shift, noise problems and a noise margin of only 700 mV is not acceptable in many applications. RS-232 guarantees a 2V noise margin and Nationals DS14C335 is the preferred choice for applications requiring data rates pushing 120 kbps. Also, we have observed that in a half-duplex RS-232 DTE to DCE application, the supply current of the device is lower than simultaneous switching of all drivers and receivers as the application only requires one driver (TXD) or one receiver (RXD) switching at a time while the rest of the drivers/receivers maintain known steady state levels. Along with the power dissipation calculations, a discussion of the SHUTDOWN feature was also presented. This SHUTDOWN mode is highly desirable for any application that is battery powered, as it saves battery charge when the serial port is inactive.

References

Piecewise analysis and accurate emulation yield precise power estimates, William Hall and Ray Mentzer, National Semiconductor Corp., *EDN March 16, 1992.*

CMOS, the Ideal Logic Family, Stephen Calebotta, National Semiconductor Corp., *Application Note AN-77.*

References (Continued)

54C/74C Family Characteristics, Thomas P. Redfern, National Semiconductor Corp., *Application Note AN-90* .

HC-MOS Power Dissipation, Kenneth Karakotsios, National Semiconductor Corp., *Application Note AN-303* .

RS-232 Made Easy: Connecting Computers, Printers, Terminals and Modems, Martin D. Seyer.

Automotive Physical Layer SAE J1708 and the DS36277

National Semiconductor
Application Note 915
Michael Wilson
Todd Nelson

Introduction

Multiplex (MUX) wiring, or networking, has been introduced in automotive applications to address the increase in complexity and the number of onboard electronic devices in automobiles. Both standardized and proprietary solutions exist to address these issues. A standardized approach may be more desirable as cost and interoperability become important factors to consider for all original equipment manufacturers including automobile manufacturers.

The purpose of this application note is to give a general understanding of the J1708 recommended practice (SAE J1708) and the DS36277 transceiver which is optimized for use with SAE J1708. Additionally, this application note explains the significant differences between the DS36277 and a standard RS-485 transceiver, the DS75176B.

Explanation of Terms

Dominant Mode—This is a mode of operation in which one logic state is dominant over any other state on the bus.

Listen Mode—This is a mode of operation in which a receiver is always active (assuming the device is powered) and its output is always in a known state.

Definition of TIA/EIA-485 and SAE J1708

This section explains the definition of TIA/EIA-485 (RS-485) and SAE J1708. However, this section does not explain the electrical characteristic specifications of RS-485 or SAE J1708. The provisions for SAE J1708 will be discussed in the next section and for a brief definition of the RS-485 electrical specifications, refer to National application note AN-216.

First, RS-485 is an interface standard that specifies only electrical characteristics for balanced multipoint interface circuits. A complete interface standard will specify electrical, mechanical, and functional characteristics as does the popular interface standard TIA/EIA-232-E (see Table 1). Second, SAE J1708 specifies only the functional characteristics for balanced interface circuits. RS-485 is referenced by SAE J1708 for its electrical specifications but with a few modifications. Thus, the end designer of a SAE J1708 application must specify their own mechanical connections.

TABLE 1. Definition of RS-485 and SAE J1708

	Mechanical	Functional	Electrical
TIA/EIA-485			✓
SAE J1708		✓	REF. RS-485
TIA/EIA-232-E	✓	✓	✓

The SAE Recommended Practice J1708

The Society of Automotive Engineers (SAE) has defined this recommended practice for serial data communications between microcomputer systems in heavy duty vehicle applications. It is also well suited to passenger car applications (as shown in *Figure 1*) and many non-automotive uses. The bus is expected to be used for sharing data. An applications document, like SAE J1587 or SAE J1922, defines the actual data and/or functions to be transmitted. SAE J1708 only defines the hardware and basic software.

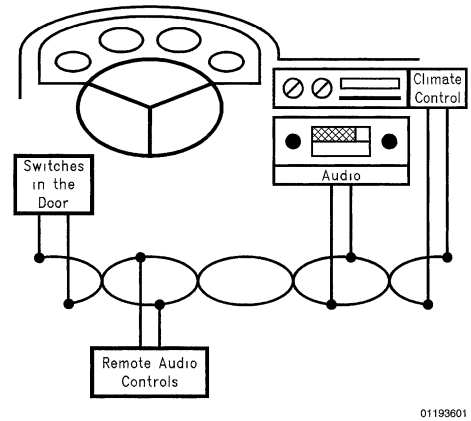


FIGURE 1. Automobile Controls on a SAE J1708 Bus

The physical media is a two-wire bus using 18-gauge twisted pair with a minimum of 1 twist per inch. The maximum length is intended to be 40m. A maximum of 20 nodes is specified. Deviations from this must be carefully analyzed to determine impact on bus performance over the entire operating range.

Each node may access the bus randomly once the bus is idle for a predetermined access time. If two or more nodes attempt to access the bus at the same time, the contending nodes must arbitrate for the bus. Arbitration is determined by priority, which is set between 1 (top priority) and 8. An applications document shall reference SAE J1708 and define the priority associated with each message. Since there can be up to 20 nodes, it is possible for two contending nodes to have the same priority. When contention exists between two or more nodes, arbitration is determined by the bus access time. This is the time a node is required to wait before it can attempt to access the bus.

The protocol is consistent with standard UART operation. A message consists of a Message Identification character (MID), a data character(s) and a checksum character. The total message length should not exceed 21 characters. A

The SAE Recommended Practice J1708 (Continued)

character is defined as 10 bits: the first bit is always the start bit (logic level LOW), followed by eight bits of data and, the tenth bit is the stop bit (logic level HIGH) (see *Figure 2*).

The bit timing equates to a baud rate of 9600. The logic LOW and HIGH levels are encoded as "dominant" and "recessive" which will be described later. The hardware is defined by the RS-485 standard for its electrical characteristics, with some exceptions and modifications.

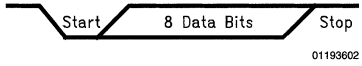


FIGURE 2. Character Format

J1708 Bus Loading

The recommended implementation for a SAE J1708 load is shown in *Figure 3* . The recommended implementation for a SAE J1708 system using a standard RS-485 transceiver, such as the DS75176B (see *Figure 4*), is shown in *Figure 7*. The circuitry between the bus and the transceiver differs from RS-485 and is intended to provide several features:

- R1 and R2 provide the bias for the "recessive" state.
- C1 and C2 combine to form a 6 MHz low pass filter, effective for reducing FM interference.
- R2, C1, R4 and C2 combine to form a 1.6 MHz low pass filter, effective for reducing AM interference.
- Since the bus is unterminated, at high frequencies R3 and R4 perform a pseudo-termination. This makes the implementation more flexible as no specific "termination nodes" are required at the ends of the bus.

The resistor and capacitor values are as follows and are shown in *Figure 3*:

Resistor 1 and 2 (R1 and R2)— 4.7 kΩ

Resistor 3 and 4 (R3 and R4)— 47Ω

Capacitor 1 and 2 (C1 and C2)— 2.2 nF

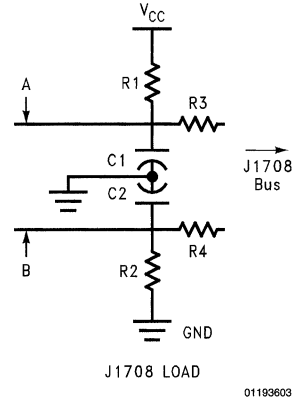


FIGURE 3. Node Load Circuit

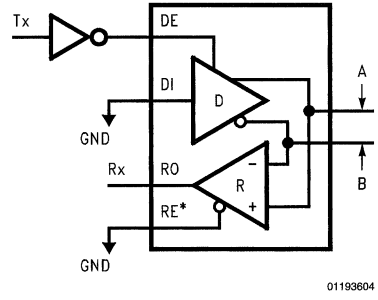


FIGURE 4. The DS75176B in a SAE J1708 Application

Dominant Mode

The drivers used by SAE J1708 are used in a dominant mode application. The driver's input (DI) is tied LOW and the signal (Tx) to be transmitted is tied to the driver's enable. The enable (DE) is active HIGH for the DS75176B while the enable (DE*) for the DS36277 is active LOW. First, this information is very important because this tells us that the driver is only capable of driving LOW. Therefore, a logic level LOW is encoded as "dominant". When the driver is disabled, the bus is pulled high by external bias resistors R1 and R2 (as shown in *Figure 3*). Thus, a logic level HIGH is encoded as "recessive". Second, if the driver's enable is active LOW, then you will transmit positive logic. But, if the driver's enable is active HIGH you will transmit negative logic. SAE J1708 is only defined for positive logic. Therefore, to implement a SAE J1708 application using DS75176B, which has an active HIGH driver enable, an inverter is needed for the driver enable (see *Figure 4* and *Figure 6*). However, the active LOW driver enable pin on the DS36277 saves the user an externally needed inverter (see *Figure 5*).

Dominant Mode (Continued)

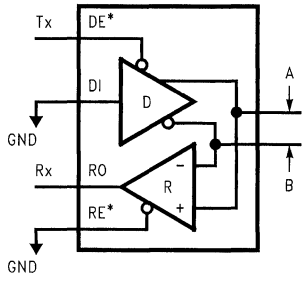


FIGURE 5. The DS36277 in a SAE J1708 Application

In the case of a SAE J1708 application, a logic LOW can overwrite a logic HIGH. Thus, if contention exists between two drivers with transmitting signals (Tx) in opposite states, the driver driving the "dominant" state wins.

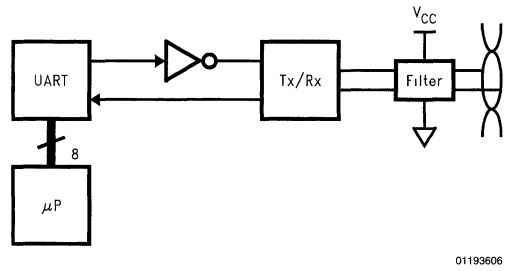


FIGURE 6. Typical SAE J1708 System Block Diagram

SAE J1708 requires all receivers to listen to every message identification character transmitted to determine if contention exists. Unlike the driver, the receiver's enable (RE*) is always tied LOW (see *Figure 4* and *Figure 5*). This means the receiver is always in listen mode (see Explanation of Terms).

The external components shown in *Figure 3* provide the necessary bias for a logic High "recessive" state. SAE J1708 requires no additional external components other than the J1708 load. This means that no parallel termination can be used at the ends of the SAE J1708 bus. The required loading also provides failsafe protection.

Features of the DS75176B

The DS75176B offers full compliance with the RS-485 standard and it is compatible with RS-422 and V.11. The device is available with industrial temperature range. Additionally, a thermal shutdown circuit protects the device against thermal overstress due to excessive power dissipation. Furthermore, the receiver has failsafe protection. However, the receiver's output is only guaranteed to be in a logic HIGH state for an open input line condition. The receiver also has ±200 mV threshold levels. The driver has an active HIGH enable while the receiver has an active LOW enable.

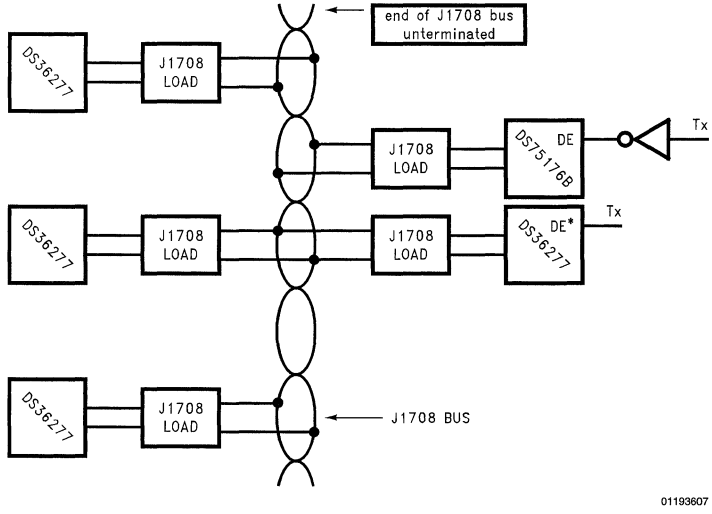


FIGURE 7. SAE J1708 Typical Bus Configuration and Loading

Features of the DS36277

The DS36277 is optimized for use with SAE J1708 electrical applications and the device is still compatible with RS-485, RS-422, and V.11 standards. Like the DS75176B, the device is available with industrial temperature range. Also the device includes thermal shutdown protection; plus the receiver has failsafe protection. Additionally, the receiver has full failsafe defenses that includes shorted and terminated line fault/conditions as well as open line conditions. The receiver's output is guaranteed to be in a logic HIGH state for all three line faults/conditions. The receiver's 0V to −500 mV threshold provides the protection from shorted line faults. Unlike the DS75176B, both the driver and the receiver have an active LOW enable.

The DS36277 also has a very rugged ESD structure that allows it to withstand electrostatic discharges (ESD) up to 7 kV (HBM). The device is also available in SOIC as well as DIP packages.

Conclusions

Selecting an established physical layer such as J1708 can eliminate many of the challenges of designing a serial communications system. The dominant mode operation allows for a non-destructive arbitration scheme.

J1708 is based on RS-485 electrical specifications and therefore benefits from the ruggedness, low cost and availability of compliant ICs already on the market.

The DS36277 transceiver has been optimized for J1708. It provides failsafe protection against bus faults and eliminates the need for an external inverter.

This application note provides a brief overview of the recommended practice and the interface standard. It is highly recommended to carefully review the complete documents. The documents can be obtained from:

SAE, 400 Commonwealth Dr.

Warrendale, PA 15096-0001

Global Engineering Documents

2805 McGraw Avenue

P.O. Box 19539

Irvine, CA 92174

References

1. EIA RS-485, Standard for *Electrical Characteristics of Generators and Receivers for use in Balanced Digital Multipoint Systems,* Electronic Industries Association Engineering Department. Washington D.C. 1983.

2. SAE J1708, *Serial Data Communications Between Microcomputer Systems In Heavy Duty Vehicle Applications.* Society of Automotive Engineers. 1990.

Popular Connector Pin Assignments for Data Communication

National Semiconductor
Application Note 917
John Goldie
Syed Huq

Introduction

This application note provides a graphical reference to popular connector pin assignments (pin outs) that are commonly used in telecom and computing applications.

In the field of data communication, the cable and connector play a critical part in the system's performance along with the line driver and receiver integrated circuits. Together the components (PCBs, ICs, cables, and connectors) form a channel, which all information must pass through. This channel forms a true chain, and a fault in any link may break the chain.

As stated in the introduction, this application note focuses on the connectors, and more specifically the pin assignments of the connectors. When equipment is built by a manufacturer and is intended to interwork with equipment from different manufacturers the use of an industry standard is critical. To properly inter-operate, the two pieces of equipment must support the same protocol (functional specifications), electrical levels, mechanical dimensions of the connector, and most importantly the connector's pin assignment. Since industry standards, TIA/EIA (Telecommunications Industry Association/Electronic Industries Association) for example, commonly specify or reference all three areas. Functional, Electrical, and Mechanical specifications, the chance of success is greatly increased when hooking up the two pieces of equipment.

A substantial amount of standardization work has been done in the telecommunications and computing area for interface standards. In addition to the connector pin outs, this application note also provides a short description of the standard or historical perspective. The reader is referenced to the actual standards from complete information on the standard.

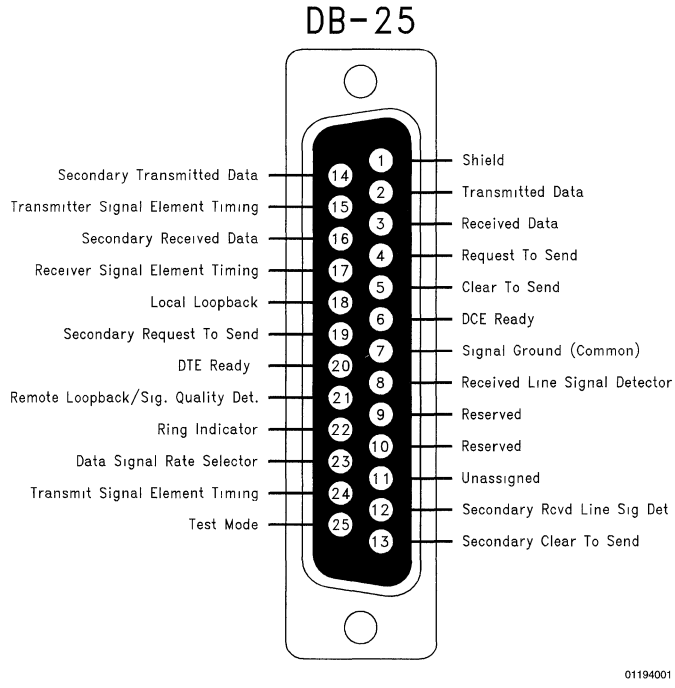


FIGURE 1. RS-232 DB-25

Introduction (Continued)

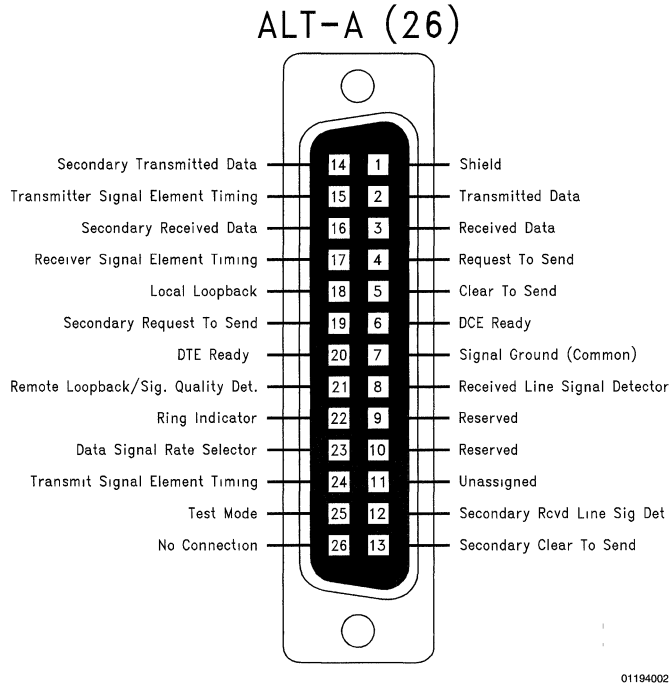


FIGURE 2. RS-232 ALT-A

RS-232

RS-232 is one of the most popular interface standards in the world. Originally intended for DTE/DCE interfacing, this standard has been used in a wide range of applications including telecom, computing, test and measurement, and industrial control applications. Now in its fifth revision (E), RS-232 is still very popular, and new devices (line drivers and receivers) are being developed to support the standard. The correct name of the standard is EIA/TIA-232-E which has replaced the more common RS-232 nomenclature. This standard specifies two connectors, the standard DB-25, also a new smaller alternate connector with 26 pins. The original version of RS-232 dates back to the early 1960s and is known as a complete standard as it specifies all functional, electrical, and mechanical specifications. There is also a very popular 9 pin defacto version of this standard commonly employed on personal computers that was developed by IBM®. The two full (25 line) connector pin outs are shown on *Figure 1* and *Figure 2*. See *Figure 7* for an illustration of the defacto 9 pin implementation, now standardized as EIA/TAI-574.

RS-449

RS-449 was intended to replace RS-232 at one time. It also specifies a DTE/DCE interface, but references the RS-422-A and RS-423-A standards for electrical specifications. This standard specified a DB-37 pin connector along with an additional DB-9 pin connector when additional lines were required. The 37 pin connector proved too large for many applications and limited the acceptance of this interface. RS-449 is mainly found in high-end telecom applications but rarely elsewhere. It has been replaced with a new standard that specifies the common DB-25 connector (EIA/TIA-530-A). The pin out of the DB-37 pin connector is shown in *Figure 3*.

RS-449 (Continued)

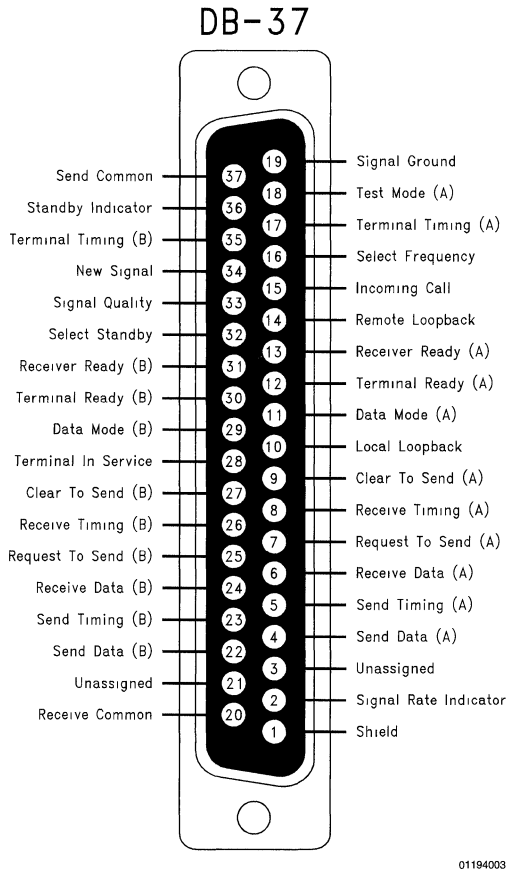


FIGURE 3. RS-449 DB-37

EIA-530 and EIA/TIA-530-A

EIA-530 is an extension of RS-449 but is based on the DB-25 connector. This standard specifies both functional and mechanical specifications, and references RS-422-A and RS-423-A standards for electrical specifications. This connector is the same one commonly used in EIA/TIA-232-E (RS-232) applications. This standard has been revised (denoted by the letter suffix — "A"), which altered the pin assignments slightly from EIA-530. Both pin assignments are shown in *Figure 4* and *Figure 5*.

EIA-530 and EIA/TIA-530-A (Continued)

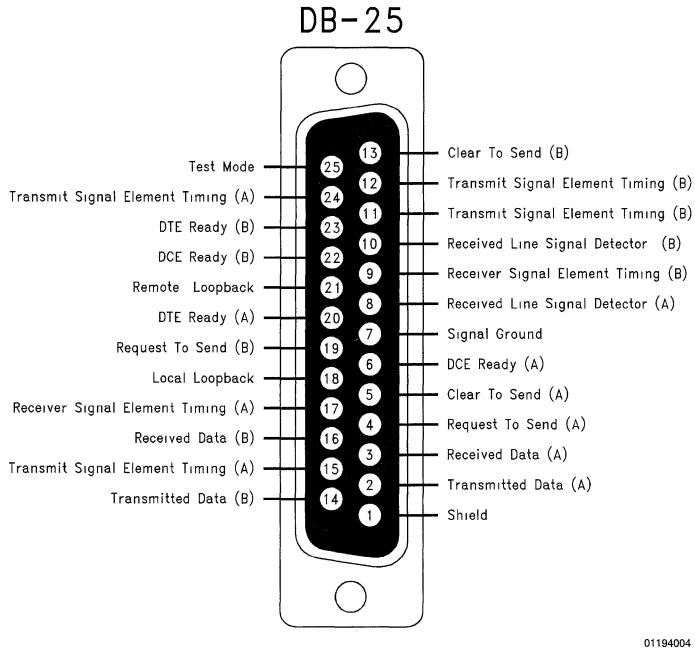


FIGURE 4. EIA-530 DB-25

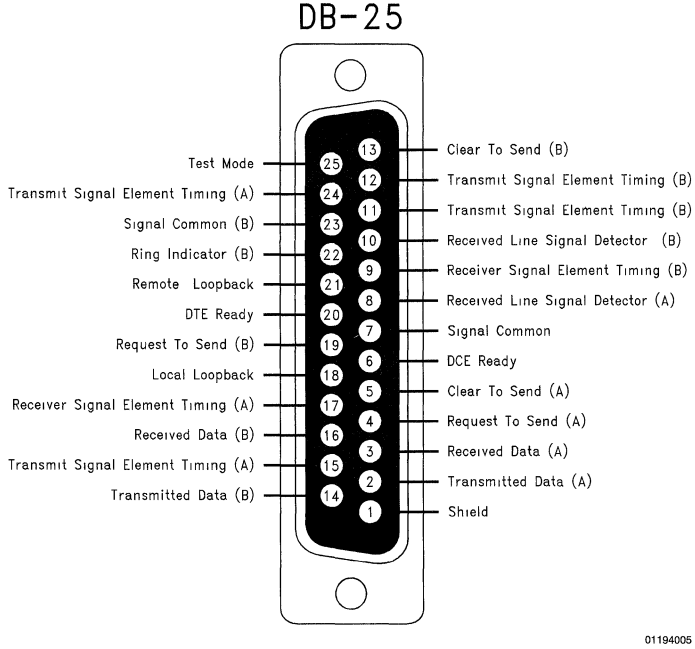
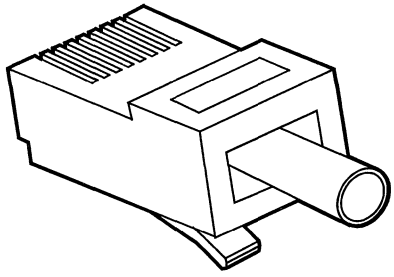


FIGURE 5. EIA/TIA-530-A DB-25

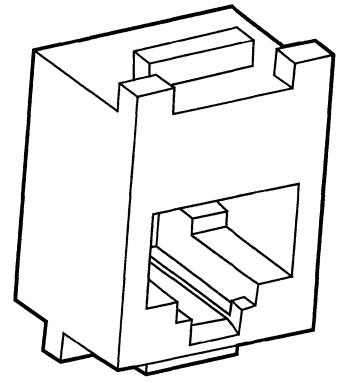
EIA/TIA-561

EIA/TIA-561 is a new standard released in 1990 and specifies a small 8 position interface for non-synchronous interface between DTEs and DCEs. The uniqueness of this standard is the fact that it does not specify a DB style connector, but rather a modular receptacle and plug type connector. This standard references the companion standard EIA/TIA-562 for electrical levels (similar to RS-232 but lower power and faster). The plug and jack are shown in *Figure 6.*

Several other pin out options for the MJ connector exist. Most of these are proprietary implementations. Check with the specifications for the equipment that is being interfaced to This will ensure inter-operation when employing an MJ connector.



Plug



Receptacle

01194006

1 Ring Indicator
2 Received Line Signal Detector
3 DTE Ready
4 Signal Common
5 Received Data
6 Transmitted Data
7 Clear to Send
8 Request to Send/Ready for Receiving

FIGURE 6. EIA/TIA-561 MJ-8

EIA/TIA-574

EIA/TIA-574 was developed due to confusion arising between the official RS-232 interface and the exceedingly popular defacto 9-pin version developed by IBM. This standard specifies the DB-9 interface, however, it recommends the use of the RS-562 standard instead of RS-232 electrical levels. It is noted that EIA/TIA-562 can inter-operate with RS-232 drivers and receivers in many applications. This standard supplies the minimum number of lines for non-synchronous serial data interchange between DTEs and DCEs The connector pin out is shown in *Figure 7.*

V.35

Recommendations V.35 was developed by the CCITT (International Telegraph and Telephone Consultative Committee) as a high speed modem standard that also specified the DTE/DCE interface. This standard used RS-232 type line drivers and receivers for control circuits, and its own unique differential drivers and receivers for high speed data and timing lines. This recommendation specifies a unique connector and is shown in *Figure 8.* It should also be noted that the CCITT has been replaced with the ITU (International Telecommunications Union) and new standards will adopt the ITU prefix instead of CCITT.

V.35 (Continued)

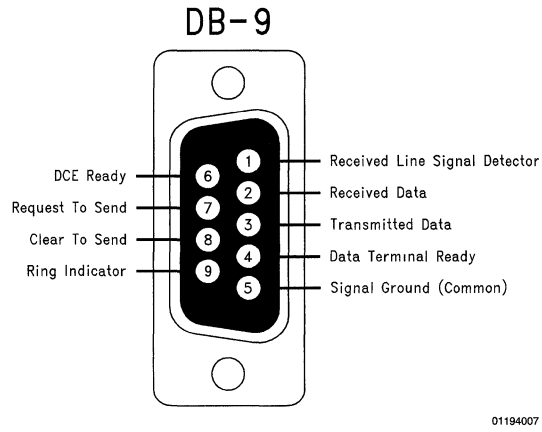


FIGURE 7. EIA/TIA-574 DB-9

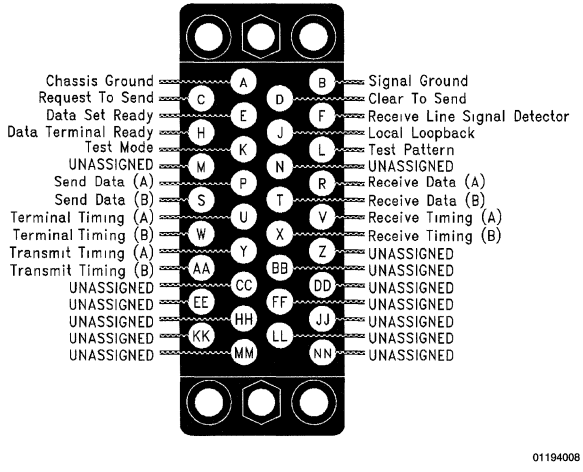


FIGURE 8. CCITT V.35

IEEE-488

The IEEE (Institute of Electrical and Electronic Engineers) also standardizes many interfaces in the area of computing and instrumentation. IEEE-488 is a complete standard specifying all functional, electrical, and mechanical specifications for a 16 line parallel bus for instrumentation. This interface is commonly found on test, and measurement equipment that feature computerized programming and control. This standard is also known under the acronym as GPIB (General Purpose Interface Bus). The pin out of the standardized connector is shown in *Figure 9*.

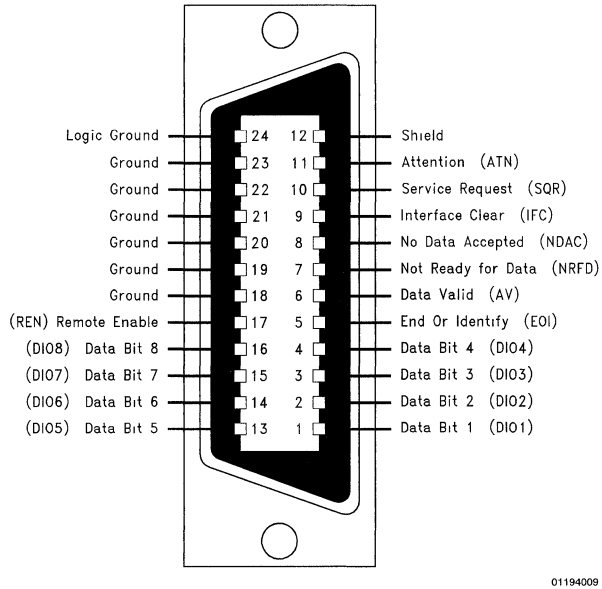


FIGURE 9. IEEE-488

Centronics Port and IBM PC Parallel Port

These two defacto standards both specify parallel interface that are commonly used in computing applications (computer to peripheral-printer). Both are defacto standards, and support similar functions but different pin outs and mechanical specifications. The IEEE has also defined a parallel port in the 1284 standard. It defines the 1284 connector and pin out (not shown here). The Centronics and IBM Parallel port pin outs are defined in the informational annexes of IEEE-1284. The two defacto connectors are shown in *Figure 10* and *Figure 11*.

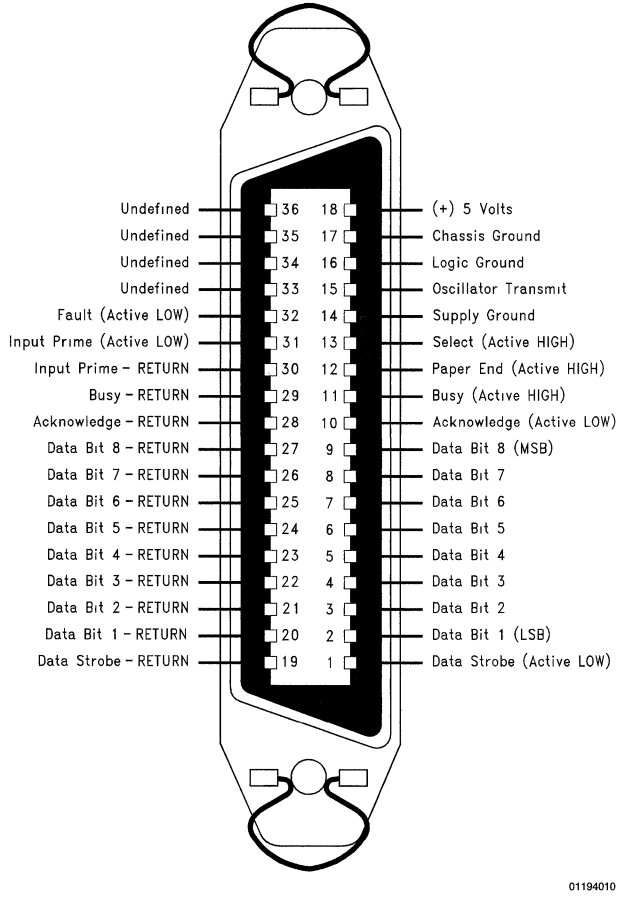


FIGURE 10. Centronics Port

Centronics Port and IBM PC Parallel Port (Continued)

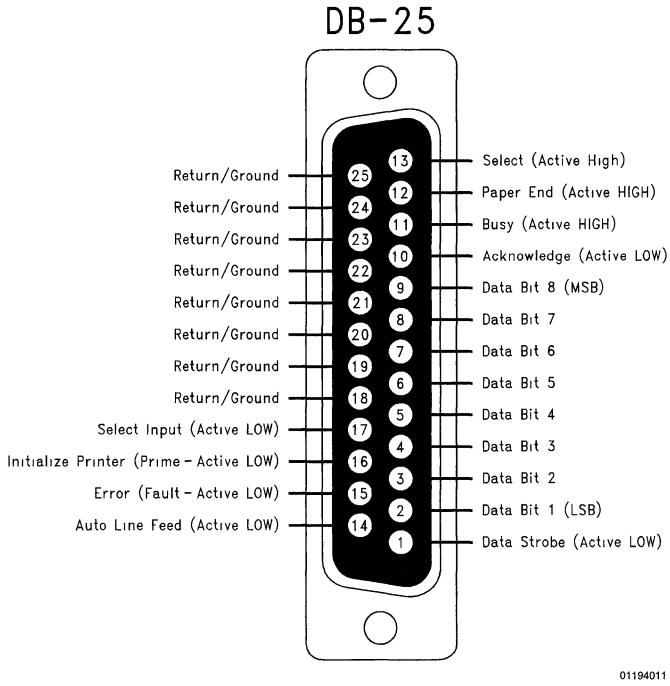


FIGURE 11. IBM PC Parallel Port

Summary

By selecting an industry standard, the problem of getting signals from one board or box to another is greatly reduced. This is especially true when inter-operation between systems built by different manufacturers is required (open system).

Interface standards from the TIA/EIA and other standards groups greatly resolve this interfacing problem. This application note provides insight into those standards by providing a graphical representation of the connectors referenced in the standards. As always, whenever designing a system to an industry standard, a thorough review of the most recent revision of the standard is highly recommended.

Reference

Most standards are available from:

Global Engineering Documents

15 Inverness Way East

Englewood, CO 80112-5704

303-397-7956 or 800-854-7179

http://global.ihs.com/

Various connector, cable and data communication products are available from:

South Hills Datacom

Pittsburgh, PA, USA

Toll-Free: 800-245-6215

Local: 412-921-9000

FAX: 412-921-2254

Inter-Operation of Interface Standards

National Semiconductor
Application Note 972
J. Goldie

Introduction

When communication is required between systems that support *different* interfaces is required, a detailed study of driver output and receiver input characteristics is required to determine if direct "electrical" inter-operation is possible. The results of this study may also conclude that some translation devices are required for inter-operation. This may include passive devices or active devices, and even perhaps a repeater circuit. This application note focuses on the simplest way to gain electrical inter-operation between devices conforming to different Interface standards. Compatibility of various protocol and mechanical dimensions of connectors is beyond the scope of this application note, but must also be investigated to determine if inter-operation is possible. The following cases are covered, along with a discussion on important electrical characteristics of standard drivers and receivers.

- **Single-ended to Differential**
  RS-232 to RS-422
  TTL to RS-422
- **Differential to Single-ended**
  RS-422 to RS-232 (unipolar)
  RS-422 to RS-232 (polar)
  RS-422 to TTL
  RS-485 to TTL
- **Single-ended to Single-ended**
  TTL to RS-232
  RS-232 to TTL
- **Differential to Differential**
  ECL to RS-422
  RS-422 to RS-485

Driver Output and Receiver Input Characteristics

Before any connection is made, a careful review of the driver output electrical characteristics, and the receiver input electrical characteristics should be completed. For the driver, the following parameters should be reviewed: driver output levels (minimum and maximum), and typical driver loading. For the receiver, the following parameters should be reviewed: input thresholds (sensitivity), input voltage range, and input resistance. Once these parameters have been reviewed, a decision upon what intermediate circuitry between the driver and receiver is required if any. The following pairs of parameters should be compared to determine if they are directly compatible: driver load to receiver input resistance, driver output levels to receiver input voltage range, and driver output levels to receiver thresholds.

Case One: Single-Ended to Differential

When interfacing a single-ended driver to a differential receiver it is important to establish that the maximum output voltage of the single-ended driver does not exceed the recommended input voltage rating of the differential receiver. If it does not, then a direct connection is possible from a maximum voltage level point of view. If it does a simple resistor voltage divider should be inserted to attenuate the signal down to acceptable levels. A second check must be done to make sure that the minimum driver level, after the divider network if employed, is still greater than the receiver's sensitivity. The divider network, should be selected such that the total load presented to the driver is that of a single-ended receiver. Two examples are provided.

RS-232 to RS-422

Depending upon the RS-232 driver that has been specified, driver output levels may be as high as ±15V, and for some RS-422 receivers the maximum input range is specified at ±10V. For this case, a divider network is required. A simple 3 kΩ in series with a 2 kΩ will provide the required attenuation and the correct load. It attenuates the signal 40%, dropping the ±15V to ±9V on the high side, and ±5V (driver minimum output level) to ±3V (which is greater than the receivers thresholds of ±200 mV). In addition the RS-232 driver also sees a 5 kΩ load of the divider network as it should. If the RS-422 receivers can withstand a ±15V input signal, the attenuator circuit is not required from a voltage level point perspective, but may still be desirable. This is due to the fact that many RS-422 (or RS-485) receiver's input impedance is in the range of 18 kΩ, which would cause a faster driver transition time and possibly an EMI and or crosstalk issue. *Figure 1* illustrates inter-operation between the RS-232 driver with a divider network to a RS-422 differential receiver. Note, that one receiver input is referenced to ground. Depending upon the input referenced to ground, a logic NOT may be achieved by tying the + input to ground, and connection to the divider network with the – input. Historically, this divider network has been termed an L-Pad in TIA/EIA documents and other international standards.

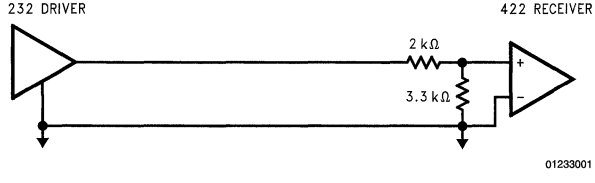


FIGURE 1. RS-232 to RS-422

TTL to RS-422

Since differential receivers are basically modified comparitors, they detect logical states by the difference in potential between their input pins, not with respect to circuit ground. Due to this fact, they can also accept standard TTL or CMOS levels if the other input is appropriately referenced. For TTL levels, one input should be tied to +1.5V, and the resulting thresholds will be +1.7V, and +1.3V. In other words, any levels greater that or equal to +1.7V will be a logic HIGH, and any level less than or equal to +1.3V a LOW, if the reference voltage was applied to the – input. Receivers normally have internal references between +2V and +3V, but it is not recommended that you float the reference input and rely on the internal reference due to the following reasons. First, the internal reference voltage is not normally specified in a datasheet, thus tolerances are not guaranteed or supported. Secondly, the input is a high impedance input, and depending upon the environment, it may pick up external noise and shift the thresholds around. A voltage regulator, or a simple resistor divider may be used depending upon the accuracy required. If a resistor divider is used, remember to take into account the input impedance of the receiver, which can be model (1st level) as a resistor to the internal bias voltage. These two values may be measured with a curve tracer. By sweeping voltage on the reference input, the resulting slope of the line (V_{IN} vs. I_{IN}) is the input impedance, and the crossing of the X axis is the zero current point or internal reference voltage. Note, that this test must be done with the receiver powered up to measure the reference voltage. *Figure 2* illustrates the inter-operation between standard TTL logic and a differential RS-422 receiver.

Case Two: Differential to Single-Ended

Differential to single-ended poses a more difficult problem to solve. Since single-ended receivers, RS-232 for example, essentially detect positive or negative voltage with respect to ground, an active solution is required to gain inter-operation with a single supply differential drivers. The following cases are provided as examples.

RS-422 to RS-232

RS-422 drivers (unipolar) are commonly powered from a single +5V power supply, thus both output states are positive voltages (V_{OL} and V_{OH}). RS-232 receivers as discussed detect positive and negative voltages, therefore to obtain inter-operation the circuit illustrated in *Figure 3* can be used. The PNP transistor is used as a switch, that when it is ON, the receiver input voltage is basically a $V_{CE(SAT)}$ below the driver's V_{OH} level. This is typically greater than +3V, and is a valid RS-232 input level. When the driver is in the opposite state, the PNP is off, the receiver input is pulled to ground by its internal input resistor. Note, RS-232 specifies the receiver thresholds are between –3V and +3V, however most receiver support TTL like thresholds centered around +1.5V, and guarantee a failsafe HIGH output state for an open input state (pulled low by internal input resistor). In the circuit shown in *Figure 3*, the resistor (R1) limits the base current and prevents the PNP from entering deep saturation, the diode (D1) prevents break down of the emitter base junction when the PNP is off. An additional resistor (R2) may be inserted to pull the RS-232 input to a voltage (below –3V) if required, but this also requires a negative supply and is typically not necessary. *Figure 3* illustrates this case of inter-operation.

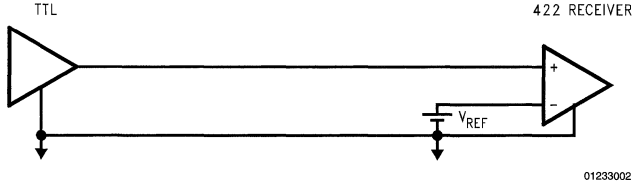


FIGURE 2. TTL to RS-422

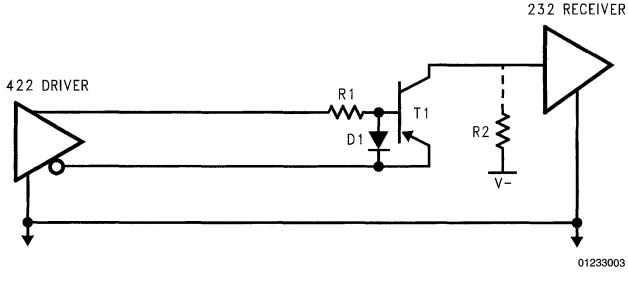


FIGURE 3. RS-422 to RS-232—with Active Device

RS-422 to RS-232 (Continued)

However, this active circuitry may not be required if the two systems share the same ground reference, are located close together, are in a relativity noise free environment and the RS-232 receiver provides a TTL threshold. This is due to the fact that RS-422 driver output levels are quite similar to standard TTL levels, however, driver output curves should be consulted to determine that the drivers V_{OH} level will be detected by the RS-232 receiver as a valid V_{IH}, and the V_{OL} as a V_{IL} respectively. These output levels can be determined by superimposing a 5 kΩ load line over the driver V_{OH}/I_{OH} curve. If the resulting driver V_{OH} is greater than the receivers V_{IH}, then inter-operation is possible. Similarly the output low case should be checked. RS-422 drivers are voltage mode drivers, and both outputs are not required to inter-operate with the single-ended receiver. Therefore, select the output which provides the desired logic (true or inverting), and leave the other output "open". Do not tie the unused output to ground, as that could yield an output short circuit condition (I_{OS}) which is undesirable from a power dissipation consideration. *Figure 4* illustrates the direct connection example.

RS-422 to RS-232

RS-422 drivers are also available that are powered from polar (±5V) power supplies. If this is the case then once again a direct connection to a RS-232 receiver is possible. This is possible since the V_{OH} of the driver is typically between +3V and V_{CC}, while the V_{OL} of the driver is between −3V and V_{EE}, in both the output levels are greater in magnitude than the RS-232 receivers thresholds. *Figure 5* illustrates this second case of direct inter-operation.

RS-422 to TTL

As discussed above, RS-422 driver output levels are quite similar to standard TTL levels, however, driver output curves should be consulted to determine that the drivers V_{OH} level will be detected by the TTL input as a valid V_{IH}, and the V_{OL} as a V_{IL} respectively. In almost all cases a direct connection will be possible. RS-422 drivers are voltage mode drivers, and both outputs need not be used. Simply pick the output (true or inverting), and leave the other output "open". Do not tie the unused output to ground, as that could yield an output short circuit condition (I_{OS}) which is undesirable from a power dissipation consideration. *Figure 6* illustrates the inter-operation of a RS-422 driver with a standard TTL input.

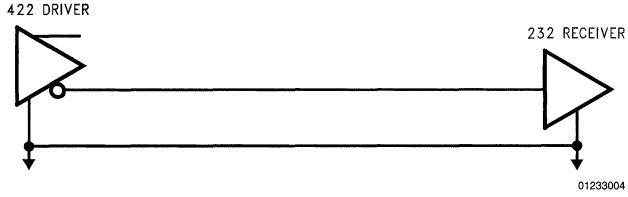


FIGURE 4. RS-422 to RS-232—Direct Connection

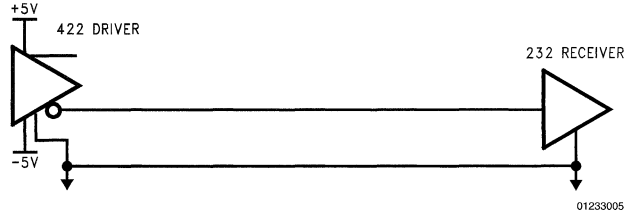


FIGURE 5. RS-422 to RS-232

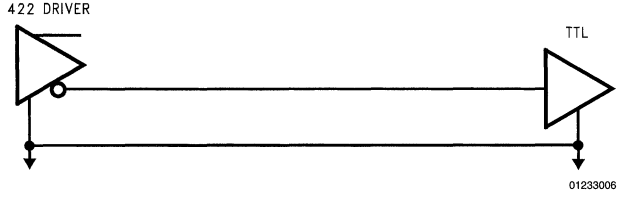


FIGURE 6. RS-422 to TTL

RS-485 to TTL

RS-485 driver output levels are NOT similar to standard TTL levels, however, direct inter-operation may be possible. Again, driver output curves should be consulted to determine that the drivers V_{OH} level will be detected by the TTL input as a valid V_{IH}, and the V_{OL} as a V_{IL} respectively. Since the RS-485 outputs include blocking diodes, the V_{OH} levels are lower than standard TTL levels, and the V_{OL} levels are a diode higher than standard levels. Once again, RS-485 drivers are voltage mode drivers, and both outputs need not be used. Simply select the desired output (true or inverting), and leave the other output "open". Do not tie the unused output to ground, as that could yield an output short circuit condition (I_{OS}) which is undesirable from a power dissipation consideration. If the driver output levels do not meet the TTL input V_{IH} and V_{IL} specifications, a RS-485 receiver should be used to receive the RS-485 levels and correctly translate them to TTL compatible levels *Figure 7* illustrates this connection.

Case Three: Single-Ended To Single-Ended

Single-ended to Single-ended is once again simply comparing output levels to thresholds and input voltage ranges. In some cases, a direct connection is possible, as described in the following examples.

TTL to RS-232

TTL output levels can directly inter-operate with certain RS-232 receivers. This is true since most RS-232 receivers support a tighter threshold specification than required by the RS-232 standard. The RS-232 standard specifies that the thresholds are between +3V and –3V, however, most thresholds are centered around +1.5V. If this is the case, then standard TTL levels (High > 2.0V and Low < 0.8V) will be detected correctly. One note of caution is that the TTL gate will be loaded with the 5 kΩ load instead of a standard TTL input load. The TTL gate driving the RS-232 receiver must have adequate drive capability to obtain the correct levels with the RS-232 receiver load. This connection is illustrated in *Figure 8*.

RS-232 to TTL

RS-232 output levels are polar, and therefore they swing around ground. This negative swing typically prevents direct inter-operation to TTL inputs which prefer positive voltages only. To clamp off the negative swing a diode may be used to clip the negative swing but will load down the driver when the diode is forward biased. This is typically acceptable if the driver employed provides a relatively tight current limit in the range of 10 mA. *Figure 9* illustrates this inter-operation with a diode clamp.

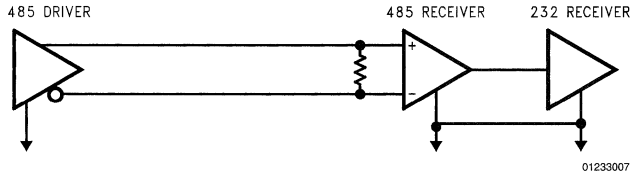


FIGURE 7. RS-485 to TTL

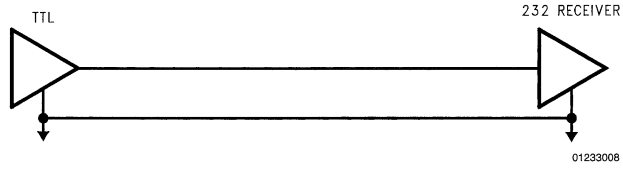


FIGURE 8. TTL to RS-232

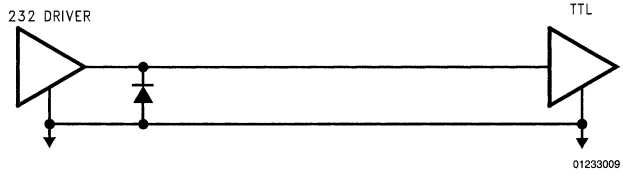


FIGURE 9. RS-232 to TTL

Case Four: Differential to Differential

As in the other three cases described, driver output levels need to be compared to receiver input thresholds and input voltage ranges. If they agree, then a direct connection is possible. If the levels are not compatible then a repeater/ translator circuit will be required.

ECL to RS-422

Differential ECL or even Pseudo ECL (PECL) will typically directly inter-operate with a RS-422 receiver. This is possible since a RS-422 receiver provides a tight threshold specification of ±200 mV, and a wide common mode range of ±10V. Differential ECL output levels are normally between ±500 mV to ±800 mV which are detectable by the receiver. Since the receiver supports a positive and negative common mode range ECL or PECL signals may be received. *Figure 10* illustrates a ECL to RS-422 (or RS-485) connection.

RS-422 to RS-485

Direct connection of RS-422 to RS-485 is always possible. RS-485 can be considered a subset of RS-422 which supports multipoint (multiple drivers) applications. RS-422 and RS-485 receivers are virtually identical, except for the fact that the RS-485 receiver present a input impedance that is typically 3 times the RS-422 receiver. For this reason, the RS-422 driver can now drive at least 32 receiver loads opposed to the RS-422 limit of 10. Recall that RS-422 is limited to single driver/multiple receiver applications, and only RS-485 devices (drivers) should be employed in true multipoint (multiple driver) applications. *Figure 11* illustrates a RS-422 driver driving up to 32 RS-485 receivers in a multidrop uni-directional application.

Summary

In many cases direct inter-operation is possible between different interface standards. In cases where that is not possible, typically simple circuitry can be inserted between the two devices to alter or clamp the levels to levels that are compatible with the other device. In the extreme case, where simple circuitry can not solve the problem, a repeater may be used. For example, if an "A" driver needs to inter-operate with a "B" receiver, a repeater may be inserted between the two that includes a "A" receiver and a "B" driver. For example, this may be desirable for interfacing a RS-422 driver to a ECL differential receiver since most ECL receivers can not accept positive (above ground) input voltages. This method should be a solution of last resort due to the added cost of the active devices, and the repeater itself. The methods described above are preferred, as they provide direct, or inter-operation with only simple circuitry. As a final word of caution, always review the respective device specifications to determine if inter-operation is possible before connecting the two together.

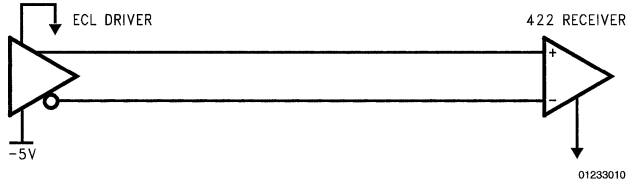


FIGURE 10. ECL to RS-422

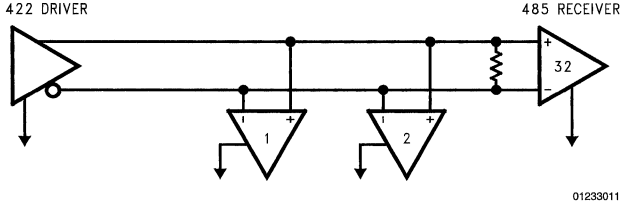


FIGURE 11. RS-422 to RS-485

Table 1 lists key generic electrical characteristics of common interface standards.

TABLE 1. Electrical Characteristics Comparison of Common Interface Standards

Parameter	RS-232	RS-422	RS-423	RS-485
Maximum Driver Output Level	±25V No Load ±15V 7 kΩ Load	±10V No Load ±6V Diff.	±6V No Load	±6V No Load ±6V Diff.
Minimum Driver Output Level	±5V 3 kΩ Load	±2V 100Ω Load	±3.6V 450Ω Load	±1.5V 54Ω Load

Summary (Continued)

TABLE 1. Electrical Characteristics Comparison of Common Interface Standards (Continued)

Parameter	RS-232	RS-422	RS-423	RS-485
Standard Driver Load	3 kΩ–7 kΩ 5 kΩ Typical	100Ω	>4 kΩ Typical 450Ω Minimum	54Ω
Receiver Input Voltage Range	±15V	±10V	±10V	±10V
Receiver Thresholds	±3V +1.5V Typical	±0.2V	±0.2V	±0.2V
Receiver Input Impedance	3 kΩ–7 kΩ 5 kΩ Typical	≥4 kΩ	≥4 kΩ	~>12 kΩ
MODE	Single Ended	Differential	Single Ended	Differential

References

EIA/TIA Standard EIA/TIA-232-E, Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data interchange, EIA/TIA, Washington, D C.

TIA/EIA Standard TIA/EIA-422-B, Electrical Characteristics of Balanced Voltage Digital Interface Circuits, TIA, Washington, D.C.

TIA/EIA Standard TIA/EIA-423-B, Electrical Characteristics of Unbalanced Voltage Digital Interface Circuits, TIA, Washington, D.C.

EIA Standard EIA RS-485, Standard for Electrical Characteristics of Generators and Receivers for use in a Balanced Digital Multipoint Systems, EIA, Washington, D.C.

Application Note #216, Summary of Well Known Interface Standards, Interface Databook, National Semiconductor, Santa Clara, CA

Application Note #759, Comparing EIA-485 and EIA-422-A Line Drivers and receivers in Multipoint Applications, Interface Databook, National Semiconductor, Santa Clara, CA

The Practical Limits of RS-485

National Semiconductor
Application Note 979
Todd Nelson

Introduction

This application note discusses the EIA-485 standard for differential multipoint data transmission and its practical limits. It is commonly called RS-485, however its official name is EIA-485 which reflects the name of the committee at the time it was released. It is expected to be revised soon and will then become TIA/EIA-485-A.

Differential data transmission is ideal for transmitting at high data rates, over long distances and through noisy environments. It nullifies the effects of ground shifts and noise signals which appear as common mode voltages on the transmission line. TIA/EIA-422-B is a standard that defines differential data transmission from a single driver to multiple receivers. RS-485 allows multiple drivers in operation, which makes multipoint (party line) configurations possible.

This application note will discuss the specifications as defined in the RS-485 document. Interpretations of the standard and device specifications can vary among manufacturers. However, there are some guarantees required to be completely compliant with the standard.

There are many possibilities and trade-offs associated with being partially compliant—or "compatible." Some applications can tolerate the trade-offs in return for increased performance or added value. For that reason, this application note will discuss the practical application of the specifications.

A detailed explanation of each requirement of the standard will not be given as this is beyond the scope of this note. Also beyond the scope are advanced topics relating to new technology.

Key RS-485 Requirements

The key features are:

- Differential (Balanced) Interface
- Multipoint Operation
- Operation from a single +5V Supply
- −7V to +12V Bus Common Mode Range
- Up to 32 Unit Loads (Transceivers)
- 10 Mbps Maximum Data Rate (@40 feet)

4000 Foot Maximum Cable Length (@100 kbps)

A typical application is shown in *Figure 4.*

The key requirement of the driver is its guaranteed differential output voltage as measured: with no load; with a minimum configuration of two nodes; and with the full load of 32 nodes. The terms used in the specification are:

V_{OA} True output voltage with respect to ground

V_{OB} Complimentary output voltage with respect to ground

V_{OD} Differential output voltage (V_{OA}–V_{OB})

V_{OS} Offset voltage, or center point of V_{OA} or V_{OA}, also called V_{OC}

V_{CM} Algebraic mean of V_{OA} and V_{QB}, including any ground potential difference or noise

The specifications are best represented by the following figures and table.

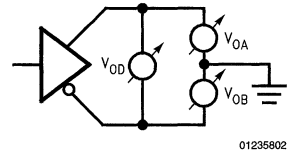


FIGURE 1. No Load Configuration

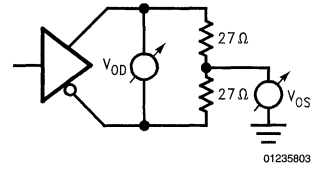


FIGURE 2. Termination Load Configuration

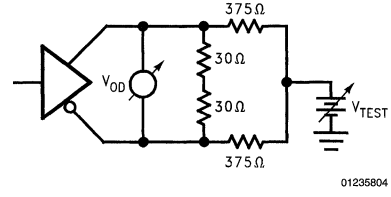


FIGURE 3. Full Load Configuration

Key RS-485 Requirements (Continued)

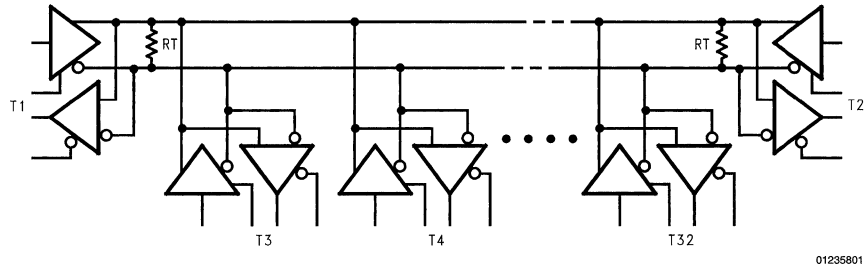


FIGURE 4. Typical RS-485 Application

TABLE 1. Driver Output Voltage Requirements

Configuration	Test	Min	Max	Units
No Load	V_{OD1}	1.5	6.0	V
Figure 1	V_{OA}	0	6.0	V
	V_{OB}	0	6.0	V
Termination	V_{OD2}	1.5	5.0	V
Figure 2	V_{OS}	−1.0	3.0	V
Full Load	V_{OD3}	1.5	5 0	V
Figure 3	with $-7V \le V_{CM} \le +12V$			

There is also a condition that the driver must not be damaged when the outputs are shorted to each other or any potential within the common mode range of −7V to +12V The peak current under shorted conditions must be less than 250 mA. This point is key to multipoint operation, since contention may occur.

The data rate requirements have implications on the speed of the device. Switching characteristics must specify that the transition time (t_r, t_f) be ≤ 0.3 of the unit interval. The minimum unit interval for 10 Mbps at 40 feet is 100 ns so $t_r/t_f \le 33$ ns; for 100 kbps at 4000 feet it is 10 µs so $t_r/t_f \le 3.3$ µs.

A Unit Load is defined as a load on the bus, it is commonly a driver and a receiver. The result should be that the unit load does not load down the bus under power-on or power-off conditions. Driver leakage tends to be in micro-amps but receiver input current can be significant compared to driver leakage. Four points define the unit load, shown in *Figure 5*.

Rec. Input current (I_{IN}) at +12V ≤1 mA

I_{IN} between +5V and +12V≥0 mA

I_{IN} at −7V≥ −0.8 mA

I_{IN} between −3V and −7V≤ 0 mA

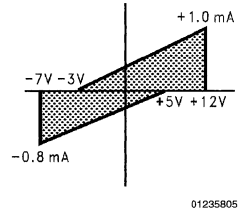


FIGURE 5. V/I Relationship defining a Unit Load

The shaded area effectively defines the receiver input impedance (R_{IN}), ≥10.6 kΩ (19V/1.8 mA). The standard does not require a specific impedance, only that it falls within the shaded area.

The key receiver requirements are its threshold voltage levels and common mode range. The receiver output must be HIGH if the true input is more than 200 mV above the complimentary input; LOW if it is more than 200 mV below the complimentary input. This must be possible with the inputs varying from −7V to +12V. A graphic representation is shown in *Figure 6*. In this diagram, the lightly shaded region represents the range of points where RI is more than 200 mV below RI*; therefore the output is LOW.

Key RS-485 Requirements (Continued)

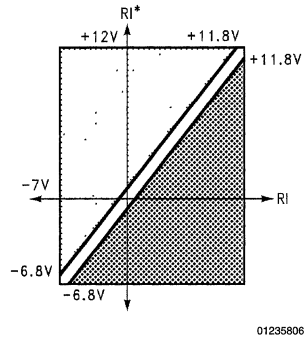


FIGURE 6. Receiver Input Range

The 200 mV receiver threshold and the 1.5V minimum differential driver output voltage provide 1.3V of differential noise margin. Since the bus is typically a twisted pair, ground noise is canceled out by the differential operation. The result is a bus that is well suited for high data rates and noisy environments.

There are further requirements such as balance of terminated voltage, balance of offset voltage and timing which can be reviewed in the standard. Note that all of these requirements should be met over the full supply voltage and temperature range in which the device will operate.

Interpreting the standard and creating device specifications appears to be straight forward. However, the range of practices shows that there are differing opinions.

Compatibility Tradeoffs

It is not always practical to meet all of the requirements. The devices may have limitations, the applications may not need full compliance or there may be a possible improvement in one area at the expense of another.

Commonly accepted minimum specifications for compatibility include V_{OD1}, V_{OD2}, I_{OS}, V_{CM}, V_{TH}. At times, these are specified at controlled conditions—not over the full operating range, as is required. Furthermore, "Up to 32 unit loads . . ." implies V_{OD3} and R_{IN} or the V/I relationship discussed above. V_{OD3} can be traded off if the application is not expected to be fully loaded.

R_{IN} can be increased and thereby allowing more than 32 nodes to be connected without exceeding the 32 unit loads. For example, a R_{IN} of 24 kΩ implies that 64 nodes equates to 32 unit loads.

In many applications, I_{CC} is the differentiating factor. Optimizing a device for low power may slow switching speed. The end user may define the acceptable speed but switching speed is quite often defined by the choice of protocol.

Many low power technologies have lower breakdown voltages, which reduces the recommended maximum voltage range for the bus pins. The recommended voltage range for the bus pins defines how much protection the device has beyond the −7V to +12V common mode range. If the environment demands that the bus survive voltages up to ±24V, then the device must guarantee this, otherwise external protection must be included.

External limitations may dictate controlled edge rates to allow greater stub lengths or reduced EMI, which may result in a device that does not meet the prescribed data rate. All of these trade-offs must be considered in the design of the system.

Implementation Issues

Topology: RS-485 is defined as a multi-point bus, (*Figure 7*) therefore multiple drivers and receivers can be connected to the bus at the same time (see discussion regarding unit load).

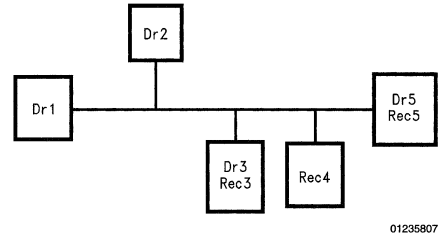


FIGURE 7. Bus Topology

In such a configuration, only one driver has control at a time and all the active receivers receive the same signals.

A ring which is created by connecting both ends of a bus together will not work. A traditional ring uses point-to-point links between the nodes. This can be implemented using RS-485, however, there are many other point-to-point technologies available.

Star configurations are also discouraged. In a star configuration (*Figure 8*) the device is effectively at the end of a very long stub, and this causes reflection and termination problems.

Implementation Issues (Continued)

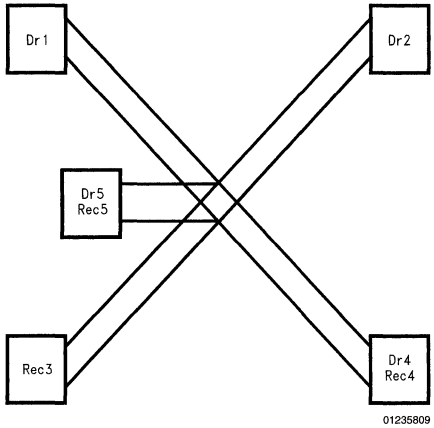


FIGURE 8. Star Topology

Stubs: RS-485 recommends keeping the stubs as short as practical. A stub is the distance from the device to the bus, or the termination resistor (in the case at the ends of the bus), see *Figure 9*. The maximum length is not defined by the standard, but longer stubs will have a negative impact on signal quality. This affect can be reduced by controlling the transition time of the driver.

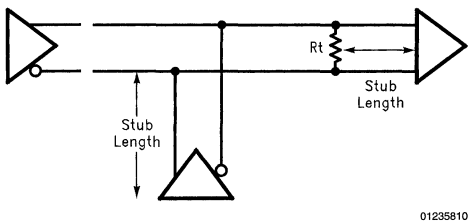


FIGURE 9. Stub Length

The driven signal encounters a reflection at the end of the stub, if this occurs within the rising edge of the signal then it can be neglected. A general rule is that stubs should be less than ⅓ of the transition time. Therefore, slowing the transition time can extend the practical stub length.

stub $\ell \leq$ ⅓ (transition time)/(velocity)

ℓft ≤ ⅓ (t_r or t_f)/(1.5 ns/ft)

Number of Nodes: The standard allows 32 unit loads, as defined by the driver leakage and receiver impedance—this was intended to mean 32 transceivers. If a number of the devices guarantee a greater impedance, then it is possible to add more than 32 transceivers to a bus.

Termination: RS-485 has defined the termination as 120Ω parallel termination at each end of the bus. This assumes a characteristic impedance in the range of Z_O = 100Ω to 120Ω for the cable. Other termination schemes could be implemented, but a thorough analysis must be done to assure adequate signal quality. For more information on termination, see AN-903.

Bus Faults: This bus is defined to be resistant to many of the faults associated with a cable environment such as noise and variations in device ground. It is built for party line applications so it can withstand driver contention. In most cases, there is enough noise margin to detect a valid HIGH or LOW. However, in the case where both lines are open or there is a short between the two lines, the state may be unknown. Such a case requires the designer to implement a "failsafe" scheme to bias the receiver to a known state. See AN-847 and AN-903 for a detailed discussion of failsafe techniques.

Data Rate: Earlier, the data rate vs distance guidelines were given as 10 Mbps at 40 feet and 100 kbps at 4000 feet. Advances in technology continue to push these limits. At long distances the practical limitation is dominated by the rise time degradation due to the cable. The approximate delay associated with 100Ω cable is 1.5 ns/foot. Therefore, 4000 feet of cable will cause 6 µs of delay—which limits the data rate to 333 kbps (166 kHz) before device delays are involved. At 100 feet only 150 ns of delay are added by the cable, so an ideal driver/receiver could switch at 10 Mbps theoretically. Further complications are added by encoding schemes (PWM, RTZ, etc.) and protocol requirements (idle time, overhead, etc.). If an off-set bias is implemented for receiver failsafe, this may induce some signal distortion or cause slight duty cycle distortion which must be factored in to the data rate considerations.

RS-485 is defined as a half-duplex bus, though many applications use multiple channels in parallel or full-duplex. In parallel bus applications, channel-to-channel skew becomes a critical issue. These and possible protocol requirements would have to be considered in the evaluation of each device.

Supply Power: I_{CC} is not always the dominant indicator of power requirements. Low power CMOS devices require little quiescent current, typically less than 1 mA. However, when switching against a heavy load, the load current can be over 60 mA! And switching at higher frequencies also requires more current. Comparing bipolar and CMOS devices should include the case when switching a heavy load at high frequencies as well as the quiescent case. The total requirement will depend on the portion of time at idle versus switching.

Signal Quality: At the extremes of distance and data rate, the signal quality will be degraded. This is a qualitative parameter that is usually judged with eye patterns or in probabilities of errors.

Eye patterns show the effects of intersymbol interference, a hypothetical example is shown in *Figure 10*. A full discussion on signal quality is given in AN-808.

Interfacing to other standards: This bus is not intended to be inter-operable with other standards such as TIA/EIA-232-E or ECL. TIA/EIA-422-B buses can accept RS-485 devices, but the opposite case is not true for the drivers. For a full discussion on this topic, see AN-972. The international standard ISO 8482.1994 has recently become compatible with RS-485.

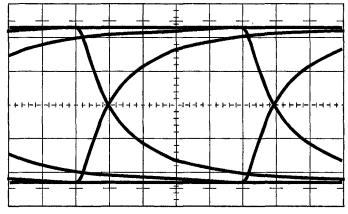
Practical Limits

Theoretical limits defined by the standard should not be exceeded without fully examining the trade-offs discussed above. However, there are some common practices which can extend RS-485 beyond its defined limits.

The maximum number of nodes can exceed 32. R_{IN} can be defined as ½ unit load or ¼ unit load, thus extending the number of nodes that can be attached to a single bus to 64 or 128 respectively. The leakage specifications must also support the stated unit load. Note that a bus with 128 nodes requires that the average loading be ¼ unit load—including any third-party nodes that may be attached. Not all devices need the same unit load rating, but the total cannot exceed 32 unit loads.

The common-mode voltage range requirements continue to be a factor that limits many other types of interfaces. TIA/EIA-422-B offers a common-mode range of ±7V, but does not allow multiple drivers on the bus. The process technologies and design techniques required to meet the −7V to +12V range are somewhat unique. In fact, many applications see common-mode voltages beyond this range, such as ±24V! Generally, reducing common-mode voltage in trade for any performance or integration gains has not been acceptable. Increasing common-mode beyond the RS-485 limits depends on the specific devices; wider common-mode may affect the thresholds and hysteresis of the receiver which reduces the noise margin.

Speed and power requirements are opposing trends: higher data rates tend to use more power, yet lower power (I_{CC}) technologies tend to be slower. Technologies that effectively combine both high speed and low power are becoming available, and will come down in cost. Optimizing for speed in excess of the RS-485 limits may require technologies that consume greater quiescent current. In applications that are not transmitting for extended periods, optimizing for low power is common. Such devices may not meet the 10 Mbps data rate referenced in RS-485, which is acceptable since many of these applications are specified between 9600 bps and 1 Mbps.



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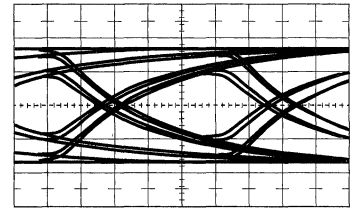

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FIGURE 10. Eye Patterns

Conclusion

RS-485 is a well-defined, multi-purpose electrical specification for multi-point data transmission. The standard allows manufacturers to optimize devices for speed and power. Despite the definition, there is still potential for compatibility issues if the devices are not fully specified.

Many of the limits imposed in RS-485 can be exceeded at some cost and with increased risk. But technology barriers are continuously being removed and this promises tremendous performance gains, perhaps eliminating those costs and risks.

RS-485 is a very rugged standard for multi-point applications. It has proven to be popular over a span of many years. With the breadth of devices available and new technologies being applied, RS-485 will continue for many years to come.

References

EIA RS-485 standard for differential multi-point data transmission

TIA/EIA-422-B standard for differential multi-drop data transmission

ISO 8482.1994 Information processing systems—Data communication Twisted pair multipoint inter-connections

TIA/EIA-422-B Overview

National Semiconductor
Application Note 1031
Michael R. Wilson

Abstract

This application note covers topics associated with concerns for implementing a balanced interface circuit utilizing the TIA/EIA-422-B (formerly RS-422-A) electrical interface standard The items designated by bullets below indicate the topics covered within this application note.

- Cable Length and Data Rate
- Termination
- Failsafe
- Configuration
- ESD Protection
- Live Insertion
- By-Pass Capacitors
- Stub Lengths
- Receiver Power Off Characteristics
- Typical Cable Media

Each topic has an independent section. The sections are identified by bold all upper case titles Subsection titles are bold only

Introduction/Overview

TIA/EIA-422-B (RS-422) is an industry standard specifying the electrical characteristics of a balanced interface circuit Other prefixes are commonly used with the RS-422 standard. These include EIA, EIA/TIA, and RS, although previously correct, today TIA/EIA is the correct prefix. However, for simplicity, RS-422 will be used throughout the rest of this application note Also, a suffix letter denotes the different revisions of the standard but various prefixes with the same suffix reference the same identical standard.

RS-422 was introduced to solve the limitation problems of single-ended standards like TIA/EIA-232-E Single-ended interfaces lack common-mode noise rejection capability; ideal for noisy environments. Also, data rates are usually limited to less than 0.5 Mbps. A RS-422 interface may be implemented to overcome these limitations.

A RS-422 driver can drive up to ten unit loads (i e., 4 kΩ to circuit common is one unit load). The driver is capable of transmitting data across 4000 feet (recommended limit) of cable; but not at maximum data rates (see *Figure 3*). Standard RS-422 drivers are guaranteed to source and sink a minimum 20 mA across a 100Ω load. This corresponds to a minimum differential output voltage, V_{OD}, of 2V across the load (see *Figure 1*).

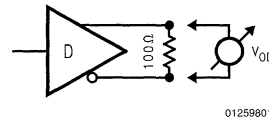


FIGURE 1. Terminated Configuration

The complement RS-422 receiver must be equal to or less than one unit load. This is represented by the slope of the shaded region in *Figure 2*. The operating range of receiver is defined between ±10V and is represented by the shaded area in *Figure 2*.

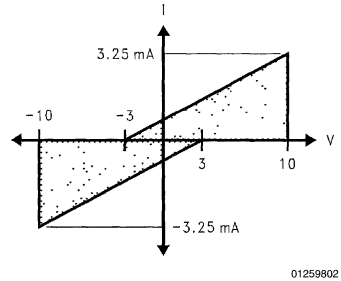


FIGURE 2. Receiver Operating Range

Also, RS-422 receivers have a ±200 mV threshold over the entire common mode range of ±7V. A differential noise margin ≥1.8V is guaranteed between the driver's differential output swing and the receiver's threshold.

RS-422 drivers and receivers are designed for point-to-point and multi-drop configurations but not multi-point. For multi-drop configurations, a daisy chain is the recommended interface configuration.

Caution, at long distances or high data rates, termination is recommended to reduce reflections caused by a mismatch in the impedance of the cable and the impedance of the receiver's input Refer to the section entitled "Termination" for further information.

Significantly, the RS-485 differential interface standard is very similar to RS-422 However, there are differences that distinguish the two standards from one another; which include the output stage of the driver, the common mode range of the interface, the input resistance of the receiver, and the drive capability of the driver. For more details concerning the comparison of RS-422 and RS-485, please reference National's application note AN-759

Cable Length and Data Rate

Cable Length and Data Rate have an inverse affect on each other. When operating at either the recommended maximum cable length or data rate the other can not be obtained. For instance, it is not possible to operate at 4000 feet when operating at 10 Mb/s or vice-versa.

A chart displaying the recommended operational region of a typical RS-422 standard interface is shown in *Figure 3*. Other electrical interface standards operating regions are also shown for comparison. The curves were obtained from empirical data using a 24 AWG, copper, 16 pF/ft, twisted-pair cable parallel terminated with a 100Ω load.

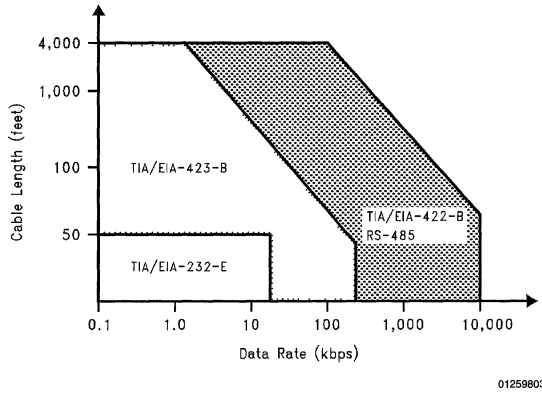


FIGURE 3. Cable Length vs. Data Rate

Termination

Termination is recommended for use when designing a RS-422 interface that is considered to be a transmission line. An interface is considered to be a transmission line if the propagation delay of the cable is greater than 1/8 the transition (rise or fall) time of the signal. This is a time-domain analysis. The same is also true in frequency-domain.

For clarification, the transition time for the time-domain analysis is measured from zero to one hundred percent of the transition. The rising or falling edge may be used for analysis, whichever edge is the fastest.

Transmission lines may restrict the use of a multi-drop configuration and limit the maximum data rate of the RS-422 interface.

Transmission line theory will not be discussed in this application note but is useful knowledge. For more details on transmission line theory, please refer to National application notes AN-806, AN-807, and AN-808.

PARALLEL TERMINATION

Parallel termination, a very popular form of termination, has the advantage of allowing higher data rates and longer cable lengths than an interface using some other termination schemes because transmission line effects are minimized. This is possible because the termination resistor (Rt) is chosen to closely match the cable impedance (Z_O) (see *Figure 4*). The cable impedance can be obtained from the cable manufacturer. The cable impedance may also be measured using TDR, time domain reflectometry, techniques. Additionally, because of the minimized affect of the transmission line, multi-drop configurations with good signal quality are also possible, as long as the stubs (discussed later) are not transmission lines themselves.

A disadvantage of parallel termination is the high power dissipation associated with the heavy termination load. This also leads to a smaller differential output voltage and lower DC noise margins than with a series termination. Also, if the receiver has built-in failsafe circuitry, a known output can not be guaranteed with this type of termination scheme unless the receiver specifically says that it supports "terminated" failsafe. The cost associated with purchasing the one external component should also be considered.

Other schemes exist to choose from and each type has its advantages and disadvantages. Please refer to application note AN-903 for more detailed information on parallel and other termination schemes.

Failsafe

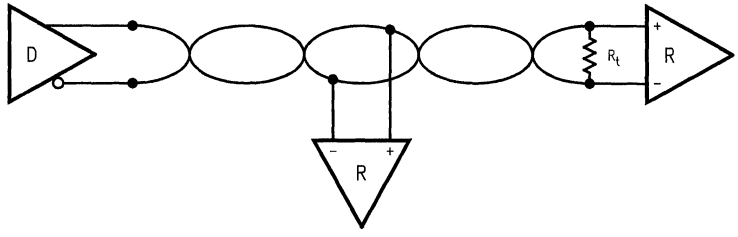
For typical RS-422 interfaces, open, terminated, and shorted input are the three types of failsafe to consider as shown in *Figure 5*. A receiver with full failsafe protection guarantees a known receiver output for all three types failsafe conditions.

OPEN INPUT FAILSAFE

Open input failsafe is the condition when the receiver's output is known when its inputs are left open or floating. The driver is not connected but the receiver is powered. A receiver that provides failsafe for an open input condition, may provide failsafe for idle (driver's output idle) and TRI-STATE® (driver's output disabled) conditions if the bus is not parallel terminated. Therefore, the output state of the receiver may be known for both idle and TRI-STATE bus conditions in some instances.

A receiver is able to provide open input failsafe with internal pull-up and pull-down resistors, typically >50 kΩ. Sometimes only one bias resistor is used on one input and the other input biased to a voltage reference point. Note that any receiver that does not have built-in failsafe, may use external pull-up and pull-down resistors to provide failsafe protection.

Failsafe (Continued)



$R_t = Z_O$

where

R_t = termination resistor

Z_O = characteristic impedance of cable

FIGURE 4. Multi-Drop Application with Parallel Termination

TERMINATED INPUT FAILSAFE

A receiver has terminated failsafe when its output can be determined while its inputs are under terminated conditions. This must be valid for various types of termination schemes; otherwise the receiver does not have terminated failsafe. Additionally, terminated idle line and terminated TRI-STATE line conditions should also be supported. For RS-422 receivers with built-in open input failsafe, the protection circuitry does not guarantee terminated failsafe operation. If a receiver does not have this feature, external bias resistors may be used to provide terminated failsafe protection. For more information please reference application note AN-847 that is devoted to this topic.

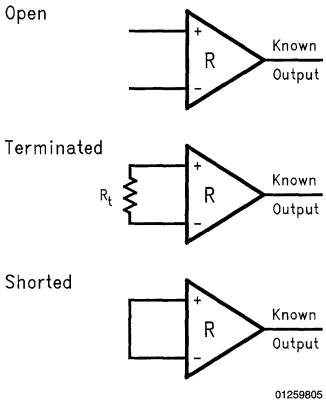


FIGURE 5. Types of Failsafe

SHORTED INPUT FAILSAFE

Shorted failsafe is when the receiver output is known when the receiver inputs are shorted together. If a receiver does not have this type of failsafe, external pull-up and pull-down resistors alone may not help. However, using an alternate-failsafe termination technique will provide protection. Please refer to application note AN-903 for details about alternate-failsafe termination.

National's DS36276 and DS36277 are interface devices that provide all three forms of failsafe protection with no external components required. To accomplish this, the threshold point of the receiver was shifted, violating the RS-422 ±200 mV threshold specification.

Configuration

For RS-422 interface devices, usually three types of configurations are commonly used.

POINT-TO-POINT CONFIGURATION

First, point-to-point, is a one driver and one receiver system. Point-to-point applications may be thought of as using single-ended standards like TIA/EIA-232-E because this is the configuration single-ended standards are popular for. However, differential standards are not restricted from use in point-to-point applications. A typical point-to-point system is shown in *Figure 7*.

MULTI-DROP CONFIGURATION

The second configuration, multi-drop, is one driver with two or more receivers normally connected in a daisy chain layout. For RS-422, the maximum number of receivers is 10 if the receiver's input impedance (R_{IN}) is equal to 4 kΩ or one unit load. If a receiver's R_{IN} is equal to 8 kΩ then that receiver is equal to ½ a unit load. Therefore a RS-422 driver that can drive 10 unit loads can drive 20 receivers with a R_{IN} = 8 kΩ. An example of a multi-drop application is shown in *Figure 4*.

MULTI-POINT

The last type of configuration is multi-point, which uses two or more drivers connected to one or more receivers (see *Figure 6*). RS-422 drivers are normally not designed into this type of configuration. However, a multi-point system can be accomplished if certain issues are addressed. The three

Configuration (Continued)

issues are ground potential differences between drivers, contention between drivers, and the drive capability of the drivers. Therefore, RS-485 devices are recommended for multi-point applications.

For further details and illustrations concerning these issues please reference application note AN-759.

ESD Protection

Electrostatic Discharge (ESD) is normally an event of very high potential for a short period of time. This may be damaging to some integrated circuits (IC). ESD is not limited to a one time occurence in the life of an IC, unless it is fatal the very first time. It may be an ongoing transpiration that can wear down an IC until it eventually fails fatally.

The RS-422 standard does not specify requirements for ESD protection. However, the industry has developed a defacto minimum standard of 2,000V ESD protection under human body model (HBM) conditions. However, many systems today require much higher levels of ESD protection. Possibly as high as 10 kV or 15 kV.

ESD protection may be enhanced in different ways. IC protection circuitry, TransZorbs®, and protected connectors are three possible solutions for increasing an IC's ESD protection. The first method is built-in IC protection circuitry that requires no external components. This type of protection is the result of the manufacturer's IC design. In the early years of IC manufacturing, ESD was not as well publicized or standardized as it is today. Today, IC designers strive to achieve five, ten, even fifteen thousand Volts of ESD protection.

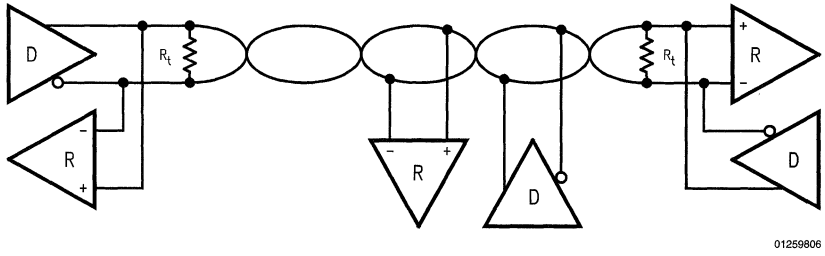


FIGURE 6. Example of Multi-Point Configuration

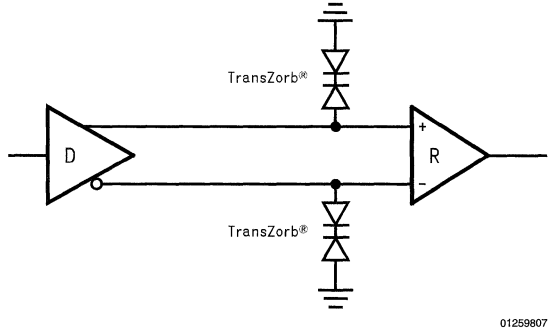


FIGURE 7. A Point-to-Point RS-422 System with TransZorbs

The later two solutions, TransZorbs and protected connectors, are both external to the IC and usually implemented, by the system manufacturer, to provide additional protection, if needed, beyond that which is supplied by the IC itself.

INTEGRATED CIRCUITS

IC protection circuitry is normally designed into the die at the input and output stages of the device. This is because these are the stages that connect to the outside world (via cables or other media). Thus, these are the locations damaged most often by ESD phenomenon. The purpose of the circuitry is to, one, be able to drain off very large amounts of current very quickly, and two, keep the high current away from sensitive areas of the IC. An analogy may be made with lightning rods that channel away large amounts of current, caused by a very large electric field (potential), from your house.

TRANSZORB

TransZorbs are like back-to-back diodes. They are connected between the interface line that needs protection and ground. They act like voltage clamps, clamping voltages that are above the TransZorb's specified reverse stand-off voltage (V_{rs}). Take care when selecting a TransZorb, if the V_{rs} is too high, the IC may become damaged before the TransZorb ever turns on. One TransZorb should be used per interface line. This solution could become expensive as the number of

ESD Protection (Continued)

interface lines requiring protection increases. *Figure 7* shows an example of a RS-422 point-to-point system with TransZorbs.

PROTECTED CONNECTORS

Protected connectors, another solution for increasing ESD protection of an IC, provides the same type of clamping protection that TransZorbs do. However, only one device is needed per interface connector. Therefore, if you have a DB-25 pin connector, all 25 lines receive the same increase in ESD damage resistance. Additionally, designers do not need to worry about lack of additional PC board space, since the device is built into the connector. Also, the protected connector only adds an additional 5 pF or 6 pF of capacitance to the signal load. Designers will be able to find protected connectors in a variety of connector sizes. *Figure 8* shows a diagram of two connectors with built-in ESD protection.

In the later two solutions, the system manufacturer provides additional ESD protection. Ideally, system manufacturers would like the IC manufacturers to provide all the ESD protection required for their systems, internal to the device. National Semiconductor's Interface Group recognizes the importance of ESD protection and has released the DS36276 and the DS36277 with ESD protection up to 7,500V. Future Interface products will trend toward higher ESD protection.

Live Insertion

RS-422 does not specify how to insert an IC (driver or receiver) into a live interface. The same is true for removing the IC. PC board connectors, cable connectors, and sockets are likely interface points A device may be inserted live via one of these interfaces. Live insertion is a larger concern, since removing an IC, from a live interface, normally is less damaging to an IC For live insertion, the device may not be powered up when being inserted Thus, the RS-422 device may receive bus potentials that exceed the power supply voltage (V_{CC}). First, this may cause biasing of diodes and bus clamping, or result in large current faults that damage devices. Second, the potential difference between ICs connections and the interface connector may be large enough to cause ESD strikes which may be harmful to the IC. In addition, the IC may transmit signals when the supply voltage is below minimum operating level which may result in data transfer errors. On the other hand, when removing an IC from an active interface, the V_{CC} should be within normal operating levels with no device pins higher than the supply pin. Also, the potential difference at the instance of the disconnect is minimized since the potential is the equivalent just prior.

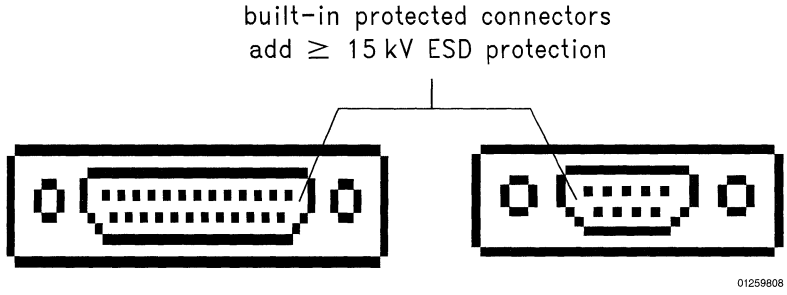


FIGURE 8. Example of Protected Connectors

Recommendations for implementing a live interface are, one, use an IC that supports the feature. Look for this feature in the device's datasheet. However, it will not always appear there so be sure to ask the chip manufacturer's technical support group, to be certain. These ICs usually have specially designed input and output structures that prevent damage to the device even if bus voltages exceed V_{CC}. Two, since removal is less harmful than inserting, try to create similar conditions for inserting the chip that would exist when removing the chip. In other words, it is ideal to have the device powered and referenced to the same ground potential as the interface before the inputs and outputs make physical contact.

For a PC board, a staggered connection where the ground trace is the longest, so that it makes contact first, and the V_{CC} trace is the second longest followed by the input traces then the output traces last would suffice. Live insertion via cables or sockets may require special design but should make contact in the same pattern.

By-pass Capacitors

By-pass capacitors help reduce transients on output signals. Therefore, by-pass capacitors are recommended for better signal quality. One 0.1 µF capacitor is recommended for each powered IC in the system. If a device has more than one power supply (i.e., V_{CC} and V_{EE}) then use one capacitor for each supply. The capacitor should be placed between the power supply pin and ground. Place the capacitor as close to the V_{CC} pin of the device as possible. Additionally, a 10 µF capacitor may be used near the main path where V_{CC} is delivered to the system for bulk charge storage. If a system is large, additional bulk capacitance may be distributed across the system.

Stub Length

Since RS-422 is a multi-drop standard, receivers may be connected to the bus via a stub. The length of the stub is

Stub Length (Continued)

important because of the affect it may have on the signal. As the stub length is increased, its characteristics begin to act as a transmission line. When is a stub considered to be a transmission line? A typical guideline for stubs and transmission lines is stated here:

Time Domain:

If the propagation delay of the stub (one way trip) is greater than 1/8 the transition time, measured from 0% to 100% of the signal transition, then the stub may be considered a transmission line.

The boundary conditions at which a stub begins to act as a transmission line are not precise. Therefore, designers may use slightly different ratios.

Furthermore, the maximum length of the stub depends on the transition time measured at the point of the stub interconnect. This is very important to remember because if the total length of the cable is 1,000 feet, a longer stub can be hung off the cable at 750 feet away from the driver than at 75 feet away from the driver. This is because the cable capacitance slows the transition time of the driver's output as it propagates down the cable and the transition time is longer.

The length of the stub may be increased by slowing down the transition edge at the stub interconnect. This can be done using a bulk capacitance load or a RS-422 driver with output wave shape control like National's DS3691, DS3692, or DS36C280.

To implement a RS-422 interface with stubs of equal length. Apply the stub guideline rule to the stub(s) closest to the driver's output and use this length for the maximum length for all stubs on the interface bus.

If a stub is too long and causes a noticeable reflection, it will be measured positive on the stub because the voltage reflection coefficient is positive since the load impedance Z_L is larger than the stub impedance Z_o. The formula for the reflection coefficient at the load is shown in equation 1.

$$\left\{\Gamma = \frac{Z_L - Z_O}{Z_L + Z_O}\right\}$$

Eq. 1. Load Reflection Coefficient

Note, the load impedance is equivalent to the input impedance of the receiver which is equal to or greater than 4 kΩ. The stub impedance is typically about 100Ω–130Ω. The reflection created at the stub will propagate in both directions away from the stub (see *Figure 9*). Keep in mind that reflections are time dependent events.

Receiver Power Off Characteristics

The receivers characteristics powered down are similar to those when powered up (see *Figure 10*). Therefore, the receiver, when physically connected, may be powered up or down transparent to the RS-422 driver.

RECEIVER INPUT IMPEDANCE

The receiver input impedance curve is identical for both inputs while the receiver is powered off. The characteristic curves also pass through the (0V, 0 mA) coordinate (see *Figure 10*). While the receiver is powered on, the impedance of both inputs are the same but the input impedance curves do not pass through the (0V, 0 mA) point. Additionally, the curves may or may not cross the x and y axis at the same points (see *Figure 10*). For receivers with built-in open input failsafe, the curves will differ by at least 200 mV over operating range.

The input impedance of a RS-422 receiver is guaranteed from −10V to +10V which is the operating range for RS-422 receivers. The 10V is equal to the 7V common mode voltage plus 3V offset voltage.

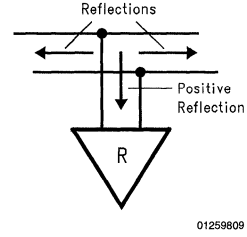


FIGURE 9. Stub Reflections

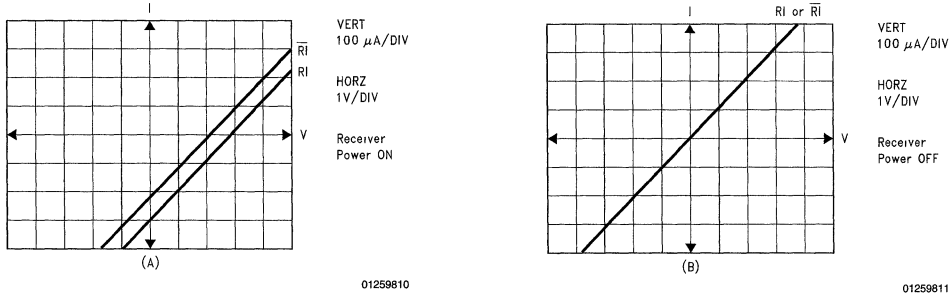


FIGURE 10. Receiver ON/OFF Characteristics

Receiver Power Off Characteristics

(Continued)

RECEIVER BREAKDOWN VOLTAGE

The receiver breakdown voltage is guaranteed to be greater than ±10V whether the receiver is powered on or off. The breakdown point may be found by curve tracing the device out past ±10V. Breakdown voltages may be more than twice the maximum operating voltage.

Typical Cable Media

CABLE TYPE

Flat or round cables may be used when connecting a RS-422 driver and receiver(s). Twisted pair or non-twisted conductors may be used. Twisted pair cables have an advantage over non-twisted when transmitting differential signals. Twisted pair cables couple noise more symmetrically than non-twisted pair cables. This helps preserve the noise rejection limits of the RS-422 receiver (±7V).

CABLE SIZE

The defacto standard gauge size is 24 AWG. A range of 22 AWG to 28 AWG is acceptable for most applications. For cable length see "Cable Length and Data Rate" section in this application note.

MORE ON CABLES

For more details on cable selections, including information concerning shields, insulation, and cable characteristics, refer to application note AN-916.

Summary

RS-422 is a standardized differential electrical interface capable of transmitting data in point-to-point and multi-drop applications. When implementing a RS-422 interface, make sure design-in concerns are addressed at the early stages of design to eliminate problems later in the application, which may be a lot more costly. Understanding RS-422 means understanding the issue associated with the interface.

RS-422 is a well-defined standard and has many applications. However, RS-422 has been superseded by RS-485 which builds onto the existing foundation and creates an even more rugged standard. For more information on RS-485, please reference AN-979.

References

1. TIA/EIA-422-B, *Electrical Characteristics of Balanced Digital Interface Circuits,* Electronic Industries Association Engineering Department. Washington D.C. 1994.
2. *INTERFACE: Data Transmission Databook.* National Semiconductor Corporation. Santa Clara, CA 95052. 1994.

Referenced Application Notes:

AN-759	RS-422 vs. RS-485
AN-806	Transmission Lines
AN-807	Transmission Lines
AN-808	Transmission Lines
AN-847	Failsafe
AN-903	Termination
AN-916	Cables

Ten Ways to Bulletproof RS-485 Interfaces

National Semiconductor
Application Note 1057
John Goldie

Despite its widespread use, RS-485 is not as well understood as it should be. However, if you invest a little time on familiarizing yourself with the bus and pay attention to 10 aspects of your application, you'll find that designing rock-solid implementations is easy.

Recommended Standard 485 (RS-485) has become the industry's workhorse interface for multipoint, differential data transmission. RS-485 is unique in allowing multiple nodes to communicate bidirectionally over a single twisted pair. No other standard combines this capability with equivalent noise rejection, data rate, cable length, and general robustness For these reasons, a variety of applications use RS-485 for data transmission. The list includes automotive radios, hard-disk drives, LANs, cellular base stations, industrial programmable logic controllers (PLCs), and even slot machines. The standard's widespread acceptance also results from its generic approach, which deals only with the interface's electrical parameters. RS-485 does not specify a connector, cable, or protocol. Higher level standards, such as the ANSI's SCSI standards and the Society of Automotive Engineers' (SAE's) J1708 automotive-communication standard, govern these parameters and reference RS-485 for the electrical specifications.

Although RS-485 is extremely popular, many system designers must learn how to address its interface issues. You should review 10 areas before you design an RS-485 interface into a product. Understanding the issues during system design can lead to a trouble-free application and can reduce time to market.

RS-485 addresses a need beyond the scope of RS-422, which covers buses with a single driver and multiple receivers RS-485 provides a low-cost, bidirectional, multipoint interface that supports high noise rejection, fast data rates, long cable, and a wide common mode range. The standard specifies the electrical characteristics of drivers and receivers for differential multipoint data transmission but does not specify the protocol, encoding, connector mechanical characteristics, or pinout. RS-485 networks include many systems that the general public uses daily. These applications appear wherever a need exists for simple, economical communication among multiple nodes Examples are gas-station pumps, traffic and railroad signals, point-of-sale equipment, and aircraft passenger seats. The Electronic Industries Association (EIA) Technical Recommendation Committee, TR30, made RS-485 a standard in 1983. The Telecommunitcations Industry Association (TIA) is now responsible for revisions. RS-485 is currently being revised. After successful balloting, the revised standard will become "ANSI TIA/EIA-485-A."

The 10 considerations that you should review early in a system design are:

- Mode and nodes,
- Configurations,
- Interconnect media,
- Data rate vs cable length,
- Termination and stubs,
- Unique differential and RS-485 parameters,
- Grounding and shielding,
- Contention protection,
- Special-function transceivers, and
- Fail-safe biasing.

Mode and Nodes

In its simplest form, RS-485 is a bidirectional half-duplex bus comprising a transceiver (driver and receiver) located at each end of a twisted-pair cable. Data can flow in either direction but can flow only in one direction at a time. A full-duplex bus, on the other hand, supports simultaneous data flow in both directions. RS-485 is mistakenly thought to be a full-duplex bus because it supports bidirectional data transfer. Simultaneous bidirectional transfers require not one but two data pairs, however.

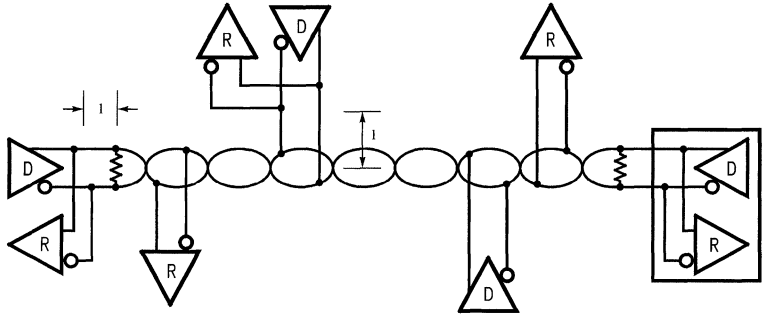
RS-485 allows for connection of up to 32 unit loads (ULs) to the bus. The 32 ULs can include many devices but commonly comprise 32 transceivers *Figure 1* illustrates a multipoint bus. In this application, three transceivers—two receivers receivers and one driver—connect to the twisted pair. You must observe the 32-UL limitation, because the loads appear in parallel with each other and add to the load that the termination resistors present to the driver. Exceeding 32-UL loads excessively limits the drivers and attenuates the differential signal, thus reducing the differential noise margin.

RS-485 drivers are usually called "60 mA drivers." The name relates to the allowable loading. Developing 1.5V across the 60Ω termination load (120Ω at each end of the bus) requires 25 mA. The worst-case input current of a UL is 1 mA (at extreme common mode, explained later) *Figure 2* shows the loading curve of a full UL. The worst-case UL input resistance is 10 56 kΩ, although a frequently quoted incorrect value is 12 kΩ. Thus, 32 ULs require 32 mA drive capability Adding this current to the 25 mA for the terminations yields 57 mA, which rounds up to an even 60 mA. A driver that cannot supply the full 60 mA violates the standard and reduces the bus's performance. The resulting problems include reduced noise margin, reduction in the number of unit loads or allowable cable length, and limited common-mode voltage tolerance.

Designers frequently ask, "What is the maximum number of transceivers the bus allows?" The standard does not specify a maximum number of transceivers, but it does specify a maximum of 32 ULs. If a transceiver imposes one unit load, the maximum number of transceivers is also 32. You can now obtain transceivers with ½- and ¼-UL ratings, which allow 64 and 128 transceivers. However, these fractional-UL devices, with their high-impedance input stages, typically operate much more slowly than do single-UL devices. The lower speed is acceptable for buses operating in the low hundreds of kilobits per second, but it may not be acceptable for a 10 Mbps bus.

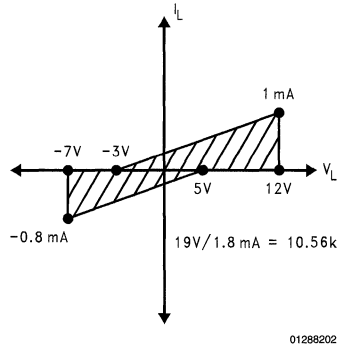
Mode and Nodes (Continued)

A solution exists for high-speed buses: You can use RS-485 repeaters to connect multiple buses end to end. In this setup, each bus must have no more than 32 loads. Directional control of the repeaters is complex, but hardware can handle it (Reference 1). Therefore, a conservative estimate is that, without using special transceivers, a bus can include 32 transceivers.



An RS-485 bus supports two-way data transfer over a single pair of wires. A typical bus includes multiple nodes. Each transceiver includes a differential driver, D, and a differential receiver, R The stub length is l The bus is terminated only at the ends — not at each node

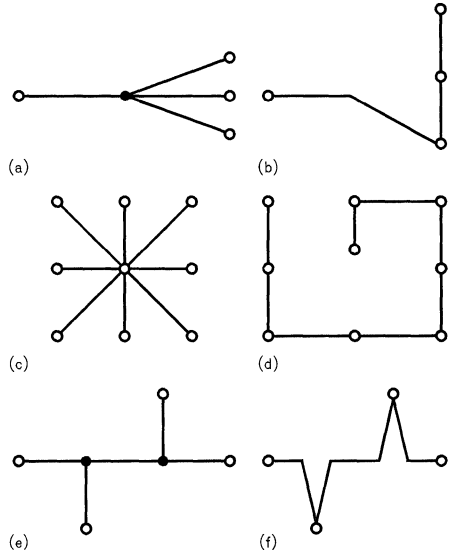
FIGURE 1.



The loading of a tranceiver must remain within the shading region to be one unit load

FIGURE 2.

Mode and Nodes (Continued)



Although you can make RS-485 buses with all of these configurations work, you should avoid the ones in (a), (c), and (e) Those in (b), (d), and (f), offer superior transmission-line performance

FIGURE 3.

Warning: A final word of caution Do not connect too many transceivers to the bus or lump too many transceivers too close together The AC loading, which results mainly from the devices' pin I/O capacitance (usually about 15 pF), can alter the interconnect-medium impedance and cause transmission-line problems

Configurations

Because RS-485 allows connecting multiple transceivers, the bus configuration is not as straightforward as in a point-to-point bus (RS-232C, for example). In a point-to-point bus, a single driver connects to one receiver alone. The optimal configuration for the RS-485 bus is the daisy-chain connection from node 1 to node 2 to node 3 to node n. The bus must form a single continuous path, and the nodes in the middle of the bus must not be at the ends of long branches, spokes, or stubs. *Figure 3a*, *Figure 3c*, and *Figure 3e* illustrate three common but *improper* bus configurations. (If you mistakenly use one of these configurations, you can usually make it work but only through substantial effort and modification.) *Figure 3b*, *Figure 3d*, and *Figure 3f* show equivalent daisy-chained configurations.

Connecting a node to the cable creates a stub, and, therefore, every node has a stub. Minimizing the stub length minimizes transmission-line problems. For standard transceivers with transition times around 10 ns, stubs should be shorter than 6 in. A better rule is to make the stubs as short as possible. A "star" configuration (*Figure 3c*) is a special case and a cause for concern. This configuration usually does not provide a clean signaling environment even if the cable runs are all of equal length. The star configuration also presents a termination problem, because terminating every endpoint would overload the driver. Terminating only two endpoints solves the loading problem but creates transmission-line problems at the unterminated ends. A true daisy-chain connection avoids all these problems.

Interconnect Media

The standard specifies only the driver-output and receiver-input characteristics—not the interconnection medium. You can build RS-485 buses using twisted-pair cables, flat cable, and other media, even backplane pc traces. However, twisted-pair cable is the most common. You can use a range of wire gauges, but designers most frequently use 24 AWG. The characteristic impedance of the cable should be 100Ω to 120Ω. A common misconception is that the cable's chatacteristic impedance (Z_0) must be 120Ω, but 100Ω works equally well in most cases. Moreover, the 120Ω cable's higher Z_0 presents a lighter load, which can be helpful if the cable runs are extremely long.

Twisted pair offers noise benefits over flat or ribbon cables. In flat cable, a noise source (usually a conductor carrying an unrelated signal) can be closer to one member of the conductor pair than to the other over an entire wiring-run length. In such cases, more noise capacitively couples to the closer conductor than to the more distant one, producing a differential noise signal that can be large enough to corrupt the data. When you use the twisted pair, the noise source is closest to each of the conductors for roughly half of the wiring-run length. Therefore, the two conductors pick up roughly equal noise voltages. The receiver rejects these voltages because they appear mainly as common mode.

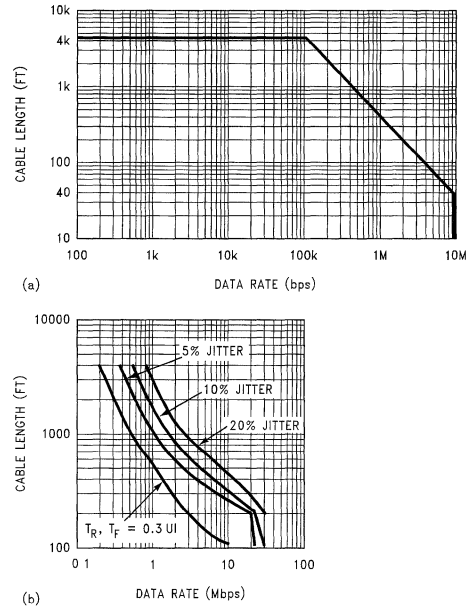
Interconnect Media (Continued)

A special ribbon cable that is useful for noise reduction intermixes relatively long twisted sections with short flat sections. This cable provides the advantages of twisted pair between the flat sections and allows the use of insulation displacement connectors at the flat points.

Data Rate Vs Cable Length

You can transmit data over an RS-485 bus for 4000 ft (1200m), and you can also send data over the bus at 10 Mbps. But, you cannot send 10 Mbps data 4000 ft. At the maximum cable length, the maximum data rate is not obtainable. The longer the cable, the slower that data rate, and vice versa. *Figure 4a* shows a conservative curve of data rate vs cable length for RS-422 and RS-485. The two slopes result from different limitations. The maximum cable length is the result of the voltage divider that the cable's DC loop resistance and the termination resistance create. Remember, for differential buses, the loop resistance is twice as high as you might expect, because both conductors in the pair equally contribute.

The curve's sloped portion results from AC limitations of the drivers and the cable. *Figure 4b* shows four limits for a DS3695 transceiver that drives a common twisted-pair cable. Notice that the data rate vs cable length depends significantly on how you determine the necessary signal quality. This graph includes two types of criteria. The first is a simple ratio of the driver's transition time to the unit interval. A curve showing the results for the common 30% ratio defines the most conservative set of operating points.



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As you increase the cable length, the maximum data rate decreases The more jitter you can accept, the greater is the allowable data rate for a given length of cable

FIGURE 4.

Special Transceivers Solve Special Problems

DS3696/A —Thermal shutdown reporting pin: This device provides an open collector pin that reports the occurrence of a severe bus fault that has caused a thermal shutdown of the driver (>150°C junction temperature).	**DS36276** —Fail-safe transceiver: Standard transceiver pinout with fail-safe detecting receiver, optimal for use with UARTs and asynchronous buses.	**DS36C279** —Ultra-low-power CMOS transceiver with automatic-sleep mode: Optimizes current with the automatic-sleep mode. With inactivity on the enable lines, I_{CC} drops to less than 10 µA.
DS3697 —Repeater pinout: Special pinout that internally connects a receiver port to a driver port. You need two of these devices for a bidirectional repeater.	**DS36277** —Fail-safe transceiver with active-low driver enable: Similar to the DS36276 but includes an active-low driver-enable pin. This feature allows a simplified connection to a UART and supports dominant-mode operation (use of the enable pin as the data pin).	**DS36C280** —Ultra-low-power CMOS transceiver with adjustable-slew-rate control: Adjustable driver slew rate allows tailoring for long stub lengths and reduced emissions.
DS3698 —Repeater pinout with thermal-shutdown pin: A repeater device that also provides the thermal-shutdown reporting pin.	**DS36C278** —Ultra-low-power CMOS transceiver: µA supply current and full RS-485 drive capability. One-fourth unit load allows up to 128 transceivers on the bus.	**DS36954** —Quad transceiver: Offers four independent transceivers in a single package. Useful for parallel buses.

A second method of determining the operating points uses eye-pattern (jitter) measurements. To make such measurements, you apply a pseudo random bit sequence (PRBS) to the driver's input and measure the resulting eye pattern at the far end of the cable. The amount of jitter at the receiver's threshold vs the unit interval yields the data point. Less jitter means better signal quality. Common operating curves use 5, 10, or 20% jitter. Above 50%, the eye pattern starts to close, and error-free data recovery becomes difficult (Reference 2). The key point is that you can't obtain the maximum data rate at the maximum cable length. But, if you operate the bus within the published, conservative curves, you can expect an error-free installation.

Termination and Stubs

Most RS-485 buses require termination because of fast transitions, high data rates, or long cables. The purpose of

Termination and Stubs (Continued)

the termination is to prevent adverse transmission-line phenomena, such as reflections. Both ends of the main cable require termination. A common mistake is to connect a terminating resistor at each node—a practice that causes trouble on buses that have four or more nodes. The active driver sees the four termination resistors in parallel, a condition that excessively loads the driver. If each of the four nodes connects a 100Ω termination resistor across the bus, the active driver sees a load of 25Ω instead of the intended 50Ω. The problem becomes substantially worse with 32 nodes. If each node includes a 100Ω termination resistor, the load becomes 3.12Ω. You can include provisions for termination at every node, but you should activate the termination resistors only at the end nodes (by using jumpers, for example).

Stubs appear at two points. The first is between the termination and the device behind it. The second is between the main cable and a device at the middle of the cable. *Figure 1* shows both stubs. The symbol "I" denotes the stub length. Keep this distance as short as possible. Keeping a stub's electrical length below one-fourth of the signal's transition time ensures that the stub behaves as a lumped load and not as a separate transmission line. If the stub is long, a signal that travels down the stub reflects to the main line after hitting the input impedance of the device at the end of the stub. This impedance is high compared with that of the cable. The net effect is degradation of signal quality on the bus. Keeping the stubs as short as possible avoids this problem. Instead of adding a long branch stub, loop the main cable to the device you wish to connect. If you must use a long stub, drive it with a special transceiver designed for the purpose.

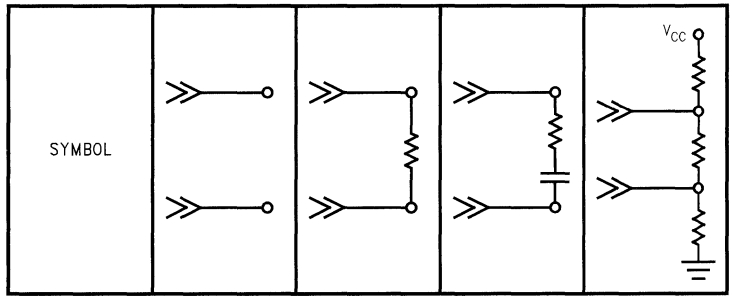
Termination Options

You have several options for terminating an RS-485 bus. The first option is no termination. This option is feasible if the cable is short and if the data rate is low. Reflections occur, but they settle after about three round-trip delays. For a short-cable, the round-trip delay is short and, if the data rate is low, the unit interval is long. Under these conditions, the reflections settle out before sampling, which occurs at the middle of the bit interval

The most popular termination option is to connect a single resistor across the conductor pair at each end The resistor value matches the cable's differential-mode characteristic impedance. If you terminate the bus in this way, no reflections occur, and the signal fidelity is excellent. The problem with this termination option is the power dissipated in the termination resistors.

If you must minimize power dissipation, an RC termination may be the solution. In place of the single resistor, you use a resistor in seris with a capacitor. The capacitor appears as a short circuit during transitions, and the resistor terminates the line. Once the capacitor charges, it blocks the DC loop current and presents a light load to the driver. Lowpass effects limit use of the RC termination to lower data-rate applications, however (Reference 3).

Another popular option is a modified parallel termination that also provides a fail-safe bias. A detailed discussion of fail-safe biasing occurs later in the article. *Figure 5* compares the four popular termination methods. The main point to remember is that, if you use termination, you should locate the termination networks at the two extreme ends of the cable, not at every node.



TERMINATION NAME:	UNTERMINATED	PARALLEL	RC TERMINATION	FAILSAFE
DATA RATE:	LOW	HIGH	MEDIUM	HIGH
SIGNAL QUALITY:	LIMITED	EXCELLENT	LIMITED	EXCELLENT
POWER:	LOW	HIGH	LOW	HIGH

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RS-485 buses can use four methods of termination Achieving the best electrical performance requires accepting higher power dissipation in the termination resistors

FIGURE 5.

Unique Differential and RS-485 Parameters

Four parameters that are important to differential data transmission and RS-485 are V_{OD}, V_{OS}, V_{GPD}, and V_{CM}. *Figure 6*, *Figure 7* and *Figure 8* illustrate these parameters, which are not common in the world of single-ended signaling and standard logic families.

Unique Differential and RS-485 Parameters (Continued)

V_{OD} represents the differential output voltage of the driver across the termination load. The RS-485 standard refers to this parameter as "termination voltage" (V_T), but V_{OD} is also commonly used. You measure V_{OD} differentially across the transmission line—not with respect to ground. On long cable runs, the DC resistance attenuates V_{OD}, but the receivers require only a 200 mV potential to assume the proper state. Attenuation, therefore, is not a problem. At the driver output, V_{OD} is 1.5V minimum. The IC manufacturer should guarantee this voltage under two test conditions: The first uses a simple differential load resistor. The second includes two 375Ω resistors connected to a common-mode supply. These resistors model the input impedance of 32 parallel ULs, all referenced to an extreme common-mode voltage. To make the 1.5V limit in this test, the driver must source or sink roughly 60 mA. This test is difficult and is important, because it essentially guarantees the system's differential-noise margin under worst-case loading and common-mode conditions.

Data sheets for RS-485 drivers usually do not include V_{OL} or V_{OH} specifications. The driver's $V_{OL}$is typically around 1V. Even for CMOS devices, V_{OH} is slighly above 3V, because both the source and sink paths of the output structure include a series-connected diode, which provides the common-mode tolerance for an Off driver. Because V_{OL} is usually greater than 0.8V, an RS-485 driver is not TTL-compatible.

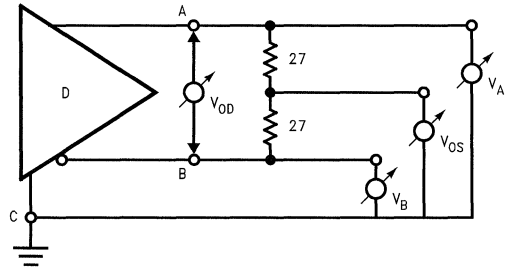
V_{OS} represents the driver's offset voltage measured from the center point of the load with respect to the driver's ground reference. V_{OS} is also called "V_{OC}" for output common-mode voltage. This parameter is related to V_{CM}.

V_{CM} represents the common-mode voltage for which RS-485 is famous. The limit is −7V to +12V. Common-mode voltage is defined as the algebraic mean of the two local-ground-referenced voltages applied to the referenced terminals (receiver input pins, for example). The common-mode voltage represents the sum of three voltage sources. The first is the active driver's offset voltage. The second is coupled noise that shows up as common mode on both signal lines. The third is the ground-potential difference between the node and the active driver on the bus. Mathematically,

$$V_{CM} = V_{OS} + V_{NOISE} + V_{GPD}.$$

V_{GPD} represents the ground-potential difference that can exist between nodes in the system. RS-485 allows for a 7V shift in grounds. A shift of 7V below the negative (0V) power rail yields the −7V common-mode limit, whereas 7V above the 5V positive power rail yields the other common-mode limit of 12V. Understanding these parameters enables improved component selection, because some devices trade off certain parameters to gain others.

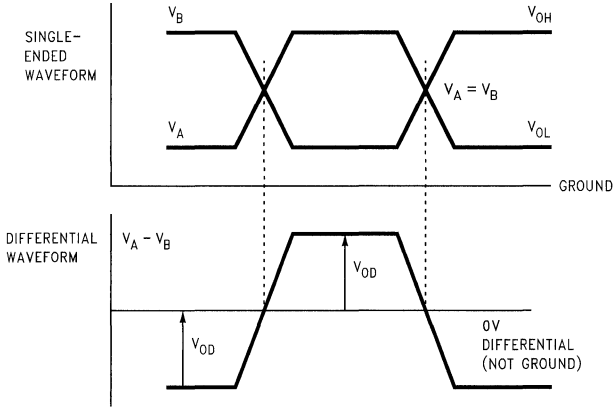
To further illustrate RS-485's common-mode noise-rejection capability, you can conduct the following test: Connect a driver to a receiver via an unshielded twisted-pair cable. Then, couple a noise signal onto the line, and, from the scope, plot the resulting waveform at the receiver input (*Figure 9*). The plot includes the receiver's output signal. Note that the receiver clearly detects the correct signal state, despite the common-mode noise. Differential transmission offers this high noise rejection; a single-ended system would erroneously switch states several times under these test conditions.



Because RS-485 buses are differential, they involve parameters that have no counterparts in single-ended systems

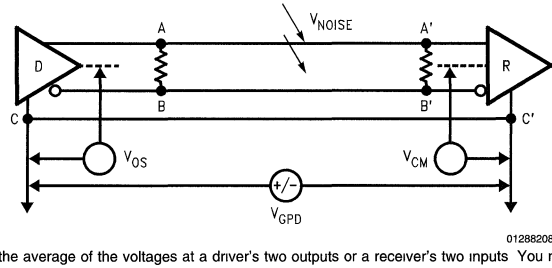
FIGURE 6.

Unique Differential and RS-485 Parameters (Continued)



Although the voltages on the bus's two conductors vary symmetrically about a value that is halfway between the driver's Low and High output-state values, the differential voltage between the conductors varies about zero In addition, the differential voltage swing is double the swing on either of the bus conductors

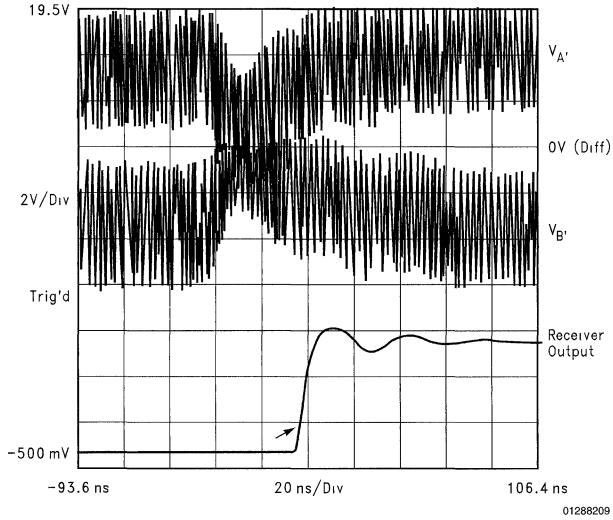
FIGURE 7.



The common-mode voltage, V_{CM}, is the average of the voltages at a driver's two outputs or a receiver's two inputs You measure all voltages with respect to the driver's or receiver's common terminal

FIGURE 8.

Unique Differential and RS-485 Parameters (Continued)



Because of the bus's differentail nature and the receiver's common-mode rejection, the receiver's output (lowest trace) is clean despite large common-mode noise voltages on both of the bus conductors

FIGURE 9.

Standards Related to RS-485

EIA RS-485 —Originally published in 1983, the multipoint standard specifies the concept of the unit load along with electrical characteristics of the drivers and receivers. It was developed from the RS-422 standard, adding multipoint capability, extended common-mode range, increased drive capability, and contention protection. It is an "electrical-only" standard that does not specify the function of the bus or any connectors.

TIA/EIA-485-A (PN-3498) —The TIA expects completion of the first revision to RS-485 this year (Project Number 3498). The goals of the revision are to clean up vague text and to provide additional information to clarify certain technical topics. This work will become the "A" revision of RS-485 once the balloting (approval) process is complete. In addition to the revision work, an application bulletin (PN-3615) is also in process. This document will provide additional application details and system considerations to aid the designer.

ISO/IEC 8482.1993 —The current revision of this international standard maps closely to RS-485. The original ISO standard specified different limits and conditions. However, the 1993 revision changed many of these differences, and RS-485 and ISO 8482 are now similar.

Grounding and Shielding

Although the potential difference between the data-pair conductors determines the signal without officially involving ground, the bus needs a ground wire to provide a return path for induced common-mode noise and currents, such as the receivers' input current. A typical mistake is to connect two nodes with only two wires. If you do this, the system may radiate high levels of EMI, because the common-mode return current finds its way back to the source, regardless of where the loop takes it. An intentional ground provides a low-impedance path in a known location, thus reducing emissions.

Electromagnetic-compatibility and application requirements determine whether you need a shield. A shield both prevents the coupling of external noise to the bus and limits emissions from the bus. Generally, a shield connects to a solid ground (normally, the metal frame around the system or subsystem) with a low impedance at one end and a series RC network at the other. This arrangement prevents the flow of DC ground-loop currents in the shield.

Contention Protection

Because RS-485 allows for connecting multiple drivers to the bus, the standard addresses the topic of contention. When two or more drivers are in contention, the signal state on the bus is not guaranteed. If two drivers are on at the same time and if they are driving the same state, the bus state is valid. However, if the drivers are in opposite states,

Contention Protection (Continued)

the bus state is undetermined, because the differential voltage on the bus drops to a low value within the receiver's threshold range Because you do not know the driver states, you must assume the worst—namely, that the data on the bus is invalid.

Contention can also damage the ICs. If several drivers are in one state, a single driver in the opposite state sinks a high current (as much as 250 mA). This large current causes excessive power dissipation. A difference in ground potential between nodes only aggravates this dissipation. In this situation, the driver's junction temperature can increase beyond safe limits. The RS-485 standard recommends the use of special circuitry, such as a thermal shutdown circuit, to prevent such damage. Most RS-485 devices use this technique. The shutdown circuit disables the driver outputs when the junction temperature exceeds 150°C and automatically re-enables the outputs when the junction cools. If the fault is still present, the device cycles into and out of thermal shutdown until someone clears the fault.

Besides thermal shutdown, other current limiting is required to prevent accidental damage. If an active output is shorted to any voltage within the –7V to +12V range, the resulting current must not exceed 250 mA In addition, the outputs of a driver must not sustain damage if they are shorted together indefinitely (Entering thermal shutdown is allowed, of course.) Lastly, RS-485 drivers must source and sink large currents (60 mA) This situation requires outputs of rather large geometry, which provide robust ESD protection.

Special-Function Transceivers

You can handle many of the above-mentioned issues by using special transceivers, of which there are several types, differing in pinout or functions supported. The most common device is a standard transceiver (DS3695/DS75176B), which provides a two-pin connection to the RS-485 bus and a four-pin TTL interface (driver input, driver enable, receiver output, and receiver enable). Among the problems you can solve with an appropriate transceiver are these:

For ultra-low-power applications, the DS36C279 provides an auto-sleep function. Inactivity on the two enable lines automatically triggers the sleep mode, dropping the power-supply current to less than 10 µA. This characteristic is extremely valuable in applications that provide an interface connection but that are connected to their cables for down-loading only a small percentage of the time. This is the case for package-tracking boxes carried by many overnight-delivery services. With this sleep feature, idle transceivers do not consume precious battery current.

For applications that are asynchronous and based on a standard UART, fail-safe biasing is an issue. UARTs look for a low or a high state, and, between characters, the line usually remains high. With RS-485, this condition is troublesome, because, when there are no active drivers on the bus, the bus state is undetermined. (See the following section for a detailed discussion of fail-safe biasing.) In this case, the DS36276 simplifies the hardware design. This unique transceiver's receiver detects a high state for a driven high and also for the nondriven (V_{ID} = 0) bus state, thus providing the UART with the high state between characters and only valid start bits

Although the discussion of configurations and the section on stubs advises minimizing stub length to avoid transmission-line problems, the application may not permit minimizing stub length Another approach is to increase the driver's transition time to permit longer stubs without transmission-line effects. If you use the DS36C280, long stubs can branch off the main cable. This arrangement keeps the main cable short, whereas looping the cable back and forth to reach inconveniently located nodes would greatly increase the main-cable length. Besides allowing longer stubs, the slower edge rates generate lower emissions. Thus, this transceiver is also useful for applications that severely limit emitted noise.

Fail-Safe Biasing

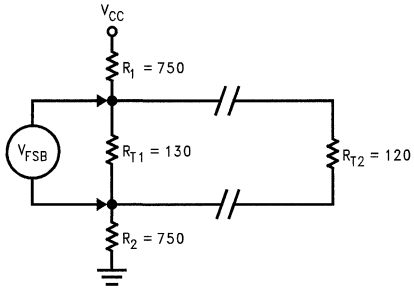
The need for fail-safe operation is both the principal application issue and most frequently encountered problem with RS-485. Fail-safe biasing provides a known state in which there are no active drivers on the bus. Other standards do not have to deal with this issue, because they typically define a point-to-point or multidrop bus with only one driver. The one driver either drives the line or is off. Because there is only one source on the bus, the bus is off when the driver is off. RS-485, on the other hand, allows for connection of multiple drivers to the bus. The bus is either active or idle. When it is idle with no drivers on, a question arises as to the state of the bus. Is it high, low, or in the state last driven? The answer is any of the above. With no active drivers and low-impedance termination resistors, the resulting differential voltage across the conductor pair is close to zero, which is in the middle of the receivers' thresholds. Thus, the state of the bus is truly undetermined and cannot be guaranteed.

Some of the functional protocols that many applications use aggravate this problem. In an asynchronous bus, the first transition indicates the start of a character. It is important for the bus to change states on this leading edge. Otherwise, the clocking inside the UART is out of sync with the character and creates a framing error. The idle bus can also randomly switch because of noise. In this case, the noise emulates a valid start bit, which the UART latches. The result is a framing error or, worse, an interrupt that distracts the CPU from other work.

The way to provide fail-safe operation requires only two additional resistors. At one end of the bus (the master node, for example), connect a pullup and pulldown resistor (*Figure 10*). This arrangement provides a simple voltage divider on the bus when there are no active drivers. Select the resistors so that at least 200 mV appears across the conductor pair. This voltage puts the receivers into a known state. Values that can provide this bias are 750Ω for the pullup and pulldown resistors, 130Ω across the conductor pair at the fail-safe point, and a 120Ω termination at the other end of the cable. For balance, use the same value for the pullup and pulldown resistors. Reference 4 provides extensive details on this issue.

Forethought into these 10 areas before production greatly reduces the likelihood of problems. RS-485 is unique in its capabilities and requirements. Fully understanding these 10 issues leads to a rock-solid, trouble-free, multipoint differential interface that maximizes the benefits of RS-485 and provides the application with robust, rugged, highly noise-tolerant data communication.

Fail-Safe Biasing (Continued)



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Unless you do something to keep the situation from occurring, when no driver is driving the bus, the receivers cannot determine the bus state Fail-safe biasing is a bus-termination method, which ensures that, even when no driver is active, a differential voltage large enough to unambiguously determine the bus state appears at the receiver inputs

FIGURE 10.

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Understanding the Power Supply Requirements of PCI Bus Standard-How to Protect the Digital Components

National Semiconductor
Application Note 1077
Mary Kao
Dave Mishler

Until recently, PCI systems primarily used 5V components. But as submicron process technology advances, the trend is to support mixed voltage components in the newer PCI systems. As a result, power supply requirements on mixed voltage PCI systems are getting increasing attention from the design community. Understanding and designing to these requirements will prevent any power supply variations from damaging PCI components. These requirements are defined in the analog portion of the PCI Specification Revision 2.1. They specifically deal with 5V and 3.3V mixed-voltage environment.

This article provides a guide to the PCI system designers. The analog portion of the PCI 2.1 is scattered in various sections of the document. This article compiles all the analog requirements in *Table 1* and explains the requirements in detail.

Inside a typical computer, there are ±12V, ±5V and +3.3V power supplies. The analog portion of PCI Specification Revision 2.1 focuses on the +5V and +3.3V power supply requirements, because the PCI local bus and add-in cards may run on either or both voltages. The requirements outline what actions must be taken when the supply voltages are out of tolerance, as in Section 4.3.2 of PCI 2.1. It also describes possible behaviors of supply voltages that may destroy PCI components. Real danger exists if these requirements are ignored. Therefore, building a robust PCI system demands a solution to address the issues discussed above. This responsibility falls on the PCI system architecture designers and system design engineers.

Table 1 lists the sections in the PCI Specification Revision 2.1 that cover the analog requirements. Specs I and II establish the ±5% initial tolerance for 5V supply. Specs III and IV establish ±9% initial tolerance for 3.3V supply.

TABLE 1. Analog Requirements Found in PCI Specification Revision 2.1

	PCI Local Bus Specification Revision 2.1	Where to Find Spec	Page #
I	Maximum for 5V Supply Voltage 5.25V *see Spec V	Section 4.2.1.1 Table 4.1	123
II	Minimum for 5V Supply Voltage 4.75V *see Spec V	Section 4.2.1.1 Table 4.1	123
III	Maximum for 3.3V Supply Voltage 3.6V *see Spec V	Section 4.2.2.1 Table 4.3	128
IV	Minimum for 3.3V Supply Voltage 3.0V *see Spec V	Section 4.2.2.1 Table 4.3	128
V	The value of T_{fail} is the minimum of 500 ns (maximum) from either power rail going out of specifications *(exceeding specified tolerances by more than 500 mV). 100 ns (maximum) from the 5V rail failing below 3.3V rail by more than 500 mV.	Section 4.3.2 Reset Section	139
VI	Anytime $\overline{RST}$ is asserted, all PCI output signals must be driven to their benign state. In general, this means they must be asynchronously tri-stated.	Section 2.2.1 $\overline{RST}$ Section	9
VII	Clamping directly to the 3.3V rail with a simple diode must never be used in the 5V signaling environment. When dual power rails are used, parasitic diode paths can exist from one supply to another. These diode paths can become significantly forward biased (conducting) if one of the power rails goes out of spec momentarily. Diode clamps to a power rails as well as to output pull-up devices, must be able to withstand short circuit current until drivers can be tri-stated. Refer to Section 4.3.2 for more information.	Section 4.2.1.2 (refer to the article for more information)	126

TABLE 1. Analog Requirements Found in PCI Specification Revision 2.1 (Continued)

	PCI Local Bus Specification Revision 2.1	Where to Find Spec	Page #
VIII	There is no specified sequence in which the four power rails (12V, -12V, 5V and 3.3V) are activated or deactivated. They may come up and go down in any order. The system must assert $\overline{RST}$ both at power up and whenever either the 5V or 3.3V rails go out of spec (per Section 4.3.2). During reset, all PCI signals are driven to a "safe" state, as described in Section 4.3.2.	Section 4.3.4.2 (refer to the article for more information)	142

Spec V establishes an additional ±500 mV on both of the 5V and 3.3V supplies for noise margin consideration. Moreover, Spec V states that if either the 5V supply or the 3.3V supply is out of limit, a $\overline{RST}$ signal has to be asserted within 500 ns. For example, if 5V supply is over 5.75V, $\overline{RST}$ has to be asserted within 500 ns. The worst case in Spec V, and a potentially destructive case, is if 5V supply falls below 3.3V supply by more than 300 mV. $\overline{RST}$ signal has to be asserted within 100 ns when this occurs.

Spec VI requires that all PCI output signals be tri-stated once $\overline{RST}$ is asserted. Tri-stating the PCI devices will prevent any current flowing from the PCI devices to damage other PCI devices connected to the PCI bus.

Spec VII describes possible dangers of protection diodes being turned on in mixed voltage environment. In the event that a protection diode is clamped directly to 3.3V supply in an 3.3V I/O device, it will be forwarded biased when the input of the I/O is coming from 5V devices. This is shown in *Figure 1.* Possibly, a large amount of current will flow from 5V outputs into the 3.3V device through the protection diode, damaging the 3.3V device. Consequently, Spec VII advises never to clamp a diode directly to 3.3V supply in 5V signaling environment.

Specs VII describes another situation where the current flow is from 3.3V supply to 5V supply. In the case when 5V supply is accidently crowbarred to ground, a current path exists between 3.3V supply and 5V supply (now ground), shown in *Figure 2.* The current flows from the 3.3V device through the PCI bus into the 5V device. Since the 5V supply is now ground, the input protection diode inside the 5V device becomes forward biased, allowing the large current to pass through, possibly damaging the 5V device. Spec V and VI protect the 5V device by asserting $\overline{RST}$ in 100 ns when the 5V falls below 3.3V by more than 300 mV. Upon $\overline{RST}$ assertion, all PCI output signals will be tri-stated.

The 5V and the 3.3V devices in *Figure 2* can be part of a discrete logic, chipset, or ASIC.

Spec VIII points out another threat that mixed voltage supplies have on PCI components. PCI 2.1 does not guarantee power-up and power-down sequences. As as example of Spec VIII, consider the instance where 3.3V supply comes up before 5V supply. If 5V rises slowly, staying under 3.3V, there can be a current path from 3.3V supply to 5V supply through the protection diode inside the 5V logic. Destruction can happen. The same principle applies when 3.3V power supply goes to ground slower than 5V. Spec V prevents disasters by asserting $\overline{RST}$ until supplies are within their limits.

A second example on Spec VIII is the case where 5V and 3.3V supplies are independently regulated from the main power supply. If the 5V supply momentarily fails, 5V devices can suffer from electrical overstress resulting from current flowing from 3.3V to 5V through the 5V device input protection diodes. Again, Spec V saves the situation by asserting $\overline{RST}$ when 5V is out of limit.

A third example of Spec VIII is the case where 3.3V is generated from 5V via a linear regulator either in the main power supply or add-in cards. Some regulators do not provide current limiting on 3.3V output. Electrical overstress can damage the pass transistor inside the regulator, allowing the 3.3V to rise to 5V. This would exceed the operating voltage range on the 3.3V devices. PCI 2.1 provides over-voltage protection by asserting $\overline{RST}$ to tri-state outputs in this situation.

Mixed voltage environment presents a new challenge to the PCI system architecture designers. With so many different power supply sources using various implementations, it is very difficult to ensure that a power supply complies with PCI 2.1 at all times. Many believe that PCI voltage monitoring is the responsibility of the power supply section. Today, this is not the case. A PCI system designer has no control of power supplies and add-in cards. However, he does have control of the motherboard. Therefore, it is far better to design the protection function that will monitor all types of power supplies and add-in cards on the motherboard. As a reference, *Table 2* shows some safe and unsafe conditions in mixed voltage PCI systems.

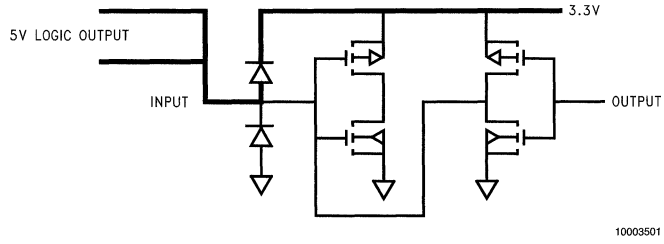


FIGURE 1. Possible Current Diode Path from 5V to 3.3V via 3.3V Clamp Diode

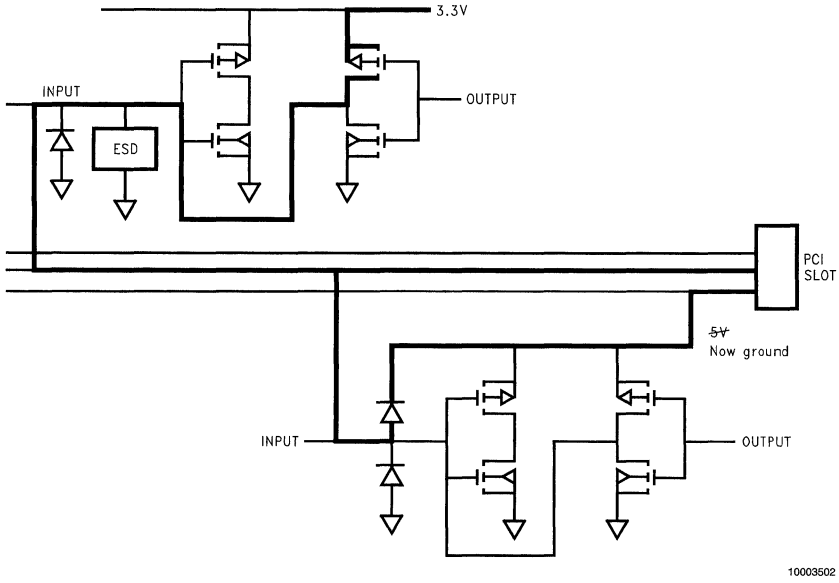


FIGURE 2. Possible Current Diode Path from 3.3V to 5V when 5V is Crowbarred

TABLE 2. Safe and Unsafe Conditions in Mixed Voltage PCI Systems

UNSAFE CONDITIONS:
3.3V supply coming up before 5V supply.
5V and 3.3V power supplies are independently regulated from the main power supply.
3.3V is generated from 5V via linear regulator.
Any 3.3V logic IC that is not 5V tolerant and does not use buffers that are 5V tolerant to drive directly on the PCI bus.
SAFE CONDITIONS:
PCI bus is 5V only or 3.3V only This includes PCI add-in cards.
3.3V logic is 5V tolerant. This includes any I/O being directly connected to the PCI bus. Mixed 5V and 3.3V have compatible logic levels.
Any 3.3V logic IC's that are not 5V tolerant use buffers that are 5V tolerant to drive directly on the PCI bus. This applies to motherboard as well as add-in cards.

National Semiconductor recognizes the need for monitoring power supplies in PCI environment to ensure system integrity and safety. The LMC6953 PCI power supply monitor IC is designed to comply with PCI 2.1, meeting all the analog requirements. It fully addresses all the specs discussed.

There are five comparators inside the LMC6953. Two of them monitor over-voltage and under-voltage on the 5V supply; two other monitor the over-voltage and under-voltage on the 3.3V supply. The fifth one is a differential comparator monitoring for power failure - 5V going 300 mV below 3.3V. The LMC6953 also has a 5V/3.3V logic compatible interrupt pin. During power-up, the LMC6953 holds $\overline{RST}$ low for 100 ms (as required by Section 4.3.2, Figure 4.12 on page 140 of PCI 2.1) after both 5V and 3.3V supplies are within their specified windows. It asserts $\overline{RST}$ within 490 ns when an over-voltage or an under-voltage is detected. In case of power failure or momentary fault where the 5V supply falls below 3.3V supply by 300 mV maximum, $\overline{RST}$ is asserted within 90 ns.

$\overline{RST}$ also can be instantly asserted by sending a CMOS logic low to the manual interrupt pin. Each time $\overline{RST}$ is asserted, it holds low for 100 ms after all fault conditions are recovered. The 100 ms delay is generated by the 0.01 µF C_{EXT} capacitor, and can be adjusted by changing the value of C_{EXT}.

The LMC6953 is designed for desktop PC motherboards or add-in cards. *Figure 3* shows the LMC6953 monitoring the 5V and 3.3V power supplies from the power supplies and asserting $\overline{RST}$ to the system controllers in case of a fault condition. $\overline{RST}$ from the LMC6953 has an open-drain output and can be ORed to different system controllers. If monitoring a third voltage is desired, for example, 12V, it can be achieved by voltage dividing the 12V down to 2.5V and connecting it to the manual reset input. Furthermore, the manual reset input can, at the same time, accept a logic output and the divided-down 12V, as shown in *Figure 4.*

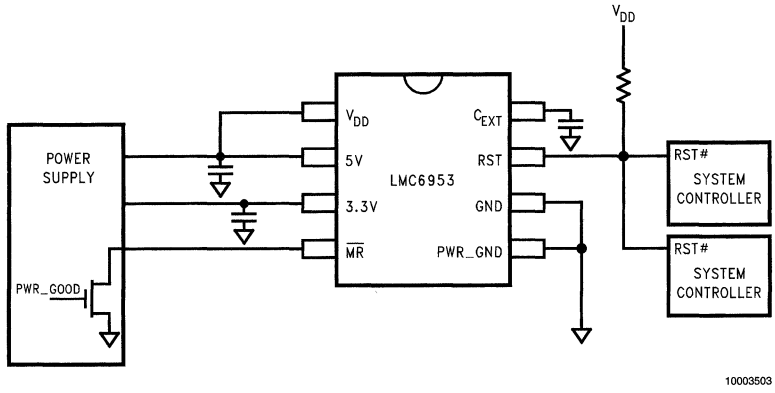


FIGURE 3. Typical Application Circuit using the LMC6953 on a Motherboard

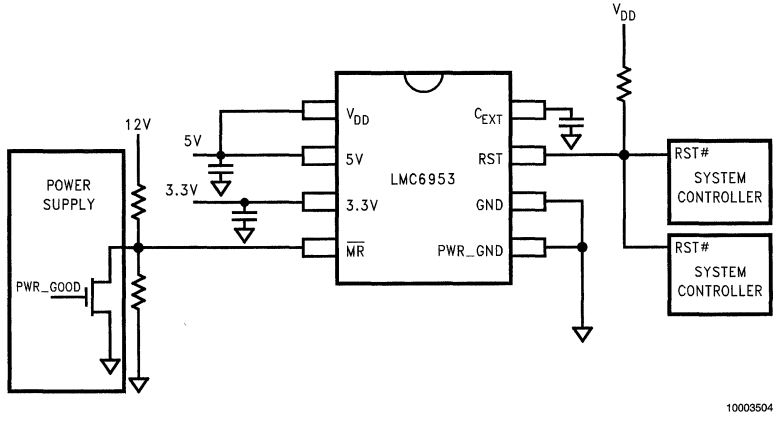


FIGURE 4. Using LMC6953 to Monitor Three Different Voltages

Power supplies do not provide any functions defined in PCI 2.1. In fact, power supplies have such diverse designs that the only sure way to design a PCI-compliant system is to include the power supply monitoring functions on the motherboard. The LMC6953 is designed for that purpose. It offers an integrated solution that completely covers the power supply requirements in PCI 2.1. Designing the LMC6953 into a mixed voltage PCI system will protect the digital components in that system. The LMC6953 asserts $\overline{RST}$ to the system controllers when there is a fault condition on the supply voltages. The $\overline{RST}$ in turn drives all PCI output signals to their benign state, preventing destructive events due to any of the conditions listed in *Table 1*.

There are datasheets, demonstration boards and powerpoint presentation to aid designers and the sales force to learn more about the LMC6953 as well as gaining further insight into this subject.

Section 8
Packaging

Section 8 Contents

Understanding Integrated Circuit Package Power Capabilities

National Semiconductor
Application Note 336
Charles Carinalli
Josip Huljev

Introduction

The short and long term reliability of National Semiconductor's interface circuits, like any integrated circuit, is very dependent on its environmental condition. Beyond the mechanical/environmental factors, nothing has a greater influence on this reliability than the electrical and thermal stress seen by the integrated circuit. Both of these stress issues are specifically addressed on every interface circuit data sheet, under the headings of Absolute Maximum Ratings and Recommended Operating Conditions.

However, through application calls, it has become clear that electrical stress conditions are generally more understood than the thermal stress conditions Understanding the importance of electrical stress should never be reduced, but clearly, a higher focus and understanding must be placed on thermal stress. Thermal stress and its application to interface circuits from National Semiconductor is the subject of this application note.

Factors Affecting Device Reliability

Figure 1 shows the well known "bathtub" curve plotting failure rate versus time. Similar to all system hardware (mechanical or electrical) the reliability of interface integrated circuits conform to this curve. The key issues associated with this curve are infant mortality, failure rate, and useful life.

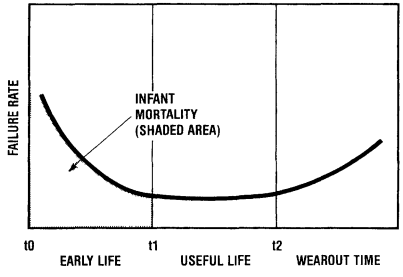


FIGURE 1. Failure Rate vs Time

Infant mortality, the high failure rate from time t0 to t1 (early life), is greatly influenced by system stress conditions other than temperature, and can vary widely from one application to another. The main stress factors that contribute to infant mortality are electrical transients and noise, mechanical maltreatment and excessive temperatures. Most of these failures are discovered in device test, burn-in, card assembly and handling, and initial system test and operation. Although important, much literature is available on the subject of infant mortality in integrated circuits and is beyond the scope of this application note.

Failure rate is the number of devices that will be expected to fail in a given period of time (such as, per million hours). The mean time between failure (MTBF) is the average time (in hours) that will be expected to elapse after a unit has failed before the next unit failure will occur. These two primary "units of measure" for device reliability are inversely related:

$$\text{MTBF} = \frac{1}{\text{Failure Rate}}$$

Although the "bathtub" curve plots the overall failure rate versus time, the useful failure rate can be defined as the percentage of devices that fail per-unit-time during the flat portion of the curve. This area, called the useful life, extends between t1 and t2 or from the end of infant mortality to the onset of wearout. The useful life may be as short as several years but usually extends for decades if adequate design margins are used in the development of a system.

Many factors influence useful life including: pressure, mechanical stress, thermal cycling, and electrical stress. However, die temperature during the device's useful life plays an equally important role in triggering the onset of wearout.

Failure Rates vs Time and Temperature

The relationship between integrated circuit failure rates and time and temperature is a well established fact. The occurrence of these failures is a function which can be represented by the Arrhenius Model. Well validated and predominantly used for accelerated life testing of integrated circuits, the Arrhenius Model assumes the degradation of a performance parameter is linear with time and that MTBF is a function of temperature stress. The temperature dependence is an exponential function that defines the probability of occurrence. This results in a formula for expressing the lifetime or MTBF at a given temperature stress in relation to another MTBF at a different temperature. The ratio of these two MTBFs is called the acceleration factor F and is defined by the following equation:

$$F = \frac{X1}{X2} = \exp\left[\frac{E}{K}\left(\frac{1}{T2} - \frac{1}{T1}\right)\right]$$

Where: X1 = Failure rate at junction temperature T1

X2 = Failure rate at junction temperature T2

T = Junction temperature in degrees Kelvin

E = Thermal activation energy in electron volts (ev)

K = Boltzman's constant

However, the dramatic acceleration effect of junction temperature (chip temperature) on failure rate is illustrated in a plot of the above equation for three different activation energies in *Figure 2*. This graph clearly demonstrates the impor-

8

Failure Rates vs Time and Temperature (Continued)

tance of the relationship of junction temperature to device failure rate. For example, using the 0.99 ev line, a 30° rise in junction temperature, say from 130°C to 160°C, results in a 10 to 1 increase in failure rate.

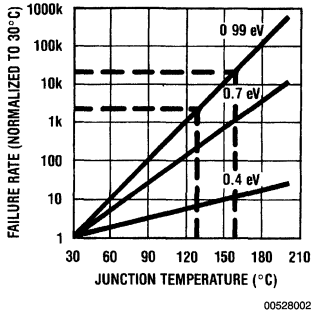


FIGURE 2. Failure Rate as a Function of Junction Temperature

Device Thermal Capabilities

There are many factors which affect the thermal capability of an integrated circuit. To understand these we need to understand the predominant paths for heat to transfer out of the integrated circuit package. This is illustrated by *Figure 3* and *Figure 4.*

Figure 3 shows a cross-sectional view of an assembled integrated circuit mounted into a printed circuit board.

Figure 4 is a flow chart showing how the heat generated at the power source, the junctions of the integrated circuit flows from the chip to the ultimate heat sink, the ambient environment. There are two predominant paths. The first is from the die to the die attach pad to the surrounding package material to the package lead frame to the printed circuit board and then to the ambient. The second path is from the package directly to the ambient air.

Improving the thermal characteristics of any stage in the flow chart of *Figure 4* will result in an improvement in device thermal characteristics. However, grouping all these characteristics into one equation determining the overall thermal capability of an integrated circuit/package/environmental condition is possible. The equation that expresses this relationship is:

$$T_J = T_A + P_D (\theta_{JA})$$

Where: T_J = Die junction temperature

T_A = Ambient temperature in the vicinity device

P_D = Total power dissipation (in watts)

θ_{JA} = Thermal resistance junction-to-ambient

θ_{JA}, the thermal resistance from device junction-to-ambient temperature, is measured and specified by the manufacturers of integrated circuits. National Semiconductor utilizes special vehicles and methods to measure and monitor this parameter. All interface circuit data sheets specify the thermal characteristics and capabilities of the packages available for a given device under specific conditions—these package power ratings directly relate to thermal resistance junction-to-ambient or θ_{JA}.

Although National provides these thermal ratings, it is critical that the end user understand how to use these numbers to improve thermal characteristics in the development of his system using interface components.

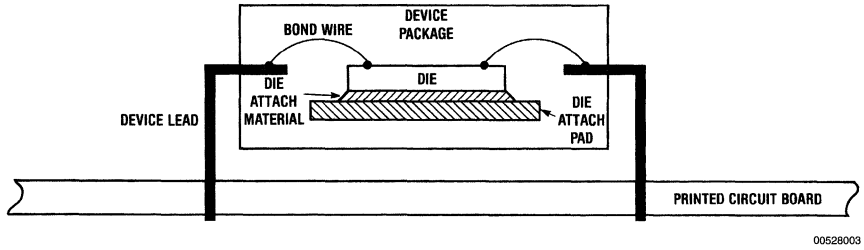


FIGURE 3. Integrated Circuit Soldered into a Printed Circuit Board (Cross-Sectional View)

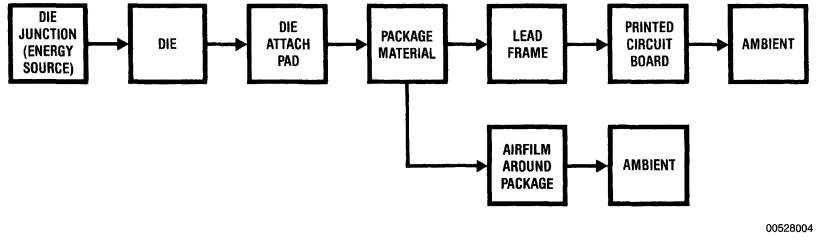


FIGURE 4. Thermal Flow (Predominant Paths)

Determining Device Operating Junction Temperature

From the above equation the method of determining actual worst-case device operating junction temperature becomes straightforward. Given a package thermal characteristic, θ_{JA}, worst-case ambient operating temperature, T_A(max), the only unknown parameter is device power dissipation, P_D. In calculating this parameter, the dissipation of the integrated circuit due to its own supply has to be considered, the dissipation within the package due to the external load must also be added. The power associated with the load in a dynamic (switching) situation must also be considered. For example, the power associated with an inductor or a capacitor in a static versus dynamic (say, 1 MHz) condition is significantly different.

The junction temperature of a device with a total package power of 600 mW at 70°C in a package with a thermal resistance of 63°C/W is 108°C.

$$T_J = 70°C + (63°C/W) \times (0.6W) = 108°C$$

The next obvious question is, "how safe is 108°C?"

Maximum Allowable Junction Temperatures

What is an acceptable maximum operating junction temperature is in itself somewhat of a difficult question to answer. Many companies have established their own standards based on corporate policy. However, the semiconductor industry has developed some defacto standards based on the device package type. These have been well accepted as numbers that relate to reasonable (acceptable) device lifetimes, thus failure rates.

National Semiconductor has adopted these industry-wide standards. For devices fabricated in a molded package, the maximum allowable junction temperature is 150°C. For these devices assembled in ceramic or cavity DIP packages, the maximum allowable junction temperature is 175°C. The numbers are different because of the differences in package types. The thermal strain associated with the die package interface in a cavity package is much less than that exhibited in a molded package where the integrated circuit chip is in direct contact with the package material.

Let us use this new information and our thermal equation to construct a graph which displays the safe thermal (power) operating area for a given package type. *Figure 5* is an example of such a graph. The end points of this graph are easily determined. For a 16-pin molded package, the maximum allowable temperature is 150°C; at this point no power dissipation is allowable. The power capability at 25°C is 1.98W as given by the following calculation:

$$P_D @ 25°C = \frac{T_J(max) - T_A}{\theta_{JA}} = \frac{150°C - 25°C}{63°C/W} = 1.98W$$

The slope of the straight line between these two points is minus the inversion of the thermal resistance. This is referred to as the derating factor.

$$\text{Derating Factor} = -\frac{1}{\theta_{JA}}$$

As mentioned, *Figure 5* is a plot of the safe thermal operating area for a device in a 16-pin molded DIP. As long as the intersection of a vertical line defining the maximum ambient temperature (70°C in our previous example) and maximum device package power (600 mW) remains below the maximum package thermal capability line the junction temperature will remain below 150°C—the limit for a molded package. If the intersection of ambient temperature and package power fails on this line, the maximum junction temperature will be 150°C. Any intersection that occurs above this line will result in a junction temperature in excess of 150°C and is not an appropriate operating condition.

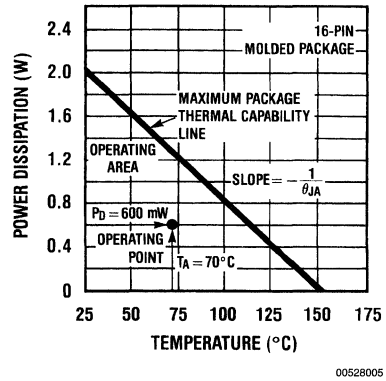


FIGURE 5. Package Power Capability vs Temperature

The thermal capabilities of all interface circuits are expressed as a power capability at 25°C still air environment with a given derating factor. This simply states, for every degree of ambient temperature rise above 25°C, reduce the package power capability stated by the derating factor which is expressed in mW/°C. For our example—a θ_{JA} of 63°C/W relates to a derating factor of 15.9 mW/°C.

Factors Influencing Package Thermal Resistance

As discussed earlier, improving any portion of the two primary thermal flow paths will result in an improvement in overall thermal resistance junction-to-ambient. This section discusses those components of thermal resistance that can be influenced by the manufacturer of the integrated circuit. It also discusses those factors in the overall thermal resistance that can be impacted by the end user of the integrated circuit. Understanding these issues will go a long way in understanding chip power capabilities and what can be done to insure the best possible operating conditions and, thus, best overall reliability.

DIE SIZE

Figure 6 shows a graph of our 16-pin DIP thermal resistance as a function of integrated circuit die size Clearly, as the chip size increases the thermal resistance decreases—this relates directly to having a larger area with which to dissipate a given power.

Factors Influencing Package Thermal Resistance (Continued)

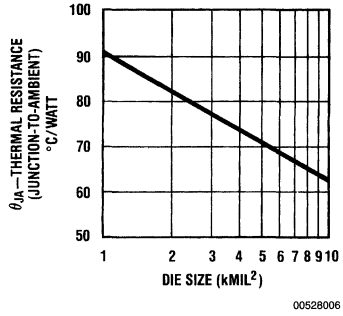


FIGURE 6. Thermal Resistance vs Die Size

PIN COUNT

For higher pin count packages such as Plastic Quad Flat Packages (PQFPs), *Figure 7* shows the range of thermal resistances for a number of different package pin counts, from 44 to 160-lead. Better thermal dissipation is achieved with the larger packages. The values observed depend on the die and corresponding paddle sizes.

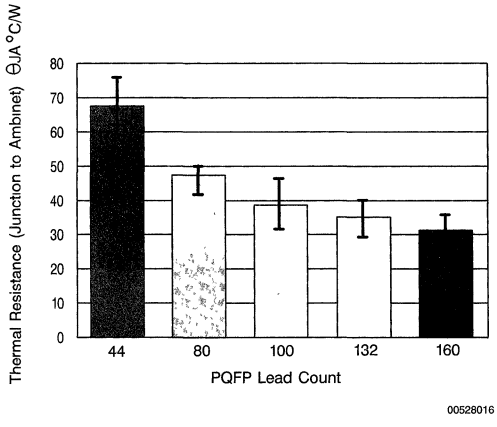


FIGURE 7. Thermal resistance for the PQFP family of packages. The bars on the data points indicate the variation of the thermal resistance. This variation is dependent on the device size and the die attach paddle size.

LEAD FRAME MATERIAL

Figure 8 shows the influence of lead frame material (both die attach and device pins) on thermal resistance. This graph compares our same 16-pin DIP with a copper lead frame, a Kovar lead frame, and finally an Alloy 42 type lead frame—these are lead frame materials commonly used in the industry. Obviously the thermal conductivity of the lead frame material has a significant impact in package power capability. Molded interface circuits from National Semiconductor use the copper lead frame exclusively.

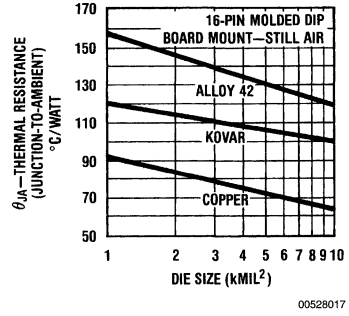


FIGURE 8. Thermal Resistance vs Lead Frame Material

BOARD vs SOCKET MOUNT

One of the major paths of dissipating energy generated by the integrated circuit is through the device leads. As a result of this, the graph of *Figure 9* comes as no surprise. This compares the thermal resistance of our 16-pin package soldered into a printed circuit board (board mount) compared to the same package placed in a socket (socket mount). Adding a socket in the path between the PC board and the device adds another stage in the thermal flow path, thus increasing the overall thermal resistance. The thermal capabilities of National Semiconductor's interface circuits are specified assuming board mount conditions. If the devices are placed in a socket the thermal capabilities should be reduced by approximately 5% to 10%.

An example of the thermal resistance observable for board mounted packages is illustrated in *Figure 10*. In this case, the typical thermal resistance is shown for three TO-263 packages mounted on a PC board with 1 oz copper. A rapid drop in thermal resistance is observed, albeit the gain has diminishing returns as the copper surface area is enlarged.

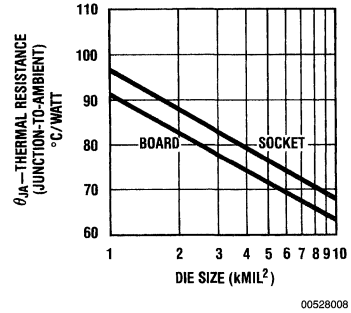
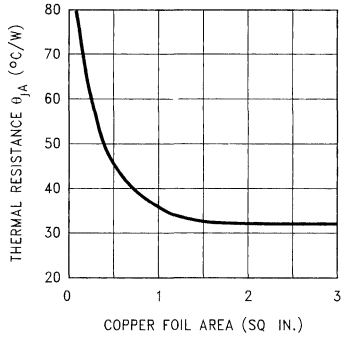


FIGURE 9. Thermal Resistance vs Board or Socket Mount

Factors Influencing Package Thermal Resistance (Continued)



*For products with high current ratings (>3A), thermal resistance may be lower Consult product datasheet for more information

FIGURE 10. Thermal Resistance (typ.*) for 3-, 5-, and 7-L TO-263 packages mounted on 1 oz. (0.036mm) PC board foil

AIR FLOW

When a high power situation exists and the ambient temperature cannot be reduced, the next best thing is to provide air flow in the vicinity of the package. Forced convection around packages mounted on boards can be divided into laminar flow and turbulent flow. The transition from laminar to turbulent occurs at a typical velocity of 180 feet per minute (180 LFPM). In laminar flow, the fluid particles follow a smooth path, while on the other hand, turbulent flow is characterized by irregular motion of fluid "eddies" in which particles are continuously re-arranged and mixed. Greater heat transfer is obtained with turbulent flow. *Figure 11* and *Figure 12* illustrate the impact of air flow on the thermal resistance of a 16-pin DIP and a 100-pin PQFP, respectively. The thermal ratings on National Semiconductor's interface circuits data sheets relate to the still air environment.

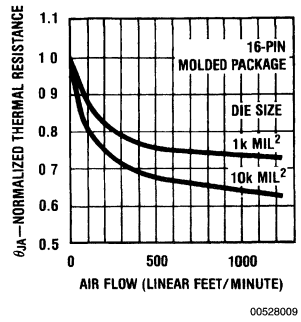


FIGURE 11. Thermal Resistance vs Air Flow (16-pin DIP)

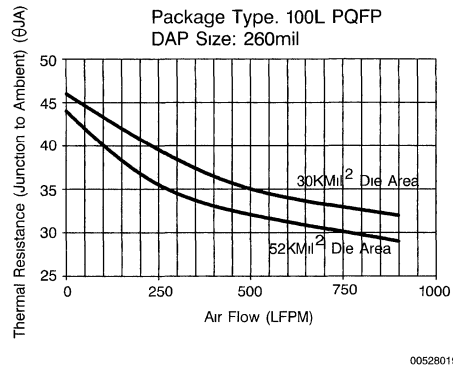


FIGURE 12. Effect of air flow on a 100 lead PQFP mounted on a JEDEC thermal board. The package has a die attach paddle size of 260x260 mil. The data also shows the effect on two different device sizes.

Factors Influencing Package Thermal Resistance (Continued)

OTHER FACTORS

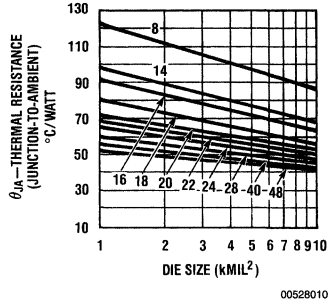
A number of other factors influence thermal resistance. The most important of these is using thermal epoxy in mounting ICs to the PC board and heat sinks. Generally these techniques are required only in the very highest of power applications.

Some confusion exists between the difference in thermal resistance junction-to-ambient (θ_{JA}) and thermal resistance junction-to-case (θ_{JC}). The best measure of actual junction temperature is the junction-to-ambient number since nearly all systems operate in an open air environment. The only situation where thermal resistance junction-to-case is important is when the entire system is immersed in a thermal bath and the environmental temperature is indeed the case temperature. This is only used in extreme cases and is the exception to the rule and, for this reason, is not addressed in this application note.

National Semiconductor Package Capabilities

Figure 13 and *Figure 14* show composite plots of the thermal characteristics of the most common package types in the National Semiconductor Interface Circuits product family. *Figure 13* is a composite of the copper lead frame molded package. *Figure 14* is a composite of the ceramic (cavity) DIP using poly die attach. These graphs represent board mount still air thermal capabilities. Another, and final, thermal resistance trend will be noticed in these graphs. As the number of device pins increase in a DIP the thermal resistance decreases. Referring back to the thermal flow chart, this trend should, by now, be obvious.

Molded (N Package) DIP* Copper Leadframe—HTP Die Attach Board Mount— Still Air



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 40-pin 0.6 mil width

FIGURE 13. Thermal Resistance vs Die Sizevs Package Type (Molded Package)

Ratings On Interface Circuits Data Sheets

In conclusion, all National Semiconductor Interface Products define power dissipation (thermal) capability. This information can be found in the Absolute Maximum Ratings section of the data sheet. The thermal information shown in this application note represents average data for characterization of the indicated package. Actual thermal resistance can vary from ±10% to ±15% due to fluctuations in assembly quality, die shape, die thickness, distribution of heat sources on the die, etc. The numbers quoted in the interface data sheets reflect a 15% safety margin from the average numbers found in this application note. Insuring that total package power remains under a specified level will guarantee that the maximum junction temperature will not exceed the package maximum.

The package power ratings are specified as a maximum power at 25°C ambient with an associated derating factor for ambient temperatures above 25°C. It is easy to determine the power capability at an elevated temperature. The power specified at 25°C should be reduced by the derating factor for every degree of ambient temperature above 25°C. For example, in a given product data sheet the following will be found:

Maximum Power Dissipation* at 25°C

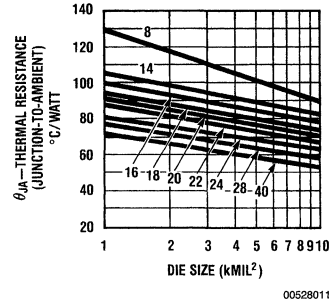
Cavity Package	1509 mW
Molded Package	1476 mW

Note: Derate cavity package at 10 mW/°C above 25°C, derate molded package at 11.8 mW/°C above 25°C

If the molded package is used at a maximum ambient temperature of 70°C, the package power capability is 945 mW.

P_D @ 70°C=1476 mW–(11.8 mW/°C)x(70°C–25°C)
= 945 mW

Cavity (J Package) DIP* Poly Die Attach Board Mount—Still Air



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 48-pin 0.6 mil width

FIGURE 14. Thermal Resistance vs Die Size vs Package Type (Cavity Package)

Micro SMD Wafer Level Chip Scale Package

National Semiconductor
Application Note 1112
Charles Carinalli
Josip Huljev

Introduction to MICRO SMD

Micro SMD is a wafer level CSP (WLCSP) with the following features:

1. Package size equal to die size.
2. Smallest footprint per I/O count.
3. No need for underfill material.
4. Interconnect layout at 0.5 mm pitch.
5. No interposer between the silicon IC and the printed circuit board.

Package Construction

Figure 1 shows typical micro SMD products. They have solder bumps located on the active side of silicon IC. The micro SMD is offered in the standard and thin version. The micro SMD manufacturing process steps include standard wafer fabrication process, wafer re-passivation, deposition of eutectic solder bumps on i/o pads, backgrinding (for thin version only), application of protective encapsulation coating, testing using wafer sort platform, laser marking, singulation and packing in tape and reel. The package is assembled on PCB using standard surface mount assembly techniques (SMT).

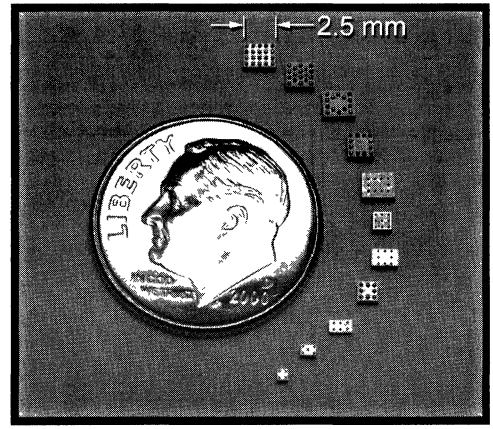


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FIGURE 1. Micro SMD 4-20 Bump

MICRO SMD Package Data

Package Arrays

Bump Count	4	5	6	8	9	10	12	14	16	18	20
Array Outline	2 x 2	2 x 1 x 2	3 x 2	3 x 3 (perimeter)	3 x 3 (area)	4 x 3 (perimeter)	4 x 4 (perimeter)	5 x 4 (stagger perimeter)	4 x 4 (area)	5 x 4 (stagger area)	4 x 5 (area)

Bump Size Options

	Small bump size (0.17 mm diameter)	**Large bump size (0.3 mm diameter)**
I/O Count Range	4 - 9	5 - 20
Pitch (mm)	0.5	0.5
Standard Package Thickness Nominal (mm) for 150 mm / 200 mm Wafer Diameter	0.875 / 0.95	0.975 / 1.05
Thin Package Thickness Nominal (mm) for 150 mm / 200 mm Wafer Diameter	0.5	0.6
Bump Diameter (mm)	0.16 - 0.18	0.29 - 0.31
Bump Height (mm)	0.11 - 0.14	0.21 - 0.24
Bump Coplanarity (mm)	± 0.015	± 0.015
Shipping Media	Tape & Reel	Tape & Reel
Moisture Sensitivity Level	Level 1	Level 1

Surface Mount Assembly Considerations

Micro SMD surface mount assembly operations include,

- Printing solder paste on PCB.
- Component placement using standard pick and place equipment.
- Solder reflow and cleaning (depending on flux type).

Advantages of micro SMD during SMT assembly include,

- Standard tape and reel shipping media eases handling issues (per EIA-481-1)
- Uses standard SMT pick and place equipment.
- Standard reflow process.

PCB Layout

Two types of land patterns are used for surface mount packages,

1. Non-solder mask defined (NSMD)
2. Solder mask defined (SMD).

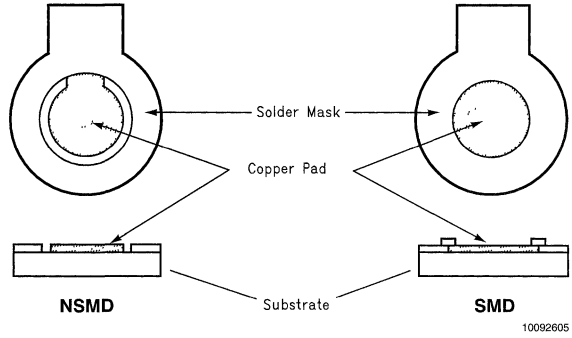

FIGURE 2. NSMD and SMD Pad Definition

1. NSMD configuration is preferred due to its tighter control on copper etch process and a reduction in the stress concentration points on the PCB side compared to SMD configuration.
2. A copper layer thickness of less than 1 oz is recommended to achieve higher stand-off. A 1 oz. (30 micron) or greater copper thickness results in a lowering of the effective stand-off, which may compromise solder joint reliability.
3. For the NSMD pad geometry, the trace width at the connection to the land pad should not exceed 2/3 of the pad diameter.

The recommended pad geometry is shown in *Table 1*.

TABLE 1. Recommended PCB Pad Geometry

	Small Bump Size (0.17 mm Diameter)		Large Bump Size (0.3 mm Diameter)	
Pad Definition	**Copper Pad**	**Solder Mask Opening**	**Copper Pad**	**Solder Mask Opening**
NSMD	0.175 +0.0/–0.025 mm	0.350 ± 0.025 mm	0.275 +0.0/–0.025 mm	0.375 ± 0.025 mm
SMD	0.350 ± 0.025 mm	0.175 ± 0.025 mm	0.375 +0.0/–0.025 mm	0.275 ± 0.025 mm

For PCB layouts employing via-in-pad structures (micro-via), NSMD pad definition should be used, since this ensures adequate wetting area on the copper pads and hence a better joint.

Organic solderability preservative coating (OSP) board finish is used for internal characterization. Allowable board finishes are Copper-OSP and Nickel-Gold.

- For Ni-Au (electroplated Nickel, immersion Gold) gold thickness must be less than 0.5 microns to avoid solder joint embrittlement.
- The fan-out for the traces should be symmetrical across X and Y directions to avoid part rotation due to surface tension of solder.
- HASL (Hot Air Solder Leveled) board finish is not recommended.

Stencil Printing Process

- Use laser cutting followed by electro-polishing for stencil fabrication.
- The recommended stencil apertures are shown in *Table 2*.
- If possible, offset apertures from land pads to maximize separation and minimize possibility of bridging for micro SMD packages with less than 10 bump counts and using small bump size. No print offset is required for higher bump counts and larger bump size.
- Use Type 3 (25 to 45 micron particle size range) or finer solder paste for printing.

Stencil Printing Process (Continued)

TABLE 2. Recommended Stencil Apertures

	0.17 mm Diameter Solder Bump	0.3 mm Diameter Solder Bump
Recommended Stencil Aperture Size	0.3 x 0.3 mm square, 0.125 mm thick	0.25 x 0 25 mm square, 0.125 mm thick

Component Placement

Standard pick-and-place machines can be used for placing the micro SMD. Either of the following methods can be used for recognition and positioning.

1. Vision system to locate package silhouette.
2. Vision system to locate individual bumps (slower and more expensive)

Other features of micro SMD placement are,

1. It is preferable to use IC placement/fine pitch placement machines over chip-shooters for better accuracy.
2. Micro SMD solder bumps self-align when placed at an offset due to selfcentering nature of solder bumps.
3. Though micro SMD can withstand a placement force of up to 1 kg for 0.5 seconds, little or no force needs to be exerted during placement. It is recommended that bumps be dipped into solder paste on PCB to greater than 20% of paste block height.

Solder Paste Reflow and Cleaning

- Micro SMD is compatible with industry standard reflow process.
- It is recommended to use Nitrogen purge during reflow
- Micro SMD is qualified for up to three reflow operations (235° C peak) per J-STD-020.
- Micro SMD can withstand peak reflow temperatures of 260° C for up to 30 seconds.

Rework

The key features for the micro SMD rework are listed below

1. Rework procedure used is identical to the one used for most BGA and CSP packages
2. Rework reflow process should duplicate original reflow profile used for assembly
3. Rework system should include localized convection heating element with profiling capability, a bottom side pre-heater and a part pick and placer with image overlay.
4. A rework demo video is available from National Semiconductor at http://www national com/appinfo/microsmd.

Qualification

The following sections describe solder joint reliability qualification and mechanical testing results for micro SMD when mounted on FR-4 PCB. Testing included use of daisy chain components. Product reliability data is included in respective product qualification reports.

SOLDER JOINT RELIABILITY QUALIFICATION

1. TEMPERATURE CYCLING: Testing performed per IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments. The results of this testing after following the above mentioned assembly conditions described here are shown in *Figure 3*, *Figure 4* and *Table 3*

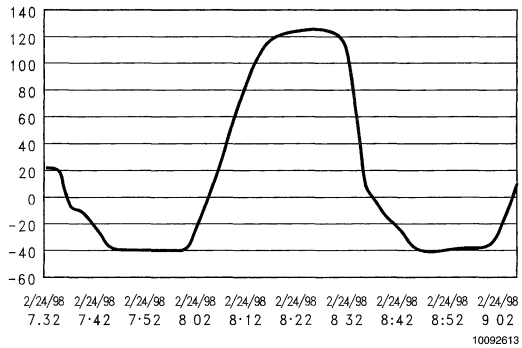

FIGURE 3. –40°C to 125°C, 1 cycle/hr Temperature Cycling Profile per IPC-SM-785

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Qualification (Continued)

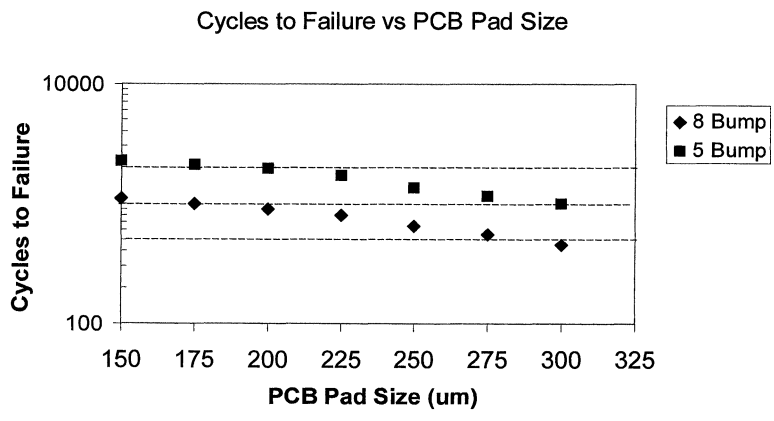

FIGURE 4. Impact of PCB Pad Size on Reliability for 0.17 mm Bump Package

TABLE 3. Temperature Cycling of Micro SMD Devices

Micro SMD Assembly	Stencil Type	Test Condition	0 cycles	284 cycles	764 cycles	1056 cycles	1152 cycles	
8 bump 0.17 mm bump diameter	0.100 mm thick 0.250 x 0.300 mm Oval aperture	–40 to 125° C, 1 cycle/hr, 25 min dwell, 5 min transfer	0/32	0/32	0/32	4/32	5/32	
8 bump 0.17 mm bump diameter	0.125 mm thick 0.300 x 0.300 mm Square aperture		0/32	0/32	0/32	0/32	0/32	
Micro SMD Assembly	**Stencil Type**	**Test Condition**	**0 cycles**	**300 cycles**	**600 cycles**	**624 cycles**	**924 cycles**	**1224 cycles**
18 Bump 0.3 mm bump diameter	0.125 mm thick 0.300 x 0.300 mm Square aperture	–40 to 125° C, 1 cycle/hr, 15 min dwell, 15 min ramp	0/102	0/102	0/102	0/102	0/102	0/102

2. PACKAGE SHEAR: As part of the manufacturing process, bump shear data is collected at package level to ensure attachment of solder ball to the package. The average package shear strength recorded was approximately 100 gm per solder joint for 0.17 mm diameter solder bump. For the 0.3 mm diameter solder bump, the package shear was greater than 200 gm per solder joint. Measured value of package shear may vary depending on materials and methods used in surface mount assembly.

3. PULL TEST: Assembled micro SMD 8 bump units were pulled vertically upward with a stud machined into the back of the component. Component was pulled till it was removed off the board. Average stud pull strength was recorded as 80 gm per solder joint for 0.17 mm diameter solder bump.

Qualification (Continued)

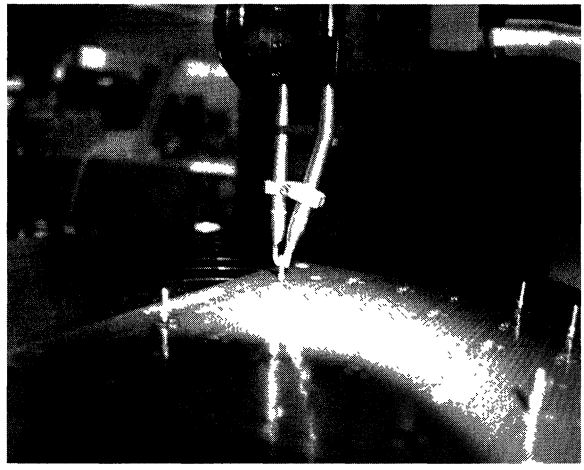

FIGURE 5. Pull Test Carried Out on the SMD 8 Bump (0.17 mm Diameter Bump)

4. DROP TEST: Drop test results are shown in *Table 4.* The tests were carried out on micro SMD 8 bump packages (0.17 mm diameter bump) mounted on 1.5 mm thick PCB. It included 7 drops on first edge, 7 on second edge, 8 drops on the corner and 8 drops on flat face, a total of 30 drops. An increase of 10% or more in daisy chain loop resistance was considered as a failure.

TABLE 4. Micro SMD Drop Test Results (0.17 mm Diameter Bump Package)

Test Results (Failures after 30 drops)				
Length		1m	1.5m	2m
Weight	75 gm	0/8	0/8	0/8
	150 gm	0/8	0/8	0/8

5. THREE-POINT BEND TEST: The three-point bend test used a test board with a 100 mm span. Deflection was applied at the center at 9.45 mm/min. No solder joint failure was observed even with deflections as high as 25 mm.

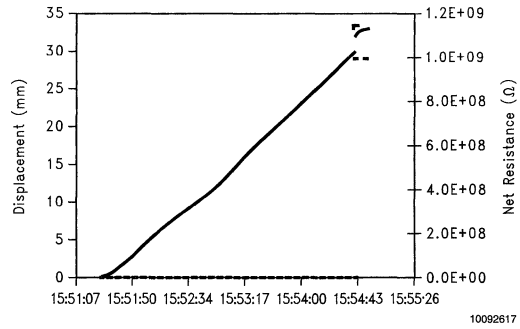

FIGURE 6. Board Deflection and Net Resistance (0.17 mm Diameter Bump Package)

Thermal Characterization

Thermal performance of micro SMD packages was assessed using low effective thermal conductivity test boards per EIA/JESD51-3. The performance of the SMD product depends on product die size and application (PCB layout and design), and the details of Theta JA values are available in product data sheets at http://www.national.com .

MICRO SMD Do's and Don'ts

SMALL BUMP		
	DO's	**DON'Ts**
PCB	150 µm < Pad Dia < 200 µm	Pad Dia < 150 µm or Pad Dia > 200 µm
	Prefer non-solder mask defined (NSMD) over solder mask defined (SMD). Solder mask opening ≤ 350 µm round.	Solder mask opening > 375 µm round.
	Organic Solderability Preservative (OSP) or Ni-Au surface finish (Less than 0.5 µm Au thickness).	Greater than 0.5 µm Au thickness for Ni-Au surface finish.
		HASL (Hot Air Solder Leveled) board finish.
Stencil	300 µm x 300 µm square aperture	Less than 275 x 275 µm square aperture
		Greater than 300 µm x 300 µm square aperture
	Laser cut + electro-polished or Additive build-up	Chemical etch
	100 µm < Thickness < 125 µm	Thickness > 125 µm or < 100 µm
Solder Paste	Type 3 (25 to 45 µm particle size range) or finer	Type 2 or Type 1

LARGE BUMP		
	DO's	**DON'Ts**
PCB	250 µm < Pad Dia < 275 µm	Pad Dia < 250 µm or Pad Dia > 275 µm
	Prefer non-solder mask defined (NSMD) over solder mask defined (SMD). Solder mask opening ≤ 375 µm round.	Solder mask opening > 375 µm round.
	Organic Solderability Preservative (OSP) or Ni-Au surface finish (Less than 0.5 µm Au thickness).	Greater than 0.5 µm Au thickness for Ni-Au surface finish.
		HASL (Hot Air Solder Leveled) board finish.
Stencil	250 µm x 250 µm square aperture	Less than 200 x 200 µm square aperture
		Greater than 275 µm x 275 µm square aperture
	Laser cut + electro-polished or Additive build-up	Chemical etch
	100 µm < Thickness < 125 µm	Thickness > 125 µm or Thickness < 100 µm
Solder Paste	Type 3 (25 to 45 µm particle size range) or finer	Type 2 or Type 1

Leadless Leadframe Package (LLP)

National Semiconductor
Application Note 1187
Charles Carinalli
Josip Huljev

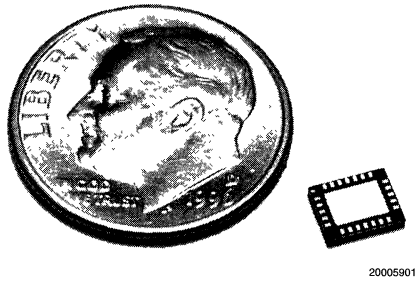

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FIGURE 1. 24 Pin LLP

Introduction

The Leadless Leadframe Package (LLP) is a leadframe based chip scale package (CSP) that may enhance chip speed, Reduces thermal impedance, and reduces the printed circuit board area required for mounting. The small size and very low profile make it ideal for high density PCBs used in small-scale electronic applications such as cellular phones, pagers, and handheld PDAs. The LLP has the following advantages:

- Low thermal resistance
- Reduced electrical parasitics
- Improved board space efficiency
- Reduced package height
- Reduced package mass

Package Overview

KEY ATTRIBUTES

- Construction of the LLP is Illustrated in *Table 1*, *Figure 2*, and *Figure 3*.
- Terminal contacts:
  - The contact pads are located peripherally in single row, dual rows or in array format depending on the specific number of pins and body size.
  - For certain specific applications the packages are incorporated with common power and/or ground pins as illustrated in *Figure 10*.
  - All LLP contacts are plated with 85Sn/15Pb solder for ease of surface mount processing.
- Printed Circuit Board (PCB) footprint:
  - National recommends a one-to-one correlation between the PCB land patterns and the package footprint.
  - Soldering the exposed die attach pad (DAP) to the PCB provides the following advantages:
    - Optimizes thermal performance.
    - Enhances solder joint reliability.
    - Facilitates package self alignment to the PCB during reflow.
- The LLP is offered in either dual-in-line (DIP) or quad configuration.
- Coplanarity is not an area of concern for this package.
  - All LLP contacts are flush with the bottom of the package.
- Moisture Sensitivity Level (MSL).
  - All LLP packages are MSL 1. Confirm MSL level via product application sheets.
  - MSL of specific applications, requiring large packages, may vary depending on die size and exposed DAP design.

TABLE 1. Elements of the 24, 44 and 56 pin LLP

	24 Pin	44 Pin	56 Pin
Package Dimensions	5 x 4 x 0.8 mm	7 x 7 x 0.8 mm	9 x 9 x 0.8 mm
PCB Footprint Area (mm^2)	20	49	81
Standard	JEDEC	JEDEC	JEDEC
Pitch	0.5 mm	0.5 mm	0.5 mm
Weight	0.047 grams	0.104 grams	0.208 grams
Lead Frame	Copper	Copper	Copper
Lead Finish	Sn/Pb	Sn/Pb	Sn/Pb
Typical Thermal Resistance θ_{JA} (Note 1)	33° C/W	20° C/W	27° C/W (Note 2)

Note 1: The typical data reported are measured values at still air and 1 watt input power using four layer FR4 substrate with Vias and copper thickness of 2 0/1 0/1 0/2 0 oz.

Note 2: Package option with limited exposed pad size due to incorporations of ground and power rings

Package Overview (Continued)

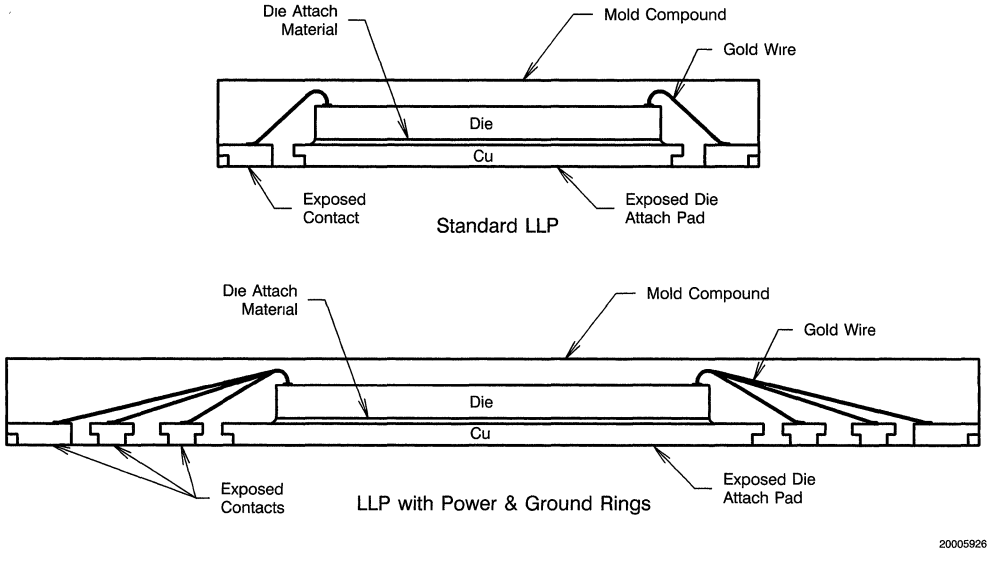


FIGURE 2. Construction of LLP

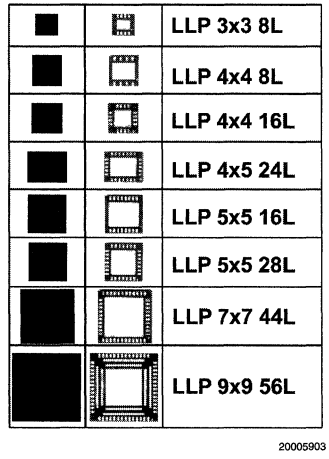


FIGURE 3. Examples

PACKAGE HANDLING

The LLP is shipped in standard polycarbonate conductive carrier tape with pressure sensitive adhesive (PSA) cover tape. The LLP is shipped in 7" reels. Samples can be shipped in carrier tape format. *Figure 4*, *Figure 5* and *Figure 6* show configurations of tape cavity design for LLP packages.

Package Overview (Continued)

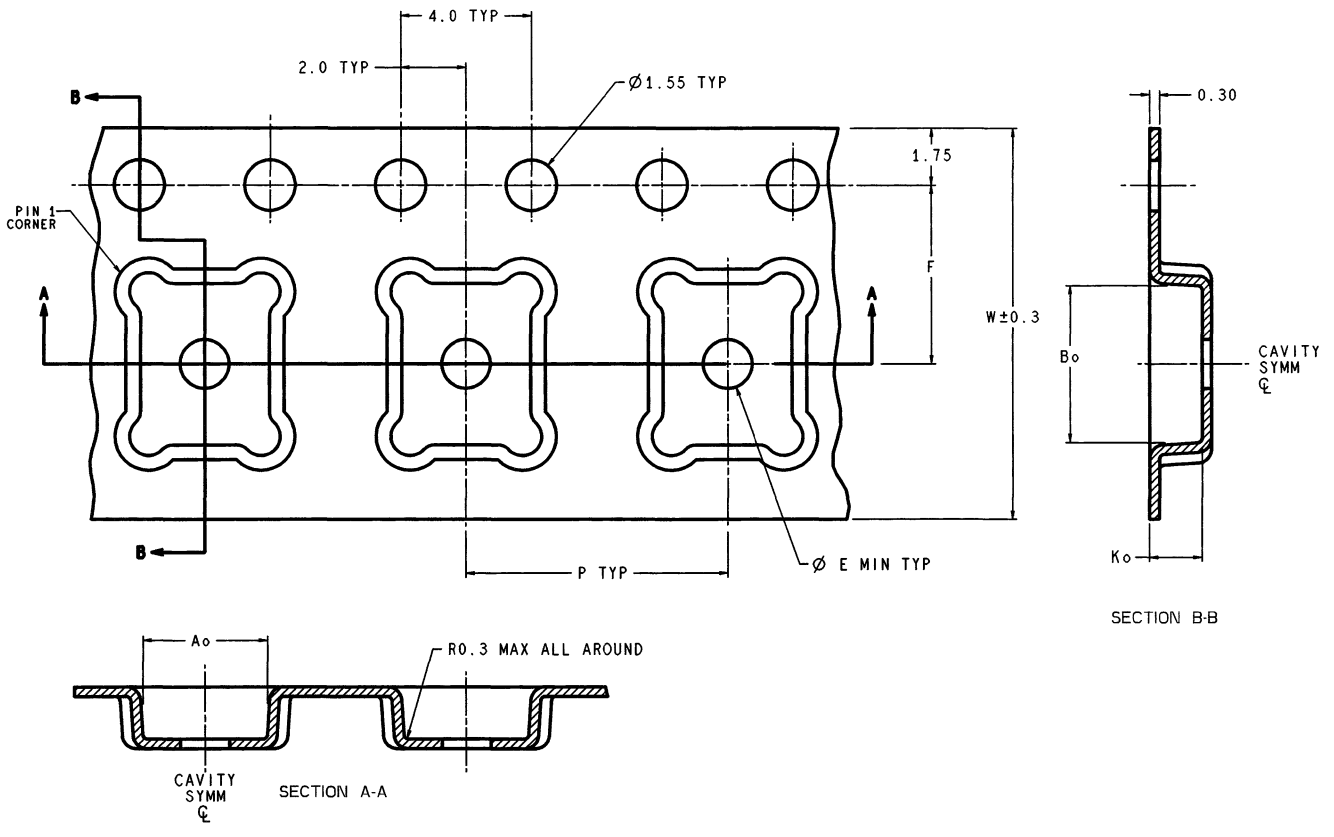


FIGURE 4. Tape and Reel Layout for Package Sizes < 4 x 4 mm. See *Table 2* for Dimensions.

Package Overview (Continued)

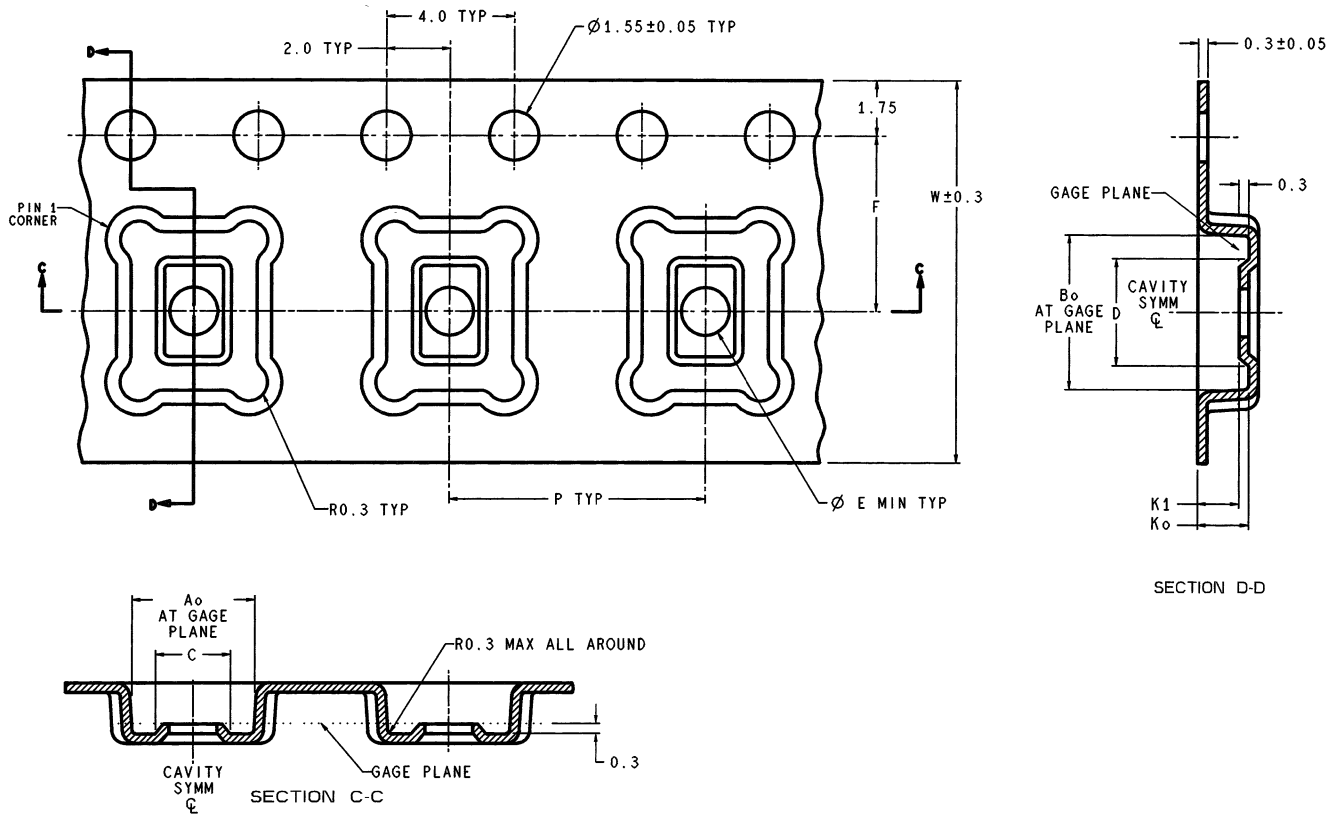


FIGURE 5. Tape and Reel for 4x4, 5x4, 5x5, 6x5 and 7x7 LLP. See *Table 2* for Dimensions.

Package Overview (Continued)

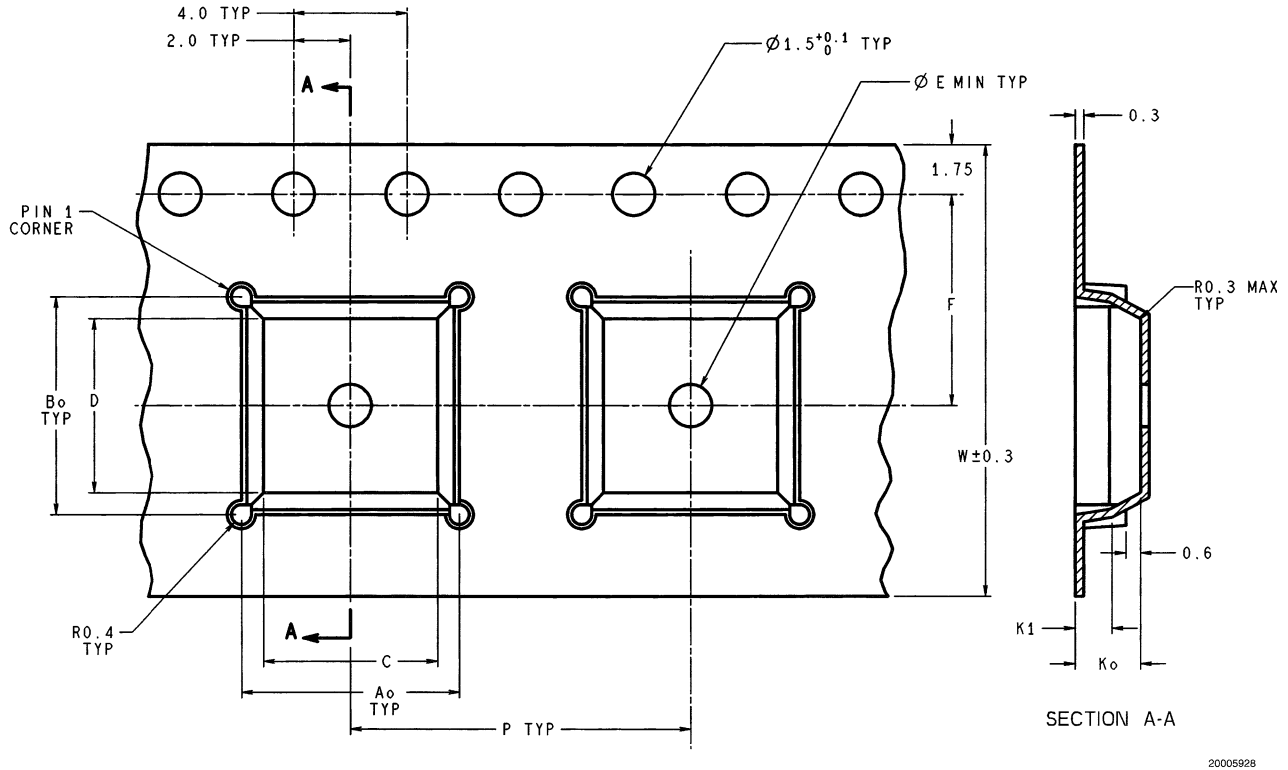


FIGURE 6. Tape and Reel for 9x9 LLP. See *Table 2* for Dimensions

Package Overview (Continued)

TABLE 2. Tape and Reel Dimensions

Package Size	Ao	Bo	C	D	E	F	P	W	Ko	K1
Dimensions for *Figure 4*										
2.5 x 2.5	2.8	2.8	N/A	N/A	1.0	5.5	8.0	12.0	1.0	N/A
2.5 x 3.0	3.3	2.8	N/A	N/A	1.0	5.5	8.0	12.0	1.0	N/A
2.92 x 3.29	3.6	3.2	N/A	N/A	1.5	5.5	8.0	12.0	1.0	N/A
3 x 3	3.3	3.3	N/A	N/A	1.5	5.5	8.0	12.0	1.0	N/A
3 x 4	4.3	3.3	N/A	N/A	1.5	5.5	8.0	12.0	1.0	N/A
Dimensions for *Figure 5*										
4 x 4	4.3	4.3	2.6	2.6	1.5	5.5	8.0	12.0	1.3	1.0
5 x 4	4.3	5.3	2.9	3.9	1.5	5.5	8.0	12.0	1.3	1.0
5 x 5	5.3	5.3	3.0	3.0	1.5	5.5	8.0	12.0	1.3	1.0
6 x 5	5.3	6.3	3.9	4.0	1.5	7.5	12.0	16.0	1.5	1.2
7 x 7	7.3	7.3	4.2	4.2	1.5	7.5	12.0	16.0	1.3	1.0
Dimensions for *Figure 6*										
9 x 9	9.25	9.25	7.35	7.35	N/A	7.5	12.0	16.0	2.3	1.3

MARKING LAYOUT

LLP Size	No of lines	Characters / line	Example	Comments
< 3 x 3 mm	1	3	XAB o	X = Single digit date code A = Product line ID B = Product ID o = pin 1 dot
3 x 3 mm up to 3 x 4 mm	2	4	ABCD o 123	AB = 2 digit data code CD = 2 digit die-run code o = pin 1 dot 123 = Device ID
4 x 4 mm and >	2	5	ABCDE 12345 o	A = Plant code BC = 2 digit date code DE = 2 digit die-run code 12345 = Device ID o = pin 1 dot

JEDEC REGISTRATIONS

- Quad LLP Packages: MO-220
- Dual-in-line LLP Packages: MO-229

PCB Design Recommendations

NSMD VS. SMD LAND PATTERN

Two types of land patterns are used for surface mount packages: (1) Non-Solder Mask Defined Pads (NSMD) and (2) Solder Mask Defined Pads (SMD). NSMD has an opening that is larger than the pad, whereas SMD pads have a solder mask opening that is smaller than the metal pad. *Figure 7* Illustrates the two different types of pad geometry.

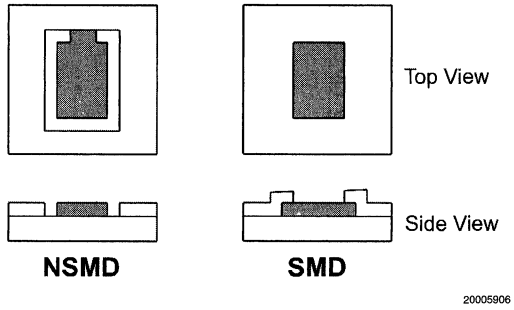


FIGURE 7. NSMD and SMD Pad Geometry

NSMD is preferred because the copper etch process has tighter control than the solder masking process. Moreover, the smaller size of the copper pad in the NSMD definition facilitates escape routing on the PCB when necessary.

NSMD pads require a ±0.075 mm (3 mils) clearance around the copper pad and solder mask this avoids overlap between the solder joint and solder mask and account for mask registration tolerances

SMD pad definition can introduce stress concentration points near the solder mask on the PCB side. Exrtreme environmental conditions such as large temperature variations may cause fatigue that leads to cracked solder joints and reliability problems.

For optimal reliability, National recommends a 1:1 ratio between the package pad and the PCB pad for the LLP. If probing of signal pad is required, it is recommended to design probe pads adjacent to signal pads as shown in *Figure 8*. The trace between the signal pad and the probe pad must be covered by solder mask such that the requirement of 1:1 ratio of package pad to PCB pad is not violated. See *Figure 9* for PCB pad recommendations.

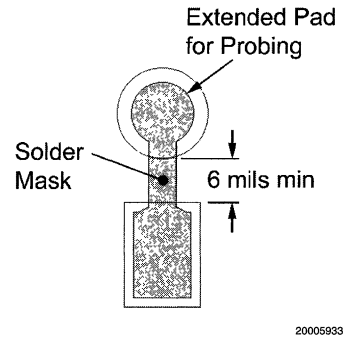
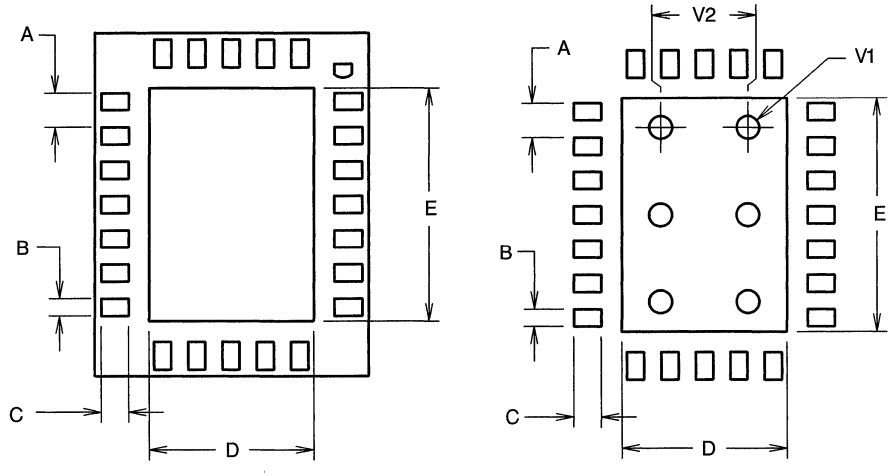


FIGURE 8. Recommended Pad Design for Probing

PCB Design Recommendations (Continued)



LLP Package Outline

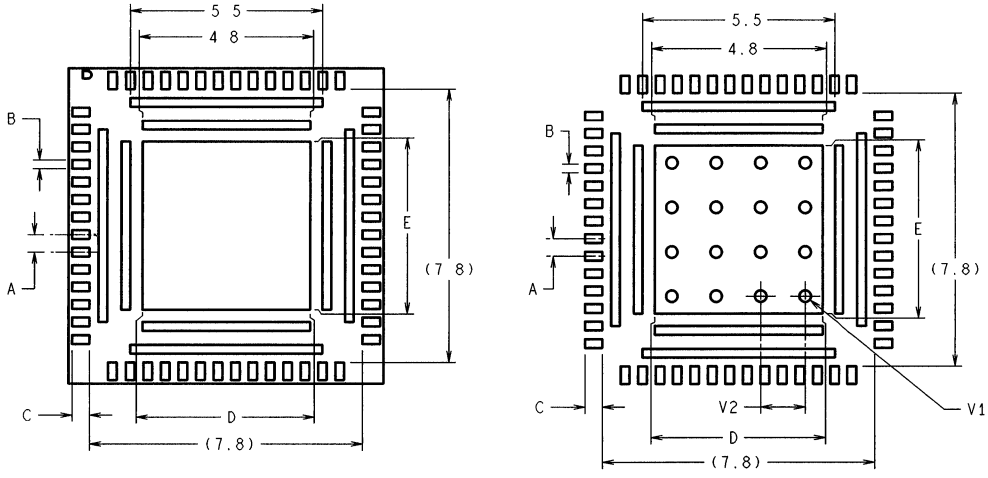
PCB Outline

20005907

Dimensions A, B, C, D, and E of PCB are 1:1 ratio with package pad dimensions. For specific detailed package dimensions refer to respective marketing outlines.
A - LLP Terminal Pitch
B - LLP Terminal Width
C - LLP Terminal Length
D - Exposed DAP Width
E - Exposed DAP Length
V1 - Thermal Via Diameter. Recommended 0.33 mm
V2 - Thermal Via Pitch. Recommended 1.27 mm

FIGURE 9. Typical Recommended Printed Circuit Board Dimensions

PCB Design Recommendations (Continued)



LLP Package Outline

PCB Outline

20005927

Number of pins	56
Package Size (mm)	9 x 9
A - LLP Terminal Pitch (mm)	0.5
B - LLP Terminal Width (mm)	0.25
C - LLP Terminal Length (mm)	0.5
D - Exposed DAP Width (mm)	4.8
E - Exposed DAP Length (mm)	4.8
V1 - Thermal Via Diameter (mm)	0.33
V2 - Thermal Via Pitch (mm)	1.27

FIGURE 10. Recommended Printed Circuit Board Dimensions for LLP 56 L with Power and Ground Rings.

THERMAL DESIGN CONSIDERATIONS

THERMAL LAND The LLP thermal land is a metal (normally copper) region centrally located under the package and on top of the PCB. It has a rectangular or square shape and should match the dimensions of the exposed pad on the bottom of the package (1:1 ratio).

For certain high power applications, the PCB land may be modified to a "dog bone" shape that enhances thermal performance. The packages used with the "dog bone" lands will be a dual inline configuration. (See *Figure 11*).

PCB Design Recommendations
(Continued)

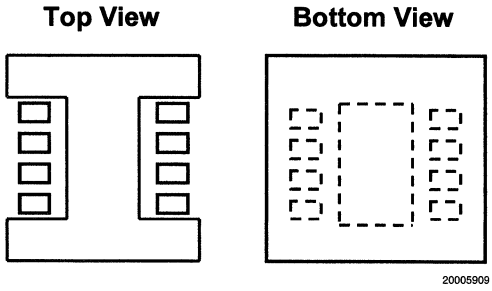


FIGURE 11. Dog Bone

THERMAL VIAS Thermal vias are necessary. They conduct heat from the surface of the PCB to the ground plane. The number of vias is application specific and is dependent upon electrical requirements and power dissipation. A package thermal performance may be improved by increasing the number of vias. The improvement diminishes, however, as the number of vias increase. See *Figure 12*.

A typical array of vias with a 1.27 mm pitch is shown in *Figure 9*. The via diameter should be 0.3 mm to 0.33 mm with 1oz. copper via barrel plating. It is important to plug the via to avoid any solder wicking inside the via during the soldering process. If the copper plating does not plug the via, the thermal vias can be tented with solder mask on the top surface of the PCB. The solder mask diameter should be at least 4 mils larger than the via diameter. The solder mask thickness should be the same accross the entire PCB.

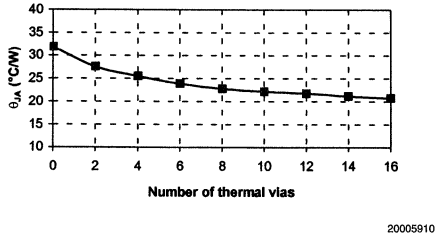


FIGURE 12. θ_{JA} vs. Number of Thermal Vias for the 44L LLP

EFFECTS OF THERMAL VOIDS A void in the solder paste or die attach (generated during the manufacturing process) could have a direct impact on heat dissipation. The effect is not significant unless the void volume exceeds a certain percentage of the corresponding material volume (see *Figure 13*). **NOTE:** voids typically do not have an impact on reliability.

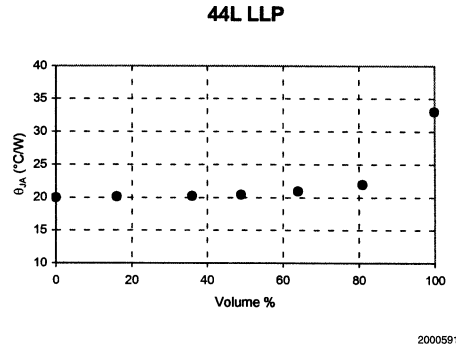


FIGURE 13. Thermal Voids Impact for the 44L LLP

THERMAL LAYERS IN THE PCB Because of the small size and low profile, the majority of heat generated by the die within the LLP is dissipated through the exposed pad to PCB. Consequently, the PCB configuration and metal layers embedded in the PCB become important to achieving good thermal performance. In a 4-layer PCB (2 layers for signals and 2 layers for power/ ground), the area of the embedded copper layer connecting to the thermal vias has significant effect on the thermal performance of the package. *Figure 14* shows simulation data of θ_{JA} vs. the embedded copper layer area for the 44L LLP. Increasing the copper layer area reduces the thermal resistance. However, in a manner similar to what occurs as the number of vias increases, the amount of thermal resistance improvement diminishes as the embedded copper area increases.

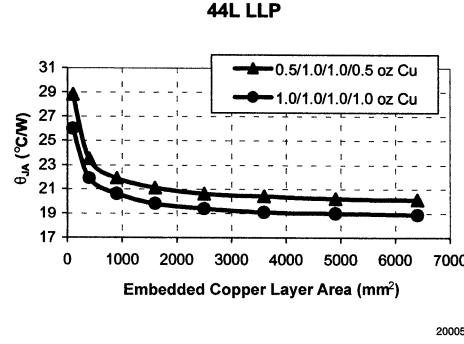


FIGURE 14. Effect of Thermal Layers on the 44L LLP's Junction-to-Ambient Thermal Resistance

SMT Assembly Recommendations

The LLP surface mount assembly operations include:

- PCB plating requirements
- Screen printing the solder paste on the PCB
- Monitor the solder paste volume (uniformity)
- Package placement using standard SMT placement equipment
- X-ray pre reflow check - paste bridging
- Reflow and cleaning (dependent upon the flux type)
- X-ray post reflow check - solder bridging & Voids

PCB PLATING REQUIREMENTS

A uniform PCB plating thickness is key for high assembly yield.

- For an electroless, nickel-immersion, gold finish, the gold thickness should range from 0.05 µm to 0.127 µm to avoid solder joint embrittlement.
- Using a PCB with **O**rganic **S**olderability **P**reservative coating (OSP) finish is also recommended, as an alternative to Ni-Au.

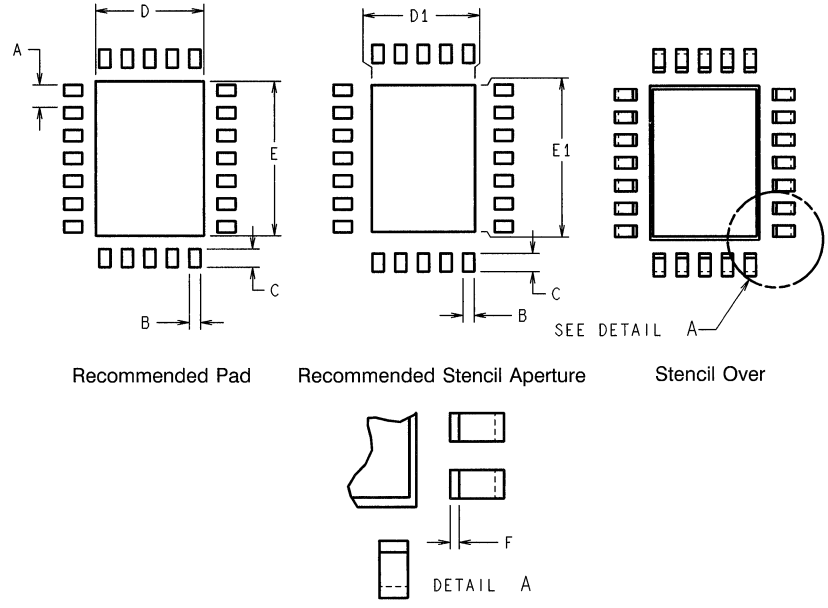
SOLDER STENCIL

Solder paste deposition using a stencil-printing process involves the transfer of the solder paste through pre-defined apertures with the application of pressure. Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the LLP package is highly recommended to improve board assembly yields.

Stencils fabricated from Nickel-plated electro polished chem-etch or Laser cut is recommended. Tapered aperture walls (5° tapering) is recommended to facilitate paste release. Recommended stencil thickness is 127 µm. In order to prevent solder bridging the stencil aperture openings need to be modified as follows:

- The terminal contact aperture openings should be offset by 0.1 mm from the pads.
- For exposed pad aperture, up to 5 mm, the opening should be reduced to 95% of the corresponding PCB exposed DAP dimensions. See *Figure 15* and *Figure 16.*
- For exposed pad aperture with any side greater than 5 mm, the stencil opening should be split in two for any side > 5 mm. See *Figure 18.*
- For packages with exposed Power and Ground Rings, the stencil opening for the exposed pad aperture of any size should be split into an array of opening with minimal spacing between each openings.
- The aperture opening for the power and ground pads is 1:1 with pads but with splits into several openings. See *Figure 19.*
- Stencil openings for SOT23 5/6L footprint compatible LLP:
  - — For the SOT23 5/6L footprint compatible LLP for which the PCB has been designed for the SOT23 package, refer to *Figure 17* for solder stencil openings.
  - — For new board design, it is recommended to use *Figure 16* for PCB pad and stencil openings.

SMT Assembly Recommendations (Continued)

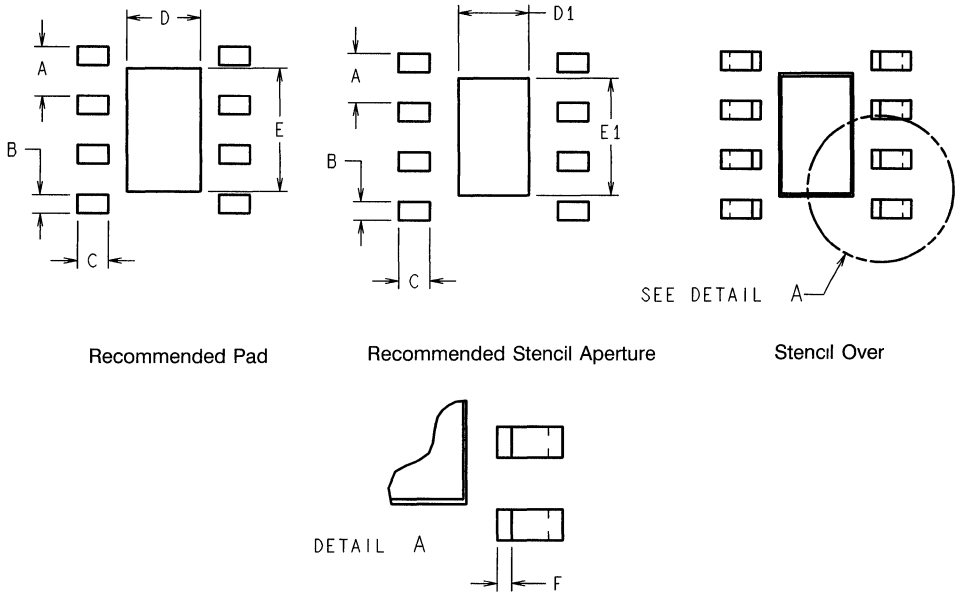


A, B and C of Stencil	1:1 ratio with A, B and C of PCB pad
D1	0.95 x D
E1	0.95 x E
F	0.1 mm
Note: For specific detailed package dimensions refer to respective Marketing Outlines.	

Note 3: Dimensions shown are for a specific case - LLP 24 package only

FIGURE 15. Typical Recommended PCB Dimensions vs. Stencil Aperture for Quad Packages.

SMT Assembly Recommendations (Continued)



Recommended Pad | Recommended Stencil Aperture | Stencil Over

20005914

A, B and C of Stencil	1:1 ratio with A, B and C of PCB pad
D1	0.95 x D
E1	0.95 x E
F	0.1 mm
Note: For specific detailed package dimensions refer to respective Marketing Outlines.	

FIGURE 16. Typical Recommended PCB Dimensions vs. Stencil Aperture for Dual In-line Packages.

SMT Assembly Recommendations (Continued)

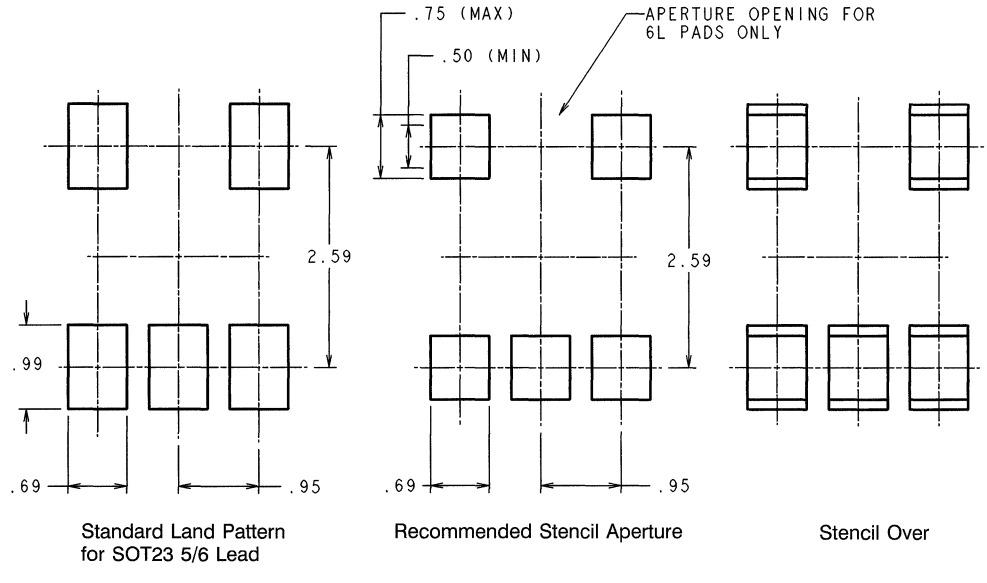
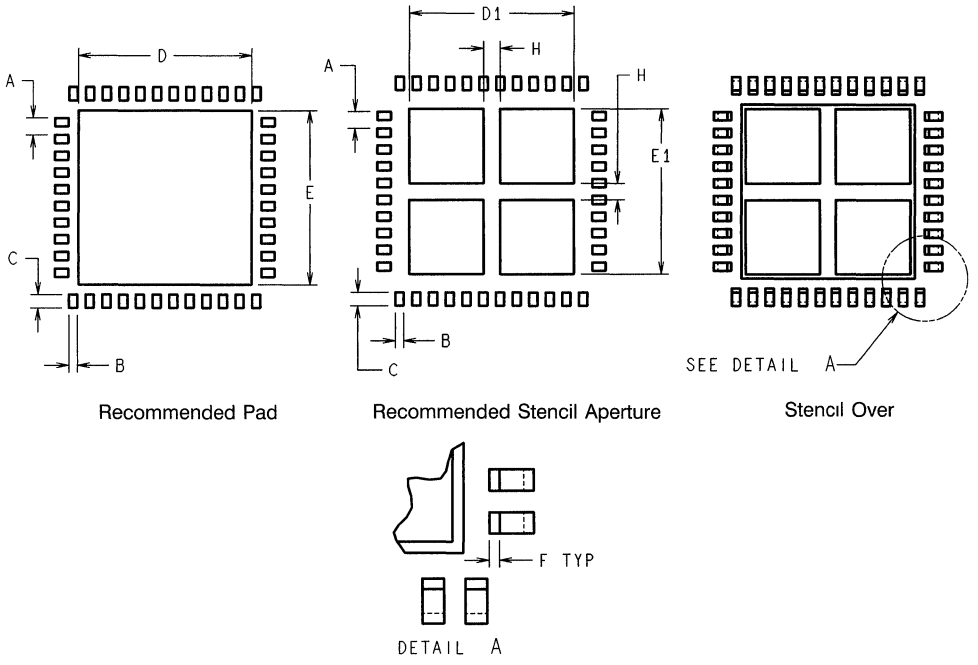


FIGURE 17. Recommended Stencil Aperture for SOT23 5/6 Lead Footprint Compatible LLP

Note:

1. For stencil thickness of 0.15 mm and above a 0.50 mm (min) aperture length is recommended. For stencil thickness of 0.13 mm and below a 0.75 mm (max) aperture length is recommended.
2. For new board designs, it is recomeneded to use *Figure 16* for pad and stencil openings.

SMT Assembly Recommendations (Continued)



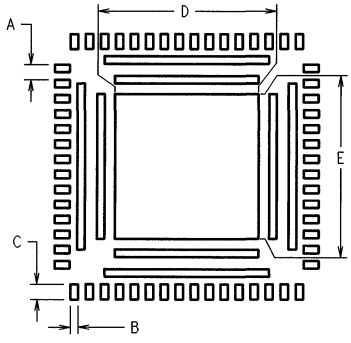
Recommended Pad | Recommended Stencil Aperture | Stencil Over

Number of pins	44
A - LLP, PCB, Stencil Terminal Pitch (mm)	0.5
B - LLP, PCB, Stencil Terminal Width (mm)	0.25
C - LLP, PCB, Stencil Terminal Length (mm)	0.5
D - LLP, PCB Exposed DAP Width (mm)	5.2
D1 - Exposed DAP Aperture Width (mm) D1 = .95 D	4.94
H - Aperture split width, centered (mm)	0.5
E - LLP, PCB Exposed DAP Length (mm)	5.2
E1 - Exposed DAP Aperture Length (mm) E1 = .95 E	4.94
F - Stencil Aperture opening offset (mm)	0.1

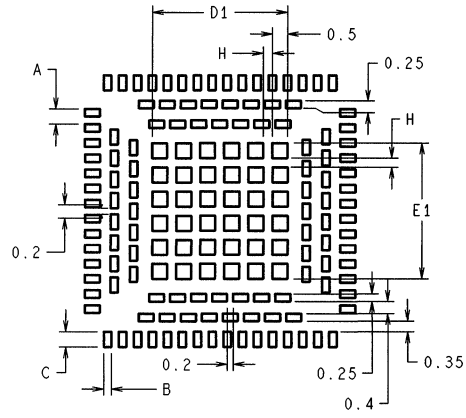
FIGURE 18. Typical Recommended Stencil Opening for Exposed DAP > 5 mm on any side.

Note: For DAP options with exposed DAP ≤ 5 mm, use similar stencil opening as recommended in *Figure 15*.

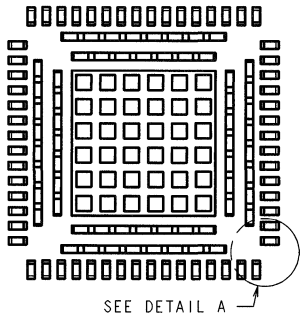
SMT Assembly Recommendations (Continued)



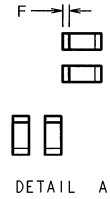
Recommended Pad



Recommended Stencil Aperture



Stencil Over



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Number of pins	56
A - LLP, PCB, Stencil Terminal Pitch (mm)	0.5
B - LLP, PCB, Stencil Terminal Width (mm)	0.25
C - LLP, PCB, Stencil Terminal Length (mm)	0.5
D - LLP, PCB Exposed DAP Width (mm)	4.8
D1 - Exposed DAP Aperture Width (mm)	4.5
H - Aperture split width, centered (mm)	0.3
E - LLP, PCB Exposed DAP Length (mm)	4.8
E1 - Exposed DAP Aperture Length (mm)	4.5
F - Stencil Aperture opening offset (mm)	0.1

FIGURE 19. Typical Recommended Stencil Opening for LLP with Exposed DAP, Power and Ground Rings

PACKAGE PLACEMENT

LLP packages can be placed using standard pick and place equipment with an accuracy of ±0.05 mm. Component pick and place systems are composed of a vision system that recognizes and positions the component and a mechanical system which physically performs the pick and place operation. Two commonly used types of vision systems are: (1) a vision system that locates a package silhouette and (2) a vision system that locates individual bumps on the interconnect pattern. The latter type renders more accurate place but tends to be more expensive and time consuming. Both methods are acceptable since the parts align due to a self-centering feature of the LLP solder joint during solder reflow.

It is recommended to release the LLP package 1 to 2 mils into the solder paste.

SMT Assembly Recommendations

(Continued)

SOLDER PASTE

Type 3 or Type 4 solder paste is acceptable.

REFLOW AND CLEANING

The LLP may be assembled using standard IR / IR convection SMT reflow processes without any special considerations. As with other packages, the thermal profile for specific board locations must be determined. Nitrogen purge is recommended during solder for no-clean fluxes. The LLP is qualified for up to three reflow cycles at 235°C peak (J-STD-020). The actual temperature of the LLP is a function of:

- Component density
- Component location on the board
- Size of surrounding components

It is recommended that the temperature profile be checked at various locations on the board. *Figure 20* illustrates a typical reflow profile.

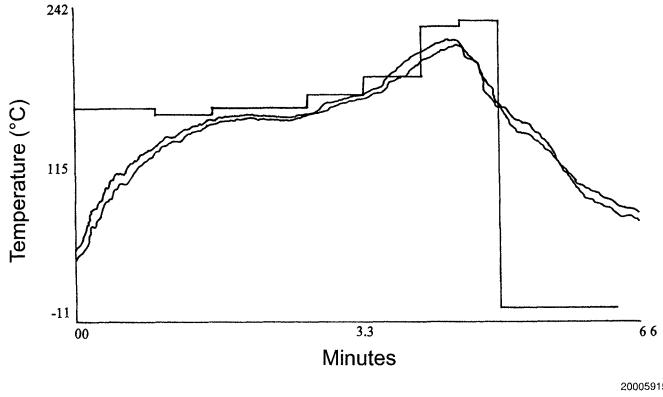

FIGURE 20. Typical Reflow Profile

SOLDER JOINT INSPECTION

After surface mount assembly, transmission X-ray should be used for **sample** monitoring of the solder attachment process. This identifies defects such as solder bridging, shorts, opens and voids. **NOTE:** voids typically do not have an impact on reliability. *Figure 21* shows a typical X-ray photograph after assembly.

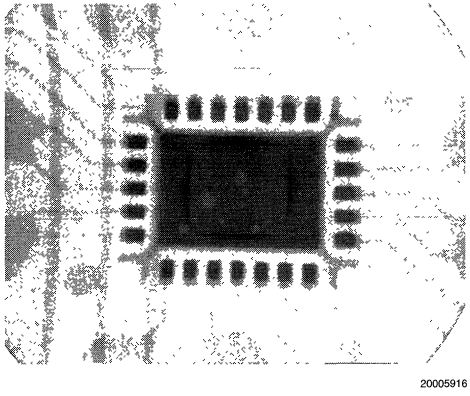

FIGURE 21. Typical X-ray after process

In the process setup, it is recommended to use side view inspection in addition to X-ray to determine if there are 'Hour Glass' shaped solder existing. The 'Hour Glass' solder shape is is not a reliable joint. 90° mirror projection can be used for side view inspection.

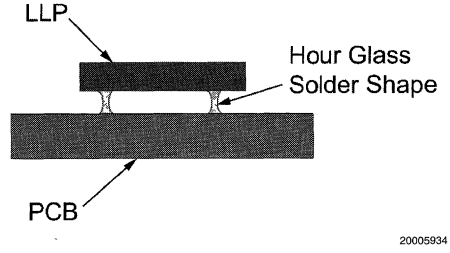

FIGURE 22.

REPLACEMENT/ REWORK

The quality of the rework is controlled by:

- Directing the thermal energy through the component body to solder without over-heating the adjacent components.
- Heating should occur in an encapsulated, inert, gas-purged environment where the temperature gradients do not exceed ±5°C across the heating zone.
- Using a convective bottom side pre-heater to maximize temperature uniformity.

SMT Assembly Recommendations

(Continued)

- Interchangeable nozzles designed with different geometries will accommodate different applications to direct the airflow path

NOTE: Standard SMT rework systems are capable of these elements.

Removal of the LLP Removing the LLP from the PCB involves heating the solder joints above the liquidus temperature of eutectic (63Sn-37Pb) solder using a vacuum gas nozzle. Baking the PCB at 125˚C for 4 hours is recommended PRIOR to any rework. Doing this removes any residual moisture from the system, preventing moisture induced cracking or PCB delamination during the demount process.

A 1.27 mm (50 mil) keep-out zone for adjacent components is recommended for standard rework processing. If the adjacent components are closer than 1.27 mm, custom tools are required for the removal and rework of the package.

It is recommended that the reflow profile used to reflow the LLP be as close to the PCB mount profile as possible. Preheat the PCB area, through the bottom side of the board, to 100˚C before heating the LLP to ensure a controlled process. Once the liquidus temperature is reached, nozzle vacuum is automatically activated and the component is removed. After removing the package, the pads may be heated with the nozzle to reflow any residual solder, which may be removed using a Teflon tipped vacuum wand.

Site Preparation Once the LLP is removed, the site must be cleaned in preparation for package attachment. The best results are achieved with a low-temperature, blade-style conductive tool matching the footprint area of the LLP in conjunction with a de-soldering braid. No-clean flux is needed throughout the entire rework process. Care must be taken to avoid burn, lift-off, or damage of the PCB attachment area. See *Figure 23*.

Solder Paste Deposition Because the LLP is a land area type package, solder paste is required to insure proper solder joint formation after rework. A 127 µm (5 mil) thick mini-stencil is recommended to deposit the solder paste patterns prior to replacement of the LLP. See *Figure 24*.

Component Placement Most CSP rework stations will have a pick and place feature for accurate placement and alignment. Manual pick and place, with only eye-ball alignment, is not recommended. It is difficult or impossible to achieve consistent placement accuracy.

Component Reflow It is recommended that the reflow profile used to reflow the LLP be as close to the PCB mount profile as possible. Preheat the PCB area, through the bottom side of the board, to 100˚C before heating the LLP to ensure a controlled process. Once the liquidus temperature is reached, the solder will reflow and the LLP will self align. *Figure 25* shows a cross section of a solder joint after rework.

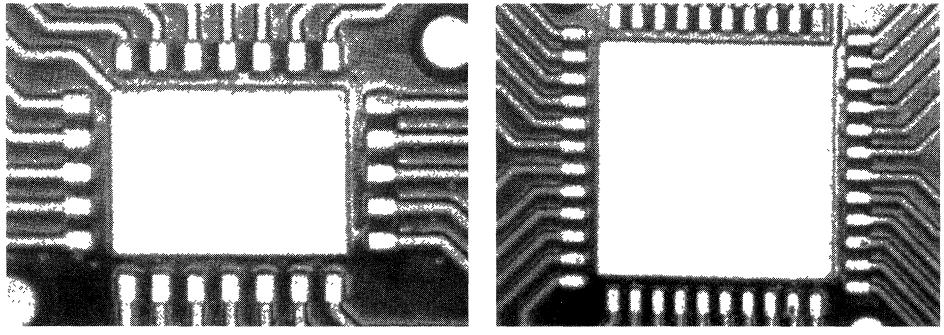

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FIGURE 23. Pads After Removing Components and Cleaning

SMT Assembly Recommendations (Continued)

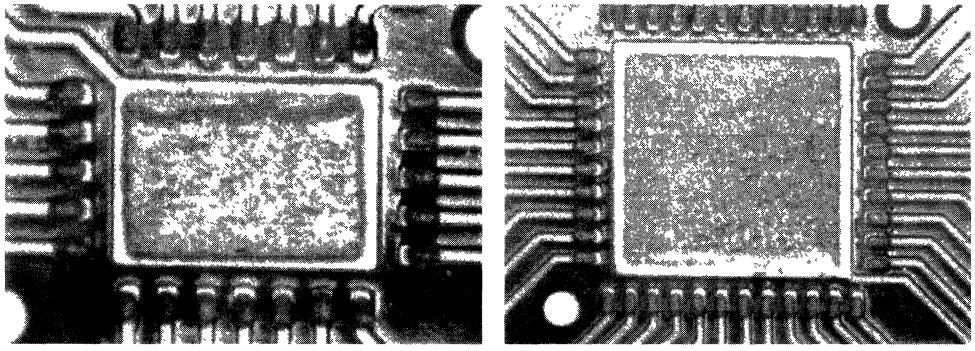

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FIGURE 24. Solder Paste Printing of LLP 24 and LLP 44 Using 127 µm (5 mil) Thick Stencil

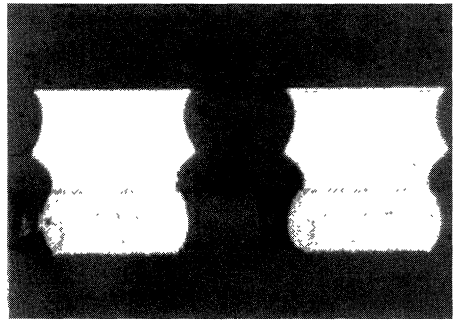

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FIGURE 25. X-section Across Solder Joints

Appendices

APPENDIX 1: REFLOW RECOMMENDATIONS

		Convection / IR
Ramp Up °C/sec (Note 6)	Maximum	4°C/sec
	Recommended	**2°C/sec** (Note 4)
	Minimum	(Note 5)
Dwell Time ≥ 183°C (Note 6)	Maximum	85 seconds
	Recommended	**75 seconds** (Note 4)
	Minimum	(Note 5)
Peak Temperature (Note 6)	Maximum	240°C
	Recommended	**215°C**
	Minimum	(Note 5)
Dwell Time Max. (within 5°C of peak temperature)	Maximum	10 seconds
	Recommended	**5 seconds**
	Minimum	1 second
Ramp Down °C/sec (Note 6)	Maximum	4°C/sec
	Recommended	**2°C/sec**
	Minimum	(Note 5)

Note 4: Will vary depending on board density, geometry, and package types May vary depending on solder paste manufactures recommendations.

Note 5: Will vary depending on package types, and board density

Note 6: All Temperatures are measured at the PCB surface

APPENDIX 2: BOARD LEVEL RELIABILITY TEST DATA

Temperature Cycle Test

Test Conditions:

- Temperature Range: −40 to 125°C
- Cycle Duration: 1 hour (15 minute ramp/15 minute Dwell)
- Test Board Dimension: 142.5 mm x 142.5 mm x 1.6 mm
- Test Board Finish: Ni-Au 0.05 µm to 0.127 µm thickness
- Dummy die in package
- Package is bonded with a Daisy Chain Circuit

Failure Determination: Change of 10% in Net Resistance

Results:

24L 4 mm x 5 mm LLP Package (Package Die Attach Pad soldered to the PCB)

Timepoint	Lot A	Lot B	Lot C
0 Cycles	0/41	0/84	0/83
500 Cycles	0/41	0/84	0/83
1050 Cycles	0/41		

24L 4 mm x 5 mm LLP Package (Package Die Attach Pad NOT soldered to the PCB)

Timepoint	Lot A	Lot B	Lot C
0 Cycles	0/81	0/78	0/76
500 Cycles	0/81	0/78	0/76
950 Cycles	0/81	0/78	0/76
1050 Cycles	0/81	0/78	0/76

44L 7 mm x 7 mm LLP Package (Package Die Attach Pad soldered to the PCB)

Timepoint	Lot A	Lot B	Lot C
0 Cycles	0/33	0/69	0/88
500 Cycles	0/33	0/69	0/88
1050 Cycles	0/33	0/69	0/88

44L 7 mm x 7 mm LLP Package (Package Die Attach Pad NOT soldered to the PCB)

Timepoint	Lot A	Lot B	Lot C
0 Cycles	0/81	0/78	0/76
500 Cycles	0/81	0/78	0/76
950 Cycles	0/81	0/78	0/76
1050 Cycles	0/81	0/78	0/76

56L 9 mm x 9 mm Package (With Power and Ground Rings) (Package Die Attach Pad soldered, Power and Ground Ring not soldered to the PCB)

Timepoint	Results
0 Cycles	0/75
500 Cycles	0/75
1050 Cycles	0/75

SOT23 5/6L Footprint Compatible LLP

Timepoint	DAP soldered to PCB	DAP not soldered to PCB
0 cycles	0/126	0/84
500 cycles	0/126	0/84
1050 cycles	0/126	0/84

14 Lead Power LLP

Timepoint	Results
0 Cycles	0/80
500 Cycles	0/80
1050 Cycles	0/80

Appendices (Continued)

Board Drop Test

Test Conditions:

- Test Board Dimension: 142.5 mm x 142.5 mm x 1.6 mm
- Printed Circuit Board Finish: Ni-Au 2 - 5 micro inches thickness
- Dummy die in package
- Package is bonded with a Daisy Chain Circuit
- Cumulative Dead weight of the board: 150 Grams
- Drop Height: 1.5 meters
- Drop Surface: Non cushioning vinyl tile
- Number of Drops: 30 total
  - — 7 drops: along the length of the PCB
  - — 7 drops: along the width of the PCB
  - — 8 Drops: Along the diagonal of the board
  - — 8 Drops: With the components on the top of the board

Failure Determination: Change of 10% in Net Resistance

Results:

Package Type	Drop Test Results
24L 4 mm x 5 mm LLP (DAP soldered to PCB)	0/20
24L 4 mm x 5 mm LLP (DAP NOT soldered to PCB)	0/20
44L 7 mm x 7 mm LLP (DAP soldered to PCB)	0/20
44L 7 mm x 7 mm LLP (DAP NOT soldered to PCB)	0/20
56L 9 mm x 9 mm LLP (DAP soldered, Power/Ground Rings soldered to PCB)	0/25
14L Power LLP	0/32

3 Point Bend Test

Test Conditions:

- Test Board Dimension: 142.5 mm x 142.5 mm x 1.6 mm
- Printed Circuit Board Finish: Ni-Au 0.05 µm to 0.127 µm thickness
- Dummy die in package
- Package is bonded with a Daisy Chain Circuit
- Bend Span: 100 mm
- Bend Speed: 3.81 mm/min
- Die attach pad soldered to PCB

Package Type	Bend Test Results
24L 4 mm x 5 mm LLP	0/10
44L 7 mm x 7 mm LLP	0/15
56L 9 mm x 9 mm LLP	0/25
14L 6 mm x 5 mm Power LLP	0/8

Vibration Test

Test Conditions:

- Test Board Dimension: 142.5 mm x 142.5 mm x 1.6 mm
- Printed Circuit Board Finish: Ni-Au 0.05 µm to 0.127 µm thickness
- Dummy die in package
- Package is bonded with a Daisy Chain Circuit
- Die attach pad soldered to PCB
- Vibration test conditions:
  - — Sinusoidal excitation performed for 1 hour at 20G force followed by 3 hours at 40G force
  - — Random Vibration with variable frequencies ranging from 20Hz to 2,000Hz for 3 hours with a force of 2G RMS

Results: DAP Soldered to PCB

Package Type	Test Results
24L 4 mm x 5 mm LLP	0/24
44L 7 mm x 7 mm LLP	0/20
56L 9 mm x 9 mm LLP	0/25
14L 6 mm x 5 mm Power LLP	0/32

APPENDIX 3: THERMAL SIMULATION DATA FOR POWER LLP

Thermal Simulation Conditions

All dimensions are in millimeters	
Die Size	4.09 x 2.67 x 0.216
DAP Size	4.35 x 3.00
Package Size	6.00 x 5.00 x 1.00
Thermal Vias	0, 2, 4, 8, 12. See *Figure 26.*
Board Size	101.6 x 76.2 x 1.6 (4 layer JEDEC)
Copper Thickness	2.0/1.0/1.0/2.0 oz. (1 oz. = 36 µm)
Copper Coverage	Top layer: traces (27.5 x 0.25) plus metalization area as shown in *Figure 27.* Middle layers: 60.0 x 60.0 Bottom layer: 15% of the board area.

Appendices (Continued)

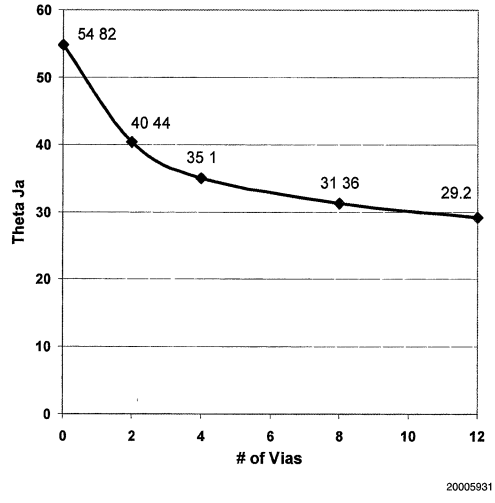


FIGURE 26. θ_{JA} as a Function of Number of Vias Placed in PCB

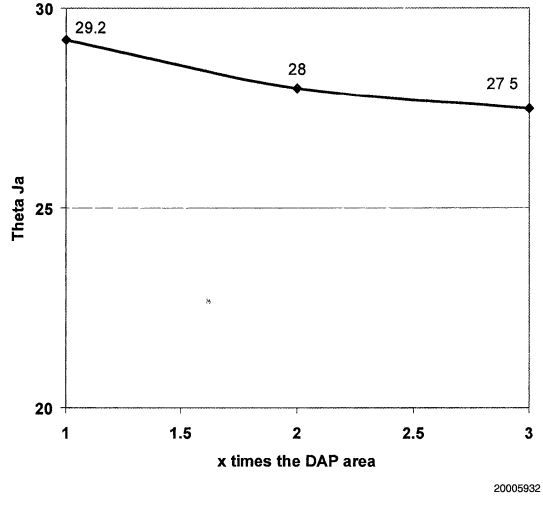


FIGURE 27. θ_{JA} as a Function of Top Metalization Area

8-Lead LLP Thermal Performance and Design Guidelines

National Semiconductor
Application Note 1201
Chester Simpson

Introduction

The new leadless leadframe package (LLP) provides significantly increased power dissipation capability in a tiny surface-mount package. The key feature of the LLP is that it has a center metal area located directly below the die which allows a direct path for heat to flow out, providing very low thermal resistance. When this pad is connected to PC board copper to provide heatsinking, values of total thermal resistance (junction-to-ambient) below 40°C/W can be obtained in still air environments.

Modelling Assumptions

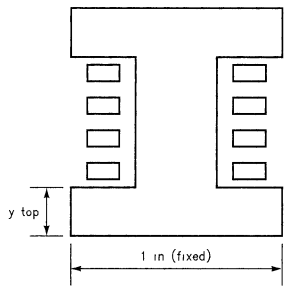
The data listed in this application note is derived from finite element modelling in which the following assumptions are used:

1. DAP (die attach paddle) size = 3.0 mm x 2.2 mm
2. Die size = 2.11 mm x 1.63 mm
3. Package size = 4.0 mm x 4.0 mm x 0.75 mm
4. Power Dissipation = 1W
5. Thermal Vias (0.3 mm diameter) = 8

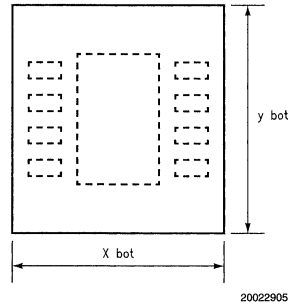
Copper Patterns

Data is provided for PCB designs using copper patterns which are "dog-bone" shaped on the top layer and a square pattern directly beneath the part on the bottom layer (see below). In the bottom layer pattern, the X and Y dimensions are equal.

PCB Top Copper Pattern



PCB Bottom Copper Pattern



Performance Data

Curves are provided showing the thermal resistance (junction-to-ambient) values obtained for various size copper patterns using top layer only, bottom layer only, and top + bottom layer for PC boards with 0.5 oz., 1 oz., and 2 oz. copper weights (all data is for still air):

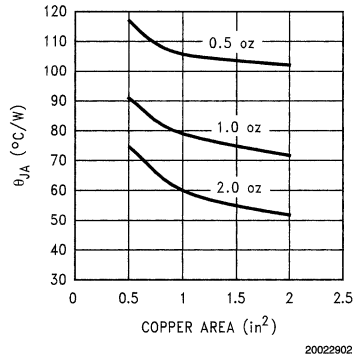


FIGURE 1. Thermal Data for Top Layer only

Performance Data (Continued)

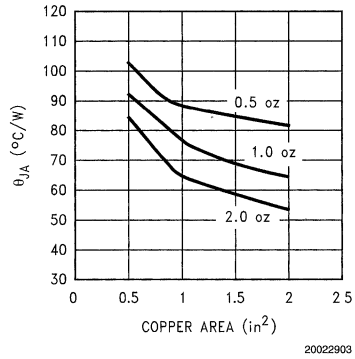


FIGURE 2. Thermal Data for Bottom Layer only

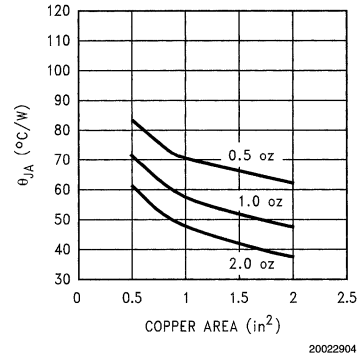


FIGURE 3. Thermal Data for Top and Bottom Layers

Conclusions

It was shown that the still-air thermal resistance value (junction-to-ambient) for the 8-lead LLP will vary from a maximum of 115°C/W down to about 37°C/W by increasing the available PCB copper from about 0.5 sq. in. (0.5 oz., top layer only) to about 2 sq. in. (2 oz., top and bottom layers used). This gives the designer the information needed to design a PC board which can provide a thermal resistance value within that range.

Electrical Performance of Packages

National Semiconductor
Application Note 1205
Chester Simpson

Introduction

This note is a snapshot of electrical performance of National's IC packages. It is provided to help designers get an idea about electrical parasitics associated with the package, and help them compare the electrical performance of different packages The electrical performance of a package is usually expressed in terms of resistance (R), inductance (L), and capacitance (C). Example R-L-C data is provided for National's package types.

RESISTANCE

Resistance is the cause of IR drops in the package. DC resistance is the resistance of a conductor when the entire cross section of the conductor is carrying current. At higher frequencies, the current is concentrated along the surface of the conductor, due to skin effect. AC resistance increases with frequency, because as the frequency increases, skin depth decreases, and the available cross section for the current flow decreases. AC resistance varies linearly with length of the conductor, but not with respect to cross sectional area.

INDUCTANCE

Inductance (L) is defined as the relationship between the following for a closed current path:

- flux linkage (λ) and current flow (i): $\lambda = L \times i$ or
- time varying voltage (v) and current (i): $v = L \times di/dt$

On an IC package, signals propagate in and out through the signal leads and return through the power leads. The closed current path (or loop) is thus formed by signal leads together with power or ground leads. It is also possible to calculate inductance for an open circuit path, or a section of a closed loop (e.g., just a single lead). This is called **partial inductance**. Using this concept, the inductance contributions of different elements in the loop (and their interactions) can be separated into different inductance elements. This allows the designer to determine return paths and noise by simulation. It is possible to determine the total loop inductance of an IO signal (returning through the power lead) or a differential pair using partial self and mutual inductance. (See *Figure 1*).

DC and AC Inductance: DC Inductance is calculated assuming that the current flows through the entire cross section of the conductor. AC inductance is calculated assuming that the skin depth is small compared to the cross section of the conductor, and current flows only on the surface of the conductors. Both DC and AC Inductance can be provided for packages. To determine which inductance is appropriate for your application, please see the section "Frequency limitations of R-L-C parameters".

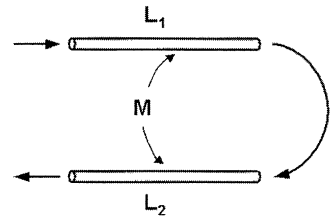


FIGURE 1. Inductance of a Signal Loop

CAPACITANCE

Self capacitance is the capacitance of any element to "ground" In package electrical models, the plane on the PC board is assumed to be an ideal ground Thus, self capacitance of any package element is the capacitance of that element to the board plane. Mutual capacitance is the capacitance between any two elements. For example, in a lumped model of ball grid array package, capacitance from a package trace to the package VSS plane is mutual capacitance.

FREQUENCY LIMITATIONS OF R-L-C PARAMETERS

As long as the conductor lengths are small compared to the maximum sinusoidal frequency of the signal, the lumped R-L-C approximation of the element is appropriate. For digital ICs, a lumped model is appropriate for a maximum lead length of 60 x t_r (t_r is rise time in nanoseconds and length is in millimeters). When using lumped elements, it is important to know which parameters (DC or AC) should be used. *Table 1* gives this information.

Transmission line models or distributed models should be used for high frequencies. To determine if your product requires this analysis, contact your local National Semiconductor technical representative

TABLE 1. Frequency limitations of RLC parameters

Parameter	Valid Frequency Range	
DC Resistance	Leadframe packages: DC to 500 kHz	Substrate packages: DC to 5 MHz
AC Resistance	Leadframe packages: 500 kHz to any freq.	Substrate packages: 5 MHz to any freq.
DC Inductance	Leadframe packages: DC to 10 MHz	Substrate packages: DC to 100 MHz
AC Inductance	Leadframe packages: 10 MHz to any frequency provided lumped model is adequate.	
	Substrate packages: 10 MHz to any frequency provided lumped model is adequate.	
Capacitance	From DC to any frequency, as long as dielectric loss can be neglected.	

Circuit Model of a Package Lead

National Semiconductor defines package models in terms of their T-equivalent circuits. Each lead has two terminals - a "source" and a "sink" - representing its two ends. In a T-equivalent circuit, the lead inductance and resistance are divided in two parts, and placed on either sides of the lead capacitance. *Figure 2* shows a T-equivalent model of three leads. The leads are labeled "Lead 1", "Lead 2" and "Return". Signal current flows in or out of "Lead 1" and return current flows on the "Return" lead. Mutual inductance between signal and return lead significantly affects the performance of the signal loop. Therefore, mutual inductance of all leads to the ground lead must be included in detailed simulations. Similarly for calculating package cross-talk, mutual inductance between two signal leads should be taken into account. Package circuit models can be provided in SPICE format. For package SPICE models contact your local National Semiconductor technical representative.

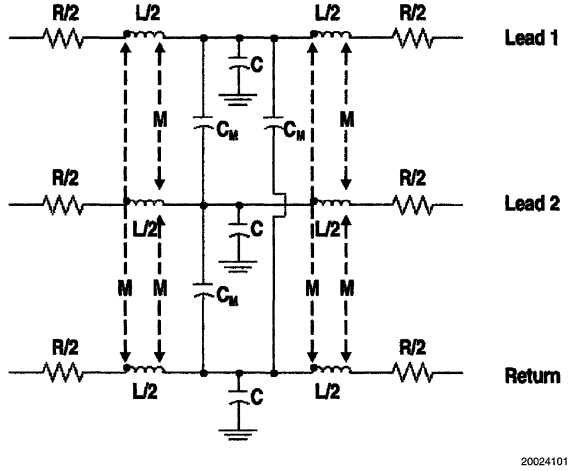


FIGURE 2. Equivalent of three package leads

Example R-L-C Values for Packages

This section provides RLC values for National's packages. The following is true for the data presented in this note:

1. Example R-L-C data is provided for typical leads only. For detailed analysis, accurate package models should be obtained.
2. The PC board plane is assumed 20 mils (0.5 mm) below the seating plane of the package.
3. Wirebond parasitics are not included in this section; they are separately provided in *Table 7*.
4. Inductance given is partial AC inductance; it does not scale linearly with length.
5. Resistance provided is AC resistance calculated at 1GHz.
6. Mutual inductance to the immediate (M12) and the next-of-immediate (M13) leads is provided. It should be noted that in packages with no power planes, significant mutual coupling exists beyond these. For example for a PQFP, the coupling coefficient (k) between two leads that are separated by 10 leads can be as high as 0.3.

TABLE 2. Example RLC values for lead-frame based packages and micro SMD

Package	Body Size (mm)	Lead Count	R (ohm)		L (nH)		M (nH)				C (pF)		C_{M12} (pF)	
			Corner	Center	Corner	Center	Corner		Center		Corner	Center	Corner	Center
							M12	M13	M12	M13				
QFP	28 x 28	208	0.90	0.65	12.00	8.00	8.00	6.50	5.50	4.50	0.20	0.06	1.00	0.60
	20 x 14	128	1.2	0.8	4.50	2.40	2.80	2.20	1.40	1.10	0.10	0.05	0.45	0.20
	12 x 12	80	0.36	0.28	2.90	2.40	2.30	1.60	1.30	0.90	0.15	0.10	0.27	0.20
LLP	all sizes	all	0.001	0.001	0.008	0.008	0.001	0.001	0.001	0.001	0.03	0.03	0.03	0.03
Mini SOIC	5 x 3	8	0.015	0.015	0.45	0.45	0.15	0.08	0.15	0.08	0.05	0.05	0.04	0.04
SC-70	2 x 1.25	5	0.015	-	0.45	-	0.08	0.05	-	-	0.06	-	0.06	-
PLCC	11.43 x 11.43	28	0.05	0.04	4.4	3.2	2	1.5	1.5	1.1	0.35	0.25	0.6	0.45
SSOP	5.3 x 10.2	28	0.3	0.25	2.9	1.3	1.45	0.85	0.6	0.35	0.2	0.08	0.27	0.1
MDIP	19 x 6.35	14	0.15	0.05	7.0	3.0	2.5	1.8	1.0	0.7	0.65	0.25	1.1	0.4

Example R-L-C Values for Packages (Continued)

TABLE 2. Example RLC values for lead-frame based packages and micro SMD (Continued)

Package	Body Size (mm)	Lead Count	R (ohm)		L (nH)		M (nH)				C (pF)		C_{M12} (pF)	
			Corner	Center	Corner	Center	Corner		Center		Corner	Center	Corner	Center
							M12	M13	M12	M13				
Micro SMD (small bump) (Note 1)	all sizes	all	0.003	-	0.011	-	0.002	-	-	-	0.012	-	0.005	-
Micro SMD (large bump) (Note 1)	all sizes	all	0.002	-	0.013	-	0.002	-	-	-	0.016	-	0.012	-

Note 1: Micro SMD package does not have wirebonds

LAMINATE BASED CSP (CHIP-SCALE PACKAGE)

There are two types of laminate based CSPs: single row and dual row. Because the lead-geometry of all single row CSPs is the same, the RLC parasitics are the same. However, for the dual row CSPs, there are three types of lead geometries (labeled as #1, #2 and #3 in *Table 3*), and the parasitics are different for different geometries. To determine which dual row design is being used for your product, please contact your local National Semiconductor technical representative. *Figure 3* shows a picture of a typical single and dual row CSP. Table 3 gives typical RLC characteristics of CSPs. Mutual inductance terms in the columns in *Table 3* are illustrated in *Figure 3*. M12 is the mutual inductance between two neighboring leads in the same (inner or outer) row. M_{RR} is the mutual inductance between the neighboring leads of different rows. For more details on the construction of CSP packages, browse to http://www.national.com/packaging.

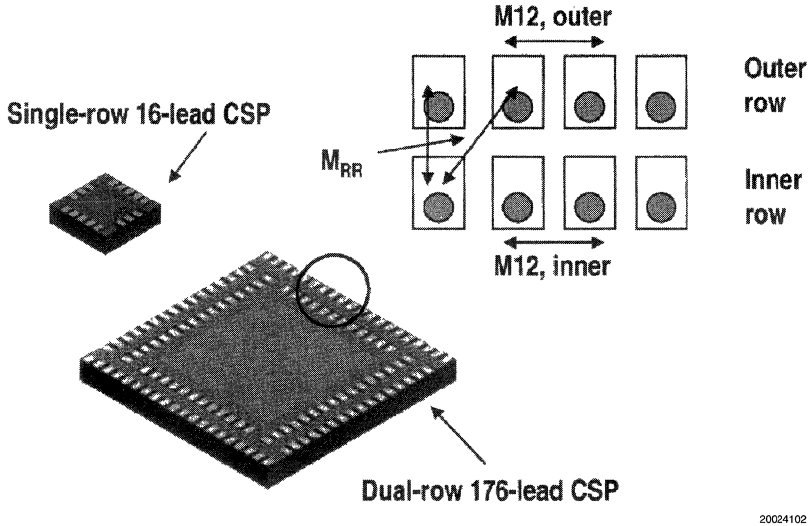


FIGURE 3. Laminate CSP packages (not to scale)

TABLE 3. Example RLC data for CSP packages

Package	Lead Count	R (ohm)		L (nH)		M (nH)			C (pF)		C_M (pF)
		Outer	Inner	Outer	Inner	M12		MRR	Outer	Inner	
						Outer	Inner				
Dual row, #1	128 /176	0.03	0.03	0.40	0.40	0.10	0.10	0.08	0.08	0.08	0.07

8

Example R-L-C Values for Packages (Continued)

TABLE 3. Example RLC data for CSP packages (Continued)

Package	Lead Count	R (ohm)		L (nH)		M (nH)			C (pF)		C_M (pF)
		Outer	Inner	Outer	Inner	M12		MRR	Outer	Inner	
						Outer	Inner				
Dual row/ inline bond pads #2	128 /176	0.04	0.03	0.60	0.40	0.09	0.06	0.06	0.10	0.08	0.07
Dual row/ inline bond pads #3	128 /176	0.03	0.08	0.40	1.00	0.06	0.27	0.12	0.08	0.10	0.07
Single row	all	0.03		0.40		0.10			0.08		0.07

BGA PACKAGES

A typical BGA (ball grid array) package is shown in *Figure 4*. Each side of the package has four rows of solder-balls. The traces going to the solder balls in the corners of the package are significantly longer, therefore the data is grouped by "corner" and "center" leads. In *Table 4*, "O" column gives data for the outermost row of solder-balls on the package (as illustrated in *Figure 4*); similarly, "I" column gives data for the innermost row of solder balls on the package. LBGAs and FBGAs (low-profile BGAs and fine-pitch BGAs, respectively) are often custom routed, and it is therefore difficult to provide generalized R-L-C data. Data for an LBGA and an FBGA is provided for reference.

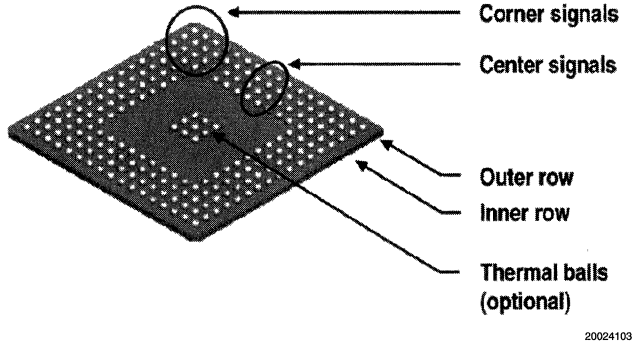


FIGURE 4. Ball Grid Array packages

TABLE 4. Example RLC Characteristics of BGAs (without planes)

Package	Body Size (mm)	R (ohm)				L (nH)				M (nH)				C (pF)				C_M (pF)			
		Corner		Center		Corner		Center		Corner		Center		Corner		Center		Corner		Center	
		O	I	O	I	O	I	O	I	O	I	O	I	O	I	O	I	O	I	O	I
PBGA-208	23 x 23	1.20	0.80	0.90	0.60	9.00	6.00	5.50	2.50	6.00	4.50	3.50	1.50	0.20	0.10	0.15	0.10	0.35	0.15	0.15	0.10
PBGA-388	35 x 35	1.80	1.20	1.35	1.00	14.00	10.00	8.00	4.50	9.00	6.50	5.00	3.00	0.30	0.15	0.25	0.18	0.50	0.25	0.25	0.15
LBGA-196	15 x 15	0.4		0.2	0.3	1.70		0.90	1.20	0.60		0.30	0.45	0.08		0.04	0.04	0.10		0.10	0.10
FBGA-81	9 x 9	0.025 - 0.075				0.4 - 1.5				0.03 - 0.1				0.04 - 0.06				0.03 - 0.075			

Modeling packages which have planes for power and ground is more complex. Signals propagate through the signal leads and return over the power and ground planes. The high-speed return signal tends to concentrate on the area of the plane closest to the propagating signal. This means that the current density on the plane is non-uniform, and

Example R-L-C Values for Packages (Continued)

non-constant with time. It is therefore not possible to give a ***single*** inductance number for a power or a ground plane in a package. However, inductance for the ***return path*** of a particular signal lead on a plane can be calculated. *Table 5* and *Table 6* give the example RLC values for EBGA packages. Plane inductance values in the L_{PLANE} column of *Table 5* give inductance in the return path (VDDIO and/or VSSIO) of a typical signal that returns over the power plane. Similarly, the plane capacitance values pertain only to that section of the plane.

TABLE 5. AC Inductance - EBGA packages

Package	Lead Count	L		M		M (trace to planes)						L_{PLANE}
		Corner	Center	Corner	Center	Corner (Note 2)			Center (Note 2)			
						1	2	3	1	2	3	
EBGA	215	5.0 - 7.8	2.5 - 4.0	2.9 - 3.8	1.4 - 2.0	2.8 - 4.0	2.2 - 3.2	2.0 - 2.8	2.0 - 2.5	1.4 - 2.2	1.2 - 1.5	4.0
	368	7.5 - 10.5	6.5 - 8.0	2.5 - 4.0	2.5 - 3.5	3.1 - 4.0	2.5 - 3.0	2.5 - 2.8	1.8 - 3.0	1.5 - 2.0	1.1 - 1.5	4.0

Note 2: Mutual inductance to all the 3 planes is given, 1 is nearest to traces 3 is farthest

TABLE 6. Resistance and Capacitance - EBGA packages

Package	Body Size (mm)	Lead Count	R		C	C_M	$C_{M-PLANE}$	C_{PLANE}	
			Corner	Center				Self (Note 3)	Mutual (Note 4)
EBGA	27 x 27	215	0.75 - 0.90	0.60 - 0.80	0.08 - 0.12	0.10 - 0.14	1.10 - 1.50	0.6 - 1.2	5.0 - 8.0
	40 x 40	368	1.00 - 1.30	0.7 - 1.0	0.30 - 0.50	0.10 - 0.20	1.20 - 1.80	1.5 - 2.0	14.51 - 50

Note 3: Self capacitance of the plane closest to the board ground plane Self capacitance to planes other than this plane is zero

Note 4: Mutual capacitance between adjacent planes This capacitance, if between power planes, will provide help in decoupling

Wirebonds

To obtain package parasitics with wirebonds, add the inductances and resistances for the appropriate wire lengths to the package parasitics provided in the previous sections. Following table gives wirebond inductance for different wire lengths. AC resistance of wirebonds (at 1 GHz) is 0.1–Ω/mm (= 0.0025–Ω/mil). Capacitance of wirebonds is negligible, and is therefore omitted from this note. For CSPs and LLPs, use the L and M values in the "Wire Inductance" column of the table. It has been observed that there is a significant amount of coupling between wirebonds and leads/traces of a package (exceptions: CSPs and LLPs, due to their short trace/lead lengths). The column "Effective Inductance" in *Table 7* gives L and M values corrected for this mutual coupling. Use the L and M values in this column for all packages other than CSPs and LLPs. Because of space limitations, mutual inductance is provided only for two neighboring wires. Significant mutual coupling exists beyond these, and it should be taken into account in detailed analysis.

TABLE 7. Wirebond inductance

Length		Wire Inductance (For CSPs and LLPs)			Effective Inductance (For all other packages)		
(mm)	(mils)	L (nH)	M12 (nH)	M13 (nH)	L (nH)	M12 (nH)	M13 (nH)
0.50	19.60	0.32	0.14	0.09	0.45	0.19	0.12
1.00	39.20	0.78	0.39	0.28	1.09	0.55	0.39
2.00	78.40	1.83	1.04	0.78	2.57	1.46	1.12
3.00	117.60	2.99	1.80	1.40	4.19	2.52	1.96
4.00	156.80	4.22	2.62	2.09	5.91	3.67	2.93
5.00	196.00	5.50	3.48	2.82	7.70	4.87	3.95

Section 9

Power Management: Device Information

Section 9 Contents

High-Efficiency Regulator has Low Drop-Out Voltage

National Semiconductor
Application Brief 11

Conventional regulators have a high drop-out voltage that is a function of the total output current. However, with just a regulator chip, an external transistor and a few passive components, this design forms a high output current regulator with a limited input voltage and high efficiency. The circuit presented has a drop-out of 0.7V at 5A load current and 1.3V at a current level of as high as 10A.

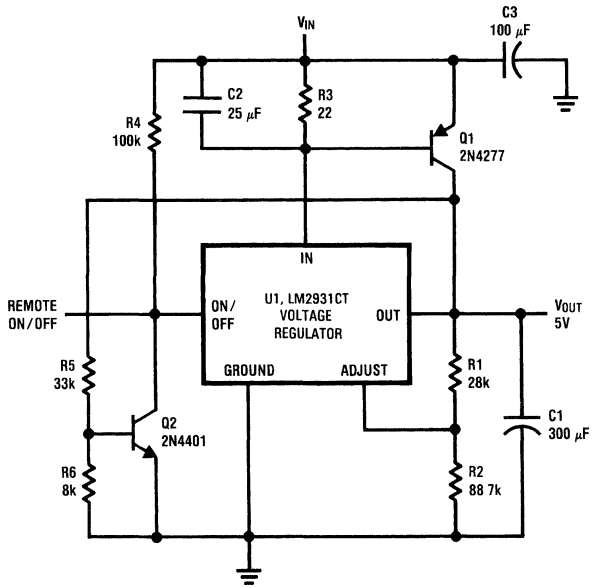
The circuit output voltage equals that of PNP regulator U1 and may be expressed as $V_{OUT} = V_{REF}$ (R1 + R2)/R1 where V_{REF} equals U1's reference voltage of 1.2V. To compensate for bias-current errors and to keep the extra quiescent current that is induced by this resistor network to a few μA, resistor R1 is set at 28 kΩ. Thus for a 5V regulated output voltage, R2 is set at 88.7 kΩ. In addition, the output voltage can be adjusted between 3V and 24V by varying R2.

The circuit can handle a great deal of current because of external PNP transistor Q1. At high current levels, the circuit's drop-out voltage is a function of the saturation voltage of the PNP device. As a result, Q1 must have low saturation levels for V_{CE} and V_{BE} along with a high beta. In addition, the maximum output current is equal to the maximum output sink of regulator U1 multiplied by the maximum beta of Q1. A germanium transistor, such as a 2N4277 for the external pass element, satisfies the above requirements. For the components shown, the circuit gives excellent regulation at V_{IN} = 5.7V up to 5A in load current, giving a drop-out of only 0.7V.

U1 is biased to a minimum of 30 mA by a resistor R3, which also functions as a bleeding resistor for Q1. The on-off pin of U1 permits extra remote on-off control and current-limiting functions for the circuit. Pulling this pin to ground enables the circuit, whereas keeping it open disables the circuit and leaves the regulator in the standby mode. The ratio R5:R6 limits the maximum output current. When the load current exceeds this maximum, the output voltage begins to fall and the voltage across R6 decreases. This low voltage cuts off transistor Q2, thereby disabling the circuit output. As a result, transistor Q1 and the load are protected from overdrive and damage.

Efficiency

Using National Semiconductor's regulator LM2931CT, external transistors Q1 and Q2, and a few passive components, this circuit forms a high-current regulator having a low drop-out. For the components shown in the figure, the regulator has a drop-out of 0.7V at 5A load current and 1.3V at a level as high as 10A. The on-off pin of regulator U1 provides remote control, while transistor Q2 limits the maximum output current.



00552301

Wide Adjustable Range PNP Voltage Regulator

National Semiconductor
Application Brief 12

What happens when the need arises for a regulator voltage that isn't matched by your stock of fixed voltage I/C regulators? For the standard NPN pass transistor regulators (LM340 for example) the answer may be as simple as adding a resistor (R1) in the ground pin (*Figure 1*). The new output voltage (V_O) will then be:

$$V_O = V_{REG} + I_Q \times R1 \quad (1)$$

where: V_{REG} is the original regulator output voltage,

I_Q is the regulator's quiescent current.

But if the need is also for a low drop across the regulator, then a PNP pass regulator is required. Simply adding a resistor in the ground pin doesn't work, since the regulator internal current varies too much because of increased base drive to compensate for lower PNP beta. However, if a zener is used instead of a resistor, the higher voltages can be accommodated *(Figure 2)*. The new output voltage (V_O) is:

$$V_O = V_{REG} + V_Z \quad (2)$$

where V_Z is the zener voltage.

As V_{REG} is constant, the output voltage regulation will depend largely on the zener voltage (V_Z) and its dynamic impedance.

The zener voltage will vary slightly with the current flowing through. Let's take the popular LM2931Z PNP regulator from National Semiconductor as an example of variation of the quiescent current. When the regulator load changes from 50 mA to 150 mA, the zener current will increase by 12.5 mA. The zener voltage variation due to this current change will only be a few hundred mV. That is, the output voltage will vary slightly, but not as much (as high as a few volts) as with a resistor to ground. Thus, a much better regulated output voltage is maintained.

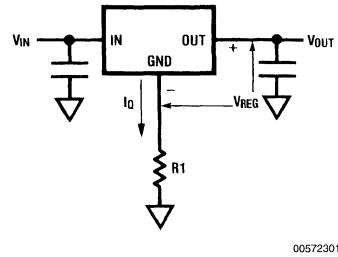


FIGURE 1. NPN Regulator

One advantage inherent to this circuit is the ability to achieve higher output voltages than the normal regulator rating The maximum regulator output is limited by the breakdown of its internal circuitry. However, carefully selecting the zener to keep the input and ground pin differential voltage well below the breakdown, the input is allowed to exceed its maximum rating. For example, a 5V 3-terminal LM2931Z PNP regulator (maximum operating input voltage = 26V) can become a 56V regulator with a 51V zener. And the input voltage can be as low as 56 6V with a load current of 150 mA or less. Most of the PNP regulator's features are still maintained. The short circuit protection may or may not be there, depending on the output voltage and the safe operating area of the output pass PNP transistor.

Capacitors C1 and C2 should have the same values as those specified for normal operation. However, their maximum operating voltage ratings should exceed the input voltage. Capacitor C3 should be located as close as possible to the ground pin to get good decoupling and ensure stable operation. The value of C3 will depend on zener impedance and noise characteristics. The capacitor types must also be rated over the desired operating temperature range.

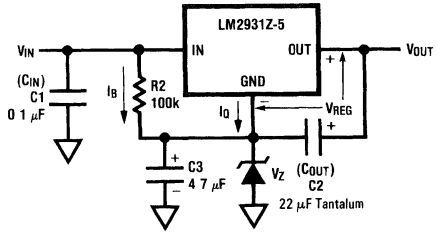


FIGURE 2. PNP Regulator

LM340 Series Three Terminal Positive Regulators

National Semiconductor
Application Note 103
George Cleveland

Introduction

The LM340-XX are three terminal 1.0A positive voltage regulators, with preset output voltages of 5.0V or 15V. The LM340 regulators are complete 3-terminal regulators requiring no external components for normal operation. However, by adding a few parts, one may improve the transient response, provide for a variable output voltage, or increase the output current. Included on the chip are all of the functional blocks required of a high stability voltage regulator; these appear in *Figure 1*.

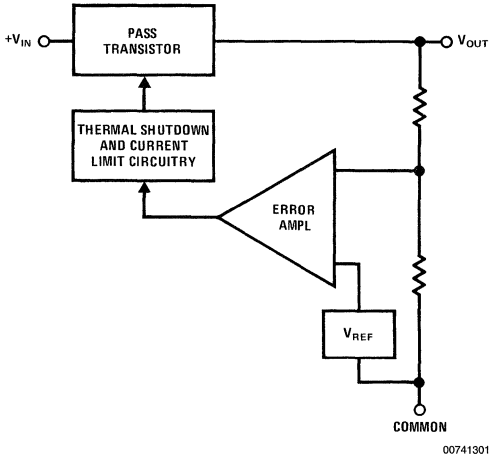


FIGURE 1. Functional Block of the LM340

The error amplifier is internally compensated; the voltage reference is especially designed for low noise and high predictability; and, as the pass element is included, the regulator contains fixed current limiting and thermal protection. The LM340 is available in either metal can TO-3 or plastic TO-220 package.

1.0 Circuit Design

VOLTAGE REFERENCE

Usually IC voltage regulators use temperature-compensated zeners as references. Such zeners exhibit BV > 6.0V which sets the minimum supply voltage somewhat above 6.0V. Additionally they tend to be noisy, thus a large bypass capacitor is required.

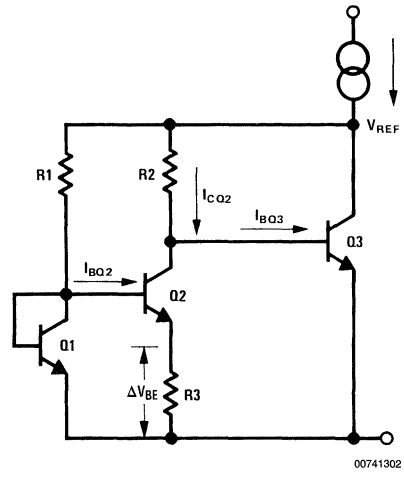


FIGURE 2. Simplified Volt Reference

Figure 2 illustrates a simplified reference using the predictable temperature, voltage, and current relationship of emitter-base junctions.

Assuming $J_{Q1} > J_{Q2}$, $I_{CQ2} \gg I_{BQ2} = I_{BQ3}$,
Area (emitter Q1) = Area (emitter Q2), and

$$V_{BEQ1} = V_{BEQ3}, \quad (1)$$

then

$$V_{REF} \cong \left(\frac{kT}{q} \ln \frac{R2}{R1}\right) \frac{R2}{R3} + V_{BEQ3} \quad (2)$$

SIMPLIFIED LM340

In *Figure 3* the voltage reference includes R1–R3 and Q1–Q5. Q3 also acts as an error amplifier and Q6 as a buffer between Q3 and the current source. If the output drops, this drop is fed back, through R4, R5, Q4, Q5, to the base of Q3. Q7 then conducts more current re-establishing the output given by:

$$V_{OUT} = V_{REF} \frac{R4 + R5}{R4} \quad (3)$$

1.0 Circuit Design (Continued)

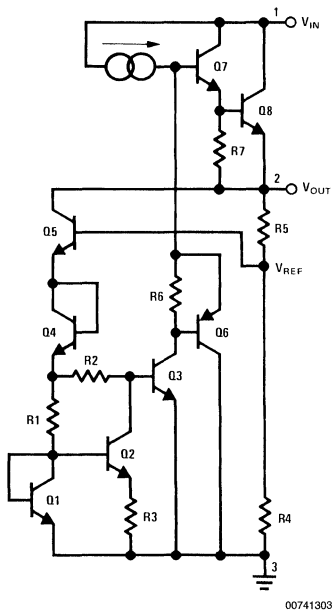


FIGURE 3. LM340 Simplified

COMPLETE CIRCUIT OF THE LM340 *Figure 4*

Here (J_{Q2}, J_{Q3}) > (J_{Q4}, J_{Q5}) and a positive TC ΔV_{BE} appears across R6. This is amplified by 17, (R6/R6 = 17) and is temperature compensated by the V_{BE} of Q6, Q7, Q8 to develop the reference voltage. R17 is changed to get the various fixed output voltages.

SHORT CIRCUIT PROTECTION

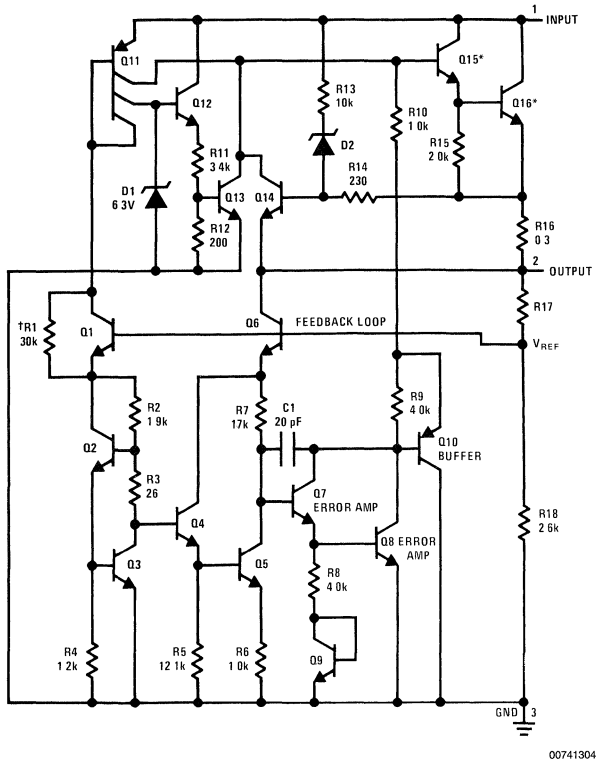
1. V_{IN}–V_{OUT} < 6.0V: There is no current through D2 and the maximum output current will be given by:

$$I_{OUT\ MAX} = \frac{V_{BEQ14}}{R16} \cong 2\ 2A\ (T_j = 25°C) \tag{4}$$

2. V_{IN}–V_{OUT} > 6.0V: To keep Q16 operating within its maximum power rating the output current limit must decrease as V_{IN}–V_{OUT} increases. Here D2 conducts and the drop across R16 is less than V_{BE} to turn on Q14. In this case I_{OUT} maximum is:

$$I_{OUT\ MAX} = \int \frac{1}{R16}\left(V_{BEQ14} - \frac{[(V_{IN} - V_{OUT}) - V_{ZD2} - V_{BEQ14}]}{R13} R14\right)$$
$$= 0.077\ [37.2 - (V_{IN} - V_{OUT})]\ (A)$$
$$\text{at } T_j = 25°C \tag{5}$$

1.0 Circuit Design (Continued)



*Series pass element

†Starting up resistor

FIGURE 4. Complete Circuit of the LM340

THERMAL SHUT DOWN

In *Figure 4* the V_{BE} of Q13 is clamped to 0.4V. When the die temperature reaches approximately +175°C the V_{BE} to turn on Q13 is 0.4V. When Q13 turns on it removes all base drive from Q15 which turns off the regulator thus preventing a further increase in die temperature.

POWER DISSIPATION

The maximum power dissipation of the LM340 is given by:

$$P_{D\,MAX} = (V_{IN\,MAX} - V_{OUT})\, I_{OUT\,MAX} + V_{IN\,MAX}\, I_Q \text{ (W)} \quad (6)$$

The maximum junction temperature (assuming that there is no thermal protection) is given by:

$$T_{jM} = \frac{36 - 13\, I_{OUT\,MAX} - (V_{IN} - V_{OUT})}{0.0855} + 25°C \quad (7)$$

Example:

$V_{IN\,MAX}$ = 23V, $I_{OUT\,MAX}$ = 1.0A, LM340T-15.

Equation *Equation (7)* yields: T_{jM} = 200°C. So the T_j max of 150°C specified in the data sheet should be the limiting temperature.

From *Equation (6)* $P_D \cong 8.1$W. The thermal resistance of the heat sink can be estimated from:

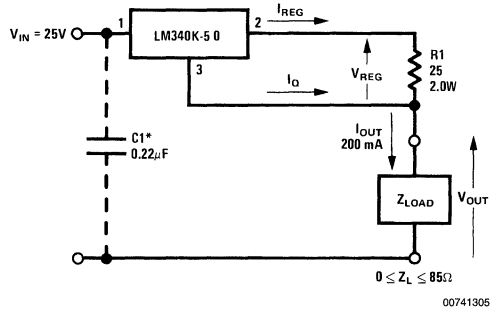
$$\theta_{s\text{-}a} = \frac{T_{jMAX} - T_A}{P_D} - (\theta_{j\text{-}c} + \theta_{c\text{-}s}) \text{ (°C/W)} \quad (8)$$

The thermal resistance $\theta_{j\text{-}c}$ (junction to case) of the TO-220 package is 6°C/W, and assuming a $\theta_{c\text{-}s}$ (case to heat sink) of 0.4, equation *Equation (8)* yields:

$\theta_{s\text{-}a}$ = 8.4°C/W

2.0 Current Source

The circuit shown on *Figure 5* provides a constant output current (equal to $V_{OUT}/R1$ or 200 mA) for a variable load impedance of 0 to 85Ω. Using the following definitions and the notation shown on *Figure 5*, Z_{OUT} and I_{OUT} are:



*Required if regulator is located far from power supply filter

FIGURE 5. Current Source

Q_{CC}/V = Quiescent current change per volt of input/output (pin 1 to pin 2) voltage change of the LM340

L_r/V = Line regulation per volt: the change in the LM340 output voltage per volt of input/output voltage change at a given I_{OUT}.

$$\Delta I_{OUT} = (Q_{CC}/V)\,\Delta V_{OUT} + \frac{L_r/V}{R1}\Delta V_{OUT} \tag{9}$$

$$Z_{OUT} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \tag{10}$$

$$Z_{OUT} = \frac{\Delta V_{OUT}}{(Q_{CC}/V)\Delta V_{OUT} + \frac{(L_r/V)}{R1}\Delta V_{OUT}} \tag{11}$$

$$Z_{OUT} = \frac{1}{(Q_{CC}/V) + \frac{(L_r/V)}{R1}} \tag{12}$$

The LM340-5.0 data sheet lists maximum quiescent current change of 1.0 mA for a 7.0V to 25V change in input voltage; and a line regulation (interpolated for I_{OUT} = 200 mA) of 35 mV maximum for a 7.0V to 25V change in input voltage:

$$Q_{CC}/V = \frac{1.0\text{ mA}}{15V} = 55\ \mu A/V \tag{13}$$

$$L_r/V = \frac{35\text{ mV}}{18V} \cong 2\text{ mV/V} \tag{14}$$

The worst case change in the 200 mA output current for a 1.0V change in output or input voltage using equation *Equation (9)* is:

$$\frac{\Delta I_{OUT}}{1.0V} = 55\ \mu A + \frac{2\text{ mV}}{25\Omega} = 135\ \mu A \tag{15}$$

and the output impedance for a 0 to 85Ω change in Z_L using equation *Equation (12)* is:

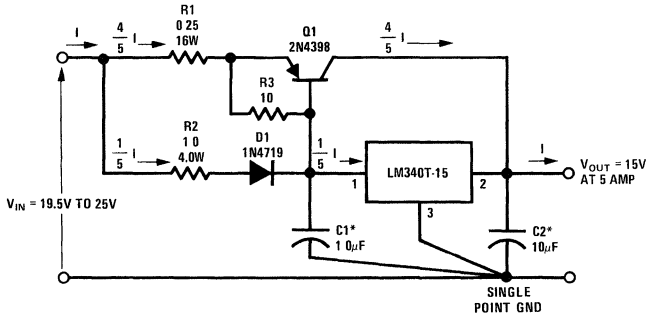
$$Z_{OUT} = \frac{1}{55\ \mu A + \frac{2\text{ mV}}{25\Omega}} = 7.4\text{ k}\Omega \tag{16}$$

Typical measured values of Z_{OUT} varied from 10–12.3 kΩ, or 81–100 μA/V change input or output (approximately 0.05%/V).

3.0 High Current Regulator with Short Circuit Current Limit

The 15V regulator circuit of *Figure 6* includes an external boost transistor to increase output current capability to 5.0A. Unlike the normal boosting methods, it maintains the LM340's ability to provide short circuit current limiting and thermal shut-down without use of additional active components. The extension of these safety features to the external pass transistor Q1 is based on a current sharing scheme using R1, R2, and D1. Assuming the base-to-emitter voltage of Q1 and the voltage drop across D1 are equal, the voltage drops across R1 and R2 are equal. The currents through R1 and R2 will then be inversely proportional to their resistances. For the example shown on *Figure 6*, resistor R1 will have four times the current flow of R2. For reasonable values of Q1 beta, the current through R1 is approximately equal to the collector current of Q1; and the current through R2 is equal to the current flowing through the LM340. Therefore, under overload or short circuit conditions the protection circuitry of the LM340 will limit its own output current and, because of the R1/R2 current sharing scheme, the output current of Q1 as well. Thermal overload protection also extends Q1 when its heat sink has four or more times the capacity of the LM340 heat sink. This follows from the fact that both devices have approximately the same input/output voltage and share the load current in a ratio of four to one.

3.0 High Current Regulator with Short Circuit Current Limit (Continued)



*Solid tantalum

Note 1: Current sharing between the LM340 and Q1 allows the extension of short circuit current limit, safe operating area protection, and (assuming Q1's heat sink has four or more times the capacity of the LM340 head sink) thermal shutdown protection

Note 2: $I_{SHORT\ CIRCUIT}$ is approximately 5.5 amp.

Note 3: $I_{OUT\ MAX}$ at V_{OUT} = 15V is approximately 9 5 amp

FIGURE 6. 15V 5.0A Regulator with Short Circuit Current Limit

The circuit shown on *Figure 6* normally operates at up to 5.0A of output current. This means up to 1.0A of current flows through the LM340 and up to 4.0A flows through Q1. For short term overload conditions the curve of *Figure 7* shows the maximum instantaneous output current versus temperature for the boosted regulator. This curve reflects the approximately 2.0A current limit of the LM340 causing an 8.0A current limit in the pass transistor, or 10A, total.

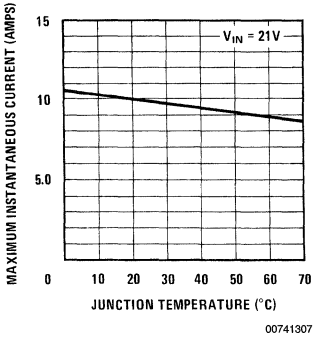


FIGURE 7. Maximum Instantaneous Current vs Junction Temperature

Under continuous short circuit conditions the LM340 will heat up and limit to a steady total state short circuit current of 4.0A to 6.0A as shown in *Figure 8.* This curve was taken using a Wakefield 680-75 heat sink (approximately 7.5°C/W) at a 25°C ambient temperature.

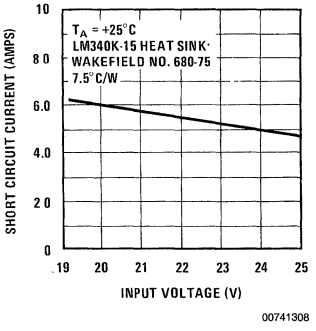


FIGURE 8. Continuous Short Circuit Current vs Input Voltage

For optimum current sharing over temperature between the LM340 and Q1, the diode D1 should be physically located close to the pass transistor on the heat sink in such a manner as to keep it at the same temperature as that of Q1. If the LM340 and Q1 are mounted on the same heat sink the LM340 should be electrically isolated from the heat sink since its case (pin 3) is at ground potential and the case of

3.0 High Current Regulator with Short Circuit Current Limit (Continued)

Q1 (its collector) is at the output potential of the regulator. Capacitors C1 and C2 are required to prevent oscillations and improve the output impedance respectively. Resistor R3 provides a path to unload excessive base charge from the base of Q1 when the regulator goes suddenly from full load to no load. The single point ground system shown on *Figure 6* allows the sense pins (2 and 3) of the LM340 to monitor the voltage directly at the load rather than at some point along a (possibly) resistive ground return line carrying up to 5.0A of load current. *Figure 9* shows the typical variation of load regulation versus load current for the boosted regulator. The insertion of the external pass transistor increases the input/output differential voltage from 2.0V to approximately 4.5V. For an output current less than 5.0A, the R2/R1 ratio can be set lower than 4:1. Therefore, a less expensive PNP transistor may be used.

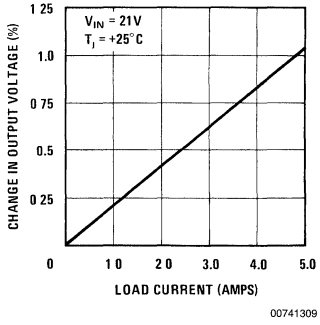


FIGURE 9. Load Regulation

4.0 5.0V, 5.0A Voltage Regulator for TTL

The high current 5.0V regulator for TTL shown in *Figure 11* uses a relatively inexpensive NPN pass transistor with a lower power PNP device to replace the single, higher cost, power PNP shown in *Figure 6.* This circuit provides a 5.0V output at up to 5.0A of load current with a typical load regulation of 1.8% from no load to full load. The peak instantaneous output current observed was 10.4A at a 25°C junction temperature (pulsed load with a 1.0 ms ON and a 200 ms OFF period) and 8 4A for a continuous short circuit. The typical line regulation is 0.02% of input voltage change (I_{OUT} = 0).

One can easily add an overload indicator using the National's new NSL5027 LED. This is shown with dotted lines in *Figure 11.* With this configuration R2 is not only a current sharing resistor but also an overload sensor. R5 will determine the current through the LED; the diode D2 has been added to match the drop across D1. Once the load current exceeds 5.0A (1.0A through the LM340 assuming perfect current sharing and $V_{D1} = V_{D2}$) Q3 turns ON and the overload indicator lights up

Example:

$I_{OVERLOAD}$ = 5.0A

I_{LED} = 40 mA (light intensity of 16 mcd)

$$V_{LED} = 1.75,\ R5 \cong \frac{V_{IN} - 2.65}{I_{LED}} \qquad (17)$$

5.0 Adjustable Output Voltage Regulator for Intermediate Output Voltages

The addition of two resistors to an LM340 circuit allows a non-standard output voltage while maintaining the limiting features built into IC. The example shown in *Figure 10* provides a 10V output using an LM340K-5.0 by raising the reference (pin number 3) of the regulator by 5.0V.

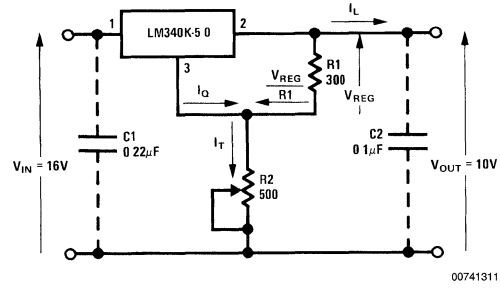
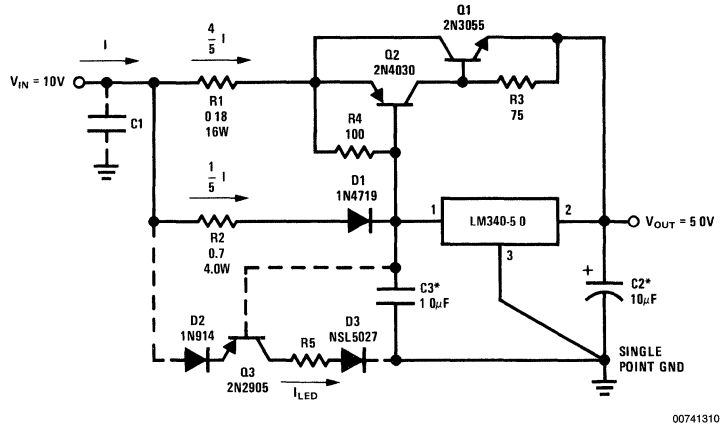


FIGURE 10. 10V Regulator

The 5 0V pedestal results from the sum of regulator quiescent current I_Q and a current equal to $V_{REG}/R1$, flowing through potentiometer R2 to ground R2 is made adjustable to compensate for differences in I_Q and V_{REG} output. The circuit is practical because the change in I_Q due to line voltage and load current changes is quite small.

5.0 Adjustable Output Voltage Regulator for Intermediate Output Voltages

(Continued)



*Solid tantalum

FIGURE 11. 5.0V, 5.0A Regulator for TTL (with short circuit, thermal shutdown protection, and overload indicator)

The line regulation for the boosted regulator is the sum of the LM340 line regulation, its effects on the current through R2, and the effects of ΔI_Q in response to input voltage changes. The change in output voltage is:

$$\Delta V_{OUT} = (L_r/V)\,\Delta V_{IN} + \frac{(L_r/V)\,\Delta V_{IN}\,R2}{R1} + (Q_{CC}/V)\,\Delta V_{IN}\,R2 \quad (18)$$

giving a total line regulation of:

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} = (L_r/V)\left(1 + \frac{R2}{R1}\right) + (Q_{CC}/V)\,R2 \quad (19)$$

The LM340-5.0 data sheet lists $\Delta V_{OUT} < 50$ mV and $\Delta I_Q < 1.0$ mA for $\Delta V_{IN} = 18$V at $I_{OUT} = 500$ mA. This is:

$$L_r/V = \frac{50\text{ mV}}{18\text{V}} \approx 3\text{ mV/V} \quad (20)$$

$$Q_{CC}/V = \frac{1.0\text{ mA}}{18\text{V}} = 55\ \mu\text{A/V} \quad (21)$$

The worst case at line regulation for the circuit of *Figure 10* calculated by equation *Equation (19)*, $I_{OUT} = 500$ mA and R2 = 310Ω is:

$$\frac{\Delta V_{OUT}}{1.0\text{V}} = 3\text{ mV/V}\left(1 + \frac{310\Omega}{300\Omega}\right) + (55\ \mu\text{A/V})310\Omega \quad (22)$$

$$\frac{\Delta V_{OUT}}{1.0\text{V}} = 6\text{ mV/V} + 17\text{ mV/V} = 23\text{ mV/V} \quad (23)$$

This represents a worst case line regulation value of 0.23%/V.

The load regulation is the sum of the LM340 voltage regulation, its effect on the current through R2, and the effect of ΔI_Q in response to changes in load current. Using the following definitions and the notation shown on *Figure 10* ΔV_{OUT} is:

Z_{OUT} = Regulator output impedance: the change in output voltage per amp of load current change.

Z_{340} = LM340 output impedance

Q_{CC}/A= Quiescent current change per amp of load current change

$$\Delta V_{OUT} = (Z_{340})\,\Delta I_L + \frac{(Z_{340})}{R1}\,\Delta I_L\,R2 + (Q_{CC}/A)\,\Delta I_L\,R2 \quad (24)$$

and the total output impedance is:

$$Z_{OUT} = \frac{\Delta V_{OUT}}{\Delta I_L} = Z_{340}\left(1 + \frac{R2}{R1}\right) + (Q_{CC}/A)\,R2 \quad (25)$$

The LM340-5.0 data sheet gives a maximum load regulation $L_r = 50$ mV and $\Delta I_Q = 1.0$ mA for a 1.0A load change.

$$Z_{340} = \frac{50\text{ mV}}{1.0\text{A}} = 0.05\Omega \quad (26)$$

5.0 Adjustable Output Voltage Regulator for Intermediate Output Voltages (Continued)

$$Q_{CC}/A = \frac{1\ mA}{1.0A} = 100\ \mu A/A \quad (27)$$

This gives a worst case dc output impedance (ac output impedance being a function of C2) for the 10V regulator using equation *Equation (25)* of:

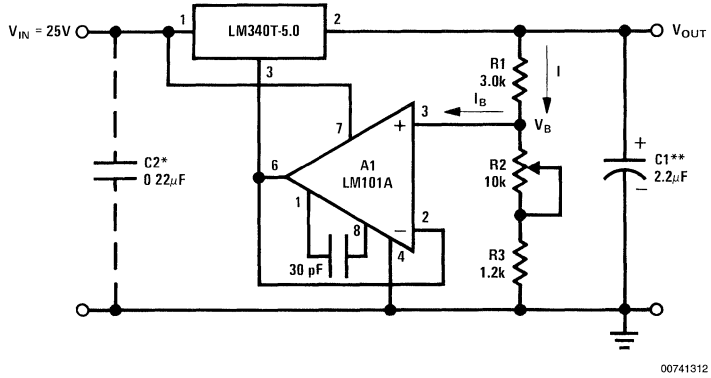
$$Z_{OUT} = 0.05\Omega \left(1 + \frac{310\Omega}{300\Omega}\right) + (100\ \mu A/A)\ 310\Omega \quad (28)$$

$Z_{OUT} = 0.10\Omega + 0.031\Omega = 0.13\Omega$

or a worst case change of approximately 1.5% for a 1.0A load change. Typical measured values are about one-third of the worst case value.

6.0 Variable Output Regulator

In *Figure 12* the ground terminal of the regulator is "lifted" by an amount equal to the voltage applied to the non-inverting input of the operational amplifier LM101A. The output voltage of the regulator is therefore raised to a level set by the value of the resistive divider R1, R2, R3 and limited by the input voltage. With the resistor values shown in *Figure 12*, the output voltage is variable from 7.0V to 23V and the maximum output current (pulsed load) varies from 1.2A to 2.0A (T_j = 25°C) as shown in *Figure 13*.



*Required if the regulator is located far from the power supply filter

**Solid tantalum

FIGURE 12. Variable Output Regulator

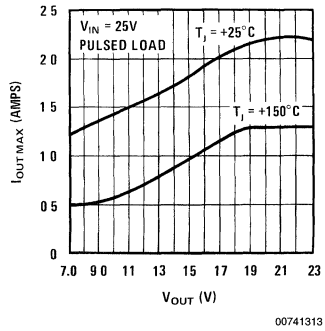


FIGURE 13. Maximum Output Current

Since the LM101A is operated with a single supply (the negative supply pin is grounded). The common mode voltage V_B must be at least at a 2.0 V_{BE} + V_{SAT} above ground. R3 has been added to insure this when R2 = 0. Furthermore the bias current I_B of the operational amplifier should be negligible compared to the current flowing through the resistive divider.

Example:

V_{IN} = 25V

$V_{OUT\ MIN}$ = 5 + V_B, (R2 = 0),

V_B = R3 (I − I_B) = 2.0V

R1 = 2.5 R3

$V_{OUT\ MAX}$ = V_{IN} − dropout volt

(R2 = $R2_{MAX}$)

$R2_{MAX}$ = 3.3 R1

So setting R3, the values of R1 and R2 can be determined.

If the LM324 is used instead of the LM101A, R3 can be omitted since its common mode voltage range includes the ground, and then the output will be adjustable from 5 to a certain upper value defined by the parameters of the system.

The circuit exhibits the short-circuit protection and thermal shutdown properties of the LM340 over the full output range.

6.0 Variable Output Regulator

(Continued)

The load regulation can be predicted as:

$$\Delta V_{OUT} = \frac{R1 + R2 + R3}{R1} \Delta V_{340} \tag{29}$$

where ΔV_{340} is the load regulation of the device given in the data sheet. To insure that the regulator will start up under full load a reverse biased small signal germanium diode, 1N91, can be added between pins 2 and 3.

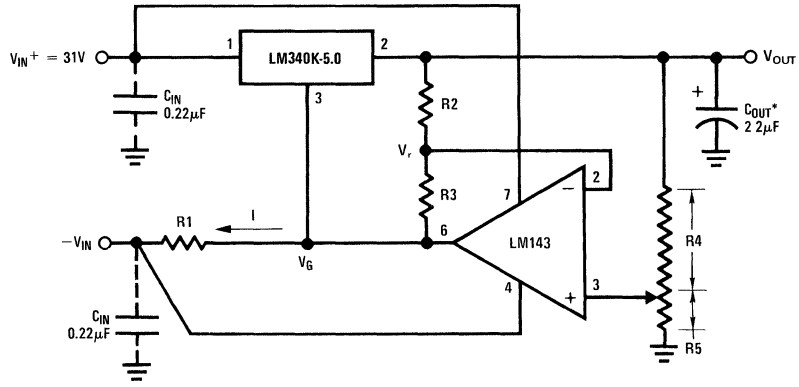
7.0 Variable Output Regulator 0.5V–29V

When a negative supply is available an approach equivalent to that outlined in section 6 may be used to lower the minimum output voltage of the regulator below the nominal voltage that of the LM340 regulator device. In *Figure 14* the voltage V_G at the ground pin of the regulator is determined by the drop across R1 and the gain of the amplifier. The current I may be determined by the following relation:

$$I = \frac{V_{340}}{R1} \frac{R2\,R5 - R3\,R4}{R4\,(R2 + R3)} + \frac{V_{IN}^-}{R1} \tag{30}$$

or if R2 + R3 = R4 + R5 = R

$$I = \frac{V_{340}\,R2}{R1\,R4} + \frac{1}{R1}(V_{IN}^- - V_{340}) \tag{31}$$



*Solid tantalum

FIGURE 14. Variable Output Voltage 0.5V–30V

considering that the output is given by:

$$V_{OUT} = V_G + V_{340} \tag{32}$$

and

$$V_G = R1\,I - V_{IN}^- \tag{33}$$

combining equations 31, 32, and 33 an expression for the output voltage is:

$$V_{OUT} = V_{340} \frac{R2}{R4} \tag{34}$$

Notice that the output voltage is inversely proportional to R4 so the output voltage may be adjusted very accurately for low values. A minimum output of 0.5V has been set. This implies that

$$\frac{R2}{R4} = 0.1 \frac{R3}{R4} = 0.9 \frac{R3}{R2} = 9 \tag{35}$$

An absolute zero output voltage will require R4 = ∞ or R2 = 0, neither being practical in this circuit. The maximum output voltage as shown in *Figure 14* is 30V if the high voltage operational amplifier LM143 is used. If only low values of V_{OUT} are sought, then an LM101 may be used. R1 can be computed from:

$$R1 = \frac{V_{IN}^-}{I_{Q340}} \tag{36}$$

7.0 Variable Output Regulator 0.5V–29V (Continued)

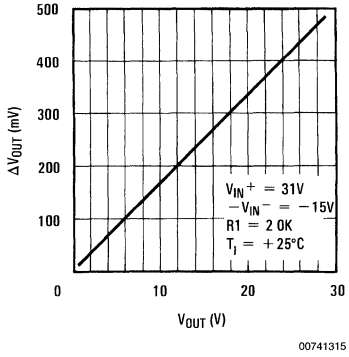


FIGURE 15. Typical Load Regulation for a 0.5V–30V Regulator (ΔI_{OUT} = 1.0A)

Figure 15 illustrates the load regulation as a function of the output voltage

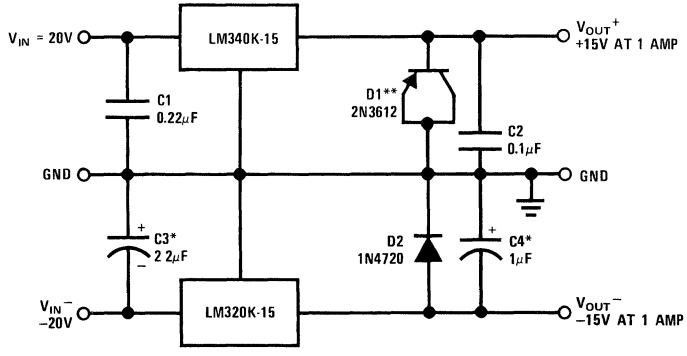
8.0 Dual Power Supply

The plus and minus regulators shown in *Figure 16* will exhibit line and load regulations consistent with their specifications as individual regulators. In fact, operation will be entirely normal until the problem of common loads occurs. A 30Ω load from the +15V output to the −15V output (representing a 0.5A starting load for the LM340K-15 if the LM320K-15 is already started) would allow start up of the LM340 in most cases. To insure LM340 startup over the full temperature range into a worst case 1.0A current sink load the germanium power "diode" D1 has been added to the circuit. Since the forward voltage drop of the germanium diode D1 is less than that of the silicon substrate diode of the LM340 the external diode will take any fault current and allow the LM340 to start up even into a negative voltage load. D1 and silicon diode D2 also protect the regulator outputs from inadvertent shorts between outputs and to ground. For shorts between outputs the voltage difference between either input and the opposite regulator output should not exceed the maximum rating of the device.

The example shown in *Figure 16* is a symmetrical ±15V supply for linear circuits. The same principle applies to non-symmetrical supplies such as a +5.0V and −12V regulator for applications such as registers

9.0 Tracking Dual Regulators

In *Figure 17*, a fraction of the negative output voltage "lifts" the ground pins of the negative LM320K-15 voltage regulator and the LM340K-15 through a voltage follower and an inverter respectively. The dual operational amplifier LM1558 is used for this application and since its supply voltage may go as high as ±22V the regulator outputs may be set between 5.0V and 20V. Because of the tighter output tolerance and the better drift of the LM320, the positive regulator is made to track the negative. The best tracking action is achieved by matching the gain of both operational amplifiers, that is, the resistors R2 and R3 must be matched as closely as possible.



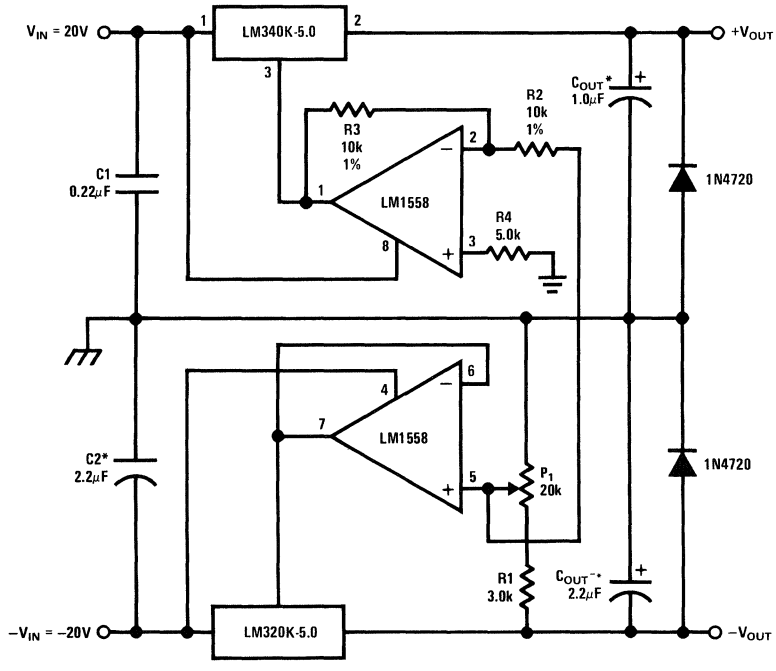
*Solid tantalum

**Germanium diode (using a PNP germanium transistor with the collector shorted to the emitter)

Note: C1 and C2 required if regulators are located far from power supply filter

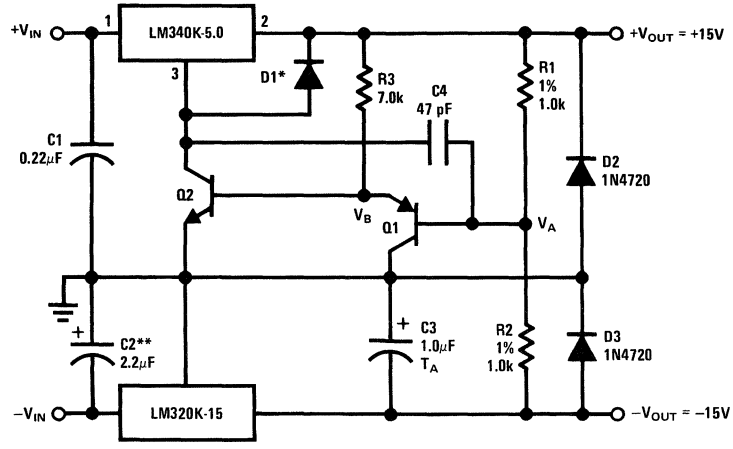
FIGURE 16. Dual Power Supply

9.0 Tracking Dual Regulators (Continued)



*Solid tantalum

FIGURE 17. Tracking Dual Supply ±5.0V – ±18V



*Germanium diode

**Solid tantalum

FIGURE 18. Tracking Dual Supply ±15V

9.0 Tracking Dual Regulators

(Continued)

Indeed, with R2 and R3 matched to better than 1%, the LM340 tracks the LM320 within 40–50 mV over the entire output range. The typical load regulation at V_{OUT} = ±15V for the positive regulator is 40 mV from a 0 to 1.0A pulsed load and 80 mV for the negative.

Figure 18 illustrates ±15V tracking regulator, where again the positive regulator tracks the negative. Under steady state conditions V_A is at a virtual ground and V_B at a V_{BE} above ground. Q2 then conducts the quiescent current of the LM340. If $-V_{OUT}$ becomes more negative the collector base junction of Q1 is forward biased thus lowering V_B and raising the collector voltage of Q2. As a result $+V_{OUT}$ rises and the voltage V_A again reaches ground potential.

Assuming Q1 and Q2 to be perfectly matched, the tracking action remains unchanged over the full operating temperature range.

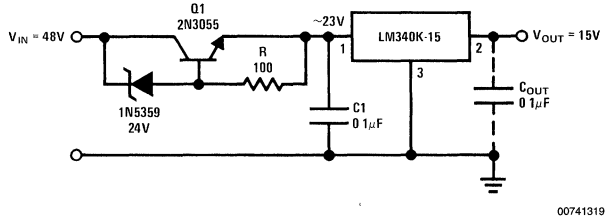
With R1 and R2 matched to 1%, the positive regulator tracks the negative within 100 mV (less than 1%). The capacitor C4 has been added to improve stability. Typical load regulations for the positive and negative sides from a 0 to 1.0A pulsed load (t_{ON} = 1.0 ms, t_{OFF} = 200 ms) are 10 mV and 45 mV respectively.

10.0 High Input Voltage

The input voltage of the LM340 must be kept within the limits specified in the data sheet. If the device is operated above the absolute maximum input voltage rating, two failure modes may occur. With the output shorted to ground, the series pass transistor Q16 (see *Figure 4*) will go to avalanche breakdown; or, even with the output not grounded, the transistor Q1 may fail since it is operated with a collector-emitter voltage approximately 4.0V below the input.

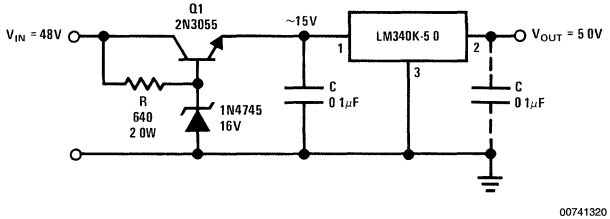
If the only available supply runs at a voltage higher than the maximum specified, one of the simplest ways to protect the regulator is to connect a zener diode in series with the input of the device to level shift the input voltage. The drawback to this approach is obvious. The zener must dissipate (V_{SUPPLY} – $V_{IN\ MAX}$ LM340) (I_{OUTMAX}) which may be several watts. Another way to overcome the over voltage problem is illustrated in *Figure 19* where an inexpensive, NPN-zener-resistor, combination may be considered as an equivalent to the power zener. The typical load regulation of this circuit is 40 mV from 0 to 1.0A pulsed load (T_J = 25°C) and the line regulation is 2.0 mV for 1.0V variation in the input voltage (I_{OUT} = 0). A similar alternate approach is shown in *Figure 20*.

With an optional output capacitor the measured noise of the circuit was 700 µVp-p.



*Heat sink Q1 and LM340

FIGURE 19. High Input Voltage



*Heat sink Q1 and LM340

FIGURE 20. High Input Voltage

10.0 High Input Voltage (Continued)

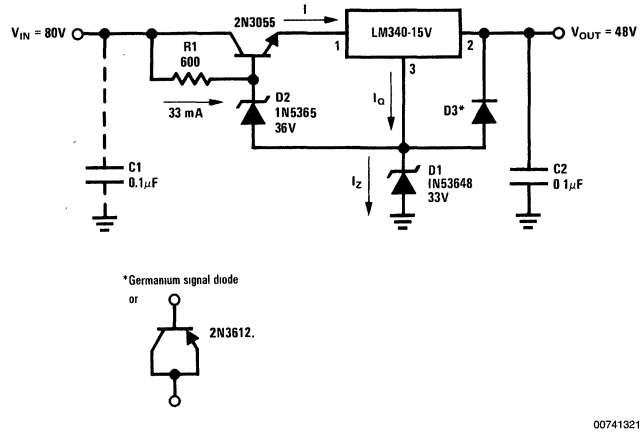


FIGURE 21. High Voltage Regulator

11.0 High Voltage Regulator

In previous sections the principle of "lifting the ground terminal" of the LM340, using a resistor divider or an operational amplifier, has been illustrated. One can also raise the output voltage by using a zener diode connected to the ground pin as illustrated in *Figure 21* to obtain an output level increased by the breakdown voltage of the zener. Since the input voltage of the regulator has been allowed to go as high as 80V a level shifting transistor-zener (D2)—resistor combination has been added to keep the voltage across the LM340 under permissible values. The disadvantage of the system is the increased output noise and output voltage drift due to the added diodes.

Indeed it can be seen that, from no load to full load conditions, the ΔI_Z will be approximately the current through R1 ($\cong$ 35 mA) and therefore the degraded regulation caused by D1 will be V_Z (at 35 mA + I_Q) − V_Z (at I_Q).

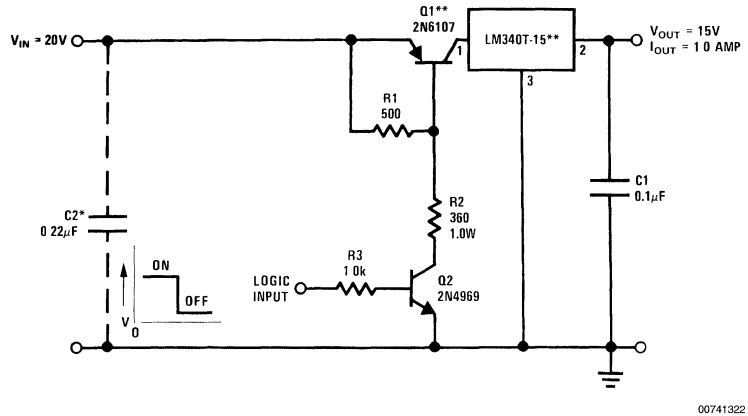
The measured load regulation was 60 mV for ΔI_{OUT} of 5.0 mA to 1.0A (pulsed load), and the line regulation is 0.01%V of input voltage change (I_{OUT} = 500 mA) and the typical output noise 2.0 mVp-p (C2 = 0.1 μF). The value of R1 is calculated as:

$$R1 \cong \beta\left[\frac{V_{IN} - (V_{Z1} + V_{Z2})}{I \text{ full load}}\right] \quad (37)$$

12.0 Electronic Shutdown

Figure 22 shows a practical method of shutting down the LM340 under the control of a TTL or DTL logic gate. The pass transistor Q1 operates either as a saturated transistor or as an open switch. With the logic input high (2.4V specified minimum for TTL logic) transistor Q2 turns on and pulls 50 mA down through R2. This provides sufficient base drive to maintain Q1 in saturation during the ON condition of the switch. When the logic input is low (0.4V specified maximum for TTL logic) Q2 is held off, as is Q1; and the switch is in the OFF condition. The observed turn-on time was 7.0 μs for resistive loads from 15Ω to infinity and the turn-off time varied from approximately 3.0 μs for a 15Ω load to 3.0 ms for a no-load condition. Turn-off time is controlled primarily by the time constant of R_{LOAD} and C1.

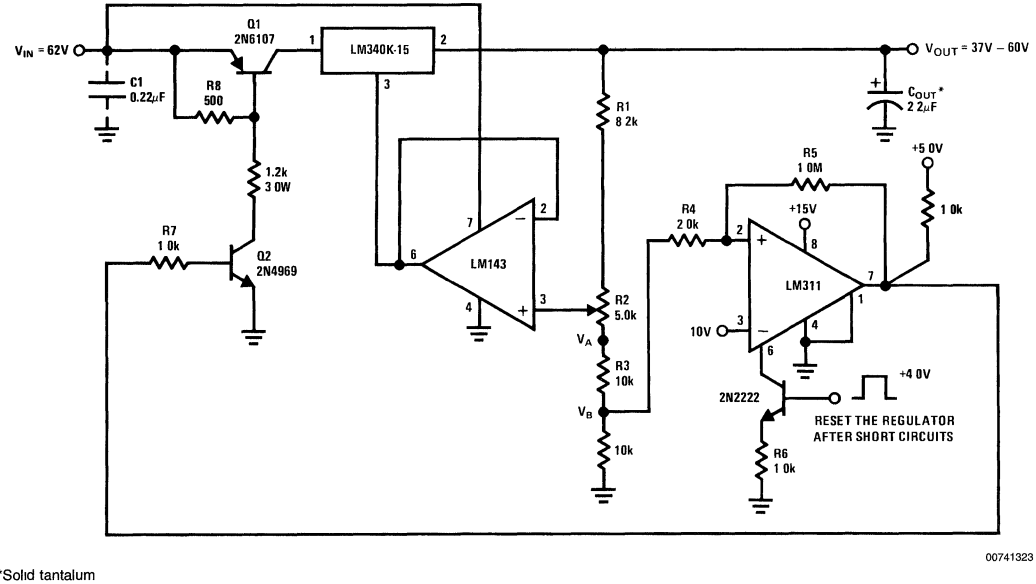
12.0 Electronic Shutdown (Continued)



*Required if the regulator is located far from the power supply filter

**Head sink Q1 and the LM340

FIGURE 22. Electronic Shutdown Circuit



*Solid tantalum

FIGURE 23. Variable High Voltage Regulator with Shortcircuit and Overvoltage Protection

13.0 Variable High Voltage Regulator with Overvoltage Shutdown

A high voltage variable-output regulator may be constructed using the LM340 after the idea illustrated in section 7 and drawn in *Figure 23*. The principal inconvenience is that the voltage across the regulator must be limited to maximum rating of the device, the higher the applied input voltage the higher must be lifted the ground pin of the LM340. Therefore the range of the variable output is limited by the supply voltage limit of the operational amplifier and the maximum voltage allowed across the regulator. An estimation of this range is given by:

$$V_{OUT\ MAX} - V_{OUT\ MIN} = V_{SUPPLY\ MAX340} - V_{NOMINAL340} - 2.0V \quad (38)$$

13.0 Variable High Voltage Regulator with Overvoltage Shutdown (Continued)

Examples:

LM340-15: $V_{OUTMAX} - V_{OUTMIN} = 35 - 15 - 2 = 18V$

Figure 23 illustrates the above considerations. Even though the LM340 is by itself short circuit protected, when the output drops, V_A drops and the voltage difference across the device increases. If it exceeds 35V the pass transistor internal to the regulator will breakdown, as explained in section 11. To remedy this, an over-voltage shutdown is included in the circuit. When the output drops the comparator switches low, pulls down the base Q2 thus opening the switch Q1, and shutting down the LM340. Once the short circuit has been removed the LM311 must be activated through the strobe to switch high and close Q1, which will start the regulator again. The additional voltages required to operate the comparator may be taken from the 62V since the LM311 has a certain ripple rejection and the reference voltage (pin 3) may have a superimposed small ac signal. The typical load regulation can be computed from equation 29.

Bibliography

1. AN-42: *"IC Provides on Card Regulation for Logic Circuits."*

2. Carl T. Nelson: *"Power distribution and regulation can be simple, cheap and rugged."* EDN, February 20, 1973.

Fast IC Power Transistor with Thermal Protection

National Semiconductor
Application Note 110
George Cleveland

Introduction

Overload protection is perhaps most necessary in power circuitry. This is shown by recent trends in power transistor technology. Safe-area, voltage and current handling capability have been increased to limits far in excess of package power dissipation In RF transistors, devices are now available and able to withstand badly mismatched loads without destruction. However, for anyone working with power transistors, they are still easily destroyed.

Since power circuitry, in many cases, drives other low level circuitry—such as a voltage regulator—protection is doubly important Overloads that cause power transistor failure can result in the destruction of the entire circuit. This is because the common failure mode for power transistors is a short from collector to emitter—applying full voltage to the load. In the case of a voltage regulator, the raw supply voltage would be applied to the low level circuitry.

A new monolithic power transistor provides virtually absolute protection against any type of overload. Included on the chip are current limiting, safe area protection and thermal limiting. Current limiting controls the peak current through the chip to a safe level below the fuzing current of the aluminum metalization. At high collector to emitter voltage the safe area limiting reduces the peak current to further protect the power transistor. If, under prolonged overload, power dissipation causes chip temperature to rise toward destructive levels, thermal limiting turns off the device keeping the devices at a safe temperature. The inclusion of thermal limiting, a feature not easily available in discrete circuitry makes this device especially attractive in applications where normal protective schemes are ineffective.

The device's high gain and fast response further reduce requirements of surrounding circuitry. As well as being used in linear applications, the IC can interface transistor-transistor logic or complementary-MOS logic to power loads without external devices. In fact, the input-current requirement of 3 microamperes is small enough for one CMOS gate to drive over 400 LM195's.

Besides high dc current gain, the IC has low input capacitance so it can be easily driven from high impedance sources—even at high frequencies. In a standard TO-3 power package, the monolithic structure ties the emitter, rather than the collector, to the case effectively boot-strapping the base-to-package capacitance. Additionally, connecting the emitter to the package is especially convenient for grounded emitter circuits.

The device is fully protected against any overload condition when it is used below the maximum voltage rating. The current-limiting circuitry restricts the power dissipation to 35 watts, 1.8 amperes are available at collector-to-emitter voltage of 17V decreasing to about 0.8 amperes at 40V. In reality, however, like standard transistors, power dissipation in actual use is limited by the size of the external heat sink.

Switching time is fast also. At 40V 25 Ohm load can be switched on or off in a relatively fast 500 ns. The internal planar double diffused monolithic transistors have an f_t of 200 MHz to 400 MHz. The limiting factor on overall speed is the protective and biasing circuitry around the output transistors. An important performance point is that no more than the normal 3 μA base current is needed for fast switching.

To the designer, the LM195 acts like an ordinary power transistor, and its operation is almost identical to that of a standard power device. However, it provides almost absolute protection against any type of overload And, since it is manufactured with standard seven-mask IC technology, the device is produceable in large quantities at reasonable cost.

Circuit Design

Besides the protective features, the monolithic power transistor should function as closely to a discrete transistor as possible. Of course, due to the circuitry on the chip, there will be some differences.

Figure 1 shows a simplified schematic of the power transistor. A power NPN Darlington is driven by an input PNP. The PNP and output NPN's are biased by internal current source I_1. The composite three transistors yield a total current gain in excess of 10^6 making it easy to drive the power transistors from high impedance sources. Unlike normal power transistors, the base current is negative, flowing out of the PNP. However, in most cases this is not a problem.

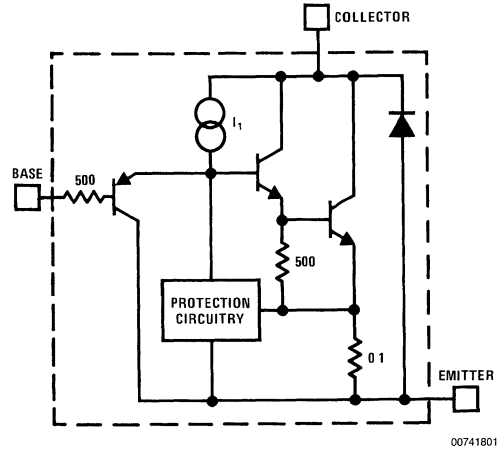


FIGURE 1. Simplified Circuit of the LM195

The input PNP transistor is made with standard IC processing and has a reverse base-emitter breakdown voltage in excess of 40V. This allows the power transistor to be driven from a stiff voltage source without damage due to excessive base current. At input voltages in excess of about 1V the input PNP becomes reverse biased and no current is drawn from the base lead. In fact it is possible for the base of the monolithic transistor to be driven with up to 40V even though the collector to emitter voltage is low. Further, the input PNP isolates the base drive from the protective circuitry insuring

Circuit Design (Continued)

that even with high base drive the device will be protected. When the device is turned off current I_1 is shunted from the base of the NPN transistor by the PNP and appears at the emitter terminal. This sets the minimum load current to about 2 mA, not a severe restriction for a power transistor. Because of the PNP and I_1, the power transistor turns "on" rather than "off" if the base is opened; however, most power circuits already include a base-emitter resistor to absorb leakage currents in present power transistors.

A schematic of the LM195 is shown in *Figure 2*. The circuitry is biased by four current sources comprised of Q4, Q7, Q8 and Q9. The operating current is set by Q5 and Q6 and is relatively independent of supply voltage. FET Q1 and R2 insure reliable starting of the bias circuitry while D1 clamps the output of the FET limiting the starting current at high supply voltage.

The output transistors Q19 and Q20 are driven from input PNP Q14. Current limiting independent of temperature changes is provided by Q21, Q16, and Q15. At high collector to emitter voltages the current limit decreases due to the voltage across R21 from D3, D4 and R20. The double emitter structure used on Q21 allows the power limiting to more closely approximate constant power curve rather than a straight line decrease in output current as input voltage increases.

Transistor Q13 thermally limits the device by removing the base drive at high temperature. The actual temperature sensing is done by Q11 and Q12 with Q10 regulating the voltage across the sensors so thermal limit temperature remains independent of supply. As temperature increases, the collector current of Q11 increases while the V_{BE} of Q12 decreases. At about 170˚C the Q12 turns on Q13 removing the base drive from the output transistors. Finally, C1, Q2 and Q3 boost operating currents during switching to obtain faster response time and Q17 and Q18 compensate for h_{fe} variations in the power devices.

Performance

The new power transistor is packaged in a standard TO-3 transistor package making it compatible with standard power transistors. An added advantage of the monolithic structure is that the emitter is tied to the case rather than the collector. This allows the device to be connected directly to ground in collector output applications.

A photomicrograph of the LM195 is shown in *Figure 3*. More than half of the die area is needed for the output power transistor (Q20). Actually, the power transistor is many individual small transistors connected in parallel with a common collector. Partitioning the power device into small discrete areas improves power handling over a single large device. Firstly, the power device has ten base sections spread across the chip. Between the base diffusion are N+ collector contacts. Each section has its own emitter ballasting resistor to insure current sharing between sections. One of these resistors is used to sense the output current for current limiting.

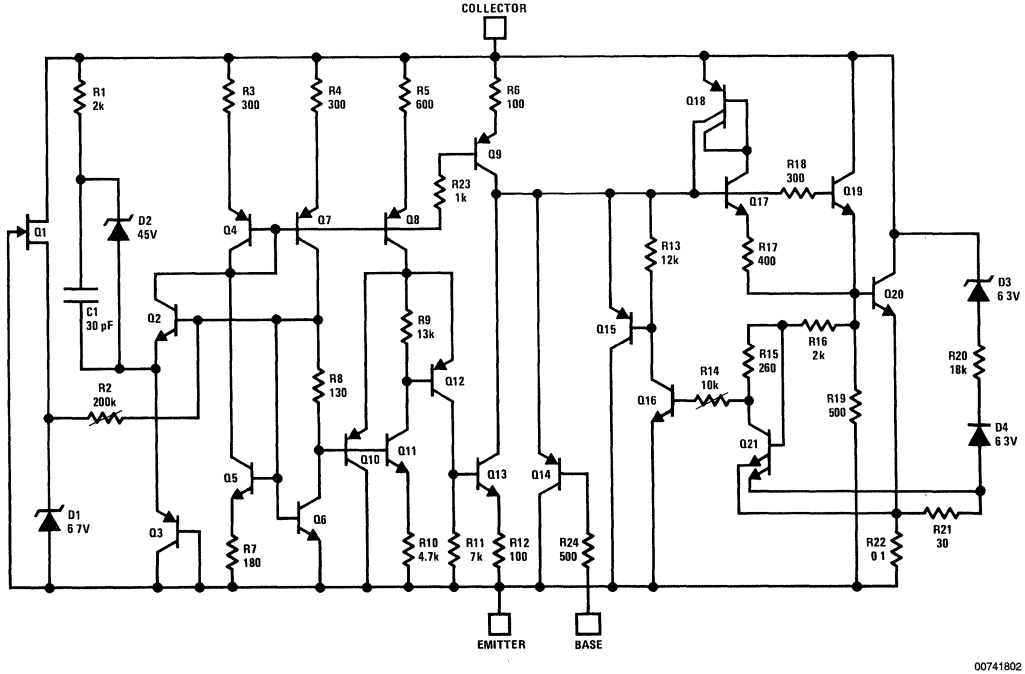


FIGURE 2. Schematic Diagram of the LM195

Performance (Continued)

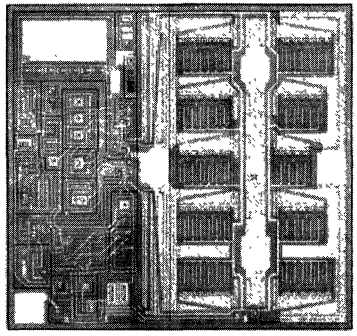


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FIGURE 3. LM195 Chip

TABLE 1. Typical Performance

Collector to Emitter Voltage	42V
Base to Emitter Voltage (max.)	42V
Peak Collector Current (internally limited)	1.8 amps
Reverse Base Emitter Voltage	20V
Base to Emitter Voltage (I_c = 1.0 amp)	0.9V
Base Current	3 μA
Saturation Voltage	2V
Switching Time (turn on or turn off)	500 ns
Power Dissipation (internally limited)	35 watts
Thermal Limit Temperature	165°C
Maximum Operating Temperature	150°C
Thermal Resistance (Junction to Case)	2.3°C/W

A detail of one of the base sections is shown in *Figure 4*. An interdigitated structure is used with alternating base contacts and emitter stripes. Integrated into each emitter is an individual emitter ballasting resistor to insure equal current sharing between emitters in each section. Aluminum metalization runs the length of the emitter stripe to prevent lateral voltage drop from debiasing a section of the stripe at high operating currents. All current in the stripe flows out through the small ballasting resistor where it is summed with the currents from the other stripes in the section. The partitioning in conjunction with the emitter resistor gives a power transistor with large safe-area and good power handling capability.

Applications

With the full protection and high gain offered by this monolithic power transistor, circuit design is considerably simplified. The inclusion of thermal limiting, not normally available in discrete design allows the use of smaller heat sinks than with conventional protection circuitry. Further, circuits where protection of the power device is difficult—if not impossible—now cause no problems.

For example, with only current limiting, the power transistor heat sink must be designed to dissipate worst case overload power dissipation at maximum ambient temperature. When the power transistor is thermally limited, only normal power need be dissipated by the heat sink. During overload, the device is allowed to heat up and thermally limit, drastically reducing the size of the heat sink needed.

Switching circuits such as lamp drivers, solenoid drivers or switching regulators do not dissipate much power during normal operation and usually no heat sink is necessary. However, during overload, the full supply voltage times the maximum output current must be dissipated. Without a large heat sink standard power transistors are quickly destroyed.

Using this new device is easier than standard power transistors but a few precautions should be observed. About the only way the device can be destroyed is excessive collector to emitter voltage or improper power supply polarity. Sometimes when used as an emitter follower, low level high frequency oscillations can occur. These are easily cured inserting a 5k-10k resistor in series with the base lead. The resistor will eliminate the oscillation without effecting speed or performance. Good power supply bypassing should also be used since this is a high frequency device.

Applications (Continued)

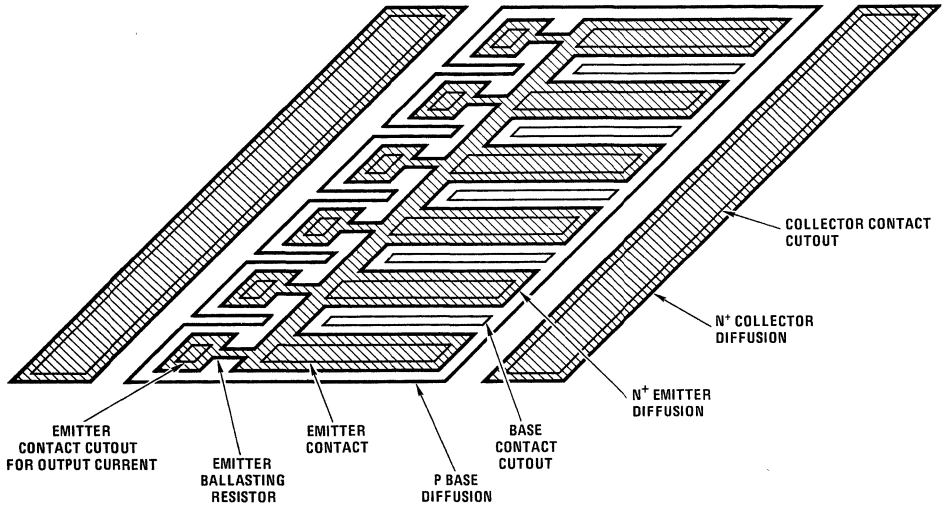
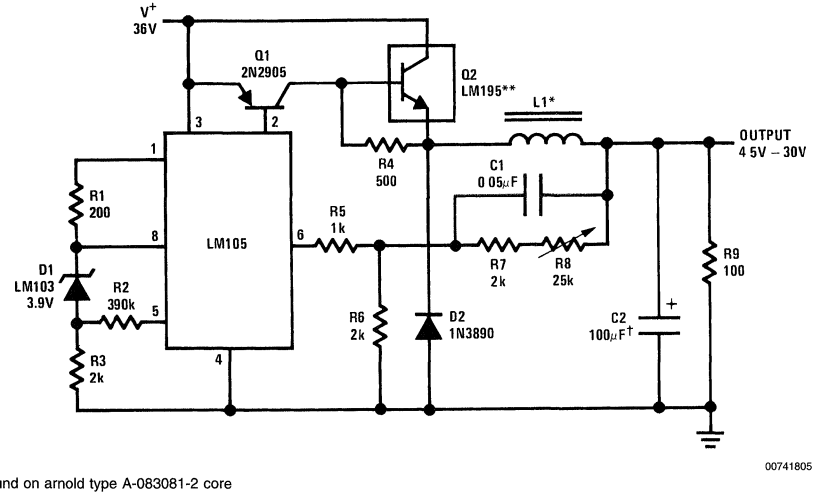


FIGURE 4. Detailed Structure of one Section of the Power Transistor



* Sixty turns wound on arnold type A-083081-2 core

** Four devices in parallel

† Solid tantalum

FIGURE 5. 6 Amp Variable Output Switching Regulator

Figure 5 shows a 6 amp, variable output switching regulator for general purpose applications. An LM105 positive regulator is used as the amplifier-reference for the switching regulator. Positive feedback to induce switching is obtained from the LM105 at pin 1 through an LM103 diode. The positive feedback is applied to the internal amplifier at pin 5 and is independent of supply voltage. This forces the LM105 to drive the pass devices either "on" or "off," rather than linearly controlling their conduction. Negative feedback, delayed by L1 and the output capacitor, C2, causes the regulator to switch with the duty cycle automatically adjusting to provide a constant output. Four LM195's are used in parallel to obtain a 6 amp output since each device can only supply about 2 amps. Note that no ballasting resistors are needed

Applications (Continued)

for current sharing. When Q1 turns "on" all bases are pulled up to V^+ and no base current flows in the LM195 transistors since the input PNP's are reverse biased.

A two terminal current/power limiter is shown in *Figure 6.* The base and collector are shorted—turning the power transistor on. If the load current exceeds 2 amps, the device current limits protecting the load. If the overload remains on, the device will thermal limit, further protecting itself and the load. In normal operation, only 2V appear across the device so high efficiency is realized and no heat sink is needed. Another method of protection would be to place the monolithic power transistor on a common heat sink with the devices to be protected. Overheating will then cause the LM195 to thermal limit protecting the rest of the circuitry.

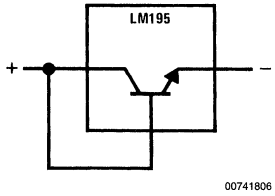


FIGURE 6. Two Terminal Current Limiter

The low base current make this power device suitable for many unique applications. *Figure 7* shows a time delay circuit. Upon application of power or S1 closing, the load is energized. Capacitor C1 slowly charges toward V^- through R1. When the voltage across R1 decreases below about 0.8 volts the load is de-energized. Long delays can be obtained with small capacitor values since a high resistance can be used.

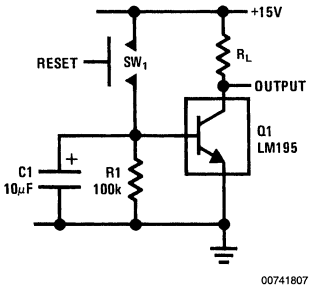


FIGURE 7. Time Delay Circuit

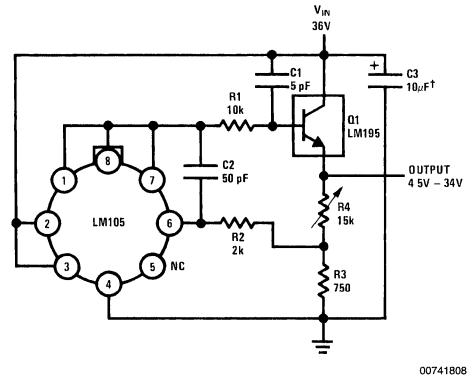
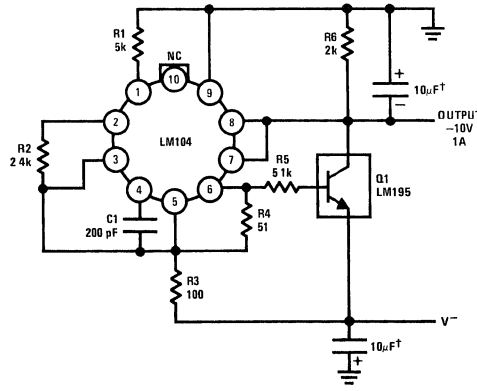


FIGURE 8. 1 Amp Positive Voltage Regulator



† Solid tantalum

FIGURE 9. 1 Amp Negative Regulator

Figure 8 and *Figure 9* show how the LM195 can be used with standard IC's to make positive or negative voltage regulators. Since the current gain of the LM195 is so high, both regulators have better than 2 mV load regulation. They are both fully overload protected and will operate with only 2V input-to-output voltage differential.

An optically isolated power transistor is shown in *Figure 10.* D1 and D2 are almost any standard optical isolator. With no drive, R1 absorbs the base current of Q1 holding it off. When

Applications (Continued)

power is applied to the LED, D2 allows current to flow from the collector to base. Less than 20 µA from the diode is needed to turn the LM195 fully on.

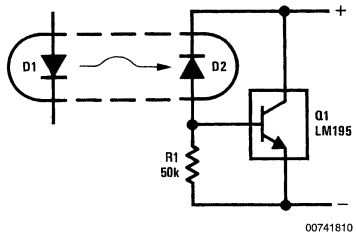


FIGURE 10. Optically Isolated Power Transistor

An alternate connection for better ac response is to return the cathode of D2 to separate positive supply rather than the collector of Q1, as shown in *Figure 11*, eliminating the added collector to base capacitance of the diode. With this circuit a 40V 1 amp load can be switched in 500 ns. Of course, any photosensitive diode can be used instead of the opto-isolator to make a light activated switch.

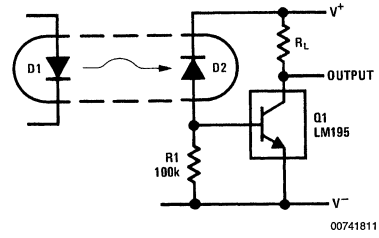


FIGURE 11. Fast Optically Isolated Switch

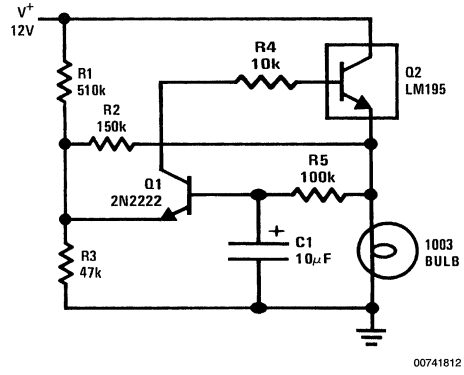
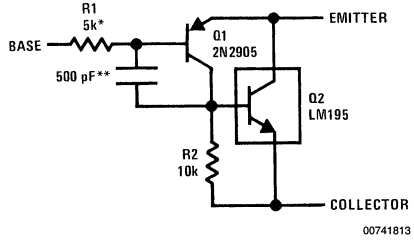


FIGURE 12. 1 Amp Lamp Flasher

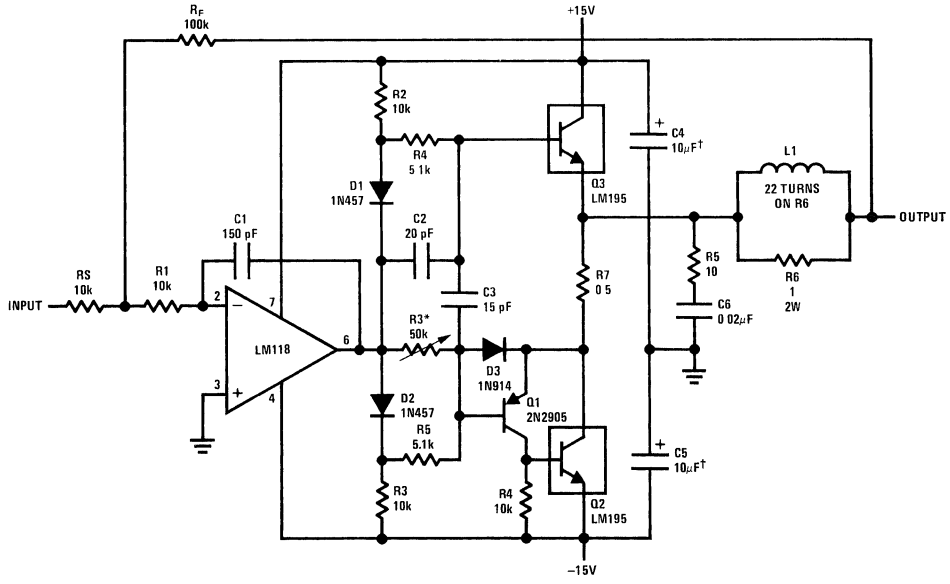


* Protects against excessive base drive

** Needed for stability

FIGURE 13. PNP Configuration for LM195

Applications (Continued)



* Adjust for 50 mA quiescent current.

† Solid tantalum

FIGURE 14. Power Op Amp

A power lamp flasher is shown in *Figure 12*. It is designed to flash a 12V bulb at about a once-per second rate. The reverse base current of Q2 provides biasing for Q1 eliminating the need for a resistor. Typically, a cold bulb can draw 8 times its normal operating current. Since the LM195 is current limited, high peak currents to the bulb are not experienced during turn-on. This prolongs bulb life as well as easing the load on the power supply.

Since no PNP equivalent of this device is available, it is advantageous to use the LM195 in a quasi-complementary configuration to simulate a power PNP. *Figure 13* shows a quasi PNP made with an LM195. A low current PNP is used to drive the LM195 as the power output device. Resistor R1 protects against overdrive destroying the PNP and, in conjunction with C1, frequency compensates the loop against oscillations. Resistor R2 sets the operating current for the PNP and limits the collector current.

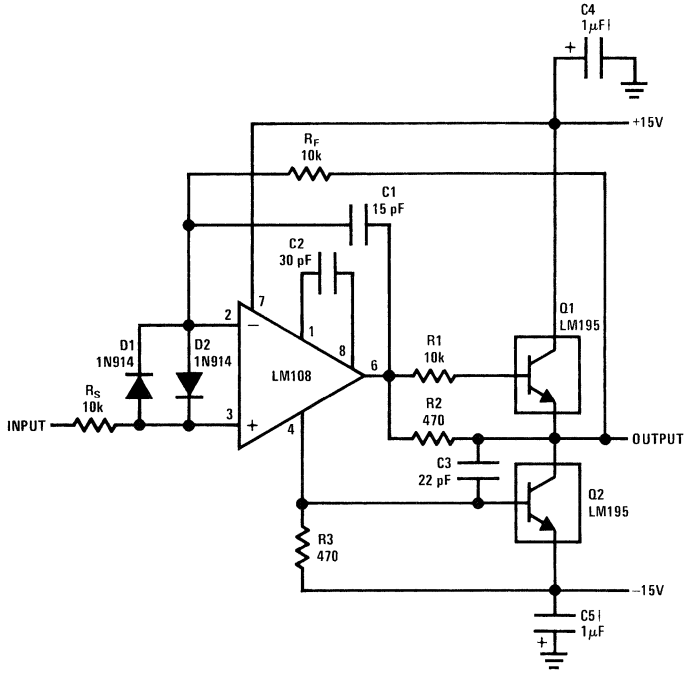
Figure 14 shows a power op amp with a quasi-complementary power output stage. Q1 and Q2 form the equivalent of a power PNP. The circuit is simply an op amp with a power output stage. As shown, the circuit is stable for almost any load. Better bandwidth can be obtained by decreasing C1 to 15 pF (to obtain 150 kHz full output response), but capacitive loads can cause oscillation. If due to layout, the quasi-complimentary loop oscillates, collector to base capacitance on Q1 will stabilize it. A simpler power op amp for up to 300 Hz operation is shown in *Figure 15*.

One of the more difficult circuit types to protect is a current regulator. Since the current is already fixed, normal protection doesn't work. Circuits to limit the voltage across the current regulator may allow excessive current to flow through the load. About the only protection method that protects both the regulator and the driven circuit is thermal limiting.

A 100 mA, two terminal regulator is shown in *Figure 16*. The circuit has low temperature coefficient and operates down to 3V. Once again, the reverse base current of the LM195 to bias the operating circuitry.

A 2N2222 is used to control the voltage across a current sensing resistor, R2 and diode D1, and therefore the current through it. The voltage across the sense network is the V_{BE} of the 2N2222 plus 1.2V from the LM113. In the sense network R2 sets the current while D1 compensates for the V_{BE} of the transistor. Resistor R1 sets the current through the LM113 to 0.6 mA.

Applications (Continued)



†Solid tantalum

FIGURE 15. 1 Amp Voltage Follower

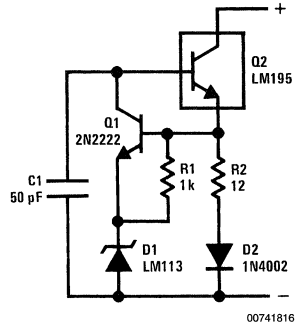


FIGURE 16. Two Terminal 100 mA Current Regulator

Conclusions

A new IC power transistor has been developed that significantly improves power circuitry reliability. The device is virtually impossible to destroy through abuse. Further it has high gain and fast response. It is manufactured with standard seven mask IC technology making it produceable in large quantities at reasonable prices. Finally, in addition to the protection features, it has high gain simplifying surrounding circuitry.

3-Terminal Regulator is Adjustable

National Semiconductor
Application Note 181

Introduction

Until now, all of the 3-terminal power IC voltage regulators have a fixed output voltage. In spite of this limitation, their ease of use, low cost, and full on-chip overload protection have generated wide acceptance. Now, with the introduction of the LM117, it is possible to use a single regulator for any output voltage from 1.2V to 37V at 1.5A. Selecting close-tolerance output voltage parts or designing discrete regulators for particular applications is no longer necessary since the output voltage can be adjusted. Further, only one regulator type need be stocked for a wide range of applications. Additionally, an adjustable regulator is more versatile, lending itself to many applications not suitable for fixed output devices.

In addition to adjustability, the new regulator features performance a factor of 10 better than fixed output regulators. Line regulation is 0.01%/V and load regulation is only 0 1%. It is packaged in standard TO-3 transistor packages so that heat sinking is easily accomplished with standard heat sinks. Besides higher performance, overload protection circuitry is improved, increasing reliability.

Adjustable Regulator Circuit

The adjustment of a 3-terminal regulator can be easily understood by referring to *Figure 1*, which shows a functional circuit An op amp, connected as a unity gain buffer, drives a power Darlington. The op amp and biasing circuitry for the regulator are arranged so that all the quiescent current is delivered to the regulator output (rather than ground) eliminating the need for a separate ground terminal. Further, all the circuitry is designed to operate over the 2V to 40V input to output differential of the regulator.

A 1.2V reference voltage appears inserted between the non-inverting input of the op amp and the adjustment terminal. About 50 µA is needed to bias the reference and this current comes out of the adjustment terminal. In operation, the output of the regulator is the voltage of the adjustment terminal plus 1.2V. If the adjustment terminal is grounded, the device acts as a 1.2V regulator. For higher output voltages, a divider R1 and R2 is connected from the output to ground as is shown in *Figure 2*. The 1.2V reference across resistor R1 forces 5 mA of current to flow. This 5 mA then flows through R2, increasing the voltage at the adjustment terminal and therefore the output voltage. The output voltage is given by:

$$V_{OUT} = 1.2V\left(1 + \frac{R2}{R1}\right) + 50\ \mu A\ R2$$

The 50 µA biasing current is small compared to 5 mA and causes only a small error in actual output voltages. Further, it is extremely well regulated against line voltage or load current changes so that it contributes virtually no error to dynamic regulation. Of course, programming currents other than 5 mA can be used depending upon the application.

Since the regulator is floating, all the quiescent current must be absorbed by the load. With too light of a load, regulation is impaired. Usually the 5 mA programming current is sufficient; however, worst case minimum load for commercial grade parts requires a minimum load of 10 mA. The minimum load current can be compared to the quiescent current of standard regulators.

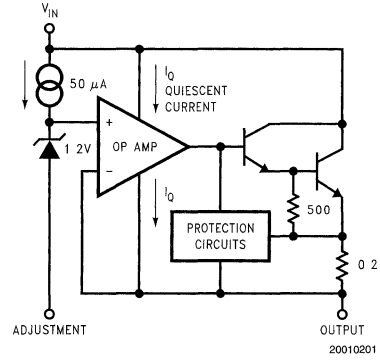
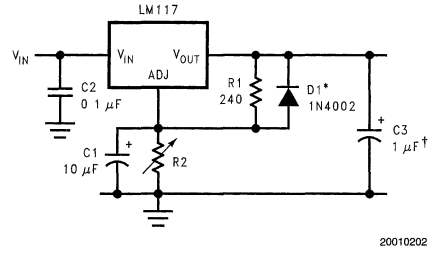


FIGURE 1. Functional Schematic of the LM117



†Solid tantalum

*Discharges C1 if output is shorted to ground

FIGURE 2. Adjustable Regulator with Improved Ripple Rejection

Overload Protection Circuitry

An important advancement in the LM117 is improved current limit circuitry. Current limit is set internally at about 2.2A and the current limit remains constant with temperature. Older devices such as the LM309 or LM7800 regulators use the turn-on of an emitter-base junction of a transistor to set the current limit. This causes current limit to typically change by a factor of 2 over a −55°C to +150°C temperature range. Further, to insure adequate output current at 150°C the current limit is relatively high at 25°C, which can cause problems by overloading the input supply.

Also included is safe-area protection for the pass transistor to decrease the current limit as input-to-output voltage differential increases. The safe area protection circuit in the LM117 allows full output current at 15V differential and does not allow the current limit to drop to zero at high

Overload Protection Circuitry

(Continued)

input-to-output differential voltages, thus preventing start up problems with high input voltages. *Figure 3* compares the current limit of the LM117 to an LM340 regulator.

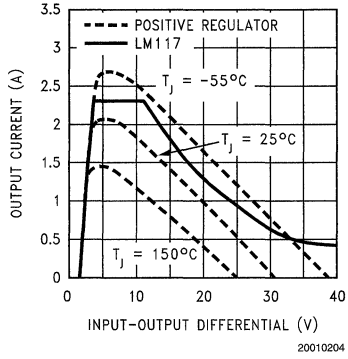


FIGURE 3. Comparison of LM117 Current Limit with Older Positive Regulator

Thermal overload protection, included on the chip, turns the regulator OFF when the chip temperature exceeds about 170°C, preventing destruction due to excessive heating. Previously, the thermal limit circuitry required about 7V to operate. The LM117 has a new design that is operative down to about 2V. Further, the thermal limit and current limit circuitry in the LM117 are functional, even if the adjustment terminal should be accidently disconnected.

Operating the LM117

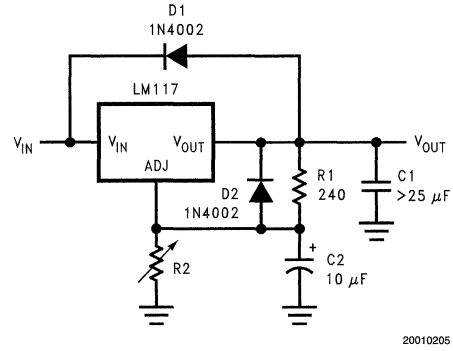
The basic regulator connection for the LM117, as shown in *Figure 2*, only requires the addition of 2 resistors and a standard input bypass capacitor. Resistor R2 sets the output voltage while R1 provides the 5 mA programming current. The 2 capacitors on the adjustment and output terminals are optional for improved performance.

Bypassing the adjustment terminal to ground improves ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10 µF bypass capacitor, 80 dB ripple rejection is obtainable at any output level. Increases over 10 µF do not appreciably improve the ripple rejection at 120 Hz. If a bypass capacitor is used, it is sometimes necessary to include protection diodes as discussed later, to prevent the capacitor from discharging through internal low current paths in the LM117 and damaging the device.

Although the LM117 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1 µF solid tantalum (or 25 µF aluminum electrolytic) on the output swamps this effect and insures stability. When external capacitors are used with any IC regulator, it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10 µF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the LM117, this discharge path is through a large junction that is able to sustain a 20A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 20 µF or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal (C2) can discharge through a low current junction. Discharge occurs when either the input or output is shorted. Internal to the LM117 is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V and less than 10 µF capacitance. *Figure 4* shows an LM117 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.



$$V_{OUT} = 1.25V \left(1 + \frac{R2}{R1}\right) + R2 * I_{ADJ}$$

D1 protects against C1 (input shorts)
D2 protects against C2 (output shorts)

FIGURE 4. Regulator with Protection Diodes Against Capacitor Discharge

Some care should be taken in making connection to the LM117 to achieve the best load regulation. Series resistance between the output of the regulator and programming resistor R1 should be minimized. Any voltage drop due to load current through this series resistance appears as a change in the reference voltage and degrades regulation. If possible, 2 wires should be connected to the output—1 for load current and 1 for resistor R1. The ground of R2 can be returned near the ground of the load to provide remote sensing and improve load regulation.

Applications

Figure 5 shows a 0V to 25V general purpose lab supply. Operation of the LM317 down to 0V output requires the addition of a negative supply so that the adjustment terminal

Applications (Continued)

can be driven to −1.2V. An LM329 6.9V reference is used to provide a regulated −1.2V reference to the bottom of adjustment pot R2. The LM329 is an IC zener which has exceptionally low dynamic impedance so the negative supply need not be well regulated. Note that a 10 mA programming current is used since lab supplies are often used with no-load, and the LM317 requires a worst-case minimum load of 10 mA.

The 1.2V minimum output of the LM117 makes it easy to design power supplies with electrical shut-down. At 1.2V, most circuits draw only a small fraction of their normal operating current. In *Figure 6*, a TTL input signal causes Q1 to ground the adjustment terminal decreasing the output to 1.2V. If true zero output is desired, the adjustment can be driven to −1.2V; however, this does require a separate negative supply.

When fixed output voltage regulators are used as on-card regulator for multiple cards, the normal output voltage tolerance of ±5% between regulators can cause as much as 10% difference in operating voltage between cards.

This can cause operating speed differences in digital circuitry, interfacing problems or decrease noise margins.

Figure 7 shows a method of adjusting multiple on-card regulators so that all outputs track within ±100 mV. The adjustment terminals of all devices are tied together and a single divider is used to set the outputs. Programming current is set at 10 mA to minimize the effects of the 50 µA biasing current of the regulators and should further be increased if many LM117's are used. Diodes connected across each regulator insure that all outputs will decrease if 1 regulator is shorted.

Two terminal current regulators can be made with fixed-output regulators; however, their high output voltage and high quiescent current limit their accuracy. With the LM117 as shown in *Figure 8*, a high performance current source useful from 10 mA to 1.5A can be made. Current regulation is typically 0.01%/V even at low currents since the quiescent current does not cause an error. Minimum operating voltage is less than 4V, so it is also useful as an in-line adjustable current limiter for protection of other circuitry.

Low cost adjustable switching regulators can be made using an LM317 as the control element. *Figure 9* shows the simplest configuration. A power PNP is used as the switch driving an L-C filter. Positive feedback for hysteresis is applied to the LM317 through R6. When the PNP switches, a small square wave is generated across R5. This is level shifted and applied to the adjustment terminal of the regulator by R4 and C2, causing it to switch ON or OFF. Negative

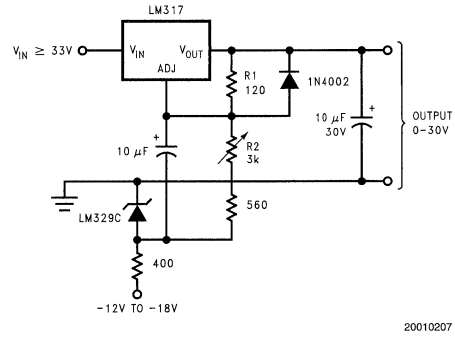
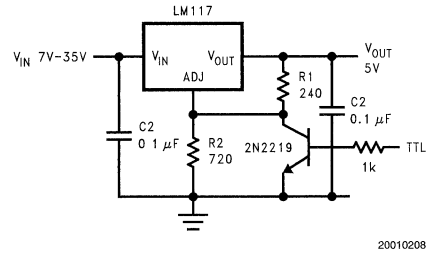
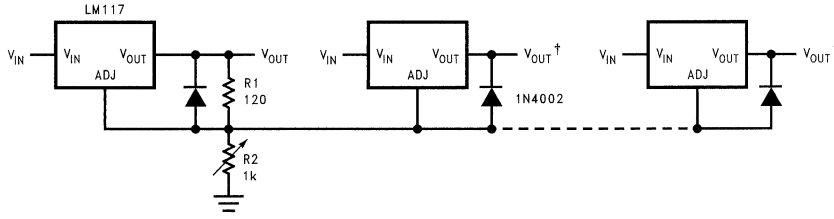


FIGURE 5. General Purpose 0–30V Power Supply



*Min output ≈ 1.2V

FIGURE 6. 5V Logic Regulator with Electronic Shutdown*

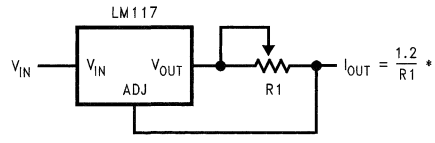


*All outputs within ±100 mV

†Minimum load −10 mA

FIGURE 7. Adjusting Multiple On-Card Regulators with Single Control*

Applications (Continued)



*0 8Ω ≤ R1 ≤ 120Ω

FIGURE 8. Precision Current Limiter

feedback is taken from the output through R3, making the circuit oscillate. Capacitor C3 acts as a speed-up, increasing switching speed, while R2 limits the peak drive current to Q1.

The circuit in *Figure 9* provides no protection for Q1 in case of an overload. A blow-out proof switching regulator is shown in *Figure 10*. The PNP transistor has been replaced by a PNP-NPN combination with LM395's used as the NPN transistors. The LM395 is an IC which acts as an NPN transistor with overload protection. Included on the LM395 are current limiting, safe-area protection and thermal overload protection making the device virtually immune to any type of overload.

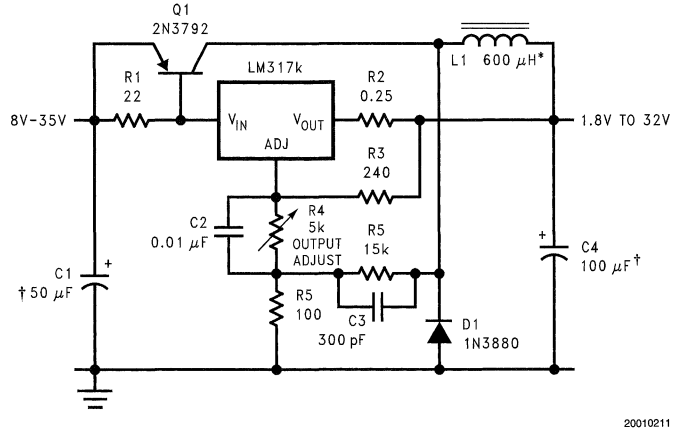
Efficiency for the regulators ranges from 65% to 85%, depending on output voltage. At low output voltages, fixed power losses are a greater percentage of the total output power so efficiency is lowest. Operating frequency is about 30 kHz and ripple is about 150 mV, depending upon input voltage. Load regulation is about 50 mV and line regulation about 1% for a 10V input change.

One of the more unique applications for these switching regulators is as a tracking pre-regulator. The only DC connection to ground on either regulator is through the 100Ω resistor (R5 or R8) that sets the hysteresis. Instead of tying this resistor to ground, it can be connected to the output of a linear regulator so that the switching regulator maintains a constant input-to-output differential on the linear regulator. The switching regulator would typically be set to hold the input voltage to the linear regulator about 3V higher than the output.

Battery charging is another application uniquely suited for the LM117. Since battery voltage is dependent on electro-chemical reactions, the charger must be designed specifically for the battery type and number of cells. Ni-Cads are easily charged with the constant current sources shown previously. For float chargers on lead-acid type batteries all that is necessary is to set the output of the LM117 at the float voltage and connect it to the battery. An adjustable regulator is mandatory since, for long battery life the float voltage must be precisely controlled. The output voltage temperature coefficient can be matched to the battery by inserting diodes in series with the adjustment resistor for the regulator and coupling the diodes to the battery.

A high performance charger for gelled electrolite lead-acid batteries is shown in *Figure 11*. This charger is designed to quickly recharge a battery and shut off at full charge.

Initially, the charging current is limited to 2A by the internal current limit of the LM117. As the battery voltage rises, current to the battery decreases and when the current has decreased to 150 mA, the charger switches to a lower float voltage preventing overcharge. With a discharged battery, the start switch is not needed since the charger will start by itself; however, it is included to allow topping off even slightly discharged batteries.

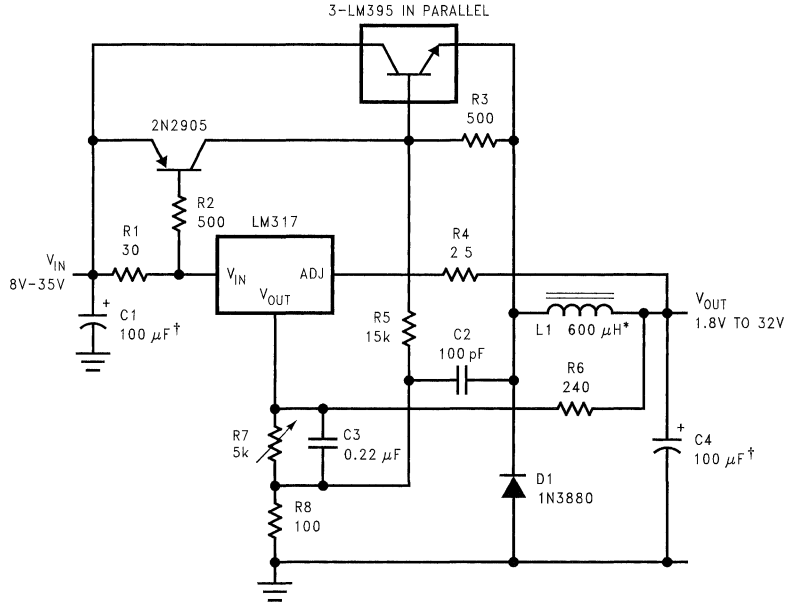


†Solid tantalum

*Core — Arnold A-254168-2 60 turns

FIGURE 9. Low Cost 3A Switching Regulator

Applications (Continued)



†Solid tantalum

*Core — Arnold A-254168-2 60 turns

FIGURE 10. 4A Switching Regulator with Overload Protection

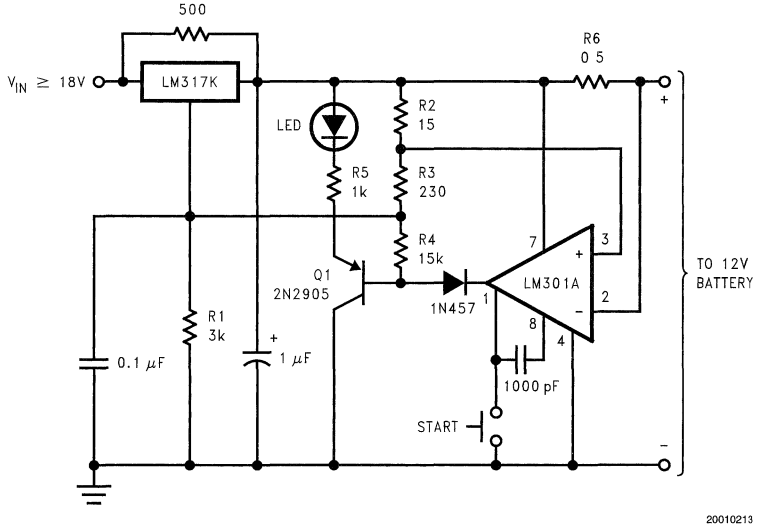


FIGURE 11. 12V Battery Charger

Applications (Continued)

When the start switch is pushed, the output of the charger goes to 14.5V set by R1, R2 and R3. Output current is sensed across R6 and compared to a fraction of the 1.2V reference (across R2) by an LM301A op amp. As the voltage across R8 decreases below the voltage across R2, the output of the LM301A goes low shunting R1 with R4. This decreases the output voltage from 14.5V to about 12.5V terminating the charging. Transistor Q1 then lights the LED as a visual indication of full charge.

The LM117 can even be used as a peak clipping AC voltage regulator. Two regulators are used, 1 for each polarity of the input as shown in *Figure 12*, internal to the LM117 is a diode from input-to-output which conducts the current around the device when the opposite regulator is active. Since each regulator is operating independently, the positive and negative peaks must be set separately for a symmetrical output.

Conclusions

A new IC power voltage regulator has been developed which is significantly more versatile than older devices. The output voltage is adjustable, in addition to improved regulation specifications. Further, reliability is increased in 2 fashions. Overload protection circuitry has been improved to make the device less susceptable to fault conditions and under short circuit conditions, minimum stress is transmitted back to the input power supply. Secondly, the device is 100% burned-in under short circuit conditions at the time of manufacture. Finally, the LM117 is made with a standard IC production process and packaged in a standard TO-3 power package, keeping costs low.

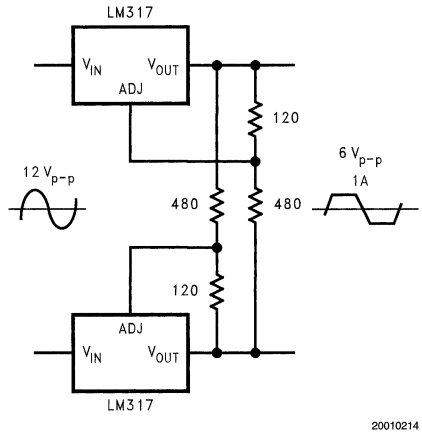


FIGURE 12. AC Voltage Regulator

LM628 Programming Guide

National Semiconductor
Application Note 693
Steven Hunt

Introduction

The LM628/LM629 are dedicated motion control processors Both devices control DC and brushless DC servo motors, as well as, other servomechanisms that provide a quadrature incremental feedback signal Block diagrams of typical LM628/LM629-based motor control systems are shown in *Figures 1, 2.*

As indicated in the figures, the LM628/LM629 are bus peripherals; both devices must be programmed by a host processor. This application note is intended to present a concrete starting point for programmers of these precision motion controllers. It focuses on the development of short programs that test overall system functionality and lay the groundwork for more complex programs. It also presents a method for tuning the loop-compensation PID filter. (Note 1)

Reference System

Figure 15 is a detailed schematic of a closed-loop motor control system. All programs presented in this paper were developed using this system. For application of the programs in other LM628-based systems, changes in basic programming structure are not required, but modification of filter coefficients and trajectory parameters may be required.

I. Program Modules

Breaking programs for the LM628 into sets of functional blocks simplifies the programming process; each block executes a specific task. This section contains examples of the principal building blocks (modules) of programs for the LM628.

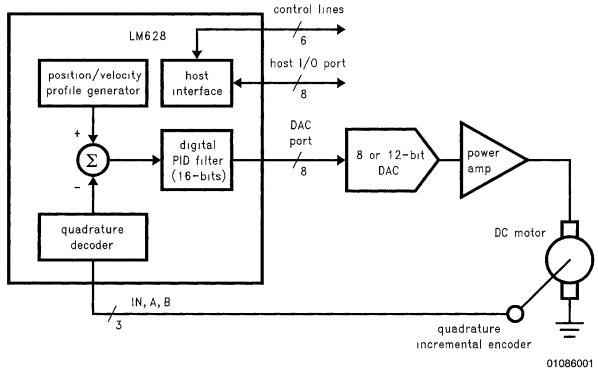


FIGURE 1. LM628-Based Motor Control System

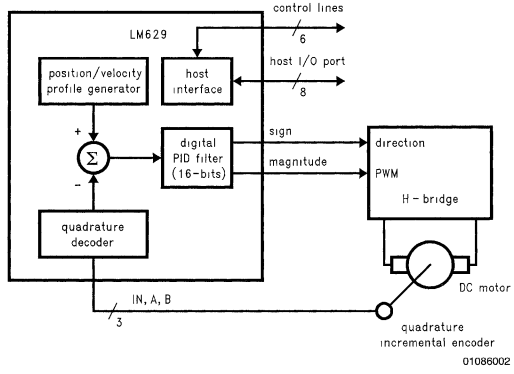


FIGURE 2. LM629-Based Motor Control System

Note 1: For the remainder of this paper, all statements about the LM628 also apply to the LM629 unless otherwise noted

I. Program Modules (Continued)

BUSY-BIT CHECK MODULE

The first module required for successful programming of the LM628 is a busy-bit check module.

The busy-bit, bit zero of the status byte, is set immediately after the host writes a command byte, or reads or writes the second byte of a data word. See *Figure 5.* While the busy-bit is set, the LM628 will ignore any commands or attempts to transfer data.

A busy-bit check module that polls the Status Byte and waits until the busy-bit is reset will ensure successful host/LM628 communications. ***It must be inserted after a command write, or a read or write of the second byte of a data word.*** *Figure 3* represents such a busy-bit check module. This module will be used throughout subsequent modules and programs.

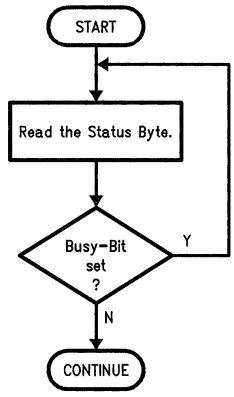


FIGURE 3. Busy-bit Check Module

Reading the Status Byte is accomplished by executing a RDSTAT command. RDSTAT is directly supported by LM628 hardware and is executed by pulling $\overline{CS}$, $\overline{PS}$, and $\overline{RD}$ logic low.

INITIALIZATION MODULE

In general, an initialization module contains a reset command and other initialization, interrupt control, and data reporting commands.

The example initialization module, detailed in *Table 1*, contains a hardware reset block and a PORT 12 command.

Hardware Reset Block

Immediately following power-up, a hardware reset ***must*** *be* executed. Hardware reset is initiated by strobing $\overline{RST}$ (pin 27) logic low for *a* ***minimum of eight LM628 clock periods.***

The reset routine begins after $\overline{RST}$ is returned to logic high. During the reset execution time, **1.5 ms** maximum, the LM628 will ignore any commands or attempts to transfer data.

A hardware reset forces the LM628 into the state described in what follows.

1. The derivative sampling coefficient, d_S, is set to one, and all other filter coefficients and filter coefficient input buffers are set to zero. With d_S set to one, the derivative sampling interval is set to $2048/f_{CLK}$.
2. All trajectory parameters and trajectory parameters input buffers are set to zero.
3. The current absolute position of the shaft is set to zero ("home").
4. The breakpoint interrupt is masked (disabled), and the remaining five interrupts are unmasked (enabled).
5. The position error threshold is set to its maximum value, 7FFF hex.
6. The DAC output port is set for an 8-bit DAC interface.

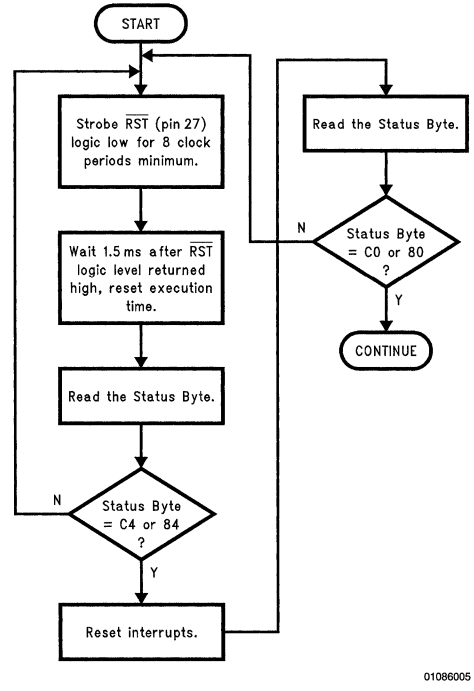


FIGURE 4. Hardware Reset Block

Figure 4 illustrates a hardware reset block that includes an LM628 functionality test. This test *should be* completed immediately following all hardware resets.

I. Program Modules (Continued)

Reset Interrupts

TABLE 1. Initialization Module (with Hardware Reset)

Port	Bytes	Command	Comments
	(Note 5)	hardware reset	Strobe $\overline{RST}$, pin 27, logic low for eight clock periods minimum.
		wait	The maximum time to complete hardware reset tasks is 1.5 ms. During this reset execution time, the LM628 will ignore any commands or attempts to transfer data.
c (Note 2)	xx (Note 3)	RDSTAT	This command reads the status byte. It is directly supported by LM628 hardware and can be executed at any time by pulling $\overline{CS}$, $\overline{PS}$, and $\overline{RD}$ logic low. Status information remains valid as long as $\overline{RD}$ is logic low.
		decision	If the status byte is C4 hex or 84 hex, continue. Otherwise loop back to hardware reset.
c	1D	RSTI	This command resets *only* the interrupts indicated by zeros in bits one through six of the next data word. It also resets bit fifteen of the Signals Register and the host interrupt output pin (pin 17).
Busy-bit Check Module			
d	xx	HB (Note 4)	don't care
d	00	LB	Zeros in bits one through six indicate *all* interrupts will be reset.
Busy-bit Check Module			
c	xx	RDSTAT	This command reads the status byte.
		decision	If the status byte is C0 hex or 80 hex, continue Otherwise loop back to hardware reset.
c	06	PORT12	The reset default size of the DAC port is eight bits. This command initializes the DAC port for a 12-bit DAC. It should not be issued in systems with an 8-bit DAC.
Busy-bit Check Module			

Note 2: The 8-bit host I/O port is a dual-mode port, it operates in command or data mode The logic level at $\overline{PS}$ (pin 16) selects the mode Port c represents the LM628 command port-commands are written to the command port and the Status Byte is read from the command port A logic level of "0" at $\overline{PS}$ selects the command port Port d represents the LM628 data port— data is both written to and read from the data port A logic level of "1" at $\overline{PS}$ selects the data port

Note 3: x - don't care

Note 4: HB - high byte, LB - low byte

Note 5: All values represented in hex

An RSTI command sequence allows the user to reset the interrupt flag bits, bits one through six of the status byte. See *Figure 5.* It contains an RSTI command and one data word.

The RSTI command initiates resetting the interrupt flag bits. Command RSTI also resets the host interrupt output pin (pin 17).

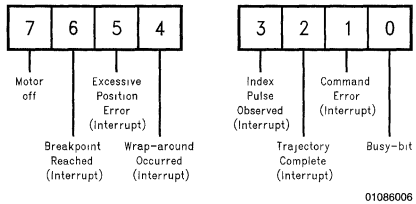


FIGURE 5. Status Byte Bit Allocation

Immediately following the RSTI command, a single data word is written. The first byte is not used. Logical zeros in bits one through six of the second byte reset the corresponding interrupts. See *Figure 6.* Any combination of the interrupt flag bits can be reset within a single RSTI command sequence. This feature allows interrupts to be serviced according to a user-programmed priority.

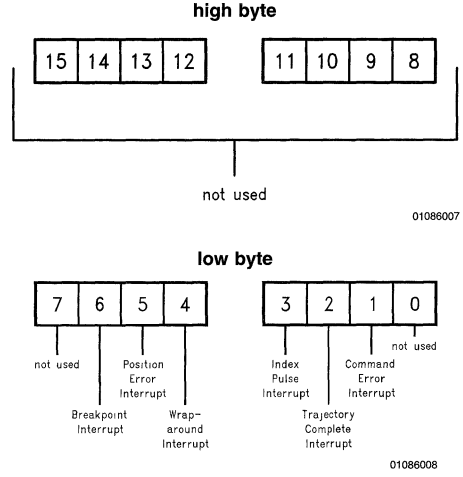


FIGURE 6. Interrupt Mask/Reset Bit Allocations

I. Program Modules (Continued)

In the case of the example module, the second byte of the RSTI data word, 00 hex, resets *all* interrupt flag bits. See *Table 1.*

DAC Port Size

During both hardware and software resets, the DAC output port defaults to 8-bit mode. If an LM628 control loop utilizes a 12-bit DAC, command PORT12 should be issued immediately following the hardware reset block and all subsequent resets. Failure to issue command PORT12 will result in erratic, unpredictable motor behavior.

If the control loop utilizes an 8-bit DAC, command PORT12 must not be executed; this too will result in erratic, unpredictable motor behavior.

An LM629 will ignore command PORT8 (as it provides an 8-bit sign/magnitude PWM output). Command PORT12 *should not* be issued in LM629-based systems.

Software Reset Considerations

After the initial hardware reset, resets can be accomplished with either a hardware reset or command RESET (software reset). Software and hardware resets execute the same tasks (Note 6) and require the same execution time, 1.5 ms maximum. During software reset execution, the LM628 will ignore any commands or attempts to transfer data.

The hardware reset module includes an LM628 functionality test. This test is ***not*** required after a software reset.

Table 2 details an initialization module that uses a software reset.

Note 6: In the case of a software reset, the position error threshold remains at its pre-reset value

TABLE 2. Initialization Module (with Software Reset)

Port	Bytes	Command	Comments
c	00	RESET	See Initialization Module text.
		wait	The maximum time to complete RESET tasks is 1.5 ms.
c	06	PORT12	The RESET default size of the DAC port is eight bits. This command initializes the DAC port for a 12-bit DAC. It should not be issued in a system with an 8-bit DAC.
Busy-bit Check Module			
c	1D	RSTI	This command resets *only* the interrupts indicated by zeros in bits one through six of the next data word. It also resets bit fifteen of the Signals Register and (pin 17) the host interrupt output pin.
Busy-bit Check Module			
d	xx	HB	Don't care
d	00	LB	Zeros in bits one through six indicate *all* interrupts will be reset.
Busy-bit Check Module			

Comments

Figure 7 illustrates, in simplified block diagram form, the LM628. The profile generator provides the control loop input, desired shaft position. The quadrature decoder provides the control loop feedback signal, actual shaft position. At the first summing junction, actual position is subtracted from desired position to generate the control loop error signal, position error. This error signal is filtered by the PID filter to provide the motor drive signal.

After executing the example initialization module, the following observations are made. With the integration limit term (i_L) and the filter gain coefficients (k_p, k_i, and k_d) initialized to zero, the filter gain is zero. Moreover, after a reset, desired shaft position tracks actual shaft position. Under these conditions, the motor drive signal is zero. The control system can not affect shaft position. The shaft should be stationary and "free wheeling". If there is significant drive amplifier offset, the shaft may rotate slowly, but with minimal torque capability.

Note: Regardless of the free wheeling state of the shaft, the LM628 continuously tracks shaft absolute position

I. Program Modules (Continued)

FILTER PROGRAMMING MODULE

The example filter programming module is shown in *Table 4*.

Load Filter Parameters (Coefficients)

An LFIL (Load FILter) command sequence includes command LFIL, a filter control word, and a variable number of data words.

The LFIL command initiates loading filter coefficients into input buffers.

The two data bytes, written immediately after LFIL, comprise the filter control word. The first byte programs the derivative sampling coefficient, d_s (i.e selects the derivative sampling interval). The second byte indicates, with logical ones in respective bit positions, which of the remaining four filter coefficients will be loaded. See *Figure 8*,*Table 3*. Any combination of the four coefficients can be loaded within a single LFIL command sequence

Immediately following the filter control word, the filter coefficients are written. Each coefficient is written as a pair of data bytes, a data word. Because any combination of the four coefficients can be loaded within a single LFIL command sequence, the number of data words following the filter control word can vary in the range from zero to four.

In the case of the example module, the first byte of the filter control word, 00 hex, programs a derivative sampling coefficient of one. The second byte, x8 hex, indicates only the proportional gain coefficient will be loaded.

Immediately following the filter control word, the proportional gain coefficent is written. In this example, k_p is set to ten with the data word 000A hex. The other three filter coefficients remain at zero, their reset value.

Update Filter

The update filter command, UDF, transfers new filter coefficients from input buffers to working registers. Until UDF is executed, the new filter coefficients do not affect the transfer characteristic of the filter.

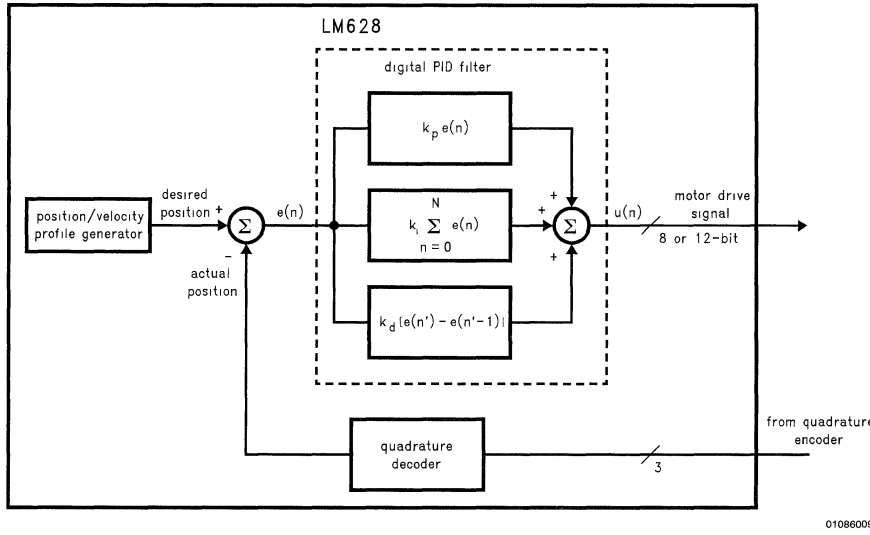


FIGURE 7. LM628—Simplified Block Diagram Form

I. Program Modules (Continued)

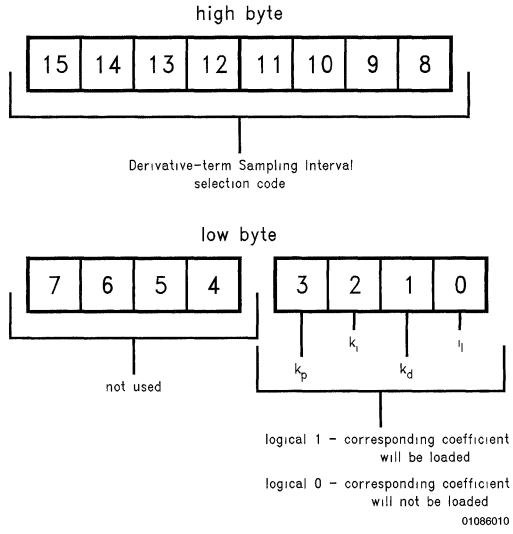


FIGURE 8. Filter Control Word Bit Allocation

TABLE 3. Derivative—Term Sampling Interval Selection Codes

Filter Control Word Bit Position								d_s	Selected Derivative-Term Sampling Interval—T_d
15	14	13	12	11	10	9	8		
0	0	0	0	0	0	0	0	1	T_s
0	0	0	0	0	0	0	1	2	$2T_s$
0	0	0	0	0	0	1	0	3	$3T_s$
0	0	0	0	0	0	1	1	4	$4T_s$
			•					•	•
			•					•	•
			•					•	•
1	1	1	1	1	1	1	1	256	$256T_s$

$T_s = (2048) \times \left(\frac{1}{f_{CLK}}\right)$ System Sample Period

$T_d = d_s \times T_s$ Derivative-term Sampling Interval

I. Program Modules (Continued)

TABLE 4. Filter Programming Module

Port	Bytes	Command	Comments
c	1E	LFIL	This command initiates loading the filter coefficients input buffers.
			Busy-bit Check Module
d d	00 x8	HB LB	These two bytes are the filter control word. A 00 hex HB sets the derivative sampling interval to $2048/f_{CLK}$ by setting d_s to one. A x8 hex LB indicates only k_p will be loaded. The other filter parameters will remain at zero, their reset default value.
			Busy-bit Check Module
d d	00 0A	HB LB	These two bytes set k_p to ten.
			Busy-bit Check Module
c	04	UDF	This command transfers new filter coefficients from input buffers to working registers. Until UDF is executed, coefficients loaded via the LFIL command do not affect the filter transfer characteristic.
			Busy-bit Check Module

Comments

After executing both the example initialization and example filter programming modules, the following observations are made. Filter gain is nonzero, but desired shaft position continues to track actual shaft position. Under these conditions, the motor drive signal remains at zero. The shaft should be stationary and "free wheeling". If there is significant drive amplifier offset, the shaft may rotate slowly, but with minimal torque capability.

Initially, k_p should be set below twenty, d_s should be set to one, and k_i, k_d, and i_i should remain at zero. These values will not provide optimum system performance, but they will be sufficient to test system functionality. See Tuning the PID Filter.

TRAJECTORY PROGRAMMING MODULE

Table 5 details the example trajectory programming module.

Load Trajectory Parameters

An LTRJ (Load TRaJectory) command sequence includes command LTRJ, a trajectory control word, and a variable number of data words.

The LTRJ command initiates loading trajectory parameters into input buffers.

The two data bytes, written immediately after LTRJ, comprise the trajectory control word. The first byte programs, with logical ones in respective bit positions, the trajectory mode (velocity or position), velocity mode direction, and stopping mode. See Stop Module. The second byte indicates, with logical ones in respective bit positions, which of the three trajectory parameters will be loaded. It also indicates whether the parameters are absolute or relative. See *Figure 9*. Any combination of the three parameters can be loaded within a single LTRJ command sequence.

Immediately following the trajectory control word, the trajectory parameters are written. Each parameter is written as a pair of data words (four data bytes). Because any combination of the three parameters can be loaded within a single LTRJ command sequence, the number of data words following the trajectory control word can vary in the range from zero to six.

In the case of the example module, the first byte of the trajectory control word, 00 hex, programs the LM628 to operate in position mode. The second byte, 0A hex, indicates velocity and position will be loaded and both parameters are absolute. Four data words, two for each parameter loaded, follow the trajectory control word.

Start Motion Control

The start motion control command, STT (STarT), transfers new trajectory parameters from input buffers to working registers and begins execution of the new trajectory. Until STT is executed, the new trajectory parameters do not affect shaft motion.

Note: At this point no actual trajectory parameters are loaded. Calculation of trajectory parameters and execution of example moves is left for a later section.

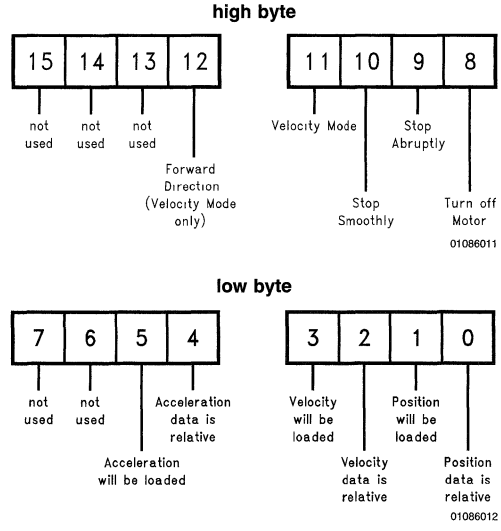


FIGURE 9. Trajectory Control Word Bit Allocation

I. Program Modules (Continued)

TABLE 5. Trajectory Programming Module

Port	Bytes	Command	Comments
c	1F	LTRJ	This command initiates loading the trajectory parameters input buffers.
			Busy-bit Check Module
d	00	HB	These two bytes are the trajectory control word. A 0A hex LB indicates velocity and
d	0A	LB	position will be loaded and both parameters are absolute.
			Busy-bit Check Module
d	xx	HB	Velocity is loaded in two data words. These two bytes are the high data word.
d	xx	LB	
			Busy-bit Check Module
d	xx	HB	velocity data word (low)
d	xx	LB	
			Busy-bit Check Module
d	xx	HB	Position is loaded in two data words. These two bytes are the high data word.
d	xx	LB	
			Busy-bit Check Module
d	xx	HB	position data word (low)
d	xx	LB	
			Busy-bit Check Module
c	01	STT	STT must be issued to execute the desired trajectory.
			Busy-bit Check Module

STOP MODULE

This module demonstrates the programming flow required to stop shaft motion.

While the LM628 operates in position mode, normal stopping is always smooth and occurs automatically at the end of a specified trajectory (i.e. no stop module is required). Under exceptional conditions, however, a stop module can be used to affect a premature stop.

While the LM628 operates in velocity mode, stopping is always accomplished via a stop module.

The example stop module, shown in *Table 5*, utilizes an LTRJ command sequence and an STT command.

Load Trajectory Parameters

Bits eight through ten of the trajectory control word select the stopping mode. See *Figure 9*.

In the case of the example module, the first byte of the trajectory control word, x1 hex, selects motor-off as the desired stopping mode. This mode stops shaft motion by setting the motor drive signal to zero (the appropriate offset-binary code to apply zero drive to the motor).

Setting bit nine of the trajectory control word selects stop abruptly as the desired stopping mode. This mode stops shaft motion (at maximum deceleration) by setting the target position equal to the current position.

Setting bit ten of the trajectory control word selects stop smoothly as the desired stopping mode. This mode stops shaft motion by decelerating at the current user-programmed acceleration rate.

Note: Bits eight through ten of the trajectory control word must be used exclusively, only one of them should be logic one at any time.

Start Motion Control

The start motion control command, STT, must be executed to stop shaft motion.

Comments

After shaft motion is stopped with either an "abrupt" or a "smooth" stop module, the control system will attempt to hold the shaft at its current position. If forced away from this desired resting position and released, the shaft will move back to the desired position. Unless new trajectory parameters are loaded, execution of another STT command will restart the specified move.

After shaft motion is stopped with a "motor-off" stop module, desired shaft position tracks actual shaft position. Consequently, the motor drive signal remains at zero and the control system can not affect shaft position; the shaft should be stationary and free wheeling. If there is significant drive amplifier offset, the shaft may rotate slowly, but with minimal torque capability. Unless new trajectory parameters are loaded, execution of another STT command will restart the specified move.

I. Program Modules (Continued)

TABLE 6. Stop Module (Motor-Off)

Port	Bytes	Command	Comments
c	1F	LTRJ	This command initiates loading the trajectory parameters input buffers.
			Busy-bit Check Module
d	x1	HB	These two bytes are the trajectory control word. A x1 hex HB selects motor-off as the
d	00	LB	desired stopping mode. A 00 hex LB indicates no trajectory parameters will be loaded.
			Busy-bit Check Module
c	01	STT	The start motion control command, STT, must be executed to stop shaft motion.
			Busy-bit Check Module

II. Programs

This section focuses on the development of four brief LM628 programs.

LOOP PHASING PROGRAM

Following initial power-up, the correct polarity of the motor drive signal must be determined. If the polarity is incorrect (loop inversion), the drive signal will push the shaft away from its desired position rather than towards it This results in "motor runaway", a condition characterized by the motor running continuously at high speed.

The loop phasing program, detailed in *Table 7*, contains both the example initialization and filter programming modules. It also contains an LTRJ command sequence and an STT command.

Note: Execution of this simple program is only required the *first* time a new system is used

Load Trajectory Parameters

An LTRJ (Load TRaJectory) command sequence includes command LTRJ, a trajectory control word, and a variable number of data words.

In the case of the Loop Phasing Program, the first byte of the trajectory control word, 00 hex, programs the LM628 to operate in position mode. The second byte, 00 hex, indicates no trajectory parameters will be loaded (i.e. in this program, zero data words follow the trajectory control word). The three trajectory parameters will remain at zero, their reset value.

Start Motion Control

The start motion control command, STT (STarT), transfers new trajectory parameters from input buffers to working registers and begins execution of the new trajectory. Until STT is executed, the new trajectory parameters do not affect shaft motion.

TABLE 7. Loop Phasing Program

Port	Bytes	Command	Comments
			Initialization Module
			Filter Programming Module
c	1F	LTRJ	This command initiates loading the trajectory parameters input buffers.
			Busy-bit Check Module
d	00	HB	These two bytes are the trajectory control word. A 00 hex LB indicates no trajectory
d	00	LB	parameters will be loaded
			Busy-bit Check Module
c	01	STT	STT must be issued to execute the desired trajectory.

Comments

Execution of command STT results in execution of the desired trajectory. With the acceleration set at zero, the profile generator generates a desired shaft position that is both constant and equal to the current absolute position. See *Figure 7*. Under these conditions, the control system will attempt to hold the shaft at its current absolute postion. The shaft will feel lightly "spring loaded". If forced (CAREFULLY) away from its desired position and released, the shaft will spring back to the desired position.

If the polarity of the motor drive signal is incorrect (loop inversion), motor runaway will occur immediately after execution of command STT, or after the shaft is forced (CAREFULLY) from its resting position.

Loop inversion can be corrected with one of three methods: interchanging the shaft position encoder signals (channel A and channel B), interchanging the motor power leads, or inverting the motor command signal before application to the motor drive amplifier. For LM629 based systems, loop inversion can be corrected by interchanging the motor power leads, interchanging the shaft position encoder signals, or logically inverting the PWM sign signal.

SIMPLE ABSOLUTE POSITION MOVE

The Simple Absolute Position Move Program, detailed in *Table 8*, utilizes both the initialization and filter programming modules, as well as, an LTRJ command sequence and an STT command.

Factors that influenced the development of this program included the following: the program must demonstrate simple trajectory parameters calculations, the program must demonstrate the programming flow required to load and execute an absolute position move, and correct completion of the move must be verifiable through simple observation.

Move: The shaft will accelerate at 0.1 rev/sec^2 until it reaches a maximum velocity of 0.2 rev/sec, and then decelerate to a stop exactly two revolutions from the starting position. See *Figure 10*.

II. Programs (Continued)

Note: Absolute position is position measured relative to zero (home) An absolute position move is a move that ends at a specified absolute position For example, independent of the current absolute position of the shaft, if an absolute position of 30,000 counts is specified, upon completion of the move the absolute position of the shaft will be 30,000 counts (i.e 30,000 counts relative to zero) The example program calls for a position move of two revolutions Because the starting absolute position is 0 counts, the move is accomplished by specifying an absolute position of 8000 counts See *Table 8*

The Quadrature Incremental Encoder

As a supplement to the trajectory parameters calculations, a brief discussion is provided here to differentiate between encoder ***lines*** and encoder ***counts***.

A quadrature incremental shaft encoder encodes shaft rotation as electrical pulses. *Figure 11* details the signals generated by a 3-channel quadrature incremental encoder. The LM628 decodes (or "counts") a quadrature incremental signal to determine the absolute position of the shaft.

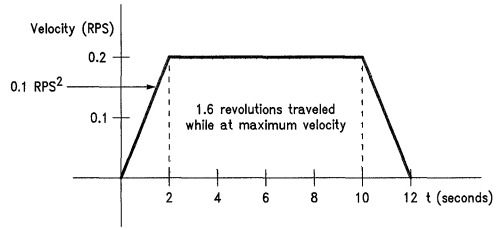


FIGURE 10. Velocity Profile for Simple Absolute Position Move Program

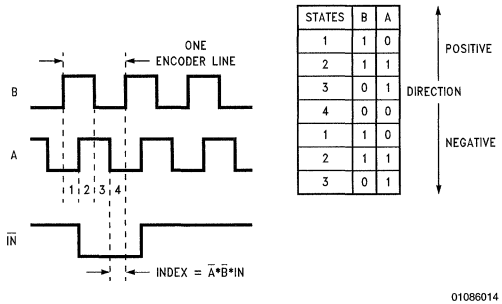


FIGURE 11. 3-Channel Quadrature Encoder Signals

The resolution of a quadrature incremental encoder is usually specified as a number of ***lines***. This number indicates the number of cycles of the output signals for each complete shaft revolution. For example, an N-line encoder generates N cycles of its output signals during each complete shaft revolution.

By definition, two signals that are in quadrature are 90° out of phase. When considered together, channels A and B (*Figure 11*) traverse four distinct digital states during each full cycle of either channel. Each state transition represents one ***count*** of shaft motion. The leading channel indicates the direction of shaft rotation.

Each line, therefore, represents one cycle of the output signals, and each cycle represents four encoder counts.

$$\left(N\frac{\text{CYCLES}}{\text{REVOLUTION}}\right)\times\left(4\frac{\text{COUNTS}}{\text{CYCLE}}\right)=4N\frac{\text{COUNTS}}{\text{REVOLUTION}}$$

The reference system uses a one thousand line encoder.

$$\left(1000\frac{\text{CYCLES}}{\text{REVOLUTION}}\right)\times\left(4\frac{\text{COUNTS}}{\text{CYCLE}}\right)=4000\frac{\text{COUNTS}}{\text{REVOLUTION}}$$

Sample Period

Sampling of actual shaft position occurs at a fixed frequency, the reciprocal of which is the system sample period. The system sample period is the unit of time upon which shaft acceleration and velocity are based.

$$T_S = (2048)\times\left(\frac{1}{f_{CLOCK}}\right)\ \text{System Sample Period}$$

The reference system uses an 8 MHz clock. The sample period of the reference system follows directly from the definition.

$$T_S = (2048)\times\left(\frac{1}{8\times10^6\ \text{Hz}}\right) = 256\times10^{-6}\frac{\text{SECONDS}}{\text{SAMPLE}}$$

Trajectory Parameters Calculations

The shaft will accelerate at 0.1 rev/sec^2 until it reaches a maximum velocity of 0.2 rev/sec, and then decelerate to a stop exactly two revolutions from the starting position.

Trajectory parameters calculations for this move are detailed in *Figure 12.*

Comments

After completing the move, the control system will attempt to hold the shaft at its current absolute position. The shaft will feel lightly "spring loaded". If forced away from its desired resting position and released, the shaft will move back to the desired position.

II. Programs (Continued)

$$A = \left(4000 \frac{\text{COUNTS}}{\text{REVOLUTION}}\right) \times \left(256 \times 10^{-6} \frac{\text{SECONDS}}{\text{SAMPLE}}\right)^2 \times \left(0.1 \frac{\text{REVOLUTIONS}}{\text{SECOND}^2}\right) = 2.62 \times 10^{-5} \frac{\text{COUNTS}}{\text{SAMPLE}^2}$$

$$A = \left(2.62 \times 10^{-5} \frac{\text{COUNTS}}{\text{SAMPLE}^2}\right) \times (65{,}536) = 1.718 \frac{\text{COUNTS}}{\text{SAMPLE}^2} \quad \text{Acceleration Scaled}$$

$$A = 2 \frac{\text{COUNTS}}{\text{SAMPLE}^2} \quad \text{Acceleration Rounded}$$

$$A = 00\ 00\ 00\ 02 \text{ hex} \frac{\text{COUNTS}}{\text{SAMPLE}^2}$$

$$V = \left(4000 \frac{\text{COUNTS}}{\text{REVOLUTION}}\right) \times \left(256 \times 10^{-6} \frac{\text{SECONDS}}{\text{SAMPLE}}\right) \times \left(0.2 \frac{\text{REVOLUTIONS}}{\text{SECOND}}\right) = 0.2048 \frac{\text{COUNTS}}{\text{SAMPLE}}$$

$$V = \left(0.2048 \frac{\text{COUNTS}}{\text{SAMPLE}}\right) \times (65{,}536) = 13{,}421.77 \frac{\text{COUNTS}}{\text{SAMPLE}} \quad \text{Velocity Scaled}$$

$$V = 13{,}422 \frac{\text{COUNTS}}{\text{SAMPLE}} \quad \text{Velocity Rounded}$$

$$V = 00\ 00\ 34\ 6E \text{ hex} \frac{\text{COUNTS}}{\text{SAMPLE}}$$

$$P = \left(4000 \frac{\text{COUNTS}}{\text{REVOLUTION}}\right) \times (2.0 \text{ REVOLUTIONS}) = 8000 \text{ COUNTS}$$

$$P = 00\ 00\ 1F\ 40 \text{ hex COUNTS}$$

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FIGURE 12. Calculations of Trajectory Parameters for Simple Absolute Position Move

II. Programs (Continued)

TABLE 8. Simple Absolute Position Move Program

Port	Bytes	Command	Comments
			Initialization Module
			Filter Programming Module
c	1F	LTRJ	This command initiates loading the trajectory parameters input buffers
			Busy-bit Check Module
d	00	HB	These two bytes are the trajectory control word. A 2A hex LB indicates acceleration,
d	2A	LB	velocity, and position will be loaded and all three parameters are absolute.
d	00	HB	Acceleration is loaded in two data words. These two bytes are the high data word. In
d	00	LB	this case, the acceleration is 0.1 rev/sec^2.
			Busy-bit Check Module
d	00	HB	acceleration data word (low)
d	02	LB	
d	00	HB	velocity is loaded in two data words. These two bytes are the high data word. In this
d	00	LB	case, the velocity is 0.2 rev/sec.
			Busy-bit Check Module
d	34	HB	velocity data word (low)
d	6E	LB	
			Busy-bit Check Module
d	00	HB	Position is loaded in two data words. These two bytes are the high data word. In this
d	00	LB	case, the position loaded is eight thousand counts. This results in a move of two
			revolutions in the forward direction.
			Busy-bit Check Module
d	1F	HB	position data word (low)
d	40	LB	
			Busy-bit Check Module
c	01	STT	STT must be issued to execute the desired trajectory.

SIMPLE RELATIVE POSITION MOVE

This program demonstrates the programming flow required to load and execute a relative position move. See *Table 9.*

Move: Independent of the current resting position of the shaft, the shaft will complete thirty revolutions in the reverse direction. Total time to complete the move is fifteen seconds. Total time for acceleration and deceleration is five seconds.

Note: Target position is the final requested position If the shaft is stationary, and motion has not been stopped with a "motor-off" stop module, the current absolute position of the shaft is the target position If motion has been stopped with a "motor-off" stop module, or a position move has begun, the absolute position that corresponds to the endpoint of the current trajectory is the target position Relative position is position measured relative to the current target position of the shaft. A relative position move is a move that ends the specified "relative" number of counts away from the current target position of the shaft For example, if the current target position of the shaft is 10 counts, and a relative position of 30,000 counts is specified, upon completion of the move the absolute position of the shaft will be 30,010 counts (i e 30,000 counts relative to 10 counts)

Load Trajectory Parameters

The first byte of the trajectory control word, 00 hex, programs position mode operation. The second byte, 2B hex, indicates all three trajectory parameters will be loaded. It also indicates both acceleration and velocity will be absolute values while position will be a relative value.

Trajectory Parameters Calculations

Independent of the current resting position of the shaft, the shaft will complete thirty revolutions in the reverse direction. Total time to complete the move is fifteen seconds. Total time for acceleration and deceleration is five seconds.

The reference system utilizes a one thousand line encoder. The number of counts for each complete shaft revolution and the total counts for this position move are determined.

$$\left(1000\ \frac{\text{CYCLES}}{\text{REVOLUTION}}\right)\times\left(4\ \frac{\text{COUNTS}}{\text{CYCLE}}\right)=4000\ \frac{\text{COUNTS}}{\text{REVOLUTION}}$$

$$\left(4000\ \frac{\text{COUNTS}}{\text{REVOLUTION}}\right)\times(30\ \text{REVOLUTIONS})=120{,}000\ \text{COUNTS}$$

With respect to time, two-thirds of the move is made at maximum velocity and one-third is made at a velocity equal to one-half the maximum velocity (Note 7). Therefore, total counts traveled during acceleration and deceleration periods is one-fifth the total counts traveled. See *Figure 13.*

II. Programs (Continued)

$$\frac{120{,}000\ \text{COUNTS}}{5} = 24{,}000\ \text{COUNTS}$$ total counts traveled during acceleration and deceleration

$$\frac{24{,}000\ \text{COUNTS}}{2} = 12{,}000\ \text{COUNTS}$$ counts traveled during acceleration

The reference system uses an 8 MHz clock. The sample period of the reference system is determined.

$$T_S = (2048) \times \left(\frac{1}{8 \times 10^6 \text{Hz}}\right) = 256 \times 10^{-6} \frac{\text{SECONDS}}{\text{SAMPLE}}$$

The number of samples during acceleration (and deceleration) is determined.

$$\frac{2.5\ \text{SECONDS}}{256 \times 10^{-6} \frac{\text{SECONDS}}{\text{SAMPLE}}} = 9766\ \text{SAMPLES}$$ number of samples during acceleration

Using the number of counts traveled during acceleration and the number of samples during acceleration, acceleration is determined.

$$s = \frac{at^2}{2}$$ distance traveled during time t at acceleration a

$$a = \frac{2s}{t^2} = \frac{(2) \times (12{,}000\ \text{COUNTS})}{(9766\ \text{SAMPLES})^2} = 0.000252 \frac{\text{COUNTS}}{\text{SAMPLE}^2}$$

Total counts traveled while at maximum velocity is four-fifths the total counts traveled.

$$\frac{(4) \times (120{,}000\ \text{COUNTS})}{5} = 96{,}000\ \text{COUNTS}$$

Note 7: Average velocity during acceleration and deceleration periods is one-half the maximum velocity

TABLE 9. Simple Relative Position Move Program

Port	Bytes	Command	Comments
			Initialization Module
			Filter Programming Module
c	1F	LTRJ	This command initiates loading the trajectory parameters input buffers
			Busy-bit Check Module
d d	00 2B	HB LB	These two bytes are the trajectory control word. A 2B hex LB indicates all three parameters will be loaded and both acceleration and velocity will be absolute values while position will be a relative value.
			Busy-bit Check Module
d d	00 00	HB LB	Acceleration is loaded in two data words. These two bytes are the high data word. In this case, the acceleration is 17 counts/sample^2.
			Busy-bit Check Module
d d	00 11	HB LB	acceleration data word (low)
			Busy-bit Check Module
d d	00 02	HB LB	Velocity is loaded in two data words. These two bytes are the high data word. In this case, velocity is 161,087 counts/sample.
			Busy-bit Check Module
d d	75 3F	HB LB	velocity data word (low)
			Busy-bit Check Module
d d	FF FE	HB LB	Position is loaded in two data words. These two bytes are the high data word. In this case, the position loaded is −120,000 counts. This results in a move of thirty revolutions in the reverse direction.
			Busy-bit Check Module
d d	2B 40	HB LB	position data word (low)
			Busy-bit Check Module
c	01	STT	STT must be issued to execute the desired trajectory.

II. Programs (Continued)

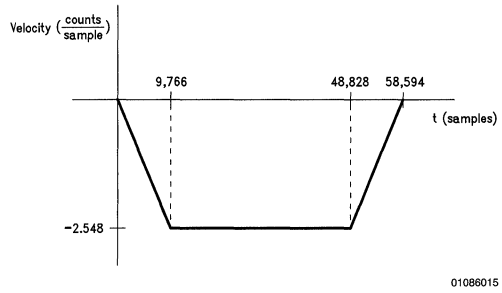


FIGURE 13. Velocity Profile for Simple Relative Position Move Program

The number of samples while at maximum velocity is determined.

$$\frac{10 \text{ SECONDS}}{256 \times 10^{-6} \frac{\text{SECONDS}}{\text{SAMPLE}}} = 39{,}062 \text{ SAMPLES}$$ number of samples while at maximum velocity

Using the total counts traveled while at maximum velocity and the number of samples while at maximum velocity, velocity is determined.

$$\frac{96{,}000 \text{ COUNTS}}{39{,}062 \text{ SAMPLES}} = 2.458 \frac{\text{COUNTS}}{\text{SAMPLE}}$$

Both acceleration and velocity values are scaled.

$$\left(0.000252 \frac{\text{COUNTS}}{\text{SAMPLE}^2}\right) \times (65{,}536) = 16.515 \frac{\text{COUNTS}}{\text{SAMPLE}^2}$$

$$\left(2\,458 \frac{\text{COUNTS}}{\text{SAMPLE}}\right) \times (65{,}536) = 161{,}087\,488 \frac{\text{COUNTS}}{\text{SAMPLE}}$$

Acceleration and velocity are rounded to the nearest integer and all three trajectory parameters are converted to hexadecimal.

$$A = 17 = 00\ 00\ 00\ 11 \text{ hex } \frac{\text{COUNTS}}{\text{SAMPLE}^2}$$

$$V = 161{,}087 = 00\ 02\ 75\ 3F \text{ hex } \frac{\text{COUNTS}}{\text{SAMPLE}}$$

$$P = -120{,}000 = FF\ FE\ 2B\ 40 \text{ hex COUNTS}$$

BASIC VELOCITY MODE MOVE WITH BREAKPOINTS

This program demonstrates basic velocity mode programming and the (typical) programming flow required to set both absolute and relative breakpoints. See *Table 10.*

Move: The shaft will accelerate at 1.0 rev/sec^2 until it reaches a maximum velocity of 2.0 rev/sec. After completing twenty forward direction revolutions (including revolutions during acceleration), the shaft will accelerate at 1.0 rev/sec^2 until it reaches a maximum velocity of 4.0 rev/sec. After completing twenty forward direction revolutions (including revolutions during acceleration), the shaft will decelerate (at 1.0 rev/sec^2) to a stop. See *Figure 14.*

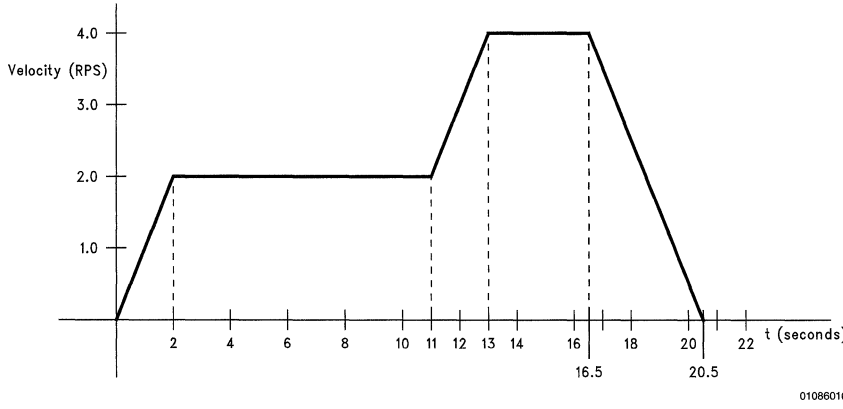


FIGURE 14. Velocity Profile for Basic Velocity Mode with Breakpoints Program

Mask Interrupts

An MSKI command sequence allows the user to determine which interrupt conditions result in host interrupts; interrupting the host via the host interrupt output (pin 17). It contains an MSKI command and one data word.

The MSKI command initiates interrupt masking.

Immediately following the MSKI command, a single data word is written. The first byte is not used. Bits one through six of the second byte determine the masked/unmasked status of each interrupt. See *Figure 6.* Any zeros in this 6-bit field mask (disable) the corresponding interrupts while any ones unmask (enable) the corresponding interrupts.

II. Programs (Continued)

In the case of the examlple program, the second byte of the MSKI data word, 40 hex, enables the breakpoint interrupt. All other interrupts are disabled (masked).

When interrupted, the host processor can read the Status Byte to determine which interrupt condition(s) occurred. See *Figure 5.*

Note: Command MSKI controls only the host interrupt process Bits one through six of the Status Byte reflect actual conditions independent of the masked/unmasked status of individual interrupts This feature allows interrupts to be serviced with a polling scheme

Set Breakpoints (Absolute and Relative)

An SBPA command sequence enables the user to set breakpoints in terms of absolute shaft position. An SBPR command sequence enables setting breakpoints relative to the current target position. When a breakpoint position is reached, bit six of the status byte, the breakpoint interrupt flag, is set to logic high. If this interrupt is enabled (unmasked), the host will be interrupted via the host interrupt output (pin 17).

An SBPA (or SBPR) command initiates loading/setting a breakpoint. The two data words, written immediately following the SBPA (or SBPR) command, represent the breakpoint position.

The example program contains a relative breakpoint set at 80,000 counts relative to position zero (the current target position). This represents a move of twenty forward direction revolutions. When this position is reached, the LM628 interrupts the host processor, and the host executes a sequence of commands that increases the maximum velocity, resets the breakpoint interrupt flag, and loads an absolute breakpoint.

The example program contains an absolute breakpoint set at 160,000 counts. When this absolute position is reached, the LM628 interrupts the host processor, and the host executes a Smooth Stop Module.

Breakpoint positions for this example program are determined

$$\left(4000\ \frac{\text{COUNTS}}{\text{REVOLUTION}}\right) \times (20\ \text{REVOLUTIONS}) = 80{,}000\ \text{COUNTS}_{\text{relative breakpoint}}$$

$$\left(4000\ \frac{\text{COUNTS}}{\text{REVOLUTION}}\right) \times (40\ \text{REVOLUTIONS}) = 160{,}000\ \text{COUNTS}_{\text{absolute breakpoint}}$$

Load Trajectory Parameters

This example program contains two LTRJ command sequences. The trajectory control word of the first LTRJ command sequence, 1828 hex, programs forward direction velocity mode, and indicates an absolute acceleration and an absolute velocity will be loaded. The trajectory control word of the second LTRJ command sequence, 180C hex, programs forward direction velocity mode, and indicates a relative velocity will be loaded. See *Figure 9.*

Trajectory parameters calculations follow the same format as those detailed for the simple absolute position move. See *Figure 12.*

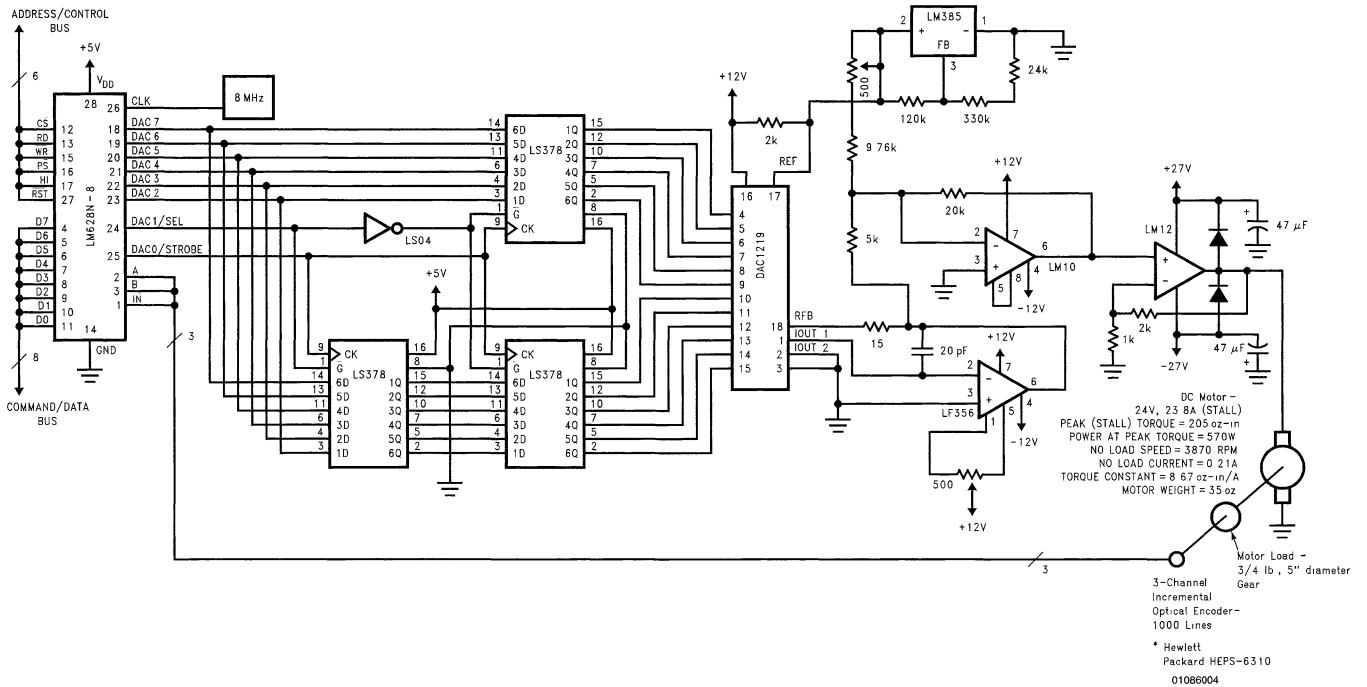
TABLE 10. Basic Velocity Mode Move with Breakpoints Program

Port	Bytes	Command	Comments
			Initialization Module
			Filter Programming Module
c	1C	MSKI	Mask interrupts.
			Busy-bit Check Module
d	xx	HB	don't care
d	40	LB	A 40 hex LB enables (unmasks) the breakpoint interrupt. All other interrupts are disabled (masked).
			Busy-bit Check Module
c	21	SPBR	This command initiates loading a relative breakpoint.
			Busy-bit Check Module
d	00	HB	A breakpoint is loaded in two data words. These two bytes are the high data word. In
d	01	LB	this case, the breakpoint is 80,000 counts relative to the current commanded target position (zero).
			Busy-bit Check Module
d	38	HB	breakpoint data word (low)
d	80	LB	
			Busy-bit Check Module
c	1F	LTRJ	Load trajectory.
			Busy-bit Check Module
d	18	HB	These two bytes are the trajectory control word. A 18 hex HB programs forward
d	28	LB	direction velocity mode operation. A 28 hex LB indicates acceleration and velocity will be loaded and both values are absolute.

II. Programs (Continued)

TABLE 10. Basic Velocity Mode Move with Breakpoints Program (Continued)

Port	Bytes	Command	Comments
			Busy-bit Check Module
d d	00 00	HB LB	Acceleration is loaded in two data words. These two bytes are the high data word. In this case, the acceleration is 1.0 rev/sec^2.
			Busy-bit Check Module
d d	00 11	HB LB	acceleration data word (low)
			Busy-bit Check Module
d d	00 02	HB LB	Velocity is loaded in two data words. These two bytes are the high data word. In this case, velocity is 2.0 rev/s.
			Busy-bit Check Module
d d	0C 4A	HB LB	velocity data word (low)
			Busy-bit Check Module
c	01	STT	Start motion control.
			Busy-bit Check Module
c	1F	LTRJ	This command initiates loading the trajectory parameters input buffers.
			Busy-bit Check Module
d d	18 0C	HB LB	These two bytes are the trajectory control word. A 18 hex HB programs forward direction velocity mode operation. A 0C hex LB indicates only velocity will be loaded and it will be a relative value.
			Busy-bit Check Module
d d	00 02	HB LB	Velocity is loaded in two data words. These two bytes are the high data word. In this case, velocity is 2.0 rev/s. Because this is a relative value, the current velocity will be increased by 2.0 rev/s. The resultant velocity will be 4.0 rev/s.
			Busy-bit Check Module
d d	0C 4A	HB LB	velocity data word (low)
		wait	This wait represents the host processor waiting for an LM628 breakpoint interrupt.
c	01	STT	Start motion control.
			Busy-bit Check Module
c	1D	RSTI	Reset interrupts.
			Busy-bit Check Module
d d	xx 00	HB LB	don't care Zeros in bits one through six reset **all** interrupts.
			Busy-bit Check Module
c	20	SPBA	This command initiates loading an absolute breakpoint.
			Busy-bit Check Module
d d	00 02	HB LB	A breakpoint is loaded in two data words. These two bytes are the high data word. In this case, the breakpoint is 160,000 counts absolute.
			Busy-bit Check Module
d d	71 00	HB LB	breakpoint data word (low)
		wait	This wait represents the host processor waiting for an LM628 breakpoint interrupt.
			"Smooth" Stop Module



***Note:** All resistor values in Ω

FIGURE 15. Reference System

III. Tuning the PID Filter

BACKGROUND

The transient response of a control system reveals important information about the "quality" of control, and because a step input is easy to generate and sufficiently drastic, the transient response of a control system is often characterized by the response to a step input, the system step response.

In turn, the step response of a control system can be characterized by three attributes: maximum overshoot, rise time, and settling time. These step response attributes are defined in what follows and detailed graphically in *Figure 16*.

1. The maximum overshoot, Mp, is the maximum peak value of the response curve measured from unity. The amount of maximum overshoot directly indicates the relative stability of the system.
2. The rise time, t_r, is the time required for the response to rise from ten to ninety percent of the final value.
3. The settling time, t_s, is the time required for the response to reach and stay within two percent of the final value.

A critically damped control system provides optimum performance. The step response of a critically damped control system exhibits the minimum possible rise time that maintains zero overshoot and zero ringing (damped oscillations). *Figure 17* illustrates the step response of a critically damped control system.

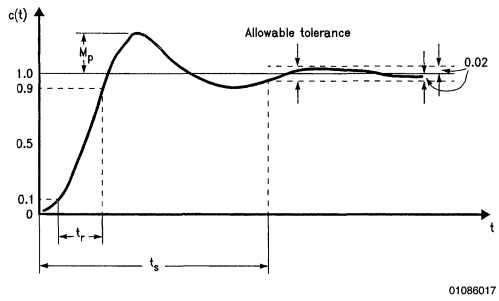


FIGURE 16. Unit Step Response Curve Showing Transient Response Attributes

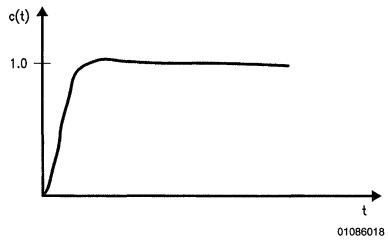


FIGURE 17. Unit Step Response of a Critically Damped System

INTRODUCTION

The LM628 is a digital PID controller. The loop-compensation filter of a PID controller is usually tuned experimentally, especially if the system dynamics are not well known or defined.

The ultimate goal of tuning the PID filter is to critically damp the motor control system—provide optimum tracking and settling time.

As shown in *Figure 7*, the response of the PID filter is the sum of three terms, a proportional term, an integral term, and a derivative term. Five variables shape this response. These five variables include the three gain coefficients (k_p, k_i, and k_d), the integration limit coefficient (i_l), and the derivative sampling coefficient (d_s). *Tuning the filter equates to determining values for these variable coefficients, values that critically damp the control system* .

Filter coefficients are best determined with a two-step experimental approach. In the first step, the values of k_p, k_i, and k_d (along with i_l and d_s) are systematically varied until reasonably good response characteristics are obtained. Manual and visual methods are used to evaluate the effect of each coefficient on system behavior. In the second step, an oscilloscope trace of the system step response provides detailed information on system damping, and the filter coefficients, determined in step one, are modified to critically damp the system.

Note: In step one, adjustments to filter coefficient values are inherently coarse, while in step two, adjustments are inherently fine Due to this coarse/fine nature, steps one and two complement each other, and the two-step approach is presented as the "best" tuning method The PID filter can be tuned with either step one or step two alone

STEP ONE—MANUAL VISUAL METHOD

Introduction

In the first step, the values of k_p, k_i, and k_d (along with i_l and d_s) are systematically varied until reasonably good response characteristics are obtained. Manual and visual methods are used to evaluate the effect of each coefficient on system behavior.

Note: The next four numbered sections are ordered steps to tuning the PID filter

1. Prepare the System

The initialization section of the filter tuning program is executed to prepare the system for filter tuning. See *Table 11*. This section initializes the system, presets the filter parameters (k_p, k_i, il = 0, k_d = 2, d_s = 1), and commands the control loop to hold the shaft at the current position.

After executing the initialization section of the filter tuning program, both desired and actual shaft positions equal zero; the shaft should be stationary. Any displacement of the shaft constitutes a position error, but with both k_p and k_i set to zero, the control loop can not correct this error.

2. Determine the Derivative Gain Coefficient

The filter derivative term provides damping to eliminate oscillation and minimize overshoot and ringing, stabilize the system. Damping is provided as a force proportional to the rate of change of position error, and the constant of proportionality is k_d x d_s. See *Figure 18*.

Coefficients k_d and d_s are determined with an iterative process. Coefficient k_d is systematically increased until the shaft begins high frequency oscillations. Coefficient d_s is then increased by one. The entire process is repeated until d_s reaches a value appropriate for the system.

III. Tuning the PID Filter (Continued)

The system sample period sets the time interval between updates of position error. The derivative sampling interval is an integer multiple of the system sample period. See *Table 3*. It sets the time interval between successive position error samples used in the derivative term, and, therefore, directly affects system damping. The derivative sampling interval should be five to ten times smaller than the system mechanical time constant — this means many systems will require low d_s. In general, however, k_d and d_s should be set to give the largest k_d x d_s product that maintains acceptably low motor vibrations.

Note: Starting k_d at two and doubling it is a good method of increasing k_d Manually turning the shaft reveals that with each increase of k_d, the resistance of the shaft to turning increases The shaft feels increasingly sluggish and, because k_d provides a force proportional to the rate of change of position error, the faster the shaft is turned the more sluggish it feels For the reference system, the final values of k_d and d_s are 4000 and 4 respectively

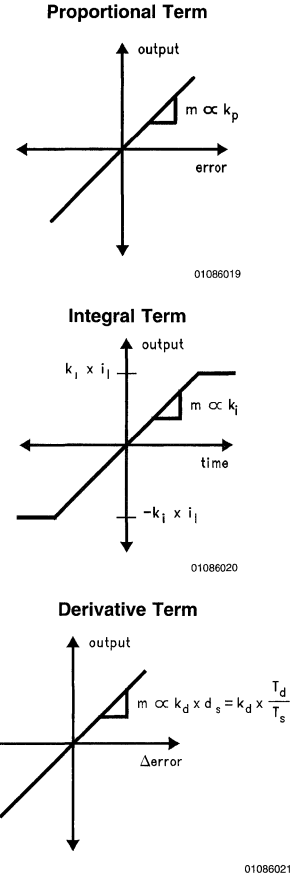


FIGURE 18. Proportional, Integral, and Derivative (PID) Force Components

TABLE 11. Initialization Section— Filter Tuning Program

Port	Bytes	Command	Comments
c	00	RESET	See Initialization Module Text
		wait	The maximum time to complete RESET tasks is 1.5 ms.
c	06	PORT12	The RESET default size of the DAC port is eight bits. This command initializes the DAC port for a 12-bit DAC. It should not be issued in systems with an 8-bit DAC.
Busy-bit Check Module			
c	1D	RSTI	This command resets **only** the interrupts indicated by zeros in bits one through six of the next data word. It also resets bit fifteen of the Signals Register and the host interrupt pin (pin 17).
Busy-bit Check Module			
d	xx	HB	don't care
d	00	LB	Zeros in bits one through six indicate **all** interrupts will be reset.
Busy-bit Check Module			
c	1C	MSKI	This command masks the interrupts indicated by zeros in bits one through six of the next data word.
Busy-bit Check Module			
d	xx	HB	don't care

III. Tuning the PID Filter (Continued)

TABLE 11. Initialization Section— Filter Tuning Program (Continued)

Port	Bytes	Command	Comments
d	04	LB	A 04 hex LB enables (unmasks) the trajectory complete interrupt. All other interrupts are disabled (masked). See *Figure 6*.
			Busy-bit Check Module
c	1E	LFIL	This command initiates loading the filter coefficients input buffers.
			Busy-bit Check Module
d d	00 x2	HB LB	These two bytes are the filter control word. A 00 hex HB sets the derivative sampling interval to $2048/f_{CLK}$ by setting d_s to one. A x2 hex LB indicates only k_d will be loaded. The other filter parameters will remain at zero, their reset default value.
			Busy-bit Check Module
d d	00 02	HB LB	These two bytes set k_d to two.
			Busy-bit Check Module
c	04	UDF	This command transfers new filter coefficients from input buffers to working registers. Until UDF is executed, coefficients loaded via the LFIL command do not affect the filter transfer characteristic.
			Busy-bit Check Module
c	1F	LTRJ	This command initiates loading the trajectory parameters input buffers.
			Busy-bit Check Module
d d	00 00	HB LB	These two bytes are the trajectory control word. A 00 hex LB indicates no trajectory parameters will be loaded.
			Busy-bit Check Module
c	01	STT	STT must be issued to execute the desired trajectory.

3. Determine the Proportional Gain Coefficient

Inertial loading causes following (or tracking) error, position error associated with a moving shaft. External disturbances and torque loading cause displacement error, position error associated with a stationary shaft. The filter proportional term provides a restoring force to minimize these position errors. The restoring force is proportional to the position error and increases linearly as the position error increases. See *Figure 18*. The proportional gain coefficient, k_p, is the constant of proportionality.

Coefficient k_p is determined with an iterative process—the value of k_p is increased, and the system damping is evaluated. This is repeated until the system is critically damped.

System damping is evaluated manually. Manually turning the shaft reveals each increase of k_p increases the shaft "stiffness". The shaft feels spring loaded, and if forced away from its desired holding position and released, the shaft "springs" back. If k_p is too low, the system is over damped, and the shaft recovers too slowly. If k_p is too large, the system is under damped, and the shaft recovers too quickly. This causes overshoot, ringing, and possibly oscillation. The proportional gain coefficient, k_p, is increased to the largest value that does not cause excessive overshoot or ringing. At this point the system is critically damped, and therefore provides optimum tracking and settling time.

Note: Starting k_p at two and doubling it at each iteration is a good method of increasing k_p. The final value of k_p for the reference system is 40.

4. Determine the Integral Gain Coefficient

The filter proportional term minimizes the errors due to inertial and torque loading. The integral term, however, provides a corrective force that can eliminate following error while the shaft is spinning and the deflection effects of a static torque load while the shaft is stationary. This corrective force is proportional to the position error and increases linearly with time. See *Figure 18*. The integral gain coefficient, k_i, is the constant of proportionality.

High values of k_i provide quick torque compensation, but increase overshoot and ringing. In general, k_i should be set to the smallest value that provides the appropriate compromise between three system characteristics: overshoot, settling time, and time to cancel the effects of a static torque load. In systems without significant static torque loading, a k_i of zero may be appropriate.

The corrective force provided by the integral term increases linearly with time. The integration limit coefficient, i_l, acts as a clamping value on this force to prevent integral wind-up, a backlash effect. As noted in *Figure 18*, i_l limits the summation of error (over time), not the product of k_i and this summation. In many systems i_l can be set to its maximum value, 7FFF hex, without any adverse effects. The integral term has no effect if i_l is set to zero.

For the test system, the final values of k_i and i_l are 5 and 1000 respectively.

STEP TWO—STEP RESPONSE METHOD

Introduction

The step response of a control system reveals important information about the "quality" of control—specifically, detailed information on system damping.

In the second step to tuning the PID filter, an oscilloscope trace of the control system step response is used to accurately evaluate system damping, and the filter coefficients, determined in step one, are fine tuned to critically damp the system.

III. Tuning the PID Filter (Continued)

Software Considerations

The step generation section of the filter tuning program provides the control loop with a repetitive small-signal step input. This is accomplished by repeatedly executing a small position move with high maximum velocity and high acceleration. See *Figure 19* and *Table 12*.

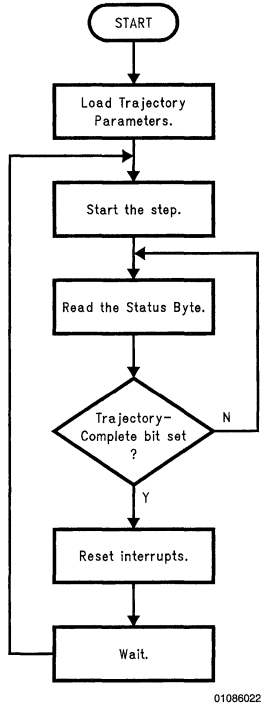


FIGURE 19. Step Generation Section of Filter Tuning Program

III. Tuning the PID Filter (Continued)

TABLE 12. Step Generation Section—Filter Tuning Program

Port	Bytes	Command	Comments
c	1F	LTRJ	This command initiates loading the trajectory parameters input buffers.
			Busy-bit Check Module
d d	00 2B	HB LB	These two bytes are the trajectory control word. A 2B hex LB indicates acceleration, velocity, and position will be loaded and both acceleration and velocity are absolute while position is relative.
			Busy-bit Check Module
d d	00 04	HB LB	Acceleration is loaded in two data words. These two bytes are the high data word.
			Busy-bit Check Module
d d	93 E0	HB LB	acceleration data word (low)
			Busy-bit Check Module
d d	00 07	HB LB	Velocity is loaded in two data words. These two bytes are the high data word.
			Busy-bit Check Module
d d	A1 20	HB LB	velocity data word (low)
			Busy-bit Check Module
d d	00 00	HB LB	Position is loaded in two data words. These two bytes are the high data word.
			Busy-bit Check Module
d d	00 C8	HB LB	position data word (low)
			Busy-bit Check Module
c	01	STT	STT must be issued to execute the desired trajectory.
			Busy-bit Check Module
c	xx	RDSTAT	This command reads the Status Byte. It is directly supported by LM628 hardware and can be executed at any time by pulling $\overline{CS}$, $\overline{PS}$, and $\overline{RD}$ logic low. Status information remains valid as long as $\overline{RD}$ is logic low.
		decision	If the Trajectory Complete interrupt bit is set, continue. Otherwise loop back to RDSTAT.
c	1D	RSTI	This command resets **only** the interrupts indicated by zeros in bits one through six of the next data word. It also resets bit fifteen of the Signals Register and the host interrupt pin (pin 17).
d d	xx 00	HB LB	don't care Zeros in bits one through six indicate **all** interrupts will be reset.
		wait	This wait block inserts a delay between repetitions of the step input. The delay is application specific, but a good range of values for the delay is 5 ms to 5000 ms.
		loop	Loop back to STT.

Hardware Considerations

For a motor control system, an oscilloscope trace of the system step response is a graph of the real position of the shaft versus time after a small and instantaneous change in desired position.

For an LM628-based system, no extra hardware is needed to view the system step response. During a step, the voltage across the motor represents the system step response, and an oscilloscope is used to generate a graph of this response (voltage).

For an LM629-based system, extra hardware is needed to view the system step response. *Figure 20* illustrates a circuit for this purpose. During a step, the voltage output of this circuit represents the system step response, and an oscilloscope is used to generate a graph of this response.

The oscilloscope trigger signal, a rectangular pulse train, is taken from the host interrupt output pin (pin 17) of the LM628/LM629. This signal is generated by the combination of a trajectory complete interrupt and a reset interrupts (RSTI) command. See *Figure 19*.

Note: The circuit of *Figure 20* can be used to view the step response of an LM628-based system.

III. Tuning the PID Filter (Continued)

Observations

What follows are example oscilloscope traces of the step response of the reference system.

Note 8: All traces were generated using the circuit of *Figure 20*

Note 9: All traces were generated using the following "step" trajectory parameters. relative position, 200 counts, absolute velocity, 500,000 counts/sample, acceleration, 300,000 counts/sample/sample These values generated a good small-signal step input for the reference system, other systems will require different trajectory parameters In general, step trajectory parameters consist of a small relative position, a high velocity, and a high acceleration

The position parameter must be relative Otherwise, a define home command (DFH) must be added to the main loop of the step generation section — filter tuning program See *Figure 19*

The circuit for viewing the system step response uses an 8-bit analog-to-digital converter See *Figure 20* To prevent converter overflow, the step position parameter must not be set higher than 200 counts

Note 10: The circuit of *Figure 20* produces an "inverted" step response graph The oscilloscope input was inverted to produce a positive-going (more familiar) step response graph

Figure 21 represents the step response of an under damped control system; this response exhibits excessive overshoot and long settling time. The filter parameters used to generate this response were as follows: k_p, 35; k_i, 5; k_d, 600; d_s, 4; i_l, 1000. *Figure 21* indicates the need to increase k_d, the derivative gain coefficient.

Figure 22 represents the step response of an over damped control system; this response exhibits excessive rise time which indicates a sluggish system. The filter parameters used to generate this response were as follows: k_p, 35; k_i, 5, k_d, 10,000; d_s, 7; i_l, 1000. *Figure 22* indicates the need to decrease k_d and d_s.

Figure 23 represents the step response of a critically damped control system; this response exhibits virtually zero overshoot and short rise time. The filter parameters used to generate this response were as follows: k_p, 40; k_i, 5; k_d, 4000; d_s, 4; i_l, 1000.

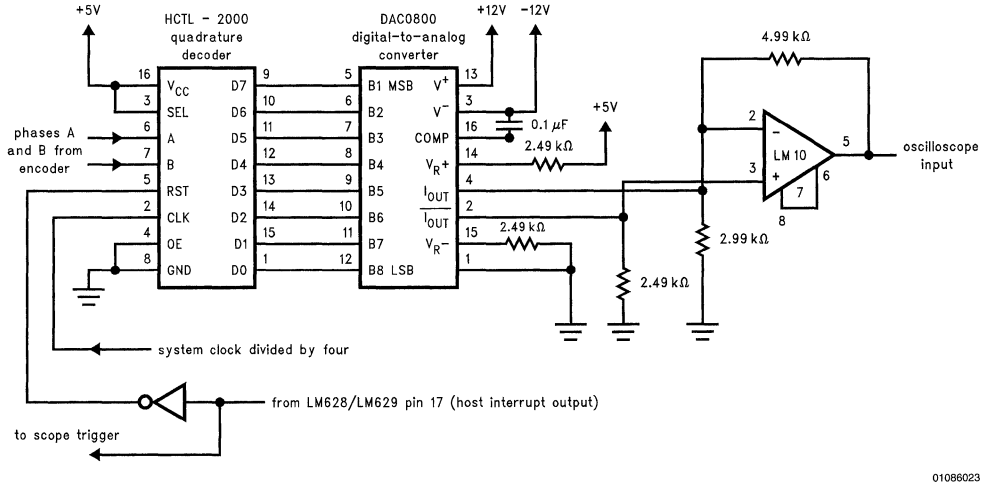


FIGURE 20. Circuit for Viewing the System Step Response with an Oscilloscope

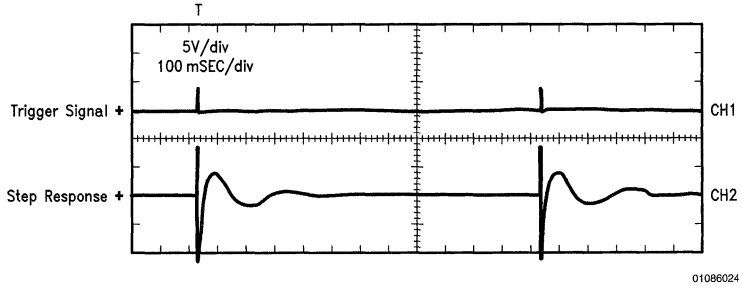


FIGURE 21. The Step Response of an Under Damped Control System

III. Tuning the PID Filter (Continued)

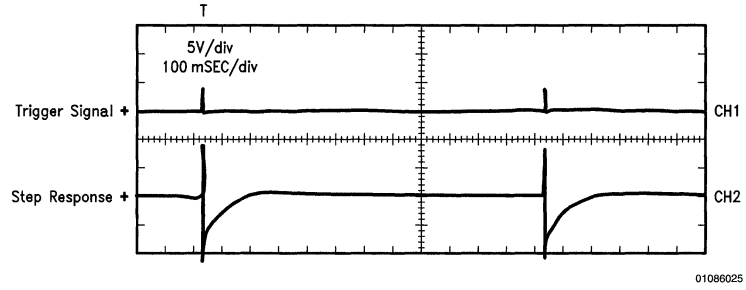


FIGURE 22. The Step Response of an Over Damped Control System

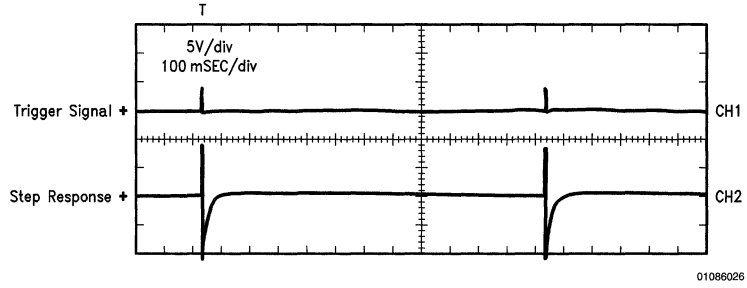


FIGURE 23. The Step Response of a Critically Damped Control System

A DMOS 3A, 55V, H-Bridge: The LMD18200

National Semiconductor
Application Note 694
Tim Regan

Introduction

The switching power device shown in *Figure 1* is called an H-Bridge. It takes a DC supply voltage and provides 4-quadrant control to a load connected between two pairs of power switching transistors. Because the switches allow current to flow bidirectionally, the voltage across the load and the direction of current through the load can be of either polarity.

H-Bridges are often used to control the speed, position or torque of DC and stepper motors. Traditionally implemented with either discrete or monolithic bipolar transistors, fully integrated solutions are becoming increasingly popular in printer, plotter, robotics and process control applications that require 0.5A to 3.0A and operate from 12V to 55V. The LMD18200 was designed to operate within this range and was optimized for such applications.

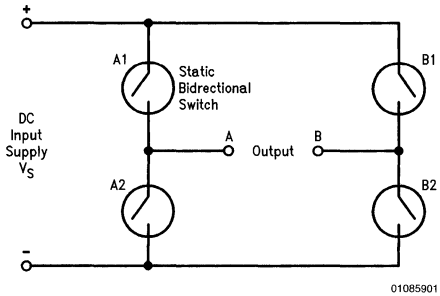


FIGURE 1. Basic H-Bridge Circuit

The LMD18200 was implemented in a process that allows bipolar, CMOS and DMOS devices to be incorporated together on one die. As each of these types of transistor structures has its own unique characteristics, each is ideally suited for a different function. By integrating them together, this allowed us to take advantage of several innovative design techniques to provide easy to use benefits typically unassociated with a simple motor driver.

Figure 2 shows a functional block diagram of the LMD18200. The circuit contains four DMOS power switching transistors, with intrinsic clamp diodes, connected in an H-Bridge configuration. All level shifting and drive circuits are included to permit control of the H-Bridge from standard logic compatible signal levels. Other unique features include current sense circuitry, overcurrent and under-voltage protection, thermal warning and thermal shutdown. Each is discussed in more detail in the following section.

Key Features

DMOS POWER DRIVERS

DMOS power transistors allow current to flow bidirectionally and provide a lower voltage drop than similarly rated bipolar power transistors by virtue of a greatly reduced on resistance for each switch. They also have the potential to operate at much faster switching speeds for more efficient operation. And, as each switch contains its own intrinsic protection diode, the additional external protection diodes that are required for bipolar transistor implementations are no longer necessary.

LOW ON RESISTANCE

Unlike bipolar transistors, which have a relatively high voltage drop across them, even at lower currents, the DMOS devices in the LMD18200 have a voltage drop that is essentially a linear function of temperature. The on resistance, $R_{DS(on)}$, of each output transistor is typically 0.3Ω at a junction temperature of 25°C and 0.6Ω at 125°C. At 100°C and 1A of current, a comparable bipolar transistor will have a voltage drop from collector to emitter of about 1.1V whereas with the LMD18200 this voltage drop will only be 0.45V. At higher current levels the lower voltage drop across a DMOS power device provides an appreciable reduction in power dissipation resulting in smaller heat sink requirements and better efficiency with more power throughput to the load.

Key Features (Continued)

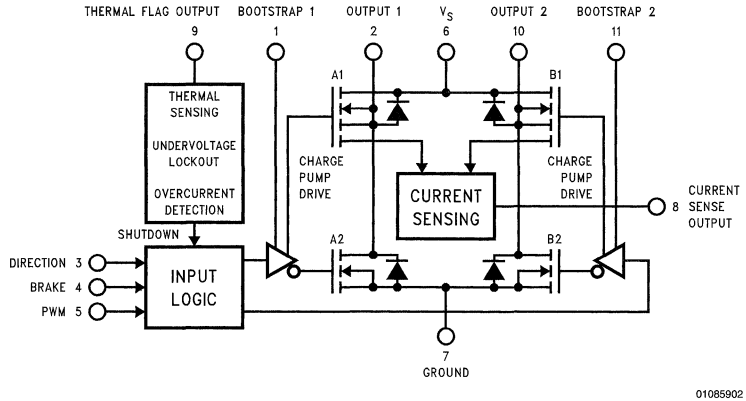


FIGURE 2. Block Diagram of the LMD18200

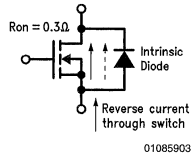


FIGURE 3. A DMOS Switch with Intrinsic Protection Diode

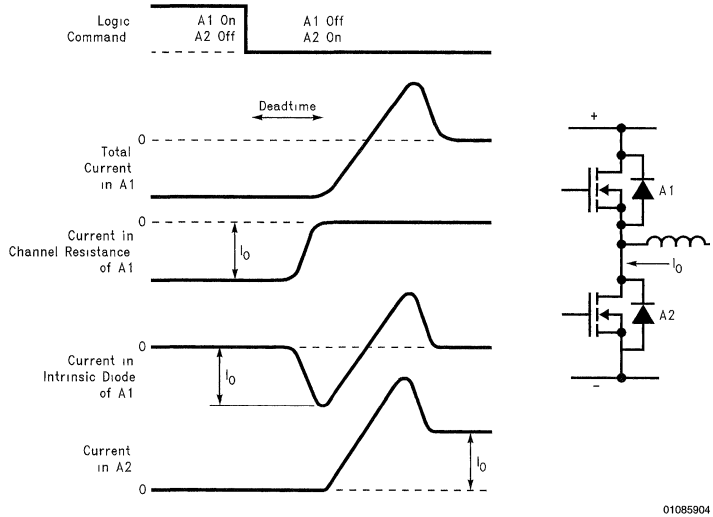


FIGURE 4. Waveforms Illustrating the Commutation of "Reverse" Current in One Switch (A1) to "Forward" Current in Another Switch (A2)

Key Features (Continued)

BIDIRECTIONAL CURRENT SWITCHES WITH INTRINSIC PROTECTION DIODES

When driving inductive and inertial loads such as motors the power switches must be able to conduct "forward" as well as "reverse" current. The energy stored in these types of loads must generally be free to return to the supply.

The conventional method of providing a path for reverse current is to connect an antiparallel diode across the power switch as shown in *Figure 3*.

With the DMOS structure used in the LMD18200 this diode is intrinsic. Reverse current is actually shared between the power switch and the diode due to the fact that the DMOS switch can conduct current in either direction. For current levels less than 2A to 2.5A the voltage across the power switch, ($IxR_{DS(on)}$), is less than the forward threshold voltage of the diode and all of the current flows through the switch. At higher current levels the diode conducts and the current is shared

An important consideration in the design of the LMD18200 was to make sure that the power switches could handle not only the load current but also the additional reverse recovery current of the protection diodes. This is illustrated in *Figure 4* where switch A1 is initially ON and conducting reverse current. At the interval when A1 is commanded OFF and the lower switch in the same leg of the H-Bridge, A2 is commanded ON, a short deadtime (purposely built in to the LMD18200 to eliminate "shoot-through" currents) occurs. During this time current begins to flow through the protection diode across switch A1. When switch A2 comes ON, the diode becomes reverse biased. Switch A2 must then conduct the load current plus the reverse recovery current of the diode for the short (approximately 100 ns) reverse recovery time of the diode. This additional requirement on the power switches has been accommodated in the design of the LMD18200.

CURRENT SENSING

A unique feature of the LMD18200 is circuitry that allows for the sensing of the current through the load without affecting the supply or ground return lines. A common method for sensing the load current is to insert a small valued power resistor in series with either the V_{CC} supply or ground lines and detect the voltage drop across this resistor. This voltage drop not only takes away from the available voltage to be applied to the load but is also somewhat difficult to amplify due to very low or possibly fast varying common mode voltage presented to the amplifier.

The principle employed in the LMD18200 is the same as that used in discrete current sensing power MOSFETs. Each DMOS power transistor is actually comprised of many smaller cells connected in parallel. Due to the positive temperature coefficient of the ON resistance of each cell, the total current through the switch divides almost equally between the individual cells. A few of these cells are separated out to provide a current that is a scaled down replica of the total switch current. *Figure 5* shows a simplified functional diagram of the current sensing circuitry

The current sourced by the Current Sense Output pin is a current proportional to the sum of the total forward current conducted by the two upper DMOS switches of the H-Bridge. This sense current has a typical value of 377 µA per Amp of current through the power devices Simply connecting a resistor between the sense output pin and ground converts this current to a voltage proportional to the current being delivered to the load. This voltage is then suitable for feedback control or load over-current protection purposes.

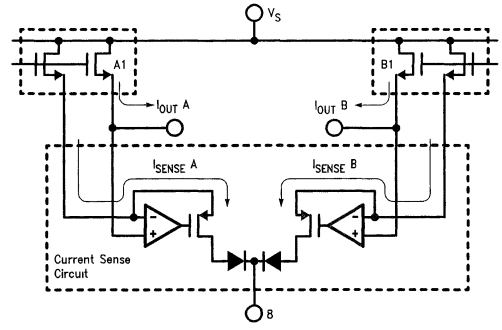


FIGURE 5. The Current Sensing Circuitry of the LMD18200

CHARGE PUMP AND BOOTSTRAP CIRCUITRY

In order to drive a DMOS switch ON, its gate must be driven approximately 10V more positive than its source voltage. The lower switches of the H-Bridge have their source terminals connected to ground and their gate drive is derived from the V_S supply voltage to the device. The two upper switches however have their source terminals connected to the output pins which are continually being switched between ground and V_S. In order to generate the gate drive voltage for these switches a charge pump circuit is used. *Figure 6a* illustrates this circuitry.

Transistors Q1 and Q2 are toggled at an internally generated clock frequency of 300 kHz. When Q2 is ON, the on-chip charge pump capacitor, C_{CP}, is charged to approximately 14V. When Q1 is switched ON the bottom of this capacitor is connected to the supply voltage, V_S. This causes the voltage at point X, which connects to the gate of the upper DMOS power switch, to rise to about 14V more positive than the supply. This ensures that the upper device switches ON even if its source is at the V_S potential.

Key Features (Continued)

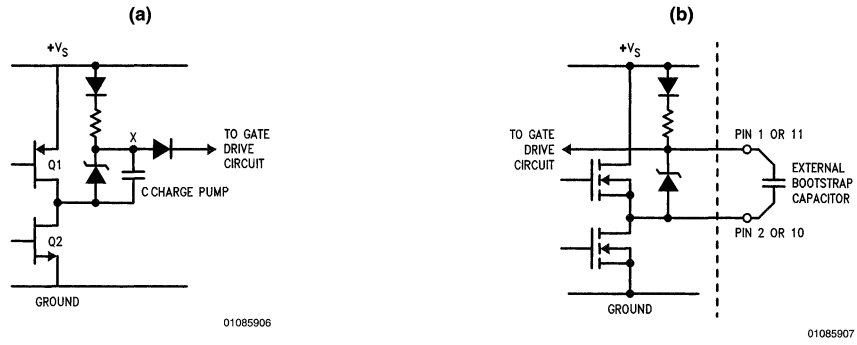


FIGURE 6. Internal Charge Pump Used in the LMD18200 (a); the Use of External Bootstrap Capacitors (b)

Capacitor C_{CP} is limited in value for practical considerations. Due to the limited charge that can be stored in C_{CP} the turn-on time of the upper DMOS transistors is relatively slow but nevertheless satisfactory for operating frequencies up to around 1 kHz. Once the DMOS device is turned ON the 300 kHz oscillator keeps the charge pump circuit running thereby holding the power device ON as long as it is commanded by the input control to do so. This charge pump circuit takes care of all the necessary voltage conditioning required by the DMOS transistors so that the external logic control applied to the LMD18200 can be simple TTL compatible signals.

For higher frequency operation, faster turn-on of the upper DMOS switches is necessary. This can be obtained through the use of external bootstrap capacitors. The bootstrap circuit is shown in *Figure 6b*. The operating principle is similar to that of the charge pump circuitry except that the switching of the bootstrap capacitor, C_B, is assumed by the DMOS power switches of the H-Bridge itself. With plenty of current available to charge these external capacitors they can have a relatively large value (10 nF is recommended) and still be charged in typically less than one microsecond. Since C_B is much larger than the input capacitance of the DMOS power transistors, these transistors can now turn ON very rapidly, typically in about 100 ns, thus allowing operating the LMD18200 at switching frequencies up to 500 kHz. *Figure 7* illustrates the switching performance of the upper transistors with and without the use of external bootstrap capacitors.

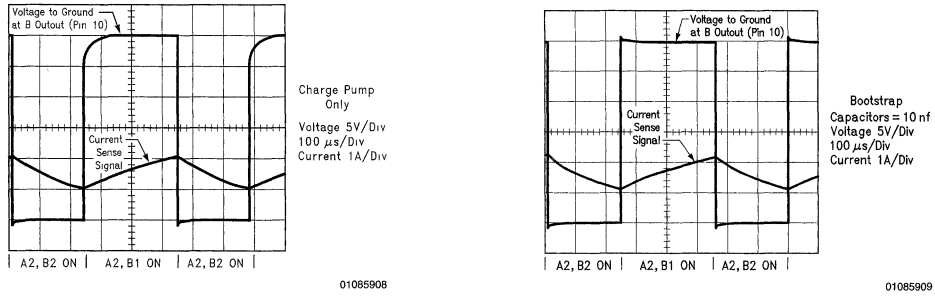


FIGURE 7. Comparison of Switching Waveforms with and without the Use of Bootstrap Capacitors

OVERCURRENT PROTECTION

The current through the upper two power DMOS switches is continually monitored and compared against a shutdown trip level (approximately 10A). In the event of a short between the two outputs or a short from either output to ground or any load condition creating excessive current to flow, the overcurrent protection circuitry will switch the upper switches OFF. A unique feature of this protection mechanism is that the protection circuitry will periodically (approximately every 8 µs) turn the upper switches back ON again, so long as the input logic is commanding the switch to be ON. This allows the H-Bridge to restart automatically following a temporary overload fault.

THERMAL WARNING/THERMAL SHUTDOWN

As with any power device protection against excessive operating temperature is a must. The LMD18200 continually senses the junction temperature near the DMOS switches and disables all of the switches in the event that this temperature reaches approximately 170°C thus protecting the

Key Features (Continued)

device from catastrophic failure. There is a slight amount of hysteresis associated with this temperature threshold so that when the temperature cools slightly the device will automatically restart.

Another unique feature of the LMD18200 is the provision of an early warning flag of excessive operating temperature. This is an open collector output pin which pulls to a logic 0 state when the junction temperature reaches 145°C. This flag can signal the system controller that the power driver is getting too hot and should be either shut down or have the output power cut back. The warning flags from any number of H-Bridges can be directly wired together for an "Or'd" connection.

UNDERVOLTAGE LOCKOUT

The LMD18200 also features undervoltage lockout. This circuitry disables all of the switches when the DC power supply voltage falls below approximately 10V. The reason for this feature is that reliable, well controlled operation of the switches cannot be assured without at least 10V applied.

Operation

The average output voltage across the load of the H-Bridge is continuously controlled by Pulse Width Modulation (PWM). Either polarity of output voltage can be obtained and current can flow through the load in either direction as required. The LMD18200 has three logic control inputs, PWM, Direction and Brake which control the switching action of the H-Bridge. *Figure 8* outlines the effect of these control inputs. The logic control inputs can be used directly (without external logic) to implement two of the more common PWM control techniques, Locked Antiphase control and Sign/Magnitude control.

PWM	Dir	Brake	Active Output Drivers
H	H	L	A1, B2
H	L	L	A2, B1
L	X	L	A1, B1
H	H	H	A1, B1
H	L	H	A2, B2
L	X	H	NONE

FIGURE 8. Control Logic Truth Table

LOCKED ANTI-PHASE CONTROL

The basic connection diagram and idealized waveforms for driving an inductive load using Locked Anti-phase control are illustrated in *Figure 9*. Under the control of the single PWM input signal, diametrically opposite pairs of switches (the top switch in one leg of the H-Bridge together with the bottom switch of the opposite leg) are driven ON and OFF together ("locked" together, hence the name Locked Anti-phase control). At zero average output voltage, the average voltage at each output terminal is midway between the V_{CC} supply and ground. For this condition the conduction duty cycle of each switch is 50% and the average current through the load is zero.

As the A1,B2 locked conduction interval is increased by changing the duty cycle of the control signal (75% as shown in the figure), the conduction time for the A2,B1 pair is correspondingly decreased. This duty cycle change makes the average voltage at V_OA more positive than V_OB thereby impressing a voltage across the load. The average current through the load then flows in the direction from terminal V_OA to V_OB. With a motor load this causes rotation in one direction with a speed proportional to the amount that the duty cycle deviates from 50%. Conversely, when the duty cycle is decreased to less than 50%, the average voltage from V_OA to V_OB becomes negative, the average current through the load then flows from V_OB to V_OA and the direction of rotation reverses.

If the ripple current through the load ever wants to reverse its direction it is free to do so. This is due to the fact that two switches are always driven ON and are always able to conduct current of either polarity. Another benefit of this type of control is that the voltage across the load is always defined by the state of the switches, regardless of the direction the load current wants to flow.

In applications where fast dynamic control of inertial loads (i.e., the rapid reversal of the direction of rotation of a motor) it is important that the "regeneration" of net average power from the load back to the supply be able to take place With two switches ON there is always a path for this regenerative energy.

A major advantage of Locked Anti-phase control is that only one control signal is required to control both the speed and direction of a motor load. Simply modifying the duty cycle adjusts the average voltage and current to the load for speed control and the direction of rotation depends on whether the duty cycle is greater than or less than 50%.

One disadvantage of Locked Anti-phase control with the LMD18200 is that the current sense output is discontinuous as shown in *Figure 9*. This is because the current sensing transistors only mirror "forward" current through the upper two DMOS power devices. "Reverse" current, when the direction of current flow is in the opposite direction of what it should be for a given polarity of voltage across the load, is not output to the current sense pin.

SIGN/MAGNITUDE CONTROL

A second method of PWM control directly supported by the LMD18200 is termed Sign/Magnitude control. The ideal waveforms for this technique are illustrated in *Figure 10*.

The voltage of the output terminal of one leg of the H-Bridge is held stationary while the average voltage of the opposite leg is varied by the duty cycle of a pulse width modulated input signal. The Sign or polarity of the voltage across the load is dictated by which side of the H-Bridge is held stationary by having one of the transistors constantly ON, and the Magnitude of the average load voltage is determined by the switching duty cycle of the two switches in the opposite leg.

Locked Antiphase Control

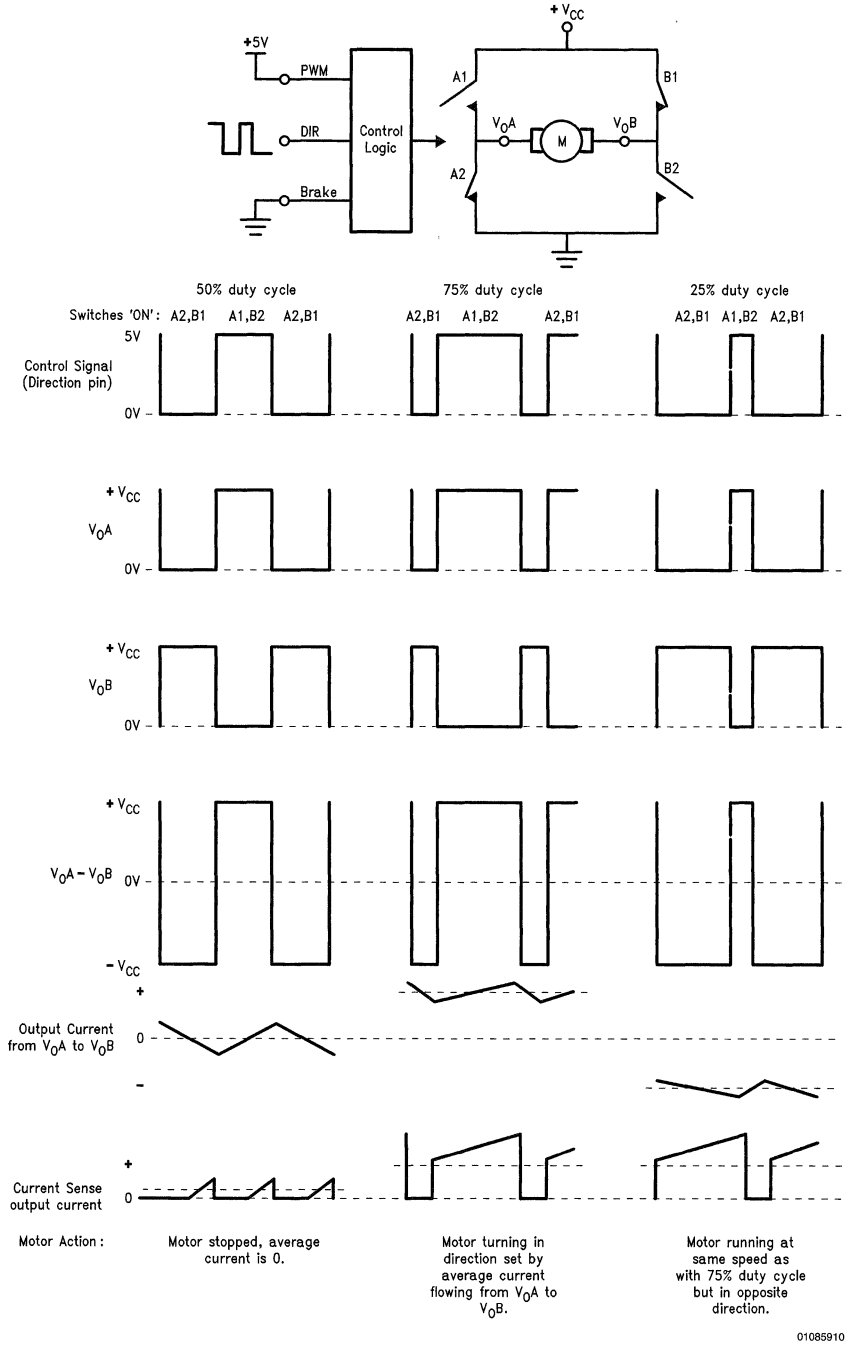


FIGURE 9. Idealized Switching Waveforms for Locked Antiphase Control

Sign/Magnitude Control

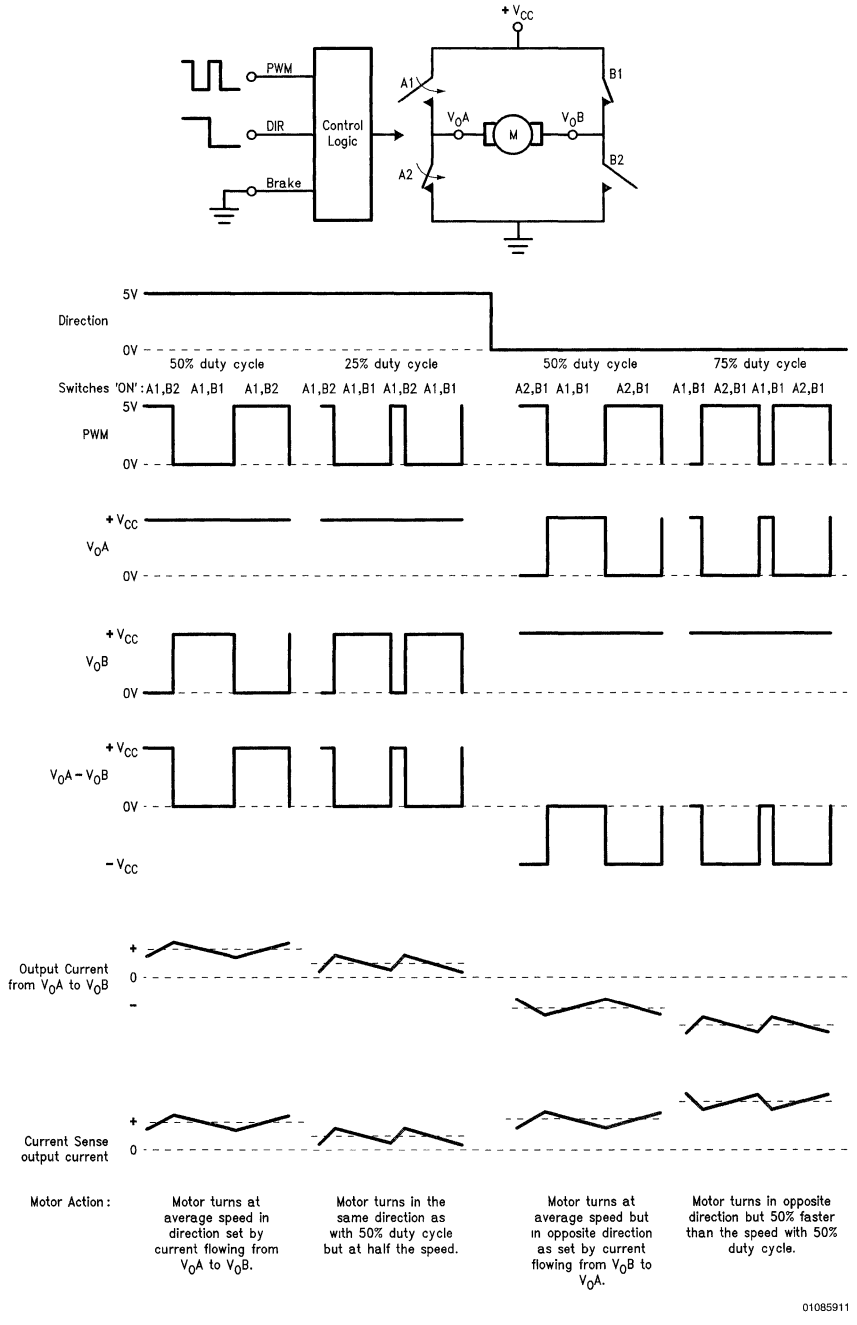


FIGURE 10. Idealized Switching Waveforms for Sign/Magnitude Control

Sign/Magnitude Control (Continued)

The logic level applied to the Direction input turns ON either switch A1 or B1. This fixes output V_OA or V_OB at the positive supply voltage potential and therefore sets the direction of current flow through the load. The duty cycle of the signal applied to the PWM pin then adjusts the average voltage and current to the load. As the duty cycle is increased, the power to the load increases causing a faster speed of rotation of motor loads

Keeping one of the upper transistors continually ON for Sign/Magnitude control is preferred with the LMD18200 because the current sense output will remain permanently active. Current will always be flowing through one upper transistor or the other (through switch A1 or B1) which will be sensed and output to the current sense pin. This gives a continuous representation of the load current without the discontinuities of the locked anti-phase technique. This is true so long as the direction of the current through the load corresponds with the polarity of voltage across the load. If the direction of rotation of a motor load is required to reverse there will be a short interval where the load regenerates net energy back to the supply and "reverse" current flows through the upper power devices and momentarily causes a discontinuity in the current sense output signal.

BRAKING

Emergency braking of a motor by shorting its terminals is achieved by taking both the PWM and Brake input pins to a logic 1 level. If the Direction input is at a logic 1, then braking will be accomplished by the two upper switches (A1 and B1) turning ON and shorting the motor, if a logic 0 then the lower switches (A2 and B2) will short out the motor. It is preferable to perform braking using the upper switches because they are protected by the overcurrent trip circuitry.

Calculating Power Dissipation

To obtain the full performance benefits of the LMD18200 it is important to consider the power dissipation of the device and provide adequate heat sinking as necessary. There are three components that make up the total power dissipation, Quiescent, Conductive and Switching power. The following equations will provide a worst case approximation of each of these components.

QUIESCENT POWER DISSIPATION, P_Q

This term is simply the quiescent, no load, power dissipation:

$$PQ = I_S \times V_{CC}$$

I_S = the quiescent supply current (typically 13 mA with a maximum value of 25 mA)

V_{CC} = the supply voltage

CONDUCTIVE POWER DISSIPATION, P_{COND}

This term is the power dissipation of the switches carrying the load current. In all applications the load current is conducted by two of the switches. The equivalent series resistance of the H-Bridge is approximately twice the on-resistance of one switch. The power dissipated by the switches can be found by:

$$P_{COND} = 2 \times I^2RMS \times R_{DS(on)}$$

I_{RMS} = worst case value of the RMS load current

$R_{DS(on)}$ = the ON resistance of a power switch at the operating junction temperature, 0.33Ω typically at 25°C and 0.6Ω maximum at 125°C.

SWITCHING POWER DISSIPATION, P_{SW}

Switching power dissipation is the combination of the energy dissipated by the switches and protection diodes during the ON/OFF switching action of the H-bridge. The combined total energy of a switch turning ON and the protection diode of a switch turning OFF can be approximated by:

$$E_{ON} = \frac{V_S I_O t_{ON}}{2} + V_S Q_{RR} + V_S I_O t_{RR}$$

When turning OFF one of the DMOS switches and transferring the current back to the protection diodes of the other switches, the turn-off energy can be approximated by:

$$E_{OFF} = \frac{V_S I_O t_{OFF}}{2}$$

The total average switching power dissipation can then be found by:

$$P_{SW} = (E_{ON} + E_{OFF}) \times f$$

This is the switching power dissipation for applications using Sign/Magnitude control where only one transistor is switched at a time. This power dissipation is **doubled** with locked anti-phase control because two transistors are always being switched simultaneously:

$P_{SW} = 2 \times (E_{ON} + E_{OFF}) \times f$, for locked anti-phase.

For these equations use the following values:

V_S= Supply voltage

I_O= peak current to the load

t_{ON}= turn ON time of the DMOS transistors, 100 ns with external bootstrap capacitors, 20 µs without

t_{OFF}= turn OFF time of the DMOS transistors, 100 ns with external bootstrap capacitors, 20 µs without

Q_{RR}= recovered charge of the intrinsic protection diode, use 150 nanocoulombs

t_{RR}= reverse recovery time of the intrinsic diode, use 100 ns

f= operating switching frequency of the H-Bridge

These values will provide a good, worst case approximation of the switching power dissipation.

Total Power Dissipation, P_{TOT}

The total power dissipation of the package is the sum of these three components:

$$P_{TOT} = P_Q + P_{COND} + P_{SW}$$

At low switching frequencies, less than 50 kHz, most of the power dissipated is conductive. When operating at higher frequencies, the switching power dissipation can become considerable and must be taken into consideration.

At 25°C ambient operating temperature with the power TO-220 package in free air, the LMD18200 can dissipate approximately 3W without requiring a heat sink.

Application Examples

Applying the LMD18200 is very easy because it is fully self-contained. The only external components required for the power stage are supply bypass capacitors and optional bootstrap capacitors and/or a current sense resistor depending on the particular application. The challenging part of any application is generating and modulating the PWM control signal. This can be achieved with dedicated PWM genera-

Application Examples (Continued)

tors like the LM3524D, with simple op amp/comparator configurations, a programmable micro-controller output line, or with a dedicated motion control device like the LM629.

Figure 11 illustrates the direct interface of an LM629 to the LMD18200 to control either the position or velocity of a DC motor. The LM629 is a digitally programmable motor controller which outputs a Sign bit and variable PWM control signal to drive the LMD18200. Feedback of the motor position is accomplished via an optical shaft encoder which generates a given number of counts per revolution of the motor shaft. The digital control algorithm is processed by the LM629 in response to commands from a host microcontroller. As shown, the thermal flag output of the LMD18200 can be used to shutdown the system or back off the drive to the motor should the IC begin to overheat. Emergency braking can also be achieved by directly driving the Brake input of the LMD18200 from an output line of the processor.

In many applications it is desired to control the torque of a motor load which is proportional to the current through the motor. Using the current sense feature of the LMD18200 provides an easy means of sensing and controlling the motor current as shown in *Figure 12*. In this application the LM3524D Regulating Pulse Width Modulator compares the voltage at the current sense output pin of the LMD18200 with an externally generated control voltage and adjusts the duty cycle of the control signal (from 0 to approximately 50%) until the motor is running at the set desired current level. In this example the switching frequency is set to 40 kHz thereby requiring the use of bootstrap capacitors. This is also an example of locked anti-phase control. By simply inverting the phase of the single control input the direction of motor rotation can be reversed.

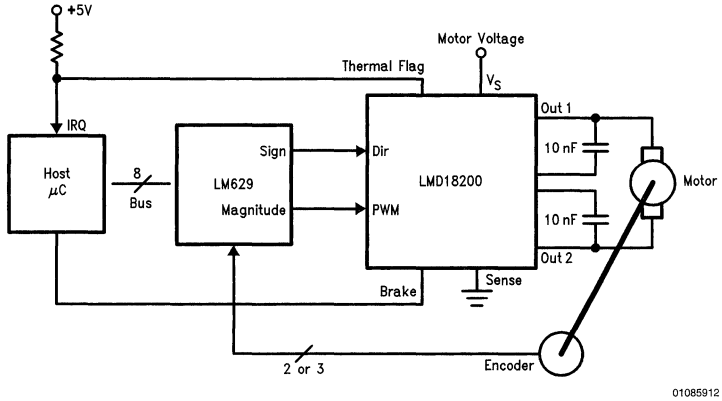


FIGURE 11. Direct Interface of an LMD 18200 to the LM629 Motion Control Device

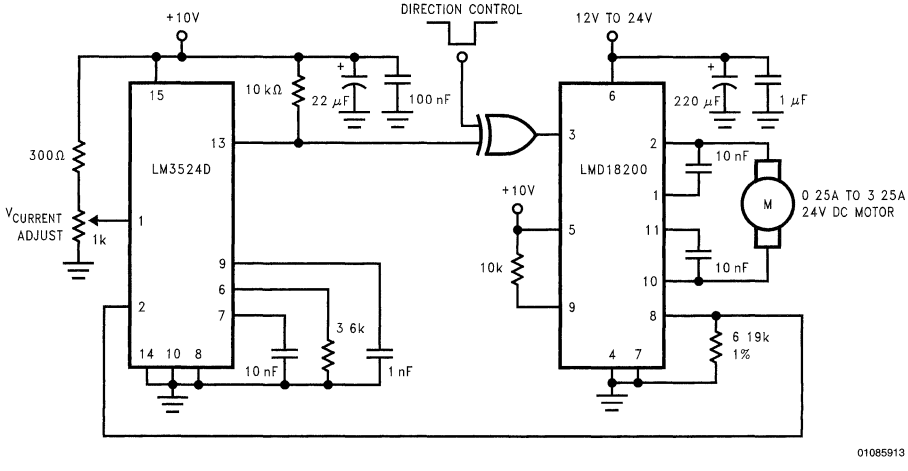


FIGURE 12. Utilizing the Current Sense Feature to Control the Torque of a Motor Load

Application Examples (Continued)

Figure 13 shows a conventional analog control scheme termed "Fixed Off Time Control". This again takes advantage of the current sensing feature of the LMD18200. A voltage representing the current through the motor is again compared with an externally generated control voltage. Whenever the motor current exceeds the desired set level a one shot is triggered which turns on the two upper switches of the H-Bridge, shorting out the motor for a fixed time interval. This causes the motor current to decrease. At the end of the one-shot interval, voltage is reapplied to the motor until the current once again exceeds the desired level. As shown in the accompanying waveforms, *Figure 14*, the average motor current modulates or "dithers" about the preset level. The amount of ripple current is proportional to the time interval of the one-shot. A certain minimum amount of ripple is required to prevent the voltage comparator from oscillating. The equivalent of 50 mV voltage change at the input to the comparator is sufficient.

The off time interval is equal to 1.1 RC, which are the timing components for the LM555 timer.

This application is an example of Sign/Magnitude control. To reverse the motor direction simply drive the Direction input of the LMD18200.

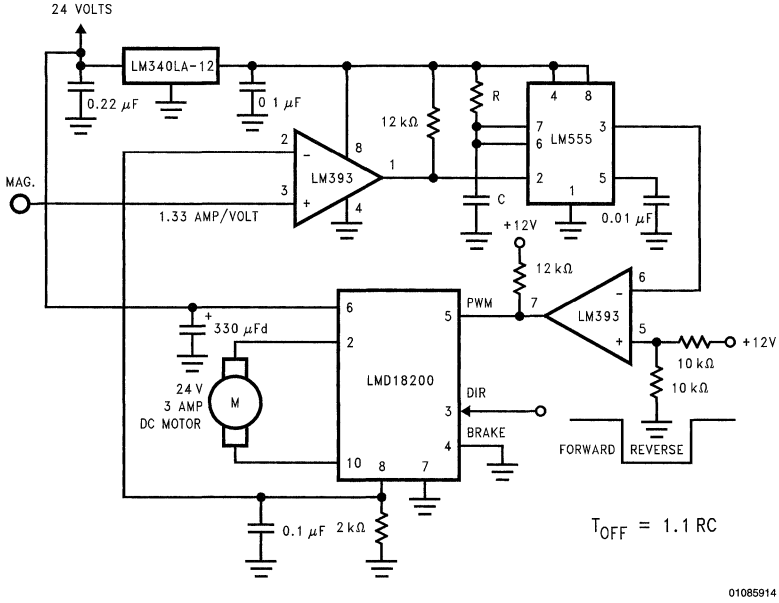


FIGURE 13. Fixed OFF Time Control

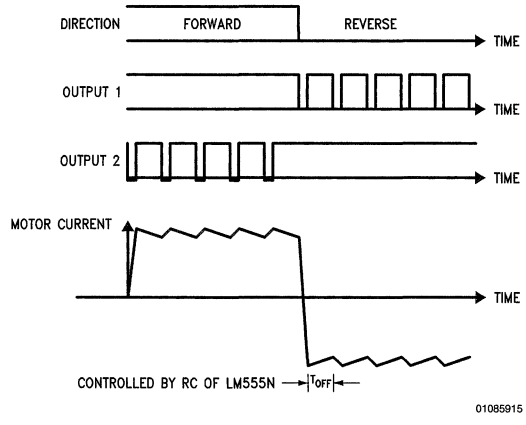


FIGURE 14. Switching Waveforms for the Fixed OFF Time Control Loop

LM628/629 User Guide

National Semiconductor
Application Note 706
Tim Regan

1.0 Introduction

1.1 APPLICATION NOTE OBJECTIVE

This application note is intended to explain and complement the information in the data sheet and also address the common user questions. While no initial familiarity with the LM628/629 is assumed, it will be useful to have the LM628/629 data sheet close by to consult for detailed descriptions of the user command set, timing diagrams, bit assignments, pin assignments, etc.

After the following brief description of the LM628/629, Section 2.0 gives a fairly full description of the device's operation, probably more than is necessary to get going with the device. This section ends with an outline of how to tune the control system by adjusting the PID filter coefficients.

Section 3 "User Command Set" discusses the use of the LM628/629 commands. For a detailed description of each command the user should refer to the data sheet.

Section 4 "Helpful User Ideas" starts with a short description of the actions necessary to get going, then proceeds to talk about some performance enhancements and follows on with a discussion of a couple of operating constraints of the device.

Section 5 "Theory" is a short foray into theory which relates the PID coefficients that would be calculated from a continuous domain control loop analysis to those of the discrete domain including the scaling factors inherent to the LM628/629. No attempt is made to discuss control system theory as such, readers should consult the ample references available, some suggestions are made at the end of this application note. Section 5 concludes with an example trajectory calculation, reviving those perhaps forgotten ideas about acceleration, velocity, distance and time.

Section 6 "Questions and Answers", is in question and answer format and is born out of and dedicated to the many interesting discussions with customers that have taken place.

1.2 BRIEF DESCRIPTION OF LM628/629

LM628/629 is a microcontroller peripheral that incorporates in one device all the functions of a sample-data motion control system controller. Using the LM628/629 makes the potentially complex task of designing a fast and precise motion control system much easier. Additional features, such as trajectory profile generation, on the "fly" update of loop compensation and trajectory, and status reporting, are included. Both position and velocity motion control systems can be implemented with the LM628/629.

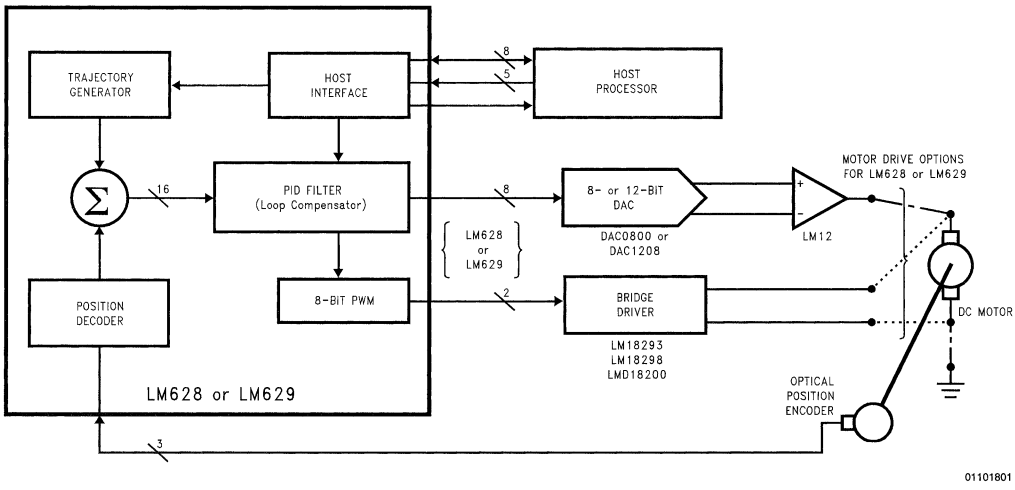


FIGURE 1. LM628 and LM629 Typical System Block Diagram

LM628/629 is itself a purpose designed microcontroller that implements a position decoder, a summing junction, a digital PID loop compensation filter, and a trajectory profile generator, *Figure 1.* Output format is the only difference between LM628 and LM629. A parallel port is used to drive an 8- or 12-bit digital-to-analog converter from the LM628 while the LM629 provides a 7-bit plus sign PWM signal with sign and magnitude outputs. Interface to the host microcontroller is via an 8-bit bi-directional data port and six control lines which includes host interrupt and hardware reset. Maximum sampling rates of either 2.9 kHz or 3.9 kHz are available by choosing the LM6268/9 device options that have 6 MHz or 8 MHz maximum clock frequencies (device -6 or -8 suffixes).

1.0 Introduction (Continued)

In operation, to start a movement, a host microcontroller downloads acceleration, velocity and target position values to the LM628/629 trajectory generator. At each sample interval these values are used to calculate new demand or "set point" positions which are fed into the summing junction. Actual position of the motor is determined from the output signals of an optical incremental encoder. Decoded by the LM628/629's position decoder, actual position is fed to the other input of the summing junction and subtracted from the demand position to form the error signal input for the control loop compensator. The compensator is in the form of a "three term" PID filter (proportional, integral, derivative), this is implemented by a digital filter. The coefficients for the PID digital filter are most easily determined by tuning the control system to give the required response from the load in terms of accuracy, response time and overshoot. Having characterized a load these coefficient values are downloaded from the host before commencing a move. For a load that varies during a movement more coefficients can be downloaded and used to update the PID filter at the moment the load changes. All trajectory parameters except acceleration can also be updated while a movement is in progress.

2.0 Device Description

2.1 HARDWARE ARCHITECTURE

Four major functional blocks make up the LM628/629 in addition to the host and output interfaces. These are the Trajectory Profile Generator, Loop Compensating PID Filter, Summing Junction and Motor Position Decoder (*Figure 1*).

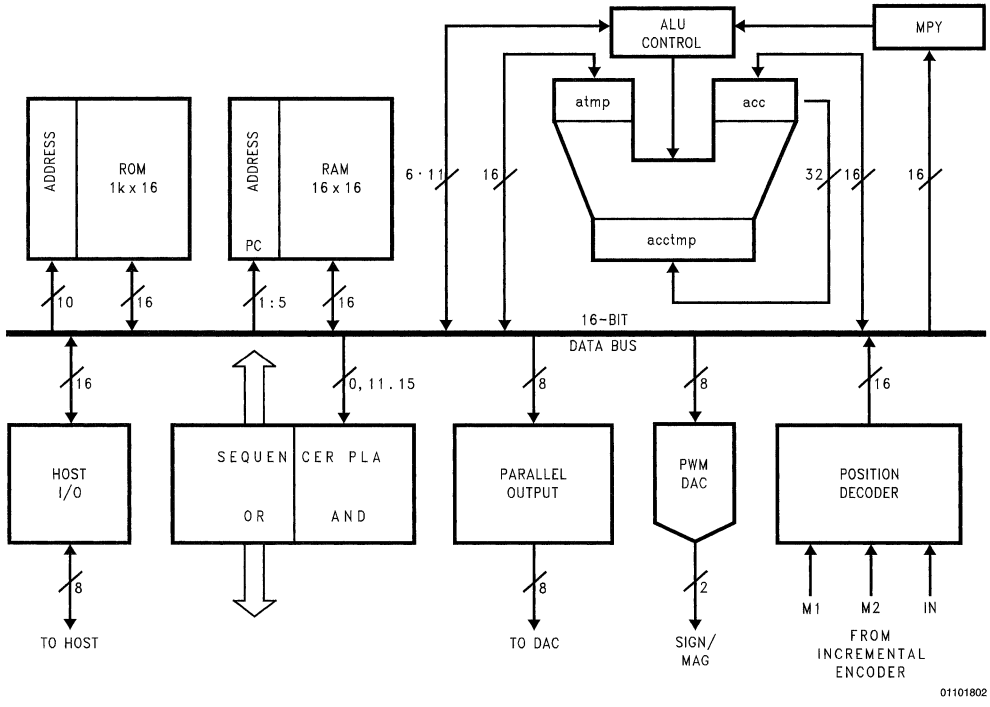


FIGURE 2. Hardware Architecture of LM628/629

Details of how LM628/629 is implemented by a purpose designed microcontroller are shown in *Figure 2*. The control algorithm is stored in a 1k x 16-bit ROM and uses 16-bit wide instructions. A PLA decodes these instructions and provides data transfer timing signals for the single 16-bit data and instruction bus. User variable filter and trajectory profile parameters are stored as 32-bit double words in RAM. To provide sufficient dynamic range a 32-bit position register is used and for consistency. 32 bits are also used for velocity and acceleration values. A 32-bit ALU is used to support the 16 x 16-bit multiplications of the error and PID digital filter coefficients.

2.2 MOTOR POSITION DECODER

LM628/629 provides an interface for an optical position shaft encoder, decoding the two quadrature output signals to provide position and direction information, *Figure 3*. Optionally a third index position output signal can be used to capture position once per revolution. Each of the four states of the quadrature position signal are decoded by the LM628/629 giving a 4 times increase in position resolution over the number of encoder lines. An "N" line encoder will be decoded as "4N" position counts by LM628/629.

2.0 Device Description (Continued)

Position decoder block diagram, *Figure 4*, shows three lines coming from the shaft encoder, M1, M2 and Index. From these the decoder PLA determines if the motor has moved forward, backward or stayed still and then drives a 16-bit up-down counter that keeps track of actual motor position. Once per revolution when all three lines including the index line are simultaneously low, *Figure 3*, the current position count is captured in an index latch.

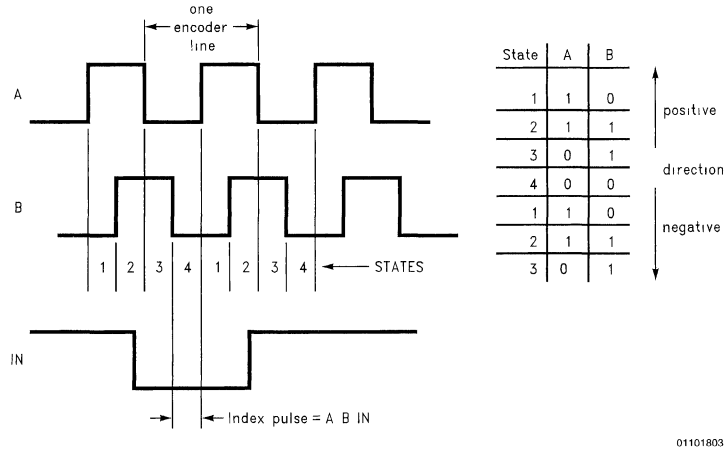


FIGURE 3. Quadrature Encoder Output Signals and Direction Decode Table

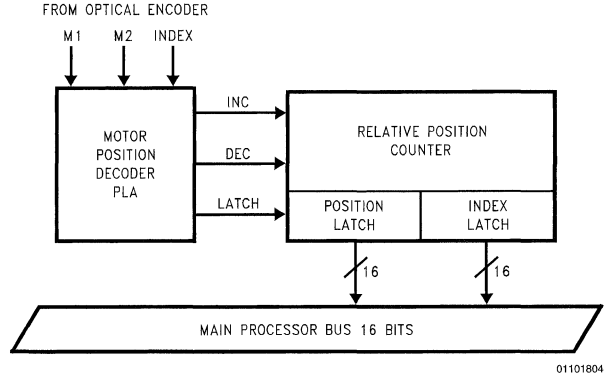


FIGURE 4. LM628/629 Motor Position Decoder

The 16-bit up-down counter is used to capture the difference in position from one sample to the next. A position latch attached to the up-down counter is strobed at the same time in every sample period by a sync pulse that is generated in hardware. The position latch is read soon after the sync pulse and is added to the 32-bit position register in RAM that holds the actual current position. This is the value that is subtracted in the summing junction every sample interval from the new desired position calculated by the trajectory generator to form the error input to the PID filter.

Maximum encoder state capture rate is determined by the minimum number of clock cycles it takes to decode each encoder state, see *Figure 3*, this minimum number is 8 clock cycles, capture of the index pulse is also achieved during these 8 clock cycles. This gives a more than adequate 1 MHz maximum encoder state capture rate with the 8 MHz f_{CLK} devices (750 kHz for the 6 MHz f_{CLK} devices). For example, with the 1 MHz capture rate, a motor using a 500 line encoder will be moving at 30,000 rpm.

There is some limited signal conditioning at the decoder input to remove problems that would occur due to the asynchronous position encoder input being sampled on signal edges by the synchronous LM628/629. But there is no noise filtering as such on the encoder lines so it is important that they are kept clean and away from noise sources.

2.0 Device Description (Continued)

2.3 TRAJECTORY PROFILE GENERATOR

Desired position inputs to the summing junction, *Figure 1*, within the LM628/629 are provided by an internal independent trajectory profile generator. The trajectory profile generator takes information from the host and computes for each sample interval a new current desired position. The information required from the host is, operating mode, either position or velocity, target acceleration, target velocity and target position in position mode.

2.4 DEFINITIONS RELATING TO PROFILE GENERATION

The units of position and time, used by the LM628/629, are counts (4 x N encoder lines) and samples (sample intervals = $2048/f_{CLK}$) respectively. Velocity is therefore calculated in counts/sample and acceleration in counts/sample/sample.

Definitions of "target", "desired" and "actual" within the profile generation activity as they apply to velocity, acceleration and position are as follows. Final requested values are called "target", such as target position. The values computed by the profile generator each sample interval on the way to the target value are called "desired". Real values from the position encoder are called "actual".

For example, the current actual position of the motor will typically be a few counts away from the current desired position because a new value for desired position is calculated every sample interval during profile generation. The difference between the current desired position and current actual position relies on the ability of the control loop to keep the motor on track. In the extreme example of a locked rotor there could be a large difference between the current actual and desired positions.

Current desired velocity refers to a fixed velocity at any point on a on-going trajectory profile. While the profile demands acceleration, from zero to the target velocity, the velocity will incrementally increase at each sample interval.

Current actual velocity is determined by taking the difference in the actual position at the current and the previous sample intervals. At velocities of many counts per sample this is reasonably accurate, at low velocities, especially below one count per sample, it is very inaccurate.

3.0 Profile Generation

Trajectory profiles are plotted in terms of velocity versus time, *Figure 5*, and are velocity profiles by reason that a new desired position is calculated every sample interval. For constant velocity these desired position increments will be the same every sample interval, for acceleration and deceleration the desired position increments will respectively increase and decrease per sample interval. Target position is the integral of the velocity profile.

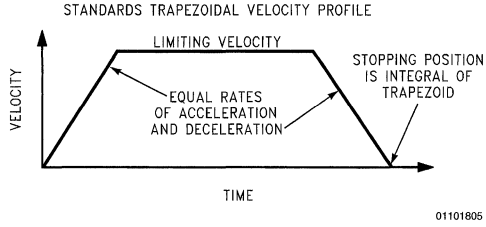


FIGURE 5. Typical Trajectory Velocity Profile

When performing a move the LM628/629 uses the information as specified by the host and accelerates until the target velocity is reached. While doing this it takes note of the number of counts taken to reach the target velocity. This number of counts is subtracted from the target position to determine where deceleration should commence to ensure the motor stops at the target position. LM628/629 deceleration rates are equal to the acceleration rates. In some cases, depending on the relative target values of velocity, acceleration and position, the target velocity will not be reached and deceleration will commence immediately from acceleration.

3.1 TRAJECTORY RESOLUTION

The resolution the motor sees for position is one integral count. The algorithm used to calculate the trajectory adds the velocity to the current desired position once per sample period and produces the next desired position point. In order to allow very low velocities it is necessary to have velocities of fractional counts per sample. The LM628/629 in addition to the 32-bit position range keeps track of 16 bits of fractional position. The need for fractional velocity counts can be illustrated by the following example using a 500 line (2000 count) encoder and an 8 MHz clock LM628/629 giving a 256 µs sample interval. If the smallest resolution is 1 count per sample then the minimum velocity would be 2 revolutions per second or 120 rpm. (1/2000 revs/count x 1/256 µs counts/second). Many applications require velocities and steps in velocity less than this amount. This is provided by the fractional counts of acceleration and velocity.

3.2 POSITION, VELOCITY AND ACCELERATION RESOLUTION

Every sample cycle, while the profile demands acceleration, the acceleration register is added to the velocity register which in turn is added to the position register. When the demand for increasing acceleration stops, only velocity is added to the position register. Only integer values are output from the position register to the summing junction and so fractional position counts must accumulate over many sample intervals before an integer count is added and the position register changed. *Figure 6* shows the position, velocity and acceleration registers.

The position dynamic range is derived from the 32 bits of the integer position register, *Figure 6*. The MSB is used for the direction sign in the conventional manner, the next bit 30 is used to signify when a position overflow called "wraparound" has occurred. If the wraparound bit is set (or reset when

3.0 Profile Generation (Continued)

going in a negative direction) while in operation the status byte bit 4 is set and optionally can be used to interrupt the host. The remaining 30 bits provide the available dynamic range of position in either the positive or negative direction (±1,073,741,824 counts).

Velocity has a resolution of $1/2^{16}$ counts/sample and acceleration has a resolution of $1/2^{16}$ counts/sample/sample as mentioned above. The dynamic range is 30 bits in both cases. The loss of one bit is due to velocity and acceleration being unsigned and another bit is used to detect wrap-around. This leaves 14 bits or 16,383 integral counts and 16 bits for fractional counts.

3.3 VELOCITY MODE

LM628 supports a velocity mode where the motor is commanded to continue at a specified velocity, until it is told to stop (LTRJ bits 9 or 10). The average velocity will be as specified but the instantaneous velocity will vary. Velocities of fractional counts per sample will exhibit the poorest instantaneous velocity. Velocity mode is a subset of position mode where the position is continually updated and moved ahead of the motor without a specified stop position. Care should be exercised in the case where a rotor becomes locked while in velocity mode as the profile generator will continue to advance the position. When the rotor becomes free high velocities will be attained to catch-up with the current desired position.

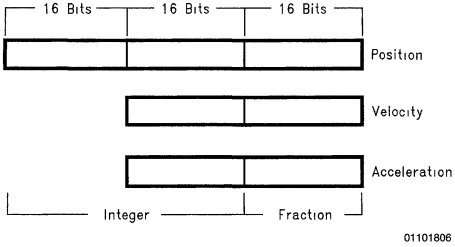


FIGURE 6. Position, Velocity and Acceleration Registers

3.4 MOTOR OUTPUT PORT

LM628 output port is configured to 8 bits after reset. The 8-bit output is updated once per sample interval and held until it is updated during the next sample interval. This allows use of a DAC without a latch. For 12-bit operation the PORT12 command should be issued immediately after reset. The output is multiplexed in two 6-bit words using pins 18 through 23. Pin 24 is low for the least significant word and high for the most significant. The rising edge of the active low strobe from pin 25 should be used to strobe the output into an external latch, see *Figure 7*. The DAC output is offset binary code, the zero codes are hex'80' for 8 bits and hex'800' for 12 bits.

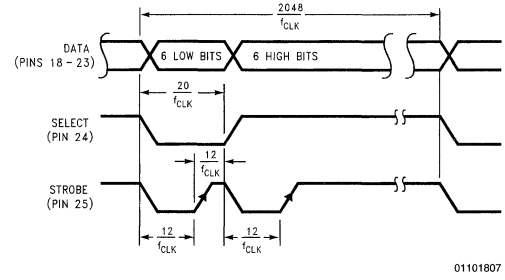
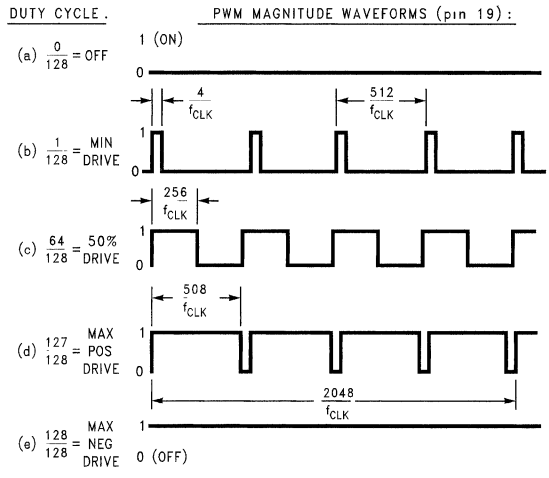


FIGURE 7. LM628 12-Bit DAC Output Multiplexed Timing

The choice of output resolution is dependant on the user's application. There is a fundamental trade-off between sampling rate and DAC output resolution, the LM628 8-bit output at a 256 µs sampling interval will most often provide as good results as a slower, e.g. microcontroller, implementation which has a 4 ms typical sampling interval and uses a 12-bit output. The LM628 also gives the choice of a 12-bit DAC output at a 256 µs sampling interval for high precision applications.

LM629 PWM sign and magnitude signals are output from pins 18 and 19 respectively. The sign output is used to control motor direction. The PWM magnitude output has a resolution of 8 bits from maximum negative drive to maximum positive drive. The magnitude output has an off condition, with the output at logic low, which is useful for turning a motor off when using a bridge motor drive circuit. The minimum duty cycle is 1/128 increasing to a maximum of 127/128 in the positive direction and a maximum of 128/128 in the negative direcition, i.e., a continuous output. There are four PWM periods in one LM629 sample interval. With an 8 MHz clock this increases the PWM output rate to 15.6 kHz from the LM629 maximum 3.9 kHz sample rate, see *Figure 8* for further timing information.

3.0 Profile Generation (Continued)



Note: Sign output (pin 18) not shown.

FIGURE 8. LM629 PWM Output Signal Format

3.5 HOST INTERFACE

LM628/629 has three internal registers: status, high, and low bytes, *Figure 9*, which are used to communicate with the host microcontroller. These are controlled by the $\overline{RD}$, $\overline{WR}$, and $\overline{PS}$ lines and by use of the busy bit of the status byte. The status byte is read by bringing $\overline{RD}$ and $\overline{PS}$ low, bit 0 is the busy bit. Commands are written by bringing $\overline{WR}$ and $\overline{PS}$ low. When $\overline{PS}$ is high, $\overline{WR}$brought low writes data into LM628/629 and similarly, $\overline{RD}$ is brought low to read data from LM628/629. Data transfer is a two-byte operation written in most to least significant byte order. The above description assumes that $\overline{CS}$ is low.

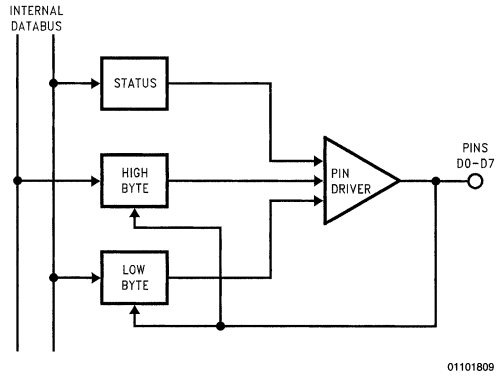


FIGURE 9. Host Interface Internal I/O Registers

3.6 HARDWARE BUSY BIT OPERATION

Before and between all command byte and data byte pair transfers, the busy bit must be read and checked to be at logic low. If the busy bit is set and commands are issued they will be ignored and if data is read it will be the current contents of the I/O buffer and not the expected data. The busy bit is set after the rising edge of the write signal for commands and the second rising edge of the respective read or write signal for two byte data transfers, *Figure 10*. The busy bit remains high for approximately 15 µs.

3.0 Profile Generation (Continued)

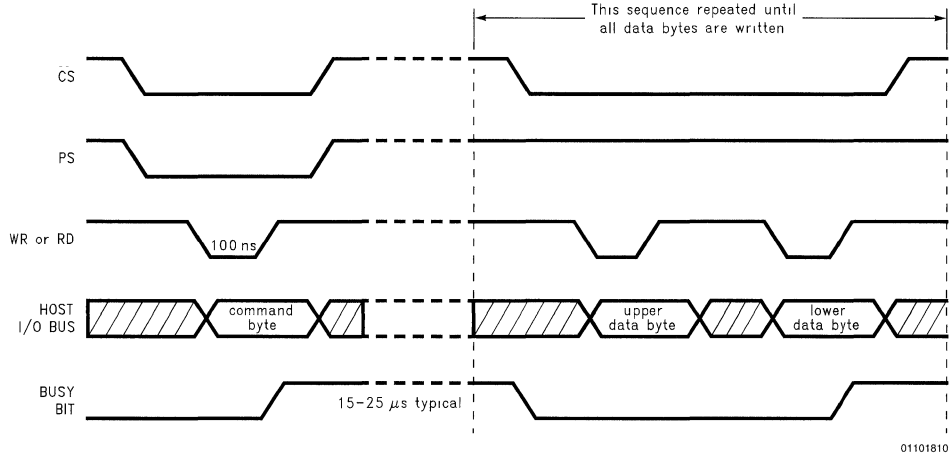


FIGURE 10. Busy Bit Operation during Command and Data Write Sequence

The busy bit reset to logic low indicates that high and low byte registers shown in *Figure 9* have been either loaded or read by the LM628/629 internal microcode. To service the command or data transfer this microcode which performs the trajectory and filter calculations is interrupted, except in critical areas, and the on-going calculation is suspended The microcode was designed this way to achieve minimum latency when communicating with the host. However, if this communication becomes too frequent and on-going calculations are interrupted too often corruption will occur. In a 256 μs sample interval, the filter calculation takes 50 μs, outputting a sample 10 μs and trajectory calculation 90 μs If the LM628 behaves in a manner that is unexpected the host communication rate should be checked in relation to these timings.

3.7 FILTER INITIAL VALUES AND TUNING

When connecting up a system for the first time there may be a possibility that the loop phasing is incorrect. As this may cause violent oscillation it is advisable to initially use a very low value of proportional gain, say $k_p = 1$ (with k_d, k_i and il all set to zero), which will provide a weak level of drive to the motor. (The Start command, STT, is sent to LM628/629 to close the control loop and energize the motor.) If the system does oscillate with this low value of k_p then the motor connections should be reversed.

Having determined that the loop phasing is correct k_p can be increased to a value of about 20 to see that the control system basically works. This value of k_p should hold the motor shaft reasonably stiffly, returning the motor to the set position, which will be zero until trajectory values have been input and a position move performed. If oscillation or unacceptable ringing occurs with a k_p value of 20 reduce this until it stops. Low values of acceleration and velocity can now be input, of around 100, and a position move commanded to say 1000 counts. All values suggested here are decimal. For details of loading trajectory and filter parameters see Section 3.0, reference (5) and the data sheet.

It is useful at this stage to try different values of acceleration and velocity to get a feel for the system limitations These can be determined by using the reporting commands of desired and actual position and velocity, to see if the error between desired and actual positions of the motor are constant and not increasing without bound. See Section 3.6 and the data sheet for information about the reporting commands. Clearly it will be difficult to tune for best system response if the motor and its load cannot achieve the demanded values of acceleration and velocity. When correct operation is confirmed and limiting values understood, filter tuning can commence.

Due to the basic difficulty of accurately modeling a control system, with the added problem of variations that can occur in mechanical components over time and temperature, it is always necessary at some stage to perform tuning empirically. Determining the PID filter coefficients by tuning is the preferred method with LM628/629 because of the inherent flexibility in changing the filter coefficients provided by this programmable device

Before tuning a control system the effect of each of the PID filter coefficients should be understood. The following is a very brief review, for a detailed understanding reference (2) should be consulted. The proportional coefficient, k_p, provides adjustment of the control system loop proportional gain, as this is increased the output steady state error is reduced. The error between the required and actual position is effectively divided by the loop gain. However there is a natural limitation on how far k_p can be increased on its own to reduce output position error because a reduction in phase margin is also a consequence of increasing k_p This is first encountered as ringing about the final position in response to a step change input and then instability in the form of oscillation as the phase margin becomes zero. To improve stability, k_d, the derivative coefficient, provides a damping effect by providing a term proportional to velocity in an-

3.0 Profile Generation (Continued)

tiphase to the ringing, or viewed in another way, adds some leading phase shift into the loop and increases the phase margin.

In the tuning process the coefficients k_p and k_d are iteratively increased to their optimum values constrained by the system constants and are trade-offs between response time, stability and final position error. When k_p and k_d have been determined the integral coefficient, k_i, can be introduced to remove steady state errors at the load. The steady state errors removed are the velocity lag that occurs with a constant velocity output and the position error due to a constant static torque. A value of integration limit, il, has to be input with k_i, otherwise k_i will have no effect. The integral coefficient k_i adds another variable to the system to allow further optimization, very high values of k_i will decrease the phase margin and hence stability, see Section 5 and reference (2) for more details. Reference (5) gives more details of PID filter tuning and how to load filter parameters.

Figure 11 illustrates how a relatively slow response with overshoot can be compensated by adjustment of the PID filter coefficients to give a faster critically damped response.

4.0 User Command Set

4.1 OVERVIEW

The following types of User Commands are available:

Initialization

Filter control commands

Trajectory control commands

Interrupt control commands

Data reporting commands

User commands are single bytes and have a varying number of accompanying data bytes ranging from zero to fourteen depending upon the command. Both filter and trajectory control commands use a double buffered scheme to input data. These commands load primary registers with multiple words of data which are only transferred into secondary working registers when the host issues a respective single byte user command. This allows data to be input before its actual use which can eliminate any potential communication bottlenecks and allow synchronized operation of multiple axes.

4.2 HOST-LM628/629 COMMUNICATION—THE BUSY BIT

Communication flow between the LM628/629 and its host is controlled by using a busy bit, bit 0, in the Status Byte. The busy bit must be checked to be at logic 0 by the host before commands and data are issued or data is read. This includes between data byte pairs for commands with multiple words of data.

4.3 LOADING THE TRAPEZOIDAL VELOCITY PROFILE GENERATOR

To initiate a motor move, trajectory generator values have to be input to the LM628/629 using the Load Trajectory Parameters, LTRJ, command. The command is followed by a trajectory control word which details the information to be loaded in subsequent data words. *Table 1* gives the bit allocations, a bit is set to logic 1 to give the function shown.

TABLE 1. Trajectory Control Word Bit Allocations

Bit Position	Function
Bit 15	Not Used
Bit 14	Not Used
Bit 13	Not Used
Bit 12	Forward Direction (Velocity Mode Only)
Bit 11	Velocity Mode
Bit 10	Stop Smoothly (Decelerate as Programmed)
Bit 9	Stop Abruptly (Maximum Deceleration)
Bit 8	Turn Off Motor (Output Zero Drive)
Bit 7	Not Used
Bit 6	Not Used
Bit 5	Acceleration Will Be Loaded
Bit 4	Acceleration Data Is Relative
Bit 3	Velocity Will Be Loaded
Bit 2	Velocity Data Is Relative
Bit 1	Position Will Be Loaded
Bit 0	Position Data Is Relative

Bits 0 to 5 determine whether any, all or none of the position, velocity or acceleration values are loaded and whether they are absolute values or values relative to those previously loaded. All trajectory values are 32-bit values, position values are both positive and negative. Velocity and acceleration are 16-bit integers with 16-bit fractions whose absolute value is always positive. When entering relative values ensure that the absolute value remains positive. The manual stop commands bits 8, 9 and 10 are intended to allow an unprogrammed stop in position mode, while a position move is in progress, perhaps by the demand of some external event, and to provide a method to stop in velocity mode. They do not specify how the motor will stop in position mode at the end of a normal position move. In position mode a programmed move will automatically stop with a deceleration rate equal to the acceleration rate at the target position. Setting a stop bit along with other trajectory parameters at the beginning of a move will result in no movement! Bits 8, 9 and 10 should only be set one at a time, bit 8 turns the motor off by outputting zero drive to the motor, bit 9 stops the motor at maximum deceleration by setting the target position equal to the current position and bit 10 stops the motor using the current user-programmed acceleration value. Bit 11 is set for operating in velocity mode and bit 12 is set for forward direction in velocity mode.

4.0 User Command Set (Continued)

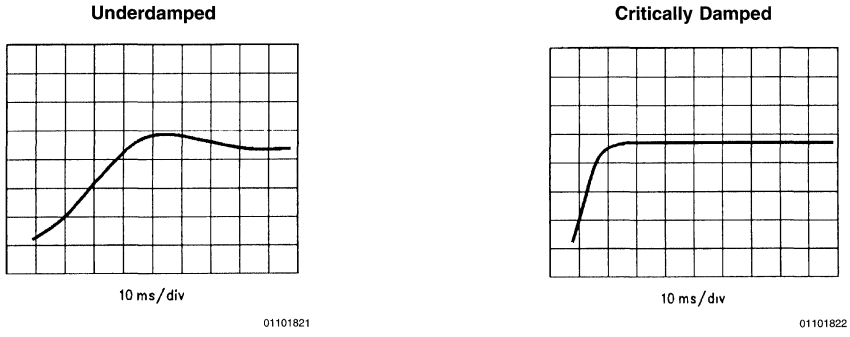


FIGURE 11. Position vs Time for 100 Count Step Input

Following immediately after the trajectory control word should be two 16-bit data words for each parameter specified to be loaded. These should be in the descending order of the trajectory control word bits, that is acceleration, velocity and position. They are written to the LM628/629 as two pairs of data bytes in most to least significant byte order. The busy bit should be checked between the command byte and the data byte pair forming the trajectory control word and the individual data byte pairs of the data. The Start command, STT, transfers the loaded trajectory data into the working registers of the double buffered scheme to initiate movement of the motor. This buffering allows any parameter, except acceleration, to be updated while the motor is moving by loading data with the LTRJ command and to be later executed by using the STT command.

New values of acceleration can be loaded with LTRJ while the motor is moving, but cannot be executed by the STT command until the trajectory has completed or the drive to the motor is turned off by using bit 8 of the trajectory control word. If acceleration has been changed and STT is issued while the drive to the motor is still present, a command error interrupt will be generated and the command ignored. Separate pairs of LTRJ and STT commands should be issued to first turn the motor off and then update acceleration. System operation when changing acceleration while the motor is moving, but with the drive removed, is discussed in Section 4.5.1.

4.4 LOADING PID FILTER COEFFICIENTS

PID filter coefficients are loaded using the Load Filter Parameters, LFIL, command and are the proportional coefficient k_p, derivative coefficient k_d and integral coefficient k_i. Associated with k_i, an integration limit, il, has to be loaded. This constrains the magnitude of the integration term of the PID filter to the il value, see Section 4 4.2. Associated with the derivative coefficient, a derivative sample rate can be chosen from $2048/f_{CLK}$ to $(2048 \times 256)/f_{CLK}$ in steps of $2048/f_{CLK}$, see Section 4.4.1.

The first pair of data bytes following the LFIL command byte form the filter control word. The most significant byte sets the derivative sample rate, the fastest rate, $2048/f_{CLK}$, being hex'00' the slowest rate $(2048 \times 256)/f_{CLK}$ being hex'FF'. The lower four bits of the least significant byte tell the LM628/629 which of the coefficients is going to be loaded, bit 3 is k_p, bit 2 is k_i, bit 1 is k_d and bit 0 is il. Each filter coefficient and the integration limit can range in value from hex'0000' to '7FFF', positive only. If all coefficient values are loaded then ten bytes of data, including the filter control word, will follow the LFIL command. Again the busy bit has to be checked between the command byte and filter control word and between data byte pairs. Use of new filter coefficient values by the LM628/629 is initiated by issuing the single byte Update Filter command, UDF.

When controlled movement of the motor has been achieved, by programming the filter and trajectory, attention turns to incorporating the LM628/629 into a system. Interrupt Control Commands and Data Reporting Commands enable the host microcontroller to keep track of LM628/629 activity.

4.5 INTERRUPT CONTROL COMMANDS

There are five commands that can be used to interrupt the host microcontroller when a predefined condition occurs and two commands that control interrupt operation. When the LM628/629 is programmed to interrupt its host, the event which caused this interrupt can be determined from bits 1 to 6 of the Status Byte (additionally bit 0 is the busy bit and bit 7 indicates that the motor is off) All the Interrupt Control commands are executable during motion.

The Mask Interrupts command, MSKI, is used to tell LM628/629 which of bits 1 to 6 will interrupt the host through use of interrupt mask data associated with the command. The data is in the form of a data byte pair, bits 1–6 of the least significant byte being set to logic 1 when an interrupt source is enabled. The Reset Interrupts command, $\overline{\text{RSTI}}$, resets interrupt bits in the Status Byte by sending a data byte pair, the least significant byte having logic 0 in bit positions 1 to 6 if they are to be reset.

Executing the Set Index Position command, SIP, causes bit 3 of the status byte to be set when the absolute position of the next index pulse is recorded in the index register. This can be read with the command, Read Index Position, RDIP.

Executing either Load Position Error for Interrupt, LPEI, or Load Position Error for Stopping, LPES, commands, sets bit 5 of the Status Byte when a position error exceeding a specified limit occurs. An excessive position error can indicate a serious system problem and these two commands give the option when this occurs of either interrupting the

4.0 User Command Set (Continued)

host or stopping the motor and interrupting the host. The excessive position is specified following each command by a data byte pair in most to least significant byte order.

Executing either Set Break Point Absolute, SBPA, or Set Break Point Relative, SBPR, commands, sets bit 6 of the status byte when either the specified, absolute or relative, breakpoint respectively is reached. The data for SBPA can be the full position range (hex'C0000000' to '3FFFFFFF') and is sent in two data byte pairs in most to least significant byte order. The data for the Set Breakpoint Relative command is also of two data byte pairs, but its value should be such that when added to the target position it remains within the absolute position range. These commands can be used to signal the moment to update the on-going trajectory or filter coefficients. This is achieved by transferring data from the primary registers, previously loaded using LTRJ or LFIL, to working registers, using the STT or UDF commands.

Interrupt bits 1, 2 and 4 of the Status Byte are not set by executing interrupt commands but by events occurring during LM628/629 operation as follows. Bit 1 is the command error interrupt, bit 2 is the trajectory complete interrupt and bit 4 is the wraparound interrupt. These bits are also masked and reset by the MSKI and $\overline{\text{RSTI}}$ commands respectively. The Status Byte still indicates the condition of interrupt bits 1–6 when they are masked from interrupting the host, allowing them to be incorporated in a polling scheme.

4.6 DATA REPORTING COMMANDS

Read Status Byte, RDSTAT, supported by a hardware register accessed via $\overline{\text{CS}}$, $\overline{\text{RD}}$ and $\overline{\text{PS}}$ control, is the most frequently used method of determining LM628/629 status. This is primarily to read the busy bit 0 while communicating commands and data as described in Section 3.2.

There are seven other user commands which can read data from LM628/629 data registers.

The Read Signals Register command, RDSIGS, returns a 16-bit data word to the host. The least-significant byte repeats the RDSTAT byte except for bit 0 which indicates that a SIP command has been executed but that an index pulse has not occurred. The most significant byte has 6 bits that indicate set-up conditions (bits 8, 9, 11, 12, 13 and 14). The other two bits of the RDSIGS data word indicate that the trajectory generator has completed its function, bit 10, and that the host interrupt output (Pin 17) has been set to logic 1, bit 15. Full details of the bit assignments of this command can be found in the data sheet.

The Read Index Position, RDIP, command reads the position recorded in the 32 bits of the index register in four data bytes. This command, with the SIP command, can be used to acquire a home position or successive values. These could be used, for example, for gross error checking.

Both on-going 32-bit position inputs to the summing junction can be read. Read desired position, RDDP, reads the current desired position the demand or "set point input" from the trajectory generator and Read Real Position, RDRP, reads the current actual position of the motor.

Read Desired Velocity, RDDV, reads the current desired velocity used to calculate the desired position profile by the trajectory generator. It is a 32-bit value containing integer and fractional velocity information. Read Real Velocity, RDRV, reads the instantaneous actual velocity and is a 16-bit integer value.

Read Integration-Term Summation Value, RDSUM, reads the accumulated value of the integration term. This is a 16-bit value ranging from zero to the current, il, integration limit value.

4.7 SOFTWARE EXAMPLE

The following example shows the flow of microcontroller commands needed to get the LM628/629 to control a simple motor move. As it is non-specific to any microcontroller pseudo commands $\overline{\text{WR}}$,XXXXH and RD,XXXXH with hex immediate data will be used to indicate read and write operations respectively by the host to and from the LM628/629. Decisions use IF..THEN..ELSE. BUSY is a user routine to check the busy bit in the Status Byte, WAIT is a user routine to wait 1.5 ms after hardware reset.

```
LABEL    MNEMONIC          :REMARK
Initialization:
         WAIT              :Routine to wait 1.5 ms after reset.
         RDSTAT            :Check correct RESET operation by reading the
                           :Status Byte. This should be either hex'84' or 'C4'
         IF Status byte not equal hex'84' or 'C4' THEN repeat
         hardware RESET
                            :Make decision concerning validity of RESET
```

Optionally the Reset can be further checked for correct operation as follows. It is useful to include this to reset all interrupt bits in the Status Byte before further action:

```
          MSKI              :Mask interrupts
          BUSY              :Check busy bit 0 routine
          WR, 0000H         :Host writes two zero bytes of data to
                            :LM628/629. This mask disables all interrupts.
          BUSY              :Check busy bit
          RSTI              :Reset Interrupts command
          BUSY              :Check busy bit
          WR, 0000H         :Host writes two zero bytes of data to LM628/629
          RDSTAT            :Status byte should read either hex'80' or 'C0'
          IF Status Byte not equal hex'80' or 'C0' THEN repeat
          hardware RESET
                            :
          IF Status Byte equal to hex'C0' THEN continue ELSE PORT
                            :
          BUSY              :Check busy bit
```

4.0 User Command Set (Continued)

```
            RSTI            :Reset Interrupts
            BUSY            :Check busy bit
            WR, 0000H       :Reset all interrupt bits
        Set Output Port Size for a 12-bit DAC.
        PORT    BUSY            :Check busy bit
            PORT12          :Sets LM628 output port to 12-bits
                             (Only for systems with 12-bit DAC)
        Load Filter Parameters
            BUSY            :Check busy bit
            LFIL            :Load Filter Parameters command
            BUSY            :Check busy bit
            WR, 0008H       :Filter Control Word
                            :    Bits 8 to 15 (MSB) set the derivative
                            :sample rate.
                            :    Bit 3    Loading kp data
                            :    Bit 2    Loading ki data
                            :    Bit 1    Loading kd data
                            :    Bit 0    Loading il data
                            :Choose to load kp only at maximum
                            :derivative sample rate then Filter Control
                            :Word = 0008H
            BUSY            :Check busy bit
            WR, 0032H       :Choose kp = 50, load data byte pair MS
                            :byte first
        Update Filter
            BUSY            :Check busy bit
            UDF             :
        Load Trajectory Parameters
            BUSY            :Check busy bit
            LTRJ            :Load trajectory parameters command.
            BUSY            :Check busy bit
            WR, 002AH       :Load trajectory control word:
                            :    See Table I
                            :Choose Position mode, and load absolute
                            :acceleration, velocity and position. Then
                            :trajectory control word = 002AH. This means
                            :6 pairs of data bytes should follow.
            BUSY            :Check busy bit
            WR, XXXXH       :Load Acceleration integer word MS byte first
            BUSY            :Check busy bit
            WR, XXXXH       :Load Acceleration fractional word MS byte first
            BUSY            :Check busy bit
            WR, XXXXH       :Load Velocity integer word MS byte first
            BUSY            :Check busy bit
            WR, XXXXH       :Load Velocity fractional word MS byte first
            BUSY            :Check busy bit

            WR, XXXXH       :Load Position MS byte pair first
            BUSY            :Check busy bit
            WR, XXXXH       :Load position LS byte pair
        Start Motion
            BUSY            :Check busy bit
            STT             :Start command
        Check for Trajectory complete.
            RDSTAT          :Check Status Byte bit 2 for trajectory
                            :complete
        Busy bit check routine
        BUSY    RDSTAT          :Read status byte
            If bit 0 is set THEN BUSY ELSE RETURN
            END
```

*Consult reference (5) for more information on programming the LM628/629.

4.0 User Command Set (Continued)

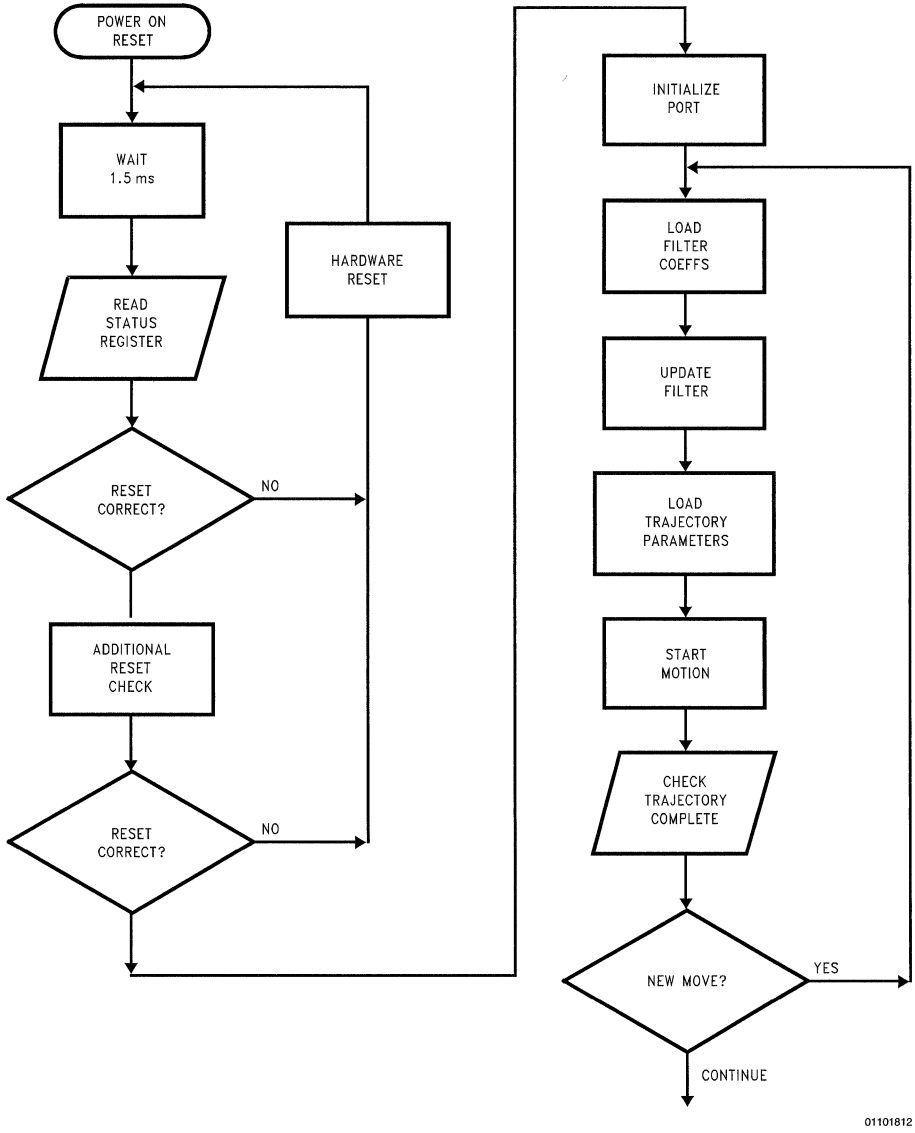


FIGURE 12. Basic Software Flow

5.0 Helpful User Ideas

5.1 GETTING STARTED

This section outlines the actions that are necessary to implement a simple motion control system using LM628/629. More details on how LM628/629 works and the use of the User Command Set are given in the sections "2.0 DEVICE DESCRIPTION" and "3.0 USER COMMAND SET".

5.2 HARDWARE

The following hardware connections need to be made:

5.2.1 Host Microcontroller Interface

Interface to the host microcontroller is via an 8-bit command/data port which is controlled by four lines. These are the conventional chip select $\overline{CS}$, read $\overline{RD}$, write $\overline{WR}$ and a line called Port Select $\overline{PS}$, see *Figure 13*. $\overline{PS}$ is used to select

5.0 Helpful User Ideas (Continued)

user Command or Data transfer between the LM628/629 and the host. In the special case of the Status Byte (RDSTAT) bringing $\overline{PS}$, $\overline{CS}$ and $\overline{RD}$ low together allows access to this hardware register at any time. An optional interrupt line, HI, from the LM628/629 to the host can be used A microcontroller output line is necessary to control the LM628/629 hardware reset action.

5.2.2 Position Encoder Interface

The two optical incremental position encoder outputs feed into the LM628/629 quadrature decoder TTL inputs A and B. The leading phase of the quadrature encoder output defines the forward direction of the motor and should be connected to input A. Optionally an index pulse may be used from the position encoder. This is connected to the $\overline{IN}$ input, which should be tied high if not used, see *Figure 13*.

5.2.3 Output Interface

LM628 has a parallel output of either 8 or 12 bits, the latter is output as two multiplexed 6-bit words. *Figure 14* illustrates how a motor might be driven using a LM12 power linear amplifier from the output of 8-bit DAC0800.

LM629 has a sign and magnitude PWM output, *Figure 13*, of 7-bit resolution plus sign. *Figure 15* shows how the LM629 sign and magnitude outputs can be used to control the outputs of an LM18293 quad half-H driver. The half-H drivers are used in pairs, by using 100 mΩ current sharing resistors, and form a full-H bridge driver of 2A output. The sign bit is used to steer the PWM LM629 magnitude output to either side of the H-bridge lower output transistors while holding the upper transistors on the opposite side of the H-bridge continuously on.

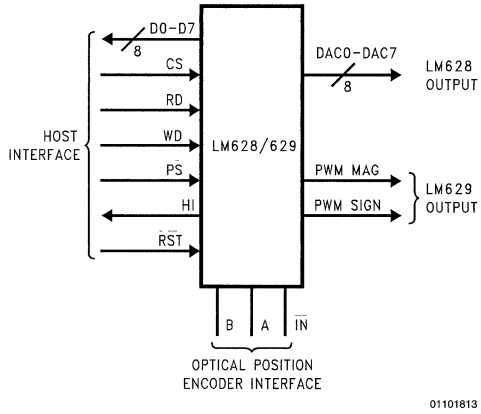


FIGURE 13. LM628 and LM629 Host, Output and Position Encoder Interfaces

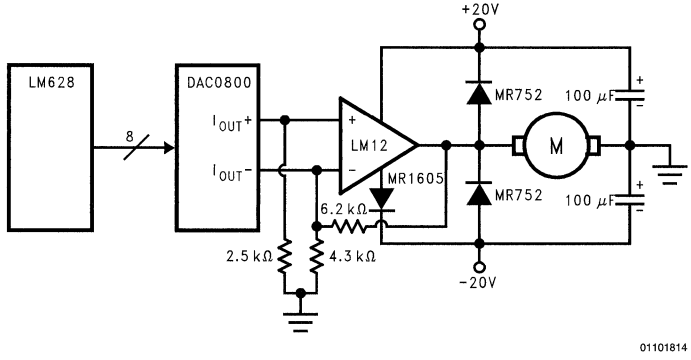


FIGURE 14. LM628 Example of Linear Motor Drive Using LM12

5.0 Helpful User Ideas (Continued)

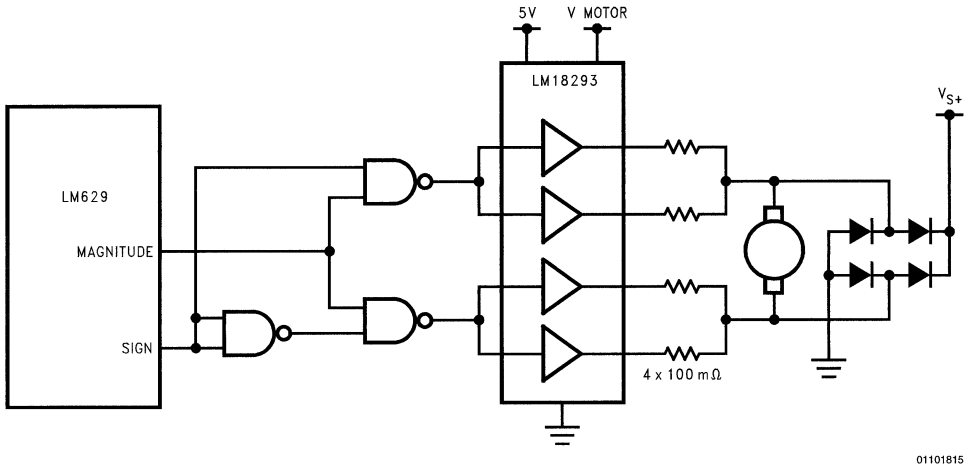


FIGURE 15. LM629 H-Bridge Motor Drive Example Using LM18293

5.3 SOFTWARE

Making LM628/629 perform a motion control function requires that the host microcontroller, after initializing LM628/629, loads coefficients for the PID filter and then loads trajectory information. The interrupt and data reporting commands can then be used by the host to keep track of LM628/629 actions. For detailed descriptions see the LM628/629 data sheet and Section 3.

5.4 INITIALIZATION

There is only one initialization operation that must be performed; a check that hardware reset has operated correctly. If required, the size of the LM628 output port should be configured. Other operations which might be part of user's system initialization are discussed under Interrupt and Data Reporting commands, Sections 3.5 and 3.6.

5.4.1 Initializing LM628 Output Port

Reset sets the LM628 output port size to 8 bits. If a 12-bit DAC is being used, then the output port size is set by the use of the PORT12 command.

5.4.2 Hardware RESET Check

The hardware reset is activated by a logic low pulse at pin 27, $\overline{RST}$, from the host of greater than 8 clock cycles. To ensure that this reset has operated correctly the Status Byte should be checked immediately after the reset pin goes high, it should read hex'00'. If the reset is successful this will change to hex'84' or 'C4' within 1.5 ms. If not, the hardware reset and check should be repeated. A further check can be used to make certain that a reset has been successful by using the Reset Interrupts command, RSTI. Before sending the RSTI, issue the Mask Interrupts command, MSKI, and mask data that disables all interrupts, this mask is sent as two bytes of data equaling hex'0000'. Then issue the RSTI command plus mask data that resets all interrupts, this equals hex'0000' and is again sent as two bytes. Do not forget to check the busy bit between the command byte and data byte pairs. When the chip has reset properly the status byte will change from hex'84' or 'C4' to hex'80' or 'C0'.

5.4.3 Interrupt Commands

Optionally the commands which cause the LM628/629 to take action on a predefined condition (e.g., SIP, LPEI, LPES, SBPA and SBPR) can be included in the initialization, these are discussed under Interrupt Commands.

5.5 PERFORMANCE REFINEMENTS

5.5.1 Derivative Sample Rate

The derivative sample interval is controllable to improve the stability of low velocity, high inertia loads. At low speeds, when fractional counts for velocity are used, the integer position counts, desired and actual, only change after several sample intervals of the LM628/629 ($2048/f_{CLK}$). This means that for sample intervals between integer count changes the error voltage will not change for successive samples. As the derivative term, k_d, multiplies the difference betweeen the previous and current error values, if the derivative sample interval is the same as the sample interval, several consecutive sample intervals will have zero derivative term and hence no damping contribution. Lengthening the derivative sample interval ensures a more constant derivate term and hence improved stability. Derivative sample interval is loaded with the filter coefficient values as the most significant byte of the LFIL control word everytime the command is used, the host therefore needs to store the current value for re-loading at times of filter coefficient change.

5.5.2 Integral Windup

Along with the integral filter coefficient, k_i, an integration limit, il, has to be input into LM628/629 which allows the user to set the maximum value of the integration term of equation (3), Section 5.2.2. This term is then able to accumulate up to

5.0 Helpful User Ideas (Continued)

the value of the integration limit and any further increase due to error of the same sign is ignored. Setting the integration limit enables the user to prevent an effect called "Integral Windup". For example, if an LM628/629 attempts to accelerate a motor at a faster rate than it can achieve, a very large integral term will result. When the LM628/629 tries to stop the motor at the target position the large accumulated integral term will dominate the filter and cause the motor to badly overshoot, and thus integral windup has occurred.

5.5.3 Profiles Other Than Trapezoidal

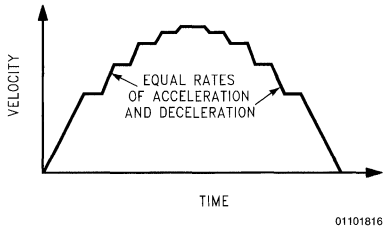


FIGURE 16. Generating a Non-Trapezoidal Profile

If it is required to have a velocity profile other than trapezoidal, this can be accomplished by breaking the profile into small pieces each of which is part of a small trapezoid. A piecewise linear approximation to the required profile can then be achieved by changing the maximum velocity before the trapezoid has had time to complete, see *Figure 16*.

5.5.4 Synchronizing Axes

For controlling tightly coupled coordinated motion between multiple-axes, synchronization is required. The best possible synchronization that can be achieved between multiple LM628/629 is within one sample interval, ($2048/f_{CLK}$, 256 µs for an 8 MHz clock, 341 µs for a 6 MHz clock). This is achieved by using the pipeline feature of the LM628/629 where all controlled axes are loaded individually with trajectory values using the LTRJ command and then simultaneously given the start command STT PID filter coefficients can be updated in a similar manner using LFIL and UDF commands.

5.6 OPERATING CONSTRAINTS

5.6.1 Updating Acceleration on the Fly

Whereas velocity and target position can be updated while the motor is moving, on the "fly", the algorithm described in Section 2.5 prevents this for acceleration. To change acceleration while the motor is moving in mid-trajectory the motor off command has to be issued by setting LTRJ command bit 8. Then the new acceleration can be loaded, again using the LTRJ command. When the start command STT is issued the motor will be energized and the trajectory generator will start generating a new profile from the actual position when the STT command was issued. In doing this the trajectory generator will assume that the motor starts from a stationary position in the normal way. If the motor has sufficient inertia and is still moving when the STT command is issued then the control loop will attempt to bring the motor on to the new profile, possibly with a large error value being input to the PID filter and a consequential saturated output until the motor velocity matches the profile This is a classic case of overload in a feedback system. It will operate in an open loop manner until the error input gets within controllable bounds and then the feedback loop will close. Performance in this situation is unpredictable and application specific. LM628/629 was not intentionally designed to operate in this way.

5.6.2 Command Update Rate

If an LM628/629 is updated too frequently by the host it will not keep up with the commands given. The LM628/629 aborts the current trajectory calculation when it receives a new STT command, resulting in the output staying at the value of the previous sample. For this reason it is recommended that trajectory is not updated at a greater rate than once every 10 ms.

6.0 Theory

6.1 PID FILTER

6.1.1 PID Filter in the Continuous Domain

The LM628/629 uses a PID filter as the loop compensator, the expression for the PID filter in the continuous domain is:

$$H(s) = K_p + K_i/s + K_d s \quad (1)$$

Where K_p = proportional coefficient

K_i = integral coefficient

K_d = derivative coefficient

6.0 Theory (Continued)

6.1.2 PID Filter Bode Plots

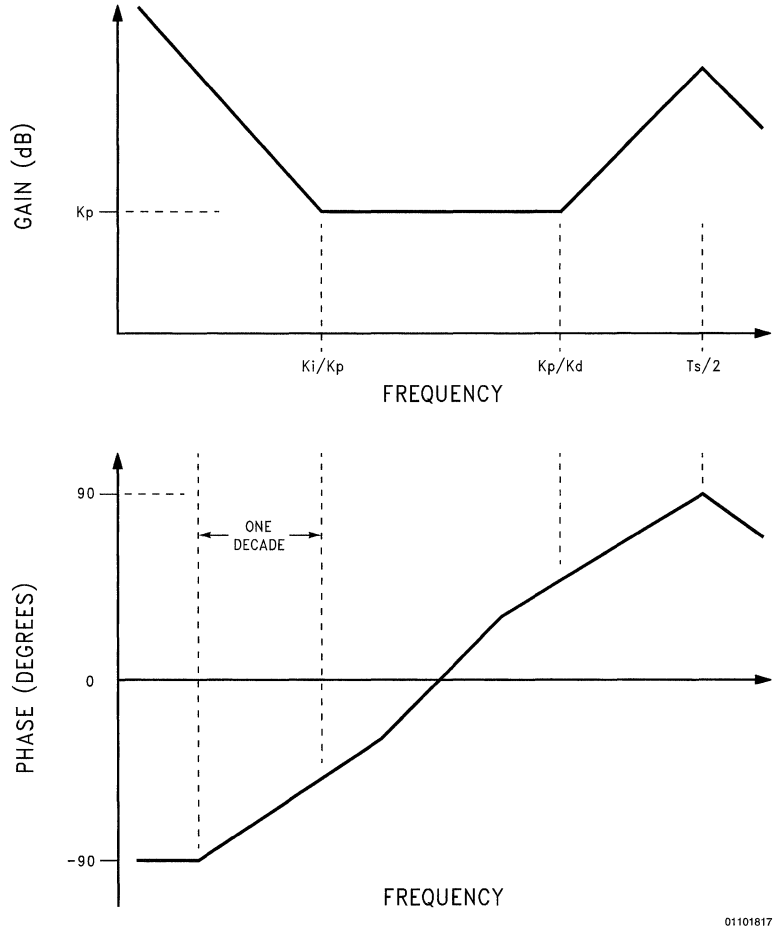


FIGURE 17. Bode Plots of PID Transfer Function

The Bode plots for this function (shown in *Figure 17*) show the effect of the individual terms of *Equation (1)*. The proportional term, K_p provides adjustment of proportional gain. The derivative term K_d increases the system bandwidth but more importantly adds leading phase shift to the control loop at high frequencies. This improves stability by counteracting the lagging phase shift introduced by other control loop components such as the motor. The integral term, K_i, provides a high DC gain which reduces static errors, but introduces a lagging phase shift at low frequencies. The relative magnitudes of K_d, K_i and loop proportional gain have to be adjusted to achieve optimum performance without introducing instability.

6.2 PID FILTER COEFFICIENT SCALING FACTORS FOR LM628/629

While the easiest way to determine the PID filter coefficient k_p, k_d, and k_i values is to use tuning as described in Section 2.11, some users may want to use a more theoretical approach to at least find initial starting values before fine tuning. As very often this analysis is performed in the continuous (s) domain and transformed into the discrete digital domain for implementation, the relationship between the continuous domain coefficients and the values input into LM628/629 is of interest.

6.0 Theory (Continued)

6.2.1 PID Filter Difference Equation

In the discrete domain, *Equation (1)* becomes the difference equation:

$$u(n) = K_p e(n) + K_i T \sum_{n=0}^{N} e(n) + K_d/T_s[e(n) - e(n-1)] \quad (2)$$

Where:

T is the sample interval $2048/f_{CLK}$

T_s is the derivative sample interval ($2048/f_{CLK}$ x (1..255)

6.2.2 Difference Equation with LM628/629 Coefficients

In terms of LM628/629 coefficients, *Equation (2)* becomes:

$$u(n) = k_p e(n) + k_i \sum_{n=0}^{N} e(n) + k_d[e(n') - e(n'-0)] \quad (3)$$

Where:

k_p, k_i and k_d are the discrete-time LM628/629 coefficients

e(n) is the position error at sample time n

n' indicates sampling at the derivative sampling rate.

The error signal e(n) [or e(n')] is a 16-bit number from the output of the summing junction and is the input to the PID filter. The 15-bit filter coefficients are respectively multiplied by the 16-bit error terms as shown in *Equation (3)*A to produce 32-bit products.

6.2.3 LM628/629 PID Filter Output

The proportional coefficient k_p is multiplied by the error signal directly. The error signal is continually summed at the sample rate to previously accumulated errors to form the integral signal and is maintained to 24 bits. To achieve a more usable range from this term, only the most significant 16 bits are used and multiplied by the integral coefficient, k_i. The absolute value of this product is compared with the integration limit, il, and the smallest value, appropriately signed, is used. To form the derivative signal, the previous error is subtracted from the current error over the derivative sampling interval. This is multiplied by the derivative coefficient k_d and the product contributes every sample interval to the output independently of the user chosen derivative sample interval.

The least significant 16 bits of the 32-bit products from the three terms are added together to produce the resulting u(n) of *Equation (3)* each sample interval. From the PID filter 16-bit result, either the most significant 8 or 12 bits are output, depending on the output word size being used. A consequence of this and the use of the 16 MSB's of the integral signal is a scaling of the filter coefficients in relation to the continuous domain coefficients.

6.2.4 Scaling for k_p and k_d

Figure 18 gives details of the multiplication and output for k_p and k_d. Taking the output from the MS byte of the LS 16 bits of the 32-bit result register causes an effective 8-bit right-shift or division of 256 associated with k_p and k_d as follows:

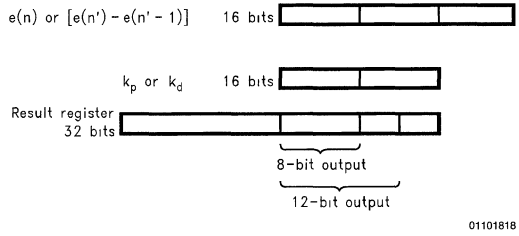


FIGURE 18. Scaling of k_p and k_d

Result = k_p x e(n)/256 = K_px e(n) .'. k_p
= 256 x K_p.

Similarly for k_d:

Result = (k_d x [e(n') – e(n'–1)])/256
= K_d/T_s x e(n) .'. k_d = 256 x K_d/T_s

Where T_s is the derivative sampling rate.

6.2.5 Scaling for k_i

Figure 19 shows the multiplication and output for the integral term k_i. The use of a 24-bit register for the error terms summation gives further scaling:

Result = k_i/256 x > e(n)/256
= K_i x T .'. k_i = 65536 K_i x T.

Where T is the sampling interval $2048/f_{CLK}$.

For a 12-bit output the factors are:

k_p = 16 x K_p, k_d = 16 x K_d/T_s and k_i = 4096 K_i x T.

If the 32-bit result register overflows into the most significant 16-bits as a result of a calculation, then all the lower bits are set high to give a predictable saturated output.

6.3 AN EXAMPLE OF A TRAJECTORY CALCULATION

Problem: Determine the trajectory parameters for a motor move of 500 revolutions in 1 minute with 15 seconds of acceleration and deceleration respectively. Assume the optical incremental encoder used has 500 lines.

The LM628/629 quadrature decoder gives four counts for each encoder line giving 2000 counts per revolution in this example. The total number of counts for this position move is 2000 x 500 = 1,000,000 counts.

By definition, average velocity during the acceleration and deceleration periods, from and to zero, is half the maximum

6.0 Theory (Continued)

velocity. In this example, half the total time to make the move (30 seconds) is taken by acceleration and deceleration. Thus in terms of time, half the move is made at maximum velocity and half the move at an average velocity of half this maximum. Therefore, the combined distance traveled during acceleration and deceleration is half that during maximum velocity or ⅓ of the total, or 333,333 counts. Acceleration and deceleration takes 166,667 counts respectively.

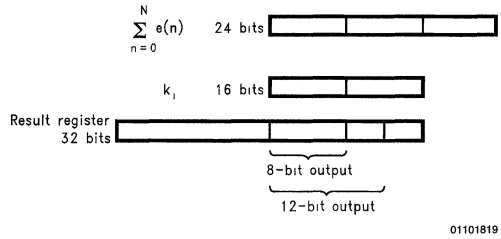


FIGURE 19. Scaling for k_i

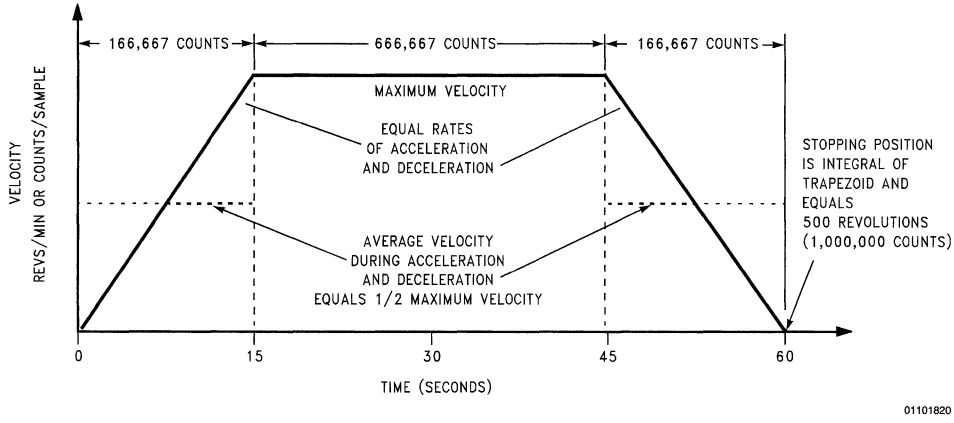


FIGURE 20. Trajectory Calculation Example Profile

The time interval used by the LM628/629 is the sample interval which is 256 µs for a f_{CLK} of 8 MHz.

The number of sample periods in 15 seconds = 15s/ 256 µs = 58,600 samples

Remembering that distance s = $at^2/2$ is traveled due to acceleration 'a' and time 't'.

Therefore acceleration a = $2S/t^2$

= 2 x 166,667/58,600

= 97.1 x 10^{-6} counts/sample ^{2}

Acceleration and velocity values are entered into LM628/629 as a 32-bit integer double-word but represents a 16-bit integer plus 16-bit fractional value. To achieve this acceleration and velocity decimal values are scaled by 65536 and any remaining fractions discarded. This value is then converted to hex to enter into LM628 in four bytes.

Scaled acceleration a = 97.1 x 10^{-6}x 65536

= 6.36 decimal = 00000006 hex.

The maximum velocity can be calculated in two ways, either by the distance in counts traveled at maximum velocity divided by the number of samples or by the acceleration multiplied by the number of samples over acceleration duration, as follows:

Velocity = 666,667/117,200 = 97.1 x 10^{-6} x 58,600

= 5.69 counts/sample

Scaled by 65536 becomes 372,899.8 decimal = 0005B0A3 hex.

Inputting these values for acceleration and velocity with the target position of 1,000,000 decimal, 000F4240 hex will achieve the desired velocity profile.

7.0 Questions and Answers

7.1 THE TWO MOST POPULAR QUESTIONS

Why doesn't the motor move, I've loaded filter parameters, trajectory parameters and issued Update Filter, UDF, and Start, STT, commands?

Answer: The most like cause is that a stop bit (one of bits 8, 9 or 10 of the trajectory control word) has been set in error,

7.0 Questions and Answers

(Continued)

supposedly to cause a stop in position mode. This is unnecessary, in position mode the trajectory stops automatically at the target position, see Section 3.3.

Can acceleration be changed on the fly?

Answer: No, not directly and a command error interrupt will be generated when STT is issued if acceleration has been changed. Acceleration can be changed if the motor is turned off first using bit 8 of the Load Trajectory Parameter, LTRJ, trajectory control word, see Section 4.6.1.

7.2 MORE ON ACCELERATION CHANGE

What happens at restart if acceleration is changed with the motor drive off and the motor is still moving?

Answer: The trajectory generation starting position is the actual position when the STT command is issued, but assumes that the motor is stationary. If the motor is moving the control loop will attempt to bring the motor back onto an accelerating profile, producing a large error value and less than predictable results. The LM628/629 was not designed with the intention to allow acceleration changes with moving motors.

Is there any way to change acceleration?

Answer: Acceleration change can be simulated by making many small changes of maximum velocity. For instance if a small velocity change is loaded, using LTRJ and STT commands, issuing these repeatedly at predetermined time intervals will cause the maximum velocity to increment producing a piecewise linear acceleration profile. The actual acceleration between velocity increments remains the same.

7.3 MORE ON STOP COMMANDS

What happens if the on-going trajectory is stopped by setting LTRJ control word bits 9 or 10, stop abruptly or stop smoothly, and then restarted by issuing Start, STT?

Answer: While stopped the motor position will be held by the control loop at the position determined as a result of issuing the stop command. Issuing STT will cause the motor to restart the trajectory toward the original target position with normal controlled acceleration.

What happens if the on-going trajectory is stopped by setting LTRJ control word bit 8, motor-off?

Answer: The LM628's DAC output is set to mid-scale, this puts zero volts on the motor which will still have a dynamic braking effect due to the commutation diodes. The LM629's PWM output sets the magnitude output to zero with a similar effect. If the motor freewheels or is moved the desired and actual positions will be the same. This can be verified using the RDDP and RDRP commands. When Start, STT, is issued the loop will be closed again and the motor will move toward the original trajectory from the actual current position.

If the motor is off, how can the control loop be closed and the motor energized?

Answer: Simply by issuing the Start, STT command. If any previous trajectory has completed then the motor will be held in the current position. If a trajectory was in progress when the motor-off command was issued then the motor will restart and move to the target position in position mode, or resume movement in velocity mode.

7.4 MORE ON DEFINE HOME

What happens if the Define Home command, DFH, is issued while a current trajectory is in progress?

Answer: The position where the DFH command is issued is reset to zero, but the motor still stops at the original position commanded, i.e., the position where DFH is issued is subtracted from the original target position.

Does issuing Define Home, DFH, zero both the trajectory and position register?

Answer: Yes, use Read Real Position, RDRP, and Read Desired Position, RDDP to verify.

7.5 MORE ON VELOCITY

Why is a command error interrupt generated when inputting negative values of relative velocity?

Answer: Because the negative relative velocity would cause a negative absolute velocity which is not allowed. Negative absolute values of velocity imply movement in the negative direction which can be achieved by inputting a negative position value or in velocity mode by not setting bit 12. Similarly negative values of acceleration imply deceleration which occurs automatically at the acceleration rate when the LM628/629 stops the motor in position mode or if making a transition from a higher to a lower value of velocity.

What happens in velocity (or position) mode when the position range is exceeded?

Answer: The position range extends from maximum negative position hex'C0000000' to maximum positive position hex'3FFFFFFF' using a 32-bit double word. Bit 31 is the direction bit, logic 0 indicates forward direction, bit 30 is the wraparound bit used to control position over-range in velocity (or position) mode.

When the position increases past hex'3FFFFFFF' the wraparound bit 30 is set, which also sets the wraparound bit in the Status byte bit 4. This can be polled by the host or optionally used to interrupt the host as defined by the MSKI commands. Essentially the host has to manage wraparound by noting its occurrence and resetting the Status byte wraparound bit using the RSTI command. When the wraparound bit 30 is set in the position register so is the direction bit. This means one count past maximum positive position hex'3FFFFFFF' moves the position register onto the maximum negative position hex'C0000000'. Continued increase in positive direction causes the position register to count up to zero and back to positive values of position and on toward another wraparound.

Similarly when traveling in a negative direction, using two's complement arithmetic, position counts range from hex'FFFFFFF' (–1 decimal) to the maximum negative position of hex'C0000000'. One more negative count causes the position register to change to hex'3FFFFFFF', the maximum positive position. This time the wraparound bit 30 is reset, causing the wraparound bit 4 of the status byte to be set. Also the direction bit 31 is reset to zero. Further counts in the negative direction cause the position register to count down to zero as would be expected. With management there is no reason why absolute position should be lost, even when changing between velocity and position modes.

7.0 Questions and Answers

(Continued)

7.6 MORE ON USE OF COMMANDS

If filter parameter and trajectory commands are pipelined for synchronization of axes, can the Update Filter, UDF, and Start, STT, commands be issued consecutively?

Answer: Yes.

Can commands be issued between another command and its data?

Answer: No.

What is the response time of the set breakpoint commands, SBPA and SBPR?

Answer: There is an uncertainty of one sample interval in the setting of the breakpoint bit 6 in the Status Byte in response to these commands.

What happens when the Set Index Position, SIP, command is issued?

Answer: On the next occurrence of all three inputs from the position encoder being low the corresponding position is loaded into the index register. This can be read with the Read Index Position command, RDIP. Bit 0 of the Read Signals register, shows when an SIP command has been issued but the index position has not yet been acquired. RDSIGS command accesses the Read Signals Register.

What happens if the motor is not able to keep up with the specified trajectory acceleration and velocity values?

Answer: A large, saturated, position error will be generated, and the control loop will be non-linear. The acceleration and velocity values should be set within the capability of the motor. Read Desired and Real Position commands, RDDP and RDRP can be used to determine the size of the error. The Load Position Error commands, for either host Interrupt or motor Stopping, LPEI and LPES, can be used to monitor the error size for controlled action where safety is a factor.

When is the command error bit 1 in the Status Byte set?

Answer:

1. When an acceleration change is attempted when the motor is moving and the drive on.
2. When loading a relative velocity would cause a negative absolute velocity.
3. Incorrect reading and writing operations generally.

What does the trajectory complete bit 2 in the Status Byte indicate?

Answer: That the trajectory loaded by LTRJ and initiated by STT has completed. The motor may or may not be at this position. Bit 2 is also set when the motor stop commands are executed and completed.

What do the specified minimum and maximum values of velocity mean in reality?

Answer: Assume a 500 line encoder = 1/2000 revs/count is used.

The maximum LM628/629 velocity is 16383 counts/sample and for a 8 MHz clock the LM628/629 sample rate is 3.9k samples/second, multiplying these values gives 32k revs/second or 1.92M rpm.

The maximum encoder rate is 1M counts/second multiplied by 1/2000 revs/count gives 500 revs/second or 30k rpm. The encoder capture rate therefore sets the maximum velocity limit.

The minimum LM628/629 velocity is 1/65536 counts/sample (one fractional count), multiplying this value by the sample rate and encoder revs/count gives 30×10^{-6} revs/second or 1.8×10^{-3} rpm.

The LM628 provides no limitation to practical values of velocity.

How long will it take to get to position wraparound in velocity mode traveling at 5000 rpm with a 500 line encoder?

Answer: 107 minutes.

8.0 References and Further Reading

1. LM628/LM629 Precision Motion Controller. Data sheet March 1989.
2. Automatic Control Systems. Benjamin C. Kuo. Fifth edition Prentice-Hall 1987.
3. DC Motors, Speed Controls, Servo Systems. Robbins & Myers/Electro Craft.
4. PID Algorithms and their Computer Implementation. D.W. Clarke. Institute of Measurement and Control, Trans. v. 6 No. 6 Oct/Dec 1984 86/178.
5. LM628 Programming Guide. Steven Hunt. National Semiconductor Application Note AN-693.

LM2825 Application Information Guide

National Semiconductor
Application Note 1038
Luc Van de Perre

Introduction

The LM2825 is a complete 1A DC-DC buck converter packaged in a 24-lead molded dual-in-line integrated circuit package.

Contained within the package are all the active and passive components for a high efficiency step-down (buck) switching regulator. Available in fixed output voltages of 3.3V, 5V, 12V and adjustable version, these devices can provide up to 1A of load current with fully guaranteed electrical specifications.

This application note is intended to provide the user of this device with all the information and applications necessary to use the part in its fullest extent.

The following topics are covered:

- Pin functions
- Input capacitor selection
- Output ripple voltage and transients
- Start-up considerations including use of $\overline{\text{Shutdown}}$/Soft-start feature
- Application circuits
- Thermal considerations and board layout

Pin Functions (See *Figure 1*)

Input (pin 16–21)—This is the positive input supply for the switching regulator. If the main bypass capacitor is more than 6 inches away from the device, a suitable input bypass capacitor must be present at this pin to minimize voltage transients and to supply the switching currents needed by the regulator. See additional information in "Input Capacitor Selection" section.

Ground (pin 1, 2, 11, 12, 23)—Circuit ground. See additional information in "Thermal Considerations and Board Layout" section.

Output (pin 4–8)—This is the regulated positive output from the switching regulator. See additional information in "Output Ripple Voltage and Transient" and "Thermal Considerations and Board Layout" section.

$\overline{\text{Shutdown}}$/Soft-start (pin 13, 14)—This dual function pin provides the following features: (a) Allows the switching regulator circuit to be shut down using logic level signals thus dropping the total input supply current to approximately 65 µA. (b) Adding a capacitor to this pin provides a Soft-start feature which minimizes startup current and provides a controlled ramp up of the output voltage. See additional information in "Start-up Considerations including use of $\overline{\text{Shutdown}}$/Soft-start feature" section.

NC (Do not use) (pin 3, 9, 10, 15, 22, 24)—These pins should remain electrically isolated. Do not connect any signal to these pins. The only reason to connect these pins to the PCB is for reduced thermal resistance. See additional information in "Thermal Considerations and Board Layout" section.

Special Note: If the $\overline{\text{Shutdown}}$/Soft-start feature is not used, the pin should be left open. The internal pull-up current will make sure that the device is ON.

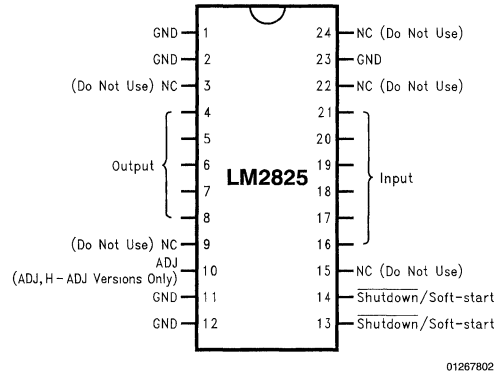


FIGURE 1. Connection Diagram

Input Capacitor Selection

If the package is more than 6" away from the main filter or bypass capacitor, a low ESR (Equivalent Series Resistance) aluminum or tantalum input capacitor is required between the input pin and ground pin. This input capacitor prevents large voltage transients from appearing at the input, and provides the instantaneous current needed each time the switch turns on.

The important parameters for the input capacitor are the voltage rating and the RMS current rating. Because of the relatively high RMS currents flowing in a buck regulator's input capacitor, this capacitor should be chosen for its RMS current rating rather than its capacitance or voltage ratings, although the capacitance value and voltage rating are directly related to the RMS current rating.

The RMS current rating of a capacitor could be viewed as a capacitor's power rating. The RMS current flowing through the capacitor's internal ESR produces power which causes the internal temperature of the capacitor to rise. The RMS current rating of a capacitor is determined by the amount of current required to raise the internal temperature approximately 10°C above an ambient temperature of 105°C. The ability of the capacitor to dissipate this heat to the surrounding air will determine the amount of current the capacitor can safely sustain. Capacitors that are physically large and have a large surface area will typically have higher RMS current ratings. For a given capacitor value, a higher voltage electrolytic capacitor will be physically larger than a lower voltage capacitor, which will allow it to dissipate more heat to the surrounding air, and therefore will have a higher RMS current rating.

The consequences of operating an electrolytic capacitor above the RMS current rating is a shortened operating life. The higher temperature speeds up the evaporation of the capacitor's electrolyte, resulting in eventual failure.

Input Capacitor Selection (Continued)

Selecting an input capacitor requires consulting the manufacturer's data sheet for maximum allowable RMS ripple current. For a maximum ambient temperature of 40˚C, a general guideline would be to select a capacitor with a ripple current rating of approximately 50% of the DC load current. For ambient temperatures up to 70˚C, a current rating of 75% of the DC load current would be a good choice for a conservative design. If you want a more accurate number for the current rating, you can use the following formulas:

$$I_{CAP\ RMS} = \sqrt{D \cdot \left(I_{OUT}^{2} - D * I_{OUT}^{2} + \frac{\Delta I_{LOAD}^{2}}{12}\right)}$$

$$\Delta I_{LOAD} = \frac{(V_{IN} - V_{SAT})\,D}{10.2}$$

$$D = \frac{(V_{OUT} - V_{D})}{(V_{IN} - V_{SAT}) + (V_{OUT} + V_{D})}$$

$$V_{D} = 0.5V \quad V_{SAT} = 1V$$

The capacitor voltage rating must be at least 1.25 times greater than the maximum input voltage, and often a much higher voltage capacitor is needed to satisfy the RMS current requirements.

The graph shown in *Figure 2* shows the relationship between a electrolytic capacitor value, its voltage rating, and the RMS current it is rated for. These curves were obtained from the Nichicon series of low ESR, high reliability electrolytic capacitors designed for switching regulator applications. Other capacitor manufacturers offer similar types of capacitors.

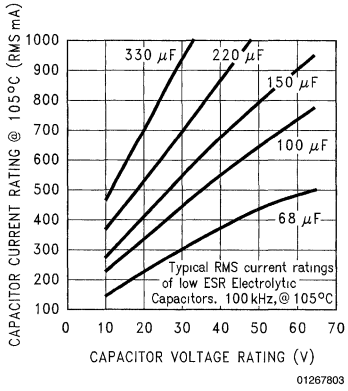


FIGURE 2. RMS Current Ratings for Low ESR Electrolytic Capacitors (typical)

Standard electrolytic capacitors typically have much higher ESR values, lower RMS current ratings and typically have a shorter operating lifetime, compared to low ESR electrolytic capacitors.

Surface mount solid tantalum capacitors are often used for input bypassing, because of their small size and excellent performance. However, several precautions must be observed. A small percentage of solid tantalum capacitors can short if the inrush current rating is exceeded. High dV/dt applied at the input can cause excessive charge current through low ESR tantalum capacitors. This high charge current can result in shorting within the capacitor. Several capacitor manufacturers do a 100% surge current testing on their products to minimize this potential problem. If high start-up currents are expected, it may be necessary to limit this current by adding either some resistance or inductance before the tantalum capacitor, or select a higher voltage capacitor. As with aluminum electrolytic capacitors, the RMS ripple current rating must be sized to the load current.

An aluminum electrolytic capacitor's ESR value is related to the capacitance value and its voltage rating. In most cases, higher voltage electrolytic capacitors have lower ESR values (see *Figure 3*). To provide the low ESR values and the high RMS current ratings, a high voltage capacitor may be needed.

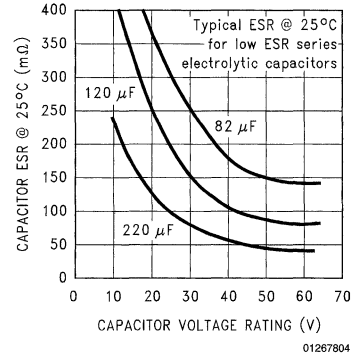


FIGURE 3. Capacitor ESR vs Capacitor Voltage Rating (Typical Low ESR Electrolytic Capacitor)

Electrolytic capacitors are not recommended for temperatures below −25˚C. The ESR rises dramatically at cold temperatures and typically rises 3X @ −25˚C and as much as 10X at −40˚C (see *Figure 4*). Fortunately, in an application circuit, the current flowing through the capacitor will warm up the capacitor, so the ESR will decrease somewhat.

Solid tantalum capacitors have a much better ESR for cold temperatures and are recommended for temperatures below −25˚C.

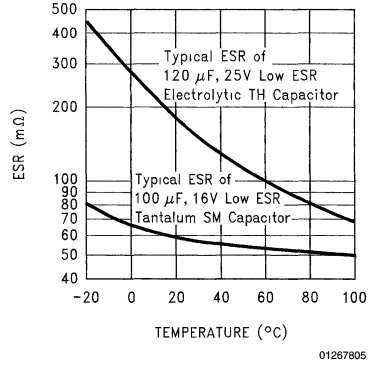


FIGURE 4. Capacitor ESR Changes vs Temperature

For a through hole design, an electrolytic capacitor (Panasonic HFQ series or Nichicon PL series or equivalent) would

Input Capacitor Selection (Continued)

be adequate. Other types or other manufacturers capacitors can be used provided the RMS ripple current ratings are adequate.

For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

Use caution when using ceramic capacitors for input bypassing, because it may cause severe ringing at the V_{IN} pin

Output Voltage Ripple and Transients

The output voltage of a switching power supply operating in the continuous mode will contain a sawtooth ripple voltage at the switcher frequency, and may also contain short voltage spikes at the peaks of the sawtooth waveform. The LM2825 switching power supply will operate in continuous mode when the load current is 0.25A or greater.

A typical output ripple voltage can range from approximately 0.5% to 3% of the output voltage. If very low output ripple voltage is needed (less than 15 mV), a post ripple filter is recommended (See *Figures 5, 6*). The inductance required is typically between 2 µH and 3 µH, with low DC resistance, to maintain good load regulation.

A 47 µF capacitor is used to maintain low output impedance and good transient response. A smaller capacitor can be used if the load does not require these characteristics.

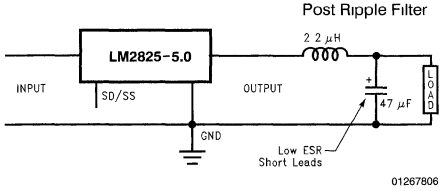


FIGURE 5. Post Ripple Filter

The photo shown in *Figure 6* shows a typical output ripple voltage, with and without a post ripple filter.

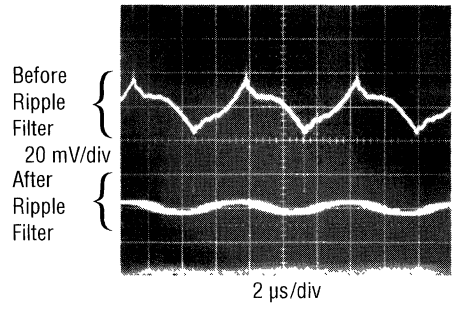


FIGURE 6. Post Ripple Filter Waveform

The voltage spikes are caused by the fast switching action of the switch, the diode, and the parasitic inductance of the output filter capacitor, which are all inside the LM2825 Wiring inductance, stray capacitance, as well as impedance of the scope probe used to evaluate these transients, will contribute to the amplitude of these spikes.

When observing output ripple on an oscilloscope, it is essential that a short, low inductance scope probe ground connection be used (see also "Thermal Considerations and Board Layout" section) Most scope probe manufacturers provide a special probe terminator which is soldered onto the regulator board, preferably at the output capacitor This provides a very short scope ground thus eliminating the problems associated with the 3 inch ground lead normally provided with the probe, and provides a much cleaner and more accurate picture of the ripple voltage waveform.

When the device is operating in the continuous mode, the inductor current waveform ranges from a triangular to a sawtooth type of waveform (depending on the input voltage). For a given input and output voltage, the peak-to-peak amplitude of this inductor current waveform remains constant As the load current increases or decreases, the entire sawtooth current waveform also rises and falls. The average value (or the center) of this current waveform is equal to the DC load current.

If the load current drops to a low enough level, the bottom of the sawtooth current waveform will reach zero, and the

Output Voltage Ripple and Transients (Continued)

switcher will smoothly change from a continuous to a discontinuous mode of operation. The LM2825 will run discontinuous if the output is lightly loaded. This is a perfectly acceptable mode of operation.

Start-Up Considerations, Including Use of Shutdown/Soft-Start Feature

NORMAL START-UP

Under normal operating conditions, the LM2825 can require large input currents during start-up. *Figure 7* shows that the input current reaches a peak of almost 2A with only 250 mA load current. The output voltage comes up in approximately 400 µs. Although the input peak current and the output voltage transient can be very high, for most conditions, the device will start-up without problems.

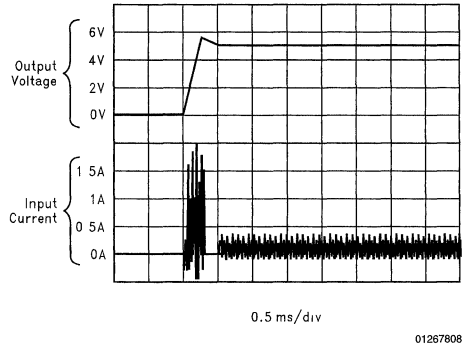


FIGURE 7. Output Voltage and Input Current during Start-Up

However, some power supplies can't deliver these high start-up currents, which may cause the device to have difficulties during start-up.

CIRCUMSTANCES THAT MAY CAUSE DIFFICULTY IN START-UP

The LM2825 will have difficulties starting when the voltage applied to the input of the device has a high dV/dt and is used under the following conditions:

- High input voltage (> 20V)

and/or

- High temperature (T_J > 75˚C)

Because of the high start-up currents needed at the input under these conditions, the device goes into second stage current limit (oscillator frequency decreases, output voltage drops) and it can't get out of this state. The start-up current is calculated as follows:

$$dI = ((V_{IN} - V_{OUT})/L) * dt$$

For Example:

V_{IN} = 35V

V_{OUT} = 5V (desired)

I_{OUT} = 1A

f_{osc} = 150 kHz→dt = 6.67 µs

L = 68 µH

When the device is turned on, the output is 0V, so the duty cycle wants to go to its maximum. The initial current ramp is:

$$dI = ((35V - 0V/68\ \mu H) * 6.67\ \mu s$$

$$dI = 3.43A$$

The higher the input voltage the higher the dI. Since the current limit of the LM2825 is 1.4A (typical), the device will go into current limit. *Figure 9* shows the inductor current waveform versus time. The device goes into current limit even faster when the inductor saturates. The inductor is designed for a maximum of 1.3A. The higher the temperature, the faster the inductor saturates, as indicated by the dotted line in *Figure 9*.

During the OFF time, we get the following:

$$dI = ((0.5V + 0V)/68\ \mu H) * \text{small } t_{off}$$

As a result: dI = very small

The inductor won't be able to release the stored energy. During the next ON cycle, the current ramps up quickly until it hits current limit again. The device can't get out of this state, unless it is reset.

IMPROVING START-UP BY USING A SOFT-START CAPACITOR

Start-up can be improved by using a Soft-start capacitor. *Figure 8* shows the range of input voltages, and ambient temperatures, where the Soft-start capacitor (C_{SS}) is required. This curve is typical for maximum rated output current loads and can be used as a guideline. As the output current decreases, the operating area requiring a Soft-start capacitor decreases. For temperatures above 70˚C, you typically need a Soft-start capacitor. Capacitor values between 0.1 µF and 1 µF are recommended. Tantalum or ceramic capacitors are appropriate for the application.

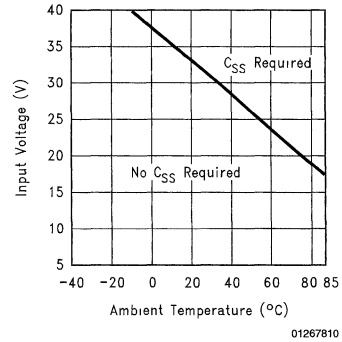


FIGURE 8. Usage of The Soft-Start Capacitor

Start-Up Considerations, Including Use of Shutdown/Soft-Start Feature
(Continued)

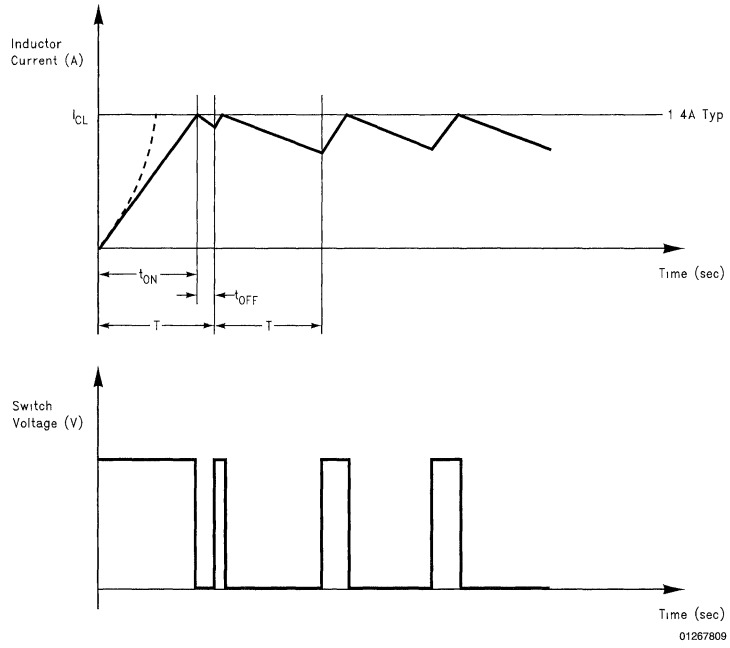


FIGURE 9. Inductor Current and Switch Voltage vs Time, during Current-Limited Start-Up

A capacitor on the $\overline{SD}$/SS pin provides the regulator with a Soft-start feature (slow start-up) When the DC input voltage is first applied to the regulator, or when the Shutdown/ Soft-start pin is allowed to go high, a constant current (approximately 5 µA begins charging this capacitor As the capacitor voltage rises, the regulator goes through four operating regions (see the bottom curve in *Figure 10*).

Start-Up Considerations, Including Use of Shutdown/Soft-Start Feature (Continued)

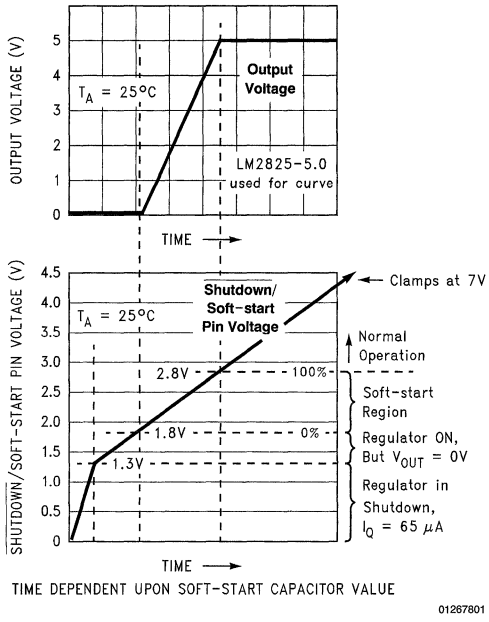


FIGURE 10. Soft-Start and Output Voltage Waveforms

1. **Regulator in shutdown.** When the SD/SS pin voltage is between 0V and 1.3V, the regulator is in shutdown, the output voltage is zero, and the IC quiescent current is approximately 65 μA.
2. **Regulator ON, but the output voltage is zero.** With the $\overline{SD}$/SS pin voltage between approximately 1.3V and 1.8V, the internal regulator circuitry is operating, the quiescent current rises to approximately 5 mA, but the output voltage is still zero. Also, as the 1.3V threshold is exceeded, the Soft-start capacitor charging current decreases from 5 μA down to approximately 1.6 μA. This decreases the slope of capacitor voltage ramp.
3. **Soft-start Region.** When the $\overline{SD}$/SS pin voltage is between 1.8V and 2.8V (@ 25˚C), the regulator is in a Soft-start condition. The output (pin 4–8) duty cycle initially starts out very low, with narrow pulses and gradually get wider as the capacitor SD/SS pin ramps up towards 2.8V. As the duty cycle increases, the output voltage also increases at a controlled ramp up. See the top curve in *Figure 10*. The input supply current requirement also starts out at a low level for the narrow pulses and ramp up in a controlled manner. This is a very useful feature in some switcher topologies that require large startup currents which can load down the input power supply.

   Note that the lower curve shown in *Figure 10* shows the Soft-start region from 0% to 100%. This is not the duty cycle percentage, but the output voltage percentage. Also, the Soft-start voltage range has a negative temperature coefficient associated with it.
4. **Normal operation.** Above 2.8V, the circuit operates as a standard Pulse Width Modulated switching regulator. The capacitor will continue to charge up until it reaches the internal clamp voltage of approximately 7V.

The circuit of *Figure 11* shows the LM2825 with the Shutdown/Soft-start feature, using different logic signals to shutdown the device, while allowing the use of Soft-start. When the regulator is shutdown, the quiescent current is typically reduced to 65 μA.

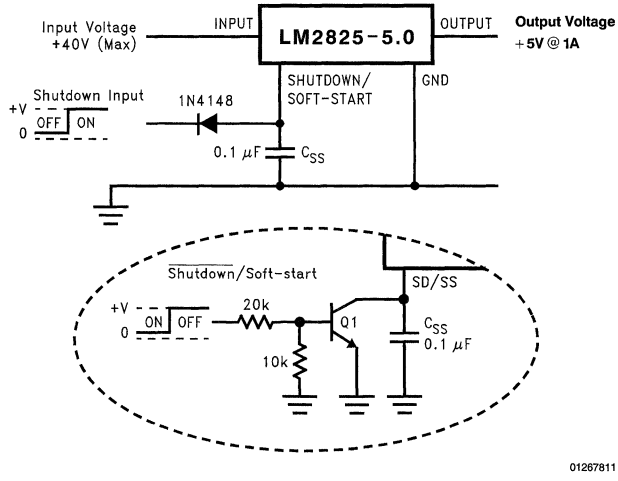


FIGURE 11. Typical Circuits Using Shutdown/Soft-Start Features

Start-Up Considerations, Including Use of Shutdown/Soft-Start Feature (Continued)

The plots in *Figures 12, 13* show the effect of Soft-start on the output voltage and the input current, with and without a Soft-start capacitor. The reduced input current required at startup is very evident when comparing the two plots. The Soft-start feature reduces the startup current from almost 2A down to several hundred mA (V_{IN} = 10V, V_{OUT} = 5V and I_{load} = 250 mA, C_{SS} = 0.1 µF). and delays and slows down the output voltage rise time.

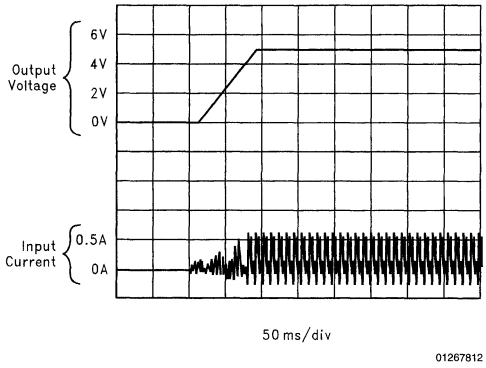


FIGURE 12. Output Voltage and Input Current at Start-Up, with Soft-Start

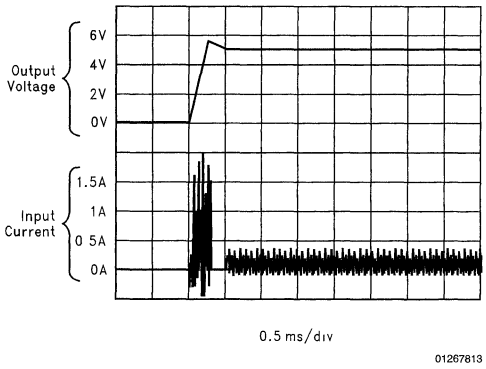


FIGURE 13. Output Voltage and Input Current at Start-Up, without Soft-Start

This reduction in start-up current is useful in situations where the input power source is limited in the amount of current it can deliver.

If a very slow output voltage ramp is desired, a larger Soft-start capacitor can be used. Many seconds or even minutes are possible. The Start-up time can be estimated to be:

$$\Delta t = (C_{SS})\ (2 \times 10^6) \text{ sec}$$

This is the time between applying the input voltage and the output reaching its nominal voltage.

If this pin is driven from a voltage source, the current must be limited to about 1 mA.

Undervoltage Lockout

Some applications require that the regulator remains OFF until the input voltage reaches a predetermined voltage. An example of an undervoltage lockout is shown in *Figure 14.* The zener diode establishes the threshold voltage when the device begins operating. When the input voltage is less than the zener voltage, resistors R1 and R2 hold the $\overline{\text{Shutdown}}$/Soft-start pin low, keeping the device in the shutdown mode. As the input voltage exceeds the zener voltage, the zener conducts, pulling the $\overline{\text{Shutdown}}$/Soft-start pin high, allowing the LM2825 to begin switching. The threshold voltage for the undervoltage lockout feature is approximately 1.5V greater than the zener voltage.

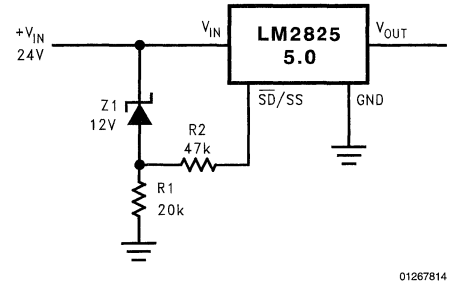


FIGURE 14. Undervoltage Lockout Circuit

This solution is cheap and simple, but at the same time, the precision is low. If you want a high precision undervoltage lockout circuit, *Figure 15* gives you a better solution.

For a predetermined input voltage, resistor R1 can be calculated with the following equation:

$$R1 = \frac{5.1\left[1 - \left(\frac{1.225}{V_{IN}} - \frac{R_3}{R_3 + R_4 + R_5}\right)\right]}{\left(\frac{1.225}{V_{IN}} - \frac{R_3}{R_3 + R_4 + R_5}\right)}$$

The schematic and equation will provide a hysteretic undervoltage lockout circuit design. The hysteresis band is approximately 10 mV.

Once the circuit has been incorporated with the complete power supply and powered circuitry, the values of R1, R2, R3, R4, and R5 can be optimized.

Undervoltage Lockout (Continued)

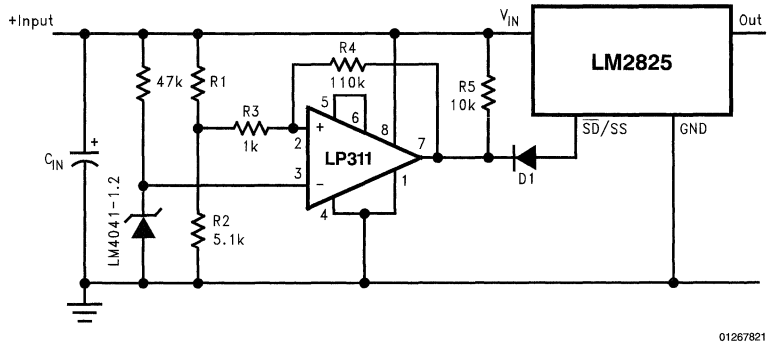


FIGURE 15. Precision Undervoltage Lockout Circuit

Inverting Regulator

The circuit in *Figure 16* converts a positive input voltage to a negative output voltage with a common ground. The circuit operates by bootstrapping the regulator's ground pin to the negative output voltage, then grounding the output pin, the regulator senses the inverted output voltage and regulates it.

This example uses the LM2825-5.0 to generate a −5V output, but other output voltages are possible by selecting other output voltage versions, including the adjustable version.

Since this regulator topology can produce an output voltage that is either greater than or less than the input voltage, the maximum output current greatly depends on both the input and output voltage. The curve shown in *Figure 17* provides a guide as to the amount of output load current possible for the different input and output voltage conditions.

The maximum voltage appearing across the regulator is the absolute sum of the input and output voltage, and this must be limited to a maximum of 40V. For example, when converting +20V to −12V, the regulator would see 32V between the input pin and ground pin. The LM2825 has a maximum input voltage spec of 40V.

Additional diodes are required in this regulator configuration. Diode D1 is used to isolate input voltage ripple or noise from coupling through the C_{IN} capacitor to the output, under light or no load conditions. Also, this diode isolation changes the topology to closley resemble a buck configuration thus providing good closed loop stability. A Schottky diode is recommended for low input voltages, (because of its lower voltage drop) but for higher input voltages, a fast recovery diode could be used.

Without diode D2, when the input voltage is first applied, the charging current of C_{IN} can pull the output positive by several volts for a short period of time. Adding D2 prevents the output from going positive by more than a diode voltage.

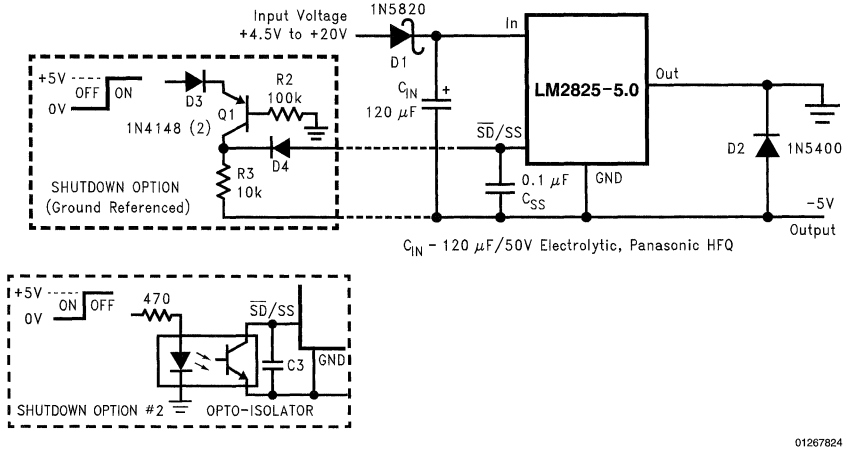


FIGURE 16. Inverting Regulator

Inverting Regulator (Continued)

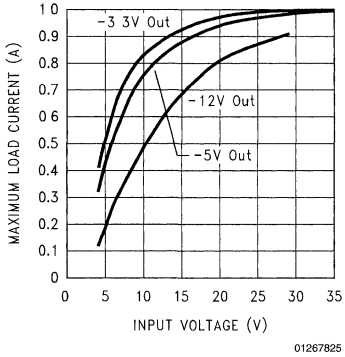


FIGURE 17. Inverting Regulator Typical Load Current

This type of inverting regulator can require relatively large amounts of input current when starting up, even with light loads. Input currents as high as the LM2825 current limit (approx 1.4A) are needed for at least 2 ms or more, until the output reaches its nominal output voltage. The actual time depends on the output voltage. Input power sources that are current limited or sources that can not deliver these currents without getting loaded down, may not work correctly. Because of the relatively high startup currents required by the inverting topology, the Soft-start feature shown in *Figure 16* is recommended.

Also shown in *Figure 16* are several shutdown methods for the inverting configuration. With the inverting configuration, some level shifting is required, because the ground pin of the regulator is no longer at ground, but is now at the negative output voltage. The shutdown methods shown accept ground referenced shutdown signals.

Figures 18, 19 apply the undervoltage lockout feature to an inverting circuit. *Figure 18* features a constant threshold voltage for turn ON and turn OFF (zener voltage plus approximately one volt). Since the $\overline{SD}$/SS pin has an internal 7V zener clamp, R2 is needed to limit the current into this pin to approximately 1 mA when Q1 is on. If hysteresis is needed, the circuit in *Figure 19* has a turn ON voltage which is different than the turn OFF voltage. The amount of hysteresis is approximately equal to the value of the output voltage.

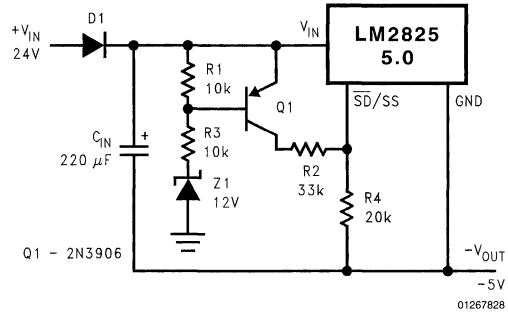


FIGURE 18. Undervoltage Lockout Without Hysteresis for an Inverting Regulator

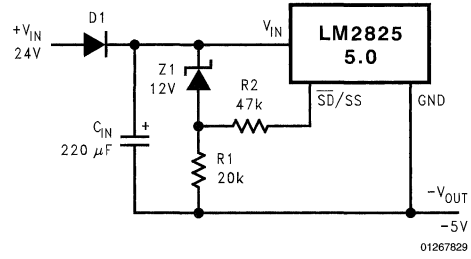


FIGURE 19. Undervoltage Lockout With Hysteresis for an Inverting Regulator

Thermal Considerations and Board Layout

For best thermal performance, wide copper traces (several mm's) should be used. Pins should be soldered to generous amounts of printed circuit board copper (except for the No Connect (NC) pins). Large areas of copper provide the best transfer of heat (lower thermal resistance) to the surrounding air, and even double sided or multilayer boards provide a better heat path to the surrounding air. Unless power levels are small, sockets are not recommended because of the increased thermal resistance and the resultant higher junction temperatures.

Thermal Considerations and Board Layout (Continued)

Figure 20 shows θ_{JA} for different PCB areas and two different output power levels.

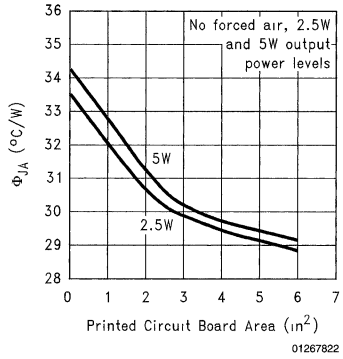


FIGURE 20. θ_{JA} vs Board Area for 2 Output Power Levels

Figure 21 shows the effect of forced air on θ_{JA}. The higher the windspeeds, the less influence the board area has.

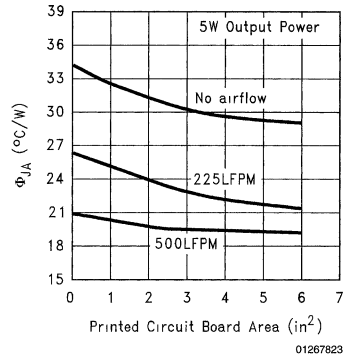


FIGURE 21. θ_{JA} vs Board Area for 3 Windspeed Levels

Package thermal resistance numbers are all approximate, and there are many factors that will affect the junction temperature. Some of these factors include board size, shape, thickness, position, location, and even board temperature. Other factors are, trace width, printed circuit copper area, copper thickness, single- or double-sided, multilayer board, and the amount of solder on the board.

For best ripple performance, use pin 23 as the input GND and pin 11 and 12 as the output GND for minimum spikes at the output. If you can, avoid using pins 1, 2 and 23 as output GND pins. *Figure 22* shows the PCB layout which gives you the smallest spikes at the output voltage.

When you measure the output ripple voltage with a scopeprobe (see also "Output Ripple Voltage and Transients" section), it makes a difference where you connect the ground of the probe. Photo a) in *Figure 23*, shows the output voltage ripple when the ground is connected to pin 1, 2 or/and 23. Photo b) shows the same thing when the ground is connected to pin 11 and 12. So, for a better ac performance, it is better to connect the ground of your power supply to pin 23 and the ground of your system electronics to pin 11 and 12.

Thermal Considerations and Board Layout (Continued)

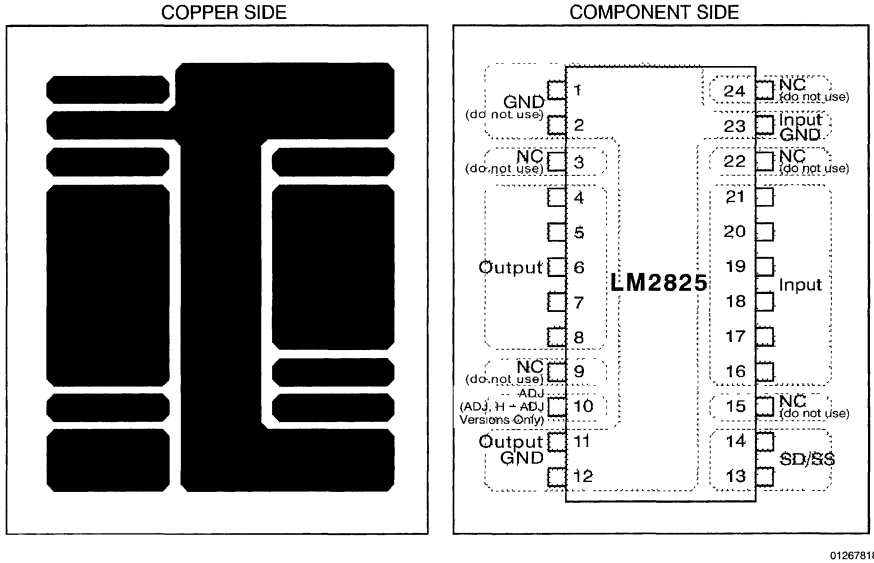
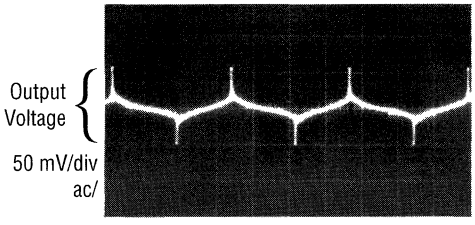


FIGURE 22. PCB Layout for Better Ripple and Spikes Performance (2 x Size)



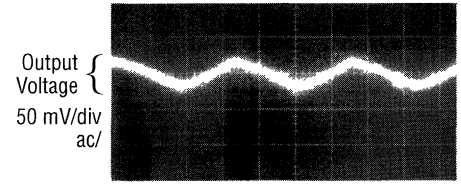


FIGURE 23. Ripple and Spikes at the Output Voltage

Information About the LM2650 Evaluation Board Rev. 1

National Semiconductor
Application Note 1071
Steven Hunt

Introduction

A printed circuit board (PCB) has been developed. This application note contains information about the board.

General Description

The LM2650 evaluation board is provided as a tool for developing DC/DC converters based on the LM2650 IC. It is configured for single-output, step-down DC/DC converters. *Figure 1* is a complete schematic of the board which can accommodate up to 28 components including the LM2650. *Table 1* is a complete list of pads for placing components.

Note: Not all applications will require the placement of all 28 components. The number of components placed depends on the requirements of the application and the use of features like programmable soft-start. The LM2650 evaluation board is intended to be a reusable tool on which many different converters meeting the requirements of many different applications can be built. It is not intended to demonstrate only one application of the LM2650.

For convenience, a sample of the LM2650 and eight other components have been assembled: a 0.1 µF capacitor at each of C1, C2, C6, and CB, a 0.2 µF capacitor at CVDD, a 0.01 µF capacitor at CSS, a 24.9 kΩ resistor at R2, and a 0Ω resistor at R4. Of the eight, the first seven are common to many applications, and the last is simply a jumper grounding the SYNC input. When the synchronization feature is not being used, the SYNC input should be grounded.

Example Circuits

The components contained in Tables 2, 3, and 4 can be used to build typical application circuits. As with the design of any DC/DC converter, the design of these involved tradeoffs between efficiency, size, and cost. The converters detailed in Table 2 were designed with efficiency as the number one criteria. Those detailed in Table 4 trade slightly higher switching losses for a much smaller inductor.

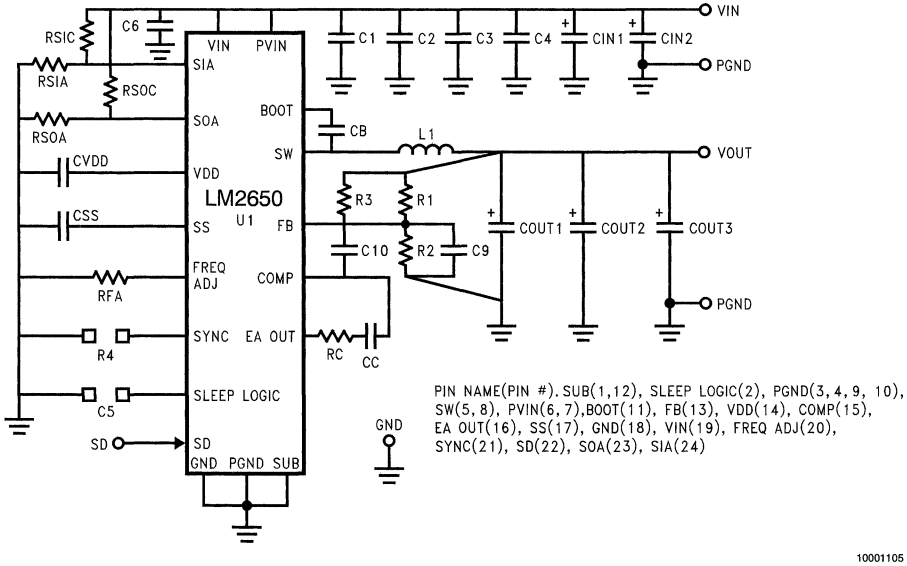


FIGURE 1. The LM2650 Evaluation Board Rev. 1 Schematic

Thermal Performance

The 24-lead SO package is a molded plastic package with a solid copper lead frame. Most of the heat generated at the die flows through the lead frame into the 3-ounce copper planes on the board. The board then acts as a heat sink. The junction-to-ambient thermal resistance of the packaged IC mounted on the board has been measured to be 38°C/W, 37 °C/W, and 35 °C/W for the dissipation of 1.0W, 1.5W, and 2.0W respectively. These measurements were made in still air. The junction-to-ambient thermal resistance of the packaged IC alone in still air is 78°C/W. The board is 0.063" thick FR-4 material.

Art

Figure 2 through *Figure 4* show the PCB art work.

TABLE 1. A Complete List of Pads for Placing Components

Label	#	Notes
U1	1	For placing the LM2650.
C1, C2, C3, and C4	4	Capacitors placed here filter high-frequency switching noise from the input power rail.
C5	0	These pads should not be labeled with a C. No component is placed here. They can be used to ground the SLEEP LOGIC input. The pad connected to the SLEEP LOGIC pin can be used to pull the input up
C6	1	A capacitor placed here also filters high-frequency switching noise from the input power rail but at the VIN rail, the rail used by the signal-level circuits inside the IC.
C9	1	Usually no component is placed here. A capacitor might be placed here for loop compensation purposes, but most applications don't use it.
C10	1	A capacitor is placed here for loop compensation purposes.
CB	1	The bootstrap capacitor is placed here.
CC	1	A capacitor is placed here for loop compensation purposes. This capacitor and an internal 6.5 kΩ resistor create an integrator pole.
CIN1 and CIN2	2	The bulk input capacitors are placed here.
COUT1, COUT2, and COUT3	3	The output filter capacitors are placed here.
CSS	1	A capacitor placed here programs the soft-start interval.
CVDD	1	A capacitor placed here bypasses the output of the VDD regulator.
L1	1	The inductor is placed here.
R1	1	One of the feedback resistors is placed here.
R2	1	The other feedback resistor is placed here.
R3	1	A resistor is placed here for loop compensation purposes.
R4	1	These pads can be used to ground the SYNC input when the synchronization feature is not being used. The pad connected to the SYNC input can be used to connect the synchronization signal. The evaluation board has a 0Ω jumper placed here to ground the SYNC input.
RC	1	A resistor is also placed here for loop compensation purposes. This resistor and the capacitor placed at CC create an integrator zero.
RFA	1	A resistor placed here adjusts the switching frequency up from the nominal 90 kHz. No component is placed here for applications switching at 90 kHz.
RSIA and RSIC	2	Resistors placed here program the sleep-in threshold.
RSOA and RSOC	2	Resistors placed here program the sleep-out threshold.

TABLE 2. Components for Two Typical 90 kHz Application Circuits

Input Voltage	**7 to 18V IN**	
Applicable Cell Stacks	8- to 12-Cell NiCd or NiMH, 3- to 4-Cell Li Ion, 8- to 11-Cell Alkaline, 6-Cell Lead Acid	
Output	**5V, 3A Out**	**3.3V, 3A Out**
Input Filter Capacitors C1, C2, and C6	0.1 µF ceramic chip capacitor	0.1 µF ceramic chip capacitor
Bootstrap Capacitor CB	0.1 µF ceramic chip capacitor	0.1 µF ceramic chip capacitor
Soft-start Capacitor CSS	0.01 µF ceramic chip capacitor	0.01 µF ceramic chip capacitor
VDD Bypass Capacitor CVDD	0.2 µF ceramic chip capacitor	0.2 µF ceramic chip capacitor
Input Bulk Capacitors CIN1 and CIN2	22 µF, 35V AVX TPS Series or Sprague 593D Series tantalum chip capacitor	22 µF, 35V AVX TPS Series or Sprague 593D Series tantalum chip capacitor
Inductor L1	40 µH (See Table 3.)	33 µH (See Table 3.)
Output Capacitors COUT1, COUT2, and COUT3	220 µF, 10V AVX TPS Series or Sprague 593D Series tantalum chip capacitor	220 µF, 10V AVX TPS Series or Sprague 593D Series tantalum chip capacitor
Feedback Resistors R1 and R2	R1 = 75 kΩ, 1%, R2 = 24.9 kΩ, 1%	R1 = 41.2 kΩ, 1%, R2 = 24.9 kΩ, 1%
Compensation Components RC, CC, R3, and C10	RC = 37.4 kΩ, CC = 4.7 nF, R3= 3.57 kΩ,C10 = 5.6 nF	RC = 23.2 kΩ, CC= 8.2 nF, R3 = 2.0 kΩ, C10 = 10 nF

TABLE 2. Components for Two Typical 90 kHz Application Circuits (Continued)

Sleep Resistors RSIA and RSOA	RSIA = 33 kΩ, RSOA = 200 kΩ	RSIA = 39 kΩ, RSOA = 130 kΩ

TABLE 3. Toroidal Inductors Using Cores from MICROMETALS, INC.

	Core #	Core Material	Wire Gauge	# of Strands	# of Turns
15 µH	T38	−52	AWG #23	1	21
20 µH	T38	−52	AWG #23	1	25
33 µH	T50	−52	AWG #21	1	41
40 µH	T50(B)	−18	AWG #21	1	41

TABLE 4. Components for Two Typical 200 kHz Application Circuits

Input Voltage	**7 to 18V IN**	
Applicable Cell Stacks	8- to 12-Cell NiCd or NiMH, 3- to 4-Cell Li Ion, 8- to 11-Cell Alkaline, 6-Cell Lead Acid	
Output	**5V, 3A Out**	**3.3V, 3A Out**
Input Filter Capacitors C1, C2, and C6	0.1 µF ceramic chip capacitor	0.1 µF ceramic chip capacitor
Bootstrap Capacitor CB	0.1 µF ceramic chip capacitor	0.1 µF ceramic chip capacitor
Soft-start Capacitor CSS	0.01 µF ceramic chip capacitor	0.01 µF ceramic chip capacitor
VDD Bypass Capacitor CVDD	0.2 µF ceramic chip capacitor	0.2 µF ceramic chip capacitor
Input Bulk Capacitors CIN1 and CIN2	22 µF, 35V AVX TPS Series or Sprague 593D Series tantalum chip capacitor	22 µF, 35V AVX TPS Series or Sprague 593D Series tantalum chip capacitor
Inductor L1	20 µH (See Table 3.)	15 µH (See Table 3.)
Output Capacitors COUT1, COUT2, and COUT3	220 µF, 10V AVX TPS Series or Sprague 593D Series tantalum chip capacitor	220 µF, 10V AVX TPS Series or Sprague 593D Series tantalum chip capacitor
Feedback Resistors R1 and R2	R1 = 75 kΩ, 1%, R2 = 24.9 kΩ, 1%	R1 = 41.2 kΩ, 1%, R2 = 24.9 kΩ, 1%
Compensation Components RC, CC, R3, and C10	RC = 53.6 kΩ, CC = 2.7 nF, R3= 4.02 kΩ, C10 = 4.7 nF	RC = 33.2 kΩ, CC= 3.9 nF, R3 = 3.01 kΩ, C10 = 6.8 nF
Sleep Resistors RSIA and RSOA	RSIA = 47 kΩ, RSOA = 200 kΩ	RSIA = 47 kΩ, RSOA = 91 kΩ
Frequency Adjusting Resistor RFA	RFA = 24.9 kΩ	RFA = 24.9 kΩ

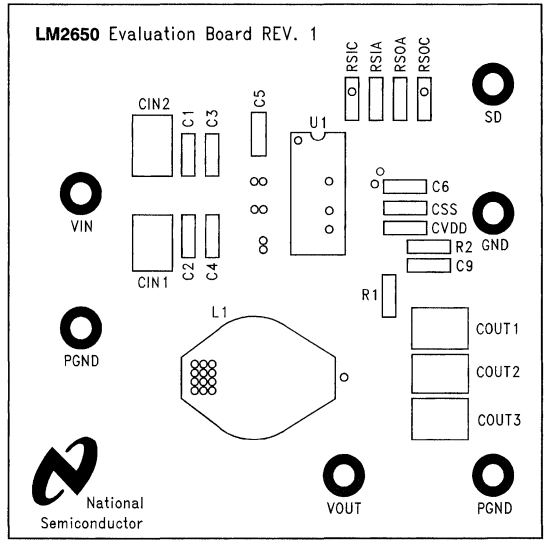


FIGURE 2. LM2650 Evaluation Board Top Silk Screen (Scale 1:1)

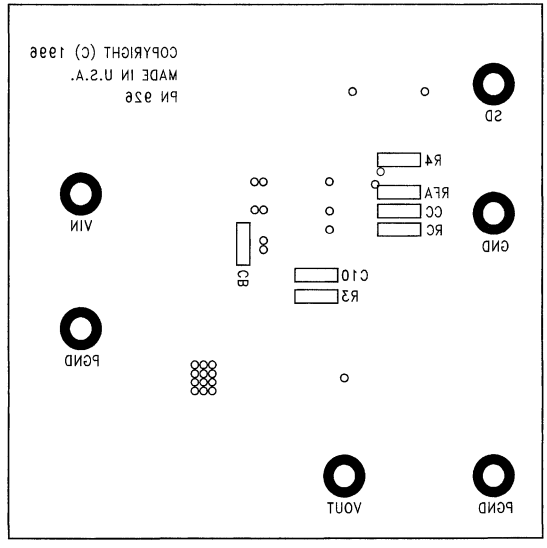


FIGURE 3. LM2650 Evaluation Board Bottom Silk Screen (Scale 1:1)

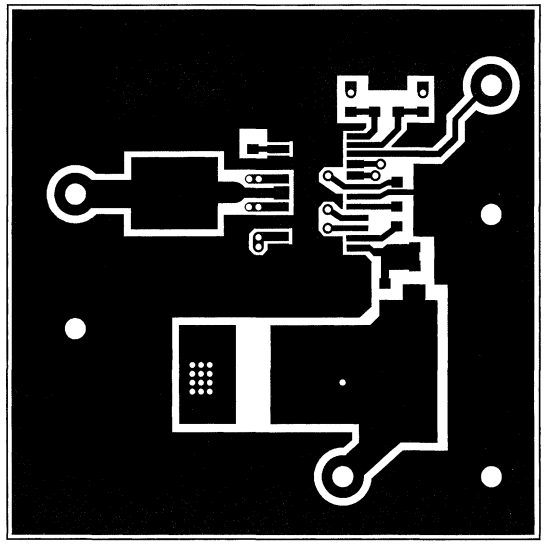


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FIGURE 4. LM2650 Evaluation Board Component Side (Scale 1:1)

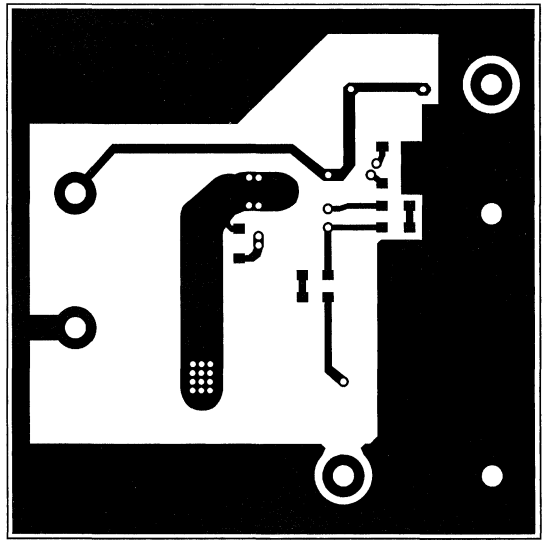

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FIGURE 5. LM2650 Evaluation Board Solder Side (Scale 1:1)

Adjust or Synchronize LM2586/88 Switching Frequency

National Semiconductor
Application Note 1082

Introduction

Switching frequency is a very important parameter in switching power converters. As the switching frequency increases, the physical size of magnetic elements and other components in the circuit reduce significantly. Switching frequency also plays a great role in control loop gain and compensation design. Switching frequency determines the maximum allowable bandwidth of the control loop. Switching frequency is also important parameter for EMI and noise issues. The EMI spectrum is a direct function of the switching frequency.

From the above cited reasons, it can be deduced that a great advantage will be gained by having control over the switching frequency. Simple switcher boost converters are available in two flavors. While the LM2585 and LM2587 operate at a fixed switching frequency of 100 kHz, the LM2586 and LM2588 allows its switching frequency to be modified. Using either of two control methods, the switching frequency can be varied between 100 kHz (its base frequency) to 200 kHz. *Figure 1* shows the LM2586 boost regulator with synchronization and frequency adjust pins.

Synchronization forces the LM2586/8 switching frequency to match that of an external source, such as another switching regulator or a system clock. This keeps the EMI generated within the system to a predictable set of frequencies. It also prevents similar (but not matching) switching frequencies from producing a beat frequency. Both of these results make it easier to filter out switching noise in the system. By synchronizing to a higher frequency (>100 kHz) system clock or switching regulator, the LM2586/88 can be made to operate at higher frequencies, in order to reduce the size of the magnetic elements and other components.

The threshold voltage for the synchronization pin is typically around 0.75V. The voltage levels of the clock signal should be 0V and 2V. If the sync Pin is not used, it should be left open.

The second frequency control method changes the switching frequency of an LM2586/8, using a single resistor (from the Frequency Adjust pin to ground). Once again, this allows a design to be customized for a smaller size, as the sizes of the transformer and output capacitor tend to go down as the switching frequency increases. *Table 1* shows the resistor values corresponding to commonly used frequencies.

If the Frequency Adjust pin is not to be used, it should be left open. Pulling this pin above 3V will turn the regulator off.

TABLE 1. Frequency Settling Resistor Guide

R_{SET} (kΩ)	Frequency (kHz)
Open	100
200	125
47	150
33	175
22	200

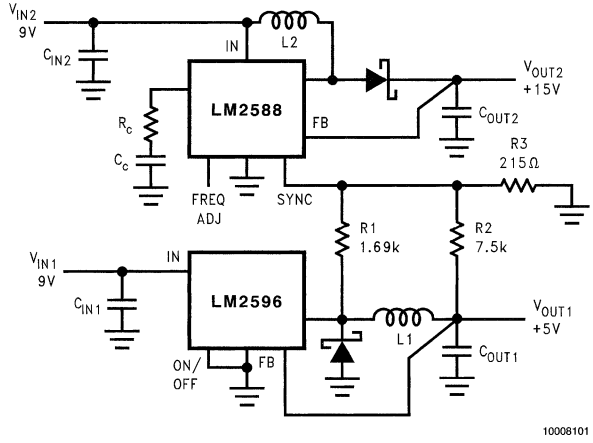

FIGURE 1. Synchronizing LM2588 Boost to LM2596 Buck Regulator

Example

In the example shown, the LM2588 has been synchronized to the 150 kHz LM2596. With the LM2596 output voltage of 5V, the resistor divider of R1, R2, and R3 sets the voltage applied to the LM2588 SYNC pin to swing between 0.1V and 1.5V. To assure correct operation, the regulator designated "master" (in this case, the LM2596) must be in continuous operation (i.e., the current in inductor L1 must be continually above 0A). In addition, to keep the sync voltage at the designated levels, the input voltage to the master regulator (V_{IN1}) should not vary more than ±10%. Synchronization of the LM2588 (or LM2586) occurs on the falling edge of the sync signal. The LM2596 buck converter and LM2588 boost regulator are designed using the *Switchers Made Simple*® Software, SMS4.2.1. *Figure 2* shows the diode and switch voltage waveforms of the buck and boost regulators respectively.

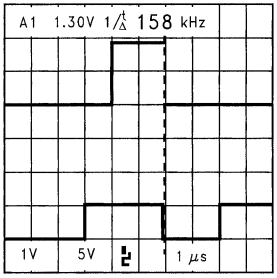

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FIGURE 2. Waveforms (Top-Synchronization Signal, Bottom-LM2588 Switch Waveform)

LM2675-5.0EVAL 1A Step-Down High-Efficiency SIMPLE SWITCHER Evaluation Board

National Semiconductor
Application Note 1120
Wanda Garrett

Introduction

The LM2675 SIMPLE SWITCHER step-down regulator provides all the active functions for a step-down regulator capable of driving a 1A load with excellent line and load regulation. Switching frequency is internally set to 260 kHz, allowing smaller-sized filter components than would be needed with lower-frequency switching regulators. The internal switch is an 0.25Ω DMOS device, providing very high-efficiency power conversion. With this high efficiency, the copper traces on the printed circuit board are the only heat sinking needed.

The LM2675-5.0EVAL evaluation board is a fully-assembled and tested surface-mount regulator that provides a 5V±1.5% output at up to 1A, from an input of 8V to 40V. The overall efficiency is typically as high as 90%. The operating temperature range is 0°C to +85°C.

Evaluation Board Design

This evaluation board is designed for supplying 5V at up to 1 Amp to a load. The input voltage range is 8V to 40V. Components, shown in the schematic of *Figure 1*, were selected based on the design procedure in the LM2675 datasheet.

Layout is very important in switching regulator designs. Rapidly switching currents associated with wiring inductance can generate voltage transients which can cause problems. For minimal inductance and ground loops, the traces which carry the highest currents (input, ground, switch, and output signals) are relatively wide and short. The external components are located physically close to the IC.

Components in this design were selected according to the design procedure in the LM2675 datasheet. The input capacitor C_{IN} was chosen for its voltage rating and RMS current rating. A 40V maximum input requires a capacitor with voltage rating of at least 1.25x40, or 50V. A conservative estimate of RMS input current is approximately ½ the DC load current. The input capacitor chosen for this application has a voltage rating of 50V and an RMS current rating of 900 mA. The inductor and output capacitor were selected for a combination of good regulator stability and compact size, according to the design tables in the datasheet.

While the LM2675 has an ON/$\overline{\text{OFF}}$ control, this has not been provided on the evaluation board.

The parts list for this board is given in *Table 1*, while contact information for the component manufacturers is given in *Table 2*.

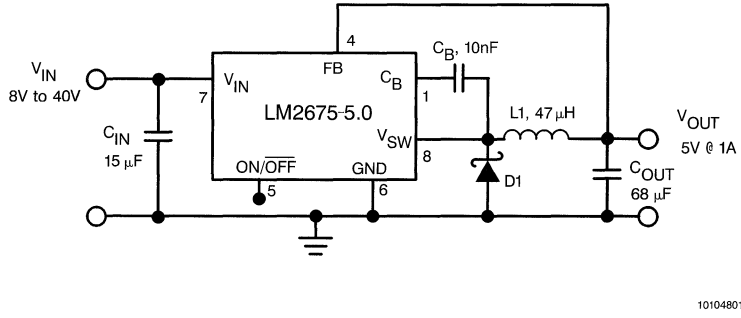


FIGURE 1. LM2675-5.0EVAL Schematic

TABLE 1. Parts List (Bill of Materials)

Designator	Description	Quantity
U1	LM2675M-5.0 National Semiconductor SIMPLE SWITCHER voltage converter	1
C_{IN}	15 µF, 50V Solid Tantalum, Sprague type 594D	1
C_{OUT}	68 µF, 16V Solid Tantalum, Sprague type 595D	1
D1	1A, 40V Schottky rectifier	1
L1	47 µH Power Inductor, Coilcraft D03316-473	1
C_B	0.01 µF, 50V Ceramic	1

Evaluation Board Design (Continued)

TABLE 2. Component Manufacturers

Manufacturer	Phone	FAX	Internet
National Semiconductor	(800) 272-9959	(800) 737-7018	www.national.com
Coilcraft Inc.	(800) 322-2645	(708) 639-1469	www.coilcraft.com
Coilcraft Inc., Europe	+44 1236 730 595	+44 1236 730 627	www.coilcraft.com
Sprague/Vishay	(207) 324-7223	(207) 324-4140	www.vishay.com

Operating the Evaluation Board

The input source for the LM2675-5.0 evaluation board must be greater than 8V for proper startup and operation. The maximum input voltage is 40V, including transients. During startup, the LM2675 may be left unloaded. If a load is connected, the peak current drawn from the source may be as great as 2.2A (for a full 1A load). A source with a lower current limit will slow down the startup of the regulator. If its current limit is sufficiently low, typically at or near the steady-state input current level, the regulator may not start up at all

The load for the evaluation board can be from 0 Amps (an open-circuit) to 1 Amp. Higher load currents can activate the LM2675 current limit, which will shut the regulator down until the load is reduced.

Designing with the LM2675

The LM2675 SIMPLE SWITCHER step-down converters are available in fixed output voltages of 3.3V, 5.0V, 12V, and an adjustable output version, each rated for a 1A load.

A family of standard inductors for use with the LM2675 are available from several manufacturers, which greatly simplifies the design of switch-mode power supplies. The datasheet also includes selection guides for diodes and capacitors designed to work in these switching regulator designs.

While the LM2675 product datasheet contains an easy, straight-forward design procedure, design software is also available, which further simplifies the system design. "LM267X Made Simple" is available from the Power Management Products section of National Semiconductor's web site at www.national.com/appinfo/power/index.html.

LM2653EVAL 1.5A Synchronous Switching Regulator Evaluation Board

National Semiconductor
Application Note 1133
Dongyan Zhou

Introduction

The LM2653 switching regulator provides high efficiency power conversion over a 100:1 load range (1.5A to 15mA). This feature makes the LM2653 an ideal fit in battery-powered applications.

Synchronous rectification and 75 mΩ internal switches provide up to 97% efficiency. At light loads, the LM2653 enters a low power hysteretic or "sleep" mode to keep the efficiency high. In many applications, the efficiency still exceeds 80% at 15 mA load. A shutdown pin is available to disable the LM2653 and reduce the supply current to 7 µA.

The IC contains patented current sensing circuitry for current mode control. This feature eliminates the external current sensing required by other current-mode DC-DC converters.

The IC has a 300kHz fixed frequency internal oscillator. The high oscillator frequency allows the use of extremely small, low profile components.

The evaluation board can be obtained by ordering part number LM2653EVAL from your local National Semiconductor sales office, or National's website at http://www.national.com.

Evaluation Board Design

The evaluation board is designed to supply 2.5V at up to 1.5A. The input voltage range is 4V to 14V. Components were selected based on the design procedure in the LM2653 datasheet. The feedback resistors can be adjusted to achieve a different output voltage:

$$V_{OUT} = 1.238V \times [1+ (R_1/R_2)]$$

Choose 1% resistors between 10kΩ to 100kΩ for R1 and R2.

PCB layout is critical to reduce noises and ensure specified performance. See the LM2653 datasheet for layout guidelines. The artwork for the evaluation board is shown at the end of this application note.

The schematic for the evaluation board is shown in *Figure 1*, and the parts list is given in *Table 1*.

When the undervoltage protection occurs, the output voltage can be pulled below ground as the inductor current is reversed through the synchronous FET. For applications which need to be protected from a negative voltage, a clamping diode D2 is recommended.

The PGOOD flag goes low whenever the overvoltage or undervoltage latch protection is enabled. The overvoltage protection will be enabled immediately when the output voltage exceeds 110% of its nominal. While the undervoltage latch protection will wait for a period of time set by the LDELAY capacitor. If the output voltage is still below 80% of its nominal after this waiting period, the latch protection will be enabled.

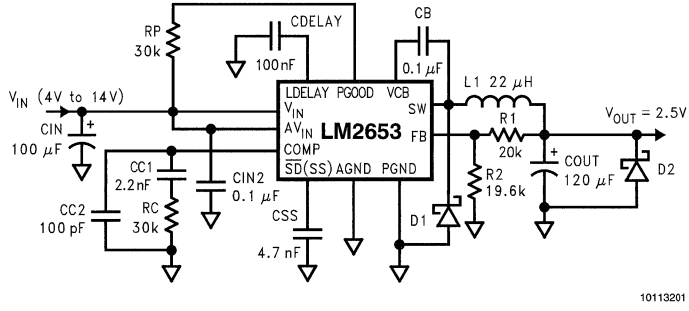


FIGURE 1. LM2653 EVAL Schematic

TABLE 1. Parts List (Bill Of Materials)

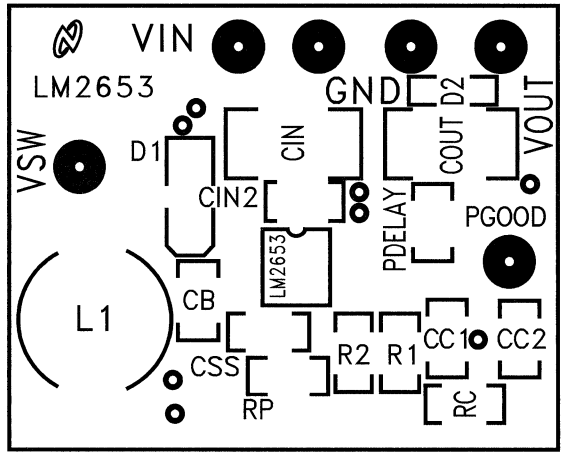
Designation	Description
L1	22µH, Coilcraft DO3316P-223
CIN (input capacitor)	100µF, 16V, Sprague 594D107X0016D2T
CIN2 (input capacitor)	0.1µF ceramic capacitor
CB (bootstrap capacitor)	0.1µF ceramic capacitor
CSS (softstart capacitor)	4.7nF ceramic capacitor
COUT (output capacitor)	120µF, 6.3V, Sprague 594D127X06R3C2T
CC1 (compensation)	2.2nF ceramic capacitor
CC2 (compensation)	100pF ceramic capacitor

Evaluation Board Design (Continued)

TABLE 1. Parts List (Bill Of Materials) (Continued)

Designation	Description
RC (compensation)	30kΩ, 5% resistor
D1	1A Schottky diode, Motorola MBRA130LT3
R1	20.0k, 1% resistor
R2	19.6k, 1% resistor
CDELAY	100nF ceramic capacitor
RP	50K, 5% resistor
D2	Open

Typical PC Board Layout: (2X Size)



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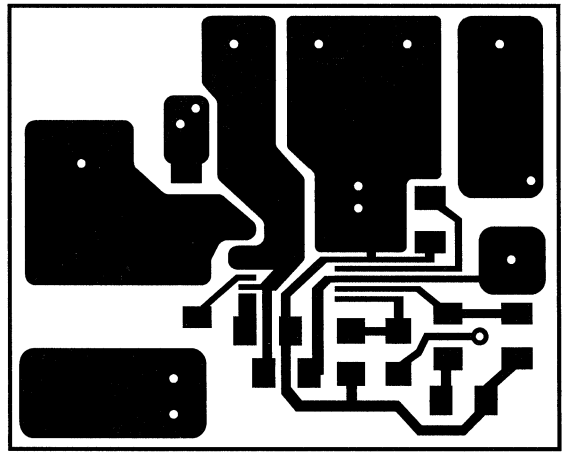
Component Placement Guide



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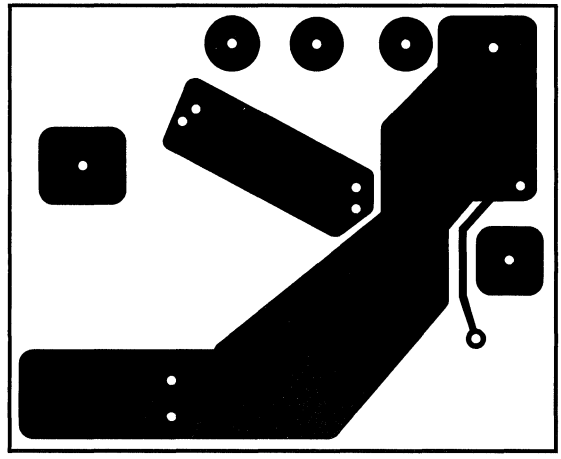
Component Side PC Board Layout

Typical PC Board Layout: (2X Size) (Continued)



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Solder Side PC Board Layout

LM267X 3A, 5A Evaluation Boards

National Semiconductor
Application Note 1135

Introduction

The LM267X evaluation board was developed for the evaluation of LM267X SIMPLE SWITCHER® series of 3 Amp and 5 Amp high efficiency step-down (Buck) switching voltage regulators. This application note describes the printed circuit board, and provides example circuits and directions on setup and operation of the **LM2673S-5_EVAL** and **LM2679S-5_EVAL** evaluation boards.

General Description

Many of our boards are intended to provide the user with device characterization and layout optimization data. The LM267x evaluation board was intended to allow the user to experiment with a variety of circuit topologies and components, and therefore not optimized for size. Please refer to the discussions of layout optimization in the PCB Layout Optimization section.

This board was designed such that both through-hole and surface-mount components can be used for construction. The regulator IC can be placed on the board as a surface-mount component only. The ground plane serves as a heatsink.

Table 1 shows an overview of the family of devices with special features of each indicated. Consult the device data sheet, or use the special power supply design software called ***Switchers Made Simple version 6.X*** (available for free download from National Semiconductor's Internet page, power.national.com) to determine all necessary component values for the particular device being used to accomplish a specific design and board layout considerations.

The printed circuit board, PCB, is labeled to indicate the location of all of the needed components for all possible design options. *Table 2* shows a complete list of the component labels and their functions.

Figure 1 identifies all components, but not all are necessary in every design.

Figure 2, *Figure 3* and *Figure 4* show the top, bottom and silk screen of the printed circuit board respectively.

TABLE 1. LM267X Family of High-Current Regulators supported by the Evaluation Board

DEVICE	Maximum Load Current (A)	SPECIAL FEATURES
LM2670	3	ON/OFF, External Frequency Sync Capability
LM2673	3	Adjustable Current Limit, Softstart
LM2676	3	ON/OFF
LM2677	5	ON/OFF, External Frequncy Sync. Capability
LM2678	5	ON/OFF
LM2679	5	Adjustable Current Limit, Softstart

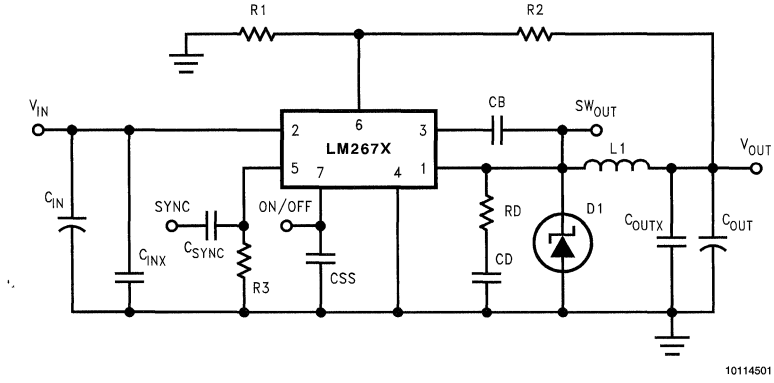


FIGURE 1. Example Schematic Showing Connection for all Components.

General Description (Continued)

TABLE 2. List of Component Labels and Functionality

LABEL	FUNCTION
U1	LM267X Switching Regulator IC
CIN	Input Capacitor(s); All devices.
CINX	0.47µF, optional high frequency input bypass capacitor, recommended in all designs: All devices.
CB	Boost capacitor; All devices.
D1	Catch diode; All devices.
R1	Feedback resistor (1kΩ) for adjustable output devices and shorted, replaced by a jumper wire, with fixed output voltage devices.
R2	Feedback resistor for adjustable output devices and open, not connected for fixed voltage devices.
R3*	Current limit resistor for LM2673, LM2679; Sync input resistor (1KΩ) for LM2670 and LM2677; Not inserted for LM2676 and LM2678.
L1	Inductor; All devices.
CSYNC	Sync input capacitor (100pF); LM2670 and LM2677only. Not inserted with other devices.
CSS	Soft start capacitor; LM2673 and LM2679 only. Not inserted with other devices.
COUTX	0.47µF, optional high frequency output bypass capacitor; All devices.
COUT	Output capacitor(s); All devices.

*All devices have internally preset current limits, but those with adjustable current limit capability can be used to set the current limit to any value up to the maximum preset value.

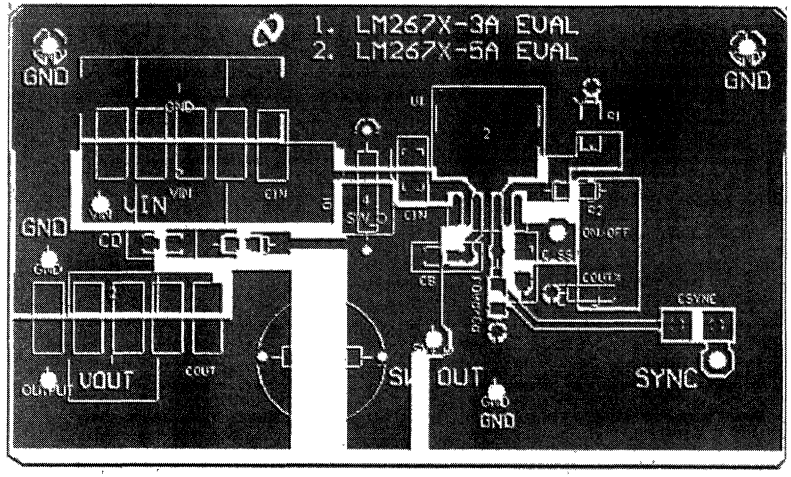
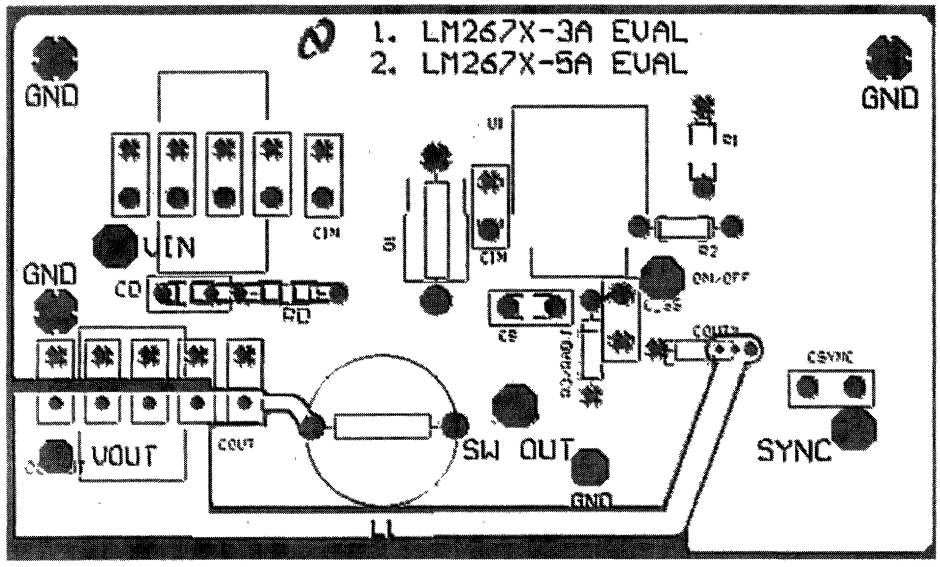
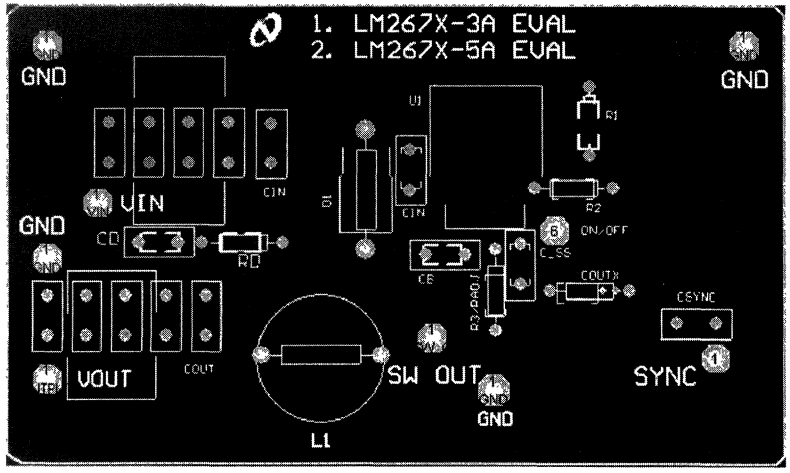


FIGURE 2. Top Layer Foil Pattern of Printed Circuit Board



10114503

FIGURE 3. Bottom Layer Foil Pattern of Printed Circuit Board



10114504

FIGURE 4. Silkscreen Image Of Printed Circuit Board

Special Notes

The evaluation board was designed primarily for circuit implementation using all surface-mount components. The small series "trace inductance", particularly from the Switch Output pin, can create a high frequency (10's of MHz) ringing signal at the switch output. If problematic, this ringing can be reduced or eliminated by the use of a series RC damper or snubber network from the switch output to ground. The addition of these components is made at the locations labeled CD and RD. Values of 0.01µF and 10Ω are good starting values that may need to be varied depending on the magnitude of parasitic factors in a given design. In an actual

Special Notes (Continued)

end application, these components are normally not required if proper care to minimize trace lengths is taken in the PCB design.

In this example, it is desired to convert a voltage range of between 8V and 12V, to 5VDC with load current of 3A. It is also desired to implement the design with surface mount components only. Softstart duration will be set to between 1 and 1.5 ms.

Example Circuit Designs

Example 1: 5V/3A Converter with Surface Mount Components.

Target Design Specifications

V_{IN} min.	8V
V_{IN} max.	16V
V_{OUT}	5V
I_{LOAD}	3A
I_{CL}	5.0A (approx.)
T_{SS}	1 to 1.5ms

TABLE 3. Component Values for an 8-12V in, 5V/3A Out LM2673S-5.0 Buck Converter

Component	Value	Suggested Part Number
U1		National LM2673S-5.0
CIN	2 x 33µF/35V	Sprague 594D336X0035R2T
CINX	0.47µF	Vitramon VJ1210U474ZXAA
CB	0.01µF/50V	Vitramon VJ1206Y103MXXA
D1	3A/60V Schottky (450mV at 3A)	Motorola MBRD360
R3*	7.15 kΩ (5.19A current limit)	DALE CRCW12067151J
L1	22µH (L41)	SUMIDA ELECTRIC CO. CDRH127-220
CSS	3.3nF/100V (softstart)	Vitramon VJ1206Y33ZJXBAB
COUTX	0.47µF	Vitramon VJ1210U474ZXAA
COUT	2 x 180µF/16V	Sprague 594D187X0016R2T

Figure 5 below shows the 5V/3A design circuit. This solution is available as evaluation board **LM2673S-5_EVAL**.

Figure 6, *Figure 7*, *Figure 8* and *Figure 9* show the output waveforms for output voltage with 500 mA load, output voltage with 1A load, output ripple with 1A load, output voltage with 3A load, output ripple with 3A load, output response to 1A transient load and output response to 3A transient load respectively.

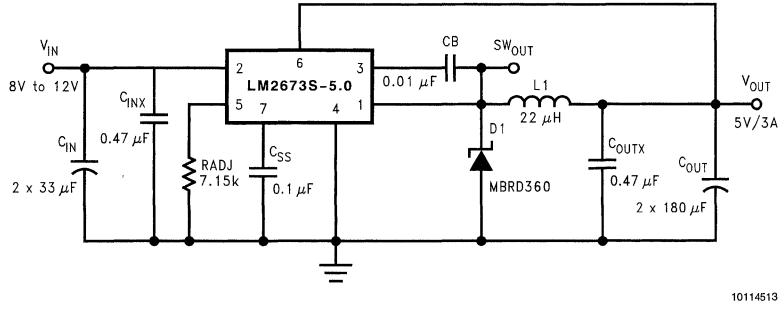
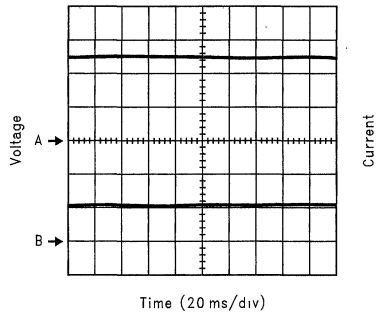


FIGURE 5. 5V/3A Design Circuit

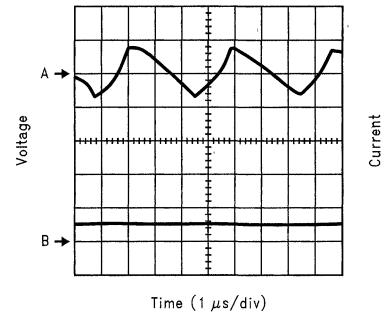


10114505

A OUTPUT VOLTAGE V_{OUT}, 2V/DIV

B LOAD CURRENT I_{LOAD} = 500mA, 500mA/DIV

Output Voltage with 500mA Load



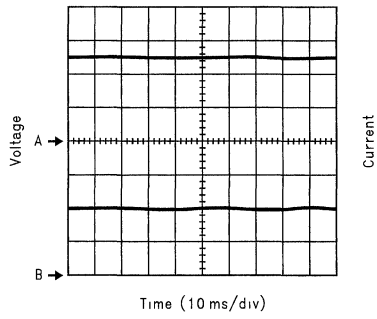
10114506

A: OUTPUT RIPPLE; 10mV/DIV

B· LOAD CURRENT· I_{LOAD} = 0 5A, 1A/DIV

Output Ripple with 500mA Load

FIGURE 6. Output Voltage Waveforms with 500mA Load

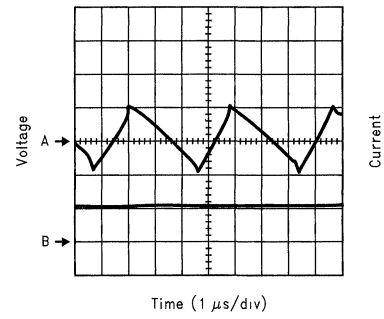


10114507

A· OUTPUT VOLTAGE. V_{OUT}, 2V/DIV

B: LOAD CURRENT I_{LOAD} = 1A, 500mA/DIV

Output Voltage with 1A Load



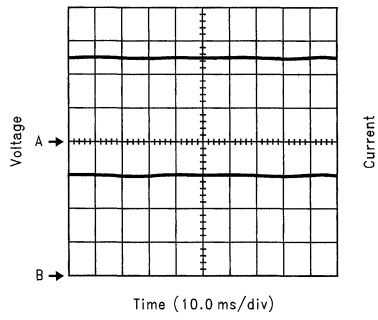
10114508

A OUTPUT RIPPLE; 10mV/DIV

B: LOAD CURRENT I_{LOAD} = 1A; 1A/DIV

Output Ripple with 1 Amp Load

FIGURE 7. Output Voltage Waveforms with 1A Load

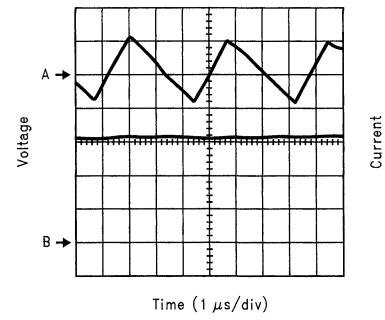


10114509

A OUTPUT VOLTAGE· V_{OUT}, 2V/DIV

B· LOAD CURRENT I_{LOAD} = 3A; 1A/DIV

Output Voltage with 3A Load



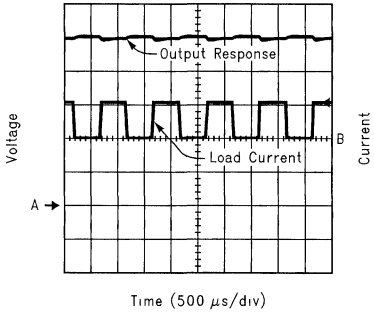
10114510

A. OUTPUT RIPPLE, 10mV/DIV

B. LOAD CURRENT I_{LOAD} = 3A; 1A/DIV

Output Ripple with 3 Amp Load

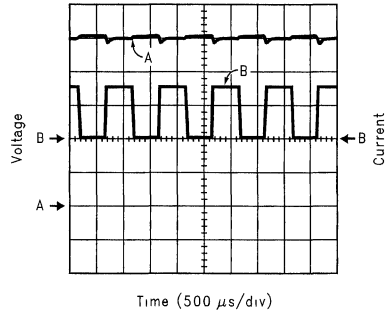
FIGURE 8. Output Voltage Waveforms with 3 Amp Load



A OUTPUT RESPONSE, 1V/DIV

B TRANSIENT LOAD CURRENT 1A/DIV

Output Response to 0~1A Transient Load



A OUTPUT RESPONSE, 1V/DIV

B TRANSIENT LOAD CURRENT: 2A/DIV

Output Response to 0~3A Load Transient

FIGURE 9. Output Response To Load Transient

Example 2: 5V/5A Design with Surface Mount Components

For this example, it is desired to design a power supply to convert an input voltage within the range of 14V and 28V to an output voltage of 5V with a maximum load current of 5A using only surface mount components. In addition, the current limit of the regulator will be set to approximately 7.0A, and the softstart time will be set to approximately 1.0ms to limit the startup surge current.

Target Design Specifications:

V_{IN} min.	14V
V_{IN}max.	28V
V_{OUT}	5V
I_{LOAD}	5A
I_{CL}	7.0A (approx.)
T_{SS}	1.0ms (approx.)

TABLE 4. Component Values for an 14V-28V in, 5V/5A Out LM2679S-5.0 Buck Converter

Component	Value	Suggested Part Number
U1		National LM2679S-5.0
CIN	3 x 15µF/50V	Sprague 594D336X0035R2T
CINX	0.47µF	Vitramon VJ1210U474ZXAA
CB	0.01µF/50V	Vitramon VJ1206Y103ZXXA
D1	8A/35V Schottky (500mV at 5A)	Motorola MBRD835L
R3*	4.99 kΩ (7.19A current limit)	DALE CRCW12064991J
L1	15µH (L50)	Pulse Engineering P0850 or Coilcraft D05022P-153
CSS	4.7nF/100V (1.0ms softstart)	Vitramon VJ1206Y47ZJXBAB
COUTX	0.47µF	Vitramon VJ1210U474ZXAA
COUT	2 x 180µF/16V	Sprague 594D187X0016R2T

Figure 10 below shows the circuit for the 5V/5A design. This solution is available as evaluation board **LM2679S-5_EVAL**.

Figure 11, *Figure 12*, *Figure 13*, *Figure 14*, and *Figure 15* show the output waveforms for output voltage with 500 mA load, output voltage with 2.5A load, output ripple with 2.5A load, output voltage with 5A load, output ripple with 5A load, output response to 500mA transient load, output response to 2.5A transient load and output response to 5A transient load respectively.

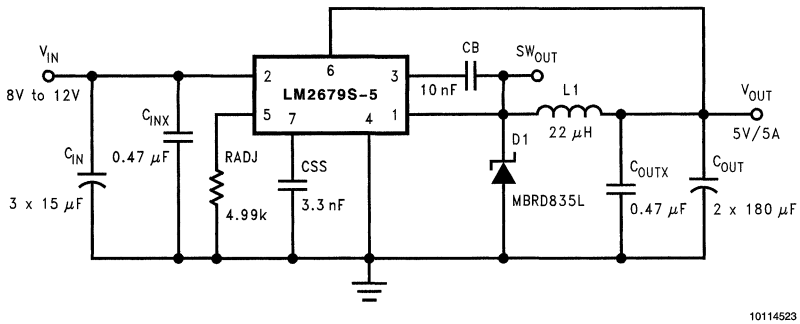
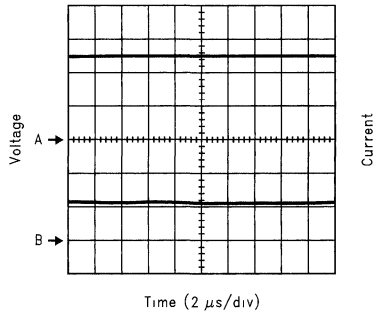


FIGURE 10. 5V/5A Design Circuit

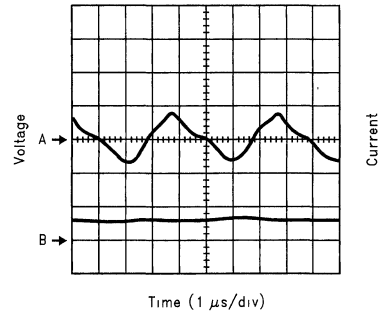
Example 2: 5V/5A Design with Surface Mount Components (Continued)



A OUTPUT VOLTAGE V_{OUT}, 2V/DIV

B LOAD CURRENT I_{LOAD} = 500mA, 500mA/DIV

Output Voltage with 500mA Load

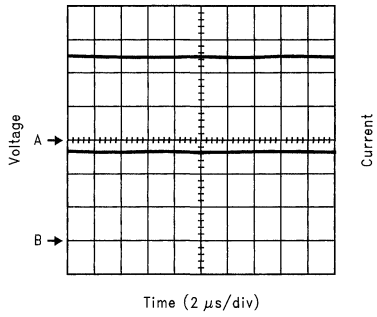


A OUTPUT RIPPLE; 100mV/DIV

B LOAD CURRENT I_{LOAD} = 500mA; 1A/DIV

Output Ripple with 500mA Load

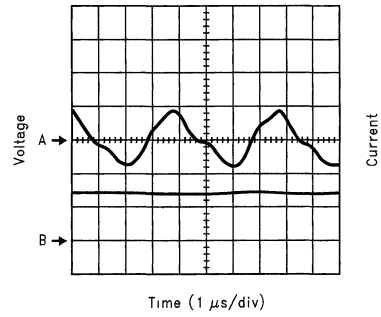
FIGURE 11. Output Voltage Waveforms with 500mA Load



A OUTPUT VOLTAGE. V_{OUT}, 2V/DIV

B LOAD CURRENT I_{LOAD} = 2 5A, 1A/DIV

Output Voltage with 2.5A Load



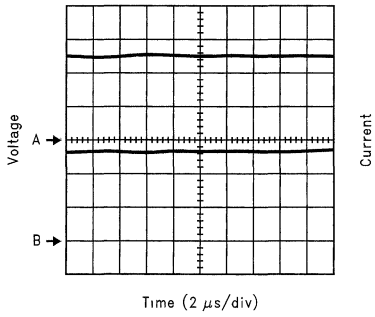
A OUTPUT RIPPLE, 100mV/DIV

B· LOAD CURRENT· I_{LOAD} = 2.5A; 2A/DIV

Output Ripple with 2.5A Load

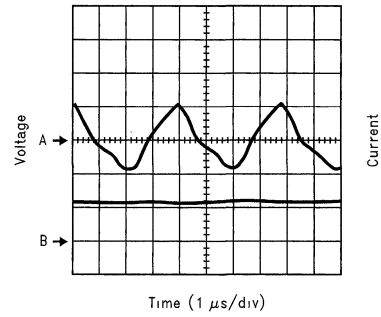
FIGURE 12. Output Voltage Waveforms with 2.5A Load

Example 2: 5V/5A Design with Surface Mount Components (Continued)



A OUTPUT VOLTAGE. V_{OUT}, 2V/DIV
B LOAD CURRENT I_{LOAD} = 5A; 2A/DIV

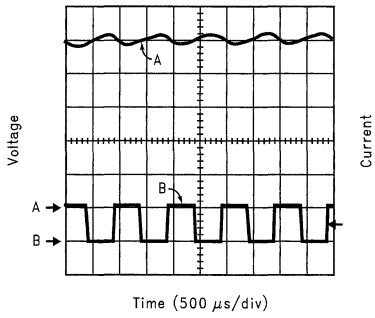
Output Voltage with 5A Load



A OUTPUT RIPPLE, 100mV/DIV
B. LOAD CURRENT. I_{LOAD} = 5A; 5A/DIV

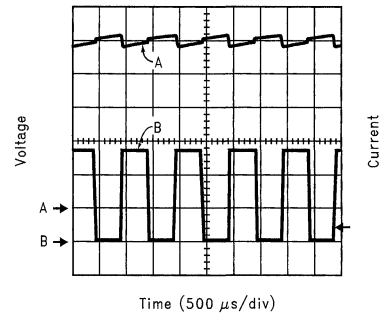
Output Ripple with 5A Load

FIGURE 13. Output Voltage Waveforms with 5A Load



A. OUTPUT RESPONSE, 1V/DIV
B· TRANSIENT LOAD CURRENT 500mA/DIV

Output Response to 0–0.5A Transient Load



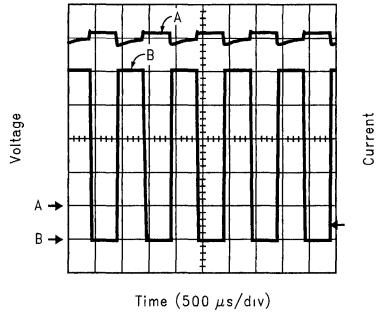
A. OUTPUT RESPONSE, 1V/DIV
B TRANSIENT LOAD CURRENT 1A/DIV

Output Response to 0–2.5A Load Transient

FIGURE 14. Output Response To Load Transient

Example 2: 5V/5A Design with Surface Mount Components

(Continued)



A OUTPUT RESPONSE 1V/DIV
B LOAD CURRENT I_{LOAD} = 1A/DIV

FIGURE 15. Output Response to 0–5A Transient Load

Operating the Evaluation Boards

SETUP

The **LM2673S-5_EVAL** and **LM2679S-5_EVAL** evaluation boards come ready to be tested. The only setup needed is connecting the input voltage to the VIN and GND posts. The output can be taken from the VOUT post. The other signals of interest, switch output (SW out) and softstart (C_SS) posts, are clearly marked for use in checking the signal integrity. The softstart post has an ON/OFF input when this feature is being used.

OPERATING CONDITIONS

The input source for the LM267x family of regulators must be 8V or greater for proper setup and operation. The input voltage range for **LM2673S-5_EVAL** evaluation board is from 8V to 12V and the range for **LM2679S-5_EVAL** is from 14V to 28V. The maximum voltage rating of the LM267x family of regulators is 40V.

Load can be applied from 0A to the maximum for the design. Higher current above the design current limit will result in activation of the design current limit circuit. It is advisable to have a minimal load of (at least 10mA) during startup when the input to output differential voltage is greater than 10V to prevent output ramping beyond desired value.

PCB LAYOUT OPTIMIZATION

As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance can generate voltage transients which can cause problems. For minimal inductance and ground loops, the printed circuit traces should be as wide and short as possible on the PCB. For best results, external components should be located as close to the switcher IC as possible using ground plane construction or single point grounding.

If **open core inductors are used,** special care must be taken as to the location and positioning of this type of inductor. Allowing the inductor flux to intersect sensitive feedback, IC groundpath and C_{OUT} wiring can cause problems.

When using the adjustable version, special care must be taken as to the location of the feedback resistors and associated wiring. Physically locate both resistors near the IC, and route the wiring away from the inductor, especially an open core type of inductor.

LM2661/3/4 Evaluation Board

National Semiconductor
Application Note 1142
Clinton Jensen

Introduction

The LM2661, LM2663, and LM2664 are part of a family of CMOS charge-pump voltage converters (*Table 2*). Each uses two small capacitors to achieve voltage inversion or voltage doubling without the cost, size, and EMI of inductor based converters. Each device has a shutdown feature and the LM2661 and LM2663 also provide the ability to run the clock oscillator from an external source. You may also slow the clock with an external capacitor on the LM2661 and LM2663. The small size and low profile of these circuits makes them attractive for cellular phones, laptop computers, Op Amp power supplies, interface power supplies, medical instruments, PDAs, and handheld instruments.

The LM2661 comes in SO-8 and MSOP-8 packages and requires only an extra diode to double the input voltage and provide up to 100mA of output current. It has a typical efficiency of 88% at 100mA output and a typical output resistance of 6.5Ω. This circuit typically draws only 500nA of supply current in shutdown mode and 120µA when operating. The internal oscillator frequency is 80kHz and the input voltage range is +2.5V to +5.5V (Note 1). The LM2661 is also capable of inverting an input voltage from +1.5V to +5.5V when used in a different configuration.

The LM2663 comes in a SO-8 package and inverts the input voltage to provide up to 200mA of output current. It has a typical efficiency of 86% at 200mA output and a typical output resistance of 3.5Ω. This circuit draws only 10µA of supply current in shutdown and 300µA when operating. The internal oscillator frequency is 150kHz and the input voltage range is +1.5V to +5.5V (Note 1). The LM2663 is also capable of doubling an input voltage from +2.5V to +5.5V when used in a different configuration.

The LM2664 comes in a SOT23-6 package and inverts the input voltage to provide up to 40mA of output current. It has a typical efficiency of 91% at 40mA output and a typical output resistance of 12Ω. This circuit draws only 1µA of supply current in shutdown and 220µA when on. The oscillator frequency is 160kHz and the input voltage range is +1.8V to +5.5V (Note 1).

Note 1: Maximum input voltage for any input on this evaluation board is +5.5V

Figure 1 contains the schematic for each circuit used.

A silkscreen for the evaluation board is shown in *Figure 2*.

A listing of the products used is shown in *Table 1*.

A listing of the switched capacitor family is given in *Table 2*.

Introduction (Continued)

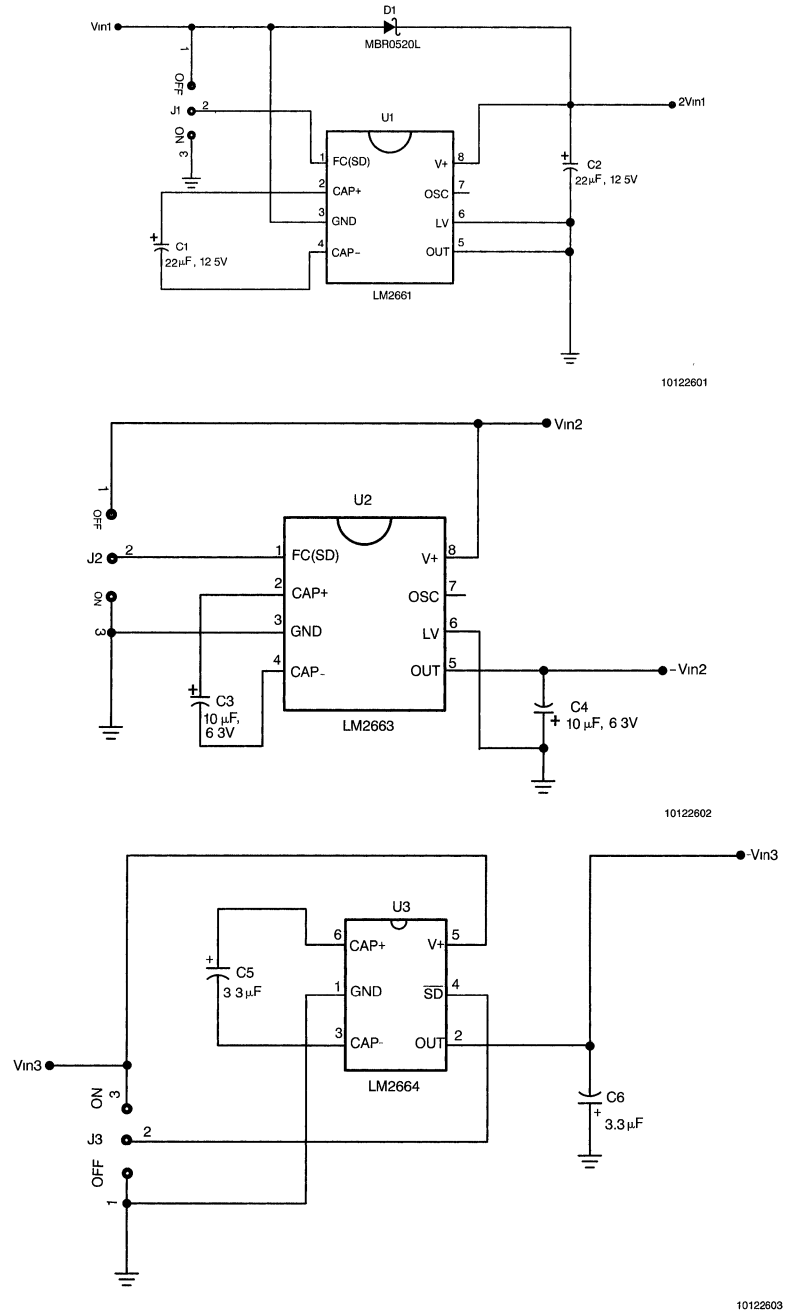


FIGURE 1. Schematics

Discussion and Component Selection

On this evaluation board, the **LM2661** is used in the doubling configuration. This configuration uses only two capacitors and one diode. There is a manual shutdown jumper designated as J1 included. The internal oscillator is used with a frequency of 80kHz. In doubling mode, the oscillator frequency can only be modified using an external capacitor and cannot be driven by an external clock. The Schottky diode D1 is needed only for start-up but should be able to handle the current required to charge the output capacitor (I=C*dV/dt). An MBR0520LT1 20V, 0.5A diode is used on this board. Capacitor selection is very important. The capacitors chosen determine the output voltage ripple as well as the output resistance (*Equation (1)* and *Equation (2)*). From these equations it is easy to see how capacitor value and ESR help determine the output resistance and output voltage ripple. For this circuit Cornell-Dubilier ESRD type 22µF polymer electrolytic capacitors are used (Model ESRD220M12B). These capacitors are used because of their low ESR (typically 20 mΩ @ 100kHz) as well as stable temperature and frequency characteristics. Therefore they enhance the parts performance. The output voltage ripple was measured at less than 55 mV peak to peak with a 100 mA load. Tantalum and ceramic capacitors and other values may be used as well to fit different performance, size, or cost requirements. Universal pads have been put on the evaluation board so that the capacitors can be replaced with those of a different size.

The **LM2663** is configured as an inverter on this board. A manual shutdown is included and designated J2. The internal oscillator frequency of 150kHz is used. The capacitor selection here is important as well since the output resistance and voltage ripple equations are the same as they are for the LM2661 (*Equation (1)* and *Equation (2)*). This circuit runs at a higher frequency than the LM2661 so smaller capacitor values can be used. For this circuit Cornell-Dubilier ESRD type 10µF polymer electrolytic capacitors are used (Model ESRD100M06B). Once again the low ESR (typically 42 mΩ @ 100kHz) and stable characteristics of these capacitors are the reasons they were chosen. Output voltage ripple was measured to be less than 140 mV peak to peak with a 200 mA load. Other types and sizes of capacitors may be used here as well for different performance, size, or cost requirements.

The **LM2664** is also used as an inverter on this board. A manual shutdown designated as J3 is included. The LM2664 does not have an adjustable frequency; it is fixed at 160kHz. This circuit has the same equations for output resistance and output voltage ripple as the previous two circuits and the capacitor selection is once again important (*Equation (1)* and *Equation (2)*). Taiyo Yuden multi-layer ceramic chip 3.3µF capacitors are used for this circuit (Model LMK316BJ335ML-T). These capacitors are chosen for their low ESR (measured ≅ 25 mΩ) and small (1206) case size. They show the high performance of the LM2664 as well as the small size for the complete circuit. The output voltage ripple was measured to be less than 75mV peak to peak with a 40 mA load. Again other types and sizes of capacitors may be used for different performance and/or size requirements.

$$R_{OUT} \cong 2R_{SW} + \frac{2}{f_{OSC} \times C_1} + 4ESR_{C1} + ESR_{C2} \quad (1)$$

where R_{SW} is the sum of the ON resistance of the internal switches. R_{SW} is typically 1.4Ω for the LM2661, 0.9Ω for the LM2663, and 4Ω for the LM2664.

$$V_{RIPPLE} = \frac{I_L}{f_{OSC} \times C_2} + 2 \times I_L \times ESR_{C2} \quad (2)$$

Note 2: In these equations C_2 is always the output capacitor of the circuit.

Discussion and Component Selection (Continued)

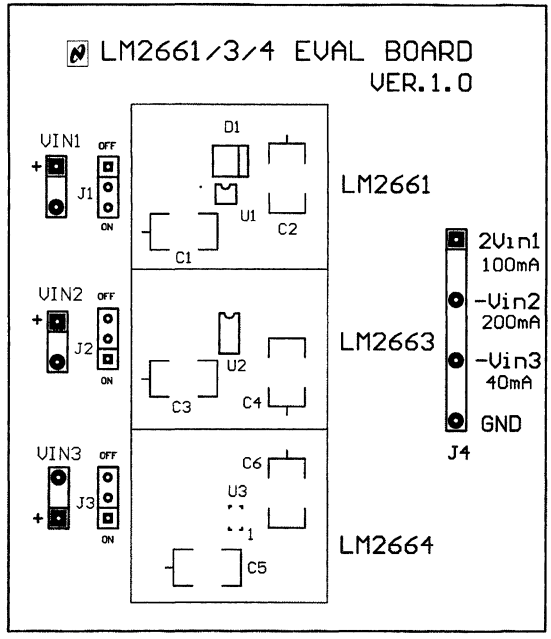


FIGURE 2. Silkscreen

Discussion and Component Selection (Continued)

TABLE 1. Components List

Designator	Part Type	Manufacturer and Model #	Footprint	Description
U1	LM2661	National Semiconductor Corp.	MSOP-8	Charge-pump voltage converter
D1	Diode	Motorola (MBR0520LT1)	SOD123	20V, 0.5A Start-up diode
C1	22µF	Cornell-Dubilier (ESRD220M12B)	D-Case	Low ESR charge-pump capacitor, polymer electrolytic
C2	22µF	Cornell-Dubilier (ESRD220M12B)	D-Case	Low ESR charge-pump capacitor, polymer electrolytic
U2	LM2663	National Semiconductor Corp.	SO-8	Charge-pump voltage converter
C3	10µF	Cornell-Dubilier (ESRD100M06B)	D-Case	Low ESR charge-pump capacitor, polymer electrolytic
C4	10µF	Cornell-Dubilier (ESRD100M06B)	D-Case	Low ESR charge-pump capacitor, MLCC
U3	LM2664	National Semiconductor Corp.	SOT23-6	Charge-pump voltage converter
C5	3.3µF	Taiyo Yuden (LMK316BJ335ML-T)	1206	Low ESR charge-pump capacitor, MLCC
C6	3.3µF	Taiyo Yuden (LMK316BJ335ML-T)	1206	Low ESR charge-pump capacitor, MLCC
VIN1, VIN2, VIN3, J1, J2, J3, J4	Headers (36 posts per strip)	Amphenol (842-800-272-015) Newark stock # 87F6830	0.1" spacing	Connectors for input voltage, output voltage, and ON/OFF jumpers (2/3 strip used, 22 posts used, 19 actual pins used per board)
J1, J2, J3	Shunts	Circuit Assembly Corp. (CA-02SJC-B) Newark stock # 90F9279		Shunts for ON/OFF jumpers, shorts 2 pins, 3 shunts used per board

Contact Information

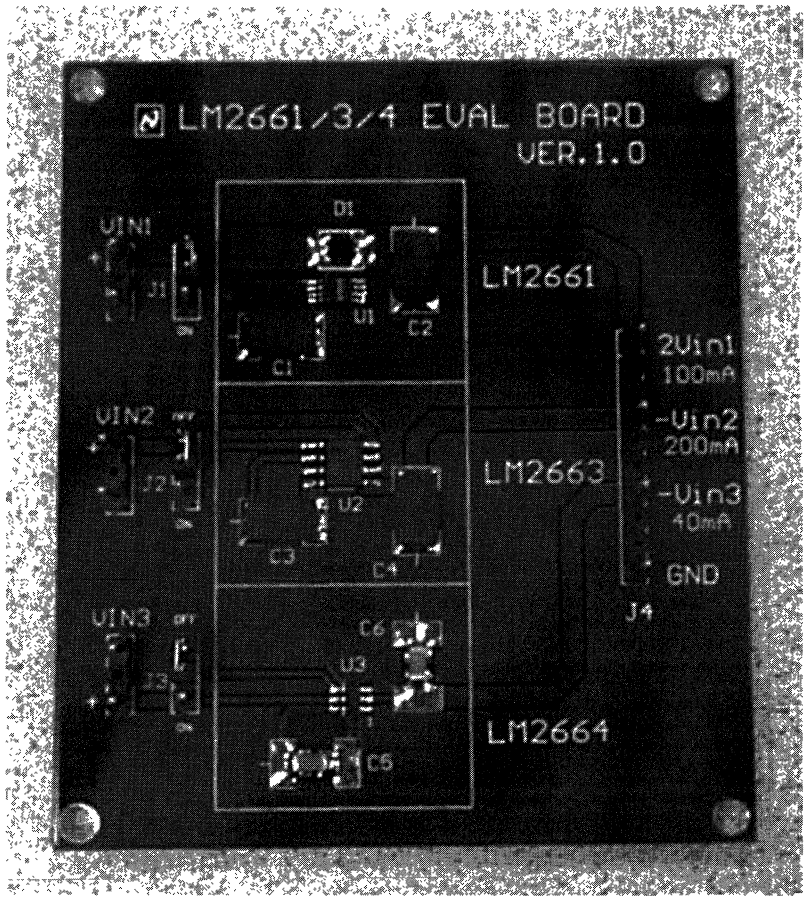
National Semiconductor Corp.	www.national.com	1-800-272-9959
Motorola	www.mot.com	1-800-521-6274
Cornell-Dubilier	www.cornell-dubilier.com	1-508-996-8564
Taiyo Yuden	www.T-Yuden.com	1-800-348-2496
Newark	www.Newark.com	1-800-298-3133

Discussion and Component Selection (Continued)

TABLE 2. Switched Capacitor Family

Product	Function	R_O (ohms)	I_{OUT} (mA)	V_{IN} range	f_{OSC} kHz	I_Q (µA)	Shutdown	Freq. Control	Freq. Sync	Package
LM2660	$-V_{IN}$ or $2V_{IN}$	6.5	100	1.5 to 5.5	10/80	120/400	No	Yes	Yes	MSOP-8, SO-8
LM2661	$-V_{IN}$ or $2V_{IN}$	6.5	100	1.5 to 5.5	80	1000	Yes	No	Yes	MSOP-8, SO-8
LM2662	$-V_{IN}$ or $2V_{IN}$	3.5	200	1.5 to 5.5	20/150	300/1300	No	Yes	Yes	SO-8
LM2663	$-V_{IN}$ or $2V_{IN}$	3.5	200	1.5 to 5.5	150	1300	Yes	No	Yes	SO-8
LM2664	$-V_{IN}$	12	40	1.8 to 5.5	160	220	Yes	No	No	SOT23-6
LM2665	$2V_{IN}$	12	40	1.8 to 5.5	160	550	Yes	No	No	SOT23-6
LM3350	3/2 V_{IN} or 2/3 V_{IN}	4.2/1.8	50	1.5 to 5.5	1600	3750	Yes	No	No	MSOP-8
LM3351	3/2 V_{IN} or 2/3 V_{IN}	4.2/1.8	50	1.5 to 5.5	400	1110	Yes	No	No	MSOP-8

Discussion and Component Selection (Continued)



10122607

LM2651_3.3V_EVAL 1.5A High Efficiency Synchronous Switching Regulator Evaluation Board

National Semiconductor
Application Note 1143
Ifeanyi Nwachukwu

Introduction

The LM2651 switching regulator provides high efficiency power conversion over a 100:1 load range (1.5A to 15mA). This feature makes the LM2651 an ideal fit in battery powered applications.

Synchronous rectification and 75 mΩ internal switches provide up to 97% efficiency. At light loads, the LM2651 enters a low power hysteretic or sleep mode to keep the efficiency high. In many applications, the efficiency still exceeds 80% at 15 mA load.

A shutdown pin is available to disable the LM2651 and reduce the supply current to 7 µA but the shutdown function is not available on this board. The IC contains patented current sensing circuitry for current mode control. This feature eliminates the external current sensing required by other current mode DC to DC converters. The IC has a 300kHz fixed frequency internal oscillator. The high oscillator frequency allows the use of extremely small, low profile components.

The evaluation board can be obtained by ordering part number LM2651_3.3V_EVAL from your local National Semiconductor sales office, or National's website at www.national.com.

Evaluation Board Design

The evaluation board is designed to supply 3.3V at 15 mA up to 1.5A. The input voltage range is 4V to 14V. Components were selected based on the design procedure in the LM2651 datasheet. PCB layout is critical to reduce noise and ensure specified performance for any power supply design. To minimize the parasitic inductance in the loop of input capacitors and the internal MOSFETs, connect the capacitors to V_{IN} and PGND pins with short and wide traces. This is important because the rapidly switching current, together with wiring inductance can generate large voltage spikes that may cause noise problems. The feedback trace from the output to the feedback pin should be wide, short and kept away from the flux field of the inductor. The artwork for the evaluation board is shown at the end of this application note and the schematic shown in *Figure 1*. The parts list is given in *Table 1*. The pictorial representations of top, bottom and silkscreen layers are shown at the end of this application note.

When an undervoltage situation occurs, the output voltage can be pulled below ground as the inductor current is reversed through the synchronous FET. For applications which need to be protected from a negative voltage, a clamping diode D2 is recommended. When used, D2 should be connected cathode to V_{OUT} and anode to ground. A diode rated for a minimum of 2A is recommended.

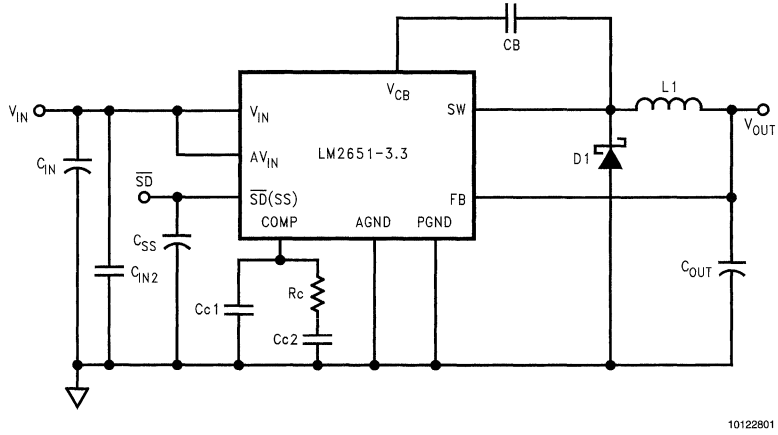


FIGURE 1. LM2651_3.3V_EVAL Schematic

Evaluation Board Design (Continued)

TABLE 1. LM2651_3.3V_EVAL Bill of Material

Component	Value	Suggested Part Number
U1		National's LM2651-3.3
L1	22µH	Coilcraft D03316P-223
C_{IN} (Input Capacitor)	100µF, 16V	Sprague 594D107X0016D2T
C_{IN2} (Input Capacitor)	0.1µF	Ceramic Capacitor
CB (Bootstrap Capacitor)	0.1µF	Ceramic Capacitor
C_{SS} (softstart Capacitor)	4.7nF	Ceramic Capacitor
C_{OUT} (Output Capacitor)	120µF, 6.3V	Sprague 594D127X06R3C2T
CC1 (Compensation Capacitor)	2.2nF	Ceramic Capacitor
CC2 (Compensation Capacitor)	100pF	Ceramic Capacitor
RC (Compensation Resistor)	30 kΩ, 5%	Resistor
D1	1A Schottky Diode	Motorola MBRA130LT3

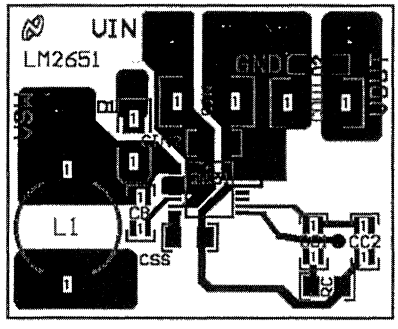
Operating the Evaluation Board

SETUP

The LM2651_3.3V_EVAL evaluation board comes ready to be tested. The only setup needed is connecting the input voltage to the V_{IN} and GND posts. The load and output are connected to the V_{OUT} post.

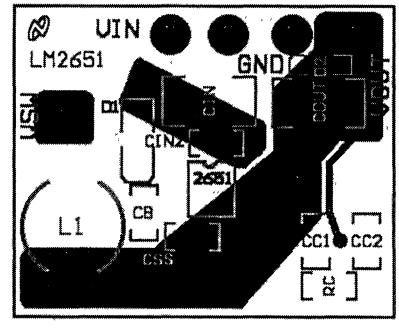
OPERATING CONDITIONS

The input voltage to the LM2651-3.3 regulator must be within the range of 4V to 14V DC for proper operation. The device will not function properly with voltages below 4V and damage may occur if any voltage greater than 16V is applied.



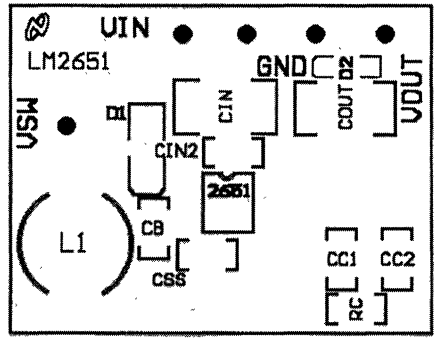
10122802

Layout Top Layer



10122803

Layout Bottom Layer



10122804

Layout Silkscreen

Maximizing Start-Up Loads with the LM3352 Regulated Buck/Boost Switched Capacitor Converter

National Semiconductor
Application Note 1144
Clinton Jensen

The LM3352 is a regulated switched capacitor voltage converter. It achieves Buck/Boost operation by using a variety of different switching schemes to produce seven different gains between a minimum of ½ and a maximum of 2. At any given time the input and output comparators determine the required gain to give a regulated output voltage. The switching scheme used does however pose some minor restrictions regarding start-up of the IC with the output loaded. For the majority of applications a power-on reset circuit will be used. In these cases the restrictions are of no concern regardless of the type of load presented to the LM3352. For applications not using a power-on reset circuit the restrictions are described below.

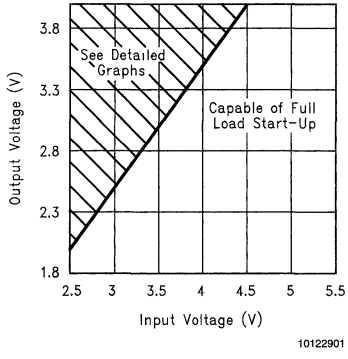
As the part starts up, it cycles through the necessary gain regions (gains) until regulation is reached. Each gain region has an associated output impedance which may be greater than or less than its neighboring gain region. The greater the output impedance, the less current the part is able to supply without losing regulation. Therefore the weakest gain region (the gain with the highest output impedance) sets the maximum start up current for the part. For the LM3352, the weakest region is from $V_{IN} = V_{OUT}$ to $V_{IN} = V_{OUT} + 200mV$. For some output voltage options, the part will never cycle through this region and therefore maximum start up current will be equal to the maximum rated load current.

The datasheet shows a maximum start up current of 45 mA. This number is a worst case number encompassing all voltage options across all input voltages as well as the worst case condition of $T_A = 85°C$. As mentioned above, the weakest region is setting this limit. If the input range is more limited than the datasheet limits, the circuit may start up with loads greater than 45 mA. This effect can also change with different load types. For example, some CMOS loads will not draw significant current until a certain operational threshold voltage is reached. If this threshold voltage occurs after the LM3352 has cycled through the gain region of 1 there will be no start-up restrictions. However, systems with resistive loads will draw current as soon as voltage is applied. A description of the limitations for a resistive load follows.

Because the maximum load current during start-up is input voltage dependent *(See graph titled Start-up Regions)*, lower input voltages will need to use the gain of 1 during start-up and therefore will have decreased current capabilities. Due to the added effect of the R_{OUT}, input voltages slightly higher than the output will be affected as well *(See graphs titled Maximum Start-up Load Current vs. Input Voltage)*. These graphs are taken using a resistive load on the output.

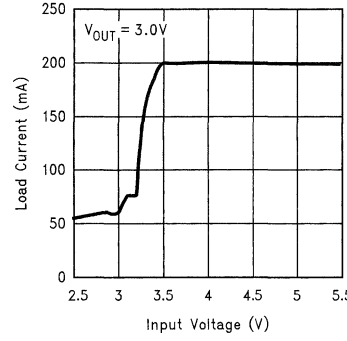
With higher input voltages that do not need to use or go through the weakest gain region during start-up, the maximum load during start-up is dramatically increased. As the graphs show, much higher loads than 45 mA can be tolerated during start-up with high input voltage conditions. The graphs are also at the worst case condition of $T_A = 85°C$. This should clarify the start-up issues involved with the LM3352 and allow more possibilities of use for those who are unable to use the part with the low stated maximum of 45 mA in the datasheet. If larger start-up currrents are expected for an application that has a minimum input voltage lower than the minimum input required, a power-on reset circuit such as the LP3470 is still recommended.

Start-Up Regions



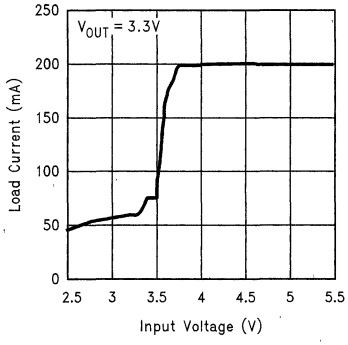
10122901

Maximum Start-Up Load Current vs. Input Voltage



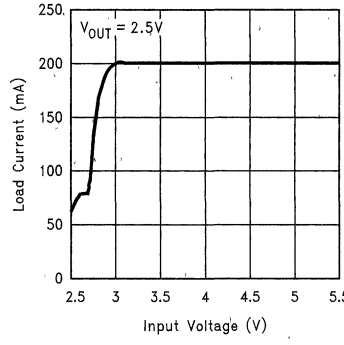
10122902

Maximum Start-Up Load Current vs. Input Voltage



10122903

Maximum Start-Up Load Current vs. Input Voltage



10122904

Linear Regulators: Theory of Operation and Compensation

National Semiconductor
Application Note 1148
Chester Simpson

Introduction

The explosive proliferation of battery powered equipment in the past decade has created unique requirements for a voltage regulator that cannot be met by the industry standards like the LM340 or the LM317. These regulators use an NPN Darlington pass transistor (*Figure 1*), and will be referred to in this document as **NPN regulators**. The demand for higher performance is being met by the newer **low-dropout (LDO)** regulators and **quasi-LDO** regulators.

The NPN Regulator

The NPN Darlington pass transistor with PNP driver used in an NPN regulator requires that at least 1.5V to 2.5V be maintained from input-to-output for the device to stay in regulation. This minimum voltage "headroom" (called the **dropout voltage)** is:

$$V_{DROP} = 2V_{BE} + V_{SAT} \text{ (NPN REG)}$$

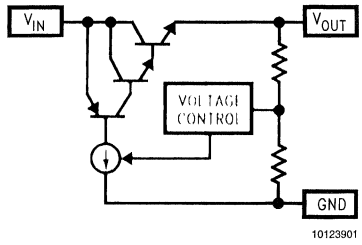


FIGURE 1. NPN REGULATOR

The LDO Regulator

In the low-dropout (LDO) regulator, the pass transistor is a single PNP transistor (*Figure 2*). The big advantage of the LDO is that the PNP pass transistor can maintain output regulation with very little voltage drop across it:

$$V_{DROP} = V_{SAT} \text{ (LDO REGULATOR)}$$

Full-load dropout voltages < 500 mV are typical. At light loads, dropout voltages can fall as low as 10 to 20 mV.

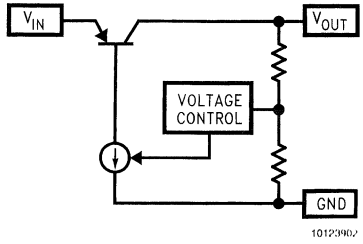


FIGURE 2. PNP LDO REGULATOR

The Quasi-LDO Regulator

Another regulator configuration that is becoming very popular in certain applications (like 5 - 3.3V conversion) is the quasi-LDO regulator (*Figure 3*). The quasi-LDO is so named because it is "half way" between the NPN Darlington and the true LDO. The pass transistor is made up of a single NPN transistor being driven by a PNP. As a result, the dropout voltage is less than the NPN Darlington regulator, but more than an LDO:

$$V_{DROP} = V_{BE} + V_{SAT}$$

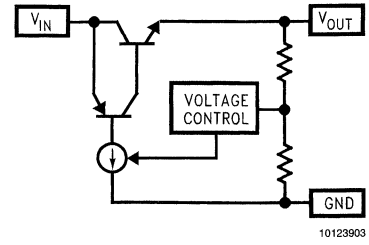


FIGURE 3. QUASI-LDO REGULATOR

Regulator Operation

All three of these regulator types regulate the output voltage to a fixed (constant) value using the same technique (*Figure 4*).

The output voltage is sampled (measured) through a resistive divider which is fed into the inverting input of the error amplifier. The non-inverting input is tied to a reference voltage, which is derived from an internal bandgap reference. The error amplifier will always try to force the voltages at it's input to be equal. To do this, it sources current as required to provide sufficient load current to maintain the output voltage at the regulated value which is given by:

$$V_{OUT} = V_{REF} (1 + R1/R2)$$

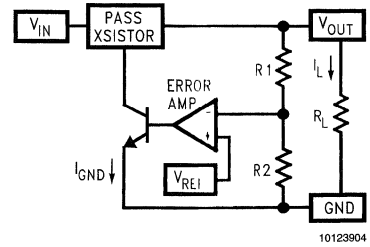


FIGURE 4. VOLTAGE REGULATOR

Performance Comparison

The primary differences in performance between the NPN, LDO, and quasi-LDO are in the parameters of **dropout voltage** (previously defined) and **ground pin current**. For this analysis, we will define ground pin current (I_{GND}) as shown in *Figure 4*, neglecting the small IC bias currents which also flow to ground. It can be seen that the value of I_{GND} is the load current I_L divided by the gain of the pass transistor.

The high gain of the Darlington in an NPN regulator means it requires very little drive to source I_L, so it's ground pin current is very low (typically a few mA). The quasi-LDO also has very good performance, with products like National's LM1085 being able to source more than 3A with less than 10 mA of ground pin current.

The ground pin current of an LDO is typically much higher At full load current, PNP beta values of 15 - 20 are not unusual, which means the LDO ground pin current can be as high as 7% of the load current

A big advantage of NPN regulators is that they are unconditionally stable (most require no external capacitors). An LDO does require at least one external capacitor on the output to reduce the loop bandwidth and provide some positive phase shift. Quasi-LDOs typically require some output capacitance, but much less than an LDO and with less restrictive limits on its performance characteristics.

Feedback and Loop Stability

All voltage regulators use a feedback loop to hold the output voltage constant. The feedback signal experiences changes in both gain and phase as it goes through the loop, and the amount of phase shift which has occurred at the unity gain (0 dB) frequency determines stability.

BODE PLOTS

Understanding stability requires the use of **Bode Plots**, which show the loop gain (in **dB**) plotted as a function of frequency (*Figure 5*). Loop gain and associated terms are defined in the next sections.

Loop gain can be measured on a network analyzer, which injects a low-level sine wave into the feedback path and then measures the gain response while the frequency of the signal is swept from DC up to the frequency where the gain drops well below 0 dB

Bode plots are convenient tools because they contain all the information necessary to determine if a closed-loop system is stable. However, decoding the information contained in a Bode plot requires understanding the key elements· **loop gain, phase margin, poles and zeros**.

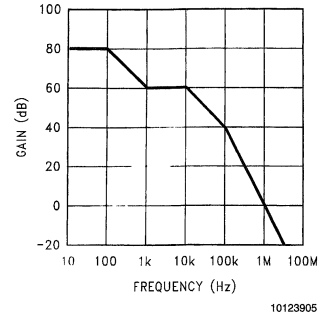


FIGURE 5. TYPICAL BODE PLOT

LOOP GAIN

Every closed-loop system has a characteristic called **loop gain**. In this analysis of voltage regulators, loop gain will be defined as the magnitude of the voltage gain that the feedback signal experiences as it travels through the loop. The block diagram of the LDO in *Figure 2* will be redrawn to illustrate this concept (*Figure 6*).

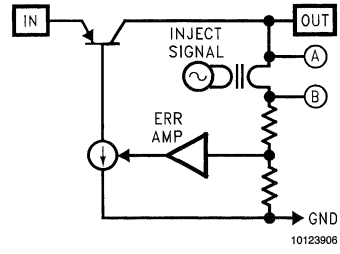


FIGURE 6. LOOP GAIN EXAMPLE

A transformer is used to inject an AC signal into the feedback path between points "A" and "B" Using this transformer, a small-signal sine wave is used to "modulate" the feedback signal. The AC voltages at "A" and "B" are measured and used to calculate loop gain.

The loop gain is defined as the ratio of the two voltages:

$$\text{Loop Gain} = V_A/V_B$$

Feedback and Loop Stability

(Continued)

It is important to note that the signal starting at the V_B point has a phase shift introduced into it as it travels through the loop (eventually arriving at the V_A point). The amount of phase shift is critical in determining stability.

FEEDBACK

Feedback is used in all voltage regulators to hold the output voltage constant. The output voltage is sampled through a resistive divider (*Figure 6*), and that signal is fed back to one input of the error amplifier. Since the other input of the error amplifier is tied to a reference voltage, the error amplifier will supply current as required to the pass transistor to keep the regulated output at the correct DC voltage.

It is important to note that for a stable loop, **negative feedback** must be used. Negative feedback (sometimes called **degenerative feedback)** is opposite in polarity to the source signal (see *Figure 7*).

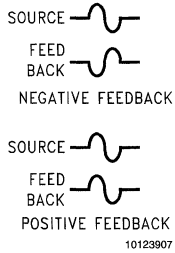


FIGURE 7. FEEDBACK SIGNALS

Because it is opposite in polarity with the source, negative feedback will always cause a response by the loop which opposes any change at the output. This means that if the output voltage tries to rise (or fall), the loop will respond to force it back to the nominal value.

Positive Feedback occurs when the feedback signal has the same polarity as the source signal. In this case, the loop responds in the same direction as any change which occurs at the output. This is clearly unstable, since it does not **cancel out** changes in output voltage, but **amplifies** them.

It should be obvious that no one would intentionally design positive feedback into the loop of a linear regulator, but **negative feedback becomes positive feedback if it experiences a phase shift of 180°.**

PHASE SHIFT

Phase shift is defined as the total amount of phase change (referred to the starting point) that is introduced into the feedback signal as it goes around the loop. Phase shift (expressed in degrees) is most often measured using a network analyzer.

Ideal negative feedback is 180° out of phase wit the source (*Figure 8*), so its "starting point" is at –180°. This "180°" offset can also be seen in *Figure 7*, as the negative feedback waveforms are exactly one half cycle shifted with respect to each other.

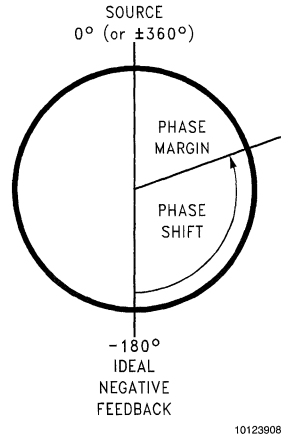


FIGURE 8. PHASE SHIFT MAP

It can be seen that starting at –180°, an additional phase shift of 180° (positive or negative) brings the signal back to zero, **which is in phase with the source signal and would cause the loop to be unstable.**

PHASE MARGIN

Phase margin is defined as the difference (in degrees) between the total phase shift of the feedback signal and –180° **at the frequency where the loop gain is equal to 0 dB (unity gain).** A stable loop typically needs at least 20° of phase margin.

Phase shift and phase margin can be calculated using the poles and zeros present in the Bode plot.

POLES

A pole (*Figure 9*) is defined as a point where the slope of the gain curve changes by –20 dB/decade (with reference to the slope of the curve prior to the pole). Note that the effect is additive: each additional pole will increase the negative slope by the factor **"n" x (–20 dB/decade)**, where "n" is the number of additional poles.

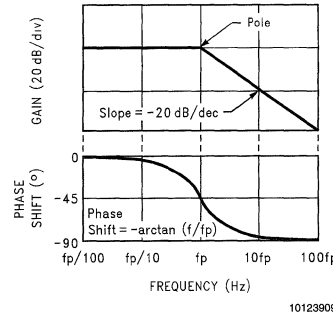


FIGURE 9. POLE GAIN/PHASE PLOT

Feedback and Loop Stability

(Continued)

The phase shift introduced by a single pole is frequency dependent, varying from 0 to −90° (with a phase shift added by a pole (frequency). The most important point is that nearly all of the phase shift added by a pole (or zero) occurs within the frequency range one decade above and one decade below the pole (or zero) frequency.

NOTE: a single pole can add only −90° of total phase shift, so at least two poles are needed to reach −180° (which is where instability can occur).

ZEROS

A zero (*Figure 10*) is defined as a point where the gain changes by +20 dB/decade (with respect to the slope prior to the zero). As before, the change in slope is additive with additional zeros.

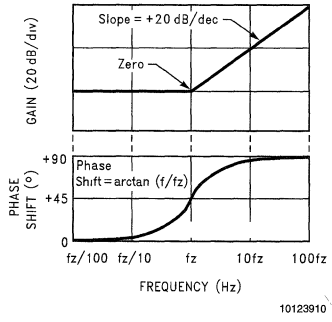


FIGURE 10. ZERO GAIN/PHASE PLOT

The phase shift introduced by a zero varies from 0 to +90°, with a +45° shift occurring at the frequency of the zero.

The most important thing to observe about a zero is that it is an **"anti-pole"**, which is to say its effects on gain and phase are exactly the opposite of a pole.

This is why zeros are intentionally added to the feedback loops of LDO regulators: they can cancel out of the effect of one of the poles that would cause instability if left uncompensated.

BODE PLOT ANALYSIS

A Bode plot which contains three poles and one zero (*Figure 11*) will be analyzed for gain and phase margin.

The DC gain is assumed to be 80 dB, with the first pole occurring at 100 Hz. At that frequency, the slope of the gain curve changes to −20 dB/decade.

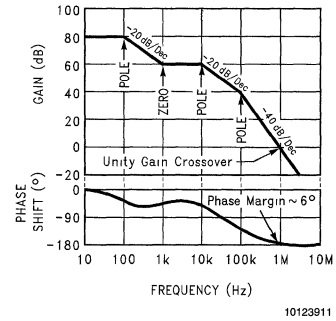


FIGURE 11. BODE PLOT WITH PHASE INFO

The zero at 1 kHz changes the slope back to 0 dB/decade until the second pole at 10 kHz, where the gain curve slope returns to −20 dB/decade.

The third and final pole at 100 kHz changes the gain slope to the final value of −40 dB/decade.

It can also be seen that the unity-gain (0 dB) crossover frequency is 1 MHz. The 0 dB frequency is sometimes referred to as the **loop bandwidth**.

The plot of the phase shift shows how the various poles and zeros contribute their effect on the feedback signal. To produce this plot, the phase shift at each frequency point was calculated based upon summing the contributions of every pole and zero at that frequency. The phase shift at any frequency "f" which is caused by a pole frequency located at frequency "f_p" can be calculated from:

$$\text{Pole Phase Shift} = -\arctan(f/f_p)$$

The phase shift resulting from a zero located at frequency "f_z" can be found using:

$$\text{Zero Phase Shift} = \arctan(f/f_z)$$

Is this loop stable? To answer that question, we need only the phase shift at 0 dB (which is 1 MHz in this case). Finding this does not require complex calculations:

As stated in the previous sections, a pole or zero contributes nearly its full phase shift in the frequency range one decade above and below the center frequency of the pole (or zero).

Feedback and Loop Stability

(Continued)

Therefore, the first two poles and the first zero contribute their full phase shifts of −180° to +90°, respectively, resulting in a net phase shift of −90°.

The final pole is exactly one decade below the 0 dB frequency. Using the formula for Pole Phase Shift, this pole will contribute −84° of phase shift @ 1 MHz. Added to the −90° from the two previous poles and the zero, the total phase shift is −174° (which means the phase margin is 6°). This loop would either oscillate or ring severely.

NPN Regulator Compensation

The pass transistor of the NPN regulator (see *Figure 1*) is connected in a circuit configuration known as **common collector**. An important characteristic of all common collector circuits is low output impedance, which means the pole from the power stage that it places in the loop gain occurs at a very high frequency.

The NPN regulator uses a technique called **dominant pole compensation** because it has no inherent low-frequency poles. In this case, a capacitor is built into the IC which places a pole in the loop gain at a low frequency (*Figure 12*).

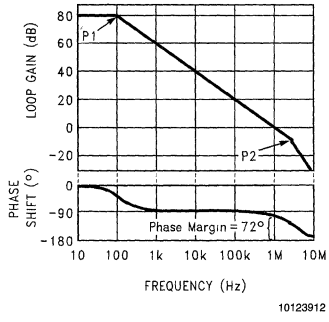


FIGURE 12. BODE PLOT FOR NPN REGULATOR

This **dominant pole** (shown as P1) for a typical NPN regulator is set at about 100 Hz. The 100 Hz pole causes the gain to decrease at a rate of −20 dB/decade until the second pole (P2) which is located at 3 MHz. At that point, the slope of the gain plot changes to −20 dB/decade.

The frequency of P2 is primarily due to the NPN power transistor and associated drive circuitry, so it is sometimes referred to as the **power pole**. Since P2 occurs at a frequency where the loop gain is −10 dB, its contribution to phase shift at the 0 dB frequency (1 MHz) will be small.

To determine stability, it only requires that the phase margin at the 0 dB frequency be calculated:

The first pole (P1) will contribute −90° of phase shift, but the second pole (P2) will add only −18° of negative phase shift @ 1 MHz (0 dB). This means the total phase shift @ 0 dB is −108°, which yields a phase margin of 72° (which is very stable).

It should also be noted that simple observation would clearly show this loop is stable, since reaching −180° of phase shift (the point of instability) would require the full contribution of −90° (each) from both poles, and P2 is too high in frequency to contribute significant phase shift at the 0 dB frequency (1 MHz).

LDO Regulator Compensation

The PNP transistor in an LDO regulator (*Figure 2*) is connected in a configuration called **common emitter**, which has a higher output impedance than the common collector configuration in the NPN regulator. This adds an additional low-frequency pole **whose frequency is dependent both on load resistance and output capacitance**. The frequency of this pole (which will be designated $\mathbf{P_L}$ for **load pole**) is found from:

$$f(P_L) = 1/(2\pi \times R_{LOAD} \times C_{OUT})$$

The presence of the frequency-variable load pole P_L means that the simple dominant pole compensation method used in the NPN regulator will not work in an LDO unless additional compensation is added. To illustrate why this is true, the loop gain of a 5V/50 mA LDO regulator will be illustrated using these assumptions:

At maximum load current, the load pole (P_L) occurs at a frequency given by:

$$P_L = 1/(2\pi \times R_{LOAD} \times C_{OUT}) = 1/(2\pi \times 100 \times 10^{-5}) = 160 \text{ Hz}$$

The internal compensation will be assumed to add a fixed pole (**P1**) at 1 kHz.

A 500 kHz power pole (which will be designated $\mathbf{P_{PWR}}$) is present due to the PNP power transistor and driver.

The DC gain is assumed to be 80 dB

$R_L = 100\Omega$ (which is the value at maximum load current)

$C_{OUT} = 10\ \mu F$.

Using the conditions stated above, a Bode plot (*Figure 13*) is drawn. It is immediately obvious that this loop is not stable: the two poles P_L and P1 will each contribute −90° of phase shift to reach −180° at the 0 dB frequency (which is about 40 kHz in this example).

To reduce the negative phase shift (and prevent oscillations), a zero must be added to the loop. A zero can contribute as much as +90° of positive phase shift, which will cancel out the effects of one of the two low frequency poles.

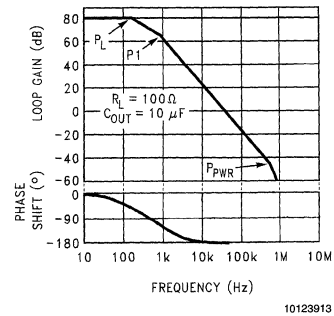


FIGURE 13. LDO GAIN PLOT WITHOUT COMPENSATION

LDO Regulator Compensation

(Continued)

Nearly all monolithic LDO regulators require that this zero be added to the loop, and they derive it from a characteristic that is inherent in the output capacitor: **equivalent series resistance** (usually referred to **ESR**).

LDO Compensation Using ESR

Equivalent series resistance (ESR) is a characteristic that is present in every capacitor. It can be modeled electrically as a resistance that is placed in series with the capacitor (*Figure 14*).

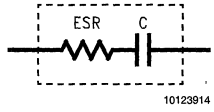


FIGURE 14. CAPACITOR SHOWING ESR

The ESR of the output capacitor puts a zero in the loop gain which can be used to reduce excess negative phase shift.

The frequency where the zero occurs is directly related to the value of the ESR and amount of output capacitance:

$$F_{ZERO} = 1/(2\pi \times C_{OUT} \times ESR)$$

Using the example in the previous section (Bode plot shown in *Figure 13*), we will assume that the value of C_{OUT} = 10 µF and the output capacitor ESR = 1Ω, which means a zero will occur at 16 kHz.

Figure 15 shows how this added zero will change the unstable plot into a stable one:

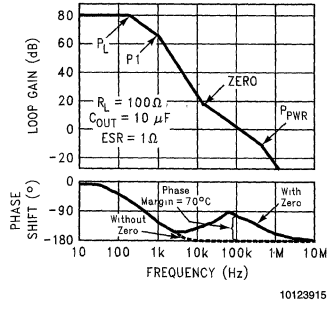


FIGURE 15. ESR ZERO STABILIZES LDO

The bandwidth of the loop is increased so that the 0 dB crossover frequency moves form 30 kHz to 100 kHz.

The zero adds a total of +81° positive phase shift at 100 kHz (the 0 dB frequency). This will reduce the negative phase shift caused by the poles P_L and P1.

Since the pole P_{PWR} is located at 500 kHz, it adds only −11° of phase shift at 100 kHz.

Summing all poles and zeros, the total phase shift at 0 dB is now −110°. This corresponds to a phase margin of +70°, which is extremely stable.

This illustrates how an output capacitor with the correct value of ESR can generate a zero that stabilizes an LDO.

ESR and Stability

Virtually all LDO regulators require that the ESR of the output capacitor be within a set range to assure regulator stability.

The LDO manufacturer provides a set of curves which define the boundaries of the stable region, plotted as a function of load current (*Figure 16*).

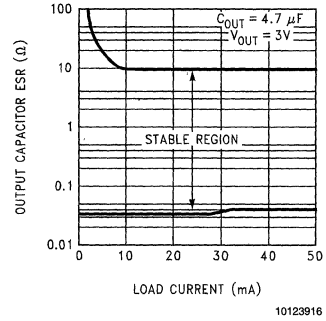


FIGURE 16. ESR RANGE FOR Typical LDO

To explain why these boundaries exist, the effects of low and high ESR on phase margin will be illustrated using the example previously developed.

HIGH ESR

Using the examples developed in the previous sections, we will change the conditions and assume the ESR of the 10 µF output capacitor is increased to 20Ω. This will decrease the frequency of the zero to 800 Hz (*Figure 17*). Reducing the frequency of the zero causes the loop bandwidth to increase, moving the 0 dB crossover frequency from 100 kHz to 2 MHz.

This increase bandwidth means that the pole P_{PWR} occurs at a gain value of +20 dB (compared to −10 dB in *Figure 14*).

Analyzing the plot (*Figure 17*) for phase margin, it can be assumed that the zero cancels out either P1 or P_L. This means the loop has a two-pole response with the low frequency pole contributing −90° of phase shift and the high frequency pole P_{PWR} contributing about −76° of phase shift.

ESR and Stability (Continued)

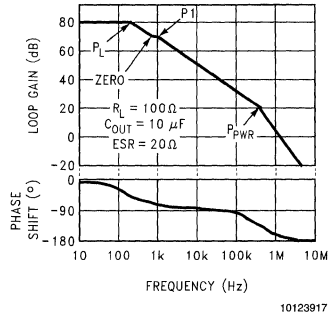


FIGURE 17. HIGH ESR CAUSES UNSTABLE LOOP

Although this appears to leave a phase margin of 14° (which **might** be stable), bench test data shows that ESR values > 10 Ω usually cause instability because of phase shifts contributed by other high-frequency poles which are not shown in this simplified model.

LOW ESR

An output capacitor with a very low ESR value can cause oscillations for a different reason.

Continuing the example developed in the previous section, we will now reduce the ESR of the 10 µF output capacitor to 50 mΩ, increasing the frequency of the zero to 320 kHz (*Figure 18*).

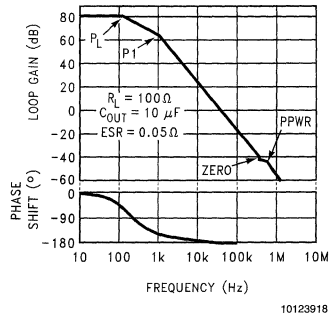


FIGURE 18. LOW ESR CAUSES UNSTABLE LOOP

When the plot is analyzed for phase margin, no calculations are required to see that it is unstable.

The −90° phase shift from each of the two poles P1 and P_L will produce a total phase shift of −180° at the 0 dB frequency.

For this system to be stable, a zero is needed that would provide positive phase shift before the 0 dB point. However, since the zero is at 320 kHz, it's too far out to do any good (and is cancelled out by P_{PWR}).

Output Capacitor Selection

Since the output capacitor is the user's tool for compensating a monolithic LDO regulator, it must be selected very carefully. Most cases of oscillations in LDO applications are caused by the ESR of the output capacitor being too high or too low.

When selecting an output capacitor for an LDO, a solid tantalum capacitor is usually the best choice (except for parts specifically designed for ceramic capacitors like the LP2985). Tests performed on an AVX 4.7 µF Tantalum showed an ESR of 1.3Ω @ 25°C, a value that is almost perfectly centered in the stable region (*Figure 16*).

Also very important, the ESR of the AVX capacitor varied less than 2:1 over the temperature range of −40°C to +125°C. Aluminium electrolytic capacitors are notorious for exhibiting an exponential increase in ESR at cold temperatures, and are not suitable for use as an LDO output capacitor.

It must be noted that large (≥ 1 µF) ceramic capacitors typically have very low ESR values (< 20 mΩ), and will cause most LDO regulators to oscillate if connected directly to the output (except the LP2985). A ceramic capacitor can be used if some external resistance is added in series with it to increase the effective ESR. Large value ceramics also have a poor tempco (typically Z5U) which means the capacitance will drop in half as the temperature is increased or decreased to the operating limits.

Quasi-LDO Compensation

When evaluating the quasi-LDO regulator (*Figure 3*) for stability and compensation, it has some of the electrical characteristics of both the LDO and NPN regulator. Since the quasi-LDO uses an NPN pass device, it is in the common-collector configuration which means it's output device node (emitter) looks like a relatively low impedance.

However, because of the base of the NPN is being driven from a high-impedance PNP current source, the regulator output impedance of a quasi-LDO is not as low as the NPN regulator with an NPN Darlington pass device (but is much lower than a true LDO which drives the regulator output off the collector of a PNP).

This means that the troublesome power pole of a quasi-LDO is at a lower frequency than the NPN regulator, so some compensation (output capacitance) is required to make a quasi-LDO stable. Of course, the pole is at a much higher frequency than the LDO, so the quasi-LDO requires less capacitance and the ESR is not as critical.

For example, the LM1085 quasi-LDO rated for 3A of load current requires only 10 µF of Tantalum output capacitance to assure complete stability over all line and load conditions. No ESR graphs are given, since the value of ESR is not critical as it is in an LDO.

Low-ESR Specific LDO's

National Semiconductor does have LDO regulators like the LP2985 and LP2989 which are specifically designed to work with extremely low ESR capacitors like surface-mount ce-

Low-ESR Specific LDO's (Continued)

ramics. This type of capacitor can have ESR values as low as 5-10 mΩ, which will cause most typical LDO regulators to oscillate (as demonstrated in *Figure 18*.

To make the LP2985 stable with such low ESR values, an internal zero is built in which takes the place of the ESR zero previously provided by the Tantalum output capacitor. The effect of this is to shift the stable ESR range downward. A typical LDO with no added internal zero might be stable ESR range from about 100 mΩ to 5 Ω (well suited for Tantalums but not ceramics). The stable range for the LP2985 extends down to 3 mΩ, and has an upper limit of about 500 mΩ so it can be used with ceramics.

The reason the upper limit is moved down can be understood by referring to *Figure 15*. As previously stated, the zero is now built into the LDO, so the ESR zero resulting from the output capacitor must stay at a high enough frequency that it does not cause the bandwidth to get too wide where high frequency poles would add enough phase shift to produce oscillations.

The FET Advantage

An LDO regulator can be built using a P-FET as the pass transistor (see *Figure 19*).

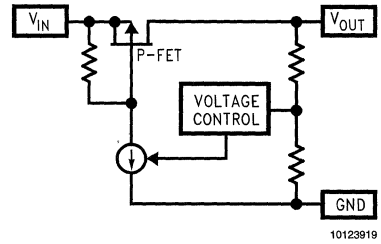


FIGURE 19. P-FET LDO REGULATOR

To see why using a P-FET LDO would be advantageous, it should be noted that all of the base current required by the power transistor in a PNP LDO (*Figure 2*) flows out of the ground pin and back to the negative input voltage return. Therefore, this base drive current is drawn from the input supply but does not drive the load, so it generates wasted power that must be dissipated within the LDO regulator:

$$\text{PWR (Base Drive)} = V_{IN} \times I_{BASE}$$

The amount of base current required to drive the PNP is equal to the load current divided by the beta (gain) of the PNP, and beta may be as low as 15 - 20 (at rated load current) in some PNP LDO regulators. The wasted power generated by this base drive current is very undesirable (especially in battery-powered applications). Using a P-FET solves this problem, since the Gate drive is very small.

Another advantage of the P-FET LDO is that the dropout voltage can be made very small by adjusting the ON-resistance of the FET. For monolithic regulators, FET power transistors typically will give a lower ON-resistance per unit area than bipolar ONP devices. This allows making higher current regulators in smaller packages.

LP2980, LP2981, LP2982, LP2985 Micro SMD Demo Boards

National Semiconductor
Application Note 1172
Chester Simpson

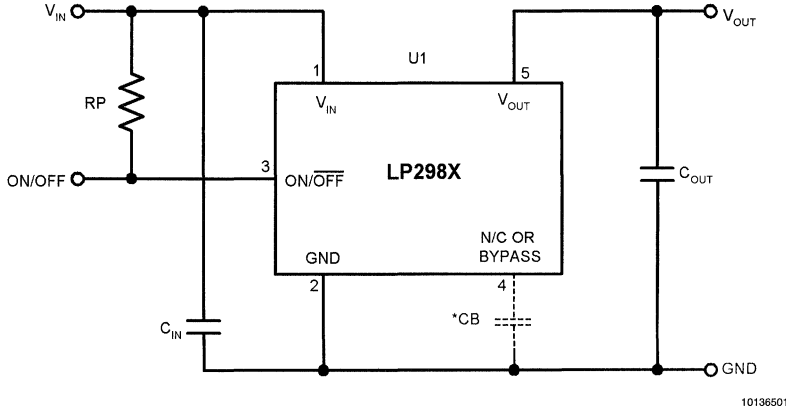
Abstract

This document describes the characteristics of the demo board designed for use with the micro SMD versions of National's LP298X low dropout regulators.

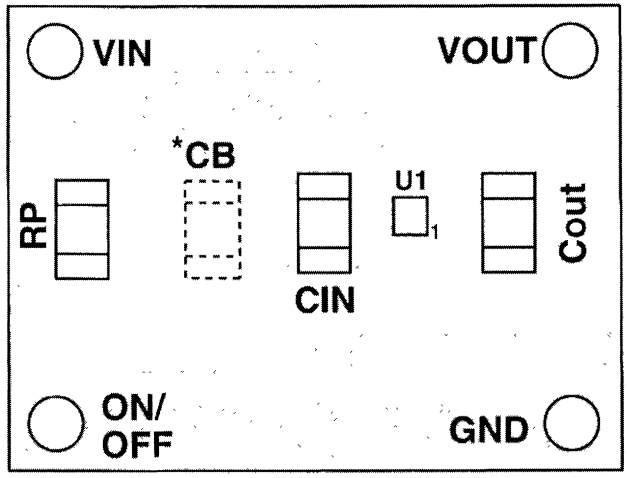
The components of each demo board vary by device type and voltage option. Lists of materials are provided which specify the correct external components to be used with each NSC part type.

It should be noted that the noise bypass capacitor is only used on the LP2982 and LP2985. Demo boards for other parts types will not have a component installed at this location.

Care must be taken so that the input voltage is not raised above 10V, since a 10V ceramic capacitor is called out for use at the C_{IN} location.



Schematic Diagram



*Used only On Low-Noise parts LP2982 and LP2985

Demo Board (Top View)

List of Materials

COMPONENTS COMMON TO ALL BOARD ASSEMBLIES

Quantity	Description	Ref Designator
1	LP298X Micro SMD PCB Etch 001	
1	Ceramic Cap, 1 µF, 10V X7R (1206)	C_{IN}
4	Terminal, Uninsulated 0.094" IPI Cambion P/N 160-1026-02-01-00	V_{IN}, V_{OUT}, GND, ON/OFF
1	Resistor, 10K, ⅛W %5 (1206)	RP

COMPONENTS WHICH VARY BY PART TYPE AND/OR VOLTAGE OPTION

LP2980-4.5 Through LP2980-5.0

Quantity	Description	Ref Designator
1	LP2980-X.X Micro SMD Device	U1
1	Tantalum Cap, 2.2 µF, 10V	C_{OUT}
1	Not Used	CB

LP2980-3.1 Through LP2980-4.4

Quantity	Description	Ref Designator
1	LP2980-X.X Micro SMD Device	U1
1	Tantalum Cap, 4.7 µF, 6V	C_{OUT}
1	Not Used	CB

LP2980-1.5 Through LP2980-3.0

Quantity	Description	Ref Designator
1	LP2980-X.X Micro SMD Device	U1
1	Tantalum Cap, 10 µF, 6V	C_{OUT}
1	Not Used	CB

LP2981-4.5 Through LP2981-5.0

Quantity	Description	Ref Designator
1	LP2981-X.X Micro SMD Device	U1
1	Tantalum Cap, 2.2 µF, 10V	C_{OUT}
1	Not Used	CB

LP2981-3.1 Through LP2981-4.4

Quantity	Description	Ref Designator
1	LP2981-X.X Micro SMD Device	U1
1	Tantalum Cap, 4.7 µF, 6V	C_{OUT}
1	Not Used	CB

LP2981-1.5 Through LP2981-3.0

Quantity	Description	Ref Designator
1	LP2981-X.X Micro SMD Device	U1
1	Tantalum Cap, 10 µF, 6V	C_{OUT}
1	Not Used	CB

LP2982-4.5 Through LP2982-5.0

Quantity	Description	Ref Designator
1	LP2982-X.X Micro SMD Device	U1

List of Materials (Continued)

LP2982-4.5 Through LP2982-5.0 (Continued)

Quantity	Description	Ref Designator
1	Tantalum Cap, 2.2 µF, 10V	C_{OUT}
1	Ceramic Cap, .01 µF, X7R or COG	CB

LP2982-3.1 Through LP2982-4.4

Quantity	Description	Ref Designator
1	LP2982-X.X Micro SMD Device	U1
1	Tantalum Cap, 4.7 µF, 6V	C_{OUT}
1	Ceramic Cap, .01 µF, X7R or COG	CB

LP2982-1.5 Through LP2982-3.0

Quantity	Description	Ref Designator
1	LP2982-X.X Micro SMD Device	U1
1	Tantalum Cap, 10 µF, 6V	C_{OUT}
1	Ceramic Cap, .01 µF, X7R or COG	CB

LP2985-4.5 Through LP2985-5.0

Quantity	Description	Ref Designator
1	LP2985-X.X Micro SMD Device	U1
1	Tantalum Cap, 2.2 µF, 10V	C_{OUT}
1	Ceramic Cap, .01 µF, X7R or COG	CB

LP2985-3.1 Through LP2985-4.4

Quantity	Description	Ref Designator
1	LP2985-X.X Micro SMD Device	U1
1	Tantalum Cap, 4.7 µF, 6V	C_{OUT}
1	Ceramic Cap, .01 µF, X7R or COG	CB

LP2985-1.5 Through LP2985-3.0

Quantity	Description	Ref Designator
1	LP2985-X.X Micro SMD Device	U1
1	Tantalum Cap, 10 µF, 6V	C_{OUT}
1	Ceramic Cap, .01 µF, X7R or COG	CB

LM3477 Evaluation Board

National Semiconductor
Application Note 1193
Mark Hartman

Introduction

The LM3477 is a current mode, high-side N channel FET controller. It is most commonly used in buck configurations, as shown in *Figure 1*. All the power conducting components of the circuit are external to the LM3477, so a large variety of inputs, outputs, and loads can be accommodated by the LM3477.

The LM3477 evaluation board comes ready to operate at the following conditions:

$4.5V \le V_{IN} \le 15V$

$V_{OUT} = 3.3V$

$0A \le I_{OUT} \le 1.6A$

The circuit and BOM for this application are given below:

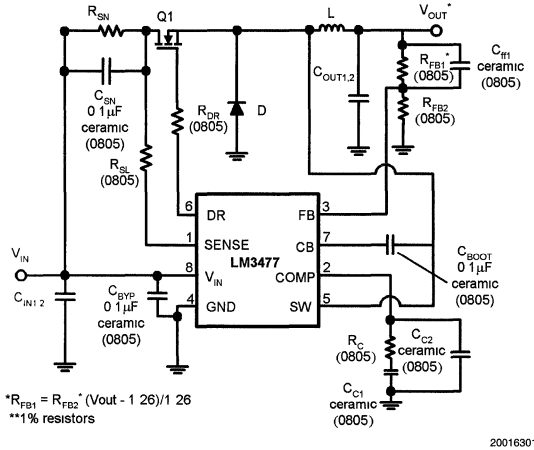


FIGURE 1. LM3477 Buck Converter

TABLE 1. Bill of Materials

Component	Value	Part Number
C_{IN1}	120µF/20V	594D127X0020R2
C_{IN2}	No connect	
C_{OUT1}	22µF/10V	LMK432BJ226MM (Taiyo Yuden)
C_{OUT2}	22µF/10V	LMK432BJ226MM (Taiyo Yuden)
L	10µH, 3.8A	DO3316P-103 (Coilcraft)
R_C	1.8kΩ	CRCW08051821FRT1 (Vitramon)
C_{C1}	12nF/50V	VJ0805Y123KXAAT (Vitramon)
C_{C2}	No connect	
Q1	5A, 30V	IRLMS2002 (IRF)
D	100V, 3A	MBRS340T3 (Motorola)
R_{DR}	20Ω	CRCW080520R0FRT1 (Vitramon)
R_{SL}	1kΩ	CRCW08051001FRT1 (Vitramon)
R_{FB1}	16.2kΩ	CRCW08051622FRT1 (Vitramon)
R_{FB2}	10.0kΩ	CRCW08051002FRT1 (Vitramon)
C_{FF}	470pF	VJ0805Y471KXAAT (Vitramony)
R_{SN}	0.03Ω	WSL 2512 0.03Ω ±1% (Dale)

Performance

Following are some benchmark data taken from the circuit above on the LM3477 evaluation board. This evaluation board may also be used to evaluate a buck regulator circuit optimized for a different operating point, or to evaluate a trade-off between cost and some performance parameter. For example, the conversion efficiency may be increased by using a lower $R_{DS(ON)}$ MOSFET, ripple voltage may be lowered with lower ESR output capacitors, and the hysteretic threshold may be changed as a function of the R_{SN} and R_{SL} resistors.

The conversion efficiency may be increased by using a lower $R_{DS(ON)}$ MOSFET, however it drops as input voltage increases. The efficiency reduces because of increased diode conduction time and increased switching losses. Switching losses are due to the Vds*Id transition losses and to the gate charge losses, both of which may be lowered by using a FET with low gate capacitance. At low duty cycles, where most of the power loss in the FET is from the switching losses, trading off higher $R_{DS(ON)}$ for lower gate capacitance will increase efficiency.

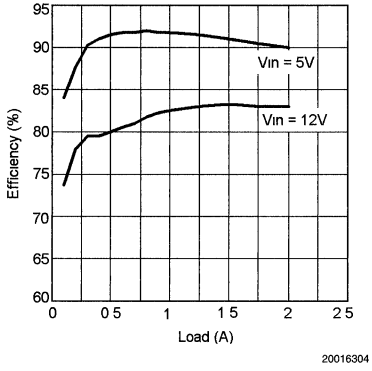


FIGURE 2. Efficiency vs Load
V_{OUT} = 3.3V

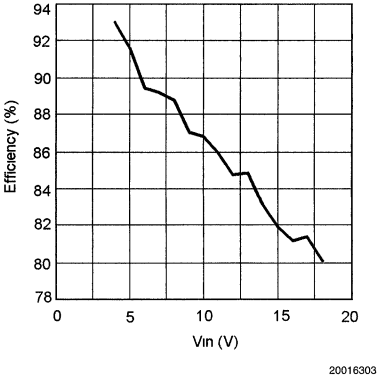
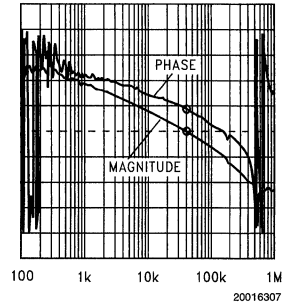


FIGURE 3. Efficiency vs V_{IN}
V_{OUT} = 3.3V, I_{OUT} = 2A

Given below is a bode plot of LM3477 open loop frequency response using the external components listed in *Table 1*.



Magnitude = 20 dB/Decade Bandwidth = 39.8kHz
Phase = 45°/Decade Phase Margin = 41°

FIGURE 4. Open Loop Frequency Response
V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1.5A

Hysteretic Mode

As the load current is decreased, the LM3477 will eventually enter a 'hysteretic' mode of operation. When the load current drops below the hysteretic mode threshold, the output voltage rises slightly. The over voltage protection (OVP) comparator senses this rise and causes the power MOSFET to shut off. As the load pulls current out of the output capacitor, the output voltage drops until it hits the low threshold of the OVP comparator and the part begins switching again. This behavior results in a lower frequency, higher peak-to-peak output voltage ripple than with the normal pulse width modulation scheme. The magnitude of the output voltage ripple is determined by the OVP threshold levels, which are referred to the feedback voltage and are typically 1.25V to 1.31V (see Electrical Characteristics table in the LM3477 datasheet). In the case of a 3.3V output, this translates to a regulated output voltage between 3.27V and 3.43V. The hysteretic mode threshold point is a function of R_{SN} and R_{SL}. *Figure 5* shows the Hysteretic Threshold vs. V_{IN} for the LM3477 evaluation board with and without R_{SL}.

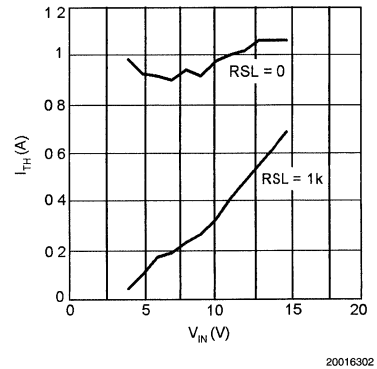


FIGURE 5. I_{TH} vs V_{IN}

Increasing Current Limit

The R_{SL} resistor offers flexibility in choosing the ramp of the slope compensation. Slope compensation affects the minimum inductance for stability (see the Slope Compensation section in the LM3477 datasheet), but also helps determine the current limit and hysteretic threshold. As an example, R_{SL} can be disconnected and replaced by a 0 ohm resistor so that no extra slope compensation is added to the current sense waveform to increase the current limit. A more conventional way to adjust the current limit is to change R_{SN}. R_{SL} is used here to change current limit for the sake of simplicity and to demonstrate the dependence of current limit to R_{SL}. By changing R_{SL} to 0 ohm, the following conditions may be met:

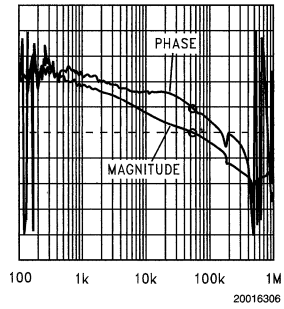
$4.5V \le V_{IN} \le 15V$

$V_{OUT} = 3.3V$

$0A \le I_{OUT} \le 3A$

The current limit is a weak function of slope compensation and a strong function of the sense resistor. By decreasing R_{SL}, slope compensation is decreased, and as a result the current limit increases. The hysteretic mode threshold will also increase to about 1A (see *Figure 5*).

Given below is a bode plot of LM3477 open loop frequency response using the modified (R_{SL} = 0Ω) components to achieve higher output current capability.



Magnitude = 20 dB/Decade Bandwidth = 55.3kHz

Phase = 45°/Decade Phase Margin = 42°

FIGURE 6. Open Loop Frequency Response
V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 3A

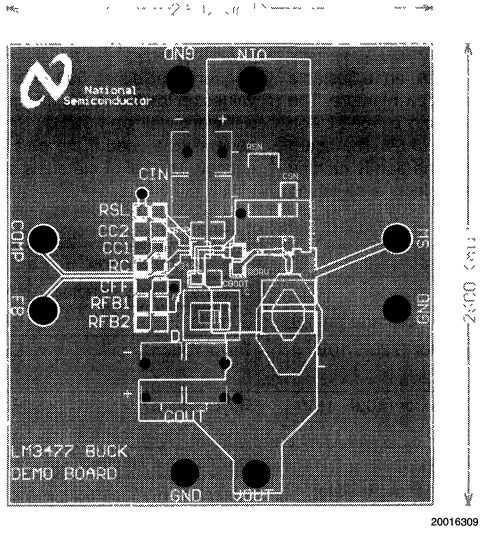
Layout Fundamentals

Good layout for DC-DC converters can be implemented by following a few simple design guidelines:

1 Place the power components (catch diode, inductor, and filter capacitors) close together. Make the traces between them short.

2. Use wide traces between the power components and for power connections to the DC-DC converter circuit.
3. Connect the ground pins of the input and output filter capacitors and catch diode as close as possible using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground-plane with several vias.
4. Arrange the power components so that the switching current loops curl in the same direction.
5. Route high-frequency power and ground return as direct continuous parallel paths.
6. Separate noise sensitive traces, such as the voltage feedback path, from noisy traces associated with the power components.
7. Ensure a good low-impedance ground for the converter IC.
8. Place the supporting components for the converter IC, such as compensation, frequency selection and charge-pump components, as close to the converter IC as possible but away from noisy traces and the power components. Make their connections to the Converter IC and it's pseudo-ground plane as short as possible.
9. Place noise sensitive circuitry, such as radio-modem IF blocks, away from the DC-DC converter, CMOS digital blocks, and other noisy circuitry.

Layout Fundamentals (Continued)



20016309

FIGURE 7. LM3477 Evaluation Board PCB Layout (Top Side)

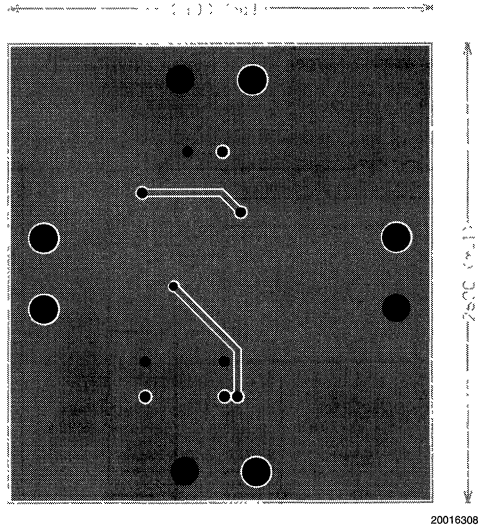


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FIGURE 8. LM3477 Evaluation Board PCB Layout (Bottom Side)

LM2622 Step-Up DC/DC Converter Evaluation Board

National Semiconductor
Application Note 1198
Clinton Jensen

The LM2622 is a step-up converter with an adjustable switching frequency and a low power shutdown feature. The evaluation board was designed for boosting a I-cell Li-Ion battery input volatge to a regulated output of 5V. The board includes 2 jumpers: One selects whether the part is running or is in shutdown mode, and the other selects a switching frequency of either 600 kHz or 1.3 MHz. The component values on the board are designed for 600 kHz operation, but will work well at 1.3MHz. Smaller component values can generally be used if the part is operated at the higher frequency. The bill of materials and the schematic follows:

TABLE 1. Bill of Materials

Designator	Description	Manufacturer	Model Number
U1	Step-Up Regulator	National Semiconductor	LM2622
L1	Inductor (1.2A average rating)	Sumida	CRDH5D18-100NC
C_{IN2}	Input Capacitor (22µF, 10V rating)	Taiyo-Yuden	LMK432BJ226K
C_{OUT1}	Output Capacitor (10µF, 16V rating)	Taiyo-Yuden	EMK325BJ106K
D1	Output Diode	International Rectifier	15MQ040N
R_{FB1}	20.5 kΩ Feedback Resistor		
R_{FB2}	6.98 kΩ Feedback Resistor		
R_C	20 kΩ Compensation Resistor		
C_C	1 nF Compensation Resistor		

Because of the capacitor ratings, the input to the board should always be 10V or less and the output should not be set to higher than 16V. Higher voltages (to the IC limits) may be used if higher voltage capacitors are used. A larger inductor may also be required if the input current is expected to exceed 1.2A, or if output short circuit conditions are anticipated.

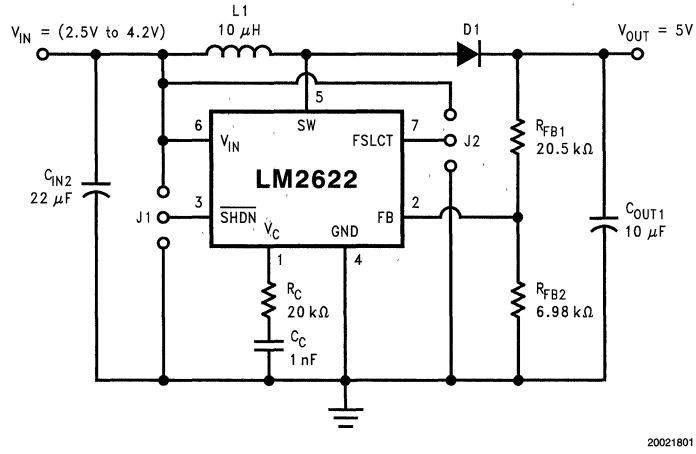

FIGURE 1.

LM2698 Demoboard

National Semiconductor
Application Note 1202
Mark Hartman

Introduction

A printed circuit board has been developed to aid in the design and evaluation of the LM2698 DC-DC boost converter. This application note contains information about the board.

General Description

The LM2698 is a general purpose, high frequency DC-DC converter. This board is intended to demonstrate the primary advantages of the LM2698. The LM2698 is able to operate at 1.25MHz switching frequency, yielding extremely high power density. The low $R_{DS(ON)}$ internal MOSFET allows for high conversion efficiency. It uses a current mode control scheme, giving superior line and load regulation. The LM2698 is a Simple Switcher®, which includes Switchers Made Simple software for fast, effective designs.

The LM2698 demoboard will operate with the following parameters:

$4.5V \le V_{IN} \le 9V$

$V_{OUT} = 12V$

$0 \le I_{OUT} \le 400mA$*

Note: * See *Figure 2* for I_{OUT} vs V_{IN}

Note 1: The inductance affects the stability of the converter See the COMPENSATION section in the datasheet for tips on optimizing the inductance value, especially for input voltages less than 5V To operate this demoboard at voltages below 4 5V with the supplied 10µH inductor and remain in a safe stability region, use a 1 25 MHz switching frequency (if V_{IN} > 5V, a 600 kHz or 1 25 MHz switching frequency is acceptable)

Note 2: When operating the LM2698 at 1 25 MHz switching frequency, it is recommended to increase the bypass capacitance, C_{BYP}, to 0 220 µF

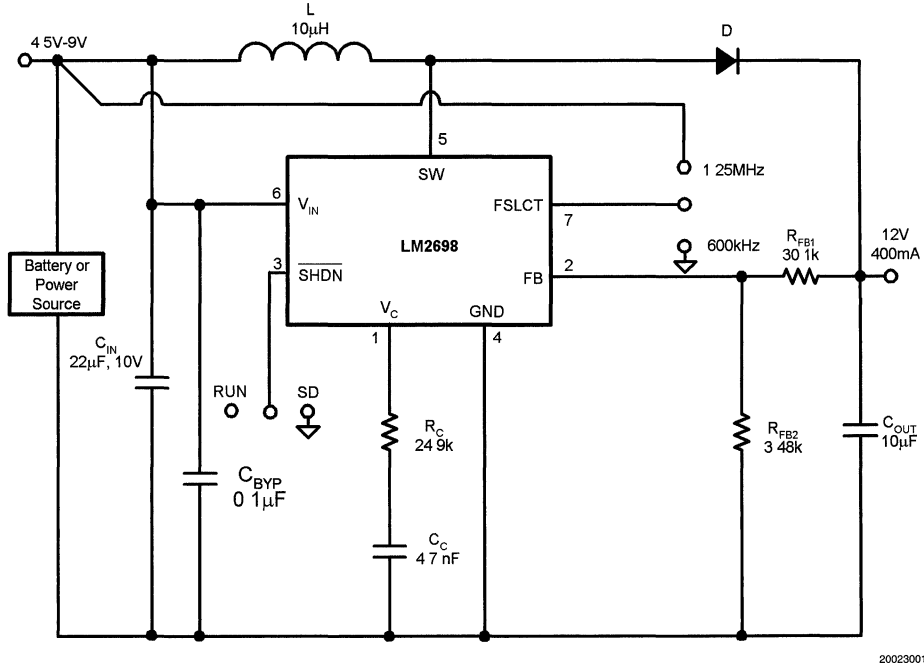

FIGURE 1. LM2698 Demoboard Schematic

TABLE 1. Bill of Materials

Component	Value	Description	Model Number
C_{OUT}	10µF	Output Capacitor	TMK432BJ106MM (Taiyo Yuden)
C_{IN}	22µF	Input Capacitor	LMK432BJ226MM (Taiyo Yuden)
C_C	4.7nF	Compensation Capacitor	VJ0805Y472MXAAT (Vishay)
C_{BYP}	0.1µF	Bypass Capacitor	VJ0805Y104KXAAT (Vishay)
D	1A, 20V	Schottky Power Diode	MBRM120LT3 (ON-Semiconductor)
L	10µH	Power Inductor	CDRH6D38-100 (Sumida)
R_C	24.9k	Compensation Resistor	CRCW 0805 2492 FRT1 (Vishay)
R_{FB1}	30.1k	Top Feedback Resistor	CRCW 0805 3012 FRT1 (Vishay)
R_{FB2}	3.48k	Bottom Feedback Resistor	CRCW 0805 3481 FRT1 (Vishay)

TABLE 2. Jumper Settings

Jumper	Setting	Description
J1	600 kHz	600 kHz switching frequency
	1.25 MHz	1.25 MHz switching frequency
J2	Run	LM2698 is regulating
	SD	LM2698 is shutdown

Maximum Output Current

The current limit of the LM2698 is with respect to the switch current. This means that the maximum output current to the load is dependent on duty cycle. With a fixed V_{OUT}, the maximum output current will be a function of V_{IN}, as shown in *Figure 2*.

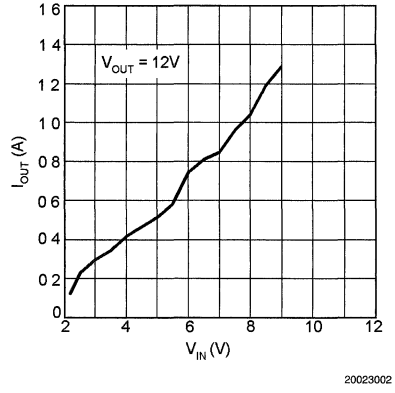

FIGURE 2. Maximum Output Current vs Input Voltage

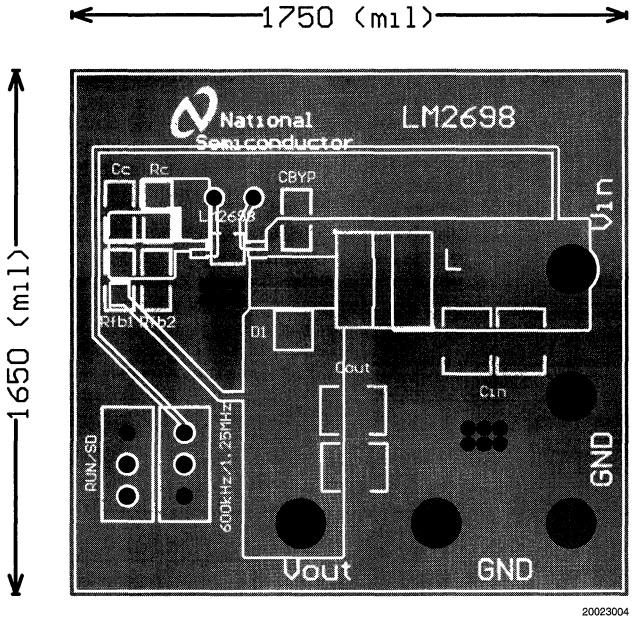

FIGURE 3. LM2698 Demoboard Top Layer Layout

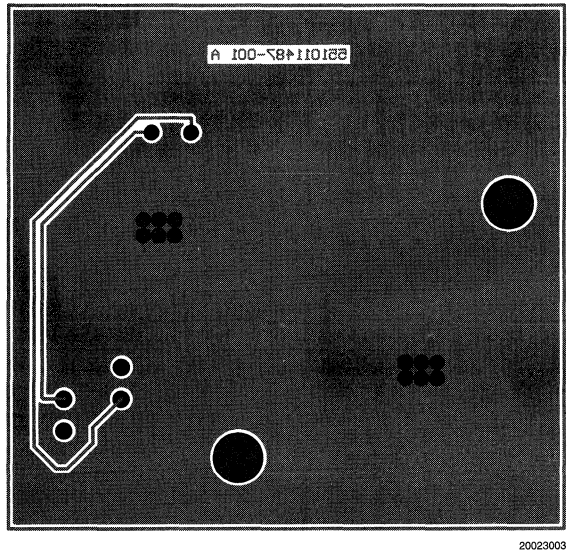

FIGURE 4. LM2698 Demoboard Bottom Layer Layout

LM2611 Demoboard

National Semiconductor
Application Note 1203
Mark Hartman

Introduction

The LM2611 demoboard is a working demonstration of a typical LM2611 Cuk converter layout. This application note contains information about the board. See the datasheet for more information on the LM2611 and Cuk topology.

General Description

The LM2611 is typically used in inverting Cuk converter applications. The Cuk converter offers the advantages of low input and output ripple current and the ability to step up or step down the magnitude of the input voltage. The NFB pin allows for simple feedback of the negative output voltage. The demoboard is assembled to show a small yet practical layout. The board will operate under the following conditions:

$4.5V \leq V_{IN} \leq 5.5V$

$V_{OUT} = -5V$

$0 \leq I_{OUT} \leq 300mA$

Note: The input capacitor is rated for 6.3V. Do not apply greater than 5.5V without first replacing the input capacitor with one of higher voltage rating ($V_{IN(MAX)}$ = 14V). The input voltage may be as low as 2.7V, however the maximum load will be lower than 300 mA.

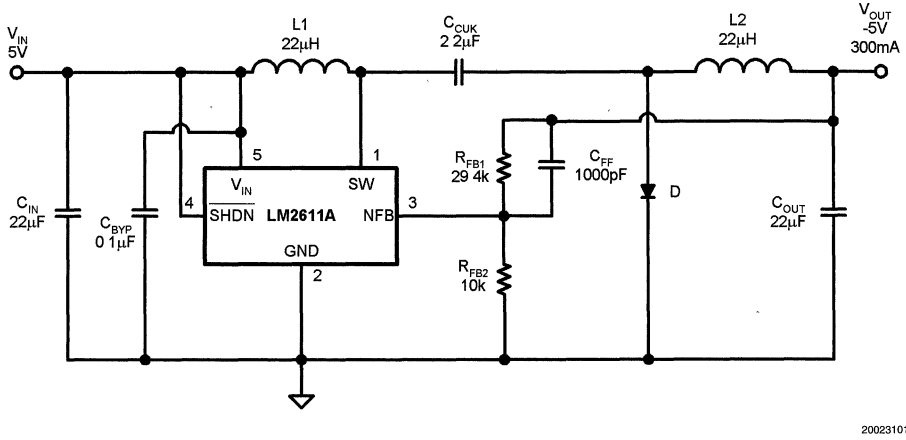

FIGURE 1.

TABLE 1. Bill of Materials

Component	Value	Description	Model Number
C_{BYP}	0.1µF	Bypass Capacitor	VJ0805Y104KXAAT (Vishay)
C_{CUK}	2.2µF	Cuk Capacitor	EMK316BJ225ML (Taiyo Yuden)
C_{FF}	1nF	Feedforward Capacitor	VJ0805Y102KXAAT (Vishay)
C_{IN}	22µF/6.3V	Input Capacitor	LMK325BJ226MM (Taiyo Yuden)
C_{OUT}	22µF/6.3V	Output Capacitor	LMK325BJ226MM (Taiyo Yuden)
D		Scottky Diode	MBRM120LT3 (Motorola)
L_1	22µH	Input Inductor	CR32-220 (Sumida)
L_2	22µH	Output Inductor	CR32-220 (Sumida)
R_{FB1}	29.4kΩ	Feedback Resistor	CRCW08052492FRT1 (Vishay)
R_{FB2}	10.0kΩ	Feedback Resistor	CRCW08051002FRT1 (Vishay)

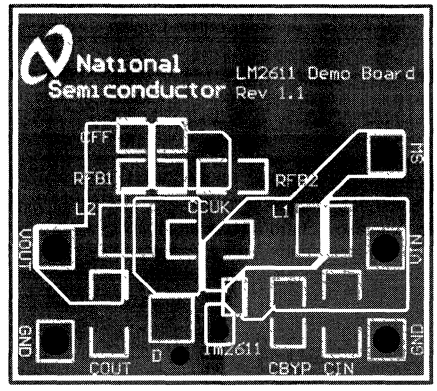

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FIGURE 2. LM2611 Demoboard Top Layer Layout

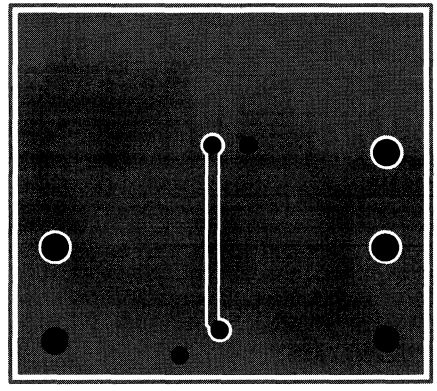

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FIGURE 3. LM2611 Demoboard Bottom Layer Layout

LM3478/LM3488 Evaluation Board

National Semiconductor
Application Note 1204
Chance Dunlap

Introduction

The LM3478 and LM3488 are current mode, low side N channel FET controllers. They can utilized in numerous configurations including a Boost, Flyback or SEPIC (Single Ended Primary Inductor Converter). This evaluation board demonstrates the flexibility of the LM3478 in a boost topology. The operating conditions for the evaluation board are listed below:

$4.5V \leq V_{IN} \leq 5.5V$

$V_{OUT} = 12V$

$0A \leq I_{OUT} \leq 1.5A$

The circuit and bill of materials for this design are given below:

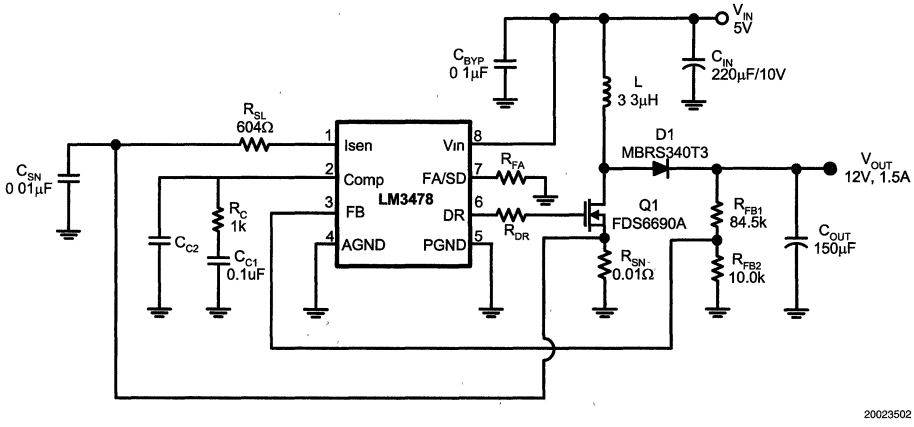


FIGURE 1. Circuit Diagram

TABLE 1. Bill of Materials

Component	Value	Model Number
U1		LM3478
L1	3.3µH	DO3316P-332 (Coilcraft)
Q1	30V/11A	FDS6690A (Fairchild)
D1	100V/3A	MBRS340T3 (Motorola)
C_{IN}	Tantalum, 220µF/10V	595D227X9010R2 (Sprague)
C_{OUT}	Tantalum, 150µF/16V	595D157X9016R2 (Sprague)
C_{OUT1}	No Connect	
C_{C1}	0.1µF/25V	VJ0805Y104KXXA (Vitramon)
C_{C2}	No Connect	
C_{BYP}	0.1µF/25V	VJ0805Y104KXXA (Vitramon)
C_{SEN}	0.01µF/25V	VJ0805Y103KXXA (Vitramon)
R_{FB1}	84.5kΩ	CRCW08058452 (Vitramon)
R_{FB2}	10kΩ	CRCW08051002 (Vitramon)
R_C	1kΩ	CRCW08051001 (Vitramon)
R_{SEN}	0.010Ω	(Dale, 1%, 1W, R01F, 2512)
R_{DR}	0Ω	CRCW0805600R0 (Vitramon)
R_{S1}	604Ω	CRCW08056040 (Vitramon)
R_{FA}	40.2kΩ	CRCW08054022 (Vitramon)

Performance

Benchmark data has been taken from the evaluation board using the LM3478. *Figure 2* shows an efficiency measurement taken at the maximum load of 1.5A with Vin at 5V.

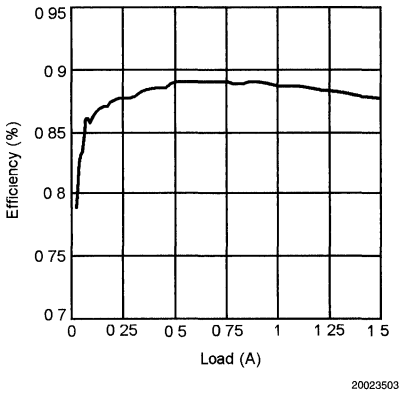


FIGURE 2. Efficiency vs Load

The open loop frequency response was also measured using the evaluation board as specified in the bill of materials. The bode plot can be seen below in *Figure 3*.

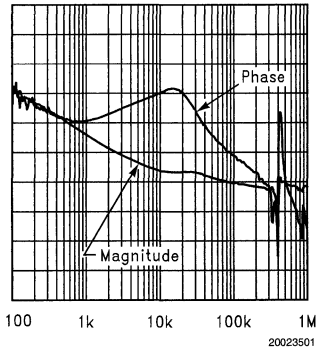


FIGURE 3. Frequency Response

The advantage of the evaluation board is the ability to examine performance tradeoffs through substitution of parts. By careful selection of the components used, it is possible to optimize the application circuit for a given parameter. For instance, the FET footprint has been designed to accommodate either a SO-8 or SOT23-6 package. The selection of FET would then be determined by the design constraints. An example would be that a lower system cost could be obtained by selection of a FET with a higher $R_{DS(ON)}$, although performance would be sacrificed through reduced efficiency.

Current Limit

The purpose of the R_{SL} resistor is to provide flexibility in the selection of the slope compensation needed for the required application. The amount of slope compensation directly determines the minimum inductance required for stability. (Please see the LM3478 or LM3488 datasheet for adjustment of slope compensation). In addition to slope compensation R_{SL} also provides assistance in the adjustment of current limit. Current limit is usually solely determined by the value of the sense resistor Rsn. But in the LM3478 and LM3488 an increase in R_{SL} causes the current limit to decrease by a slight amount. This can be advantageous in several situations. Common sense resistor values are typically separated by large intervals, making the task of accurately setting the current limit in any application difficult. As a result current limit is often ignored during the design phase, which can cause the application to suffer. An excessively high current limit can result in startup problems if the cycle-by-cycle current limit does not engage, limiting the effect of the soft start feature Or worse, current limit could be set to low causing the output voltage to drop at the maximum load. This is where the R_{SL} resistor can be used to avoid these issues. By selecting a common value sense resistor, current limit can be accurately set by calculating the R_{SL} size needed. This eliminates the need to choose custom sense resistors that can be cost prohibitive and cause production issues because of the difficulty in obtaining an adequate supply. For a complete discussion on how to calculate the R_{SL} value needed, refer to the current limit section in the LM3478 or LM3488 datasheet.

Layout Fundamentals

Good layout for DC-DC converters can be implemented by following a few simple design guidelines:

1. Place the power components (catch diode, inductor, and filter capacitors) close together. Make the traces between them as short and wide as possible.
2. Use wide traces between the power components and for power connections to the DC-DC converter circuit.
3. Connect the ground pins of the input and output filter capacitors and catch diode as close as possible using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground plane through several vias.
4. Arrange the power components so that the switching loops curl in the same direction.
5. Separate noise sensitive traces, such as the voltage feedback path, from noisy traces associated with the power components.
6. Ensure a good low-impedance ground for the converter IC.
7. Place the supporting components for the converter IC, such as compensation and frequency selection components as close to the converter IC as possible, but away from noisy traces and the power components. Make their connections to the converter IC and its pseudo-ground plane as short as possible.
8. Place noise sensitive circuitry such as radio or modem blocks away from the DC-DC converter.

Layout Fundamentals (Continued)

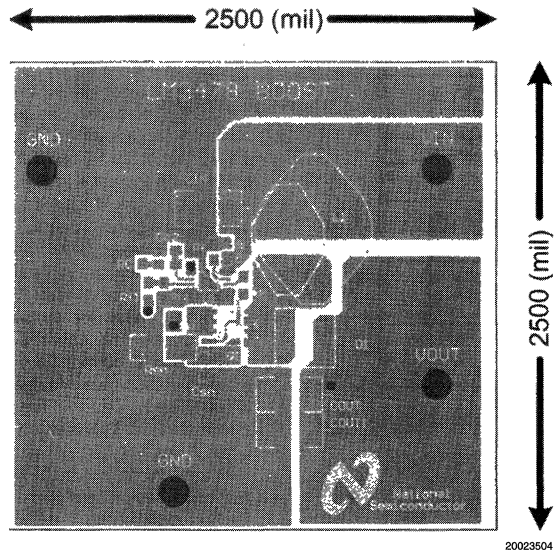


FIGURE 4. Front Side

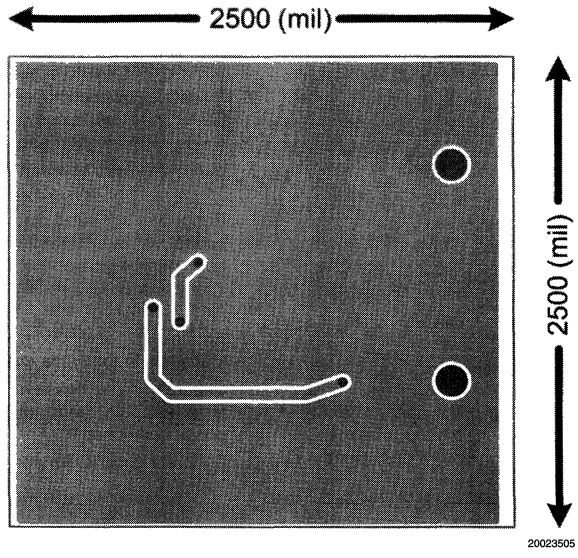


FIGURE 5. Back Side

LM2593HV Evaluation Board

National Semiconductor
Application Note 1207
Sanjaya Maniktala

Specifications of the Board

The board is designed for a nominal DC input of 48V, but can safely withstand up to 60V. The regulated DC output is 12V at a maximum load current of 2A. It uses the Adjustable Version of the LM2593HV in 7 lead Surface Mount Package (TO263). Relying on careful layout, it eliminates the need for a snubber across the diode and uses a minimum number of components. It has shutdown capability and error flag output available on the board It incorporates soft-start and delayed output error signaling and has an overall efficiency higher than 85%.

The board uses no external heatsinks, or through-hole parts and is therefore suitable for a fully automatic production process. It requires only 1.7 x 2.0 x 0.7 cu. inches of space. The printed circuit board is standard 1.6 mm thick (62 mils) '½ oz' double-sided FR4 laminate, with additional cooper plating, totaling a little over 1 oz of copper ("1 oz" is 1.4 mils/35 µm thick). The traces have been left unmasked to allow solder to deposit on the traces during reflow, so as to aid thermal dissipation. The converter is designed for continuous operation at rated load under natural convection up to a maximum ambient of 40˚C.

Component Selection

We set

V_{IN} = 48V

V_O = 12V

I_O = 2A

INDUCTOR

We define 'D' as the Duty Cycle and 'r' the ripple current ratio $\Delta I/I_O$. See Application Note AN-1197 for more details on the terms and equations used here.

We choose r to be 0.3 here as per the design procedure inductor nomographs in the LM2593HV datasheet as well as the guidelines in the referenced Application Note. 'r' is related to the inductance through the equation

$$r = \frac{Et}{L \cdot I_{DC}}$$

where 'Et' is the applied Voltµsecs, I_{DC} is the maximum rated load in Amps, and L is the inductance in µH.

The Duty Cycle is

$$D = \frac{V_O + V_D}{V_{IN} - V_{SW} + V_D}$$

where V_D is the diode forward voltage drop (≅0.5V), and V_{SW} is the drop across the switch when it is ON, plus any parasitics (≅1.5V). So

$$D = \frac{12 + 0.5}{48 - 1.5 + 0.5} = 0.27$$

The switch ON-time is

$$t_{ON} = \frac{D}{f} = \frac{(12 + 0.5) \times 10^6}{(48 - 1.5 + 0.5) \times 150000}\ \mu\text{secs}$$

t_{ON} = 1.77 µs

So the Voltµseconds 'Et' is

Et = $(V_{IN} - V_{SW} - V_O) \times t_{ON}$ = (48–1.5–12) x 1.77 Vµs

Et = 61.1 Vµs

Estimated inductance is therefore

$$L = \frac{Et}{r \times I_O}\ \mu H$$

$$L = \frac{61.1}{0.3 \times 2.0}\ \mu H$$

L = 101.8 µH

The first pass selection of the inductor is usually on the basis of the inductance calculated above and the max load current. But if the Input Voltage exceeds 40V, as it does here, we need to evaluate the inductor further to ensure that the converter withstands damage if the outputs are overloaded/shorted. Here we have chosen a 100 µH/1.8A drum core type (large inherent air gap) from Coilcraft, which saturates above 3A. It is designed for a 40˚C rise in temperature at a maximum ambient of 85˚C. We have accepted its use at a load current slightly higher than its continuous rating since the maximum ambient temperature for the demo-board is only 40˚C not 85˚C, and since we also know it does not saturate at the maximum load current.

INPUT CAPACITOR

The Voltage rating of the input capacitor must be higher than the DC Input. Tantalum capacitors were not considered suitable here due to their 50V maximum rating, and their inherent surge current limitations (which are always of concern especially at high input voltages). We have chosen a 63V aluminum electrolytic SMT capacitor from Panasonic, sized to handle the RMS current as calculated below:

$$I_{RMS\_IN} = I_O \cdot \sqrt{D \cdot \left[1 - D + \frac{r^2}{12}\right]}\ A$$

$$I_{RMS\_IN} = 2 \cdot \sqrt{0.27 \cdot \left[1 - 0.27 + \frac{0.3^2}{12}\right]} = 0.89\ A$$

The capacitor we chose is 100 µF with an RMS current rating of 1.02A at 100 kHz.

9

Component Selection (Continued)

OUTPUT CAPACITOR

We have chosen a capacitor type similar to the input capacitor mainly for logistic reasons. It was initially sized simply to handle the RMS current as calculated below, and with a voltage rating just higher than the output voltage. Subsequently, a Bode plot for the feedback loop confirmed that the phase margin was acceptable at around 40°. This validated the initial selection. The required RMS rating of the output capacitor is:

$$I_{RMS\_OUT} = I_O \cdot \frac{r}{\sqrt{12}} A$$

$$I_{RMS\_OUT} = 2 \cdot \frac{0.3}{\sqrt{12}} = 0.17 A$$

The capacitor we chose is 47 µF/16V with an RMS current rating of 0.24A at 100 kHz and an ESR of 0.36Ω.

CATCH DIODE

The Voltage rating must be higher than the input voltage. We have picked a 60V Schottky diode here. The average current in the catch diode is

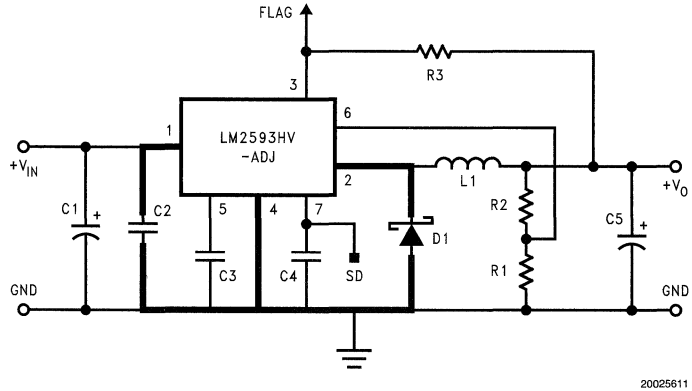
$I_{AVG\_D} = I_O \cdot (1-D)$

$I_{AVG\_D} = 2 \cdot (1-0.27) = 1.47A$

Usually the average current would be a starting point for the diode selection. But 60V Schottky diodes have a higher forward voltage drop than low voltage Schottkys, unless they are 'over-sized' in terms of their current rating. So to force good efficiency, we wanted to consider a diode with a 'hot-drop' (the forward drop with the diode hot) of no greater than 0.5V (at an instantaneous forward current of about 2A). This meant using a 3A/60V Schottky diode from International Rectifier.

Schematic

The board schematic is presented in *Figure 1*. The key layout suggestions are also indicated on the schematic. Shutdown capacity is available and the pinout marked 'SD' on the board can be taken low to cause the output of the converter to fall to 0V. The 'Flag' pin output is also available and it goes high (pulled up by R3 to the 12V rail) to indicate that the output is well-regulated. When the output is 'not OK', this pin is pulled down internally by the IC and in this condition it sinks 12V/21K=0.6 mA. The maximum voltage on the Flag pin should not exceed 45V and the current into it should not be higher than 3 mA. Therefore in our case it cannot be connected directly to the input voltage rail. The resistors R1 and R2 from a simple voltage divider designed to give 1.23V at the feedback pin when the output is at 12V.



Layout Suggestions

a) Traces shown in BOLD need to be short (not wide) as they pass high frequency current pulses Wide copper planes with switching current/voltage can radiate excessively

b) Trace to Feedback Pin (Pin 6) should not pass directly under L1 (to avoid pickup)

FIGURE 1.

Layout and Bill of Material

The two sides of the board are presented in *Figures 2, 3.* The Bill of Material is presented in *Table 1.*

TABLE 1. Bill of Material

Designator	Description	Manufacturer	Part Number	Quantity
U1	LM2593HVS-ADJ	National Semiconductor	LM2593HVS-ADJ	1
D1	3A/60V Schottky	International Rectifier	MBRS360TR	1
L1	100 µH/1.8A	Coilcraft	DO5022-104	1
C1	100 µF/63V	Panasonic	EEVFC1J101Q	1
C2, C3, C4	0.1 µF/100V	Vishay-Vitramon	VJ1206Y104KXBA	3
C5	47 µF/16V	Panasonic	EEVFK1C470P	1
R1	2.37K/1%	Vishay	CRCW12062371F	1
R2, R3	21K/1%	Vishay	CRCW12062102F	2

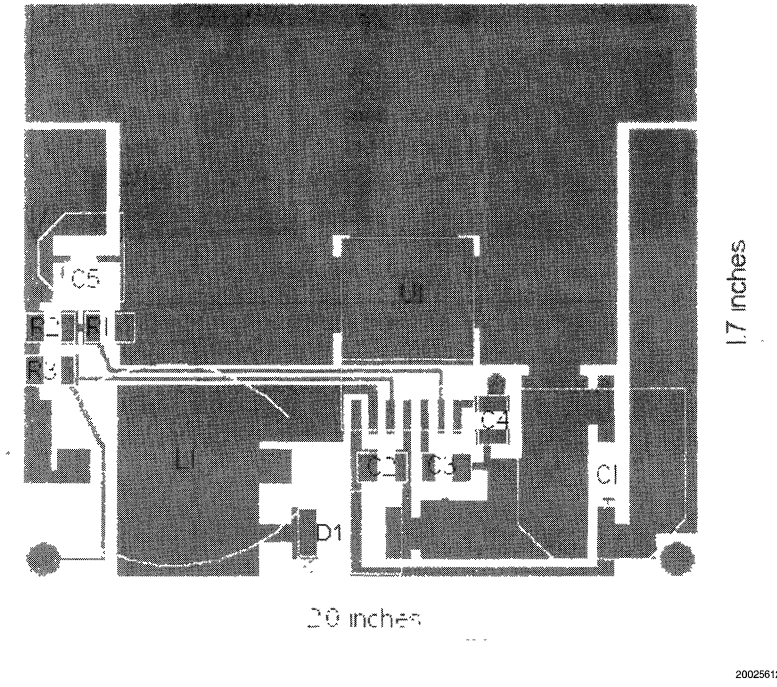


FIGURE 2. Top Side (Component Side) of PCB

Layout and Bill of Material (Continued)

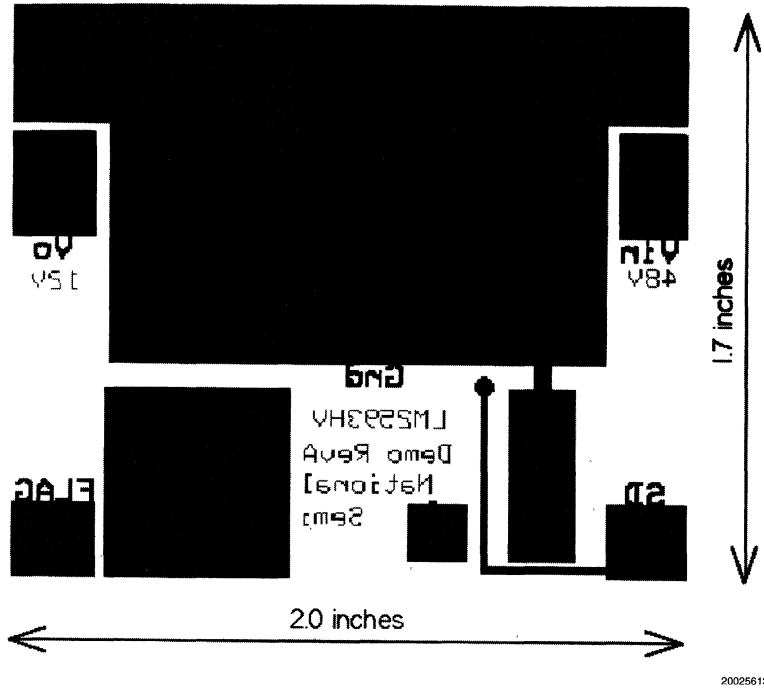


FIGURE 3. Bottom Side of PCB Viewed from Top

LM2633 Evaluation Board

National Semiconductor
Application Note 1208

Notes

1. When a DIP switch slide is ON, the signal whose label appears beside that slide is grounded;
2. Much flexibility is built into the board. For example, it is possible to use a dual SO-8 FET in Ch2, it is possible to use leaded capacitors at the switching outputs, and VDDX voltage (5V) can be supplied externally, etc.

Specifications

Input Voltage: 5V to 24V (don't go above 24V because input capacitors are rated for 25V only);

Continuous Load Current:

Ch1 = 16A;

Ch2 = 5A;

Ch3 = 300 mA;

Output Voltage:

Ch1 = DAC-Programmable (0.9V ~ 2.0V);

Ch2 = 1.5V;

Ch3 = 2.5V;

Minimum Steady-State Duty Cycle:

8% (steady-state duty cycle lower than this may cause sub-harmonic oscillations)

DIP Switch-Changeable Settings:

VID0 to VID4 logic levels;

ON/SS1 and ON/SS2 pins (either grounded or connected to a capacitor);

FPWM pin (either grounded or pulled up to 5V);

UV_Delay pin (either grounded or connected to a capacitor).

Troubleshooting Guide

1. Board wouldn't start;

   Try one or all of the following:

   A. Check the DIP switch (S1) setting and make sure ON1 and ON2 are not grounded at the same time;

   B. Check the current limit setting on the input power supply and make sure it is more than 2A during start up;

   C. Disconnect all loads;

   D. Make sure input voltage is between 5V and 24V.
2. Power Good flag does not go high;

   A. Make sure the 3.3V is connected;

   B. If a scope probe is used to measure the voltage, make sure the scope is not set to 50Ω termination impedance;

   C. Make sure all three channels are presenting the correct voltage.
3. Under-Voltage Shutdown does not activate;

   A. Make sure the UVD bit is not grounded at the DIP switch;

   B. Channel 3 will recover after the fault condition disappears.
4. The board shuts down after a VID bit is toggled on the DIP switch;

   Do not change the Ch1 voltage setting on the fly using the DIP switch. Instead, set the corresponding DIP VID bits to float, and then use a signal generator to toggle the corresponding VID terminal(s).
5. Output voltage is too noisy;

   If you see large voltage spikes in the output voltage waveform, with a 2 µs/div time base, it is most probably noise picked up by your probe. You can greatly reduce the sensitivity of your probe to the radiated noise by shortening its ground lead.

Using an External 5V to Supply the FET Drivers

Using the internal VLIN5 to power the VDDX pins has an efficiency penalty at light loads, especially when the input voltage is high. If there happens to be an external 5V available, it may make sense to use the external one. However, there may be a timing issue. Namely, if the external 5V comes up too late so that at the end of the soft start process the output voltages are still too low, then UVP will activate and cause the system to shut down. To work around this potential issue, it is recommended to DIODE OR the two 5V rails. Of course, the external 5V needs to be slightly higher than VLIN5 so that the latter will not be supplying VDDX current. To do this, remove R16 on the evaluation board, and connect the external 5V to terminal "ext5v".

Speedstep™ Setup

There are five VID terminals on the board. Determine which VID pins you need to toggle, and set the corresponding DIP switch slides to OFF. Set the signal generator to square wave, with a frequency below 1 kHz, and voltage levels between 0V and 5V. Connect the signal generator to the corresponding VID terminal(s) and to the "sgnd" terminal. Enable the signal generator after soft start.

Adaptive Voltage Positioning

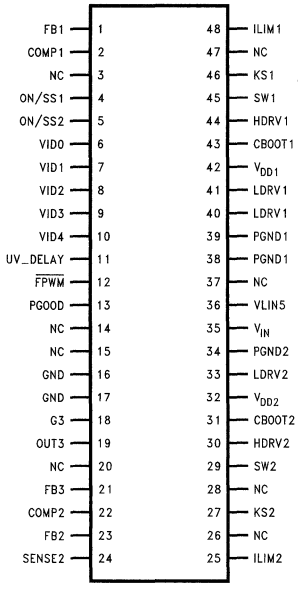
Adaptive voltage positioning (AVP) is a technique that lowers the output voltage when the load is heavier and raises it when the load is lighter. The technique creates more room for fast load transients and thus saves output capacitors To do AVP, cut open the wide trace that is shorting the two pads of R17, and install a current sense resistor. Then use R15 and R18 to adjust the amount of current feedback needed.

Using NFET with Channel 3

While G3 pin of Channel 3 can go up to 4V maximum, if the output voltage is low enough, it is still possible to use an NFET as the pass transistor. With this evaluation board, a TSOP-6 FET can be installed as Q8. Check the "Current Sourcing Capability of Pin G3 vs. Its Voltage" curve in the data sheet and determine if an NFET can be used for your application.

Connection Diagram

TOP VIEW



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48-Lead TSSOP (MTD)
Order Number LM2633MTD
See NS Package Number MTD48

Pin Descriptions

FB1 (Pin 1): The feedback input for Channel 1. Connect to the load directly.

COMP1 (Pin 2): Channel 1 compensation network connection (connected to the output of the voltage error amplifier).

NC (Pins 3, 14, 15, 20, 26, 28, 37 and 47): No internal connection.

ON/SS1 (Pin 4): Adding a capacitor to this pin provides a soft-start function which minimizes inrush current and output voltage overshoot; A lower than 0.8V input (open-collector type) at this pin turns off Channel 1; also if both ON/SS1 and ON/SS2 pins are below 0.8V, the whole chip goes into *shut down mode.*

ON/SS2 (Pin 5): Adding a capacitor to this pin provides a soft-start function which minimizes inrush current and output voltage overshoot; A lower than 0.8V input (open-collector type) at this pin turns off Channel 2; also if both ON/SS1 and ON/SS2 pins are below 0.8V, the whole chip goes into *shut down mode.*

VID4-0 (Pins 6-10): Voltage identification code. Each pin has an internal pull-up. They can accept open collector compatible 5-bit binary code from the CPU. The code table is shown in *Table 2.*

UV_DELAY (Pin 11): A capacitor from this pin to ground adjusts the delay for the output under-voltage lockout.

$\overline{\text{FPWM}}$ (Pin 12): When $\overline{\text{FPWM}}$ is low, pulse-skip mode operation at light load is disabled. The regulator is forced to operate in constant frequency mode.

PGOOD (Pin 13): A constant monitor on the output voltages. It indicates the general health of the regulators. For more information, see Power Good Truth Table and Power Good Function in Operation Descriptions,

GND (Pin 16-17): Low-noise analog ground.

G3 (Pin 18): Connect to the base of the linear regulator transistor.

OUT3 (Pin 19): Connect to the output of the linear regulator.

FB3 (Pin 21): The feedback input for the linear regulator, connected to the center of the external resistor divider.

COMP2 (Pin 22): Channel 2 compensation network connection (it's the output of the voltage error amplifier).

FB2 (Pin 23): The feedback input for Channel 2. Connect to the center of the output resistor divider.

SENSE2 (Pin 24): Remote sense pin of Channel 2. This pin is used for skip-mode operation.

ILIM2 (Pin 25): Current limit threshold setting for Channel 2. It sinks at a constant current. A resistor is connected between this pin and the top MOSFET drain. The voltage across this resistor is compared with the V_{DS} of the top MOSFET to determine if an over-current condition has occurred in Channel 2.

KS2 (Pin 27): The Kelvin sense for the drain of the top MOSFET of Channel 2.

SW2 (Pin 29): Switch-node connection for Channel 2, which is connected to the source of the top MOSFET.

HDRV2 (Pin 30): Top gate-drive output for Channel 2. HDR is a floating drive output that rides on SW voltage. MOSFET of Channel 2.

CBOOT2 (Pin 31): Bootstrap capacitor connection for Channel 2 top gate drive.

VDD2 (Pin 32): The input voltage supply for the LDRV2 gate driver.

LDRV2 (Pin 33): Low-side gate-drive output for Channel 2.

PGND2 (Pin 34): The analog input voltage supply.

VIN (Pin 35): The Kelvin sense for the drain of the top MOSFET of Channel 2.

VLIN5 (Pin 36): The output of the internal 5V linear regulator. Connect to the ground with a 1UF ceramic capacitor. This pin can be connected to a 5V supply (if available) to improve efficiency.

PGND1 (Pin 38-39): Power ground for Channel 1.

LDRV1 (Pin 40-41): Bottom gate-drive output for Channel 1.

VDD1 (Pin 42): The input voltage supply for the LDRV1 gate driver.

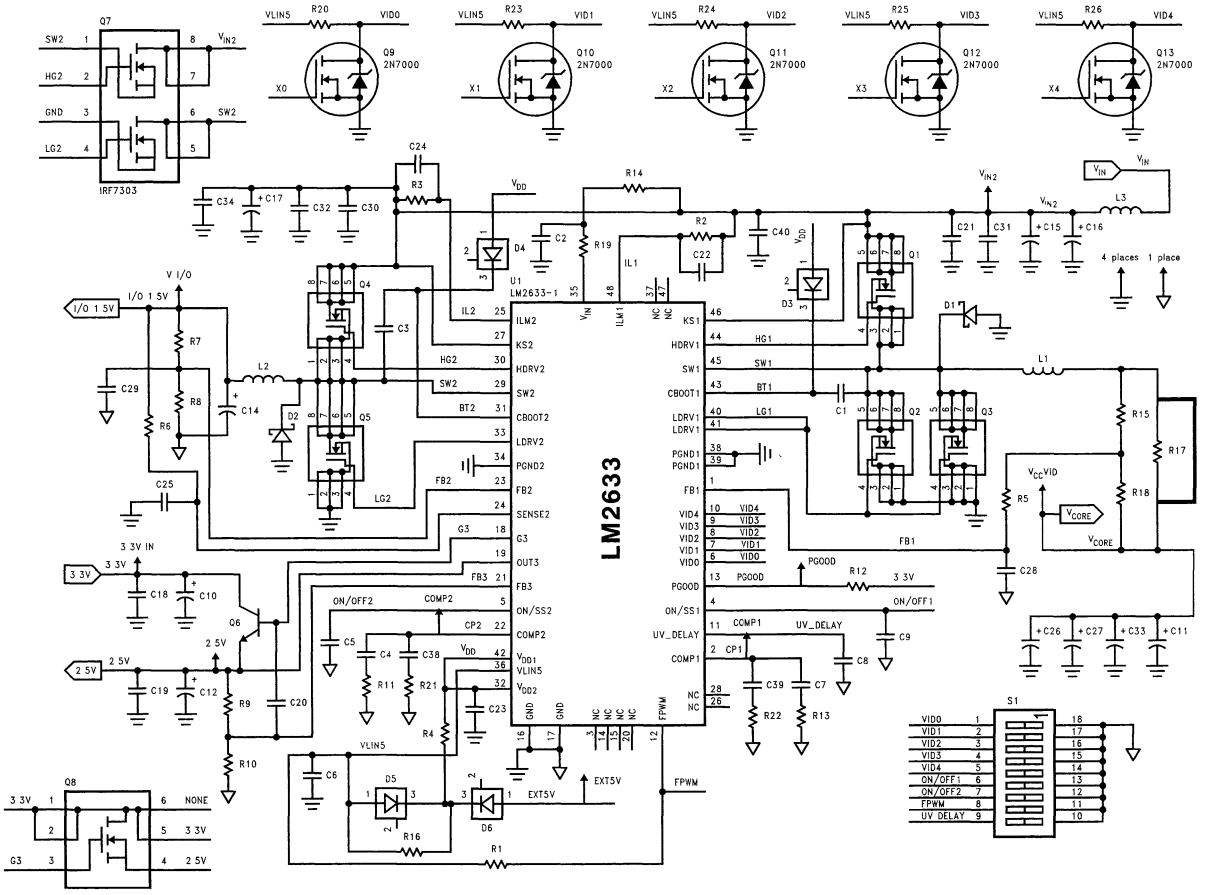
CBOOT1 (Pin 43): Bootstrap capacitor connection for Channel 1 top gate drive.

HDRV1 (Pin 44): Top gate-drive output for Channel 1. HDRV is a floating drive output that rides on SW voltage.

SW1 (Pin 45): Switch-node connection for Channel 1, which is connected to the source of the top MOSFET.

KS1 (Pin 46): The Kelvin sense for the drain of the top MOSFET of Channel 1.

ILIM1 (Pin 48): Current limit threshold setting for Channel 1. It sinks a constant current. A resistor is connected between this pin and the top MOSFET drain. The voltage across this resistor is compared with the V_{DS} of the top MOSFET to determine if an over-current condition has occurred in Channel 1.



LM2633 Evaluation Board

TABLE 1. Bill of Materials (Parts not listed are not installed.)

Designator	Part Specification	Size	Part Type	Part Number	Manufacturer	Qty. Per Board
C15, C16, C17	56UF, 25V, OSCON	RADIAL, 10.3 mm x 10.3 mm	CAPACITOR, OSCON	**25SP56M**	Sanyo	3
C14, C26, C27, C33	1 mF, 4V, 18 mΩ	E Case	CAPACITOR, TANTALUM	**T510E108M004AS**	Kemet	4
C39	150 pF, 16V, X7R, 20%	805	CAPACITOR, CERAMIC	**VJ0805Y151MXJAB**	Vishay	1
C38	680 pF, 16V, X7R, 20%	805	CAPACITOR, CERAMIC	**VJ0805Y681MXJAB**	Vishay	1
C5, C9	4700 pF, 16V, X7R, 20%	805	CAPACITOR, CERAMIC	**VJ0805Y472MXJAB**	Vishay	2
C22, C24	0.01 µF, 50V, X7R, 20%	805	CAPACITOR, CERAMIC	**VJ0805Y103MXJAB**	Vishay	2
C4, C7	0.015 µF, 16V, X7R, 20%	805	CAPACITOR, CERAMIC	**VJ0805Y153MXJAB**	Vishay	2
C1, C2, C3, C8	0.1 µF, 50V, X7R, 20%	805	CAPACITOR, CERAMIC	**VJ0805Y104MXJAB**	Vishay	4
C21, C30, C31, C32, C34, C40	0.33 µF, 50V, X7R, 20%	1206	CAPACITOR, CERAMIC	**VJ1206Y334MXAAB**	Vishay	6
C18, C19, C23	0.47 µF, 16V, X7S, 20%	805	CAPACITOR, CERAMIC	**VJ0805S474MXJAB**	Vishay	3
C6	1 µF, 16V, X7S, 20%	1206	CAPACITOR, CERAMIC	**VJ1206S105MXJAC**	Vishay	1
D3, D4, D5, D6	30V, 200 mA	SOT-23	DIODE, SCHOTTKY	**BAT54**	Vishay	4
L1	1.6 µH, 15.5A, 1.5 mΩ	14.6 mm x 14.6 mm	INDUCTOR	**CEPH149-1R6MC**	Sumida	1
L2	10 µH, 5.4A, 21.6 mΩ	12 mm x 12 mm	INDUCTOR	**CDRH127-100MC**	Sumida	1
L3	1.5 µH, 6.4A, 10 mΩ	13 mm x 9.4 mm	INDUCTOR	**DO3316P-152**	Coilcraft	1
Q9, Q10, Q11, Q12, Q13	60V, 115 mA	SOT-23	N-FET	**2N7002LT1**	ON	5
Q6	40V, 600 mA	SOT-23	BJT, NPN	**MMBT2222ALT1**	ON	1
Q1, Q2, Q3	30V, 10 mΩ @ 4.5V, 16 nC	SO-8	N-FET	**IRF7805**	IR	3
Q4, Q5	30V, 25 mΩ @ 4.5V, 14 nC	SO-8	N-FET	**IRF7807**	IR	2
R11	22k, 5%	805	RESISTOR	**CRCW0805223J**	Vishay	1
R21	2.2k, 5%	805	RESISTOR	**CRCW0805222J**	Vishay	1
R5, R6, R18, R19	0Ω	805	RESISTOR		Vishay	4
R4, R14	10Ω, 20%	805	RESISTOR	**CRCW0805100J**	Vishay	2
R7, R9, R10, R22	10.0k, 1%	805	RESISTOR	**CRCW08051002F**	Vishay	4
R3	16.2k, 1%	805	RESISTOR	**CRCW08051622F**	Vishay	1
R2	26.1k, 1%	805	RESISTOR	**CRCW08052612F**	Vishay	1
R8	47.5k, 1%	805	RESISTOR	**CRCW08054752F**	Vishay	1
R1, R12, R13, R20, R23, R24, R25, R26	100k, 20%	805	RESISTOR	**CRCW0805104J**	Vishay	8

TABLE 1. Bill of Materials (Parts not listed are not installed.) (Continued)

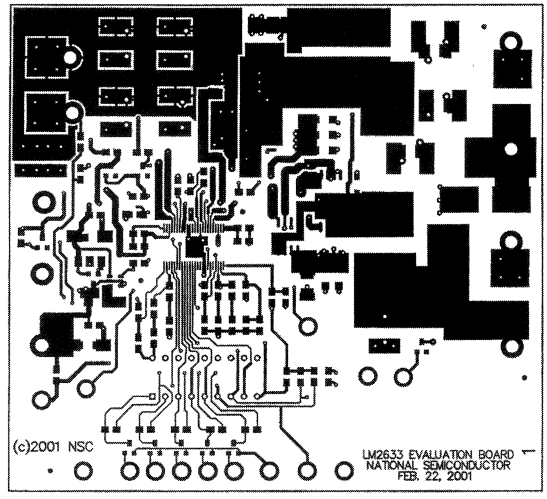
Designator	Part Specification	Size	Part Type	Part Number	Manufacturer	Qty. Per Board
S1	9 POSITION DIP SWITCH	DIP-9	SWITCH, DIP	**435640-6**	AMP	1
TP1–TP23	0.094"	94 mils	TERMINAL	**160-1026-02-01-00**	IPI CAMBION	23
U1	Triple Controller	TSSOP-48	IC	**LM2633**	National	1

TABLE 2. VID Code and DAC Output

VID4	VID3	VID2	VID1	VID0	DAC Voltage (V)
1	1	1	1	1	No CPU*
1	1	1	1	0	0.925
1	1	1	0	1	0.950
1	1	1	0	0	0.975
1	1	0	1	1	1.000
1	1	0	1	0	1.025
1	1	0	0	1	1.050
1	1	0	0	0	1.075
1	0	1	1	1	1.100
1	0	1	1	0	1.125
1	0	1	0	1	1.150
1	0	1	0	0	1.175
1	0	0	1	1	1.200
1	0	0	1	0	1.225
1	0	0	0	1	1.250
1	0	0	0	0	1.275
0	1	1	1	1	1.25
0	1	1	1	0	1.30
0	1	1	0	1	1.35
0	1	1	0	0	1.40
0	1	0	1	1	1.45
0	1	0	1	0	1.50
0	1	0	0	1	1.55
0	1	0	0	0	1.60
0	0	1	1	1	1.65
0	0	1	1	0	1.70
0	0	1	0	1	1.75
0	0	1	0	0	1.80
0	0	0	1	1	1.85
0	0	0	1	0	1.90
0	0	0	0	1	1.95
0	0	0	0	0	2.00

*This code is set to 0.900V for convenience

PCB Layout



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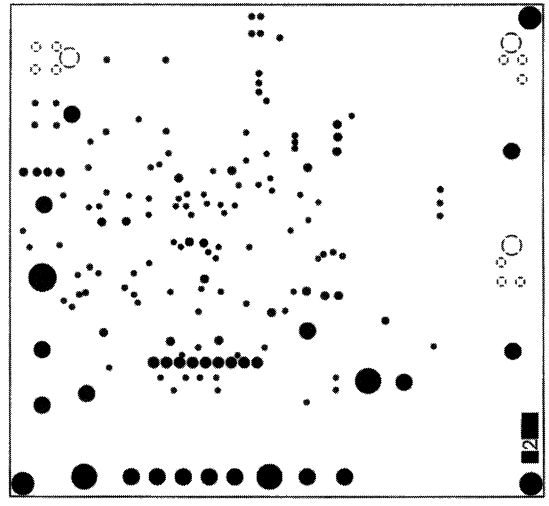
TOP LAYER



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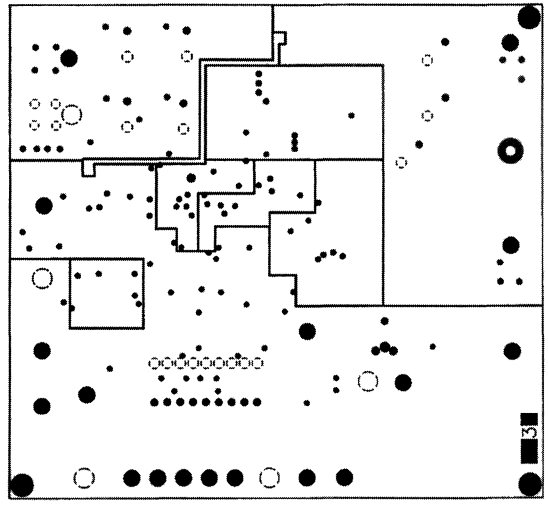
INTERNAL 1

PCB Layout (Continued)



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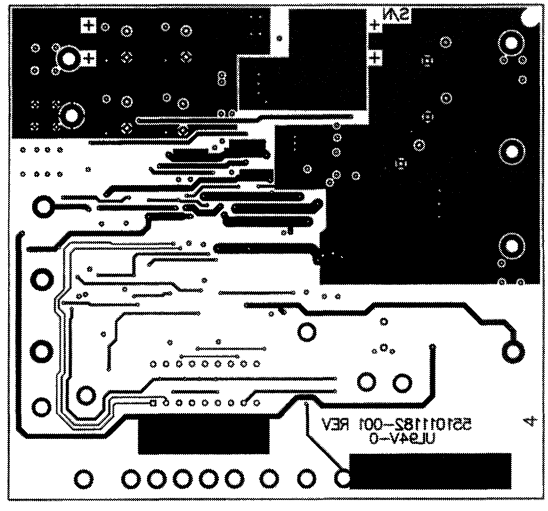
INTERNAL 2



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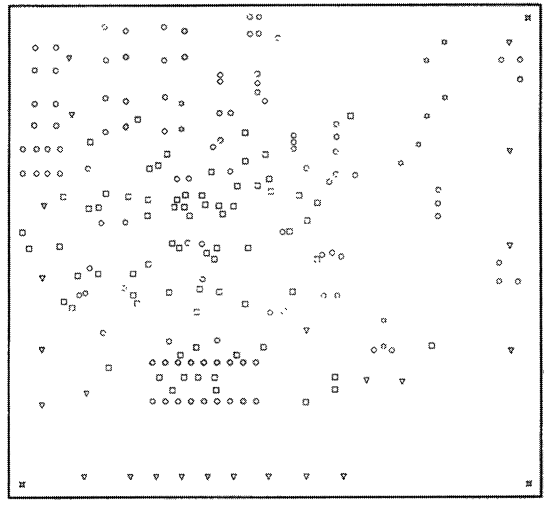
BOTTOM LAYER

PCB Layout (Continued)



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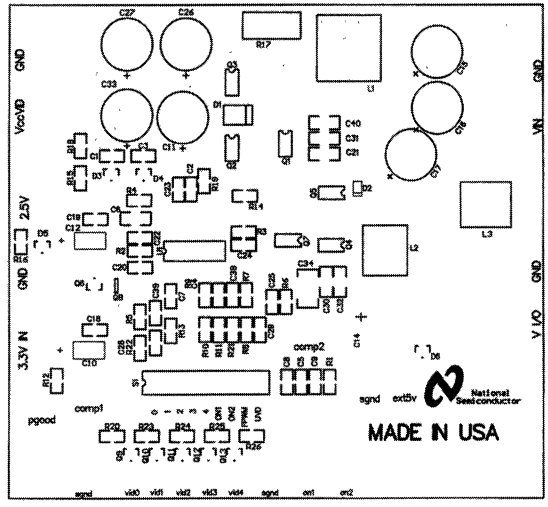
DRILL DRAWING



20025708

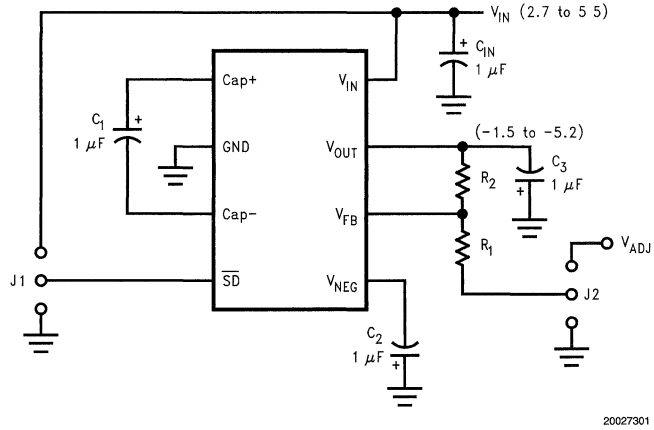
TOP SILKSCREEN

LM2787 Evaluation Board

National Semiconductor
Application Note 1209
Clinton Jensen

This application note provides the schematic and bill of materials for the LM2787 evaluation board. The board was designed specifically for evaluation and therefore is not optimized for the smallest size. Included in the layout are extra pads for all capacitors so a variety of values and case sizes can be tested. The resistors are physically large to make changing the output voltage via feedback resistors easy. The output voltage may also be changed to any acceptable value, or dynamically, by placing the shunt "V_{fb} Sel" in the "V_{ADJ}" position and applying a voltage on the "V_{ADJ}" pin. The default is "V_{fb} Sel" in the "GND" position and an output voltage of −2.4V. Since the output ripple is very low, a direct connection for a scope probe (eliminating the ground lead) is included for monitoring the output.

Evaluation Board Schematic



Bill of Materials

Designation	Description	Value	Manufacturer
U1	LM2787, micro SMD		National Semiconductor
C_{IN}	Input Capacitor	1 µF, X7R Ceramic, 0805	Taiyo Yuden
C1A	Charge Pump Capacitor	1 µF, X7R Ceramic, 0805	Taiyo Yuden
C2A	Charge Pump Output Capacitor	1 µF, X7R Ceramic, 0805	Taiyo Yuden
C3A	LDO Output Capacitor	1 µF, X7R Ceramic, 0805	Taiyo Yuden
R1	Feedback Resistor	261 kΩ, 1206	Any
R2	Feedback Resistor	261 kΩ, 1206	Any

LM3354/5 Evaluation Board

National Semiconductor
Application Note 1214
Clinton Jensen

Intoduction

The LM3354 and LM3355 are switched capacitor DC/DC converters which utilize a number of different gains to achieve output regulation. The LM3354/5 evaluation board is programmed for an output of 4.1V, ideal for White or Blue LED applications. An LM3354 1.8V option is also available. The LM3355 is capable of up to 50mA of output current while the LM3354 is capable of up to 90mA of output current. See the LM3354 datasheet for more information on driving LED's or for information on other standard voltage options of the LM3354. A bill of materials and a schematic follow:

TABLE 1. LM3354/5 Evaluation Board List of Components

Designator	Description	Manufacturer
U1	LM3354/5 DC/DC Converter	National Semiconductor
C_{IN}	10µF ceramic capacitor (X5R, 6.3V)	Taiyo Yuden
C_{OUT}	10µF ceramic capacitor (X5R, 6.3V)	Taiyo Yuden
C1	0.33µF ceramic capacitor (X7R, 16V)	Taiyo Yuden
C2	0.33µF ceramic capacitor (X7R, 16V)	Taiyo Yuden
C_{FIL}	1µF ceramic capacitor (X7R, 10V)	Taiyo Yuden

Typical Application Circuit

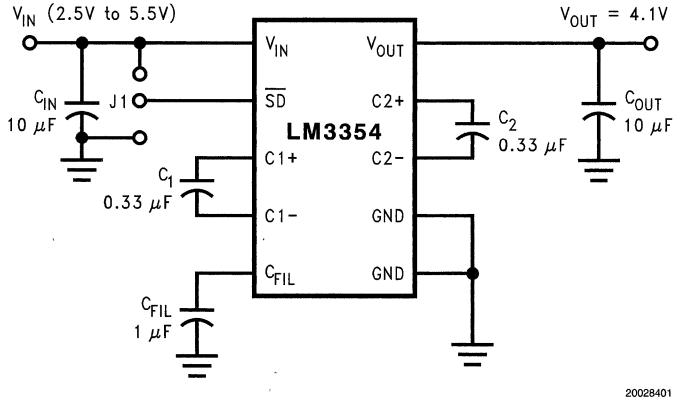
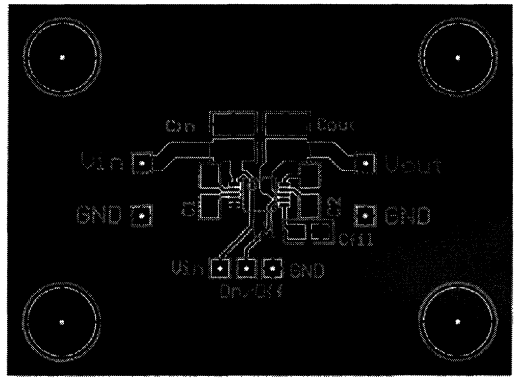


FIGURE 1. Basic Buck/Boost Regulator

Typical Application Circuit (Continued)



20028402

FIGURE 2. Typical Layout, Top View (magnification 1.5X)

LM2655 2.5A Synchronous Switching Regulator Evaluation Board

National Semiconductor
Application Note 1215
Robert Wood

Intoduction

The LM2655 is a high efficiency current -mode controlled PWM step down switching regulator. Efficiencies > 90% are obtained with synchronous operation.

Internal low ON resistance MOSFET and an external N-channel MOSFET provide the highest efficiency design. For cost saving at the expense of some efficiency, the external MOSFET can be replaced with a suitable Shottky diode. (Asynchronous operation). The IC uses patented current sensing circuitry that eliminates the need for an external current sense resistor. A programmable soft start limits start-up current surges and provides a means of sequencing multiple power supplies.

The evaluation board can be obtained by ordering part number LM2655EVAL from your local National Semiconductor sales office, or National's website at http://www.national.com.

Evaluation Board Design

The LM2655 evaluation board is designed to supply 2.5V at a maximum of 2.5A. The input voltage is from 4V to 14V. The board can be loaded with an SO-8 MOSFET as the lower switching element for lower switching losses than a Schottky Diode would provide by itself. The Schottky Diode, D1, improves efficiency.

Components were selected based on the design procedure in the LM2655 data sheet. The feedback resistors can be adjusted to achieve different output voltages. Use the formula:

$$R_{FB1} = R_{FB2}*(V_{out}-V_{ref})/V_{ref}$$

where V_{ref} = 1.238V.

PCB layout is critical to reduce noises and ensure specified performance. See the LM2655 datasheet for layout guidelines. The artwork for this evaluation board is included in this document.

The schematic of the evaluation board is shown in *Figure 2* and the parts list is given in *Table 2*.

The LM2655 has both under voltage and over voltage shutdown protection on the output as well as under voltage lock out on the input. When the under voltage protection occurs, the output voltage can be pulled below ground by the inductor. In applications that must be protected from reverse polarity, an output clamping diode can be added across C_{OUT}.

Soft Start

Soft start in the LM2655 provides delay and current ramp-up rate control at startup. Both are a function of the value of C_{ss}. After a delay, pulses begin with the current limit set to zero then ramped up to full. The total time for soft start process is estimated as:

$$T_{ss} = C_{ss} (.6V/2\mu A) + C_{ss} (2V-.6V)//10\mu A$$

Which reduces to $T_{ss} = C_{ss}$ (440,000)

TABLE 1. Examples:

C_{ss}	T_{ss}
470pF	225.5µs
1nF	451µs
2.2nF	992µs
4.7nF	2.07ms

To begin with, use 4.7nF. This will assure the circuit will get up and running under full load.

If the output voltage does not attain 80% of its intended voltage when the under voltage lockout is enabled, (C_{ss} too small) the regulator will latch off. The actual time required for the output voltage to rise will depend upon the value of the inductor, output capacitor, the load on start up, and the supply voltage, as well as the value of C_{ss}. The calculated value of T_{ss} approximates the time that the under voltage and over voltage lock out circuitry will be delayed from the application of power.

LDelay

A capacitor at Ldelay provides an additional delay in enabling the undervoltage latch after the output voltage has reached 80% of its nominal. The value of the capacitor C_delay is determined by the equation:

T_delay (mS) = C_delay (nF) *.4

200pF is a good start point for this component.

LDelay (Continued)

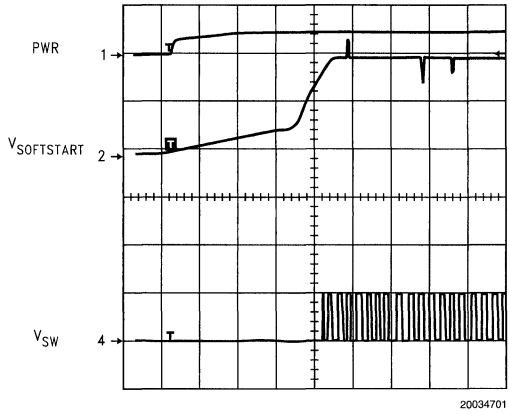
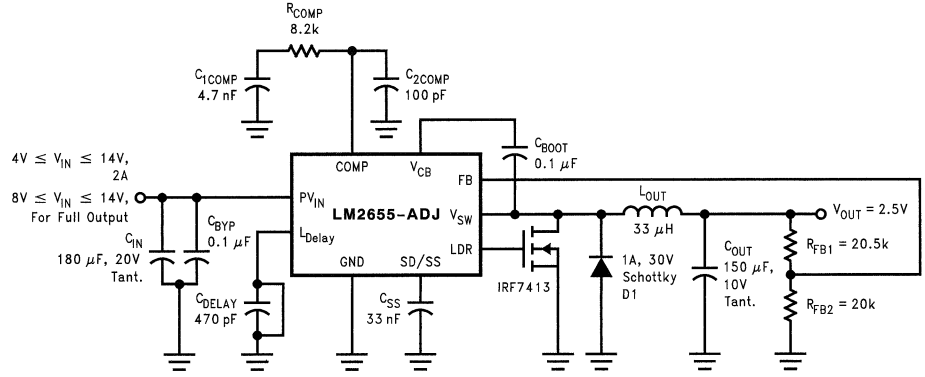


FIGURE 1. Start-Up Waveform

TABLE 2. Parts List

Component	Value	Description	Model Number
C_{OUT}	150µF, 10V	Output Capacitor	595D1570010 (Sprague) (Vishay)
C_{IN}	180µF/20V	Input Capacitor	595D1870020 (Sprague) (Vishay)
C_{DELAY}	200pF, 0805	Delay	VJ0805Y221KXAA (Vishay)
C_{BYP}	0.1µF, 0805	Bypass Capacitor	VJ0805Y104KXAA (Vishay)
C_{ss}	4.7nF, 0805	Soft start	VJ0805Y472KXAA (Vishay)
Q1	3A, 30V	Synchronous N-FET	IRF7413 or Si 4874 (International Rectifier or Siliconix)
D1	1A, 30V (Schottky)	Catch Diode	MBRS130L (On Semiconductor)
L_{OUT}	15µH, 3A	Power Inductor	MIDCOM DUS5121-150
C_{OUT}	150µF, 10V	Output Capacitor	595D1570010 (Sprague) (Vishay)
C_{1COMP}	4.7nF, 0805	Compensation Capacitor	VJ0805Y472KXAA (Vishay)
C_{2COMP}	100pF, 0805	Compensation Capacitor	VJ0805Y100KXAA (Vishay)
C_{BOOT}	0.1µF, 50V, 0805	Bootstrap Capacitor	VJ0805Y104KXAA (Vishay)
R_{COMP}	8.2k, 0805	Compensation Resistor	CRCW08058251F (Dale)
R_{FB1}	15k, 0805	Upper Feedback Resistor	CRCW08051502F (Dale)
R_{FB2}	10k, 0805	Lower Feedback Resistor	CRCW08051002F (Dale)
U1	LM2655-ADJ	Voltage Regulator	LM2655MTC-ADJ (National Semiconductor)



$V_{OUT} = 1.23 * (R_{FB1} + R_{FB2})/R_{FB2}$

C_{DELAY} is shorted to turn off undervoltage protection.

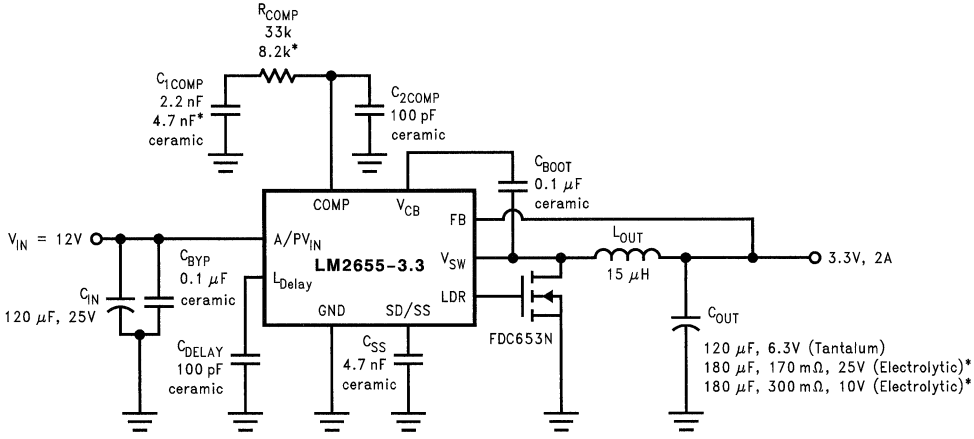
A jumper between SD/SS and ground provides on/off functionality.

Shipped in synchronous mode. Take MOSFET out to run in Asynchronous mode. Diode is large to accommodate synchronous and asynchronous operation.

D1 will limit output1 Low V_{IN} ... with 3A Diode V_{IN} Low Limit is < 4V.

20034705

FIGURE 2. LM2655 Eval Board Schematic

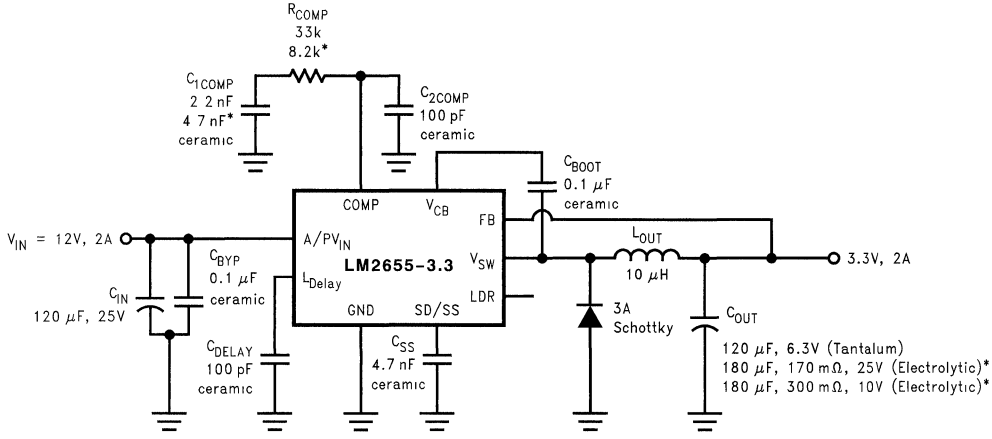


* If electrolytic capacitors are used, make compensation network R_c = 8.2 kΩ and C_c = 4.7 nF.

Efficiency ≅ 91%

20034703

FIGURE 3. LM2655 Buck Converter (12V to 3.3V, Synchronous)



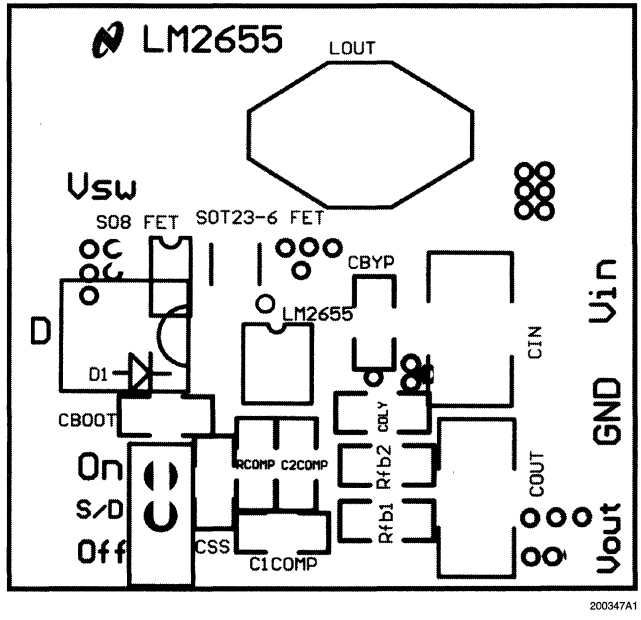
* If electrolytic capacitors are used, make compensation network R_c = 8.2 kΩ and C_c = 4.7 nF.

Efficiency ≅ 88%

20034704

FIGURE 4. LM2655 Buck Converter (12V to 3.3V, Asynchronous)

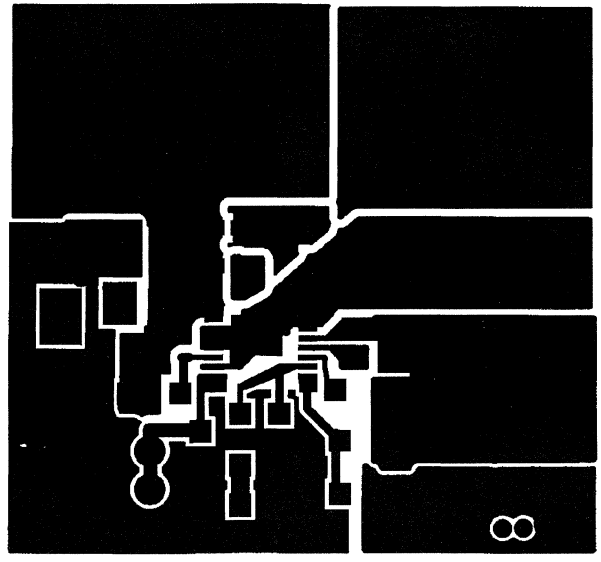
Board Layout



200347A1

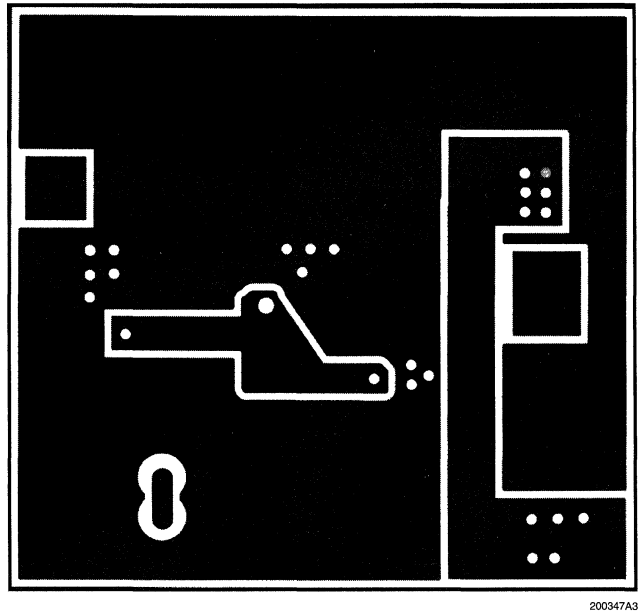
FIGURE 5. Slik Screen

Board Layout (Continued)



200347A2

FIGURE 6. Top Layer



200347A3

FIGURE 7. Bottom Layer

LM2791/2/4/5 Evaluation Board

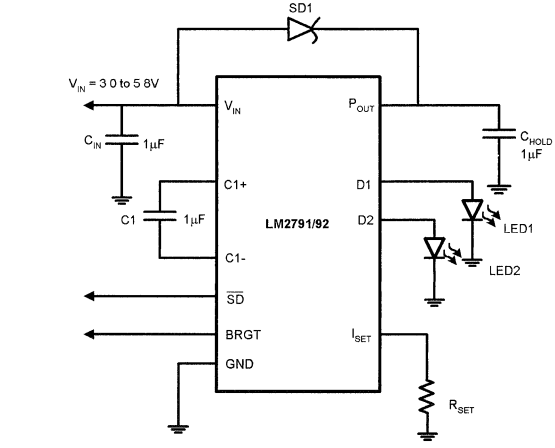
National Semiconductor
Application Note 1218
Anne Lu

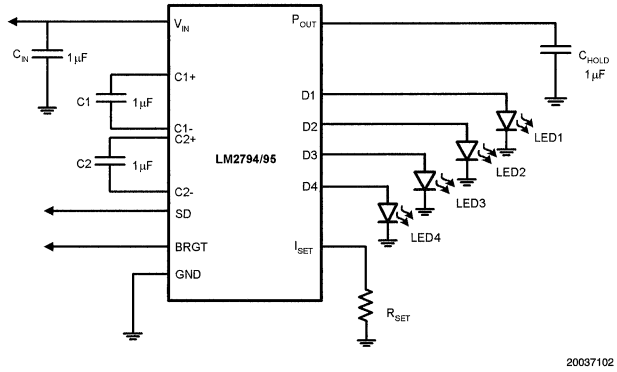
Introduction

The LM2791, LM2792, LM2794 and LM2795 are a family of CMOS Current Regulated Switched Capacitor. They are designed to drive white (or blue) LEDs with matched currents to produce balanced light sources for display backlights. The LM2791/2 is offered in a 10 pin Leadless Leadframe (LLP) package. The LM2791/2 is a charge-pump voltage doubler that provides two regulated current sources. The LM2791 delivers up to a total of 36mA through the LEDs with an offset voltage of 200mV at the Iset pin. The LM2792 delivers up to 34mA with zero offset at the Iset to provide fully off to maximum current control. The switching frequency is between 450KHz to 850KHz for the LM2791 and 900KHz to 1800KHz for LM2792. Both devices accept an input voltage range of 3V to 5.8V. The LM2791 and the LM2792 are also available in active high and low shutdown versions.

The LM2794/5 is offered in a 14 bump micro-SMD package. LM2794/5 is a fractional charge pump that provides four regulated current sources. The devices deliver up to 80mA with an offset voltage of 188mV at the Iset pin. The switching frequency for both device are 325kHz to 675kHz and the input voltage range is 2.7V to 5.5V. Note that if V_{IN} is greater than 4.5V, the device will switch from charge pump mode to pass mode. During pass mode, the device output (P_{OUT}) will follow V_{IN}. This is done to prevent P_{OUT} from exceeding the package voltage rating if V_{IN} is greater than 4.5V. The LM2794 option offers active low for shutdown while the LM2795 offers active high for shutdown.

Typical Application Circuit





R_{SET} Selection (LM2791/2)

R_{SET} is the resistor that sets the current through both LEDs. It is left intentionally for the end users to set the desired current range. Equations below are used for determining R_{SET} value:

Eq. 1 for LM2792:

$$R_{SET} = ((0.42 \bullet BRGT) / ILED) \bullet 25$$

Eq. 2 for LM2791:

$$R_{SET} = (((0.42 \bullet BRGT) + 0.200)/ ILED) \bullet 25$$

For example, if 15mA is the desired current per LED and BRGT = 3V, using the above equation 1 yields R_{SET} = 2.1K ohms. *Table 1* below shows a typical LED current when BRGT is at 3V(LM2792) maximum and *Table 2* shows a typical LED current when BRGT is at 0V(LM2791). If BRGT voltage is other than 3V, *Table 5* shows R_{SET} and BRGT combination per LED current.

TABLE 1. R_{SET} when BRGT = 3V (example given for LM2792)

I_{LED}	*R_{SET}
15mA	2.1kΩ
10mA	3.15kΩ
5mA	6.3kΩ

* Use 1% resistor for Rset

TABLE 2. R_{SET} when BRGT = 0V (example given for LM2791)

I_{LED}	* R_{SET}
15mA	330Ω
10mA	500Ω
5mA	1KΩ

*Use 1% resistor for Rset

R_{SET} Selection (LM2794/5)

Similar to the LM2791/2, R_{SET} is left intentionally for the end users to set the desired current range. Below is the equation for determining R_{SET} value:

Eq. 3 for LM2794/5:

$$R_{SET} = ((0.188 + (0.385 \bullet BRGT)) / ILED) \bullet 10$$

For example, if 15mA is the desired current per LED and BRGT = 0V (or ground), using the above equation 3 yields R_{SET} = 124 ohms. *Table 3* below shows typical LED current when BRGT is tied to ground and *Table 4* shows typical LED current when BRGT is at 3V maximum. If BRGT is used in the application, *Table 5* shows R_{SET} and BRGT combination per LED current.

TABLE 3. R_{SET} when BRGT = 0V

I_{LED}	R_{SET}
15mA	124Ω
10mA	196Ω
5mA	383Ω

*Rset value is rounded off to the nearest 1% value

TABLE 4. R_{SET} when BRGT = 3V

I_{LED}	*R_{SET}
15mA	909Ω
10mA	1.4KΩ
5mA	2.67Ω

*Rset value is rounded off to the nearest 1% value

BRGT (LM2791/2)

A voltage from 0 to 3V may be applied to the BRGT pin to control the brightness of the LEDs by varying the current through the LEDs. Note that some voltage must be provided at BRGT pin or no current will flow through the LEDs for the LM2792. BRGT pin is connected to an internal resistor divider that gives a factor of 0.42 (LM2792). The product of this factor and the voltage at BRGT is fed to the input of an internal amplifier that sets the current mirror resistor R_{SET}. *Table 5* shows the relationship between LED current with various R_{SET} and BRGT values. Care must be taken to ensure that the voltage at BRGT does not cause LEDs current to exceed a total of 34mA (LM2792). Note that calculations are based on when both D1 and D2 are in use.

TABLE 5. LED Current When Using BRGT Input (Example for LM2792 & both D1 & D2 are in use)

Voltage on BRGT (V)	R_{SET}			
	1000Ω	1500Ω	2000Ω	2500Ω
	Current through LED (mA)			
0	0	0	0	0
0.5	5.25	3.5	2.6	2.1
1.0	10.05	7	5.25	4.2
1.5	15.75	10.5	7.88	6.3
2.0	**21**	14	10.5	8.4
2.5	**26.25**	**17.5**	13.1	10.5
3.0	**31.5**	**21**	15.75	12.6

(Values Highlighted in **Boldface** exceed maximum current range of the device if both D1 & D2 are in use)

By rearranging equation 1, the following equation can be used to determine ILED:

Eq. 4 for LM2792:

$$ILED = ((0.42 \bullet BRGT) / R_{SET}) \bullet 25$$

Eq. 5 for LM2791:

$$ILED = (((0.42) + 0.200) \bullet BRGT) / R_{SET}) \bullet 25$$

BRGT (LM2794/5)

A voltage from 0 to 3V may be applied to the BRGT pin to control the brightness of the LEDs by varying the current through the LEDs. BRGT pin is connected to an internal resistor divider and summed with an offset voltage from the internal bandgap (188mV). This voltage is fed to the input of an internal amplifier that sets the current mirror resistor R_{SET}. *Table 6* below shows the relationship between LED current with various R_{SET} and BRGT values. Care must be taken to ensure that the voltage at BRGT does not cause LEDs current to exceed total of 80mA. By rearranging equation 3, the following equation can be used to determine the ILED:

Eq. 6:

$$ILED = ((0.188 + (0.385 \bullet BRGT)) / R_{SET}) \bullet 10$$

BRGT (LM2794/5) (Continued)

TABLE 6. LED Current When Using BRGT Input (D1-D4 are active)

Voltage on BRGT (V)	R_{SET}			
	124Ω	500Ω	900Ω	1750Ω
	Current through LED (mA)			
0	15.16	3.76	2.09	1.07
0.5	**30.69**	7.61	4.23	2.17
1.0	**46.21**	11.46	6.37	3.27
1.5	**61.73**	15.31	8.51	4.37
2.0	**77.26**	19.16	10.64	5.47
2.5	**92.78**	**23.01**	12.78	6.57
3.0	**101.88**	**26.86**	14.92	7.67

(Values Highlighted in **Boldface** exceed Maximum curent range of the device if all D1-D4 are in use).

Besides adjusting the BRGT pin to control the brightness of the LEDs, SD pin can also be used to control the brightness by applying a PWM signal at the SD pin and varying the duty cycle. A duty cycle of zero will turn off the device and a 50% duty cycle waveform will produce an average current of 7.5mA if the intended LED(s) current is 15mA.

Shutdown (LM2791/2)

During normal operation, SD pin is connected to V_{IN} (for LM2792LD-H) or connected to ground (for LM2792LD-L). If SD pin is used to control the brightness instead of the BRGT pin, applying a PWM (Pulse Width Modulation) signal in the range of 100Hz to 1KHz is recommended for best result. In the case of the LM2792, connect BRGT to 3V before applying a PWM signal at SD or connect BRGT pin to GND if LM2791 is used),

Shutdown (LM2794/5)

During normal operation, SD pin is connected to V_{IN} (for LM2794) or connected to ground (for LM2795). If SD pin is used to control the brightness instead of the BRGT pin, a PWM signal in the range of 100Hz to 1KHz is recommended.

Components List for LM2791/2

Component Name	Type	Value	Size	Manufacturer
U1	LM2791/2	LM2791/2LD-L	LLP-10	National Semiconductor
C_{IN}	X7R	C2012X7R1C105K, 16V uF	0805	TDK
C1	X7R	C2012X7R1C105K, 16V uF	0805	TDK
C_{HOLD}	X7R	C2012X7R1C105K, 16V uF	0805	TDK
R_{SET}	Through hold	Value to be determined by the end users, +/-1%		
White LEDs	Surface Mount Device, White LEDs (TOPLED)	LWT67C/LWT673		Osram
Schottky Diode	Surface Mount Device	BAT-54 =4P	SOT23-3	Fairchild

LM2791/2 Evaluation Board

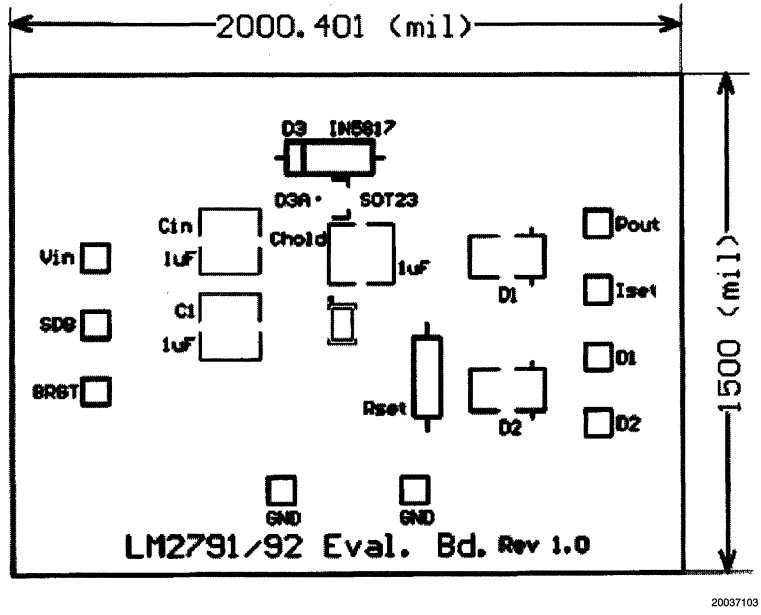


FIGURE 1. Silksreen

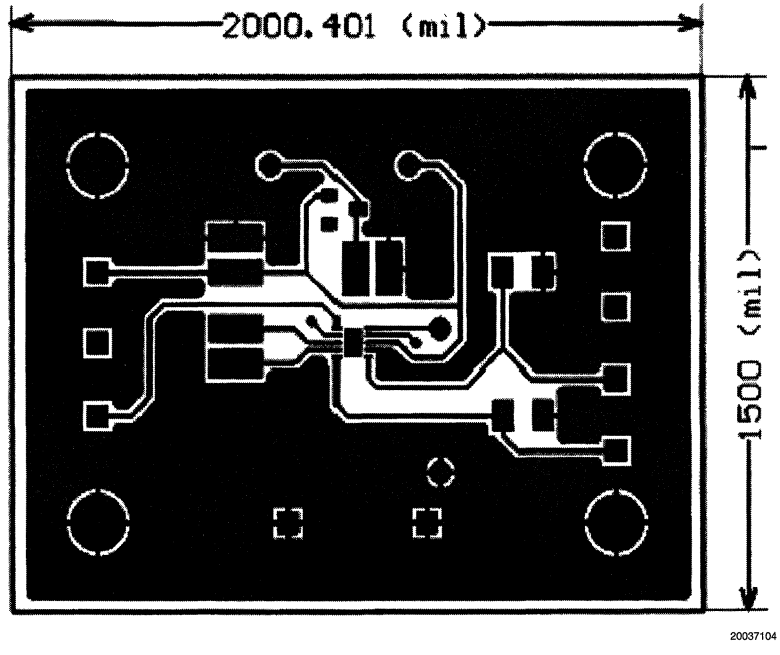


FIGURE 2. PCB Layout

Component List for LM2794/5

Component Name	Type	Value	Size	Manufacturer
U1	LM2794/5	LM2794BL --- Active Low Shutdown LM2795BL --- Active High Shutdown	14 Bump MicroSMD	
C_{IN}	X7R	C2012X7R1C105K, 16V uF	0805	TDK
C1	X7R	C2012X7R1C105K, 16V uF	0805	TDK
C_{HOLD}	X7R	C2012X7R1C105K, 16V uF	0805	TDK
R_{SET}	Through hold	Value to be determined by the end uers, +/-1%		
Diode1 - 4	Surface Mount Device, White LEDs (TOPLED)	LWT67C/LWT673	SOT23-3	Osram

LM2794/5 Evaluation Board

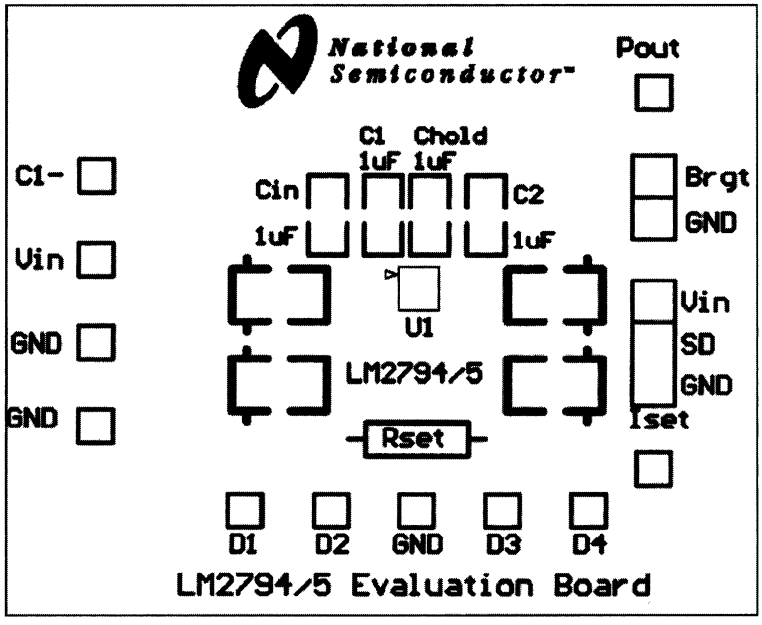


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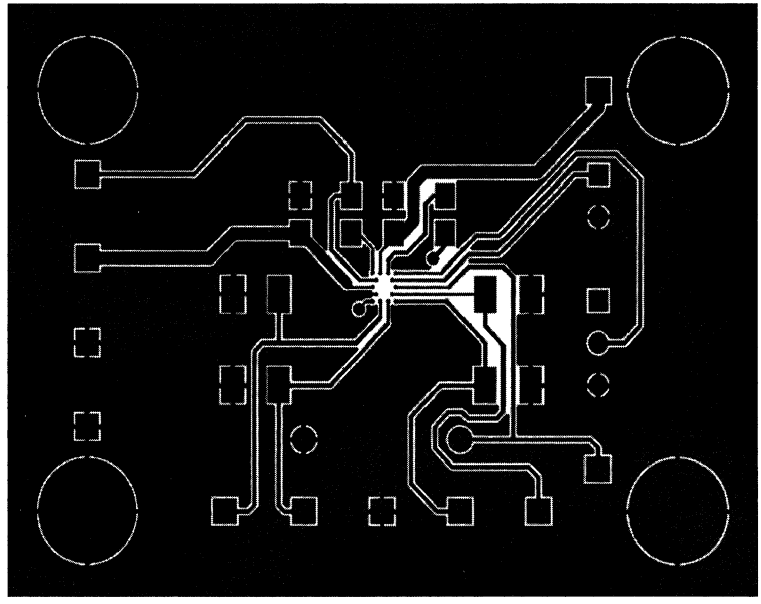
FIGURE 3. Silksreen

LM2794/5 Evaluation Board (Continued)



20037106

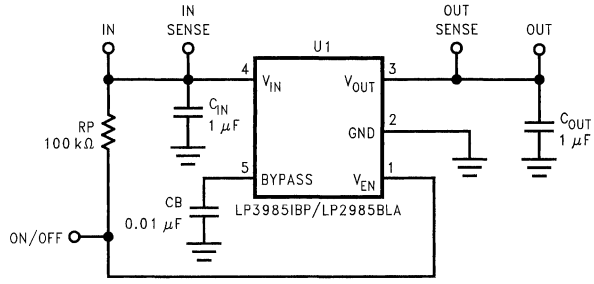
FIGURE 4. PCB Layout

LP3985 MicroSMD-5 Evaluation Board Instruction

National Semiconductor
Application Note 1219
Mary F Kao

This evaluation board is designed to enable independent evaluation of the LP3985 electrical performances. Each board is assembled and tested in the factory. This evaluation board instruction is for the microSMD-5 large bump and small bump packages.

The schematic and layout of the evaluation board are given below:



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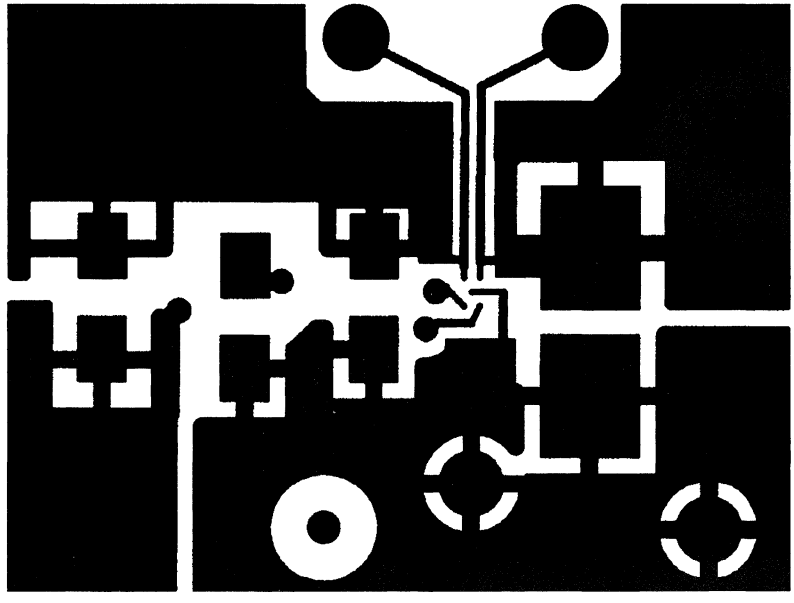

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Note The board layout for the large bump and the small bump microSMD-5 is the same Only the footprints are different

The LP3985 is a micropower CMOS voltage regulator that can provide up to 150 mA of output current. The 0.01 µF bypass capacitor is optional; but if used, it will reduce noise on the regulator output. The RP resistor is tied to V_{IN} so that the regulator is on all the time. To control the V_{EN} pin externally, disconnect RP resistor and use the ON/OFF connector on the evaluation board.

The input sense and output sense pins are used for more precise voltage measurements. These pins are connected to the LP3985 input and output via high impedance traces.

The LP3895 is also available in SOT23-5. An evaluation board for the SOT23-5 package is available as well.

Below is the bill of material for the LP3985 microSMD-5 board.

Designator	Value	Amount	Footprint	Note
RP	100 kΩ	1	0805	
CB	0.01 µF	1	0805	
C_{IN}	1 µF	1	0805	X5R or X7R
C_{OUT}	1 µF	1	0805/1812	X5R or X7R
U1	LP3985IBP-xx, or LP3985IBL-xx	1	BPA05CMC or BLA05ADC	The "xx" corresponds to the appropriate LDO output voltage option.
Test Pins		7		Keystone 1040

LM3485 Evaluation Board

National Semiconductor
Application Note 1227
Naomi Sugiura

Introduction

The LM3485 is a Hysteretic P-FET Buck Controller, which uses a pulse-frequency modulation (PFM) scheme to regulate the output voltage. This LM3485 demo board and the recommended components are intended to demonstrate the performance with a 3.3V output from a 12V source. The demo board can be used with source voltages from 7V to 28V to deliver output load currents up to 1A. By changing the size of a single resistor, regulated output voltages from 1.242V to 5V can be obtained.

The circuit schematic is shown in *Figure 1* and the bill of materials is given in *Table 1*.

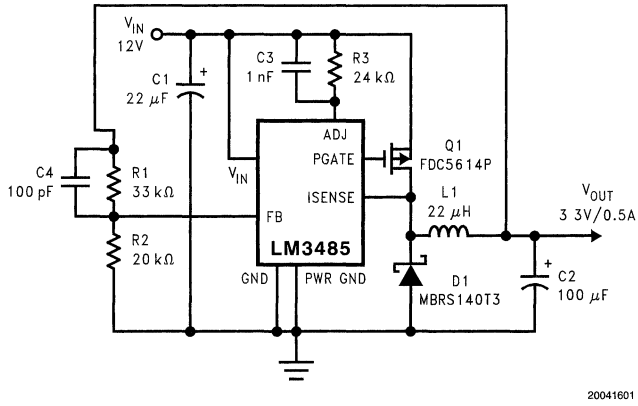


FIGURE 1. Regulator with 3.3V Output at 0.5A

TABLE 1. Bill of Materials

Code	Description	Manufacturer
C1	Input Capacitor CAP-Tantalum 22µF 35V EEJL1VD226R	Panasonic
C2	Output Capacitor CAP-POSCAP 100µF 6.3V 6TPC100M	Sanyo
C3	C_{ADJ} CAP-Ceramic Chip 1nF 50V GRM39X7R102K50	Murata
C4	C_{ff} CAP-Ceramic Chip 100pF 50V GRM39X7R101K50	Murata
D1	Catch Diode Schottky Diode 1A 30V MBRS130T3	On Semiconductor
L1	Inductor 22µH LQH66SN220M01L	Murata
Q1	P-channel MOSFET -60V FDC5614P	Fairchild
R1	Feedback high side resistor Chip Resistor 33KΩ MCR10EZHF3302	Rohm
R2	Feedback low side resistor Chip Resistor 20KΩ MCR10EZHF2002	Rohm
R3	R_{ADJ} Chip Resistor 24KΩ MCR10EZHF2402	Rohm
U1	Buck Controller LM3485	National Semiconductor

Output Voltage Current Limit Setting

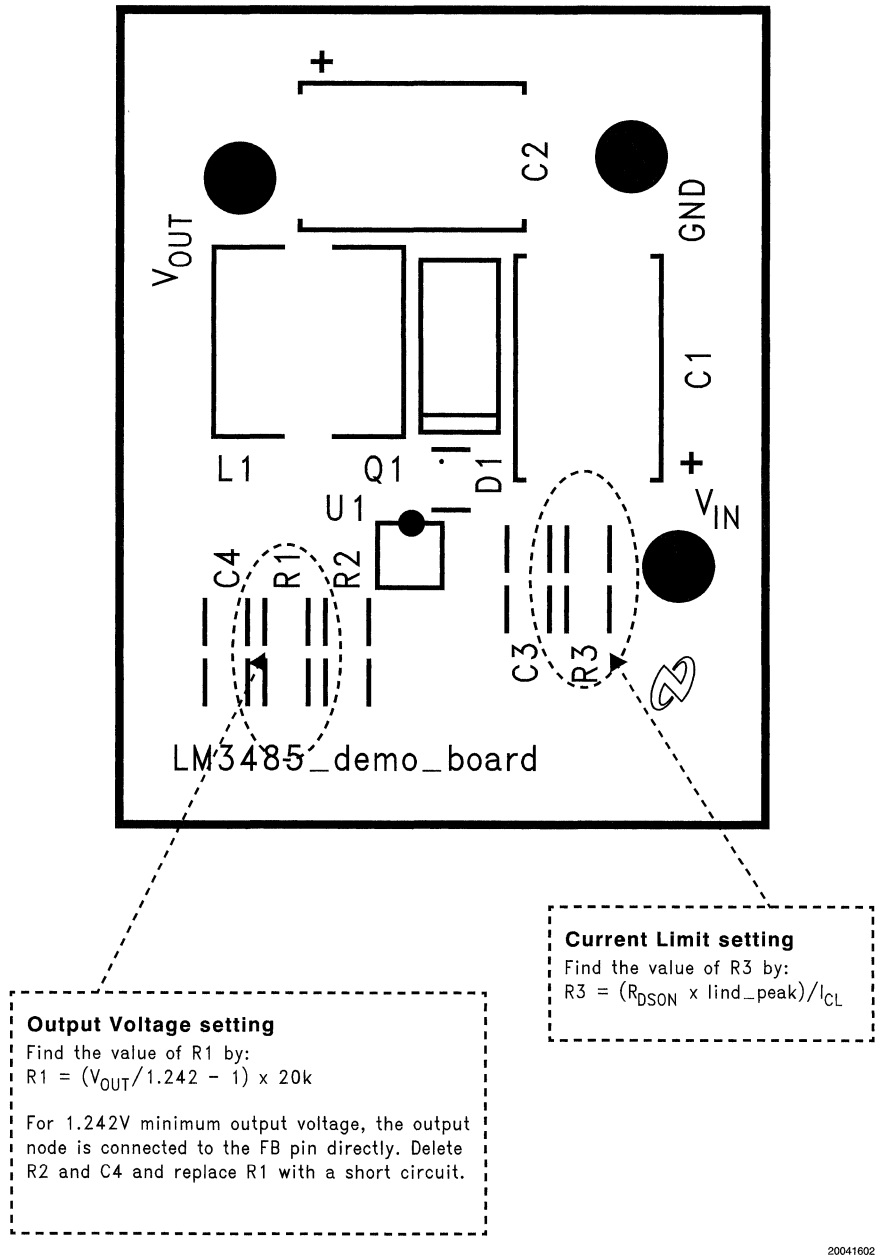
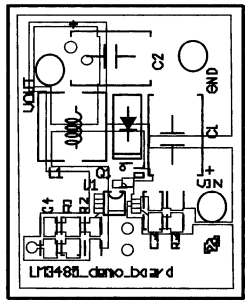


FIGURE 2. Component Location (Top Side)

Layout Fundamentals

The LM3485 can work in a wide range of applications. For your application circuit, proper layout for the buck regulator should be implemented by following a few simple guidelines.

1. Place the power components, which are the MOSFET, diode, inductor and filter capacitors, close together. Make the traces between them as short and as wide as possible.
2. Place the trace for the Gate of the external PFET as close as possible to the PGATE pin of the LM3485.
3. Separate any noise sensitive traces, primarily in the voltage feedback path, from noise source traces associated with the inductor.
4. Keep the trace short between the ground pin of the input capacitor and the anode of the diode.
5. Ensure the ground is low impedance.



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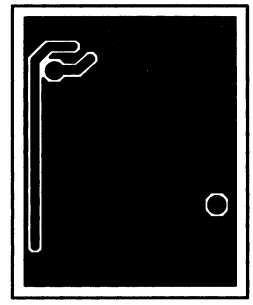
Top Layer



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Bottom Layer

LM2642 Evaluation Board

National Semiconductor
Application Note 1239
Allan Fisher

Introduction

The LM2642 evaluation board has been developed to aid in the design and evaluation of dc/dc converters based on the LM2642 controller IC. The board is intended to be a reusable tool on which several different circuit configurations meeting the requirements of different applications can be built. As shown in Figure 1, the evaluation board is configured to provide two outputs of 5V/3A and 3.3V/3A from an input range of 6V to 30V. The corresponding bill of materials is given in *Table 1*. *Figure 2*, *Figure 9* and *Figure 10* show the full evaluation board schematic and layout.

Board Configuration

The LM2642 Eval. Board can be easily configured for different current sensing schemes, as well as for parallel operation. *Table 1* gives the jumper and part settings for the current sensing. *Table 2* gives the jumper and circuit configurations for parallel and two-channel operation. The evaluation board also includes several optional component pads for reducing switch node ringing and current sense noise, and for low input voltage applicatons.

TABLE 1. Jumper Settings for Current Sensing

Jumper/Part#	Connects To	Current Sense
KSx	VIN	Sense Resistor
RSNx	RSx	
KSx	DSx	$R_{DS(ON)}$ Sense
RSNx	SWx	
C28, 29, 30, 31	Installed	Sense Resistor
C5, 32, 17, 33	Open	
C28, 29, 30, 31	Open	$R_{DS(ON)}$ Sense
C5, 32, 17, 33	Installed	

Board Configuration (Continued)

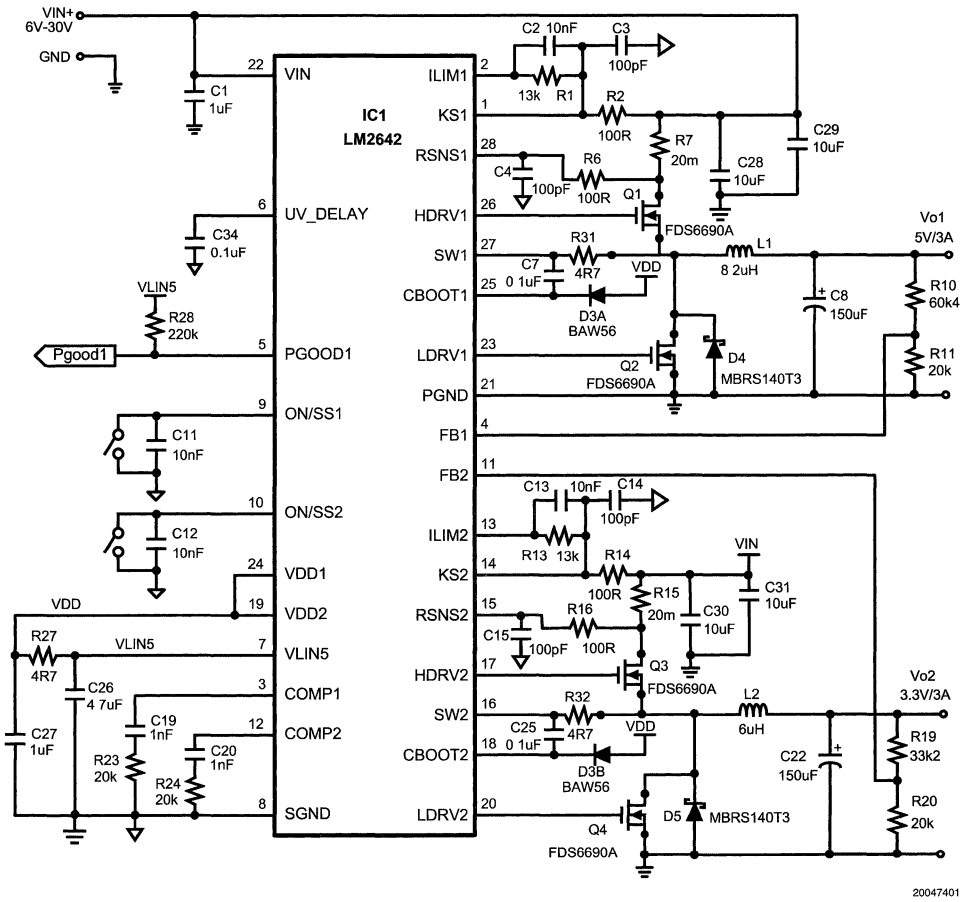


FIGURE 1. Example Circuit

Parallel Operation

In applications with high output current demand, the two switching channels can be configured to operate as a two-180° out of phase converter to provide a single output voltage with current sharing between the two switching channels. This approach greatly reduces the stress and heat on the output stage components while lowering input ripple current. The sum of inductor ripple current is also reduced which results in lowering output ripple voltage. Because precision current sense is the primary design criteria to ensure accurate current sharing between the two channels, both channels must use external sense resistors for current sensing. To minimize the error between the error amplifiers of the two channels, tie the feedback pins FB1 and FB2 together using **J1** and **J2** and connect to one voltage divider for output voltage sensing. Also, tie pins COMP1 and COMP2 together with **R30** and connect to a single compensation network. ON/SS1 and ON/SS2 must be tied together with **R29** to enable and disable both channels simultaneously. Also, both output nodes must be connected.

TABLE 2. Parallel Configuration Settings

Jumper/Part#	2-Ch. Setting	Parallel Setting
J1	Open	Short
J2	Open	Short
R29	Open	Short
R30	Open	Short
R24	Installed	Open
R19	Installed	Open
R20	Installed	open

Optional Components

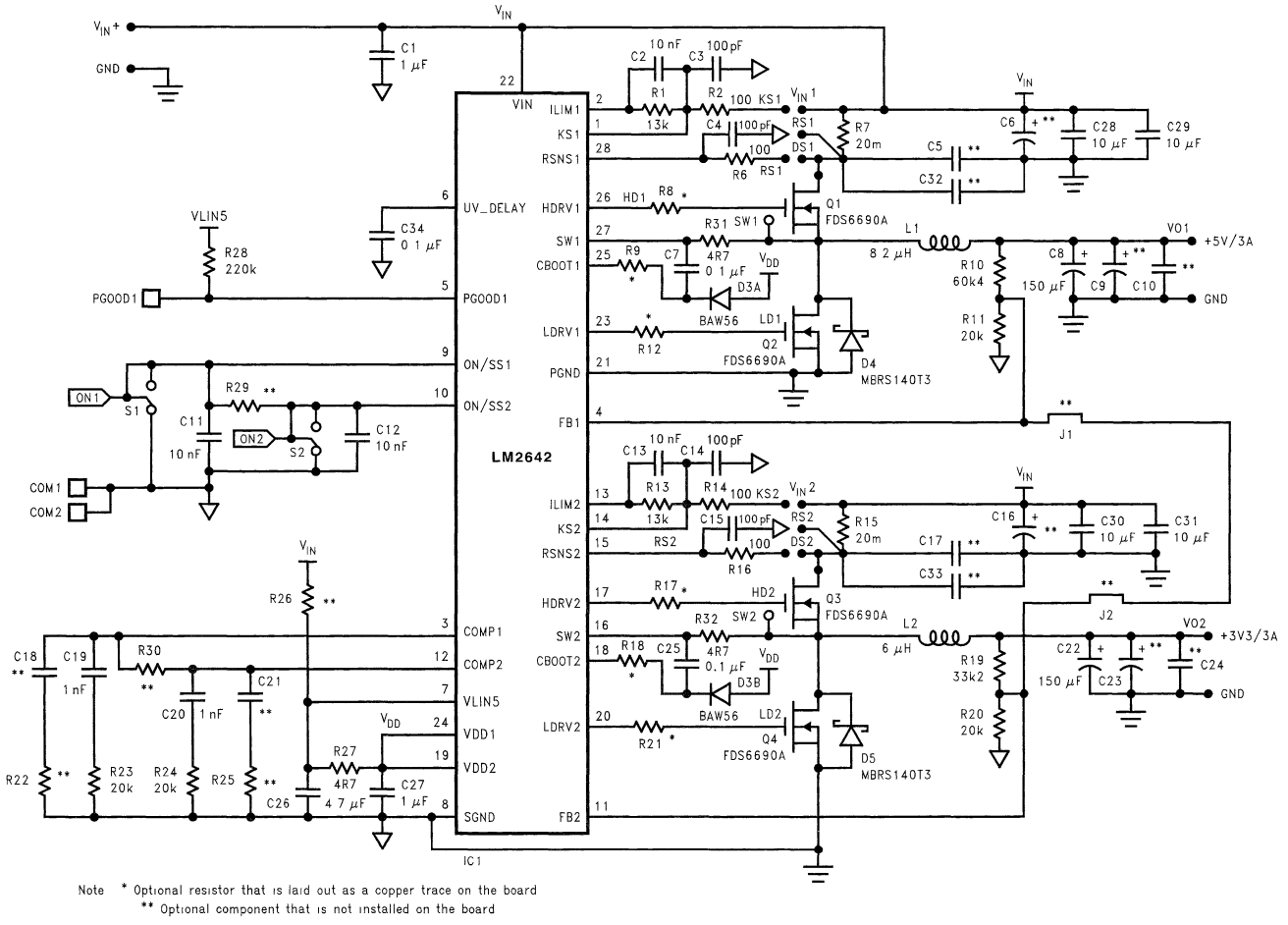
Optional resistor **R26**, must be installed with a 4.7ohm resistor when the input voltage is below 5.5V. This will ensure that VLIN5 does not fall below the UVLO threshold.

Power MOSFETs are very fast switching devices. In synchronous rectifier converters, the rapid increase of drain current in the top FET coupled with parasitic inductance will generate unwanted Ldi/dt noise spikes at the source node of the FET (SWx node) and also at the VIN node. The magnitude of this noise will increase as the output current increases. This parasitic spike noise may turn into electromagnetic interference (EMI), and can also cause problems in device performance. The LM2642 evaluation board provides several options for suppressing this noise.

R-C filters can be added to the current sense amplifier inputs as shown in *Figure 7*. These filters are comprised of **R2, C3, C4, R6,** and R**14, C14, R16, C15,** and are included in the example circuit. These filters will reduce the susceptibility to switching noise, especially during heavy load transients and short on-time conditions. Note that these filters should only be used when a current sense resistor is used.

The resistor in series with the SWx pin **(R31, R32)** slows down the gate drive (HDRVx), thus slowing the rise and fall time of the top FET, yielding a longer drain current transition time and reducing switch node ringing. Top FET switching losses will increase with higher resistance values. Small resistors (1-5 ohms) can also be placed in series with the HDRVx pin **(R8, R17)** or the CBOOTx pin **(R9, R18)** to effectively reduce switch node ringing. A CBOOT resistor will slow the rise time of the FET, whereas a resistor at HDRV will reduce both rise and fall times.

To maintain stable regulation, the FBx pins should remain free of noise. The LM2642 evaluation board provides pads for **C10** and **C24**, which can be used to suppress noise that may be picked up by the FBx traces. Notice that both of these capacitors are placed close to the FBx nodes.



Note * Optional resistor that is laid out as a copper trace on the board
** Optional component that is not installed on the board

20047402

FIGURE 2. Full Schematic of the LM2642 Evaluation Board

TABLE 3. Bill Of Materials

Code	Description	Manufacturer
C1	Cap-MLCC 1uF 50V UMK212F10560ZG	TaiyoYuden
C11	Cap-MLCC 10nF 50V VJ0805Y103KXA	Vishay
C12	Cap-MLCC 10nF 50V VJ0805Y103KXA	Vishay
C13	Cap-MLCC 10nF 50V VJ0805Y103KXA	Vishay
C18, C21	Cap-MLCC 470pF 50V VJ0805Y471KXAMT	Vishay
C19	Cap-MLCC 1nF 25V VJ0805Y102KXA	Vishay
C2	Cap-MLCC 10nF 50V VJ0805Y103KXA	Vishay
C20	Cap-MLCC 1nF 50V VJ0805Y102KXA	Vishay
C22	CAP-SP 150uF 6.3V +/-20% EEFUE0J151R	Panasonic
C25	Cap-MLCC 0.1uF 50V VJ0805Y104KXA	Vishay
C26	Cap-MLCC 4.7uF 10V LMK316475JML	TaiyoYuden
C27	Cap-MLCC 1uF 10V LMK212105FML	TaiyoYuden
C28, C29, C30, C31	Cap-MLCC 10uF 35V GMK 325 F106ZH-B	TaiyoYuden
C3, C4, C14, C15	Cap-MLCC 100pF 50V VJ0805Y101KXA	Vishay
C34	Cap-MLCC 0.1uF 50V VJ0805Y104KXA	Vishay
C7	Cap-MLCC 0.1uF 50V VJ0805Y104KXA	Vishay
C8	CAP-SP 150uF 6.3V +/-20% EEFUE0J151R	Panasonic
COM1&2, PGOOD1	Terminal Silver 0.094" Dia 40F6004	Newark
D3	Switching Diode-Dual 70V 200mA BAW56F	Fairchild
D4	Schottky Diode 40V MBRS140T31A	ON Semiconductor
D5	Schottky Diode 40V MBRS140T31A	ON Semiconductor
IC1	IC controller LM2642	National
L1	Inductor 8u2H CEP125-8R2MC	Sumida
L2	Inductor 6uH CEP125-6R0MC	Sumida
P1	HEADER- BREAKAWAY 2 POST PITCH = 0.156" 26-48-1025	Molex
P2	HEADER- BREAKAWAY 2 POST PITCH = 0.156" 26-48-1025	Molex
P3	HEADER- BREAKAWAY 2 POST PITCH = 0.156" 26-48-1025	Molex
Q1	N-MOSFET FDS6690A	Fairchild
Q2	N-MOSFET FDS6690A	Fairchild
Q3	N-MOSFET FDS6690A	Fairchild
Q4	N-MOSFET FDS6690A	Fairchild
R1	Resistor Chip 13K 0.1W 0.05 CRCW0805*J	Vishay
R10	Resistor Chip 60K4 0.1W 0.01 CRCW08056042F	Vishay
R11	Resistor Chip 20K 0.1W 0.01 CRCW08052002F	Vishay
R13	Resistor Chip 13K 0.1W 0.05 CRCW0805*J	Vishay
R15	Resistor Thick Film 20m 0.5W 0.01 WSL20100.020.01	Vishay
R19	Resistor Chip 33K2 0.1W 0.01 CRCW08053322F	Vishay
R2, R6, R14, R16	Resistor Chip 100R 0.1W 0.05 CRCW08051000J	Vishay
R20	Resistor Chip 20K 0.1W 0.01 CRCW08052002F	Vishay
R22, R25	Resistor Chip 0R0 0.1W ±5% CRCW08050RJ	Vishay
R23	Resistor Chip 20K 0.1W 0.05 CRCW0805203J	Vishay
R24	Resistor Chip 20K 0.1W 0.05 CRCW0805203J	Vishay
R27	Resistor Chip 4R7 0.1W 0.05 CRCW08054R7J	Vishay
R28	Resistor Chip 220K 0.1W 0.05 CRCW0805*J	Vishay
R31, R32	Resistor Chip 4R7 0.1W 0.05 CRCW08054R7J	Vishay
R7	Resistor Thick Film 20m 0.5W 0.01 WSL20100.020.01	Vishay
SW1, SW2	Switch SPST 0.4VA 28V AC/DC A12AB	NKK

TABLE 3. Bill Of Materials (Continued)

Code	Description	Manufacturer
KS1, RS1, KS2, RS2	Jumper Tinned Copper Wire AWG26 L=0.5' x 4pcs.	

Output Voltage Setting

The output voltage for each channel is set by the ratio of a voltage divider as shown in (**R10, R11** and **R19, R20**)*Figure 3*. The resistor values can be determined by the following equation:

$$R_1 = \frac{R_2}{\left(\frac{V_{nom}}{V_{fb}} - 1\right)} \quad (1)$$

Where Vfb=1.238V. Although increasing the value of R1 and R2 will increase efficiency, this will also decrease accuracy. Therefore, a maximum value is recommended for R2 in order to keep the output within .3% of Vnom. This maximum R2 value should be calculated first with the following equation:

$$R_{2\ max} = \frac{.3\% \cdot V_{nom}}{200\ nA} \quad (2)$$

Where 200nA is the maximum current drawn by FBx pin.

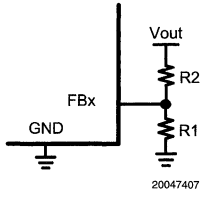


FIGURE 3. Output Voltage Setting

Example: Vnom=5V, Vfb=1.238V, Ifbmax=200nA.

$$R_{2\ max} = \frac{.003 \cdot 5V}{200\ nA} = 75\ k\Omega \quad (3)$$

Choose 60K

$$R_1 = \frac{60k}{\left(\frac{5V}{1.238V} - 1\right)} = 19.75\ k\Omega \cong 20\ k\Omega \quad (4)$$

The output voltage is limited by the maximum duty cycle as well as the minimum on time. *Figure 4* shows the limits for input and output voltages. The recommended maximum output voltage is approximately 1V less than the nominal input voltage. At 30V input, the minimum output is approximately 2.3V.

For input voltages below 5.5V, VLIN5 must be connected to Vin through resistor **R26** (approximately 4.7 ohm).

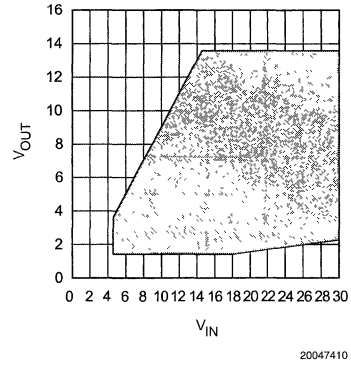


FIGURE 4. Output Voltage Range

Current Sensing and Limiting

As shown in *Figure 5*, the KSx and RSNSx pins are the inputs of the current sense amplifier. Current sensing is accomplished either by sensing the Vds of the top FET or by sensing the voltage across a current sense resistor (**R7** and **R15**) connected from VIN to the drain of the top FET. The advantage of sensing current across the top FET are reduced parts count, cost and power loss, whereas using a current sense resistor improves the current sense accuracy. Keeping the differential current-sense voltage below 200mV ensures linear operation of the current sense amplifier. Therefore, the Rdson of the top FET or the current sense resistor must be small enough so that the current sense voltage does not exceed 200mV when the top FET is on. There is a leading edge blanking circuit that forces the top FET on for at least 166ns. Beyond this minimum on time, the output of the PWM comparator is used to turn off the top FET. Additionally, a minimum voltage of at least 50mV across Rsns is recommended to ensure a high SNR at the current sense amplifier.

Assuming a maximum of 200mV across Rsns, the current sense resistor can be calculated as follows:

$$R_{sns\ max} = \frac{200\ mV}{I_{max} + \frac{1}{2} I_{rip}} \quad (5)$$

where Imax is the maximum expected load current, including overload multiplier (ie:120%), and Irip is the inductor ripple current (see *Equation (14)*). The above equation gives the maximum allowable value for Rsns. Switching losses will increase with Rsns, thus lowering efficiency.

The peak current limit is set by an external resistor (**R1** and **R13**) connected between the ILIMx pin and the KSx pin. An internal 10µA current sink on the ILIMx pin produces a voltage across the resistor to set the current limit threshold which is compared to the current sense voltage. A 10nF capacitor across this resistor is required to filter unwanted noise that could improperly trip the current limit comparator.

Current Sensing and Limiting

(Continued)

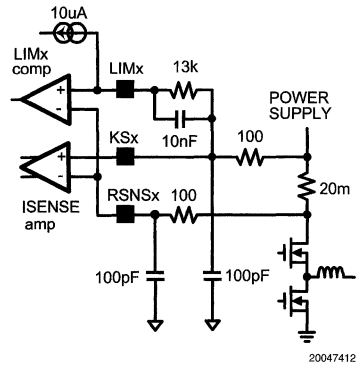


FIGURE 5. Current Sense and Current Limit

Current limit is activated when the inductor current is high enough to cause the voltage at the RSNSx pin to be lower than that of the ILIMx pin. This toggles the comparator, thus turning off the top FET immediately. The comparator is disabled either when the top FET is turned off or during the leading edge blanking time. The equation for current limit resistor, R_{lim}, is as follows:

$$R_{lim} = \frac{(I_{lim} + \frac{1}{2} I_{rip}) R_{sns}}{10\ \mu A} \quad (6)$$

Where Ilim is the load current at which the current limit comparator will be tripped.

When sensing current across the top FET, replace Rsns with the Rdson of the FET. This calculated Rlim value guarantees that the minimum current limit will not be less than Imax. It is recommended that a 1% tolerance resistor be used.

When sensing across the top FET, Rdson will show more variation than a current sense resistor, largely due to temperature. Rdson will increase proportional to temperature according to a specific temperature coefficient. Refer to the manufacturer's datasheet to determine the range of Rdson values over operating temperature or see the *COMPONENT SELECTION* section for a calculation of maximum Rdson. This will prevent Rdson variations from prematurely setting off the current limit comparator as the operating temperature increases.

Output Capacitor Selection (C8, C9, C22 and C23)

In applications that exhibit large and fast load current swings, the slew rate of such a load current transient may be beyond the response speed of the regulator. Therefore, to meet voltage transient requirements during worst-case load transients, special consideration should be given to output capacitor selection. The total combined ESR of the output capacitors must be lower than a certain value, while the total capacitance must be greater than a certain value. Also, in applications where the specification of output voltage regulation is tight and ripple voltage must be low, starting from the required output voltage ripple will often result in fewer design iterations.

ALLOWED TRANSIENT VOLTAGE EXCURSION

The allowed output voltage excursion during a load transient (ΔVc_s) is:

$$\Delta V_{c\_s} = (\delta\% - \varepsilon\%) \cdot V_{nom} - \frac{1}{2} V_{rip}. \quad (7)$$

Where $\pm\delta\%$ is the output voltage regulation window and $\pm\epsilon\%$ is the output voltage initial accuracy.

Example: Vnom = 5V, $\delta\%$ = 7%, $\epsilon\%$ = 3.4%, Vrip = 40mV peak to peak.

$$\Delta V_{c\_s} = (7\% - 3.4\%) \times 5V - \frac{40\ mV}{2}$$

$$= 160\ mV. \quad (8)$$

Since the ripple voltage is included in the calculation of ΔVc_s, the inductor ripple current should not be included in the worst-case load current excursion. That is, the worst-case load current excursion should be simply maximum load current change specification, ΔIc_s.

MAXIMUM ESR CALCULATION

Unless the rise and fall times of a load transient are slower than the response speed of the control loop, if the total combined ESR (Re) is too high, the load transient requirement will not be met, no matter how large the capacitance.

The maximum allowed total combined ESR is:

$$R_{e\_max} = \frac{\Delta V_{c\_s}}{\Delta I_{c\_s}} \quad (9)$$

Example: ΔVc_s = 160mV, ΔIc_s = 3A. Then Re_max = 53.3mΩ.

Maximum ESR criterion can be used when the associated capacitance is high enough, otherwise more capacitors than the number determined by this criterion should be used in parallel.

MINIMUM CAPACITANCE CALCULATION

In a switch mode power supply, the minimum output capacitance is typically dictated by the load transient requirement. If there is not enough capacitance, the output voltage excursion will exceed the maximum allowed value even if the maximum ESR requirement is met. The worst-case load transient is an unloading transient that happens when the input voltage is the highest and when the present switching cycle has just finished. The corresponding minimum capacitance is calculated as follows:

$$C_{min} = \frac{L \cdot \left[\Delta V_{c\_s} - \sqrt{(\Delta V_{c\_s})^2 - (\Delta I_{c\_s} \cdot R_e)^2}\right]}{V_{nom} \cdot R_e^2} \quad (10)$$

Notice it is already assumed the total ESR, Re, is no greater than Re_max, otherwise the term under the square root will be a negative value. Also, it is assumed that L has already been selected, therefore the minimum L value should be

Output Capacitor Selection (C8, C9, C22 and C23) (Continued)

calculated before Cmin and after Re (see Inductor Selection below). Example: Re = 20mΩ, Vnom = 5V, ΔVc_s = 160mV, ΔIc_s = 3A, L = 8μH

$$C_{min} = \frac{8\,\mu H \cdot \left[160\,mV - \sqrt{(160\,mV)^2 - (3A \times 20\,m\Omega)^2}\right]}{5 \times (20\,m\Omega)^2}$$

$$= 47\,\mu F.$$

(11)

Generally speaking, Cmin decreases with decreasing Re, ΔIc_s, and L, but with increasing Vnom and ΔVc_s.

Inductor Selection

The size of the output inductor (**L1** and **L2**) can be determined from the desired output ripple voltage, Vrip, and the impedance of the output capacitors at the switching frequency. The equation to determine the minimum inductance value is as follows:

$$L_{min} = \frac{V_{in} - V_{nom}}{f \cdot V_{in}} \cdot \frac{V_{nom} \cdot R_e}{V_{rip}}$$

(12)

In the above equation, Re is used in place of the impedance of the output capacitors. This is because in most cases, the impedance of the output capacitors at the switching frequency is very close to Re. In the case of ceramic capacitors, replace Re with the true impedance.

Example: Vin (max)= 30V, Vnom = 5.0V, Vrip = 40mV, Re =20mΩ, f = 300kHz

$$L_{min} = \frac{30V - 5.0V}{300\,kHz \cdot 30V} \cdot \frac{5.0V \cdot 20\,m\Omega}{40\,mV}$$

$$L_{min} = 7\,\mu H$$

(13)

Lmin = 7μH

The actual selection process usually involves several iterations of all of the above steps, from ripple voltage selection, to capacitor selection, to inductance calculations. Both the highest and the lowest input and output voltages and load transient requirements should be considered. If an inductance value larger than Lmin is selected, make sure that the Cmin requirement is not violated.

Priority should be given to parameters that are not flexible or more costly. For example, if there are very few types of capacitors to choose from, it may be a good idea to adjust the inductance value so that a requirement of 3.2 capacitors can be reduced to 3 capacitors.

Since inductor ripple current is often the criterion for selecting an output inductor, it is a good idea to double-check this value. The equation is:

$$I_{rip} = \frac{(V_{in} - V_{nom})}{f \cdot L} \cdot D$$

(14)

Also important is the ripple content, which is defined by Irip /Inom. Generally speaking, a ripple content of less than 50% is ok. Larger ripple content will cause too much loss in the inductor.

Example: Vin = 12V, Vnom = 5.0V, f = 300kHz, L = 8μH

$$I_{rip} = \frac{12V - 5.0V}{300\,kHz \cdot 8\,\mu H} \cdot \frac{5.0V}{12V} = 1.22A$$

(15)

Given a maximum load current of 3A, the ripple content is 1.2A / 3A = 40%.

When choosing the inductor, the saturation current should be higher than the maximum peak inductor current and the RMS current rating should be higher than the maximum load current.

Input Capacitor Selection

The LM2642 eval. board provides 5 input capacitor options for each channel (**C5, C6, C28, C29, C32** and **C16, C17, C30, C31, C33**). Referring to *Table 2*, two capacitors are used on each channel and their placement depends on the method of current sensing. C6 and C16 can be installed when higher input capacitances are necessary.

The fact that the two switching channels of the LM2642 are 180° out of phase will reduce the RMS value of the ripple current seen by the input capacitors. This will help extend input capacitor life span and result in a more efficient system. Input capacitors must be selected that can handle both the maximum ripple RMS current at highest ambient temperature as well as the maximum input voltage. In applications in which output voltages are less than half of the input voltage, the corresponding duty cycles will be less than 50%. This means there will be no overlap between the two channels' input current pulses. The equation for calculating the maximum total input ripple RMS current for duty cycles under 50% is:

$$I_{irrm} = \sqrt{I_1^2 D_1 (1 - D_1) + I_2^2 D_2 (1 - D_2) - 2 I_1 I_2 D_1 D_2}$$

(16)

where I1 is maximum load current of Channel 1, I2 is the maximum load current of Channel 2, D1 is the duty cycle of Channel 1, and D2 is the duty cycle of Channel 2.

Example: Imax_1 = 3.6A, Imax_2 = 3.6A, D1 = 0.42, and D2 = 0.275

$$I_{irrm} = \left[(3.6A)^2 \cdot 0.42 \cdot (1 - 0.42) + (3.6A)^2 \cdot 0.275 \cdot (1 - 0.275) - 2 \cdot 3.6A \cdot 3.6A \cdot 0.42 \cdot 0.275\right]^{.5}$$

$$= 2.75A.$$

(17)

Choose input capacitors that can handle 2.75A ripple RMS current at highest ambient temperature. In applications where output voltages are greater than half the input voltage, the corresponding duty cycles will be greater than 50%, and there will be overlapping input current pulses. Input ripple current will be highest under these circumstances. The input RMS current in this case is given by:

$$I_{irrm} = \left[\begin{array}{l}\left[I_1(1 - D_1) + I_2(1 - D_2)\right]^2 (D_1 + D_2 - 1) \\ + \left[I_1(1 - D_1) - I_2(D_2)\right]^2 (1 - D_2) + \\ \left[I_2(1 - D_2) - I_1(D_1)\right]^2 (1 - D_1)\end{array}\right]^5$$

(18)

Where, again, I1 and I2 are the maximum load currents of channel 1 and 2, and D1 and D2 are the duty cycles. This equation should be used when both duty cycles are expected to be higher than 50%.

Input Capacitor Selection (Continued)

Input capacitors must meet the minimum requirements of voltage and ripple current capacity. The size of the capacitor should then be selected based on hold up time requirements. Bench testing for individual applications is still the best way to determine a reliable input capacitor value. The input capacitor should always be placed as close as possible to the current sense resistor or the drain of the top FET.

MOSFET Selection

BOTTOM FET SELECTION (Q2 AND Q4)

During normal operation, the bottom FET is switching on and off at almost zero voltage. Therefore, only conduction losses are present in the bottom FET. The most important parameter when selecting the bottom FET is the on resistance (Rdson). The lower the on resistance, the lower the power loss. The bottom FET power loss peaks at maximum input voltage and load current. The equation for the maximum allowed on resistance at room temperature for a given FET package, is:

$$R_{dson\_max} = \frac{1}{I_{max}^2 \cdot \left(1 - \frac{V_{nom}}{V_{in\_max}}\right)} \times \frac{T_{j\_max} - T_{a\_max}}{\left[1 + TC \cdot (T_{j\_max} - 25°C/W)\right] \cdot R_{\theta ja}} \quad (19)$$

where Tj_max is the maximum allowed junction temperature in the FET, Ta_max is the maximum ambient temperature, $R_{\theta ja}$ is the junction-to-ambient thermal resistance of the FET, and TC is the temperature coefficient of the on resistance which is typically in the range of 10,000ppm/°C.

If the calculated Rdson_max is smaller than the lowest value available, multiple FETs can be used in parallel. This effectively reduces the Imax term in the above equation, thus reducing Rdson. When using two FETs in parallel, multiply the calculated Rdson_max by 4 to obtain the Rdson_max for each FET. In the case of three FETs, multiply by 9.

$$R_{ds\_max} = \frac{1}{(3.6A)^2 \cdot \left(1 - \frac{5V}{30V}\right)} \times \frac{100°C - 60°C}{\left[1 + 0.01/°C \cdot (100°C - 25°C)\right] \cdot 60°C/W} = 35.3\,m\Omega \quad (20)$$

If the selected FET has an Rds value higher than 35.3Ω, then two FETs with an Rdson less than 141mΩ (4 x 35.3mΩ) can be used in parallel. In this case, the temperature rise on each FET will not go to Tj_max because each FET is now dissipating only half of the total power.

TOP FET SELECTION (Q1 AND Q3)

The top FET has two types of losses: switching loss and conduction loss. The switching losses mainly consist of crossover loss and bottom diode reverse recovery loss. Since it is rather difficult to estimate the switching loss, a general starting point is to allot 60% of the top FET thermal capacity to switching losses. The best way to precisely determine switching losses is through bench testing. The equation for calculating the on resistance of the top FET is thus:

$$R_{ds\_max} = \frac{V_{in\_min} \cdot .4}{I_{max}^2 \cdot V_{nom}} \times \frac{T_{j\_max} - T_{a\_max}}{\left[1 + TC \cdot (T_{j\_max} - 25°C/W)\right] \cdot R_{\theta ja}} \quad (21)$$

Example: Tj_max = 100°C, Ta_max = 60°C, Rqja = 60°C/W, Vin_min = 4.5V, Vnom = 5V, and Iload_max = 3.6A.

$$R_{ds\_max} = \frac{5.5V \times .4}{(3.6A)^2 \times 5V} \times \frac{100°C - 60°C}{\left[1 + 0.01/°C \cdot (100°C - 25°C)\right] \cdot 60°C/W} = 13\,m\Omega \quad (22)$$

When using FETs in parallel, the same guidelines apply to the top FET as apply to the bottom FET.

Loop Compensation

The general purpose of loop compensation is to meet static and dynamic performance requirements while maintaining stability. Loop gain is what is usually checked to determine small-signal performance. Loop gain is equal to the product of control-output transfer function and the output-control transfer function (the compensation network transfer function). Generally speaking it is a good idea to have a loop gain slope that is -20dB /decade from a very low frequency to well beyond the crossover frequency. The crossover frequency should not exceed one-fifth of the switching frequency, i.e. 60kHz in the case of LM2642. The higher the bandwidth is, the faster the load transient response speed will potentially be. However, if the duty cycle saturates during a load transient, further increasing the small signal bandwidth will not help. Since the control-output transfer function usually has very limited low frequency gain, it is a good idea to place a pole in the compensation at zero frequency, so that the low frequency gain will be relatively large. A large DC gain means high DC regulation accuracy (i.e. DC voltage changes little with load or line variations). The rest of the compensation scheme depends highly on the shape of the control-output plot.

Loop Compensation (Continued)

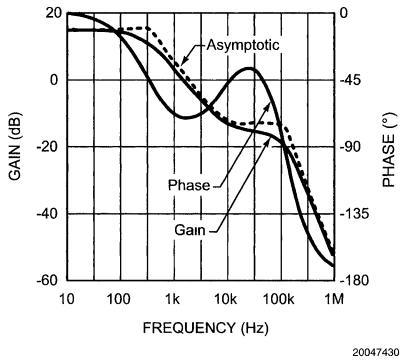


FIGURE 6. Control-Output Transfer Function

As shown in *Figure 6*, the control-output transfer function consists of one pole (fp), one zero (fz), and a double pole at fn (half the switching frequency). The following can be done to create a -20dB /decade roll-off of the loop gain: Place the first pole at 0Hz, the first zero at fp, the second pole at fz, and the second zero at fn. The resulting output-control transfer function is shown in *Figure 7*.

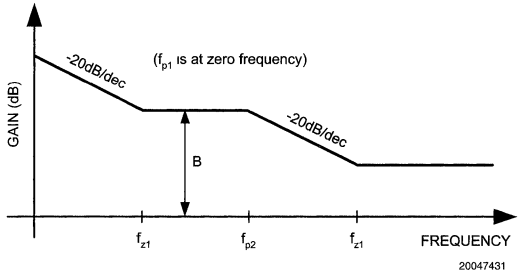


FIGURE 7. Output-Control Transfer Function

The control-output corner frequencies, and thus the desired compensation corner frequencies, can be determined approximately by the following equations:

$$f_z = \frac{1}{2\pi R_e C_o} \quad (23)$$

$$f_p = \frac{1}{2\pi R_o C_o} + \frac{1 - D - .5}{2\pi L_f C_o} \quad (24)$$

Since fp is determined by the output network, it will shift with loading (Ro). It is best to use a minimum Iout value of approximately 100mA when determining the maximum Ro value.

Example: Re=20mΩ, Co=100uF, Romax=5V/100mA=50Ω:

$$f_z = \frac{1}{2\pi \cdot 20\,m\Omega \cdot 100\,\mu F} = 80\,kHz \quad (25)$$

$$f_{p\,min} = \frac{1}{2\pi \cdot 50\Omega \cdot 100\,\mu F} + \frac{1}{2\pi \cdot 300k \cdot 8\mu \cdot 100\,\mu F} = 695\,Hz \quad (26)$$

First determine the minimum frequency (fpmin) of the pole across the expected load range, then place the first compensation zero at or below that value. Once fpmin is determined, Rc1 (**R23** and **R24**) should be calculated using:

$$R_{c1} = \frac{B}{gm}\left(\frac{R_1 + R_2}{R_1}\right) \quad (27)$$

Where B is the desired gain in V/V at fp (fz1), gm is the transconductance of the error amplifier, and R1 and R2 are the feedback resistors. A gain value around 10dB (3.3v/v) is generally a good starting point.

Example. B=3.3v/v, gm=650m, R1=20KΩ, R2=60.4KΩ:

$$R_{c1} = \frac{3.3}{650\mu}\left(\frac{20k + 60.4k}{20k}\right) = 20.4\,k\Omega \cong 20\,k\Omega \quad (28)$$

Bandwidth will vary proportional to the value of Rc1. Next, Cc1 (**C19** and **C20**) can be determined with the following equation:

$$C_{c1} = \frac{1}{2\pi \cdot f_{p\,min} \cdot R_{c1}} \quad (29)$$

Example: fpmin=695Hz, Rc1=20KΩ:

$$C_{c1} = \frac{1}{2\pi \cdot 695\,Hz \cdot 20\,k\Omega} \cong 11\,nF \quad (30)$$

The compensation network (*Figure 8*) will also introduce a low frequency pole which will be close to 0Hz.

A second pole should also be placed at fz. This pole can be created with a single capacitor Cc2 (**C18** and **C21**) and a shorted Rc2 (see *Figure 8*). The minimum value for this capacitor can be calculated by:

$$C_{c2\,min} = \frac{1}{2\pi \cdot f_z \cdot R_{c1}} \quad (31)$$

Cc2 may not be necessary, however it does create a more stable control loop. This is especially important with high load currents and in current sharing mode.

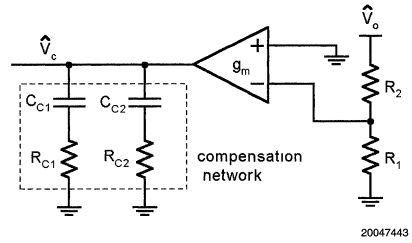
Example: fz=80kHz, Rc1= 20KΩ:

$$C_{c2\,min} = \frac{1}{2\pi \cdot 80\,kHz \cdot 20\,k\Omega} \cong 100\,pF \quad (32)$$

A second zero can also be added with a resistor in series with Cc2 (**R22** and **R25**). If used, this zero should be placed at fn, where the control to output gain rolls off at -40dB/dec. Generally, fn will be well below the 0dB level and thus will have little effect on stability. Rc2 can be calculated with the following equation:

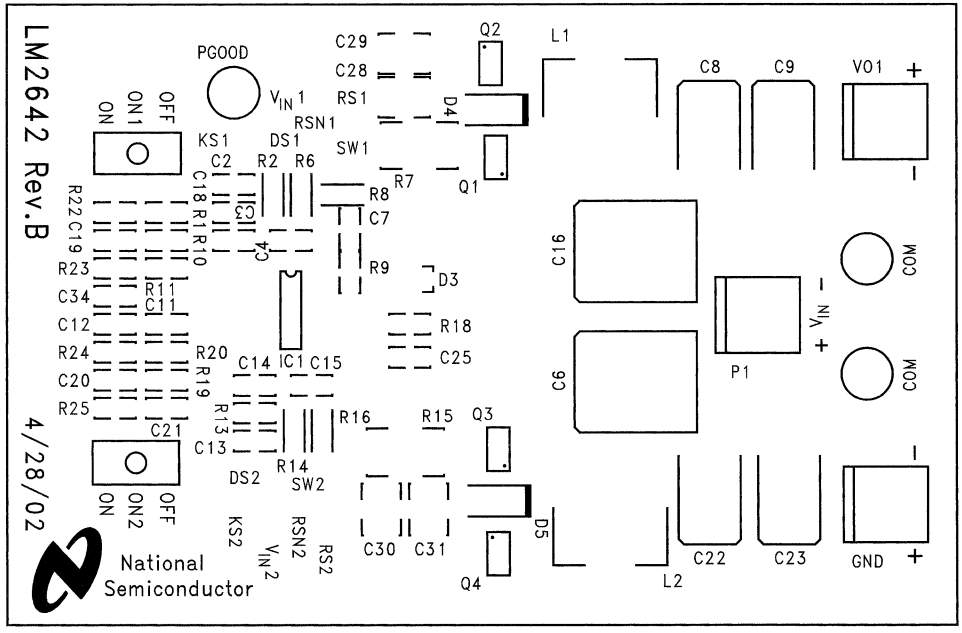
Loop Compensation (Continued)

$$R_{c2} = \frac{1}{2\pi \cdot f_n \cdot C_{c2}} \quad (33)$$



20047443

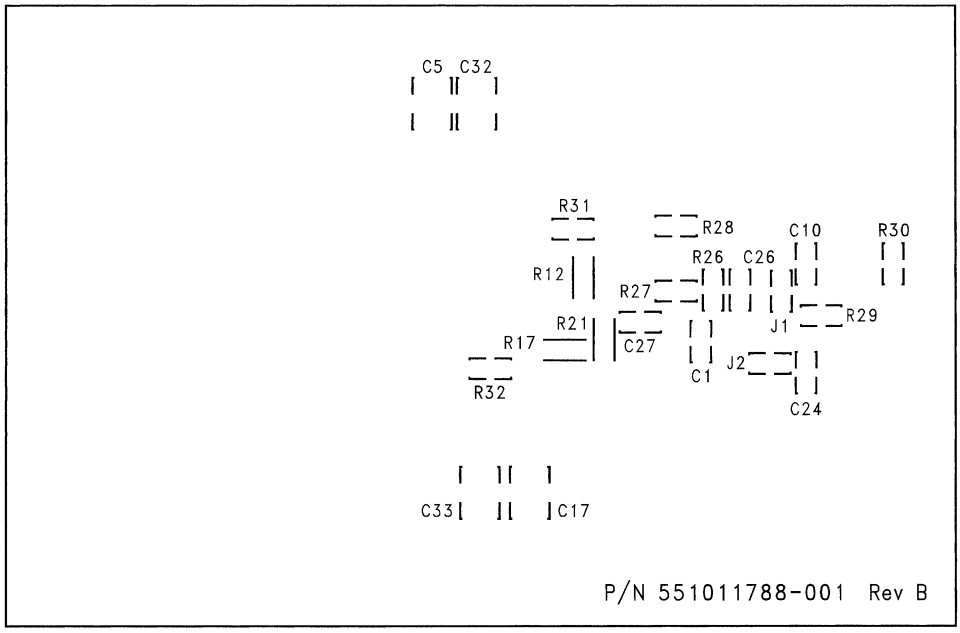
FIGURE 8. Compensation Network



20047403

Top Layer

FIGURE 9.



20047404

Bottom Layer

FIGURE 10.

LP2995 Evaluation Board

National Semiconductor
Application Note 1241
Chance Dunlap

Introduction

The LP2995 evaluation board is designed to provide the design engineer with a fully functional prototype system in which to evaluate the LP2995 in both a static environment and with a complete memory system. There are two versions of the board, while identical in functionality they differ in the package implemented, either an SO-8 or LLP-16 LP2995 is used. This application note contains information regarding the evaluation board. For more information regarding the LP2995 please refer to the datasheet.

Schematic

The following schematic was used to create the layout.

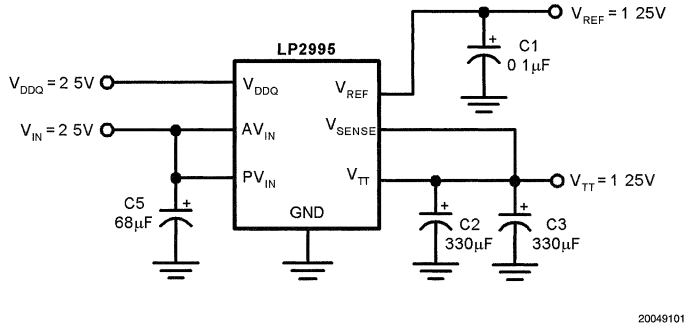


FIGURE 1. Schematic

TABLE 1. Bill Of Materials

Name	Value	Description	Manufacturer	Model Number
U1		LP2995 DDR Linear Regulator	National Semiconductor	LP2995M or LP2995LQ
C1	0.1µF	1206 Ceramic Capacitor X7R 25V	Vishay Vitrammon	VJ1206Y104KXXAT
C2	330µF	6.3V Electrolytic Radial FC Series	Panasonic	EEU-FC0J331S
C3	330µF	6.3V Electrolytic Radial FC Series	Panasonic	EEU-FC0J331S
C4		Not Connected		
C5	68µF	6.3V Electrolytic Radial FC series	Panasonic	EEU-FC0J680

Application

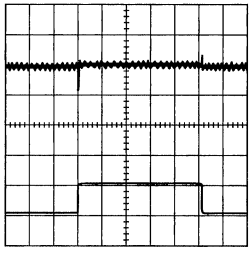
The LP2995 evaluation board can be used immediately in either a static test environment to check functionality or in a memory termination scheme on a motherboard. In either implementation the following steps should be taken to ensure correct operation.

1. Connect leads from the evaluation board. The board layout has been designed to allow banana jack sockets to be directly soldered.
2. V_{IN} should be connected to a 2.5V power supply. This pad connects both the AV_{IN} and PV_{IN} pins of the LP2995.
3. Two GND pads have been provided for ease of use. Either is sufficient for grounding of the board.
4. The V_{DDQ} input provides the internal divide by two reference voltage. Both V_{REF} and V_{TT} will track this internal voltage, nominally a 2.5V will be applied.
5. The V_{REFOUT} pad is the output for the V_{REF} from the LP2995 after being bypassed by a ceramic capacitor. This can be connected either to a multimeter for confirmation or directly to the memory controller and DIMMS.
6. The remaining two pads are for the force and sense leads of the V_{TT} output. These should be connected directly to the termination plane or a multimeter if interested in verification. The output will be regulated where the V_{SENSE} leads connect to the V_{TT} leads permitting the connection to a motherboard without suffering from large resistance drops.

Performance

The following series of scope plots shows the performance of the LP2995 evaluation board when it is subjected to various load tests. On each of the six scope plots there are two traces. The upper trace is the V_{TT} output voltage that has been AC coupled with a scale of 20mV per division. The lower trace is the output current with a scale of 500mA per division. All the load transients begin from an initial condition of zero current and show magnitude. Please refer to the title to determine whether the current flow is into (sinking) or out of (sourcing) the V_{TT} pin. The time scale for all the plots is 2mS per division.

0.5A Load Transient (Sourcing)



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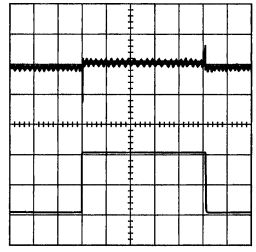
1A Load Transient (Sourcing)



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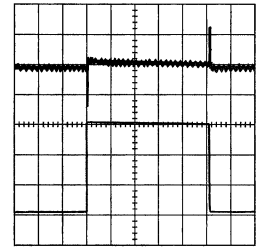
1.5A Load Transient (Sourcing)



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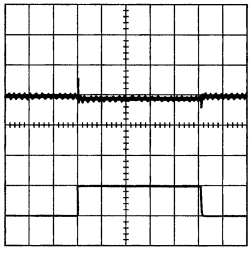
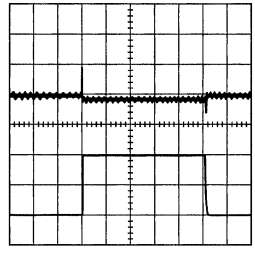
0.5A Load Transient (Sinking)



20049111

1A Load Transient (Sinking)



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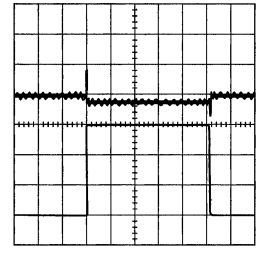
1.5A Load Transient (Sinking)



20049108

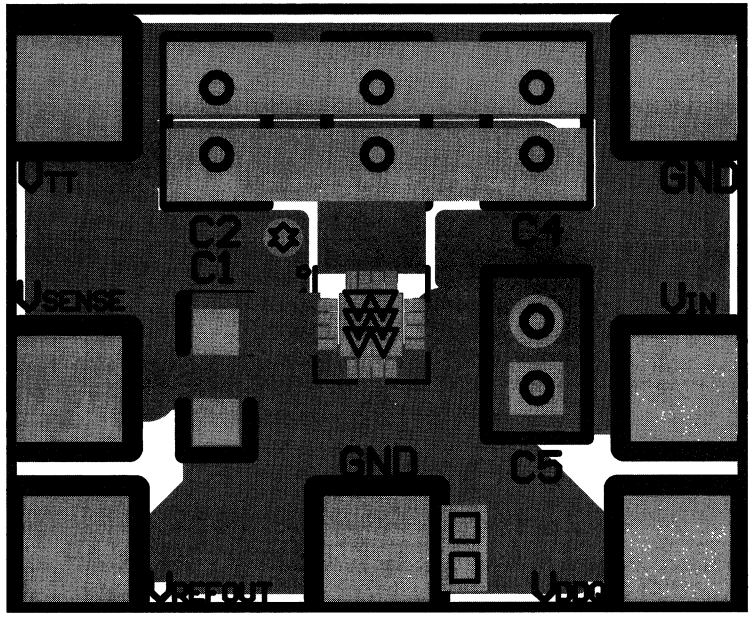
The LP2995 has been designed to accommodate several different capacitor options to allow the designer to optimize the solution for the specific application. For most desktop systems large aluminum electrolytic capacitors will be used for their low cost. However, in height limited situations such as laptops fewer high performance capacitors might be implemented such as specialty polymers. The table below lists some of the capacitors that can be used and a vendor that offers that product line.

TABLE 2.

Capacitor Series	Vendor	Vendor Phone Number
Oscon	Vishay	(207) 324-4140
SP	Panasonic	(714) 373-7857
MLCC	Taiyo Yuden	(800)-348-2496
Aluminum	Panasonic	(714) 373-7857

Board Layout

LLP Top Side



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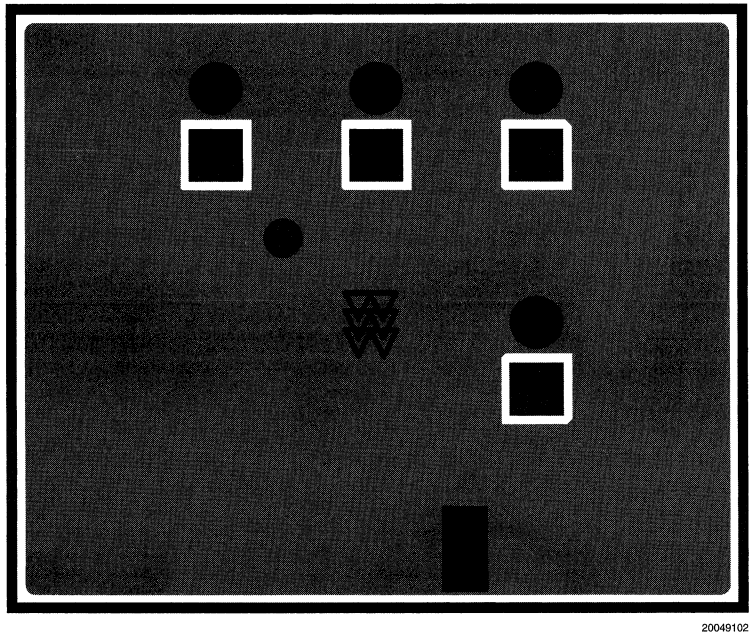
LLP Bottom Side



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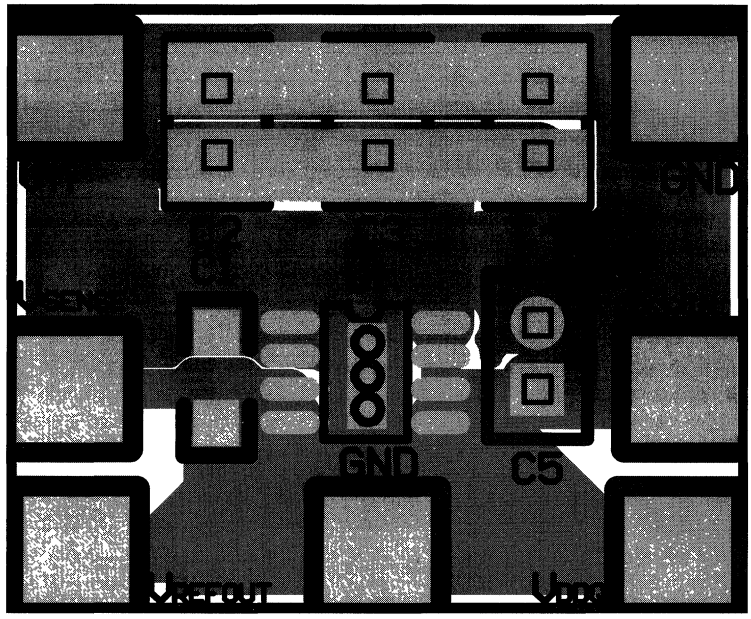
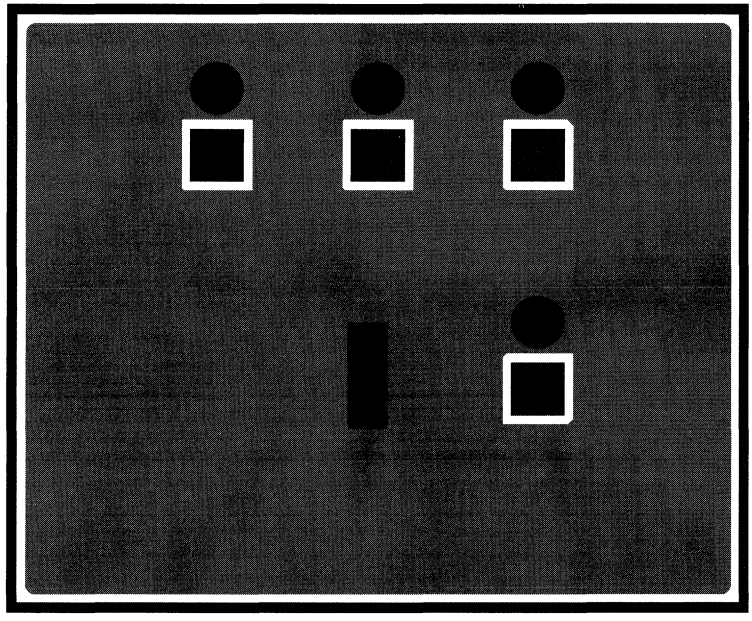
Board Layout (Continued)

SO-8 Top Side



20049104

SO-8 Bottom Side



20049105

Board Layout (Continued)

TABLE 3.

Information	SO-8 Board	LLP-16 Board
Board Material	FR4	FR4
Size	0.9 x 1.1 inches	0.9 x 1.1 inches
Board Thickness	0.062 inch	0.062 inch
Layers	2	2
Copper Thickness	1 oz	1 oz
Plating	HASL	HASL
Thermal Vias	3	6
Thermal Vias Size	25 mil	10 mil
Board Thickness	0.062 inch	0.062 inch

LM2727 Evaluation Board

National Semiconductor
Application Note 1247
Chris Richardson

Introduction

The LM2727 Evaluation board has been designed for a wide variety of components in order to show the flexibility of the LM2727 chips. The input voltage limitations are the same as the chip: 2.2 to 16VDC. The regulated output voltage range is from 0.6V up to 85% of the input voltage. Output current is limited by the components chosen, however the size of this board and the limitation to SO-8 MOSFETs means a realistic limit of about 10A.

The example design steps 12V down to 3.3V at 4A, with a switching frequency of 800kHz. This design can be modified by following the Design Considerations section of the LM2727 datasheet. Design work can also by tested and simulated using WEBENCH™ software, available as an on-line tool or for download at www.national.com.

The board is four layers, consisting of signal/power traces on top and bottom, with one internal ground plane and an internal split power plane. All planes are 1oz. copper, and the board is 62mil FR4 laminate.

Boot Voltage

The default circuit that comes with the LM2727 demo board uses a bootstrap diode and small capacitor (D1 and Cboot) to provide enough gate-to-source voltage on the high side MOSFET to drive the FET. If a separate rail is available that is more than twice the value of Vin, this higher voltage can be connected directly to the BOOT pin, via the BOOT connector, with a 0.1µF bypass capacitor, Cc. In this case D1 and Cboot should be removed from the board. Do not connect both Cc and Cboot/D1 at the same time.

Dual MOSFET Footprints

The LM2727 demo board has two extra footprints for dual N-channel MOSFETs in SO-8 packages. Footprint Q3 corresponds to devices with footprints such as the Si4816DY "LITTLEFOOT Plus" from Vishay Siliconix. Footprint Q4 corresponds to devices with footprints such as the Si4826DY, also from Vishay Siliconix.

Low Side Diode

A footprint D2 is available for a Schottky diode to be placed in parallel with the low side FET. This can improve efficiency because a discrete Schottky will have a lower forward voltage than the low side FET's body diode. The footprint fits SMA size devices. If desired, the low side FET can be removed entirely, and the LM2727 will run as an asynchronous Buck controller.

Additional Footprints

The 1206 footprints Rc2 and Cc3 are available for designs with more complex compensation needs.

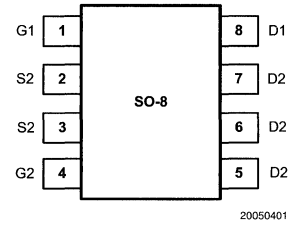


FIGURE 1. Pinout for Dual FET for Footprint Q3

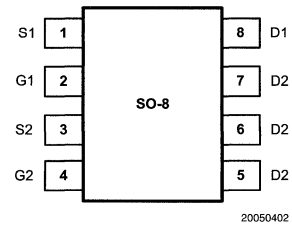


FIGURE 2. Pinout for Dual FET for Footprint Q4

Layout Optimization

The LM2727 PCB layout could be improved with several techniques used in switching converter design. The traces that run from the HG and LG pins of the IC to the gates of the high and low side MOSFETs should be shorter and thicker, reducing their parasitic inductance and resistance. The mid-frequency decoupling capacitor Cinx should be placed as close to the pins of the high side MOSFET as possible. The bulk input capacitors Cin1 and Cin2 should also be placed close, keeping the loop between the input capacitors and the high side MOSFET small. Likewise, the Schottky diode D2 should be located as close as possible to the pins of the low side MOSFET. The local capacitors Cin, Cboot, and Cc (if used) should be close to the pins of the LM2727 IC. These techniques help reduce parasitic inductance throughout the PCB.

Layout Optimization (Continued)

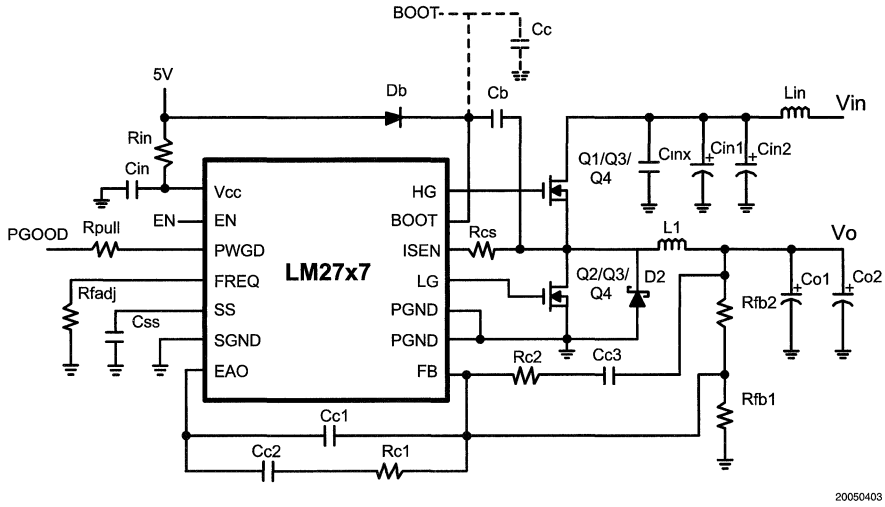
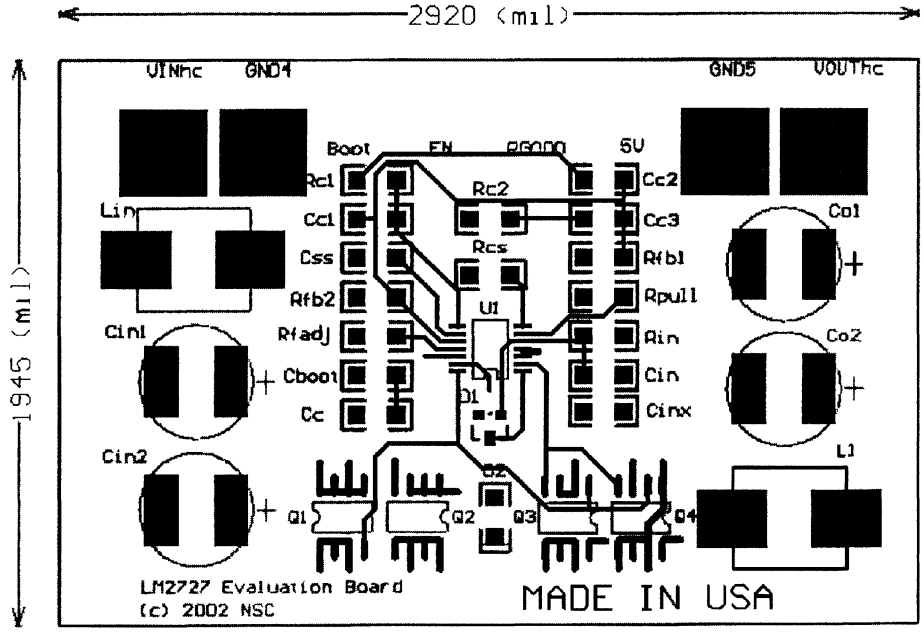


FIGURE 3. Circuit Schematic

TABLE 1. Bill of Materials for Typical Application Circuit

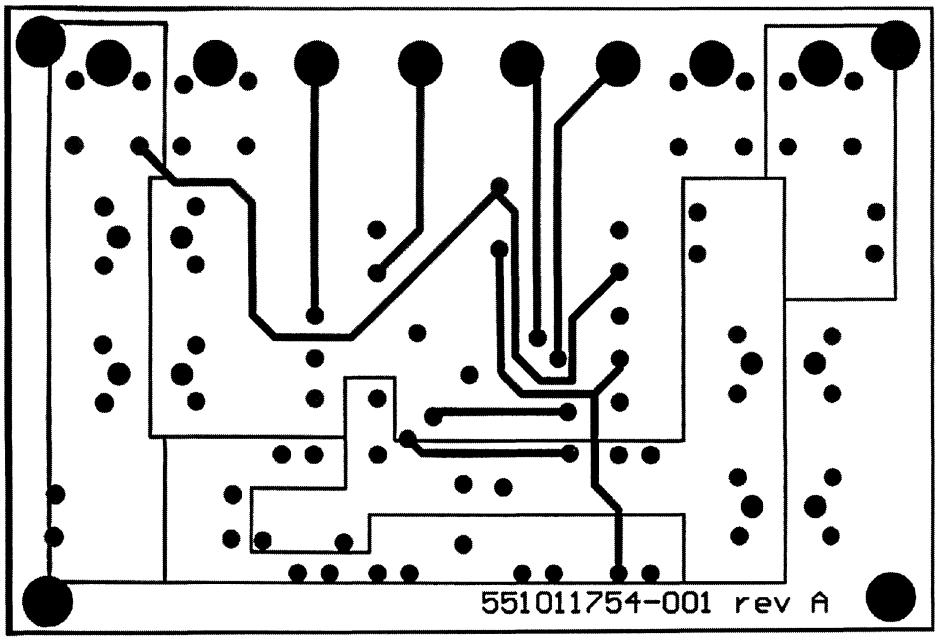
ID	Part Number	Type	Size	Parameters	Qty.	Vendor
U1	LM2727	Synchronous Controller	TSSOP-14		1	NSC
Q1	Si4884DY	N-MOSFET	SO-8	13.5mΩ, @ 4.5V, 15.3nC	1	Vishay
Q2	Si4884DY	N-MOSFET	SO-8	13.5mΩ, @ 4.5V, 15.3nC	1	Vishay
Db	BAT-54	Schottky Diode	SOT-23	30V	1	ON
Lin	P1168.162T	Inductor	12x12x4.5mm	1.6µH, 8.5A 5.4mΩ	1	Pulse
L1	P1168.162T	Inductor	12x12x4.5mm	1.6µH, 8.5A 5.4mΩ	1	Pulse
Cin1	C4532X5R1E106M	Capacitor	1812	10µF 25V 3.3Arms	2	TDK
Cinx	C3216X7R1E105K	Capacitor	1206	1µF, 25V	1	TDK
Co1	6TPB470M	Capacitor	7.3x4.3x3.8mm	470µF 2.5V 55mΩ	2	Sanyo
Cin	C3216X7R1E225K	Capacitor	1206	2.2µF, 25V	1	TDK
Css	VJ1206X123KXX	Capacitor	1206	12nF, 25V	1	Vishay
Cc1	VJ1206A3R9KXX	Capacitor	1206	3.9pF 10%	1	Vishay
Cc2	VJ1206A391KXX	Capacitor	1206	390pF 10%	1	Vishay
Rin	CRCW1206100J	Resistor	1206	10Ω 5%	1	Vishay
Rfadj	CRCW12063052F	Resistor	1206	30.5kΩ 1%	1	Vishay
Rc1	CRCW12069532F	Resistor	1206	95.3kΩ 1%	1	Vishay
Rfb1	CRCW12064871F	Resistor	1206	4.87kΩ 1%	1	Vishay
Rfb2	CRCW12062181F	Resistor	1206	21.8kΩ 1%	1	Vishay
Rcs	CRCW1206272J	Resistor	1206	2.7kΩ 5%	1	Vishay

PCB Layout



20050404

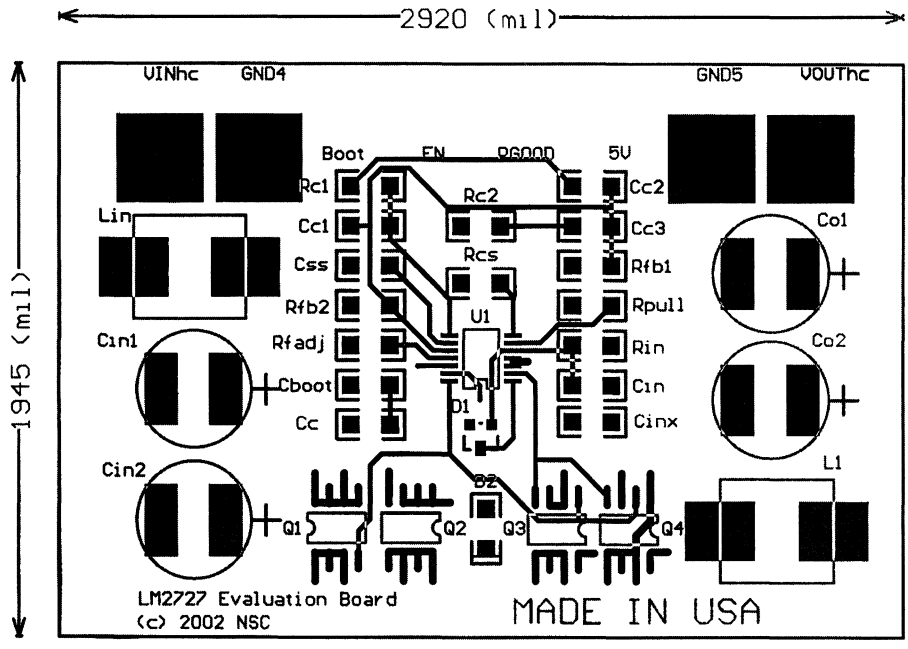
PCB Top Layer and Top Overlay



20050405

PCB Bottom Layer and Internal Power Plane

PCB Layout (Continued)



20050406

PCB Overall

Wide-Input, High Voltage Buck Converter

National Semiconductor
Application Note 1253
Sanjaya Maniktala

Introduction

When the DC input voltage to a buck converter has a wide range, it becomes important to not only select a suitable switching regulator IC for the application, but to select the power components to handle the worst-case input voltage. For a given component, the worst-case may be the maximum input voltage or the minimum input voltage, but in fact may also be somewhere in between. A typical design scenario is presented, using the high voltage SIMPLE SWITCHER® IC, the LM2593HV. The IC is rated for an input of 4.5V to 60V for a 2A load and switches at 150kHz. Considerations reflecting the higher than usual maximum input voltage are also highlighted.

Component Selection

We set the specifications of the converter to be

V_{IN_MAX} = 60V

V_{IN_MIN} = 7V

V_O = 5V

I_O = 2A

Inductor

The inductor design for a buck converter must be done at the maximum input voltage V_{IN_MAX}. This represents the worst-case for all the key inductor parameters: the core loss, the peak/RMS inductor current, the copper loss, the temperature rise, the energy it must handle, and the peak flux density.

We define 'D' as the Duty Cycle and 'r' the ripple current ratio $\Delta I/I_O$. See Application Note AN-1197 for more details on the terms and equations used here.

We choose 'r' to be 0.3 here as per the design procedure inductor nomographs in the LM2593HV datasheet as well as the guidelines in the referenced Application Note. 'r' is related to the inductance through the equation

$$r = \frac{Et}{L \bullet I_{DC}}$$

where 'Et' is the applied Voltμsecs, I_{DC} is the maximum rated load in Amps, and L is the inductance in μH.

The Duty Cycle is

$$D = \frac{V_O + V_D}{V_{IN} - V_{SW} + V_D}$$

where V_D is the diode forward voltage drop (≅ 0.5V), and V_{SW} is the drop across the switch when it is ON, plus any parasitics (≅1.5V). So at maximum input

$$D = \frac{5 + 0.5}{60 - 1.5 + 0\,5} = 0\,093$$

In general it should be ensured that the minimum duty cycle is indeed achievable by the controller. For the LM2593HV, the minimum duty cycle before start of pulse skipping is typically about 5-8%

The switch ON-time is

$$t_{ON} = \frac{D}{f} = \frac{0\,093}{150000} \times 10^6 = 0\,62\ \mu s$$

So the Voltμseconds 'Et' is

$$Et = (V_{IN} - V_{SW} - V_O) \times t_{ON} = (60 - 1.5 - 5) \times 0.62$$
$$= 33.17 V\mu secs$$

Estimated inductance is therefore

$$L = \frac{Et}{r \times I_O} = \frac{33\,17}{0.3 \times 2.0} = 55.3\ \mu H$$

The first pass selection of the inductor is usually on the basis of the inductance calculated above and the max load current.

Note that if the maximum load current was less than 2A, say 1A, and the input voltage is greater than 40V, we may still need to size the inductor for 2A current rather than the maximum load of 1A. This is because during a typical (hard) startup/power-up, the feedback loop is ineffective in limiting the duty cycle, and the peak switch current hits the current limit of the controller. For low input voltages, this is usually not a problem, as the controller can nevertheless still protect itself by limiting the current to the set current limit. But if the input voltage exceeds 40V, it is empirically seen that a typical inductor can saturate so rapidly that the current limit cannot be 'enforced' by the controller. This will cause destruction of the switch. Exculpatory factors are the use of substantial soft-start, and paying attention to the material of the core. Powdered iron cores for example, despite other inherent limitations, do not saturate as 'sharply' as do most ferrites, and survive such momentary overloads much better. Ferrites with 'open' magnetic structures like drums/rods (possessing a large inherent air gap in the closed magnetic path) also fare quite well. In general, for all high voltage devices like the LM2593HV, we recommend a careful evaluation of the inductor to ensure that the converter withstands damage during power-up, and also if the outputs are overloaded/shorted (in which case soft-start cannot help either). In our particular example, any standard 56μH/2A inductor should work.

Input Capacitor

The input capacitor of a buck converter sees the maximum ripple current when the duty cycle is 50% (or closest point within range to this). The input voltage corresponding to D=0.5 is $V_{0\,5}$ below

$$V_{0\,5} - (2 \times V_O) + V_{SW} + V_D \text{ Volts}$$
$$V_{0\,5} - (2 \times 5) + 1.5 + 0.5 = 12 \text{ Volts}$$

Input Capacitor (Continued)

In our case the input voltage range does include this point. But in a more general case, if the input voltage range did not include this point, we would take either V_{IN_MAX} or V_{IN_MIN} whichever happens to be closer to $V_{O\,5}$. And we would need to calculate the duty cycle at that input voltage for the ripple current calculation below.

The ripple current is (for small 'r')

$$I_{RMS\_IN} = I_O \cdot \sqrt{D \cdot [1-D]}\ A$$

$$I_{RMS\_IN} = 2 \cdot \sqrt{0.5 \cdot [1-0.5]} = 1.0\ A$$

The voltage rating of the input capacitor must obviously be higher than the DC Input. Tantalum capacitors were not considered suitable here due to their 50V maximum rating, and their inherent surge current limitations (which are always of concern especially at high input voltages). We recommend at the bare minimum a 63V aluminum electrolytic (preferably 100V) sized to handle 1A RMS current as calculated above. A suitable candidate is Part Number EEVFC1J680Q from Panasonic. This is a 68µF/63V/1.02A SMT Al capacitor. Note that Aluminum electrolytics are quite tolerant of surge voltages provided they do not last 'long'. Further there seems to be no modern statistical evidence to suggest anymore that voltage derating leads to significantly lower failure rates or higher life in such capacitors, as was believed in the past. But please validate these general statements with specific vendors, before relying on them fully.

Output Capacitor

For the output capacitor, the worst-case is again the highest input voltage. The basic selection is based on the ripple current and output ripple.

The ripple current is

$$I_{RMS\_OUT} = I_O \cdot \frac{r}{\sqrt{12}}\ A$$

$$I_{RMS\_OUT} = 2 \cdot \frac{0.3}{\sqrt{12}} = 0.17\ A$$

A suitable candidate is Part Number EEVFC0J221P from Panasonic. This is a 220µF/6.3V/0.23A SMT Al capacitor.

A confirmation of the output voltage ripple is required here. The peak to peak current in the output capacitor is

$I_{PP} = I_O \times r = 0.6$

So with the chosen capacitor, which has an ESR of 0.4 ohms, the output ripple will be 0.6*0.4=0.24V. This is equivalent to ±120mV. If this is considered excessive, a lower ESR capacitor should be selected. However, too low an ESR could lead to instability in the feedback loop particularly when using voltage mode controllers like the LM2593HV.

Catch Diode

The voltage rating of the diode must be higher than the input voltage. We have picked a 100V Schottky diode here. The average current in the catch diode is

$$I_{AVG\_D} = I_O \times (1-D)$$

The diode conducts during the OFF-time, so minimum duty cycle (or highest input) is again the worst-case here. Therefore

$$I_{AVG\_D} = 2 \times (1-0.093) = 1.81A$$

We can use a 3A/100V Schottky diode from any vendor.

Additional Information

power.national.com

www.national.com/pf/LM/LM2593HV.html

www.national.com/an/AN/AN-1197.pdf

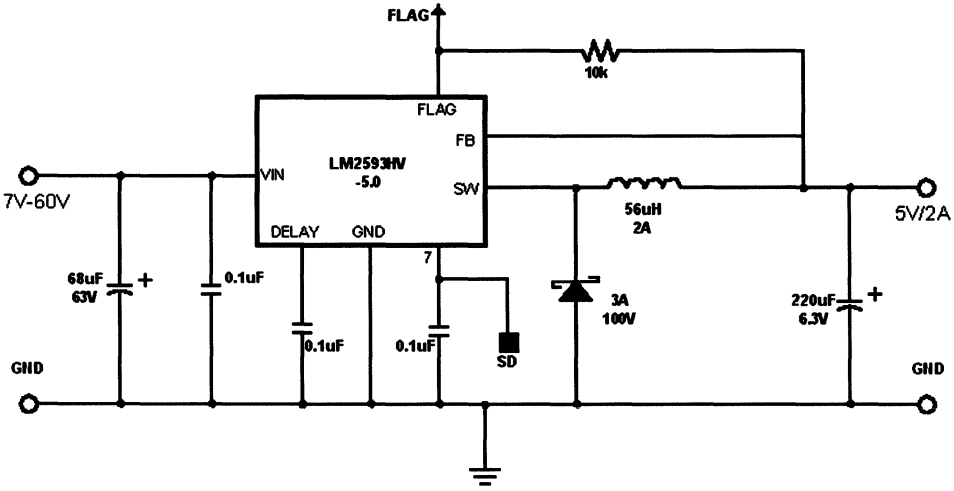


FIGURE 1. Schematic

National's LM2623 Boost Converter - A Simple Technology Twist Produces the Industry's Most Versatile Supply

National Semiconductor
Application Note 1258
John Fairbanks

- Efficient operation from single NiMH to three LiIon input voltages.
- Application circuit meets the emerging 1.8 to 4.5 volt industry standart.
- Iq allows up to 6 months shelf life for rechargeable applications.
- Can be used by most electrical engineers - a control system specialist is not required to design for stable operation.
- Usable in circuits requiring very low ripple voltage.
- Low cost per watt.

Many traditional analog problems are increasingly being solved with digital solutions. As a result, the majority of today's electronic product designers are digital engineers who find it difficult to design with switching power supply ICs. Analog engineers are specialists and control system engineers are even more specialized. Today's high speed, low voltage systems require tight tolerance power supplies with fast response times. This increases the opportunity for complex control system problems (stability problems). These represent stumbling blocks for product designers and they end up needing the IC manufacturers to design their solutions. The product designers would usually prefer to do it themselves and have a higher degree of control over their projects. Since the product designers are usually not control system engineers, their application of a switching power supply requires a supply that is inherently stable.

Gated Oscillators - Advantages and Limitations

Gated oscillator based switching power supplies use inherently stable, on-off control systems, rather than proportional controllers, such as the ones used in pulse width modulated (PWM) systems. The gated oscillator parts typically exhibit higher levels of ripple. However, because of their inherent stability, gated oscillators are usually safe for a digital hardware engineer to design into an application without encountering a control system problem.

Gated oscillators operate at a fixed duty cycle, which limits their range of output voltage and load capability. In order to maintain continuous current mode in a boost converter, a duty cycle greater than $1\text{-}V_{IN}/V_{OUT}$ must be maintained. When this ratio is not maintained, the output capability drops dramatically. Fixing the duty cycle sets the maximum output to input voltage ratio for the power supply. This is an inherent architectural limitation of this type of system. For low output to input voltage ratios, the duty cycle of a gated oscillator will limit the output current of the supply. If the output transistor is conducting 90% of the time, the coil can only discharge into the load 10% of the time. When the output current exceeds 10% of the coil current, the system cannot supply the load. For these ratios, 400 milliamps load current requires an output transistor that can sink at least 4 amps to supply the load. If the duty cycle was 10%, the output transistor would only need to sink 1.1 amps. Running higher coil current than necessary results in excessive overshoot (ripple) when the supply reaches the voltage limit, stops the oscillator and discharges all the stored energy in the coil. Higher than necessary peak coil current also lowers the efficiency because the output is proportional to the current while the losses are proportional to the current squared. Making the duty cycle user adjustable would allow a gated oscillator to be an effective solution for a much broader range of applications.

The Ratio Adaptive Gated Oscillator

Adapts the Duty Cycle to Optimize Output, Efficiency and Ripple as the Battery Discharges.

The LM2623 is a gated oscillator with a frequency proportional to the current into the oscillator pin (see *Figure 1*). The duty cycle is user adjustable with the addition of a small capacitor. This capacitor (C3 in *Figure 1*) also makes the duty cycle adjust itself as the battery runs down. It transfers a constant charge into the oscillator pin when the output device turns off and out of that pin when the output device turns on. This increases the on time and decreases the off time (increases the duty cycle). As the input current and frequency decrease due to the battery voltage running down, the fixed charge transfer becomes a larger percentage of the oscillator current and the duty cycle increases further. This increase in duty cycle as the battery runs down significantly expands the gated oscillator operating range.

The Ratio Adaptive Gated Oscillator (Continued)

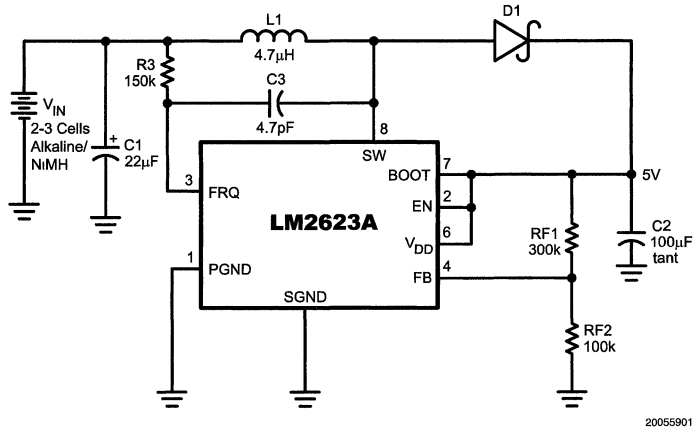


FIGURE 1. LM2623 Boost Converter for Digital Camera Motor

The circuit in *Figure 1* is a very practical LM2623A ratio adaptive circuit to drive a digital camera motor. It produces 5 volts from input voltages ranging between 1.8 and 4.5 volts. The graph below *Figure 2* shows the efficiency at different input voltages and output loads. The duty cycle is not shown, but it varies from about 86% at 1.8 volts in to 71% at 4.5 volts in. Maintaining the 86% duty cycle at 4.5 volts would reduce the efficiency and increase the ripple. Maintaining the 70% duty cycle at 1.8 volts would significantly reduce the output capability. Several camera manufacturers are already requiring 1.8 to 4.5 volt operation from all the power supplies. The 1.8 to 4.5 voltage standard allows a manufacturer to build his product and let the user select disposable Alkalines, NiMH or LiIon at the point of purchase.

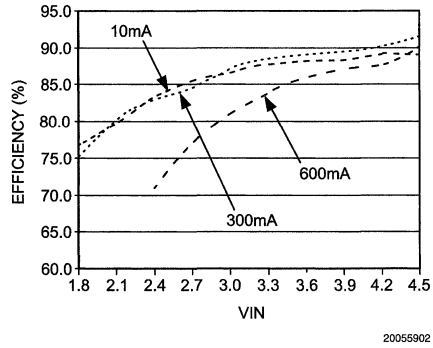


FIGURE 2. Efficiency for Circuit of *Figure 1*

The industry's most flexible power supply needs to solve more problems than just wide range efficiency. Low ripple is important for many applications, particularly digital cameras. This requires matching the duty cycle to the voltage ratio to limit the overshoot due to excessive stored energy in the coil. The change in duty cycle with battery voltage can be increased significantly by adding resistance in series with C3 (see *Figure 3*). The ripple can also be decreased significantly by adding a small capacitor (30 to 100pf) in parallel with RF1 and adding a ceramic capacitor (4.7 to 10µf) in parallel with C2. The circuit in *Figure 3* was developed to supply the analog and digital circuits in a digital camera. It runs between 80% and 90% efficient with ripple below 30 millivolts at 300 ma. Ripple is below 10 millivolts from 50 ma to no load. The typical duty cycle ranges from 69% at 1.8 volts to 38% at 3 volts. These ripple and efficiency figures compare favorably with PWM parts in the same application. The quiescent current of this circuit will also support up to 6 months of shelf life in a rechargeable application using two AA NiMH cells.

The Ratio Adaptive Gated Oscillator (Continued)

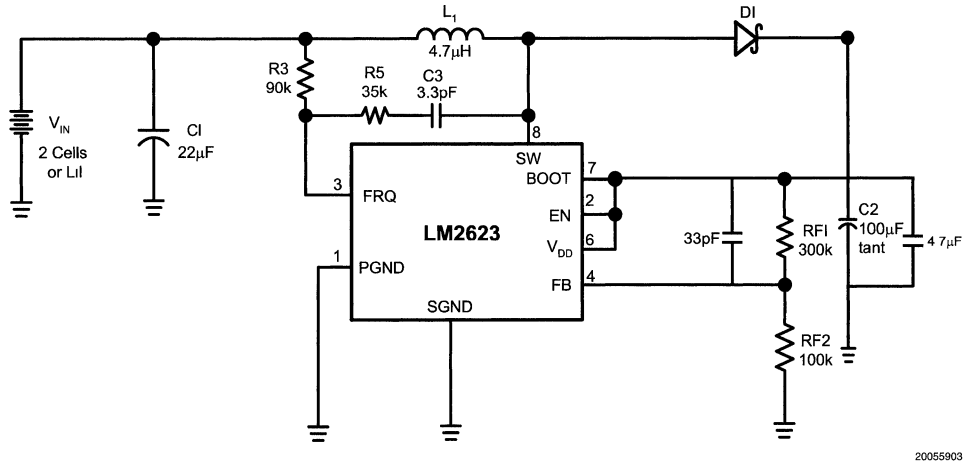


FIGURE 3. LM2623 Boost Converter Circuit with Low Ripple for Digital Cameras

The LM2623 also has the capability to handle both buck and buck/boost applications cost effectively and efficiently. This can be done with a transformer coupled circuit like the one shown in *Figure 4*. This circuit requires a duty cycle adjustment from the 17% open loop value but does not require a significant duty cycle change with voltage. For loads of 200 mA, this circuit runs 75% to 80% efficient, generating 3.3 volts over the LiIon voltage range of 2.7 to 4.5 volts. This alternative compares favorably with both the cost and efficiency of dedicated buck/boost converter products. The inherent stability of the LM2623 also comes in very handy when multiple output windings are used. Since the LM2623 operates from input voltages up to 14 volts, it can handle a significant variety of transformer coupled applications.

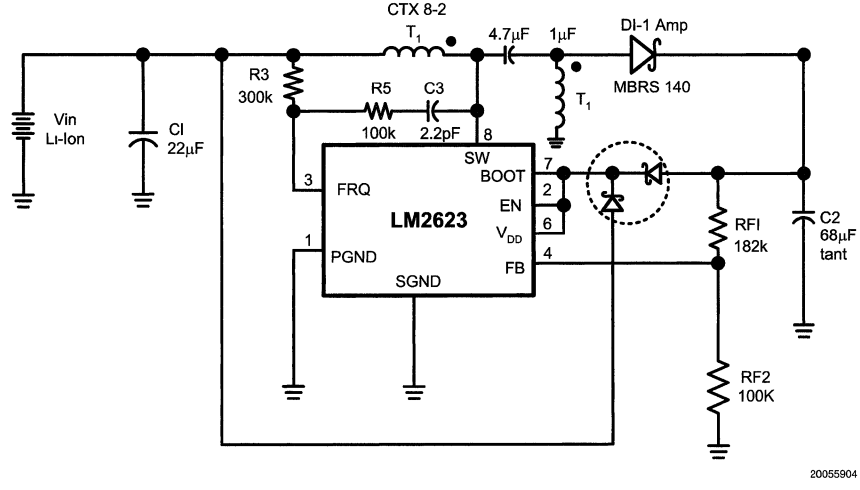


FIGURE 4. LM2623 Sepic Converter for Digital Cameras

The industry's most flexible power supply also needs to handle single cell applications. The circuit below will put out 3.3 volts at efficiencies from 75% to over 80% in the 15 ma to 150 ma load range from a single NiMH battery. It requires the adaptive duty cycle feature as well as bootstrapping of the V_{DD} and the oscillator from the output voltage. Use of a large junction Schottky diode is recommended both for efficiency and to minimize the voltage drop from the input supply to the V_{DD} pin for start-up. The 3-amp diode used in this circuit has a forward drop of about 20 millivolts under

The Ratio Adaptive Gated Oscillator (Continued)

start-up conditions. The maximum start-up voltage required at V_{DD} is 1.1 volts at 25 C. After start-up, the circuit will run down to below the minimum disposable battery voltage of .8 volts. It also runs efficiently up to 1.6 volts.

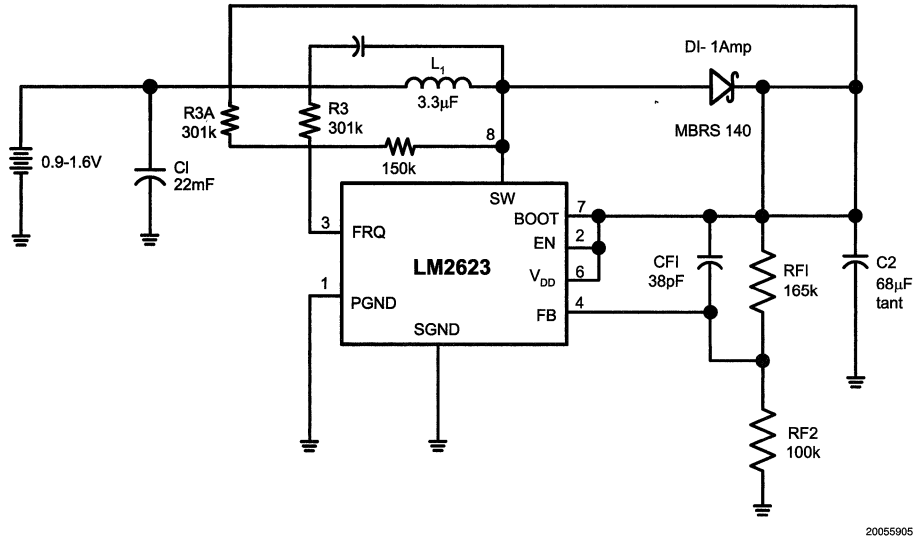


FIGURE 5. LM2623 1 Cell Converter for Pagers or Digital Cameras

The LM2623 is not the optimum solution for all portable power applications. However, the simplicity of the gated oscillator architecture makes it a very cost effective solution. Its inherent stability eliminates most of the application problems and the adjustable duty cycle makes it versatile enough for almost any portable power application. If you only want to stock one IC switching supply and minimize your expense for training and obsolescence, the LM2623 is a very good choice.

Section 10

Power Management: System Applications

Section 10 Contents

RS-232 Line Driver Power Supply

National Semiconductor
Application Brief 30

Introduction

A large segment of today's systems comply with the Electronic Industries Association (EIA) RS-232 specification for the interface between data processing and data communications equipment. Because this specification calls for the use of positive and negative signal levels, the designer quite often needs to add a dual supply to a board which can otherwise operate from a single 5V supply. The LM1578A Switching Regulator can be used to convert the already existing supply into a separate ±12V supply for powering the interface line drivers.

Circuit Description

The power supply, shown in *Figure 1*, operates from an input voltage as low as 4.2V, and delivers an output of ±12V at ±40 mA with an efficiency of better than 70%. The circuit provides a load regulation of ±1.25% (from 10% to 100% of full load) and a line regulation of ±0.08%. Other notable features include a cycle-by-cycle current limit and an output voltage ripple of less than 40 mVp-p.

A unique feature of this flyback regulator is its use of feedback from BOTH outputs. This dual feedback configuration results in a sharing of the output voltage regulation by each output so that one output is not left unregulated as in single feedback systems. In addition, since both sides are regulated, it is not necessary to use a linear regulator for output regulation.

Component Selection

The following design procedure is provided for the user who wishes to tailor the power supply circuit to fit their own specific converter application.

The feedback resistors, R2 and R3, may be selected as follows by assuming a value of 10 kΩ for R1;

$R2 = (V_{OUT} - 1V)/45.8\ \mu A = 240\ k\Omega$

$R3 = (|V_{OUT}| + 1V)/54.2\ \mu A = 240\ k\Omega$

Actually, the currents used to program the values for the feedback resistors may vary from 40 µA to 60µA, as long as their sum is equal to the 100 µA necessary to establish the 1V threshold across R1 (10 kΩ). Ideally, these currents should be equal (50 µA each) for optimal control. However, as was done here, they may be mismatched in order to use standard resistor values. This results in a slight mismatch of regulation between the two outputs.

The current limit resistor, R4, is selected by dividing the current limit threshold voltage (approximately 100 mV) by the maximum peak current level in the output switch (750 mA steady-state). For our purposes R4 = 100 mV/750 mA = 0.13Ω. A value of 0.1Ω, used here, will trip the current limit at 1A peak. A more conservative design would use 0.15Ω for this resistor.

Capacitor C1 sets the oscillator frequency according to the equation C1 = 80/f, where C1 is in nano-Farads and f is the frequency of the oscillator in kHz. This application runs at 80 kHz and used a 1 nF (1000 pF) silver-mica capacitor. The oscillator section provides a 10% deadtime each cycle to protect the output transistor.

Capacitor C2 serves as a compensation capacitor for operating the circuit in the synchronous conduction mode. That is, the output transistor will switch on each cycle, thereby eliminating the random noise spikes which occur with non-synchronous operation and are at best difficult to filter. This capacitor is optional and may be omitted if desired. If used, a value of 10 to 50 pF should be sufficient for most applications.

The choice for an output capacitor value depends primarily on the allowed output ripple voltage, ΔV_{OUT}. In most cases, the capacitor's equivalent series resistance (ESR) at the switching frequency produces more ripple voltage than does the charging and discharging of the capacitor. The capacitor should be chosen to have an ESR $\leq \Delta V_{OUT}/100$ mA, where 100 mA is approximately the greatest ripple current produces by the transformer secondary. Higher-value capacitors tend to have lower ESR; 1000 µF aluminum electrolytic was used in this circuit to assure low ESR, under 0.4Ω.

The input capacitors, C5 and C6, are used to reduce the transients that may be fedback to the main supply. Capacitor C5 is a 100 µF electrolytic and is bypassed by C6, a 0.1 µF ceramic disc.

For good efficiency, the diodes must have a low forward voltage drop and be fast switching. 1N5819 Schottky diodes work well.

Component Selection (Continued)

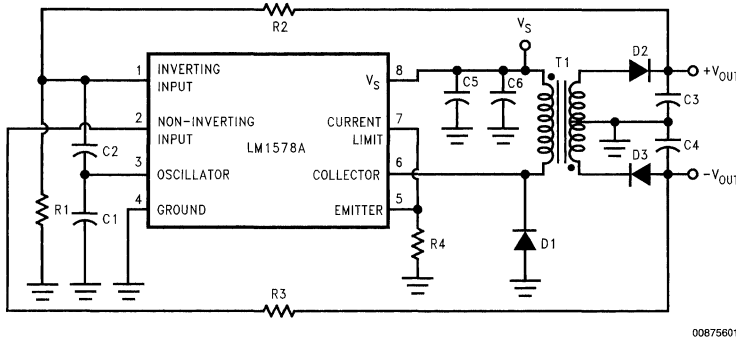


FIGURE 1. RS-232 Power Supply (See *Table 1*, Parts List)

Transformer selection should be picked for an output transistor "on" time of 0.4/f, and a primary inductance high enough to prevent the output transistor switch from ramping higher than the transistor's rating of 750 mA. Pulse Engineering (San Diego, Calif.) and Renco Electronics, Inc. (Deer Park, N.Y.) can provide further assistance in selecting the proper transformer for a specific application need. The transformer used in the power supply was a Pulse Engineering PE-64287 with turns ratio of Np:Ns:Ns = 1:1.6:1.6 and primary inductance of 50 µH.

Table 1 is a parts listing for the components used in the building of the power supply circuit.

TABLE 1. Parts List

R1 = 10 kΩ
R2 = 240 kΩ
R3 = 240 kΩ
R4 = 0.1Ω
C1 = 1000 pF
C2 = 18 pF
C3 = 220 µF
C4 = 220 µF
C5 = 100 µF
C6 = 0.1 µF
All diodes are 1N5819
T1 = Pulse Engineering PE-64287

IC Provides On-Card Regulation for Logic Circuits

National Semiconductor
Application Note 42
Robert J. Widlar

Introduction

Because of the relatively high current requirements of digital systems, there are a number of problems associated with using one centrally-located regulator. Heavy power busses must be used to distribute the regulated voltage. With low voltages and currents of many amperes, voltage drops in connectors and conductors can cause an appreciable percentage change in the voltage delivered to the load. This is aggravated further with TTL logic, as it draws transient currents many times the steady-state current when it switches.

These problems have created a considerable interest in on-card regulation, that is, to provide local regulation for the subsystems of the computer. Rough preregulation can be used, and the power distributed without excessive concern for line drops. The local regulators then smooth out the voltage variations due to line drops and absorb transients.

A monolithic regulator is now available to perform this function. It is quite simple to use in that it requires no external components. The integrated circuit has three active leads—input, output and ground—and can be supplied in standard transistor power packages. Output currents in excess of 1A can be obtained. Further, no adjustments are required to set up the output voltage, and overload protection is provided that makes it virtually impossible to destroy the regulator. The simplicity of the regulator, coupled with low-cost fabrication and improved reliability of monolithic circuits, now makes on-card regulation quite attractive.

Design Concepts

A useful on-card regulator should include everything within one package—including the power-control element, or pass transistor. The author has previously advanced arguments against including the pass transistor in an integrated circuit regulator.[1] First, there are no standard multi-lead power packages. Second, integrated circuits necessarily have a lower maximum operating temperature because they contain low-level circuitry. This means that an IC regulator needs a more massive heat sink. Third, the gross variations in chip temperature due to dissipation in the pass transistors worsen load and line regulation. However, for a logic-card regulator, these arguments can be answered effectively.

For one, if the series pass transistor is put on the chip, the integrated circuit need only have three terminals. Hence, an ordinary transistor power package can be used. The practicality of this approach depends on eliminating the adjustments usually required to set up the output voltage and limiting current for the particular application, as external adjustments require extra pins. A new solid-state reference, to be described later, has sufficiently-tight manufacturing tolerances that output voltages do not always have to be individually trimmed. Further, thermal overload protection can protect an IC regulator for virtually any set of operating conditions, making current—limit adjustments unnecessary.

Thermal protection limits the maximum junction temperature and protects the regulator regardless of input voltage, type of overload or degree of heat sinking. With an external pass transistor, there is no convenient way to sense junction temperature so it is much more difficult to provide thermal limiting. Thermal protection is, in itself, a very good reason for putting the pass transistor on the chip.

When a regulator is protected by current limiting alone, it is necessary to limit the output current to a value substantially lower than is dictated by dissipation under normal operating conditions to prevent excessive heating when a fault occurs. Thermal limiting provides virtually absolute protection for any overload condition. Hence, the maximum output current under normal operating conditions can be increased. This tends to make up for the fact that an IC has a lower maximum junction temperature than discrete transistors.

Additionally, the 5V regulator works with relatively low voltage across the integrated circuit. Because of the low voltage, the internal circuitry can be operated at comparatively high currents without causing excessive dissipation. Both the low voltage and the larger internal currents permit higher junction temperatures. This can also reduce the heat sinking required—especially for commercial-temperature-range parts.

Lastly, the variations in chip temperature caused by dissipation in the pass transistor do not cause serious problems for a logic-card regulator. The tolerance in output voltage is loose enough that it is relatively easy to design an internal reference that is much more stable than required, even for temperature variations as large as 150°C.

Circuit Description

The internal voltage reference for this logic-card regulator is probably the most significant departure from standard design techniques. Temperature-compensated zener diodes are normally used for the reference. However, these have breakdown voltages between 7V and 9V which puts a lower limit on the input voltage to the regulator. For low voltage operation, a different kind of reference is needed.

The reference in the LM109 does not use a zener diode. Instead, it is developed from the highly-predictable emitter-base voltage of the transistors. In its simplest form, the reference developed is equal to the energy-band-gap voltage of the semiconductor material. For silicon, this is 1.205V, so the reference need not impose minimum input voltage limitations on the regulator. An added advantage of this reference is that the output voltage is well determined in a production environment so that individual adjustment of the regulators is frequently unnecessary.

A simplified version of this reference is shown in *Figure 1*. In this circuit, Q_1 is operated at a relatively high current density. The current density of Q_2 is about ten times lower, and the emitter-base voltage differential (ΔV_{BE}) between the two devices appears across R_3. If the transistors have high current gains, the voltage across R_2 will also be proportional to ΔV_{BE}. Q_3 is a gain stage that will regulate the output at a voltage equal to its emitter base voltage plus the drop across R_2. The emitter base voltage of Q_3 has a negative temperature coefficient while the ΔV_{BE} component across R_2 has a positive temperature coefficient. It will be shown that the

Circuit Description (Continued)

output voltage will be temperature compensated when the sum of the two voltages is equal to the energy-band-gap voltage.

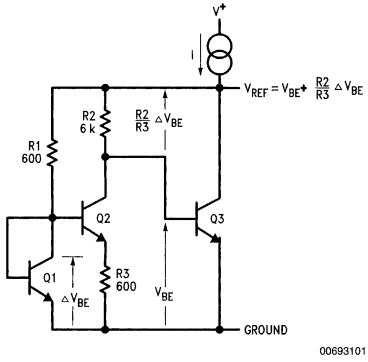


FIGURE 1. The low voltage reference in one of its simpler forms.

Conditions for temperature compensation can be derived starting with the equation for the emitter-base voltage of a transistor which is[2]

$$V_{BE} = V_{g0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\left(\frac{T}{T_0}\right) + \frac{nkT}{q} \log_e \frac{T_0}{T} + \frac{kT}{q} \log_e \frac{I_C}{I_{C0}}, \quad (1)$$

where V_{gO} is the extrapolated energy-band-gap voltage for the semiconductor material at absolute zero, q is the charge of an electron, n is a constant which depends on how the transistor is made (approximately 1.5 for double-diffused, NPN transistors), k is Boltzmann's constant, T is absolute temperature, I_C is collector current and V_{BE0} is the emitter-base voltage at T_0 and I_{C0}.

The emitter-base voltage differential between two transistors operated at different current densities is given by[3]

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{J_1}{J_2}, \quad (2)$$

where J is current density.

Referring to *Equation (1)*, the last two terms are quite small and are made even smaller by making I_C vary as absolute temperature. At any rate, they can be ignored for now because they are of the same order as errors caused by nontheoretical behavior of the transistors that must be determined empirically.

If the reference is composed of V_{BE} plus a voltage proportional to ΔV_{BE}, the output voltage is obtained by adding *Equation (1)* in its simplified form to *Equation (2)*:

$$V_{ref} = V_{g0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\left(\frac{T}{T_0}\right) + \frac{kT}{q} \log_e \frac{J_1}{J_2}. \quad (3)$$

Differentiating with respect to temperature yields

$$\frac{\partial V_{ref}}{\partial T} = -\frac{V_{g0}}{T_0} + \frac{V_{BE0}}{T_0} + \frac{k}{q} \log_e \frac{J_1}{J_2}. \quad (4)$$

For zero temperature drift, this quantity should equal zero, giving

$$V_{g0} = V_{BE0} + \frac{kT_0}{q} \log_e \frac{J_1}{J_2}. \quad (5)$$

The first term on the right is the initial emitter-base voltage while the second is the component proportional to emitter-base voltage differential. Hence, if the sum of the two are equal to the energy-band-gap voltage of the semiconductor, the reference will be temperature-compensated.

A simplified schematic for a 5V regulator is given in *Figure 2*. The circuitry produces an output voltage that is approximately four times the basic reference voltage The emitter-base voltage of Q_3, Q_4, Q_5 and Q_8 provide the negative-temperature-coefficient component of the output voltage. The voltage dropped across R_3 provides the positive-temperature-coefficient component. Q_6 is operated at a considerably higher current density than Q_7, producing a voltage drop across R_4 that is proportional to the emitter-base voltage differential of the two transistors. Assuming large current gain in the transistors, the voltage drop across R_3 will be proportional to this differential, so a temperature-compensated-output voltage can be obtained.

Circuit Description (Continued)

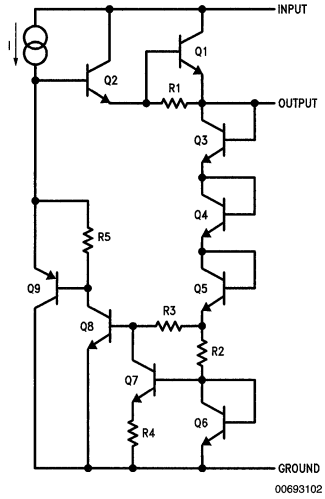


FIGURE 2. Schematic showing essential details of the 5V regulator.

In this circuit, Q_8 is the gain stage providing regulation. Its effective gain is increased by using a vertical PNP, Q_9, as a buffer driving the active collector load represented by the current source. Q_9 drives a modified Darlington output stage (Q_1 and Q_2) which acts as the series pass element. With this circuit, the minimum input voltage is not limited by the voltage needed to supply the reference. Instead, it is determined by the output voltage and the saturation voltage of the Darlington output stage.

Figure 3 shows a complete schematic of the LM109, 5V regulator. The ΔV_{BE} component of the output voltage is developed across R_8 by the collector current of Q_7. The emitter-base voltage differential is produced by operating Q_4 and Q_5 at high current densities while operating Q_6 and Q_7 at much lower current levels. The extra transistors improve tolerances by making the emitter-base voltage differential larger. R_3 serves to compensate the transconductance[4] of Q_5, so that the ΔV_{BE} component is not affected by changes in the regular output voltage or the absolute value of components.

The voltage gain for the regulating loop is provided by Q_{10}, with Q_9 buffering its input and Q_{11} its output. The emitter base voltage of Q_9 and Q_{10} is added to that of Q_{12} and Q_{13} and the drop across R_8 to give a temperature-compensated, 5V output. An emitter-base-junction capacitor, C_1, frequency compensates the circuit so that it is stable even without a bypass capacitor on the output.

The active collector load for the error amplifier is Q_{17}. It is a multiple-collector lateral PNP[4]. The output current is essentially equal to the collector current of Q_2, with current being supplied to the zener diode controlling the thermal shutdown, D_2, by an auxiliary collector. Q_1 is a collector FET[4] that, along with R_1, insures starting of the regulator under worst-case conditions.

The output current of the regulator is limited when the voltage across R_{14} becomes large enough to turn on Q_{14}. This insures that the output current cannot get high enough to cause the pass transistor to go into secondary breakdown or damage the aluminum conductors on the chip. Further, when the voltage across the pass transistor exceeds 7V, current through R_{15} and D_3 reduces the limiting current, again to minimize the chance of secondary breakdown. The performance of this protection circuitry is illustrated in *Figure 4*.

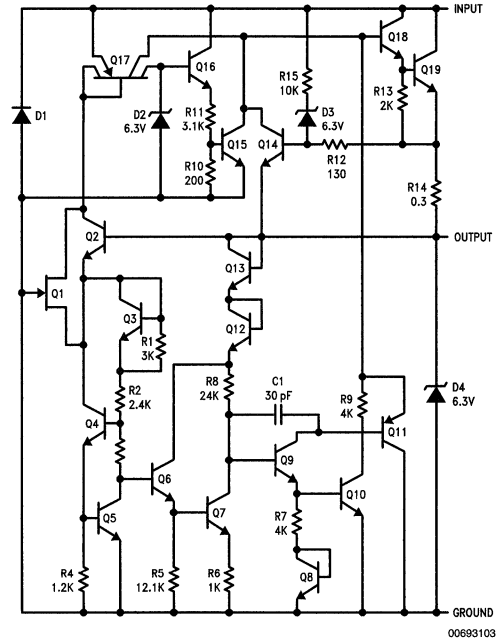


FIGURE 3. Detailed schematic of the regulator.

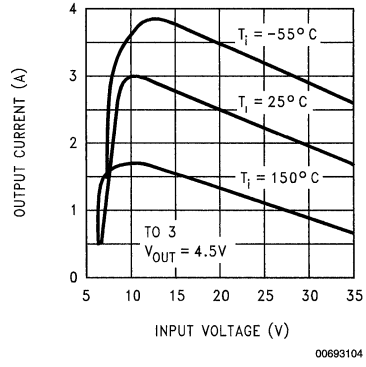


FIGURE 4. Current-limiting characteristics.

Even though the current is limited, excessive dissipation can cause the chip to overheat. In fact, the dominant failure mechanism of solid state regulators is excessive heating of the semiconductors, particularly the pass transistor. Thermal protection attacks the problem directly by putting a temperature regulator on the IC chip. Normally, this regulator is

Circuit Description (Continued)

biased below its activation threshold; so it does not affect circuit operation. However, if the chip approaches its maximum operating temperature, for any reason, the temperature regulator turns on and reduces internal dissipation to prevent any further increase in chip temperature.

The thermal protection circuitry develops its reference voltage with a conventional zener diode, D_2. Q_{16} is a buffer that feeds a voltage divider, delivering about 300 mV to the base of Q_{15} at 175°C. The emitter-base voltage, Q_{15}, is the actual temperature sensor because, with a constant voltage applied across the junction, the collector current rises rapidly with increasing temperature.

Although some form of thermal protection can be incorporated in a discrete regulator, IC's have a distinct advantage: the temperature sensing device detects increases in junction temperature within milliseconds. Schemes that sense case or heat-sink temperature take several seconds, or longer. With the longer response times, the pass transistor usually blows out before thermal limiting comes into effect.

Another protective feature of the regulator is the crowbar clamp on the output. If the output voltage tries to rise for some reason, D_4 will break down and limit the voltage to a safe value. If this rise is caused by failure of the pass transistor such that the current is not limited, the aluminum conductors on the chip will fuse, disconnecting the load. Although this destroys the regulator, it does protect the load from damage. The regulator is also designed so that it is not damaged in the event the unregulated input is shorted to ground when there is a large capacitor on the output. Further, if the input voltage tries to reverse, D_1 will clamp this for currents up to 1A.

The internal frequency compensation of the regulator permits it to operate with or without a bypass capacitor on the output. However, an output capacitor does improve the transient response and reduce the high frequency output impedance. A plot of the output impedance in *Figure 5* shows that it remains low out to 10 kHz even without a capacitor. The ripple rejection also remains high out to 10 kHz, as shown in *Figure 6*. The irregularities in this curve around 100 Hz are caused by thermal feedback from the pass transistor to the reference circuitry. Although an output capacitor is not required, it is necessary to bypass the input of the regulator with at least a 0.22 µF capacitor to prevent oscillations under all conditions.

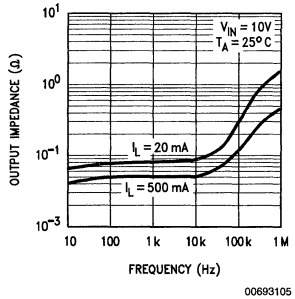


FIGURE 5. Plot of output impedance as a function of frequency.

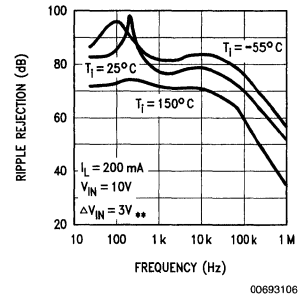


FIGURE 6. Ripple rejection of the regulator.

Figure 7 is a photomicrograph of the regulator chip. It can be seen that the pass transistors, which must handle more than 1A, occupy most of the chip area. The output transistor is actually broken into segments. Uniform current distribution is insured by also breaking the current limit resistor into segments and using them to equalize the currents. The overall electrical performance of this IC is summarized in *Table 1*.

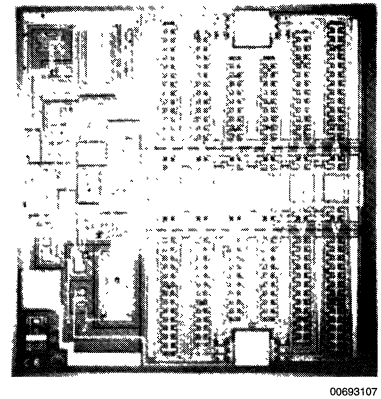


FIGURE 7. Photomicrograph of the regulator shows that high current pass transistor (right) takes more area than control circuitry (left).

TABLE 1. Typical Characteristics of the Logic-Card Regulator: T_A = 25°C

Parameter	Conditions	Typ
Output Voltage		5.0V
Output Current		1.5A
Output Resistance		0.03Ω
Line Regulation	7.0V ≤ V_{IN} ≤ 35V	0.005%/V
Temperature Drift	−55°C ≤ T_A ≤ 125°C	0.02%/°C
Minimum Input Voltage	I_{OUT} = 1A	6.5V
Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz	40 µV

Circuit Description (Continued)

TABLE 1. Typical Characteristics of the Logic-Card Regulator: T_A = 25°C (Continued)

Parameter	Conditions	Typ
Thermal Resistance	LM109H (TO-5)	15°C/W
Junction to Case	LM109K (TO-3)	3°C/W

Applications

Because it was designed for virtually foolproof operation and because it has a singular purpose, the LM109 does not require a lot of application information, as do most other linear circuits. Only one precaution must be observed: it is necessary to bypass the unregulated supply with a 0.22 µF capacitor, as shown in *Figure 8*, to prevent oscillations that can cause erratic operation. This, of course, is only necessary if the regulator is located on appreciable distance from the filter capacitors on the output of the dc supply.

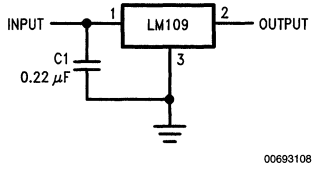


FIGURE 8. Fixed 5V regulator

Although the LM109 is designed as a fixed 5V regulator, it is also possible to use it as an adjustable regulator for higher output voltages. One circuit for doing this is shown in *Figure 9*.

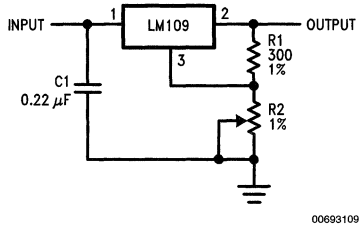


FIGURE 9. Using the LM109 as an adjustable-output regulator.

The regulated output voltage is impressed across R_1, developing a reference current. The quiescent current of the regulator, coming out of the ground terminal, is added to this. These combined currents produce a voltage drop across R_2 which raises the output voltage. Hence, any voltage above 5V can be obtained as long as the voltage across the integrated circuit is kept within ratings.

The LM109 was designed so that its quiescent current is not greatly affected by variations in input voltage, load or temperature. However, it is not completely insensitive, as shown in *Figures 10, 11*, so the changes do affect regulation somewhat. This tendency is minimized by making the reference current though R_1 larger than the quiescent current. Even so, it is difficult to get the regulation tighter than a couple percent.

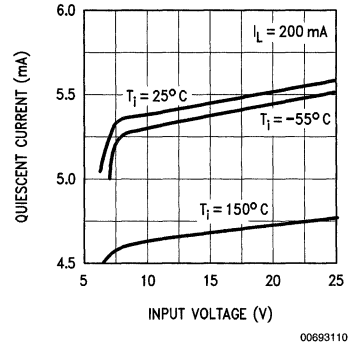


FIGURE 10. Variation of quiescent current with input voltage at various temperatures.

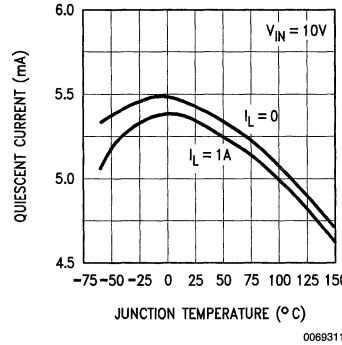


FIGURE 11. Variation of quiescent current with temperature for various load currents.

The LM109 can also be used as a current regulator as is shown in *Figure 12*. The regulated output voltage is impressed across R_1, which determines the output current. The quiescent current is added to the current through R_1, and this puts a lower limit of about 10 mA on the available output current.

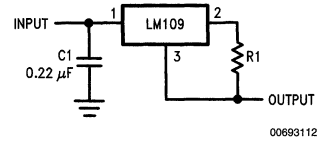


FIGURE 12. Current regulator.

The increased failure resistance brought about by thermal overload protection make the LM109 attractive as the pass

Applications (Continued)

transistor in other regulator circuits. A precision regulator that employs the IC thusly is shown in *Figure 13.* An operational amplifier compares the output voltage with the output voltage of a reference zener. The op amp controls the LM109 by driving the ground terminal through an FET.

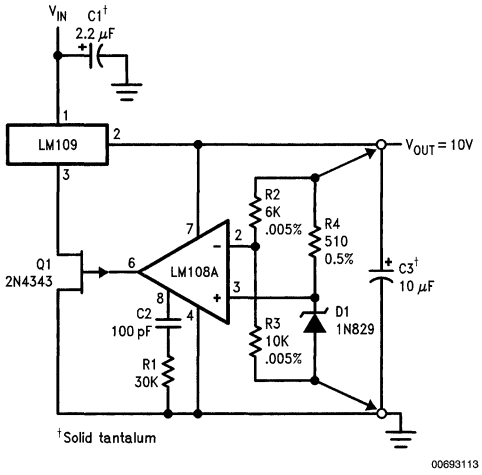


FIGURE 13. High stability regulator.

The load and line regulation of this circuit is better than 0.001%. Noise, drift and long term stability are determined by the reference zener, D_1. Noise can be reduced by inserting 100 kΩ, 1% resistors in series with both inputs of the op amp and bypassing the non-inverting input to ground. A 100 pF capacitor should also be included between the output and the inverting input to prevent frequency instability. Temperature drift can be reduced by adjusting R_4, which determines the zener current, for minimum drift. For best performance, remote sensing directly to the load terminals, as shown in the diagram, should be used.

Conclusions

The LM109 performs a complete regulation function on a single silicon chip, requiring no external components. It makes use of some unique advantages of monolithic construction to achieve performance advantages that cannot be obtained in discrete-component circuits. Further, the low cost of the device suggests its use in applications where single-point regulation could not be justified previously.

Thermal overload protection significantly improves the reliability of an IC regulator It even protects the regulator for unforseen fault conditions that may occur in field operation. Although this can be accomplished easily in a monolithic regulator, it is usually not completely effective in a discrete or hybrid device.

The internal reference developed for the LM109 also advances the state of the art for regulators. Not only does it provide a low voltage, temperature-compensated reference for the first time, but also it can be expected to have better long term stability than conventional zeners. Noise is inherently much lower, and it can be manufactured to tighter tolerances.

Reference

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2. J.S. Brugler, *"Silicon Transistor Biasing for Linear Collector Current Temperature Dependence," IEEE Journal of Solid State Circuits*, pp. 57–58, June, 1967.
3. R.J. Widlar, *"Some Circuit Design Techniques for Linear Integrated Circuits,"* IEEE *Trans. on Circuit Theory*, Vol. XII, pp. 586–590, December, 1965.
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Applications for an Adjustable IC Power Regulator

National Semiconductor
Application Note 178
Robert J. Widlar

A new 3-terminal adjustable IC power regulator solves many of the problems associated with older, fixed regulators. The LM117, a 1.5A IC regulator is adjustable from 1.2V to 40V with only 2 external resistors. Further, improvements are made in performance over older regulators. Load and line regulation are a factor of 10 better than previous regulators. Input voltage range is increased to 40V and output characteristics are fully specified for load of 1.5A. Reliability is improved by new overload protection circuitry as well as *100% burn-in* of all parts. The table below summarizes the typical performance of the LM117.

TABLE 1.

Output Voltage Range	1.25V–40V
Line Regulation	0.01%/V
Load Regulation I_L = 1.5A	0.1%
Reference Voltage	1.25V
Adjustment Pin Currrent	50 µA
Minimum Load Current (Quiescent Current)	3.5 mA
Temperature Stability	0.01%/°C
Current Limit	2.2A
Ripple Rejection	80 dB

The overload protection circuitry on the LM117 includes current limiting, safe-area protection for the internal power transistor and thermal limiting. The current limit is set at 2.2A and, unlike presently available positive regulators, remains relatively constant with temperature. Over a −55°C to +150°C temperature range, the current limit only shifts about 10%.

At high input-to-output voltage differentials the safe-area protection decreases the current limit. With the LM117, full output current is available to 15V differential and, even at 40V, about 400 mA is available. With some regulators, the output will shut completely off when the input-to-output differential goes above 30V, possibly causing start-up problems. Finally, the thermal limiting is always active and will protect the device even if the adjustment terminal should become accidentally disconnected.

Since the LM117 is a floating voltage regulator, it sees only the input-to-output voltage differential. This is of benefit, especially at high output voltage. For example, a 30V regulator nominally operating with a 38V input can have 70V input transient before the 40V input-to-output rating of the LM117 is exceeded.

Basic Operation

The operation of how a 3-terminal regulator is adjusted can be easily understood by referring to *Figure 1*, which shows a functional circuit. An op amp, connected as a unity gain buffer, drives a power Darlington. The op amp and biasing circuitry for the regulator is arranged so that all the quiescent current is delivered to the regulator output (rather than ground) eliminating the need for a separate ground terminal. Further, all the circuitry is designed to operate over the 2V to 40V input-to-output differential of the regulator.

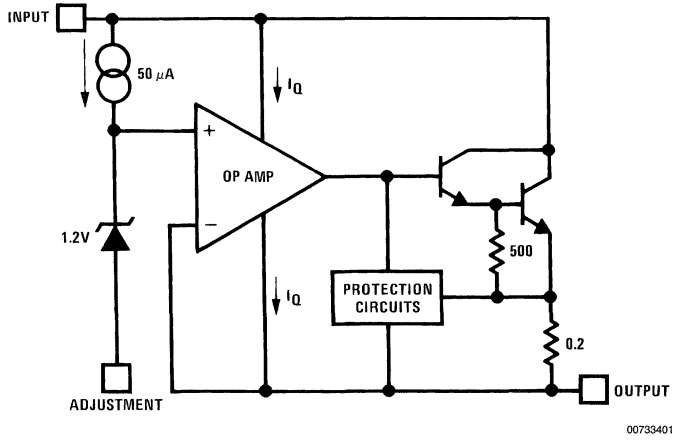


FIGURE 1. Functional Schematic of the LM117

A 1.2V reference voltage appears inserted between the non-inverting input of the op amp and the adjustment terminal. About 50 µA is needed to bias the reference and this current comes out of the adjustment terminal. In operation, the output of the regulator is the voltage of the adjustment terminal plus 1.2V. If the adjustment terminal is grounded, the device acts as a 1.2V regulator. For higher output voltages, a divider R1 and R2 is connected from the output to

Basic Operation (Continued)

ground as is shown in *Figure 2*. The 1.2V reference across resistor R1 forces 10 mA of current to flow. This 10 mA then flows through R2, increasing the voltage at the adjustment terminal and therefore the output voltage. The output voltage is given by:

$$V_{OUT} = 1.2V \times \left(1 + \frac{R2}{R1}\right) + 50\ \mu A\ R2$$

The 50 µA biasing current is small compared to 5 mA and causes only a small error in actual output voltages Further, it is extremely well regulated against line voltage or load current changes so that it contributes virtually no error to dynamic regulation. Of course, programming currents other than 10 mA can be used depending upon the application.

Since the regulator is floating, all the quiescent current must be absorbed by the load. With too light of a load, regulation is impaired Usually, a 5 mA programming current is sufficient; however, worst case minimum load for commercial grade parts requires a minimum load of 10 mA. The minimum load current can be compared to the quiescent current of standard regulators.

Applications

An adjustable lab regulator using the LM117 is shown in *Figure 2* and has a 1.2V to 25V output range. A 10 mA program current is set by R1 while the output voltage is set by R2 Capacitor C1 is optional to improve ripple rejection so that 80 dB is obtained at any output voltage. The diode, although not necessary in this circuit since the output is limited to 25V, is needed with outputs over 25V to protect against the capacitors discharging through low current nodes in the LM117 when the input or output is shorted.

The programming current is constant and can be used to bias other circuitry, while the regulator is used as the power supply for the system. In *Figure 3*, the LM117 is used as a 15V regulator while the programming current powers an LM127 zener reference. The LM129 is an IC zener with less than 1Ω dynamic impedance and can operate over a range of 0.5 mA to 15 mA with virtually no change in performance.

Another example of using the programming current is shown in *Figure 4* where the output setting resistor is tapped to provide multiple output voltage to op amp buffers. An additional transistor is included as part of the overload protection. When any of the outputs are shorted, the op amp will current limit and a voltage will be developed across its inputs. This will turn "ON" the transistor and pull down the adjustment terminal of the LM117, causing all outputs to decrease, minimizing possible damage to the rest of the circuitry.

Ordinary 3-terminal regulators are not especially attractive for use as precision current regulators. Firstly, the quiescent current can be as high as 10 mA, giving at least 1% error at 1A output currents, and more error at lower currents. Secondly, at least 7V is needed to operate the device. With the LM117, the only error current is 50 µA from the adjustment terminal, and only 4.2V is needed for operation at 1.5A or 3.2V at 0.5A. A simple 2-terminal current regulator is shown in *Figure 5* and is usable anywhere from 10 mA to 1.5A.

Figure 6 shows an adjustable current regulator in conjunction with the voltage regulator from *Figure 2* to make constant voltage/constant current lab-type supply. Current sensing is done across R1, a 1Ω resistor, while R2 sets the current limit point. When the wiper of R2 is connected, the 1Ω sense resistor current is regulated at 1.2A. As R2 is adjusted, a portion of the 1.2V reference of the LM117 is cancelled by the drop across the pot, decreasing the current limit point. At low output currents, current regulation is degraded since the voltage across the 1Ω sensing resistor becomes quite low. For example, with 50 mA output current, only 50 mV is dropped across the sense resistor and the supply rejection of the LM117 will limit the current regulation

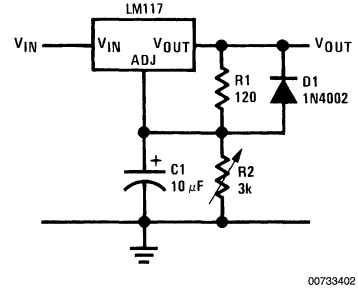


FIGURE 2. Basic Voltage Regulator

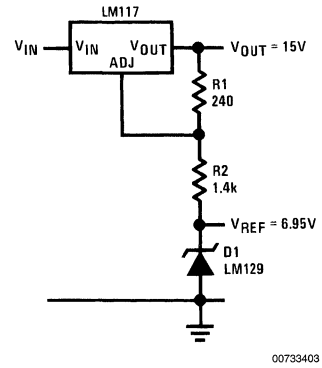


FIGURE 3. Regulator and Voltage Reference

to about 3% for a 40V change across the device. An alternate current regulator is shown in *Figure 7* using an additional LM117 to provide the reference, rather than an LM113 diode. Both current regulators need a negative supply to operate down to ground.

Figure 8 shows a 2-wire current transmitter with 10 mA to 50 mA output current for a 1V input. An LM117 is biased as a 10 mA current source to set the minimum current and provide operating current for the control circuitry. Operating off the 10 mA is an LM108 and an LM129 zener. The zener provides a common-mode voltage for operation of the LM108 as well as a 6.9V reference, if needed. Input signals are impressed across R3, and the curent through R3 is delivered to the output of the regulator by Q1 and Q2. For a 25Ω resistor, this gives a 40 mA current change for a 1V input. This circuit can be used in 4 mA to 20 mA applications, but the LM117 must be selected for low quiescent current. Minimum operating voltage is about 12V.

Applications (Continued)

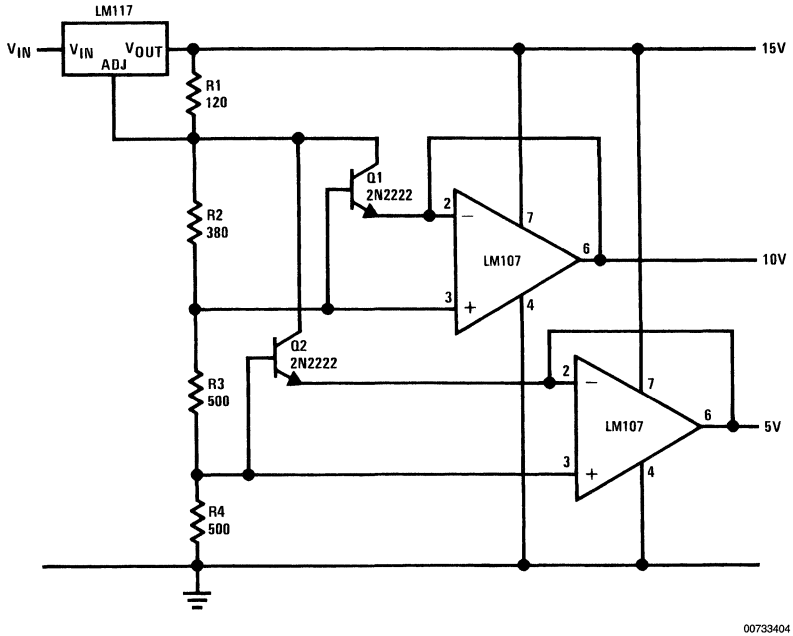
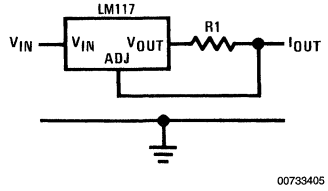


FIGURE 4. Regulator with Multiple Outputs



$$I_{OUT} = \frac{1.25V}{R1}$$

$10\ mA \leq I_{OUT} \leq 1.5A$

FIGURE 5. 2-Terminal Current Regulator

Applications (Continued)

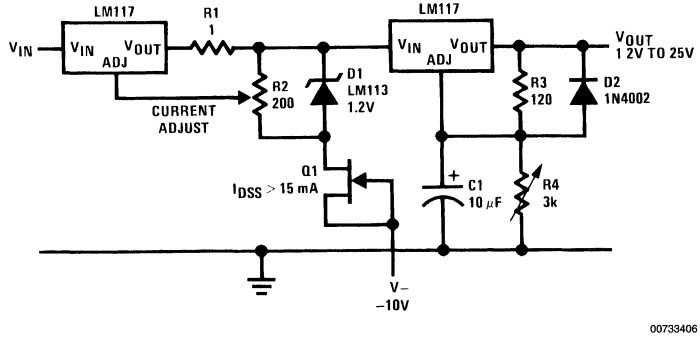


FIGURE 6. Adjustable Regulator. Constant Voltage/Constant Current, 10 mA to 1.2A

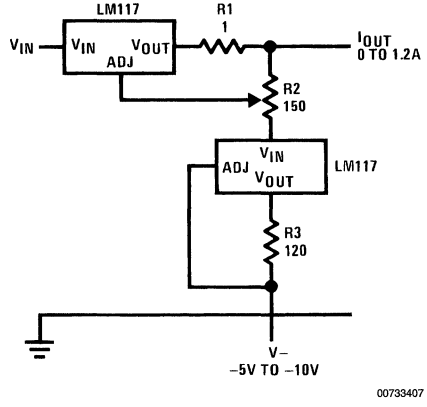


FIGURE 7. Adjustable Current Regulator

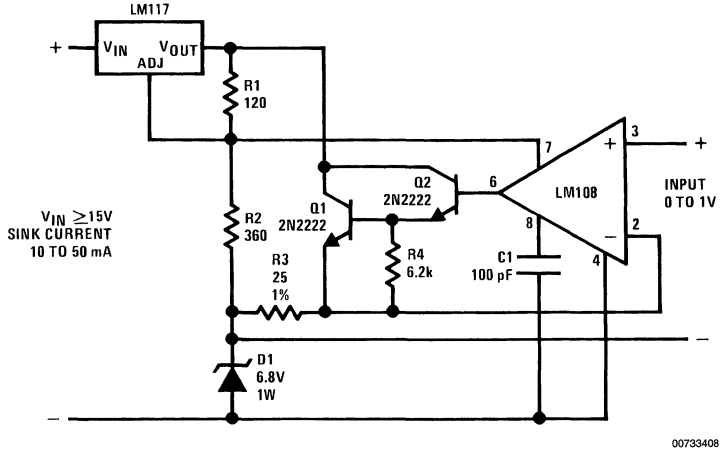


FIGURE 8. 10 mA to 50 mA 2-Wire Current Transmitter

Improving Power Supply Reliability with IC Power Regulators

National Semiconductor
Application Note 182
Robert J. Widlar

Three-terminal IC power regulators include on-chip overload protection against virtually any normal fault condition. Current limiting protects against short circuits fusing the aluminum interconnects on the chip. Safe-area protection decreases the available output current at high input voltages to insure that the internal power transistor operates within its safe area. Finally, thermal overload protection turns off the regulator at chip temperatures of about 170°C, preventing destruction due to excessive heating. Even though the IC is fully protected against normal overloads, careful design must be used to insure reliable operation in the system.

Short Circuits Can Overload the Input

The IC is protected against short circuits, but the value of the on-chip current limit can overload the input rectifiers or transformer. The on-chip current limit is usually set by the manufacturer so that with worst-case production variations and operating temperature the device will still provide rated output current. Older types of regulators, such as the LM309, LM340 or LM7800 can have current limits of 3 times their rated output current.

The current limit circuitry in these devices uses the turn-on voltage of an emitter-base junction of a transistor to set the current limit. The temperature coefficient of this junction combined with the temperature coefficient of the internal resistors gives the current limit a −0.5%/°C temperature coefficient. Since devices must operate and provide rated current at 150°C, the 25°C current limit is 120% higher than typical. Production variations will add another ±20% to initial current limit tolerance so a typical 1A part may have a 3A current limit at 25°C. This magnitude of overload current can blow the input transformer or rectifiers if not considered in the initial design—even though it does not damage the IC.

One way around this problem (other than fuses) is by the use of minimum size heat sinks. The heat sink is designed for only normal operation. Under overload conditions, the device (and heat sink) are allowed to heat up to the thermal shut-down temperature. When the device shuts down, loading on the input is reduced.

Newer regulators have improved current limiting circuitry. Devices like the LM117 adjustable regulator, LM123, 3A, 5V logic regulator or the LM120 negative regulators have a relatively temperature-stable current limit. Typically these devices hold the current limit within ±10% over the full −55°C to +150°C operating range. A device rated for 1.5A output will typically have a 2.2A current limit, greatly easing the problem of input overloads.

Many of the older IC regulators can oscillate when in current limit. This does not hurt the regulator and is mostly dependent upon input bypassing capacitors. Since there is a large variability between regulator types and manufacturers, there is no single solution to eliminating oscillations. Generally, if oscillations cause other circuit problems, either a solid tantalum input capacitor or a solid tantalum in series with 5Ω to 10Ω will cure the problem. If one doesn't work, try the other.

Start-up problems can occur from the current limit circuitry too. At high input-ouput differentials, the current limit is decreased by the safe-area protection. In most regulators the decrease is linear, and at input-output voltages of about 30V the output current can decrease to zero. Normally this causes no problem since, when the regulator is initially powered, the output increases as the input increases. If such a regulator is running with, for example, 30V input and 15V output and the output is momentarily shorted, the input-output differential increases to 30V and available output current is zero. Then the output of the regulator stays at zero even if the short is removed. Of course, if the input is turned OFF, then ON, the regulator will come up to operating voltage again. The LM117 is the only regulator which is designed with a new safe-area protection circuit so output current does not decrease to zero, even at 40V differential.

This type of start-up problem is particularly load dependent. Loads to a separate negative supply or constant-current devices are among the worst. Another, usually overlooked, load is pilot lights. Incandescent bulbs draw 8 times as much current when cold as when operating. This severely adds to the load on a regulator, and may prevent turn-on. About the only solutions are to use an LM117 type device, or bypass the regulator with a resistor from input to output to supply some start-up current to the load. Resistor bypassing will not degrade regulation if, under worst-case conditions of maximum input voltage and minimum load current, the regulator is still delivering output current rather than absorbing current from the resistor. *Figure 1* shows the output current of several different regulators as a function of output voltage and temperature.

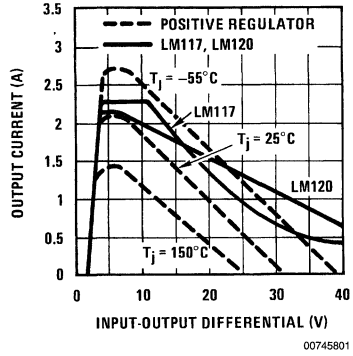


FIGURE 1. Comparison of LM117 Current Limit with Older Positive Regulator

When a positive regulator (except for the LM117) is loaded to a negative supply, the problem of start-up can be doubly bad. First, there is the problem of the safe-area protection as mentioned earlier. Secondly, the internal circuitry cannot supply much output current when the output pin is driven more negative than the ground pin of the regulator. Even with low input voltages, some positive regulators will not start when loaded by 50 mA to a negative supply. Clamping the output to ground with a germanium or Schottky diode usually solves this problem. Negative regulators, because of different internal circuitry, do not suffer from this problem.

Diodes Protect Against Capacitor Discharge

It is well recognized that improper connections to a 3-terminal regulator will cause its destruction. Wrong polarity inputs or driving current into the output (such as a short between a 5V and 15V supply) can force high currents through small area junctions in the IC, destroying them. However, improper polarities can be applied accidently under many normal operating conditions, and the transient condition is often gone before it is recognized.

Perhaps the most likely sources of transients are external capacitors used with regulators. *Figure 2* shows the discharge path for different capacitors used with a positive regulator. Input capacitance, C1, will not cause a problem under any conditions. Capacitance on the ground pin (or adjustment pin is the case of the LM117) can discharge through 2 paths which have low current junctions.

If the output is shorted, C2 will discharge through the ground pin, possibly damaging the regulator. A reverse-biased diode, D2, diverts the current around the regulator, protecting it. If the input is shorted, C3 can discharge through the output pin, again damaging the regulator. Diode D1 protects against C3, preventing damage. Also, with both D1 and D2 in the circuit, when the input is shorted, C2 is discharged through both diodes, rather than the ground pin.

In general, these protective diodes are a good idea on all positive regulators. At higher output voltages, they become more important since the energy stored in the capacitors is larger. With negative regulators and the LM117, there is an inernal diode in parallel with D1 from output-to-input, eliminating the need for an external diode if the output capacitor is less than 25 µF.

Another transient condition which has been shown to cause problems is momentary loss of the ground connection. This charges the output capacitor to the unregulated input voltage minus a 1—2V drop across the regulator. If the ground is then connected, the output capacitor, C3, discharges through the regulator output to the ground pin, destroying it. In most cases, this problem occurs when a regulator (or card) is plugged into a powered system and the input pin is connected before the ground. Control of the connector configuration, such as using 2 ground pins to insure ground is connected first, is the best way of preventing this problem. Electrical protection is cumbersome. About the only way to protect the regulator electrically is to make D2 a power zener 1V to 2V above the regulator voltage and include 10Ω to 50Ω in the ground lead to limit the current.

Low Operating Temperature Increases Life

Like any semiconductor circuit, lower operating temperature improves reliability. Operating life decreases at high junction temperatures. Although many regulators are rated to meet specifications at 150°C, it is not a good idea to design for continuous operation at that temperature. A reasonable maximum operating temperature would be 100°C for epoxy packaged devices and 125°C for hermetically sealed (TO-3) devices. Of course, the lower the better, and decreasing the above temperatures by 25°C for normal operation is still reasonable.

Another benefit of lowered operating temperatures is improved power cycle life for low cost soft soldered packages. Many of today's power devices (transistors included) are assembled using a TO-220 or TO-3 aluminum soft solder system. With temperature excursions, the solder work-hardens and with enough cycles the solder will ultimately fail. The larger the temperature change, the sooner failure will occur. Failures can start at about 5000 cycles with a 100°C temperature excursion. This necessitates, for example, either a large heat sink or a regulator assembled with a hard solder, such as steel packages, for equipment that is continuously cycled ON and OFF.

Thermal Limiting Gives Absolute Protection

Without thermal overload protection, the other protection circuitry will only protect against short term overloads. With thermal limiting, a regulator is not destroyed by long time short circuits, overloads at high temperatures or inadequate heat sinking. In fact, this overload protection makes the IC regulator tolerant of virtually any abuse, with the possible exception of high-voltage transients, which are usually filtered by the capacitors in most power supplies.

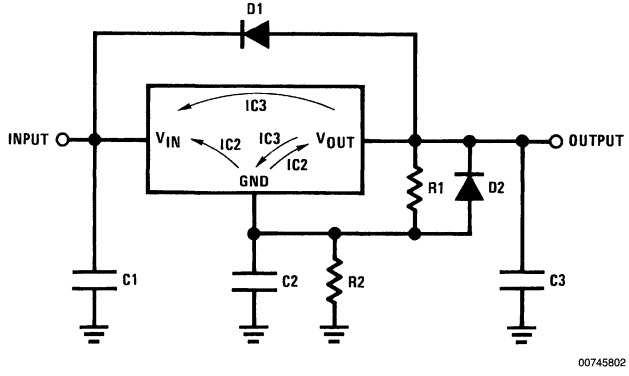


FIGURE 2. Positive Regulator with Diode Protection Against Transient Capacitor Discharge

Thermal Limiting Gives Absolute Protection (Continued)

One problem with thermal limiting is testing. With a 3-terminal regulator, short-circuit protection and safe-area protection are easily measured electrically. For thermal limiting to operate properly, the electrical circuitry on the IC must function and the IC chip must be well die-attached to the package so there are no hot spots. About the only way to insure that thermal limiting works is to power the regulator, short the output, and let it cook. If the regulator still works after 5 minutes (or more) the thermal limit has protected the regulator.

This type of testing is time consuming and expensive for the manufacturer so it is not always done. Some regulators, such as the LM117, LM137, LM120 and LM123, do receive an electrical burn-in in thermal shutdown as part of their testing. This insures that the thermal limiting works as well as reducing infant mortality. If it is probable that a power supply will have overloads which cause the IC to thermally limit, testing the regulator is in order.

An Electronic Watt-Watt-Hour Meter

National Semiconductor
Application Note 265
Robert J. Widlar

The continued emphasis on energy conservation has forced designers to consider the power consumption and efficiency of their products. While equipment for the industrial market must be designed with attention towards these factors, the consumer area is even more critical. The high cost of electricity has promoted a great deal of interest in the expense of powering various appliances. The watt-watt-hour meter outlined in *Figure 1* allows the designer to easily determine power consumption of any 115V AC powered device. The extremely wide dynamic range of the design allows measurement of loads ranging from 0.1W to 2000W.

Conceptually, the instrument is quite straightforward (*Figure 1*). The device to be monitored is plugged into a standard 110V AC outlet which is mounted on the front panel of the instrument. The AC line voltage across the monitored load is divided down and fed via an op amp to one input of a 4-quadrant analog multiplier. The current through the load is determined by the voltage across a low resistance shunt. Even at 20A the shunt "steals" only 133 mV, eliminating the inaccuracies a high resistance current shunt would contribute. This single shunt is used for all ranges, eliminating the need to switch in high impedance shunts to obtain adequate signal levels on the high sensitivity scales.

This provision is made possible by low uncertainty in the current amplifier, whose output feeds the other multiplier input. Switchable gain at the current amplifier allows decade setting of instrument sensitivity. The instantaneous power product (E x I) drawn by the load is represented by the multiplier output. Because the multiplier is a 4-quadrant type, its output will be a true reflection of load power consumption, regardless of the phase relationship between voltage and current in the load. Because the multiplier and its associated amplifiers are connected directly to the AC line, they must be driven from a floating power supply. In addition, their outputs cannot be safely monitored with grounded test equipment, such as strip chart recorders. For this reason, the multiplier output drives an isolation amplifier which operates at unity gain but has no galvanic connection between its input and output terminals.

This feature is accomplished through pulse amplitude modulation techniques in conjunction with a small transformer, which provides isolation. The isolated amplifier output is ground referenced and may safely be connected to any piece of test equipment. This output is filtered to provide a strip chart output and drive the readout meter, both of which indicate load power consumption. The isolation amplifier output also biases a voltage-to-frequency converter which combines with digital counters to form a digital integrator. This allows power over time (watt-hours) to be integrated and displayed. Varying the divide ratio of the counters produces ranging of the watt-hour function.

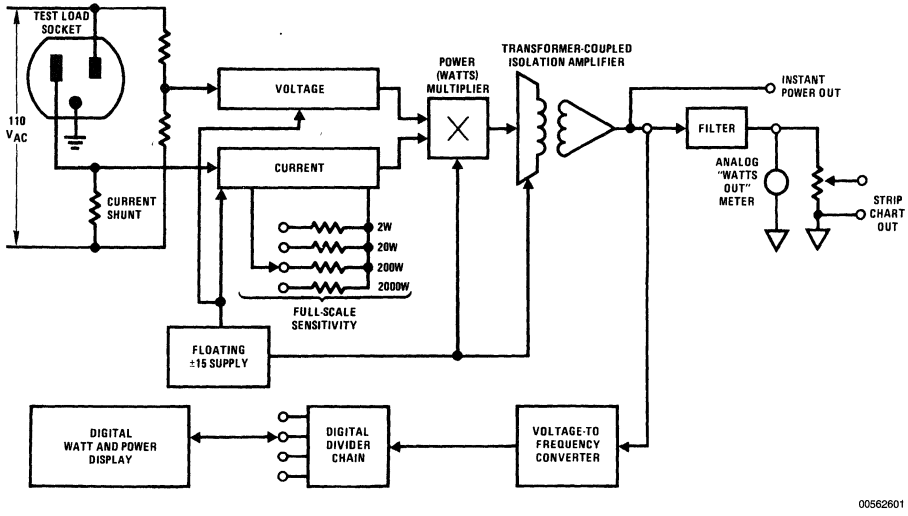
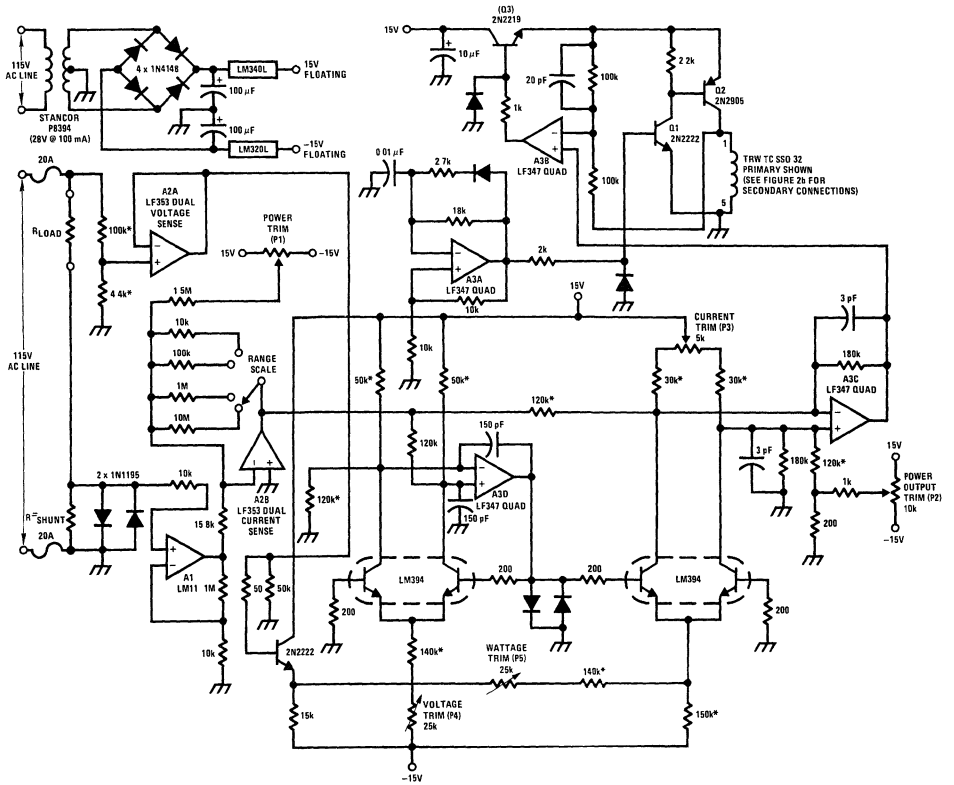


FIGURE 1.



Note 1: All diodes 1N4148

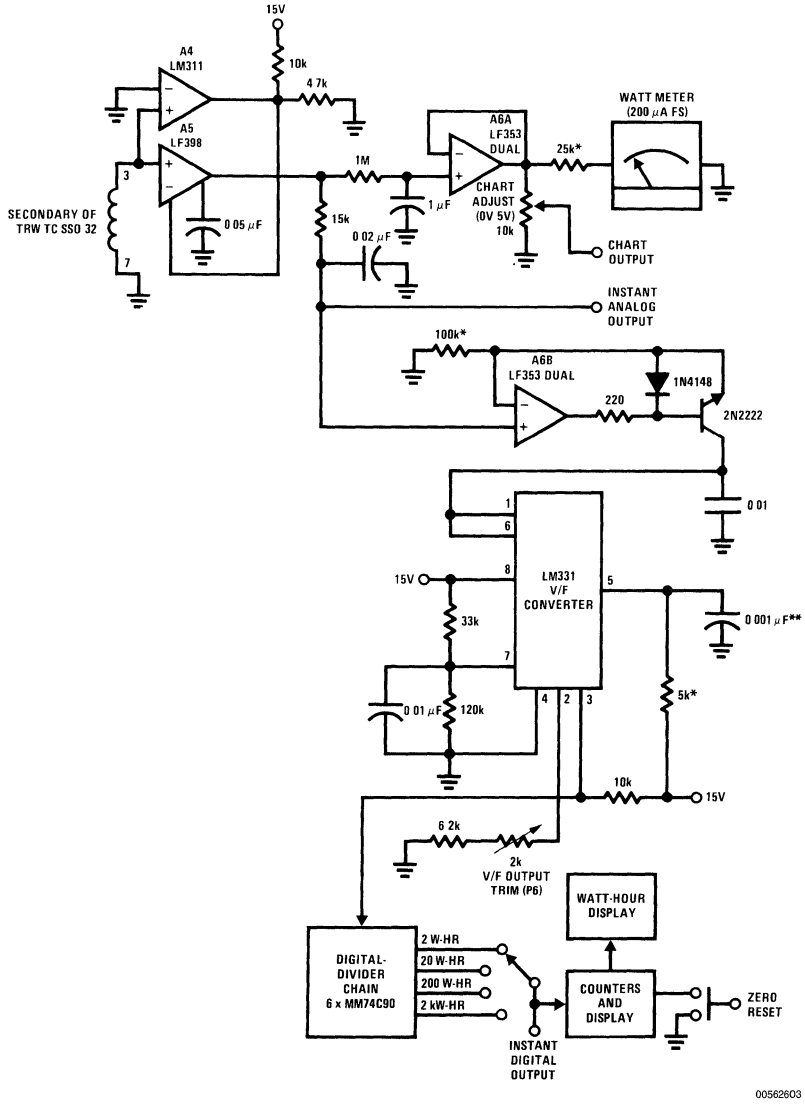
Note 2: ⏚ floating ground connected to neutral side of 110 VAC line

Note 3: R#=G E current shunt 50–140034NDAA

Note 4: Circuit power from ±15V floating supply shown in schematic

Note 5: *Resistors are 1% metal film types

FIGURE 2. Floating Half of Circuit is Connected Directly to the AC Line. Always Use Caution when Working with this Circuitry.



Note 6: *Resistors are 1% metal film types

Note 7: **Polystyrene capacitor

Note 8: DO NOT connect ( ) ground of this half of circuit to (C) ground of *Figure 2*

Note 9: ±15V power must come from a source other than floating supply of *Figure 2*

Note 10: *Figure 2* and *Figure 3* must be electrically isolated from each other

FIGURE 3. Grounded Side of Circuit. This Circuit Can Safely Be Connected to a Chart Recorder or Computer Due to Isolation Provided by TRW Transformer.

Figure 2 and *Figure 3* show the detailed schematic, with *Figure 4* giving the waveforms of operation. The AC line is divided down by the 100 kΩ–4.4 kΩ resistor string. ½ of A2 (amplifier A) serves as a buffer and feeds one input of an analog multiplier configuration. A1 monitors the voltage across the current shunt at a fixed gain of 100. The other half of A2 (B) provides additional gain and calibrated switching of wattage sensitivities from 2W to 2000W full-scale over four decade ranges. The 1N1195 diodes and the 20A fuses protect A1 and the shunt in the event a short appears across the load test socket. The voltage and current signals are multiplied by a multiplier configuration comprised of amplifiers A3, C and D, and the LM394 dual transistors. The multiplier is of

the variable transconductance type and works by using one input to vary the gain of an amplifier whose output is the other input of the multiplier.

The output of the multiplier (*Figure 4*, Trace A) represents the instantaneous power consumed by the load. This information is used to bias a pulse amplitude modulating isolation amplifier. The isolation amplifier is made up of A3 (A and B) and the discrete transistors. The A3 (A) oscillator output (*Figure 4*, Trace B) biases the Q1-Q2 switch, which drives a pulse transformer. A3 (B) measures the amplitude of the pulses at the transformer and servo controls them to be the same amplitude as its "+" input, which is biased from the multiplier output. Q3 provides current drive capability and completes the feedback path for A3 (B). *Figure 4*, Trace D shows the pulses applied to the transformer. Note that the amplitude of the pulses applied to the transformer forms an envelope whose amplitude equals the multiplier output. *Figure 4*, Trace C shows Q3's emitter voltage changing to meet the requirements of the servo loop.

The amplitude modulated pulses appear at the transformer's secondary, which is referenced to instrument ground. The amplitude of each pulse is sampled by A5, a sample-hold amplifier. The sample command is generated by A4. The output of A5 is lightly filtered by the 15 kΩ–0.02 µF combination and represents a sampled version of the instantaneous power consumed in the load (*Figure 4*, Trace E). Heavy filtering by the 1 MΩ–1 µF time constant produces a smoothed version of the power signal, which drives the watts meter and the strip chart output via the A6 (A) buffer. The watt-hour time integration function is provided by an LM331 voltage-to-frequency converter and a digital divider chain which form a digital integrator. The lightly filtered A5 output is fed to A6 (B) which is used to bias the V/F converter. The V/F output drives a divider chain. The ratio of the divider chain sets the time constant of the integrator and is used to switch the scale factor of the watt-hours display. The additional counters and display provide the digital readout in watt-hours. A zero reset button allows display reset.

Instrument Calibration

To calibrate the instrument, pull the 20A fuses from their holders. Next, adjust P1 for 0.00V out at A2 (B) with the watts range switch in the 2 watt position. Then, disconnect both multiplier input lines and connect them to floating instrument ground. Adjust P2 for 0V out at A6 (A). Next, apply a 10 Vp-p 60 Hz waveform to the current input of the multiplier (leave the voltage input grounded) and adjust P3 for zero volts out at A6 (A). Then, reverse the state of the multiplier inputs and adjust P4 for zero volts out at A6 (A). Reconnect the multiplier input into the circuit. Read the AC line voltage with a digital voltmeter. Plug in a known load (e.g., 1% power resistor) to the test socket and adjust P5 until the meter reads what the wattage should be (wattage = line voltage^2/resistance of load). Finally, lift A6's (B's) "+" input line, apply 5.00V to it, and adjust P6 until the LM331V/F output (pin 3) runs at 27.77 kHz. Reconnect A6's (B's) input. This completes the calibration.

Applications

Once calibrated, the watt-watt-hour meter provides a powerful measurement capability. A few simple tests provide some surprising and enlightening results. The strip chart of *Figure 5* shows the measured power a home refrigerator draws over 3½ hours at a temperature set-point of 7°C. Each time the compressor comes on, the unit draws about 260W. Actually, the strip chart clearly shows that as the compressor warms up over time, the amount of power drawn drops off a bit. The watt-hour display was used to record the total watt-hours consumed during this 3½ hour period. The data is summarized in the table provided. With the temperature control in the refrigerator set to maintain 5°C, just 2°C colder, it can be seen that the compressor duty cycle shifts appreciably (*Figure 6*), over 6%! This factor is directly reflected in the kW-H/cycle and yearly operating cost columns. If you want your milk 2°C colder you will have to pay for it!

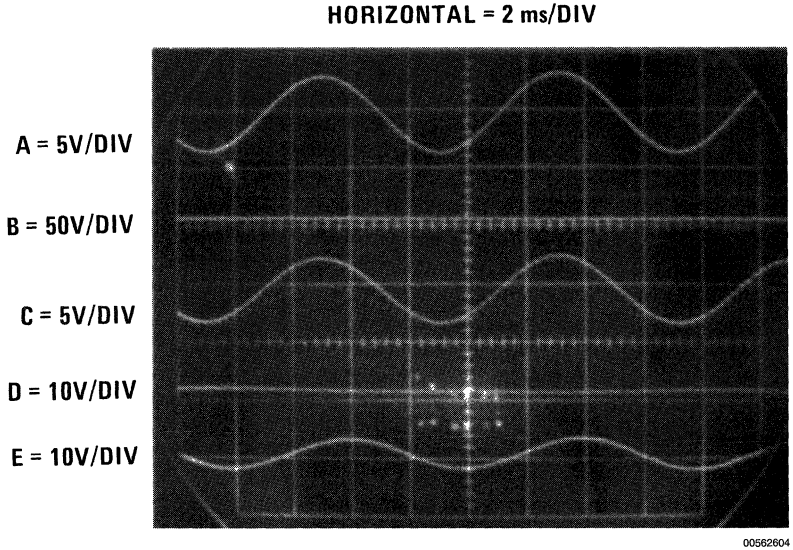
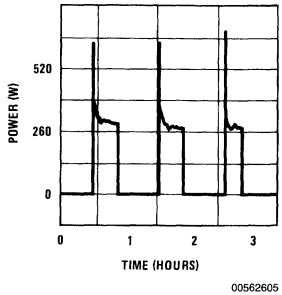


FIGURE 4.

Applications (Continued)



Temperature	Watts	Kilowatt-Hours/Cycle	Cost/Day	Cost/Year
5°C	260	0.119	$0.1147	$41.89
7°C	260	0.104	$0.0998	$36.44

FIGURE 5. Temperature=7.0°C Compressor Duty Cycle=40%

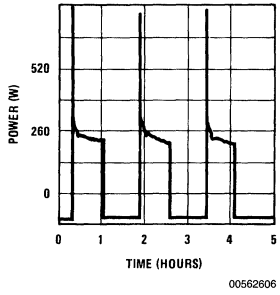
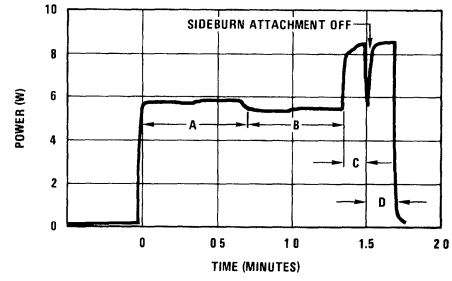


FIGURE 6. b. Temperature=5.0°C Compressor Duty Cycle=46%

The strip chart of *Figure 7* is somewhat less depressing but no less informative. In this example, the watt-watt-hour meter was used to record power consumption during morning shaving with an electric razor. From the strip chart and the table it can be seen that various facial areas cost more to shave than others. The high power drawn by the sideburn attachment on the razor is somewhat compensated for by the relatively short period of time it is in use. A complete shave, including the 4 areas listed, costs 0.00692 cents/day or 8.68 cents per year. If this is too high, you can economize by growing a beard.



Facial Area	Power (W)	Watt-Hours	Cost (at 4¢ Kilowatt-Hours) Per Shave
Cheeks ("A")	5.8	0.173	0.00692¢
Upper/Lower Lip ("B")	5.4	0.123	0.00492¢
Right Sideburn ("C")	8.4	0.063	0.00252¢
Left Sideburn ("D")	8.4	0.061	0.00244¢

FIGURE 7.

System-Oriented DC-DC Conversion Techniques

National Semiconductor
Application Note 288
Robert J. Widlar

In many electronic systems, the need arises to generate small amounts of power at voltages other than the main supply voltage. This is especially the case in digital systems where a relatively small amount of analog circuitry must be powered. A number of manufacturers have addressed this requirement by offering modular DC-DC converters which are PC mountable, offer good efficiency and are available in a variety of input and output voltage ranges. These units are widely applied and, in general, are well engineered for most applications. The sole problem with these devices is noise, in the form of high frequency switching spikes which appear on the output lines. To understand why these spikes occur, it is necessary to examine the operation of a converter.

A typical DC-DC converter circuit is shown in *Figure 1*. The transistors and associated components combine with the transformer primary to form a self-driven oscillator which provides drive to the transformer. The transformer secondary is rectified, filtered and regulated to obtain the outputs required. Typically, the transistors switch in saturated mode at 20 kHz, providing high efficiency square wave drive to the transformer. The output filter capacitors are relatively small compared to sine wave driven transformers and overall losses are quite low. The high speed, saturated switching of the transistors does, however, generate high frequency noise components. These manifest themselves as short duration current spikes drawn from the converter's input supply and as high speed spikes which appear on the output lines. In addition, the transformer can radiate noise in RF fashion. Manufacturers have dealt with these problems through careful converter design, including attention to input filter design, transformer construction and package shielding. *Figure 2* shows typical output noise of a good quality commercial DC-DC converter. The spikes are approximately 10 mV–20 mV in amplitude and occur at each transition of the switching transistors. In many applications this noise level is acceptable, but in data acquisition and other systems which work at 12-bit and higher resolutions, problems begin to crop up. In these situations, special system-oriented DC-DC converter techniques must be employed to insure against the problems outlined above.

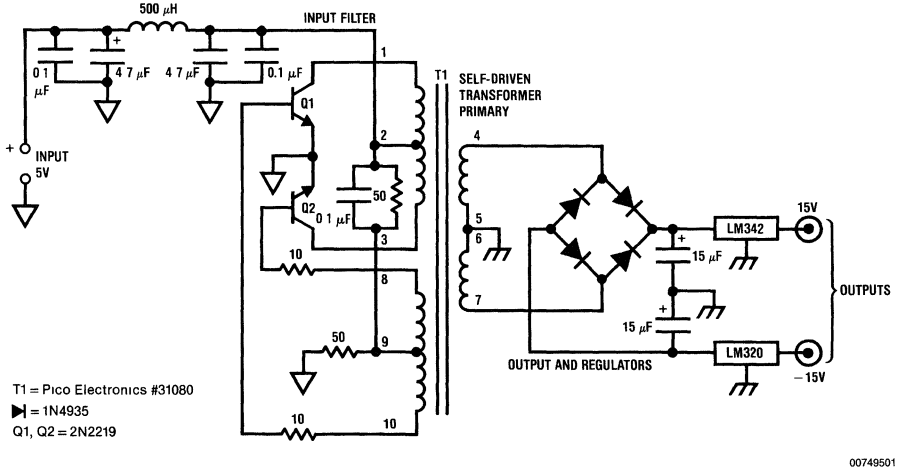


FIGURE 1.

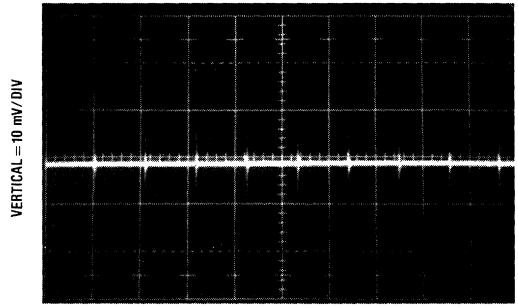


FIGURE 2.

Blank Pulse Converter

Figure 3 shows a converter which will supply 100 mA at ±15V from a 5V input. This design attacks the noise problem in two ways. The LM3524 switching regulator chip provides non-overlapping drive to the transistors, eliminating simultaneous conduction which helps keep input current spiking down. The LM3524 operates open loop. Its feedback connection (pin 9) is tied high, forcing the chip's outputs to full duty cycle. Internal logic in the LM3524 prevents the transistors from conducting at the same time. The components at pins 6 and 7 set the switching frequency. The LM3524's timing ramp biases the LM311 comparator to generate a blank pulse which "brackets" the output noise pulse. *Figure 4* shows the switching transistor waveforms (trace A and B) and the blank pulse (trace C) which is issued at each switching transition. The converter's output noise is shown in trace D. The blank pulse is used to alert the system that a noise spike is imminent. In this fashion, a critical A/D conversion or sample-hold operation can be delayed until the converter's noise spike has settled. This technique is quite effective, because it does not allow the system to "see" noise spikes during critical periods. This not only insures good system performance, but also means that a relatively simplistic converter design can be employed. The expense associated with low output noise (e.g., shielding, special filtering, etc.) can be eliminated in many cases. *Figure 5* details a converter design which uses a different approach to solving the same problem.

Blank Pulse Converter (Continued)

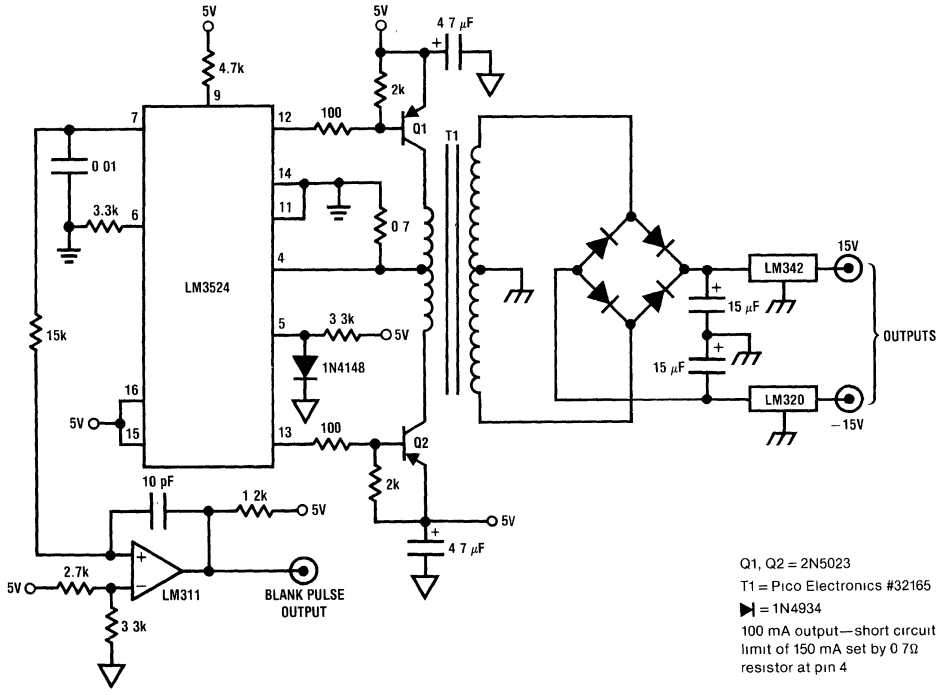


FIGURE 3.

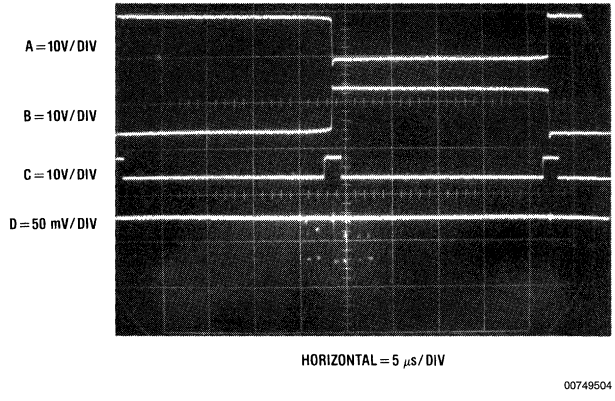


FIGURE 4.

Blank Pulse Converter (Continued)

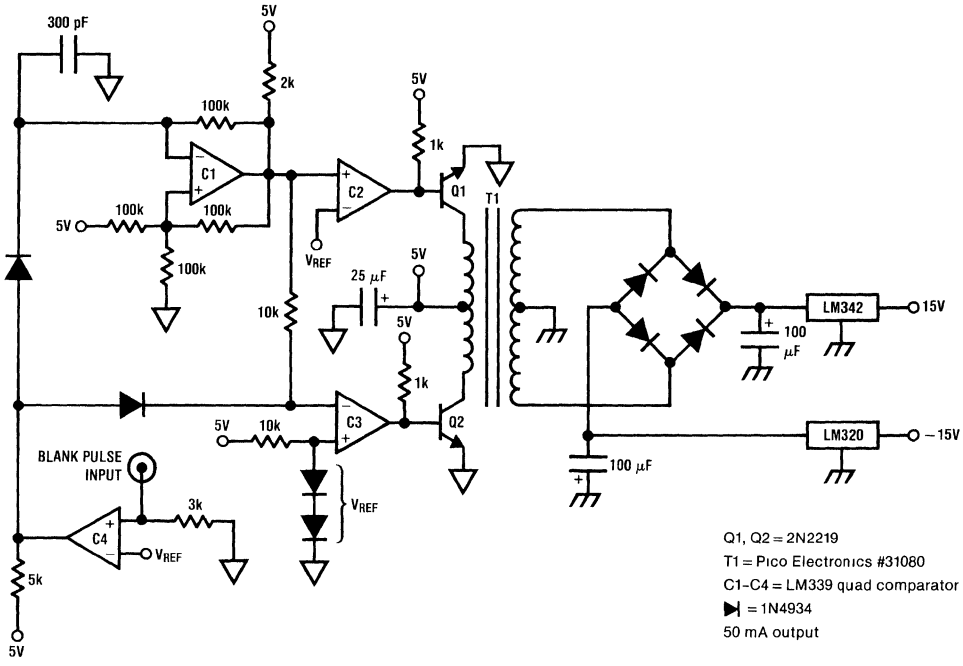


FIGURE 5.

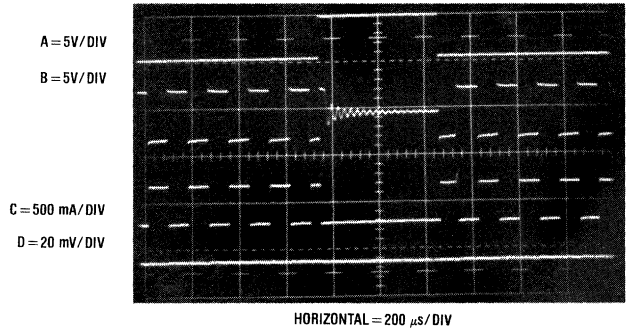


FIGURE 6.

Externally Strobed Converter

In *Figure 5* the system controls the converter, instead of the converter issuing blank commands. This arrangement uses an LM339 quad comparator to provide the necessary drive to the converter. C1 functions as a clock which provides drive to C2 and C3. These comparators drive the transistors (trace B, *Figure 6* is Q1's collector voltage waveform, while trace C details its current) to provide power to the transformer. When a critical system operation must occur, an external blank pulse (trace A) is applied to C4. C4's output goes high, shutting off all transformer drive. Under these conditions, the transformer current ceases (note voltage ringing on turn-off in trace B) and output noise (trace D) virtually disappears because the output regulators are powered only by the 100 µF filter capacitors. The value of these capacitors will depend directly on the output load and the length of the blank pulse. If synchronization to the system is desired, a system-derived 20 kHz square wave may be

Externally Strobed Converter

(Continued)

applied at C1's negative input through 2k, after removing the 300 pF capacitor and the 100k feedback resistor. The low noise during the blank pulse period affords ideal conditions for sensitive system operations. Although this approach allows great flexibility, the amount of off time is limited by the storage capacity of the output filter capacitors. In most systems this is not a problem, but some cases may require a converter which supplies low noise outputs at 100% duty cycles.

Sine Wave Driven Converter

Figure 7 diagrams a converter which sacrifices the efficient saturated-switch mode of operation to achieve an inherently low noise output at a 100% duty cycle. In this converter, sine wave drive is used to power the transformer. Q1 functions as a 20 kHz phase shift oscillator with Q2 providing an emitter-followed output. A1 and A2 are used to drive the transformer in complementary-bridge fashion (traces A and B, *Figure 8*). The high current output capability of the amplifiers, in combination with the transformer's paralleled primaries, results in a high power transformer drive. The transformer output is rectified, filtered and regulated in the usual fashion. Because the sine wave drive contains little harmonic content and current spiking, output noise is well below 1 mV (trace C, *Figure 8*). To adjust this circuit, ground the wiper arm of the 1k potentiometer and adjust the 100k value for minimum power supply drain. Next, unground the 1k potentiometer wiper arm and adjust it so that both A1 and A2's outputs are as large as possible without clipping. This circuit yields a low noise output on a 100% available basis but efficiency degrades to about 30%. In relatively low power converters such as this one (e.g., 50 mA output current) this is often acceptable.

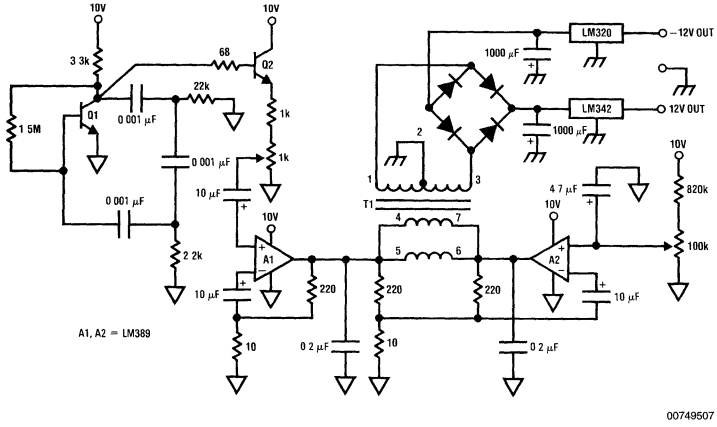


FIGURE 7.

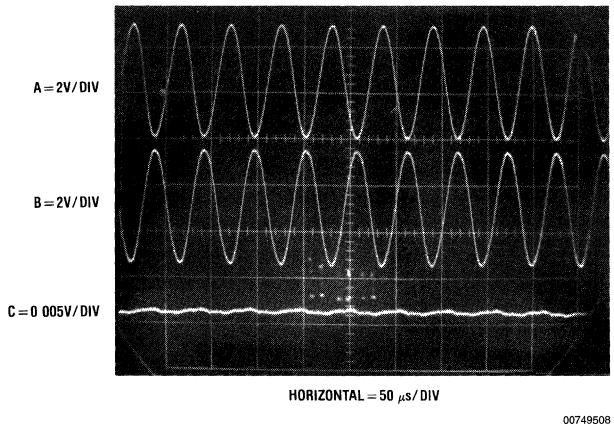


FIGURE 8.

Low Power Converter

Figure 9 shows a converter which operates from very low power. This circuit will provide 7.5V output from a 1.5V D cell battery. With a 125 µA load current (typically 20 CMOS ICs) it will run for 3 months. It may be externally strobed off during periods where lowest output noise is desired and it also issues a "converter running" pulse. This circuit is unusual in that the amount of time required for Q1 and Q2 to drive the transformer is directly related to the load resistance. The converter's output voltage is sensed by an LM10 op amp reference IC, which compares the converter output to its own internal 200 mV reference via the 5.1M-160k voltage divider. Whenever the converter output is below 7.5V, the LM10 output goes high, driving the Q1-Q2 pair and the transformer which form an oscillator. The transformer output is rectified and used to charge the 47 µF capacitor. When the capacitor charges to a high enough value, the LM10 output goes low and oscillation ceases. Trace A, *Figure 10* shows the collector of Q1, while trace B shows the output voltage across the 47 µF capacitor (AC coupled). It can be seen that each time the output voltage falls a bit the LM10 drives the oscillator, forcing the voltage to rise until it is high enough to switch the LM10 output to its low stage. The frequency of this regulating action is determined by the load on the converter output. To prevent the converter from oscillating about the trip point, the 0.1 µF unit is used to provide hysteresis of response. Very low loading of the converter will result in almost no on time for the oscillator while large loads will force it to run almost constantly. Loop operating frequencies of 0.1 Hz to 40 Hz are typical. The LM10 output state may be used to alert the system that the converter is running. A pulse applied to the LM10 negative input will override normal converter operation for low noise operation during a critical system A/D conversion.

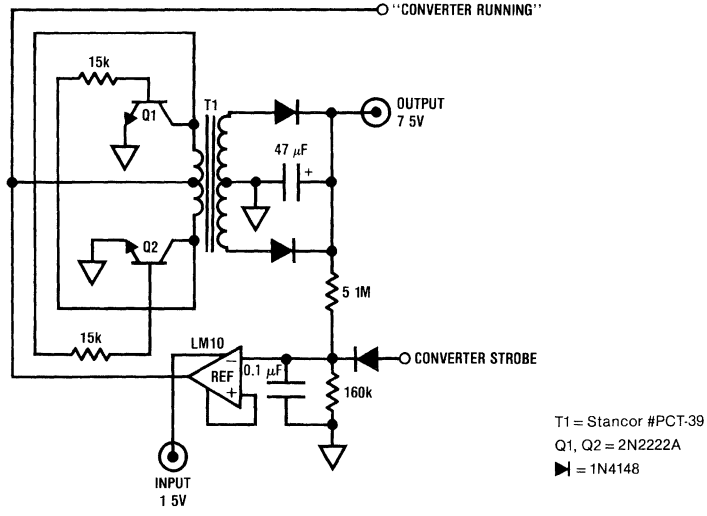


FIGURE 9.

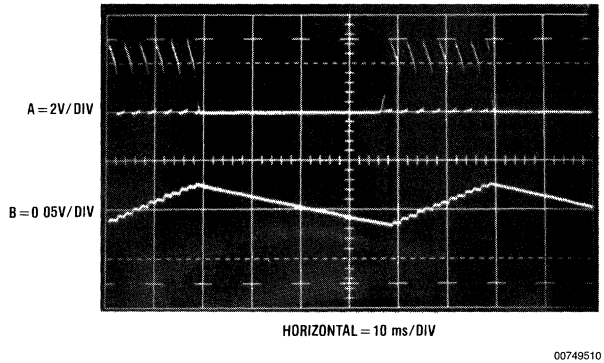


FIGURE 10.

Applications of the LM3524 Pulse-Width-Modulator

National Semiconductor
Application Note 292
Robert J. Widlar

The LM3524 Regulating Pulse-Width-Modulator is commonly used as the control element in switching regulator power supplies. This is in keeping with its intended purpose. Engineers closely associate this part with switching power supplies. Nevertheless, the flexible combination of elements (see box) within the LM3524 also allows it to be used in a number of other applications outside the power supply area. Because the device is inexpensive and operates off a single-sided supply, it can considerably reduce component count and circuit complexity in almost any application. The constant light intensity servo of *Figure 1* furnishes a good example.

Constant Light Intensity Servo

The circuit of *Figure 1* uses a photodiode's output to control the intensity of a small light bulb. The constant intensity output of the light bulb is useful in a number of areas, including opto-electronic component evaluation and quality control of photographic film during manufacture. In this circuit, the photodiode pulls a current out of the LF356 summing junction, which is directly related to the amount of light that falls on the photodiode's surface. The LF356 output swings positive to maintain the summing junction at zero and represents the photodiode current in amplified voltage form. This potential is compared at the LM3524 to the voltage coming from the 2.5k "intensity" potentiometer wiper. A stable voltage for the "intensity" control is taken from the LM3524's internal five-volt regulator. The difference between the LF356 output and the "intensity" potentiometer output is amplified at a gain of about 70 dB, which is set by the 1 MΩ value at pin 9. The LM3524 output transistors are paralleled and provide drive to the 2N2219 switch transistor. The 5.6k and .01 µF values set the switching frequency at about 30 kHz. Because the LM3524 forms a switched mode feedback loop around the light bulb and photodiode, the average power delivered to the light bulb will be controlled by the photodiode output, which is directly proportional to the lamp's output. Frequency compensation for this feedback loop is provided by the .001 µF capacitor, which rolls off the loop gain at a 1 ms time constant. *Figure 2* shows the wave forms in the circuit. Trace A is the 2N2219 collector and trace B is the AC-coupled LF356 output. Each time the 2N2219 collector goes low, power is driven into the lamp. This is reflected in the positive going ramp at the LF356's output. When the 2N2219 goes off, the lamp cools. This is shown in the negative going relatively slow ramp in trace B. It is interesting to note that this indicates the bulb is willing to accept energy more quickly than it will give it up. *Figure 3* elaborates on this. Here, trace A is the output of a pulse generator applied to the "step test" input and trace B is the AC-coupled LF356 output. When the pulse generator is high, the diode blocks its output, but when it goes low, current is drawn away from the "intensity" control wiper through the 22k resistor. This forces the servo to control bulb intensity at a lower value. This photo shows that the bulb servos to a higher output almost three times as fast as it takes to go to the lower output state, because the bulb more readily accepts energy than it gives it up. Surprisingly, at high intensity levels, the situation reverses because the increased incandescent state of the bulb makes it a relatively efficient radiator (*Figure 4*).

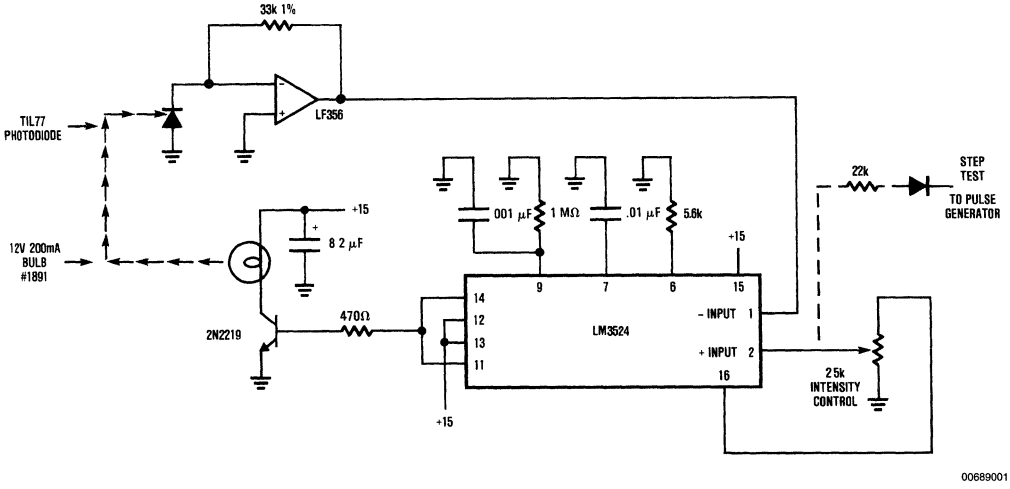


FIGURE 1.

Temperature-to-Pulse-Width Converter

The circuit in *Figure 5* uses the LM3524 to convert the output of an LM135 temperature transducer into a pulse width which can be measured by a digital system, such as a microprocessor-controlled data acquisition system. Although this example uses the temperature transducer as the input, the circuit will convert any 0.1 to 5V input applied to the 100 kΩ resistor into a 0–500 ms output pulse width with 0.1% linearity. In this circuit, the LM135's temperature-dependent output (10 mV/°K) is divided down and applied to A1's positive input. This moves A1's output high, driving the input to the LM3524's pulse-width modulation circuitry. The LM3524 pulse-width output is clipped by the LM185 reference and integrated by the 1 MΩ-0.1 µF combination. The DC level across the 0.1 µF capacitor is fed back to A1's negative input. This feedback path forces the LM3524's output pulse width to vary in a highly linear fashion according to the potential at A1's positive input. The overall temperature-to-pulse width scale factor is adjusted with the "gain trim" potentiometer. The 1000 pF capacitor provides stable loop compensation. A1, an LM358, allows voltages very close to ground to be sensed. This provides greater input range than the LM3524's input amplifier, which has a common mode range of 1.8–3.4V. The oscillator output pulse at pin 3 may be used to reset counters or other digital circuitry because it occurs just before the output pulse width begins.

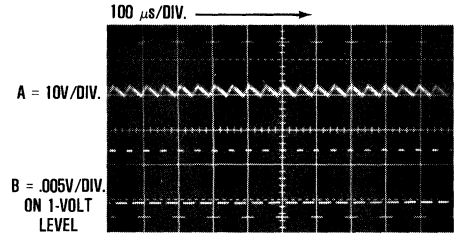


FIGURE 2.

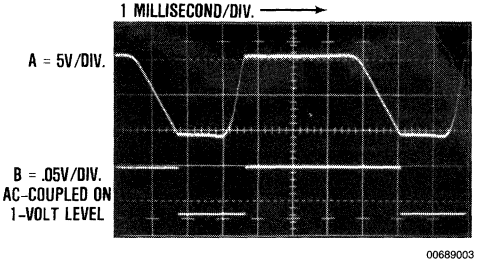


FIGURE 3.

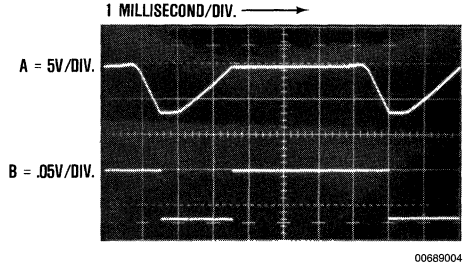
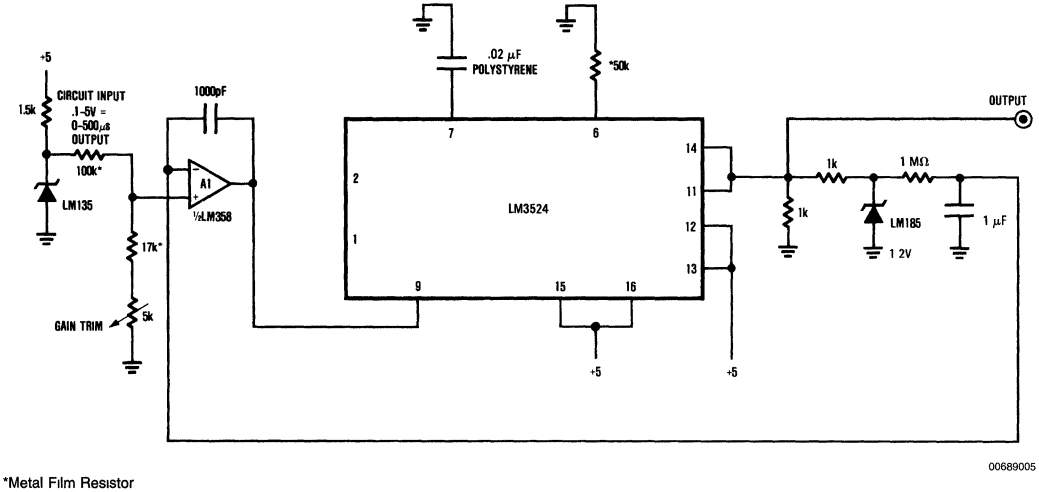


FIGURE 4.

Temperature-to-Pulse-Width Converter (Continued)



*Metal Film Resistor

FIGURE 5.

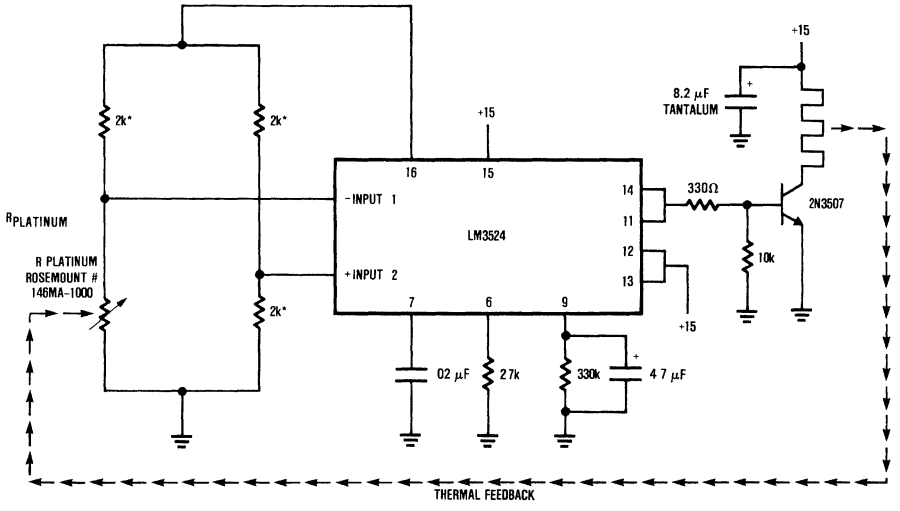
RTD Temperature Controller

Figure 6 is another temperature circuit which uses the LM3524 to control the temperature of a small oven. Here, a platinum RTD is used as a sensor in a bridge circuit made up of the 2 kΩ resistors. When power is applied, the positive temperature coefficient platinum sensor is at a low value and the LM3524's positive input is at a higher potential than its negative input. This forces the output to go high, turning on the 2N3507 and driving the heater. When the servo point is reached, the duty cycle of the heater is reduced from 90% (full on) to whatever value is required to keep the oven at temperature. The 330k-4.7 μF combination at the internal input amplifier's output sets the servo gain at about 55 dB at 1 Hz, more than adequate for most thermal-control applications. The 0.02 μF-2.7k combination sets the pulse frequency at about 15 kHz, far above the 1 Hz pole of the servo gain. If the sensor is maintained in close thermal contact with the heater, this circuit will easily control to .1°C stability over widely varying ambients.

"SENSORLESS" Motor Speed Control

Figure 7 shows the LM3524 in an arrangement which controls the speed of a motor without requiring the usual tachometer or other speed pick-off. This circuit uses the back EMF of the motor to bias a feedback loop, which controls motor speed. When power is applied, the positive input of the LM3524 is at a higher potential than the negative input. Under these conditions, the output of the LM3524 is biased full on (90% duty cycle). The output transistors, paralleled in the common emitter configuration, drive the 2N5023 and the motor turns. (LM3524 output is waveform A, *Figure 8*; waveform B is the 2N5023 collector.) The LM3524 output pulse is also used to drive a 1000 pF-500 kΩ differentiator network whose output is compared to the LM3524's internal 5V reference. The result is a delayed pulse (*Figure 8*, waveform D), which is used to trigger an LF398 sample-hold IC. As the waveforms show, the sample-hold is gated high (ON) just as the 2N5023 collector stops supplying current to the motor. At this instant, the motor coils produce a flyback pulse, which is damped by the shunt diode. (Motor waveform is *Figure 8*, trace C). After the flyback pulse decays, the back EMF of the motor remains. This voltage is "remembered" by the sample-hold IC when the sample trigger pulse ceases and is used to complete the speed control loop back at the LM3524 input. The 10k-4k divider at the motor output insures the LF398's output will always be within the common range of the LM3524's input. The 10k-1 μF combination provides filtering during the time the LF398 is sampling. The diode associated with this time constant prevents any possible LF398 negative output from damaging the LM3524. The 10 MΩ resistor paralleling the 0.01 μF sampling capacitor prevents the servo from "hanging up" if this capacitor somehow manages to charge above the motor's back EMF value. The 39k-100 μF pair sets the loop frequency response. The maximum pulse-width-modulator duty cycle is clamped by the 2k-2k divider and diode at 80%, thus avoiding overshoot and aiding transient response at turn-on and during large positive step changes. The 60k-0.1 μF values at pins 6 and 7 set the pulse modulation frequency at 300 Hz.

"SENSORLESS" Motor Speed Control (Continued)



*TRW Type MAR-60 1%

FIGURE 6.

"SENSORLESS" Motor Speed Control (Continued)

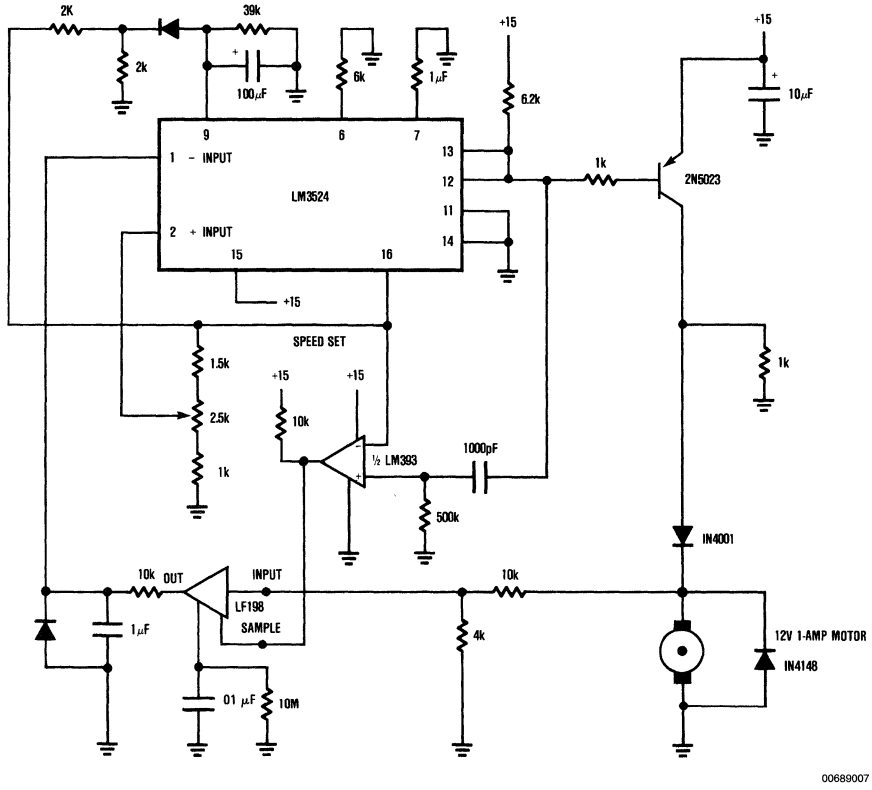


FIGURE 7.

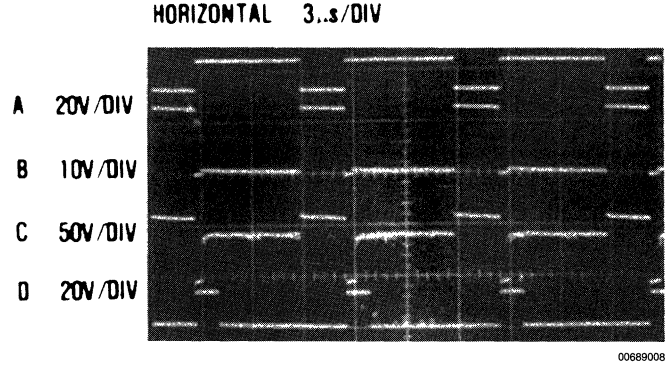
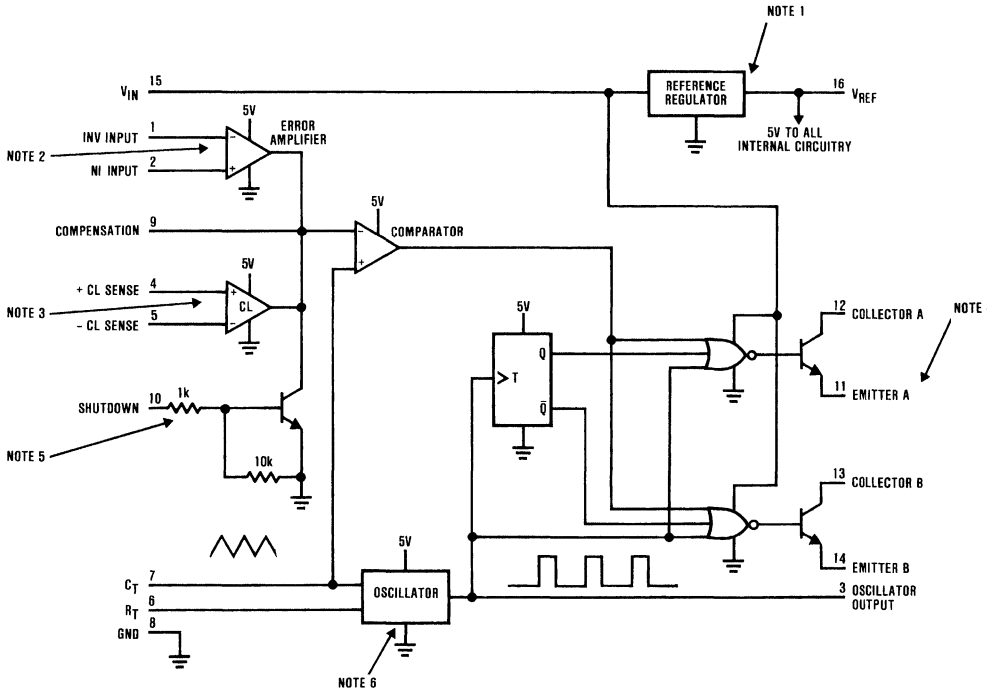


FIGURE 8.

"SENSORLESS" Motor Speed Control (Continued)

The LM3524 at a Glance



00689009

Note 1: 5V 50 mA regulator available to user

Note 2: Transconductance diff input amplifier Gains from 40–80 dB available by resistor loading of output 1 8–3 4V common mode input range

Note 3: Over current sense comparator –0 7 to 1V common mode input range.

Note 4: Output transistors switch out of phase and may be paralleled Up to 100 mA maximum output current

Note 5: Transistor may be used to strobe LM3524 into an off state at its outputs

Note 6: Oscillator typically frequency programmable for up to 100 kHz.

Introduction to Power Supplies

National Semiconductor
Application Note 556

Introduction

Virtually every piece of electronic equipment, e.g., computers and their peripherals, calculators, TV and hi-fi equipment, and instruments, is powered from a DC power source, be it a battery or a DC power supply. Most of this equipment requires not only DC voltage but voltage that is also well filtered and regulated. Since power supplies are so widely used in electronic equipment, these devices now comprise a worldwide segment of the electronics market in excess of $5 billion annually.

There are three types of electronic power conversion devices in use today which are classified as follows according to their input and output voltages: 1) DC/DC converter; 2) the AC/DC power supply; 3) the DC/AC inverter. Each has its own area of use but this paper will only deal with the first two, which are the most commonly used.

A power supply converting AC line voltage to DC power must perform the following functions at high efficiency and at low cost:

1. Rectification: Convert the incoming AC line voltage to DC voltage.
2. Voltage transformation: Supply the correct DC voltage level(s).
3. Filtering: Smooth the ripple of the rectified voltage.
4. Regulation: Control the output voltage level to a constant value irrespective of line, load and temperature changes.
5. Isolation: Separate electrically the output from the input voltage source.
6. Protection: Prevent damaging voltage surges from reaching the output; provide back-up power or shut down during a brown-out.

An ideal power supply would be characterized by supplying a smooth and constant output voltage regardless of variations in the voltage, load current or ambient temperature at 100% conversion efficiency. *Figure 1* compares a real power supply to this ideal one and further illustrates some power supply terms.

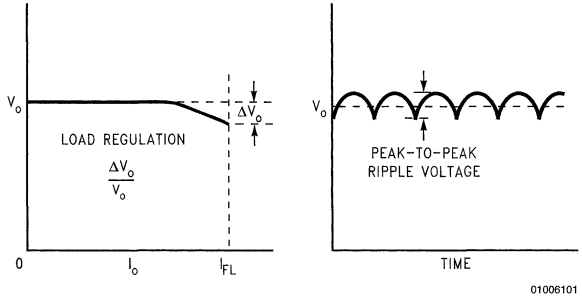


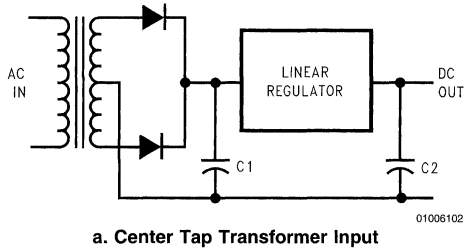
FIGURE 1. Real Power Supply has error compared to Ideal Power Supply

Linear Power Supplies

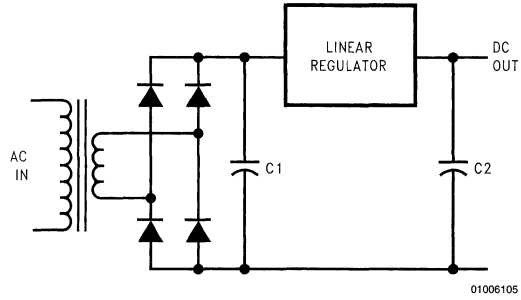
Figure 2 illustrates two common linear power supply circuits in current use. Both circuits employ full-wave rectification to reduce ripple voltage to capacitor C1. The bridge rectifier circuit has a simple transformer but current must flow through two diodes. The center-tapped configuration is preferred for low output voltages since there is just one diode voltage drop. For 5V and 12V outputs, Schottky barrier diodes are commonly used since they have lower voltage drops than equivalently rated ultra-fast types, which further increases power conversion efficiency. However, each diode must withstand twice the reverse voltage that a diode sees in a full-wave bridge for the same input voltage.

The linear voltage regulator behaves as a variable resistance between the input and the output as it provides the precise output voltage. One of the limitations to the efficiency of this circuit is due to the fact that the linear device must drop the difference in voltage between the input and output. Consequently the power dissipated by the linear device is $(V_I - V_O) \times I_O$. While these supplies have many desirable characteristics, such as simplicity, low output ripple, excellent line and load regulation, fast response time to load or line changes and low EMI, they suffer from low efficiency and occupy large volumes. Switching power supplies are becoming popular because they offer better solutions to these problems.

Linear Power Supplies (Continued)



a. Center Tap Transformer Input



b. Full-Wave Bridge Input

FIGURE 2. Linear Voltage Regulator

Switching vs Linear Power Supplies

Switching power supplies are becoming popular due to high efficiency and high power density. *Table 1* compares some of the salient features of both linear and switching power supplies. Line and load regulation are usually better with linear supplies, sometimes by as much as an order of magnitude, but switching power supplies frequently use linear post-regulators to improve output regulation.

DC-DC Converters

DC-DC converters are widely used to transform and distribute DC power in systems and instruments. DC power is usually available to a system in the form of a system power supply or battery. This power may be in the form of 5V, 28V, 48V or other DC voltages. All of the following circuits are applicable to this type of duty. Since voltages are low, isolation is not usually required.

TABLE 1. Linear vs Switching Power Supplies (typical)

Specification	Linear	Switcher
Line Regulation	0.02%–0.05%	0.05%–0.1%
Load Regulation	0.02%–0.1%	0.1%–1.0%
Output Ripple	0.5 mV–2 mV RMS	10 mV–100 mV_{P-P}
Input Voltage Range	±10%	±20%
Efficiency	40%–55%	60%–95%
Power Density	0.5 W/cu. in.	2W–10W/cu. in.
Transient Recovery	50 µs	300 µs
Hold-Up Time	2 ms	34 ms

Switching Power Supplies

PULSE WIDTH MODULATION

In the early 60's, switching regulators started to be designed for the military, who would pay a premium for light weight and efficiency. One way to control average power to a load is to control average voltage applied to it. This can be done by opening and closing a switch in rapid fashion as being done in *Figure 3*.

The average voltage seen by the load resistor R is equal to:

$$V_{o(avg)} = (t_{(on)}/T) \times V_i \qquad (1)$$

Reducing $t_{(on)}$ reduces $V_{o(avg)}$. This method of control is referred to as pulse width modulation (PWM).

BUCK REGULATOR

As we shall see, there are many different switching voltage regulator designs. The first one to be considered because of its simplicity is the buck regulator (*Figure 4*), also known as a step-down regulator since the output voltage as given by *Equation (1)* is less than the input voltage. A typical application is to reduce the standard military bus voltage of 28V to 5V to power TTL logic.

At time $t_{(o)}$ in *Figure 4*, the controller, having sensed that the output voltage V_O is too low, turns on the pass transistor to build up current in L, which also starts to recharge capacitor C. At a predetermined level of V_o, the controller switches off the pass transistor Q, which forces the current to free wheel around the path consisting of L, C, and the ultra-fast rectifier D. This effectively transfers the energy stored in the inductor L to the capacitor. Inductor and capacitor and capacitor sizes are inversely proportional to switching frequency, which accounts for the increasing power density of switching power supplies. Power MOSFETs are rapidly replacing bi-polar transistors as the pass transistor because of their high frequency capability Since the pass transistor must not only carry load current but reverse recovery current of diode D, an ultra-fast recovery diode or Schottky diode is mandatory.

Switching Power Supplies (Continued)

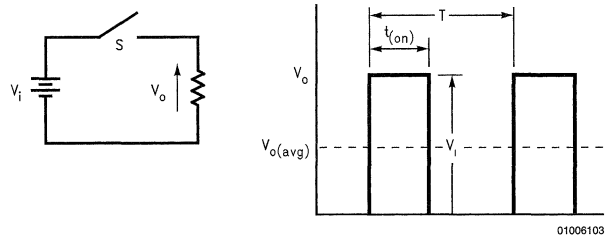


FIGURE 3. Example of Pulse Width Modulation

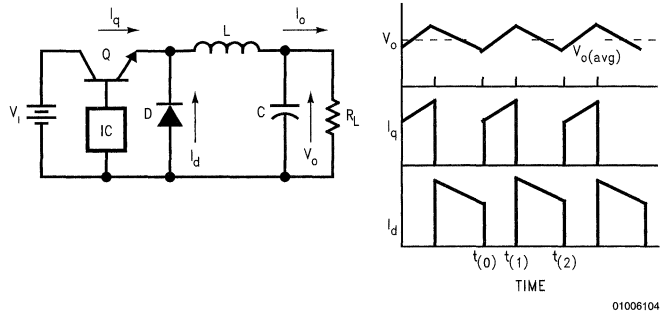


FIGURE 4. Buck Regulator Circuit with Voltage and Current Waveforms

BOOST REGULATOR

A second type of regulator shown in *Figure 5* is capable of boosting the input voltage. Applications for this circuit would be to increase 5V battery sources to 12V for interface circuits or even to 150V for electro-luminescent displays.

The concept of this circuit is still the same as the previous, namely to transfer the energy stored in the inductor into the capacitor. The inductor current can ramp up quickly when the transistor switch is closed at time $t_{(0)}$ since the full input voltage is applied to it. The transistor is turned off at time $_{(1)}$ which forces the inductor current to charge up the capacitor through the ultra-fast diode D. Since the energy stored in the inductor is equal to L x I x ½, the PWM IC can increase V_o by increasing its own on-time to increase the peak inductor current before switching. The transfer function is:

$$V_o = V_{IN} (T/(T - t_{(on)})) \quad (2)$$

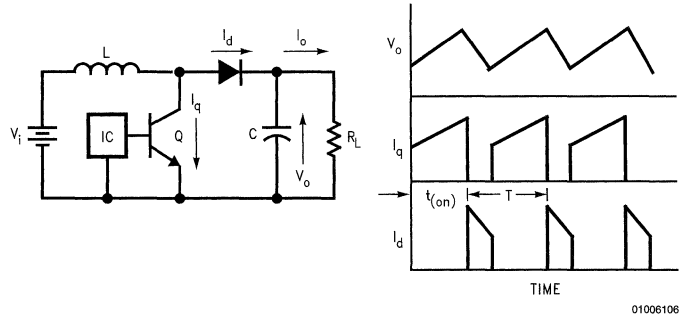


FIGURE 5. Boost Regulator and Associated I/V Waveforms

Switching Power Supplies (Continued)

INVERTING REGULATOR

Figure 6 shows a switching circuit which produces an output voltage with the opposite polarity of the input voltage. This circuit works in the same fashion as the boost converter but has achieved the voltage inversion by exchanging positions of the transistor and inductor. The circuit is also known as a buck-boost regulator since the absolute magnitude of the output voltage can be higher or lower than the input voltage, depending upon the ratio of on-time to off-time of the pass transistor.

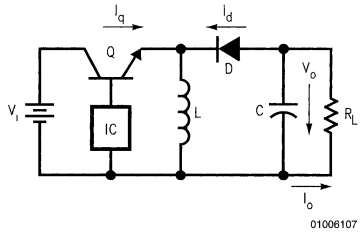


FIGURE 6. Inverting Regulator

FLYBACK CONVERTER

The three previous regulators are suitable for low voltage control when no electrical isolation is required. However in off-line switchers operating from 110V/220V mains, electrical isolation is an absolute must. This is achieved by using a transformer in place of the inductor. The flyback converter shown in *Figure 7* is commonly used in power supplies up through 150W, which is sufficient for most personal computers, many test instruments, video terminals and the like.

Since the transformer operates at high frequency, its size is much smaller than a 50 Hz/60 Hz transformer shown in *Figure 2*. Within certain frequency limits, transformer size is inversely proportional to frequency.

Inspection of the switching waveforms in *Figure 7* shows that the circuit behaves very similarly to the boost regulator. The transformer should be regarded as an inductor with two windings, one for storing energy in the transformer core and the other for dumping the core energy into the output capacitor. Current increases in the primary of the transformer during the on-time of the transistor ($t_{(0)} - t_{(1)}$) but note that no secondary current flows because the secondary voltage reverse biases diode D. When the transistor turns off, the transformer voltage polarities reverse because its magnetic field wants to maintain current flow. Secondary current can now flow through the diode to charge up the output capacitor. The output voltage is given by the basic PWM equation times the transformer turns ration (N2/N1):

$$V_o = V_{IN} \times (t_{(on)})/(T - t_{(on)}) \times (N2/N1) \qquad (3)$$

Voltage control is achieved by controlling the transistor on-time to control the peak primary current.

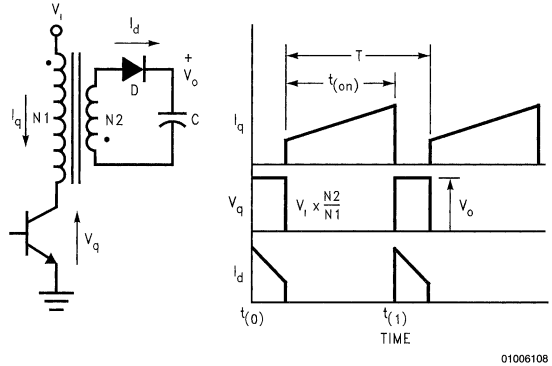


FIGURE 7. Flyback Converter

The flyback converter is well suited for multiple output and high voltage power supplies since the transformer inductance replaces the filter inductor(s). The major disadvantages which limit its use to lower wattage supplies are:

1. The output ripple voltage is high because of half-wave charging of the output capacitor.
2. The transistor must block 2 x V_{IN} during turn-off.
3. The transformer is driven in only one direction, which necessitates a larger core, i.e., more expensive, in a flyback design than for an equivalent using a forward or push-pull design.

OFF-LINE SWITCHING SUPPLY

Based on the flyback regulator circuit, a complete off-line switching supply is shown in *Figure 8*. The supply is called "off-line" because the DC voltage to the switch is developed right from the AC line.

The circuit also shows the feedback loop completed from the output back to the switching transistor. This feedback loop must have isolation in order for the DC output to be isolated from the AC line. This is normally accomplished by a small transformer or opto-coupler.

Switching Power Supplies (Continued)

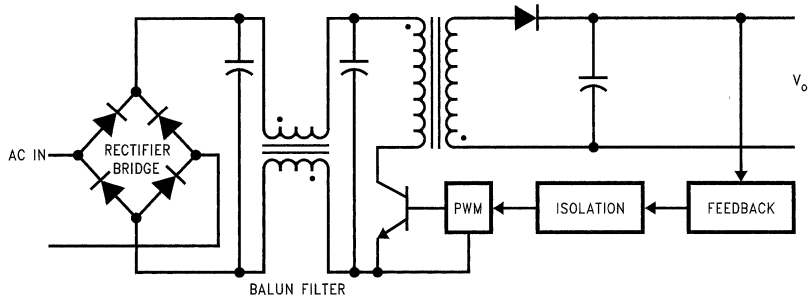


FIGURE 8. Complete Isolated Flyback Switching Supply

Switching power supplies designed for international usage must have selectable AC input voltage ranges of 115V and 230V. *Figure 9* shows how this is accomplished for many switching power supplies.

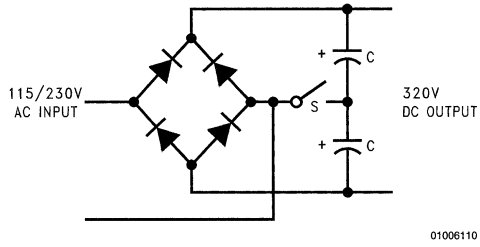


FIGURE 9. Selector Switch for 115V/230V Inputs

FORWARD CONVERTER

Although the forward converter is not as well-known as the flyback converter, it is becoming increasingly popular for power supplies in the 100W–500W range. *Figure 10* shows the basic circuit of the forward converter. When the transistor is switched on, current rises linearly in the primary and secondary current also flows through diode D1 into the inductor and capacitor. When the transistor switch is opened, inductor current continues to free-wheel through the capacitor and diode D2. This converter will have less ripple since the capacitor is being continuously charged, an advantage of particular interest in high current supplies.

The relationship between input and output for this circuit configuration is:

$$V_o = V_{IN} \times (N2/N1) \times (t_{(on)}/T) \quad (4)$$

Note that the transformer shown in the above figure has been wound with a third winding and series diode D3. The purpose of this winding is to transfer the magnetizing energy in the core back to the DC supply so it does not have to be dissipated in the transistor switch or some other voltage suppressor. The turns ratio N3/N1 limits the peak voltage seen by the transistor and is normally chosen equal to 1 so that the forward converter can run at 50% duty cycle. Under this condition, the transistor must block 2 x V_{IN} during turn-off.

Switching Power Supplies (Continued)

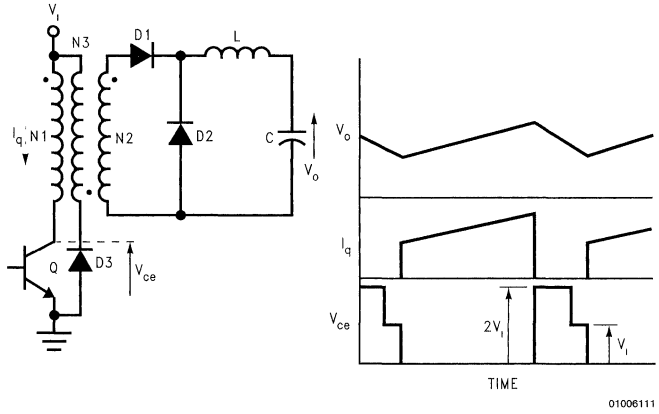


FIGURE 10. Forward Converter

Symmetrical Converters

PUSH-PULL CONVERTER

The circuit for this widely used converter is shown in *Figure 11*.

Transistors Q1 and Q2 are alternately switched on for time period ($t_{(on)}$ This subjects the transformer core to an alternating voltage polarity to maximize its usefulness. The transfer function still follows the basic PWM formula but there is the added factor 2 because both transistors alternately conduct for a portion of the switching cycle.

$$V_o = 2 \times V_{IN} \times (N2/N1) \times (t_{(on)}/T) \quad (5)$$

The presence of a dead time period $t_{(d)}$ is required to avoid having both transistors conduct at the same time, which would be the same as turning the transistors on into a short circuit. The output ripple frequency is twice the operating frequency which reduces the size of the LC filter components Note the anti-parallel diodes connected across each transistor switch. They perform the same function as diode D3 in the forward converter, namely to return the magnetization energy to the input voltage whenever a transistor turns off.

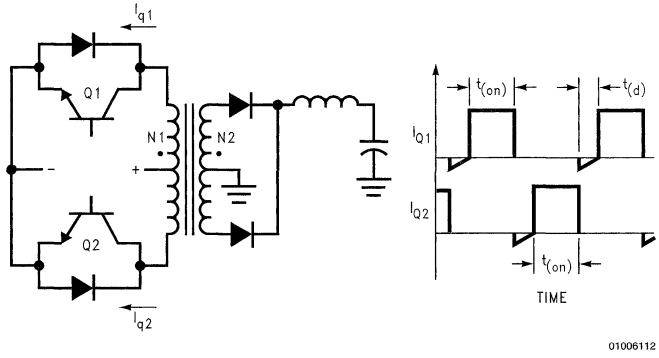


FIGURE 11. Push-Pull Converter

Compared to the following symmetrical converters, this circuit has the advantage that the transistor switches share a common signal return line. Its chief disadvantages are that the transformer center-tap connection complicates the transformer design and the primary windings must be tightly coupled in order to avoid voltage spikes when each transistor is turning off.

HALF-BRIDGE CONVERTER

This converter (*Figure 12*) operates in much the same fashion as the previous push-pull circuit

Symmetrical Converters (Continued)

The input capacitors C1 and C2 split the input voltage equally so that when either transistor turns on, the transformer primary sees $V_{in}/2$. Consequently note no factor of "2" in the following transfer equation:

$$V_o = V_{IN} \times (N2/N1) \times (t_{(on)}/T) \quad (6)$$

Since the two transistors are connected in series, they never see more than the input voltage V_{IN} plus the inevitable switching transient voltages. The necessity of a dead time is even more obvious here since the simultaneous conduction of both transistors results in a dead short across the input supply. Anti-parallel ultra-fast diodes return the magnetization energy as in the push-pull circuit but alternately to capacitors C1 and C2. This circuit has the slight inconvenience of requiring an isolated base drive to Q1, but since most practical base drive circuits use a transformer for isolation, this shortcoming is hardly worth noting.

FULL-BRIDGE CONVERTER

Because of its complexity and expense, the full-bridge converter circuit of *Figure 13* is reserved for high power converters. Ideally, all voltages are shared equally between two transistors so that the maximum voltage rating of the device can approach V_{IN}.

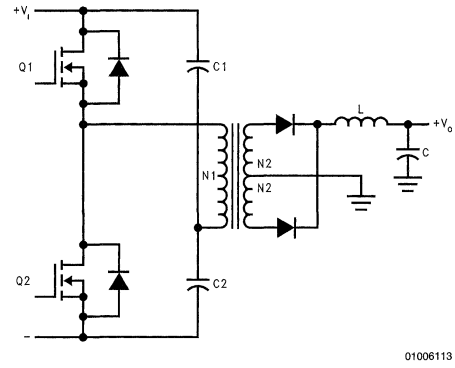


FIGURE 12. Half-Bridge Converter Circuit

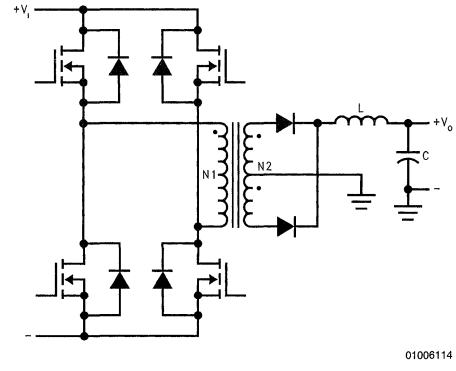


FIGURE 13. Full-Bridge Converter Circuit

LM78S40 Switching Voltage Regulator Applications

National Semiconductor
Application Note 711

Contents

Introduction

In modern electronic systems, voltage regulation is a basic function required by the system for optimal performance. The regulator provides a constant output voltage irrespective of changes in line voltage, load requirements, or ambient temperature.

For years, monolithic regulators have simplified power-supply design by reducing design complexity, improving reliability, and increasing the ease of maintenance. In the past, monolithic regulator systems have been dominated by linear regulators because of relatively low cost, low external component count, excellent performance, and high reliability. However, limitations to applicability and performance of linear regulators can force the user to other more complex regulator systems, such as the switching regulator.

Because of improvements in components made especially for them, switching-regulated power supplies have proliferated during the past few years. The emergence of inexpensive, high-speed switching power transistors, low-loss ferrites for inductor cores, and low-cost LSI circuits containing all necessary control circuitry has significantly expanded the range of switching regulator application.

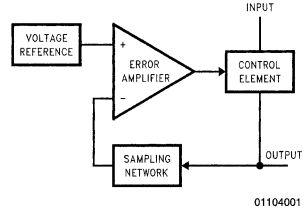
This application note describes a new integrated subsystem that contains the control circuitry, as well as the switching elements, required for constructing switching regulator systems (*Figure 1*). The principle of operation is discussed, a complete system description provided, and the analysis and design of the basic configurations developed. Additional information concerning selection of external switching elements and design of the inductor is provided.

Principle of Operation

A D.C. power supply is usually regulated by some type of feedback circuit that senses any change in the D.C. output and develops a control signal to compensate for this change. This feedback maintains an essentially constant output.

In a monolithic regulator, the output voltage is sampled and a high-gain differential amplifier compares a portion of this voltage with a reference voltage. The output of the amplifier is then used to modulate the control element, a transistor, by varying its operating point within the linear region or between the two operating extremes, cutoff and saturation. When the pass transistor is operated at a point between cutoff and saturation, the regulator circuit is referred to as *linear* voltage regulator. When the pass transistor is operated only at cutoff or at saturation, the circuit is referred to as a *switching* regulator.

Linear System



Switching System

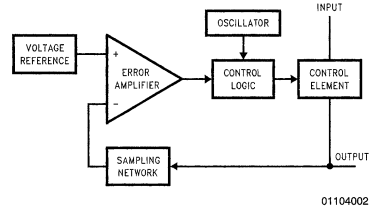


FIGURE 1. Regulator System Block Diagrams

One advantage of the switching regulator over the more conventional linear regulator is greater efficiency, since cutoff and saturation modes are the two most efficient modes of operation. In the cutoff mode, there is a large voltage across the transistor but little current through it; in the saturation mode, the transistor has little voltage across it but a large amount of current. In either case, little power is wasted, most of the input power is transferred to the output, and efficiency is high. Regulation is achieved by varying the duty cycle that controls the average current transferred to the load. As long as this average current is equal to the current required by the load, regulation is maintained.

Besides high efficiency operation, another advantage of the switching regulator is increased application flexibility offered by output voltages that are less than, greater than, or of opposite polarity to the input voltage. *Figure 2* illustrates these three basic operating modes.

Architecture

Each of the fundamental operating modes is built from the same set of functional blocks (*Figure 3*). Additional functions are required for control and protection, but again, these functional blocks are common to each of the operational modes. The different modes are obtained by proper arrangement of these basic blocks.

Architecture (Continued)

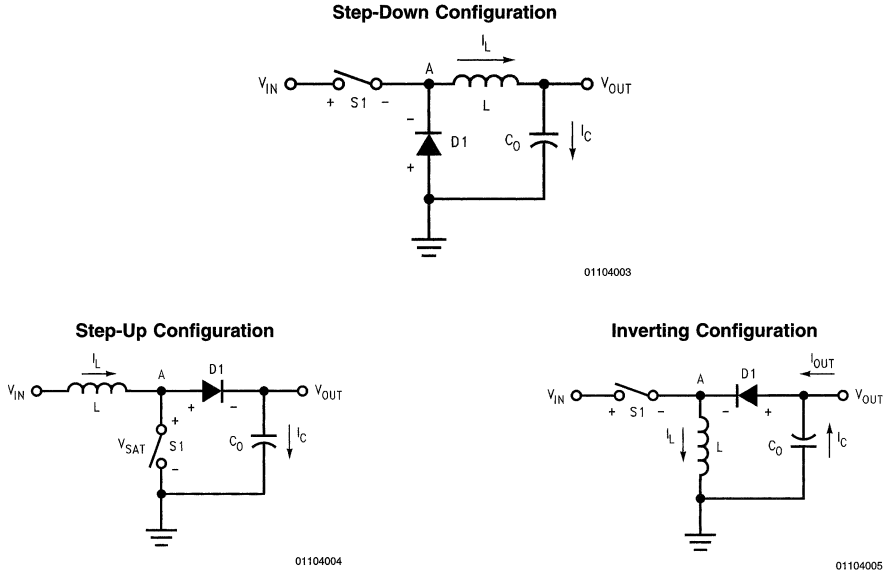


FIGURE 2. Basic Operating Modes

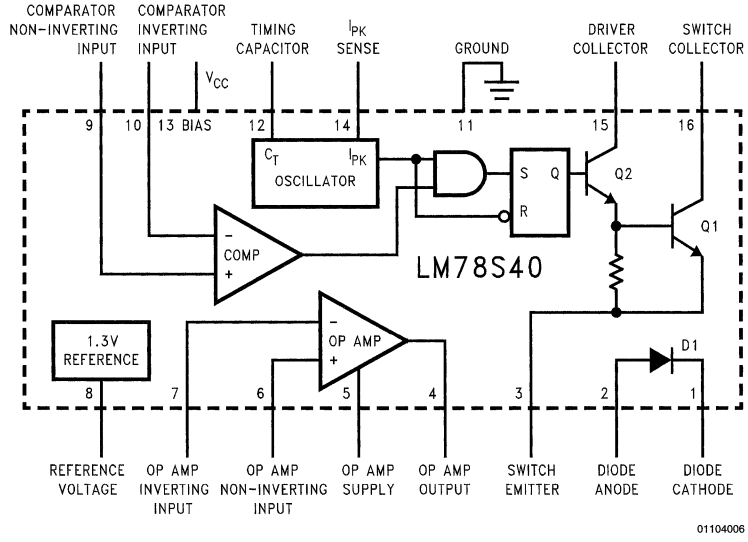


FIGURE 3. Functional Block Diagram

For maximum design flexibility and minimum external part count, the LM78S40 was designed to include all of the fundamental building blocks in an uncommitted arrangement. This provides for a simple, cost-effective design of any switching regulator mode.

The functional blocks of the regulator, illustrated in *Figure 3*, are:

- Current-controlled oscillator
- Temperature-compensated current-limiting circuit

Architecture (Continued)

- Temperature-compensated voltage reference
- High-gain differential comparator
- Power switching circuit
- High-gain amplifier

The current-controlled oscillator generates the gating signals used to control the on/off condition of the transistor power switch. The oscillator frequency is set by a single external capacitor and may be varied over a range of 100 Hz to 100 kHz. Most applications require an oscillator frequency from 20 kHz to 30 kHz. The oscillator duty cycle (t_{on}/t_{off}) is internally fixed at 6:1, but may be modified by the current-limiting circuit.

The temperature-compensated, current-limiting circuitry senses the switching transistor current across an external resistor and may modify the oscillator on-time, which in turn limits the peak current. This provides protection for the switching transistor and power diode. The nominal activation voltage is 300 mV, and the peak current can be programmed by a single resistor R_{SC}.

A 1.3V temperature-compensated, band-gap voltage source provides a stable reference to which the sampled portion of the output is compared. The reference is capable of providing up to 10 mA of current without an external pass transistor.

A high-gain ifferential comparator with a common-mode input range extending from ground to 1.5V less than V_{CC} is used to inhibit the basic gating signal generated by the oscillator turning on the transistor switch when the output voltage is too high.

The transistor switch, in a Darlington configuration with the collectors and emitter brought out externally for maximum design flexibility, is capable of handling up to 1.5A peak current and up to 40V collector-emitter voltage. The power switching diode is rated for the same current and voltage capabilities as the transistor switch; both have switching times that are normally 300 ns–500 ns.

Although not required by the basic operating modes, an independent operational amplifier has been included to increase flexibility. The characteristics of this amplifier are similar to the LM741, except that a power output stage has been provided, capable of sourcing up to 150 mA and sinking 35 mA. The input has also been modified to include ground as part of the common-mode range. This amplifier may be connected to provide series pass regulation or a second output voltage, or configured to provide special functions for some of the more advanced applications.

The switching regulator can be operated over a wide range of power conditions, from battery power to high-voltage, high-current supplies. Low voltage operation down to 2.4V and low standby current, less than 2.5 mA at 5V, make it ideal for battery-powered systems. On the other end, high-voltage capability, up to 40V, and high-current capability, up to 1.5A peak current, offer an operating range unmatched by other switching systems.

Analysis—Step-Down Operation

Figure 2 illustrates the basic configuration for a step-down switching voltage regulator system. The waveforms for this system are shown in *Figure 4*.

Assume, for analysis, that the following condition is true: before the switch is turned on,

$$i_L = 0$$

When switch S1 is closed, the voltage at point A becomes:

$$V_A = V_{IN} - V_{SAT}$$

where V_{SAT} is the saturation voltage of the switch.

At this time, the diode is reverse biased and the current through the inductor i_L is increasing at a rate equal to:

$$\frac{di}{dt} = \frac{V_L}{L} = \frac{V_{IN} - V_{SAT} - V_{OUT}}{L}$$

The current through the inductor continues to increase at this rate as long as the switch is closed and the inductor does not saturate. Assuming that the output voltage over a full cycle does not change significantly, this rate may be considered to be constant, and the current through the inductor at any instant, while the switch is closed, is given by:

$$i_L = \left(\frac{V_{IN} - V_{SAT} - V_{OUT}}{L}\right) t$$

The peak current through the inductor, which is dependent on the on-time t_{on} of S1, is given by:

$$I_{pk} = \left(\frac{V_{IN} - V_{SAT} - V_{OUT}}{L}\right) t_{on}$$

At the end of the on-time, switch S1 is opened. Since the inductor current cannot change instantaneously, it generates a voltage that forward biases diode D1, providing a current path for the inductor current. The voltage at point A is now:

$$V_A = -V_D$$

where V_D is the forward voltage of the diode.

The current through the inductor now begins to decay at a rate equal to:

$$\frac{di_L}{dt} = \frac{V_L}{L} = -\left(\frac{V_D + V_{OUT}}{L}\right)$$

Analysis—Step-Down Operation (Continued)

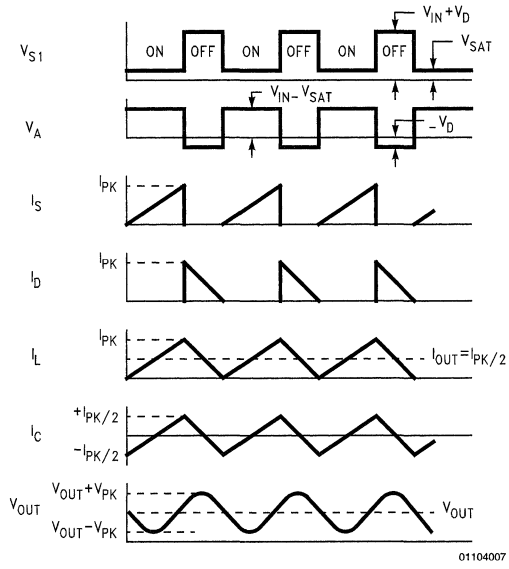


FIGURE 4. Waveforms for Step-Down Mode

The current through the inductor at any instant, while the switch is open, is given by:

$$i_L = I_{pk} - \left(\frac{V_D + V_{OUT}}{L}\right) t$$

Assuming that the current through the inductor reaches zero after the time interval t_{off}, then:

$$I_{pk} = \left(\frac{V_D + V_{OUT}}{L}\right) t_{off}$$

which results in the following relationship between t_{on} and t_{off}:

$$\frac{t_{on}}{t_{off}} = \frac{V_{OUT} + V_D}{V_{IN} - V_{SAT} - V_{OUT}}$$

In the above analysis, a number of assumptions were made. For the average output voltage to remain constant, the net charge delivered to the output capacitor must be zero. *Figure 4* (i_L waveform) shows that:

$$\left(\frac{I_{pk}}{2}\right) t_{on} + \left(\frac{I_{pk}}{2}\right) t_{off} = I_{OUT}\,(t_{on} + t_{off}),$$

$$\text{or } I_{pk} = 2\, I_{OUT}$$

For the average output voltage to remain constant, the average current through the inductor must equal the output current.

It was also assumed that the change (ripple) in the output voltage was small in comparison to the output voltage. The ripple voltage can be calculated from a knowledge of switching times, peak current and output capacitor size. *Figure 4* (i_C waveform) shows that:

$$V_{P\text{-}P} = \frac{\Delta Q}{C_O} = \frac{\frac{1}{2}\left(t_{on}\frac{I_{pk}}{4} + t_{off}\frac{I_{pk}}{4}\right)}{C_O} = \frac{I_{pk}\,(t_{on}/t_{off})}{8\,C_O}$$

The ripple voltage will be increased by the product of the output capacitor's equivalent series resistance (ESR) and i_C (though the two ripple terms do not directly add). Using large-value, low-ESR capacitors will minimize the ripple voltage, so the previous analysis will remain valid.

To calculate the efficiency of the system, n:

$$n = \frac{P_{OUT}}{P_{IN}}$$

The input power is given by:

$$P_{IN} = I_{IN}\, V_{IN}$$

The average input current can be calculated from the i_S waveform of *Figure 4*:

$$I_{IN(avg)} = \frac{t_{on}\left(\frac{I_{pk}}{2}\right)}{t_{on} + t_{off}} = I_{OUT}\left(\frac{t_{on}}{t_{on} + t_{off}}\right)$$

Analysis—Step-Down Operation

(Continued)

The output power is given by:

$$P_{OUT} = I_{OUT} V_{OUT}$$

Combining the above equations gives an expression for efficiency:

$$n = \left(\frac{V_{OUT}}{V_{OUT} + V_D}\right)\left(\frac{V_{IN} - V_{SAT} + V_D}{V_{IN}}\right)$$

As the forward drops in the diode and switch decrease, the efficiency of the system is improved. With variations in input voltage, the efficiency remains relatively constant.

The above calculation for efficiency did not take into account quiescent power dissipation, which decreases efficiency at low current levels when the average input current is of the same magnitude as the quiescent current. It also did not take into account switching losses in the switch and diode or losses in the inductor that tend to reduce efficiency. It does, however, give a good approximation for efficiency, providing a close match with what is asured for the system.

Analysis—Step-Up Operation

Figure 2 illustrates the basic configuration for step-up switching voltage regulator system. The waveforms for this system are shown in *Figure 5*.

To analyze, first assume that just prior to closing S1:

$$i_L = 0$$

When switch S1 is closed, the voltage at point A, which is also the voltage across the switch, is:

$$V_A = V_{SAT}$$

where V_{SAT} is the saturation voltage of the switch.

At this time, the diode is reverse biased and the current through the inductor I_L is increasing at a rate equal to:

$$\frac{di_L}{dt} = \frac{V_L}{L} = \frac{V_{IN} - V_{SAT}}{L}$$

The current through the inductor continues to increase at this rate as long as the switch remains closed and the inductor does not saturate. This rate will be constant if the input voltage remains constant during the on-time of the switch, and the current through the inductor at any instant, while the switch is closed, is given by:

$$i_L = \left(\frac{V_{IN} - V_{SAT}}{L}\right) t$$

The peak current through the inductor, which is dependent on the on-time t_{on} of S1, is given by:

$$I_{PK} = \left(\frac{V_{IN} - V_{SAT}}{L}\right) t_{on}$$

At the end of the on-time, switch S1 is opened. The inductor generates a voltage that forward biases diode D1, providing a current path for the inductor current. The voltage at point A is now:

$$V_A = V_{OUT} + V_D$$

The current through the inductor now begins to decay at a rate equal to:

$$\frac{di_L}{dt} = \frac{V_L}{L} = -\frac{V_{OUT} + V_D - V_{IN}}{L}$$

The current through the inductor and diode at any instant, while the switch is open, is given by:

$$i_L = I_{pk} - \left(\frac{V_{OUT} + V_D - V_{IN}}{L}\right) t$$

Analysis—Step-Up Operation (Continued)

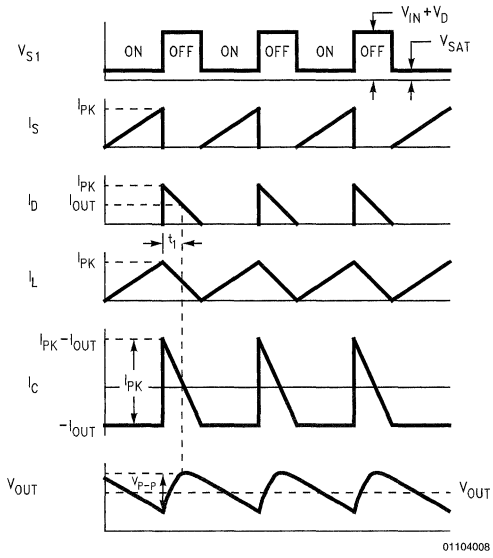


FIGURE 5. Waveforms for Step-Up Mode

Assuming that the current through the inductor reaches zero after the time interval t_{off}, then:

$$I_{pk} = \left(\frac{V_{OUT} + V_D - V_{IN}}{L}\right) t_{off}$$

Thus, the relationship between t_{on} and t_{off} is given by:

$$\frac{t_{on}}{t_{off}} = \frac{V_{OUT} + V_D - V_{IN}}{V_{IN} - V_{SAT}}$$

The above analysis assumes that the output voltage remains relatively constant. For the average output voltage to remain constant, the net charge delivered to the output capacitor must be zero. *Figure 5* (i_D waveform) shows that:

$$\left(\frac{I_{pk}}{2}\right) t_{off} = (t_{on} + t_{off})\, I_{OUT}$$

$$\text{or } I_{pk} = 2\, I_{OUT} \left(\frac{V_{OUT} + V_D - V_{SAT}}{V_{IN} - V_{SAT}}\right)$$

Also for the average output voltage to remain constant, the average current through the diode must equal the output current. The ripple voltage can be calculated using *Figure 5* (i_D waveform) where:

$$t_1 = t_{off} - \left(\frac{I_{OUT}}{I_{pk}}\right) t_{off}$$

During time interval t_1, the output capacitor C_O charges from its minimum value to its maximum value. Therefore:

$$V_{P-P} = \frac{\Delta Q}{C_O} = \frac{1}{C_O}\left(\frac{I_{pk} + I_{OUT}}{2}\right) t_1 - \frac{I_{OUT}\, t_1}{C_O}$$

which simplifies to:

$$V_{P-P} = \frac{(I_{pk} - I_{OUT})^2}{2\, I_{pk}} \left(\frac{t_{off}}{C_O}\right)$$

As with the step-down regulator, this ripple voltage will be increased by the product of the output capacitor's ESR and the ripple current through the capacitor.

To calculate the efficiency of the system:

$$n = \frac{P_{OUT}}{P_{IN}}$$

The input power is given by:

$$P_{IN} = I_{IN}\, V_{IN}$$

The average input current can be calculated from the i_L waveform of *Figure 5*:

$$I_{IN(avg)} = \frac{I_{pk}}{2}$$

The output power is given by:

$$P_{OUT} = I_{OUT}\, V_{OUT}$$

Combining and simplifying the above equations gives an expression for efficiency:

Analysis—Step-Up Operation

(Continued)

$$n = \frac{V_{IN} - V_{SAT}}{V_{IN}} \left(\frac{V_{OUT}}{V_{OUT} + V_D - V_{SAT}} \right)$$

As the forward drops in the diode and switch are reduced, the efficiency of the system improves.

The above calculation did not take into account quiescent power dissipation or switching losses, which will reduce efficiency from the calculated value, it does, however, give a good approximation for efficiency.

Analysis—Inverting Operation

Figure 2 illustrates the basic configuration for an inverting regulator system. The waveforms for this system are shown in *Figure 6*.

To analyze, assume that the following condition is true just prior to turning on the switch:

$$i_L = 0$$

When switch S1 is closed, the voltage at point A is:

$$V_A = V_{IN} - V_{SAT}$$

where V_{SAT} is the saturation voltage of the switch. At this time, diode D1 is reverse biased and the current through the inductor increases at a rate equal to:

$$\frac{di_L}{dt} = \frac{V_L}{L} = \frac{V_{IN} - V_{SAT}}{L}$$

The current through the inductor continues to increase at this rate as long as the switch is closed and the inductor does not saturate. This rate is constant if the input voltage remains constant during the on-time of the switch, and the current through the inductor at any instant, while the switch is closed, is given by.

$$i_L = \left(\frac{V_{IN} - V_{SAT}}{L} \right) t$$

The peak current through the inductor, which is dependent on the on-time t_{on} of S1 is given by:

$$I_{pk} = \left(\frac{V_{IN} - V_{SAT}}{L} \right) t_{on}$$

At the end of the on-time, switch S1 is opened and the inductor generates a voltage that forward biases D1, providing a current path for the inductor current. The voltage at point A is now:

$$V_A \text{ s; } V_{OUT} - V_D$$

The current through the inductor now begins to decay at a rate equal to:

$$\frac{di_L}{dt} = \frac{V_L}{L} = -\left(\frac{V_D - V_{OUT}}{L} \right)$$

The current through the inductor and diode at any given instant, while the switch is open, is given by:

$$i_L = I_{pk} - \left(\frac{V_D - V_{OUT}}{L} \right) t$$

Assuming that the current through the inductor reaches zero after a time interval t_{off}, then:

$$I_{pk} = \left(\frac{V_D - V_{OUT}}{L} \right) t_{off}$$

Analysis shows the relationship between t_{on} and t_{off} to be:

$$\frac{t_{on}}{t_{off}} = \frac{V_D - V_{OUT}}{V_{IN} - V_{SAT}}$$

The previous analysis assumes that the output voltage remains relatively constant For the average output voltage to remain constant, the net charge delivered to the output capacitor must be zero. *Figure 6* (i_D waveform) shows that:

$$\left(\frac{I_{pk}}{2} \right) t_{off} = (t_{on} + t_{off})\, I_{OUT}$$

$$\text{or } I_{pk} = 2\, I_{OUT} \left(\frac{V_{IN} + V_D - V_{OUT} - V_{SAT}}{V_{IN} - V_{SAT}} \right)$$

For average output voltage to remain constant, the average current through the diode must equal the output current.

The ripple voltage can be calculated using *Figure 6* (i_D waveform)·

$$t_1 = t_{off} - \left(\frac{I_{OUT}}{I_{pk}} \right) t_{off}$$

During time interval t_1, the output capacitor C_O charges from its most positive value to its most negative value, therefore:

$$V_{P\text{-}P} = \frac{\Delta Q}{C_O} = \frac{1}{C_O} \left(\frac{I_{pk} + I_{OUT}}{2} \right) t_1 - \frac{I_{OUT}\, t_1}{C_O}$$

which simplifies to:

$$V_{P\text{-}P} = \frac{t_{off}}{C_O} \times \frac{(I_{pk} - I_{OUT})^2}{2\, I_{pk}}$$

This ripple voltage will be increased by the product of the output capacitor's ESR and the ripple current through the capacitor.

To calculate the efficiency of the system:

$$n = \frac{P_{OUT}}{P_{IN}} = \frac{I_{OUT}\, V_{OUT}}{I_{IN}\, V_{IN}}$$

Average input current can be calculated from *Figure 6* (i_S waveform):

$$I_{IN(avg)} = \frac{I_{pk}}{2} \left(\frac{t_{on}}{t_{on} + t_{off}} \right)$$

Analysis—Inverting Operation

(Continued)

Combining and simplifying the previous equations gives an expression for the system efficiency:

$$n = \frac{V_{IN} - V_{SAT}}{V_{IN}} \left(\frac{|V_{OUT}|}{V_D + |V_{OUT}|} \right)$$

Again, as the forward drops in the diode and switch are reduced, the efficiency of the system improves. Also, since switching losses and quiescent current power dissipation are not included in the calculations, efficiency will be somewhat lower than predicted by the above equation.

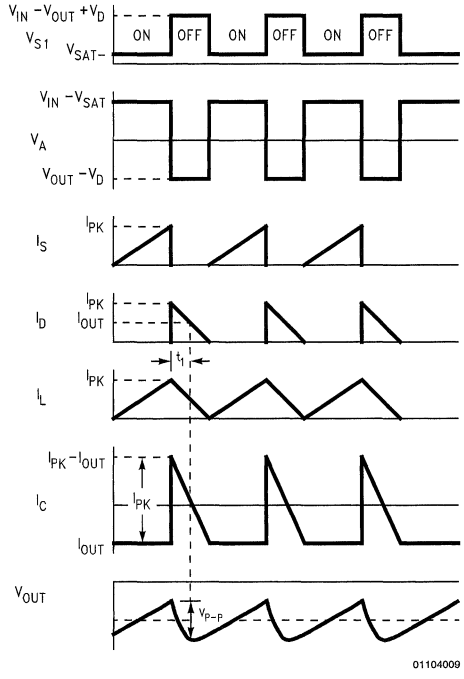


FIGURE 6. Voltage Inverter Waveforms

Analysis—Inverting Operation (Continued)

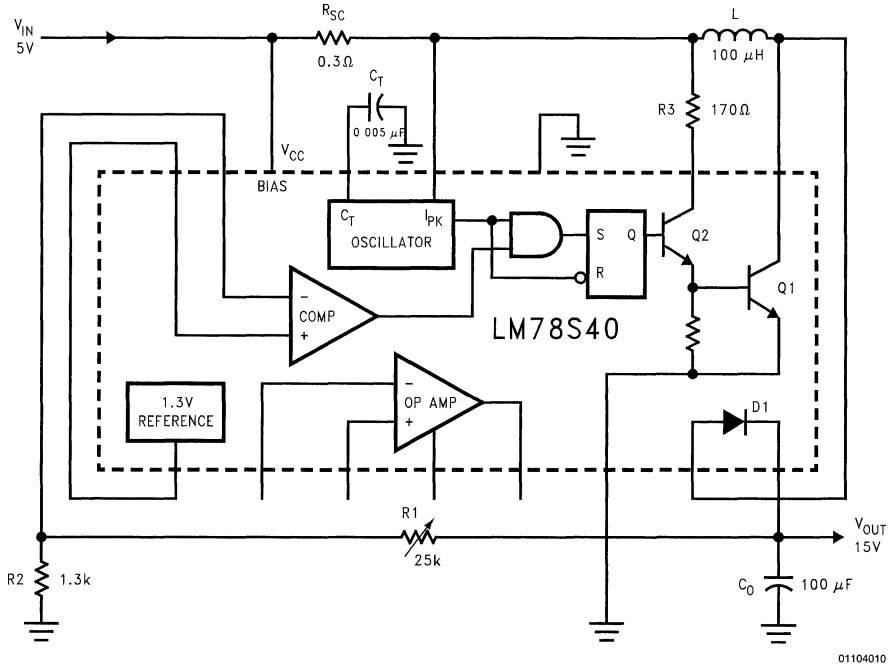


FIGURE 7. Step-Up Voltage Regulator

Design—Step-Up Regulator

A schematic of the basic step-up regulator is shown in *Figure 7.*

Conditions.

V_{IN} = 5V I_{OUT} = 150 mA

V_{OUT} = 15V $V_{RIPPLE} \leq 1\%$

Calculations:

$$I_{pk} = 2\, I_{OUT(max)} \left(\frac{V_{OUT} + V_D - V_{SAT}}{V_{IN} - V_{SAT}} \right)$$

$$I_{pk} = 2\,(0.15) \left(\frac{15 + 1.25 - 0.45}{5 - 0.45} \right) \approx 1\ A$$

Therefore:

$$R_{SC} = \frac{0.3}{I_{pk}} \approx 0.3\Omega$$

To calculate the ratio of t_{on}/t_{off}:

$$\frac{t_{on}}{t_{off}} = \frac{V_{OUT} + V_D - V_{IN}}{V_{IN} - V_{SAT}} = \frac{15 + 1.25 - 5}{5 - 0.45} \approx 1.9$$

$$t_{on} = 1.9\, t_{off}$$

At this point, a value is selected for t_{off}, which in turn defines t_{on}. In making the selection, two constraints must be considered. The first constraint comes from efforts to maintain high efficiency. Rise and fall times should be kept small in comparison to the total period ($t_{on} + t_{off}$) so that only a small portion of the total time is spent in the linear mode of operation, where losses are high. This can be achieved if both t_{on} and t_{off} are made greater than or equal to 10 μs.

The second constraint is due to the techniques used to reduce the effects of the switching mode of operation on external systems. Filtering requirements can be made less stringent by maintaining a high switching frequency, i.e., above 15 or 20 kHz. This condition can be met by specifying the total period, $t_{on} + t_{off}$, to be less than 50 μs.

Therefore, the two design constraints are:

$$t_{on} \geq 10\ \mu s;\ t_{off} \geq 10\ \mu s$$

$$(t_{on} + t_{off}) \leq 50\ \mu s$$

In some cases, both constraints cannot be met and some trade-offs will be necessary.

Following these constraints, value is selected for t_{off}:

$$t_{off} = 10\ \mu s$$

It is now possible to calculate values for the timing capacitor C_T and the inductor L.

The timing capacitor is related (by design) to the off-time by the equation:

$C_T = (45 \times 10^{-5})\, t_{off}$

$C_T = (45 \times 10^{-5})\, 10^{-5} = 4500$ pF

Therefore, set C_T = 5000 pF, which results in:

$$t_{off} \approx 11\ \mu s \text{ and } t_{on} \approx 21\ \mu s$$

Design—Step-Up Regulator

(Continued)

For the inductor

$$L = t_{off}\left(\frac{V_{OUT} + V_D - V_{IN}}{I_{pk}}\right)$$

$$L = (11 \times 10^{-6})\left(\frac{15 + 1.25 - 5}{1}\right) \approx 96\ \mu H$$

The inductor may be designed, using the equations in Appendix A, or purchased. An inductor such as a Delevan 3443-48, rated at 100 µH, is close enough in value for this application.

The output capacitor C_O value can be calculated using the ripple requirement specified:

$$C_O \geq \frac{I_{pk}\,(t_{on} + t_{off})}{8\,V_{RIPPLE}}$$

$$C_O \geq \frac{(1)\,(21 + 11)\,10^{-6}}{(8)\,(150 \times 10^{-3})} \geq 26.6\ \mu F$$

Select C_O to be:

$$C_O = 100\ \mu F$$

to allow for the additional ripple voltage caused by the ESR of the capacitor.

The sampling network, R1 and R2, can be calculated as follows. Assume the sampling network current is 1 mA. Then:

$$R1 + R2 = 15\ k\Omega$$

$$R2 = (R1 + R2)\left(\frac{V_{REF}}{V_{OUT}}\right)$$

$$R2 = (15 \times 10^3)\frac{1.3}{15} = 1.3\ k\Omega$$

Select R2 = 1.3 kΩ and make R1 a 25 kΩ pot that can be used for adjustments in the output voltage.

Note: Sampling current as low as 100 µA can be used without affecting the performance of the system.

R3 is selected to provide enough base drive for transistor Q1. Assume a forced β of 20:

$$I_{C2} \approx I_{B1} = \frac{I_{pk}}{\beta} = \frac{1}{20} = 50\ mA$$

$$R3 \approx \frac{V_{IN} - 1.3}{I_B} = \frac{10 - 1.3}{0.05} = 174\Omega$$

Let R3 = 170Ω.

Using Q1 and Q2 with the external resistor R3 makes it possible to reduce the total power dissipation and improve the efficiency of this system over a system using Q1 and Q2 tied together as the control element. Each application should be checked to see which configuration yields the best performance.

An optional capacitor can be placed at the input to reduce transients that may be fed back to the main supply. The capacitor value is normally in the range of 100 µF to 500 µF, bypassed by a 0.01 µF capacitor.

Applications with peak operating currents greater than 1.5A or higher than 40V require an external transistor and diode as shown in *Figure 8*. This circuit assumes a 15V input and a 70V output.

Design—Step-Up Regulator (Continued)

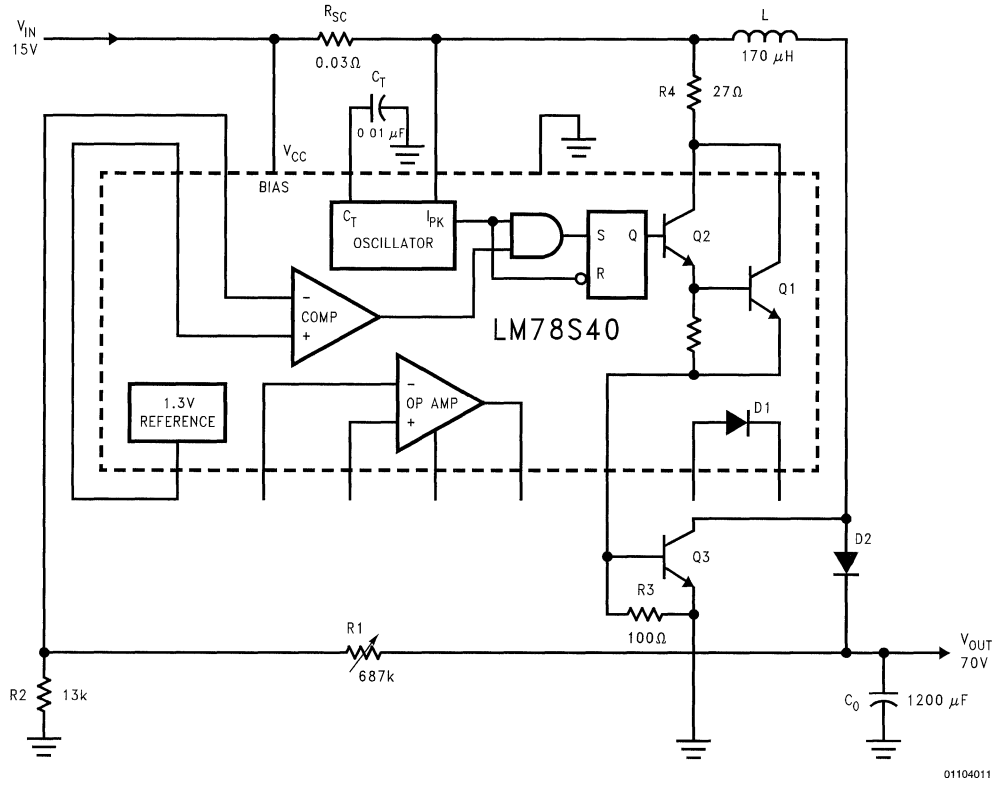


FIGURE 8. Switching Regulator with 15V Input, 70V Output

Design—Step-Down Regulator

A schematic of the basic step-down regulator is shown in *Figure 9.*

Conditions:

V_{IN} = 25V $I_{OUT(max)}$ = 500 mA

V_{OUT} = 10V V_{RIPPLE} < 1%

Calculations:

$I_{pk} = 2\ I_{OUT(max)}$

I_{pk} = 2 (0.5) = 1A

Therefore:

$$R_{SC} = \frac{0.33}{I_{pk}} = 0.33\Omega$$

Next, calculate the ratio of t_{on} to t_{off}:

$$\frac{t_{on}}{t_{off}} = \frac{V_{OUT} + V_D}{V_{IN} - V_{SAT} - V_{OUT}}$$

$$\frac{t_{on}}{t_{off}} = \frac{10 + 1.25}{25 - 1.1 - 10} \approx 0.8$$

$$t_{on} = 0.8\ t_{off}$$

Following design constraints previously discussed, a value is selected for t_{off}:

$$t_{off} = 22\ \mu s$$

$$t_{on} = 18.6\ \mu s$$

Then calculate C_T and L:

$$C_T = (45 \times 10^{-5})\ t_{off}$$

$$C_T = (45 \times 10^{-5})\ (22 \times 10^{-6}) \approx 0.1\ \mu F$$

Design—Step-Down Regulator (Continued)

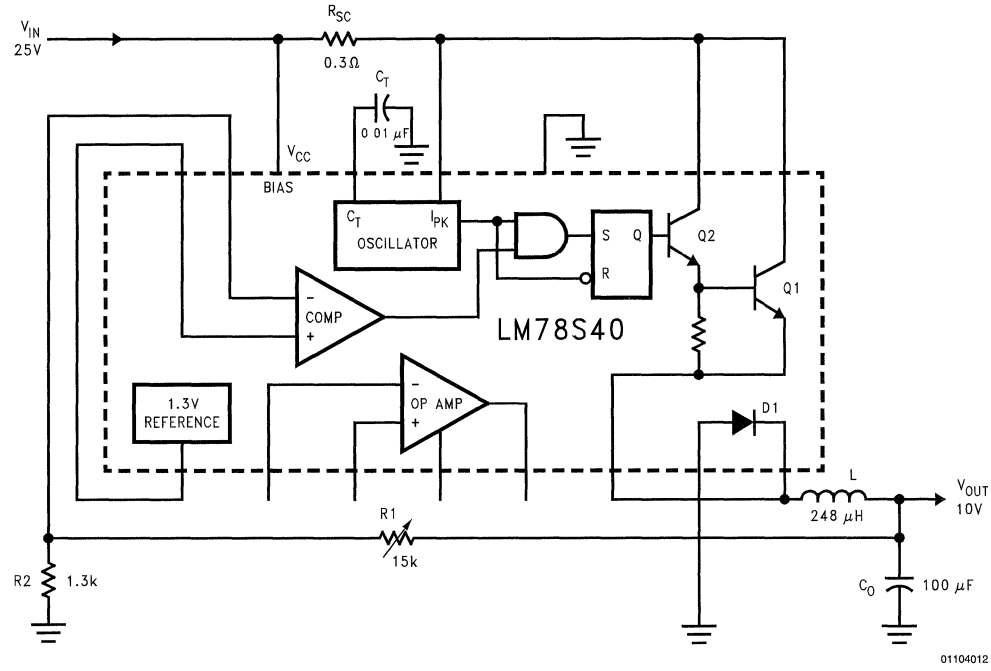


FIGURE 9. Step-Down Voltage Regulator

$$L = \left(\frac{V_{OUT} + V_D}{I_{pk}}\right) t_{off}$$

$$L = \frac{10 + 1.25}{1}(22 \times 10^{-6}) = 248\ \mu H$$

Output capacitor C_O can be calculated from ripple requirements:

$$C_O \geq \frac{I_{pk}\,(t_{on} + t_{off})}{8\,V_{RIPPLE}}$$

$$C_O \geq \frac{(1)\,(18.6 + 22)\,10^{-6}}{(8)\,(0.1)} = 50\ \mu F$$

Select C_O to be:

$$C_O = 100\ \mu F$$

Assuming that the sampling network current is 1 mA, then:

$$R1 + R2 = 10\ k\Omega$$

$$R2 = (R1 + R2)\frac{V_{REF}}{V_{OUT}} = 1.3\ k\Omega$$

Select R2 = 1.3 kΩ and make R1 a 15 kΩ pot that can be used for adjustments in output voltage.

If $I_{pk} \geq 300$ mA, during the off-time when the diode is forward biased, the negative voltage generated at pin 1 causes a parasitic transistor to turn on, dissipating excess power. Replacing the internal diode with an external diode eliminates this condition and allows normal operation.

For applications with peak currents greater than 1A or voltages greater than 40V, an external transistor and diode are required, as shown in *Figure 10*, which assumes a 30V input and a 5V output at 5A.

Design—Step-Down Regulator (Continued)

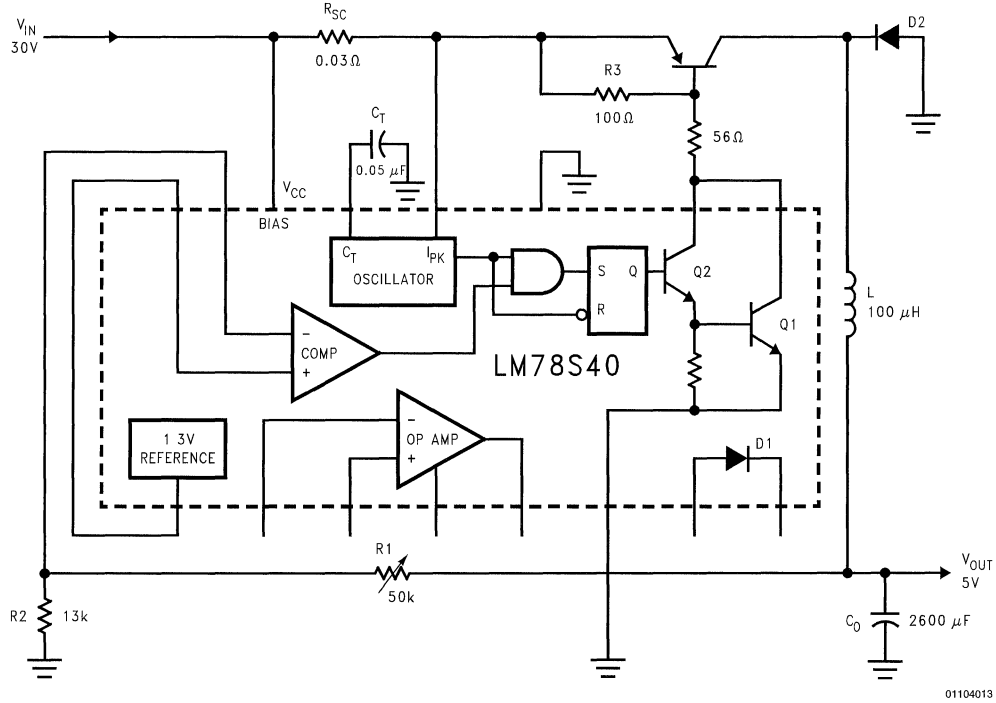


FIGURE 10. Modified Step-Down Regulator with 5A, 5V Output

Design—Inverting Regulator

A schematic of the basic inverting regulator is shown in *Figure 11.*

Conditions:

V_{IN} = 12V $I_{OUT(max)}$ = 500 mA

V_{OUT} = −15V $V_{RIPPLE} \leq 1\%$

Calculations.

$$I_{pk} = 2\, I_{OUT(max)} \left(\frac{V_{IN} + V_D - V_{OUT} - V_{SAT}}{V_{IN} - V_{SAT}} \right)$$

For 2N6051 $V_{SAT} \leq 2V$

$$I_{pk} = 2\,(0.5) \left(\frac{12 + 1.25 + 15 - 2)}{12 - 2} \right) \cong 2.57$$

Therefore:

$$R_{SC} = \frac{0.3}{I_{pk}} \approx 0.1\Omega$$

Calculating the ratio of t_{on} to t_{off},

$$\frac{t_{on}}{t_{off}} = \frac{V_D - V_{OUT}}{V_{IN} - V_{SAT}}$$

$$\frac{t_{on}}{t_{off}} = \frac{1.25 + 15}{10 - 2} \approx 2$$

$$t_{on} = 2\, t_{off}$$

Following design constraints, a value is selected for t_{off}:

$$t_{off} = 10\ \mu s$$

Now, calculate C_T and L:

$C_T = (45 \times 10^{-5})\, t_{off}$

$C_T = (45 \times 10^{-5})\, 10^{-5} = 4500$ pF

Setting C_T = 5000 pF makes $t_{off} \approx 11\ \mu s$ and $t_{on} \approx 22\ \mu s$.

$$L = \left(\frac{V_D - V_{OUT}}{I_{pk}} \right) t_{off}$$

$$L = \left(\frac{1.25 + 15}{2.57} \right) (11 \times 10^{-6}) \approx 70\ \mu H$$

The output capacitor C_O again is calculated:

Design—Inverting Regulator

(Continued)

C_O is selected to be 200 µF.

$$C_O \geq \frac{(I_{pk} - I_O)^2 \, t_{off}}{2 \, I_{pk} \times V_{RIPPLE}}$$

$$C_O \geq \frac{(2.57 - 0.5)^2 \, (11 \times 10^{-6})}{(2)\,(2.57)\,(0.1)} = 97 \, \mu F$$

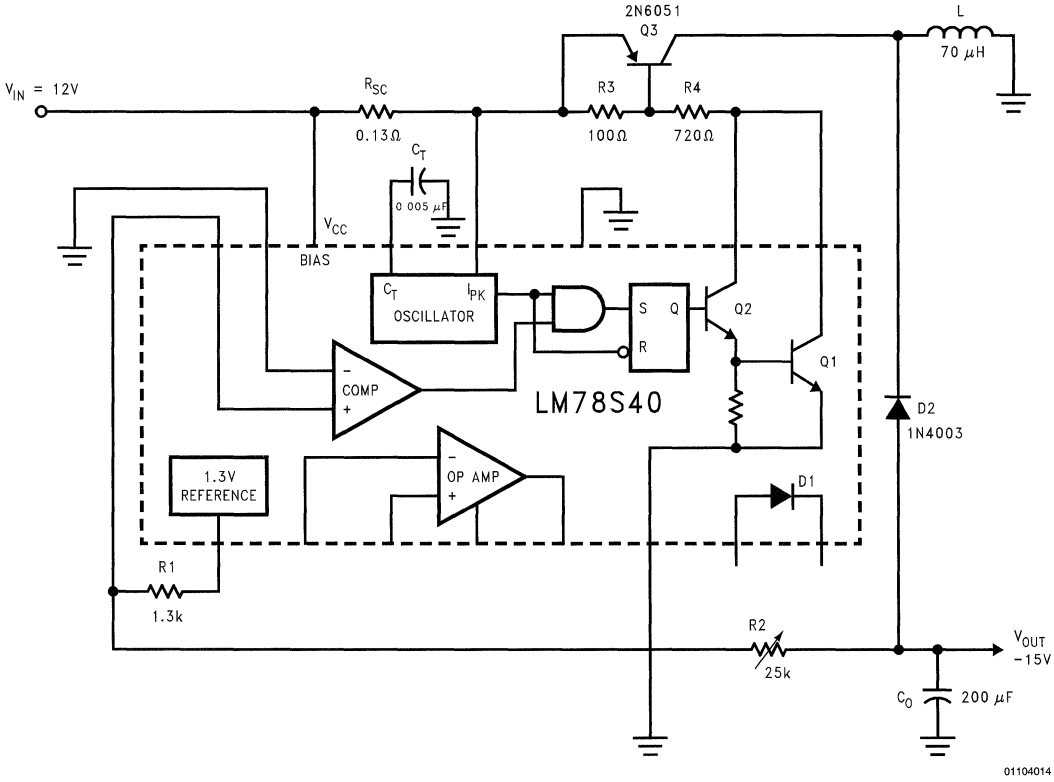


FIGURE 11. Inverting Regulator

The sampling network, R1 and R2, can easily be calculated. Assuming the sampling network current I_S is 1 mA:

$$R_1 = \frac{V_{REF}}{I_S} = 1.3 \, k\Omega$$

$$R_2 = \frac{-V_{OUT}}{I_S} = 15 \, k\Omega$$

Set R1 = 1.3 kΩ and use a 25 kΩ pot for R2 so that output voltage can be adjusted.

This application requires an external diode and transistor since the substrate of the IC is referenced to ground and a negative voltage is present on the output. The external diode and transistor prevent the substrate diodes from a forward-biased condition. See Appendix B for selection of the diode and transistor.

R3 is provided for quick turn-off on the external transistor and is usually in the range of 100Ω to 300Ω. R4 can be calculated as follows:

$$R_4 \approx \frac{V_{IN} - V_{SAT} - V_T - V_{BE}}{I_{pk}/\beta}$$

where:

V_T = threshold voltage = 300 mV

V_{BE} = base emitter drop across the external transistor

$\beta \approx \frac{1}{4} \, h_{FE}$ of the external transistor

If the 2N6051 is used, the value for R4 is:

Design—Inverting Regulator

(Continued)

$$R_4 = \frac{12 - 1.3 - 0.3 - 0.7}{(2.57/190)} \approx 720\Omega$$

Again, an optional capacitor can be placed at the input to reduce transients.

Appendix A
Analysis and Design of the Inductor

To select the proper core for a specific application, two factors must be considered.

The core must provide the desired inductance without saturating magnetically at the maximum peak current. In this respect, each core has a specific energy storage capability LI^2SAT.

The window area for the core winding must permit the number of turns necessary to obtain the required inductance with a wire size that has acceptable D.C. losses in the winding at maximum peak current. Each core has a specific dissipation capability LI^2 that will result in a specific power loss or temperature rise. This temperature rise plus the ambient temperature must not exceed the Curie temperature of the core.

The design of any magnetic circuit is based on certain equations for formulae. *Equation (1)* defines the value of inductance L in terms of basic core parameters and the total number of turns N wound on the core:

$$L = N^2 \times 0\,4\pi\,\mu\,A_e/\ell_e \times 10^{-8} \qquad (1)$$

where:

μ= effective permeability of core

ℓ_e= effective magnetic path length (cm)

A_e= effective magnetic cross section (cm^2)

Equation (2) defines a compound parameter called the inductor index A_L:

$$A_L = 0\,4\pi\,\mu A_e\,\ell_e \times 10 \text{ (mH/1000 turns)} \qquad (2)$$

Combining *Equation (1)* and *Equation (2)*and multiplying by I^2 gives:

$$LI^2 = (NI)^2\,(A_L \times 10^{-6}) \text{ (millijoules)} \qquad (3)$$

Any specific core has a maximum ampere-turn NI capability limited by magnetic saturation of the core material The maximum LI^2SAT of the core can then be calculated from *Equation (3)* or, if the saturation flux density B_{SAT} is given, from *Equation (4)*:

$$LI^2 = \frac{(B_{SAT})^2\,(A_e^2 \times 10^{-4})}{A_L} \text{ (millijoules)} \qquad (4)$$

(4)

The core selected for an application must have an LI^2SAT value greater than calculated to insure that the core does not saturate under maximum peak current conditions.

In switching regulator applications, power dissipation in the inductor is almost entirely due to D.C. losses in the winding. The dc resistance of the winding R_w can be calculated from *Equation (5)*:

$$R_w = P(\ell_w/A_w)\,N \quad (5) \qquad (5)$$

where

P= resistivity of wire (Ω/cm)

ℓ_w= length of turn (cm)

A_w= effective area of wire (cm^2)

Core geometry provides a certain window area A_c for the winding. The effective area A'_c is 0.5 A_c for toroids and 0.65 A_c for pot cores relates the number of turns, area of wire, and effective window area of a fully wound core.

$$A_w = A'_c/N \ (cm^2) \qquad (6)$$

By combining *Equation (5)* and *Equation (6)* and multiplying each side by I^2, the power dissipation in the winding P_w can be calculated.

$$P_w = I^2R_w = I^2P\left(\frac{\ell_w}{A'_c}\right)N^2 \qquad (7)$$

(7)

Substituting for N and rearranging:

$$LI^2 = P_w\left(\frac{A_L A'_c}{P\,\ell_w}\right) \times 10^{-6} \text{ (millijoules)} \qquad (8)$$

(8)

Equation (8) shows that the LI^2 capability is directly related to and limited by the maximum permissible power dissipation. One procedure for designing the inductor is as follows:

1. Calculate the inductance L and the peak current I_{pk} for the application. The required energy storage capability of the inductor $LI_{pk}2$ can now be defined.
2. Next, from Equation 3 or 4, calculate the maximum LI^2SAT capability of the selected core, where
   $$LI^2SAT > LI_{pk}2$$
3. From Equation 1, calculate the number of turns N required for the specified inductance L, and finally, from Equation 7, the power dissipation P_w. P_w should be less than the maximum permissible power dissipation of the core
4. If the power losses are unacceptable, a larger core or one with a higher permeability is required and steps 1 through 3 will have to be repeated.

Several design cycles are usually required to optimize the inductor design With a little experience, educated guesses as to core material and size come close to requirements.

Appendix B
Selection of Switching Components

The designer should be fully aware of the capabilities and limitations of power transistors used in switching applications. Transistors in linear applications operate around a quiescent point; whereas in switching applications operation is fully on or fully off Transistors must be selected and tested to withstand the unique stress caused by this mode of operation. Parameters such as current and voltage ratings, secondary breakdown ratings, power dissipation, saturation voltage and switching times critically affect transistor performance in switching applications. Similar parameters are important in diode selection, including voltage, current, and power limitations, as well as forward voltage drop and switching speed.

Initial selection can begin with voltage and current requirements. Voltage ratings of the switching transistor and diode must be greater than the maximum input voltage, including

Appendix B Selection of Switching Components (Continued)

any transient voltages that may appear at the input of the switching regulator. Transistor saturation voltage $V_{CE(SAT)}$ and diode forward voltage V_D at full load output current should be as low as possible to maintain high operating efficiency. The transistor and diode should be selected to handle the required maximum peak current and power dissipation.

Good efficiency requires fast switching diodes and transistors. Transistor switching losses become significant when the combined rise t_r plus fall time t_f exceeds:

$$0.05\ (t_{on} + t_{off})$$

For 20 kHz operation, $t_r + t_f$ should be less than 2.5 µs for maximum efficiency. While transistor delay and storage times do not affect efficiency, delays in turn-on and turn-off can result in increased output voltage ripple. For optimal operation combined delay time t_d plus storage time t_s should be less than:

$$0.05\ (t_{on} + t_{off})$$

Appendix C Selection of Output Filter Capacitors

In general, output capacitors used in switching regulators are large (>100 µF), must operate at high frequencies (>20 kHz), and require low ESR and ESL. An excellent trade-off between cost and performance is the solid-tantalum capacitor, constructed of sintered tantalum powder particles packed around a tantalum anode, which makes a rigid assembly or slug. Compared to aluminum electrolytic capacitors, solid-tantalum capacitors have higher CV product-per-unit volume, are more stable, and have hermetic seals to eliminate effects of humidity.

Appendix D EMI

Due to the wiring inductance in a circuit, rapid changes in current generate voltage transients. These voltage spikes are proportional to both the wiring inductance and the rate at which the current changes:

$$V = L\frac{di}{dt}$$

The energy of the voltage spike is proportional to the wiring inductance and the square of the current:

$$E = 1/2\ LI^2$$

Interference and voltage spiking are easier to filter if the energy in the spikes is low and the components predominantly high frequency.

The following precautions will reduce EMI:

- Keep loop inductance to a minimum by utilizing appropriate layout and interconnect geometry.
- Keep loop area as small as possible and lead lengths small and, in step-down mode, return the input capacitor directly to the diode to reduce EMI and ground-loop noise.
- Select an external diode that can hold peak recovery current as low as possible. This reduces the energy content of the voltage spikes.

Appendix E Design Equations

LM78S40 Design Formulae

Characteristic	Step Down	Step Up	Inverting
I_{pk}	$2\ I_{OUT(max)}$	$2\ I_{OUT(max)}\left(\frac{V_{OUT} + V_D - V_{SAT}}{V_{IN} - V_{SAT}}\right)$	$2\ I_{OUT(max)}\left(\frac{V_{IN} + \lvert V_{OUT}\rvert + V_D - V_{SAT}}{V_{IN} - V_{SAT}}\right)$
R_{SC}	$0.33\ \frac{I_{pk}}{}$	$0.33\ \frac{I_{pk}}{}$	$0.33\ \frac{I_{pk}}{}$
$\frac{t_{on}}{t_{off}}$	$\frac{V_{OUT} + V_D}{V_{IN} - V_{SAT} - V_{OUT}}$	$\frac{V_{OUT} + V_D - V_{IN}}{V_{IN} - V_{SAT}}$	$\frac{\lvert V_{OUT}\rvert + V_D}{V_{IN} - V_{SAT}}$
L	$\left(\frac{V_{OUT} + V_D}{I_{pk}}\right) t_{off}$	$\left(\frac{V_{OUT} + V_D - V_{IN}}{I_{pk}}\right) t_{off}$	$\left(\frac{\lvert V_{OUT}\rvert + V_D}{I_{pk}}\right) t_{off}$
t_{off}	$\frac{I_{pk}\ L}{V_{OUT} + V_D}$	$\frac{I_{pk}\ L}{V_{OUT} + V_D - V_{IN}}$	$\frac{I_{pk}\ L}{\lvert V_{OUT}\rvert + V_D}$
$C_{T\ (\mu F)}$	$45 \times 10^{-5}\ t_{off}(\mu s)$	$45 \times 10^{-5}\ t_{off}(\mu s)$	$45 \times 10^{-5}\ t_{off}(\mu s)$

Appendix E
Design Equations (Continued)

LM78S40 Design Formulae (Continued)

Characteristic	Step Down	Step Up	Inverting
C_O	$\frac{I_{pk}\,(t_{on} + t_{off})}{8\,V_{RIPPLE}}$	$\frac{(I_{pk} - I_{OUT})^2\,t_{off}}{2\,I_{pk}\,V_{RIPPLE}}$	$\frac{(I_{pk} - I_{OUT})^2\,t_{off}}{2\,I_{pk}\,V_{RIPPLE}}$
Efficiency	$\left(\frac{V_{IN} - V_{SAT} + V_D}{V_{IN}}\right)\frac{V_{OUT}}{V_{OUT} + V_D}$	$\frac{V_{IN} - V_{SAT}}{V_{IN}}\left(\frac{V_{OUT}}{V_{OUT} + V_D - V_S}\right)$	$\left(\frac{\lvert V_{OUT}\rvert}{V_D + \lvert V_{OUT}\rvert}\right)$
$I_{IN(avg)}$ (Max load condition)	$\frac{I_{pk}}{2}\left(\frac{V_{OUT} + V_D}{V_{IN} - V_{SAT} + V_D}\right)$	$\frac{I_{pk}}{2}$	$\frac{I_{pk}}{2}\left(\frac{\lvert V_{OUT}\rvert + V_D}{V_{IN} + \lvert V_{OUT}\rvert + V_D - V_{SAT}}\right)$

Note 1: V_{SAT} — Saturation voltage of the switching element V_D — Forward voltage of the flyback diode

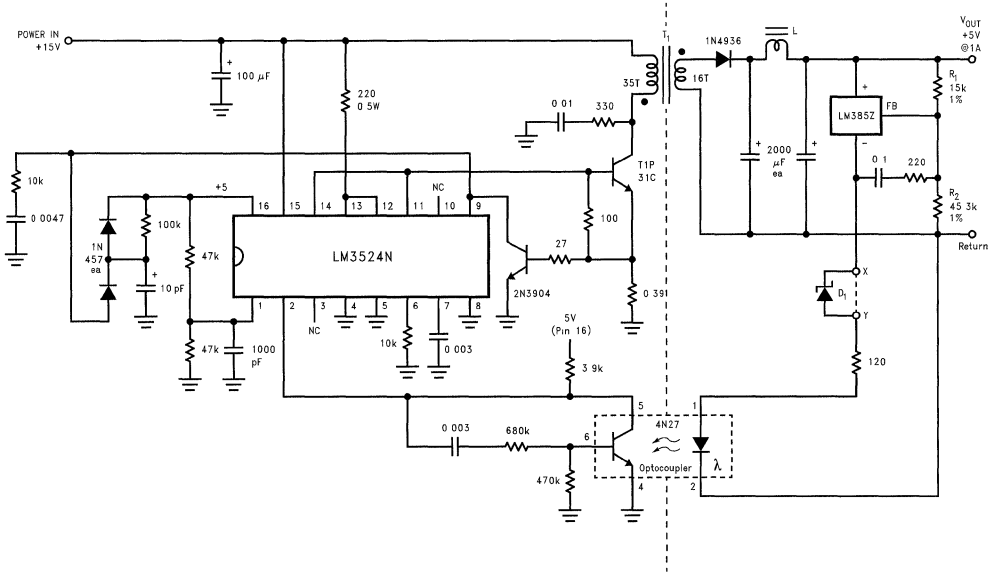
LM385 Feedback Provides Regulator Isolation

National Semiconductor
Application Note 715
Robert Pease
Fran Hoffart

You can use a conventional 4N27 optocoupler in a feedback arrangement (*Figure 1*) to design a switching regulator with a floating output. The LM3524 switch-mode-regulator IC is configured as a simple flyback power supply with transformer-isolated output. The LM385 acts as a reference and comparison amplifier that satisifes the 4N27's current demands for balancing the dc feedback to pin 2 of the LM3524, thereby closing the loop. The LM385 automatically compensates for any LED degradation or optical-coupling loss.

The 4N27 specs a 0.1 dc to 1.6 dc gain range; the ac gain varies from 0.05 to 1.0. Fortunately, the "Miller" damper from pins 5 to 6 nullifies the effect of the wide gain variance. Moreover, the damper provides excellent loop stability for a wide range of 4N27 optocouplers from several manufacturers. In the example shown, the LM385 provides 0.5 mA to 5 mA to the optocoupler.

If the 5V output available from this circuit does not meet your needs, choose $R_2 = R_1 (V_{OUT} - 1.25)/1.25$. If V_{OUT} is greater than 6V, insert a zener diode between points X and Y, with $V_Z = V_{OUT} - 5V$; this addition prevents the voltage across the LM385 from exceeding its 5.3V max limit. The circuit is suitable for regulated output voltages from 3.2V to 25V.



L = 15 turns #22 wire wrapped on ½W resistor body

D_1 = optional (see text)

FIGURE 1. Optocoupler-based feedback circuit produces galvanically-isolated, regulated voltages. The heavy negative feedback compensates for wide variations in optocoupler gains. The values portrayed in this schematic yield 5V output; by varying R_2, you can obtain voltages from 3.2V to 25V.

20 Watt Simple Switcher Forward Converter

National Semiconductor
Application Note 776
Frank DeStasi
Tom Gross

A 20W, 5V at 4A, step-down regulator can be developed using the LM2577 Simple Switcher IC in a forward converter topology. This design allows the LM2577 IC to be used in step-down voltage applications at output power levels greater than the 1 A LM2575 and 3 A LM2576 buck regulators. In addition, the forward converter can easily provide galvanic isolation between input and output.

The design specifications are:

V_I Range	20V–24V
V_o	5V
$I_{o(max)}$	4A
ΔV_o	20 mV

With the input and output conditions identified, the design procedure begins with the transformer design, followed by the output filter and snubber circuit design.

Transformer Design

1. Using the maximum switch voltage, input voltage, and snubber voltage, the transformer's primary-to-clamp windings turns ratio is calculated:

$$V_{SW} \geq V_{imax} + V_{imax}\,(N_p/N_c) + V_{snubber}$$
$$N_p/N_c \leq (V_{SW} - V_{imax} - V_{snubber})/V_{imax}$$
$$N_p/N_c \leq (60V - 24V - 5V)/24V = 1.29$$
$$\Delta \text{ let } N_p/N_c = 1.25$$

The $V_{snubber}$ voltage is an estimate of the voltage spike caused by the transformer's primary leakage inductance.

2. The duty cycle, t_{on}/T, of the switch is determined by the volt-second balance of the primary winding.

During t_{on};

$$V_I = L_p\,(\Delta i/T_{ON}) \rightarrow \Delta i = (V_I/L_P)\,t_{on}$$

During t_{off};

$$V_I = (N_p/N_c) = L_p\,(\Delta i/t_{off}) \rightarrow \Delta I = (N_p/N_c)\,(V_I/L_p)\,t_{off}$$

Setting Δi's equal;

$$(V_I/L_p)\,t_{on} = (N_p/N_c)\,(V_I/L_p)\,t_{off}$$
$$t_{on}/t_{off} = N_p/N_c$$
$$\text{Since D} = t_{on}/T = t_{on}/(t_{on} + t_{OFF})$$
$$\text{max. duty cycle} = D_{max} = (N_p/N_c)/\,[(N_p/N_c) + 1]$$
$$D_{max} = (1.25)/\,(1.25 + 1) = 0.56\ (56\%)$$

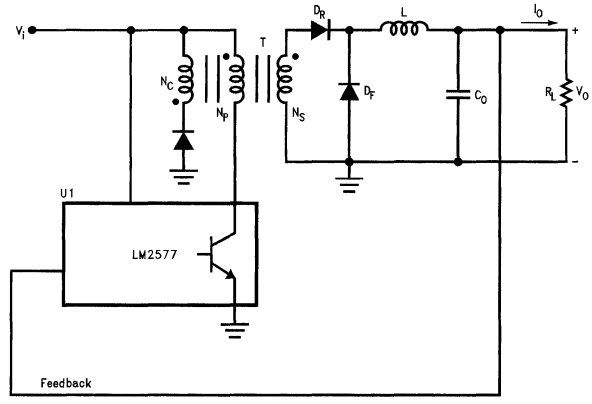
3. The output voltage equations of a forward converter provides the transformer's secondary-to-primary turns ratio:

$$V_o + V_{diode} \leq V_{imin} \times D_{max}\,(N_s/N_p)$$
$$N_s/N_p \geq (V_o + V_{diode})/\,(V_{imin} \times D_{max})$$
$$N_s/N_p \geq (5.5V)/(20V)(56\%) = 0.49$$
$$\Delta \text{let } N_s/N_p = 0.5$$

4. Calculate transformer's primary inductance by finding the maximum magnetizing current (Δi_{Lp}) that does not allow the maximum switch current to exceed it's 3 A limit (capital I for DC current, Δi for AC current, and lower case i for total current):

$$i_{sw} = i_{pri} = i_{Lo'} + \Delta i_{Lp}$$

Basic Forward Converter



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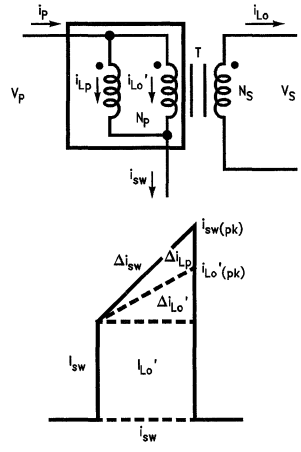
where $i_{Lo'}$ is the reflected secondary current and Δi_{LP} is the primary inductance current.

$$i_{Lo'} = i_{Lo}(N_s/N_p) \quad (i_{Lo} \text{ reflected to primary})$$
$$i_{Lo} = I_{Lo} \pm \Delta i_{Lo}/2$$
$$\Delta i_{Lo} \text{ is the output inductor's ripple current}$$
$$I_{Lo} = I_o \text{ (the load current)}$$

$$i_{Lo'} = (I_o \pm \Delta i_{Lo}/2)(N_s/N_p)$$
$$i_{Lo'(pk)} = (I_{o(max)} + \Delta i_{Lo}/2)(N_s/N_p)$$
$$i_{sw} = I_{sw} + \Delta i_{sw}$$
$$i_{sw(pk)} = i_{Lo'(pk)} + \Delta i_{Lp(pk)}$$
$$i_{sw(pk)} = (I_{o(max)} + \Delta i_{Lo}/2)(N_s/N_p) + \Delta i_{Lp(pk)}$$

Transformer Design (Continued)



Using standard inductors, a good practical value to set the output inductor current (Δi_{Lo}) to is 30% of the maximum load current (I_o). Thus;

$$i_{sw(pk)} = (I_{o(max)} + 0.15\Delta i_{Lo})(N_s/N_p) + \Delta i_{LP(pk)}$$

$$\Delta i_{LP(pk)} = i_{sw(pk)} - (I_{o(max)} + 0.15\Delta i_{Lo})(N_s/N_p)$$

$$\Delta i_{LP(pk)} = 3A - (4A + 0.15 \times 4A)(0.5) = 0.7A$$

$$L_p = V_{pri} \times \Delta t/\Delta i = (V_i - V_{sat})(t_{on}/\Delta i_{LP(pk)})$$

$$= (V_{i(max)} - V_{sat})(D_{max}/(\Delta i_{LP(pk)} \times f)$$

$$= (24V - 0.8V)(0.56/0.7 \times 52\ kHz)$$

$$L_p = 357\ \mu H$$

$$\Delta let\ L_p = 350\ \mu H$$

Output Filter—Inductor

The first component calculated in the design is the output inductor, using the current-to-voltage relationship of an inductor:

$$V_L = L_o\ (\Delta i_{Lo}/t_{on})$$

Choosing an inductor ripple current value of $0.3I_o$ and a maximum output current of 4A:

$$\Delta i_{Lo} = 0.3\ (4A) = 1.2A$$

During t_{on};

$$V_L = V_S - V_D - V_o\ [\text{where } V_s = (V_i - V_{sat})(N_s/N_p)]$$

Thus,

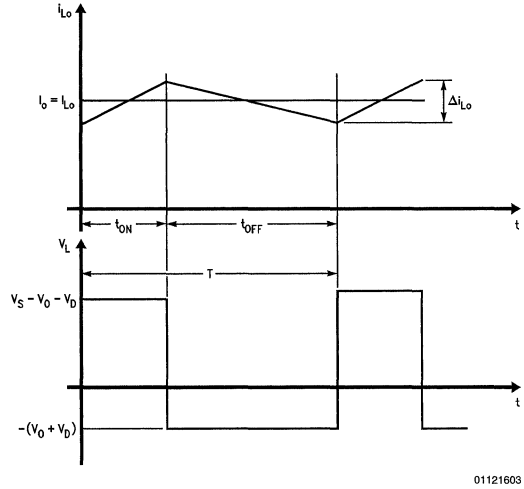
$$[(V_i - V_{sat})(N_s/N_p) - V_d - V_o] = L_o\ (\Delta i_{Lo}/D)\ f$$

$$L_o = [(V_i - V_{sat})(N_s/N_p) - V_d - V_o] \times D/\Delta i_{Lo} \times f$$

$$L_o = [(24V - 0.8V)(0.5) - 0.5V - 5V]\ 56\%/1.2A \times 52\ kHz$$

$$L_O = 55\ \mu H$$

$$\Delta\ let\ L_o = 60\ \mu H$$



Output Filter—Capacitor

Since the output capacitor's current is equal to inductor's ripple current, the output capacitor's value can be found using the inductor's ripple current. Starting with the current-voltage relationship, the output capacitance is calculated:

$$\Delta V_o = 1/C_o \int i\ dt$$

$$= \Delta i_{Lo}/\ 4C_o\ (TR/2)$$

$$= (\Delta i_{Lo} \bullet T)/\ 8C_o$$

$$C_o = (\Delta i_{Lo} \bullet T)/\ 8\Delta V_o$$

However, the equivalent series resistance (ESR) of the capacitor multiplied by the inductor's ripple current creates a parasitic output ripple voltage equal to:

$$\Delta V_o = ESR_{co} \bullet \Delta i_{Lo} = ESR_{co} \bullet 0.3\ I_o$$

This parasitic voltage is usually much larger than the inherent ripple voltage. Hence, the output capacitor parameter of interest, when calculating the output ripple voltage, is the equivalent series resistance (the capacitance of the output capacitor will be determined by the frequency response analysis). Using a standard-grade capacitor with ESR of 0.05Ω produces a total output ripple voltage of:

Output Filter—Capacitor (Continued)

$$\Delta V_o = 0.05\Omega \bullet 1.2A \cong 60\ mV$$

To get output ripple voltage of 20 mV or less (as was part of the design specs) requires a capacitor with ESR of less than 17 mΩ.

Snubber Circuit

A snubber circuit (C_S, R_S, D_S) is added to reduce the voltage spike at the switch, which is caused by the transformer's leakage inductance. It is designed as follows: when the switch is off,

$$V_R = V_{CE} - V_{IN} - V_D$$

$$V_{LL} = V_D + V_R - V_{IN}(N_p/N_c)$$

Substituting for V_R, the voltage across the leakage inductance, V_{LL}, is,

$$V_{LL} = V_{CE} - V_{IN}(1 + N_p/N_c)$$

Using the current-voltage relationship of inductors,

$$t_S = I_{PRI}(L_L/V_{LL})$$

Substituting for V_{LL},

$$t_S = I_{PRI}\ L_L/(V_{CE} - V_{IN}(1 + N_p/N_c))$$

Calculating for the average leakage inductance current, $I_{L\text{-}L(AVE)}$,

$$I_{LL(AVE)} = I_{PRI(MAX)}\ (t_S)/2T$$

$$= I_{PRI(MAX)}{}^2\ L_L f/2(V_{CE} - V_{IN}(1 + N_p/N_c))$$

Solving for the snubber resistor;

$$R_S = V_R/I_{LL(AVE)}$$

Substituting $I_{LL(AVE)}$ and V_R results in,

$$R_S = 2\ (V_{CE} - V_{IN}(1 + N_p/N_c))\ X$$

$$(V_{CE} - V_{IN} - V_D)/(L_L\ (I_{PRI(MAX)})^2 f)$$

Choosing L_L to equal 10% of L_p,

$$R_S = 2\ (65V - 24V - 1V)\ X\ (65V - 24V(2.25))/$$

$$(7\ \mu H\ (3A)^2\ 52\ kHz)$$

$$= 268.9\Omega \cong 270\Omega$$

Using the current-voltage relationship of capacitors,

$$\Delta V_R = (T - t_S)\ I_C/C_S = (T - t_S)\ V_R/R_S C_S \cong V_R/R_S C_S f$$

The capacitor C_S equates to,

$$C_S = V_R/R_S\ f\ \Delta V_R$$

$$C_S = 40V/(270\Omega)(52\ kHz)\ 10V = 0.28\ \mu F \cong 0.33\ \mu F$$

The snubber diode has a current rating of 1A peak and a reverse voltage rating of 30V.

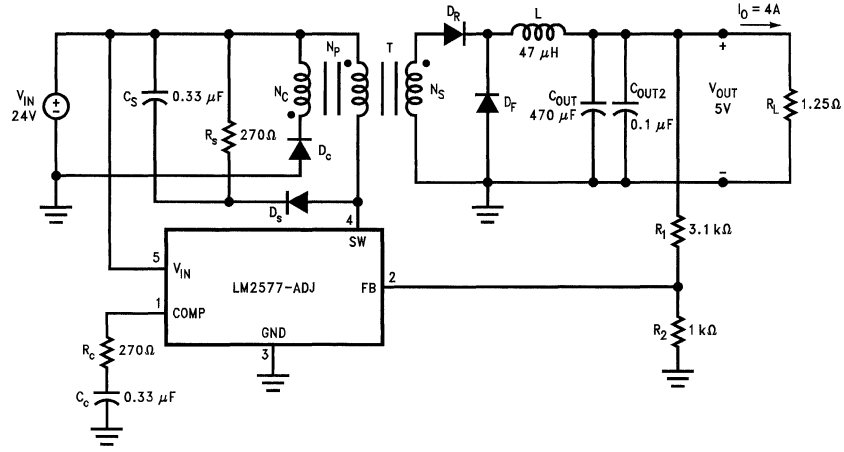
Other Components

Diodes, D_R and D_F, used in the secondary are 5A, 30V Schottky diodes. The same diode type is used for D_c, however a lower current diode could have been used.

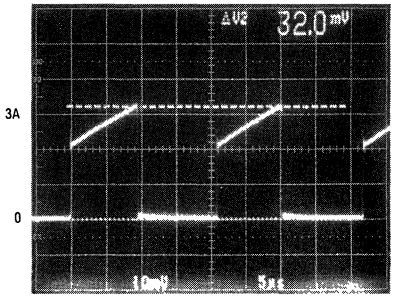
A compensation network of R_c and C_c optimizes the regulator's stability and transient response and provides a soft-start function for a well-controlled power-up.

The finished circuit is shown below.

5V, 4 A Forward Converter Circuit Schematic



Other Components (Continued)



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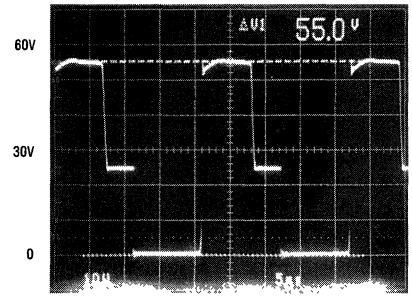
Vertical: 1 A/div
Horizontal: 5 µs/div

Switch Current



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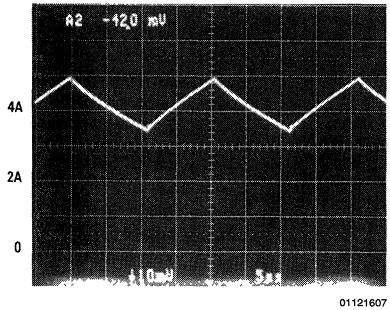
Vertical 10 V/div
Horizontal 5 µs/div

Switch Voltage



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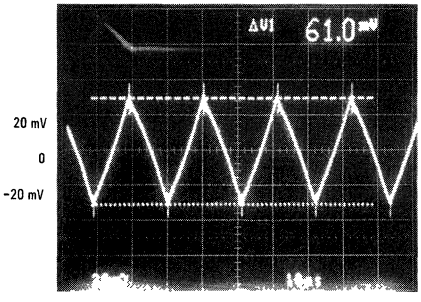
Vertical: 1 A/div
Horizontal 5 µs/div

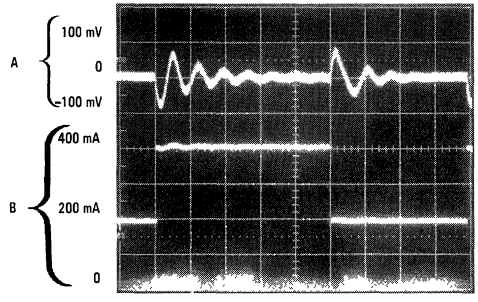
Inductor Current



01121608

Vertical. 20 mV/div
Horizontal 10 µs/div

Output Ripple Voltage



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A Output Voltage Change, 100 mV/div
B: Output Current, 200 mA/div
Horizontal 10 ms/div

Load Step Response

LM2577 Three Output, Isolated Flyback Regulator

National Semiconductor
Application Note 777
Tom Gross

Many voltage regulator applications require multiple outputs, such as a computer's power supply or a regulator used to meet the voltage requirements inside an automobile. Some of these applications require isolation between the regulator's input and output for protection and separate ground specifications. Using this criteria, a LM2577 simple switcher flyback regulator has been designed with multiple (3) outputs and input-to-output isolation. The three outputs are: 1) 5V @ 150 mA, 2) 7.5V @ 100 mA, and 3) −7.5V @ 70 mA. The table below gives the electrical specifications.

The LM2577 flyback regulator uses a 4N27 optocoupler to provide a galvanic isolation. The base resistor of the optocoupler is chosen so that it is large enough (47 kΩ) to supply a minimum base current—which in turn, demands a lower drive current to the optocoupler's diode—but not so large as to produce a pole in the regulator's frequency response. If the pole's frequency is below the regulator loop's crossover frequency, stability problems will occur. Thus, a zero must be developed, requiring extra circuitry, to compensate for the extra pole in the loop.

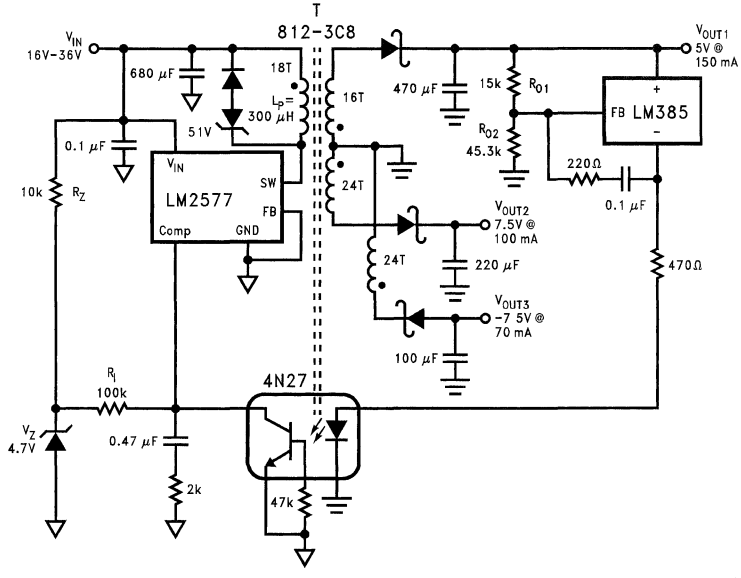
An LM385 Adjustable Voltage Reference, along with resistors R_{O1} and R_{O2}, set the main output voltage to 5V ±4% by the equation: $V_O = 1.24V\ (1 + R_{O2}/R_{O1})$. The LM385 supplies a drive current to the optocoupler (about 10 mA) proportional to the output voltage. Due to the high gain of the LM385, the LM2577's error amplifier is bypassed, and the feedback signal is fed directly to the compensation pin. Employing the error amplifier's gain block in the loop would add with the LM385 gain (the optocoupler's gain is around unity) to produce a very large overall loop gain. Such a large loop gain makes the loop too difficult to stabilize—thus the bypassed error amplifier. With the regulator input voltage of 26V and full load on all outputs, the frequency response has a crossover frequency at 1 kHz and phase margin of 90°.

The flyback regulator's mode of operation is continuous, so a large primary inductance (L_P = 300 µH) is needed for the transformer. Using a Ferroxcube 812E250-3C8 E core, the primary winding requires about 50 turns. With the turnsratios as they are shown on the schematic and the small core size, the transformer windings must be wound tightly so that they fit the core windows. Interlaying the primary winding between the secondary windings improves the transformers coupling.

The zener diode circuit (V_Z, R_Z, R_I) is added to provide the optocoupler transistor with about 20 µA of bias current, on top of the current sourced from the compensation pin (about 7 µA). The isolation resistor, between the compensation pin and the zener diode, needs to be as large as 100 kΩ, or at start-up, the compensation pin will see too large a voltage, turning the power switch fully on—thus forcing the LM2577 into current limit. Also, to ensure good line regulation, the dynamic impedance of the zener diode must be very good.

Test data for this regulator follows the schematic. Since feedback is taken from Output 1, its load and line regulation are better than that of the other two outputs, which rely on feedback through the transformer coupling. The output ripple voltage of all three outputs is largely dependent on the filter capacitors used, and could be reduced by the use of additional high-quality filter capacitors or an additional L-C filter section.

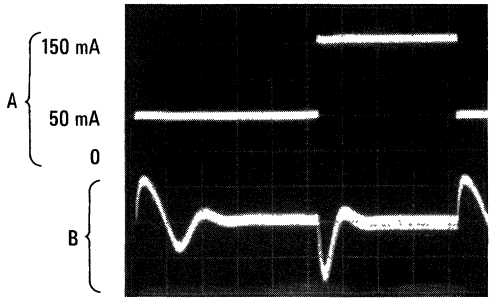
LM2577 Three Output, Isolated Flyback Regulator



ELECTRICAL TEST DATA

V_I = 16V–36V

Output Voltages	Line Regulation (I_O = Full Load)	Load Regulation (V_I = 26V)	Output Ripple Voltage (T_A = 25˚C)
V_{O1} = 5V	0.2%	0.04% 30 mA–150 mA	50 mV
V_{O2} = 7.5V	0.3%	3% 20 mA–100 mA	50 mV
V_{O3} = 7.5V	0.3%	2% 12 mA–70 mA	50 mV



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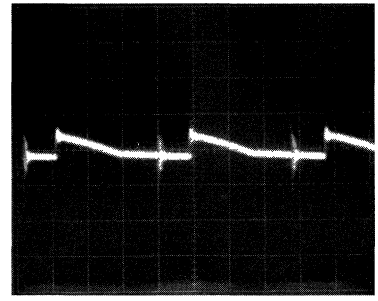
Load Transient Response
A. Load Current, 50 mA/div
B. Output Voltage Change 50 mV/div (AC-Coupled)
Horizontal: 5 ms/div



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Output Ripple Voltage
20 mV/div (AC-Coupled)
Horizontal: 5 ms/div

Increasing the High Speed Torque of Bipolar Stepper Motors

National Semiconductor
Application Note 828
Steven Hunt

Introduction

To successfully follow a velocity profile, a motor and drive combination must generate enough torque to: accelerate the load inertia at the desired rates, and drive the load torque at the desired speeds. While the size of a bipolar stepper motor generally dictates the low speed torque, the ability of the drive electronics to force current through the windings of the motor dictates the high speed torque. This application note shows that increasing the slew rates of the winding currents in a bipolar stepper motor pushes the motor to deliver more torque at high speeds. Simple voltage drives, L/R drives, and chopper drives are explained. L/R drives and chopper drives achieve slew rates higher than those achieved by simple voltage drives. Finally, an example chopper drive is presented.

Background

In standard full-step operation, quadrature (out of phase by 90°) bipolar currents (*Figure 1*) energize the windings of a bipolar stepper motor. One step occurs at each change of direction of either winding current, and the motor steps at four times the frequency of the currents. The ideal winding currents of *Figure 1* exhibit infinite slew rates.

Ideally, each phase contributes a sinusoidal torque;

$$T_1 = -i_1\ T\sin(N\theta) \text{ and} \quad (1)$$

$$T_2 = i_2\ T\cos(N\theta), \quad (2)$$

with the winding currents, i(t), in amps and the torque constants, -Tsin(N•θ) and Tcos(N•θ), in newton•centimeters per amp. θ represents the angular displacement of the rotor relative to a stable detent (zero torque) position. N represents the number of motor poles; that is, the number of electrical cycles per mechanical cycle or revolution. N•θ, therefore, represents the electrical equivalent of the mechanical rotor position. The torque contributions add directly to yield a total torque of

$$T_t = T_1 + T_2 = T\,(i_2 \cos(N\theta) - i_1 \sin(N\theta)). \quad (3)$$

Integrating (3) over a full period of one of the torque constants and multiplying the result by the reciprocal of that period gives the average torque generated by the motor. Assuming ideal square wave winding currents and sinusoidal torque constants (*Figure 2*), the motor generates an average torque of

$$T_{avg} = \frac{1}{2\pi}\left[\int_0^{2\pi} -i_1\ T\sin(N\theta)\ dN\theta + \int_0^{2\pi} i_2\ T\cos(N\theta)\ d\,N\theta\right] = \quad (4)$$

$$= \frac{2}{\pi} I_{rated}\ T\cos\phi. \quad (5)$$

In open loop applications, φ adjusts automatically to match the average torque generated by the motor with that required to execute a motion task. When the winding currents and their respective torque constants are in phase (φ is zero), the motor generates the maximum average torque or *pull-out torque;*

$$T_{pull\text{-}out} = T_{avg\ (max)} = \frac{2}{\pi} I_{rated}\ T. \quad (6)$$

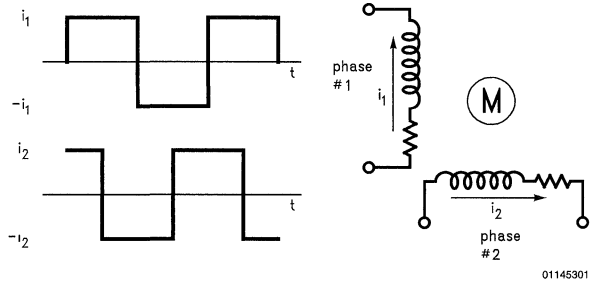


FIGURE 1. Ideal Quadrature Currents Drive the Windings of a Bipolar Stepper Motor

Square waves make good approximations for the winding currents at low speeds only, and (6), therefore, makes a good approximation of the pull-out torque at low speeds only. Real winding currents have an exponential shape dictated by the L/R-time constants of the windings, the voltage applied across the windings, and, to a lesser extent, the back emf generated by the motor as the rotor spins. For either winding,

$$i(t) = \left(I_o - \frac{V_{CC} - V_{emf}}{R}\right) e^{\frac{-R}{L}t} + \frac{V_{CC} - V_{emf}}{R} \quad (7)$$

Background (Continued)

describes the winding current at a change in the direction of that current, where I_o is the initial winding current, V_{CC} is the voltage applied across the winding, V_{emf} is the back emf, and R and L are the winding resistance and inductance. At low step rates, assuming $V_{CC} = V_{rated} >> V_{emf}$, the current easily slews to the peak value of V_{rated}/R before a subsequent direction change (*Figure 3a*). At higher step rates, because the time between direction changes is shorter, the current cannot reach the peak value (*Figure 3a*). V_{rated} is the rated voltage of the windings.

Clearly from (4) and *Figure 3*, as the speed increases, decreases in the winding currents result in decreases in $T_{pull\text{-}out}$. The torque vs. speed characteristic of a typical bipolar stepper motor (*Figure 4*) reflects this phenomenon. Each pull-out torque curve bounds (on the right) a region of torque-speed combinations inside which the stepper motor runs and outside which the stepper motor stalls.

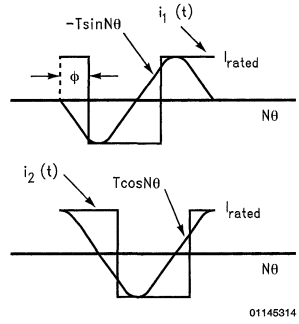


FIGURE 2. Ideal Square Wave Winding Currents and Sinusoidal Torque Constants for Average Torque Calculation

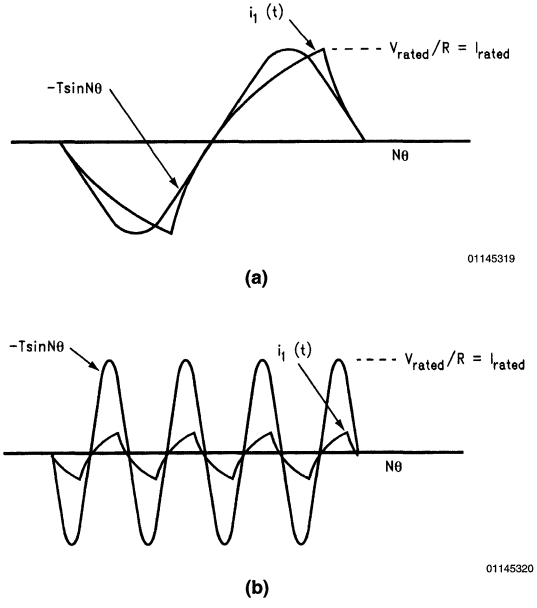


FIGURE 3. Real Winding Current and Sinusoidal Torque Constant vs Step Rate at Low Step Rates (a) and at High Step Rates (b)

It follows then, that the goal of increasing the high speed torque is achieved by increasing the winding currents at high speeds. This, in turn, is achieved by increasing the slew rates of the winding currents; for example, with the increased slew rates realized by raising V_{CC} well above V_{rated}, the winding current easily slews to the peak value of V_{rated}/R at

Background (Continued)

both low and high step rates (*Figure 5*). Winding currents realized with $V_{CC} = V_{rated}$ are represented with dashed lines, and, assuming a means for limiting at V_{rated}/R, winding currents realized with $V_{CC} >> V_{rated}$ are represented with solid lines.

Both decreasing the L/R-time constants of the windings and increasing the voltage applied across the windings increases the slew rates of the winding currents. L/R drives and chopper drives take these tactics to raise the slew rates of the winding currents well above those realized by simply applying the rated voltage to the windings. The torque vs. speed characteristic of a typical bipolar stepper motor (*Figure 4* again) reflects the resulting high speed torque gains.

It is important to note, however, that applying $V_{CC} >> V_{rated}$ also results in excessive winding currents at low speeds. The winding currents must be held at or below the rated limit (usually V_{rated}/R per winding) to hold power dissipated inside the motor at or below the rated limit (usually $2 \times V_{rated} \times I_{rated}$).

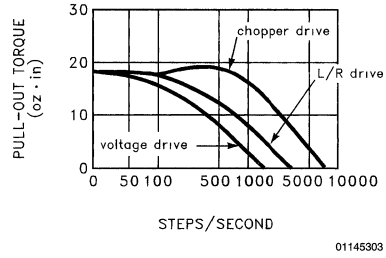


FIGURE 4. A Typical Torque vs Speed Characteristic of a Bipolar Stepper Motor

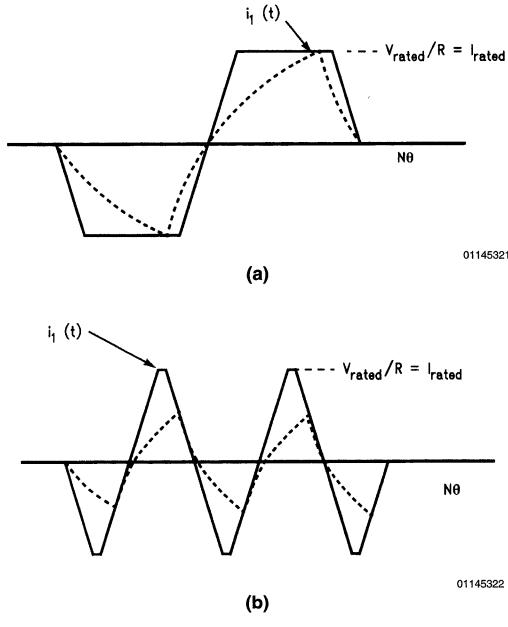


FIGURE 5. Real Winding Current vs Step Rate with $V_{CC} >> V_{rated}$ at Low Step Rates (a) and at High Step Rates (b)

Simple Voltage Drives

Simple drives employ two H-bridge power amplifiers to drive bipolar currents through the phase windings (*Figure 6*). For either amplifier, closing switches S1 and S4 forces the rated voltage (less two switch drops) across the winding, and current flows from supply to ground via S1, the winding, and S4. After opening S1 and S4, closing S2 and S3 reverses the direction of current in the winding. This drive scheme is commonly referred to as simple voltage drive. Because only the winding resistances limit the winding currents, V_{CC} cannot exceed V_{rated}.

L/R Drives

L/R drives employ two series power resistors to decrease the L/R-time constants of the windings; for example, a 45Ω power resistor in series with each of two 15Ω winding resistances divdes the L/R-time constants by four and allows the rated supply voltage to be increased by a factor of four. Both the crispness of the response and the high speed torque are increased. While the rotor holds position or moves at low step rates, the series power resistors protect the motor by holding the winding currents to the rated limit. Since both the L/R-time constants of the phase windings and the rated

L/R Drives (Continued)

supply voltage were increased by a factor of four, the example drive would commonly be referred to as an L/4R drive.

The maximum operating supply voltage of the power amplifiers can limit the factor by which the supply voltage is increased above the rated voltage of the windings, but power losses in the series resistors more likely limit this factor. If, for example, 60V is applied across two 0.5A, 15Ω phase windings, two 105Ω series resistors are required to hold the winding currents to the 0.5A/phase limit. This is an L/8R drive. Power dissipated in the series resistors while the rotor holds position is 105 x 0.5 x 0.5 x 2 = 52.5W, while power dissipated in the entire drive is 60 x 0.5 x 2 = 60W. The drive efficiency approaches 12.5%. After looking at these numbers, the drive designer may opt to cut losses by using the 30V power supply/45Ω series resistor combination of an L/4R drive. Unfortunately, while the rotor holds position, total power dissipated in the series resistors remains high at 22.5W and drive efficiency remains low at 25%.

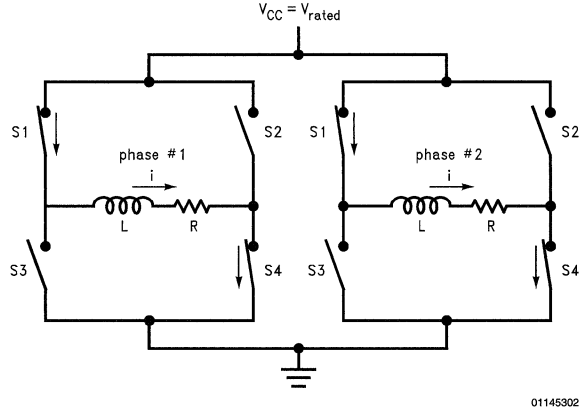


FIGURE 6. Simple Voltage Drive of a Bipolar Stepper Motor

Chopper Drives

Chopper drives increase the slew rates of the winding currents by applying $V_{CC} >> V_{rated}$. Feedback-driven switching of the H-bridges holds the winding currents to the rated limit. *Figure 7* shows the chopping states of a single H-bridge of a chopper drive. A low value resistor in the ground lead of the H-Bridge converts the winding current into a proportional feedback voltage, and the feedback voltage is compared to a reference voltage (not shown). While the feedback voltage is less than the reference voltage, switches S1 and S4 apply the full supply voltage across the winding (*Figure 7a*), and the winding current increases rapidly. When the feedback voltage is equal to the reference voltage; that is, when the winding current reaches the desired limit, S1 and S2 short the winding for a fixed period or *off-time* (*Figure 7b*). During the off-time, the winding current *recirculates* and decays slowly. At the end of the off-time, S1 and S4 reapply the full supply voltage across the winding, and the winding current again increases. Repetition of this sequence results in a *current chopping action* that limits the peak winding current to a level determined by the reference voltage and the resistor in the ground lead of the amplifier (*Figure 7c*), limit = $V_{reference}/R_S$. Chopping of the current only occurs when the current reaches the desired limit (usually the rated current of the winding). When the winding current changes direction to step the motor, the general operation remains the same except S2 is held closed and S1 and S3 are switched to limit the winding current. Because the H-bridge shorts the winding for a fixed period, this type of chopper drive is commonly referred to as a *fixed off-time* drive. By eliminating the series resistors required by L/R drives, chopper drives increase dramatically the drive efficiency. Typical efficiencies of chopper drives range from 75% to 90%.

Chopper Drives (Continued)

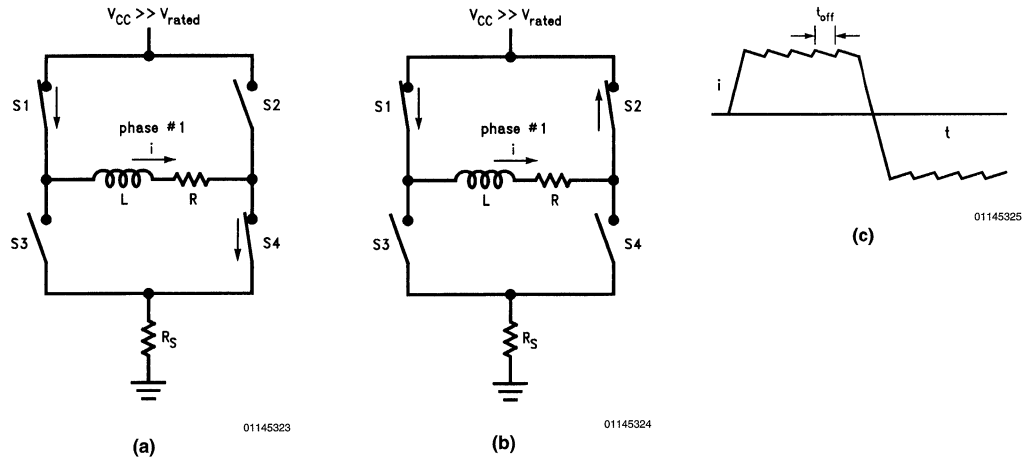


FIGURE 7. The Chopping States of a Single H-Bridge of a Chopper Drive: the Full V_{CC} is Applied Across the Winding (a), the Winding is Shorted (the Current Recirculates) (b), and the Chopped Winding Current (c)

An LMD18200-Based Chopper Drive

The LMD18200 is a 3A, 55V H-bridge (*Figure 8*). It is built using a multi-technology process which combines bipolar and CMOS control (logic) and protection circuitry with DMOS power switches on the same monolithic structure. The LMD18200 data sheet and AN-694 contain more information about the operation of the LMD18200.

Two LMD18200 H-bridges form the core of an example chopper drive (*Figure 9*). The PWM input (pin #5) of each LMD18200 accepts a logic signal that controls the state of that device. While the signal at PWM is logic-high, the H-bridge applies the full supply voltage across the winding, and while the signal at PWM is logic-low, the upper two switches of the H-bridge short the winding. The feedback voltage associated with either H-bridge is directly proportional to the current in the winding driven by that device. One half of an LM319 dual comparator compares the feedback voltage to the reference voltage. While the feedback voltage is less than the reference voltage, the signal at PWM is logic-high, the LMD18200 applies the full supply voltage across the winding, and the winding current increases. When the winding current increases to the point the feedback voltage and the reference voltage are equal, the LM319 triggers the LMC555-based one-shot. For the duration of the one-shot timing pulse, the signal at PWM is logic-low, the LMD18200 shorts the winding, and the winding current *recirculates* and decays. After the timing pulse, the signal, a PWM returns to logic-high, the LMD18200 reapplies the full supply voltage across the winding, and the winding current again increases. Repetition of this sequence results in a current chopping action (*Figure 10*) that limits the winding current to the 0.5A rating while allowing the 12V, 24Ω winding to be driven with 36V. **Note:** the RC components associated with the LMC555 set the one-shot timing pulse. To best illustrate the current chopping action, the one-shot timing pulse or off-time was set at approximately 100µs. Shorter off-times yield smoother winding currents.

The Dir input (pin #3) of each LMD18200 accepts a logic signal that controls the direction of the current in the winding driven by that device; in other words, changing the logic level of the signal at Dir commands the motor to take a step.

This chopper drive takes advantage of the current sense amplifier on board the LMD18200. The current sense amplifier sources a signal level current that is proportional to the total forward current conducted by the two upper switches of the LMD18200. This *sense* current has a typical value of 377 µA per Amp of load current. A standard ¼W resistor connected between the output of the current sense amplifier (pin #8) and ground converts the sense current into a voltage that is proportional to the load current. This proportional voltage is useful as a feedback signal for control and/or overcurrent protection purposes. The 18 kΩ resistors (*Figure 9*) set the gain of the drive at approximately 0.15A per volt of reference voltage (simply the reciprocal of the product of 377 µA/A and 18 kΩ).

An LMD18200-Based Chopper Drive (Continued)

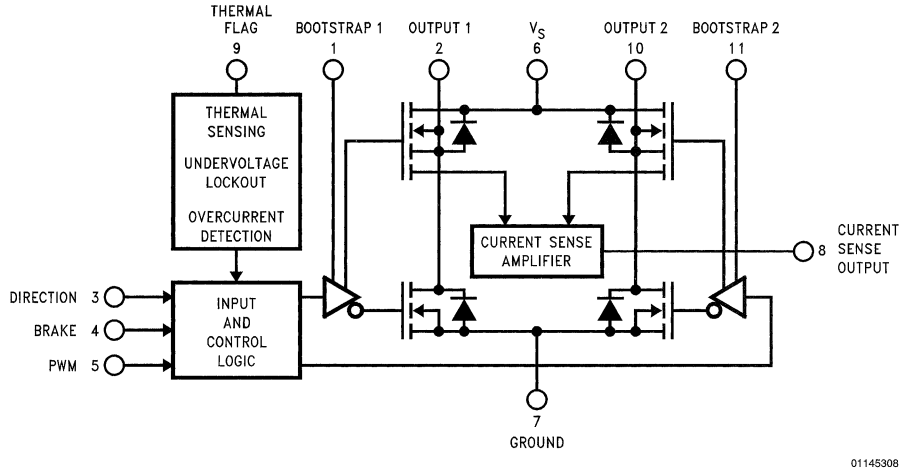
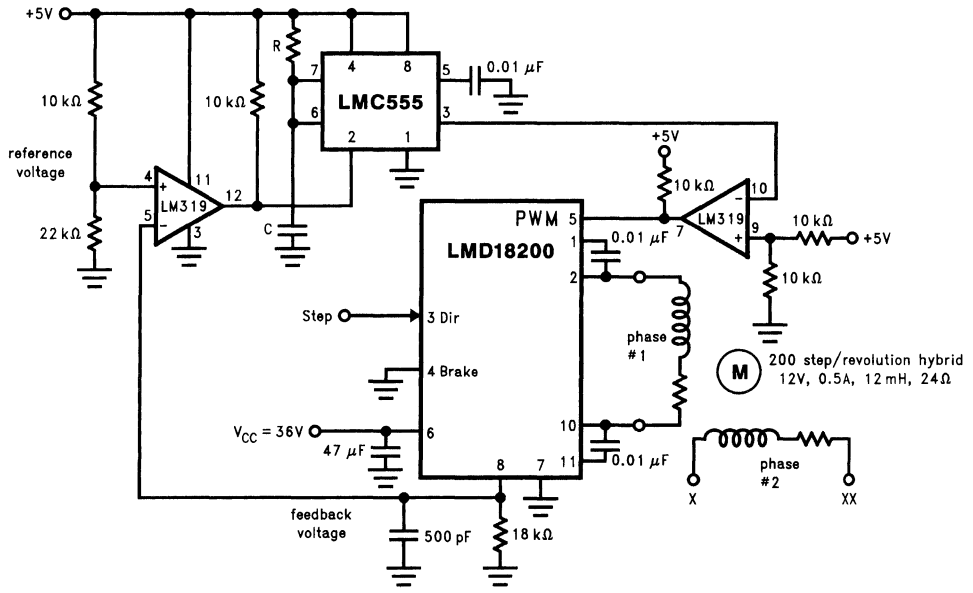


FIGURE 8. The LMD18200 3A, 55V Full H-Bridge

An LMD18200-Based Chopper Drive (Continued)



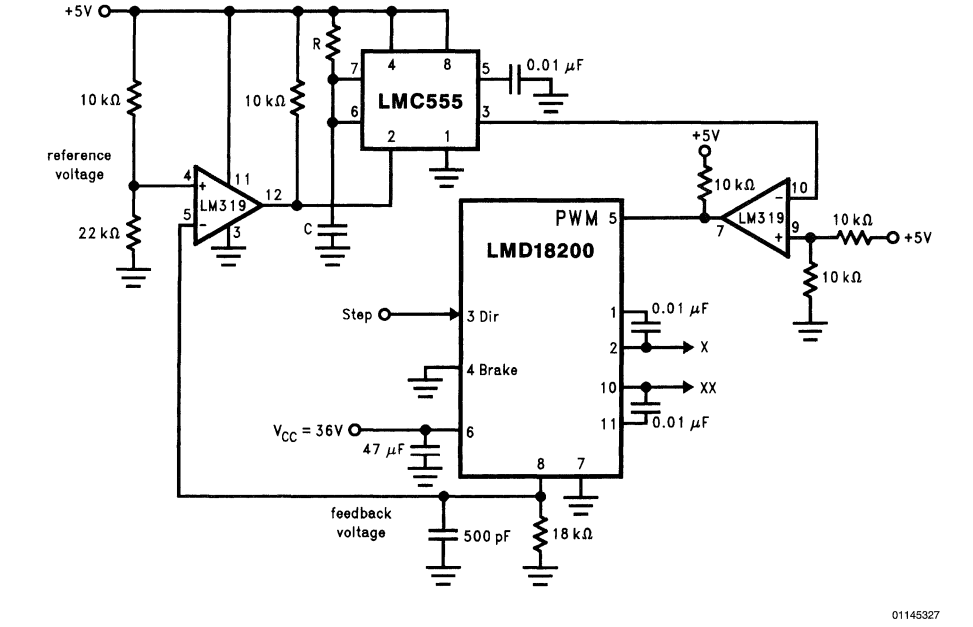
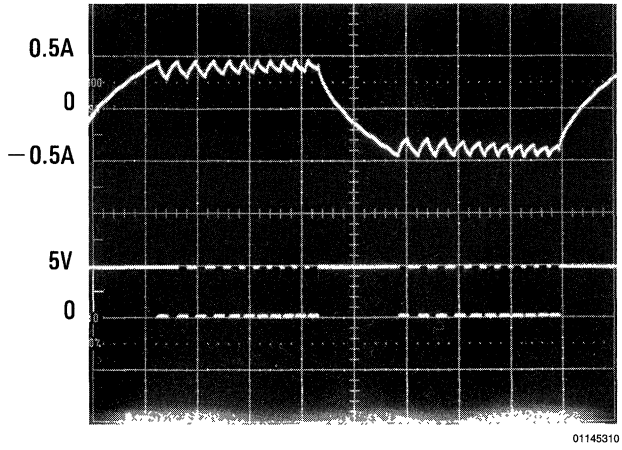


FIGURE 9. An LMD18200-Based Chopper Drive

An LMD18200-Based Chopper Drive (Continued)

During the current chopping action, the feedback voltage tracks the winding current (*Figure 11*). When the signal at Dir initiates a change in the direction of the winding current, the feedback voltage ceases tracking the winding current until the winding current passes through zero. This phenomenon occurs because the current sense amplifier only sources a current proportional to the total *forward* current conducted by the two upper switches of the LMD18200. During the period the feedback voltage does not track the winding current, the winding current actually flows from ground to supply as reverse current through a lower and an upper switch of the H-bridge. Only after the winding current passes through zero does it once again become forward current in one of the upper switches (see AN-694). The feedback voltage is ground referenced; thus, it appears the same regardless of the direction of the winding current.

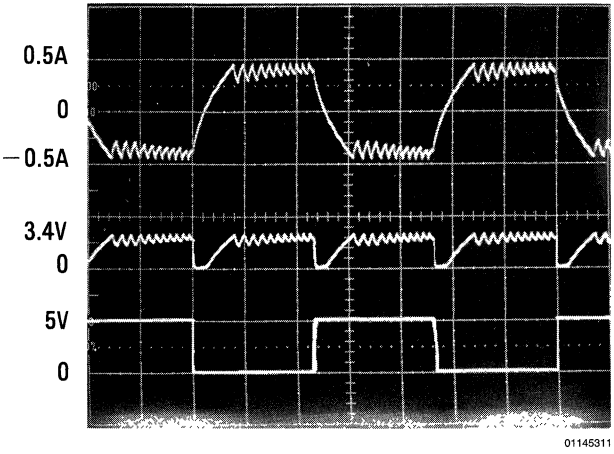
The same 200 step/revolution hybrid stepper (*Figure 9*) was used to generate *Figures 10, 11, 12, 13. Figure 12* shows the winding current for simple voltage drive with $V_{CC} = V_{rated} = 12V$. *Figure 13* shows the winding current for L/4R drive with added series resistance of 72Ω/phase and $V_{CC} = 4V_{rated} = 48V$.



Top Trace: Winding Current at 0.5A/div
Bottom Trace: PWM Signal at 5V/div
Horizontal: 0.5 ms/div

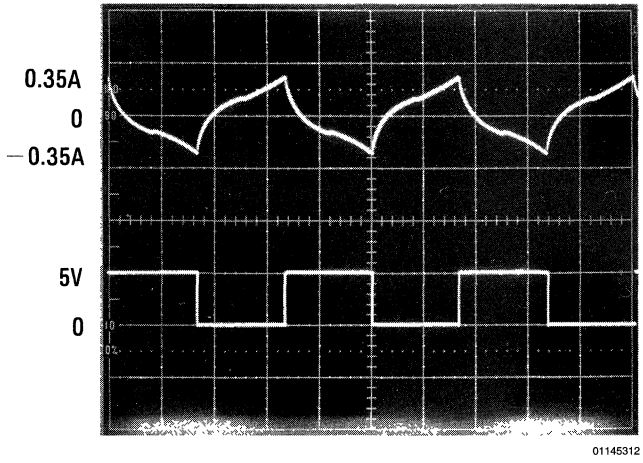
FIGURE 10. The Chopped Winding Current and the Logic Signal at PWM

An LMD18200-Based Chopper Drive (Continued)



Top Trace: Winding Current at 0.5A/div
Middle Trace: Feedback Voltage at 5V/div
Bottom Trace: Step Logic Signal at 5V/div
Horizontal: 1 ms/div

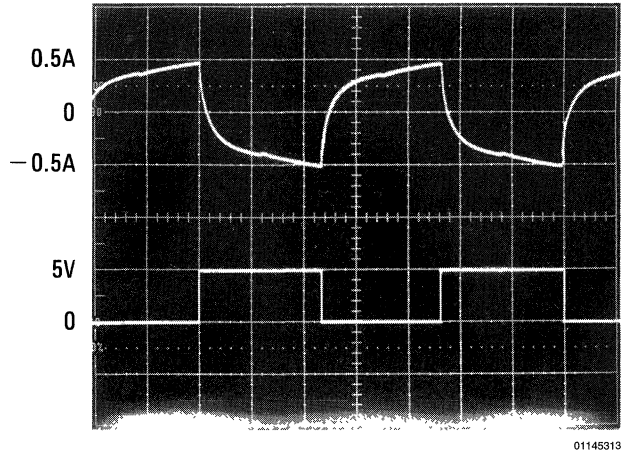
FIGURE 11. The Chopped Winding Current and Feedback Voltage at 860 Steps/Second



Top Trace: Winding Current at 0.5A/div
Bottom Trace: Step Logic Signal at 5V/div
Horizontal: 2 ms/div

FIGURE 12. The Winding Current for Simple Voltage Drive at 600 Steps/Second

An LMD18200-Based Chopper Drive (Continued)



Top Trace: Winding Current at 0.5A/div
Bottom Trace: Step Logic Signal at 5V/div
Horizontal: 1 ms/div

FIGURE 13. The Winding Current for L/4R Drive at 860 Steps/Second

High-Efficiency 3A Battery Chargers Use LM2576 Regulators

National Semiconductor
Application Note 946
Chester Simpson

This paper describes two LM2576-based designs which provide up to 3A of current for battery charging.

3A Battery Charger Has Built-In Overcharge Protection

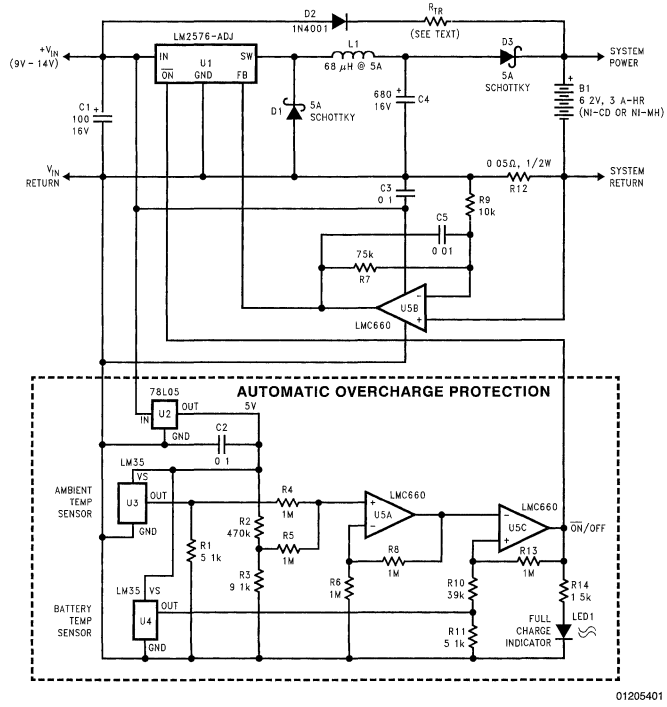
This design is a 3A battery charger intended for use with 5-cell Ni-Cd or Ni-MH battery packs (but can be modified to suit other numbers of cells). The circuit includes automatic shutoff that occurs when the battery temperature rises 10°C above ambient.

CIRCUIT CONCEPT

This battery charger shown in *Figure 1* was developed specifically for applications using either ***Nickel-Cadmium (Ni-Cd)*** or ***Nickel-Metal Hydride (Ni-MH)*** batteries that will accept a 3A fast-charge rate, and provides automatic shutoff of the high-current charge when the battery is full.

After shutoff, a continuous (low level) charge current is used to "trickle charge" the battery which keeps it topped off and prevents charge loss due to any internal leakage.

The trickle charge rate used must always be low enough that the amount of gas developed within the cell is small enough that it can recombine, thus preventing pressure build-up and venting (opening of the cell's internal vent to release pressure). The maximum safe trickle charging rate is determined by the size and type of battery (this is covered later in the paper).



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Notes (Unless Otherwise Specified)

All capacitance values are in µF

All resistors are 5%, ¼W

U1 requires small heatsink (R_{TH} < 15°C/W)

C1 and C4 must be low ESR aluminum electrolytic

U5D is not used

FIGURE 1. 3A Charger with Overcharge Protection

3A Battery Charger Has Built-In Overcharge Protection (Continued)

The critical specification for a battery is its ***Amp-hour (A-hr) rating,*** which is numerically equal to the maximum amount of current the battery can supply to a load for one hour before the cell reaches its ***end-of-life voltage*** (usually taken as 1.0V/cell for Ni-Cd and Ni-MH batteries.

When a battery is charged or discharged at a current that is equal to its A-hr rating, ***this is known as the "c" rate.***

Most Ni-Cd and Ni-MH batteries can be safely charged at a 1c rate, as long as they are not overcharged. However, the battery temperature must be within a range of about 15˚C to 45˚C (the reasons are detailed later in this paper).

OVERCHARGING: THE SILENT KILLER

The nemesis of all rechargeable batteries is overcharge ... although some battery types tolerate it better than others, the results of overcharge range from minor damage to catastrophic failure.

In the case of Ni-Cd, which is the most popular rechargeable battery type presently in use, sustained overcharge causes increasing pressure within the battery that eventually causes the cell's vent to open and release oxygen. This has a detrimental effect on the battery, although it may still retain some useful capacity.

If Ni-MH batteries are overcharged, they will also build up pressure and release gas: however, the gas released will be hydrogen, which is extremely explosive near spark or flame. One battery manufacturer created an interesting euphemism for some of the unfortunate accidents in cases where Ni-MH batteries were overcharged: ***Rapid Spontaneous Disassembly.***

DETECTING END-OF-CHARGE

There are several ways to detect end-of-charge for Ni-Cd or Ni-MH batteries, but one way that is both simple and reliable is called a ΔT detector. It measures both the ambient temperature and the battery temperature and cuts off the high current charger when the battery rises a pre-set amount above ambient. This design uses a 10˚C rise as the cutoff point (which is recommended by most battery makers), but can be easily adjusted by changing resistor values.

Ni-Cd cells are perfectly suited for ΔT cutoff techniques, because their charge process is ***endothermic*** (they get slightly ***cooler*** when a discharged battery is being recharged). Even at fast charge rates, the battery will not begin to heat until it is nearly fully recharged. At that point, the battery is no longer converting the electrical current into a chemical reaction, so it must be dissipated as heat. The resulting increase in temperature provides a very accurate indicator that it is time to stop charging.

The Ni-MH battery is not quite as accommodating: the recharge cycle is ***exothermic*** (the battery gets slightly ***warmer*** during recharge) but still shows a fairly well defined increase in temperature when the battery is fully charged. Using a 10˚C ΔT detection point will give good results in most cases, and is recommended by the battery makers.

NOTE: WARNINGS ABOUT FAST CHARGING NI-MH AND NI-CD BATTERIES

Since the Ni-MH battery normally gives off heat during recharge, the 10˚C "window" may have to be adjusted to suit the characteristics of the specific cell: The window must be wide enough to prevent premature cutoff from "normal" heating, but narrow enough to detect the temperature rise which occurs at full charge (and execute appropriate charge termination).

Any new design that uses Ni-MH batteries should be carefully evaluated to verify accurate end-of-charge termination because of the potential for battery explosion if hydrogen is released.

IMPORTANT: ***With Ni-Cd or Ni-MH cells, the 1c (fast) charge rate can only be safely used if the battery temperature is in the range of about 15˚C to 45˚C.***

At ***low temperatures,*** gas recombination within NiCd and NiMH batteries does not occur as easily, which limits the amount of charging current that can be safely used before venting will occur. If low-temperature (<15˚C) recharging is required, consult the battery maker for safe charging current levels.

A battery that is recharged at ***elevated temperature*** will retain substantially less energy than a battery recharged at 25˚C. At high temperatures (>35˚C) gas generation within the cell occurs at a much lower state of charge, meaning that the cell will not accept as much charge (compared to 25˚C) for a given amount of cell temperature rise.

The poor charging efficiency seen at high battery temperatures means that extremely long recharge times (at low charging currents) are required to deliver full (25˚C) capacity of charge to a "hot" battery.

TRICKLE CHARGE CURRENT

All batteries lose charge internally due to self-discharge, usually occurring due to leakage paths through the battery separators (insulators). The amount of leakage is dependent primarily on battery age and usage, with leakage increasing dramatically in batteries that are old or have completed many cycles of charge and discharge.

Trickle charging is a continuous low-level charging current that tops off the total charge in the battery, and prevents any energy loss that would occur due to leakage.

The ***maximum safe trickle charging current for a typical Ni-Cd cell is about 0.1c,*** this being the maximum charge rate at which all of the gas developed internally is able to recombine (so there is no internal pressure buildup that would cause venting).

For Ni-MH batteries, the maximum (safe) trickle charge rate is lower (one manufacturer specifies c/40). This is an important difference between Ni-Cd and Ni-MH batteries, and must not be exceeded for continuous charging.

In this design, the trickle charge current is provided by the resistor labeled R_{TR} (see *Figure 1*). This current flows any time V_{IN} is present, regardless of operation of the high-current charger. When the high-current charger is operating, the total charging current is the ***sum*** of the trickle current and the current provided by U1.

Once the input voltage V_{IN} and the desired trickle charge current I_{TR} are known, the value for R_{TR} is found using Ohm's Law:

$$R_{TR} = (V_{IN} - 7 - 0.7)/I_{TR}$$

The maximum power dissipation in R_{TR} must also be calculated (when selecting a resistor, make sure the power rating is greater than the value calculated below):

$$P_{MAX}\,(R_{TR}) = (V_{IN} - 4 - 0.7)^2/R_{TR}$$

3A Battery Charger Has Built-In Overcharge Protection (Continued)

Note that the power dissipation in the resistor is dependent on the battery voltage. As the battery voltage increases, the voltage drop across R_{TR} decreases (causing the power dissipation to decrease).

In the above equation, a battery voltage of 4V is assumed as a worst-case minimum value for battery operating voltage for a five-cell battery pack (which would provide the maximum power dissipation for R_{TR}).

A ***good*** 5-cell Ni-Cd or Ni-MH battery which is being trickle charged (after being fully recharged) will read about 7V, which will produce the *minimum* power dissipation in resistor R_{TR}.

DETAILS OF CIRCUIT FUNCTION (REFER TO *Figure 1*)

The 3A of charging current provided by the fast-charger is obtained from an LM2576, which is a buck regulator that switches at 52 kHz. Because it is a switcher, it allows the user the option of using a wider input voltage range and still retaining high power conversion efficiency (about 80% @3A with V_{IN} in the 10V–14V range).

The LM2576 IC (U1) is used to provide a charging current that is independent of the battery voltage. Whenever the ON/OFF pin is held low, U1 will source current into the battery through D3. A current-control feedback loop is established using U5B, R12, and associated components.

R12 is used as a current shunt, and it provides a voltage to the input of U5B that is proportional to the charging current. U5B functions as an amplifier with a gain of 8.5, which causes the output of U5B to be 1.23V when the current through R12 is about 2.9A. The 1.23V signal on the feedback pin of U1 will "lock" the loop at this value of charging current.

A fast-charge current value other than 2.9A can be set by adjusting the values of R7, R9, or R12. These values (which set the overall gain of the stage) should be adjusted so that the output of U5B is 1.23V at the desired amount of fast-charge current.

AUTOMATIC SHUTDOWN AT FULL CHARGE

The crucial part of fast charging a battery (especially if it is Ni-MH) is ***knowing when to stop.*** This design uses a ΔT detector that measures ***both*** the battery temperature and the ambient temperature, and shuts down the fast-charge current source when the battery is +10˚C ***above ambient.***

This method is superior to techniques which sense only battery temperature. Single-ended temperature sensing may not accurately measure charge: a "cold" battery will have to heat up too much before the detection point is reached (overcharging it), while a "hot" battery will terminate charge long before full charge has been delivered to the battery (because its temperature starts out too near the detection level).

Two LM35 temperature sensors (U3 and U4) provide output voltages of 10 mV/˚C (proportional to their temperature). U3 is used to measure the ambient, while U4 measures the battery temperature.

Note: U4 must be in contact with the metal case of the battery to accurately measure its temperature. The plastic sleeve around the battery may have to be opened up to allow flush contact. Best results are obtained if the sensor is located ***between two batteries*** (touching both).

Monitoring more than one battery virtually eliminates the possibility that the sensor happens to be reading a bad (shorted) cell which will not heat up and provide charge termination. In some laptops, multiple sensors are used so that all battery cells are monitored, with charge termination occurring when ***any*** cell temperature reaches the trip level.

The 78L05 regulator (U2) is used to provide a 5V source to power the LM35 sensors and also acts as a reference point for resistive divider R2 and R3. Resistors R1 and R11 are used to sink current (since the LM35 can not).

CONTROLLING THE FAST-CHARGE CURRENT SOURCE

U5C acts as a comparator which controls the on/off pin of the high-current charging source (U1). When the output of U5C is low, the 3A current source is turned on. When the output of U5C is high, U1 is turned off and LED1 is lit which indicates that the charger has completed the high-current charge phase and is now trickle charging.

Hysteresis is built into U5C (see R13), which effectively "latches" the output of U5C high after it completes the fast-charge portion of the cycle (it stays latched until the input power is cycled on and off). Without hysteresis, the charger would again turn on the 3A charger after the fully-charged battery had cooled during trickle charging.

DETECTING AN END-OF-CHARGE CONDITION

The signals that are sent to U5C are derived from the temperature sensors. They cannot be compared directly, since detection must occur when the signal coming from U4 (the battery sensor) is 100 mV above the signal coming from U3 (the ambient sensor).

In this design, the signal from U3 is DC level shifted up about 0.1V by U5A and its associated components. R2 and R3 set a 0.1V reference point for U5A, whose output voltage is the voltage at the output of U3 added to the 0.1V reference.

With the signal from U3 level shifted by an amount that is equal to 10˚C, U5C can be used to compare the level-shifted signal from U3 to the signal from U4. When these two are equal, the temperature sensed by U4 (the battery) will be 10˚C above the temperature sensed by U3 (the ambient). This is the point where shutdown of the 3A charger occurs, and trickle charging continues.

3A Battery Charger has Logic-Level Current Controls

This design is a 3A battery charger with logic-level controls, allowing a logic controller to adjust the battery charging current to any one of four rates. The circuit was designed to implement µP-based charging control in a system that operates from Ni-Cd or Ni-MH batteries.

GENERAL DESCRIPTION

The circuit shown in *Figure 1* is a 3A (maximum) battery charger that uses a 52 kHz switching converter to step down the input DC voltage and regulate the charging current flowing into the battery. The switching regulator maintains good efficiency over a wide input voltage range, which allows the use of a cheap, poorly regulated "DC wall adaptor" for the input source.

The key feature of this circuit is that it allows the µP controller inside the PC to select from one of four different charging currents by changing the logic levels at two bits. The various

3A Battery Charger has Logic-Level Current Controls

(Continued)

charge levels are necessary to accommodate both Ni-Cd and Ni-MH type batteries, as they require slightly different charge methods.

Both Ni-Cd and Ni-MH batteries can be charged at the high-current "c" rate up until the end-of-charge limit is reached, but the two batteries must be trickle-charged differently (trickle charging is a continuous, low-current charging rate that keeps the battery "topped off" after the high-current charge cycle has delivered about 95% of the battery's total charge capacity).

The recommended trickle-charge rate for a Ni-Cd is about c/10, but for Ni-MH most manufacturers recommend that the charge rate not exceed c/40. If a continuous charge rate greater than c/40 is applied to a Ni-MH battery, the internal pressure can build up to the point where the battery will vent hydrogen gas. This is detrimental to the life of the Ni-MH battery and potentially dangerous for the user (hydrogen gas is easily ignited).

The circuit shown in *Figure 2* was designed to charge a 3A-hr Ni-Cd or Ni-MH battery with high efficiency, using logic-level signals to control the charging current. The four selectable charge rates are 3A, 0.75A, 0.3A, and 0.075A which correspond to charge rates of c, c/4, c/10, and c/40 for the 3A-hr battery used in this application.

CIRCUIT OPERATION (REFER TO *Figure 2*)

The unregulated DC input voltage is stepped down using an LM2576 3A buck regulator, providing up to 3A of current to charge the battery.

In order to regulate the amount of charging current flowing into the battery, a current control loop is implemented using op-amp U2. The voltage drop across the sense resistor R8 provides a voltage to U2 that is proportional to the charging current.

Note: The 0.05Ω value for R8 was specified by the customer in this application to minimize the power dissipated in this resistor. If a higher Ohmic value is used (more resistance), a larger sense voltage is developed and a less precise (cheaper) op-amp can be used at U2, since the input offset voltage would not be as critical (of course, increasing the value of R8 also increases its power dissipation).

When the current-control loop is operating, the voltage at the feedback pin of U1 is held at 1.23V. The battery charging current that corresponds to this voltage is dependent on the overall gain of U2 and the attenuators made up of Q1, Q2 and the resistors R10, R11, R2 and R3.

Turning Q1 on (by putting a "1" on logic input "A") provides an increase of 4:1 in load current. The load current is higher with Q1 on because R2 and R3 divide down the output of U2 by 4:1, requiring U2 to output a higher voltage to get the 1.23V on the feedback line of U1. Higher voltage at the output of U2 means that more charging current is flowing through R8 (also the battery).

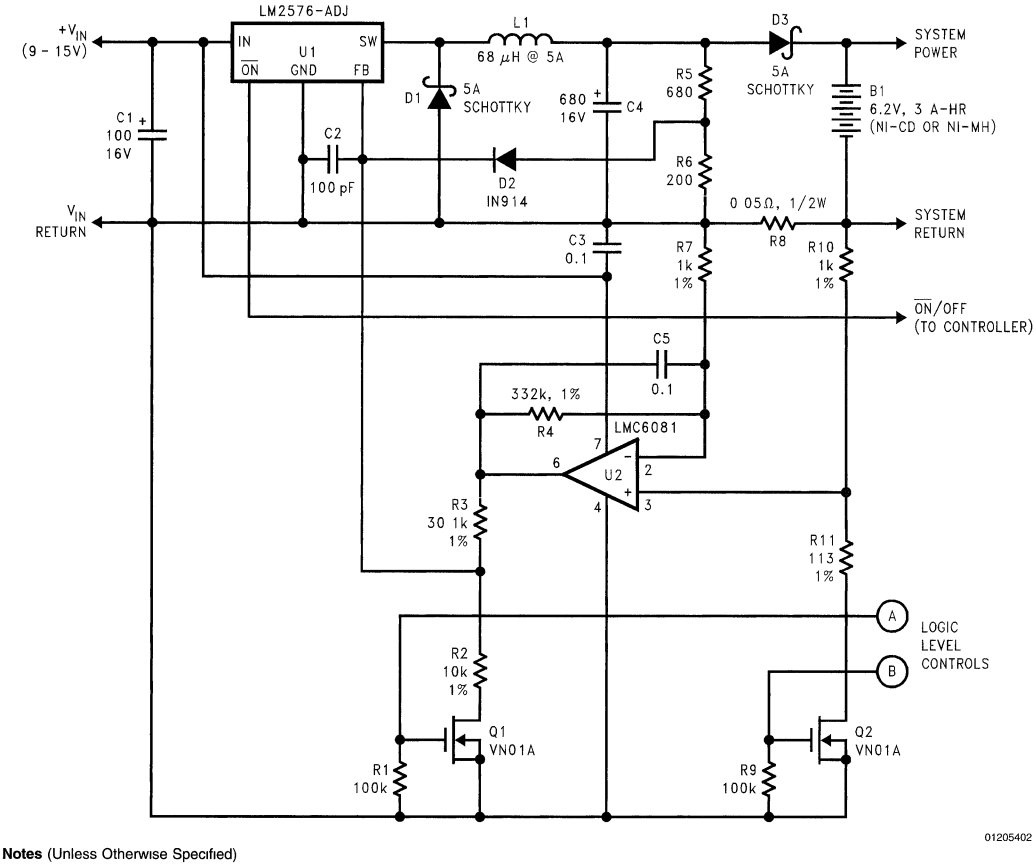
The operation of Q2 is similar to Q1: when Q2 is turned on by putting a logic "1" on input "B", the load current is increased by a factor of 10:1. This is because when Q2 is on, the sense voltage coming from R8 is divided down by R10 and R11, requiring ten times as much signal voltage across R8 to get the same voltage at the non-inverting input of U2.

Although both attenuating dividers could have been placed on the input side of U2, putting the 4:1 divider at the output improves the accuracy and noise immunity of the amplifier U2 (because the voltage applied to the input of U2 is larger, this reduces the input-offset voltage error and switching noise degradation).

R5, R6, and D2 are included to provide a voltage-control loop in the case where the battery is disconnected. These components prevent the voltage at the cathode side of D3 from rising above about 8V when there is no path for the charging current to return (and the current control loop would not be operational).

Capacitor C2 is included to filter some of the 52 kHz noise present on the control line coming from U2. Adding this component improved the accuracy of the measured charging current on the breadboard (compared to the predicted design values).

3A Battery Charger has Logic-Level Current Controls (Continued)



Notes (Unless Otherwise Specified)

Note 1: All resistors are in Ω, 5% tolerance, ¼W

Note 2: All capacitors are in µF

Note 3: Q1 and Q2 are made by SUPERTEX

Note 4: For 3A current, U1 requires small heatsink ($R_{TH} \leq 15°C/W$)

BENCH TEST DATA

Logic Input "A"	Logic Input "B"	Nominal Battery Charging Current (A)		Measured Battery Charging Current (A) with V_{IN} = 10V	Power Conversion Efficiency (%) with V_{IN} = 10V
1	1	3.0	(C RATE)	3.06	77
0	1	0.75	(C/4 RATE)	0.78	79
1	0	0.30	(C/10 RATE)	0.30	
0	0	0.075	(C/40 RATE)	0.077	

FIGURE 2. 3A Battery Charger With Logic-Level Current Controls

Maximum Power Enhancement Techniques for Power Packages

National Semiconductor
Application Note 1028

Introduction

As packages become smaller, achieving efficient thermal performance for power applications requires that the designers employ new methods of meliorating the heat flow out of devices. Thus the purpose of this paper is to aid the user in maximizing the power handling capability of National Semiconductor's power packages by using the SOT-223 as an example. Ultimately the user may achieve improved component performance and higher circuit board packing density by using the thermal solution suggested below.

In natural cooling, the method of improving power performance should be focused on the optimum design of copper mounting pads. The design should take into consideration the size of the copper and its placement on either or both of the board surfaces. A copper mounting pad is important because the substrate of the integrated circuit is mounted directly onto the pad. The pad acts as a heatsink to reduce thermal resistance and leads to improved power performance.

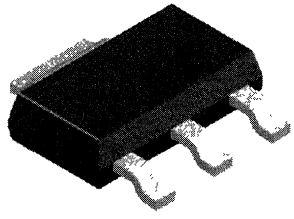


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FIGURE 1. SOT-223 Package achieves junction-to-case thermal resistance $R_{\theta JC}$ of 12˚C/W.

Theory

When a device operates in a system under the steady-state condition, the maximum power dissipation is determined by the maximum junction temperature rating, the ambient temperature, and junction-to-ambient thermal resistance.

$$P_{DMAX} = (T_{JMAX} - T_A) / R_{\theta JA} \quad (1)$$

The term junction refers to the point of thermal reference of the semiconductor. *Equation (1)* can also be applied to the transient-state:

$$P_{DMAX}(t) = [T_{JMAX} - T_A] / R_{\theta JA}(t) \quad (2)$$

where $P_{DMAX}(t)$ and $R_{\theta JA}(t)$ are time dependent. By using the transient thermal resistance curves shown in the data sheet, a transient temperature change can be calculated. The transient thermal behavior is a complicated subject because $R_{\theta JA}(t)$ increases non-linearly with time and the conditions of the power pulse. A more thorough treatment of transient power analysis is beyond the scope of this document and the reader can refer to [13] for details.

$R_{\theta JA}$ has two distinct elements, $R_{\theta JC}$ junction-to-case and R_{CA} case-to-ambient thermal resistance.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad (3)$$

The case thermal reference of the SOT-223 Power Package is defined as the point of contact between the lead of the package and the mounting surface.

$R_{\theta CA}$ is influenced by many variables such as ambient temperature, board layout, and cooling method. Due to the lack of an industry standard, the value of $R_{\theta CA}$ is not easily defined and can affect $R_{\theta JA}$ significantly. In addition, the case reference may be defined differently by various manufacturers. Under such conditions, it becomes difficult to define $R_{\theta CA}$ from the component manufacturer standpoint.

On the other hand, $R_{\theta JC}$ is independent of users' conditions and can be accurately measured by the component manufacturer.

Therefore, in this paper an effort has been made to define a procedure which can be used to quantify the junction-to-ambient thermal resistance $R_{\theta JA}$ which is more useful to the circuit board designer.

Result

The scope of the investigation has been limited to the size of copper mounting pad and its relative surface placement on the board. In still air with no heatsink, the application of these heat dissipation methods is the most cost effective thermal solution. A total of sixteen different combinations of 2 oz. copper pad sizes and their placement were designed to study their influence on $R_{\theta JA}$ thermal resistance. The configurations of the board layout are shown in *Figure 2* and *Table 1*. Layouts 1 to 6 have the copper pad sizes from 0.0123 to 1 square inches on the top side of the board (top side is defined as the component side of the board). Layouts 7 to 11 have copper pad sizes from 0.2 to 1 square inches on the bottom side of the board. Layouts 12 to 16 have copper pad sizes from 0.132 to 1 square inches divided equally on both sides of the board.

Result (Continued)

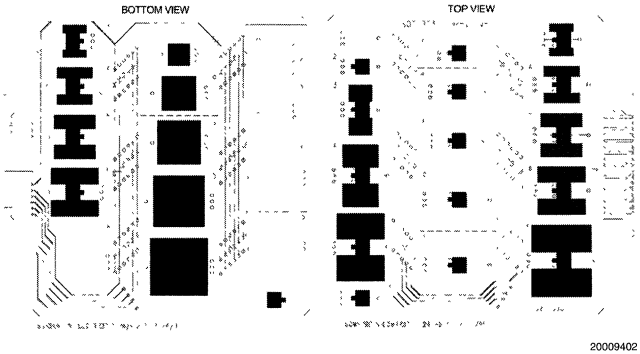


FIGURE 2. Both Sides of the 4.5" x 5" SOT-223 Thermal Board. Complete scale drawings is shown in Appendix D.

TABLE 1. Thermal Board Configurations

Layout	2 oz. Copper Mounting Pad Area (in^2)	Relative Placement on Board
1–6	0.0123, 0.066, 0.3, 0.53. 0.76, 1	Top
7–11	0.2, 0.4, 0.6, 0.8, 1	Bottom
12–16	0.132, 0.35, 0.568, 0.784, 1	½ Top and ½ Bottom

$R_{\theta JA}$ was calculated from the relationship between power and the change of junction temperature. If readers are interested in the test conditions and method, they are encouraged to refer to Appendix B for details.

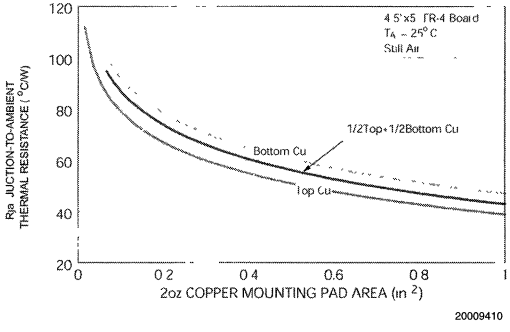


FIGURE 3. SOT-223 Junction-to-Ambient Thermal Resistance versus Copper Mounting Pad Area and its Surface Placement

Plots in *Figure 3* show the relationship of $R_{\theta JA}$ versus the copper mounting pad area and its surface placement on the board. It is apparent that increasing copper mounting pad area considerably lowers $R_{\theta JA}$ from approximately 110°C/W to 40°C/W in the range from 0.0123 to 1 square inches. In addition, placing all the copper on the top side of the board further reduces $R_{\theta JA}$ by 10°C/W to 15°C/W when compared with the other two placements.

By substituting the thermal resistance, ambient temperature, and the maximum junction temperature rating into *Equation (1)*, the steady-state maximum power dissipation curves can be obtained and are shown in *Figure 4*.

A 18% increase in the power handling can be achieved by increasing the copper pad area on top of the board from 0.0123 to 0.066 in.^{2}, layout 2. This thermal pad fits directly under the package, so that no additional board space is required. For maximum performance, it is recommended to put extra copper on the bottom of the board connected to the top pad by through-hole thermal vias.

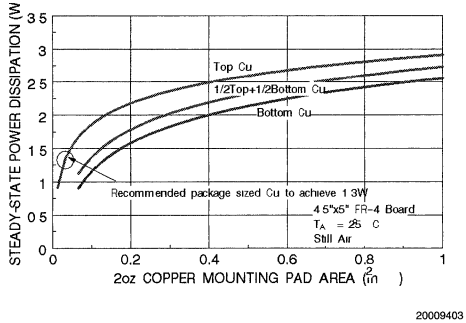


FIGURE 4. Maximum Power Dissipation Curves for SOT-223. 0.066 in.^{2} 2 oz. copper mounting pad area, Layout 2, is recommended to achieve approximately 1.3W.

Conclusion

National Semiconductor has attempted to define the thermal performance of the SOT-223 Power Package, from a systems point of view. It has been demonstrated that significant thermal improvement can be achieved in the maximum power dissipation through the proper design of copper mounting pads on the circuit board. The results can be summarized as follows:

- Enlarged copper mounting pads, on either one or both sides of the board, are effective in reducing the case-to-ambient thermal resistance $R_{\theta CA}$.
- Placement of the copper pads on the top side of the board gives the best thermal performance.
- The most cost effective approach of designing layout 2: 0.066 square inches copper pad directly under the package, without occupying additional board space, can increase the maximum power from approximately 1.1W to 1.3W.

Appendix A

HEAT FLOW THEORY APPLIED TO POWER DEVICES

When a power device operates with an appreciable current, its junction temperature is elevated. It is important to quantify its thermal limits in order to achieve acceptable performance and reliability. This limit is determined by summing the individual parts consisting of a series of temperature rises from the semiconductor junction to the operating environment. A one dimensional steady-state model of conduction heat transfer is demonstrated in *Figure 5.* The heat generated at the device junction flows through the die to the die attach pad, through the lead frame to the surrounding case material, to the printed circuit board, and eventually to the ambient environment. There are also secondary heat paths. One is from the package to the ambient air. Using a MOSFET device as an example, the other is from the drain lead frame to the detached source and gate leads then to the printed circuit board. These secondary heat paths are assumed to be negligible contributors to the heat flow in this analysis.

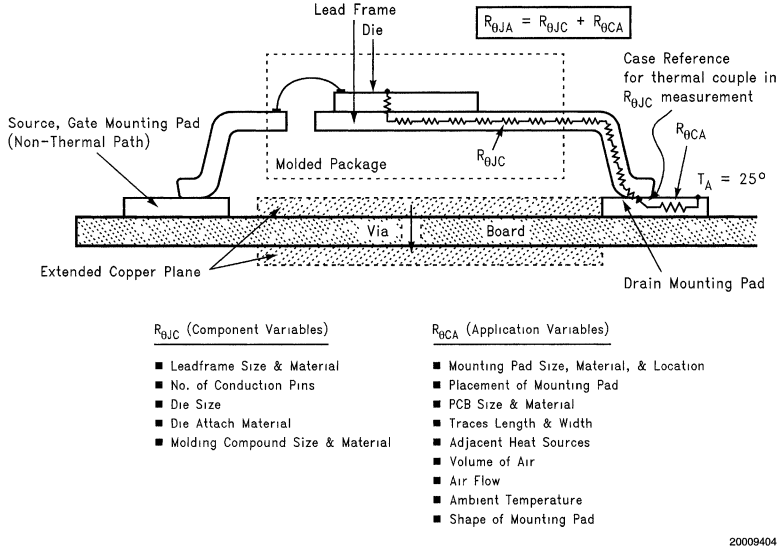


FIGURE 5. Cross-sectional view of a Power MOSFET mounted on a printed circuit board. Note that the case temperature is measured at the point where the drain lead(s) contact with the mounting pad surface.

The increase of junction temperature above the surrounding environment is directly proportional to dissipated power and the thermal resistance.

The steady-state junction-to-ambient thermal resistance, $R_{\theta JA}$, is defined as

$$R_{\theta JA} = (T_J - T_A)/P$$

where T_J is the average temperature of the device junction. The term junction refers to the point of thermal reference of the semiconductor device. T_A is the average temperature of the ambient environment. P is the power applied to the device which changes the junction temperature.

$R_{\theta JA}$ is a function of the junction-to-case $R_{\theta JC}$ and case-to-ambient $R_{\theta CA}$ thermal resistance.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where the case of a power MOSFET is defined at the point of contact between the drain lead(s) and the mounting pad surface. $R_{\theta JC}$ can be controlled and measured by the component manufacturer independent of the application and

Appendix A (Continued)

mounting method and is therefore the best means of comparing various suppliers component specifications for thermal performance. On the other hand, it is difficult to quantify $R_{\theta CA}$ due to heavy dependence on the application. Before using the data sheet thermal data, the user should always be aware of the test conditions and justify the compatibility in the application.

Appendix B

THERMAL MEASUREMENT

Prior to any thermal measurement, a K factor must be determined. It is a linear factor related to the change of intrinsic diode voltage with respect to the change of junction temperature. From the slope of the curve shown in *Figure 6*, K factor can be determined. It is approximately 2.2 mV/°C for most Power MOSFET devices

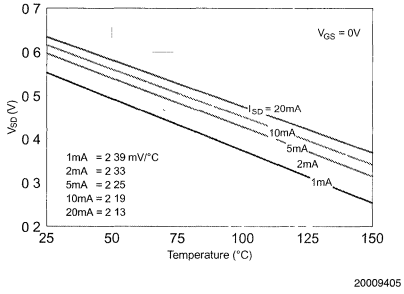


FIGURE 6. K Factors, Slopes of a V_{SD} vs Temperature Curves, of a Typical Power MOSFET

After the K factor calibration, the drain-source diode voltage of the device is measured prior to any heating. A pulse is then applied to the device and the drain-source diode voltage is measured 30 µs following the end of the power pulse. From the change of the drain-source diode voltage, the K factor, input power, and the reference temperature, the time dependent single pulsed junction-to-reference thermal resistance can be calculated. From the single pulse curve on *Figure 7*, duty cycle curves can be determined. Note: a curve set in which $R_{\theta JA}$ is specified indicates that the part was characterized using the ambient as the thermal reference. The board layout specified in the data sheet notes will help determine the applicability of the curve set.

B.1 JUNCTION-TO-AMBIENT THERMAL RESISTANCE MEASUREMENT

Equipment and Setup:

- Tesec DV240 Thermal Tester
- 1 cubic foot still air environment
- Thermal Test Board with 16 layouts defined by the size of the copper mounting pad and their relative surface placement. For layouts with copper on the top and bottom planes, there are 0.02 inch copper plated vias (heat pipes) connecting the two planes. See *Figure 2* and *Table 1* on the thermal application note for board layout and description. The conductivity of the FR-4 PCB used is 0.29 W/m-C. The length is 5.00 inches ± 0.005; width 4 50 inches ± 0.005; and thickness 0.062 inches ± 0.005. 2 oz. copper clad PCB.

The junction-to-ambient thermal measurement was conducted in accordance with the requirements of MIL-STD-883 and MIL-STD-750 with the exception of using 2 oz. copper and measuring diode current at 10 mA.

A test device is soldered on the thermal test board with minimum soldering. The copper mounting pad reaches the remote connection points through fine traces. Jumpers are used to bridge to the edge card connector. The fine traces and jumpers do not contribute significant thermal dissipation but serve the purpose of electrical connections. Using the intrinsic diode voltage measurement described above, the junction-to-ambient thermal resistance can be calculated.

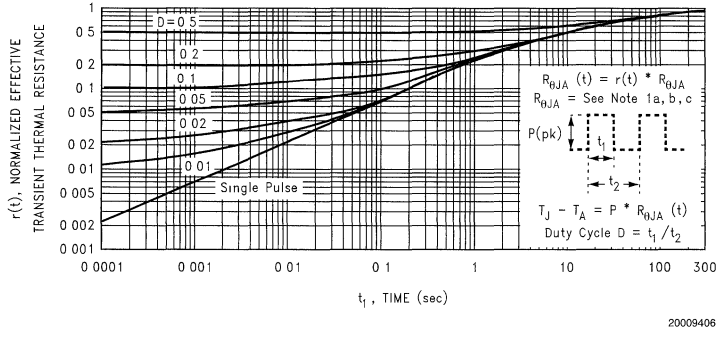


FIGURE 7. Normalized Transient Thermal Resistance Curves

Appendix B (Continued)

B.2 JUNCTION-TO-CASE THERMAL RESISTANCE MEASUREMENT

Equipment and Setup:

- Tesec DV240 Thermal Tester
- large aluminum heat sink
- type-K thermocouple with FLUKE 52 K/J Thermometer

The drain lead(s) is soldered on a 0.5 x 1.5 x 0.05 copper plate. The plate is mechanically clamped to a heat sink which is large enough to be considered ideal. Thermal grease is applied in-between the two planes to provide good thermal contact. Theoretically the case temperature should be held constant regardless of the conditions. Thus a thermocouple is used and fixed at the point of contact between the drain lead(s) and the copper plate surface, to account for any heatsink temperature change. Using the intrinsic diode voltage measurement described earlier, the junction-to-case thermal resistance can be obtained. A plot of junction-to-case thermal resistance for various packages is shown in *Figure 8*. Note $R_{\theta JC}$ can vary with die size and the effect is more prominent as $R_{\theta JC}$ decreases.

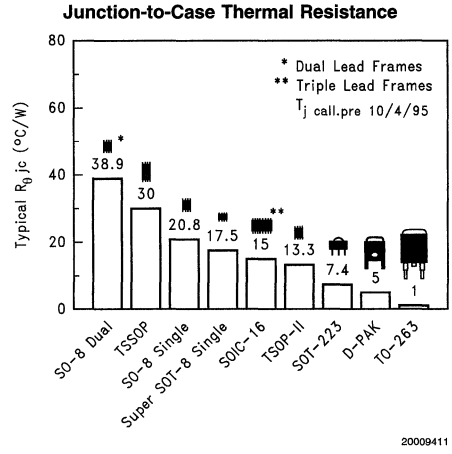
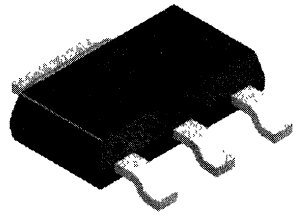


FIGURE 8. Junction-to-Case Thermal Resistance $R_{\theta JC}$ of Various Surface Mount Packages

Appendix C—Package Dimension

SOT-223



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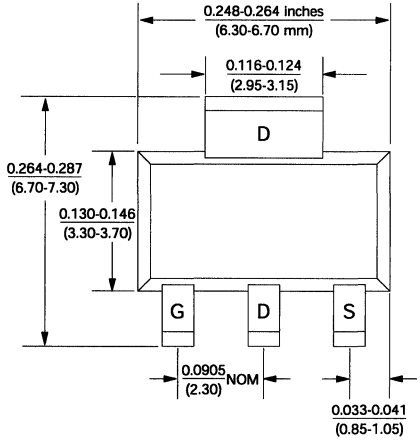
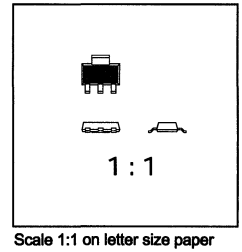
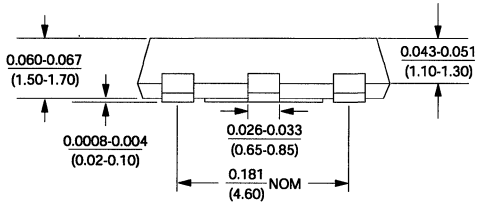
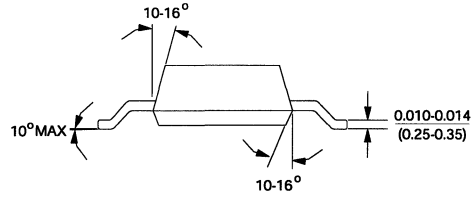




Scale 1:1 on letter size paper





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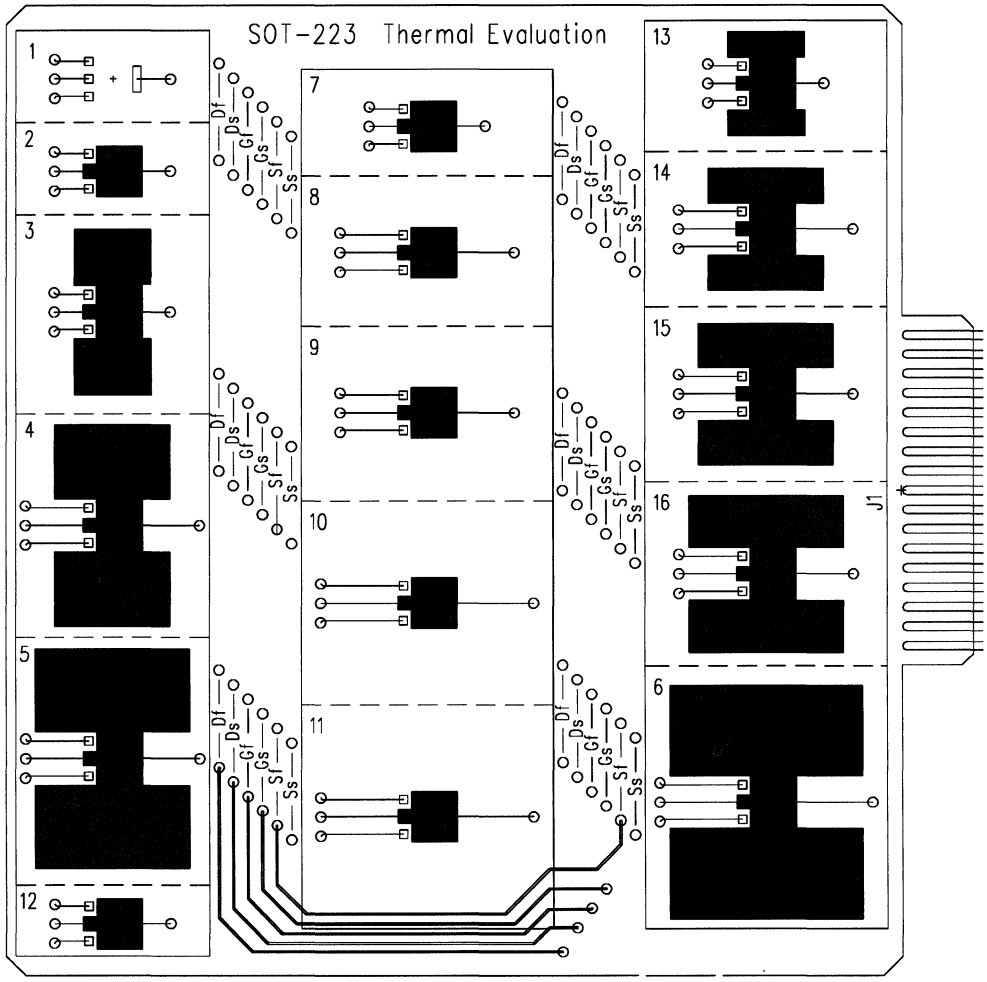
Appendix D

SOT-223 Thermal Board Top View in Actual Scale



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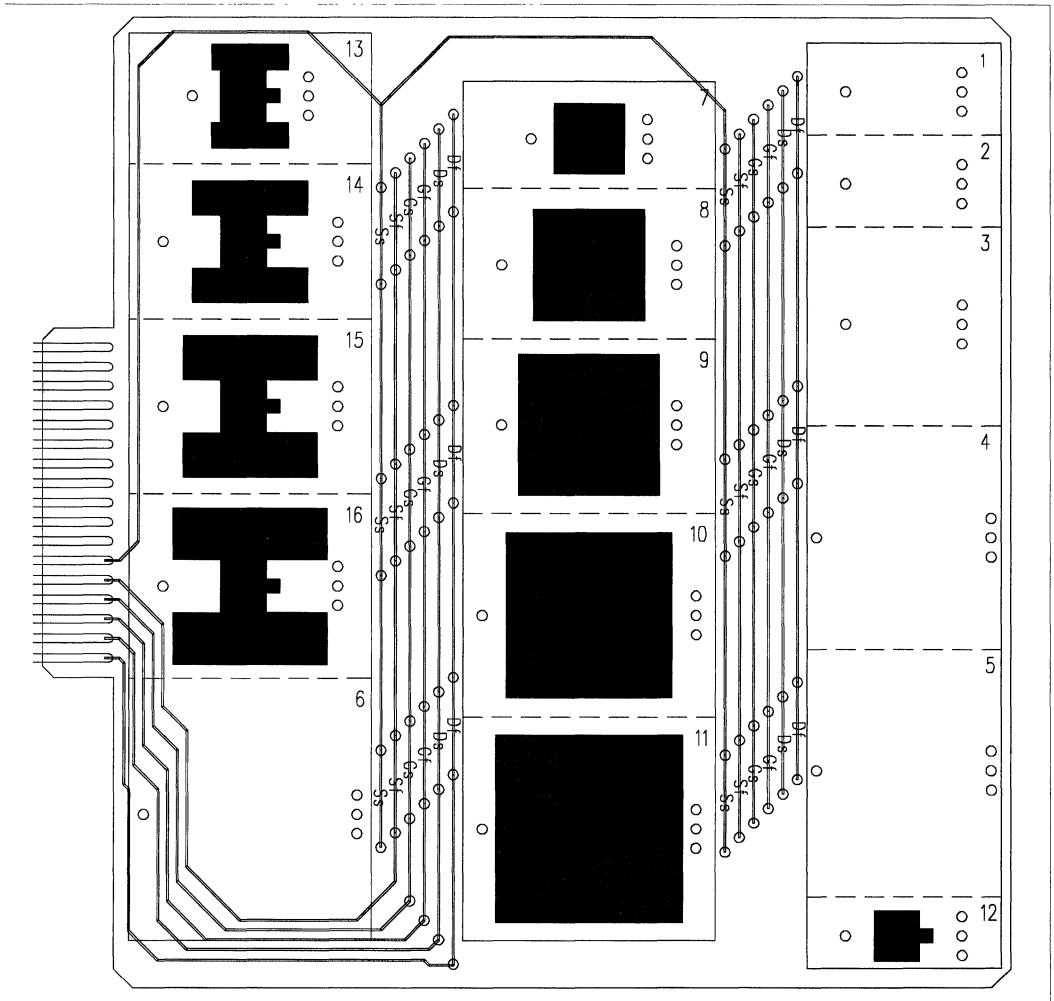
Appendix D (Continued)

SOT-223 Thermal Board Bottom View in Actual Scale



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Power Conversion in Line-Powered Equipment

National Semiconductor
Application Note 1061
Jon Cronk

Most equipment used in the office or home draws its power from the AC line. This line may be between 90 V_{AC}–264 V_{AC} and 47 Hz–63 Hz, depending on which portion of the world the equipment is located. However, the internal circuitry and motors rarely operate at these voltages. It now becomes necessary to provide Power Conversion within the equipment. This conversion means a power supply.

The following examples will describe typical power needs within line powered equipment and methods to solve those power needs. *Figure 1* shows an example of a power supply requirement for any given piece of line powered equipment.

The AC input line must be converted by the power supply to provide three DC output voltages which are well regulated over input line and output load. Most circuitry requires low output ripple on its supply voltage. Output ripple is generally specified to be no more than 1% of the output voltage.

The power conversion technique we will address includes a line transformer which provides safety isolation from the line voltage. The line transformer is the only portion of the power supply which needs to meet UL1950, CSA950, or EN60950 (IEC950) standards. All voltages produced by the transformer will be assumed to meet the requirements for SELV (Safe Extra Low Voltage) circuits. These transformers may be purchased as catalog items, or may be specified with custom requirements.

The power supply following the isolation transformer (see *Figure 2*) can be easily designed using National Semiconductor's Power ICs. Standard data sheets include design procedures and application hints on the use of all parts. Other parts will be supported with design software providing a complete solution.

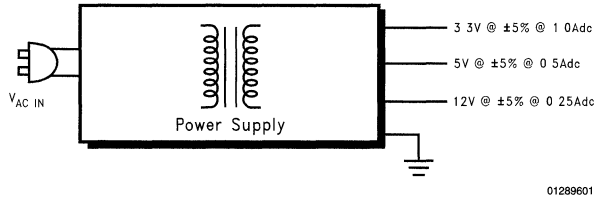


FIGURE 1. Typical Power Supply Requirement

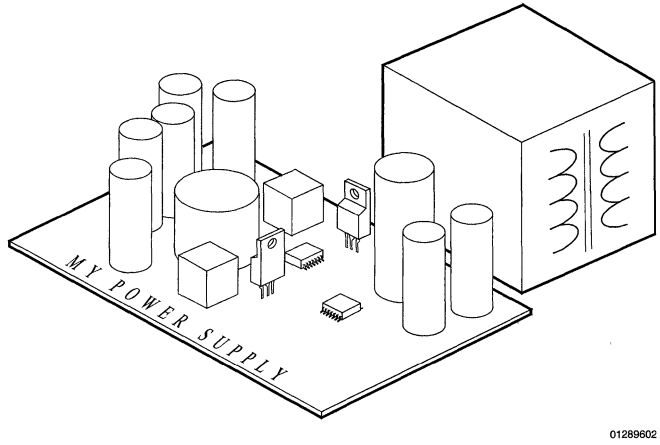


FIGURE 2. Power Supply Solution Using Isolation Transformer and Low-Voltage DC/DC Converters

Converting Line Voltage to Safe Low Voltage

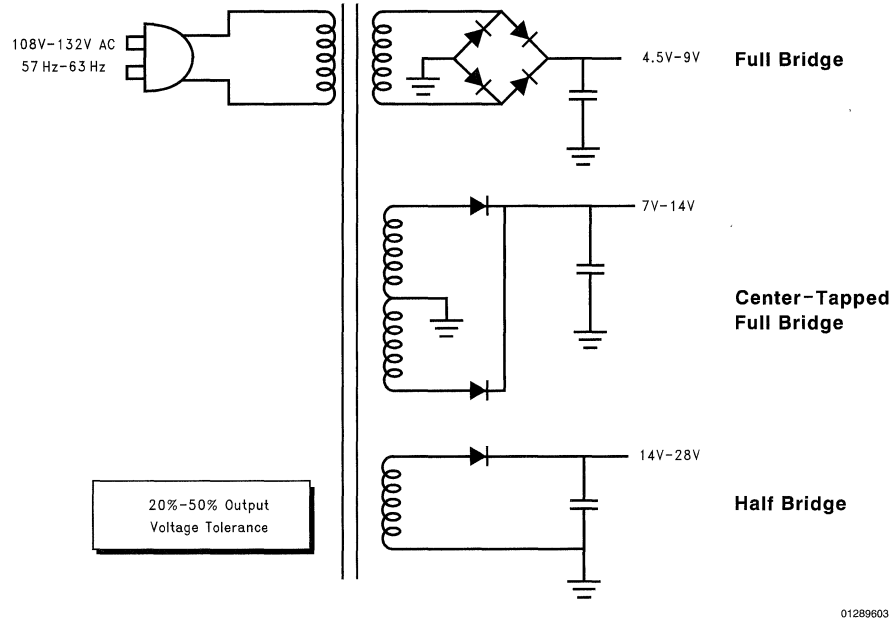


FIGURE 3. AC Line Rectification Methods

A line frequency transformer will be used to convert the hazardous line voltage to an isolated safe low voltage. One must understand the characteristics of low frequency line transformers to begin to design this type of power supply.

Figure 3 shows three different rectification techniques to develop a basic DC voltage source. The first, Full Bridge, is most efficient in the transformer, but requires a four diode rectification bridge. The second, Center-Tapped Full Bridge, requires more turns of wire in the secondary, but saves two diodes. The output ripple on both Full Bridge designs is the same. The last, Half Bridge, is a low cost method best for low output power. The half bridge creates a DC bias on the winding and as a result should only be used for very low current outputs. A half bridge will also give higher output ripple.

Output regulation is poor in a line transformer. If one assumes an ideal transformer, the regulation of the output will be no better than the input. Typical design requirements for input voltage is nominal ±10% (some require ±12.5%). In the case above, nominal is 120 V_{AC}.

Given a line variation of 10%, the output voltage tolerance is no better than ±10%. Adding the resistance of the transformer windings results in output voltage variation with load. The change in output voltage with load is a complex function. The definitive analysis can be found in a paper published by O.H. Shade in the July, 1943 Proceedings of the Institute of Radio Engineers entitled *Analysis of Rectifier Operation.* Although Shade used vacuum tube rectifiers, the analysis still holds true for modern diodes. In general, load regulation can vary from 10% to 40%. In the example above, the load regulation is 25%.

The size of the transformer is a function of a number of items: output power, load regulation, efficiency, maximum allowable temperature rise, and cost (core material is the primary variable).

Since the output voltages are poorly regulated, they can not be used as the output of the power supply. Additional regulation is necessary

Selecting the DC/DC Conversion Method

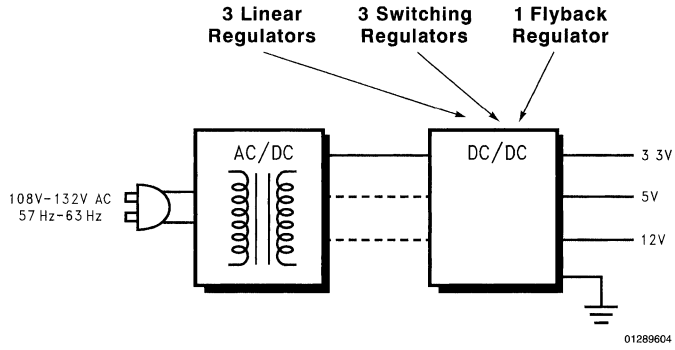


FIGURE 4. DC/DC Converter Options

As shown in *Figure 4*, there are generally three ways to provide the tightly regulated DC outputs required in this example.

The first is using three linear regulators from three different transformer outputs. This is the lowest efficiency solution. However, it is also the easiest to design and has the lowest component count. This solution requires an output winding for each supply to obtain acceptable power loss in the linear regulators.

The second is using three switching regulators (buck DC/DC) from a single transformer output. This provides excellent efficiency. However, the design complexity increases slightly and component count may increase. This solution requires only a single poorly regulated output from the transformer.

The third is a single flyback switching regulator. This also provides good efficiency, but is even more complex. The example above has no compelling reason to use a flyback regulator. A more appropriate set of requirements for this type of switching regulator will be presented later.

The solution in *Figure 5* shows how one would use linear regulators to obtain the desired regulated output voltages. The bulk capacitors across the rectified transformer windings may be reduced depending on the transformer being used. The linear regulators provide exceptional rejection of the 120 Hz ripple voltage found at the output of the transformer as long as the voltage does not go below the dropout voltage of the linear regulator. The regulator output capacitors are selected using the Application Hints in the datasheet for each part.

Each linear regulator must have a heat sink to prevent over heating. All calculations for power loss in the linear regulators will be performed at 132 V_{AC} input to the transformer and full load on the outputs. This is the worst case condition. The power loss in the linear regulator can be described as:

$$P_{LOSS} = V_{IN} \times I_{GND} + (V_{IN} - V_{OUT}) \times I_L$$

Where V_{IN} is the average DC from the transformer, I_{GND} is the ground pin current at full load (see data sheet), and I_L is the output current.

The LM3940 is the low dropout regulator chosen for the 3.3V output at 1 A_{DC}. V_{IN} is approximately 5.5 V_{DC}, and the calculated power loss is 2.8W (I_{GND} = 110 mA).

The LP2960 is the low dropout regulator chosen for the 5.0V output at 0.5 A_{DC}. V_{IN} is approximately 7.3 V_{DC}, and the calculated power loss is 1.3W (I_{GND} = 21 mA, max).

The LM2952 is the low dropout regulator chosen for the 12V output at 0.25 A_{DC}. V_{IN} is approximately 15.9 V_{DC}, and the calculated power loss is 1.3W (I_{GND} = 21 mA, max).

The total output power is 8.8W and the total power loss is 5.4W. As a result, the line transformer must provide 14.2W. If lower cost non-LDO were used, there would be an additional 3.8W loss (because of the higher input voltage required, countered by lower supply current). This would result in a 27% increase in transformer size.

If a simple transformer with a single winding was used with LDO regulators, the extra loss would be 14.9W. 12W of this would be the loss in the 3.3V regulator dropping the voltage down from a 14V winding! As a result, 3 windings are required.

Selecting the DC/DC Conversion Method (Continued)

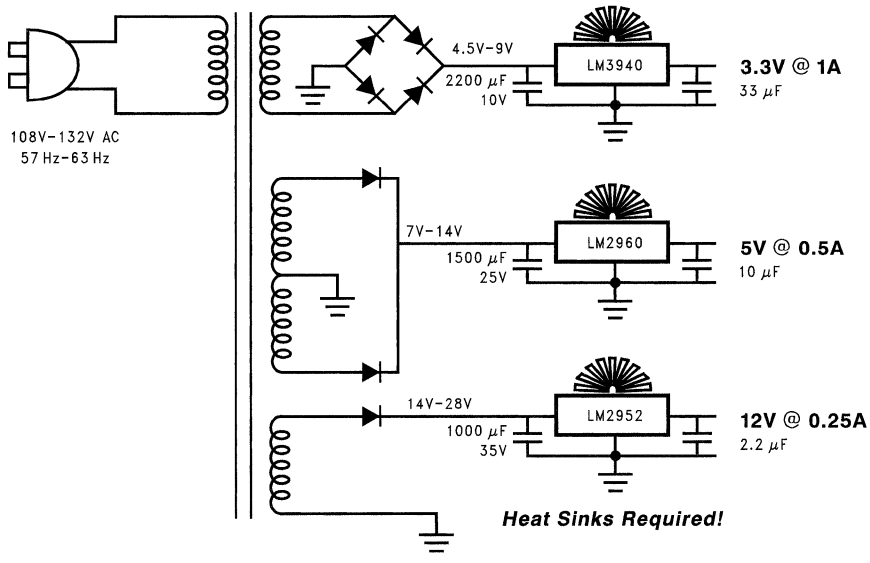


FIGURE 5. Power Supply Solution Using Linear Regulators

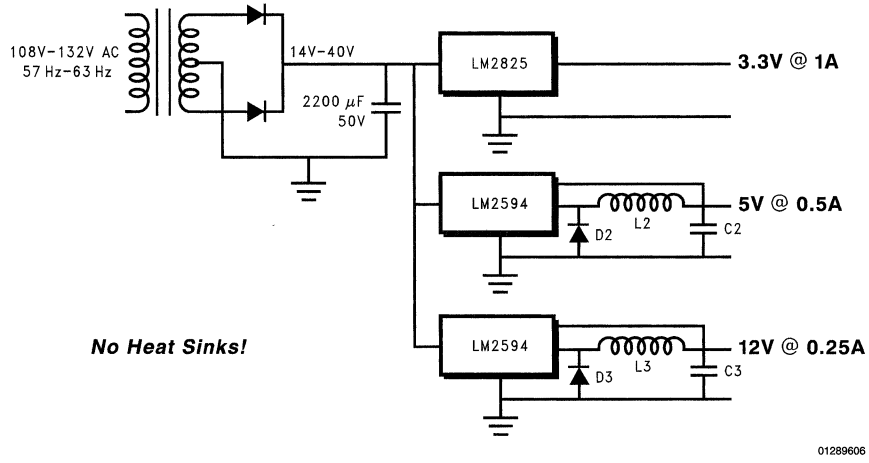


FIGURE 6. Power Supply Solution Using Step-Down Switching Regulators

Figure 6 shows a solution using three switching regulators. The average voltage supplied by the line transformer is 14V–40V. This voltage represents a relaxation of the line transformer load regulation (from 25% to 40%) and can allow a smaller transtormer. Again, the size of the input capacitor may be reduced and 120 Hz ripple rejection is excellent.

None of the switching regulators requires a heat sink given proper heat sinking to the PCB (Printed Circuit Board).

The components are selected by a software design tool, Switchers Made Simple (ver. 4.2.1), which is available for use with SIMPLE SWITCHER DC/DC Converters. National's WEB site at http://www.national.com/ is the best place to get a current version.

The overall efficiency of this switching regulator solution is approximately 80%. Therefore, the line transformer only needs to provide 11W. By reducing the required power, line transformer used in this solution can be 22% smaller than that used in the previous linear regulator solution. Also, only one output winding is required, thus simplifying the transformer manufacture.

Design for 3-Output Modem Power Supply

The design of *Figure 7*, for a modem application, required a DC/DC converter that was easy to configure and had low power loss. The modem was external and required that all output voltages be generated from a single output on a plug in wall transformer. To meet these needs, a multi-output flyback switching regulator was used to regulate the voltage developed by the line transformer. Not only does the use of a switching regulator keep the power loss much lower than if a linear regulator were used, the flyback topology is well suited for providing negative voltages while using one of the positive outputs as the feedback point.

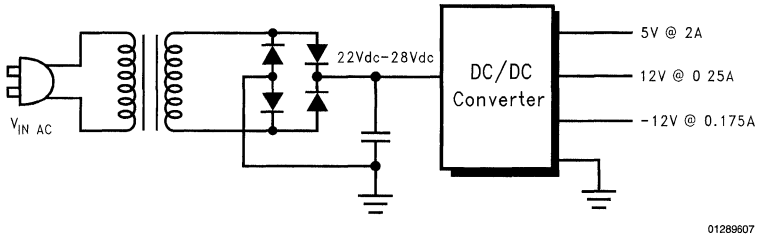


FIGURE 7. 3-Output Flyback Converter Provides Power for Modem

The easiest way to develop such a DC/DC converter is to generate a SIMPLE SWITCHER converter design with the software tool "Switchers Made Simple". The customer requirements were entered into the software and the resulting design is shown in *Figure 8*. This DC/DC convertor is approximately 75% efficient.

One important thing to note is that only the +5V output is directly regulated. The 12V and –12V outputs will vary over line and load much more than the 5V winding. For example, if the 5V winding only varies 1% over line and load, the 12V outputs may vary by 5%. This phenomenom is called "cross-regulation". It is a function of the design of the flyback transformer and the line and load range on all the outputs. For more information on this subject, reference a paper published in the 1995 PCIM Proceedings entitled *Improving Cross Regulation of Multiple Output Flyback Converters* written by J. Marrero of National Semiconductor.

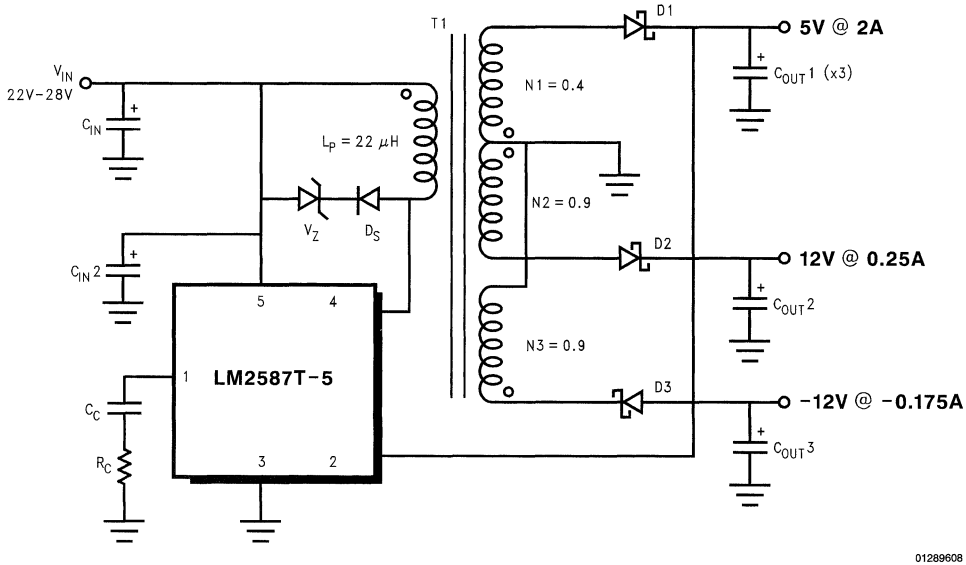


FIGURE 8. Schematic for Power Supply of *Figure 7*

Design for 3-Output Modem Power Supply (Continued)

U_1	5.00A	National	LM2587T-5
T_1	(Software provides detailed specification ...)		
C_{IN}	270.00 µF*	Nichicon	UPL1J271MRH
C_{IN2}	100.00 nF	AVX	SR595C104KAA
C_{OUT1}	2.70 mF (x3)	Nichicon	UPL1V272MRH
C_{OUT2}	330.00 µF	Nichicon	UPL1V331MPH
C_{OUT3}	270.00 µF	Nichicon	UPL1V271MPH
R_C	3.00 kW	Dale	CCF-07302J
C_C	330.00 nF	AVX	TAPA334K035R
D1	Schottky	Motorola	MBR745
D2	Schottky	Motorola	MBR1100
D3	Schottky	Motorola	MBR1100
VZ	20.00V	Motorola	SA20A
D_S	Ultrafast	Motorola	MUR120

*May require a larger value if used as the bulk capacitor for the line transformer.

FIGURE 9. Component Summary for the Circuit of *Figure 8*, as Generated by Switchers Made Simple 4.2

Undervoltage Lockout

Although the power supply is designed to operate properly over a given input voltage range, there is no guarantee that the line voltage available to the customer will always stay within that range. For over-voltage and transient conditions, we can protect our power supply and other internal circuitry by using a zener diode to clamp the input voltage. For brown out conditions we can use an undervoltage lockout circuit in conjunction with the shutdown pins on the Simple Switchers.

The undervoltage lockout must have special features due to the load regulation of the 60 Hz transformer. If we were to set a fixed on/off voltage for the power supply the following sequence of events would occur:

1. The input voltage falls below our minimum operating point (say 105 V_{AC}).
2. The undervoltage circuit trips and turns off the power supply and equipment.
3. The 60 Hz transformer is unloaded and the output voltage jumps up above the on/off trip point.
4. The power supplies try to start and pulls the output of the 60 Hz transformer down again.
5. Steps 2 through 4 repeat constantly causing the power supplies and equipment to oscillate on and off.

The problem is the difference between no-load and loaded output voltage of the 60 Hz transformer. Our undervoltage lockout must be able to turn on the power supplies once the input voltage is within our operating range (about 108 V_{AC}).

But, once the supplies turn on, recognize that the output voltage will be pulled down, and not turn off until the input falls below our operating minimum (about 100 V_{AC}).

By using an undervoltage circuit with hysteresis (illustrated in *Figure 10*), we can prevent the power supply from oscillating on and off.

$V_{(turn\ on)}$ is the no load voltage from the transformer. This is very close to

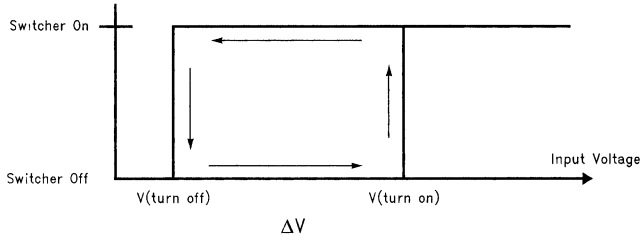
$$108 \bullet \frac{Ns}{Np} \bullet \sqrt{2}$$

$V_{(turn\ off)}$ is the full load voltage from the transformer at 100 V_{AC}. This value is very sensitive to the load conditions for each design, and should be measured on the bench during design.

ΔV is the difference between these two voltages, and is the value we will use for the undervoltage lockout hysteresis.

The schematic and equations of *Figure 11* will provide a hysteretic undervoltage lockout circuit design. Some assumptions have been made to simplify the equations, primarily that $R_h \gg R_1$ and R_2. Also, the current through R_1 and R_2 should be at least 10 times greater than the input current to the comparator. The LM6511 input current is typically less than 50 nA (datasheet maximum over all conditions is 200 nA which occurs at –40°C).

Undervoltage Lockout (Continued)



- $V_{(turn\ on)}$ = No load voltage from transformer @108 V_{AC}
- $V_{(turn\ off)}$ = Full load voltage from transformer @100 V_{AC}
- $\Delta V = V_{(turn\ on)} - V_{(turn\ off)}$, Hysteresis

FIGURE 10. Hysteresis Controls Turn-on and Turn-off Thresholds of Undervoltage Circuit

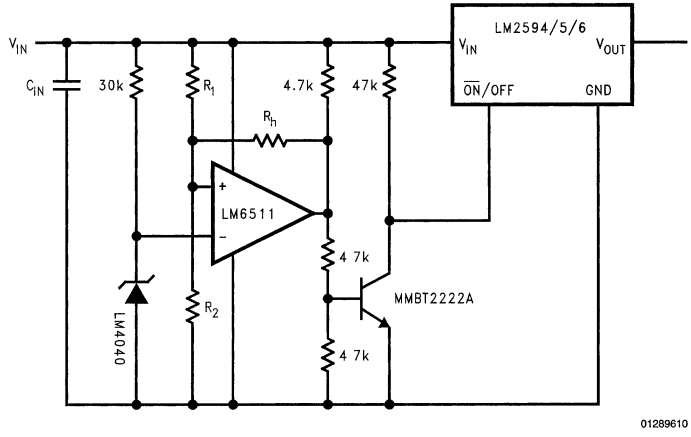


FIGURE 11. Undervoltage Lockout Circuit with Hysteresis

Undervoltage Lockout (Continued)

Once the circuit has been incorporated with the complete power supply and powered circuitry, the values of R_h, R_1, and R_2 can be optimized.

Make sure to check that the regulator you are using turns on by grounding the on/off pin. Some regulators turn off when grounding this pin. If the logic needs to be inverted, just swap the inputs to the comparator.

Comparison of Power Supply Solutions

Linear Regulators	Switching Regulators
No EMI from power supply	Smaller line transformer • Lower power • One winding • Poorer regulation okay
Fewer components in converter	One diode bridge and bulk capacitor required
Typically lower cost	No heat sinks*

*Small heat sinks may be required at higher ambient temperature or output power levels

FIGURE 12. Linear Regulator Solutions vs Switching Regulator Solutions

As indicated in *Figure 12*, each type of regulator has its own strengths and weaknesses.

The linear regulator provides a fast simple solution. Overall, the linear regulator will be the lowest cost solution. The drawbacks are a complicated line transformer with multiple output windings, low efficiency, and heat sinks to dissipate the power lost in the regulator.

A multi-output line transformer, with output voltages close to the desired levels, can be used with low-dropout linear regulators on each output. This yields a low-component-count power supply.

These LDOs may include:

- LP2980/2 for ≤50 mA loads
- LP2950/51/81 for ≤100 mA loads
- LP2952/53/54/57 for ≤250 mA loads
- LP2960 for ≤500 mA loads
- LM3940 for ≤1 Amp loads

Switching regulators provide a more efficient solution at the expense of slightly greater complexity. The line transformer can be less expensive than that used for the linear regulator. One benefit of higher efficiency is the ability to omit heat sinks unless the ambient temperature is very high (>50˚C at rated current). In some cases the cost of adding a heat sink to a linear regulator is more than a switching regulator.

A single-output line transformer can be used with multiple buck regulators. This yields a high-efficiency power supply with independent control of each output. Or, you could use a single multi-output flyback switching regulator. This yields a relatively simple, high-efficiency supply.

One issue which may arise is EMI from the switching regulators getting back into the AC line. Linear regulators do not generate any EMI. Switching regulators may require a filter stage at the output of the line transformer if the bulk capacitor does not provide sufficient attenuation at the switching frequency.

While new requirements for harmonic content and power factor correction (PFC) are being put in place in Europe, they will not be required on the sub-50W power supplies we are discussing here. Power supplies above 75W input power will require input stages to limit harmonic distortion. All line frequency transformers feeding into an output rectifier and bulk capacitor have distorted input currents. For this reason, none of the solutions here are intended to address these requirements.

Simple Switcher Converters

While there are many types of DC/DC voltage converters on the market, there are few that combine the ease-of-use and adaptability of the SIMPLE SWITCHER DC/DC converters. See *Figure 13* for a selection guide of these converters.

SIMPLE SWITCHER products offer guaranteed system specifications, such as maximum output voltage tolerance, not just the tolerance of a subsection of the integrated circuit.

In addition, a SIMPLE SWITCHER is easy to configure, with a variety of standard output voltages available. A few external components are required, and they are fully specified in the product documentation. Components which may be unfamiliar to the system designer, such as magnetics, are available as standard part numbers from other vendors.

"Switchers Made Simple" design software is also available, to customize a SIMPLE SWITCHER converter for a specific application.

See our WEB site at http://www.national.com/sw/SimpleSwitcher/0,1043,0,00.html (Feb. 20, 1998).

Simple Switcher Converters (Continued)

Buck Converters	Switching Frequency	Output Current	Input Voltage Range	Features
LM2825	150 kHz	1.0A	4.75 V_{DC}–40 V_{DC}	Fully integrated DC/DC Convertor IC in a 24-pin DIP requiring no external components with TTL on/off and soft-start
LM2671	260 kHz	0.5A	7 V_{DC}–40 V_{DC}	High efficiency, SO-8, sync to 400 kHz, softstart, TTL on/off
LM2672	260 kHz	1.0A	7 V_{DC}–40 V_{DC}	High efficiency, SO-8, sync to 400 kHz, softstart, TTL on/off
LM2674	260 kHz	0.5A	7 V_{DC}–40 V_{DC}	High efficiency, SO-8, TTL on/off
LM2675	260 kHz	1.0A	7 V_{DC}–40 V_{DC}	High efficiency, SO-8, TTL on/off
LM267X	260 kHz	3.0A, 5.0A	7 V_{DC}–40 V_{DC}	Future products, check for availability
LM2594	150 kHz	0.5A	5 V_{DC}–40 V_{DC}	SO-8, TTL on/off
LM2595	150 kHz	1.0A	5 V_{DC}–40 V_{DC}	TTL on/off
LM2596	150 kHz	3.0A	5 V_{DC}–40 V_{DC}	TTL on/off
LM2597	150 kHz	0.5A	5 V_{DC}–40 V_{DC}	SO-8, Soft-start, µP reset and error flag, TTL on/off
LM2598	150 kHz	1.0A	5 V_{DC}–40 V_{DC}	Soft-start, µP reset and error flag, TTL on/off
LM2599	150 kHz	3.0A	5 V_{DC}–40 V_{DC}	Soft-start, µP reset/error flag, TTL on/off
LM2574 LM2574HV	52 kHz	0.5A	7 V_{DC}–40 V_{DC} 7 V_{DC}–60 V_{DC}	TTL on/off
LM2575 LM2575HV	52 kHz	1.0A	7 V_{DC}–40 V_{DC} 7 V_{DC}–60 V_{DC}	TTL on/off
LM2576 LM2576HV	52 kHz	3.0A	7 V_{DC}–40 V_{DC} 7 V_{DC}–60 V_{DC}	TTL on/off
Flyback or Boost Converters		**Switch Current**		
LM2585	100 kHz	3.0A	4 V_{DC}–40 V_{DC}	
LM2586	100 kHz	3.0A	4 V_{DC}–40 V_{DC}	Synch, on/off, freq. adj to 200 kHz
LM2587	100 kHz	5.0A	4 V_{DC}–40 V_{DC}	
LM2588	100 kHz	5.0A	4 V_{DC}–40 V_{DC}	Synch, on/off, freq. adj to 200 kHz
LM2577	52 kHz	3.0A	4 V_{DC}–40 V_{DC}	

FIGURE 13. SIMPLE SWITCHER® Power Converters

Low Cost Boost Converters Using LM3578A

National Semiconductor
Application Note 1066
Ravindra Ambatipudi

Abstract

The LM3578A integrated circuit is a switching regulator with all the power, control, and protection features. It operates over a wide input voltage range. This together with its low-cost makes it a very popular choice for use in switching regulators. This paper will present several low cost boost converter circuits developed using the LM3578A switching regulator. The operation and the design of the boost converter will also be discussed in detail.

Introduction

The Boost or Step-up converter converts a DC voltage to a higher DC voltage. *Figure 1* shows the basic boost topology. When the switch SW is turned on, energy is stored in the inductor L and the inductor current i_L ramps up at a slope determined by the input voltage. Diode D is off during this period. Once the switch, SW, turns off, diode D starts to conduct and the energy stored in the inductor is released to the load. Current in the inductor ramps down at a slope determined by the difference between the input and output voltages.

MODES OF OPERATION

Based on the amount of energy that is delivered to the load during each switching period, the boost converter can be classified into continuous or discontinuous conduction mode. If all the energy stored in the inductor is delivered to the load during each switching cycle, the mode of operation is classified as discontinuous conduction mode (DCM). In this mode, the inductor current ramps down all the way to zero during the switch off-time. If only part of the energy is delivered to the load, then the converter is said to be operating in continuous conduction mode (CCM). *Figure 2* shows the inductor current waveforms for all the modes of operation.

The mode of operation is a fundamental factor in determining the electrical characteristics of the converter. The characteristics vary significantly from one mode to the other.

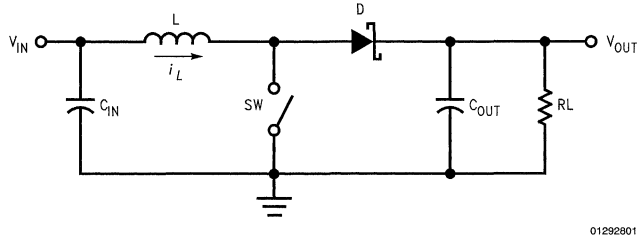


FIGURE 1. Basic Boost Topology

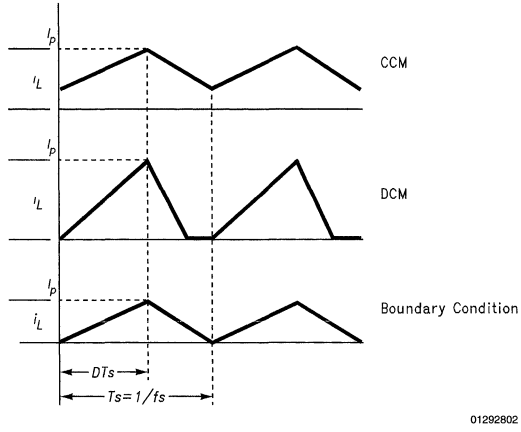


FIGURE 2. Inductor Current (i_L) Waveforms

Introduction (Continued)

CONTINUOUS VERSUS DISCONTINUOUS MODE

Both modes of operation have advantages and disadvantages. The main disadvantage in using CCM is the inherent stability problems (caused by the right-half-plane zero and the double pole in the small-signal control to output voltage transfer function). However, the switch and output diode peak currents are larger when the converter is operating in discontinuous mode. Larger peak currents necessitate using power switch and output diode with larger current and power dissipation ratings. Larger peak currents also force the designer to use larger output capacitors. The larger peak currents also cause greater EMI/RFI problems.

The mode of operation can be selected by the user. For very low load currents, discontinuous mode is preferred over continuous mode. If the load current requirements are high, then in order to minimize the peak currents and the associated problems, continuous mode is preferred. Two of the circuits presented in Section 3 have very low load current requirements. Hence, they have been selected to operate in discontinuous mode. The third circuit has very high peak current requirements and is selected to operate in continuous mode.

Selection of Boost Power Stage Components

The boost converter design involves the selection of the inductor, the input and output capacitors, the power switch (included in the LM3578A), and the output diode. In order to select these components, it is necessary to know the duty cycle range and the peak currents.

Knowing the maximum and minimum input voltages, the output voltage, and the voltage drops across the output diode and the switch, the maximum and minimum duty cycles are calculated. Next, the average inductor current can be estimated from the load current and duty cycle. Now, assuming the peak to peak inductor current ripple to be certain percentage of the average inductor current ripple, the peak inductor current can be estimated. The inductor value can be calculated using the ripple current, switching frequency, input voltage, and duty cycle information. Finally, it is necessary to establish the boundary condition, i.e. the critical value of the inductor below which the converter will operate in discontinuous mode.

Once the inductor value has been chosen and the peak currents have been established, the other components can be selected very easily. The following paragraphs outline the selection of the boost power stage components, in a step by step approach.

SELECTION OF THE BOOST INDUCTOR

STEP 1: Given the maximum and minimum input voltages, the maximum and minimum duty cycles can calculated using the following equations:

$$D_{max} = \frac{\left(V_o + V_d - V_{in(min)}\right)}{\left(V_o + V_d - V_{ce(sat)}\right)} \quad (1)$$

$$D_{min} = \frac{\left(V_o + V_d - V_{in(max)}\right)}{\left(V_o + V_d - V_{ce(sat)}\right)} \quad (2)$$

In *Equations (1), (2)*, V_O is the output voltage, V_d is the forward voltage drop of the output diode D, and $V_{ce(sat)}$ is the on state voltage of the switch, SW. $V_{in(max)}$ and $V_{in(min)}$ are the maximum and minimum input voltages respectively.

STEP 2: The average inductor current (maximum) can be calculated using the output current, I_O as follows:

$$I_{L(avg)} = \frac{I_o}{1 - D_{max}} \quad (3)$$

STEP 3: Assume the peak to peak inductor current ripple, Δi_L to be a certain percentage of the average inductor current calculated in *Equation (3)*. The peak inductor current is then given by:

$$I_p = I_{L(avg)} + \frac{\Delta i_L}{2} \quad (4)$$

STEP 4: Knowing the switching frequency, f_s the required inductance value can be selected using the equation:

$$L_{(min)} = \frac{\left(V_{in(min)} - V_{ce(sat)}\right) D_{max}}{f_s \Delta i_L} \quad (5)$$

STEP 5: Calculate the boundary condition, i.e., the minimum inductance required to operate the inductor in continuous mode.

At the boundary between CCM and DCM modes of operation, the peak inductor current, I_p is same as the peak to peak inductor current ripple, Δi_L, as shown in *Figure 2*. Hence, the average inductor current is given by:

$$I_{L(avg)} = \frac{I_p}{2} \quad (6)$$

Using *Equations (3), (6)*

$$I_p = \frac{2I_o}{1 - D_{max}} \quad (7)$$

The critical value of the inductance to maintain the converter in continuous mode of operation, derived from *Equations (5), (7)* is given by:

$$L_{(crit)} = \frac{\left(V_{in(min)} - V_{ce(sat)}\right) D_{max}\left(1 - D_{max}\right)}{2 f_s I_o} \quad (8)$$

Using an inductance value lower than the critical value will result in discontinuous mode of operation. It can also be observed from *Equations (5), (8)* that increasing the switching frequency helps in reducing the size of the inductor.

Selection of Boost Power Stage Components (Continued)

SELECTION OF POWER SWITCH

The power switch is internal to the LM3578A. In general , it is necessary to ensure that the estimated peak switch current (which is nothing but the peak inductor current, I_p calculated above) does not exceed the rated current of the switch. It is also necessary to ensure that the off-state voltage rating of the switch is never exceeded. The internal transistor in the LM3578A switching regulator is rated for a peak current of 750 mA. The off-state sustaining voltage of the internal transistor is 50V.

SELECTION OF THE OUTPUT CAPACITOR

In the boost converter, the instantaneous value of currents entering and exiting the output capacitor is very high, since there is no inductive element between the output diode and the capacitor. This high current flows through the equivalent series resistance (ESR) and equivalent series inductance (ESL) of the capacitor. ESR increases the capacitor temperature and increases ripple voltage. ESL adds sharp spikes to the ripple voltage waveform. Hence, it is desired to use output capacitors with very low ESR and ESL.

The peak to peak output ripple voltage, ΔV_O, is given by

$$\Delta V_o = \frac{I_{o\,max}\left(1 - D_{min}\right)}{f_s C_o} + I_p R_{esr} \tag{9}$$

where I_{Omax} is the maximum output current. The output capacitor, C_O can be selected using *Equation (9)*. It should be noted that the ripple voltage due to the ESR, (R_{esr}) is dominant in *Equation (9)*. Also, ESL will add sharp spikes over the ripple voltage given by *Equation (9)*. The ESR of the selected capacitor can be determined from the manufacturer catalogs or by actual bench measurement. If the value of the ripple exceeds the desired ripple voltage, then there are two choices- paralleling two or more capacitors to lower the effective ESR and ESL, or using a secondary LC filter. In general, low values of ESR are achieved by using large value capacitors or by paralleling smaller value capacitors. (Note: Tantalum capacitors are known to have very low ESR. But they are expensive when compared to electrolytic capacitors.)

SELECTION OF THE INPUT CAPACITOR

In boost switching regulators, triangular ripple current is drawn from the supply voltage due to the switching action. This appears as noise on the input line. This problem is less severe in boost converter due to the presence of inductor in series with input line. Select the input capacitor for

$$I_{rms} = \frac{I_p}{\sqrt{12}} \tag{10}$$

From *Equation (10)*, it can be observed that the rms current value is very low. Hence, a very small value capacitor is sufficient for boost converters.

SELECTION OF THE OUTPUT DIODE

As in all switching power supplies, two factors govern the choice of output rectifier—the forward voltage drop, V_F, and the reverse recovery time, t_{rr}. V_F determines the forward conduction loss and should be as low as possible. The reverse recovery time of the diode (and also the forward recovery time) should be as low as possible for minimizing the switching losses and RFI problems. Schottky rectifiers have very low forward voltage drops and reverse recovery times.

The maximum reverse bias voltage on the output rectifier is given by:

$$V_r = V_o - V_{ce(sat)} \tag{11}$$

Select a Schottky diode satisfying the reverse voltage and peak current ratings given by *Equations (4), (11)* respectively.

Low Cost Boost Converters

This section will present several low-cost boost circuits based on the LM3578A switching regulator. The LM3578A IC is a switching regulator featuring an internal comparator, oscillator, protection circuitry and a transistor. This IC operates from supply voltages ranging from 2V to 40V. This wide supply voltage range, together with its low cost makes it very popular. The transistor internal to LM3578A can handle currents only up to 750 mA. However, for higher load current requirements, this internal transistor can be used to drive an external transistor with higher current rating such as the npn transistor, D44C3A.

VOLTAGE DOUBLER CIRCUIT

Figure 3 shows a low-cost voltage doubler circuit used typically in the *RF card of a cable modem*. This converter uses the LM3578A switching regulator for performing the required power conversion. The inductor and other power stage components are selected using the procedure discussed in Section 2. The converter specifications are as follows:

Input Voltage, V_{IN} = 12V

Output Voltage V_{OUT} = 24V

Load Current I_L = 10 mA (max.)

Switching Frequency, f_s = 100 kHz

Since the load current requirements are very low, this converter is chosen to operate in discontinuous conduction mode. The output voltage is maintained at 24V by the feedback network consisting of the resistors, R_{f1} and R_{f2}. The reference pin (pin 1) is set at 1V using these resistors. Capacitor C_{IN2} is needed to ensure low noise at the input.

The switching frequency is set by using the timing capacitor C_T. Choosing a value of 680 pF for C_T sets the switching frequency at 100 kHz. Capacitor C_1 (typically between 10-25 pF), together with the feedback resistors (R_{F1} and R_{F2}), is used for compensation. For more details on the choice of the above components, please refer to the data sheet for LM3578A.

Low Cost Boost Converters (Continued)

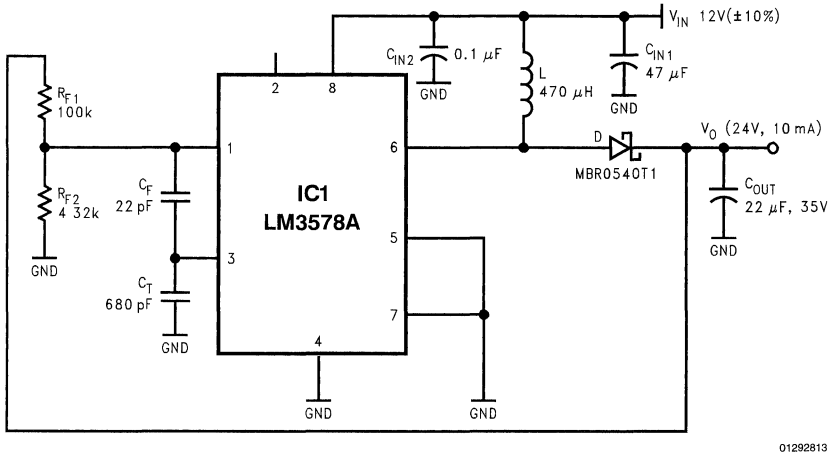


FIGURE 3.

Parts List

Designator	Value/Rating	Description
IC1	—	LM3578M, Switching Regulator
D	40V, 0.5A	MBR0540T1, Output Diode
L	470 µH, 60 mA	Boost Inductor
C_{IN1}	47 µF, 16V	Input Capacitor
C_{IN2}	0.1 µF, 50V	Input Capacitor (Ceramic)
C_{OUT}	22 µF, 35V	Output Capacitor
R_{F1}	100k	Feedback Resistor
R_{F2}	5k	Feedback Resistor
C_F	22 pF	Feedback Capacitor
C_T	680 pF	Timing Capacitor, Sets the Switching Frequency

BOOST CONVERTER FOR WIDE BAND TUNERS

Figure 4 shows a 5V to 27V boost converter used typically to create a high voltage for wide band tuners. Wide band cable and DSS tuners require about 27V at 5 mA load current to bias the VCO varactor. The converter specifications are as follows:

Input Voltage, V_{IN} = 5V

Output Voltage, V_{OUT} = 27V

Load Current I_L = 20 mA (max.)

Switching Frequency, f_s = 90 kHz

Input Ripple Voltage: 17 mV

Output Ripple Voltage: 58 mV

The design of this circuit is very straightforward and is very similar to the design of the voltage doubler circuit discussed above. As in previous case, since the load current requirements are very low, this converter is chosen to operate in discontinuous conduction mode. The feedback resistors (R_{F1} and R_{F2}), the timing capacitor, C_T and the compensation capacitor, C_C are chosen in the same way. In order to ensure low noise at the input, it is essential to add a high-frequency ceramic capacitor C_{IN2} at the input rail, as shown in *Figure 4*.

Low Cost Boost Converters (Continued)

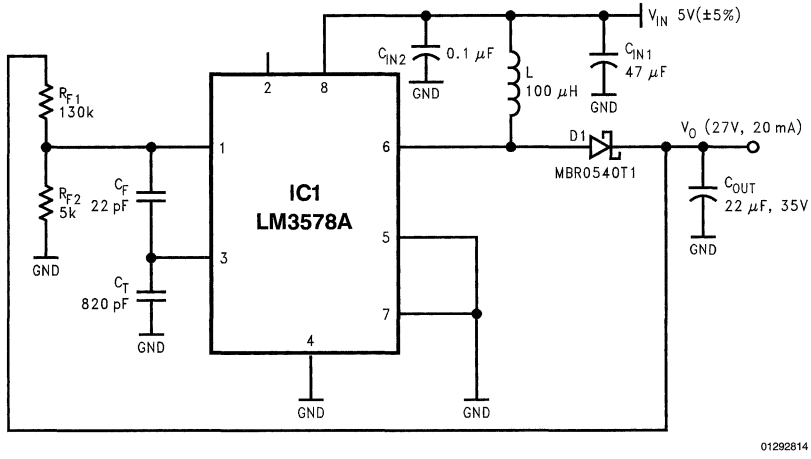


FIGURE 4.

Parts List

Designator	Value/Rating	Description
IC1	—	LM3578M, Switching Regulator
D	40V, 0.5A	MBR0540T1, Output Diode
L	100 µH, 100 mA	Boost Inductor
C_{IN1}	47 µF, 10V	Input Capacitor
C_{IN2}	0.1 µF, 10V	Input Capacitor (Ceramic)
C_{OUT}	22 µF, 35V	Output Capacitor
R_{F1}	130k	Feedback Resistor
R_{F2}	5k	Feedback Resistor
C_F	22 pF	Feedback Capacitor
C_T	820 pF	Timing Capacitor, Sets the Switching Frequency

LOW COST BOOST CIRCUIT FOR I/O CARDS

Figure 5 shows a low cost boost converter which converts a 3.3V input to 5V at 600 mA load current. This circuit is typically used in I/O cards.

Converter Specifications:

Input Voltage, V_{in} = 3.3V (±10%)

Output Voltage = 5V (±5%)

Output Current = 0 mA–600 mA

Efficiency = 80%

The maximum and minimum duty cycles calculated using *Equations (1), (2)* are equal to 0.52 and 0.4 respectively.

The average inductor current calculated using *Equation (3)* is:

$$I_{L(avg.)} = \frac{I_{o(max)}}{1 - D_{max}} = \frac{0.6}{1 - 0.52} = 1.25A$$

Assuming the peak to peak ripple current to be 50% of the average inductor current, the peak current calculated using *Equation (4)* is equal to:

$$I_{L(peak)} = I_{L(avg)} + \frac{\Delta I_L}{2} = 1.25 + \frac{0.5 \times 1.25}{2} = 1.563A$$

The peak current calculated above is very much higher than the rated current of the internal switch in the LM3578A. Hence, it is necessary to use an external transistor or a FET. The selected external switch should be capable of handling the high peak currents. The internal transistor in LM3578A can handle up to 750 mA. So the current gain of the external transistor should be sufficient at the peak primary current. The off state voltage rating, V_{CE}, of the transistor should be at least 10V. One npn transistor meeting these requirements is D44C3A. The current gain (h_{fe}) of this transistor at the peak current of 1.563A is about 50. So the maximum current that the internal transistor needs to provide is equal to 1.563/50 = 31 mA, which is very much less than the rated current of the internal transistor.

The circuit shown in *Figure 5* performs the required conversion using LM3578A and D44C3A npn transistor. The power stage components are selected using the procedure discussed in Section 2. From the above calculations, it can be

Low Cost Boost Converters

(Continued)

seen that the peak current requirements are very high. Hence, this converter is chosen to operate in continuous conduction mode. The boost converter operating in continuous mode has inherent stability problems (due to the right half plane zero and the double pole in the small-signal control to output transfer function). Hence, additional compensation is needed in the control loop. This additional compensation is provided by the capacitor C_{C1} (typically around 1 nF) and the resistor R_{C1} (typically between 100k and 200k).

The current limiting in this circuit is activated whenever pin 7 is pulled 110 mV above the ground. The voltage across the current sense resistor, R_{sn} is sensed in order to prevent excessive current through the external switch. The value of R_{sn} is given by:

$$R_{sn} = \frac{0.110}{I_{lim}}\ \Omega \qquad (12)$$

where I_{lim} is the desired current limit set point. As an example, for the circuit shown in *Figure 5*, the peak switch current calculated above is 1.563A. Hence, if the desired current, I_{lim} is set at 2A, then the value of the current-sense resistor will be R_{sn} = 0.110/2 = 0.055Ω.

For cost reasons, the current-sense resistor can also be fabricated on a copper trace. Reference[1] describes the procedure for calculating the trace length and width.

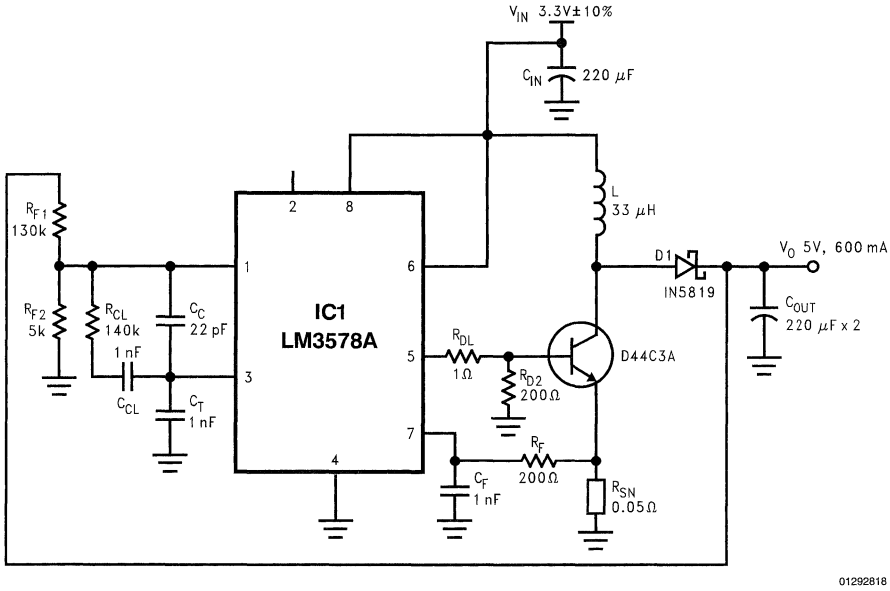


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FIGURE 5.

Parts List

Designator	Value/Rating	Description
IC1	—	LM3578A Switching Regulator
Q_1	5A, 30V	D44C3A, NPM Transistor
D_1	1A, 40V	Diode, 1N5819
L	Lp-33 µH, Ip-2.0A	Inductor
C_{in}	220 µF, 6.3V	Input Capacitor
C_o	2 x 220 µF, 10V	Output Capacitor
R_{sn}	0.050Ω, 1W	Current Sense Resistor/Copper Trace
R_{F1}	40.06k, 1/4W	Feedback Resistor
R_{F2}	10k, 1/4W	Feedback Resistor
R_{d1}	1Ω, 1/4W	Base Drive Resistor

Low Cost Boost Converters (Continued)

Parts List (Continued)

Designator	Value/Rating	Description
R_{d2}	200Ω, 1/4W	Base Drive Resistor
R_f	2000Ω, 1/4W	Resistor for Spike Suppression
C_f	1 nF	Capacitor for Spike Suppression
C_T	820 pF	Timing Capacitor
C_c	22 pF	Compensation Capacitor
C_{c1}	1 nF	Compensation Capacitor
R_{c1}	140k	Compensation Capacitor

Summary

This paper has presented several low cost boost converters, designed using the LM3578A switching regulator. The circuits can be used in many different applications. The parts list has been provided for these circuits. Recommended layouts for these circuits have been presented in the appendix.

Layout is very critical in these circuits. Pins 1, 2, and 7 of LM3578A are very noise sensitive. So these pins should be placed away from high frequency noise sources in the circuit. It is also necessary to have the feedback trace away from the inductor. In order to avoid false triggering of current limiting circuitry, filtering is very much essential for the sensed current. It is also important to note that the current sense voltage shut down level has very high tolerance. The voltage can vary from 80 mV to 160 mV (typical value is 100 mV). This factor should be taken into consideration while selecting the current sense resistor.

The compensation capacitor, C_C connected between pins 1 and 3 should be typically between 10 to 25 pF. Using a larger value for C_C will start effecting the switching frequency. It is also necessary to note that LM3578A can skip pulses at very low load currents when the minimum duty cycle of each pulse provides more energy than the load demands. Under these conditions, the controller internal to the LM3578A starts skipping pulses to maintain the output voltage at its correct value. This mode of operation is also known as burst mode.

Although only three boost circuits have been presented, the design approach for other voltage and current levels is the same.

Appendix

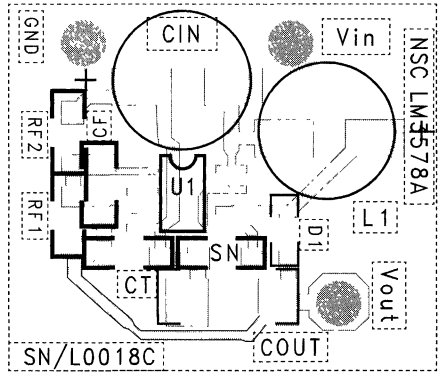
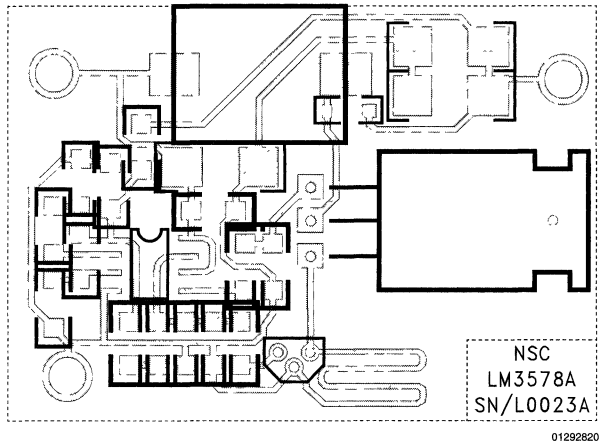


FIGURE 6. PCB Layout for the Circuits Shown in *Figures 3, 4* (Scale: 2:1)



Note: Copper trace is used as current sense resistor

FIGURE 7. PCB Layout for the Circuit Shown in *Figure 5* (Scale: 2:1)

References

1. National Semiconductor Application Note, AN1055: "Low Cost Multiple Output Flyback Converter for I/O Cards", 1996.
2. National Power ICs Databook.

A Low Cost, Low Parts-Count DC/DC Converter with Multiple Outputs

National Semiconductor
Application Note 1081
Musiri Srivathsan

Introduction

This application note describes a simple low cost, low parts-count multiple output DC/DC converter based on the LM2596 five terminal step-down switching regulator. The circuit described provides multiple output voltages (positive and negative) with good regulation using a step-down converter circuit with flyback windings. It uses only one switching regulator IC.

Performance

The circuit has an input voltage range of 15V to 40V. It has 5 outputs: 3.3V at 1.5A; +12V and −12V at 50 mA each; and +5V and −5V at 50 mA each. The 3.3V, +5V and −5V outputs are regulated with ±5% accuracy over line and load variations. The +12V and −12V outputs are regulated with ±20% accuracy. A typical application of this circuit is where the 3.3V output provides the power to the main circuit which is 3.3V logic, the ±5V outputs power the 5V logic and ±12V outputs provide the bias supply of op-amps.

The efficiency of the circuit with full load at all outputs is 75%. The ripple voltage across the 3.3V output is less than 20 mV and that across the ±12V outputs is less than 30 mV. The ripple across the ±5V is less than 10 mV.

Schematic and Parts List

Figure 1 shows the schematic of the circuit.

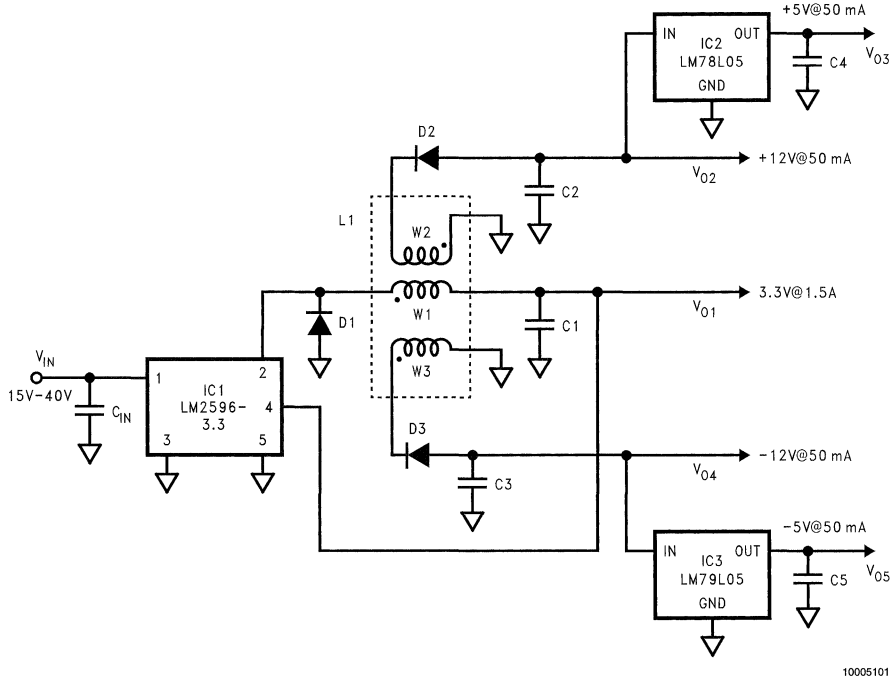


FIGURE 1. Circuit Schematic

The parts list for the circuit is:

Cin : 220 µF, 50V, Nichicon UPL1H221MPH,

C1: 270 µF, 63V, Nichicon UPL1J271MRH,

C2, C3: 47 µF, 35V, Nichicon UPL1V470MPH,

D1: MBR360,

D2, D3: 1N459,

C4, C5: 0.01 µF,

IC1: LM2596-3.3 (SIMPLE SWITCHER® Step-Down Voltage Regulator),

IC2, IC3: LM78L05, and LM79L05. (3- Terminal Regulators),

L1: Custom Inductor with three windings (W1, W2 and W3) with the following specs:

W1: 47 µH; Peak Current: 2.6A, RMS Current ≈ 2.32A

W2: Number of turns = 3.4 x Number of turns in W1; RMS

Schematic and Parts List (Continued)

Current; 113 mA

W3: Same as W2.

Circuit Operation

The circuit operates as a standard step-down (buck) switching regulator, except for the flyback windings (W2, W3). The flyback windings conduct current during the on-period of D1 and supply the 3-terminal regulators (IC2 and IC3). C2 and C3 should be of high enough value to smooth out the high ripple due to the flyback action of W2 and W3. The flyback windings supply the +12V and −12V outputs with ±20% accuracy. The 3-terminal regulators are used to provide +5V and −5V with ±5% accuracy. The LM2596 regulates the main output (3.3V) by standard step-down action.

Design

STEP 1: DESIGN OF STEP-DOWN REGULATOR FOR THE MAIN (3.3V) OUTPUT

This can be done using the *Switchers Made Simple* software by National Semiconductor. The following values (underlined) are entered into the software:

V_{IN}(min): 15V

V_{IN}(max): 40V

V_{OUT}: 3.3V

I_{OUT}:

$$I_{OUT} = I_{O1} + N\,(I_{O2} + I_{O3} + I_{O4} + I_{O5}) \quad (1)$$

1.5A is the load for the 3.3V output. I_{O1}, I_{O2}, I_{O3}, I_{O4} and I_{O5} are the load currents of outputs V_{O1}, V_{O2}, V_{O3}, V_{O4} and V_{O5} respectively. N is the turns ratio between W2 and W1 (also between W3 and W1). It is calculated using

$$N = \frac{V_{O2} + V_{FD2}}{V_{O1} + V_{FD1}} = \frac{12 + 0.7}{3.3 + 0.4} = 3.4 \quad (2)$$

In this equation V_{FD2} is the forward voltage drop of D2 and V_{FD1} is the forward voltage drop of D1.

Using (1), I_{OUT} = 1.5A + 3.4 (50 mA + 50 mA + 50 mA + 50 mA) = 2.18A

I_{OUT} = 2.18A.

The software designs the step-down regulator and gives the following values:

IC1: LM2596-3.3

C_{IN} : 220 µF, 50V, Nichicon UPL1H221MPH

C1: 270 µF, 63V, Nichicon UPL1J271MRH

D1: MBR360

L1: 47 µH.

IC I_{pk}: 2.38A.

C_{IN} and C_1 have been chosen primarily for ESR, not for voltage rating.

STEP 2: DESIGN OF L1 AND FLYBACK OUTPUTS

Design of L1

The value of inductance due to W1 is the same as the value of L1 obtained in Step 1. The number of turns in windings W2 (N_{w2}) and W3 (N_{w3}) are

$$N_{w2} = N_{w3} = N \times \text{Number of turns in W1} \quad (3)$$

= 3.4 x Number of turns in W1.

The peak current in W2 (I_{pkw2}) is

$$I_{pkw2} = \frac{I_{O2} + I_{O3}}{1 - \frac{V_{O1}}{V_{in(min)}}} = \frac{0.05+0.05}{1 - \frac{3.3}{15}} = 128\ \text{mA}. \quad (4)$$

The peak current in W3 (I_{pkw3}) is

$$I_{pkw3} = \frac{I_{O4} + I_{O5}}{1 - \frac{V_{O1}}{V_{in(min)}}} = \frac{0.05+0.05}{1 - \frac{3.3}{15}} = 128\ \text{mA}. \quad (5)$$

The RMS current of W2 (I_{rmsw2}) is

$$I_{rmsw2} \approx \sqrt{I_{pkw2}^{\,2}\left(1 - \frac{V_{O1}}{V_{in(min)}}\right)} = \sqrt{0.128^2\left(1 - \frac{3.3}{15}\right)} = 113\ \text{mA}. \quad (6)$$

The RMS current of W3 (I_{rmsw3}) is

$$I_{rmsw3} \approx \sqrt{I_{pkw3}^{\,2}\left(1 - \frac{V_{O1}}{V_{in(min)}}\right)} = \sqrt{0.128^2\left(1 - \frac{3.3}{15}\right)} = 113\ \text{mA}. \quad (7)$$

The peak current of W1 (I_{pkw1}) is

$$I_{pkw1} \approx IC\ I_{pk} + 3.4\,(I_{pkw2}\text{-}(I_{O2} + I_{O3}) + I_{pkw3}\text{-}(I_{O4}+I_{O5})) \quad (8)$$

= 2.38A + 3.4 (0.128-(0.05+0.05)+(0.05+0.05)) = 2.6A.

This value is below the $I_{CL(min)}$ specified in the LM2596 datasheet and thus is acceptable.

Since the current through W1 is continuous the RMS current is approximately equal to IC Ipk which is 2.38A.

Design (Continued)

Selection of C2 and C3

C2 and C3 should be selected to be large enough to smooth out the high ripple caused due to the flyback operation of W2 and W3. Also they should have a low enough ESR value. 47 µH, 50V aluminum electrolytic capacitors are sufficient for this design.

Selection of D2 and D3

D2 and D3 should be selected to conduct the sum of the current through the two outputs each is connected to. The DC blocking voltage rating of D2 (V_{RD2}) and D3 (V_{RD3}) are calculated using equations (9) and (10).

$$V_{RD2} = (V_{in(max)} - V_{O1})N + V_{O2} \quad (9)$$

= (40V - 3.3V) x 3.4 + 12V = 137V.

$$V_{RD3} = (V_{in(max)} - V_{O1})N + V_{O3} \quad (10)$$

= (40V - 3.3V) x 3.4 + 12V = 137V.

1N459 diodes which have a reverse voltage rating of 175V are used in this design.

STEP 3: DESIGN OF 3-TERMINAL REGULATORS

The 3-terminal linear regulators are used to regulate the auxiliary outputs with ±5% accuracy. Their design is straightforward and can be done using the datasheets for the 3-terminal regulators.

Advantages

This circuit can save both parts and cost by making use of only one step-down regulator IC, two inexpensive 3-terminal linear regulators, and a simple three-winding inductor to provide 5 outputs.

The usual solution for this design with multiple (positive and negative) outputs is a flyback converter. The design described in this application note is better than using a flyback regulator with multiple outputs because:

- It uses a much smaller output capacitor for the 3.3V output (270 µF against 2.4 mF for flyback solution with a comparable output ripple voltage).
- It uses an inductor with only three windings whereas a flyback regulator solution requires a transformer with four windings.
- The overall peak current of the inductor in this design is less than that of a flyback transformer for the same application.
- Transformer construction is simplified because the leakage inductance does not result in power loss. Because of these reasons the magnetic structure of this design costs less than that in a flyback converter design.
- The peak switch current of this design is much less than that of a similar flyback design. The disadvantages of this design compared to the flyback converter are
- The 3.3V output should be loaded to keep the inductor in continuous conduction mode. Otherwise large peak currents result in the flyback windings. In worst cases (deep into discontinuous conduction mode), the auxiliary outputs (±12V and ±5V) will not be regulated.
- When the duty cycle of the main output gets large, large peak currents result in the flyback windings and may result in loss of regulation of the auxiliary outputs in worst cases.

  In most applications the advantages far outweigh the disadvantages, as can be inferred from the comparison above.

  The IC's used in this circuit are all available in surface mount packages.

Summary

In applications where multiple output DC/DC conversion is needed, the circuit presented in this application note is an attractive solution. It is low-cost, has a low-parts count, and provides the regulation needed with good efficiency. The detailed design procedure given in this application note makes this design easy and straightforward.

Design of Isolated Converters Using Simple Switchers

National Semiconductor
Application Note 1095
Ravindra Ambatipudi

Introduction

Isolated converters are required to provide electrical isolation between two interrelated systems. Isolation between the power source and the load is required in certain applications in order to meet safety specifications such as UL1459, which necessitates 500V of isolation for telecom applications.

Isolation must be provided between all the input and output stages of the power converter Thus, isolation must be provided in the power stage and the control loop. Power stage isolation is generally provided using transformer. Isolation in the feedback/control loop is often provided through an opto-coupler (also known as opto-isolator).

Transformers are well suited for power stage isolation, since they are known for providing good dielectric barrier between two systems, with the ability to have multiple outputs. Transformers also allow stepping up or stepping down of the input voltage.

In isolated switching power supplies, opto-couplers are very widely used to provide isolation in the feedback loop. Opto-couplers do an excellent job of isolation, minimizing circuit complexity and reducing cost. One of the disadvantages of using an opto-coupler is its low bandwidth. The bandwidth of the converter is reduced by the introduction of an extra pole in the control loop gain of the converter. This is not a problem in conventional low frequency converters. However, in modern high-frequency converters, the opto-coupler imposes severe restrictions on control loop bandwidth/speed.

Another disadvantage of using opto-isolator is the large unit-to-unit variation in the current transfer ratio (CTR). CTR or the coupling efficiency is defined as the ratio of opto-isolator transistor collector current to the diode current. The loop gain is directly proportional to CTR gain. Hence, high variation in CTR imposes constraints on control loop design.

Part I. Design of Opto-Isolated Power Supply

DESIGN APPROACH

With the advent of SIMPLE SWITCHER™, and the associated "Switchers Made Simple" software (SMS4.2.1, SMS3.3), the non-isolated converter design has become very simple. However, the non-isolated converters can be modified to isolated converters very easily. The procedure for design of opto-isolated converter is as follows:

Step 1: Design the power stage components for a flyback converter using SMS4.2.1/3.3. The "Switchers Made Simple" software can be used to design the transformer, input/output capacitors, output rectifier, clamping network, etc.

Step 2: Modify the feedback/control loop by introducing a secondary side controller (such as LM3411) and an opto-isolator for feedback isolation. Also, disable the internal reference in the Simple Switcher.

DESIGN OF POWER STAGE COMPONENTS

The first step in the design process is to enter the converter specifications (shown in *Table 1*) in the input menu of the "Switchers Made Simple" software. Using these specifications, the software will design the power stage components. The following example will be based on Switchers Made Simple 4.2.1 (SMS4.2.1) and the associated LM258X flyback converters.

If the input specifications are entered as shown in *Figure 1*, SMS4.2 will design a buck converter instead of flyback. In order to design a flyback converter when the output voltage is lower than input voltage levels, it is necessary to enter initially a fictitious output voltage value which is greater than V_{IN}(min). The software will then design a flyback. Now, go to the main menu and change input requirements. Change the fictitious output voltage value to the required value. If the output voltage is greater than the minimum input voltage, these extra steps are not necessary.

TABLE 1. Isolated Power Converter Specifications (Example)

Input Voltage	10V to 30V
Output Voltage	5V
Load (maximum)	2A
Operating Temp. Range	0°C to 70°C

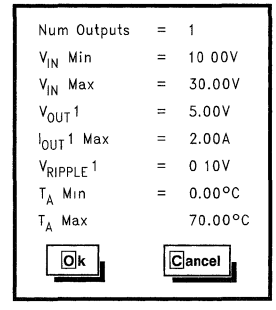


FIGURE 1. Enter the Converter Specifications in the Input Menu of SMS4.2.1

Modify the component values, input specs, etc. to suit the requirements. The software will design all the power stage components and give a list of vendors. In the example shown in *Figure 2*, the component values were entered manually to produce a surface mount design.

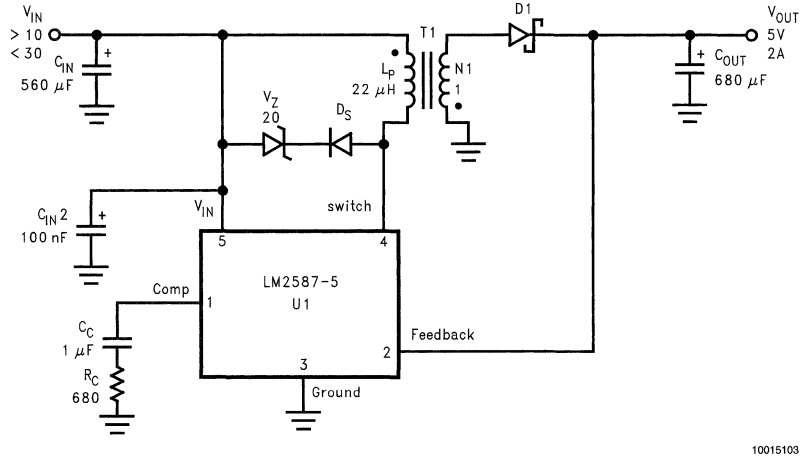
The isolation voltage of the transformer is not listed in the software. The isolation voltage is generally mentioned in the transformer manufacturer's catalog. Select a transformer taking into consideration the isolation voltage. Any of the transformers listed in the LM258X Simple Switcher data sheets meet UL1459 spec, and are suitable for telecom applications.

Part I. Design of Opto-Isolated Power Supply (Continued)

Input Parameters			Operating Values			Component Values		
V_{IN} Min	=	10.00V	Mode	=	Cont	Pri L	=	22.00 µH
V_{IN} Max	=	30.00V	Frequency	=	100.00 kHz	Leakage L	=	470.00 nH
$V_{OUT}1$	=	5.00V	Duty Cycle	=	38.68%	N1 sec/pri	=	1.00
$I_{OUT}1$ Max	=	2.00A	IC I_{PK} Max	=	5.00A	V_Z	=	20.00V
$V_{RIPPLE}1$	=	0.10V	IC I_{PK}	=	4.04A	C_{IN}	=	560.00 µF
T_A Min	=	0.00°C	L I_{PP}	=	1.56A	C_{IN} ESR	=	40.00 mΩ
T_A Max		70.00°C	Efficiency	=	72.88%	C_C	=	1.00 µF
			IC Pd	=	1.71W	R_C	=	1.00 kΩ
			IC T_J	=	106.21°C	IC Heatsnk	=	19.23°C/W
			Diode1 Pd	=	1.00W	Pri DCR	=	35.84 mΩ
			Xformer Pd	=	0.32W	$C_{OUT}1$	=	660.00 µF
			Zener Pd	=	0.49W	$C_{OUT}1$ ESR	=	24.00 mΩ
			I_{IN} Avg	=	1.37A			
			Cross Freq	=	2.40 kHz			
			Phase Marg	=	89.78 Deg			
			$V_{OUT}1$ P-P	=	96.61 mV			

10015102

FIGURE 2. Main Screen of SMS4.2.1 Summarizes the Design



10015103

FIGURE 3. Circuit Designed using SMS4.2.1

The software will also produce a schematic of the non-isolated converter as shown in *Figure 3.* This concludes the first step of the design process.

MODIFICATION OF CONTROL LOOP FOR ISOLATED DESIGN

The second step in designing an opto-isolated converter is to modify the feedback loop by using a secondary controller such as LM3411 and to use an opto-isolator for feedback isolation. To do this, connect an opto-coupler between the secondary controller and the compensation pin for feedback isolation. Power stage isolation is provided by the transformer.

Part I. Design of Opto-Isolated Power Supply (Continued)

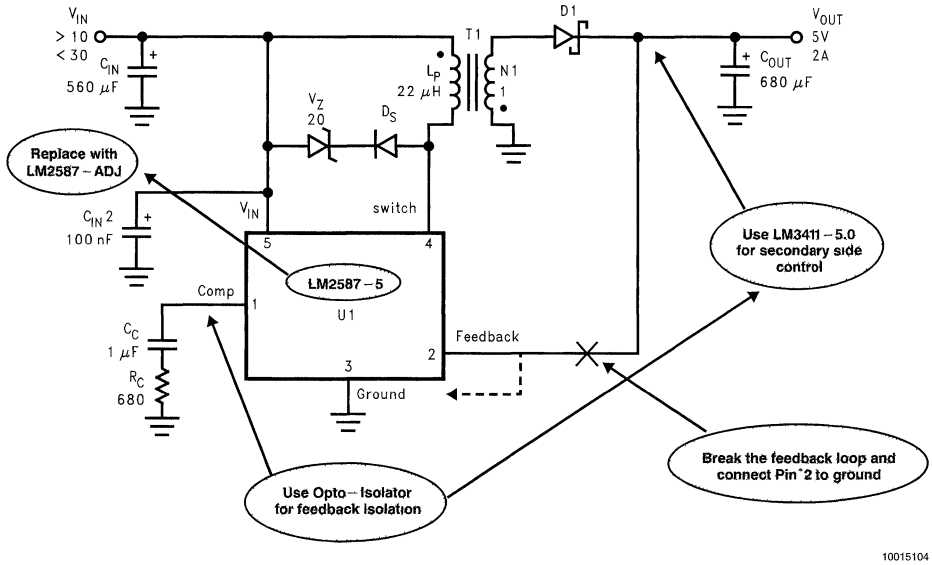


FIGURE 4. Modification of Non-Isolated Flyback to Isolated Flyback

The reference and the error amplifier internal to LM2587 have to be disabled in order to avoid interaction with the reference in secondary controller and to avoid excessive gain in the feedback loop. *Figure 5* shows the internal block diagram of LM2587. By connecting the feedback pin to ground and by connecting the opto-coupler output to the compensation pin, the error-amp is by-passed. For this reason, any voltage option of the LM2587 can be used. This completes the design of the isolated converter.

Part I. Design of Opto-Isolated Power Supply (Continued)

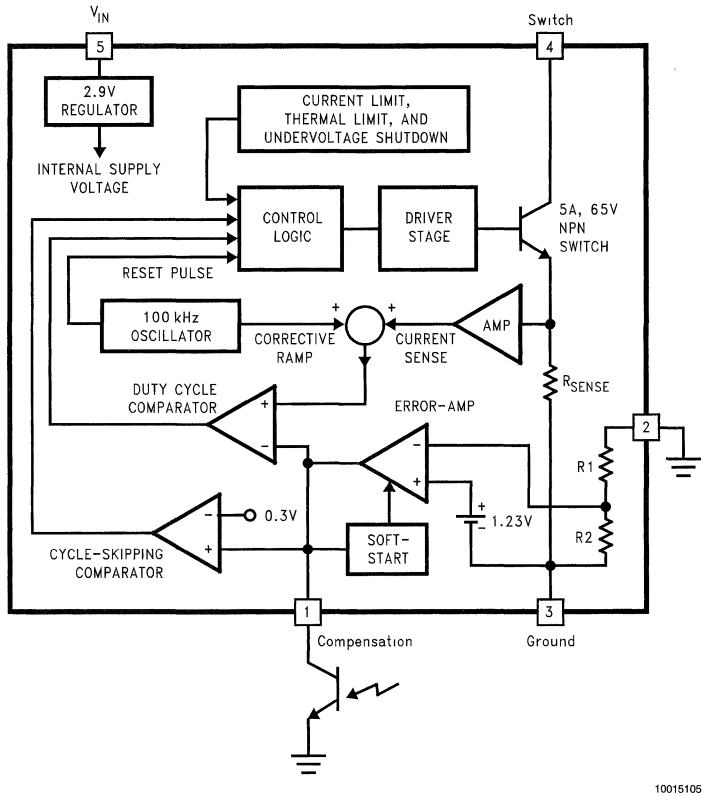


FIGURE 5. LM2587 Block Diagram; Grounding Feedback Pin Disables Error Amplifier, Opto-Coupler Delivers Feedback to Compensation Pin Instead

Figure 6 shows the circuit diagram of an LM2587 based opto-isolated flyback power supply. With the LM2587 error amplifier disabled, the feedback control now consists of LM3411-5.0 secondary side controller and the opto-isolator. Resistors R_o and R_d are required for biasing the opto-isolator. Capacitor C_s is required for soft-start.

Note: Short Circuit Protection. In LM258X switchers, the soft-start comparator and the short-circuit protection are both controlled by the feedback pin voltage. At start-up, when the output voltage is zero, the soft-start comparator is activated and the output gradually increases to the nominal value After this, the soft-start comparator gets disabled and the short-circuit protection is enabled Now if the output is shorted, the frequency will change to 25% of normal operating frequency

The short-circuit protection is activated only after the soft-start is disabled. In the isolated converter, the feedback pin is grounded The converter never comes out of soft-start mode So the short-circuit protection (which changes the frequency to 25 kHz under short circuit conditions) never gets activated Hence, an external circuit is required for short-circuit protection

Part I. Design of Opto-Isolated Power Supply (Continued)

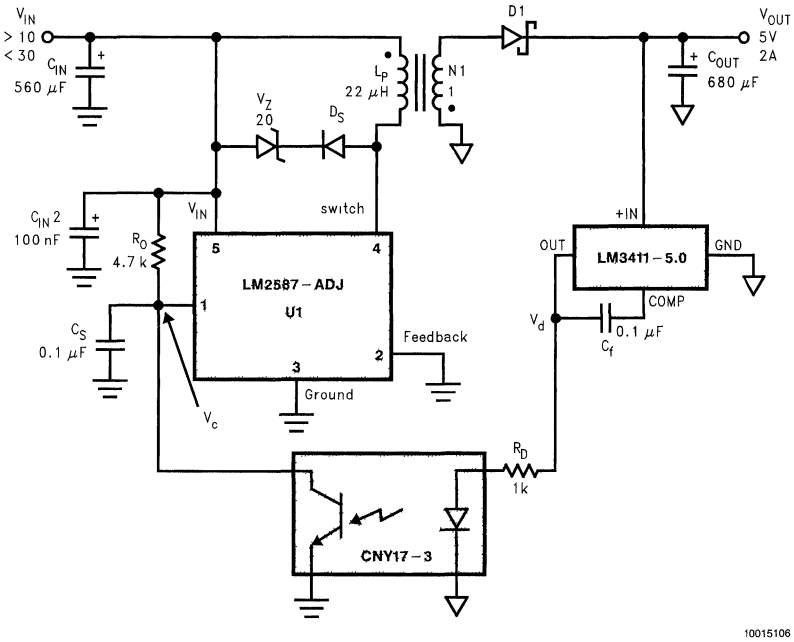


FIGURE 6. 10 Watt Opto-Isolated Flyback Converter

SELECTION OF COMPENSATION COMPONENTS

The compensation circuit design involves selection of the opto-coupler output resistance, R_o, the opto-coupler input resistance, R_d, and the feedback capacitance, C_f. The compensator transfer function is the small-signal transfer function from the output voltage, V_O to the control voltage, V_c. The transfer function, A(s) is given by:

$$A(s) = \frac{CTR \times R_o}{R_d}\left(1 + \frac{1}{sC_fR_f}\right)$$

Thus, the compensator is a two pole, one zero compensator. In the above equation, *CTR* is the opto-coupler current transfer ratio or coupling-efficiency. The power stage transfer function is a one pole, one zero (esr) compensator (in the frequency range of interest). Choose R_o and R_d such that voltage V_c is always more than 0.3V. Also, the maximum voltage on the compensation pin should be no more than 2V.

Choose C_f to place a zero to cancel the power stage pole, as shown in *Figure 7*. If the compensator is designed as shown above, the loop gain should have very good phase margin and gain margin. In *Figure 7*,

$$f_z = \frac{1}{2\pi C_f 94K}, \quad f_{p1} = \frac{1}{2\pi C_o R_L}$$

$$f_{esr} = \frac{1}{2\pi C_o R_{esr}}$$

where f_{p1} is the frequency of the power stage pole in current mode converter, f_z is the compensator zero, and f_{esr} is the esr zero. f_c is the loop cross over frequency. f_{p2} is the pole(s) created due to current mode control (located at high frequencies close to half the switching frequency).

Part I. Design of Opto-Isolated Power Supply (Continued)

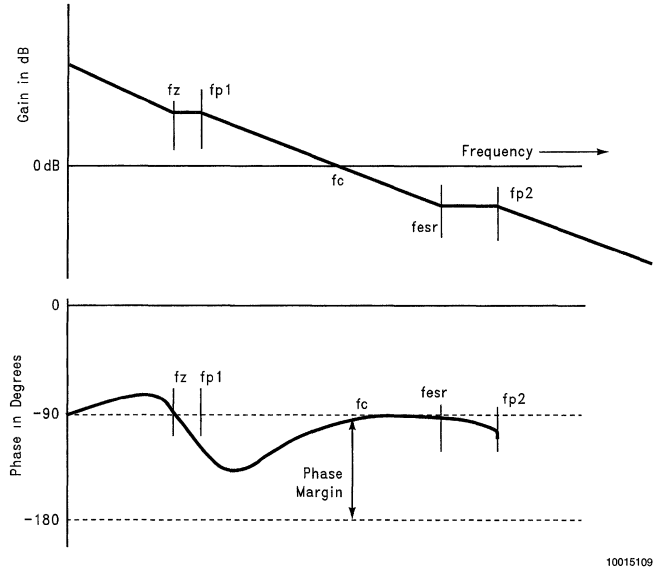


FIGURE 7. The Estimated Loop Response

The loop gain measured on the experimental converter shown in *Figure 6*, is shown in *Figure 8*. The bandwidth and phase margin are very much lower than expected.

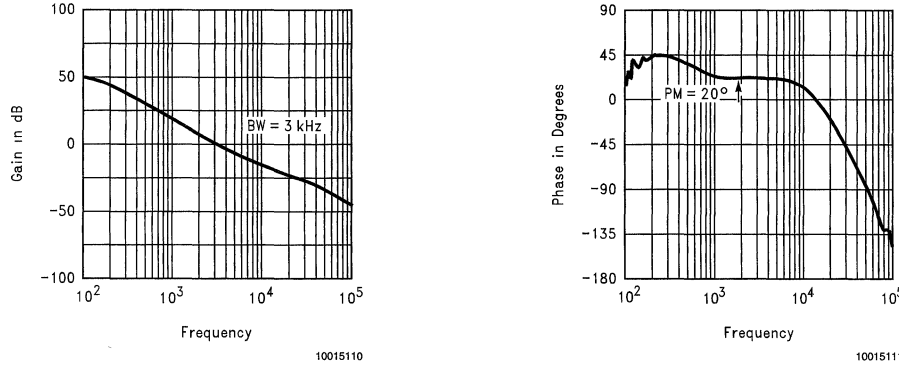


FIGURE 8. Measured Loop Gain of the Experimental Converter (Bandwidth = 3 kHz and Phase Margin = 20°)

Since the bandwidth and phase margin are very low, a transient step of 0 to 1A produces a very poor transient response, as shown in *Figure 9*. This also indicates poor stability in the control loop.

Part I. Design of Opto-Isolated Power Supply (Continued)

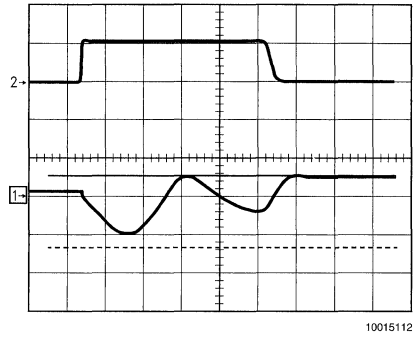


FIGURE 9. Transient Response for a Step Change in Load from 0 to 1A

Part II. Improving Transient Response of Opto-Isolated Converters

WHAT CAUSES THE DIVERGENCE BETWEEN ESTIMATED AND MEASURED RESULTS?

The converter shown in *Figure 6* uses an opto-isolator CNY17-3 for feedback isolation and LM3411 for secondary side control. Since this converter is operated at 100 kHz switching frequency, then it is desired to have its loop crossover at around 10 kHz–20 kHz for superior transient performance. However, the opto-coupler CNY17-3 used in this configuration has a −3 dB frequency of 5 kHz–10 kHz depending on the resistance R_o shown in *Figure 6*. The opto-coupler pole will introduce a phase-shift of more than 45° at around 10 kHz as shown in *Figure 10*. Because this fact was not taken into consideration while designing the compensator or loop gain, the measured phase margin and the bandwidth are lower than what was estimated.

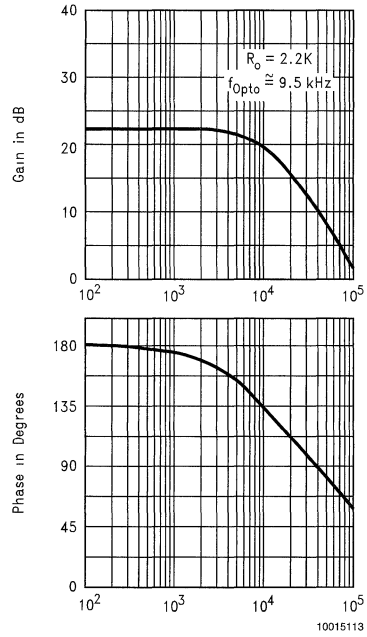


FIGURE 10. Opto-Coupler CNY17-3 Adds More Than 45° of Phase Shift at the Desired Loop Bandwidth of 10 kHz

Part II. Improving Transient Response of Opto-Isolated Converters (Continued)

WHAT LIMITS THE BANDWIDTH OF THE OPTO-COUPLER?

The severe bandwidth limitations of the opto-coupler is due entirely to the characteristics of the opto-coupler photo-transistor. When forward current is passed through the opto-coupler diode, it emits infra-red radiation. This radiant energy is transmitted through an optical coupling medium and falls on the surface of the photo-transistor. In order to make the photo-transistor base region sensitive to light, and to minimize the losses in radiant energy transfer, the photo-transistors are designed to have a very large base-collector junction area and a very thick base region. This results in a very large base capacitance, Cob. This capacitance is typically in the order of several pico farads. However, this gets effectively multiplied due to the Miller effect, resulting in a very large Miller capacitance Com. The Miller capacitance is in the order of several nana farads.

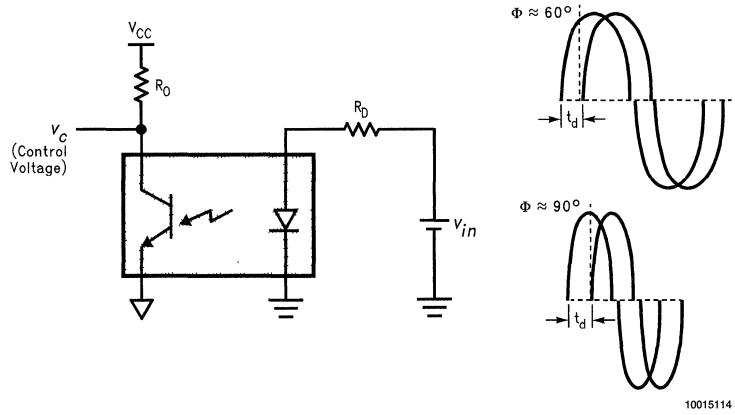


FIGURE 11. Opto-Coupler Transmission Delay Adds Phase Change at High Frequencies (as the frequency of the input sinusoid increases, the phase shift between the input and output increases linearly)

The Miller capacitance Com, coupled with the resistance R_o, will produce a pole in its transfer function. This pole should be taken into consideration while designing the compensation circuit.

It can also be observed from the opto-isolator characteristics that the phase changes very dramatically at very high frequencies. This is due to the inherent delay in transmission of radiant energy through the optical medium. If the input signal to the opto-coupler, as shown in *Figure 11*, is a sinusoid, the output signal is also a sinusoid, but phase shifted due to the delay. As the frequency of this sinusoid increases, the phase shift increases, almost linearly. The phase shift will increase linearly only if this shift is due to time delay.

HOW TO SOLVE THE OPTO-COUPLER BANDWIDTH PROBLEMS?

The control loop bandwidth can be improved in three ways:

1. The phase margin can be improved by reducing the system cross-over frequency. However, the transient performance of the converter is sacrificed.
2. Opto-isolators with better frequency characteristics (such as MOC8101) can be used. However, these opto-couplers are more expensive.
3. The opto-isolator pole can be compensated by introducing an additional zero in the control loop. This requires proper prediction of opto-coupler pole.

ESTIMATION OF THE OPTO-COUPLER POLE

The opto-coupler pole can be estimated in a number of ways. One method is to characterize the pole by actual bench measurements. *Figure 12* shows the bench measurement setup for characterization of an opto-coupler using a network analyzer. A signal is injected at the opto-coupler input and frequency of this signal is swept over the frequency range of interest. The input signal is measured with probe A and the output signal with probe B. By taking the ratio of the input signal to the output signal, the frequency characteristics are obtained.

Part II. Improving Transient Response of Opto-Isolated Converters (Continued)

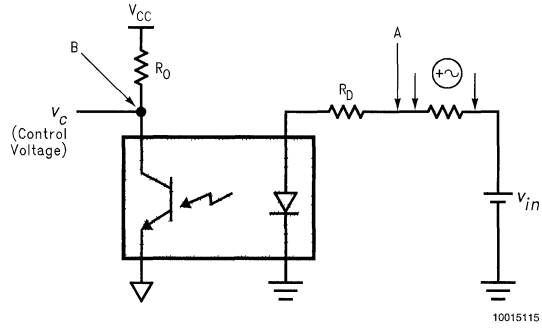


FIGURE 12. Bench Measurement Setup for Frequency Characterization of Opto-Coupler Pole Using a Network Analyzer

Figure 13 shows the typical performance curve obtained by actual measurements for the opto-coupler CNY17-3. In this figure, the opto-coupler bandwidth (pole) has been plotted versus the resistance R_o. The opto-coupler pole can be very easily predicted from this curve As an example, let us predict the pole for CNY17-3 when the resistance, $R_o = 5\ k\Omega$. Draw a line parallel to Y-axis at $R_o = 5\ k\Omega$. From the point of intersection on the curve, read the corresponding value on Y-axis. The opto-coupler pole would be at 4 kHz.

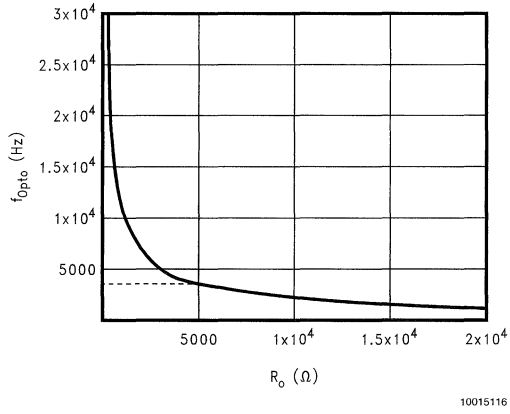


FIGURE 13. Opto-Coupler CNY17-3 Bandwidth versus Resistance R_o

From the results of Part I, it is very obvious that the opto-isolator pole imposes severe restrictions on the control loop bandwidth. This pole can be compensated in two ways.

- If the base connection is available, then by connecting a large resistor between the base and emitter of the opto-coupler photo-transistor, the bandwidth can be improved. However, the opto-coupler gain will reduce by doing so.
- The bandwidth can also be improved by introducing an additional zero in the compensation circuit.

IMPLEMENTATION OF THE OPTO-COUPLER POLE COMPENSATION

For the circuit shown in *Figure 6*, the opto-coupler pole can be estimated as discussed in previous sections. However, the soft-start capacitor appears in parallel with opto-coupler device capacitances and influences the position of the opto-coupler pole. The additional zero required to compensate the opto-coupler pole can be obtained by connecting a capacitor in parallel with R_{d1} as shown in *Figure 14* In the process, this creates an additional pole due to R_{d2} and C_d. To obtain sufficient gain margin and attenuation of high frequency switching noise, this pole can be placed at a high frequency above the cross-over frequency.

Part II. Improving Transient Response of Opto-Isolated Converters (Continued)

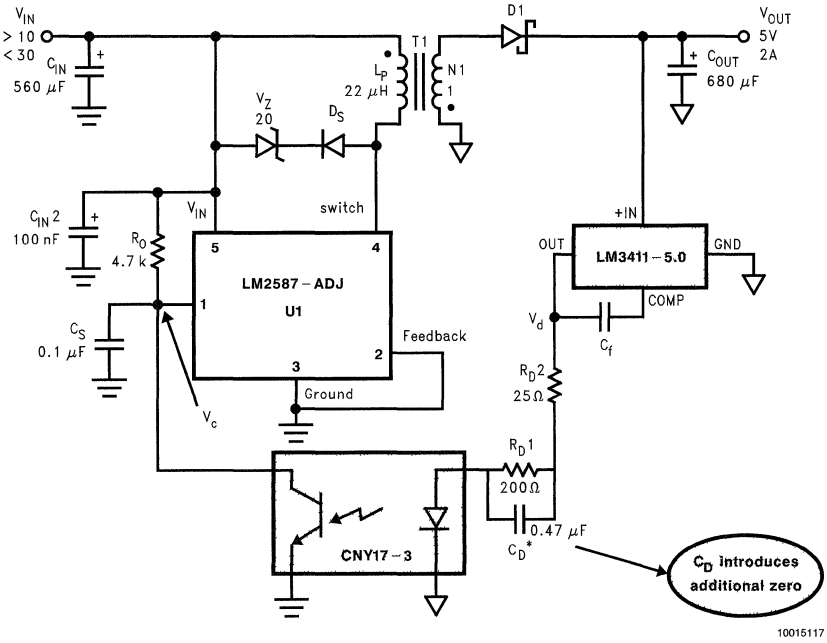


FIGURE 14. Compensating the Opto-Coupler Pole to Improve the Bandwidth Limitations

The modified compensator transfer function is:

$$A(s) = \frac{CTR \times R_o}{R_{d1} + R_{d2}} \left(\frac{sC_cR_f + 1}{sC_cR_f}\right)\left(\frac{sC_dR_{d1} + 1}{sC_dR_{d2} + 1}\right) \text{ (assuming } R_{d2} >> R_{d1})$$

where:

CTR = Opto-coupler current transfer ratio or coupling efficiency

R_f = feedback resistor internal to LM3411 (92k for LM3411-5.0)

C_c = Compensation capacitor

An additional zero can also be obtained by connecting a resistor in series with capacitor C_s, the additional zero required to compensate the opto-coupler pole can be placed at a frequency equal to f_z.

$$f_z = \frac{1}{2\pi R_o C_s}$$

(Assuming C_s is very much larger than the opto-coupler Miller capacitance).

Notice that the compensator transfer function is directly dependent on the opto-coupler CTR, which varies from unit-to-unit, so it is important to take this factor into consideration. This means that an opto-coupler with low CTR variation and guaranteed limits should be used.

Figure 15 shows the loop gain with modified compensator. Significant improvement in bandwidth and phase margin are observed. The loop gain is as expected and shows excellent stability. As expected, the transient response is also improved, as shown in *Figure 16*.

Part II. Improving Transient Response of Opto-Isolated Converters (Continued)

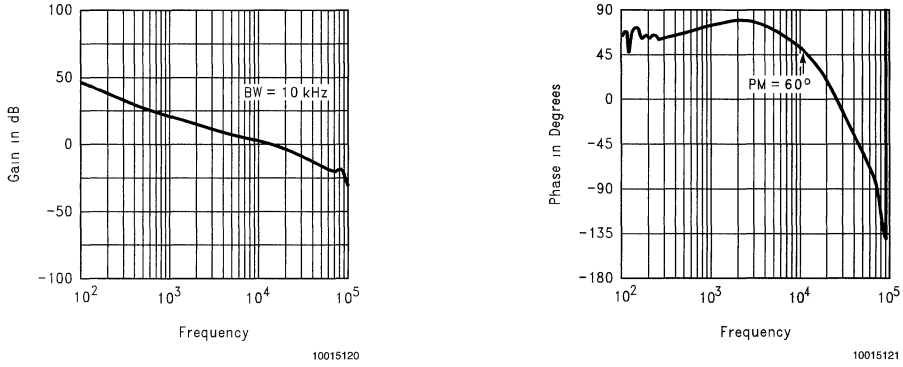


FIGURE 15. Significant Improvement in Bandwidth and Phase Margin is Observed with Opto-Coupler Pole Compensation (Bandwidth = 10 kHz and Phase Margin = 60°)

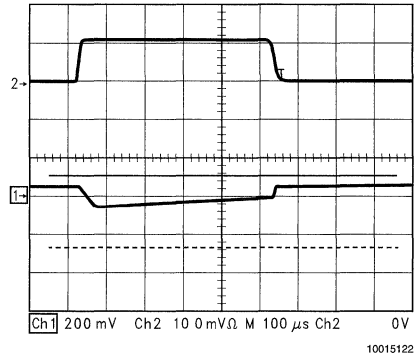


FIGURE 16. Transient Response with Opto-Coupler Pole Compensation (0 to 1A Step-Change in Load)

Simple Regulator Provides ±12V from 5V Source

National Semiconductor
Application Note 1118
Michael Shrivathsan

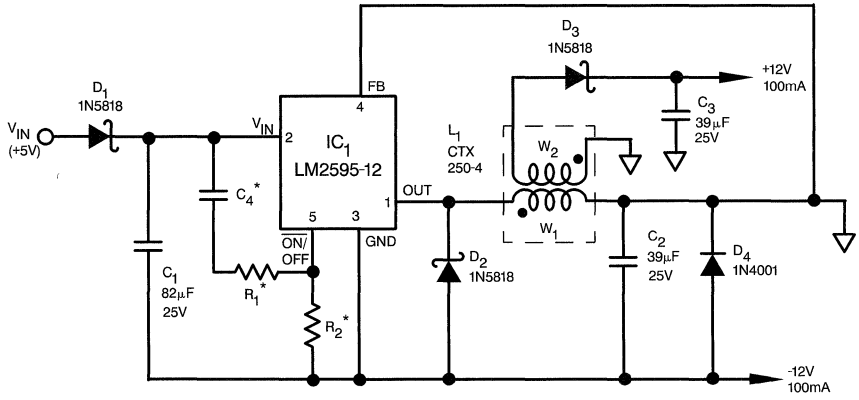
Many systems require a ±12V power supply. Typical examples include analog circuits or RS-232 driver power supplies. The ±12V typically needs to be generated from a 5V system bus. The solutions normally used involve a multiple secondary transformer or multiple switching regulators. These solutions can be complicated, may require custom transformer design and may have poor efficiency and poor regulation. The circuit shown in *Figure 1* is simple, uses only one switching regulator IC, uses a small number of components, and provides good regulation at a high efficiency. Additionally, all the components used in this circuit are off-the-shelf components.

The circuit in *Figure 1* uses an LM2595-12 (buck SIMPLE SWITCHER™) based switching regulator to generate both the +12V and the −12V outputs from 5V input. The LM2595 is configured as an inverting buck-boost converter to obtain the negative output. The positive output is generated using an additional winding in the off-the-self inductor (CTX250-4 from *Coiltronics*) used in this circuit. Only one additional diode (D_3) and a capacitor (C_3) are needed to generate the positive output.

During the on-time of the switching cycle, the inductor (L_1) is charged by applying the supply voltage across the inductor. During this time the output capacitors (C_2 and C_3) are supplying the load. During the off-time of the switching cycle, the energy stored in the inductor is transferred to the output capacitors and the loads. The LM2595 is regulated off of the negative output. The positive output is regulated because of the coupling between the windings of the inductor. The diode D_4 prevents the −12V output from the going positive above a diode drop during the turn-on of the circuit. The diode D_1 is used for providing isolation between the output and the input. LM2595 operates at a switching frequency of 150 kHz resulting in small inductor and capacitor sizes.

This circuit was built in the lab using the components shown in *Figure 1*. The −12V output varied between −11.99V and −11.97V under a load variation between 50 mA and 100 mA and a line variation between 4.5V and 5.5V. The +12V output varied between 11.15V and 11.45V under the same conditions. The +12V output is lower than the −12V output because of the voltage divider effect of the leakage inductance and a mismatch in the forward voltage drops of D_2 and D_3. The efficiency of this circuit varied between 76% and 83% over the line and load variation. The ripple voltage on the +12V and the −12V outputs is less than 1%. A majority of this ripple voltage is due to the ESR (Equivalent Series Resistance) of the output capacitors C_2 and C_3. The capacitors used in this circuit have an ESR of 0.65Ω. A smaller ripple voltage can be obtained by using lower ESR, higher value output capacitors.

If higher load currents are desired, the LM2596 SIMPLE SWITCHER should be used in the place of LM2595. This will provide up to 275 mA of load current each from the +12V and −12V outputs. Other output voltages are also achievable using LM2596-ADJ versions.



* Components needed if the 5V supply is current-limited during start-up
C4 0.1µF, ceramic
R1, R2 47kΩ, 1/4W, 10%

10099201

FIGURE 1.

Using Dynamic Voltage Positioning to Reduce the Number of Output Capacitors in Microprocessor Power Supplies

National Semiconductor
Application Note 1145
Dongbing Zhang
Steven Hunt

Abstract

The relatively large steady-state window and the relatively small transient window for the core voltage of a modern advanced microprocessor make attractive implementation of the dynamic voltage positioning technique. By employing that technique, significant cost savings can be realized due to the reduced number of output bulk capacitors. Careful consideration of all sources of error is necessary for generating a sound design.

Example I

In this example, a net savings of $0.44 is realized through the implementation of the dynamic voltage positioning (DVP below) technique.

Assume a microprocessor requires a maximal 18A. The allowed core voltage steady-state window is ±100mV. Suppose a synchronous buck converter is used and the controller's DAC tolerance is ±30mV. Also assume the output voltage ripple is set to 17mV peak-to-peak.

To accommodate the worst case load transient (i.e. the processor current changes between 0A to 18A within a few clock cycles), 14 Sanyo 6MV1500GX aluminium capacitors are needed at the output.

Or, if a 3mΩ ±5% IRC power resistor is put in series with the output inductor, DVP can be used and the number of output caps can be reduced to 10. Two additional signal level resistors (1.00KΩ and 75.0KΩ, 1%) are necessary to raise the initial output voltage by 26mV.

The cost of the power resistor is approximately $0.20, and the cost of the capacitors is about $0.16 each. So the total savings realized by implementing DVP is $0.44.

The drawback is an additional maximum power loss of about 1W in the power resistor. A side benefit is the same power resistor can be used to provide an accurate current limit when a more serious over-current protection mechanism than high-side MOSFET r_{DS_ON} sensing is desired.

Example II

In this example, a net savings of $0.48 is realized through the implementation of the DVP technique.

Assume the same processor as in Example I is considered. If a PCB etch resistor is used instead of the discrete power resistor, a number of things are going to change. First, the total tolerance of the resistance will be increased to about 20% including the effect of temperature. Second, the resistor itself is free. So the amount of savings in output caps is the net savings.

By calculation, the optimal resistance of the etch resistor is 2.2mΩ. The initial output voltage should be raised by 16mV. This can be done by using two signal-level resistors, 100Ω and 12.4KΩ, 1%.

The number of output caps is now 11. So the savings is $0.48.

The maximum power loss due to the etch resistor is 0.71W.

Introduction

For modern high-speed microprocessors such as those in the Intel Pentium® pro and Pentium® II families, there are strict load transient response requirements on the processor core voltage. Two operating windows are defined for the MPU core voltage, i.e., the transient window (or so-called AC window) and the steady-state window (or so-called DC window). The AC window is greater than or equal to the DC window. For example, the Klamath processor (Pentium® II family) requires, at the VRM connector, a DC window of 100mV, −60mV and an AC window of ±140mV for a nominal core voltage of 2.8V. During steady-state, the core voltage is allowed to stay outside of the DC window for a short while but should never be outside of the AC window. Both windows are for instantaneous voltages, i.e. set point tolerance, ripple and noise etc. are included.

For a typical core power supply controller, the initial output voltage tolerance plus ripple is much smaller than the DC window. It therefore may be beneficial for the output voltage to be positioned at different levels within the DC window in response to different load current levels. The idea is by dynamically positioning the core voltage level according to the load current, extra window margin for the load transient response can be created.

As an illustration, *Figure 1* shows two load transient response waveforms, one with DVP, the other without. Factors such as initial output voltage tolerance (typically the DAC tolerance in the case of a digitally programmable controller), ripple voltage, etc. are excluded. In the figure, the lines labeled "AC" are the transient window limits, the lines labeled "DC" are the steady state window limits, and the line marked "V_N" is the nominal core voltage.

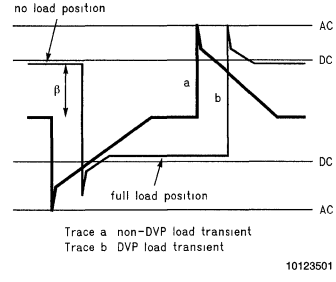


FIGURE 1. DVP and non-DVP Output Voltage Transients Caused by Load Transients

Introduction (Continued)

For a non-DVP converter, steady-state core voltage doesn't vary with load current. Therefore, after a transient in either direction, the core voltage returns to V_N. See trace "a". For a DVP converter, the core voltage is a function of the load current. See trace "b". At no load, the core voltage is close to the upper limit of the DC window whereas at full load it is close to the lower limit of the DC window. This allows extra headroom for load transients in both directions. In *Figure 1*, β is the amount of extra transient headroom DVP creates. It is also the amount by which the nominal output voltage should be raised.

Implementation

As mentioned above, to implement DVP, the steady-state output voltage should be raised slightly at no load and it should droop as the load current increases. This characteristic can be realized by using a voltage divider in the feedback loop and adding an external droop resistor after the inductor. See *Figure 2*. In the figure, a synchronous buck PWM controller such as National Semiconductor's LM2635/6/7/8 is used. Now, instead of regulating point "a" as is done in non-DVP converters, point "c" is regulated. The voltage divider between points "b", "c" and ground raises the voltage at point "b" so that at no load the output voltage is slightly higher than nominal. (Notice at no load, points "b" and "a" are at the same potential). The voltage across the droop resistor is proportional to the load current during steady-state. Therefore, the heavier the load current is, the lower the output voltage will be. The corresponding voltage vs. output current characteristic is shown in *Figure 3*.

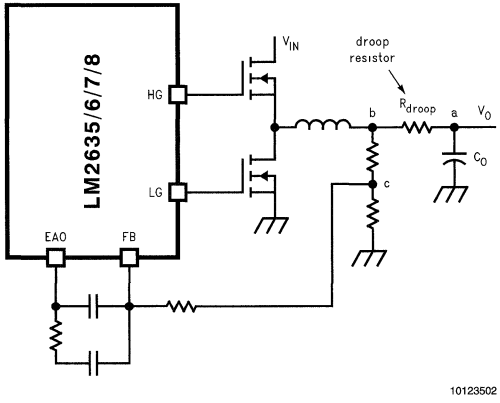


FIGURE 2. Implementing DVP Using a Droop Resistor and National's LM2635/6/7/8 Controllers

The resistor divider is not necessary if the internal reference voltage (typically the DAC output in the case of a digitally programmable controller) of the switching controller IC has been prebiased for DVP.

The droop resistor must be a power resistor since it is in the power path. It can be a discrete current sense resistor or it can be a PCB etch resistor. The typical resistance value is a few milli-ohms.

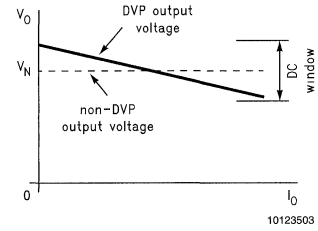


FIGURE 3. DVP Converter Output Characteristics

The benefits of a discrete resistor are better tolerance and an ultra-low temperature coefficient (typically ±20ppm/°C). It also creates less thermal stress on the PCB. The disadvantages are component cost and availability, and very limited choice of resistance values.

The benefits of a PCB etch resistor are no cost and a flexible resistance value. The disadvantages are worse tolerance, high temperature coefficient (about 4000ppm/°C) and more thermal stress on the PCB. Which kind of droop resistor creates more savings depends on load current, DC and AC window sizes, initial output voltage tolerance, etc.

The Equations

To make a realistic comparison between a non-DVP converter and a DVP converter and to provide a design tool for DVP implementation, factors such as the DAC tolerance (assuming digitally programmable controller), output voltage ripple and droop resistor tolerance and temperature coefficient must be considered.

Figure 4 shows the distribution of the steady-state voltage of a non-DVP converter, assuming the load regulation is perfect. Note the load current is irrelevant to the distribution.

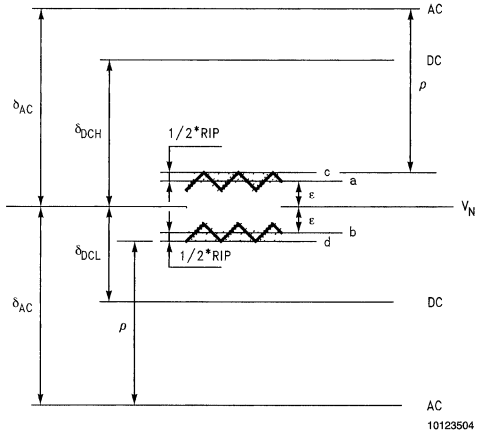


FIGURE 4. Non-DVP Steady-State Output Voltage Distribution and Transient Margins

The gray band between lines "a" and "b" corresponds to the total DAC tolerance which is 2ε. When voltage ripple is considered, the steady-state tolerance band must be widened to the one confined by lines "c" and "d", i.e. 2ε+RIP. RIP is the peak-to-peak ripple voltage. The worst case full-load-to-no-load transient would occur when the steady-state voltage at full load is at line "c" because this is the case having the least transient margin (ρ in the figure). The corresponding transient margin is:

$$\rho = \delta_{AC} - \left(\frac{1}{2}\,RIP + \varepsilon\right), \qquad (1)$$

where δ_{AC} is half the size of the AC window. Assuming the AC window is symmetrical around the nominal voltage V_N, the same formula applies to load transients in the opposite direction (no-load-to-full-load).

In the case of DVP, the position of the tolerance band becomes a function of load current. It is higher at light load and lower at heavy load. See *Figure 5*.

The maximum voltage across the droop resistor (V_{droop}) determines by how much the output voltage should be raised at no load. If the error introduced by the droop resistor is ignored (as in the case of *Figure 5*), the center of the output voltage tolerance band should be half of V_{droop} above V_N at no load, and half of V_{droop} below V_N at full load, as shown in *Figure 5*. The extra transient margin created is thus half of V_{droop}.

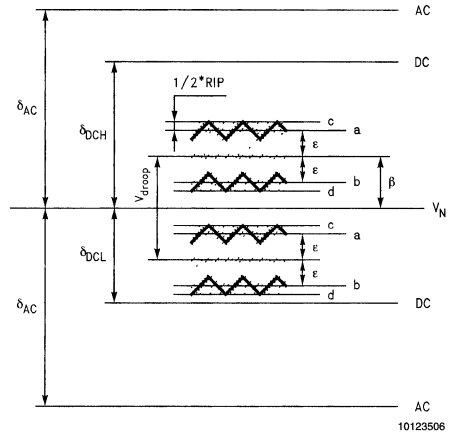


FIGURE 5. DVP Steady-State Output Voltage Distribution with Zero-Tolerance Droop Resistor

However, there is inevitably a tolerance and temperature coefficient associated with the droop resistor. Assume the tolerance and variation due to the temperature change of the droop resistor is ±λ. See *Figure 6* below.

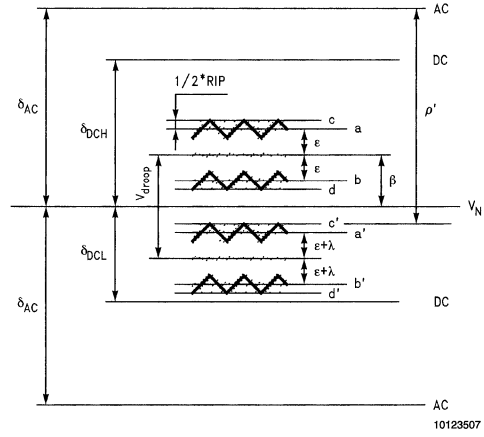


FIGURE 6. DVP Steady-State Output Voltage Distribution with Finite-Tolerance Droop Resistor

This error will make the upper boundary of the tolerance band at full load (line "c'") 1λ closer to V_N than the lower boundary of the tolerance band at no load (line "d"). To keep the two boundaries (lines "c'" and "d") equidistant from V_N so

The Equations (Continued)

that transients in both directions have the same margin, the no-load offset β should be adjusted to a value smaller than half of V_{droop}.

The appropriate offset of the no-load tolerance band is:

$$\beta = \frac{1}{2} V_{droop}(1 - \Sigma), \tag{2}$$

where V_{droop} is the maximum droop voltage, i.e. the droop voltage at full load, and Σ is droop resistor tolerance ($\lambda = V_{droop} \times \Sigma$).

The new transient margin ρ' is now the distance between the line "c'" and the upper boundary of the AC window or that between the line "d" and the lower boundary of the AC window. The formula to calculate the margin is:

$$\rho' = \rho + \beta \tag{3}$$

,

so the difference between the new and old transient margins is the offset β.

It is necessary to check whether the line "d'" is still above the lower boundary of the DC window. The reason line "d'" is more important is that it is farther away from V_N than line "c" and in some cases the lower half of the DC window is smaller than the upper half. The criterion is :

$$V_{droop} \leq \frac{2\delta_{DCL} - RIP - 2\varepsilon}{1 + 3\Sigma}, \tag{4}$$

where δ_{DCL} is the size of the lower half of the DC window.

The percentage savings in the amount of output capacitors is:

$$SVGS\% = \frac{\beta}{\rho'}. \tag{5}$$

The cost savings in output capacitors can be determined by the following equation:

$$\Delta\$ = \left(\frac{1}{\rho} - \frac{1}{\rho'}\right) \bullet ESR \bullet PRICE \bullet I_{CORE}, \tag{6}$$

where ESR is the equivalent series resistance of each output capacitor, PRICE is the unit price of a capacitor and I_{CORE} is the maximum load current.

The actual savings may be slightly more or less than the result of *Equation (6)* because the number of capacitors is always an integer.

Once the type of output capacitors is known, the number of them can be determined by the following criterion:

$$N \geq \frac{ESR \bullet I_{CORE}}{m}, \tag{7}$$

where m is transient margin, i.e. ρ or ρ'.

Example I Revisited

Assumptions:

RIP = 17mV, ε = 30mV,

δ_{AC} = 100mV, $\delta_{DCH} = \delta_{DCL}$ = 70mV,

R_{droop} = 3mΩ±5%, I_{CORE} = 18A.

Thus,

V_{droop} = 3mΩ x 18A = 54mV.

Then by *Equation (1)*, the non-DVP load transient margin is:

ρ = 100mV – (½x17mV+30mV) = 61.5mV.

The DAC offset in this case will be, by *Equation (2)*:

β = 0.5 x 54mV x (1-5%) = 26mV.

By *Equation (3)*, the DVP transient margin is:

ρ' = 61.5mV + 26mV = 87mV.

Check if the tolerance band is out of the DC window by using *Equation (4)*:

(2 x 70mV–17mV–2 x 30mV) ÷ (1+3 x 5%) = 54.8mV.

This value is greater than the 54mV actual maximum droop voltage so the condition is satisfied.

Suppose the output capacitors are from the Sanyo MV-GX series, the unit price is $0.16, and the ESR of each capacitor is 47mΩ, then the cost savings in output capacitors is:

Δ$ = (1/61.5mV–1/87mV) x 47mΩ x $0.16 x 18A = $0.64.

After subtracting the cost of the droop resistor, the net savings is $0.44.

Example II Revisited

Since the droop resistance value is now flexible, it is necessary to find out the optimal value first. The larger the droop voltage, the larger the offset β and the larger the extra margin will be. The largest allowable droop voltage can be determined by *Equation (4)*:

V_{droop} = (2 x 70mV–17mV–2 x 30mV) ÷ (1+3 x 20%)
= 39.4mV.

Therefore, the optimal droop resistance is:

$R_{droop} = V_{droop} \div I_{CORE}$ = 39.4mV ÷ 18A = 2.2mΩ.

The initial offset β is, by *Equation (2)*:

β = 0.5 x 39.4mV x (1-20%) = 16mV.

The new transient margin is, by *Equation (3)*:

ρ' = ρ+β = 61.5mV+16mV = 77mV.

Therefore, by *Equation (5)*, the savings in output caps is:

Δ$ = (1/61.5mV–1/77mV) x 47mΩ x $0.16 x 18A = $0.45.

To calculate the actual savings, calculate the number of caps needed in the non-DVP case:

N1 = 47mΩ x 18A ÷ 61.5mV ≅ 14.

And calculate the number of caps needed in the DVP case:

N2 = 47mΩ x 18A ÷ 77mV ≅ 11.

So the difference is 3 caps, and thus $0.48.

Comments

1. As discrete resistors go lower in resistance value, it is harder and harder for resistor vendors to make them very accurate. IRC has resistance values down to 3mΩ. Sometimes paralleling two discrete resistors is the only solution.
2. When designing an on-board supply, the DC window can be relaxed to slightly larger than that written in the VRM specifications. Refer to the processor specifications instead. Typically a relaxation of ±10mV is possible.
3. When switching from a non-DVP design to a DVP design, a slightly larger inductor might be necessary to keep the output ripple voltage to same.

Comments (Continued)

4. Normally the top and bottom layers of a PCB are plated and copper thickness on those two layers is inaccurate. Try to use an inner layer to place an etch resistor.
5. As a good rule, use 20mil/A current density for 1 oz. copper when designing an etch resistor.
6. A DVP design tool in the form of a Microsoft Excel spreadsheet is available from the authors to automate the design process. The tool is good for designing DVP for National Semiconductor's LM2635/6/7/8 family of products.
7. To realize the deadbeat type of response similar to trace "b" in *Figure 1* during a fast load transient, the converter's loop characteristic needs to be fine tuned.

Designing a Multi-Phase Asynchronous Buck Regulator Using the LM2639

National Semiconductor
Application Note 1146
Dongbing Zhang

Overview

The LM2639 provides a unique solution to high current, low voltage DC/DC power supplies such as those for fast microprocessors. The two major features of the LM2639-based solutions are multiphase and ultra-high switching frequency, which result in the following three advantages when compared to a conventional buck and a high frequency single-phase buck.

The first advantage is thermal. Since the load current is evenly shared among multiple channels, the heat generated is greatly reduced for each channel due to the fact that power loss is proportional to square of current. Surface mount MOSFETs and diodes (such as DPAK and D2PAK packages) can be used to handle a fairly high load current such as 20A or even higher. Physical size of the output inductor shrink significantly because of a similar reason.

The second advantage is reduced input and output ripple current. Since the channels are phase shifted, the AC components of the currents tend to cancel. This eases the burden of ripple RMS current requirement on input capacitors. Output voltage ripple is also reduced.

The third advantage, and probably the most prominent for microprocessors is, the solution enables the use of ceramic capacitors for output filtering. This is because in such an application, the output inductance is usually the gating factor in slowing the supply current during a fast load transient. Duty cycle usually saturates. However, a LM2639-based solution not only can use low output inductance values (because of high switching frequency), but the inductors are like paralleled during a load transient event (because of multi-phase operation). That makes the solution not only faster than a conventional buck, but also faster than a single-phase high switching-frequency buck. Because of that, small surface mount multi-layer ceramic capacitors can be used as output capacitors. This advantage is especially attractive to low voltage, high current processors such as K7 and Pentium III, because countless number of bulky low-ESR aluminium capacitors can be completely replaced by small, surface-mount ceramic capacitors.

The LM2639 helps accurate load current sharing by guaranteeing a 1% duty cycle match among the channels. Two, three or four phase operation can be configured. It can also be configured to use internal clock or to use an external clock signal.

The LM2639 also features a precision 5-bit DAC whose output voltages comply with Intel's VRM specifications.

Current limit is realized through a current sense resistor at the input end.

Soft Start

The LM2639 has an initial digital soft start function. Upon VCC5V pin exceeding power-on-reset level (about 4.2V), duty cycle will grow from 0 to maximum value gradually, in a manner of 16 steps (see *Figure 1*). It takes about 12,800 clock cycles to go through all 16 steps. For a typical clock frequency of 8MHz it takes 1.6ms to finish all 16 steps, 100µs each step.

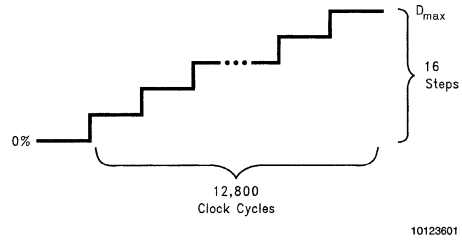


FIGURE 1. Digital Soft Start

Clock Signal

The clock signal can be generated internally or it can be synchronized to an external source. The internal clock can be set to run at 40kHz to 10MHz by adjusting the value of the resistor connecting from R_{ref} pin to the ground. To use the internal clock, connect the Clksel and Extclk pins to V_{CC} 5V pin. To use external clock, connect Clksel pin to ground and the Extclk pin to the clock source. To generate an 8MHz internal clock, use a 8.06kΩ resistor at the R_{ref} pin. To lower the internal clock frequency, increase the resistor value.

Three-Phase Operation

The regulator can be configured to operate in 3-phase mode instead of 4-phase mode. The phase associated with DRV3 will be disabled, and the rest three phases will be 120° apart. To enable 3-phase mode, pull the Divsel to logic high. The 3-phase mode can be used for relatively low current applications to save cost.

Two-phase operation is the same as 4-phase operation - just use any two channels that are 180° out of phase.

Loop Compensation

The purpose of loop compensation is to tailor the dynamic characteristics of the regulator so that it meets both the steady-state and transient response requirements. The error amplifier inside the LM2639 is of transconductance type. The typical compensation network is a lag compensation and is formed by a capacitor and a resistor in series (C_c and R_c in *Figure 2*). The function of the lag compensation network is two folds. One is to enhance the DC gain so that the regulator will have a highly precise output voltage in the steady

Loop Compensation (Continued)

state over all line and load ranges. The other is to boost the total gain of the loop transfer function so that the regulator will have a higher control bandwidth and gain.

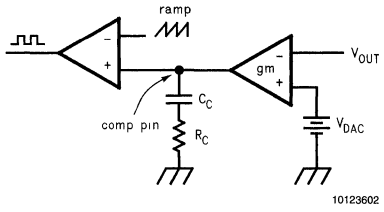


FIGURE 2. Loop Compensation

As an example, let us go through the loop compensation process of the typical application circuit. The loop can be broken into two parts. That is, control-to-output transfer function (also known as power stage transfer function), and output-to-control transfer function. The small signal model for the control-to-output portion of the circuitry is illustrated in *Figure 3*.

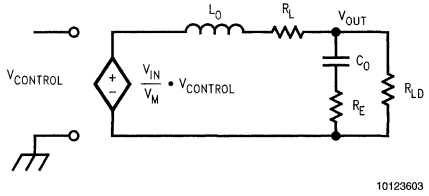


FIGURE 3. Small Signal Model of Power Stage

In the model, L_o is the equivalent output conductor, which is output inductance of each channel by number of channels. R_L is the MOSFET R_{dson} divided by number of channels is output capacitance and R_o is the total combined ESR. R_{LD} is load resistance. $V_{control}$ is the voltage at COMP pin. V_m is the peak-to-peak value of the PWM ramp appearing at the PWM comparator, which is 2V in the case of LM2639.

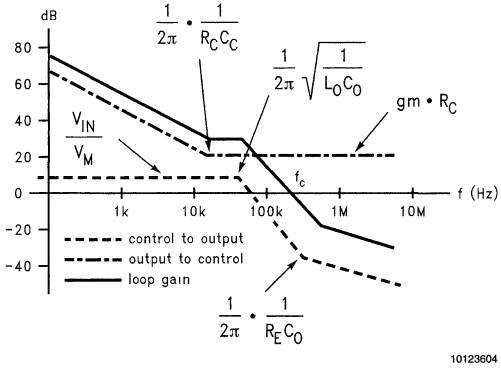


FIGURE 4. Bode Plots of Transfer Functions

It is easy to see that the DC gain of the control-to-output transfer function is:

$$G_{dc} = \frac{V_{IN}}{V_M}$$

In our case, it is 5V ÷ 2V = 2.5 or 8dB. A double pole occurs at:

$$f_{dp} = \frac{1}{2\pi}\sqrt{\frac{1}{L_O C_O}}$$

In our case, L_o = 300nH ÷ 4 = 75nH, and C_o = 22µF x 12 = 264µF. So the double pole is at 35kHz.

The next significant parameter in the power stage transfer function is the ESR zero:

$$f_{ESR} = \frac{1}{2\pi} X \frac{1}{R_E \cdot C_O}$$

In our case, R_E = 15mΩ ÷ 12 = 1.3mΩ. So ESR zero is at 464kHz.

Refer to *Figure 4* for asymptotic bode plot of the power stage (broken line).

The lag compensation has one pole-zero pair. The pole occurs at zero frequency. The location of the zero is determined by:

$$f_{zero} = \frac{1}{2\pi} X \frac{1}{R_C \cdot C_C}$$

In our case, it is important to place the zero before the power stage double pole to avoid stability issue. The trade-off between a higher zero frequency and a lower one is the mid-frequency gain and the phase margin. In our specific case, the higher the zero frequency the less the phase margin but the higher the mid-frequency gain. This, in time domain, will translate into a faster load transient recovery speed. If we choose 17kHz, and a compensation gain of 20dB beyond the zero frequency, the output-to-control and the final loop transfer functions will be like those shown in *Figure 4*.

The cut off frequency (f_c in *Figure 4*) is where the loop transfer function has a 0dB gain and is usually referred to as control bandwidth. In this case, we have a control bandwidth of 200kHz. In a LM2639-based solution, the control bandwidth is pretty important in load transient response.

Loop Compensation (Continued)

To calculate the compensation values, use the following equations:

$$R_C = \frac{G_{comp}}{gm}$$

and

$$C_C = \frac{1}{2\pi \bullet f_{zero}} \times \frac{gm}{G_{comp}}$$

where G_{comp} is the compensation gain beyond the compensation zero frequency. In our case, G_{comp} is 20dB or 10, gm is 1.3m mho, so R_C = 7.7kΩ, and C_c = 1.2nF.

Since the loop transfer function bode plot crosses the 0dB line at a slope of –40dB/decade, phase margin can be pretty low. A phase margin of 30° to 40° is typical. The phase margin is determined by how far the cutoff frequency is from the double pole, how far it is from the ESR zero and the damping of the system. A low phase margin tends to give an under-damped transient response. Fine-tuning on the bench is necessary to determine what compensation values make the best trade-off.

The user might be tempted to further increase the compensation gain G_{comp} by increasing R_C value so as to have a higher cutoff frequency and a better phase margin (because the cutoff frequency is getting closer to the ESR zero). He should be cautioned that there are parasitic parameters that start to take effect when it gets close to 1MHz. So he may lose phase margin instead by doing so. The best way to find out is still to fine-tune R_C on the bench.

The ESR of the same type of capacitor may differ from different vendors. Sometimes this may make one set of compensation values good for one brand of capacitor and bad for another. The solution is either stick with the working brand of capacitor or change the compensation values that work for both. However, the latter usually results in a compromise of the performance of load transient response.

Current Limit

The LM2639 can be configured to provide input current limit (see *Figure 5*). The way the circuit works is as follows. OC– pin draws a fixed amount of current from external resistor R_{LIM}. So the voltage of OC– pin can be preset to be any value below V_{IN} by adjusting the value of R_{LIM}. When I_{IN} is high enough, OC+ pin voltage will be lower than OC– pin, which will trigger the internal current limit comparator. A PCB trace can be used to act as the current sense resistor. To set the current limit, use an R_{LIM} value as calculated by the following equation:

$$R_{LIM} = \frac{I_{LIM} \bullet R_{sense} + V_{offset}}{I_{OC-}}$$

where I_{LIM} is the desired current limit value, R_{sense} is the resistance of the sense resistor value, V_{offset} is the input offset voltage of the current limit comparator (see data sheet), and I_{OC-} is the current drawn by OC- pin. The capacitor is used to get rid of possible high frequency noise. A value of 0.1µF is usually good enough.

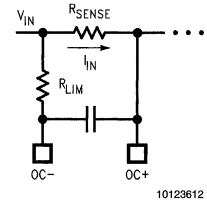


FIGURE 5. Current Limit Setup

Output Inductor Selection

There are several considerations when selecting the output inductors. The inductance should not be too high so as to hinder the load transient response. The inductance should not be too low to avoid high output voltage ripple and high hysteresis loss. To find out about the load transient response aspect, simulate the circuit operation using the average model of the regulator and see if the duty cycle saturates during a worst case load transient. If the duty cycle saturates, it means the inductor is probably too large. The most practical method to find out about the power loss is to measure it on the bench. As a first cut, use the 20% ripple current criterion to determine the inductance value.

Falco has some inductor designs that are very suitable for high frequency multi-phase operation. Popular models include the T02502 and T025A2. The former is 400nH, 10A nominal. The latter is 300nH, 10A nominal. Falco can be reached at (305) 662-9076 Ext. 206. Coiltronics also has some low inductance drum core inductors that are suitable for this type of applications.

Output Capacitor Selection

Output capacitor selection is closely related to loop stability, ripple voltage and load transient response. As has been discussed in the loop compensation section above, the ESR zero created by the output capacitors is important to phase margin and thus loop stability. Different vendors may have different ESR values for the same amount of capacitance. For multi-layer ceramic capacitors, ESR is usually determined by the number of layers.

Due to high frequency operation, the output ripple voltage is usually dominated by ESL rather than ESR or capacitance. So if ESR zero frequency is the same, to reduce the total ESL it is desirable to have more capacitors in parallel than fewer, even if they have the same total capacitance and ESR. It is probably a good idea to use some smaller capacitors in parallel with the larger ones to reduce the combined ESL.

Adding more capacitors will definitely help load transient response but the effect is not very significant unless the duty cycle tends to saturate during a large and fast load transient. The most effective way to reduce load transient excursions of output voltage is to increase the control bandwidth and make sure the output impedance is low enough so that duty cycle will not saturate.

Since multi-layer ceramic capacitors have very low ESR values, they seem to be more suitable for fast load transient applications. It would take too many low ESR tantalum or aluminum capacitors to achieve the same amount of com-

Output Capacitor Selection

(Continued)

bined ESR. The landscape changes with the speed of the regulator as compared to the load slew rate. In low switching frequency regulators, the speed of the regulator is slow anyway, the load transient response solely depends on the combined ESR of the output bulk capacitors. The high speed LM2639-based regulator enables the use of low value capacitors, and the load transient response is a combination of voltage across the ESR and the delta voltage caused by the capacitor discharge. The ESR becomes less and less important as the speed difference of the load and the regulator diminishes.

Murata and Taiyo Yuden offer some high capacitance multi-layer ceramic capacitors that are very suitable for LM2639-based solutions. As an example, both offer 22µF, 10V, Y5V ceramic capacitors in a 1210 package. Murata's part number is GRM235Y5V226Z and Taiyo Yuden's part number is LMK325F226ZN. They also have higher capacitance parts.

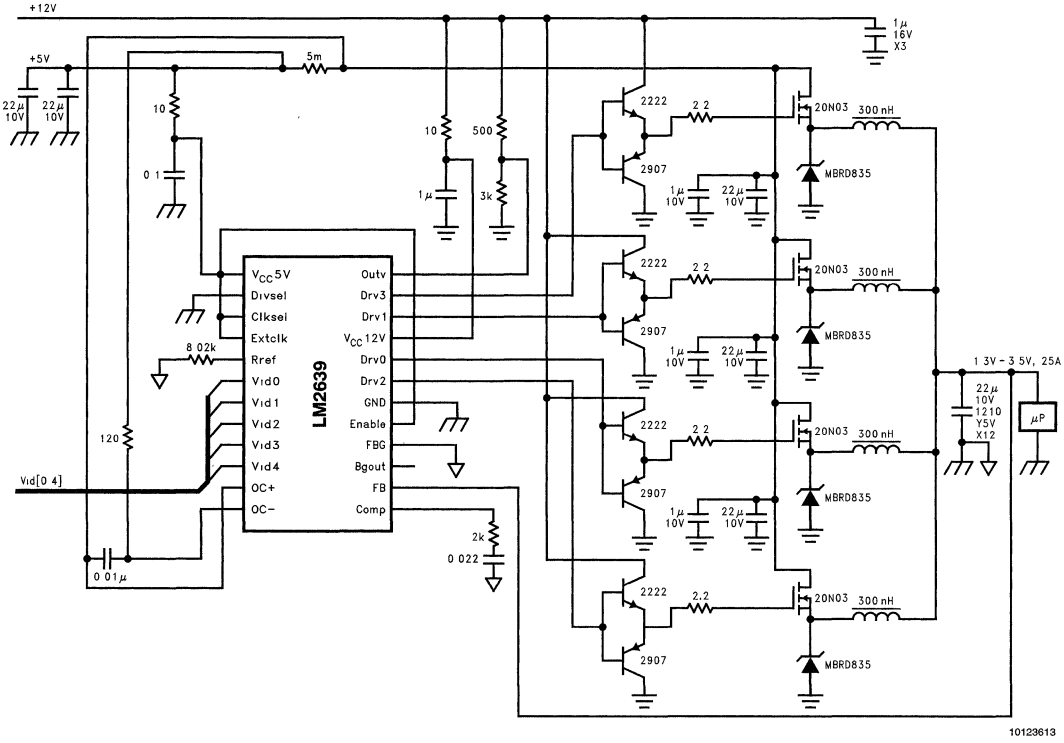
Input Capacitor and Inductor

An input filter is necessary if the input rail is also shared by other loads. The input capacitors will experience significant current when large load transient occurs. To limit the input rail di/dt, an input inductor is necessary. Refer to Intel VRM documents for input rail di/dt specification and LM2636 data sheet for input filter design.

PCB Layout Guidelines

1. Put grounding via the output capacitors as close to the ground as possible to reduce the ESL.
2. Use two or more via each ground pad when grounding the output capacitors.
3. Try to arrange the output capacitors as symmetrical as possible as appeared tro the output inductors so that the output voltage ripple will be minimized.
4. Consider using some of the board areas to provide a heat sink to the MOSFETs and diodes.
5. DO not place the LM2639 too close to the MOSFETs, diodes and inductors so that the IC will not be over-heated.
6. Keep the compensation components close to the LM2639 to minimize noise.
7. Use large pads for the external bipolar drivers to reduce temperature rise on them.
8. When designing the input rail current sense resistor using the PCB trace, use an inner layer to have good tolerance.
9. Keep the output inductors and capacitors close to the load to reduce distribution loss.
10. The DRV:4 traces do not have to be very short. They can be 10mil and can go a long way (such as a few inches) from the pins to the discrete drivers.
11. The traces form the discrete driver outputs to the MOSFETs can be 20mil to 30mil wide, and as long as 1 or 2 inches.
12. Connect the feedback ground pin (FBG) to the copper that is local to the load ground to have a good load regulation.

Typical Application



Layout Guidelines for Switching Power Supplies

National Semiconductor
Application Note 1149
Clinton Jensen

Introduction

When designing a high frequency switching regulated power supply, layout is very important. Using a good layout can solve many problems associated with these types of supplies. The problems due to a bad layout are often seen at high current levels and are usually more obvious at large input to output voltage differentials. Some of the main problems are loss of regulation at high output current and/or large input to output voltage differentials, excessive noise on the output and switch waveforms, and instability. Using the simple guidelines that follow will help minimize these problems.

Inductor

Always try to use a low EMI inductor with a ferrite type closed core. Some examples would be toroid and encased E core inductors. Open core can be used if they have low EMI characteristics and are located a bit more away from the low power traces and components. It would also be a good idea to make the poles perpendicular to the PCB as well if using an open core. Stick cores usually emit the most unwanted noise.

Feedback

Try to run the feedback trace as far from the inductor and noisy power traces as possible. You would also like the feedback trace to be as direct as possible and somewhat thick. These two sometimes involve a trade-off, but keeping it away from inductor EMI and other noise sources is the more critical of the two. It is often a good idea to run the feedback trace on the side of the PCB opposite of the inductor with a ground plane separating the two.

Filter Capacitors

When using a low value ceramic input filter capacitor, it should be located as close to the V_{IN} pin of the IC as possible. This will eliminate as much trace inductance effects as possible and give the internal IC rail a cleaner voltage supply. Some designs require the use of a feed-forward capacitor connected from the output to the feedback pin as well, usually for stability reasons. In this case it should also be positioned as close to the IC as possible. Using surface mount capacitors also reduces lead length and lessens the chance of noise coupling into the effective antenna created by through-hole components.

Compensation

If external compensation components are needed for stability, they should also be placed closed to the IC. Surface mount components are recommended here as well for the same reasons discussed for the filter capacitors. These should not be located very close to the inductor as well.

Traces and Ground Plane

Make all of the power (high current) traces as short, direct, and thick as possible. It is a good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381mm) per Ampere. The inductor, output capacitors, and output diode should be as close to each other possible. This helps reduce the EMI radiated by the power traces due to the high switching currents through them. This will also reduce lead inductance and resistance as well which in turn reduces noise spikes, ringing, and resistive losses which produce voltage errors. The grounds of the IC, input capacitors, output capacitors, and output diode (if applicable) should be connected close together directly to a ground plane. It would also be a good idea to have a ground plane on both sides of the PCB. This will reduce noise as well by reducing ground loop errors as well as by absorbing more of the EMI radiated by the inductor. For multi-layer boards with more than two layers, a ground plane can be used to separate the power plane (where the power traces and components are) and the signal plane (where the feedback and compensation and components are) for improved performance. On multi-layer boards the use of vias will be required to connect traces and different planes. It is good practice to use one standard via per 200mA of current if the trace will need to conduct a significant amount of current from one plane to the other.

Arrange the components so that the switching current loops curl in the same direction. Due to the way switching regulators operate, there are two power states One state when the switch is on and one when the switch is off. During each state there will be a current loop made by the power components that are currently conducting. Place the power components so that during each of the two states the current loop is conducting in the same direction. This prevents magnetic field reversal caused by the traces between the two half-cycles and reduces radiated EMI.

Heat Sinking

When using a surface mount power IC or external power switches, the PCB can often be used as the heatsink. This is done by simply using the copper area of the PCB to transfer heat from the device. Refer to the device datasheet for information on using the PCB as a heatsink for that particular device. This can often eliminate the need for an externally attached heatsink.

These guidelines apply for any inductive switching power supply. These include Step-down (Buck), Step-up (Boost), Flyback, inverting Buck/Boost, and SEPIC among others. The guidelines are also useful for linear regulators, which also use a feedback control scheme, that are used in conjunction with switching regulators or switched capacitor converters. Some layout pictures are included: *Figure 1* shows Step-up switching regulator schematic to be used for some layout examples. *Figure 2* is an example of a bad layout that violates many of the suggestions given. *Figure 3* and *Figure 4* show an example of a good layout that incorporates most of the suggestion given.

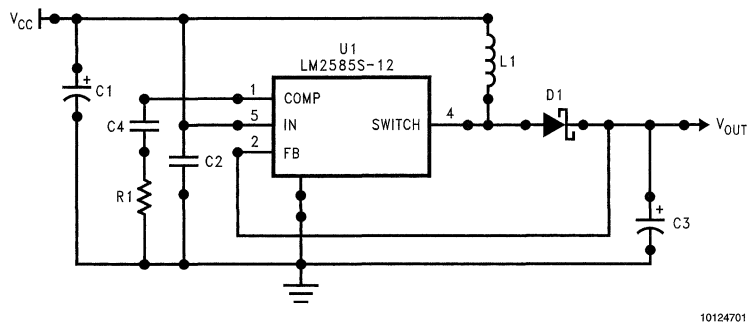


FIGURE 1. Step-up Switching Regulator Schematic

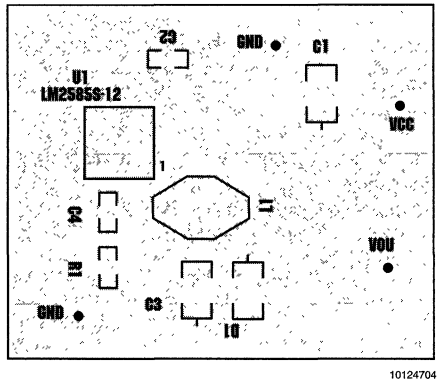


FIGURE 2. Bad Layout Example

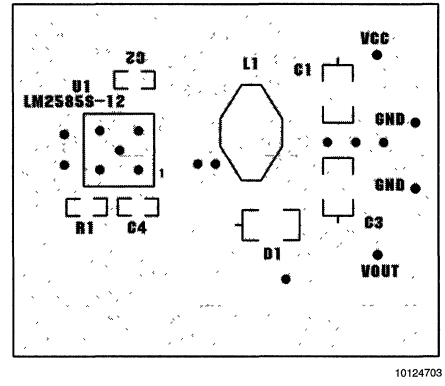


FIGURE 3. Good Layout Example, Top Layer

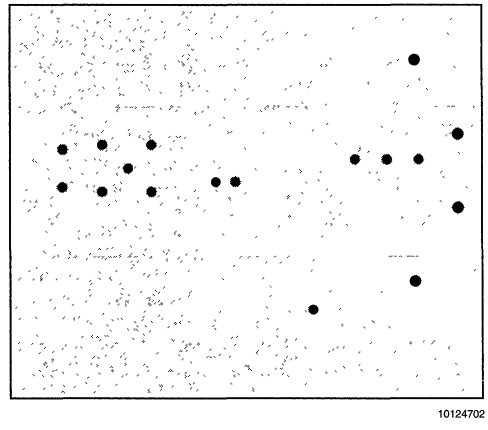


FIGURE 4. Good Layout Example, Bottom Layer

Positive to Negative Buck-Boost Converter Using LM267X SIMPLE SWITCHER® Regulators

National Semiconductor
Application Note 1157

Abstract

The 3rd generation Simple Switcher LM267X series of regulators are monolithic integrated circuits with an internal MOSFET switch. These regulators are simple to use and require only a few external components. In this article the design of a polarity inverting converter will be discussed.

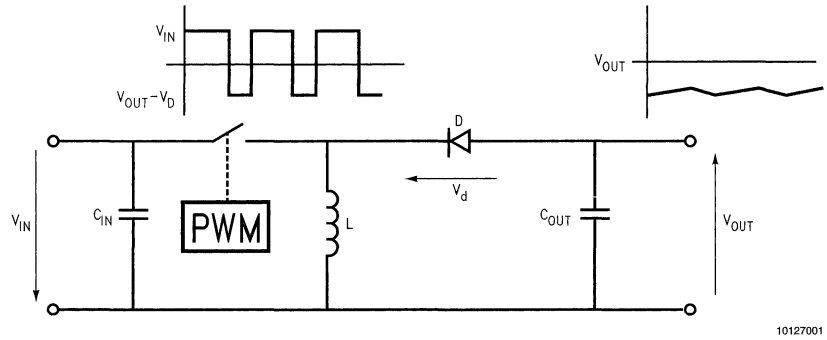


FIGURE 1. Basic Configuration of a Polarity Inverting Converter (Buck-Boost Converter)

Principle of Operation

The polarity-inverting converter, shown in *Figure 1*, uses the basic principle of energy storage in the inductor L during the first part of the operating period, and then transfers the energy via the free wheeling diode D to the output. When the switch turns on, the diode is reverse biased and the inductor current will ramp up linearly. When the switch is turned off, the inductor will reverse its polarity in order to maintain the peak switch current. Thus the free wheeling diode will be forward biased, and the energy stored in the inductance will be transferred to the load as well as the capacitor. (Please see switching waveforms *Figure 3* and *Figure 4*).

Since the node V_A at the "top end" of the inductor is negative with respect to ground, the output voltage across the capacitor will become negative.

It is important to notice this type of converter can step up and step down the magnitude of the input voltage. Therefore this circuit is also known as a buck-boost converter.

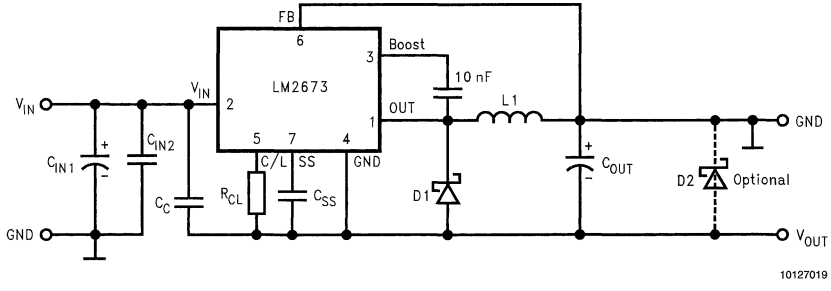


FIGURE 2. LM2673 Positive to Negative Converter

Design Considerations

Figure 2 shows the typical configuration of a polarity inverting regulator using the LM2673. Note that the ground is connected to the negative output and the feedback is referred to GND. Therefore no extra level shift and inversion of the feedback signal is needed to properly regulate the negative output. Such an application is also possible with the adjustable version of the LM2673 by connecting feedback resistors from GND to V_{OUT} (across the output capacitor).

Usually such a circuit is particularly difficult to stabilize because it has a right half plane zero in its control to output transfer function.Therefore a relatively small capacitor C_C

Design Considerations (Continued)

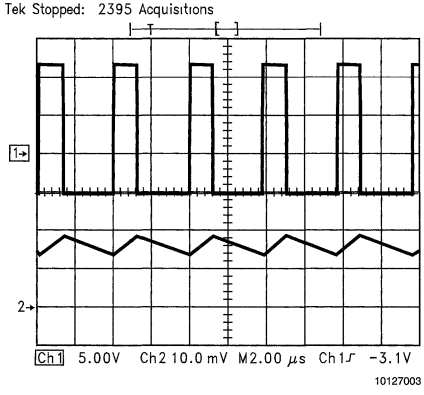
(compared to the input capacitor) is connected from the input to the negative output in order to provide more phase margin to stabilize the regulator loop. A small capacitor ≤ 100 µF yields the best performance.

For lower output currents ≤ 100 mA, the regulator can be operated in discontinuous mode and no capacitor C_C is required.

When the voltage is first applied to the circuit the initial capacitor charge current will cause a positive voltage spike at the output when the capacitor C_C is used. However this positive voltage spike is typically small enough to not cause any problems.

The initial capacitor charge current will cause a voltage drop across the capacitor ESR. Since the capacitor C_C and output capacitor form a voltage divider, the magnitude of the initial voltage spike depends on the ESR values of C_C and the output capacitor. Since the overall output capacitor ESR value is usually much smaller than the compensation capacitor ESR, the initial voltage spike is very small, typically 500 mV. if the inductor DC resistance is high (2Ω and greater) and the initial start-up current is high, the spike may be higher. The diode D2 would clamp the positive output voltage spike at around 300 mV in the case of a Schottky diode. In most cases this clamp is not required, and D2 can be omitted.

Figure 3 and *Figure 4* show the typical waveforms of the switching regulator.

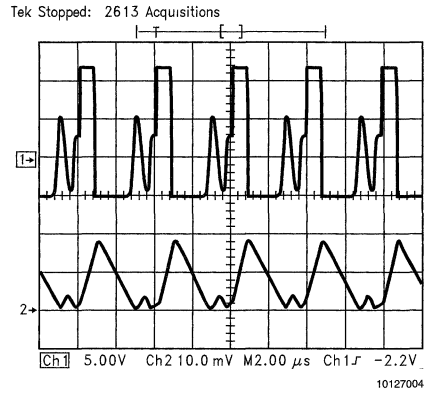


Upper Trace: Switch Voltage, 5V/div

Lower Trace: Inductor Current, 2A/div

Horizontal: 2µs/div

FIGURE 3. Continuous Mode



Upper Trace: Switch Voltage, 5V/div

Lower Trace: Inductor Current, 0.5A/div

Horizontal: 2µs/div

FIGURE 4. Discontinuous Mode

Component Selection

The section below will detail the calculation and selection of the circuit components. The calculations are done for continuous mode operation.

Inductor Selection

The duty cycle is calculated as:

$$D = \frac{|V_{OUT}| + V_d}{V_{IN} + |V_{OUT}| + V_d - V_{SW}}$$

where

V_d = Diode forward voltage

V_{sw} = Transistor Switch On voltage (please refer to datasheet for $R_{DS}(on)$ and for Isw_{max} see calculation below; $V_{sw} = Isw_{max} \bullet R_{DS}(on)$

Average inductor current I_L:

$$I_L = \frac{I_{OUT}}{1 - D}$$

There are different ways to calculate the required inductance. A good way to do this is to choose the inductor ripple current ΔI_L between 20% and 30% of the average inductor current I_L. This will make the regulator operate in continuous mode and the design will have a good load transient response with an acceptable output ripple voltage.

Inductor Selection (Continued)

Therefore the peak-to-peak inductor ripple current ΔI_L is selected as:

$$\Delta I_L \cong 0.2 \text{ to } 0.3 \bullet I_L$$

Required inductance:

$$L = \frac{V_{IN} \cdot D}{f \cdot \Delta I_L}$$

where f = Switching Frequency

The inductor should have a RMS current rating equal or greater than the maximum switch current Isw_{max} in order to avoid saturation of the inductance. In addition, the inductor should have a volt-second rating of at least:

$$E \bullet T = V_{IN} / D \bullet f$$

IC Device Ratings

The DC/DC Converter has to be rated for the maximum current and voltage ratings.

Peak switch current:

$$Isw_{max} = I_L + \frac{\Delta I_L}{2}$$

Since the ground of the device is connected to output, the maximum input voltage rating of the device has to be able to handle the nominal application input voltage plus the output voltage.

Peak switch voltage and input voltage rating of the IC:

$$Vsw_{max} = V_{IN} + |V_{OUT}|$$

Power Dissipation:

$$P_D = V_{IN} \bullet I_q + Isw_{max}^2 \bullet R_{DS}(on)$$

Please refer to datasheet for $R_{DS}(on)$.

Maximum switch current depends on the duty cycle D and the inductor value. This is important to know because a 3A step down regulator like the LM2673 cannot always deliver 3A load current in such a topology, as shown in *Figure 5.*

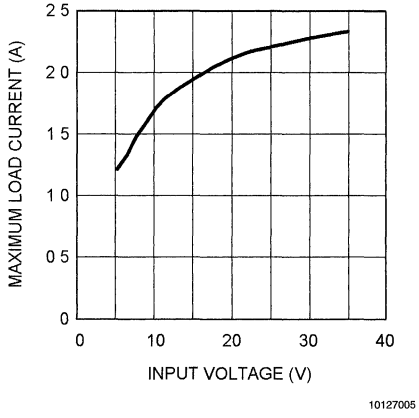


FIGURE 5. LM2673 Input Voltage vs. Load Current (V_{OUT} = −5V, L = 33µH)

Diode Ratings

The free wheeling diode D1 has to be able to handle the following parameters:

$$I_{Dmax} = Isw_{max}$$

$$V_{Dmax} = V_{IN} + |V_{OUT}|$$

$$P_D = I_{Dmax} \bullet V_D \bullet (1-D)$$

Usually a Schottky diode with a low forward voltage rating is chosen to achieve good converter efficiency.

Output Capacitor Selection

The output capacitor has to be selected mainly on its ESR value, and the capacitance must be able to deliver the load current when the switch is on. The ESR value will be the main parameter in determining the output voltage ripple. Because at the first moment when the free wheeling diode becomes forward biased only the output capacitor ESR value determines the load impedance and therefore the ripple voltage.

Thus the required ESR for a desired output ripple voltage is calculated as:

$$ESR = \frac{\Delta V_{OUT}}{Isw_{max}};$$

where

ΔV_{OUT} = Desired output ripple voltage

The minimum capacitor value for a desired output ripple and load current is:

$$C_{OUT_{min}} = \frac{I_{OUT} \ D}{f \ \Delta V_{OUT}}$$

Input Capacitor Selection

The input capacitor is selected mainly on its ESR value and on the RMS current rating its order to support the high current changes on the input. Low ESR capacitors are recommended in order to minimise the input voltage ripple and the interference with other circuits in the system. An additional L-C input filter might be considered for EMI sensitive applications.

Efficiency

The efficiency is calculated as detailed below. This calculation does not include the inductor, copper and capacitor losses but becomes very close to what you can expect in the final application.

$$\eta = \frac{V_{IN} - V_{SW}}{V_{IN}} \cdot \frac{|V_{OUT}|}{|V_{OUT}| + V_D}$$

Example: Inverting Regulator, 12V Input to −5V Output at 1.5A Load Current

For this example, we will assume the freewheeling diode D1 is Schottky, with a forward voltage drop of 0.5V. We can estimate the switch voltage to be 0.5V, although it may be a little different in the actual application.

Example: Inverting Regulator, 12V Input to −5V Output at 1.5A Load Current (Continued)

The duty cycle is:

D = (5V+0.5V)/(12V+5V+0.5V−0.5V)=0.32

Calculate parameters related to the inductor:

I_L= 1.5A/(1−0.33) = 2.21A

ΔI_L= 0.2•I_{OUT} = 0.44A

L = (12V•0.32)/(260kHz•0.44A) = 33.6µH

E•T = (12V+5V)/(0.32•260kHz) = 204V•µs

Peak inductor current is the same as the peak switch current:

I_{SWmax} = 2.21A + (0.44A/2) = 2.43A

An appropriate choice of inductor would be 33µH, rated for more than 3A and 210V•µs. An appropriate switching regulator IC would be the LM2673-5.0, which has a 3A/40V switch rating and 40V input rating. In addition, the LM2673-5.0 is configured to control a −5V output in this topology. The LM2673 has an R_{DSon} of 0.15Ω; checking the switch voltage estimate, we find it to be

V_{SWmax} = 2.43A•0.15Ω = 0.37V

This lower switch voltage will slightly reduce the peak switch current, but will not significantly change the other calculations.

The resulting circuit is shown in *Figure 6*. Its efficiency is typically 82% at full load.

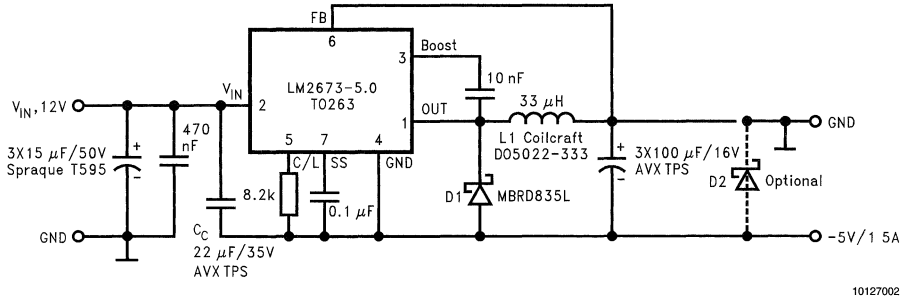


FIGURE 6. 5V to −15V/150mA Buck Boost Converter

PCB Layout Guidelines

A recommended printed circuit board (PCB) layout for the LM267X inverting regulator is shown in *Figure 7*.

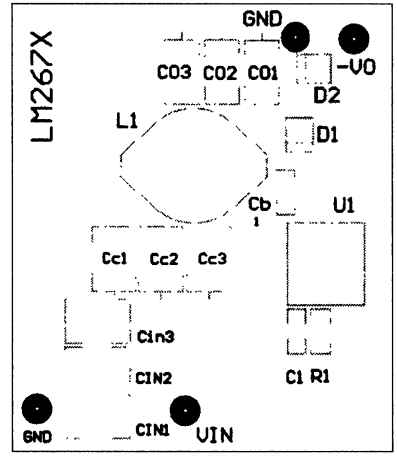
It is very important to place the input capacitor as close as possible to the input pin of the regulator. In order to achieve the best performance special care has to be taken for proper grounding. A good practice is always the use of a separate ground plane or at least a single point ground structure. At higher load currents like >1A, special care of metal traces and component placement has to be taken. One reason for this is that high switching currents cause voltage drops in the PCB metal trace, and long metal traces and component leads cause parasitic unwanted inductance as well, especially at switching frequencies of 260kHz and above. This parasitic inductance is very often main source of high voltage spikes at input and output lines and EMI problems.

Therefore place the inductor, free wheeling diode, and especially the input capacitor as close as possible to the IC. Use heavy lines for the metal traces to these components.

Wire the feedback circuit away from the inductor in order to avoid flux intersection. Use shielded cores for better EMI performance.

In sensitive applications, input and output voltage spikes may still not be acceptable even if low ESR input and output filter capacitors are already used. In such a case, input and output L/C filters should be considered.

PCB Layout Guidelines (Continued)



10127020

Top Layer

10127021

Silk Screen

L1 = DO5022-333. Coilcraft
C_{IN} = 3x15µF/50V Spraque T595
C_{OUT} = 3x100µF AVX TPS Series
D1 = MBRD835L
C_C = 22µF/35V AVX TPS Series

FIGURE 7. LM2673 Demo Board 12V to −5V/1.5A; Please refer to *Figure 6* for the application circuit

Stability Considerations

Pulse-width modulated switch mode DC/DC converters consist of a frequency response control loop, and therefore the design has to fulfill the stability criteria of a control loop.

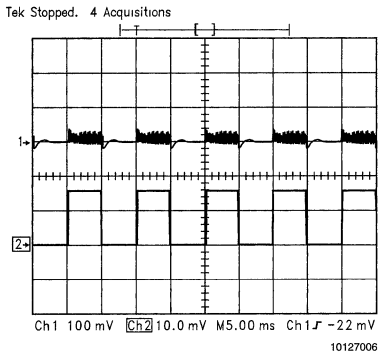
Since the value of the inductance, output capacitor value and ESR, and compensation capacitor C_C will influence the regulator loop stability, the converter has to be tested for stability.

The first test for stability is to check the switch voltage waveform across the semiconductor switch, which is the output pin of the LM2673. This waveform should be stable and free of jitter as it is shown in *Figure 3* and *Figure 4* for continuous and discontinuous operation.

If this is the case under all input voltage and load current conditions it is already a good indication of a stable design.

The next measurement is the pulsating load test, or load transient response. During this test the load current is pulsed (rectangular waveform, fast rise time) between minimum and maximum load. The output voltage waveform is monitored with an oscilloscope. Please see *Figure 8*. Under these conditions the output voltage should respond without any oscillation to the load current changes. This has to be verified again under all input voltage conditions.

If the regulator exhibits stability problems during these tests, the output capacitor and/or compensation capacitor C_c has to be changed accordingly. For the LM267x inverting buck-boost applications, the stability will usually improve with an increase in the capacitor value of C_C (use a low ESR capacitor).



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Upper Trace: Output Voltage, 100mV/div
Lower Trace: Load Current, 1A/div
Horizontal: 2µs/div

FIGURE 8. Load Transient Response Shows Stable Operation

Startup Considerations

At low input voltages (down to 5V), the LM267x series of switching regulators can take full advantage of the buck-boost topology. Usually these regulators have a minimum input voltage requirement of V_{IN} = 6.5V, because of the internal 5V regulator which provides the internal bias for the IC.

Since the ground of the device is connected to the output, the resulting voltage from V_{IN} to GND is the input voltage plus the magnitude of the output voltage, typically totalling over 8V. Please refer to the chapter "Device Ratings". Therefore, the part initially has 5V at the input enabling the device to start up, and as soon as the output goes negative the input voltage of the device will raise eventually up to (V_{IN} + V_{OUT}) which is greater than 6.5V and well within the specification.

Inverting regulators often require high peak input currents during startup. These can be minimized by using the soft-start feature of the switching regulator IC.

Selecting Inductors for Buck Converters

National Semiconductor
Application Note 1197
Sanjaya Maniktala

Introduction

This Application Note provides design information to help select an off-the-shelf inductor for any continuous-mode buck converter application.

The first part shows how the designer should estimate his requirements, specifically the required inductance

The next part takes an off-the-shelf inductor and shows how to interpret the specs provided by the vendor in greater detail. A step-by-step procedure is provided.

Finally, all the previous steps are consolidated in a single design table, which answers the question: "How will the selected inductor actually perform in a specific application?"

The important point to note here is that though every inductor is designed assuming certain specific 'design conditions', that does not imply that these conditions cannot be varied. In fact every inductor can be satisfactorily used for many applications. But to be able to do this, the designer must know how to be able to accurately predict, or extrapolate, the performance of the inductor to a new set of conditions, which are his specific 'application conditions'. It will be shown that 'intuition' can be rather misleading. A detailed procedure is required and is presented in the form of the Design Table (*Table 2*) and the Selection Flow Chart (*Figure 2*).

Background: The Inductor Current Waveform

Refer to *Figure 1*, which shows the current through an inductor in continuous mode operation (bold line). Consider its main elements:

1. I_{DC}
   - — is the geometrical center of the AC/ramp component
   - — is the average value of the total inductor current waveform
   - — is the current into the load, since the average current through the output capacitor, as for any capacitor in steady state, is zero
2. I_{PEAK} is $I_{DC}+\Delta I/2$, and it determines the peak energy in the core ($e = \frac{1}{2}*L*I^2$), which in turn is directly related to the peak field the core must withstand without saturating.
3. I_{TROUGH} is $I_{DC}-\Delta I/2$ and determines the constant residual level of current/energy in the inductor. Note that it depends on the load, even though it is not itself transferred to the load.
4. The AC component of the current is
   $I_{AC} = \Delta I = I_{PEAK} - I_{TROUGH}$
5. The DC component is the load current for the case shown in the figure.
   $I_{DC} = I_O$
   where I_O is the maximum rated load.
6. and 'r' is defined as the ratio of the AC to DC components (current ripple ratio) evaluated at maximum load, I_O. Note that by definition 'r' is a constant for a given converter/application (as it is calculated only at maximum load), and it is also defined only for continuous conduction mode.

$$r = \frac{\Delta I}{I_O}$$

A high inductance reduces ΔI and results in lower 'r' (and lower RMS current in the output capacitor), but may result in a very large and impractical inductor So typically, for most buck regulators, 'r' is chosen to be in the range of 0.25–0.5 (at the maximum rated load). *See Appendix to this Application Note.* Once the inductance is selected, as we decrease the load on the converter (keeping input voltage constant), ΔI remains fixed but the DC level decreases and so the current ripple ratio increases. Ultimately, at the point of transition to discontinuous mode of operation, the DC level is $\Delta I/2$ as shown in *Figure 1*. So

- The current ripple ratio at the point of transition to discontinuous mode is 2. Therefore, the upper limit for 'r' is also 2.
- The load at which this happens can be shown by simple geometry to be r/2 times I_O. So for example, if the inductance is chosen to be such that 'r' is 0.3 at a load of 2A, the transition to discontinuous mode of operation will occur at 0.15 times 2A, which is 300 mA.

Note: If the inductor is a 'swinging' inductor, its inductance normally increases as load current decreases and the point of transition to discontinuous mode may be significantly lower We do not consider such inductors in this Application Note

Estimating Requirements for the Application

There are two equivalent ways to go about calculating the required inductance and the designer should be aware of both.

BASIC METHOD TO CALCULATE L

From the general rule V = L*dI/dt we get during the ON time of the converter:

$$V_{IN} - V_{SW} - V_O = L \times \frac{\Delta I}{D/f}$$

where V_{IN} is the applied DC input voltage, V_{SW} is the voltage across the switch when it is ON, D is the duty cycle and f is the switching frequency in Hz. Solving for ΔI we can write 'r' as:

$$r = \frac{(V_{IN} - V_{SW} - V_O) \times D}{L \times f \times I_O}$$

Now, for a buck regulator, we can show that the duty cycle is

Estimating Requirements for the Application (Continued)

$$D = \frac{V_O + V_D}{V_{IN} - V_{SW} + V_D}$$

where V_D is the forward drop across the catch diode (≅ 0.5V for a Schottky diode).

'r' can be finally written as:

$$r = \frac{(V_{IN} - V_{SW} - V_O) \times (V_O + V_D)}{(V_{IN} - V_{SW} + V_D) \times L \times f \times I_O}$$

and L is therefore

$$L = \frac{(V_{IN} - V_{SW} - V_O) \times (V_O + V_D)}{(V_{IN} - V_{SW} + V_D) \times r \times f \times I_O} \times 10^6 \ \mu H$$

where f is in Hz.

EXAMPLE 1

The input DC voltage is 24V into an LM2593HV buck converter. The output is 12V at a maximum load of 1A. We require an output voltage ripple of 30 mV peak-to-peak (±15 mV). We assume V_{SW} = 1.5V, V_D = 0.5V and f = 150,000 Hz.

Since, for loop stability reasons, we should not use any output capacitor of less than 100 mΩ, and since we do not wish to use an LC post filter, our ΔI must be

$$\Delta I = \frac{30\ mV}{100\ m\Omega} = 0.3A$$

So 'r' is

$$r = \frac{0.3}{1.0} = 0.3$$

The required inductance is

$$L = \frac{(24 - 1.5 - 12) \times (12 + 0.5)}{(24 - 1.5 + 0.5) \times 0.3 \times 150000 \times 1.0} \times 10^6 \ \mu H$$

L = 127 µH

The required energy handling capability is next calculated. Every cycle, the peak current is

$$I_{PEAK} = I_O + \frac{\Delta I}{2} = 1.0 + \frac{0.3}{2} A$$

$$I_{PEAK} = 1.15A$$

The required energy handling capability 'e' is

$$e = \frac{1}{2} \times L \times I_{PEAK}^2 \ \mu J$$

where L is in µH. So

$$e = \frac{1}{2} \times 127 \times 1.15^2 = 84 \ \mu J$$

Note: During a hard power-up (no soft start) or abnormal conditions like a short circuit on the output, the feedback loop is not effective in limiting the current to the value used above for calculating the energy handling capability. The current is actually going to hit the internal current limit of the device, I_{CLIM} in *Figure 1*, and this could be much higher than the steady state value calculated above. If the inductor has saturated, and if the input DC voltage is higher than 40V the current could slew up at a rate so high that the controller may not be able to limit the current at all, leading to destruction of the switch. Luckily, most off-the-shelf inductors are designed with large inherent air gaps and do not saturate very sharply even under overload conditions. **However we strongly recommend that at least when the input voltage is above 40V, the inductor should be sized to handle the worst case energy e_{CLIM}:**

$$e_{CLIM} = \frac{1}{2} \times L \times I_{CLIM}^2 \ \mu J$$

where L is in µH and I_{CLIM} is the internal limit of the regulator in amps.

VOLTSECONDS METHOD TO CALCULATE L

Talking in terms of voltseconds allows very general equations and curves to be generated. Here we talk of voltsµsecs or 'Et' which is simply the voltage across the winding of the inductor times the duration in µsecs for which it is applied.

Note:

- Current ramps up to the same peak value whether V (the applied voltage across inductor) is large but t (the time for which V is applied) is small, or whether V is small but t is large. So an infinite number of regulators with different combinations of input and output voltages but having the same voltseconds are actually the same regulator from the viewpoint of basic magnetics design. Et is what really counts. (The only exception to this is the Core Loss term since this depends directly on the absolute value of the frequency too, not just the Et)
- Also, Et can be calculated during the ON-time, (Vµsecs gained), or during the OFF-time (Vµsecs lost). Both will give the same result since there is no net change in Vµsecs per cycle in steady state.
- Also, remember that though Vµsecs is related to the energy in the core, it does not tell us the total energy. The Vµsecs gives information only about the AC component of 'r', i.e., ΔI. Combined with the DC component I_{DC}, it determines the peak current and energy of the inductor. So both I_O and Et are the variables on which our design procedure and tables are based upon. But a given application is completely defined by a certain I_O and Et (and frequency for the core loss term), and so these cannot be changed. Our only degree of freedom is L (or 'r') and we fix it according to the guidelines in the Appendix.

From the general equation V = L*dI/dt we can write that V*dt = L*dI. Here V*dt is the applied voltseconds. So by definition

$$Et = V\Delta t = L\Delta I \ V\mu secs$$

where L is in µH. 'r' can therefore be written as

$$r = \frac{Et}{L \times I_O}$$

Solving for L

$$L = \frac{Et}{r \times I_O} \mu H$$

which gives us an alternate and more general way of calculating L.

Estimating Requirements for the Application (Continued)

EXAMPLE 2

We repeat Example 1 from the viewpoint of Et.

The ON-time is

$$t_{ON} = \frac{D}{f} = \frac{(12 + 0.5) \times 10^6}{(24 - 1.5 + 0.5) \times 150000} \ \mu s$$

t_{ON} = 3.62 µsecs

So Et is

Et = (V_{IN}–V_{SW}–V_O) x t_{ON} = (24–1.5–12) x 3.62 Vµsecs

Et = 38.0 Vµsecs

L is therefore

$$L = \frac{Et}{r \times I_0} \ \mu H$$

$$L = \frac{38.0}{0.3 \times 1.0} \ \mu H$$

L = 127 µH

which gives us the same result as in Example 1 as expected.

SUMMARY OF REQUIREMENTS

- An inductance of 127 µH (or greater, based on maximum 'r' of 0.3)
- DC load of 1A (to ensure acceptable temperature rise, specify ΔT) **OR** steady state Energy handling capability of 84 µJ
- Peak load of 4.0A (to rule out core saturation if DC input voltage ≥40V) **OR** peak energy handling capability of 1016 µJ. (Max Current Limit of LM2593HV is 4.0A)
- Et of 38 Vµsecs
- Frequency 150 kHz

These can be communicated directly to a vendor for a custom-built design.

Characterizing an Off-the-Shelf Inductor

With reference to our design flow chart in *Figure 2*, the first pass selection is based upon inductance and DC current rating. We tentatively select a part from Pulse Engineering because its L and I_{DC} are close to our requirements, even though the rest does not seem to fit our application (see *Table 1* and bullets below). In particular the frequency for which the inductor was designed is 250 kHz, but our application is 150 kHz. We are intuitively lead to believe that since we are decreasing the frequency our core losses will go up, and so will the peak flux density. In fact the reverse happens in our case, and that is why it is important to follow the full procedure presented below. 'Intuition' can be very misleading.

The vendor also states that:

- The inductor is such that 380 mW dissipation corresponds to 50˚C rise in temperature.
- The core loss equation for the core is $6.11 \times 10^{-18} \times B^{2.7} \times f^{2.04}$ mW where f is in Hz and B is in Gauss.
- The inductor was designed for a frequency of 250 kHz.
- Et_{100} is the Vµsecs at which 'B' is 100 Gauss.

Note: For core loss equations it is conventional to use *half* the peak-to-peak flux swing So, like most vendors, the 'B' above actually refers to ΔB/2 This must be kept in mind in the calculations that follow

The step-by-step calculations are:

a) AC Component of Current:

This can be easily calculated from

Et = LΔI Vµsecs

where L is in µH.

So

$$\Delta I = \frac{Et}{L} = \frac{59.4}{137} = 0.434A$$

b) 'r':

So this inductor has been designed for the following 'r'

$$r = \frac{\Delta I}{I_0} = \frac{0.434}{0.99}$$

r = 0.438

at a load current of 0.99A.

c) Peak Current:

$$I_{PEAK} = I_0 + \frac{\Delta I}{2} = 0.99 + \frac{0.434}{2} \ A$$

I_{PEAK} = 1.21A

d) RMS Current:

$$I_{RMS} = \sqrt{I_0^2 + \frac{\Delta I^2}{12}} \ A$$

$$I_{RMS} = \sqrt{0.99^2 + \frac{0.434^2}{12}} \ A$$

I_{RMS} = 0.998A

e) Copper Loss:

This is

$P_{CU} = I_{RMS}^2$ x DCR mW

where DCR is in mΩ.

In most cases, to a close approximation, we can simply use I_{DC} instead of I_{RMS} in the above equation. Also sometimes, the vendor may have directly given the RMS current rating of the inductor.

$P_{CU} = 0.998^2$ x 387 mW

P_{CU} = 385 mW

f) The AC Component of the B-Field:

This is proportional to the AC component of the inductor current.

Characterizing an Off-the-Shelf Inductor (Continued)

The vendor has provided the information that an Et of Et_{100} = 10.12 Vμsecs produces 100 Gauss (B). So since the inductor is designed for an Et = 59.4 Vμsecs, we get

$$B = \frac{Et}{Et_{100}} \times 100 = \frac{59.4}{10.12} \times 100 \text{ Gauss}$$

B = 587 Gauss

But this is half the peak-to-peak swing by convention. So

ΔB = 2•B = 1174 Gauss

CHECK: We can use the alternative form for ΔB as given in *Table 2*. We asked the vendor for more details than he had provided on the datasheet and we learned that the effective area of the core, A_e, is 0.0602 cm^2 and the number of turns is N = 84. So

$$\Delta B = \frac{100 \cdot Et}{N \cdot A_e} \text{ Gauss}$$

$$\Delta B = \frac{100 \cdot 59.4}{84 \cdot 0.0602} = 1175 \text{ Gauss}$$

which is what we expected.

g) The DC Component of the B-Field:

This is proportional to the DC component of the inductor current. In fact the instantaneous value of B can always be considered proportional to the instantaneous value of the current (for a given inductor).

The proportionality constant is known from f) above, i.e., a ΔI of 0.434A produces a ΔB of 1174 Gauss. So the DC component of the B-field must be

$$B_{DC} = \frac{\Delta B}{\Delta I} \times I_{DC} \text{ Gauss}$$

where

$I_{DC} = I_O = 0.99A$

$$B_{DC} = \frac{1174}{0.434} \times 0.99 \text{ Gauss}$$

B_{DC} = 2678 Gauss

h) Peak B-Field:

Since B is proportional to I, we can write for the peak B-field

$$B_{PEAK} = B_{DC} + \frac{\Delta B}{2} \text{ Gauss}$$

$$B_{PEAK} = 2678 + \frac{1174}{2} \text{ Gauss}$$

B_{PEAK} = 3265 Gauss

i) Core Loss:

The vendor has stated that core loss (in mW) is 6.11 x 10^{-18} x $B^{2.7}$ x $f^{2.04}$ watts where f is in Hz and B is in Gauss.

$$P_{CORE} = 6.11 \times 10^{-18} \times \left[\frac{\Delta B}{2}\right]^{2.7} \times f^{2.04} \text{ mW}$$

$P_{CORE} = 6.11 \times 10^{-18} \times 587^{2.7} \times 250000^{2.04}$ mW

P_{CORE} = 18.7 mW

j) Total Inductor Loss:

$P = P_{CU} + P_{CORE}$ mW

P = 385 + 18.7 mW

P = 404 mW

k) Thermal Resistance of Inductor:

The vendor has stated that 380 mW dissipation corresponds to a 50°C rise in temperature. So thermal resistance of the inductor is

$$R_{TH} = \frac{50}{\frac{380}{1000}} \text{ °C/W}$$

R_{TH} = 131.6°C/W

l) Estimated Temperature Rise of Inductor:

$$\Delta T = R_{TH} \times \frac{P}{1000} \text{ °C}$$

$$\Delta T = 131.6 \times \frac{404}{1000} \text{ °C}$$

ΔT = 53°C

Here the temperature rise 'ΔT' is the temperature of the core, 'T_{CORE}' minus the worst case ambient temperature '$T_{AMBIENT}$'. The 'ambient' is the local ambient around the inductor.

m) Energy Handling Capability of Core:

$$e = \frac{1}{2} \times L \times I_{PEAK}^2 \text{ μJ}$$

where L is in μH

$$e = \frac{1}{2} \times 137 \times 1.21^2 \text{ μJ}$$

e = 100 μJ

As before, we warn that the energy in the core during hard power-up or a short circuit on the outputs, may be significantly higher.

In case of soft-start it should also be remembered that there are several ways to implement this feature, and not all lead to a reduction in switch or inductor current at start-up. The worst condition is *start-up with a short already present on the output.* The inductor waveforms should therefore be monitored on the bench during all conditions to check this out.

Also it will be seen that all inductors of a 'family', i.e., using the same core will typically have the same rated energy capability. So if this core is found to be inadequate, normally the only way out is to move to a physically larger core/inductor. Other options include the use of improved and more expensive core materials.

Characterizing an Off-the-Shelf Inductor (Continued)

SUMMARY OF INDUCTOR PARAMETERS

- The inductor is designed for about 50°C rise in temperature over ambient at a load of 1A.
- The copper losses (385 mW) predominate (as is usual for such inductors/core materials) and the core losses are relatively small.
- The peak flux density is about 3200 Gauss, which occurs at a peak instantaneous current of 1.2A.
- The rated energy handling capability of the core is 100 µJ.

Note: Most vendors do not explicitly provide the material used, though an astute designer can figure this out by looking at the exponents of B and f in the core loss equation provided, or of course simply by asking the vendor In this case we know that the material is ferrite and can typically handle a peak flux density of over 3000–4000 Gauss before it starts to saturate (Caution not all ferrite grades are similar in this regard and also that the saturation flux density B_{SAT} falls as the core heats up)

Evaluating the Inductor for the Actual Application

Above we have the limits of the inductor operating under its design conditions We will now *extrapolate* its performance to our specific application conditions. Unprimed parameters are the original 'design values', and the corresponding primed parameters are the extrapolated 'application values'.

The following are the design conditions (these may be allowed to change):

- I_{DC}
- Et
- f
- $T_{AMBIENT}$

The 'Application Conditions' are:

- I'_{DC}
- Et'
- f'
- $T'_{AMBIENT}$

In going from the 'Design Conditions' to the 'Application Conditions' the following are considered constant

- L
- DCR
- Rth
- The core loss equation

And, finally, to 'approve' the inductor for the given application we need to certify

- 'r' is acceptable (choice of L)
- B_{PEAK} OK.
- $I_{PEAK} < I_{CLIM}$.
- ΔT OK (evaluate $P_{CU} + P_{CORE}$).
- $B_{CLIM} < B_{SAT}$ (if DC input voltage is ≥40V).

We assume the vendor has provided all the following inputs:

- Et (Vµsecs)
- Et_{100} (Vµsecs per 100 Gauss)
- L (µH)
- I_{DC} (Amps)
- DCR (mΩ)
- f (Hz)
- The form for core losses (mW) as $a*B^{b}*f^{c}$, where B is in Gauss, f in Hz. Note that B is half the peak-to-peak flux swing.
- Thermal resistance of inductor in free air (°C/W)

If any of these are unknown, the vendor should be contacted. *Table 2* condenses the step-by-step procedure given earlier and also shows how to 'extrapolate' the performance of the inductor.

EXAMPLE 3

This shows the complete selection procedure. Refer to *Table 2* and *Figure 2*. We have seen that the 'Design Conditions' of the inductor are:

- Et = 59.4 Vµsecs
- f = 250,000 Hz
- I_{DC} = 0.99A

Our 'Application Conditions' are

- Et' = 38 Vµsecs
- f' = 150,000 Hz
- I'_{DC} = 1A

(We assume that $T_{AMBIENT}$ is unchanged so we can ignore it above).

We need to verify that using the inductor in the given application:

a) current ripple ratio 'r' is close to desired

b) peak flux density/current are within bounds

c) temperature rise is acceptable

Using *Table 2*:

a) 'r':

Design Value:

$$r = \frac{Et}{L \cdot I_{DC}}$$

$$r = \frac{59.4}{137 \cdot 0.99}$$

r = 0.438

Extrapolated to our Application:

$$r' = r \cdot \left[\frac{Et' \cdot I_{DC}}{Et \cdot I'_{DC}}\right]$$

$$r' = 0.438 \cdot \left[\frac{38 \cdot 0.99}{59.4 \cdot 1}\right]$$

r' = 0.277

We expected 'r' to be slightly lower than 0.3 since the chosen inductor has a higher inductance than we required (137 µH instead of 127 µH). This is acceptable however as the output voltage ripple will be less than demanded.

b) Peak Flux Density

Design Value:

Evaluating the Inductor for the Actual Application (Continued)

$$B_{PEAK} = \frac{200}{Et_{100}} \cdot \left[(I_{DC} \cdot L) + \frac{Et}{2} \right] \text{Gauss}$$

$$B_{PEAK} = \frac{200}{10.12} \cdot \left[(0.99 \cdot 137) + \frac{59.4}{2} \right] \text{Gauss}$$

B_{PEAK} = 3267 Gauss

Extrapolated to our Application:

$$B'_{PEAK} = B_{PEAK} \cdot \left[\frac{2 \cdot L \cdot I'_{DC} + Et'}{2 \cdot L \cdot I_{DC} + Et} \right] \text{Gauss}$$

$$B'_{PEAK} = 3267 \cdot \left[\frac{2 \cdot 137 \cdot 1 + 38}{2 \cdot 137 \cdot 0.99 + 59.4} \right] \text{Gauss}$$

B'_{PEAK} = 3084 Gauss

which is less than B_{PEAK} and therefore acceptable.

c) Peak Current

To ensure that the regulator will deliver rated load, we need to ensure that the peak current is less than the internal current limit of the Switcher IC.

Design Value:

$$I_{PEAK} = I_{DC} + \frac{Et}{2 \cdot L} \text{A}$$

$$I_{PEAK} = 0.99 + \frac{59.4}{2 \cdot 137} \text{A}$$

I_{PEAK} = 1.21A

This corresponds to a B-field of 3267 Gauss as calculated above.

Extrapolated to our Application:

$$I'_{PEAK} = I_{PEAK} \cdot \left[\frac{(2 \cdot L \cdot I'_{DC}) + Et'}{(2 \cdot L \cdot I_{DC}) + Et} \right] \text{A}$$

$$I'_{PEAK} = 1.21 \cdot \left[\frac{(2 \cdot 137 \cdot 1.0) + 38}{(2 \cdot 137 \cdot 0.99) + 59.4} \right] \text{A}$$

I'_{PEAK} = 1.14A

This corresponds to a B-field of 3084 Gauss as calculated above and is less than I_{CLIM}. (Min Current Limit of LM2593HV is 2.3A).

d) Temperature Rise:

Design Values:

$$P_{CU} = DCR \cdot \left(I_{DC}^2 + \frac{Et^2}{12 \cdot L^2} \right) \text{mW}$$

$$P_{CU} = 387 \cdot \left(0.99^2 + \frac{59.4^2}{12 \cdot 137^2} \right) \text{mW}$$

P_{CU} = 385 mW

$$P_{CORE} = a \cdot \left[\frac{Et}{Et_{100}} \cdot 100 \right]^b \cdot f^c \text{ mW}$$

where the vendor has provided that $a = 6.11 * 10^{-18}$, b = 2.7 and c = 2.04. So

$$P_{CORE} = 6.11 \cdot 10^{-18} \cdot \left[\frac{59.4}{10.12} \cdot 100 \right]^{2.7} \cdot f^{2.04} \text{ mW}$$

P_{CORE} = 18.7 mW

So

$$\Delta T = Rth \cdot \frac{P_{CU} + P_{CORE}}{1000} \text{°C}$$

$$\Delta T = \frac{50}{0.380} \cdot \frac{385 + 18.7}{1000} \text{°C}$$

ΔT = 53°C

because the vendor has stated that 380 mW dissipation in the inductor causes 50°C rise in temperature.

Extrapolated to our Application:

$$P'_{CU} = P_{CU} \cdot \frac{(12 \cdot I'^2_{DC} \cdot L^2) + Et'^2}{(12 \cdot I_{DC}^2 \cdot L^2) + Et^2} \text{ mW}$$

$$P'_{CU} = 385 \cdot \frac{(12 \cdot 1^2 \cdot 137^2) + 38^2}{(12 \cdot 0.99^2 \cdot 137^2) + 59.4^2} \text{ mW}$$

P'_{CU} = 389 mW

$$P'_{CORE} = P_{CORE} \cdot \left[\left(\frac{Et'}{Et} \right)^b \cdot \left(\frac{f'}{f} \right)^c \right] \text{mW}$$

$$P'_{CORE} = 18.7 \cdot \left[\left(\frac{38}{59.4} \right)^{2.7} \cdot \left(\frac{150000}{250000} \right)^{2.04} \right] \text{mW}$$

P'_{CORE} = 2 mW

So,

$$\Delta T' = \Delta T \cdot \left[\frac{P'_{CU} + P'_{CORE}}{P_{CU} + P_{CORE}} \right] \text{°C}$$

$$\Delta T' = 53 \cdot \left[\frac{389 + 2}{385 + 18.7} \right] \text{°C}$$

$\Delta T'$ = 51°C

which is considered to be acceptable in this application.

Conclusions

By the detailed selection procedure above, we can expect the selected inductor to work well for the given lower frequency application example. As mentioned earlier, we would have 'intuitively' thought that since the inductance and current rating is about what we need, if we lowered the frequency from 250 kHz to 150 kHz, the peak current and field would increase. But they actually decrease as we can now see. The reason being, that the inductor was designed for a higher Et in mind (59.4 Vμsecs vs. our 38 Vμsecs). As stated earlier, Et in effect, defines the regulator configuration itself, so we did not just lower the frequency, we actually went to an entirely different input-output voltage combination to what the inductor had been originally designed for. As we can now guess, the original inductor had been probably designed for a much higher applied voltage to what we subjected it to. But this was not obvious at first sight. The full procedure as given in *Figure 2* and *Table 2* is therefore necessary to avoid such 'errors of intuition'.

The data sheets of National's Simple Switchers also generally include simple nomograms and these are useful in most cases, but limit the selection to certain previously specified or custom built inductors and are also based on certain assumptions. In particular, there are many factors to consider when fixing a certain current ripple ratio 'r', which happens to be the key input in the process of selection an inductor. Nomograms are easy to use but assume a certain 'r' which may not be ideal for all purposes. In fact in the example discussed above, we did in fact select an inductance higher than what the nomograms may have recommended, because of output voltage ripple considerations.

In general, this Application Note should help in selecting a more optimum and readily available off-the-shelf inductor.

Appendix: Optimizing the Size of the Inductor

The size of the inductor is related to the energy handling capability required. The energy handling capability is $\frac{1}{2}*L*I_{PEAK}^2$. For a given application, if we reduce inductance, it seems that this would increase ΔI and thereby I_{PEAK}, which would cause the energy requirement to increase since it depends on square of current. However, a detailed calculation shows agin that reality is counterintuitive. The energy handling requirement is actually substantially *reduced* if the inductance is decreased. In terms of 'r', we can in fact write the energy handling capability as

$$e = \frac{I_O \bullet Et}{8} \bullet \left[r \bullet \left(\frac{2}{r} + 1 \right)^2 \right] \mu J$$

where 'r' is $\Delta I/I_O$ and Et is in Vμsecs.

For a given application, Et is fixed as is I_O, so the term in square brackets gives 'e' the shape shown in *Figure 3*. We can see that the energy handling requirement (size of inductor) decreases as 'r' increases (L decreasing). The best value is the 'knee' and so it is a good idea to target an 'r' of 30%–40%. No great improvement in the size of the inductor will take place by increasing 'r' much more than this, but the RMS current in the output cap, and also the RMS current in the input capacitor (especially for large duty cycles), will increase substantially. The absolute value of the RMS ripple current in the input capacitor is much higher than in the output capacitor, and the designer should watch out for the cost penalty on the input capacitor too! Refer to *Table 3* for the complete set of optimization equations expressed as a function of 'r'.

While optimizing, the following points need to be considered:

- For a given application, having defined input and output voltages and load current, Et is fixed as are D and I_O. So the only degree of freedom is in selecting the 'r'. The equations in *Table 3* are therefore written in terms of 'r'.
- *Table 3* provides the general equations required for optimization but also provides the values at an 'r' of 0.3 in the adjacent column as a benchmark. This is also equivalent to the 'flat top approximation' often used for quick estimates.
- *Figure 3* plots the variation of each parameter, normalized to the benchmark values (i.e., set to unity at an 'r' of 0.3).
- Note that when calculating dissipation in the switch, one must consider whether the switch is a bipolar transistor or a FET. If it is a FET, we need to apply I^2*R where I is the RMS switch current and R is the R_{DS} of the FET. If it is bipolar, we need to use V*I where V is the saturation voltage across the switch, and I is the average switch current. That is why both have been provided in *Table 3*. Also note that for a bipolar switch, the dissipation is seems almost independent of 'r'. In practice, the saturation voltage drop depends on the instantaneous value of current, so dissipation does increase slightly with 'r'.
- Referring to *Figure 3* we can see that the RMS inductor current hardly changes over a very wide range of 'r'. That is why, earlier in this Application Note, it was mentioned that for the purpose of evaluating copper losses we may use I_O^2 instead of I_{RMS}^2.
- The core losses also increase substantially with increasing 'r'. It can be shown that even if we keep the same core size, *the flux density B_{AC} will go up as $r^{1/2}$*. Going to a smaller core could increase this further.
- The RMS capacitor currents in the input and output are the main components to consider because they can increase rapidly with 'r'. So for example, if we increase 'r' to 0.6 (from 0.3), the energy handling requirement of the inductor falls by about 35% but the dissipation in the output capacitors (if ESR is unchanged) will increase by 400%! Alternatively stated, we now need to select an output capacitor with twice the ripple current rating.
- It must also be kept in mind that there is an output voltage ripple ΔV = ESR x ΔI associated with the current ripple. Now, the ESR of the output capacitor cannot usually be decreased below 100 mΩ–200 mΩ (with voltage mode control) for loop stability reasons. So for high loads (and high 'r'), the dissipation in the output capacitor will necessarily be high since we cannot reduce ESR further. This may call for physically large sized output capacitors to handle the dissipation. In addition, the output voltage ripple will be high too, and since we cannot reduce this by reducing the ESR, we will need to add on a post LC filter. So, for high load currents, it may become necessary to decrease 'r' substantially. This in turn will lead to a large inductor with slow transient response ability.

Appendix: Optimizing the Size of the Inductor (Continued)

- We have implied that the physical size of the inductor is related to its energy handling capability only. This in turn suggests that we are talking of inductor designs that are core-saturation limited. While this is usually true if the core material is a ferrite, it may not be true of some powdered iron inductors for example. The size of these may be limited not by core saturation but by core losses, which depend on flux swing, or ΔI, not I (or 'e'). So, while *Figure 3* is still valid, the criterion of 'best choice' may change. It may be necessary to choose or restrict 'r' to much smaller values than the 'knee'.

This completes the information required to optimize not only the inductor but the buck regulator itself. The key factor affecting cost/size of almost all the components is the current ripple ratio 'r' and this needs to be carefully optimized as discussed above.

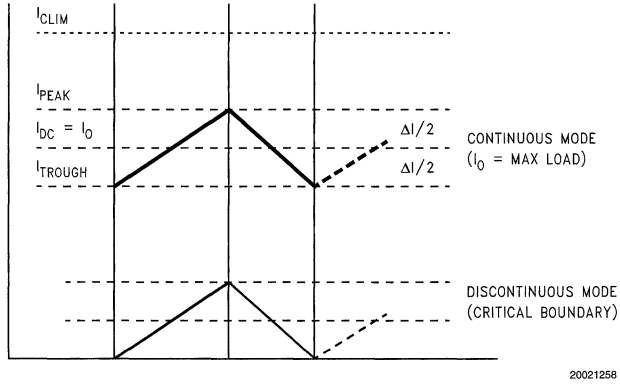


FIGURE 1. Inductor Current Waveform

TABLE 1. Specifications of Available Inductor

Part Number	Reference Values			Control Values	Calculation Data
	I_{DC} (Amps)	L_{DC} (µH)	Et (Vµsecs)	DCR (nom) mΩ	Et_{100} (Vµsecs)
P0150	0.99	137	59.4	387	10.12

Appendix: Optimizing the Size of the Inductor (Continued)

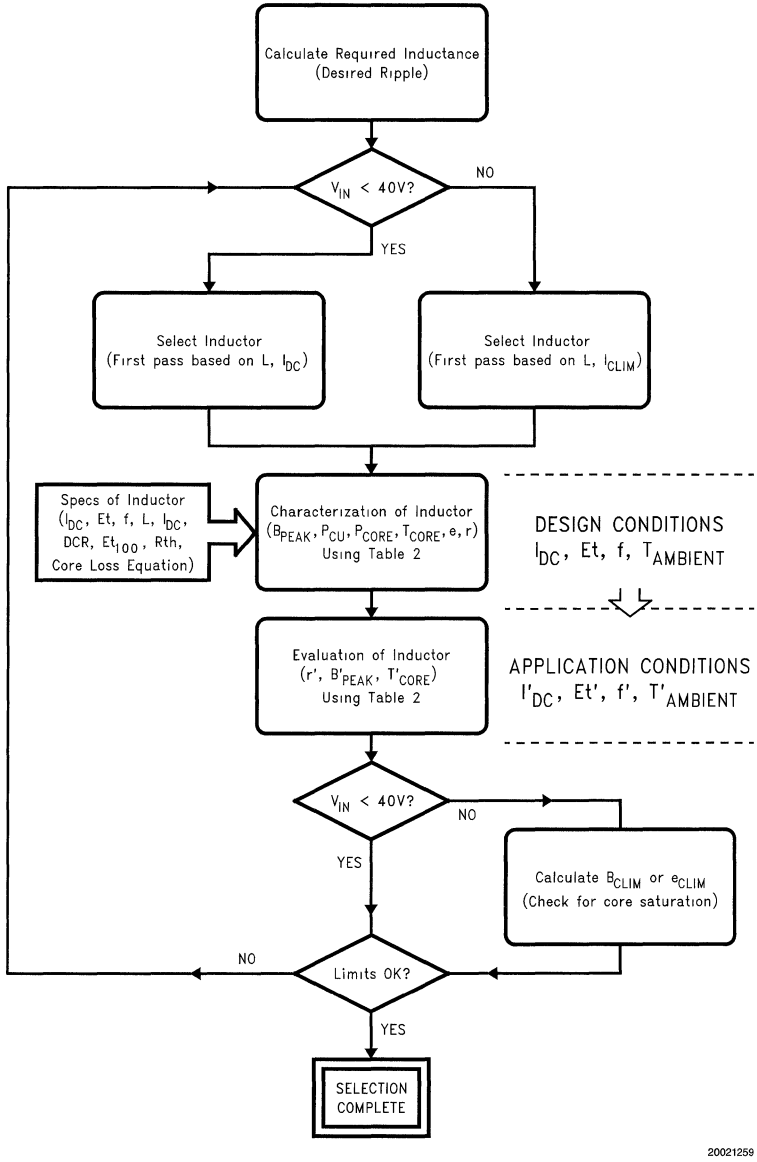


FIGURE 2. Design Flow Chart for Selection of Inductor

Appendix: Optimizing the Size of the Inductor (Continued)

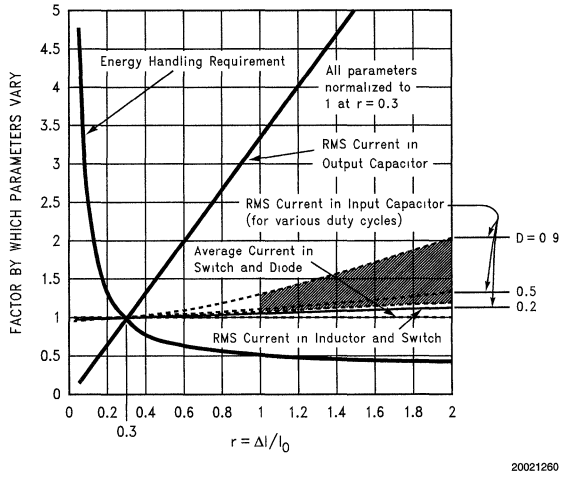


FIGURE 3. Optimization Chart for Setting 'r'

TABLE 2. Complete Design Table for Evaluating the Inductor for a Given Application

Design Parameters	Design Conditions I_{DC}, Et, f, $T_{AMBIENT}$	Application Conditions $I'_{DC} = I_O$, Et', f', $T'_{AMBIENT}$
AC Component of Current Amps	$\Delta I = \frac{Et}{L}$	$\Delta I' = \Delta I \cdot \left[\frac{Et'}{Et}\right]$
Current Ripple Ratio 'r' ($\Delta I/I_{DC}$)	$r = \frac{Et}{L \cdot I_{DC}}$	$r' = r \cdot \left[\frac{Et' \cdot I_{DC}}{Et \cdot I'_{DC}}\right]$
Peak Current in Inductor Amps	$I_{PEAK} = I_{DC} + \frac{Et}{2 \cdot L}$	$I'_{PEAK} = I_{PEAK} \cdot \left[\frac{(2 \cdot L \cdot I'_{DC}) + Et'}{(2 \cdot L \cdot I_{DC}) + Et}\right]$
RMS Current in Inductor Amps	$I_{RMS} = \sqrt{I_{DC}^2 + \frac{Et^2}{12 \cdot L^2}}$	$I'_{RMS} = I_{RMS} \cdot \left[\frac{(12 \cdot I'^2_{DC} \cdot L^2) + Et'^2}{(12 \cdot I^2_{DC} \cdot L^2) + Et^2}\right]^{1/2}$
AC Flux Density Gauss	$\Delta B = \frac{Et}{Et_{100}} \cdot 200 = \frac{100 \cdot Et}{N \cdot A_e}$	$\Delta B' = \Delta B \cdot \left[\frac{Et'}{Et}\right]$
Peak Flux Density Gauss	$B_{PEAK} = \frac{200}{Et_{100}} \cdot \left[(I_{DC} \cdot L) + \frac{Et}{2}\right]$	$B'_{PEAK} = B_{PEAK} \cdot \left[\frac{2 \cdot L \cdot I'_{DC} + Et'}{2 \cdot L \cdot I_{DC} + Et}\right]$
Copper Losses mW	$P_{CU} = DCR \cdot (I_{DC}^2 + \frac{Et^2}{12 \cdot L^2})$	$P'_{CU} = P_{CU} \cdot \frac{(12 \cdot I'^2_{DC} \cdot L^2) + Et'^2}{(12 \cdot I^2_{DC} \cdot L^2) + Et^2}$
Core Losses mW	$P_{CORE} = a \cdot [\frac{Et}{Et_{100}} \cdot 100]^b \cdot f^c$	$P'_{CORE} = P_{CORE} \cdot \left[\left(\frac{Et'}{Et}\right)^b \cdot \left(\frac{f'}{f}\right)^c\right]$
Energy in Core μJ	$e = \frac{1}{2} \cdot L \cdot [I_{DC} + \frac{Et}{2 \cdot L}]^2$	$e' = e \cdot \left[\frac{(2 \cdot L \cdot I'_{DC}) + Et'}{(2 \cdot L \cdot I_{DC}) + Et}\right]^2$

Appendix: Optimizing the Size of the Inductor (Continued)

TABLE 2. Complete Design Table for Evaluating the Inductor for a Given Application (Continued)

Design Parameters	Design Conditions I_{DC}, Et, f, $T_{AMBIENT}$	Application Conditions $I'_{DC} = I_O$, Et', f', $T'_{AMBIENT}$
Temperature Rise (ΔT) °C	$\Delta T = Rth \bullet \frac{P_{CU} + P_{CORE}}{1000}$	$\Delta T' = \Delta T \bullet \left[\frac{P'_{CU} + P'_{CORE}}{P_{CU} + P_{CORE}}\right]$

Et in Vμsecs, DCR in mΩ, L in μH, f in Hz, Effective Area Ae in cm^2, N is number of turns

TABLE 3. Optimization Table for Fixing Current Ripple Ratio 'r'

Parameters	As a Function of 'r'	For 'r' = 0.3 (to a first approximation)
Energy Handling Capability μJ	$\frac{I_O \bullet Et}{8} \bullet \left[r \bullet \left(\frac{2}{r} + 1\right)^2\right]$	$2.2 \bullet I_O \bullet Et$
RMS Current in Output Cap Amps	$I_O \bullet \frac{r}{\sqrt{12}}$	$0.09 \bullet I_O$
RMS Current in Input Cap Amps	$I_O \bullet \sqrt{D \bullet \left[1 - D + \frac{r^2}{12}\right]}$	$I_O \bullet \sqrt{D \bullet (1 - D)}$
RMS Current in Inductor Amps	$I_O \bullet \sqrt{1 + \frac{r^2}{12}}$	I_O
RMS Current in Switch Amps	$I_O \bullet \sqrt{D \bullet \left[1 + \frac{r^2}{12}\right]}$	$I_O \bullet \sqrt{D}$
Average Current in Switch Amps	$I_O \bullet D$	$I_O \bullet D$
Average Current in Diode Amps	$I_O \bullet (1-D)$	$I_O \bullet (1-D)$

$r = \Delta I / I_O$, Et in Vμsecs

LM2623 Ratio Adaptive, Gated Oscillator Cookbook

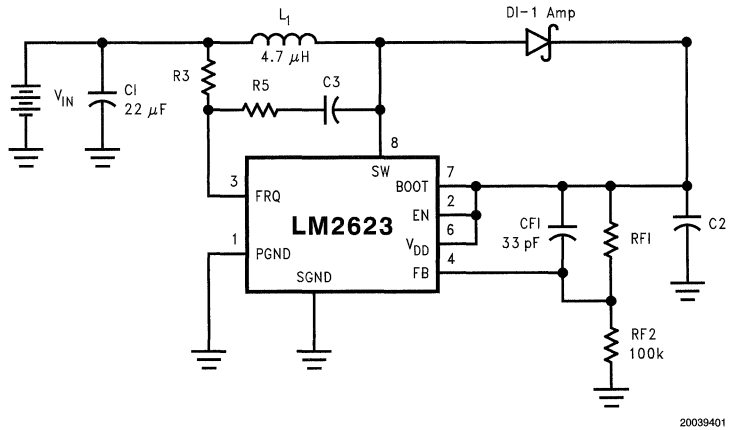
National Semiconductor
Application Note 1221
John Fairbanks

LM2623 General Purpose, Boost Converter Circuit

The next page shows the generic application circuit for LM2623 boost converters. The LM2623 boost converter circuits are very conventional, except for the ratio adaptive circuitry that is used to change the duty cycle. These components adjust the duty cycle to match it to the input/output voltage ratio requirements. R3 provides the drive current for the oscillator (frequency increases with lower resistance values). C3 and R5 provide the duty cycle adjustment. The default duty cycle when C3 and R5 are left out is about 17%. The value of C3 generally determines the total amount of charge transfer and resulting duty cycle adjustment. Smaller R3 values require larger C3 values (more charge transfer) to achieve the same duty cycle adjustment percentage. When more than 17% is necessary and it is not necessary to adjust the duty cycle dynamically (as the input to output voltage ratio changes), R5 can be omitted. Adding R5 allows the duty cycle to change as the input to output voltage ratio changes due to the battery discharging in portable applications. In applications where the fresh or fully charged battery voltage is close to the output voltage (2 cells generating 3.3V), the optimum duty cycle changes dramatically as the battery discharges. Use of the correct R5 in these situations will optimize the duty cycle for the voltage ratio and minimize the ripple due to overshoot caused by stored energy in the coil.

The table of values below the application circuit on the next page should produce good performance for the application requirements stated. Recommended inductor values are based on input voltage, load current and operating frequency. 4.7 µH works well in most LM2623 two cell applications. 6.8 µH works well in most LM2623 LiIon or three cell applications. RF1 and RF2 set the output voltage by dividing the output voltage for comparison to the reference at the pin 4 FB pin. CF1 couples the AC ripple from the output directly into the comparator at pin 4. When in regulation, this triggers the regulation limit each switching cycle. Triggering this limit allows the comparator to make the voltage comparison from the same direction (above the limit) each switching cycle. This minimizes the hysteretic component of ripple. A 68 µF or larger output capacitor is recommended to minimize ripple resulting from overshoot due to stored energy in the coil. The rectifier diode should be selected as a function of peak currents and efficiency requirements.

LM2623 Boost Converter Circuit
Typical Applications
Digital Cameras



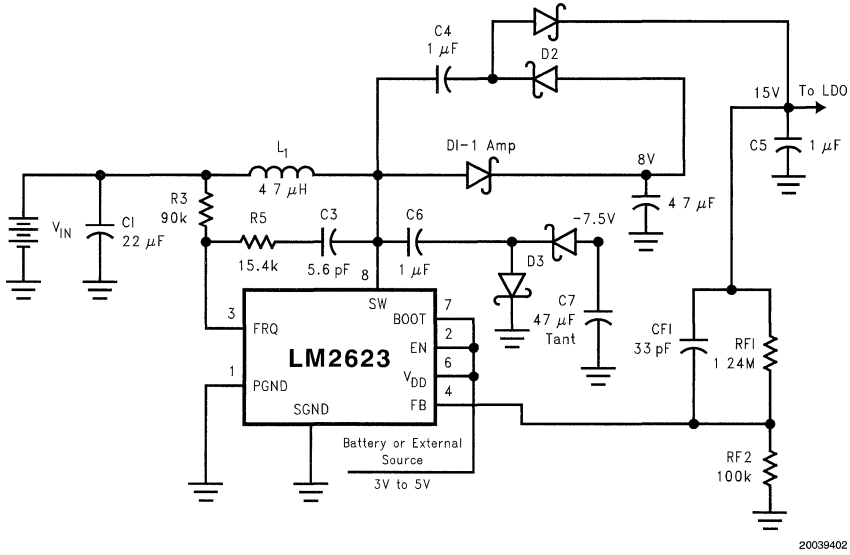
V_{IN}	Load Type	V_{OUT}	RFI	R3	R5	C3	C2
2 Cells	Analog/Digital	3.6V	182k	90k	35k	3.3 pF	100 µF Tant + 4.7 µF Cer
2 Cells	Motor Drive	5V	300k	90k	22k	4.7 pF	68 µF Tant
3 Cells or Li I	Motor Drive	5V	300k	150k	35k	4.7 pF	68 µF Tant

Dual Output Supply for CCD/LCD from 2 Cell Input

This supply begins with a general purpose, 8V, boost converter circuit Conventional, plus and minus doubler circuits are then added to generate a regulated 16V and a tracking, negative supply (nominally −7 5V) Since the −7.5V supply tracks but is not regulated, a large capacitor (47 µF) is required to keep the voltage close to a regulated value. The 16V supply is regulated, so a smaller capacitor value (1 µF) can be used. Dual SOT-23 diode packages are recommended to minimize component count in the doubler circuits. Losses in the primary 8V stage are reflected in both the 16V and −7.5V outputs, so a one amp schottky and 4.7 µF capacitor are recommended here. The V_{DD} supply on the IC can run off the 8V output or be supplied externally from a minimum 3V source.

The circuit as shown will put out about 800 mW. Conversion efficiency of the 8V primary stage is typically over 80% for nominal loads. Efficiency of the final output stages will be in the low to mid 70s for nominal loads. In typical applications, the 16V usually goes through an LDO to satisfy the very low ripple requirements of the CCD. The −7.5V supply may also need to be followed by a linear regulator or filter to be used for CCDs.

LM2623 Dual Output Converter Circuit
Typical Applications
Digital Cameras CCD/LCD Supply

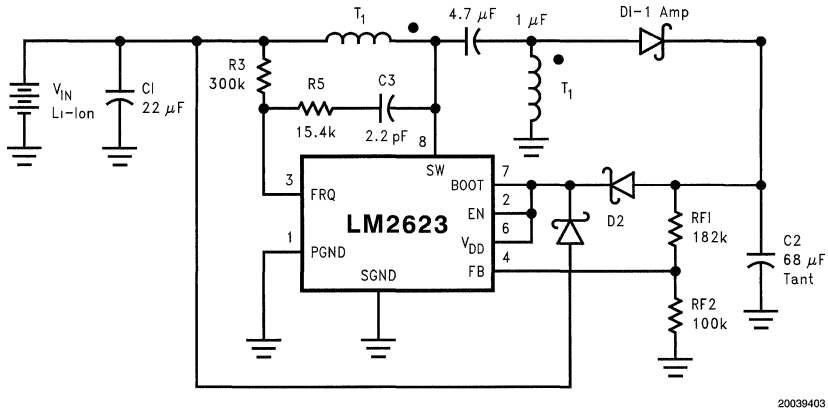


Transformer Coupled, (SEPIC) Converter for LI-ION or 3 Cell Input

Transformer coupled solutions are commonly used in cases where multiple output voltages are required. The application shown below uses a single output winding to obtain 3.3V. Because of the inherent stability of the on/off control system in the LM2623, the control portion of the circuit does not need to change when multiple output windings are added. The circuit shown is a generic example for generating any number of outputs from a single Lithium-Ion cell, as long as the 3.3V output is used for regulation. Efficiencies of 75% to 80% can be obtained for generation of 3.3V with this circuit configuration.

LM2623 Sepic Circuit
Typical Applications
Digital Cameras

CTX 8-2



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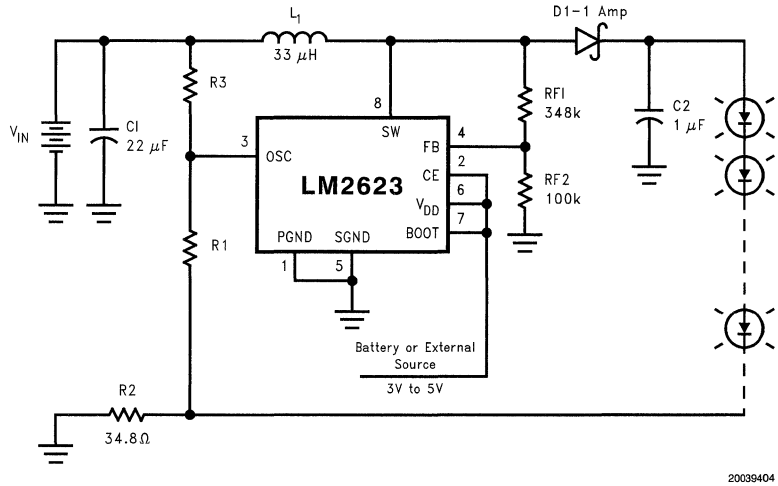
White Led Driver Application Circuits

Optimal drive circuits for LEDs require reasonable current regulation and very high efficiency. Since the human eye cannot detect small variations in light intensity, particularly when adjacent LEDs are driven with the same current, tight regulation tolerances used for processor voltage sources are not necessary. Most power supply ICs use 1.2V bandgap references and these are typically used to sense current for current source applications. The application circuit shown on the next page uses about .6V drop in series with LEDs to sense current. This reduces the losses in a 2 LED circuit by about 9% The LED current will usually be held within 10% for input voltage, temperature, LED voltage and IC process variations combined. Typical regulation is much closer than that.

The application circuit shown below is a balanced circuit that draws essentially constant power from the battery. Constant power with a constant voltage load results in constant current drive. The oscillator is supplied current through R3. R1 shunts current away from the oscillator pin through the current sense resistor, R2. The circuit is balanced when the voltage across R2 is approximately .6V. The balance is such that input voltage changes are offset by decreases in oscillator "on time". This results in constant power being drawn from the battery. Small current fluctuations change the voltage across R2 and increase or decrease the oscillator drive to compensate. This maintains the balance. The IC's change in frequency with temperature is very well matched to the change in LED voltage with temperature. This also helps to maintain the balance. The output pulse on the switch pin is voltage divided through RF1 and RF2 and triggers the regulation limit each time the switch pin swings positive. When the coil discharges its energy, the output voltage reduces and falls below the regulation limit. This turns the oscillator back on again and the supply goes through another switching cycle. Discharging the coil energy each cycle makes the off time vary in proportion to the on time. The power drawn from the battery is then linear with increases or decreases in on time (rather than varying as the "on time" squared). The circuit needs to be balanced with nominal parts in a given application. Once balanced, it should keep the current constant within 10% for voltage, temperature and part variations. Conversion efficiencies (neglecting the sensing resistor drop) will approach 90%. Over 80% of the input power is actually converted into power driving the LEDs for most input voltage and output loading conditions.

LM2623 White LED Driver Circuit



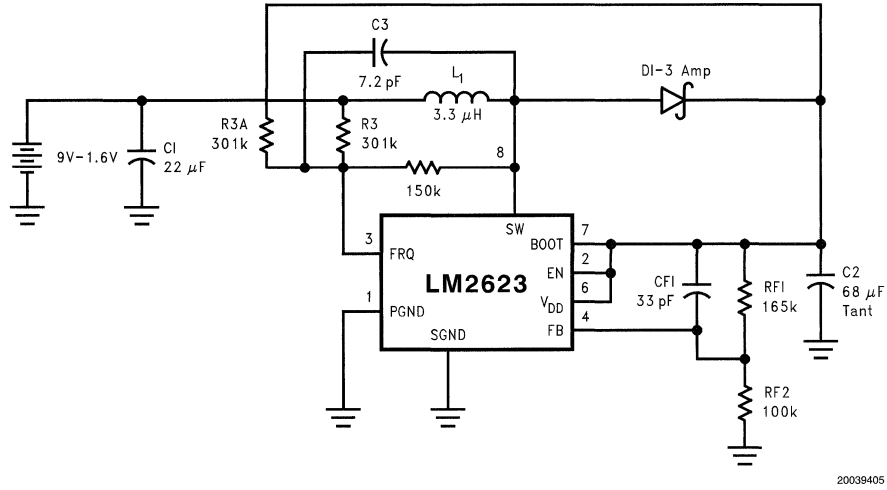
I_{OUT}	LED	V_{IN}	R1	R3	RF1
20 mA	2	3 Cell or Lil	900k	1M	348k
17	3	3 Cell or Lil	1.2M	1.2M	348k
18	2	2 Cells	845k	845k	348k
17.5	3	2 Cells	1.38M	1.33M	348k

Note For small changes in I_{OUT}, adjust R2 accordingly

Boost Converter for Single Cell Systems

The LM2623 has a guaranteed start-up voltage of 1.1V @ 25˚C. The start-up voltage is below the open circuit cell potential of NiCad and NiMH over the entire operating range (0 to 85˚C). This allows it to be used for single cell boost converters in rechargeable systems (NiCad and NiMH). Both the V_{DD} supply and the oscillator drive for the IC need to be "boot-strapped" from the output after the supply starts up to insure proper operation. Use of a 3 amp rectifier is recommended to minimize the voltage drop from input to output during start-up to a few millivolts. The addition of R3A drives the oscillator from the output voltage after the supply has started up. Using both R3 and R3A is necessary to allow the duty cycle to vary as the input voltage varies. Efficiencies of 75% to 80% are achievable for conversion from a single cell to 3.3V with the circuit shown.

LM2623 1 Cell Converter Circuit
Typical Applications
Pager or Digital Cameras



SIMPLE SWITCHER® PCB Layout Guidelines

National Semiconductor
Application Note 1229
Sanjaya Maniktala

Introduction

One problem with writing an Application Note on PCB layout is that the people who read it are usually not the ones who are going to use it Even if the designer has struggled through electromagnetic fields, EMC, EMI, board parasitics, transmission line effects, grounding, etc., he will in all probability then go on with his primary design task, leaving the layout to the CAD/layout person. Unfortunately, especially when it comes to switching regulators, it is not enough to be concerned with just basic routing/connectivity and mechanical issues. **Both the designer and the CAD person need to be aware that the design of a switching power converter is only as good as its layout.** Which probably explains why a great many of customer calls received, concerning switcher applications, are ultimately traced to poor layout practices. Sadly, these could and should have been avoided on the very first prototype board, saving time and money on all sides.

The overall subject of PCB design is an extremely wide one, embracing several test/mechanical/production issues and also in some cases compliance/regulatory issues. There is also a certain amount of physics/electromagnetics involved, if a clearer understanding is sought. But the purpose of this Application Note is to reach the audience most likely to use it Though there is enough design information for the more experienced designer/CAD person, the Application Note includes a quick-set of clear and concise basic rules that should be scrupulously followed to avoid a majority of problems. In particular, we have provided **recommended starting points for layout when using the popular LM267x, LM259x and LM257x families (Figure 2)** The focus is on the step-down (Buck) Simple Switcher ICs from National, but the same principles hold for any topology and switching power application.

Most of the issues discussed in this Note revolve around simply assuring the desired performance in terms of basic electrical functionality. Though luckily, as the beleaguered switcher designer will be happy to know, in general all the electrical aspects involved are related and point in the same general 'direction'. So for example, an 'ideal' layout, i.e. one which helps the IC function properly, also leads to reduced electromagnetic emissions, and vice-versa For example, reducing the area of loops with switching currents will help in terms of EMI and performance. However the designer is cautioned that there are some exceptions to this general 'trend'. One which is brought out in some detail here is the practice of 'copper-filling', which may help reduce parasitic inductances and reduce noise-induced IC problems, but can also increase EMI.

Quick-Set of Rules for SIMPLE SWITCHER PCB Layout (Buck)

a) Place the catch diode and input capacitor as shown in *Figure 2.*

b) For high-speed devices (e.g. LM267x) do not omit placing input decoupling/bypass ceramic capacitor (0.1 µF–0.47 µF) as in *Figure 2.*

c) Connect vias to a Ground plane if available (optional, marked 'X' in *Figure 2*)

d) If vias fall under tab of SMT power device, these are considered 'thermal vias'. Use correct dimensions as discussed to avoid production issues. Or place the vias close to but not directly under the tab.

e) Route feedback trace correctly as discussed, away from noise sources such as the inductor and the diode.

f) Do not increase width of copper on switching node injudiciously.

g) If very large heatsink area is required for catch diode (having estimated the heatsink requirement correctly) use isolation as discussed

h) For higher power SMT applications, use 2 oz board for better thermal management with less copper area.

Introduction (Continued)

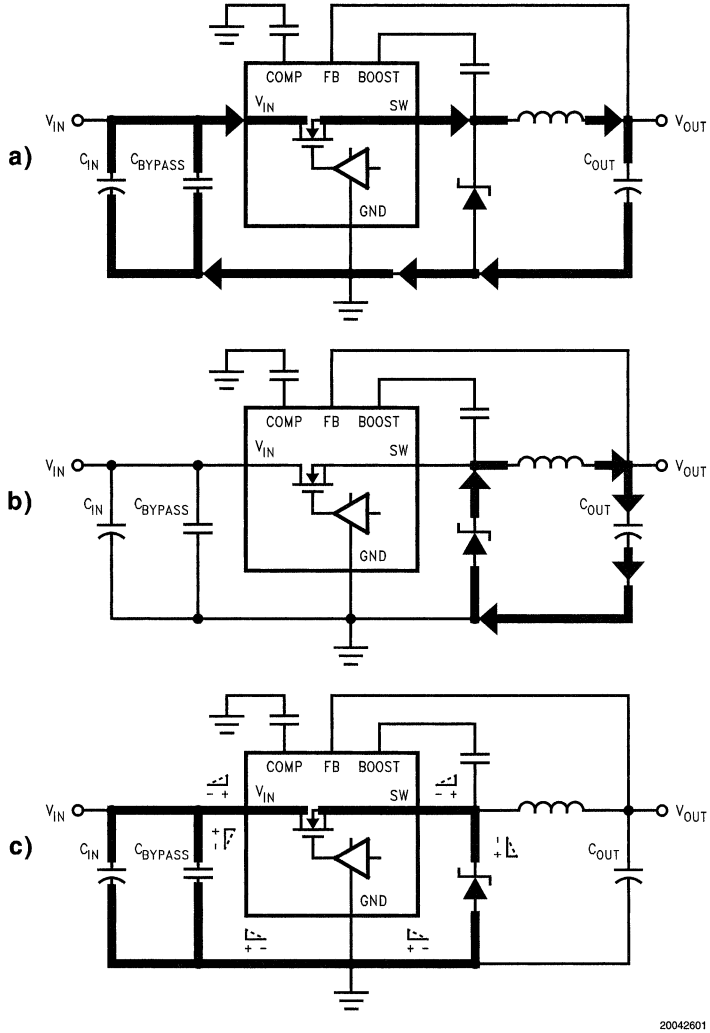


FIGURE 1.

The AC and DC Current Paths

Referring to *Figure 1a*, the bold lines represents the main (power) current flow in the converter during the time the switch is ON. As the switch turns ON, the edge of the of the current waveform is provided largely by CBYPASS, the remainder coming mainly from CIN. Some slower current components come from the input DC power supply (not shown) and also refresh these input caps. *Figure 1b* represents the situation when the switch is OFF. We can therefore see that in certain trace sections, current has to start flowing suddenly during the instant of switch turn-off and in some sections it needs to stop flowing equally suddenly. *Figure 1c* represents the 'difference', i.e. traces shown bold in this Figure are those where the current flow **changes suddenly**.

During the turn-on transition the picture reverses, but the 'difference' trace sections are the same. Therefore during either switch transition, 'step changes' of current take place in these difference sections. These traces encounter the harmonic-rich rising or trailing edges of the current pedestal waveform. The difference traces are considered 'critical' and deserve utmost attention during PCB layout. It is often stated colloquially, that 'AC current' flows in these trace sections, and 'DC current' in the others. The reason is that the basic switching PWM frequency forms only a fraction of the total harmonic (Fourier) content of the current waveform in the 'AC' traces. In comparison, where 'DC current' flows, the current does not change in a stepped fashion and so the harmonic content is lower. It is also no surprise that the DC

The AC and DC Current Paths

(Continued)

sections are those in series with the main inductor, because it is known that inductors have the property of preventing sudden changes in current (this is analogous to a capacitor which 'resists' sudden changes in voltage).

Summing up. **In switching regulator layout, it is the AC paths that are considered critical, whereas the DC paths are not. That is the only basic rule to be kept in mind, and from which all the others follow. This is also true for any topology.** Perform an analysis of the current flow for any topology in the same manner as we did for the Buck, to find the 'difference traces': and these traces are by defintion the 'critical' ones for layout.

What is the problem with step current changes anyway? In a resistor for example, this causes no unexpected/ unidentifiable problem. The voltage is given by V=IR, and so for a given change of current, the voltage will change proportionally. For example, a **0.5 cm wide Cu trace of thickness 1.4 mil has a resistance of 1milliohm per cm length** (at 20 degC). So it seems that a 1 inch long trace with a current changeover of 1A, would produce a change in voltage of only 2.5 millivolts across the trace, which is insignificant enough to cause the control sections of most ICs to misbehave. But in fact the induced voltage is much larger. The important thing to realize is that traces of copper on a PCB, though barely resistive, are also inductive. Now, the oft-repeated thumb-rule is that **'every inch of trace length has an inductance of about 20 nH'**. Like the trace resistance, that too doesn't seem much at first sight. But it is this rather minute inductance which is in fact responsible for a great many customer calls in SIMPLE SWITCHER applications!

The equation for voltage across an inductance is V=L*dI/dt, and so the voltage does not depend on the current but on the *rate* of change of the current. This fact makes all the difference when the 1A change we spoke about occurs within a very short time. The induced voltage can be very high, even for small inductances and currents, if the dI/dt is high. A high dI/dt event occurs during transition from *Figure 1a* to *Figure 1b* (and back) in all the AC trace sections (shown bold in *Figure 1c*). The induced voltage spike appears across each affected trace, lasting for the duration of the crossover.

To get a better feel for the numbers here: **the change in current in the AC sections of a typical buck converter is about 1.2 times the load current during the switch turn-off transition and is about 0.8 times the load current during the switch turn-on transition** (for an 'optimally' designed Buck inductor, as per inductor design guidelines in the relevant Datasheets/Selection Software). The transition time is about 30 ns for high speed Fet switchers like the LM267x, and is about 75 ns for the slower bipolar switchers like the LM259x series. This also incidentally means that the voltage spikes in the high-speed families can be more than twice that in the slower families, for a comparable layout and load. Therefore **layout becomes all the more critical in high-speed switchers**.

So, one inch of trace switching say 1A of instantaneous current in a transition time of 30 ns gives 0.7V, as compared to 2.5mV (that we estimated on the basis of resistance alone). For 3A, and two inches of trace, the induced voltage 'tries' to be 4V! In *Figure 1c*, the small triangles along the sections indicate the direction of the momentary induced voltage, as the converter changes from the situation in *Figure 1a* to that in *Figure 1b* (switch turn-off). We can see that assuming that the ground pin of the IC is the reference point, the switching node (marked 'SW') tries to go negative (all its series trace sections adding up). Similarly the input pin (marked 'VIN' goes high through series contributions in all its related sections. *Figure 1c* represents the picture during the turn-off transition During the turn-on transition all the induced voltage polarities shown are simply reversed. In that case, the VIN pin is dragged low, and the switching node pin is dragged high momentarily.

The astute designer will recognize that this was to be expected since any inductance, even if it is parasitic, demands to be 'reset', which means that the volt-seconds during the on-time must equal and be opposite in sign to the volt-seconds during the off-time.The designer will also realize that till these parasitic trace inductances reset, they do not 'allow' the crossover to occur. So for example, traces which were carrying current prior to switch turn-off will 'insist' on carrying current till the voltage spikes force them to do otherwise. Similarly, the traces which need to start carrying current will 'refuse' to do so till the spikes across them force them to do likewise. Since switching losses are proportional to crossover time, even if these voltage spikes do not cause anomalous behavior, they can degrade efficiency. For example, in transformer-based flyback regulators, when the the primary number of turns is much larger than the secondary turns, designers may be surprised to learn how much the secondary side trace inductances alone can degrade efficiency. This is because any **secondary side uncoupled (trace/transformer leakage) inductances reflect into the primary side as an equivalent parasitic inductance in series with the switch. This adds an additional term to the effective leakage as seen by the switch that equals the secondary inductance multiplied by square of the turns ratio** (turns ratio being Np/Ns). Therefore the dissipation in the flyback clamp (zener/RCD) can increase dramatically, lowering efficiency. One lesson here is that though 'leakage inductance' (from traces or the transformer) is considered 'uncoupled', in reality it can make its presence severely felt from one side of the transformer to the other. So it is not totally 'uncoupled' at all! In fact this happens to be the main reason why flybacks with low output voltages (high turns ratio) show poorer efficiency as compared to higher output flybacks. Therefore, reducing critical trace inductances is important for several reasons: efficiency, EMI, besides basic functionality.

The momentary voltage spikes which last for the duration of the transition can be very hard to capture on an oscilloscope. But they may be presumed to be present if the IC is seen to be misbehaving for no 'obvious reason'. These spikes, if present with sufficiently high amplitude, can propagate into the control sections of the IC causing what we call here a controller 'upset'. This leads to the observed performance anomalies, and in rare cases this can even cause device failure. Since none of these spike-related problems can be easily corrected, or band-aided, once the layout is initially bad, the important thing is to get the layout 'right' to start with.

The designer may well ask, why is it that these step current changes are a problem with the parasitic trace inductances, and not with the main inductor of the Buck converter? That is because all inductors try to resist any sudden current change. But since the main inductor has a much larger inductance (and energy storage) as compared to the parasitic trace inductances, it therefore ends up 'dominating'. From V*dt=L*dI we can also see that if L is large, a much higher voltseconds (V*dt) is required to cause a given

The AC and DC Current Paths

(Continued)

change in current. The trace inductances therefore simply 'give in' first before the main inductor does. But they certainly don't go down without a fight...and the voltage spikes bear testimony to this!

Notice that the currents in the signal traces in the schematic are not shown. For example those connected to the compensation node (marked 'COMP') or bootstrap (marked 'BOOST') carry relatively minute currents and therefore are not likely to cause upsets. They are therefore not critical and can be routed relatively 'carelessly'. The feedback trace is an exception, and will be discussed later. The Ground pin of the IC is another potential entry point of noise pickup. Inexperienced designers often grossly under estimate the needs of this pin, particulary for Buck converters. They assume that since the main power flow in a Buck converter does not pass through the ground pin, the 'current through the ground pin is very low', and therefore the trace length leading up to this pin is not critical. In fact, though the average current through this pin is very low, the peak current or its dI/dt is not. Consider the switch driver as shown schematically in *Figure 1*. Clearly it needs to supply current to drive the switch. In any Fet operated as a switch, large peak to peak instantaneous current spikes are needed to charge and discharge the gate capacitance. This is essential so as to cause the Fet to switch fast, and this reduces the switching/crossover losses inside the switch and improves the overall efficiency of the converter. (Actually, in a practical IC, the 'spike' of current comes from the bootstrap capacitor, and then the bootstrap capacitor is quickly refreshed by the internal circuitry of the IC ---- it is the refresh current that passes through the ground pin). Further, as in any high-speed digital IC, parts of the internal circuitry, clocks, gates, comparators etc., can turn on and off suddenly, leading to small but abrupt changes in the current through the ground pin. This can cause 'ground bounce' which in turn can lead to controller upsets. Therefore the length of the trace to the Ground pin also needs to be kept as small as possible. This also implies that **the input capacitors, especially the bypass capacitor 'CBYPASS' should be placed very close to the IC**, even for a Buck IC.

Placing Components 'acap' (as Close as Possible)

One has heard this before: "component X needs to be 'acap' ". Soon we are told the "component Y too needs to be 'acap' ". Then "Z too". And so on. Which would be physically impossible because matter cannot occupy the same place at the same time! So which one comes first? This is the million-dollar predicament always facing switcher layout.

The troubling trace lengths are those indicated *Figure 1c*. To keep them small, clearly two components need to be acap. These are the input bypass capacitor and also the catch diode. Consider the input capacitor section first.

In the schematic there are in two input capacitors shown. These are marked 'CIN' and 'CBYPASS' respectively. The purpose of the total input capacitance is to reduce the voltage variations at the input pin. The variations are mainly due to the pulsed input current waveshape, as demanded by a Buck topology. Note that for this particular topology, the output capacitor current is smooth (because the inductor is in series with it). In a Boost topology the situation is reversed: i.e. the input capacitor current is smooth and the current into the output capacitor is pulsed. This makes the demand for input decoupling less stringent than in a Buck (or Buck-Boost). In a Buck-Boost or 'flyback', both the input and the output capacitor currents are pulsed, and input decoupling is required not only for the control-section/drivers of the IC but for the input current step waveform of the power stage. Designers familiar with a Cuk topology know that in this case both input and output currents are smooth. The Cuk converter is therefore often called the 'ideal DC to DC' converter, and expectedly its parasitic inductances can be largely ignored ---- because there are no AC trace sections in the sense we described.

Now if the input power to a Buck converter was coming through long leads from a distant voltage source, the inductance of the incoming leads would seriously inhibit their ability to provide the fast changing pulsed current shape. So an on-board source of power is required right next to the converter, and this is provided by the input capacitor. It provides the pulsed current, and then is itself refreshed at a slower rate (DC current) from the distant voltage source.

However, since the input capacitor is fairly large in size, it may not be physically possible to place it as close as desired. Especially for very high speed switchers such as the LM267x series (note that a **'high speed' switcher as defined here, is one with a very small crossover/transition time, and it does not necessarily have to be one with a high switching frequency**). In addition, the Equivalent Series Resistance ('esr') and Equivalent Series Inductance ('esl') of the main input capacitor may be too high, and this can cause high frequency input voltage ripple on the VIN pin.

For the Buck converter schematic as shown in *Figure 1*, the input pin connects not only to the Drain of the Fet switch, but also provides a low internally regulated supply rail to the control sections of the IC. But no real series pass regulator can 'hold off' very fast changes in the applied input voltage. Some noise will feed through into the control section and then much will depend on the internal sensitivity of the IC to noise (related to its design, internal layout, process/logic family). It is therefore best to try to keep voltage on the VIN pin fairly clean ---- from a high frequency point of view. Note that it is not being suggested here that one responds to this statement by increasing the input capacitance indiscriminately, because we are not talking about the natural input voltage ripple which occurs at the rate of the switching frequency (e.g. 100 kHz–260 kHz). Our concern here is the noise occurring at the moment of the transitions, and this noise spectrum peaks at around 10 MHz–30 MHz, as determined by the transition/crossover time of the switch. The crossover time has nothing to do with the basic PWM switching frequency, but does of course depend on the type of switch used i.e. bipolar or Fet.

Therefore a high frequency 'bypass' or 'decoupling' capacitor with small or no leads, shown as 'CBYPASS' in *Figure 1*, is to be placed very close to the VIN and GND pins of the IC. This is usually a 0.1 µF–0.47 µF (monolithic) multilayer ceramic (typically X7R type, size 1206 or the more recent 'inverted' termination version of this popular size, the '0612' ---- also note that smaller sized ceramic caps generally have higher esr/esl, but check before use). Since now this component provides the main pulsed current waveshape, the bulk capacitor shown as 'CIN', may be moved slightly further up (about an inch) without any deleterious effect. For lighter loads, and if it is possible to place the input bulk capacitor very close to the IC, the high frequency bypass capacitor may sometimes be omitted. **But for high-speed switchers like the LM267x, the input ceramic bypass capacitor is considered almost mandatory for any application.**

Placing Components 'acap' (as Close as Possible) (Continued)

The position of the catch diode is also critical It too needs to be acap. Now, every topology has a node called the 'switching node'. This is the 'hot' or 'swinging' end of the switch. For integrated switchers, this node can also be an easy entry point for noise feed-through into the control sections. Note that the problem is not caused by the simple fact that the voltage at this node swings, for it is designed for exactly that situation in mind. The problem is with the additional noise spikes riding on top of the basic square voltage waveform, arising from the trace inductances as explained earlier. Therefore, **it is essential to place the catch diode very close to the IC and connect it directly to the SW pin and GND pins of the IC, with traces that are very short and fairly wide** In some erroneous layouts, where the catch diode was not appropriately placed to start with, the converter could be 'bandaided' by a small series RC snubber. This consists typically of **a resistor (low inductive type preferred) of value 10Ω–100Ω and a capacitor, which should be ceramic of value 470 pF–2.2 nF.** Larger capacitance than this would lead to unacceptably higher dissipation ($=1/2*C*V^2*f$), chiefly in the resistor, and would serve no additional purpose. However, note that this **RC snubber needs to be placed very close to and across the Switching pin and Gnd pin of the IC, with short leads/traces.** Sometimes designers think that this is 'across the diode', because on the schematic there is no way to tell the difference. However, particularly when the diode is a Schottky, the primary purpose of such a snubber is to absorb the voltage spikes of the trace inductances. Therefore its position must be such that it provides bypassing of the critical or AC trace sections of the output side as shown in *Figure 1c* (right hand side of the switcher) ----which means it must be close to the IC. Of course, as mentioned previously, it is best to get the layout right to start with, rather than adding such extra components.

Remaining component placements can be taken up only after the input bypass capacitor and the catch diode are firmly in place and are both acap. The traces to either of these two components should be short, fairy wide, and should not go pass through any vias on the way to the IC. For SMT boards this implies that the input capacitor and catch diode are on the same layer as the IC. **In *Figure 2* suggested PCB starting points are provided for several switchers.** All of them focus on placing these two critical components correctly. These layouts are strongly recommended for most applications. **The 'X' marks suggest the recommended location where vias can be used to connect to a Ground Plane (if present).**The remaining components can be placed relatively carelessly (though in doing so, there may be slight impact, for example on the accuracy of the output voltage rail and its ripple, but nothing compared to what can happen if the input decoupling cap and catch diode are incorrectly placed). Trace routing is now discussed in more detail.

Placing Components 'acap' (as Close as Possible) (Continued)

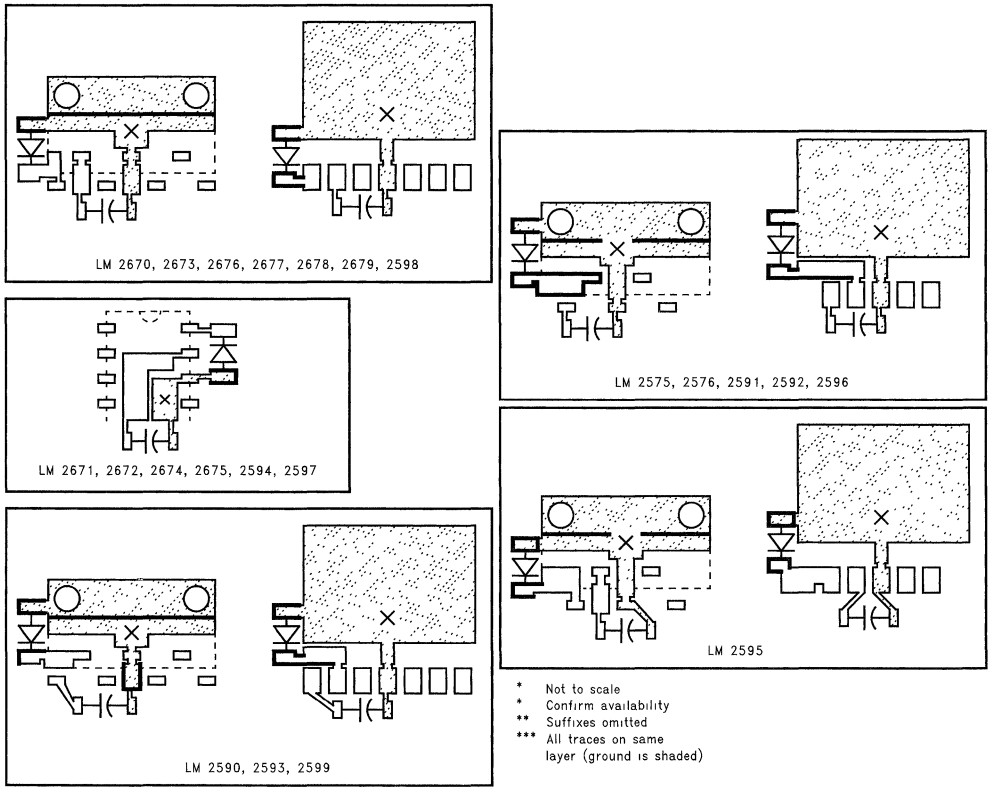


FIGURE 2. Recommended Layout Starting Points

Routing the Traces

As mentioned above, it is not advisable to route any of the critical traces through 'vias'. Vias are considered useful from a purely CAD perspective for 'layer jumping', but are often used indiscriminately as they seem an easy solution to connectivity problems. But they also add impedance, and that is exactly what we are trying to avoid. The inductance of a via is given by

$$L = \frac{h}{5}\left(1 + \ln\frac{4h}{d}\right) nH$$

where 'h' is the height of the via in mm (equal to the thickness of the board, commonly 1.6 mm), and 'd' is the diameter in mm. Therefore a single via of diameter 0.4 mm on a standard 1.6 mm board gives an inductance of 1.2 nH. It may not sound much, but it is almost twice that of a wire of the same length and diameter. **It has been seen empirically that for the high speed LM267x series, if the bypass capacitor is connected through vias to the IC, occasional field problems do arise.**So if vias have to be used for some reason, **several vias in parallel will yield better results than a single via. And larger via diameters would help further (unless they are being used as 'thermal vias'** --- discussed later).

It is also said that "the traces also need to be 'wide' and 'short' ". The necessity of short traces is clearly understood, usually intuitively, by most engineers. In fact the thumbrule of '20 nH per inch' also implies that trace inductance is almost proportional to length. However, **a common 'intuitive' mistake is to assume that inductance is inversely proportional to the width of the trace**. So some engineers mistakenly 'add copper' lavishly to critical traces (though there are some other reasons why this may be being done, and these will be discussed later). A first approximation for the inductance of a conductor having length 'l' and diameter 'd' is

$$L = 2l \cdot \left(\ln\frac{4l}{d} - 0.75\right) nH$$

where l and d are in centimeters. Note that the equation for a PCB trace is not much different from that of a wire.

Routing the Traces (Continued)

$$L = 2l \cdot (\ln \frac{2l}{w} - 0.5 + 0.2235 \frac{w}{l}) \text{ nH}$$

where 'w' is the width of the trace. For PCB traces, L hardly depends on the thickness of the copper (1 oz or 2 oz board). Both the above equations are plotted in *Figure 3.* It will be seen that for a given length, a PCB trace of width 'x' has higher inductance than a wire of diameter 'x'. In fact **the width of a PCB trace has to be about 1.78 times the diameter of a wire for the same inductance**.

A wire of AWG 20 has a diameter of 32 mils (or 0.081 cm). So for a length of one inch (1000 mils or 2.54 cm) L equals 21 nH (which is the usual thumbrule). We can see that L is almost proportional to length. But if we double the diameter to 0.16 cm, L equals 17 nH, which is not much different from 21 nH. This indicates a non-linear relationship. Referring to *Figure 3,* where the above function is plotted out (dotted lines are for a PCB trace), we can see that **the diameter/width of a wire/trace has to typically increase by a factor of 10 for the inductance to halve**. The relationship of L to d is therefore logarithmic in nature. The reason for this is the effects of mutual inductance between parallel sections/strips of the conductor.

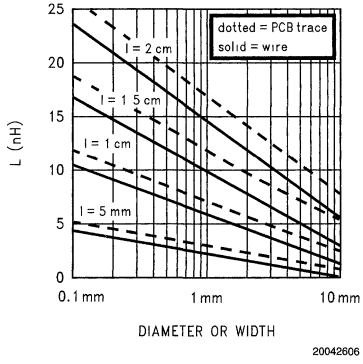


FIGURE 3. Inductance of Wire of Length 'l'

'Beefing up' traces to reduce the effects of parasitic inductances should be a last resort. **Decreasing the length of the trace should be the first step. Increasing the width of certain traces can in fact become counterproductive.** In particular, the trace from the switch node to the diode is 'hot' from an EMI point of view. This is not only because of the AC (high frequency) current it carries, but because of its voltage, which is a switched waveform. Any conductor with a varying voltage, irrespective of the current, becomes an antenna if its dimensions are large enough. Radiated emissions from this antenna can cause undesirable common-mode interference in its vicinity. Therefore this calls for the area of the copper around the switching node to be reduced, not increased. Large planes of switched voltage also cause capacitive noise coupling into nearby traces. On a typical SMT board, if the opposite side happens to be a 'ground plane', noise from the switching node can couple through the FR4 dielectric of the PCB into the Ground plane. No Ground plane is 'perfect', and therefore this injected high frequency noise can also cause the ground plane to not only radiate, but to pass noise onto the IC through 'ground bounce'. Some people suggest that a copper island, exactly the same size/shape as the switching-node island be created on the opposite side of the PCB, connected through several vias. This is supposed to prevent 'capacitive cross-talk' to other traces and to enhance thermal dissipation. But this obviously also leads to the breaking-up/partioning of the Ground plane. This defeats the very purpose of Ground plane as it can cause strange effects arising due to the odd current flow patterns in the now divided Ground plane. In general, **the Ground plane should be kept continuous/unbroken as far as possible, or it could behave like a slot antenna. For the switching node therefore, the best option is to keep the amount of copper around it to the actual minimum requirement.**

Some basic physics to be reminded of here: electric fields are caused by electric charge, and magnetic fields by currents. But if an electric field varies with time, it produces a corresponding magnetic field. However magnetic fields are associated with currents. Therefore AC voltages (varying electric fields) on opposite planes of copper on a PCB cause a 'displacement current' (capacitive coupling current) through the FR4 dielectric. Similarly, a varying magnetic field causes an electric field. So for example in a transformer, when we pass AC current (varying magnetic field) in a winding, we get Faraday induced voltages (electric field). Whenever voltage or current is switched, an electromagnetic field is generated, which produces EMI. And this EMI is inadvertently 'helped' by antenna structures. Therefore, on a PCB layout, **the area enclosed by all current loops carrying 'AC (switched) current' must be kept small. Similarly the area of copper planes with 'AC (switched) voltage' must be kept small. Both can behave as antennae. In addition, traces carrying switching currents/voltages must also be kept away from 'quieter' traces to avoid cross-coupling. Further, since 'sharp edges' are known to cause an increase in field strengths, two 45 degree bends in a trace are preferred to a single 90 degree bend.**

Copper Filling: when to Stop

Adding copper lavishly to traces serves some purpose occasionally, sometimes none at all, and sometimes it even works against the design in an unintended manner. There may be no simple hard and fast rules here. Judiciousness needs to be applied. But first it is instructive to consider some of the 'reasons' why copper is lavished, and to the degree it is really required. Most often the requirements are actually much less than predictions based on 'gut instinct':

We will take each of these separately:

A) CURRENT HANDLING CAPABILITY

If we multiply the width of a trace with its thickness we get the 'cross sectional area' of the conductor. This determines the resistance (per unit length) of the conductor and the consequent self-heating. This leads to an estimable temperature rise. It is important to note that the 'current handling capability' is therefore not a 'stake in the ground' as some people think, but is related to a permissible temperature rise.

Copper Filling: when to Stop

(Continued)

Mil Standards call for maximum 20°C rise, but 30°C–40°C are also common. *Figure 4* is a chart which helps in the correct estimation.

Current Density Curve for Outer Layer PCB Copper Etch

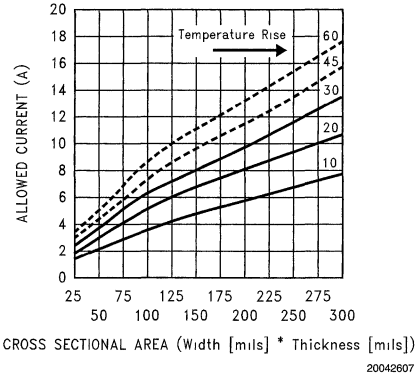


FIGURE 4. MIL-STD-275E Curves for Current Density vs. Temperature Rise

Commercial PCB's are often referred to as '1 oz' or '2 oz' for example. This refers to the weight of copper in ounces per square foot deposited on the copper clad laminate. **1 oz is actually equivalent to 1.4 mils copper thickness (or 35 µm). Similarly 2 oz is twice that**. We are only considering outer layers (not internal layers) in this Application Note, and therefore at most double-sided (2 layer) boards.

Using the thickness of the copper trace we can find the trace width required. For example for 1 oz copper board (1.4 mils copper thickness), and allowing 20°C rise in temperature, for 4A of current we need 75/1.4=54 mils (1.4 mm) wide trace. For a 2 oz board we need exactly half of that i.e. 0.7 mm width.

However note that a 1 oz double sided board will pass through an electroless copper plating process stage (before solder mask is applied) to create the vias (/PTH: Plated Through Hole), and so it may end up effectively as being considered closer to a 1.4 oz copper board. Therefore it is a good idea to check this out with the PCB manufacturer before even starting the layout. Also note that even a single-sided board passes through a hot air solder level finishing stage (after solder mask), where a thin Tin-Lead layer is deposited on the 'unmasked' (no solder mask) copper areas. This does increase the effective thickness of these traces, but doesn't help as much as copper plating, since Tin-Lead has 10 times higher resistivity than copper.

When estimating resistive heating, it is important to know the average current in the traces. For a Buck converter, in the AC traces of the input sections (the left hand side of the IC in *Figure 1c*) the average current is Io*D, where Io is the load current and D the duty cycle. For the AC traces of the output section (the right-hand side), the average current is Io*(1-D). So if the load current is 3A, and the duty cycle (≈Vo/Vin) is say 0.4, then the average current on the input side is 1.2A only On the output side it is 1.8A. In neither case is this equal to the load current of 3A! So the trace should be sized correctly and according to such a calculation.

Note that the expected temperature rise stated above is based on 'self-heating'. But a trace can become very hot simply due to heat from a nearby component. In that case, even a 30°C (additional) rise due to self-heating may be unacceptable. And the 'acceptable' rise also depends on worst-case ambient temperature, and also the rated temperature of the board laminate (keep below 120°C for FR4)

A quick thumb rule that closely follows the above discussion is:

For moderate temperature rise (less than 30°C) and currents less than 5A

- Use at least 12 mils width of copper per amp for 1 oz board
- Use at least 7 mils width of copper per amp for 2 oz board

B) TRACE INDUCTANCE

We have seen that the preferred method to reduce trace inductance is to reduce length, not increase width. Beyond a certain point, widening of traces does not reduce inductance significantly. Nor does it depend much on whether we use 1 oz or 2 oz boards. Neither does it depend on whether the trace is unmasked or not (to allow solder/copper to deposit and thereby increase effective conductor thickness). But if for some reason the length cannot be reduced, another way to reduce inductance is by paralleling of forward and return current traces.

Inductances exist because they can store magnetic energy. Therefore conversely, **if the magnetic field is somehow cancelled, the inductance too vanishes**. By paralleling two current traces, each carrying current of the same magnitude but in opposite direction on a PCB, the magnetic field is greatly reduced. These two traces should be parallel and very close. They can be run side-by-side on the same side for a single-sided board. If a double-sided PCB is being used, the most effective solution is to run the traces parallel and on opposite sides of the PCB. The traces can and should be fairly wide in this case to improve their mutual coupling and create the required field cancellation. Note that **if a ground plane is used on one side, the return automatically 'images' the forward current trace and produces field cancellation and reduction in inductance**.

The designer may well ask: what happens to the inductance equation for trace length we presented earlier? ---that didn't seem to indicate that paralleling should help. The problem with the simple trace inductance equation is that it is an approximation. **There is simply no such thing as an independent straight piece of wire carrying current in a given direction --- current must return and so there are only current loops**. This follows from basic Physics --- charge cannot accumulate and must return: in this case to the opposite terminal of the emf source responsible for the flow of current. So whenever we talk about the inductance of just a single wire, basically we are talking about a very large loop. Since inductance of a current carrying loop is proportional to the area enclosed by the loop, if the loop area is made very small, inductance too is reduced.

Copper Filling: when to Stop

(Continued)

C) THERMAL MANAGEMENT

Natural convection depends on the amount of surface area that is in contact with the air. If a conductive plate serving as a 'heatsink' is thick enough to ensure perfect thermal conduction into the far recesses of the plate, the temperature rise would have been simply inversely proportional to the total exposed area. PCB copper planes too are in that sense an aid to convection, the difference being that they are not thick enough to ensure perfect conduction. Therefore at some point, we will reach a point of diminishing returns: very large increases in the copper area will produce smaller and smaller improvement in the thermal resistance. This occurs roughly for a square of side 1 inch on a 1 oz copper board. Some improvement continues till about 3 inches, especially for 2 oz boards and better, but beyond that, external heatsinks are required. Ultimately, a reasonable practical value attainable for the thermal resistance (from the case of the power device to the ambient) is about 30˚C/W.

That is not to say that heat is lost only from the copper side. The usual laminate (board material) used for SMT applications is epoxy-glass 'FR4' (also known as GF or G10) which is a fairly good conductor of heat. More commercial and cost-effective applications use cheaper board materials like CEM1, CEM2, CEM3 etc., which are fortunately not much worse as thermal conductors than FR4. So some of the heat from the device side does get to the other side where it contacts the air. Therefore **putting a copper plane on the other side (this need not even be electrically the same node, it could be the ground plane) also helps, but only by about 10%–20% as compared to a copper plane on only one side. A much greater reduction of thermal resistance by about 50%–70% can be produced if 'thermal vias' are used to conduct heat to the other side.** This thermally 'shunts' or bypasses the board material to get the heat to the other side where there is more exposure to air movement.

The tab of the power packages of the Simple Switcher devices is fortunately at Ground potential, so having large copper planes around the tab will not produce EMI. The tab can be left floating, but if it is used, it must be physically connected directly to the GND pin of the IC as indicated in *Figure 2* If a double-sided board is used, several small vias can be sunk right next to the IC Ground in positions marked 'X' on to a 'Ground plane' on the other side of the PCB. These vias therefore not only help in the correct electrical implementation of grounding, but also can serve as thermal shunts. They are therefore appropriately called **'thermal vias'. It is recommended that they be small (0.3 mm–0.33 mm barrel diameter) so that the hole is essentially filled up during the plating process, thus aiding conduction to the other side. Too large a hole can cause 'solder wicking' problems during the reflow soldering process. The pitch (distance between the centers) of several such thermal vias in an area is typically 1 mm–1.2 mm and a grid of thermal vias can be created right under the tab.** Since the thermal vias also 'steal' heat away from the area during the reflow cycle, occasionally leading to poor solder joints, some recommend that vias (thermal or otherwise) should be close to, but never directly under the tab/legs/pins of any component.

From the point of view of the internal construction of a typical switcher IC, there is no reason to make the trace around the switching node wide since very little heat can come out this way. As mentioned earlier, this node can act as an antenna and cause radiation problems. However, there are situations where a large amount of copper on the switching node may just be unavoidable. The tab of most power diodes is the cathode. To sink heat from the diode, a large heatsink or copper plane must be connected to the tab. Unfortunately for a conventional positive to positive Buck topology (unlike the positive to positive Boost or the negative to positive Buck-Boost) the cathode/tab of the diode corresponds to the switching node, which is not 'quiet'. Therefore we have a conflict of interest here between thermal requirements and EMI. For EMI-sensitive applications, a rather non-typical diode with the anode internally connected to the tab can be sought. Or, if an external heatsink is being used, it is recommended that there be electrical (not thermal!) isolation between the power device and the (grounded) heatsink. Mica or 'Sil-pads' are possible choices here. If the diode must be SMT, an isolated SMT package may be a good choice.

Overestimating the amount of the copper plane for device cooling is a common mistake, and can lead to excessive EMI. **The heating in a Buck converter diode is based on the average current through the diode, not the load current.** Note that a typical Schottky diode has a forward voltage drop of 0.5V. If the load current is 5A and the duty cycle is 0.4, the dissipation is only 5*0.5*(1–0.4)=1.5W. If the temperature of the board (the copper area around the tab) is to be say a maximum of 100˚C, and the maximum ambient is 55˚C, the allowed temperature rise here is 100–55=45˚C. For 1.5W of estimated dissipation, the required board (or case) to ambient thermal resistance is 45/1.5=30˚C/W. This as we have seen is achievable on a PCB. To calculate the required area, **we can use as a good approximation an equation derived from empirical equations for a plate of area 'A'**:

$A = 985 \times Rth^{-1.43} \times P^{-0.28}$ sq.inches

Here P is in Watts and Rth is the required thermal resistance in ˚C/W. Solving for our example

$A = 985 \times 30^{-1.43} \times 1.5^{-0.28}$ sq.inches

A = 6.79 sq.inches

If this area is square in shape, the length of each side needs to be $6.79^{0.5} = 2.6$ inches. **If the area called for exceeds 1 sq inch, a 2 oz board should be used.** Clearly a 2 oz board should be used in the example, as it reduces the thermal 'constriction' around the power device and allows the large copper area to be more effectively used for convection. Note that we are considering only a copper plane exposed to air on one side of the PCB. Breaking up the Ground plane to create islands on the other side to connect to was not considered a good option as it leads to odd return current patterns.

The Ground Plane

With double-sided boards, it is a common practice to almost completely fill one side with ground. There are people who usually rightly so consider this a panacea or 'silver bullet' for most problems. As we have seen, every signal has a return, and as its harmonics get higher, the return 'wants' to be directly under the signal path, thus leading to field cancellation, and reduction of inductance. It also helps thermal management as it couples some of the heat produced by power devices on one side of the board to the other side. The Ground plane also capacitively links to noisy traces above it, causing some 'softening' of transients and thereby some reduction in noise/EMI ---**unless the cross-coupling is so severe as to start causing the Ground plane itself to**

The Ground Plane (Continued)

radiate. Vias can be sunk under the ground terminal of all power components in to the Ground plane, and this reduces DC resistance offset errors on the output voltage too for example. As mentioned, in *Figure 2*, 'X' marks have been placed to indicate that if there is a double sided board in use, and a Ground plane is present, then vias can be added at these points. They are optional, and so if a low cost single-sided board is preferred, they can be omitted. But if these vias are also doubling over as 'thermal vias' for the switcher IC, as when they are under the tab of an SMT power device, they should be sized appropriately as previously discussed.

However, a Ground plane should be an 'add-on' to the recommendations in *Figure 2*. It does not substitute the correct placement of the two critical components. Much effort should go into not breaking or partitioning this plane. Further, in general, if too much switching power flow occurs through such a plane, it can create 'ground bounce' and cause controller upsets. Therefore in higher power applications, with the added luxury of multi-layer PCBs, separate signal and power ground planes are used. But for the lower power SIMPLE SWITCHER family, a single Ground plane is all that may be required. And if the layout is carried out conscientiously, keeping all the recommendations in mind, even a single-sided board should suffice.

Signal Traces: Feedback

The only critical signal trace is the feedback trace. First consider only the Adjustable versions of the Simple Switchers. One end of the trace connects to a low impedance node, which is the output rail or a resistive divider at the output. The other end connects to the feedback pin, which is the high impedance input of the error amplifier. If this trace picks up noise (capacitively or inductively) as it passes between these two nodes, it can lead to erroneous output voltages, and in extreme cases even instability or device failure. There seem to be just two options for this

1. Keep the feedback trace short if possible so as to minimize pickup AND/OR
2. Keep it away from noise sources (e.g. switching diode, inductor)

Keeping the trace short may not be feasible. In fact **the feedback trace may be deliberately kept slightly longer so as to route it away from potential noise sources. It should not pass under the inductor or diode in particular.** If a double-sided SMT board is being used, a good strategy is as follows:

- use a via at the output resistive divider to bring the trace to the other side
- run the trace to cut through the surrounding ground plane areas, taking care not to pass it under the inductor/diode and not parallel to any power trace on either side of the board (though it can cross them perpendicularly)
- and then very close to the IC, use another via to bring out the trace to the component side where it connects to the feedback pin of the IC

Refer to *Figure 5a* which shows the situation for the Adjustable part. The trace which picks up noise is bold. However, if we consider a fixed voltage part, we learn an important thing. This is *Figure 5b*. Note that the feedback trace here is not marked bold. The reason is that **a trace can pick up noise only if at least one end of it is a high impedance node**. In *Figure 5b*, the feedback pin goes to a resistive divider rather than directly to the input of the error amplifier. So it is relatively immune to noise pickup. The only section where noise can be picked up is inside the IC (shown bold), and this is a very short path. Applying the same principle to an Adjustable part provides another interesting way to route the feedback trace. One way is shown in *Figure 5c*. Here the length of the 'feedback trace' is very short, so it is relatively noise-free. The feedback resistors are physically close to the IC and the trace from the output to the upper resistor has low impedances on either side, and so does not pick up noise. However, the connection of the lower resistor to ground is not ideal as the resistive drop across the section marked 'Io*R' will affect the output voltage load regulation slightly. **Another way is in Figure 5d, and this resolves both issues. This is therefore recommended.** If a ground plane is used however, both *Figure 5c* and *Figure 5d* are actually the same if vias are correctly placed to couple into this plane. For *Figure 5d*, if possible, it is a good idea to run the top and bottom traces to the resistive divider parallel and close to each other, so as to minimize any further chance of noise pickup.

Signal Traces: Feedback (Continued)

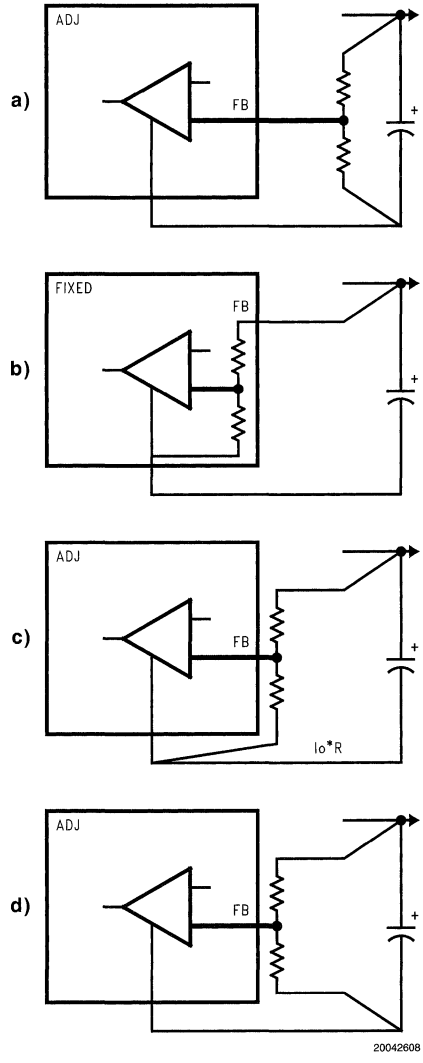


FIGURE 5. Feedback Traces (bold lines susceptible to noise)

Stresses in Wide Input DC-DC Converters

National Semiconductor
Application Note 1246
Sanjaya Maniktala

Introduction

Experienced power supply designers previously working with one topology who turn their attention to another, know they must shift mental gears quite dramatically. The "rules of the game" change and therefore major design issues will arise if this this fact is not recognized at the very outset.

"Equations for all topologies are available, and one just needs to use them"—correct? No, in fact though one of the things this Application Note also provides is such a set of design equations, that is not enough.

Equations are by nature "single-point" computations. So if for example we input a given operating condition: say V_{IN} = 15V, V_{OUT} = 5V, Io = 1A, we can use the appropriate Buck converter equation to calculate the input capacitor RMS current—valid for this specific condition. But under a more practical scenario suppose V_{IN} could vary between 8V and 22V, with 15V just representing a vague "nominal" value? What is then the most appropriate input voltage to use to calculate the worst-case input capacitor current? We will find that no set of equations, however complete, guides us to that information directly. So if Designer A "picks" the lowest input voltage 8V, Designer B picks the highest input voltage 22V, and Designer C picks the nominal value of 15V, all of them are actualy wrong. For the correct answer here is V_{IN} = 10V.

Take another example: should the inductor be designed at the highest input or the lowest input voltage of the range? For a Buck it didn't seem to matter too much at what input voltage we design the inductor, but if one applies the same nonchalance to a Boost or a Buck-Boost, there may be no power supply to put through any further testing.

The important point is even while delivering this constant maximum load, the internal currents of the power supply do change their shape, peak values, RMS and average values considerably in response to changes in input voltage. The purpose of this Note is to figure out how these values vary for each topology and to thereby fix a "worst case" design or test condition for each of them. A logical design procedure finally emerges based on the topology on hand.

As mentioned, a comprehensive table of design information (*Table 2*) is provided for all the three main topologies: the Buck, the Buck-Boost and the Boost. Unlike most other references in literature, this table is cast in terms of 'r'. This actually makes the table very designer-friendly because it recognizes that the only real degree of design freedom available is the inductor current ripple ratio 'r'. The criterion for selection of 'r' (in fact its actual value too) happens to be the same for any topology, at any application condition, and for any switching frequency. Once 'r' is fixed (usually between 0.3-0.5), everthing else is more or less predetermined. We only have to pay heed to the appropriate input voltage end at which to set 'r', as this can change from one topology to another. It will also be noticed that the design table includes the drops across the switch and diode for all the topologies, something that is not commonly available in related literature. We must realize that because of the ever-shrinking output voltages, these 'negligible' forward "drops" have actually become increasingly important today.

The design procedure based on the design table considers a power supply operating at a constant (maximum) load with a fixed output voltage, whose input voltage is varied. We can predict its response to the resulting variation in duty cycle, and thereby figure out the worst case input test or design condition. Conclusions are summarized in *Table 1*. The equations are essentially cast in terms of the output voltage (V_O), max load ("I_O") and Duty Cycle ("D"), and inductor current ripple ratio ("r"). The input voltage "V_{IN}" is not included directly in the stress formulae, as "D" is intended to reflect the input voltage variation. *The most important fact to keep in mind in this article when relating D to V_{IN} is that for all topologies, low D corresponds to high V_{IN} and a high D to low V_{IN}* (since output voltage is considered fixed).

Inductor Current Waveforms

An inductor current waveform consists of an AC/ramp component "ΔI", and a DC/average component "I_{DC}", the latter being the geometric center of the ramp. Note that in literature the 'AC' value is usually taken to be half the ramp, but here we are just equating them for convenience. The essential difference between the topologies is that for the Buck, the average inductor current equals the load current at all times, but for the Boost and the Buck-Boost, it is the average diode current that equals the load current. So as from *Table 2*, it can be shown that

$$I_{DC} = I_O = \text{constant} \quad \text{BUCK}$$

$$I_{DC} = \frac{I_O}{1 - D} \propto \frac{1}{1 - D} \quad \text{BOOST/BUCK-BOOST}$$

It is clear that the average inductor current for the Boost and the Buck-Boost becomes very high if D approaches 1. Remember that this corresponds to decreasing input voltage "V_{IN_MIN}". Therefore the inductor design must be conducted at the lowest input voltage for these topologies. For the Buck there is hardly any dependency of the inductor current to input voltage since the average current depends only on the load (which is considered fixed in our analysis). So for a Buck regulator, as a first pass selection, we often simply pick an inductor with a current rating equal to the load, irrespective of input voltage. These variations are included in the plots shown in *Figure 1*. Read these in consultation with the listing provided in *Table 1*.

Inductor Current Waveforms (Continued)

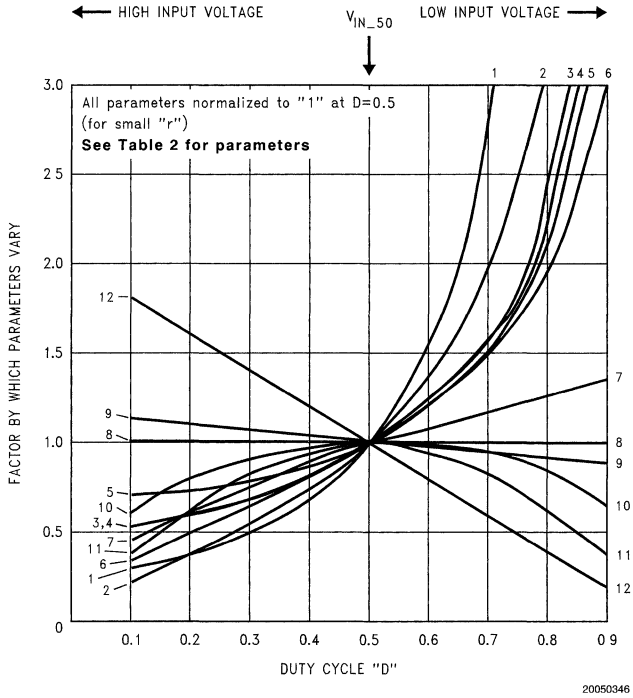


FIGURE 1.

TABLE 1. The Worst Input Voltage Condition for Design/Test of a Given Parameter

Parameter	Buck	Boost	Buck-Boost
ΔI (I_{AC} in Inductor)	V_{IN_MAX} 12	V_{IN_50} 11	V_{IN_MAX} 12
Core Loss	V_{IN_MAX}	V_{IN_50}	V_{IN_MAX}
Inductor Energy/Core Saturation	V_{IN_MAX}/V_{IN} 8	V_{IN_MIN} 1	V_{IN_MIN} 1
Average Current in Inductor	V_{IN} 8	V_{IN_MIN} 3	V_{IN_MIN} 3
RMS Current in Inductor	V_{IN_MAX}/V_{IN} 8	V_{IN_MIN} 3	V_{IN_MIN} 3
Copper Loss/Temperature of Inductor	V_{IN_MAX}/V_{IN}	V_{IN_MIN}	V_{IN_MIN}
RMS Current in Input Capacitor	V_{IN_50} 10	V_{IN_50} 11	V_{IN_MIN} 6
Input Voltage Ripple	V_{IN_MAX}/V_{IN} 8	V_{IN_MAX} 12	V_{IN_MIN} 3
RMS Current in Output Capacitor	V_{IN_MAX} 12	V_{IN_MIN} 6	V_{IN_MIN} 6
Output Voltage Ripple	V_{IN_MAX} 12	V_{IN_MIN} 3	V_{IN_MIN} 3
RMS Current in Switch	V_{IN_MIN} 7	V_{IN_MIN} 2	V_{IN_MIN} 2
Average Current in Switch	V_{IN_MIN}	V_{IN_MIN}	V_{IN_MIN}

Inductor Current Waveforms (Continued)

TABLE 1. The Worst Input Voltage Condition for Design/Test of a Given Parameter (Continued)

Parameter	Buck	Boost	Buck-Boost
Peak Current in Switch/Diode/Inductor	V_{IN_MAX} 9	V_{IN_MIN} 4	V_{IN_MIN} 5
Average Current in Diode	V_{IN_MAX} 12	V_{IN} 8	V_{IN} 8
Temperature of Diode	V_{IN_MAX} 12	V_{IN} 8	V_{IN} 8
Worst Case Efficiency	V_{IN_MAX}	V_{IN_MIN}	V_{IN_MIN}

Numbers in the columns refer to corresponding numbered curves in *Figure 1.*
V_{IN} means any input voltage is appropriate
V_{IN_50} is input voltage at which D=0 5

The AC component of the inductor current, "I_{AC}", or "ΔI" cannot be fully ignored even for a Buck. This parameter is important, firstly, because along with I_{DC}, it determines the peak value of the inductor current. This peak value needs to be known so as to accurately evaluate the energy handling requirement of the inductor (defined as $\frac{1}{2}*L*I^2_{PEAK}$). If we do not size the inductor accordingly, the core may saturate. But more importantly, for all topologies, this AC component is completely responsible for the core loss. Core loss does not depend on I_{DC}, so long as the inductor is not saturating).

Now, for all the topologies, there is an applied voltage "V_{ON}" across the inductor when the switch is ON. This causes a certain resulting AC ramp component "ΔI" across the inductor based on the fundamental equation $V_{ON} = L*\Delta I/(D/f)$ or $\Delta I = V_{ON}*D/(L*f)$, where f is the frequency. As the input voltage falls, V_{ON}decreases helping to lower the ramp component, but at the same time D increases and this helps to promote the ramp. So the interesting question can be asked: what eventually happens to ΔI as input voltage falls?

The equation for ΔI are provided in *Table 2.* We see that

$\Delta I \propto (1 - D)$ BUCK/BUCK-BOOST

$\Delta I \propto D\bullet(1 - D)$

So plotting these out in *Figure 1,* we see that

$\Delta I \rightarrow$ maximum at highest input voltage for Buck/Buck-Boost

$\Delta I \rightarrow$ maximum at V_{IN_50} (or closest voltage) for Boost

where V_{IN_50} is defined here as the input voltage at which D=50% for the topology under consideration. This value is also provided in *Table 2.* If the input voltage range does not include V_{IN_50}, we must choose either V_{IN_MIN} or V_{IN_MAX}, *whichever happens to be closer to* V_{IN_50}.

We also define a useful parameter called the current ripple ratio "r" which is the ratio of the AC to the DC value of the inductor current, with the converter delivering maximum load. So

$$r = \frac{\Delta I}{I_{DC}} = \frac{\Delta I}{I_O} \qquad \text{BUCK}$$

$$r = \frac{\Delta I}{I_{DC}} = \frac{\Delta I}{I_O} \cdot (1 - D) \qquad \text{BOOST/BUCK-BOOST}$$

This parameter "r" is important as it determines among other things, the inductance "L", and the physical size of most of the power components. It can be shown that the size of the inductor is reduced by increasing "r". However an "r" of 0.3–0.4 represents the most optimum choice for any topology. The reader can refer to AN-1197 for a deeper understanding of how the current ripple ratio relates to the optimization. That particular Application Note is based on the Buck converter, but the same principles apply to all the topologies. In any case, allowing for a greater current ripple than the optimum of 0.3-0.5 (by reducing inductance) does not appreciably reduce the size of the inductor, but does increase the size/requirements of either or both the input/output capacitors. Now, having designed the inductor for a given value of "r" at the appropriate input voltage end, as discussed earlier, as we vary the input voltage over the expected range, "r" changes accordingly. The equations in *Table 2* are cast essentially in terms of "r" and D, as these are the two main parameters that vary with input voltage. The variation of "r" with D is also provided, thus making D the only actual variable in our analysis. The value of the required inductance (based on a chosen "r") can be found in *Table 2,* and the physical size of this inductor can be also calculated from the required energy handling capability as listed. More on inductor design later.

Input Capacitor Currents

A key parameter is the RMS current, "I_{IN}", through the input electrolytic capacitor. It determines the basic/minimum selection criterion since the capacitor must be rated at least for the worst case RMS current that may pass through it. A capacitor operated with an RMS current higher than its rated value, is not guaranteed to have any specific life by most manufacturers. Life expectancy vs. temperature curves/equations as provided, are then not considered to be valid.

From *Table 2,* for small "r", we can see that this goes as

$$I_{IN} \propto \sqrt{D \cdot (1 - D)} \qquad \text{BUCK}$$

$$I_{IN} \propto \frac{r}{1 - D} \propto \frac{D \cdot (1 - D)^2}{1 - D} = D \cdot (1 - D) \qquad \text{BOOST}$$

$$I_{IN} \propto \frac{1}{(1 - D)} \cdot \sqrt{D \cdot (1 - D)} = \sqrt{\frac{D}{1 - D}} \qquad \text{BUCK-BOOST}$$

Plotting these out in *Figure 1,* we can see that

$I_{IN} \rightarrow$ maximum at V_{IN_50} (or closest voltage) for Buck/Boost

$I_{IN} \rightarrow$ maximum at lowest input voltage for Buck-Boost

So the temperature of the output capacitor must also be evaluated at the above input voltages. If the input voltage

Input Capacitor Currents (Continued)

range does not include V_{IN_50}, we must choose either V_{IN_MIN} or V_{IN_MAX}, *whichever happens to be closer to* V_{IN_50}.

We are also concerned with the peak to peak current, I_{PP_IN} through the input capacitor as this determines the input voltage ripple $\Delta V_{IN}=I_{PP\_IN}*ESR_{IN}$, where ESR_{IN} is the Equivalent Series Resistance of the input capacitor. This input ripple is a major component of the EMI spectrum at the input of the power supply.

From *Table 2*, for small "r", we can see that this goes as

$$I_{PP\_IN} \propto \text{constant} \quad \text{BUCK}$$

$$I_{PP\_IN} \propto \frac{r}{1-D} \propto \frac{(1-D)^2}{1-D} = (1-D) \quad \text{BOOST}$$

$$I_{PP\_IN} \propto \frac{1}{1-D} \quad \text{BUCK-BOOST}$$

Plotting these out in *Figure 1*, we can see that

$I_{PP\_IN} \rightarrow$ constant/maximum at highest input voltage for Buck

$I_{PP\_IN} \rightarrow$ maximum at highest input voltage for Boost

$I_{PP\_IN} \rightarrow$ maximum at lowest input voltage for Buck-Boost

For a Buck stage, the input voltage ripple is almost a constant with respect to input voltage variations, provided "r" is very small. However since "r" does increase somewhat at high input voltages, it is preferable to evaluate this parameter at the highest input voltage.

Output Capacitor Currents

The Output Capacitor also needs to be at least big enough to handle the worst case RMS current through it, "I_{OUT}".

From *Table 2*, for small "r", we can see that this goes as

$$I_{OUT} \propto r \propto (1-D) \quad \text{BUCK}$$

$$I_{OUT} \propto \sqrt{\frac{D}{1-D}} \quad \text{BOOST/BUCK-BOOST}$$

Plotting these out in *Figure 1*, we can see that

$I_{OUT} \rightarrow$ maximum at highest input voltage for Buck

$I_{OUT} \rightarrow$ maximum at lowest input voltage for Boost/Buck-Boost

So the temperature of the output capacitor must also be evaluated at the above input voltages.

We are also concerned with the peak to peak current, I_{PP_OUT} through the output capacitor as this determines the output voltage ripple $\Delta V_{OUT} = I_{PP\_OUT}*ESR_{OUT}$, where ESR_{OUT} is the Equivalent Series Resistance of the output capacitor. This output ripple is a major component of the noise spectrum at the output of the power supply.

From *Table 2*, for small "r", we can see that this goes as

$$I_{PP\_OUT} \propto r \propto (1-D) \quad \text{BUCK}$$

$$I_{PP\_OUT} \propto \frac{1}{1-D} \quad \text{BOOST/BUCK-BOOST}$$

Plotting these out in *Figure 1*, we can see that

$I_{PP\_OUT} \rightarrow$ maximum at highest input voltage for Buck

$I_{PP\_OUT} \rightarrow$ maximum at lowest input voltage for Boost/Buck-Boost

Switch RMS/Avg Current

For a MOSFET Switch we need to calculate the conduction loss as given by $I^2_{RMS}*rds$. The crossover losses are lowest at the minimum input voltage. But since they are usually a small fraction of the conduction losses, and are thus ignored here. The I_{RMS} of the switch varies in the following manner

From *Table 2*, for small "r", we can see that this goes as

$$I_{RMS} \propto \sqrt{D} \quad \text{BUCK}$$

$$I_{RMS} \propto \frac{\sqrt{D}}{1-D} \quad \text{BOOST/BUCK-BOOST}$$

Plotting these out in *Figure 1*, we can see that

$I_{RMS} \rightarrow$ maximum at lowest input voltage for Buck/Boost/Buck-Boost

It should however be noted that for a Buck, the dissipation in the Switch at low input voltages goes up only slightly, but for the remaining topologies, this dissipation is expected to go up steeply at low input voltages, leading to a large drop in efficiency. In *Table 2*, the average switch current is also provided, for calculation of dissipation in bipolar switches. It can be shown that the above conclusions for RMS are also valid for the average value of the switch current (which is required to calculate the conduction loss for a bipolar switch).

Talking about efficiency leads to the other main component of loss in a power supply, the diode loss. We will now see how this varies, and what it implies for the effect of input variations on the efficiency of the power supply.

Average Diode Current/Efficiency

For a diode we need to calculate the forward loss as given by $I_{AVG}*V_D$, where "V_D" is the drop across the diode when it conducts. For the Boost and the Buck-Boost, the average diode current is the load current, so it is not going to change with duty cycle. But for the Buck it does vary.

From *Table 2*, we can see that this goes as

$I_{AVG} \propto (1-D)$ BUCK

$I_{AVG} \propto$ constant BOOST/BUCK-BOOST

Plotting these out in *Figure 1*, we can see that

$I_{AVG} \rightarrow$ maximum at highest input voltage for Buck

$I_{AVG} \rightarrow$ constant for Boost/Buck-Boost

We saw that the dissipation in the switch of a Buck remains almost constant as input voltage increases, and now we see that the diode dissipation however increases as we do so. So we expect the efficiency of a Buck regulator to *fall at high input voltages on account of increased diode dissipation.* For the Boost and Buck-Boost, the diode dissipation does not change as input voltage falls, but the switch dissipation increases dramatically. So we expect the efficiency of a Boost or a Buck-Boost to *fall at low input voltages on account of increased switch dissipation* (unless crossover losses are very large, in which case the reverse is occasionally found to be true).

Average Diode Current/Efficiency

(Continued)

For diode temperatures, we need to test a Buck regulator at the highest input voltage. For the other topologies, it does not matter. This is shown as "V_{IN}" in *Table 1*, implying any input voltage.

This also tells us at what input voltage we need to check efficiency check of a power supply. It clearly varies from topology to topology. See *Table 1*.

Inductor Energy

The "Energy Handling Capability" is $e=\frac{1}{2}*L*I^2_{PEAK}$. This parameter literally "sizes" up the inductor for a given application. Note that the size is not determined just by inductance, since almost any inductance can be theoretically achieved on any core, simply by winding the appropriate number of turns on it. The complete equations for "e" are provided in *Table 2*. For our analysis here, we first make an approximation for the rather complicated term involving "r". Assuming "r" to be small this term becomes

$$r \cdot \left[\frac{2}{r} + 1\right]^2 \approx r \cdot \left[\frac{2}{r}\right]^2 \propto \frac{1}{r}$$

From *Table 2*, for small "r", we can see that the Energy handling Capability goes as

$$e \propto \frac{Et}{r} \propto \frac{(1 - D)}{(1 - D)} = 1 \quad \text{BUCK}$$

$$e \propto \frac{Et}{(1 - D) \cdot r} \propto \frac{D \cdot (1 - D)}{D \cdot (1 - D)^3} \propto \frac{1}{(1 - D)^2} \quad \text{BOOST}$$

$$e \propto \frac{Et}{(1 - D) \cdot r} \propto \frac{(1 - D)}{(1 - D)^3} \propto \frac{1}{(1 - D)^2} \quad \text{BUCK-BOOST}$$

Plotting these out in *Figure 1*, we can see that

$e \rightarrow$ constant/maximum at highest input voltage for Buck

$e \rightarrow$ maximum at lowest input voltage for Boost/Buck-Boost

Note that for both the Boost and the Buck-Boost, the required energy handling capability increases dramatically as duty cycle approaches 0.6. This is known to designers of front-end PFC stages. Such stages are typically of Boost topology, providing an internal 400VDC rail from a worldwide AC input. It is seen that the size of the required inductor goes up sharply as the minimum input voltage falls, and so the inductor design should be carried out at the minimum input voltage. As for the Buck, some designers use the maximum input voltage, some the minimum, and some simply use the nominal input voltage. It really does not matter too much, provided "r" is, and remains, small as we assumed. In reality, "r" does increase as input voltage increases (thereby causing a slight increase in peak value), so it is preferable to design the inductor of a buck regulator for the highest input voltage.

Inductor Avg/RMS Currents

If "r" is small, the average and RMS values of the inductor current are the same, "I_L". The copper loss in the inductor is I_L^2*R, where "R" is the winding resistance. The copper loss is usually very large compared to the core loss (which depends on ΔI, as discussed earlier), and largely determines the temperature rise of the inductor.

From *Table 2*, for small "r", we can see that the RMS/Avg current goes as

$$I_L \propto \text{constant} \quad \text{BUCK}$$

$$I_L \propto \frac{1}{(1 - D)} \quad \text{BOOST/BUCK-BOOST}$$

We can see that for the Boost and Buck-Boost, if D is large, I_L increases. Therefore when evaluating copper loss or temperature rise of the inductor for these, we need to use the minimum input voltage. For the Buck, since "r" does increase with increasing input voltage, the RMS value of the inductor current is also higher, and so we should use the maximum input voltage.

$I_L \rightarrow$ constant/maximum at highest input voltage for Buck

$I_L \rightarrow$ maximum at lowest input voltage for Boost/Buck-Boost

Peak Switch Current

This parameter is important because every controller has a current limit for the switch, and if the calculated peak exceeds the lowest value possible of the switch current limit, *anywhere in the input voltage range*, the required output power cannot be delivered. The peak current in a Buck is just a little higher than the load current, and so for example, the LM2593HV "Step Down (Buck) regulator" IC from National Semiconductor, which is designed for "2A load", has a minimum set value of 2.3A for the switch current limit. Yet, as seen in *Figure 2*, and from the datasheet of this device, this Buck IC can be operated as a "positive to negative" regulator, which is actually a standard Buck-Boost topology. In this mode, the peak current values are much higher, as can be seen from *Table 2*, and in fact depend not only on load, but on the duty cycle/input voltage too. We now try to see how the peak current values vary for all the topologies, with changes in input voltage.

From *Table 2*, for small "r", we can see that the peak current goes as

$$I_{PEAK} \propto \left[1 + \frac{r}{2}\right] \propto \left[2 + (1 - D)\right] = (3 - D) \quad \text{BUCK}$$

$$I_{PEAK} \propto \frac{\left[1 + \frac{r}{2}\right]}{1 - D} \propto \frac{\left[2 + (D \cdot (1 - D)^2)\right]}{1 - D} \quad \text{BOOST}$$

$$I_{PEAK} \propto \frac{\left[1 + \frac{r}{2}\right]}{1 - D} \propto \frac{\left[2 + (1 - D)^2\right]}{1 - D} \quad \text{BUCK-BOOST}$$

Plotting these in *Figure 1* we see that for the Boost and the Buck-Boost the peak value of switch current occurs at maxi-

Peak Switch Current (Continued)

mum duty cycle (minimum input voltage), whereas for the Buck this occurs at lowest duty cycle (highest input voltage). Therefore Current Limit must be tested at minimum input voltage for the Boost and the Buck-Boost, but for the Buck we must go to the highest input voltage. We conclude

$I_{PEAK} \rightarrow$ maximum at highest input voltage for Buck

$I_{PEAK} \rightarrow$ maximum at lowest input voltage for Boost/Buck-Boost

Therefore the designer can use *Table 2* to calculate the peak current, but must do so at the lowest input voltage for the Boost and Buck-Boost, to ensure that it is less than the current limit. For a Buck, the peak current must be calculated and compared to the current limit at the highest input voltage.

Example

The LM2593HV (5V fixed output version) is to be used to generate a −5V output from an input voltage ranging from 4.5V to 20V. This is a 150 kHz Buck Regulator IC with a switch current limit of 2.3A (min). What is the maximum load it can deliver in this positive to negative configuration. (Assume V_D = 0.5V and V_{SW} = 1.5V).

The inductor design must be done at the minimum input i.e. 4.5V for a Buck-Boost topology according to the guidelines in *Table 1*. We fix an "r" of 0.3 as this always represents an optimum size for the inductor. The worst-case peak current in the switch for a buck-boost (which this is) corresponds to the curve #5 from *Table 1*. Looking for this curve in *Figure 1* shows that this reaches its maximum at high duty cycle (low input voltage). Therefore we can proceed with this peak switch current calculation at the minimum input voltage, at which we will also perform the inductor design.

The duty cycle is calculated from *Table 2*

$$D = \frac{V_O + V_D}{V_{IN} + V_O - V_{SW} + V_D} = \frac{5 + 0.5}{4.5 + 5 - 1.5 + 0.5}$$

$D = 0.65$

The peak current in the switch is

$$I_{PEAK} = \frac{I_O}{1 - D} \cdot \left[1 + \frac{r}{2}\right]$$

So setting I_{PEAK} = 2.3A, we can solve for I_O

$$I_O = \frac{I_{PEAK} \cdot (1 - D)}{\left(1 + \frac{r}{2}\right)} = \frac{2.3 \cdot (1 - 0.65)}{\left(1 + \frac{0.3}{2}\right)}$$

$I_O = 0.7A$

So we can assure ourselves of only a maximum load of 0.7A in this configuration. The required L can be evaluated from *Table 2*

$$L = \frac{V_O + V_D}{I_O \cdot r \cdot f} \cdot (1 - D)^2 \cdot 10^6 \ \mu H$$

$$L = \frac{5 + 0.5}{0.7 \cdot 0.3 \cdot 150000} \cdot (1 - 0.65)^2 \cdot 10^6 \ \mu H$$

$L = 21.4\ \mu H$

This is the minimum inductance for the application If the inductance is higher than this, the calculated peak current may exceed the current limit of the device, causing foldback. Remaining parameters/ratings can be calculated in a similar way, by looking at *Table 2*, but using the guidelines from *Table 1*.

Note that if we want to estimate core losses in the inductor, which depends on the AC swing ΔI, this has a maximum at highest input voltage, not at minimum input voltage. So we would need to first set r = 0.3 at the lowest input voltage, then calculate the required inductance, and then finally to use the equations for ΔI, to calculate it at the highest input voltage. Basically "L" forms the required "bridge" to go from one voltage end to another, because once we fix its value, it remains so. Everything else can change.

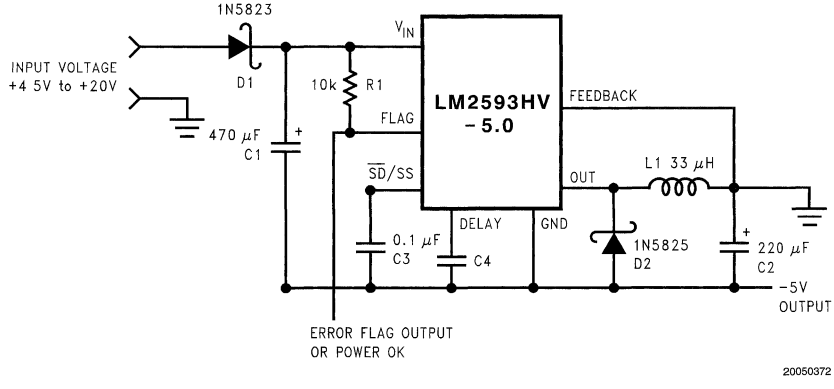


FIGURE 2. Buck Regulator IC Used in a Buck-Boost Application

Example (Continued)

TABLE 2. Design Table: r = $\Delta I/I_{DC}$, Et in Vμsecs, L in μH, f in Hz, All voltages and currents are magnitudes.

Parameter	Buck	Boost	Buck-Boost
Duty Cycle	$\frac{V_O + V_D}{V_{IN} - V_{SW} + V_D}$	$\frac{V_O - V_{IN} + V_D}{V_O - V_{SW} + V_D}$	$\frac{V_O + V_D}{V_{IN} + V_O - V_{SW} + V_D}$
V_{IN_50} *(V)*	$(2 \cdot V_O) + V_{SW} + V_D \approx 2 \cdot V_O$	$\frac{1}{2} \cdot \left[V_O + V_{SW} + V_D\right] \approx \frac{V_O}{2}$	$V_O + V_{SW} + V_D \approx V_O$
Output Voltage, V_O *(V)*	$V_{IN} \cdot D - V_{SW} \cdot D - V_D \cdot (1 - D)$	$\frac{V_{IN} - V_{SW} \cdot D - V_D \cdot (1 - D)}{1 - D}$	$\frac{V_{IN} \cdot D - V_{SW} \cdot D - V_D \cdot (1 - D)}{1 - D}$
Et *(Vμsec)*	$\frac{V_O + V_D}{f} \cdot (1 - D) \cdot 10^6$	$\frac{V_O - V_{SW} + V_D}{f} \cdot D \cdot (1 - D) \cdot 10^6$	$\frac{V_O + V_D}{f} \cdot (1 - D) \cdot 10^6$
L *(μH)*	$\frac{V_O + V_D}{I_O \cdot r \cdot f} \cdot (1 - D) \cdot 10^6$	$\frac{V_O - V_{SW} + V_D}{I_O \cdot r \cdot f} \cdot D \cdot (1 - D)^2 \cdot 10^6$	$\frac{V_O + V_D}{I_O \cdot r \cdot f} \cdot (1 - D)^2 \cdot 10^6$
"r"	$\frac{V_O + V_D}{I_O \cdot L \cdot f} \cdot (1 - D) \cdot 10^6$	$\frac{V_O - V_{SW} + V_D}{I_O \cdot L \cdot f} \cdot D \cdot (1 - D)^2 \cdot 10^6$	$\frac{V_O + V_D}{I_O \cdot L \cdot f} \cdot (1 - D)^2 \cdot 10^6$
ΔI *(A)*	$\frac{V_O + V_D}{L \cdot f} \cdot (1 - D) \cdot 10^6$	$\frac{V_O - V_{SW} + V_D}{L \cdot f} \cdot D \cdot (1 - D) \cdot 10^6$	$\frac{V_O + V_D}{L \cdot f} \cdot (1 - D) \cdot 10^6$
RMS Current in Input Cap *(A)*	$I_O \cdot \sqrt{D \cdot \left[1 - D + \frac{r^2}{12}\right]}$	$\frac{I_O}{1 - D} \cdot \frac{r}{\sqrt{12}}$	$\frac{I_O}{1 - D} \cdot \sqrt{D \cdot \left[1 - D + \frac{r^2}{12}\right]}$
I_{PP} in Input Capacitor *(A)*	$I_O \cdot \left[1 + \frac{r}{2}\right]$	$\frac{I_O \cdot r}{1 - D}$	$\frac{I_O}{1 - D} \cdot \left[1 + \frac{r}{2}\right]$
RMS Current in Output Cap *(A)*	$I_O \cdot \frac{r}{\sqrt{12}}$	$I_O \cdot \sqrt{\frac{D + \frac{r^2}{12}}{1 - D}}$	$I_O \cdot \sqrt{\frac{D + \frac{r^2}{12}}{1 - D}}$
I_{PP} in Output Capacitor *(A)*	$I_O \cdot r$	$\frac{I_O}{1 - D} \cdot \left[1 + \frac{r}{2}\right]$	$\frac{I_O}{1 - D} \cdot \left[1 + \frac{r}{2}\right]$
Energy Handling Capability *(μJoules)*	$\frac{I_O \cdot Et}{8} \cdot \left[r \cdot \left(\frac{2}{r} + 1\right)^2\right]$	$\frac{I_O \cdot Et}{8 \cdot (1 - D)} \cdot \left[r \cdot \left(\frac{2}{r} + 1\right)^2\right]$	$\frac{I_O \cdot Et}{8 \cdot (1 - D)} \cdot \left[r \cdot \left(\frac{2}{r} + 1\right)^2\right]$
RMS Current in Inductor *(A)*	$I_O \cdot \sqrt{1 + \frac{r^2}{12}}$	$\frac{I_O}{1 - D} \cdot \sqrt{1 + \frac{r^2}{12}}$	$\frac{I_O}{1 - D} \cdot \sqrt{1 + \frac{r^2}{12}}$
Average Current in Inductor *(A)*	I_O	$\frac{I_O}{1 - D}$	$\frac{I_O}{1 - D}$
RMS Current in Switch *(A)*	$I_O \cdot \sqrt{D \cdot \left[1 + \frac{r^2}{12}\right]}$	$\frac{I_O}{1 - D} \cdot \sqrt{D \cdot \left[1 + \frac{r^2}{12}\right]}$	$\frac{I_O}{1 - D} \cdot \sqrt{D \cdot \left[1 + \frac{r^2}{12}\right]}$
Peak Current Switch/Diode/ Inductor *(A)*	$I_O \cdot \left[1 + \frac{r}{2}\right]$	$\frac{I_O}{1 - D} \cdot \left[1 + \frac{r}{2}\right]$	$\frac{I_O}{1 - D} \cdot \left[1 + \frac{r}{2}\right]$
Average Current in Switch *(A)*	$I_O \cdot D$	$I_O \cdot \frac{D}{1 - D}$	$I_O \cdot \frac{D}{1 - D}$
Average Current in Diode *(A)*	$I_O \cdot (1 - D)$	I_O	I_O

Inductive Based Switching Regulator Circuits Provide High Efficiency White LED Drives

National Semiconductor
Application Note 1250
Clinton Jensen

Introduction

White LEDs are quickly becoming the light of choice for backlighting of small color displays because of their falling costs, longer life, and smaller size. The problem this presents is that the white LED has a high voltage drop (3.1V to 4.0V depending on manufacturer) as compared to the monochrome displays' green LED with a voltage drop of 1.8V to 2.7V. Whereas the green LED can be powered directly from the commonly used Li-Ion battery, with a linear regulator, and a ballast resistor, the white LED used for backlight or frontlight purposes will requires the battery voltage be boosted.

National has many solutions for driving LEDs including switched capacitor converters and inductive based switching regulators. This application note will describe some methods of driving white LEDs using inductive based switching regulators and some of the benefits of each. The main areas of concern for most designers of portable equipment are efficiency, size, cost, functionality, and LED current matching. Balancing these competing demands will help designers make the right choice for his or her application.

The Switching Regulator

A boost switching regulator set up as a constant current source can drive several white LEDs in series, keeping brightness constant even over a wide variation in supply voltage.

Figure 1, *Figure 2* and *Figure 3* show some designs using the LM2622 PWM boost regulator and the LM2704 PFM boost regulator.

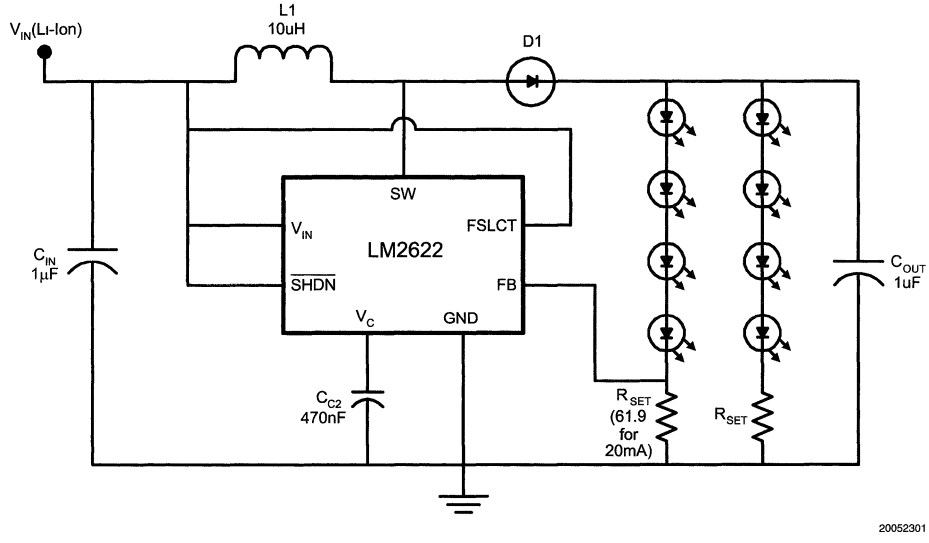


FIGURE 1. Basic LED Driver for Two to Eight LEDs at up to 30mA Each

The Switching Regulator (Continued)

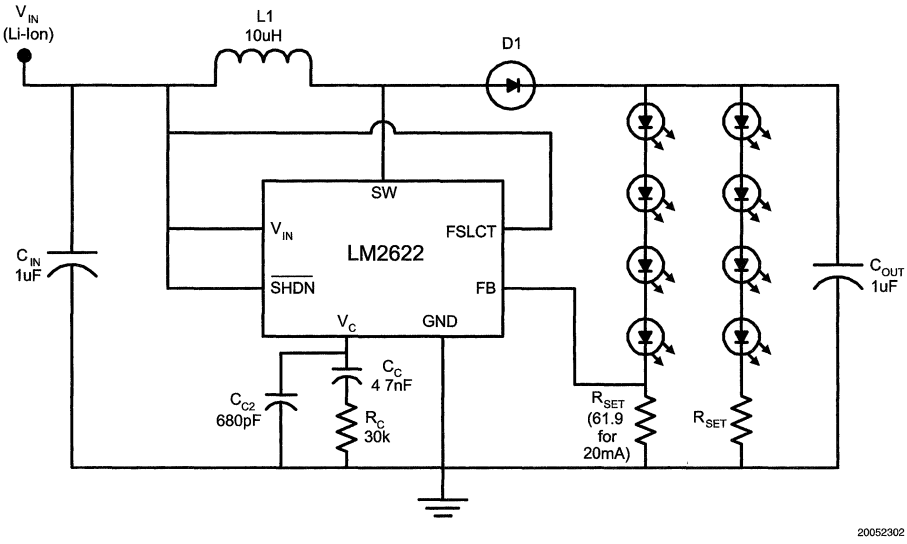


FIGURE 2. LED Driver with Improved Compensation for Faster Setup

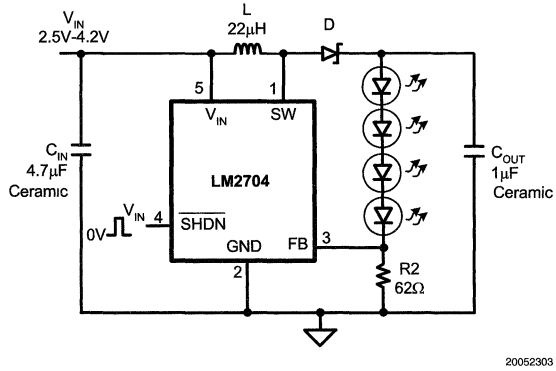


FIGURE 3. High-Efficiency LED Driver with Low Components Count Drives Two to Eight LEDs at up to 20mA Each

Figure 1 is capable of driving 2 to 8 white LEDs at up to 30mA each. When using 4 or fewer, the second string of LEDs (not connected to the FB pin) is eliminated. The desired LED current is set using the equation:

$$I_D = (1.26V/R_{SET})$$

When all of the LEDs are in series with each other (using up to 4), there is perfect current matching through each.

When a second string of LEDs is added it too will have perfect current matching through its LEDs, but not with the first string of LEDs. The current matching between the two strings will depend on how well the LED forward voltages match. Probability works to your advantage because the sum of four LEDs VF tend to balance widely varying VF in individual LEDs.

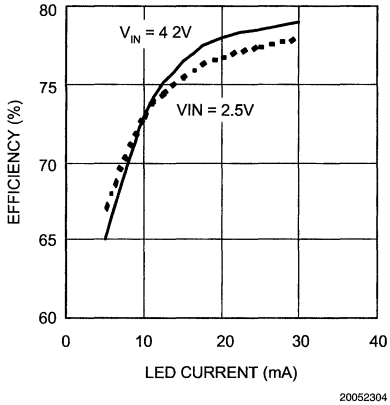
An inductive switching regulator also has a relatively high efficiency of typically 70% to 85% over the Li-Ion input voltage range (see Graph 1 for actual LM2622 measurements). However, higher efficiency comes at the expense of using an inductor for energy storage versus switched capacitor solutions that use only capacitors. The circuit of Figure 1 is best suited for static LED currents so dimming via a PWM (pulse width modulated square wave at the shutdown pin) signal is not recommended. This is due to the slow startup time of the circuit, which does not allow a sufficiently fast PWM signal to eliminate visible blinking. *Figure 1* is a reduced component count version of *Figure 2* at the expense of functionality.

The Switching Regulator (Continued)

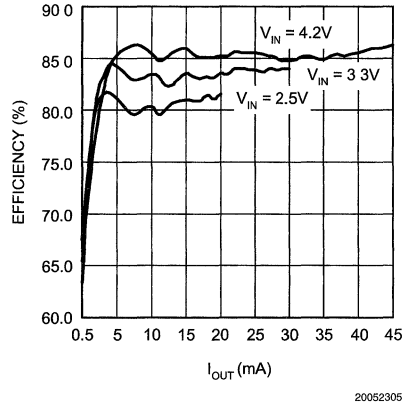
Figure 2 is identical in description to *Figure 1*, with the only difference being a change in how it is compensated. This requires an extra capacitor and resistor on the VC pin, but provides a faster startup time. The brightness of the LEDs can now be controlled using a PWM signal on the shutdown (SHDN) pin. This signal can be anywhere from 60Hz to 200Hz and the brightness is controlled by the duty cycle of the PWM signal (50% duty cycle equals approximately 50% LED current).

Figure 3 shows the LM2704 PFM (pulse frequency modulated) regulator. The LM2704 circuit has the same benefits of current matching and high efficiency as the LM2622 circuit but with a few advantages. Since it is a PFM architecture, it has a slightly better efficiency than the LM2622 . It is also more inherently stable which means a lower component count since the compensation R's and C's are no longer required. The LM2704 circuit is also physically smaller since it comes in a SOT-23 package versus the MSOP package of the LM2622. he costs of these advantages are a lower current output and a larger input capacitor The LM2704 is only capable of driving up to 8 LEDs at 20mA each, but this is plenty for most applications. PFM circuits are also more susceptible to noise and require more energy storage at the input. This requires the use of a large input capacitor relative to the PWM architecture.

In conclusion, the switching regulator approach is desirable for applications that require 2 to 8 LEDs, the highest efficiency, basic brightness functionality, and precise current matching.



LM2622 Efficiency (4 LEDs)



LM2704 Efficiency (4 LEDs)

Switched Capacitor Circuits Provide Efficient and Functional White LED Drive

National Semiconductor
Application Note 1251
Clinton Jensen

Introduction

Since the conception of cellular phones, PDAs, and handheld computers, there has been a continuing push for more useful and dynamic displays. One of the more drastic changes in miniature display technology has emerged due to the availability of Internet content, pictures, and videos on ever-shrinking personal devices. The promise of more content and functionality has caused a migration toward higher resolution color displays. This presents some added design issues, however, as a color LCD display requires white backlighting as opposed to the more standard green. The current options are using a cold cathode fluorescent lamp (CCFL), an electroluminescent backlight, or newer white LEDs. White LEDs are quickly becoming the light of choice because of their falling costs, longer life, and smaller size. The problem this presents is that the white LED has a high voltage drop (3.1V to 4.0V depending on manufacturer) as compared to the green LED with a voltage drop of 1.8V to 2.7V. Whereas the green LED can be powered directly from the commonly used Li-Ion battery, with a linear regulator, and a ballast resistor, the white LED used for backlight or frontlight purposes will requires the battery voltage be boosted.

National has many solutions for driving LEDs including switched capacitor converters and inductive based switching regulators. This application note will describe some different switched capacitor methods of driving white LEDs and the benefits of each. The main areas of concern for most designers of portable equipment are efficiency, size, cost, functionality, and LED current matching. Balancing these competing demands will help designers make the right choice for his or her application.

Switched Capacitor Voltage Regulator

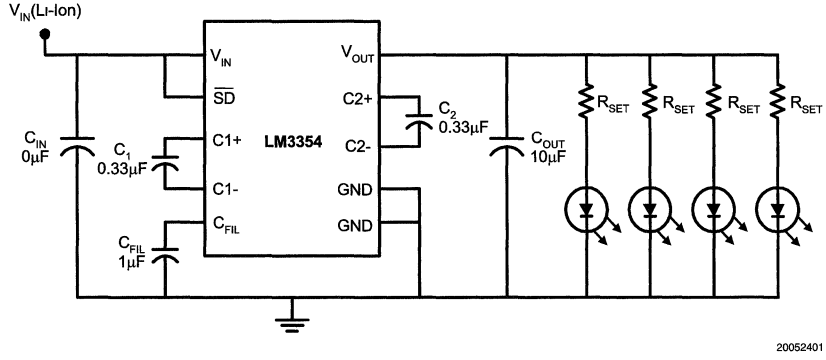


FIGURE 1. Switched Capacitor Voltage Regulator

This circuit is capable of supplying 90mA at 4.1V output (see the LM3355 for up to 50mA output current). The number of LEDs that may be driven depends on the LED current desired in each. The current is set using the equation:

$$I_D = (4.1V - V_F)/R_{SET}$$

where VF is the forward voltage drop of the LED chosen. As the LEDs are in parallel, the current matching is not perfect. The current matching will depend on the forward voltage drop of each LED and how well they match. This circuit is smaller than a switching regulator solution yet still maintains an average efficiency of about 70% (actual efficiency to LEDs, some power is dissipated by the ballast resistors) over the Li-Ion input voltage range. The brightness of the LEDs in this circuit may be controlled using a 60Hz to 200Hz PWM signal on the shutdown (SD) pin.

The switched capacitor voltage regulator approach is desirable for applications requiring 1 to 10 LEDs, high efficiency, brightness control functionality, lower cost and small solution size. However, this solution suffers from poor brightness matching due to varying LED currents.

Switched Capacitor Current Regulator

The second method presented here is a switched capacitor current regulator. Current regulation is achieved by using a switched capacitor boost circuit to drive a set of current sources. Figure 2 shows the LM2792 switched capacitor LED driver.

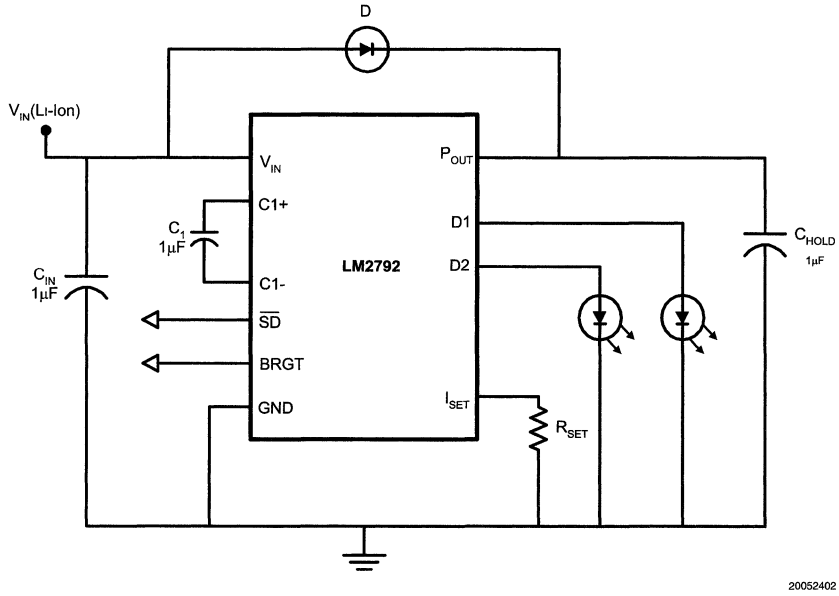


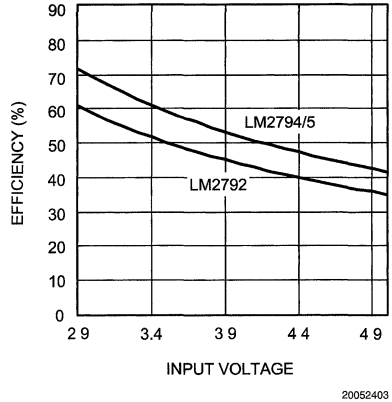
FIGURE 2. Switched Capacitor Current Regulator

This circuit uses a switched capacitor doubler (2X) circuit to power the current sources. It is capable of driving 1 to 2 LEDs at up to 32mA total (16mA each LED when using two). The current is set using the resistor RSET and the BRGT pin (refer to the datasheet for a description on setting current using RSET and the BRGT pin). Because current sources are used, the LED current matching is exceptional, within one percent. This circuit yields a smaller solution size than the voltage regulator and it provides more functionality, although at the cost of a significantly lower efficiency. The brightness can be controlled one of two ways. A PWM signal between 100Hz and 1kHz may be used at the shutdown (SD) pin as in the previous two examples. An analog voltage can be applied to the BRGT pin as well. This provides the ability to control the brightness with much better linearity. The BRGT pin also allows a variety of lighting patterns and effects since a continuous analog waveform of any desired shape can be used for controlling LED brightness.

For driving up to 4 LEDs the LM2794 or LM2795 may be used. These circuits are similar to the LM2792 in that they have all the same functionality. The difference is that a three halves (3/2X) charge pump is used to power the current sources. This provides higher efficiency (see Graph 1) since the current sources will have a reduced voltage drop across the transistors. They are capable of supplying a total of 60mA for up to 4 LEDs. The LM2794 and LM2795 also do not require the diode D shown in the LM2792 schematic. The only other difference is that where the LM2792 requires some signal at the BRGT pin to set the LED current, the LM2794 and LM2795 LED currents can be set using only RSET if desired. LM2794 and LM2795 are identical except for the polarity of the shutdown pin, to make it easier for designers to incorporate these solutions into existing systems.

The switched capacitor current regulator approach is desirable for circuits requiring 1 to 4 LEDs, precise current matching, small solution size, lowest cost and the highest functionality and control.

Switched Capacitor Current Regulator (Continued)



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Comparison of LM2792 and LM2794/5 Efficiency

DDR-SDRAM Termination Simplified Using a Linear Regulator

National Semiconductor
Application Note 1254
Chance Dunlap

With the advent of DDR-SDRAM as the industry standard for memory in desktop computers, laptops and videocards, power management has become a focal point for system designers. Active termination of bus interconnects has required the use of another regulator, increasing cost and system complexity. To specifically address this issue, National Semiconductor has just released the LP2995 DDR Termination Linear Regulator, offering a linear topology in a marketplace dominated by switchers. The implementation of this architecture has been made possible by careful examination of the system requirements. It is the intent of this article to illustrate the actual requirements of DDR-SDRAM termination and compare the two solution topologies.

With the memory migration from SDRAM to DDR-SDRAM, higher bus speeds and data transfer rates are attainable. As a consequence of the increased bandwidth, transmission problems have begun to appear The length of the memory interconnects, coupled with the multiple stubs that are required for supporting DIMMs result in signal reflection causing data corruption. This problem has required more attention as speeds have increased from DDR200 (100MHz clock) to DDR266 (133MHz clock) to the newly released DDR333 (166MHz clock) Concerned with the integrity of the signals at these high frequencies, JEDEC sought to create an industry standard for low voltage, high speed signaling as an improvement over LV_{TTL}. The result was an active termination scheme called SSTL (Stub Series Termination Logic).

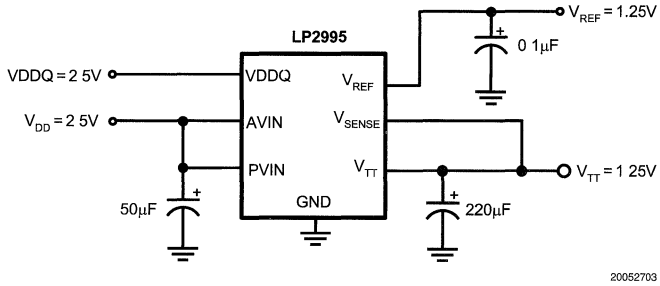


FIGURE 1. Implementation of SSTL

The JEDEC definition of SSTL-2 for 2.5V memory called for an active termination using a V_{TT} output voltage. This voltage is required to track a reference, VREF, which is created by dividing the memory power rail exactly in half. With the JEDEC specification defining the voltage tolerance on the individual rails, power delivery calculations have been left to the system designers. It is easily identifiable that V_{TT} needs to sink and source current, the problem is determining the magnitude. Historically, numbers were generated based on a macroscopic viewpoint of the system using static worst-case conditions. These approximate calculations defined the solution, by stating the following requirements:

- V_{TT} must sink and source current
- Maximum output current is 3A

Based on this definition, only one clear choice existed. a synchronous switcher had to be used. To meet these exacting requirements a plethora of switchers were designed to tackle this exact application from various manufacturers. The end solution was typically a synchronous PWM buck controller. A representation of a typical circuit implementing this topology can be seen in *Figure 2.*

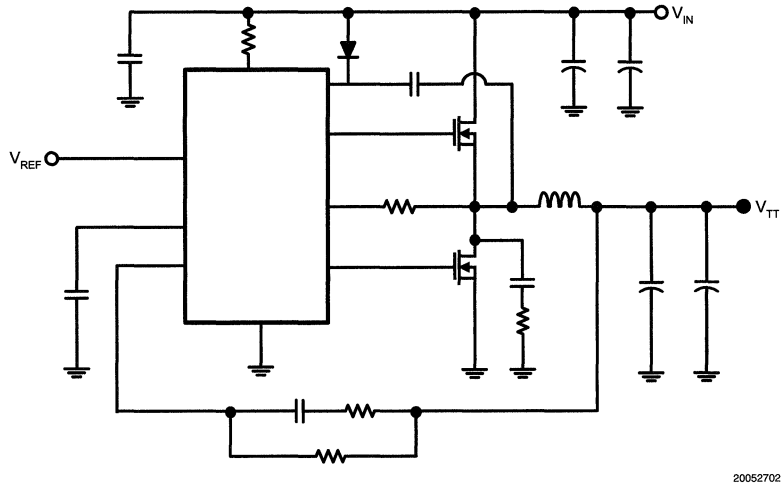


FIGURE 2. Synchronous PWM Switcher Topology

The synchronous buck switcher, while providing a feasible solution does not present an ideal or even optimal DDR termination regulator. Limitations exist that are inherent with the topology and the practical implementation. Several examples include:

Board Space: Due to the complexity of this solution a controller with high pin count is required to drive two external MOSFETs. Coupled with an inductor and the associated capacitors this implementation can occupy a significant amount of board area. This can be extremely critical in laptops and videocards where real estate is at a premium.

Cost: The high component count required for the application translates directly into increased cost.

Performance The most fundamental requirement for any DDR termination regulator is performance. While the task of creating a 1.25V reference signal within a +/-200mV window is trivial, the challenge in designing a switching power supply is limiting the switching noise and EMI. Signal interference resulting in data loss is possible if switching harmonics are present on the bus. Though not impossible to limit, it poses an increase in cost and development time to reduce the effects.

The initial assumption that 3A were required for the maximum output current, resulting in the selection of the buck switcher, was actually an oversight. The cause of this problem was that the worst-case conditions were incorrect resulting in over design of the regulator. To counter this problem, National Semiconductor approached the power delivery calculations from a memory architecture and control point of view to define an entirely new solution. From an in-depth analysis of the PC memory it becomes apparent that 3A are not required. The exact analysis is not included in this article due to length, however, several of the key points have been highlighted:

- DDR-SDRAM is a dynamic system, static assumptions of a 133MHz clock (266MHz data rate) are not realistic when applied to the regulator requirements.
- Theoretical peak calculations are not obtainable for sustained durations. Data cannot be clocked every edge indefinitely. Delays such as CAS latencies are an important assessment in every memory access.
- Significant current cancellation can occur from complementary signals such as data strobes.
- Two line conditions are insufficient for a complete model, tri-stating and transitional periods need to be incorporated.
- Even periodic refresh affects the average output current required by the regulator.

Coupled with technical analysis, confirmed by empirical measurements, National Semiconductor found that the average currents required are closer to 200mA. Worse case conditions, simulated by intensive memory burn-in tests, result in little deviation from this figure. This new design target meant that an entirely new topology can be used: **LINEAR**, bestowing all its advantages.

Leveraging the results found from the measurements, National Semiconductor addressed the shortcomings of the switcher topology and created a new standard in DDR bus termination by releasing the LP2995. The LP2995 utilizes an exclusive linear topology to create the V_{TT} output voltage and the reference output, VREF, for the chipset and DIMMs. A typical application circuit for the LP2995 can be seen in *Figure 3*

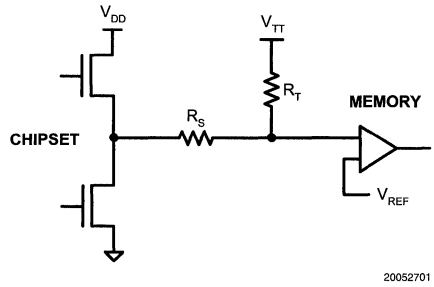


FIGURE 3. LP2995 Typical Application Circuit

Re-examining the limitations of the switcher and comparing it to the LP2995, the benefits of a linear topology are immediately recognizable.

Size: The external component count has been drastically reduced, permitting the solution to occupy a minimal amount of space. Combined with the LP2995 in an LLP package (Leadless Leadframe Package) an optimal solution can be obtained.

Cost: Removal of the external components creates an instant system cost reduction by 60%.

Performance: By its nature as a linear topology, there is no internal oscillator or switching noise to take into consideration. This results in increased performance, as data integrity can be improved with the absence of switching noise on V_{TT}.

Through careful analysis of the actual memory requirements National Semiconductor was able to provide the optimal solution for DDR termination, the LP2995. Designed with consideration of the end user it offers the highest level of integration while increasing the system performance and lowering the total system cost. The LP2995 offers the perfect solution for any DDR-SDRAM application where space, performance and cost are critical constraints.

High Stability Regulators

National Semiconductor
Linear Brief 15
Chance Dunlap

Monolithic IC's have greatly simplified the design of general purpose power supplies. With an IC regulator and a few external components 0.1% regulation with 1% stability can be obtained. However, if the application requires better performance, it is advisable to use some other design approach.

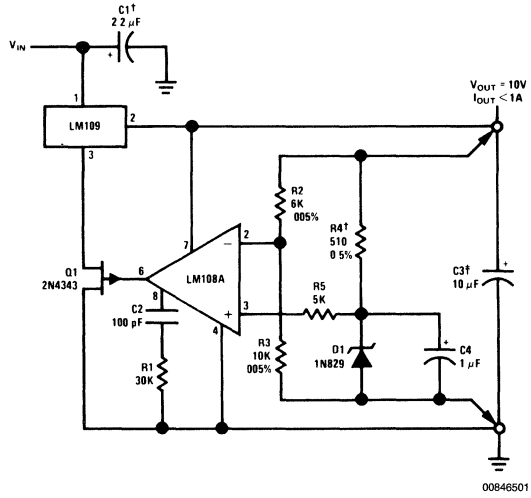
Precision regulators can be built using an IC op amp as the control amplifier and a discrete zener as a reference, where the performance is determined by the reference. *Figures 1, 2* show schematics of simple positive and negative regulators. They are capable of providing better than 0.01% regulation for worst case changes of line, load and temperature. Typically, the line rejection is 120 dB to 1 kHz; and the load regulation is better than 10 µV for a 1A change. Temperature is the worst source of error; however, it is possible to achieve less than a 0.01% change in the output voltage over a −55°C to +125°C range.

The operation of both regulators is straightforward. An internal voltage reference is provided by a high-stability zener diode. The LM108A[1] operational amplifier compares a fraction of the output voltage with reference. In the positive regulator, the output of the op amp controls the ground terminal of an LM109[2] regulator through source follower, Q_1. Frequency compensation for the regulator is provided by both the R_1 C_2 combination and output capacitor, C_3.

The negative regulator shown in *Figure 2* operates similarly, except that discrete transistors are used for the pass element. A transistor, Q_1, level shifts the output of the LM108 to drive output transistors, Q_3 and Q_4. Current limiting is provided by Q_2. Capacitors C_3 and C_4 frequency compensate the regulator.

In the positive regulator the use of an LM109 instead of discrete power transistors has several advantages. First, the LM109 contains all the biasing and current limit circuitry needed to supply a 1A load. This simplifies the regulator. Second, and probably most important, the LM109 has thermal overload protection, making the regulator virtually burn-out proof. If the power dissipation becomes excessive or if there is inadequate heat sinking, the LM109 will turn off when the chip temperature reaches 175°C, preventing the device from being destroyed. Since no such device is available for use in the negative regulator, the heat sink should be large enough to keep the junction temperature of the pass transistors at an acceptable level for worst case conditions of maximum ambient temperature, maximum input voltage and shorted output.

Although the regulators are relatively simple, some precautions must be taken to eliminate possible problems. A solid tantalum output capacitor must be used. Unlike electrolytics, solid tantalum capacitors have low internal impedance at high frequencies. Low impedance is needed both for frequency compensation and to eliminate possible minor loop oscillations. The power transistor recommended for the negative regulator is a single-diffused wide-base device. This transistor type has fewer oscillation problems than double diffused transistors. Also, it seems less prone to failure under overload conditions.

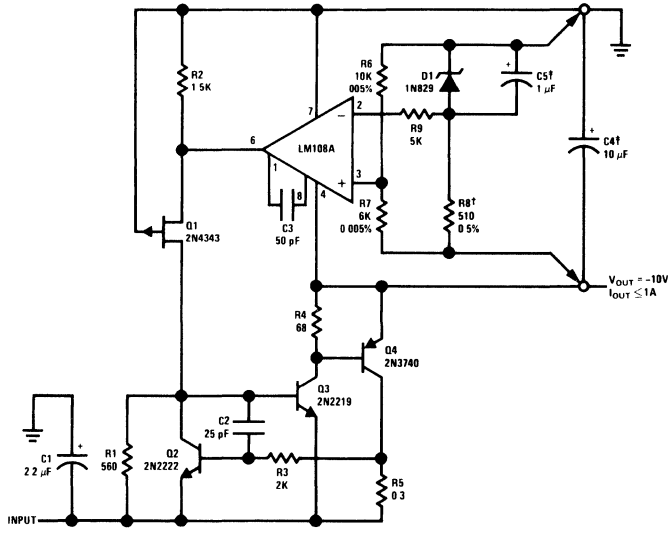


†Determines zener current. May be adjusted to minimize thermal drift
‡Solid tantalum

FIGURE 1. High Stability Positive Regulator

Some unusual problems are encountered in the construction of a high stability regulator. Component choice is most important since the resistors, amplifier and zener can contribute to temperature drift. Also, good circuit layout is needed to eliminate the effect of lead drops, pickup, and thermal gradients.

The resistors must be low-temperature-coefficient wirewound or precision metal film. Ordinary 1% carbon film, tin oxide or metal film units are not suitable since they may drift as much as 0.5% over temperature. The resistor accuracy need not be 0.005% as shown in the schematic; however, they should track better than 1 ppm/°C. Additionally, wirewound resistors usually have lower thermoelectric effects than film types. The resistor driving the zener is not quite as critical; but it should change less than 0.2% over temperature.



†Determines zener current May be adjusted to minimize thermal drift

‡Solid tantalum

FIGURE 2. High Stability Negative Regulator

The excellent dc characteristics of the LM108A make it a good choice as the control amplifier. The offset voltage drift of less than 5 µV/°C contributes little error to the regulator output. Low input current allows standard cells to be used for the voltage reference instead of a reference diode. Also the LM108 is easily frequency compensated for regulator applications.

Of course, the most important item is the reference. The IN829 diode is representative of the better zeners available. However, it still has a temperature coefficient of 0.0005%/°C or a maximum drift of 0.05% over a −55°C to +125°C temperature range. The drift of the zener is usually linear with temperature and may be varied by changing the operating current from its nominal value of 7.5 mA. The temperature coefficient changes by about 50 µV/°C for a 15% change in operating current. Therefore, by adjusting the zener current, the temperature drift of the regulator may be minimized.

Good construction techniques are important. It is necessary to use remote sensing at the load, as is shown on the schematics. Even an inch of wire will degrade the load regulation. The voltage setting resistors, zener, and the amplifier should also be shielded. Board leakages or stray capacitance can easily introduce 100 µV of ripple or dc error into the regulator. Generally, short wire length and single-point grounding are helpful in obtaining proper operation.

References

1. R.J. Widlar, "IC Op Amp Beats FETs on Input Current," *National Semiconductor AN-29*, December, 1969.
2. R.J. Widlar, "New Developments in IC Voltage Regulators," in *1970 International Solid-State Circuits Conference Digest of Technical Papers*, Vol. XIII, pp. 158–159.

+5 to −15 Volts DC Converter

National Semiconductor
Linear Brief 18
Chance Dunlap

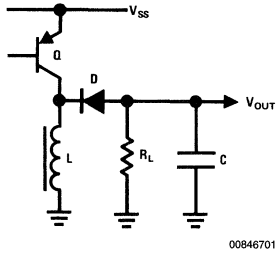
Introduction

It is frequently necessary to convert a DC voltage to another higher or lower DC-voltage while maximizing efficiency. Conventional switching regulators are capable of converting from a high input DC voltage to a lower output voltage and satisfying the efficiency criteria. The problem is a little more troublesome if a higher output voltage than the input voltage is desired. Particularly, generating DC voltage with opposite polarity to the input voltage usually involves a complicated design.

This brief demonstrates the use of the switching regulator idea for a +5 volts to −15 volts converter. The converter has an application as a power supply for MOS memories in a logic system where only +5 volts is available. However, the principle used can be amplied for almost any input output combination.

Operation

The method by which the regulator generates the opposite polarity is explained in *Figure 2.* The transistor Q is turned ON and OFF with a given duty cycle. If the base drive is sufficient the voltage across the inductor is equal to the supply voltage minus V_{SAT}. The current change in the inductor is given by:



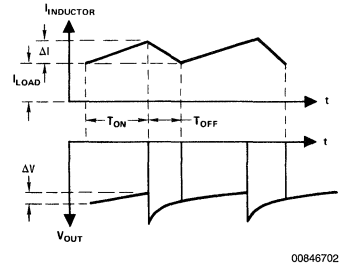


FIGURE 1. Switching Circuit for Voltage Conversion

$$\Delta I = \frac{V_{SS} - V_{SAT}}{L} \times T_{ON} \approx \frac{V_{SS}}{L} T_{ON} \quad (1)$$

Turning OFF the transistor the inductor current has a path through the catch diode and this in turn builds up a negative voltage across R_L.

The figure also shows the current and voltage levels versus time. A capacitor in parallel to the resistor will prevent the voltage from dropping to zero during the transistor ON time.

Assuming a large capacitor, we can also write the current change as:

$$\Delta I = \frac{V_{OUT} - V_D}{L} \times T_{OFF} \approx \frac{V_{OUT}}{L} \times T_{OFF} \quad (2)$$

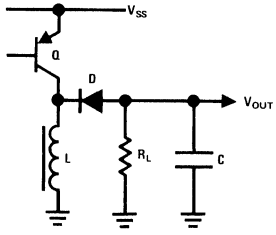
In order to get a general idea of the operation for certain input output conditions, we will develop a set of equations.

During the transistor ON time, energy is loaded into the inductor. In the same time interval, the capacitor is drained due to the load resistor R_L.

Drop in capacitor voltage:

$$\Delta V = \frac{I_{LOAD} \times T_{ON}}{C} \quad (3)$$

Operation (Continued)



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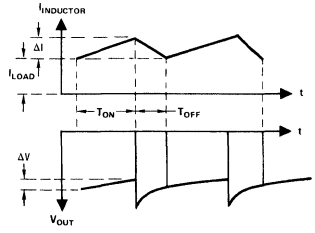

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FIGURE 2. Switching Circuit for Voltage Conversion

During the T_{OFF} time the stored energy in the inductor is transferred to the load and capacitor. A rough estimate of T_{OFF} can be expressed as:

$$T_{OFF} = \frac{V_{SS}}{V_{OUT}} \times T_{ON} \quad (4)$$

The capacitor voltage will be restored with a average current given by:

$$I_C = \frac{\Delta V \times C}{T_{OFF}} = \frac{I_{LOAD} \times V_{OUT}}{V_{SS}} \quad (5)$$

The total inductor current during the OFF time can be written as:

$$I_{INDUCTOR} = I_{LOAD} + I_C \quad (6)$$

Inspecting *Figure 2*. We find:

$$I_C = \frac{\Delta I}{2} = \frac{V_{SS} \times T_{ON}}{2 \times L} \quad (7)$$

which yields:

$$T_{ON} = \frac{2 \times L \times I_{LOAD} \times V_{OUT}}{V_{SS}^2} \quad (8)$$

Taking into account that the efficiency is in the order of 75% the final expression is:

$$T_{ON} = \frac{1.5 \times L \times I_{LOAD} \times V_{OUT}}{V_{SS}^2} \quad (9)$$

The above equations will be applied to the regulator shown at *Figure 3*. The regulator must deliver −15 volts at 200 mA from a +5 volt supply. Using a 1 mH inductor the T_{ON} time for Q_2 is 0.18 ms from *Equation (9)*. T_{OFF} is 60 µs from *Equation (4)* and the oscillator frequency to:

$$F = \frac{1}{T_{ON} + T_{OFF}} \approx 4\ kHz$$

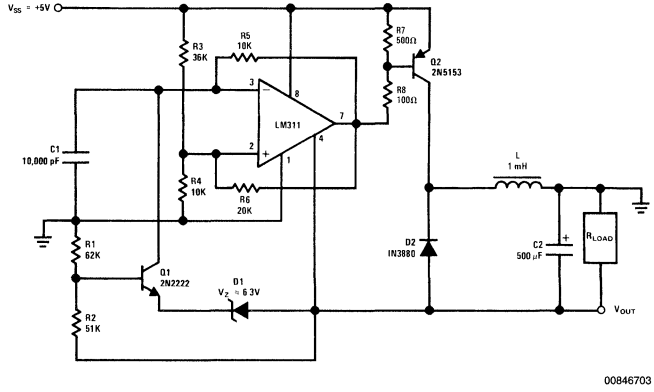

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FIGURE 3. Switching Regulator for Voltage Conversion

Operation (Continued)

$$\eta = \frac{P_{OUT}}{P_{IN}} \geq 75\%$$

$$F = 6\ kHz\ 80\%\ DUTY$$

$$V_{RIPPLE} = 100\ mV\ @200\ mA\ OUT$$

$$I_L = 200\ mA\ MAX$$

$$V_{OUT} = -15V$$

$$V_{OUT} = (V_2 + V_{BE}\left(\frac{R_1}{R_2} + 1\right))$$

The LM311 performs like a free running multivibrator with high duty cycle. The IC is designed to operate from a standard single 5 volt supply and has a high output current capability for driving the switching transistor Q_2. The duty cycle is given by the voltage divider R_3 and R_4 and the frequency of C_1 in conjunction with R_5.

By setting the duty cycle higher than first calculated, the output voltage will tend to increase above the desired output voltage of 15 volts. However, an extra loop performed by Q_1 and the zener diode in conjunction with the resistor network will modify the oscillator duty cycle until the desired output level is obtained.

The output voltage is given by:

$$V_{OUT} = \left(V_Z + V_{BE}\right)\left(\frac{R_1}{R_2} + 1\right)$$

Data and results obtained with the design:

V_{IN}	= 5 volts
V_{OUT}	= −15 volts
I_{OUT}	= max 200 mA
Efficiency	≅ 75%
Frequency	≅ 6 kHz 80% duty cycle
V_{RIPPLE}	≅ 100 mV @ 200 mA load
Line regulation:	V_{IN} = 5V to 10V < 3% V_{OUT}
	I_{LOAD} = 200 mA
Load regulation:	V_{IN} = 5V < 3% V_{OUT}
	I_{LOAD} = 0 − 100 mA

General Purpose Power Supply

National Semiconductor
Linear Brief 28
Chance Dunlap

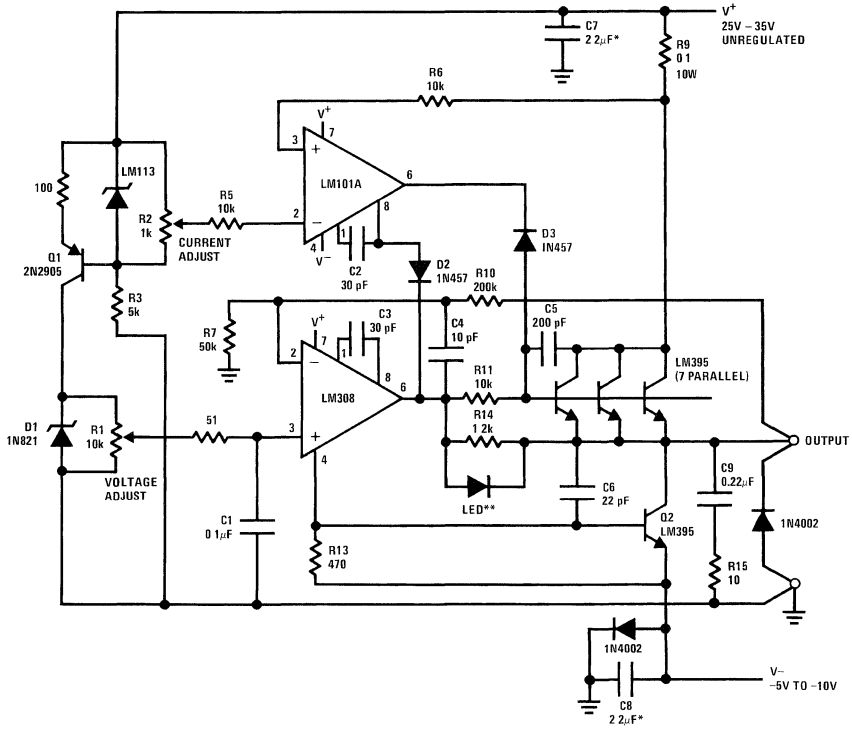
Introduction

A general purpose lab type constant voltage/constant current power supply is easily made using standard integrated circuits. The circuit shown will provide up to 25V at up to 10A output with both the output voltage and current adjustable down to zero. Although relatively simple, very high performance is obtained.

Lab supplies must withstand considerable abuse. Good control of maximum output current is mandatory both to protect the supply and the powered circuitry. One of the shortcomings of many commercial supplies is the use of a large output capacitor to help frequency compensate the regulator loop This output capacitor can discharge many times the peak output current of the supply into the load as well as degrade the ac output impedance when the supply is used as a constant current source. (Of course, the output capacitor helps keep the ac output impedance low when the supply is used as a constant voltage source.) The circuit shown has good response both as a constant voltage or constant current source.

The use of the LM395 monolithic power transistor as the pass element considerably simplifies the design power. The LM395 acts as a 2A current limited, thermally limited, high gain power transistor. Since only a maximum of 10 µA is needed to drive the pass elements and complete overload protection is included on the chip, external biasing and protection circuitry is minimized. Only two control op amps are needed–one for voltage control and one for current control.

In constant voltage operation, a reference voltage is fed from voltage control pot, R1, through a high frequency filter into the non-inverting input of an LM308 op amp. The output of the LM308 drives seven paralleled LM395's as emitter followers to obtain a 10A capability.



*Solid Tantalum **Lights during current limit

Feedback is taken through R10 directly from the output with the overall gain set at 5 by the ratio of R10 to R7. An additional LM395 is driven from the negative power supply lead of the LM308 to provide some output current sink capability (2A) so the supply can be quickly programmed even with large capacitive loads. Frequency compensation is achieved with C3 for the LM308 and C4 for the overall loop. Resistor R11, capacitors C5 and C6 and network R15–C9 suppress parasitic high frequency oscillations

When the circuit is used in the constant current mode, the LM101A overcomes the constant voltage loop to control the

output. Output current is sensed in R9 and compared with the voltage between V^+ and the arm of R2. R2 is connected across an LM113 low voltage reference diode to provide a 0V to 1.2V reference for 0A to 12A output. When the output current is below the set level, the LM101A output is positive, reverse biasing D3 and the LM308 control the outpput. When the current increases to the control point the output of the LM101A swings negative and decreases the drive to the output pass devices through D3, limiting the current. (Note that no separate positive supply is needed since the common mode operative range of the LM101A is equal to the positive supply.) Diode, D2, clamps the output of the LM101A when it is not regulatıng, decreasing the switchover time from voltage to current mode operation.

A few special precautions are needed in construction for proper operation. All LM395's should be mounted on the same heat sink to insure good current sharing. Also, a large heat sink is necessary since 300W will be dissipated under worst case conditions. Since the LM395's are high devices, the supply bypasses should be near the power transistors.

Adjustable 3-Terminal Regulator for Low-Cost Battery Charging Systems

National Semiconductor
Linear Brief 35
Chance Dunlap

With the introduction of the LM317, a 3-terminal adjustable regulator, it becomes relatively easy to design high-performance, low-cost battery charging systems. Even single battery cells can be charged on this new regulator, which is adjustable down to 1.2V. The internal protection circuitry can be used to limit charging current as well as to protect against overloads. The output voltage is easily adjusted so multiple voltage chargers can be made.

The ability to accurately adjust the output voltage of the LM317 makes it especially attractive for constant voltage battery charging applications. Batteries are most quickly charged by "constant-voltage" charging circuits; however, close control of the charging voltage is necessary to prevent overcharging, especially with nickel cadmium cells. The internal protection circuitry of the LM317 is helpful in protecting against accidental overload conditions commonly occurring in charging systems.

Internal Current Limit

The peak charging current or output current is controlled by the internal current limit of the LM317. This current limit will work even if a battery is connected backwards to the output of the charger. Should a fault condition exist for an extended period of time, the thermal limiting circuitry will decrease the output current, protecting the regulator as well as the transformer A constant voltage charger circuit is shown in *Figure 1*. The output voltage is set with resistors R2 and R3 and given by

$$V_{OUT} = 1.25\left(1 + \frac{R3}{R2}\right)$$

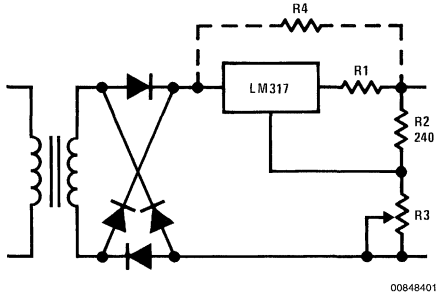


FIGURE 1. Constant Voltage Charging Circuit

Since, in low cost applications, no filter capacitors are used on the output of the rectifier, the battery is only charged on the peaks of the sine wave. This requires the peak output voltage from the transformer to be at least 50% greater than the battery voltage plus 3V. However, little cost premium should result since the average current from the transformer is lower than capacitive input filter circuits. Optional resistors R1 and R2 are used to further control the charging characteristics. Resistor R1 controls the output impedance of the charger allowing a "taper-charge" characteristic to be generated. The LM317 can also be used to limit the peak charging current to a partially charged battery at a value other than the regulator current limit. With R1 in the circuit, the output impedance is:

$$Z_{OUT} = R1\left(1 + \frac{R3}{R2}\right)$$

Including R1 in the feedback loop decreases the value of resistor needed for a particular output impedance reducing cost and power dissipation.

For example, with a 6V gelled electrolyte battery the regulator can be set to give a 6.9V output. Nominally, the battery is discharged to about 5V, making R1 0.4Ω output impedance and limiting the charging current to 0.5A at the start of charging rather than the internal current limit of the regulator. With a fully discharged battery or under short circuit conditions, the peak output current is still 2A for the LM317K with the resistor dissipating 1.6A as opposed to 8W if a 2Ω resistor were used directly in series with the battery.

Resistor R4 can be included to provide a low "topping-up" current for a charged battery.

This regulator configuration provides some other important features to the charger. If input power is removed and a fully charged battery is connected to the charger output, there is no damage. Under these conditions about 5 mA of current will be drawn by divider R2, R3. Since there is no ground connection to the LM317 regulator, very little current flows through the LM317. In this respect, the LM317 differs from other 3-terminal regulators, which can be damaged by applying power to the output terminal with the input open-circuited. If the battery is connected backwards, the LM317 will current limit and thermal limit normally, protecting the charger.

Decreasing Current Limit

Adding a single NPN transistor can be used to decrease the current limit of the charge as shown in *Figure 2.*

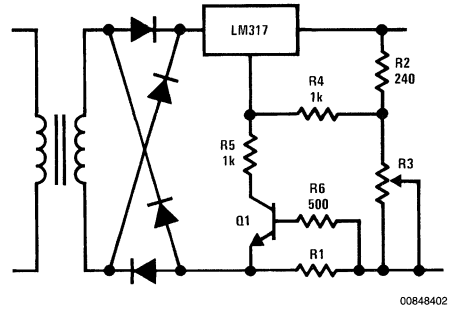


FIGURE 2. Constant Voltage Charger with Peak Current Limiting

Decreasing Current Limit (Continued)

Resistor R1 senses the output current and turns on Q1 when I_{OUT} R1 equals about 0.6V. Transistor Q1 pulls the adjustment terminal negatively decreasing the output voltage and controlling the output current. A limitation of this circuit is that it does not work for direct short circuits. The output voltage must be above about 0.6V for the external current limiting to be active. The internal current limit of the LM317, of course, is still operative. This is not usually a problem since batteries charge to above 0.6V very quickly. Resistors R4, R5 and R6 protect the regulator and transistor for both direct short circuits or reverse battery connections.

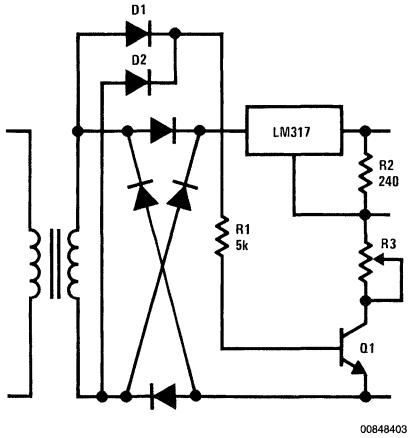


FIGURE 3. Charger with No Battery Loading when Power is "OFF"

As illustrated in *Figure 3*, in float or standby applications, it is desirable to remove all loading from the battery when input power is "OFF." When power is "ON," Q1 is saturated, grounding the voltage setting divider R2, R3 and the circuit works in a similar manner to the charger circuit in *Figure 1*. When power is "OFF," Q1 is open, eliminating any loading on the battery. A separate pair of low current diodes D1, D2 are necessary to bias Q1, rather than the power bridge rectifier.

If R1 was tied to the output of the bridge, reverse current flow through the LM317 would keep Q1 "ON" and loading the battery.

A simple constant current charger for any type of battery is shown in *Figure 4*. A resistor R1 between the adjustment terminal and the output of the regulator sets the output current at:

$$I_{OUT} = \frac{1.25}{R1}$$

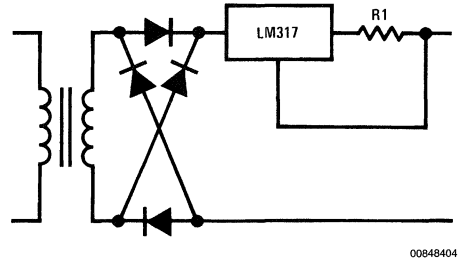


FIGURE 4. Constant Current Charger

Current can be set at anywhere between 10 mA and 1.5A by appropriate resistor choice. Current regulation is very tight at any current level since only 50 µA flows out of the adjustment terminal. This circuit is also immune to damage from shorts or reverse battery connections. The input voltage for regulation should also be about 1.5 times the battery voltage plus 3V.

Uniquely Suited

The ability to adjust the output of the LM317 3-terminal regulator makes it uniquely suited for battery charging systems. Little has been included about charging specific types of batteries, since the characteristics of the charger should be matched to the battery. These charger circuits, although very simple, perform well. They are easily modified for voltage, current or even temperature coefficient by making the divider string temperature sensitive. More complex chargers can be made since the output of the LM317 is easily controlled by driving the adjustment terminal. Finally, the chargers are inherently protected against overloads and fault conditions.

A New Production Technique for Trimming Voltage Regulators

National Semiconductor
Linear Brief 46
Robert A. Pease

Three-terminal adjustable voltage regulators such as the LM317 and LM337 are becoming popular for making regulated supplies in instruments and various other OEM applications. Because the regulated output voltage is easily programmed by two resistors, the designer can choose any voltage in a wide range such as 1.2V to 37V. In a typical example (*Figure 1*) the output voltage will be:

$$V_{OUT} = V_{REF}\left(\frac{R2}{R1} + 1\right) + R2 \bullet I_{ADJ}$$

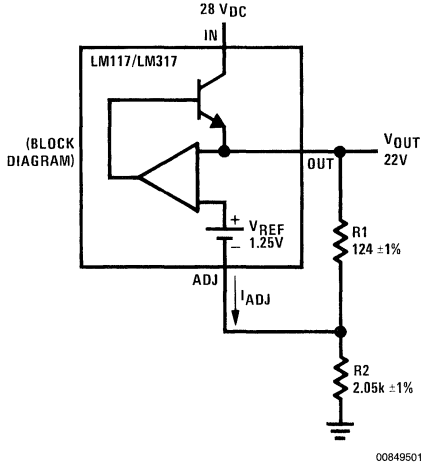


FIGURE 1. Basic Regulator

In many applications, when R1 and R2 are inexpensive ±1% film resistors, and the room temperature accuracy of the LM117 is better than ±3%, the overall accuracy of ±5% will be acceptable. In other cases, a tighter tolerance such as ±1% is required. Then a standard technique is to make up part of R2 with a small trim pot, as in *Figure 2*. The effective range of R2 is 2.07k ±10%, which is adequate to bring V_{OUT} to exactly 22.0V. (Note that a 200Ω rheostat in series with 1.96 kΩ ±1% would not necessarily give a ±5% trim range, because the end resistance and wiper resistance could be as high as 10Ω or 20Ω; and the maximum value of an inexpensive 10% or 20% tolerance trimmer might be as low as 180Ω or 160Ω.)

In some designs, the engineering policy may frown on the use of such trim pots, for one or more of the following reasons:

- Good trim pots are more expensive.
- Inexpensive trim pots may be drifty or unreliable.
- Any trim pot which can be adjusted can be *mis*adjusted, sooner or later.

To get a tighter accuracy on a regulated supply, while avoiding these disadvantages of trim pots, consider the scheme in *Figure 3*.

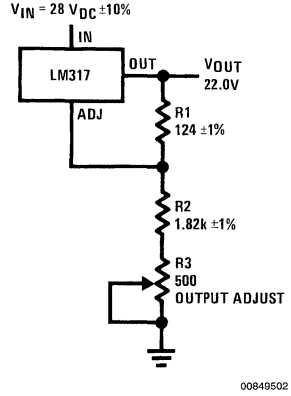


FIGURE 2. Regulator with Small Adjustment Range

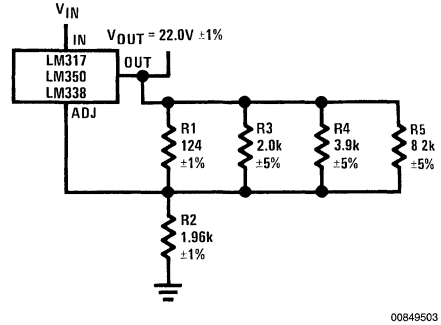


FIGURE 3. Regulator with Trimmable Output Voltage

When first tested, V_{OUT} will tend to be 4% to 6% higher than the 22.0V target. Then, while monitoring V_{OUT}, snip out R3, R4, and/or R5 as appropriate to bring V_{OUT} closer to 22.0V. This procedure will bring the tolerance inside ±1%:

- If V_{OUT} is 23.08V or higher, cut out R3 (if lower, don't cut it out).
- Then if V_{OUT} is 22.47V or higher, cut out R4 (if lower, don't).
- Then if V_{OUT} is 22.16V or higher, cut out R5 (if lower, don't).

The entire production distribution will be brought inside 22.0V ±1%, with a cost of 3 inexpensive carbon resistors,

much lower than the cost of any pot. After the circuit is properly trimmed, it is relatively immune to being misadjusted by a screwdriver. Of course, the resistors' carcasses must be properly removed and disposed of, for full reliability to be maintained.

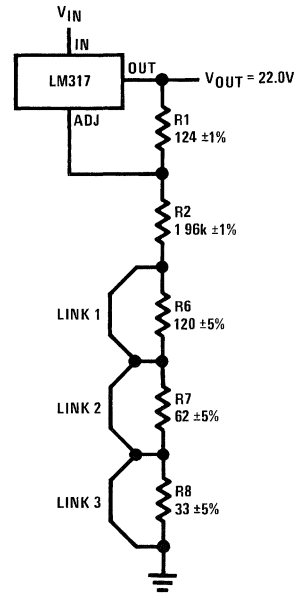
An alternate scheme shown in *Figure 4* has R6, R7, and R8 all shorted out initially with a stitch or jumper of wire. The trim procedure is to open up a link to bring a resistor into effect. The advantage of this circuit is that V_{OUT} starts out *lower* than the target value, and never exceeds that voltage during trimming. In this scheme, note that a total "pot resistance" of 215Ω is plenty for a 10% trim span, because the *minimum* resistance is always below 1Ω, and the maximum resistance is always more than 200Ω—it can cover a much wider range than a 200Ω pot.

The circuit of *Figure 5* shows a combination of these trims which provides a new advantage, if a ±2% max tolerance is adequate. You may snip out R4, or link L1, or both, to accommodate the worst case tolerance, but in most cases, the output will be within spec without doing any trim work at all.

This takes advantage of the fact that most ±1% resistors are well within ±⅓%, and most LM337's output voltage tolerances are between −½% and +1½%, to cut the average trim labor to a minimum. Note that L1 could be made up of a 2.7Ω ±10% resistor which may be easier to handle than a piece of wire.

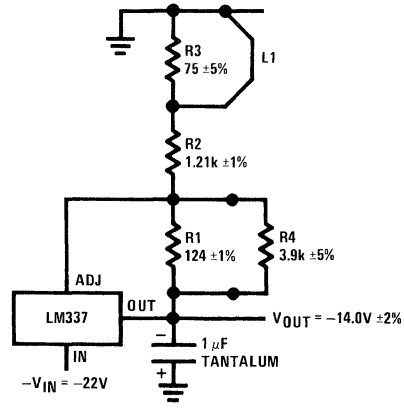
In theory, a 10% total tolerance can be reduced by a factor of $(2^n - 1)$ when n binary-weighted trims are used. In practice, the factor would be $(1.8^n - 1)$ if ±10% trim resistors are used, or $(1.9^n - 1)$ if ±5% resistors are used. For n = 2, a 10% tolerance can be cut to 3.8% p-p or ±1.9%. For n = 3, the spread will be 1.7% p-p or ±0.85%, and most units will be inside ±0.5%, perfectly adequate for many regulator applications.

National Semiconductor manufactures several families of adjustable regulators including LM117, LM150, LM138, LM117HV, LM137, and LM137HV, with output capabilities from 0.5A to 5A and from 1.2V to 57V. For complete specifications and characteristics, refer to the appropriate data sheet or the 1982 Linear Databook.



If V_{OUT} is lower than 20 90V, snip link 1 (if not, don't)
Then if V_{OUT} is lower than 21 55V, snip link 2 (if not, don't)
Then if V_{OUT} is lower than 21 82V, snip link 3 (if not, don't).

FIGURE 4. Alternate Trim Scheme



If $|V_{OUT}|$ is smaller than 13 75V, snip L1 and it will get bigger by 6%
Then if $|V_{OUT}|$ is bigger than 14 20V, snip R4 and it will get smaller by 3%

FIGURE 5. Circuit Which Usually Needs No Trim to Get V_{OUT} Within ±2% Tolerance

High Voltage Adjustable Power Supplies

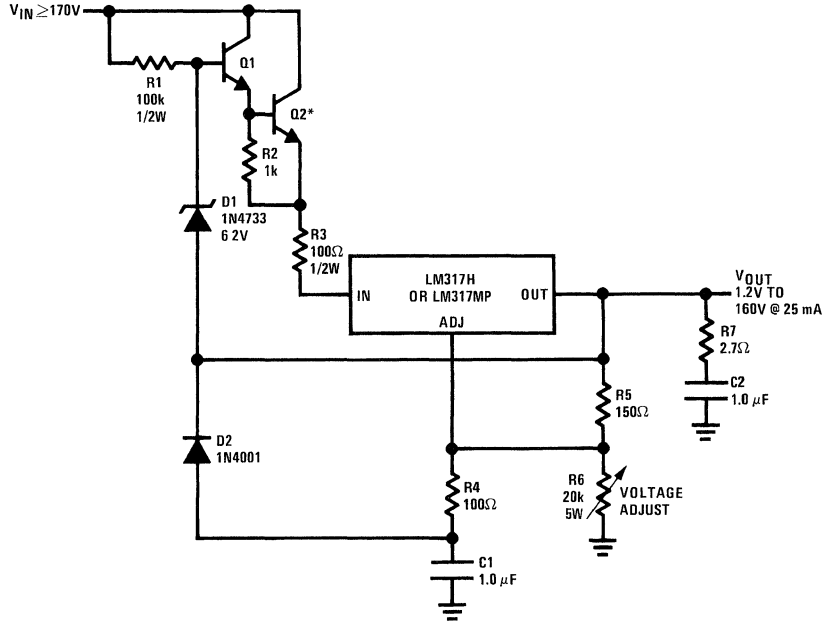
National Semiconductor
Linear Brief 47
Michael Maida

High Voltage Adjustable Power Supplies

The floating-mode operation of adjustable three-terminal regulators such as the LM117 family make them ideal for high voltage operation. The regulator has no ground pin; instead, all the quiescent current (about 5 mA) flows to the output terminal. Since the regulator sees only the input-output differential, its voltage rating — 40V for the standard LM117 series and 60V for the high voltage LM117HV series — will not be exceeded for outputs of hundreds of volts. However, the IC may break down when the output is shorted unless special design approaches are used to protect against it.

Figure 1 shows how it's done. Zener diode D1 ensures that the LM317H sees only a 5V input-output differential over the entire range of output voltage from 1.2V to 160V. Since high-voltage transistors by necessity have a low β, a Darlington is used to stand off the high voltage. The zener impedance is low enough that no bypass capacitor is required directly at the LM317 input. (In fact, *no* capacitor should be used here if the circuit is to survive an output short!) R3 limits short circuit current to 50 mA. The RC network on the output improves transient response as does bypassing the ADJUST pin, while R4 and D2 protect the ADJUST pin during shorts.

Since Q2 may dissipate up to 5W normally or 10W during a short circuit, it should be well heat sunk. For higher output currents substitute a pass device in a TO-3 or TO-220 package in place of the TO-202 NSD134 and reduce R3. Of course, if the required output current is less than 25 mA, R3 can be increased to reduce the size of the heat sink needed.



Q1, Q2 NSD134 or similar
C1, C2 1 μF, 200V MYLAR
*Heat Sink

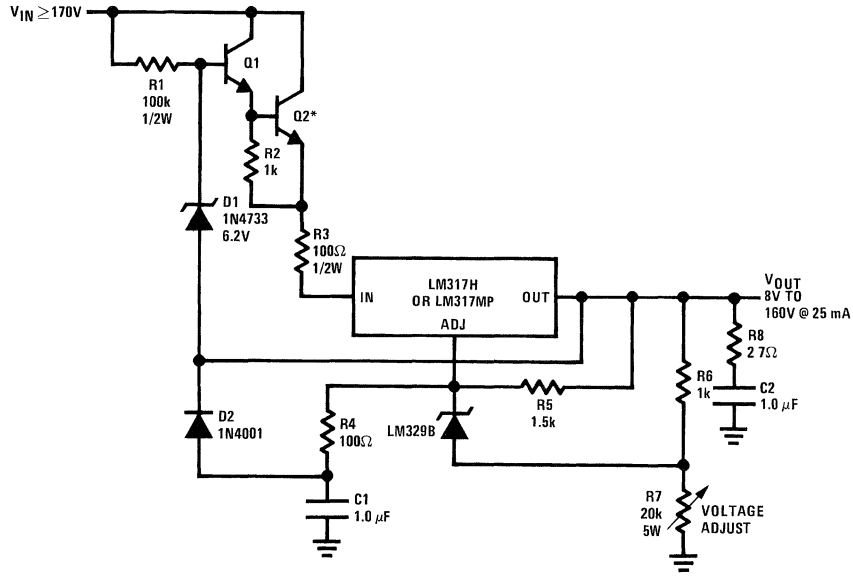
FIGURE 1. Basic High Voltage Regulator

An improved approach is shown in *Figure 2*. Here an LM329B 6.9V zener reference has been stacked in series with the LM317's internal reference. This both improves temperature stability, since the LM329B has a guaranteed TC of ±20 ppm/°C, and improves regulation, because more loop gain is available from the LM317.

These techniques can be extended for higher output voltages and/or currents by either using better high voltage transistors or cascoding or paralleling (with appropriate emitter ballasting resistors) several transistors. The output short

High Voltage Adjustable Power Supplies (Continued)

circuit current, determined by R3, must be within Q2's safe area of operation so that secondary breakdown cannot occur.



Q1, Q2 NSD134 or similar
C1, C2 1 μF, 200V MYLAR
*Heat Sink

FIGURE 2. Precision High Voltage Regulator

Add Kelvin Sensing and Parallel Capability to 3-Terminal Regulators

National Semiconductor
Linear Brief 51
Michael Maida

Paralleling of 3-terminal regulators is generally not recommended because the devices do not share current equally. If, for instance, you try to make a 3 amp regulator using three 1 amp regulators, the device with the highest output could be carrying 2.5 amps in a current limit mode The regulator with the second highest output would be carrying only 0.5 amps, and the third regulator would be totally off. The reliability of such a system is poor because of the combination of high temperature and high current in the first regulator. A simple way to improve sharing is to insert a low value resistor in series with each output. The problem with this approach is that load regulation is very poor if the resistors are made large enough to ensure adequate sharing.

A new technique for current sharing overcomes the load regulation problem and, as an added bonus, provides remote sensing capability not available in the standard 3-terminal regulators. This is a great advantage when the regulators must be mounted off-card with their outputs fed through a connector. Total cost of added components is less than 50¢.

Figure 1 shows the new Kelvin sense scheme using the LM338 5 amp adjustable regulator. A1 forces a voltage drop across R3 equal to the voltage across the parasitic resistance, r_s. The current through R3 flows into the output of A1 and out the negative supply pin. This creates a voltage drop across R4 just equal to the voltage across r_s, cancelling the effect of r_s on load regulation There is an error in V_{OUT} created by the quiescent current of A1, but for a 5V output, this error is only about 0.7%. Voltage loss across r_s must be limited to 300 mV to avoid current limiting in A1. If larger drops must be accommodated, R3 and R4 will have to be increased. C1 is necessary only if intermediate values of capacitance (2 µF–20 µF) are put directly across the load. Any of the positive adjustable regulators may be used in place of the LM338.

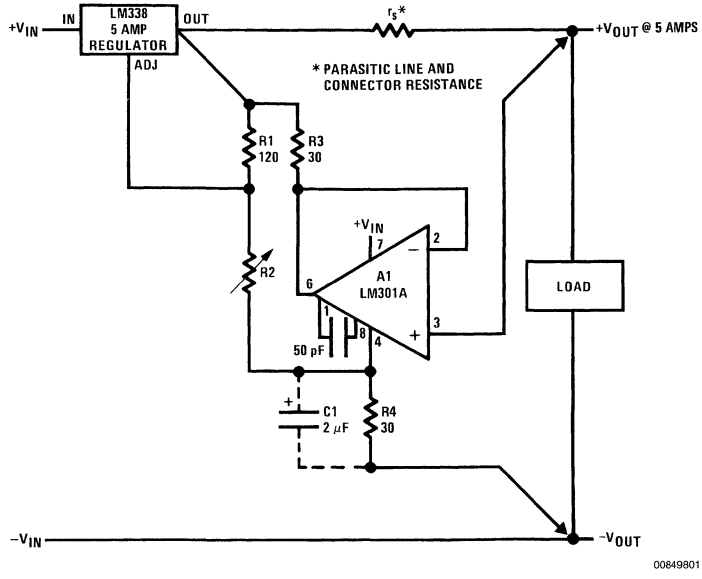


FIGURE 1.

Figure 2 combines Kelvin sensing with paralleling, where the voltage loss across the current sharing resistors is corrected by the sensing connection. r_{s1} through r_{s3} are equal lengths of #22 gauge lead wire which act as ballasting resistors. These resistors can be kept small because LM338 adjustment pins are paralleled, forcing the outputs to track to within about 60 mV. r_{s4} consists of the parasitic resistance of any additional output lead plus connector loss. The total loss for r_{s4} may be up to 0.25V without loss of proper Kelvin sensing. Note that if U1 has the lowest reference voltage of the three regulators, full Kelvin sensing might not become effective until output current has increased above a threshold value of several amps. If this is undesirable, the adjustment pin of U1 may be connected to a 5Ω tap on R1, increasing its effective reference voltage by 50 mV. The current load for U1 would be 1.5 amps higher, however.

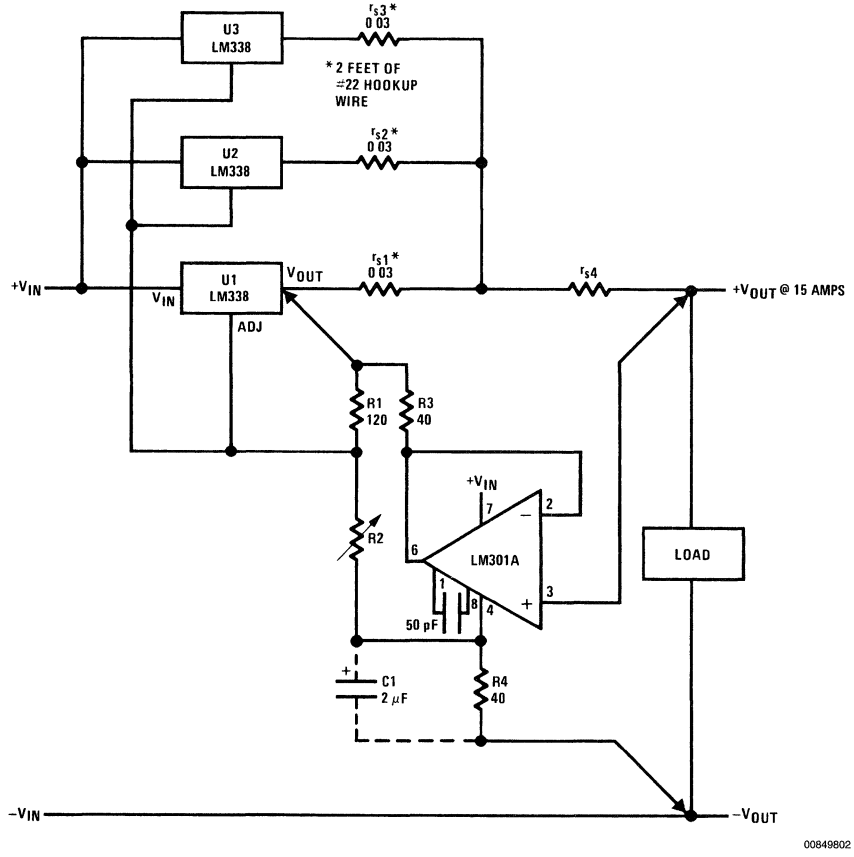

U3
LM338
r_{s3}*
0.03
*2 FEET OF
#22 HOOKUP
WIRE
U2
LM338
r_{s2}*
0.03
U1
LM338
V_{IN}
V_{OUT}
ADJ
r_{s1}*
0.03
r_{s4}
+V_{IN}
+V_{OUT} @ 15 AMPS
R1
120
R3
40
R2
+V_{IN}
LM301A
LOAD
50 pF
C1
2 μF
R4
40
−V_{IN}
−V_{OUT}
00849802

FIGURE 2.

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