National Semiconductor

June 1994

DP84902
1,7 Encoder/Decoder Circuit

General Description

The DP84902 is designed to perform the encoding and decoding for disk memory systems. It is designed to interface directly with Integrated Read Channel Products (such as National Semiconductor's DP84910) and with Disk Data Controller Products with a 2-bit NRZ interface (such as National Semiconductor's Advanced Disk Controllers). This Encoder/Decoder (ENDEC) circuit employs a 2/3 (1,7) Run Length Limited (RLL) code type and supports the hard sectored format.

The DP84902 has the option of selecting either TTL or ECL compatible code output to interface with preamplifiers commonly used in high data rate applications. This is accomplished by the setting of a bit in the control register.

The ENDEC also includes write data precompensation control circuitry which detects the need for write precompensation. This circuitry issues early and late output signals necessary for precompensation. The precompensation information is generated against a 2T pattern. The precompensation circuitry can be bypassed by the setting of a bit in the control register.

A control reigster is included to configure the ENDEC and to select device operation options such as output code inversion, differential code output, bypassing of the encoder, and the use of an internal write clock.

The DP84902 is available in 20-pin SO and 20-pin SSO packages.

Features

- Operates at 2-bit Non-Return to Zero (NRZ) Data Rates up to 50 Mbits/second
- Single +5V Power Supply Operation
- Low Power Dissipation when TTL compatible code output is selected. 150 mW at 50 Mbits/second NRZ Rate
- TTL Compatible Inputs and Outputs
- ECL Compatible Code Outputs (patented) are control register selectable
- Two-bit NRZ Interface
- Supports Write Data Precompensation with Early and Late output signals
- Selectable use of either an Internal or External Write Clock
- Power Down Mode Included
- DC-Erasure is available to support Analog Flaw Mapping Testing
- Bypass Mode available which permits Un-Encoded Test Patterns to be issued at the CODEOUT Pin

Block Diagram

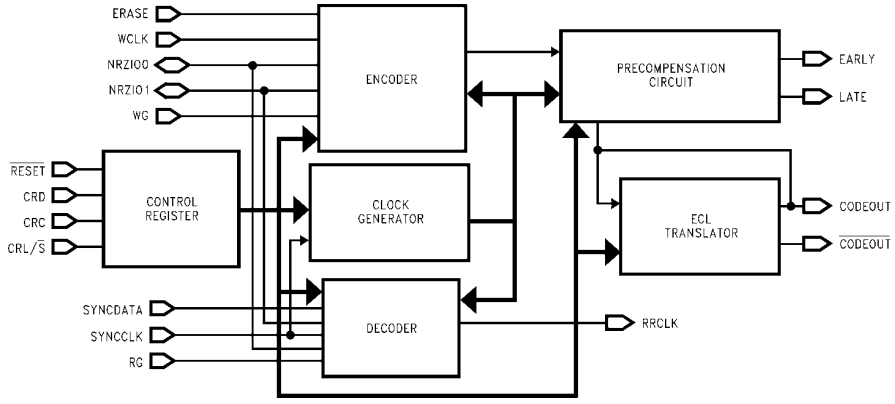

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FIGURE 1. DP84902 ENDEC Block Diagram

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RRD-B30M105/Printed in U. S. A.

Connection Diagram

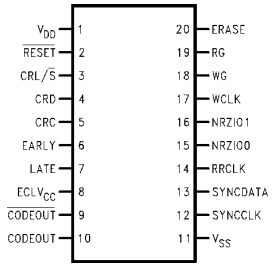

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FIGURE 2. DP84902 Pinout

Order Number DP84902M or DP84902MS
See NS Package Number M20B or MSA20

Pin Descriptions

Symbol	Pin #	Functional Description
Power Supply and Ground Pins		
$ECLV_{CC}$	8	$ECLV_{CC}$ Supply Pin: 5V ±10%
V_{DD}	1	V_{DD} Supply Pin: 5V ± 10%
V_{SS}	11	V_{SS}: Ground reference
Input Pin Descriptions		
CRC	5	**CONTROL REGISTER CLOCK:** Positive-edge-active control register clock input.
CRD	4	**CONTROL REGISTER DATA:** Control register data input
CRL/$\overline{S}$	3	**CONTROL REGISTER LATCH/$\overline{SHIFT}$:** A logical low state applied to this input allows the CONTROL REGISTER CLOCK input to clock data into the control register's shift register via the CONTROL REGISTER DATA input. A logical high state latches the data into a bank of latches and issues the information to the appropriate circuitry within the ENDEC.
ERASE	20	**ERASE:** This active high input is used while in the write mode to force a logical low at the CODEOUT output (or a logical high if CODEOUT is inverted). This is useful to blank out (DC erase which issues no transitions) a track for analog flaw map tesing.
$\overline{RESET}$	2	**$\overline{RESET}$:** A logical low level applied to this input forces the ENDEC to a power-on-reset state, and presets its control register to predetermined operating setup conditions. During normal operation, this pin must be held at a logical high level.
RG	19	**READ GATE:** This input accepts a mode control signal from the controller for the decoder. It permits the reading of data from the disk when at a logical high level. It inhibits reading and resets the decoder state machine when at a logical low level. There are no set-up or hold timing requirements for the enabling or disabling of this input.
SYNCCLK	12	**SYNCHRONIZED CLOCK:** This input accepts the code rate (1.5F) synchronized clock signal from the read channel's data synchronizer. This signal is used to clock the synchronized data into the decoder on the negative edge of SYNCCLK in the read mode and is the source clock for clocking codeout data from the encoder during the write mode.
SYNCDATA	13	**SYNCHRONIZED DATA:** This input accepts the synchronized data signal, MSB first, from the read channel's data synchronizer for the decoder's use.
WCLK	17	**WRITE CLOCK:** This input is used only in the external write clock mode. The write clock signal (Note 1) from the controller is used to strobe the NRZ input data into the ENDEC. The write clock signal from the controller must be the RRCLK echoed by the controller. If the external write clock mode is not selected, this pin should be tied to V_{DD} or V_{SS}.
WG	18	**WRITE GATE:** This input accepts a mode control signal from the controller for the encoder. It permits the writing of a header and data to the disk when at a logical high level. It inhibits writing and resets the encoder state machine when at a logical low level. There are no set-up or hold timing requirements for the enabling or disabling of this input.

Pin Descriptions (Continued)

Symbol	Pin #	Functional Description
Output Pin Descriptions		
CODEOUT	10	**(1,7) RLL CODE OUTPUT:** This output issues encoded data, MSB first, to be written to the disk. The control register controls various attributes of this output. It can be configured either as a TTL or ECL compatible output. In the TTL mode, the sense of the output can be selectively inverted to allow the active edge to be either the positive or negative transition and can also be put into a high impedance state (TRI-STATE®) which allows the multiplexing of this pin with another device or pin. The precompensation circuitry can be bypassed. The encoder can also be bypassed thus permitting uncoded test patterns to be issued from this pin.
$\overline{\text{CODEOUT}}$	9	**(1,7) RLL COMPLEMENTARY CODE OUTPUT:** This output is the complement of the ECL differential CODEOUT output pin. It issues encoded data to be written to the disk. It is enabled as an ECL output by a control register bit. If the TTL mode is selected (by a control register bit), this pin will be in a high impedance state (TRI-STATE).
EARLY	6	**EARLY PRECOMPENSATION OUTPUT:** This pin is the early precompensation output. It issues a logical high level to indicate that early precompensation is needed. This signal is used by National Semiconductor Integrated Read Channel Products, such as the DP8492, to precompensate the final coded data before it goes to the read/write circuit.
LATE	7	**LATE PRECOMPENSATION OUTPUT:** This pin is the late precompensation output. It issues a logical high level to indicate that late precompensation is needed. This signal is used by National Semiconductor Integrated Read Channel Products, such as the DP8492, to precompensate the final coded data before it goes to the read/write circuit.
RRCLK	14	**READ/REFERENCE CLOCK:** This output issues read clock to the controller at all times (Note 1). This signal is used to clock decoded NRZ data into the controller in the read mode (READ CLOCK) and is to be echoed back to the ENDEC by the controller in the write mode for use as a write clock (REFERENCE CLOCK) if external write clock mode is selected in the control register.
Input/Output Pin Descriptions		
NRZIO0	15	**LEAST SIGNIFICANT BIT NRZ INPUT/OUTPUT:** This I/O pin represents the Least Significant Bit (LSB) of NRZ data. As an input, it accepts the NRZ LSB data signal from the controller. Data is strobed into the ENDEC on the positive-edge of the WRITE CLOCK (if external write clock mode is selected in the control register), encoded and written to the disk in (1,7) format. This NRZ input must be low while the preamble and address mark fields are being written. This pin is also used to transfer un-encoded test patterns to the CODEOUT pin. As an output, it issues the decoded NRZ LSB data to the controller during a read operation. NRZ output data will be clocked into the controller on the positive-edge of the READ/REFERENCE CLOCK (RRCLK).
NRZIO1	16	**MOST SIGNIFICANT BIT NRZ INPUT/OUTPUT:** This I/O pin represents the Most Significant Bit (MSB) of NRZ data. As an input, it accepts the NRZ MSB data signal from the controller. Data is strobed into the ENDEC on the positive-edge of the WRITE CLOCK (if external write clock mode is selected in the control register), encoded, and written to the disk in (1,7) format. This NRZ input must be held low while the preamble and address mark fields are being written. As an output, this pin issues the decoded NRZ MSB data to the controller during a read operation. The decoded NRZ output data will be clocked into the controller on the positive-edge of the READ/REFERENCE CLOCK (RRCLK).

Note 1: With the code rate at 1.5F, the effective NRZ data rate is 1F. Since this chip employs a 2-bit NRZ interface, the write (WCLK) and read/reference (RRCLK) clocks are 0.5F.

DC and AC Device Specifications

Absolute Maximum Ratings (Note)

Note: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" tables are not guaranteed at these ratings. The "operating conditions" table will define the conditions for actual device operation.

Supply Voltage 7V
TTL Input Maximum Voltage 7V
Maximum Output Voltage 7V
ESD Susceptibility (Note 1) 2000V

Note 1: Human Body model used. (100 pF through 1.5 kΩ)

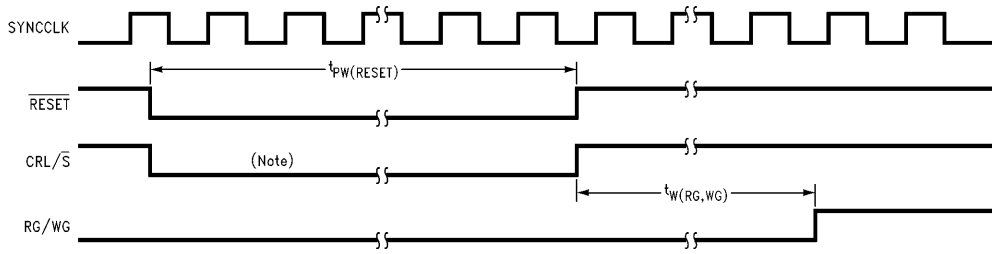
General Operating Conditions are guaranteed over supply voltage and operating ambient temperature ranges unless otherwise specified.

Symbol	Parameter		Min	Typ (Note 1)	Max	Units	Test
V_{DD}, $ECLV_{CC}$	Supply Voltage		4.5	5	5.5	V	N/A
T_A	Operation Ambient Temperature		0		70	°C	N/A
T_S	Storage Temperature		−65		150	°C	N/A
C_{LOAD}	Capacitive Load on any Output	ECL Output			10	pF	N/A
		TTL Output			15		
I_{OH}	High Logic Level Output Current (CMOS Logic Outputs Only)				−8	mA	(Note A)
I_{OL}	Low Logic Level Output Current (CMOS Logic Outputs Only)	EARLY, LATE			6	mA	(Note A)
		All Others			8		(Note A)
V_{IH}	High Logic Level Input Voltage		2			V	(Note A)
V_{IL}	Low Logic Level Input Voltage				0.8	V	(Note A)
f_{NRZ}	NRZ Transfer Rate Operating Frequency		5		50	Mb/s	(Note A)
f_{SCLK}	SYNCCLK Operating Frequency		7.5		75	MHz	(Note A)
$t_{PW(RESET)}$	RESET Pulse Width (negative) (See *Figure 3*)		5			SYNCCLK PERIODS	(Note A)
$t_{PW(RG, WG)}$	RG or WG Wait Time after Power Down or Reset with Respect to Positive Edge of CRL/$\overline{S}$ Pin. (See *Figure 3*)		10			SYNCCLK PERIODS	(Note B)

Note 1: Typical values are specified at 25°C and 5V supply.

Note A: This parameter is guaranteed by outgoing testing.

Note B: The limit values have been determined by characterization data. No outgoing tests are performed.



Note: Power down mode selected in control register (see Table I).

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FIGURE 3. Reset Pin and Power Down Timing Diagram

Control Register Operating Conditions are guaranteed over operating conditions (see table) unless otherwise specified.

Symbol	Parameter	Min	Typ (Note 1)	Max	Units	Test
$t_{PW(CRC)}$	CRC Pulse Width (positive or negative) (see *Figures 4* and *9*)	14			ns	(Note A)
$t_{SU(CRD)}$	CRD Setup Time with respect to CRC (positive edge) (see *Figures 4* and *8*)	5			ns	(Note A)
$t_{H(CRD)}$	CRD Hold Time with respect to CRC (positive edge) (see *Figures 4* and *8*)	5			ns	(Note A)
$t_{SU(CRL/\overline{S})}$	CRL/$\overline{S}$ Setup Time with respect to CRC (positive edge) (see *Figures 4* and *8*)	5			ns	(Note A)
$t_{H(CRL/\overline{S})}$	CRL/$\overline{S}$ Hold Time with respect to CRC (positive edge) (see *Figures 4* and *8*)	5			ns	(Note A)

Note 1: Typical values are specified at 25°C and 5V supply.

Note A: This parameter is guaranteed by outgoing testing.

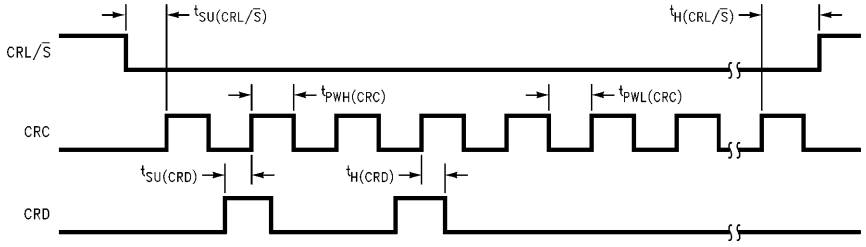

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FIGURE 4. Control Register Timing Diagram

DC Electrical Characteristics are guaranteed over operating conditions (see table) unless otherwise specified.

Symbol	Parameter		Conditions		Min	Typ (Note 1)	Max	Units	Test
V_{OH}	High Logic Level Output Voltage		(Note 2)	ECL Outputs	0.815 $ECLV_{CC}$		0.878 $ECLV_{CC}$	V	(Note A)
			V_{DD} = Min I_{OH} = 20 μA	TTL Outputs	V_{DD} − 0.1				(Note A)
			V_{DD} = Min, I_{OH} = Max		3.5				(Note A)
V_{OL}	Low Logic Level Output Voltage		(Note 2)	ECL Outputs	0.575 $ECLV_{CC}$		0.705 $ECLV_{CC}$	V	(Note A)
			V_{DD} = Min, I_{OL} = 20 μA	TTL Outputs			0.1		(Note A)
			V_{DD} = Min, I_{OL} = Max				0.4		(Note A)
I_{IN}	Input Current		V_{DD} = $ECLV_{CC}$ = Max		−20		20	μA	(Note A)
I_{OZ}	TRI-STATE Output Current		V_{DD} = $ECLV_{CC}$ = Max		−20		20	μA	(Note A)
I_{DD}	Supply Current	TTL Code Output	V_{DD} = Max, f_{NRZ} = 50 Mb/s, $ECLV_{CC}$ = Max			30	50	mA	(Note A)
		ECL Code Output (Write Mode)				70	95		(Note A)
		ECL Code Output (Non-Write Mode)				30	50		(Note A)
$I_{DD(PD)}$	Supply Current in Power Down Mode		V_{DD} = $ECLV_{CC}$ = Max			1	1.5	mA	(Note A)

Note 1: Typical values are specified at 25°C and 5V supply.

Note 2: Assumes output is driving a 50 kΩ load.

Note A: This parameter is guaranteed by outgoing testing.

AC Electrical Characteristics—Write Mode are guaranteed over operating conditions (see table) unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units	Test
$t_{SU(NRZIO(0,1))}$	NRZIO(0,1) Setup Time w.r.t. WCLK (positive edge) (see *Figures 5* and *8*) (Note 3)		8			ns	(Note A)
$t_{H(NRZIO(0,1))}$	NRZIO(0,1) Hold Time w.r.t. WCLK (positive edge) (see *Figures 5* and *8*) (Note 3)		5			ns	(Note A)
t_{PD1}	Propagation Delay of Encoder, WCLK (positive edge) to CODEOUT (positive edge) (Note 2) (see *Figures 5* and *7*)	Precomp. Enabled		5		WCLK PERIODS	(Note B)
t_{PD2}	Propagation Delay of Encoder, WCLK (positive edge) to CODEOUT (positive edge) (Note 2) (see *Figures 5* and *7*)	Precomp. Disabled		4		WCLK PERIODS	(Note B)
t_{PD3}	Propagation Delay of Encoder, WG (positive edge) to First Valid CODE-OUT Output (see *Figures 5* and *7*)	Precomp. Enabled		19		SYNCCLK PERIODS	(Note B)
t_{PD4}	Propagation Delay of Encoder, WG (positive edge) to First Valid CODE-OUT Output (see *Figures 5* and *7*)	Precomp. Disabled		14		SYNCCLK PERIODS	(Note B)
$t_{SU(EARLY)}$	EARLY Setup Time w.r.t. CODE-OUT (positive edge) or $\overline{\text{CODEOUT}}$ (negative edge) (see *Figures 5* and *8*)		6			ns	(Note A)
$t_{H(EARLY)}$	EARLY Hold Time w.r.t. CODEOUT (positive edge) or $\overline{\text{CODEOUT}}$ (negative edge) (see *Figures 5* and *8*)		6			ns	(Note A)
$t_{SU(LATE)}$	LATE Setup Time w.r.t. CODEOUT (positive edge) or $\overline{\text{CODEOUT}}$ (negative edge) (see *Figures 5* and *8*)		6			ns	(Note A)
$t_{H(LATE)}$	LATE Hold Time w.r.t. CODEOUT (positive edge) or $\overline{\text{CODEOUT}}$ (negative edge) (see *Figures 5* and *8*)		6			ns	(Note A)
$t_{PW(WCLK)}$	WCLK Pulse Width (High or Low) (see *Figures 5* and *9*)		10			ns	(Note A)

Note 1: Typical values are specified at 25°C and 5V supply.

Note 2: A WCLK period is twice the NRZ rate period since a 2-bit interface is used.

Note 3: This specification is valid for either internal or external WCLK mode of operation.

Note A: This parameter is guaranteed by outgoing testing.

Note B: This specification is provided for information only.

AC Electrical Characteristics—Write Mode

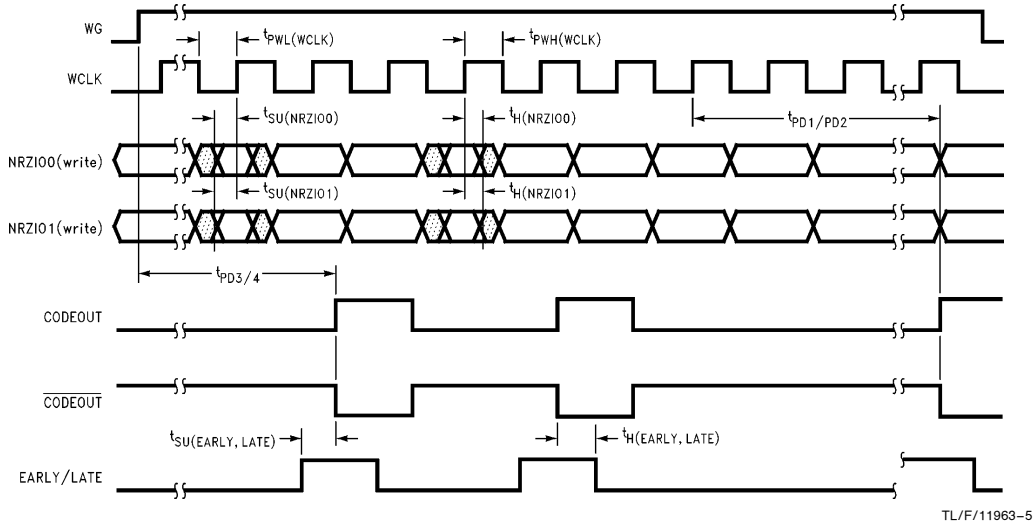

FIGURE 5. Write Timing Diagram

AC Electrical Characteristics—Read Mode are guaranteed over operating conditions (see table) unless otherwise specified.

Symbol	Parameter	Min	Typ (Note 1)	Max	Units	Test
$t_{SU(SYNCDAT)}$	SYNCDATA Setup Time w.r.t. SYNCCLK (negative edge) (see *Figures 6* and *8*)	4	1		ns	(Note A)
$t_{H(SYNCDAT)}$	SYNCDATA Hold Time w.r.t. SYNCCLK (negative edge) (see *Figures 6* and *8*)	1	0		ns	(Note A)
$t_{SU(NRZIO(0,1))}$	NRZIO(0,1) Setup Time w.r.t. RRCLK (positive edge) (see *Figures 6* and *8*)	9	19		ns	(Note A)
$t_{H(NRZIO(0,1))}$	NRZIO(0,1) Hold Time w.r.t. RRCLK (positive edge) (see *Figures 6* and *8*)	9	17		ns	(Note A)
t_{PD5}	Propagation Delay of Decoder, SYNCCLK (negative edge) to RRCLK (Note 2) (see *Figures 6* and *7*)	2			RRCLK PERIODS	(Note B)
$t_{PW(RRCLK)}$	RRCLK Pulse Width (High or Low) (see *Figures 6* and *9*)	13	20		ns	(Note A)

Note 1: Typical values are specified at 25°C and 5V supply.

Note 2: A RRCLK period is twice the NRZ rate period since a 2-bit interface is used.

Note A: This parameter is guaranteed by outgoing testing.

Note B: The limit values have been determined by characterization data. No outgoing tests are performed.

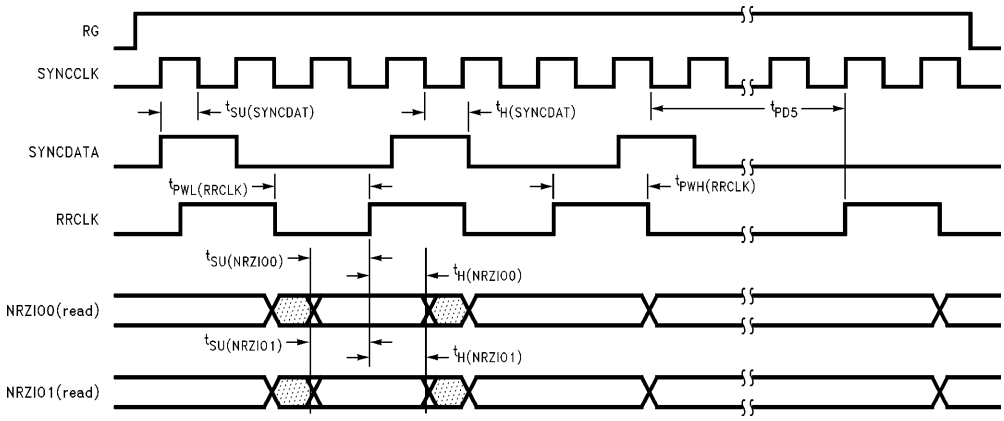

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FIGURE 6. Read Timing Diagram

AC Electrical Characteristics—General are guaranteed over operating conditions (see table) unless otherwise specified.

Symbol	Parameter	Min	Typ (Note 1)	Max	Units	Test
t_{ECLON}	ECL Section Turn On Time w.r.t. CRL/$\overline{S}$ pins (positive edge) (see *Figures 6.5* and *7*) (Note 2)		2	5	μs	(Note B)
t_{ECLOFF}	ECL Section Turn Off Time w.r.t. CRL/$\overline{S}$ pins (positive edge) (see *Figures 6.5* and *10*) (Note 3)		2	4	μs	(Note B)
t_{WRTON}	ECL Output Enabling Time w.r.t. WG Positive Edge (see *Figure 6.5*)		15	50	ns	(Note A)
t_{WRTOFF}	ECL Output Disabling Time w.r.t. WG negative edge (see *Figure 6.5*)		20	50	ns	(Note A)

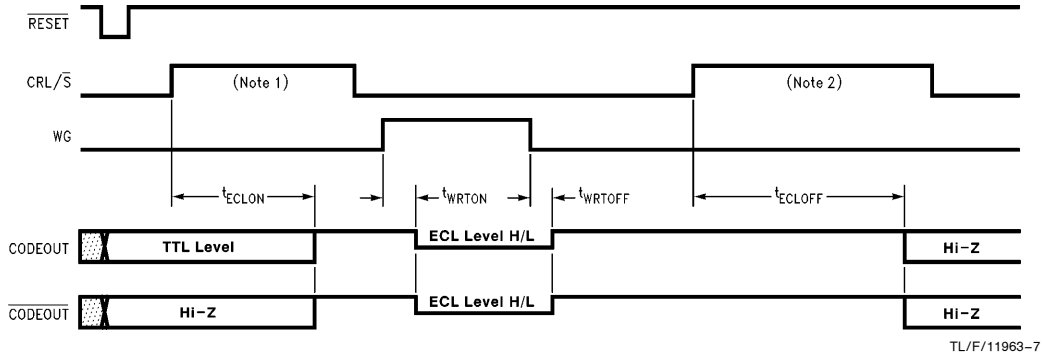
Note 1: Typical values are specified at 25°C and 5V supply.

Note 2: The start and stop measurement voltage points are 1.3V.

Note 3: The start measurement voltage point is 1.3V and the stop measurement voltage point is V_{OL} + 0.3V.

Note A: This parameter is guaranteed by outgoing testing.

Note B: The limit values have been determined by characterization data. No outgoing test are performed.



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Note 1: For t_{ECLON}, the ECL output mode is selected in the control register (see Table I).

Note 2: For t_{ECLOFF}, the power down mode is selected in the control register (see Table I).

FIGURE 6.5. ECL Code Write Timing Diagram

AC Electrical Characteristics—Waveforms

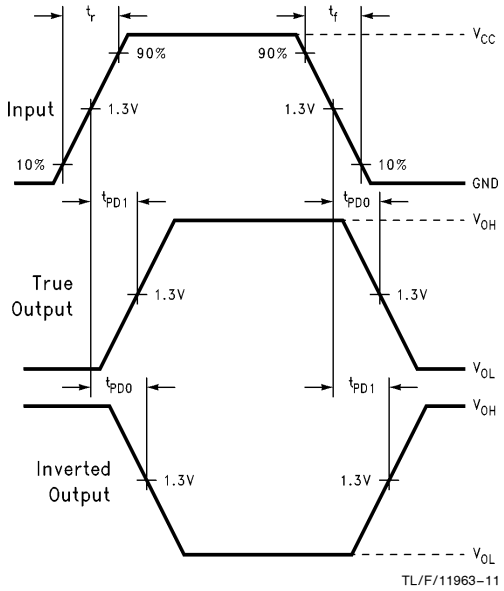

FIGURE 7. Propagation Delay Waveforms

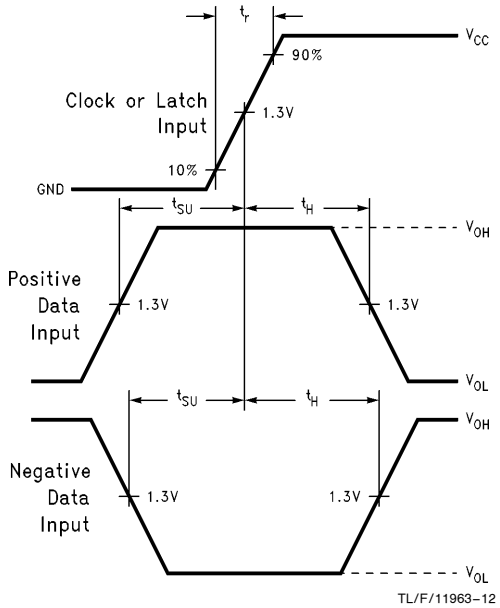

FIGURE 8. Setup and Hold Time Waveforms

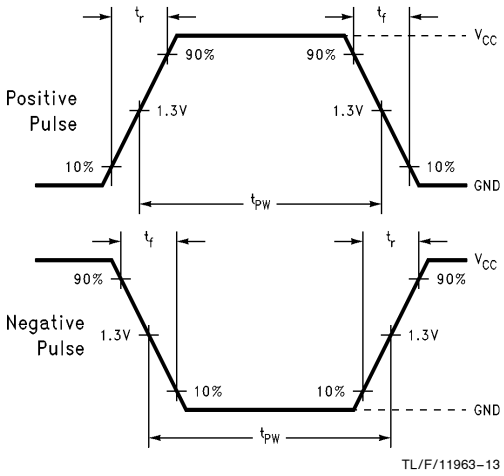

FIGURE 9. Input or Output Pulse Width Waveforms

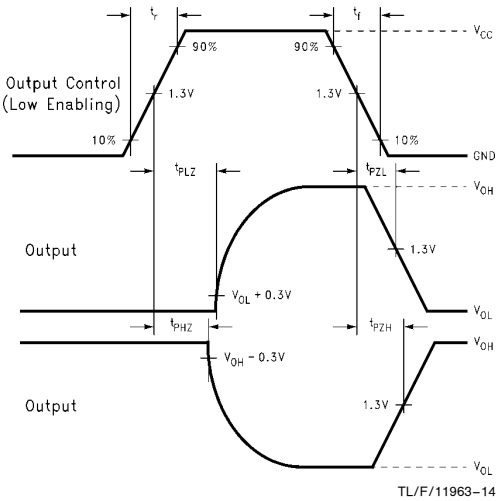

FIGURE 10. TRI-STATE Output Enable and Disable Waveforms

Functional Description

The Encoder/Decoder (ENDEC) translates NRZ data to and from the (1,7) RLL format; receives and transfers NRZ data in a 2-bit format; generates code output that can be made either TTL or ECL compatible; indicates the need to precompensate write data and issues READ/REFERENCE CLOCK (RRCLK). READ/REFERENCE CLOCK multiplexing is done without glitches.

Control Register

The control register is comprised of a fourteen-bit serial shift register and a fourteen-bit latch *(Figure 11).* Information is strobed into the shift register via the CONTROL REGISTER DATA (CRD) input on the positive edge of the CONTROL REGISTER CLOCK (CRC) input with the CONTROL REGISTER LATCH/SHIFT BAR (CRL/$\overline{S}$) pin at a logical low state. The information is parallel transmitted to the latch bank and the ENDEC when the CRL/$\overline{S}$ input is taken to a logical high state. The control register truth table (Table I) describes the functions controlled by each bit in the control register. The bit at the right of each bit stream (13) in the table is the first bit entered into the shift register.

Two bits of the control register (bits 1,2) control the power down option. The other bits of the control register determine various aspects of the ENDEC's outputs. Bit4 inverts the sense of the CODEOUT output data. Bit 6 changes CODEOUT from a TTL compatible output to a ECL (differential) compatible output. Bits 7, 8 controls bypass selection. No bypass can be selected (bit7 = bit8 = 0), the precompensation circuit can be bypassed (bit7 = 0, bit8 = 1) and the CODEOUT pin can be tri-stated (bit7 = bit8 = 1). Bit 9 permits the use of an internal write clock. Bit 10 must be set to 1 for normal operation. Bit 11 puts the encoder in a bypass mode if bit 7 and bit 8 are also set to 0. In this mode, the data received at the NRZIO0 pin will pass through the encoder to the CODEOUT pin. All of the reserved bits (0, 3, 5, 12, 13) are to be programmed at a logical low level.

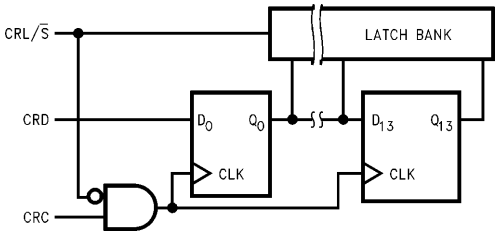

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FIGURE 11. CTRL Register Block Diagram

TABLE I. Control Register Truth Table

BIT STREAM														Function Selected
LSB													MSB	
0	1	2	3	4	5	6	7	8	9	10	11	12	13	
0	x	x	x	x	x	x	x	x	x	x	x	x	x	Reserved Bit
x	0	0	x	x	x	x	x	x	x	x	x	x	x	Normal Operation
x	1	1	x	x	x	x	x	x	x	x	x	x	x	Power Down
x	x	x	0	x	x	x	x	x	x	x	x	x	x	Reserved Bit
x	x	x	x	1	x	x	x	x	x	x	x	x	x	Inverts CODEOUT Data
x	x	x	x	x	0	x	x	x	x	x	x	x	x	Reserved Bit
x	x	x	x	x	x	1	x	x	x	x	x	x	x	Differential CODEOUT Data
x	x	x	x	x	x	x	0	0	x	x	x	x	x	No Bypass
x	x	x	x	x	x	x	0	1	x	x	x	x	x	Bypass Precompensation Circuit
x	x	x	x	x	x	x	1	1	x	x	x	x	x	TRI-STATE CODEOUT Pin
x	x	x	x	x	x	x	x	x	1	x	x	x	x	Use Internal Write Clock
x	x	x	x	x	x	x	x	x	x	1	x	x	x	Normal Operation
x	x	x	x	x	x	x	0	0	x	x	1	x	x	Bypass Encoder
x	x	x	x	x	x	x	x	x	x	x	x	0	x	Reserved Bit
x	x	x	x	x	x	x	x	x	x	x	x	x	0	Reserved Bit

Functional Description (Continued)

1,7 RLL CODE

The (1,7) code used is based on US patent #4,413,251 via cross-licensing with International Business Machines Corporation (IBM®). Table II summarizes the decoding method used for this device. Nine SYNCDATA bits are used to decode the middle three SYNCDATA bits of the nine bit stream into two NRZ output bits, a Most Significant Bit (MSB) and a Least Significant Bit (LSB). Bit 8 is the first SYNCDATA bit shifted into the decoder. The left-most column of the table (''NRZIO OUTPUT BIT'') identifies whether the row represents the NRZ MSB or LSB. This table identifies the combinations which will produce a high logical level. If the code bits do not match the table, a low logical state will be produced. Table III represents the same decoding operation in a different format.

Table IV summarizes the state diagram used by this device to encode NRZ data into 1,7 coded data. The table is read from left to right during the encoding process. To encode data the ''CURRENT STATE'' (column 1) must be determined first.

The initial ''CURRENT STATE'' is always zero. This ''CURRENT STATE'' selects a group of four rows in the table. The two NRZ input bits determine the exact row, within the group, to be used. Once the row is identified, follow the row to the right of the ''NRZIO'' column to locate the coded output, in the ''1,7 OUT'' column. Continue by identifying the next state in the ''NEXT STATE'' column immediately to the right of the ''1,7 OUT'' column. The number located in this column is used as the ''CURRENT STATE'' for the next two NRZ input bits. This procedure is continued until all the NRZ data is encoded.

TABLE II. Decoding State Table

NRZ OUTPUT BIT	SYNCDATA (CODE BITS)								
	8	7	6	5	4	3	2	1	0
NRZIO0 (LSB) = 1	x	x	x	1	x	x	x	x	x
	x	x	x	x	0	0	x	x	x
NRZIO1 (MSB) = 1	x	x	x	x	x	1	x	x	x
	x	x	0	0	0	x	x	x	x
	x	x	x	x	x	x	0	0	0

TABLE III. Decoding State Table

Encoded Read Data (SYNCDATA)									Decoded Data (NRZ Data)	
Previous			Present			Next				
Y1	Y2	Y3	Y1	Y2	Y3	Y1	Y2	Y3	D1	D2
MSB → LSB			MSB → LSB			MSB → LSB			MSB → LSB	
		0	0	0	0				1	1
		1	0	0	0	0	0	0	1	1
		1	0	0	0	0	0	1	0	1
		1	0	0	0	0	1	0	0	1
		1	0	0	0	1	0	0	0	1
		1	0	0	0	1	0	1	0	1
			0	0	1				1	0
			0	1	0	0	0	0	1	0
			0	1	0	0	0	1	0	0
			0	1	0	0	1	0	0	0
			0	1	0	1	0	0	0	0
			0	1	0	1	0	1	0	0
			1	0	0	0	0	0	1	1
			1	0	0	0	0	1	0	1
			1	0	0	0	1	0	0	1
			1	0	0	1	0	0	0	1
			1	0	0	1	0	1	0	1
			1	0	1				1	1

Functional Description (Continued)

TABLE IV. Encoding State Table

NRZIO			CODEOUT			
CURRENT STATE	MSB	LSB	1,7 OUT			NEXT STATE
0	0	0	0	1	0	0
0	0	1	0	1	0	2
0	1	0	0	1	0	4
0	1	1	0	1	0	3
1	0	0	0	0	0	0
1	0	1	0	0	0	2
1	1	0	0	0	0	4
1	1	1	0	0	0	3
2	0	0	1	0	0	0
2	0	1	1	0	0	2
2	1	0	1	0	0	4
2	1	1	1	0	0	3
3	0	0	1	0	1	0
3	0	1	1	0	1	1
3	1	0	1	0	1	4
3	1	1	1	0	0	1
4	0	0	0	0	1	0
4	0	1	0	0	1	1
4	1	0	0	0	1	4
4	1	1	0	1	0	1

Precompensation Outputs

The precompensation circuit in this ENDEC generates output data to be used externally to provide write precompensation. The precompensation truth table (Table V) demonstrates what outputs are expected per data sequence (bit stream). In the table, the bit which is being considered for precompensation is the target bit, T. This target bit is a logical high level. The location of data bits on either side of the target bit indicates the logic states of the precompensation outputs. No shift indicates that all the precompensation outputs are at a logical low level. The mention of a precompensation output in the ''FUNCTION'' column indicates that it is at a logical high while those not mentioned are at a logical low level.

TABLE V. Precompensation Truth Table

BIT STREAM MSB				LSB	FUNCTION
0	0	T	0	0	NO SHIFT
1	0	T	0	1	NO SHIFT
1	0	T	0	0	EARLY
0	0	T	0	1	LATE

The EARLY and LATE outputs need to be connected to inputs of a precompensation circuit to achieve write precompensation. Using the NSC DP8492 device as an example, the EARLY and LATE outputs of the ENDEC will be connected to the EARLY and LATE inputs to the DP8492, respectively.

Address Mark Mode

Hard Sectored Read Mode *(Figure 13)*

This ENDEC supports only a 3T preamble pattern. At the assertion of READ GATE, the decoder searches for 16 uninterrupted code pulses of (3T) preamble. Once the preamble counter has filled to a count of 16, an internal preamble detected signal is issued. It resets an internal state machine and initiates the phase synchronization process. Decoding of 1,7 data will begin after phase synchronization.

Hard Sectored Write Mode *(Figure 12)*

At the assertion of WRITE GATE with NRZIO inputs held low, the encoder issues (3T) preamble at the CODEOUT pin. Preamble will continue until the first non-zero NRZ input bit appears.

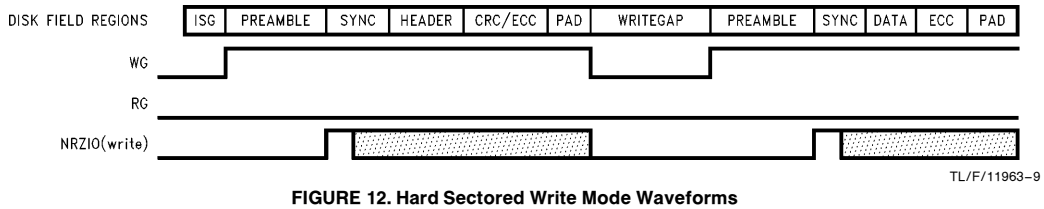

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FIGURE 12. Hard Sectored Write Mode Waveforms

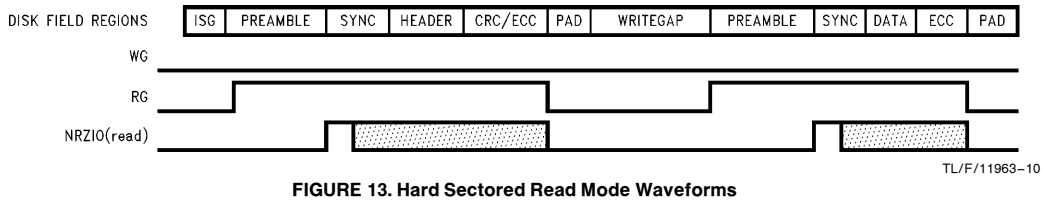

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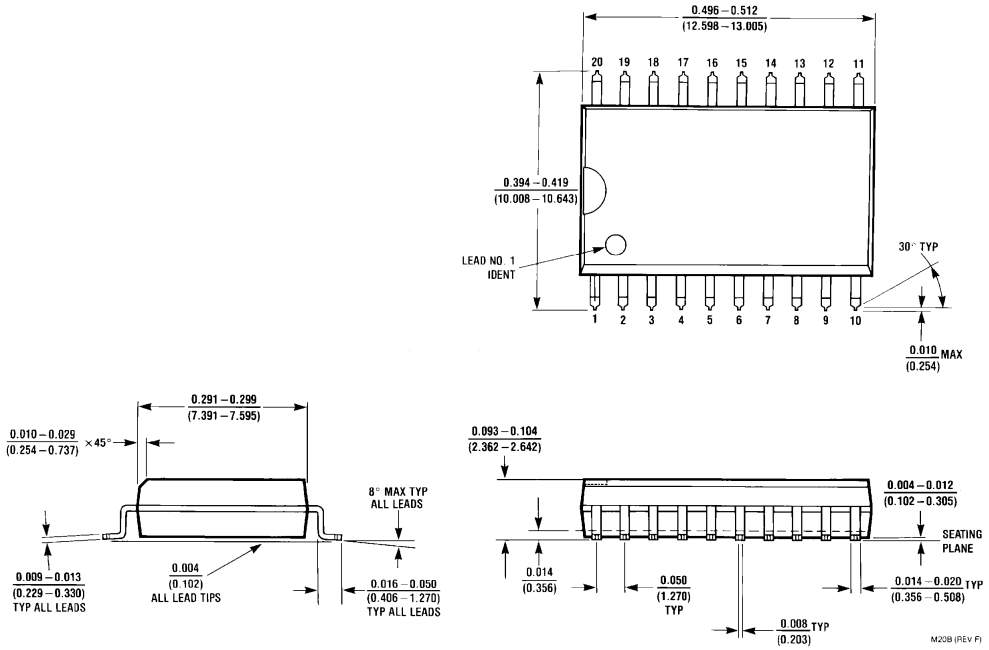
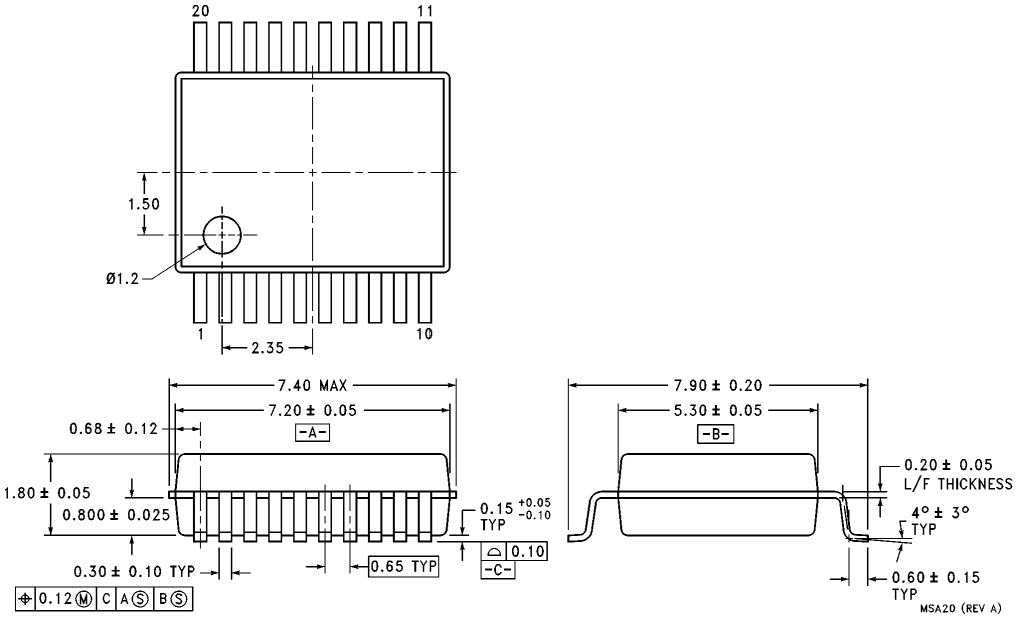
FIGURE 13. Hard Sectored Read Mode Waveforms

Physical Dimensions inches (millimeters)



20-Pin Small Outline Package
Order Number DP84902M
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)



20-Pin Shrink Small Outline Package
Order Number DP84902MS
NS Package Number MSA20

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