NCR 53C720 SCSI I/O Processor

NCR

Data Manual

Trademarks

NCR is the name and mark of NCR Corporation.

SCSI SCRIPTS is a registered trademark of NCR Corporation.

Additional Information

NCR 53C720 Programmer's Guide

NCR SCSI Engineering Note 831, Comparison of 53C720 to 53C710

SCSI Specifications

This data manual is not a SCSI specification. It assumes some prior knowledge of SCSI current and proposed standards. To obtain a copy of the proposed standard or background information on SCSI, write to:

ANSI

1430 Broadway

New York, NY 10018

(212) 642-4900

Ask for document number: X3.131 – 1986 (SCSI-1)

Global Engineering Documents

2805 McGaw

Irvine, CA 92714

(800) 854-7179 or (714) 261-1455

Ask for document number:

X3.131-198x (SCSI-2)

ENDL Publications

14426 Black Walnut Court

Saratoga, California 95070

(408) 867-6642

Document Name:

SCSI Bench Reference

SCSI Encyclopedia

Prentice Hall

Englewood Cliffs, New Jersey 07632

(201) 767-5937

Ask for document number: ISBN 0-13-796855-8

Docuemnt Name: (SCSI -Understanding the Small Computer System Interface).

REVISION RECORD		
Revision	**Date**	**Affected Pages/Remarks**
	May 91	First printing
1.0	August 91	2-1, 2-5, 3-1, 3-9, 3-10, 3-11,1 3-13, 4-3, 4-4, 4-5, 4-8,5-9, 5-14, 5-15, 5-17, 5-20, 5-22, 5-25, 5-28, 5-29, 5-30, 5-38

Table of Contents

Chapter 1
Introduction

Chapter 2
SCSI I/O Processor Description

Chapter 3
Functional Description

Chapter 4
Signal Descriptions

Chapter 5
Registers

Table of Contents (Continued)

Chapter 6
Instruction Set of the I/O Processor

Chapter 7
Electrical Specifications

Appendix A
53C720 Register Summary

Appendix B
53C720 Mechanical Drawing

Appendix C
Register Differences Between the 53C710 and 53C720

NCR Microelectronic Products Division Sales Locations

Chapter 1

Introduction

I/O Performance

The demands on today's I/O interfaces are being pushed by the increasing performance of personal computers and workstations. High powered CPUs, both CISC and RISC, only provide marginal system performance improvements if their I/O interfaces are not properly designed. Interrupt service routines, which often take an excess of several hundred microseconds to execute, can be a large source of performance degradation. Interrupts may be generated for exception conditions, I/O completion, I/O status save/restore, or accommodation of the myriad of options currently available in I/O definitions. Interrupts can be reduced by register polling; however, this can be time consuming and does not provide a complete solution for multitasking systems.

The Need for I/O Flexibility

Options in the SCSI bus protocol allow increased flexibility. The need for I/O flexibility is partially responsible for the popularity of the SCSI standard. I/O flexibility allows configuration of systems for a wide range of peripherals from high performance disk drives to hand held scanners.

Additionally, SCSI supports command queueing, asynchronous & synchronous data transfer protocols, caching controllers, and peer level communication. If not implemented properly, all of this flexibility can increase interrupts and negatively impact system performance.

A Better Solution

First generation (NCR 5380) SCSI devices are register oriented and require processor intervention to make the most fundamental protocol decisions. Users like the flexibility of these devices because the low level firmware interface provides specific information about the SCSI bus and improved testability of the SCSI device. First generation SCSI devices typically requires in excess of 4,000 lines of code to implement a SCSI-1 initiator.

Second generation (NCR 53C90) SCSI devices provide on-chip state machines allowing some complex bus sequences to be performed automatically, thus reducing protocol overhead. However, these devices have little decision making capability because the internal sequences are fixed in hardware or, in some cases, software. This generation of SCSI devices typically requires in excess of 2,500 lines of driver support software.

The flexibility of the SCSI bus has created a dilemma for system integrators and OEMs alike. The dilemma is determining whether first and second generation SCSI devices should be used as non-intelligent, stand alone devices or whether they should be integrated into intelligent host adaptor boards. Non-intelligent SCSI host ports or host bus adapters require a fair amount of processor intervention, but are inexpensive to implement.

Intelligent host adapters are more expensive than non-intelligent adapters. They provide slower decision making capabilities (typically using less powerful CPUs), experience interpretation delays (2-8 ms) to start any I/O, and suffer from interprocessor communication delays. Consequently, non-intelligent host adapters consistently outperform their intelligent counterparts in many systems.

With MIPs increasing in the system CPU, the delays caused by intelligent host adapter cards increase in severity. Two possible solutions would be to build more versatile (complex) sequences inside the SCSI components or to add additional CPU power to the intelligent host adapters. Both solutions are costly and do not adequately address the problem.

NCR 53C720

NCR Third Generation Products

To accommodate the flexibility requirements of the SCSI bus, reduce interrupts and control host adapter cost, an additional level of intelligence and integration is required. NCR offers third generation, programmable SCSI devices that make decisions based on SCSI bus phase changes, compare specific data values, and minimize interrupts.

NCR's third generation SCSI devices reduce interrupt service routine complexity by providing a unique status report for any interrupts that occur. A fully integrated DMA channel also allows full use of available host bus bandwidth. This is the key to overall I/O performance, given the current use of virtual memory schemes that require the ability to support scatter/gather memory operations without processor intervention.

NCR's 53C7X0 family of SCSI devices require only a few hundred lines of driver code. This code supports exception conditions and passes addresses of the user data buffer to the SCSI interface device.

Chapter 2

SCSI I/O Processor Description

General Description

The NCR 53C720 is the third member of the 53C7X0 family of intelligent, single-chip, third generation SCSI host adapters. A high performance SCSI core and an intelligent 16 or 32-bit bus master DMA core are integrated with a SCSI SCRIPTS processor to accommodate the flexibility requirements of not only SCSI-1 and SCSI-2, but future SCSI standards as well. In addition, the 53C720 solves the protocol overhead problems that have plagued all previous intelligent and non-intelligent adapter designs.

The 53C720 is designed to completely implement a multi-threaded I/O algorithm in either a workstation or file server environment, completely free of processor intervention except at the end of an I/O transfer. In addition, the 53C720 provides automatic relocation of SCRIPTS, and requires no dynamic alteration of SCRIPTS instructions at the start of an I/O operation. All of the SCRIPTS code may be placed on a PROM. The 53C720 allows easy firmware upgrades and is compatible with the 53C710.

The 53C720 supports four different host processor interfaces, or bus modes. Bus Mode 1 closely resembles the Motorola 68030 interface, and Bus Mode 2 closely resembles the Motorola 68040 interface. Bus Mode 3 closely resembles the Intel 80386SX interface; the 16-bit host interface should be enabled in this mode. Finally, Bus Mode 4 closely resembles the 80386DX interface. Bus Modes 1, 2 and 4 support both the Big and Little Endian byte ordering schemes and Bus Mode 3 supports Little Endian byte ordering, for a total of seven operating modes. The modes are selected by using the bus mode select pins (BS 2-0).

53C720 Features Summary

Performance

- Supports variable block size & scatter/gather data transfers
- Supports 16 and 32-bit word data bursts with variable burst lengths
- Memory-to-memory DMA transfers in excess of 33 Mbytes/sec
- Minimizes SCSI I/O start latency
- Performs complex bus sequences without interrupts including restore data pointers
- Unique interrupt status reporting – reduces ISR overhead
- High-speed async/sync wide SCSI bus transfers
  10 MB/S asynchronous
  20 MB/S synchronous
- Memory transfers in excess of 97 MB/S (@ 33 MHz)
- Cache-line burst mode
- 64-byte DMA FIFO

Integration

- Full 16 or 32-bit DMA bus master
- High performance wide SCSI core
- Integrated SCRIPTS processor
- Allows intelligent host adapter performance on a motherboard

Ease of Use

- Reduces SCSI development effort
- Support for Big and Little Endian environments
- Easily adapted to the SCSI Common Access Method (CAM)
- Compiler-compatible with existing 53C710 SCRIPTS

NCR 53C720

- Development tools and SCSI SCRIPTS provided
- All interrupts are maskable and pollable
- Supports wide SCSI, A or P cable, and up to sixteen devices
- Interfaces with seven different host processor busses, including Motorola (680X0 family) and Intel (80X86 family).
- Odd-byte block sizes are supported in conjunction with wide SCSI
- Three programmable SCSI timers: Select/Reselect, Handshake-to-Handshake, and General Purpose. The time-out period is programmable from 100 µs to greater than 1.6 seconds.

Flexibility

- High level programmer's interface (SCSI SCRIPTS)
- Allows tailored SCSI sequences to be executed from main memory or from a host adapter board.
- Flexible sequences to tune I/O performance or to adapt to unique SCSI devices
- Accommodates changes in the logical I/O interface definition
- Low level programmability (register oriented)
- Allows a target to disconnect and later reselect with no interrupt to the system processor
- Allows a multithreaded I/O algorithm to be executed in SCSI SCRIPTS with fast I/O context switching
- Allows relative jumps
- Allows indirect fetching of DMA address and byte counts so that SCRIPTS can be placed in a PROM.
- Separate SCSI and system clocks

Reliability

- 4 K volts ESD protection on SCSI signals
- Typical 350 mV SCSI bus hysteresis
- Protection against bus reflections due to impedance mismatches
- Controlled bus assertion times (reduces RFI, improves reliability, and eases FCC certification)
- Latch-up protection greater than 150 mA
- Voltage feed through protection (minimum leakage current through SCSI pads)
- 20% of pins are power and ground
- Ground isolation of I/O pads and chip logic

Testability

- All SCSI signals accessible through programmed I/O
- SCSI loopback diagnostics
- Self-selection capability
- SCSI bus signal continuity checking
- Supports single step mode operation

Figure 2-1. 53C720 Block Diagram
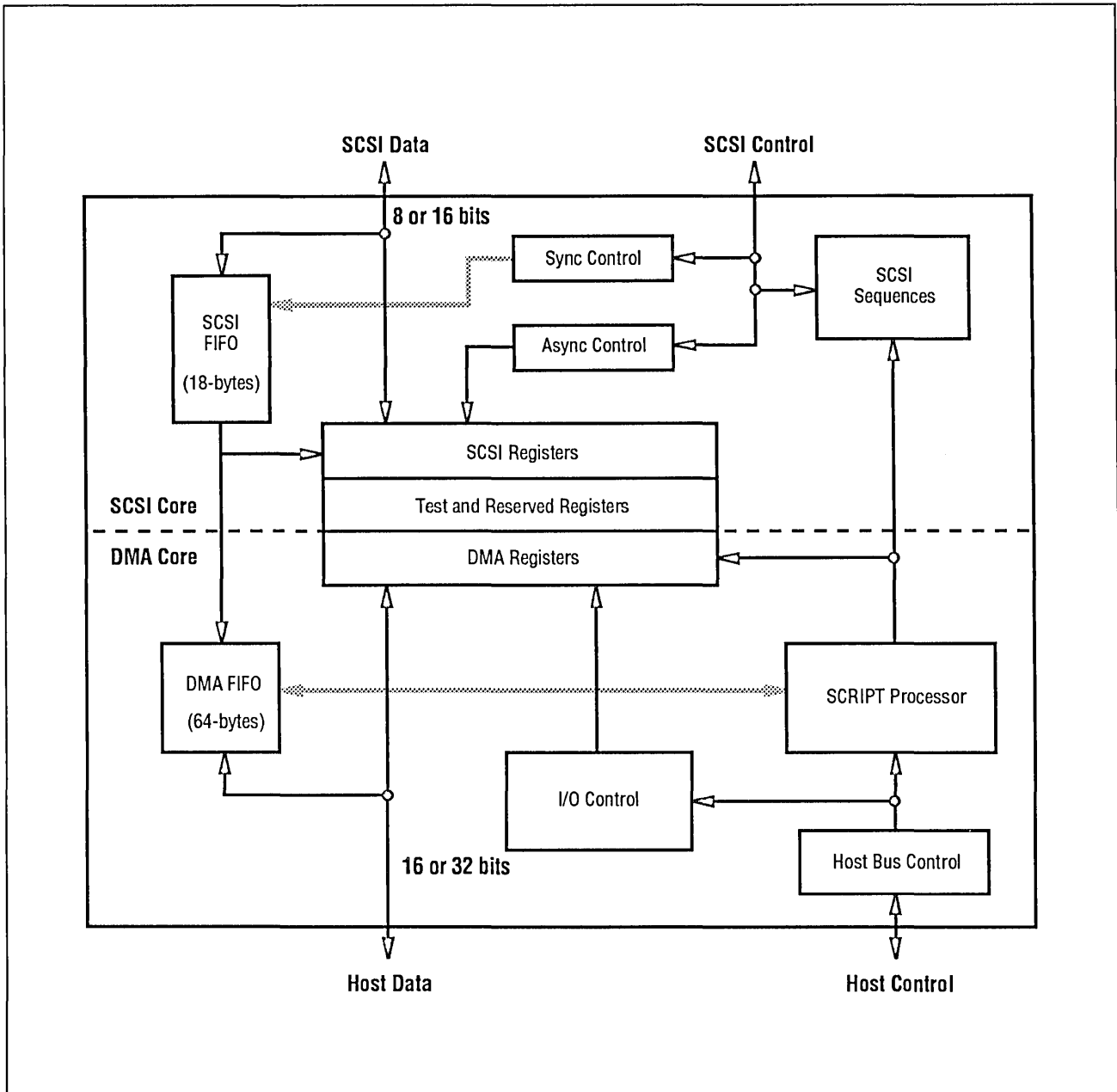
NCR 53C720

Figure 2-2. 53C720 Pin Configuration, Bus Modes 1 and 2
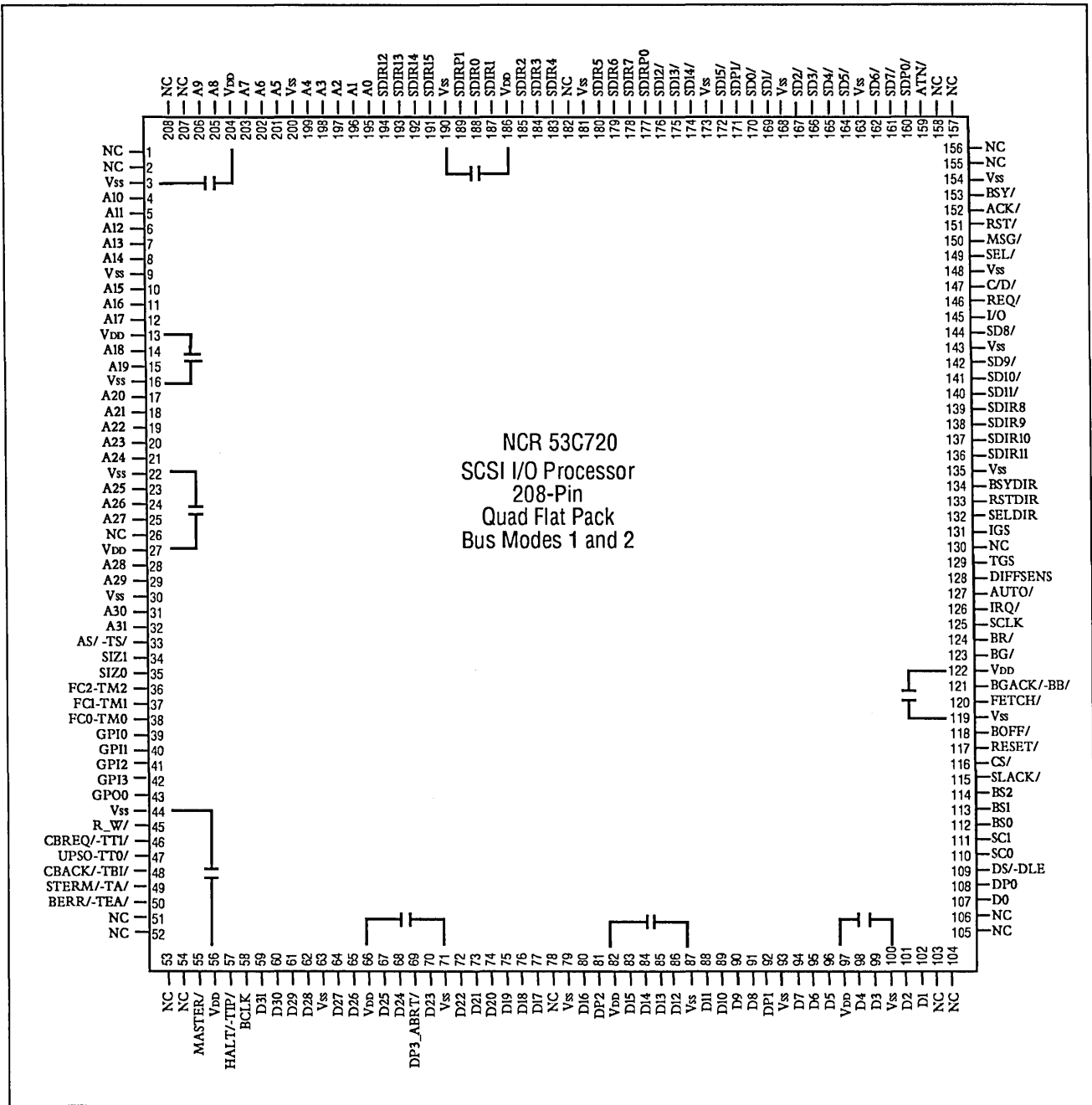
NCR 53C720
SCSI I/O Processor
208-Pin
Quad Flat Pack
Bus Modes 1 and 2

Note: The above decoupling capacitor arrangement shown is recommended to maximize the benefits of the internal split ground system. Capacitor values between 0.01 and 0.1 μF should provide adequate noise isolation. Because of the number of high current drivers on the 53C720, a multilayer PC board with power & ground planes is required.

Figure 2-3. 53C720 Pin Configuration, Bus Modes 3 and 4
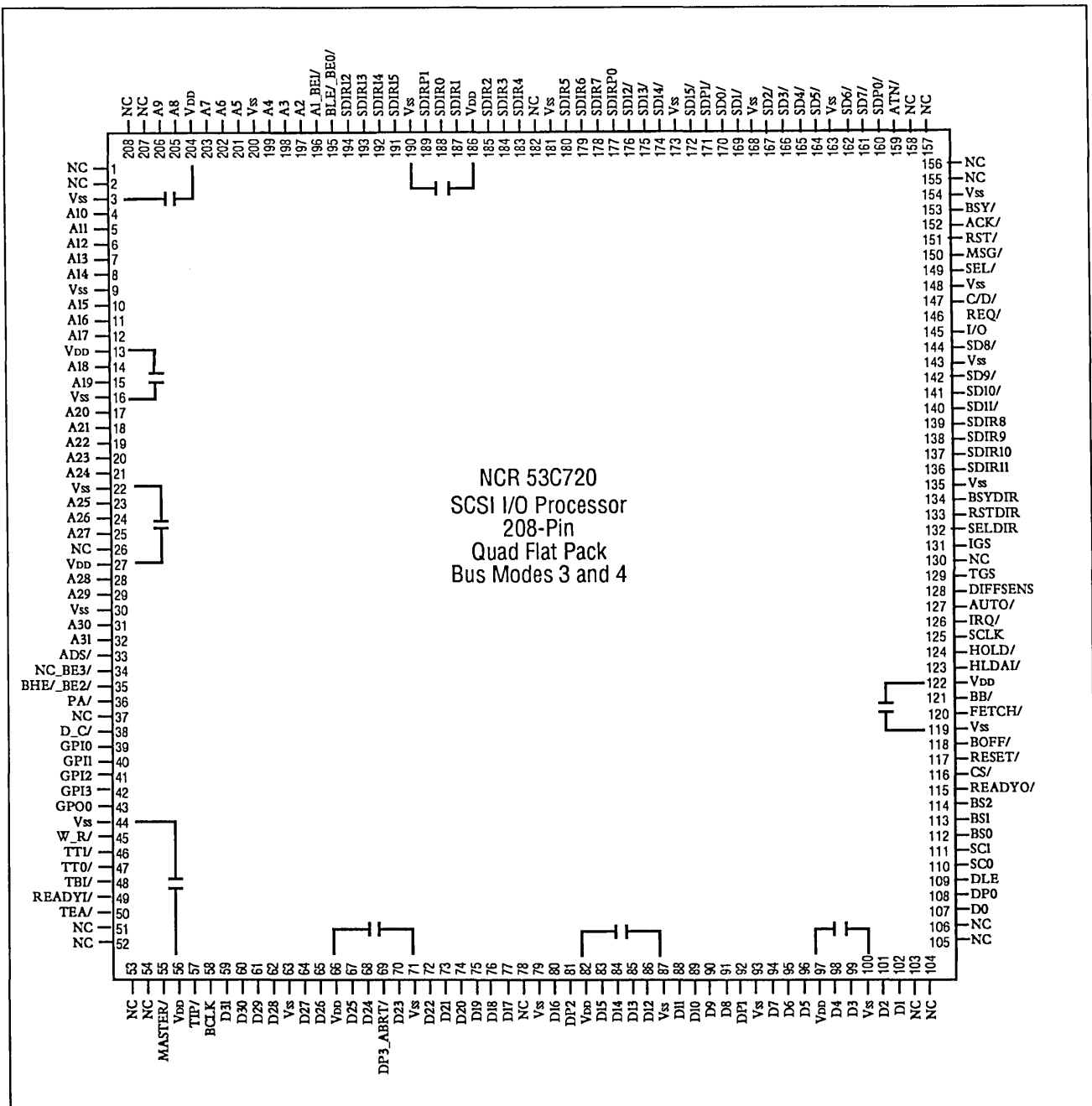
Note: The above decoupling capacitor arrangement shown is recommended to maximize the benefits of the internal split ground system. Capacitor values between 0.01 and 0.1 µF should provide adequate noise isolation. Because of the number of high current drivers on the 53C720, a multilayer PC board with power & ground planes is required. DCNTL bit 6 should be asserted when the 53C720 is initialized so that the PA/ (Preview of address) and D_C/ (Data and Control) are activated.

Transceiver Grounds - V_{SS} (200, 3, 9, 16, 22, 30, 63, 71, 79, 87, 93, 100); Transceiver Power - V_{DD} (204, 13, 27, 66, 82, 97); SCSI Ground - V_{SS} (173, 168, 163, 154, 148, 143); Internal Logic Ground - V_{SS} (44, 119, 135, 181, 190); Internal Logic Power - V_{DD} (56, 122, 186)

Chapter 3

Functional Description

The 53C720 is composed of three tightly coupled functional blocks: the SCSI Core, the DMA Core, and the SCRIPTS Processor.

SCSI Core

The SCSI core supports the SCSI-2 wide bus. It supports synchronous transfer rates of up to 20 MB/S, and asynchronous transfer rates up to 10 MB/S. The programmable SCSI interface makes it easy to "fine tune" the system for specific mass storage devices or SCSI-2 requirements.

The SCSI core offers low level register access or a high-level control interface. Like first generation SCSI devices, the 53C720 SCSI core can be accessed as a register-oriented device. The ability to sample and/or assert any signal on the SCSI bus can be used in error recovery and diagnostic procedures. In support of loopback diagnostics, the SCSI core may perform a self-selection and operate as both an initiator and a target. The 53C720 can test the SCSI pins for physical connection to the board or the SCSI bus.

Unlike previous generation devices, the SCSI core can be controlled by the integrated DMA core through a high-level logical interface. Commands controlling the SCSI core are fetched out of the main host memory. These commands instruct the SCSI core to Select, Reselect, Disconnect, Wait for a Disconnect, Transfer Information, Change Bus Phases and in general, implement all aspects of the SCSI protocol. The SCRIPTS processor is a special high-speed processor optimized for SCSI protocol.

DMA Core

The DMA core is a bus master DMA device that is made to attach to Intel (80386SX and 80386DX), and Motorola (68030 and 68040) processors.

The 53C720 supports 16 or 32-bit memory and automatically supports misaligned DMA transfers. A 64-byte FIFO allows the 53C720 to support two, four, eight, or sixteen longwords to be burst across the memory bus interface . This DMA interface does not support dynamic bus sizing.

The DMA core is tightly coupled to the SCSI core through the SCRIPTS processor which supports uninterrupted scatter/gather memory operations.

SCRIPTS Processor

The SCSI SCRIPTS processor allows both DMA and SCSI instructions to be fetched from host memory. Algorithms written in SCSI SCRIPTS can control the actions of the SCSI and DMA cores and are executed from 16- or 32-bit system memory. Complex SCSI bus sequences are executed independently of the host CPU.

The SCRIPTS processor can begin a SCSI I/O operation in approximately 500 ns. This compares with 2-8 ms required for traditional intelligent host adapters. The SCRIPTS processor offers performance and customized algorithms. Algorithms may be designed to tune SCSI bus performance, to adjust to new bus device types (i.e. scanners, communication gateways, etc.), or to incorporate changes in the SCSI-2/3 logical bus definitions without sacrificing I/O performance.

SCSI SCRIPTS are independent of the CPU and system bus in use. For detailed information on SCSI SCRIPTS, please see the NCR 53C720 *Programmer's Guide.*

Big/Little Endian Support

The Bus Mode select pin gives the 53C720 the flexibility of operating with either Big or Little Endian byte orientation. Internally, in either mode, the byte lanes of the DMA FIFO and registers are not modified. The 53C720 supports byte and longword slave accesses in Big Endian Mode, and byte, word, and longword accesses in Little Endian Mode (Word accesses must be word-aligned).

When a longword is accessed, no repositioning of the individual bytes is necessary, since longwords are addressed by the address of the least significant byte. SCRIPTS always uses longwords in 32-bit systems, so compatibility is maintained between systems using different byte orientations. When a word is accessed, repositioning of individual bytes is necessary. Internally, the 53C720 adjusts the byte control logic of the DMA FIFO and register decodes to enable the appropriate byte lanes. The registers will always appear on the same byte lane, but the address of the register will be repositioned. Words are addressed by the address of the least significant byte. In 16-bit systems words are always used by SCRIPTS, so Big Endian addressing is not supported.

Big/Little Endian mode selection has the most effect on individual byte access. Internally, the 53C720 adjusts the byte control logic of the DMA FIFO and register decodes to enable the appropriate byte lane. The registers will always appear on the same byte lane, but the address of the register will be repositioned.

Data to be transferred between system memory and the SCSI bus always starts at address zero and continues through address 'n' - there is no byte ordering in the chip. The first byte in from the SCSI bus goes to address 0, the second to address 1, etc. Going out onto the SCSI bus, address zero is the first byte out on the SCSI bus, address 1 is the second byte, etc.

Correct SCRIPTS will be generated if the SCRIPTS compiler is run on a system that has the same byte ordering as the target system. Any SCRIPT patching in memory must patch the instruction in the order that the SCRIPTS processor expects it.

Software drivers for the 53C720 should access registers by their logical name (i.e., "SCNTL0) rather than by their address. The logical name should be equated to the register's Big Endian address in Big Endian mode (SCNTL0 = 03h), and its Little Endian address in Little Endian Mode (SCNTL0 = 00h). This way, there is no change to the software when moving from one mode to the other; only the equate statement setting the operating modes needs to be changed.

Addressing of registers from within a SCRIPT is independent of bus mode. Internally, the 53C720 always operates in Little Endian mode.

Big Endian Mode

Big Endian is used primarily in designs based on Motorola processors. The 53C720 treats D(31-24) as the lowest physical memory address. The register map is left-justified (Address 03h = SCNTL0).

Little Endian Mode

Little Endian is used primarily in designs based on Intel processors. This mode treats D(7-0) as the lowest physical memory address. The register map is right-justified (Address 00h = SCNTL0).

System data bus	(31:24)	(23:16)	(15:8)	(7:0)
53C720 pins	(31:24)	(23:16)	(15:8)	(7:0)
Register	SCNTL3	SCNTL2	SCNTL1	SCNTL0
Little Endian addr	03h	02h	01h	00h
Big Endian addr	00h	01h	02h	03h

Loopback Mode

The 53C720 loopback mode allows testing of both initiator and target functions and, in effect, lets the chip talk to itself. When the Loopback Enable bit is set in the STEST1 register, the 53C720 allows control of all SCSI signals, whether the 53C720 is operating in initiator or target mode. For additional instructions on using loopback mode, refer to the 53C720 *Programmer's Guide*.

Parity Options

The 53C720 implements a flexible parity scheme that allows control of the parity sense, allows parity checking to be turned on or off, and has the ability to deliberately send a byte with bad parity over the SCSI bus to test parity error recovery procedures. The following bits are involved in parity control and observation:

1) Assert ATN/ on Parity Errors – Bit 1 in the SCNTL0 register.

   This bit causes the 53C720 to automatically assert SCSI ATN/ when it detects a parity error while operating as an initiator.

2) Enable Parity Generation – Bit 2 in the SCNTL0 register.

   This bit determines whether the 53C720 generates parity sent to the SCSI bus or allows parity to "flow through" the chip to/from the SCSI bus and system bus.

3) Enable Parity Checking – Bit 3 in the SCNTL0 register.

   This bit enables the 53C720 to check for parity errors. The 53C720 checks for odd parity.

4) Assert Even SCSI Parity – Bit 2 in the SCNTL1 register.

   This bit determines the SCSI parity sense checked & generated by the 53C720.

5) Disable Halt on ATN/ or a Parity Error)Target Mode Only) – Bit 5 in the SCNTL1 register.

   This bit causes the 53C720 to halt operations when a parity error is detected in target mode.

6) Enable Parity Error Interrupt – Bit 0 in the SIEN0 register.

   This bit determines whether the 53C720 will generate an interrupt when it detects a parity error.

7) Parity Error – Bit 0 in the SIST0 register.

   This status bit is set whenever the 53C720 has detected a parity error on either the SCSI bus or the system bus.

8) Status of SCSI Parity Signal – Bit 0 in the SSTAT0 register and bit 0 in SSTAT2.

   These status bits represent the live SCSI Parity Signal (SDP0 and SDP1.

9) Latched SCSI Parity Signal – Bit 3 in the SSTAT1 register and bit 3 in SSTAT2.

   These status bits contain the SCSI parity of the bytes latched in the SIDL.

10) DMA FIFO Parity – Bit 3 in the CTEST2 register.

   This status bit represents the parity bit in the DMA FIFO after data is read from the FIFO by reading the CTEST6 register.

11) DMA FIFO Parity – Bit 3 in the CTEST0 register.
    This write-only bit is written to the DMA FIFO after writing data to the DMA FIFO by writing the CTEST6 register.

12) SCSI FIFO Parity – Bit 0 in the STEST1 register.

   This status bit represents the parity bit in the SCSI FIFO after data is read from the FIFO by reading the SODL register, once bit 0 in STEST3 is asserted.

NCR 53C720

Table 3-1. SCSI Parity Control

EPG	EPC	ASEP	Description
0	0	0	Will not check for parity errors. Parity flows from DP(3-0) through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP(3-0) when receiving SCSI data. Asserts odd parity when sending SCSI data.
0	0	1	Will not check for parity errors. Parity flows from DP(3-0) through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP(3-0) when receiving SCSI data. Asserts even parity when sending SCSI data.
0	1	0	Checks for odd parity on both SCSI data received and system data when sending. Parity flows from DP(3-0) through the chip to the SCSI bus when sending SCSI data, Parity flows from SCSI bus to DP(3-0) when receiving SCSI data. Asserts odd parity when sending SCSI data.
0	1	1	Checks for odd parity on both SCSI data received and system data when sending. Parity flows from DP(3-0) through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP(3-0) when receiving SCSI data. Asserts even parity when sending SCSI data.
1	0	0	Will not check for parity errors. Parity on DP(3-0) is ignored. Parity is generated when sending SCSI data. Parity flows from SCSI bus to the chip but is not asserted on DP(3-0) when receiving SCSI data. Asserts odd parity when sending SCSI data.
1	0	1	Will not check for parity errors. Parity on DP(3-0) is ignored. Parity is generated when sending SCSI data. Parity flows from SCSI bus to chip, but is not asserted on DP(3-0) when receiving SCSI data. Asserts even parity when sending SCSI data.
1	1	0	Checks for odd parity on SCSI data received. Parity on DP(3-0) is ignored. Parity is generated when sending SCSI data. Parity flows from SCSI bus to the chip, but is not asserted on DP(3-0) when receiving SCSI data. Asserts odd parity when sending SCSI data.
1	1	1	Checks for odd parity on SCSI data received. Parity on DP(3-0) is ignored. Parity is generated when sending SCSI data. Parity flows from SCSI bus to the chip, but is not asserted on DP(3-0) when receiving SCSI data. Asserts even parity when sending SCSI data.

Key: EPG = Enable Parity Generation (bit 2 SCNTL0)
EPC = Enable Parity Checking (bit 3 SCNTL0)
ASEP = Assert SCSI Even Parity (bit 2 SCNTL1)

Table 3-2. SCSI Parity Errors and Interrupts

This table describes the options available when a parity
error occurs. This table only applies when the Enable
Parity Checking bit is set.

DHP	PAR	Description
0	0	Will NOT halt when a parity error occurs in target or initiator mode.
0	1	Will interrupt when a parity error occurs in target or initiator mode.*
1	0	Will halt when a parity error occurs in target mode and will NOT generate an interrupt.
1	1	Will halt when a parity error occurs in target mode and will generate an interrupt in target or initiator mode.*

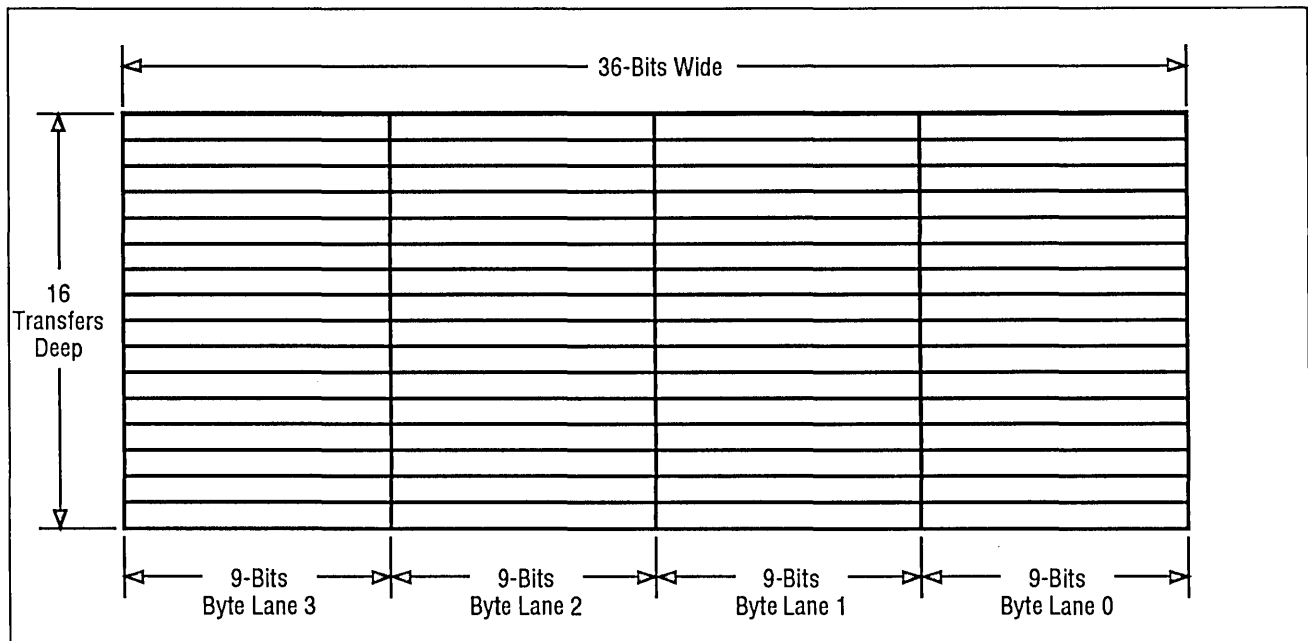*Key:*   *DHP = Disable Halt on ATN/ or Parity Error (bit 5 SCNTL1)*

          PAR= Parity Error (bit 0 SIEN0)

*Initiator mode parity error interrupts are generated at
the end of a block move.

DMA FIFO

The DMA FIFO is more complex than the SCSI FIFO.
The DMA FIFO is a 36 x 16 bit FIFO. It is divided into 4
sections, each 9 bits wide and 16 transfers deep.

Figure 3-1. DMA FIFO Sections

Data Paths

The data path through the 53C720 is dependent on whether data is being moved into or out of the chip, and whether SCSI data is being transferred asynchronously or synchronously.

Figure 3-2 shows how data is moved to/from the SCSI bus in each of the different modes.

The following steps will determine if any bytes remain in the data path when the chip halts an operation:

Asynchronous SCSI Send:

1) Subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register. AND the result with 7Fh for a byte count between zero and 64.

2) Read bit 5 in the SSTAT0 and SSTAT2 registers to determine if any bytes are left in the SODL register. If bit 5 is set in the SSTAT0 and SSTAT2, then the least significant byte and the most significant byte in the SODL register is full, respectively.

Synchronous SCSI Send:

1) Subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register. AND the result with 7Fh for a byte count between zero and 64.

2) Read bit 5 in the SSTAT0 and SSTAT2 registers to determine if any bytes are left in the SODL register. If bit 5 is set in the SSTAT0 and SSTAT2, then the least significant byte and the most significant bytes in the SODL register is full, respectively.

3) Read bit 6 in the SSTAT0 and SSTAT2 registers to determine if any bytes are left in the SODR register. If bit 6 is set in the SSTAT0 and SSTAT2, then the least significant byte and the most significant byte in the SODR register is full, respectively.

Asynchronous SCSI Receive:

1) Subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register. AND the result with 7Fh for a byte count between 0 and 64.

2) Read bit 7 in the SSTAT0 and SSTAT2 register to determine if any bytes are left in the SIDL register. If bit 7 is set in the SSTAT0 and SSTAT2, then the least significant byte and the most significant byte is full, respectively.

Synchronous SCSI Receive:

1) Subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register. AND the result with 7Fh for a byte count between 0 and 64.

2) Read the SSTAT1 register and examine bits 7-4, the binary representation of the number of valid bytes in the SCSI FIFO, to determine if any bytes are left in the SCSI FIFO.

Figure 3-2. 53C720 Data Paths

μP Interface	μP Interface	μP Interface	μP Interface
DMA FIFO (36-bits x 16)	DMA FIFO (36-bits x 16)	DMA FIFO (36-bits x 16)	DMA FIFO (36-bits x 16)
SODL Register	SIDL Register	SODL Register	SCSI FIFO (18-bits x 9)
SCSI Interface	SCSI Interface	SODR Register	SCSI Interface
		SCSI Interface	
Asynchronous SCSI Send	Asynchronous SCSI Receive	Synchronous SCSI Send	Synchronous SCSI Receive

Host Interface

Misaligned Transfers

The 53C720 accommodates block data transfers beginning or ending on odd byte or odd word addresses in system memory. Such addresses are termed "misaligned." An odd byte is defined as one in which the address contains A0 = 1; an odd word is defined as one in which the address contains A1 = 1. Misaligned transfers differ depending on the type of transfer (cache line or programmable bursting) and whether they occur at the start or end of the transfer. The 53C720 does not perform 24-bit transfers.

Cache line Bursting

Start of Transfer

At the start of the transfer, if the address starts at an odd byte boundary (bit A0 = 1), the 53C720 will line up to a word boundary by performing a single-byte (8-bit) transfer in a single bus ownership. Then, if the address is at an odd word boundary (bit A1 = 1), the 53C720 will line up to a longword boundary by performing a single-word (2-byte) transfer in a single bus ownership. At this point, longword (4-byte) transfers will be performed, one per bus ownership, until the address bits line up to a cache line boundary (A(3-0) = 0). Once aligned, multiple cache line bursts of four longwords per bus ownership will be

performed until the byte count decreases to 31 or less. The worst-case example of five bus ownerships before cache line bursting can begin is depicted in Big Endian mode in Figure 3-3.

End of Transfer

When the byte count decreases to 31 or fewer bytes, the 53C720 transfers the remaining longwords, words, and/or bytes in the same bus ownership until the transfer is complete. The 53C720 transfers longwords until the byte count decreases to 3 or less. If the byte count is 3 or 2, one word is transferred. If the byte count is 1, one byte is transferred. An example depicting the remaining transfers when the byte count is 31 is shown in Figure 3-4.

Figure 3-3. Cache Line Bursting, Start of Transfer (Big Endian Mode)

Address Bits A4-A2	Address Bits A1-A0				Notes:
	00	01	10	11	
000		1	2		a) At the start of this diagram, 47 bytes remain to be transferred
001		3			
010		4			b) The programmable burst length is 8
011		5			
100					c) Only two longwords, one word, and one byte are transferred in the last bus ownership.
101		6			
110					
111					

Programmable Bursting

When not in cache line burst mode, the 53C720 is able to do 2, 4, 8 or 16 transfers per bus ownership. The transfers can be either byte, word, or longword transfers.

Start of Transfer

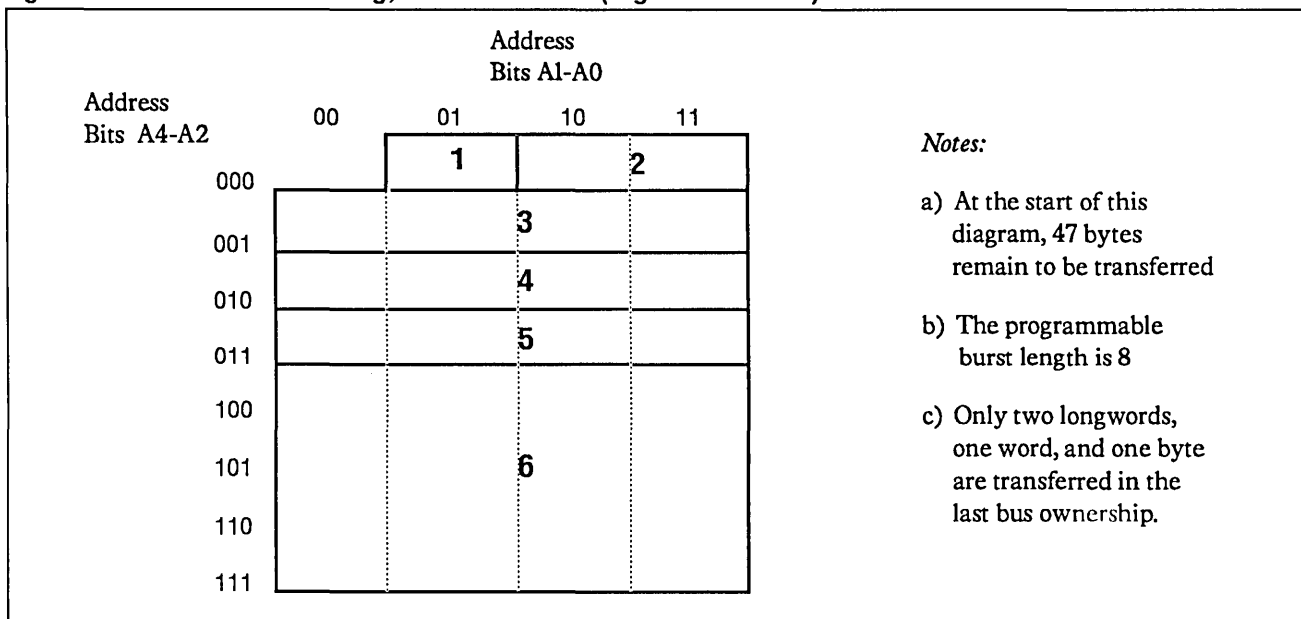The 53C720 transfers the programmable burst length number of transfers during each bus ownership. If the address starts at an odd byte boundary (bit A0 = 1), the 53C720 will line up to a word boundary by performing a single-byte transfer. Then, if the address is at an odd word boundary (bit A1 = 1), the 53C720 will line up to a longword boundary by performing a single-word (2-byte) transfer in a single bus ownership. At this point, the 53C720 will transfer longwords until the byte count decreases to 3 or less. The chip will transfer the programmable-burst-length number of transfers per bus ownership regardless of the width (byte, word or longword). An example of a transfer in which the programmable burst length is 8 is depicted in Figure 3-5.

End of Transfer

The 53C720 transfers longwords until the byte count decreases to 3 or less. If the byte count is 3 or 2, one word is transferred. If the byte count is 1, one byte is transferred. The 53C720 will transfer up to the programmable-burst-length number of transfers per bus ownership. At the end of a block transfer, if the byte count is less than the programmable-burst-length, the remaining bytes will be transferred during the bus ownership. It is possible to transfer less but not more than the programmable-burst-length number of transfers per bus ownership. An example of a transfer in which the programmable burst length is 8 is depicted in Figure 3-6. *Note:* Each bus ownership requires the 53C720 to arbitrate for the host bus. There is a fairness delay of 5-8 clocks between each bus ownership.

Figure 3-4. Cache Line Bursting, End of Transfer (Big Endian Mode)
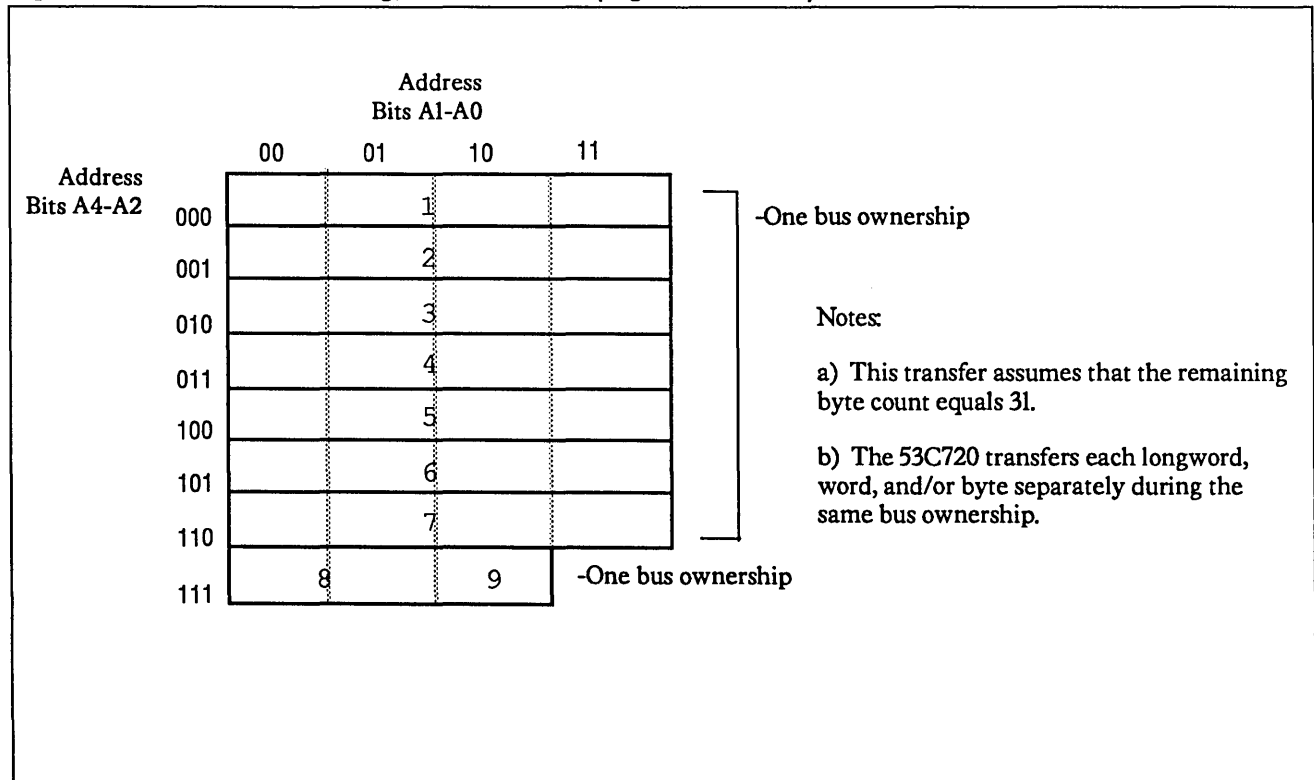
Figure 3-5. Programmable Bursting, Start of Transfer (Big Endian Mode)

Notes:

a) This transfer begins at Address 000001

b) The programmable burst length is 8

c) The 53C720 transfers each byte, word and longword separately during the same bus ownership.
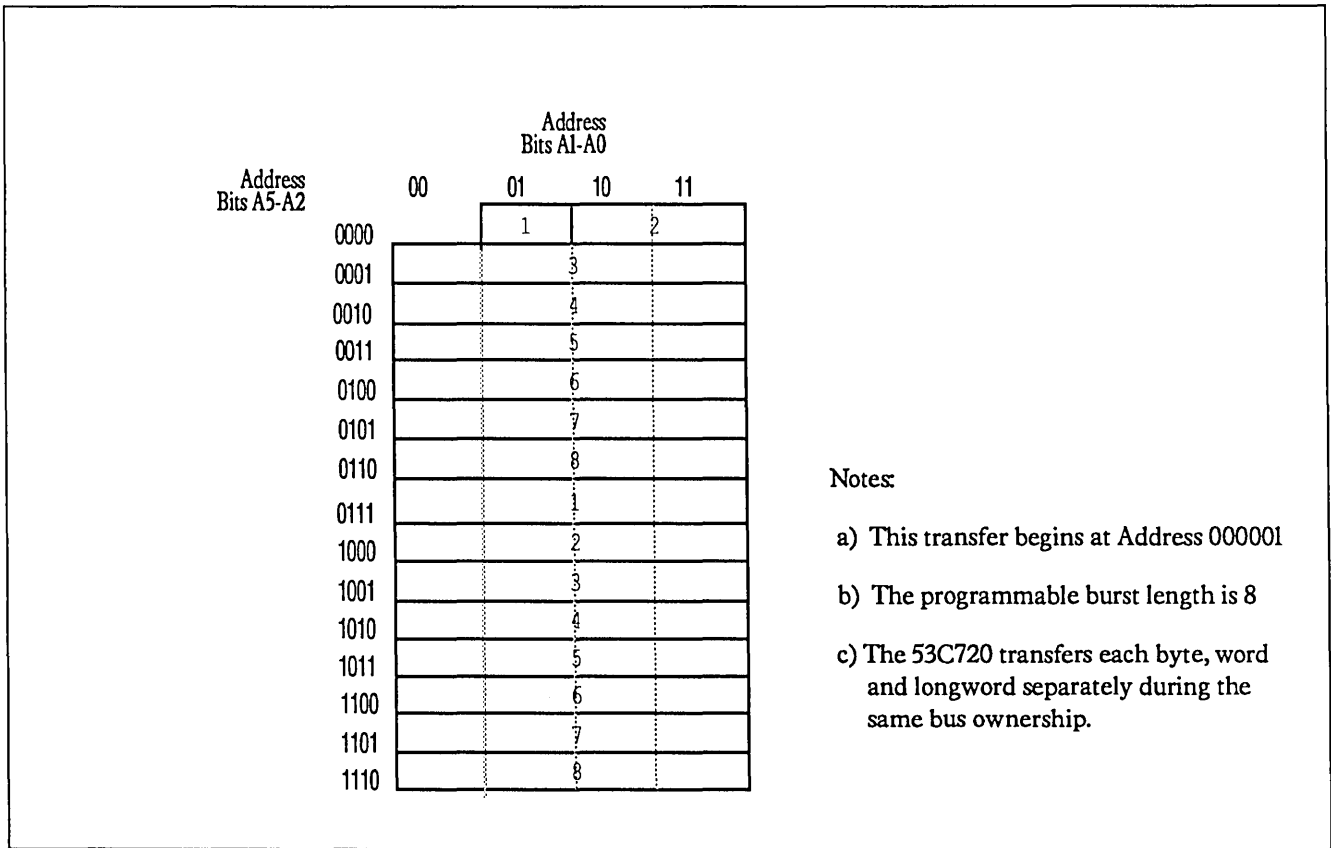
Figure 3-6. Programmable Bursting, End of Transfer (Big Endian Mode)

Notes:

a) At the start of this diagram, 47 bytes remain to be transferred

b) The programmable burst length is 8

c) Only three longwords, one word, and one byte are transferred in the last bus ownership.
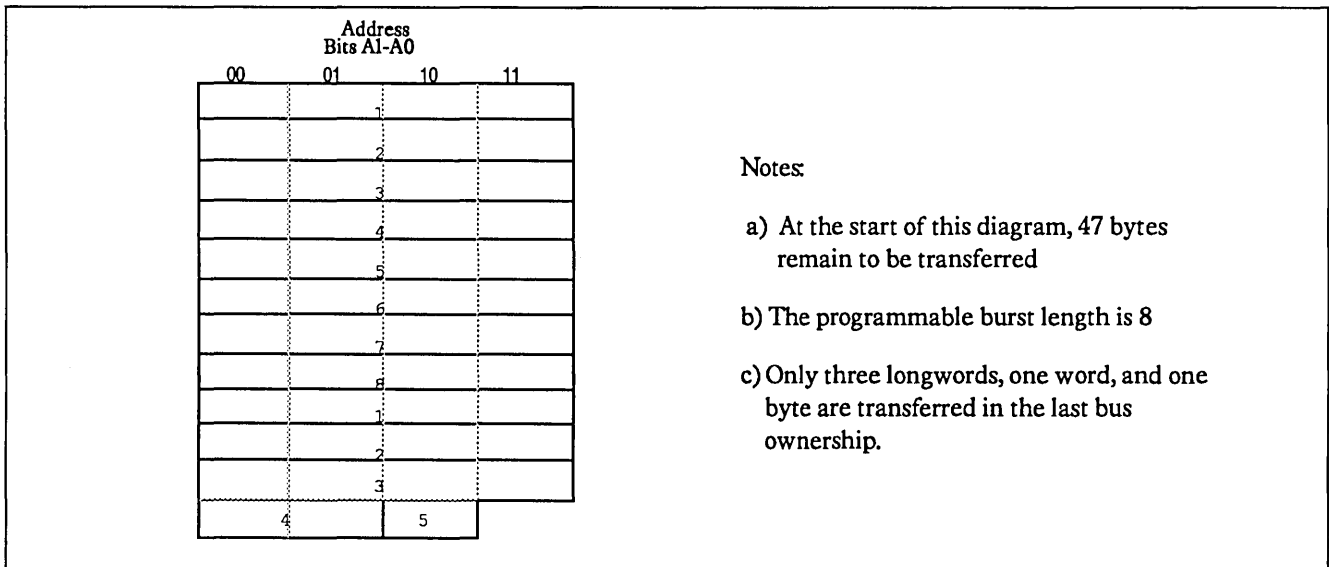
Bus Retry

Bus Retry allows the 53C720 to retry the previous cycle using the same address, size, etc. The bus retry signals are asserted by an external device using the HALT/ (Halt) and BERR/ (Bus error) signals in Bus Mode 1 and the TA/ (Transfer Acknowledge) and TEA/ (Transfer Error Acknowledge) in Bus Mode 2. During a non-cache line burst, a bus retry can be executed in any cycle. During a cache line burst, however, the bus retry should be executed during the first cycle. In Bus Mode 1, the 53C720 will retry the bus cycle and assert the CBREQ/ (Cache Burst Request) again. If a bus retry is attempted during one of the subsequent cycles, the 53C720 will halt the transfer until the halt signal is deasserted. If the bus error signal is still asserted at this time, the 53C720 will abort the transfer. In Bus Mode 2, if a bus retry is attempted during one of the subsequent cycles the 53C720 will abort the transfer. A bus retry cannot be attempted during a Preview of Address (PA/). For more information on the PA/ signal, refer to Chapter 4.

Bidirectional STERM/-TA/--ReadyIn

The STERM/TA/ReadyIn (Referred to as STERM/) signal terminates a read or write cycle. In a typical system, STERM/ is a wire-OR signal driven by slave devices and monitored by bus masters. When the system CPU is faster than the slave device being accessed, a cycle may be terminated as soon as the slave is ready. Slave devices which are faster than the CPU present a special problem in that they are required to insert wait states to allow the CPU to catch up. The 53C720 is able to accommodate both situations.

During slave accesses, the SLACK/-ReadyO/ (Referred to as SLACK/) output provides an indication that the 53C720 is ready to terminate a read or write cycle. After asserting SLACK/, the 53C720 will sample STERM/ on every subsequent rising BCLK edge until it is sampled active, at which time the read/write cycle will be terminated. Any time between SLACK/ and STERM/ is treated as a wait state; a read/write cycle may be stretched indefinitely. However on a write cycle, data is taken into the 53C720 before the SLACK/ signal is asserted. Wait states may not be added to allow for late write data.

Typically, SLACK/ is tied back to STERM/ as in Figure 3-7. If the system CPU is not capable of completing a slave cycle in the minimum time required by the 53C720, SLACK/ must be delayed before asserting STERM/. If the system CPU is capable of running slave/write cycles with zero additional wait states, no delay is necessary.

In systems where the CPU is faster than the 53C720, SLACK/ may be connected to STERM/ with external logic, but the best solution is to set the Enable Acknowledge (EA) bit in the DCNTL register to internally connect SLACK/ to STERM/. When the EA bit is set, the STERM/ pin changes from being an input in both master and slave modes, and becomes bidirectional: input in master mode, and output in slave mode. This way, no external logic is required and proper timing for zero wait state operation is guaranteed. Setting the EA bit must be the first slave I/O access to the 53C720.

Figure 3-7. Bidirectional STERM/-TA/-ReadyIn/
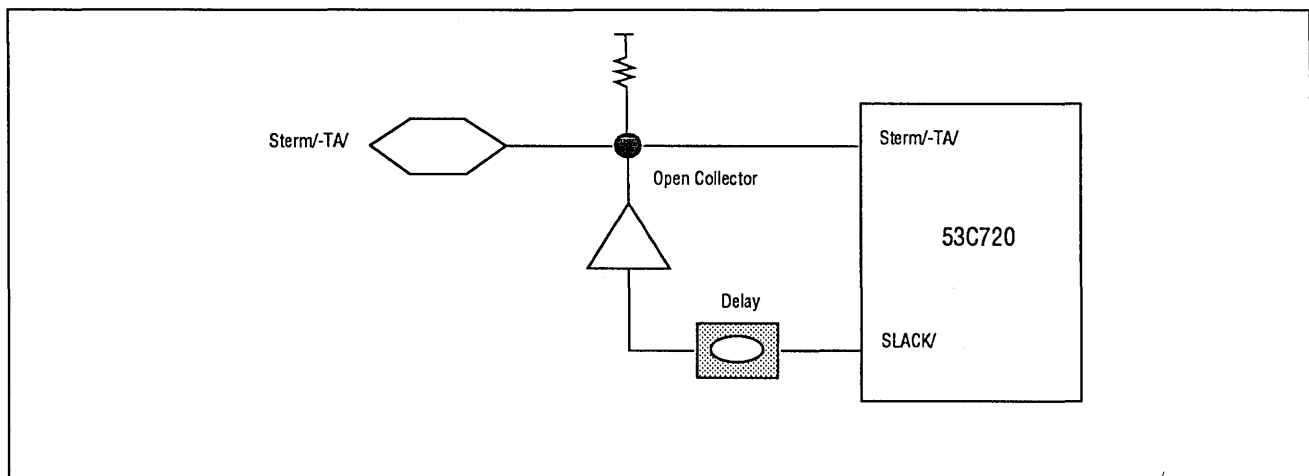
SCSI Bus Interface

The 53C720 can be used in both single-ended and differential applications.

In single-ended mode, all SCSI signals are active low. The 53C720 contains the open-drain output drivers and can be connected directly to the SCSI bus. Each output is isolated from the power supply to ensure that a powered-down 53C720 has no effect on an active SCSI bus (CMOS "voltage feed-through" phenomenon). Additionally, signal filtering is present at the inputs of REQ/ and ACK/ to increase immunity to signal reflections.

In differential Mode, the SDIR (15-0), SDIRP (1-0), IGS, TGS, RSTDIR, BSYDIR, and SELDIR signals control the direction of external differential-pair transceivers. See Figure 3-8 for the suggested differential wiring diagram. The wiring diagram shows eight 75ALS170 3-channel transceivers and one 75ALS171 3-channel transceiver, though other single and multi-channel devices may be used (DS36954 4-channel transceiver, for instance). The suggested value for the 15 pull-up resistors in the diagram is 680 Ω. The pull-up value should be no lower than the transceiver IOL can tolerate, but not so high as to cause RC timing problems.

Terminator Networks

The terminator networks provide the biasing needed to pull inactive signals to an inactive voltage level, and are required for both single-ended and differential applications. Terminators must be installed at the extreme ends of the SCSI cable, and only at the ends; no system should ever have more or less than 2 sets of terminators installed and active. SCSI host adapters should provide a means of accommodating terminators. The terminators should be socketed, so that if not needed they may be removed.

Single-ended cables are terminated differently from differential cables. Single-ended cables use a 220 ohm pull-up to the termination power supply (Term-Power) line and a 330 ohm pull-down to Ground. Differential cables use a 330 ohm pull-up from "– SIG" to Term-Power, a 330 ohm pull-down from "+ SIG" to Ground, and a 150 ohm resistor from "– SIG" to "+ SIG".

Because of the high performance nature of the 53C720, Alternative Two termination (Defined in the ANSI standard) is recommended. This method employs a 2.85 Volt regulator and 110 Ohm pull-up resistors (no pull-down). Figure 3-9 shows the schematics for Alternative Two termination. For additional information, refer to the SCSI-2 specifica tion.

(Re)Select During (Re)Selection

In multi-threaded SCSI I/O environments, it is not uncommon to be selected or reselected while trying to perform selection/reselection. This situation may occur when a SCSI controller (operating in initiator mode) tries to select one target and gets reselected by another. The analogous situation for target devices is being selected while trying to perform a reselection.

Once a change in operating mode occurs, the initiator SCRIPT should start with a Set Initiator instruction or the target SCRIPT should start with a SET Target instruction. It should be noted that the selection and reselection enable bits (SCID bits 5 and 6, respectively) should both be asserted so that the 53C720 may respond as an initiator or as a target.

The selection or reselection enable bits allow the 53C720 to respond as either a target or an initiator. For example, if only selection is enabled, the 53C720 cannot be reselected as an initiator. There are also status and interrupt bits in the SIST0 and SIEN0 registers respectively, indicating if the 53C720 has been selected (bit 5) and reselected (bit 4).

Synchronous Operation

The 53C720 can transfer synchronous SCSI data in both initiator and target modes. The SXFER register controls both the synchronous offset and the transfer period, and may be loaded by the CPU before SCRIPT execution begins or from within a SCRIPT via a table indirect I/O instruction.

The 53C720 can always receive data from the SCSI bus at a synchronous transfer period as short as 80 ns for SCSI-1 or 160 ns for SCSI-2, regardless of the transfer period used to send data. Therefore, when negotiating for synchronous data transfers, the suggested transfer period is 80 or 160 ns. Depending on the SCLK frequency and the synchronous clock divider , the 53C720 can send synchronous data at intervals as short as 100 or 200 ns.

NCR 53C720

Figure 3-8. Differential Wiring Diagram
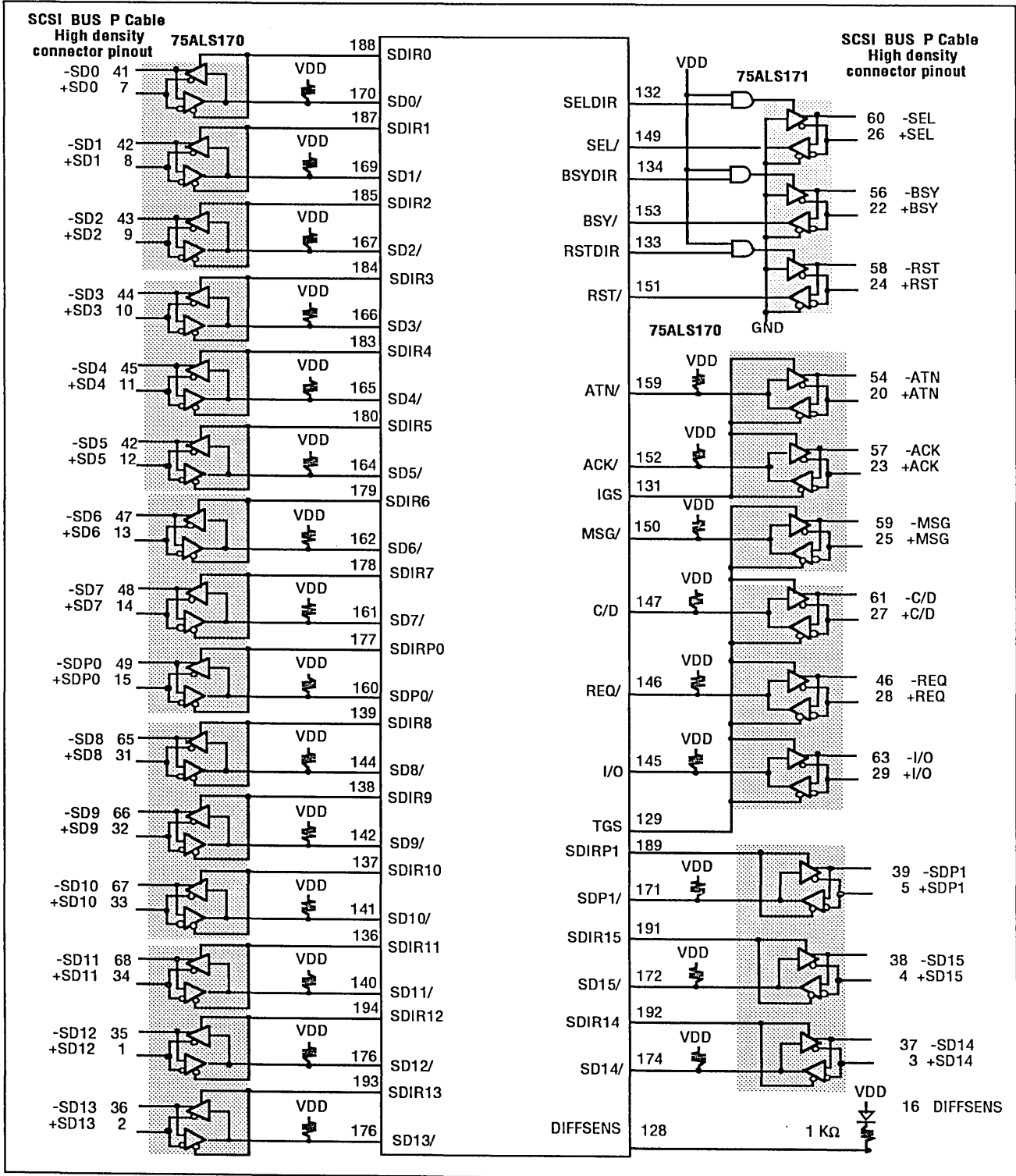
Figure 3-9. 53C720 Alternative Two Termination

Key:
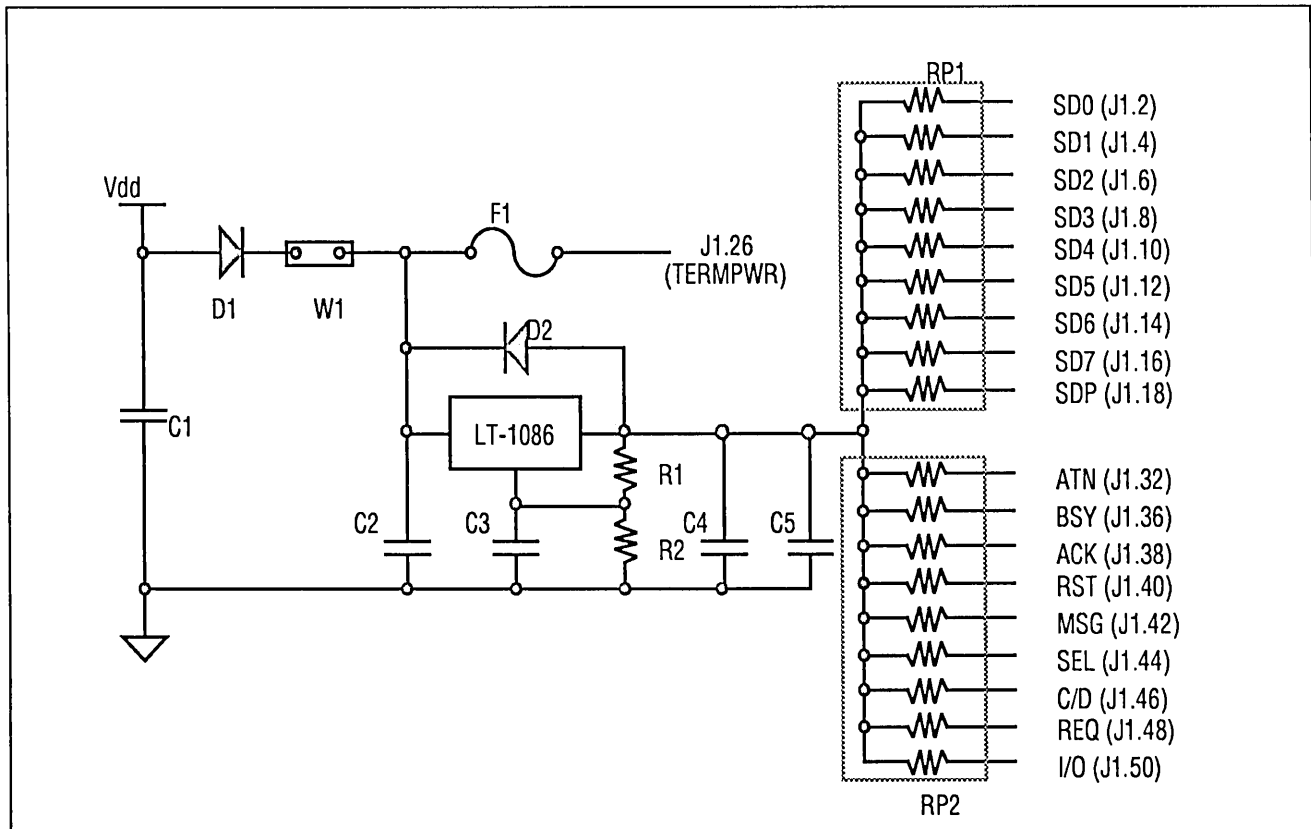
C1	*4.7 μF tantalum, SMT*
C2, C3	*1.0 μF tantalum, SMT*
C4	*22 μF tantalum, SMT*
C5	*0.1 μF ceramic, SMT*
D1-D2	*Schottkey diode*
F1	*1.5 Amp fuse, socketed, 2AG*
J1	*50-pin dual row header, male*
RP1-RP2	*110 x 9 (1%) pull-ups, SIP-10*
U4	*Voltage Regulator, TO-39*
W1	*2-position header*

Chapter 4

Signal Descriptions

The 53C720 host bus can operate in one of four modes: Bus Mode 1 (68030-like), Bus Mode 2 (68040-like), Bus Mode 3 (80386SX-like), and Bus Mode 4 (80386DX-like). Both Big and Little Endian byte orientations are supported in Bus Modes 1, 2, and 4. The bus mode is selected by using the BS (2:0) pins. A function is listed on the table as NC (not connected) if it is not active for a given bus mode. A slash ("/") indicates an active-low signal. Refer to Chapter 7, *Electrical Specifications*, for specific pin type (tristate, open drain, etc.) and current drive capabilities.

Table 1. Interface Signals

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Description (Slave Type, Master Type)
D(31:0)	D(31:0)	D(31:0)	D(31:0)	*Host Data Bus* (I/O, I/O) - Main data path into host memory for all Bus Modes. *Note*: In order to interface to a 16-bit bus, Bit 3 in the DCNTL register should be asserted and data lines 31 through 16 should be tied to data lines 15 through 0, respectively.
DP(2:0)	DP(2:0)	DP(1:0)	DP(2:0)	*Host Bus Data Parity* (I/O, I/O) In all Bus Modes: DP0 provides parity for D(7:0) DP1 provides parity for D(15:8) DP2 provides parity for D(23:16) *Note*: In order to interface to a 16-bit bus and to support parity, DP3 and DP2 should be tied to DP1 and DP0, respectively.
DP3_Abort/	DP3_Abort/	Abort/	DP3_Abort/	*Host Bus Data Parity* (I/O, I/O) - In all bus modes, DP3 provides parity for D(31:24). Parity is valid on all byte lanes, including unused lanes. In order to disable parity through mode,, assert Bit 2 in the SCNTL0 register. DP3 becomes a hardware abort input (ABRT/).

NCR 53C720

Table 1. Interface Signals (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Description (Slave Type, Master Type)
DS/	DLE	DLE	DLE	DS/ - *Data Strobe* (Z, I/O) - In Bus Mode 1, this signal indicates that valid data has been or should be placed on the data lines.
				DLE - *Data Latch Enable* (I, I) - In Bus Modes 2, 3 and 4, this signal transparently latches read data into the 53C720 prior to an acknowledge.
A(31:2)	A(31:2)	A(31:2)	A(31:2)	*Address Bus* (I, O) - In all bus modes, this signal provides an address bus to the host memory.
AS/	TS/	ADS/	ADS/	AS/ - *Address Strobe* (I, O) - In Bus Mode 1, this signal indicates that a valid address is on A(31:0).
				TS/ - *Transfer Start* (I, O) - In Bus Mode 2, Transfer start indicates that a bus cycle is starting and all of the status and address lines are valid.
				ADS/ - *Address Status* (I, O) - In Bus Modes 3 and 4, this signal indicates that a valid bus cycle definition and address are being driven.
R_W/	R_W/	W_R/	W_R/	*Read/Write* (I, O) - Indicates the direction of the data transfer relative to the current master.
				R_W/ - Signal for Bus Modes 1 and 2.
				W_R/ - Signal for Bus Modes 3 and 4.
BR/	BR/	HOLD/	HOLD/	BR/ - *Bus Request* (O, O) - In Bus Modes 1 and 2, this signal indicates that there is a request to use the host bus.
				HOLD/ - *Hold* (O, O) - In Bus Modes 3 and 4, this signal indicates there is a request to use the host bus.

Table 1. Interface Signals (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Description (Slave Type, Master Type)
BG/	BG/	HLDAI/	HLDAI/	BG/ - *Bus Grant* (I, I) - In Bus Modes 1 and 2, this signal indicates that the host bus has been granted to the 53C720. HLDAI/ - *Hold Acknowledge* (I, I) - In Bus Modes 3 and 4, this signal indicates that the previous bus master has given up the use of the host bus.
BGACK/	BB/	BB/	BB/	BGACK/ - *Bus Grant Acknowledge* (Z, I/O) - In Bus Mode 1, this signal indicates that the 53C720 or another device has taken control of the host signals. BB/ - *Bus Busy (wire-OR'd)* (Z, I/O) - In Bus Modes 2, 3 and 4, this signal indicates that the 53C720 or another device has taken control of the host bus signals.
BOFF/	BOFF/	BOFF/	BOFF/	BOFF/- *Back Off* (I, I) - In all Bus Modes, this forces the 53C720 to relinquish bus mastership at the end of the current cycle, if the proper setup timing requirements are met. When BOFF/ is deasserted, a new arbitration will take place and the cycles will resume. BOFF/ is sampled at every start cycle. During worst case operation, if timing is not met it will take the 53C720 two clocks to get off the SCSI bus. The start cycle will become a release cycle. If BOFF/ is asserted during arbitration, the 53C720 will com plete arbitration and get off the bus at the first start cycle.
BCLK	BCLK	BCLK	BCLK	*Bus Clock* (I, I) - This clock controls all host related activity in all bus modes.
RESET/	RESET/	RESET/	RESET/	*Chip Reset* (I, I) - Forces a full chip reset in all bus modes.

NCR 53C720

Table 1. Interface Signals (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Description (Slave Type, Master Type)
CS/	CS/	CS/	CS/	*Chip Select* (I, I) – Selects the 53C720 as a slave I/O device in all bus modes. When CS/ is detected: Bus Mode 1: CBACK/ is deasserted. Bus Modes 2, 3 and 4: TBI/ is asserted.
IRQ/	IRQ/	IRQ/	IRQ/	*Interrupt* (O, O) - In all bus modes, this signal indicates that service is required from the host CPU.
UPSO	TT0/	TT0/	TT0/	UPSO - *User Programmable Status* (Z,O) - General purpose line in Bus Modes 1, 3, and 4. The value in a register bit is asserted while the chip is a bus master. TT0/ - *Transfer Type Zero* (Z,O) - In Bus Mode 2, this signal indicates the current bus transfer type. This bit can be programmed from a register bit (default = 0). It is asserted only when the 53C720 is bus master.
SIZ0	SIZ0	BHE/	BE2/	SIZ0 - *Transfer Size Zero* (I, O) - In Bus Modes 1 and 2, SIZ0 indicates the current transfer size in combination with SIZ1 (see table below). BHE/ - *Byte High Enable* (I, O) - In Bus Mode 3, this signal enables data transfer on the high order byte lane D(15-8). BE2/ - *Byte Enable Two* (I, O) - In Bus Mode 4, this signal enables data transfer on byte lane D(23:16).
SIZ1	SIZ1	NC	BE3/	SIZ1 - *Transfer Size One* (I,O) - In Bus Modes 1 and 2, SIZ1 indicates the current transfer size in combination with SIZ0, as shown in the table below. **SIZ1, SIZ0** 00 Long word (4-bytes) 01 Byte (1 byte) 10 Word (2-byte slave cycles are allowed , if word-aligned, in Little Endian mode) 11 Bus Mode 1, Illegal; Bus Mode 2, Cache line burst BE3/- *Byte Enable Three* (I, O) - In Bus Mode 4, this signal enables data transfer on byte lane D(31:24).

Table 1. Interface Signals (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Description (Slave Type, Master Type)
A0	A0	BLE/	BE0/	A0 - *Address Line Zero* (I,O) - Address line zero to the host bus memory, used in Bus Modes 1, 2 and 3 BE0/ - *Byte Enable Zero* (I,O) - In Bus Mode 4, this signal enables data transfer on the low order byte lane D(7-0). BLE/ - Byte Low Enable (I, O) - In Bus Mode 3, this signal enables data transfer on the low order byte lane D(7-0).
A1	A1	A1	BE1/	A1 - *Address Line One* (I, O) - Address Line One to the host bus memory in Bus Modes 1, 2 and 3. BE1/ - *Byte Enable One* (I,O) - In Bus Mode 4, this signal enables data transfer on byte lane D(15-8).
STERM/	TA/	READYI/	READYI/	STERM/ - *Synchronous Cycle Termination* (I/O, I) - In Bus Mode 1, this signal acknowledges transfer to a 32-bit wide port TA/ - *Transfer Acknowledge* (I/O, I) - In Bus Mode 2, this signal acknowledges transfer to a 32-bit wide port. READYI/ - *Ready In* (I, I) - In Bus Modes 3 and 4 during master mode operation, this signal indicates that the slave device is ready to transfer data. During slave mode, this signal is monitored by the 53C720 to determine when to stop driving the bus.
BERR/	TEA/	TEA/	TEA/	BERR/ -*Bus Error Acknowledge* (O, I) - In Bus Mode 1, this indicates that a bus fault has occurred. Used with HALT/ to force a bus retry. Will be asserted on an illegal slave access. TEA/ - *Transfer Error Acknowledge* (O, I) - Indicates that a bus fault has occurred in Bus Modes 2, 3, or 4. Used in conjunction with TA/-READYI/ to force a bus retry. Will be asserted on an illegal slave access
HALT/	TIP/	TIP/	TIP/	HALT/ (Z, I/O) - Input ONLY in Bus Mode 1, used with BERR/ to indicate a bus retry cycle. TIP/ - *Transfer in Progress* (Z, I/O) - Bidirectional signal for Bus Modes 2, 3 and 4, indicating that bus activity is in progress.

NCR 53C720

Table 1. Interface Signals (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Description (Slave Type, Master Type)
SLACK/	SLACK/	READYO/	READYO/	SLACK/ - *Slave Acknowledge* (O, O) - Asserted in Bus Modes 1 and 2 to indicate the internal end of a valid slave mode cycle. The external slave cycle ends when the 53C720 observes either STERM/-TA/ or BERR/-TEA.
				READYO/ -*Ready Out* (O, Z) - Asserted in Bus Modes 3 and 4 to indicate the end of a slave mode cycle.
FC(2-0)	TM(2-0)	FC(2-0)	FC(2-0)	*Function Codes and Transfer Modifier* For All Bus Modes: FC0-TM0 (Z, O) - Indicates the status of the current bus cycle. FC0-TM0 = 1 Indicates data space; it is the default for all transfers. FC0-TM0 = 0 Indicates program space. It may be optionally selected when setting the Program Data (PD) bit. FC1-TM1 (Z,O) - User Definable from register bits. FC2-TM2 (Z,O) - User definable from register bits. *Note:* If DCNTL (bit 6) is asserted, FC0 becomes a continuously enabled, general purpose output in all Bus Modes. FC1 becomes a continuously enabled, general purpose output in all bus modes, and FC2 becomes PA/ (Preview of Address). PA/ (I, I) -*Preview of Address* - Input signal only, used to tell the 53C720 that the system is ready for the next address/ value and byte enable signals.
SC(1:0)	SC(1:0)	SC(1:0)	SC(1:0)	SC - *Snoop Control* (Z(O), O) - Indicates the bus snooping level in all bus modes. The bits are user programmable through register bits. They are asserted when the 53C720 is bus master (SC(1:0) may be optionally used as pure outputs, active in both master and slave modes.)
MASTER/	MASTER/	MASTER/	MASTER/	*Master Status* (O, O) - Driven low when the 53C720 becomes bus master. This signal is valid in all bus modes.

Table 1. Interface Signals (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Description (Slave Type, Master Type)
FETCH/	FETCH/	FETCH/	FETCH/	*Fetching Op Code* (O, O) - In all bus modes, this signal indicates that the next bus request will be for an op code fetch.
CBREQ/	TT1/	TT1/	TT1/	CBREQ/ - *Cache Burst Request* (Z, O) - In Bus Mode 1, Cache Burst Request indicates an attempt to execute a line transfer of four long words. TT1/ - Transfer Type Bit One (Z, O) - Transfer Type Bit One is a three-state output line indicating the current bus transfer type in all four bus modes This bit can be programmed from a register bit (default = 0). It is only asserted when the 53C720 is bus master.
CBACK/	TBI/	TBI/	TBI/	CBACK/ - *Cache Burst Acknowledge* (O, I) - In Bus Mode 1, this signal indicates that the memory system or 53C720 can handle a burst request. In slave mode this signal is deasserted in response to CS/. TBI/ - *Transfer Burst Inhibit* (O, I) - In Bus Modes 2, 3 and 4, Transfer Burst Inhibit indicates that the memory or the 53C720 cannot handle a burst request at this time. In slave mode this signal is asserted in response to CS/.
BS(2:0)	BS(2:0)	BS(2:0)	BS(2:0)	*Bus Mode Select* (I, I) – This signal is active in all four bus modes. It selects between Motorola/Intel (BS2), Big/Little Endian (BS1) and 386sx/_030 and 386dx/_040 (BS0).

BS2	BS1	BS0	Bus Mode
0	0	0	80386DX-like, Little Endian, Bus Mode 4
0	0	1	80386SX-like, Little Endian, Bus Mode 3
0	1	0	80386DX-like, Big Endian, Bus Mode 4
0	1	1	Reserved
1	0	0	68040-like, Little Endian, Bus Mode 2
1	0	1	68030-like, Little Endian, Bus Mode 1
1	1	0	68040-like, Big Endian, Bus Mode 2
1	1	1	68030-like, Big Endian, Bus Mode 1

NCR 53C720

Table 1. Interface Signals (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Description (Slave Type, Master Type)
AUTO/	AUTO/	AUTO/	AUTO/	*SCRIPTS Autostart Mode* (I, I) – In all bus modes, this signal selects between automatic SCRIPTS start and manual SCRIPTS start modes. AUTO/ = 0 Auto start. The DMA SCRIPT pointer register (DSP) will point to an address of all zeroes following a chip reset. This address is the starting address of the SCRIPT instructions. The SCRIPTS will automatically be fetched and executed until an interrupt instruction occurs. AUTO/ = 1 Manual start. The DMA SCRIPT pointer register (DSP) must be written to so that it points to the starting address of the SCRIPT instructions. The SCRIPTS will automatically be fetched and executed until an interrupt condition occurs.
GPI(3:0)	GPI(3:0)	GPI(3:0)	GPI(3:0)	*General Purpose Input* (I, I) – In all bus modes, this signal detects the input signal of the connected device. It can read the 53C720's ID or other configuration information.
GPO	GPO	GPO	GPO	*General Purpose Output* (O, O) - In all bus modes, outputs a user selected output signal. This feature can be used to enable attached RAM, ROM, LEDs, etc.
DIFFSENS	DIFFSENS	DIFFSENS	DIFFSENS	*Differential Sense* (I, I) – This pin detects the presence of a single-ended device on a differential system. When using external differential transceivers and a zero is detected on this pin, all chip SCSI outputs will be tristated to avoid damage to the transceivers. When running in single-ended mode, this pin should be tied high. The normal value of this pin is L
SCLK	SCLK	SCLK	SCLK	*SCSI Clock* (I, I) - SCLK is used to derive all SCSI-related timings. The speed of this clock will be determined by the application's requirements; in some applications SCLK and BCLK may be tied to the same source.

Table 1. Interface Signals (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Description (Slave Type, Master Type)
SDATA/	SDATA/	SDATA/	SDATA/	*SCSI Data* (I/O, I/O) - Includes the following data lines and parity signals for all Bus Modes.
				SD15-0/ 16-bit SCSI data bus
				SDP0/ SCSI data parity bit (byte 7-0)
				SDP1/ SCSI data parity bit (byte 15-8)
SCTRL/	SCTRL/	SCTRL/	SCTRL/	*SCSI Control* (I/O, I/O)
				CD/ SCSI phase line, command/data
				IO/ SCSI phase line, input/output
				MSG/ SCSI phase line, message
				REQ/ Data handshake signal from target device
				ACK/ Data handshake signal from initiator device
				BSY/ SCSI bus arbitration signal, signal busy
				SEL/ SCSI bus arbitration signal, select device
				ATN/ Attention, the initiator is requesting a message out phase.
				RST/ SCSI bus reset.
SDIR(15-0)	SDIR(15-0)	SDIR(15-0)	SDIR(15-0)	*Differential Support Lines* (O, O) - Driver direction control for SCSI data lines.
SDIRP0	SDIRP0	SDIRP0	SDIRP0	*Differential Support Line* - (O, O) Driver direction control for SCSI parity signal (byte (7-0)).
SDIRP1	SDIRP1	SDIRP1	SDIRP1	*Differential Support Line* (O, O) - Driver direction control for SCSI parity signal (byte(15-8)).

NCR 53C720

Table 1. Interface Signals (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Description (Slave Type, Master Type)
BSYDIR	BSYDIR	BSYDIR	BSYDIR	*Differential Support Line* (O, O) - Driver enable control for SCSI BSY/ signal.
SELDIR	SELDIR	SELDIR	SELDIR	*Differential Support Line* (O, O) - Driver enable control for SCSI SEL/ signal.
RSTDIR	RSTDIR	RSTDIR	RSTDIR	*Differential Support Line* (O, O) - Driver enable control for SCSI RST/ signal.
IGS	IGS	IGS	IGS	*Differential Support Line* (O, O) - Direction control for initiator driver group.
TGS	TGS	TGS	TGS	*Differential Support Line* (O, O) - Direction control for target driver

Chapter 5

Registers

This section contains descriptions of all 53C720 registers. Table 5-1 summarizes the 53C720 register set. Figure 5-1, the register map, lists registers by both their Big and Little Endian addresses. The Big Endian Address for each register is shown in parentheses. The terms "set" and "assert" are used to refer to bits that are programmed to a binary one. Similarly, the terms "deassert," "clear" and "reset" are used to refer to bits that are programmed to a binary zero. Reserved bits are designated as "RES" in each register diagram. These bits should always be written to zero; *mask all information read from them.*

Reserved bit functions may be changed at any time. Unless otherwise indicated, all bits in registers are active high, i.e., the feature is enabled by setting the bit. The bottom of every register diagram shows the default register values, which are enabled after the chip is powered on or reset. Registers can be addressed as bytes, words or longwords. Other access sizes can result in bus errors. The only register that the host CPU can access while the 53C720 is executing SCRIPTS is the ISTAT register; attempts to access other registers will interfere in the operation of the chip. However, all registers are accessible via SCRIPTS.

Table 5-1. Register Addresses and Descriptions

Little Endian Address	Big Endian Address	Read/ Write	Label	Description
00	03	R/W	SCNTL0	SCSI Control 0
01	02	R/W	SCNTL1	SCSI Control 1
02	01	R/W	SCNTL2	SCSI Control 2
03	00	R/W	SCNTL3	SCSI Control 3
04	07	R/W	SCID	SCSI Chip ID
05	06	R/W	SXFER	SCSI Transfer
06	05	R/W	SDID	SCSI Destination ID
07	04	R/W	GPREG	General Purpose
08	0B	R/W	SFBR	SCSI First Byte Received
09	0A	R/W	SOCL	SCSI Output Control Latch
0A	09	R	SSID	SCSI Selector ID
0B	08	R/W	SBCL	SCSI Bus Control Lines
0C	0F	R	DSTAT	DMA Status
0D	0E	R	SSTAT0	SCSI Status 0
0E	0D	R	SSTAT1	SCSI Status 1
0F	0C	R	SSTAT2	SCSI Status 2
10-13	10-13	R/W	DSA	Data Structure Address
14	17	R/W	ISTAT	Interrupt Status
18	1B	R/W	CTEST0	Chip Test 0
19	1A	R	CTEST1	Chip Test 1
1A	19	R	CTEST2	Chip Test 2
1B	18	R	CTEST3	Chip Test 3

NCR 53C720

Table 5-1. Register Addresses and Descriptions (Continued)

Little Endian Address	Big Endian Address	Read/ Write	Label	Description
1C-1F	1C-1F	R/W	TEMP	Temporary stack
20	23	R/W	DFIFO	DMA FIFO
21	22	R/W	CTEST4	Chip Test 4
22	21	R/W	CTEST5	Chip Test 5
23	20	R/W	CTEST6	Chip Test 6
24-26	25-27	R/W	DBC	DMA Byte Counter
27	24	R/W	DCMD	DMA Command
28-2B	28-2B	R/W	DNAD	DMA Next Address for Data
2C-2F	2C-2F	R/W	DSP	DMA SCRIPTS Pointer
30-33	30-33	R/W	DSPS	DMA SCRIPTS Pointer Save
34-37	34-37	R/W	SCRATCH A	General Purpose Scratch Pad A
38	3B	R/W	DMODE	DMA Mode
39	3A	R/W	DIEN	DMA Interrupt Enable
3A	39	R/W	DWT	DMA Watchdog Timer
3B	38	R/W	DCNTL	DMA Control
3C-3F	3C-3F	R	ADDER	Sum output of internal adder
40	43	R/W	SIEN0	SCSI Interrupt Enable 0
41	42	R/W	SIEN 1	SCSI Interrupt Enable 1
42	41	R	SIST0	SCSI Interrupt Status 0
43	40	R	SIST1	SCSI Interrupt Status 1
44	47	R/W	SLPAR	SCSI Longitudinal Parity
45	46	R	SWIDE	SCSI Wide Residue Data
48	4A	R/W	STIME0	SCSI Timer 0
49	4B	R/W	STIME1	SCSI Timer 1
4C	4F	R	STEST0	SCSI Test 0
4D	4E	R	STEST1	SCSI Test 1
4E	4D	R/W	STEST2	SCSI Test 2
4F	4C	R/W	STEST3	SCSI Test 3
50-51	52-53	R	SIDL	SCSI Input Data Latch
54-55	56-57	R/W	SODL	SCSI Output Data Latch
58-59	5A-5B	R	SBDL	SCSI Bus Data Lines
5C-5F	5C-5F	R/W	SCRATCH B	General Purpose Scratch Pad B

Figure 5-1. Register Address Map

Big Endian Mode ⟹

SCRIPTS and Little Endian Mode ⟸

00	SCNTL 3	SCNTL2	SCNTL1	SCNTL0	00
04	GPREG	SDID	SXFER	SCID	04
08	SBCL	SSID	SOCL	SFBR	08
0C	SSTAT2	SSTAT1	SSTAT0	DSTAT	0C
10	DSA				10
14	RESERVED			ISTAT	14
18	CTEST3	CTEST2	CTEST1	CTEST0	18
1C	TEMP				1C
20	CTEST6	CTEST5	CTEST4	DFIFO	20
24	DCMD	DBC			24
28	DNAD				28
2C	DSP				2C
30	DSPS				30
34	SCRATCH A				34
38	DCNTL	DWT	DIEN	DMODE	38
3C	ADDER				3C
40	SIST1	SIST0	SIEN1	SIEN0	40
44	RESERVED		SWIDE	SLPAR	44
48	RESERVED		STIME1	STIME0	48
4C	STEST3	STEST2	STEST1	STEST0	4C
50	RESERVED		SIDL		50
54	RESERVED		SODL		54
58	RESERVED		SBDL		58
5C	SCRATCH B				5C

NCR 53C720

Register 00 (03)   SCSI Control 0 (SCNTL0)

Read/Write

ARB1	ARB0	START	WATN/	EPC	EPG	AAP	TRG
7	6	5	4	3	2	1	0

Default >>>

1	1	0	0	0	0	0	0

Bit 7   ARB1 (Arbitration mode bit 1)

Bit 6   ARB0 (Arbitration mode bit 0)

ARB1	ARB0	Arbitration Mode
0	0	Simple arbitration
0	1	Reserved
1	0	Reserved
1	1	Full arbitration, selection or reselection

Simple Arbitration

1) The 53C720 waits for a bus free condition to occur.

2) It asserts BSY/ and its SCSI ID (contained in the SCID register) onto the SCSI bus

   If the SEL/ signal is asserted by another SCSI device, the 53C720 will deassert BSY/, deassert its ID and set the Lost Arbitration bit (bit 3) in the SSTAT0 register.

3) After an arbitration delay, the CPU should read the SBDL register to check if a higher priority SCSI ID is present. If no higher priority ID bit is set, and the Lost Arbitration bit is not set, the 53C720 has won arbitration.

4) Once the 53C720 has won arbitration, SEL must be asserted via the SOCL for a bus clear plus a bus settle delay (1.2 µs) before a low level selection can be performed.

Full Arbitration, Selection/Reselection

1) The 53C720 waits for a bus free condition.

2) It asserts BSY/ and its SCSI ID (the highest priority ID stored in the SCID register) onto the SCSI bus.

3) If the SEL/ signal is asserted by another SCSI device or if the 53C720 detects a higher priority ID, the 53C720 will deassert BSY/, deassert its ID, and wait until the next bus free state to try arbitration again.

4) The 53C720 repeats arbitration until it wins control of the SCSI bus. When it has won, the Won Arbitration bit is set in the SSTAT0 register, bit 2.

5) The 53C720 performs selection by asserting the following onto the SCSI bus: SEL/, the target's ID (stored in the SDID register) and the 53C720's ID (the highest priority ID stored in the SCID register).

6) After a selection is complete, the Function Complete bit is set in the SIST0 register, bit 6.

7) If a selection timeout occurs, the Selection Timeout bit is set in the SIST1 register, bit 2.

Bit 5   START (Start sequence)
When this bit is set, the 53C720 will start the arbitration sequence indicated by the Arbitration Mode bits. The Start Sequence bit is used in low level mode; when executing SCSI SCRIPTS, this bit is controlled by the SCRIPTS processor. An arbitration sequence should not be started if the connected bit in the SCNTL1 register, bit 4, indicates that 53C720 is already connected to the SCSI bus.

This bit is automatically cleared when the arbitration sequence is complete. If a sequence is aborted, bit 4 in the SCNTL1 register should be checked to verify that the 53C720 did not connect to the SCSI bus.

Bit 4   WATN (Select with ATN/ on a start sequence)
When this bit is set and the 53C720 is in initiator mode, the SCSI ATN/ signal will be asserted during 53C720 selection of a target device. This is to inform the target that the 53C720 has a message to send. If a selection timeout occurs while attempting to select a target device, ATN/ will be deasserted at the same time SEL/ is deasserted.

When this bit is clear, the ATN/ signal will not be asserted during selection.

When executing SCSI SCRIPTS, this bit is controlled by the SCRIPTS processor, but it may be set manually in low level mode.

Bit 3   EPC (Enable parity checking)
When this bit is set, the SCSI data bus is checked for odd parity when data is received from the SCSI bus in either initiator or target mode. The host data bus is checked for odd parity if bit 2, the Enable Parity Generation bit, is cleared. Host data bus parity is checked as data is loaded into the SODL register when sending SCSI data in either

initiator or target mode. If a parity error is detected, bit 0 of the SSTAT0 register is set and an interrupt may be generated.

If the 53C720 is operating in initiator mode and a parity error is detected, ATN/ can optionally be asserted, but the transfer continues until the target changes phase.

When this bit is cleared, parity errors are not reported.

Bit 2   EPG (Enable parity generation/parity through)

When this bit is set, the SCSI parity bit will be generated by the 53C720. The host data bus parity lines DP(3-0) are ignored and should not be used as parity signals. When this bit is cleared, the parity present on the host data parity lines will flow through the 53C720's internal FIFOs and be driven onto the SCSI bus when sending data (if the host bus is set to even parity, it is changed to odd before it is sent to the SCSI bus).

This bit is set to enable the DP3_ABRT/ pin to function as an abort input (ABRT/).

Bit 1   AAP (Assert ATN/ on parity error)

When this bit is set, the 53C720 automatically asserts the SCSI ATN/ signal upon detection of a parity error. ATN/ is only asserted in initiator mode. The ATN/ signal is asserted before deasserting ACK/ during the byte transfer with the parity error. The Enable Parity Checking bit must also be set for the 53C720 to assert ATN/ in this manner. The following parity errors can occur:

1) A parity error detected on data received from the SCSI bus.

2) A parity error detected on data transferred to the 53C720 from the host data bus.

If the Assert ATN/ on Parity Error bit is cleared or the Enable Parity Checking bit is cleared, ATN/ will not be automatically asserted on the SCSI bus when a parity error is received.

Bit 0   TRG (Target mode)

This bit determines the default operating mode of the 53C720. The user must manually set target or initiator mode. This can be done using the SCRIPTS language (SET target or CLEAR target).

When this bit is set, the chip is a target device by default. When the target mode bit is cleared, the 53C720 is an initiator device by default.

Register 01 (02)   SCSI Control One (SCNTL1)

Read/Write

EXC 7	ADB 6	DHP 5	CON 4	RST 3	AESP 2	IARB 1	SST 0

Default >>>

0	0	0	0	0	0	0	0

Bit 7   EXC (Extra clock cycle of data setup)

When this bit is set, an extra clock period of data setup is added to each SCSI data transfer. The extra data setup time can provide additional system design margin, though it will affect the SCSI transfer rates. Clearing this bit disables the extra clock cycle of data setup time.

Bit 6   ADB (Assert SCSI data bus)

When this bit is set, the 53C720 drives the contents of the SCSI Output Data Register (SODL) onto the SCSI data bus. When the 53C720 is an initiator, the SCSI I/O signal must be inactive to assert the SODL contents onto the SCSI bus. The low order data and parity signal will always be asserted onto the SCSI bus, whereas the high order data and parity signal will only be asserted onto the SCSI bus if the Enable Wide SCSI bit (SCNTL3, bit 3) is asserted and a data phase is specified by the data phase signals. When the 53C720 is a target, the SCSI I/O signal must be active for the SODL contents to be asserted onto the SCSI bus. The contents of the SODL register can be asserted at any time, even before the 53C720 is connected to the SCSI bus. This bit should be cleared when executing SCSI SCRIPTS. It is normally used only for diagnostics testing or operation in low level mode.

Bit 5   DHP (Disable Halt on Parity Error or ATN) (Target Only)

The DHP bit is only defined for target mode. When this bit is cleared, the 53C720 halts the SCSI data transfer when a parity error is detected or when the ATN/ signal is asserted. If ATN/ or a parity error is received in the middle of a data transfer, the 53C720 may transfer up to three additional bytes (or words, if wide SCSI is enabled) before halting to synchronize between internal core cells. During synchronous operation, the 53C720 transfers data until there are no outstanding synchronous offsets. If the

NCR 53C720

53C720 is receiving data, any data residing in the SCSI or DMA FIFOs is sent to memory before halting. while sending data in target mode with pass parity enabled, the byte with the parity error will not be sent across the SCSI bus.

When this bit is set, the 53C720 does not halt the SCSI transfer when ATN/ or a parity error is received.

Bit 4   CON (Connected)
This bit is automatically set anytime the 53C720 is connected to the SCSI bus as an initiator or as a target. It will be set after successfully completing arbitration or when the 53C720 has responded to a bus initiated selection or reselection. It will also be set after successfully completing simple arbitration when operating in low level mode. When this bit is clear, the 53C720 is not connected to the SCSI bus.

The CPU can force a connected or disconnected condition by setting or clearing this bit. This feature would be used primarily during loopback mode.

Bit 3   RST (Assert SCSI RST/ signal)
Setting this bit asserts the SCSI RST/ signal. The RST/ output remains asserted until this bit is cleared. The 25 μs minimum assertion time defined in the SCSI specification must be timed out by the controlling microprocessor or a SCRIPT loop.

Bit 2   AESP (Assert even SCSI parity (force bad parity))
When this bit is set and the Enable Parity Generation bit is set (bit 2) in the SCNTL0 register, the 53C720 asserts even parity. It forces a SCSI parity error on each byte sent to the SCSI bus from the 53C720. If parity checking is enabled, then the 53C720 checks data received for odd parity. This bit is used for diagnostic testing and should be clear for normal operation. It can be used to generate parity errors to test error handling functions.

Bit 1   IARB (Immediate Arbitration)
Setting this bit will cause the SCSI core to immediately begin arbitration once a BUS FREE phase is detected following an expected SCSI disconnect. This bit is useful for multi-threaded applications. The ARB1-0 bits in SCNTL0 should be set for full arbitration and selection before setting Immediate Arbitration.

Arbitration will be re-tried until won. At that point, the 53C720 will hold BSY and SEL asserted, and wait for a select or reselect sequence to be requested. The Immediate Arbitration bit will be reset automatically when the selection or reselection sequence is completed, or times out.

An unexpected disconnect condition will clear IARB without attempting arbitration. See the SCSI Disconnect Unexpected bit (SCNTL2 bit 7) for more information on expected versus unexpected disconnects.

An immediate arbitration sequence can be aborted. First, the abort bit in the SCRIPTS processor registers should be set. Then one of two things will eventually happen:

1) The Won Arbitration bit (SSTAT0 bit 2) will be asserted. In this case, the Immediate Arbitration bit needs to be reset. This will complete the abort sequence and disconnect the 53C720 from the SCSI bus. If it is not acceptable to go to BUS FREE phase immediately following the arbitration phase, a low level selection may instead be performed.

2) The abort will complete because the 53C720 loses arbitration. This can be detected by the Immediate Arbitration bit being deasserted. The Lost Arbitration bit (SSTAT0 bit 3) should not be used to detect this condition. No further action needs to be taken in this case.

Bit 0   SST (Start SCSI Transfer)
This bit is automatically set during SCRIPTS execution, and should not be used. It causes the SCSI core to begin a SCSI transfer, including REQ/ACK handshaking. The determination of whether the transfer is a send or receive is made according to the value written to the I/O bit in SOCL. This bit is self-resetting. This bit should not be set for low level operation.

Register 02 (01) SCSI Control Register 2 (SCNTL2)

Read/Write

SDU	CHM	RES	RES	WSS	RES	RES	WSR
7	6	5	4	3	2	1	0

Default >>>

0	0	X	X	0	X	X	0

Bit 7   SDU   (SCSI Disconnect Unexpected)

When this bit is set, the SCSI core is not expecting the SCSI bus to enter the BUS FREE phase. If it does, an unexpected disconnect error will be generated (see the Unexpected Disconnect bit in the SIST0 register, bit 2).

During normal SCRIPTS mode operation, this bit is set automatically whenever the SCSI core is reselected, or successfully selects another SCSI device. The SDU bit should be reset with a register write before the SCSI core expects a disconnect to occur, normally prior to sending an ABORT, ABORT TAG, BUS DEVICE RESET, CLEAR QUEUE or RELEASE RECOVERY message, or before deasserting ACK after receiving a DISCONNECT command or COMMAND COMPLETE message.

Bit 6   CHM   (Chained Mode)
This bit determines whether or not the SCSI core is programmed for chained SCSI mode. This bit is automatically set by the Chained Block Move (CHMOV) SCRIPTS instruction and is automatically cleared by the Block Move SCRIPTS instruction (MOVE).

Chained mode is primarily used to transfer consecutive wide data blocks. Using chained mode facilitates partial receive transfers and allows correct partial send behavior. When this bit is set and a data transfer ends on an odd byte boundary, the 53C720 will store the last byte in the SCSI Wide Residue Data Register during a receive operation or in the SCSI Output Data Latch register during a send operation. This byte will be combined with the first byte from the subsequent transfer so that a wide transfer can be completed.

Bits 5-4   Reserved
Bit 3   WSS   (Wide SCSI Send)
When read, this bit returns the value of the Wide SCSI Send (WSS) flag. Asserting this bit will clear the WSS flag. This clearing function is self-resetting.

When the WSS flag is high following a wide SCSI send operation, the SCSI core is holding a byte of "chain" data in the SODL register. This data will become the first low-order byte sent when "married" with a high-order byte during a subsequent data send transfer.

Performing a SCSI receive operation will clear this bit. Also, performing any non-wide transfer will clear this bit.

Bits 2-1   Reserved
Bit 0   WSR   (Wide SCSI Receive)
When read, this bit returns the value of the Wide SCSI Receive (WSR) flag. Asserting this bit will clear the WSR flag. This clearing function is self-resetting.

The WSR flag indicates that the SCSI core received data from the SCSI bus, detected a possible partial transfer at the end of a chained or non-chained block move command, and temporarily stored the high-order byte in the SWIDE register rather than passing the byte out the DMA channel. The hardware uses the WSR status flag to determine what behavior must occur at the start of the next data receive transfer. When the flag is set, the stored data in SWIDE may be "residue" data, valid data for a subsequent data transfer, or overrun data. The byte may be read as normal data by starting a data receive transfer.

Performing a SCSI send operation will clear this bit. Also, performing any non-wide transfer will clear this bit.

NCR 53C720

Register 03 (00) SCSI Control 3 (SCNTL3)

Read/Write

RES	SCF2	SCF1	SCF0	EWS	CCF2	CCF1	CCF0
7	6	5	4	3	2	1	0

Default >>>

X	0	0	0	0	0	0	0

Bit 7   Reserved
Bits 6-4   SCF2-0   (Synchronous Clock Conversion Factor)

These bits select a factor by which the frequency of SCLK is divided before being presented to the synchronous SCSI control logic. They should be written to the same value as the Clock Conversion Factor bits below unless fast SCSI operation is desired. They are encoded as follows. All other combinations are reserved for future combinations and should never be used.

SCF2 CCF2	SCF1 CCF1	SCF0 CCF0	Factor	SCSI Clock Frequency (MHz)
0	0	0	SCLK / 3	50.01-75
0	0	1	SCLK / 1	16.67-25
0	1	0	SCLK / 1.5	25.01-37.5
0	1	1	SCLK / 2	37.51-50
1	0	0	SCLK / 3	50.01-66
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Reserved	

Bit 3 EWS   (Enable Wide SCSI)
When this bit is deasserted all information transfer phases are assumed to be eight bits, transmitted on SD7-0/, SDP0/. When this bit is asserted, data transfers are done 16 bits at a time with the least significant byte on SD7-0/, SDP/ and the most significant byte on SD15-8/, SDP1/. Command, status, and message phases remain eight bits.

Bits 2-0   CCF2-0   (Clock Conversion Factor)
These bits select a factor by which the frequency of SCLK is divided before being presented to the SCSI core. The bits are encoded as shown in the description of bits 6-4. All other combinations are reserved for future expansion and should never be used. Also note that the synchronous portion of the SCSI core can be run at a different clock rate for fast SCSI. See the synchronous clock conversion factor bits above. *Note:* It is important that these bits be set to the proper values to guarantee that the 53C720 meets the SCSI timings as defined by the ANSI specification.

Register 04 (07)   SCSI Chip ID (SCID)

Read/Write

RES 7	RRE 6	SRE 5	RES 4	ID3 3	ID2 2	ID1 1	ID0 0

Default >>>

X	0	0	X	0	0	0	0

Bit 7   Reserved

Bit 6   RRE   (Enable Response to Reselection)
When this bit is set, the 53C720 is enabled to respond to bus-initiated reselection at the chip ID encoded in this register. Note that the 53C720 will not automatically reconfigure itself to initiator mode as a result of being reselected.

Bit 5   SRE   (Enable Response to Selection)
When this bit is set, the 53C720 is enabled to respond to bus-initiated selection at the chip ID encoded in this register. Note that the 53C720 will not automatically reconfigure itself to target mode as a result of being selected.

Bit 4   Reserved

Bits 3-0   Encoded 53C720 Chip SCSI ID, bits 3-0
These bits are used to store the 53C720 encoded SCSI ID. This is the ID which the chip will assert when arbitrating for the SCSI bus, and the ID to which it will respond during bus-initiated selection or reselection. The priority of the sixteen possible IDs, in descending order is:

Highest   Lowest

7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8

Register 05 (06)   SCSI Transfer (SXFER)

Read/Write

TP2 7	TP1 6	TP0 5	RES 4	MO3 3	MO2 2	MO1 1	MO0 0

Default >>>

0	0	0	X	0	0	0	0

Note: When using Table Indirect I/O commands, bits 7-5 and 3-0 of this register will be loaded from the I/O data structure.

Bits 7-5   TP2-0   (SCSI Synchronous Transfer Period)
These bits determine the SCSI synchronous transfer period used by the 53C720 when sending synchronous SCSI data in either initiator or target mode. See the following table:

TP2	TP1	TP0	XFERP
0	0	0	4
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	9
1	1	0	10
1	1	1	11

NCR 53C720

The synchronous transfer period the 53C720 should use when transferring SCSI data is found as in the followig an example: The 53C720 is interfaced to a hard disk which can transfer data at 10 Mbytes/sec synchronously. The 53C720's SCLK is running at 40 MHz . The synchronous transfer period (SXFERP) is found as follows:

$$SXFERP = Period/SSCP + ExtCC$$

$$Period = 1 \div Frequency = 1 \div 10 \ Mbytes/sec = 100 \ ns$$

$$SSCP = 1 \div SSCF = 1 \div 40 \ MHz = 25 \ ns$$

(This SCSI synchronous core clock is determined in SCNTL3 bits 6-4).

ExtCC = 1 if SCNTL1 bit 7 is asserted and the 53C720 is sending data.

(ExtCC = 0 if the 53C720 is receiving data.)

$$SXFERP = 100 \div 25 = 4$$

Key: SXFERP = Synchronous transfer period

SSCP = SCSI Synchronous core period

SSCF = SCSI Synchronous core frequency

ExtCC = Extra clock cycle of data setup

Examples of synchronous transfer periods for SCSI-1 transfer rates.

CLK (MHz)	SCSI CLK ÷ SCNTL3 bits 6-4	XFERP	Synch Transfer Period (ns)	Synch Transfer Rate (MB/S)
66.67	÷ 3	4	180	5.55
66.67	÷ 3	5	225	4.44
50	÷ 2	4	160	6.25
50	÷ 2	5	200	5
40	÷ 2	4	200	5
37.50	÷ 1.5	4	160	6.25
33.33	÷ 1.5	4	180	5.55
25	÷ 1	4	160	6.25
20	÷ 1	4	200	5
16.67	÷ 1	4	240	4.17

Example transfer periods for fast SCSI-2 transfer rates.

CLK (MHz)	SCSI CLK ÷ SCNTL bits 6-4	XFERP	Synch Transfer Period (ns)	Synch Transfer Rate (MB/S)
66.67	÷ 1.5	4	90	11.11*
66.67	÷ 1.5	5	112.5	8.88
50	÷ 1	4	80	12.5*
50	÷ 1	5	100	10.0
40	÷ 1	4	100	10.0
37.50	÷ 1	4	106.67	9.375
33	÷ 1	4	120	8.33
25	÷ 1	4	160	6.25
20	÷ 1	4	200	5
16.67	÷ 1	4	240	4.17

*Violates SCSI specifications. Slower rates are achieved by using larger XFERP values and/or different SCLK prescale values.

Bit 4   Reserved
Bits 3-0   MO3-MO0 (Max SCSI synchronous offset)
These bits describe the maximum SCSI synchronous offset used by the 53C720 when transferring synchronous SCSI data in either initiator or target mode. The following table describes the possible combinations and their relationship to the synchronous data offset used by the 53C720. These bits determine the 53C720's method of transfer for Data In and Data Out phases only; all other information transfers will occur asynchronously.

MO3	MO2	MO1	MO0	Synchronous Offset
0	0	0	0	0 – Asynchronous
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	X	X	1	Reserved
1	X	1	X	Reserved
1	1	X	X	Reserved

Register 06 (05) SCSI Destination ID (SDID)

Read/Write

RES 7	RES 6	RES 5	RES 4	ID3 3	ID2 2	ID1 1	ID0 0

Default >>>

X	X	X	X	0	0	0	0

Bits 7-4   Reserved

Bits 3-0   Encoded destination SCSI ID bits 3-0

Writing these bits sets the SCSI ID of the intended initiator or target during SCSI reselection or selection phases respectively. When executing SCSI SCRIPTS, the SCRIPTS processor writes the destination SCID to this register. The SCSI ID is defined by the user in a SCSI SCRIPTS SELECT or RESELECT instruction. The value written should be the binary-encoded ID value. The priority of the sixteen possible IDs, in descending order, is:

Highest	Lowest
7 6 5 4 3 2 1 0 15 14 13 12 11 10 9 8	

Register 07 (04)   Read/Write General Purpose (GPREG)

Read/Write

RES 7	RES 6	RES 5	GPO 4	GPI3 3	GPI2 2	GPI1 1	GPI0 0

Default >>>

X	X	X	0	X	X	X	X

Bits 7-5   Reserved
Bit 4   GPO (General Purpose Output)
This bit allows the user to enable or disable a user-defined output signal (GPO pin) on the 53C720. The general purpose output feature may be used to enable attached ROM, RAM, LEDs, etc., on a 53C720 board.

Bits 3-0   GPI3-0   (General Purpose Inputs)
These bits allow the 53C720 to detect the input signals of a connected device. The general purpose inputs can be used to sense the 53C720 chip ID or board configuration at power up. A Register-to-Register Move instruction may be used to move the sensed value into the appropriate register. These are live signals; if the pin is changing, the data is also changing. *Note:* The input pins all have internal pull-ups.

NCR 53C720

Register 08 (0B)   SCSI First Byte Received (SFBR)

Read/Write

7	6	5	4	3	2	1	0

Default >>>

0	0	0	0	0	0	0	0

Bits 7-0   1B7-1B0 (First byte received)
This register contains the first byte received in any asynchronous information transfer phase. For example, when the 53C720 is operating in initiator mode, this register contains the first byte received in Message In, Status Phase, Reserved In and Data In.

When a Block Move Instruction is executed for a particular phase, the first byte received is stored in this register - even if the present phase is the same as the last phase. The first byte-received value for a particular input phase is not valid until after a MOVE instruction is executed.

This register is also the accumulator for register read-modify-writes with the SFBR as the destination. This allows bit testing after an operation.

The SFBR is not writable via the CPU, and therefore not by a Memory Move. However, it can be loaded via SCRIPT Read/Write operations. To load the SFBR with a byte stored in system memory, the byte must first be moved to an intermediate 53C720 register (such as the SCRATCH register), and then to the SFBR.

Register 09 (0A)   SCSI Output Control Latch (SOCL)

Read /Write

REQ 7	ACK 6	BSY 5	SEL 4	ATN 3	MSG 2	C/D 1	I/O 0

Default >>>

0	0	0	0	0	0	0	0

Bit 7   REQ   (Assert SCSI REQ/ signal)

Bit 6   ACK   (Assert SCSI ACK/ signal)

Bit 5   BSY   (Assert SCSI BSY/ signal)

Bit 4   SEL   (Assert SCSI SEL/ signal)

Bit 3   ATN   (Assert SCSI ATN/ signal)

Bit 2   MSG   (Assert SCSI MSG/ signal)

Bit 1   C/D   (Assert SCSI C/D signal)

Bit 0   I/O - Assert SCSI I/O signal
This register is used primarily for diagnostic testing or programmed I/O operation. It is controlled by the SCRIPTS processor when executing SCSI SCRIPTS. SOCL should only be used when transferring data via programmed I/O. Some bits are set (1) or reset (0) when executing SCSI SCRIPTS. Do not write to the register once the 53C720 starts executing SCSI SCRIPTS.

Register 0A (09) SCSI Selector ID Register (SSID)

Read Only

VAL 7	RES 6	RES 5	RES 4	ID3 3	ID2 2	ID1 1	ID0 0

Default >>>

0	X	X	X	0	0	0	0

Bit 7   VAL (SCSI Valid Bit)

If VAL is asserted, the two SCSI IDs were detected on the bus during a bus-initiated selection or reselection, and the encoded destination SCSI ID bits below are valid. If VAL is deasserted, only one ID was present and the contents of the encoded destination ID are meaningless.

Bits 6-4   Reserved
Bits 3-0   Encoded Destination SCSI ID bits 3-0
Reading the SSID register immediately after the 53C720 has been selected or reselected returns the binary-encoded SCSI ID of the device which performed the operation. These bits are invalid for targets which are selected under the single initiator option of the SCSI-1 specification. This condition can be detected by examining the VAL bit above.

Register 0B (08) SCSI Bus Control Lines (SBCL)

Read Only

REQ 7	ACK 6	BSY 5	SEL 4	ATN 3	MSG 2	C/D 1	I/O 0

Default >>>

X	X	X	X	X	X	X	X

Bit 7   REQ (REQ/ status)
Bit 6   ACK (ACK/ status)
Bit 5   BSY (BSY/ status)
Bit 4   SEL (SEL/ status)
Bit 3   ATN (ATN/ status)
Bit 2   MSG (MSG/ status)
Bit 1   C/D (C/D status)
Bit 0   I/O (I/O status)

When read, this register returns the SCSI control line status. A bit will be set when the corresponding SCSI control line is asserted. These bits are not latched; they are a true representation of what is on the SCSI bus at the time the register is read; they may change while being read. This register can be used for diagnostics testing or operation in low level mode.

Register 0C (0F)   DMA Status (DSTAT)

Read Only

DFE	HPE	BF	ABRT	SSI	SIR	WTD	IID
7	6	5	4	3	2	1	0

Default >>>

1	0	0	0	0	0	0	0

Reading this register will clear any bits that are set at the time the register is read, but will not necessarily clear the register because additional interrupts may be pending (the 53C720 stacks interrupts). The ISTAT register will also be cleared. DMA interrupt conditions may be individually masked through the DIEN register.

When performing consecutive 8-bit reads of the DSTAT, SIST0 and SIST1 registers (in any order), insert a delay equivalent to 12 BCLK periods between the reads to ensure the interrupts clear properly. Also, if reading any of the registers when the ISTAT SIP and DIP bits may not be set, the SIST0 and SIST1 registers should be read before the DSTAT register to avoid missing a SCSI interrupt.

Bit 7   DFE (DMA FIFO empty)
This status bit is set when the DMA FIFO is empty. This bit may be changing at the time this register is read. It may be used to determine if any data resides in the FIFO when an error occurs and an interrupt is generated. This bit is a pure status bit and will not cause an interrupt.

Bit 6   HPE (Host Parity Error)

This bit is set when a host bus parity error is detected during a slave write or DMA read execution.

Bit 5   BF (Bus fault)
This bit is set when a host bus fault condition is detected. A host bus fault can only occur when the 53C720 is bus master, and is defined as a memory cycle that is ended by the assertion of BERR/ or TEA/.

Bit 4   ABRT (Aborted)
This bit is set when an abort condition occurs. An abort condition occurs because of the following: the DP3_ABRT/ input signal is asserted by another device (parity generation mode) or a software abort command is issued by setting bit 7 of the ISTAT register.

Bit 3   SSI (SCRIPT step interrupt)
If the Single-Step Mode bit in the DCNTL register is set, this bit will be set and an interrupt generated after successfully executing each SCRIPT instruction.

Bit 2   SIR (SCRIPT interrupt instruction received)
This status bit is set whenever an INTERRUPT instruction is evaluated as true.

Bit 1   WTD (Watchdog timeout detected)
This status bit is set when the watchdog timer decrements to zero. The watchdog timer is only used for the host memory interface. When the timer decrements to zero, it indicates that the memory system did not assert the acknowledge signal within the specified timeout period.

Bit 0   IID (Illegal instruction detected)
This status bit will be set anytime an illegal instruction is detected, whether the 53C720 is operating in single-step mode or automatically executing SCSI SCRIPTS.

This bit will also be set if the 53C720 is executing a Wait Disconnect instruction and the SCSI REQ line is asserted without a disconnect occurring.

Register 0D (0E)   SCSI Status Zero (SSTAT0)

Read Only

ILF	ORF	OLF	AIP	LOA	WOA	RST/	SDP/
7	6	5	4	3	2	1	0

Default >>>

| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7   ILF (SIDL least significant byte full)
This bit is set when the least significant byte in the SCSI Input Data Latch register (SIDL) contains data. Data is transferred from the SCSI bus to the SCSI Input Data Latch register before being sent to the DMA FIFO and then to the host bus. The SIDL register contains SCSI data received asynchronously. Synchronous data received does not flow through this register.

Bit 6   ORF (SODR least significant byte full)
This bit is set when the least significant byte in the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) contains data. The SODR register is used by the SCSI logic as a second storage register when sending data synchronously. It is a not accessible to the user (cannot be read or written). This bit can be used to determine how many bytes reside in the chip when an error occurs.

Bit 5   OLF (SODL least significant byte full)
This bit is set when the least significant byte in the SCSI Output Data Latch (SODL) contains data. The SODL register is the interface between the DMA logic and the SCSI bus. In synchronous mode, data is transferred from the host bus to the SODL register, and then to the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) before being sent to the SCSI bus. In asynchronous mode, data is transferred from the host bus to the SODL register, and then to the SCSI bus. The SODR buffer register is not used for asynchronous transfers. This bit can be used to determine how many bytes reside in the chip when an error occurs.

Bit 4   AIP (Arbitration in progress)
Arbitration in Progress (AIP = 1) indicates that the 53C720 has detected a bus free condition, asserted BSY and asserted its SCSI ID onto the SCSI bus.

Bit 3   LOA (Lost arbitration)
When set, LOA indicates that the 53C720 has detected a bus free condition, arbitrated for the SCSI bus, and lost arbitration due to another SCSI device asserting the SEL/ signal.

Bit 2   WOA (Won arbitration)
When set, WOA indicates that the 53C720 has detected a bus free condition, arbitrated for the SCSI bus and won arbitration. The arbitration mode selected in the SCNTL0 register must be full arbitration & selection for this bit to be set.

Bit 1   RST/ (SCSI RST/ signal)
This bit reports the current status of the SCSI RST/ signal, and the RST signal (bit 6) in the ISTAT register. This signal is not latched and may be changing when read.

Bit 0   SDP0/ (SCSI SDP0/ parity signal)
This bit represents the active high current status of the SCSI SDP0/ parity signal. This signal is not latched and may be changing as it is read.

NCR 53C720

Register 0E (0D)   SCSI Status One (SSTAT1)

Read Only

FF3	FF2	FF1	FF0	SDP	MSG	C/D	I/O
7	6	5	4	3	2	1	0

Default >>>

0	0	0	0	X	X	X	X

Bits 7-4   FF3-FF0 (FIFO flags)

FF3	FF2	FF1	FF0	Bytes or Words in the SCSI FIFO
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

These four bits define the number of bytes or words that currently reside in the 53C720's SCSI synchronous data FIFO. These bits are not latched and they will change as data moves through the FIFO. Because the FIFO is only 9 bytes deep, values over 9 will not occur.

Bit 3   SDP0 (Latched SCSI parity)
This bit reflects the SCSI parity signal (SDP0/) corresponding to the data latched in the SCSI Input Data Latch register (SIDL). It changes when a new byte is latched into the least significant byte of the SIDL register. This bit is active high, i.e. it is set when the parity signal is active.

Bit 2   MSG (SCSI MSG/ signal)
Bit 1   C/D (SCSI C/D signal)
Bit 0   I/O (SCSI I/O signal)
These SCSI phase status bits are latched on the asserting edge of REQ/ when operating in either initiator or target mode. These bits are set when the corresponding signal is active. They are useful when operating in low level mode.

Register 0F (0C)   SCSI Status Two (SSTAT2)

Read Only

ILF1	ORF1	OLF1	RES	SPL1	RES	LDSC	SDP1
7	6	5	4	3	2	1	0

Default >>>

0	0	0	X	X	X	1	X

Bit 7   ILF1 (SIDL most significant byte full)
This bit is set when the most significant byte in the SCSI Input Data Latch register (SIDL) contains data. Data is transferred from the SCSI bus to the SCSI Input Data Latch register before being sent to the DMA FIFO and then to the host bus. The SIDL register contains SCSI data received asynchronously. Synchronous data received does not flow through this register.

Bit 6   ORF1 (SODR most significant byte full)
This bit is set when the most significant byte in the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) contains data. The SODR register is used by the SCSI logic as a second storage register when sending data synchronously. It is not accessible to the user. This bit can be used to determine how many bytes reside in the chip when an error occurs.

Bit 5   OLF1 (SODL most significant byte full)
This bit is set when the most significant byte in the SCSI Output Data Latch (SODL) contains data. The SODL register is the interface between the DMA logic and the SCSI bus. In synchronous mode, data is transferred from the host bus to the SODL register, and then to the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) before being sent to the SCSI bus. In asynchronous mode, data is transferred from the host bus to the SODL register, and then to the SCSI bus. The SODR buffer register is not used for asynchronous transfers. This bit can be used to determine how m any bytes reside in the chip when an error occurs.

Bit 4 Reserved
Bit 3 Latched SCSI parity for SD15-8
This active high bit reflects the SCSI odd parity signal corresponding to the data latched into the most significant byte in the SIDL register.

Bit 2 Reserved
Bit 1 LDSC (Last Disconnect)
Used in conjunction with the "Connected" bit in SCNTL1, this status bit allows the user to detect the case in which a target device disconnects, and then some SCSI device selects or reselects 53C720. If the CON bit is asserted and the LDSC bit is asserted, a disconnect has occurred.

Bit 0 SDP1 (SCSI SDP1 Signal)
This bit represents the active-high current state of the SCSI SDP1 parity signal. It is unlatched and may be changing as it is read.

Registers 10-13 (10-13) Data Structure Address (DSA)

Read/Write

Default >>> Unknown

This 32-bit register contains the base address used for all table indirect calculations.

During any Memory-to-Memory Move operation, the contents of this register are shadowed.

Register 14 (17)   Interrupt Status (ISTAT)

Read/Write

ABRT	RST	SIGP	SEM	CON	INTF	SIP	DIP
7	6	5	4	3	2	1	0

Default >>>

0	0	0	0	0	0	0	0

This is the only register that can be accessed by the host CPU while the 53C720 is executing SCRIPTS (without interfering in the operation of the 53C720). It may be used to poll for interrupts if interrupts are disabled. There may be stacked interrupts pending; read this register after clearing an interrupt to check for stacked interrupts.

Bit 7   ABRT (Abort operation)
Setting this bit aborts the current operation being executed by the 53C720. If this bit is set and an interrupt is received, reset this bit before reading the DSTAT register to prevent further aborted interrupts from being generated. The sequence to abort any operation is:

1) Set this bit

2) Wait for an interrupt

3) Read the ISTAT register

4) If the SCSI Interrupt Pending bit is set, then read the SIST0 or SIST1 register to determine the cause of the SCSI Interrupt and go back to Step 2

5) If the SCSI Interrupt Pending bit is clear, and the DMA Interrupt Pending bit is set, then write 00h value to this register

6) Read the DSTAT register to verify the aborted interrupt and to see if any other interrupting conditions have occurred.

Bit 6   RST (Software reset)
Setting this bit resets the 53C720. All registers are cleared to their respective default values and all SCSI signals are deasserted. Setting this bit does not cause the SCSI RST/ signal to be asserted. This bit is not self-clearing; it must be cleared to clear the reset condition (a hardware reset will also clear this bit). This reset will not clear the Enable Acknowledge (EA) bit, Function Code 1 bit, or the ID Mode bit.

Bit 5   SIGP (Signal process)
SIGP is a R/W bit that can be written at any time, and polled & reset via CTEST2. The SIGP bit can be used in various ways to pass a flag to or from a running SCRIPT.

The only SCRIPT instruction directly affected by the SIGP bit is Wait For Selection/Reselection. Setting this bit causes that opcode to jump to the alternate address immediately. The instructions at the alternate jump address should check the status of SIGP to determine the cause of the jump. The SIGP bit may be used at any time and is not restricted to the wait for selection/ reselection condition.

Bit 4   SEM (Semaphore)
This bit can be set by the SCRIPTS processor using a SCRIPTS register write instruction. The bit may also be set by an external processor while the 53C720 is executing a SCRIPT. This bit enables the 53C720 to notify an external processor of a predefined condition while SCRIPTS are running. The external processor may also notify the 53C720 of a predefined condition and the SCRIPTS processor may take action while SCRIPTS are executing.

Bit 3   CON (Connected)
This bit is automatically set anytime the 53C720 is connected to the SCSI bus as an initiator or as a target. It will be set after successfully completing arbitration or when the 53C720 has responded to a bus-initiated selection or reselection. It will also be set after successfully completing arbitration when operating in low level mode. When this bit is clear, the 53C720 is not connected to the SCSI bus.

Bit 2   INTF (Interrupt on the Fly)
This bit is asserted by an INTFLY instruction during SCRIPTS execution. SCRIPTS programs will not halt when the interrupt occurs. This bit can be used to notify a service routine, running on the main processor while the SCRIPT processor is still executing a SCRIPTS program. If this bit is set, when the ISTAT register is read it will automatically be cleared. *Note:* If the INTF bit is set but SIP or DIP is not set, do not attempt to read the other chip status registers.

Bit 1   SIP (SCSI interrupt pending)
This status bit is set when an interrupt condition is detected in the SCSI portion of the 53C720. The following conditions will cause a SCSI interrupt to occur:

- A phase mismatch (initiator mode) or ATN/ becomes active (target mode)
- An arbitration sequence complete
- A selection or reselection timeout occurs
- The 53C720 was selected
- The 53C720 was reselected
- A SCSI gross error occurs
- An unexpected disconnect occurs
- A SCSI reset occurs
- A parity error is detected
- A selection/reselection timeout occurs
- The handshake-to-handshake timer is expired
- The general purpose timer is expired

To determine exactly which condition(s) caused the interrupt, the SIST0 and SIST1 registers should be read.

Bit 0   DIP (DMA interrupt pending)
This status bit is set when an interrupt condition is detected in the DMA portion of the 53C720. The following conditions will cause a DMA interrupt to occur:

- A host parity error is detected
- A bus fault is detected
- An abort condition is detected
- A SCRIPTS instruction is executed in single-step mode
- A SCRIPTS interrupt instruction is executed
- The Watchdog Timer decrements to zero
- An illegal instruction is detected

To determine exactly which condition(s) caused the interrupt, the DSTAT register should be read.

Register 18 (1B)   Chip Test Zero (CTEST0)

Read/Write

CDIS	SC1	SC0	RES	DFP	EHP	TT1	RES
7	6	5	4	3	2	1	0

Default >>>

| 0 | 0 | 0 | X | 0 | 0 | 0 | X |

Bit 7   CDIS (Cache burst disable)
When this bit is set, the 53C720 will not request a cache-line burst. When this bit is clear, the chip will attempt cache-line bursts when all necessary conditions are met. *Note:* If the hardware does not support cache-line bursts, this bit should be set to maximize performance.

Bits 6-5   SC1-SC0 (Snoop control)
The values of these bits are asserted on the corresponding device pins during bus mastership if bit 0 of CTEST3 is clear. Otherwise, the SC1 pin will always be driven with the value of the SC1 bit, and the SC0 pin will reflect the state of the internal host cycle request signal.

Bit 4   Reserved
Bit 3   DFP (DMA FIFO parity)
This bit represents the parity bit of the DMA FIFO when reading data out of the DMA FIFO via programmed I/O. In order to transfer data to/from the DMA FIFO, perform a read or a write to the CTEST6 register. When loading data into the FIFO via programmed I/O, write this bit to the FIFO as the parity bit for each byte loaded. When writing data to the DMA FIFO, set this bit with the status of the parity bit to be written to the FIFO before writing the byte to the FIFO. For the details of performing a diagnostic test of the DMA FIFO, refer to the *53C720 Programmer's Guide*.

Bit 2   EHP (Even host parity)
Parity is generated for all slave mode register reads and master mode memory writes. This bit controls the parity sense.

Setting this bit causes the 53C720 to generate even parity when driving data on the host data bus. The 53C720 inverts the parity bit received from the SCSI bus to create even parity. In addition, the even parity received from the host bus is inverted to odd parity before the 53C720 checks parity and sends the data to the SCSI bus. Clearing this bit causes the 53C720 to maintain odd parity throughout the chip.

NCR 53C720

Bit 1 TT1 (Transfer type bit)

The inverted value of this bit is asserted on the TT1 pin during bus mastership (Bus Modes 2, 3 and 4 only). This bit is not used in Bus Mode 1.

Bit 0 Reserved

Register 19 (1A) Chip Test One (CTEST1)

Read Only

FMT3	FMT2	FMT1	FMT0	FFL3	FFL2	FFL1	FFL0
7	6	5	4	3	2	1	0

Default >>>

| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7-4 FMT3-0 (Byte Empty in DMA FIFO)

These bits identify the bottom bytes in the DMA FIFO that are empty. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane three is empty, then FMT3 will be set. Since the FMT flags indicate the status of bytes at the bottom of the FIFO, if all FMT bits are set, the DMA FIFO is empty.

Bits 3-0 FFL3-0 (Byte Full in DMA FIFO)

These status bits identify the top bytes in the DMA FIFO that are full. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane three is full then FFL3 will be set. Since the FFL flags indicate the status of bytes at the top of the FIFO, if all FFL bits are set, the DMA FIFO is full.

Register 1A (19)   Chip Test Two (CTEST2)

Read Only

DDIR	SIGP	RES	RES	DFP	TEOP	DREQ	DACK
7	6	5	4	3	2	1	0

Default >>>

0	0	X	X	0	0	0	1

Bit 7   DDIR   (Data Transfer Direction)
This status bit indicates which direction data is being transferred. When this bit is set, the data will be transferred from the SCSI bus to the host bus. When this bit is clear, the data will be transferred from the host bus to the SCSI bus.

Bit 6   SIGP (Signal process)
This bit is a copy of the SIGP bit in the ISTAT register (bit 5). The SIGP bit is used to signal a running SCRIPT. When this register is read, the SIGP bit in the ISTAT register is cleared.

Bit 5   Reserved
Bit 4   Reserved
Bit 3   DFP (DMA FIFO parity)
This bit represents the parity bit of the DMA FIFO when the CTEST6 register reads data out of the FIFO. Reading the CTEST6 register unloads one data byte from the bottom of the DMA FIFO. When the CTEST6 register is read the parity signal is latched into this bit location and the next byte falls down to the bottom of the FIFO.

Bit 2   TEOP (SCSI true end of process)
This bit indicates the status of the 53C720's internal TEOP signal. The TEOP signal acknowledges the completion of a transfer through the SCSI portion of the 53C720. When this bit is set, TEOP is active. When this bit is clear, TEOP is inactive.

Bit 1   DREQ (Data request status)
This bit indicates the status of the 53C720's internal Data Request signal (DREQ). When this bit is set, DREQ is active. When this bit is clear, DREQ is inactive.

Bit 0   DACK (Data acknowledge status)
This bit indicates the status of the 53C720's internal Data Acknowledge signal (DACK/). When this bit is set, DACK/ is inactive. When this bit is clear, DACK/ is active.

Register 1B (18)   Chip Test Three (CTEST3)

Read/Write

V3	V2	V1	V0	FLF	CLF	FM	SM
7	6	5	4	3	2	1	0

Default >>>

X	X	X	X	0	0	0	0

Bits 7-4   V3-V0 (Chip revision level)
These bits identify the chip revision level for software purposes. This data manual applies to devices with revision level 0.

Bit 3   FLF (Flush DMA FIFO)
When this bit is set, data residing in the DMA FIFO is transferred to or from memory, starting at the address in the DNAD register. The internal DMAWR signal, controlled by the CTEST5 register, determines the direction of the transfer. This bit is not self clearing; once the 53C720 has successfully transferred the data, this bit should be reset.

Bit 2   CLF (Clear DMA and SCSI FIFOs)
When this bit is set, all data pointers for the SCSI and DMA FIFOs are cleared. In addition to the SCSI and DMA FIFO pointers, the SIDL, SODL, and SODR least and most significant byte full bits in the SSTAT0 and SSTAT2 registers are cleared. Any data in either of the FIFOs is lost. This bit automatically resets after the 53C720 has successfully cleared the appropriate FIFO pointers and registers.

Bit 1   FM (Fetch pin mode)
When set, this bit causes the FETCH/ pin to deassert during indirect and table indirect read operations. FETCH/ will only be active during the opcode portion of an instruction fetch. This allows SCRIPTS to be stored in a PROM while data tables are stored in RAM.

If this bit is not set, FETCH/ will be asserted for all bus cycles during instruction fetches.

Bit 0   SM (Snoop pins mode)
When set, the two snoop pins change functions and become pure outputs that are always driven, except when in ZMODE.

NCR 53C720

Pin	Function
SC0	Becomes a copy of the internal bus request signal. Signal will assert prior to BR/ and will be negated during the TS/ of the last bus cycle.
SC1	Drives the value in the SC1 register bit.

When clear, the snoop pins are driven during host bus ownership with the values of the CTEST0 SC(1-0) bits.

Registers 1C-1F (1C-1F) Temporary Stack (TEMP)

Read/Write

Default >>> Unknown

This 32-bit register stores the instruction address pointer for a CALL or a RETURN instruction. The address pointer stored in this register is loaded into the DSP register. This address points to the next instruction to be executed. Do not write to TEMP while the 53C720 is executing SCSI SCRIPTS.

During any Memory-to-Memory Move operation, the contents of this register are shadowed.

Register 20 (23)   DMA FIFO (DFIFO)

Read/Write

RES 7	BO6 6	BO5 5	BO4 4	BO3 3	BO2 2	BO1 1	BO0 0

Default >>>

0	0	0	0	0	0	0	0

Bit 7   Reserved

Bits 6-0   BO6-BO0 (Byte offset counter)
These six bits indicate the amount of data transferred between the SCSI core and the DMA core. It may be used to determine the number of bytes in the DMA FIFO when a DMA error occurs. These bits are unstable while data is being transferred between the two cores; once the chip has stopped transferring data, these bits are stable.

The following steps will determine how many bytes are left in the DMA FIFO when an error occurs, regardless of the direction of the transfer:

1) Subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register

2) AND the result with 7Fh for a byte count between zero and 64

Register 21 (22)   Chip Test Four (CTEST4)

Read Only

MUX 7	ZMOD 6	ZSD 5	SRTM 4	EHPC 3	FBL2 2	FBL1 1	FBL0 0

Default >>>

0	0	0	0	0	0	0	0

Bit 7   MUX (Host bus multiplex mode)
When set, the MUX bit puts the 53C720 into host bus MUX mode. In this mode, the chip asserts a valid address for one BCLK (during which AS/TS is valid and the data bus is tristated), and then tristates the address bus and drives the data bus (if a write). This allows the address and data buses to be tied together. It should be written prior to acquiring bus mastership.

Bit 6   ZMOD (High impedance mode)
Setting this bit causes the 53C720 to place all output and bidirectional pins into a high-impedance state. In order to read data out of the 53C720, this bit must be cleared.

This bit is intended for board-level testing only. Setting this bit during system operation will likely result in a crash.

Bit 5   ZSD   (SCSI High Impedance Mode)
Setting this bit causes the 53C720 to place the SCSI data bus SD (15-0) and the parity lines SDP (1-0) in a high-impedance state.   In order to transfer data on the SCSI bus, this bit must be cleared.

Bit 4   SRTM   (Shadow Register Test Mode)
Asserting this bit allows the user to read the shadowed temporary stack (TEMP) and Data Structure Address (DSA) registers. These registers are shadowed because both are written over during a Memory to Memory move operation. The DSA and TEMP registers contain the base address used for table indirect calculations, and the instruction address pointer for a call or return instruction, respectively.

Bit 3   EHPC   (Enable Host Parity Check)
Asserting this bit enables parity checking during slave write and DMA read execution if enable parity generation in cleared (SCNTL0 bit 2). The system powers up with this bit disabled so that the 53C720 will function properly with systems that do not support parity.

NCR 53C720

Bits 2-0   FBL2-FBL0 (FIFO byte control)

FBL2	FBL1	FBL0	DMA FIFO Byte Lane	Pins
0	X	X	Disabled	n/a
1	0	0	0	D(7-0)
1	0	1	1	D(15-8)
1	1	0	2	D(23-16)
1	1	1	3	D(31-24)

These bits send the contents of the CTEST6 register to the appropriate byte lane of the 32-bit DMA FIFO. If the FBL2 bit is set, then FBL1 & FBL0 determine which of four byte lanes can be read or written. Each of the four bytes that make up the 32-bit DMA FIFO can be accessed by writing these bits to the proper value. For normal operation, FBL2 must equal zero (set it to this value before executing SCSI SCRIPTS).

Register 22 (21)   Chip Test Five (CTEST5)

Read/Write

ADCK 7	BBCK 6	RES 5	MASR 4	DDIR 3	RES 2	RES 1	RES 0

Default >>>

0	0	X	0	0	X	X	X

Bit 7   ADCK (Clock address incrementor)
Setting this bit increments the address pointer contained in the DNAD register. The DNAD register is incremented based on the DNAD contents and the current DBC value. This bit automatically clears itself after incrementing the DNAD register.

Bit 6   BBCK (Clock byte counter)
Setting this bit decrements the byte count contained in the DBC register. The DBC register supports only 24 bits. It is decremented based on the DBC contents and the current DNAD value. This bit automatically clears itself after decrementing the DBC register.

Bit 5   Reserved

Bit 4   MASR (Master control for set or reset pulses)
This bit controls the operation of bit 3. When this bit is set, bit 3 asserts the corresponding signals. When this bit is reset, bit 3 deasserts the corresponding signals. This bit and bit 3 should not be changed in the same write cycle.

Bit 3   DDIR (DMA direction)
Setting this bit either asserts or deasserts the internal DMA Write (DMAWR) direction signal depending on the current status of the MASR bit in this register. Asserting the DMAWR signal indicates that data will be transferred from the SCSI bus to the host bus. Deasserting the DMAWR signal transfers data from the host bus to the SCSI bus.

Bit 2   Reserved
Bit 1   Reserved
Bit 0   Reserved

Register 23 (20)   Chip Test Six (CTEST6)

Read/Write

7	6	5	4	3	2	1	0

Default >>>

0	0	0	0	0	0	0	0

Bits 7-0   DF7-DF0 (DMA FIFO)

Writing to this register writes data to the appropriate byte lane of the DMA FIFO as determined by the FBL bits in the CTEST4 register. Reading this register unloads data from the appropriate byte lane of the DMA FIFO as determined by the FBL bits in the CTEST4 register. Data written to the FIFO is loaded into the top of the FIFO. Data read out of the FIFO is taken from the bottom. When data is read from the DMA FIFO, the parity bit for that byte is latched and stored in the DMA FIFO parity bit in the CTEST2 register.

To prevent DMA data from being corrupted, this register should not be accessed before starting or restarting a SCRIPT.

Registers 24-26 (25-27) DMA Byte Counter (DBC)

Read/Write

Default >>> Unknown

This 24-bit register determines the number of bytes to be transferred in a Block Move instruction. While sending data to the SCSI bus, the counter is decremented as data is moved into the DMA FIFO from memory. While receiving data from the SCSI bus, the counter is decremented as data is written to memory from the 53C720. The DBC counter is decremented each time that the AS/ (TS/ in Bus Mode 2, ADS/ in Bus Modes 3 and 4) signal is pulsed by the 53C720. It is decremented by an amount equal to the number of bytes that were transferred.

The maximum number of bytes that can be transferred in any one Block Move command is 16,777,215 bytes. The maximum value that can be loaded into the DBC register is FFFFFFh. If the instruction is Block Move and a value of 000000h is loaded into the DBC register, an illegal instruction interrupt will occur if not a target mode command phase.

The DBC register is also used during table indirect I/O SCRIPTS to hold the offset value.

NCR 53C720

Register 27 (24)   DMA Command (DCMD)

Read/Write

7	6	5	4	3	2	1	0

Default >>>

  0   0   0   0   0   0   0   0

Bits 7-0   DMA Command

This 8-bit register determines the instruction for the 53C720 to execute. This register has a different format for each instruction. For a complete description, refer to the 53C720 instruction set in Chapter 6.

Registers 28-2B (28-2B) DMA Next Data Address (DNAD)

Read/Write

Default >>> all zeros

This 32-bit register contains the general purpose address pointer. At the start of some SCRIPT operations, its value is copied from the DSPS register. Its value may not be valid except in certain abort conditions.

Registers 2C-2F (2C-2F)
DMA SCRIPTS Pointer (DSP)

Read/Write

Default >>> all zeros

To execute SCSI SCRIPTS, the address of the first SCSI SCRIPT must be written to this register. In normal SCRIPT operation, once the starting address of the SCSI SCRIPTS is written to this register, the SCRIPTS are automatically fetched and executed until an interrupt condition occurs.

In single-step mode, there is a SCRIPTS step interrupt after each instruction is executed. The DSP register does not need to be written with the next address, but the Start DMA bit (bit 2, DCNTL register) must be set each time the step interrupt occurs to fetch and execute the next SCSI SCRIPT. When writing this register eight bits at a time, writing the upper eight bits begins execution of the SCSI SCRIPTS.

Registers 30-33(30-33)
DMA SCRIPTS Pointer Save (DSPS)

Read/Write

Default >>> Unknown

This register contains the second longword of a SCRIPTS instruction. It is overwritten each time a SCRIPTS instruction is fetched. When a SCRIPTS interrupt is fetched, this register holds the interrupt vector.

NCR 53C720

Registers 34-37 (34-37) Scratch Register A (SCRATCHA)

Read/Write

Default >>> Unknown

This is a general purpose user definable scratch pad register. Normal SCRIPTS operations will not destroy the contents of this register; only Register Read/Write and Memory Moves into the SCRATCH register will alter its contents.

Register 38 (3B)   DMA Mode (DMODE)

Read/Write

BL1	BL0	FC2	FC1	PD	FAM	UO	MAN
7	6	5	4	3	2	1	0

Default >>>

0	0	0	0	0	0	0	0

Bit 7-6		BL1-BL0 (Burst length)
BL1	**BL0**	**Burst Length**
0	0	2 - transfer burst
0	1	4- transfer burst
1	0	8- transfer burst
1	1	16 - transfer burst

These bits control the maximum number of bus cycles performed per bus ownership. The 53C720 asserts the Bus Request output when the DMA FIFO can accommodate a transfer of at least one burst size of data. Bus Request (Hold in Bus Modes 3 and 4) is also asserted during start-of-transfer and end-of-transfer cleanup and alignment, even though less than a full burst of transfers may be performed.

To perform cache line bursts, these bits must be set to 4, 8 or 16 transfers and cache bursting must be enabled (CTEST0).

The 53C720 inserts a "fairness delay" of approximately 5 to 8 CLKs between bus ownerships. This gives the CPU and other bus master devices the opportunity to access memory between bursts.

Bit 5-4   FC2-FC1 (Function code) (Bus Modes 1, 3 and 4), or TM2-TM1 (Transfer Modifier) (Bus Mode 2)

These bits are user defined. Their values are asserted onto the corresponding device pins during bus mastership. If bit 6 in DCNTL register is asserted, FC2/TM2 becomes a Preview of Address (PA/). This is an input signal only and is used to tell the 53C720 that the system is ready for the next address value and the byte enable signals. This signal should not be driven during a slave access. FC1/TM1 becomes a general purpose output that is always driven when DCNTL bit 6 is asserted.

Bit 3   PD (Program/data)

This bit affects the function of the FC0 (TM0, Bus Mode 2) pin. Setting this bit causes the 53C720 to drive the FC0 (TM0) signal low when fetching instructions from memory. The FC0 (TM0) signal is always driven high when moving data to or from memory and can only be driven low during instruction fetch cycles. This feature can be used to allow SCRIPTS and data to be stored in separate memory banks. When bit 6 in DCNTL register is asserted, FC0/TM0 is a data control signal that is an output signal indicating what type of bus cycle is preferred (This is the same function performed by the DC/ signal that is commonly found in Intel processors).

FC0/TM0 = 1 Data spaces is being accessed

FC0/TM0 = 0   Control space is present on the bus

Bit 2   FAM (Fixed address mode)

Setting this bit disables the address pointer (DNAD register) so that it will not increment after each data transfer. If this bit is clear, the pointer increments after each data transfer. This bit is used to transfer data to or from a fixed port address. The port width must be 32 bits. Setting this bit does not affect SCRIPTS opcode fetching instructions; only data transfer instructions are affected.

Bit 1   UO/TT0 (User programmable transfer type)

In all bus modes, UPSO-TT0/ is a general purpose output pin. The value in the register bit is asserted onto the UPSO-TT0/ pin while the 53C720 is a bus master.

Bit 0   MAN (Manual start mode)

Setting this bit disables the 53C720 from automatically fetching and executing SCSI SCRIPTS after the DSP register is written. When the Start DMA bit in the DCNTL register is cleared, the chip is running in normal mode. Once the Start DMA bit in the DCNTL register is set, the 53C720 automatically fetches and executes each instruction. Clearing this bit causes the 53C720 to automatically fetch and execute SCSI SCRIPTS after the DSP register is written.

Register 39 (3A)   DMA Interrupt Enable (DIEN)

Read/Write

RES 7	HPED 6	BF 5	ABRT 4	SSI 3	SIR 2	WTD 1	IID 0

Default >>>

X	0	0	0	0	0	0	0

Bit 7   Reserved

Bit 6   HPED (Host parity error detected during DMA read or Slave write execution)

Bit 5   BF (Bus fault)

Bit 4   ABRT (Aborted)

Bit 3   SSI (SCRIPT step interrupt)

Bit 2   SIR (SCRIPT interrupt instruction received)

Bit 1   WTD (Watchdog timeout detected)

Bit 0   IID (Illegal instruction detected)

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the DSTAT register. An interrupt is masked by clearing the appropriate mask bit. Masking an interrupt prevents IRQ/ from being asserted for the corresponding interrupt, but the status bit will still be set in the DSTAT register. Masking an interrupt will not prevent the ISTAT DIP from being set; all DMA interrupts are considered fatal. Setting a mask bit enables the assertion of IRQ/ for the corresponding interrupt.

A masked or non-fatal interrupt will not prevent unmasked or fatal interrupts from getting through; interrupt stacking does not begin until either the ISTAT SIP or DIP bit is set.

The 53C710 IRQ/ output is latched; once asserted, it will remain asserted until the interrupt is cleared by reading the appropriate status register. Masking an interrupt after the IRQ/ output is asserted will not cause IRQ/ to be deasserted.

NCR 53C720

Register 3A (39)   DMA Watchdog Timer (DWT)

Read/Write

7	6	5	4	3	2	1	0

Default >>>

| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The DMA watchdog timer register provides a timeout mechanism during data transfers between the 53C720 and memory. This register determines the amount of time that the 53C720 will wait for the assertion of the transfer acknowledge/ signal after starting a bus cycle. Write the timeout value to this register during initialization. Every time that the 53C720 transfers data to/from memory, the value stored in this register is loaded into the counter. Disable the timeout feature by writing 00h to this register.

The unit time base for this register is 16* BCLK input period. For example, at 50 MHz the time base for this register is 16 x 20 ns = 320 ns. If a timeout of 50 μs is desired, then this register should be loaded with a value of 9Dh.

The minimum timeout value that should be loaded into this register is 02h; the value 01h will not provide a reliable timeout period.

Register 3B (38)   DMA Control Register (DCNTL)

Read/Write

RES 7	BSM 6	EA 5	SSM 4	BW16 3	STD 2	FA 1	COM 0

Default >>>

| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7   Reserved

Bit 6   BSM   (Bus Mode)
Asserting this bit nges the meaning of the Function Code (Bus Mode 1) or Transfer Modifier (Bus Mode 2) pins. FC0 or TM0 remains unaffected and becomes a general purpose output. FC1 or TM1 becomes a general purpose output, and FC2 or TM2 becomes an input to allow PA/ (Preview of next address). For more information on these signal, see the DMODE register description.

Bit 5   EA (Enable ack)
Setting this bit will cause the STERM/ (TA/ in Bus Mode 2, ReadyIn/ in Bus Modes 3 and 4) pin to become bidirectional, i.e. the 53C720 will generate STERM/ during slave accesses. When this bit is clear, the 53C720 will monitor STERM/ to determine the end of a cycle. This bit takes effect during the cycle in which it is set; setting this bit must be the first I/O performed to the 53C720 if this feature is desired. This bit is not cleared with a software reset. Refer to the *Bidirectional STERM/-TA/* section in Chapter 3, for more information on how this bit operates.

Bit 4   SSM (Single-step mode)
Setting this bit causes the 53C720 to stop after executing each SCRIPT instruction, and generate a SCRIPT step interrupt. When this bit is clear the 53C720 will not stop after each instruction; instead it continues fetching and executing instructions until an interrupt condition occurs. For normal SCSI SCRIPTS operation, this bit should be clear. To restart the 53C720 after it generates a SCRIPT Step interrupt, the ISTAT and DSTAT registers should be read to clear the interrupt and then the START DMA bit in this register should be set.

Bit 3   BW16   (Host Bus Width Equal to 16)
When this bit is set, the 53C720 host interface will become 16 bits wide. *Note:* Data lines 31-16 must be tied to data lines 15-0.

Bit 2   STD (Start DMA operation)
The 53C720 fetches a SCSI SCRIPTS instruction from the address contained in the DSP register when this bit is set. This bit is required if the 53C720 is in one of the following modes:

1) *Manual start mode* – Bit 0 in the DMODE register is set

2) *Single-step mode* – Bit 4 in the DCNTL register is set

When the 53C720 is executing SCRIPTS in manual start mode, the Start DMA bit needs to be set to start instruction fetches, but does not need to be set again until an interrupt occurs. When the 53C720 is in single-step mode, the Start DMA bit needs to be set to restart execution of SCRIPTS after a single-step interrupt.

Bit 1   FA (Fast arbitration)
When this bit is set, the 53C720 will immediately become bus master after receiving a Bus Grant (HLDAI in Bus Modes 3 and 4), saving one clock cycle of arbitration time. When this bit is clear, the 53C720 will follow the normal arbitration sequence.

Bit 0   COM (53C700 compatibility)
When this bit is clear, the 53C720 will behave in a manner compatible with the 53C700; selection/reselection IDs will be stored in both the SSID and SFBR registers.

When this bit is set, the ID will be stored only in the SSID register, protecting the SFBR from being overwritten should a selection/reselection occur during a DMA register to register operations. The default condition of this bit (clear) causes the 53C720 to act the same as the 53C700, which does not support register to register operations.

Register 3C-3F (3C-3F) Adder Sum Output (ADDER)

Read Only

Default >>> Unknown

This register contains the output of the internal adder, and is used primarily for test purposes.

Register 40 (43)   SCSI Interrupt Enable (SIEN0)

Read/Write

M/A	CMP	SEL	RSL	SGE	UDC	RST	PAR
7	6	5	4	3	2	1	0

Default >>>

| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the SIST0 register. An interrupt is masked by clearing the appropriate mask bit. Masking an interrupt prevents IRQ/ from being asserted for the corresponding interrupt, but the status bit will still be set in the SIST0 register. Masking an interrupt will not prevent the ISTAT SIP bit from being set, except in the case of non-fatal interrupts (SEL, RSL, and CMP). Setting a mask bit un-masks the corresponding interrupt, enabling the assertion of IRQ/ for that interrupt.

A masked non-fatal interrupt will not prevent un-masked or fatal interrupts from getting through; interrupt stacking does not begin until either the ISTAT SIP or DIP is set.

The 53C720 IRQ/ output is latched; once asserted, it will remain asserted until the interrupt is cleared by reading the appropriate status register. Masking an interrupt after the IRQ/ output is asserted will not cause IRQ/ to be deasserted. In the case of non-fatal interrupts, masking an interrupt after it occurs will cause the ISTAT SIP bit to clear and allow pending interrupts to fall through (interrupt stacking will be disabled).

Bit 7   M/A   (SCSI Phase Mismatch - Initiator Mode SCSI ATN Condition - Target Mode)
In initiator mode, the SCSI phase asserted by the target

NCR 53C720

and sampled during REQ does not match the expected phase in the SOCL register. This expected phase is automatically written by the SCSI transfer SCRIPT.

In target mode, the initiator has asserted ATN/. See the Disable halt on parity error or ATN condition bit in the SCNTL1 register for more information on when this status is actually raised.

Bit 6   CMP   (Function Complete)
Full arbitration and selection sequence has completed.

Bit 5   SEL   (Selected)
The 53C720 has been selected by a SCSI target device. The Enable response to selection bit in the SCID register must be set for this to occur.

Bit 4   RSL   (Reselected)
The 53C720 has been reselected by a SCSI initiator device. The Enable response to reselection bit in the SCID register must be set for this to occur.

Bit 3   SGE   (SCSI Gross Error)
The following conditions are considered SCSI Gross Errors:

1) Data underflow: the SCSI FIFO was read when no data   was present.

2) Data overflow: the SCSI FIFO was written to while full.

3) Offset underflow: in target mode, an ACK pulse was received before the corresponding REQ was sent.

4) Offset overflow: in initiator mode, a REQ pulse was received which caused the maximum offset (Defined by the MO3-0 bits in the SXFER register) to be exceeded.

5) In initiator mode, a phase change occurred with an outstanding REQ/ACK offset.

6) Residual data in SCSI FIFO: a transfer other than synchronous data receive was started with data left in the SCSI synchronous receive FIFO.

Bit 2   UDC (Unexpected Disconnect)
This condition only occurs in initiator mode. It happens when the target to which the 53C720 is connected disconnects from the SCSI bus unexpectedly. See the SCSI Disconnect Unexpected bit in the SCNTL2 register for more information on expected versus unexpected

disconnects. Any disconnect in low level mode causes this condition.

Bit 1   RST   (SCSI Reset Condition)
The SCSI RST signal has been asserted by the 53C720 or any other SCSI device. Note that this condition is edge-triggered so that multiple interrupts cannot occur because of a single RST pulse.

Bit 0   PAR   (SCSI Parity Error)
The 53C720 detected a parity error while receiving or sending SCSI data. See the Disable Halt on Parity Error or ATN Condition bits in the SCNTL1 register for more information on when this condition will actually be raised.

Register 41 (42) SCSI Interrupt Enable One Register (SIEN1)

Read/Write

RES 7	RES 6	RES 5	RES 4	RES 3	STO 2	GEN 1	HTH 0

Default >>>

0	0	0	0	0	0	0	0

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the SIST0 register. An interrupt is masked by clearing the appropriate mask bit. Masking an interrupt prevents IRQ/ from being asserted for the corresponding interrupt, but the status bit will still be set in the SIST0 register. Masking an interrupt will not prevent the ISTAT SIP bit from being set. Setting a mask bit unmasks the corresponding interrupt, enabling the assertion of IRQ/ for that interrupt.

A masked non-fatal interrupt will not prevent unmasked or fatal interrupts from getting through; interrupt stacking does not begin until either the ISTAT DIP or SIP bit is set.

The 53C720 IRQ/ output is latched; once asserted, it will remain asserted until the interrupt is cleared by reading the appropriate status register. Masking an interrupt after the IRQ/ output is asserted will not cause IRQ/ to be deasserted. In the case of non-fatal interrupts, masking an interrupt after it occurs will cause the ISTAT SIP bit to clear and allow pending interrupts to fall through (interrupt stacking will be disabled).

Bits 7-3 Reserved

Bit 2 STO (Selection or Reselection Timeout)
The SCSI device which the 53C720 was attempting to select or reselect did not respond within the programmed timeout period. See the description of the STIME0 register bits 3-0 for more information on the timeout timer.

Bit 1 GEN (General Purpose Timer Expired)
The general purpose timer has expired. The time measured is the time between enabling and disabling of the timer. See the description of the STIME1 register, bits

3-0, for more information on the general purpose timer.

Bit 0 HTH (Handshake to Handshake timer Expired)
The handshake-to-handshake timer has expired. The time measured is the SCSI Request to Request (target) or Acknowledge to Acknowledge (initiator) period. See the description of the STIME0 register, bits 7-4, for more information on the handshake-to-handshake timer.

Register 42 (41)   SCSI Interrupt Status Zero (SIST0)

Read Only

M/A 7	CMP 6	SEL 5	RSL 4	SGE 3	UDC 2	RST 1	PAR 0

Default >>>

0	0	0	0	0	0	0	0

Reading the SIST0 register returns the status of the various interrupt conditions, whether they are enabled in the SIEN0 register or not. Each bit asserted indicates that the corresponding condition has occurred. Reading a bit in SIST0 will reset the selected conditions.

Reading this register will clear any bits that are not set at the time the register is read, but will not necessarily clear the register because additional interrupts may be pending (the 53C720 stacks interrupts). SCSI interrupt conditions may be individually masked through the SIEN0 register.

When performing consecutive 8-bit reads of the DSTAT, SIST0, and SIST1 registers (in any order), insert a delay equivalent to 12 BCLK periods between the reads to ensure the interrupts clear properly. Also, if reading the registers when both the ISTAT SIP and DIP bits may not be set, the SIST0 and SIST1 registers should be read before the DSTAT register to avoid missing a SCSI interrupt.

Bit 7 M/A (Initiator Mode: Phase Mismatch; Target Mode: ATN/ Active)

In initiator mode, this bit is set if the SCSI phase asserted by the target does not match the instruction. The phase is sampled when REQ/ is asserted by the target. In target mode, this bit is set when the ATN/ signal is asserted by the initiator. This status bit is used in diagnostics testing or in low level mode.

Bit 6 CMP (Function Complete)
This bit is set when an arbitration only or full arbitration sequence has completed.

Bit 5 SEL (Selected)
This bit is set when the 53C720 is selected by another SCSI device. The enable response to selection bit must have been set in the SCID register for the 53C720 to respond to selection attempts.

Bit 4 RSL (Reselected)
This bit is set when the 53C720 is reselected by another SCSI device. The Enable Response to Reselection bit must have been set in the SCID register for the 53C720 to respond to reselection attempts.

Bit 3 SGE (SCSI Gross Error)
This bit is set when the 53C720 encounters a SCSI Gross Error Condition. The following conditions can result in a SCSI Gross Error Condition:

1) Data Underflow - the SCSI FIFO register was read when no data was present.

2) Data Overflow - too many bytes were written to the SCSI FIFO or the synchronous offset caused the SCSI FIFO to be overwritten.

3) Offset Underflow - the 53C720 is operating in target mode and an ACK/ pulse is received when the outstanding offset is zero.

4) Offset Overflow - the other SCSI device sent a REQ/ or ACK/ pulse with data which exceeded the maximum synchronous offset defined by the SXFER register.

5) Residual data in the Synchronous data FIFO - a transfer other than synchronous data receive was started with data left in the synchronous data FIFO.

6) A phase change occurred with an outstanding synchronous offset when the 53C720 was operating as an initiator.

Bit 2 UDC (Unexpected Disconnect)
This bit is set when the 53C720 is operating in initiator mode and the target device unexpectedly disconnects from the SCSI bus. This bit is only valid when the 53C720 operates in the initiator mode. When the 53C720 operates in low level mode, any disconnect will cause an interrupt, even a valid SCSI disconnect.

This bit will also be set if a selection timeout occurs (it may occur before, at the same time, or stacked after the STO interrupt).

Bit 1 RST (SCSI RST/ Received)
This bit is set when the 53C720 detects an active RST/ signal, whether the reset was generated external to the chip or caused by the Assert RST/ bit in the SCNTL1 register. This 53C720 SCSI reset detection logic is edge-

sensitive so that multiple interrupts will not be generated for a single assertion of the SCSI RST/ signal.

Bit 0 PAR (Parity Error)
This bit is set when the 53C720 detects a parity error when receiving or sending SCSI data. The Enable Parity Checking bit (bit 3 in the SCNTL0 register) must be set for this bit to become active. A parity error can occur w hen receiving data from the SCSI bus or when receiving data from the host bus. From the host bus, parity is checked as it is transferred from the DMA FIFO to the SODL register. A parity error can occur from the host bus only if Pass Through parity is enabled (bit 3 in the SCNTL0 register = 1, bit 2 in the SCNTL0 register = 0).

Register 43 (40) SCSI Interrupt Status One Register (SIST1)

Read Only

RES 7	RES 6	RES 5	RES 4	RES 3	STO 2	GEN 1	HTH 0

Default >>>

0	0	0	0	0	0	0	0

Reading the SIST1 register returns the status of the various interrupt conditions, whether they are enabled in the SIEN1 register or not. Each bit that is asserted indicates that the corresponding condition has occurred.

Reading a bit in SIST1 will reset the selected conditions.

Bits 7-3 Reserved
Bit 2 STO (Selection or Reselection Timeout)
The SCSI device which the 53C720 was attempting to select or reselect did not respond within the programmed timeout period. See the description of the STIME0 register, bits 3-0, for more information on the timeout timer.

Bit 1 GEN (General Purpose Timer Expired)
The general purpose timer has expired. The time measured is the time between enabling and disabling of the timer. See the description of the STIME1 register, bits 3-0, for more information on the general purpose timer.

Bit 0 HTH (Handshake to Handshake timer Expired)
The handshake-to-handshake timer has expired. The time measured is the SCSI Request to Request (target) or Acknowledge to Acknowledge (initiator) period. See the description of the STIME0 register, bits 7-4, for more information on the handshake-to-handshake timer.

NCR 53C720

Register 44 (47)   SCSI Longitudinal Parity (SLPAR)

Read/Write

Default >>> all zeros

This register performs a bytewise longitudinal parity check on all SCSI data received or sent through the SCSI core. If one of the bytes received or sent (usually the last) is the set of correct even parity bits, SLPAR should go to zero (assuming it started at zero). As an example, suppose that the following three data bytes and one check byte are received from the SCSI bus (all signals are shown active high):

Data Bytes	Running SLPAR
---	00000000
1. 11001100	11001100 (XOR of word 1)
2. 01010101	10011001 (XOR of word 1 and 2)
3. 00001111	10010110 (XOR of word 1, 2 and 3)
Even Parity >>>10010110	
4. 10010110 00000000	

A one in any bit position of the final SLPAR value would indicate a transmission error.

The SLPAR register can also be used to generate the check bytes for SCSI send operations. If the SLPAR register contains all zeros prior to sending a block move, it will contain the appropriate check byte at the end of the block move. This byte must then be sent across the SCSI bus.

Writing any value to this register resets it to zero.

The longitudinal parity checks are meant to provide an added measure of SCSI data integrity and are entirely optional. This register does not latch SCSI selection/reselection IDs under any circumstances.

Register 45 (46)   SCSI Wide Residue Data (SWIDE)

Read Only

Default >>> Unknown

After a wide SCSI data receive operation, this register will contain a residual data byte if the last byte received was never sent across the DMA bus. It represents either the first data byte of a subsequent data transfer, or it is a residue byte which should be cleared when an Ignore Wide Residue message is received. It may also be an overrun data byte.

Register 48 (4A) SCSI Timer Register 0 (STIME0)

Read /Write

HTH3	HTH2	HTH1	HTH0	SEL3	SEL2	SEL1	SEL0
7	6	5	4	3	2	1	0

Default >>>

0	0	0	0	0	0	0	0

Bits 7-4 HTH (Handshake -to-Handshake Timer Period)

These bits select Handshake-to-Handshake Timeout Period, the maximum time between SCSI handshakes (REQ to REQ in target mode, or ACK to ACK in initiator mode). When this timing is exceeded, the HTH bit in the SIST1 register is set, and an interrupt is optionally generated, if bit 0 in the SIEN1 register is set. The following table applies to the Handshake-to-Handshake Timer, the Selection/Reselection Timer (bits 3-0), and the General Purpose Timer (STIME1 bits 3-0).

HTH 7-4, SEL 3-0, GEN 3-0	Minimum Timeout
0000	Disabled
0001	100 μs
0010	200 μs
0011	400 μs
0100	800 μs
0101	1.6 ms
0110	3.2 ms
0111	6.4 ms
1000	12.8 ms
1001	25.6 ms
1010	51.2 ms
1011	102.4 ms
1100	204.8 ms
1101	409.6 ms
1110	819.2 ms
1111	1.6+ sec

Bits 3-0 SEL (Selection Timeout Period)

These bits select the SCSI selection/reselection timeout period. When this timing (plus the 200 μs selection abort time) is exceeded, the STO bit in the SIST1 register is set. An interrupt is optionally generated, if bit 2 in the SIEN1 register is set.

NCR 53C720

Register 49 (4B)   SCSI Timer Register One (STIME1)

Read/Write

RES 7	RES 6	RES 5	RES 4	GEN3 3	GEN2 2	GEN1 1	GEN0 0

Default >>>

X	X	X	X	0	0	0	0

Bits 7-4   Reserved

Bits 3-0   GEN3-0   (General Purpose Timer Period)
These bits select the period of the general purpose timer. The time measured is the time between enabling and disabling of the timer. When this timing is exceeded, the GEN bit in the SIST1 register is set and an interrupt is optionally generated, if bit 1 in the SIEN1 register is set. Refer to the table under STIME0, bits 3-0, for the available timeout periods.

Register 4C (4F)   SCSI Test Register Zero (STEST0)

Read Only

RES 7	RES 6	RES 5	RES 4	SLT 3	ART 2	SOZ 1	SOM 0

Default >>>

X	X	X	X	0	X	1	1

Bits 7-4   Reserved

Bit 3   SLT   (Selection Response Logic Test)
This bit is asserted when the 53C720 is ready to be selected or reselected. This does not take into account the bus settle delay of 400 ns. This bit is used for functional test and fault purposes.

Bit 2   ART   (Arbitration Priority Encoder Test)
This bit will always be asserted when the 53C720 exhibits the highest priority ID asserted on the SCSI bus during arbitration. It is primarily used for chip level testing, but it may be used during low level mode operation to determine if the 53C720 has won arbitration.

Bit 1   SOZ   (SCSI Synchronous Offset Zero)
This bit indicates that the current synchronous SCSI REQ/ACK offset is zero. This bit is not latched and may change at any time. It is used in low level synchronous SCSI operations. When this bit is set, the 53C720, as an initiator, is waiting for the target to request data transfers. If the 53C720 is a target then the initiator has sent the offset number of acknowledges.

Bit 0   SOM   (SCSI Synchronous Offset Maximum)
This bit indicates that the current synchronous SCSI REQ/ACK offset is the maximum specified by bits 3-0 in the SCSI Transfer register. This bit is not latched and may change at any time. It is used in low level synchronous SCSI operations. When this bit is set the 53C720, as a target, is waiting for the initiator to acknowledge the data transfers. If the 53C720 is an initiator then the target has sent the offset number of requests.

Register 4D (4E) SCSI Test Register One (STEST1)

Read Only

RES 7	RES 6	RES 5	RES 4	RES 3	RES 2	SFP1 1	SFP0 0

Default >>>

X	X	X	X	X	X	X	X

Bits 7-2   Reserved
Bits 1-0   SFP1-0   (SCSI FIFO Parity)
These bits represent the parity that is read from the SCSI FIFO byte lanes during test access through the SODL register. For reading the SCSI FIFO in test mode, these bits may be read after reading the SODL registers. SFP1 represents parity for the most significant byte and SFP0 represents parity for the least significant byte. See the description of the SCSI FIFO Test Mode bit in the STEST3 register for more information on testing the SCSI FIFO.

Register 4E (4D) SCSI Test Register Two (STEST2)

Read/Write

SCE 7	ROF 6	DIF 5	SLB 4	SZM 3	AWS 2	EXT 1	LOW 0

Default >>>

0	0	0	0	0	0	0	0

Bit 7   SCE   (SCSI Control Enable)
This bit, when set, allows all SCSI control and data lines to be asserted through the SOCL and SODL registers regardless of whether the 53C720 is configured as a target or initiator. *Note: This bit should not be set during normal operation, since it could cause contention on the SCSI bus. It is included for diagnostic purposes only.*

Bit 6   ROF   (Reset SCSI Offset)
Setting this bit clears any outstanding synchronous SCSI REQ/ACK offset. This bit should be set if a SCSI gross error condition occurs, to clear the offset when a synchronous transfer does not complete successfully. The bit automatically clears itself after resetting the synchronous offset.

Bit 5   DIF   (SCSI Differential Mode)
Setting this bit allows the 53C720 to interface properly to external differential transceivers. Its only real effect is to tristate the BSY/, SEL/, and RST/ pads so that they can be used as pure inputs. Resetting this bit enables single ended mode operation. This bit should be set in the initialization routine if the differential pair interface is to be used.

Bit 4   SLB   (SCSI Loopback Mode)
Setting this bit allows the 53C720 to perform SCSI loopback diagnostics. That is, it enables the SCSI core to simultaneously perform as both initiator and target. For more information on loopback mode, refer to the 53C720 Programmer's Guide.

NCR 53C720

Bit 3 SZM (SCSI High-Impedance Mode)
Setting this bit places all the open-drain 48 mA SCSI drivers into a high-impedance state. This is to allow internal loopback mode operation without affecting the SCSI bus.

Bit 2 AWS (Always Wide SCSI)
When this bit is set, all SCSI information transfers will be done in 16-bit wide mode. This includes data, message, command, status and reserved phases. This bit should normally be deasserted since 16-bit wide message, instruction, and status phases are not supported by the SCSI specifications. This bit is not guaranteed to function properly with future SCSI specifications.

Bit 1 EXT (Extend REQ/ACK Filtering)
The SCSI core contains a special digital filter on the REQ/ and ACK/ pins which will cause glitches on deasserting edges to be disregarded. Asserting this bit will provide additional filtering on the deasserting edge of the REQ/ and ACK/ signals. *Note:* This bit must never be set during fast SCSI (> 5M transfers per second) operations, because a valid assertion could be treated as a glitch.

Bit 0 LOW (SCSI Low level Mode)
Setting this bit places the 53C720 in low level mode. In this mode, no DMA operations can occur, and no SCRIPT instructions can be executed. Arbitration and selection may be performed by setting the start sequence bit as described in the SCNTL0 register. SCSI bus transfers are performed by manually asserting and polling SCSI signals. Clearing this bit allows instructions to be executed in SCSI SCRIPTS mode. *Note:* It is not necessary to set this bit for access to the SCSI bit-level registers (SODL, SBCL, and input registers)

Register 4F (4C)   SCSI Test Register Three (STEST3)

Read/Write

RES 7	RES 6	HSC 5	DSI 4	S16 3	TTM 2	CSF 1	FTM 0

Default >>>

X	X	0	0	0	0	0	0

Bits 7-6 Reserved
Bit 5 HSC (Halt SCSI Clock)
Asserting this bit causes the internal divided SCSI clock to come to a stop in a glitchless manner. This bit may be used for test purposes or to lower I_{DD} during a power down mode.

Bit 4 DSI (Disable Single Initiator Response)
If this bit is set, the 53C720 will ignore all bus-initiated selection attempts which employ the single-initiator option from SCSI-1. In order to select the 53C720 while this bit is set, the 53C720's SCSI ID and the initiator's SCSI ID must both be asserted. This bit should be asserted in SCSI-2 systems so that a single bit error on the SCSI bus will not be interpreted as a single initiator response.

Bit 3 S16 (16-bit System)
If this bit is set, all devices in the SCSI system implementation are assumed to be 16 bits. This causes the 53C720 to always check the parity bit for SCSI IDs 15-8 during bus-initiated selection or reselection, assuming parity checking has been enabled. If an 8-bit SCSI device attempts to select the 53C720 while this bit is set, the 53C720 will ignore the selection attempt, because the parity bit for IDs 15-8 will be undriven. See the description of the Enable Parity checking bit in the SCNTL0 register for more information.

Bit 2 TTM (Timer Test Mode)
Asserting this bit facilitates testing of the selection timeout, general purpose, and handshake-to-handshake timers by greatly reducing all three timeout periods. Setting this bit starts all three timers and if the respective bits in the SIEN1 register are asserted, the 53C720 will generate interrupts at timeout.

Bit 1 CSF (Clear SCSI FIFO)
Setting this bit will cause the "full flags" for the SCSI FIFO to be cleared. This empties the FIFO. This bit is self-resetting.

Bit 0 FTM (SCSI FIFO Test Mode)
Setting this bit places the SCSI core into a test mode in which the FIFO can be easily read and written. While this bit is set, writes to the least significant byte of the SODL register will cause the entire word contained in this register to be loaded into the FIFO. Reading the least significant byte of the SODL register will cause the FIFO to unload. These functions are summarized in the table below:

Register Name	Register Operation	FIFO Bits	FIFO Function
SODL	Read	15-0	Unload
SODL	Write	15-0	Load
SODL0	Read	7-0	Unload
SODL1	Read	15-8	None
SODL0	Write	7-0	Load
SODL1	Write	15-8	None

Registers 50-51 (52-53) SCSI Input Data Latch (SIDL)

Read Only

Default >>> Unknown

This register is used primarily for diagnostic testing, programmed I/O operation or error recovery. Data received from the SCSI bus can be read from this register. Data can be written to the SODL register and then read back into the 53C720 by reading this register to allow loopback testing. When receiving SCSI data, the data will flow into this register and out to the host FIFO. This register differs from the SBDL register; SIDL contains latched data and the SBDL always contains exactly what is currently on the SCSI data bus. Reading this register causes the SCSI parity bit to be checked, and will cause a parity error interrupt if the data is not valid.

Registers 54-55 (56-57)   SCSI Output Data Latch (SODL)

Read/Write

Default >>> Unknown

This register is used primarily for diagnostic testing or programmed I/O operation. Data written to this register is asserted onto the SCSI data bus by setting the Assert Data Bus bit in the SCNTL1 register. This register is used to send data via programmed I/O. Data flows through this register when sending data in any mode. It is also used to write to the synchronous data FIFO when testing the chip.

Registers 58-59 (5A-5B)   SCSI Bus Data Lines (SBDL)

Read Only

Default >>> Unknown

This register contains the SCSI data bus status. Even though the SCSI data bus is active low, these bits are active high. The signal status is not latched and is a true representation of exactly what is on the data bus at the time the register is read. This register is used when receiving data via programmed I/O. This register can also be used for diagnostic testing or in low level mode.

Registers 5C-5F   Scratch Register B
(SCRATCHB)

Read/Write

Default >>> Unknown

This is a general purpose user definable scratch pad
register. Apart from CPU access, only Register Read/
Write and Memory Moves directed at the SCRATCH
register will alter its contents.

Chapter 6

Instruction Set of the I/O Processor

SCSI SCRIPTS

After power up and initialization of the 53C720, the chip may be operated in one of two modes:

1) Low level register interface; or

2) SCSI SCRIPTS mode.

In the low level register interface, the user has access to the DMA control logic and the SCSI bus control logic. The chip may be operated much like an NCR 53C80. An external processor has access to the SCSI bus signals and the low level DMA signals, which allows creation of complicated board level test algorithms. The low level interface is useful for backward compatibility with SCSI devices that require certain unique timings or bus sequences to operate properly. Another feature allowed at the low level is loopback testing. In loopback mode, the SCSI core can be directed to talk to the DMA core to test internal data paths all the way out to the chip's pins.

To operate in the SCSI SCRIPTS mode, the 53C720 requires only a SCRIPTS start address. All commands are fetched from local or external memory. The 53C720 fetches and executes its own instructions by becoming a bus master on the host bus and fetching two or three 32-bit words into its registers. Commands are fetched until an interrupt command is encountered, or until an unexpected event (such as a hardware error) causes an interrupt to the external processor.

Once an interrupt is generated, the 53C720 halts all operations until the interrupt is serviced. Then, the start address of the next SCRIPTS instruction may be written to the DMA SCRIPTS Pointer register to restart the automatic fetch and execution of instructions.

The SCSI SCRIPTS mode of execution allows the 53C720 to make decisions based on the status of the SCSI bus, which off-loads the microprocessor from servicing the numerous interrupts inherent in I/O operations.

Given the rich set of SCSI oriented features included in the command set, and the ability to re-enter the SCSI algorithm at any point, this high level interface is all that is required for both normal and exception conditions. Therefore, switching to low level mode for error recovery should never be required.

Four types of instructions are implemented in the 53C720:

• Block Move

• I/O or Read/Write

• Transfer Control

• Memory Move

Each instruction consists of two or three 32-bit words. The first 32-bit word is always loaded into the DCMD and DBC registers, the second into the DSPS register. The third word, only used by Memory Move instructions, is loaded into the TEMP register.

Block Move Instructions

Figure 6-1. Block Move Instruction Register

First 32-bit word of the Block Move instruction

DCMD Register — DBC Register

I/O
C/D
MSG/
Op Code
Table Indirect Addressing
Indirect Addressing (53C700 compatible)
0 - Instruction Type - Block Move
0 - Instruction Type - Block Move

24-bit Block Move byte counter

Second 32-bit word of the Block Move instruction

DSPS Register

32- bit Start Address of the data to be moved or table entry offset
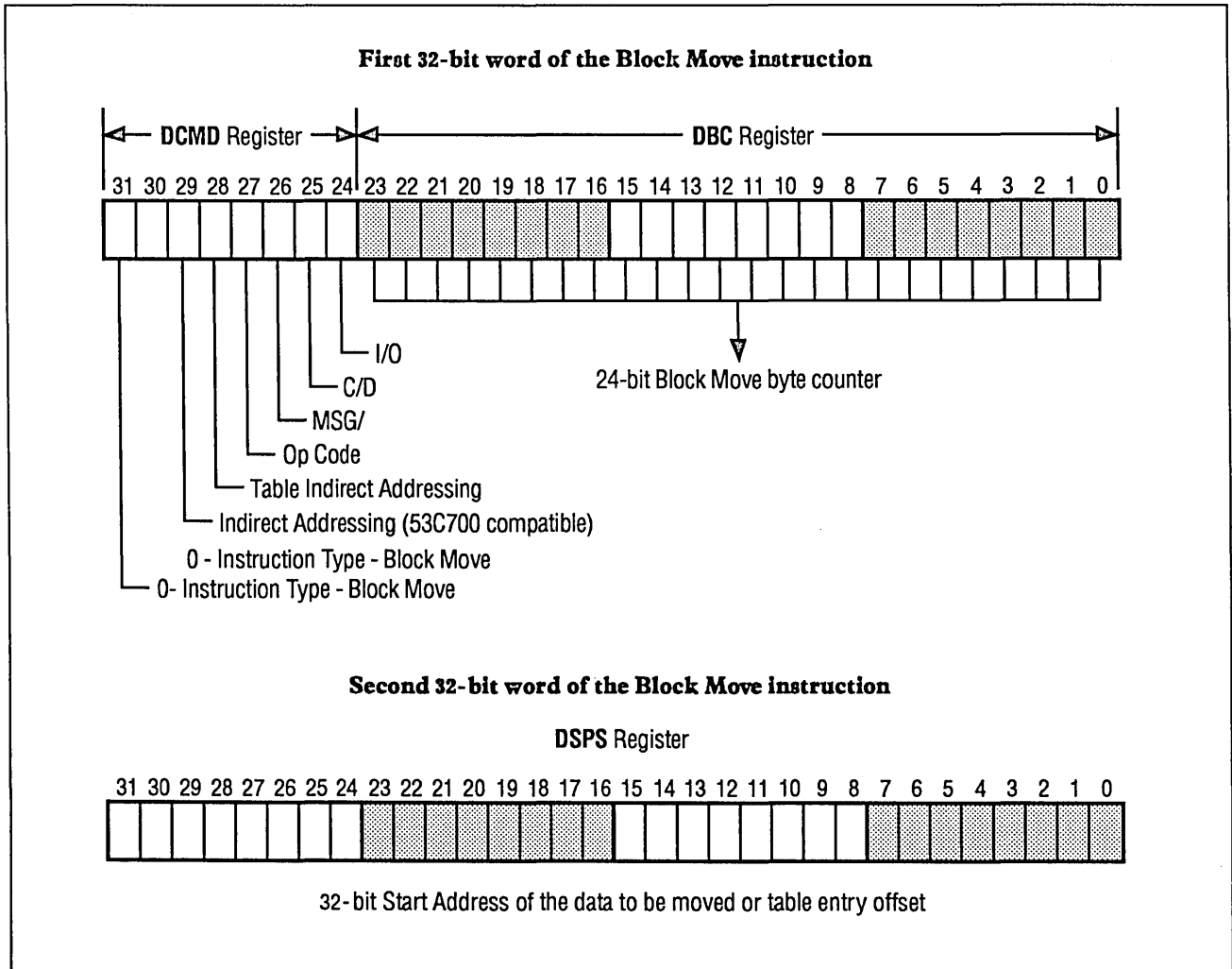
Bits 31-30   Instruction Type-Block Move

Bit 29   Indirect Addressing

When this bit is cleared, user data is moved to or from the 32-bit data start address for the Block Move instruction. The value is loaded into the chip's address register and incremented as data is transferred.

When set, the 32-bit user data start address for the Block Move is the address of a pointer to the actual data buffer address. The value at the 32-bit start address is loaded into the chip's DNAD register via a third long word fetch (4-byte transfer across the host computer bus).

Direct – The byte count and absolute address are as follows:

Command	Byte Count
Address of Data	

Indirect – Use the byte count and fetch the data address from the address in the command. The byte count is contained in the DBC register and the data address is fetched from the DSPS register.

Command	Byte Count
Address of Data	

Once the data buffer address is loaded, it is executed as if the chip operates in the direct mode. This indirect feature allows a table of data buffer addresses to be specified. Using the NCR SCSI SCRIPTS compiler, the table offset is placed in the script at compile time. Then at the actual data transfer time, the offsets are added to the base address of the data address table by the external processor. The logical I/O driver builds a structure of addresses for an I/O rather than treating each address individually. This feature makes it possible to locate SCSI SCRIPTS in a PROM.

Bit 28   Table Indirect

When this bit is set, the 24-bit signed value in the start address of the move is treated as a relative displacement from the value in the DSA register. Both the transfer count and the source/destination address are fetched from this address.

Table Indirect – Use the signed integer offset in bits 23-0 of the second 4 bytes of the instruction to fetch first the byte count and then the data address. The signed value is combined with the data structure base address to generate the physical address used to fetch values from the data structure. Sign-extended values of all ones for negative values are allowed, but ignored.

Command	Not Used
	Table Offset

Prior to the start of an I/O the Data Structure Base Address register (DSA) must be loaded with the base address of the I/O data structure. The address may be any long word on a long word boundary.

At the start of an I/O, the DSA is added to the 24-bit signed offset value from the opcode to generate the address of the required data; both positive and negative offsets are allowed. A subsequent fetch from the address brings the data values into the chip.

For a MOVE command, the 24-bit byte count is fetched from system memory. Then the 32-bit physical address is brought into the 53C720. Execution begins at this point.

SCRIPTS can directly execute operating system I/O data structures, saving time at the beginning of an I/O operation. The I/O data structure can begin on any longword boundary and can cross system segment boundaries.

There are two restrictions on the placement of data in system memory: the 8 bytes of data in the MOVE command must be contiguous, as shown below; and indirect data fetches are not available during execution of a Memory-to-Memory DMA operation.

(00)	Byte Count
Physical Data Address	

Bit 27 Opcode

This 1-bit field defines the instruction to be executed, either a block move (MOVE) or a chained block move (CHMOV). The Opcode Field bit has different meaning depending on whether the 53C720 is operating in initiator or target mode. If the Opcode bit is asserted (target mode) or deasserted (initiator mode) during a chained block move instruction, the corresponding bit in the SCNTL2 register (SCNTL bit 6) is asserted. The opcode bit and the SCNTL2 bit are cleared once a block move instruction is executed.

Target Mode

OPC	Instruction Defined
0	MOVE
1	CHMOV

1) The 53C720 verifies that it is connected to the SCSI bus as a target before executing this instruction.

2) The 53C720 asserts the SCSI phase signals (MSG/, C/D, & I/O) as defined by the Phase Field bits in the instruction.

3) If the instruction is for the command phase, the 53C720 receives the first command byte and decodes its SCSI Group Code.

   a) If the SCSI Group Code is either Group 0, Group 1, Group 2, or Group 5, then the 53C720 overwrites the DBC register with the length of the Command Descriptor Block: 6, 10, or 12 bytes.

   b) If any other Group Code is received, the DBC register is not modified and the 53C720 will request the number of bytes specified in the DBC register. If the DBC register contains 000000h an illegal instruction interrupt is generated.

4) The 53C720 transfers the number of bytes specified in the DBC register starting at the address specified in the DNAD register. If the opcode bit is set and a data transfer ends on an odd byte boundary, the 53C720 will store the last byte in the SCSI Wide Residue Data Register during a receive operation or in the SCSI Output Data Latch register during a send operation. This byte will be combined with the first byte from the subsequent transfer so that a wide transfer can be completed. See Figure 6-2.

5) If the SCSI ATN/ signal is asserted by the initiator or a parity error occurred during the transfer, the transfer can optionally be halted and an interrupt generated. The Disable Halt on Parity Error or ATN bit in the SCNTL1 register controls whether an interrupt will be generated.

Initiator Mode

OPC	Instruction Defined
0	CHMOV
1	MOVE

1) The 53C720 verifies that it is connected to the SCSI bus as an initiator before executing this instruction.

2) The 53C720 waits for an unserviced phase to occur. An unserviced phase is defined as any phase (with REQ/ asserted) for which the 53C720 has not yet transferred data by responding with an ACK/.

3) The 53C720 compares the SCSI phase bits in the DCMD register with the latched SCSI phase lines stored in the SSTAT1 register. These phase lines are latched when REQ/ is asserted.

4) If the SCSI phase bits match the value stored in the SSTAT1 register, the 53C720 will transfer the number of bytes specified in the DBC register starting at the address pointed to by the DNAD register. If the opcode bit is cleared and a data transfer ends on an odd byte boundary, the 53C720 will be store the last byte in the SCSI Wide Residue Data Register during a receive operation, or in the SCSI Output Data Latch Register during a send operation. This byte will be combined with the first byte from the subsequent transfer so that a wide transfer can be completed. See Figure 6-2.

5) If the SCSI phase bits do not match the value stored in the SSTAT1 register, the 53C720 generates a phase mismatch interrupt and the command is not executed.

Figure 6-2. Block Move and Chained Block Move Instructions

Host Memory | SCSI Bus

03	02	01	00	00
07	06	05	04	04
0B	0A	09	08	08
0F	0E	0D	0C	0C
13	12	11	10	10

SCSI Bus:

04	03
06	05
09	07
0B	0A
0D	0C

|◁—— 32 Bits ——▷| |◁— 16 Bits —▷|

Notes:

CHMOV 5, 3, when DATA_OUT: Move 5 bytes from address 03 in the host memory to the SCSI bus (bytes 03, 04, 05 and 06 are moved and byte 07 remains in the low order byte of the SCSI Output Data Latch register and is married with the first byte of the following MOVE instruction.

MOVE 5, 9, when DATA_OUT: Moves 5 bytes from address 09 in the host memory to the SCSI bus.

Bits 26-24   SCSI Phase

This 3-bit field defines the desired SCSI information transfer phase. When the 53C720 operates in initiator mode, these bits are compared with the latched SCSI phase bits in the SSTAT1 register. When the 53C720 operates in target mode, the 53C720 asserts the phase defined in this field. The following table describes the possible combinations and the corresponding SCSI phase.

MSG	C/D	I/O	SCSI Phase
0	0	0	Data out
0	0	1	Data in
0	1	0	Command
0	1	1	Status
1	0	0	Reserved out
1	0	1	Reserved in
1	1	0	Message out
1	1	1	Message in

Bits 23-0   Transfer Counter

A 24-bit field specifying the number of data bytes to be moved between the 53C720 and system memory. The field is stored in the DBC register. When the 53C720 transfers data to/from memory, the DBC register is decremented by the number of bytes transferred. In addition, the DNAD register is incremented by the number of bytes transferred. This process is repeated until the DBC register has been decremented to zero. At that time, the 53C720 fetches the next instruction.

Bits 31-0   Start Address

This 32-bit field specifies the starting address of the data to be moved to/from memory. This field is copied to the DNAD register. When the 53C720 transfers data to or from memory, the DNAD register is incremented by the number of bytes transferred.

NCR 53C720

I/O Instructions

Figure 6-3. I/O Instruction Register

First 32-bit word of the I/O instruction

RES
RES
RES
RES

Set/Clear ATN/
Set/Clear ACK/
Set/Clear Target Mode
Set/Clear/Carry
Encoded Destination ID 0
Encoded Destination ID 1
Encoded Destination ID 2
Encoded Destination ID 3
Reserved
Reserved
Reserved
Reserved
Select with ATN
Table Indirect Mode
Relative Address Mode
Op Code bit 0
Op Code bit 1
Op Code bit 2
1 - Instruction Type - I/O
0 - Instruction Type - I/O

Second 32-bit word of the I/O instruction

DSPS Register

32-bit Jump Address

Bits 31-30 Instruction Type - I/O Instruction

Bits 29-27 Opcode

The following Opcode Field bits have different meanings, depending on whether the 53C720 is operating in initiator or target mode. *Note: The following opcodes determine if the instruction is a Read/Write or an I/O instruction. Opcode selections 101-111 are considered Read/Write instructions, and are described in that section.*

Target Mode

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Reselect
0	0	1	Disconnect
0	1	0	Wait Select
0	1	1	Set
1	0	0	Clear

Reselect Instruction

1) The 53C720 arbitrates for the SCSI bus by asserting the SCSI ID stored in the SCID register. If the 53C720 loses arbitration, then it tries again during the next available arbitration cycle without reporting any lost arbitration status.

2) If the 53C720 wins arbitration, it attempts to reselect the SCSI device whose ID is defined in the destination ID field of the instruction. Once the 53C720 has won arbitration, it fetches the next instruction from the address pointed to by the DSP register.

3) If the 53C720 is selected or reselected before winning arbitration, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The 53C720 should manually be set to initiator mode if it is reselected, or to target mode if it is selected.

Disconnect Instruction

The 53C720 disconnects from the SCSI bus by deasserting all SCSI signal outputs. The SCSI direction control signals are deasserted, which disables the differential pair output drivers.

Wait Select Instruction

1) If the 53C720 is selected, it fetches the next instruction from the address pointed to by the DSP register.

2) If reselected, the 53C720 fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The 53C720 should manually be set to initiator mode when reselected.

3) If the CPU sets the SIGP bit in the ISTAT register, the 53C720 will abort the WAIT SELECT instruction and fetch the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register.

Set Instruction

When the ACK/ or ATN/ bits are set, the corresponding bits in the SOCL register are set. ACK/ or ATN/ should not be set except for testing purposes. When the target bit is set, the corresponding bit in the SCNTL0 register is also set. When the carry bit is set the corresponding bit in the ALU is set. Note: *None of the signals are set on the SCSI bus in target mode.*

Clear Instruction

When the ACK/ or ATN/ bits are set, the corresponding bits are cleared in the SOCL register. ACK/ or ATN/ should not be set except for testing purposes. When the target bit is cleared, the corresponding bit in the SCNTL0 register is cleared. When the carry bit is cleared, the corresponding bit in the ALU is cleared. *Note: None of the signals are reset on the SCSI bus in target mode.*

Initiator Mode

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Select
0	0	1	Wait Disconnect
0	1	0	Wait Reselect
0	1	1	Set
1	0	0	Clear

NCR 53C720

Select Instruction

1) The 53C720 arbitrates for the SCSI bus by asserting the SCSI ID stored in the SCID register. If the 53C720 loses arbitration, it tries again during the next available arbitration cycle without reporting any lost arbitration status.

2) If the 53C720 wins arbitration, it attempts to select the SCSI device whose ID is defined in the destination ID field of the instruction. It then fetches the next instruction from the address pointed to by the DSP register.

3) If the 53C720 is selected or reselected before winning arbitration, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The 53C720 should manually be set to initiator mode if it is reselected, or to target mode if it is selected.

4) If the Select with ATN/ field is set, the ATN/ signal is asserted during the selection phase.

Wait Disconnect Instruction

1) The 53C720 waits for the target to perform a "legal" disconnect from the SCSI bus. A "legal" disconnect occurs when BSY/ and SEL/ are inactive for a minimum of one Bus Free Delay (400 ns), after the 53C720 has received a Disconnect Message or a Command Complete Message.

Wait Reselect Instruction

1) If the 53C720 is selected before being reselected, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The 53C720 should be manually set to target mode when selected.

2) If the 53C720 is reselected, it fetches the next instruction from the address pointed to by the DSP register.

3) If the CPU sets the SIGP bit in the ISTAT register, the 53C720 will abort the Wait Reselect instruction and fetch the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register.

Set Instruction

When the ACK/ or ATN/ bits are set, the corresponding bits in the SOCL register are set. ACK/ or ATN/ should not be set except for testing purposes. When the target bit is set, the corresponding bit in the SCNTL0 register is also set. When the carry bit is set the corresponding bit in the Arithmetic Logic Unit (ALU) is set.

Clear Instruction

When the ACK/or ATN/ bits are set, the corresponding bits are cleared in the SOCL register. ACK/ or ATN/ should not be set except for testing purposes. When the target bit is cleared, the corresponding bit in the SCNTL0 register is cleared. When the carry bit is cleared, the corresponding bit in the ALU is cleared.

Bit 26   Relative Addressing Mode

When this bit is set, the 24-bit signed value in the DNAD register is used as a relative displacement from the current DSP address.

This bit should only be used in conjunction with the Select, Reselect, Wait Select, and Wait Reselect instructions. The Select and Reselect instructions can contain an absolute alternate jump address or a relative transfer address.

Bit 25   Table Indirect Mode

When this bit is set, the 24-bit signed value in the DBC register is used as an offset relative to the value in the Data Structure Base Address (DSA) register. The SCSI ID, synchronous offset and synchronous period are loaded from this address.

Prior to the start of an I/O, the DSA must be loaded with the base address of the I/O data structure. The address may be any longword on a longword boundary.

At the start of an I/O, the DSA is added to the 24-bit signed offset value from the opcode to generate the address of the required data; both positive and negative offsets are allowed. A subsequent fetch from the address brings the data values into the chip.

SCRIPTS can directly execute operating system I/O data structures, saving time at the beginning of an I/O operation. The I/O data structure can begin on any longword

boundary and can cross system segment boundaries.

There are two restrictions on the placement of data in system memory.

1) The I/O data structure must lie within the 8 MB above or below the base address.

2) An I/O command structure must have all four bytes contiguous in system memory, as shown below. The offset/period bits are ordered as in the SXFER register. The configuration bits are ordered as in the SCNTL3 register.

config	ID	offset/period	(00)

This bit should only be used in conjunction with the Select, Reselect, Wait Select, and Wait Reselect instructions. Bits 25 and 26 may be set individually or in combination:

	Bit 25	Bit 26
Direct	0	0
Table Indirect	0	1
Relative	1	0
Table Relative	1	1

Direct – Uses the device ID and physical address in the command.

Command	ID	Not Used	Not Used
Absolute Alternate Address			

Table Indirect – Uses the physical jump address, but fetches data using the table indirect method.

Command	Table Offset
Absolute Alternate Address	

Relative – Uses the device ID in the command, but treats the alternate address as a relative jump

Command	ID	Not Used	Not Used
Alternate Jump Offset			

Table Relative – Treats the alternate jump address as a relative jump and fetches the device ID, synchronous offset, and synchronous period indirectly. Adds the value in bits 23-0 of the first four bytes of the SCRIPT to the data structure base address to form the fetch address.

Command	Table Offset
Alternate Jump Offset	

Bit 24   Select with ATN/

This bit specifies whether ATN/ will be asserted during the selection phase when the 53C720 is executing a Select instruction. When operating in initiator mode, set this bit for the Select instruction. If this bit is set on any other I/O instruction, an illegal instruction interrupt is generated.

Bit 23-20   Reserved
Bits 19-16   Encoded SCSI Destination ID

This 8-bit field specifies the destination SCSI ID for an I/O instruction. Only one bit may be set in this field.

Bit 10   Set/Clear Carry

This bit is used in conjunction with a Set or Clear command to set or clear the Carry bit. Setting this bit with a Set command asserts the Carry bit in the ALU. Clearing this bit with a Set command deasserts the Carry bit in the ALU.

Bit 9   Set/Clear Target Mode

This bit is used in conjunction with a Set or Clear command to set or clear target mode. Setting this bit with a Set command configures the 53C720 as a target device (this sets bit 0 of the SCNTL0 register). Setting this bit with a Clear command configures the 53C720 as an initiator device (this clears bit 0 of the SCNTL0 register).

Bit 6   Set/Clear ACK/
Bit 3   Set/Clear ATN/

These two bits are used in conjunction with a Set or Clear command to assert or deassert the corresponding SCSI control signal. Bit 6 controls the SCSI ACK/ signal; bit 3 controls the SCSI ATN/ signal.

Setting either of these bits will set or reset the corresponding bit in the SOCL register, depending on the command used. The Set command is used to assert ACK/ and/or ATN/ on the SCSI bus. The Clear command is used to deassert ACK/ and/or ATN/ on the SCSI bus.

NCR 53C720

Since ACK/ and ATN/ are initiator signals, they will not be asserted on the SCSI bus unless the 53C720 is operating as an initiator or the SCSI Loopback Enable bit is set in the STEST2 register.

The Set/Clear SCSI ACK/ATN instruction would be used after message phase Block Move operations to give the initiator the opportunity to assert attention before acknowledging the last message byte. For example, if the initiator wishes to reject a message, an Assert SCSI ATN instruction would be issued before a Clear SCSI ACK instruction. After the target has serviced the request for a message-out phase, ATN is deasserted with a Clear SCSI ATN instruction.

Bits 31-0   Jump Address

This 32-bit field specifies the address of the instruction to fetch when the 53C720 encounters a jump condition. The 53C720 fetches instructions from the address pointed to by this field whenever the 53C720 encounters a SCSI condition that is different from the condition specified in the instruction.

For example, during the execution of a Select instruction in initiator mode, if the 53C720 is reselected, then the next instruction is fetched from the address pointed to by the jump address field. For a complete description of the different jump conditions, refer to the description of each instruction.

Read/Write Instructions

Figure 6-4. Read/Write Instruction Register

First 32-bit word of the Read/Write instruction

DCMD Register | DBC Register

31 30 29 28 27 26 25 24 | 23 22 21 20 19 18 17 16 | 15 14 13 12 11 10 9 8 | 7 6 5 4 3 2 1 0

Immediate Data

Reserved (must be 0)

A0
A1
A2 — Register Address
A3
A4
A5
A6
0 (Reserved)
Carry Enable
Operator 0
Operator 1
Op Code bit 0
Op Code bit 1
Op Code bit 2
1 - Instruction Type - R/W
0 - Instruction Type - R/W

Second 32-bit word of the Read/Write instruction

DSPS Register

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Not used, must be 0

NCR 53C720

Table 6-1. Read/Write Insturctions

Operator	Op Code 111 Read Modify Write	Op Code 110 Move to SFBR	Op Code 101 Move from SFBR
00	Immediate data to destination register	Immediate register to SFBR	Immediate SFBR to destination register
01	Immediate data OR'ed with destination register	Immediate data OR register to SFBR	Immediate data OR'ed with SFBR to destination register
10	Immediate data AND'ed with destination register	Immediate data AND register to SFBR	Immediate data AND'ed with SFBR to destination register
11	Immediate data added to destination register with or without carry	Immediate data added with register to SFBR with or without carry	Immediate data added with SFBR to destination register with or without carry

Bits 31-30   Instruction Type - Read/Write Instruction

Bits 29-27   Opcode

The combinatios of these bits determine if the instruction is a Read/Write or an I/O instruction. Opcodes 000 through 100 are considered I/O instructions.

Bits 26-25   Operator

These bits are used in conjunction with the opcode bits to determine which instruction is currently selected.

Bit 24   Carry Enable

When this bit is set it will allow the previous carry value to be used by the present add instruction. The carry value will remain intact unless it is modified by an add, set carry or clear carry instruction. All other instructions do not affect carry. If Carry Enable is not set, no carry in will be used during the present add instruction.

Bits 22-16   Register Address - A(6-0)

Register values may be changed from SCRIPTS in read-modify-write cycles or move to/from SFBR cycles. A(6-0) select an 8-bit source/destination register within the 53C720. Register addresses are always Little Endian addresses.

Read-Modify-Write Cycles

The register is read, the selected operation is performed, and the result is written back to the source register.

The Add operation can be used to increment or decrement register values (or memory values if used in conjunction with a Memory-to-Register Move operation) for use as loop counters.

Move to/from SFBR Cycles

All operations are read-modify-writes. However, two registers are involved, one of which is always the SFBR. The possible functions of this command are:

• Write one byte (value contained within the SCRIPTS instruction) into any chip register.

• Move to/from the SFBR from/to any other register.

• Alter the value of a register with AND/OR/ADD operators.

• After moving values to the SFBR, the compare and jump, call, or similar commands may be used to check the value.

• A Move-to-SFBR followed by a Move-from-SFBR can be used to perform a register to register move.

Using Read-Modify-Write operations on the ISTAT register may clear pending interrupts which have not yet been serviced.

Transfer Control Instructions

Figure 6-5. Transfer Control Instruction Register

First 32-bit word of the Transfer Control instruction

DCMD Register → ← DBC Register →

31 30 29 28 27 26 25 24 | 23 22 21 20 19 18 17 16 | 15 14 13 12 11 10 9 8 | 7 6 5 4 3 2 1 0

Mask for compare

Data to be compared
with the SCSI First
Byte Received

Wait for Valid Phase
Compare Phase
Compare Data
Jump if: True=1, False=0
Interrupt on the Fly
Carry Test
0 (Reserved)
Relative addressing mode
I/O
C/D
MSG
Op Code bit 0
Op Code bit 1
Op Code bit 2
0 - Instruction Type - Transfer Control
1- Instruction Type - Transfer Control

Second 32-bit word of the Transfer Control instruction

DSPS Register

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

32-bit Jump Address

Bits 31-30   Instruction Type - Transfer Control Instruction

Bits 29-27   Opcode

This 3-bit field specifies the type of transfer control instruction to be executed. All transfer control instructions can be conditional. They can be dependent on a true/false comparison of the ALU Carry bit or a comparison of the SCSI information transfer phase with the Phase field, and/or a comparison of the First Byte Received with the Data Compare field. Each instruction can operate in initiator or target mode.

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Jump
0	0	1	Call
0	1	0	Return
0	1	1	Interrupt
1	X	X	Reserved

Jump Instruction

1) The 53C720 can do a true/false comparison of the ALU carry bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare and True/False bit fields. If the comparisons are true, the 53C720 loads the DSP register with the contents of the DSPS register. The DSP register now contains the address of the next instruction.

2) If the comparisons are false the 53C720 fetches the next instruction from the address pointed to by the DSP register, leaving the instruction pointer unchanged.

Call Instruction

1) The 53C720 can do a true/false comparison of the ALU carry bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, the 53C720 loads the DSP register with the contents of the DSPS register and that address value becomes the address of the next instruction.

When the 53C720 executes a Call instruction, the instruction pointer contained in the DSP register is stored in the TEMP register.

When a Return instruction is executed, the value stored in the TEMP register is returned to the DSP register.

2) If the comparisons are false, the 53C720 fetches the next instruction from the address pointed to by the DSP register and the instruction pointer is not modified.

Return Instruction

1) The 53C720 can do a true/false comparison of the ALU bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, then the 53C720 loads the DSP register with the contents of the DSPS register. That address value becomes the address of the next instruction.

When the 53C720 executes a Call instruction, the current instruction pointer contained in the DSP register is stored in the TEMP register.

When a Return instruction is executed, the value stored in the TEMP register is returned to the DSP register.

The 53C720 does not check to see whether the Call instruction has already been executed. It will not generate an interrupt if a Return instruction is executed without previously executing a Call instruction.

2) If the comparisons are false, then the 53C720 fetches the next instruction from the address pointed to by the DSP register and the instruction pointer will not be modified.

Interrupt Instructions

Interrupt

a) The 53C720 can do a true/false comparison of the ALU bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, then the 53C720 generates an interrupt by asserting the IRQ/ signal.

b) The 32-bit address field stored in the DSPS register (not DNAD as in 53C700) can contain a unique interrupt service vector. When servicing the interrupt, this unique status code allows the ISR to quickly identify the point at which the interrupt occurred.

c) The 53C720 halts and the DSP register must be written to start any further operation.

Interrupt on-the-Fly

a) The 53C720 can do a true/false comparison of the ALU carry bit or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, the 53C720 will assert the Interrupt on the fly bit (ISTAT bit 2).

Bits 26-24   SCSI Phase

This 3-bit field corresponds to the three SCSI bus phase signals which are compared with the phase lines latched when REQ/ is asserted. Comparisons can be performed to determine the SCSI phase actually being driven on the SCSI bus. The following table describes the possible combinations and their corresponding SCSI phase. These bits are only valid when the 53C720 is operating in initiator mode; when the 53C720 is operating in the target mode, these bits should be cleared.

MSG	C/D	I/O	SCSI Phase
0	0	0	Data out
0	0	1	Data in
0	1	0	Command
0	1	1	Status
1	0	0	Reserved out
1	0	1	Reserved in
1	1	0	Message out
1	1	1	Message in

Bit 23   Relative Addressing Mode

When this bit is set, the 24-bit signed value in the DSPS register is used as a relative offset from the current DSP address (which is pointing to the next instruction, not the one currently executing). Relative mode does not apply to Return and Interrupt SCRIPTS.

Jump/Call an Absolute Address – Start execution at the new absolute address.

Command	Condition Codes
Absolute Alternate Address	

Jump/Call a Relative Address – Start execution at the current address plus (or minus) the relative offset.

Command	Condition Codes
	Alternate Jump Offset

The SCRIPTS program counter is a 32-bit value pointing to the SCRIPT currently being executed by the 53C720. The next address is formed by adding the 32-bit program counter to the 24-bit signed value of the last 24 bits of the Jump or Call instruction. Because it is signed (twos compliment), the jump can be forward or backward.

A relative transfer can be to any address within a 16-MB segment. The program counter is combined with the 24-bit signed offset (using addition or subtraction) to form the new execution address.

SCRIPTS programs may contain a mixture of direct jumps and relative jumps to provide maximum versatility when writing SCRIPTS. For example, major sections of code can be accessed with far calls using the 32-bit physical address, then local labels can be called using relative transfers. If a SCRIPT is written using only relative transfers it would not require any run time alteration of physical addresses, and could be stored in and executed from a PROM.

NCR 53C720

Bit 21 Carry Test

When this bit is set, decisions based on the ALU carry bit can be made. True/False comparisons are legal, but Data Compare and Phase Compare are illegal.

Bit 20 Interrupt on the Fly

When this bit is asserted, the interrupt instruction will not halt the SCRIPTS processor. Once the interrupt occurs, the Interrupt on the Fly bit (ISTAT bit 2) will be asserted.

Bit 19 Jump If True/False

This bit determines whether the 53C720 should branch when a comparison is true or when a comparison is false. This bit applies to both Phase Compares and Data Compares. If both the Phase Compare and Data Compare bits are set, then both compares must be true to branch on a true condition. Both compares must be false to branch on a false condition.

Bit 19	Compare	Action
0	False	Jump Taken
0	True	No Jump
1	False	No Jump
1	True	Jump Taken

Bit 18 Compare Data

When this bit is set, then the first byte received from the SCSI data bus (contained in SFBR register) is compared with the Data to be Compared Field in the Transfer Control instruction. The Wait for Valid Phase bit controls when this compare will occur. The Jump if True/False bit determines the condition (true or false) to branch on.

Bit 17 Compare Phase

When the 53C720 is in initiator mode, this bit controls phase compare operations. When this bit is set, the SCSI phase signals (latched by REQ/) are compared to the Phase Field in the Transfer Control instruction; if they match, then the comparison is true. The Wait for Valid Phase bit controls when the compare will occur.

When the 53C720 is operating in target mode this bit, when set, tests for an active SCSI ATN/ signal.

Bit 16 Wait For Valid Phase

If the Wait for Valid Phase bit is set, then the 53C720 waits for a previously unserviced phase before comparing the SCSI phase & data.

If the Wait for Valid Phase bit is clear, then the 53C720 compares the SCSI phase & data immediately.

Bits 15-8 Data Compare Mask

The Data Compare Mask allows a SCRIPT to test certain bits within a data byte. During the data compare, any mask bits that are set cause the corresponding bit in the SFBR data byte to be ignored.

For instance, a mask of 01111111b and data compare value of 1XXXXXXXb allows the SCRIPTS processor to determine whether or not the high order bit is on while ignoring the remaining bits.

Bits 7-0 Data Compare Value

This 8-bit field is the data to be compared against the SCSI First Byte Received (SFBR) register. These bits are used in conjunction with the Data Compare Mask Field to test for a particular data value.

Bits 31-0 Jump Address

This 32-bit field contains the address of the next instruction to fetch when a jump is taken. Once the 53C720 has fetched the instruction from the address pointed to by these 32 bits, this address is incremented by 4, loaded into the DSP register and becomes the current instruction pointer.

Memory Move Instructions

Figure 6-6. Memory Move Instruction Register

First 32-bit word of the Memory Move instruction

|← DCMD Register →|← DBC Register →|

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

— 0 (Reserved)
— 0 (Reserved)
— 0 (Reserved)
— 0 (Reserved)
— 0 (Reserved)
— 0 (Reserved)
— 1 - Instruction Type - Memory Move
— 1 - Instruction Type - Memory Move

24-bit Memory Move byte counter

Second 32-bit – source address of the Memory Move instruction

DSPS Register

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Third 32-bit word – destination address of the Memory Move instruction

TEMP Register

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

The Memory Move instruction is used to copy the specified number of bytes from the source address to the destination address.

Allowing the 53C720 to perform memory moves frees the system processor for other tasks and moves data at higher speeds than available from current DMA controllers. Up to 16 MB may be transferred with one instruction. There are two restrictions:

1) Both the source and destination addresses must start with the same address alignment (A(1-0) must be the same). If source and destination are not aligned, then an illegal instruction interrupt will occur.

2) Indirect addresses are not allowed.

A special block move instruction passes the source and destination addresses and the byte count to the 53C720. A burst of data is fetched from the source address, put into the DMA FIFO and then written out to the destination address. The move continues until the byte count decrements to zero, then another SCRIPT is fetched from system memory.

Upon completion of the move, an interrupt instruction or jump to a SCSI function should be executed.

The DSPS and DSA registers are additional holding registers used during the Memory Move.

Bits 29-24   Reserved
These bits are reserved and must be zero. If any of these bits is set, an illegal instruction interrupt will occur.

Bits 23-0   Transfer Count
The number of bytes to be transferred is stored in the lower 24 bits of the first instruction word.

Read/Write System Memory from a Script
By using the Memory Move instruction, single or multiple register values may be transferred to/from system memory.

Because the Chip Select (CS/) input is derived from an address decode, it could activate during a Memory Move operation if the source/destination address decodes to within the chip's register space. If this occurs, the register indicated by the lower 6 bits of the memory address is taken to be the data source or destination. In this way, register values can be saved to system memory and later restored, and SCRIPTS can make decisions based on data values in system memory.

The SFBR is not writable via the CPU, and therefore not by a Memory Move. However, it can be loaded via SCRIPTS Read/Write operations. To load the SFBR with a byte stored in system memory, the byte must first be moved to an intermediate 53C720 register (for example, from a SCRATCH register), and then to the SFBR.

The same address alignment restrictions apply to register access operations as to normal memory-to-memory transfers.

Chapter 7

Electrical Specifications

DC Characteristics

Absolute Maximum Stress Ratings

Parameter	Symbol	Min	Max	Unit
Storage temperature	T_{STG}	-55	150	°C
Supply voltage	V_{DD}	-0.5	7.0	V
Input voltage	V_{IN}	$V_{SS} - 0.5$	$V_{DD} + 0.5$	V
Electrostatic discharge	ESD*	-	4K	V

SCSI pins only. Test using the human body model, 100 pF at 1.5 K ohms

Stresses beyond those listed above may cause permanent
damage to the device. These are stress ratings only;
functional operation of the device at these or at any other
conditions beyond those indicated in the *Operating
Conditions* section of this specification is not implied.

Operating Conditions

Parameter	Symbol	Min	Max	Units
Supply voltage	V_{DD}	4.75	5.25	V
Supply current	I_{DD}	-	TBD	mA
Operating free-air	T_A	0	70	°C

SCSI Signals – SD(15-0)/, SDP0/, REQ/, MSG/, I/O, C/D, ATN/, ACK/, BSY/, SEL/, RST/, SDP1/

Parameter	Symbol	Min	Max	Unit	Conditions
Input high voltage	V_{IH}	2.0	$V_{DD} + 0.5$	V	-
Input low voltage	V_{IL}	$V_{SS} - 0.5$	0.8	V	-
Output low voltage	V_{OL}	V_{SS}	0.5	V	$I_{OL} = 48$ mA
Hysteresis	V_{HYS}	200	-	mV	-
Input leakage current	I_{IN}	-10	10	µA	-
Input leakage – SCSI RST		-200	50	µA	-
Tristate leakage current	I_{OZ}	-10	10	µA	-

NCR 53C720

Input Signals – BG-HLDAI/, BOFF/, RESET/, CS/, BS(2-0), BCLK-, SCLK, AUTO/, DIFFSENS

Parameter	Symbol	Min	Max	Units	Conditions
Input high voltage	V_{IH}	2.0	$V_{DD} + 0.5$	V	-
Input low voltage	V_{IL}	$V_{SS} - 0.5$	0.8	V	-
Input leakage current	I_{IN}	-1.0	1.0	µA	-

Input Signals – GPI (3-0)

Parameter	Symbol	Min	Max	Units	Conditions
Input high voltage	V_{IH}	2.0	$V_{DD} + 0.5$	V	-
Input low voltage	V_{IL}	$V_{SS} - 0.5$	0.8	V	-
Input leakage current	I_{IN}	-10	10	µA	$V_{IL} = V_{DD}$
Input high leakage current	I_{IL}	-200	-50	µA	$V_{IL} = 0\,V$

Output Signals – SDIR(15-0), SDIRP0, BSYDIR, SELDIR, RSTDIR, TGS, IGS, SDIRP1

Parameter	Symbol	Min	Max	Units	Conditions
Output high voltage	V_{OH}	2.4	V_{DD}	V	$I_{OH} = -4\,mA$
Output low voltage	V_{OL}	V_{SS}	0.4	V	$I_{OL} = 4\,mA$
Output high current	I_{OH}	-2.0	-	mA	$V_{OH} = V_{DD} - 0.5\,V$
Output low current	I_{OL}	4.0	-	mA	$V_{OL} = 0.4\,V$

Output Signals – FETCH/, IRQ/

Parameter	Symbol	Min	Max	Units	Conditions
Output high voltage	V_{OH}	2.4	V_{DD}	V	$I_{OH} = -8\,mA$
Output low voltage	V_{OL}	V_{SS}	0.4	V	$I_{OL} = 8\,mA$
Output high current	I_{OH}	-4.0	-	mA	$V_{OH} = V_{DD} - 0.5\,V$
Output low current	I_{OL}	8.0	-	mA	$V_{OL} = 0.4\,V$

Output Signals – READYO/-READYO/, MASTER/, GPO

Parameter	Symbol	Min	Max	Units	Conditions
Output high voltage	V_{OH}	2.4	V_{DD}	V	$I_{OH} = -16$ mA
Output low voltage	V_{OL}	V_{SS}	0.4	V	$I_{OL} = 16$ mA
Output high current	I_{OH}	-8.0	-	mA	$V_{OH} = V_{DD} - 0.5$ V
Output low current	I_{OL}	16.0	-	mA	$V_{OL} = 0.4$ V

Tristate Output Signals – A(31-7), FC(2-0)-TM(2-0), SC(1-0), UPSO-TT0/, CBREQ/-TT1/, BR/-HOLD/

Parameter	Symbol	Min	Max	Units	Conditions
Output high voltage	V_{OH}	2.4	V_{DD}	V	$I_{OH} = -16$ mA
Output low voltage	V_{OL}	V_{SS}	0.4	V	$I_{OL} = 16$ mA
Output high current	I_{OH}	-8.0	-	mA	$V_{OH} = V_{DD} - 0.5$ V
Output low current	I_{OL}	16.0	-	mA	$V_{OL} = 0.4$ V
Tristate leakage current	I_{OZ}	-10	10	μA	-

Bidirectional Signals – A(6-0), D(31-0), DP(3-0), DS/-DLE, AS/-TS/-ADS/, R_W/-W_R/, BE0/, BE1/, SIZ0-BHE/-BE2/, SIZ1-BE3/, BERR/-TEA/, HALT/-TIP/, BGACK-BB/, CBACK/-TBI/, STERM/-TA/-READYI/

Parameter	Symbol	Min	Max	Units	Conditions
Input high voltage	V_{IH}	2.0	$V_{DD} + 0.5$	V	-
Input low voltage	V_{IL}	$V_{SS} - 0.5$	0.8	V	-
Output high voltage	V_{OH}	2.4	V_{DD}	V	$I_{OH} = -16$ mA
Output low voltage	V_{OL}	V_{SS}	0.5	V	$I_{OL} = 16$ mA
Output high current	I_{OH}	-8.0	-	mA	$V_{OH} = V_{DD} - 0.5$ V
Output low current	I_{OL}	16.0	-	mA	$V_{OL} = 0.4$ V
Input leakage current	I_{IN}	-10	10	μA	-
Tristate leakage current	I_{OZ}	-10	10	μA	-

NCR 53C720

AC Characteristics

The AC characteristics described in this section apply over the entire range of operating conditions (refer to the *DC Characteristics* section). Chip timings are based on simulation at worst case voltage, temperature, and processing.

Figure 7-1. Clock Timing
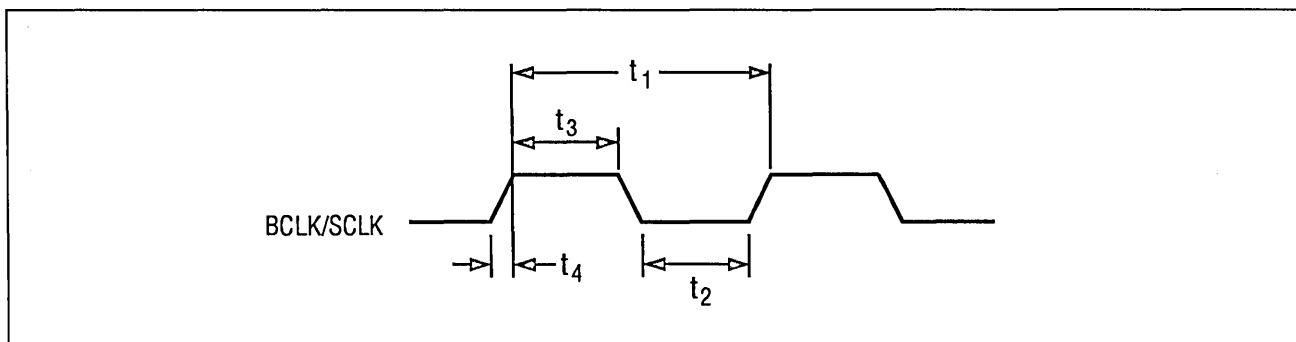
Parameter	Symbol	Min	Max	Units
Bus clock cycle time (t_{BCLK})	t_1	30	-	ns
SCSI clock cycle time (t_{SCLK})*		13.3	60	ns
BCLK low time	t_2	12	-	ns
SCLK low time		6	33	ns
BCLK high time	t_3	12	-	ns
SCLK high time		6	33	ns
BCLK slew rate	t_4	1	-	V/ns
SCLK slew rate		1	-	V/ns

* *This parameter must be met to insure SCSI timings are within specification.*
Maximum SCSI CLK Frequency = 75 MHz
Maximum BCLK Frequency = 33 MHz

Figure 7-2. Chip Reset Timing
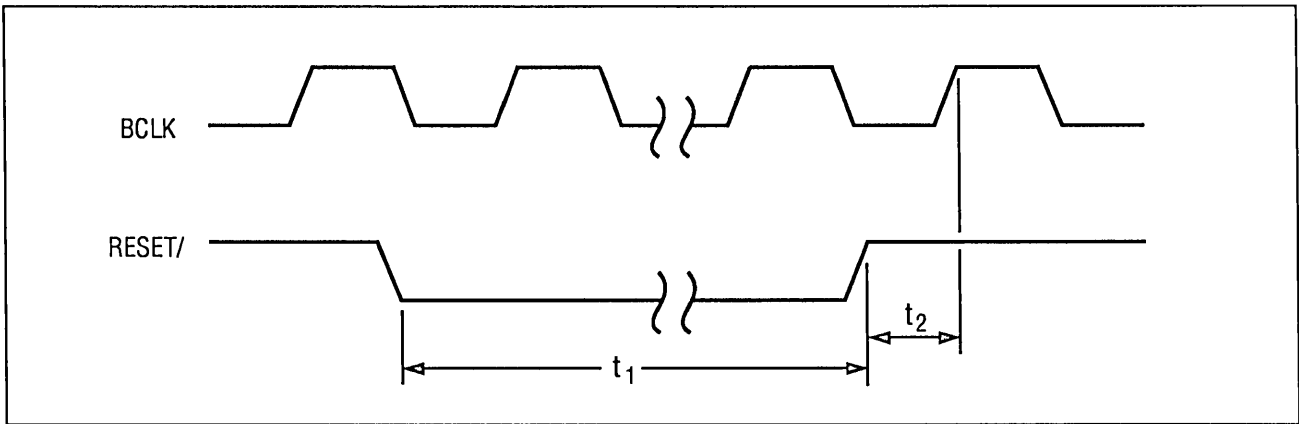
Parameter	Symbol	Min	Max	Units
Reset pulse width	t_1	10	-	t_{BCLK}
Reset deasserted setup to BCLK high	t_2	10	-	ns

NCR 53C720

Bus Mode 1 Slave Cycle

Bus Mode 1 Slave Read Sequence

1) R_W/, Address and Size lines are asserted by the CPU.

2) Address Strobe is asserted by the CPU.

3) Chip Select is validated by the 53C720 on any following rising edge of BCLK.

4) Cache Burst Acknowledge is deasserted by the 53C720.

5) Two clock cycles of wait state are inserted (these wait states are required) and the Data lines are asserted by the 53C720.

6) Slave Acknowledge is asserted by the 53C720 if the cycle ends normally or Bus Error is asserted if a bus error is detected.

7) Address Strobe is deasserted by the CPU.

8) Slave Acknowledge or Bus Error is deasserted by the 53C720 and the Data lines are tristated by the 53C720.

Parameter	Symbol	Min	Max	Units
AS/ setup to CS/ clocked active	t_1	5	-	ns
A(6-0), SIZ(1-0), R-W/ setup to AS/	t_2	4	-	ns
A(6-0), SIZ(1-0), R-W/ hold from AS/	t_3	8	-	ns
CS/ setup to BCLK high after AS/	t_4	5	-	ns
CS/ hold from BCLK high after AS/	t_5	5	-	ns
BCLK high to CBACK/ high	t_6	5	26	ns
BCLK high to CBACK/ low	t_7	3	17	ns
BCLK high to READYO/, BERR/ low	t_8	-	22	ns
AS/ high to READYO/, BERR/ high	t_9	-	20	ns
STERM/ setup to BCLK high	t_{10}	2	-	ns
STERM/ hold from BCLK high	t_{11}	6	-	ns
BCLK high to data bus driven	t_{12}	5	28	ns
BCLK high to read data valid	t_{13}	-	75	ns
AS/ high to data bus high-Z	t_{14}	7	32	ns

Figure 7-3. Bus Mode 1 Slave Read Cycle
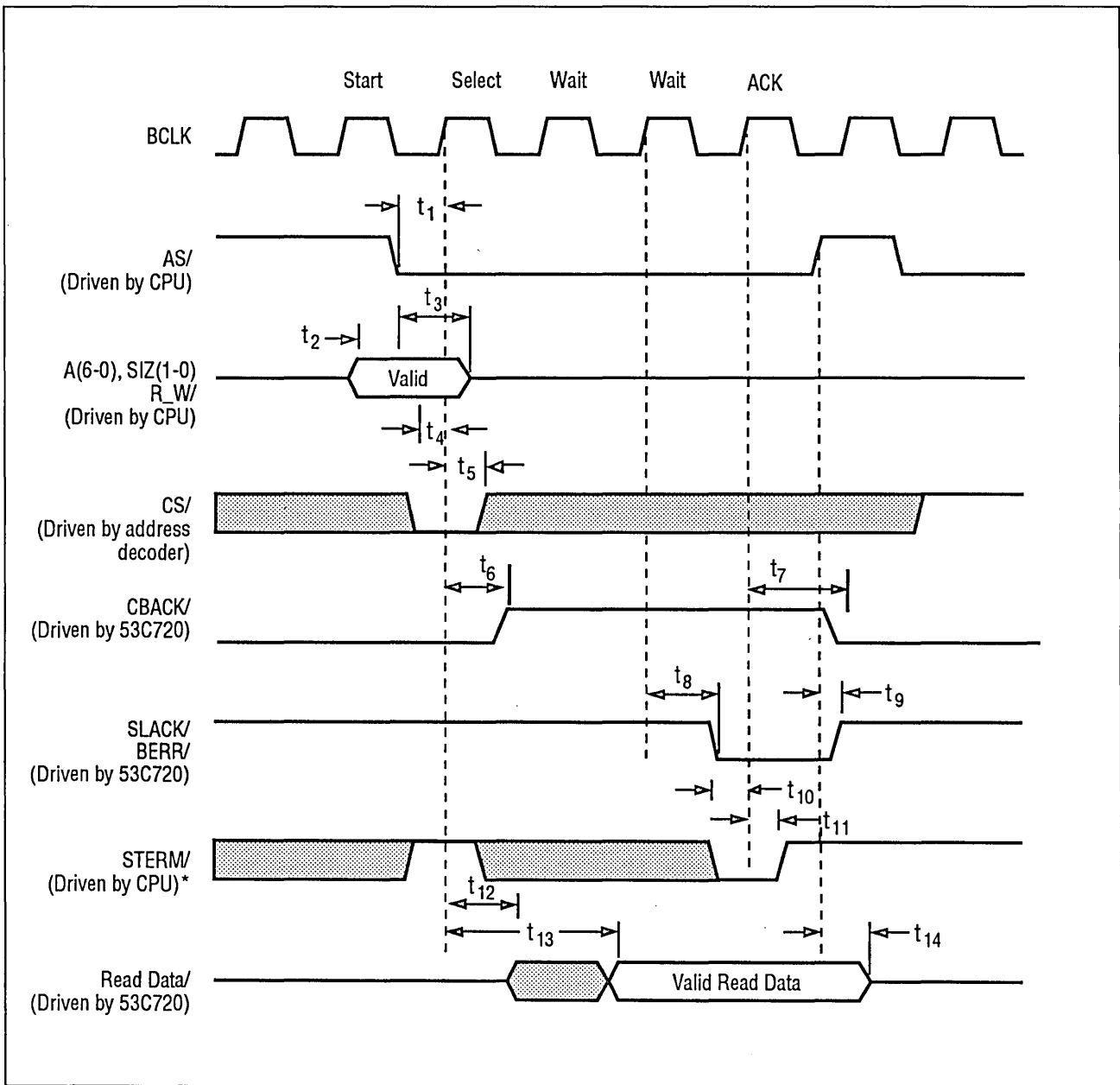
Note: Shaded area indicates that the signal is a don't care.

*This signal may be driven by the 53C720 if the ENABLE ACK bit is set (DCNTL Bit 5). See explanation on page 3-10 for use of this signal as an output.

NCR 53C720

Bus Mode 1 Slave Write Sequence

1) R_W/, Address and Size lines are asserted by the CPU.

2) Address Strobe is asserted by the CPU.

3) Chip Select is validated by the 53C720 on any following rising edge of BCLK.

4) Cache Burst Acknowledge is deasserted by the 53C720.

5) The Data lines are asserted by the CPU.

6) Slave Acknowledge is asserted by the 53C720 if the cycle ends normally or Bus Error is asserted if a bus error is detected.

7) Address Strobe is deasserted by the CPU.

8) Slave Acknowledge or Bus Error is deasserted by the 53C720.

Parameter	Symbol	Min	Max	Units
AS/ setup to CS/ clocked active	t_1	5	-	ns
A(6-0), SIZ(1-0), R-W/ setup to AS/	t_2	4	-	ns
A(6-0), SIZ(1-0), R-W/ hold from AS/	t_3	8	-	ns
CS/ setup to BCLK high after AS/	t_4	5	-	ns
CS/ hold from BCLK high after AS/	t_5	5	-	ns
BCLK high to CBACK/high	t_6	5	26	ns
BCLK high to CBACK/ low	t_7	3	17	ns
BCLK high to SLACK/, BERR/ low	t_8	-	22	ns
AS/ high to SLACK/, BERR/ high	t_9	-	20	ns
STERM/ (input) setup to BCLK high	t_{10}	2	-	ns
STERM/ (input) hold from BCLK high	t_{11}	6	-	ns
AS/ high to data bus high-Z	t_{12}	7	32	ns
Write data setup to BCLK low	t_{13}	2	-	ns
Write data hold from BCLK low	t_{14}	6	-	ns

Figure 7-4. Bus Mode 1 Slave Write Cycle

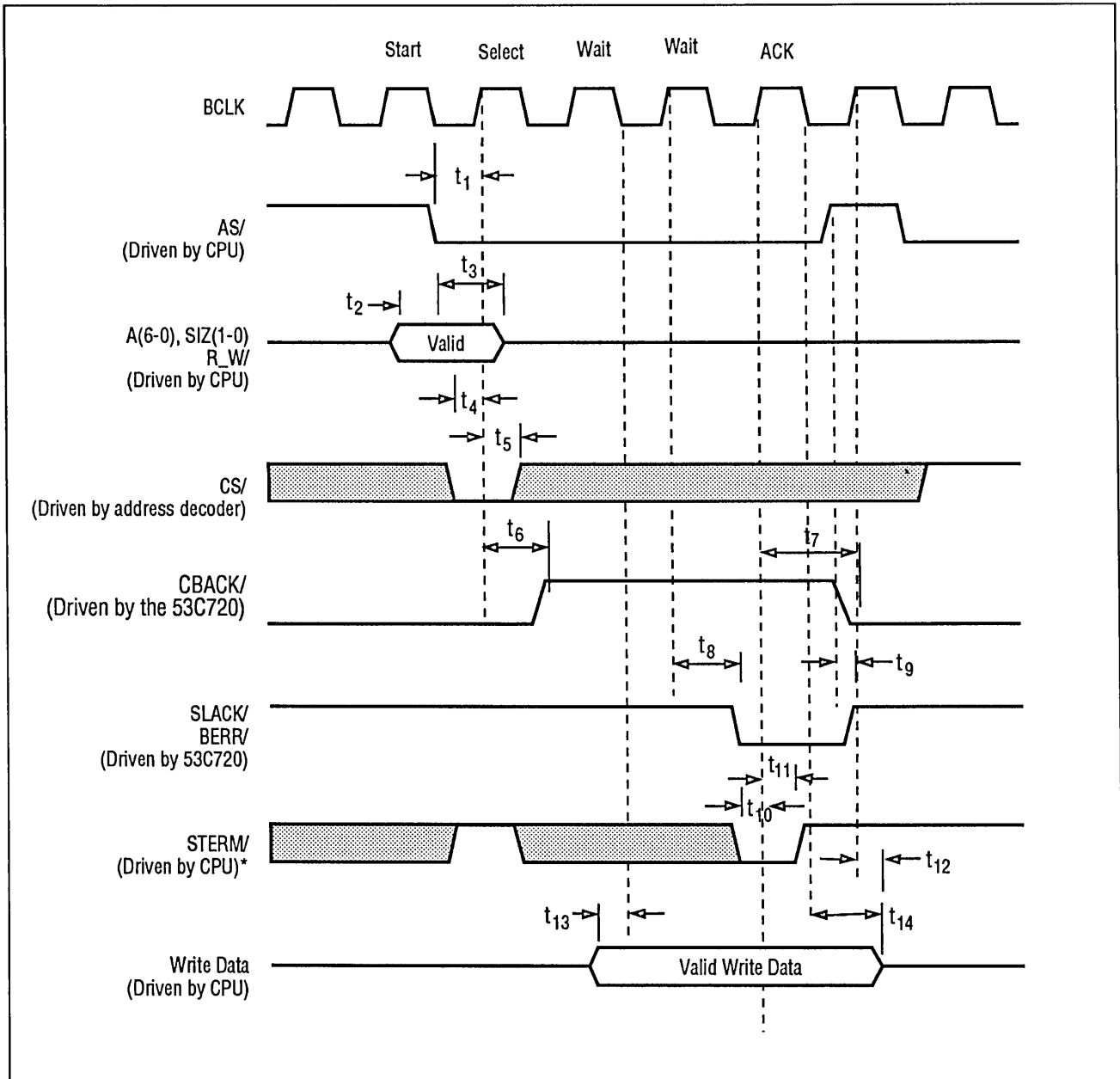Note: Shaded area indicates that the signal is a don't care.

*This signal may be driven by the 53C720 if the Enable Ack bit is set (DCNTL bit 5). See explanation on page 3-10 for use of this signal as an output.

NCR 53C720

Host Bus Arbitration, Bus Mode 1

Bus Arbitration Sequence

1) The 53C720 internally determines bus mastership is required. If appropriate, FETCH/ is asserted.

2) Bus Request is asserted.

3) The 53C720 waits for Bus Grant and checks that bus Grant Acknowledge is deasserted. Then the 53C720 asserts Bus Grant Acknowledge and Master, and deasserts Bus Request.

Parameter	Symbol	Min	Max	Units
SC0 high to BR/ low*	t_1	1	2	BCLK
BCLK high to SC0 low on last cycle*	t_2	5	28	ns
BCLK high to BR/ low	t_3	4	20	ns
BCLK high to BR/ high	t_4	5	25	ns
BG/ setup to BCLK high (any rising edge after BR/)	t_5	4	-	ns
BG/ hold from BCLK high (any rising edge after BR/)	t_6	5	-	ns
BGACK/ setup to BCLK high (any rising edge after BR/)	t_7	5	-	ns
BCLK high to BGACK/ low	t_8	4	24	ns
BCLK high to BGACK/ high	t_9	3	19	ns
BCLK high to BGACK/ high-Z	t_{10}	7	32	ns
BCLK high to MASTER/ low	t_{11}	5	22	ns
BCLK high to MASTER/ high	t_{12}	6	26	ns
BCLK high to FETCH/ low	t_{13}	5	36	ns
BCLK high to FETCH/ high	t_{14}	5	36	ns
FETCH/ low to BR/ low	t_{15}	1	2	BCLK
BGACK/ high to FETCH/ high**	t_{16}	1	2	BCLK

*When Snoop Mode bit 0 of CTEST3 is set to 1.

**During a Retry operation, FETCH/ will remain low until a successful completion of the opcode fetch or a fatal bus error.

Figure 7-5. Host Bus Arbitration, Bus Mode 1
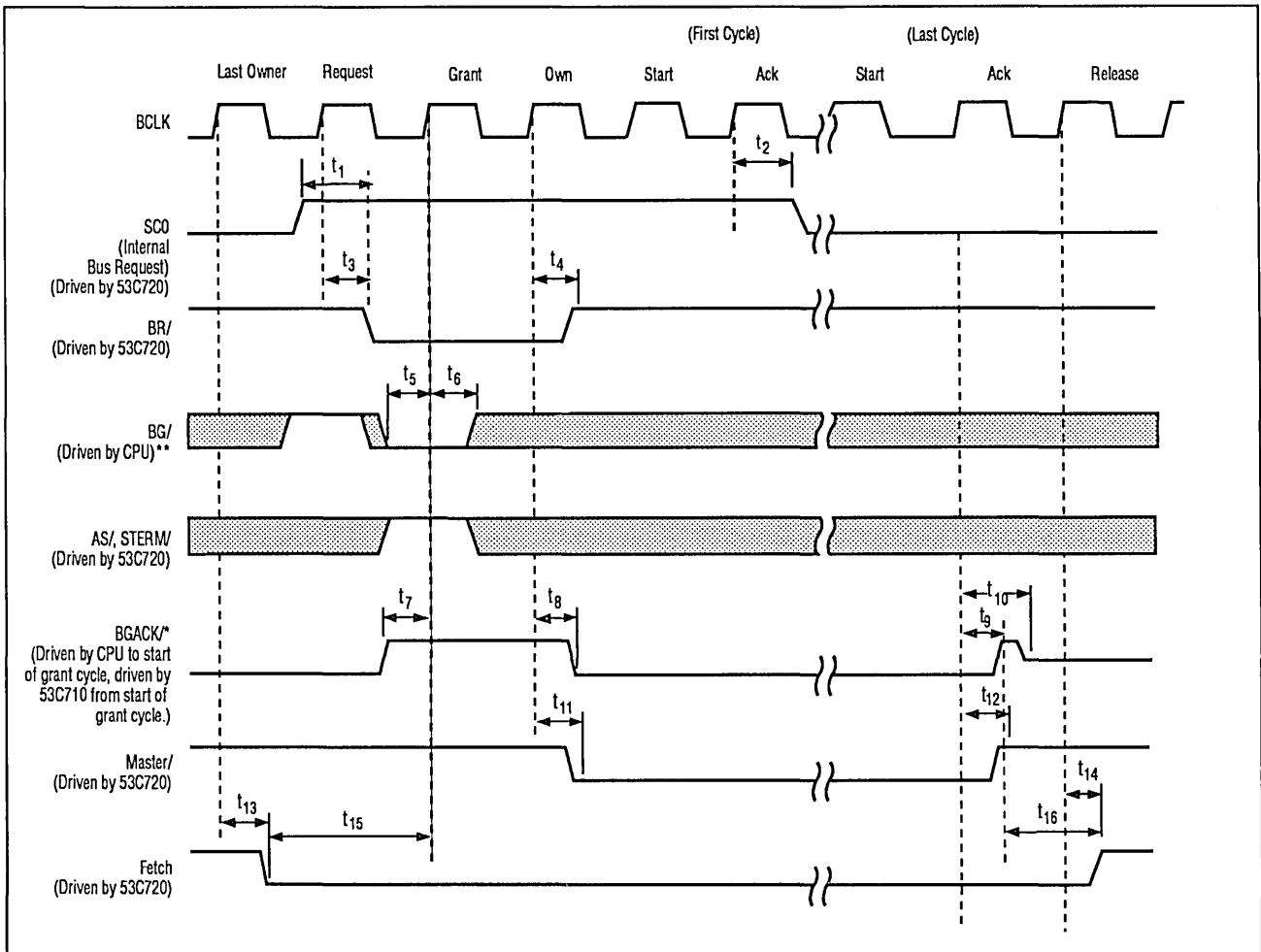
Note: Shaded area indicates that the signal is a don't care.

*If the fast arbitration bit is set (DCNTL bit 1) the 53C720 will drive the Bus Grant Acknowledge signal as soon as it receives a bus grant. One clock cycle of arbitration will be saved.

NCR 53C720

Bus Mode 1 Bus Master Read Sequence

1) The 53C720 has attained bus mastership.

2) The 53C720 asserts the R_W/, Snoop Control, Function Control and General Purpose lines.

3) The 53C720 asserts the Address and Size lines.

4) The 53C720 asserts Address Strobe, Cache Burst Request and Data Strobe.

5) The 53C720 waits for Synchronous Termination, Valid Data, Cache Burst Acknowledge, Bus Error and HALT.

   • If Cache Burst Acknowledge is asserted, attempt bursting.

   • If Bus Error and HALT are asserted, attempt a retry.

   • If Synchronous Termination is asserted without Bus Error or HALT, and the 53C720 requires more cycles, then return to function 3.

6) Upon acknowledge of the last bus cycle, the 53C720 deasserts Master and Bus Grant Acknowledge.

7) The 53C720 floats the Control and Address lines.

Bus Mode 1 Bus Master Read (Non-Cache-Line & Cache-Line Burst)

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	26	-	ns
BCLK high to AS/, DS/ driven	t_3	5	28	ns
BCLK low to AS/, DS/ low	t_4	3	16	ns
BCLK low to AS/, DS/ high	t_5	3	15	ns
BCLK high to AS/, DS/ high-Z	t_6	7	32	ns
STERM/ setup to BCLK high	t_7	3	-	ns
STERM/hold from BCLK high	t_8	7	-	ns
BCLK high to SIZ(1-0), A(31-0) driven	t_9	5	28	ns
BCLK high to SIZ(1-0), A(31-0) valid	t_{10}	4	20	ns
BCLK high to SIZ(1-0), A(31-0) high-Z	t_{11}	7	32	ns
BCLK high to R_W/, SC(1-0), FC(2-0), UPSO driven and valid	t_{12}	5	28	ns
BCLK high to R_W/, SC(1-0), FC(2-0), UPSO high-Z	t_{13}	6	30	ns
Read Data setup to BCLK low	t_{14}	2	-	ns
Read Data hold from BCLK low	t_{15}	4	-	ns
BCLK high to CBREQ/ driven	t_{16}	5	28	ns
BCLK low to CBREQ/ low	t_{17}	3	18	ns
BCLK low to CBREQ/ high	t_{18}	3	17	ns
BCLK high to CBREQ/ high-Z	t_{19}	7	32	ns
CBACK/ setup to BCLK high	t_{20}	6	-	ns
CBACK/ hold from BCLK high	t_{21}	4	-	ns
BERR/, HALT/ setup to BCLK low	t_{22}	6	-	ns
BERR/, HALT hold from BCLK low	t_{23}	4	-	ns

Figure 7-6. Bus Mode 1 Bus Master Read (Non-Cache-Line Burst)

* SC (1-0) timings apply only if Snoop Mode bit 0 of CTEST3 = 0.

Note: Shaded area indicates that the signal is a don't care.

Figure 7-7. Bus Mode 1 Bus Master Read (Cache-Line Burst)
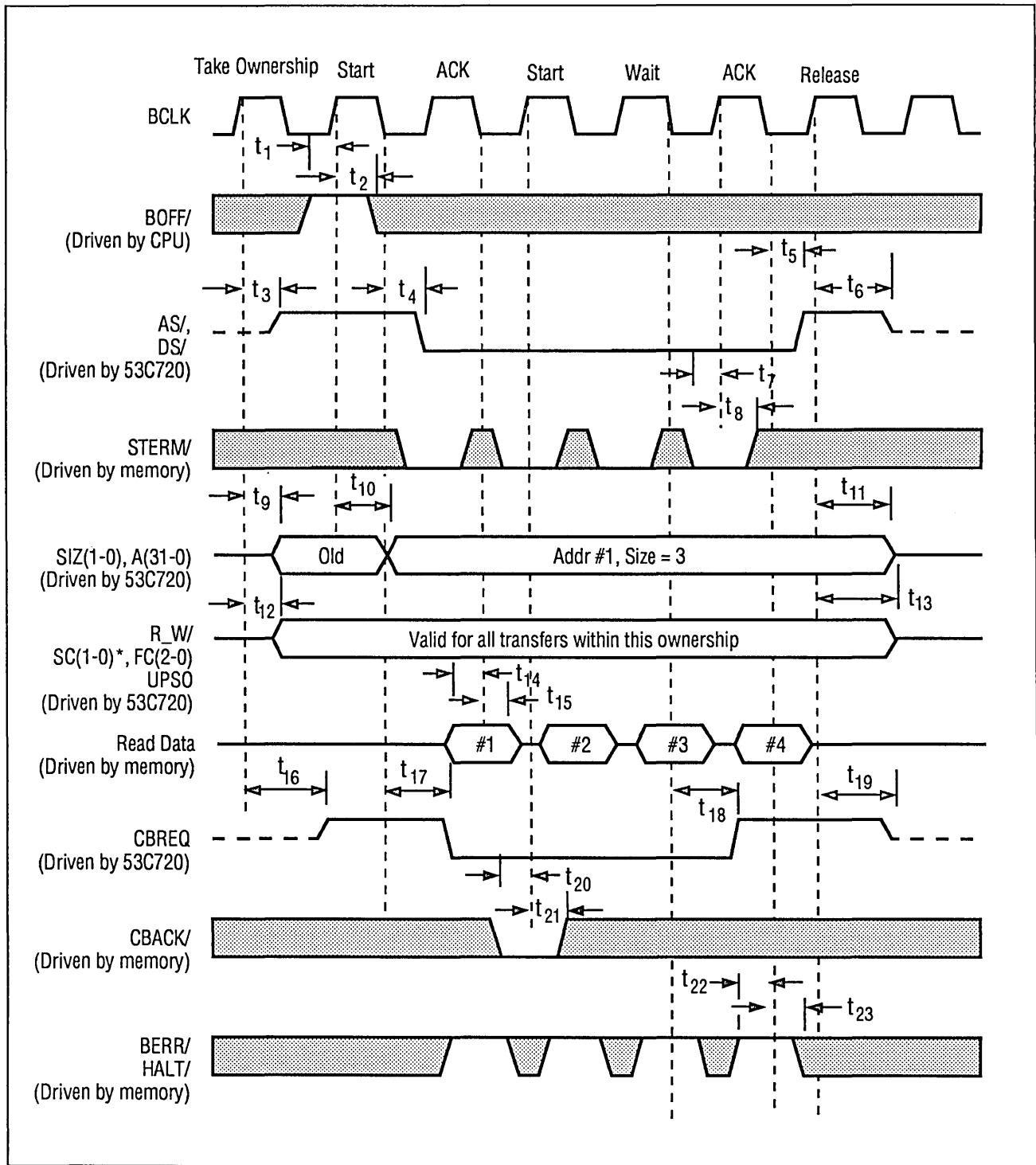
* SC (1-0) timings apply only if Snoop Mode bit 0 of CTEST3 = 0.

Note: Shaded area indicates that the signal is a don't care.
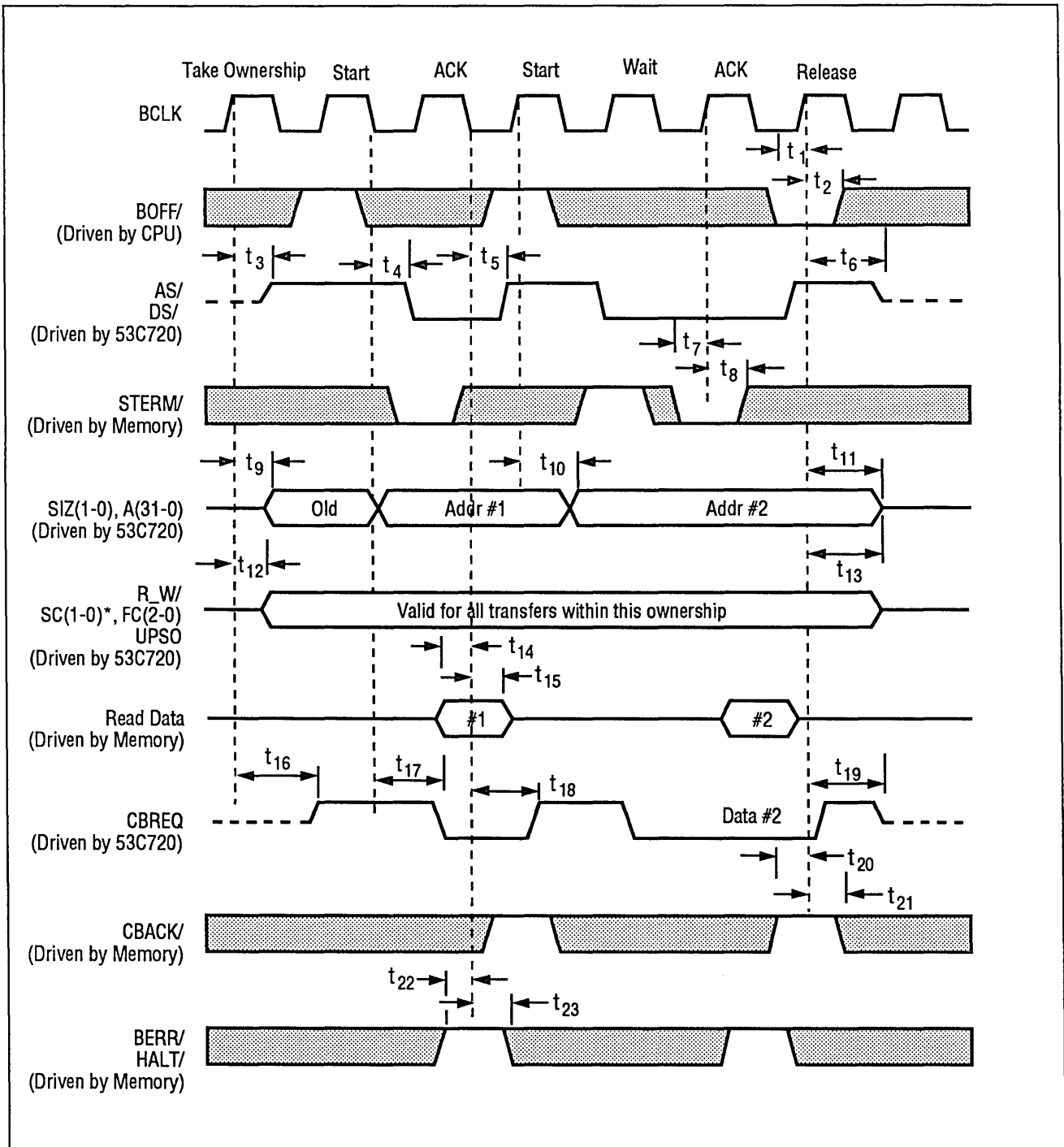
NCR 53C720

Bus Mode 1 Bus Master Write Sequence

1) The 53C720 has attained bus mastership.

2) The 53C720 asserts the R_W/, Snoop Control, Function Control and General Purpose lines.

3) The 53C720 asserts the Address, Size and Data lines.

4) The 53C720 asserts Address Strobe and Cache Burst Request.

5) The 53C720 asserts Data Strobe.

6) The 53C720 waits for Synchronous Termination, Cache Burst Acknowledge, Bus Error and HALT.

   • If Cache Burst Acknowledge is asserted, attempt bursting.

   • If Bus Error and HALT are asserted, attempt a retry.

   • If Synchronous Termination is asserted without Bus Error or HALT, and the 53C720 requires more cycles, then return to function 3.

7) Upon acknowledge of the last bus cycle, the 53C720 deasserts Master and Bus Grant Acknowledge.

8) The 53C720 floats the Control, Address and Data lines.

Bus Mode 1 Bus Master Write (Non-Cache-Line & Cache-Line Burst)

| Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	26	-	ns
BCLK high to AS/ driven	t_3	5	28	ns
BCLK low to AS/ low	t_4	3	16	ns
BCLK low to AS/ high	t_5	3	15	ns
BCLK high to AS/ high-Z	t_6	7	32	ns
STERM/ setup to BCLK high	t_7	3	-	ns
STERM/ hold from BCLK high	t_8	7	-	ns
BCLK high to SIZ(1-0), SIZ(1-0), A(31-0) driven	t_9	5	28	ns
BCLK high to SIZ(1-0), SIZ(1-0), A(31-0) valid	t_{10}	4	20	ns
BCLK high to SIZ(1-0), A(31-0) high-Z	t_{11}	7	32	ns
BCLK high to R_W/, SC(1-0), FC(2-0), UPSO driven and valid	t_{12}	5	28	ns
BCLK high to R_W/, SC(1-0), FC(2-0), UPSO high-Z	t_{13}	6	30	ns
BCLK high to Write Data driven	t_{14}	6	28	ns
BCLK high to Write Data valid	t_{15}	6	28	ns
BCLK high to Data high-Z	t_{16}	6	32	ns
BCLK high to DS/ driven	t_{17}	5	28	ns
BCLK low to DS/ low	t_{18}	3	17	ns
BCLK low to DS/ high	t_{19}	3	17	ns
BCLK high to DS/ high-Z	t_{20}	7	32	ns
BCLK high to CBREQ/ driven	t_{21}	5	28	ns
BCLK low to CBREQ/ low	t_{22}	3	18	ns
BCLK low to CBREQ/ high	t_{23}	3	17	ns
BCLK high to CBREQ/ high-Z	t_{24}	7	32	ns
CBACK/ setup to BCLK high	t_{25}	6	-	ns
CBACK/ hold from BCLK high	t_{26}	4	-	ns
BERR/, HALT/ setup to BCLK low	t_{27}	6	-	ns
BERR/, HALT hold from BCLK low	t_{28}	4	-	ns

Figure 7-8. Bus Mode 1 Bus Master Write (Non-Cache-Line Burst)

* SC (1-0) timings apply only if Snoop Mode bit 0 of CTEST3 = 0.

Note: Shaded area indicates that the signal is a don't care.
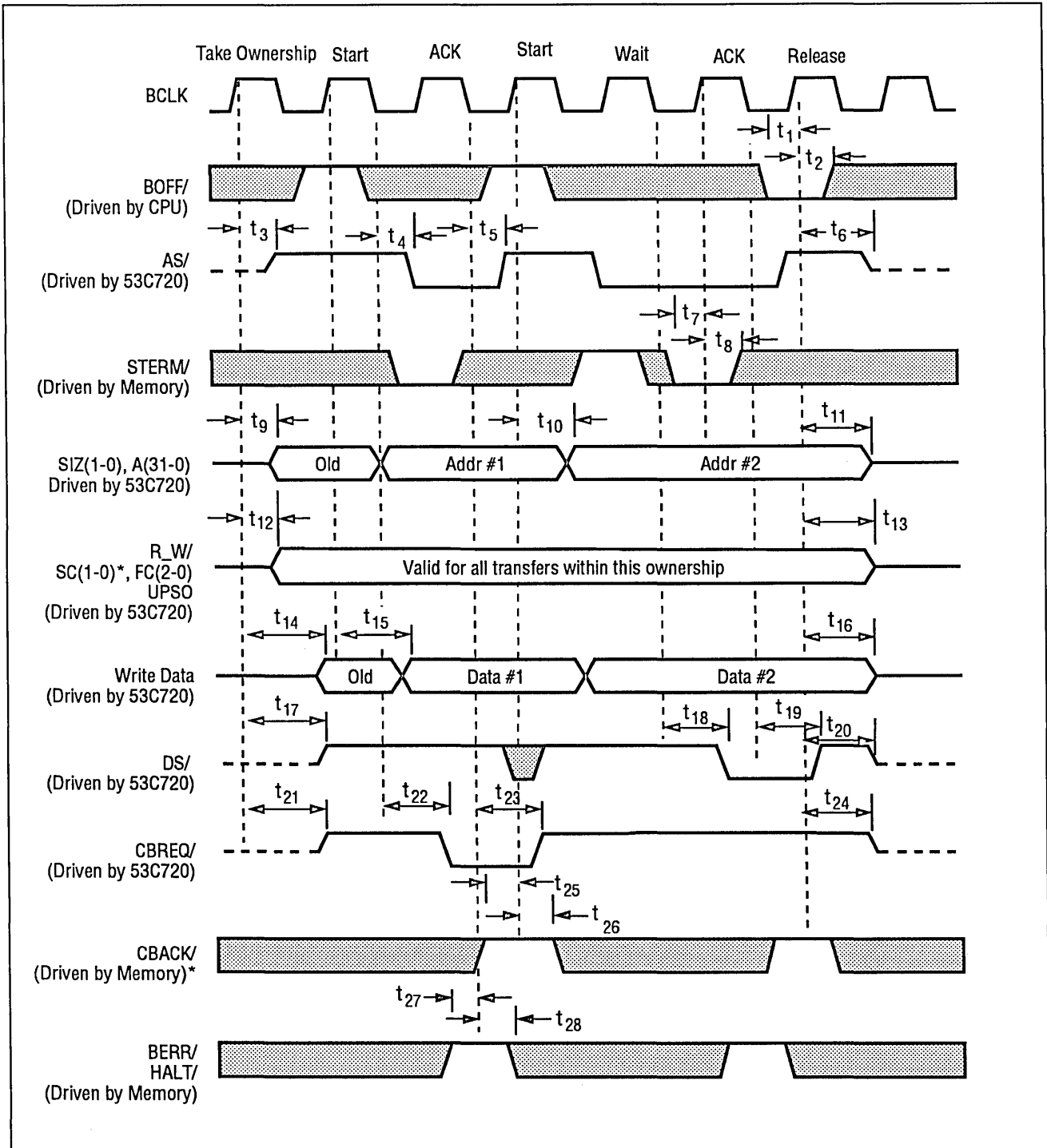
Figure 7-9. Bus Mode 1 Bus Master Write (Cache-Line Burst)
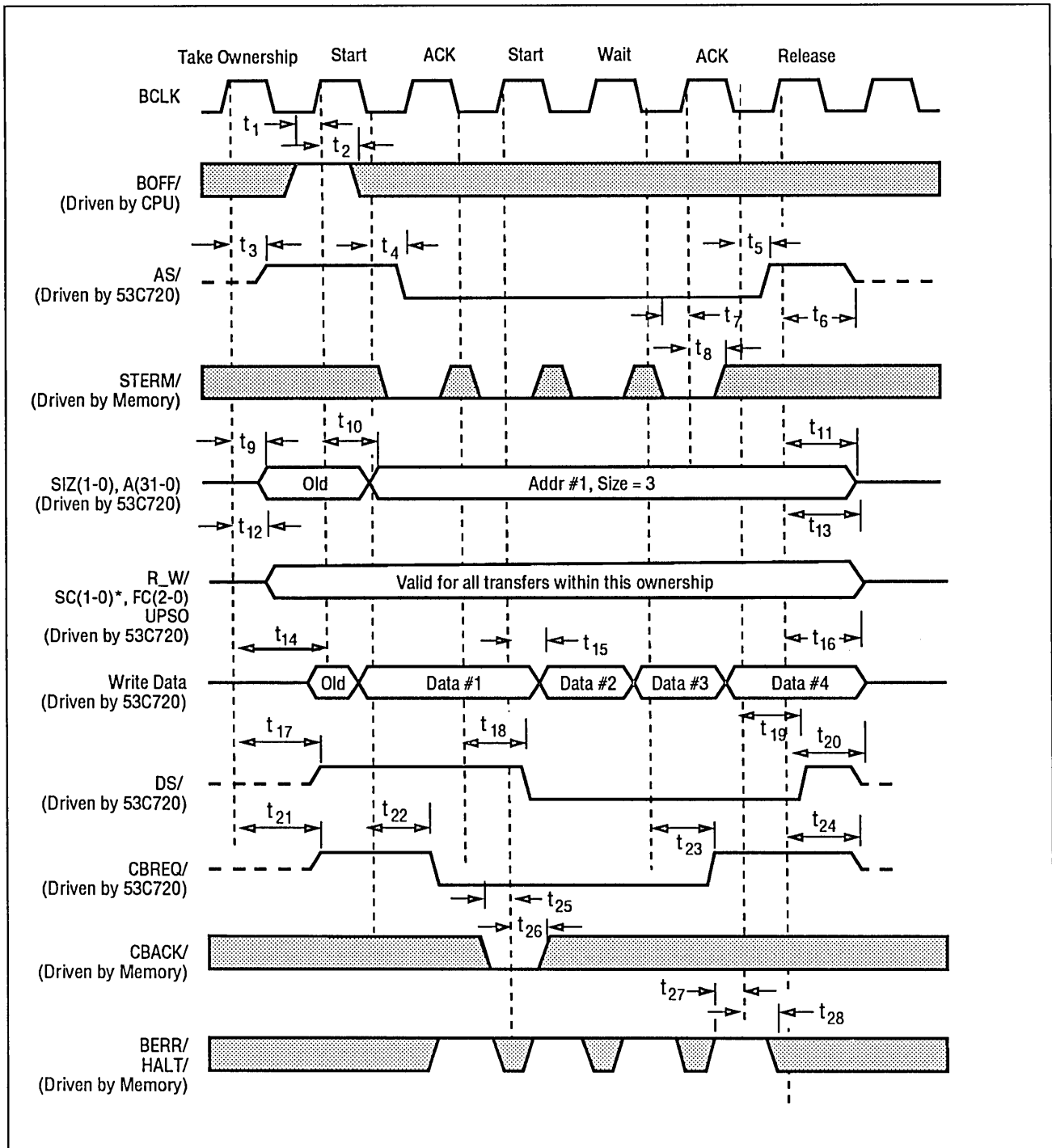
* SC (1-0) timings apply only if Snoop Mode bit 0 of CTEST3 = 0.

Note: Shaded area indicates that the signal is a don't care.

NCR 53C720

Bus Mode 2 Slave Cycle

Bus Mode 2 Slave Read Sequence

1) R_W/, Address, Transfer Start and the Size lines are asserted by the CPU.

2) Chip Select is validated by the 53C720 on any following rising edge of BCLK.

3) Transfer Burst Inhibit is asserted.

4) Transfer Start is deasserted by the CPU.

5) Three clock cycles of wait state are inserted and the Data lines are asserted.

6) Slave Acknowledge is asserted by the 53C720, if no errors are detected.

7) If a bus error is detected, only Transfer Error Acknowledge is asserted and the bus cycle ends on the next rising edge of BCLK.

8) Slave Acknowledge or Transfer Error Acknowledge is deasserted.

9) The 53C720 waits for Transfer Acknowledge to be asserted and then ends the slave cycle, if no errors are detected.

10) The Data lines are tristated by the 53C720.

Parameter	Symbol	Min	Max	Units
TS/ setup to BCLK high	t_1	4	-	ns
TS/ hold from BCLK high	t_2	5	-	ns
CS/ setup to BCLK high after TS/	t_3	5	-	ns
CS/ hold from BCLK high after TS/	t_4	5	-	ns
BCLK high to TBI/ low	t_5	5	30	ns
BCLK high to TBI/ high	t_6	4	22	ns
BCLK high to SLACK/, TEA/ low	t_7	5	22	ns
BCLK high to SLACK/, TEA/ high	t_8	4	20	ns
TA/ setup to BCLK high during or after SLACK/, TEA/	t_9	8	-	ns
TA/ hold from BCLK high during or after SLACK/, TEA/	t_{10}	4	-	ns
BCLK high to data bus driven	t_{11}	5	28	ns
BCLK high to read data valid	t_{12}	-	75	ns
BCLK high to data bus high-Z	t_{13}	7	32	ns
A(6-0), SIZ(1-0), R_W/ setup to BCLK high	t_{14}	2	-	ns
A(6-0), SIZ(1-0), R_W/ hold from BCLK high	t_{15}	12	-	ns

Figure 7-10. Bus Mode 2 Slave Read
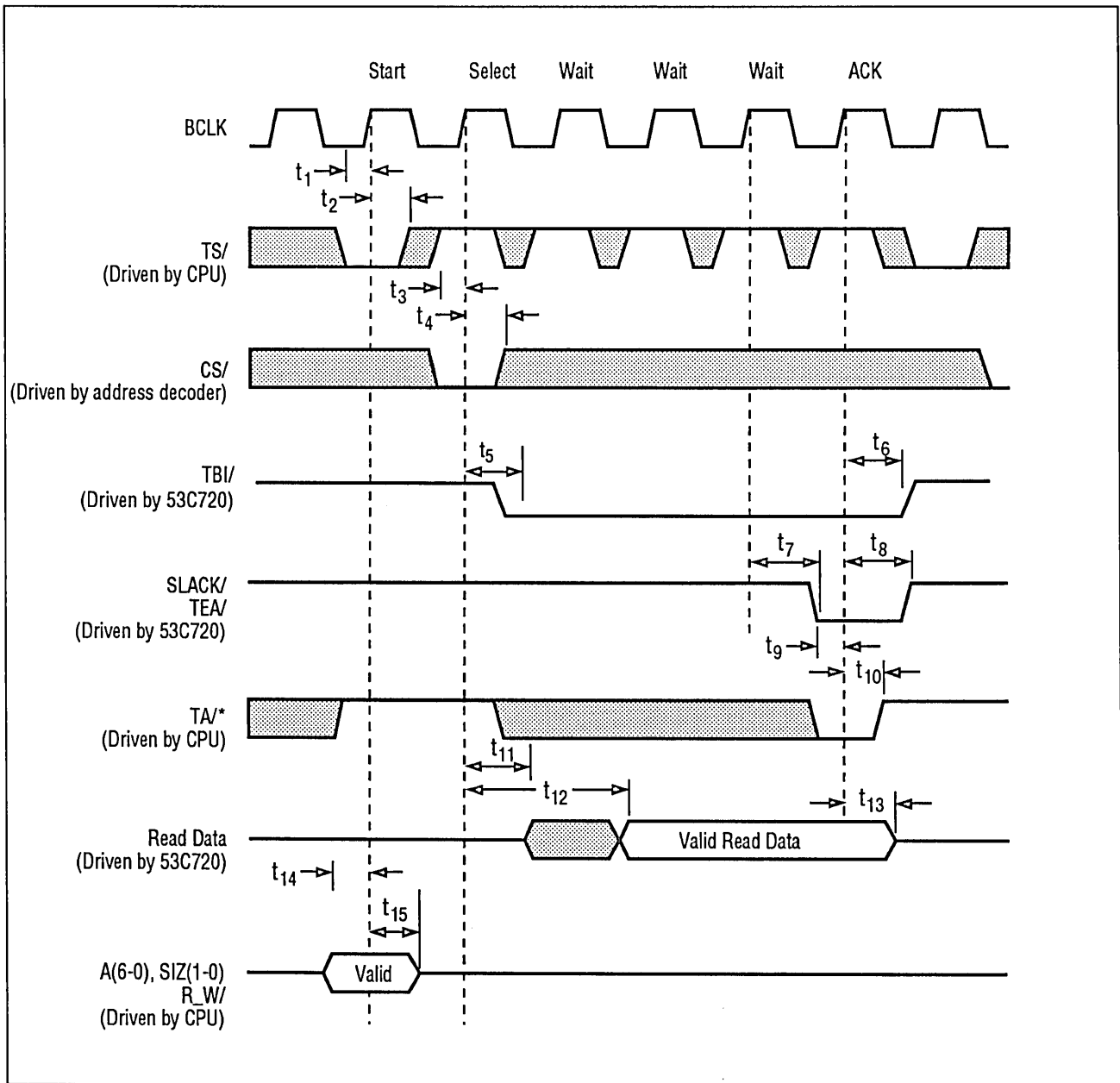
Note: Shaded areas indicate that the signal is a don't care.

*This signal may be driven by the 53C720 if the ENABLE ACK bit is set (DCNTL Bit 5). See explanation on page 3-10 for use of this signal as an output.

NCR 53C720

Bus Mode 2 Slave Write Sequence

1) R_W/, Address, Transfer Start and the Size lines are asserted by the CPU.

2) Chip Select is validated by the 53C720 on any following rising edge of BCLK.

3) Transfer Burst Inhibit is asserted.

4) Transfer Start is deasserted by the CPU.

5) The Data lines are asserted by the CPU.

6) Three clock cycles of wait state are inserted (These wait states are required).

7) Slave Acknowledge is asserted by the 53C720, if no errors are detected

8) If a bus error is detected, only Transfer Error Acknowledge is asserted and the bus cycle ends on the next rising edge of BCLK.

9) Slave Acknowledge or Transfer Error Acknowledge is deasserted.

10) The 53C720 waits for Transfer Acknowledge to be asserted and then ends the slave cycle, if no error.

Parameter	Symbol	Min	Max	Units
TS/ setup to BCLK high	t_1	4	-	ns
TS/ hold from BCLK high	t_2	5	-	ns
CS/ setup to BCLK high after TS/	t_3	5	-	ns
CS/ hold from BCLK high after TS/	t_4	5	-	ns
BCLK high to TBI/ low	t_5	5	30	ns
BCLK high to TBI/ high	t_6	4	22	ns
BCLK high to SLACK/, TEA/ low	t_7	5	22	ns
BCLK high to SLACK/, TEA/ high	t_8	4	20	ns
TA/ setup to BCLK high during or after SLACK/, TEA/	t_9	8	-	ns
TA/ hold from BCLK high during or after SLACK/, TEA/	t_{10}	4	-	ns
Valid write data setup to BCLK high	t_{11}	4	-	ns
Valid write data hold from BCLK high	t_{12}	6	-	ns
A(6-0), SIZ(1-0), R_W/ setup to BCLK high	t_{13}	2	-	ns
A(6-0), SIZ(1-0), R_W/ hold from BCLK high	t_{14}	12	-	ns

Figure 7-11. Bus Mode 2 Slave Write

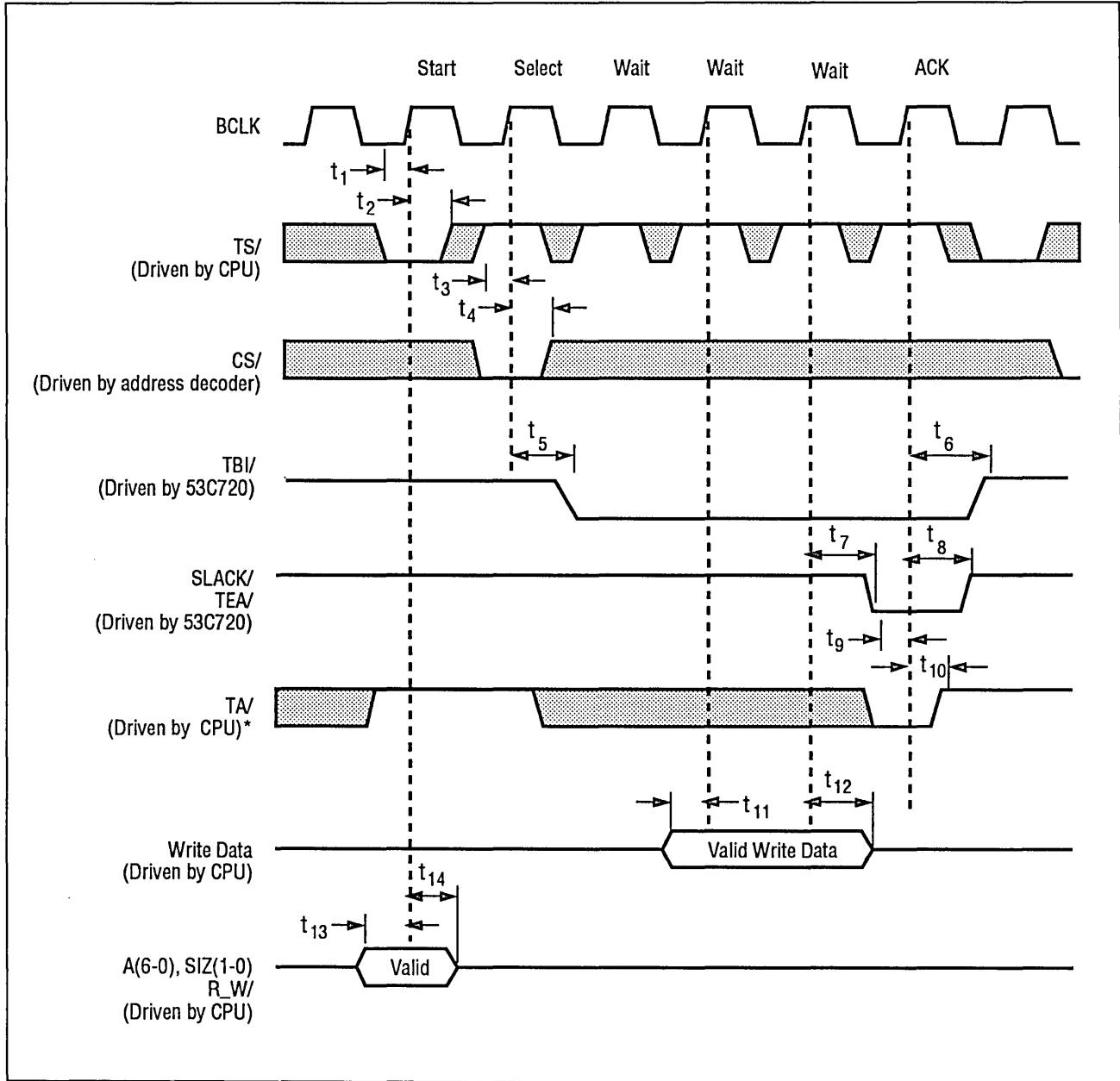Note: Shaded areas indicate that the signal is a don't care.

*This signal may be driven by the 53C720 if the ENABLE ACK bit is set (DCNTL Bit 5). See explanation on page 3-10 for use of this signal as an output.

NCR 53C720

Host Bus Arbitration, Bus Mode 2

Bus Arbitration Sequence

1) The 53C720 internally determines bus mastership is required. If appropriate, FETCH/ is asserted.

2) Bus Request is asserted.

3) The 53C720 waits for Bus Grant and checks that bus Grant Acknowledge is deasserted. Then the 53C720 asserts Bus Grant Acknowledge and Master, and deasserts Bus Request.

Parameter	Symbol	Min	Max	Units
SC0 high to BR/ low*	t_1	1	2	BCLK
BCLK high to SC0 low on last cycle*	t_2	5	28	ns
BCLK high to BR/ low	t_3	4	20	ns
BCLK high to BR/ high	t_4	5	25	ns
BG/ setup to BCLK high (any rising edge after BR/)	t_5	4	-	ns
BG/ hold from BCLK high (any rising edge after BR/)	t_6	5	-	ns
BB/ setup to BCLK high (any rising edge after BR/)	t_7	4	-	ns
BCLK high to BB/ low	t_8	4	24	ns
BCLK high to BB/ high	t_9	3	19	ns
BCLK high to BB/ high-Z	t_{10}	7	32	ns
BCLK high to MASTER/ low	t_{11}	5	22	ns
BCLK high to MASTER/ high	t_{12}	6	26	ns
BCLK high to FETCH/ low	t_{13}	5	36	ns
BCLK high to FETCH/ high	t_{14}	5	36	ns
FETCH/ low to BR/ low	t_{15}	1	2	BCLK
BB/ high to FETCH/ high**	t_{16}	1	2	BCLK

*When Snoop Mode bit 0 of CTEST 3 is set to 1.

**During a retry operation, FETCH/ will remain low until a successful completion of the opcode fetch or a fatal bus error.

Figure 7-12. Host Bus Arbitration, Bus Mode 2
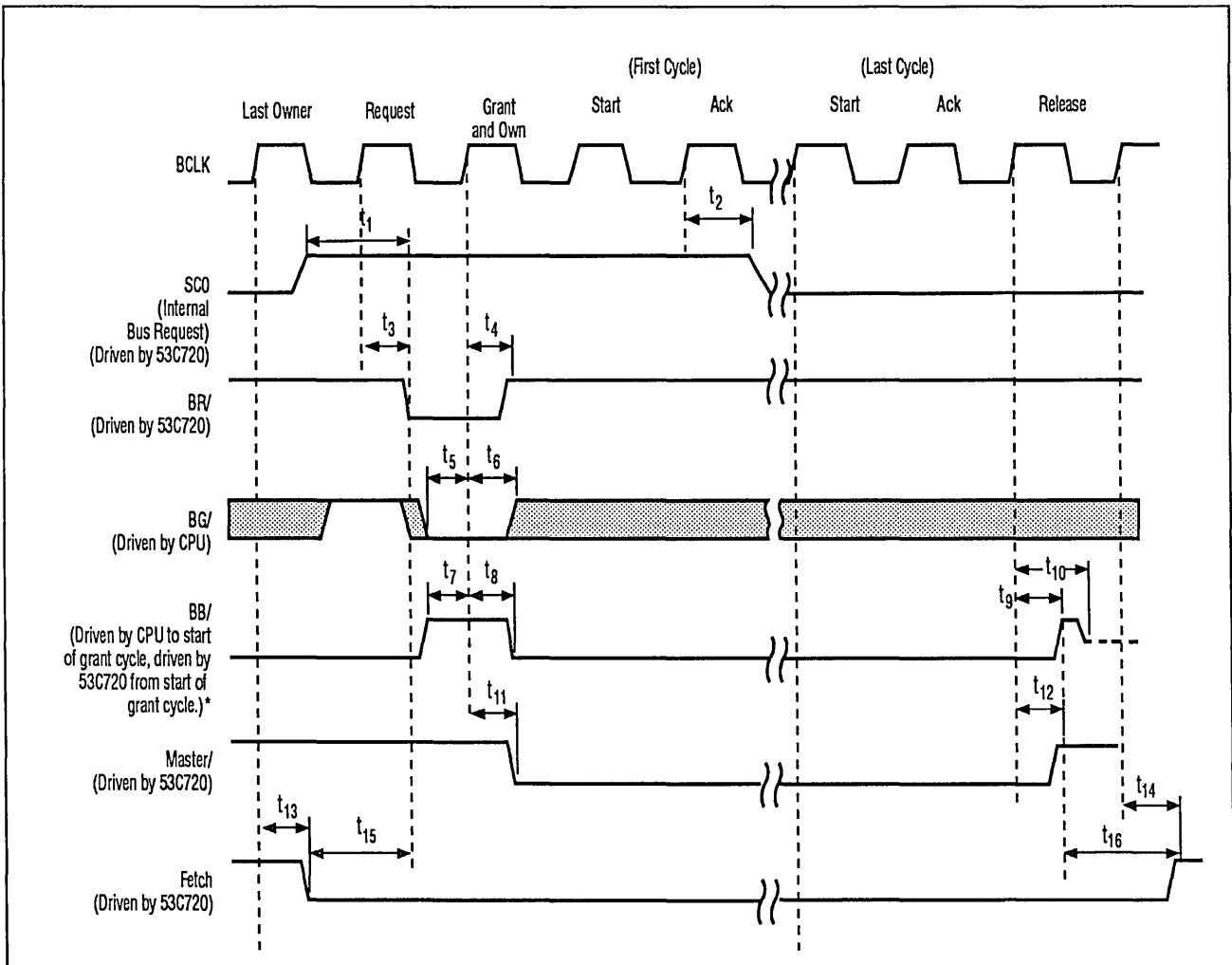
Note: shaded area indicates that the signal is a don't care.

*If the fast arbitration bit is set (DCNTL bit 1) the 53C720 will drive the Bus Grant Acknowledge signal as soon as it receives a bus grant. One clock cycle of arbitration will be saved.

NCR 53C720

Bus Mode 2 Master Cycle

Bus Mode 2 Bus Master Read Sequence

1) The 53C720 has attained bus mastership.

2) The 53C720 asserts the R_W/, Snoop Control, Transfer Modifier and Transfer Type lines.

3a) The 53C720 asserts Transfer in Progress.

3b) The 53C720 asserts Transfer Start, Address, and Size lines.

4) The 53C720 deasserts Transfer Start.

5) The 53C720 waits for Transfer Acknowledge, Valid Data, Transfer Burst Inhibit and Transfer Error Acknowledge.

   • If Transfer Burst Inhibit is not asserted, attempt cache bursting.

   • If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.

   • If Transfer Error Acknowledge is asserted and Transfer Acknowledge is not asserted, a bus fault condition will be generated.

   • If Transfer Acknowledge is asserted and Transfer Error Acknowledge is not asserted and the 53C720 requires more cycles, then return to step 3b.

6) Upon acknowledge of the last bus cycle, the 53C720 deasserts Master, Bus Busy, and Transfer in Progress.

7) The 53C720 floats the Control and Address lines.

Bus Mode 2 Bus Master Read (Non-Cache-Line & Cache-Line Burst)

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high*	t_2	26	-	ns
BCLK high to TIP/ driven	t_3	5	30	ns
BCLK high to TIP/ low	t_4	3	18	ns
BCLK high to TIP/ high	t_5	3	17	ns
BCLK high to TIP/ high-Z	t_6	7	32	ns
BCLK high to TS/ driven	t_7	5	28	ns
BCLK high to TS/ low	t_8	3	17	ns
BCLK high to TS/ high	t_9	3	17	ns
BCLK high to TS/ high-Z	t_{10}	7	32	ns
TA/ setup to BCLK high	t_{11}	8	-	ns
TA/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-0), SIZ(1-0) driven	t_{13}	5	28	ns
BCLK high to A(31-0), SIZ(1-0) valid	t_{14}	3	20	ns
BCLK high to A(31-0), SIZ(1-0) high-Z	t_{15}	7	32	ns
BCLK high to R_W/, SC(1-0), TM(2-0), TT(1-0) driven and valid	t_{16}	5	28	ns
BCLK high to R_W/, SC(1-0), TM(2-0), TT(1-0) high-Z	t_{17}	-	32	ns
Read Data setup to BCLK high	t_{18}	4	-	ns
Read Data hold from BCLK high	t_{19}	6	-	ns
TBI setup to BCLK high	t_{20}	6	-	ns
TBI hold from BCLK high	t_{21}	4	-	ns
TEA setup to BCLK high	t_{22}	6	-	ns
TEA hold from BCLK high	t_{23}	4	-	ns

*Only required during the cycle in which BOFF/ is recognized.

Figure 7-13. Bus Mode 2 Bus Master Read (Non-Cache-Line Burst)
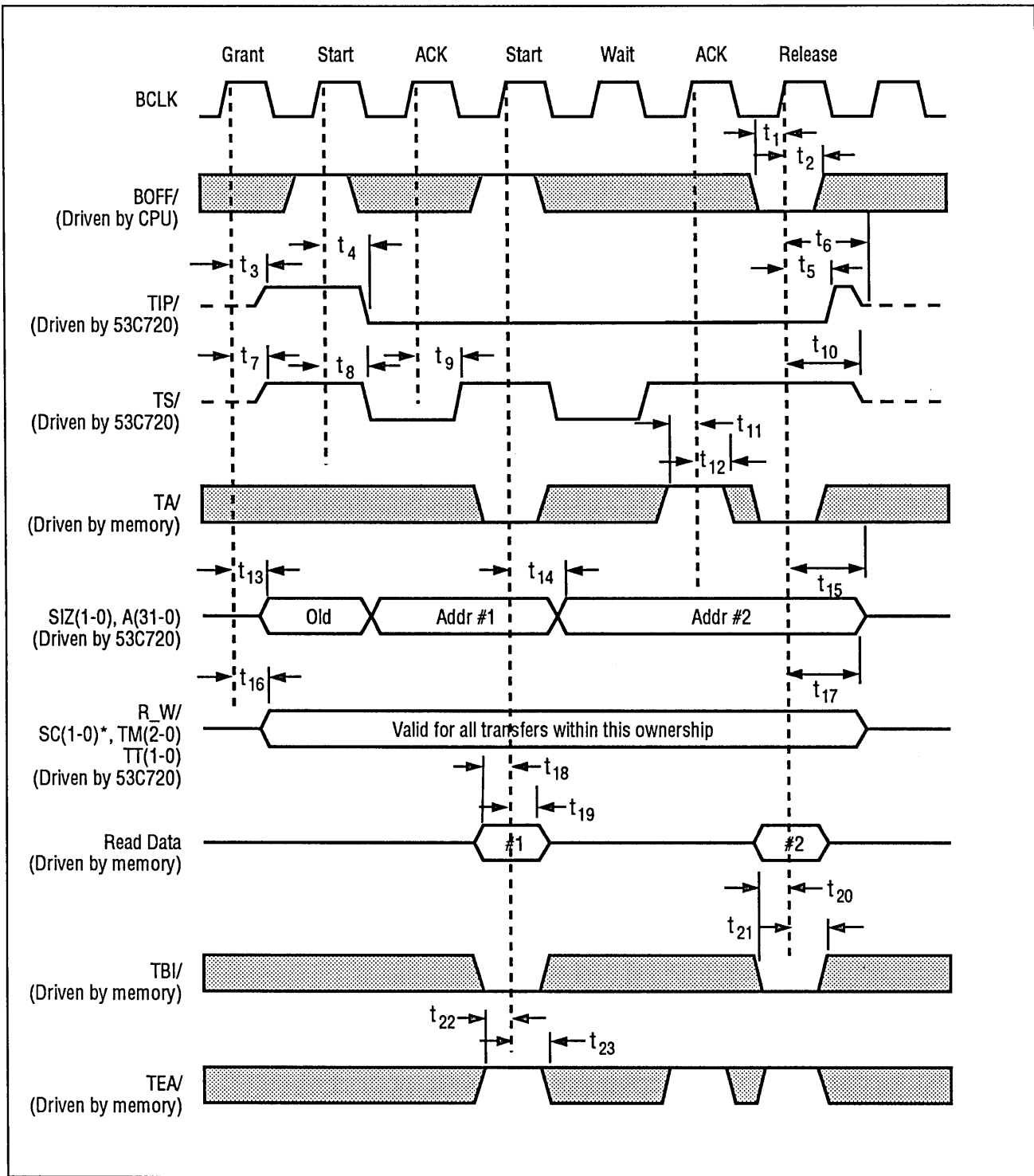
* SC (1-0) timings apply only if Snoop Mode bit 0 of CTEST3 = 0.

Note: Shaded areas indicate that the signal is a don't care

Figure 7-14. Bus Mode 2 Bus Master Read (Cache-Line Burst)

* SC (1-0) timings apply only if Snoop Mode bit 0 of CTEST3 = 0.

Note: Shaded areas indicate that the signal is a don't care

Bus Mode 2 Bus Master Write Sequence

1) The 53C720 has attained bus mastership.

2) The 53C720 asserts the R_W/, Snoop Control, Transfer Modifier and Transfer Type lines.

3a) The 53C720 asserts Transfer in Progress.

3b) The 53C720 asserts Transfer Start, Address, Size lines and Data lines.

4) The 53C720 deasserts Transfer Start.

5) The 53C720 waits for Transfer Acknowledge, Transfer Burst Inhibit and Transfer Error Acknowledge.

- If Transfer Burst Inhibit is not asserted, attempt cache bursting.

- If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.

- If Transfer Error Acknowledge is asserted and Transfer Acknowledge is not asserted, a bus fault condition will be generated.

- If Transfer Acknowledge is asserted and Transfer Error Acknowledge is not asserted and the 53C720 requires more cycles, then return to step 3b.

6) Upon acknowledge of the last bus cycle, the 53C720 deasserts Master, Busy, and Transfer in Progress.

7) The 53C720 floats the Control, Address and Data lines.

Bus Mode 2 Bus Master Write Cycle (Non-Cache-Line & Cache-Line Burst)

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high*	t_2	26	-	ns
BCLK high to TIP/ driven	t_3	5	30	ns
BCLK high to TIP/ low	t_4	3	18	ns
BCLK high to TIP/ high	t_5	3	17	ns
BCLK high to TIP/ high-Z	t_6	7	32	ns
BCLK high to TS/ driven	t_7	5	28	ns
BCLK high to TS/ low	t_8	3	17	ns
BCLK high to TS/ high	t_9	3	17	ns
BCLK high to TS/ high-Z	t_{10}	7	32	ns
TA/ setup to BCLK high	t_{11}	8	-	ns
TA/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-0), SIZ(1-0) driven	t_{13}	5	28	ns
BCLK high to A(31-0), SIZ(1-0) valid	t_{14}	3	20	ns
BCLK high to A(31-0), SIZ(1-0) high-Z	t_{15}	7	32	ns
BCLK high to R_W/, SC(1-0), TM(1-0), TT(1-0) driven and valid	t_{16}	5	28	ns
BCLK high to R_W/, SC(1-0), TM(2-0), TT(1-0) high-Z	t_{17}	5	32	ns
BCLK high to Write Data driven	t_{18}	5	30	ns
BCLK high to Write Data valid	t_{19}	5	28	ns
BCLK high to Write Data high-Z	t_{20}	5	30	ns
TBI setup to BCLK high	t_{21}	6	-	ns
TBI hold from BCLK high	t_{22}	4	-	ns
TEA setup to BCLK high	t_{23}	6	-	ns
TEA hold from BCLK high	t_{24}	4	-	ns

*Only required during the cycle in which BOFF/ is recognized.
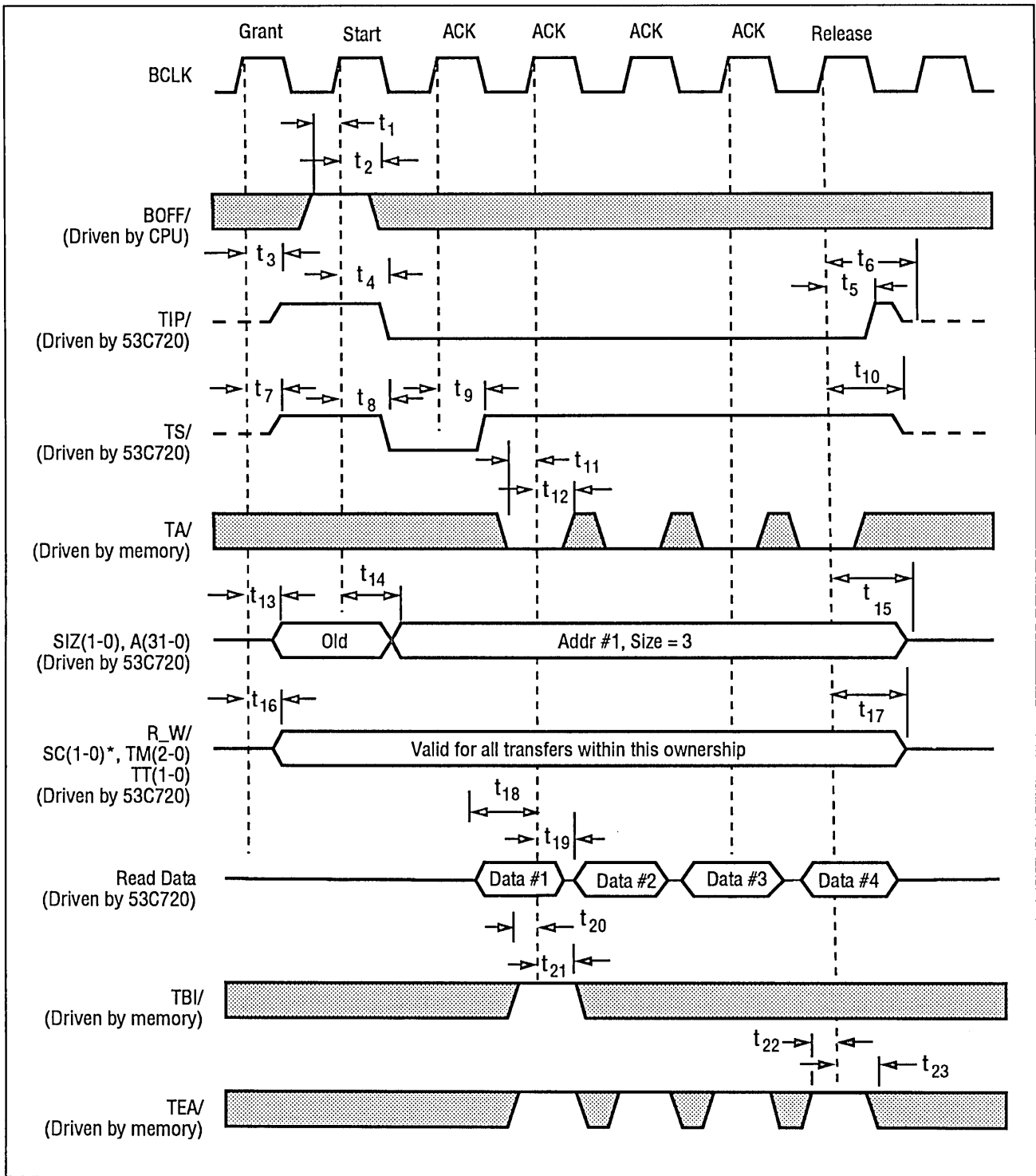
NCR 53C720

Figure 7-15. Bus Mode 2 Bus Master Write (Non-Cache-Line Burst)
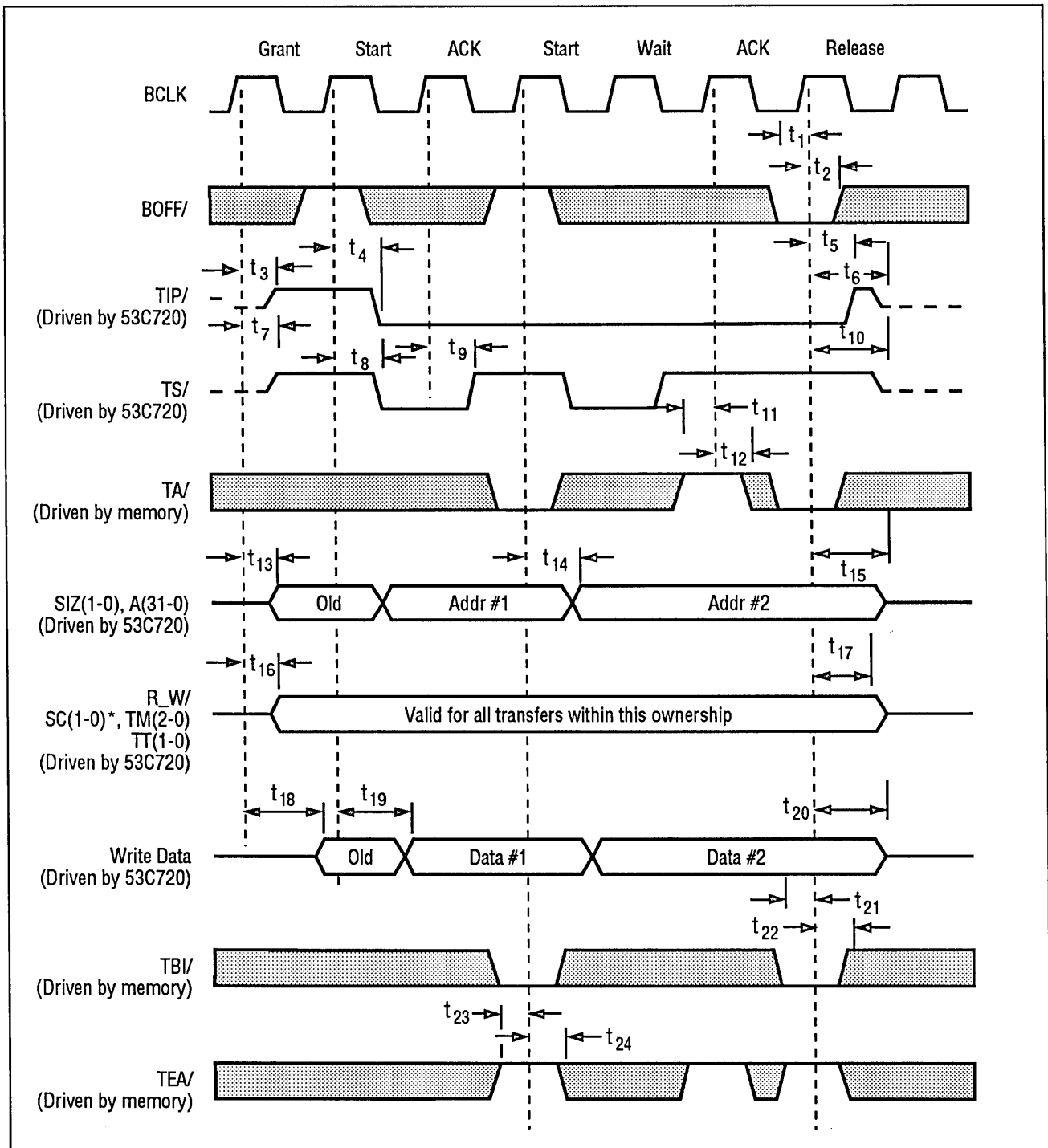
* SC (1-0) timings apply only if Snoop Mode bit 0 of CTEST3 = 0.

Note: Shaded areas indicate that the signal is a don't care

Figure 7-16. Bus Mode 2 Bus Master Write (Cache-Line Burst)
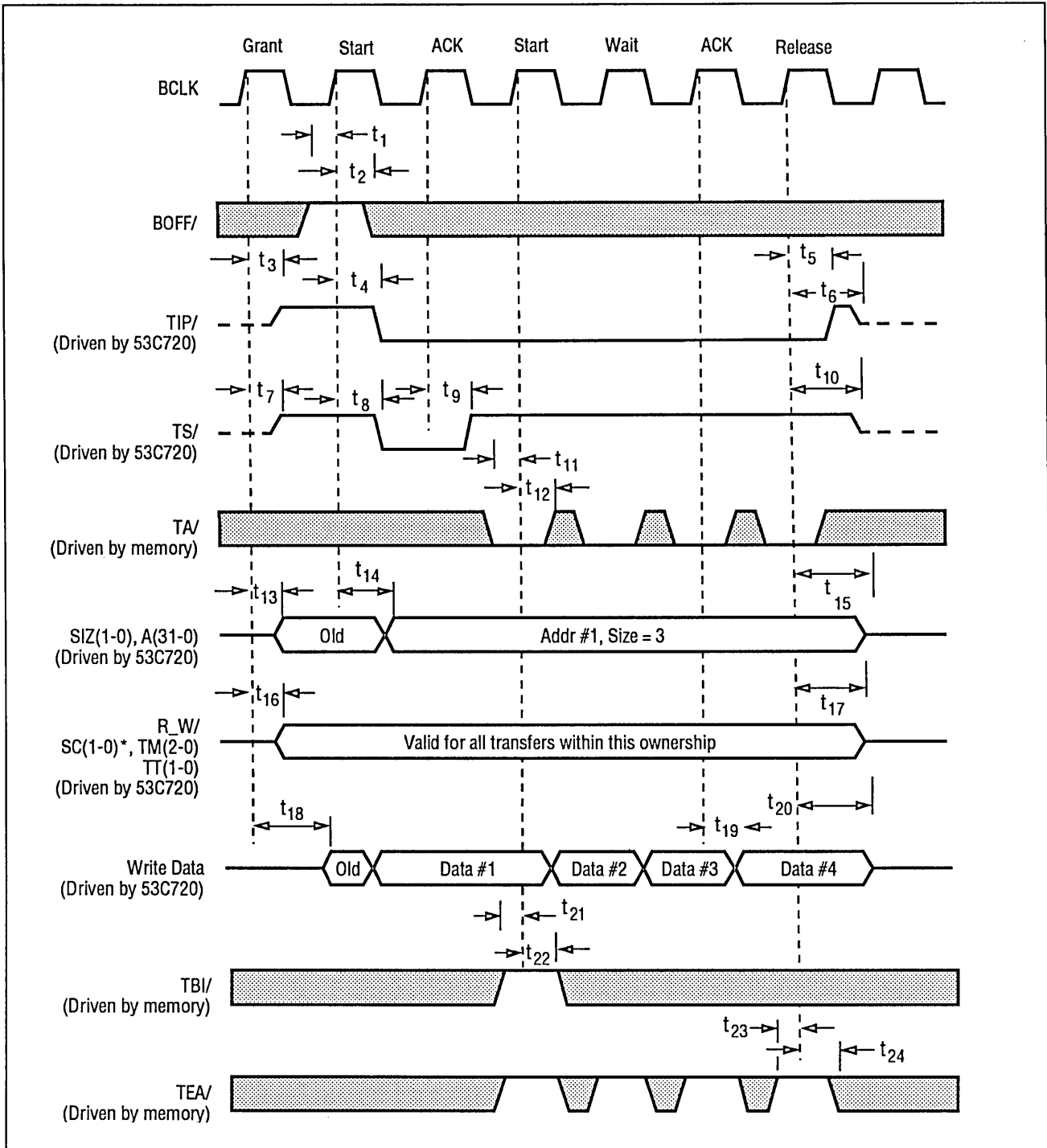
* SC (1-0) timings apply only if Snoop Mode bit 0 of CTEST3 = 0.

Note: Shaded areas indicate that the signal is a don't care

NCR 53C720

Bus Mode 3 and 4 Slave Cycle

Bus Mode 3 and 4 Slave Read Sequence

1) Address, Address Status and the Byte Enable signals are asserted by the CPU.

2) Chip Select is validated by the 53C720 on any following rising edge of BCLK.

3) Transfer Burst Inhibit is asserted.

4) Address Status may be deasserted by the CPU.

5) Three clock cycles of wait state are inserted and the Data lines are asserted.

6) Ready Out is asserted by the 53C720, if no errors are detected.

7) If a bus error is detected, only Transfer Error Acknowledge is asserted and the bus cycle ends on the next rising edge of BCLK.

8) Ready Out or Transfer Error Acknowledge is deasserted.

9) The 53C720 waits for Ready In to be asserted and then ends the slave cycle, if no errors are detected.

10) The Data lines are tristated by the 53C720.

Recommended Setup for Bus Mode 3 and 4

1) Disable Cache Line Mode (set CTEST0, bit 7).

2) Set the Bus Mode Bit (DCNTL, bit 6).

3) Set the Snoop Mode bit (CTEST3, bit 0)

4) Tie BB/ high resistively.

5) Tie TBI/ low resistively.

6) Tie TEA/ high resistively.

Parameter	Symbol	Min	Max	Units
ADS/ setup to BCLK high	t_1	4	-	ns
ADS/ hold from BCLK high	t_2	5	-	ns
CS/ setup to BCLK high after ADS/	t_3	5	-	ns
CS/ hold from BCLK high after ADS/	t_4	5	-	ns
BCLK high to TBI/ low	t_5	5	30	ns
BCLK high to TBI/ high- z	t_6	4	22	ns
BCLK high to READYO/, TEA/ low	t_7	5	22	ns
BCLK high to READYO/, TEA/ high	t_8	4	20	ns
READYI/ setup to BCLK high during or after READYO/, TEA/	t_9	8	-	ns
READYI/ hold from BCLK high during or after READYO/, TEA/	t_{10}	4	-	ns
BCLK high to data bus driven	t_{11}	5	28	ns
BCLK high to read data valid	t_{12}	-	75	ns
BCLK high to data bus high-Z	t_{13}	7	32	ns
A(6-0), SIZ(1-0), W_R/ setup to BCLK high	t_{14}	2	-	ns
A(6-0), SIZ(1-0), W_R/ hold from BCLK high	t_{15}	12	-	ns

Figure 7-17. Bus Mode 3 and 4 Slave Read Cycle

Note: Shaded areas indicate that the signal is a don't care.

*This signal may be driven by the 53C720 if the ENABLE ACK bit is set (DCNTL Bit 5). See explanation on page 3-10 for use of this signal as an output.

NCR 53C720

Bus Mode 3 and 4 Slave Write Sequence

1) W_R/, the address lines, and the Address Status and Byte Enable signals are asserted by the CPU.

2) Chip Select is validated by the 53C720 on any following rising edge of BCLK.

3) Transfer Burst Inhibit is asserted.

4) Address Status may be deasserted by the CPU.

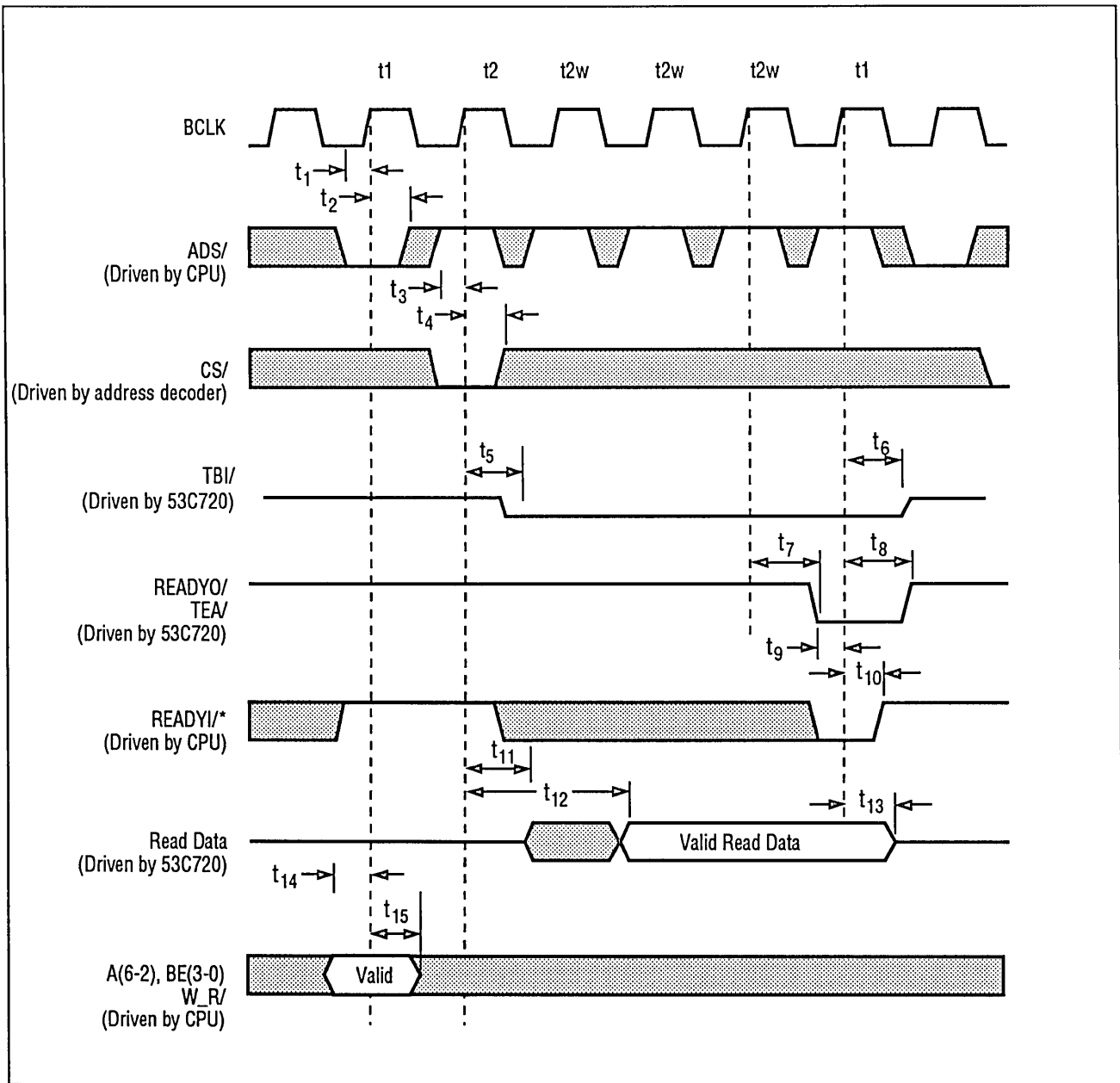5) The data lines are asserted by the CPU.

6) Three clock cycles of wait state are inserted (These wait states are required).

7) Ready Out is asserted by the 53C720, if no errors are detected

8) If a bus error is detected, only Transfer Error Acknowledge is asserted and the bus cycle ends on the next rising edge of BCLK.

9) Ready Out or Transfer Error Acknowledge is deasserted.

10) The 53C720 waits for Ready In to be asserted and then ends the slave cycle, if no error.

Parameter	Symbol	Min	Max	Units
TS/ setup to BCLK high	t_1	4	-	ns
ADS/ hold from BCLK high	t_2	5	-	ns
CS/ setup to BCLK high after ADS/	t_3	5	-	ns
CS/ hold from BCLK high after ADS/	t_4	5	-	ns
BCLK high to TBI/ low	t_5	5	30	ns
BCLK high to TBI/ high	t_6	4	22	ns
BCLK high to READYO/, TEA/ low	t_7	5	22	ns
BCLK high to READYO/, TEA/ high	t_8	4	20	ns
READYI/ setup to BCLK high during or after READYO/, TEA/	t_9	8	-	ns
READYI/ hold from BCLK high during or after READYO/, TEA/	t_{10}	4	-	ns
Valid write data setup to BCLK high	t_{11}	4	-	ns
Valid write data hold from BCLK high	t_{12}	6	-	ns
A(6-0), SIZ(1-0), W_R/ setup to BCLK high	t_{13}	2	-	ns
A(6-0), SIZ(1-0), W_R/ hold from BCLK high	t_{14}	12	-	ns

Figure 7-18. Bus Mode 3 and 4 Slave Write Cycle

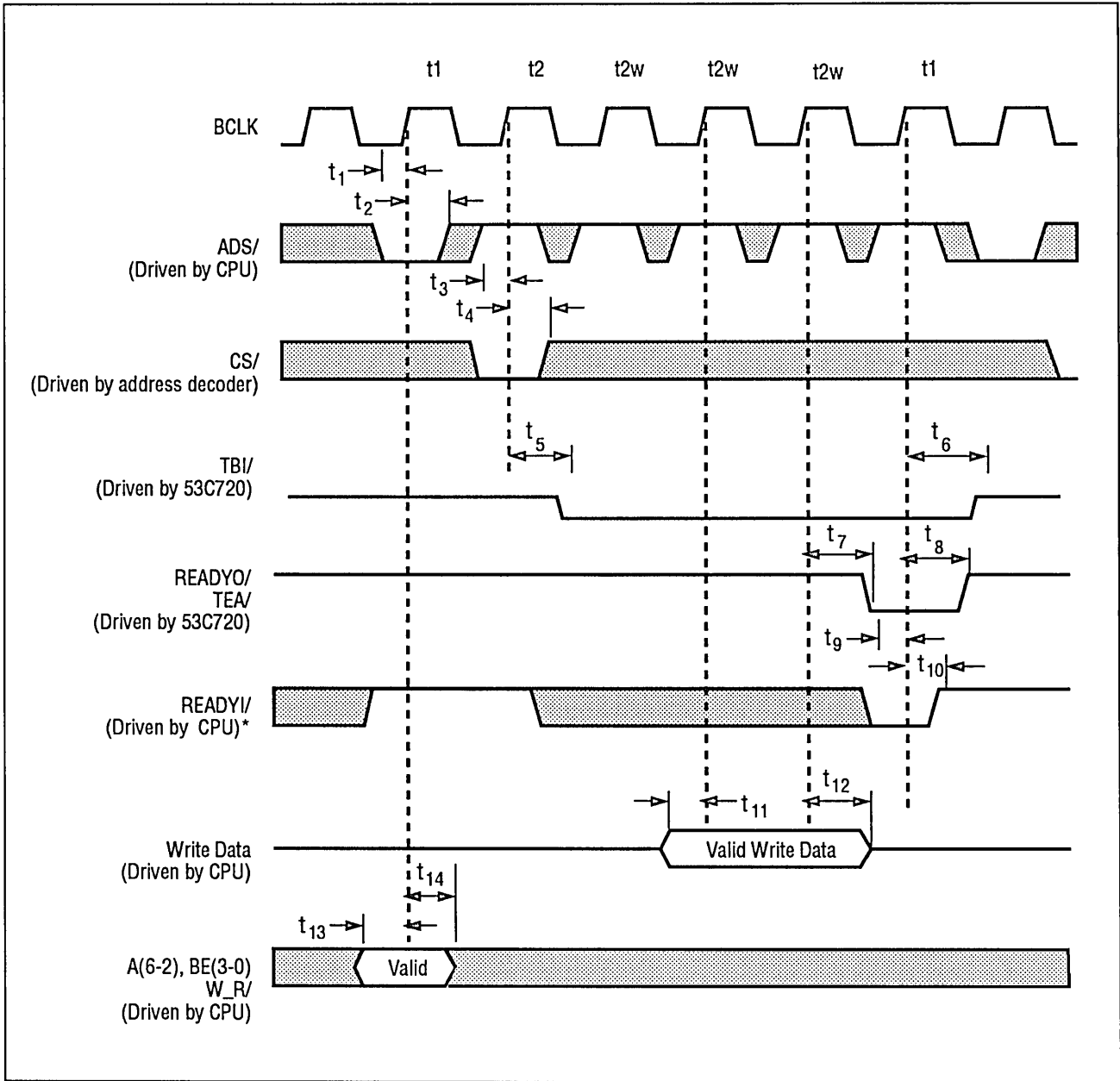Note: Shaded areas indicate that the signal is a don't care.

*This signal may be driven by the 53C720 if the Enable Acknowledge bit is set (DCNTL Bit 5). See explanation on page 3-10 for use of this signal as an output.

NCR 53C720

Host Bus Arbitration, Bus Mode 3 and 4

Bus Arbitration Sequence

1) The 53C720 internally determines bus mastership is required. If appropriate, FETCH/ is asserted.

2) Bus Request is asserted.

3) The 53C720 waits for Bus Grant and checks that bus Grant Acknowledge is deasserted. Then the 53C720 asserts Bus Grant Acknowledge and Master, and deasserts Bus Request.

Parameter	Symbol	Min	Max	Units
SC0 high to BR/ low*	t_1	1	2	BCLK
BCLK high to SC0 low on last cycle*	t_2	5	28	ns
BCLK high to BR/ low	t_3	4	20	ns
BCLK high to BR/ high	t_4	5	25	ns
BG/ setup to BCLK high (any rising edge after BR/)	t_5	4	-	ns
BG/ hold from BCLK high (any rising edge after BR/)	t_6	5	-	ns
BB/ setup to BCLK high (any rising edge after BR/)	t_7	4	-	ns
BCLK high to BB/ low	t_8	4	24	ns
BCLK high to BB/ high	t_9	3	19	ns
BCLK high to BB/ high-Z	t_{10}	7	32	ns
BCLK high to MASTER/ low	t_{11}	5	22	ns
BCLK high to MASTER/ high	t_{12}	6	26	ns
BCLK high to FETCH/ low	t_{13}	5	36	ns
BCLK high to FETCH/ high	t_{14}	5	36	ns
FETCH/ low to BR/ low	t_{15}	1	2	BCLK
BB/ high to FETCH/ high**	t_{16}	1	2	BCLK

*When Snoop Mode bit 0 of CTEST 3 is set to 1.

**During a retry operation, FETCH/ will remain low until a successful completion of the opcode fetch or a fatal bus error.

Figure 7-19. Host Bus Arbitration, Bus Mode 3 and 4
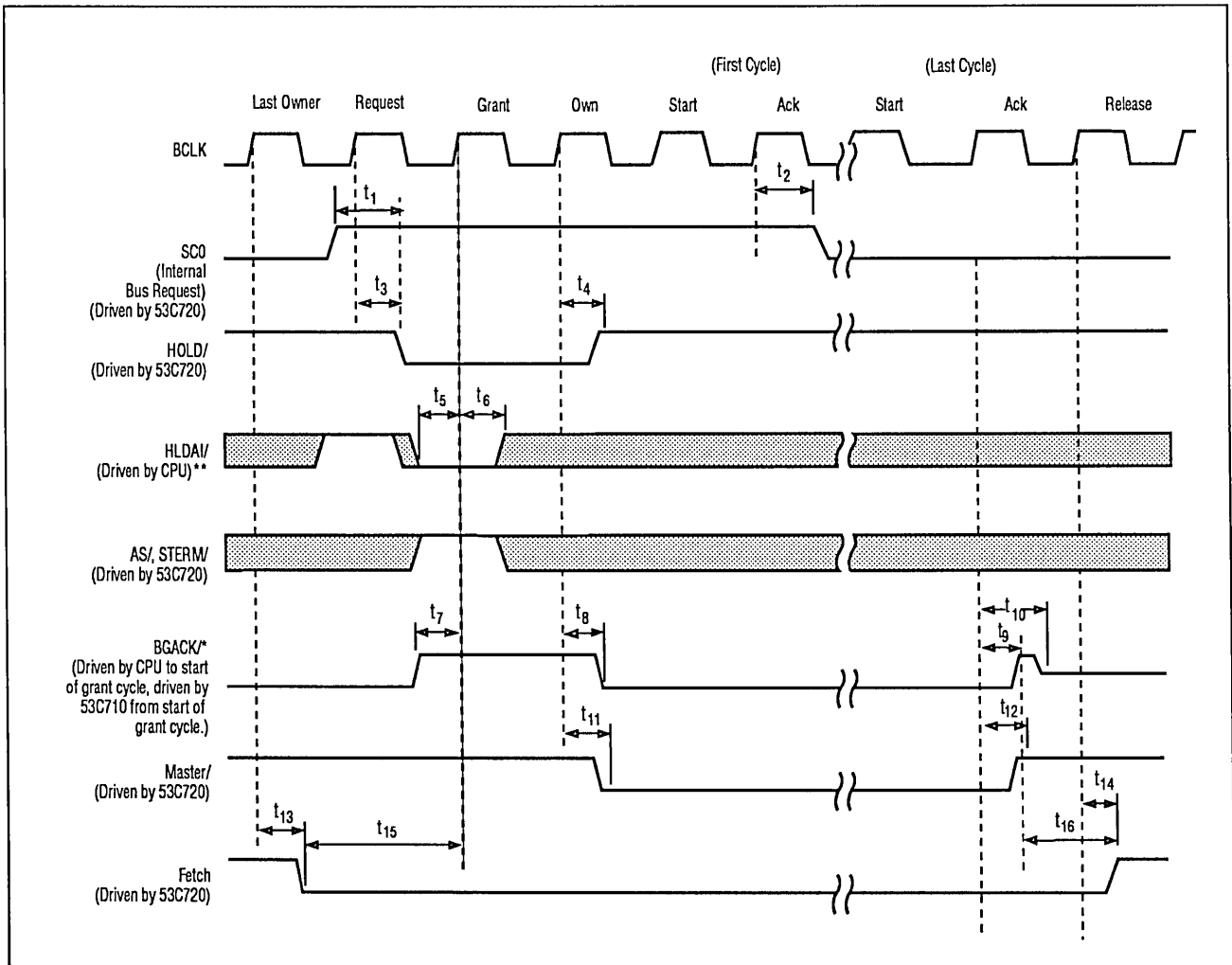
Note: shaded area indicates that the signal is a don't care.

*BB/ should be tied resistively if not used.

**HOLD/ may be NANDed with MASTER/ to obtain HOLD required by the 80286 or 80386 processors.

Bus Mode 3 and 4 Master Cycle

Bus Mode 3 and 4 Bus Master Read Sequence

1) The 53C720 has attained bus mastership.

2) The 53C720 asserts the W_R/, Transfer Modifier and Transfer Type lines.

3a) The 53C720 asserts Transfer in Progress .

3b) The 53C720 asserts Address Status, Address, and Byte Enable signals.

4) The 53C720 deasserts Address Status.

5) The 53C720 waits for Transfer Acknowledge, Valid Data, Transfer Burst Inhibit and Transfer Error Acknowledge.

- If Transfer Burst Inhibit is not asserted, attempt cache bursting.

- If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.

- If Transfer Error Acknowledge is asserted and Ready In is not asserted, a bus fault condition will be generated.

- If Ready In is asserted and Transfer Error Acknowledge is not asserted and the 53C720 requires more cycles, then return to step 3b.

6) Upon acknowledge of the last bus cycle, the 53C720 deasserts Master, Bus Busy, and Transfer in Progress.

7) The 53C720 floats the Control and Address lines.

Bus Mode 3 and 4 Bus Master Read (Non-Preview & Preview of Address)

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high*	t_2	26	-	ns
BCLK high to TIP/ driven	t_3	5	30	ns
BCLK high to TIP/ low	t_4	3	18	ns
BCLK high to TIP/ high	t_5	3	17	ns
BCLK high to TIP/ high-Z	t_6	7	32	ns
BCLK high to ADS/ driven	t_7	5	28	ns
BCLK high to ADS/ low	t_8	3	17	ns
BCLK high to ADS/ high	t_9	3	17	ns
BCLK high to ADS/ high-Z	t_{10}	7	32	ns
READYI/ setup to BCLK high	t_{11}	8	-	ns
READYI/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-2), SIZ(1-0) driven	t_{13}	5	28	ns
BCLK high to A(31-2), SIZ(1-0) valid	t_{14}	3	20	ns
BCLK high to A(31-2), SIZ(1-0) high-Z	t_{15}	7	32	ns
BCLK high to W_R/, TM(2-0), TT(1-0) driven and valid	t_{16}	5	28	ns
BCLK high to W_R/, TM(2-0), TT(1-0) high-Z	t_{17}	-	32	ns
Read Data setup to BCLK high	t_{18}	4	-	ns
Read Data hold from BCLK high	t_{19}	6	-	ns
PA/ setup to BCLK high	t_{20}	5	-	ns
PA/ hold from BCLK high	t_{21}	5	-	ns
TBI setup to BCLK high	t_{22}	6	-	ns
TBI hold from BCLK high	t_{23}	4	-	ns
TEA setup to BCLK high	t_{24}	6	-	ns
TEA hold from BCLK high	t_{25}	4	-	ns

*Only required during the cycle in which BOFF/ is recognized.

Figure 7-20. Bus Mode 3 and 4 Bus Master Read (Non-Preview of Address)
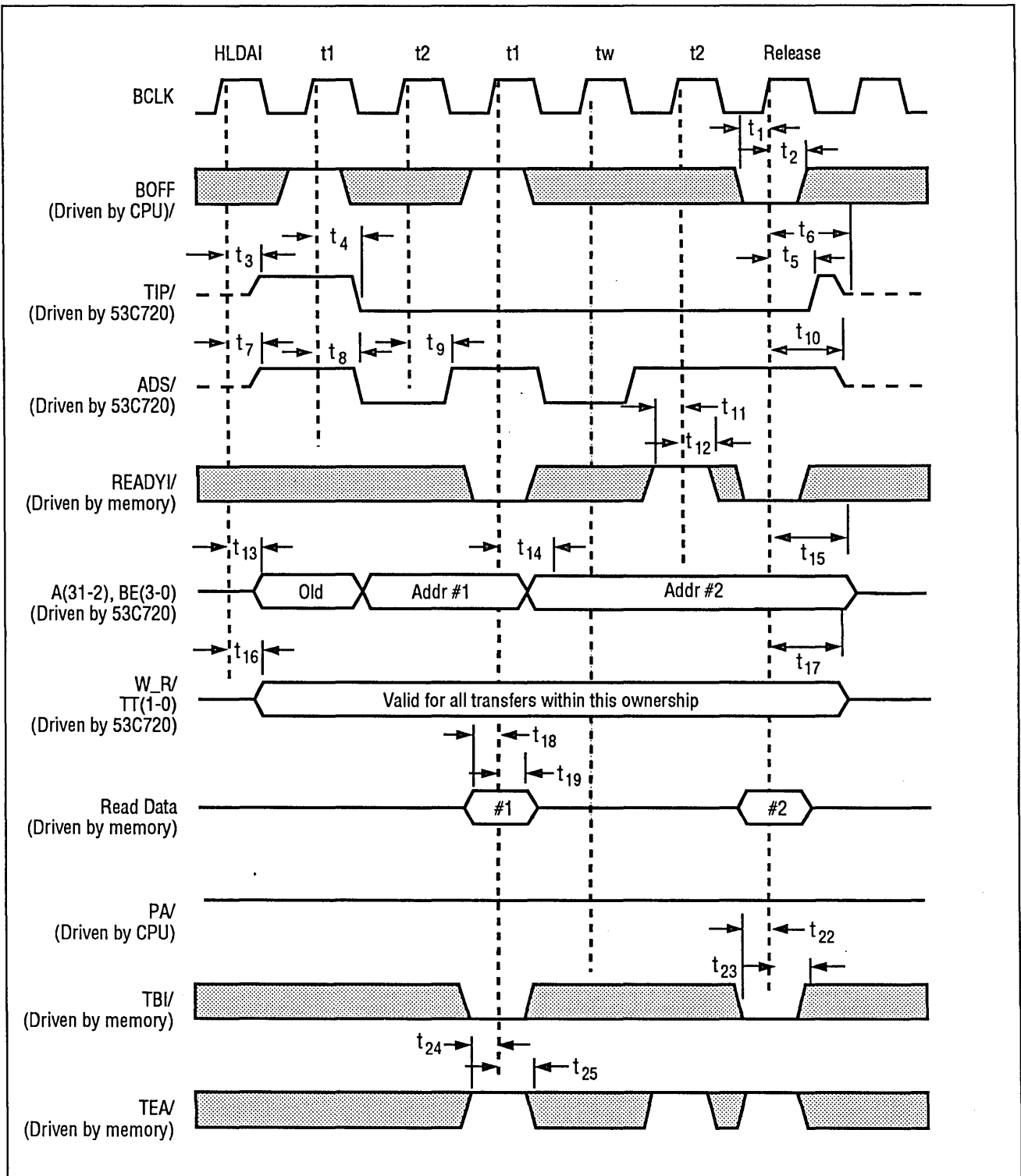
Note: Shaded areas indicate that the signal is a don't care

Figure 7-21. Bus Mode 3 and 4 Bus Master Read (Preview of Address)
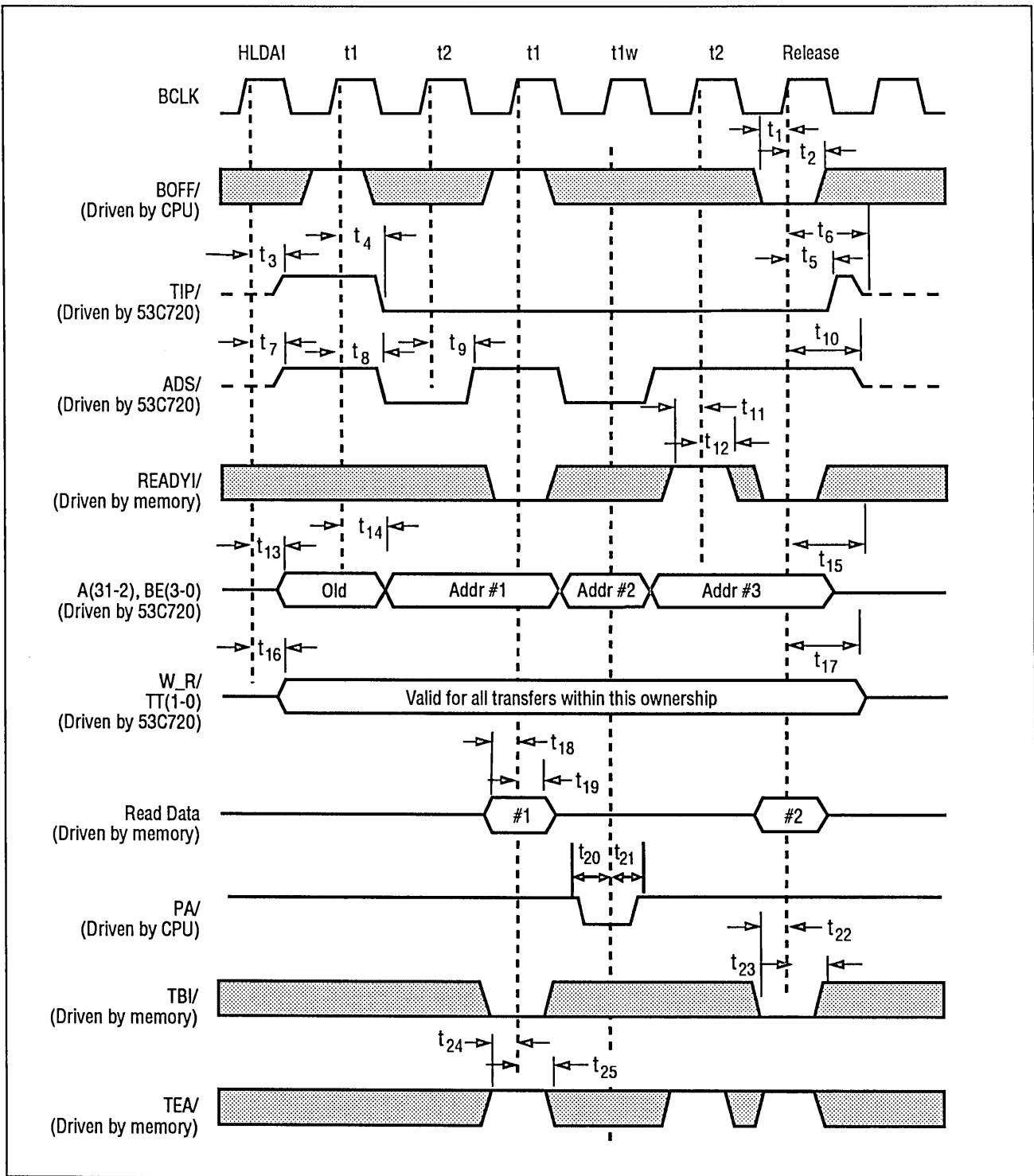
Note: Shaded areas indicate that the signal is a don't care

NCR 53C720

Bus Mode 3 and 4 Bus Master Write Sequence

1) The 53C720 has attained bus mastership.

2) The 53C720 asserts the W_R/, Transfer Modifier and Transfer Type lines.

3a) The 53C720 asserts Transfer in Progress.

3b) The 53C720 asserts Address Status, Address, Byte Enable signals and Data lines.

4) The 53C720 deasserts Address Status.

5) The 53C720 waits for Ready In, Transfer Burst Inhibit and Transfer Error Acknowledge.

   - If Transfer Burst Inhibit is not asserted, attempt cache bursting.

   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.

   - If Transfer Error Acknowledge is asserted and Ready In is not asserted, a bus fault condition will be generated.

   - If Ready In is asserted and Transfer Error Acknowledge is not asserted and the 53C720 requires more cycles, then return to step 3b.

6) Upon acknowledge of the last bus cycle, the 53C720 deasserts Master, Busy, and Transfer in Progress.

7) The 53C720 floats the Control, Address and Data lines.

Bus Mode 3 and 4 Bus Master Write Cycle (Non-Preview & Preview of Address)

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high*	t_2	26	-	ns
BCLK high to TIP/ driven	t_3	5	30	ns
BCLK high to TIP/ low	t_4	3	18	ns
BCLK high to TIP/ high	t_5	3	17	ns
BCLK high to TIP/ high-Z	t_6	7	32	ns
BCLK high to ADS/ driven	t_7	5	28	ns
BCLK high to ADS/ low	t_8	3	17	ns
BCLK high to ADS/ high	t_9	3	17	ns
BCLK high to ADS/ high-Z	t_{10}	7	32	ns
READYI/ setup to BCLK high	t_{11}	8	-	ns
READYI/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-2), SIZ(1-0) driven	t_{13}	5	28	ns
BCLK high to A(31-2), SIZ(1-0) valid	t_{14}	3	20	ns
BCLK high to A(31-2), SIZ(1-0) high-Z	t_{15}	7	32	ns
BCLK high to W_R/, TM(1-0), TT(1-0) driven and valid	t_{16}	5	28	ns
BCLK high to W_R/, TM(2-0), TT(1-0) high-Z	t_{17}	5	32	ns
BCLK high to Write Data driven	t_{18}	5	30	ns
BCLK high to Write Data valid	t_{19}	5	28	ns
BCLK high to Write Data high-Z	t_{20}	5	30	ns
PA/ setup to BCLK high	t_{21}	5	-	ns
PA/ hold from BCLK high	t_{22}	5	-	ns
TBI setup to BCLK high	t_{23}	6	-	ns
TBI hold from BCLK high	t_{24}	4	-	ns
TEA setup to BCLK high	t_{25}	6	-	ns
TEA hold from BCLK high	t_{26}	4	-	ns

*Only required during the cycle in which BOFF/ is recognized.

NCR 53C720

Figure 7-22. Bus Mode 3 and 4 Bus Master Write (Non-Preview of Address)
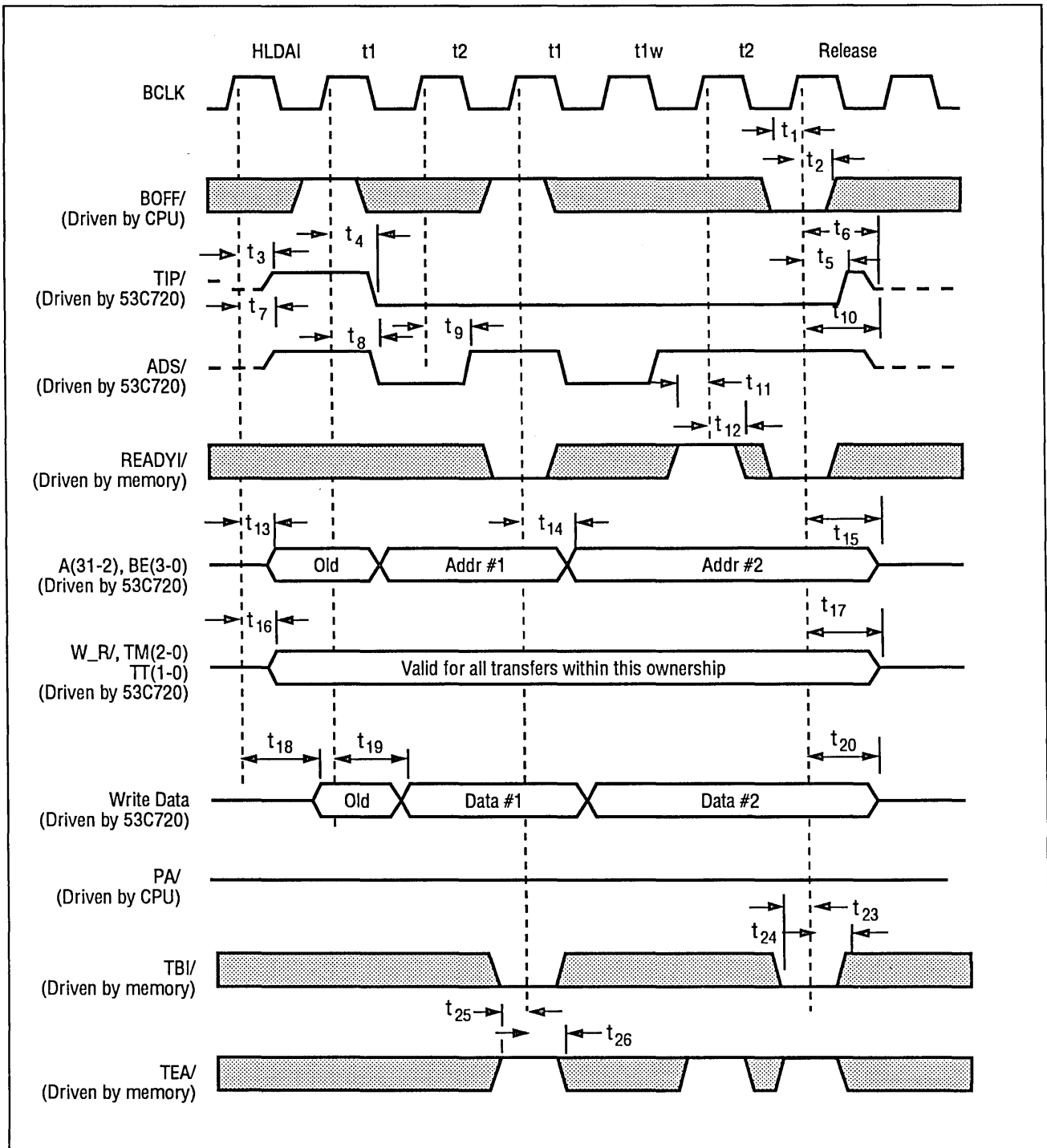
Note: Shaded areas indicate that the signal is a don't care

Figure 7-23. Bus Mode 3 and 4 Bus Master Write (Preview of Address)
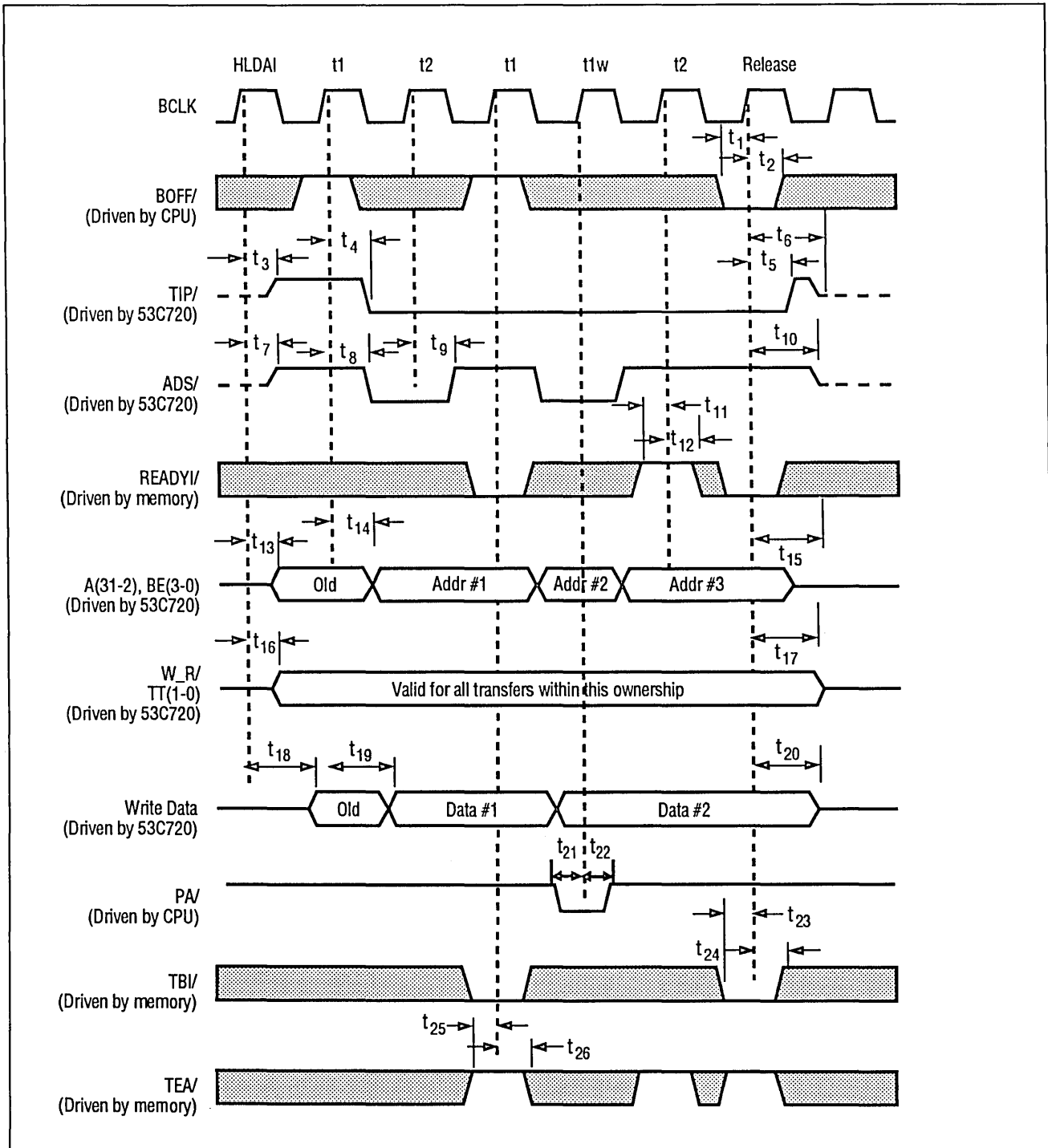
Note: Shaded areas indicate that the signal is a don't care

NCR 53C720

Figure 7-24. Initiator Asynchronous Send
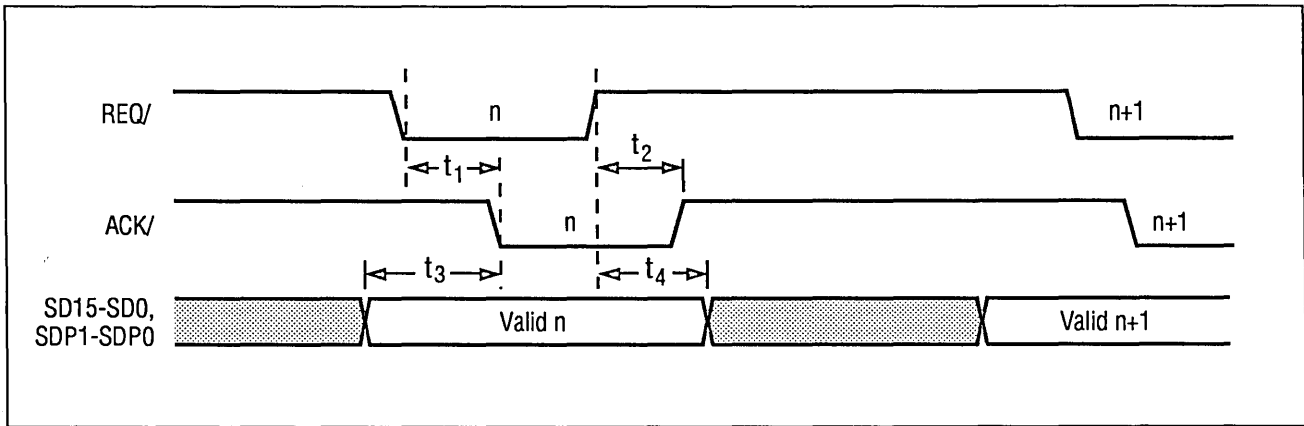
Parameter	Symbol	Min	Max	Units
ACK/ asserted from REQ/ asserted	t_1	10	-	ns
ACK/ deasserted from REQ/ deasserted	t_2	10	-	ns
Data setup to ACK/ asserted	t_3	55	-	ns
Data hold from REQ/ deasserted	t_4	20	-	ns

Figure 7-25. Initiator Asynchronous Receive
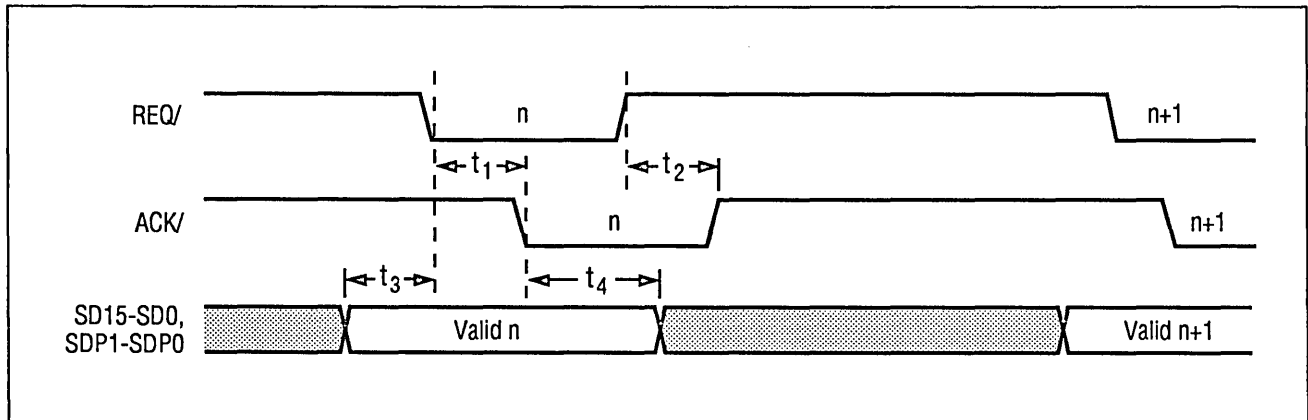
Parameter	Symbol	Min	Max	Units
ACK/ asserted from REQ/ asserted	t_1	10	-	ns
ACK/ deasserted from REQ/ deasserted	t_2	10	-	ns
Data setup to REQ/ asserted	t_3	0	-	ns
Data hold from ACK/ deasserted	t_4	0	-	ns

Figure 7-26. Target Asynchronous Send
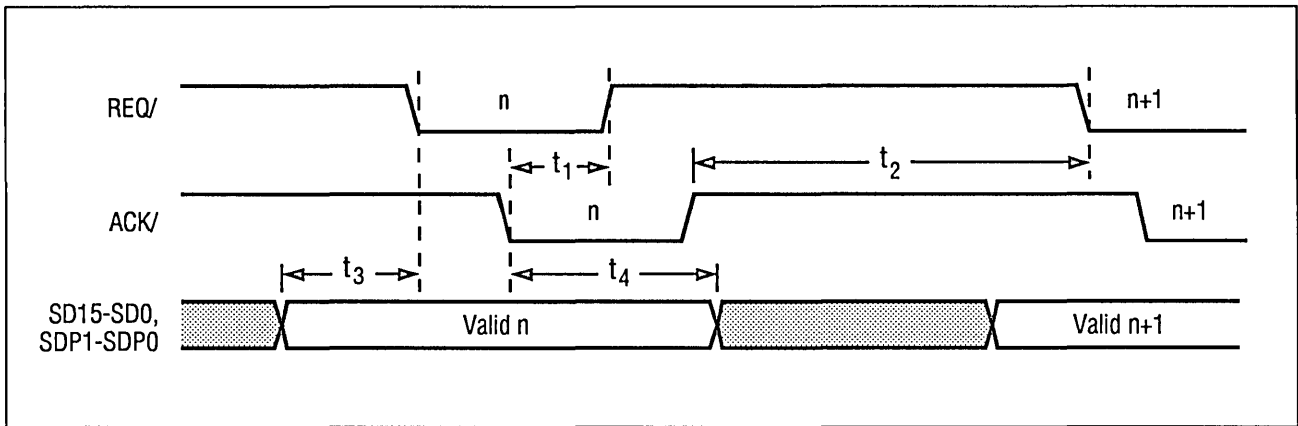
Parameter	Symbol	Min	Max	Units
REQ/ deasserted from ACK/ asserted	t_1	10	-	ns
REQ/ asserted from ACK/ deasserted	t_2	0	-	ns
Data setup to REQ/ asserted	t_3	55	-	ns
Data hold from ACK/ asserted	t_4	20	-	ns

Figure 7-27. Target Asynchronous Receive
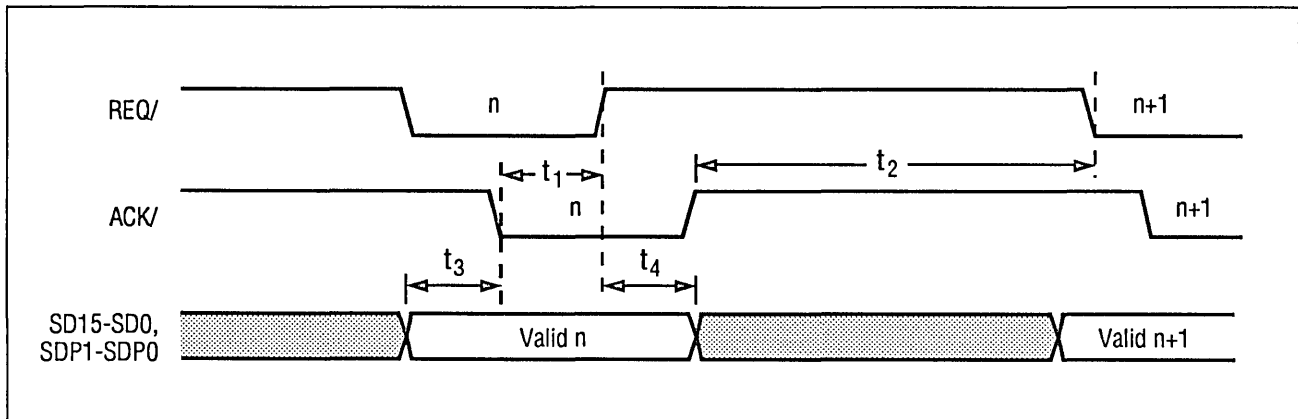
Parameter	Symbol	Min	Max	Units
REQ/ deasserted from ACK/ asserted	t_1	10	-	ns
REQ/ asserted from ACK/ deasserted	t_2	10	-	ns
Data setup to ACK/ asserted	t_3	0	-	ns
Data hold from REQ/ deasserted	t_4	0	-	ns

Figure 7-28. Initiator and Target Synchronous Transfers
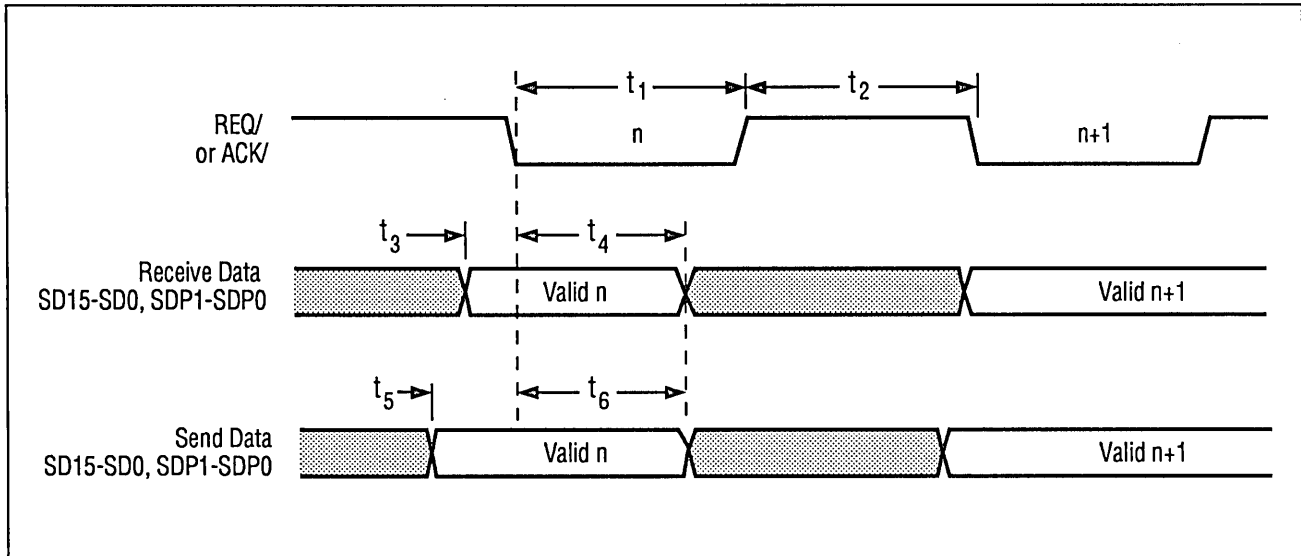
SCSI-1 Transfers

Parameter	Symbol	Min	Max	Units
REQ/ or ACK/ assertion pulse width	t_1	90	-	ns
REQ/ or ACK/ deassertion pulse width	t_2	90	-	ns
Receive data setup to REQ/ or ACK/ asserted	t_3	0	-	ns
Receive data hold from REQ/ or ACK/ asserted	t_4	45	-	ns
Send data setup to REQ/ or ACK/ asserted	t_5	65	-	ns
Send data hold from REQ/ or ACK/ asserted	t_6	110	-	ns

SCSI-2 Fast Transfers

Parameter	Symbol	Min	Max	Units
REQ/ or ACK/ assertion pulse width	t_1	36	-	ns
REQ/ or ACK/ deassertion pulse width	t_2	36	-	ns
Receive data setup to REQ/ or ACK/ asserted	t_3	0	-	ns
Receive data hold from REQ/ or ACK/ asserted	t_4	10	-	ns
Send data setup to REQ/ or ACK/ asserted	t_5	35	-	ns
Send data hold from REQ/ or ACK/ asserted	t_6	45	-	ns

Appendix A

53C720 Register Summary

(*Default values for each bit are shown in the shaded areas.*)

SCNTL0 Register R/W (00h)
```
7  6  5  4  3  2  1  0
1  1  0  0  0  0  0  0
```
- Target Mode
- Assert ATN/ on Parity Error
- Enable Parity Generation
- Enable Parity Checking
- Select with ATN/
- Start Sequence
- Arbitration Mode bit 0
- Arbitration Mode bit 1

SCNTL1 Register R/W (01h)
```
7  6  5  4  3  2  1  0
0  0  0  0  0  0  0  0
```
- Start SCSI Transfer
- Immediate Arbitration
- Assert Even SCSI Parity
- Assert SCSI RST/
- Connected
- Disable Halt on Parity Error or ATN Condition
- Assert contents of SODL on SCSI bus
- Extra Clock Cycle of Data Setup

SCNTL2 Register R/W (02h)
```
7  6  5  4  3  2  1  0
0  0  X  X  0  X  X  0
```
- Wide SCSI Receive
- Reserved
- Reserved
- Wide SCSI Send
- Reserved
- Reserved
- Chained Mode
- SCSI Disconnect Unexpected

SCNTL3 Register R/W 03
```
7  6  5  4  3  2  1  0
X  0  0  0  0  0  0  0
```
- Clock Conversion Factor
- Clock Conversion Factor
- Clock Conversion Factor
- Enable Wide SCSI
- Synchronous Clock Conversion Factor bit 0
- Synchonous Clock Conversion Factor bit 1
- Synchronous Clock Conversion Factor bit 2
- Reserved

SCID Register R/W (04h)
```
7  6  5  4  3  2  1  0
X  0  0  X  0  0  0  0
```
- Encoded Chip ID 0
- Encoded Chip ID 1
- Encoded Chip ID 2
- Encoded Chip ID 3
- Reserved
- Enable Response to Selection
- Enable Response to Reselection
- Reserved

SXFER Register R/W (05h)
```
7  6  5  4  3  2  1  0
0  0  0  X  0  0  0  0
```
- Max SCSI Synchronous Offset 0
- Max SCSI Synchronous Offset 1
- Max SCSI Synchronous Offset 2
- Max SCSI Synchronous Offset 3
- Reserved
- Synchronous Transfer Period bit 0
- Synchronous Transfer Period bit 1
- Synchronous Transfer Period bit 2

SDID Register R/W (06h)
```
7  6  5  4  3  2  1  0
X  X  X  X  0  0  0  0
```
- Encoded Destination ID 0
- Encoded Destination ID 1
- Encoded Destination ID 2
- Encoded Destination ID 3
- Reserved
- Reserved
- Reserved
- Reserved

GPREG Register R/W (07h)
```
7  6  5  4  3  2  1  0
X  X  X  0  X  X  X  X
```
- General Purpose Input 0
- General Purpose Input 1
- General Purpose Input 2
- General Purpose Input 3
- General Purpose Output 0
- Reserved
- Reserved
- Reserved

NCR 53C720

53C720 Register Summary (Continued)

SFBR Register R (08h)

```
 7  6  5  4  3  2  1  0
[0][0][0][0][0][0][0][0]
                      └ 1B0
                   └ 1B1
                └ 1B2
             └ 1B3
          └ 1B4
       └ 1B5
    └ 1B6
 └ 1B7
```

SOCL Register W (09h)

```
 7  6  5  4  3  2  1  0
[0][0][0][0][0][0][0][0]
                      └ I/O
                   └ C/D
                └ MSG/
             └ ATN/
          └ SEL/
       └ BSY/       1 = Active
    └ ACK/          0 = Inactive
 └ REQ/
```

SSID Register R (0Ah)

```
 7  6  5  4  3  2  1  0
[0][X][X][X][0][0][0][0]
                      └ Encoded Destination SCSI ID bit 0
                   └ Encoded Destination SCSI ID bit 1
                └ Encoded Destination SCSI ID bit 2
             └ Encoded Destination SCSI ID bit 3
          └ Reserved
       └ Reserved
    └ Reserved
 └ SCSI Selector ID Valid
```

SBCL Register R (0Bh)

```
 7  6  5  4  3  2  1  0
[X][X][X][X][X][X][X][X]
                      └ I/O
                   └ C/D
                └ MSG/
             └ ATN/
          └ SEL/
       └ BSY/
    └ ACK/       1 = Active
 └ REQ/          0 = Inactive
```

DSTAT Register R (0Ch)

```
 7  6  5  4  3  2  1  0
[1][0][0][0][0][0][0][0]
                      └ Illegal Instruction Detected
                   └ Watchdog Timeout Interrupt Detected
                └ Script Interrupt Instruction Received
             └ Script Single Step Interrupt
          └ Abort Interrupt
       └ Bus Fault Interrupt
    └ Host Parity Error
 └ DMA FIFO Empty
```

SSTAT0 Register R (0Dh)

```
 7  6  5  4  3  2  1  0
[0][0][0][0][0][0][0][0]
                      └ Status of SCSI Parity Signal
                   └ Status of SCSI RST/
                └ Won Arbitration
             └ Lost Arbitration
          └ Arbitration In Progress
       └ SODL Least Significant Byte Full
    └ SODR Least Significant Byte Full
 └ SIDL Least Significant Byte Full
```

SSTAT1 Register R (0Eh)

```
 7  6  5  4  3  2  1  0
[0][0][0][0][X][X][X][X]
                      └ Latched I/O signal
                   └ Latched C/D signal
                └ Latched MSG/ signal
             └ Latched SCSI Parity signal
          └ FIFO Flags bit 0
       └ FIFO Flags bit 1
    └ FIFO Flags bit 2
 └ FIFO Flags bit 3
```

SSTAT2 Register R (0Fh)

```
 7  6  5  4  3  2  1  0
[0][0][0][X][X][X][1][X]
                      └ SCSI SDP1 signal
                   └ Last Disconnect
                └ Reserved
             └ Latched SCSI Parity SD 15-8
          └ Reserved
       └ SODL Most Significant Byte Full
    └ SODR Most Significant Byte Full
 └ SIDL Most Significant Byte Full
```

53C720 Register Summary (Continued)

DSA Register R/W (10-13h)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X

ISTAT Register R/W (14h)

7 6 5 4 3 2 1 0
0 0 0 0 0 0 0 0
- DMA Interrupt Pending
- SCSI Interrupt Pending
- Interrupt on the Fly
- Connected/Disconnect
- Semaphore
- Signal Process
- Software Reset
- Abort Operation

CTEST0 Register R/W (18h)

7 6 5 4 3 2 1 0
0 0 0 X 0 0 0 X
- Reserved
- Transfer Type bit 1
- Even Parity
- DMA FIFO Parity
- Reserved
- Snoop Control 0
- Snoop Control 1
- Cache Burst Disable

CTEST1 Register R (19h)

7 6 5 4 3 2 1 0
0 0 0 0 0 0 0 0
- Byte Lane 0 Full in DMA FIFO
- Byte Lane 1 Full in DMA FIFO
- Byte Lane 2 Full in DMA FIFO
- Byte Lane 3 Full in DMA FIFO
- Byte Lane 0 Empty in DMA FIFO
- Byte Lane 1 Empty in DMA FIFO
- Byte Lane 2 Empty in DMA FIFO
- Byte Lane 3 Empty in DMA FIFO

CTEST2 Register R (1Ah)

7 6 5 4 3 2 1 0
0 0 X X 0 0 0 0
- DACK/ Status
- DREQ Status
- SCSI TEOP Status
- DMA FIFO Parity bit
- Reserved
- Reserved
- Signal Process
- Data Transfer Direction

CTEST3 Register R (1Bh)

7 6 5 4 3 2 1 0
X X X X 0 0 0 0
- Snoop Pin
- Fetch Pin
- Clear DMA SCSI FIFOs
- Flush FIFO
- Chip Version
- Chip Version
- Chip Version
- Chip Version

TEMP Register R/W (1C-1Fh)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X X

DFIFO Register R/W (20h)

7 6 5 4 3 2 1 0
X 0 0 0 0 0 0 0
- FIFO Byte Offsetr Counter bit 0
- FIFO Byte Offset Counter bit 1
- FIFO Byte Offset Counter bit 2
- FIFO Byte Offset Counter bit 3
- FIFO Byte Offset Counter bit 4
- FIFO Byte Offset Counter bit 5
- FIFO Byte Offset Counter bit 6
- Reserved

CTEST4 Register R/W (21h)

7 6 5 4 3 2 1 0
0 0 0 0 0 0 0 0
- FIFO Byte Control bit 0
- FIFO Byte Control bit 1
- FIFO Byte Control bit 2
- Host Parity Check Enable
- Shadow Register Test Mode
- SCSI Z-Mode
- Z-Mode
- Host Bus Multiplex

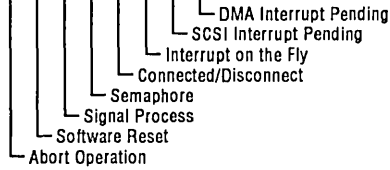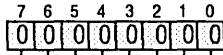## 53C720 Register Summary (Continued)

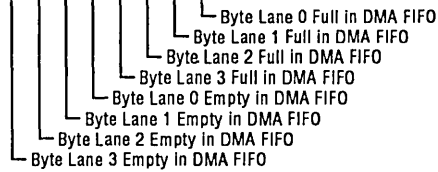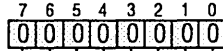**CTEST5 Register R/W (22h)**

```
 7  6  5  4  3  2  1  0
| 0| 0| X| 0| 0| 0| X| X| X|
```
— Reserved
— Reserved
— Reserved
— DMA Direction
— Master Control for Set or Reset Pulses
— Reserved
— Clock Byte Counter (DBC)
— Clock Address Incrementor (DNAD)

CTEST6 Register R/W (23h)

```
 7  6  5  4  3  2  1  0
| 0| 0| 0| 0| 0| 0| 0| 0|
```
— DMA FIFO bit 0
— DMA FIFO bit 1
— DMA FIFO bit 2
— DMA FIFO bit 3
— DMA FIFO bit 4
— DMA FIFO bit 5
— DMA FIFO bit 6
— DMA FIFO bit 7

DBC Register R/W (24-26h)

```
23 22 21 20 19 18 17 16 15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X|
```

DCMD Register R/W (27h)

```
 7  6  5  4  3  2  1  0
| 0| 0| 0| 0| 0| 0| 0| 0|
```
— Function bit 0
— Function bit 1
— Function bit 2
— Function bit 3
— Function bit 4
— Function bit 5
— Instruction Op Code bit 0
— Instruction Op Code bit 1

DNAD Register R/W (28-2Bh)

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0|
```

DSP Register R/W (2C-2Fh)

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0| 0|
```

DSPS Register R/W (30-33h)

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X|
```

SCRATCHA Register R/W (34-37h)

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X| X|
```

53C720 Register Summary (Continued)

DMODE Register R/W (38h)

```
 7  6  5  4  3  2  1  0
[0][0][0][0][0][0][0][0]
```
└─ Manual Start Mode
└─ User Programmable Transfer
└─ Fixed Address Mode
└─ Program Data
└─ Function Code bit 1
└─ Function Code bit 2
└─ Burst Length bit 0
└─ Burst Length bit 1

DIEN Register R/W (39h)

```
 7  6  5  4  3  2  1  0
[X][0][0][0][0][0][0][0]
```
└─ Enable Illegal Instruction Interrupt
└─ Enable Watchdog Time-Out Interrupt
└─ Enable Script Interrupt Instruction Received Interrupt
└─ Enable Script Step Interrupt
└─ Enable Aborted Interrupt
└─ Enable Bus Fault Interrupt
└─ Host Parity Error Detected
└─ Reserved

DWT Register R/W (3Ah)

```
 7  6  5  4  3  2  1  0
[0][0][0][0][0][0][0][0]
```
└─ DWT0
└─ DWT1
└─ DWT2
└─ DWT3
└─ DWT4
└─ DWT5
└─ DWT6
└─ DWT7

DCNTL Register R/W (3Bh)

```
 7  6  5  4  3  2  1  0
[0][0][0][0][0][0][0][0]
```
└─ 53C700 Compatibility Bit
└─ Fast ARB
└─ Start DMA Operation
└─ Host Bus Width Equal to 16
└─ Single Step Mode
└─ Enable ACK
└─ Bus Mode
└─ Reserved

ADDER Register R (3C-3Fh)

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
[X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X]
```

SIEN0 Register R/W (40h)

```
 7  6  5  4  3  2  1  0
[0][0][0][0][0][0][0][0]
```
└─ Parity Error Received
└─ SCSI RST/ Received
└─ Unexpected Disconnect
└─ SCSI Gross Error
└─ Reselected
└─ Selected
└─ Function Complete
└─ Phase Mismatch or ATN/ Active

SIEN1 Register R/W (41h)

```
 7  6  5  4  3  2  1  0
[X][X][X][X][X][0][0][0]
```
└─ Handshake-to-HandshakeTimer Expired
└─ General Purpose Timer Expired
└─ Selection or Reselection Time-Out
└─ Reserved
└─ Reserved
└─ Reserved
└─ Reserved
└─ Reserved

NCR 53C720

53C720 Register Summary (Continued)

SIST0 Register R (42h)
```
7  6  5  4  3  2  1  0
0  0  0  0  0  0  0  0
```
- Parity Error Received
- SCSI RST/ received
- Unexpected Disconnect
- SCSI Gross Error
- Reselected
- Selected
- Function Complete
- Phase Mismatch or ATN/ Active

SIST1 Register R (43h)
```
7  6  5  4  3  2  1  0
X  X  X  X  X  0  0  0
```
- Handshake-to-Handshake Timer Expired
- General Purpose Timer Expired
- Selection/Reselection Time-Out
- Reserved
- Reserved
- Reserved
- Reserved
- Reserved

SLPAR Register R/W (44h)
```
7  6  5  4  3  2  1  0
0  0  0  0  0  0  0  0
```
- SCSI Longitudinal Parity
- SCSI Longitudinal Parity
- SCSI Longitudinal Parity
- SCSI Longitudinal Parity
- SCSI Longitudinal Parity
- SCSI Longitudinal Parity
- SCSI Longitudinal Parity
- SCSI Longitudinal Parity

SWIDE Register R (45h)
```
7  6  5  4  3  2  1  0
X  X  X  X  X  X  X  X
```
- SRD8
- SRD9
- SRD10
- SRD11
- SRD12
- SRD13
- SRD14
- SRD15

STIME0 Register R/W (48h)
```
7  6  5  4  3  2  1  0
0  0  0  0  0  0  0  0
```
- Selection Time-Out Period bit 0
- Selection Time-Out Period bit 1
- Selection Time-Out Period bit 2
- Selection Time-Out Period bit 3
- Handshake-to-Handshake Timer Period bit 0
- Handshake-to-Handshake Timer Period bit 1
- Handshake-to-Handshake Timer Period bit 2
- Handshake-to-Handshake Timer Period bit 3

STIME1 Register R/W (49h)
```
7  6  5  4  3  2  1  0
X  X  X  X  0  0  0  0
```
- General Purpose Timer Period bit 0
- General Purpose Timer Period bit 1
- General Purpose Timer Period bit 2
- General Purpose Timer Period bit 3
- Reserved
- Reserved
- Reserved
- Reserved

STEST0 Register R (4Ch)
```
7  6  5  4  3  2  1  0
X  X  X  X  0  X  1  1
```
- SCSI Synchronous Offset Maximum
- SCSI Synchronous Offset Zero
- Arbitration Priority Encoder Test
- Selection Response Logic Test
- Reserved
- Reserved
- Reserved
- Reserved

STEST1 Register R (4Dh)
```
7  6  5  4  3  2  1  0
X  X  X  X  X  X  X  X
```
- SCSI FIFO Parity bit 0
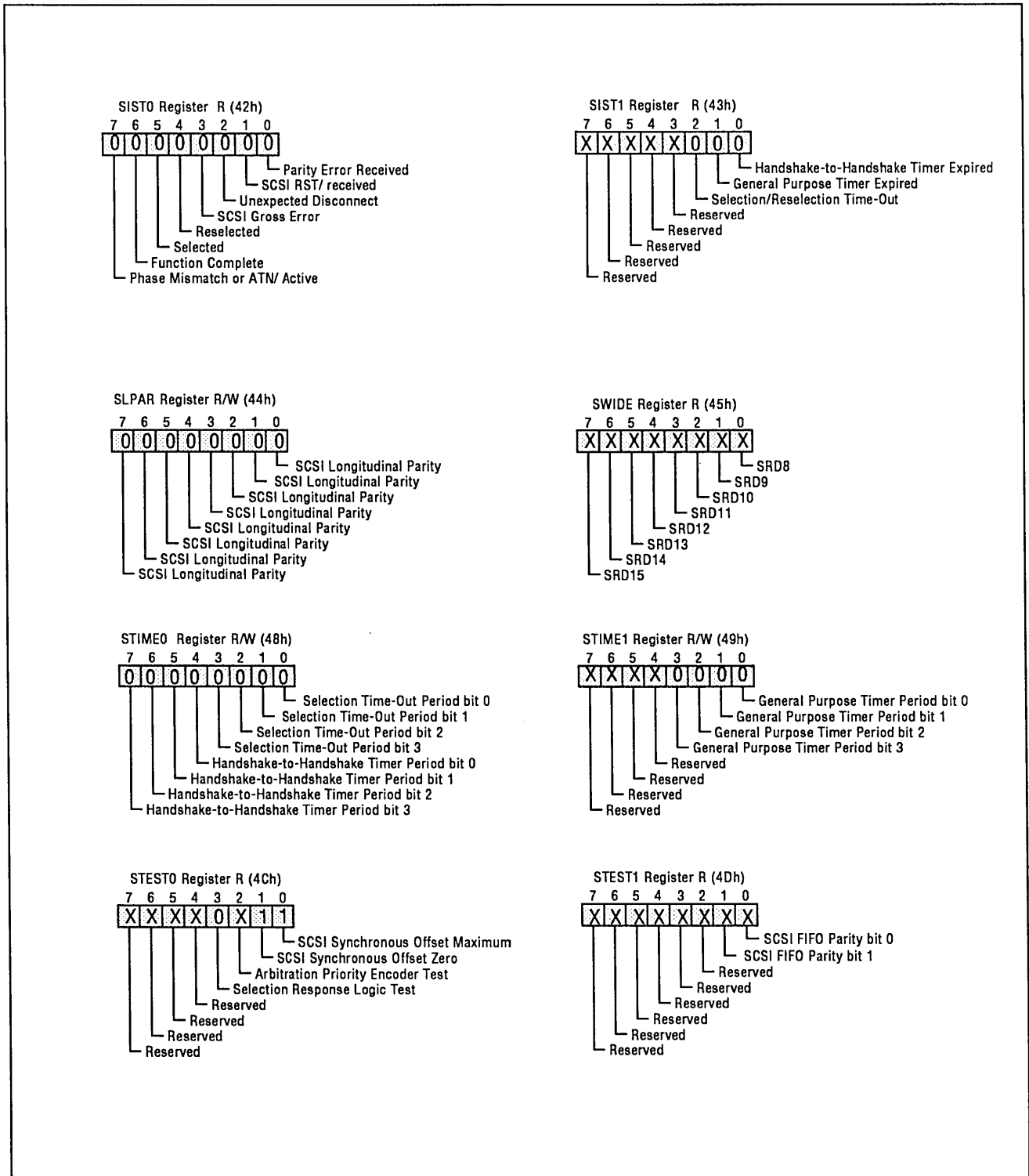- SCSI FIFO Parity bit 1
- Reserved
- Reserved
- Reserved
- Reserved
- Reserved
- Reserved

53C720 Register Summary (Continued)

STEST2 Register R/W (4Eh)

7 6 5 4 3 2 1 0

| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

— SCSI Low-Level Mode
— Extend Req/Ack filtering
— Always Wide SCSI
— SCSI High Impedance Mode
— SCSI Loopback Mode
— SCSI Differential Mode
— Reset SCSI Offset
— SCSI Control Enable

STEST3 Register R/W (4Fh)

7 6 5 4 3 2 1 0

| X | X | 0 | 0 | 0 | 0 | 0 | 0 |

— SCSI FIFO Test Mode
— Clear SCSI FIFO
— Timer Test Mode
— 16-bit System
— Disable Single Initiator Response
— Halt SCSI Clock
— Reserved
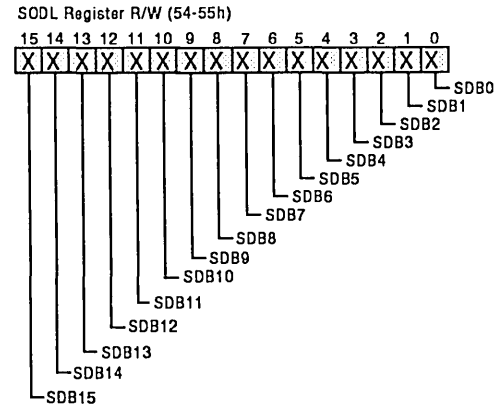— Reserved

SIDL Register R (50-51h)

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |

— SDB0
— SDB1
— SDB2
— SDB3
— SDB4
— SDB5
— SDB6
— SDB7
— SDB8
— SDB9
— SDB10
— SDB11
— SDB12
— SDB13
— SDB14
— SDB15

SODL Register R/W (54-55h)

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |

— SDB0
— SDB1
— SDB2
— SDB3
— SDB4
— SDB5
— SDB6
— SDB7
— SDB8
— SDB9
— SDB10
— SDB11
— SDB12
— SDB13
— SDB14
— SDB15

SBDL Register R (58-59h)

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |

— SDB0
— SDB1
— SDB2
— SDB3
— SDB4
— SDB5
— SDB6
— SDB7
— SDB8
— SDB9
— SDB10
— SDB11
— SDB12
— SDB13
— SDB14
— SDB15

SCRATCHB Register R/W (5C-5Fh)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

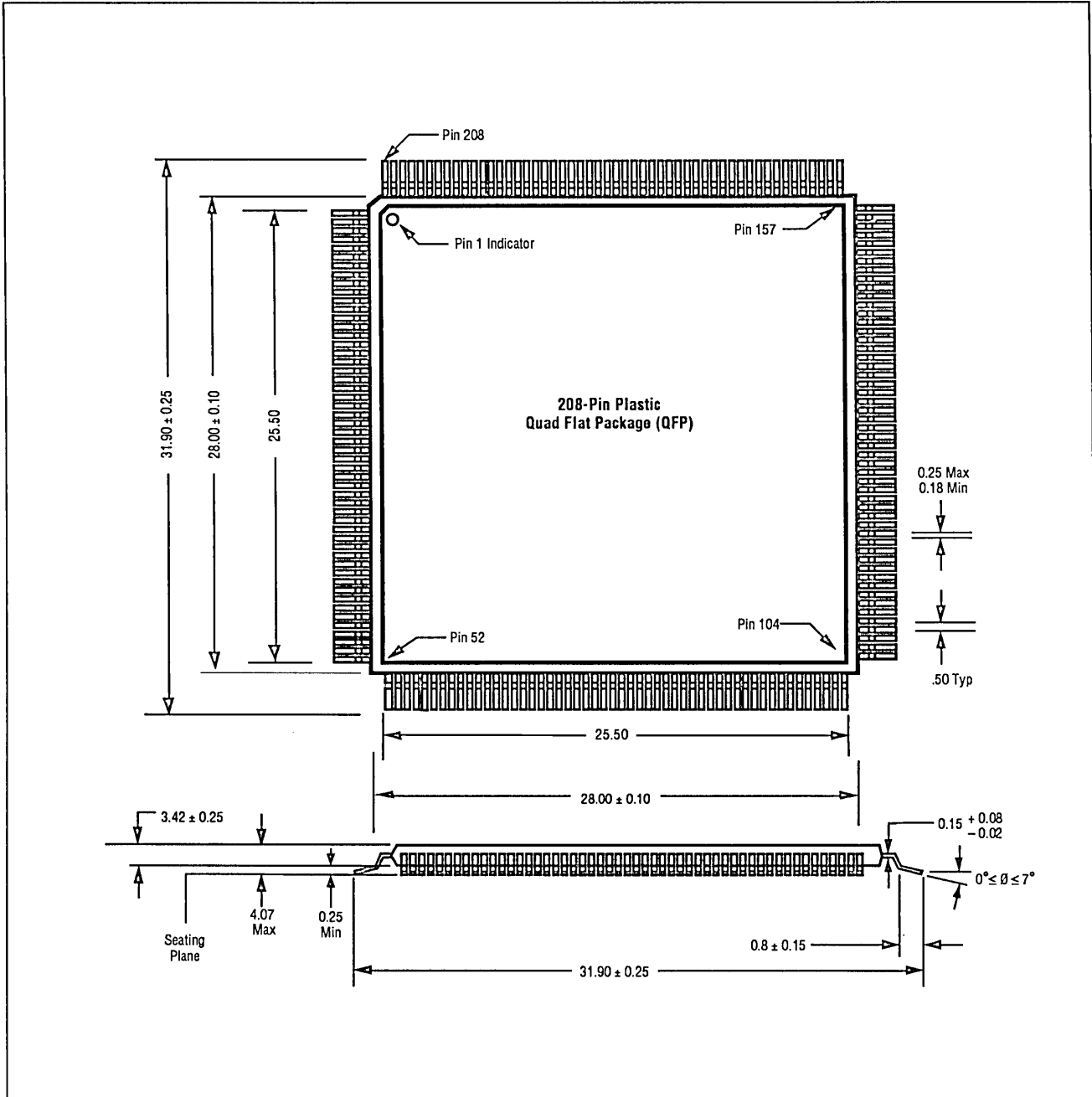| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |

Appendix B

Mechanical Data

Note: All dimensions are in millimeters. This package is known as a
Metric QFP, and should not be confused with the similiar JEDEC QFP.

Appendix C

Register Differences Between the 53C710 and 53C720

New Registers/Bits

Registers/Bits	53C710	53C720
Start SCSI Transfer bit	Not Supported	SCNTL1, bit 0
Immediate Arbitration bit	Not Supported	SCNTL1, bit 1
SCSI Control Register Two — 02h	Not Supported	SCNTL2
Wide SCSI Receive bit	Not Supported	SCNTL2, bit 0
Wide SCSI Send bit	Not Supported	SCNTL2, bit 3
Chained Mode bit	Not Supported	SCNTL2, bit 6
SCSI Disconnect Unexpected bit	Not Supported	SCNTL2, bit 7
SCSI Control Register Three — 03h	Not Supported	SCNTL3
Enable Wide SCSI bit	Not Supported	SCNTL3, bit 3
Enable Response to Selection bit	Not Supported	SCID, bit 5
Enable Response to Reselection bit	Not Supported	SCID, bit 6
General Purpose Register — 07h	Not Supported	GPREG
General Purpose Input bits	Not Supported	GPREG, bits 3-0
General Purpose Output bit	Not Supported	GPREG, bit 4
SCSI Selector ID Register — 0Ah	Not Supported	SSID
Encoded Destination SCSI ID Bits	Not Supported	SSID, bits 3-0
SCSI Selector ID Valid bit	Not Supported	SSID, bit 7
SCSI Parity SD 15-8-Bit	Not Supported	SSTAT2, bit 0
Last Disconnect bit	Not Supported	SSTAT2, bit 1

NCR 53C720

New Registers/Bits (continued)

Registers/Bits	53C710	53C720
Latched SCSI Parity SD 15-8-Bit	Not Supported	SSTAT2, bit 3
SODL Most Significant Byte Full	Not Supported	SSTAT2, bit 5
SODR Most Significant Byte Full	Not Supported	SSTAT2, bit 6
SIDL Most Significant Byte Full	Not Supported	SSTAT2, bit 7
Interrupt On The Fly bit	Not Supported	ISTAT, bit 2
Semaphore bit	Not Supported	ISTAT, bit 4
Host Parity Check Enable bit	Not Supported	CTEST4, bit 3
Shadow Register Test Mode bit	Not Supported	CTEST4, bit 4
SCSI Data Bus High Impedance Mode	Not Supported	CTEST4, bit 5
Enable Host Parity Error Interrupt	Not Supported	DIEN, bit 6
Host Bus Width 16 bits	Not Supported	DCNTL, bit 3
Bus Mode bit	Not Supported	DCNTL, bit 6
SCSI Interrupt Enable Register One — 41h	Not Supported	SIEN1
Handshake Timer Expired	Not Supported	SIEN1, bit 0
General Purpose Timer Expired	Not Supported	SIEN1, bit 1
SCSI Interrupt Status Register Zero — 42h	Not Supported	SIST0
SCSI Interrupt Status Register One — 43h	Not Supported	SIST1
SCSI Wide Register — 45h	Not Supported	SWIDE
SCSI Time Register Zero — 48h	Not Supported	STIME0
Programmable Select/Reselect Timer	Not Supported	STIME0, bits 3-0
Programmable Handshake Timer	Not Supported	STIME0, bits 7-4
SCSI Time Register One — 49h	Not Supported	STIME1
Programmable General Purpose Timer	Not Supported	STIME1, bits 3-0
SCSI Test Register Zero — 4Ch	Not Supported	STEST0

New Registers/Bits (continued)

Registers/Bits	53C710	53C720
SCSI Synchronous Offset Max. bit	Not Supported	STEST0, bit 0
SCSI Synchronous Offset Min. bit	Not Supported	STEST0, bit 1
Arbitration Priority Test bit	Not Supported	STEST0, bit 2
Selection Response Logic bit	Not Supported	STEST0, bit 3
SCSI Test Register One — 4Dh	Not Supported	STEST1
SCSI Test Register Two — 4Eh	Not Supported	STEST2
Extended REQ/ACK Filtering bit	Not Supported	STEST2, bit 1
Always Wide SCSI bit	Not Supported	STEST2, bit 2
SCSI Control Enable bit	Not Supported	STEST2, bit 7
SCSI Test Register Three — 4Fh	Not Supported	STEST3
SCSI FIFO Test Mode bit	Not Supported	STEST3, bit 0
Clear SCSI FIFO bit	Not Supported	STEST3, bit 1
Timer Test Mode bit	Not Supported	STEST3, bit 2
16-bit System	Not Supported	STEST3, bit 3
Disable Single Initiator Response	Not Supported	STEST3, bit 4
Halt SCSI Clock bit	Not Supported	STEST3, bit 5
SCSI Input Data Latch bits 15-8	Not Supported	SIDL
SCSI Output Data Latch bits 15-8	Not Supported	SODL
SCSI Bus Data Lines bits 15-8	Not Supported	SBDL
General Purpose Scratch Pad Register1 — 5C-5Fh	Not Supported	SCRATCH1

NCR 53C720

Deleted Registers/Bits

Registers/Bits	53C710	53C720
Start SCSI Receive Operation bit	SCNTL1, bit 0	Not Supported
Start SCSI Send Operation bit	SCNTL1, bit 1	Not Supported
Enable Selection and Reselection	SCNTL1, bit 5	Not Supported
SCSI Destination ID bits 7-4	SDID bit 7-4	Not Supported
SCSI Chip ID bits 7-4	SCID bit 7-4	Not Supported
SCSI Offset Compare bit	CTEST2, bit 5	Not Supported
SCSI FIFO Write Enable bit	CTEST4, bit 3	Not Supported
DACK/ bit	CTEST5, bit 0	Not Supported
DREQ/ bit	CTEST5, bit 1	Not Supported
EOP bit	CTEST5, bit 2	Not Supported
Chip Test Register Seven	CTEST7	Not Supported

Moved Registers/Bits

Registers/Bits	53C710	53C720
SCSI Destination ID Register (SDID)	Address 02h	Address 06h
SCSI Interrupt Enable Register (SIEN)	Address 03h	Address 40h
SCSI Synchronous Transfer Period	SXFER, bits 6-4	SXFER, bit 7-5
Disable Halt on Parity Error or ATN bit	SXFER, bit 7	SCTRL1, bit 5
SCSI Output Data Latch Register (SODL)	Address 06h	Address 54-55h
SCSI Output Control Latch Register (SOCL)	Address 07h	Address 09h
SCSI Input Data Latch Register (SIDL)	Address 09h	Address 50-51h

Moved Registers/Bits (Continued)

Registers/Bits	53C710	53C720
SCSI Bus Data Line Register (SBDL)	Address 0Ah	Address 58-59h
Synchronous SCSI Clock Frequency	SBCL, bits 1-0	SCNTL3, bits 6-4
SCSI RST/ Received bit	SSTAT0, bit 1	SIST0, bit 1
Unexpected Disconnect bit	SSTAT0, bit 2	SIST0, bit 2
SCSI Gross Error bit	SSTAT0, bit 3	SIST0, bit 3
Selection or Reselection Timeout bit	SSTAT0, bit 5	STIME0, bits 3-0
Function Complete bit	SSTAT0, bit 6	SIST0, bit 6
Phase Mismatch or ATN/ Active bit	SSTAT0, bit 7	SIST0, bit 7
SCSI Status Register One	SSTAT1	SSTAT0
SCSI Status Register Two	SSTAT2	SSTAT1
Chip Test Register Zero (CTEST0)	Address 14h	Address 18h
Data Transfer Direction bit	CTEST0, bit 0	CTEST2, bit 7
Chip Test Register One (CTEST1)	Address 15h	Address 19h
Chip Test Register Two (CTEST2)	Address 16h	Address 1Ah
SCSI FIFO Parity (bits 7-0) bit	CTEST2, bit 4	STEST1, bit 0
Chip Test Register Three (CTEST3)	Address 17h	Address 1Bh
Chip Test Register Four (CTEST4)	Address 18h	Address 21h
SCSI Loopback Enable bit	CTEST4, bit 4	STEST2, bit 4
SCSI High Impedance Mode bit	CTEST4, bit 5	STEST2, bit 3
Chip Test Register Five (CTEST5)	Address 19h	Address 22h
Reset SCSI Offset bit	CTEST5, bit 5	STEST2, bit 6
Chip Test Register Six (CTEST6)	Address 1Ah	Address 23h
SCSI Differential Mode bit	CTEST7, bit 0	STEST2, bit 5
Transfer Type bit	CTEST7, bit 1	CTEST0, bit 1
Even Parity - Host Bus bit	CTEST7, bit 2	CTEST0, bit 2

NCR 53C720

Moved Registers/Bits (Continued)

Registers/Bits	53C710	53C720
DMA FIFO Parity bit	CTEST7, bit 3	CTEST0, bit 3
Snoop Control bits 1-0	CTEST7, bits 6-5	CTEST0, bits 6-5
Selection Timeout Disable bit	CTEST7, bit 4	STIME0 bits 3-0
Cache Burst Disable bit	CTEST7, bit 7	CTEST0, bit 7
Chip Test Register Eight	CTEST8	CTEST3
Interrupt Status Register (ISTAT)	Address 21h	Address 14h
Longitudinal Parity Register	LCRC 23h	SLPAR 44h
Enable Low Level SCSI Mode	DCNTL, bit 3	STEST2, bit 0
Clock Frequency bits	DCNTL, bits 7-6	SCNTL3, bits 2-0

READER'S COMMENT FORM

N C R

BOOK TITLE	BOOK NO.	PRINT DATE

To help us plan future editions of this document, please take a few minutes to answer the following questions. Explain in detail using the space provided. Include page numbers where applicable.

Are there any technical errors or misrepresentations in the document?

_____

_____

_____

Is the material presented in a logical and consistent order?

_____

_____

_____

Is it easy to locate specific information in the document?

_____

_____

_____

Is there any information you would like to have added to the document?

_____

_____

_____

Are the examples relevant to the task being described?

_____

_____

_____

Could parts of the document be deleted without affecting the document's usefulness?

_____

_____

_____

Did the document help you to perform your job?

_____

_____

_____

Any general comments?

_____

_____

_____

CUT ALONG THIS

NAME _____

TITLE _____

COMPANY _____

ADDRESS _____

Thank you for your evaluation of this document.
Fold the form as indicated and mail to NCR. No postage is necessary in the U.S.A.

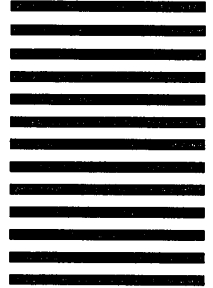TELEPHONE NO. ( ) _____

— fold —

BUSINESS REPLY MAIL

FIRST CLASS   PERMIT NO. 3   DAYTON, OHIO

POSTAGE WILL BE PAID BY ADDRESSEE

NCR Corporation
ATTENTION: Publication Services
WHQ-4
1700 S. Patterson Blvd.
Dayton, Ohio 45409

— fold —

NCR Microelectronic Products Division – Sales Locations

**For literature on any
NCR product or service
call the NCR hotline toll-free:**

1-800-334-5454

**NCR Microelectronic Products Division
Worldwide Sales Headquarters**
1731 Technology Drive, Suite 600
San Jose, CA 95110
(408) 453-0303

Division Plants
NCR Microelectronic Products Division
2001 Danfield Court
Fort Collins, CO 80525
(303) 226-9500

Commercial ASIC Products

Customer Owned Tooling Products

Communication Products

Memory Products

NCR Microelectronic Products Division
1635 Aeroplaza Drive
Colorado Springs, CO 80916
(719) 596-5612

High Reliability ASIC Products

Military Products

Automotive Products

Logic Products

SCSI Products

Internal ASIC Products

North American Sales Offices
Northwest Sales
1731 Technology Drive, Suite 600
San Jose, CA 95110
(408) 441-1080

Southwest Sales
3300 Irvine Avenue, Suite 255
Newport Beach, CA 92660
(714) 474-7095

North Central Sales
8000 Townline Avenue, Suite 209
Bloomington, MN 55438
(612) 941-7075

South Central Sales
17304 Preston Road, Suite 635
Dallas, TX 75252
(214) 733-3594

Northeast Sales
500 West Cummings Park, Suite 4000
Woburn, MA 01801
(617) 933-0778

Southeast Sales
1051 Cambridge Square, Suite C
Alpharetta, GA 30201
(404) 740-9151

International Sales Offices
European Sales Headquarters
Westendstr. 193
8000 Munchen 21
West Germany
49 89 57931199

Asia/Pacific Sales Headquarters
35th Floor, Shun Tak Centre
200 Connaught Road
Central
Hong Kong
852 859 6044