NCR 53C720
SCSI I/O Processor

NCR

Data Manual

Preface

![SCSI Specifications heading bar]

SCSI Specifications

This manual assumes some prior knowledge of current and proposed SCSI standards. For background information, please contact:

ANSI
11 West 42nd Street
New York, NY 10036
(212) 642-4900
Ask for document number X3.131-1986 (SCSI-1)

Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112
(800)-854-7179 or (303) 792-2181 (outside U.S.)
Ask for document number X3.131-199X (SCSI-2)

ENDL Publications
14426 Black Walnut Court
Saratoga, CA 95070
(408) 867-6642
Document names: *SCSI Bench Reference, SCSI Encyclopedia*

Prentice Hall
Englewood Cliffs, NJ 07632
(201) 767-5937
Ask for document number ISBN 0-13-796855-8, *SCSI: Understanding the Small Computer System Interface*

NCR Microelectronic Products Division Electronic Bulletin Board
(719) 576-1649

SCSI Electronic Bulletin Board
(719) 574-0424

Additional Information

NCR 53C720 Programmers Guide
NCR SCSI Engineering Note 839, *NCR TolerANT Technology*

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Chapter One
SCSI I/O Processor Introduction

General Description

The NCR 53C720 is the third member of the 53C7XX family of intelligent, single-chip, third generation SCSI host adapters. A high performance SCSI core and an intelligent 16 or 32-bit bus master DMA core are integrated with a SCSI SCRIPTS processor to accommodate the flexibility requirements of not only SCSI-1 and SCSI-2, but future SCSI standards as well. In addition, the NCR 53C720 solves the protocol overhead problems that have plagued all previous intelligent and non-intelligent adapter designs.

The NCR 53C720 is designed to completely implement a multi-threaded I/O algorithm in either a workstation or file server environment, completely free of processor intervention except at the end of an I/O transfer. In addition, the NCR 53C720 provides automatic relocation of SCRIPTS, and requires no dynamic alteration of SCRIPTS instructions at the start of an I/O operation. All of the SCRIPTS code may be placed on a PROM. The NCR 53C720 allows easy firmware upgrades and is SCRIPTS-compatible with the NCR 53C710.

The NCR 53C720 supports four different host processor interfaces, or bus modes. Bus Mode 1 closely resembles the Motorola 68030 interface, and Bus Mode 2 closely resembles the Motorola 68040 interface. Bus Mode 3 closely resembles the Intel 80386SX interface; the 16-bit host interface should be enabled in this mode. Finally, Bus Mode 4 closely resembles the 80386DX interface. Bus Modes 1, 2 and 4 support both the Big and Little Endian byte ordering schemes and Bus Mode 3 supports Little Endian byte ordering, for a total of seven operating modes. The modes are selected by using the bus mode select pins (BS 2-0).

NCR TolerANT ® Technology

The NCR 53C720 features NCR TolerANT® SCSI driver and receiver technology, which includes active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation causes the SCSI REQ, ACK, Data and Parity signals to be actively driven high by transistors on each pin. The 48 mA drivers actively force the SCSI bus signal to the high (negated) state faster than passive pull-up drivers. TolerANT receivers filter SCSI bus signals to eliminate unwanted transitions without the long signal delay associated with RC-type input filters. This improved driver and receiver technology helps eliminate the double clocking of data, which is the single biggest data reliability problem with the SCSI interface. TolerANT improves data integrity in unreliable cabling environments, where other devices would be subject to data corruption. The benefits of this technology include increased immunity to noise when the signal is going high, increased performance due to balanced duty cycles, and improved Fast SCSI transfer rates. Active Negation is enabled by setting bit 7 in the STEST3 register. It can be used in both single-ended and differential mode. NCR Active Negation technology is compatible with both the Alternative One and Alternative Two termination schemes proposed by the American National Standards Institute.

NCR 53C720 Features Summary

Performance

- Supports variable block size and scatter/gather data transfers

- Supports 16- and 32-bit word data bursts with variable burst lengths

- Memory-to-memory DMA transfers in excess of 44 MB/s

- Minimizes SCSI I/O start latency

- Performs complex bus sequences without interrupts, including restore data pointers

- Unique interrupt status reporting – reduces ISR overhead

- High-speed wide SCSI bus transfers:
  10 MB/S asynchronous
  20 MB/S synchronous

- Memory transfers in excess of 101 MB/s (@ 33 MHz)

- Cache line burst mode

- 64-byte DMA FIFO

Integration

- Full 16 or 32-bit DMA bus master

- High performance wide SCSI core

- Integrated SCRIPTS processor

- Allows intelligent host adapter performance on a motherboard

Ease of Use

- Reduces SCSI development effort

- Supports Big and Little Endian environments

- Compiler-compatible with existing NCR 53C710 SCRIPTS

- Development tools and sample SCSI SCRIPTS provided

- All interrupts are maskable and pollable

- Supports wide SCSI, A or P cable, and up to 16 devices

- Interfaces with seven different host processor buses, including Motorola (680X0 family) and Intel (80X86 family).

- Odd-byte block sizes are supported in conjunction with wide SCSI

- Three programmable SCSI timers: Select/Reselect, Handshake-to-Handshake, and General Purpose. The time-out period is programmable from 100 μs to greater than 1.6 seconds

Flexibility

- High level programming interface (SCSI SCRIPTS)

- Allows tailored SCSI sequences to be executed from main memory or from a host adapter board.

- Flexible sequences to tune I/O performance or to adapt to unique SCSI devices

- Accommodates changes in the logical I/O interface definition

- Low level programmability (register oriented)

- Allows a target to disconnect and later reselect with no interrupt to the system processor

- Allows a multi-threaded I/O algorithm to be executed in SCSI SCRIPTS with fast I/O context switching

- Allows relative jumps

- Allows indirect fetching of DMA address and byte counts so that SCRIPTS can be placed in a PROM.

- Separate SCSI and system clocks

Reliability

- NCR TolerANT SCSI driver and receiver technology

- 2 K volts ESD protection on SCSI signals

- Typical 350 mV SCSI bus hysteresis

- Protection against bus reflections due to impedance mismatches

- Controlled bus assertion times (reduces RFI, improves reliability, and eases FCC certification)

- Latch-up protection greater than 150 mA

- Voltage feed through protection (minimum leakage current through SCSI pads)

- 20% of pins are power and ground

- Ground isolation of I/O pads and chip logic

Testability

- All SCSI signals accessible through programmed I/O

- SCSI loopback diagnostics

- Self-selection capability

- SCSI bus signal continuity checking

- Supports single step mode operation

Figure 1-1. NCR 53C720 Block Diagram
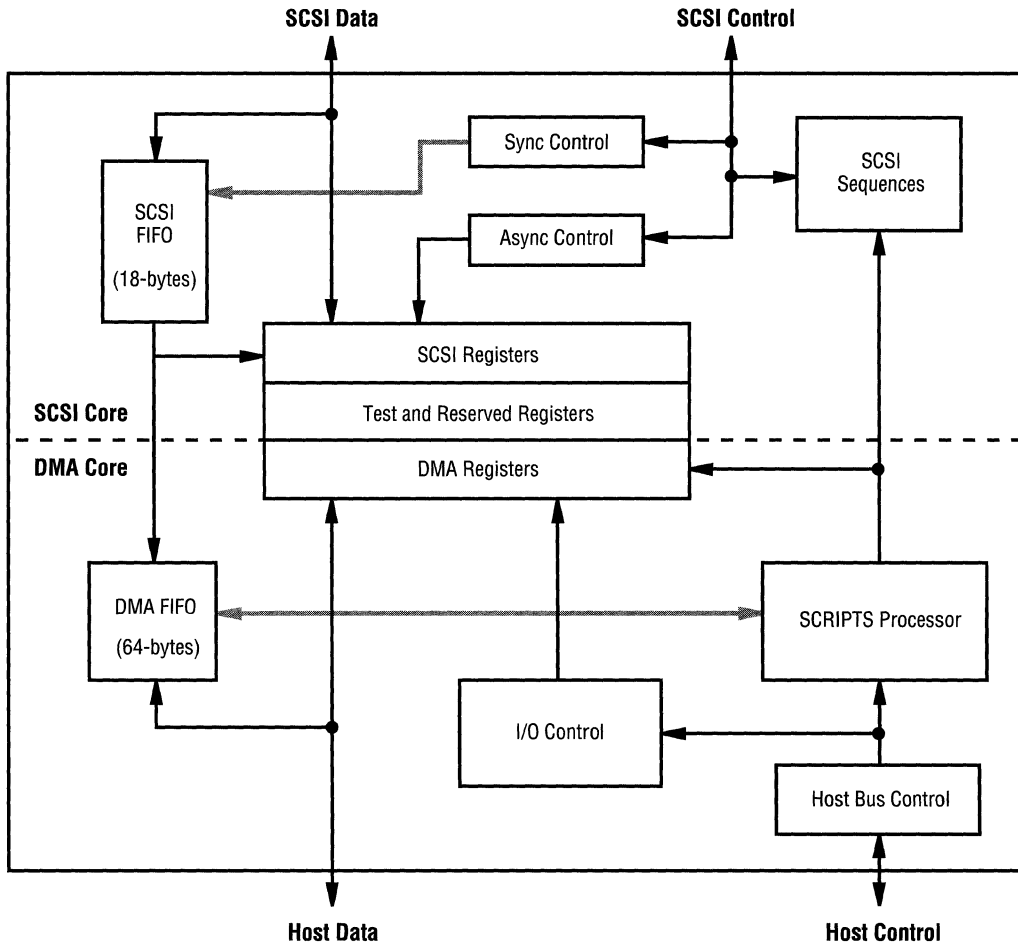
Chapter Two
Functional Description

The NCR 53C720 is composed of three interrelated functional blocks: the SCSI Core, the DMA Core, and the SCRIPTS Processor.

SCSI Core

The SCSI core supports the SCSI-2 fast and wide bus. It supports synchronous transfer rates of up to 20 MB/s, and asynchronous transfer rates up to 10 MB/s. The programmable SCSI interface makes it easy to "fine tune" the system for specific mass storage devices or advanced SCSI requirements.

The SCSI core offers low level register access or a high-level control interface. Like first generation SCSI devices, the NCR 53C720 SCSI core can be accessed as a register-oriented device. The ability to sample and/or assert any signal on the SCSI bus can be used in error recovery and diagnostic procedures. In support of loopback diagnostics, the SCSI core may perform a self-selection and operate as both an initiator and a target. The NCR 53C720 can test the SCSI pins for physical connection to the board or the SCSI bus.

Unlike previous generation devices, the SCSI core can be controlled by the SCRIPTS processor, a high-level logical interface optimized for SCSI protocol. SCRIPTS commands controlling the SCSI core are fetched out of the main host memory. These commands instruct the SCSI core to Select, Reselect, Disconnect, Wait for a Disconnect, Transfer Information, Change Bus Phases and in general, implement all aspects of the SCSI protocol.

DMA Core

The DMA core is a bus master DMA device that is made to attach to Intel (80386SX and 80386DX), and Motorola (68030 and 68040) processors.

The NCR 53C720 supports 16 or 32-bit memory and automatically supports misaligned DMA transfers. A 64-byte FIFO allows the NCR 53C720 to support two, four, eight, or sixteen longwords to be burst across the memory bus interface. This DMA interface does not support dynamic bus sizing.

The DMA core communicates with the SCSI core through the SCRIPTS processor, which supports uninterrupted scatter/gather memory operations.

SCRIPTS Processor

The SCSI SCRIPTS processor allows both DMA and SCSI instructions to be fetched from host memory. Algorithms written in SCSI SCRIPTS can control the actions of the SCSI and DMA cores and are executed from 16- or 32-bit system memory. Complex SCSI bus sequences are executed independently of the host CPU.

The SCRIPTS processor can begin a SCSI I/O operation in approximately 500 ns. This compares with 2-8 ms required for traditional intelligent host adapters. The SCRIPTS processor offers performance and customized algorithms.

Algorithms may be designed to tune SCSI bus performance, to adjust to new bus device types (i.e. scanners, communication gateways, etc.), or to incorporate changes in the SCSI-2/3 logical bus definitions without sacrificing I/O performance.

SCSI SCRIPTS are independent of the CPU and system bus in use. For detailed information on SCSI SCRIPTS, please see the NCR 53C720 *Programmer's Guide.*

Big/Little Endian Support

The Bus Mode Select pin gives the NCR 53C720 the flexibility of operating with either Big or Little Endian byte orientation. Internally, in either mode, the byte lanes of the DMA FIFO and registers are not modified. The NCR 53C720 supports byte and longword slave accesses in Big Endian mode, and byte, word, and longword accesses in Little Endian mode (word accesses must be word-aligned).

When a longword is accessed, no repositioning of the individual bytes is necessary, since longwords are addressed by the address of the least significant byte. SCRIPTS always uses longwords in 32-bit systems, so compatibility is maintained between systems using different byte orientations. When a word is accessed, individual bytes must be repositioned. Internally, the NCR 53C720 adjusts the byte control logic of the DMA FIFO and register decodes to access the appropriate byte lanes. The registers will always appear on the same byte lane, but the address of the register will be repositioned. Words are addressed by the address of the least significant byte.

Note: Big Endian addressing is not supported in 16-bit systems, since SCRIPTS always uses word accesses.

Big/Little Endian mode selection has the most effect on individual byte access. Internally, the NCR 53C720 adjusts the byte control logic of the DMA FIFO and register decodes to enable the appropriate byte lane. The registers will always appear on the same byte lane, but the address of the register will be repositioned.

Data to be transferred between system memory and the SCSI bus always starts at address zero and continues through address 'n' - there is no byte ordering in the chip. The first byte in from the SCSI bus goes to address 0, the second to address 1, etc. Going out onto the SCSI bus, address zero is the first byte out on the SCSI bus, address 1 is the second byte, etc.

Correct SCRIPTS will be generated if the SCRIPTS compiler is run on a system that has the same byte ordering as the target system. Any SCRIPTS patching in memory must patch the instruction in the order that the SCRIPTS processor expects it.

Software drivers for the NCR 53C720 should access registers by their logical name (i.e., "SCNTL0) rather than by their address. The logical name should be equated to the register's Big Endian address in Big Endian mode (SCNTL0 = 03h), and its Little Endian address in Little Endian Mode (SCNTL0 = 00h). This way, there is no change to the software when moving from one mode to the other; only the equate statement setting the operating modes needs to be changed.

Addressing of registers from within a SCRIPTS instruction is independent of bus mode. Internally, the NCR 53C720 always operates in Little Endian mode.

Big Endian Mode

Big Endian addressing is used primarily in designs based on Motorola processors. The NCR 53C720 treats D(31-24) as the lowest physical memory address. The register map is left- justified (Address 03h = SCNTL0).

Little Endian Mode

Little Endian is used primarily in designs based on Intel processors. This mode treats D(7-0) as the lowest physical memory address. The register map is right-justified (Address 00h = SCNTL0).

Table 2-1. Big and Little Endian Addressing

System data bus	(31-24)	(23-16)	(15-8)	(7-0)
53C720 pins	(31-24)	(23-16)	(15-8)	(7-0)
Register	SCNTL3	SCNTL2	SCNTL1	SCNTL0
Little Endian addr	03h	02h	01h	00h
Big Endian addr	00h	01h	02h	03h

Loopback Mode

The NCR 53C720 loopback mode allows testing of both initiator and target functions and, in effect, lets the chip talk to itself. When the Loopback Enable bit is set in the STEST2 register, the NCR 53C720 allows control of all SCSI signals, whether it is operating in initiator or target mode.

Parity Options

The NCR 53C720 implements a flexible parity scheme that allows control of the parity sense, allows parity checking to be turned on or off, and has the ability to deliberately send a byte with bad parity over the SCSI bus to test parity error recovery procedures. The following bits are involved in parity control and observation:

1) Assert ATN/ on Parity Errors – Bit 1 in the SCNTL0 register.

   This bit causes the NCR 53C720 to automatically assert SCSI ATN/ when it detects a parity error while operating as an initiator.

2) Enable Parity Generation – Bit 2 in the SCNTL0 register.

   This bit determines whether the NCR 53C720 generates parity sent to the SCSI bus or allows parity to "flow through" the chip to/from the SCSI bus and system bus.

3) Enable Parity Checking – Bit 3 in the SCNTL0 register.

   This bit enables the NCR 53C720 to check for parity errors. The NCR 53C720 checks for odd parity.

4) Assert Even SCSI Parity – Bit 2 in the SCNTL1 register.

   This bit determines the SCSI parity sense generated by the NCR 53C720, being sent to the host. Parity generation must be enabled.

5) Disable Halt on ATN/ or a Parity Error (Target Mode Only) – Bit 5 in the SCNTL1 register.

   This bit causes the NCR 53C720 to halt operations when a parity error is detected in target mode.

6) Enable Parity Error Interrupt – Bit 0 in the SIEN0 register.

   This bit determines whether the NCR 53C720 will generate an interrupt when it detects a parity error.

7) Parity Error – Bit 0 in the SIST0 register.

   This status bit is set whenever the NCR 53C720 has detected a parity error on either the SCSI bus or the system bus.

8) Status of SCSI Parity Signal – Bit 0 in the SSTAT0 register and bit 0 in SSTAT2.

   These status bits represent the live SCSI Parity Signal (SDP0 and SDP1).

9) Latched SCSI Parity Signal – Bit 3 in the SSTAT1 register and bit 3 in SSTAT2.

   These status bits contain the SCSI parity of the bytes latched in the SIDL.

10) DMA FIFO Parity – Bit 3 in the CTEST2 register.

    This status bit represents the parity bit in the DMA FIFO after data is read from the FIFO by reading the CTEST6 register.

11) DMA FIFO Parity – Bit 3 in the CTEST0 register.
    This write-only bit is written to the DMA FIFO after writing data to the DMA FIFO by writing the CTEST6 register.

12) SCSI FIFO Parity – Bit 0 in the STEST1 register.

    This status bit represents the parity bit in the SCSI FIFO after data is read from the FIFO by reading the SODL register, once bit 0 in STEST3 is asserted.

Table 2-2. SCSI Parity Control

EPG	EPC	ASEP	Description
0	0	0	Will not check for parity errors. Parity flows from DP(3-0) through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP(3-0) when receiving SCSI data. Asserts odd parity when sending SCSI data.
0	0	1	Will not check for parity errors. Parity flows from DP(3-0) through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP(3-0) when receiving SCSI data. Asserts even parity when sending SCSI data.
0	1	0	Checks for odd parity on both SCSI data received and system data when sending. Parity flows from DP(3-0) through the chip to the SCSI bus when sending SCSI data, Parity flows from SCSI bus to DP(3-0) when receiving SCSI data. Asserts odd parity when sending SCSI data.
0	1	1	Checks for odd parity on both SCSI data received and system data when sending. Parity flows from DP(3-0) through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP(3-0) when receiving SCSI data. Asserts even parity when sending SCSI data.
1	0	0	Will not check for parity errors. Parity on DP(3-0) is ignored. Parity is generated when sending SCSI data. Parity flows from SCSI bus to the chip but is not asserted on DP(3-0) when receiving SCSI data. Asserts odd parity when sending SCSI data.
1	0	1	Will not check for parity errors. Parity on DP(3-0) is ignored. Parity is generated when sending SCSI data. Parity flows from SCSI bus to chip, but is not asserted on DP(3-0) when receiving SCSI data. Asserts even parity when sending SCSI data.
1	1	0	Checks for odd parity on SCSI data received. Parity on DP(3-0) is ignored. Parity is generated when sending SCSI data. Parity flows from SCSI bus to the chip, but is not asserted on DP(3-0) when receiving SCSI data. Asserts odd parity when sending SCSI data.
1	1	1	Checks for odd parity on SCSI data received. Parity on DP(3-0) is ignored. Parity is generated when sending SCSI data. Parity flows from SCSI bus to the chip, but is not asserted on DP(3-0) when receiving SCSI data. Asserts even parity when sending SCSI data.

Key: *EPG = Enable Parity Generation (bit 2 SCNTL0)*

EPC = Enable Parity Checking (bit 3 SCNTL0)

ASEP = Assert SCSI Even Parity (bit 2 SCNTL1)

Table 2-3. SCSI Parity Errors and Interrupts

This table describes the options available when a parity error occurs. This table only applies when the Enable Parity Checking bit is set.

DHP	PAR	Description
0	0	Will NOT halt when a parity error occurs in target or initiator mode.
0	1	Will interrupt when a parity error occurs in target or initiator mode.*
1	0	Will halt when a parity error occurs in target mode and will NOT generate an interrupt.
1	1	Will halt when a parity error occurs in target mode and will generate an interrupt in target or initiator mode.*

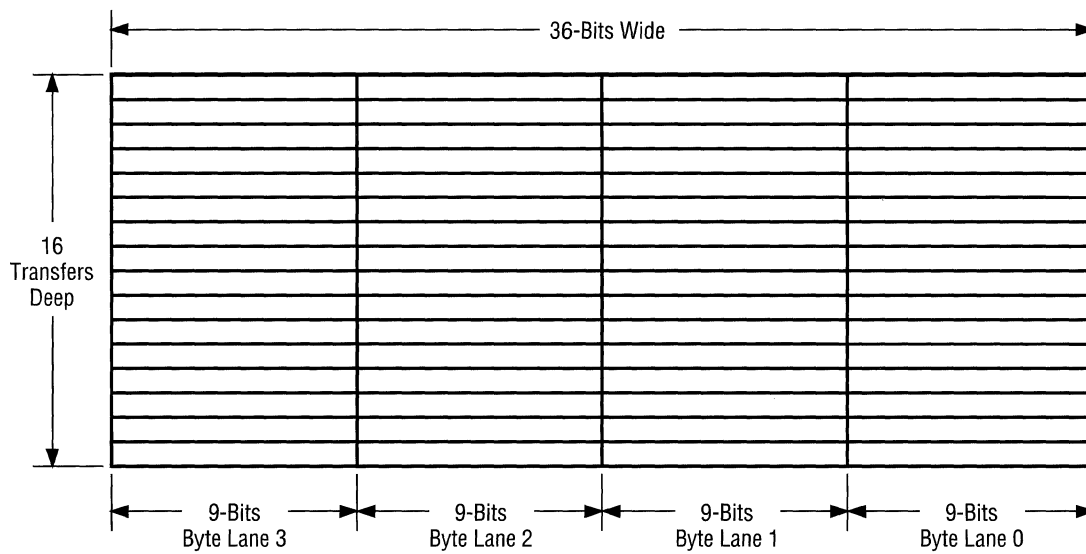**Key:** *DHP = Disable Halt on ATN/ or Parity Error (bit 5 SCNTL1)*

PAR= Parity Error (bit 0 SIEN0)

*Initiator mode parity error interrupts are generated at the end of a block move.

DMA FIFO

The DMA FIFO is more complex than the SCSI
FIFO. The DMA FIFO is a 36 x 16 bit FIFO. It
is divided into 4 sections, each 9 bits wide and 16
transfers deep.

Figure 2-1. DMA FIFO Sections

Data Paths

The data path through the NCR 53C720 is dependent on whether data is being moved into or out of the chip, and whether SCSI data is being transferred asynchronously or synchronously.

Figure 2-2 shows how data is moved to/from the SCSI bus in each of the different modes.

The following steps will determine if any bytes remain in the data path when the chip halts one of the operations listed below.

Asynchronous SCSI Send

1) Subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register. AND the result with 7Fh for a byte count between zero and 64.

2) Read bit 5 in the SSTAT0 and SSTAT2 registers to determine if any bytes are left in the SODL register. If bit 5 is set in the SSTAT0 and SSTAT2, then the least significant byte and the most significant byte in the SODL register is full, respectively.

Synchronous SCSI Send

1) Subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register. AND the result with 7Fh for a byte count between zero and 64.

2) Read bit 5 in the SSTAT0 and SSTAT2 registers to determine if any bytes are left in the SODL register. If bit 5 is set in the SSTAT0 and SSTAT2, then the least significant byte and the most significant byte in the SODL register is full, respectively.

3) Read bit 6 in the SSTAT0 and SSTAT2 registers to determine if any bytes are left in the SODR register. If bit 6 is set in the SSTAT0 and SSTAT2, then the least significant byte and the most significant byte in the SODR register is full, respectively.

Asynchronous SCSI Receive

1) Subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register. AND the result with 7Fh for a byte count between 0 and 64.

2) Read bit 7 in the SSTAT0 and SSTAT2 register to determine if any bytes are left in the SIDL register. If bit 7 is set in the SSTAT0 and SSTAT2, then the least significant byte and the most significant byte is full, respectively.

Synchronous SCSI Receive

1) Subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register. AND the result with 7Fh for a byte count between 0 and 64.

2) Read the SSTAT1 register and examine bits 7-4, the binary representation of the number of valid bytes in the SCSI FIFO, to determine if any bytes are left in the SCSI FIFO.

Figure 2-2. NCR 53C720 Data Paths

μP Interface	μP Interface	μP Interface	μP Interface
↓	↑	↓	↑
DMA FIFO (36-bits x 16)	DMA FIFO (36-bits x 16)	DMA FIFO (36-bits x 16)	DMA FIFO (36-bits x 16)
↓	↑	↓	↑
SODL Register	SIDL Register	SODL Register	SCSI FIFO (18-bits x 9)
↓	↑	↓	↑
SCSI Interface	SCSI Interface	SODR Register	SCSI Interface
		↓	
		SCSI Interface	
Asynchronous SCSI Send	Asynchronous SCSI Receive	Synchronous SCSI Send	Synchronous SCSI Receive

Host Interface

Misaligned Transfers

The NCR 53C720 accommodates block data transfers beginning or ending on odd byte or odd word addresses in system memory. Such addresses are termed "misaligned." An odd byte is defined as one in which the address contains A0 = 1; an odd word is defined as one in which the address contains A1 = 1. Misaligned transfers differ depending on the type of transfer and whether they occur at the start or end of the transfer. The NCR 53C720 does not perform 24-bit transfers.

Transfer Size Throttling

The burst control logic in the NCR 53C720 includes an optional throttling technique which will not allow a size change to occur within a bus ownership. When size throttling is enabled, a new bus ownership will occur each time the transfer changes size. When size throttling is enabled, bit 0 (SM) of the CTEST3 register should be clear. Size throttling can be enabled or disabled using the Size Throttle Enable (STE) bit, bit 7 in the DCNTL register. Cache line bursting is controlled with the Cache Burst Disable (CDIS) bit, bit 7 in the CTEST0 register. Figure 2-3 illustrates the function of the CDIS and STE bits. In Item 1, cache line burst is enabled and size throttling is disabled. Since the starting address is at an odd byte boundary, the NCR 53C720 lines up to a word boundary by performing a single-byte transfer in a single bus ownership. Then, since the address is at an odd word boundary (bit A1 = 1), the NCR 53C720 lines up to a longword boundary by performing a single word transfer in a single bus ownership. At this point, one longword transfer is performed per bus ownership until the address bits line up to a cache line boundary. Once aligned, the cache line, longword, word and byte are transferred in a single bus ownership to complete the transfer.

In Item 2, cache line burst and size throttling are enabled. The NCR 53C720 lines up to a cache line boundary as described for Figure 1 above. Once aligned, the cache line and longword are transferred in the same bus ownership since the two are considered the same size. The remaining word and byte are transferred in two separate bus ownerships to complete the transfer.

In Item 3, cache line burst and size throttling are disabled. The NCR 53C720 completes eight transfers in one bus ownership, since the burst length is set to eight. The remaining four transfers are transferred in one bus ownership to complete the transfer.

In Item 4, cache line burst is disabled and size throttling is enabled. The NCR 53C720 lines up to a longword boundary. Since the address starts on an odd byte boundary, the NCR 53C720 lines up to a word boundary by performing a single byte transfer in a single bus ownership. Then, since the address is at an odd word boundary, the NCR 53C720 lines up to a longword boundary by performing a single word transfer in a single bus ownership. Once aligned, longwords are transferr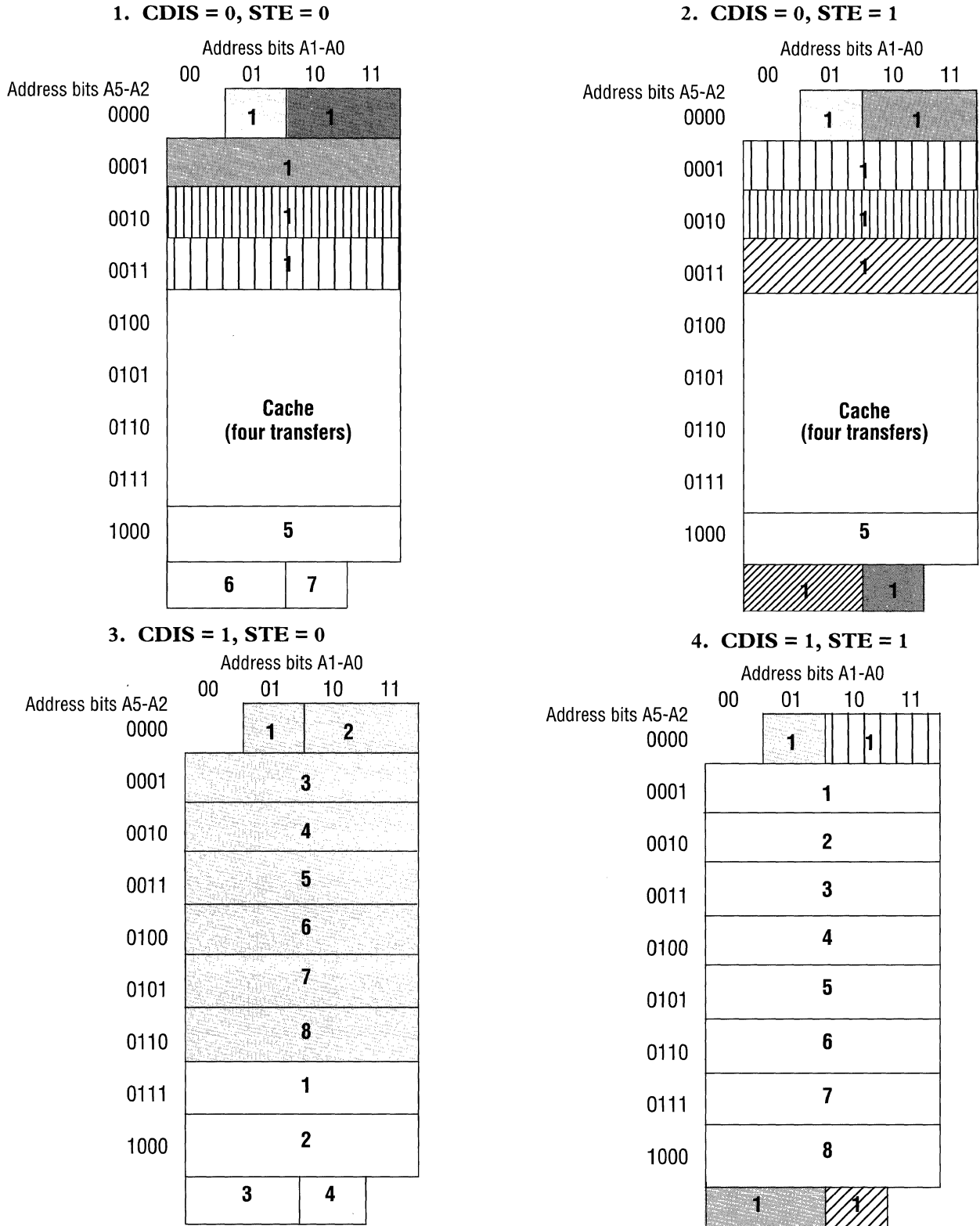ed in the same bus ownership. The remaining word and byte are transferred in separate bus ownerships to complete the transfer.

Figure 2-3. Transfer Size Throttling

1. CDIS = 0, STE = 0

Address bits A1-A0

| | 00 | 01 | 10 | 11 |

Address bits A5-A2

0000 — 1, 1
0001 — 1
0010 — 1
0011 — 1
0100
0101
0110 — Cache (four transfers)
0111
1000 — 5
6 | 7

2. CDIS = 0, STE = 1

Address bits A1-A0

| | 00 | 01 | 10 | 11 |

Address bits A5-A2

0000 — 1, 1
0001 — 1
0010 — 1
0011 — 1
0100
0101
0110 — Cache (four transfers)
0111
1000 — 5
1 | 1

3. CDIS = 1, STE = 0

Address bits A1-A0

| | 00 | 01 | 10 | 11 |

Address bits A5-A2

0000 — 1 | 2
0001 — 3
0010 — 4
0011 — 5
0100 — 6
0101 — 7
0110 — 8
0111 — 1
1000 — 2
3 | 4

4. CDIS = 1, STE = 1

Address bits A1-A0

| | 00 | 01 | 10 | 11 |

Address bits A5-A2

0000 — 1, 1
0001 — 1
0010 — 2
0011 — 3
0100 — 4
0101 — 5
0110 — 6
0111 — 7
1000 — 8
1 | 1

Notes: 1. CDIS = Cache Burst Disable bit, STE = Size Throttle Enable bit.
2. At the start of the diagram, 38 bytes remain to be transferred.
3. The programmable burst length is 8.
4. Each of the shaded areas represents a new bus ownership.
5. The numbers within the shaded areas represent the number of transfers done in the bus ownership.
6. In order for a cache line burst to be attempted, there must be more than 31 bytes left to transfer.

Bus Retry

Bus Retry allows the NCR 53C720 to retry the previous cycle using the same address, size, etc. The bus retry signals are asserted by an external device using the HALT/ (Halt) and BERR/ (Bus Error) signals in Bus Mode 1, the TA/ (Transfer Acknowledge) and TEA/ (Transfer Error Acknowledge) in Bus Mode 2, and TEA/ (Transfer Error Acknowledge) and ReadyI/ in Bus Modes 3 and 4. Asserting these two signals causes the chip to release the SCSI bus and assert the Bus Request signal immediately, without a fairness delay, to try to regain control of the SCSI bus. This will repeat indefinitely (as long as the signals are asserted) until the cycle completes normally, or a bus error occurs.

During a non-cache line burst, a bus retry can be executed in any cycle. During a cache line burst, however, the bus retry should be executed during the first cycle. In Bus Mode 1, the NCR 53C720 will retry the bus cycle and assert the CBREQ/ (Cache Burst Request) again. If a bus retry is attempted during one of the subsequent cycles, the NCR 53C720 will halt the transfer until the Halt signal is deasserted. If the bus error signal is still asserted at this time, the NCR 53C720 will abort the transfer. In Bus Mode 2, if a bus retry is attempted during one of the subsequent cycles the NCR 53C720 will abort the transfer. A bus retry cannot be attempted during a Preview of Address (PA/). For more information on the PA/ signal, refer to Chapter 3, "Signal Descriptions."

If the BERR/ or TEA/ signal is asserted without HALT/, TA/, or ReadyI/, a Bus Fault interrupt will be generated, which sets bit 5 in the DSTAT register (0Ch). The 53C720 will not automatically attempt to regain control of the SCSI bus.

The NCR 53C720 may also relinquish the SCSI bus by asserting the Backoff (BOFF/) signal. For more information on the operation of this signal, refer to Chapter 3, "Signal Descriptions." BOFF/ causes the NCR 53C720 to release the bus and

stay off in accordance with the timings in Chapter 7, "Electrical Characteristics. " Since BOFF/ is sampled only at the beginning and end of each cycle, the NCR 53C720 may get off the bus by executing a bus retry, then assert BOFF/ at the end of the cycle to prevent the chip from immediately trying to regain control of the bus.

Note: the data that is on the bus at the beginning of a retry remains in the 53C720 output buffer until the cycle completes. Therefore, any read of the chip will return this data, rather than data from a more recent operation. The output buffer is cleared only by a bus error or normal completion of the cycle.

Bidirectional STERM/-TA/ -ReadyIn/

The STERM/_TA/_ReadyIn/ (referred to as STERM/) signal terminates a read or write cycle. In a typical system, STERM/ is a wired-OR signal driven by slave devices and monitored by bus masters. When the system CPU is faster than the slave device being accessed, a cycle may be terminated as soon as the slave is ready. Slave devices that are faster than the CPU present a special problem in that they are required to insert wait states to allow the CPU to catch up. The NCR 53C720 is able to accommodate both situations.

During slave accesses, the SLACK/-ReadyO/ (Referred to as SLACK/) output provides an indication that the NCR 53C720 is ready to terminate a read or write cycle. After asserting SLACK/, the NCR 53C720 will sample STERM/ on every subsequent rising BCLK edge until it is sampled active, at which time the read/write cycle will be terminated. Any time between SLACK/ and STERM/ is treated as a wait state; a read/write cycle may be stretched indefinitely. However on a write cycle, data is taken into the NCR 53C720 before the SLACK/ signal is asserted. Wait states may not be added to allow for late write data.

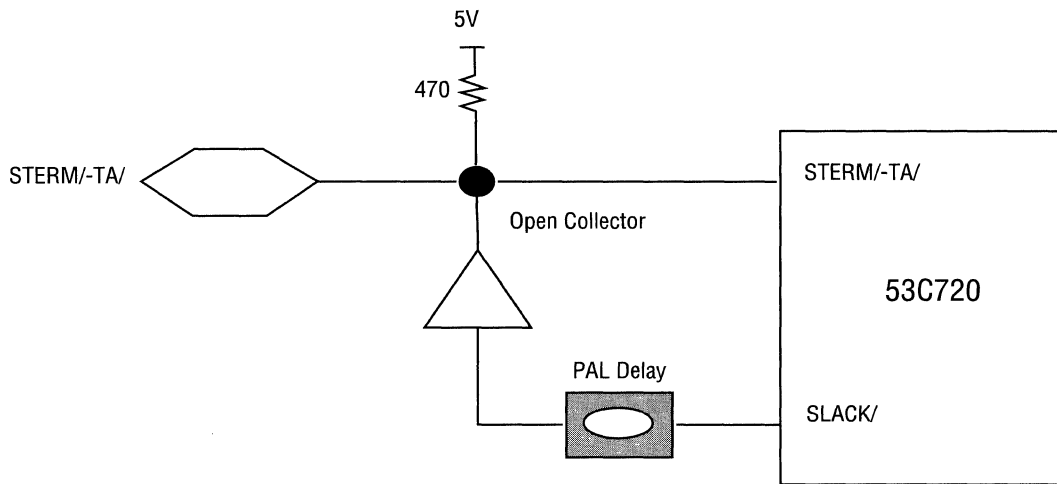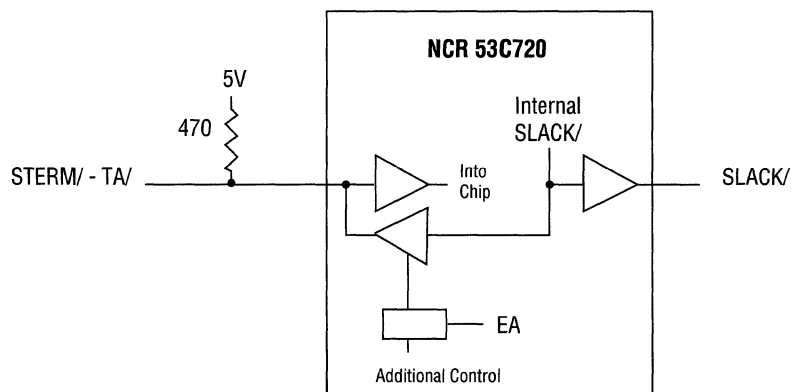Figure 2-4. SLACK/ tied back to STERM/, EA bit not set

Figure 2-5. Bidirectional STERM/, EA bit set

Typically, SLACK/ is tied back to STERM/ as in Figure 2-4. If the system CPU is not capable of completing a slave cycle in the minimum time required by the NCR 53C720, SLACK/ must be delayed before asserting STERM/. If the system CPU is capable of running slave write cycles with zero additional wait states, no delay is necessary.

In systems where the CPU is faster than the NCR 53C720, SLACK/ may be connected to STERM/ with external logic, but the best solution is to set the Enable Acknowledge (EA) bit in the DCNTL register to internally connect SLACK/ to STERM/. When the EA bit is set, the STERM/ pin changes from being an input in both master and slave modes, and becomes bidirectional: input in master mode, and output in slave mode. This way, no external logic is required and proper timing for zero wait state operation is guaranteed. Setting the EA bit must be the first slave I/O access to the NCR 53C720. In addition, when the Enable Acknowledge is set, a signal with the same timing characteristics as SLACK/ will be driven onto the STERM/_TA/ pin, as illustrated in Figure 2-4. The external timings on this signal will be the same as the signal generated if EA was not used, as illustrated in Figure 2-5. The additional control logic will tristate the STERM/_TA/ for 5 ns after it is deasserted. The SLACK/ signal will always be driven.

SCSI Bus Interface

The NCR 53C720 can be used in both single-ended and differential applications.

In single-ended mode, all SCSI signals are active low. The NCR 53C720 contains the open-drain output drivers and can be connected directly to the SCSI bus. Each output is isolated from the power supply to ensure that a powered-down NCR 53C720 has no effect on an active SCSI bus

(CMOS "voltage feed-through" phenomenon). Additionally, NCR TolerANT provides signal filtering at the inputs of REQ/ and ACK/ to increase immunity to signal reflections.

In differential Mode, the SDIR (15-0), SDIRP (1-0), IGS, TGS, RSTDIR, BSYDIR, and SELDIR signals control the direction of external differential-pair transceivers. See Figure 2-6 for the suggested differential wiring diagram. The wiring diagram shows eight 75ALS170 3-channel transceivers and one 75ALS171 3-channel transceiver, though other single and multi-channel devices may be used (DS36954 4-channel transceiver, for instance). The suggested value for the 15 pull-up resistors in the diagram is 680 Ω. The pull-up value should be no lower than the transceiver IOL can tolerate, but not so high as to cause RC timing problems.

Interrupt Handling

The SCRIPTS processor in the NCR 53C720 performs most functions independently of the host microprocessor. However, certain interrupt situations must be handled by the external microprocessor. This section explains all aspects of interrupts as they apply to the NCR 53C720.

Polling vs. Hardware Interrupts

The external microprocessor can be informed of an interrupt condition by polling or hardware interrupts. Polling means that the microprocessor must continually loop and read a register until it detects a bit set that indicates an interrupt. This method is the fastest, but it wastes CPU time that could be used by other system tasks. The preferred method of detecting interrupts in most systems is hardware interrupts. In this case, the NCR 53C720 will assert the Interrupt Request

Figure 2-6. Differential Wiring Diagram
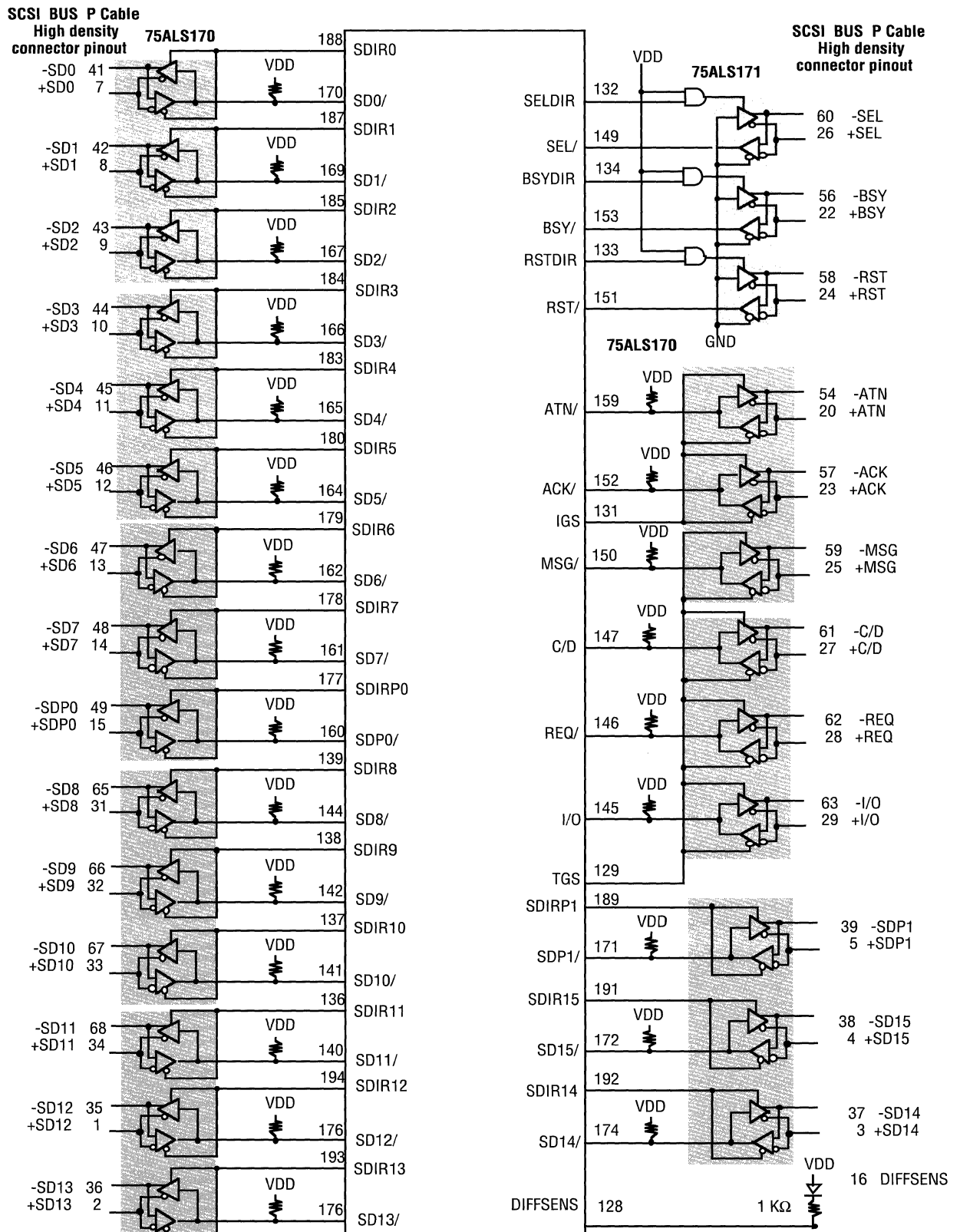
(IRQ/) line that will interrupt the microprocessor, causing the microprocessor to execute an interrupt service routine. A hybrid approach would use hardware for long waits, and use polling for short waits.

Registers

The registers in the NCR 53C720 that are used for detecting or defining interrupts are the ISTAT, SIST0, SIST1, DSTAT, SIEN0, SIEN1, and DIEN.

The ISTAT is the only register than can be accessed as a slave during SCRIPTS operation, therefore it is the register that is polled when polled interrupts are used. It is also the first register that should be read when the IRQ/ pin has been asserted in association with a hardware interrupt. The INTF (Interrupt on the Fly) bit should be the first interrupt serviced. It must be written to one to be cleared. This interrupt must be cleared before servicing any other interrupts. If the SIP bit in the ISTAT register is set, then a SCSI-type interrupt has occurred and the SIST0 and SIST1 registers should be read. If the DIP bit in the ISTAT register is set, then a DMA-type interrupt has occurred and the DSTAT register should be read. SCSI-type and DMA-type interrupts may occur simultaneously, so in some cases both SIP and DIP may be set.

The SIST0 and SIST1 registers contain the SCSI-type interrupt bits. Reading these registers will determine which condition or conditions caused the SCSI-type interrupt, and will clear that SCSI interrupt condition. If the NCR 53C720 is receiving data from the SCSI bus and a fatal interrupt condition occurs, the NCR 53C720 will attempt to send the contents of the DMA FIFO to memory before generating the interrupt. If the NCR 53C720 is sending data to the SCSI bus and a fatal SCSI interrupt condition occurs, data could be left in the DMA FIFO. Because of this the DFE bit in DSTAT should be checked. If this bit is clear, set the CLF (Clear DMA) and CSF (SCSI FIFO)) bits before continuing.

The DSTAT register contains the DMA-type interrupt bits. Reading this register will determine which condition or conditions caused the DMA-type interrupt, and will clear that DMA interrupt condition. Bit 7 in DSTAT, DFE (DMA FIFO Empty), is purely a status bit; it will not generate an interrupt under any circumstances and will not be cleared when read. DMA interrupts will flush neither the DMA nor SCSI FIFOs before generating the interrupt, so the DFE bit in the DSTAT register should be checked after any DMA interrupt. If the DFE bit is clear, then the FIFOs must be cleared by setting the CLF (Clear DMA) and CSF (SCSI FIFO) bits, or flushed by setting the FLF (Flush DMA FIFO) bit. The CLF bit is bit 2 in CTEST3. The FLF bit is bit 3 in CTEST3. The CSF bit is bit 1 in STEST3.

The SIEN0 and SIEN1 registers are the interrupt enable registers for the SCSI interrupts in SIST0 and SIST1.

The DIEN register is the interrupt enable register for DMA interrupts in DSTAT.

Fatal vs. Non-Fatal Interrupts

A fatal interrupt, as the name implies, always causes SCRIPTS to stop running. A non-fatal interrupt will cause SCRIPTS to stop running only if it is not masked. Masking will be discussed later in this engineering note. All DMA interrupts (indicated by the DIP bit in ISTAT and one or more bits in DSTAT being set) are fatal.

Some SCSI interrupts (indicated by the SIP bit in the ISTAT and one or more bits in SIST0 or SIST1 being set) are non-fatal. When the chip is operating in Initiator mode, only the CMP (Function Complete) and SEL (Selected or Reselected) interrupts are non-fatal. When operating in Target mode CMP, SEL, and M/A (Target mode: ATN/ active) are non-fatal. Refer to the description for the DHP (Disable Halt on a Parity Error or ATN/ active (Target Mode Only)) bit in the SXFER register to configure the chip's behavior when the ATN/ interrupt is enabled during Target mode operation. The Interrupt on the Fly interrupt is also non-fatal, since SCRIPTS can continue when it occurs.

The reason for non-fatal interrupts is to prevent SCRIPTS from stopping when an interrupt occurs that does not require service from the CPU. This prevents an interrupt when arbitration is complete (CMP set), when the NCR 53C720 has been selected or reselected (SEL set), or when the initiator has asserted ATN (target mode: ATN/ active). These interrupts are not needed for events that occur during high-level SCRIPTS operation.

Masking

Masking an interrupt means disabling or ignoring that interrupt. Interrupts can be masked by clearing bits in the SIEN (for SCSI interrupts) register or DIEN (for DMA interrupts) register. How the chip will respond to masked interrupts depends on: whether polling or hardware interrupts are being used; whether the interrupt is fatal or non-fatal; and whether the chip is operating in Initiator or Target mode.

If a non-fatal interrupt is masked and that condition occurs, SCRIPTS **will not** stop, the appropriate bit in the SIST0 or SIST1 **will** still be set, the SIP bit in the ISTAT **will not** be set, and the IRQ/ pin **will not** be asserted. See the section on non-fatal vs. fatal interrupts for a list of the non-fatal interrupts.

If a fatal interrupt is masked and that condition occurs, then SCRIPTS **will** still stop, the appropriate bit in the DSTAT, SIST0, or SIST1 register **will** be set, the SIP or DIP bits in the ISTAT **will** be set, and the IRQ/ pin **will not** be asserted.

When the chip is initialized, enable **all** fatal interrupts if you are using hardware interrupts. If a fatal interrupt is disabled and that interrupt condition occurs, SCRIPTS will halt and the system will never know it unless it times out and checks the ISTAT after a certain period of inactivity.

If you are polling the ISTAT instead of using hardware interrupts, then masking a fatal interrupt will make no difference since the SIP and DIP bits in the ISTAT inform the system of interrupts, not the IRQ/ pin.

Masking an interrupt after IRQ/ is asserted will not cause IRQ/ to be deasserted.

Stacked Interrupts

The NCR 53C720 has the ability to stack interrupts if they occur one after the other. If the SIP or DIP bits in the ISTAT register are set (first level), then there is already at least one pending interrupt and any future interrupts will be stacked in extra registers behind the SIST0, SIST1, and DSTAT registers (second level). When two interrupts have occurred and the two levels of the stack are full, any further interrupts will set additional bits in the extra registers behind SIST0, SIST1, and DSTAT. When the first level of interrupts are cleared, all the interrupts that came in afterward will move into the SIST0, SIST1, and DSTAT. After the first interrupt is cleared by reading the appropriate register, the IRQ/ pin will be deasserted for a set time as published in the product Data Manual; the stacked interrupt(s) will move into the SIST0, SIST1, or DSTAT; and the IRQ/ pin will be asserted once again.

Since a masked non-fatal interrupt will not set the SIP or DIP bits, interrupt stacking will not occur as a result of a masked, non-fatal interrupt. A masked, non-fatal interrupt will still post the interrupt in SIST0 or SIST1, but will not assert the IRQ/ pin. Since no interrupt is generated, future interrupts will move right into the SIST0 or SIST1 instead of being stacked behind another interrupt. When another condition occurs that generates an interrupt, the bit corresponding to the earlier masked non-fatal interrupt will still be set.

A related situation to interrupt stacking is when two interrupts occur simultaneously. Since stacking does not occur until the SIP or DIP bits are set, there is a small timing window in which

multiple interrupts can occur but will not be stacked. These could be multiple SCSI interrupts (SIP set), multiple DMA interrupts (DIP set), or multiple SCSI and multiple DMA interrupts (both SIP and DIP set).

As previously mentioned, DMA interrupts will not attempt to flush the FIFOs before generating the interrupt. It is important to set either the CLF (Clear DMA) or CSF (SCSI FIFO) bit if a DMA interrupt occurs and the DFE (DMA FIFO Empty) bit is not set. This is because any future SCSI interrupts will not be posted until the DMA FIFO is clear of data. These 'locked out' SCSI interrupts will be posted as soon as the DMA FIFO is empty.

Halting in an Orderly Fashion

When an interrupt occurs, the NCR 53C720 will attempt to halt in an orderly fashion.

- If in the middle of an instruction fetch, the fetch will be completed, except in the case of a Bus Fault or Watchdog Time-out. Execution will not begin, but the DSP will point to the next instruction since it is updated when the current Script is fetched.

- If the DMA direction is a write to memory and a SCSI interrupt occurs, the 53C720 will attempt to flush the DMA FIFO to memory before halting. Under any other circumstances only the current cycle will be completed before halting, so the DFE bit in DSTAT should be checked to see if any data remains in the DMA FIFO.

- SCSI REQ/ACK handshakes that have begun will be completed before halting.

- The 53C720 will attempt to clean up any outstanding synchronous offset before halting.

- In the case of Transfer Control Instructions, once instruction execution begins it will continue to completion before halting.

- If the instruction is a JUMP/CALL WHEN <phase>, the DSP will be updated to the transfer address before halting.

- All other instructions may halt before completion.

Sample Interrupt Service Routine

The following is a sample of an interrupt service routine for the NCR 53C720. It can be repeated if polling is used, or should be called when the IRQ/ pin is asserted if hardware interrupts are used.

1. Read ISTAT.

2. If the INTF bit is set, it must be written to a one to clear this status.

3. If only the SIP bit is set, read SIST0 and SIST1 to clear the SCSI interrupt condition and get the SCSI interrupt status. The bits in the SIST0 and SIST1 tell which SCSI interrupt(s) occurred and determine what action is required to service the interrupt(s).

4. If only the DIP bit is set, read the DSTAT to clear the interrupt condition and get the DMA interrupt status. The bits in the DSTAT will tell which DMA interrupt(s) occurred and determine what action is required to service the interrupt(s).

5. If both the SIP and DIP bits are set, read SIST0, SIST1, and DSTAT to clear the SCSI and DMA interrupt condition and get the interrupt status. If using 8-bit reads of the SIST0, SIST1, and DSTAT registers to clear interrupts, insert 12 BCLKs between the consecutive reads to ensure that the interrupts clear properly. Both the SCSI and DMA interrupt conditions should be handled before leaving the ISR. It is recommended that the DMA interrupt be serviced before the SCSI interrupt because a serious DMA interrupt condition could influence how the SCSI interrupt is acted upon.

6. When using polled interrupts, go back to step 1 before leaving the interrupt service routine, in case any stacked interrupts moved in when the first interrupt was cleared. When using hardware interrupts, the IRQ/ pin will be asserted again if there are any stacked interrupts. This should cause the system to re-enter the interrupt service routine.

Terminator Networks

The terminator networks provide the biasing needed to pull inactive signals to an inactive voltage level, and are required for both single-ended and differential applications. Terminators must be installed at the extreme ends of the SCSI cable, and only at the ends; no system should ever have more or less than 2 sets of terminators installed and active. SCSI host adapters should provide a means of accommodating terminators. The terminators should be socketed, so that if not needed they may be removed.

Single-ended cables are terminated differently from differential cables. Single-ended cables use a 220 Ω pull-up to the termination power supply (Term-Power) line and a 330 Ω pull-down to Ground. Differential cables use a 330 Ω pull-up from "– SIG" to Term-Power, a 330 Ω pull-down from "+ SIG" to Ground, and a 150 Ω resistor from "– SIG" to "+ SIG".

Because of the high performance nature of the NCR 53C720, Alternative Two termination (Defined in the ANSI standard) is recommended for single-ended systems. This method employs a 2.85 Volt regulator and 110 Ω pull-up resistors (no pull-down). Figure 2-7 shows the schematics for Alternative Two termination. For additional information, refer to the SCSI-2 specification.

(Re)Select During (Re)Selection

In multi-threaded SCSI I/O environments, it is not uncommon to be selected or reselected while trying to perform selection/reselection. This situation may occur when a SCSI controller (operating in initiator mode) tries to select one target and gets reselected by another. The analogous situation for target devices is being selected while trying to perform a reselection.

Once a change in operating mode occurs, the initiator SCRIPT should start with a Set Initiator instruction or the target SCRIPT should start with a SET Target instruction. It should be noted that the selection and reselection enable bits (SCID bits 5 and 6, respectively) should both be asserted so that the NCR 53C720 may respond as an initiator or as a target.

The selection or reselection enable bits allow the NCR 53C720 to respond as either a target or an initiator. For example, if only selection is enabled, the NCR 53C720 cannot be reselected as an initiator. There are also interrupt status and interrupt enable bits in the SIST0 and SIEN0 registers respectively, indicating if the NCR 53C720 has been selected (bit 5) and reselected (bit 4).

Figure 2-7. NCR 53C720 Alternative Two Termination

Key:
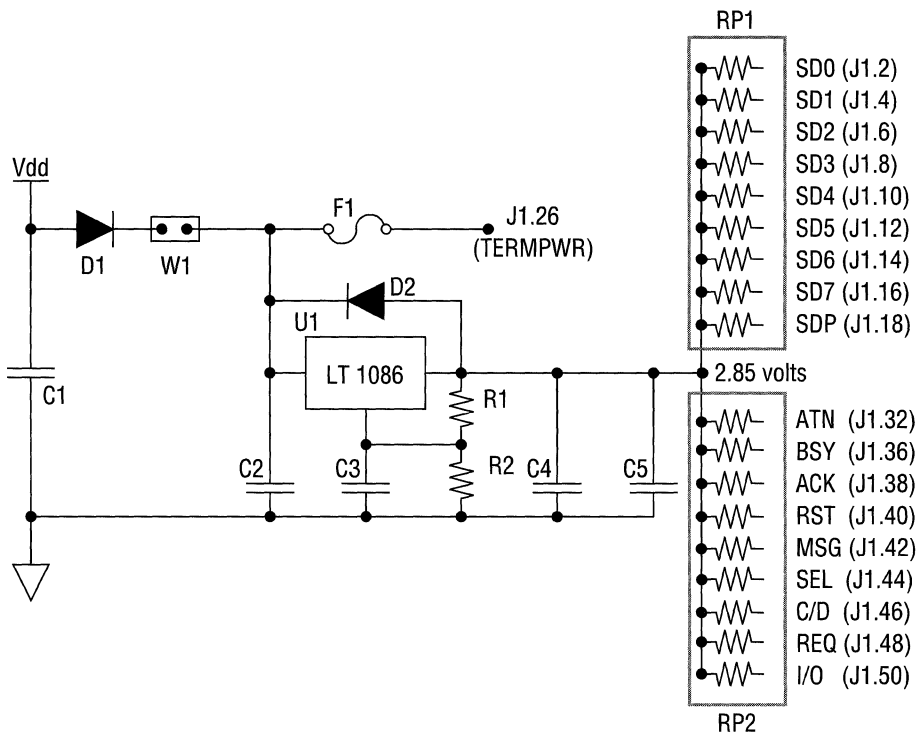
C1	4.7μF tantalum, SMT
C2, C3	1.0μF tantalum, SMT
C4	22μF tantalum, SMT
C5	0.1μF ceramic, SMT
D1-D2	Schottkey diode, 1NS817
F1	1.5 Amp fuse, socketed, 2AG
J1	50-pin dual row header, male SCSI connector for 8-bit SCSI bus
RP1-RP2	110x9 (1%) pull-ups, SIP-10
U4	Voltage Regulator, TO-39
W1	2-position header
R1	121 Ω, 1 %
R2	154 Ω, 1%

Synchronous Operation

The NCR 53C720 can transfer synchronous SCSI data in both initiator and target modes. The SXFER register controls both the synchronous offset and the transfer period, and may be loaded by the CPU before SCRIPTS execution begins or from within a SCRIPT via a table indirect I/O instruction.

The NCR 53C720 can always receive data from the SCSI bus at a synchronous transfer period as short as 160 ns for SCSI-1 or 80 ns for SCSI-2, regardless of the transfer period used to send data. Therefore, when negotiating for synchronous data transfers, the suggested transfer period is 80 or 160 ns. Depending on the SCLK frequency and the synchronous clock divider, the NCR 53C720 can send synchronous data at intervals as short as 100 or 200 ns.

Chapter Three
Signal Descriptions

The NCR 53C720 host bus can operate in one of four modes: Bus Mode 1 (68030-like), Bus Mode 2 (68040-like), Bus Mode 3 (80386SX-like), and Bus Mode 4 (80386DX-like).   Both Big and Little Endian byte orientations are supported in Bus Modes 1, 2, and 4.   The bus mode is selected by using the BS (2-0) pins. A function is listed on the table as NC (not connected) if it is not active for a given bus mode. A slash   ("/") indicates an active-low signal. All pins have a totem pole architecture unless otherwise noted. When the NCR 53C720 is in slave mode, the following signals are tristated: DS/, HALT/, FC(2-0), SC(1-0), BGACK/, UPSO, and CBREQ/.

Figure 3-1. NCR 53C720 Pin Diagram, Bus Modes 1 and 2
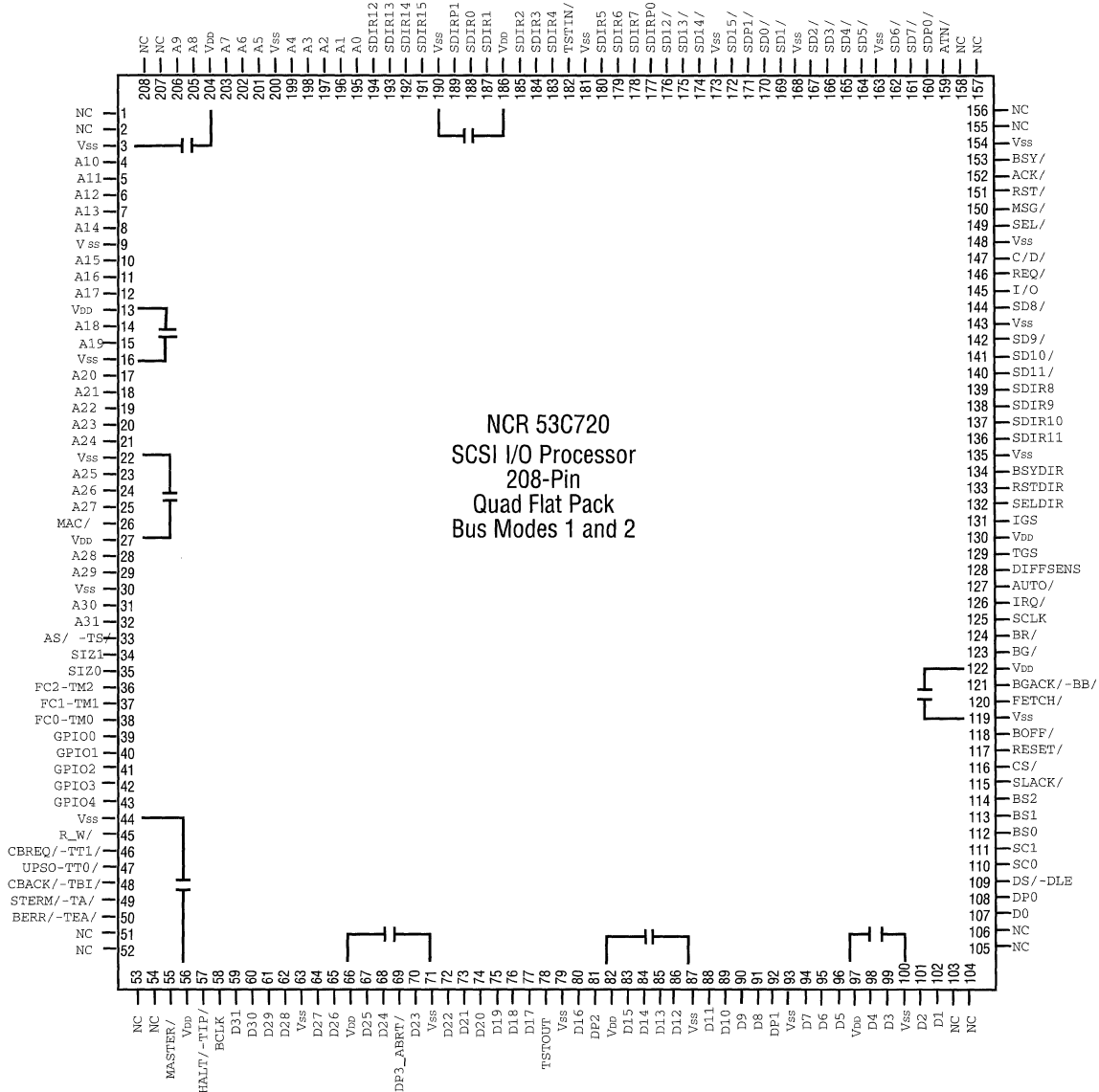
Figure 3-2. NCR 53C720 Pin Diagram, Bus Modes 3 and 4

NCR 53C720
SCSI I/O Processor
208-Pin
Quad Flat Pack
Bus Modes 3 and 4

Top pins (left to right): 208 NC, 207 NC, 206 A9, 205 A8, 204 VDD, 203 A7, 202 A6, 201 A5, 200 Vss, 199 A4, 198 A3, 197 A2, 196 A1_BE1/, 195 A0_BE0/, 194 SDIR12, 193 SDIR13, 192 SDIR14, 191 SDIR15, 190 Vss, 189 SDIRP1, 188 SDIR0, 187 SDIR1, 186 VDD, 185 SDIR2, 184 SDIR3, 183 SDIR4, 182 TSTIN/, 181 Vss, 180 SDIR5, 179 SDIR6, 178 SDIR7, 177 SDIRP0, 176 SD12/, 175 SD13/, 174 SD14/, 173 Vss, 172 SD15/, 171 SDP1/, 170 SD0/, 169 SD1/, 168 Vss, 167 SD2/, 166 SD3/, 165 SD4/, 164 SD5/, 163 Vss, 162 SD6/, 161 SD7/, 160 SDP0/, 159 ATN/, 158 NC, 157 NC

Left pins (top to bottom): 1 NC, 2 NC, 3 Vss, 4 A10, 5 A11, 6 A12, 7 A13, 8 A14, 9 Vss, 10 A15, 11 A16, 12 A17, 13 VDD, 14 A18, 15 A19, 16 Vss, 17 A20, 18 A21, 19 A22, 20 A23, 21 A24, 22 Vss, 23 A25, 24 A26, 25 A27, 26 MAC/, 27 VDD, 28 A28, 29 A29, 30 Vss, 31 A30, 32 A31, 33 ADS/, 34 NC_BE3/, 35 BHE/_BE2/, 36 PA/, 37 NC, 38 D_C/, 39 GPIO0, 40 GPIO1, 41 GPIO2, 42 GPIO3, 43 GPIO4, 44 Vss, 45 W_R/, 46 TT1/, 47 TT0/, 48 TBI/, 49 READYI/, 50 TEA/, 51 NC, 52 NC

Bottom pins (left to right): 53 NC, 54 NC, 55 MASTER/, 56 VDD, 57 TIP/, 58 BCLK, 59 D31, 60 D30, 61 D29, 62 D28, 63 Vss, 64 D27, 65 D26, 66 VDD, 67 D25, 68 D24, 69 DP3_ABRT/, 70 D23, 71 Vss, 72 D22, 73 D21, 74 D20, 75 D19, 76 D18, 77 D17, 78 TSTOUT, 79 Vss, 80 D16, 81 DP2, 82 VDD, 83 D15, 84 D14, 85 D13, 86 D12, 87 Vss, 88 D11, 89 D10, 90 D9, 91 D8, 92 DP1, 93 Vss, 94 D7, 95 D6, 96 D5, 97 VDD, 98 D4, 99 D3, 100 Vss, 101 D2, 102 D1, 103 NC, 104 NC

Right pins (top to bottom): 156 NC, 155 NC, 154 Vss, 153 BSY/, 152 ACK/, 151 RST/, 150 MSG/, 149 SEL/, 148 Vss, 147 C/D/, 146 REQ/, 145 I/O, 144 SD8/, 143 Vss, 142 SD9/, 141 SD10/, 140 SD11/, 139 SDIR8, 138 SDIR9, 137 SDIR10, 136 SDIR11, 135 Vss, 134 BSYDIR, 133 RSTDIR, 132 SELDIR, 131 IGS, 130 VDD, 129 TGS, 128 DIFFSENS, 127 AUTO/, 126 IRQ/, 125 SCLK, 124 HOLD/, 123 HLDAI/, 122 VDD, 121 BB/, 120 FETCH/, 119 Vss, 118 BOFF/, 117 RESET/, 116 CS/, 115 READYO/, 114 BS2, 113 BS1, 112 BS0, 111 SC1, 110 SC0, 109 DLE, 108 DP0, 107 D0, 106 NC, 105 NC

Note: *The decoupling capacitor arrangements shown in Figure 3-1 and Figure 3-2 are recommended to maximize the benefits of the internal split ground system. Capacitor values between 0.01 and 0.1 µF should provide adequate noise isolation. Because of the number of high current drivers on the 53C720, a multilayer PC board with power and ground planes is required.*

Table 3-1. Interface Signals

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Description (Slave Type, Master Type)
D(31-0)	D(31-0)	D(31-0)	D(31-0)	*Host Data Bus* (I/O, I/O) - Main data path into host memory for all Bus Modes. **Note**: In order to interface to a 16-bit bus, Bit 3 in the DCNTL register should be asserted and data lines 31 through 16 should be tied to data lines 15 through 0, respectively.
DP(2-0)	DP(2-0)	DP(1-0)	DP(2-0)	*Host Bus Data Parity* (I/O, I/O) In all Bus Modes: DP0 provides parity for D(7-0) DP1 provides parity for D(15-8) DP2 provides parity for D(23-16) **Note:** In order to interface to a 16-bit bus and to support parity, DP3 and DP2 should be tied to DP1 and DP0, respectively.
DP3_Abort/	DP3_Abort/	Abort/	DP3_Abort/	*Host Bus Data Parity* (I/O, I/O) - In all bus modes, DP3 provides parity for D(31-24). Parity is valid on all byte lanes, including unused lanes. In order to disable parity through mode, assert Bit 2 in the SCNTL0 register. DP3 becomes a hardware abort input (ABRT/) when parity through mode is disabled. When Abort is asserted, the 53C720 will finish the current transfer, then get off the bus. An abort leaves data in an undetermined state and does not flush the FIFOs.
DS/	DLE	DLE	DLE	DS/ - *Data Strobe* (Z , O) - In Bus Mode 1, this signal indicates that valid data has been or should be placed on the data lines. DLE - *Data Latch Enable* (I, I) - In Bus Modes 2, 3 and 4, this signal transparently latches read data into the 53C720 prior to an acknowledge. It is typically used when data becomes valid asynchronous to the clock. Tie this signal high if it is not used.
A(31-2)	A(31-2)	A(31-2)	A(31-2)	*Address Bus* (I, O) - In all bus modes, this signal provides an address bus to the host memory.

Table 3-1. Interface Signals (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Description (Slave Type, Master Type)
AS/	TS/	ADS/	ADS/	AS/ - *Address Strobe* (I, O) - In Bus Mode 1, this signal indicates that a valid address is on A(31-0).
				TS/ - *Transfer Start* (I, O) - In Bus Mode 2, Transfer start indicates that a bus cycle is starting and all of the status and address lines are valid.
				ADS/ - *Address Status* (I, O) - In Bus Modes 3 and 4, this signal indicates that a valid bus cycle definition and address are being driven.
R_W/	R_W/	W_R/	W_R/	*Read/Write* (I, O) - Indicates the direction of the data transfer relative to the current master.
				R_W/ - Signal for Bus Modes 1 and 2.
				W_R/ - Signal for Bus Modes 3 and 4.
BR/	BR/	HOLD/	HOLD/	BR/ - *Bus Request* (O, O) - In Bus Modes 1 and 2, this signal indicates that there is a request to use the host bus.
				HOLD/ - *Hold* (O, O) - In Bus Modes 3 and 4, this signal indicates there is a request to use the host bus.
BG/	BG/	HLDAI/	HLDAI/	BG/ - *Bus Grant* (I, I) - In Bus Modes 1 and 2, this signal indicates that the host bus has been granted to the 53C720.
				HLDAI/ - *Hold Acknowledge* (I, I) - In Bus Modes 3 and 4, this signal indicates that the previous bus master has given up the use of the host bus.
BGACK/	BB/	BB/	BB/	BGACK/ - *Bus Grant Acknowledge* (Z, I/O) - In Bus Mode 1, this signal indicates that the 53C720 or another device has taken control of the host signals.
				BB/ - *Bus Busy (wire-OR'd)* (Z, I/O) - In Bus Modes 2, 3 and 4, this signal indicates that the 53C720 or another device has taken control of the host bus signals.

Table 3-1. Interface Signals (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Description (Slave Type, Master Type)
BOFF/	BOFF/	BOFF/	BOFF/	BOFF/- *Back Off* (I, I) - In all Bus Modes, this forces the 53C720 to relinquish bus mastership at the end of the current cycle, if the proper setup timing requirements are met. When BOFF/ is deasserted, a new arbitration will take place and the cycles will resume. BOFF/ is sampled at every start cycle. During worst case operation, if timing is not met it will take the 53C720 two clocks to get off the host bus. The start cycle will become a release cycle. If BOFF/ is asserted during arbitration, the 53C720 will complete arbitration and get off the bus at the first start cycle.
BCLK	BCLK	BCLK	BCLK	*Bus Clock* (I, I) - This clock controls all host related activity in all bus modes.
RESET/	RESET/	RESET/	RESET/	*Chip Reset* (I, I) - Forces a full chip reset in all bus modes
CS/	CS/	CS/	CS/	*Chip Select* (I, I) – Selects the 53C720 as a slave I/O device in all bus modes. When CS/ is detected: Bus Mode 1: CBACK/ is deasserted. Bus Modes 2, 3 and 4: TBI/ is asserted.
IRQ/	IRQ/	IRQ/	IRQ/	*Interrupt* (O, O) - In all bus modes, this signal indicates that service is required from the host CPU.
UPSO	TT0/	TT0/	TT0/	UPSO - *User Programmable Status* (Z,O) - General purpose line in Bus Mode 1. The value in a register bit is asserted while the chip is a bus master. TT0/ - *Transfer Type Zero* (Z,O) - In Bus Modes 2, 3, and 4, this signal indicates the current bus transfer type. This bit can be programmed from a register bit (default = 0). It is asserted only when the 53C720 is bus master.
SIZ0	SIZ0	BHE/	BE2/	SIZ0 - *Transfer Size Zero* (I, O) - In Bus Modes 1 and 2, SIZ0 indicates the current transfer size in combination with SIZ1 (see table below). BHE/ - *Byte High Enable* (I, O) - In Bus Mode 3, this signal enables data transfer on the high order byte lane D(15-8). BE2/ - *Byte Enable Two* (I, O) - In Bus Mode 4, this signal enables data transfer on byte lane D(23-16).

Table 3-1. Interface Signals (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Description (Slave Type, Master Type)
SIZ1	SIZ1	NC	BE3/	SIZ1 - *Transfer Size One* (I,O) - In Bus Modes 1 and 2, SIZ1 indicates the current transfer size in combination with SIZ0, as shown in the table below. **SIZ1, SIZ0** 00 Long word (4-bytes) 01 Byte (1 byte) 10 Word (2-byte slave cycles are allowed , if word-aligned, in Little Endian mode) 11 Bus Mode 1, Illegal; Bus Mode 2, Cache line burst (since cache line bursts are not supported in slave mode, this size request will result in a standard longword slave access) BE3/- *Byte Enable Three* (I, O) - In Bus Mode 4, this signal enables data transfer on byte lane D(31-24).
A0	A0	BLE/	BE0/	A0 - *Address Line Zero* (I,O) - Address line zero to the host bus memory, used in Bus Modes 1, 2 and 3 BE0/ - *Byte Enable Zero* (I,O) - In Bus Mode 4, this signal enables data transfer on the low order byte lane D(7-0). BLE/ - Byte Low Enable (I, O) - In Bus Mode 3, this signal enables data transfer on the low order byte lane D(7-0).
A1	A1	A1	BE1/	A1 - *Address Line One* (I, O) - Address Line One to the host bus memory in Bus Modes 1, 2 and 3. BE1/ - *Byte Enable One* (I,O) - In Bus Mode 4, this signal enables data transfer on byte lane D(15-8).
STERM/	TA/	READYI/	READYI/	STERM/ - *Synchronous Cycle Termination* (I/O, I) - In Bus Mode 1, this signal acknowledges transfer to a 32-bit wide port TA/ - *Transfer Acknowledge* (I/O, I) - In Bus Mode 2, this signal acknowledges transfer to a 32-bit wide port. READYI/ - *Ready In* (I, I) - In Bus Modes 3 and 4 during master mode operation, this signal indicates that the slave device is ready to transfer data. During slave mode, this signal is monitored by the 53C720 to determine when to stop driving the bus.

Table 3-1. Interface Signals (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Description (Slave Type, Master Type)
MAC/	MAC/	MAC/	MAC/	MAC/ - *Memory Access Control* - This signal indicates if the next access will be to local memory (on-board memory) or to far memory (system memory). When MAC/=1 the memory access is to local memory. If MAC/=0 the access is to far or system memory. The default setting is zero, all accesses are far.
TSTOUT	TSTOUT	TSTOUT	TSTOUT	TSTOUT - *Test Out* - This signal is used to test the connectivity of the 53C720 signals using an "AND tree" scheme. The Test Out pin is only driven when the Test In pin is driven low; otherwise the signal is tristated.
TSTIN	TSTIN	TSTIN	TSTIN	TSTIN - *Test In* - When this pin is driven low, the 53C720 connects all inputs and outputs (excluding certain SCSI bus signals) to an "AND tree". The SCSI control signals and data lines are not connected to the "AND tree". In other words, SD15-0, SDP0-1, CD/, IO/, MSG/, REQ/, ACK/, BSY/, SEL/, ASTN/, RST/, and DIFFENS are not connected to the "AND tree". The output of the "AND tree" is connected to the Test Out pin (TSTOUT). This allows manufacturers to verify chip connectivity to the board, and to determine exactly which pins are not properly attached. When the TSTIN pin is driven low, internal pullups are enabled on all input, output and bidirectional pins, all outputs and bidirectional signals will be tristated and the TSTOUT pin will be enabled. Connectivity can be tested by driving one of the 53C720 pins low. The TSTOUT pin should respond accordingly by driving low.
BERR/	TEA/	TEA/	TEA/	BERR/ -*Bus Error Acknowledge* (O, I) - In Bus Mode 1, this indicates that a bus fault has occurred. Used with HALT/ to force a bus retry. Will be asserted on an illegal slave access.
				TEA/ - *Transfer Error Acknowledge* (O, I) - Indicates that a bus fault has occurred in Bus Modes 2, 3, or 4. Used in conjunction with TA/-READYI/ to force a bus retry. Will be asserted on an illegal slave access
HALT/	TIP/	TIP/	TIP/	HALT/ (Z, I) - Input ONLY in Bus Mode 1, used with BERR/ to indicate a bus retry cycle.
				TIP/ - *Transfer in Progress* (Z, O) - Output signal for Bus Modes 2, 3 and 4, indicating that bus activity is in progress.

Table 3-1. Interface Signals (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Description (Slave Type, Master Type)
SLACK/	SLACK/	READYO/	READYO/	SLACK/ - *Slave Acknowledge* (O, O) - Asserted in Bus Modes 1 and 2 to indicate the internal end of a valid slave mode cycle. The external slave cycle ends when the 53C720 observes either STERM/-TA/ or BERR/-TEA. READYO/ -*Ready Out* (O, O) - Asserted in Bus Modes 3 and 4 to indicate the end of a slave mode cycle.
FC(2-0)	TM(2-0)	FC(2-0)	FC(2-0)	*Function Codes and Transfer Modifier* For All Bus Modes: FC0-TM0 (Z, O) - Indicates the status of the current bus cycle. FC0-TM0 = 1 - Indicates data space; it is the default for all transfers. FC0-TM0 = 0 - Indicates program space. It may be optionally selected when setting the Program Data (PD) bit. FC1-TM1 (Z,O) - User Definable from register bits. FC2-TM2 (Z,O) - User definable from register bits. **Note**: If DCNTL (bit 6) is asserted, FC0 becomes a continuously enabled, general purpose output in all Bus Modes. FC1 becomes a continuously enabled, general purpose output in all bus modes, and FC2 becomes PA/ (Preview of Address). PA/ (I, I) -*Preview of Address* - Input signal only, used to tell the 53C720 that the system is ready for the next address/value and byte enable signal
SC(1-0)	SC(1-0)	SC(1-0)	SC(1-0)	SC - *Snoop Control* (Z(O), O) - Indicates the bus snoop ing level in all bus modes. The bits are user programmable through register bits. They are asserted when the 53C720 is bus master. SC(1-0) may be optionally used as pure outputs, active in both master and slave modes.
MASTER/	MASTER/	MASTER/	MASTER/	*Master Status* (O, O) - Driven low when the 53C720 becomes bus master. This signal is valid in all bus modes. This signal is driven at all times except when the 53C720 is in Z Mode. Therefore, do not tie these signals together.
FETCH/	FETCH/	FETCH/	FETCH/	*Fetching Op Code* (O, O) - In all bus modes, this signal indicates that the next bus request will be for an op code fetch.

Table 3-1. Interface Signals (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Description (Slave Type, Master Type)
CBREQ/	TT1/	TT1/	CBREQ/	CBREQ/ - *Cache Burst Request* (Z, O) - In Bus Modes 1 and 4, Cache Burst Request indicates an attempt to execute a line transfer of four long words. CBREQ/ is valid in Mode 4 only when 386 Cache mode is enabled (Cache 386 bit, CTEST0 register).
				TT1/ - Transfer Type Bit One (Z, O) - Transfer Type Bit One is a three-state output line indicating the current bus transfer type in all four bus modes TT1/ is not valid in Bus Mode 4 if Cache 386 mode is enabled. This bit can be programmed from bit 1 in the CTEST0 register. It is only asserted when the 53C720 is bus master.
CBACK/	TBI/	TBI/	TBI/	CBACK/ - *Cache Burst Acknowledge* (O, I) - In Bus Mode 1, this signal indicates that the memory system or 53C720 can handle a burst request. In slave mode this signal is deasserted in response to CS/.
				TBI/ - *Transfer Burst Inhibit* (O, I) - In Bus Modes 2, 3 and 4, Transfer Burst Inhibit indicates that the memory or the 53C720 cannot handle a burst request at this time. In slave mode this signal is asserted in response to CS/.
BS(2-0)	BS(2-0)	BS(2-0)	BS(2-0)	*Bus Mode Select* (I, I) − These signals are active in all four bus modes. They select between Motorola/Intel (BS2), Big/ Little Endian (BS1) and 386sx/_030 and 386dx/_040(BS0).

BS2	BS1	BS0	Bus Mode
0	0	0	80386DX-like, Little Endian, Bus Mode 4
0	0	1	80386SX-like, Little Endian, Bus Mode 3
0	1	0	80386DX-like, Big Endian, Bus Mode 4
0	1	1	Reserved
1	0	0	68040-like, Little Endian, Bus Mode 2
1	0	1	68030-like, Little Endian, Bus Mode 1
1	1	0	68040-like, Big Endian, Bus Mode 2
1	1	1	68030-like, Big Endian, Bus Mode 1

Table 3-1. Interface Signals (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Description (Slave Type, Master Type)
AUTO/	AUTO/	AUTO/	AUTO/	*SCRIPTS Autostart Mode* (I, I) – In all bus modes, this signal selects between automatic SCRIPTS and manual SCRIPTS start modes.
				AUTO/ = 0 Auto start. The DMA SCRIPT pointer register (DSP) will point to an address of all zeroes following a chip reset. This address is the starting address of the SCRIPT instructions. The SCRIPTS will automatically be fetched and executed until an interrupt instruction occurs.
				AUTO/ = 1 Manual start. The DMA SCRIPT pointer register (DSP) must be written to so that it points to the starting address of the SCRIPT instructions. The SCRIPTS will automatically be fetched and executed until an interrupt condition occurs.
GPI(3-0)	GPI(3-0)	GPI(3-0)	GPI(30)	*General Purpose Input* (I, I) – In all bus modes, this signal detects the input signal of the connected device. It can read the 53C720's ID or other configuration information.
GPO	GPO	GPO	GPO	*General Purpose Output* (O, O) - In all bus modes, outputs a user-selected output signal. This feature can be used to enable attached RAM, ROM, LEDs, etc.
DIFFSENS	DIFFSENS	DIFFSENS	DIFFSENS	*Differential Sense* (I, I) – This pin detects the presence of a single-ended device on a differential system. When using external differential transceivers and a zero is detected on this pin, all chip SCSI outputs will be tristated to avoid damage to the transceivers. When running in single-ended mode, this pin should be tied high. The normal value of this pin is 1.
SCLK	SCLK	SCLK	SCLK	*SCSI Clock* (I, I) - SCLK is used to derive all SCSI-related timings. The speed of this clock will be determined by the application's requirements; in some applications SCLK and BCLK may be tied to the same source.
SDATA/	SDATA/	SDATA/	SDATA/	*SCSI Data* (I/O, I/O) - These open collector signals include the following data lines and parity signals for all Bus Modes.

SD15-0/	16-bit SCSI data bus
SDP0/	SCSI data parity bit (bits 7-0)

SDP1/   SCSI data parity bit (bits 15-8)

Table 3-1. Interface Signals (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Description (Slave Type, Master Type)
SCTRL/	SCTRL/	SCTRL/	SCTRL/	Open Collector *SCSI Control* signals (I/O, I/O)
				C_D/ SCSI phase line, command/data
				I_O/ SCSI phase line, input/output
				MSG/ SCSI phase line, message
				REQ/ Data handshake signal from target device
				ACK/ Data handshake signal from initiator device
				★ BSY/ SCSI bus arbitration signal, signal busy
				★ SEL/ SCSI bus arbitration signal, select device
				ATN/ Attention, the initiator is requesting a message out phase
				★ RST/ SCSI bus reset
				★ Input only in differential mode.
SDIR(15-0)	SDIR(15-0)	SDIR(15-0)	SDIR(15-0)	*Differential Support Lines* (O, O) - Driver direction control for SCSI data lines.
SDIRP0	SDIRP0	SDIRP0	SDIRP0	*Differential Support Line* - (O, O) Driver direction control for SCSI parity signal (bits (7-0)).
SDIRP1	SDIRP1	SDIRP1	SDIRP1	*Differential Support Line* (O, O) - Driver direction control for SCSI parity signal (bits (15-8)).
BSYDIR	BSYDIR	BSYDIR	BSYDIR	*Differential Support Line* (O, O) - Driver enable control for SCSI BSY/ signal.
SELDIR	SELDIR	SELDIR	SELDIR	*Differential Support Line* (O, O) - Driver enable control for SCSI SEL/ signal.

RSTDIR RSTDIR   RSTDIR   RSTDIR   *Differential Support Line* (O, O) - Driver enable control for SCSI RST/ signal.

Table 3-1. Interface Signals (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Description (Slave Type, Master Type)
IGS	IGS	IGS	IGS	*Differential Support Line* (O, O) - Direction control for initiator driver group.
TGS	TGS	TGS	TGS	*Differential Support Line* (O, O) - Direction control for target driver

Chapter Four

Registers

This section contains descriptions of all NCR 53C720 registers. Table 4-1 summarizes the NCR 53C720 register set. Figure 4-1, the register map, lists registers by both their Big and Little Endian addresses. The Big Endian address for each register is shown in parentheses. The terms "set" and "assert" are used to refer to bits that are programmed to a binary one. Similarly, the terms "deassert," "clear" and "reset" are used to refer to bits that are programmed to a binary zero. Reserved bits should always be written to zero; *mask all information read from them.* Reserved bit functions may be changed at any time. Unless otherwise indicated, all bits in registers are active high, i.e., the feature is enabled by setting the bit. The bottom of every register diagram shows the default register values, which are enabled after the chip is powered on or reset. Registers can be addressed as bytes, words or longwords. Other access sizes will result in bus errors. *The only register that the host CPU can access while the NCR 53C720 is executing SCRIPTS is the ISTAT register; attempts to access other registers will interfere in the operation of the chip.* However, all registers are accessible via SCRIPTS.

Table 4-1. NCR 53C720 Register Addresses and Descriptions

Little Endian Address	Big Endian Address	Read/Write	Label	Description
00	03	R/W	SCNTL0	SCSI Control 0
01	02	R/W	SCNTL1	SCSI Control 1
02	01	R/W	SCNTL2	SCSI Control 2
03	00	R/W	SCNTL3	SCSI Control 3
04	07	R/W	SCID	SCSI Chip ID
05	06	R/W	SXFER	SCSI Transfer
06	05	R/W	SDID	SCSI Destination ID
07	04	R/W	GPREG	General Purpose
08	0B	R/W	SFBR	SCSI First Byte Received
09	0A	R/W	SOCL	SCSI Output Control Latch
0A	09	R	SSID	SCSI Selector ID
0B	08	R/W	SBCL	SCSI Bus Control Lines
0C	0F	R	DSTAT	DMA Status
0D	0E	R	SSTAT0	SCSI Status 0
0E	0D	R	SSTAT1	SCSI Status 1
0F	0C	R	SSTAT2	SCSI Status 2
10-13	10-13	R/W	DSA	Data Structure Address
14	17	R/W	ISTAT	Interrupt Status
18	1B	R/W	CTEST0	Chip Test 0

Table 4-1. NCR 53C720 Register Addresses and Descriptions (Continued)

Little Endian Address	Big Endian Address	Read/Write	Label	Description
19	1A	R	CTEST1	Chip Test 1
1A	19	R	CTEST2	Chip Test 2
1B	18	R	CTEST3	Chip Test 3
1C-1F	1C-1F	R/W	TEMP	Temporary stack
20	23	R/W	DFIFO	DMA FIFO
21	22	R/W	CTEST4	Chip Test 4
22	21	R/W	CTEST5	Chip Test 5
23	20	R/W	CTEST6	Chip Test 6
24-26	25-27	R/W	DBC	DMA Byte Counter
27	24	R/W	DCMD	DMA Command
28-2B	28-2B	R/W	DNAD	DMA Next Address for Data
2C-2F	2C-2F	R/W	DSP	DMA SCRIPTS Pointer
30-33	30-33	R/W	DSPS	DMA SCRIPTS Pointer Save
34-37	34-37	R/W	SCRATCH A	General Purpose Scratch Pad A
38	3B	R/W	DMODE	DMA Mode
39	3A	R/W	DIEN	DMA Interrupt Enable
3A	39	R/W	DWT	DMA Watchdog Timer
3B	38	R/W	DCNTL	DMA Control
3C-3F	3C-3F	R	ADDER	Sum output of internal adder
40	43	R/W	SIEN0	SCSI Interrupt Enable 0
41	42	R/W	SIEN1	SCSI Interrupt Enable 1
42	41	R	SIST0	SCSI Interrupt Status 0
43	40	R	SIST1	SCSI Interrupt Status 1
44	47	R/W	SLPAR	SCSI Longitudinal Parity
45	46	R	SWIDE	SCSI Wide Residue Data
46	45	R/W	MACNTL	Memory Access Control
47	44	R/W	GPCNTL	General Purpose Control
48	4A	R/W	STIME0	SCSI Timer 0
49	4B	R/W	STIME1	SCSI Timer 1
4A	49	R/W	RESPID0	Response ID0
4B	48	R/W	RESPID1	Response ID1
4C	4F	R	STEST0	SCSI Test 0
4D	4E	R	STEST1	SCSI Test 1
4E	4D	R/W	STEST2	SCSI Test 2
4F	4C	R/W	STEST3	SCSI Test 3
50-51	52-53	R	SIDL	SCSI Input Data Latch
54-55	56-57	R/W	SODL	SCSI Output Data Latch
58-59	5A-5B	R	SBDL	SCSI Bus Data Lines
5C-5F	5C-5F	R/W	SCRATCH B	General Purpose Scratch Pad B

Figure 4-1. NCR 53C720 Register Address Map

Big Endian Mode →					SCRIPTs and Little Endian ← Mode
00	SCNTL3	SCNTL2	SCNTL1	SCNTL0	00
04	GPREG	SDID	SXFER	SCID	04
08	SBCL	SSID	SOCL	SFBR	08
0C	SSTAT2	SSTAT1	SSTAT0	DSTAT	0C
10	DSA				10
14	RESERVED			ISTAT	14
18	CTEST3	CTEST2	CTEST1	CTEST0	18
1C	TEMP				1C
20	CTEST6	CTEST5	CTEST4	DFIFO	20
24	DCMD	DBC			24
28	DNAD				28
2C	DSP				2C
30	DSPS				30
34	SCRATCH A				34
38	DCNTL	DWT	DIEN	DMODE	38
3C	ADDER				3C
40	SIST1	SIST0	SIEN1	SIEN0	40
44	GPCNTL	MACNTL	SWIDE	SLPAR	44
48	RESPID1	RESPID0	STIME1	STIME0	48
4C	STEST3	STEST2	STEST1	STEST0	4C
50	RESERVED		SIDL		50
54	RESERVED		SODL		54
58	RESERVED		SBDL		58
5C	SCRATCHB				5C

Register 00 (03)
SCSI Control Zero (SCNTL0)
Read/Write

ARB1	ARB0	START	WATN/	EPC	EPG	AAP	TRG
7	6	5	4	3	2	1	0

Default>>
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7   ARB1 (Arbitration mode bit 1)

Bit 6   ARB0 (Arbitration mode bit 0)

ARB1	ARB0	Arbitration Mode
0	0	Simple arbitration
0	1	Reserved
1	0	Reserved
1	1	Full arbitration, selection or reselection

Simple Arbitration

1) The NCR 53C720 waits for a bus free condition to occur.

2) It asserts BSY/ and its SCSI ID (contained in the SCID register) onto the SCSI bus If the SEL/ signal is asserted by another SCSI device, the NCR 53C720 will deassert BSY/, deassert its ID and set the Lost Arbitration bit (bit 3) in the SSTAT0 register.

3) After an arbitration delay, the CPU should read the SBDL register to check if a higher priority SCSI ID is present. If no higher priority ID bit is set, and the Lost Arbitration bit is not set, the NCR 53C720 has won arbitration.

4) Once the NCR 53C720 has won arbitration, SEL must be asserted via the SOCL for a bus clear plus a bus settle delay (1.2 μs) before a low level selection can be performed.

Full Arbitration, Selection/Reselection

1) The NCR 53C720 waits for a bus free condition.

2) It asserts BSY/ and its SCSI ID (the highest priority ID stored in the SCID register) onto the SCSI bus.

3) If the SEL/ signal is asserted by another SCSI device or if the NCR 53C720 detects a higher priority ID, the NCR 53C720 will deassert BSY/, deassert its ID, and wait until the next bus free state to try arbitration again.

4) The NCR 53C720 repeats arbitration until it wins control of the SCSI bus. When it has won, the Won Arbitration bit is set in the SSTAT0 register, bit 2.

5) The NCR 53C720 performs selection by asserting the following onto the SCSI bus: SEL/, the target's ID (stored in the SDID register) and the NCR 53C720's ID (the highest priority ID stored in the SCID register).

6) After a selection is complete, the Function Complete bit is set in the SIST0 register, bit 6.

7) If a selection time-out occurs, the Selection Time-out bit is set in the SIST1 register, bit 2.

Bit 5   START (Start sequence)
When this bit is set, the NCR 53C720 will start the arbitration sequence indicated by the Arbitration Mode bits. The Start Sequence bit is used in low level mode; when executing SCSI SCRIPTS, this bit is controlled by the SCRIPTS processor. An arbitration sequence should not be started if the connected bit in the SCNTL1 register, bit 4, indicates that NCR 53C720 is already connected to the SCSI bus.

This bit is automatically cleared when the arbitration sequence is complete. If a sequence is aborted, bit 4 in the SCNTL1 register should be checked to verify that the NCR 53C720 did not connect to the SCSI bus.

Bit 4   WATN (Select with ATN/ on a start sequence)

When this bit is set and the NCR 53C720 is in initiator mode, the SCSI ATN/ signal will be asserted during NCR 53C720 selection of a target device. This is to inform the target that the NCR 53C720 has a message to send. If a selection time-out occurs while attempting to select a target device, ATN/ will be deasserted at the same time SEL/ is deasserted.

When this bit is clear, the ATN/ signal will not be asserted during selection.

This bit is controlled by the SCRIPTS processor during SCRIPTS execution, but it may be set manually in low level mode.

Bit 3   EPC (Enable parity checking)

When this bit is set, the SCSI data bus is checked for odd parity when data is received from the SCSI bus in either initiator or target mode. The host data bus is checked for odd parity if bit 2, the Enable Parity Generation bit, is cleared. Host data bus parity is checked as data is loaded into the SODL register when sending SCSI data in either initiator or target mode. If a parity error is detected, bit 0 of the SSTAT0 register is set and an interrupt may be generated.

If the NCR 53C720 is operating in initiator mode and a parity error is detected, ATN/ can optionally be asserted, but the transfer continues until the target changes phase.

When this bit is cleared, parity errors are not reported.

Bit 2   EPG (Enable parity generation/parity through)

When this bit is set, SCSI parity will be generated by the NCR 53C720. The host data bus parity lines DP(3-0) are ignored and should not be used as parity signals. When this bit is cleared, the parity present on the host data parity lines will flow through the NCR

53C720's internal FIFOs and be driven onto the SCSI bus when sending data (if the host bus is set to even parity, it is changed to odd before it is sent to the SCSI bus).

This bit is set to enable the DP3_ABRT/ pin to function as an abort input (ABRT/).

Bit 1   AAP (Assert ATN/ on parity error)

When this bit is set, the NCR 53C720 automatically asserts the SCSI ATN/ signal upon detection of a parity error. ATN/ is only asserted in initiator mode. The ATN/ signal is asserted before deasserting ACK/ during the byte transfer with the parity error. The Enable Parity Checking bit must also be set for the NCR 53C720 to assert ATN/ in this manner. The following parity errors can occur:

1) A parity error detected on data received from the SCSI bus.

2) A parity error detected on data transferred to the NCR 53C720 from the host data bus.

If the Assert ATN/ on Parity Error bit is cleared or the Enable Parity Checking bit is cleared, ATN/ will not be automatically asserted on the SCSI bus when a parity error is received.

Bit 0   TRG (Target mode)

This bit determines the default operating mode of the NCR 53C720. The user must manually set target or initiator mode. This can be done using the SCRIPTS language (SET target or CLEAR target).

When this bit is set, the chip is a target device by default. When the target mode bit is cleared, the NCR 53C720 is an initiator device by default.

Register 01 (02)
SCSI Control One (SCNTL1)
Read/Write

EXC	ADB	DHP	CON	RST	AESP	IARB	SST
7	6	5	4	3	2	1	0

Default>>

| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7   EXC (Extra clock cycle of data setup)

When this bit is set, an extra clock period of data setup is added to each SCSI send data transfer. The extra data setup time can provide additional system design margin, though it will affect the SCSI transfer rates. Clearing this bit disables the extra clock cycle of data setup time.

Bit 6   ADB (Assert SCSI data bus)

When this bit is set, the NCR 53C720 drives the contents of the SCSI Output Data Register (SODL) onto the SCSI data bus. When the NCR 53C720 is an initiator, the SCSI I/O signal must be inactive to assert the SODL contents onto the SCSI bus. The low order data and parity signal will always be asserted onto the SCSI bus, whereas the high order data and parity signal will only be asserted onto the SCSI bus if the Enable Wide SCSI bit (SCNTL3, bit 3) is asserted and a data phase is specified by the data phase signals. When the NCR 53C720 is a target, the SCSI I/O signal must be active for the SODL contents to be asserted onto the SCSI bus. The contents of the SODL register can be asserted at any time, even before the NCR 53C720 is connected to the SCSI bus. This bit should be cleared when executing SCSI SCRIPTS. It is normally used only for diagnostics testing or operation in low level mode.

Bit 5   DHP   (Disable Halt on Parity Error or ATN) (Target Only)

The DHP bit is only defined for target mode operation. When this bit is cleared, the NCR 53C720 halts the SCSI data transfer when a parity error is detected or when the ATN/ signal is asserted. If ATN/ or a parity error is received in the middle of a data transfer, the NCR 53C720 may transfer up to three additional bytes (or words, if wide SCSI is enabled) before halting to synchronize between internal core cells. During synchronous operation, the NCR 53C720 transfers data until there are no outstanding synchronous offsets. If the NCR 53C720 is receiving data, any data residing in the SCSI or DMA FIFOs is sent to memory before halting. While sending data in target mode with pass parity enabled, the byte with the parity error will not be sent across the SCSI bus.

When this bit is set, the NCR 53C720 does not halt the SCSI transfer when ATN/ or a parity error is received.

Bit 4   CON (Connected)

This bit is automatically set any time the NCR 53C720 is connected to the SCSI bus as an initiator or as a target. It will be set after successfully completing arbitration or when the NCR 53C720 has responded to a bus initiated selection or reselection. It will also be set after successfully completing simple arbitration when operating in low level mode. When this bit is clear, the NCR 53C720 is not connected to the SCSI bus.

The CPU can force a connected or disconnected condition by setting or clearing this bit. This feature would be used primarily during loopback mode.

Bit 3   RST (Assert SCSI RST/ signal)
Setting this bit asserts the SCSI RST/ signal. The RST/ output remains asserted until this bit is cleared. The 25 µs minimum assertion time defined in the SCSI specification must be timed out by the controlling microprocessor or a SCRIPTS loop. In differential mode, RST/ becomes an input, and setting this bit causes RSTDIR to be asserted.

Bit 2   AESP (Assert even SCSI parity (force bad parity))
When this bit is set and the Enable Parity Generation bit is set (bit 2) in the SCNTL0 register, the NCR 53C720 asserts even parity. It forces a SCSI parity error on each byte sent to the SCSI bus from the NCR 53C720. If parity checking is enabled, then the NCR 53C720 checks data received for odd parity. This bit is used for diagnostic testing and should be clear for normal operation. It can be used to generate parity errors to test error handling functions.

Bit 1   IARB   (Immediate Arbitration)
Setting this bit will cause the SCSI core to immediately begin arbitration once a Bus Free phase is detected following an expected SCSI disconnect. This bit is useful for multi-threaded applications. The ARB1-0 bits in SCNTL0 should be set for full arbitration and selection before setting Immediate Arbitration.

Arbitration will be re-tried until won. At that point, the NCR 53C720 will hold BSY and SEL asserted, and wait for a select or reselect sequence to be requested. The Immediate Arbitration bit will be reset automatically when the selection or reselection sequence is completed, or times out.

An unexpected disconnect condition will clear IARB without attempting arbitration. See the SCSI Disconnect Unexpected bit (SCNTL2 bit 7) for more information on expected versus unexpected disconnects.

An immediate arbitration sequence can be aborted. First, the abort bit in the SCRIPTS processor registers should be set. Then one of two things will eventually happen:

1) The Won Arbitration bit (SSTAT0 bit 2) will be asserted. In this case, the Immediate Arbitration bit needs to be reset. This will complete the abort sequence and disconnect the NCR 53C720 from the SCSI bus. If it is not acceptable to go to Bus Free phase immediately following the arbitration phase, a low level selection may instead be performed.

2) The abort will complete because the NCR 53C720 loses arbitration. This can be detected by the Immediate Arbitration bit being deasserted. The Lost Arbitration bit (SSTAT0 bit 3) should not be used to detect this condition. No further action needs to be taken in this case.

Bit 0   SST   (Start SCSI Transfer)
This bit is automatically set during SCRIPTS execution, and should not be used. It causes the SCSI core to begin a SCSI transfer, including REQ/ACK handshaking. The determination of whether the transfer is a send or receive is made according to the value written to the I/O bit in SOCL. This bit is self-resetting. This bit should not be set for low level operation.

Register 02 (01)
SCSI Control Register Two (SCNTL2)
Read/Write

SDU	CHM	RES	RES	WSS	RES	RES	WSR
7	6	5	4	3	2	1	0

Default>>>

0	0	X	X	0	X	X	0

Bit 7   SDU   (SCSI Disconnect Unexpected)
   When this bit is set, the SCSI core is not
   expecting the SCSI bus to enter the Bus Free
   phase. If it does, an unexpected disconnect
   error will be generated (see the Unexpected
   Disconnect bit in the SIST0 register, bit 2).

   During normal SCRIPTS mode operation,
   this bit is set automatically whenever the SCSI
   core is reselected, or successfully selects
   another SCSI device. The SDU bit should be
   reset with a register write before the SCSI core
   expects a disconnect to occur, normally prior
   to sending an Abort, Abort Tag, Bus Device
   Reset, Clear Queue or Release Recovery
   message, or before deasserting ACK after
   receiving a Disconnect command or Com-
   mand Complete message.

Bit 6   CHM   (Chained Mode)
   This bit determines whether or not the SCSI
   core is programmed for chained SCSI mode.
   This bit is automatically set by the Chained
   Block Move (CHMOV) SCRIPTS instruction
   and is automatically cleared by the Block
   Move SCRIPTS instruction (MOVE).

   Chained mode is primarily used to transfer
   consecutive wide data blocks. Using chained
   mode facilitates partial receive transfers and
   allows correct partial send behavior. When this
   bit is set and a data transfer ends on an odd
   byte boundary, the NCR 53C720 will store
   the last byte in the SCSI Wide Residue Data
   Register during a receive operation or in the

SCSI Output Data Latch register during a
send operation. This byte will be combined
with the first byte from the subsequent transfer
so that a wide transfer can be completed.

Bits 5-4   Reserved

Bit 3   WSS   (Wide SCSI Send)
   When read, this bit returns the value of the
   Wide SCSI Send (WSS) flag. Asserting this bit
   will clear the WSS flag. This clearing function
   is self-resetting.

   When the WSS flag is high following a wide
   SCSI send operation, the SCSI core is holding
   a byte of "chain" data in the SODL register.
   This data will become the first low-order byte
   sent when "married" with a high-order byte
   during a subsequent data send transfer.

   Performing a SCSI receive operation will clear
   this bit. Also, performing any non-wide trans-
   fer will clear this bit.

Bits 2-1   Reserved

Bit 0   WSR   (Wide SCSI Receive)
   When read, this bit returns the value of the
   Wide SCSI Receive (WSR) flag. Asserting this
   bit will clear the WSR flag. This clearing
   function is self-resetting.

   The WSR flag indicates that the SCSI core
   received data from the SCSI bus, detected a
   possible partial transfer at the end of a chained
   or non-chained block move command, and
   temporarily stored the high-order byte in the
   SWIDE register rather than passing the byte
   out the DMA channel. The hardware uses the
   WSR status flag to determine what behavior
   must occur at the start of the next data receive
   transfer. When the flag is set, the stored data
   in SWIDE may be "residue" data, valid data
   for a subsequent data transfer, or overrun
   data. The byte may be read as normal data by
   starting a data receive transfer.

   Performing a SCSI send operation will clear
   this bit. Also, performing any non-wide trans-
   fer will clear this bit.

Register 03 (00)
SCSI Control Three (SCNTL3)
Read/Write

RES	SCF2	SCF1	SCF0	EWS	CCF2	CCF1	CCF0
7	6	5	4	3	2	1	0

Default>>

| X | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7   Reserved

Bits 6-4   SCF2-0   (Synchronous Clock Conversion Factor)
These bits select a factor by which the frequency of SCLK is divided before being presented to the synchronous SCSI control logic. They should be written to the same value as the Clock Conversion Factor bits below unless fast SCSI operation is desired. See the table under the description of bits 7-5 of the SCSI Transfer register for the valid combinations.

Bit 3   EWS   (Enable Wide SCSI)
When this bit is deasserted all information transfer phases are assumed to be eight bits, transmitted on SD7-0/, SDP0/. When this bit is asserted, data transfers are done 16 bits at a time with the least significant byte on SD7-0/, SDP/ and the most significant byte on SD15-8/, SDP1/. Command, status, and message phases remain eight bits.

Bits 2-0 CCF2-0   (Clock Conversion Factor)
These bits select a factor by which the frequency of SCLK is divided before being presented to the SCSI core. The bits are encoded as follows. All other combinations are reserved and should never be used. Also note that the synchronous portion of the SCSI core can be run at a different clock rate for fast SCSI. See the synchronous clock conversion factor bits above.

CCF2	CCF1	CCF0	Factor	SCSI Clock Frequency (MHz)
0	0	0	SCLK / 3	50.01-66
0	0	1	SCLK / 1	16.67-25
0	1	0	SCLK/ 1.5	25.01-37
0	1	1	SCLK / 2	37.51-50
1	0	0	SCLK / 3	50.01-66
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Reserved	

Note: It is important that these bits be set to the proper values to guarantee that the NCR 53C720 meets the SCSI timings as defined by the ANSI specification.

Register 04 (07)
SCSI Chip ID (SCID)
Read/Write

RES	RRE	SRE	RES	ID3	ID2	ID1	ID0
7	6	5	4	3	2	1	0

Default>>

X	0	0	X	0	0	0	0

Bit 7 Reserved

Bit 6 RRE (Enable Response to Reselection)
When this bit is set, the NCR 53C720 is enabled to respond to bus-initiated reselection at the chip ID in the RESPID0 and RESPID1 registers. Note that the NCR 53C720 will not automatically reconfigure itself to initiator mode as a result of being reselected.

Bit 5 SRE (Enable Response to Selection)
When this bit is set, the NCR 53C720 is enabled to respond to bus-initiated selection at the chip ID encoded in the RESPID0 and RESPID1 registers. Note that the NCR 53C720 will not automatically reconfigure itself to target mode as a result of being selected.

Bit 4 Reserved

Bits 3-0 Encoded 53C720 Chip SCSI ID
These bits are used to store the NCR 53C720 encoded SCSI ID. This is the ID which the chip will assert when arbitrating for the SCSI bus. The priority of the sixteen possible IDs, in descending order is:

Highest   Lowest

7 6 5 4 3 2 1 0 15 14 13 12 11 10 9 8

Register 05 (06)
SCSI Transfer (SXFER)
Read/Write

TP2	TP1	TP0	RES	MO3	MO2	MO1	MO0
7	6	5	4	3	2	1	0

Default>>>

0	0	0	X	0	0	0	0

Note: When using Table Indirect I/O commands, bits 7-5 and 3-0 of this register will be loaded from the I/O data structure.

Bits 7-5   TP2-0 (SCSI Synchronous Transfer Period)
These bits determine the SCSI synchronous transfer period used by the NCR 53C720 when sending synchronous SCSI data in either initiator or target mode. See the following table:

TP2	TP1	TP0	XFERP
0	0	0	4
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	9
1	1	0	10
1	1	1	11

The synchronous transfer period the NCR 53C720 should use when transferring SCSI data is found as in the following example: The NCR 53C720 is interfaced to a hard disk which can transfer data at 10 MB/s synchronously. The NCR 53C720's SCLK is running at 40 MHz. The synchronous transfer period (SXFERP) is found as follows:

SXFERP = Period/SSCP + ExtCC

Period = 1 ÷ Frequency = 1 ÷ 10 MB/s = 100 ns

SSCP = 1 ÷SSCF = 1 ÷ 40 MHz = 25 ns

(This SCSI synchronous core clock is determined in SCNTL3 bits 6-4).

ExtCC = 1 if SCNTL1 bit 7 is asserted and the NCR 53C720 is sending data.

(ExtCC = 0 if the NCR 53C720 is receiving data.)

SXFERP = 100 ÷ 25 = 4

Key: SXFERP = Synchronous transfer period

SSCP = SCSI Synchronous core period

SSCF = SCSI Synchronous core frequency

ExtCC = Extra clock cycle of data setup

Examples of synchronous transfer periods for SCSI-1 transfer rates.

CLK (MHz)	SCSI CLK ÷ SCNTL3 bits 6-4	XFERP	Synch Transfer Period (ns)	Synch Transfer Rate (MB/s)
66.67	÷ 3	4	180	5.55
66.67	÷ 3	5	225	4.44
50	÷ 2	4	160	6.25
50	÷ 2	5	200	5
40	÷ 2	4	200	5
37.50	÷ 1.5	4	160	6.25
33.33	÷ 1.5	4	180	5.55
25	÷ 1	4	160	6.25
20	÷ 1	4	200	5
16.67	÷ 1	4	240	4.17

Example transfer periods for fast SCSI-2 transfer rates.

CLK (MHz)	SCSI CLK ÷ SCNTL bits 6-4	XFERP	Synch Transfer Period (ns)	Synch Transfer Rate (MB/s)
66.67	÷ 1.5	4	90	11.11*
66.67	÷ 1.5	5	112.5	8.88
50	÷ 1	4	80	12.5*
50	÷ 1	5	100	10.0
40	÷ 1	4	100	10.0
37.50	÷ 1	4	106.67	9.375
33	÷ 1	4	120	8.33
25	÷ 1	4	160	6.25
20	÷ 1	4	200	5
16.67	÷ 1	4	240	4.17

*Violates SCSI specifications. Slower rates are achieved by using larger XFERP values and/or different SCLK prescale values.

Bit 4   Reserved

Bits 3-0   MO3-MO0 (Max SCSI synchronous offset)

These bits describe the maximum SCSI synchronous offset used by the NCR 53C720 when transferring synchronous SCSI data in either initiator or target mode. The following table describes the possible combinations and their relationship to the synchronous data offset used by the NCR 53C720. These bits determine the NCR 53C720's method of transfer for Data In and Data Out phases only; all other information transfers will occur asynchronously.

MO3	MO2	MO1	MO0	Synchronous Offset
0	0	0	0	0 – Asynchronous
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	X	X	1	Reserved
1	X	1	X	Reserved
1	1	X	X	Reserved

Register 06 (05)
SCSI Destination ID (SDID)
Read/Write

RES	RES	RES	RES	ID3	ID2	ID1	ID0
7	6	5	4	3	2	1	0

Default>>>

X	X	X	X	0	0	0	0

Bits 7-4   Reserved

Bits 3-0   Encoded destination SCSI ID bits 3-0

Writing these bits sets the SCSI ID of the intended initiator or target during SCSI reselection or selection phases respectively. When executing SCSI SCRIPTS, the SCRIPTS processor writes the destination SCSI ID to this register. The SCSI ID is defined by the user in a SCSI SCRIPTS Select or Reselect instruction. The value written should be the binary-encoded ID value. The priority of the 16 possible IDs, in descending order, is:

Highest   Lowest

7 6 5 4 3 2 1 0 15 14 13 12 11 10 9 8

Register 07 (04)
Read/Write General Purpose (GPREG)
Read/Write

RES 7	RES 6	RES 5	GPIO4 4	GPIO3 3	GPIO2 2	GPIO1 1	GPIO0 0

Default>>>

X	X	X	0	X	X	X	X

Bits 7-5 Reserved

Bits 4-0 GPIO4-0   (General Purpose Inputs/Outputs)

These bits allow the NCR 53C720 to detect the input signals of a connected device. The general purpose inputs can be used to sense the NCR 53C720 chip ID or board configuration at power up. A Register-to-Register Move instruction may be used to move the sensed value into the appropriate register. These are live signals; if the pin is changing, the data is also changing. The bit values in the General Purpose Control Register (47h) determine whether these bits are inputs or outputs.

Bits 3-0 power up as inputs, and Bit 4 powers up as an output. The general purpose output feature may be used to enable attached ROM, RAM, LEDs, or other components on a NCR 53C720 board.

Note: The input pins all have internal pull-ups.

Register 08 (0B)
SCSI First Byte Received (SFBR)
Read/Write

7	6	5	4	3	2	1	0

Default>>>

0	0	0	0	0	0	0	0

Bits 7-0 1B7-1B0 (First byte received)

This register contains the first byte received in any asynchronous information transfer phase. For example, when the NCR 53C720 is operating in initiator mode, this register contains the first byte received in Message In, Status Phase, Reserved In and Data In.

When a Block Move Instruction is executed for a particular phase, the first byte received is stored in this register - even if the present phase is the same as the last phase. The first byte value received for a particular input phase is not valid until after a Move instruction is executed.

This register is also the accumulator for register read-modify-writes with the SFBR as the destination. This allows bit testing after an operation.

The SFBR is not writable via the CPU, and therefore not by a Memory Move. However, it can be loaded via SCRIPTS Read/Write operations. To load the SFBR with a byte stored in system memory, the byte must first be moved to an intermediate NCR 53C720 register (such as the SCRATCH register), and then to the SFBR.

This register will also hold the state of the lower eight bits of the SCSI data bus during a selection or reselection, unless the COM bit in the DCNTL register is set.

Register 09 (0A)
SCSI Output Control Latch (SOCL)
Read /Write

REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
7	6	5	4	3	2	1	0

Default>>>
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7 REQ (Assert SCSI REQ/ signal)

Bit 6 ACK (Assert SCSI ACK/ signal)

Bit 5 BSY (Assert SCSI BSY/ signal)

Bit 4 SEL (Assert SCSI SEL/ signal)

Bit 3 ATN (Assert SCSI ATN/ signal)

Bit 2 MSG (Assert SCSI MSG/ signal)

Bit 1 C/D (Assert SCSI C_D/ signal)

Bit 0 I/O (Assert SCSI I_O/ signal)

This register is used primarily for diagnostic testing or programmed I/O operation. It is controlled by the SCRIPTS processor when executing SCSI SCRIPTS. SOCL should only be used when transferring data via programmed I/O. Some bits are set (1) or reset (0) when executing SCSI SCRIPTS. Do not write to the register once the NCR 53C720 starts executing SCSI SCRIPTS.

Register 0A (09)
SCSI Selector ID Register (SSID)
Read Only

VAL	Reserved			Encoded SCSI Destination ID			
7	6	5	4	3	2	1	0

Default>>>
| X | X | X | X | X | X | X | X |

Bit 7 VAL (SCSI Valid Bit)
If VAL is asserted, the two SCSI IDs were detected on the bus during a bus-initiated selection or reselection, and the encoded destination SCSI ID bits below are valid. If VAL is deasserted, only one ID was present and the contents of the encoded destination ID are meaningless.

Bits 6-4   Reserved

Bits 3-0   Encoded Destination SCSI ID
Reading the SSID register immediately after the NCR 53C720 has been selected or reselected returns the binary-encoded SCSI ID of the device which performed the operation. These bits are invalid for targets that are selected under the single initiator option of the SCSI-1 specification. This condition can be detected by examining the VAL bit, bit 1.

Register 0B (08)
SCSI Bus Control Lines (SBCL)
Read Only

REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
7	6	5	4	3	2	1	0

Default>>>

X	X	X	X	X	X	X	X

Bit 7 REQ (REQ/ status)

Bit 6 ACK (ACK/ status)

Bit 5 BSY (BSY/ status)

Bit 4 SEL (SEL/ status)

Bit 3 ATN (ATN/ status)

Bit 2 MSG (MSG/ status)

Bit 1 C/D (C_D/ status)

Bit 0 I/O   (I_O/ status)

When read, this register returns the SCSI control line status. A bit will be set when the corresponding SCSI control line is asserted. These bits are not latched; they are a true representation of what is on the SCSI bus at the time the register is read; they may change while being read. This register can be used for diagnostics testing or operation in low level mode.

Register 0C (0F)
DMA Status (DSTAT)
Read Only

DFE	HPE	BF	ABRT	SSI	SIR	WTD	IID
7	6	5	4	3	2	1	0

Default>>>

1	0	0	0	0	0	0	0

Reading this register will clear any bits that are set at the time the register is read, but will not necessarily clear the register because additional interrupts may be pending (the NCR 53C720 stacks interrupts). The ISTAT register will also be cleared. DMA interrupt conditions may be individually masked through the DIEN register.

When performing consecutive 8-bit reads of the DSTAT, SIST0 and SIST1 registers (in any order), insert a delay equivalent to 12 BCLK periods between the reads to ensure the interrupts clear properly. Also, if reading any of the registers when the ISTAT SIP and DIP bits may not be set, the SIST0 and SIST1 registers should be read before the DSTAT register to avoid missing a SCSI interrupt.

Bit 7 DFE (DMA FIFO empty)
This status bit is set when the DMA FIFO is empty. This bit may be changing at the time this register is read. It may be used to determine if any data resides in the FIFO when an error occurs and an interrupt is generated. This bit is a pure status bit and will not cause an interrupt.

Bit 6 HPE (Host Parity Error)
This bit is set when a host bus parity error is detected during a slave write or DMA read operation.

Bit 5 BF (Bus fault)
This bit is set when a host bus fault condition is detected. A host bus fault can only occur when the NCR 53C720 is bus master, and is defined as a memory cycle that is ended by the assertion of BERR/ or TEA/.

Bit 4   ABRT (Aborted)
This bit is set when an abort condition occurs. An abort condition occurs because of the following: the DP3_ABRT/ input signal is asserted by another device (parity generation mode) or a software abort command is issued by setting bit 7 of the ISTAT register.

Bit 3   SSI (SCRIPTS step interrupt)
If the Single-Step Mode bit in the DCNTL register is set, this bit will be set and an interrupt generated after successfully executing each SCRIPTS instruction.

Bit 2   SIR (SCRIPTS interrupt instruction received)
This status bit is set whenever an Interrupt instruction is evaluated as true.

Bit 1   WTD (Watchdog time-out detected)
This status bit is set when the watchdog timer decrements to zero. The watchdog timer is only used for the host memory interface. When the timer decrements to zero, it indicates that the memory system did not assert the acknowledge signal within the specified time-out period.

Bit 0   IID (Illegal instruction detected)
This status bit will be set any time an illegal instruction is detected, whether the NCR 53C720 is operating in single-step mode or automatically executing SCSI SCRIPTS.

This bit will also be set if the NCR 53C720 is executing a Wait Disconnect instruction and the SCSI REQ line is asserted without a disconnect occurring.

Register 0D (0E)
SCSI Status Zero (SSTAT0)
Read Only

ILF	ORF	OLF	AIP	LOA	WOA	RST/	SDP/
7	6	5	4	3	2	1	0

Default>>>

0	0	0	0	0	0	0	0

Bit 7   ILF (SIDL least significant byte full)
This bit is set when the least significant byte in the SCSI Input Data Latch register (SIDL) contains data. Data is transferred from the SCSI bus to the SCSI Input Data Latch register before being sent to the DMA FIFO and then to the host bus. The SIDL register contains SCSI data received asynchronously. Synchronous data received does not flow through this register.

Bit 6   ORF (SODR least significant byte full)
This bit is set when the least significant byte in the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) contains data. The SODR register is used by the SCSI logic as a second storage register when sending data synchronously. It cannot be read or written by the user. This bit can be used to determine how many bytes reside in the chip when an error occurs.

Bit 5   OLF (SODL least significant byte full)
This bit is set when the least significant byte in the SCSI Output Data Latch (SODL) contains data. The SODL register is the interface between the DMA logic and the SCSI bus. In synchronous mode, data is transferred from the host bus to the SODL register, and then to the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) before being sent to the SCSI bus. In asynchronous mode, data is transferred from the host bus to the SODL register, and then to the SCSI bus. The SODR buffer register is not used for asynchronous transfers. This bit can be used to determine how many bytes reside in the chip when an error occurs.

Bit 4   AIP (Arbitration in progress)
Arbitration in Progress (AIP = 1) indicates that the NCR 53C720 has detected a Bus Free condition, asserted BSY, and asserted its SCSI ID onto the SCSI bus.

Bit 3   LOA (Lost arbitration)
When set, LOA indicates that the NCR 53C720 has detected a bus free condition, arbitrated for the SCSI bus, and lost arbitration due to another SCSI device asserting the SEL/ signal.

Bit 2   WOA (Won arbitration)
When set, WOA indicates that the NCR 53C720 has detected a Bus Free condition, arbitrated for the SCSI bus and won arbitration. The arbitration mode selected in the SCNTL0 register must be full arbitration and selection for this bit to be set.

Bit 1   RST/ (SCSI RST/ signal)
This bit reports the current status of the SCSI RST/ signal, and the RST signal (bit 6) in the ISTAT register. This bit is not latched and may be changing when read.

Bit 0   SDP0/ (SCSI SDP0/ parity signal)
This bit represents the active high current status of the SCSI SDP0/ parity signal. This signal is not latched and may be changing as it is read.

Register 0E (0D)
SCSI Status One (SSTAT1)
Read Only

FF3	FF2	FF1	FF0	SDP	MSG	C/D	I/O
7	6	5	4	3	2	1	0

Default>>>

0	0	0	0	X	X	X	X

Bits 7-4   FF3-FF0 (FIFO flags)

FF3	FF2	FF1	FF0	Bytes or Words in the SCSI FIFO
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

These four bits define the number of bytes or words that currently reside in the NCR 53C720's SCSI synchronous data FIFO. These bits are not latched and they will change as data moves through the FIFO. Because the FIFO is only nine bytes deep, values over nine will not occur.

Bit 3   SDP0 (Latched SCSI parity)
This bit reflects the SCSI parity signal (SDP0) corresponding to the data latched in the SCSI Input Data Latch register (SIDL). It changes when a new byte is latched into the least significant byte of the SIDL register. This bit is active high, i.e., it is set when the parity signal is active.

Bit 2   MSG (SCSI MSG/ signal)

Bit 1   C/D (SCSI C_D/ signal)

Bit 0   I/O (SCSI I_O/ signal)

These SCSI phase status bits are latched on
the asserting edge of REQ/ when operating in
either initiator or target mode. These bits are
set when the corresponding signal is active.
They are useful when operating in low level
mode.

Register 0F (0C)
SCSI Status Two (SSTAT2)
Read Only

ILF1	ORF1	OLF1	RES	SPL1	RES	LDSC	SDP1
7	6	5	4	3	2	1	0

Default>>>

0	0	0	X	X	X	1	X

Bit 7   ILF1 (SIDL most significant byte full)

This bit is set when the most significant byte
in the SCSI Input Data Latch register (SIDL)
contains data. Data is transferred from the
SCSI bus to the SCSI Input Data Latch
register before being sent to the DMA FIFO
and then to the host bus. The SIDL register
contains SCSI data received asynchronously.
Synchronous data received does not flow
through this register.

**Bit 6   ORF1 (SODR most significant byte
full)**

This bit is set when the most significant byte
in the SCSI Output Data Register (SODR, a
hidden buffer register which is not accessible)
contains data. The SODR register is used by
the SCSI logic as a second storage register
when sending data synchronously. It is not
accessible to the user. This bit can be used to
determine how many bytes reside in the chip
when an error occurs.

Bit 5   OLF1 (SODL most significant byte full)

This bit is set when the most significant byte in the SCSI Output Data Latch (SODL) contains data. The SODL register is the interface between the DMA logic and the SCSI bus. In synchronous mode, data is transferred from the host bus to the SODL register, and then to the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) before being sent to the SCSI bus. In asynchronous mode, data is transferred from the host bus to the SODL register, and then to the SCSI bus. The SODR buffer register is not used for asynchronous transfers. This bit can be used to determine how m any bytes reside in the chip when an error occurs.

Bit 4   Reserved

Bit 3   Latched SCSI parity for SD15-8

This active high bit reflects the SCSI odd parity signal corresponding to the data latched into the most significant byte in the SIDL register.

Bit 2   Reserved

Bit 1   LDSC   (Last Disconnect)

Used in conjunction with the Connected (CON) bit in SCNTL1, this status bit allows the user to detect the case in which a target device disconnects, and then some SCSI device selects or reselects, the NCR 53C720. If the Connected bit is asserted and the LDSC bit is asserted, a disconnect has occurred. This bit is set when the Connected bit in SCNTL1 is off. This bit is cleared when a Block Move instruction is executed while the Connected bit in SCNTL1 is on.

Bit 0   SDP1 (SCSI SDP1 Signal)

This bit represents the active-high current state of the SCSI SDP1 parity signal. It is unlatched and may be changing as it is read.

Registers 10-13 (10-13)
Data Structure Address (DSA)
Read/Write

This 32-bit register contains the base address used for all table indirect calculations. During any Memory-to-Memory Move operation, the contents of this register are shadowed.

Register 14 (17)
Interrupt Status (ISTAT)
Read/Write

ABRT	RST	SIGP	SEM	CON	INTF	SIP	DIP
7	6	5	4	3	2	1	0

Default>>>

0	0	0	0	0	0	0	0

This is the only register that can be accessed by the host CPU while the NCR 53C720 is executing SCRIPTS (without interfering in the operation of the NCR 53C720). It may be used to poll for interrupts if interrupts are disabled. There may be stacked interrupts pending; read this register after clearing an interrupt to check for stacked interrupts.

Bit 7   ABRT (Abort operation)
Setting this bit aborts the current operation being executed by the NCR 53C720. If this bit is set and an interrupt is received, reset this bit before reading the DSTAT register to prevent further aborted interrupts from being generated. The sequence to abort any operation is:

1) Set this bit

2) Wait for an interrupt

3) Read the ISTAT register

4) If the SCSI Interrupt Pending bit is set, then read the SIST0 or SIST1 register to determine the cause of the SCSI Interrupt and go back to Step 2

5) If the SCSI Interrupt Pending bit is clear, and the DMA Interrupt Pending bit is set, then write 00h value to this register

6) Read the DSTAT register to verify the aborted interrupt and to see if any other interrupting conditions have occurred.

Note: the abort function cannot be used during a select or reselect instruction. In these cases, the time-out feature should be used.

Bit 6   RST (Software reset)
Setting this bit resets the NCR 53C720. All registers are cleared to their respective default values and all SCSI signals are deasserted. Setting this bit does not cause the SCSI RST/ signal to be asserted. This bit is not self-clearing; it must be cleared to clear the reset condition (a hardware reset will also clear this bit). This reset will not clear the Enable Acknowledge (EA) bit, Function Code 1 bit, or the ID Mode bit.

Bit 5   SIGP (Signal process)
SIGP is a R/W bit that can be written at any time, and polled and reset via CTEST2. The SIGP bit can be used in various ways to pass a flag to or from a running SCRIPT.

The only SCRIPTS instruction directly affected by the SIGP bit is Wait For Selection/ Reselection. Setting this bit causes that op code to jump to the alternate address immediately. The instructions at the alternate jump address should check the status of SIGP to determine the cause of the jump. The SIGP bit may be used at any time and is not restricted to the wait for selection/ reselection condition.

Bit 4   SEM (Semaphore)
This bit can be set by the SCRIPTS processor using a SCRIPTS register write instruction. The bit may also be set by an external processor while the NCR 53C720 is executing a SCRIPT. This bit enables the NCR 53C720 to notify an external processor of a predefined

condition while SCRIPTS are running. The external processor may also notify the NCR 53C720 of a predefined condition and the SCRIPTS processor may take action while SCRIPTS are executing.

Bit 3   CON (Connected)
This bit is automatically set any time the NCR 53C720 is connected to the SCSI bus as an initiator or as a target. It will be set after successfully completing arbitration or when the NCR 53C720 has responded to a bus-initiated selection or reselection. It will also be set after successfully completing arbitration when operating in low level mode. When this bit is clear, the NCR 53C720 is not connected to the SCSI bus. This bit is unlatched and may be changing as it is read.

Bit 2   INTF (Interrupt on the Fly)
This bit is asserted by an INTFLY instruction during SCRIPTS execution. SCRIPTS programs will not halt when the interrupt occurs. This bit can be used to notify a service routine, running on the main processor while the SCRIPTS processor is still executing a SCRIPTS program.

Note: this bit must be written to one in order to clear it after it has been set.

Note: If the INTF bit is set but SIP or DIP is not set, do not attempt to read the other chip status registers. An interrupt on the fly interrupt must be cleared before servicing any other interrupts indicated by SIP or DIP.

Bit 1   SIP (SCSI interrupt pending)
This status bit is set when an interrupt condition is detected in the SCSI portion of the NCR 53C720. The following conditions will cause a SCSI interrupt to occur:

- A phase mismatch (initiator mode) or ATN/ becomes active (target mode)

- An arbitration sequence is complete

- A selection or reselection time-out occurs

- The NCR 53C720 was selected

- The NCR 53C720 was reselected

- A SCSI gross error occurs

- An unexpected disconnect occurs

- A SCSI reset occurs

- A parity error is detected

- The handshake-to-handshake timer is expired

- The general purpose timer is expired

To determine exactly which condition(s) caused the interrupt, the SIST0 and SIST1 registers should be read. Both registers must be read to clear the interrupt.

This bit is synchronous to BCLK, but may change during read cycles.

Bit 0   DIP (DMA interrupt pending)
This status bit is set when an interrupt condition is detected in the DMA portion of the NCR 53C720. The following conditions will cause a DMA interrupt to occur:

- A host parity error is detected

- A bus fault is detected

- An abort condition is detected

- A SCRIPTS instruction is executed in single-step mode

- A SCRIPTS interrupt instruction is executed

- The Watchdog Timer decrements to zero

- An illegal instruction is detected

To determine exactly which condition(s) caused the interrupt, read the DSTAT register.

This bit is synchronous to BCLK, but may change during read cycles.

Register 18 (1B)
Chip Test Zero (CTEST0)
Read/Write

CDIS	SC1	SC0	RES	DFP	EHP	TT1	C386E
7	6	5	4	3	2	1	0

Default>>>

| 0 | 0 | 0 | X | 0 | 0 | 0 | 0 |

Bit 7   CDIS (Cache burst disable)

When this bit is set, the NCR 53C720 will not request a cache line burst. When this bit is clear, the chip will attempt cache line bursts when all necessary conditions are met.
Note: If the hardware does not support cache-line bursts, this bit should be set to maximize performance.

Bits 6-5   SC1-SC0 (Snoop control)

The values of these bits are asserted on the corresponding device pins during bus mastership if bit 0 of CTEST3 is clear. Otherwise, the SC1 pin will always be driven with the value of the SC1 bit, and the SC0 pin will reflect the state of the internal host cycle request signal.

Bit 4   GRP (Generate Receive Parity for Pass Through)

When this bit is set and the NCR 53C720 is in parity pass through mode, parity received on the SCSI bus will not pass through the DMA FIFO. Parity will be generated as data enters the DMA FIFO, eliminating the possibility of bad SCSI parity passing through to the host bus. A SCSI parity error interrupt will be generated but a system parity problem will not be created. After reset or when the bit is cleared, and when parity pass through mode is enabled, parity received on the SCSI bus will pass through the NCR 53C720 unmodified.

Bit 3   DFP (DMA FIFO parity)

This bit represents the parity bit of the DMA FIFO when reading data out of the DMA FIFO via programmed I/O. In order to transfer data to or from the DMA FIFO, perform a read or a write to the CTEST6 register. When loading data into the FIFO via programmed I/O, write this bit to the FIFO as the parity bit for each byte loaded. When writing data to the DMA FIFO, set this bit with the status of the parity bit to be written to the FIFO before writing the byte to the FIFO. For the details of performing a diagnostic test of the DMA FIFO, refer to the *NCR 53C720 Programmer's Guide.*

Bit 2   EHP (Even host parity)

Parity is generated for all slave mode register reads and master mode memory writes. This bit controls the parity sense.

Setting this bit causes the NCR 53C720 to generate even parity when driving data on the host data bus. The NCR 53C720 inverts the parity bit received from the SCSI bus to create even parity. In addition, the even parity received from the host bus is inverted to odd parity before the NCR 53C720 checks parity and sends the data to the SCSI bus. Clearing this bit causes the NCR 53C720 to maintain odd parity throughout the chip.

Bit 1   TT1 (Transfer type bit)

The inverted value of this bit is asserted on the TT1 pin during bus mastership in Bus Modes 2, 3 and 4 only. This bit is not used in Bus Mode 1. In Bus Mode 4, the TT1 pin is supported only if Cache 386 mode is not enabled. The TT0 bit is in the DMODE register.

Bit 0   C386E   (Cache 386 Enable)
Asserting this bit enables caching in the
80386DX bus mode. Caching implies that the
chip will supply an address together with an
Address Strobe (ADS/), and on the consecu-
tive clocks the NCR 53C720 will wait for four
READYI/ pulses and will either supply four
longwords of data or receive four longwords of
data. The NCR 53C720 does not support
caching in 80386SX mode or slave mode.
The chip generates the Cache Burst Request
(CBREQ) signal and samples the Transfer
Burst Inhibit (TBI) signal during the first data
transfer (first READYI/). CBREQ/ indicates
an attempt to execute a line transfer of four
longwords. TBI/ asserted indicates that the
system memory does not support the NCR
53C720 burst request. The chip powers up
with this feature disabled. The bit will be reset
during either a software or hardware reset.

Register 19 (1A)
Chip Test One (CTEST1)
Read Only

FMT3	FMT2	FMT1	FMT0	FFL3	FFL2	FFL1	FFI0
7	6	5	4	3	2	1	0

Default >>>

1	1	1	1	0	0	0	0

Bits 7-4   FMT3-0   (Byte Empty in DMA FIFO)
These bits identify the bottom bytes in the
DMA FIFO that are empty. Each bit corre-
sponds to a byte lane in the DMA FIFO. For
example, if byte lane three is empty, then
FMT3 will be set. Since the FMT flags indi-
cate the status of bytes at the bottom of the
FIFO, if all FMT bits are set, the DMA FIFO
is empty.

Bits 3-0   FFL3-0   (Byte Full in DMA FIFO)
These status bits identify the top bytes in the
DMA FIFO that are full. Each bit corresponds
to a byte lane in the DMA FIFO. For ex-
ample, if byte lane three is full then FFL3 will
be set. Since the FFL flags indicate the status
of bytes at the top of the FIFO, if all FFL bits
are set, the DMA FIFO is full.

Register 1A (19)
Chip Test Two (CTEST2)
Read Only

DDIR	SIGP	RES	RES	DFP	TEOP	DREQ	DACK
7	6	5	4	3	2	1	0

Default>>>
0	0	X	X	0	0	0	1

Bit 7   DDIR   (Data Transfer Direction)
This status bit indicates which direction data is being transferred. When this bit is set, the data will be transferred from the SCSI bus to the host bus. When this bit is clear, the data will be transferred from the host bus to the SCSI bus.

Bit 6   SIGP (Signal process)
This bit is a copy of the SIGP bit in the ISTAT register (bit 5). The SIGP bit is used to signal a running SCRIPTS operation. When this register is read, the SIGP bit in the ISTAT register is cleared.

Bit 5   Reserved

Bit 4   Reserved

Bit 3   DFP (DMA FIFO parity)
This bit represents the parity bit of the DMA FIFO when the CTEST6 register reads data out of the FIFO. Reading the CTEST6 register unloads one data byte from the bottom of the DMA FIFO. When the CTEST6 register is read the parity signal is latched into this bit location and the next byte falls down to the bottom of the FIFO.

Bit 2   TEOP (SCSI true end of process)
This bit indicates the status of the NCR 53C720's internal TEOP signal. The TEOP signal acknowledges the completion of a transfer through the SCSI portion of the NCR 53C720. When this bit is set, TEOP is active. When this bit is clear, TEOP is inactive.

Bit 1   DREQ (Data request status)
This bit indicates the status of the NCR 53C720's internal Data Request signal (DREQ). When this bit is set, DREQ is active. When this bit is clear, DREQ is inactive.

Bit 0   DACK (Data acknowledge status)
This bit indicates the status of the NCR 53C720's internal Data Acknowledge signal (DACK/). When this bit is set, DACK/ is inactive. When this bit is clear, DACK/ is active.

Register 1B (18)
Chip Test Three (CTEST3)
Read/Write

V3	V2	V1	V0	FLF	CLF	FM	SM
7	6	5	4	3	2	1	0

Default>>>

| X | X | X | X | 0 | 0 | 0 | 0 |

Bits 7-4   V3-V0 (Chip revision level)
These bits identify the chip revision level for software purposes. This data manual applies to devices with revision levels 0001 and 0010.

Bit 3   FLF (Flush DMA FIFO)
When this bit is set, data residing in the DMA FIFO is transferred to or from memory, starting at the address in the DNAD register. The internal DMAWR signal, controlled by the CTEST5 register, determines the direction of the transfer. This bit is not self clearing; once the NCR 53C720 has successfully transferred the data, this bit should be reset.

Bit 2   CLF (Clear DMA FIFO)
When this bit is set, all data pointers for the DMA FIFO are cleared. Any data in the FIFO is lost. This bit automatically resets after the NCR 53C720 has successfully cleared the appropriate FIFO pointers.

Bit 1   FM (Fetch pin mode)
When set, this bit causes the FETCH/ pin to deassert during indirect and table indirect read operations. FETCH/ will only be active during the op code portion of an instruction fetch. This allows SCRIPTS to be stored in a PROM while data tables are stored in RAM.

If this bit is not set, FETCH/ will be asserted for all bus cycles during instruction fetches.

Bit 0   SM (Snoop pins mode)
When set, the two snoop pins change functions and become pure outputs that are always driven, except when in ZMODE. The values driven are listed in the following table. When clear, the snoop pins are driven during host bus ownership with the values of the CTEST0 SC(1-0) bits.

Pin	Function
SC0	Becomes a copy of the internal bus request signal. Signal will assert prior to BR/ and will be negated during the TS/ of the last bus cycle. This signal cannot be used when the STE bit in the DCNTL register is set.
SC1	Reflects the value in the SC1 register bit.

Registers 1C-1F (1C-1F)
Temporary Stack (TEMP)
Read/Write

This 32-bit register stores the instruction address pointer for a CALL or a RETURN instruction. The address pointer stored in this register is loaded into the DSP register. This address points to the next instruction to be executed. Do not write to TEMP while the NCR 53C720 is executing SCSI SCRIPTS.

During any Memory-to-Memory Move operation, the contents of this register are shadowed.

Register 20 (23)
DMA FIFO (DFIFO)
Read/Write

RES	BO6	BO5	BO4	BO3	BO2	BO1	BO0
7	6	5	4	3	2	1	0

Default>>>

| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7   Reserved

Bits 6-0   BO6-BO0 (Byte offset counter)
These six bits indicate the amount of data transferred between the SCSI core and the DMA core. It may be used to determine the number of bytes in the DMA FIFO when a DMA error occurs. These bits are unstable while data is being transferred between the two cores; once the chip has stopped transferring data, these bits are stable.

The following steps will determine how many bytes are left in the DMA FIFO when an error occurs, regardless of the direction of the transfer:

1) Subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register.

2) AND the result with 7Fh for a byte count between zero and 64.

Register 21 (22)
Chip Test Four (CTEST4)
Read/Write

MUX	ZMOD	ZSD	SRTM	EHPC	FBL2	FBL1	FBL0
7	6	5	4	3	2	1	0

Default>>>
0   0   0   0   0   0   0

Bit 7 MUX (Host bus multiplex mode)

When set, the MUX bit puts the NCR 53C720 into host bus multiplex mode. In this mode, the chip asserts a valid address for one BCLK (during which AS/TS is valid and the data bus is tristated), and then tristates the address bus and drives the data bus (if a write). This allows the address and data buses to be tied together. It should be written before acquiring bus mastership.

Bit 6 ZMOD (High impedance mode)

Setting this bit causes the NCR 53C720 to place all output and bidirectional pins into a high-impedance state. In order to read data out of the NCR 53C720, this bit must be cleared.

This bit is intended for board-level testing only. Setting this bit during system operation will likely result in a crash.

Bit 5 ZSD (SCSI High Impedance Mode)

Setting this bit causes the NCR 53C720 to place the SCSI data bus (SD (15-0)) and the parity lines (SDP (1-0)) in a high-impedance state. In order to transfer data on the SCSI bus, this bit must be cleared.

Bit 4 SRTM (Shadow Register Test Mode)

Asserting this bit allows the user to read the shadowed temporary stack (TEMP) and Data Structure Address (DSA) registers. These registers are shadowed because both are written over during a Memory to Memory move operation. The DSA and TEMP regis-ters contain the base address used for table indirect calculations, and the instruction address pointer for a call or return instruction, respectively.

Bit 3 EHPC (Enable Host Parity Check)

Asserting this bit enables parity checking during slave write and DMA read execution if the Enable Parity Generation bit is cleared (SCNTL0 bit 2). The system powers up with this bit disabled so that the NCR 53C720 will function properly with systems that do not support parity.

Bits 2-0 FBL2-FBL0 (FIFO byte control)

FBL2	FBL1	FBL0	DMA FIFO Byte Lane	Pins
0	X	X	Disabled	n/a
1	0	0	0	D(7-0)
1	0	1	1	D(15-8)
1	1	0	2	D(23-16)
1	1	1	3	D(31-24)

These bits send the contents of the CTEST6 register to the appropriate byte lane of the 32-bit DMA FIFO. If the FBL2 bit is set, then FBL1 & FBL0 determine which of four byte lanes can be read or written. Each of the four bytes that make up the 32-bit DMA FIFO can be accessed by writing these bits to the proper value. For normal operation, FBL2 must equal zero (set it to this value before executing SCSI SCRIPTS).

▬▬▬▬
Register 22 (21)
Chip Test Five (CTEST5)
Read/Write

ADCK	BBCK	RES	MASR	DDIR	RES	RES	RES
7	6	5	4	3	2	1	0

Default>>>

0	0	X	0	0	X	X	X

Bit 7   ADCK (Clock address incrementor)
Setting this bit increments the address pointer contained in the DNAD register. The DNAD register is incremented based on the DNAD contents and the current DBC value. This bit automatically clears itself after incrementing the DNAD register.

Bit 6   BBCK (Clock byte counter)
Setting this bit decrements the byte count contained in the DBC register. The DBC register supports 24 bits. It is decremented based on the DBC contents and the current DNAD value. This bit automatically clears itself after decrementing the DBC register.

Bit 5   Reserved

Bit 4   MASR (Master control for set or reset pulses)
This bit controls the operation of bit 3. When this bit is set, bit 3 asserts the corresponding signals. When this bit is reset, bit 3 deasserts the corresponding signals. This bit and bit 3 should not be changed in the same write cycle.

Bit 3   DDIR (DMA direction)
Setting this bit either asserts or deasserts the internal DMA Write (DMAWR) direction signal depending on the current status of the MASR bit in this register. Asserting the DMAWR signal indicates that data will be transferred from the SCSI bus to the host bus. Deasserting the DMAWR signal transfers data from the host bus to the SCSI bus.

Bits 2-0   Reserved

▬▬▬▬
Register 23 (20)
Chip Test Six (CTEST6)
Read/Write

Writing to this register writes data to the appropriate byte lane of the DMA FIFO as determined by the FBL bits in the CTEST4 register. Reading this register unloads data from the appropriate byte lane of the DMA FIFO as determined by the FBL bits in the CTEST4 register. Data written to the FIFO is loaded into the top of the FIFO. Data read out of the FIFO is taken from the bottom. When data is read from the DMA FIFO, the parity bit for that byte is latched and stored in the DMA FIFO parity bit in the CTEST2 register.

To prevent DMA data from being corrupted, this register should not be accessed before starting or restarting SCRIPTS.

Registers 24-26 (25-27)
DMA Byte Counter (DBC)
Read/Write

Register 27 (24)
DMA Command (DCMD)
Read/Write

This 24-bit register determines the number of bytes to be transferred in a Block Move instruction. While sending data to the SCSI bus, the counter is decremented as data is moved into the DMA FIFO from memory. While receiving data from the SCSI bus, the counter is decremented as data is written to memory from the NCR 53C720. The DBC counter is decremented each time that the AS/ (TS/ in Bus Mode 2, ADS/ in Bus Modes 3 and 4) signal is pulsed by the NCR 53C720. It is decremented by an amount equal to the number of bytes that were transferred.

The maximum number of bytes that can be transferred in any one Block Move command is 16,777,215 bytes. The maximum value that can be loaded into the DBC register is FFFFFFh. If the instruction is Block Move and a value of 000000h is loaded into the DBC register, an illegal instruction interrupt will occur if the NCR 53C720 is not in target mode Command phase.

The DBC register is also used during table indirect I/O SCRIPTS to hold the offset value.

This 8-bit register determines the instruction for the NCR 53C720 to execute. This register has a different format for each instruction. For a complete description, refer to the NCR 53C720 instruction set in Chapter 5.

Registers 28-2B (28-2B)
DMA Next Data Address (DNAD)
Read/Write

This 32-bit register contains the general purpose address pointer. At the start of some SCRIPTS operations, its value is copied from the DSPS register. Its value may not be valid except in certain abort conditions.

Registers 2C-2F (2C-2F)
DMA SCRIPTS Pointer (DSP)
Read/Write

To execute SCSI SCRIPTS, the address of the first SCSI SCRIPT must be written to this register. In normal SCRIPTS operation, once the starting address of the SCSI SCRIPTS is written to this register, the SCRIPTS are automatically fetched and executed until an interrupt condition occurs.

In single-step mode, there is a SCRIPTS step interrupt after each instruction is executed. The DSP register does not need to be written with the next address, but the Start DMA bit (bit 2, DCNTL register) must be set each time the step interrupt occurs to fetch and execute the next SCSI SCRIPT. When writing this register eight bits at a time, writing the upper eight bits begins execution of the SCSI SCRIPTS.

Registers 30-33(30-33)
DMA SCRIPTS Pointer Save (DSPS)
Read/Write

This register contains the second longword of a SCRIPTS instruction. It is overwritten each time a SCRIPTS instruction is fetched. When a SCRIPTS Interrupt instruction is fetched, this register holds the interrupt vector.

Registers 34-37 (34-37)
Scratch Register A (SCRATCHA)
Read/Write

This is a general purpose user definable scratch pad register. Normal SCRIPTS operations will not destroy the contents of this register; only Register Read/Write and Memory Moves into the SCRATCHA register will alter its contents.

Register 38 (3B)
DMA Mode (DMODE)
Read/Write

BL1	BL0	FC2	FC1	PD	FAM	UO	MAN
7	6	5	4	3	2	1	0

Default>>>

0   0   0   0   0   0   0   0

Bit 7-6   BL1-BL0 (Burst length)

BL1	BL0	Burst Length
0	0	2 - transfer burst
0	1	4- transfer burst
1	0	8- transfer burst
1	1	16 - transfer burst

These bits control the maximum number of bus cycles performed per bus ownership. The NCR 53C720 asserts the Bus Request output when the DMA FIFO can accommodate a transfer of at least one burst size of data. Bus Request (Hold in Bus Modes 3 and 4) is also asserted during start-of-transfer and end-of-transfer cleanup and alignment, even though less than a full burst of transfers may be performed.

To perform cache line bursts, these bits must be set to 4, 8 or 16 transfers and cache bursting must be enabled (CTEST0).

The NCR 53C720 inserts a "fairness delay" of approximately 5 to 8 CLKs between bus ownerships. This gives the CPU and other bus master devices the opportunity to access memory between bursts.

Bit 5-4 FC2-FC1 (Function code) (Bus Modes 1, 3 and 4), or TM2-TM1 (Transfer Modifier) (Bus Mode 2)
These bits are user defined. Their values are asserted onto the corresponding device pins during bus mastership. If bit 6 in the DCNTL register is asserted, FC2/TM2 becomes a Preview of Address (PA/). This is an input signal only and is used to tell the NCR 53C720 that the system is ready for the next address value and the byte enable signals. This signal should not be driven during a slave access. FC1/TM1 becomes a general purpose output that is always driven when DCNTL bit 6 is asserted.

Bit 3   PD (Program/data)
This bit affects the function of the FC0 (TM0, Bus Mode 2) pin. Setting this bit causes the NCR 53C720 to drive the FC0 (TM0) signal low when fetching instructions from memory. The FC0 (TM0) signal is always driven high when moving data to or from memory and can only be driven low during instruction fetch cycles. This feature can be used to allow SCRIPTS and data to be stored in separate memory banks. When bit 6 in DCNTL register is asserted, FC0/TM0 is a data control signal that is an output signal indicating what type of bus cycle is preferred (This is the same function performed by the DC/ signal that is commonly found in Intel processors). When this bit is cleared, the NCR 53C720 drives FC0 high when the NCR 53C720 is bus master; when the NCR 53C720 is not bus master, FC0 is tristated.

FC0/TM0 = 1 Data space is being accessed

FC0/TM0 =0 Control space is present on the bus

Bit 2 FAM (Fixed address mode)
When the Fixed Address Mode bit is set, the address pointer in the DNAD register is disabled and will not increment after each data transfer. If this bit is clear, the pointer increments after each data transfer. The fixed address mode feature is used to transfer data to or from a fixed port address. This port

width must be 32 bits and longword-aligned. Setting this bit does not affect SCRIPTS fetching instructions; only data transfer instructions are affected.

In fixed address mode, if a SCSI interrupt occurs while the NCR 53C720 is receiving data, the data must be flushed manually. Once the interrupt occurs, the DMA FIFO Empty bit (bit 7 in the DSTAT register) may not have been set when reading the DMA Status register (DSTAT). At this point, the user may clear the DMA FIFO by writing to the Clear DMA FIFO bit (bit 2) in the CTEST3 register and setting the CSF (Clear SCSI FIFO) bit, bit 1 in the STEST3 register. The Block Move instruction may now be restarted. Instead of clearing the FIFO, it may be flushed. This is done as follows: 1) reset the FAM bit; 2) load the DMA Next Address register (DNAD) with a valid memory address; 3) write to the Flush DMA FIFO bit (bit 3) in the CTEST3 register; 4) set the FAM bit again. The Block Move instruction may now be restarted, assuming the byte count and address have been updated.

Bit 1   UO/TT0 (User programmable transfer type)
In all bus modes, UPSO-TT0/ is a general purpose output pin. The value in the register bit is asserted onto the UPSO-TT0/ pin while the NCR 53C720 is a bus master. The TT1 bit is in CTEST0.

Bit 0   MAN (Manual start mode)
Setting this bit disables the NCR 53C720 from automatically fetching and executing SCSI SCRIPTS after the DSP register is written. When the Start DMA bit in the DCNTL register is cleared, the chip is running in normal mode. Once the Start DMA bit in the DCNTL register is set, the NCR 53C720 automatically fetches and executes each instruction. Clearing this bit causes the NCR 53C720 to automatically fetch and execute SCSI SCRIPTS after the DSP register is written.

Register 39 (3A)
DMA Interrupt Enable (DIEN)
Read/Write

RES	HPED	BF	ABRT	SSi	SIR	WTD	IID
7	6	5	4	3	2	1	0

Default>>>

X	0	0	0	0	0	0	0

Bit 7   Reserved

Bit 6   HPED (Host parity error detected during DMA read or Slave write execution)

Bit 5   BF (Bus fault)

Bit 4   ABRT (Aborted)

Bit 3   SSI (SCRIPT step interrupt)

Bit 2   SIR (SCRIPT interrupt instruction received)

Bit 1   WTD (Watchdog time-out detected)

Bit 0   IID (Illegal instruction detected)

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the DSTAT register. An interrupt is masked by clearing the appropriate mask bit. Masking an interrupt prevents IRQ/ from being asserted for the corresponding interrupt, but the status bit will still be set in the DSTAT register. Masking an interrupt will not prevent the DIP bit (bit 0 in the ISTAT register) from being set. All DMA interrupts are considered fatal, therefore SCRIPTS will stop running when this condition occurs, whether or not the interrupt is masked. Setting a mask bit enables the assertion of IRQ/ for the corresponding interrupt.

The NCR 53C720 IRQ/ output is latched; once asserted, it will remain asserted until the interrupt is cleared by reading the appropriate status register. Masking an interrupt after the IRQ/ output is asserted will not cause IRQ/ to be deasserted.

For more information on interrupts, please refer to Chapter Two, *Functional Description*.

Register 3A (39)
DMA Watchdog Timer (DWT)
Read/Write

7	6	5	4	3	2	1	0

Default>>>

0	0	0	0	0	0	0	0

The DMA watchdog timer register provides a time-out mechanism during data transfers between the NCR 53C720 and memory. This register determines the amount of time that the NCR 53C720 will wait for the assertion of the Transfer Acknowledge signal after starting a bus cycle. Write the time-out value to this register during initialization. Every time that the NCR 53C720 transfers data to/from memory, the value stored in this register is loaded into the counter. Disable the time-out feature by writing 00h to this register.

The unit time base for this register is 32* BCLK input period. For example, at 50 MHz the time base for this register is 32 * 20 ns = 640 ns. If a time-out of 50 µs is desired, then this register should be loaded with a value of 4Eh.

The minimum time-out value that should be loaded into this register is 02h; the value 01h will not provide a reliable time-out period.

Register 3B (38)
DMA Control Register (DCNTL)
Read/Write

RES	BSM	EA	SSM	BW16	STD	FA	COM
7	6	5	4	3	2	1	0

Default>>>

0	0	0	0	0	0	0	0

Bit 7   STE (Size Throttle Enable)
Asserting this bit causes the NCR 53C720 to relinquish bus ownership every time the transfer size changes. When the size bits change from 01 (byte), 10 (word), or 00/11 (longword), the NCR 53C720 will relinquish the bus and attempt to complete the transfer in succeeding cycles. The chip powers up with this bit disabled. The bit will be reset during a software or hardware reset. When this bit is set, the SC0 signal cannot be used as an early bus request.

Note: If this bit is set, the snoop mode function of the SC0 pin, internal bus request, is not available.

Bit 6   BSM (Bus Mode)
Asserting this bit changes the meaning of the Function Code (Bus Mode 1) or Transfer Modifier (Bus Mode 2) pins. FC0 or TM0 remains unaffected. FC1 or TM1 becomes a general purpose output, and FC2 or TM2 becomes an input to allow PA/ (Preview of next address). For more information on this signal, see the DMODE register description.

Bit 5   EA (Enable ACK)
Setting this bit will cause the STERM/ (TA/ in Bus Mode 2, ReadyIn/ in Bus Modes 3 and 4) pin to become bidirectional, so the NCR 53C720 will generate STERM/ during slave accesses. When this bit is clear, the NCR 53C720 will monitor STERM/ to determine the end of a cycle. This bit takes effect during

the cycle in which it is set; setting this bit must be the first I/O performed to the NCR 53C720 if this feature is desired. This bit is not cleared with a software reset. Refer to the *Bidirectional STERM/-TA/* section in Chapter 2, for more information on how this bit operates.

Bit 4   SSM (Single–step mode)

Setting this bit causes the NCR 53C720 to stop after executing each SCRIPTS instruction, and generate a SCRIPTS step interrupt. When this bit is clear the NCR 53C720 will not stop after each instruction; instead it continues fetching and executing instructions until an interrupt condition occurs. For normal SCSI SCRIPTS operation, this bit should be clear. To restart the NCR 53C720 after it generates a SCRIPTS Step interrupt, the ISTAT and DSTAT registers should be read to clear the interrupt and then the START DMA bit in this register should be set.

Bit 3   BW16   (Host Bus Width Equal to 16)

When this bit is set, the NCR 53C720 host interface will become 16 bits wide. This bit can only be set in Little Endian mode.
Note: Data lines 31-16 must be tied to data lines 15-0.

Bit 2   STD (Start DMA operation)

The NCR 53C720 fetches a SCSI SCRIPTS instruction from the address contained in the DSP register when this bit is set. This bit is required if the NCR 53C720 is in one of the following modes:

1) *Manual start mode* – Bit 0 in the DMODE register is set

2) *Single-step mode* – Bit 4 in the DCNTL register is set

When the NCR 53C720 is executing SCRIPTS in manual start mode, the Start DMA bit needs to be set to start instruction fetches, but does not need to be set again until

an interrupt occurs. When the NCR 53C720 is in single-step mode, the Start DMA bit needs to be set to restart execution of SCRIPTS after a single-step interrupt.

Bit 1   FA (Fast arbitration)

When this bit is set, the NCR 53C720 will immediately become bus master after receiving a Bus Grant (HLDAI in Bus Modes 3 and 4), saving one clock cycle of arbitration time. When this bit is clear, the NCR 53C720 will follow the normal arbitration sequence.

Bit 0   COM (53C700 compatibility)

When this bit is clear, the NCR 53C720 will behave in a manner compatible with the 53C700; selection/reselection IDs will be stored in both the SSID and SFBR registers.

When this bit is set, the ID will be stored only in the SSID register, protecting the SFBR from being overwritten should a selection/reselection occur during a DMA register to register operation. The default condition of this bit (clear) causes the NCR 53C720 to act the same as the 53C700.

Register 3C-3F (3C-3F)
Adder Sum Output (ADDER)
Read Only

This register contains the output of the internal adder, and is used primarily for test purposes.

Register 40 (43)
SCSI Interrupt Enable Zero (SIEN0)
Read/Write

M/A	CMP	SEI	RSL	SGE	UDC	RST	PAR
7	6	5	4	3	2	1	0

Default>>>

0	0	0	0	0	0	0

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the SIST0 register. An interrupt is masked by clearing the appropriate mask bit. Masking an interrupt prevents IRQ/ from being asserted for the corresponding interrupt, but the status bit will still be set in the SIST0 register. Masking an interrupt will not prevent the ISTAT SIP bit from being set, except in the case of non-fatal interrupts (SEL, RSL, CMP, and M/A (target mode only). Setting a mask bit un-masks the corresponding interrupt, enabling the assertion of IRQ/ for that interrupt.

A masked non-fatal interrupt will not prevent un-masked or fatal interrupts from getting through; interrupt stacking does not begin until either the SIP (bit 1) or DIP (bit 0) bit in the ISTAT register is set.

The NCR 53C720 IRQ/ output is latched; once asserted, it will remain asserted until the interrupt is cleared by reading the appropriate status register. Masking an interrupt after the IRQ/ output is asserted will not cause IRQ/ to be deasserted. In the case of non-fatal interrupts, masking an interrupt after it occurs will cause the SIP bit in the ISTAT register to clear and allow pending interrupts to fall through (interrupt stacking will be disabled). The bits in this register should not be toggled on or off during normal operation. They should be set or cleared during the initialization routine.

For more information on interrupts, refer to Chapter Two, *Functional Description.*

Bit 7   M/A   (SCSI Phase Mismatch - Initiator Mode; SCSI ATN Condition - Target Mode)

In initiator mode, the SCSI phase asserted by the target and sampled during REQ does not match the expected phase in the SOCL register. This expected phase is automatically written by SCSI transfer SCRIPTS.

In target mode, the initiator has asserted ATN/. See the Disable halt on parity error or ATN condition bit in the SCNTL1 register for more information on when this status is actually raised.

Bit 6   CMP   (Function Complete)

This bit is set when full arbitration and selection sequence has completed.

Bit 5   SEL   (Selected)

The NCR 53C720 has been selected as a SCSI target device. The Enable response to selection bit in the SCID register must be set for this to occur.

Bit 4   RSL   (Reselected)

The NCR 53C720 has been reselected as a SCSI initiator device. The Enable response to reselection bit in the SCID register must be set for this to occur.

Bit 3   SGE   (SCSI Gross Error)

The following conditions are considered SCSI Gross Errors:

1) Data underflow: the SCSI FIFO was read when no data was present.

2) Data overflow: the SCSI FIFO was written to while full.

3) Offset underflow: in target mode, an ACK pulse was received before the corresponding REQ was sent.

4) Offset overflow: in initiator mode, a REQ pulse was received which caused the maximum offset (Defined by the MO3-0 bits in the SXFER register) to be exceeded.

5) In initiator mode, a phase change occurred with an outstanding REQ/ACK offset.

6) Residual data in SCSI FIFO: a transfer other than synchronous data receive was started with data left in the SCSI synchronous receive FIFO.

Bit 2   UDC   (Unexpected Disconnect)

This condition only occurs in initiator mode. It happens when the target to which the NCR 53C720 is connected disconnects from the SCSI bus unexpectedly. See the SCSI Disconnect Unexpected bit in the SCNTL2 register for more information on expected versus unexpected disconnects. Any disconnect in low level mode causes this condition.

Bit 1   RST   (SCSI Reset Condition)

The SCSI RST signal has been asserted by the NCR 53C720 or any other SCSI device. Note that this condition is edge-triggered so that multiple interrupts cannot occur because of a single RST pulse.

Bit 0   PAR   (SCSI Parity Error)

The NCR 53C720 detected a parity error while receiving or sending SCSI data. See the Disable Halt on Parity Error or ATN Condition bits in the SCNTL1 register for more information on when this condition will actually be raised.

Register 41 (42)
SCSI Interrupt Enable One (SIEN1)
Read/Write

RES	RES	RES	RES	RES	STO	GEN	HTH
7	6	5	4	3	2	1	0

Default>>>

    0   0   0   0   0   0   0

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the SIST0 register. An interrupt is masked by clearing the appropriate mask bit. Masking an interrupt prevents IRQ/ from being asserted for the corresponding interrupt, but the status bit will still be set in the SIST0 register. Masking an interrupt will not prevent the SIP bit (bit 1) in the ISTAT register from being set. Setting a mask bit un-masks the corresponding interrupt, enabling the assertion of IRQ/ for that interrupt.

A masked non-fatal interrupt will not prevent un-masked or fatal interrupts from getting through; interrupt stacking does not begin until either the DIP (bit 0) or SIP (bit 1) bit in the ISTAT register is set.

The NCR 53C720 IRQ/ output is latched; once asserted, it will remain asserted until the interrupt is cleared by reading the appropriate status register. Masking an interrupt after the IRQ/ output is asserted will not cause IRQ/ to be deasserted. In the case of non-fatal interrupts, masking an interrupt after it occurs will cause the SIP bit (bit 1) in the ISTAT register to clear and allow pending interrupts to fall through (interrupt stacking will be disabled). The bits in this register should not be toggled on or off during normal operation. They should be set or cleared during the initialization routine.

Bits 7-3　Reserved

Bit 2　STO　(Selection or Reselection Time-out)
The SCSI device which the NCR 53C720 was attempting to select or reselect did not respond within the programmed time-out period. See the description of the STIME0 register bits 3-0 for more information on the time-out timer.

Bit 1　GEN　(General Purpose Timer Expired)
The general purpose timer has expired. The time measured is the time between enabling and disabling of the timer. See the description of the STIME1 register, bits 3-0, for more information on the general purpose timer.

Bit 0　HTH　(Handshake to Handshake timer Expired)
The handshake-to-handshake timer has expired. The time measured is the SCSI Request to Request (target) or Acknowledge to Acknowledge (initiator) period. See the description of the STIME0 register, bits 7-4, for more information on the handshake-to-handshake timer.

Register 42 (41)
SCSI Interrupt Status Zero (SIST0)
Read Only

M/A	CMP	SEL	RSL	SGE	UDC	RST	PAR
7	6	5	4	3	2	1	0

Default>>>

0	0	0	0	0	0	0	0

Reading the SIST0 register returns the status of the various interrupt conditions, whether they are enabled in the SIEN0 register or not. Each bit asserted indicates that the corresponding condition has occurred. Reading the SIST0 will reset the selected conditions.

Reading this register will clear any bits that are set at the time the register is read, but will not necessarily clear the register because additional interrupts may be pending (the NCR 53C720 stacks interrupts). SCSI interrupt conditions may be individually masked through the SIEN0 register.

When performing consecutive 8-bit reads of the DSTAT, SIST0, and SIST1 registers (in any order), insert a delay equivalent to 12 BCLK periods between the reads to ensure the interrupts clear properly. Also, if reading the registers when both the ISTAT SIP (bit 1) and DIP (bit 0) bits may not be set, the SIST0 and SIST1 registers should be read before the DSTAT register to avoid missing a SCSI interrupt. For more information on interrupts, refer to Chapter Two, *Functional Description.*

Bit 7 M/A (Initiator Mode: Phase Mismatch; Target Mode: ATN/ Active)
In initiator mode, this bit is set if the SCSI phase asserted by the target does not match the instruction. The phase is sampled when REQ/ is asserted by the target. In target mode, this bit is set when the ATN/ signal is asserted by the initiator. This status bit is used in diagnostics testing or in low level mode.

Bit 6 CMP (Function Complete)
This bit is set when full arbitration and selection sequence has completed.

Bit 5 SEL (Selected)
This bit is set when the NCR 53C720 is selected by another SCSI device. The enable response to selection bit must have been set in the SCID register for the NCR 53C720 to respond to selection attempts.

Bit 4 RSL (Reselected)
This bit is set when the NCR 53C720 is reselected by another SCSI device. The Enable Response to Reselection bit must have been set in the SCID register for the NCR 53C720 to respond to reselection attempts.

Bit 3 SGE (SCSI Gross Error)
This bit is set when the NCR 53C720 encounters a SCSI Gross Error Condition. The following conditions can result in a SCSI Gross Error Condition:

1) Data Underflow - the SCSI FIFO register was read when no data was present.

2) Data Overflow - too many bytes were written to the SCSI FIFO or the synchronous offset caused the SCSI FIFO to be overwritten.

3) Offset Underflow - the NCR 53C720 is operating in target mode and an ACK/ pulse is received when the outstanding offset is zero.

4) Offset Overflow - the other SCSI device sent a REQ/ or ACK/ pulse with data which exceeded the maximum synchronous offset defined by the SXFER register.

5) Residual data in the Synchronous data FIFO - a transfer other than synchronous data receive was started with data left in the synchronous data FIFO.

6) A phase change occurred with an outstanding synchronous offset when the NCR 53C720 was operating as an initiator.

Bit 2 UDC (Unexpected Disconnect)
This bit is set when the NCR 53C720 is operating in initiator mode and the target device unexpectedly disconnects from the SCSI bus. This bit is only valid when the NCR 53C720 operates in the initiator mode. When the NCR 53C720 operates in low level mode, any disconnect will cause an interrupt, even a valid SCSI disconnect.

This bit will also be set if a selection time-out occurs (it may occur before, at the same time, or stacked after the STO interrupt, since this is not considered an expected interrupt).

Bit 1 RST (SCSI RST/ Received)
This bit is set when the NCR 53C720 detects an active RST/ signal, whether the reset was generated external to the chip or caused by the Assert RST/ bit in the SCNTL1 register. This NCR 53C720 SCSI reset detection logic is edge-sensitive so that multiple interrupts will not be generated for a single assertion of the SCSI RST/ signal.

Bit 0 PAR (Parity Error)
This bit is set when the NCR 53C720 detects a parity error when receiving or sending SCSI data. The Enable Parity Checking bit (bit 3 in the SCNTL0 register) must be set for this bit to become active. A parity error can occur when receiving data from the SCSI bus or when receiving data from the host bus. From the host bus, parity is checked as it is transferred from the DMA FIFO to the SODL register. A parity error can occur from the host bus only if Pass Through parity is enabled (bit 3 in the SCNTL0 register = 1, bit 2 in the SCNTL0 register = 0).

Register 43 (40)
SCSI Interrupt Status One (SIST1)
Read Only

RES	RES	RES	RES	RES	STO	GEN	HTH
7	6	5	4	3	2	1	0

Default>>>

0	0	0	0	0	0	0	0

Reading the SIST1 register returns the status of the various interrupt conditions, whether they are enabled in the SIEN1 register or not. Each bit that is set indicates that the corresponding condition has occurred.

Reading SIST1 will reset the selected conditions.

Bits 7-3 Reserved

Bit 2 STO (Selection or Reselection Time-out)
The SCSI device which the NCR 53C720 was attempting to select or reselect did not respond within the programmed time-out period. See the description of the STIME0 register, bits 3-0, for more information on the time-out timer.

Bit 1 GEN (General Purpose Timer Expired)
The general purpose timer has expired. The time measured is the time between enabling and disabling of the timer. See the description of the STIME1 register, bits 3-0, for more information on the general purpose timer.

Bit 0 HTH (Handshake to Handshake timer Expired)
The handshake-to-handshake timer has expired. The time measured is the SCSI Request to Request (target) or Acknowledge to Acknowledge (initiator) period. See the description of the STIME0 register, bits 7-4, for more information on the handshake-to-handshake timer.

████████
Register 44 (47)
SCSI Longitudinal Parity (SLPAR)
Read/Write

This register performs a bytewise longitudinal parity check on all SCSI data received or sent through the SCSI core. If one of the bytes received or sent (usually the last) is the set of correct even parity bits, SLPAR should go to zero (assuming it started at zero). As an example, suppose that the following three data bytes and one check byte are received from the SCSI bus (all signals are shown active high):

Data Bytes	Running SLPAR
—	00000000
1. 11001100	11001100 (XOR of word 1)
2. 01010101	10011001 (XOR of word 1 and 2)
3. 00001111	10010110 (XOR of word 1, 2 and 3) Even Parity >>>10010110
4. 10010110	00000000

A one in any bit position of the final SLPAR value would indicate a transmission error.

The SLPAR register can also be used to generate the check bytes for SCSI send operations. If the SLPAR register contains all zeros prior to sending a block move, it will contain the appropriate check byte at the end of the block move. This byte must then be sent across the SCSI bus.

Writing any value to this register resets it to zero.

The longitudinal parity checks are meant to provide an added measure of SCSI data integrity and are entirely optional. This register does not latch SCSI selection/reselection IDs under any circumstances.

████████
Register 45 (46)
SCSI Wide Residue Data (SWIDE)
Read Only

After a wide SCSI data receive operation, this register will contain a residual data byte if the last byte received was never sent across the DMA bus. It represents either the first data byte of a subsequent data transfer, or it is a residue byte which should be cleared when an Ignore Wide Residue message is received. It may also be an overrun data byte.

Register 46 (45)
Memory Access Control (MACNTL)
Read/Write

RES	RES	RES	RES	DataWR	DataRD	PSCRIPT	SCRIPT
7	6	5	4	3	2	1	0

Default>>>

X	X	X	X	0	0	0	0

MACNTL is used to determine if an external access is to local or far memory.

Bits 7-4 Reserved

Bits 3-0

These bits are used to define if a data write, data read, pointer to a SCRIPTS fetch and a SCRIPTS fetch, respectively, are considered local memory accesses. If any of the bits are set, the access will be considered local. The bits power up cleared, indicating far memory. Internal logic will determine if the specific transfer is considered local or far. The MAC/ signal, pin 26 (also referred to as the near/far pin), will be asserted high when the transfer is to local memory. Assuming the SCRIPTS fetch bit is set, the near/far pin will not be affected until completion of the next Transfer Control instruction. Changes to the MAC/ signal will be available at the pin at the same time the Bus Request pin is asserted.

Register 47 (44)
General Purpose Control (GPCNTL)
Read/Write

RES	RES	RES	GPI/O_en4	GPI/O_en3	GPI/O_en2	GPI/O_en1	GPI/O_en0
7	6	5	4	3	2	1	0

Default>>>

X	X	X	0	1	1	1	1

GPCNTL is used to determine if the pins controlled by the General Purpose register (GPREG, address 07 (04)h) are inputs or outputs.

Bits 7-5 Reserved

Bit 4 GPI/O_en4 (General Purpose Output Enable 4)

GPCNTL, corresponding to bit 4 in the GPREG register and pin 43, powers up as a general purpose output.

Bits 3-0 GPI/O_en3-0 (General Purpose Output Enable 3-0)

Bits 3-0 in GPCNTL, corresponding to bits 3-0 in the GPREG register and pins 39-42, power up as general purpose inputs. If any of the bits are cleared, this indicates an output and if any of the bits are set this indicates an input. When the bits are enabled as inputs, an internal pullup is also enabled.

Register 48 (4B)
SCSI Timer Register 0 (STIME0)
Read /Write

HTH3	HTH2	HTH1	HTH0	SEL3	SEL2	SEL1	SEL0
7	6	5	4	3	2	1	0

Default>>>

0	0	0	0	0	0	0	0

Bits 7-4 HTH (Handshake-to-Handshake Timer Period)

These bits select Handshake-to-Handshake Time-out Period, the maximum time between SCSI handshakes (REQ to REQ in target mode, or ACK to ACK in initiator mode). When this timing is exceeded, the HTH bit in the SIST1 register is set, and an interrupt is optionally generated, if bit 0 in the SIEN1 register is set. The following table applies to the Handshake-to-Handshake Timer, the Selection/Reselection Timer (bits 3-0), and the General Purpose Timer (STIME1 bits 3-0).

HTH 7-4, SEL 3-0, GEN 3-0	Minimum Time-out
0000	Disabled
0001	100 μs
0010	200 μs
0011	400 μs
0100	800 μs
0101	1.6 ms
0110	3.2 ms
0111	6.4 ms
1000	12.8 ms
1001	25.6 ms
1010	51.2 ms
1011	102.4 ms
1100	204.8 ms
1101	409.6 ms
1110	819.2 ms
1111	1.6+ sec

Bits 3-0 SEL (Selection Time-out Period)

These bits select the SCSI selection/reselection time-out period. When this timing (plus the 200 μs selection abort time) is exceeded, the STO bit in the SIST1 register is set. An interrupt is optionally generated, if bit 2 in the SIEN1 register is set.

Register 49 (4A)
SCSI Timer Register One   (STIME1)
Read/Write

RES	RES	RES	RES	GEN3	GEN2	GEN1	GEN0
7	6	5	4	3	2	1	0

Default>>>

  X   X   X   X   0   0   0   0

Bits 7-4   Reserved

Bits 3-0   GEN3-0   (General Purpose Timer Period)

These bits select the period of the general purpose timer. The time measured is the time between enabling and disabling of the timer. When this timing is exceeded, the GEN bit in the SIST1 register is set and an interrupt is optionally generated, if bit 1 in the SIEN1 register is set. Refer to the table under STIME0, bits 3-0, for the available time-out periods.

Register 4A (49)
Response ID Zero (RESPID0)
Read/Write

Register 4B (48)
Response ID One (RESPID1)
Read/Write

RESPID0 and RESPID1 contain the selection or reselection IDs. In other words, these two 8-bit registers contain the ID that the chip responds to on the SCSI bus. Each bit represents one possible ID with the most significant bit of RESPID1 representing ID 15 and the least significant bit of RESPID0 representing ID 0. The SCID register still contains the chip ID used during arbitration. The chip can respond to more than one ID because more than one bit can be set in the RESPID1 and RESPID0 registers. However, the chip can arbitrate with only one ID value in the SCID register.

Register 4C (4F)
SCSI Test Register Zero (STEST0)
Read Only

RES	RES	RES	RES	SLT	ART	SOZ	SOM
7	6	5	4	3	2	1	0

Default>>>

X	X	X	X	0	X	1	1

Bits 7-4   Reserved

Bit 3   SLT   (Selection Response Logic Test)
This bit is asserted when the NCR 53C720 is
ready to be selected or reselected. This does
not take into account the bus settle delay of
400 ns. This bit is used for functional test and
fault purposes.

**Bit 2   ART   (Arbitration Priority Encoder
Test)**
This bit will always be asserted when the NCR
53C720 exhibits the highest priority ID as-
serted on the SCSI bus during arbitration. It is
primarily used for chip level testing, but it may
be used during low level mode operation to
determine if the NCR 53C720 has won arbi-
tration.

**Bit 1   SOZ   (SCSI Synchronous Offset
Zero)**
This bit indicates that the current synchronous
SCSI REQ/ACK offset is zero. This bit is not
latched and may change at any time. It is used
in low level synchronous SCSI operations.
When this bit is set, the NCR 53C720, as an
initiator, is waiting for the target to request
data transfers. If the NCR 53C720 is a target
then the initiator has sent the offset number of
acknowledges.

**Bit 0   SOM   (SCSI Synchronous Offset
Maximum)**
This bit indicates that the current synchronous
SCSI REQ/ACK offset is the maximum
specified by bits 3-0 in the SCSI Transfer
register. This bit is not latched and may
change at any time. It is used in low level
synchronous SCSI operations. When this bit is
set the NCR 53C720, as a target, is waiting for
the initiator to acknowledge the data transfers.
If the NCR 53C720 is an initiator then the
target has sent the offset number of requests.

Register 4D (4E)
SCSI Test Register One   (STEST1)
Read Only

RES	RES	RES	RES	RES	RES	SFP1	SFP0
7	6	5	4	3	2	1	0

Default >>

X	X	X	X	X	X	X	X

Bits 7-2   Reserved

Bits 1-0   SFP1-0   (SCSI FIFO Parity)
These bits represent the parity that is read
from the SCSI FIFO byte lanes during test
access through the SODL register. For reading
the SCSI FIFO in test mode, these bits may
be read after reading the SODL registers.
SFP1 represents parity for the most significant
byte and SFP0 represents parity for the least
significant byte. See the description of the
SCSI FIFO Test Mode bit in the STEST3
register for more information on testing the
SCSI FIFO.

Register 4E (4D)
SCSI Test Register Two   (STEST2)
Read/Write

SCE	ROF	DIF	SLB	SZM	AWS	EXT	LOW
7	6	5	4	3	2	1	0

Default >>

0	0	0	0	0	0	0	0

Bit 7   SCE   (SCSI Control Enable)
This bit, when set, allows all SCSI control and
data lines to be asserted through the SOCL
and SODL registers regardless of whether the
NCR 53C720 is configured as a target or
initiator.

Note: This bit should not be set during
normal operation, since it could cause conten-
tion on the SCSI bus. It is included for diag-
nostic purposes only.

Bit 6   ROF   (Reset SCSI Offset)
Setting this bit clears any outstanding synchro-
nous SCSI REQ/ACK offset. This bit should
be set if a SCSI gross error condition occurs,
to clear the offset when a synchronous transfer
does not complete successfully. The bit auto-
matically clears itself after resetting the syn-
chronous offset.

Bit 5   DIF   (SCSI Differential Mode)
Setting this bit allows the NCR 53C720 to
interface properly to external differential
transceivers. Its only real effect is to tristate the
BSY/, SEL/, and RST/ pads so that they can
be used as pure inputs. Resetting this bit
enables single ended mode operation. This bit
should be set in the initialization routine if the
differential pair interface is to be used.

Bit 4   SLB   (SCSI Loopback Mode)
Setting this bit allows the NCR 53C720 to
perform SCSI loopback diagnostics. That is, it
enables the SCSI core to simultaneously
perform as both initiator and target.

Bit 3   SZM   (SCSI High-Impedance Mode)
Setting this bit places all the open-drain 48 mA SCSI drivers into a high-impedance state. This is to allow internal loopback mode operation without affecting the SCSI bus.

Bit 2   AWS   (Always Wide SCSI)
When this bit is set, all SCSI information transfers will be done in 16-bit wide mode. This includes data, message, command, status and reserved phases. This bit should normally be deasserted since 16-bit wide message, instruction, and status phases are not supported by the SCSI specifications. This bit is not guaranteed to function properly with future SCSI specifications.

Bit 1   EXT   (Extend REQ/ACK Filtering)
The SCSI core contains a special digital filter on the REQ/ and ACK/ pins which will cause glitches on deasserting edges to be disregarded. Asserting this bit will increase the filtering period from 30ns to 60ns on the deasserting edge of the REQ/ and ACK/ signals.

Note: This bit must never be set during fast SCSI (> 5M transfers per second) operations, because a valid assertion could be treated as a glitch.

Bit 0   LOW   (SCSI Low level Mode)
Setting this bit places the NCR 53C720 in low level mode. In this mode, no DMA operations can occur, and no SCRIPTS instructions can be executed. Arbitration and selection may be performed by setting the start sequence bit as described in the SCNTL0 register. SCSI bus transfers are performed by manually asserting and polling SCSI signals. Clearing this bit allows instructions to be executed in SCSI SCRIPTS mode.

Note: It is not necessary to set this bit for access to the SCSI bit-level registers (SODL, SBCL, and input registers). This bit must be clear for the chip to properly respond to selection or reselection.

Register 4F (4C)
SCSI Test Register Three   (STEST3)
Read/Write

TE	STR	HSC	DSI	S16	TTM	CSF	FTM
7	6	5	4	3	2	1	0

Default>>>

X	X	0	0	0	0	0	0

Bit 7   TE (TolerANT Enable)
Asserting this bit enables NCR TolerNAT Active Negation. TolerANT causes the SCSI Request, Acknowledge, Data, and parity signals to be actively deasserted, in addition to relying on external pullups when the NCR 53C720 is driving these signals. Active deassertion of these signals will occur only when the NCR 53C720 is in an information transfer phase. When operating in a differential environment or at fast SCSI timings, Active Negation should be enabled to improve setup and deassertion times. Active Negation is disabled after reset or when this bit is cleared.

Bit 6   STR (SCSI FIFO Test Read)
Setting this bit places the SCSI core into a test mode in which the SCSI FIFO can be easily read. Reading the least significant byte of the SODL register will cause the FIFO to unload. The functions are summarized in the table below.

Register Name	Register Operation	FIFO Bits	FIFO Function
SODL	Read	15-0	Unload
SODL0	Read	7-0	Unload
SODL1	Read	15-8	None

Bit 5   HSC   (Halt SCSI Clock)

Asserting this bit causes the internal divided SCSI clock to come to a stop in a glitchless manner. This bit may be used for test purposes or to lower I_{DD} during a power down mode.

Bit 4   DSI   (Disable Single Initiator Response)

If this bit is set, the NCR 53C720 will ignore all bus-initiated selection attempts which employ the single-initiator option from SCSI-1. In order to select the NCR 53C720 while this bit is set, the NCR 53C720's SCSI ID and the initiator's SCSI ID must both be asserted. This bit should be asserted in SCSI-2 systems so that a single bit error on the SCSI bus will not be interpreted as a single initiator response.

Bit 3   S16   (16-bit System)

If this bit is set, all devices in the SCSI system implementation are assumed to be 16 bits. This causes the NCR 53C720 to always check the parity bit for SCSI IDs 15-8 during bus-initiated selection or reselection, assuming parity checking has been enabled. If an 8-bit SCSI device attempts to select the NCR 53C720 while this bit is set, the NCR 53C720 will ignore the selection attempt, because the parity bit for IDs 15-8 will be undriven. See the description of the Enable Parity Checking bit in the SCNTL0 register for more information.

Bit 2   TTM   (Timer Test Mode)

Asserting this bit facilitates testing of the selection time-out, general purpose, and handshake-to-handshake timers by greatly reducing all three time-out periods. Setting this bit starts all three timers and if the respective bits in the SIEN1 register are asserted, the NCR 53C720 will generate interrupts at time-out.

Bit 1   CSF   (Clear SCSI FIFO)

Setting this bit will cause the "full flags" for the SCSI FIFO to be cleared. This empties the FIFO. This bit is self-resetting. The SIDL, SODL, and SODR Least and Most Significant Byte Full bits in the SSTAT0 and SSTAT2 registers are also cleared.

Bit 0   STW   (SCSI FIFO Test Write)

Setting this bit places the SCSI core into a test mode in which the FIFO can be easily read and written. While this bit is set, writes to the least significant byte of the SODL register will cause the entire word contained in this register to be loaded into the FIFO. Writing the least significant byte of the SODL register will cause the FIFO to load. These functions are summarized in the table below:

Register Name	Register Operation	FIFO Bits	FIFO Function
SODL	Write	15-0	Load
SODL0	Write	7-0	Load
SODL1	Write	15-8	None

Registers 50-51 (52-53)
SCSI Input Data Latch (SIDL)
Read Only

This register is used primarily for diagnostic testing, programmed I/O operation or error recovery. Data received from the SCSI bus can be read from this register. Data can be written to the SODL register and then read back into the NCR 53C720 by reading this register to allow loopback testing. When receiving SCSI data, the data will flow into this register and out to the host FIFO. This register differs from the SBDL register; SIDL contains latched data and the SBDL always contains exactly what is currently on the SCSI data bus. Reading this register causes the SCSI parity bit to be checked, and will cause a parity error interrupt if the data is not valid.

Registers 54-55 (56-57)
SCSI Output Data Latch (SODL)
Read/Write

This register is used primarily for diagnostic testing or programmed I/O operation. Data written to this register is asserted onto the SCSI data bus by setting the Assert Data Bus bit in the SCNTL1 register. This register is used to send data via programmed I/O. Data flows through this register when sending data in any mode. It is also used to write to the synchronous data FIFO when testing the chip.

Registers 58-59 (5A-5B)
SCSI Bus Data Lines (SBDL)
Read Only

This register contains the SCSI data bus status. Even though the SCSI data bus is active low, these bits are active high. The signal status is not latched and is a true representation of exactly what is on the data bus at the time the register is read. This register is used when receiving data via programmed I/O. This register can also be used for diagnostic testing or in low level mode.

Registers 5C-5F
Scratch Register B (SCRATCHB)
Read/Write

This is a general purpose, user definable scratch pad register. Apart from CPU access, only Register Read/Write and Memory Moves directed at the SCRATCHB register will alter its contents.

Chapter Five
Instruction Set of the I/O Processor

SCSI SCRIPTS

After power up and initialization of the NCR 53C720, the chip may operate in low level register interface or SCSI SCRIPTS mode. In the low level register interface, the user has access to the DMA control logic and the SCSI bus control logic. The chip operates much like an NCR 53C80 when in low level mode. An external processor has access to the SCSI bus signals and the low level DMA signals, which allows creation of complicated board level test algorithms. The low level interface provides backward compatibility with SCSI devices that require certain unique timings or bus sequences to operate properly. Another feature allowed at the low level is loopback testing. In loopback mode, the SCSI core can be directed to talk to the DMA core to test internal data paths all the way out to the chip's pins.

To operate in the SCSI SCRIPTS mode, the NCR 53C720 requires only a SCRIPTS start address. All commands are fetched from local or external memory. The NCR 53C720 fetches and executes its own instructions by becoming a bus master on the host bus and fetching two or three 32-bit words into its registers. Commands are fetched until an interrupt command is encountered, or until an unexpected event (such as a hardware error) causes an interrupt to the external processor.

Once an interrupt is generated, the NCR 53C720 halts all operations until the interrupt is serviced. Then, the start address of the next SCRIPTS instruction may be written to the DMA SCRIPTS Pointer register to restart the automatic fetch and execution of instructions.

The SCSI SCRIPTS mode of execution allows the NCR 53C720 to make decisions based on the status of the SCSI bus, which off-loads the microprocessor from servicing the numerous interrupts inherent in I/O operations.

Given the rich set of SCSI-oriented features included in the command set, and the ability to re-enter the SCSI algorithm at any point, this high level interface is all that is required for both normal and exception conditions. Therefore, switching to low level mode for error recovery should never be required.

Four types of SCSI SCRIPTS instructions are implemented in the NCR 53C720:

- Block Move
- I/O or Read/Write
- Transfer Control
- Memory Move

Each instruction consists of two or three 32-bit words. The first 32-bit word is always loaded into the DCMD and DBC registers, the second into the DSPS register. The third word, used only by Memory Move instructions, is loaded into the TEMP register.

Block Move Instructions

Figure 5-1. Block Move Instruction Register
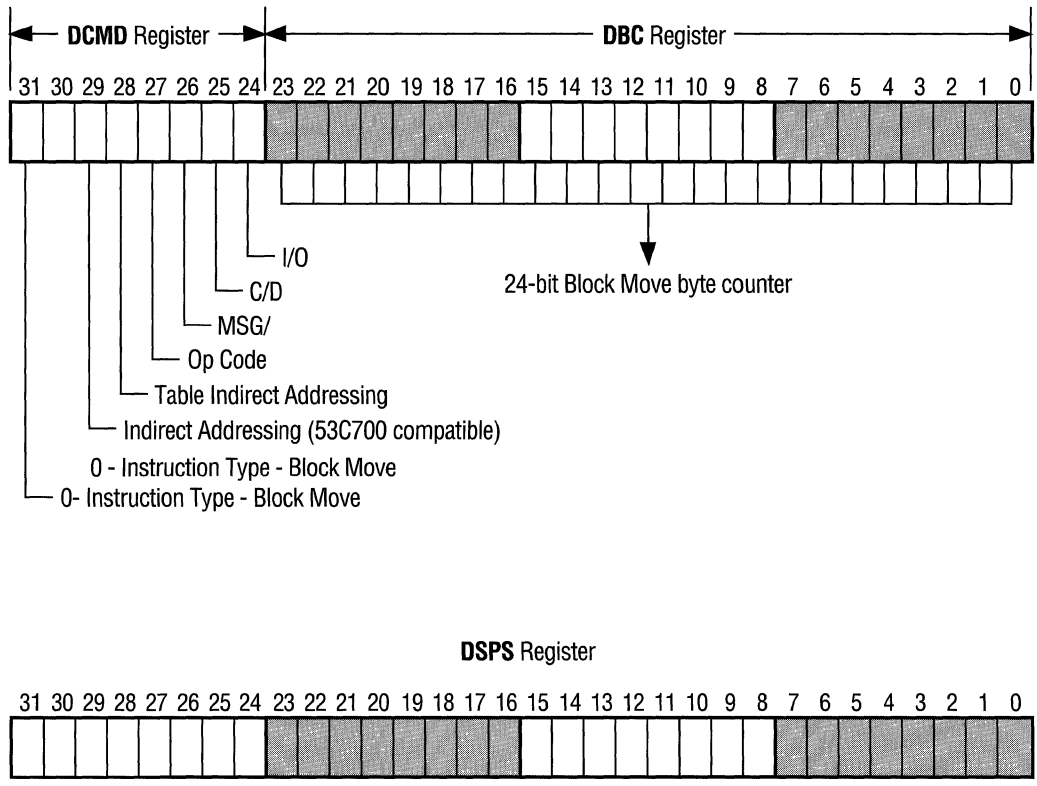
Bits 31-30   Instruction Type Block Move

Bit 29   Indirect Addressing

When this bit is cleared, user data is moved to or from the 32-bit data start address for the Block Move instruction. The value is loaded into the chip's address register and incremented as data is transferred.

When set, the 32-bit user data start address for the Block Move is the address of a pointer to the actual data buffer address. The value at the 32-bit start address is loaded into the chip's DNAD register via a third long word fetch (4-byte transfer across the host computer bus).

Direct

The byte count and absolute address are as follows:

Command	Byte Count
Address of Data	

Indirect

Use the byte count and fetch the data address from the address in the command. The byte count is contained in the DBC register and the data address is fetched from the DSPS register.

Command	Byte Count
Address of Pointer to Data	

Once the data buffer address is loaded, it is executed as if the chip operates in the direct mode. This indirect feature allows a table of data buffer addresses to be specified. Using the NCR SCSI SCRIPTS compiler, the table offset is placed in the script at compile time. Then at the actual data transfer time, the offsets are added to the base address of the data address table by the external

processor. The logical I/O driver builds a structure of addresses for an I/O rather than treating each address individually. This feature makes it possible to locate SCSI SCRIPTS in a PROM.

Bit 28   Table Indirect Addressing

When this bit is set, the 24-bit signed value in the start address of the move is treated as a relative displacement from the value in the DSA register. Both the transfer count and the source/destination address are fetched from this address.

Table Indirect

Use the signed integer offset in bits 23-0 of the second four bytes of the instruction to fetch first the byte count and then the data address. The signed value is combined with the data structure base address to generate the physical address used to fetch values from the data structure. Sign-extended values of all ones for negative values are allowed, but ignored.

Command	Not Used
	Table Offset

Prior to the start of an I/O the Data Structure Base Address register (DSA) must be loaded with the base address of the I/O data structure. The address may be any longword on a longword boundary.

At the start of an I/O, the DSA is added to the 24-bit signed offset value from the op code to generate the address of the required data; both positive and negative offsets are allowed. A subsequent fetch from the address brings the data values into the chip.

For a MOVE command, the 24-bit byte count is fetched from system memory. Then the 32-bit physical address is brought into the NCR 53C720. Execution begins at this point.

SCRIPTS can directly execute operating system I/O data structures, saving time at the beginning of an I/O operation. The I/O data structure can begin on any longword boundary and can cross system segment boundaries.

There are two restrictions on the placement of data in system memory: the eight bytes of data in the MOVE command must be contiguous, as shown below; and indirect data fetches are not available during execution of a Memory-to-Memory DMA operation.

(00)	Byte Count
Physical Data Address	

Bit 27   Op Code

This one-bit field defines the instruction to be executed, either a block move (MOVE) or a chained block move (CHMOV). The Op Code Field bit has different meaning depending on whether the NCR 53C720 is operating in Initiator or Target mode. If the Op Code bit is asserted (target mode) or deasserted (initiator mode) during a chained block move instruction, the corresponding bit in the SCNTL2 register (SCNTL bit 6) is asserted. The Op Code bit and the SCNTL2 bit are cleared once a block move instruction is executed.

Target Mode

OPC	Instruction Defined
0	MOVE
1	CHMOV

1) The NCR 53C720 verifies that it is connected to the SCSI bus as a target before executing this instruction.

2) The NCR 53C720 asserts the SCSI phase signals (MSG/, C_D/, and I_O/) as defined by the Phase Field bits in the instruction.

3) If the instruction is for the Command phase, the NCR 53C720 receives the first command byte and decodes its SCSI Group Code.

   a) If the SCSI Group Code is either Group 0, Group 1, Group 2, or Group 5, then the NCR 53C720 overwrites the DBC register with the length of the Command Descriptor Block: 6, 10, or 12 bytes.

   b) If any other Group Code is received, the DBC register is not modified and the NCR 53C720 will request the number of bytes specified in the DBC register. If the DBC register contains 000000h an illegal instruction interrupt is generated.

4) The NCR 53C720 transfers the number of bytes specified in the DBC register starting at the address specified in the DNAD register. If the Op Code bit is set and a data transfer ends on an odd byte boundary, the NCR 53C720 will store the last byte in the SCSI Wide Residue Data Register during a receive operation or in the SCSI Output Data Latch register during a send operation. This byte will be combined with the first byte from the subsequent transfer so that a wide transfer can be completed. See Figure 5-2.

5) If the SCSI ATN/ signal is asserted by the initiator or a parity error occurred during the transfer, the transfer can optionally be halted and an interrupt generated. The Disable Halt on Parity Error or ATN bit in the SCNTL1 register controls whether an interrupt will be generated.

Initiator Mode

OPC	Instruction Defined
0	CHMOV
1	MOVE

1) The NCR 53C720 verifies that it is connected to the SCSI bus as an initiator before executing this instruction.

2) The NCR 53C720 waits for an unserviced phase to occur. An unserviced phase is defined as any phase (with REQ/ asserted) for which the NCR 53C720 has not yet transferred data by responding with an ACK/.

3) The NCR 53C720 compares the SCSI phase bits in the DCMD register with the latched SCSI phase lines stored in the SSTAT1 register. These phase lines are latched when REQ/ is asserted.

4) If the SCSI phase bits match the value stored in the SSTAT1 register, the NCR 53C720 will transfer the number of bytes specified in the DBC register starting at the address pointed to by the DNAD register. If the op code bit is cleared and a data transfer ends on an odd byte boundary, the NCR 53C720 will be store the last byte in the SCSI Wide Residue Data Register during a receive operation, or in the SCSI Output Data Latch Register during a send operation. This byte will be combined with the first byte from the subsequent transfer so that a wide transfer can be completed. See Figure 5-2.

5) If the SCSI phase bits do not match the value stored in the SSTAT1 register, the NCR 53C720 generates a phase mismatch interrupt and the command is not executed.

6) During a Message Out phase, after the NCR 53C720 has performed a select with Attention, the NCR 53C720 will deassert ATN/ during the final REQ/ACK handshake.

7) When the NCR 53C720 is performing a block move for Message In phase, it will not deassert the ACK/ signal for the last REQ/ACK handshake. The ACK signal must be cleared using the Clear ACK I/O instruction.

Figure 5-2. Block Move and Chained Block Move Instructions

Host Memory   SCSI Bus

32 Bits   16 Bits
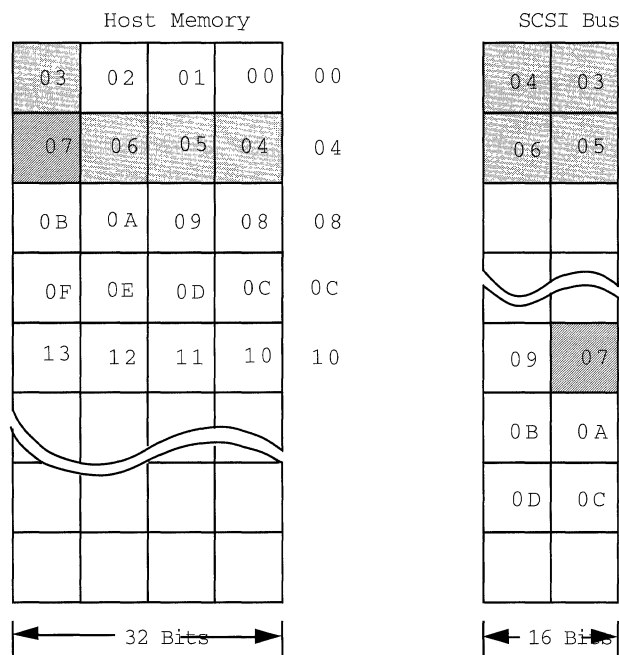
Notes: CHMOV 5, 3, when DATA_OUT: Move 5 bytes from address 03 in the host memory to the SCSI bus (bytes 03, 04, 05 and 06 are moved and byte 07 remains in the low order byte of the SCSI Output Data Latch register and is married with the first byte of the following MOVE instruction.

MOVE 5, 9, when DATA_OUT: Moves 5 bytes from address 09 in the host memory to the SCSI bus.

Bits 26-24 SCSI Phase

This 3-bit field defines the desired SCSI information transfer phase. When the NCR 53C720 operates in Initiator mode, these bits are compared with the latched SCSI phase bits in the SSTAT1 register. When the NCR 53C720 operates in target mode, the NCR 53C720 asserts the phase defined in this field. The following table describes the possible combinations and the corresponding SCSI phase.

MSG	C/D	I/O	SCSI Phase
0	0	0	Data out
0	0	1	Data in
0	1	0	Command
0	1	1	Status
1	0	0	Reserved out
1	0	1	Reserved in
1	1	0	Message out
1	1	1	Message in

Bits 23-0 Transfer Counter

A 24-bit field specifying the number of data bytes to be moved between the NCR 53C720 and system memory. The field is stored in the DBC register. When the NCR 53C720 transfers data to/from memory, the DBC register is decremented by the number of bytes transferred. In addition, the DNAD register is incremented by the number of bytes transferred. This process is repeated until the DBC register has been decremented to zero. At that time, the NCR 53C720 fetches the next instruction.

Bits 31-0 Start Address

This 32-bit field specifies the starting address of the data to be moved to/from memory. This field is copied to the DNAD register. When the NCR 53C720 transfers data to or from memory, the DNAD register is incremented by the number of bytes transferred.

I/O Instructions

Figure 5-3. I/O Instruction Register

DSPS Register
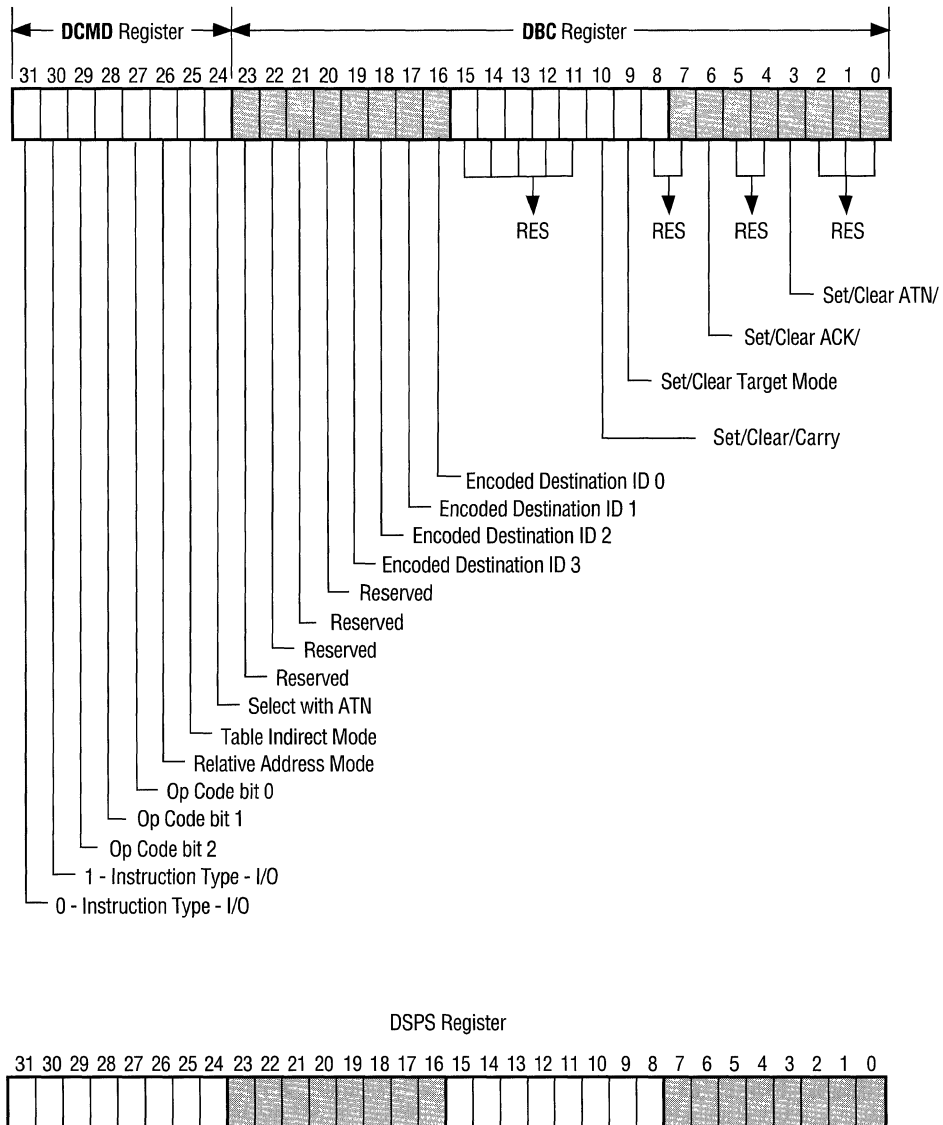
Bits 31-30 Instruction Type
I/O Instruction

Bits 29-27 Op Code

The following Op Code Field bits have different meanings, depending on whether the NCR 53C720 is operating in initiator or target mode.

Note: The following op codes determine if the instruction is a Read/Write or an I/O instruction. op code selections 101-111 are considered Read/Write instructions, and are described in that section.

Target Mode

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Reselect
0	0	1	Disconnect
0	1	0	Wait Select
0	1	1	Set
1	0	0	Clear

Reselect Instruction

1) The NCR 53C720 arbitrates for the SCSI bus by asserting the SCSI ID stored in the SCID register. If the NCR 53C720 loses arbitration, then it tries again during the next available arbitration cycle without reporting any lost arbitration status.

2) If the NCR 53C720 wins arbitration, it attempts to reselect the SCSI device whose ID is defined in the destination ID field of the instruction. Once the NCR 53C720 has won arbitration, it fetches the next instruction from the address pointed to by the DSP register.

3) If the NCR 53C720 is selected or reselected before winning arbitration, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The NCR 53C720 should manually be set to initiator mode if it is reselected, or to target mode if it is selected.

Disconnect Instruction

The NCR 53C720 disconnects from the SCSI bus by deasserting all SCSI signal outputs. The SCSI direction control signals are deasserted, which disables the differential pair output drivers.

Wait Select Instruction

1) If the NCR 53C720 is selected, it fetches the next instruction from the address pointed to by the DSP register.

2) If reselected, the NCR 53C720 fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The NCR 53C720 should manually be set to initiator mode when reselected.

3) If the CPU sets the SIGP bit in the ISTAT register, the NCR 53C720 will abort the WAIT SELECT instruction and fetch the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register.

Set Instruction

When the ACK/ or ATN/ bits are set, the corresponding bits in the SOCL register are set. ACK/ or ATN/ should not be set except for testing purposes. When the target bit is set, the corresponding bit in the SCNTL0 register is also set. When the carry bit is set the corresponding bit in the ALU is set.

Note: None of the signals are set on the SCSI bus in target mode.

Clear Instruction

When the ACK/ or ATN/ bits are set, the corresponding bits are cleared in the SOCL register. When the target bit is cleared, the corresponding bit in the SCNTL0 register is cleared. When the carry bit is cleared, the corresponding bit in the ALU is cleared.

Note: None of the signals are reset on the SCSI bus in target mode.

Initiator Mode

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Select
0	0	1	Wait Disconnect
0	1	0	Wait Reselect
0	1	1	Set
1	0	0	Clear

Select Instruction

1) The NCR 53C720 arbitrates for the SCSI bus by asserting the SCSI ID stored in the SCID register. If the NCR 53C720 loses arbitration, it tries again during the next available arbitration cycle without reporting any lost arbitration status.

2) If the NCR 53C720 wins arbitration, it attempts to select the SCSI device whose ID is defined in the destination ID field of the instruction. It then fetches the next instruction from the address pointed to by the DSP register.

3) If the NCR 53C720 is selected or reselected before winning arbitration, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The NCR 53C720 should manually be set to initiator mode if it is reselected, or to target mode if it is selected.

4) If the Select with ATN/ field is set, the ATN/ signal is asserted during the selection phase.

Wait Disconnect Instruction

1) The NCR 53C720 waits for the target to perform a disconnect from the SCSI bus. A disconnect occurs when BSY/ and SEL/ are inactive for a minimum of one Bus Free Delay (400 ns).

Wait Reselect Instruction

1) If the NCR 53C720 is selected before being reselected, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The NCR 53C720 should be manually set to target mode when selected.

2) If the NCR 53C720 is reselected, it fetches the next instruction from the address pointed to by the DSP register.

3) If the CPU sets the SIGP bit in the ISTAT register, the NCR 53C720 will abort the Wait Reselect instruction and fetch the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register.

Set Instruction

When the ACK/ or ATN/ bits are set, the corresponding bits in the SOCL register are set. When the target bit is set, the corresponding bit in the SCNTL0 register is also set. When the carry bit is set the corresponding bit in the Arithmetic Logic Unit (ALU) is set.

Clear Instruction

When the ACK/or ATN/ bits are set, the corresponding bits are cleared in the SOCL register. ACK/ or ATN/ should not be set except for testing purposes. When the target bit is cleared, the corresponding bit in the SCNTL0 register is cleared. When the carry bit is cleared, the corresponding bit in the ALU is cleared.

Bit 26   Relative Addressing Mode

When this bit is set, the 24-bit signed value in the DNAD register is used as a relative displacement from the current DSP address.

This bit should only be used in conjunction with the Select, Reselect, Wait Select, and Wait Reselect instructions. The Select and Reselect instructions can contain an absolute alternate jump address or a relative transfer address.

Bit 25   Table Indirect Mode

When this bit is set, the 24-bit signed value in the DBC register is used as an offset relative to the value in the Data Structure Base Address (DSA) register. The SCSI ID, synchronous offset and synchronous period are loaded from this address.

Prior to the start of an I/O, the DSA must be loaded with the base address of the I/O data structure. The address may be any longword on a longword boundary.

At the start of an I/O, the DSA is added to the 24-bit signed offset value from the op code to generate the address of the required data; both positive and negative offsets are allowed. A subsequent fetch from the address brings the data values into the chip.

SCRIPTS can directly execute operating system I/O data structures, saving time at the beginning of an I/O operation. The I/O data structure can begin on any longword boundary and can cross system segment boundaries.

There are two restrictions on the placement of data in system memory.

1) The I/O data structure must lie within the 8 MB above or below the base address.

2) An I/O command structure must have all four bytes contiguous in system memory, as shown below. The offset/period bits are ordered as in the SXFER register. The configuration bits are ordered as in the SCNTL3 register.

config	ID	offset/period	(00)

This bit should only be used in conjunction with the Select, Reselect, Wait Select, and Wait Reselect instructions. Bits 25 and 26 may be set individually or in combination:

	Bit 25	Bit 26
Direct	0	0
Table Indirect	0	1
Relative	1	0
Table Relative	1	1

Direct

Uses the device ID and physical address in the command.

Command	ID	Not Used	Not Used
Absolute Alternate Address			

Table Indirect

Uses the physical jump address, but fetches data using the table indirect method.

Command	Table Offset
Absolute Alternate Address	

Relative

Uses the device ID in the command, but treats the alternate address as a relative jump

Command	ID	Not Used	Not Used
	Alternate Jump Offset		

Table Relative

Treats the alternate jump address as a relative jump and fetches the device ID, synchronous offset, and synchronous period indirectly. Adds the value in bits 23-0 of the first four bytes of the SCRIPT to the data structure base address to form the fetch address.

Command	Table Offset
	Alternate Jump Offset

Bit 24   Select with ATN/

This bit specifies whether ATN/ will be asserted during the selection phase when the NCR 53C720 is executing a Select instruction. When operating in initiator mode, set this bit for the Select instruction. If this bit is set on any other I/O instruction, an illegal instruction interrupt is generated.

Bit 23-20   Reserved

Bits 19-16   Encoded SCSI Destination ID

This four-bit field specifies the encoded destination ID for an I/O instruction.

Bit 10   Set/Clear Carry

This bit is used in conjunction with a Set or Clear command to set or clear the Carry bit. Setting this bit with a Set command asserts the Carry bit in the ALU. Clearing this bit with a Set command deasserts the Carry bit in the ALU.

Bit 9   Set/Clear Target Mode

This bit is used in conjunction with a Set or Clear command to set or clear target mode. Setting this bit with a Set command configures the NCR 53C720 as a target device (this sets bit 0 of the SCNTL0 register). Setting this bit with a Clear command configures the NCR 53C720 as an initiator device (this clears bit 0 of the SCNTL0 register).

Bit 6   Set/Clear ACK/

Bit 3   Set/Clear ATN/

These two bits are used in conjunction with a Set or Clear command to assert or deassert the corresponding SCSI control signal. Bit 6 controls the SCSI ACK/ signal; bit 3 controls the SCSI ATN/ signal.

Setting either of these bits will set or reset the corresponding bit in the SOCL register, depending on the command used. The Set command is used to assert ACK/ and/or ATN/ on the SCSI bus. The Clear command is used to deassert ACK/ and/or ATN/ on the SCSI bus.

Since ACK/ and ATN/ are initiator signals, they will not be asserted on the SCSI bus unless the NCR 53C720 is operating as an initiator or the SCSI Loopback Enable bit is set in the STEST2 register.

The Set/Clear SCSI ACK/ATN instruction would be used after message phase Block Move operations to give the initiator the opportunity to assert attention before acknowledging the last message byte. For example, if the initiator wishes to reject a message, an Assert SCSI ATN instruction would be issued before a Clear SCSI ACK instruction. After the target has serviced the request for a message-out phase, ATN is deasserted with a Clear SCSI ATN instruction.

Bits 31-0   Jump Address

This 32-bit field specifies the address of the
instruction to fetch when the NCR 53C720
encounters a jump condition. The NCR 53C720
fetches instructions from the address pointed to by
this field whenever the NCR 53C720 encounters a
SCSI condition that is different from the condi-
tion specified in the instruction.

For example, during the execution of a Select
instruction in initiator mode, if the NCR 53C720
is reselected, then the next instruction is fetched
from the address pointed to by the jump address
field. For a complete description of the different
jump conditions, refer to the description of each
instruction.

Read/Write Instructions

Figure 5-4. Read/Write Instruction Register
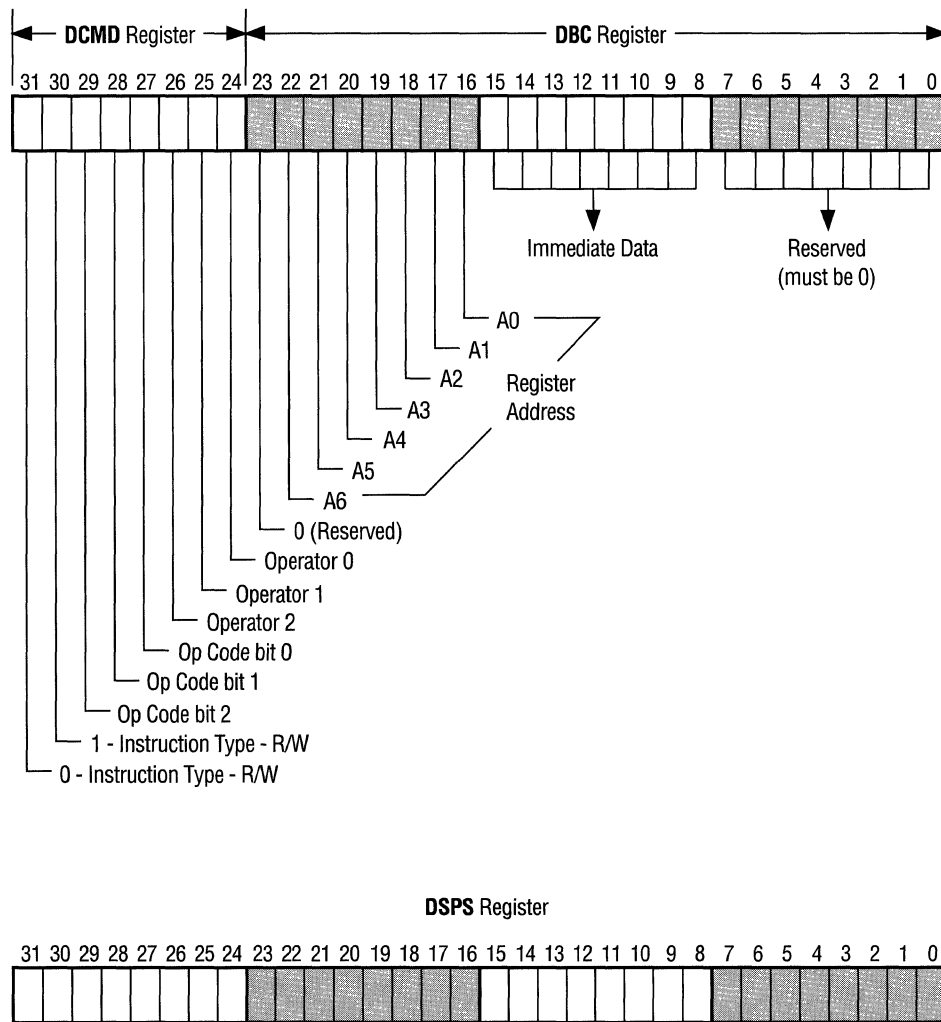
Table 5-1. Read/Write Instructions

Operator	Opcode 111 Read Modify Write	Opcode 110 Move to SFBR	Opcode 101 Move From SFBR
000	Move data into register. Syntax: "Move data8 to RegA"	Move data into SFBR register. Syntax: "Move data8 to SFBR"	Move data into register. Syntax: "Move data8 to RegA"
001*	Shift register one bit to the left and place the result in the same register. Syntax: "Move RegA SHL RegA"	Shift register one bit to the left and place the result in the SFBR register. Syntax: "Move RegA SHL SFBR"	Shift the SFBR register one bit to the left and place the result in the register. Syntax: "Move SFBR SHL RegA"
010	OR data with register and place the result in the same register. Syntax: "Move RegA | data8 to RegA"	OR data with register and place the result in the SFBR register. Syntax: "Move RegA | data8 to SFBR"	OR data with SFBR and place the result in the register. Syntax: "Move SFBR | data8 to RegA"
011	XOR data with register and place the result in the same register. Syntax: "Move RegA XOR data8 to RegA"	XOR data with register and place the result in the SFBR register. Syntax: "Move RegA XOR data8 to SFBR"	XOR data with SFBR and place the result in the register. Syntax: "Move SFBR XOR data8 to RegA"
100	AND data with register and place the result in the same register. Syntax: "Move RegA & data8 to RegA"	AND data with register and place the result in the SFBR register. Syntax: "Move RegA & data8 to SFBR"	AND data with SFBR and place the result in the register. Syntax: "Move SFBR & data8 to RegA"
101*	Shift register one bit to the right and place the result in the same register. Syntax: "Move RegA SHR RegA"	Shift register one bit to the right and place the result in the SFBR register. Syntax: "Move RegA SHR SFBR"	Shift the SFBR register one bit to the right and place the result in the register. Syntax: "Move SFBR SHR RegA"
110	Add data to register without carry and place the result in the same register. Syntax: "Move RegA + data8 to RegA"	Add data to register without carry and place the result in the SFBR register. Syntax: "Move RegA + data8 to SFBR"	Add data to SFBR without carry and place the result in the register. Syntax: "Move SFBR + data8 to RegA "
111	Add data to register with carry and place the result in the same register. Syntax: "Move RegA + data8 to RegA with carry"	Add data to register with carry and place the result in the SFBR register. Syntax: "Move RegA + data8 to SFBR with carry"	Add data to SFBR with carry and place the result in the register. Syntax: "Move SFBR + data8 to RegA with carry"

Notes: 1) Substitute the desired register name or address for "RegA" in the syntax examples.
          2) data8 indicates eight bits of data

* Data is shifted through the Carry bit and the Carry bit is shifted into the data byte

Bits 31-30   Instruction Type
Read/Write Instruction

Bits 29-27   Op code

The combinations of these bits determine if the instruction is a Read/Write or an I/O instruction. Op codes 000 through 100 are considered I/O instructions.

Bits 26-24   Operator

These bits are used in conjunction with the op code bits to determine which instruction is currently selected.

Bit 24, which in earlier versions of the NCR 53C720 was Carry Enable, is now included with the Operator bits.

Bit 23   Reserved

Bits 22-16   Register Address A(6-0)

Register values may be changed from SCRIPTS in read-modify-write cycles or move to/from SFBR cycles. A(6-0) select an 8-bit source/destination register within the NCR 53C720. Register addresses are always Little Endian addresses.

Bits 15-8   Immediate Data

Bits 7-0   Reserved

Read-Modify-Write Cycles

The register is read, the selected operation is performed, and the result is written back to the source register.

The Add operation can be used to increment or decrement register values (or memory values if used in conjunction with a Memory-to-Register Move operation) for use as loop counters.

Move to/from SFBR Cycles

All operations are read-modify-writes. However, two registers are involved, one of which is always the SFBR. The possible functions of this command are:

- Write one byte (value contained within the SCRIPTS instruction) into any chip register.

- Move to/from the SFBR from/to any other register.

- Alter the value of a register with AND/OR/ ADD operators.

- After moving values to the SFBR, the compare and jump, call, or similar commands may be used to check the value.

- A Move-to-SFBR followed by a Move-from-SFBR can be used to perform a register to register move.

Transfer Control
Instructions

Figure 5-5. Transfer Control Instruction Register

DSPS Register
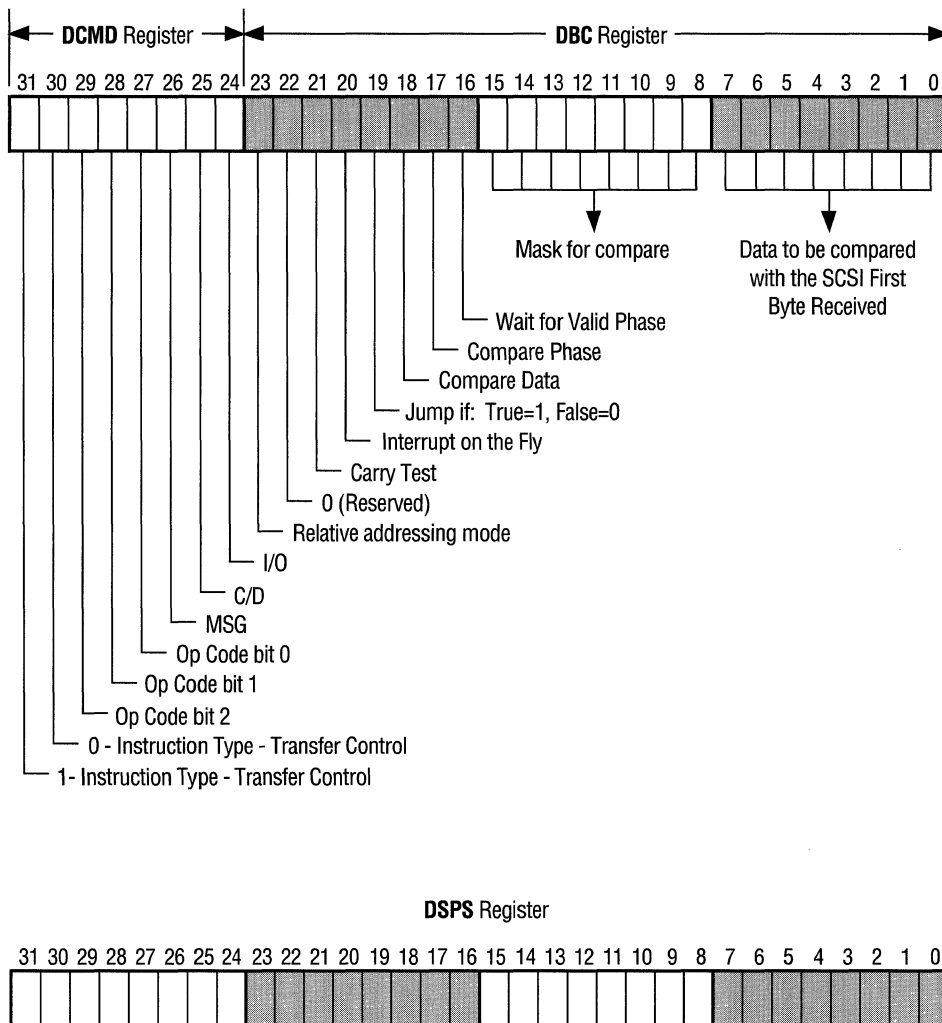
Bits 31-30   Instruction Type - Transfer Control Instruction

Bits 29-27   Op Code

This 3-bit field specifies the type of transfer control instruction to be executed. All transfer control instructions can be conditional. They can be dependent on a true/false comparison of the ALU Carry bit or a comparison of the SCSI information transfer phase with the Phase field, and/or a comparison of the First Byte Received with the Data Compare field. Each instruction can operate in initiator or target mode.

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Jump
0	0	1	Call
0	1	0	Return
0	1	1	Interrupt
1	X	X	Reserved

Jump Instruction

1) The NCR 53C720 can do a true/false comparison of the ALU carry bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare and True/False bit fields. If the comparisons are true, the NCR 53C720 loads the DSP register with the contents of the DSPS register. The DSP register now contains the address of the next instruction.

2) If the comparisons are false the NCR 53C720 fetches the next instruction from the address pointed to by the DSP register, leaving the instruction pointer unchanged.

Call Instruction

1) The NCR 53C720 can do a true/false comparison of the ALU carry bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, the NCR 53C720 loads the DSP register with the contents of the DSPS register and that address value becomes the address of the next instruction.

   When the NCR 53C720 executes a Call instruction, the instruction pointer contained in the DSP register is stored in the TEMP register.

   When a Return instruction is executed, the value stored in the TEMP register is returned to the DSP register.

2) If the comparisons are false, the NCR 53C720 fetches the next instruction from the address pointed to by the DSP register and the instruction pointer is not modified.

Return Instruction

1) The NCR 53C720 can do a true/false comparison of the ALU bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, then the NCR 53C720 loads the DSP register with the contents of the DSPS register. That address value becomes the address of the next instruction.

   When the NCR 53C720 executes a Call instruction, the current instruction pointer contained in the DSP register is stored in the TEMP register.

   When a Return instruction is executed, the value stored in the TEMP register is returned to the DSP register.

The NCR 53C720 does not check to see whether the Call instruction has already been executed. It will not generate an interrupt if a Return instruction is executed without previously executing a Call instruction.

2) If the comparisons are false, then the NCR 53C720 fetches the next instruction from the address pointed to by the DSP register and the instruction pointer will not be modified.

Interrupt Instructions

Interrupt

a) The NCR 53C720 can do a true/false comparison of the ALU bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, then the NCR 53C720 generates an interrupt by asserting the IRQ/ signal.

b) The 32-bit address field stored in the DSPS register (not DNAD as in 53C700) can contain a unique interrupt service vector. When servicing the interrupt, this unique status code allows the ISR to quickly identify the point at which the interrupt occurred.

c) The NCR 53C720 halts and the DSP register must be written to start any further operation.

Interrupt on-the-Fly

a) The NCR 53C720 can do a true/false comparison of the ALU carry bit or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, the NCR 53C720 will assert the Interrupt on the fly bit (ISTAT bit 2).

Bits 26-24   SCSI Phase

This 3-bit field corresponds to the three SCSI bus phase signals which are compared with the phase lines latched when REQ/ is asserted. Comparisons can be performed to determine the SCSI phase actually being driven on the SCSI bus. The following table describes the possible combinations and their corresponding SCSI phase. These bits are only valid when the NCR 53C720 is operating in initiator mode; when the NCR 53C720 is operating in the target mode, these bits should be cleared.

MSG	C/D	I/O	SCSI Phase
0	0	0	Data out
0	0	1	Data in
0	1	0	Command
0	1	1	Status
1	0	0	Reserved out
1	0	1	Reserved in
1	1	0	Message out
1	1	1	Message in

Bit 23   Relative Addressing Mode

When this bit is set, the 24-bit signed value in the DSPS register is used as a relative offset from the current DSP address (which is pointing to the next instruction, not the one currently executing). Relative mode does not apply to Return and Interrupt SCRIPTS.

Jump/Call an Absolute Address – Start execution at the new absolute address.

Command	Condition Codes
Absolute Alternate Address	

Jump/Call a Relative Address – Start execution at the current address plus (or minus) the relative offset.

Command	Condition Codes
	Alternate Jump Offset

The SCRIPTS program counter is a 32-bit value pointing to the SCRIPT currently being executed by the NCR 53C720. The next address is formed by adding the 32-bit program counter to the 24-bit signed value of the last 24 bits of the Jump or Call instruction. Because it is signed (twos compliment), the jump can be forward or backward.

A relative transfer can be to any address within a 16-MB segment. The program counter is combined with the 24-bit signed offset (using addition or subtraction) to form the new execution address.

SCRIPTS programs may contain a mixture of direct jumps and relative jumps to provide maximum versatility when writing SCRIPTS. For example, major sections of code can be accessed with far calls using the 32-bit physical address, then local labels can be called using relative transfers. If a SCRIPT is written using only relative transfers it would not require any run time alteration of physical addresses, and could be stored in and executed from a PROM.

Bit 22   Reserved

Bit 21   Carry Test

When this bit is set, decisions based on the ALU carry bit can be made. True/False comparisons are legal, but Data Compare and Phase Compare are illegal.

Bit 20   Interrupt on the Fly

When this bit is asserted, the interrupt instruction will not halt the SCRIPTS processor. Once the interrupt occurs, the Interrupt on the Fly bit (ISTAT bit 2) will be asserted.

Bit 19   Jump If True/False

This bit determines whether the NCR 53C720 should branch when a comparison is true or when a comparison is false. This bit applies to both Phase Compares and Data Compares. If both the Phase Compare and Data Compare bits are set, then both compares must be true to branch on a true condition. Both compares must be false to branch on a false condition.

Bit 19	Compare	Action
0	False	Jump Taken
0	True	No Jump
1	False	No Jump
1	True	Jump Taken

Bit 18   Compare Data

When this bit is set, then the first byte received from the SCSI data bus (contained in SFBR register) is compared with the Data to be Compared Field in the Transfer Control instruction. The Wait for Valid Phase bit controls when this compare will occur. The Jump if True/False bit determines the condition (true or false) to branch on.

Bit 17   Compare Phase

When the NCR 53C720 is in initiator mode, this bit controls phase compare operations. When this bit is set, the SCSI phase signals (latched by REQ/) are compared to the Phase Field in the Transfer Control instruction; if they match, then the comparison is true. The Wait for Valid Phase bit controls when the compare will occur.

When the NCR 53C720 is operating in target mode this bit, when set, tests for an active SCSI ATN/ signal.

Bit 16   Wait For Valid Phase

If the Wait for Valid Phase bit is set, then the NCR 53C720 waits for a previously unserviced phase before comparing the SCSI phase & data.

If the Wait for Valid Phase bit is clear, then the NCR 53C720 compares the SCSI phase & data immediately.

Bits 15-8   Data Compare Mask

The Data Compare Mask allows a SCRIPT to test certain bits within a data byte. During the data compare, any mask bits that are set cause the corresponding bit in the SFBR data byte to be ignored.

For instance, a mask of 01111111b and data compare value of 1XXXXXXXb allows the SCRIPTS processor to determine whether or not the high order bit is on while ignoring the remaining bits.

Bits 7-0   Data Compare Value

This 8-bit field is the data to be compared against the SCSI First Byte Received (SFBR) register. These bits are used in conjunction with the Data Compare Mask Field to test for a particular data value.

Bits 31-0   Jump Address

This 32-bit field contains the address of the next instruction to fetch when a jump is taken. Once the NCR 53C720 has fetched the instruction from the address pointed to by these 32 bits, this address is incremented by four, loaded into the DSP register and becomes the current instruction pointer.

Memory Move Instructions

Figure 5-6. Memory Move Instruction Register

DSPS Register

TEMP Register
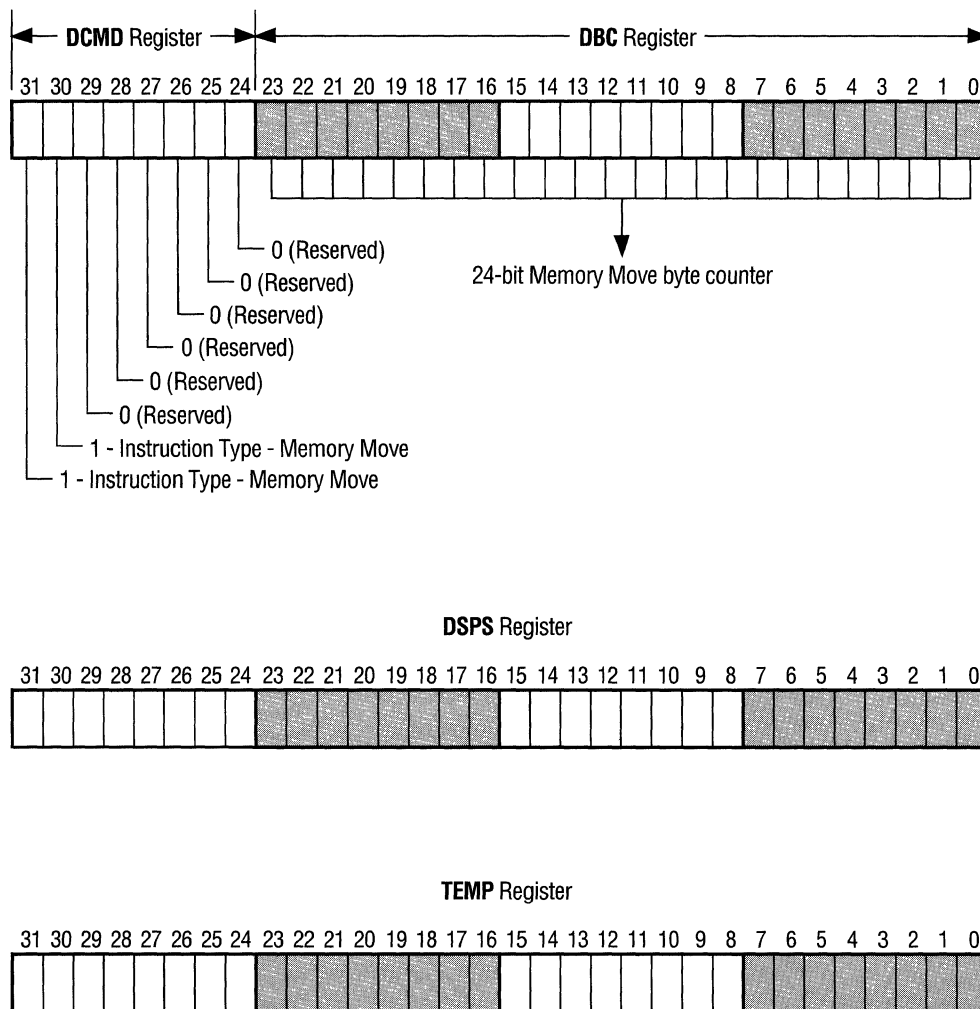
The Memory Move instruction is used to copy the specified number of bytes from the source address to the destination address.

Allowing the NCR 53C720 to perform memory moves frees the system processor for other tasks and moves data at higher speeds than available from current DMA controllers. Up to 16 MB may be transferred with one instruction. There are two restrictions:

1) Both the source and destination addresses must start with the same address alignment (A(1-0) must be the same). If source and destination are not aligned, then an illegal instruction interrupt will occur. If cache line burst is enabled, address lines A(3-0) must be the same.

2) Indirect addresses are not allowed.

A special block move instruction passes the source and destination addresses and the byte count to the NCR 53C720. A burst of data is fetched from the source address, put into the DMA FIFO and then written out to the destination address. The move continues until the byte count decrements to zero, then another SCRIPT is fetched from system memory.

Upon completion of the move, an interrupt instruction or jump to a SCSI function should be executed.

The DSPS and DSA registers are additional holding registers used during the Memory Move.

Bits 31-30   Instruction Type Memory Move

Bits 29-24   Reserved

These bits are reserved and must be zero. If any of these bits is set, an illegal instruction interrupt will occur.

Bits 23-0   Transfer Count

The number of bytes to be transferred is stored in the lower 24 bits of the first instruction word.

Read/Write System Memory from a Script

By using the Memory Move instruction, single or multiple register values may be transferred to/from system memory.

Because the Chip Select (CS/) input is derived from an address decode, it could activate during a Memory Move operation if the source/destination address decodes to within the chip's register space. If this occurs, the register indicated by the lower six bits of the memory address is taken to be the data source or destination. In this way, register values can be saved to system memory and later restored, and SCRIPTS can make decisions based on data values in system memory.

The SFBR is not writable via the CPU, and therefore not by a Memory Move. However, it can be loaded via SCRIPTS Read/Write operations. To load the SFBR with a byte stored in system memory, the byte must first be moved to an intermediate NCR 53C720 register (for example, from a SCRATCH register), and then to the SFBR.

The same address alignment restrictions apply to register access operations as to normal memory-to-memory transfers.

Chapter 6
NCR 53C720 Electrical Characteristics

Absolute Maximum Stress Ratings*

Parameter	Symbol	Min	Max	Unit
Storage temperature	T_{STG}	– 55	150	°C
Supply voltage	V_{DD}	– 0.5	7.0	V
Input voltage	V_{IN}	V_{SS}– 0.5	V_{DD} + 0.5	V
Latch-up Current	I_{LP}	± 200	-	mA**
Electrostatic discharge	ESD***	-	2K	V

*   *Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or at any other conditions beyond those indicated in the Operating Conditions section of this specification is not implied.*

** *-2V = V_{pin} > +8V*

*** *SCSI pins only. Measured according to MIL-STD-883C, Method 3015.7*

Operating Conditions

Parameter	Symbol	Min	Max	Units
Supply voltage	V_{DD}	4.75	5.25	V
Supply current (Static)	I_{DD}	-	1	mA
Supply current (Dynamic)	I_{DD}	-	75	mA
Operating temperature (free-air)	T_A	0	70	°C
Thermal resistance (Junction-ambient)	U_{JA}	50	65	°C/W
Power Dissipation	P_{DD}	0	0.40	W

DC Characteristics

$V_{DD} = 5V \pm 5\%$, $T_A = 0$ to $70°$ C, unless otherwise noted.

SCSI Signals – SD(15-0)/*, SDP0/*, REQ/*, MSG/, I/O, C/D, ATN/, ACK/*, BSY/, SEL/, RST/, SDP1/*

Parameter	Symbol	Min	Max	Unit	Conditions
Input high voltage	V_{IH}	2.0	$V_{DD} + 0.5$	V	-
Input low voltage	V_{IL}	$V_{SS} - 0.5$	0.8	V	-
Output low voltage	V_{OL}	V_{SS}	0.5	V	$I_{OL} = 48$ mA
Hysteresis	V_{HYS}	300	-	mV	-
Input leakage current	I_{IN}	– 10	10	μA	-
Input leakage – SCSI RST		– 400	10	μA	-
Tristate leakage current	I_{OZ}	– 10	10	μA	-

* *TolerANT not enabled.*

Input Signals – BG-HLDAI/, BOFF/, RESET/, CS/, BS(2-0), BCLK-, SCLK, AUTO/, DIFFSENS

Parameter	Symbol	Min	Max	Units	Conditions
Input high voltage	V_{IH}	2.0	$V_{DD} + 0.5$	V	-
Input low voltage	V_{IL}	$V_{SS} - 0.5$	0.8	V	-
Input leakage current	I_{IN}	– 1.0	1.0	μA	-

Input Signal – TSTIN/

Parameter	Symbol	Min	Max	Units	Conditions
Input high voltage	V_{IH}	2.0	$V_{DD} + 0.5$	V	-
Input low voltage	V_{IL}	$V_{SS} - 0.5$	0.8	V	-
Input leakage current	I_{IN}	– 10	10	μA	$V_{IL} = V_{DD}$
Input high leakage current	I_{IL}	– 200	– 50	μA	$V_{IL} = 0$ V

Output Signals – SDIR(15-0), SDIRP0, BSYDIR, SELDIR, RSTDIR, TGS, IGS, SDIRP1

Parameter	Symbol	Min	Max	Units	Conditions
Output high voltage	V_{OH}	2.4	V_{DD}	V	$I_{OH} = -4$ mA
Output low voltage	V_{OL}	V_{SS}	0.4	V	$I_{OL} = 4$ mA
Output high current	I_{OH}	– 2.0	-	mA	$V_{OH} = V_{DD} - 0.5$ V
Output low current	I_{OL}	4.0	-	mA	$V_{OL} = 0.4$ V

Output Signals – FETCH/, IRQ/, TST_OUT

Parameter	Symbol	Min	Max	Units	Conditions
Output high voltage	V_{OH}	2.4	V_{DD}	V	$I_{OH} = -8$ mA
Output low voltage	V_{OL}	V_{SS}	0.4	V	$I_{OL} = 8$ mA
Output high current	I_{OH}	– 4.0	-	mA	$V_{OH} = V_{DD} - 0.5$ V
Output low current	I_{OL}	8.0	-	mA	$V_{OL} = 0.4$ V

Output Signals –SLACK/- READYO/, MASTER/, MAC/

Parameter	Symbol	Min	Max	Units	Conditions
Output high voltage	V_{OH}	2.4	V_{DD}	V	$I_{OH} = -16$ mA
Output low voltage	V_{OL}	V_{SS}	0.4	V	$I_{OL} = 16$ mA
Output high current	I_{OH}	– 8.0	-	mA	$V_{OH} = V_{DD} - 0.5$ V
Output low current	I_{OL}	16.0	-	mA	$V_{OL} = 0.4$ V

Tristate Output Signals – A(31-7), FC(2-0)-TM(2-0), SC(1-0), UPSO-TT0/, CBREQ/-TT1/, BR/-HOLD/

Parameter	Symbol	Min	Max	Units	Conditions
Output high voltage	V_{OH}	2.4	V_{DD}	V	$I_{OH} = -16\,mA$
Output low voltage	V_{OL}	V_{SS}	0.4	V	$I_{OL} = 16\,mA$
Output high current	I_{OH}	-8.0	-	mA	$V_{OH} = V_{DD} - 0.5\,V$
Output low current	I_{OL}	16.0	-	mA	$V_{OL} = 0.4\,V$
Tristate leakage current	I_{OZ}	-10	10	μA	-

Bidirectional Signals – A(6-0), D(31-0), DP(3-0), DS/-DLE, AS/-TS/-ADS/, R_W/-W_R/, BE0, BE1/, SIZ0-BHE/-BE2,SIZ1-BE3/, BERR/-TEA/, HALT/-TIP/, BGACK-BB/, CBACK/-TBI/, STERM/-TA/-READYI/, GPIO (0-4)

Parameter	Symbol	Min	Max	Units	Conditions
Input high voltage	V_{IH}	2.0	$V_{DD} + 0.5$	V	-
Input low voltage	V_{IL}	$V_{SS} - 0.5$	0.8	V	-
Output high voltage	V_{OH}	2.4	V_{DD}	V	$I_{OH} = -16\,mA$
Output low voltage	V_{OL}	V_{SS}	0.5	V	$I_{OL} = 16\,mA$
Output high current	I_{OH}	-8.0	-	mA	$V_{OH} = V_{DD} - 0.5\,V$
Output low current	I_{OL}	16.0	-	mA	$V_{OL} = 0.4\,V$
Input leakage current	I_{IN}	-10	10	μA	-
Tristate leakage current	I_{OZ}	-10	10	μA	-

Capacitance

Parameter	Symbol	Min	Max	Units
Input capacitance of input pads	C_I	-	7	pF
Input capacitance of I/O pads	C_{IO}	-	10	pF

NCR TolerANT® Active Negation Technology Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{OH}[1]	Output high voltage	$I_{OH} = 2.5$ mA	2.5	3.1	3.5	V
V_{OL}	Output low voltage	$I_{OL} = 48$ mA	0.1	0.2	0.5	V
V_{IH}	Input high voltage		2.0	-	7.0	V
V_{IL}	Input low voltage	Referenced to V_{SS}	-0.5	-	0.8	V
V_{IK}	Input clamp voltage	$V_{DD} = $ min; $I_I = -20$ mA	-0.66	-0.74	-0.77	V
V_{TH}	Threshold, high to low	-	1.1	1.2	1.3	V
V_{TL}	Threshold, low to high	-	1.5	1.6	1.7	V
$V_{TH} - V_{TL}$	Hysteresis	-	300	350	400	mV
I_{OH}[1]	Output high current	$V_{OH} = 2.5$ Volts	2.5	15	24	mA
I_{OL}	Output low current	$V_{OL} = 0.5$ Volts	100	150	200	mA
I_{OSH}[1]	Short-circuit output high current	Output driving low, pin shorted to V_{DD} supply[2]	-	-	625	mA
I_{OSL}	Short-circuit output low current	Output driving high, pin shorted to V_{SS} supply	-	-	95	mA
I_{LH}	Input high leakage	$-0.5 < V_{DD} < 5.25$ $V_{PIN} = 2.7$ V	-	0.05	10	μA
I_{LL}	Input low leakage	$-0.5 < V_{DD} < 5.25$ $V_{PIN} = 0.5$V	-	-0.05	-10	μA
R_I	Input resistance	SCSI pins [3]	-	20		MΩ
C_P	Capacitance per pin	PQFP	-	8	10	pF
t_R[1]	Rise time, 10% to 90 %	Figure 6-1	9.7	15.0	18.5	ns
t_F	Fall time, 90% to 10%	Figure 6-1	5.2	8.1	14.7	ns
dV_H/dt	Slew rate, low to high	Figure 6-1	0.15	0.23	0.49	V/ns
dV_L/dt	Slew rate, high to low	Figure 6-1	0.19	0.37	0.67	V/ns

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
	Electrostatic Discharge	Mil Std 883C; 3015-7	2	-	-	KV
	Latch-up	-	100	-	-	mA
	Filter Delay	Figure 6-2	20	25	30	ns
	Extended Filter Delay	Figure 6-2	40	50	60	ns

Note: *These values are guaranteed by periodic characterization; they are not 100% tested on every device.*

[1] *Active Negation outputs only: Data, Parity, REQ, ACK*

[2] *Single pin only; irreversible damage may occur if sustained for 1 second*

[3] *SCSI RESET pin has 10kΩ pull-up resistor*

Figure 6-1. Rise and Fall Time Test Conditions
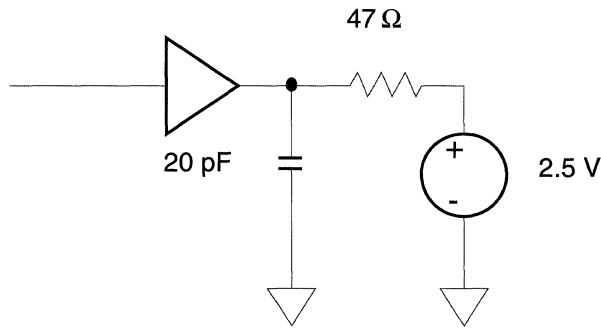
Figure 6-2. SCSI Input Filtering
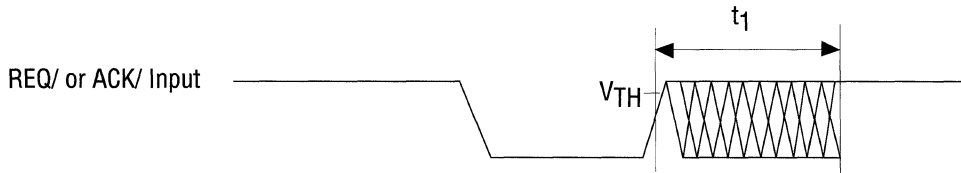
Figure 6-3. Hysteresis of SCSI Receiver
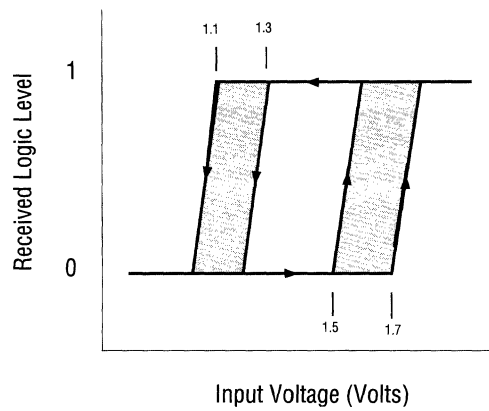
Figure 6-4. Input Current as a Function of Input Voltage
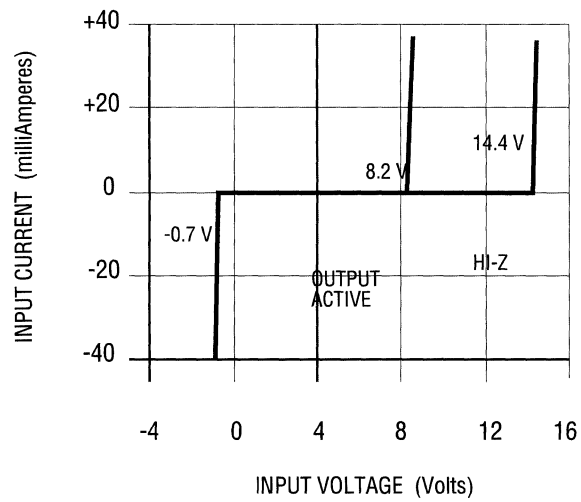
Figure 6-5. Output Current as a Function of Output Voltage
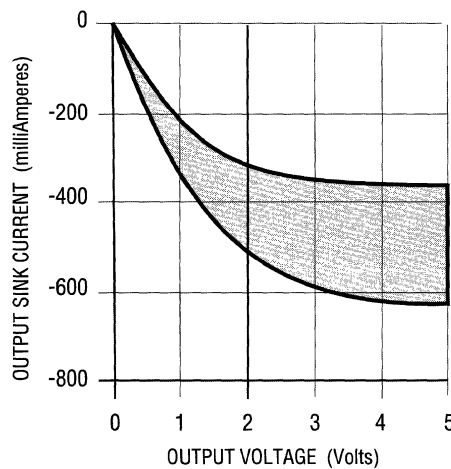
Output Source Current as a Function of Output Voltage (I_{OH})
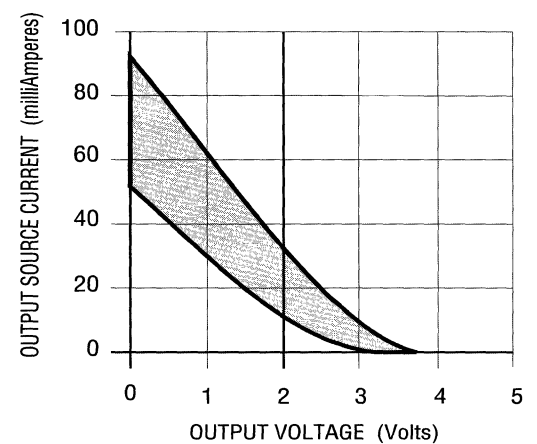
Output Sink Current as a Function of Output Voltage (I_{OL})

AC Characteristics

The AC characteristics described in this section apply over the entire range of operating conditions (refer to the *DC Characteristics* section). Chip timings are based on simulation at worst case voltage, temperature, and processing.

Figure 6-6. Clock Timing
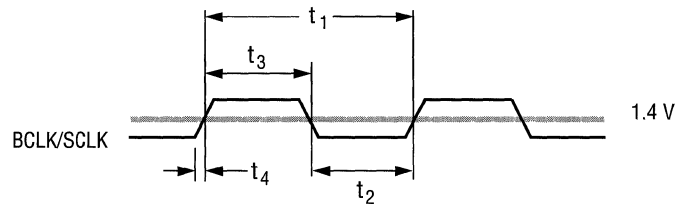
Parameter	Symbol	Min	Max	Units
Bus clock cycle time (BCLK)				
Bus Mode 1	t_1	40	DC	ns
Bus Mode 2, 3, 4		30	DC	ns
SCSI clock cycle time (SCLK)★		15	60	ns
BCLK low time★★				
Bus Mode 1	t_2	17	DC	ns
Bus Mode 2, 3, 4		14	DC	ns
SCLK low time★★		6	33	ns
BCLK high time★★				
Bus Mode 1	t_3	17	-	ns
Bus Mode 2, 3, 4		14	-	ns
SCLK high time★★		6	33	ns
BCLK slew rate	t_4	1	-	V/ns
SCLK slew rate		1	-	V/ns

★ *This parameter must be met to insure SCSI timings are within specification.*

★★ *Duty cycle not to exceed 60/40.*

Figure 6-7. Reset Input
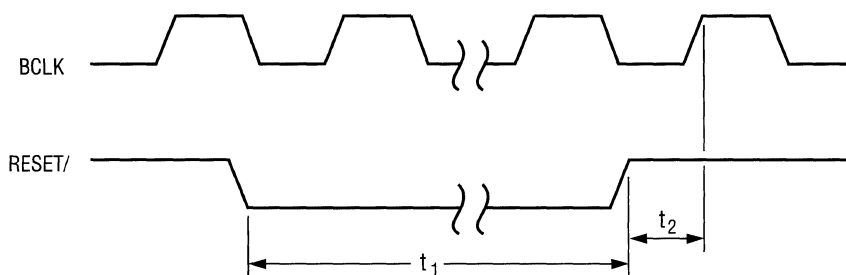
Parameter	Symbol	Min	Max	Units
Reset pulse width	t_1	10	-	BCLK
Reset deasserted setup to BCLK high	t_2	10	-	ns

Figure 6-8. Interrupt Output
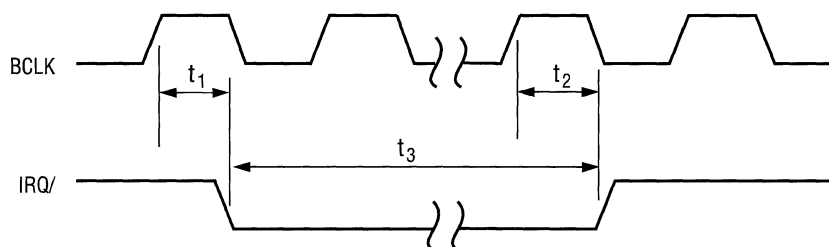
Parameter	Symbol	Min	Max	Units
BCLK high to IRQ/ low	t_1	-	20	ns
BCLK high to IRQ/ high	t_2	-	58	ns
IRQ/ deassertion time	t_3	3	-	BCLK

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Bus Mode 1 Slave Cycle

Bus Mode 1 Slave Read Sequence

1) R_W/, Address and Size lines are asserted by the CPU.

2) Address Strobe is asserted by the CPU.

3) Chip Select is validated by the 53C720 on any following rising edge of BCLK.

4) Cache Burst Acknowledge is deasserted by the 53C720.

5) Two clock cycles of wait state are inserted (these wait states are required) and the Data lines are asserted by the 53C720.

6) Slave Acknowledge is asserted by the 53C720 if the cycle ends normally or Bus Error is asserted if a bus error is detected.

7) STERM/ is sampled.

8) Address Strobe is deasserted by the CPU.

9) Slave Acknowledge or Bus Error is deasserted by the 53C720 and the Data lines are tristated by the 53C720.

Bus Mode 1 Slave Read Timings

Parameter	Symbol	Min	Max	Units
AS/ setup to CS/ clocked active	t_1	5	-	ns
A(6-0), SIZ(1-0), R-W/ setup to AS/	t_2	4	-	ns
A(6-0), SIZ(1-0), R-W/ hold from AS/	t_3	8	-	ns
CS/ setup to BCLK high after AS/	t_4	5	-	ns
CS/ hold from BCLK high after AS/	t_5	5	-	ns
BCLK high to CBACK/ high	t_6	5	30	ns
AS/ high to CBACK/ low	t_7	3	17	ns
BCLK high to SLACK/, BERR/ low	t_8	-	22	ns
AS/ high to SLACK/, BERR/ high	t_9	-	22	ns
STERM/ setup to BCLK high	t_{10}	3	-	ns
STERM/ hold from BCLK high	t_{11}	7	-	ns
BCLK high to data bus driven	t_{12}	8	28	ns
BCLK high to read data valid	t_{13}	-	75	ns
AS/ high to data bus high-Z	t_{14}	7	32	ns

Figure 6-9. Bus Mode 1 Slave Read Cycle
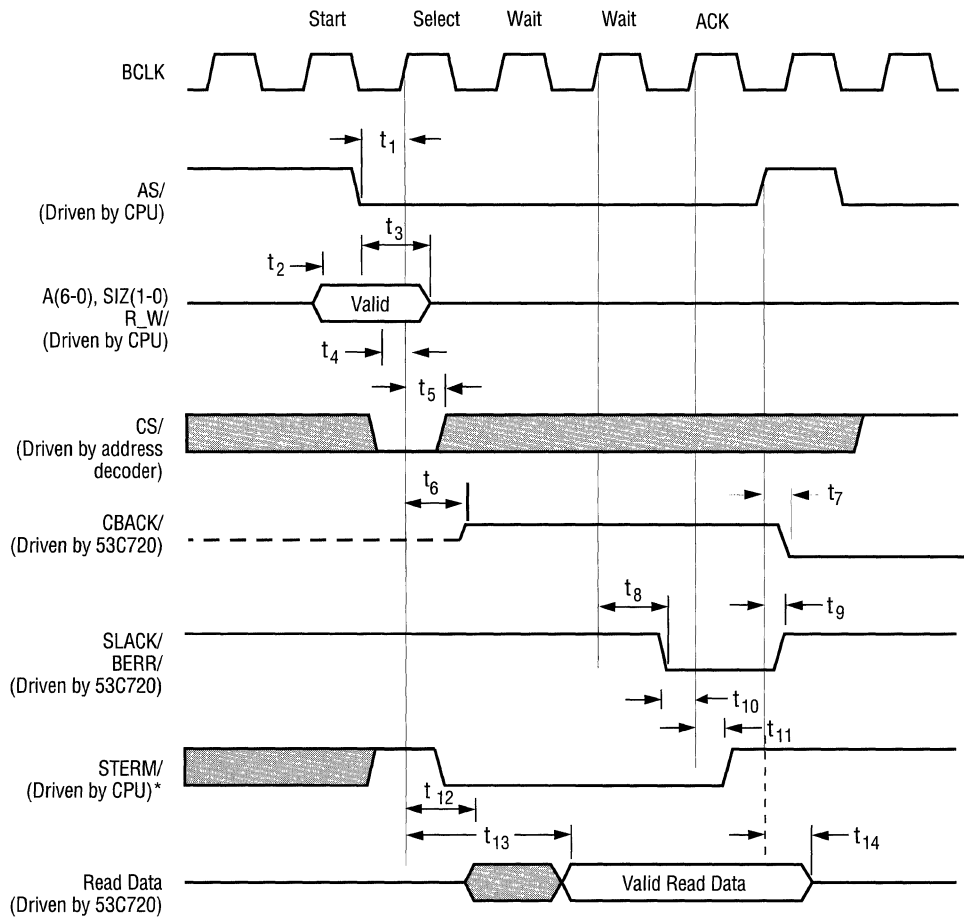
* *This signal may be driven by the 53C720 if the Enable ACK bit is set (DCNTL bit 5).*
   See the explanation in Chapter 2 of the 53C720 Data Manual for use of this signal as an
   output.

Bus Mode 1 Slave Write Sequence

1) R_W/, Address and Size lines are asserted by the CPU.

2) Address Strobe is asserted by the CPU.

3) Chip Select is validated by the 53C720 on any following rising edge of BCLK.

4) Cache Burst Acknowledge is deasserted by the 53C720.

5) The Data lines are asserted by the CPU.

6) Slave Acknowledge is asserted by the 53C720 if the cycle ends normally or Bus Error is asserted if a bus error is detected.

7) STERM/ is sampled.

8) Address Strobe is deasserted by the CPU.

9) Slave Acknowledge or Bus Error is deasserted by the 53C720.

Bus Mode 1 Slave Write Timings

Parameter	Symbol	Min	Max	Units
AS/ setup to CS/ clocked active	t_1	5	-	ns
A(6-0), SIZ(1-0), R-W/ setup to AS/	t_2	4	-	ns
A(6-0), SIZ(1-0), R-W/ hold from AS/	t_3	8	-	ns
CS/ setup to BCLK high after AS/	t_4	5	-	ns
CS/ hold from BCLK high after AS/	t_5	5	-	ns
BCLK high to CBACK/high	t_6	5	30	ns
AS/ high to CBACK/ low	t_7	3	17	ns
BCLK high to SLACK/, BERR/ low	t_8	-	22	ns
AS/ high to SLACK/, BERR/ high	t_9	-	22	ns
STERM/ (input) setup to BCLK high	t_{10}	3	-	ns
STERM/ (input) hold from BCLK high	t_{11}	7	-	ns
Write data setup to BCLK low	t_{12}	4	-	ns
Write data hold from BCLK low	t_{13}	6	-	ns

Figure 6-10. Bus Mode 1 Slave Write Cycle
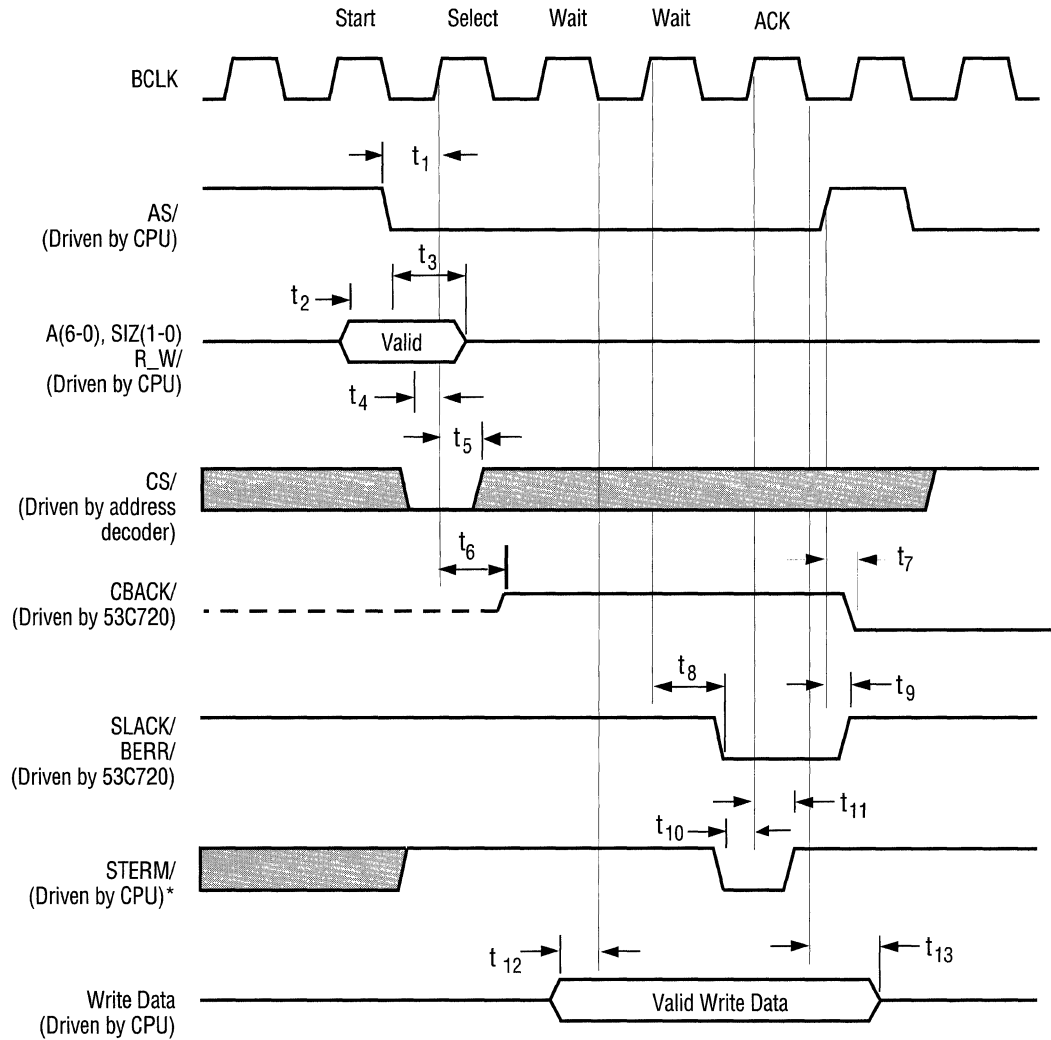
* *This signal may be driven by the 53C720 if the Enable ACK bit is set (DCNTL bit 5). See the explanation in Chapter 2 of the 53C720 Data Manual for use of this signal as an output.*

Note: data is latched on the rising edge of ACK/ when SLACK/ is asserted. Wait states cannot be inserted by using STERM/.

Bus Mode 1 Host Bus Arbitration

Bus Arbitration Sequence

1) The 53C720 internally determines bus mastership is required. If appropriate, FETCH/ is asserted.

2) Bus Request is asserted.

3) The 53C720 waits for Bus Grant and checks that Bus Grant Acknowledge is deasserted. Then the 53C720 asserts Bus Grant Acknowledge and Master, and deasserts Bus Request.

Bus Mode 1 Host Bus Arbitration Timings

Parameter	Symbol	Min	Max	Units
SC0 high to BR/ low*	t_1	1	2	BCLK
BCLK high to SC0 low on last cycle*	t_2	5	28	ns
BCLK high to BR/ low	t_3	4	20	ns
BCLK high to BR/ high	t_4	5	25	ns
BG/ setup to BCLK high any rising edge after BR/)	t_5	4	-	ns
BG/ hold from BCLK high (any rising edge after BR/)	t_6	5	-	ns
BGACK/ setup to BCLK high (any rising edge after BR/)	t_7	5	-	ns
BCLK high to BGACK/ low	t_8	4	24	ns
BCLK high to BGACK/ high	t_9	3	19	ns
BCLK high to BGACK/ high-Z	t_{10}	7	32	ns
BCLK high to MASTER/ low	t_{11}	5	22	ns
BCLK high to MASTER/ high	t_{12}	6	26	ns
BCLK high to FETCH/ low	t_{13}	5	36	ns
BCLK high to FETCH/ high	t_{14}	5	36	ns
FETCH/ low to BR/ low	t_{15}	1	2	BCLK
BGACK/ high to FETCH/ high**	t_{16}	1	2	BCLK

* *When Snoop Mode bit 0 of CTEST3 is set to 1.*

** *During a retry operation, Fetch/ will remain low until a successful completion of the opcode fetch or a fatal bus error.*

Figure 6-11. Host Bus Arbitration, Bus Mode 1
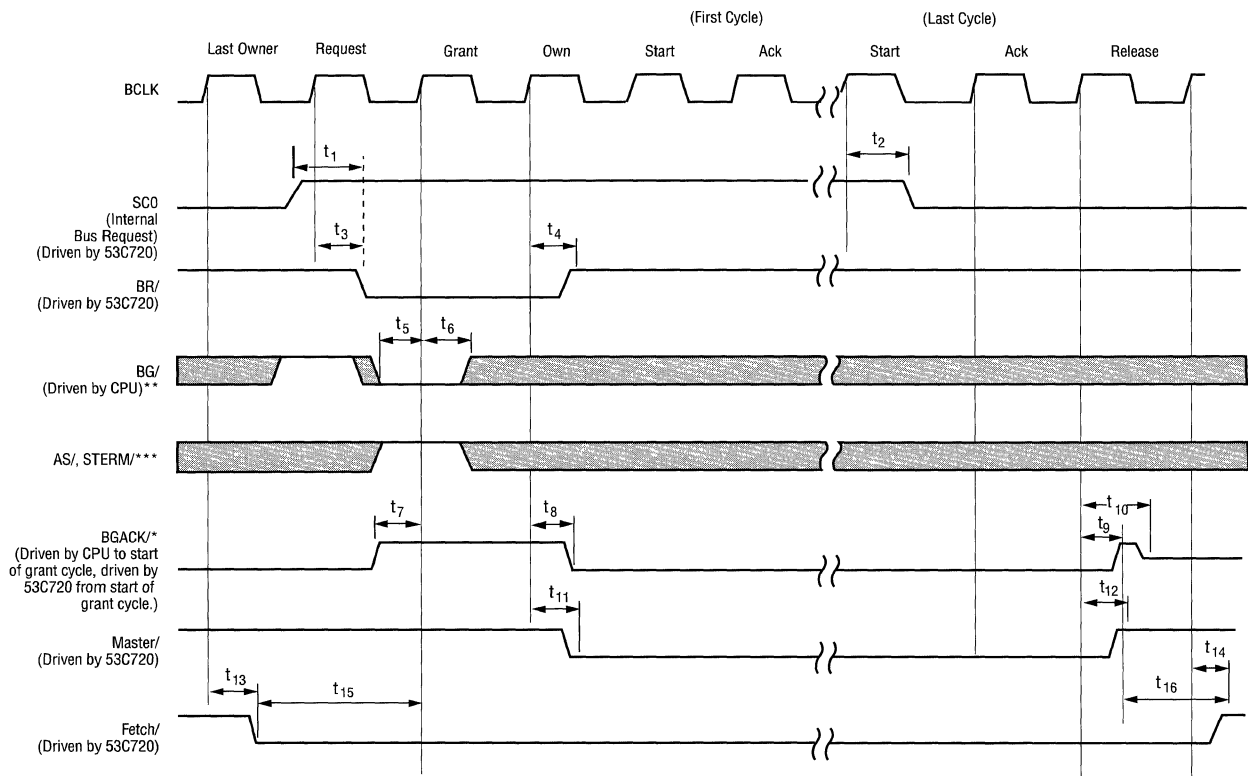
★ If the Fast Arbitration bit is set (DCNTL bit 1), the 53C720 will drive the BGACK/ signal as soon as it receives a Bus Grant. One clock cycle of arbitration will be saved.

★★★ AS/ and STERM/ must be deasserted at this point for the 53C720 to take control of the bus.

Note: the 53C720 will periodically assert the BR/ signal and receive a SCSI interrupt at the same time. When this happens, the chip will wait for the BG/ signal to complete the normal bus arbitration handshake. The chip no longer wants host bus access - it deasserts the BR/, MASTER/, and all control lines after one BCLK, and does not assert TS/, the signal that indicates a valid bus cycle is starting. The chip will next generate an interrupt, which the system may then service.

Bus Mode 1 Fast Arbitration

Fast Arbitration Sequence*

1) The 53C720 internally determines bus mastership is required. If appropriate, FETCH/ is asserted.

2) Bus Request is asserted.

3) The 53C720 waits for Bus Grant. The 53C720 becomes bus master asynchronously on the leading edge of BG/. Then the 53C720 asynchronously asserts Bus Grant Acknowledge and Master, and deasserts Bus Request.

4) The 53C720 issues a start cycle on the next rising edge of BCLK.

* *The Fast Arbitration bit must be set.*

Note: *In fast arbitration mode, the 53C720 will take bus ownership on the assertion of BG/ regardless of the state of BR/ or BGACK/.*

Bus Mode 1 Fast Arbitration Timings

Parameter	Symbol	Min	Max	Units
BCLK high to BR/ asserted	t_1	-	20	ns
BG/ setup to BCLK high	t_2	12	-	ns
BG/ asserted to BR/ deasserted	t_3	-	22	ns
BG/ asserted to BGACK/ asserted	t_4	-	20	ns
BG/ asserted to MASTER/ asserted	t_5	-	16	ns
BG/ hold after BR/ deasserted*	t_6	0	-	ns
BR/ asserted to BG/ asserted	t_7	0	-	ns

* *BG/ mzy not be asserted prior to BR/.*

Figure 6-12. Bus Mode 1 Fast Arbitration
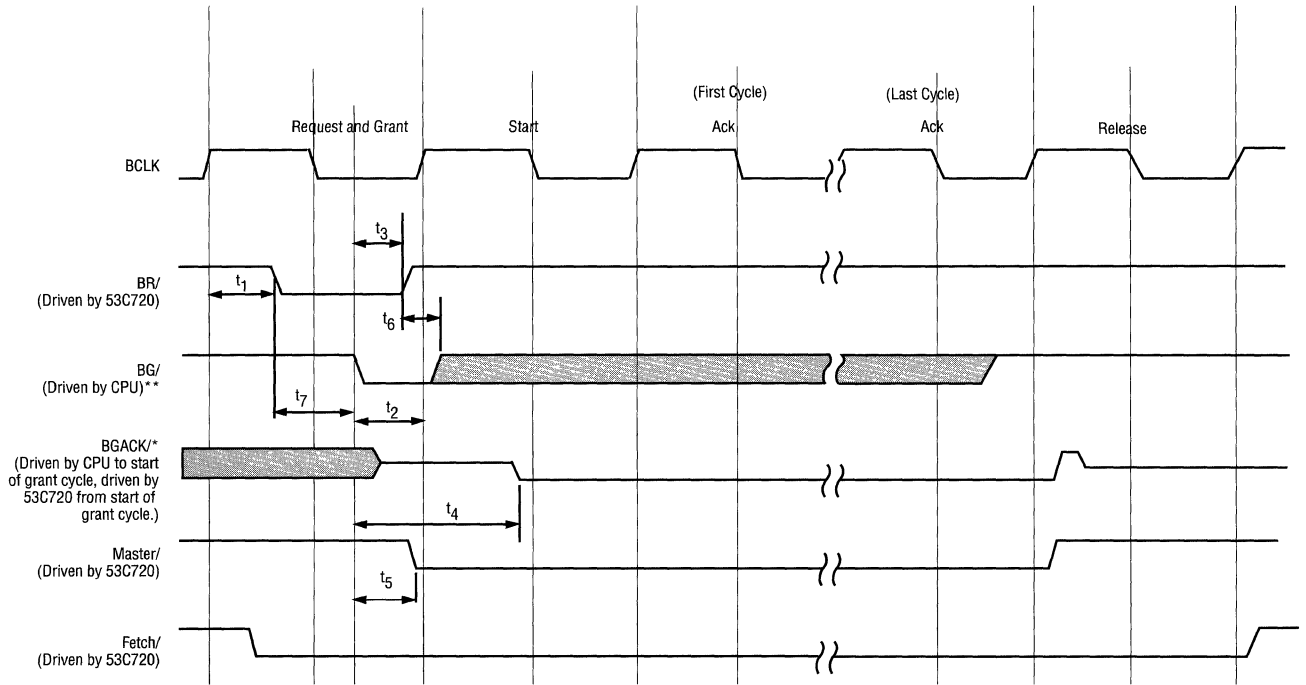
Bus Mode 1 Master Cycle

Bus Mode 1 Bus Master Read Sequence

1) The 53C720 has attained bus mastership.

2) The 53C720 asserts the R_W/, Snoop Control, Function Control and General Purpose lines.

3) The 53C720 asserts the Address and Size lines.

4) The 53C720 asserts Address Strobe, Cache Burst Request (if bursting is enabled), and Data Strobe.

5) The 53C720 waits for Synchronous Termination, Valid Data, Cache Burst Acknowledge, Bus Error and HALT.

   • If Cache Burst Acknowledge is asserted, attempt bursting.

   • If Bus Error and HALT are asserted, attempt a retry.

   • If Synchronous Termination is asserted without Bus Error or HALT, and the 53C720 requires more cycles, then return to function 3.

6) Upon acknowledge of the last bus cycle, the 53C720 deasserts Master and Bus Grant Acknowledge.

7) The 53C720 floats the Control and Address lines.

Bus Mode 1 Bus Master Read Timings

| Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to AS/ driven	t_3	5	32	ns
BCLK low to AS/ low	t_4	3	15	ns
BCLK low to AS/ high	t_5	3	15	ns
BCLK high to AS/ high-Z	t_6	7	34	ns
STERM/ setup to BCLK high	t_7	3	-	ns
STERM/hold from BCLK high	t_8	7	-	ns
BCLK high to SIZ(1-0), A(31-0) driven	t_9	5	28	ns
BCLK high to SIZ(1-0), A(31-0) valid	t_{10}	4	20	ns
BCLK high to SIZ(1-0), A(31-0) high-Z	t_{11}	7	34	ns
BCLK high to R_W/, SC(1-0), FC(2-0), UPSO driven and valid	t_{12}	5	28	ns
BCLK high to R_W/, SC(1-0), FC(2-0), UPSO high-Z	t_{13}	6	30	ns
Read Data setup to BCLK low	t_{14}	4	-	ns
Read Data hold from BCLK low	t_{15}	6	-	ns
BCLK high to DS/ driven	t_{16}	5	28	ns
BCLK low to DS/ low	t_{17}	3	17	ns
BCLK low to DS/ high	t_{18}	3	17	ns
BCLK high to DS/ high-Z	t_{19}	7	32	ns
BCLK high to CBREQ/ driven	t_{20}	5	28	ns
BCLK low to CBREQ/ low	t_{21}	3	18	ns
BCLK low to CBREQ/ high	t_{22}	3	18	ns
BCLK high to CBREQ/ high-Z	t_{23}	7	32	ns
CBACK/ setup to BCLK low	t_{24}	8	-	ns
CBACK/ hold from BCLK low	t_{25}	4	-	ns
BERR/, HALT/ setup to BCLK low	t_{26}	6	-	ns
BERR/, HALT hold from BCLK low	t_{27}	4	-	ns

Figure 6-13. Bus Mode 1 Bus Master Read (Non-Cache Line Burst)
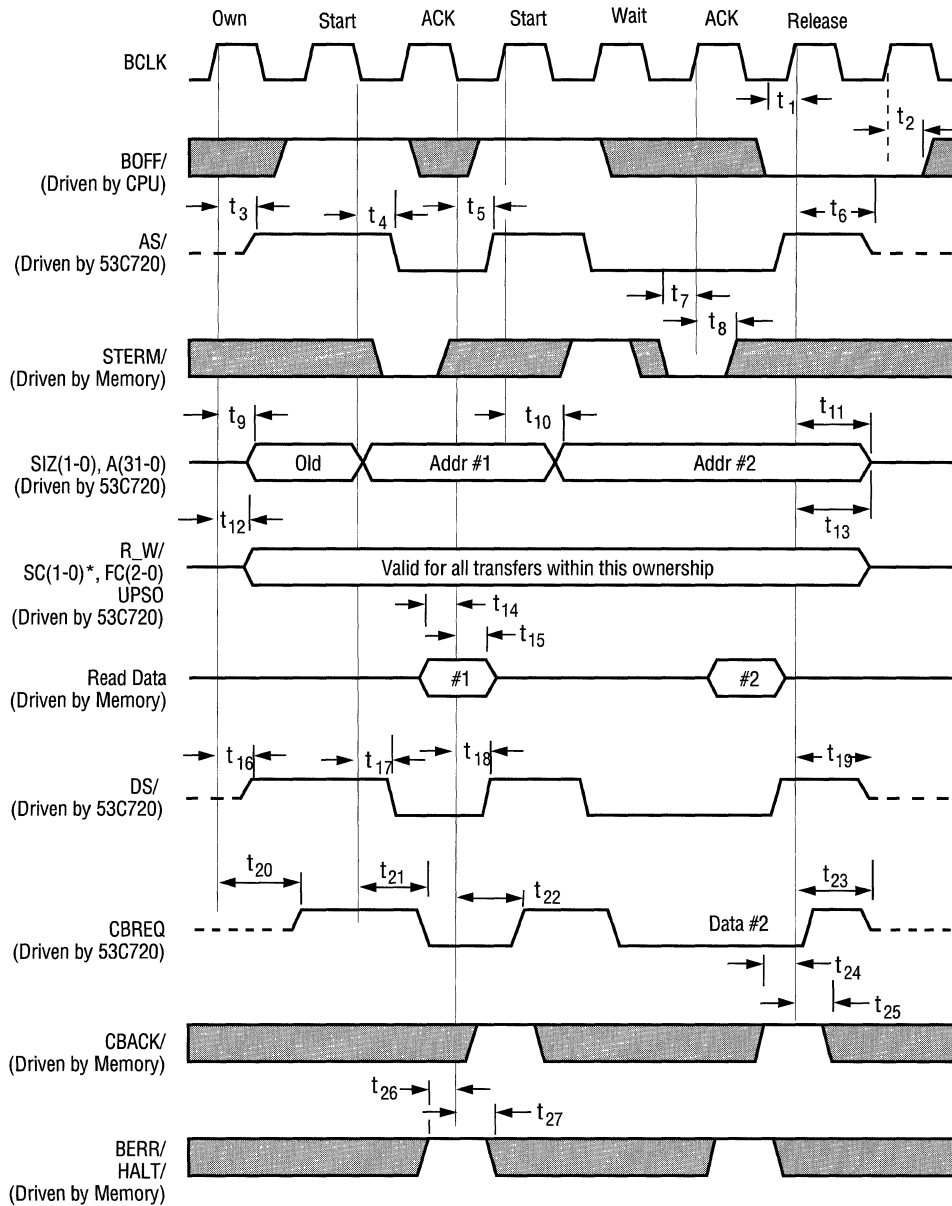
* $SC(1-0)$ *timings apply only if Snoop Mode bit 0 of CTEST3 = 0.*

Figure 6-14. Bus Mode 1 Bus Master Read (Cache Line Burst)
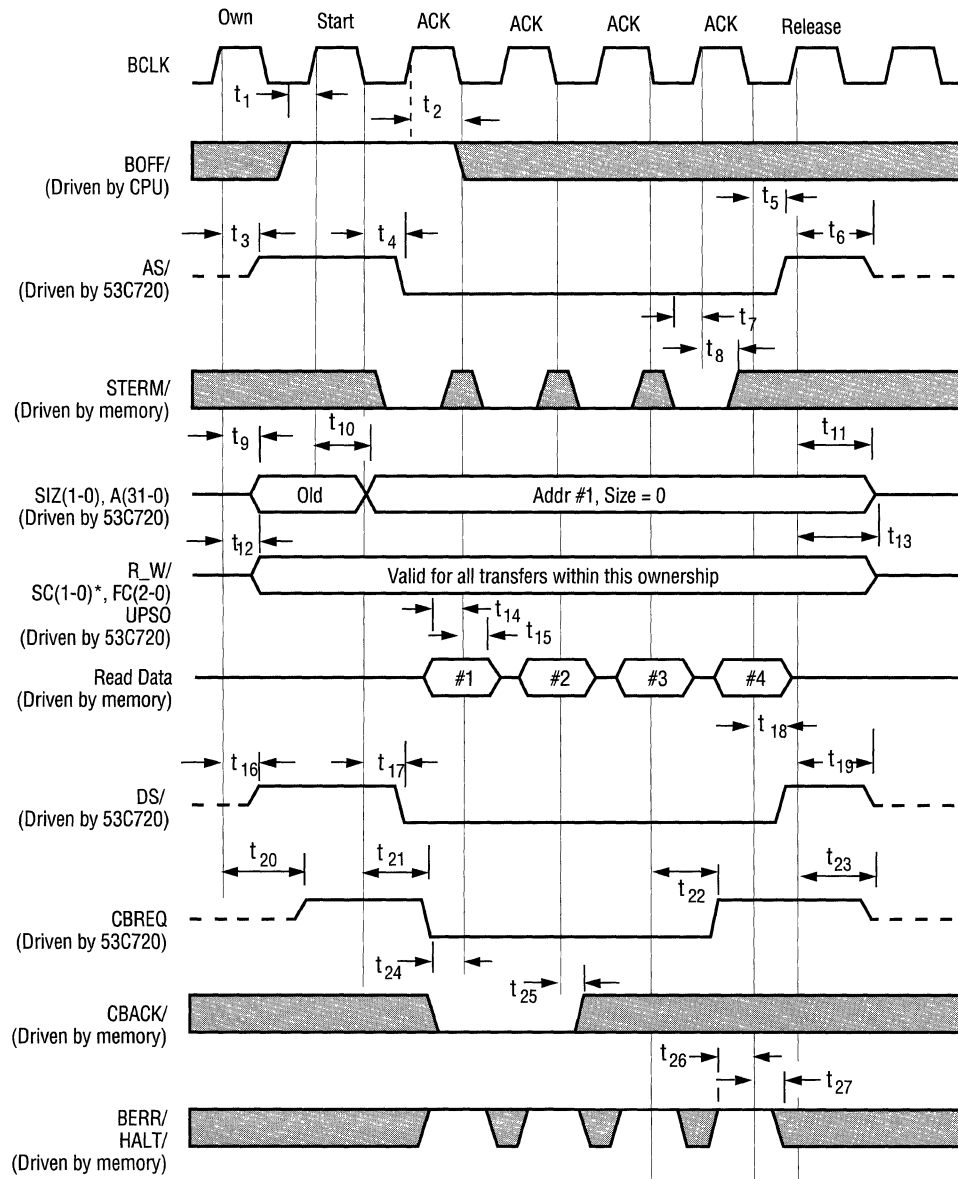
* *SC(1-0) timings apply only if Snoop Mode bit 0 of CTEST3 = 0.*

Bus Mode 1 Bus Master Write Sequence

1) The 53C720 has attained bus mastership.

2) The 53C720 asserts the R_W/, Snoop Control, Function Control and General Purpose lines.

3) The 53C720 asserts the Address, Size and Data lines.

4) The 53C720 asserts Address Strobe and Cache Burst Request.

5) The 53C720 asserts Data Strobe.

6) The 53C720 waits for Synchronous Termination, Cache Burst Acknowledge, Bus Error and HALT.

   • If Cache Burst Acknowledge is asserted, attempt bursting.

   • If Bus Error and HALT are asserted, attempt a retry.

   • If Synchronous Termination is asserted without Bus Error or HALT, and the 53C720 requires more cycles, then return to function 3.

7) Upon acknowledge of the last bus cycle, the 53C720 deasserts Master and Bus Grant Acknowledge.

8) The 53C720 floats the Control, Address and Data lines.

Bus Mode 1 Bus Master Write Timings

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to AS/ driven	t_3	5	32	ns
BCLK low to AS/ low	t_4	3	15	ns
BCLK low to AS/ high	t_5	3	15	ns
BCLK high to AS/ high-Z	t_6	7	34	ns
STERM/ setup to BCLK high	t_7	3	-	ns
STERM/ hold from BCLK high	t_8	7	-	ns
BCLK high to SIZ(1-0), A(31-0) driven	t_9	5	28	ns
BCLK high to SIZ(1-0), A(31-0) valid	t_{10}	4	20	ns
BCLK high to SIZ(1-0), A(31-0) high-z	t_{11}	7	34	ns
BCLK high to R_W/, SC(1-0), FC(2-0), UPSO driven and valid	t_{12}	5	28	ns
BCLK high to R_W/, SC(1-0), FC(2-0), UPSO high-Z	t_{13}	6	30	ns
BCLK high to Write Data driven	t_{14}	6	34	ns
BCLK high to Write Data valid	t_{15}	6	24	ns
BCLK high to Data high-Z	t_{16}	6	32	ns
BCLK high to DS/ driven	t_{17}	5	32	ns
BCLK low to DS/ low	t_{18}	3	17	ns
BCLK low to DS/ high	t_{19}	3	17	ns
BCLK high to DS/ high-Z	t_{20}	7	34	ns
BCLK high to CBREQ/ driven	t_{21}	5	30	ns
BCLK low to CBREQ/ low	t_{22}	3	18	ns
BCLK low to CBREQ/ high	t_{23}	3	18	ns
BCLK high to CBREQ/ high-Z	t_{24}	7	32	ns
CBACK/ setup to BCLK high	t_{25}	8	-	ns
CBACK/ hold from BCLK high	t_{26}	4	-	ns
BERR/, HALT/ setup to BCLK low	t_{27}	6	-	ns
BERR/, HALT hold from BCLK low	t_{28}	4	-	ns

Figure 6-15. Bus Mode 1 Bus Master Write (Non-Cache Line Burst)
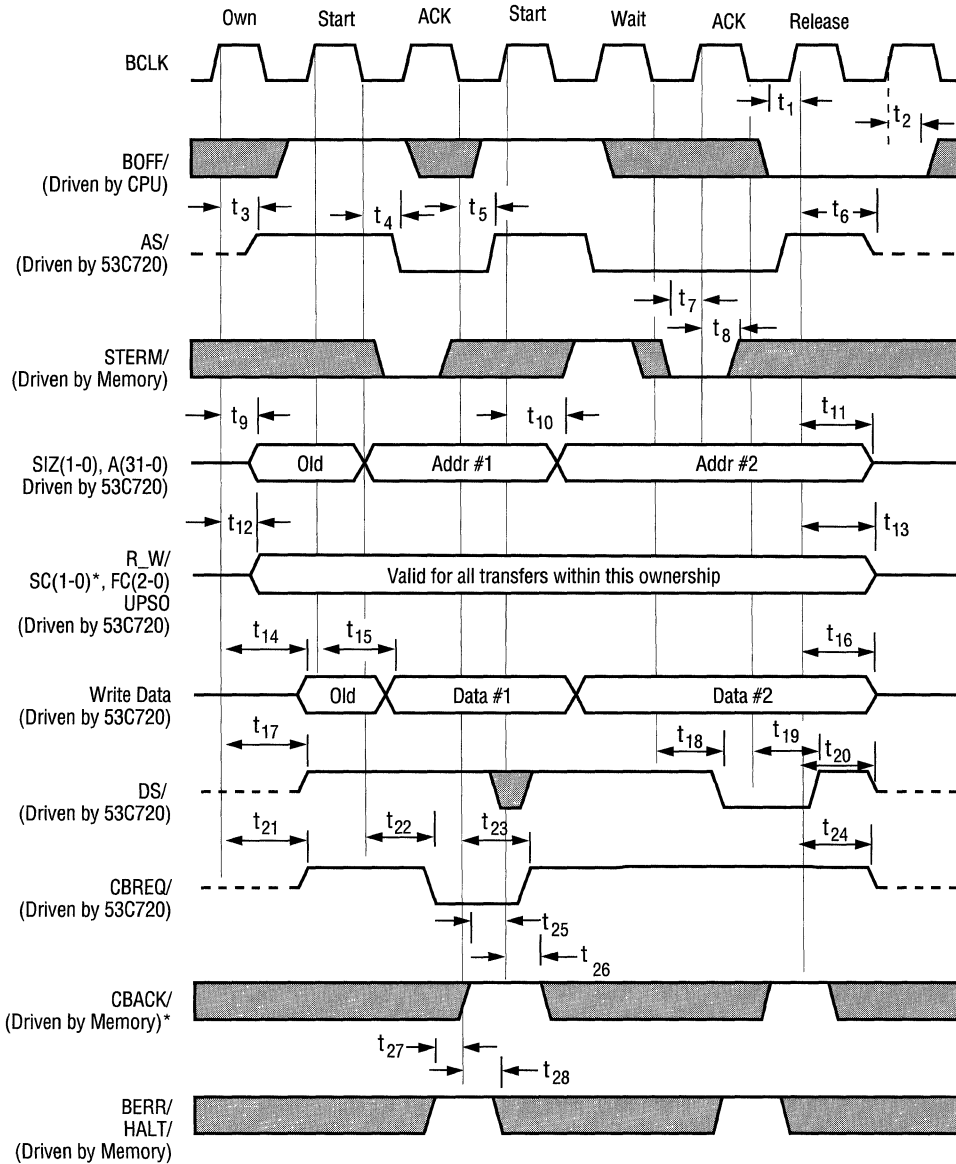
* *SC(1-0) timings apply only if Snoop Mode bit 0 of CTEST3 = 0.*

Figure 6-16. Bus Mode 1 Bus Master Write (Cache Line Burst)
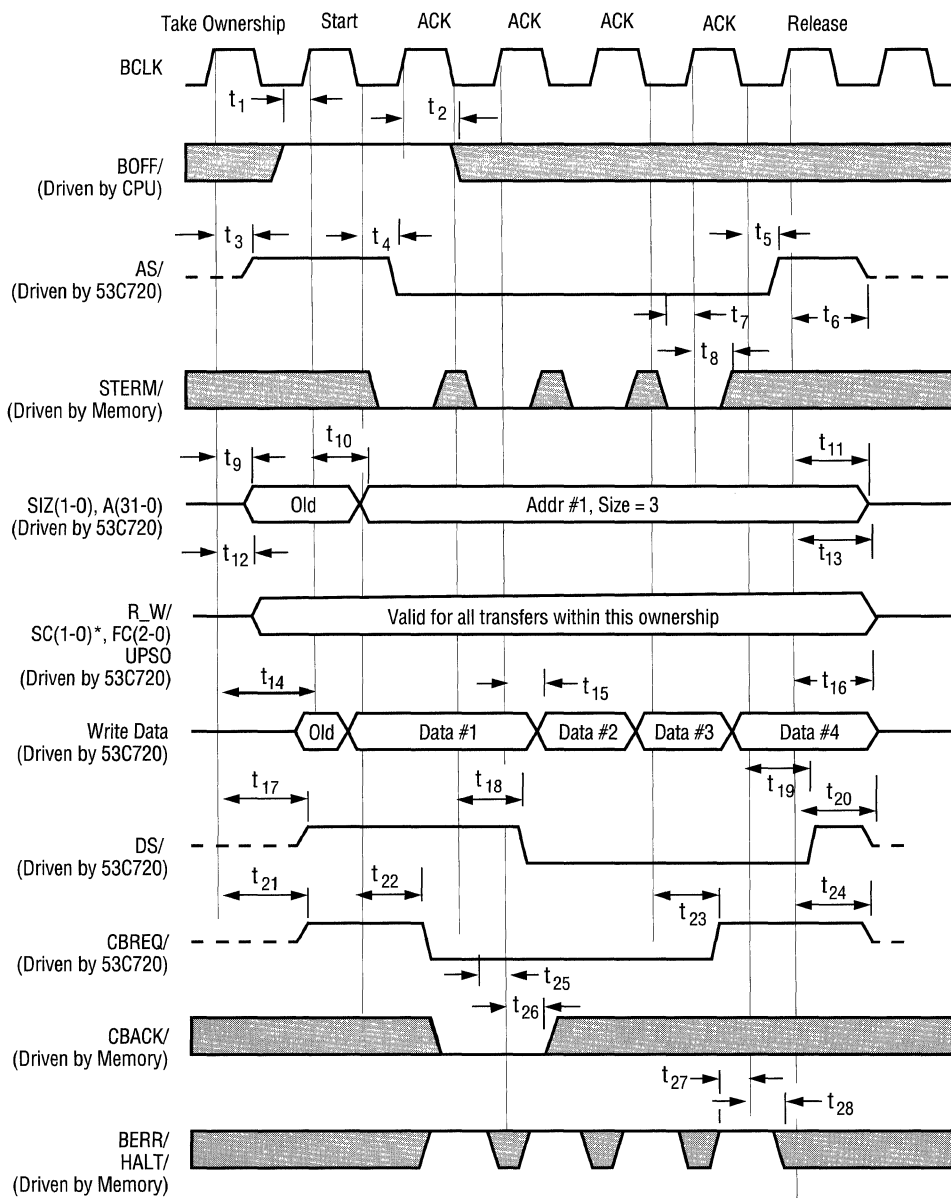
* *SC(1-0) timings apply only if Snoop Mode bit 0 of CTEST3 = 0.*

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Bus Mode 2 Slave Cycle

Bus Mode 2 Slave Read Sequence

1) R_W/, Address, Transfer Start and the Size lines are asserted by the CPU.

2) Chip Select is validated by the 53C720 on any following rising edge of BCLK.

3) Transfer Burst Inhibit is asserted.

4) Transfer Start is deasserted by the CPU.

5) Three clock cycles of wait state are inserted (these wait states are required) and the Data lines are asserted.

6) Slave Acknowledge is asserted by the 53C720, if no errors are detected.

7) If a bus error is detected, only Transfer Error Acknowledge is asserted and the bus cycle ends on the next rising edge of BCLK.

8) Slave Acknowledge or Transfer Error Acknowledge is deasserted.

9) The 53C720 waits for Transfer Acknowledge to be asserted and then ends the slave cycle, if no errors are detected.

10) The Data lines are tristated by the 53C720.

Bus Mode 2 Slave Read Timings

Parameter	Symbol	Min	Max	Units
TS/ setup to BCLK high	t_1	4	-	ns
TS/ hold from BCLK high	t_2	4	-	ns
CS/ setup to BCLK high after TS/	t_3	5	-	ns
CS/ hold from BCLK high after TS/	t_4	5	-	ns
BCLK high to TBI/ low	t_5	5	30	ns
BCLK high to TBI/ high	t_6	4	22	ns
BCLK high to SLACK/, TEA/ low	t_7	5	20	ns
BCLK high to SLACK/, TEA/ high	t_8	4	20	ns
TA/ setup to BCLK high during or after SLACK/, TEA/	t_9	9	-	ns
TA/ hold from BCLK high during or after SLACK/, TEA/	t_{10}	5	-	ns
BCLK high to data bus driven	t_{11}	8	28	ns
BCLK high to read data valid	t_{12}	-	75	ns
BCLK high to data bus high-Z	t_{13}	7	34	ns
A(6-0), SIZ(1-0), R_W/ setup to BCLK high	t_{14}	4	-	ns
A(6-0), SIZ(1-0), R_W/ hold from BCLK high	t_{15}	12	-	ns
BCLK high to TBI/ high-z	t_{16}	8	32	ns
BCLK high to TEA/ driven	t_{17}	8	27	ns
BCLK high to TEA/ high-z	t_{18}	9	34	ns
BCLK high to TA/ driven	t_{19}	8	27	ns
BCLK high to TA/ high-z	t_{20}	9	33	ns

Figure 6-17. Bus Mode 2 Slave Read
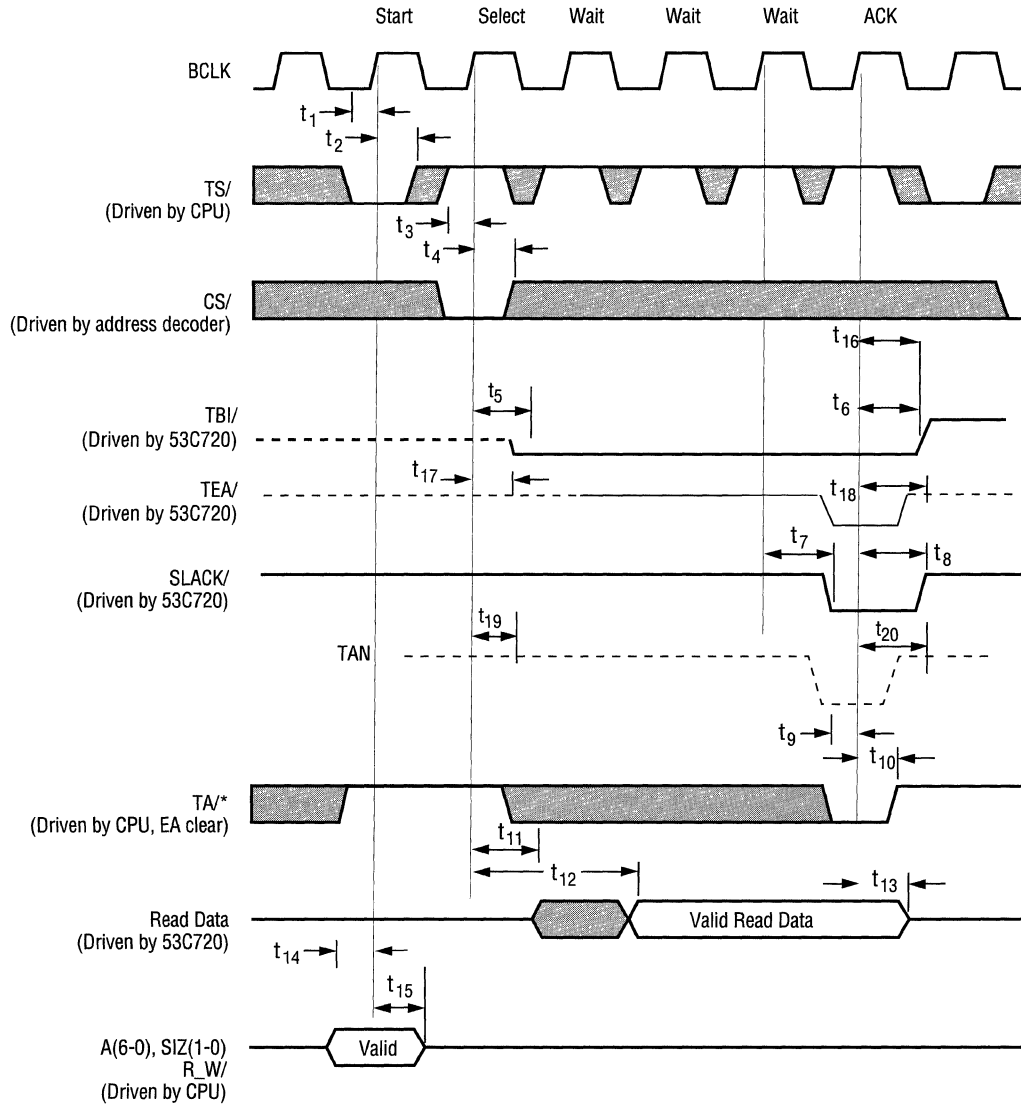
* *This signal may be driven by the 53C720 if the Enable Ack bit is set (DCNTL bit 5). See the explanation in chapter 2 of the 53C720 Data Manual for use of this signal as an output.*

Bus Mode 2 Slave Write Sequence

1) R_W/, Address, Transfer Start and the Size lines are asserted by the CPU.

2) Chip Select is validated by the 53C720 on any following rising edge of BCLK.

3) Transfer Burst Inhibit is asserted.

4) Transfer Start is deasserted by the CPU.

5) The Data lines are asserted by the CPU.

6) Three clock cycles of wait state are inserted (These wait states are required).

7) Slave Acknowledge is asserted by the 53C720, if no errors are detected

8) If a bus error is detected, only Transfer Error Acknowledge is asserted and the bus cycle ends on the next rising edge of BCLK.

9) The 53C720 waits for Transfer Acknowledge to be asserted and then ends the slave cycle, if no error.

10) Slave Acknowledge or Transfer Error Acknowledge is deasserted.

Bus Mode 2 Slave Write Timings

Parameter	Symbol	Min	Max	Units
TS/ setup to BCLK high	t_1	4	-	ns
TS/ hold from BCLK high	t_2	4	-	ns
CS/ setup to BCLK high after TS/	t_3	5	-	ns
CS/ hold from BCLK high after TS/	t_4	5	-	ns
BCLK high to TBI/ low	t_5	5	30	ns
BCLK high to TBI/ high	t_6	4	22	ns
BCLK high to SLACK/, TEA/ low	t_7	5	20	ns
BCLK high to SLACK/, TEA/ high	t_8	4	20	ns
TA/ setup to BCLK high during or after SLACK/, TEA/	t_9	9	-	ns
TA/ hold from BCLK high during or after SLACK/, TEA/	t_{10}	5	-	ns
Valid write data setup to BCLK high	t_{11}	6	-	ns
Valid write data hold from BCLK high	t_{12}	14	-	ns
A(6-0), SIZ(1-0), R_W/ setup to BCLK high	t_{13}	4	-	ns
A(6-0), SIZ(1-0), R_W/ hold from BCLK high	t_{14}	12	-	ns

Figure 6-18. Bus Mode 2 Slave Write
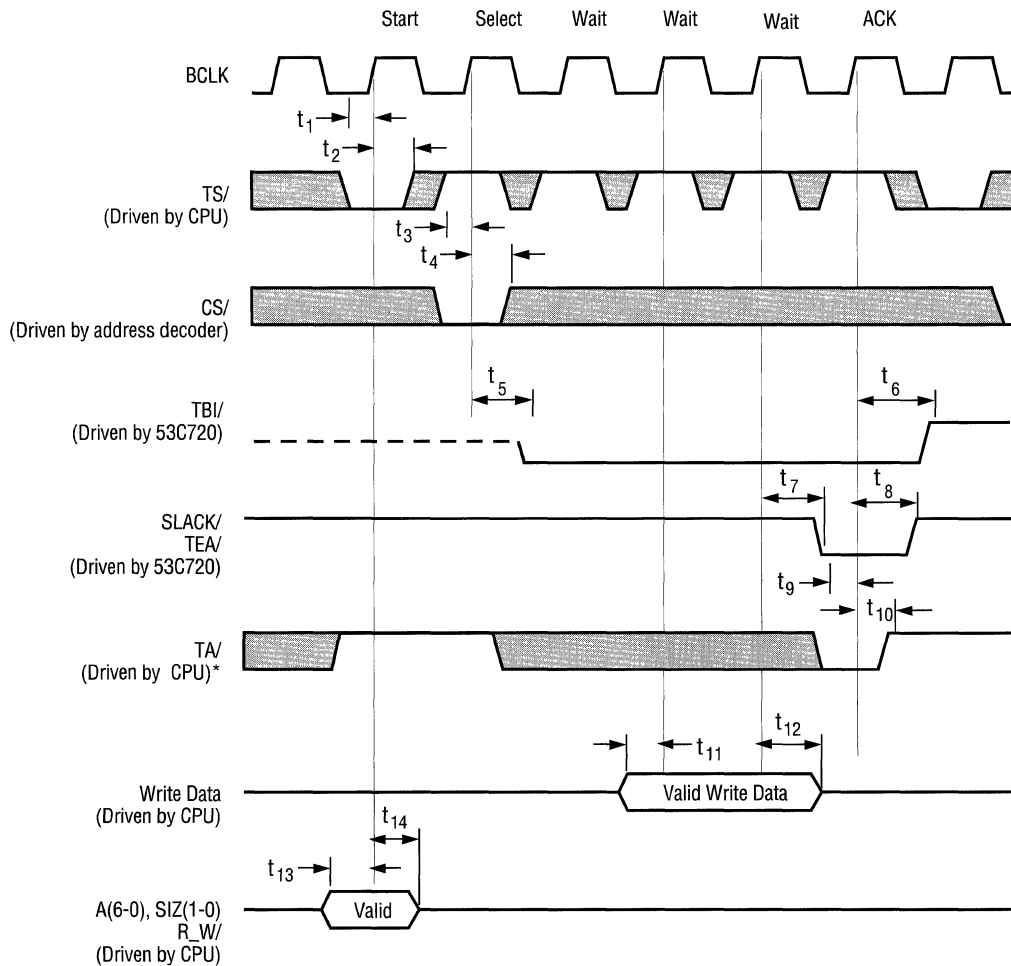
* *This signal may be driven by the 53C720 if the Enable Ack bit is set (DCNTL bit 5).*
See the explanation in chapter 2 of the 53C720 Data Manual for use of this signal as an
output.

Bus Mode 2 Host Bus Arbitration

Bus Arbitration Sequence

1) The 53C720 internally determines bus mastership is required. If appropriate, FETCH/ is asserted.

2) Bus Request is asserted.

3) The 53C720 waits for Bus Grant and checks that Bus Grant Acknowledge is deasserted. Then the 53C720 asserts Bus Grant Acknowledge and Master, and deasserts Bus Request.

Bus Mode 2 Host Bus Arbitration Timings

Parameter	Symbol	Min	Max	Units
SC0 high to BR/ low*	t_1	1	2	BCLK
BCLK high to SC0 low on last cycle*	t_2	5	28	ns
BCLK high to BR/ low	t_3	4	20	ns
BCLK high to BR/ high	t_4	5	25	ns
BG/ setup to BCLK high (any rising edge after BR/)	t_5	4	-	ns
BG/ hold from BCLK high (any rising edge after BR/)	t_6	5	-	ns
BB/ setup to BCLK high (any rising edge after BR/)	t_7	4	-	ns
BCLK high to BB/ low	t_8	4	24	ns
BCLK high to BB/ high	t_9	3	19	ns
BCLK high to BB/ high-Z	t_{10}	7	32	ns
BCLK high to MASTER/ low	t_{11}	5	22	ns
BCLK high to MASTER/ high	t_{12}	6	26	ns
BCLK high to FETCH/ low	t_{13}	5	36	ns
BCLK high to FETCH/ high	t_{14}	5	36	ns
FETCH/ low to BR/ low	t_{15}	1	2	BCLK
BB/ high to FETCH/ high**	t_{16}	1	2	BCLK

When Snoop Mode bit 0 of CTEST 3 is set to 1.

**During a retry operation, FETCH/ will remain low until successful completion of an opcode fetch or a fatal bus error.*

Figure 6-19. Host Bus Arbitration, Bus Mode 2
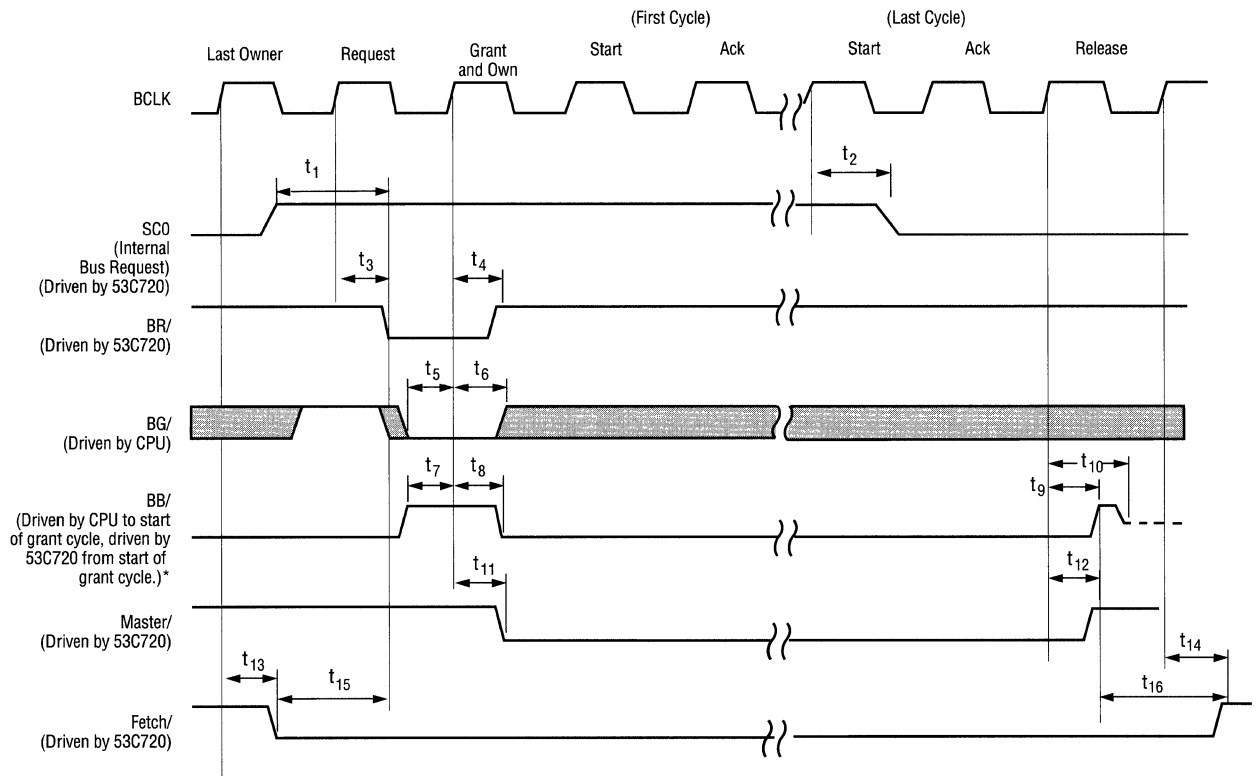
* If the Fast Arbitration bit is set (DCNTL bit 1), the 53C720 will drive the Bus Grant Acknowledge signal as soon as it receives a bus grant. One clock cycle of arbitration will be saved.

Note: the 53C720 will periodically assert the BR/ signal and receive a SCSI interrupt at the same time. When this happens, the chip will wait for the BG/ signal to complete the normal bus arbitration handshake. The chip no longer wants host bus access - it deasserts the BR/, MASTER/, and all control lines after one BCLK, and does not assert TS/, the signal that indicates a valid bus cycle is starting. The chip will next generate an interrupt which the system may service.

Bus Mode 2 Fast Arbitration

Fast Arbitration Sequence*

1) The 53C720 internally determines bus mastership is required. If appropriate, FETCH/ is asserted.

2) Bus Request is asserted.

3) The 53C720 waits for Bus Grant. The 53C710 becomes bus master asynchronously on the leading edge of BG/. Then the 53C720 asynchronously asserts Bus Busy and Master, and deasserts Bus Request.

4) The 53C720 issues a start cycle on the next rising edge of BCLK.

* *Fast Arbitration bit must be set.*

Note: *In fast arbitration mode, the 53C720 will take bus ownership on the assertion of BG/ regardless of the state of BR/ or BB/.*

Bus Mode 2 Fast Arbitration Timings

Parameter	Symbol	Min	Max	Units
BCLK high to BR/ asserted	t_1	-	20	ns
BG/ setup to BCLK high	t_2	12	-	ns
BG/ asserted to BR/ deasserted	t_3	-	22	ns
BG/ asserted to BB/ asserted	t_4	-	20	ns
BG/ asserted to MASTER/ asserted	t_5	-	16	ns
BG/ hold after BR/ deasserted	t_6	0	-	ns
BR/ asserted to BG/ asserted	t_7	0	-	ns

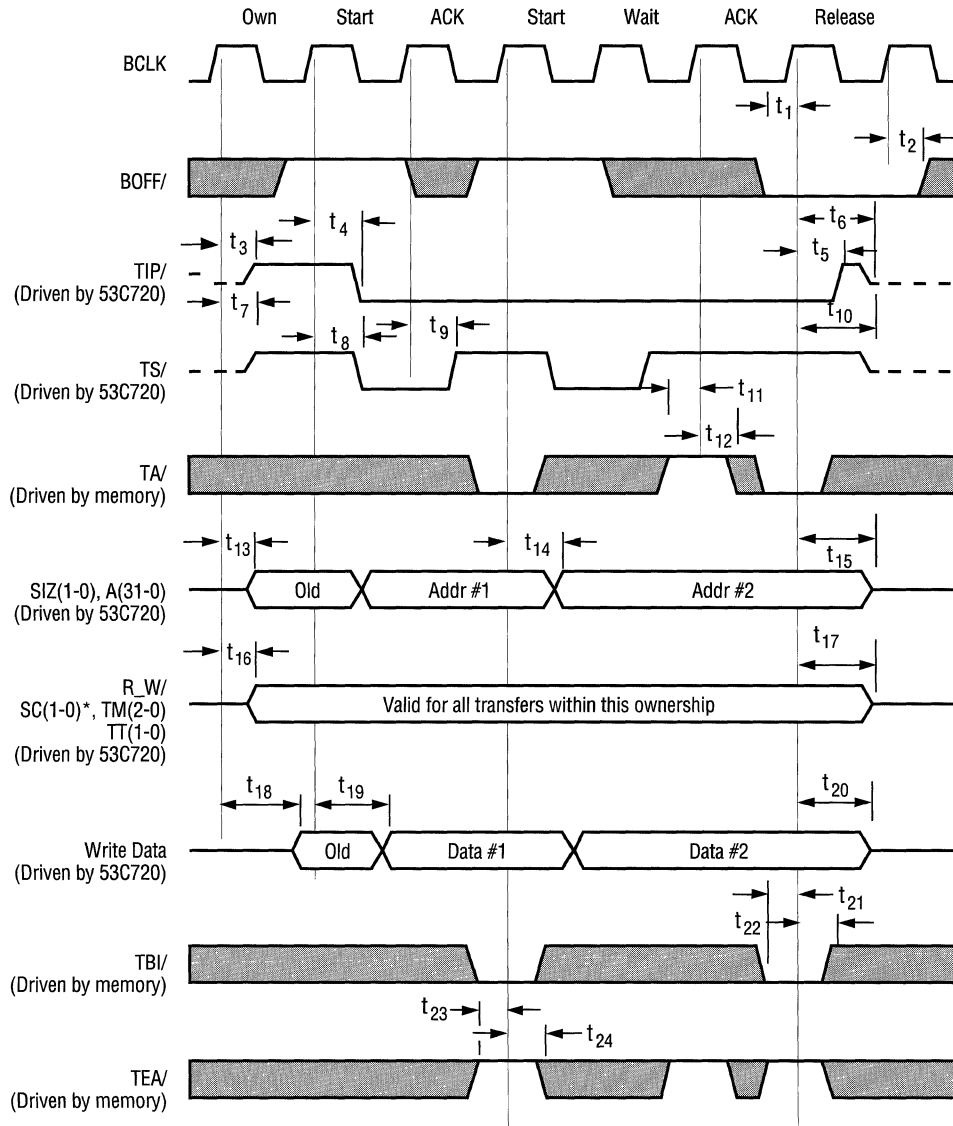Figure 6-20. Bus Mode 2 Fast Arbitration
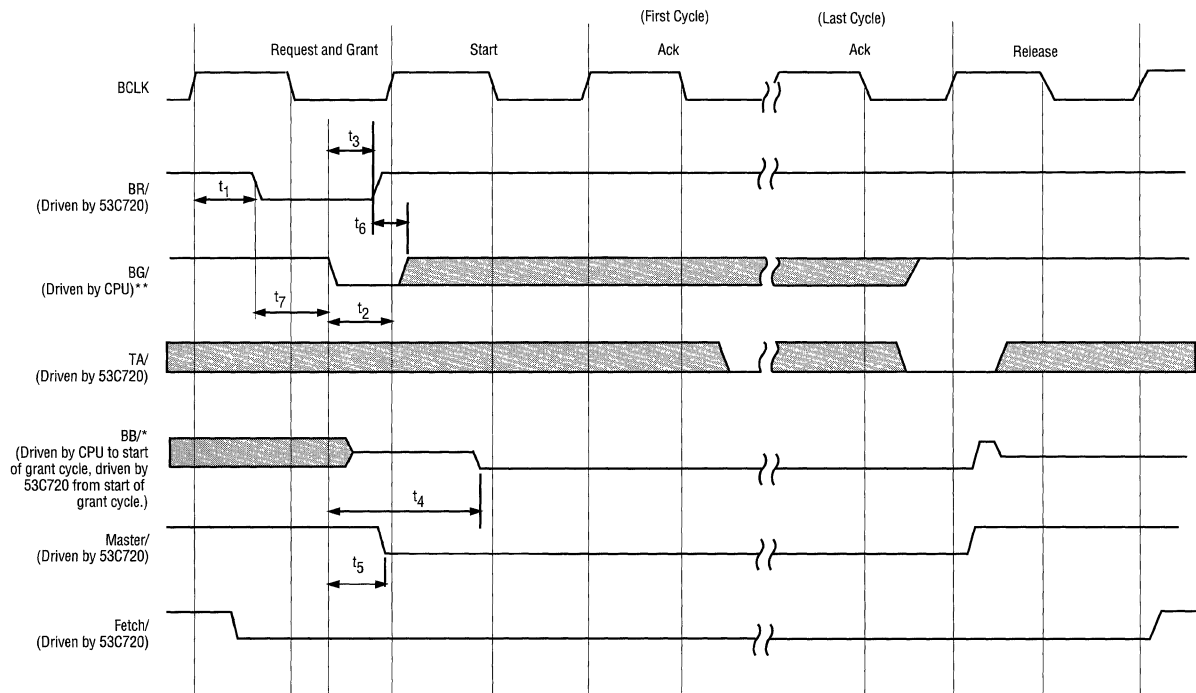
Bus Mode 2 Master Cycle

Bus Mode 2 Master Read Sequence

1) The 53C720 has attained bus mastership.

2) The 53C720 asserts the R_W/, Snoop Control, Transfer Modifier, and Transfer Type lines.

3a) The 53C720 asserts Transfer in Progress .

3b) The 53C720 asserts Transfer Start, Address, and Size lines.

4) The 53C720 deasserts Transfer Start.

5) The 53C720 waits for Transfer Acknowledge, Valid Data, Transfer Burst Inhibit, and Transfer Error Acknowledge.

- If Transfer Burst Inhibit is not asserted, attempt cache bursting.

- If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.

- If Transfer Error Acknowledge is asserted and Transfer Acknowledge is not asserted, a bus fault condition will be generated.

- If Transfer Acknowledge is asserted and Transfer Error Acknowledge is not asserted and the 53C720 requires more cycles, then return to step 3b.

6) Upon acknowledge of the last bus cycle, the 53C720 deasserts Master, Bus Busy, and Transfer in Progress.

7) The 53C720 floats the Control and Address lines.
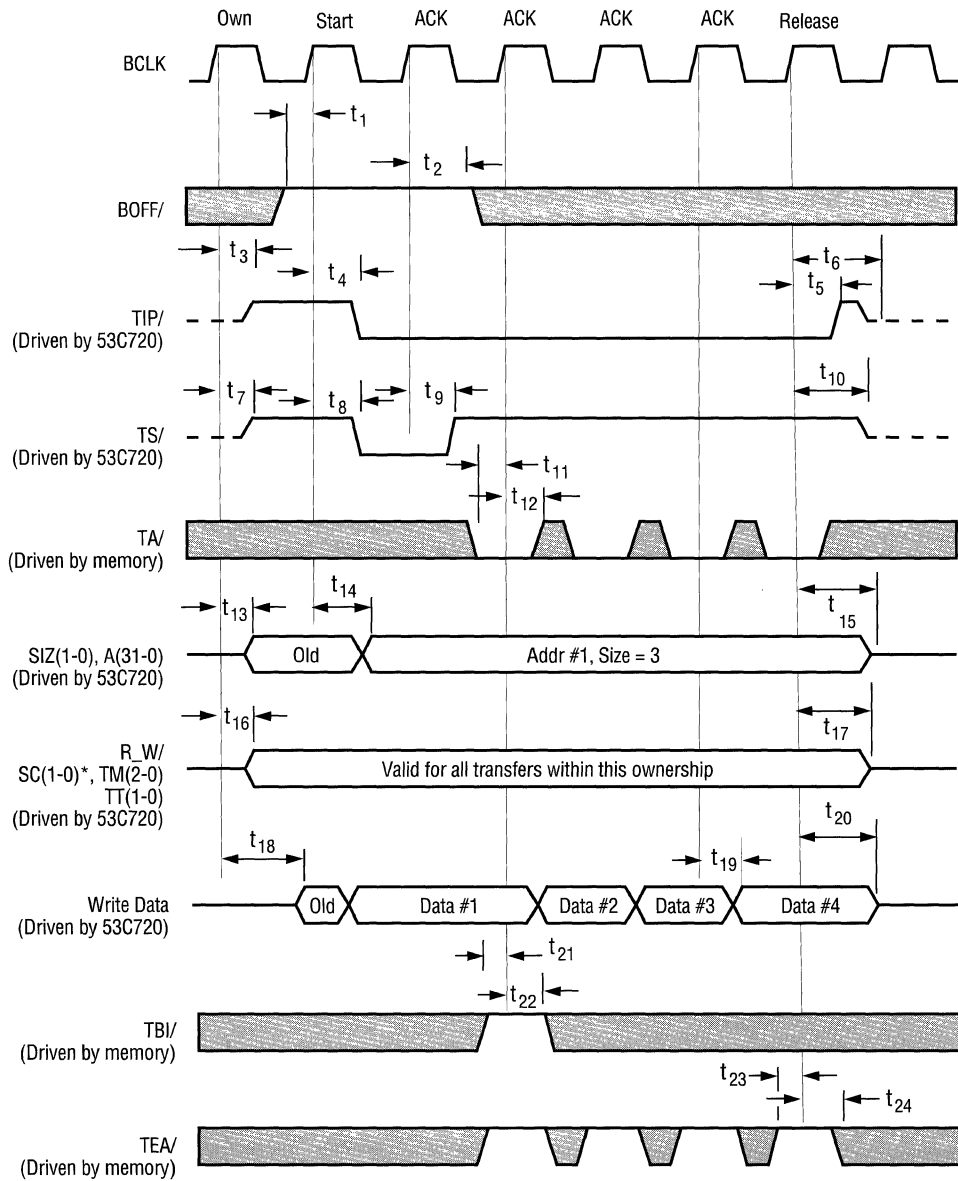
Bus Mode 2 Bus Master Read Timings

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to TIP/ driven	t_3	5	32	ns
BCLK high to TIP/ low	t_4	3	20	ns
BCLK high to TIP/ high	t_5	3	20	ns
BCLK high to TIP/ high-Z	t_6	7	32	ns
BCLK high to TS/ driven	t_7	5	30	ns
BCLK high to TS/ low	t_8	3	17	ns
BCLK high to TS/ high	t_9	4	17	ns
BCLK high to TS/ high-Z	t_{10}	7	32	ns
TA/ setup to BCLK high	t_{11}	9	-	ns
TA/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-0), SIZ(1-0) driven	t_{13}	5	28	ns
BCLK high to A(31-0), SIZ(1-0) valid	t_{14}	5	20	ns
BCLK high to A(31-0), SIZ(1-0) high-Z	t_{15}	7	32	ns
BCLK high to R_W/, SC(1-0), TM(2-0), TT(1-0) driven and valid	t_{16}	5	30	ns
BCLK high to R_W/, SC(1-0), TM(2-0), TT(1-0) high-Z	t_{17}	-	32	ns
Read Data setup to BCLK high	t_{18}	6	-	ns
Read Data hold from BCLK high	t_{19}	6	-	ns
Read Data setup to DLE low	t_{20}	4	-	ns
Read Data hold from DLE low	t_{21}	6	-	ns
TBI/ setup to BCLK high	t_{22}	6	-	ns
TBI/ hold from BCLK high	t_{23}	4	-	ns
TEA/ setup to BCLK high	t_{24}	9	-	ns
TEA/ hold from BCLK high	t_{25}	5	-	ns

Figure 6-21. Bus Mode 2 Bus Master Read (Non-Cache Line Burst)
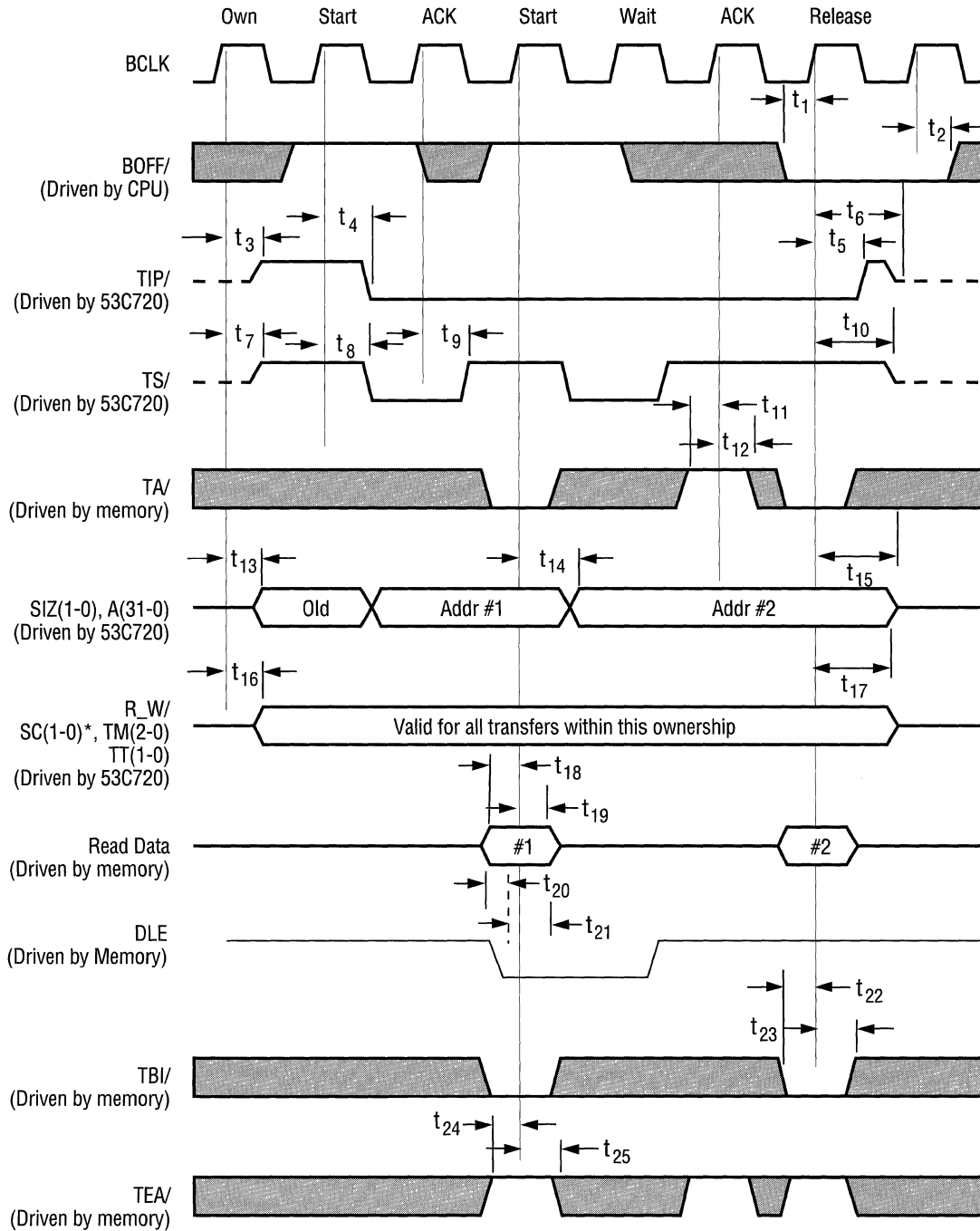
SC(1-0) timings apply only if Snoop Mode bit 0 of CTEST3 = 0.

Figure 6-22. Bus Mode 2 Bus Master Read (Cache Line Burst)
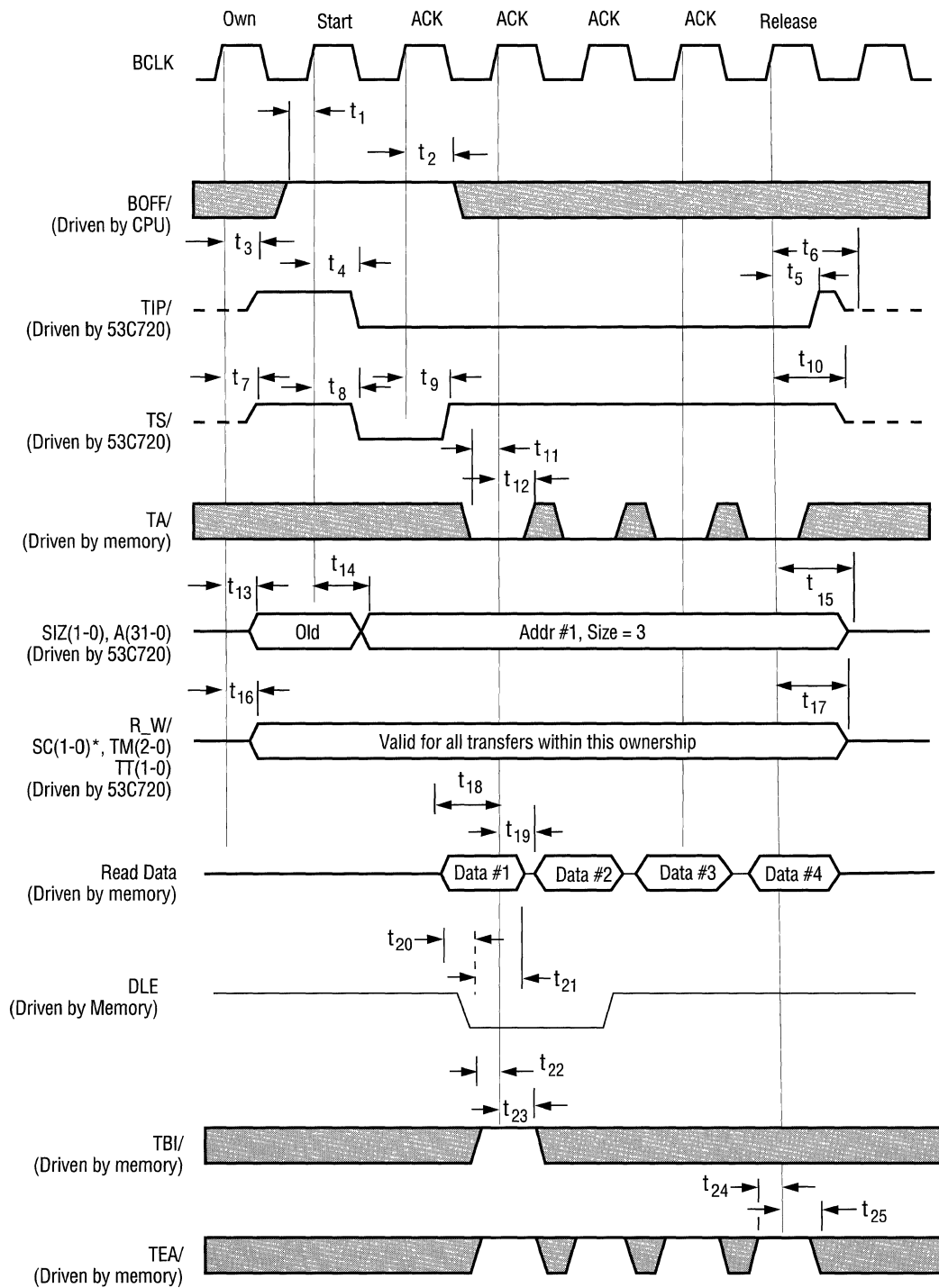
SC(1-0) timings apply only if Snoop Mode bit 0 of CTEST3 = 0.

Bus Mode 2 Bus Master Write Sequence

1) The 53C720 has attained bus mastership.

2) The 53C720 asserts the R_W/, Snoop Control, Transfer Modifier and Transfer Type lines.

3a) The 53C720 asserts Transfer in Progress.

3b) The 53C720 asserts Transfer Start, Address, Size lines and Data lines.

4) The 53C720 deasserts Transfer Start.

5) The 53C720 waits for Transfer Acknowledge, Transfer Burst Inhibit and Transfer Error Acknowledge.

   - If Transfer Burst Inhibit is not asserted, attempt cache bursting.

   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.

   - If Transfer Error Acknowledge is asserted and Transfer Acknowledge is not asserted, a bus fault condition will be generated.

   - If Transfer Acknowledge is asserted and Transfer Error Acknowledge is not asserted and the 53C720 requires more cycles, then return to step 3b.

6) Upon acknowledge of the last bus cycle, the 53C720 deasserts Master, Busy, and Transfer in Progress.

7) The 53C720 floats the Control, Address and Data lines.

Bus Mode 2 Bus Master Write Timings

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to TIP/ driven	t_3	5	32	ns
BCLK high to TIP/ low	t_4	3	20	ns
BCLK high to TIP/ high	t_5	3	20	ns
BCLK high to TIP/ high-Z	t_6	7	32	ns
BCLK high to TS/ driven	t_7	5	30	ns
BCLK high to TS/ low	t_8	3	17	ns
BCLK high to TS/ high	t_9	3	17	ns
BCLK high to TS/ high-Z	t_{10}	7	32	ns
TA/ setup to BCLK high	t_{11}	9	-	ns
TA/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-0), SIZ(1-0) driven	t_{13}	5	30	ns
BCLK high to A(31-0), SIZ(1-0) valid	t_{14}	3	20	ns
BCLK high to A(31-0), SIZ(1-0) high-Z	t_{15}	7	32	ns
BCLK high to R_W/, SC(1-0), TM(1-0), TT(1-0) driven and valid	t_{16}	5	30	ns
BCLK high to R_W/, SC(1-0), TM(2-0), TT(1-0) high-Z	t_{17}	5	32	ns
BCLK high to Write Data driven	t_{18}	5	34	ns
BCLK high to Write Data valid	t_{19}	7	24	ns
BCLK high to Write Data high-Z	t_{20}	5	30	ns
TBI/ setup to BCLK high	t_{21}	6	-	ns
TBI/ hold from BCLK high	t_{22}	4	-	ns
TEA/ setup to BCLK high	t_{23}	9	-	ns
TEA/ hold from BCLK high	t_{24}	5	-	ns

Figure 6-23. Bus Mode 2 Bus Master Write (Non-Cache Line Burst)

* *SC(1-0) timings apply only if Snoop Mode bit 0 of CTEST3 = 0.*

Figure 6-24. Bus Mode 2 Bus Master Write (Non-Cache Line Burst)

* *SC(1-0) timings apply only if Snoop Mode bit 0 of CTEST3 = 0.*

Bus Mode 2 Mux Mode Cycle

Mux Mode Read Sequence

1) The 53C720 has attained bus mastership.

2) The 53C720 asserts the Read/Write/, Snoop Control, Function Control and Transfer Type lines.

3a) The 53C720 asserts Transfer in Progress and Transfer Start.

3b) The 53C720 asserts the Transfer Start, Address, and Size lines.

4) The 53C720 deasserts Transfer Start and floats the Address lines.

5) The 53C720 waits for Transfer Acknowledge, Valid Data driven on the data pins, Transfer Burst Inhibit and Transfer Error Acknowledge.

  • If Transfer Burst Inhibit is not asserted, attempt cache bursting.

  • If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.

  • If Transfer Error Acknowledge is asserted and Transfer Acknowledge is not asserted, a bus fault condition will be generated.

  • If Transfer Acknowledge is asserted and Transfer Error Acknowledge is not asserted and the 53C720 requires more cycles, then return to step 3b.

6) The 53C720 deasserts the Control lines.

7) Upon acknowledgment of the last bus cycle, the 53C720 deasserts Master and Bus Grant Acknowledge.

Note: This mode of operation expects D(31-0) to be physically tied to A(31-0) respectively.

Bus Mode 2 Mux Mode Read Timings

Parameter	Symbol	Min	Max	Units
BCLK high to Address driven	t_1	5	22	ns
BCLK high to Address hi-z	t_2	-	23	ns
Read Data setup to BCLK high	t_3	5	-	ns
Read Data hold from BCLK high	t_4	6	-	ns

Figure 6-25. Mux Mode Read Cycle (Non-Cache Line Burst)
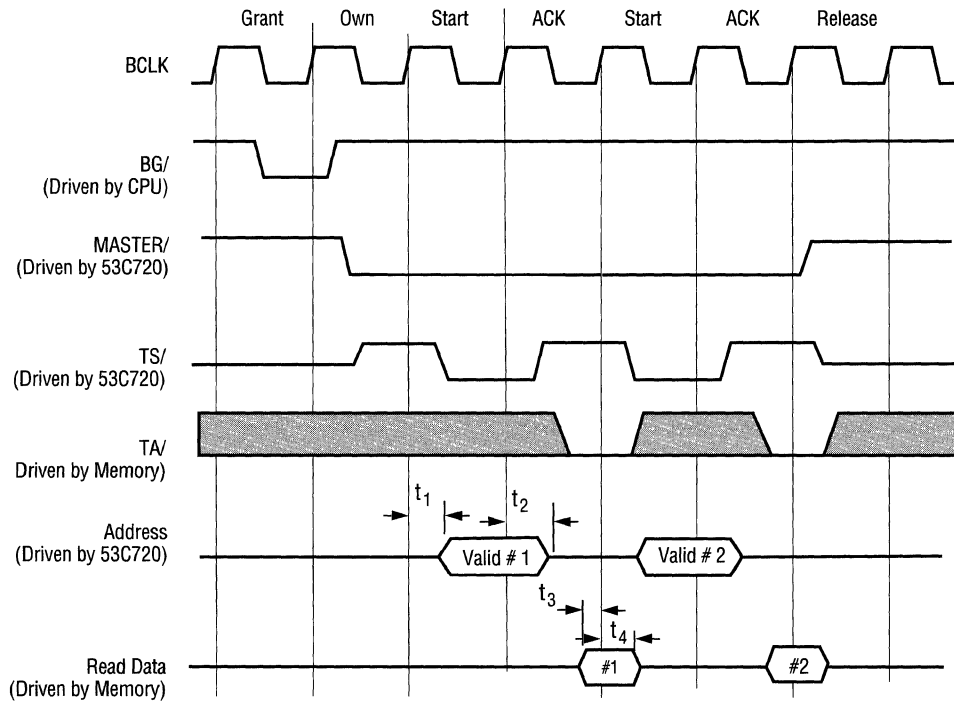
Figure 6-26. Mux Mode Read Cycle (Cache Line Burst)
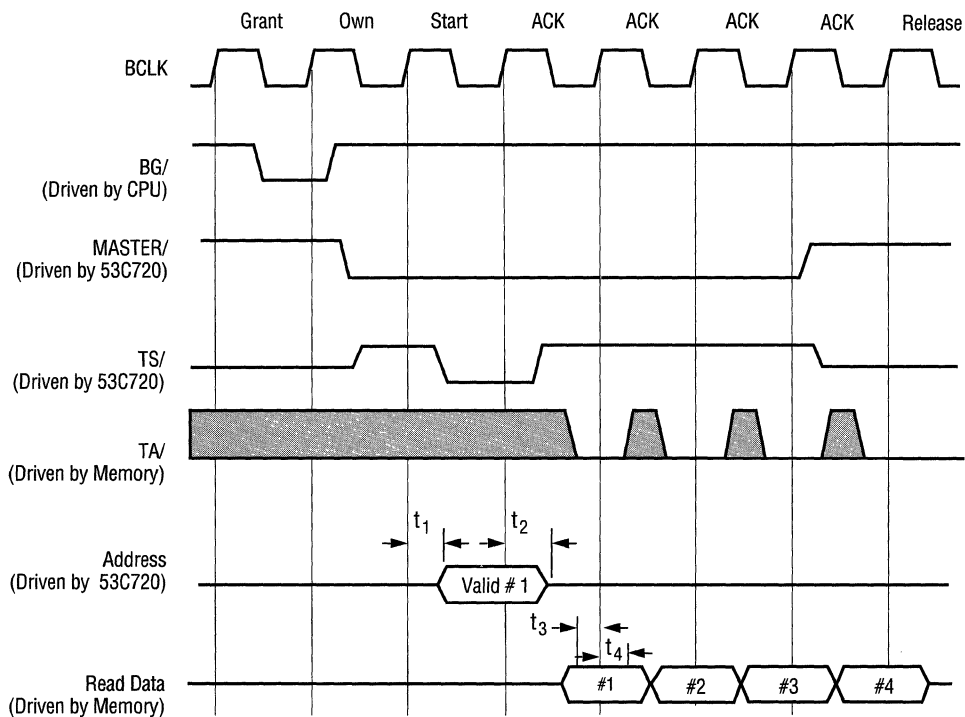
Mux Mode Write Sequence

1) The 53C720 has attained bus mastership.

2) The 53C720 asserts the Read/Write, Snoop Control, Function Control and Transfer Type lines.

3a) The 53C720 asserts Transfer in Progress and Transfer Start.

3b) The 53C720 asserts Transfer Start, Address, Size lines, and floats the Data lines.

4) The 53C720 deasserts Transfer Start, floats the address bus, and asserts the data bus.

5) The 53C720 waits for Transfer Acknowledge, Transfer Burst Inhibit and Transfer Error Acknowledge.

   • If Transfer Burst Inhibit is not asserted, attempt cache bursting.

   • If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.

   • If Transfer Error Acknowledge is asserted and Transfer Acknowledge is not asserted, a bus fault condition will be generated.

   • If Transfer Acknowledge is asserted, Transfer Error Acknowledge is not asserted, and the 53C720 requires more cycles, return to step 3b.

6) The 53C720 deasserts the Control and Data lines.

7) Upon acknowledge of the last bus cycle, the 53C720 deasserts Master and Bus Grant Acknowledge.

Note: This mode of operation expects D(31-0) to be physically tied to A(31-0) respectively.

Bus Mode 2 Mux Mode Write Timings

Parameter	Symbol	Min	Max	Units
BCLK high to Old Data driven	t_1	–	34	ns
BCLK high to Address driven	t_2	5	22	ns
BCLK high to new Data driven	t_3	8	24	ns
Hi-z to Driven switching time	t_4	1	–	ns
BCLK high to Next Data	t_5	–	24	ns

Figure 6-27. Mux Mode Write Cycle (Non-Cache Line Burst)
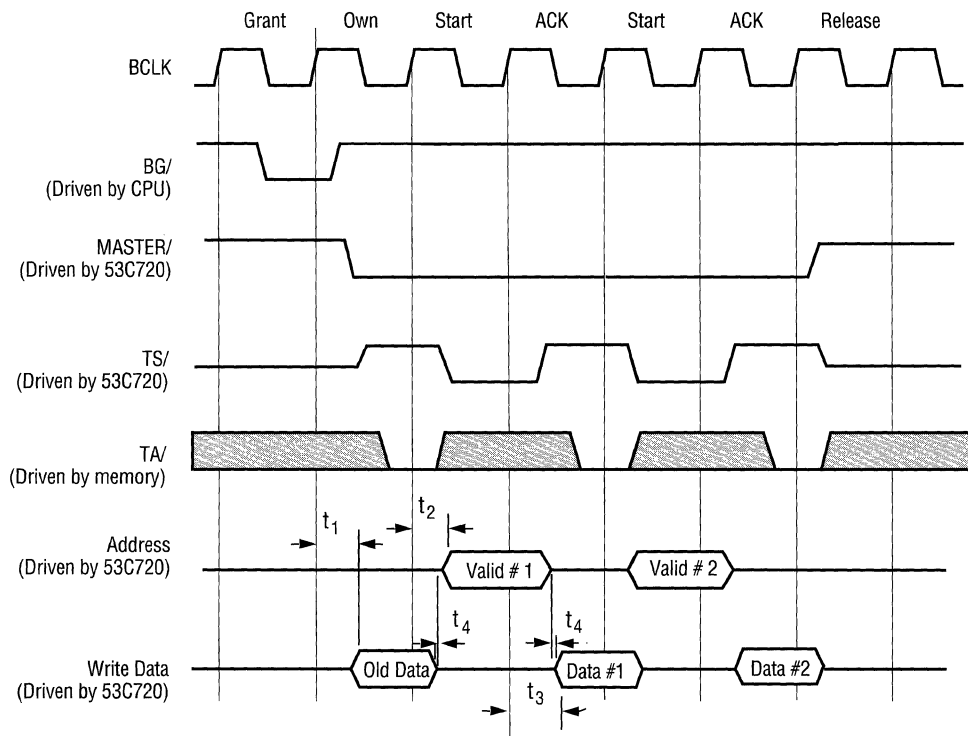
Figure 6-28. Mux Mode Write Cycle (Cache Line Burst)
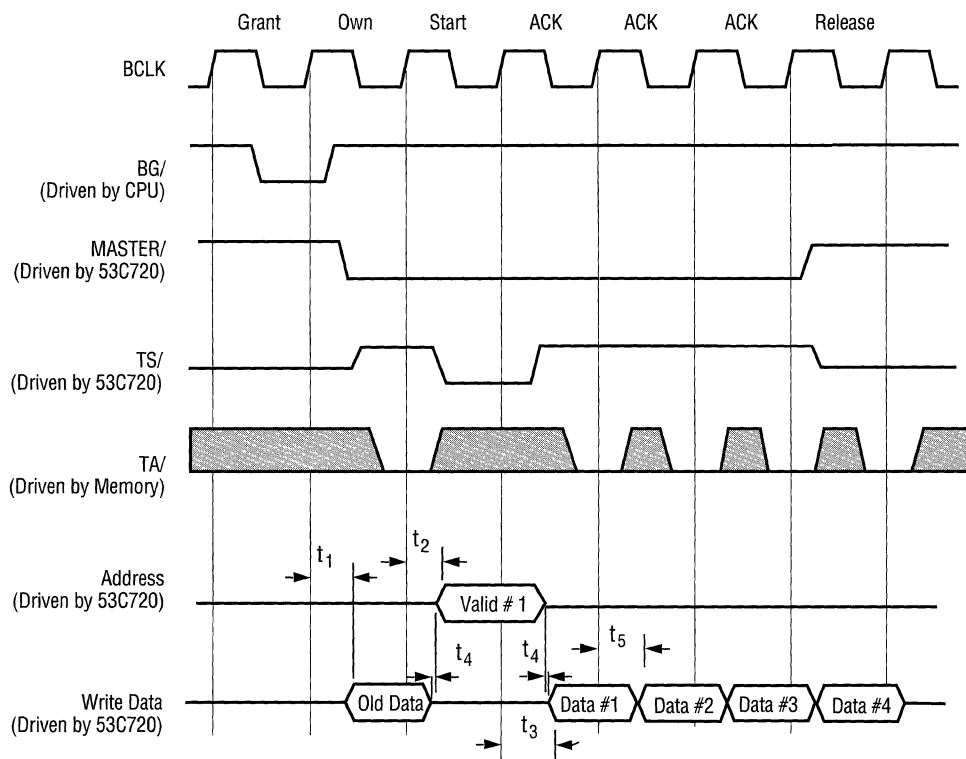
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Bus Mode 3 and 4 Slave Cycle

Bus Mode 3 and 4 Slave Read Sequence

1) Address, Address Status and the Byte Enable signals are asserted by the CPU.

2) Chip Select is validated by the 53C720 on any following rising edge of BCLK.

3) Transfer Burst Inhibit is asserted.

4) Address Status may be deasserted by the CPU.

5) Three clock cycles of wait state are inserted (these wait states are required) and the Data lines are asserted.

6) Ready Out is asserted by the 53C720, if no errors are detected.

7) If a bus error is detected, only Transfer Error Acknowledge is asserted and the bus cycle ends on the next rising edge of BCLK.

8) Ready Out or Transfer Error Acknowledge is deasserted.

9) The 53C720 waits for Ready In to be asserted and then ends the slave cycle, if no errors are detected.

10) The Data lines are tristated by the 53C720.

Recommended Setup for Bus Mode 3 and 4

1) Disable Cache Line Mode (if cache line is not supported; set CTEST0, bit 7).

2) Set the Bus Mode Bit (DCNTL, bit 6).

3) Set the Snoop Mode bit (CTEST3, bit 0)

4) Tie BB/ high resistively.

5) Tie TBI/ low resistively.

6) Tie TEA/ high resistively.

Bus Mode 3 and 4 Slave Read Timings

Parameter	Symbol	Min	Max	Units
ADS/ setup to BCLK high	t_1	4	–	ns
ADS/ hold from BCLK high	t_2	4	–	ns
CS/ setup to BCLK high after ADS/	t_3	5	–	ns
CS/ hold from BCLK high after ADS/	t_4	5	–	ns
BCLK high to TBI/ low	t_5	5	30	ns
BCLK high to TBI/ high	t_6	4	22	ns
BCLK high to READYO/, TEA/ low	t_7	5	20	ns
BCLK high to READYO/, TEA/ high	t_8	4	20	ns
READYI/ setup to BCLK high during or after READYO/, TEA/	t_9	9	–	ns
READYI/ hold from BCLK high during or after READYO/, TEA/	t_{10}	5	–	ns
BCLK high to data bus driven	t_{11}	8	28	ns
BCLK high to read data valid	t_{12}	–	75	ns
BCLK high to data bus high-Z	t_{13}	7	34	ns
A(6-0), SIZ(1-0), W_R/ setup to BCLK high	t_{14}	4	–	ns
A(6-0), SIZ(1-0), W_R/ hold from BCLK high	t_{15}	12	–	ns

Figure 6-29. Bus Mode 3 and 4 Slave Read Cycle
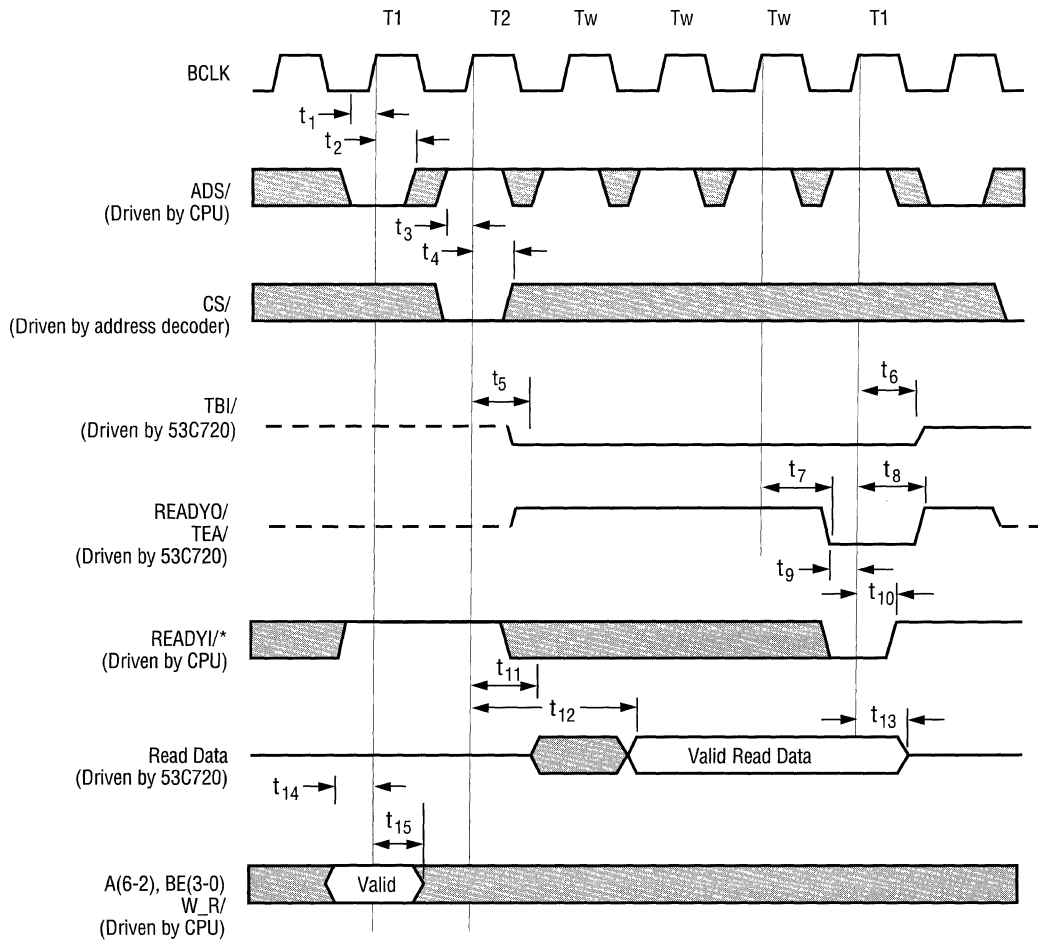
*   *This signal may be driven by the 53C720 if the Enable Ack bit is set (DCNTL bit 5). See the explanation in chapter 2 of the 53C720 Data Manual for use of this signal as an output.*

Bus Mode 3 and 4 Slave Write Sequence

1) W_R/, the address lines, and the Address Status and Byte Enable signals are asserted by the CPU.

2) Chip Select is validated by the 53C720 on any following rising edge of BCLK.

3) Transfer Burst Inhibit is asserted.

4) Address Status may be deasserted by the CPU.

5) The data lines are asserted by the CPU.

6) Three clock cycles of wait state are inserted (These wait states are required).

7) Ready Out is asserted by the 53C720, if no errors are detected

8) If a bus error is detected, only Transfer Error Acknowledge is asserted and the bus cycle ends on the next rising edge of BCLK.

9) Ready Out or Transfer Error Acknowledge is deasserted.

10) The 53C720 waits for Ready In to be asserted and then ends the slave cycle, if no error.

Bus Mode 3 and 4 Slave Write Timings

Parameter	Symbol	Min	Max	Units
ADS/ setup to BCLK high	t_1	4	-	ns
ADS/ hold from BCLK high	t_2	4	-	ns
CS/ setup to BCLK high after ADS/	t_3	5	-	ns
CS/ hold from BCLK high after ADS/	t_4	5	-	ns
BCLK high to TBI/ low	t_5	5	30	ns
BCLK high to TBI/ high	t_6	4	22	ns
BCLK high to READYO/, TEA/ low	t_7	5	20	ns
BCLK high to READYO/, TEA/ high	t_8	4	20	ns
READYI/ setup to BCLK high during or after READYO/, TEA/	t_9	9	-	ns
READYI/ hold from BCLK high during or after READYO/, TEA/	t_{10}	5	-	ns
Valid write data setup to BCLK high	t_{11}	6	-	ns
Valid write data hold from BCLK high	t_{12}	14	-	ns
A(6-0), SIZ(1-0), W_R/ setup to BCLK high	t_{13}	4	-	ns
A(6-0), SIZ(1-0), W_R/ hold from BCLK high	t_{14}	12	-	ns

Figure 6-30. Bus Mode 3 and 4 Slave Write Cycle
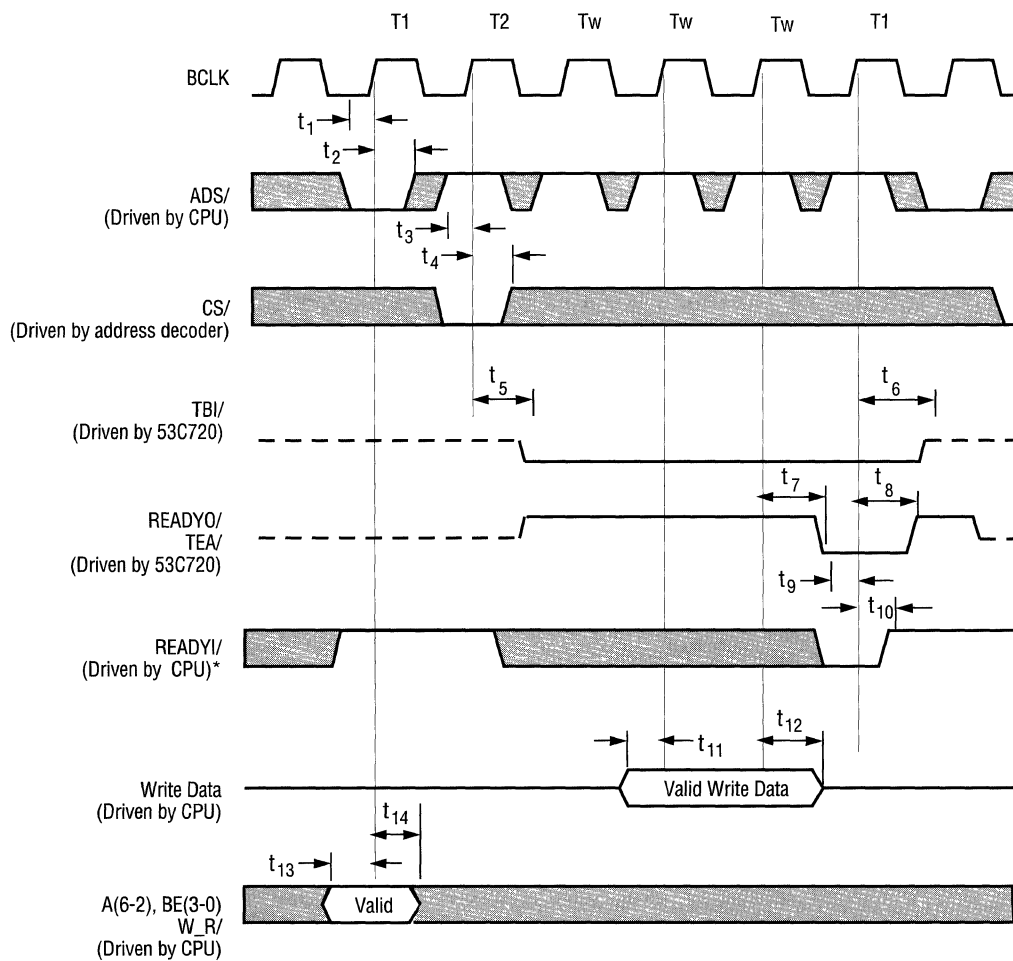
This signal may be driven by the 53C720 if the Enable Acknowledge bit is set (DCNTL Bit 5). See explanation in Chapter 2 of the 53C720 Data Manual for use of this signal as an output.

Bus Mode 3 and 4 Host Bus Arbitration

Bus Arbitration Sequence

1) The 53C720 internally determines bus mastership is required. If appropriate, FETCH/ is asserted.

2) HOLD/ is asserted.

3) The 53C720 waits for Hold Acknowledge and checks that Bus Busy is deasserted. Then the 53C720 asserts Hold Acknowledge and Master, and deasserts HOLD/.

Bus Mode 3 and 4 Host Bus Arbitration Timings

Parameter	Symbol	Min	Max	Units
SC0 high to HOLD/ low*	t_1	1	2	BCLK
BCLK high to SC0 low on last cycle*	t_2	5	28	ns
BCLK high to HOLD/ low	t_3	4	20	ns
BCLK high to HOLD/ high	t_4	5	25	ns
HLDAI/ setup to BCLK high (any rising edge after BR/)	t_5	4	-	ns
HLDAI/ hold from BCLK high (any rising edge after BR/)	t_6	5	-	ns
BB/ setup to BCLK high (any rising edge after BR/)	t_7	4	-	ns
BCLK high to BB/ low	t_8	4	24	ns
BCLK high to BB/ high	t_9	3	19	ns
BCLK high to BB/ high-Z	t_{10}	7	32	ns
BCLK high to MASTER/ low	t_{11}	5	22	ns
BCLK high to MASTER/ high	t_{12}	6	26	ns
BCLK high to FETCH/ low	t_{13}	5	36	ns
BCLK high to FETCH/ high	t_{14}	5	36	ns
FETCH/ low to HOLD/ low	t_{15}	1	2	BCLK
BB/ high to FETCH/ high**	t_{16}	1	2	BCLK

When Snoop Mode bit 0 of CTEST 3 is set to 1.

**During a retry operation, FETCH/ will remain low until a successful completion of the op code fetch or a fatal bus error.*

Figure 6-31. Host Bus Arbitration, Bus Mode 3 and 4
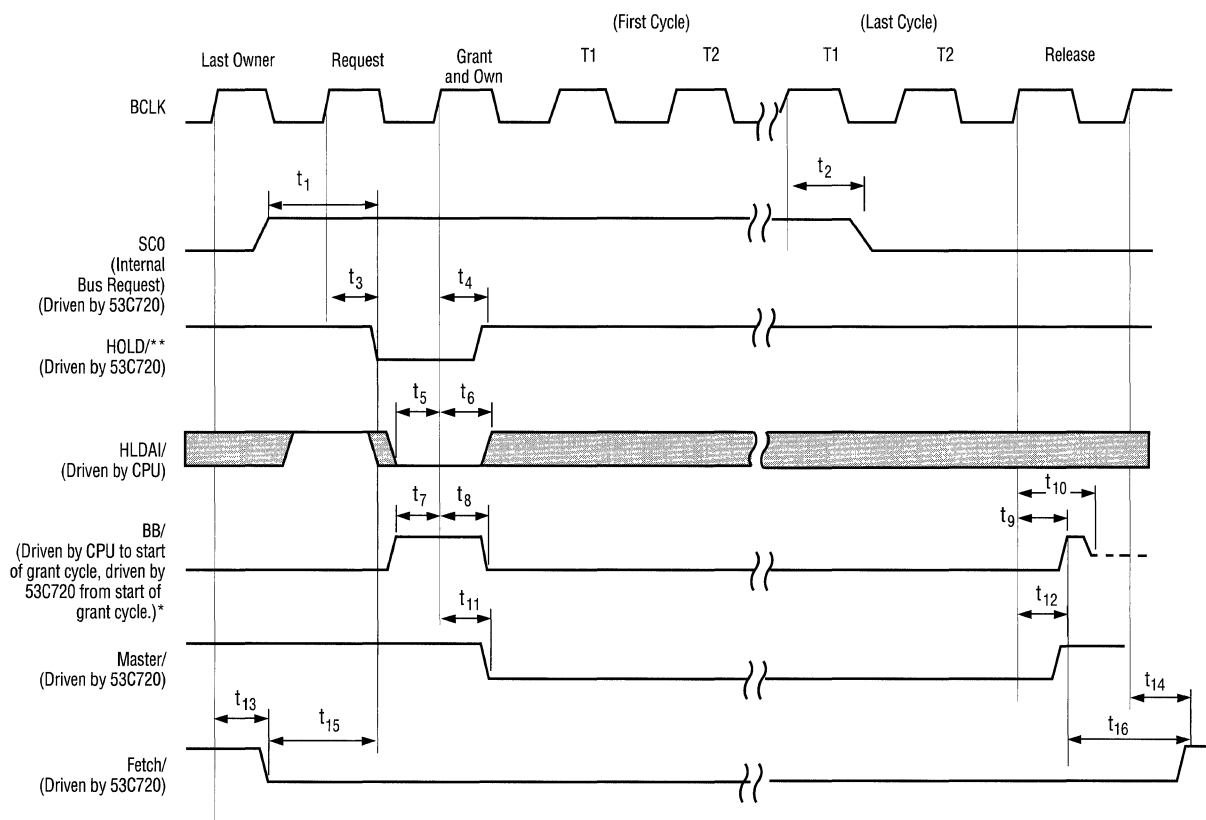
* *BB/ should be tied high resistively if not used*

** *HOLD/ may be NANDed with MASTER/ to obtain HOLD required by the 80286 or 80386 processors.*

Note: *the 53C720 will periodically assert the HOLD/ signal and receive a SCSI interrupt at the same time. When this happens, the chip will wait for the HLDAI/ signal to complete the normal bus arbitration handshake. The chip no longer wants host bus access - it deasserts the HOLD/, MASTER/, and all control lines after one BCLK, and does not assert ADS/, the signal that indicates a valid bus cycle is starting. The chip will next generate an interrupt, which the system may then service.*

Bus Mode 3 and 4 Fast Arbitration

1) The 53C720 internally determines bus mastership is required. If appropriate, FETCH/ is asserted.

2) HOLD/ is asserted.

3) The 53C720 waits for Hold Acknowledge (HLDAI/). The 53C720 becomes bus master asynchronously on the leading edge of HLDAI/. Then the 53C720 asynchronously asserts Bus Busy and Master, and deasserts HOLD/.

4) The 53C720 issues a start cycle on the next rising edge of BCLK.

Note: *In fast arbitration mode, the 53C720 will take bus ownership on the assertion of HLDAI/ regardless of the state of HOLD/ or BB/.*

Bus Mode 3 and 4 Fast Arbitration Timings

Parameter	Symbol	Min	Max	Units
BCLK high to HOLD/ asserted	t_1	-	20	ns
HLDAI/ setup to BCLK high	t_2	12	-	ns
HLDAI/ asserted to HOLD/ deasserted	t_3	-	22	ns
HLDAI/ asserted to BB/ asserted	t_4	-	20	ns
HLDAI/ asserted to MASTER/ asserted	t_5	-	16	ns
HLDAI/ hold after HOLD/ deasserted*	t_6	0	-	ns
HOLD/ asserted to HLDAI/ asserted	t_7	0	-	ns

* *BG/ may not be asserted prior to BR/.*

Figure 6-32. Bus Mode 3 and 4 Fast Arbitration
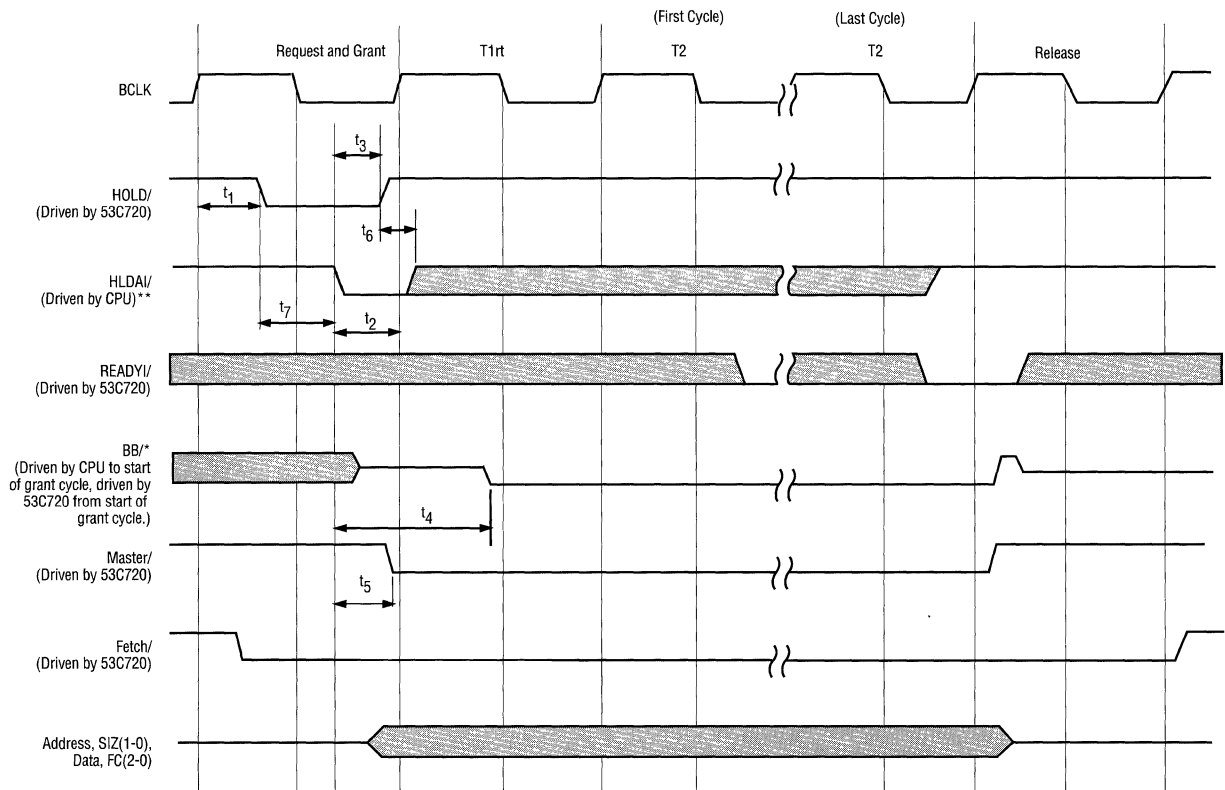
Bus Mode 3 and 4 Master Cycle

Bus Mode 3 and 4 Bus Master Read Sequence

1) The 53C720 has attained bus mastership.

2) The 53C720 asserts the W_R/, Transfer Modifier and Transfer Type lines.

3a) The 53C720 asserts Transfer in Progress.

3b) The 53C720 asserts Address Status, Address, and Byte Enable signals.

4) The 53C720 deasserts Address Status.

5) The 53C720 waits for Transfer Acknowledge, Valid Data, Transfer Burst Inhibit and Transfer Error Acknowledge.

   • If Transfer Burst Inhibit is not asserted, attempt cache bursting.

   • If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.

   • If Transfer Error Acknowledge is asserted and Ready In is not asserted, a bus fault condition will be generated.

   • If Ready In is asserted and Transfer Error Acknowledge is not asserted and the 53C720 requires more cycles, then return to step 3b.

6) Upon acknowledge of the last bus cycle, the 53C720 deasserts Master, Bus Busy, and Transfer in Progress.

7) The 53C720 floats the Control and Address lines.

Bus Mode 3 and 4 Bus Master Read Timings

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to TIP/ driven	t_3	5	32	ns
BCLK high to TIP/ low	t_4	3	20	ns
BCLK high to TIP/ high	t_5	3	20	ns
BCLK high to TIP/ high-Z	t_6	7	32	ns
BCLK high to ADS/ driven	t_7	5	30	ns
BCLK high to ADS/ low	t_8	3	17	ns
BCLK high to ADS/ high	t_9	3	17	ns
BCLK high to ADS/ high-Z	t_{10}	7	32	ns
READYI/ setup to BCLK high	t_{11}	9	-	ns
READYI/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-2), SIZ(1-0) driven	t_{13}	5	28	ns
BCLK high to A(31-2), SIZ(1-0) valid	t_{14}	3	20	ns
BCLK high to A(31-2), SIZ(1-0) high-Z	t_{15}	7	32	ns
BCLK high to W_R/, TM(2-0), TT(1-0) driven and valid	t_{16}	5	30	ns
BCLK high to W_R/, TM(2-0), TT(1-0) high-Z	t_{17}	-	32	ns
Read Data setup to BCLK high	t_{18}	6	-	ns
Read Data hold from BCLK high	t_{19}	6	-	ns
PA/ setup to BCLK high	t_{20}	5	-	ns
PA/ hold from BCLK high	t_{21}	5	-	ns
TBI/ setup to BCLK high	t_{22}	6	-	ns
TBI/ hold from BCLK high	t_{23}	4	-	ns
TEA/ setup to BCLK high	t_{24}	9	-	ns
TEA/ hold from BCLK high	t_{25}	5	-	ns

Figure 6-33. Bus Mode 3 and 4 Bus Master Read (Non-Preview of Address)
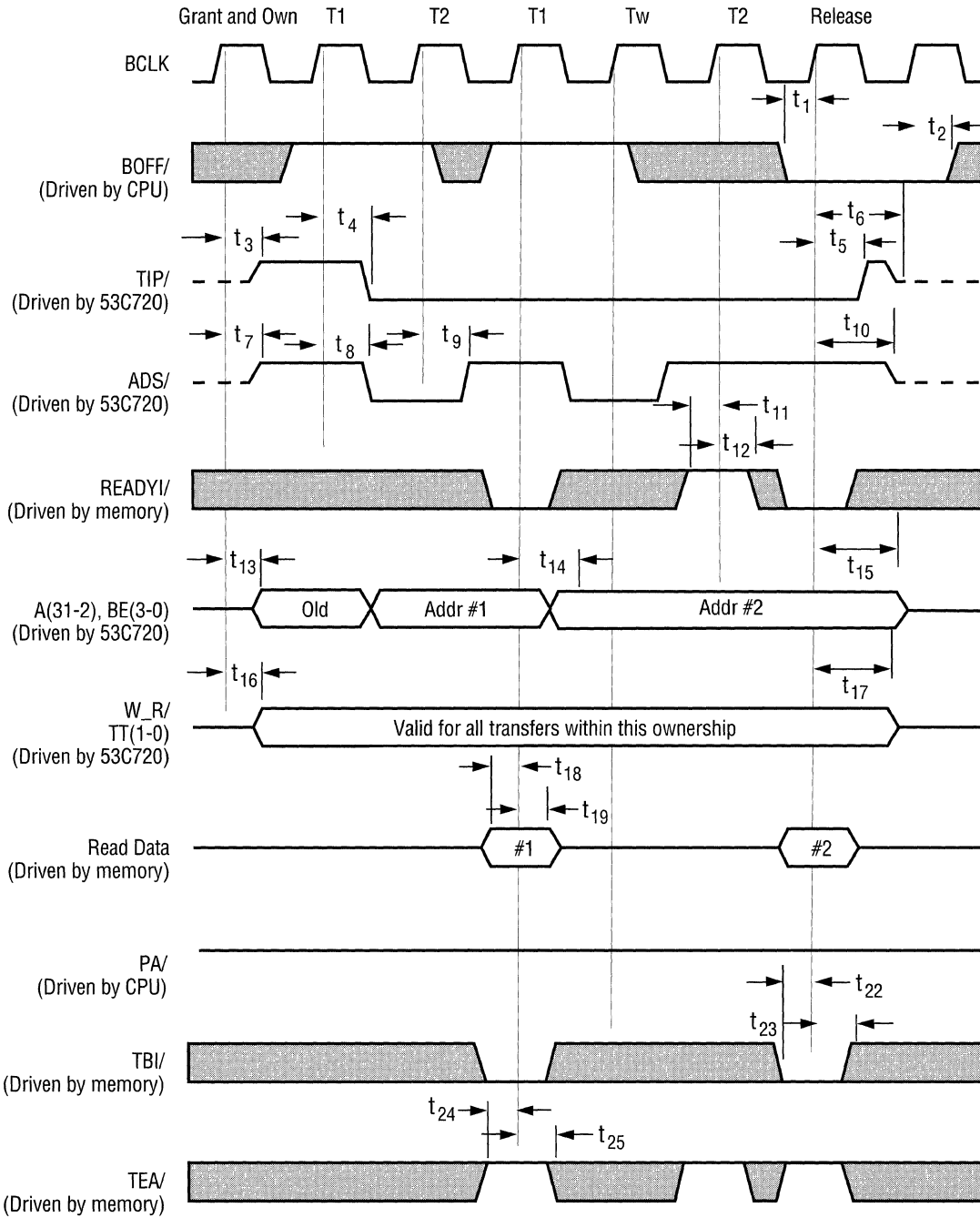
Note: this diagram shows two back-to-back cycles for a burst size of two.

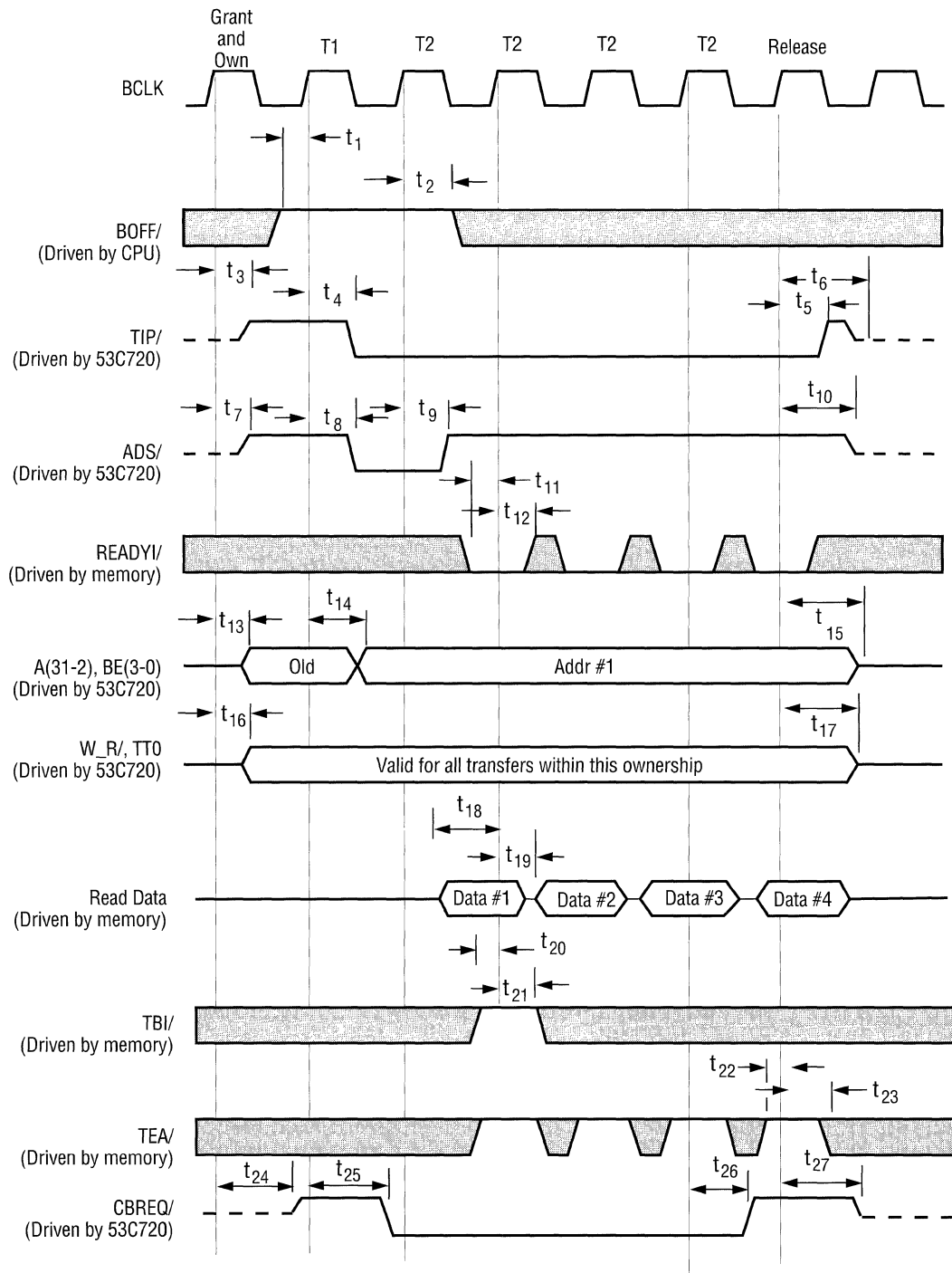Figure 6-34. Bus Mode 3 and 4 Bus Master Read (Preview of Address)
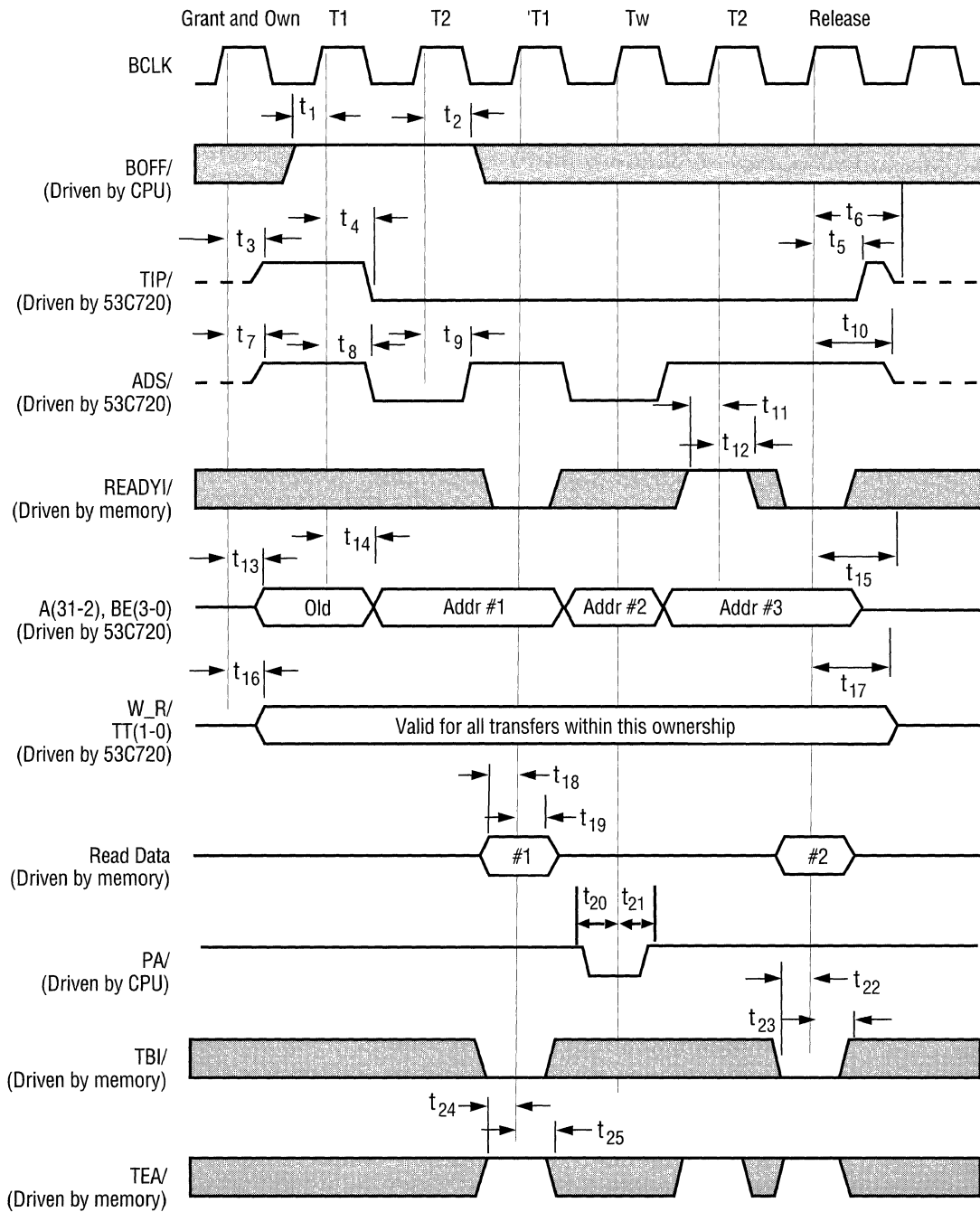
Note: this diagram shows two back-to-back cycles for a burst size of two.

Bus Mode 4 Bus Master Read Timings (Cache Line Burst)

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to TIP/ driven	t_3	5	32	ns
BCLK high to TIP/ low	t_4	3	20	ns
BCLK high to TIP/ high	t_5	3	20	ns
BCLK high to TIP/ high-Z	t_6	7	32	ns
BCLK high to ADS/ driven	t_7	5	30	ns
BCLK high to ADS/ low	t_8	3	17	ns
BCLK high to ADS/ high	t_9	3	17	ns
BCLK high to ADS/ high-Z	t_{10}	7	32	ns
READYI/ setup to BCLK high	t_{11}	9	-	ns
READYI/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-2), SIZ(1-0) driven	t_{13}	5	28	ns
BCLK high to A(31-2), SIZ(1-0) valid	t_{14}	3	20	ns
BCLK high to A(31-2), SIZ(1-0) high-Z	t_{15}	7	32	ns
BCLK high to W_R/, TM(2-0), TT(1-0) driven and valid	t_{16}	5	30	ns
BCLK high to W_R/, TM(2-0), TT(1-0) high-Z	t_{17}	5	32	ns
Read Data setup to BCLK high	t_{18}	6	-	ns
Read Data hold from BCLK high	t_{19}	6	-	ns
TBI/ setup to BCLK high	t_{20}	6	-	ns
TBI/ hold from BCLK high	t_{21}	4	-	ns
TEA/ setup to BCLK high	t_{22}	9	-	ns
TEA/ hold from BCLK high	t_{23}	5	-	ns
BCLK high to CBREQ/ driven	t_{24}	5	28	ns
BCLK high to CBREQ/ low	t_{25}	5	20	ns
BCLK high to CBREQ/ high	t_{26}	5	20	ns
BCLK high to CBREQ/ high-z	t_{27}	7	32	ns

Figure 6-35. Bus Mode 4 Bus Master Read (Cache Line Burst)

Note: this diagram shows two back-to-back cycles for a burst size of two.

Bus Mode 3 and 4 Bus Master Write Sequence

1) The 53C720 has attained bus mastership.

2) The 53C720 asserts the W_R/, Transfer Modifier and Transfer Type lines.

3a) The 53C720 asserts Transfer in Progress.

3b) The 53C720 asserts Address Status, Address, Byte Enable signals and Data lines.

4) The 53C720 deasserts Address Status.

5) The 53C720 waits for Ready In, Transfer Burst Inhibit and Transfer Error Acknowledge.

   • If Transfer Burst Inhibit is not asserted, attempt cache bursting.

   • If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.

   • If Transfer Error Acknowledge is asserted and Ready In is not asserted, a bus fault condition will be generated.

   • If Ready In is asserted and Transfer Error Acknowledge is not asserted and the 53C720 requires more cycles, then return to step 3b.

6) Upon acknowledge of the last bus cycle, the 53C720 deasserts Master, Busy, and Transfer in Progress.

7) The 53C720 floats the Control, Address and Data lines.

Bus Mode 3 and 4 Bus Master Write Timings

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to TIP/ driven	t_3	5	32	ns
BCLK high to TIP/ low	t_4	3	20	ns
BCLK high to TIP/ high	t_5	3	20	ns
BCLK high to TIP/ high-Z	t_6	7	32	ns
BCLK high to ADS/ driven	t_7	5	30	ns
BCLK high to ADS/ low	t_8	3	17	ns
BCLK high to ADS/ high	t_9	4	17	ns
BCLK high to ADS/ high-Z	t_{10}	7	32	ns
READYI/ setup to BCLK high	t_{11}	9	-	ns
READYI/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-2), SIZ(1-0) driven	t_{13}	5	28	ns
BCLK high to A(31-2), SIZ(1-0) valid	t_{14}	3	20	ns
BCLK high to A(31-2), SIZ(1-0) high-Z	t_{15}	7	32	ns
BCLK high to W_R/, TM(1-0), TT(1-0) driven and valid	t_{16}	5	30	ns
BCLK high to W_R/, TM(2-0), TT(1-0) high-Z	t_{17}	5	32	ns
BCLK high to Write Data driven	t_{18}	5	34	ns
BCLK high to Write Data valid	t_{19}	5	24	ns
BCLK high to Write Data high-Z	t_{20}	5	30	ns
PA/ setup to BCLK high	t_{21}	5	-	ns
PA/ hold from BCLK high	t_{22}	5	-	ns
TBI/ setup to BCLK high	t_{23}	6	-	ns
TBI/ hold from BCLK high	t_{24}	4	-	ns
TEA/ setup to BCLK high	t_{25}	9	-	ns
TEA/ hold from BCLK high	t_{26}	5	-	ns

Figure 6-36. Bus Mode 3 and 4 Bus Master Write (Non-Preview of Address)
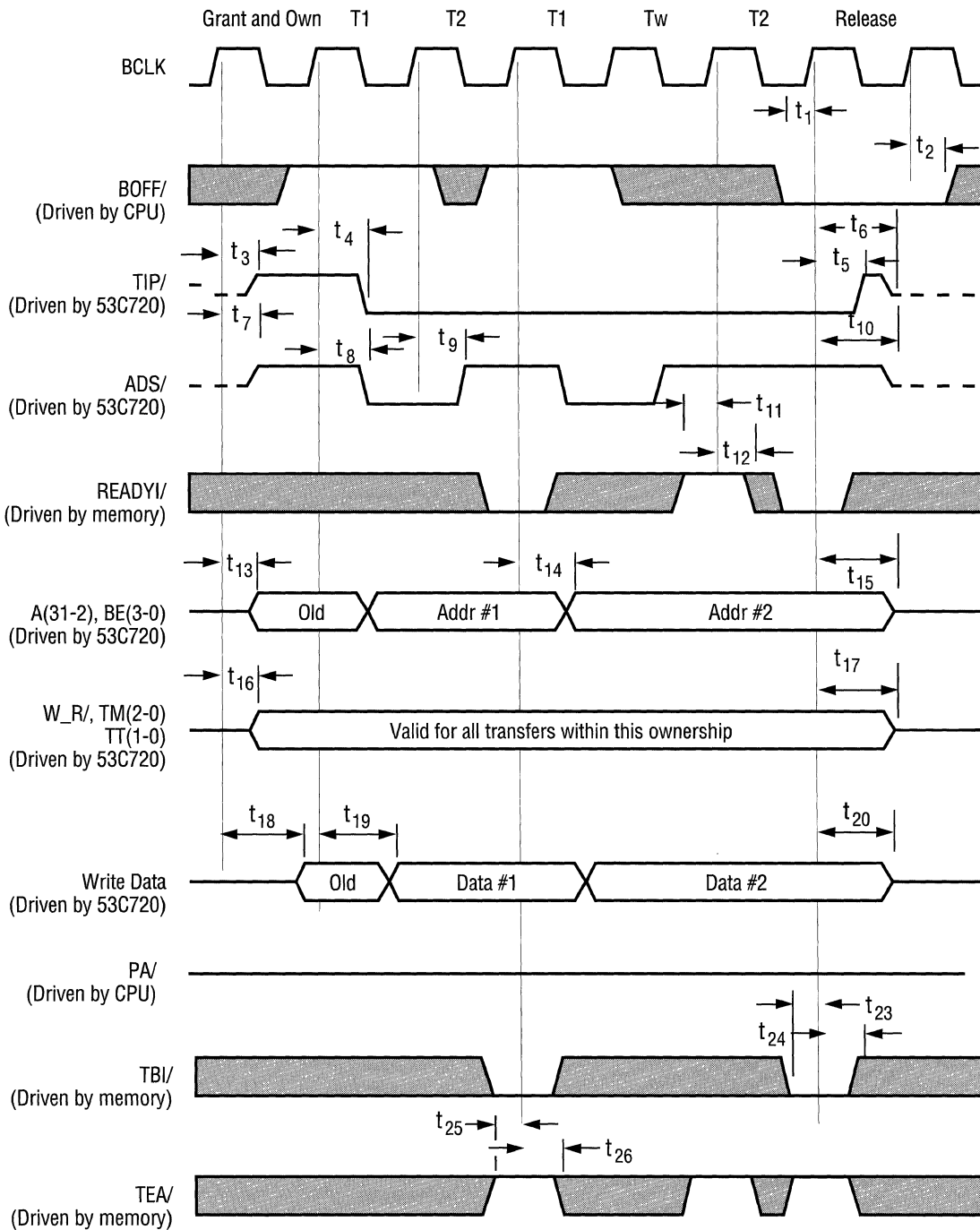
Note: *This diagram shows two back-to-back transfers for a burst size of two.*

Figure 6-37. Bus Mode 3 and 4 Bus Master Write (Preview of Address)
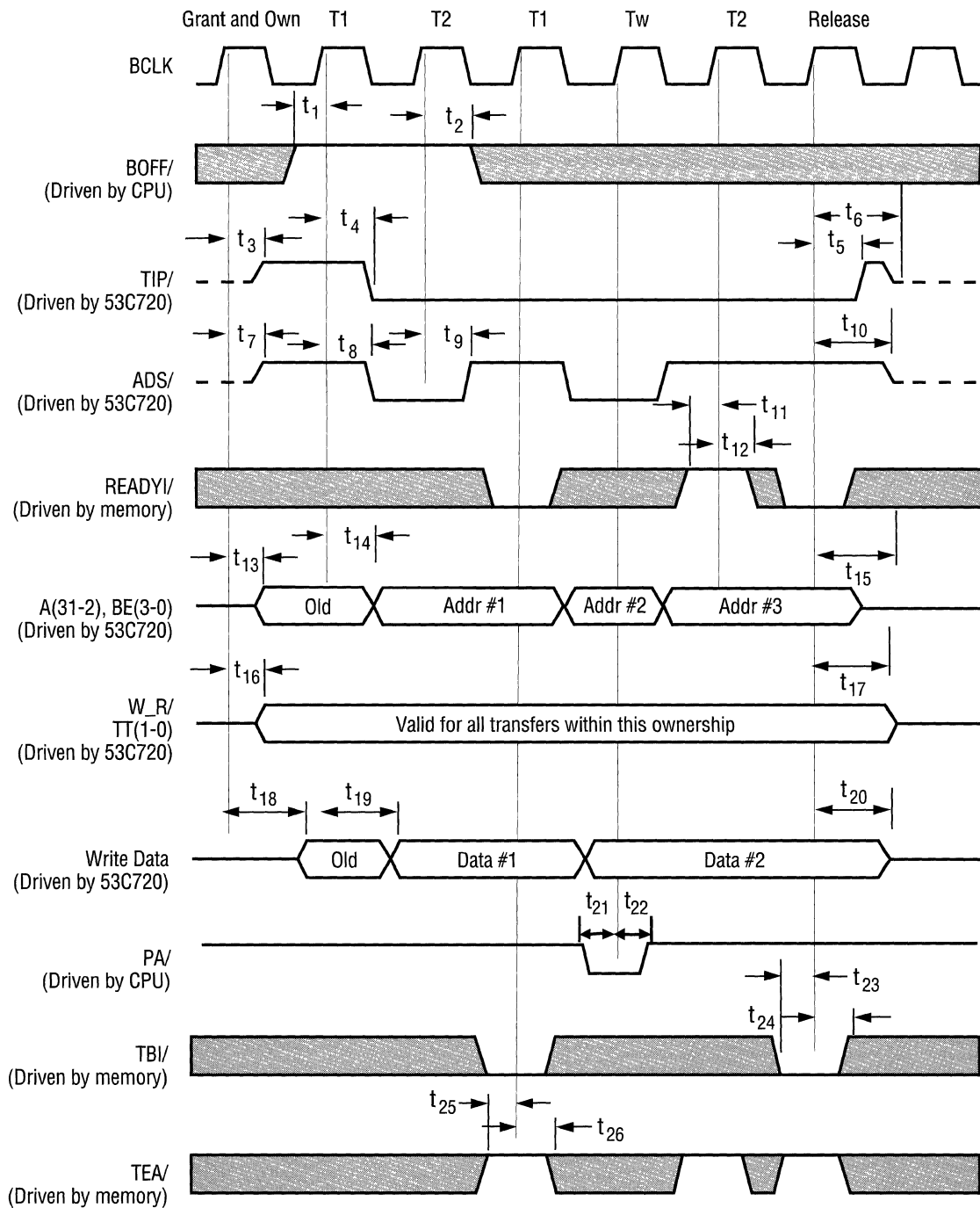
*Note: This diagram shows two back-to-back transfers for a burst size of two.*

Bus Mode 4 Bus Master Write Timings (Cache Line Burst)

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to TIP/ driven	t_3	5	32	ns
BCLK high to TIP/ low	t_4	3	20	ns
BCLK high to TIP/ high	t_5	3	20	ns
BCLK high to TIP/ high-Z	t_6	7	32	ns
BCLK high to ADS/ driven	t_7	5	30	ns
BCLK high to ADS/ low	t_8	3	17	ns
BCLK high to ADS/ high	t_9	3	17	ns
BCLK high to ADS/ high-Z	t_{10}	7	32	ns
READYI/ setup to BCLK high	t_{11}	9	-	ns
READYI/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-2), SIZ(1-0) driven	t_{13}	5	28	ns
BCLK high to A(31-2), SIZ(1-0) valid	t_{14}	3	20	ns
BCLK high to A(31-2), SIZ(1-0) high-Z	t_{15}	7	32	ns
BCLK high to W_R/, TM(1-0), TT(1-0) driven and valid	t_{16}	5	30	ns
BCLK high to W_R/, TM(2-0), TT(1-0) high-Z	t_{17}	5	32	ns
BCLK high to Write Data driven	t_{18}	5	34	ns
BCLK high to Write Data valid	t_{19}	5	24	ns
BCLK high to Write Data high-Z	t_{20}	5	30	ns
TBI/ setup to BCLK high	t_{21}	6	-	ns
TBI/ hold from BCLK high	t_{22}	4	-	ns
TEA/ setup to BCLK high	t_{23}	9	-	ns
TEA/ hold from BCLK high	t_{24}	5	-	ns
BCLK high to CBREQ/ driven	t_{25}	5	28	ns
BCLK high to CBREQ/ low	t_{26}	5	20	ns
BCLK high to CBREQ/ high	t_{27}	5	20	ns
BCLK high to CBREQ/ high-z	t_{28}	7	32	ns

Figure 6-38. Bus Mode 4 Bus Master Write (Cache Line Burst)
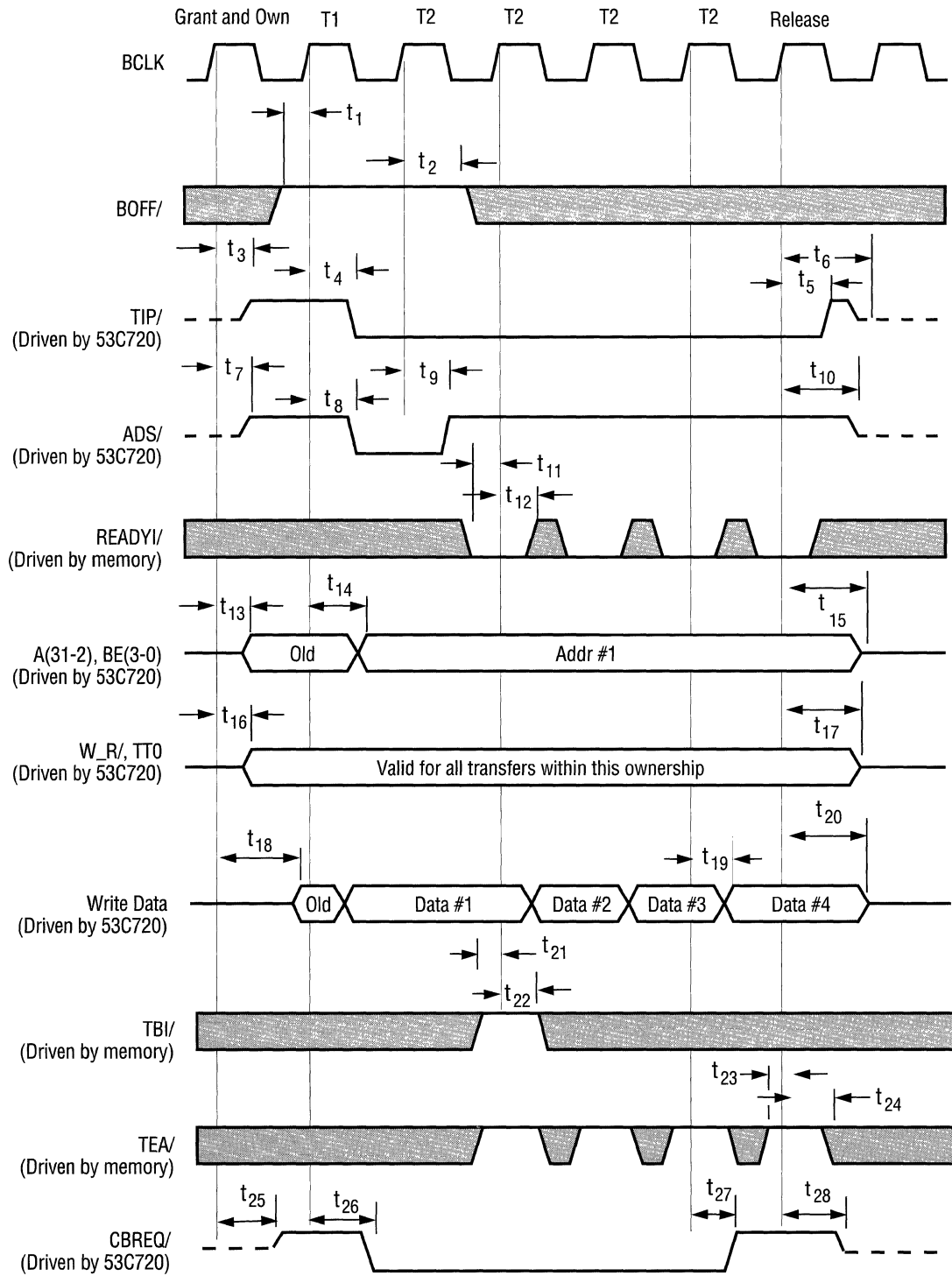
Note: This diagram shows two back-to-back transfers for a burst size of two.

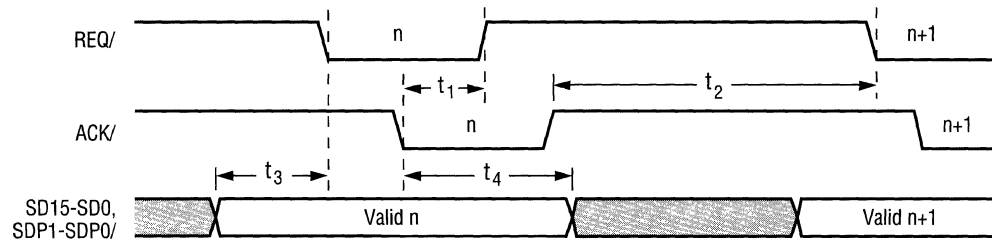# SCSI Timings

Figure 6-39. Initiator
Asynchronous Send
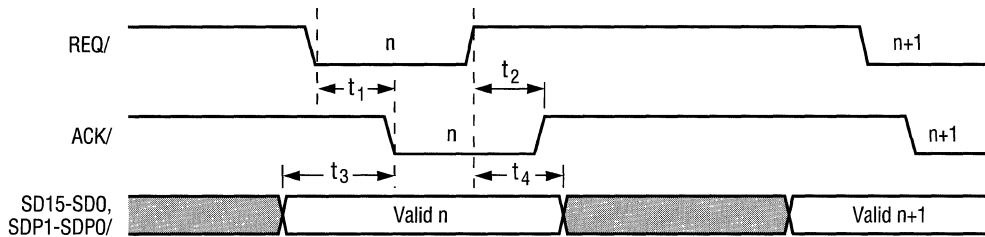
Parameter	Symbol	Min	Max	Units
ACK/ asserted from REQ/ asserted	t_1	10	-	ns
ACK/ deasserted from REQ/ deasserted	t_2	10	-	ns
Data setup to ACK/ asserted	t_3	55	-	ns
Data hold from REQ/ deasserted	t_4	20	-	ns

Figure 6-40. Initiator
Asynchronous Receive
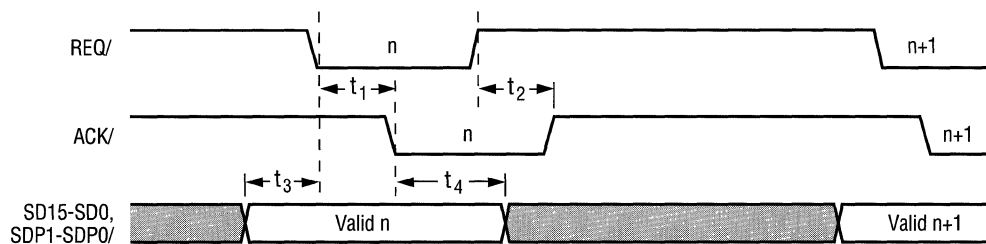
Parameter	Symbol	Min	Max	Units
ACK/ asserted from REQ/ asserted	t_1	10	-	ns
ACK/ deasserted from REQ/ deasserted	t_2	10	-	ns
Data setup to REQ/ asserted	t_3	0	-	ns
Data hold from ACK/ deasserted	t_4	0	-	ns

Figure 6-41. Target Asynchronous Send

Parameter	Symbol	Min	Max	Units
REQ/ deasserted from ACK/ asserted	t_1	10	-	ns
REQ/ asserted from ACK/ deasserted	t_2	10	-	ns
Data setup to REQ/ asserted	t_3	55	-	ns
Data hold from ACK/ asserted	t_4	20	-	ns

Figure 6-42. Target Asynchronous Receive
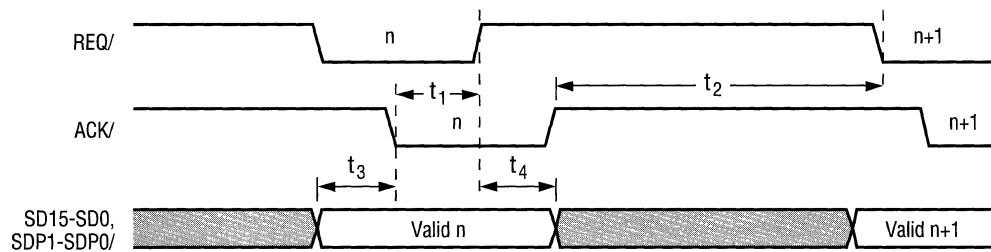
Parameter	Symbol	Min	Max	Units
REQ/ deasserted from ACK/ asserted	t_1	10	-	ns
REQ/ asserted from ACK/ deasserted	t_2	10	-	ns
Data setup to ACK/ asserted	t_3	0	-	ns
Data hold from REQ/ deasserted	t_4	0	-	ns

Figure 6-43. Initiator and Target Synchronous Transfers
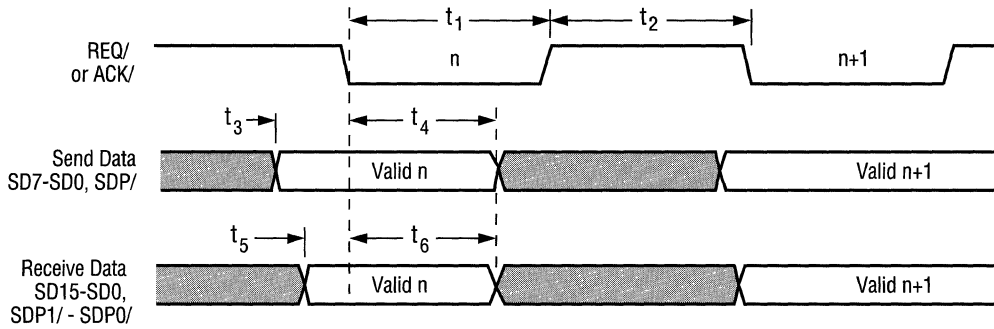
SCSI-1 Transfers (Single Ended, 5.0 MB/sec)

Parameter	Symbol	Min	Max	Units
Send REQ/ or ACK/ assertion pulse width	t_1	90	-	ns
Send REQ/ or ACK/ deassertion pulse width	t_2	90	-	ns
Receive REQ/ or ACK/ assertion pulse width	t_1	90	-	ns
Receive REQ/ or ACK/ deassertion pulse width	t_2	90	-	ns
Send data setup to REQ/ or ACK/ asserted	t_3	55	-	ns
Send data hold from REQ/ or ACK/ asserted	t_4	100	-	ns
Receive data setup to REQ/ or ACK/ asserted	t_5	0	-	ns
Receive data hold from REQ/ or ACK/ asserted	t_6	45	-	ns

SCSI-1 Transfers (Differential, 4.17 MB/sec)

Parameter	Symbol	Min	Max	Units
Send REQ/ or ACK/ assertion pulse width	t_1	96	-	ns
Send REQ/ or ACK/ deassertion pulse width	t_2	96	-	ns
Receive REQ/ or ACK/ assertion pulse width	t_1	84	-	ns
Receive REQ/ or ACK/ deassertion pulse width	t_2	84	-	ns
Send data setup to REQ/ or ACK/ asserted	t_3	65	-	ns
Send data hold from REQ/ or ACK/ asserted	t_4	110	-	ns
Receive data setup to REQ/ or ACK/ asserted	t_5	0	-	ns
Receive data hold from REQ/ or ACK/ asserted	t_6	45	-	ns

SCSI-2 Fast Transfers (10.0 MB/sec, 40 MHz Clock)

Parameter	Symbol	Min	Max	Units
Send REQ/ or ACK/ assertion pulse width	t_1	35	-	ns
Send REQ/ or ACK/ deassertion pulse width	t_2	35	-	ns
Receive REQ/ or ACK/ assertion pulse width	t_1	24	-	ns
Receive REQ/ or ACK/ deassertion pulse width	t_2	24	-	ns
Send data setup to REQ/ or ACK/ asserted	t_3	33	-	ns
Send data hold from REQ/ or ACK/ asserted	t_4	45	-	ns
Receive data setup to REQ/ or ACK/ asserted	t_5	0	-	ns
Receive data hold from REQ/ or ACK/ asserted	t_6	10	-	ns

SCSI-2 Fast Transfers (10.0 MB/sec, 50 MHz clock)

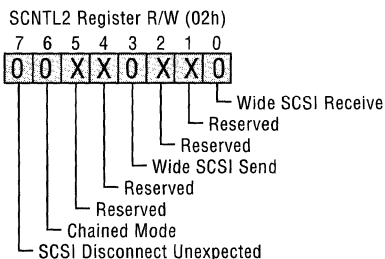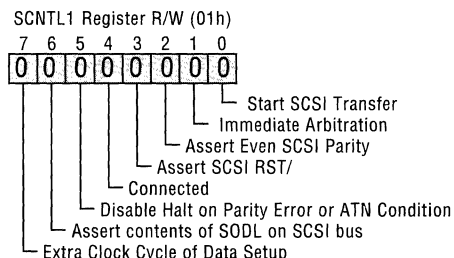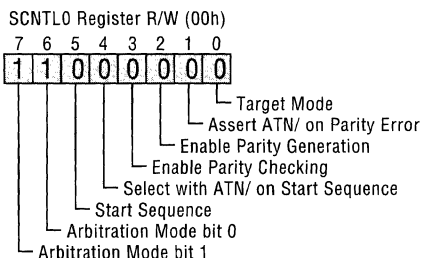| Parameter	Symbol	Min	Max	Units
Send REQ/ or ACK/ assertion pulse width	t_1	35	-	ns
Send REQ/ or ACK/ deassertion pulse width	t_2	35	-	ns
Receive REQ/ or ACK/ assertion pulse width	t_1	24	-	ns
Receive REQ/ or ACK/ deassertion pulse width	t_2	24	-	ns
Send data setup to REQ/ or ACK/ asserted	t_3	33	-	ns
Send data hold from REQ/ or ACK/ asserted	t_4	40**	-	ns
Receive data setup to REQ/ or ACK/ asserted	t_5	0	-	ns
Receive data hold from REQ/ or ACK/ asserted	t_6	10	-	ns

* *Transfer period bits (bits 6-4 in the SXFER register) are set to zero and the extra clock cycle of data setup bit (bit 7 in SCNTL1) is set.*

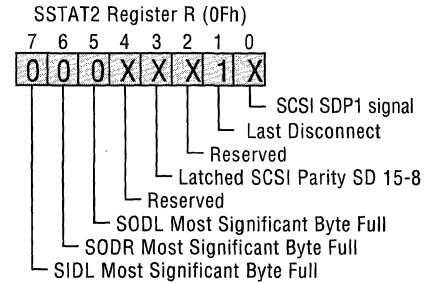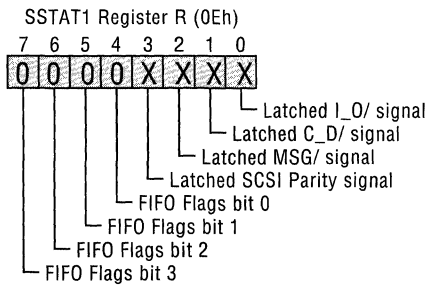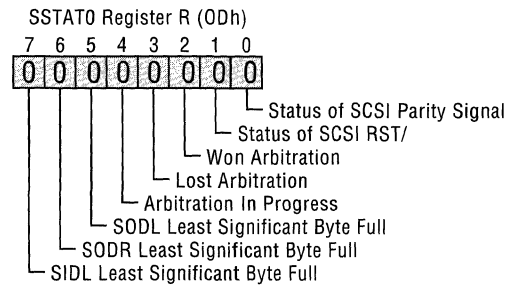** *Analysis of system configuration is recommended due to reduced driver skew margin in differential systems.*
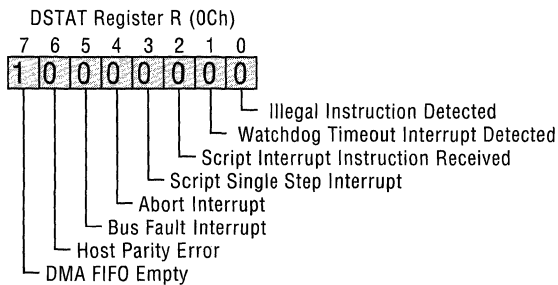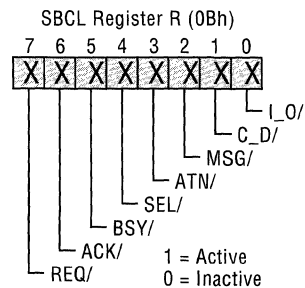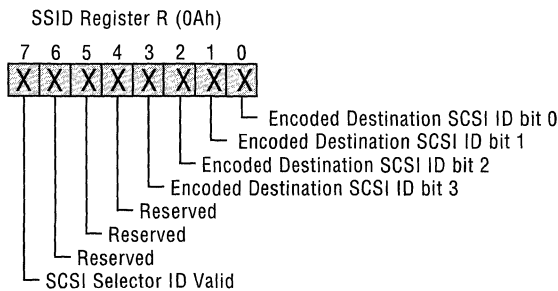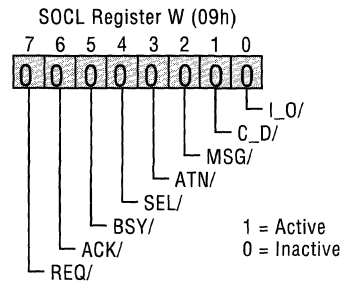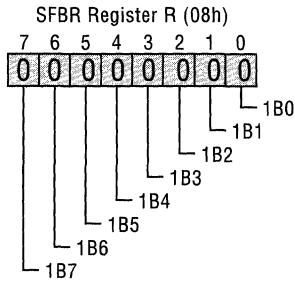
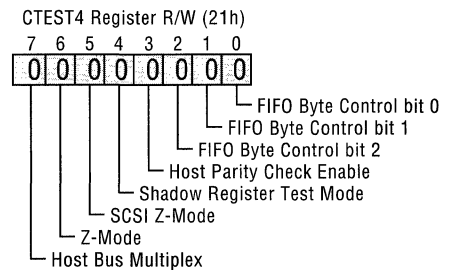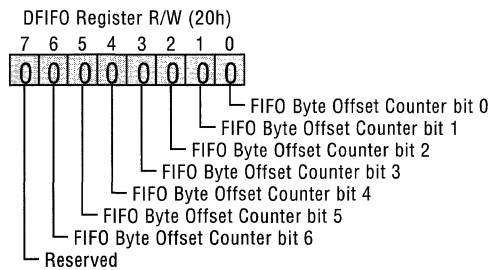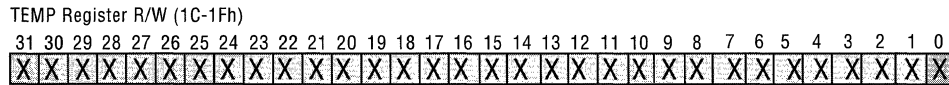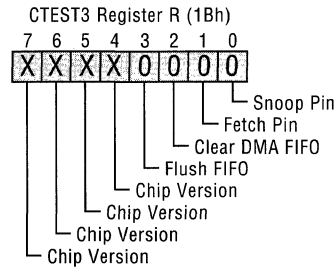**Note:** *For fast SCSI, the TolerANT Enable bit (STEST3 bit 7) should be set.*

Appendix A
Register Summary

SCNTL0 Register R/W (00h)

```
 7  6  5  4  3  2  1  0
[1][1][0][0][0][0][0][0]
```
- Target Mode
- Assert ATN/ on Parity Error
- Enable Parity Generation
- Enable Parity Checking
- Select with ATN/ on Start Sequence
- Start Sequence
- Arbitration Mode bit 0
- Arbitration Mode bit 1

SCNTL1 Register R/W (01h)

```
 7  6  5  4  3  2  1  0
[0][0][0][0][0][0][0][0]
```
- Start SCSI Transfer
- Immediate Arbitration
- Assert Even SCSI Parity
- Assert SCSI RST/
- Connected
- Disable Halt on Parity Error or ATN Condition
- Assert contents of SODL on SCSI bus
- Extra Clock Cycle of Data Setup

SCNTL2 Register R/W (02h)

```
 7  6  5  4  3  2  1  0
[0][0][X][X][0][X][X][0]
```
- Wide SCSI Receive
- Reserved
- Reserved
- Wide SCSI Send
- Reserved
- Reserved
- Chained Mode
- SCSI Disconnect Unexpected

SCNTL3 Register R/W 03

```
 7  6  5  4  3  2  1  0
[X][0][0][0][0][0][0][0]
```
- Clock Conversion Factor
- Clock Conversion Factor
- Clock Conversion Factor
- Enable Wide SCSI
- Synchronous Clock Conversion Factor bit 0
- Synchonous Clock Conversion Factor bit 1
- Synchronous Clock Conversion Factor bit 2
- Reserved

SCID Register R/W (04h)

```
 7  6  5  4  3  2  1  0
[X][0][0][X][0][0][0][0]
```
- Encoded Chip ID 0
- Encoded Chip ID 1
- Encoded Chip ID 2
- Encoded Chip ID 3
- Reserved
- Enable Response to Selection
- Enable Response to Reselection
- Reserved

SXFER Register R/W (05h)

```
 7  6  5  4  3  2  1  0
[0][0][0][X][0][0][0][0]
```
- Max SCSI Synchronous Offset 0
- Max SCSI Synchronous Offset 1
- Max SCSI Synchronous Offset 2
- Max SCSI Synchronous Offset 3
- Reserved
- Synchronous Transfer Period bit 0
- Synchronous Transfer Period bit 1
- Synchronous Transfer Period bit 2

SDID Register R/W (06h)

```
 7  6  5  4  3  2  1  0
[X][X][X][X][0][0][0][0]
```
- Encoded Destination ID 0
- Encoded Destination ID 1
- Encoded Destination ID 2
- Encoded Destination ID 3
- Reserved
- Reserved
- Reserved
- Reserved

GPREG Register R/W (07h)

```
 7  6  5  4  3  2  1  0
[X][X][X][0][X][X][X][X]
```
- General Purpose I/O 0
- General Purpose I/O 1
- General Purpose I/O 2
- General Purpose I/O 3
- General Purpose I/O 4
- Reserved
- Reserved
- Reserved

SFBR Register R (08h)

```
7 6 5 4 3 2 1 0
0 0 0 0 0 0 0 0
              └─ 1B0
            └─ 1B1
          └─ 1B2
        └─ 1B3
      └─ 1B4
    └─ 1B5
  └─ 1B6
└─ 1B7
```

SOCL Register W (09h)

```
7 6 5 4 3 2 1 0
0 0 0 0 0 0 0 0
              └─ I_O/
            └─ C_D/
          └─ MSG/
        └─ ATN/
      └─ SEL/
    └─ BSY/      1 = Active
  └─ ACK/        0 = Inactive
└─ REQ/
```

SSID Register R (0Ah)

```
7 6 5 4 3 2 1 0
X X X X X X X X
              └─ Encoded Destination SCSI ID bit 0
            └─ Encoded Destination SCSI ID bit 1
          └─ Encoded Destination SCSI ID bit 2
        └─ Encoded Destination SCSI ID bit 3
      └─ Reserved
    └─ Reserved
  └─ Reserved
└─ SCSI Selector ID Valid
```

SBCL Register R (0Bh)

```
7 6 5 4 3 2 1 0
X X X X X X X X
              └─ I_O/
            └─ C_D/
          └─ MSG/
        └─ ATN/
      └─ SEL/
    └─ BSY/
  └─ ACK/      1 = Active
└─ REQ/        0 = Inactive
```

DSTAT Register R (0Ch)

```
7 6 5 4 3 2 1 0
1 0 0 0 0 0 0 0
              └─ Illegal Instruction Detected
            └─ Watchdog Timeout Interrupt Detected
          └─ Script Interrupt Instruction Received
        └─ Script Single Step Interrupt
      └─ Abort Interrupt
    └─ Bus Fault Interrupt
  └─ Host Parity Error
└─ DMA FIFO Empty
```

SSTAT0 Register R (0Dh)

```
7 6 5 4 3 2 1 0
0 0 0 0 0 0 0 0
              └─ Status of SCSI Parity Signal
            └─ Status of SCSI RST/
          └─ Won Arbitration
        └─ Lost Arbitration
      └─ Arbitration In Progress
    └─ SODL Least Significant Byte Full
  └─ SODR Least Significant Byte Full
└─ SIDL Least Significant Byte Full
```

SSTAT1 Register R (0Eh)

```
7 6 5 4 3 2 1 0
0 0 0 0 X X X X
              └─ Latched I_O/ signal
            └─ Latched C_D/ signal
          └─ Latched MSG/ signal
        └─ Latched SCSI Parity signal
      └─ FIFO Flags bit 0
    └─ FIFO Flags bit 1
  └─ FIFO Flags bit 2
└─ FIFO Flags bit 3
```

SSTAT2 Register R (0Fh)

```
7 6 5 4 3 2 1 0
0 0 0 X X X 1 X
              └─ SCSI SDP1 signal
            └─ Last Disconnect
          └─ Reserved
        └─ Latched SCSI Parity SD 15-8
      └─ Reserved
    └─ SODL Most Significant Byte Full
  └─ SODR Most Significant Byte Full
└─ SIDL Most Significant Byte Full
```

DSA Register R/W (10-13h)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

ISTAT Register R/W (14h)
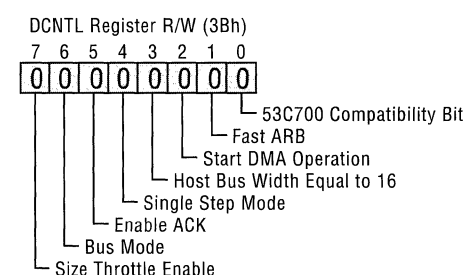
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

- DMA Interrupt Pending
- SCSI Interrupt Pending
- Interrupt on the Fly
- Connected/Disconnect
- Semaphore
- Signal Process
- Software Reset
- Abort Operation

CTEST0 Register R/W (18h)

7	6	5	4	3	2	1	0
0	0	0	X	0	0	0	0

- Cache 386 Enable
- Transfer Type bit 1
- Even Parity
- DMA FIFO Parity
- Generate Receive Parity for Pass-Through
- Snoop Control 0
- Snoop Control 1
- Cache Burst Disable

CTEST1 Register R (19h)

7	6	5	4	3	2	1	0
1	1	1	1	0	0	0	0

- Byte Lane 0 Full in DMA FIFO
- Byte Lane 1 Full in DMA FIFO
- Byte Lane 2 Full in DMA FIFO
- Byte Lane 3 Full in DMA FIFO
- Byte Lane 0 Empty in DMA FIFO
- Byte Lane 1 Empty in DMA FIFO
- Byte Lane 2 Empty in DMA FIFO
- Byte Lane 3 Empty in DMA FIFO

CTEST2 Register R (1Ah)

7	6	5	4	3	2	1	0
0	0	X	X	0	0	0	1

- DACK/ Status
- DREQ Status
- SCSI TEOP Status
- DMA FIFO Parity bit
- Reserved
- Reserved
- Signal Process
- Data Transfer Direction

CTEST3 Register R (1Bh)

7	6	5	4	3	2	1	0
X	X	X	X	0	0	0	0

- Snoop Pin
- Fetch Pin
- Clear DMA FIFO
- Flush FIFO
- Chip Version
- Chip Version
- Chip Version
- Chip Version

TEMP Register R/W (1C-1Fh)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

DFIFO Register R/W (20h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

- FIFO Byte Offset Counter bit 0
- FIFO Byte Offset Counter bit 1
- FIFO Byte Offset Counter bit 2
- FIFO Byte Offset Counter bit 3
- FIFO Byte Offset Counter bit 4
- FIFO Byte Offset Counter bit 5
- FIFO Byte Offset Counter bit 6
- Reserved

CTEST4 Register R/W (21h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

- FIFO Byte Control bit 0
- FIFO Byte Control bit 1
- FIFO Byte Control bit 2
- Host Parity Check Enable
- Shadow Register Test Mode
- SCSI Z-Mode
- Z-Mode
- Host Bus Multiplex

CTEST5 Register R/W (22h)

```
7  6  5  4  3  2  1  0
0  0  X  0  0  X  X  X
```
- Reserved
- Reserved
- Reserved
- DMA Direction
- Master Control for Set or Reset Pulses
- Reserved
- Clock Byte Counter (DBC)
- Clock Address Incrementor (DNAD)

CTEST6 Register R/W (23h)

```
7  6  5  4  3  2  1  0
0  0  0  0  0  0  0  0
```
- DMA FIFO bit 0
- DMA FIFO bit 1
- DMA FIFO bit 2
- DMA FIFO bit 3
- DMA FIFO bit 4
- DMA FIFO bit 5
- DMA FIFO bit 6
- DMA FIFO bit 7

DBC Register R/W (24-26h)

```
23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
X  X  X  X  X  X  X  X  X  X  X  X  X  X  X X X X X X X X X X
```

DCMD Register R/W (27h)

```
7  6  5  4  3  2  1  0
0  0  0  0  0  0  0  0
```
- Function bit 0
- Function bit 1
- Function bit 2
- Function bit 3
- Function bit 4
- Function bit 5
- Instruction Op Code bit 0
- Instruction Op Code bit 1

DNAD Register R/W (28-2Bh)

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0 0 0 0 0 0 0 0 0 0
```

DSP Register R/W (2C-2Fh)

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0 0 0 0 0 0 0 0 0 0
```

DSPS Register R/W (30-33h)

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
X  X  X  X  X  X  X  X  X  X  X  X  X  X  X  X  X  X  X  X  X  X  X X X X X X X X X X
```

SCRATCHA Register R/W (34-37h)

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
X  X  X  X  X  X  X  X  X  X  X  X  X  X  X  X  X  X  X  X  X  X  X X X X X X X X X X
```

DMODE Register R/W (38h)

```
7  6  5  4  3  2  1  0
0  0  0  0  0  0  0  0
```
└ Manual Start Mode
└ User Programmable Transfer
└ Fixed Address Mode
└ Program Data
└ Function Code bit 1
└ Function Code bit 2
└ Burst Length bit 0
└ Burst Length bit 1

DIEN Register R/W (39h)

```
7  6  5  4  3  2  1  0
X  0  0  0  0  0  0  0
```
└ Enable Illegal Instruction Interrupt
└ Enable Watchdog Time-Out Interrupt
└ Enable Script Interrupt Instruction Received Interrupt
└ Enable Script Step Interrupt
└ Enable Aborted Interrupt
└ Enable Bus Fault Interrupt
└ Host Parity Error Detected
└ Reserved

DWT Register R/W (3Ah)

```
7  6  5  4  3  2  1  0
0  0  0  0  0  0  0  0
```
└ DWT0
└ DWT1
└ DWT2
└ DWT3
└ DWT4
└ DWT5
└ DWT6
└ DWT7

DCNTL Register R/W (3Bh)

```
7  6  5  4  3  2  1  0
0  0  0  0  0  0  0  0
```
└ 53C700 Compatibility Bit
└ Fast ARB
└ Start DMA Operation
└ Host Bus Width Equal to 16
└ Single Step Mode
└ Enable ACK
└ Bus Mode
└ Size Throttle Enable

ADDER Register R (3C-3Fh)

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
X  X  X  X  X  X  X  X  X  X  X  X  X  X  X  X  X  X  X  X  X  X X X X X X X X X X X
```

SIEN0 Register R/W (40h)

```
7  6  5  4  3  2  1  0
0  0  0  0  0  0  0  0
```
└ Parity Error Received
└ SCSI RST/ Received
└ Unexpected Disconnect
└ SCSI Gross Error
└ Reselected
└ Selected
└ Function Complete
└ Phase Mismatch or ATN/ Active

SIEN1 Register R/W (41h)

```
7  6  5  4  3  2  1  0
0  0  0  0  0  0  0  0
```
└ Handshake-to-HandshakeTimer Expired
└ General Purpose Timer Expired
└ Selection or Reselection Time-Out
└ Reserved
└ Reserved
└ Reserved
└ Reserved
└ Reserved

SIST0 Register R (42h)

```
7  6  5  4  3  2  1  0
0  0  0  0  0  0  0  0
```
└ Parity Error Received
└ SCSI RST/ received
└ Unexpected Disconnect
└ SCSI Gross Error
└ Reselected
└ Selected
└ Function Complete
└ Phase Mismatch or ATN/ Active

SIST1 Register R (43h)

```
7  6  5  4  3  2  1  0
0  0  0  0  0  0  0  0
```
└ Handshake-to-Handshake Timer Expired
└ General Purpose Timer Expired
└ Selection/Reselection Time-Out
└ Reserved
└ Reserved
└ Reserved
└ Reserved
└ Reserved

SLPAR Register R/W (44h)

7 6 5 4 3 2 1 0
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

└─ SCSI Longitudinal Parity
└── SCSI Longitudinal Parity
└─── SCSI Longitudinal Parity
└──── SCSI Longitudinal Parity
└───── SCSI Longitudinal Parity
└────── SCSI Longitudinal Parity
└─────── SCSI Longitudinal Parity
└──────── SCSI Longitudinal Parity

SWIDE Register R (45h)

7 6 5 4 3 2 1 0
| X | X | X | X | X | X | X | X |

└─ SRD8
└── SRD9
└─── SRD10
└──── SRD11
└───── SRD12
└────── SRD13
└─────── SRD14
└──────── SRD15

Memory Access Control Register R/W (46h)

7 6 5 4 3 2 1 0
| X | X | X | X | 0 | 0 | 0 | 0 |

└─ SCRIPTS fetch
└── Pointer to SCRIPTS fetch
└─── Data Read
└──── Data Write
└───── Reserved
└────── Reserved
└─────── Reserved
└──────── Reserved

General Purpose Control Register R/W (47h)

7 6 5 4 3 2 1 0
| X | X | X | X | 0 | 0 | 0 | 0 |

└─ General Purpose Output Enable bit 0
└── General Purpose Output Enable bit 1
└─── General Purpose Output Enable bit 2
└──── General Purpose Output Enable bit 3
└───── General Purpose Output Enable 4
└────── Reserved
└─────── Reserved
└──────── Reserved

STIME0 Register R/W (48h)

7 6 5 4 3 2 1 0
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

└─ Selection Time-Out Period bit 0
└── Selection Time-Out Period bit 1
└─── Selection Time-Out Period bit 2
└──── Selection Time-Out Period bit 3
└───── Handshake-to-Handshake Timer Period bit 0
└────── Handshake-to-Handshake Timer Period bit 1
└─────── Handshake-to-Handshake Timer Period bit 2
└──────── Handshake-to-Handshake Timer Period bit 3

STIME1 Register R/W (49h)

7 6 5 4 3 2 1 0
| X | X | X | X | 0 | 0 | 0 | 0 |

└─ General Purpose Timer Period bit 0
└── General Purpose Timer Period bit 1
└─── General Purpose Timer Period bit 2
└──── General Purpose Timer Period bit 3
└───── Reserved
└────── Reserved
└─────── Reserved
└──────── Reserved

RESPID0 Register R (4Ah)

7 6 5 4 3 2 1 0
| X | X | X | X | 0 | X | 1 | 1 |

RESPID1 Register R (4Bh)

7 6 5 4 3 2 1 0
| X | X | X | X | 0 | X | 1 | 1 |

STEST0 Register R (4Ch)

7 6 5 4 3 2 1 0
| X | X | X | X | 0 | X | 1 | 1 |

└─ SCSI Synchronous Offset Maximum
└── SCSI Synchronous Offset Zero
└─── Arbitration Priority Encoder Test
└──── Selection Response Logic Test
└───── Reserved
└────── Reserved
└─────── Reserved
└──────── Reserved

STEST1 Register R (4Dh)

7 6 5 4 3 2 1 0
| X | X | X | X | X | X | X | X |

└─ SCSI FIFO Parity bit 0
└── SCSI FIFO Parity bit 1
└─── Reserved
└──── Reserved
└───── Reserved
└────── Reserved
└─────── Reserved
└──────── Reserved

STEST2 Register R/W (4Eh)

```
 7  6  5  4  3  2  1  0
[0][0][0][0][0][0][0][0]
                      └─ SCSI Low-Level Mode
                   └─ Extend Req/Ack filtering
                └─ Always Wide SCSI
             └─ SCSI High Impedance Mode
          └─ SCSI Loopback Mode
       └─ SCSI Differential Mode
    └─ Reset SCSI Offset
 └─ SCSI Control Enable
```

STEST3 Register R/W (4Fh)

```
 7  6  5  4  3  2  1  0
[X][X][0][0][0][0][0][0]
                      └─ SCSI FIFO Test Write
                   └─ Clear SCSI FIFO
                └─ Timer Test Mode
             └─ 16-bit System
          └─ Disable Single Initiator Response
       └─ Halt SCSI Clock
    └─ SCSI FIFO Test Read
 └─ TolerANT Enable
```

SIDL Register R (50-51h)

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
[X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X]
                                              └─ SDB0
                                           └─ SDB1
                                        └─ SDB2
                                     └─ SDB3
                                  └─ SDB4
                               └─ SDB5
                            └─ SDB6
                         └─ SDB7
                      └─ SDB8
                   └─ SDB9
                └─ SDB10
             └─ SDB11
          └─ SDB12
       └─ SDB13
    └─ SDB14
 └─ SDB15
```

SODL Register R/W (54-55h)

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
[X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X]
                                              └─ SDB0
                                           └─ SDB1
                                        └─ SDB2
                                     └─ SDB3
                                  └─ SDB4
                               └─ SDB5
                            └─ SDB6
                         └─ SDB7
                      └─ SDB8
                   └─ SDB9
                └─ SDB10
             └─ SDB11
          └─ SDB12
       └─ SDB13
    └─ SDB14
 └─ SDB15
```

SBDL Register R (58-59h)

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
[X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X]
                                              └─ SDB0
                                           └─ SDB1
                                        └─ SDB2
                                     └─ SDB3
                                  └─ SDB4
                               └─ SDB5
                            └─ SDB6
                         └─ SDB7
                      └─ SDB8
                   └─ SDB9
                └─ SDB10
             └─ SDB11
          └─ SDB12
       └─ SDB13
    └─ SDB14
 └─ SDB15
```

SCRATCHB Register R/W (5C-5Fh)

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
[X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X][X]
```

Appendix B
Mechanical Drawing

Pin 208

Pin 1 Indicator

Pin 157

**208-Pin Plastic
Quad Flat Package (QFP)**

Pin 52

Pin 104

0.25 Max
0.18 Min

.50 Typ

31.90 ± 0.25

28.00 ± 0.10

25.50

25.50

28.00 ± 0.10

3.42 ± 0.25

4.07
Max

0.25
Min

Seating
Plane

$0.15 \begin{array}{c} +0.08 \\ -0.02 \end{array}$

$0° \leq Ø \leq 7°$

0.8 ± 0.15

31.90 ± 0.25

Appendix C
Application Notes

NCR

INTRODUCTION

This application note compares the 53C720 with the 53C710. There are four categories of 53C720 differences.

A. Host Bus Interface Differences
B. SCRIPT Instruction Differences
C. SCSI Bus Interface Differences
D. Register Differences

FEATURES

The "Features" section summarizes the high-level differences.

	FEATURES	53C710	53C720
1.	SCSI Data Transfer Rate		
	- Asynchronous	5 Mbytes/sec	10 Mbytes/sec
	- Synchronous	10 Mbytes/sec	20 Mbytes/sec
2.	DMA Transfer Rate	66 Mbytes/sec	105 Mbytes/sec
3.	Host Bus Width	32 bits	16 or 32 bits
4.	SCSI Bus Width	8 bits	8 or 16 bits
5.	Interrupt On-The-Fly	Not Supported	Supported
6.	Bus Modes	4	7
7.	SCRIPT Auto-Start	Not Supported	Supported
8.	Programmable Burst Length	1,2,4 or 8	2,4,8 or 16
9.	Shadowed Temp and		
	DSA Registers	Not Supported	Supported
10.	Programmable SCSI Timers	Not Supported	3
11.	General Purpose I/O Pins	Not Supported	Supported
12.	Differential Sense Pin	Not Supported	Supported
13.	Preview Of Next Address	Not Supported	Supported
14.	Carry Bit In ALU	Not Supported	Supported
15.	Semaphore Bit	Not Supported	Supported
16.	Devices On SCSI Bus	8	16
17.	Host Parity Checking	Not Supported	Supported

A. HOST BUS INTERFACE DIFFERENCES

The 53C720 host bus interface has been significantly enhanced over that of the 53C710. Greater flexibility and functionality has been provided allowing the 53C720 to directly interface with a larger number of host busses. The 53C720 is still compatible signal for signal with the 53C710 host bus interface. The 53C720 host bus interface differences are as follows:

Bus Mode Select Pins

Function
> The 53C720 is capable of interfacing with host busses in a combination of the following modes: Motorola or Intel, Big or Little Endian, 68040_68030 or 80386dx_80386sx. If Intel and one of the 80386 modes is selected, several pins change functions. In particular the R_W/ pin becomes inverted and SIZ0, SIZ1, A0 and A1 become byte enable signals. The 53C710 is only capable of interfacing with host busses in a combination of the following modes without external hardware: Big or Little Endian, 68030 or 68040.

Benefit
> The ability to interface with seven different host processor busses provides the user with additional flexibility.

Enhanced Cache-Line Burst

Function
> Cache-Line burst eliminates the need for a full handshake between the 53C720 bus and the memory device when transferring data. The bus master will arbitrate for the bus at the beginning of a 16 byte transfer and it is able to transfer one long word per clock period. The 53C720 is able to start another cache-line burst without getting off the bus if it has another 8 long words stored in its FIFO. Under optimal conditions the 53C720 will have 16 long words in its FIFO and it is therefore able to do four back-to-back cache transfers. A cache line burst is always 4 long words in length. The 53C710 was only capable of doing one cache-line burst before it had to get off the bus.

Benefit
> Cache-Line Burst mode allows up to 105 Mbytes/sec DMA burst bandwidth for extremely high data transfer rates or streaming modes. The 53C710 is only capable of doing 66 Mbytes/sec DMA transfers.

Sense Pin for SCRIPT Auto-Start

Function
> When the SCRIPT auto-start sense pin is tied to ground the DMA SCRIPTS Pointer Register (DSP) points to an address of all zeros and the SCRIPTS processor will start fetching instructions from that location. If the sense pin is tied high, the DSP register will have to be written with the starting address of the first SCRIPT instruction.

Benefit
> The auto-start feature enables the 53C720 to start the SCRIPT program automatically after reset is deasserted. SCRIPT instructions will be fetched and executed until an interrupt condition occurs.

General Purpose Input and Output Pins

Function
> The 53C720 has four inputs and one output pin. These pins are user defined.

Benefit
> The input pins may be used to read the 53C720 chip ID or other configuration information. The output pin may be used to enable on-board ROM, RAM or LED's.

Memory Access Control Pin

Function
> This signal indicates if the next access will be to local memory (on-board memory) or far memory (system memory).

Benefit
> The ability to choose between near and far memory provides system design flexibility, with faster access to data in local memory.

Test In and Test Out Pins

Function
> These pins connect all inputs and outputs (excluding SCSI control signals and data lines) to an AND tree test scheme.

Benefit
> This function allows manufacturers to verify chip connectivity to the board, and to determine exactly which pins are not properly attached.

B. SCRIPT INSTRUCTION DIFFERENCES

Five SCRIPT instructions have been added to the 53C720. The 53C720 utilizes all of the SCRIPTs instructions available for the 53C710, therefore, SCRIPTs programs developed for the 53C710 will be upward compatible. For a more detailed description of the SCRIPT language, reference the NCR 53C720 Programmer's Guide. Following is a list and description of the four instructions.

CHMOV Instruction

Function
> The CHMOV instruction transfers data to and from memory locations. Data may come from any data location, so scatter/gather operations are transparent to the chip and the external processor.

Benefit
> When the 53C720 executes several CHMOV instructions and one ends on an odd byte boundary, the 53C720 temporarily stores the residual byte. The 53C720 takes the first byte from the subsequent CHMOV or MOVE instruction and line it up with the residual byte in order to complete a wide transfer and maintain a continuous data flow on the SCSI bus.

INTFLY Instruction

Function

The INTFLY instruction (DBC, bit 20) will assert the interrupt on the fly bit (ISTAT, bit 2) once the SCRIPT instruction is executed. SCRIPTS programs will not halt when the interrupt occurs. The interrupt must be serviced by reading the Interrupt Status Register only.

Benefit

The INTFLY instruction is used to notify a service routine, running on the main processor, while the SCRIPT processor is still executing a SCRIPTS program.

Transfer Control Instruction on Carry

Function

Jump, Call, Return or Interrupt may be executed depending on the resulting carry bit (DBC, bit 21) after an add operation. When executing a transfer control instruction true/false comparisons are legal whereas compare functions are illegal. As an example, INT address, IF carry and INT address, IF NOT carry would be legal.

Benefit

The transfer control on carry feature adds additional flexibility to the user by allowing additions to cross byte boundaries.

Read/Write Instruction WITH Carry Enabled

Function

When carry is enabled (DCMD, bit 0) any read/write opcode utilizing the add operation will also add in the current carry contents. MOVE SCRATCH1 + 1 To SCRATCH1 WITH Carry, is an example.

Benefit

Enabling the carry bit allows the 53C720 to perform add operations greater than one byte, since carry values from previous byte adds may be used in successive adds.

I/O Instruction SETing or CLEARing Carry

Function

The Carry bit may be SET or CLEARed using a SCRIPT Instruction (DBC, bit 10)

Benefit

This feature permits the user to assert or deassert the carry bit prior to an addition or subtraction operation.

C. SCSI BUS INTERFACE DIFFERENCES

The primary difference between the 53C710 and the 53C720 is the implementation of Wide SCSI. The 53C720 differences are as follows:

Wide SCSI

> Function
>> The 53C720 has a 16-bit data transfer capability. There is a single request/acknowledge per transfer and the SCSI bus pinout is optimized for P or A cable connection.
>
> Benefit
>> Wide SCSI provides a significant increase in system performance especially in systems requiring a large amount of data transfer between host and peripheral devices. The 53C720, as a result of wide SCSI, transfers data over the SCSI bus at up to 20 Mbytes/sec whereas the 53C710 transfers data at up to 10 Mbytes/sec. This applies only when the SCSI bus is operating in synchronous and differential modes.

Differential Sense Pin

> Function
>> The 53C720 uses the Differential Sense pin to determine if a connected SCSI device is operating in differential or single ended mode. If the external device is operating in differential mode while the 53C720 is in single ended mode, the chip will cease to drive external outputs on the SCSI bus.
>
> Benefit
>> The sense pin protects the external differential pair transceivers and the single ended device from damage.

SCSI Clock

Function
> The 53C720 has a separate SCSI clock which operates at up to 75 MHz. The 53C710 operates the SCSI clock at up to 50 MHz.

Benefit
> Separate SCSI and bus clocks allow the host interface to operate at a lower speed while a higher speed clock controlling the SCSI bus guarantees fast SCSI timings of 20 Mbytes/sec. A clock speed of minimum 40 MHz is required for fast SCSI.

Initiator/Target Auto-Switch Disabled

Function
> The auto-switch function is disabled in the 53C720.

Benefit
> This forces the user to manually set target or initiator mode in a SCRIPT program and removes any ambiguity as to the current mode of the 53C720.

SCSI Timers

Function
> The 53C720 provides programmable select/reselect, handshake to handshake, and general purpose timers. The time-out period is programmable from 100 μsec to greater than 1.6 seconds. A maskable interrupt is available for each of the timers.

Benefit
> The timers allows the user to tailor SCRIPT instructions to their specific timeout needs.

Separation of Selection and Reselection Control

Function
> The 53C720 can be enabled to respond as a target, initiator or both. There are status and interrupt bits indicating that the 53C720 has responded to selection or reselection.

Benefit
> The 53C720 will know if it is required to respond as an initiator or a target. If the user has disabled selection and another SCSI device actually tries to select the 53C720, it may notify the main processor that this has occurred.

D. REGISTER DIFFERENCES

The following figures summarize the differences between the 53C710 and the 53C720 register sets. The register/bit additions and the resulting benefits to the user are described below. For a more detailed explanation of each of the registers in the 53C720, reference the NCR 53C720 Data Manual.

New Registers/Bits

Registers/Bits	53C710	53C720
Start SCSI Transfer bit	Not Supported	SCNTL1,bit 0
Immediate Arbitration bit	Not Supported	SCNTL1,bit 1
SCSI Control Register Two -- 02h	Not Supported	SCNTL2
Wide SCSI Receive bit	Not Supported	SCNTL2,bit 0
Wide SCSI Send bit	Not Supported	SCNTL2,bit 3
Chained Mode bit	Not Supported	SCNTL2,bit 6
SCSI Disconnect Unexpected bit	Not Supported	SCNTL2,bit 7
SCSI Control Register Three -- 03h	Not Supported	SCNTL3
Enable Wide SCSI bit	Not Supported	SCNTL3,bit 3
Enable Response to Selection bit	Not Supported	SCID,bit 5
Enable Response to Reselection bit	Not Supported	SCID,bit 6
General Purpose Register -- 07h	Not Supported	GPREG
General Purpose Inputs/Outputs	Not Supported	GPREG,bits 4-0
SCSI Selector ID Register -- 0Ah	Not Supported	SSID
Encoded Destination SCSI ID Bits	Not Supported	SSID,bits 3-0
SCSI Selector ID Valid bit	Not Supported	SSID,bit 7
SCSI Parity SD 15-8-Bit	Not Supported	SSTAT2,bit 0
Last Disconnect bit	Not Supported	SSTAT2,bit 1
Latched SCSI Parity SD 15-8-Bit	Not Supported	SSTAT2,bit 3
SODL Most Significant Byte Full	Not Supported	SSTAT2,bit 5
SODR Most Significant Byte Full	Not Supported	SSTAT2,bit 6
SIDL Most Significant Byte Full	Not Supported	SSTAT2,bit 7
Interrupt On The Fly bit	Not Supported	ISTAT,bit 2
Semaphore bit	Not Supported	ISTAT,bit 4
Cache 386 Enable bit	Not Supported	CTEST0, bit 0
Generate Receive Parity for Pass Through	Not Supported	CTEST0, bit 4
Host Parity Check Enable bit	Not Supported	CTEST4,bit 3
Shadow Register Test Mode bit	Not Supported	CTEST4,bit 4
SCSI Data Bus High Impedance Mode	Not Supported	CTEST4,bit 5
Enable Host Parity Error Interrupt	Not Supported	DIEN,bit 6
Host Bus Width 16 bits	Not Supported	DCNTL,bit 3
Bus Mode bit	Not Supported	DCNTL,bit 6
Size Throttle Enable bit	Not Supported	DCNTL, bit 7
SCSI Interrupt Enable Register One -- 41h	Not Supported	SIEN1
Handshake Timer Expired	Not Supported	SIEN1,bit 0
General Purpose Timer Expired	Not Supported	SIEN1,bit 1
SCSI Interrupt Status Register Zero -- 42h	Not Supported	SIST0
SCSI Interrupt Status Register One -- 43h	Not Supported	SIST1
SCSI Wide Register -- 45h	Not Supported	SWIDE
Memory Access Control Register --46h	Not Supported	MACNTL
General Purpose Control Register -- 47h	Not Supported	GPCNTL

Note: The addresses refer to Little Endian byte orientation.

New Registers/Bits   (continued)

Registers/Bits	53C710	53C720
SCSI Time Register Zero -- 48h	Not Supported	STIME0
Programmable Select/Reselect Timer	Not Supported	STIME0,bits 3-0
Programmable Handshake Timer	Not Supported	STIME0,bits 7-4
SCSI Time Register One -- 49h	Not Supported	STIME1
Response ID Zero Register--4Ah	Not Supported	RESPID0
Response ID One Register -- 4B	Not Supported	RESPID1
SCSI Test Register Zero -- 4Ch	Not Supported	STEST0
SCSI Synchronous Offset Max. bit	Not Supported	STEST0,bit 0
SCSI Synchronous Offset Min. bit	Not Supported	STEST0,bit 1
Arbitration Priority Test bit	Not Supported	STEST0,bit 2
Selection Response Logic bit	Not Supported	STEST0,bit 3
SCSI Test Register One -- 4Dh	Not Supported	STEST1
SCSI Test Register Two -- 4Eh	Not Supported	STEST2
Extended REQ/ACK Filtering bit	Not Supported	STEST2,bit 1
Always Wide SCSI bit	Not Supported	STEST2,bit 2
SCSI Control Enable bit	Not Supported	STEST2,bit 7
SCSI Test Register Three -- 4Fh	Not Supported	STEST3
SCSI FIFO Test Write bit	Not Supported	STEST3,bit 0
Clear SCSI FIFO bit	Not Supported	STEST3,bit 1
Timer Test Mode bit	Not Supported	STEST3,bit 2
16-bit System	Not Supported	STEST3,bit 3
Disable Single Initiator Response	Not Supported	STEST3,bit 4
Halt SCSI Clock bit	Not Supported	STEST3,bit 5
SCSI FIFO Test Read bit	Not Supported	STEST3, bit 6
TolerANT Enable	CTEST0, bit 4	STEST3, bit 7
SCSI Input Data Latch bits 15-8	Not Supported	SIDL
SCSI Output Data Latch bits 15-8	Not Supported	SODL
SCSI Bus Data Lines bits 15-8	Not Supported	SBDL
General Purpose Scratch Pad Register.1 -- 5C-5Fh	Not Supported	SCRATCH1

Note: The addresses refer to Little Endian byte orientation.

Deleted Registers/Bits

Registers/Bits	53C710	53C720
Start SCSI Receive Operation bit	SCNTL1,bit 0	Not Supported
Start SCSI Send Operation bit	SCNTL1,bit 1	Not Supported
Enable Selection and Reselection	SCNTL1,bit 5	Not Supported
SCSI Destination ID bits 7-4	SDID bit 7-4	Not Supported
SCSI Chip ID bits 7-4	SCID bit 7-4	Not Supported
SCSI Offset Compare bit	CTEST2,bit 5	Not Supported
SCSI FIFO Write Enable bit	CTEST4,bit 3	Not Supported
DACK/ bit	CTEST5,bit 0	Not Supported
DREQ/ bit	CTEST5,bit 1	Not Supported
EOP bit	CTEST5,bit 2	Not Supported
Chip Test Register Seven	CTEST7	Not Supported

Note: The addresses refer to Little Endian byte orientation.

Moved Registers/Bits

Registers/Bits	53C710	53C720
SCSI Destination ID Register (SDID)	Address 02h	Address 06h
SCSI Interrupt Enable Register (SIEN)	Address 03h	Address 40h
SCSI Synchronous Transfer Period	SXFER,bits 6-4	SXFER,bit 7-5
Disable Halt on Parity Error or ATN bit	SXFER,bit 7	SCTRL1,bit 5
SCSI Output Data Latch Register (SODL)	Address 06h	Address 54-55h
SCSI Output Control Latch Register (SOCL)	Address 07h	Address 09h
SCSI Input Data Latch Register (SIDL)	Address 09h	Address 50-51h
SCSI Bus Data Line Register (SBDL)	Address 0Ah	Address 58-59h
Synchronous SCSI Clock Frequency	SBCL,bits 1-0	SCNTL3,bits 6-4
SCSI RST/ Received bit	SSTAT0,bit 1	SIST0,bit 1
Unexpected Disconnect bit	SSTAT0,bit 2	SIST0,bit 2
SCSI Gross Error bit	SSTAT0,bit 3	SIST0,bit 3
Function Complete bit	SSTAT0,bit 6	SIST0,bit 6
Phase Mismatch or ATN/ Active bit	SSTAT0,bit 7	SIST0,bit 7
SCSI Status Register One	SSTAT1	SSTAT0
SCSI Status Register Two	SSTAT2	SSTAT1
Chip Test Register Zero (CTEST0)	Address 14h	Address 18h
Data Transfer Direction bit	CTEST0,bit 0	CTEST2,bit 7
Chip Test Register One (CTEST1)	Address 15h	Address 19h
Chip Test Register Two (CTEST2)	Address 16h	Address 1Ah
SCSI FIFO Parity (bits 7:0) bit	CTEST2,bit 4	STEST1,bit 0
Chip Test Register Three (CTEST3)	Address 17h	Address 1Bh
Chip Test Register Four (CTEST4)	Address 18h	Address 21h
SCSI Loopback Enable bit	CTEST4,bit 4	STEST2,bit 4
SCSI High Impedance Mode bit	CTEST4,bit 5	STEST2,bit 3
Chip Test Register Five (CTEST5)	Address 19h	Address 22h
Reset SCSI Offset bit	CTEST5,bit 5	STEST2,bit 6
Chip Test Register Six (CTEST6)	Address 1Ah	Address 23h
Transfer Type bit	CTEST7,bit 1	CTEST0,bit 1
Even Parity - Host Bus bit	CTEST7,bit 2	CTEST0,bit 2
DMA FIFO Parity bit	CTEST7,bit 3	CTEST0,bit 3
Snoop Control bits 1-0	CTEST7,bits 6-5	CTEST0,bits 6-5
Cache Burst Disable bit	CTEST7,bit 7	CTEST0,bit 7
Chip Test Register Eight	CTEST8	CTEST3
Interrupt Status Register (ISTAT)	Address 21h	Address 14h
Longitudinal Parity Register	LCRC 23h	SLPAR 44h
Enable Low Level SCSI Mode	DCNTL,bit 3	STEST2,bit 0
Clock Frequency bits	DCNTL,bits 7-6	SCNTL3,bits 2-0

Note: The addresses refer to Little Endian byte orientation.

Start SCSI Transfer Bit

Function

The start SCSI transfer bit (SCNTL1, bit 0) has been added to initiate SCSI transfers. The 53C720 automatically sets the bit when a transfer operation is executed. It can be determined if the transfer is send or receive depending on the value written to the I/O bit in the SCSI Output Control Latch Register. The 53C710 possessed two bits to indicate that the chip was starting a send or receive operation.

Benefit

This bit is used for test purposes only and it is automatically set in low level mode and during SCRIPT execution.

Immediate Arbitration Bit

Function

Asserting the immediate arbitration bit (SCNTL1, bit 1) will prompt the 53C720 to arbitrate immediately after a disconnect has occurred.

Benefit

The immediate arbitration bit permits the 53C720 to participate in the next arbitration after a disconnect. This bit is useful for multi-threaded applications. The 53C710 was not capable of joining and winning arbitration immediately proceeding a disconnect.

Wide SCSI Receive Bit

Function

The wide SCSI receive bit (SCNTL2, bit 0) is asserted when the 53C720 detects a possible partial transfer at the end of a block move instruction. This residual byte is stored in the SCSI Wide Residue Data Register until the subsequent transfer. At this point the 53C720 can determine if the byte was "residual" data, valid data for a subsequent transfer, or overrun data. This byte will be combined with another byte during the subsequent receive operation if the data is valid.

Benefit

This bit allows the data within multiple block move instructions to be chained together. If a move instruction ends on a odd byte boundary the next move instruction will provide the additional byte so that a word transfer will occur.

Wide SCSI Send Bit

Function

The wide SCSI send bit (SCNTL2, bit 3) is asserted at the start of a wide SCSI send operation. If the transfer ends on an odd byte boundary, the bit will still be asserted at the end of the transfer. This indicates that the low order byte of the SCSI Output Data Latch Register contains the last byte from the current send operation. The low order byte will be combined with the high order byte of the subsequent send operation.

Benefit

This bit allows the data within multiple block move instructions to be chained together. If a move instruction ends on a odd byte boundary, the next move instruction will provide the high order byte so that a word transfer will occur.

Chained Mode Bit

Function

The chained mode bit (SCNTL2, bit 6) allows for chained block move instructions. The SCRIPT processor automatically sets the bit when a chained block move instruction is executed. The processor resets the bit when a regular block move SCRIPT instruction is executed.

Benefit

When this bit is set and a data transfer ends on an odd byte boundary the 53C720 will store the last byte in the SCSI Wide Residue Data Register during a receive operation or in the SCSI Output Data Latch Register during a send operation. This byte will be combined with the first byte from the subsequent transfer so that a wide transfer can be completed.

SCSI Disconnect Unexpected Bit

Function

The SCSI disconnect unexpected bit (SCNTL2, bit 7) should be asserted if the 53C720 is not expecting the SCSI bus to enter the bus free phase. The 53C720 automatically sets this bit when it is selected, reselected, performs a selection, or a reselection. The bit only has meaning in initiator mode.

Benefit

The 53C720 uses this bit to determine if the disconnect was expected. If the chip enters a bus free phase and the bit is set, an unexpected disconnect error will be generated in the SCSI Interrupt Status Register Zero.

Enable Wide SCSI Bit

Function

The wide SCSI bit (SCNTL3, bit 3) enables 16-bit data transfers over the SCSI bus. The bit is cleared for 8-Bit only data transfers.

Benefit

Wide SCSI operation allows the 53C720 to double its data transfer rate across the SCSI bus.

Selection and Reselection Control Bits

Function

The selection enable bit (SCID,bit 5) should be asserted when the 53C720 is required to respond as a target and the reselection enable bit (SCID, bit 6) should be asserted when the 53C720 is required to respond as an initiator. There are also status and interrupt bits indicating whether or not the 53C720 has been selected or reselected. The 53C710 only contains one bit indicating that the chip had been selected/reselected.

Benefit

> The selection or reselection enable bits allow the 53C720 to respond as either an initiator or a target device. For example, if only selection is enabled, the 53C720 cannot be reselected as an initiator. The status and interrupt bits can be polled so the appropriate target or initiator SCRIPT can be executed. These bits also make it possible to determine whether the 53C720 has been selected or reselected.

General Purpose Input/Output Bits

Function

> The general purpose bits (GPREG, bits 4-0) allow the 53C720 to detect the input signals of a connected device, or to enable attached ROM, RAM, or LEDs on a 53C720 board. The pins all have internal pull-ups.

Benefit

> The general purpose input feature can be used to sense the 53C720 chip ID or board configuration at power up, or . A Register to Register Move instruction may be used to move the sensed value into the appropriate register.

SCSI Selector ID Valid Bit and Encoded Destination SCSI ID Bits

Function

> SCSI selector valid ID bit (SSID, bit 7) will automatically be set when two SCSI ID's are detected on the bus during a bus-initiated selection or reselection. The encoded destination ID bits (SSID, bits 3-0) contain the ID of the initiator, selecting the 53C720, or the ID of the target, re-selecting the 53C720. The destination ID is valid when the selector ID is set.

Benefit:

> This bit enhances the development of multi-threaded I/O SCRIPTs. The 53C720 will, with greater ease, be able to support disconnects with the knowledge of the selector or re-selector's ID.

SCSI Data Parity One Signal

Function

> The SCSI data parity one signal (SSTAT2,bit 0) represents the parity on the high order byte lane. The parity signal is unlatched and may be changing at any time.

Benefit

> The SCSI Parity signal is used to detect parity errors on the upper byte lane during wide data transfer.

Last Disconnect Bit

Function

> The last disconnect bit (SSTAT2, bit 1) is used in conjunction with the connected bit in the SCSI Control Register One to determine if a disconnect and then a selection or reselection of the 53C720 has occurred. If the connected bit is asserted and the last disconnect bit is asserted, a disconnect has occurred. The bit is also asserted at chip reset indicating a disconnect state.

Benefit

> The last disconnect bit, in conjunction with the connected bit, notifies the 53C720 that a disconnect has transpired and that the 53C720 is again connected to a SCSI device. Every time the last disconnect bit is set after a CHMOV instruction has been executed, a disconnect has occurred since the prior CHMOV instruction.

Latched SCSI Data Parity One Signal

Function
> The latched SCSI data parity one signal (SSTAT2,bit 3) represents the odd parity of the high order byte in a 16-bit data transfer. The data is latched in the most significant byte of the SCSI Input Data Latch Register.

Benefit
> The SCSI parity signal is used to detect parity errors on the upper byte lane in 16-bit data transfers.

SCSI Output Data Latch Most Significant Byte Full

Function
> The SCSI output data latch most significant byte full bit (SSTAT2, bit 5) is asserted when the high order byte is written to the SCSI Output Data Latch Register (SODL) during a synchronous or an asynchronous SCSI send operation. The bit is deasserted when the byte is transferred from the SODL register to the SCSI bus during an asynchronous send, or to the internal SCSI Output Data Register during a synchronous send.

Benefit
> This bit is used to determine if the high order byte remains in the SCSI Output Data Latch Register when the chip halts a data transfer operation. This allows for restoration of data pointers after an interrupt.

SCSI Output Data Register Most Significant Byte Full

Function
> The SCSI output data register most significant byte full bit (SSTAT2, bit 6) is asserted when the high order byte is written to the SCSI Output Data Register during a synchronous SCSI send operation. The bit is deasserted when the byte is transferred to the SCSI bus during a synchronous send operation.

Benefit
> This bit is used to determine if the high order byte remains in the SCSI Output Data Register when the chip halts a data transfer operation. This allows for restoration of data pointers after an interrupt.

SCSI Input Data Latch Most Significant Byte Full

Function
> The SCSI input data latch register most significant byte full bit (SSTAT2, bit 7) is asserted when the high order byte is written to the SCSI Input Data Latch Register (SIDL) during an asynchronous SCSI receive operation. The bit is deasserted when the byte is transferred from the SIDL register to the DMA FIFO.

Benefit
> This bit is used to determine if there is a higher order byte in the SCSI Input Data Latch Register. This allows the SCRIPTs processor to finish transferring data into memory after an interrupt.

Interrupt On The Fly Bit

Function

The interrupt on the fly bit (ISTAT, bit 2) can be asserted by an interrupt instruction during SCRIPTS execution. SCRIPTS programs will not halt when the interrupt occurs. The interrupt must be serviced by reading the Interrupt Status Register only.

Benefit

This bit can be used to notify a service routine, running on the main processor, while the SCRIPT processor is still executing a SCRIPTs program.

Semaphore Bit

Function

The semaphore bit (ISTAT, bit 4) can be set by the SCRIPT processor using a SCRIPT register write. The bit may also be set by an external processor while the 53C720 is executing a SCRIPT.

Benefit

This bit enables the 53C720 to notify the external processor of a predefined condition while SCRIPTS are running. The processor may also notify the 53C720 of a predefined condition and the SCRIPT processor may take action while SCRIPTS are executing.

Generate Receive Parity for Pass Through Bit

Function

When this bit is set and the 53C720 is in parity pass through mode, parity received on the SCSI bus will not pass through the DMA FIFO. Parity will be generated as data enters the DMA FIFO, eliminating the possibility of bad SCSI parity passing through to the host bus.

Benefit

This bit isolates SCSI parity errors to the 53C720 instead on passing on bytes with bad parity to the system.

Host Parity Check Enable Bit

Function

Asserting the host parity check enable bit (CTEST4, bit 3) enables parity checking during slave write and DMA read execution. The system powers up with this bit disabled so that the 53C720 will function properly with systems that do not support parity.

Benefit

This bit may be enabled by the user for additional flexibility.

Shadow Register Test Mode

Function

Asserting the shadow register test mode bit (CTEST4, bit 4) allows the user to read the Shadowed Temporary Stack (TEMP) and Data Structure Address Registers (DSA).

Benefit

The assertion of this bit allows the user to retrieve data previously stored in these registers. These registers are "shadowed" because both are written over during a Memory to Memory Move operation. The TEMP and DSA registers contain the

base address, used for all table indirect calculations, and the instruction address pointer respectively.

SCSI Data Bus High Impedance Mode

Function
> Asserting the SCSI data bus high impedance mode bit (CTEST4, bit 5) places the SCSI data bus and parity lines in a high-impedance state.

Benefit
> This bit is used for functional or burn-in testing.

Enable Host Parity Error Interrupt

Function
> Asserting the host parity error interrupt bit (DIEN, bit 6) causes the 53C720 to generate a hardware interrupt when a parity error is detected at the host interface. If the bit is cleared the external IRQ/ signal will not be asserted.

Benefit
> The bit is used to notify the main processor that a parity error has occurred at the host interface.

Host Bus Width Equal to 16-Bits

Function
> When the host bus width equal to 16-bit (DCNTL, bit 3) is set the 53C720 host interface will convert to a 16-bit wide bus. (Note: data lines 31-16 must be tied to data lines 15-0). The default mode is 32 bits at the host interface.

Benefit
> This bit allows the 53C720 to operate with a 16-bit host bus.

Bus Mode Bit

Function
> The assertion of the bus mode bit (DCNTL, bit 6) gives the function code pins new meaning. The bit should only be asserted when the 53C720 is in 80386sx or 80386dx mode or is not used in a native 68030 or 68040 environment. FC0 remains unaffected and provides a data control signal. FC1 becomes reserved and FC2 becomes an input to allow preview of next address.

Benefit
> The assertion of this bit enables the 53C720 to interface, with greater ease, to the EISA bus.

Size Throttle Enable Bit

Function
> This bit causes the 53C720 to relinquish bus ownership every time the transfer size changes.

Benefit
> This allows the 53C720 to interface to host buses that do not allow size changes within a bus ownership.

Handshake-to-Handshake Timer Expired Interrupt Enable

Function

Assertion of the handshake-to-handshake timer expired interrupt enable bit (SIEN1, bit 0) prompts the 53C720 to generate a hardware interrupt when the handshake-to-handshake timer has expired. The time measured is the SCSI REQuest to REQuest or ACKnowledge to ACKnowledge period. The time-out period is programmed in the SCSI Timer Register ZERO, bits 7-4. Possible timeout values range from 100 microseconds to greater than 1.6 seconds. If the bit is cleared the external IRQ/ signal will not be asserted.

Benefit

The bit is used to notify the main processor that the timeout period has expired.

General Purpose Timer Expired Interrupt Enable

Function

Assertion of the general purpose timer expired interrupt enable bit (SIEN1, bit 1) prompts the 53C720 to generate a hardware interrupt when the general purpose timer has expired. The timeout period is programmed in the SCSI Timer Register One, bits 3-0. Possible timeout values range from 100 microseconds to greater than 1.6 seconds. If the bit is cleared the external IRQ/ signal will not be asserted.

Benefit

The bit is used to notify the main processor that the timeout period has expired.

SCSI Interrupt Status Zero Register

Function

The SCSI interrupt status zero register returns the status of the various interrupt conditions that can occur in the SCSI Interrupt Enable Register Zero.

Benefit

Each bit value asserted indicates that a corresponding interrupt condition has occurred. The bits have to be polled since the external IRQ/ signal will not be asserted.

SCSI Interrupt Status Register One

Function

The SCSI interrupt status one register returns the status of the various interrupt conditions that can occur in the SCSI Interrupt Enable Register One.

Benefit

Each bit value asserted indicates that a corresponding interrupt condition has occurred. The bits have to be polled since the external IRQ/ signal will not be asserted.

SCSI Wide Residue Data Register

Function

The SCSI wide residue data register contains a residual byte, the first byte of a subsequent transfer, or an overrun data byte.

Benefit

If an Ignore Wide Residue message is not received the wide residue data should become part of the next data transfer.

Response ID Zero and Response ID One Registers

Function

These registers contain the selection or reselection IDs that the chip responds to on the SCSI bus. Each bit represents one possible ID.

Benefit

These registers allow the 53C720 to respond to more than one ID. However, the chip can arbitrate with only one ID value in the SCID register.

Programmable Select/Reselect Timeout Timer

Function

A select/reselect timer (STIME0, bits 3-0) will, if activated, interrupt the 53C720 if the chip has not been selected or reselected within a user defined time period. The timer is programmable from 100 microseconds to greater than 1.6 seconds. The 53C710 used the Selection/Reselection Timer and the timeout period was fixed to be 250 msec.

Benefit

The select/reselect timer within the 53C720 is provided so that the system does not have to furnish it in software. The select/reselect timeout period required by the SCSI specification is 250 msec.

Programmable Handshake Timeout Timer

Function

A handshake timer (STIME0 bits 7-4) will, if activated, interrupt the 53C720 if the chip has not monitored a transfer within a predefined time period. The time measured is the SCSI REQuest to REQuest or ACKnowledge to ACKnowledge period. The timer is programmable from 100 microseconds to greater than 1.6 seconds. The 53C710 used the Selection/Reselection Timer and the timeout period was fixed to be 250 msec.

Benefit

The handshake timer is provided so that the system does not have to furnish it. The interrupt will inform the 53C720 that the connected SCSI device is not responding.

Programmable General Purpose Timer

Function

A general purpose timer (STIME1, bits 3-0) will, if activated, interrupt the 53C720 once a predefined time period has expired. The timer is programmable from 100 microseconds to 1.6 seconds.

Benefit

The general purpose timer may be used to limit the time the 53C720 spends on or off the bus. Once the interrupt occurs, after the predefined time period has elapsed, a SCRIPT Disconnect instruction may be executed to free the bus or a Select instruction may be issued to get back on the bus.

SCSI Synchronous Offset Maximum Bit

Function

The SCSI synchronous offset maximum bit (STEST0, bit 0) indicates that the current synchronous SCSI REQ/ACK offset is the maximum specified by bits 3-0

in the SCSI Transfer register. This bit is not latched and may change at any time. The 53C710 incorporated this function in the CTEST2 register, bit 5.

Benefit

This bit is used in low level synchronous SCSI operations. When this bit is set the 53C720, as a target, is waiting for the initiator to ACKnowledge the data transfers. If the 52C720 is an initiator then the target has sent the offset number of REQuests.

SCSI Synchronous Offset Zero Bit

Function

The SCSI synchronous offset zero bit (STEST0, bit 1) indicates that the current synchronous SCSI REQ/ACK offset is zero. This bit is not latched and may change at any time. The 53C710 incorporated this function in the CTEST2 register, bit 5.

Benefit

This bit is used in low level synchronous SCSI operations. When this bit is set the 53C720, as an initiator, is waiting for the target to REQuest data transfers. If the 53C720 is a target then the initiator has sent the offset number of ACKnowledges

Arbitration Priority Encoder Test Bit

Function

The arbitration priority encoder test bit (STEST0, bit 2) will always be asserted when the 53C720 exhibits the highest priority ID asserted on the SCSI bus during arbitration.

Benefit

This bit is primarily used for chip level testing but it may be used during low level mode to determine if the 53C720 has won arbitration.

Selection Response Logic Bit

Function

The selection response logic bit (STEST0, bit 3) is asserted when the 53C720 is ready to be selected or reselected. This does not take into account the bus settle delay of 400 ns.

Benefit

This bit is used for functional test and fault purposes.

Extended REQ/ACK Filtering Bit

Function

When the extended REQ/ACK filtering bit (STEST2, bit 1) is asserted, additional filtering on the deasserting edge of the REQ/ and ACK/ signals will be provided. The filter should not be used during fast SCSI transfers (greater than 5 Mbytes/sec).

Benefit

The assertion of this bit will filter out glitches which may be interpreted by the 53C720 as assertions of the REQ/ and ACK/ signals.

Always Wide SCSI Bit

Function

When the always wide SCSI bit (STEST2, bit 2) is asserted, all SCSI information transfers are executed in 16-bit mode. In other words, all the phases supported by

the SCRIPT language (message, data, instruction and status) are performed in 16-bit mode.

Benefit

This bit should normally be deasserted since 16-bit wide message, instruction and status phases are not supported by the SCSI specifications. This bit is not guaranteed to function properly with future SCSI wide specifications.

SCSI Control Enable Bit

Function

When the SCSI control enable bit (STEST2, bit 7) is asserted, all the SCSI control and data lines are driven regardless of whether the 53C720 is in target or initiator mode.

Benefit

This bit is primarily used for burn-in testing. This bit should not be set during normal operations, since contention on the SCSI bus may otherwise occur.

SCSI FIFO Test Read and Write bits

Function

These bits place the SCSI core into a test mode in which the SCSI FIFO can be easily written and read.

Benefit

These bits allow additional testing and system diagnostics.

SCSI FIFO Test Mode Bit

Function

Asserting the SCSI FIFO test mode bit (STEST3, bit 0) places the 53C720 in a test mode in which the FIFO can easily be read and written.

Benefit

This bit is asserted in order to test the functionality of the FIFO.

Clear SCSI FIFO Bit

Function

Asserting the clear SCSI FIFO bit (STEST3, bit 1) allows the user to clear the flags indicating that the FIFO is full.

Benefit

This bit allows the user to clear the FIFO.

Timer Test Mode Bit

Function

Asserting the timer test mode bit (STEST3 bit 2) allows the user to test the 53C720 timers. Setting the bit starts the selection timeout, general purpose, and handshake to handshake timers.

Benefit

This bit is used to facilitate functional testing and increase fault coverage.

16-Bit System

Function

Assertion of the 16-bit system bit (STEST3, bit 3) allows the 53C720 to consider 16-bit selection attempts. If parity checking is enabled parity will be checked on the high and low order byte lanes.

Benefit

Wide selection attempts are considered whereas 8-Bit only selection attempts may be ignored due to bad parity since the high order byte lane is not driven.

Disable Single Initiator Response Bit

Function

When the disable single initiator response bit (STEST3, bit 4) is asserted, the 53C720 will ignore all bus- initiated selection attempts which employ the single initiator option of SCSI-1.

Benefit

This bit may be asserted in SCSI-2 systems so that a single bit error on the SCSI bus will not be interpreted as a single initiator response by the 53C720.

Halt SCSI Clock Bit

Function

When the halt SCSI clock bit (STEST3, bit 5) is asserted, the SCSI clock will stop in a glitchless manner. Deasserting the bit will start the clock without glitches.

Benefit

This bit may be used for test purposes or to lower I_{DD} during a power down mode. (SCSI registers must be re-initialized upon power-up).

SCSI Input Data Latch Bits

Function

Bits 15 through 8 in the SCSI Input Data Latch Register were added to accommodate the 53C720's wide SCSI data transfer capability. The is utilized during asynchronous data receive.

Benefit

The addition of these bits makes the 53C720 capable of concurrently receiving 16 bits of data.

SCSI Output Data Latch Bits

Function

Bits 15 through 8 in the SCSI Output Data Latch Register were added to accommodate the 53C720's wide SCSI data transfer capability. The register is utilized during synchronous and asynchronous data send.

Benefit

The addition of these bits allows the 53C720 to send 16 bits of data at a time.

SCSI Bus Data Lines Bits

Function

Bits 15 through 8 in the SCSI Bus Data Lines Register were added to allow the extra data bits on the SCSI bus to be read. This data is not latched and may be changing while being read.

Benefit

The addition of these bits makes it possible to look at all the SCSI data lines at once.

SCRATCH Register One

Function

The SCRATCH register is a second general purpose user definable 32-bit read/write register.

Benefit

The SCRATCH register is used as a general purpose holding register.

NCR

This application note describes a suggested interface between the NCR 53C720 and the Motorola 68030. The purpose of this application note is to provide general guidance for designers who wish to connect the NCR 53C720 with the 68030 processor. This interface has not been tested, so the designer should perform a thorough design analysis before implementing this interface. The text of this application note describes the components and connection required. The suggested interface is illustrated in Figure 1.

Host Interface

The Bus Mode pins of the NCR 53C720, BS(2-0), are all tied high through a 10 KΩ resistor, causing the chip to operate in Bus Mode 1, the 68030 Big Endian mode. For more information on the operating modes of the NCR 53C720, refer to the *NCR 53C720 Data Manual*.

Circuit Components

The 74LS148 is an 8-line to 3-line priority encoder that is used to enable up to seven interrupts, in addition to the one already coming from the NCR 53C720. The NCR 53C720 SCRIPTS autostart pin can be tied low so that the NCR 53C720 will automatically fetch and execute SCRIPTS at power-up. The SCSI clock is connected to a 50 MHz oscillator, so the NCR 53C720 can support fast SCSI.

The interface uses one PAL (16V8), to decode the NCR 53C720 addresses and select the chip by asserting the CS/ signal. The address selecting the chip is 58XX XXXX hex. This address is defined as the 68030 Direct Slot expansion on the Macintosh SE board. Please refer to the attached ABEL listing.

Tie bi-directional tri-state outputs high through 10 KΩ pull-up resistors, if there is a possibility that these signals may temporarily leave an input in the high impedance state. Unused input signals must be held at a valid logic level. In this circuit, all unused inputs are tied high to minimize current draw.

The NCR 53C720 has separate ground planes within the internal logic and the output drivers. Decoupling capacitors are recommended for optimum noise isolation. Use 0.1 μF decoupling capacitors between the following ground and power pins on the NCR 53C720:

V_{SS} Ground Pin	V_{DD} Power Pin
3	204
16	13
22	27
44	56
71	66
87	82
100	97
119	122
190	186

SCSI Interface

Alternative 2 single ended termination is recommended when implementing fast SCSI (>5 MB/s). The upper half of the circuit on page 5 shows the Alternative 2 termination. This type of circuit provides better signal quality and a more stable termpower supply. A voltage regulator (Vout = 2.84V) and 110 _ pull-up resistors are employed. R55 and R56 are 121 _ and 154 _ respectively. The resistors all have a tolerance of 1%. The capacitors have the following values C51 = 4.7 μF, C52 and C53 = 1.0 μF, C54 = 22 μF and C55 = 0.01 μF. Both diodes are Schottky and the fuse is 1.5 A. Refer to the 53C720 Data Manual and the SCSI specification for more information on Alternative 2 termination. The Reset signal on the SCSI bus may be connected to a switch so the bus can be reset manually.

ABEL Listing

```
Module NCR53C720
title 'Address decoder for 53C720 board'

u12 device 'P16v8r';

VCC, GND, BCLK     pin 20, 10, 1;
A31, A30, A29, A28, A27, A26, A25, A24, A23, A22        pin 2, 3, 4, 5, 6, 7, 8, 15,
16, 17;
AS, MASTER, STERM, CS, SLACK, DSACK0, DSACK1     pin 9, 11, 12, 13, 14, 181, 19;

ON, OFF      = 1, 0;
C, X, Z      =.C., .X., .Z.;
ADDR= [A31, A30, A29, A28, A27, A26, A25, A24, A23, A22];   "hex 58 is the address
"of the 68030 direct expansion slot on the Macintosh SE/30.

equations

!CA = (SLACK & !AS & (ADDR == ^h58));
!STERM := (STERM & !AS & (!DSACK0 # !DSACK1));
DSACK0 = SLACK;
DSACK0.OE = (!AS & (ADDR == ^h58));
DSACK1 = SLACK;
DSACK1 = SLACK;
DSACK1.OE = (!AS & (ADDR == ^h58));

test_vectors ([ADDR, AS, SLACK] -> [CS])
[[X, X, X, X, X, X, X, X, X, X], 1, X] -> [1];
[[X, X, X, X, X, X, X, X, X, X], X, 0] -> [1];
[^h50, 0, 1] -> [1];
[^h58, 0, 1] -> [0];
^h60, 0, 1] -> [1];

test_vectors ([AS, ADDR, SLACK] -> {DSACK), DSACK1])
[1, [X, X, X, X, X, X, X, X, X, X], X] -> [Z, Z];
[0, ^h58, 1] -> [1, 1];
[0, ^h58, 0] -> [0, 0];
[0, ^h50, X] -> [Z, Z];
[0, ^h60, X] -> [Z, Z];

test_vectors ([BCLK, AS, DSACK0, DSACK1, MASTER] -> [STERM])
[C, X, X, X, 1] -> [Z];
[C, 1, X, X, 0] -> [1];
[C, 0, 1, 1, 0] -> [1];
[C, 0, 1, 0, 0] -> [0];
[C, 0, 1, 0, 0] -> [1];
[C, 0, 0, 1, 0] -> [0];
[C, 0, 1, 0, 0] -> [1];
[C, 0, 0, 0, 0] -> [0];
[C, 0, 1, 0, 0] -> [1];

end NCR53C720
```

Figure 1. NCR 53C720 to 68030 Interface

Figure 1. NCR 53C720 to 68030 Interface
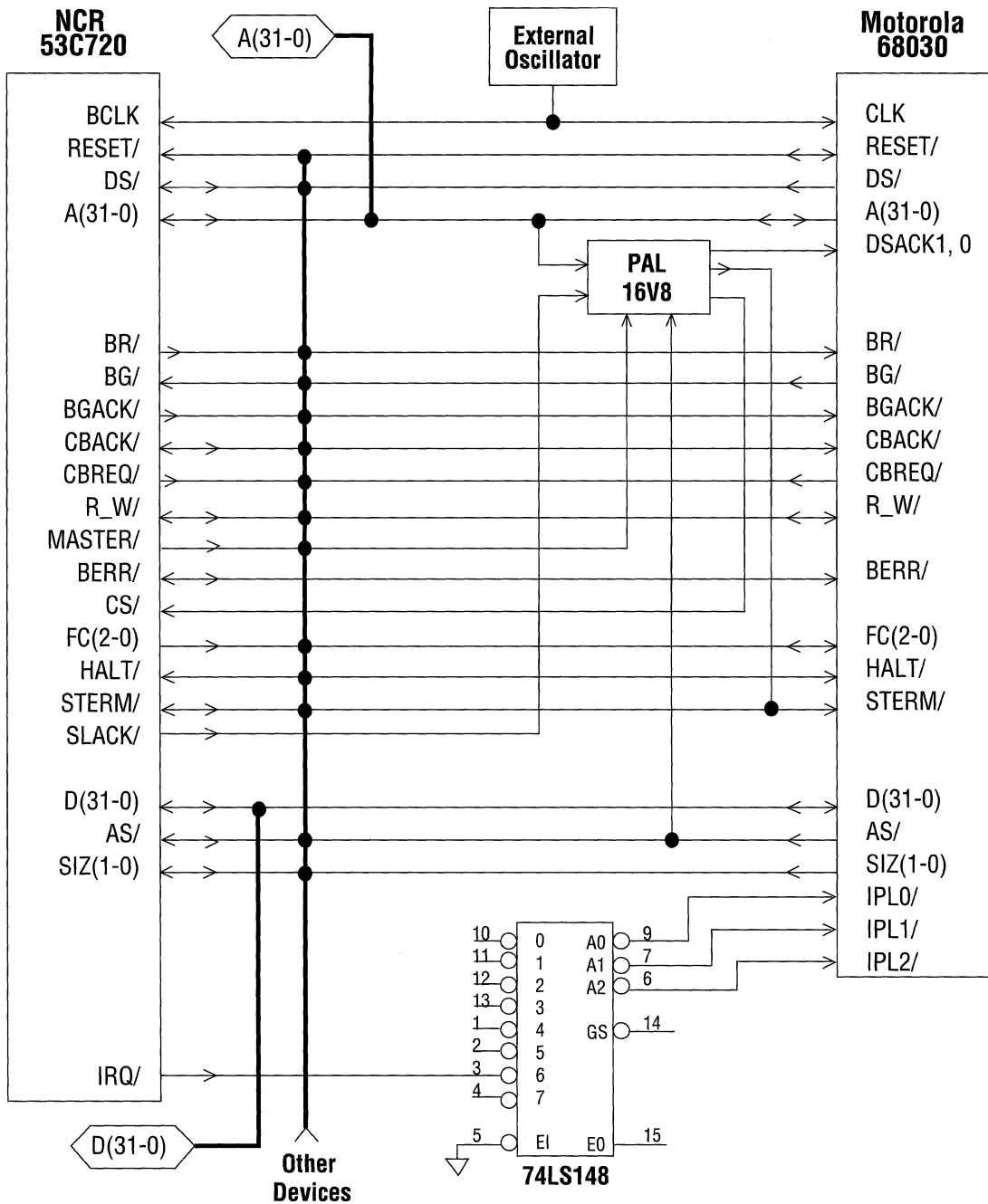
Notes:

1. *The following NCR 53C720 signals are pulled high with resistors: DP3/ABORT, DP2, DP1, BS2, BS1, BS0, BOFF/.*

2. *The NCR 53C720 cannot supply a vector number for an IACK cycle. Either additional hardware must be added or AUTOVECTORED interrupts should be used. The AVEC/ signal must be generated by glue logic if AUTOVECTORED interrupts are used.*

3. *If polled interrupts are used, the IPL2-0 lines and the 74LS148 are not used.*

SCSI	No. 836
Engineering	NCR 53C720 to 80386SX Interface
Notes	Rev. 2.0, August 1993

This application note provides a suggested interface between the NCR 53C720 and the Intel 80386SX. The purpose of this application note is to guide people in their own designs. Please note that the interface has not been tested, and the designer should perform a thorough design analysis before implementing this interface.

Host Interface

The interface to the Intel 80386SX host processor, requires the NCR 53C720 to operate in Bus Mode 3, the 80386SX little endian mode. To select this mode, tie the 53C720 Bus Mode Select pin BS0 high through a 10 KΩ resistor and tie BS2-BS1 to ground. For more information on the host bus modes supported by the NCR 53C720, refer to the *NCR 53C720 Data Manual*.

The NCR 53C720 –Intel 80386SX interface is illustrated in Figure 1. It uses an MC88915, a low skew CMOS PLL clock driver, to multiply the input clock by two. This 2x clock output drives the Intel 80386SX. The four General Purpose Input pins of the NCR 53C720 are connected to jumpers so that the chip ID can be read in during boot up. The NCR 53C720 SCRIPTS Autostart pin is tied low so the NCR 53C720 will automatically fetch and execute SCRIPTS at power-up. The SCSI clock is connected to a 50 MHz oscillator so the NCR 53C720 can support fast SCSI. TEA/ (Transfer Error Acknowledge) and TBI/ (Transfer Burst Inhibit) are tied resistively high and low through a 10KΩ resistor respectively. Bus retries and cache bursts cannot be performed.

When interfacing the NCR 53C720 to the 80386SX, the following lines should be pulled high with resistors:

NCR 53C720	80386SX
A31-A24, PA/, DP3_ABRT/, BB/, BOFF/, BS0/, TEA/, DP2-0, AUTO/, DS_DLE/	NA/, LOCK/

These lines should be tied to ground:

NCR 53C720	80386SX
BS2, BS1	n/a

The NCR 53C720 Transfer Burst Inhibit pin should be tied low with resistors.

PALs

The interface employs two pals. Their logical functions are described below.

Address decode logic: A PAL (22V10) is used to decode the NCR 53C720 addresses and select the chip by asserting the Chip Select (CS/) signal. The address selecting the chip is D000 0XXX hex. This address is defined as the cartridge ROM area in the AT system memory map. Please refer to the attached ABEL listing.

80386SX/NCR 53C720 glue logic: A PAL (16V8) is used to generate the Intel Hold and the Memory-I/O signals. In addition, the NCR 53C720 Hold Acknowledge and Reset signals are inverted. Please refer to the attached ABEL listing.

Tie bi-directional tri-state outputs high through 10 KΩ pull-up resistors if there is a possibility that these signals will temporarily leave an input in the high impedance state. Unused input signals must be held at a valid logic level. In this circuit, all unused inputs are tied high to minimize current draw.

The NCR 53C720 has separate ground planes within the internal logic and the output drivers. Decoupling capacitors are recommended for optimum noise isolation. Use 0.1 µF decoupling capacitors between the following ground and power pins on the NCR 53C720:

V_{SS} Ground Pin	V_{DD} Power Pin
3	204
16	13
22	27
44	56
71	66
87	82
100	97
119	122
190	186

The upper 16 data lines (D31-16) and the lower 16 data lines (D15-0) must be tied together. Bit 3 (BW16) in the DCNTL register (38h) must be set during the initialization so that the NCR 53C720 will operate in 16-bit wide mode. The IRQ/ output from the NCR 53C720 is not connected in this interface, since polled interrupts are used. If hardware IRQ/ interrupts are to be used, then additional glue logic may be required between the NCR 53C720 and the 80386SX.

SCSI Interface

Alternative Two single ended termination is highly recommended, especially when implementing fast SCSI (>5 MB/s). This type of circuit provides better signal quality and a more stable term-power supply. For more information on Alternative Two transition, refer to the SCSI specification.

ABEL Listing

```
module NCR53C720;
title 'Address decoder for 53C720 board'

U12 device 'P22v10';

VCC, GND                                                    pin 24, 12
A23, A22, A21, A20, A19, A18, A17, A16, A15     pin 2, 3, 4, 5, 6, 7, 8, 9, 10;
A14, A13, A12, A11, A10, A9, A8, A7         pin 23, 22, 21, 20, 19, 18, 17, 16;
ADS, READYO, CS                                         pin 11, 15, 14;

X                                                                                   =.X.;
ADDR = [A23, A22, A21, A20, A19, A18, A17, A16, A15, A14, A12, A12, A11, A10, A9, A8, A7];

equations

!CS = (READYO & !ADS & (ADDR == ^hD000)); "E000 ROM CARTRIDGE AREA

test_vectors ([ADDR, ADS, READYO] -> [CS])
[[X,X,X,X,X,X,X,X,X,X,X,X,X,X,X,X,X],1,X] -> [1];
[[X,X,X,X,X,X,X,X,X,X,X,X,X,X,X,X,X],X,0] -> [1];
[^hCfff, 0, 1] -> [1];
[^hD000, 0, 1] -> [0];
[^hD001, 0, 1] -> [1];

end NCR53C720
```

ABEL Listing

```
        module NCR 53C720
title'53C720 signals -> 80386SX signals'

u23 device 'P16v8r':

VCC, GND, BCLK                                              pin 20, 10, 1;
INTELHLDA, NCRMASTER, NCRHOLD, NCRTT0, NCRFETCH, INTELRESET   pin 2, 3, 4, 5, 6, 7;
NCRHLDAI, INTELHOLD, NCRM_IO, NCRRESET                      pin 19, 18, 17, 16;

ON,OFF                                                          = 1, 0;
X, Z                                                         =.X., .Z.;

equations

INTELHOLD = !(!NCRHOLD & !NCRMASTER);
NCRHLDAI = !INTELHLDA;
NCRRESET = !INTELRESET;
NCRM_IO.OE = !NCRMASTER;

truth_table ([NCRFETCH, NCRTT0] -> [NCRM_IO])
"INPUT         OUTPUT
"NCRFETCH NCRTT0
[0,0] -> [1];"Fetch-low=memory, TT0-low=i/o -> memory access
[0,1] -> [1];"Fetch-low=memory, TT0-high=memory -> memory access
[1,0] -> [0];"Fetch-high=i/o, TT0-low=i/o -> i/o access
[1,1] -> [1];"Fetch-high=io, TT0-high=memory -> memory access

test_vectors ([NCRHOLD, NCRMASTER] -> [INTELHOLD])
[ON,OFF] -> [ON];
[OFF, ON] -> [ON];
[ON, ON} -> [ON];
[OFF, OFF] -> [OFF];

test_vectors ([INTELHLDA] -> [NCRHLDAI])
[OFF] -> [ON];
[ON] -> [OFF];

test_vectors ([NCRFETCH, NCRTT0, NCRMASTER] -> [NCRM_IO])
[X,X,1] -> [Z];

test_vectors ([INTELRESET] -> [NCRRESET])
[OFF] -> [ON];
[ON] -> [OFF];

end NCR53C720
```
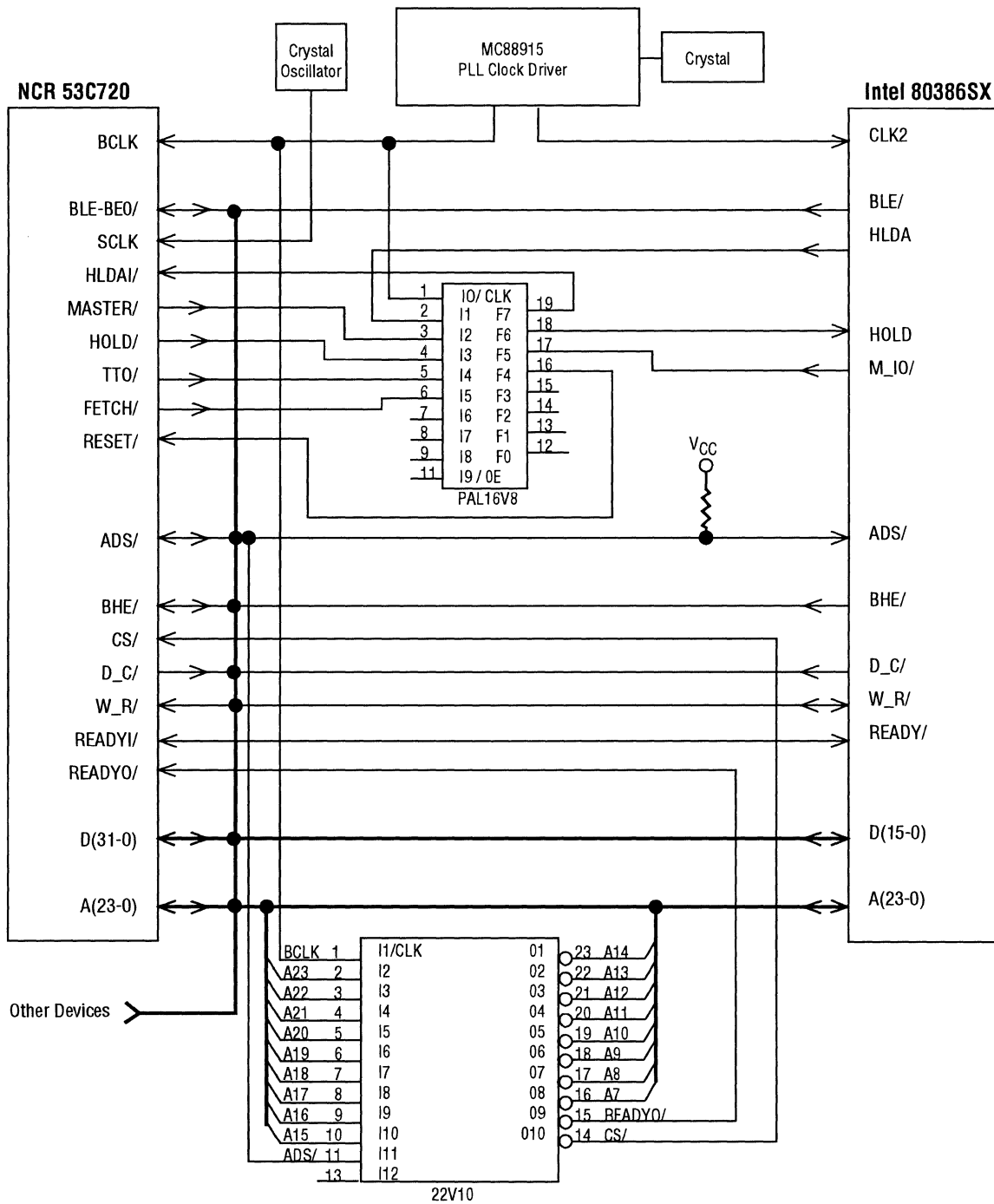
Figure 1. NCR 53C720 to 80386SX Interface

NCR

SCSI	NO. 837
ENGINEERING	NCR 53C710/20 BERR/_TEA/ pin function
NOTES	Rev. 1.0 11/91

Introduction

This application note describes the function of the BERR/_TEA/ pin on the NCR 53C710/20 SCSI I/O Processor. It applies to the following part numbers: 609-3400527, 609-3400654, and 609-3400669.

Functionality of BERR/_TEA/ during Bus Master Mode

In Bus Master Mode, BERR/_TEA/ is used in conjunction with TA/ to indicate to the NCR 53C710/20 that one of the following conditions has occurred:

NCR 53C710 or 53C720 in bus modes 1, 2, 3, or 4

TEA/	TA/	CONDITION
1	1	Execute a Wait State
1	0	Normal Cycle Acknowledge
0	1	Bus Error Condition Has Occurred
0	0	Retry the Current Cycle After Relinquishing the Bus *

* In 040 Mode the chip will attempt a bus retry operation if TEA/ is asserted in conjunction with TA/ .

* In 030 Mode the chip will attempt a bus retry operation only if BERR/ is asserted in conjunction with HALT/ .

Functionality of BERR/_TEA/ during Slave Mode

In Bus Slave Mode the 53C710/20 will respond to requests from an external master in one of the following ways:

NCR 53C710

TEA/	SLACK/	TA/ *	CONDITION
1	1	1	Requests the Bus Master to Insert a Wait State
1	0	0	Normal Cycle Acknowledge
0	1	1	Access Exception Has Occurred
0	0	0	Will Not Occur

* TA/ Will not be asserted during slave cycles unless the enable ack bit in the DCNTL register is set.

Address exceptions are as follows:

040 Mode:	any misaligned 2-byte transfer (A0 = 1) any misaligned longword (A1-A0 not equal to 00) any 2-byte transfer in Big Endian mode
030 Mode:	All of the cases mentioned above plus any 3-byte transfer.

NCR 53C720

TEA/	SLACK/	TA/ *	CONDITION
1	1	1	Requests the Bus Master to Insert a Wait State
1	0	0	Normal Cycle Acknowledge
0	1	1	Access Exception Has Occurred
0	0	0	Will Not Occur

* TA/ Will not be asserted during slave cycles unless the enable ack bit in the DCNTL register is set.

Address exceptions are as follows:

040 Mode:	any misaligned 2-byte transfer (A0 = 1) any misaligned longword (A1-A0 not equal to 00) any 2-byte transfer in Big Endian mode
030 Mode:	All of the cases mentioned above plus any 3 byte transfer.
386SX/DX Mode:	No bus exceptions will occur and the TEA/ pin will never be asserted. One, Two, Three, and Four byte operations are allowed.

![NCR logo]

SCSI	No. 840
Engineering	53C710, 53C720 False Bus Request
Notes	Rev. 1.0 4/92

This Engineering note provides information on how to identify a false bus request, and how to create a Bus Request signal that is always valid. A false bus request is defined as the condition when the 53C7X0 requests the host bus but does not use it. The information in this note is for designs that cannot accommodate false host bus requests. If your system can handle the false bus request condition, disregard this note. The information in this Engineering Note applies to 53C710 and 53C720 products with the following part numbers: 609-3400654, 609-3400527, 609-3400546, and 609-3400669.

The NCR 53C7X0 will periodically assert the Bus Request (BR/) signal and simultaneously receive a SCSI interrupt. When this happens, the chip will wait for the Bus Grant (BG/) signal to complete the normal bus arbitration handshake. The chip no longer wants host bus access - after receiving BG/ the chip will take bus ownership for one BCLK, deassert the BR/, MASTER/ and all control lines (after the one BCLK), but will not assert Transfer Start (TS/), the signal that indicates a bus cycle is starting. The chip will return the DMA bus to a Bus Free state, allowing other bus masters to take control. The chip will generate the SCSI interrupt, which the system should service, and then continue with its normal operation. The attached timing diagrams show a normal host bus access (Figure 1) and a false bus request (Figure 2).

To differentiate between a true request and a false request the SC0 (Snoop Control 0) pin can be used on the 53C710 or 53C720. When bit 0 of CTEST8 is set, Bus Snooping is enabled and SC0 is a look-ahead copy of the internal bus request signal. As Figure 2 shows, when snooping is enabled and a false bus request occurs the SC0 pin will NOT be asserted at the time BR/ is asserted.

If the processor is unable to handle a false bus request, such as when it is looking for a TS/ signal, external logic may be required. To create a bus request that is always valid, BR/ can be inverted and then NANDED with the SC0 signal. Bus snooping must be enabled. Because the BR/ signal is an interlocked handshake with BG/, logic must be implemented to create a BG/ signal that will complete the handshake in case of a false bus request. The bus will then return to a Bus Free state, allowing normal arbitration by other devices.

This logic must do four things:

  1. Logically filter out the false bus request seen by the system.
  2. Assert a BG/ signal to the 53C7X0.
  3. Ensure that the signals driven during the one BCLK ownership do not
     interfere with normal system operations.
  4. Deassert the BG/. (The BG/ signal need only be 1 BCLK wide.)

Note: When implementing the logic to create an "always valid" bus request, it is essential that the SC0 not be delayed. Therefore, the BR/ signal must be the signal of choice to be inverted and then "NANDED" with the SC0 signal (See Figure 3).
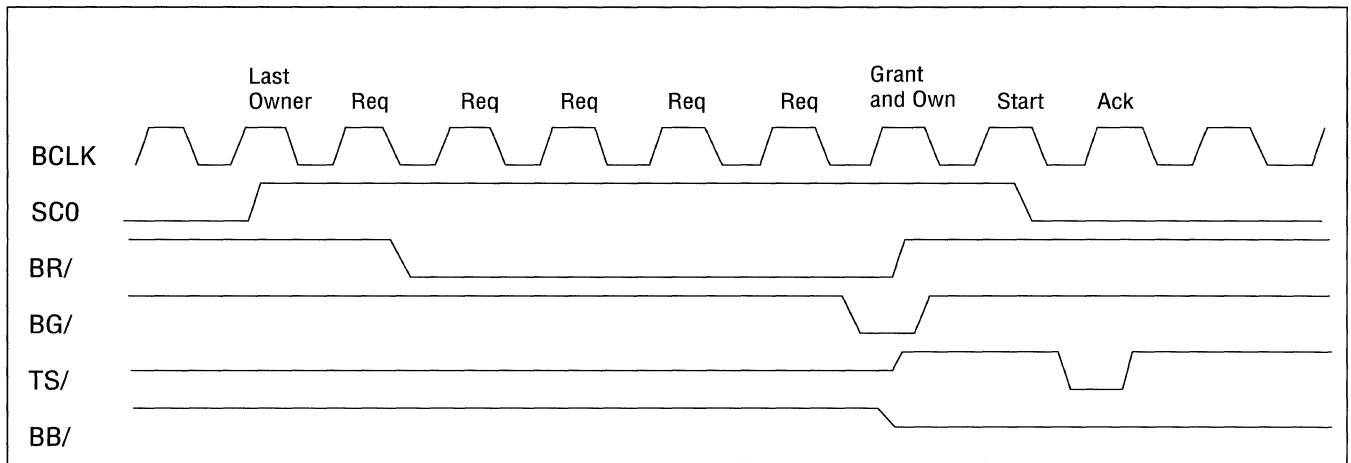
Figure 1. Normal Bus Request
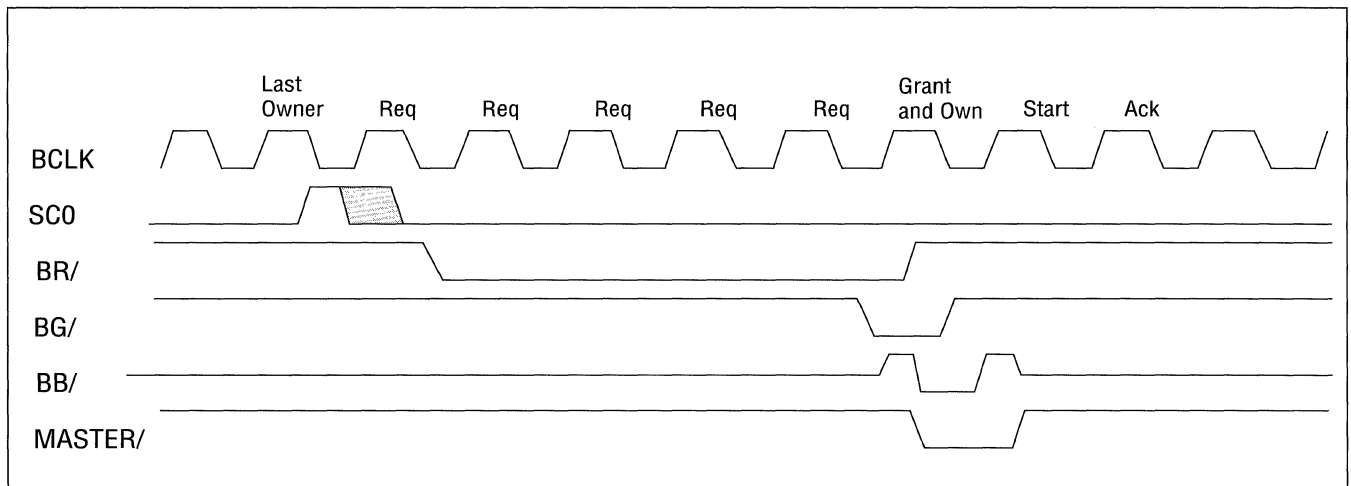
Figure 2. False Bus Request
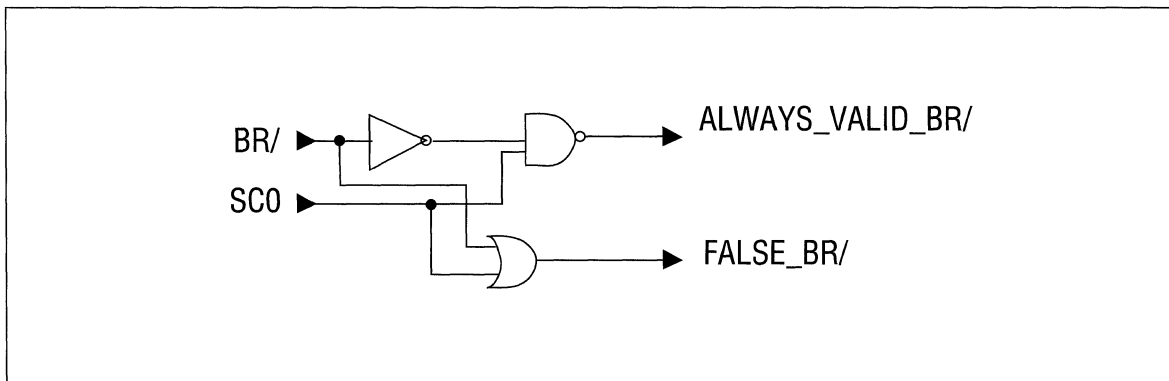
Figure 3. Circuit to Create "Always Valid" Bus Request

SCSI
Engineering
Notes

No. 848
NCR 53C720 to 80486 Interface
Rev. 1.0 , 2/93

This application note defines a logical interface between the NCR 53C720 and the Intel 80486 microprocessor. It contains guidelines for designing systems that use the 53C720/80486 interface. This application note concentrates only on interfacing the 53C720 to the 80486 local bus. Information on interfacing the NCR 53C720 to the SCSI bus can be acquired from NCR SCSI Engineering Notes 833 or 836. The pound symbol (#) is used with Intel signal names to indicate the active state occurs when the signal is at a low voltage; active low signals in the NCR 53C720 are indicated by a slash (/) following the signal name.

NOTE: this interface has not been tested and the designer should perform a thorough design analysis before implementing this interface.

Host Interface

The 53C720 bus mode pins (BS(2-0)) are all tied to ground, enabling the chip to operate in Bus Mode 4, 80386 Little Endian mode; this bus mode should be used for interfacing with the 80486. The RESET signal must be inverted before being presented to the 53C720. Two signals from the 53C720, HOLD/ and MASTER/, are NANDed to generate the 80486 Bus Hold Request input, HOLD. The 80486 hold acknowledge signal, HLDA, must be inverted before connecting to the 53C720 HLDAI/ pin. Since bus retries are not allowed on the 80486 local bus, the 53C720 TEA/ pin should tied to V_{DD} through a 1 KΩ resistor. If the 53C720 BB/ pin is not used, it should be tied to V_{DD} through a 1 KΩ resistor, so the 53C720 will operate properly during bus arbitration.

Slave cycles

The 80486 performs a slave read/write access to the 53C720 using a four wait state cycle. System logic must perform the address decode for the 53C720 and select the chip by asserting the Chip Select (CS/) signal. CS/ must meet timings t_3 and t_4 (CS/ setup to and hold from BCLK high after ADS/) specified in the Bus Mode 4 Slave Read/Write Cycle section in Chapter Six of the NCR 53C720 *Data Manual*. The first 80486 access to the 53C720 should set the EA bit (bit 5) in the DCNTL register. Setting the EA bit will cause the READYI/ pin to become bi-directional; in other words, the 53C720 will generate READYI/ during slave accesses. This signal will be connected to the 80486 RDY# signal, indicating that a burst cycle to the 53C720 cannot be performed. If the designer decides not to set the EA bit in DCNTL, then system logic must monitor the 53C720 READYO/ signal in order to generate READYI/ to the 53C720 and RDY# to the 80486. The 80486 BLAST# signal can be ignored, since the 53C720 cannot burst during slave accesses.

Master cycles

The interface logic must generate the BLAST# signal, to indicate to the memory system that the next time RDY# or BRDY# is returned, the data cycle transfer will terminate. The interface logic should generate two burst last signals then logically AND to generate the system BLAST# signal. The first burst last signal, NON_CACHE_BLAST#, will be for the basic two clock data cycle. This signal is implemented using a clocked J-K flip-flop. The J, K and NON_CACHE_BLAST# equations are as follows:

```
J = ! ( ! CBREQ/ + ADS/ + MASTER/)

K = ! RDY#

NON_CACHE_BLAST# = ! Q
```

The signals CBREQ/, ADS/ and MASTER/ are outputs from the 53C720. The signal RDY# is an output from the memory system.

For the 53C720 to perform cache line bursts as illustrated in the NCR 53C720 *Data Manual*, in register CTEST0, bit 0 (C386E) must be set and bit 7 (CDIS) must be cleared. The second burst last signal, CACHE_BLAST#, is generated by implementing a four-state grey code state machine with the state diagram in Figure 1.

Figure 1. State Diagram
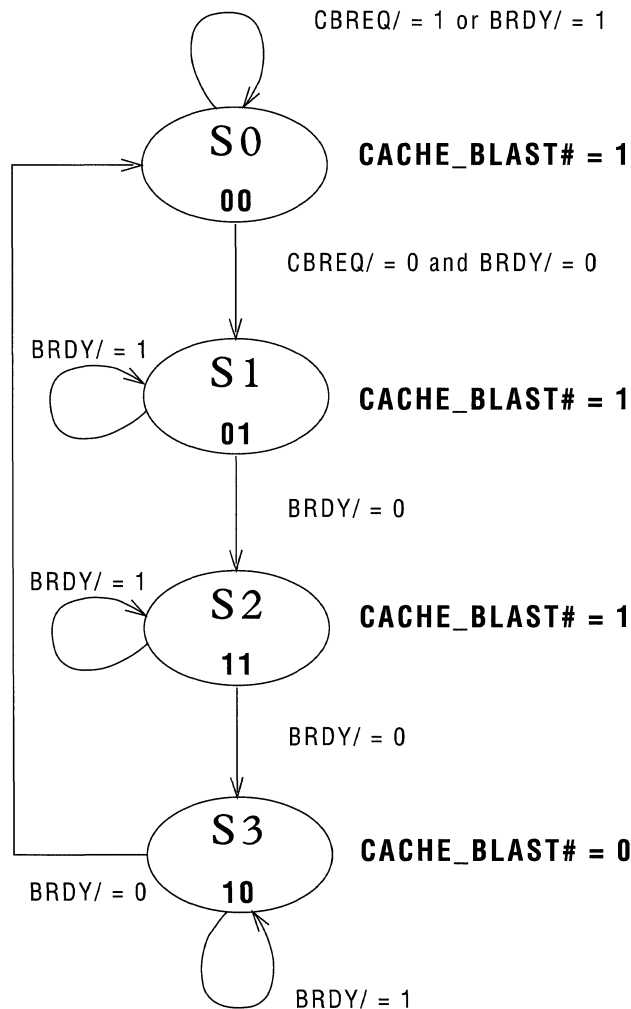
The next state equations for the state machine are given below. Qb is the most significant bit.

```
Qb(n+1) = ((Qa & ! BRDY#) + (Qb & BRDY#))

Qa(n+1) = ((Qa & BRDY#) + (! Qb & Qa) + (! Qb & ! CBREQ/ & ! BRDY#))
```

The output equation for CACHE_BLAST# is given below. This signal will not glitch during state transition, since a grey code was used for state encoding.

```
CACHE_BLAST# = ! (Qb & ! Qa)
```

Logically ANDing NON_CACHE_BLAST# and CACHE_BLAST# will give the signal needed to drive the system BLAST# to the memory system.

```
BLAST# = NON_CACHE_BLAST# & CACHE_BLAST#
```

In order for the 53C720 to transfer data on the 80486 local bus, two more signals must be discussed. The first is the 53C720 READYI/ input signal. Both the system RDY# and BRDY# should be logically ANDed to generate the READYI/ signal for the 53C720. The system RDY# should be connected to the 53C720 TBI/ signal since the memory system will return RDY# for non-burst data transfers. This will indicate to the 53C720 that the data cycle is not a cache line burst and the 53C720 will resume with the basic two clock data cycle. If the memory system does not perform bursts, it must return RDY# to the 53C720 during the first data transfer. Returning RDY# during the second, third or fourth data transfer of a 53C720 cache line burst could result in improper operation of the 53C720. See the Bus Mode 4, Bus Master Read/Write (Cache Line Burst) timings in Chapter Six of the NCR 53C720 *Data Manual* for proper operation.

The designer may choose the type of circuit components used to implement the above logic. Figure 2 illustrates signal activity on the NCR 53C720 during master cycles. Figure 3 is an interface diagram that shows the logical connections between the NCR 53C720 and the 80486 processor.

Figure 2. NCR 53C720 Master Cycle
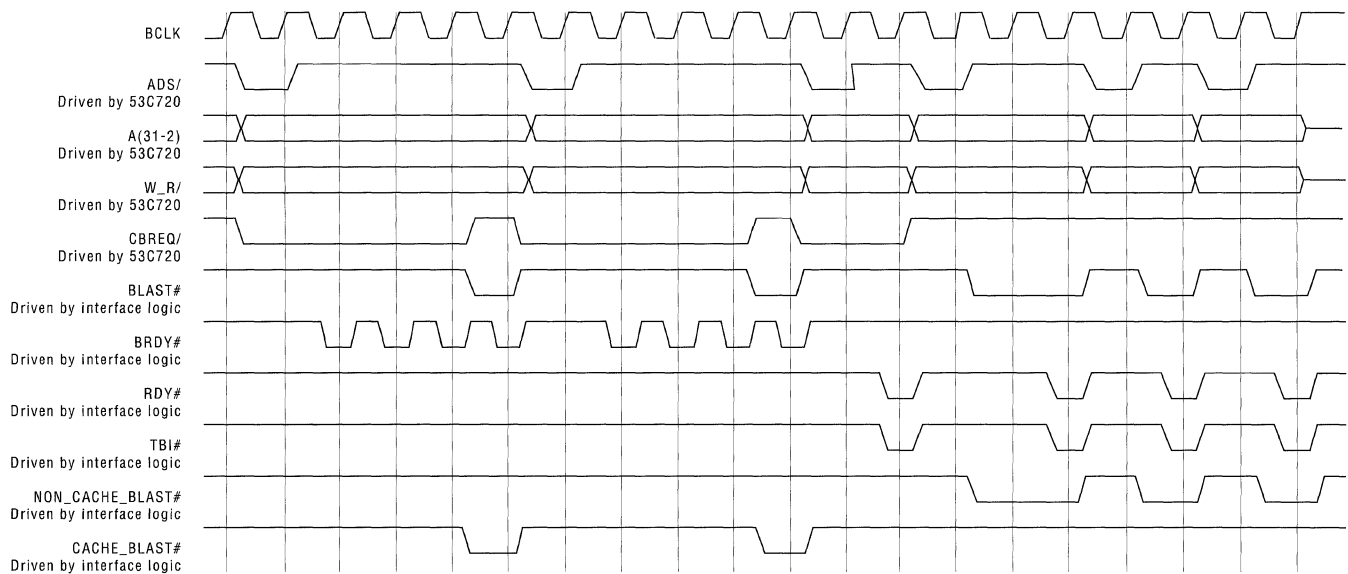
Figure 4. NCR 53C720 to 80486 Interface

SCSI
Engineering
Notes

No. 849
53C720 to VESA Local Bus Interface
Rev. 1.0 , 2/93
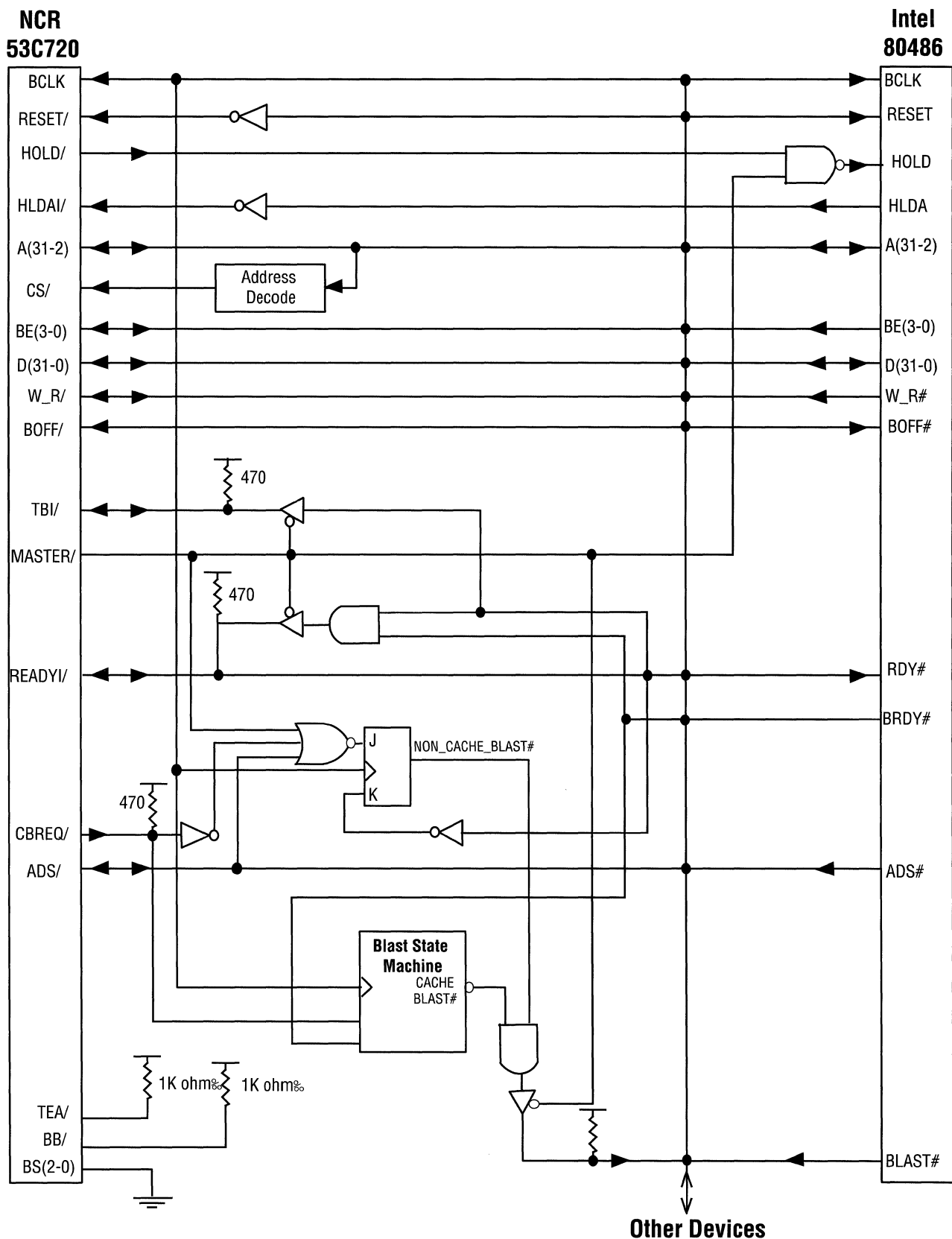
This application note defines a logical interface between the NCR 53C720 and the VESA Local Bus (VL-Bus). It contains guidelines for designing systems that use the 53C720/VL-Bus interface. This application note concentrates only on interfacing the 53C720 to the VL-Bus. Information on interfacing the 53C720 to the SCSI bus can be found in NCR SCSI Engineering Notes 833 or 836. The pound symbol (#) is used with Intel signal names to indicate that the active state occurs when the signal is at a low voltage; active low signals in the NCR 53C720 are indicated by a slash (/) following the signal name.

NOTE: this interface has not been tested, so the designer should perform a thorough design analysis before implementing this interface.

Host Interface

The 53C720 bus mode pins (BS(2-0)) are all tied to ground, enabling the chip to operate in Bus Mode 4, 80386 Little Endian mode. Two signals from the 53C720, HOLD/ and MASTER/, are ANDed to generate the VL-Bus Local Request signal, LREQ#. Since bus retries are not allowed on the VL-Bus, the 53C720 TEA/ pin should tied to V_{DD} through a 1 KΩ resistor. Because of the arbitration protocol of the VL-Bus, the 53C720 BOFF/ pin should be tied to V_{DD} through a 1KΩ resistor. If the 53C720 BB/ pin is not used, it should be tied to V_{DD} through a 1 KΩ resistor so the 53C720 will operate properly during bus arbitration.

Slave Cycles

A VL-Bus Master performs a slave read/write access to the 53C720 using a five-wait state cycle. System logic must perform the address decode for the 53C720 and select the chip by asserting the Chip Select (CS/) signal. CS/ must meet timings t_3 and t_4 (CS/ setup to and hold from BCLK high after ADS/) specified in the Bus Mode 4 Slave Read/Write Cycle section in Chapter Six of the NCR 53C720 *Data Manual*. The address decode logic should also return the LDEV# (VL-Bus Target Local Device) signal to the VL-Bus Controller. Therefore, CS/ and LDEV# can be the same signal. The interface logic will generate the LRDY# (VL-Bus Local Ready) signal. The LRDY# signal is a one-clock delayed version of the 53C720 READYO/ (Ready Out) signal. For the 53C720 to terminate the slave access, the VL-Bus Controller must generate a RDYRTN# (Ready Return), that will be sampled by the 53C720. For a slave read access, the 53C720 will hold the read data until RDYRTN# is sampled active. The VL Bus BLAST# signal can be ignored, since the 53C720 cannot burst during slave accesses. See the Slave Cycle waveforms in Figure 1 and the NCR 53C720 *Data Manual* for more information.

Figure 1. 53C720 and VL-Bus Slave Cycle
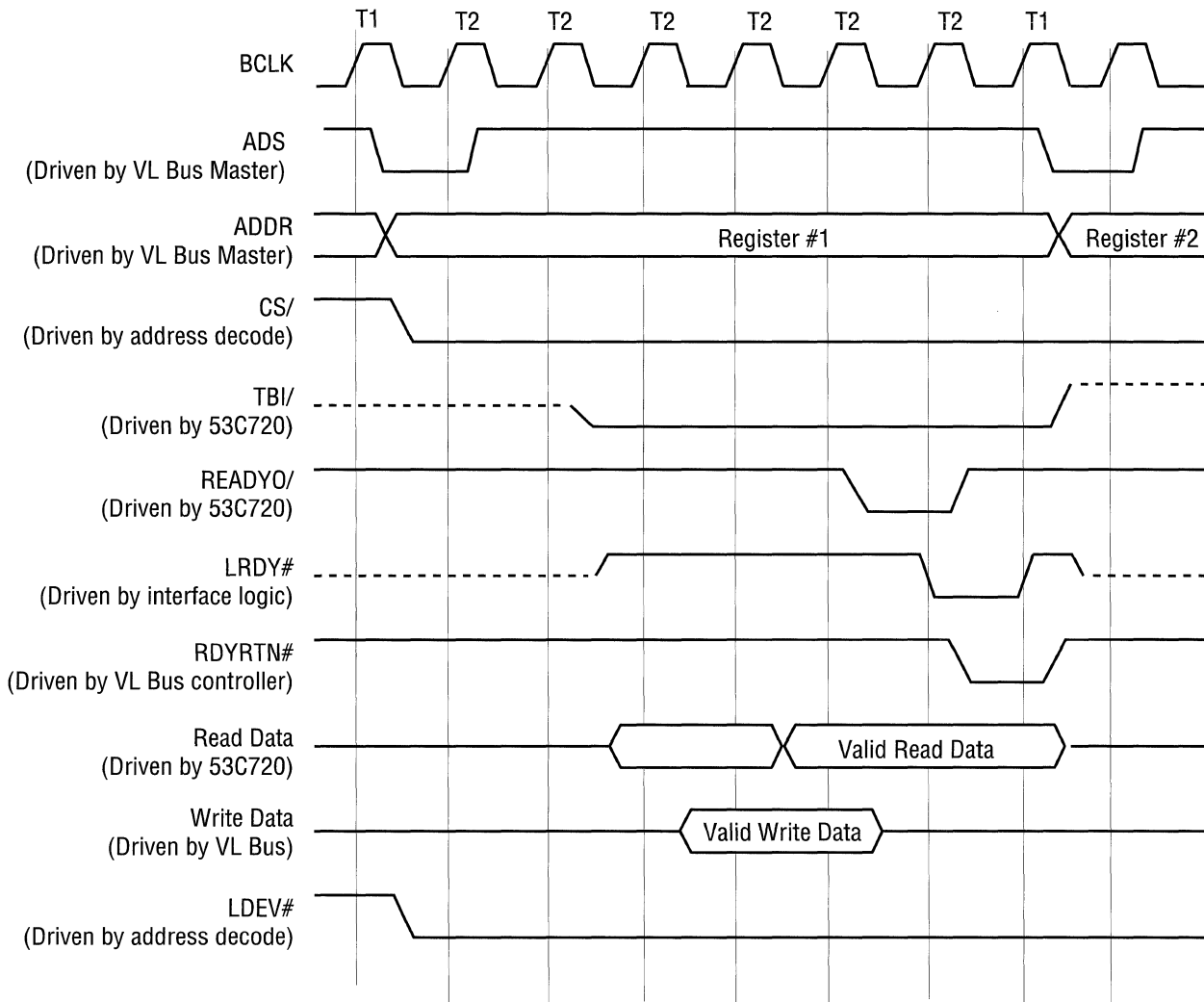
Master Cycles

The interface logic must generate the BLAST# signal, to indicate to the memory system that the next time LRDY# (VL-Bus Controller generates RDYRTN#) or BRDY# is returned, the data cycle transfer will terminate. The interface logic should generate two burst last signals, then logically AND to generate the system BLAST# signal. The first burst last signal, NON_CACHE_BLAST#, will be for the basic two-clock data cycle. This signal is implemented using a clocked J-K flip-flop. The J, K and NON_CACHE_BLAST# equations are as follows:

```
J = ! ( ! CBREQ/ + ADS/ + MASTER/)

K = ! RDYRTN#

NON_CACHE_BLAST# = ! Q
```

The signals CBREQ/, ADS/ and MASTER/ are outputs from the 53C720. The signal RDYRTN# is an output from the VL-Bus Controller and is generated from the LRDY# output by the memory system.

For the 53C720 to perform cache line bursts as illustrated in the NCR 53C720 *Data Manual*, in register CTEST0, bit 0 (C386E) must be set and bit 7 (CDIS) must be cleared. The second burst last signal, CACHE_BLAST#, is generated by implementing a four-state grey code state machine with the state diagram in Figure 2.

Figure 2. State Diagram
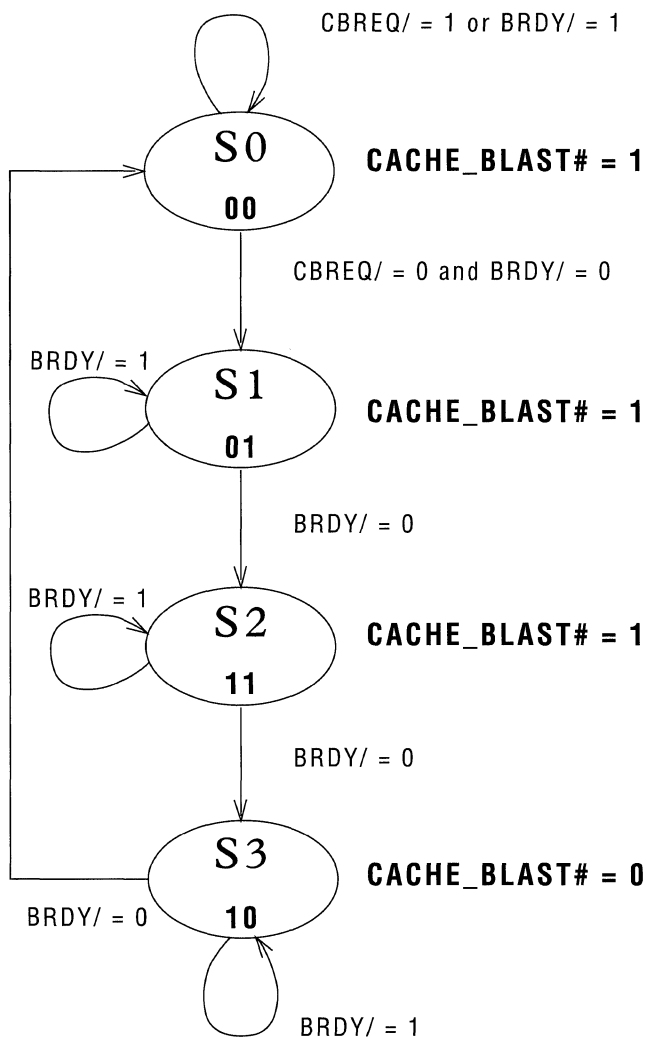
The next state equations for the state machine are given below. Qb is the most significant bit.

```
Qb(n+1) = ((Qa & ! BRDY#) + (Qb & BRDY#))

Qa(n+1) = ((Qa & BRDY#) + (! Qb & Qa) + (! Qb & ! CBREQ/ & ! BRDY#))
```

The output equation for CACHE_BLAST# is given below. This signal will not glitch during state transition since a grey code was used for state encoding.

```
CACHE_BLAST# = ! (Qb & ! Qa)
```

Logically ANDing NON_CACHE_BLAST# and CACHE_BLAST# will give the signal needed to drive the system BLAST# to the memory system.

```
BLAST# = NON_CACHE_BLAST# & CACHE_BLAST#
```

For the 53C720 to transfer data on the VL-Bus, two more signals must be discussed. The first is the 53C720 READYI/ input signal. RDYRTN# and BRDY# should be logically ANDed to generate the 53C720 READYI/ signal. The system RDYRTN# should be connected to the 53C720 TBI/ signal, since the memory system will return LRDY# for non-burst data transfers. This will indicate to the 53C720 that the data cycle is not a cache line burst and the 53C720 will resume with the basic two-clock data cycle. If the memory system does not perform bursts, it must return LRDY# during the first data transfer. Returning LRDY# during the second, third or fourth data transfer of a 53C720 cache line burst could result in improper operation of the 53C720. See the section "Bus Mode 4 Bus Master Read/Write (Cache Line Burst)" in Chapter Six of the NCR 53C720 *Data Manual,* for proper operation.

The designer may choose the type of circuit components used to implement the above logic. Figure 3 illustrates the signal activity on the NCR 53C720 during master cycles. Figure 4 is an interface diagram that shows the logical connections between the NCR 53C720 and the VL-bus.

Figure 3. 53C720 Master Cycle

Figure 3. 53C720 Master Cycle
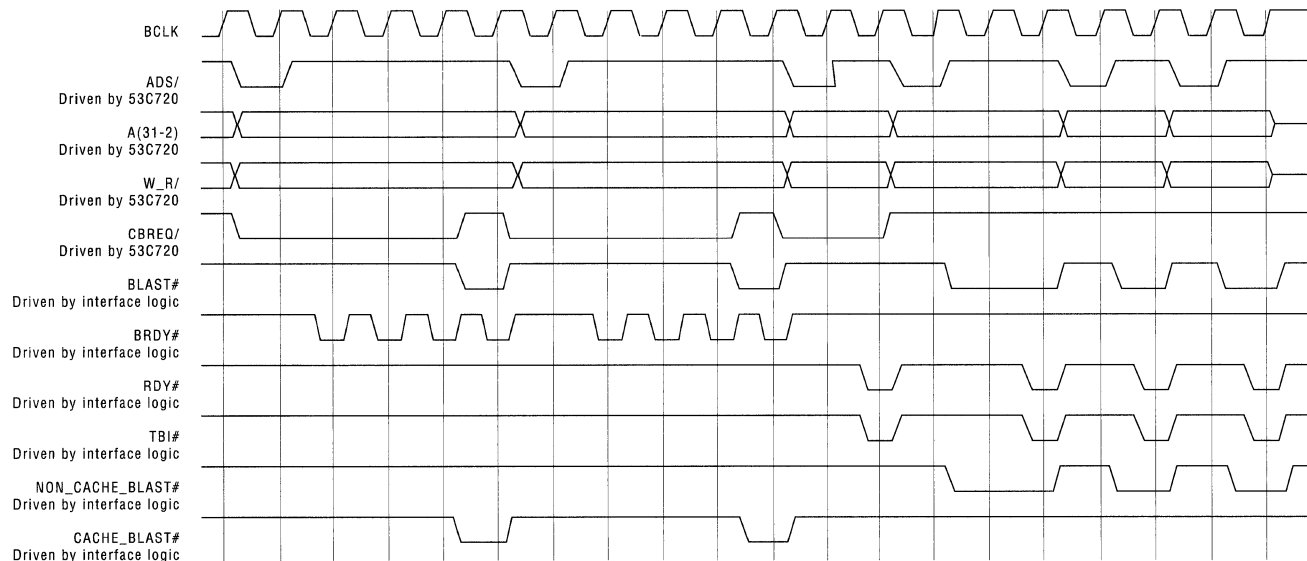
Figure 4. NCR 53C720/VL Bus Interface Diagram
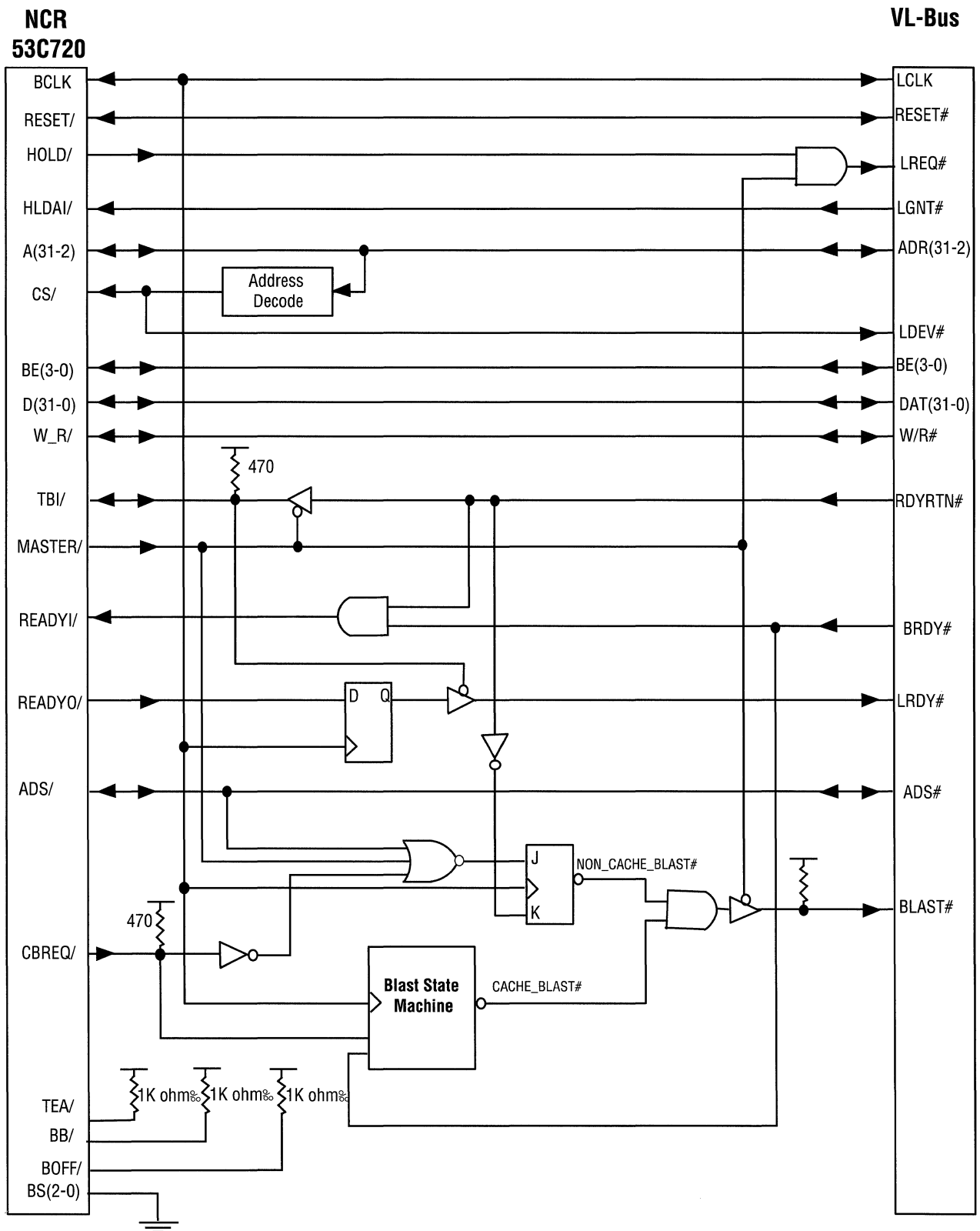
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