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INTEGRATED CIRCUITS

FOR CONSUMER USE

1983/1984

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INTEGRATED CIRCUITS FOR CONSUMER USE 1983/1984

ALPHA-NUMERICAL INDEX

QUICK REFERENCE GUIDE FOR AUDIO ICs

AM TUNER ICs

Type No.	Package	Function						Application			Page
		AM-RF CON.	AM IF	AM DET	FM IF	FM DET	Remarks	Home Audio	Car Audio	Portable Audio	
μPC1018C	16-DIP	●	●		●			▲		●	272
μPC1215V	19-VDIP	●	●	●			for DTS		●		57
μPC1216V2	19-VDIP	●	●	●					●		66
μPC1222C/C(R)	16-DIP	●	●	●	●	●	C(R): Reverse S Curve	▲		●	278
μPC1243C	16-DIP	●	●	●				●			169

FM-IF AMPLIFIER ICs

Type No.	Package	Function				Application			Page
		FM IF	FM DET	Signal Meter	DET	Home Audio	Car Audio	Portable Audio	
μPC1028H	7-SIP	⊙	⊙		PEAK	▲	⊙	▲	74
μPC1163H	7-SIP	●				●			177
μPC1167C2	16-DIP	●	●	●	QUADRATURE	●	▲		186
μPC1200V	15-VDIP	●	●		QUADRATURE	▲	●		79
μPC1245V	19-VDIP	●	●	●	PEAK	▲	●		85

FM-MULTIPLEX ICs

Type No.	Package	Function				Application			Page
		PLL	POST AMP	VCO STOP	Sep. Adj.	Home Audio	Car Audio	Portable Audio	
μPC587C2	14-DIP	●				▲	●		93
μPC1026C	14-DIP	●				▲	●		101
μPC1161C3	16-DIP	●	●	●		●			195
μPC1197C	16-DIP	●		●	●		▲	●	286
μPC1227V	19-VDIP	●		●	●		●		109
μPC1235C	16-DIP	●	●	●	●	●			206
μPC1320C	16-DIP	●		●	●		●	▲	115

PRE AMPLIFIER ICs

Type No.	Package	Supply Voltage	Function			Electrical Characteristics			Application			Page
		V_{CC} (V)	PRE AMP	ALC	DUAL	A_{VO} (dB)	T.H.D. (%)	Noise (μVr.m.s.)	Home Audio	Car Audio	Portable Audio	
μPC1032H	8-SIP	8 ~ 17	●		●	81.0	0.1	1.4		●		125
μPC1158H2	7-SIP	2.2 ~ 15	●	●		70.0	0.05	1.2			●	296
μPC1204C	16-DIP	8 ~ 20	●	●		85.0	0.3	1.3	▲		●	302
μPC1217G	20-MFP	1.8 ~ 6	●	●		72.0	0.07	1.0			●	307
μPC1224H	8-SIP	±10 ~ ±25	●		●	72.0	0.002	0.8	●			217
μPC1228H	8-SIP	6 ~ 16	●		●	100.0	0.05	1.1		●	▲	130

POWER AMPLIFIER ICs

Type No.	Package	Supply Voltage V_{CC} (V)	Electrical Characteristics				Applications			Page
			P_O (W)	R_L (Ω)	V_{CC} (V)	Remarks	Home Audio	Car Audio	Portable Audio	
μPC1177H	12- Po SIP	3.5 ~ 10	3.5	4	6	BTL (1 W DUAL)			●	314
μPC1181H3/82H3	7- Po SIP	9.5 ~ 16	5.8	4	13.2	OTL		●		137
μPC1185H2	12- Po SIP	9.5 ~ 18	5.8X2	4	13.2	OTL		●		142
μPC1188H	12- Po SIP	±17 ~ ±23	18	8	±22	OTL	●			222
μPC1212C	8- DIP TAB	3.5 ~ 9	1	4	6	OTL			●	326
μPC1213C	8- DIP TAB	4.5 ~ 11	2.4	4	9	OTL			●	336
μPC1218H	8- SIP	1.8 ~ 5	0.25	8	3	BTL			●	347
μPC1221C	14- DIP TAB	3.5 ~ 9	1	4	6	OTL Pre+ALC			●	350
μPC1230H	12- Po SIP	9 ~ 16	20	4	13.2	BTL		●		146
μPC1238	5- Po VDIP	±6 ~ ±1.5	8.4	8	±13	OTL	●			228
μPC1241H/42H	8- Po SIP	9 ~ 16	5.8	4	13.2	OTL		●		152
μPC1263C2	14- DIP TAB	3 ~ 13	1.2X2	8	9	OTL			●	357
μPC1277H	12- Po SIP	5 ~ 16	4.2X2	4	12	OTL	▲		●	363
μPC1350C	14- DIP TAB	3.5 ~ 10	0.45	8	6	OTL Pre+ALC			●	368
μPC2002	5- Po VDIP	8 ~ 18	5.4	4	14.4	OTL		●		159

QUICK REFERENCE GUIDE FOR DTS ICs

DIGITAL TUNING SYSTEM ICs μPD1700 Series (AUDIO & TV)

Item \ Type No.	μPD 1701C-011	μPD 1701C-013	μPD 1701C-014	μPD 1703C-017	μPD 1703C-018	μPD 1703C-020	μPD 1704C-011	μPD 1705C-012	μPD 1706G-011
Package	28-SLIM DIP	28-SLIM DIP	28-SLIM DIP	28-SLIM DIP	28-SLIM DIP	28-SLIM DIP	42-DIP	42-DIP	64-FLAT
Last Channel Memory	FM, MW, LW	FM, MW	FM, MW	TV	FM, MW, LW	FM, MW, LW	FM, MW	TV	FM, MW LW, SW
Preset Memory	6(FM)/6(MW)	6(FM)/6(MW)	6(FM)/6(MW)		7(FM)/ 7(MW+LW)	6(FM)/6(MW)	8(FM)/8(MW)		10(FM+MW +LW+SW)
Preset Ch. Address Ind.					●		●		
Auto Up	⊙	●	⊙	●	●	⊙	⊙	⊙	⊙
Auto Down	⊙			⊙	⊙	⊙	⊙	⊙	●
Manual Up	●	⊙	⊙	●	●	⊙	●	●	●
Manual Down	⊙	⊙	⊙	⊙	⊙	⊙	⊙	⊙	⊙
Rotary Tuning		⊙	⊙						
10-Key Direct				⊙				⊙	⊙
Muting	⊙	⊙	⊙		⊙	⊙	⊙		⊙
IF Offset	⊙	⊙	⊙		⊙	⊙	⊙		⊙
Dimmer	⊙	⊙	⊙			⊙			
Clock (Hr)	24	12	12			24	24	12	12/24
Timer (Series)						1	3	1	1
Sleep (Auto off minute)						64			60
Indicator: LED	⊙	⊙	⊙	▲	▲	▲	▲	⊙	
Indicator: FIP	▲	▲	▲	⊙	⊙	⊙	●	⊙	
Indicator: LCD									⊙
Remo. Con.				⊙			⊙	●	
Application: Audio: Car	●	●	●		▲	▲	▲		▲
Application: Audio: Home	▲	▲	▲		●	●	●		▲
Application: Audio: Portable	▲	▲	▲		▲	▲	▲		●
Application: TV-CATV				●				●	
Prescaler	μPB553AC			μPB562C	μPB553AC			μPB562C	μPB556C

QUICK REFERENCE GUIDE FOR TV ICs

CHANNEL SELECTOR ICs

Type No.	Package	Supply Voltage V_{CC} (V)	Function			Indicator		Remarks	Page
			Tuning Voltage Stabilizer	12 Ch Selector	16 Ch Selector	Neon	LED		
μPC574J	TO–92	–	●					33 V Zener	382
μPC1361C	24-DIP	12		●		●	●		386
μPC1362C	20-DIP	12		●		●	●		392
μPC1363C	24-DIP	12			●	●	●		398

DIGITAL TUNING SYSTEM ICs

Refer to "DIGITAL TUNING SYSTEM ICs μPD1700 Series" on Page 9.

INFRARED REMOTE CONTROL SYSTEM ICs

Type No.	Package	Supply Voltage V_{CC} (V)	Function				Remarks	Page
			Transmitter		Pre Amplifier	Receiver for TV		
			TV	General				
μPD1986C	16-DIP	2.2 ~ 7.2	●				27-KEY	423
μPD1913C	16-DIP	2.0 ~ 3.3		●			20-KEY 32-Custom Code	411
μPD1943G	20-MFP	2.0 ~ 3.3		●			32-KEY 256-Custom Code	411
μPD6102G	24-MFP	2.0 ~ 3.3		●			64-KEY 256-Custom Code	433
μPC1373H	8-SIP	6 ~ 14.4			●			405
μPD1937C	16-DIP	12				●	27-Command Receiver	418
μPD1987C	16-DIP	12				●	26-Command Receiver	428

PIF ICs

Type No.	Package	Supply Voltage V_{CC} (V)	Function						Page
			VIF Amplifier	AGC	Video Detector	Video Amplifier	AFT	SIF Independence	
μPC1356C2	22-DIP	12	●	●	●	●	●	●	442
μPC1366C	14-DIP TAB	12	●	●	●	●			452

SOUND ICs

Type No.	Package	Supply Voltage V_{CC} (V)	Function				Remarks	Page
			SIF Amp. & Det.	DC Volume	Audio Driver	Audio Output		
μPC1353C	14-DIP TAB	12	●	●	●	●		456
μPC1382C	14-DIP	12	●	●	●			463
μPC1391H	8-SIP	12	●				for Stereo & Bilingual Demo.	469

CHROMINANCE & LUMINANCE ICs

Type No.	Package	Supply Voltage V_{CC} (V)	Function						Remarks	Page
			Video Amp.	Pedestal Clamp	Color Sync.	Color Demo.	PAL/ SECAM Auto Sw.	Video Text Interface		
μPC1352C	28-DIP	12	●	●	●	●			NTSC; DC Res.: 75 %	473
μPC1364C2	28-DIP	12			●	●			SECAM	491
μPC1365C	28-DIP	12	●	●	●	●	●		PAL; DC Res.: 100 %	505
μPC1384C	28-DIP	12	●	●	●	●	●		PAL; DC Res.: 75 %	525
μPC1397C	22-DIP	12						●	Analogue Inputs	545

DEFLECTION ICs

Type No.	Package	Supply Voltage V_{CC} (V)	Function				Application		Page
			Sync. Sep.	Vert. OSC	Hori. AFC · OSC · X-Ray · Pre-Driver	Vert. Output	Color	B/W	
μPC1031H2	10-Po SIP	12 ~ 18		●		●	Small	●	552
μPC1379C	16-DIP TAB	12	● (H+V) Sep	●	●	●	Small	●	569
μPC1377C	22-DIP	12	● H Sep V Sep	●	●		●		560
μPC1378H	7-Po SIP	24				●	●		565

QUICK REFERENCE GUIDE FOR VOLTAGE REGULATOR ICs

SWITCHING REGULATOR CONTROL ICs

Type No.	Package	Supply Voltage V_{CC} (V)	Reference Output Voltage V_{REF} (V)	Features			Function				Page
				Output Mode	OSC-Wave Form	Over Current Protection	Inhibit	Dead Time Control	Sync.	Low Voltage Protection	
μPC494C	16-DIP	7 ~ 41	5 ± 0.25	Single or Push-Pull	Saw-Tooth	D.C.		●	●	●	816
μPC494G	16L-MFP										827
μPC1394C	14-DIP	6.6 (Shunt)		Single	Saw-Tooth	Dynamic	●	●	●		832

3-TERMINAL REGULATOR ICs

Type No.	Package	Original	Operating Temperature Range (°C)	V_{OUT} (V)	V_{IN} (V)		I_O MAX. (A)	P_T MAX. (W)
					MIN.	MAX.		
μPC78L05	SP-8 ◎	78L05	※ −20 ~ +150	☆ 5	7	30	0.1	0.8
μPC78L08	SP-8 ◎	78L08	※ −20 ~ +150	☆ 8	10.5	30	0.1	0.8
μPC78L10	SP-8 ◎	—	※ −20 ~ +150	☆ 10	12.5	35	0.1	0.8
μPC78L12	SP-8 ◎	78L12	※ −20 ~ +150	☆ 12	14.5	35	0.1	0.8
μPC78L15	SP-8 ◎	78L15	※ −20 ~ +150	☆ 15	17.5	35	0.1	0.8
μPC78M05H	TO-220AB	78M05	−20 ~ +80	★ 5	7	35	0.5	20
μPC78M08H	TO-220AB	78M08	−20 ~ +80	★ 8	10.5	35	0.5	20
μPC78M10H	TO-220AB	—	−20 ~ +80	★ 10	12.5	35	0.5	20
μPC78M12H	TO-220AB	78M12	−20 ~ +80	★ 12	14.5	35	0.5	20
μPC78M15H	TO-220AB	78M15	−20 ~ +80	★ 15	17.5	35	0.5	20
μPC78M18H	TO-220AB	78M18	−20 ~ +80	★ 18	21	35	0.5	20
μPC78M24H	TO-220AB	78M24	−20 ~ +80	★ 24	27	40	0.5	20
μPC7805H	TO-220AB	7805	−20 ~ +80	★ 5	7	35	1.0	20
μPC7808H	TO-220AB	7808	−20 ~ +80	★ 8	10.5	35	1.0	20
μPC7812H	TO-220AB	7812	−20 ~ +80	★ 12	14.5	35	1.0	20
μPC7815H	TO-220AB	7815	−20 ~ +80	★ 15	17.5	35	1.0	20
μPC7818H	TO-220AB	7818	−20 ~ +80	★ 18	21	35	1.0	20
μPC7824H	TO-220AB	7824	−20 ~ +80	★ 24	27	40	1.0	20
μPC7905H	TO-220AB	7905	−20 ~ +80	★ −5	−7	−35	1.0	20
μPC7908H	TO-220AB	7908	−20 ~ +80	★ −8	−10.5	−35	1.0	20
μPC7912H	TO-220AB	7912	−20 ~ +80	★ −12	−14.5	−35	1.0	20
μPC7915H	TO-220AB	7915	−20 ~ +80	★ −15	−17.5	−35	1.0	20
μPC7918H	TO-220AB	7918	−20 ~ +80	★ −18	−21	−35	1.0	20
μPC7924H	TO-220AB	7924	−20 ~ +80	★ −24	−27	−40	1.0	20

◎ μPC78L00 Series are used NEC original packages called SP-8.
If package dimension is needed, see each specification.
※ Junction Temperature.
☆ Output Voltage Accuracy ±10 %.
★ Output Voltage Accuracy ±5 %.

QUICK REFERENCE GUIDE FOR ARRAYS

TRANSISTOR ARRAYS

Item \ Type No.		μPA53C	μPA56C	μPA67C	μPA79C	μPA80C	μPA81C	μPA2001C	μPA2002C	μPA2003C	μPA2004C
Package		14-DIP	16-DIP	14-DIP	16-DIP	16-DIP	16-DIP	16-DIP	16-DIP	16-DIP	16-DIP
Number of units		5	7	6	7	7	7	7	7	7	7
Outputs	Sink	●		●	●		○	○	○	○	○
	Source		●			●					
$V_O(V_{SS})$ MAX. (V)		30	40	30	20	(−60)	45	60	60	60	60
I_O MAX. (A/unit)		0.4	0.1	0.15	0.15	50 m	0.4	0.5	0.5	0.5	0.5
h_{FE} TYP. (–)		3200	200	–	2500	450	2500	2800	2800	2800	2800
NPN Darlington		●	Single	●	Separate	PNP-NPN	○	○	○	○	○
Clamp Diode					○			○	○	○	○
Reverse Bias Protected Inputs				○	○						
Input Resistance (kΩ)		20	–	22	20	20	20	–	10.5 & Zener	2.7	10.5
Application	LED, Lamp	●	○			▲	○	○	○	○	○
	Printer	▲		○	●		▲	○	○	●	○
	Induction Load	▲		▲	○		▲	○	○	○	○
	FIP					○					
Remarks					Small Saturation Voltage →$V_{CE(sat)}$ ≦0.6 V	Pull down Resistors Incorpo-rated		General Purpose	14~25 V PMOS	5 V TTL, CMOS	10 V CMOS

DIODE ARRAYS

Item \ Type No.		μPA54H	μPA64H
Package		7-SIP	7-SIP
Number of Units		6	6
Common	Cathode	●	
	Anode		●
V_{RM} MAX. (V)		75	75
V_R MAX. (V)		50	50
I_O MAX. (A/unit)		0.1	0.1
t_{rr} TYP. (ns)		1.3	4.0
C_t※TYP. (pF)		2.0	5.0

※ 1 Unit

CROSS REFERENCE GUIDE FOR AUDIO ICs (I)

Function	N E C	MATSUSHITA	SANYO	HITACHI	TOSHIBA	ROHM	Other
AM Tuner	μPC1216V2	AN7510	LA1130	HA1199	TA7616P	BA3203	
AM Tuner AM/FM-IF Amplifier	μPC1018C	AN7218*					
	μPC1222C	AN7222	LA1210	HA12413	TA7614P	BA4210*	
FM-IF Amplifier (Peak Det.)	μPC1028H*		LA1150*		TA7130P*	BA403*	MB3202 (FUJITSU)
	μPC1245V						
FM-IF Amplifier (Quadrature Det.)	μPC1200V μPC1167C2*	AN377* AN7256 AN7258	LA1230* LA1231N LA1140	HA1137* HA11225* HA12411 HA12418	TA321P TA7329P		CA3089* (RCA)
FM-MPX Demodulator	μPC587C2* μPC1026C	AN115		HA1156*	TA7157P*	BA1310*	MC1310P* (MOTOROLA)
	μPC1161C3 μPC1235C	AN7470		HA1196 HA12016			
	μPC1320C*	AN362	LA3365			BA1320*	
	μPC1197C*	AN7410	LA3360	HA11227*	TA7604P*	BA1330	
	μPC1227V	AN7414 AN7417	LA3370			BA1350	
FM Noise Canceller	μPC1176C*	AN101* AN6130	LA2100* LA2101 LA2110	HA11219			TDA1001* (PHILIPS)

*Pin Replaceable

CROSS REFERENCE GUIDE FOR AUDIO ICs (II)

Function	N E C	MATSUSHITA	SANYO	HITACHI	TOSHIBA	MITSUBISHI	Other
Pre Amplifier	μPC1032H*	AN7310*	LA3161*			M5152L*	BA328* (ROHM)
	μPC1158H2		LA3200		TA7137P		
	μPC1228H				TA7325P	M51522L	
	μPC1217G					M51141P	
Pre + ALC Power Amplifier	μPC1350C				TA7628P		
	μPC1221C			HA1361	TA7223P		
Power Amplifier (Single Channel)	μPC1212C	AN7110	LA4110		TA7207P		BA527 (ROHM)
	μPC1213C	AN7120	LA4112	TBA810	TA7208P		BA534 (ROHM)
	μPC1218H				TA7331P	M51503L	BA515 (ROHM)
	μPC1181H3/ 82H3 μPC1241H/ 42H	AN7131 AN7140		HA1366W	TA7222P TA7252P	M51518L M51103L	
	μPC2002*			TDA2002*			TDA2002* (SGS)
	μPC1238*						TDA2006* (SGS)
Power Amplifier (Dual Channel)	μPC1185H2	AN7156 AN7166		HA1377A HA1398	TA7227P TA7240P	M51515L M51517L	BA535 (ROHM) BA542 (ROHM)
	μPC1177H		LA4182				
	μPC1277H	AN7145	LA4125	HA1392	TA7215P		BA536 (ROHM)
Power Amplifier (BTL)	μPC1230H			HA1388A	TA7240P		

* Pin Replaceable

CROSS REFERENCE GUIDE FOR TV ICs

Function	NEC	MATSUSHITA	SANYO	HITACHI	TOSHIBA	MITSUBISHI	Other
Tuning Voltage Stabilizer	μPC574J*		L5630*	HZT33			ZTK33 (ITT)
Channel Selector	μPC1361C μPC1363C	AN5010					
Remo. Con. Transmitter	μPD1913C	MN6024 MN6025				M50110P	
	μPD1943G	MN6027		HD43019	TC9132P	M50115P	SAB3209 (PHILIPS) SAA5010 (ITT)
	μPD6102G			HD43019A			
Remo. Con. Pre Amp.	μPC1373H	AN5020		HD44042			
PIF Processor	μPC1356C2*	AN5111	LA1357N*	HA11215F	TA7607P	M5185P	
	μPC1366C			HA11221			
SIF Processor	μPC1391H	AN5215					
	μPC1382C	AN5220	LA7700	HA1124	TA7632P		
	μPC1353C	AN5250		HA1364		TA7620P	TDA1190 (SGS)
(NTSC)	μPC1352C*	AN5310*	LA7600	HA11412A	TA7608CP		TDA3570* (PHILIPS)
Chroma Processor & (PAL) Video Amplifier	μPC1365C					M51593P	TDA3300 (MOTOROLA) TDA3560 (PHILIPS) TDA1365 (PLESSY) TA10313 (RCA)
(PAL)	μPC1384C						
Chroma Processor (SECAM)	μPC1364C2					M51397P	TDA3030 (MOTOROLA) TDA3520 (PHILIPS)
Video Text Interface	μPC1397C	AN5350 AN5352					TDA3560 (PHILIPS)
Sync. Deflection	μPC1377C						
	μPC1379C						
Vert. Output	μPC1031H2*		LA1835*				TDA1170 (SGS)
	μPC1378H	AN5512					TDA1170 (SGS)

* Pin Replaceable

CROSS REFERENCE GUIDE FOR VOLTAGE REGULATOR ICs

3-TERMINAL REGUALTOR & SWITCHING REGULATOR CONTROL ICs

Function	NEC	FAIRCHILD	NATIONAL	MOTOROLA	TEXAS
3-Terminal Positive Regulator (0.1 A)	μPC78L05	μA78L05AWC	LM78L05CZ	MC78L05CP	μA78L05CLP
	μPC78L08	μA78L08AWC	LM78L08CZ	MC78L08CP	μA78L08CLP
	μPC78L10	–	–	–	μA78L10CLP
	μPC78L12	μA78L12AWC	LM78L12CZ	MC78L12CP	μA78L12CLP
	μPC78L15	μA78L15AWC	LW78L15CZ	MC78L15CP	μA78L15CLP
3-Terminal Positive Regulator (0.5 A)	μPC78M05H	μA78M05UC	LM341P-5.	MC78M05CP	μA78M05CKC
	μPC78M08H	μA78M08UC	LM341P-8.	MC78M08CP	μA78M08CKC
	μPC78M10H	–	–	–	–
	μPC78M12H	μA78M12UC	LM341P-12	MC78M12CP	μA78M12CKC
	μPC78M15H	μA78M15UC	LM341P-15	MC78M15CP	μA78M15CKC
	μPC78M18H	μA78M18UC	LM341P-18	MC78M18CP	μA78M18CKC
	μPC78M24H	μA78M24UC	LM341P-24	MC78M24CP	μA78M24CKC
3-Terminal Positive Regulator (1A)	μPC7805H	μA7805UC	LM340T-5	MC7805CP	μA7805CKC
	μPC7808H	μA7808UC	LM340T-8	MC7808CP	μA7808CKC
	μPC7812H	μA7812UC	LM340T-12	MC7812CP	μA7812CKC
	μPC7815H	μA7815UC	LM340T-15	MC7815CP	μA7815CKC
	μPC7818H	μA7818UC	LM340T-18	MC7818CP	μA7818CKC
	μPC7824H	μA7824UC	LM340T-24	MC7824CP	μA7824CKC
3-Terminal Negative Regulator (1A)	μPC7905H	μA7905UC	LM320T-5	MC7905CP	μA7905CKC
	μPC7908H	μA7908UC	LM320T-8	MC7908CP	μA7908CKC
	μPC7912H	μA7912UC	LM320T-12	MC7912CP	μA7912CKC
	μPC7915H	μA7915UC	LM320T-15	MC7915CP	μA7915CKC
	μPC7918H	μA7918UC	LM320T-18	MC7918CP	μA7918CKC
	μPC7924H	μA7924UC	LM320T-24	MC7924CP	μA7924CKC
Switching Regulator Control	μPC494C/G	μA494	–	TL494	TL494

CROSS REFERENCE GUIDE FOR TRANSISTOR ARRAYS

TRANSISTOR ARRAYS

NEC	SPRAGUE	SHARP	HITACHI	OKI	TOSHIBA	MITSUBISHI	SANYO	Other
μPA53C*			(HD2919P)*			M54516P*	LB1287* (LB1288)*	
μPA56C					(TD62505P)			
μPA67C*						(M54527P)*	(LB1273R)*	
μPA79C*		IR2423*			TD62307P*	(M54533P)	(LB1264)*	
μPA80C	(UHP495)			(MSL915RS) (MSL916AS)	(TD62703P)		(LB1240)	(AN6873) (MATSUSHITA)
μPA81C*		IR2403*			(TD62105P)*	M54519P*		

NEC	SPRAGUE	TEXAS	MOTOROLA	PHILIPS	TOSHIBA	MITSUBISHI	SANYO	OTHER
μPA2001C*	ULN2001*	SN75466*	MC1411*	ME5501*	TD62001P*	M54524P*	LB1231*	XR2201* (ROHM)
μPA2002C*	ULN2002*	SN75467*	MC1412*	ME5502*	TD62002P*	M54525P*	LB1232*	XR2202* (ROHM)
μPA2003C*	ULN2003*	SN75468*	MC1413*	ME5503*	TD62003P*	M54523P*	LB1233*	XR2203* (ROHM)
μPA2004C*	ULN2004*	SN75469*	MC1416*	ME5504*	TD62004P*	M54526*	LB1234*	XR2204* (ROHM)

* Pin Replaceable
( ) Some Difference in Specification

MAINTENANCE AND OBSOLETE TYPES

Definitions of Maintenance and Obsolete Items

The fabrication techniques of semiconductor products, especially integrated circuits have been making steady progress and the improvement of their characteristics as well as development of new products are constantly under way to meet the demands of users.

Modifications to the specifications of existing products resulting from such characteristic improvements, or the introduction of newly developed products into the market will give rise to the necessity of maintenance actions for old products, or disposal of old products as obsolete items are phased out of the supply and distribution system. We at NEC are, as a rule, performing the maintenance and obsolescene actions for our products according to the following procedures, taking the maintenance action by users into consideration.

1. Alteration under Same Type Name

If it is determined that no problem exists on the interchangeability between a new product and an old product in stock, the new product will be shipped as soon as the old product runs out of stock. In this case, the lot identification will be changed.

If it is determined that a problem exists on the interchangeability of the old product with the new one depending on the usage of the old product by users, a suffix will be added to the name of the new product.

(Example: μPC566H→μPC566H3)

2. Designation of Maintenance Item

Prior to declaring as an obsolete item, an old type product which no longer satisfies the market needs in terms of its characteristics, price, etc. will normally be designated as a maintenance item. Users will be informed of this declaration from NEC's Sales Department. Since all the maintenance items will eventually become obsolete items, use of maintenance items is restricted to only the maintenance use for equipment with the existing circuit design. Avoid using them for equipment with new circuit design.

For the products designated as maintenance items, we at NEC are asking for co-operation of all users by restricting the distribution to users of the catalogs or samples of the maintenance products, obtaining information from each user on the future demand for the products, or encouraging users to employ substitute products for maintenance in order to decrease the number of types.

3. Designation of Obsolete Item

About one year after the declaration, if the substitution efforts at the users have proceeded, the maintenance item will be designated as an obsolete item. This declaration will also be informed to all users from NEC's Sales Department.

Once a product becomes an obsolete item, its stock on hand, catalogs and related documents will be discarded. Therefore, any product with the type name will no longer exist in the NEC's supply system. Accordingly, all users are requested to contact the nearest NEC's sales representatives, Sales Department and/or Engineering Department to secure the maintenance item in the required quantity or to convert to a substitute item during the one-year period before the maintenance item will be redeclared as an obsolete item.

MAINTENANCE AND OBSOLETE NUMBER

AUDIO ICs

Maintenance Number	Obsolete Number	Substitute Number
–	μPC27C	μPC1018C or μPC1222C/C (R)
–	μPC30C	μPC1243C
–	μPC33C	μPC1224H
μPC41C	–	μPC1221C
μPC566H	–	μPC566H3
–	μPC571C	μPC1238
–	μPC573C	
μPC576H	–	
–	μPC578C	μPC1238
–	μPC1013C	μPC1018C
–	μPC1016C	μPC1224H
–	μPC1021C	μPC1216V2
–	μPC1156H2	μPC1241H/42H
–	μPC1172C	μPC1222C/C (R)
–	μPC1183H	μPC1241H/42H

TV ICs

Maintenance Number	Obsolete Number	Substitute Number
–	μPC16C	μPC1391H or μPC1382C
–	μPC17C	μPC1391H or μPC1382C
–	μPC29C	μPC1352C
–	μPC31C	μPC1352C
–	μPC32C	μPC1352C
–	μPC35C	μPC1353C
–	μPC46C	μPC1377C
μPC558C	–	μPC1391H or μPC1382C
–	μPC561C	μPC1377C
–	μPC562C	μPC1352C
–	μPC570C	μPC1377C
–	μPC572C	μPC1377C
–	μPC584C	μPC1362C or μPC1363C
–	μPC1357C2	μPC1377C
μPC1380C	–	μPC1352C

NEC's INTEGRATED CIRCUITS FOR CONSUMER USE

1. History of ICs in NEC

History of NEC's integrated circuits (ICs) dates back to 1959 in which year NEC set its hand for the first time to the research and development of integrated circuits. As a result of the research, a DCTL digital IC consisting of grown transistors and semiconductor resistors was developed in 1960, and analog ICs such as linear amplifiers, active filters, modulators, etc., were manufactured on trial during a period from 1961 to 1962.

In 1964, NEC created a sensation by exhibiting wide-band amplifier circuits, μPC1A/B, μPC3A, and μPC11A in the WESCON show. At the same time, NEC went into mass production of the DTL μPB1 to μPB10A Series intended for NEAC computers.

In 1966, while leading semiconductor manufacturers at home and abroad were in the throes of pursuing the stability and reliability of their products, NEC, through development of various new technologies, succeeded in marketing MOS type digital integrated circuits, μPD9A to μPD16A Series as ICs for electronic desktop calculators and measuring instruments, thereby laying the foundation for today's microcomputers and large-capacity memories.

Subsequently, NEC, in anticipation of the market needs, developed and marketed such standard products as TTL, CSL, CML, CTL, and HNIL in the field of bipolar digital ICs; those ranging from MSIs and LSIs for mainly electronic calculators and watches, to microcomputers and memories in the field of MOS type digital ICs; and operational amplifiers, comparators, power regulators, and various ICs for TV and stereo equipment in the field of analog ICs.

In addition to these standard products, NEC is producing a number of custom products based on specific customer requests or through co-operative development with customers.

Integrated circuits feature light weight, compactness, improved reliability, high cost performance, etc. High performance and easiness of realizing new functions impossible with discrete parts can be realized by ICs. We at NEC are exerting ourselves in the areas of semiconductor device, circuit design, production and quality control technologies not only to improve the performance and reliability of ICs but also to expand the application range of ICs by breaking through the barriers of power and frequency, with a view toward achieving integrated circuits of much larger scale.

2. Types and Features of Integrated Circuits

There are various methods of classifying ICs such as by structure, usage, degree of integration, etc. The classifications of ICs by three different methods are given in Tables 1, 2, and 3, respectively.

Table 1. Classification of ICs by Structure

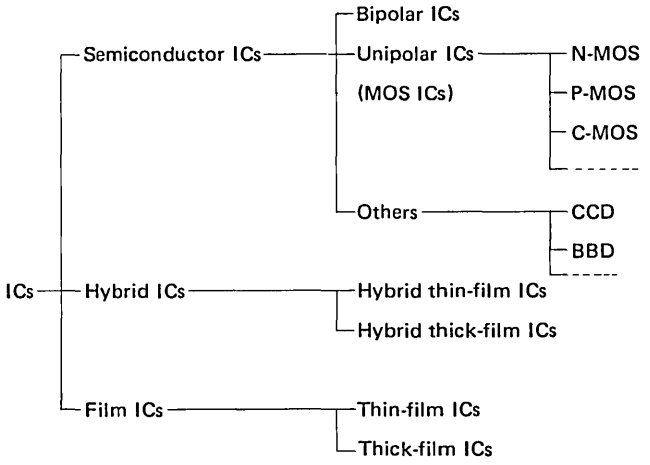


Table 2. Classification of ICs by Application

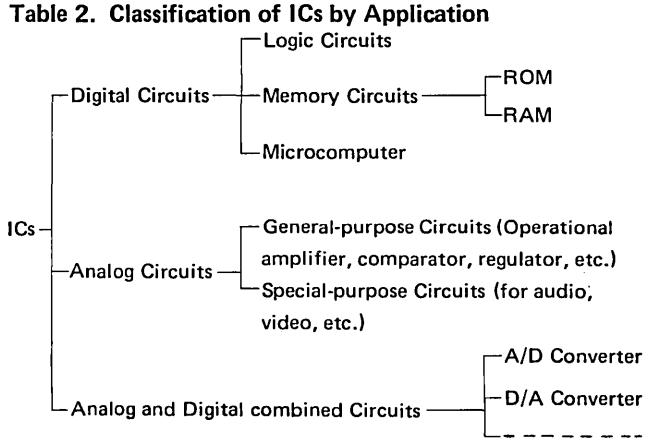


Table 3. Classification of ICs by Degree of Integration

Classification	Definition (JIS C 5610)
Small-scale IC (SSI)	An integrated circuit containing less than 100 elements on a single chip.
Medium-scale IC (MSI)	An integrated circuit containing more than 100 but less than 1 000 elements on a single chip.
Large-scale IC (LSI)	An integrated circuit containing more than 1 000 elements on a single chip but not included in the category of the VLSI below.
Very Large-scale IC (VLSI)	An integrated circuit containing more than 10,000 gates or more than 100 000 elements on a single chip.

These integrated circuits have the following features when they are viewed as devices.

(1) Small size and light weight
(2) Costs of assembling, processing, and/or managing can be reduced, which leads to reduction of cost per unit function.
(3) Since only a small number of parts are required for a system incorporating ICs, the reliability can be increased greatly.
(4) Though there are relatively large differences in the characteristics of the elements among ICs, the differences of characteristics and temperature coefficient among the elements in an IC are rather small.
(5) Not suitable for high power, high voltage and ultra-high frequency applications.
(6) Only small-capacitance (approx. 10 pF) capacitors can be incorporated and inductance can hardly be realized.

The IC industry has the following features.

(1) Knowledge-intensive industry.
(2) Equipment industry. (Participation in this industry may be costly, as most of the production equipment are highly automated.)
(3) Resource and energy conservative industry.
(4) Requires a large investment in research and development or equipment as the pace of technological innovation is rapid.

In view of the foregoing, ICs must be designed so as to make the most of the above features and be produced in the quantity sufficient to recover the investment.

3. Type Number Designation of NEC's Integrated Circuits

The Provisional Regulation by the JEDEC in the U.S.A. and the PRO ELECTRON in Europe are the only two registration systems currently adopted for ICs by official institutions. In Japan, a report on the proposed IC registration system has been submitted by the EIAJ to the Ministry of International Trade and Industry of Japan, but implementation of this proposed system is still pending. Therefore, IC manufacturers throughout the world are employing their own type numbers. All of NEC's integrated circuits are identified by the individual type number designated, based on the following principles.

3.1 Semiconductor integrated circuits

μP □○○○○□

- Symbol identifying one of the following types of packages
  - A: Metal can similar to TO-5
  - B: Flat pack (ceramic)
  - C: Dual in-line package (DIP) (plastic mold)
  - D: Dual in-line package (DIP)(ceramic)
  - G: Flat pack (plastic mold)
  - H: Single in-line package (SIP) (plastic mold)
  - J: Package similar to TO–92 (plastic mold)
  - M: MINI MOD Package (film-carrier type mold)
  - V: Vertical dual in-line package (VDIP)
- Serial number assigned to each product for in-house registration (based on major classifications by application)
- Symbol identifying one of the following type of circuits
  - A: Composite elements
  - B: Bipolar type digital circuit
  - C: Bipolar type analog circuit
  - D: Unipolar type digital circuit (MOS)
- Symbol indicating a semiconductor integrated circuit (Abbreviation for MICRO PACK)

When marketed as a second source product which is pin-compatible with the products of other manufacturers popular in the market, the second source product is designated by the same serial number as that of the first source product.

3.2 Hybrid integrated circuits

MC - ○○○○

- Serial number assigned to each product for in-house registration
- Abbreviation for trademark "NEMAC" (NEC Micro Assembled Circuit)

4. Semiconductor Device Technologies of NEC's ICs for Consumer Applications

4.1 Bipolar Technology

Although the fabrication and semiconductor device technologies for integrated circuits have been making steady progress, the types of semiconductor devices that can be used in ICs and their performances are quite limited. For this reason, in designing circuits, the design techniques peculiar to ICs have been take into account, in addition to the design techniques for individual semiconductor devices, and numerous ideas have been incorporated to make the most of the features of individual devices as well as to compensate for their drawbacks. At the same time, studies to improve semiconductor devices have been in constant progress with a view to expanding the range of their application to ICs, because the functions and performances targeted for analog circuits are becoming increasingly diversified.

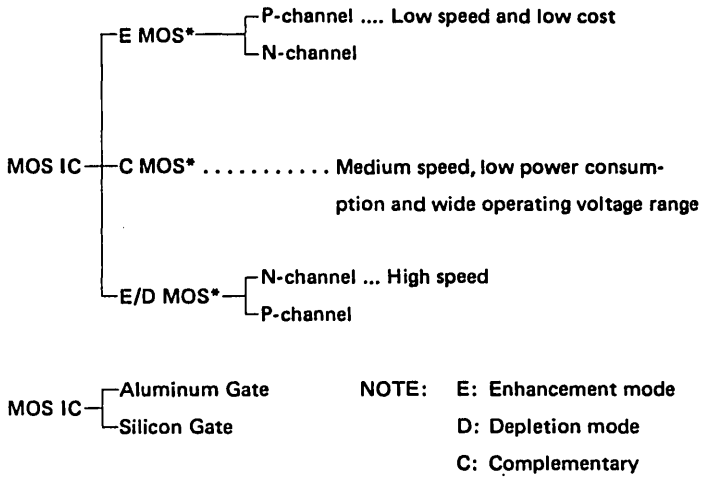
The NEC's pair transistor of "point symmetrical structure" and the low-frequency low-noise process enjoy well-established reputations.

Newly developed processes include ultrahigh-frequency process which features high-frequency (1 GHz) and low power consumption, triple diffused PNP transistors which exhibit performances equivalent to NPN transistors, high-precision polysilicon resistors, Bi-JFET (process), Bi-MOS process, I^2L process, etc. Products from these processes are displaying superb performance not only in analog ICs but also in analog and digital mixed circuits.

4.2 MOS Technology

At present, MOS devices are predominantly used in digital ICs with special exceptions, because MOS ICs feature high degree of integration as they require no P-N insulation separation, consume less power as their input impedance is high, etc. MOS ICs are thus suitable as LSIs for consumer use equipment such as electronic calculators and watches, microcomputers, memories, etc. Table 4 shows the classification of MOS ICs by structure. MOS ICs are now beginning to be adopted for analog circuits thanks to the recent advance of semiconductor device and circuit technologies.

Table 4 Classification of MOS ICs by Structure



STANDARDS OF INTEGRATED CIRCUITS

The standards of integrated circuits are prescribed by four items; absolute maximum ratings, recommended operating conditions, electrical characteristics, and outline dimensions. Integrated circuits have been designed by presupposing their operating conditions. Should they be used under conditions different from those presupposed, they can hardly exhibit their intended functions and performances. Therefore, the recommended operating conditions of ICs must be presupposed particularly in designing their circuits.

The definitions of these four items have been deliberated by the IEC and the Technical Committee of EIAJ as follows.

1. Absolute Maximum Ratings

Limiting values not to be exceeded even for a moment. These ratings are defined that any two or more of the following parameters should not reach their limiting values simultaneously.

* Absolute maximum ratings generally include the following parameters and their limiting values are specified at an ambient temperature of 25 °C.
  - ○ Terminal voltage (supply voltage, input voltage, output voltage, etc.)
  - ○ Power consumption
  - ○ Circuit current (power supply current, input/output current, etc.)
  - ○ Operating temperature range
  - ○ Storage temperature range

2. Recommended Operating Conditions

Recommended operating conditions are defined as a range within which an integrated circuit can operate normally without any discontinuous operation. The operating functions of the IC are guaranteed within this range, but its electrical characteristics are not necessarily guaranteed. The recommended operating conditions include the following parameters.

* Operating temperature range
* Terminal voltage (supply voltage, input/output voltage, etc.)
* Terminal current (input/output current, fan-out, etc.)
* Load conditions (R_L, C_L, etc.)
* Input conditions (frequency, pulse width, rise time, fall time, etc.)
* External elements (if necessary)

3. Electrical Characteristics

Electrical characteristics consist of parameters which guarantee the performance of an IC. With digital ICs, recommended operating conditions under the worst probable conditions are also specified for all parameters, whereas with analog ICs, the worst-case conditions are specified only for the parameters which become the features of the ICs.

4. Outline Dimensions

The dimensions concerning packaging space, mounting hole, lead length, lead thickness, etc., are specified.

* Standard dimensions: The dimensions most important for compatibility of ICs such as lead pitch, lead shoulder spacing, mounting hole spacing, etc., which are to be specified by their design center values.
* Lead dimensions: The lead dimensions are specified based on the principle that each lead is to be inserted into the 0.8, 1.0 or 1.2 diameter holes in a printed circuit.
* Packaging space: The maximum values of length, width, height, etc., are specified.

The outline dimensions of ICs have been standardized by IEC, EIAJ, JEDEC, etc. However, the standard dimensions are based on 2.54 mm and the number derived by either multiplying or dividing 2.54 mm by an integer. Also, in the past, the dimensional standardization was implemented by including the dimensions established by respective manufacturers. The outline dimensions of ICs are nowadays being standardized by weighting the design theory with the appropriate processing tolerances.

HINTS OF CORRECT USE

The quality and reliability of ICs largely depend on how the users handle and use ICs, as well as factors on the part of the device manufacturers. This is proved to be true by the fact that 30 to 40 % of the products returned by the users were destructed. To eliminate such trouble and enhance the quality and reliability of ICs, consideration must be given to the following points when using ICs.

1. Cautions against Static Electricity

Due to the recent spread of chemical fiber and plastics, static electricity is generated everywhere in each of processes such as the storage and transportation of ICs, mounting ICs on PC boards, assembly of ICs, etc.

Though NEC's ICs for consumer use applications have been designed to withstand a static electricity of C=200 pF, V=200 V (4 μJ), attention should be paid to the following points when handling ICs:

(1) Since the containers of ICs shipped from NEC have undergone antistatic treatment, ICs can be stored or transported in the containers just as they are.

(2) Be sure to ground a human body, work table, dip solder bath, etc., when performing the acceptance inspection of ICs or mounting ICs on PC boards. To ground a human body, insert a resistor of about 1 MΩ on the human body to prevent electric shock. The rubber on belt conveyors must be subjected to antistatic treatment or sprayed with vapor by a humidifier to prevent generation of static electricity.

(3) The shipping containers for ICs mounted on PC boards must be of antistatic material. Otherwise, the containers must be subjected to antistatic treatment. It is recommended that the I/O terminals on a PC board or the power terminals be short-circuited to the GND terminal using a shorting bar.

(4) IN a dry season, it is recommended to humidity ICs which are liable to generate static electricity.

2. Caution in Soldering

Problems such as thermal shock, strain by stress and residual flux may arise when soldering ICs.

(1) Use rosin flux, and avoid use of any flux with high acidity or high alkalinity.

(2) Observe the soldering temperature and soldering time.

* By soldering iron: Solder in 3 seconds at 350 °C,
* By dip soldering: Solder in 10 seconds at 260 °C

The soldering location must be more than 1 mm off the IC body.

(3) Ground the soldering iron or dip solder bath through a resistor of about 1 MΩ to prevent leakage of the commercial AC power.

(4) Be sure to wash off the residual flux after soldering. The residual flux causes a leak between terminals or corrosion due to a collection of dust or moisture. Clean the residual flux under the following conditions:

* Cleaning solvent: Daiflon or Freon. (Chlorosene is not applicable to transparent resin such as LEDs. Never use chloric solvent such as trichlene.)
* Cleaning method: Wash off for about 2 minutes. Ultrasonic cleaning (f=28 kHz, P=15 W/ℓ, t ≤ 30 s) is possible for resin mold products.

3. Cautions in Storage

Adverse storage environment not only causes failures in appearance but also degrades the solderability and characteristics of ICs.

(1) The storage locations for ICs must satisfy the following conditions:

* Temperature: 5 to 30 °C
* Humidity : 70 % max.
* Must be free of harmful gases such as sulfurous acid gas, etc., and dust.

(2) Do not subject the IC to severe vibration or shock which may cause deformation of the container. Also pay attention not to apply a load to the IC by stacking the containers.

4. Cautions in Measurement

The reason that 30 to 40 % of the products returned by the customers as failures is considered to have been damaged due largely to errors in measurement. So, pay attention to the following points.

(1) Erroneous insertion of IC such as reverse insertion.

(2) Adjustment of components by a soldering iron while it is being energized.
(3) Insertion of the measuring instrument probe while it is being energized.

} The soldering iron or probe may contact peripheral components, power supply, GND terminal, etc., or may cause short-circuiting of the load.

(4) Incorrect ON/OFF sequence when multiple power supplies are used.

(5) Erroneous connection with measuring instrument or the solder bridge when power is applied.

5. Cautions in Mounting

When mounting an IC onto a PC board or a heat sink, take care not to exert undue force upon the IC body or leads.

(1) When forming a lead, firmly secure the lead at its base on the IC body side with a pair of pliers. Particularly, when a metal mold is to be used for bending a lead, take care so that no tensile stress is applied to the lead. (Tensile stress will vary depending on the type of package.)

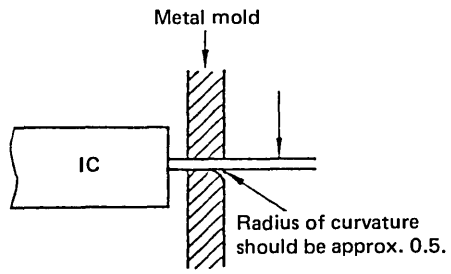
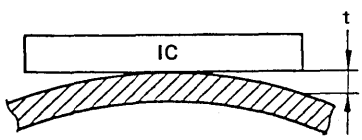


Fig. 1 Cautions in Lead Forming with Metal Mold

* Bend the lead by 90° at one time.
* Do not form the lead in a manner to widen the spacing between any two leads.
* The metal mold should not come in contact with the IC body even if tensile force is applied while bending the lead.

(2) When mounting a power IC onto a heat sink, pay attention to the following points.

* Warp of the heat sink and sagging of the mounting hole must not exceed: t= 0.05 mm.



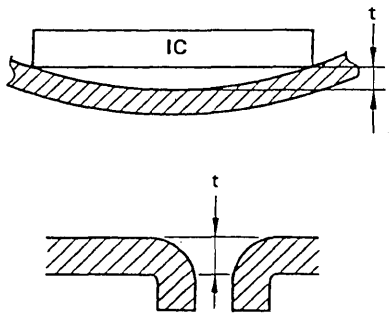


Fig. 2 Warp or Sagging of Heat Sink

* Use of binding head screws (JIS B 1101) is recommended. Avoid using countersunk head screws.
* Use a pneumatic or motor-driven screwdriver with a torque of 4 to 8 kg·cm and a rotational speed of 1 000 r.p.m.
* After mounting the power IC to the heat sink, solder the leads to the PC board.

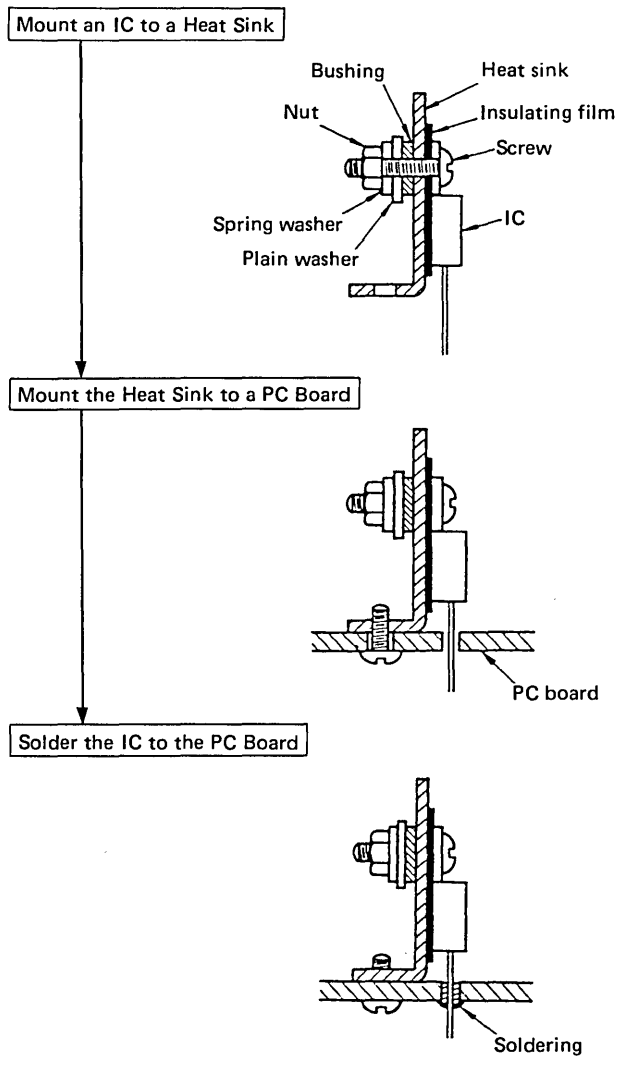


Fig. 3 Procedure for Mounting an IC to a Heat Sink and a PC Board

* The flatness of the mounting surface when the projection or riser of the rotation stopper is to be provided should not exceed 0.05 mm.

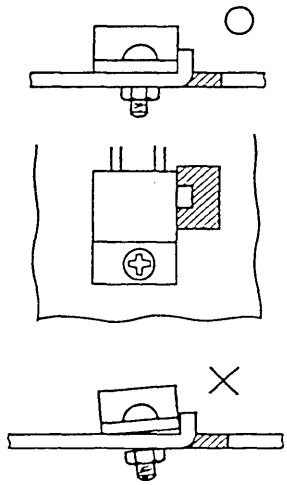


Fig. 4 Projection of Rotation Stopper

* The flatness of the IC surface to which the heat sink is mounted should not exceed 0.05 mm max. to prevent foreign matter such as burrs, cutting chips, etc., from entering between the IC and heat sink. Those will cause thermal resistance increase and resin mold crack.
* With the dual power supply system, be sure to insert an insulator film between the fin, flange, etc., of the IC and the heat sink. Since the fin, flange, etc., of the IC are biased to the lowest potential, the IC may be damaged if the heat sink is grounded.

TECHNICAL SYMBOLS AND TERMS USED IN INTEGRATED CIRCUITS FOR CONSUMER USE

BIPOLAR LINEAR ICs

AUDIO ICs

Symbol	Term
Absolute Maximum Ratings	
I_{CC}	Supply Current
I_{CCpeak}	Circuit Current
I_L	Lamp Driver Current
P_D	Package Dissipation
P_d	Power Consumption
T_{opt}	Operating Temperature
T_{stg}	Storage Temperature
V_{CC}	Supply Voltage
V_{IN}	Input Terminal Voltage
V_{in}	Input Voltage
V_L	Lamp Driver Terminal Voltage
$V^+ - V$	Supply Voltage
Electrical Characteristics	
AGC	AGC Range
AMR	Amplitude-Modulation Rejection Ratio
A_v	Voltage Gain
$A_v.M$	Voltage Gain (Demodulator)
A_{vo}	Voltage Gain (Open loop)
$A_v.P$	Voltage Gain (Pre amplifier)
$C_h.B$	Channel Balance
C_o	Output Capacitance
C_{in}	Input Capacitance
g_{in}	Input Conductance
g_o	Output Conductance
I_{CC}	Supply Current
$I_{CC(S)}$	Short Circuit Current
I_{out}	Quiescent Output Current
i_{opp}	Peak to peak Output Current
LAMP.ON	Stereo Indicator (Lamp ON)
LAMP.OFF	Stereo Indicator (Lamp OFF)
Mute ON	Mute ON
Mute OFF	Mute OFF
NF	Noise Figure
NL	Noise Level
P_d	Power Consumption
P_o	Output Power
R_i	Input Resistance
R_{in}	Input Resistance
r_o	Output Resistance

Symbol	Term
$SCA._{Rej}$	SCA Rejection Ratio
$S_{ep.}$	Stereo Channel Separation
S/N	Signal to Noise Ratio
T.H.D.	Total Harmonic Distortion
v_{HAM}	Power Supply Ripple Rejection
V_I	Stabilized Terminal Voltage
V_i	Maximum Input Signal for AM
V_n	Output Noise Voltage
V_{nin}	Equivalent Input Noise Voltage
V_{OFF}	Input Offset Voltage
V_{OFF}	Output Transient Voltage (SW OFF)
V_{OM}	Maximum Output Voltage
V_{ON}	Output Transient Voltage (SW ON)
V_{out}	Recovered Audio Output Voltage
$V_{o(sat)}$	Output Saturation Voltage
Z_i	Input Impedance

TV ICs

Symbol	Term
Absolute Maximum Ratings	
E_{in}	Input Signal Voltage
E_p	Gate Pulse Input Voltage
e_A	Reference Subcarrier Input Voltage
e_C	Chroma Input Voltage
e_Y	Luminance Signal Input Voltage
I_{ax}	Senser Terminal Input Current
I_{bx}	Indicator Circuit Output Current
I_{CC}	Supply Current
I_{CX}	Senser Circuit Current
$I_{O(OSC)}$	OSC Output Current
I_Z	Supply Current
P_d	Power Consumption
P_T	Total Power Dissipation
R_L	Load Resistance
T_{opt}	Operating Temperature
T_{stg}	Storage Temperature
V_{ax}	Senser Terminal Input Voltage
V_{CC}	Supply Voltage
$V_{CC(L)}$	Indicator Circuit Supply Voltage
V_{CX}	Selector Circuit Supply Voltage
V_{BLANK}	Blanking Pulse Voltage
V_i	Input Voltage
V_{iBURST}	Burst Amp. Input Voltage
V_{iOSC}	OSC Input Voltage
$V_{i(SYNC)}$	Synchro Separator Input Voltage
V_{i1BP}	1st Band Pass Circuit Input Voltage
V_{i2BP}	2nd Band Pass Circuit Input Voltage
V_R	Remote Control Input Voltage
Electrical Characteristics	
AMR	Amplitude-Modulation Rejection Ratio
A_vAF	AF Voltage Gain
A_vDC	DC Voltage Gain
A_vIFI	IF Amp. Voltage Gain
A_v1	1st Band pass Amp. Voltage Gain
A_v2	2nd Band pass Amp. Voltage Gain
A_vBURST	Burst Amplifier Voltage Gain
A_vOSC	OSC Circuits Voltage Gain
BW_{DET}	Detector Circuit Band Wides
BW_{IF}	IF Amp. Band Wides
C_{in}	Input Capacitance
E_a	A.C.C. Range
E_b	Burst Output Voltage
E_C	Maximum Chroma Output Voltage
E_{ODC}	Color Difference Terminal DC Voltage

Symbol	Term
ΔE_{ODC}	E_{ODC} Difference Between any two Output Terminals
$\frac{\delta E_{ODC}}{\delta T}$	Temperature Coefficient of E_{ODC}
E_{OI}	Color Difference Output Voltage
E_{Omax}	Maximum Color Difference Output Voltage
E_{G-Y}	G-Y Terminal Demodulation Output Voltage
E_{R-Y}	R-Y Terminal Demodulation Output Voltage
f_{HOLD}	Maximum Hold Frequency
Hf_{OSC}	Holizontal OSC Frequency
f_P	APC Pull-in Range
f_{PULL}	Maximum Pull-in Frequency
I_{CC}	Supply Current
I_{KB}	Killer Current (B/W)
I_{KC}	Killer Current (Color)
i_{out}	OSC Circuits Maximum Output Current
NF	Noise Figure
P_d	Power Consumption
P_G	Power Gain
$I_{b(OFF)}$	Indicator Terminal Leak Current
$I_{C(OFF)}$	Selector Output Terminal Leak Current
R_{AGC}	AGC Range
R_{in}	Input Resistance
R_{out}	Output Resistance
r_z	Operating Resistance
$V_{b(sat)}$	Indicator Circuits Saturation Voltage
$V_{C(ON)}$	Select Output Terminal Saturation Voltage
$\Delta V_{C(ON)}/\Delta T$	Select Output Terminal Temperature Coefficient
$V_{i(lim)}$	Input Limiting Voltage
V_{OAF}	Recovered Audio Output Voltage
V_{OAF2}	Audio Amplifier Maximum Output Voltage
V_{OSCmax}	Maximum OSC Output Voltage
V_Z	Regulated Voltage
$\Delta V_Z/\Delta T$	Regulated Voltage Temperature Coefficient
v_1	Input Signal Level
V_{OAFC}	AFC Output Voltage
α_{B-Y}	B-Y Relative Output Phase
α_{G-Y}	G-Y Relative Output Phase
α_{R-Y}	R-Y Relative Output Phase
β	Burst Frequency Control Sensitivity
T.H.D.	Total Harmonic Distortion
e_C	Carrier Color Signal Input Voltage
$e_{O(SYNC)}$	Synchronous Separation Output Voltage
μ	Phase Detector Sensitivity
θ_{DC}	Output DC Voltage Temperature Coefficient

BIPOLAR DIGITAL ICs

Symbol	Term
Absolute Maximum Ratings	
I_F	Forward Current
I_O	Output Current
T_{opt}	Operating Temperature
T_{stg}	Storage Temperature
V_{CC}	Supply Voltage (Positive)
V_{EE}	Supply Voltage (Negative)
V_I	Input Voltage
V_O	Output Voltage
V_R	Reverse Voltage

Symbol	Term
Recommended Operating Conditions	
N	Funout
t_f	Fall Time
Tstg	Storage Temperature
V_{CC}	Supply Voltage
V_{EE}	Supply Voltage
V_I	Input Voltage
V_{IH}	High Level Input Voltage
V_{IL}	Low Level Input Voltage
V_O	Output Voltage
Electrical Characteristics	
f_{max}	Maximum Clock Frequency
I_{CC}	Supply Current
I_{CCH}	Supply Current (Output High)
I_{CCL}	Supply Current (Output Low)
I_{IH}	High Level Input Current
I_{IL}	Low Level Input Current
I_{OFF}	Output Low Current
I_{OS}	Short Circuit Output Current
I_R	Reverse Current
t_{AA}	Address Access Time
t_{ACE}	Chip Enable Access Time
t_{pHL}	Propagation Delay Time (High to Low Level Output)
t_{pLH}	Propagation Delay Time (Low to High Level Output)
V_F	Forward Voltage
V_{IC}	Input Clamp Voltage
V_{OH}	High Level Output Voltage
V_{OL}	Low Level Output Voltage
V_R	Reverse Voltage

MOS DIGITAL ICs

MOS ICs

Symbol	Term
Absolute Maximum Ratings	
I_O	Output Current
T_{opt}	Operating Temperature
T_{stg}	Storage Temperature
V_{BB}	Supply Voltage
V_{CC}	Supply Voltage
V_{DD}	Supply Voltage
V_{GG}	Supply Voltage
V_I	Input Voltage
V_O	Output Voltage
$V\phi$	Clock Voltage
Recommended Operating Conditions	
C_{AC}	External Capacitance (Auto Clear)
C_{CR}	External Capacitance (Clock OSC)
C_L	Load Capacitance
f_{CP}	Count Pulse Frequency
f_ϕ	Clock Pulse Frequency
N	Funout
R_{AC}	External Resistance (Out Clear)
R_{CR}	External Resistance (Clock OSC)
R_L	Load Resistance
t_{CT}	Transfer Time of Count Pulse
$t_{d(\phi)}$	Clock Pulse Difference
$t_{f(CP)}$	Fall Time of Count Pulse
t_H	Hold Time
t_r (CP)	Rise Time of Count Pulse
$t_{w(CL)}$	Clear Pulse Width
$t_{w(CP)}$	Input Pulse Width
$t_{W(R)}$	Reset Pulse Width
$t_{W(T)}$	Transfer (Latch Input) Pulse Width
$t_{W(\phi)}$	Clock Pulse Width
V_{DD}	Drain Supply Voltage
V_{GG}	Gate Supply Voltage
V_{IH}	High Level Input Voltage
V_{IL}	Low Level Input Voltage
V_R	Reset Voltage
V_{ss}	Supply Volttage
$V_{\phi H}$	High Level Clock Voltage
$V_{\phi L}$	Low Level Clock Voltage
$V_{(CL)}$	Clear Voltage
Electrical Characteristics	
C_{DS}	Capacitance
C_{GS}	Capacitance
C_I	Input Capacitance
C_O	Output Capacitance
C_{SS}	Capacitance
C_ϕ	Clock Input Capacitance

Symbol	Term
f_{CP}	Operating Frequency
f_{max}	Maximum Count Pulse Frequency
f_{OSC}	Scan OSC Frequency
f_{SI}	Scan Input Frequency
f_ϕ	Clock OSC Frequency
I_{DD}	Supply Current
I_{GG}	Supply Current
I_{IH}	High Level Input Current
I_{IL}	Low Level Input Current
I_{OFF}	Output OFF Current
I_{ON}	Output ON Current
I_{SS}	Supply Current
$I_{\phi H}$	High Level Clock Input Current
$I_{\phi L}$	Low Level Clock Current
P_d	Power Consumption
t_{pHL}	Propagation Delay Time (High to Low Level Output)
t_{pLH}	Propagation Delay Time (Low to High Level Output)
V_{IH}	High Level Input Voltage
V_{IL}	Low Level Input Voltage
V_{OH}	High Level Output Voltage
V_{OHD}	High Level Output Voltage (A, B, C, D, SD)
V_{OHT}	High Level Output Voltage at Digit Output
V_{OL}	Low Level Output Voltage (A, B, C, D, SD)
V_{OLD}	Low Level Output Voltage at Digit Output
V_{OLT}	Low Level Output Voltage at Digit Output
$V_{\phi H}$	High Level Clock Input Voltage
$V_{\phi L}$	Low Level Clock Input Voltage

CMOS ICs FOR CLOCKS AND WATCHES

Symbol	Term
Absolute Maximum Ratings	
T_{opt}	Operating Temperature
T_{stg}	Storage Temperature
V_{DD}-V_{SS}	Supply Voltage
V_{SH}	Supply Voltage
V_{SS}	Supply Voltage

Symbol	Term
Electrical Characteristics	
I_n	ICD Common & Each Segment Output Current
I_p	Boosting Drive Frequency Output Current
I_O	Output Current
I_{SH}	Circuit Current
I_{SS}	Circuit Current
t_{wo}	Output Pulse Width
V_{DD}-V_{SH}	Operating Voltage
V_{DD}-V_{SS}	Operating Voltage
V_{DD}	Operating Voltage
V_r	Time Base Operating Voltage
$\lvert\Delta f/fo\rvert$	Oscillator Frequency Stability

ARRAYS

Symbol	Term
Absolute Maximum Ratings	
I_B	Base Current
I_C	Collector Current
I_D	Drain Current
I_E	Emitter Current
I_{FM}	Peak Forward Current
$I_{F\ surge}$	Surge Forward Current
I_O	Average Rectified Output Current
P	Power Dissipation
P_C	Collector Dissipation
P_D	Allowable Power Dissipation
P_T	Total Power Dissipation
T_j	Junction Temperature
T_{opt}	Operating Temperature
T_{stg}	Storage Temperature
V_{CBO}	Collector to Base Voltage
$V_{C\text{-}C}$	Collector to Collector Voltage
V_{CEO}	Collector to Emitter Voltage
V_{CER}	Collector to Emitter Voltage
$V_{C\text{-}U}$	Collector to Substrate Voltage
V_{DSO}	Drain to Source Voltage
V_{DSX}	Drain to Source Voltage
V_{EBO}	Emitter to Base Voltage
V_{ECR}	Emitter to Collector Voltage
V_{GDO}	Gate to Drain Voltage
V_{GSO}	Gate to Source Voltage
V_R	Reverse Voltage
V_{RM}	Peak Reverse Voltage
Electrical Characteristics	
C_{is}	Gate Input Capacitance
C_{iss}	Small-Signal Short Input Capacitance
ΔC_{iss}	Input Capacitnce Difference
C_{ob}	Output Capacitance
C_{rss}	Small-Signal Short-Circuit Reverse Transfer Capacitance
C_t	Capacitance
C_{TE}	Emitter Transition Capacitance
e_n	Equivalent Input Noise Voltage
f_T	Gain Bandwidth Product
g_m	Mutual Conductance
Δgm	Mutual Conductance Difference
h_{FC}	DC Reverse Current Gain
h_{FE}	DC Current Gain
$h_{FE(S)}/h_{FE(L)}$	DC Current Gain Ratio
I_{CBO}	Collector Cutoff Current
I_{DSS}	Drain Current

Symbol	Term
ΔI_{DSS}	Drain Current Difference
$I_{DSS(S)}/I_{DSS(L)}$	Drain Current Ratio
I_{EBO}	Emitter Current
I_{GSS}	Gate to Source Reverse Current
I_R	Reverse Current
NF	Noise Figure
NL	Noise Level
$R_{e(hie)}$	Real Part of Small-Signal Short-Circuit Input Impedance
R_{off}	Drain to Source Off Bulk Resistance
R_{on}	Drain to Source On Bulk Resistance
ΔR_{on}	Drain to Source On Bulk Resistance Difference
r_{on}	SW ON Operating Resistance
t_{fr}	Forward Recovery Time
t_{off}	Turn-Off Time
t_{on}	Turn-On Time
t_{rr}	Reverse Recovery Time
t_{stg}	Storage Time
$V_{BE(sat)}$	Base Saturation Voltage
ΔV_{BE}	Base to Emitter Voltage Difference
$V_{CE(sat)}$	Collector Saturation Voltage
$V_{EC(sat)}$	Emitter Saturation Voltage
V_F	Forward Voltage
ΔV_G	Gate Voltage Difference
$V_{GS(off)}$	Cutoff Voltage
$\Delta V_{GS(off)}$	Cutoff Voltage Difference
V_{IO}	Input Offset Voltage
$V_{IO}/\Delta T$	Temperature Coefficient of Input Offset Voltage
V_{pi}	Offset Voltage Difference
$\Delta V_{pi}/\Delta T$	Temperature Coefficient of Offset Voltage
V_{th}	Threshold Voltage
ΔV_{th}	Threshold Voltage Difference
$\lvert Y_{fs}\rvert$	Forward Transfer Admittance
$\lvert Y_{fs(S)}\rvert/\lvert Y_{fs(L)}\rvert$	Forward Transfer Admittance Ratio

RELIABILITY AND QUALITY CONTROL SYSTEM FOR NEC ELECTRON DEVICES

1. Organization and Functions of Electron Device Group

NEC started its business as a manufacturer of telephones and switchboards and has today grown into an all-embracing manufacturer in the fields of "Communications and Electronics", with the following 4 groups of products as its mainstays.

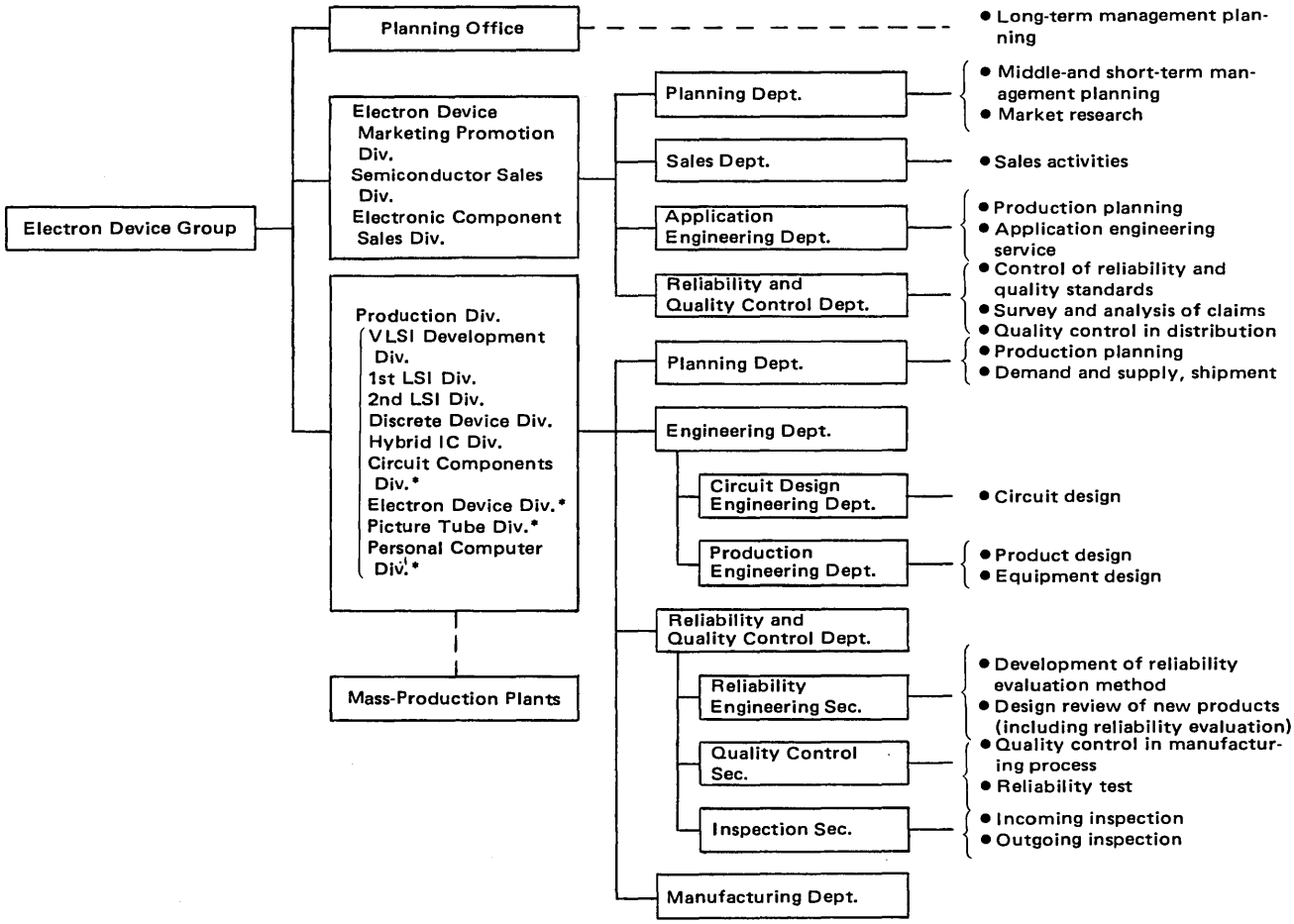
(1) Communications (microwave communications systems, broadcasting systems, PABXs, facsimile systems, etc.)

(2) Information processing and industrial systems (computer systems, industrial systems, medical equipment systems, etc.)

(3) Electron devices (transistors, diodes, ICs, capacitors, various electron tubes, etc.)

(4) Home electronics (TV sets, microwave ovens, electric refrigerators, air conditioners, lighting fixtures, etc.)

The business activity of NEC now ranges from domestic to overseas areas and is now highly recognized as an international enterprise. The Electron Device Group, one of the four mainstays described above, is engaged in the manufacturing and sales of electron devices. The Group serves as the source for producing the high reliability and quality of NEC products by the other three business groups. The following chart summarizes the organization and functions of the Electron Device Group.



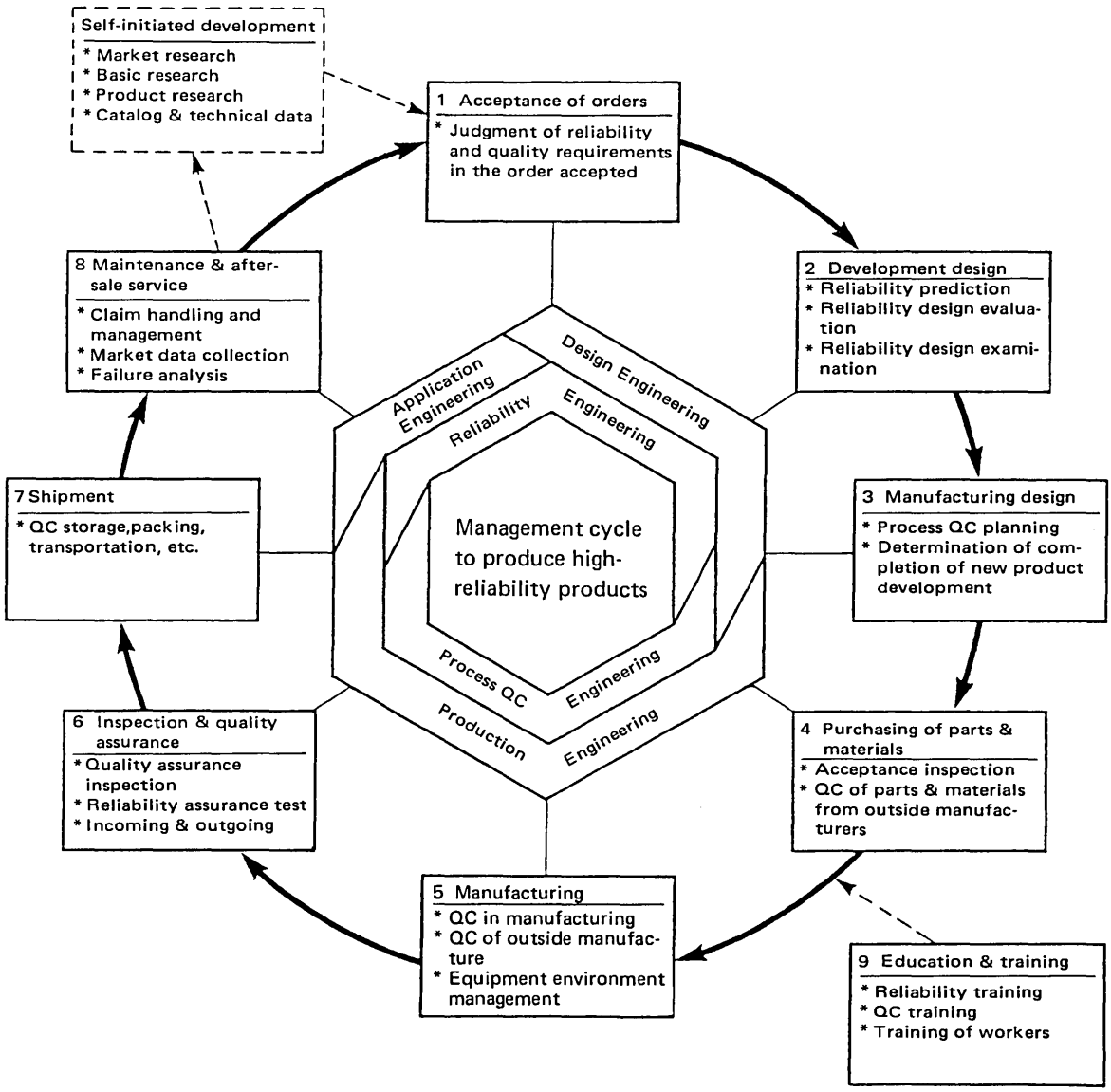
Notes: 1. Mass-production plants are engaged in production and quality control activities under the supervision of each production division.

2. The reliability and quality control system for the production division marked, with an asterisk is basically included in this manual with the exception of paragraph 3 and thereafter.

2. Basic Concept of Reliability and Quality Control

The reliability and quality control of NEC's semiconductor products is intended to perform the incorporation of reliability in each of the processes from market research and grasp of users' requirements to development design and manufacturing design, the quality control in each of the processes from the purchasing of materials and parts to be used to the manufacturing of products, the direct assurance of reliability and quality by inspections and reliability tests, shipment control and after-sale services to customers, under an integrated system. NEC is making every effort to offer the products which meet customers' expectations, by operating a logical control system so that the reliability and quality of each product is compatible with its price.

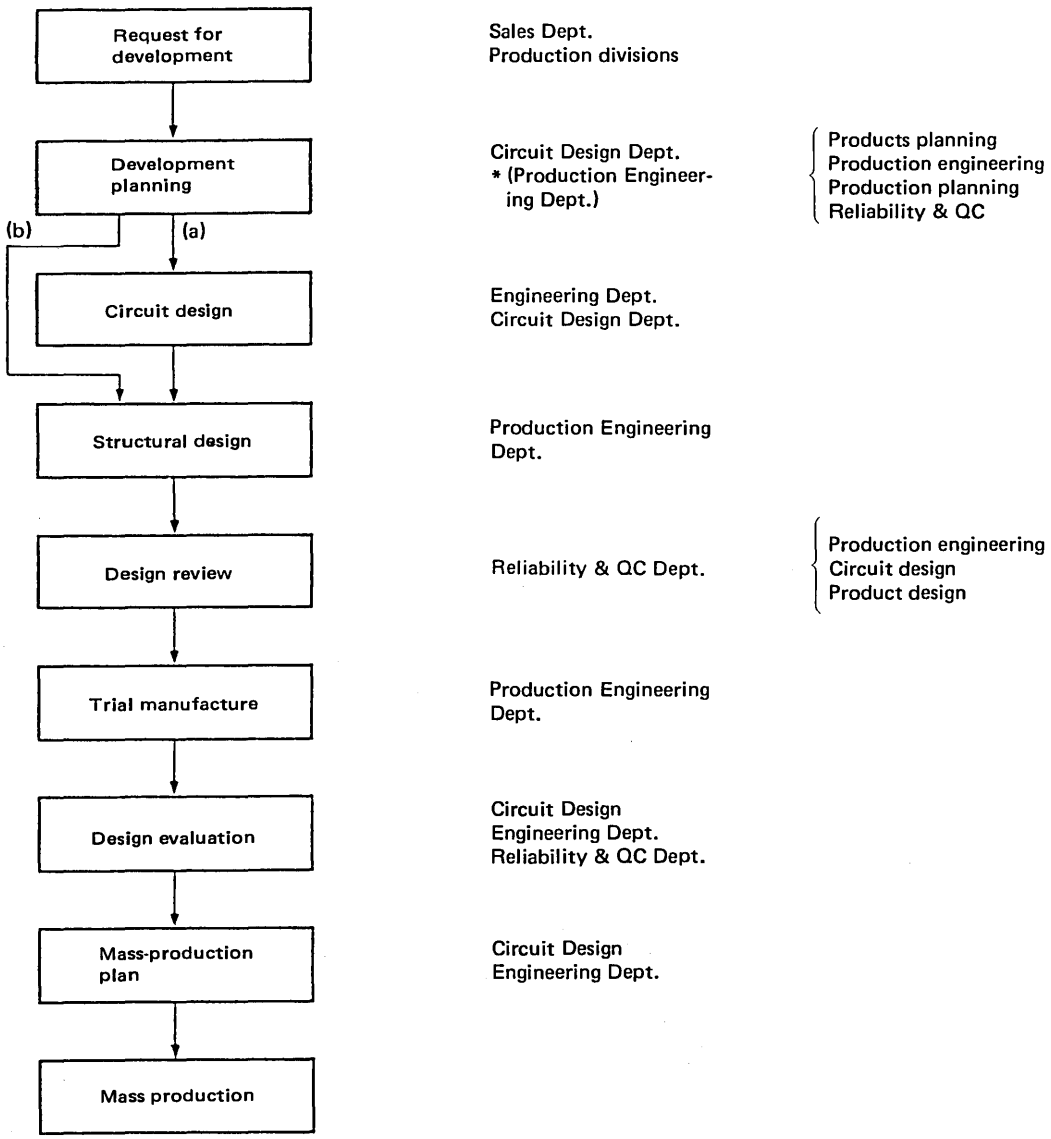
This system at NEC is conceptionally illustrated in the following diagram.



3. New Product Development Procedure

To develop a new product intended for a specific application, it is necessary first to accurately grasp the required reliability and quality of the new product, in addition to the required functions, performance, price and quantity of the new product, and the date the new product is to be placed on the market. These factors then must be incorporated into the product design.

With these factors thoroughly studied, NEC will project a development plan, and carry out the design, trial manufacture, and evaluation of the new product based on the development plan. NEC will enter the mass production of the new product only after it has been ascertained that a satisfactory result is attainable. The following diagram shows the new product development procedure implemented by NEC.



NOTES: (a) Flow for development of ICs.
(b) Flow for development of semiconductors and others.
* indicates a development planning department for semiconductors.

4. Quality Control in Manufacturing Process

NEC manufactures and markets semiconductor products under the control system mainly aimed at "incorporating high reliability and quality into the products", by thoroughly grasping the users' requirements and operating environments of products and reflecting them in the product design to achieve the desired inherent reliability.

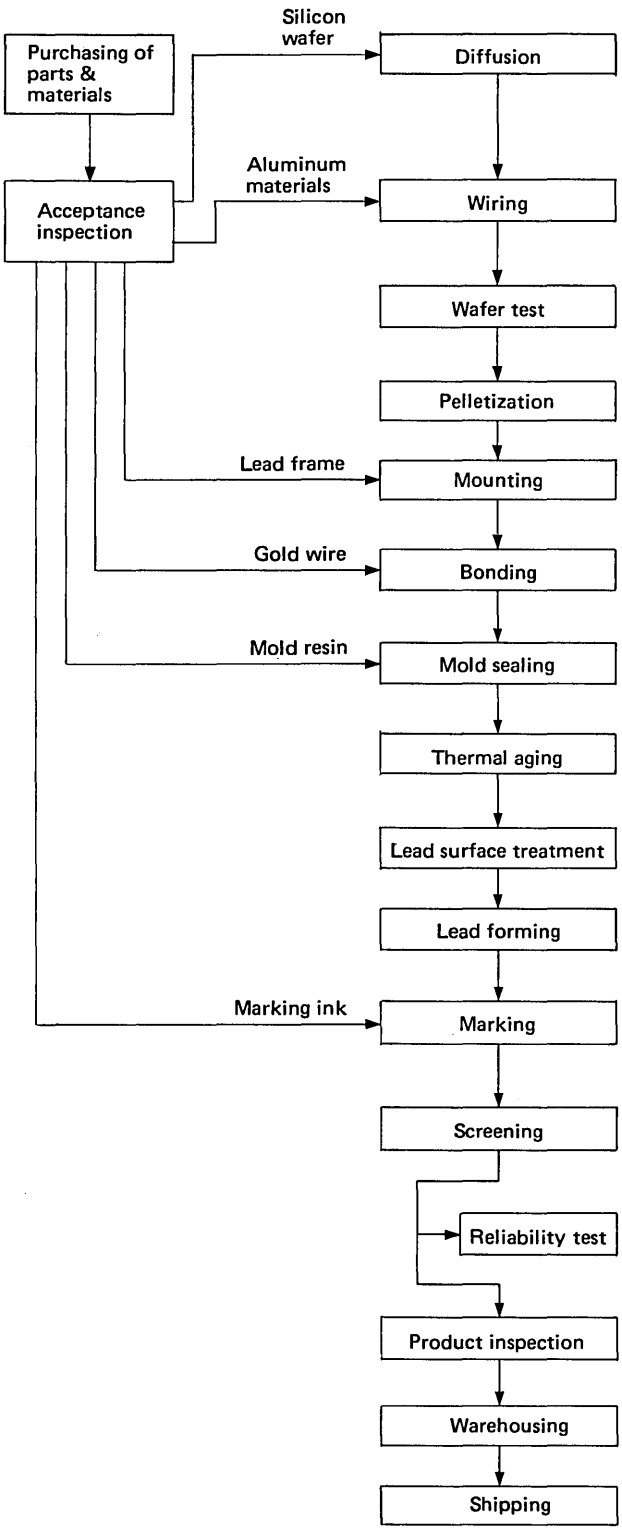
To realize the reliability and quality of a product intended in the product design, a system to control manufacturing must be such that the cause of failure due to nonuniformity in each manufacturing process may be eliminated before it develops into a failure.

Therefore, in the manufacture of its products, NEC gives importance to the quality control of such factors as parts, materials, semifinished products, manufacturing equipment, manufacturing environments, etc., which govern the reliability and quality of each product. Furthermore, with a checking process during each manufacturing process, semiconductor products being fabricated in each process are inspected at optimum intervals for control items important in quality control.

4.1 Reliability and Quality Control of NEC's Linear (Plastic Molded Package) ICs for Consumer Use Applications

As previously mentioned, NEC manufactures and markets semiconductor products under the control system mainly aimed at "incorporating reliability and quality (inherent reliability) into the products." Linear IC (plastic molded package) products for consumer use are manufactured under the control system which places an emphasis on the reliability and quality control in each manufacturing process to realize the reliability and quality intended in the product design. In addition, the parts, materials, semifinished products, manufacturing equipment, manufacturing environments for these products are subjected to quality control under the optimum conditions, as the important factors governing the reliability and quality of the products. The following table contains an example of manufacturing process control flowchart of linear IC (plastic molded package) products for consumer use.

Manufacturing Process Control Flowchart of Linear IC (Plastic Molded Package) Products for Consumer Use



Process	Control items	Purpose of control
Diffusion	Specific resistance Sheet resistance h_{FE}, breakdown voltage Appearance	To secure the required breakdown voltage. To grasp the condition of diffusion. To secure the basic characteristics. To check for proper photo etching.
Wiring	Aluminum layer thickness Appearance	To secure the standard layer thickness. To check for proper photo etching.
Wafer test	Electrical characteristics (100 % screening)	To eliminate defects in electrical characteristics.
Pelletization	Appearance	To check for proper pelletization.
Mounting	Appearance	To check for proper mounting.
Bonding	Appearance Tensile strength	To check for proper bonding. To prevent breakage of wires.
Mold sealing	Appearance	To check for proper sealing.
Thermal aging	Temperature, time	To stabilize the sealing resin. To screen latent failures.
Lead surface treatment	Appearance Dimensions	To check for proper lead surface treatment.
Lead forming	Appearance Dimensions	To check for proper lead forming.
Marking	Appearance Marking strength	To check for proper marking. To secure the required marking strength.
Screening	Electrical characteristics (100 % screening)	To eliminate defects in electrical characteristics.
Reliability test	Sevice life test Environmental test	To confirm reliability.
Product inspection	Electrical characteristics Appearance	To confirm electrical characteristics. To check for proper appearance.
Warehousing		
Shipping		

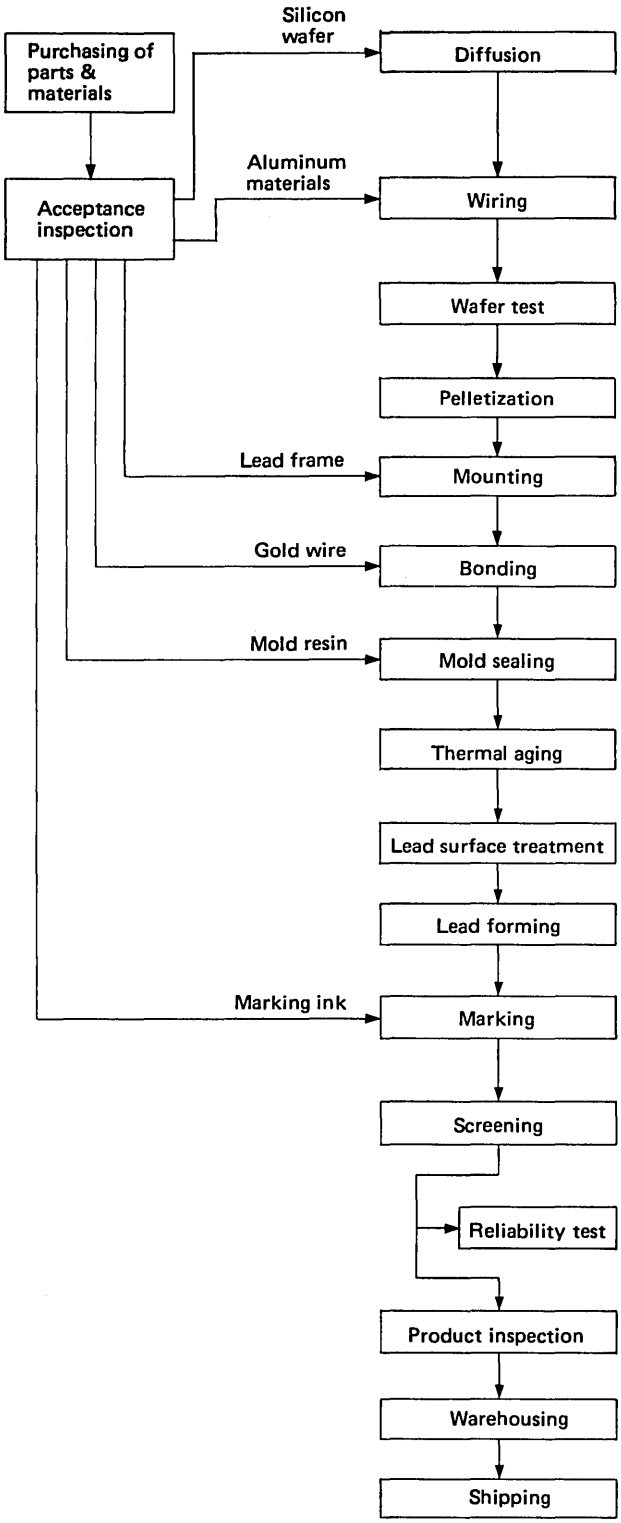
Note: Control items and frequency of inspection

To realize the desired reliability and quality, the cause of failure due to non-uniformity in each manufacturing process must be eliminated before it develops into a failure. With a checking process during each manufacturing process, semifinished products being fabricated in each process are inspected at optimum intervals for the control items important in quality control.

4.2 Quality Control of NEC's CMOS LSI (Plastic Molded Package) Products for Watches

Similar to the linear IC products described in Section 4.1 above, CMOS LSI (plastic molded package) products for watches are manufactured under the control system which places an emphasis on the reliability and quality in each manufacturing process to realize the reliability and quality intended in the product design. In addition, the parts, materials, semifinished products, manufacturing equipment, and manufacturing environments for these products are subjected to quality control under the optimum conditions, as the important factors governing the reliability and quality of the products. The following table contains an example of manufacturing process control flowchart of CMOS IC (plastic molded package) products for watches.

Manufacturing Process Control Flowchart of CMOS LSI (Plastic Molded Package) Products for Watches



Process	Control items	Purpose of control
Diffusion	Specific resistance, gate layer thickness	To secure the required breakdown voltage.
	Sheet resistance	To grasp the condition of diffusion.
	V_{th}	To secure the basic characteristics.
	Appearance	To check for proper photo etching.
Wiring	Aluminum layer thickness	To secure the standard layer thickness.
	Appearance	To check for proper photo etching.
Wafer test	Electrical characteristics (100 % screening)	To eliminate defects in electrical characteristics.
Pelletization	Appearance	To check for proper pelletization.
Mounting	Appearance	To check for proper mounting.
Bonding	Appearance	To check for proper bonding.
	Tensile strength	To prevent breakage of wires.
Mold sealing	Appearance	To check for proper sealing.
Thermal aging	Temperature, time	To stabilize the sealing resin.
		To screen latent failures.
Lead surface treatment	Plating thickness	To secure the standard plating thickness.
Lead forming	Appearance	To check for proper lead forming.
Marking	Appearance	To check for proper marking.
	Marking strength	To secure the required marking strength.
Screening	Electrical characteristics (100 % screening)	To eliminate defects in electrical characteristics.
Reliability test	Service life test	To confirm reliability.
	Environmental test	
Product inspection	Electrical characteristics	To confirm electrical characteristics.
	Appearance	To check for proper appearance.
Warehousing		
Shipping		

Note: Control items and frequency of inspection

To realize the desired reliability and quality, the cause of failure due to non-uniformity in each manufacturing process must be eliminated before it develops into a failure. With a checking process during each manufacturing process, semifinished products being fabricated in each process are inspected at optimum intervals for the control items important in quality control.

5. Confirmation of Reliability and Quality

The initial characteristic test and reliability test are conducted in the final stage of the manufacturing processes to check if the reliability and quality intended in the product design have been incorporated through the appropriate manufacturing process control.

5.1 Initial Characteristic Test

The initial characteristic test (i.e., product inspection) is conducted through sampling inspections of all lots to check if the appearance and electrical characteristics of the screened products satisfy the prescribed standards. Inspection items and sampling inspection method will vary depending on the features of the product to be inspected and other factors. The following table shows an example of initial characteristic test to be conducted for linear IC (plastic molded package) products for consumer use.

An Example of Initial Characteristic Test for Linear IC (Plastic Molded Package) Products for Consumer Use

Classification	Item	Sampling inspection method*		
		LTPD	Sample size	Acceptance number
Major defect	Open, short, defective function	1 %	231	0
DC characteristic	As per individual specification	3 %	129	1
AC characteristic	As per individual specification	7 %	75	2
Major failure in appearance	Ruptured or cracked resin, broken lead, unsoldered plating, no marking	1 %	231	0
Medium failure in appearance	Improperly molded or contaminated resin, bent or discolored lead	3 %	221	3
Minor failure in appearance	Flawed, blistered, discolored resin, bent or twisted lead, illegible marking	7 %	75	2

*: As per MIL-M-38510, Sampling Inspection Table.

5.2 Reliability Test

Referring to such standards as JIS C 7021, MIL-STD-750, JIS C 7022, MIL-STD-883, etc., a reliability test is periodically conducted through sampling inspections with emphasis placed on the life test under accelerated operation or the life test under high temperature and bias conditions at the maximum ratings, to check if the environmental resistance, service life, mechanical strength, etc., of each product satisfy the prescribed standards. Inspection items and sampling inspection method will vary depending on the features of the product to be inspected and other factors. The following tables show an example of failure criteria in the reliability test, and an example of particulars of the reliability test of linear IC (plastic molded package) products for consumer use.

An Example of Failure Criteria in Reliability Test for Linear IC (Plastic Molded Package) Products for Consumer Use.

Test item	Failure criteria			
	Item	Minimum	Maximum	Unit
Soldering heat resistance Temperature cycling Thermal shock Shock Vibration (variable frequency) Contact acceleration High temperature storage Low temperature storage High temperature with bias High temperature and high humidity storage PCT (Pressure cooker test) Surge test High temperature, high humidity with bias	Power supply voltage	L × 0.8	U × 1.2	V
	As per individual specification	As per individual specification	As per individual specification	—
Terminal strength against bending	Appearance of leads	Must be free of rupture and looseness		
Solderability	Appearance of leads	95 % or more solder must remain in the soldered area.		

NOTE: U : Upper-limit value in the product specification
L : Lower-limit value in the product specification

An Example of Reliability Test for Linear IC (Plastic Molded Package) Products for Consumer Use

Sub-group	Test Item	Related Test Methods			Test conditions	Sample size	Acceptance number
		JIS C 7022	MIL-STD-883	IEC Pub 68			
1	Solderability	A–2	2003	T	Dip the samples into noncorrosive flux for 5 to 10 s, and then into molten solder at 230 °C ± 5 °C for 5 ± 1 s. (The samples should be dipped into and pulled out of molten solder at 2.5 ± 0.5 cm/s.) Next, clean the samples to wash off the solder flux in alcohol and check each sample for proper solder adhesion.	5	0
2	Soldering heat resistance	A–1 Condition A	–	T_b Condition A	Dip the samples into molten solder at 260 °C ± 5°C for 10 ±1 s.	22	0
	Temperature cycling	A-4	1010	Na	Place the samples in a constant temperature oven at a low temperature (T_{stg} min.) for 30 minutes min., and then in a constant temperature oven at a high temperature (T_{stg} max.) for 30 minutes min. Repeat this procedure for 5 times (i.e., 5 cycles).		
	Thermal shock	A-3 Condition A	1011	Nc	Immerse the samples in city water at 100^{+0}_{-5} °C for 5 minutes min. and then in city water at 0^{+5}_{-0} °C for 5 minutes min. Repeat this procedure 5 times (i.e., 5 cycles).		
3	Shock *	A-7 Condition F	2002 Condition B	Ea	Secure each sample on a testing device and expose the sample to a shock of half sine wave with pulse duration of 0.5 ms at an acceleration of 14 700 m/s² max. (1 500 G's) in X, Y, Z directions, each 3 times.	22	0
	Vibration* (variable vibration frequency)	A–10	2007 Condition A	Fc	Secure each sample on a testing device and expose the sample to a vibration of sine wave at an acceleration of 196 m/s² (20 G's) and a sweep frequency of 100 to 2 000 to 100 Hz for 4 minutes, in X, Y, Z directions, each 4 times.		
	Constant acceleration*	A–9	2001	Ga	Secure each sample on a testing device and expose the sample to a centrifugal acceleration of 58 860 m/S² (6 000 G's), in X, Y, Z directions, each for 1 minute.		
4	Terminal strength (bending)	–	2004 Condition B_2	Ub	Secure each sample on a testing device, bend the sample 90 ° while applying the specified load to its leads and return it to the original position. Repeat this procedure 3 times for any of the 3 leads.	5	0
5	High temperature storage	B–3	1008	Ba	Perform the service life test for 1 000 hours while leaving the samples in the constant temperature oven at the maximum storage temperature (T_{stg} max.)	20	0
6	Low temperature storage	B–4	–	Aa	Perform the service life test for 1 000 hours while leaving the samples in the constant temperature oven at the minimum storage temperature (T_{stg} min.)	20	0
7	High temperature with bias	B–1	1005 Conditions A, B and C	–	Perform the service life test while applying power to the sample for 1 000 hours at the specified ambient temperature which causes the junction temperature (T_j) to become the maximum junction temperature (T_j max.).	20	0
8	High temperature and high humidity storage	B-5 Condition B	–	Ca	Perform the service life test at a storage temperature of 60 °C and humidity of 90 % RH.	20	0
9	PCT* (Pressure cooker test)	–	–	–	Expose the sample to a water vapor at 125 °C and 2.3 atm. for 24 hours.	22	0
10	Surge test*	–	–	–	Discharge the electric charge stored in a 200 pF capacitor with 200 V applied across the terminals, in both positive and negative directions, respectively one time.	20	0
11	High Temperature, high humidity with bias*	B-5 Condition C (voltage applied)	–	–	Perform the service life test for 500 hours while leaving the samples in a constant temperature oven at a temperature of 85 °C and humidity of 85^{+5}_{-10} % RH and by applying a voltage under the specified condition to each sample.	20	0

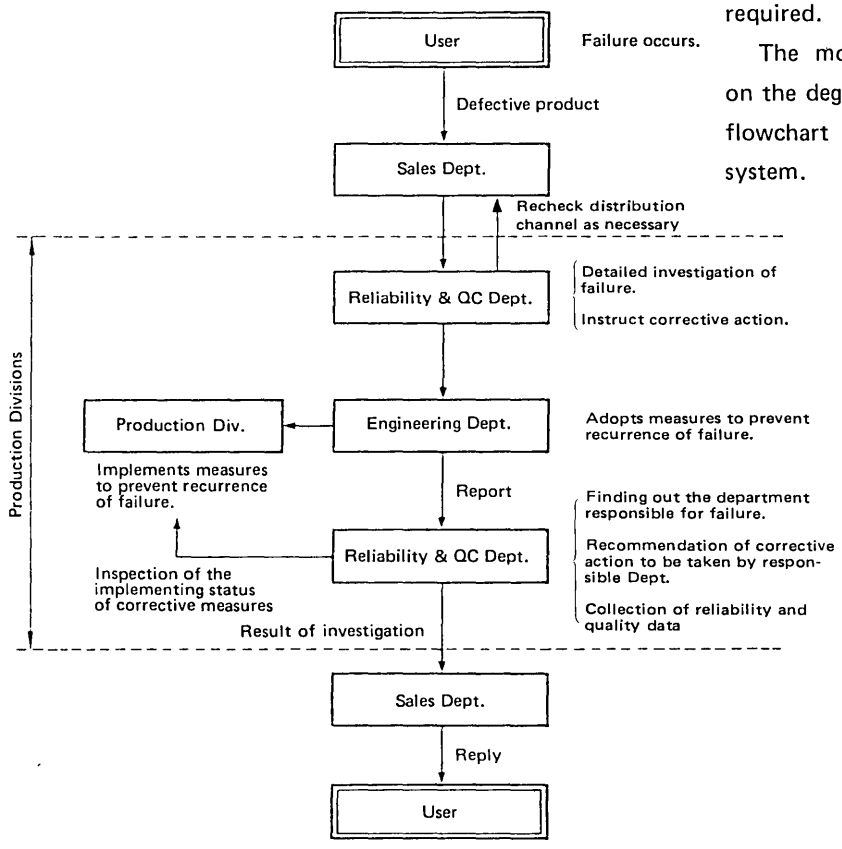
Note: Test item marked with an asterisk is performed in the Type Test and thus is not subject to the periodical reliability test.

6. Procedure for Processing Defective Products and Requests for Investigation and Analysis

Information from the market on the quality of products after shipment is of importance and indispensable to enhance the reliability and quality of our products. NEC focuses an extensive effort on the investigations of defective products and the feedback of the results of analyses of such investigations to users, since these actions are part of the after-sale service to customers and at the same time, information obtained from these actions provide the direct guideline for further improvement in the reliability and quality of our products.

The results of the investigations and analyses of defective products conducted as well as based on requests from the users are reported to the users to gain their full understanding, and are also used by NEC to improve the reliability and quality of its products. We at NEC examine in detail the correlation between the data thus obtained from the field and the information generated within NEC such as process quality data, inspection reports, and reliability test data.

The following flowchart shows the flow of processing an investigation and analysis request from a user.



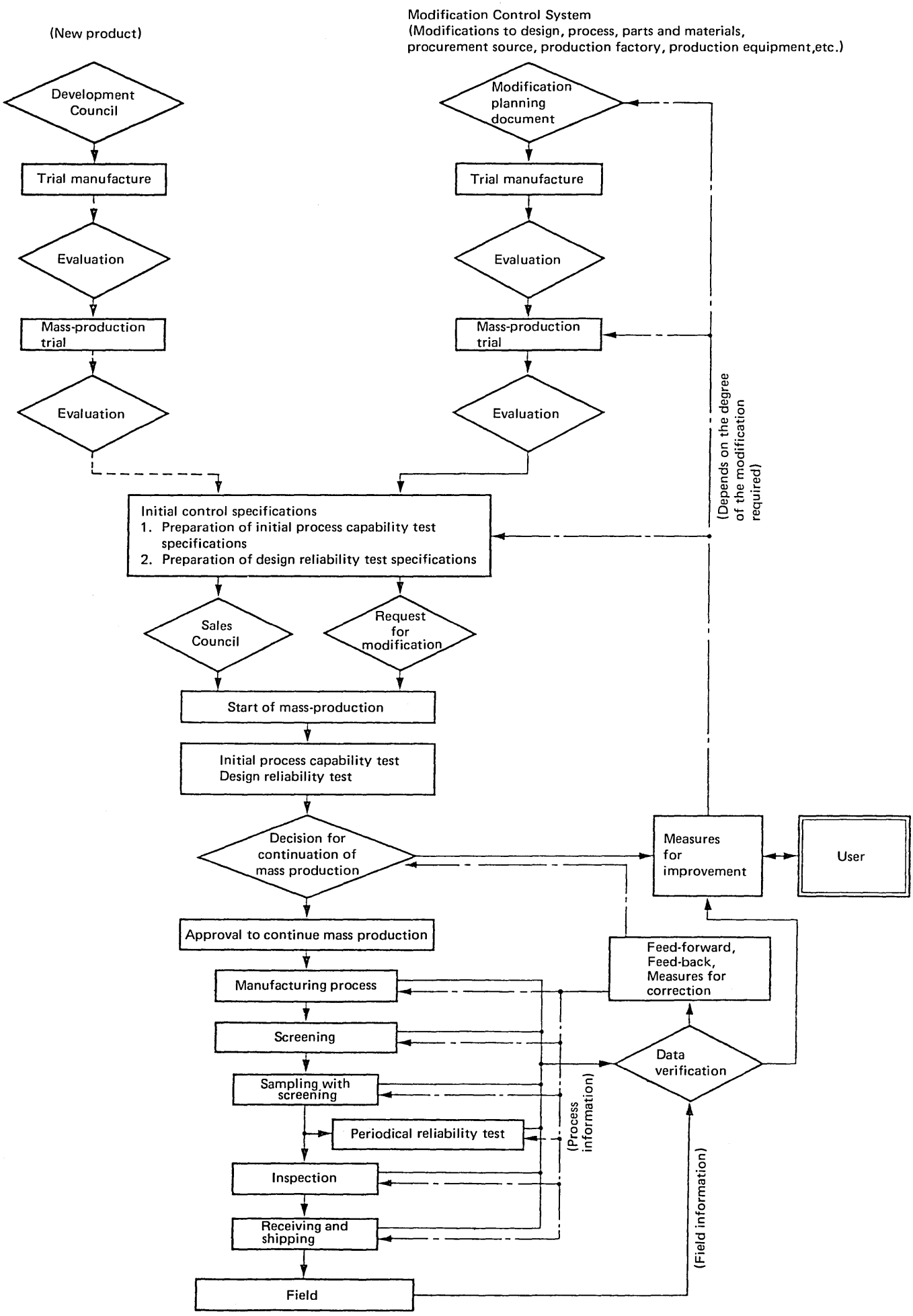
7. Modifications Control System

To allow the use of NEC's semiconductor products to the satisfaction of users, it is natural for NEC to maintain the stable reliability and quality of our products at all times. NEC believes that the imporvement of the reliability and quality of its products to meet the needs of the times is also of importance. To yield the stable reliability and quality, we at NEC are carrying out strict reliability and quality control by feeding forward and back the vital process information which governs the reliability and quality of the products, improving the structural materials and manufacturing methods for semiconductor products while keeping pace with the technological advance and utilizing the field information effectively. However, we are not self-satisfied with only meeting the existing standards we established, and are thus making every effort to improve the reliability and quality of our products to meet the user's requirements as well.

With the basically same concept as that for the development and mass production of new products, we evaluate trial products thoroughly, and conduct the initial management whenever any modifications to the manufacturing or design processes resulting from these improvements are required.

The modification control system will vary depending on the degree of the modification required. The following flowchart shows an example of modification control system.

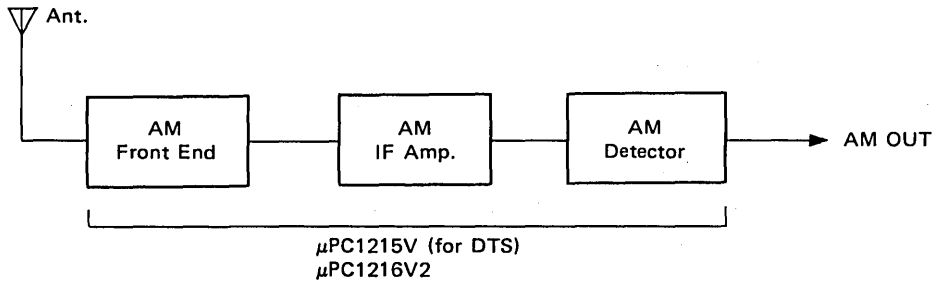
RELIABILITY AND QUALITY CONTROL SYSTEM



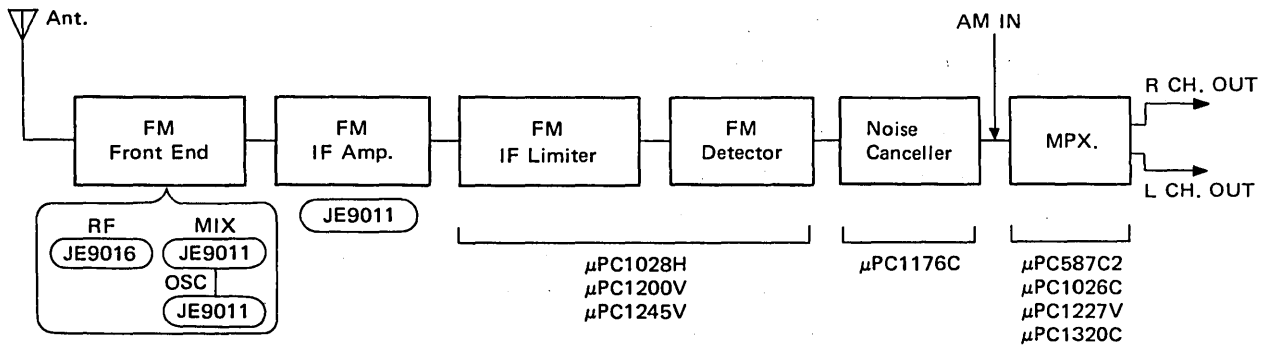
INDEX

BLOCK DIAGRAM

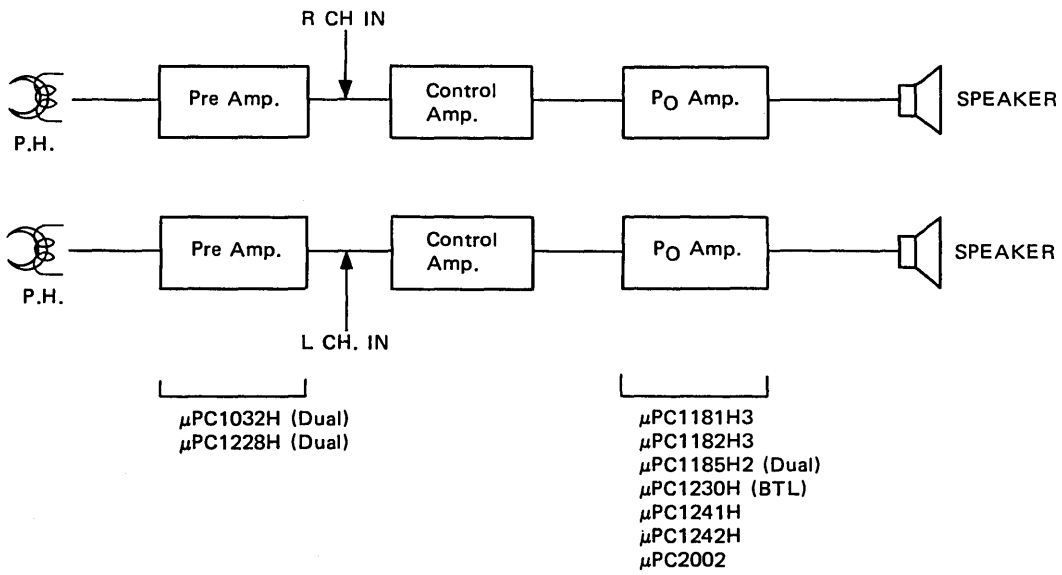
AM Block



FM Block



AF Block



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1215V

ELECTRONIC TUNING AM RADIO RECEIVER SUBSYSTEM
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

DESCRIPTION

The μPC1215V, a monolithic integrated circuit, is a subsystem that provides the mixer, low level oscillator, IF amplifier, detector and On channel detector stages for an electronic tuning AM radio receiver.

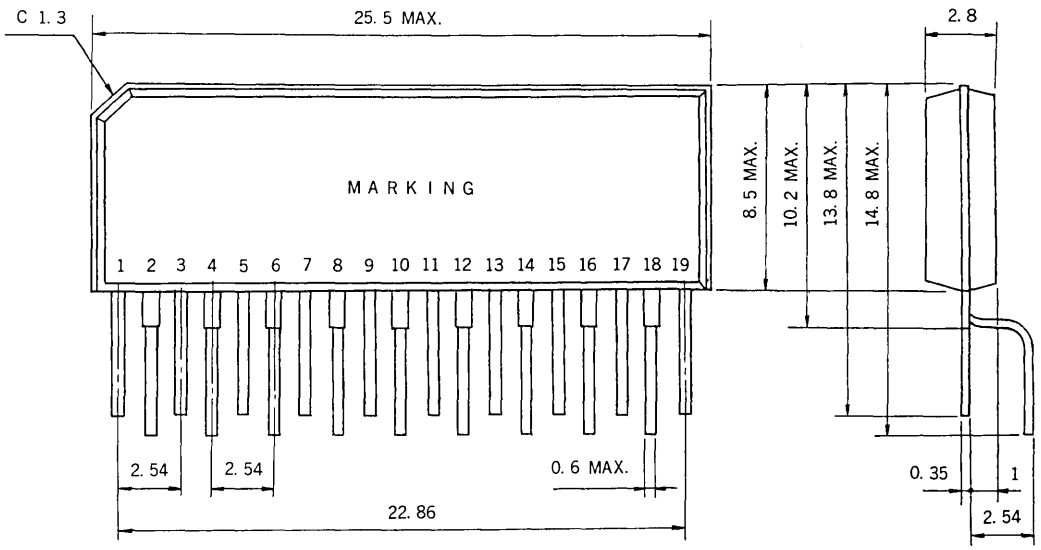
The μPC1215V also provides internal AGC for the first IF amplifier stage, delayed AGC for an optional external RF amplifier, oscillator buffer amplifier to drive a logic section and local/distance sensitivity control.

The μPC1215V is suitable for use in automotive radio receivers, specially where compact mounting is required, such as car stereo sets, because its package is the 19-leads vertical dual in-line plastic package (V-DIP).

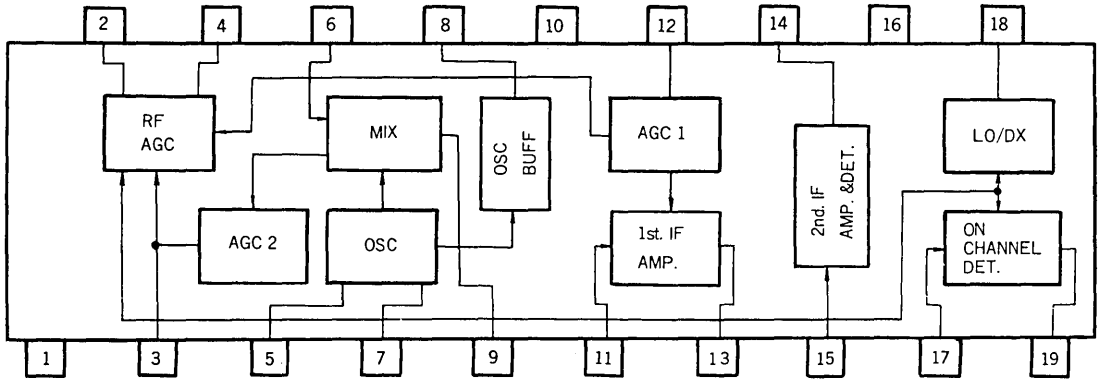
FEATURES

- Varactor-Diode tuning.
- Good sensitivity and wide AGC range.
- Excellent overload characteristics.
- Delayed AGC for RF amplifier.
- Special low level oscillator to reduce tracking error.
- Oscillator buffer output.
- ON channel detector for auto scan stop.
- Local/Distance sensitivity control.
- Occupation of minimum area in P.W.Board.

PACKAGE DIMENSIONS (in millimeters)



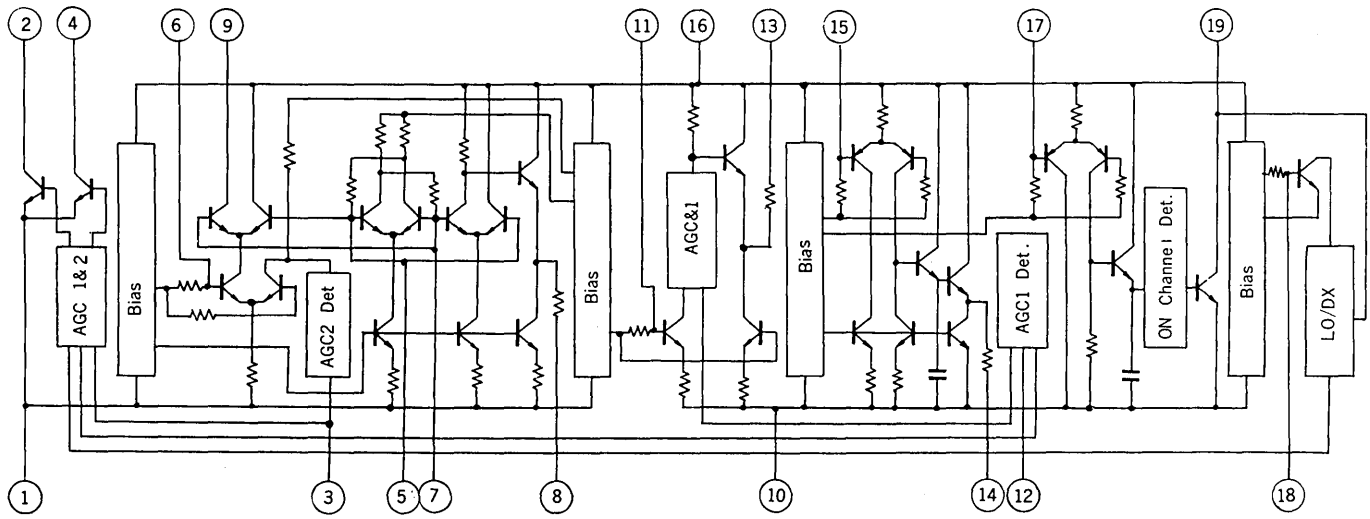
BLOCK DIAGRAM



CONNECTION DIAGRAM

Pin No.	Connection	Pin No.	Connection
1	GND1	2	AGC for Antenna
3	AGC Filter	4	AGC for RF
5	OSC Tank	6	MIX Input
7	OSC Bypass	8	OSC Buffer Output
9	MIX Output	10	GND2
11	1st. IF Amp. Input	12	AGC Input
13	1st. IF Amp. Output	14	Detector Output
15	2nd. IF Amp. Input	16	V_{CC}
17	On Channel Det. Input	18	LO/DX Control Input
19	On Channel Signal Output		

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

DC Supply Voltage	V_{CC}	15	V
Input Voltage	V_i	3.0	Vp-p
Package Dissipation	P_d	430 (Ta = 75 °C)	mW
Operating Temperature	T_{opt}	−30 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

RECOMENDED OPERATING CONDITIONS

DC Supply Voltage Range	V_{CC}	8.0 to 15	V
Operating Ambient Temperature	Ta	−30 to +75	°C

ELECTRICAL CHARACTERISTICS (Ta = 25 °C, V_{CC} = 10 V, f = 1.0 MHz, $f_{mod.}$ = 400 Hz, mod. = 30 %)

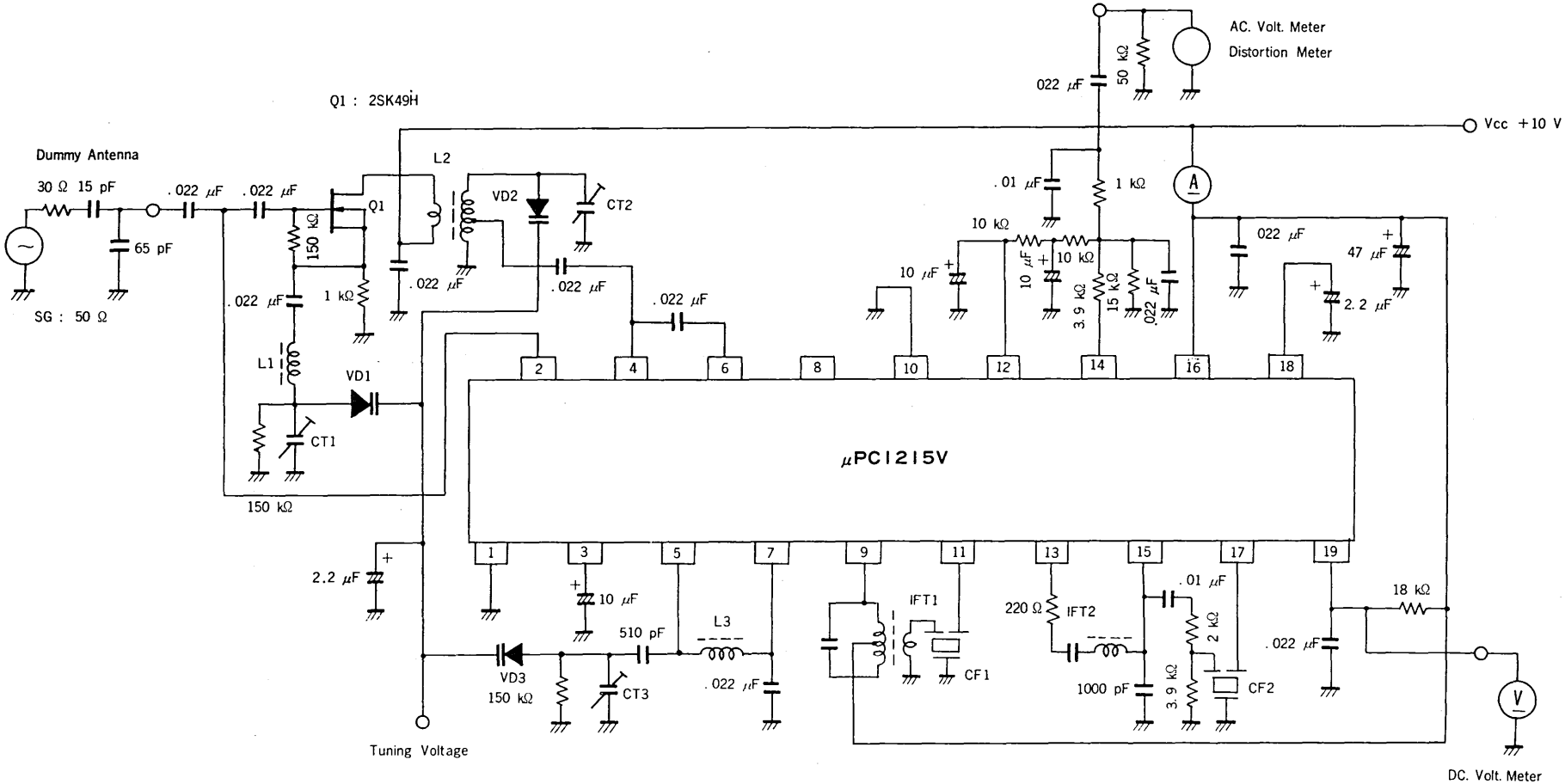
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Circuit Current	I_{CC}	10	14	21	mA	At no signal
Maximum Sensitivity	MS	14	21	28	dBμV	V_o = 30 mVr.m.s.
Signal to Noise Ratio	S/N	8.0	13		dB	V_i = 21 dBμV
Detector Output Volt.	V_o	70	100	130	mVr.m.s.	V_i = 74 dBμV
Harmonic Distortion	T.H.D.		0.5	1.0	%	V_i = 120 dBμV
On Channel Signal	V19-L			0.5	V	V_i = 0 dBμV, R_L = 18 kΩ
	V19-H	8.0			V	V_i = 74 dBμV, R_L = 18 kΩ

TUNER PERFORMANCE CHARACTERISTICS

(Ta = 25 °C, V_{CC} = 10 V, f = 1.0 MHz, $f_{mod.}$ = 400 Hz, mod. = 30 %)

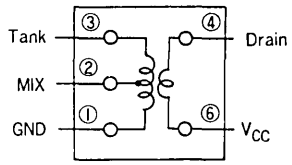
CHARACTERISTIC	TEST CONDITION	VALUE	UNIT
Maximum Sensitivity	V_o = 30 mVr.m.s.	22	dBμV
Usable Sensitivity	S/N = 20 dB	28	dBμV
Detector Output Voltage	V_i = 74 dBμV	100	mVr.m.s.
Total Harmonic Distortion	V_i = 74 dBμV	0.3	%
	V_i = 126 dBμV	0.6	%
	V_i = 74 dBμV, mod. = 80 %	1.2	%
Signal to Noise Ratio	V_i = 74 dBμV	52	dB
IF Rejection Ratio	V_o = 30 mVr.m.s., IF = 450 kHz	56	dB
Image Rejection Ratio	V_o = 30 mVr.m.s., f+2 IF	57	dB
Selectivity	Δf = ±10 kHz	39	dB
Tweet	V_i = 74 dBμV, 2 IF = 900 kHz	40	dB
	3 IF = 1 350 kHz	47	dB
DX Sensitivity	V19 = 8.0 V	26	dBμV
On Channel Bandwidth	V_i = 74 dBμV	5.0	kHz
Oscillation Voltage	At terminal 5	150	mVr.m.s.
	At terminal 8	4.0	Vp-p

TEST CIRCUIT



COIL DATA

L1 & L2 : Ant. & RF Coil



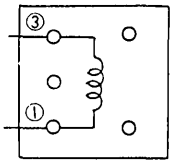
TYPE 7BR-5407N (Toko inc.)

Qu=80 min., L=170 μH

①−②, ②−③, ④−⑥

7T 62T 14T

L3 : OSC Coil



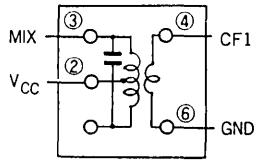
TYPE 7BR-6048Z (Toko inc.)

Qu=60 min., L=95 μH

①−③

48T

IFT1 : IFT



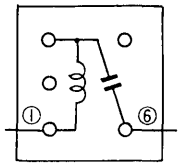
TYPE 7MC-4718N (Toko inc.)

Qu=115±20 %, C=180 pF built in

①−②, ②−③, ④−⑥

69T 77T 14T

IFT2 : IFT

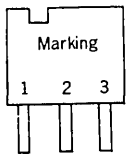


TYPE 7MC-101000CO (Toko inc.)

L=680 μH, C=180 pF built in

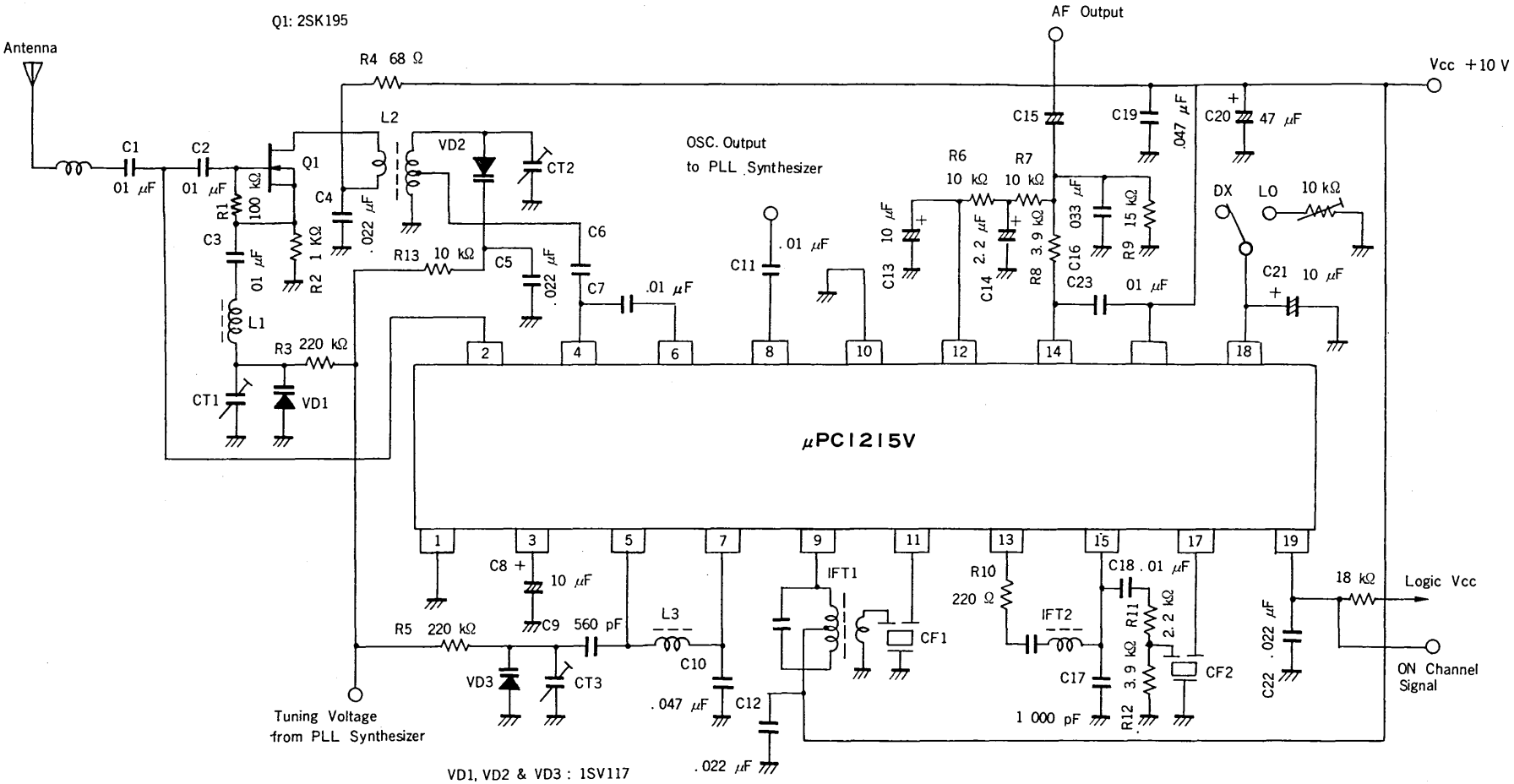
CERAMIC FILTER

	CFM2-450BL	CFM2-450ZL
Center Frequency	450 kHz	450 kHz
6 dB Bandwidth	6 kHz min.	4 kHz min.
Selectivity ±9 kHz	16 dB min.	18 dB min.
Insertion Loss	6 dB max.	6 dB max.
Input Impedance	1.5 kΩ	1.0 kΩ
Output Impedance	2.0 kΩ	1.5 kΩ



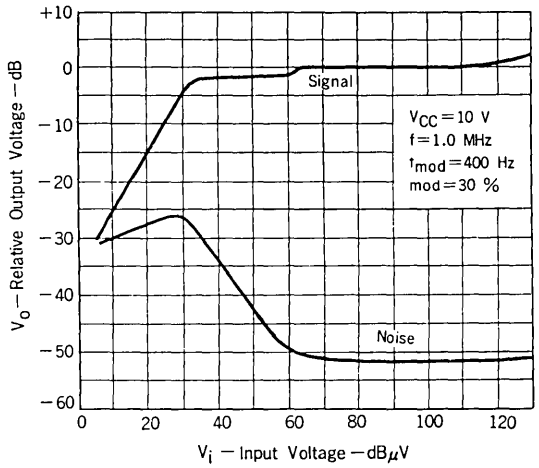
1 : Input
2 : GND
3 : Output

TYPICAL APPLICATION

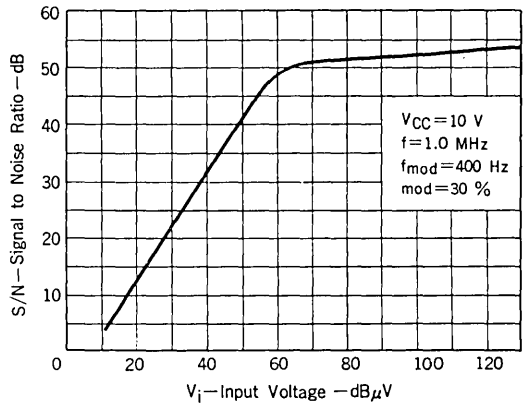


TYPICAL CHARACTERISTICS (Ta = 25 °C)

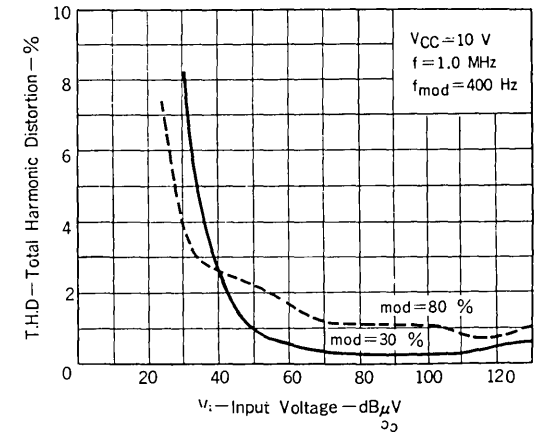
DETECTOR OUTPUT CHARACTERISTICS



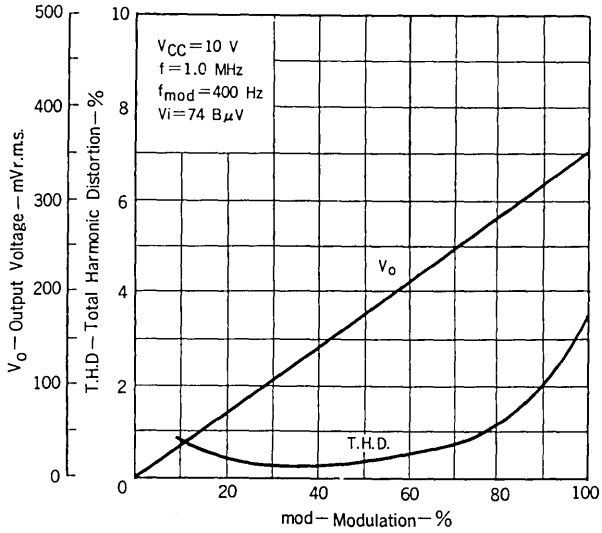
SIGNAL TO NOISE RATIO



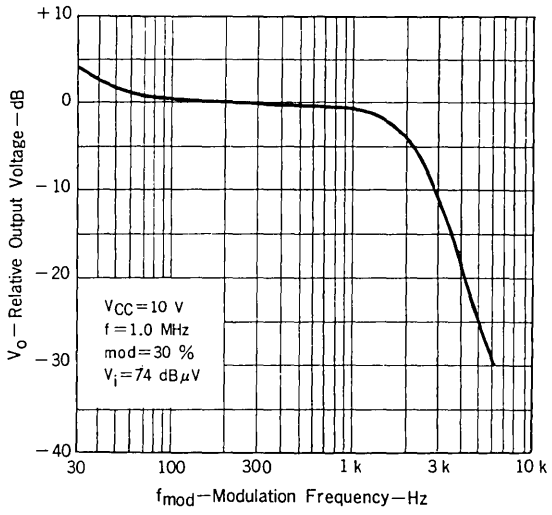
TOTAL HARMONIC DISTORTION vs. INPUT VOLTAGE



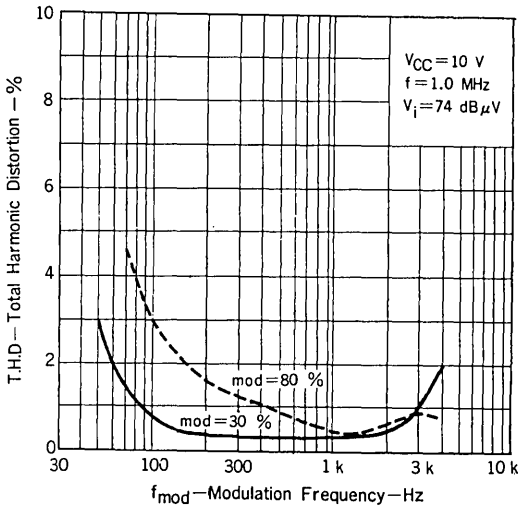
OUTPUT VOLTAGE AND TOTAL HARMONIC DISTORTION vs. MODULATION



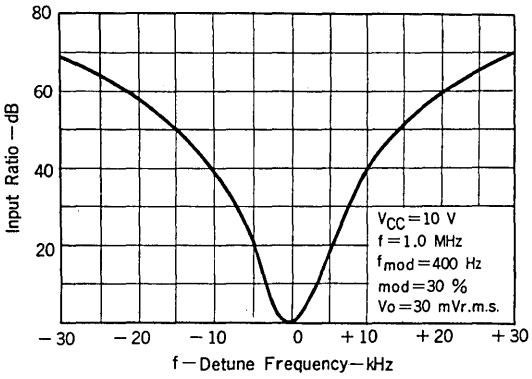
ELECTRICAL FIDELITY



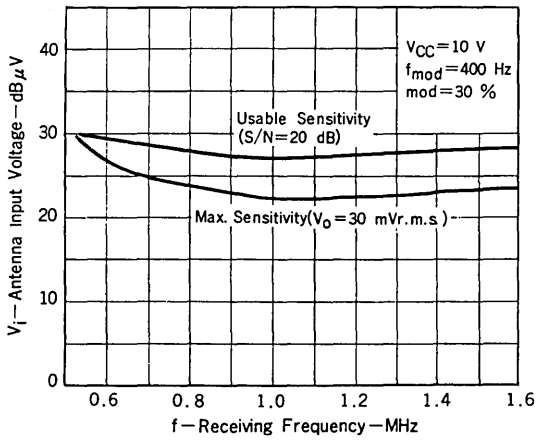
TOTAL HARMONIC DISTORTION vs. MODULATION FREQUENCY



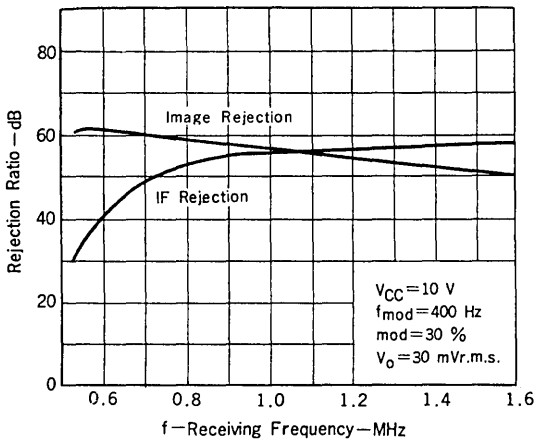
SELECTIVITY



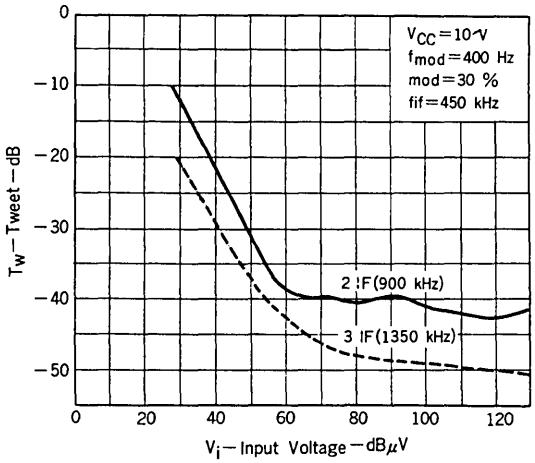
MAX. SENSITIVITY AND USABLE SENSITIVITY



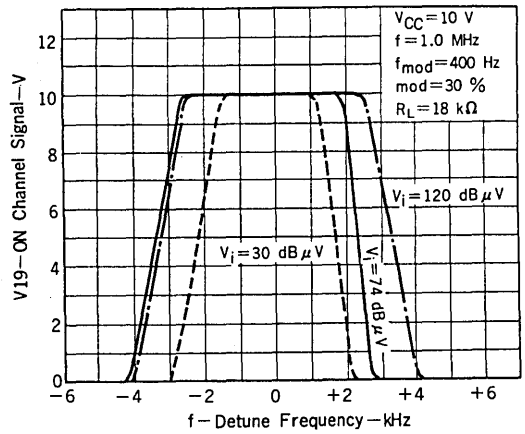
IF REJECTION AND IMAGE REJECTION



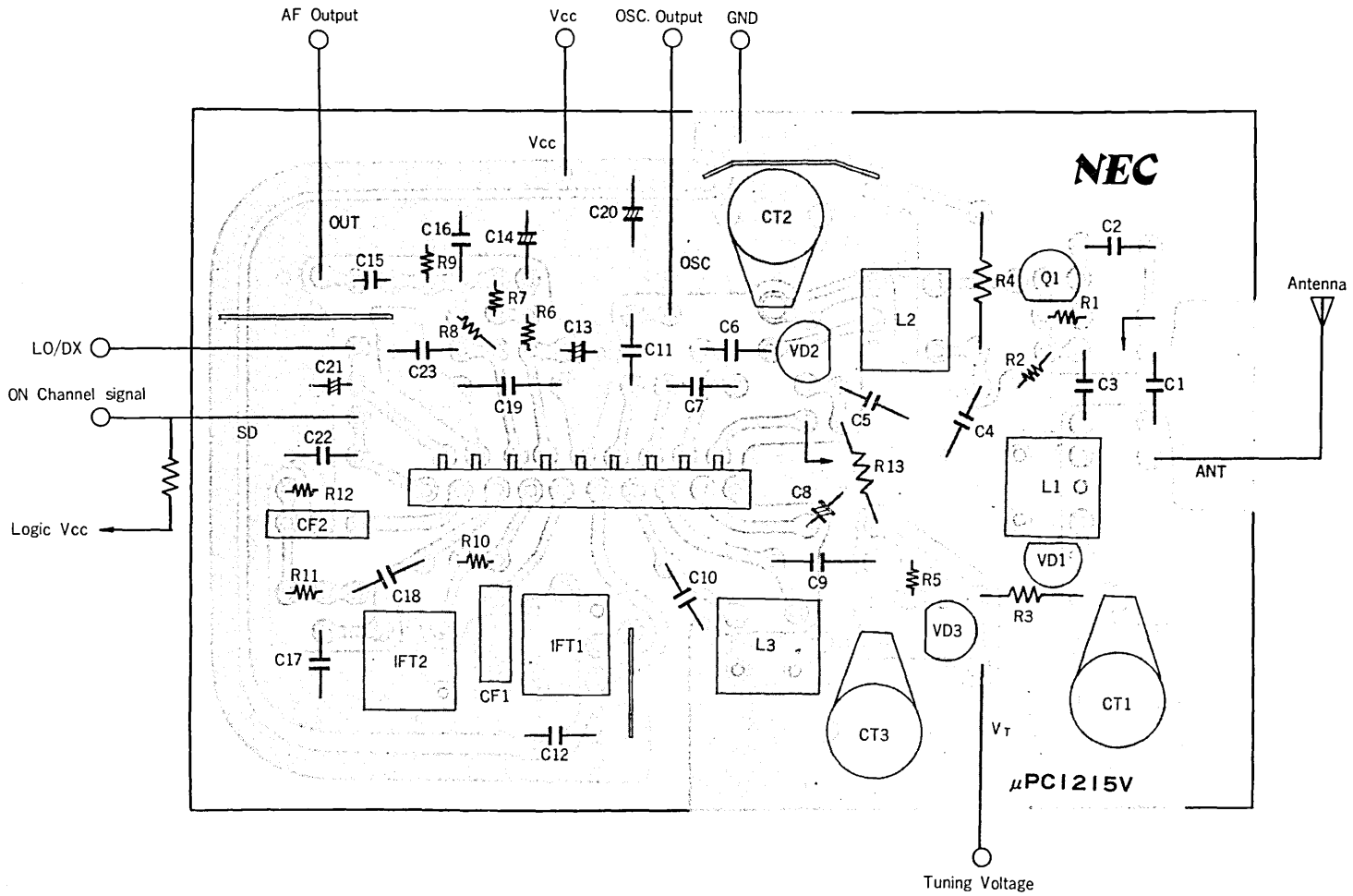
TWEET CHARACTERISTIC



ON CHANNEL BANDWIDTH



COMPONENTS LAYOUT FOR P.W.ASSEMBLY (Copper side)



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1216V2

AM TUNER
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

DESCRIPTION

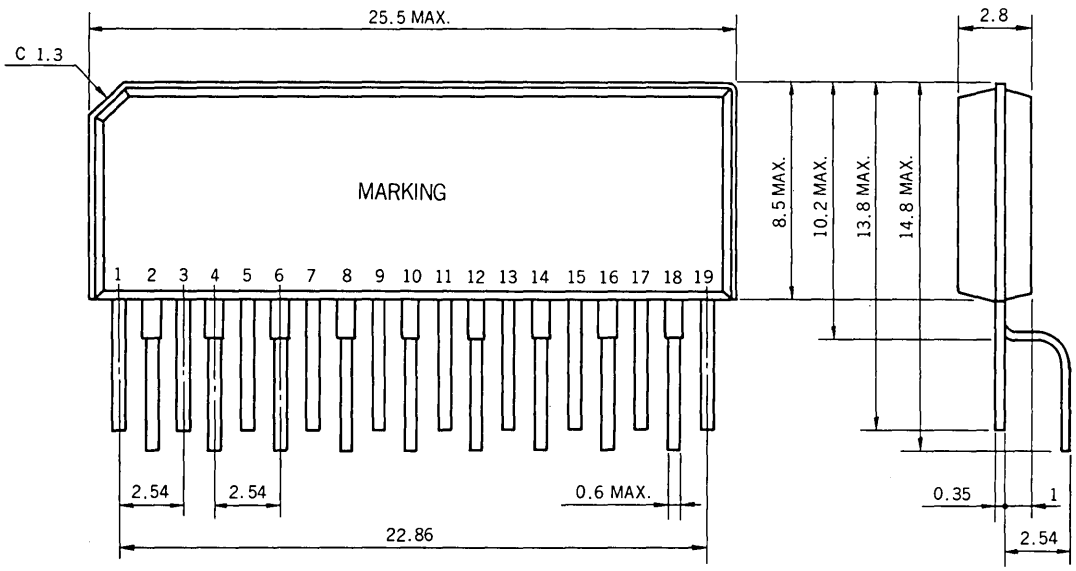
The μPC1216V2, a monolithic integrated circuit, is an AM tuner. It is suitable for use in automotive radio receivers, specially where compact mounting is required, such as car stereo sets, because its package is the 19-lead vertical dual in-line plastic package (V-DIP).

Internally, RF amplifier, Mixer, IF amplifier, Detector and two types of AGC circuit are included.

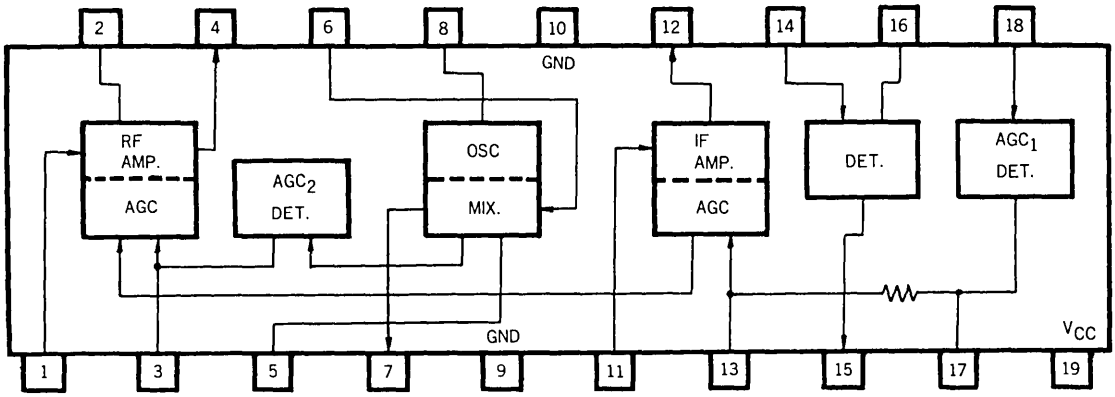
FEATURES

- Reduction of the adjustment time and the mounting area for IF transformer.
- Minimum difference of maximum sensitivity at the various receiving frequency.
- Good S/N and good tweet characteristic.
- High strength against the electrostatic damages for the antenna terminal.
- Low transient noise when power switch is turned on.
- Wide AGC range is provided by the two AGC circuits (delay type) employed in the IF and RF stages, in addition to the capability of withstanding large input and the yield of high S/N.
- Easy to handle because of its V-DIP construction.
- Free of mismounting in P.W. Board due to its lead formation.

PACKAGE DIMENSIONS in millimeters



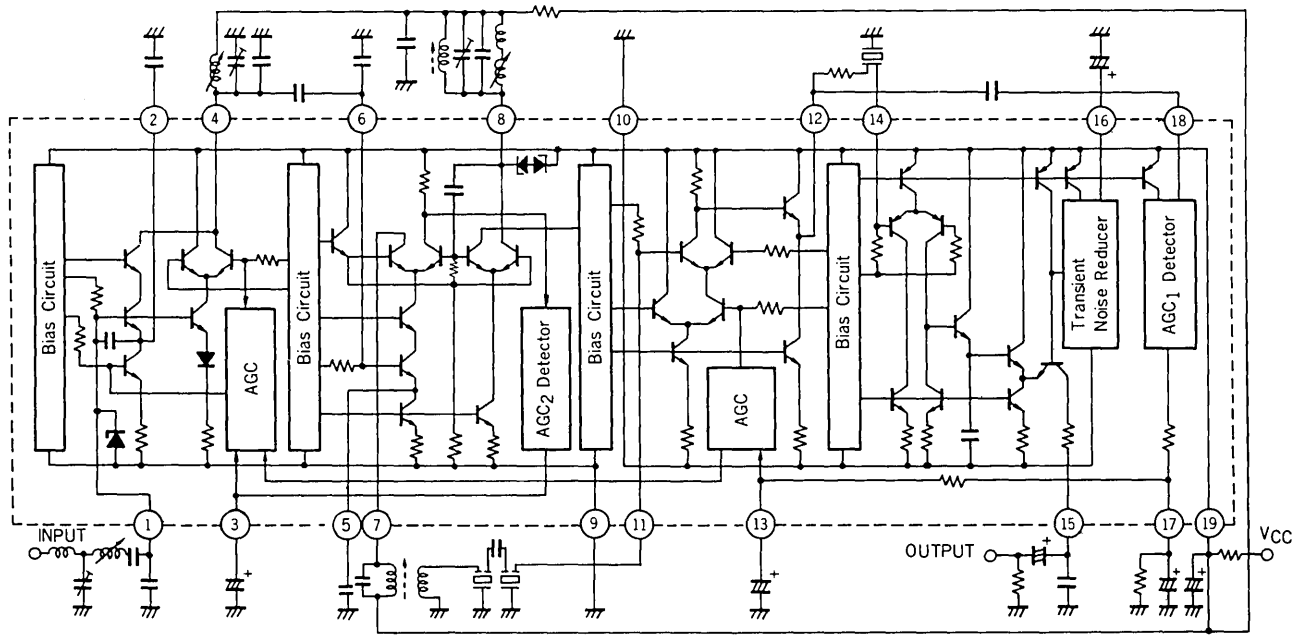
BLOCK DIAGRAM (Top View)



CONNECTION DIAGRAM

Pin No.	Electrical Connections	Pin No.	Electrical Connections
1	RF INPUT	2	BYPASS
3	BYPASS	4	RF OUTPUT
5	BYPASS	6	MIX. INPUT
7	MIX. OUTPUT	8	LOCAL OSC
9	GND	10	GND
11	IF INPUT	12	IF INPUT
13	BYPASS	14	DETECTOR INPUT
15	DETECTOR OUTPUT	16	BYPASS
17	BYPASS	18	AGC DET. INPUT
19	V_{CC}		

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Supply Voltage	V_{CC}	18	V
Input Voltage	V_i	7	Vp-p
Package Dissipation (Ta = 75 °C)	P_D	430	mW
Operating Temperature	T_{opt}	−30 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

RECOMMENDED OPERATING CONDITIONS (Ta = 25 °C)

Operating Supply Voltage	V_{CC}	13	V
Supply Voltage Range		9 to 16	V
Operating Ambient Temperature	Ta	−20 to +65	°C

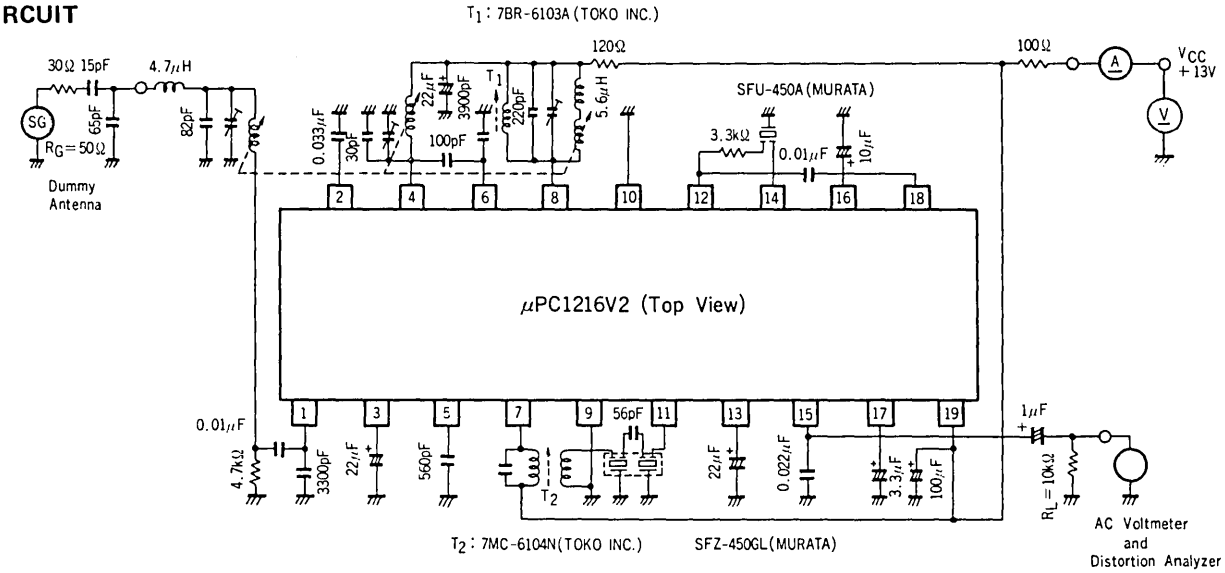
ELECTRICAL CHARACTERISTICS (Ta = 25 °C, V_{CC} = 13 V, f = 1 MHz, f_{mod} = 400 Hz, MOD = 30 %, R_L = 10 kΩ)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	I_{CC}	10.5	15	19.5	mA	At no signal
Maximum Sensitivity	MS		13	20	dBμV	Input level (v_i) at which detector output v_o gets 40mVr.m.s.
Signal-to-Noise Ratio	S/N	15	20		dB	v_i = 23 dBμV
Detector Output	v_o		110		mVr.m.s.	v_i = 74 dBμV
Overload Distortion	T.H.D.		0.4	3	%	v_i = 126 dBμV

TUNER PERFORMANCE CHARACTERISTICS
(Ta = 25 °C, V_{CC} = 13 V, f = 1 MHz, f_{mod} = 400 Hz, MOD = 30 %, R_L = 10 kΩ)

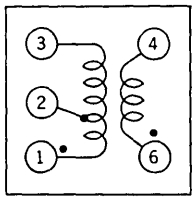
CHARACTERISTIC	TEST CONDITIONS	VALUE	UNIT
Max. Sensitivity	Input Voltage at which Det. Output Voltage is 40 mVr.m.s.	13	dBμV
Usable Sensitivity	Input Voltage at which S/N is 20 dB	23	dBμV
Detector Output	v_i = 74 dBμV	110	mVr.m.s.
Detector Distortion	v_i = 74 dBμV	0.4	%
Signal-to-Noise Ratio	v_i = 74 dBμV	54	dB
Overload Distortion	v_i = 126 dBμV	0.4	%
IF Rejection	f = 1 MHz, v_o = 40 mVr.m.s., IF = 450 kHz	72	dB
Image Rejection	f = 1 MHz, v_o = 40 mVr.m.s., f+2 IF	74	dB
Selectivity	f = 1 MHz, Δf = ±10 kHz	45	dB
Tweet	v_i = 74 dBμV, 2 IF = 900 kHz 3 IF = 1 350 kHz	45 50	dB dB

TEST CIRCUIT



COIL DATA

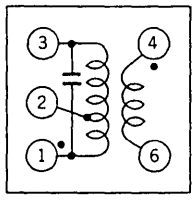
T1 : Oscillator Coil **7BR-6103A (TOKO INC.)**



①-② ②-③ ④-⑥
8T 70T 20T

L=220 μH±6 %
Q_U=80 (796 kHz)

T2 : IF Transformer **7MC-6104N (TOKO INC.)**



①-② ②-③ ④-⑥
73T 73T 10T

f_T=455 kHz±3 %
Q_U=115±20 %
C_T=180 pF

Tuner : NIHON TUNER CO. made 5M-S

Minimum Frequency Cover Range 525 ~ 1 615 kHz
Tuning Capacitor

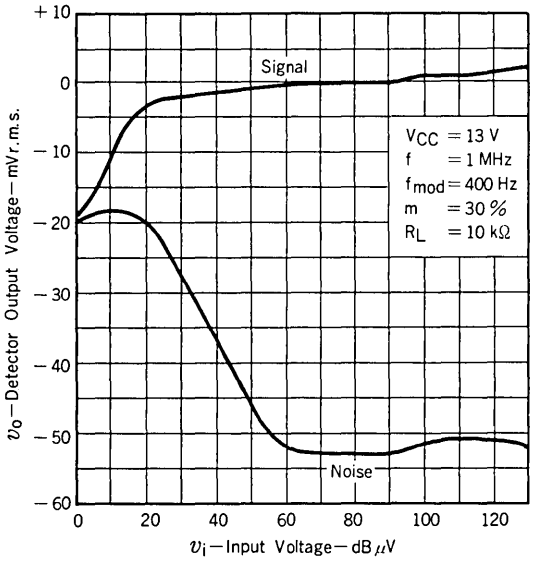
ANT Coil	150 pF
RF Coil	150 pF
OSC Coil	450 pF

CERAMIC FILTER (MURATA Co.)

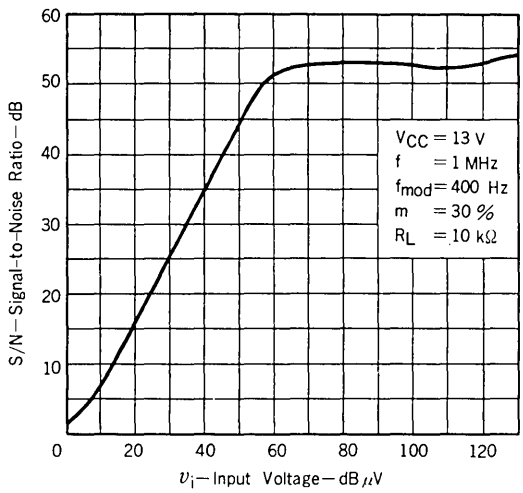
CHARACTERISTIC		SFU450A	SFZ450GL
Center Frequency		450 kHz	450 kHz
3 dB Band Width		10 kHz	6.5 kHz
Selectivity	−9 kHz	7.5 dB	20 dB
	+9 kHz	5.5 dB	20 dB
Insertion Loss		3 dB	3 dB
		Marking ③②① ①: Input ②: GND ③: Output	Marking ①②③ ⑥⑤④ ①: Input ②⑤: GND ③④: Capacitance ⑥: Output

TYPICAL TUNER PERFORMANCE CHARACTERISTICS

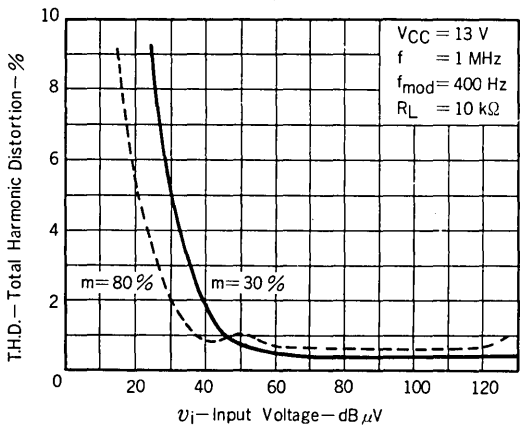
DETECTOR OUTPUT CHARACTERISTIC



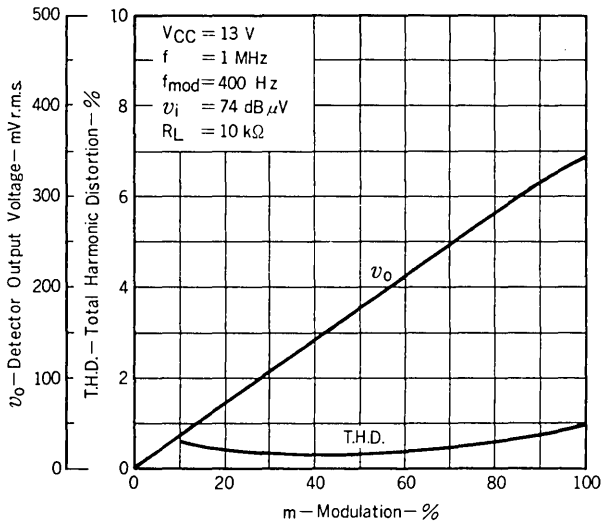
SIGNAL-TO-NOISE RATIO CHARACTERISTIC



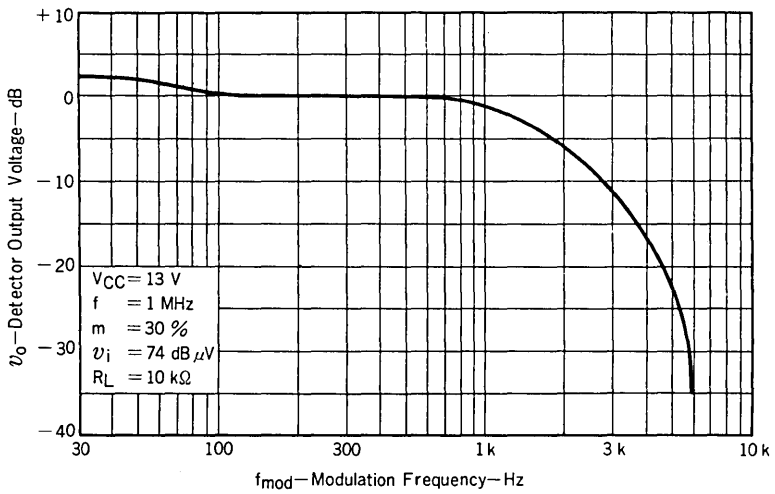
TOTAL HARMONIC DISTORTION vs. INPUT VOLTAGE



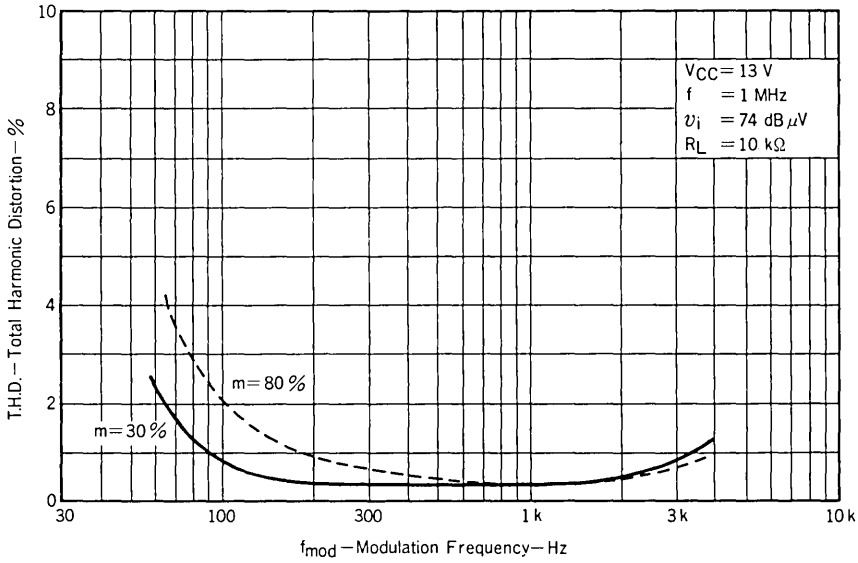
DETECTOR OUTPUT AND TOTAL HARMONIC DISTORTION vs. MODULATION



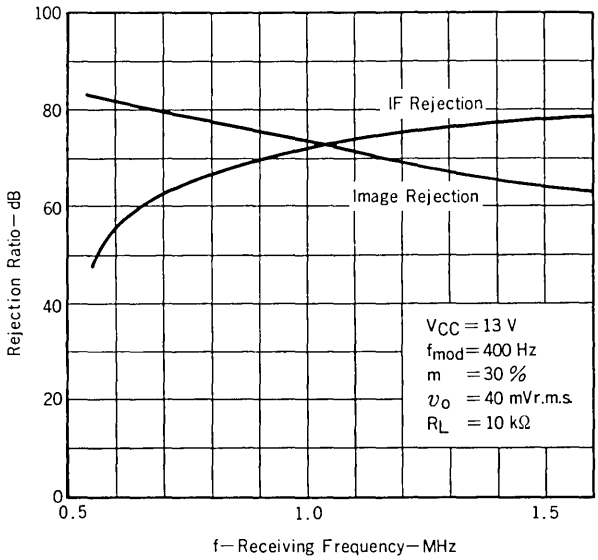
ELECTRICAL FIDELITY



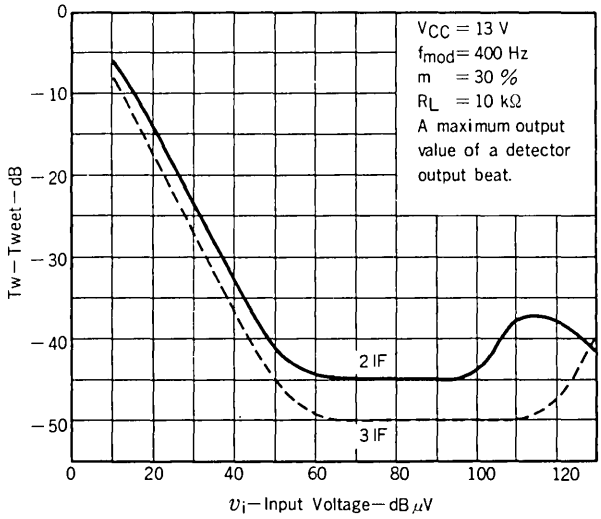
TOTAL HARMONIC DISTORTION
vs. MODULATION FREQUENCY



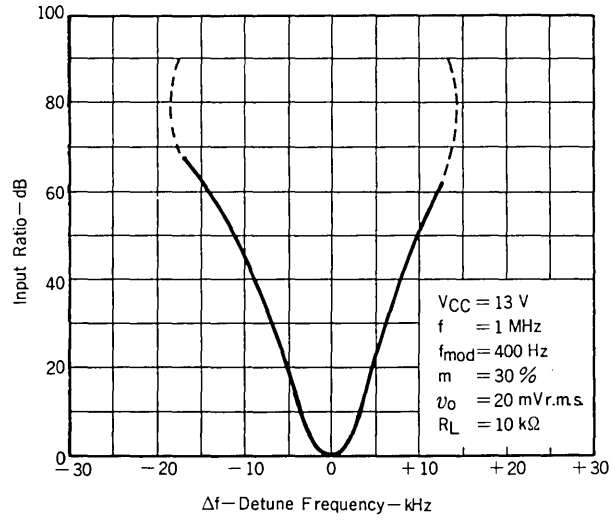
IF REJECTION AND IMAGE REJECTION



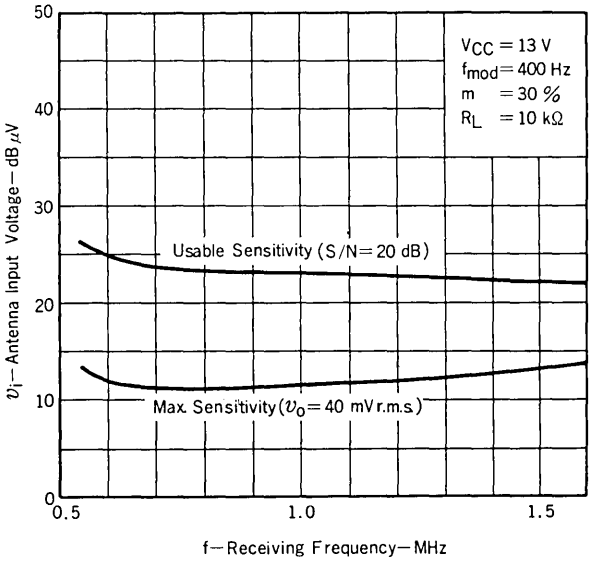
TWEET CHARACTERISTIC



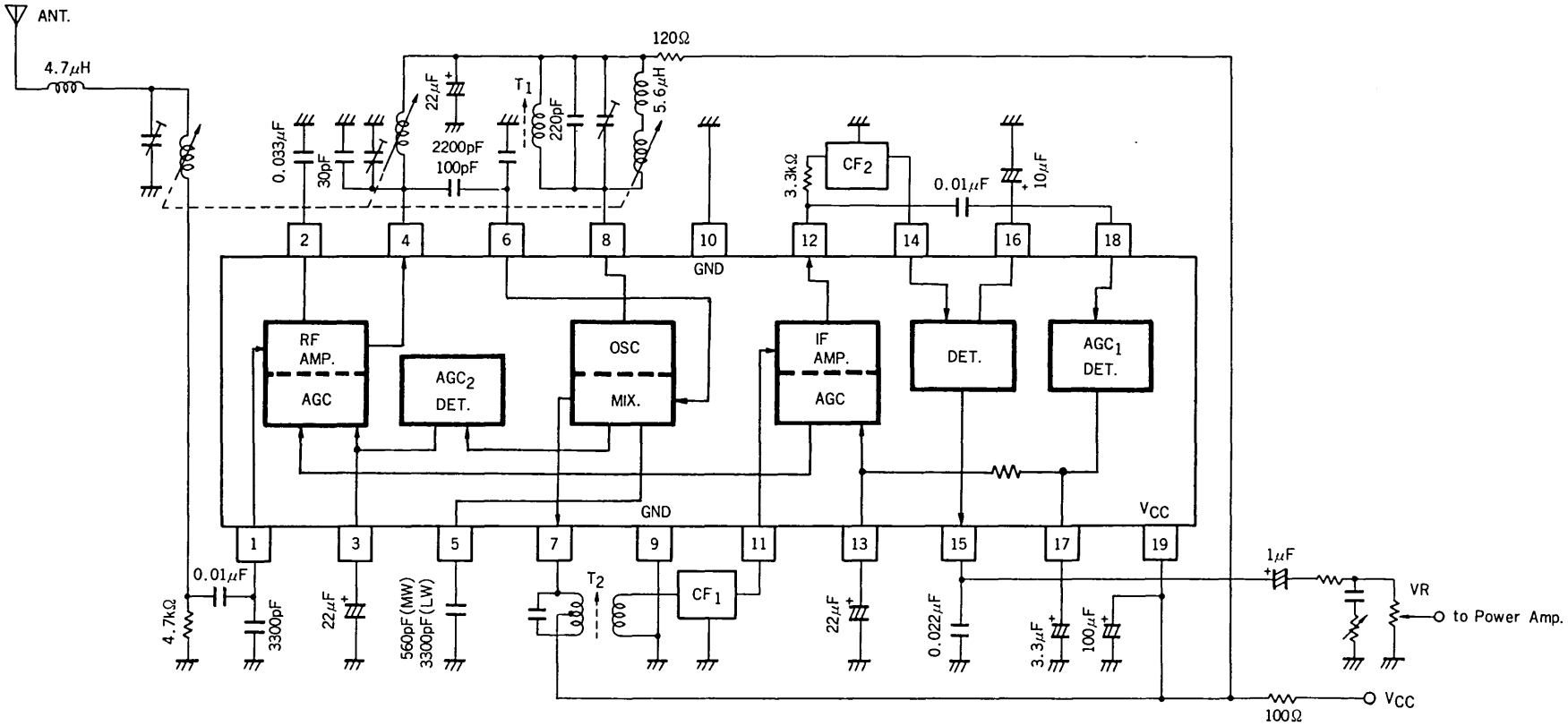
ONE-SIGNAL SELECTIVITY
CHARACTERISTIC



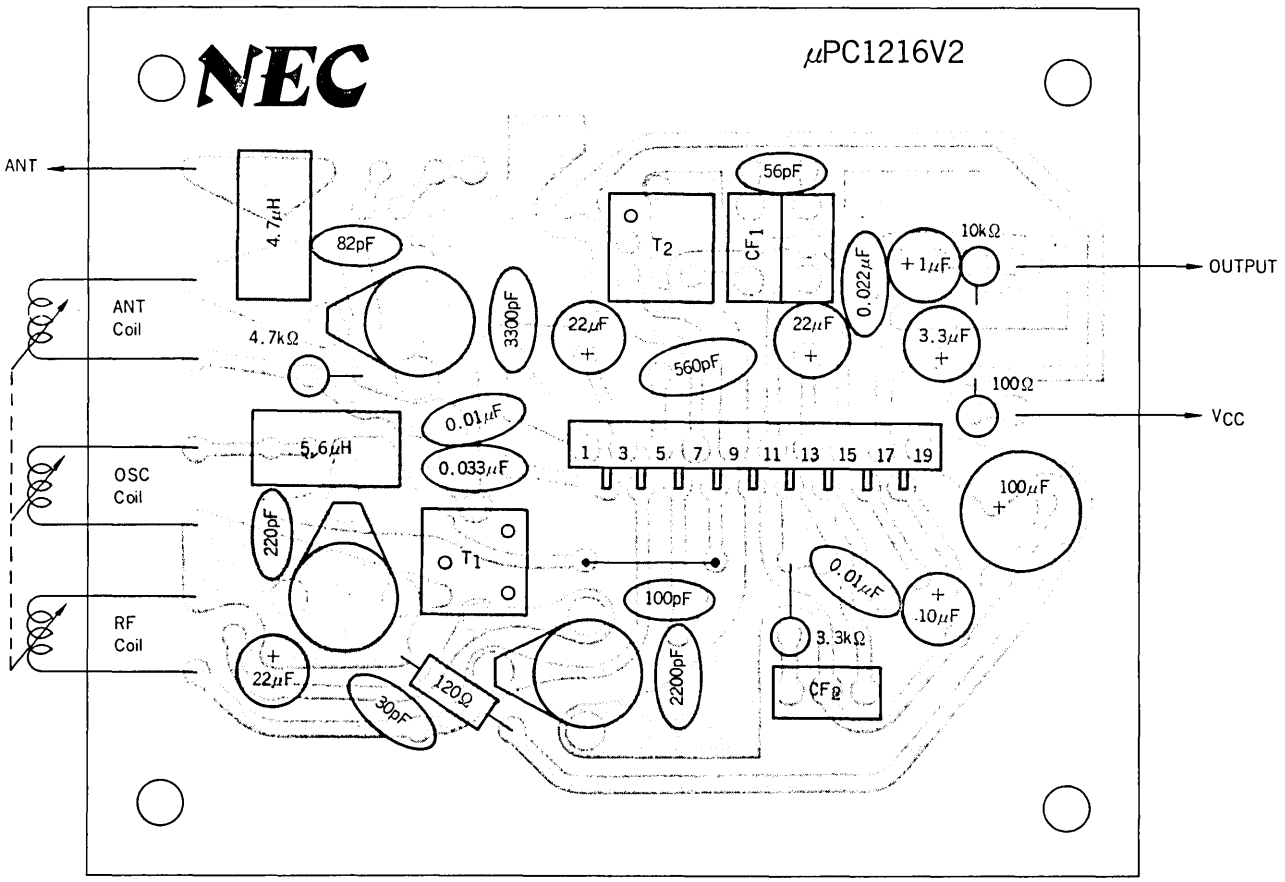
MAX. SENSITIVITY AND USABLE SENSITIVITY



TYPICAL APPLICATION

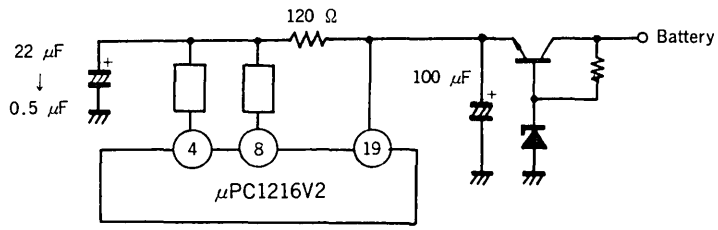


COMPONENTS LAYOUT FOR P.C. ASSEMBLY (Copper side)



CAUTION

1. Don't earth the pin-4, pin-8 or power line connected with these pins by mistake, or μPC1216V2 will be go wrong.
2. When the resistance (100 Ω) is not used between pin-19 and battery, the capacitance (22 μF) of RF stage power line should be change for less than 0.5 μF.



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1028H

FM IF AMPLIFIER WITH DIFFERENTIAL PEAK DETECTOR SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

DESCRIPTION

The μPC1028H is a silicon monolithic integrated circuit intended for an FM IF amplifier with a differential peak detector.

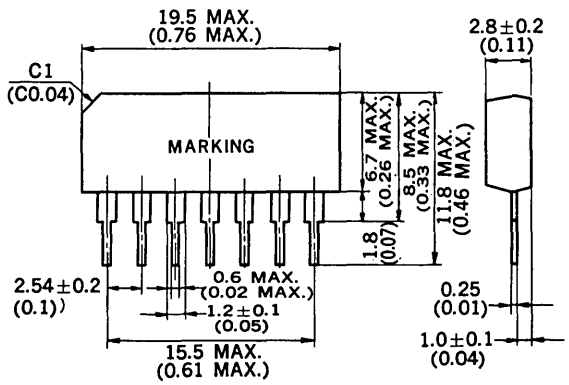
The device contains a three-stage direct coupled differential amplifier, a low pass filter, and a differential peak detector.

The differential peak detector has such feature as simplifying external circuits and components compared with a ratio detector.

The μPC1028H is packaged in a plastic single in-line package (SIP) for easy mounting on a printed circuit board.

PACKAGE DIMENSIONS

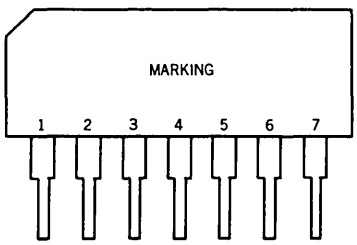
in millimeters (inches)



FEATURES

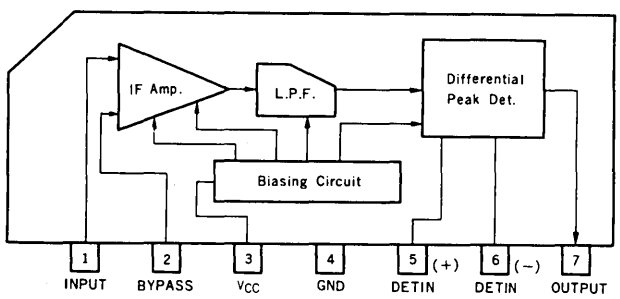
- Few external components required.
- Only one coil necessary in detector circuit, all tuning performed with the coil.
- Low distortion: T.H.D. = 0.3 % TYP. at 100 % moduration.
- SIP assures easy mounting on a printed circuit board.

CONNECTION DIAGRAM

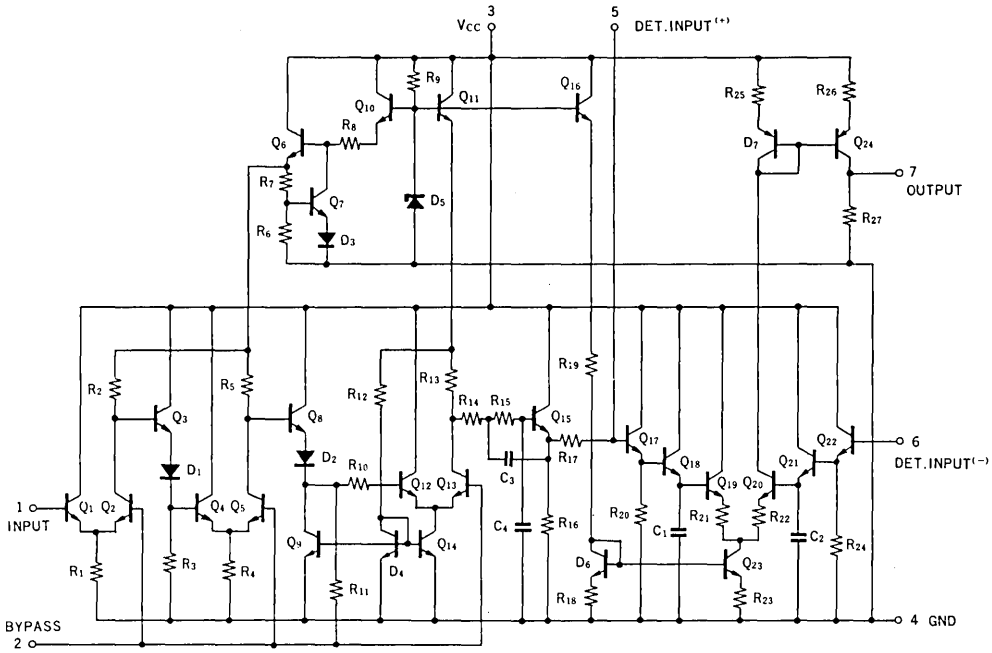


Pin No.	Electrical Connection
1	INPUT
2	BYPASS
3	V_{CC}
4	GROUND
5	DET. IN(+)
6	DET. IN(-)
7	OUTPUT

BLOCK DIAGRAM



EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Supply Voltage	V_{CC}	15	V
Package Dissipation (Ta = 75 °C)	P_D	270	mW
Operating Temperature	T_{opt}	-20 to +75	°C
Storage Temperature	T_{stg}	-40 to +125	°C

RECOMMENDED OPERATING CONDITIONS (Ta = 25 °C)

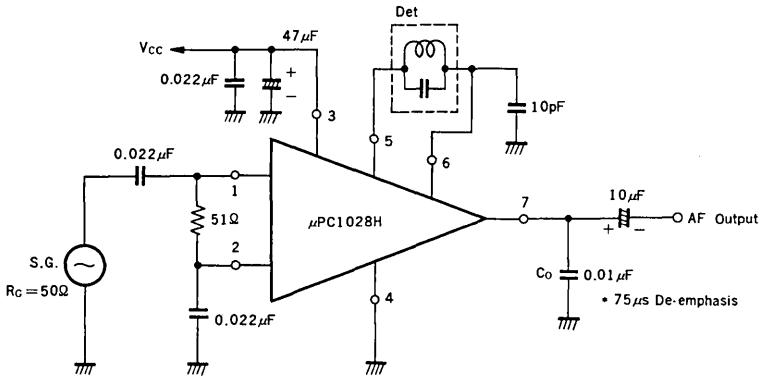
Operating Supply Voltage	10	V
Supply Voltage Range	8 to 15	V

ELECTRICAL CHARACTERISTICS

(Ta = 25 °C, V_{CC} = 10 V, f_o = 10.7 MHz, f_{MLO} = 400 Hz, Δf = ±22.5 kHz, Dev., Peak separation = 1.2 MHz, R_G = 50 Ω)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	I_{CC}	8	12	16	mA	v_{in} = 0
Voltage Gain (IF Amp. stage)	A_v		67		dB	v_{in} = 40 dBμ, carrier signal only
Limitting Sensitivity	v_{in} (lim.)		48		dBμ	Input voltage, −3 dB Limitting
AM Rejection	A.M.R.		40		dB	v_{in} = 80 dBμ, AM = 30 %
Detector Output Voltage	V_{o} AF		165		mV	v_{in} = 80 dBμ
Total Harmonic Distortion	T.H.D. 1		0.3		%	v_{in} = 80 dBμ, Δf = ±75 kHz Dev.
Total Harmonic Distortion	T.H.D. 2		0.1		%	v_{in} = 80 dBμ, Δf = ±22.5 kHz Dev.
S N Ratio	S/N		65		dB	v_{in} = 80 dBμ
Output Impedance	Ro		7.5		kΩ	f = 400 Hz

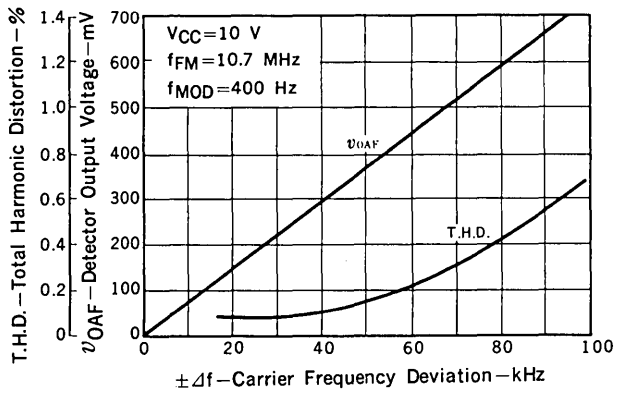
TEST CIRCUIT



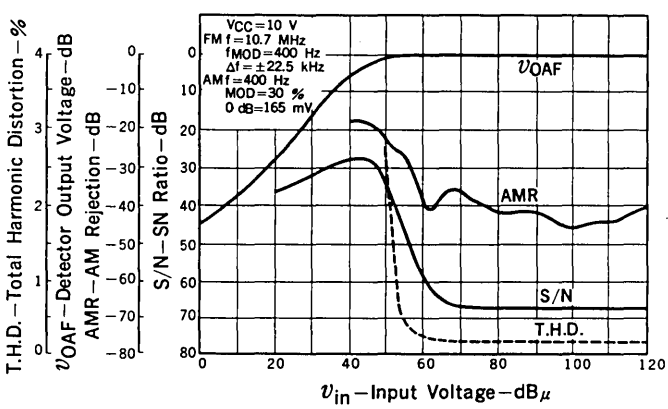
Det. Coil:
L = 9 μH, C = 22 pF, Q_u = 50
TKACA-17473
TOKO INC., of Equivalent.

TYPICAL CHARACTERISTICS (Ta = 25 °C)

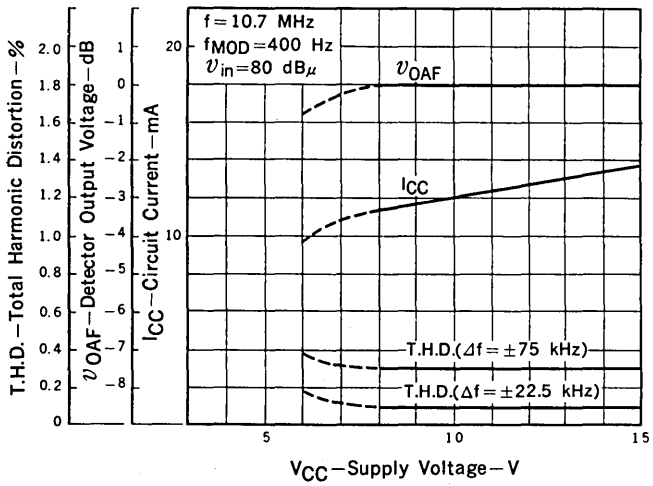
DETECTOR OUTPUT VOLTAGE, TOTAL HARMONIC DISTORTION vs. CARRIER FREQUENCY DEVIATION



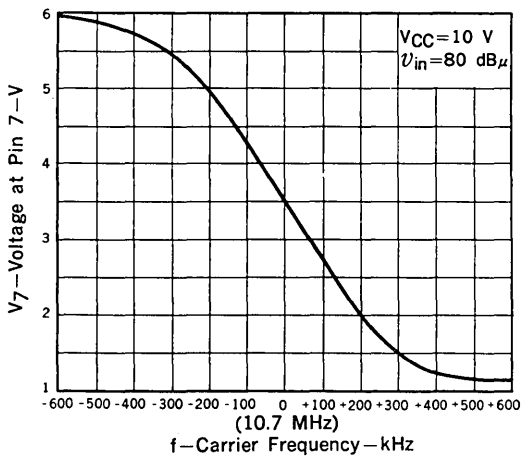
DETECTOR OUTPUT VOLTAGE, AM REJECTION, TOTAL HARMONIC DISTORTION, SN RATIO vs. INPUT VOLTAGE



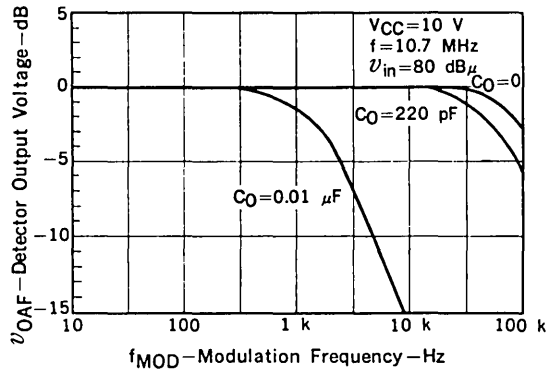
TOTAL HARMONIC DISTORTION, DETECTOR OUTPUT VOLTAGE, CIRCUIT CURRENT vs. SUPPLY VOLTAGE



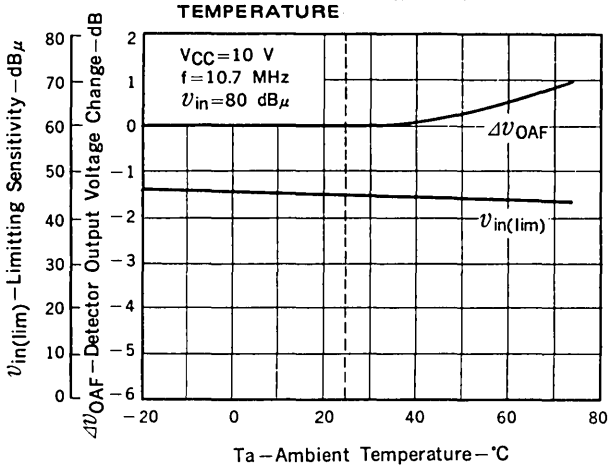
S CURVE



DETECTOR OUTPUT VOLTAGE vs. MODULATION FREQUENCY



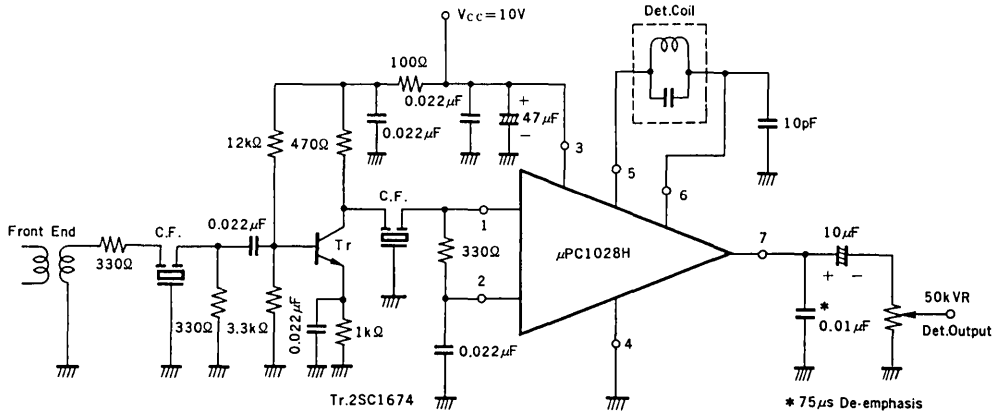
LIMITTING SENSITIVITY, DETECTOR OUTPUT VOLTAGE vs. AMBIENT TEMPERATURE



DETECTOR COIL TUNING PROCEDURE

1. In the test circuit, the signal generator SG is connected to the input terminal pin 1, and the AF voltmeter and the total harmonic distortion meter are connected to the output terminal pin 7.
2. The SG is set at f = 10.7 MHz, f_{MOD} = 400 Hz, Δf = ±22.5 kHz and the input level to the device under test should be 200 μV.
3. After the procedure of 1 and 2, the detector coil is adjusted so that the output level as indicated by the AF voltmeter is maintained the maximum value.
4. Then the detector coil is finely adjusted so that the total harmonic distortion is obtained the minimum value.
5. After the setting of 1 mV input level, the procedure of 3 and 4 are repeated.
   (By the tuning at 200 μV and 1 mV input level, the device provides the most stable characteristic from weak to strong input signal level.)

TYPICAL APPLICATION



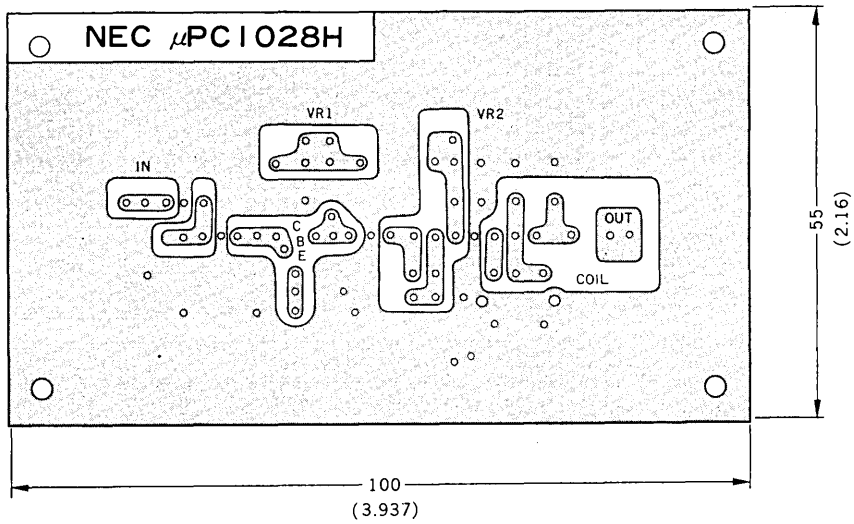
CF: Ceramic Filter
CFSA-107
TOKO INC. made
SFE 10.7MA
MURATA CO. made
or equivalent.

Det. Coil
f_O=10.7 MHz, Q_O=50
C=22 pF (Built in)
TKACA-17473Z
TOKO INC. made
or equivalent.

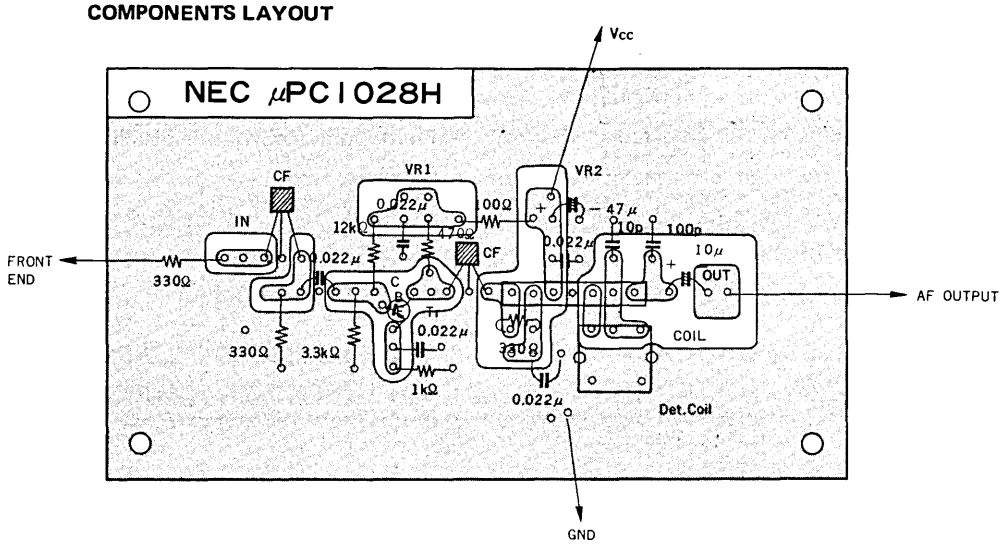
PRINTED CIRCUIT BOARD PATTERN

in millimeters (inches)

FOIL SIDE



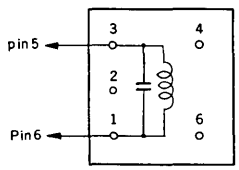
COMPONENTS LAYOUT



CF: Ceramic Filter
SFE10.7 MA (Red)
MURATA CO. made
or equivalent

Tr: 2SC1674
2SC1675

DET COIL DATA



TYPE TKACA-17473Z
TOKO INC., made
f_O=10.7 MHz
C=22 pF
Q_U=50

BIPOLAR ANALOG INTEGRATED CIRCUIT
μPC1200V

SUPER LOW NOISE FM-IF AMPLIFIER WITH QUADRATURE DETECTOR SILICON MONOLITHIC BIPOLAR INTEGRATED CIRCUIT

DESCRIPTION

The μPC1200V, a monolithic integrated circuit, is a FM-IF amplifier with a quadrature detector. FM interstation noise and lateral recovered audio signal can be extremely reduced by the new developed circuit.

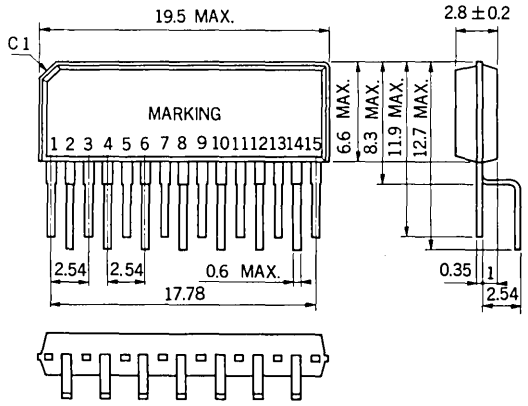
The IC, μPC1200V, enables the best use of an FM noise canceller section, because it does not affect the S/N at low input level.

Outline is a new developed 15-lead Vertical Dual In-Line Plastic Package (V-DIP), so that it is suitable for use in automotive radio receivers, where small mounting space is required.

FEATURES

- Low undesirable noise level : - 60 dB
- Very low lateral uncomfortable sound either upper or lower from the tuning point.
- Capability for effective use of FM noise canceller.
- Occupation of minimum area in P.C. Board.
- Easy to handle because of its V-DIP construction.
- Free of mismounting in P.C. Board due to its lead formation.
- Wide range of power supplies : 7 to 12 V

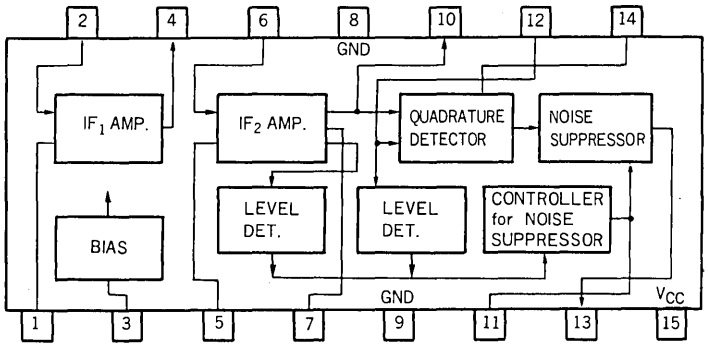
PACKAGE DIMENSION (in millimeters)



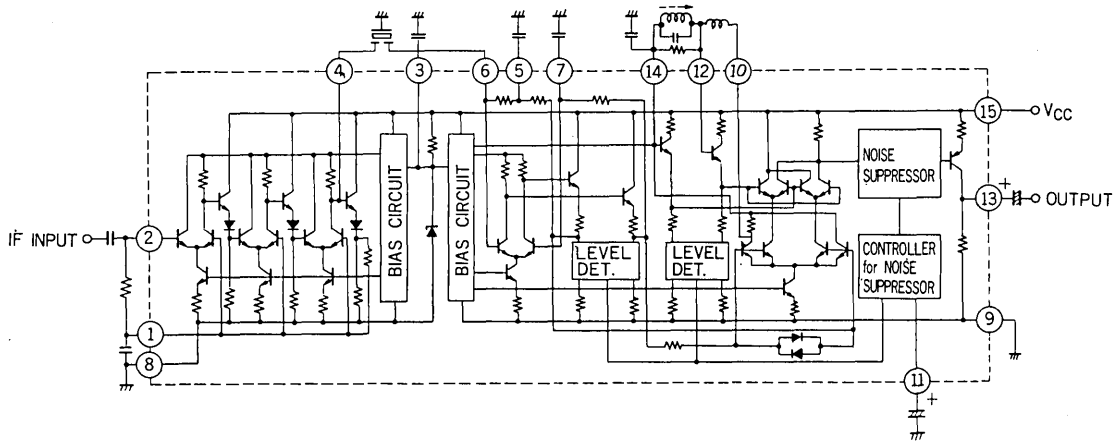
CONNECTION DIAGRAM

Pin No.	Electrical Connection	Pin No.	Electrical Connection
1	BYPASS	2	IF_1 INPUT
3	BYPASS	4	IF_1 OUTPUT
5	BYPASS	6	IF_2 INPUT
7	BYPASS	8	GND
9	GND	10	IF_2 OUTPUT
11	N.S. CONTROL	12	DETECTOR INPUT
13	AUDIO OUTPUT	14	BYPASS
15	V_{CC}		

BLOCK DIAGRAM (Top View)



EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (Ta=25 °C)

Supply Voltage	V_{CC}	15	V
Input Voltage	V_i	3	$V_{p\text{-}p}$
Package Dissipation at Ta = 75 °C	P_d	310	mW
Operating Temperature	T_{opt}	-30 to 75	°C
Storage Temperature	Tstg	-40 to 125	°C

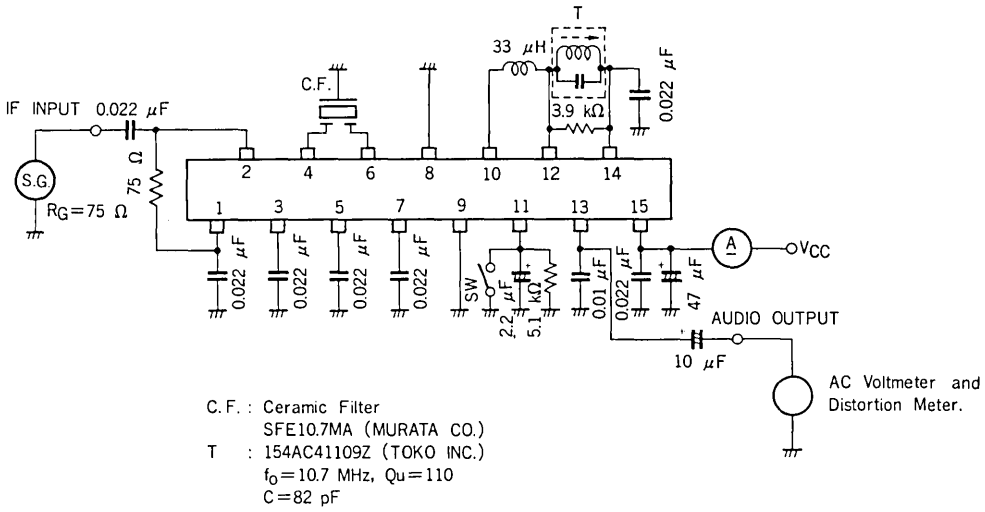
RECOMMENDED OPERATING CONDITIONS (Ta = 25 °C)

Operating Supply Voltage	V_{CC}	10	V
Supply Voltage Range	V_{CC}	7 to 12	V
Operating Ambient Temperature	Ta	-30 to 75	°C

ELECTRICAL CHARACTERISTICS (Ta = 25 °C, V_{CC} = 10 V, f = 10.7 MHz, $f_{mod.}$ = 400 Hz, DEV. = ±22.5 kHz)

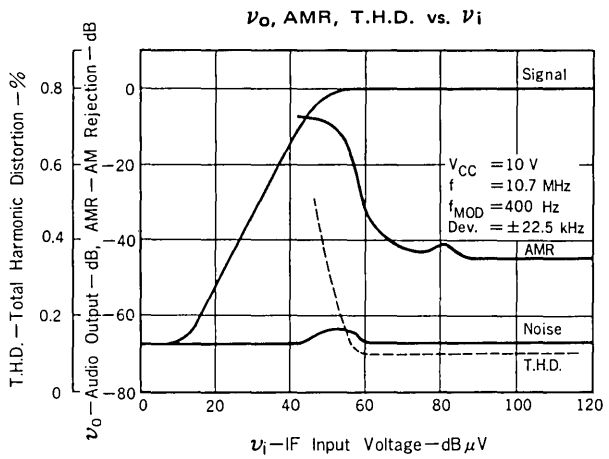
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	I_{CC}	12	19	25	mA	v_i = 0 dBμV
Limiting Sensitivity (1)	$v_{i(lim)1}$		47	53	dBμV	-3 dB point, V_R = 0 Ω, SW : ON
Recovered Audio Voltage	v_o	110	150	200	mVr.m.s.	v_i = 100 dBμV
AM Rejection	AMR		45		dB	v_i = 100 dBμV, AM: $f_{mod.}$ = 400 Hz, m = 30 %
Signal-to-Noise Ratio	S/N		67		dB	v_i = 100 dBμV
Total Harmonic Distortion	T.H.D.		0.1	0.5	%	v_i = 100 dBμV
Limiting Sensitivity (2)	$v_{i(lim)2}$		50		dBμV	-3 dB point, V_R = 5.1 kΩ, SW : OFF

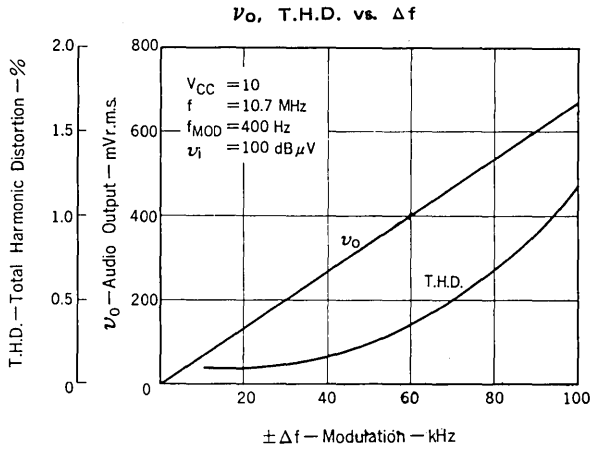
TEST CIRCUIT



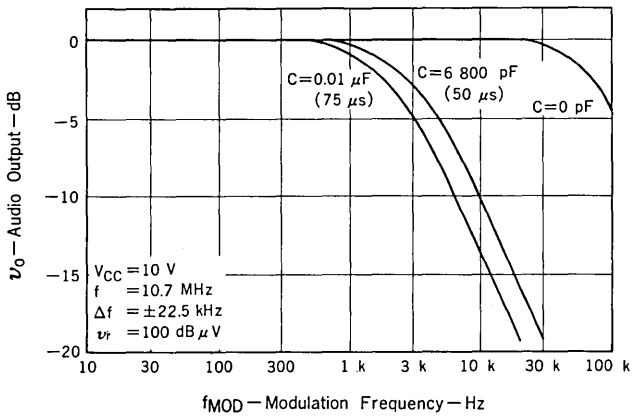
C. F. : Ceramic Filter
SFE10.7MA (MURATA CO.)
T : 154AC41109Z (TOKO INC.)
f_O=10.7 MHz, Qu=110
C=82 pF

TYPICAL CHARACTERISTICS

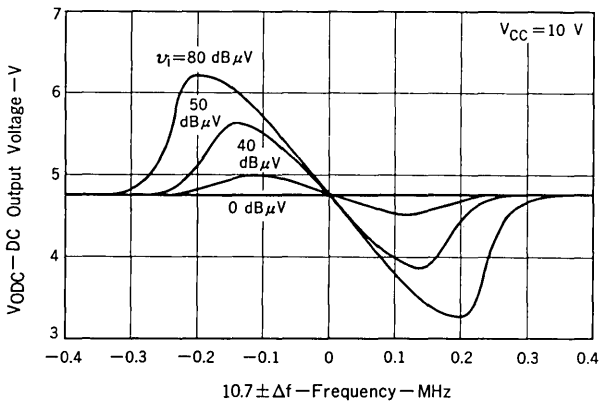




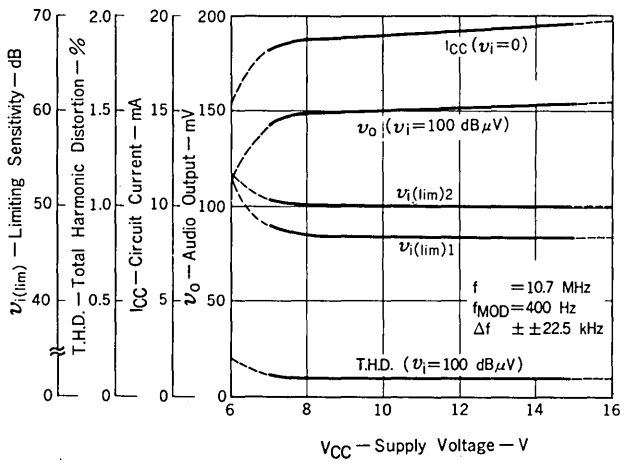
v_o vs. f_{MOD}



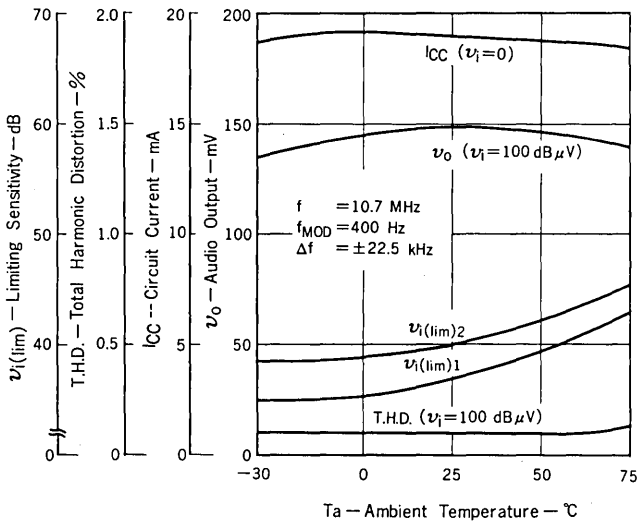
V_{ODC} vs. Δf



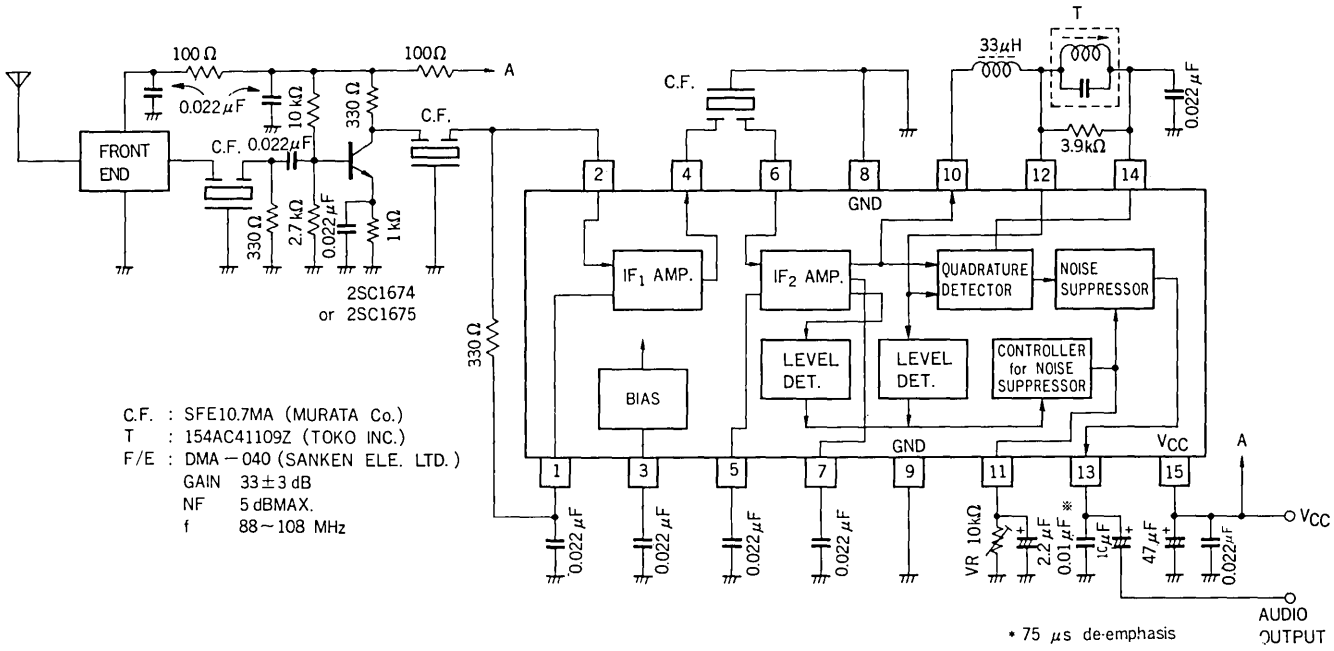
v_o, I_{CC}, T.H.D., $v_{i\,(lim)}$ vs. V_{CC}



v_o, I_{CC}, T.H.D., $v_{i\,(lim)}$ vs. Ta



TYPICAL APPLICATION



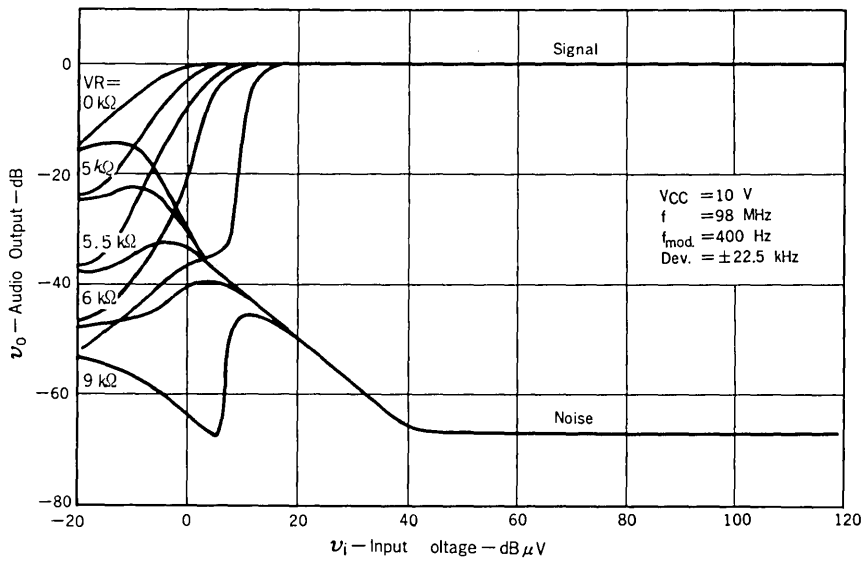
C.F. : SFE10.7MA (MURATA Co.)
T : 154AC41109Z (TOKO INC.)
F/E : DMA−040 (SANKEN ELE. LTD.)
GAIN 33±3 dB
NF 5 dBMAX.
f 88−108 MHz

The procedure below should be carefully followed, in order to get the best use of μPC1200V.

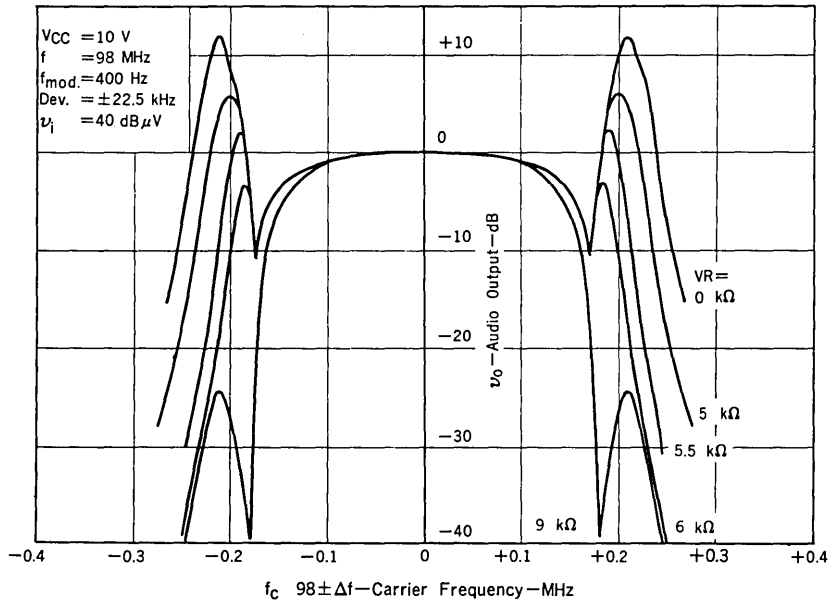
1. Limiting sensitivity should be 5 to 10 dBμV
2. FM TUNER should have Noise Figure as low as possible.
3. VR (connected with pin-11) should be adjusted until the optimum point of low lateral sound and high sensitivity is reached.

TYPICAL PERFORMANCE with complementary stages (Ref. Application Circuit)

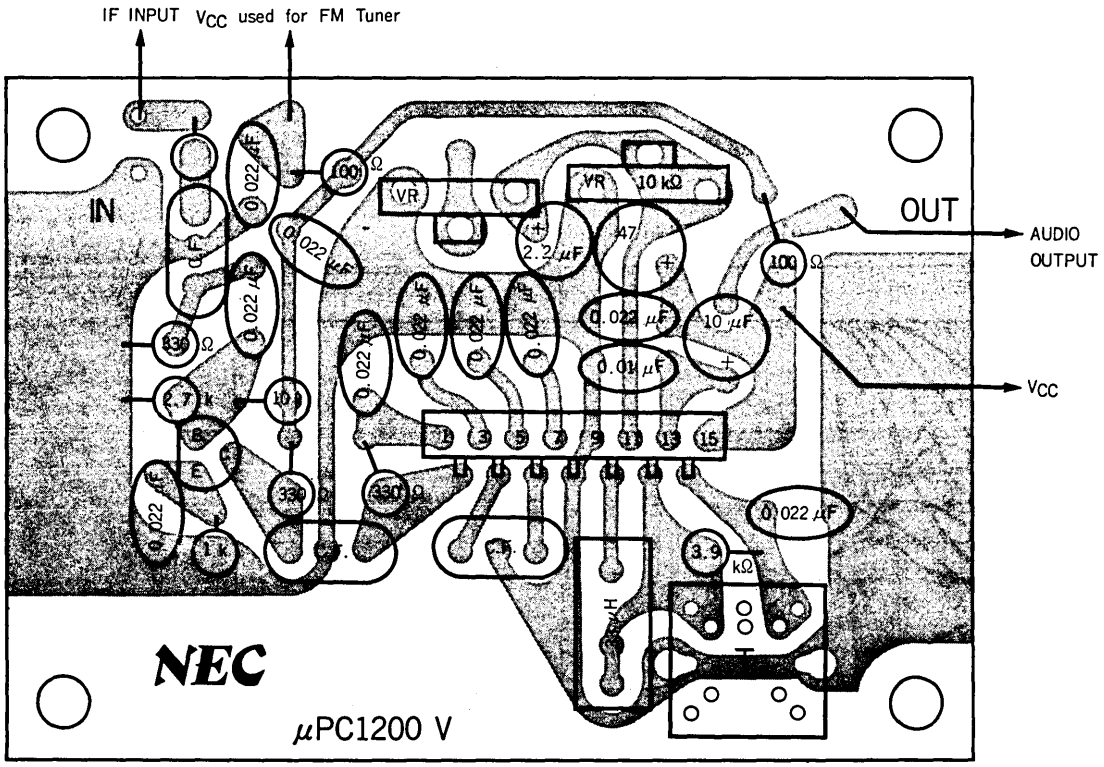
AUDIO OUTPUT vs. INPUT VOLTAGE



AUDIO OUTPUT vs. CARRIER FREQUENCY



COMPONENT LAYOUT FOR P.C. ASSEMBLY (Copper side)



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1245V

FM IF SYSTEM WITH DIFFERENTIAL PEAK DETECTOR SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

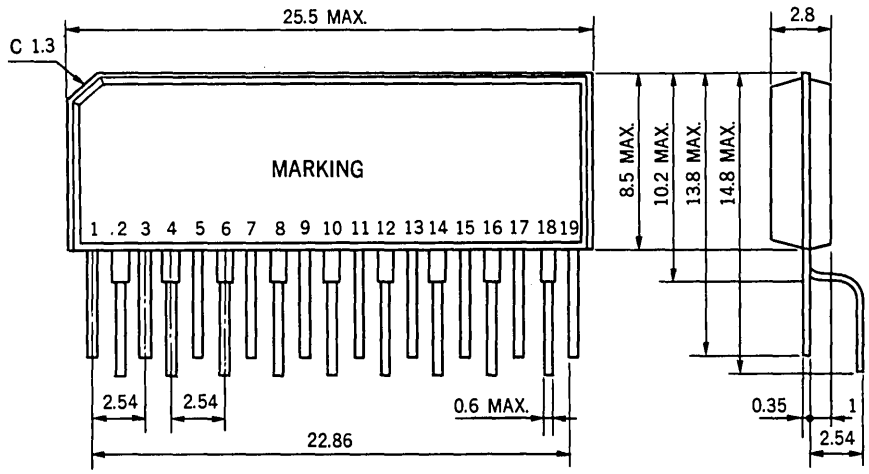
DESCRIPTION

The μPC1245V is a monolithic integrated circuit that provides all the functions of an FM-IF system. It includes a three-stage IF amplifier/limiter configuration with level detectors for each stage, a differential peak detector, and an audio amplifier that features a muting (squelch) circuit. It also includes desirable features such as AGC for the RF tuner, an AFC drive circuit, an output signal to drive a tuning meter and/or provides stereo switching logic, and a station detector that provides a stop signal for search control in Electronically Tuned Radio. The μPC1245V is suitable for use in automotive radio receivers. Outline is 19 leads Vertical Dual In-Line Package. (V-DIP).

FEATURES

- High S+N/N ratio: 67 dB TYP.
- Low distortion with single tune coil: 0.1% TYP.
- Soft muting circuit
- Programmable muting threshold and attenuation level
- Programmable AGC voltage and threshold for RF amplifier
- Programmable deviation where muting occurs and stop signal width
- Reduction of the occupation of mounting area in P.C. Board and hand-insertion time, due to the external shape of the V-DIP.

PACKAGE DIMENSIONS (in millimeters)



ABSOLUTE MAXIMUM RATINGS (Ta=25 °C)

Supply Voltage	V_{CC}	16	V
Input Voltage	V_I	3.0	V
Package Dissipation (Ta=75 °C)	P_D	430	mW
Operating Temperature	T_{opt}	−30 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

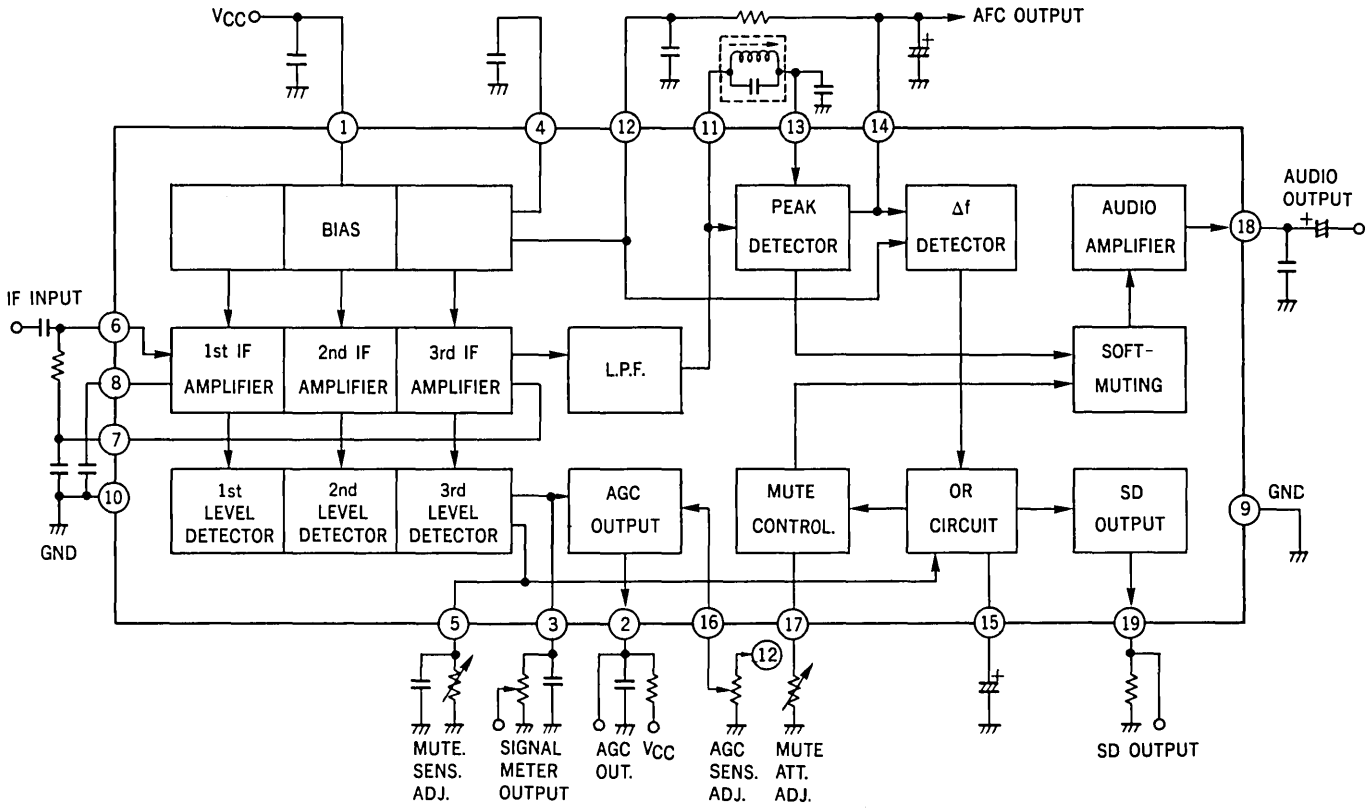
RECOMMENDED OPERATING CONDITION

Supply Voltage Range	V_{CC}	7.0 to 15	V

ELECTRICAL CHARACTERISTICS (Ta=25 °C, V_{CC}=10 V, f=10.7 MHz, f_{MOD}=400 Hz, Δf=±22.5 kHz)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Supply Current	I_{CC}	12	18	25	mA	No Signal
Recovered AF Voltage	v_{OAF}		130		mVr.m.s.	v_i=80 dBμV
Limiting Sensitivity	$v_{i(limit)1}$		44		dBμV	$v_o=v_{oAF}-3$ dB
	$v_{i(limit)2}$		50		dBμV	$v_o=v_{oAF}-3$ dB, Mute ON, R_3=22 kΩ, R_8=5.6 kΩ
Total Harmonic Distortion	T.H.D.		0.1	0.5	%	v_i=80 dBμV
Signal to Noise Ratio	S/N		67		dB	v_i=80 dBμV
AM Rejection Ratio	AMR		42		dB	v_i=80 dBμV, AM: 400 Hz, 30 % mod
Signal Meter Output Voltage	V_{s1}		0		V	v_i=0 dBμV, R_2=4.7 kΩ
	V_{s2}		1.0		V	v_i=60 dBμV, R_2=4.7 kΩ
	V_{s3}		5.3		V	v_i=100 dBμV, R_2=4.7 kΩ
AGC Output	V_{AGC1}		9.0		V	v_i=0 dBμV, V_{16}=3.0 V
	V_{AGC2}		0.1		V	v_i=100 dBμV, V_{16}=3.0 V
AFC Output	V_{AFC}		5.2		V	v_i=80 dBμV
Stop Signal Width	BW_{SD}		100		kHz	v_i=80 dBμV, R_5=5.6 kΩ, V_{SD}=5 V, R_9=3.3 kΩ

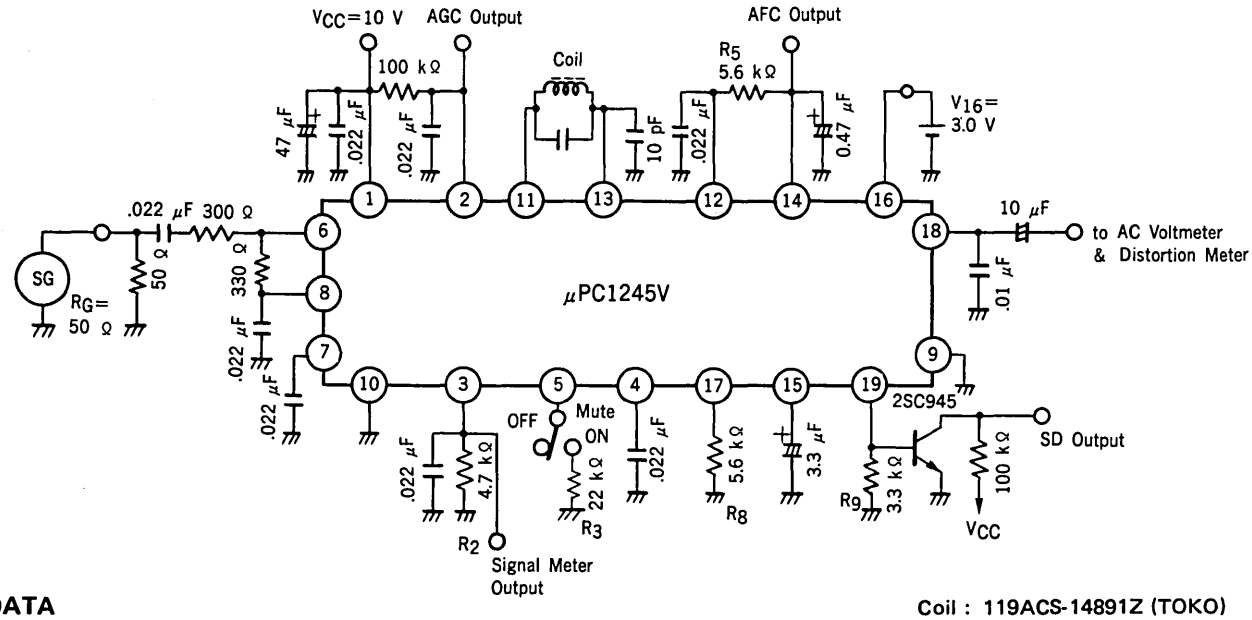
BLOCK DIAGRAM



CONECTION DIAGRAM

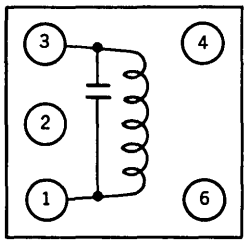
Pin No.	Electrical Connection	Pin No.	Electrical Connection
1	V_{CC}	2	AGC Output
3	Signal Meter Output	4	Bypass
5	Mute Sensitivity Adj.	6	IF Input
7	IF Bypass	8	IF Bypass
9	GND	10	GND
11	Detector Input (+)	12	Reference Voltage
13	Detector Input (–)	14	AFC Output
15	Bypass	16	AGC Sensitivity Adj.
17	Mute Att. Adj.	18	Audio Output
19	SD Output		

TEST CIRCUIT



COIL DATA

Coil : 119ACS-14891Z (TOKO)



(Bottom View)

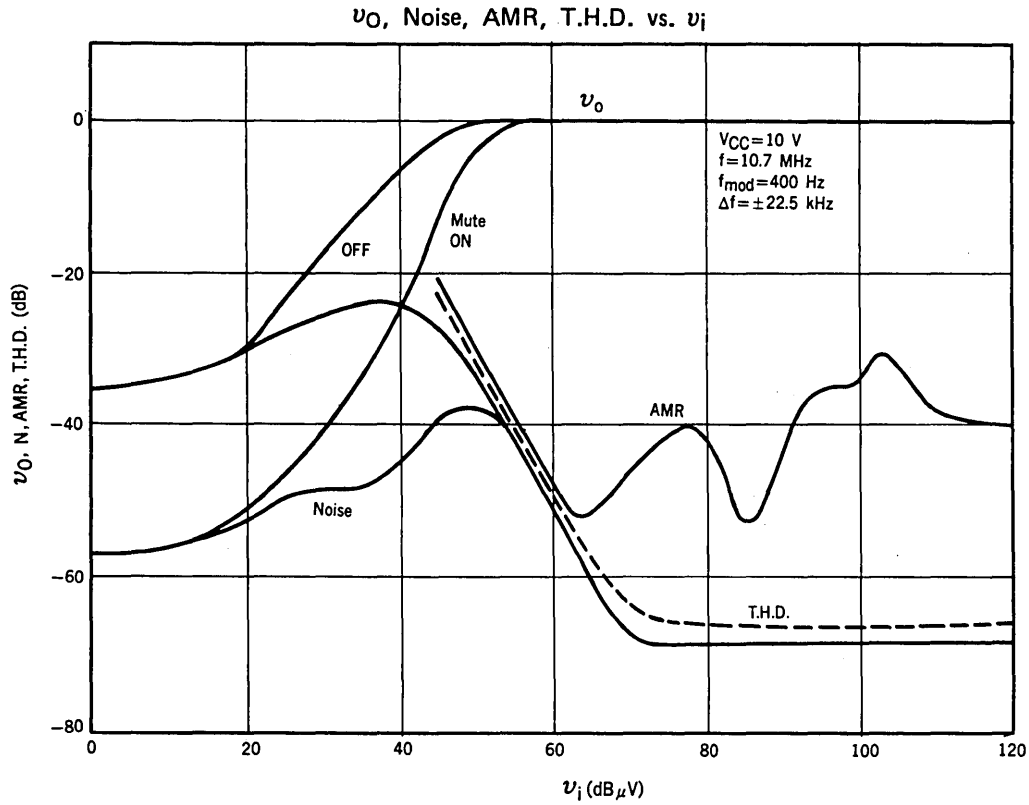
Type No.
119ACS-14891Z(TOKO INC.)

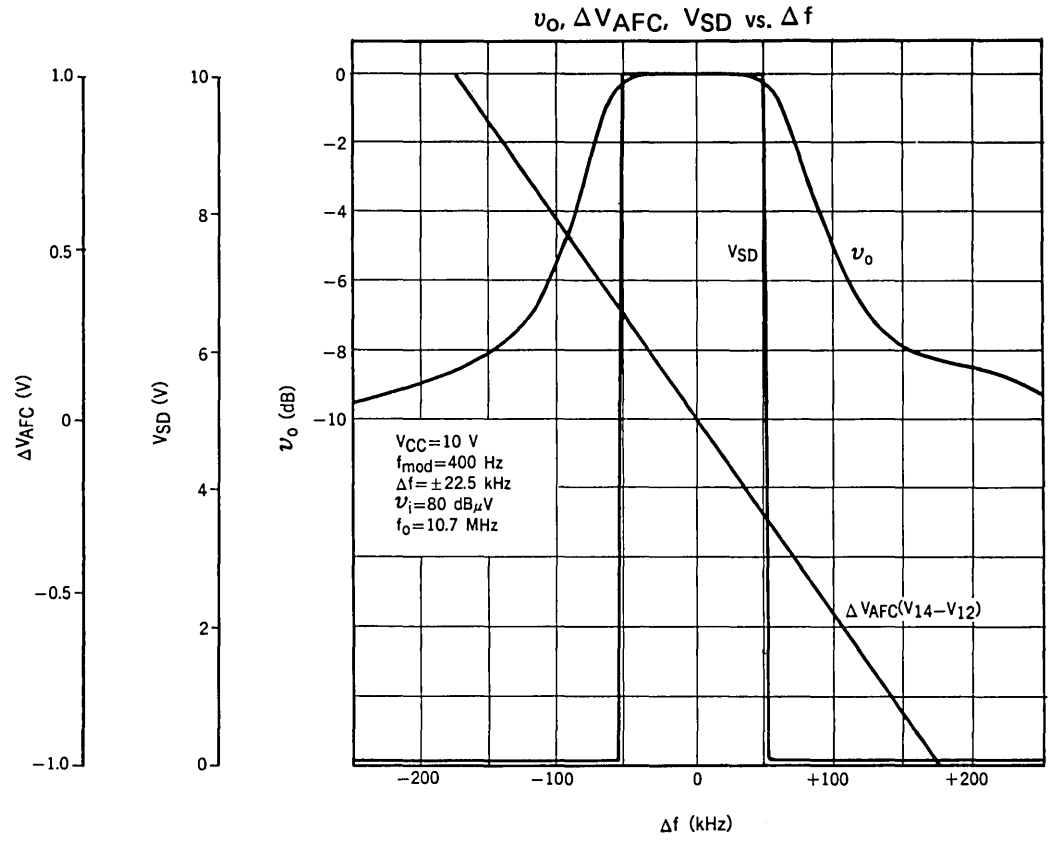
① — ③ 21T

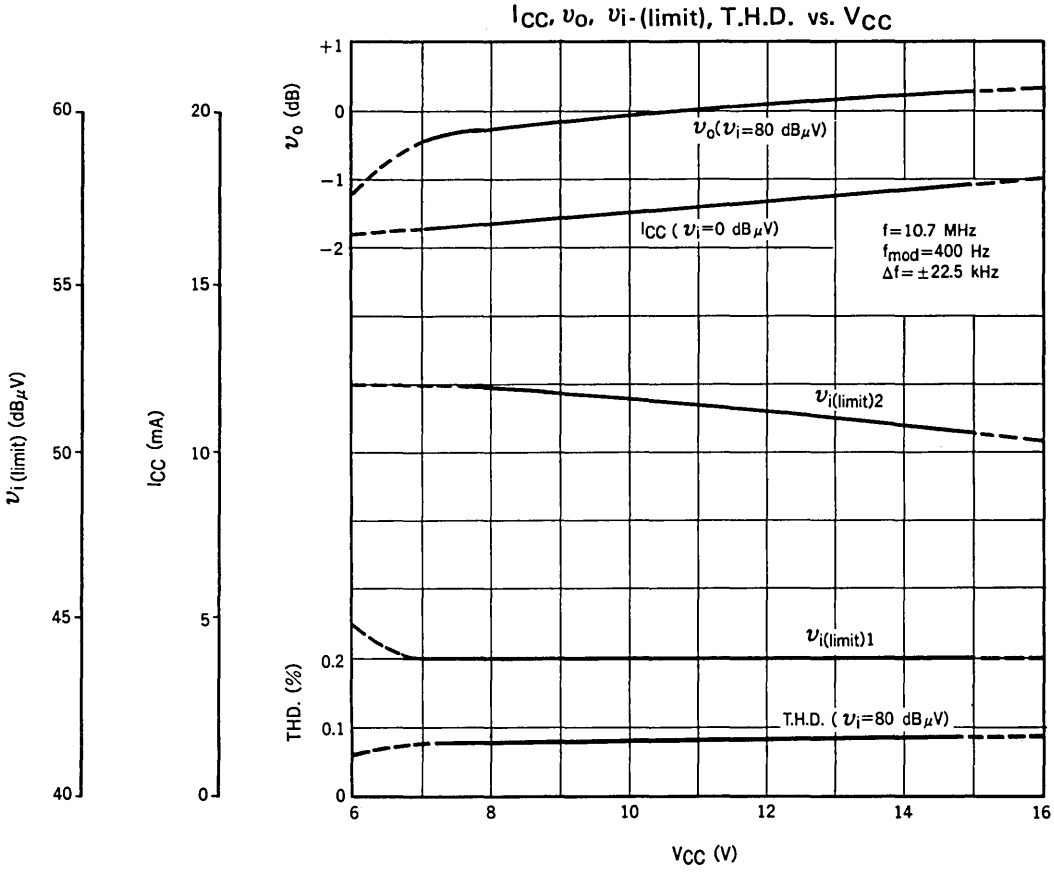
C_t=22 pF

Q_u=90 MIN.

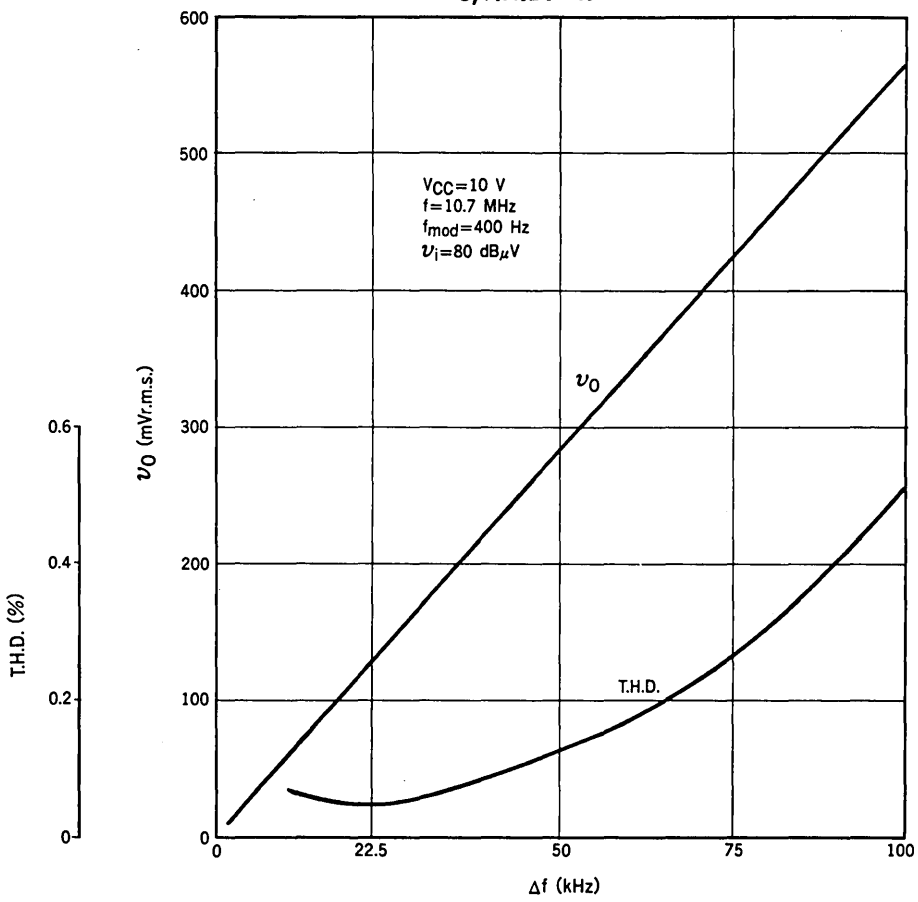
TYPICAL PERFORMANCE CHARACTERISTICS (Ta=25 °C)



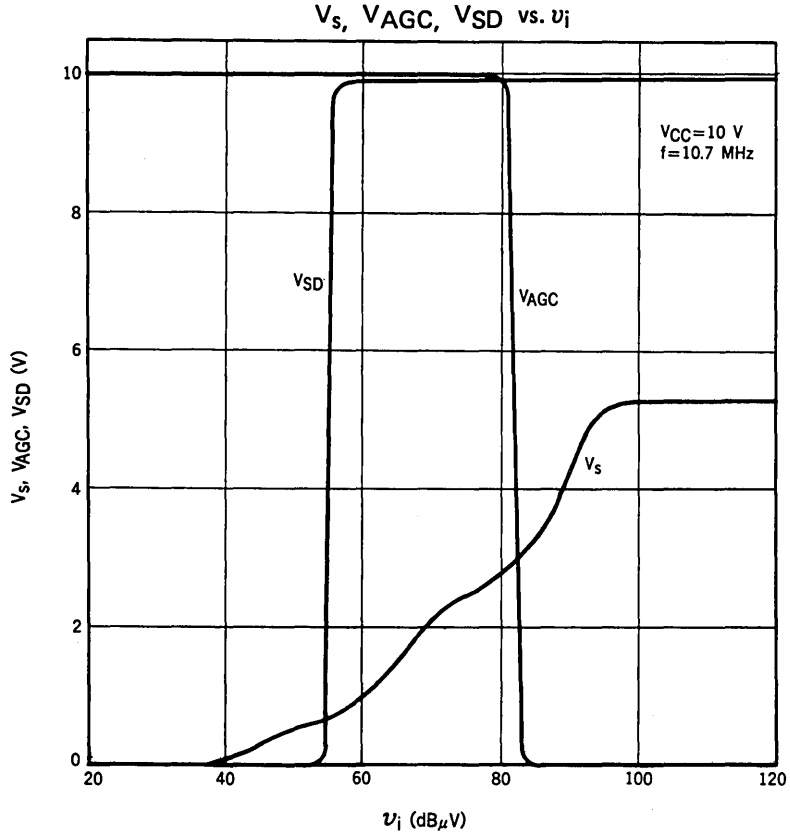

v_o, ΔV_{AFC}, V_{SD} vs. Δf
ΔV_{AFC} (V)
V_{SD} (V)
v_o (dB)
V_{CC}=10 V
f_{mod}=400 Hz
Δf=±22.5 kHz
v_i=80 dBμV
f_o=10.7 MHz
V_{SD}
v_o
$\Delta V_{AFC}(V_{14}-V_{12})$
Δf (kHz)


I_{CC}, v_o, v_i-(limit), T.H.D. vs. V_{CC}
v_i (limit) (dBμV)
I_{CC} (mA)
v_o (dB)
THD. (%)
v_o(v_i=80 dBμV)
I_{CC} (v_i=0 dBμV)
f=10.7 MHz
f_{mod}=400 Hz
Δf=±22.5 kHz
$v_{i(limit)2}$
$v_{i(limit)1}$
T.H.D. (v_i=80 dBμV)
V_{CC} (V)

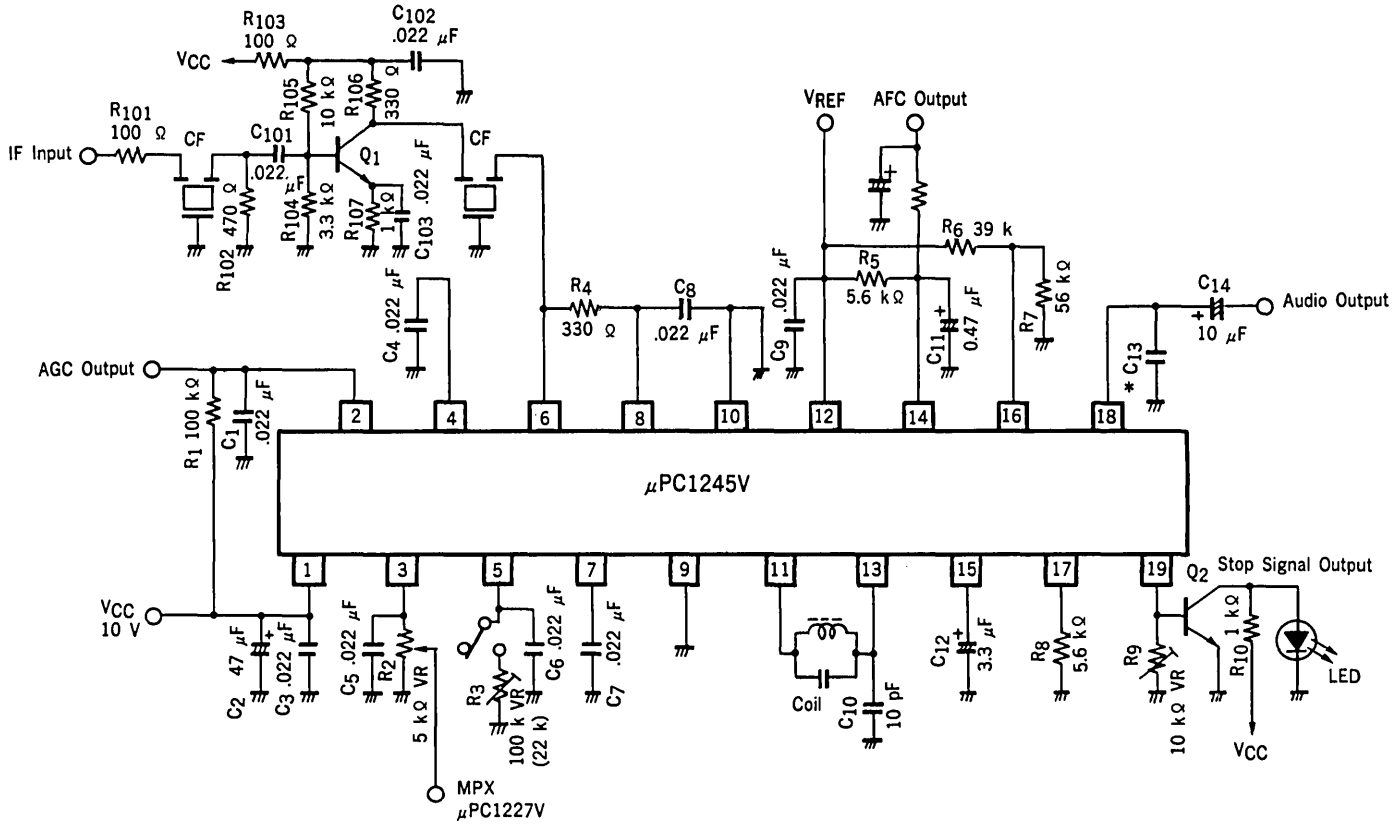
v_O, T.H.D. vs. Δf



V_s, V_{AGC}, V_{SD} vs. v_i

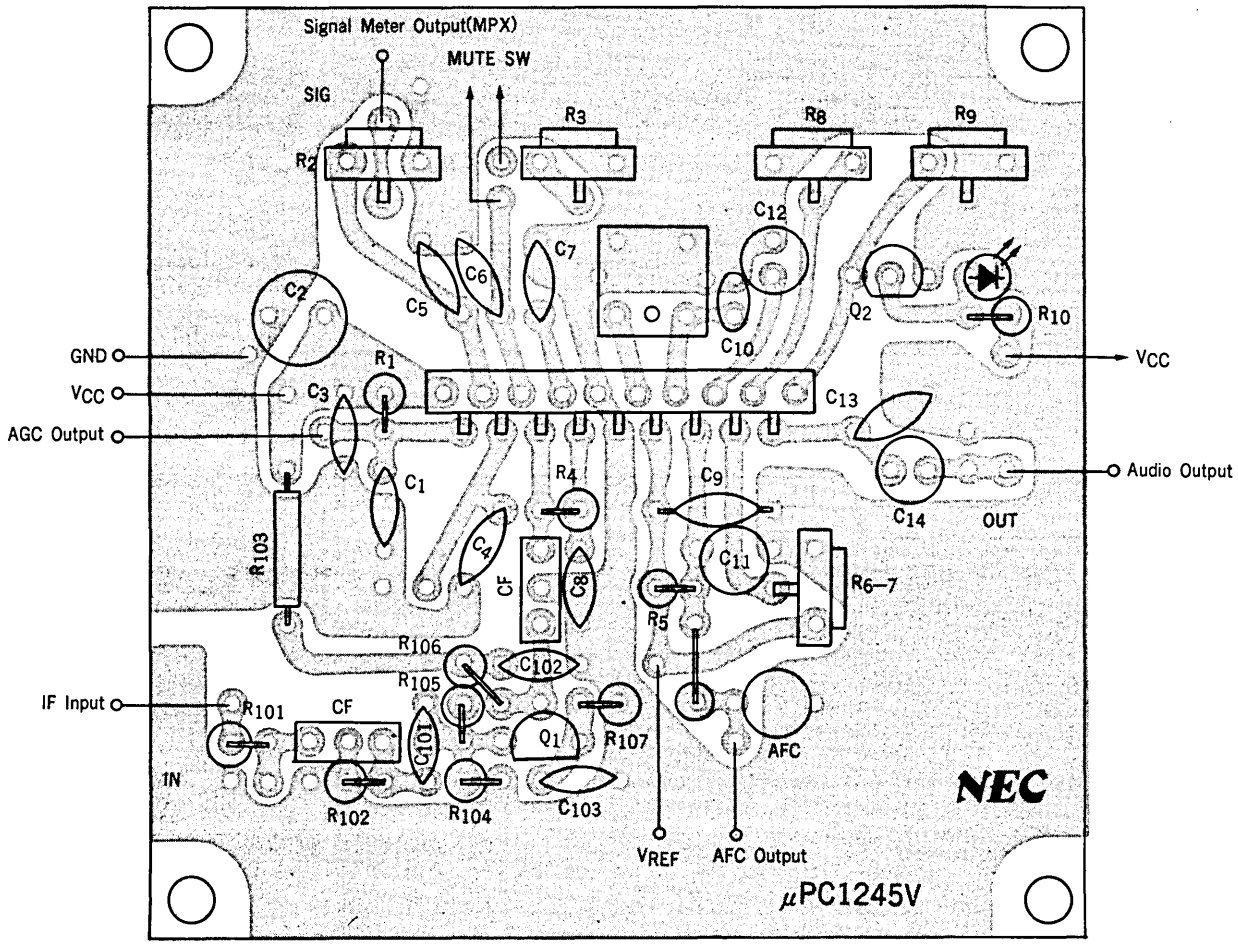


TYPICAL APPLICATION



Coil : 119ACS-14891Z (TOKO) or quivalent
Ceramic filter : SFE10.7MS2 (MURATA) or quivalent
Q_1 : 2SC1675, 2SC1674 or quivalent
Q_2 : 2SC945 or quivalent
* C_{13} : 0.01 μF 75 μs deemphasis

COMPONENT LAYOUT FOR P.W. ASSEMBLY (Copper Side)



BIPOLAR ANALOG INTEGRATED CIRCUIT
μPC587C2

FM MULTIPLEX STEREO DEMODULATOR
SILICON MONOLITHIC BIPOLAR INTEGRATED CIRCUIT

DESCRIPTION

The μPC587C2 is a silicon monolithic integrated circuit designed for FM multiplex stereo demodulator applications in FM stereo radio receivers using phase locked loop (P.L.L.) techniques.

The device contains a demodulator system, a voltage controlled oscillator, phase detectors, low pass filters, dividers and a D.C. amplifier.

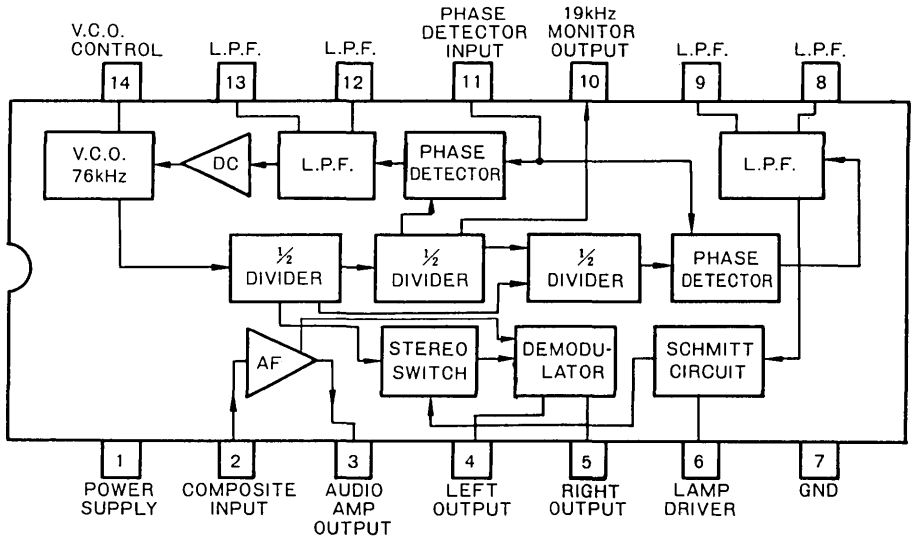
It also includes a stereo-monaural switching circuit and a driver circuit for a stereo indicator lamp.

The features available in the device make possible a system delivering high fidelity sound within the cost restrains of inexpensive stereo receivers.

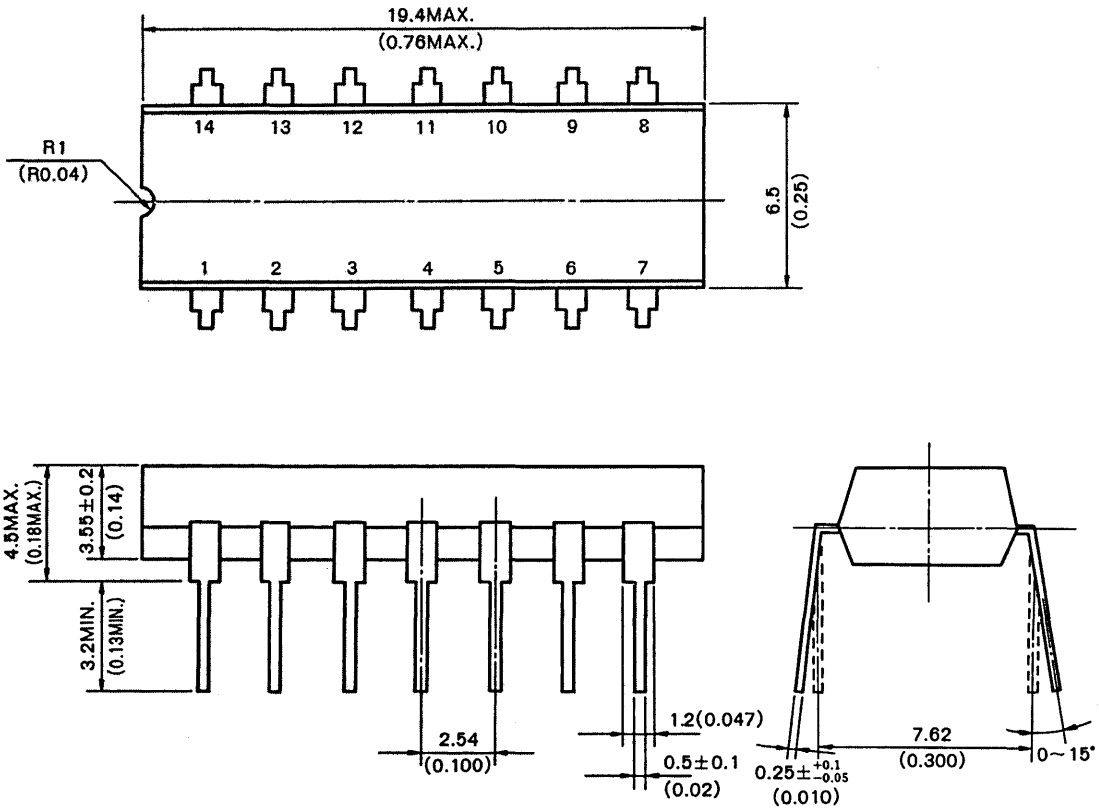
FEATURES

- No coil necessary, all tuning performed with single potentiometer.
- Automatic stereo/monaural switching.
- Wide supply operating voltage range : V_{CC}=7 to 16V.
- Low distortion at monaural operation : T.H.D.=0.07% TYP. at f=1kHz, v_{in}=300mV
- Replaceable to the μPC1026C

BLOCK DIAGRAM

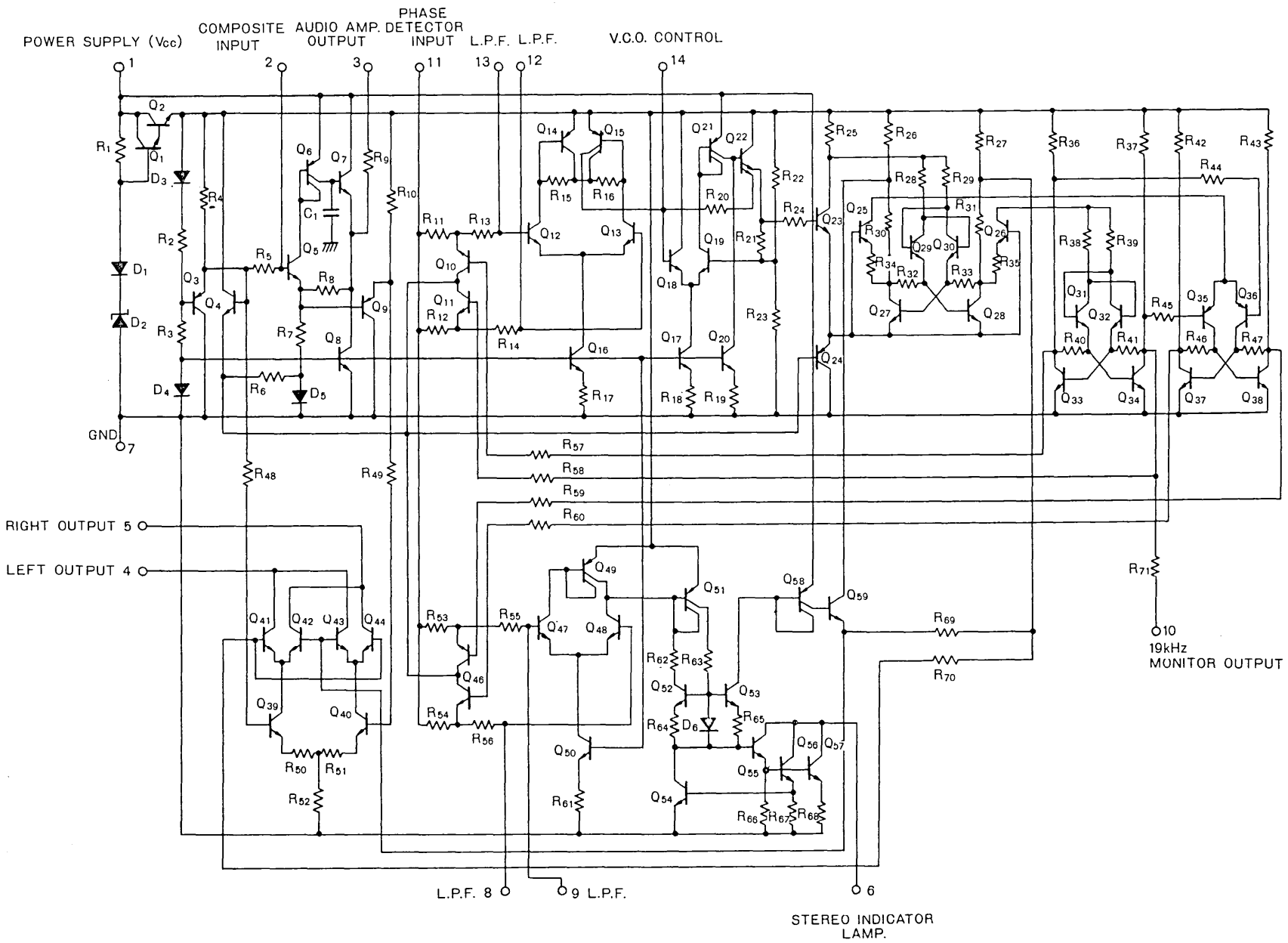


PACKAGE DIMENSIONS AND CONNECTION DIAGRAM (Top View)



Pin No.	Electrical Connections	Pin No.	Electrical Connections
1	POWER SUPPLY (V_{CC})	8	L.P.F.
2	COMPOSITE INPUT	9	L.P.F.
3	AUDIO AMP. OUTPUT	10	19kHz MONITOR OUTPUT
4	LEFT CHANNEL OUTPUT	11	PHASE DETECTOR INPUT
5	RIGHT CHANNEL OUTPUT	12	L.P.F.
6	LAMP DRIVER	13	L.P.F.
7	GND.	14	V.C.O. CONTROL

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Supply Voltage	Vcc	16V
Package Dissipation (Ta=75℃)	P_D	350mW
Lamp Driver Current (Pin 6)	I_L	100mA
Operating Temperature	T_{opt}	−20 to +75℃
Storage Temperature	T_{stg}	−40 to +125℃

RECOMMENDED CONDITIONS (Ta=25℃)

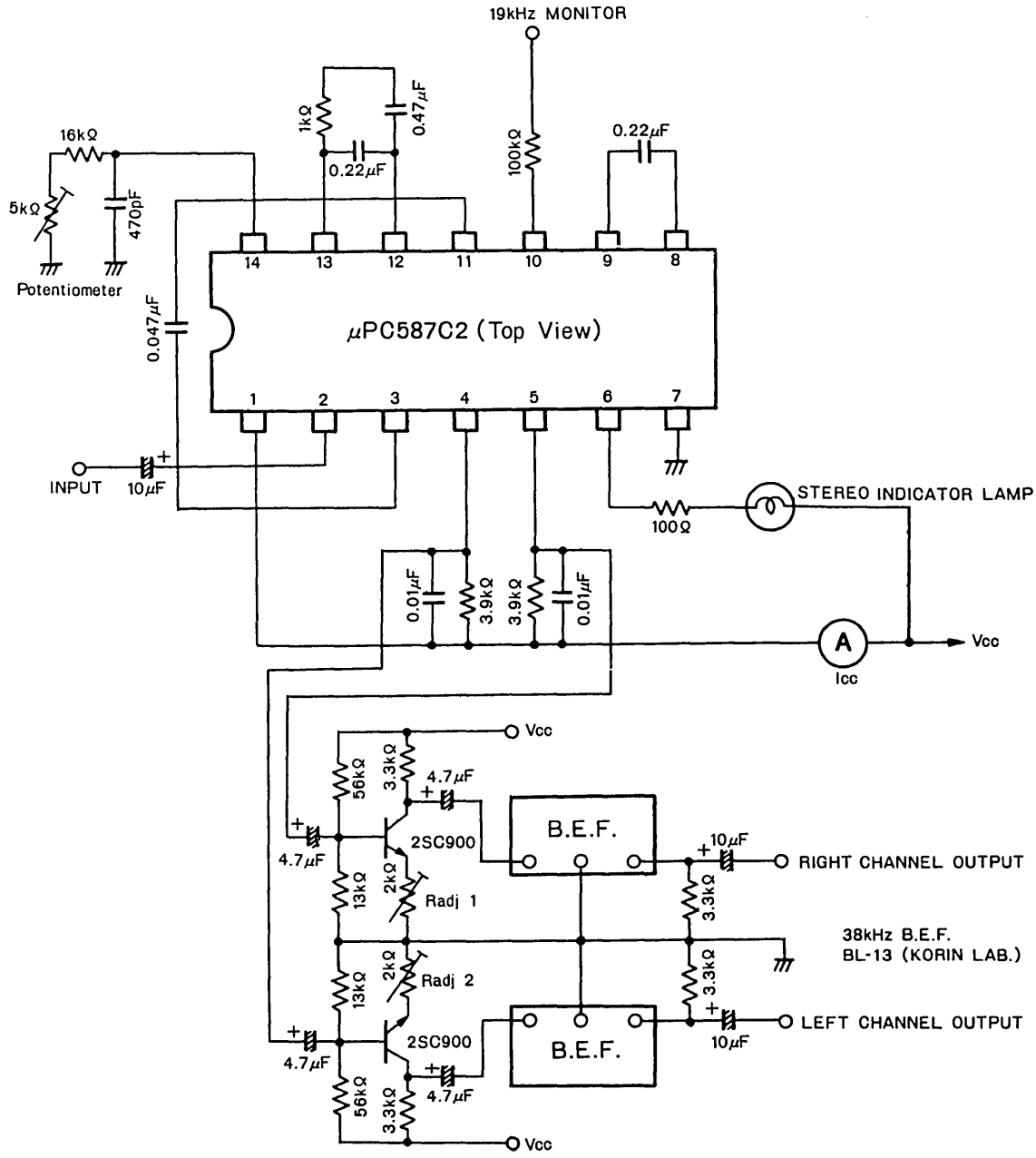
Operating Supply Voltage	Vcc	10V
Supply Voltage Range		7 to 16V
Operating Ambient Temperature	Ta	−20 to +75℃

ELECTRICAL CHARACTERISTICS

[Ta=25℃, Vcc=10V, v_{in}=300mV $\left(\frac{\text{Pilot}}{\text{Composite}}=\frac{1}{10}\right)$, f=1kHz, R_L=3.9kΩ]

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	Icc	7	13	18	mA	Quiescent
Input Impedance	Zi		50		kΩ	
Stereo Channel Separation	Sep.	30	40		dB	f=100Hz, v_{in} (Pilot)=30mV
		35	45		dB	f=1kHz, v_{in} (Pilot) =30mV
		30	40		dB	f=10kHz, v_{in} (Pilot) =30mV
Voltage Gain	A_v	−9	−6		dB	Monaural Input, v_{in} (L+R) =300mV
Channel Balance	Ch.B.	−1.5	0	1.5	dB	Monaural Input, v_{in} (L+R) =300mV
	Ch.B.	−1.5	0	1.5	dB	Stereo Input, v_{in} (Pilot) =30mV
Total Harmonic Distortion	T.H.D.		0.07	0.5	%	Monaural Input, v_{in} (L+R) =300mV
			0.15	0.5	%	Stereo Input, v_{in} (Pilot) =30mV
Lamp Indicator Input Level	LAMP ON	12	16	20	mV	Pilot Level
Lamp Hysteresis		3	6	9	dB	Pilot Level
Capture Range	C.R.	±1.5	±3		%	v_{in} (Pilot) =30mV
Ultrasonic Frequency Rejection	19kHz Rej.		35		dB	19kHz, v_{in} (Pilot) =30mV
	38kHz Rej.		45		dB	38kHz, v_{in} (Pilot) =30mV
SCA Rejection	SCA Rej.		70		dB	$\frac{\text{Pilot}}{\text{Composite}}=\frac{1}{10}$, $\frac{\text{SCA}}{\text{Composite}}=\frac{1}{10}$
Maximum Input Level	v_i	0.7	1		Vrms	Monaural Input, T.H.D.=1%

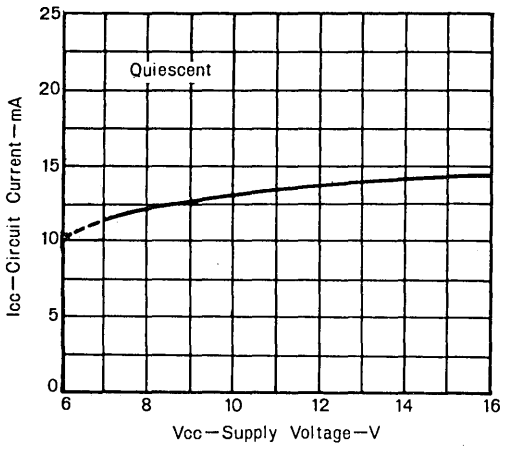
TEST CIRCUIT



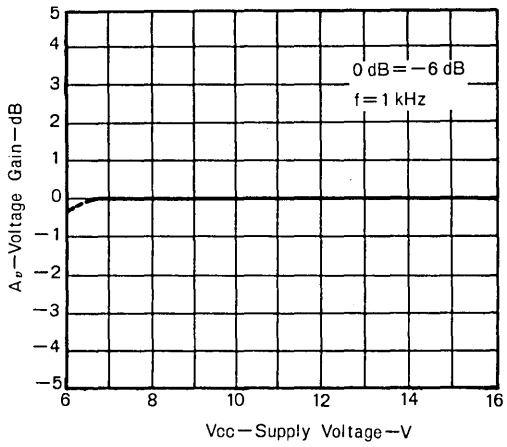
1. Use a polystylene capacitor to the 470pF capacitor connected pin 14 for temperature compensation to V.C.O.
2. Radj 1 and Radj 2 should be set the voltage gain between the output terminal of the IC and the output terminal of the B.E.F. is 0dB.
3. For tuning the V.C.O. perform with the 5kΩ potentiometer connected pin 14 by reading a frequency of 19kHz at Pin 10.

TYPICAL CHARACTERISTICS (Ta=25℃)

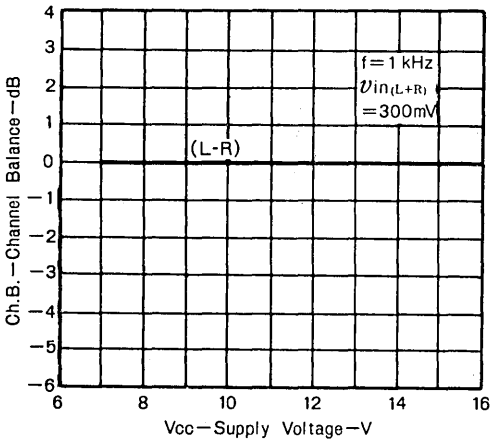
CIRCUIT CURRENT
vs. SUPPLY VOLTAGE



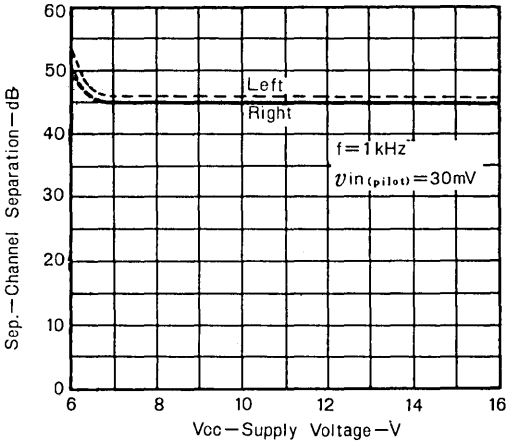
VOLTAGE GAIN
vs. SUPPLY VOLTAGE (Monaural)



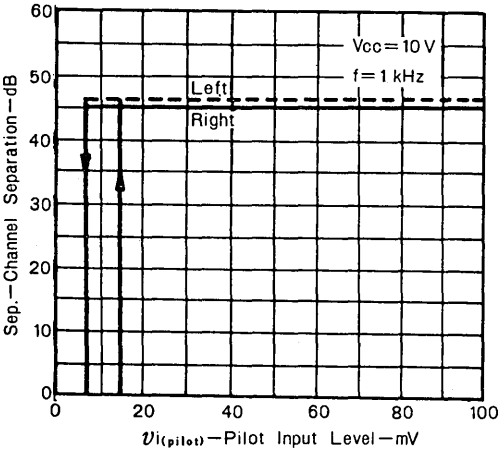
CHANNEL BALANCE
vs. SUPPLY VOLTAGE (Monaural)



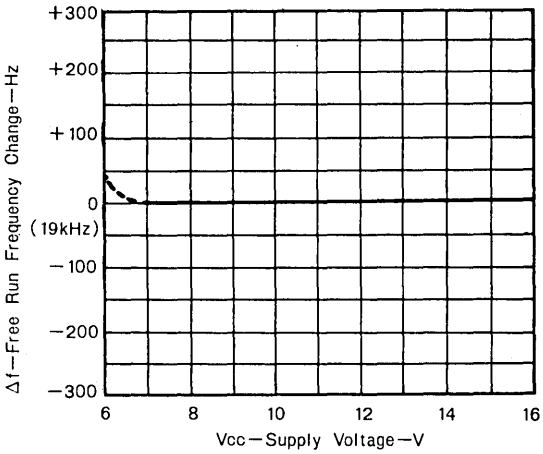
CHANNEL SEPARATION
vs. SUPPLY VOLTAGE



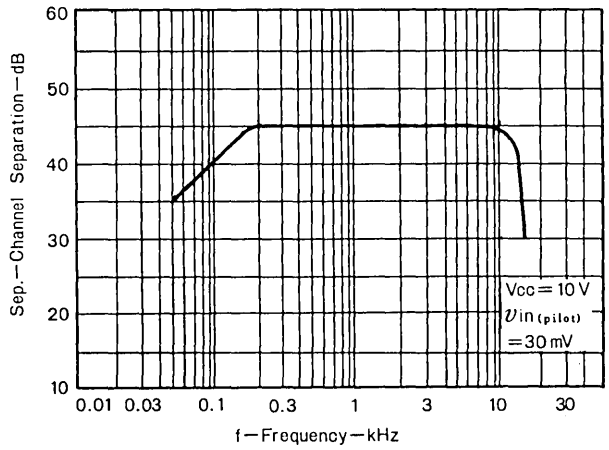
CHANNEL SEPARATION
vs. PILOT INPUT LEVEL



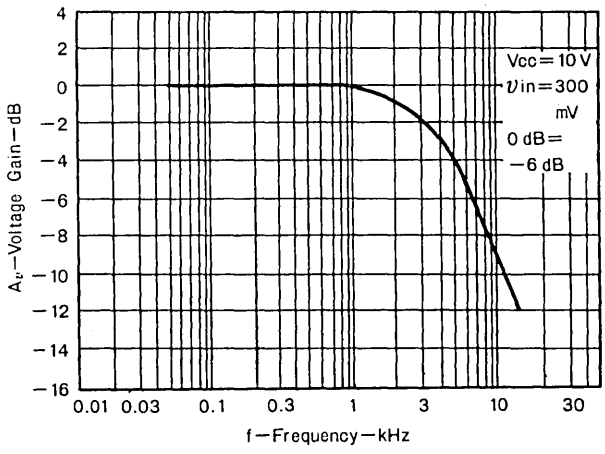
FREE RUN FREQUENCY CHANGE
vs. SUPPLY VOLTAGE



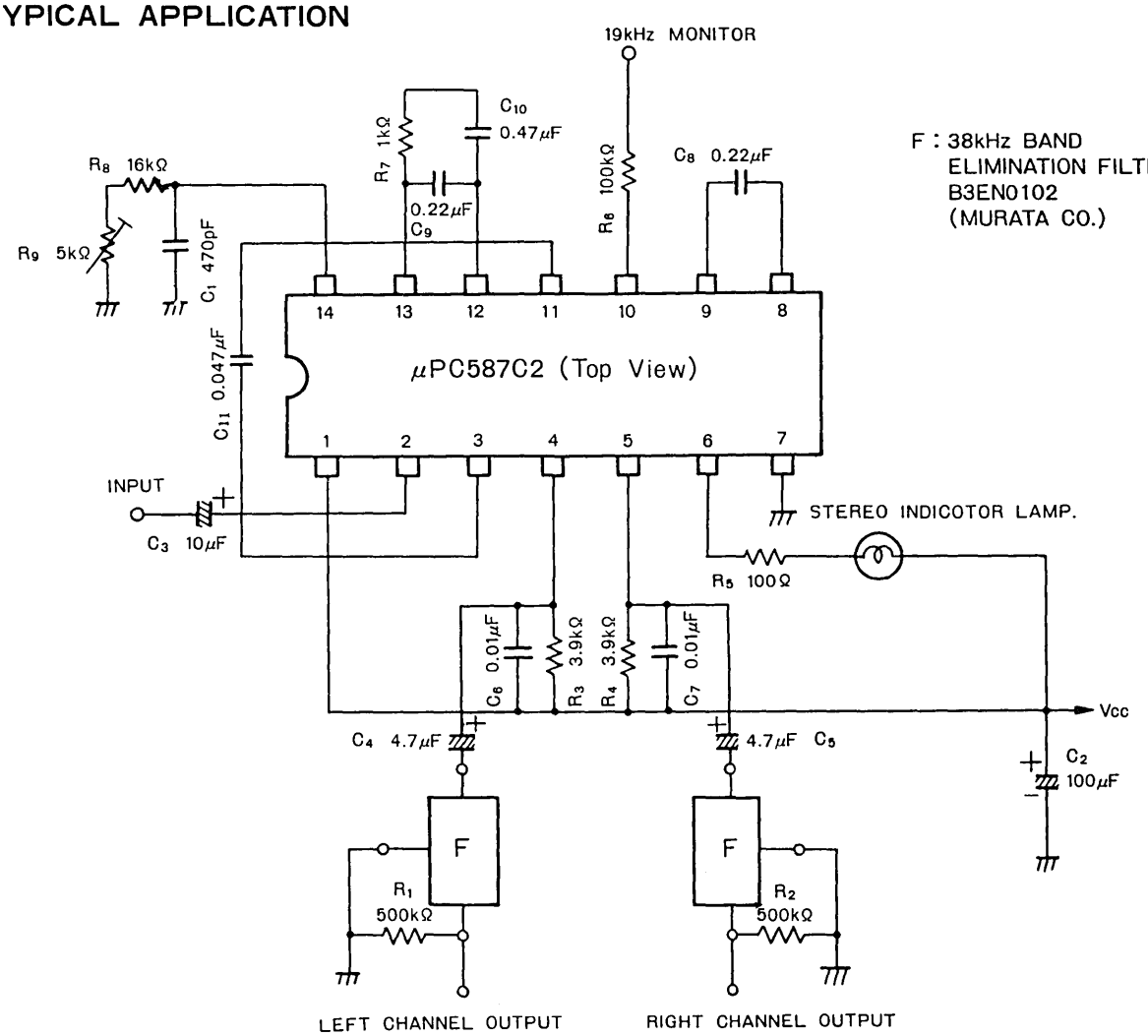
CHANNEL SEPARATION
vs. FREQUENCY



VOLTAGE GAIN
vs. FREQUENCY (Monaural)



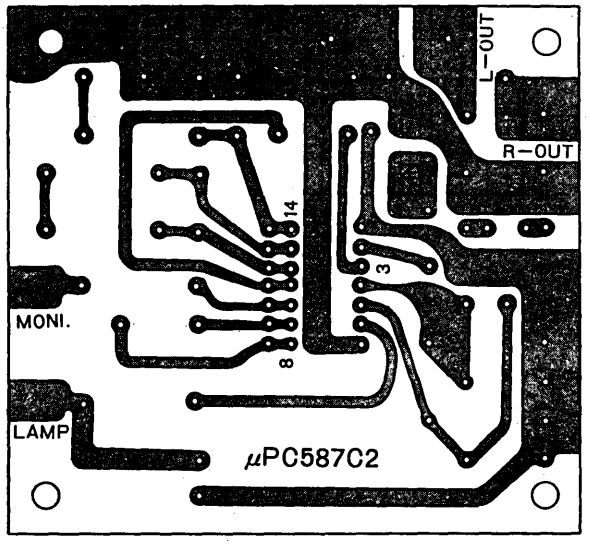
TYPICAL APPLICATION



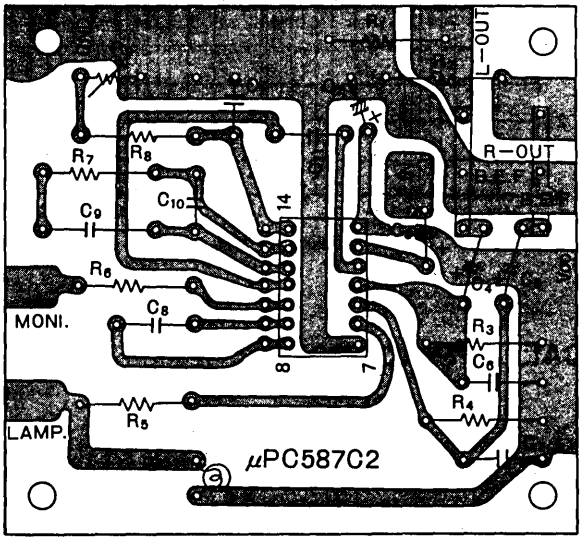
F : 38kHz BAND
ELIMINATION FILTER
B3EN0102
(MURATA CO.)

TYPICAL PRINTED CIRCUIT BOARD PATTERN

PRINTED CIRCUIT LAYOUT



COMPONENT LAYOUT (Bottom View)



R_1=500kΩ	C_1=470pF	C_{10}=0.22μF
R_2=500kΩ	C_2=100μF	C_{11}=0.047μF
R_3=3.9kΩ	C_3=10μF	
R_4=3.9kΩ	C_4=4.7μF	
R_5=100Ω	C_5=4.7μF	
R_6=100kΩ	C_6=0.01μF	
R_7=1kΩ	C_7=0.01μF	
R_8=16kΩ	C_8=0.22μF	
R_9=5kΩ Potentiometer	C_9=0.47μF	

BIPOLAR ANALOG INTEGRATED CIRCUIT
μPC1026C

FM MULTIPLEX STEREO DEMODULATOR
SILICON MONOLITHIC BIPOLAR INTEGRATED CIRCUIT

DESCRIPTION

The μPC1026C is a silicon monolithic integrated circuit designed for FM multiplex stereo demodulator applications in FM stereo radio receivers using phase locked loop (P L L) techniques.

The device contains a demodulator system, a voltage-controlled oscillator, phase detectors, low pass filters, dividers and a D.C. amplifier.

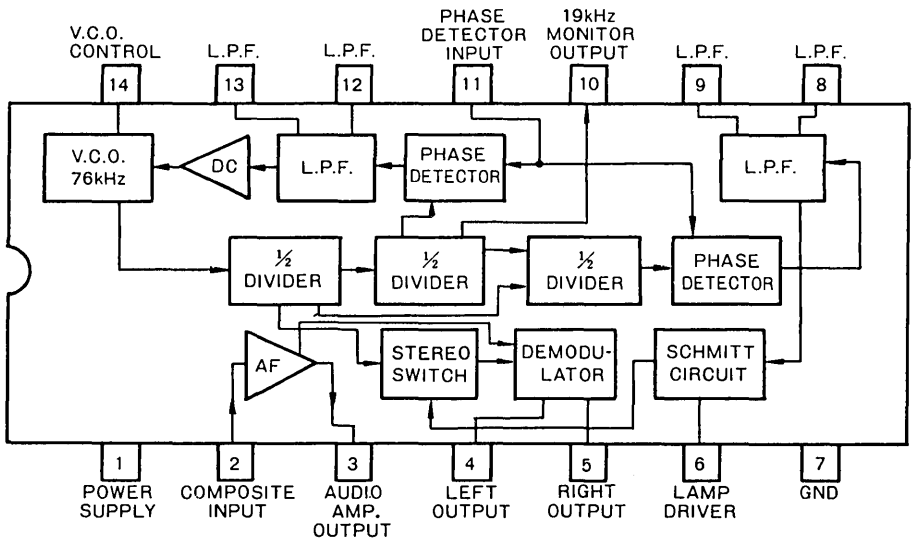
It also includes a stereo-monaural switching circuit and a driver circuit for a stereo indicator lamp.

The features available in the device make possible a system delivering high fidelity sound within the cost restrains of inexpensive stereo receivers.

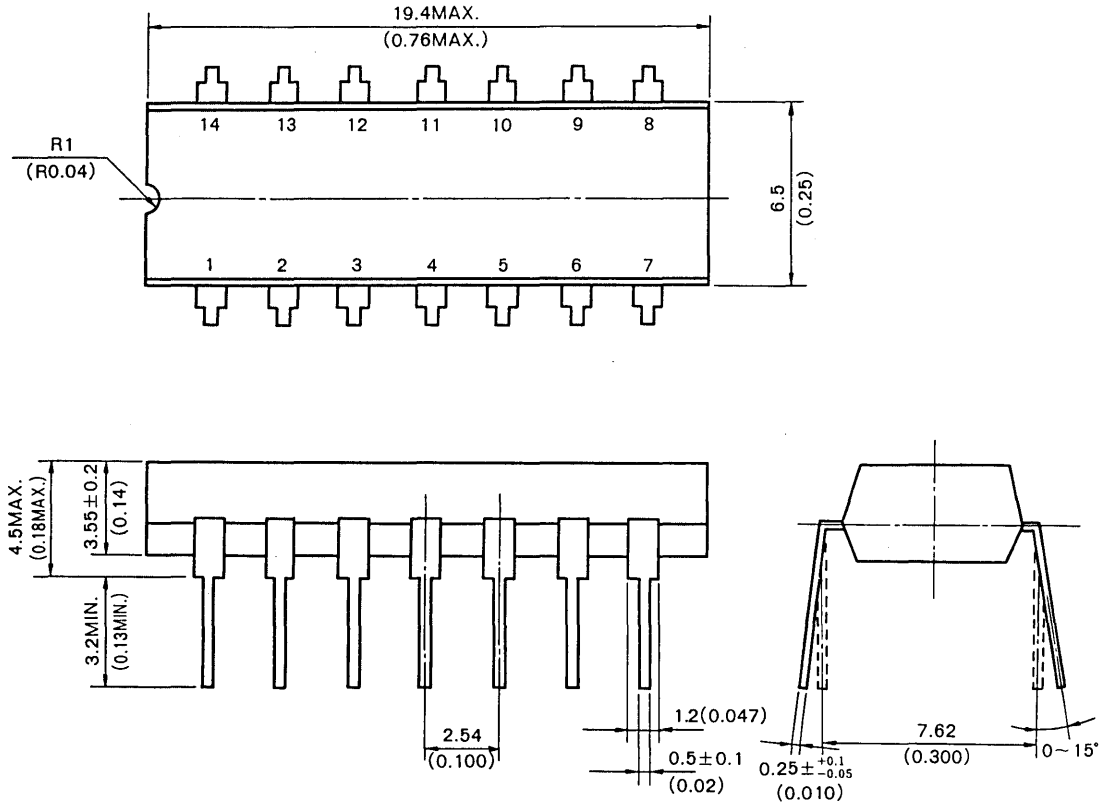
FEATURES

- No coil necessary, all tuning performed with single potentiometer.
- Automatic stereo/monaural switching.
- Wide supply operating voltage range : V_{CC} = 7 to 16V
- High Voltage gain : A_v = −1.5dB (R_L = 3.9kΩ)
- Replaceable to the μPC587C2.

BLOCK DIAGRAM



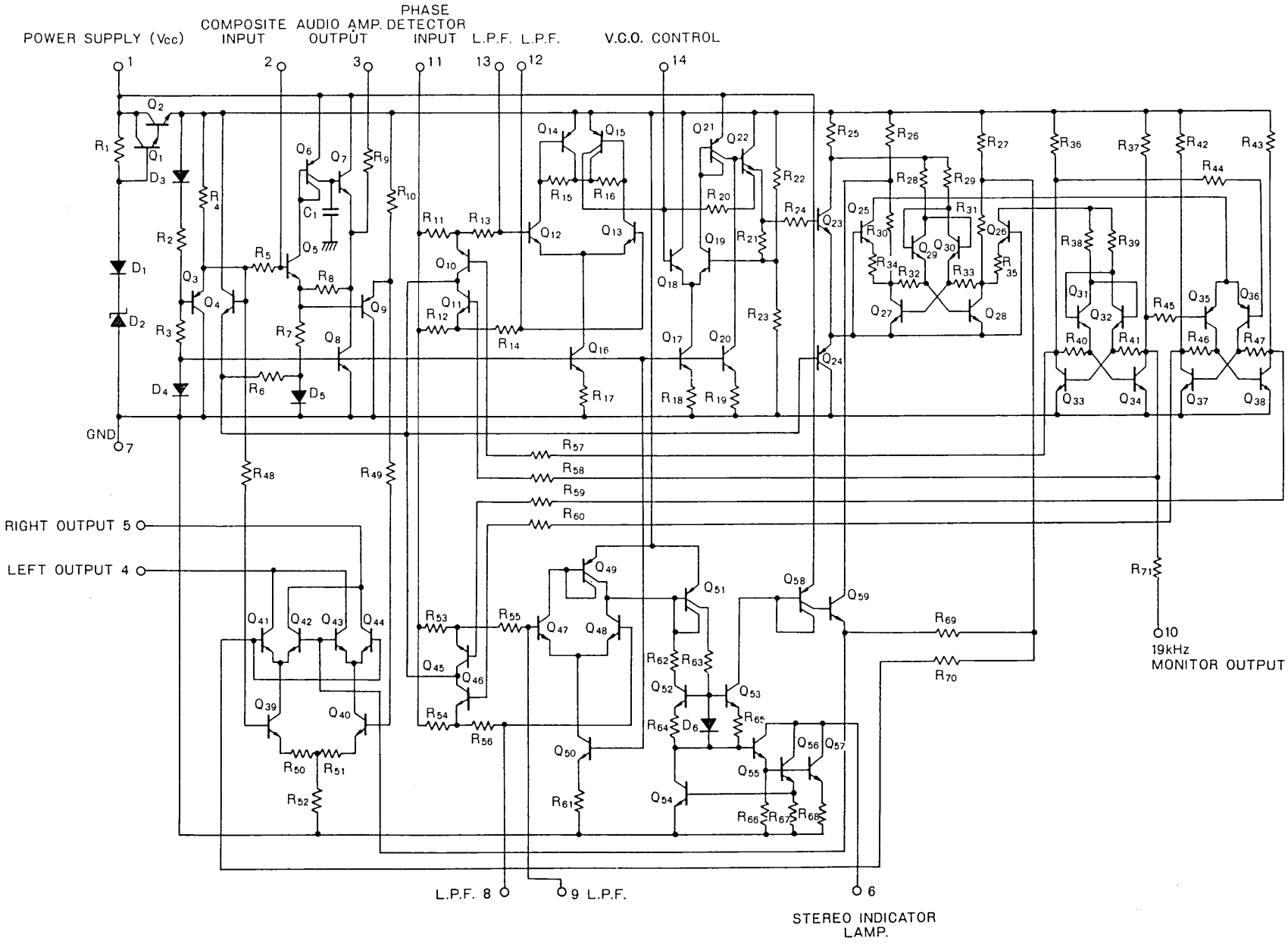
PACKAGE DIMENSIONS in millimeters (inches)



CONNECTION DIAGRAM

Pin No.	Electrical Connections	Pin No.	Electrical Connections
1	POWER SUPPLY (V_{CC})	8	L.P.F.
2	COMPOSITE INPUT	9	L.P.F.
3	AUDIO AMP. OUTPUT	10	19kHz MONITOR OUTPUT
4	LEFT CHANNEL OUTPUT	11	PHASE DETECTOR INPUT
5	RIGHT CHANNEL OUTPUT	12	L.P.F.
6	LAMP DRIVER	13	L.P.F.
7	GND.	14	V.C.O. CONTROL

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Supply Voltage	Vcc	16V
Package Dissipation (Ta=75℃)	P_D	350mW
Lamp Driver Current (Pin 6)	I_L	100mA
Operating Temperature	T_{opt}	−20 to +75℃
Storage Temperature	T_{stg}	−40 to +125℃

RECOMMENDED OPERATING CONDITIONS (Ta=25℃)

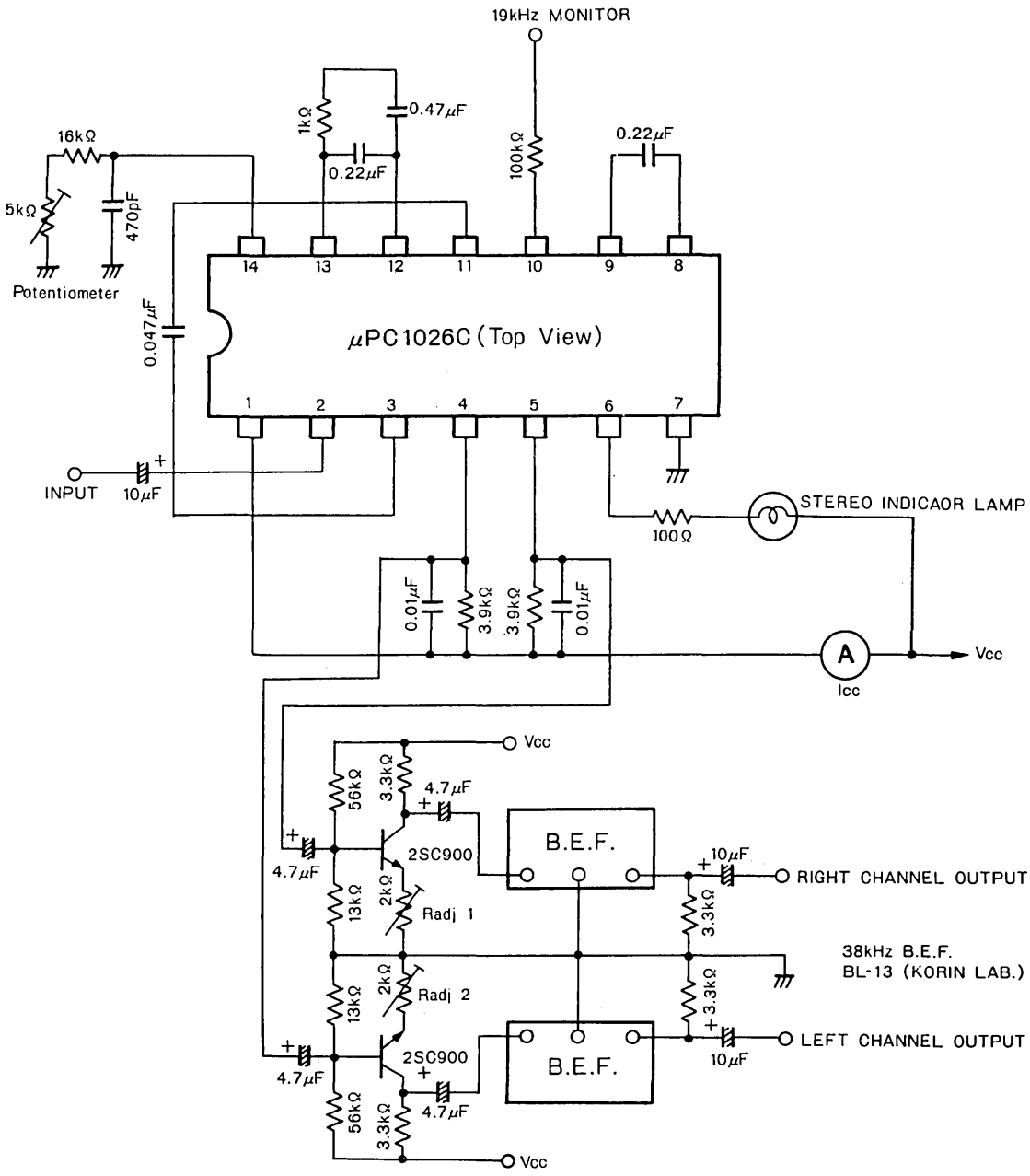
Operating Supply Voltage	Vcc	10V
Supply Voltage Range		7 to 16V
Operating Ambient Temperature	Ta	−20 to +75℃

ELECTRICAL CHARACTERISTICS

(Ta=25℃, Vcc=10V, v_{in}=150mV $\left(\frac{\text{Pilot}}{\text{Composite}}=\frac{1}{10}\right)$, f=1kHz, R_L=3.9kΩ)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	Icc	7	13	18	mA	Quiescent
Input Impedance	Z_i		50		kΩ	
Stereo Channel Separation	Sep.	30	40		dB	f=100Hz, v_{in}(Pilot) =15mV
		35	45		dB	f=1kHz, v_{in}(Pilot) =15mV
		30	40		dB	f=10kHz, v_{in}(Pilot) =15mV
Voltage Gain	A_v	−4.5	−1.5	2.0	dB	Monaural Input, v_{in}(L+R) =150mV
Channel Balance	Ch.B.	−1.5	0	1.5	dB	Monaural Input, v_{in}(L+R) =150mV
	Ch.B.	−1.5	0	1.5	dB	Stereo Input, v_{in}(Pilot) =15mV
Total Harmonic Distortion	T.H.D.		0.15	0.5	%	Monaural Input, v_{in}(L+R) =150mV
			0.15	0.5	%	Stereo Input, v_{in}(Pilot) =15mV
Lamp Indicator Input Level	LAMP ON	5	8	11	mV	Pilot Level
Lamp Hysteresis		3	6	9	dB	Pilot Level
Capture Range	C.R.	±1.5	±3		%	v_{in}(Pilot) =15mV
Ultrasonic Frequency Rejection	19kHz Rej.		35		dB	19kHz, v_{in}(Pilot) =15mV
	38kHz Rej.		45		dB	38kHz, v_{in}(Pilot) =15mV
SCA Rejection	SCA Rej.		70		dB	$\frac{\text{Pilot}}{\text{Composite}}=\frac{1}{10}$, $\frac{\text{SCA}}{\text{Composite}}=\frac{1}{10}$
Maximum Input Level	v_i	0.4	0.6		Vr.m.s.	Monaural Input, T.H.D.=1%

TEST CIRCUIT



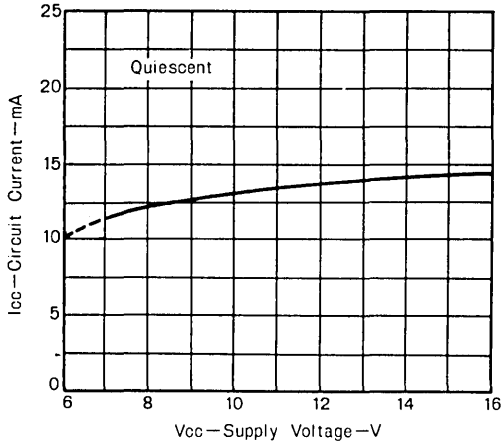
1. Use a polystylene capacitor to the 470pF capacitor connected pin 14 for temperature compensation to V.C.O.

2. Radj 1 and Radj 2 should be set the voltage gain between the output terminal of the IC and the output terminal of the B.E.F. is 0dB.

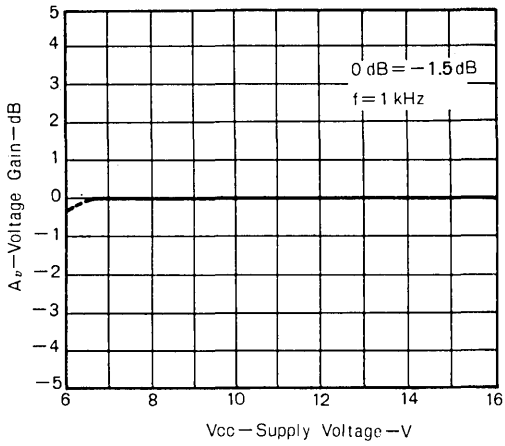
3. For tuning the V.C.O. perform with the 5kΩ potentiometer connected pin 14 by reading a frequency of 19kHz at Pin 10.

TYPICAL CHARACTERISTICS (Ta=25℃)

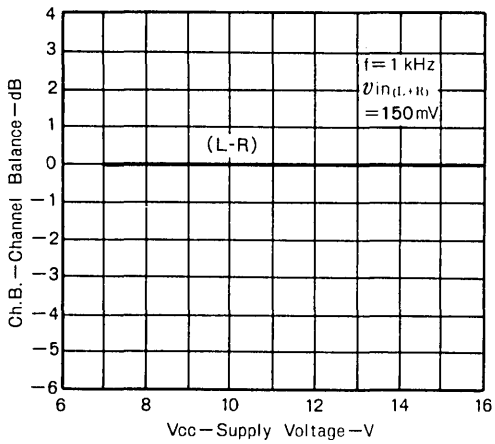
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



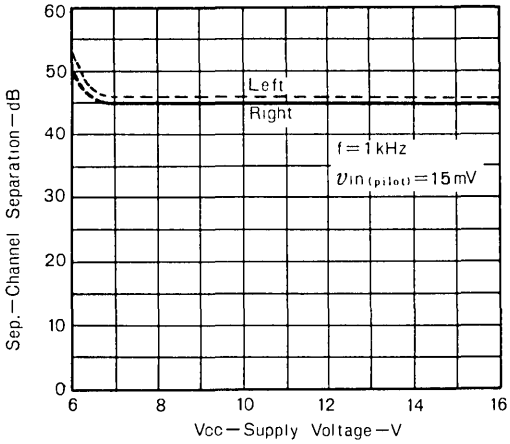
VOLTAGE GAIN vs. SUPPLY VOLTAGE (Monaural)



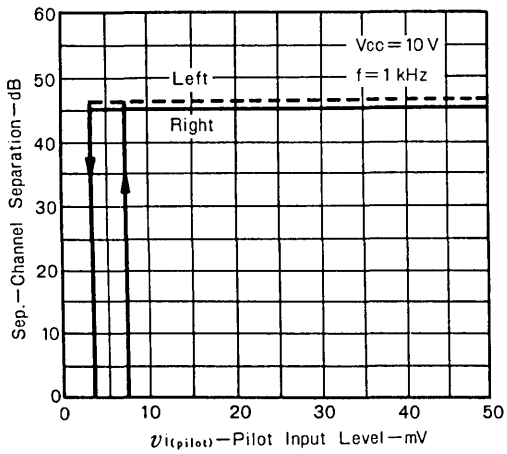
CHANNEL BALANCE vs. SUPPLY VOLTAGE (Monaural)



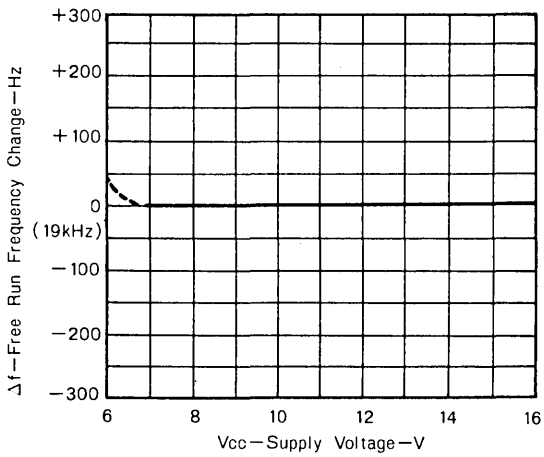
CHANNEL SEPARATION vs. SUPPLY VOLTAGE



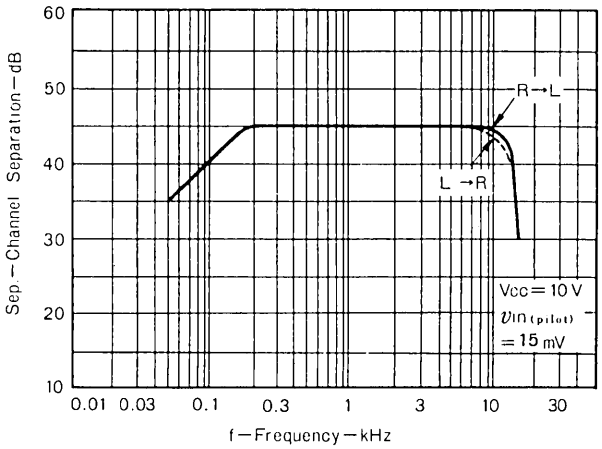
CHANNEL SEPARATION vs. PILOT INPUT LEVEL



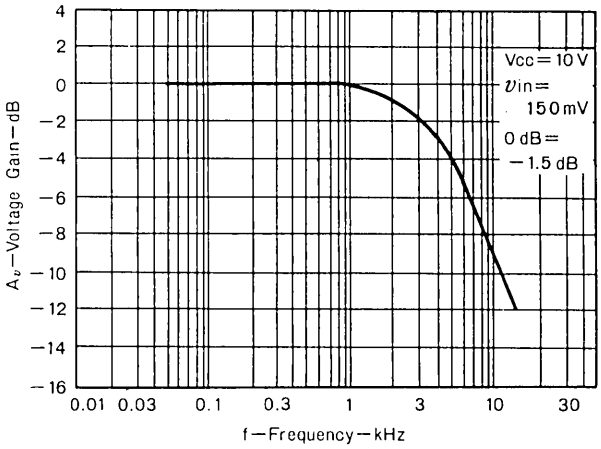
FREE RUN FREQUENCY CHANGE vs. SUPPLY VOLTAGE



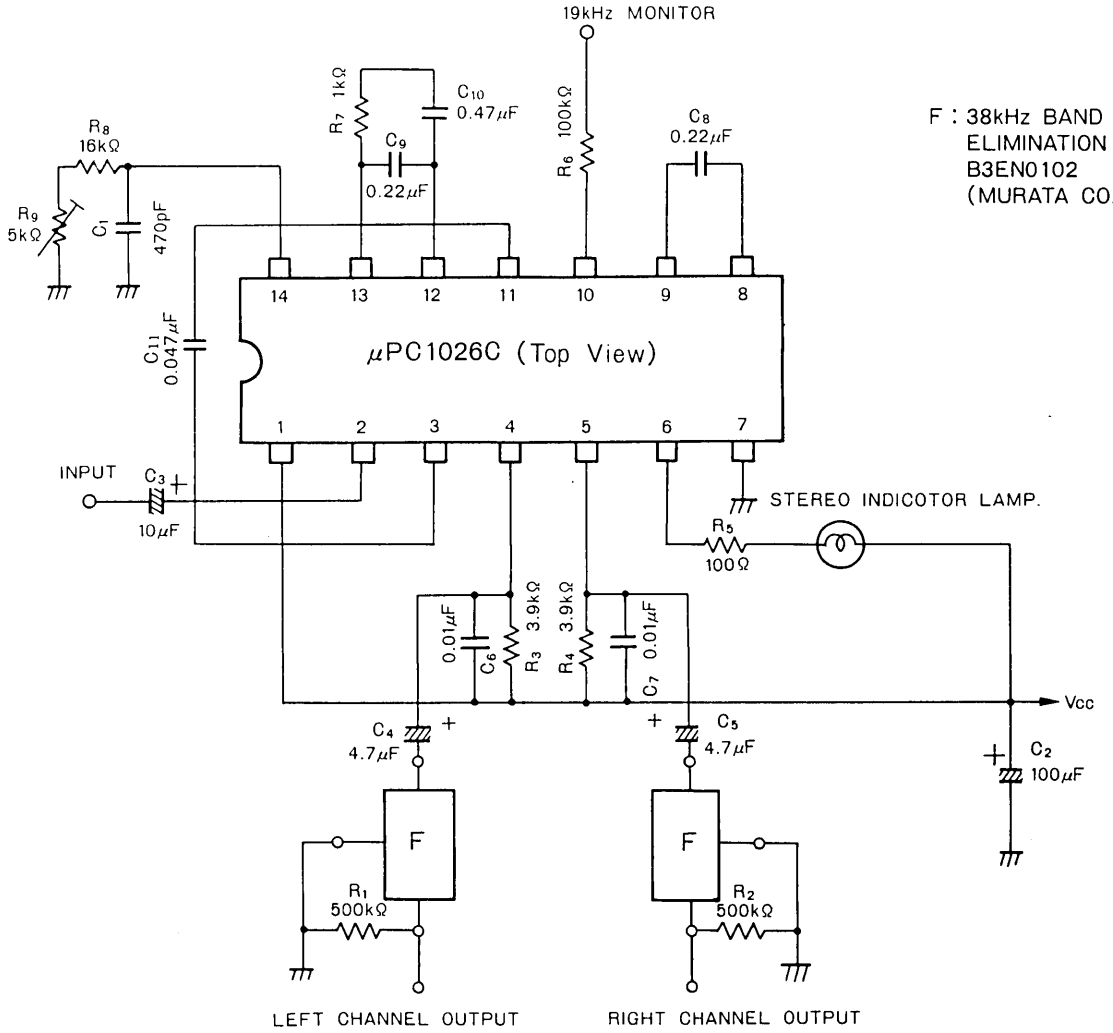
CHANNEL SEPARATION
vs. FREQUENCY



VOLTAGE GAIN
vs. FREQUENCY (Monaural)



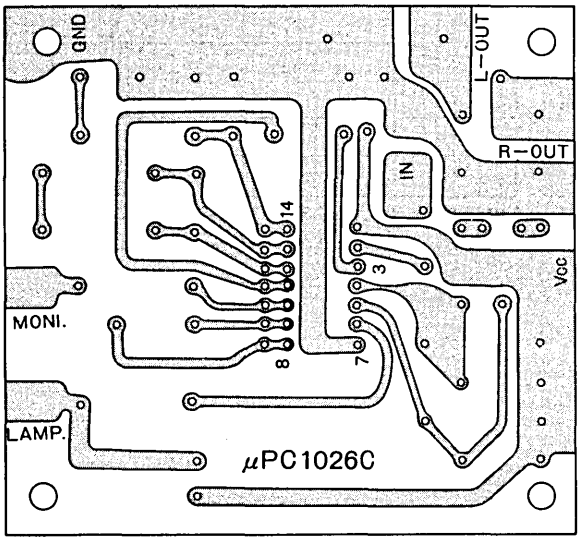
TYPICAL APPLICATION



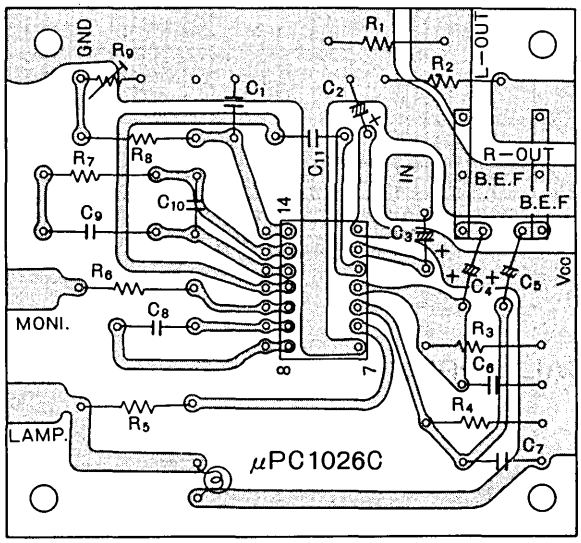
F : 38kHz BAND
ELIMINATION FILTER
B3EN0102
(MURATA CO.)

TYPICAL PRINTED CIRCUIT BOARD PATTERN

PRINTED CIRCUIT LAYOUT



COMPONENT LAYOUT (Bottom View)



R_1=500kΩ	C_1=470pF	C_{10}=0.22μF
R_2=500kΩ	C_2=100μF	C_{11}=0.047μF
R_3=3.9kΩ	C_3=10μF	
R_4=3.9kΩ	C_4=4.7μF	
R_5=100Ω	C_5=4.7μF	
R_6=100kΩ	C_6=0.01μF	
R_7=1kΩ	C_7=0.01μF	
R_8=16kΩ	C_8=0.22μF	
R_9=5kΩ Potentiometer	C_9=0.47μF	

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1227V

FM MULTIPLEX STEREO DEMODULATOR
SILICON MONOLITHIC BIPOLAR INTEGRATED CIRCUIT

DESCRIPTION

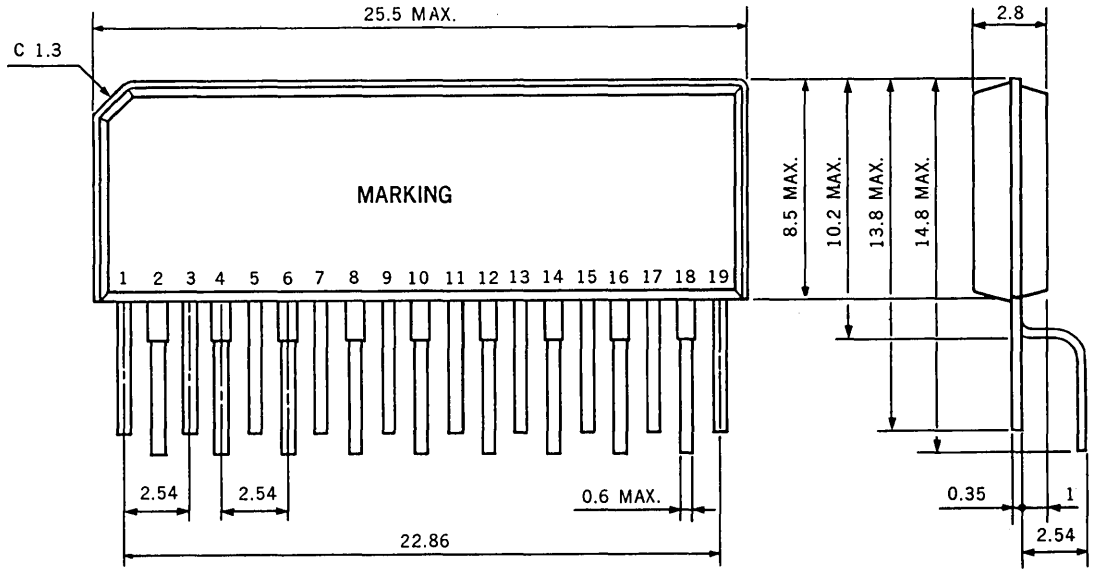
The μPC1227V is a silicon monolithic integrated circuit designed for FM multiplex stereo demodulator applications in FM stereo radio receivers using phase locked loop (PLL) techniques.

The device includes a variable blend facility that gives a smooth change from monaural to stereo reception. It also includes independent separation adjustment for L and R channels, forced monaural and VCO stop functions. Outline is a new developed 19-lead Vertical Dual In-Line Plastic Package (V-DIP), so that it is suitable for use in automotive radio receivers, where small mounting space is required.

FEATURES

- No coil necessary, all tuning performed with a single potentiometer.
- Automatic stereo/monaural switching.
- High Voltage gain: $A_V = -0.6$ dB ($R_L = 3.9$ kΩ)
- Easy to handle because of its V-DIP construction
- Reduction of the occupation of mounting area in P.C. Board and hand-insertion time, due to the external shape of the V-DIP.
- Free of mismounting due to its lead formation.
- Stereo noise reduction
- White Noise reduction
- Independent separation adjustment
- Wide supply voltage range: $V_{CC} = 6$ to 14 V

PACKAGE DIMENSIONS in millimeters



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Supply Voltage	V_{CC}	16	V
Package Dissipation (Ta = 75 °C)	P_D	430	mW
Lamp Driver Current (Pin 9)	I_L	75	mA
Operating Temperature	T_{opt}	−30 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

RECOMMENDED OPERATING CONDITIONS (Ta = 25 °C)

Operating Supply Voltage	V_{CC}	8	V
Supply Voltage Range	V_{CC}	6 to 14	V
Operating Ambient Temperature	Ta	−30 to +75	°C

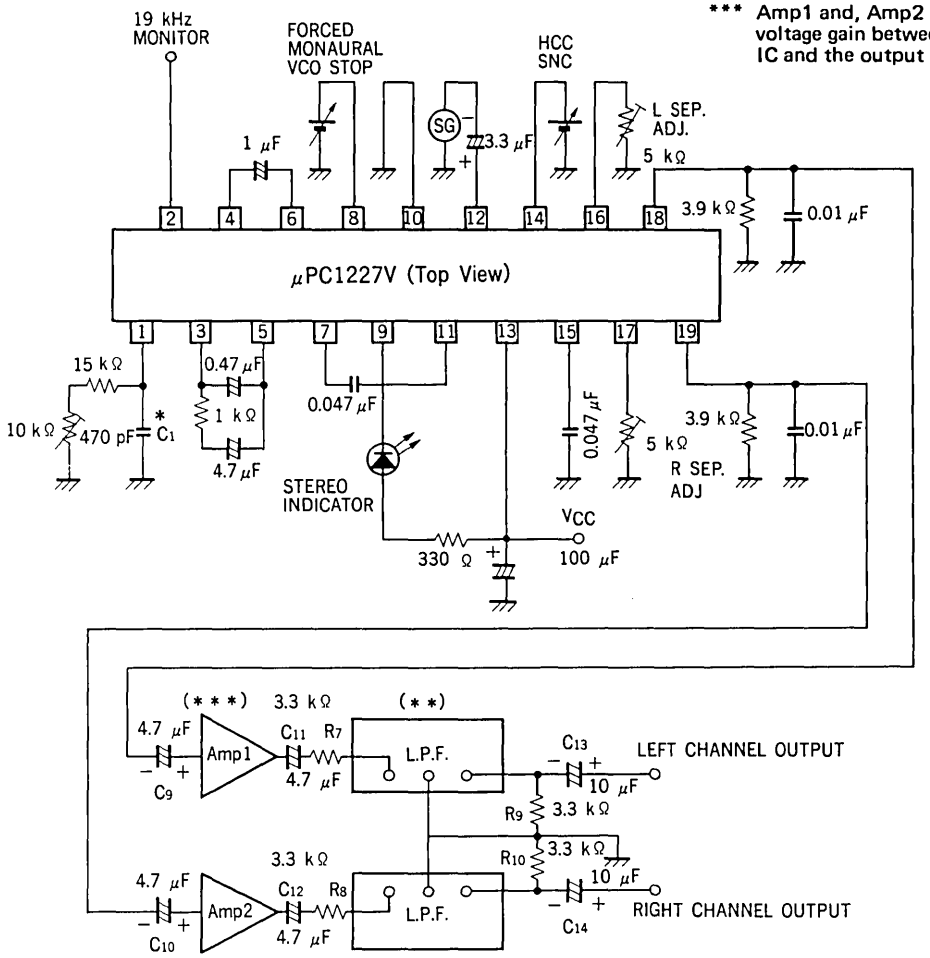
ELECTRICAL CHARACTERISTICS

[Ta = 25 °C, V_{CC} = 8 V, v_{in} = 300 mV $\left(\frac{\text{Pilot}}{\text{Composite}} = \frac{1}{10}\right)$, f = 1 kHz. R_L = 3.9 kΩ]

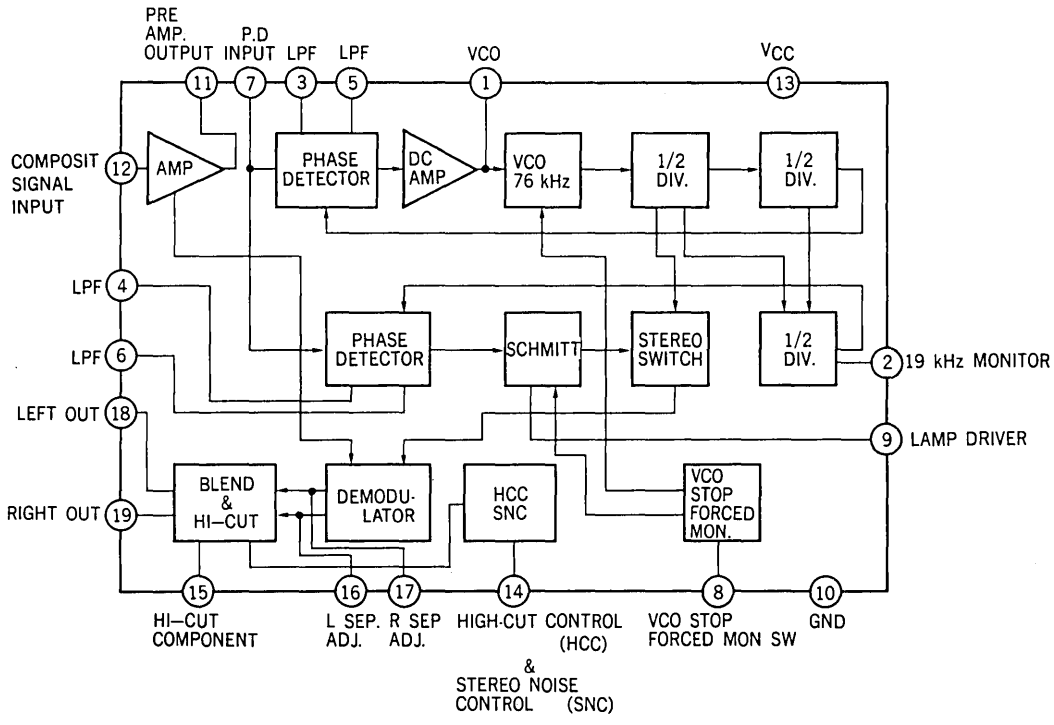
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	I_{CC}	12	20	28	mA	Quiescent
Input Impedance	Z_I		50		kΩ	
Stereo Channel Separation	Sep.	35	45		dB	f = 100 Hz, $v_{in\ (Pilot)}$ = 30 mV
		40	55		dB	f = 1 kHz, $v_{in\ (Pilot)}$ = 30 mV
		35	45		dB	f = 10 kHz, $v_{in\ (Pilot)}$ = 30 mV
Voltage Gain	A_v	−3.5	−0.6	+2.5	dB	Monaural input, $v_{in\ (L+R)}$ = 300 mV
Channel Balance	Ch.B.	−2	0	+2	dB	Monaural Input, $v_{in\ (L+R)}$ = 300 mV
	Ch.B.	−2	0	+2	dB	Stereo Input, $v_{in\ (Pilot)}$ = 30 mV
Total Harmonic Distortion	T.H.D.		0.05	0.3	%	Monaural Input, $v_{in\ (L+R)}$ = 300 mV
			0.05	0.3	%	Stereo Input, $v_{in\ (Pilot)}$ = 30 mV
Lamp Indicator Input Level	LAMP ON	4	8	12	mV	Pilot Level
Lamp Hysteresis			4		dB	Pilot Level
Capture Range	C.R.	±2	±4		%	$v_{in\ (Pilot)}$ = 30 mV
Ultrasonic Frequency Rejection	19 kHz Rej.		35		dB	19 kHz, $v_{in\ (Pilot)}$ = 30 mV
	38 kHz Rej.		45		dB	38 kHz, $v_{in\ (Pilot)}$ = 30 mV
SCA Rejection	SCA Rej.		70		dB	$\frac{\text{Pilot}}{\text{Composite}} = \frac{1}{10}$, $\frac{\text{SCA}}{\text{Composite}} = \frac{1}{10}$
Maximum Input Level	v_i	0.6	1.0		Vr.m.s.	Monaural Input, T.H.D. = 1 %
Signal-to-Noise Ratio	S/N	70	80		dB	Monaural Input, $v_{in\ (L+R)}$ = 300 mV
Forced Monaural Level	V_{mono}	0.8			V	#8 terminal
VCO Stop Level	V_{stop}	0.8			V	#8 terminal
Stereo Channel Separation	Sep. C1	0		3	dB	V_{14} = 0.4 V
	Sep. C2		17		dB	V_{14} = 1.0 V
	Sep. C3	40	55		dB	V_{14} = 1.6 V
Voltage Gain	A_{vH}	−23.5	−19	−15	dB	V_{14} = 0.4 V, f = 10 kHz

TEST CIRCUIT

* POLYSTYLENE CAPACITOR
** LOW PASS FILTER: BL – 13 (KORIN LAB.)
*** Amp1 and, Amp2 should be set so that, the voltage gain between the output terminal of the IC and the output terminal of the LPF is 0 dB

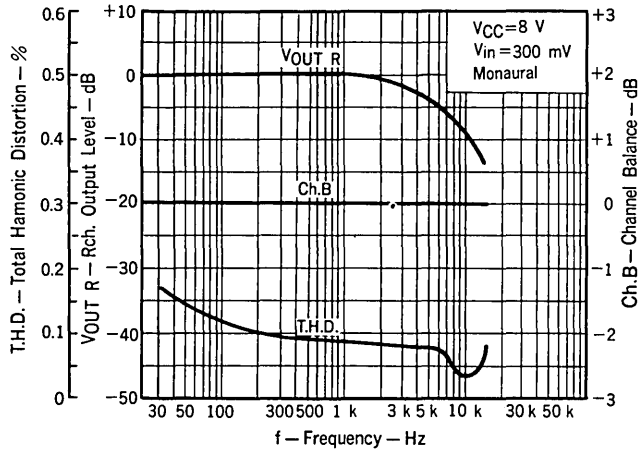


BLOCK DIAGRAM

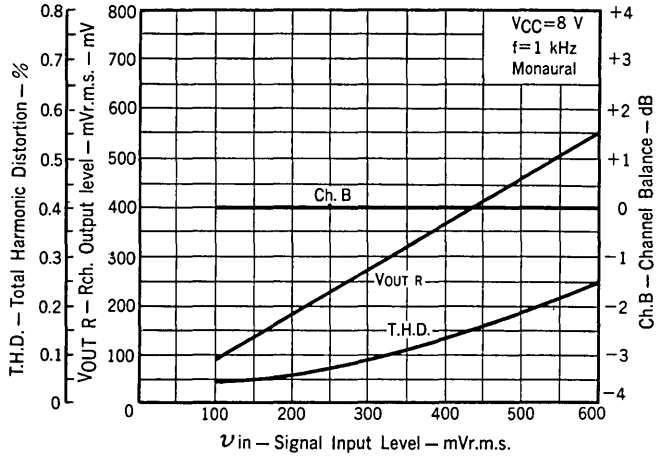


TYPICAL CHARACTERISTICS (Ta = 25 °C)

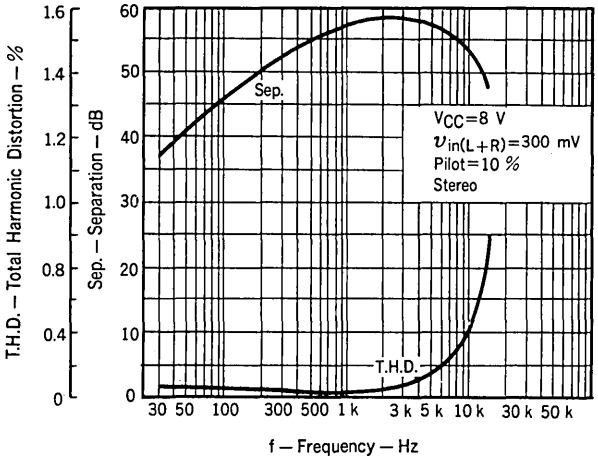
Rch. OUTPUT LEVEL, TOTAL HARMONIC DISTORTION, CHANNEL BALANCE vs. FREQUENCY



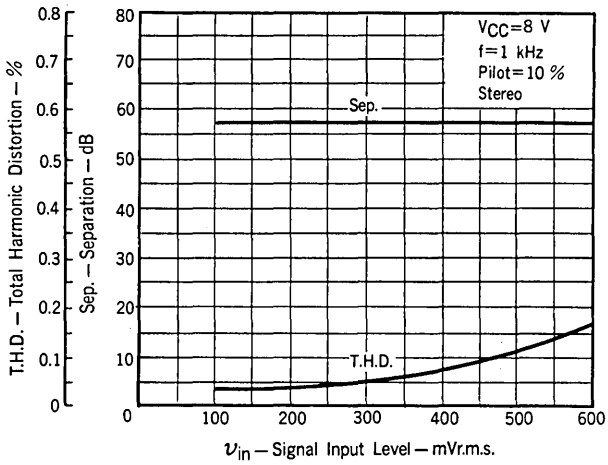
TOTAL HARMONIC DISTORTION, Rch. OUTPUT LEVEL, CHANNEL BALANCE vs. SIGNAL INPUT LEVEL



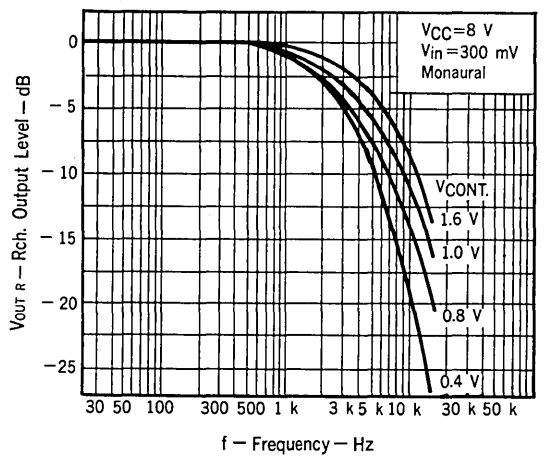
TOTAL HARMONIC DISTORITION, SEPARATION vs. FREQUENCY



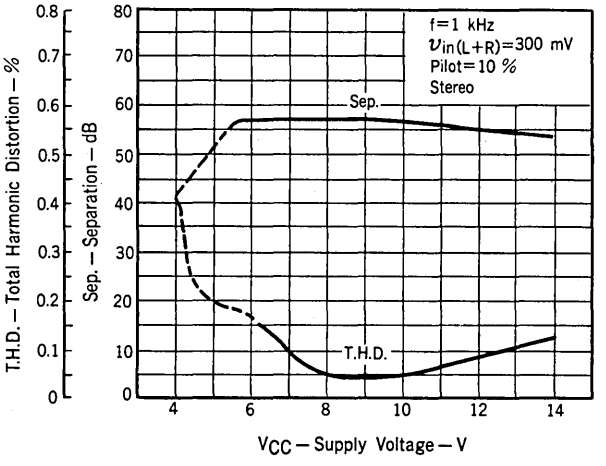
TOTAL HARMONIC DISTORTION, SEPARATION vs. SIGNAL INPUT LEVEL



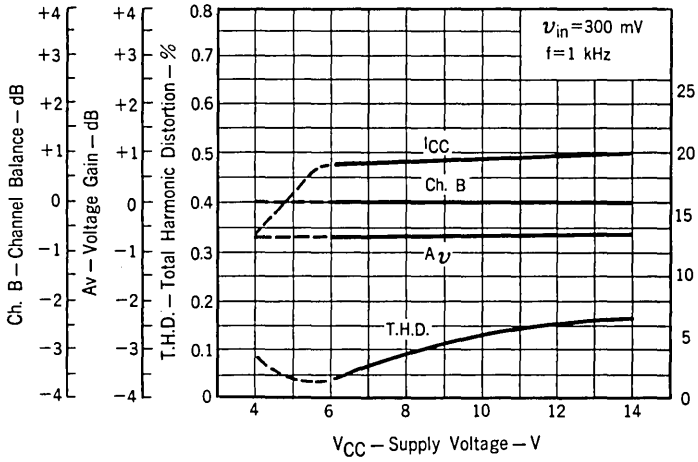
Rch. OUTPUT LEVEL vs. FREQUENCY



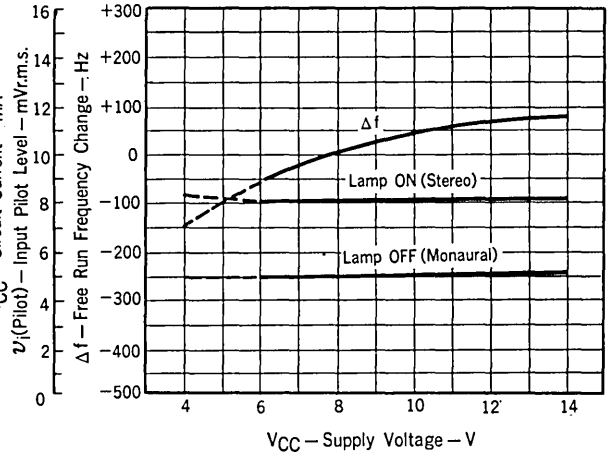
TOTAL HARMONIC DISTORTION, SEPARATION vs. SUPPLY VOLTAGE



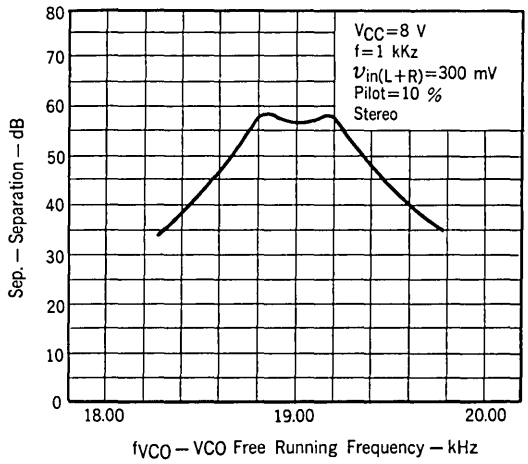
CHANNEL BALANCE, VOLTAGE GAIN, TOTAL HARMONIC DISTORTION, CIRCUIT CURRENT vs. SUPPLY VOLTAGE



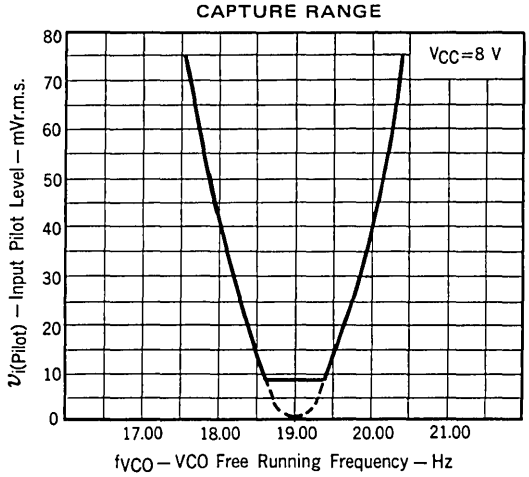
INPUT PILOT LEVEL, FREE RUN FREQUENCY CHANGE vs. SUPPLY VOLTAGE



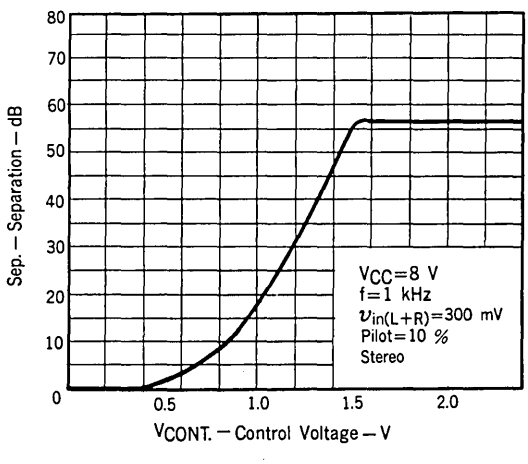
SEPARATION vs. VCO FREE RUNNING FREQUENCY



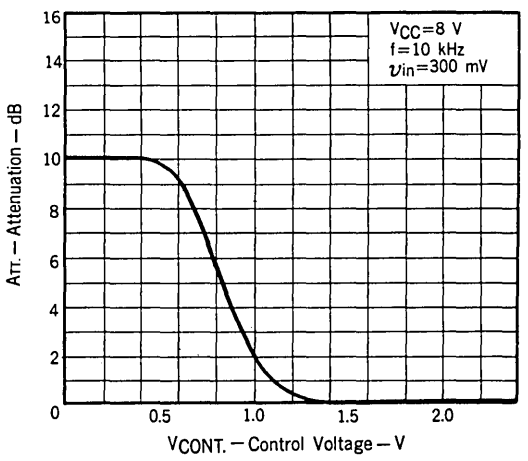
CAPTURE RANGE



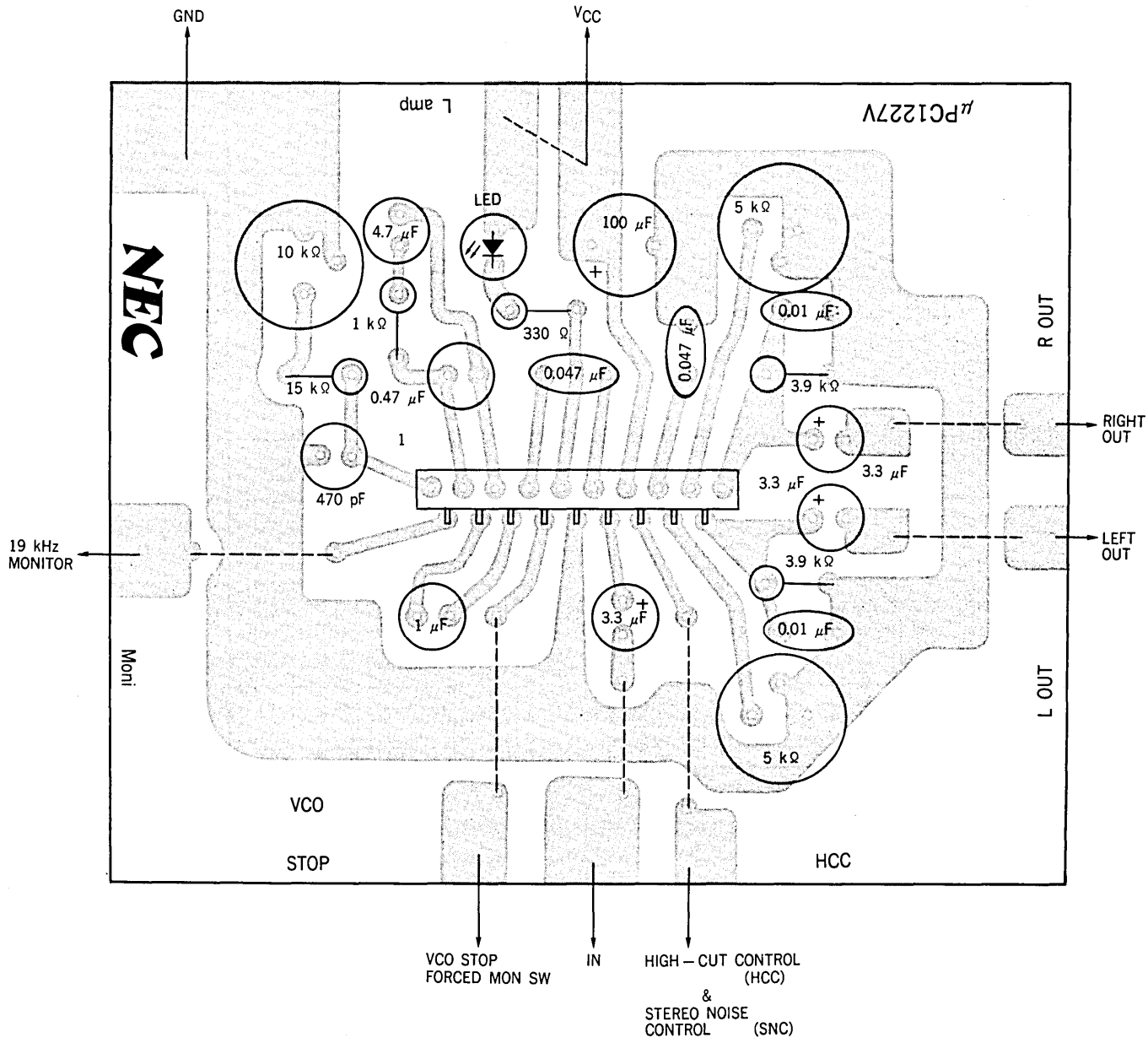
SEPARATION vs. CONTROL VOLTAGE (SNC)



ATTENUATION vs. CONTROL VOLTAGE (HCC)



COMPONENTS LAYOUT FOR P.C. ASSEMBLY (Copper side)



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1320C

FM MULTIPLEX STEREO DEMODULATOR
SILICON MONOLITHIC BIPOLAR INTEGRATED CIRCUIT

DESCRIPTION

The μPC1320C is FM stereo demodulator with utilize phase locked loop technology.

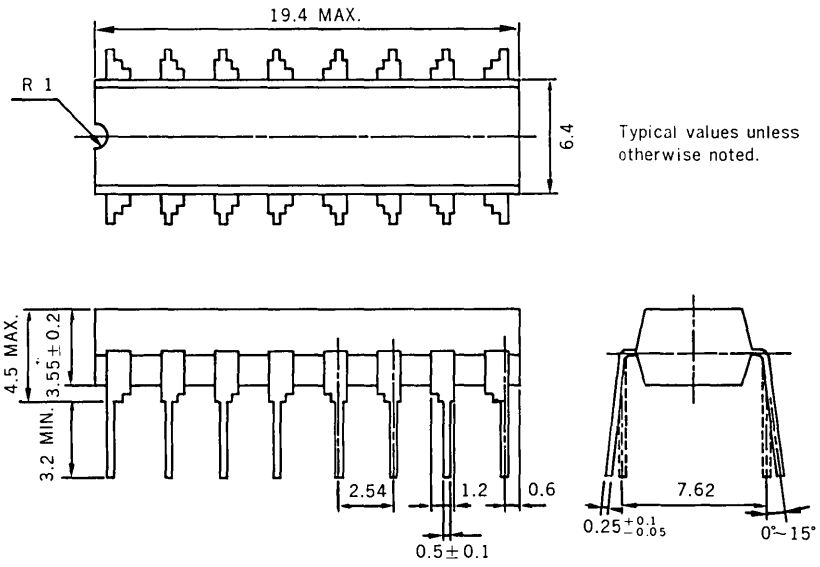
The device features excellent channel separation over a wide band of frequencies and a wide range of operating voltage with low distortion.

It contains an automatic stereo-monaural switching circuit, a VCO mute circuit for FM/AM radio application, a forced monaural switching circuit and stereo indicator lamp driver.

FEATURES

- Less external part; No coil
- Wide operating voltage range; V_{CC} = 5.4 to 14 V
- Wide dynamic range; V_{in} = 1 000 mVr.m.s. TYP.
- Excellent channel separation maintained over wide frequency range (fixed or adjustable).
- High voltage gain; A_V = –0.8 dB
- Containing an automatic stereo-monaural switching circuit, a forced monaural switching circuit and a VCO mute circuit for FM/AM radio application.

PACKAGE DEMENSIONS (Unit: mm)



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Supply Voltage	V_{CC}	14	V
Lamp Voltage (Pin 6)	V_{LAMP}	18	V
Package Dissipation (Ta = 75 °C)	P_D	350	mW
Lamp Driver Current (Pin 6)	I_L	75	mA
Operating Temperature	T_{opt}	−30 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

RECOMMENDED OPERATING CONDITIONS (Ta = 25 °C)

Operating Supply Voltage	V_{CC}	8	V
Supply Voltage Range		5.4 to 14	V
Operating Ambient Temperature	Ta	−30 to +75	°C

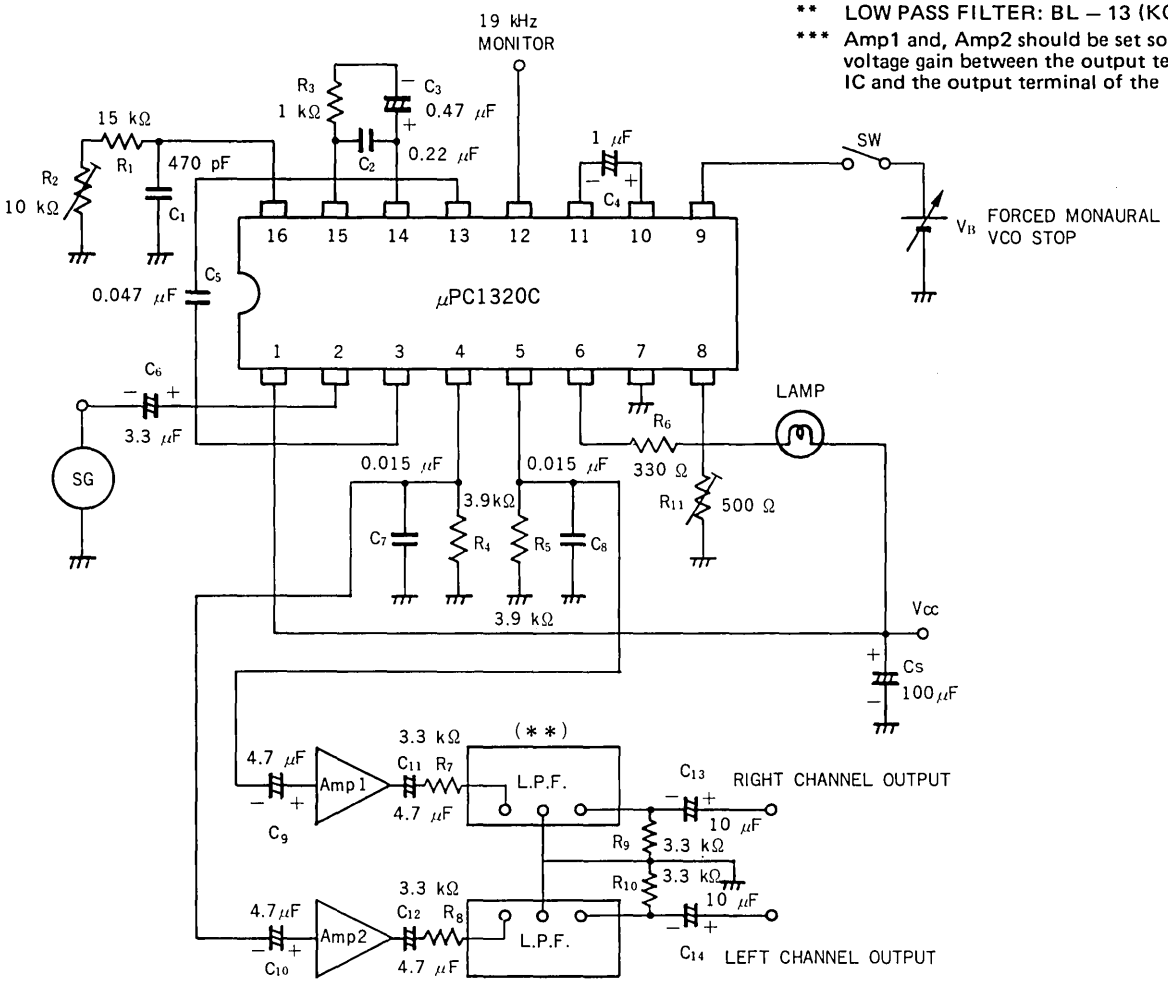
ELECTRICAL CHARACTERISTICS

(Ta = 25 °C, V_{CC} = 8 V, v_{in} = 350 mV ($\frac{Pilot}{Composite} = \frac{1}{10}$), f = 1 kHz, R_L = 3.9 kΩ)

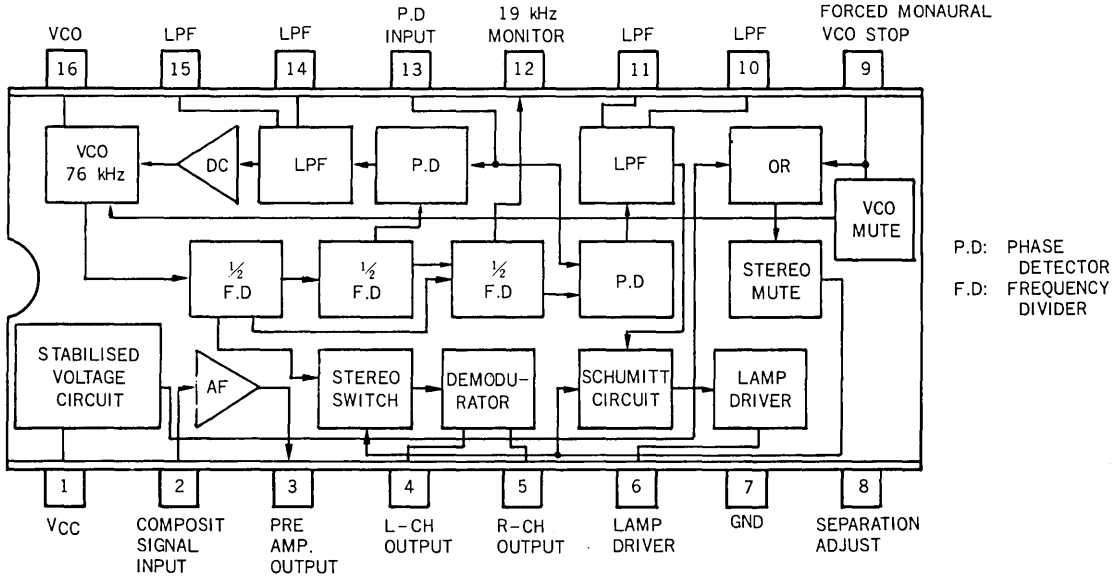
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	I_{CC}	8	12	18	mA	Quiescent
Input Impedance	Z_i		50		kΩ	
Stereo Channel Separation	$S_{ep.}$		45		dB	f = 100 Hz, $v_{in\ (Pilot)}$ = 35 mV
		40	55		dB	f = 1 kHz, $v_{in\ (Pilot)}$ = 35 mV
			45		dB	f = 10 kHz, $v_{in\ (Pilot)}$ = 35 mV
Output Voltage	V_O	250	320	430	dB	Monaural Input, $v_{in\ (L+R)}$ = 350 mV
Channel Balance	Ch.B.	−2	0	+2	dB	Monaural Input, $v_{in\ (L+R)}$ = 350 mV
	Ch.B.	−2	0	+2	dB	Stereo Input, $v_{in\ (Pilot)}$ = 35 mV
Total Harmonic Distortion	T.H.D.		0.1	0.5	%	Monaural Input, $v_{in\ (L+R)}$ = 350 mV
			0.1	0.5	%	Stereo Input, $v_{in\ (Pilot)}$ = 35 mV
Lamp Indicator Input Level	LAMP ON	4	8	12	mV	Pilot Level
Lamp Hysteresis			4		dB	Pilot Level
Capture Range	C.R.	±2	±5		%	$v_{in\ (Pilot)}$ = 35 mV
Ultrasonic Frequency Rejection	19 kHz Rej.		35		dB	19 kHz, $v_{in\ (Pilot)}$ = 35 mV
	38 kHz Rej.		45		dB	38 kHz, $v_{in\ (Pilot)}$ = 35 mV
SCA Rejection	SCA Rej.		70		dB	$\frac{Pilot}{Composite} = \frac{1}{10}$, $\frac{SCA}{Composite} = \frac{1}{10}$
Maximum Input Level	v_i	0.6	1.0		Vr.m.s.	Monaural Input, T.H.D. = 1 %
Signal-to-Noise Ratio	S/N		83		dB	V_i = 350 mV
Forced Monaural Level	V mono	0.8			V	
VCO Stop Level	V stop	0.8			V	

TEST CIRCUIT

* POLYSTYLENE CAPACITOR
** LOW PASS FILTER: BL – 13 (KORIN LAB.)
*** Amp1 and, Amp2 should be set so that, the voltage gain between the output terminal of the IC and the output terminal of the LPF is 0 dB

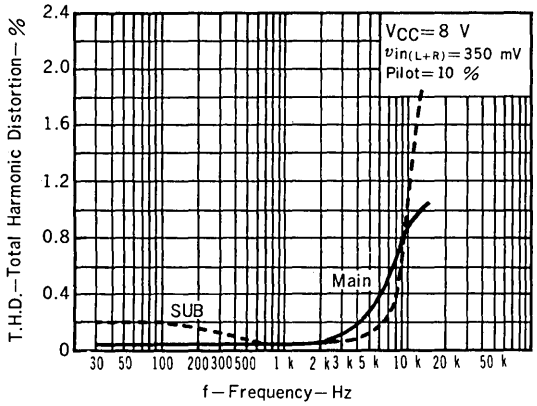


BLOCK DIAGRAM

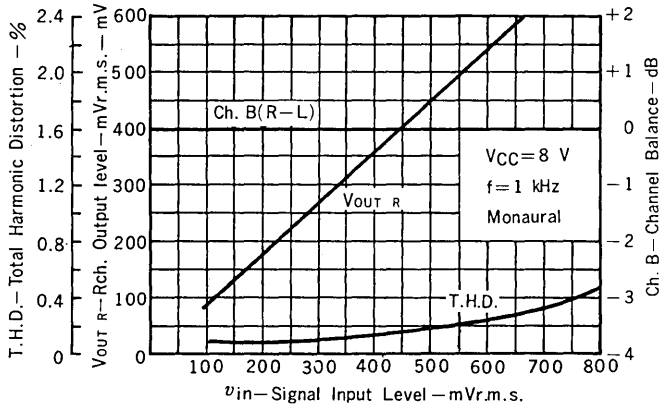


TYPICAL CHARACTERISTICS (Ta = 25 °C)

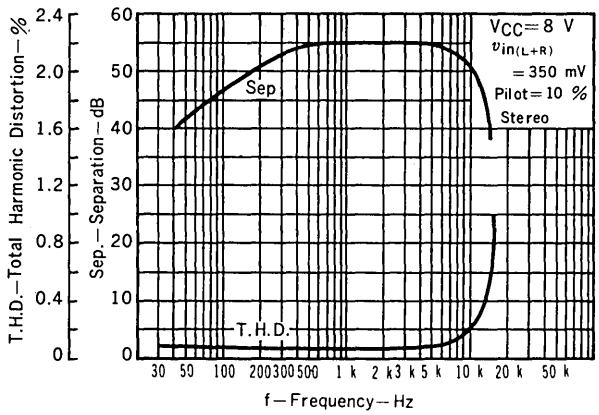
TOTAL HARMONIC DISTORTION vs. FREQUENCY



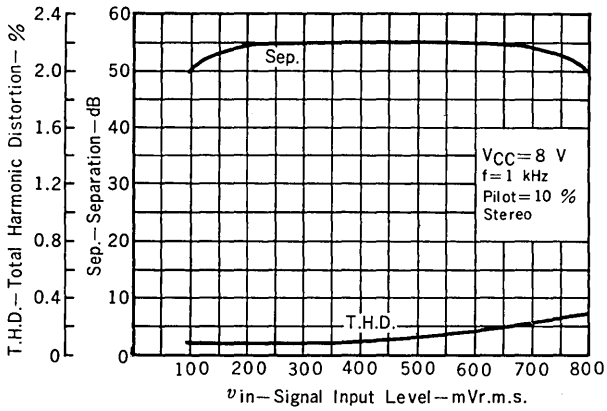
TOTAL HARMONIC DISTORTION, Rch. OUTPUT LEVEL, CHANNEL BALANCE vs. SIGNAL INPUT LEVEL



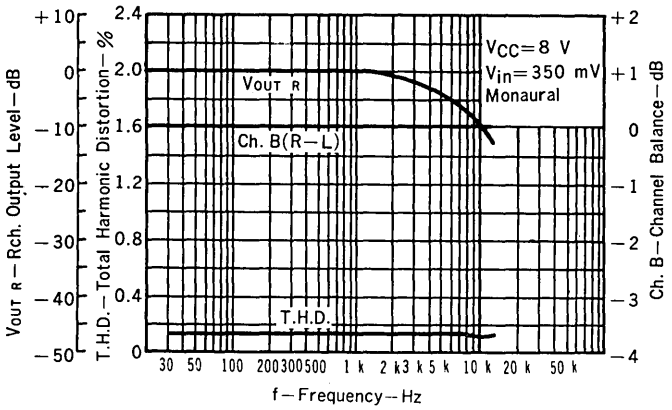
TOTAL HARMONIC DISTORTION, SEPARATION vs. FREQUENCY



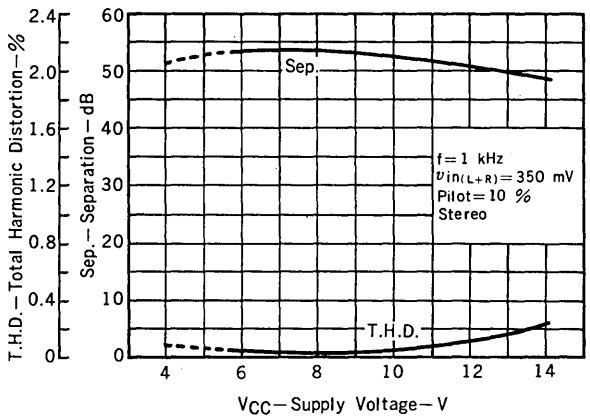
TOTAL HARMONIC DISTORTION, SEPARATION vs. SIGNAL INPUT LEVEL



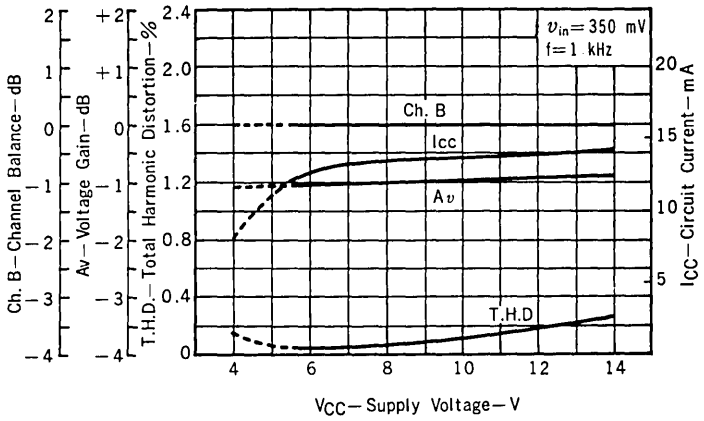
Rch. OUTPUT LEVEL, TOTAL HARMONIC DISTORTION, CHANNEL BALANCE vs. FREQUENCY



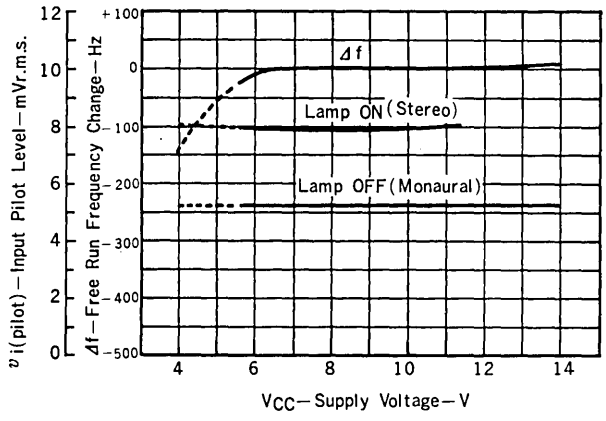
TOTAL HARMONIC DISTORTION, SEPARATION vs. SUPPLY VOLTAGE



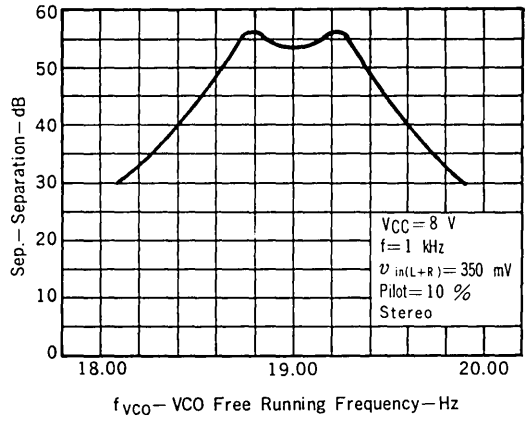
CHANNEL BALANCE, VOLTAGE GAIN, TOTAL HARMONIC DISTORTION, CIRCUIT CURRENT vs. SUPPLY VOLTAGE



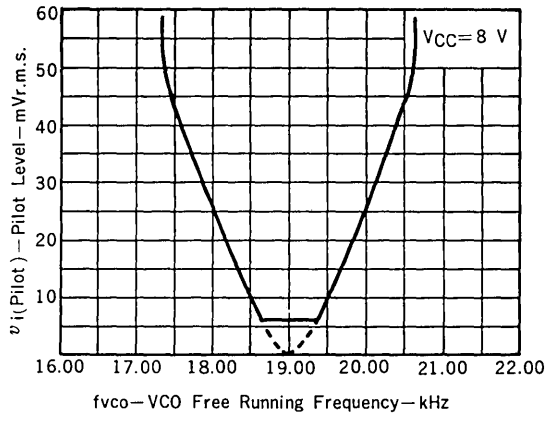
INPUT PILOT LEVEL, FREE RUN FREQUENCY CHANGE vs. SUPPLY VOLTAGE



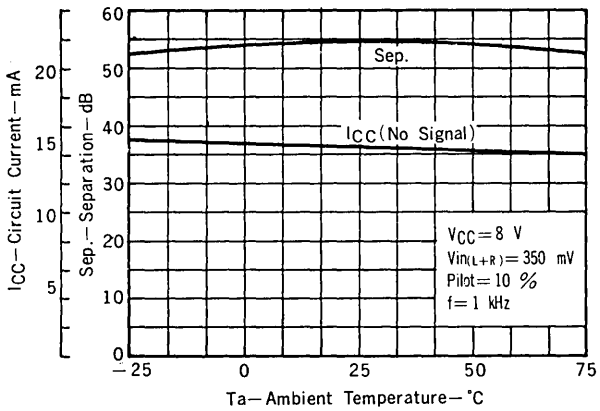
SEPARATION vs. VCO FREE RUNNING FREQUENCY



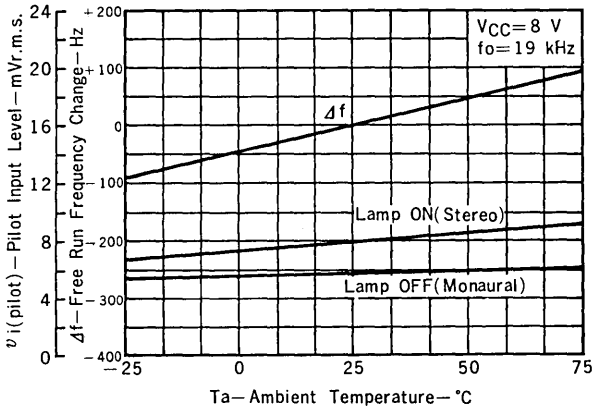
CAPTURE RANGE



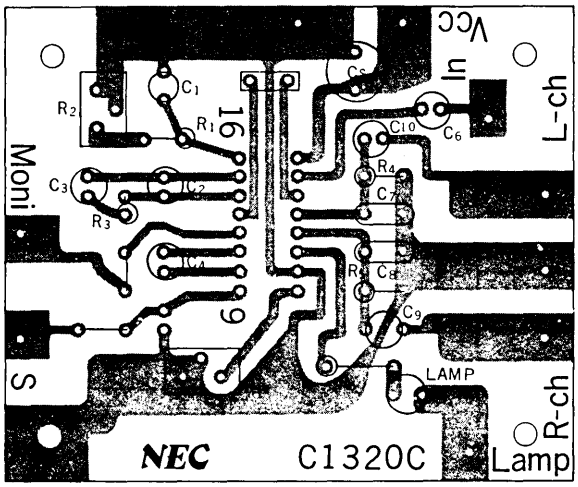
CIRCUIT CURRENT, SEPARATION vs. AMBIENT TEMPERATURE



PILOT INPUT LEVEL, FREE RUN FREQUENCY CHANGE vs. AMBIENT TEMPERATURE



Components Layout for P.C. Assembly (Copper side)

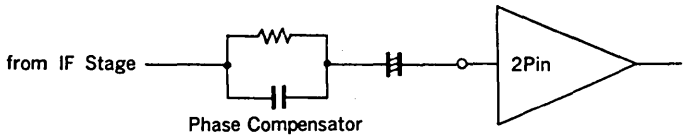


Application Information

1. Separation Adjustment

   Separation control is normally adjusted by a variable resistor connected to Pin 15.

   A phase compensator, however, is recommended to use as show below when the variable resistor is not enough to provide typical separation due to large IF phase delay.



2. Stereo-Monaural Switching

   Applying voltage higher than 0.8 V to Pin 9 make μPC1320C switch from stereo to monaural condition. The monaural switching is also performed by keeping Pin. 11 grounded. (stereo operation is kept by Pin. 10 grounded.)

BIPOLAR ANALOG INTEGRATED CIRCUIT
μPC1176C

FM NOISE CANCELLER
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

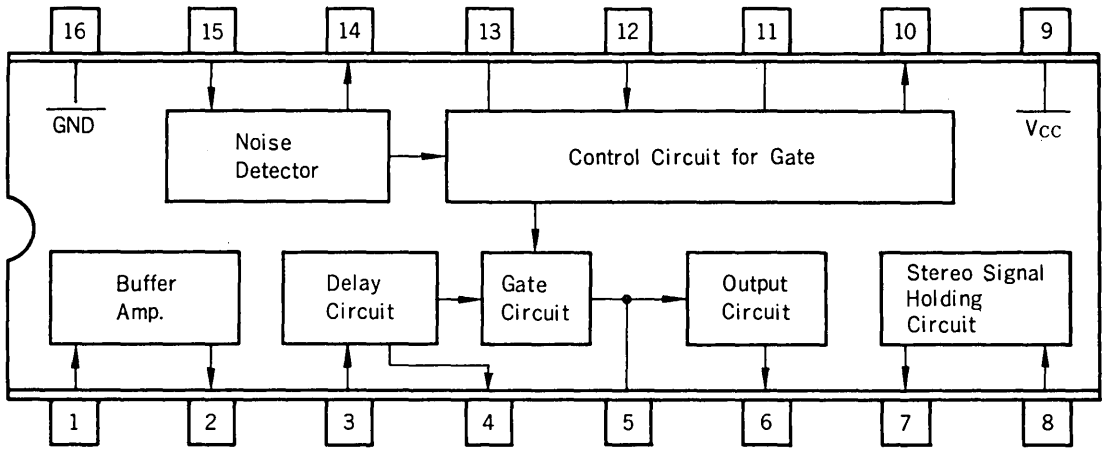
DESCRIPTION

μPC1176C, a monolithic integrated circuit, is an FM Noise Canceller for use in automotive radio receivers. The incoming noise such as that from car ignition can be suppressed. Internally, buffer-amplifier, delay circuit, gate circuit, noise detector, control circuit for gate and stereo signal holding circuit are included.

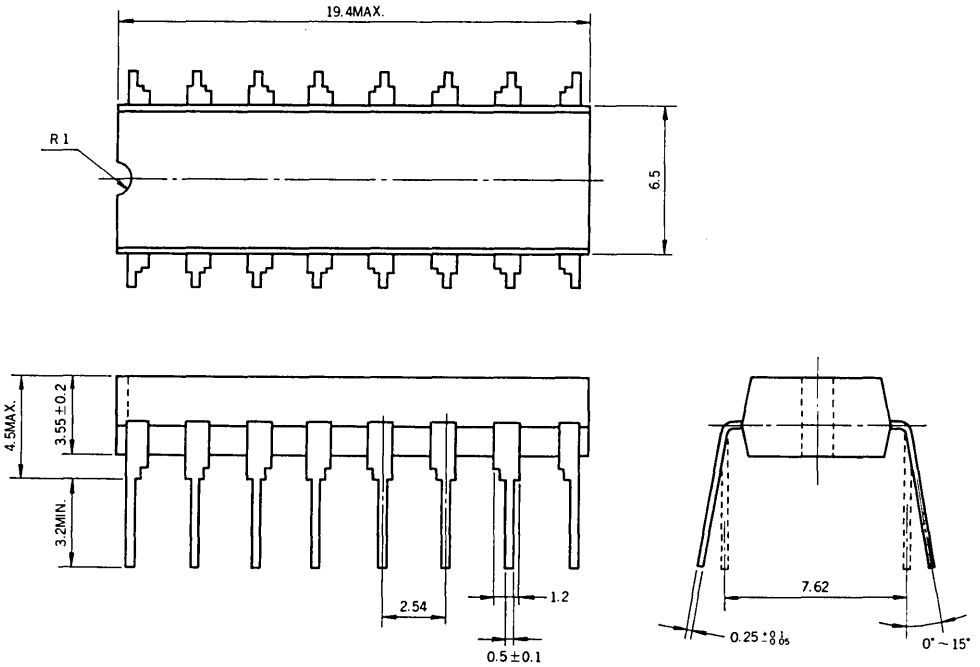
FEATURES

- Effective pulsive noise suppression.
- Minimum distortion level due to the stereo signal holding circuit.
- Automatic change of the blanking time, according to noise intensity.
- Excellent response for highly repetitive noise.

BLOCK DIAGRAM (Top View)



PACKAGE DIMENSIONS (in millimeters)



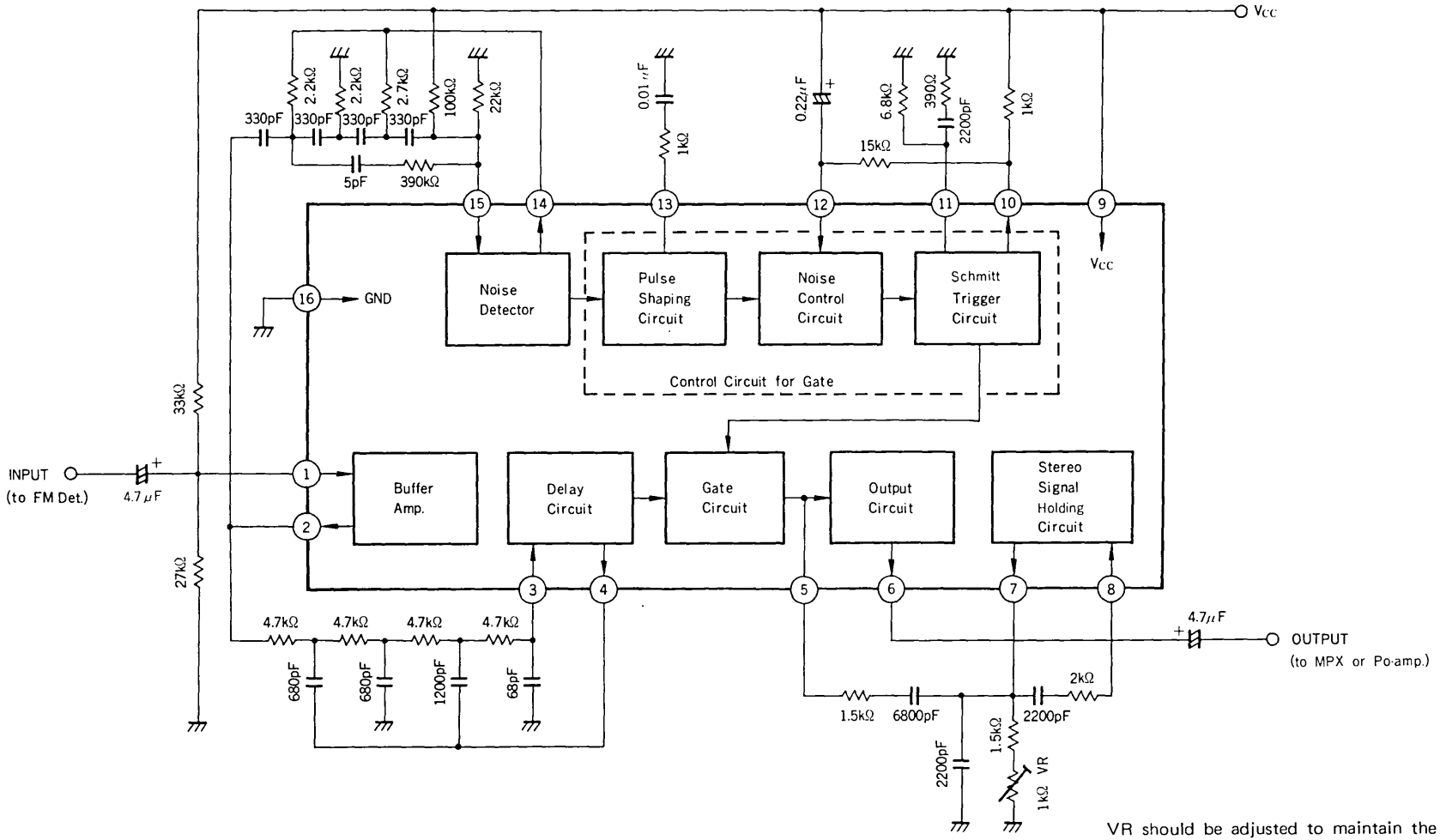
ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Supply Voltage	V_{CC}	15	V
Package Dissipation	PD	350*	mW
Operating Temperature	T_{opt}	-20 to +75	°C
Storage Temperature	T_{stg}	-40 to +125	°C
		*Ta = 75°C	

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{CC} = 10V)

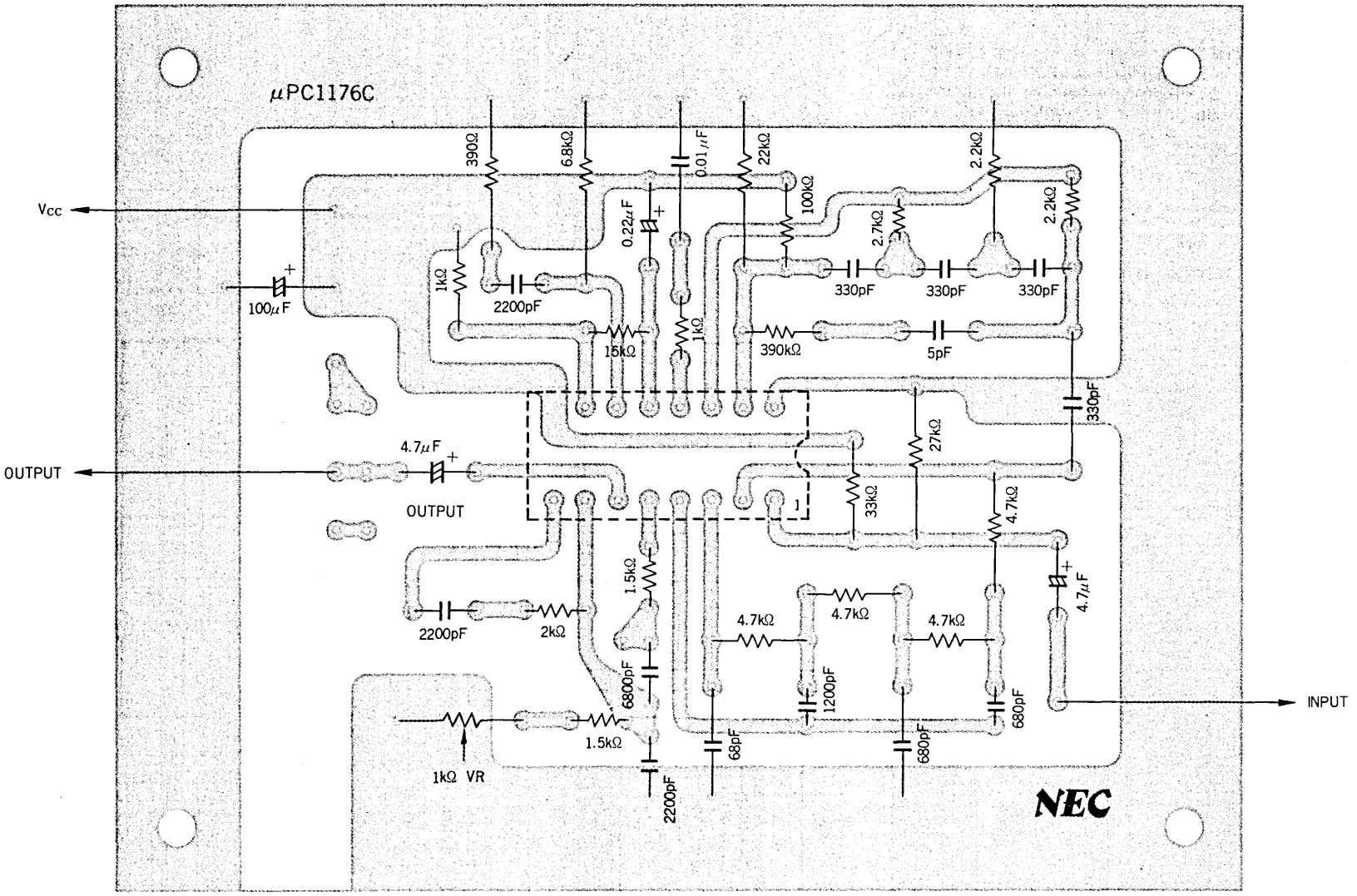
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	I_{CC}	13	16.5	23	mA	v_i = 0
Voltage Gain	A_v	-0.3	0.7	1.7	dB	v_i = 500mVr.m.s., f = 1kHz
Blanking Time	T_B		30		μs	v_i = 500mVp, f = 1kHz, tw = 1μs
Triggering Voltage	V_T		40		mVp	f = 1kHz, tw = 10μs

TYPICAL APPLICATION CIRCUIT



VR should be adjusted to maintain the amplitude and frequency of the 38 kHz signal when the gate circuit is turned off.

Diagram of Components Mounted on a Printed-Circuit Board (Bottom View)



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1032H

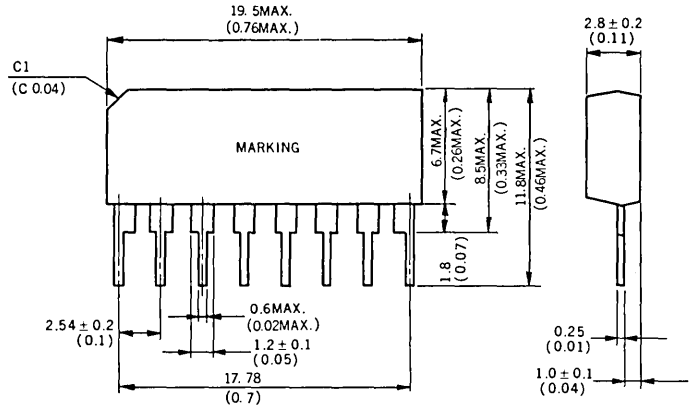
DUAL LOW NOISE PREAMPLIFIER
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

DESCRIPTION

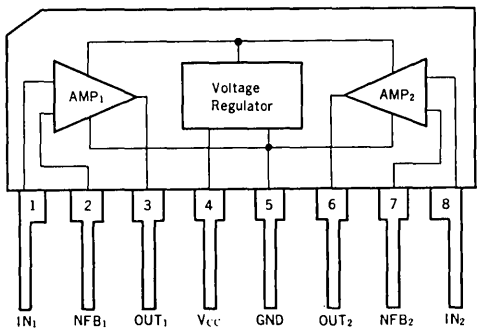
The μPC1032H is a silicon monolithic integrated circuit designed for use as a 2 channel preamplifier for a car stereo set. The device has features of low noise, high gain, high output voltage and wide supply voltage range.
Especially, as an advanced production process is used, the device has an excellent feature of very low pulsive noise.
An internal voltage regulator circuit permits the μPC1032H to operate satisfactorily over wide variation of supply voltage.

PACKAGE DIMENSIONS

in millimeters (inches)



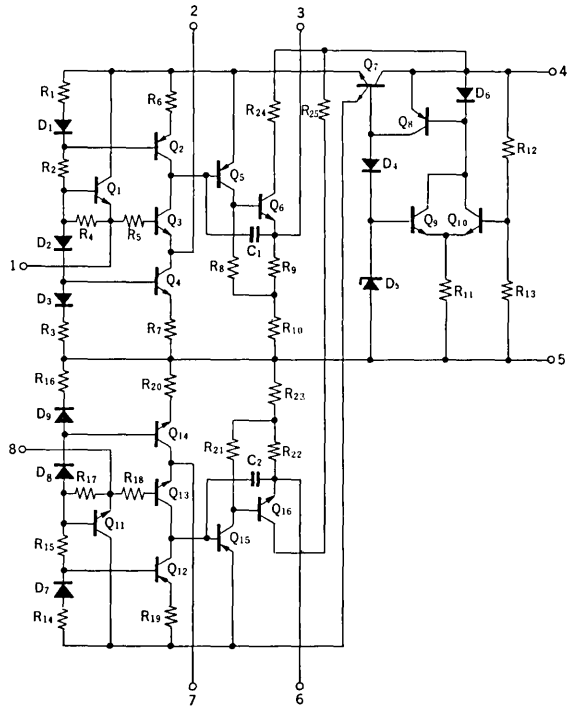
CONNECTION DIAGRAM



FEATURES

- Two channel
- Wide supply voltage range
- Minimum number of external parts required
- Low noise, especially low pulsive noise
- SIP assures easy mounting on printed circuit board.

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Supply Voltage	V_{CC}	18	V
Package Dissipation	P_D	270*	mW
Operating Temperature	T_{opt}	-20 to +75	°C
Storage Temperature	T_{stg}	-40 to +125	°C
		*Ta = 75°C	

RECOMMENDED CONDITIONS (Ta = 25°C)

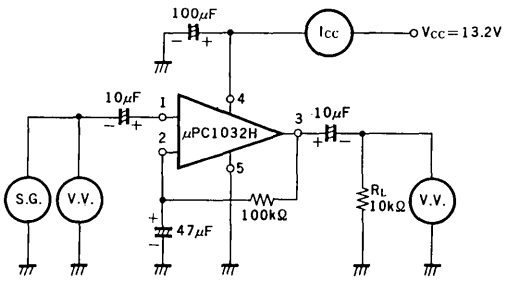
Operating Supply Voltage	V_{CC}	13.2	V
Supply Voltage Range	V_{CC}	8 to 17	V
Operating Ambient Temperature		-20 to +75	°C
Load impedance		10 kΩ TYP.	

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{CC} = 13.2V, f = 1 kHz, R_L = 10 kΩ)

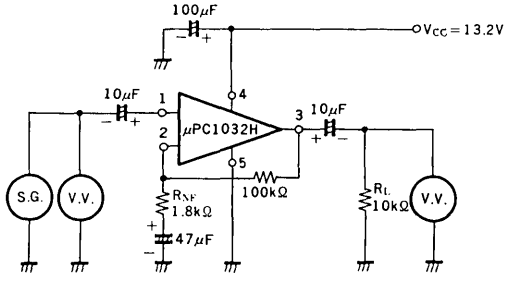
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CIRCUIT	TEST CONDITIONS
Circuit Current	I_{CC}		7	11.0	mA	①	v_{in} = 0
Open Loop Voltage Gain	A_{vo}	70	81		dB	①	v_o = 0.3V
Voltage Gain	A_v	33.5	35	35.5	dB	②	v_o = 0.3V, R_{NF} = 1.8 kΩ
Maximum Output Voltage	V_{OM}	1.1	1.7		V	③	T.H.D. = 1%, NAB ≒ 35 dB
Total Harmonic Distortion	T.H.D.		0.1	0.3	%	③	v_o = 0.3V, NAB ≒ 35dB
Input Impedance	r_i	50	100		kΩ	③	
Equivalent Input Noise Voltage	v_{nin}		1.4	2.0	μVr.m.s.	④	R_G = 2.2kΩ, NAB ≒ 35dB
Cross Talk			-62		dB	⑤	v_o = 1V, (The other channel v_{in} = 0, R_G = 2.2kΩ)
Channel Balance		-0.3	0	+0.3	dB	⑤	v_o = 0.3V

TEST CIRCUITS

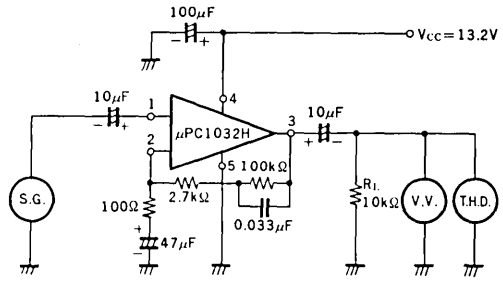
① I_{CC}, A_{vo} Test Circuit



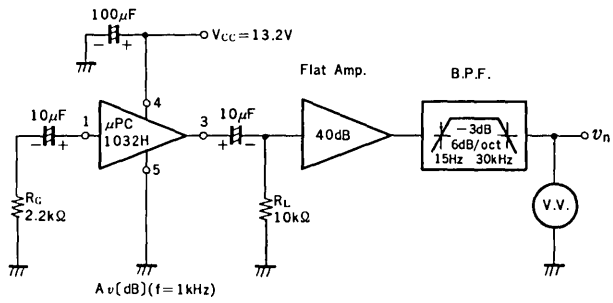
② A_v Test Circuit (for Ch. 1)



③ V_{OM}, T.H.D., r_i Test Circuit
(for Ch. 1)

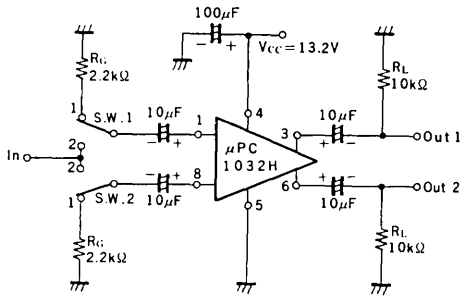


④ v_{nin} Test Circuit
(for Ch. 1)



v_{nin} is calculated by v_n and amp. gain (A_v +40 dB).
External components of the IC are the same as the Test Circuit ③.

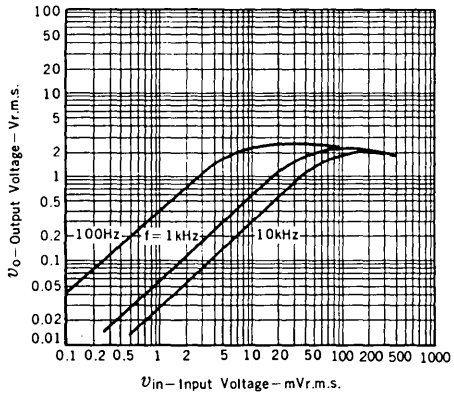
⑤ Cross Talk, Channel Balance Test Circuit



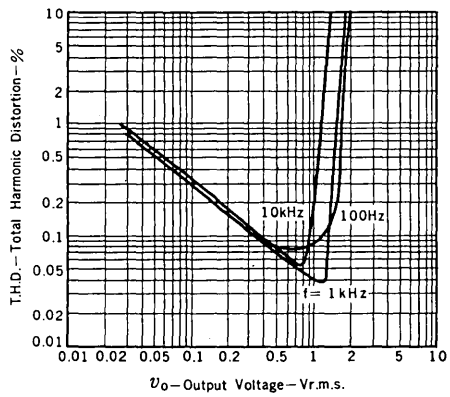
External Components of the IC are the same as the Test Circuit ③
Cross talk Test Procedure
20 log Out_2/Out_1
Switch Position $SW_1 \rightarrow 2$, $SW_2 \rightarrow 1$
20 log Out_1/Out_2
Switch Position $SW_1 \rightarrow 1$, $SW_2 \rightarrow 2$
Channel Balance Test Procedure
20 log Out_1/Out_2
Switch Position $SW_1 \rightarrow 2$, $SW_2 \rightarrow 2$

TYPICAL CHARACTERISTICS (Ta = 25°C)

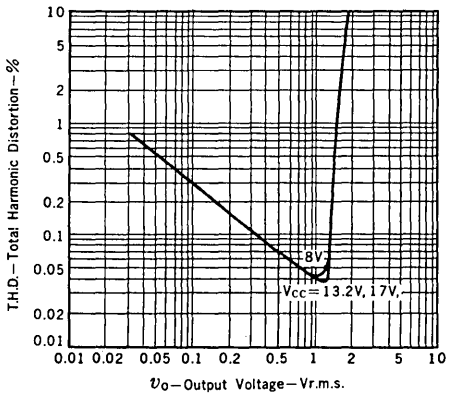
OUTPUT VOLTAGE vs.
INPUT VOLTAGE
(Test Circuit ③)



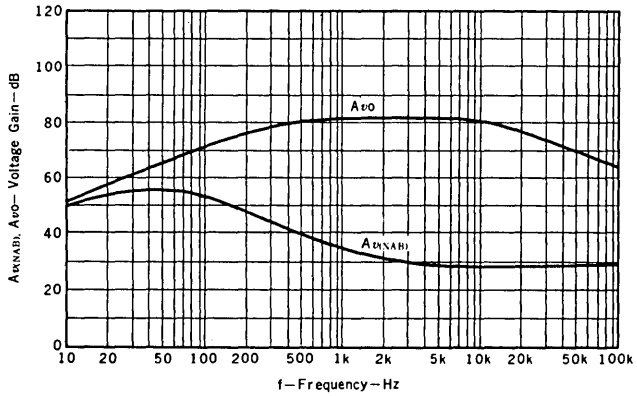
TOTAL HARMONIC DISTORTION vs.
OUTPUT VOLTAGE
(Test Circuit ③)



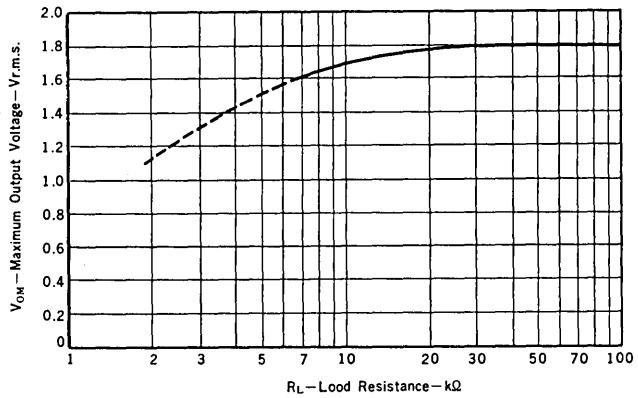
TOTAL HARMONIC DISTORTION vs. OUTPUT VOLTAGE
(Test Circuit③)



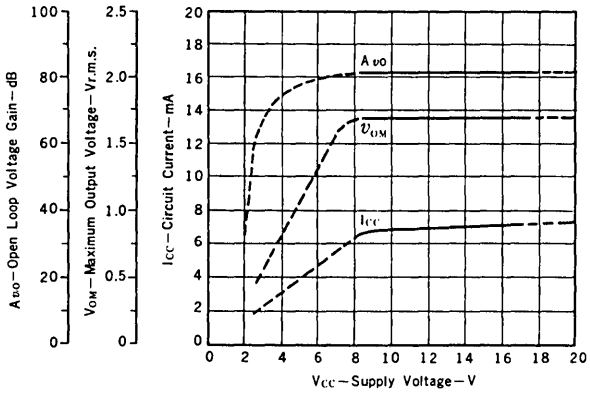
VOLTAGE GAIN vs. FREQUENCY
(Test Circuit①, ③)



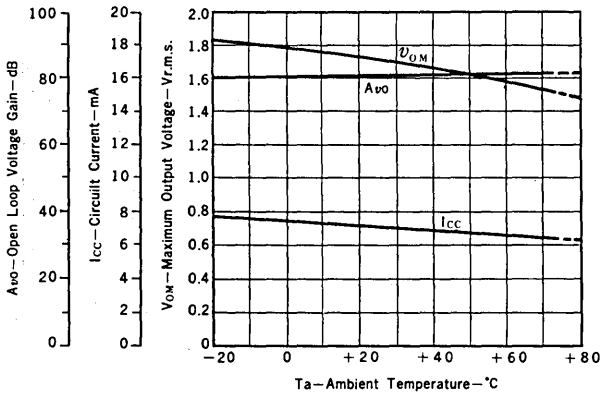
MAXIMUM OUTPUT VOLTAGE vs. LOAD RESISTANCE
(Test Circuit③)



CIRCUIT CURRENT, MAXIMUM OUTPUT VOLTAGE, OPEN LOOP VOLTAGE GAIN vs. SUPPLY VOLTAGE
(Test Circuit①, ③)

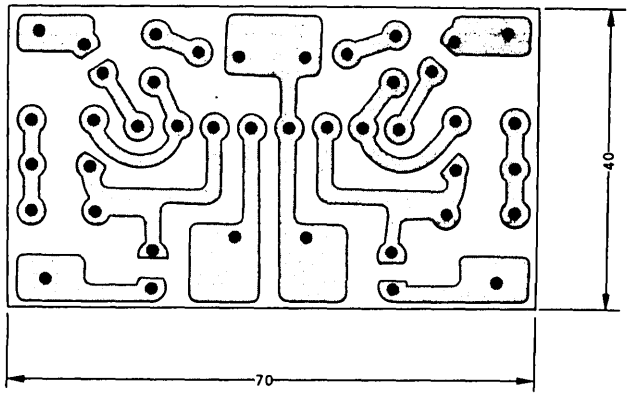


CIRCUIT CURRENT, MAXIMUM OUTPUT VOLTAGE, OPEN LOOP VOLTAGE GAIN AMBIENT TEMPERATURE
(Test Circuit①, ③)



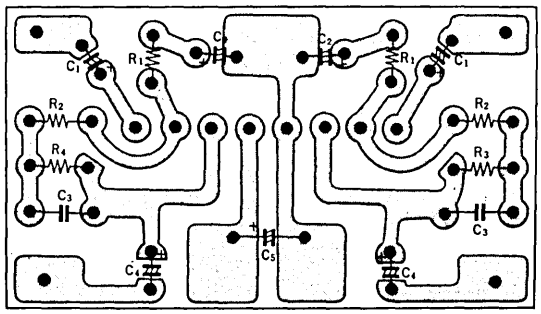
TYPICAL PRINTED CIRCUIT BOARD PATTERN

Bottom View (Unit : millimeters)

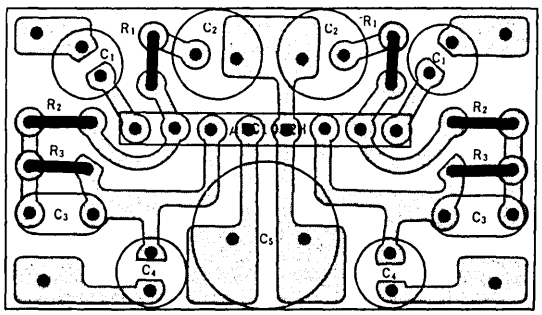


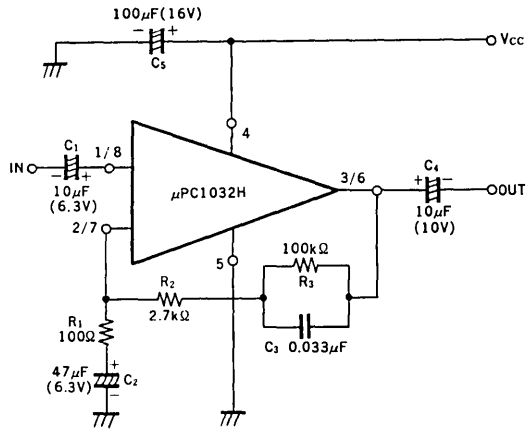
Components Layout

Foil Side



Components Side





BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1228H

LOW NOISE DUAL PREAMPLIFIER
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

DESCRIPTION

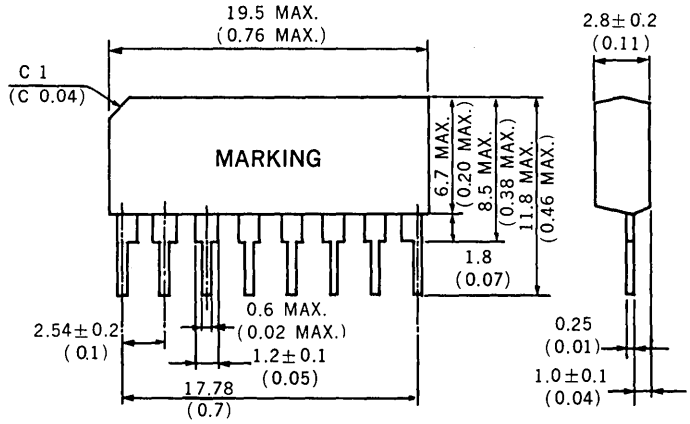
The μPC1228H, a silicon monolithic integrated circuit, is a low noise dual preamplifier designed for car stereo applications. The device consists of two separate amplification channels, and its major features are low noise, low distortion, high gain, large dynamic range and wide supply voltage range.

Outline is a 8-lead single in-line plastic package, for small mounting space and easy mounting on P. C. Board.

FEATURES

- High open loop gain : A_{VO} = 100 dB TYP.
- Low noise : V_{nin} = 1.1 μV TYP.
- Low distortion : T.H.D. = 0.05 % TYP.
- Large dynamic range : V_{OM} = 2.0 Vr.m.s. TYP.
- Wide supply voltage range : V_{CC} = 6 to 16 V
- High output current : I_{ODC} = 1 mA MAX.
- Low impedance load driving capability : R_L = 1 kΩ MIN.
- Small feedback capacitance capability

PACKAGE DIMENSIONS in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Supply Voltage	V_{CC}	18	V
Package Dissipation	P_D	270*	mW
Operating Temperature	T_{opt}	−30 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

* Ta=75 °C

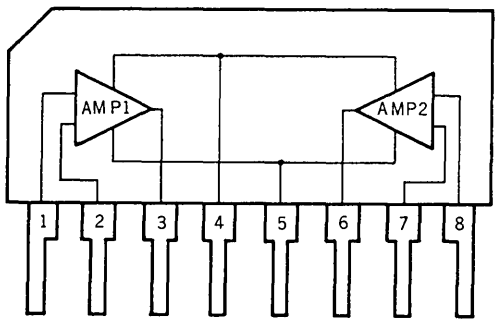
RECOMMENDED CONDITIONS (Ta = 25 °C)

Operating Supply Voltage	Vcc	13.2	V
Supply Voltage Range	V_{CC}	6 to 16	V
Operating Ambient Tamperature	T_a	−30 to +75	°C
Load impedance	R_L	10 kΩ TYP.	

ELECTRICAL CHARACTERISTICS (Ta = 25 °C, V_{CC} = 10 V, f = 1 kHz, R_L = 10 kΩ)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CIRCUIT	TEST CONDITIONS
Quiescent Current	I_{CC}	2.5	3.3	4.8	mA	(1)	v_{in} = 0
Open Loop Voltage Gain	A_{vO}	90	100		dB	(1)	v_O = 0.3 V, f = 100 Hz
Voltage Gain	A_v		40		dB	(2)	v_O = 0.3 V, NAB
Maximum Output Voltage	v_{OM}	1.0	2.0		V	(2)	T.H.D. = 1 %, NAB
Total Harmonic Distortion	T.H.D.		0.05	0.3	%	(2)	v_O = 0.3 V, NAB
Input Impedance	r_i	50	100		kΩ	(2)	
Equivalent Input Noise Voltage	v_{nin}		1.1	1.7	μVr.m.s.	(3)	R_G = 2.2 kΩ, NAB
Cross Talk		−50	−65		dB	(4)	v_o = 1V, (The other channel v_{in} = 0, R_G = 2.2kΩ)
Channel Balance		−0.3	0	+0.3	dB	(4)	v_O = 0.3 V

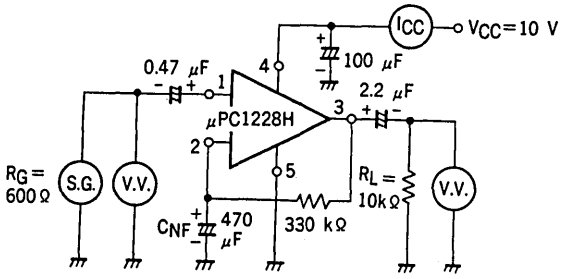
CONNECTION DIAGRAM



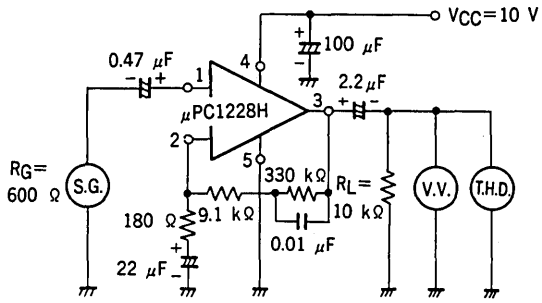
Pin No.	Electrical connection
1	Input 1
2	Negative feed back 1
3	Output 1
4	Power supply: +Vcc
5	Ground
6	Output 2
7	Negative feed back 2
8	Input 2

TEST CIRCUITS

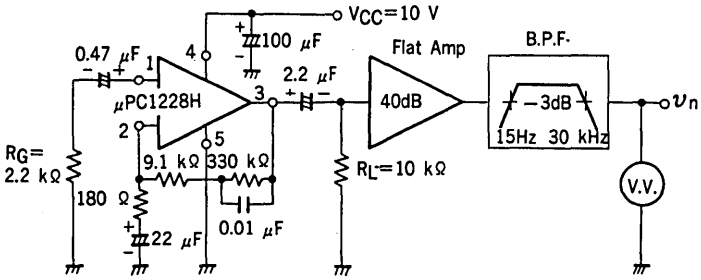
(1) I_{CC}, A_{vo} test circuit



(2) A_v, v_{OM}, T.H.D., Z_{in} test circuit (for Ch. 1)

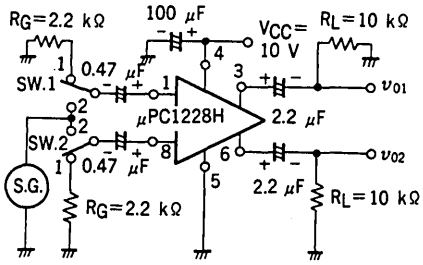


(3) v_{nin} test circuit (for CH. 1)



NOTE: v_{nin} is calculated by v_n and amp. gain (A_v +40dB).

(4) Cross talk, Channel balance test circuit



NOTE 1: External components of the IC are the same as the test circuit (2).

2: Cross talk procedure

Switch position SW.1 → 2, SW.2 → 1, 20 log v_{o2}/v_{o1}

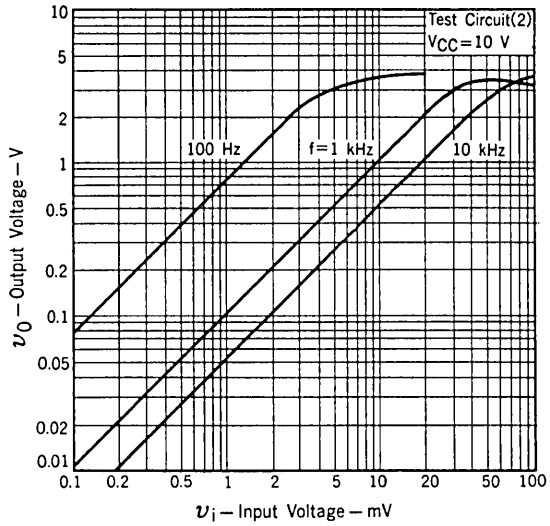
Switch position SW.1 → 1, SW.2 → 2, 20log v_{o1}/v_{o2}

3: Channel balance

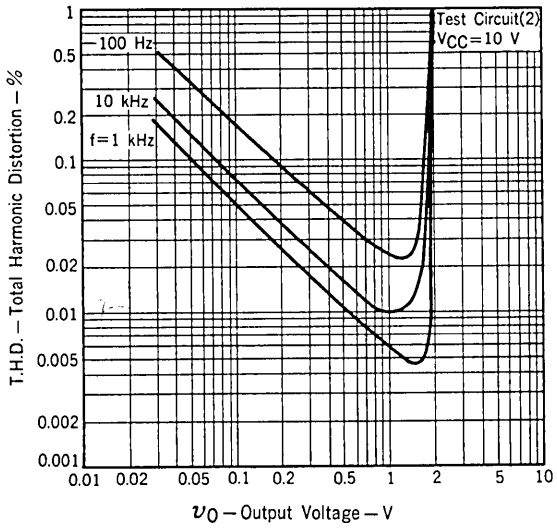
Switch position SW.1 → 2, SW.2 → 2, 20 log v_{o1}/v_{o2}

TYPICAL CHARACTERISTICS (Ta = 25 °C)

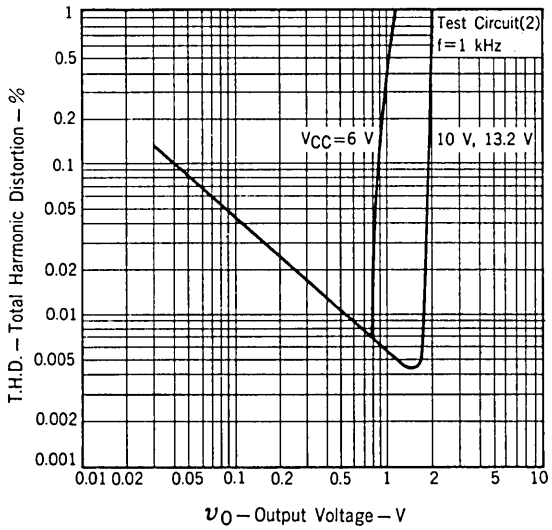
OUTPUT VOLTAGE vs. INPUT VOLTAGE



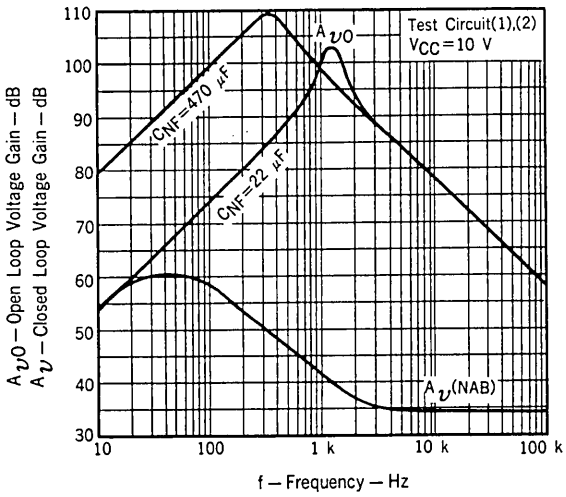
TOTAL HARMONIC DISTORTION vs. OUTPUT VOLTAGE



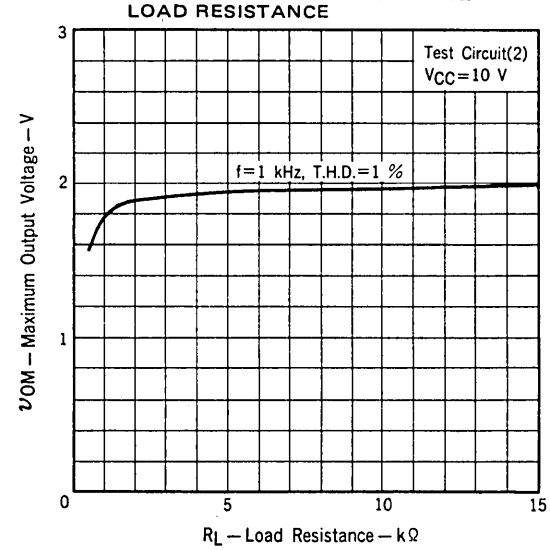
TOTAL HARMONIC DISTORTION vs. OUTPUT VOLTAGE



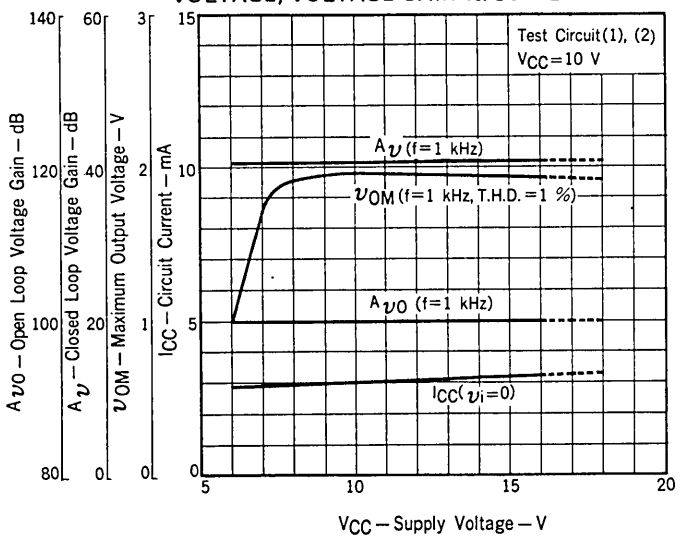
VOLTAGE GAIN vs. FREQUENCY



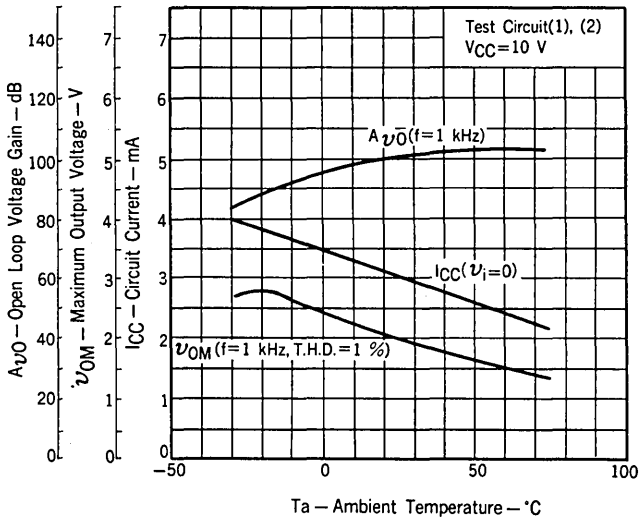
MAXIMUM OUTPUT VOLTAGE vs. LOAD RESISTANCE



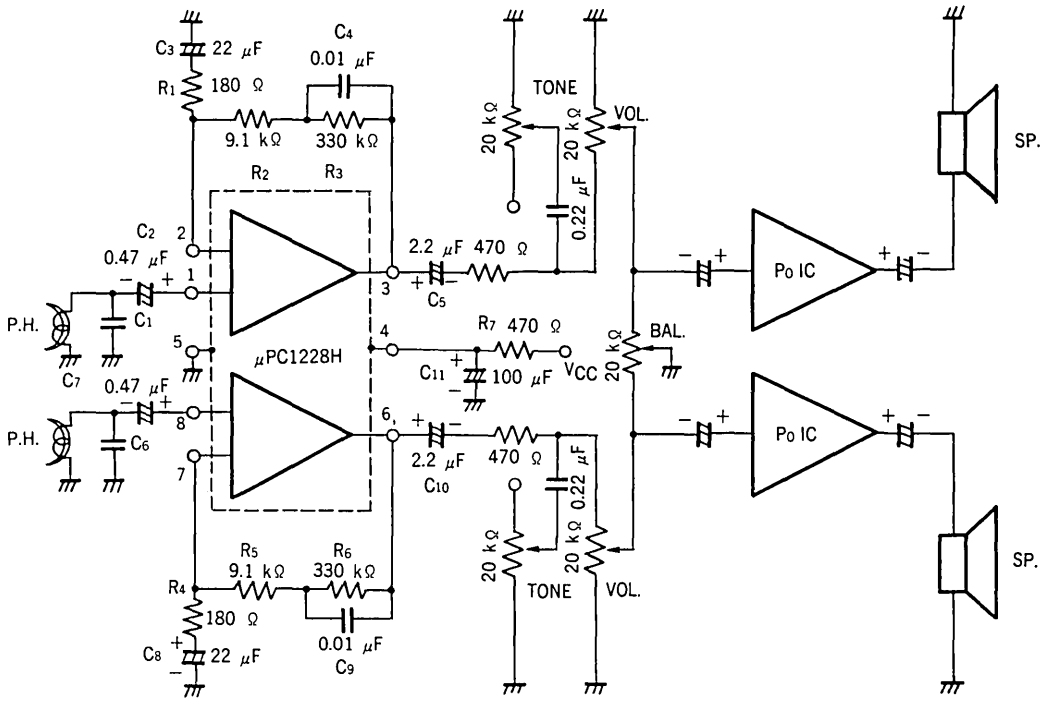
CIRCUIT CURRENT, MAXIMUM OUTPUT VOLTAGE, VOLTAGE GAIN vs. SUPPLY VOLTAGE



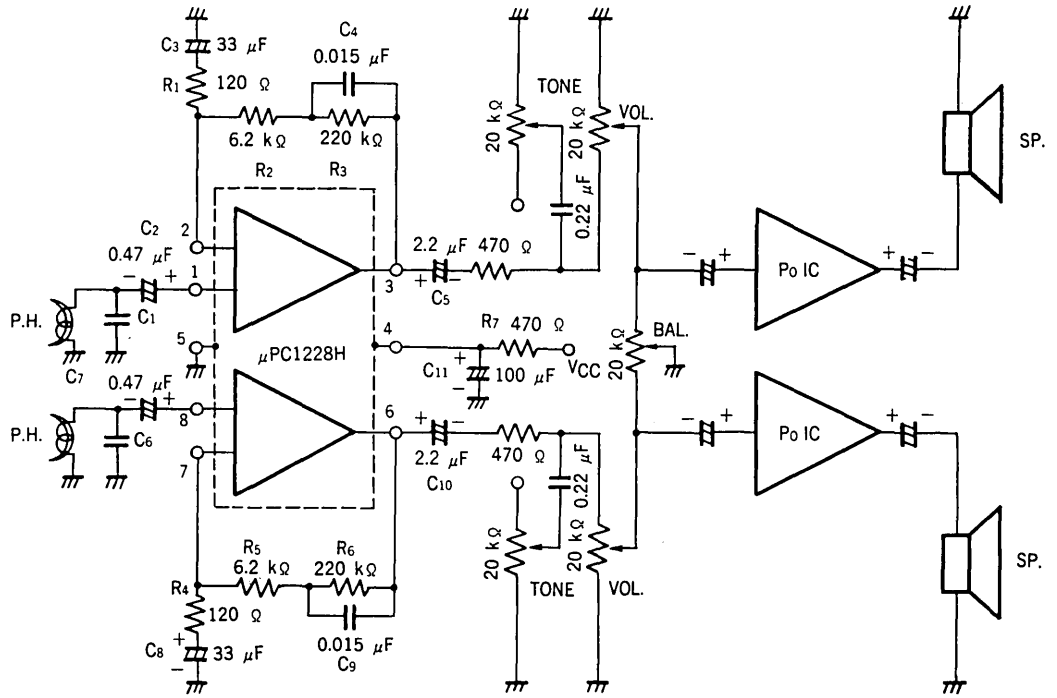
QUIESCENT CURRENT, MAXIMUM OUTPUT VOLTAGE, VOLTAGE GAIN vs. AMBIENT TEMPERATURE



TYPICAL APPLICATION 1



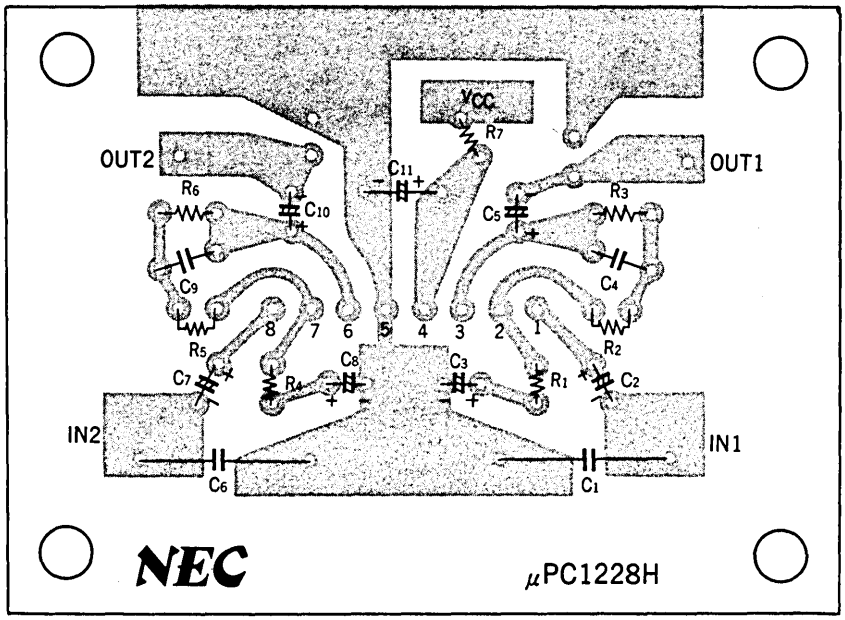
TYPICAL APPLICATION 2



* When supply voltage of pin ④ is down to 6 V, please use TYPICAL APPLICATION 2.

TYPICAL PRINTED CIRCUIT BOARD PATTERN

Bottom View



BIPOLAR ANALOG INTEGRATED CIRCUITS
μPC1181H3, μPC1182H3

5.8 W AF POWER AMPLIFIER
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

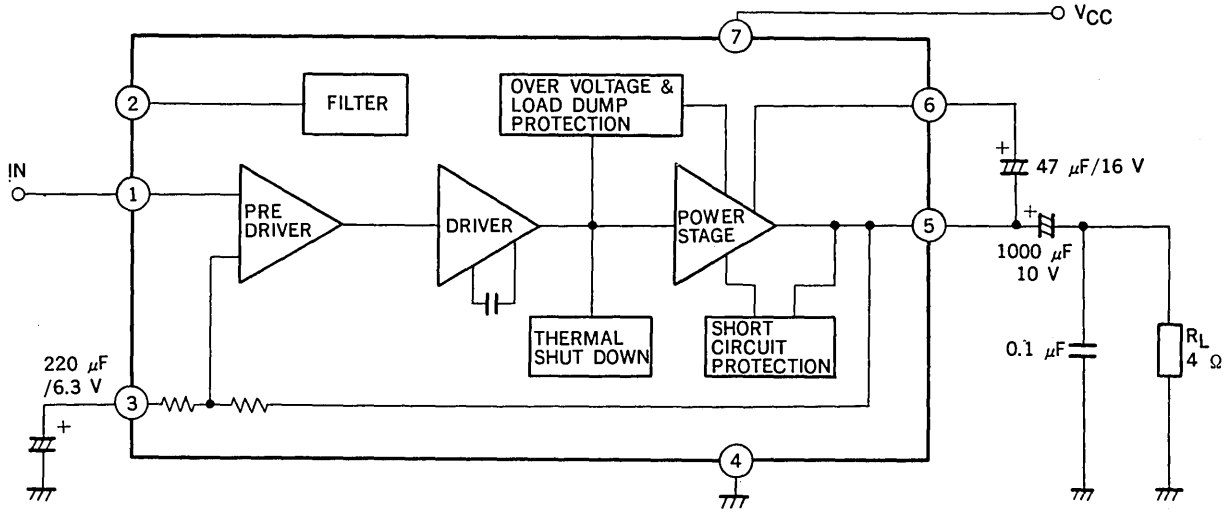
DESCRIPTION

The μPC1181H3 and μPC1182H3 are audio power amplifiers which is especially designed for car radio and car stereo.
The devices are encapsulated in newly developed small packages featuring low thermal resistance, providing easy design for 2 Ω.
At 14.4 V the devices give output power of 7 W with $R_L = 4\ \Omega$ and 11 W $R_L = 2\ \Omega$.

FEATURES

- High output power : $P_O = 7$ W TYP. $R_L = 4\ \Omega$ at 14.4 V
  $P_O = 11$ W $R_L = 2\ \Omega$ at 14.4 V
- Low transient noise at power supply switch-on.
- Few external components required (4 pieces)
- Assembly ease, due to 7 lead single in-line package with no insulation requirement.
- Pin orders of these types are symmertical each other, which reduces the area of Printed Circuit Board effectively.
- Following protective circuits are provided
  (1) Load dump protection
  (2) Thermal shut down protection
  (3) Over voltage protection
  (4) Output terminal short circuit protection
- These ICs are not destroyed nor damaged even when any of neighboring two terminals are shorted to each other, or revere insertion into Printed Circuit Board is occurred.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Supply Voltage (Surge PW = 200 ms)	$V_{CC\ surge}$	40	V
Supply Voltage (Quiecent)	V_{CC1}	25*	V
Supply Voltage (Operational)	V_{CC2}	18	V
Circuit Current (Peak)	$I_{CC\ peak}$	4.5	A
Package Dissipation	P_D	12	W
Operating Temperature	T_{opt}	−30 to +75*	°C
Storage Temperature	T_{stg}	−55 to +150	°C

*Using an aluminum heat sink 100 x 100 x 1 mm

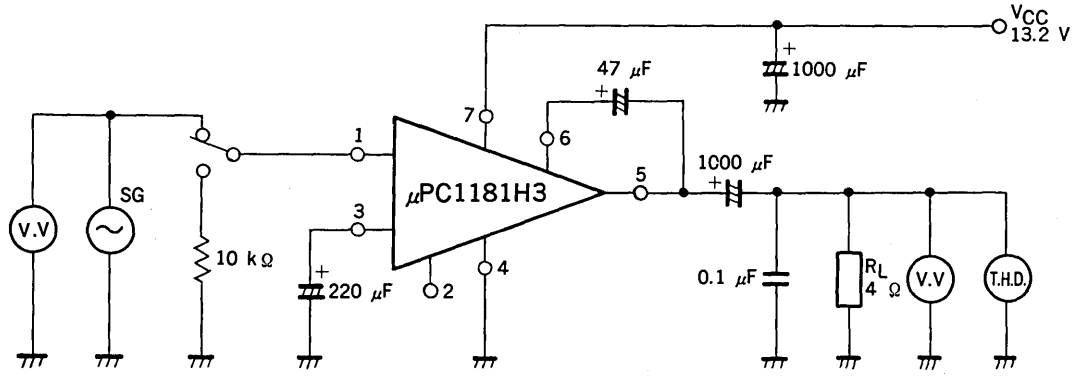
RECOMMENDED CONDITIONS (Ta = 25 °C)

Supply Voltage Range	9.5 to 16	V
Load Impedance	4 to 2	V

ELECTRICAL CHARACTERISTICS (Ta = 25 °C, f = 1 kHz, R_L = 4 Ω)

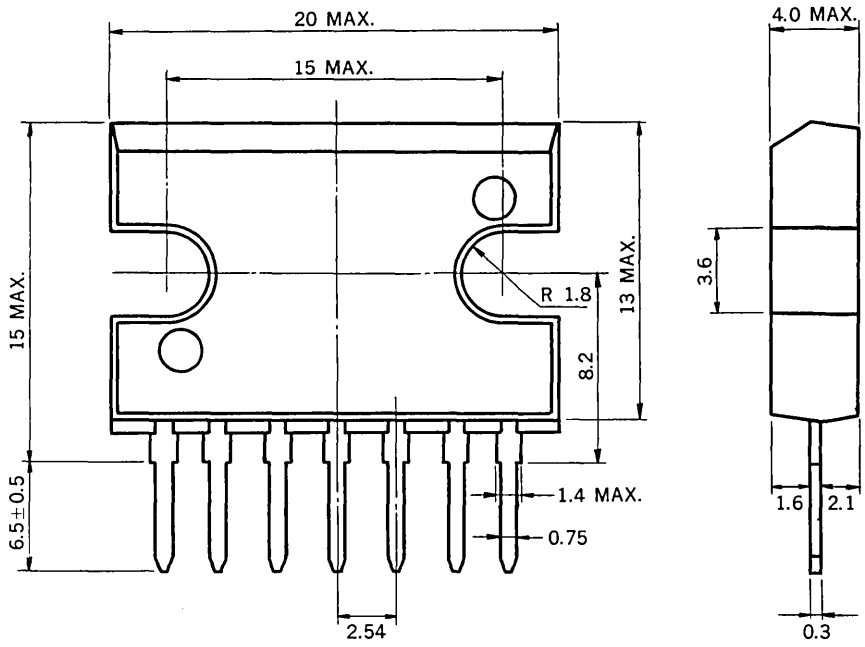
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	I_{CC}	23	45	80	mA	v_{in} = 0, V_{CC} = 13.2 V
Output Power	P_O	5.0	5.8		W	R_L = 4 Ω, T.H.D. = 10 %, V_{CC} = 13.2 V
			7		W	R_L = 4 Ω, T.H.D. = 10 %, V_{CC} = 14.4 V
			9.2		W	R_L = 2 Ω, T.H.D. = 10 %, V_{CC} = 13.2 V
			11		W	R_L = 2 Ω, T.H.D. = 10 %, V_{CC} = 14.4 V
Total Harmonic Distortion			0.3	1	%	P_O = 0.5 W
Voltage Gain	A_v	51	53.5	56	dB	P_O = 0.5 W
Output Noise Level	v_n		1.4	4.0	mVr.m.s.	R_g = 10 kΩ

TEST CIRCUIT & TYPICAL APPLICATIONS



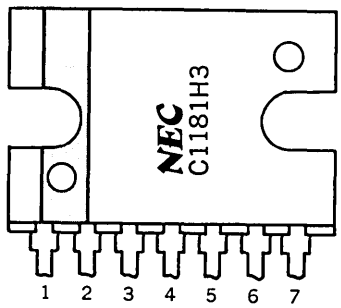
*Mylar Film Capacitor

PACKAGE DIMENSIONS (in millimeters)

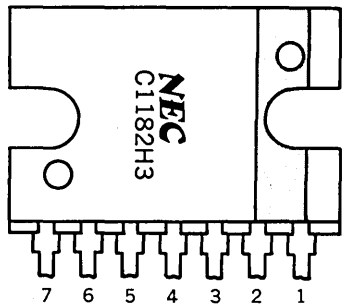


CONNECTION DIAGRAM

μPC1181H3



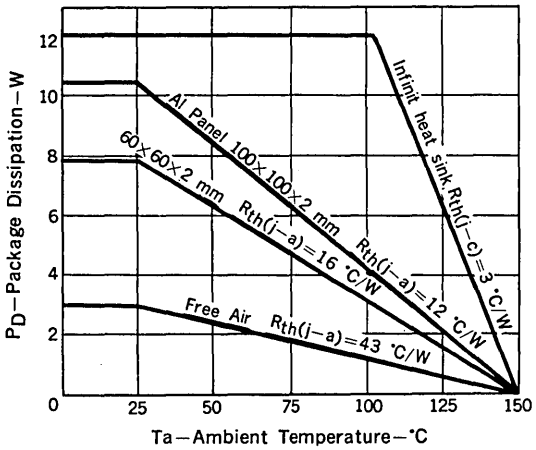
μPC1182H3



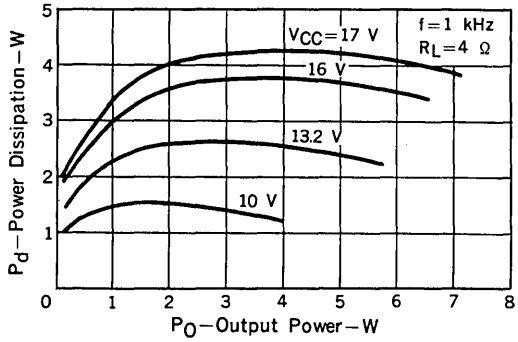
Pin No.	μPC1181H3 μPC1182H3
1	Input
2	Bypass
3	Feedback
4	GND
5	Output
6	Boot strap
7	Power supply

TYPICAL CHARACTERISTICS (Ta = 25 °C)

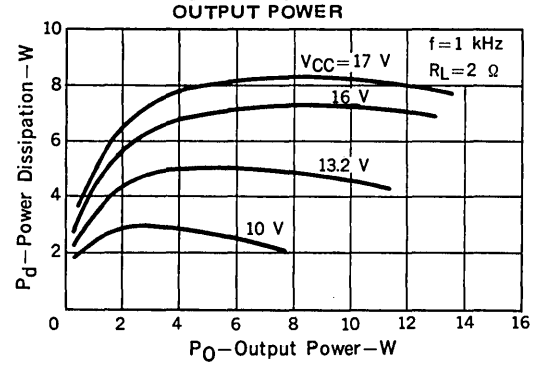
PACKAGE DISSIPATION vs. AMBIENT TEMPERATURE



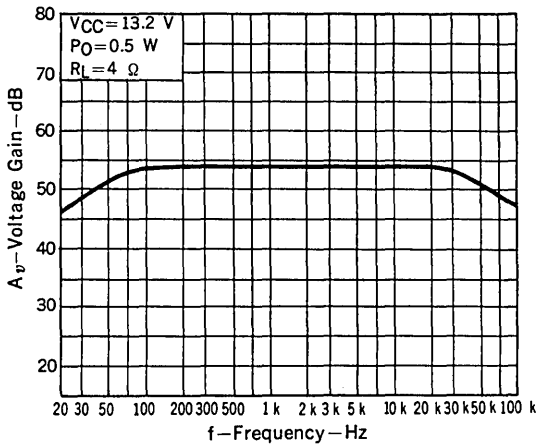
POWER DISSIPATION vs. OUTPUT POWER



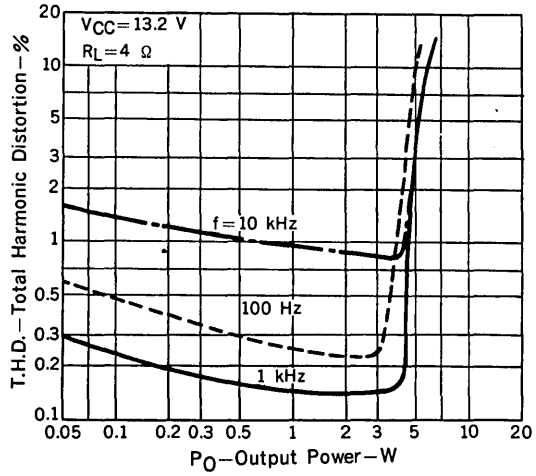
POWER DISSIPATION vs. OUTPUT POWER



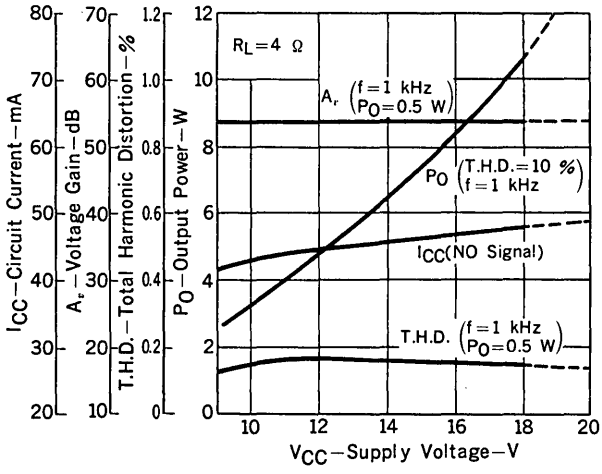
VOLTAGE GAIN vs. FREQUENCY



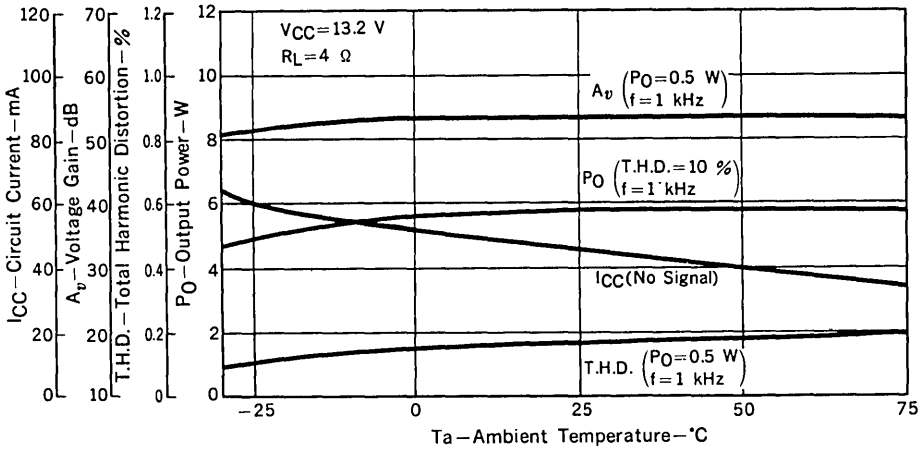
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



SUPPLY VOLTAGE CHARACTERISTICS



TEMPERATURE CHARACTERISTICS



TYPICAL APPLICATIONS

(1) Circuit Example

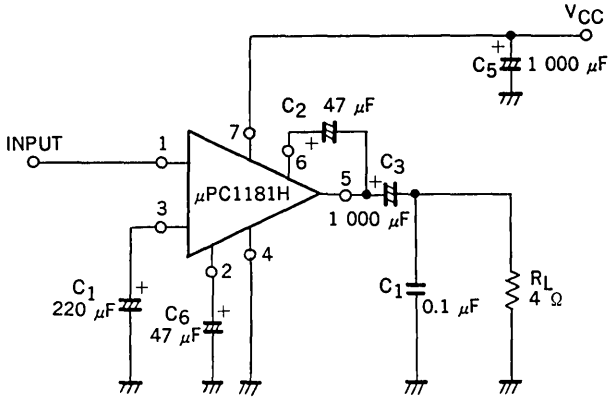


Fig. A

- The supply ripple rejection ratio is improved by C_6.

(2) Circuit Example

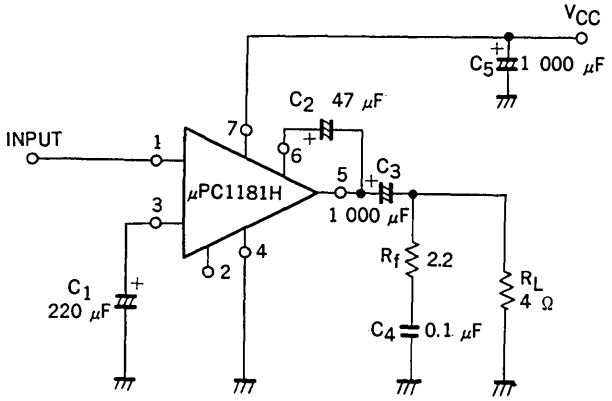


Fig. B

- The capacitor C_4 is for preventing a parasitic oscillation.
  A mylar film capacitor is recommended.
  If an oscillation occure, increase capacitance of C_4, or connect an additional resistor R_1 as shown in Fig. B.

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1185H2

7 W DUAL AF POWER AMPLIFIER

SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

The μPC1185H2 is a dual audio power amplifiers in a 12-lead single in-line package, specifically designed for car stereo application.

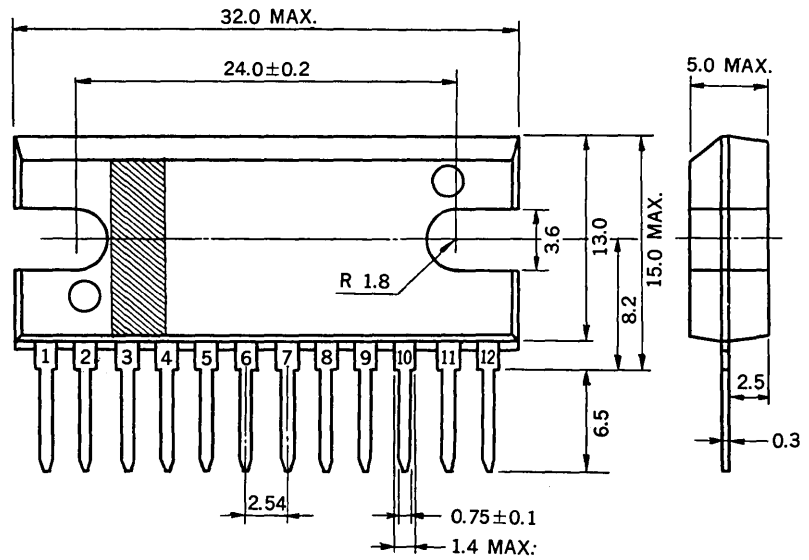
This device provides an output power of 7 watts per channel to 4 ohm load with 10 percent distortion at 14.4 volts power supply.

The μPC1185H2 is pin to pin equivalent to the μPC1185H.

FEATURES

- Very low number of external small size components.
- Easy mounting with no electrical isolation between the package and heat sink.
- Space saving due to the single in-line package.
- Very low transient noise at power switch-on.
- No damage for reverse insertion on the PC-board.
- Thermal shut-down circuit included.
- Load dump protection circuit included.

PACKAGE DIMENSIONS (in millimeters)



CONNECTION DIAGRAM

Pin No.	Function
1	GND (for input)
2	Output 1
3	Boot Strap 1
4	Filter
5	N.F. 1
6	Input 1
7	Input 2
8	N.F. 2
9	$+V_{CC}$
10	Boot Strap 2
11	Output 2
12	GND (for output)

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

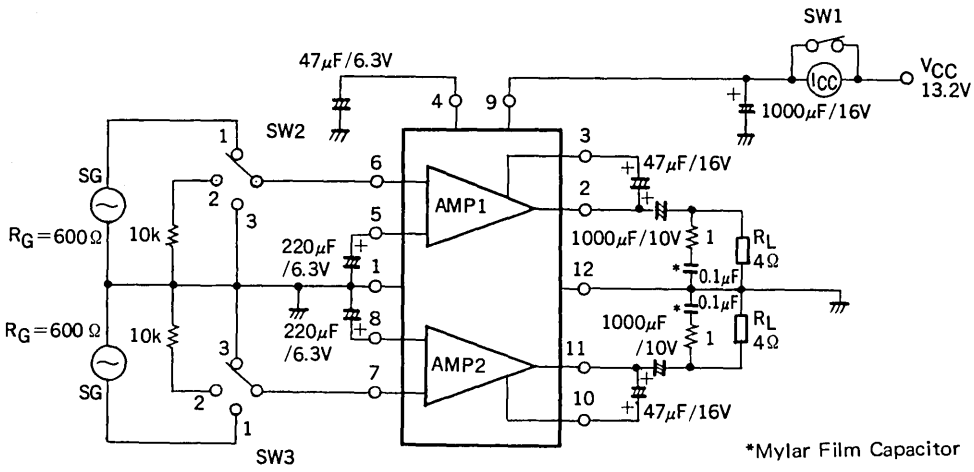
Supply Voltage (Surge PW = 200 ms)	$V_{CCsurge}$	40	V
Supply Voltage (Quiecent)	V_{CC1}	25*	V
Supply Voltage (Operational)	V_{CC2}	18	V
Circuit Current (Peak)	$I_{CC\ peak}$	4.5	A
Package Dissipation	P_D	20	W
Operating Temperature	T_{opt}	−30 to +75*	°C
Storage Temperature	T_{stg}	−55 to +150	°C

*Using an aluminum heat sink $\theta th(c\text{-}a) = 6$ °C/W

ELECTRICAL CHARACTERISTICS (Ta = 25 °C, V_{CC} = 13.2 V, f = 1 kHz, R_L = 4 Ω)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	I_{CC}	30	80	180	mA	v_{in} = 0
Output Power	P_O		7.0		W	T.H.D. = 10 %, V_{CC} = 14.4 V
		5.0	5.8		W	T.H.D. = 10 %, V_{CC} = 13.2 V
			8.5		W	T.H.D. = 10%, R_L = 2Ω, V_{CC} = 13.2V
Total Harmonic Distortion	T.H.D.		0.3	1.0	%	P_O = 0.5 W
			0.4		%	P_O = 2 W, R_L = 2 Ω
Voltage Gain	A_v	51	54	58	dB	P_O = 0.5 W
Channel Balance	ΔA_v			±1.5	dB	P_O = 0.5 W
Cross Talk	CT	30	45		dB	f = 1 kHz, other ch R_G = 0
Output Noise Level	v_n		1.4	4	mVr.m.s.	R_G = 10 kΩ

TEST CIRCUIT



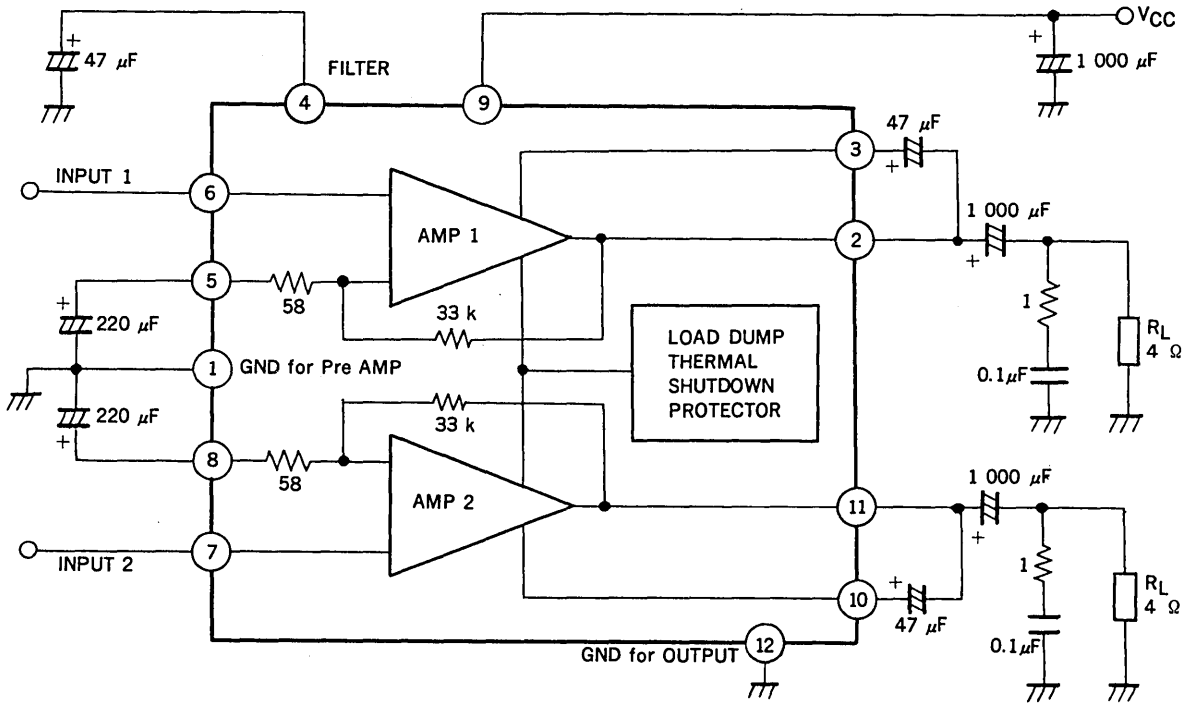
*Mylar Film Capacitor

Table 1

	SW1	SW2	SW3
I_{CC}	OFF	3	3
P_O	ON	1 (3)	3 (1)
T.H.D.	ON	1 (3)	3 (1)
A_v	ON	1 (3)	3 (1)
v_n	ON	2	2
SVR	ON	3	3
CT	ON	1 (3)	3 (1)

The position of switches at testing AMP1 is show in table 1. The numbers in parenthesis show the position of switches in testing AMP2.

BLOCK DIAGRAM

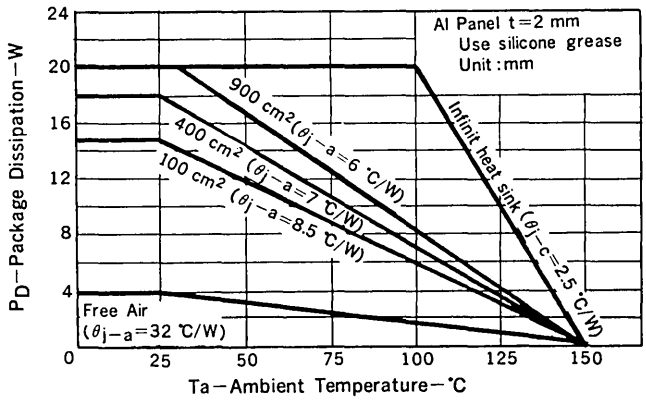


NOTICE :

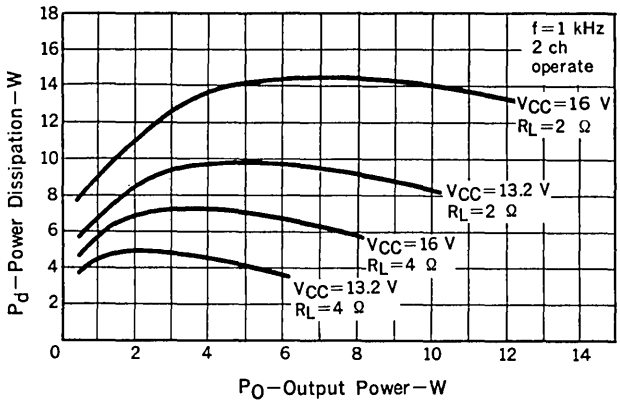
This device is not recommended for bridge and power booster amplifiers because the μPC1230H suitable for its.

TYPICAL CHARACTERISTICS (Ta = 25 °C)

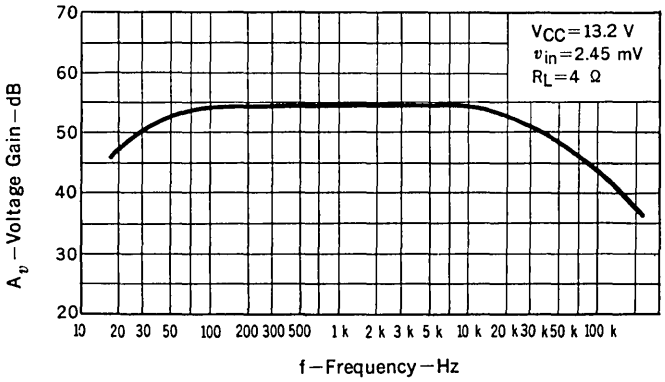
PACKAGE DISSIPATION vs. AMBIENT TEMPERATURE



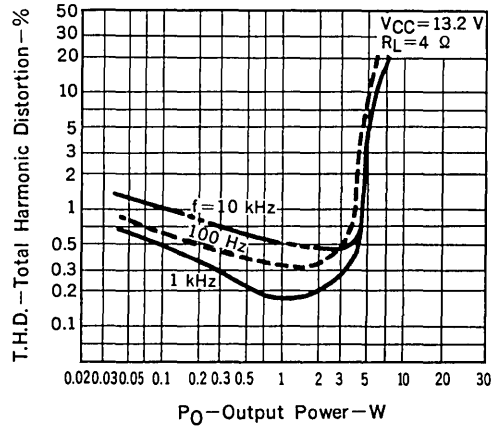
POWER DISSIPATION vs. OUTPUT POWER



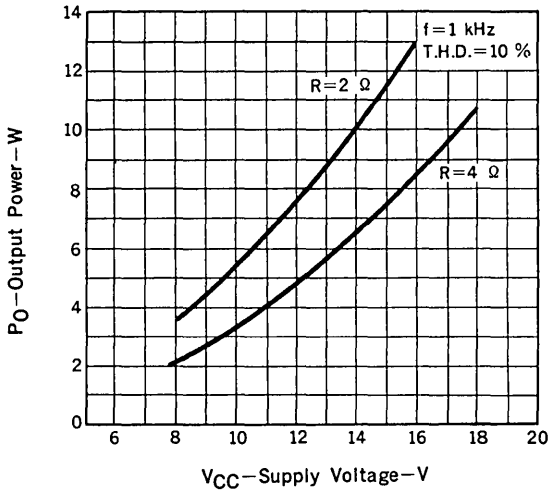
VOLTAGE GAIN vs. FREQUENCY



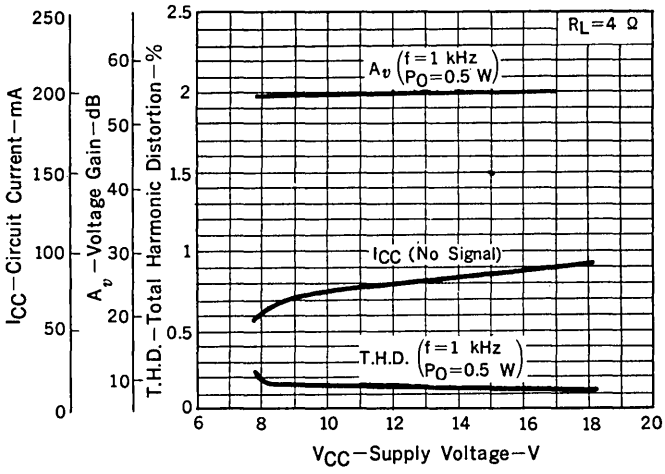
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



SUPPLY VOLTAGE CHARACTERISTICS



SUPPLY VOLTAGE CHARACTERISTICS



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1230H

23 W AF POWER AMPLIFIER
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

The μPC1230H is an audio power amplifier in a 12-lead single in-line package, specifically designed for car stereo application. Typically it provided 23 watts output power at 14.4 volt and 20 watts at 13.2 V on a 4 ohm load.

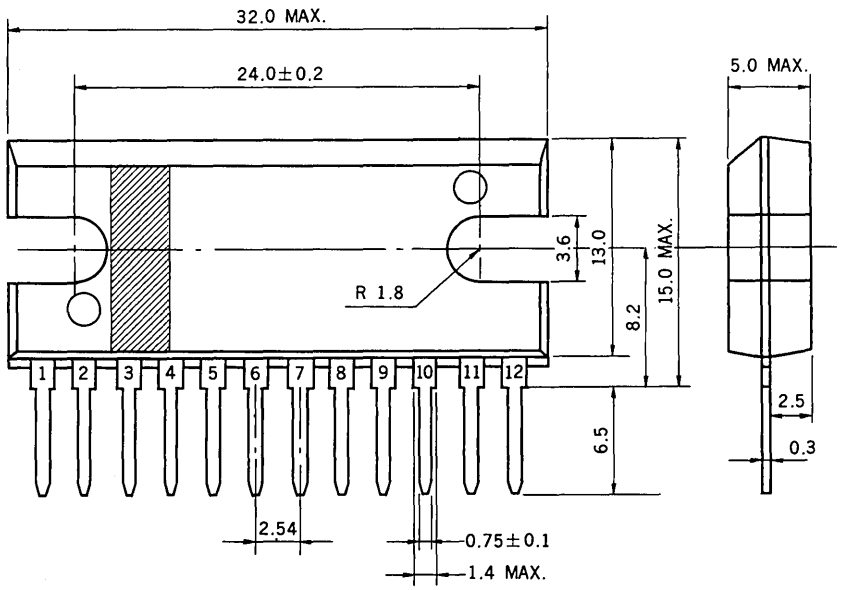
This device can be used without output capacitors, because it incorporates the orignal short circuit protection which protects output power transistors and a speaker at the same time when the output terminal is shorted to ground.

FEATURES

- Can be used as OCL connection.
- Very low output offset voltage : V_{offset} = 150 mV (MAX.)
- High output power : P_O = 23 W TYP. R_L = 4 Ω at 14.4 V
  P_O = 20 W TYP. R_L = 4 Ω at 13.2 V
- Very low distortion.
- Very low number of external low size components, very simple mounting system with no electrical isolation between the package and the heat sink.
- Low thermal resistance : $\theta_{J-C} \fallingdotseq 2.5$ °C/W
- Following protective circuit as provide

  (1) Load dump protection
  (2) Output therminal short circuit protection
  (3) Thermal shut down protection
  (4) Speaker protection

PACKAGE DIMENSIONS
(in millimeters)



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Supply Voltage (Note)	$V_{CC\ surge}$	40	V
Supply Voltage (Quiecent)	V_{CC1}	25*	V
Supply Voltage (Operational)	V_{CC2}	18	V
Circuit Current (Peak)	$I_{CC\ peak}$	4.5	A
Package Dissipation	P_D	20	W
Operating Temperature	T_{opt}	−30 to +75*	°C
Storage Temperature	T_{stg}	−55 to +150	°C

*Using an aluminum heat sink $\theta_{th(c-a)} = 4$ °C/W
Note : Pulse width = 200 ms, Trise ≥ 1 ms

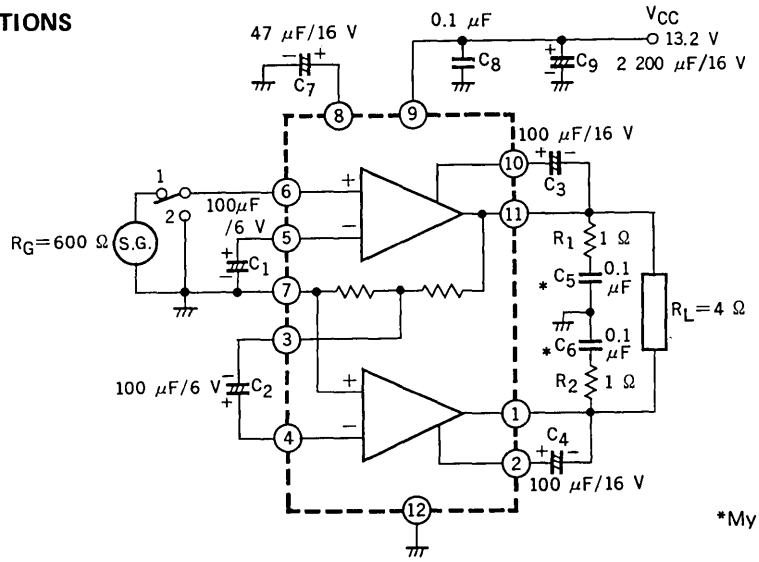
RECOMMENDED OPERATING CONDITIONS (Ta = 25 °C)

Supply Voltage Range	9.5 to 16	V
Load Impedance	3.2 to 16	Ω

ELECTRICAL CHARACTERISTICS (Ta = 25 °C, V_{CC} = 13.2 V, R_L = 4 Ω, f = 1 kHz)

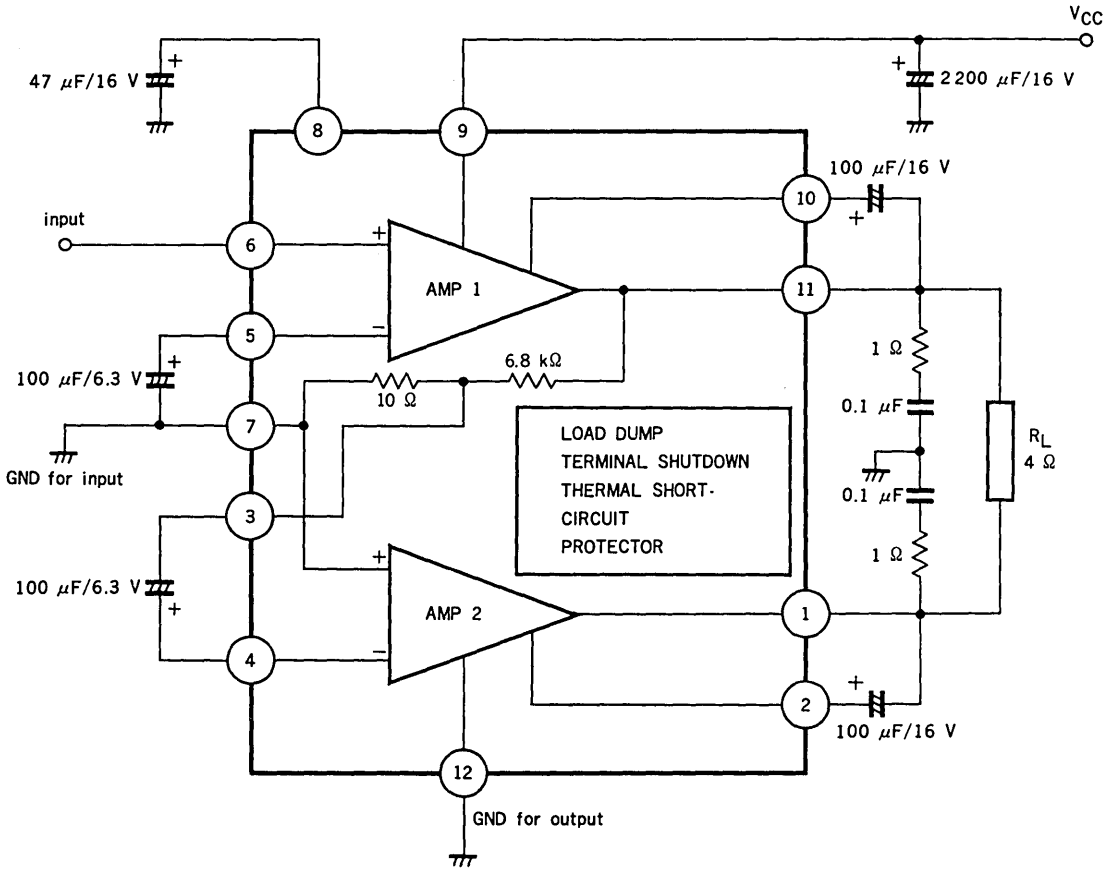
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Quiescent Current	I_{CC}		90	180	mA	$v_{in} = 0$
Output Offset Voltage	V_{offset}			±150	mV	$v_{in} = 0$
Output Power	P_O		23		W	V_{CC} = 14.4 V, T.H.D. = 10 %
		16	20		W	V_{CC} = 13.2 V, T.H.D. = 10 %
Voltage Gain	A_V	53	55	56	dB	V_{in} = 2.45 mV
Total Harmonic Distortion	T.H.D.		0.15	1.0	%	P_O = 2 W
Output Noise Level	v_n		0.65		mV	R_G = 0, BW = 20 to 20 kHz
Supply Voltage Rejection Ratio	SVR		45		dB	R_G = 0, f_{rip} = 100 Hz, v_{rip} = 0.5 V
Input Resistance	R_i		45		kΩ	
Rolloff Frequency	f_H		90		kHz	A_v = −3 dB from 1 kHz Ref. High
	f_L		15		Hz	A_v = −3 dB from 1 kHz Ref. Low

TEST CIRCUIT & TYPICAL APPLICATIONS



*Mylar film capacitor

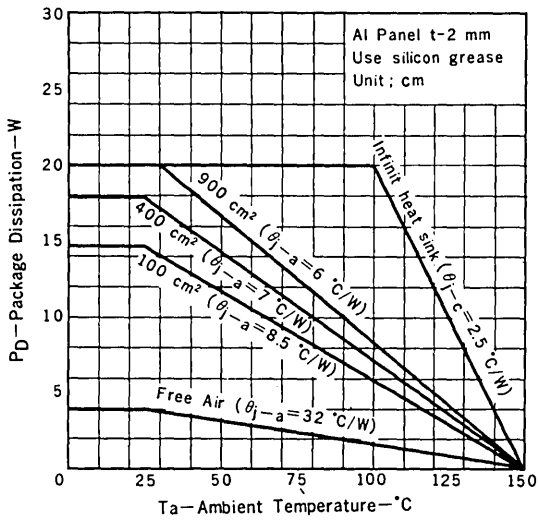
BLOCK DIAGRAM



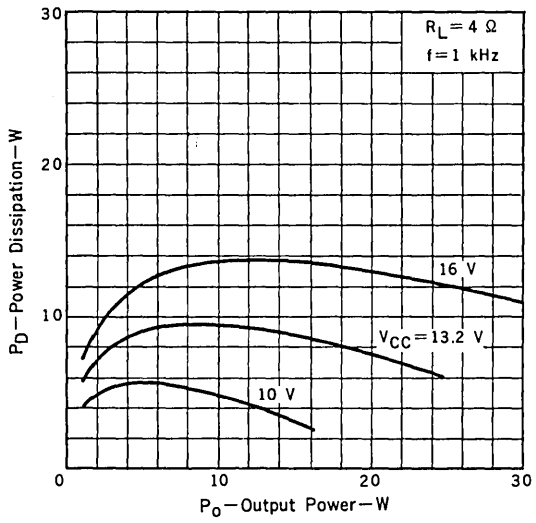
CONNECTION DIAGRAM

Pin No.	Function
1	Output 2
2	Boot Strap 2
3	Divided Output
4	Input 2
5	N.F. 1
6	Input 1
7	GND (for input)
8	Filter
9	$+V_{CC}$
10	Boot Strap 1
11	Output 1
12	GND (for output)

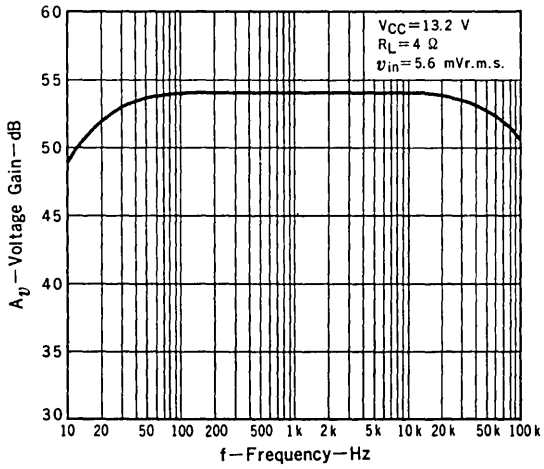
PACKAGE DISSIPATION vs.
AMBIENT TEMPERATURE



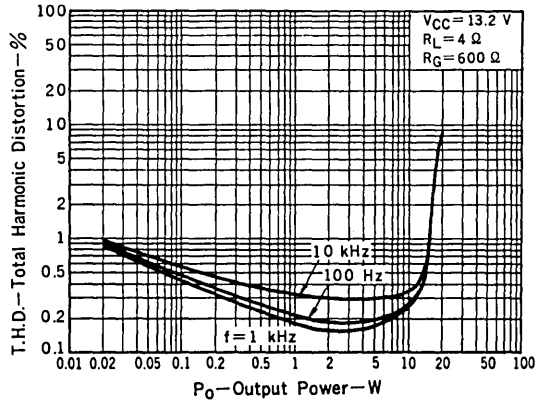
POWER DISSIPATION vs.
OUTPUT POWER



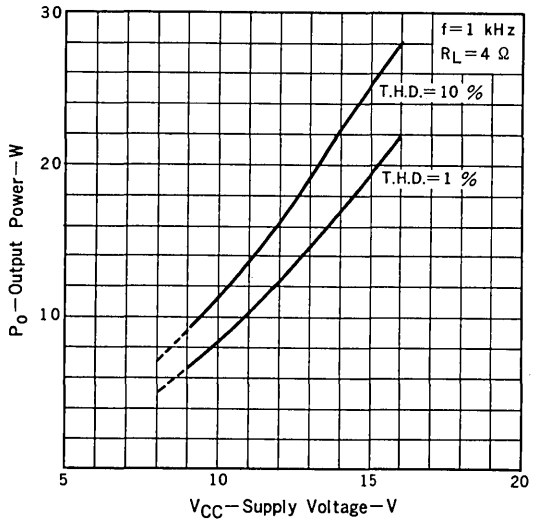
VOLTAGE GAIN vs.
FREQUENCY



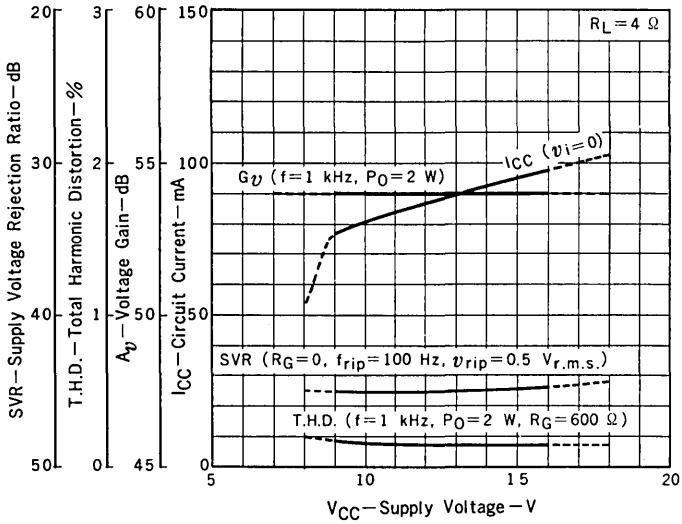
TOTAL HARMONIC DISTORTION
vs. OUTPUT POWER



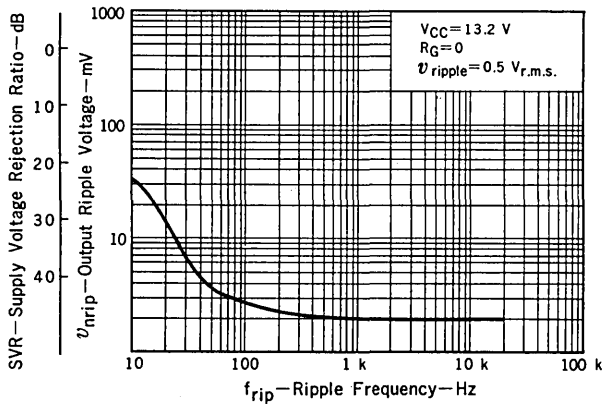
OUTPUT POWER vs.
SUPPLY VOLTAGE



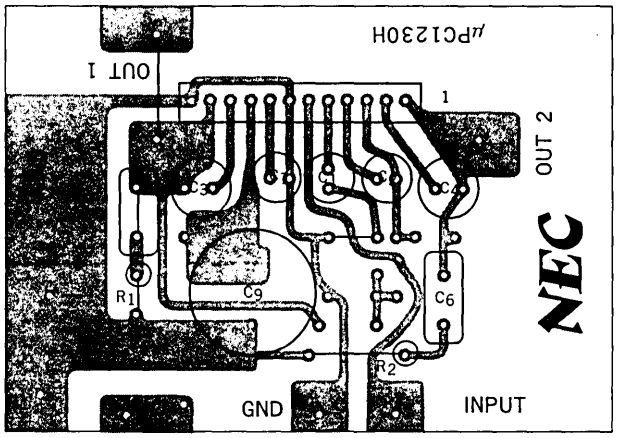
SUPPLY VOLTAGE CHARACTERISTICS



SUPPLY VOLTAGE REJECTION RATIO
vs. RIPPLE FREQUENCY



COMPONENTS LAYOUT FOR P.W. ASSEMBLY (Copper side)



BIPOLAR ANALOG INTEGRATED CIRCUITS

μPC1241H, μPC1242H

7 W AF POWER AMPLIFIER
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

DESCRIPTION

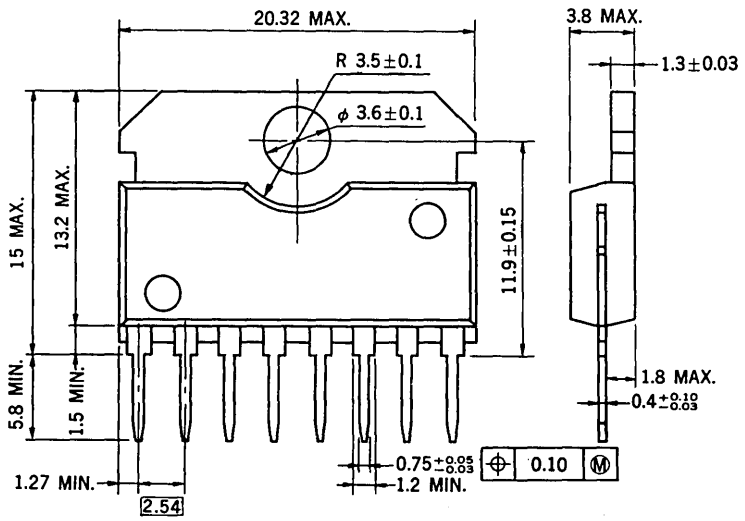
The μPC1241H and μPC1242H are audio power amplifiers which is especially designed for car radio and car stereo.
The devices are encapsulated in newly developed small packages featuring low thermal resistance, providing easy design for 2 Ω load circuit and 4 Ω load BTL circuit.
At 14.4 V the devices give output power of 7 W at R_L = 4 Ω and 11 W at R_L = 2 Ω

FEATURES

- High output power : P_o= 7 W TYP. @ R_L= 4 Ω, T.H.D. = 10 %, V_{CC}= 14.4 V
  P_o=11 W TYP. @ R_L= 2 Ω, T.H.D. = 10 %, V_{CC}= 14.4 V
  P_o=18 W (Bridge) @ R_L= 4 Ω, T.H.D. = 10 %, V_{CC}= 14.4 V
- Low distortion : T.H.D.=0.1 % TYP. @ R_L= 4 Ω, P_o= 0.5 W
- High reliability : of the chip and package with additional complete safety during operation thanks to protection against;
  (1) Load dump voltage surge.
  (2) Over rating chip temperature (150 °C).
  (3) Output DC and AC short circuit to ground or V_{CC}.
  (4) Revere insertion.

  These ICs are not destroyed nor damaged even when any of neighboring two terminals are shorted to each other.
- Space and cost saving: very low number of external components, very simple mounting system with no electrical isolation between the package and the heat sink (one screw only).
- Pin orders of these types are symmertical each other, which reduces the area of Printed Circuit Board effectively.

PACKAGE DIMENSIONS (in millimeters)



ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Supply Voltage (Surge PW=200 ms)	$V_{CC\ surge}$	50	V
Supply Voltage (Quiecent)	V_{CC1}	25*	V
Supply Voltage (Operational)	V_{CC2}	18	V
Circuit Current (Peak)	$I_{CC\ peak}$	4.5	A
Package Dissipation	P_D	12	W
Operating Temperature	T_{opt}	−30 to +75*	°C
Storage Temperature	T_{stg}	−55 to +150	°C

*Using an aluminum heat sink 100 X 100 X 1 mm

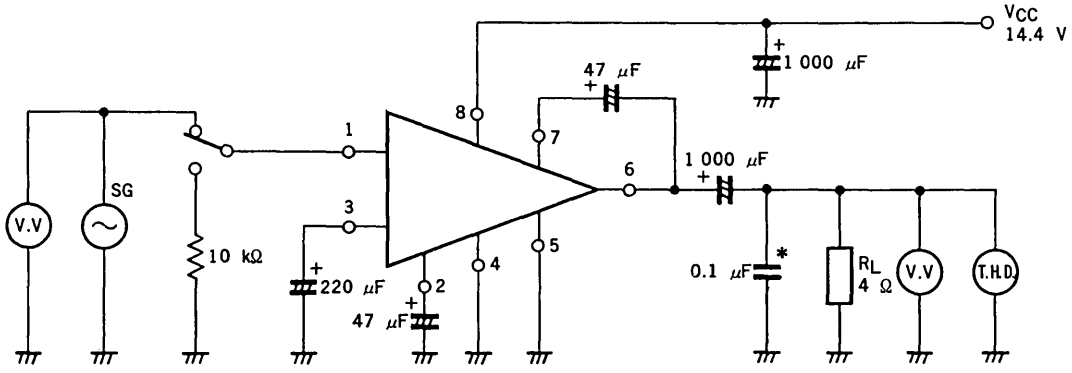
RECOMMENDED CONDITIONS (T_a=25 °C)

Supply Voltage Range	9.5 to 16	V
Load Impedance	2 to 16	Ω

ELECTRICAL CHARACTERISTICS (T_a=25 °C, f = 1 kHz, R_L=4 Ω)

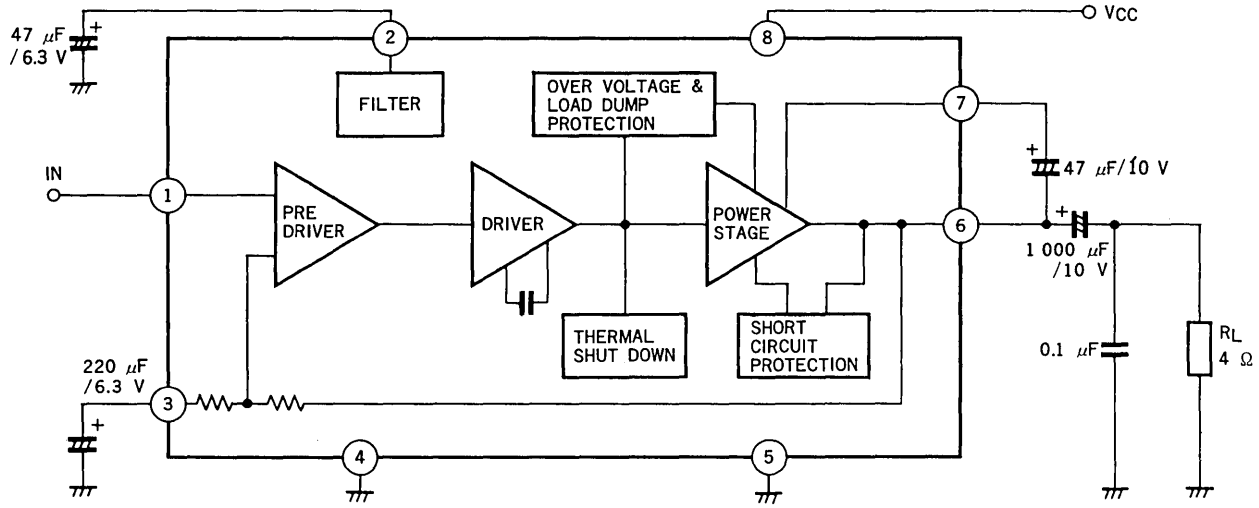
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	I_{CC}	25	45	80	mA	v_{in}=0, V_{CC}=13.2 V
Output Power	P_o	5.0	5.8		W	R_L=4 Ω, T.H.D.=10 %, V_{CC}=13.2 V
			7		W	R_L=4 Ω, T.H.D.=10 %, V_{CC}=14.4 V
			9.2		W	R_L=2 Ω, T.H.D.=10 %, V_{CC}=13.2 V
			11		W	R_L=2 Ω, T.H.D.=10 %, V_{CC}=14.4 V
Total Harmonic Distortion	T.H.D.		0.1	1	%	R_L=4 Ω, P_o=0.5 W, V_{CC}=13.2 V
			0.4		%	R_L=2 Ω, P_o=1 W, V_{CC}=13.2 V
Voltage Gain	A_v	49	51.5	54	dB	P_o=0.5 W
Output Noise Level	v_n		1.4	4.0	$mV_{r.m.s.}$	R_G=10 kΩ

TEST CIRCUIT



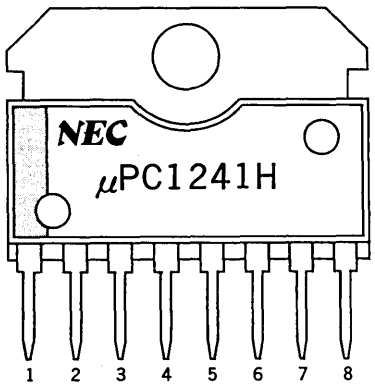
*Mylar Film Capacitor

BLOCK DIAGRAM

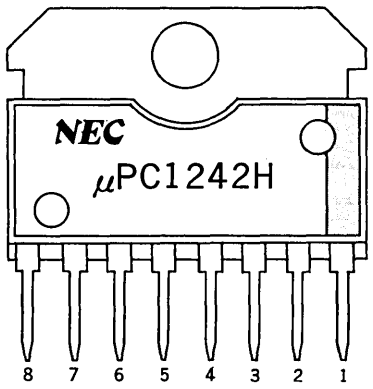


CONNECTION DIAGRAM

μPC1241H



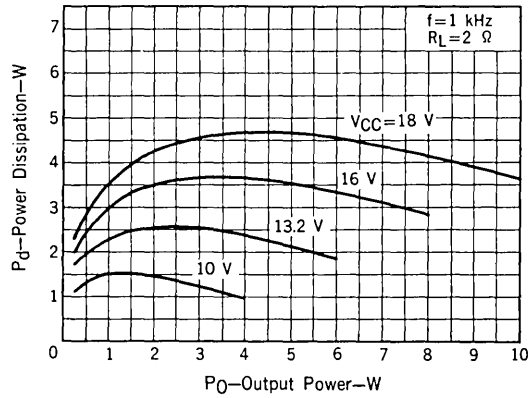
μPC1242H



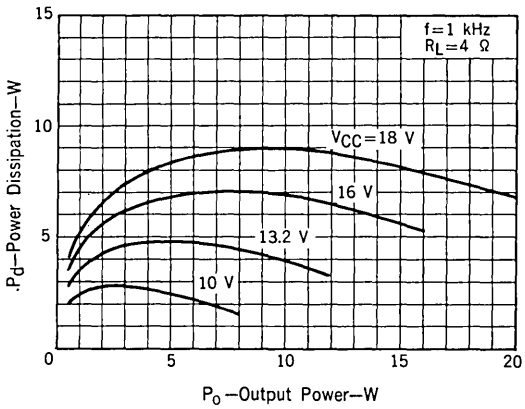
Pin No.	μPC1241H μPC1242H
1	Input
2	Bypass
3	Feedback
4	GND (for Input)
5	GND (for Output)
6	Output
7	Bootstrap
8	Power supply

TYPICAL CHARACTERISTICS (T_a=25 °C)

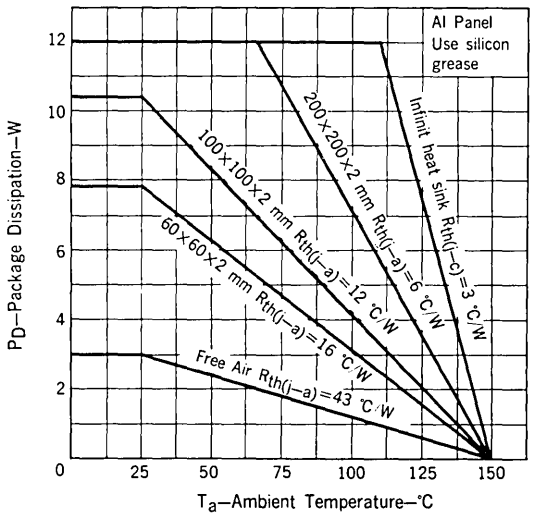
POWER DISSIPATION vs. OUTPUT POWER



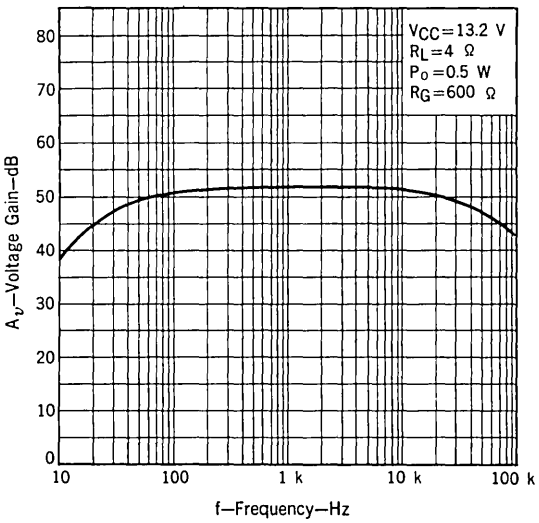
POWER DISSIPATION vs. OUTPUT POWER



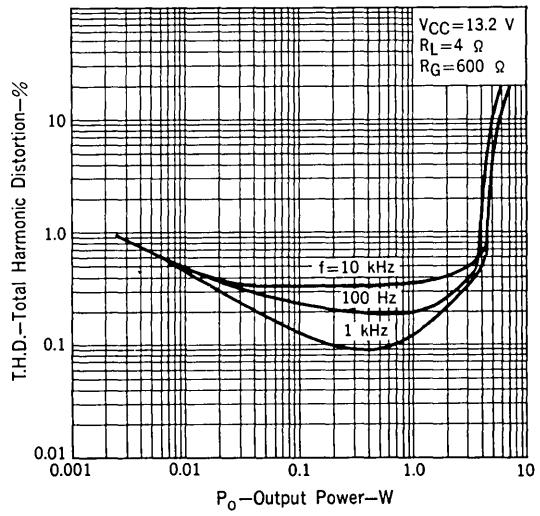
PACKAGE DISSIPATION vs. AMBIENT TEMPERATURE



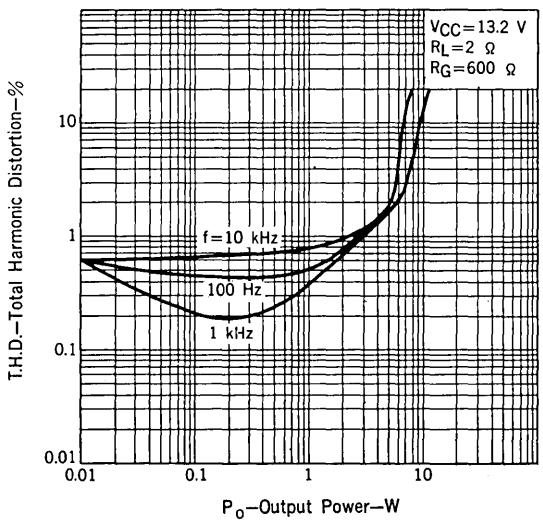
VOLTAGE GAIN vs. FREQUENCY



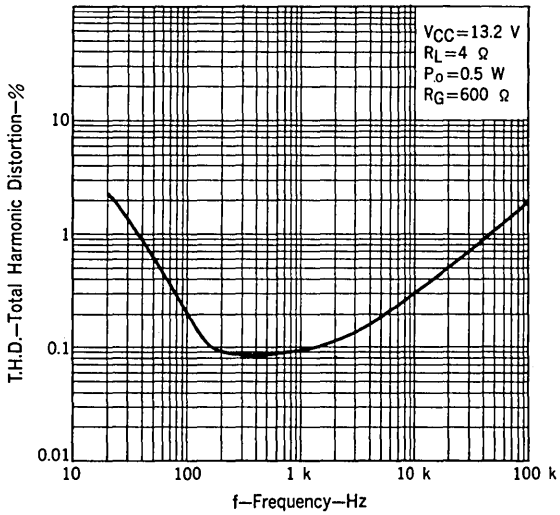
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



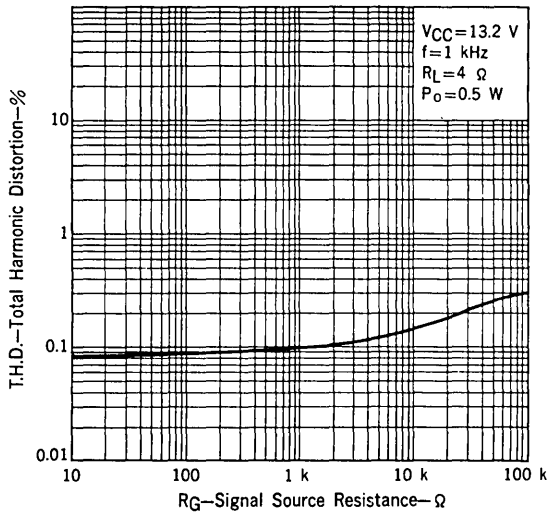
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



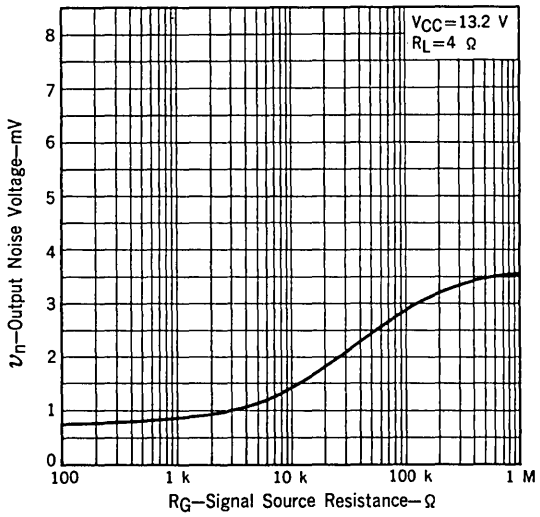
TOTAL HARMONIC DISTORTION
vs. FREQUENCY



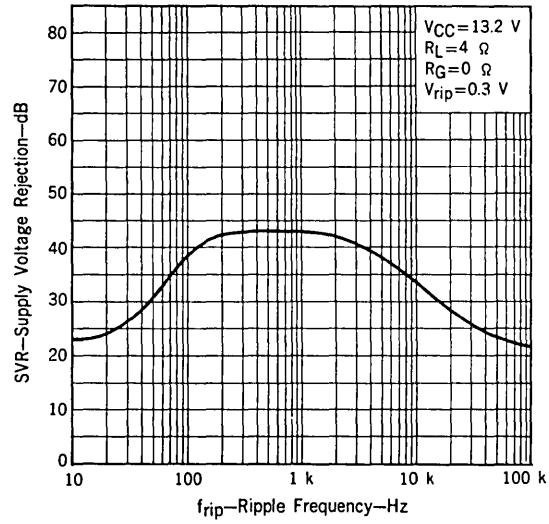
TOTAL HARMONIC DISTORTION
vs. SIGNAL SOURCE RESISTANCE



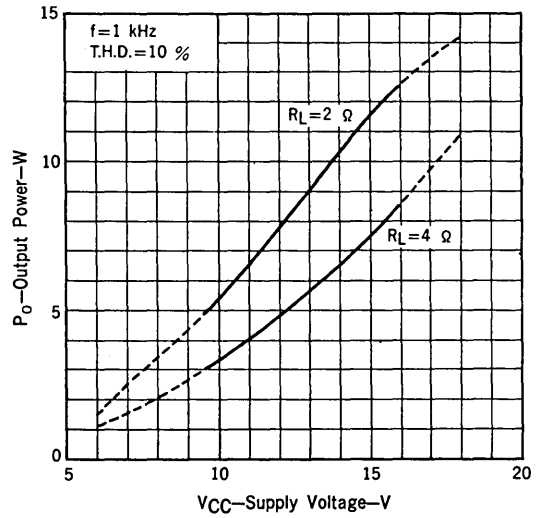
OUTPUT NOISE VOLTAGE vs.
SIGNAL SOURCE RESISTANCE



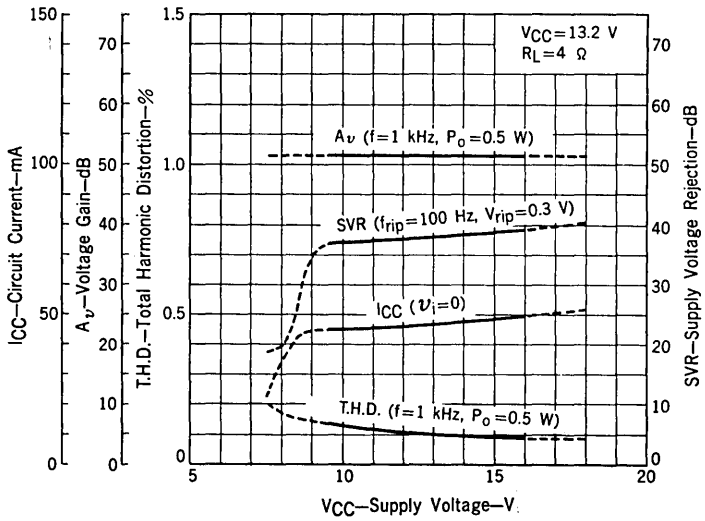
SUPPLY VOLTAGE REJECTION
vs. RIPPLE FREQUENCY



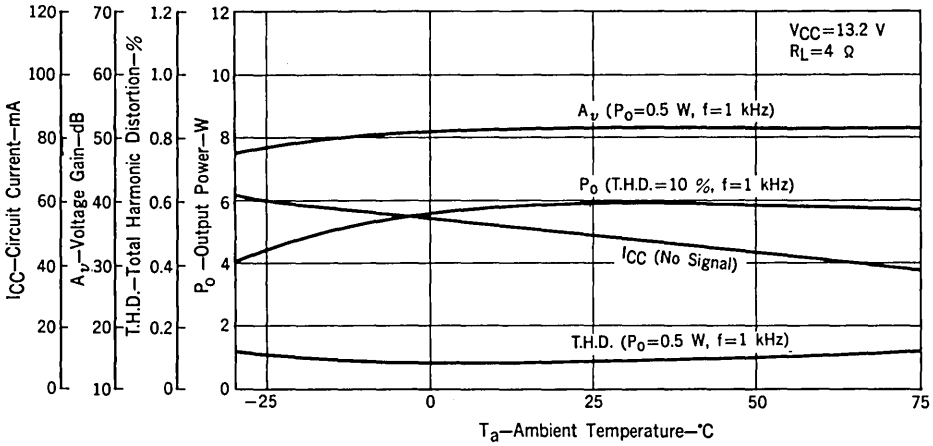
OUTPUT POWER vs.
SUPPLY VOLTAGE



SUPPLY VOLTAGE CHARACTERISTICS



TEMPERATURE CHARACTERISTICS



TYPICAL APPLICATIONS

(1) Circuit Example 1

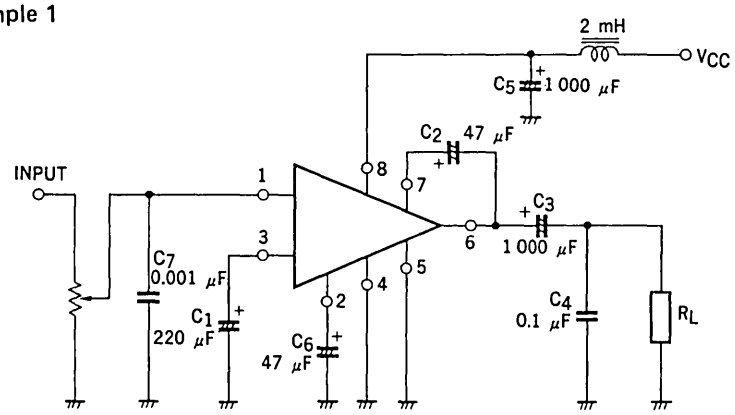


Fig. A

(2) Circuit Example 2

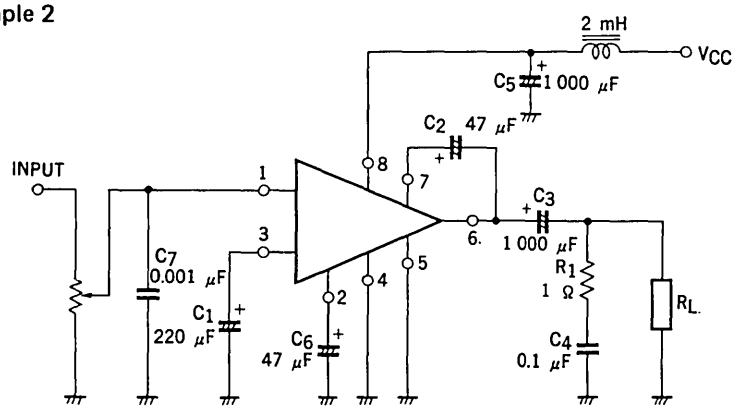
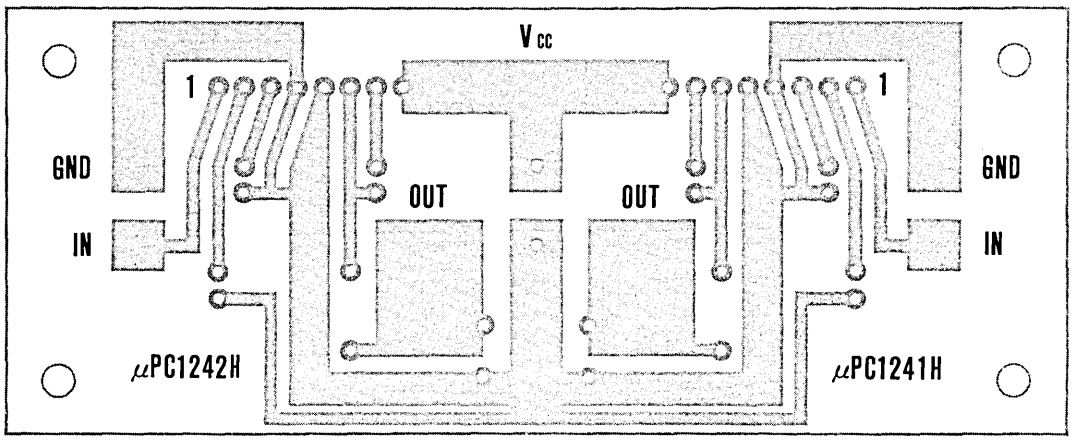


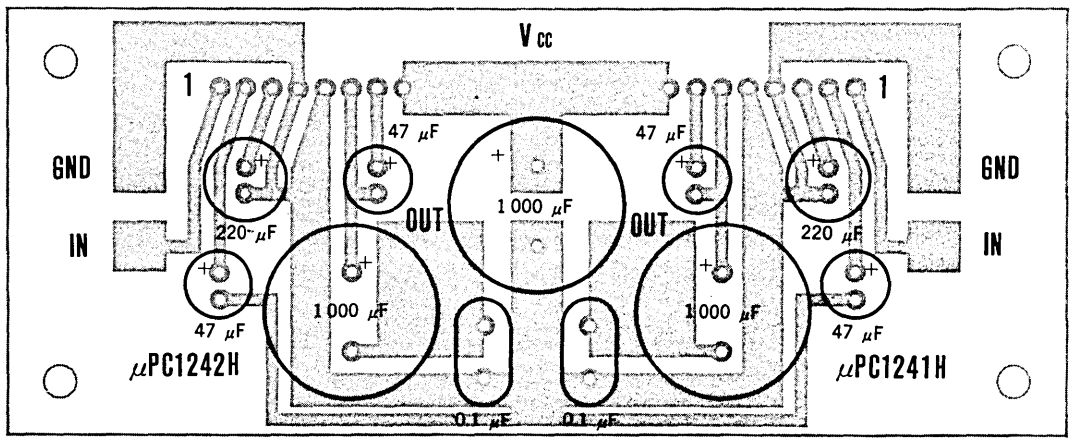
Fig. B

- The capacitor C_4 is for preventing a parasitic oscillation. A mylar film capacitor is recommended. If an oscillation occur, increase capacitance of C_4, or connect an additional resistor R_1 as shown in Fig. B.

TYPICAL PRINTED CIRCUIT BOARD PATTERN (Copper side)



COMPONENTS LAYOUT FOR P.W. ASSEMBLY (Copper side)



BIPOLAR ANALOG INTEGRATED CIRCUIT
μPC2002

5.4W AUDIO FREQUENCY POWER AMPLIFIER
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

DISCRIPTION

The μPC2002 is a silicon monolithic integrated circuit designed for use as an audio frequency power amplifier in a car radio and a car stereo.

The device is packaged in five lead plastic power package, and designed for driving low impedance loads (down to 1.6 Ω).

In addition, the device provides built-in protection against short circuit, over voltage and surge voltage of power supply.

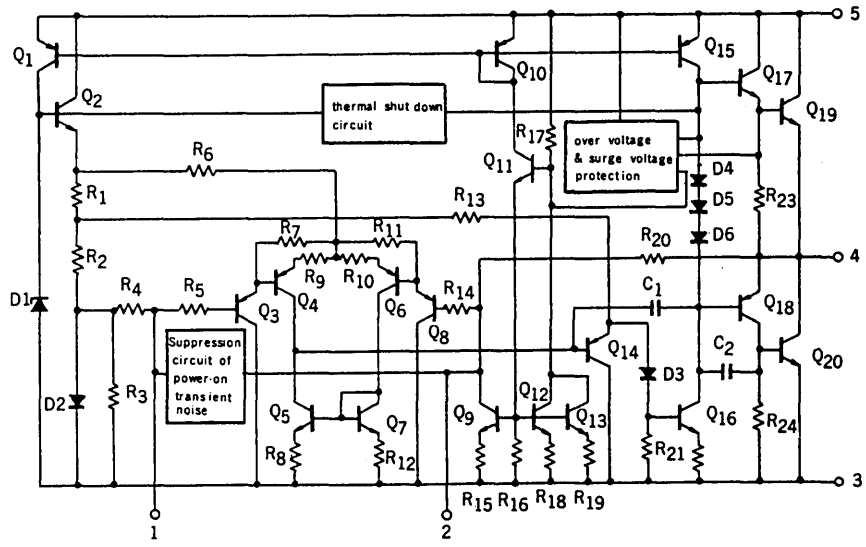
FEATURES

- High output power. :

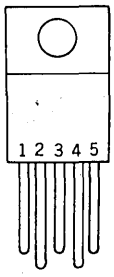
  $P_O = 5.4\,W$ (at $R_L = 4\,\Omega$), $P_O = 9.0\,W$ (at $R_L = 2\,\Omega$)
- Assembly ease and space saving.
- Low noise and low distortion. :

  $v_n = 0.6\,mV_{r.m.s.}$, T.H.D. = 0.05 %
- Low transient noise at power supply switch-on.
- Built-in over voltage and surge protection.
- Built-in short circuit protection.

EQUIVALENT CIRCUIT



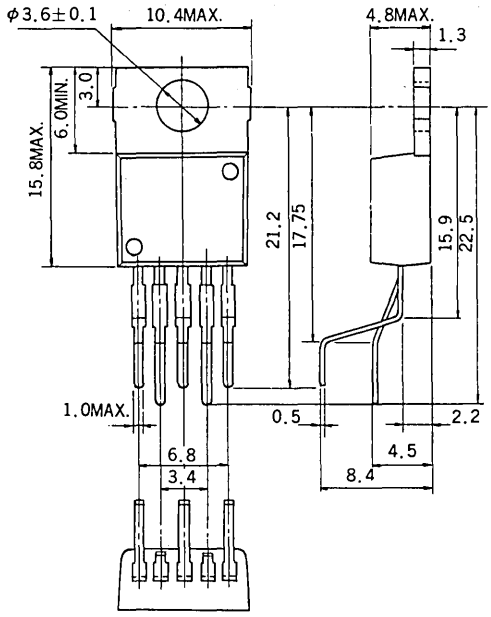
CONNECTION DIAGRAM



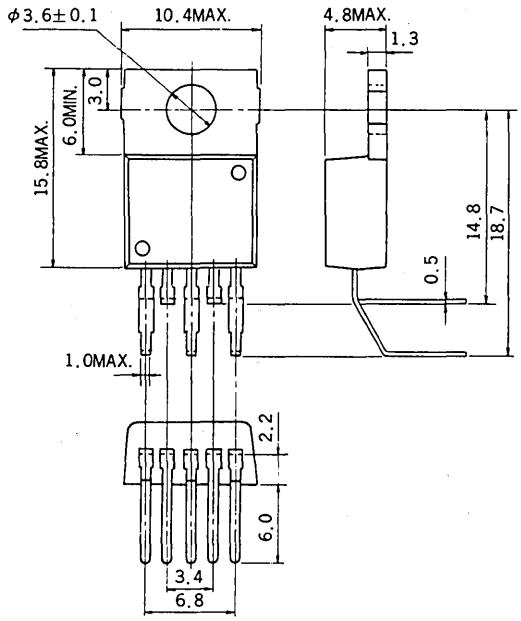
Pin No.	Electrical Connection
1	Non inverting input
2	Inverting input
3	Ground
4	Output
5	Power supply

PACKAGE DIMENSIONS (in millimeters)

μPC2002V



μPC2002H



ABSOLUTE MAXIMUM RATINGS

Peak Supply Voltage (50 ms)	V_{CC1}	40	V
DC Supply Voltage (quiescent)	V_{CC2}	28	V
DC Supply Voltage (operational)	V_{CC3}	18	V
Output Peak Current (repetitive)	$I_{CC(peak)1}$	3.5	A
Output Peak Current (non repetitive)	$I_{CC(peak)2}$	4.5	A
Package Dissipation (Tcase = 90°C)	P_D	15	W
Operating Temperature	T_{opt}	−30 to 75	°C
Storage Temperature	T_{stg}	−40 to 150	°C

THERMAL DATA

Thermal Resistance junction-case	$R_{th(j-c)}$	4	°C/W

RECOMMENDED OPERATING CONDITION (Ta = 25°C)

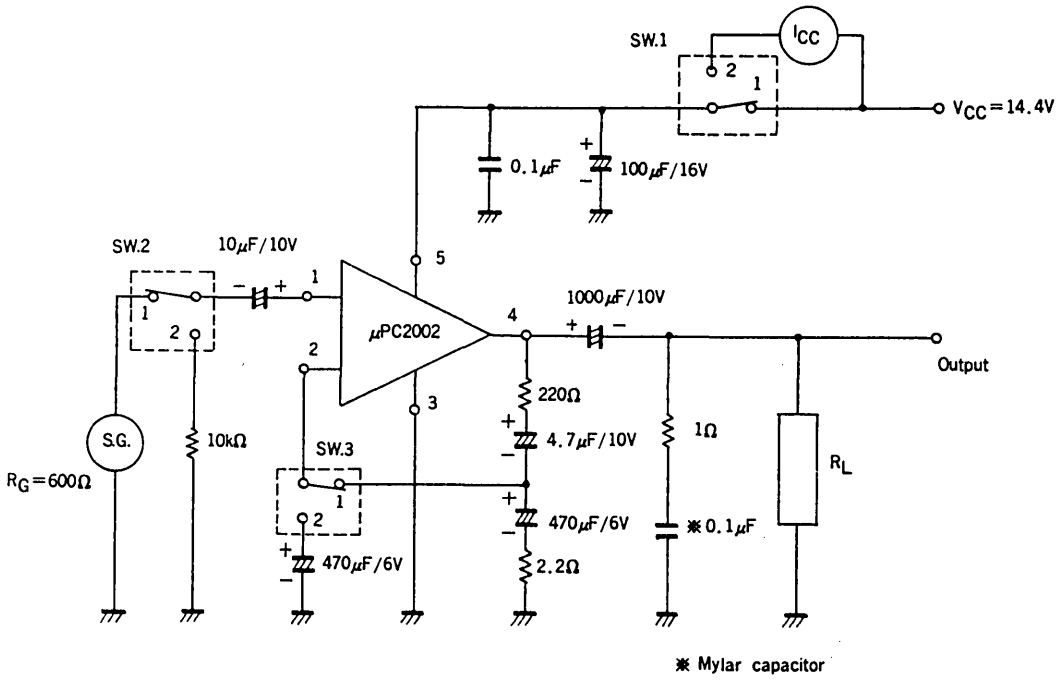
Operating Supply Voltage Range	V_{CC}	8 to 18	V

ELECTRICAL CHARACTERISTICS

(Refer to the test circuit. : Ta = 25°C, R_L = 4Ω, f = 1kHz, using an aluminum heat sink 100 x 100 x 2 mm)

CHARACTERISTIC	SYMBOL	V_{CC} = 14.4V			V_{CC} = 13.2V	UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.	TYP.		
Quiescent Current	I_{CC}	35	55	85	54	mA	v_i = 0
Output Power	Po	4.8	5.4		4.5	W	R_L = 4Ω, T.H.D. = 10%
			9.0		7.5	W	R_L = 2Ω, T.H.D. = 10%
Total Harmonic Distortion	T.H.D.		0.05	1.0	0.05	%	R_L = 4Ω, Po = 0.5W
			0.06	1.0	0.06	%	R_L = 2Ω, Po = 1.0W
Open Loop Voltage Gain	A_{vo}		78		78	dB	Po = 0.5W
Closed Loop Voltage Gain	A_v	39.5	40	40.5	40	dB	Po = 0.5W
Output Noise Voltage	v_n		0.6	3.0	0.6	mVr.m.s.	R_G = 10kΩ
Input Resistance	R_i	70	150		150	kΩ	
Supply Voltage Rejection Ratio	SVR	30	39		39	dB	R_G = 10kΩ v_{ripple} = 0.5V f_{ripple} = 100Hz

TEST CIRCUIT

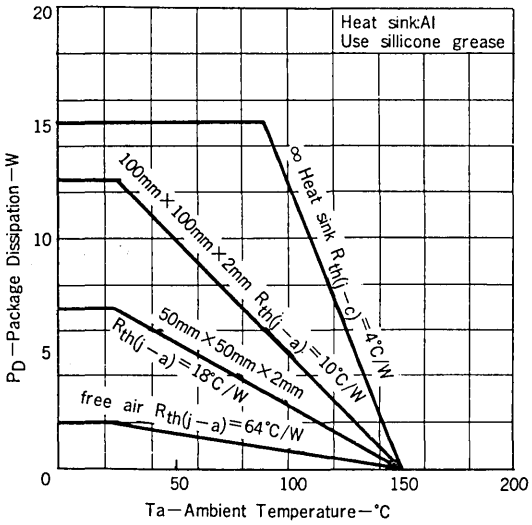


Switch position

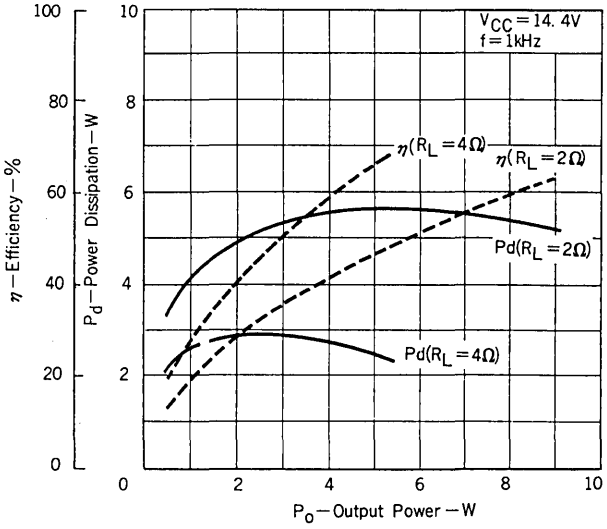
Item / SW.	I_{CC}	Po	T.H.D.	A_{vo}	A_v	v_n	SVR
SW.1	2	1	1	1	1	1	1
SW.2	2	1	1	1	1	2	2
SW.3	1	1	1	2	1	1	1

TYPICAL CHARACTERISTICS (Ta = 25°C)

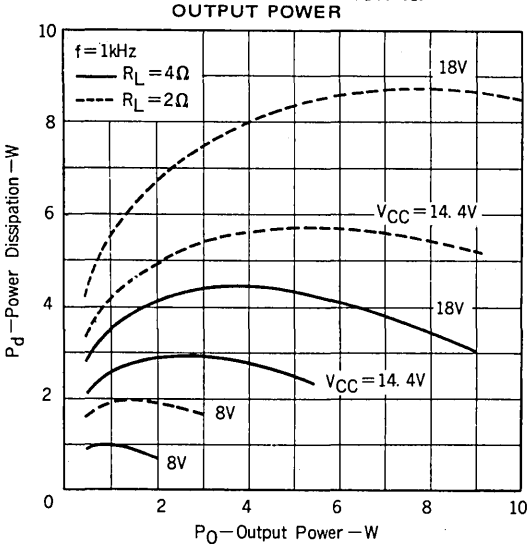
PACKAGE DISSIPATION vs. AMBIENT TEMPERATURE



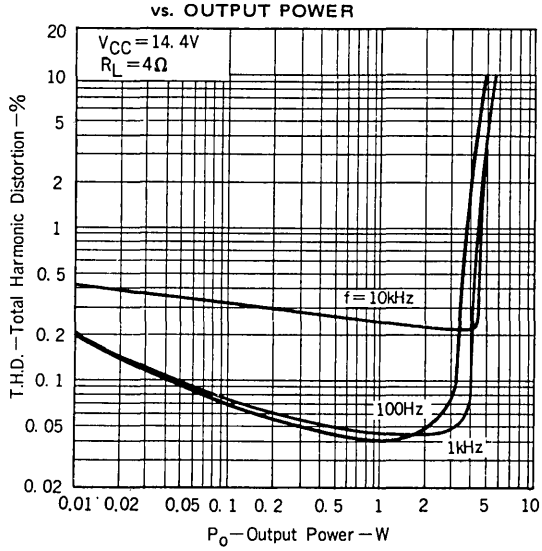
POWER DISSIPATION AND EFFICIENCY vs. OUTPUT POWER



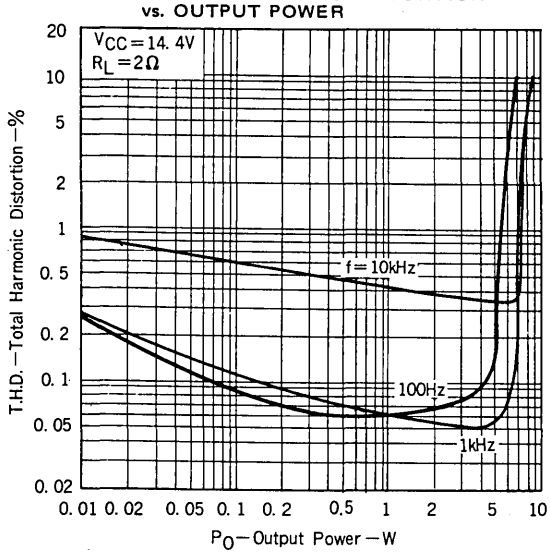
POWER DISSIPATION vs. OUTPUT POWER



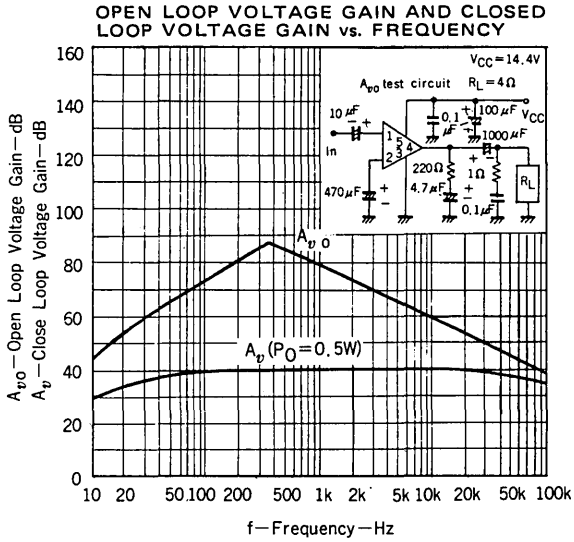
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



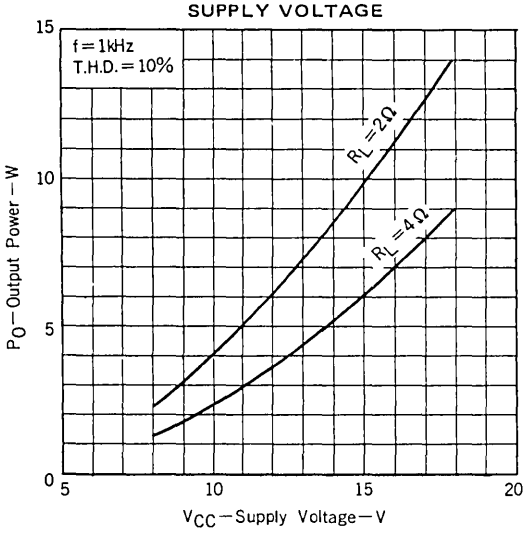
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



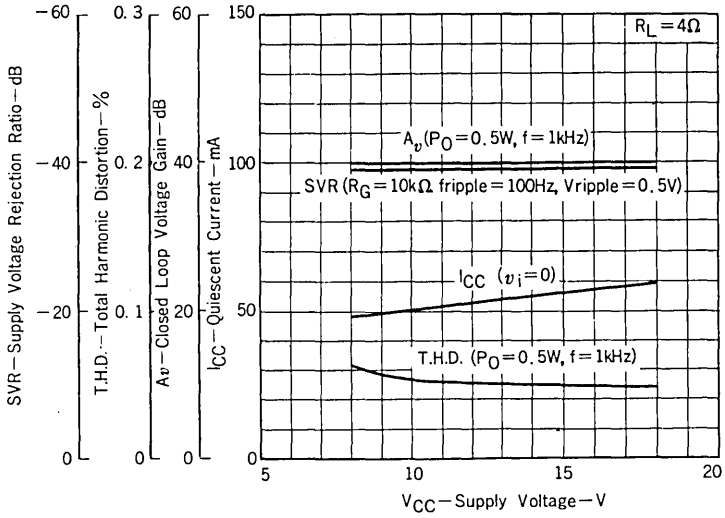
OPEN LOOP VOLTAGE GAIN AND CLOSED LOOP VOLTAGE GAIN vs. FREQUENCY



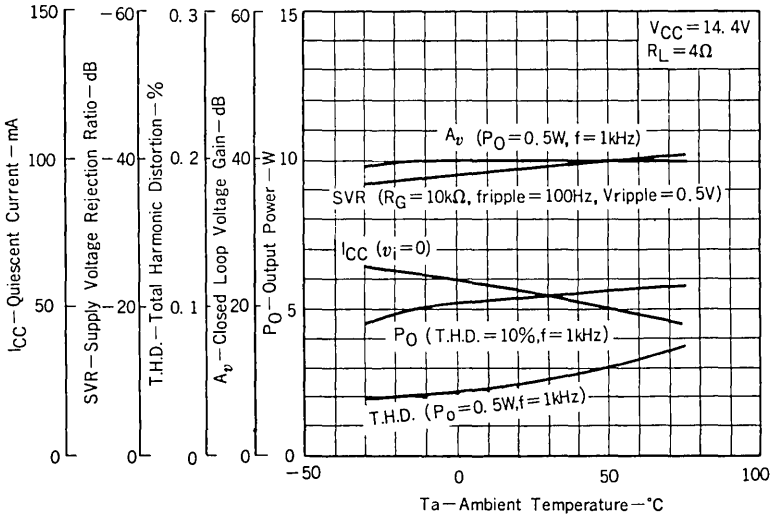
OUTPUT POWER vs. SUPPLY VOLTAGE



QUIESCENT CURRENT, CLOSED LOOP VOLTAGE GAIN, TOTAL HARMONIC DISTORTION AND SUPPLY VOLTAGE REJECTION RATIO vs. SUPPLY VOLTAGE

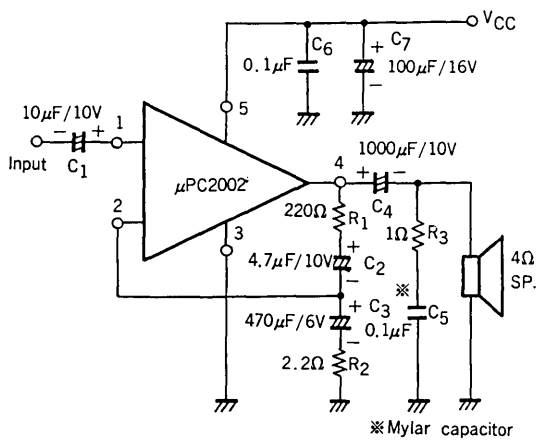


OUTPUT POWER, CLOSED LOOP VOLTAGE GAIN, TOTAL HARMONIC DISTORTION, SUPPLY VOLTAGE REJECTION RATIO AND QUIESCENT CURRENT vs. AMBIENT TEMPERATURE

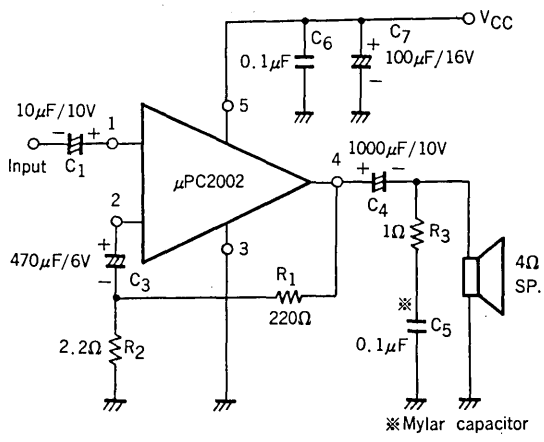


TYPICAL APPLICATIONS

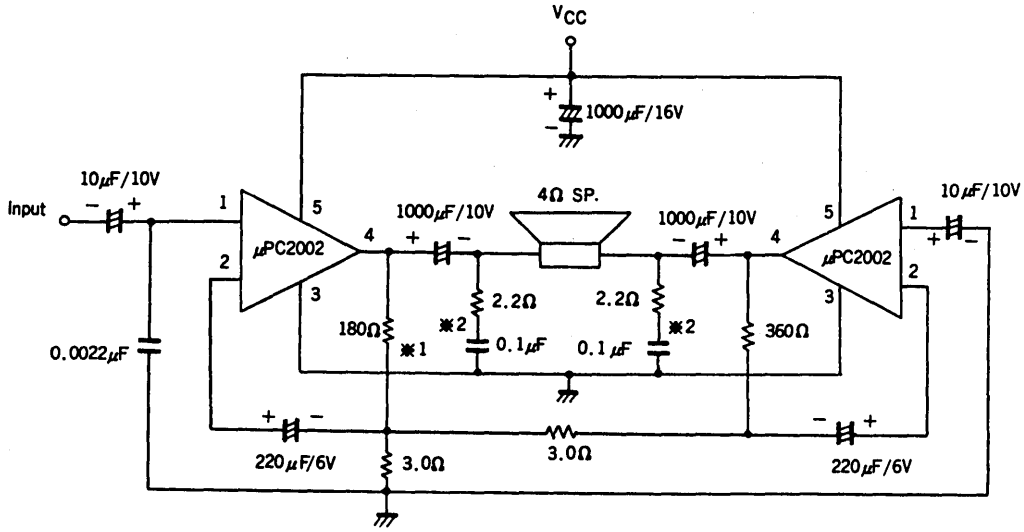
Circuit example 1.



Circuit example 2.



Circuit example 3. (Bridge configuration)

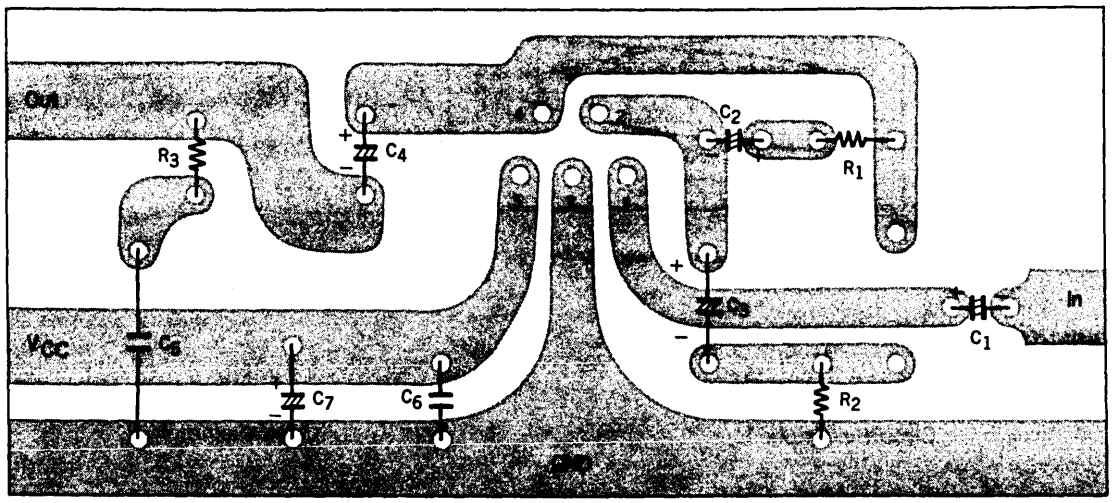


※1 : $\frac{1}{2}$W

※2 : Mylar capacitor

Typical printed circuit board and components layout for the circuit of example 1 and 2.

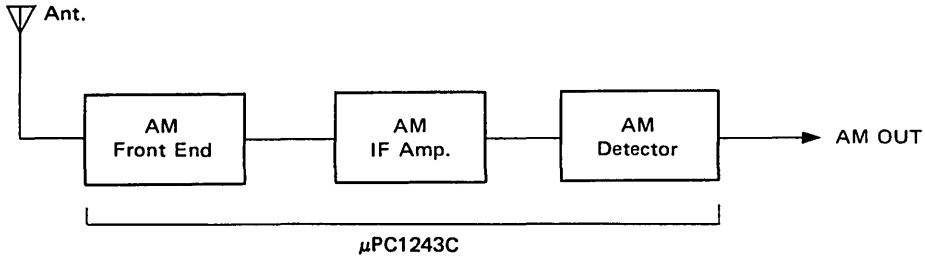
Bottom View



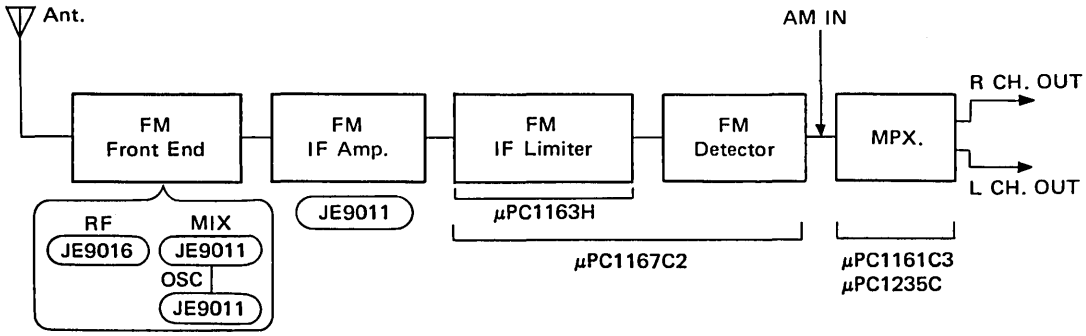
INDEX

BLOCK DIAGRAM

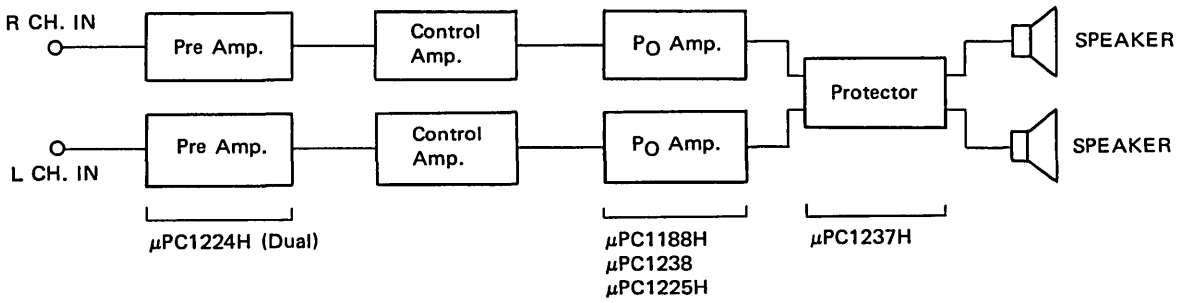
AM Block



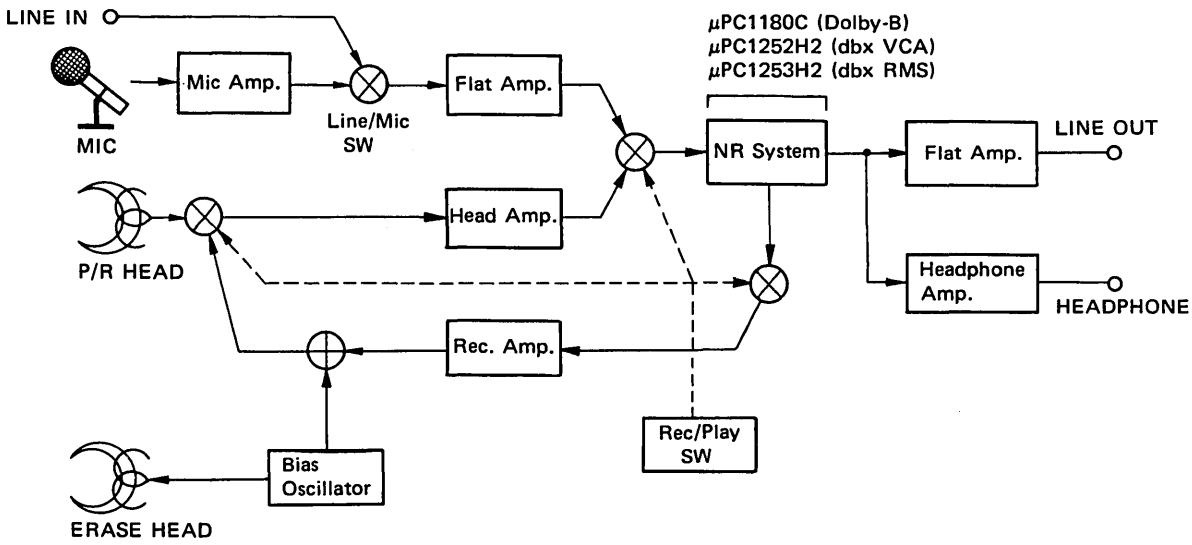
FM Block



AF Block



TAPE DECK BLOCK



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1243C

AM TUNER

SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

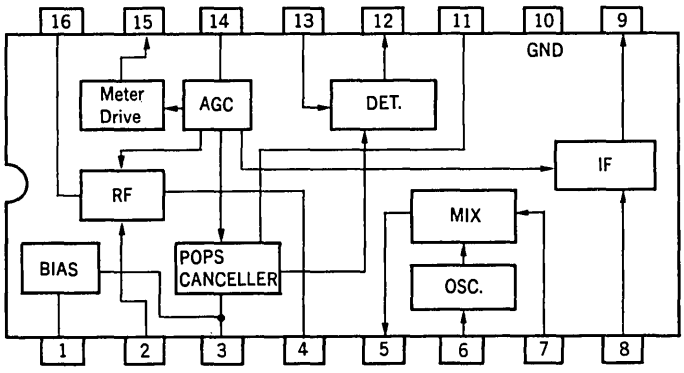
DESCRIPTION

μPC1243C is a silicon monolithic integrated circuit designed for AM tuner and the most suitable for high class tuner.
It is composed of an RF amplifier, a mixer, a local oscilator, an IF amplifier, a detector, a turn on and turn off pops canceller, an AGC amplifier and a signal meter driver.
Package is the 16 lead Dual In-Line Plastic Package (DIP).

FEATURES

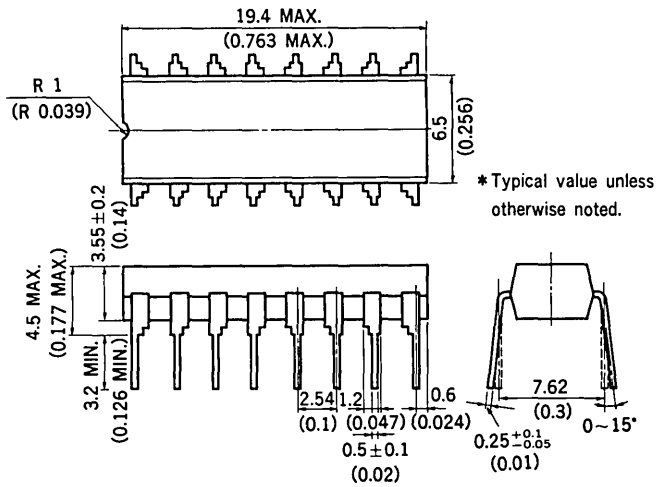
- Internally turn on and turn off pops canceller.
  The pop level is one eighth that of NEC's conventional circuit.
- High signal to noise ratio.
  S/N = 57 dB TYP. (V_{in} = 100 dB/m, f_{MOD} = 400 Hz, MOD = 30 %)
- Low harmonic distortion in wide range of input level.
  T.H.D. = 0.3 % TYP. (V_{in} = 100 dB/m, f_{MOD} = 400 Hz, MOD = 30 %)
  T.H.D. = 0.9 % TYP. (V_{in} = 130 dB/m, f_{MOD} = 400 Hz, MOD = 80 %)
- A three-stage delay-type AGC.
- High tweet ratio.
  Tweet ratio = 22 dB TYP. (V_{in} = 60 dB/m, 2 IF)
- High usable sensitivity.
  U.S. = 46 dB/m TYP. (f = 1 MHz, S/N = 20 dB)
- Signal meter driver provides excellent linearty.
  Driving current = 500 μA MAX.

CONNECTION DIAGRAM (Top View)



PACKAGE DIMENSIONS

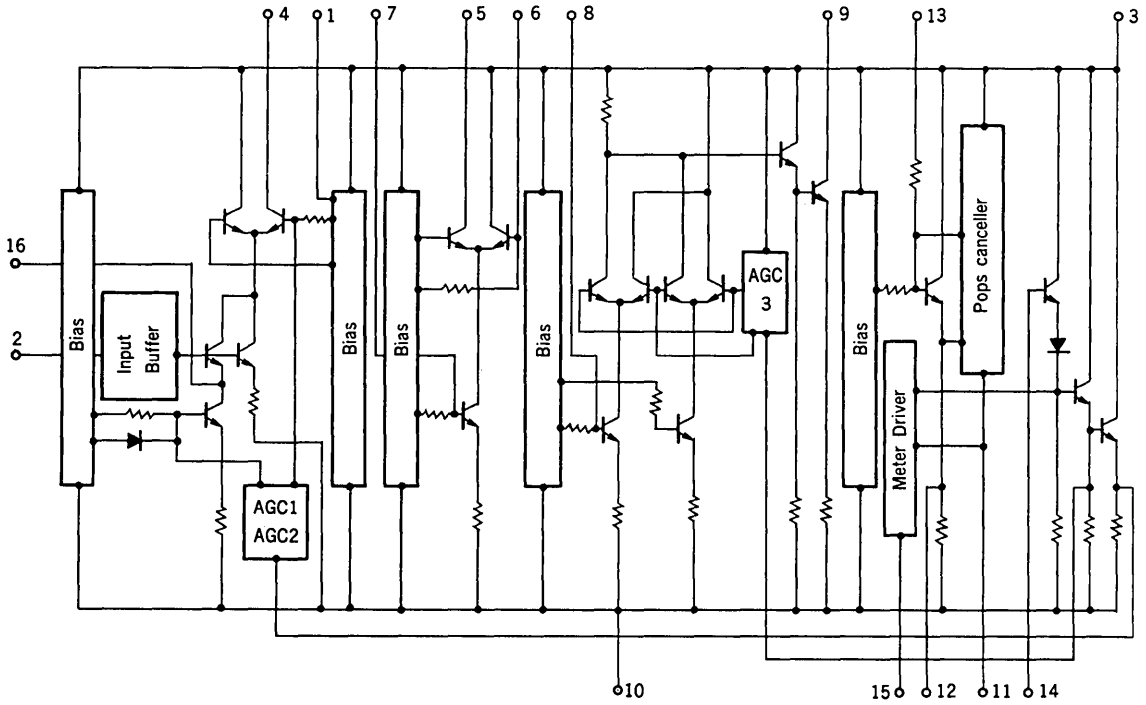
in millimeters (inches)



CONNECTIONS

Pin No.	Connection	Pin No.	Connection
1	Bias	9	IF output
2	RF input	10	GND
3	V_{CC}	11	Timing condenser
4	RF output	12	DET. output
5	MIX output	13	DET. input
6	Local osc.	14	AGC input
7	MIX input	15	Signal meter
8	IF input	16	Bypass

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Supply Voltage	V_{CC}	15	V	
Input Voltage	V_{in}	7	V_{p-p}	
Power Dissipation	P_D	350	mW	(Ta = 75 °C)
Operating Temperature	T_{opt}	−20 to +75	°C	
Storage Temperature	T_{stg}	−40 to +125	°C	

RECOMMENDED OPERATING CONDITION (Ta = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	9	12	15	V

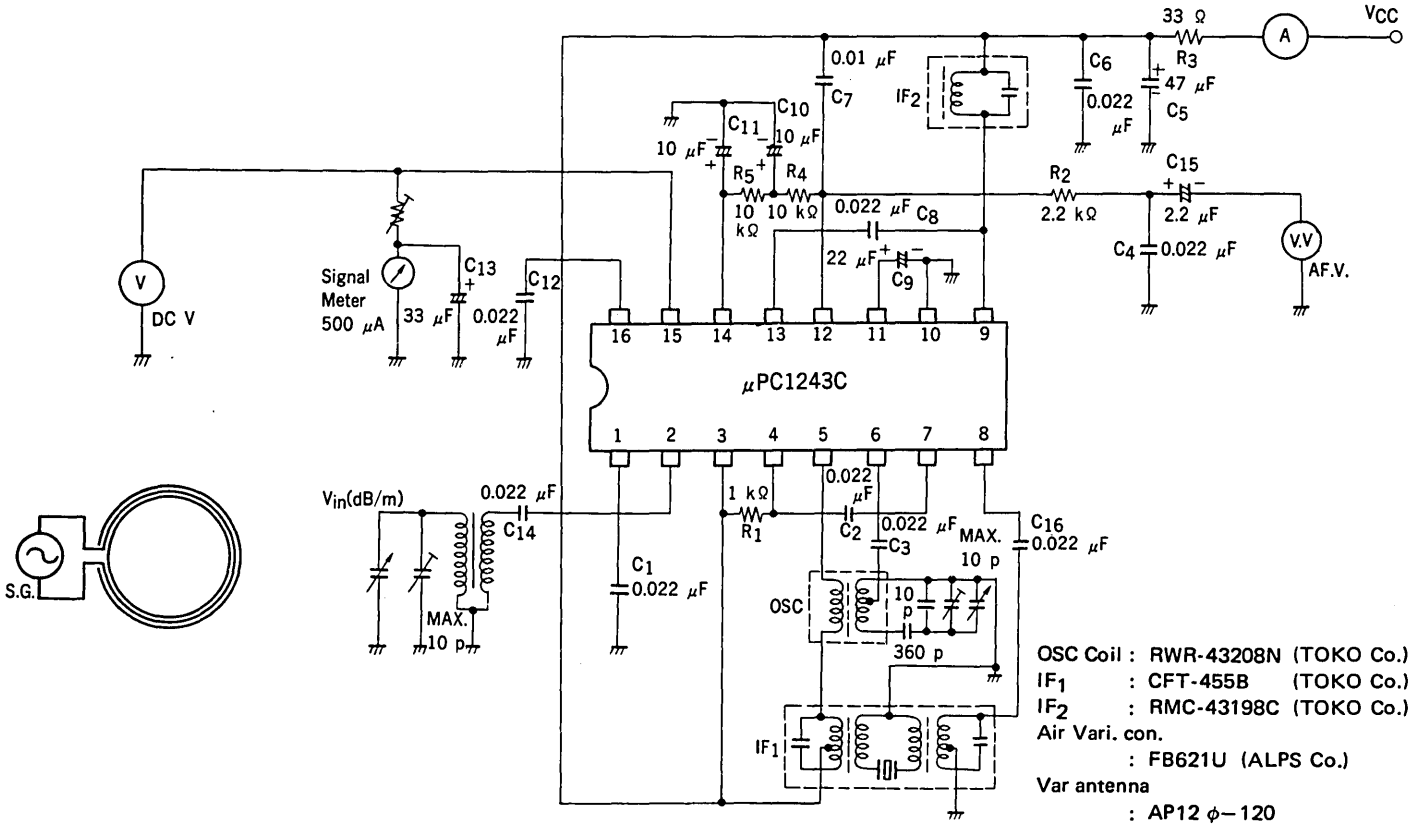
ELECTRICAL CHARACTERISTICS (Ta = 25 °C, V_{CC} = 12 V, f_{MOD} = 400 Hz, f = 1 MHz, MOD = 30 %)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Supply Current	I_{CC}	10	14.5	21	mA	V_{in} = 0
Usable Sensitivity	U. Sens	–	46	–	dB/m	S/N = 20 dB
Derector Output	V_o	120	180	240	mVr.m.s.	V_{in} = 100 dB/m
Harmonic Distortion	T.H.D. 1	–	0.3	0.8	%	V_{in} = 100 dB/m
Harmonic Distortion	T.H.D. 2	–	0.9	–	%	V_{in} = 130 dB/m, MOD = 80 %
AGC FOM	FOM	75	83	–	dB	−10 dB point
Signal to Noise Ratio	S/N	50	57	–	dB	V_{in} = 100 dB/m
Max. Sensitivity	M.S.	31	38	45	dB/m	V_o = 30 mVr.m.s.

CHARACTERISTICS FOR REFERENCE (Ta = 25 °C, V_{CC} = 12.0 V)

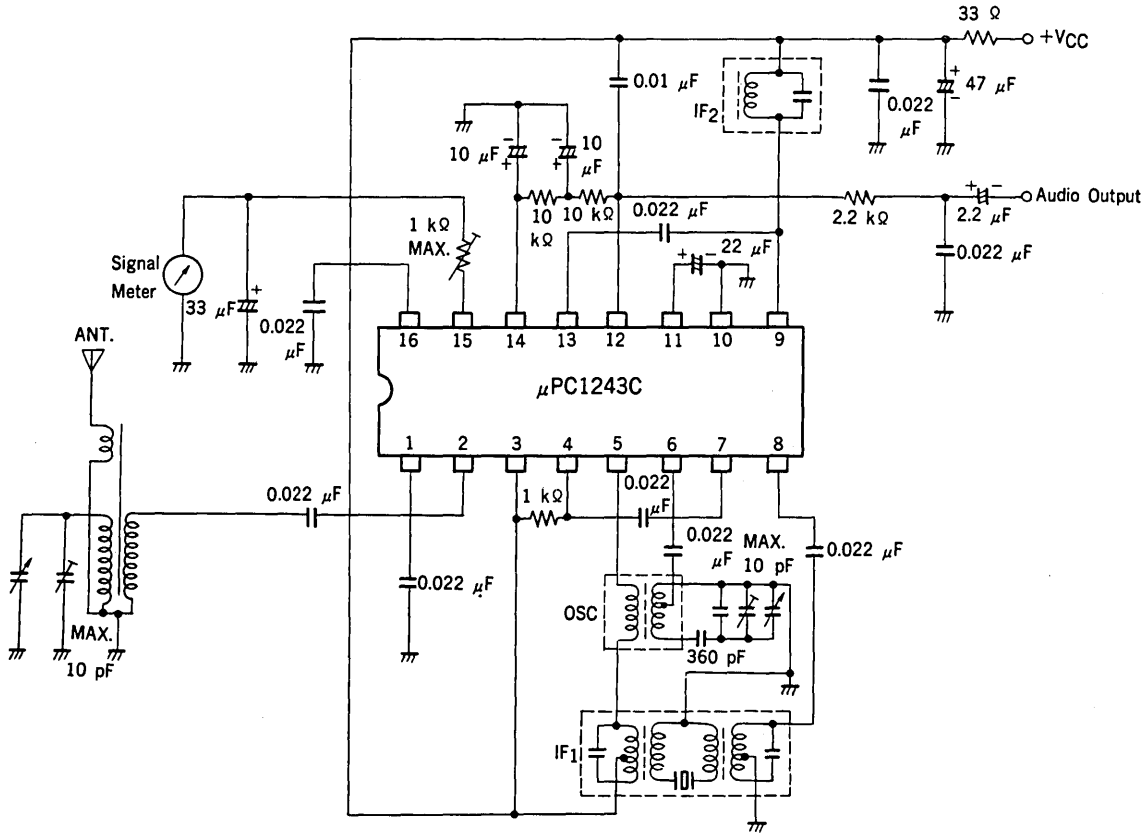
CHARACTERISTIC	TEST CONDITION	TYP.	UNIT
IF Response Ratio	f = 1 MHz, V_o = 50 mVr.m.s., IF = 455 kHz	42	dB
Image Response Ratio	f = 1 MHz, V_o = 50 mVr.m.s., f + 2 IF	60	dB
Selectivity	f = 1 MHz, Δf = ±10 kHz	30	dB
Tweet Ratio	V_i = 60 dB/m, 2 IF = 910 kHz	22	dB
	V_i = 100 dB/m, 3 IF = 1 365 kHz	48	dB
RF Input Impedance	f = 1 MHz	5.5	kΩ
RF Input Capacitance	f = 1 MHz	5	pF
RF Output Impedance	f = 1 MHz	80	kΩ
RF Output Capacitance	f = 1 MHz	2	pF
MIX Input Impedance	f = 1 MHz	8	kΩ
MIX Input Capacitance	f = 1 MHz	5	pF
MIX Output Impedance	f = 1 MHz	80	kΩ
MIX Output Capacitance	f = 1 MHz	2	pF
IF Input Impedance	f = 455 kHz	3.3	kΩ
IF Input Capacitance	f = 455 kHz	10	pF
IF Output Impedance	f = 455 kHz	80	kΩ
IF Output Capacitance	f = 455 kHz	2	pF
Det. Input Impedance	f = 455 kHz	6.5	kΩ
Det. Input Capacitance	f = 455 kHz	5	pF

TEST CIRCUIT (Top view)



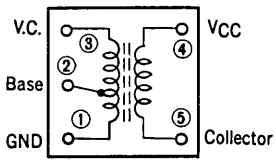
OSC Coil : RWR-43208N (TOKO Co.)
IF_1 : CFT-455B (TOKO Co.)
IF_2 : RMC-43198C (TOKO Co.)
Air Vari. con.
: FB621U (ALPS Co.)
Var antenna
: AP12 ϕ–120

APPLICATION CIRCUIT (Top view)



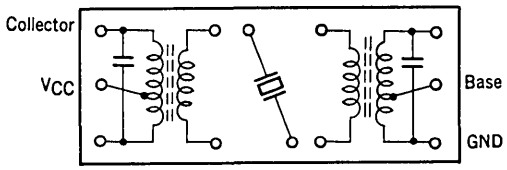
COIL SPECIFICATION (Bottom view)

(1) OSC Coil RWR-43208N (TOKO Co.)



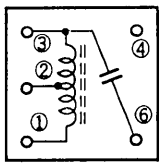
Qu = 110 ~ (796 kHz)
①~② ②~③ ④~⑥
4T 58T 10T
L = 160 μH ±6 %

(2) IFT_1 (IF transformer) CFT455B (TOKO Co.)



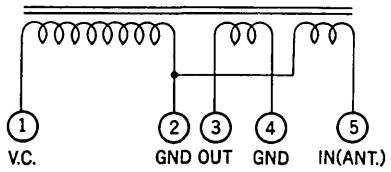
Centre freq. 455 kHz ±3.5 kHz
Selectivity ±10 kHz 26 dB Mini.

(3) IFT_2 (IF transformer) RMC-43198C (TOKO Co.)



Centre freq. 455 kHz
180 pF (Included)
Qu = 80 ~ (455 kHz)
①~③
164T

(4) Bar antenna AR12ϕ−120 (Coil Snake Co.)

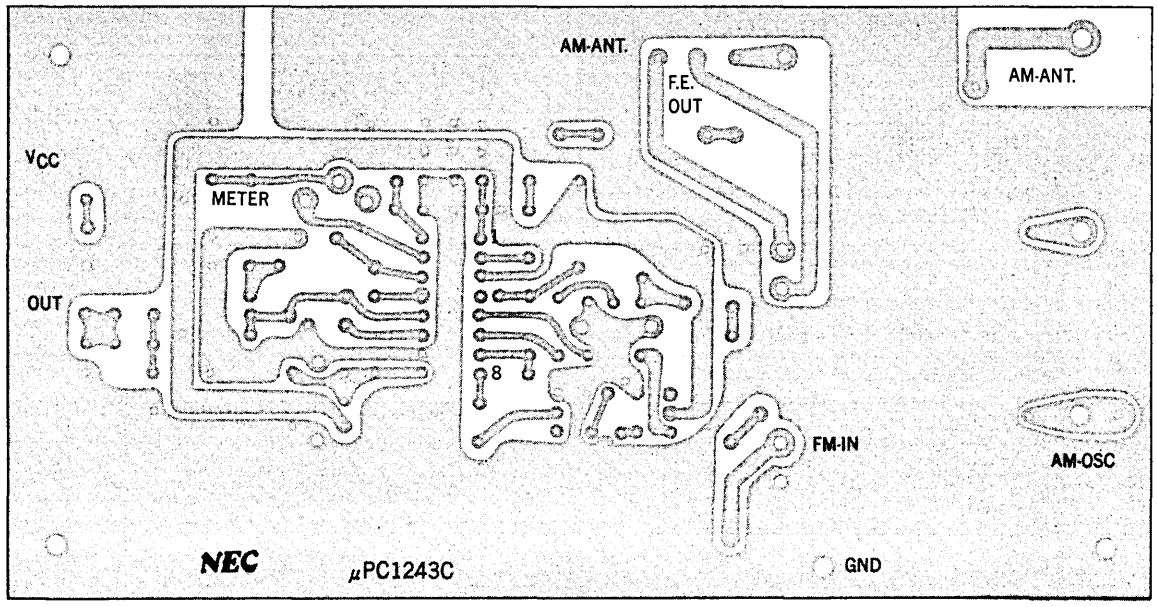


①~② ③~④ ②~⑤
58T 6T 5T

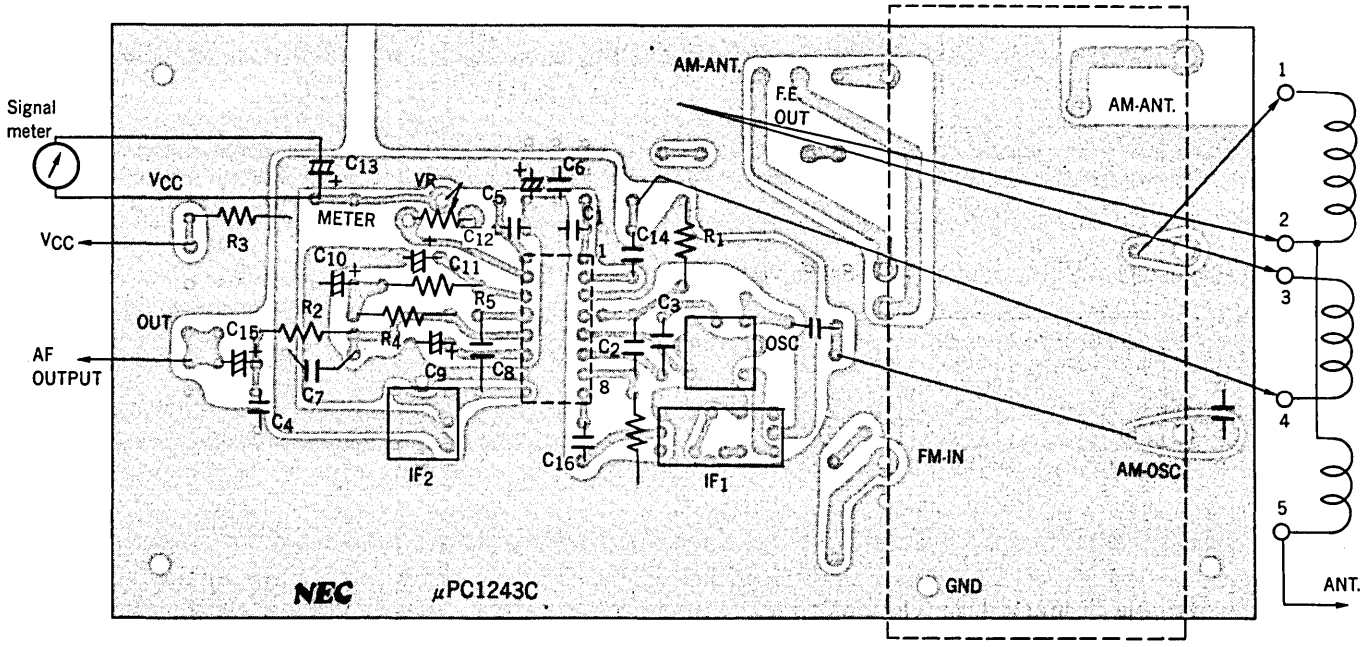
(5) Air variable FB621U (Alps Electric Co.)
Capacitor

$C_{MAX.}$ = 326 pF
$C_{MIN.}$ = 9 pF

EXAMPLE FOR PRINTED CIRCUIT BOARD



COMPONENT LAYOUT

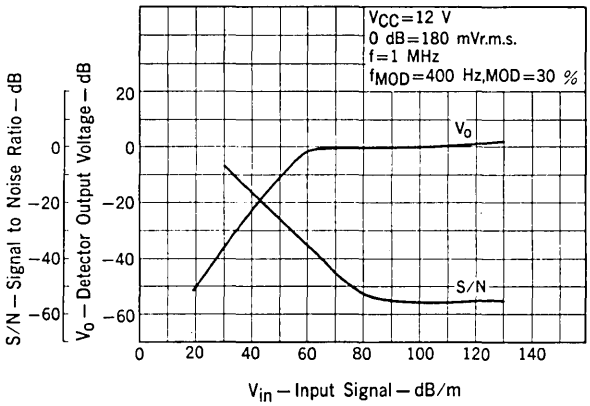


R_1 : 1kΩ
R_2 : 2.2 kΩ
R_3 : 33 Ω
R_4 : 10 kΩ
R_5 : 10 kΩ

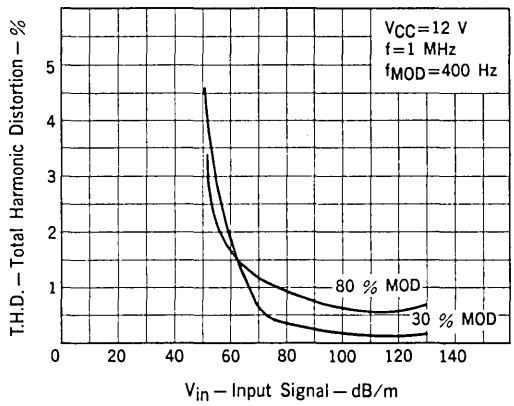
C_1 : 0.022 μF Ceramic
C_2 : 0.022 μF Ceramic
C_3 : 0.022 μF Ceramic
C_4 : 0.022 μF Ceramic
C_5 : 47 μF Chemical
C_6 : 0.022 μF Ceramic
C_7 : 0.01 μF Ceramic
C_8 : 0.022 μF Ceramic
C_9 : 22 μF Chemical
C_{10} : 10 μF Chemical
C_{11} : 10 μF Chemical
C_{12} : 0.022 μF Ceramic
C_{13} : 33 μF Chemical
C_{14} : 0.022 μF Ceramic
C_{15} : 2.2 μF Chemical
C_{16} : 0.022 μF Ceramic

VR : 1 kΩ MAX.
OSC COIL : RWR-43208N
IF_1 : CFT-455B
IF_2 : RMC-43198C
ANT.CO. : AR12 φ– 120
Air vari. con. : FB621U
Signal meter : 500 μA MAX.

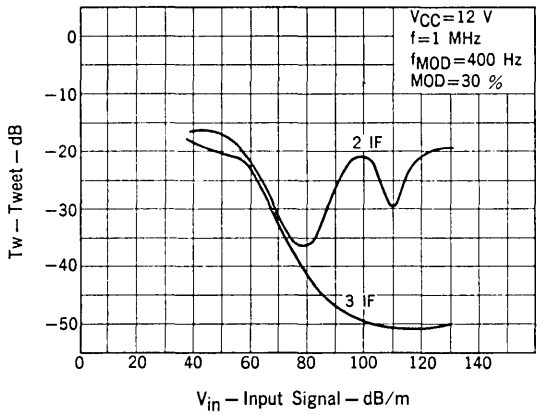
DETECTOR OUTPUT VOLTAGE AND SIGNAL TO NOISE RATIO vs. INPUT SIGNAL



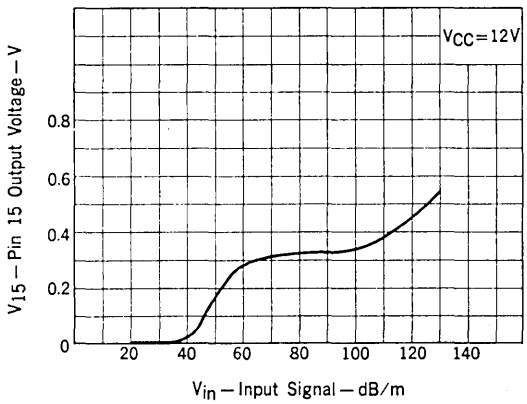
TOTAL HARMONIC DISTORTION vs. INPUT SIGNAL



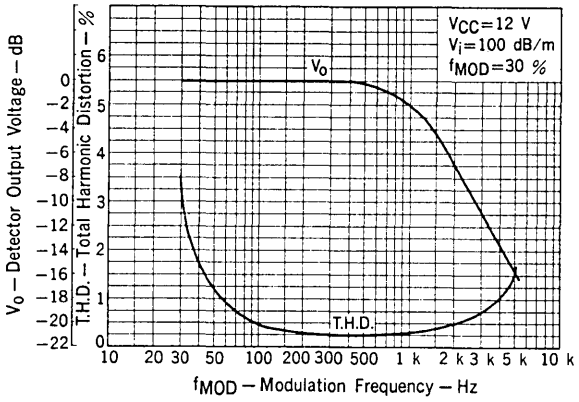
TWEET vs. INPUT SIGNAL



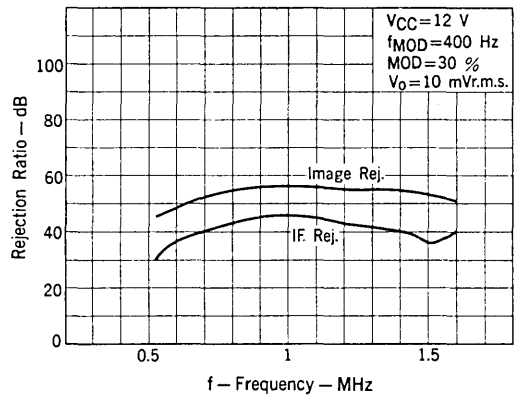
PIN 15 OUTPUT VOLTAGE vs. INPUT SIGNAL



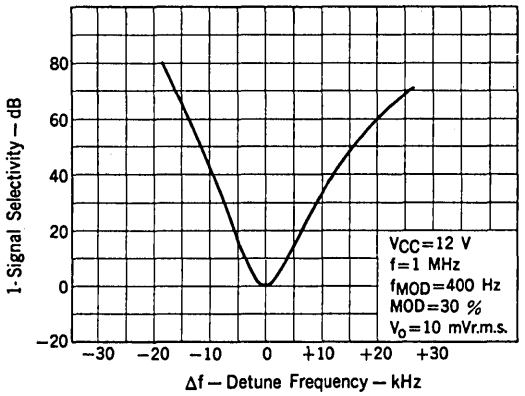
DETECTOR OUTPUT VOLTAGE AND TOTAL HARMONIC DISTORTION vs. MODULATION FREQUENCY



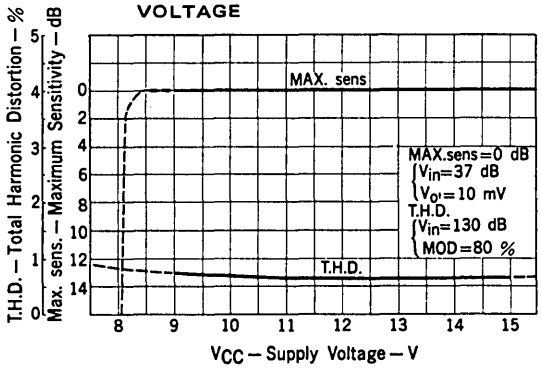
IF REJECTION AND IMAGE REJECTION vs. FREQUENCY



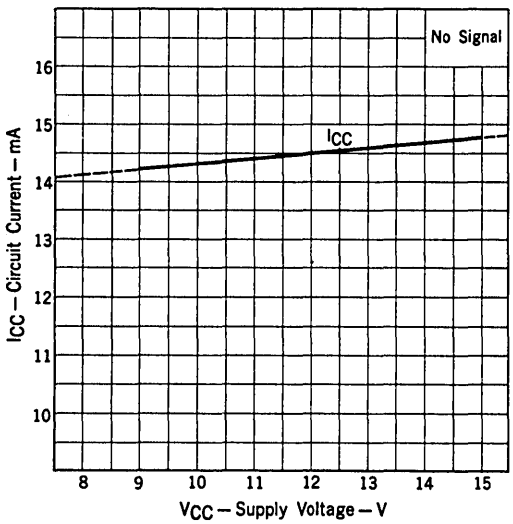
ONE-SIGNAL SELECTIVITY vs. DETUNE FREQUENCY



MAXIMUM SENSITIVITY AND TOTAL HARMONIC DISTORTION vs. SUPPLY VOLTAGE



CIRCUIT CURRENT vs. SUPPLY VOLTAGE



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1163H

FM IF AMPLIFIER
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

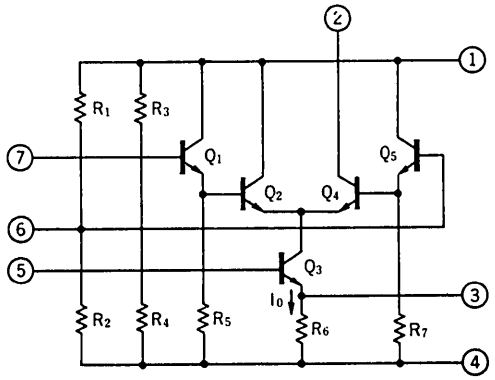
DESCRIPTION

The μPC1163H is a semiconductor integrated circuit for FM-IF amplification, and contains a emitter followered differential amplifying stage and a constant current source. The limiting characteristics for AM signals of the μPC1163H are excellent, and since it has been designed to minimize distortion at high level inputs, it is most suitable for use in high class FM-IF amplifiers.

FEATURES

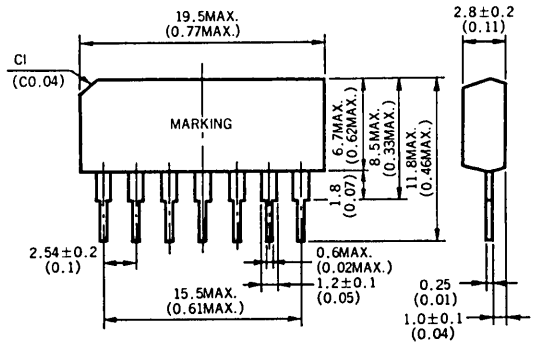
- The distortion characteristics at high level inputs are excellent.
- The group delay characteristics of the FM-IF circuit have minimum disparity.
- A terminal for varying the constant current is provided, enabling I_O to be varied from 4.5mA to 15mA. This makes possible its employment as a driver for ratio detector.
- Very few external components are required.
- High stability for parasitic oscillation.
- Capability for cascade connection.
- Wide range of supply voltage: 10V to 15V

EQUIVALENT CIRCUIT

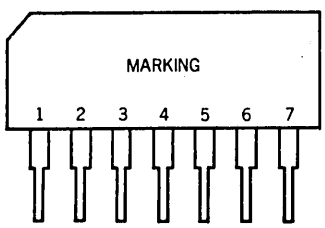


PACKAGE DIMENSIONS

in millimeters (inches)



CONNECTION DIAGRAM



Pin No.	Electrical Connection
1	V_{CC}
2	OUTPUT
3	BYPASS
4	GND
5	BYPASS
6	INPUT BIAS
7	INPUT

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Supply Voltage	V_{CC}	15	V
Output Collector Voltage	V_z	20	V
Voltage Between Input Terminals	V_i	5	Vp-p
Power Dissipation	P_d	270 (Ta = 75°C)	mW
Operating Temperature	T_{opt}	-20 to +75	°C
Storage Temperature	T_{stg}	-40 to +125	°C

RECOMMENDED OPERATING CONDITIONS (Ta = 25°C)

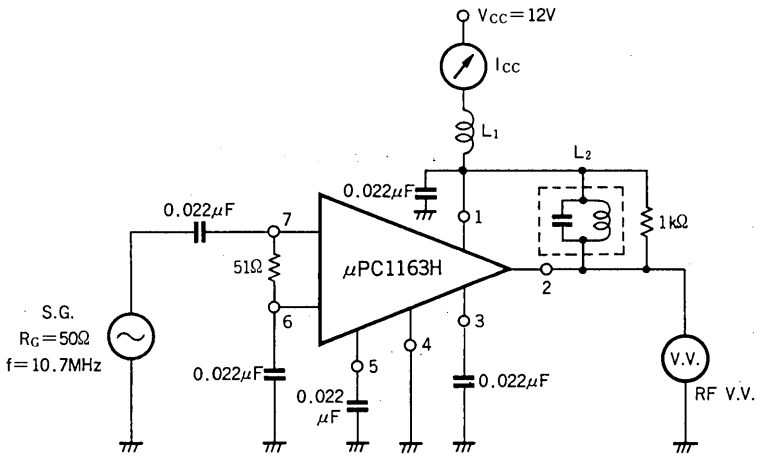
Supply Voltage	V_{CC}	10 ~ 12 ~ 15	V

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{CC} = 12 V, f = 10.7 MHz)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Current	I_{CC}	6.0	8.6	13.0	mA	V_i = 0
Output Current	I_C	1.5	2.1	3.2	mA	V_i = 0, 1 pin Current
Voltage Gain	A_V	26.5	30.0	33.5	dB	V_i = 20 mA, R_1 = 1 kΩ
Input Capacitance	C_{in}		3.0		pF	V_i = 30 mV
Input Conductance	g_{in}		0.01		m℧	V_i = 30 mV
Output Capacitance	C_o		3.4		pF	V_i = 100 mV
Output Conductance	g_o		0.035		m℧	V_i = 100 mV
Forward Transfer Admittance	$\|Y_f\|$		36.6		m℧	V_i = 100 mV
Reverse Transfer Admittance	$\|Y_r\|$		0.0038		m℧	V_i = 100 mV

TEST CIRCUIT

- I_{CC}, A_V

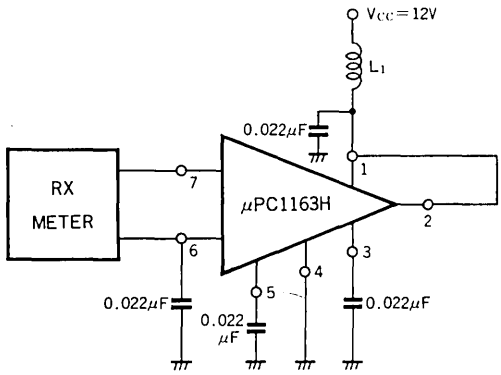


L1 { L = 1 μH; $Q_O \geqq 50$; $R_S \leqq 0.5\ \Omega$; Self-Resonance Frequency ≧ 18 MHz

L2 { $Q_O \geqq 100$; Internal Capacitance = 82 pF; f_O = 10.7 MHz ± 3 %

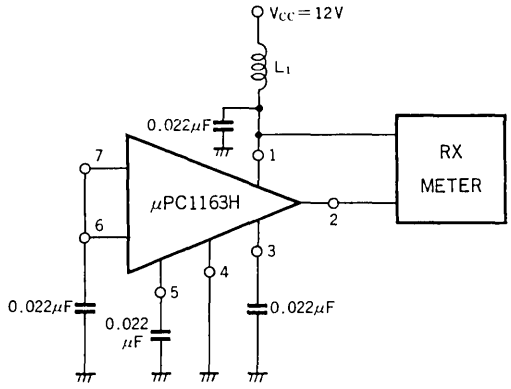
RF V.V PM = 30 dB (TOA)

● g_{in}, C_{in}



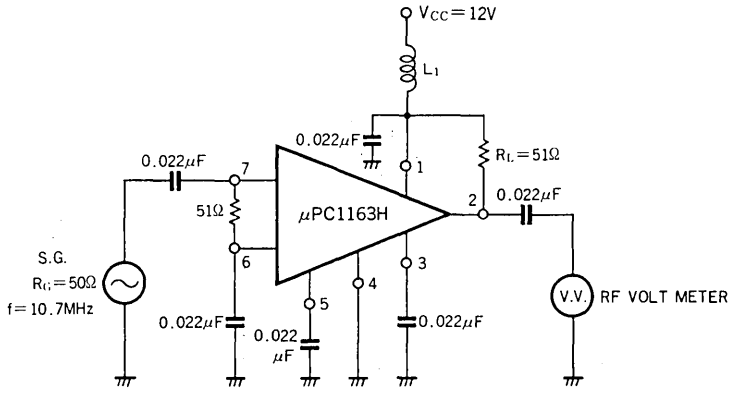
RX METER
TYPE 250-A (BOONTON)

● g_o, C_o



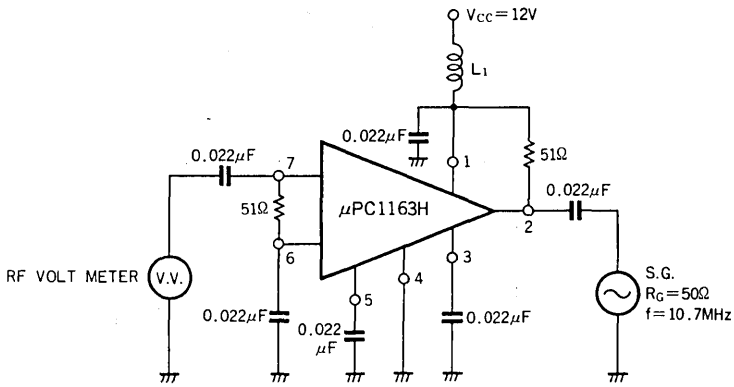
RX METER
TYPE 250-A (BOONTON)

● Y_f



RF VOLT METER
8405A (YHP)

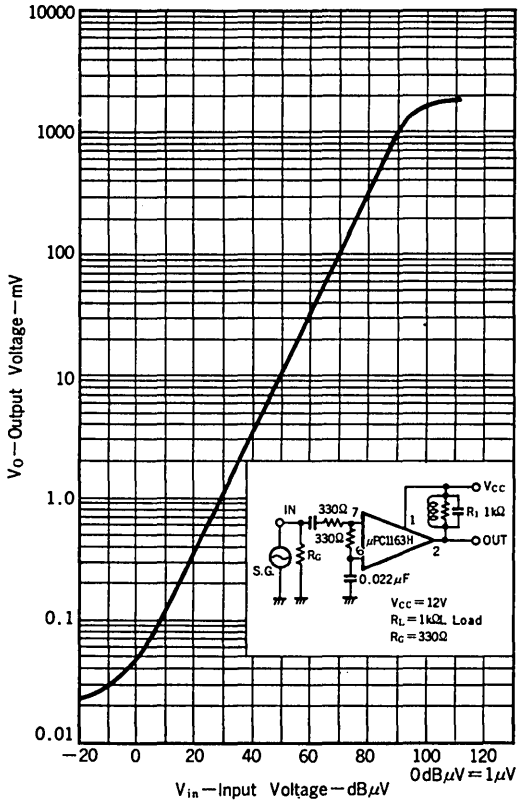
● Y_r



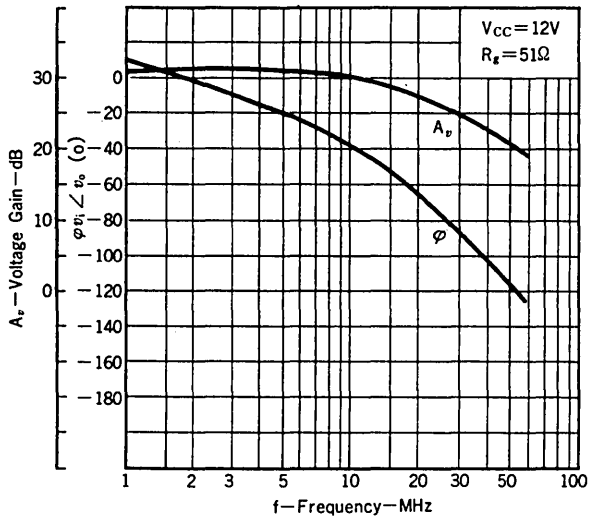
RF VOLT METER
8405A (YHP)

TYPICAL CHARACTERISTICS (Ta = 25°C)

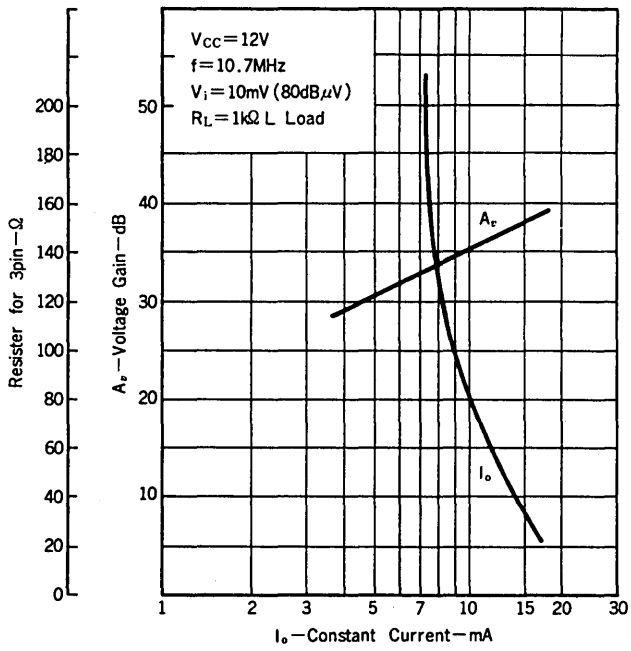
OUTPUT VOLTAGE vs. INPUT VOLTAGE
(Measure in Differential Circuit)



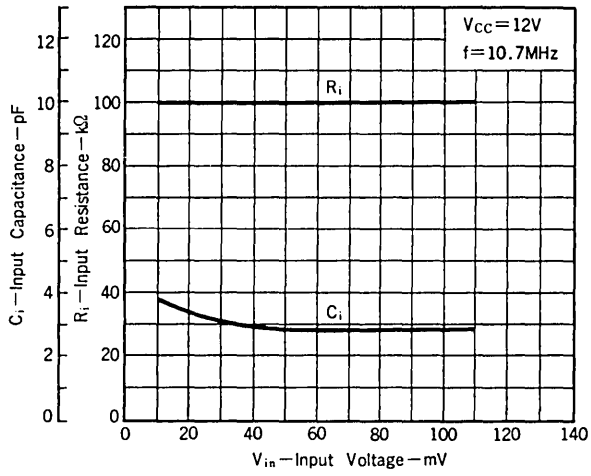
VOLTAGE GAIN, PHASE vs. FREQUENCY
(Measure in Differential Circuit)



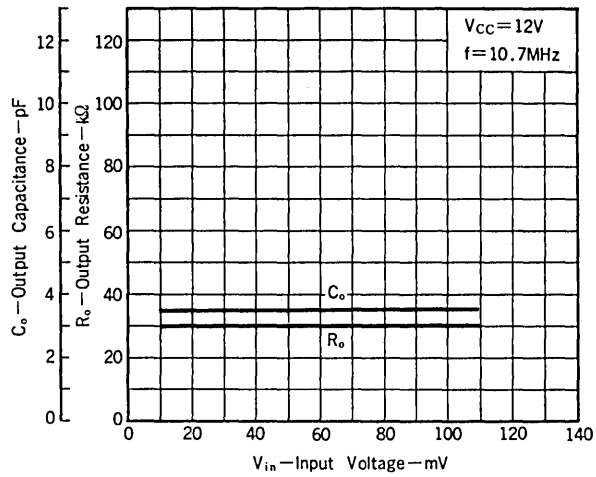
RESISTER FOR 3 pin, VOLTAGE GAIN vs.
CONSTANT CURRENT
(Measure in Differential Circuit)



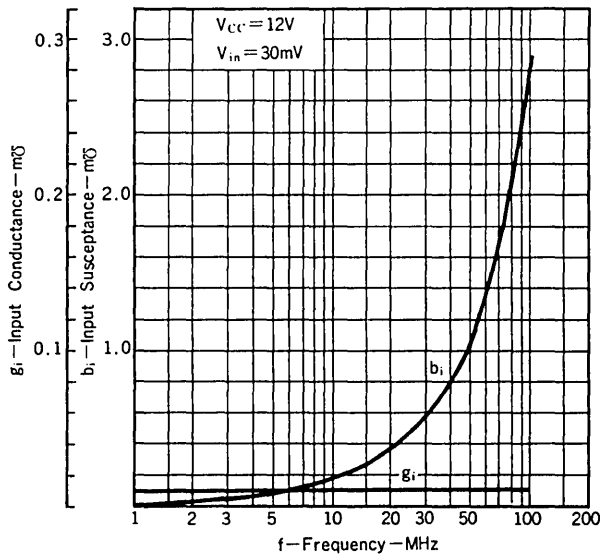
INPUT RESISTANCE AND CAPACITANCE
vs. INPUT VOLTAGE
(Measure in Differential Circuit)



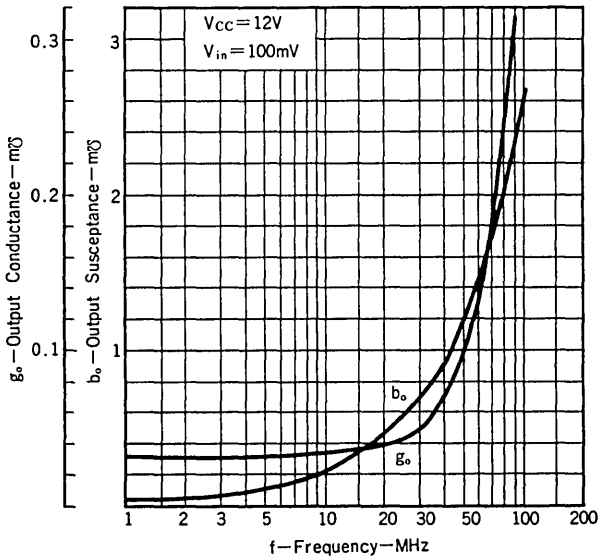
OUTPUT RESISTANCE AND CAPACITANCE
vs. INPUT VOLTAGE
(Measure in Differential Circuit)



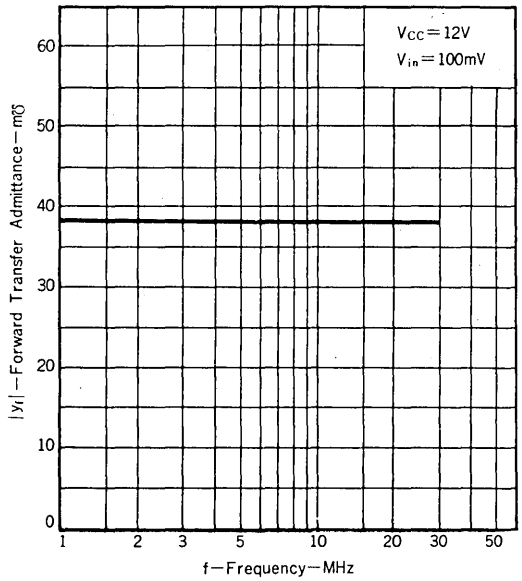
INPUT ADMITTANCE vs. FREQUENCY
(Measure in Differential Circuit)



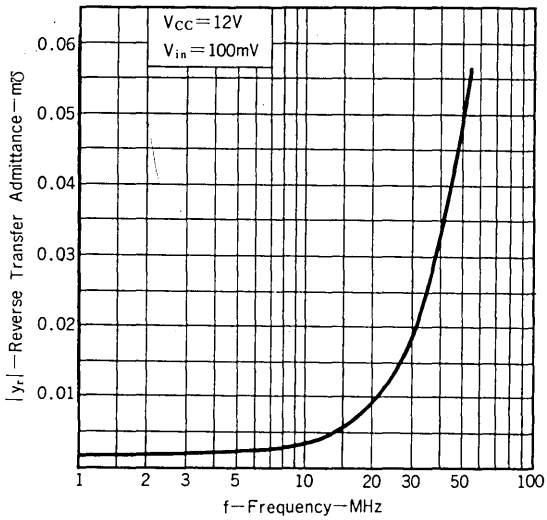
OUTPUT ADMITTANCE vs. FREQUENCY
(Measure in Differential Circuit)



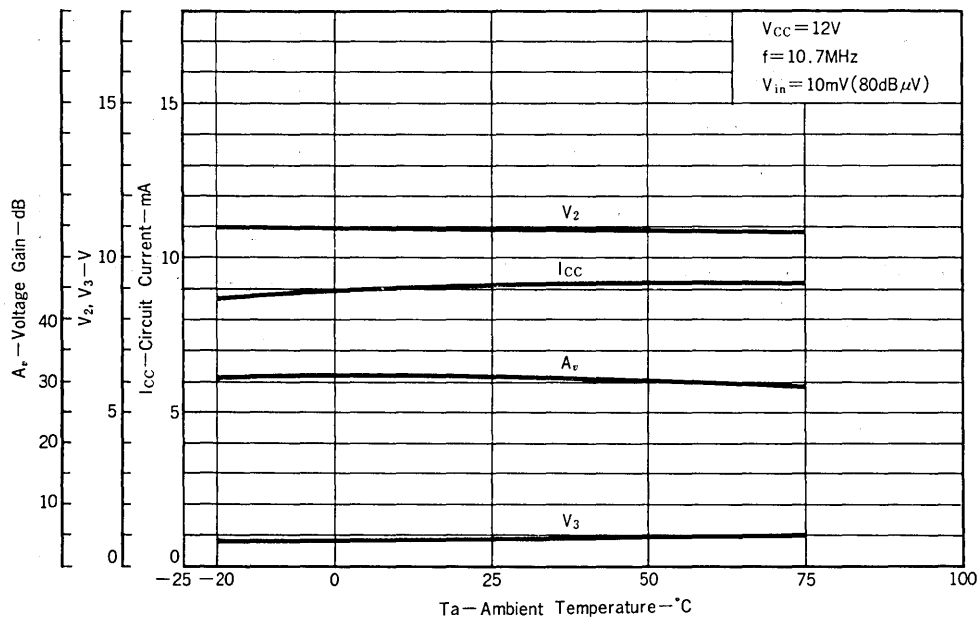
FORWARD TRANSFER ADMITTANCE
vs. FREQUENCY
(Measure in Differential Circuit)



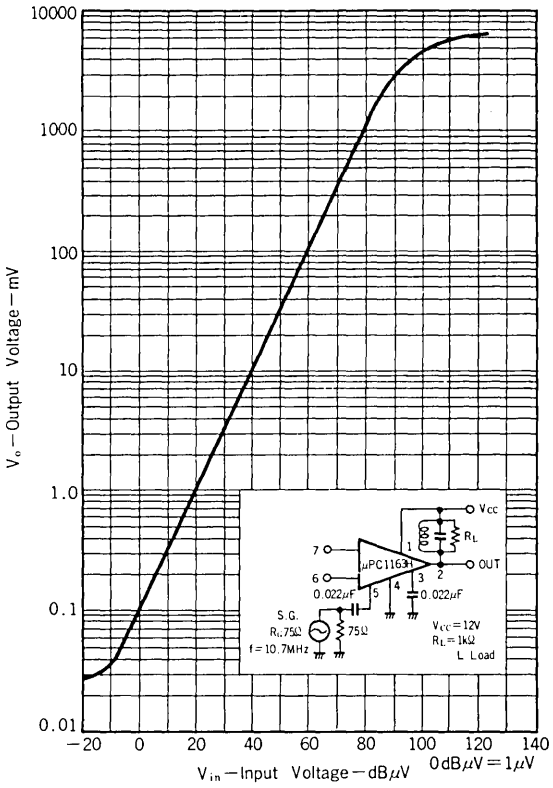
REVERSE TRANSFER ADMITTANCE
vs. FREQUENCY
(Measure in Differential Circuit)



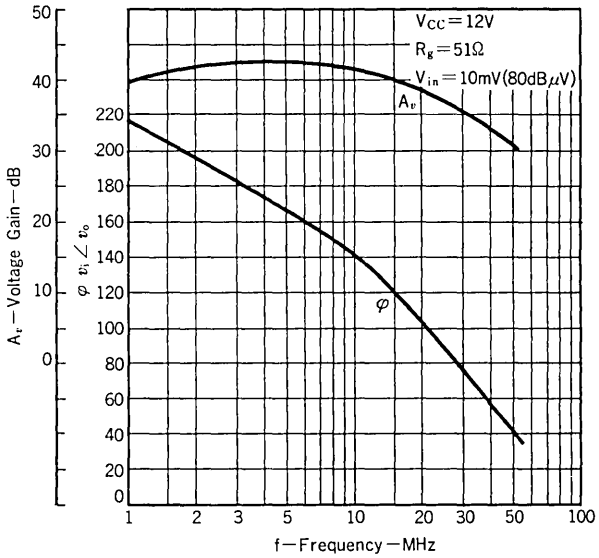
VOLTAGE GAIN, V2, V3, CIRCUIT CURRENT
vs. AMBIENT TEMPERATURE
(Measure in Differential Circuit)



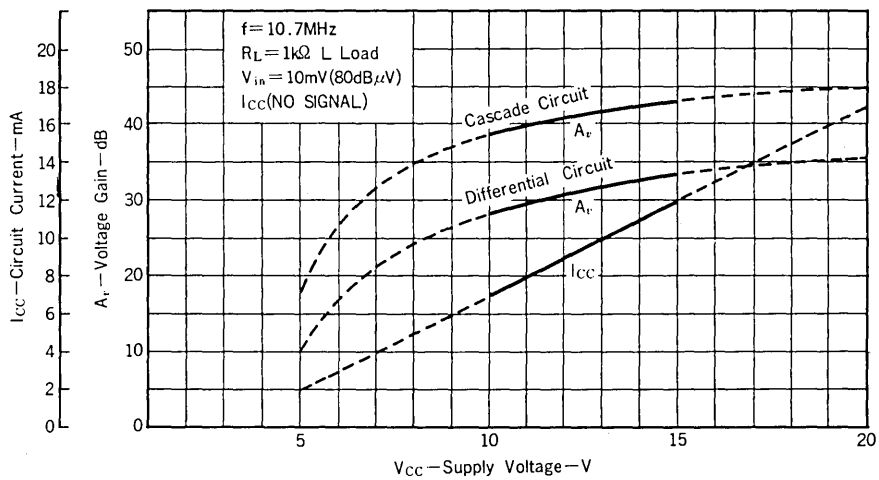
OUTPUT VOLTAGE vs. INPUT VOLTAGE
(Measure in Cascade Circuit)



VOLTAGE GAIN, PHASE vs. FREQUENCY
(Measure in Cascade Circuit)

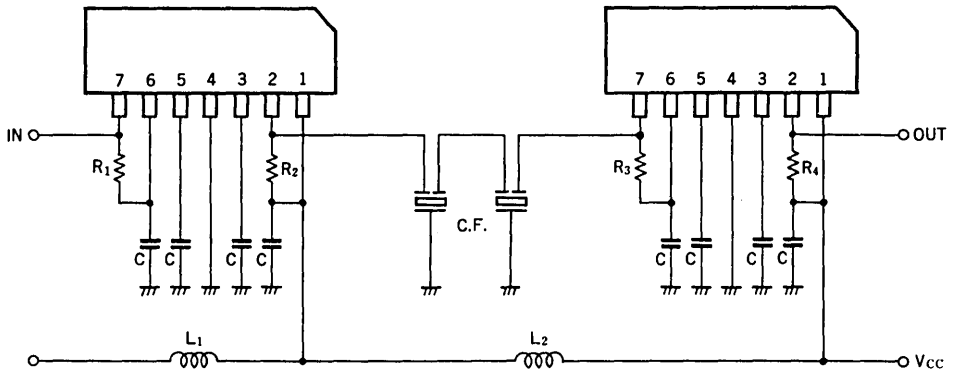


CIRCUIT CURRENT, VOLTAGE GAIN vs. SUPPLY VOLTAGE



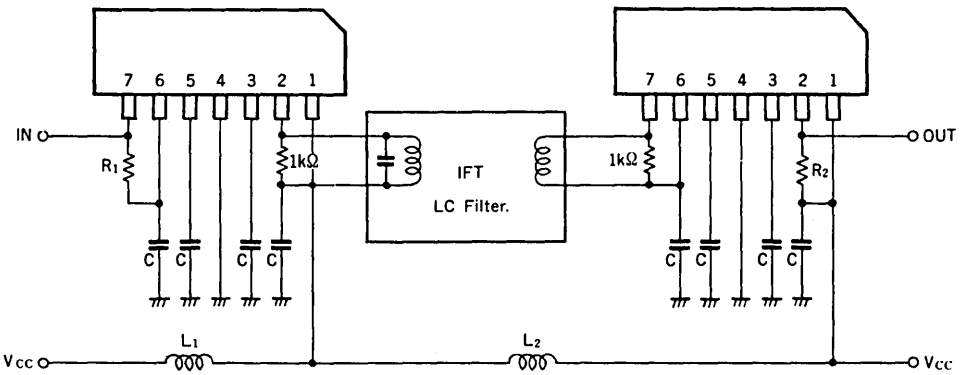
TYPICAL APPLICATIONS

- FM-IF amplifier using a ceramic filter.



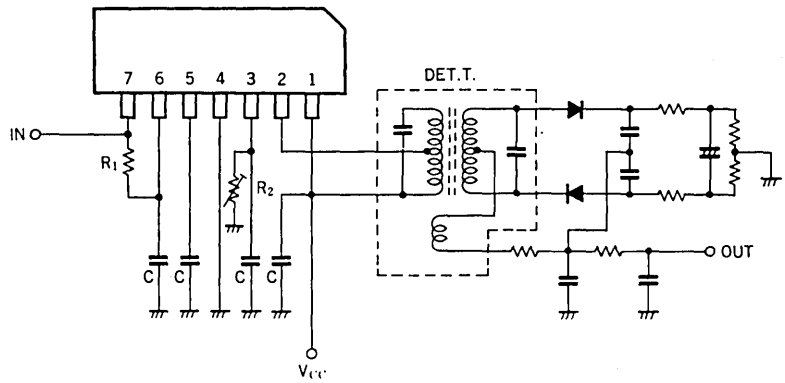
R_1 to R_4 : Match to the impedance of the ceramic filter.
C : High frequency bypass capacitors. 0.022 pF ceramic capacitor.
L_1 & L_2 : Decoupling inductances of the power supply circuit.
C. F. : Ceramic filter.

- FM-IF amplifier using a IC filter.



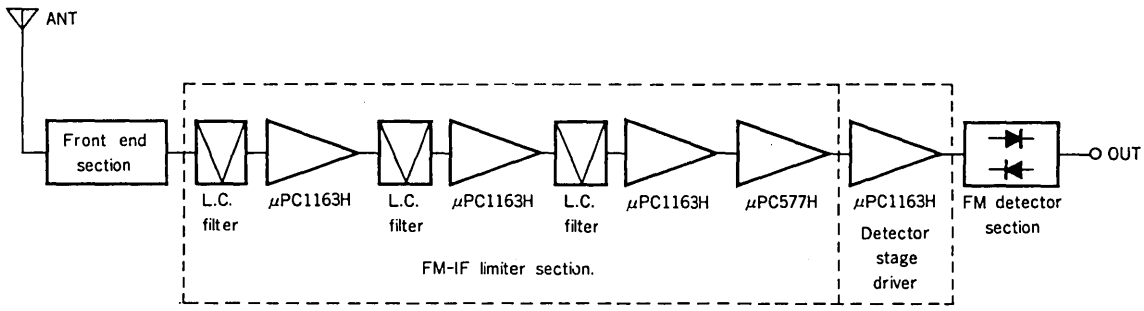
R_1 & R_2 : Match to the input and output impedance.
C : High frequency bypass capacitors. 0.022 μF ceramic capacitors.
L_1 & L_2 : Decoupling inductances of the power supply circuit.
IFT : FM intermediate-frequency filter coils. PLF (Toko Company)

- FM-IF detector circuit.



R_1	: Match to input impedance.
C	: High frequency bypass capacitors. 0.022 μF ceramic capacitors.
DET. T.	: FM detector filter coil.
R_2	: Registor for adjusting detector drive current. (Adjustment of constant current I_O.)

- Recommended line-up for high class stereo tuner.



Precautions on the use of the μPC1163H.

1. When the μPC1163H is used with a discrete resistor connected between pin 3 and ground, caution must be taken so that P_d does not exceed 270mW at 75°C with the change of the differential constant current I_o from 4.5mA to a maximum of 15mA.
2. The recommended operating supply voltage of the μPC1163H is 12V, and it should be used within a range of 10V to 15V. Since the dielectric strength of the output terminal 2 is 20V, care should be taken not to exceed this voltage when a tuned load is used.

BIPOLAR ANALOG INTEGRATED CIRCUIT
μPC1167C2

FM IF SYSTEM WITH QUADRATURE DETECTOR
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

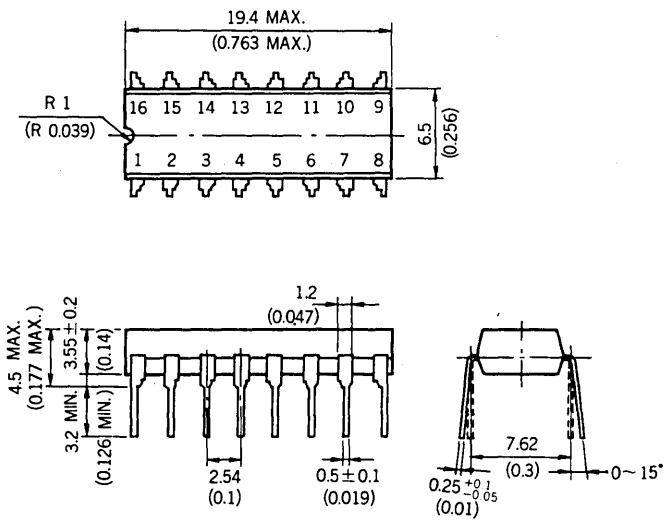
DESCRIPTION

The μPC1167C2, a monolithic integrated circuit, is a FM-IF system with Q-DET for use in Hi-Fi FM stereo tuners.
This device includes three-stage IF amplifier/limiter, quadrature detector, AF preamplifier and specific circuits for AGC, AFC, muting (squelch), signal meter and center meter.
The external form is 16 pin, dual in-line plastic package.

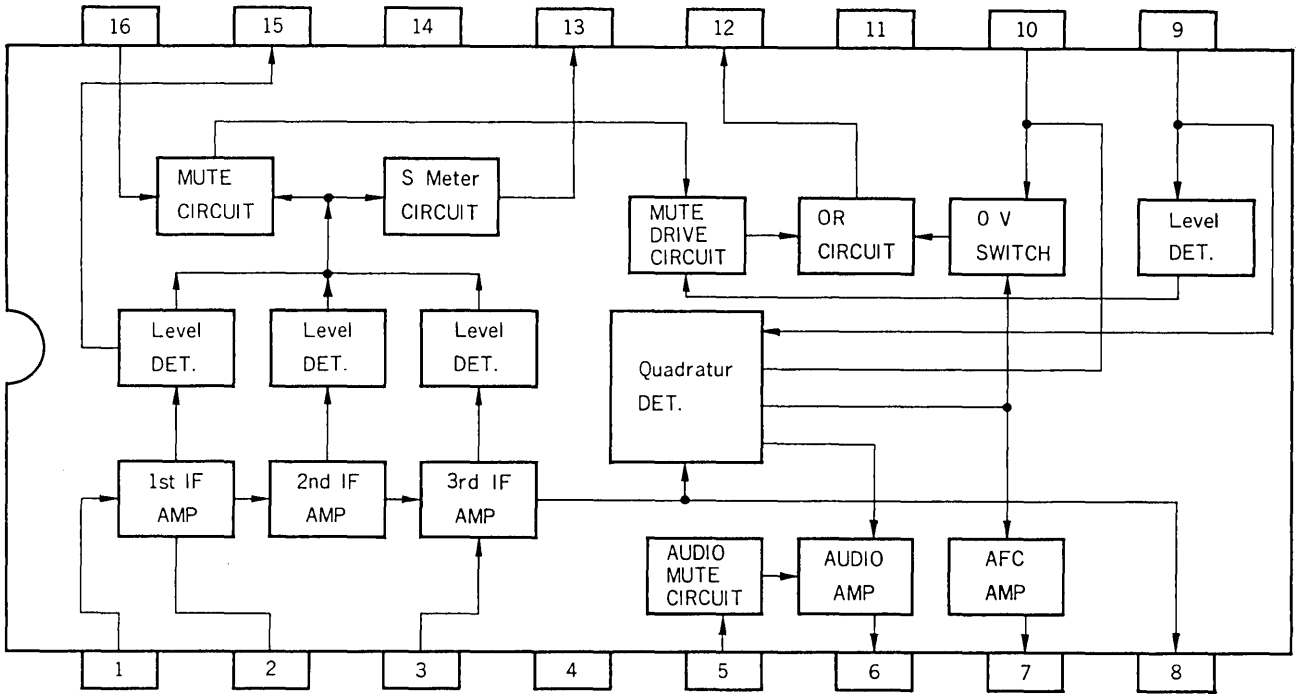
FEATURES

- Exceptional input limiting sensitivity. : 25 dBμV TYP.(−3 dB point from V_{OAF} with 100 dBμV input)
- High AM Rejection Ratio. : 55 dB TYP. (V_i = 100 dBμV, AM,: 400 Hz, 30 % MOD. FM : 400 Hz, 75 kHz, DEV.)
- Low Total Harmonic Distortion. : 0.02 % TYP. (V_i = 100 dBμV)
- High recovered audio voltage. : 340 mV TYP. (V_i = 100 dBμV)
- Low transient noise at mute circuit turn-on and off.
- Adjustable muting sensitivity. : 27 dBμV TYP. (V_{R1} = open) 35 dBμV TYP. (V_{R1} = 33 kΩ)
- Adjustable muting band width. : BW(MUTE) = ±75 kHz TYP. (V_i = 100 dBμV, V_{12} = 1.4 V, R_7 = 5.6 kΩ)
- Wide range of power supplies. : 8.5 V to 14 V

PACKAGE DIMENSIONS
in millimeters (inches)



FUNCTIONAL BLOCK DIAGRAM



TERMINAL CONNECTION

TERM. NO.	CONNECTION	TERM. NO.	CONNECTION
1	IF INPUT	9	DETECTOR INPUT
2	INPUT BYPASS	10	REFERENCE BIAS
3	INPUT BYPASS	11	V_{CC}
4	GND	12	MUTE DRIVE OUTPUT
5	MUTE CONTROL	13	SIGNAL METER OUTPUT
6	AUDIO OUTPUT	14	GND
7	AFC OUTPUT	15	AGC OUTPUT
8	IF OUTPUT	16	MUTING SENSITIVITY ADJUSTMENT

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Supply Voltage	V_{CC}	15	V
Supply Current	I_{CC}	40	mA
Input Voltage	V_I	3	V_{p-p}
Package Dissipation	P_D	420*	mW
Operating Temperature	T_{opt}	-20 to +60	°C
Storage Temperature	T_{stg}	-40 to +125	°C

*Ta = 60 °C

RECOMMENDED OPERATING CONDITION (Ta = 25 °C)

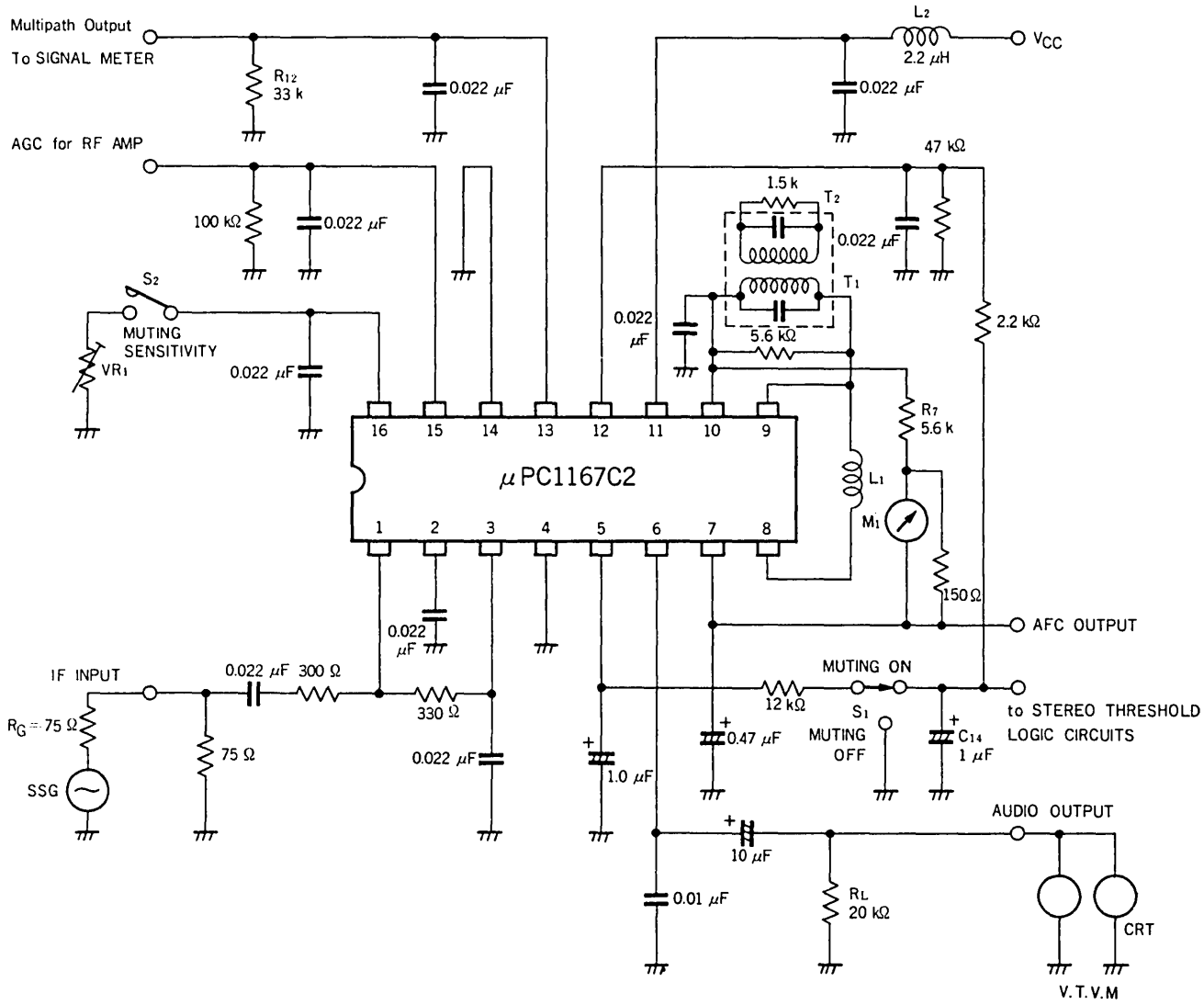
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	8.5	12	14	V

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

(V_{CC} = 12 V, f = 10.7 MHz, f_{MOD} = 400 Hz, f = ±75 kHz DEV., R_g = 330 Ω)

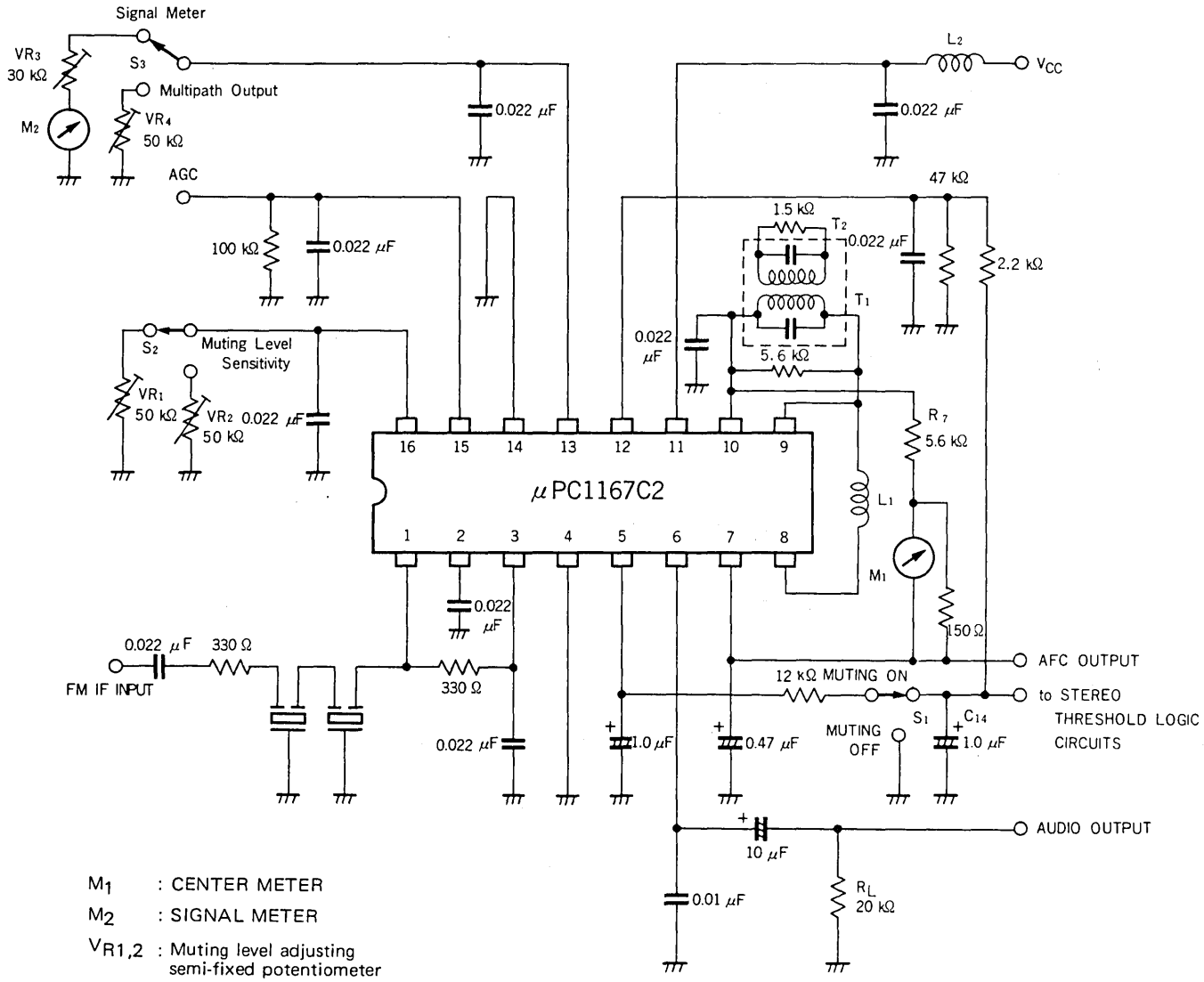
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Current	I_{CC}	14	23	31	mA	No Signal
Input Limiting Voltage	$V_{i(lim)}$		25	31	dBμV	−3 dB point from V_{OAF} with 100 dBμV input
Recovered Audio Voltage	V_{OAF}	240	340	460	mV	V_i = 100 dBμV
Total Harmonic Distortion	T.H.D.		0.02	0.2	%	V_i = 100 dBμV
Signal to Noise Ratio	S/N	75	81		dB	V_i = 100 dBμV
AM Rejection	A.M.R. (1)	45	55		dB	V_i = 100 dBμV AM : 400 Hz, 30 % MOD. FM : 400 Hz, 75 kHz DEV.
Muting Sensitivity	$V_{i(MUTE)1}$	19	27	35	dBμV	V_{12} = 1.4 V, V_{R1} = Open
	$V_{i(MUTE)2}$		35		dBμV	V_{12} = 1.4 V, V_{R1} = 3.9 kΩ
Muting Attenuation	MUTE(ATT)	69	75		dB	V_5 = 2 V, V_{R1} = Open
Muting Band Width	BW(MUTE)	90	150		kHz	V_i = 100 dBμV, V_{12} = 1.4 V R_7 = 5.6 kΩ
Mute Drive Output	$V_{12(1)}$	4.5	6.0		V	V_i = 0 dBμV
	$V_{12(2)}$		0	0.3	V	V_i = 100 dBμV
Signal Meter Drive Output	$V_{13(1)}$		0	0.3	V	V_i = 0 dBμV
	$V_{13(2)}$		2.0		V	V_i = 70 dBμV
	$V_{13(3)}$	3.0	4.0		V	V_i = 100 dBμV
AGC Output	$V_{15(1)}$	5.0	6.0	7.0	V	V_i = 0 dBμV
	$V_{15(2)}$		0.1	0.5	V	V_i = 100 dBμV

TEST CIRCUIT FOR ELECTRICAL CHARACTERISTICS



M_1	: Center Meter	L_1	: 7BA220 (K.K.TOKO)
V_{R1}	: Muting Level adjusting semi-fixed potentiometer	L_2	: 7BA2R2K (K.K.TOKO)
S_1	: Muting switch	T_1	: TKAEA24638 AUO (K.K.TOKO)
S_2	: Muting Level adjusting switch	T_2	: TKAEA25868 X (K.K.TOKO)

TYPICAL APPLICATION (Top View)



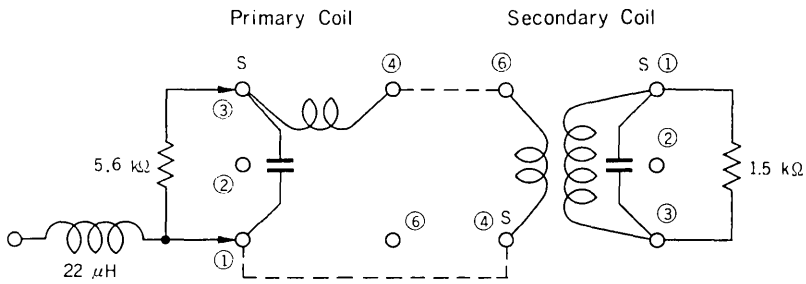
M_1	: CENTER METER	
M_2	: SIGNAL METER	
$V_{R1,2}$	: Muting level adjusting semi-fixed potentiometer	
V_{R3}	: Signal meter sensitivity adjusting semi-fixed potentiometer	
V_{R4}	: Multipath output adjusting semi-fixed potentiometer	
S_1	: Muting switch	
S_2	: Muting level adjusting switch	
S_3	: Signal meter, Multipath output switching switch	
L_1	: 7BA220	(K.K.TOKO)
L_2	: 7BA2R2K	(K.K.TOKO)
T_1	: TKAEA24638 AUO	(K.K.TOKO)
T_2	: TKAEA25868 X	(K.K.TOKO)

NOTES

Adjustment of muting sensitivity Adjust the input level by the semi-fixed potentiometer connected to #16 terminal. If the muting sensitivity is normal, make #16 terminal open. In case that you adjust the muting level at lower than normal, connect a resistor in parallel with capacitor (C_{14} : 1 μF) and adjust that resistance. (cf. Fig. 6)

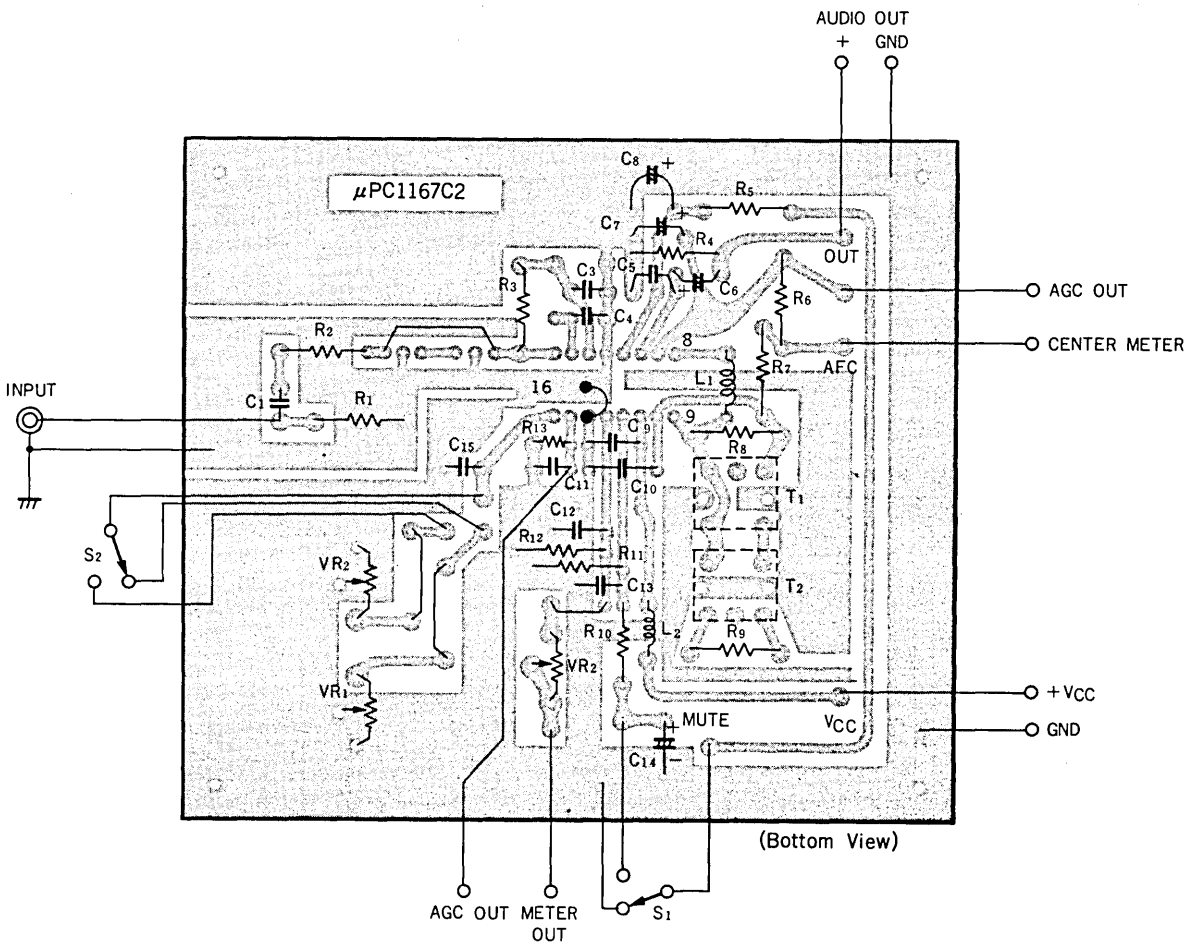
Adjustment of muting band width Adjust the resistance (R_7 : 5.6 kΩ) connected #7 with #10. (cf. Fig. 7)

WIRING DIAGRAM OF DETECTOR TRANSFORMER (Bottom View)



Primary Coil	Type No.	TKAEA24638 AUO (K.K.TOKO)
	Color of Core	White
	Center Frequency	10.7 MHz
	Tuning Range	+3 %
	Tuning Capacity	82 pF (short 1 to 4)
	Q_u	62 + 20 %
Secondary Coil	Type No.	TKAEA25868 X (K.K.TOKO)
	Color of Core	Blue
	Center Frequency	10.7 MHz
	Tuning Range	+3 %
	Tuning Capacity	75 pF
	Q_u	58 + 20 %

OUTBOARD COMPONENTS MOUNTED ON A PRINTED-CIRCUIT BOARD (Unit : mm)



R_1	.....	75 Ω	C_1	.....	0.022 μF	C_{14}	.....	1 μF
R_2	.....	300 Ω	C_3	.....	0.022 μF	C_{15}	.....	0.022 μF
R_3	.....	330 Ω	C_4	.....	0.022 μF			
R_4	.....	20 kΩ	C_5	.....	0.01 μF	V_{R1}	.....	50 kΩ
R_5	.....	12 kΩ	C_6	.....	10 μF	V_{R2}	.....	50 kΩ
R_6	.....	150 Ω	C_7	.....	0.47 μF	V_{R3}	.....	30 kΩ
R_7	.....	5.6 kΩ	C_8	.....	1 μF			
R_8	.....	5.6 kΩ	C_9	.....	0.022 μF	T_1	.....	TKAEA24638 AUO (K.K.TOKO)
R_9	.....	1.5 kΩ	C_{10}	.....	0.022 μF	T_2	.....	TKAEA25868 X (K.K. TOKO)
R_{10}	.....	2.2 kΩ	C_{11}	.....	0.022 μF	L_1	.....	7BA220 (K.K. TOKO)
R_{11}	.....	47 kΩ	C_{12}	.....	0.022 μF	L_2	.....	7BA2R2 (K.K. TOKO)
R_{12}	.....	33 kΩ	C_{13}	.....	0.022 μF	S_1	.....	Muting switch
R_{13}	.....	100 kΩ				S_2	.....	Muting level adjusting switch

TYPICAL PERFORMANCE CHARACTERISTICS (Ta = 25 °C)

Fig. 1 V_{OAF}, S/N, A.M.R., T.H.D. vs. V_{in}

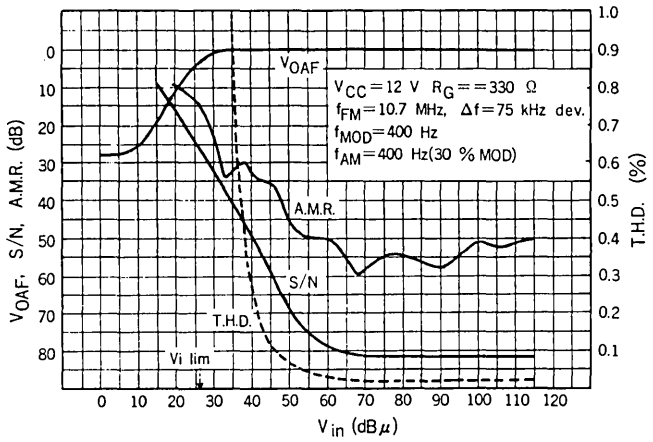


Fig. 2 V_{12}, V_{13}, V_{15} vs. V_{in}

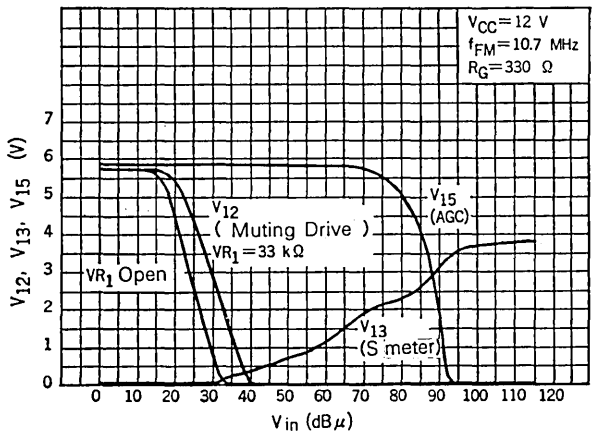


Fig. 3 V_{OAF} vs. V_{in}

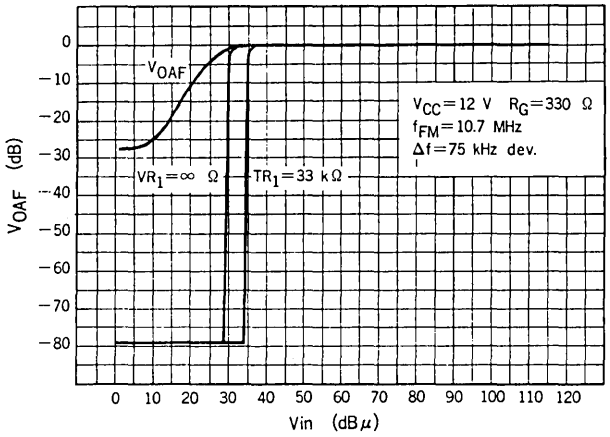


Fig. 4 Mute ATT. vs. CARRIER FREQUENCY

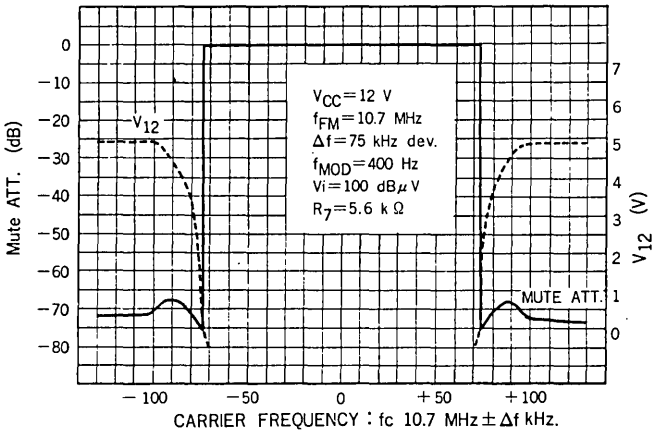


Fig. 5 V_{OAF}, T.H.D. vs. MODULATION FREQUENCY

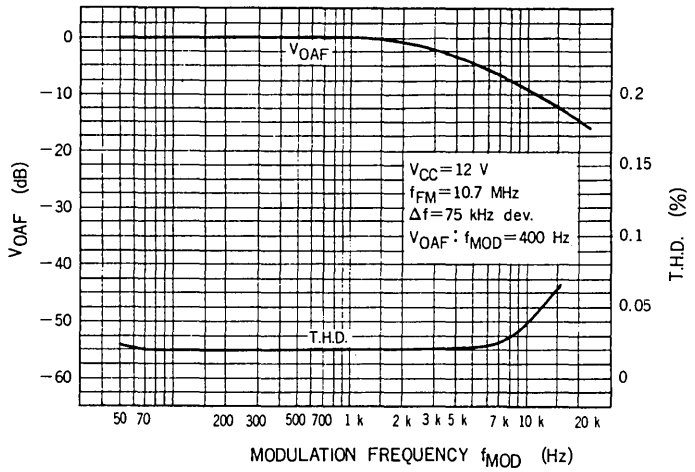


Fig. 6 VR_1 vs. V_{in}

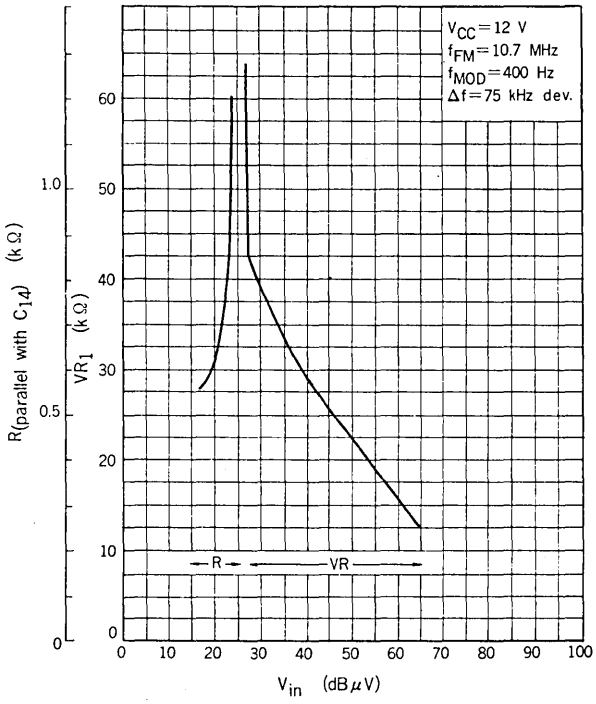
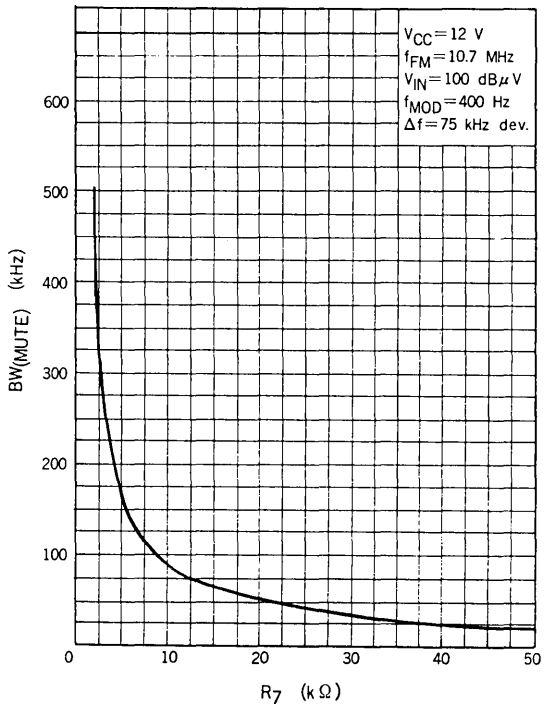


Fig. 7 $BW_{(MUTE)}$ vs. R_7



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1161C3

FM MULTIPLEX STEREO DEMODULATOR
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

DESCRIPTION

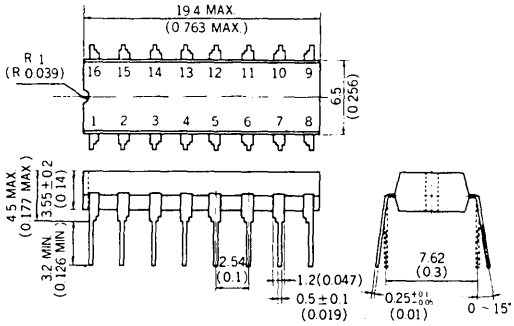
The μPC1161C3 is a silicon monolithic integrated circuit for FM multiplex demodulator developed for high class stereo FM tuners. As the IC adopts a PLL (Phase Locked Loop) system, complexity of control usually experienced when using conventional external coil is eliminated and the demodulator can easily be constructed by simply controlling the external semi-fixed potentiometer. Internal circuits are composed of a stereo demodulator, a lamp driver, an input stage pre-amplifier that is capable of establishing variable input signal levels, a VCO (Voltage Controlled Oscillator) constituting PLL, a phase comparator, a LPF (Low Pass Filter), a frequency divider, and a DC amplifier. A stereo-monaural automatic switching circuit, a circuit for manual switching, VCO forced stop circuit etc. are built-in.

FEATURES

- External parts are small. Coil is not used.
- Low monaural total harmonic distortion.
  T.H.D. = 0.02 % TYP , at f = 1 kHz.
  T.H.D. = 0.03 % TYP , at f = 10 kHz.
- Low stereo total harmonic distortion.
  T.H.D. = 0.02 % TYP , at f = 1 kHz (L+R).
  T.H.D. = 0.06 % TYP , at f = 10 kHz (L or R).
  T.H.D. = 0.12 % TYP , at f = 10 kHz (L+R).
- High channel separation
  Sep. = 55 dB TYP , at f = 1 kHz.
- Built-in output stage post amplifier.
  V_{out} = 1.5 Vr.m.s. TYP , at V_{in} = 300 mV.
  V_{out} = 3.5 Vr.m.s. TYP , at V_{in} = 700 mV.
- Stereo-monaural switching can be made either automatically or manually from outside. The shock noise at switching is reduced considerably.
- Stereo-monaural switching operation is perfectly synchronized with a stereo indicator lamp.
- Monitoring of VCO free running frequency can be performed by directly connecting the frequency counter to No. 9 terminal.
- High signal to noise ratio.
  S/N = 82 dB TYP , at V_{in} = 300 mV.
- Wide maximum input level.
  V_{in} = 700 mVr.m.s , T.H.D. = 1 %.

PACKAGE DIMENSIONS

in millimeters (inches)

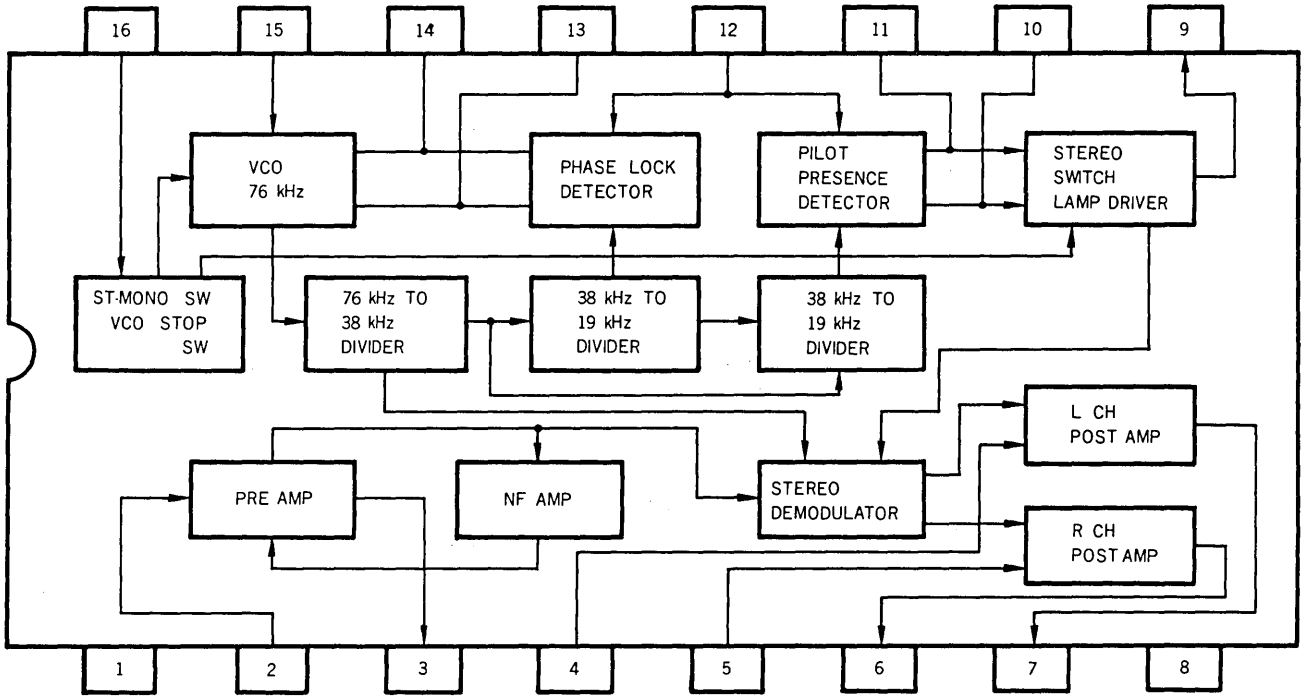


TERMINAL CONNECTION

No.	CONNECTION	No.	CONNECTION
1	V_{CC}	9	ST. LAMP & 19 kHz MONITOR
2	PRE AMP INPUT	10	LOW PASS FILTER
3	PRE AMP OUTPUT	11	LOW PASS FILTER
4	POST AMP BIAS	12	DETECTOR INPUT
5	POST AMP BIAS	13	LOOP FILTER
6	R-CH OUTPUT	14	LOOP FILTER
7	L-CH OUTPUT	15	OSC RC. NETWORK
8	GND	16	ST.-MONO. SW & VCO STOP

NOTE : Numerical values show TYP. values unless otherwise designated.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Supply Voltage	V_{CC}	15	V
Lamp Current	I_L	75	mA
Package Dissipation	P_D	400*	mW
Operating Temperature	T_{opt}	-20 to +70	°C
Storage Temperature	T_{stg}	-40 to +125	°C

*Ta = 70 °C

RECOMMENDED OPERATING CONDITION (Ta = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	9	12	15	V

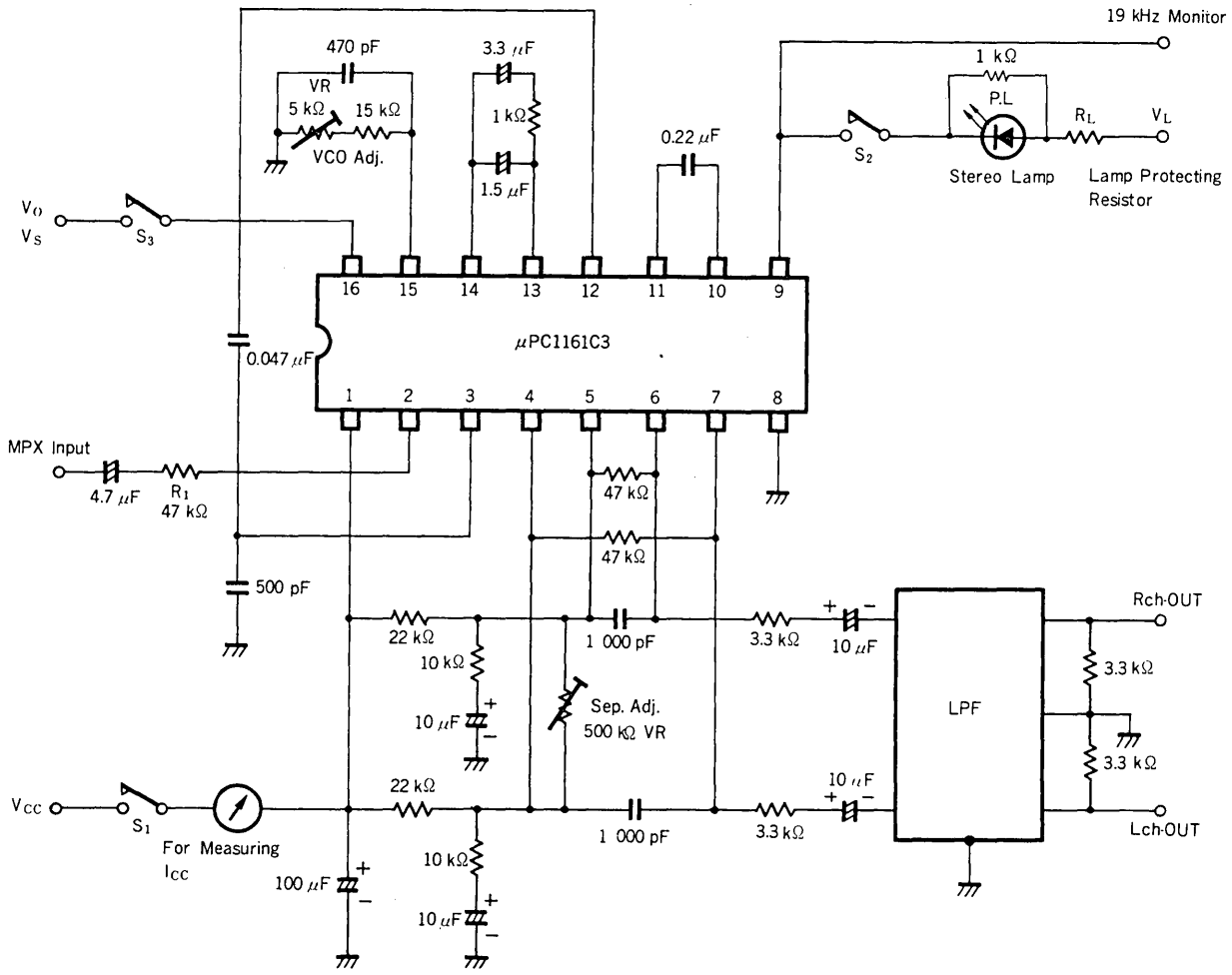
ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

(V_{CC} = 12 V, f = 1 kHz, R_1 = 47 kΩ, R+L = 270 mV, Pilot = 30 mV)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Supply Current	I_{CC}	12	20	30	mA	No Signal	
Channel Separation	Sep.	40	50		dB	Pilot = 30 mV	f = 100 Hz
		45	55		dB		f = 1 kHz
		35	45		dB		f = 10 kHz
Voltage Gain	A_V	9	13	17	dB	Monaural, V_{in} = 300 mV*	
Channel Balance	C.B.	-1.5	0	1.5	dB	Monaural, V_{in} = 300 mV	
		-1.5	0	1.5	dB	Stereo, Pilot = 30 mV	
Monaural Total Harmonic Distortion	T.H.D.		0.02	0.1	%	V_{in} = 300 mV	
Stereo Total Harmonic Distortion	T.H.D.		0.02		%	R+L = 270 mV Pilot = 30 mV	f = 100 Hz
			0.02	0.1	%		f = 1 kHz
			0.12		%		f = 10 kHz
Pilot Level for Lamp On	L-ON	6	12	20	mVr.m.s.	Pilot Level, R_1 = 47 kΩ	
Stereo Lamp Hysteresis	Hy.		6		dB	Pilot Level	
Capture Range	C.R.	±1.5	±3		%	Pilot = 30 mV	
Ultrasonic Frequency Rejection	19 kHz Rej.		35		dB	Pilot = 30 mV	
	38 kHz Rej.		45		dB	Pilot = 30 mV	
SCA Rejection	SCA Rej.		70		dB	Pilot = 30 mV, SCA = 30 mV	
Maximum Input Level	V_{in}		0.7		Vr.m.s.	Monaural, T.H.D. = 1 %	
Signal to Noise Ratio	S/N		82		dB	V_{in} = 300 mV, After LPF	
Stereo-Monaural Switching SW-ON Voltage	V_S		1.4	1.6	V	No. 16 Terminal Voltage Where Stereo Lamp-OFF	
VCO Stop Voltage	V_O	7		V_{CC}	V	No. 16 Terminal Voltage Where VCO Stops	

*A_V is from the output level measured at IC output terminal. A_V can be set by the input impedance R_1.

TEST CIRCUIT FOR ELECTRICAL CHARACTERISTICS

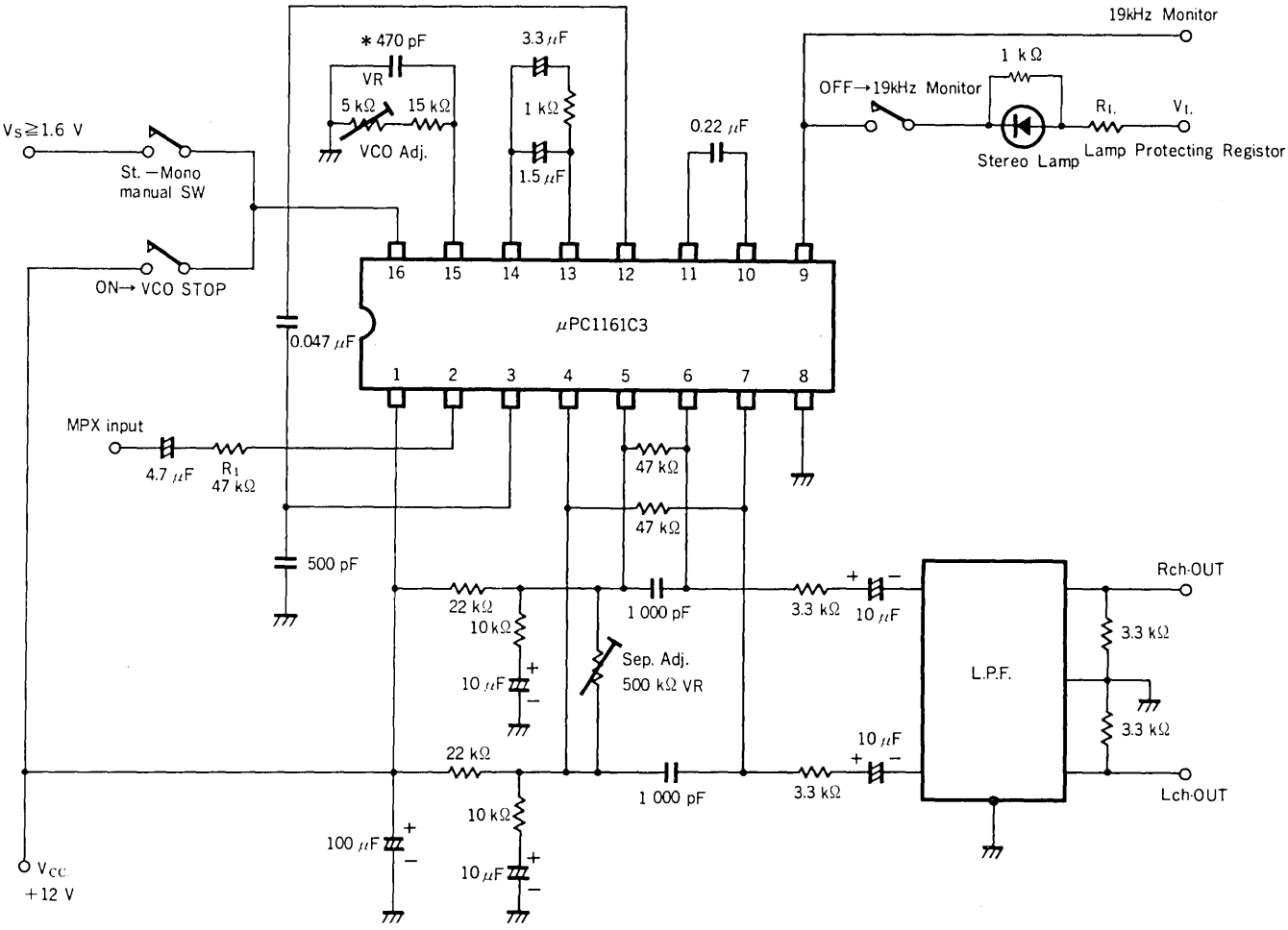


LPF	BL-13 (K.K. KORIN)
VCO Adj.	VCO tuning semi-fixed potentiometer
Sep. Adj.	Separation adjusting semi-fixed potentiometer
S1	V_{CC} ON-OFF SW
S2	SW for 19 kHz monitor
S3	SW for VCO stop

NOTES :

1. Use polystyrene capacitors for that connected to No. 15 terminal to compensate the temperature coef. of VCO.
2. For adjusting the VCO oscillation frequency, make S_2 open, connect the frequency counter to No. 9 terminal 19 kHz monitor and then set by varying the semi-fixed potentiometer VCO Adj. connected to No. 15 terminal
3. For separation adjustment, vary the semi-fixed potentiometer Sep. Adj. connected between terminals No. 4 and No. 5 to set at the best point.

TYPICAL APPLICATION

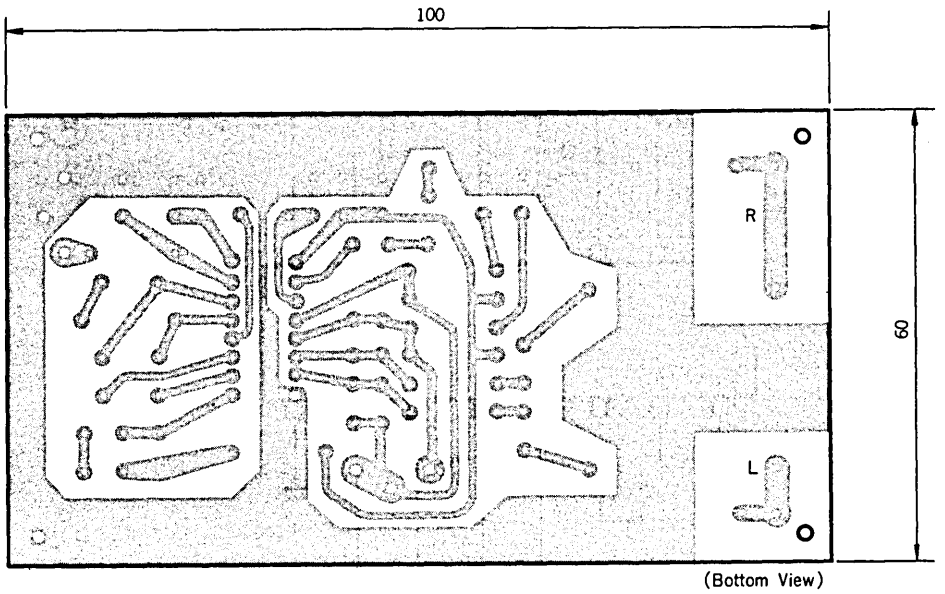


LPF	BL-13 (K.K. KORIN)
VCO Adj.	VCO tuning semi-fixed potentiometer
Sep. Adj.	Separation adjusting semi-fixed potentiometer
*470 pF	Polystyrene capacitor

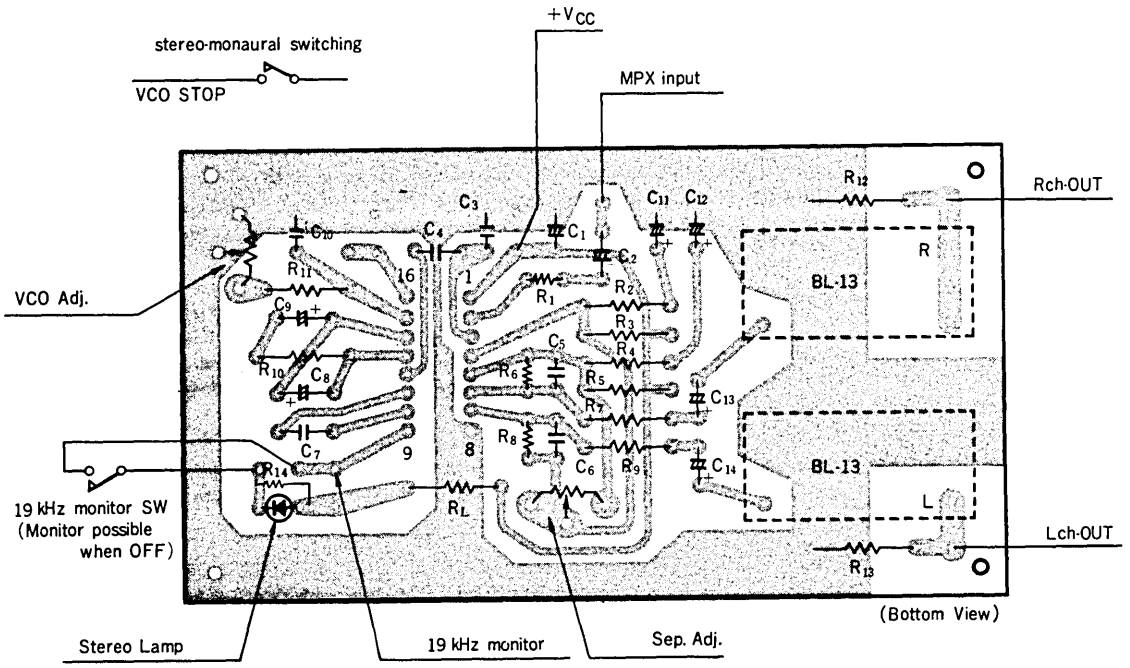
NOTES :

When the unit is used with power supply voltage of less than 12 V, the mid- point electric potential of the output terminals 6, 7 in the above typical application may change and Total Harmonic Distortion at output terminal will increase.
In this case change the bias registor 47 kΩ between terminals 5, 6 and terminals 4, 7 and keep at mid-point electric potential.

EXAMPLE OF PRINTED-CIRCUIT BOARD (Unit : mm)



OUTBOARD COMPONENTS MOUNTED ON A PRINTED-CIRCUIT BOARD



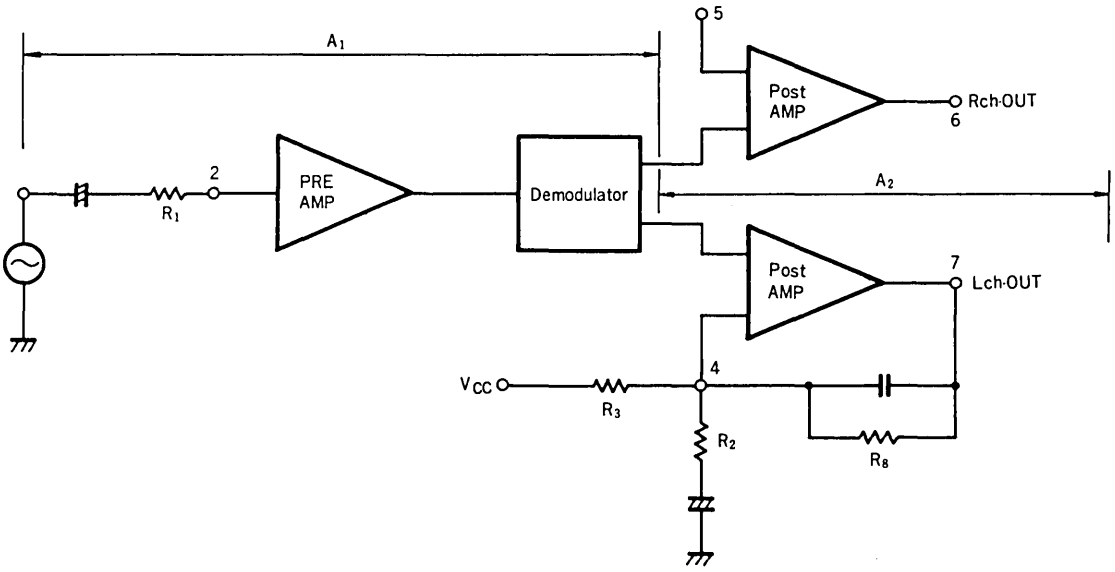
R_1=47 kΩ	R_6 =47 kΩ	R_{11}=15 kΩ	C_1=100 μF	C_6 =1 000 pF	C_{11}=10 μF	Sep. Adj.=500 kΩ VR
R_2=10 kΩ	R_7 =3.3 kΩ	R_{12}=3.3 kΩ	C_2=4.7 μF	C_7 =0.22 μF	C_{12}=10 μF	VCO Adj.=5 kΩ VR
R_3=22 kΩ	R_8 =47 kΩ	R_{13}=3.3 kΩ	C_3=500 pF	C_8 =1.5 μF	C_{13}=10 μF	BL-13=19 kHz LPF(K.K KORIN)
R_4=10 kΩ	R_9 =3.3 kΩ	R_{14}=1 kΩ	C_4=0.047 μF	C_9 =3.3 μF	C_{14}=10 μF	
R_5=22 kΩ	R_{10}=1.0 kΩ	R_L =Lamp Protecting Resistor	C_5=1 000 pF	C_{10}=470 pF(Polystyrene capacitor)		

ON CIRCUIT GAIN

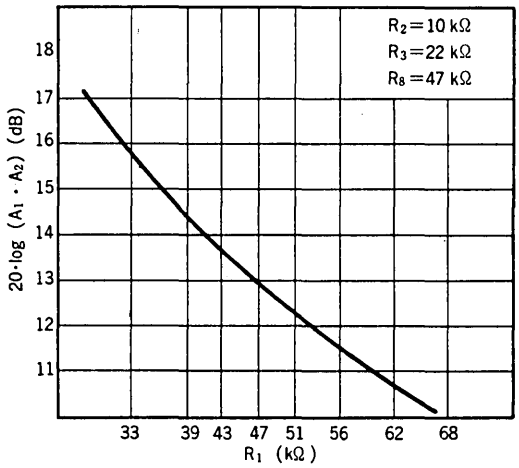
The circuit gain of the μPC1161C3 is obtained from, the input stage PRE AMP, the demodulator, and output stage POST AMP, and can be expressed equivalently from external resister ratio by following equation :

$$A_1 \fallingdotseq \frac{27}{R_1}, \qquad A_2 \fallingdotseq \frac{(R_3 /\!/ R_2) + R_8}{R_3 /\!/ R_2}$$

$$A_v \fallingdotseq 20 \log (A_1 \cdot A_2) \quad (dB)$$

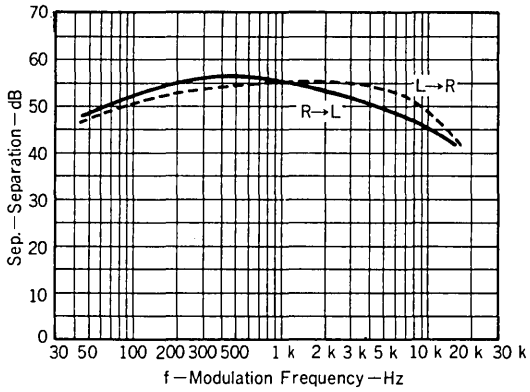


The change of the circuit gain in case an input resister R_1 has been varied is shown in the following drowing.

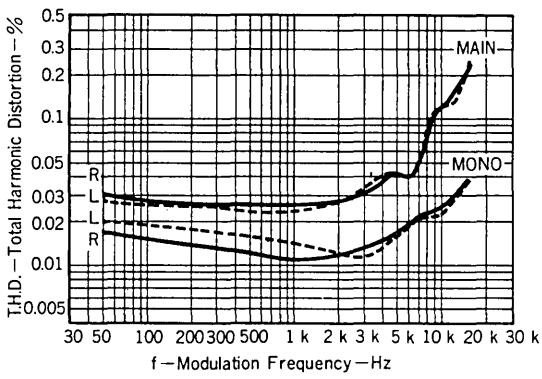


TYPICAL CHARACTERISTICS (Ta = 25 °C)

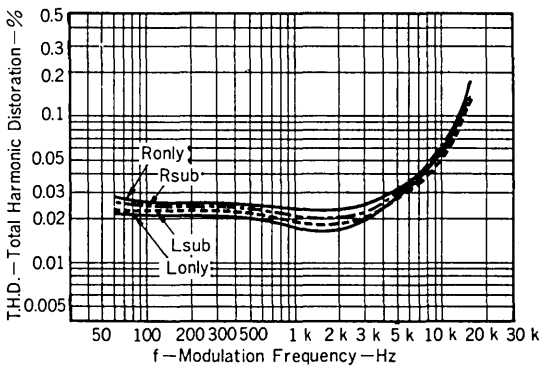
SEPARATION vs.
MODULATION FREQUENCY



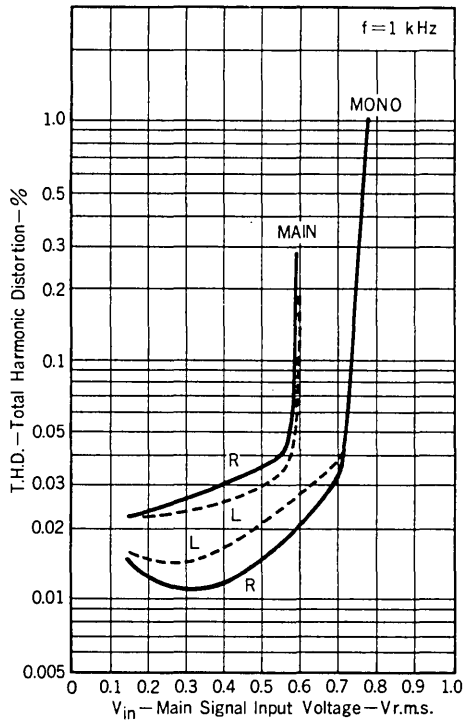
TOTAL HARMONIC DISTORTION
vs. MODULATION FREQUENCY



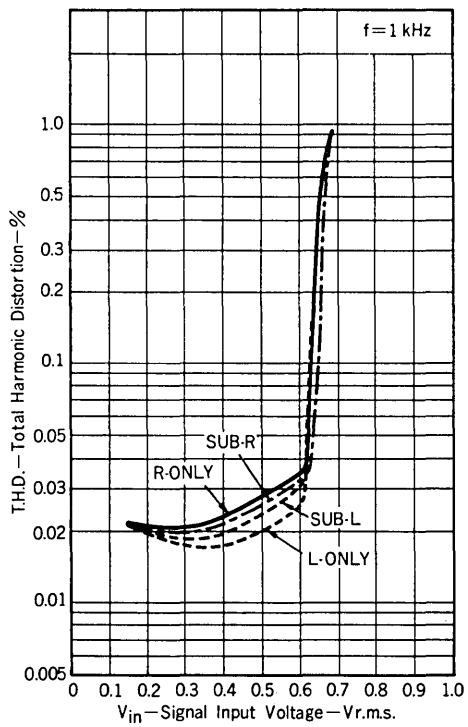
TOTAL HARMONIC DISTORTION vs.
MODULATION FREQUENCY (STEREO)



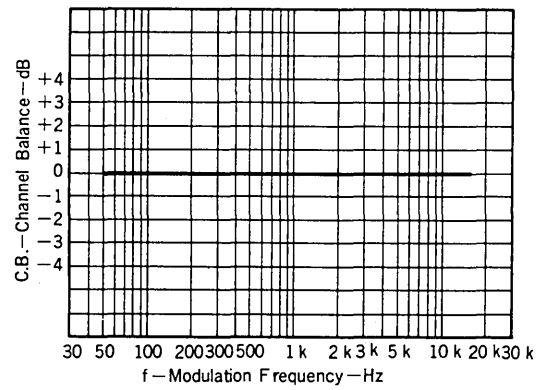
TOTAL HARMONIC DISTORTION
vs. MAIN SIGNAL INPUT VOLTAGE



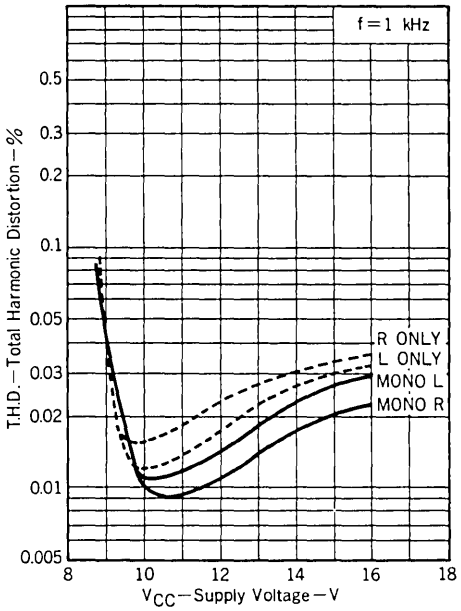
TOTAL HARMONIC DISTORTION
vs. SIGNAL INPUT VOLTAGE



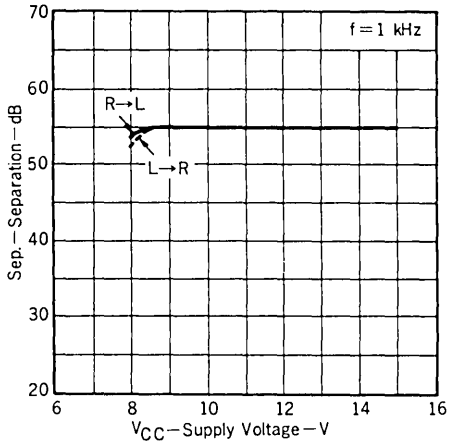
CHANNEL BALANCE vs.
MODULATION FREQUENCY



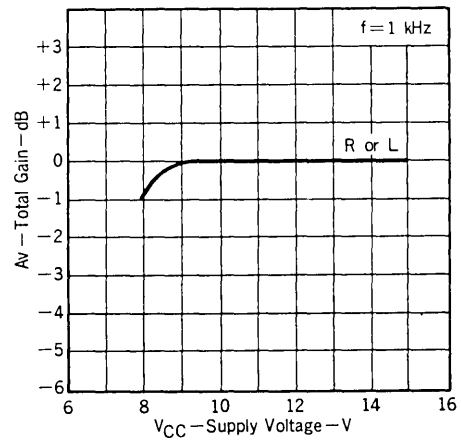
TOTAL HARMONIC DISTORTION
vs. SUPPLY VOLTAGE



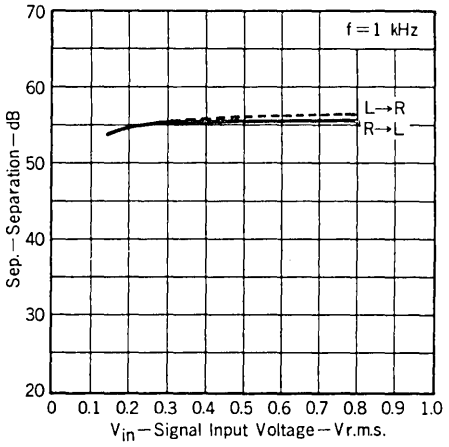
SEPARATION vs.
SUPPLY VOLTAGE



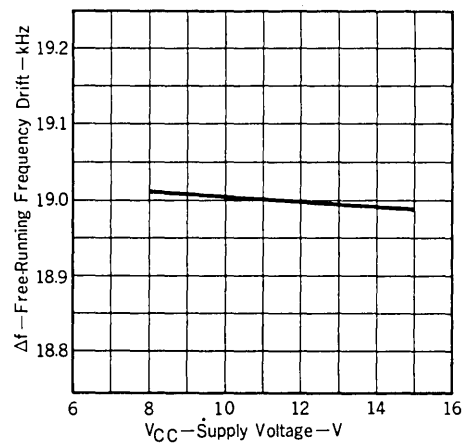
TOTAL GAIN vs.
SUPPLY VOLTAGE



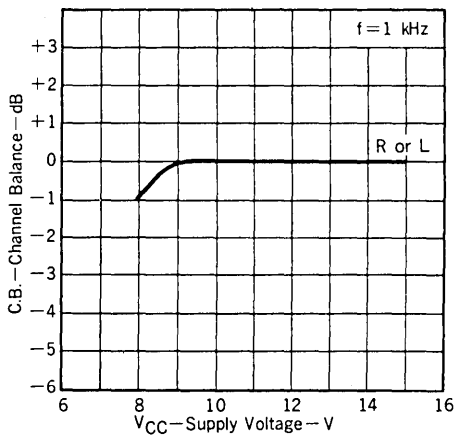
SEPARATION vs.
SIGNAL INPUT VOLTAGE



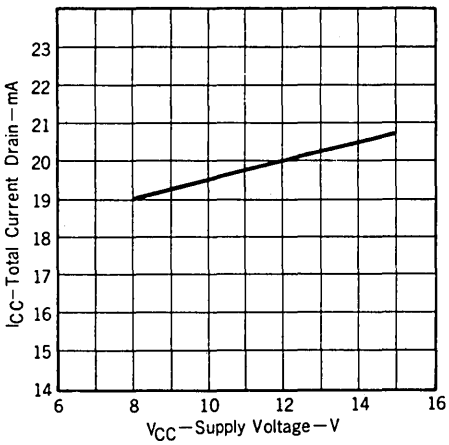
FREE-RUNNING FREQUENCY
DRIFT vs. SUPPLY VOLTAGE



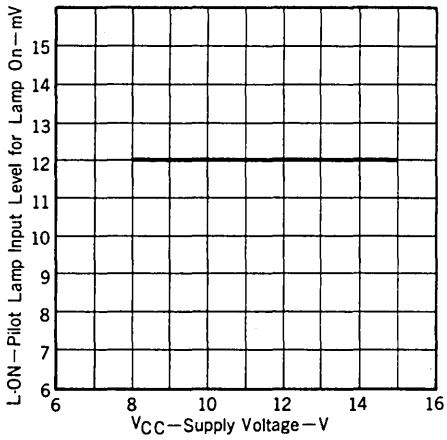
CHANNEL BALANCE vs.
SUPPLY VOLTAGE



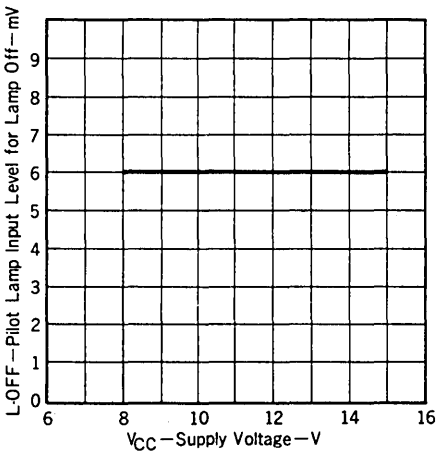
TOTAL CURRENT DRAIN vs. SUPPLY VOLTAGE (NO SIGNAL)



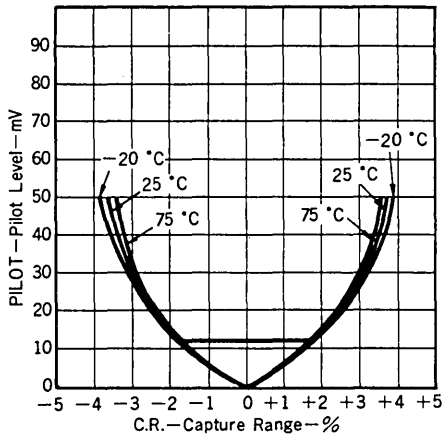
PILOT LAMP INPUT LEVEL FOR LAMP ON vs. SUPPLY VOLTAGE (PILOT ONLY)



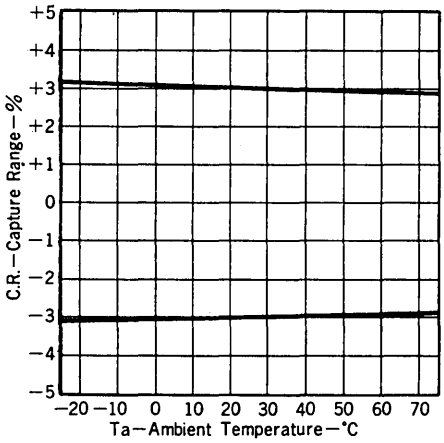
PILOT LAMP INPUT LEVEL FOR LAMP OFF vs. SUPPLY VOLTAGE (PILOT ONLY)



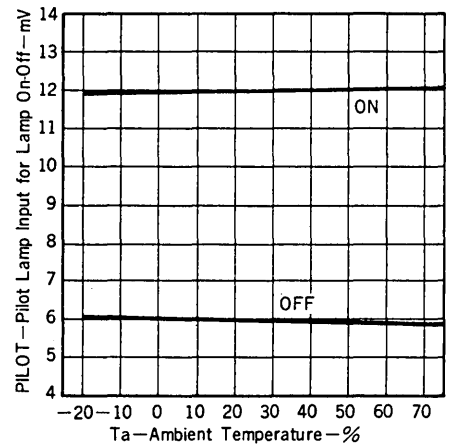
PILOT LEVEL AND AMBIENT TEMPERATURE vs. CAPTURE RANGE



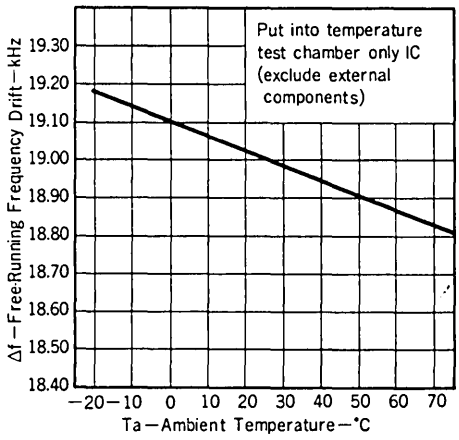
CAPTURE RANGE vs. AMBIENT TEMPERATURE (PILOT = 30 mV)



PILOT LAMP INPUT LEVEL FOR LAMP ON-OFF vs. AMBIENT TEMPERATURE



FREE-RUNNING FREQUENCY DRIFT vs. AMBIENT TEMPERATURE



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1235C

FM MULTIPLEX STEREO DEMODULATOR

SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

DESCRIPTION

The μPC1235C is a semiconductor integrated circuit for FM multiplex demodulator developed for high class stereo FM tuners. As the IC adopts a PLL (Phase Locked Loop) system, complexity of control usually experienced when using conventional external coil is eliminated and the demodulator can easily be constructed by simply controlling the external semi-fixed potentiometer. Internal circuits are composed of a stereo demodulator, a lamp driver, an input stage pre-amplifier that is capable of establishing variable input signal levels, a VCO (Voltage Controlled Oscillator) constituting PLL, a phase comparator, a LPF (Low Pass Filter), a frequency divider, and a DC amplifier. A stereo-monaural automatic switching circuit, a circuit for manual switching, VCO forced stop circuit etc. are built-in.

FEATURES

- As the coil can be omitted by the adoption of PLL system, reducing the number of external components and controlling procedures are made possible.
- Low monaural total harmonic distortion.
  T.H.D.=0.01 % TYP., at f=1 kHz.
  T.H.D.=0.03 % TYP., at f=10 kHz.
- Low stereo total harmonic distortion.
  T.H.D.= 0.02 % TYP., at f=1 kHz (L+R)
  T.H.D.= 0.06 % TYP., at f=10 kHz (L or R).
  T.H.D.= 0.12 % TYP., at f=10 kHz (L+R).
- High channel separation.
  Sep.=55 dB TYP., at f=1 kHz.
- Built-in output stage post amplifier.
  V_{out}=1.2 Vr.m.s. TYP., at V_{in}=300 mVr.m.s.
  V_{out}=3.6 Vr.m.s. TYP., at V_{in}=900 mVr.m.s.
- Stereo-monaural switching can be made either automatically or manually from outside. The shock noise at switching is reduced considerably.
- Stereo-monaural switching operation is perfectly synchronized with a stereo indicator lamp.
- Monitoring of VCO free running frequency can be performed by directly connecting the frequency counter to No. 9 terminal.
- High signal to noise ratio.
  S/N=89 dB TYP., at V_{in}=300 mVr.m.s.
- Wide maximum input level.
  V_{in}=900 mVr.m.s., T.H.D.=1 %.

ABSOLUTE MAXIMUM RATINGS (Ta=25 °C)

Supply Voltage	V_{CC}	15	V
Lamp Current	I_L	75	mA
Package Dissipation	P_D	400*	mW
Operating Temperature	T_{opt}	-20 to +70	°C
Storage Temperature	T_{stg}	-40 to +125	°C

* Ta=70 °C

RECOMMENDED OPERATING CONDITION (Ta=25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	9	12	15	V

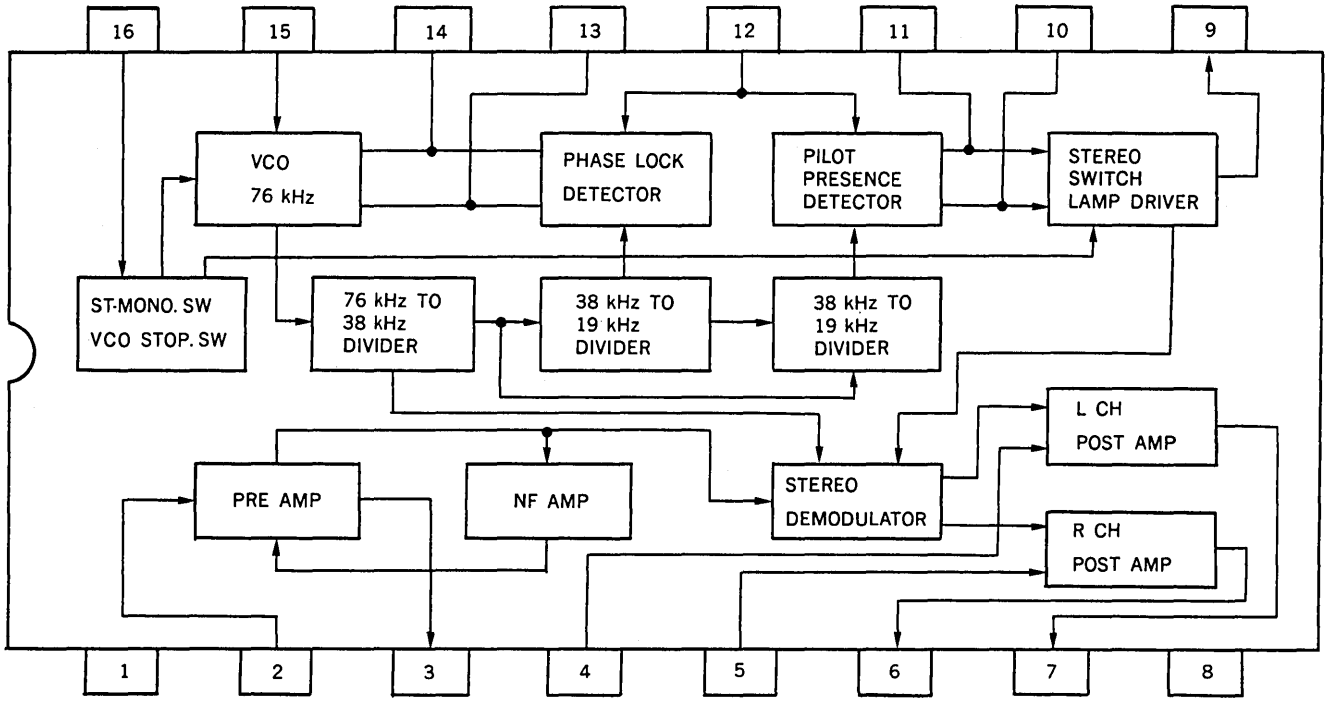
ELECTRICAL CHARACTERISTICS (Ta=25 °C)

(V_{CC}=12 V, f=1 kHz, R_1=47 kΩ, R+L=270 mVr.m.s., Pilot=30 mVr.m.s.)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION	
Supply Current	I_{CC}	12	20	30	mA	Non Signal	
Channel Separation	Sep.	40	50		dB	Pilot=30 mVr.m.s.	f=100 Hz
		45	55		dB		f=1 kHz
		35	45		dB		f=10 kHz
Voltage Gain	A_V	8	12	16	dB	Monaural, *V_{in}=300 mVr.m.s.	
Channel Balance	C.B.	−1.5	0	1.5	dB	Monaural, V_{in}=300 mVr.m.s.	
		−1.5	0	1.5	dB	Stereo, Pilot=30 mVr.m.s.	
Monaural Total Harmonic Distortion	T.H.D.		0.01	0.08	%	V_{in}=300 mVr.m.s.	
Stereo Total Harmonic Distortion	T.H.D.		0.02		%	R+L=270 mVr.m.s. Pilot=30 mVr.m.s.	f=100 Hz
			0.02	0.1	%		f=1 kHz
			0.12		%		f=10 kHz
Pilot Level for Lamp On	L−ON	6	12	20	mVr.m.s.	Pilot Level, R_1=47 kΩ	
Stereo Lamp Hysteresis	Hy.		6		dB	Pilot Level	
Capture Range	C.R.	±1.5	±3		%	Pilot=30 mVr.m.s.	
Ultrasonic Frequency Rejection	19 kHz. Rej.		35		dB	Pilot=30 mVr.m.s.	
	38 kHz. Rej.		45		dB	Pilot=30 mVr.m.s.	
SCA Rejection	SCA Rej.		70		dB	Pilot=30 mVr.m.s., SCA=30 mVr.m.s.	
Maximum Input Level	V_{in}		0.9		Vr.m.s.	Monaural, T.H.D.=1 %	
Signal To Noise Ratio	S/N	81	89		dB	V_{in}=300 mVr.m.s., After LPF	
Stereo-Monaural Switching SW-ON Voltage	V_s		1.4	1.6	V	No. 16 Terminal Voltage Where Stereo Lamp-OFF	
VCO Stop Voltage	V_o	7		V_{CC}	V	No. 16 Terminal Voltage Where VCO Stops	

* A_V is obtained from the output level measured at the output terminals of the IC.
A_V can be varied by R_1 which is the input impedance of the IC.

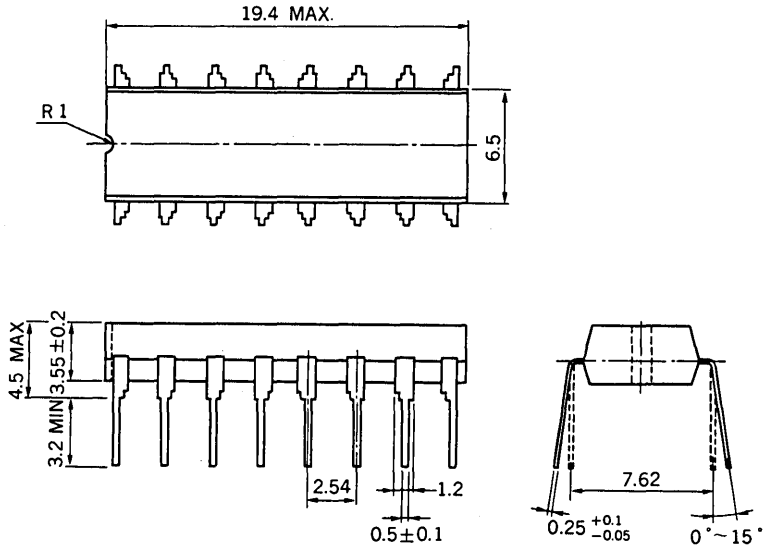
FUNCTIONAL BLOCK DIAGRAM



TERMINAL CONNECTION

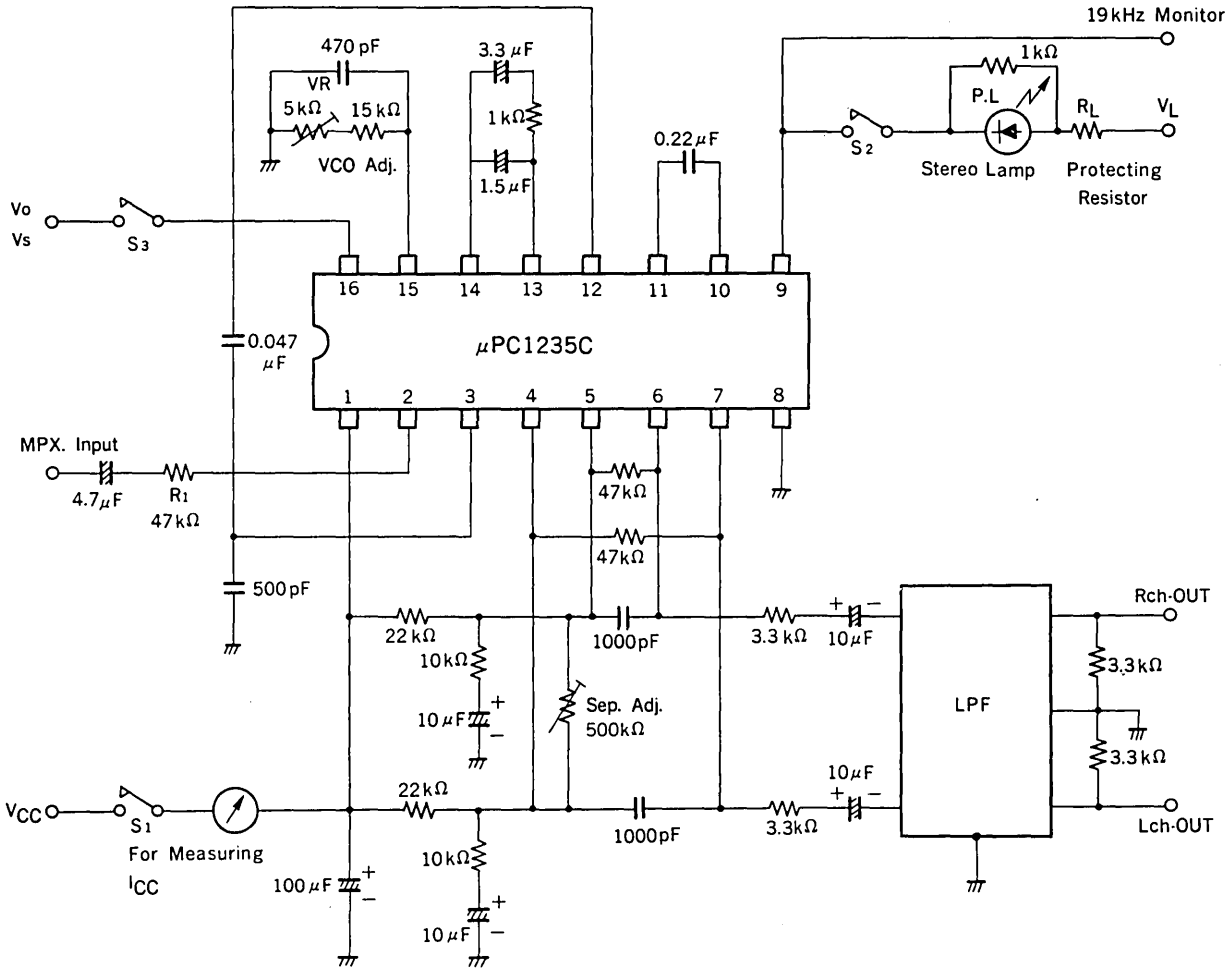
No.	CONNECTION	No.	CONNECTION
1	V_{CC}	9	ST. LAMP & 19 kHz MONITOR
2	PRE AMP INPUT	10	LOW PASS FILTER
3	PRE AMP OUTPUT	11	LOW PASS FILTER
4	POST AMP BIAS	12	DETECTOR INPUT
5	POST AMP BIAS	13	LOOP FILTER
6	R-CH OUTPUT	14	LOOP FILTER
7	L-CH OUTPUT	15	OSC RC. NETWORK
8	GND	16	ST.-MONO. SW & VCO STOP

PACKAGE DIMENSIONS (Unit: mm)



NOTE: Numerical values show TYP. values unless otherwise designated.

TEST CIRCUIT FOR ELECTRICAL CHARACTERISTICS

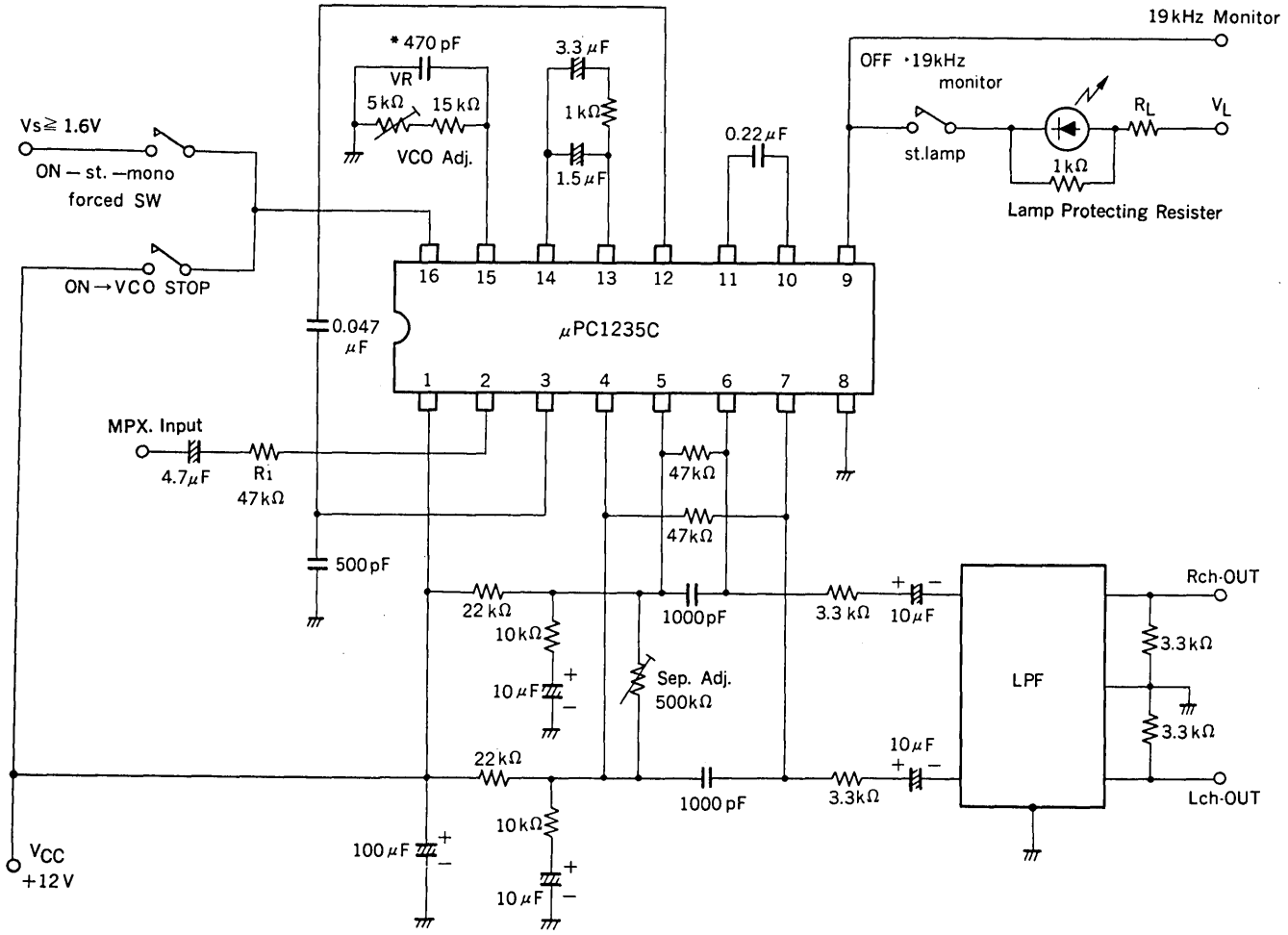


LPF	BL-13 (K.K KORIN)
VCO Adj.	VCO tuning semi-fixed potentiometer
Sep. Adj.	Separation adjusting semi-fixed potentiometer
S_1	V_{CC} ON-OFF SW
S_2	SW for 19 kHz monitor
S_3	SW for VCO stop

NOTES:

1. Use polystyrene capacitors for that connected to No. 15 terminal to compensate the temperature coef. of VCO.
2. For adjusting the VCO oscillation frequency, make S_2 open, connect the frequency counter to No. 9 terminal 19 kHz monitor and then set by varying the semi-fixed potentiometer VCO Adj. connected to No. 15 terminal.
3. For separation adjustment, vary the semi-fixed potentiometer Sep. Adj. connected between terminals No. 4 and No. 5 to set at the best point.

TYPICAL APPLICATION



LPF	BL-13 (K.K KORIN)
VCO Adj.	VCO tuning semi-fixed potentiometer
Sep. Adj.	Separation adjusting semi-fixed potentiometer
*470 pF	Polystyrene capacitor

NOTES:

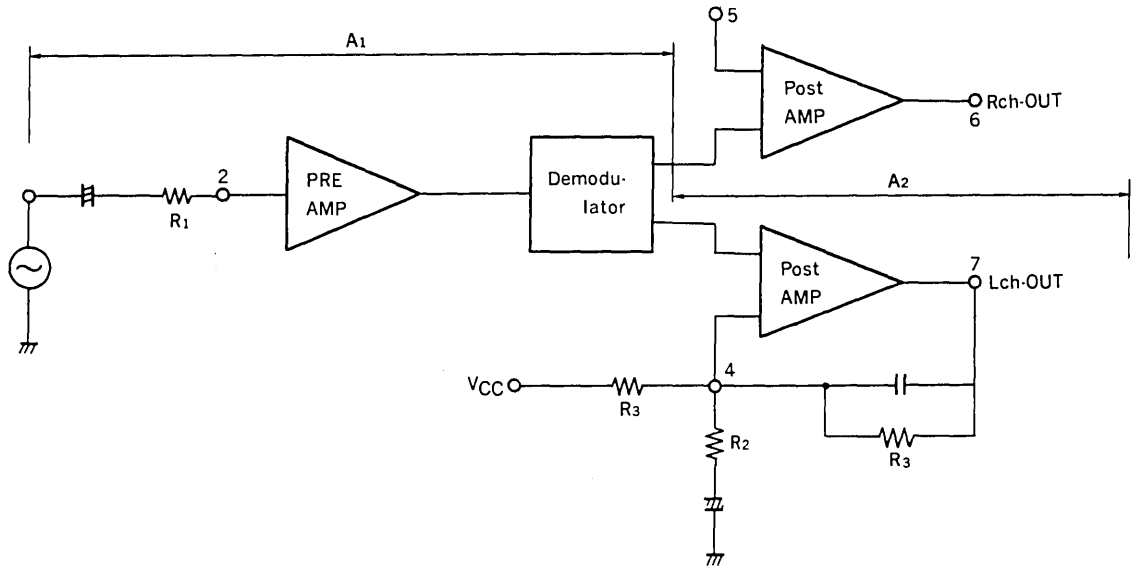
When the unit is used with power supply voltage of less than 12 V, the mid-point electric potential of the output terminals 6, 7 in the above typical application may change and Total Harmonic Distortion at output terminal will increase.
In this case change the bias registor 47 kΩ between terminals 5, 6 and terminals 4, 7 and keep at mid-point electric potential.

ON CIRCUIT GAIN

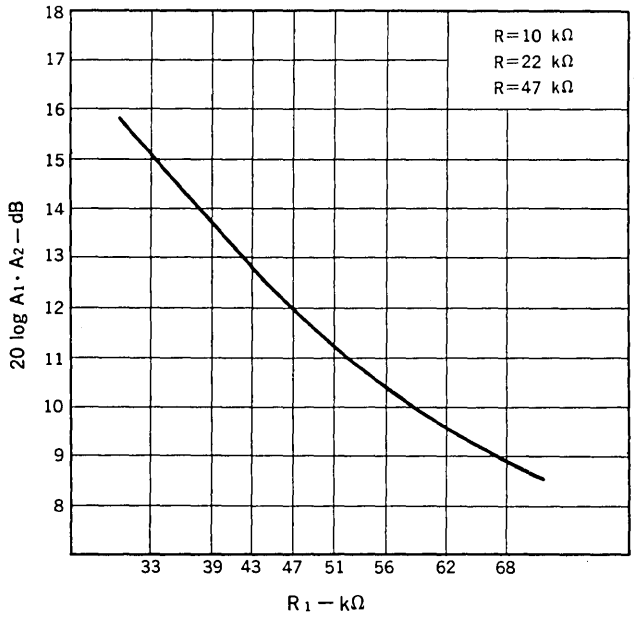
The circuit gain of the μPC1235C is obtained from, the input stage PRE AMP., the demodulator, and output stage POST AMP., and can be expressed equivalently from external resister ratio by following equation:

$$A_1 \fallingdotseq \frac{24}{R_1}, \quad A_2 \fallingdotseq \frac{(R_3 /\!/ R_2) + R_3}{R_3 /\!/ R_2}$$

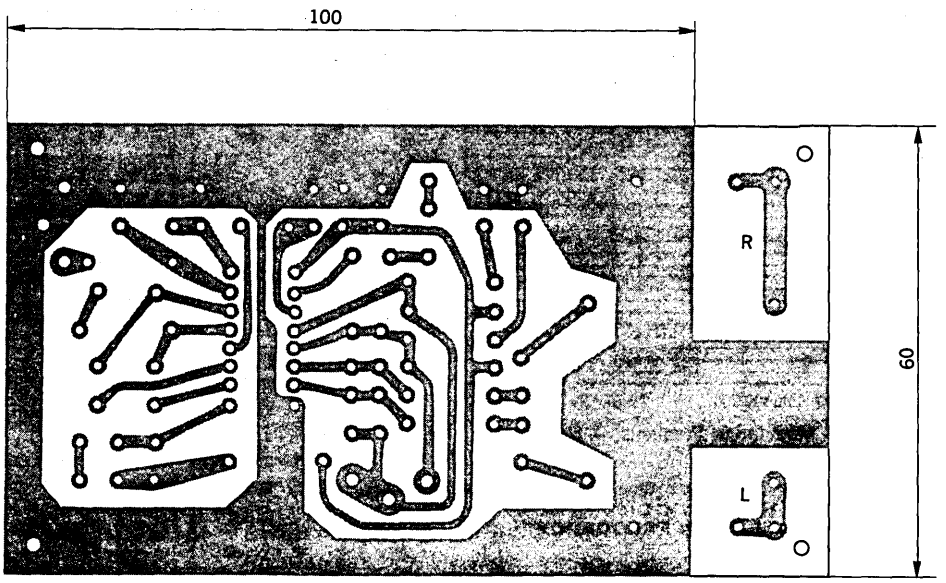
$$A_V \fallingdotseq 20 \log (A_1 \cdot A_2) \quad (dB)$$



The change of the circuit gain in case an input resister R_1 has been varied is shown in the following drowing.

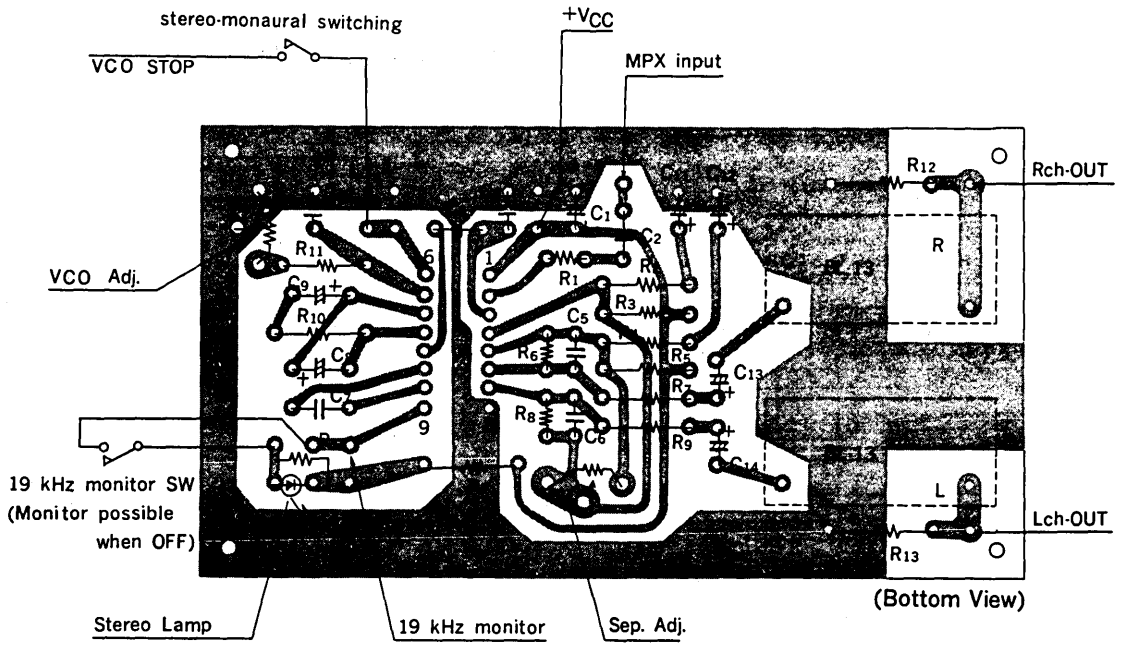


EXAMPLE OF PRINTED-CIRCUIT BOARD (Unit: mm)



(Bottom View)

OUTBOARD COMPONENTS MOUNTED ON A PRINTED-CIRCUIT BOARD

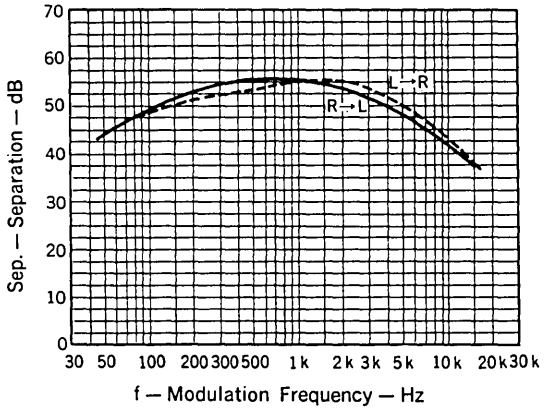


(Bottom View)

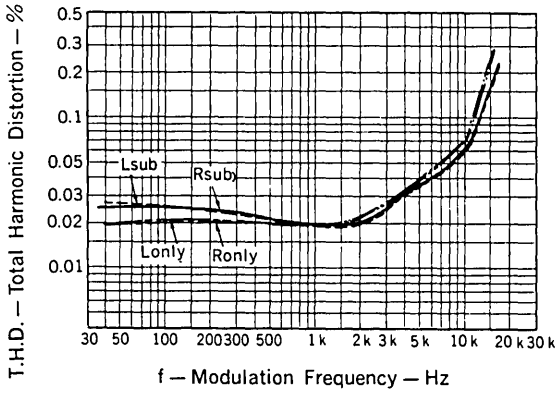
R_1=47 kΩ	R_6 =47 kΩ	R_{11}=15 kΩ	C_1=100 μF	C_6 =1 000 pF	C_{11}=10 μF	Sep. Adj. =500 kΩ VR
R_2=10 kΩ	R_7 =3.3 kΩ	R_{12}=3.3 kΩ	C_2=4.7 μF	C_7 =0.22 μF	C_{12}=10 μF	VCO Adj. =5 kΩ VR
R_3=22 kΩ	R_8 =47 kΩ	R_{13}=3.3 kΩ	C_3=500 pF	C_8 =1.5 μF	C_{13}=10 μF	BL-13=19 kHz LPE(K.K KORIN)
R_4=10 kΩ	R_9 =3.3 kΩ	R_{14}=1.0 kΩ	C_4=0.047 μF	C_9 =3.3 μF	C_{14}=10 μF	
R_5=22 kΩ	R_{10}=1.0 kΩ	R_L =Lamp Protecting Resistor	C_5=1 000 pF	C_{10}=470 pF(Polystyrene capacitor)		

TYPICAL PERFORMANCE CHARACTERISTICS

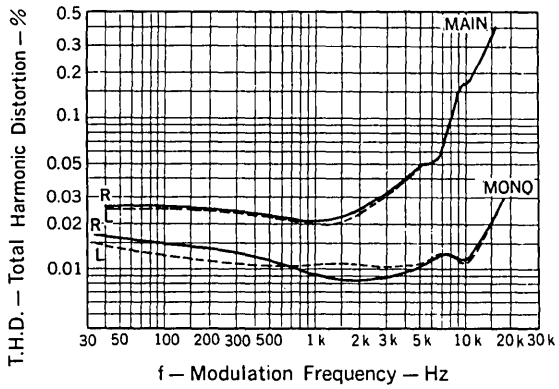
SEPARATION vs.
MODULATION FREQUENCY



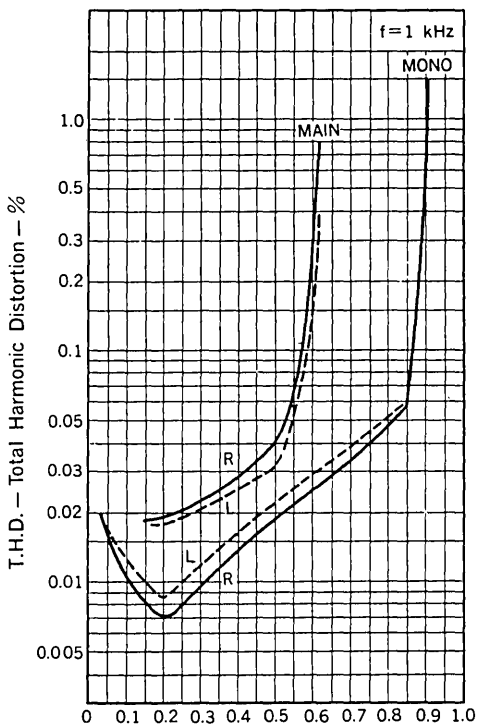
TOTAL HARMONIC DISTORTION
vs. MODULATION FREQUENCY
(STEREO)



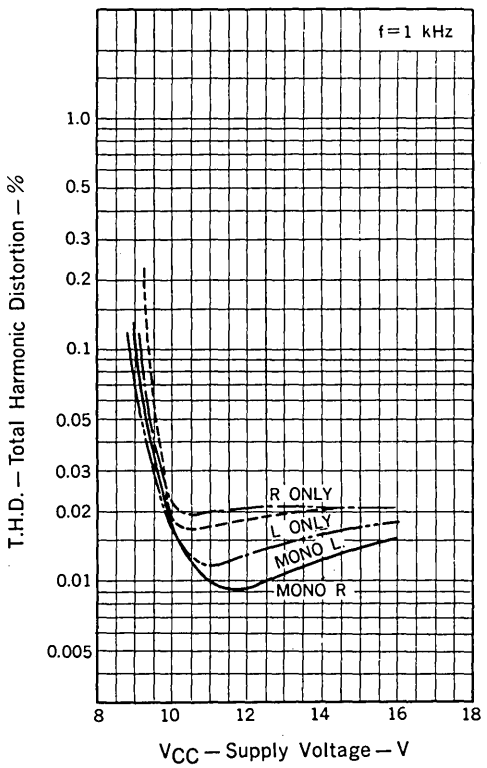
TOTAL HARMONIC DISTORTION
vs. MODULATION FREQUENCY



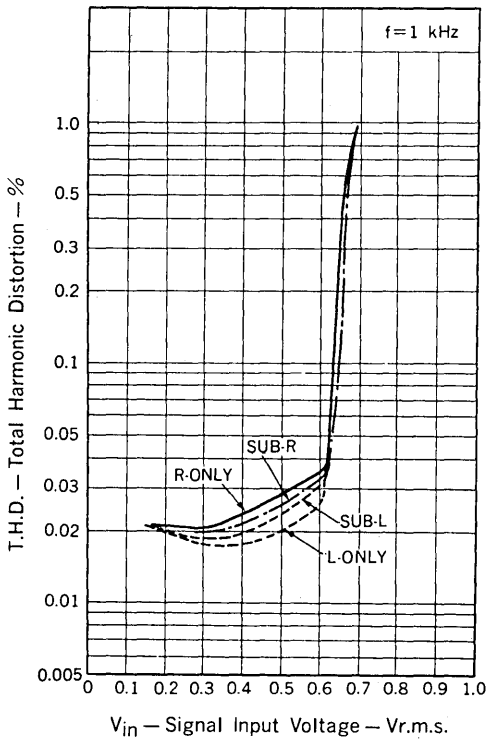
TOTAL HARMONIC DISTORTION vs.
MAIN SIGNAL INPUT VOLTAGE



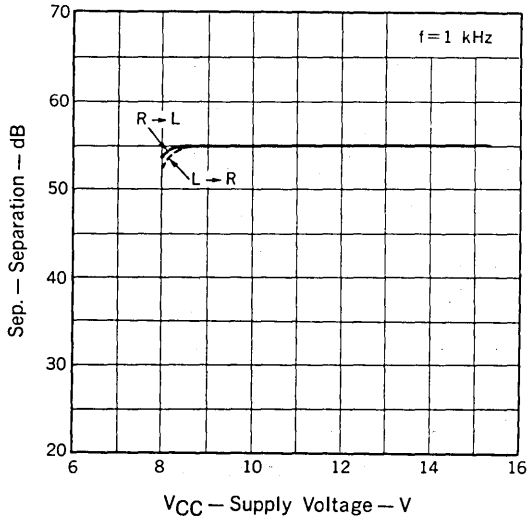
TOTAL HARMONIC DISTORTION vs.
SUPPLY VOLTAGE



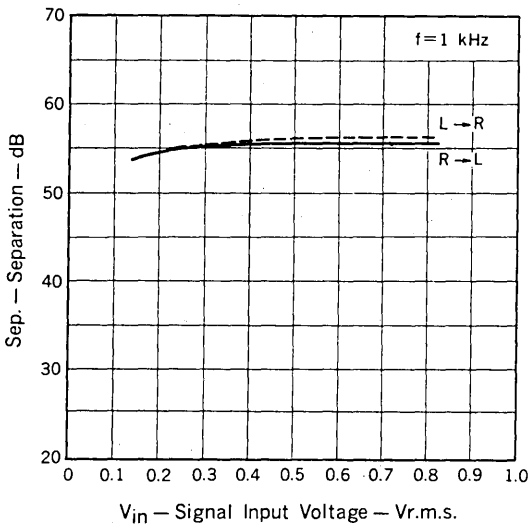
TOTAL HARMONIC DISTORTION vs. MAIN SIGNAL INPUT VOLTAGE



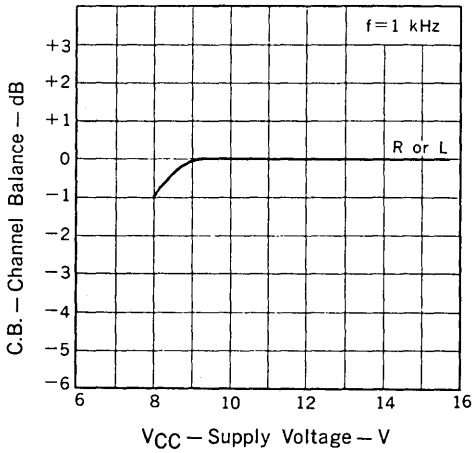
SEPARATION vs. SUPPLY VOLTAGE



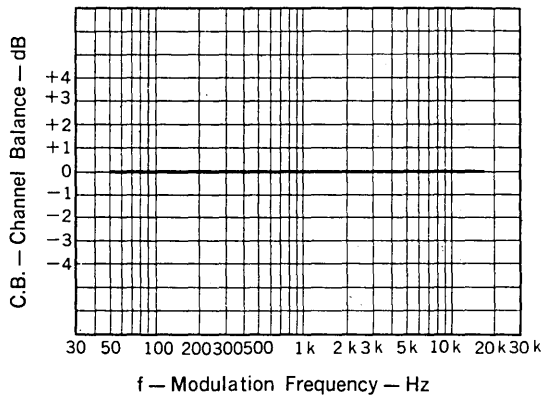
SEPARATION vs. SIGNAL INPUT VOLTAGE



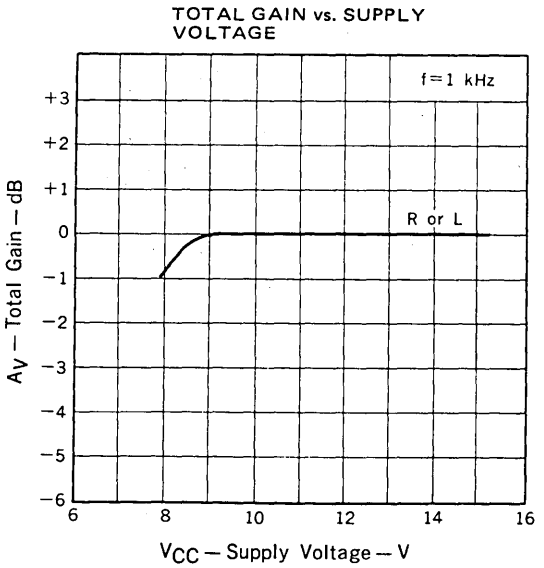
CHANNEL BALANCE vs. SUPPLY VOLTAGE



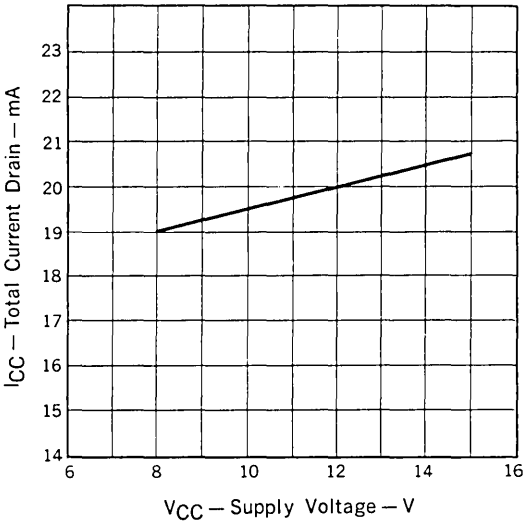
CHANNEL BALANCE vs. MODULATION FREQUENCY



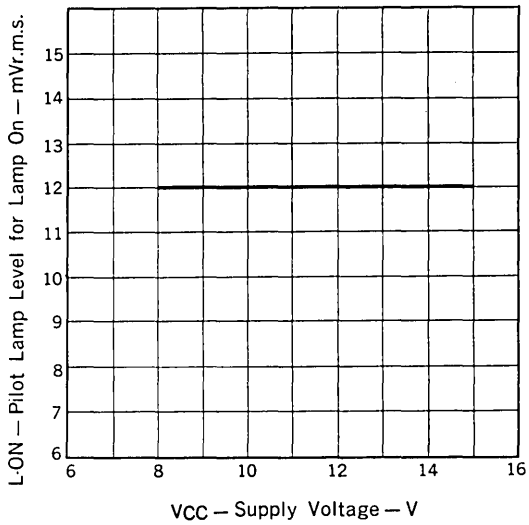
TOTAL GAIN vs. SUPPLY VOLTAGE



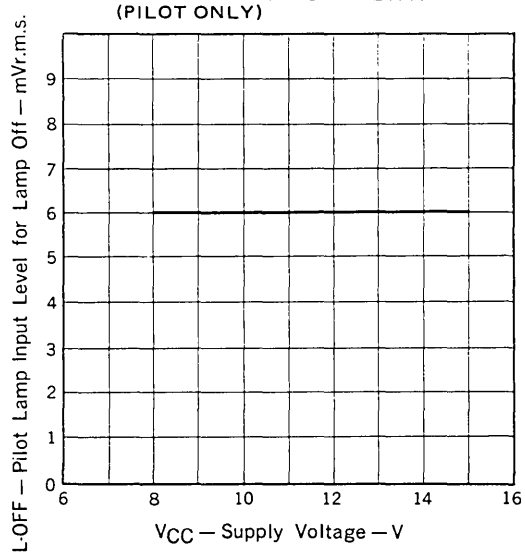
TOTAL CURRENT DRAIN vs. SUPPLY VOLTAGE (NO SIGNAL)



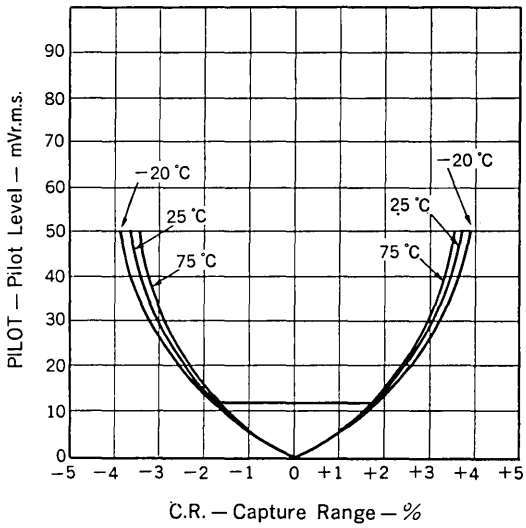
PILOT LAMP INPUT LEVEL FOR LAMP OFF vs. SUPPLY VOLTAGE (PILOT ONLY)



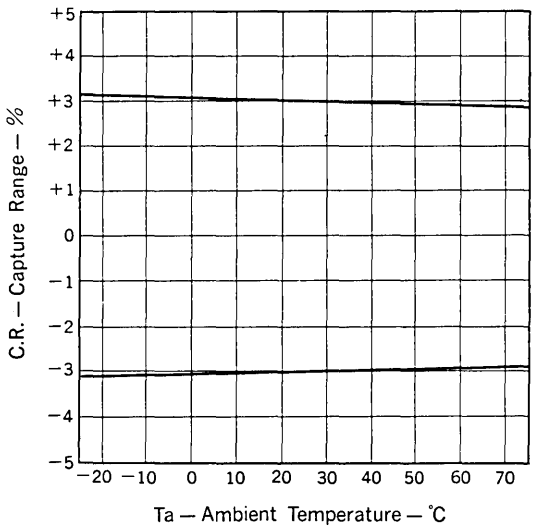
PILOT LAMP INPUT LEVEL FOR LAMP ON vs. SUPPLY VOLTAGE (PILOT ONLY)



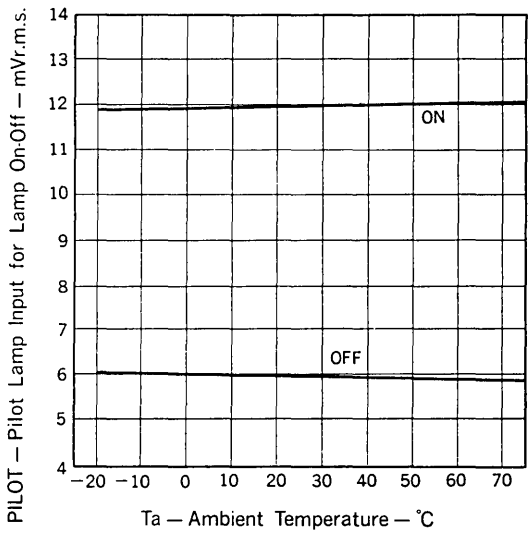
PILOT LEVEL AND AMBIENT TEMPERATURE vs. CAPTURE RANGE



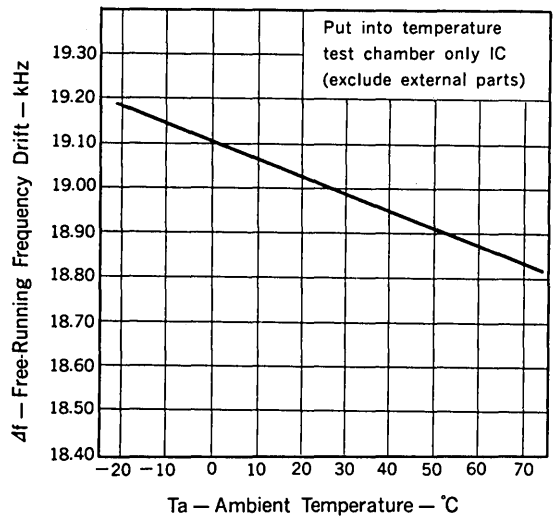
CAPTURE RANGE vs. AMBIENT TEMPERATURE (PILOT=30 mVr.m.s.)



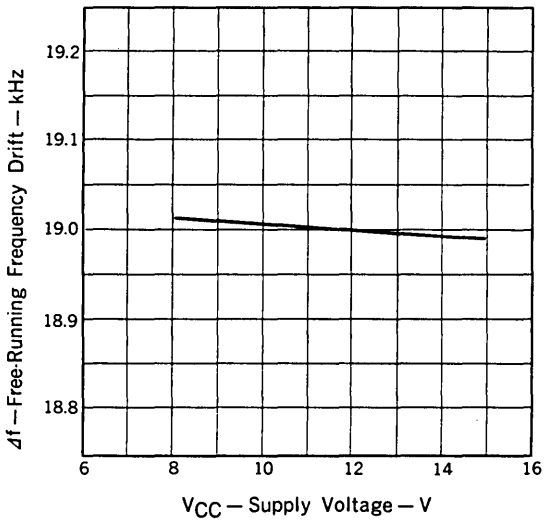
PILOT LAMP INPUT LEVEL FOR LAMP ON-OFF vs. AMBIENT TEMPERATURE



FREE-RUNNING FREQUENCY DRIFT vs. AMBIENT TEMPERATURE



FREE-RUNNING FREQUENCY DRIFT vs. SUPPLY VOLTAGE



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1224H

HIGH SUPPLY VOLTAGE LOW NOISE DUAL PRE AMPLIFIER

DESCRIPTION

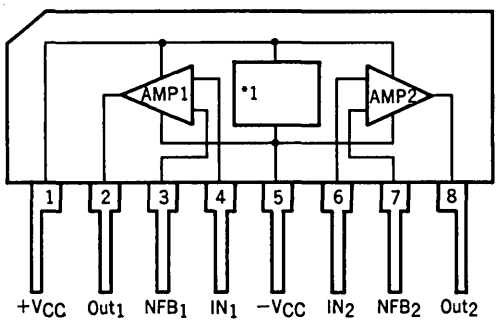
The μPC1224H is a monolithic integrated circuit and a dual pre amplifier designed for the low-end class to the middle class Hi-Fi audio sets and in an 8-pin single in-line plastic (SIP) package.

The circuit inside of μPC1224H is composed of the two stage differential amplifiers acting as a voltage amplifier stage and the SEPP (Single End Push Pull) circuit acting as a final stage.

FEATURES

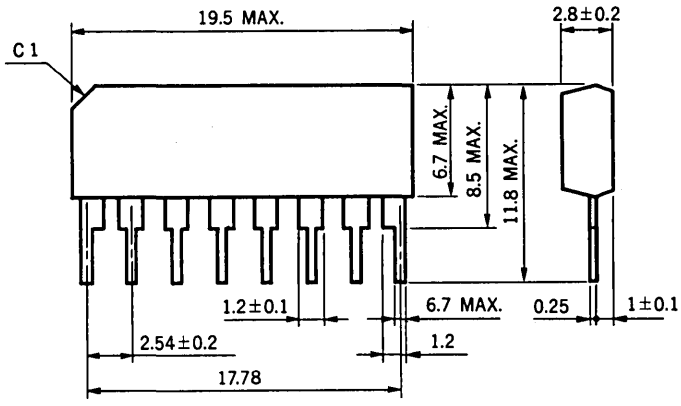
- μPC1224H has a dual pre amp in an 8-pin SIP package, so that it has a merit of design and assembly of small sets.
- Very low noise. 0.815 μVr.m.s. TYP. (R_G = 0 Ω, A_V = 36 dB at 1 kHz, RIAA, without Filter)
- Low distortion. 0.002 4 % TYP. (V_{CC} = ± 22 V, V_O = 1 Vr.m.s., R_L = 10 kΩ, f = 1 kHz)
- Wide input dynamic range. 222 mVr.m.s. TYP.
  (V_{CC} = ± 22 V, T.H.D. = 0.1 %, f = 1 kHz, A_V = 36 dB)
- μPC1224H can drive a lower impedance load because its final stage is the SEPP circuit.

BLOCK DIAGRAM & CONNECTION DIAGRAM



*1 Regulated Power Supply

PACKAGE DIMENSIONS (Unit : mm)



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Supply Voltage	V_{CC}		± 25	V
Allowable Power Dissipation	P_D	Ta = 65 °C	330	mW
Differential Mode Input Voltage	V_{ID}		±10	V
Common Mode Input Voltage	V_{ICM}		to ± V_{CC}	V
Operating Temperature	T_{opt}		−20 to +65	°C
Storage Temperature	T_{stg}		−40 to +125	°C

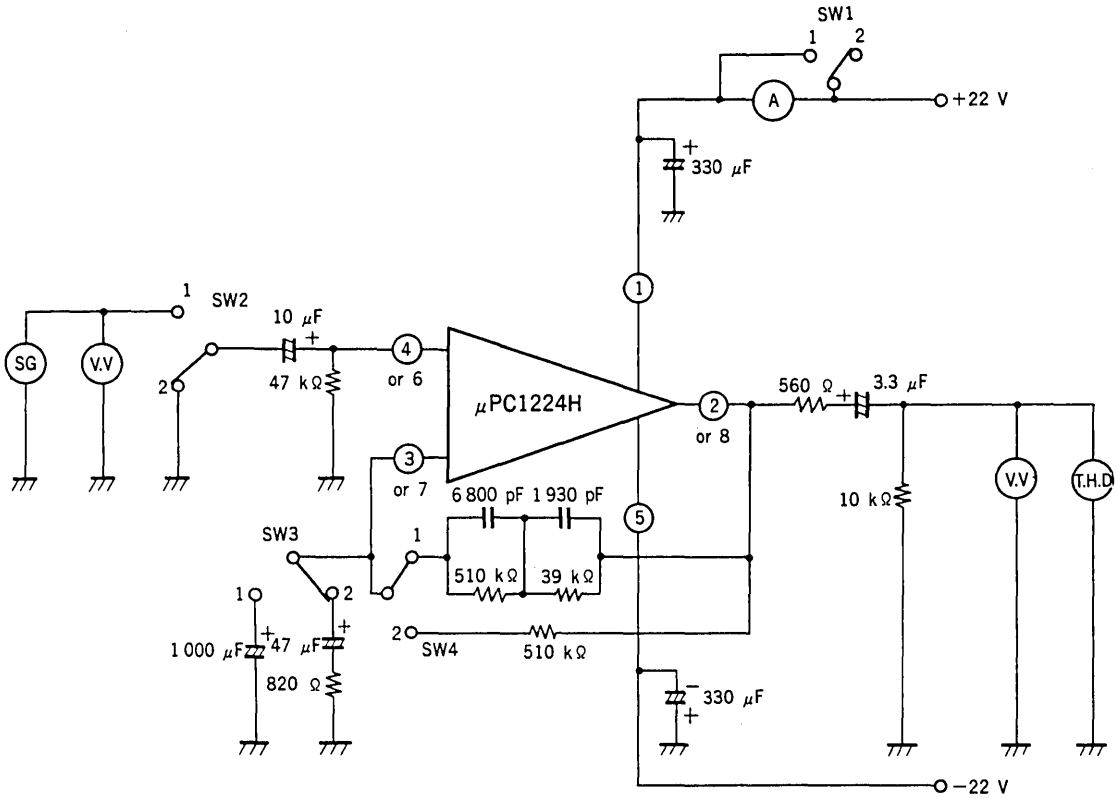
RECOMMENDED OPERATING CONDITIONS (Ta = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	±10	±22	± 24	V
Input Bias Resistance	R_{IN}	20	50	100	kΩ
Load Impedance	R_L	1	10	100	kΩ
Closed Loop Voltage Gain	A_V	15	36		dB

ELECTRICAL CHARACTERISTICS (V_{CC} = ±22 V, R_L = 10 kΩ, A_v = 36 dB, RIAA, Ta = 25 °C)

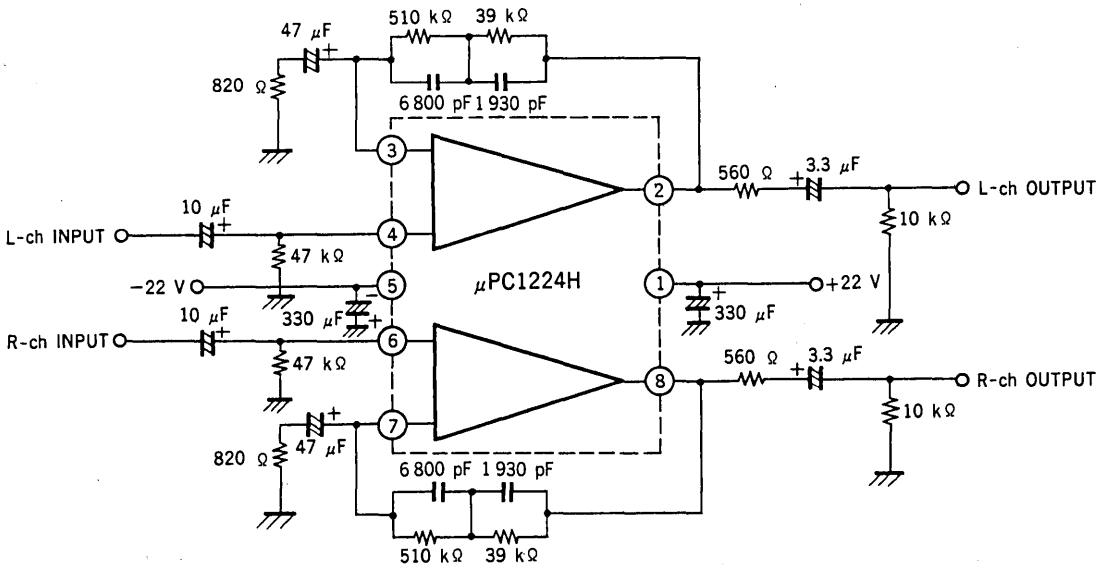
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Quiscent Circuit Current	I_{CC}		3	5.5	mA	
Open Loop Voltage Gain	A_{VO}	80	100		dB	V_O = 0.1 Vr.m.s.
Total Harmonic Distortion	T.H.D.		0.0024	0.03	%	V_O = 1 Vr.m.s., f = 1 kHz
Maximum Output Voltage	V_{OM}	12	14		Vr.m.s.	T.H.D. = 0.1 %, f = 1 kHz
Equivalent Input Noise Level	N_L		0.8	1.6	μVr.m.s.	R_g = 0 Ω, without Filter
Common Mode Reduction Ratio	C.M.R.		90		dB	R_{IN} ≦10 kΩ
Supply Voltage Reduction Ratio	SVR		65 25	(+) (−)	dB	R_{IN} ≦10 kΩ, f_{ripple} = 100 Hz
Channel Separation	$C_{h.sep.}$		90		dB	V_O = 10 Vr.m.s., f = 1 kHz

TEST CIRCUIT



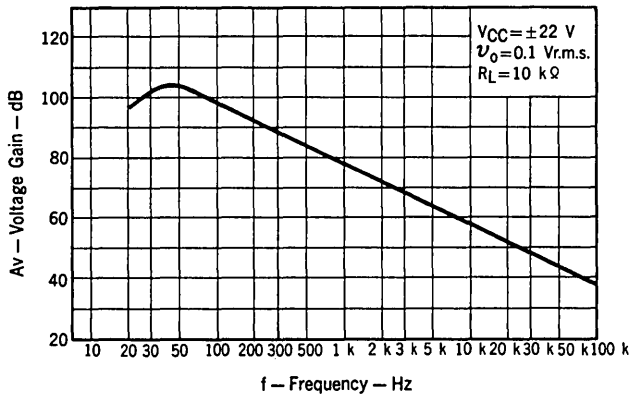
	SW1	SW2	SW3	SW4
I_{CC}	2	2	2	1
A_{vO}	1	1	1	2
T.H.D.	1	1	2	1
V_{OM}	1	1	2	1
N_L	1	2	2	1

TYPICAL APPLICATION CIRCUIT

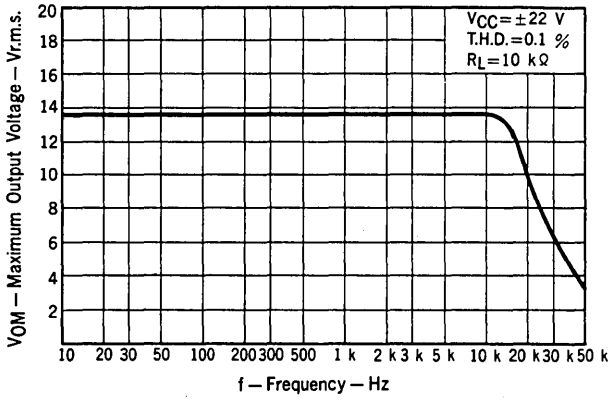


TYPICAL CHARACTERISTIC

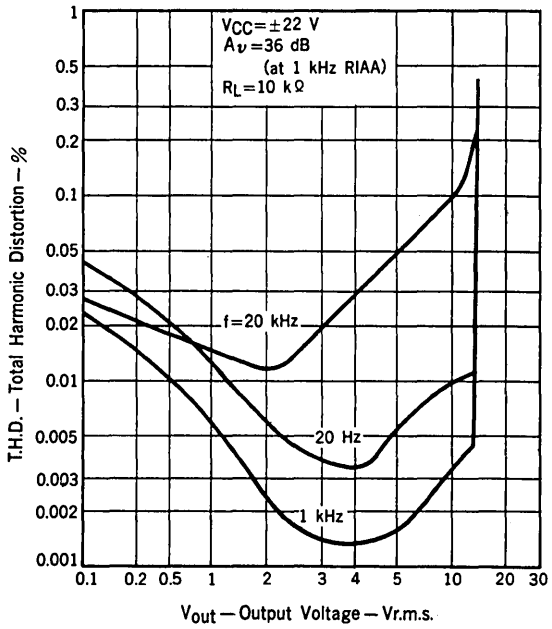
VOLTAGE GAIN vs. FREQUENCY



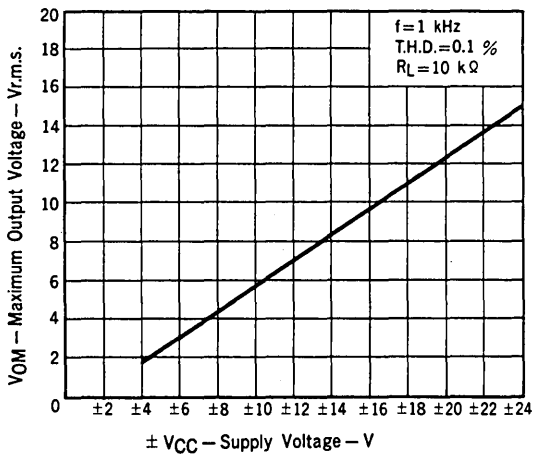
MAXIMUM OUTPUT VOLTAGE vs. FREQUENCY



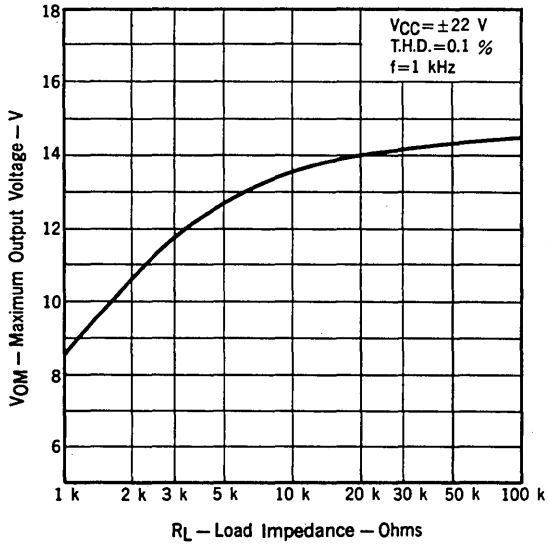
TOTAL HARMONIC DISTORTION vs. OUTPUT VOLTAGE



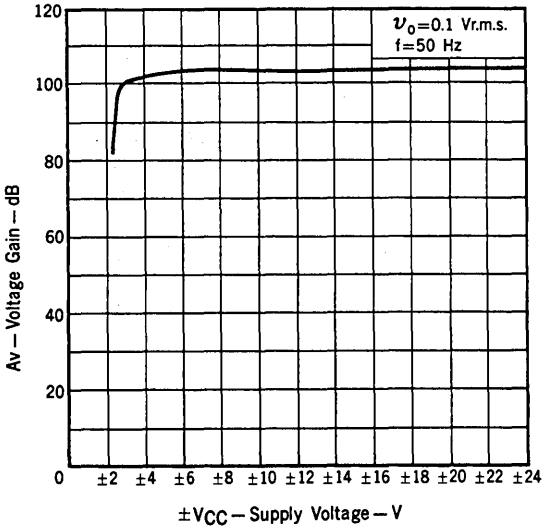
MAXIMUM OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



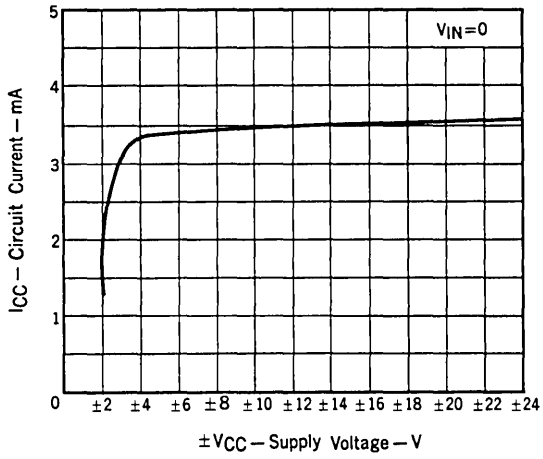
MAXIMUM OUTPUT VOLTAGE vs. LOAD INPEDANCE



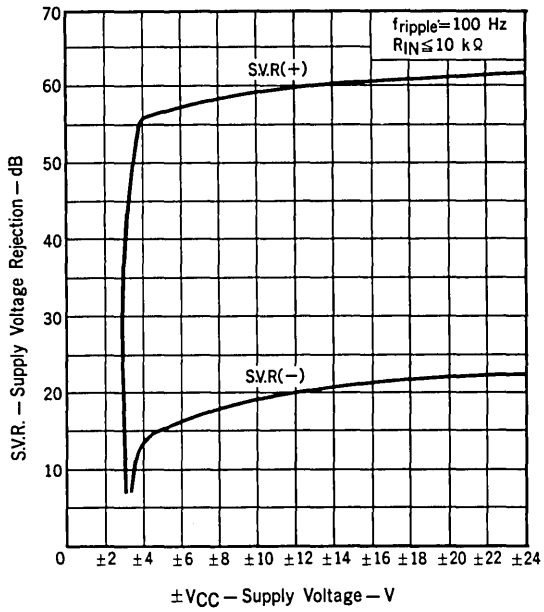
VOLTAGE GAIN vs. SUPPLY VOLTAGE



CIRCUIT CURRENT vs.
SUPPLY VOLTAGE



SUPPLY VOLTAGE REJECTION
vs. SUPPLY VOLTAGE



CHANNEL SEPARATION vs. FREQUENCY

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1188H

20 W AUDIO POWER AMPLIFIER

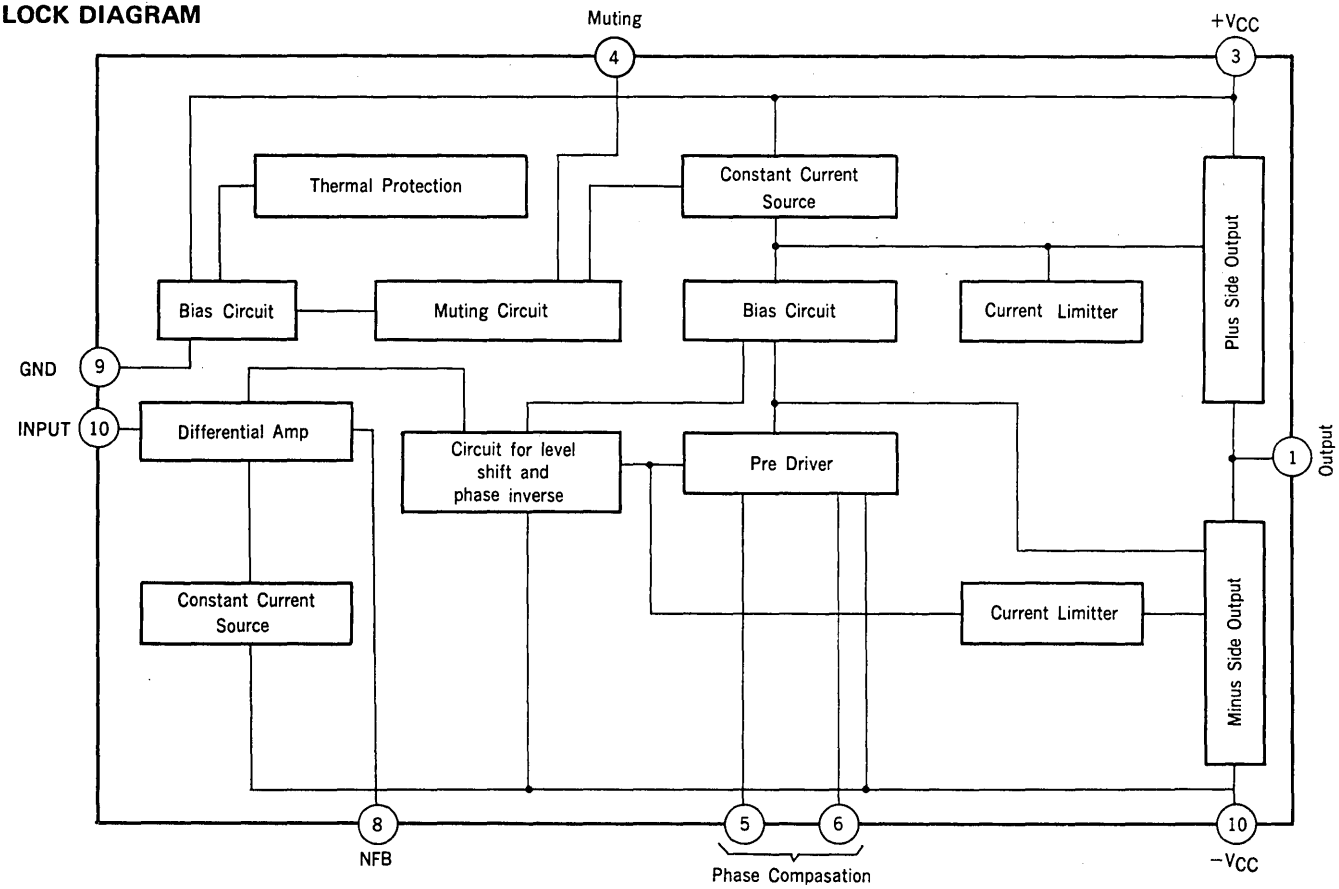
DESCRIPTION

The μPC1188H is a monolithic integrated circuit and a power amplifier designed for Hi-Fi audio sets and in a 10pin Single In-Line plastic package. μPC1188H can provide 20 W (TYP.) to 8 ohms at 1 % T.H.D. and ± 22 V Supply voltage.

FEATURES

- High output power. 20 W TYP. (V_{CC} = ± 22 V, A_V = 40 dB, f = 20 Hz ~ 20 kHz, R_L = 8 Ω, T.H.D. = 1 %)
  20 W TYP. (V_{CC} = ± 22 V, A_V = 27.5 dB, f = 20 Hz ~ 20 kHz, R_L = 8 Ω, T.H.D. = 0.5 %)
- Low distortion. 0.02 % TYP. (V_{CC} = ± 22 V, A_V = 40 dB, f = 1 kHz, R_L = 8 Ω, P_{out} = 5.0 W)
  0.005 % TYP. (V_{CC} = ± 22 V, A_V = 27.5 dB, f = 1 kHz, R_L = 8 Ω, P_{out} = 5.0 W)
- Wide frequency band width. f = 250 kHz (−3 dB)
- μPC1188H has a muting function which eliminates pop on noise and the thermal and the over current protection circuit.
- Available for NFB tone control amp.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Supply Voltage (Quiescent)	V_{CC}	± 30	V
Circuit Current	$I_{CC(peak)}$	5	A
Package Dissipation	P_D	30*	W
Operating Temperature	T_{opt}	−20 to +70	°C
Storage Temperature	T_{stg}	−55 to +150	°C
Thermal Resistance Junction to Case	$R_{th(j-c)}$	3	°C/W

* T_{tab}=60°C

RECOMMENDED OPERATING CONDITIONS (Ta = 25 °C)

CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage	±17	±22	±23	V
Input Impedance	47	56	100	kΩ
Closed Loop Voltage Gain	26	40		dB
Load Impedance	4	8		Ω

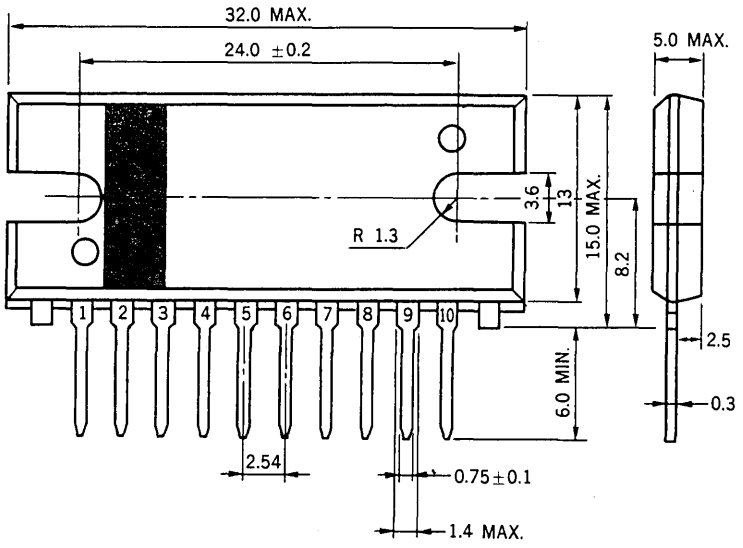
ELECTRIC CHARACTERISTICS (V_{CC} = ±22 V, A_V = 40 dB, R_L = 8 Ω, R_G = 600 Ω, Ta = 25°C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Offset Voltage	V_{IO}	−100	0	+100	mV	No Signal
Circuit Current	I_{CC}	30	60	120	mA	No Signal
Output Power	P_O	16	18		W	T.H.D. = 0.5 %, f = 20 Hz – 20 kHz
Open Loop Voltage Gain	A_{VO}	65	75		dB	P_O = 0.3 W, f = 1 kHz
Total Harmonic Distortion	T.H.D.		0.1	0.3	%	P_O = 10 W, f = 20 Hz – 20 kHz
Output Noise Voltage	NV		0.4	1.0	mV	R_G = 2.2 kΩ, No Filter
Power Band Width	P.B.W.		250		kHz	P_O = 0.3 W, −3 dB
Supply Voltage Rejection Ratio	S.V.R.	50	56		dB	R_G = 2.2 kΩ, fripple = 100 Hz

PACKAGE DIMENSION

Unit: mm

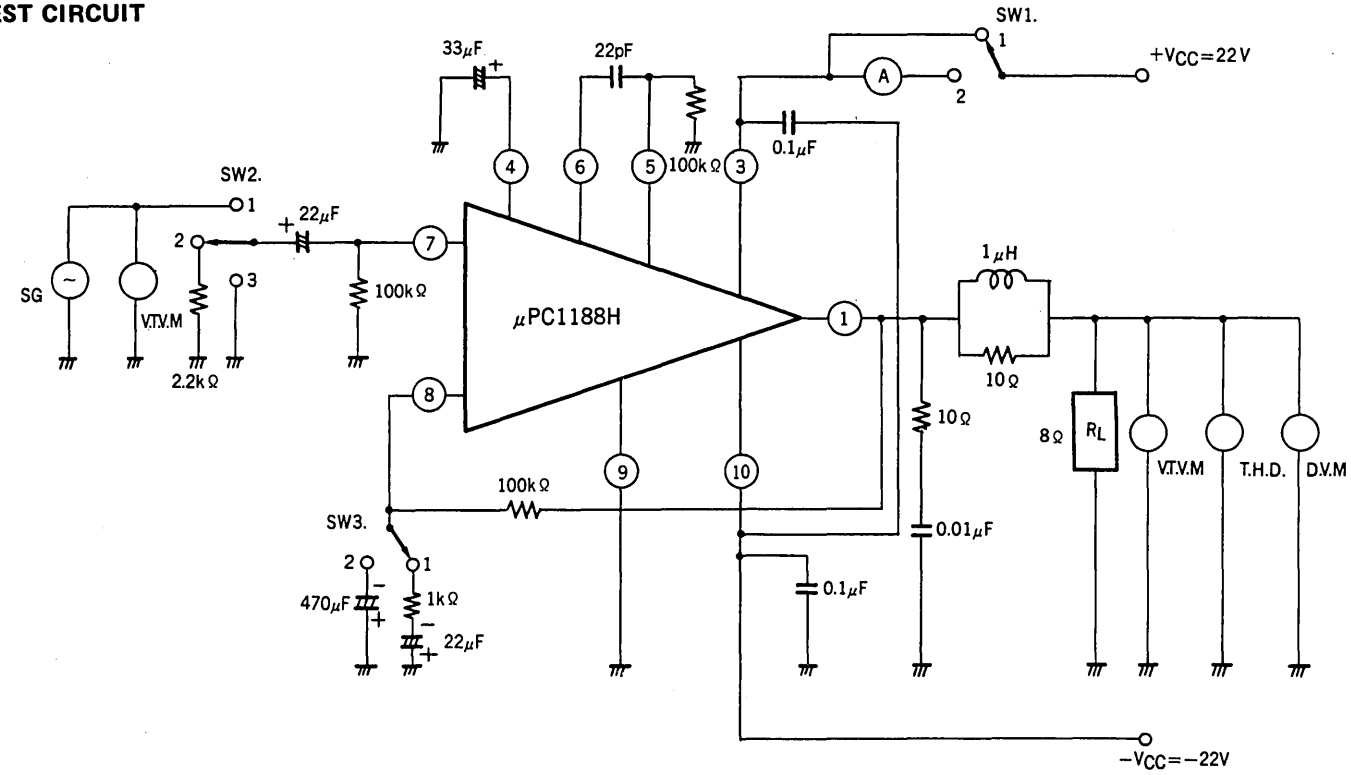
Typical value unless otherwise noted



CONNECTION DIAGRAM

1	OUTPUT
2	NC
3	+V_{CC}
4	MUTING
5	PHASE COMP
6	PHASE COMP
7	INPUT
8	NFB
9	GND
10	−V_{CC}

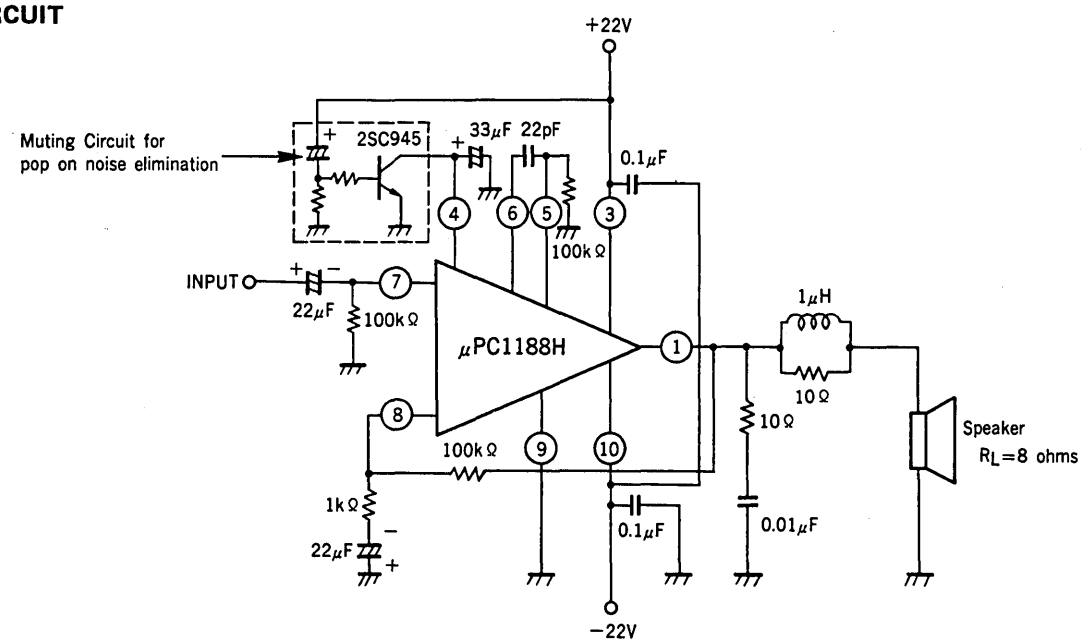
TEST CIRCUIT



NOTE: Turn on plus and minus power supply at the same time or minus power supply at first.

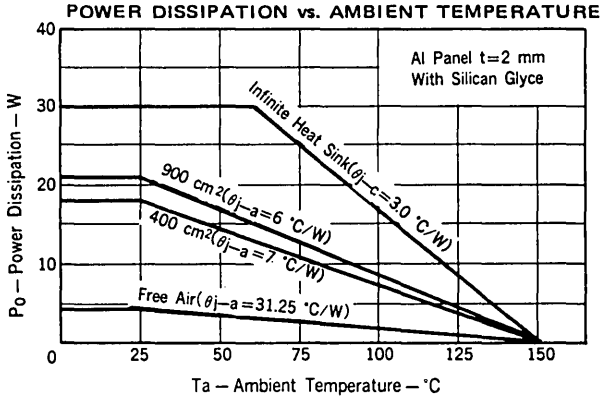
ITEM	SYMBOL	SW1	SW2	SW3
Circuit Current	I_{CC}	2	3	1
Output Offset Voltage	V_{IO}	1	3	1
Output Power	P_O	1	1	1
Open Loop Voltage Gain	A_{VO}	1	1	2
Total Harmonic Distortion	T.H.D.	1	1	1
Output Noise Voltage	NV	1	2	1
Supply Voltage Rejection Ratio	SVR	1	2	1

APPLICATION CIRCUIT

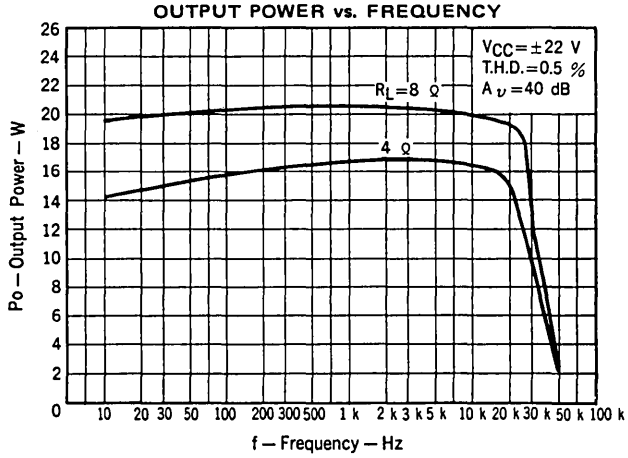


TYPICAL CHARACTERISTICS (Ta = 25 °C)

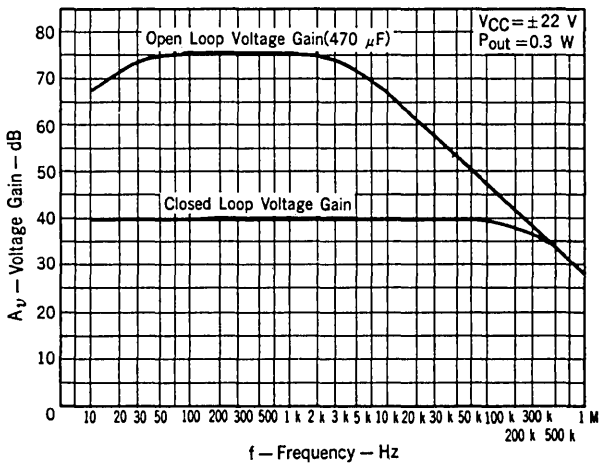
POWER DISSIPATION vs. AMBIENT TEMPERATURE



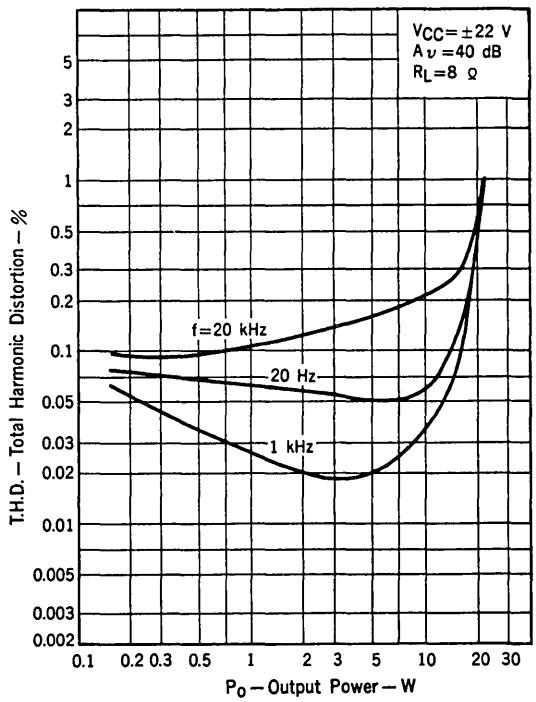
OUTPUT POWER vs. FREQUENCY



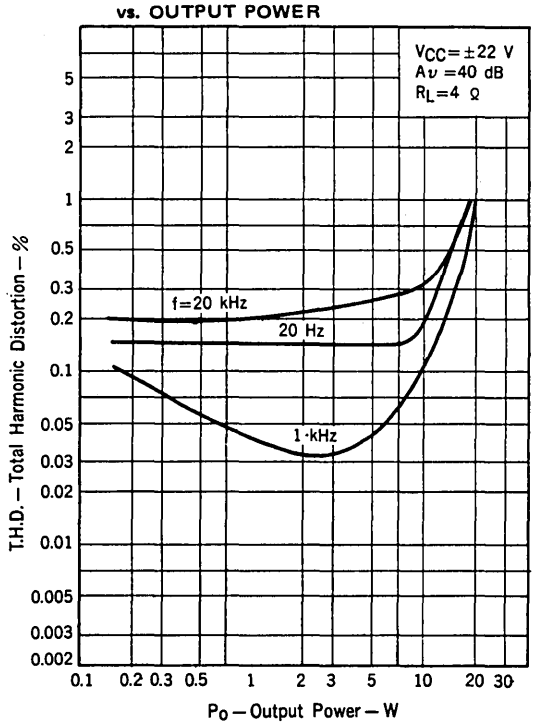
VOLTAGE GAIN vs. FREQUENCY



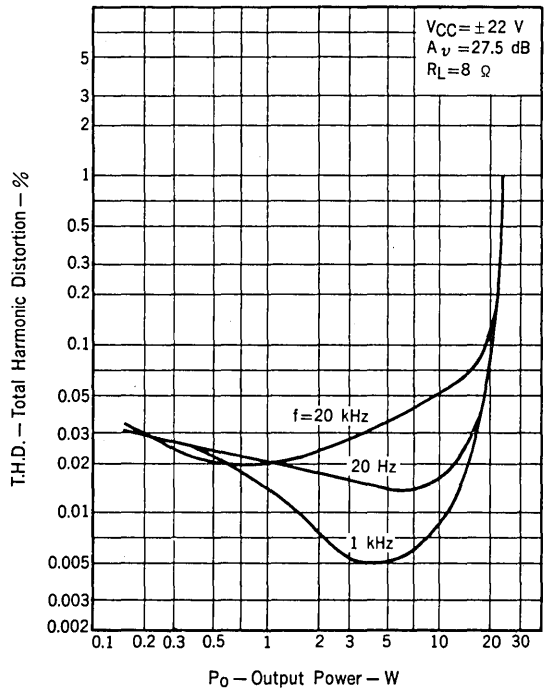
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



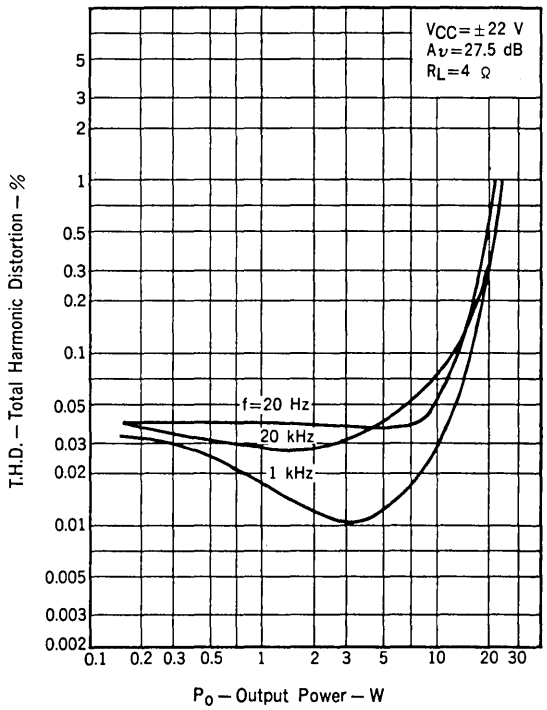
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



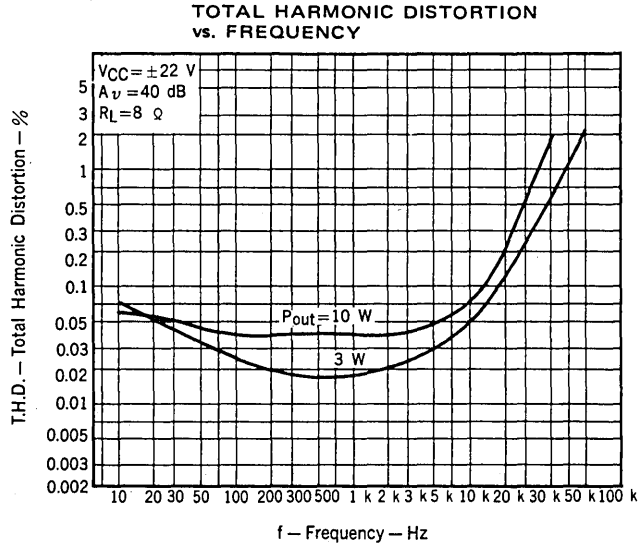
TOTAL HARMONIC DISTORTION
vs. OUTPUT POWER



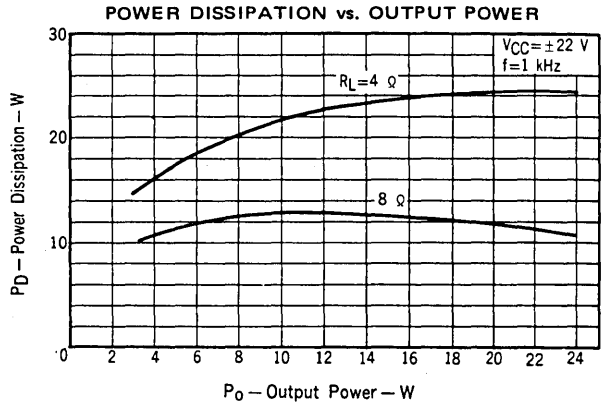
TOTAL HARMONIC DISTORTION
vs. OUTPUT POWER



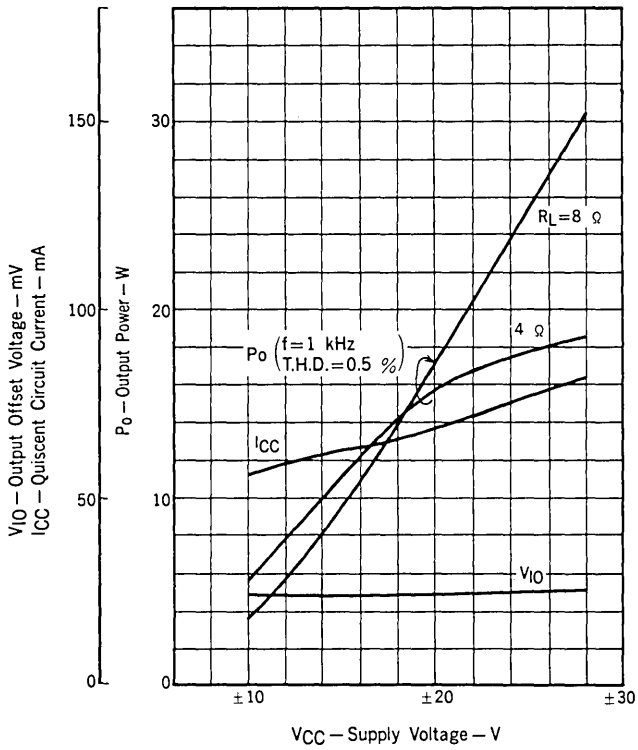
TOTAL HARMONIC DISTORTION
vs. FREQUENCY



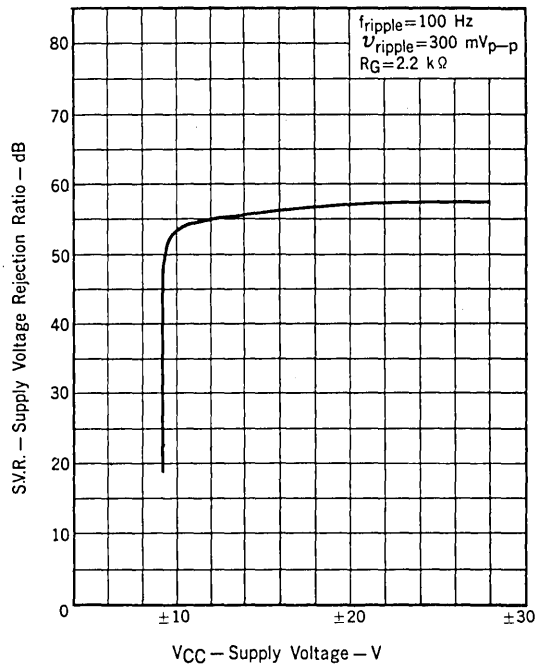
POWER DISSIPATION vs. OUTPUT POWER



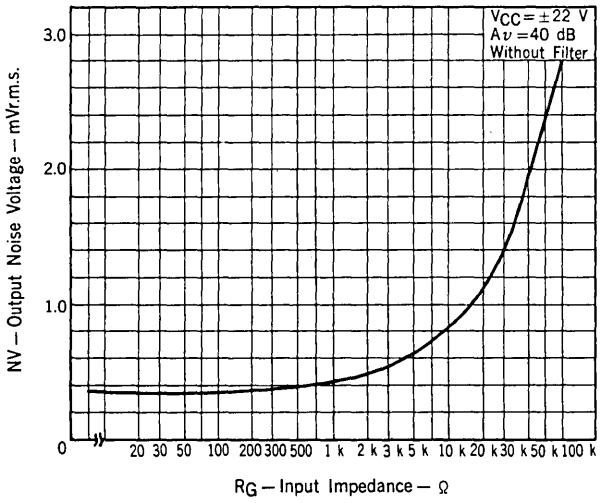
OUTPUT OFFSET VOLTAGE, CIRCUIT CURRENT vs. SUPPLY VOLTAGE



SUPPLY VOLTAGE REJECTION RATIO vs. SUPPLY VOLTAGE



OUTPUT NOISE VOLTAGE vs. INPUT IMPEDANCE



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1238

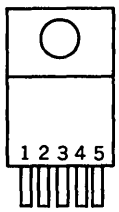
10 W AF POWER AMPLIFIER
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

The μPC1238 is an audio power amplifier designed for median Hi-Fi stereo set and TV set sound power amplifier.
This device can provide 8.4 watts to 8 ohm at 1 % T.H.D. and ±13 V supply voltage.
The μPC1238 incorporates the thermal protection circuit to protect the damage of IC chip against load damping etc.
Since the package is a 5 Pin TO-220 package, it greatly simplifies construction of a power amplifier both in design and assembly.

FEATURES

- High output power
  - 8.4 W TYP. (at 8 Ω, V_{CC} = ±13 V)
  - 12.5 W TYP. (at 4 Ω, V_{CC} = ±13 V)
- Low T.H.D.
  - 0.012 % TYP. (P_{out} = 2 W, R_L = 8 Ω)
  - 0.02 % TYP. (P_{out} = 2 W, R_L = 4 Ω)
- Low equivalent input noise voltage.
- Available for NFB tone control mode.
- Negligible power ON/OFF noise.
- High density components assembly due to 5 Pin TO-220 package.

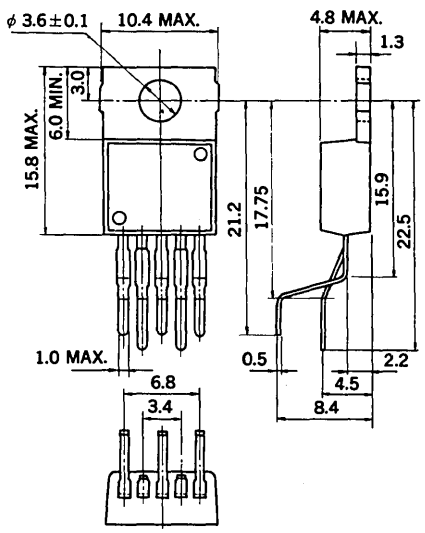
CONNECTION DIAGRAM



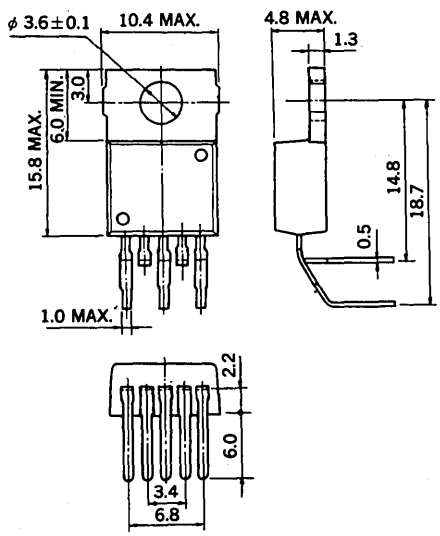
Pin No.	Electrical Connection
1	Non inverting input
2	Inverting input
3	$-V_{CC}$
4	Output
5	$+V_{CC}$

PACKAGE DIMENSIONS (in millimeters)

μPC1238V



μPC1238H



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage (Quiescent)	V_{CC}	±18	V
Supply Voltage (Operational)	V_{CC}	±15	V
Circuit Current	$I_{CC(peak)}$	4	A
Package Dissipation	P_D	*25	W
Junction Temperature	T_j	150	°C
Operating Temperature	T_{opt}	−20 to +65	°C
Storage Temperature	T_{stg}	−40 to +150	°C
Thermal Resistance Junction to Case	$R_{th(j-c)}$	3.4	°C/W

*T_{tab} = 65 °C

RECOMMENDED OPERATING CONDITIONS (T_a = 25 °C)

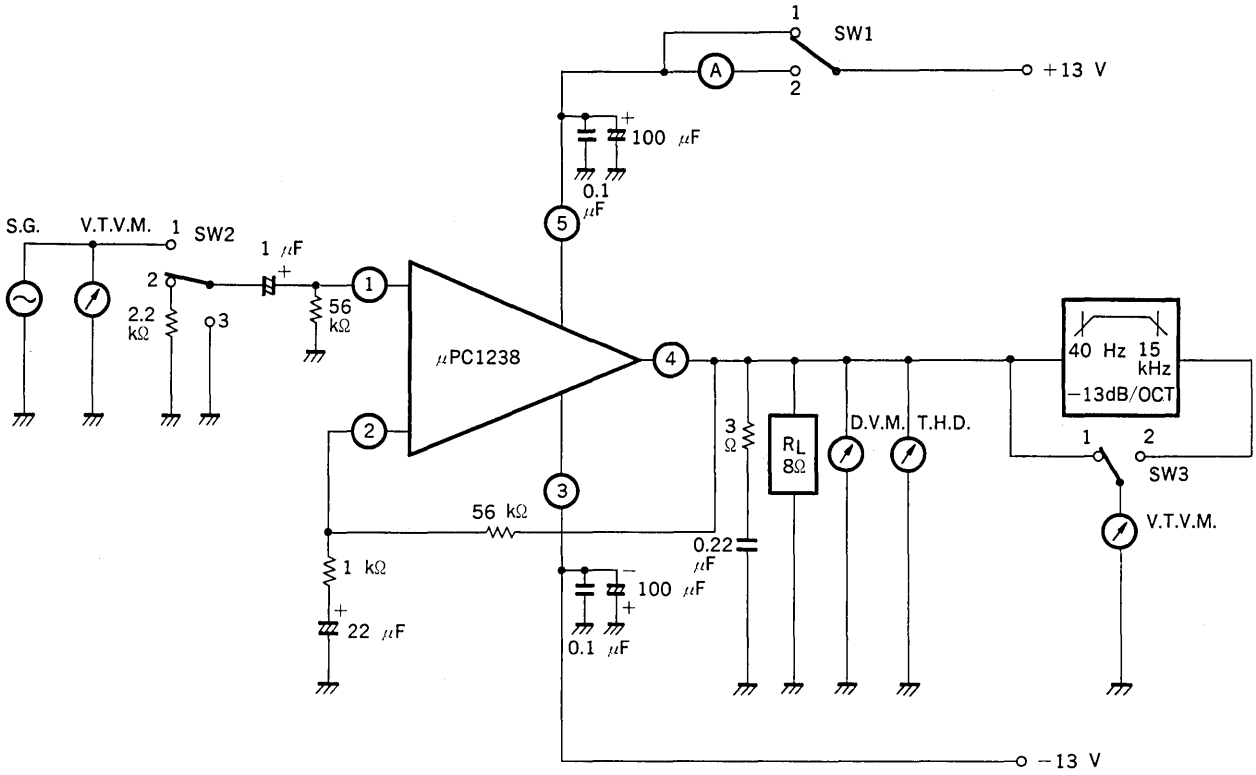
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating Supply	V_{CC}	±6	±13	±15	V
Terminated Input Resistance	R_{IN}	47	56	100	kΩ
Closed Loop Voltage Gain	A_V	20	35		dB
Load Impedance	R_L	4	8		Ω

ELECTRICAL CHARACTERISTICS

(Refer to the test circuit : T_a = 25 °C, V_{CC} = ±13 V, A_V = 35 dB, R_G = 600 Ω, R_L = 8 Ω)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Offset Voltage	V_{OFF}	−100	0	+100	mV	No Signal
Circuit Current	I_{CC}	30	60	130	mA	No Signal
Output Power	P_O	7	8.4		W	T.H.D. = 1 %, f = 1 kHz
Total Harmonic Distortion	T.H.D.		0.2	1	%	f = 40 Hz – 15 kHz P_O = 0.1 –7 W
Open Loop Voltage Gain	A_{vo}		83		dB	P_O = 0.1 W, f = 500 Hz
Equivalent Input Noise Voltage	V_{NI}		3	10	$\mu V_{r.m.s.}$	R_G = 2.2 kΩ f = 40 Hz – 15 kHz(−3 dB)
Power Band Width	P.B.W.		75		kHz	P_O = 0.1 W, −3 dB
Supply Voltage Rejection Ratio	S.V.R.	45	51		dB	f = 100 Hz, R_G = 2.2 kΩ

TEST CIRCUIT & TYPICAL APPLICATIONS

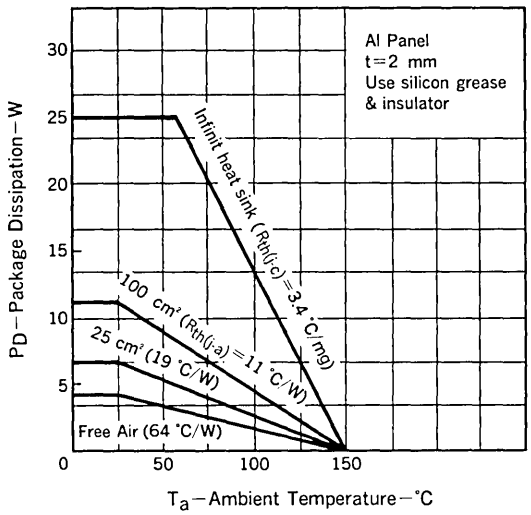


Switch Position

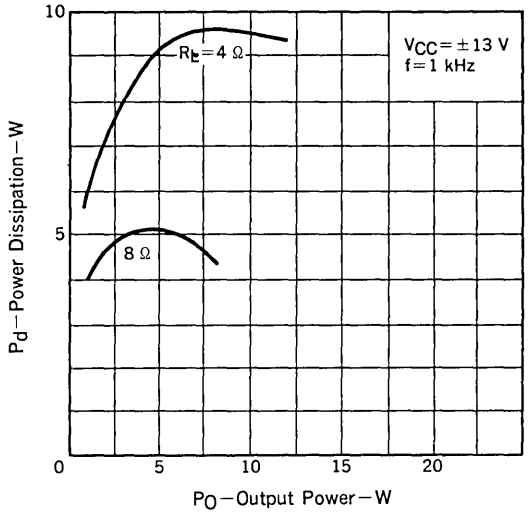
TEST ITEM	SYMBOL	SW1.	SW2.	SW3.
Output Offset Voltage	V_{OFF}	1	3	1
Circuit Current	I_{CC}	2	3	1
Output Power	P_O	1	1	1
Total Harmonic Distortion	T.H.D.	1	1	1
Equivalent Input Noise Voltage	V_{NI}	1	2	2
Supply Voltage Rejection Ratio	S.V.R.	1	2	1

TYPICAL CHARACTERISTICS (T_a = 25 °C)

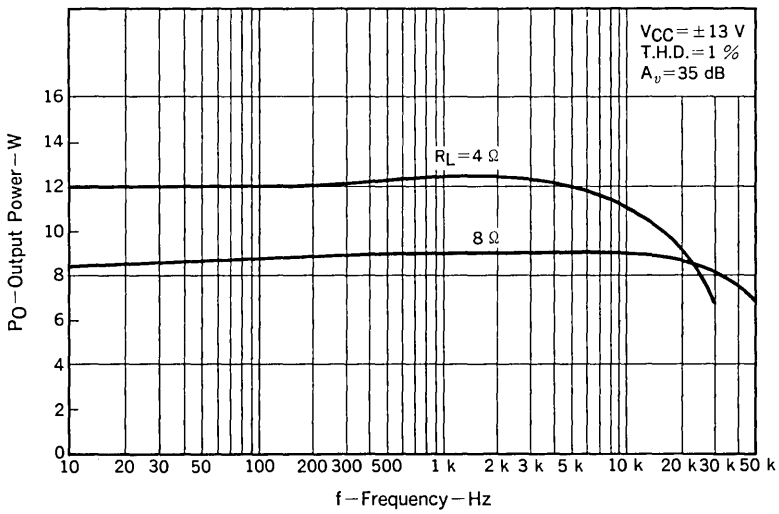
PACKAGE DISSIPATION vs. AMBIENT TEMPERATURE



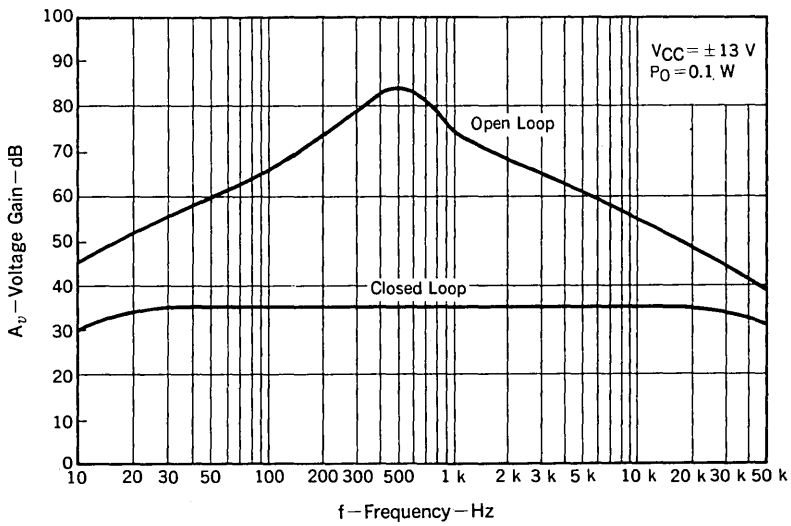
POWER DISSIPATION vs. OUTPUT POWER



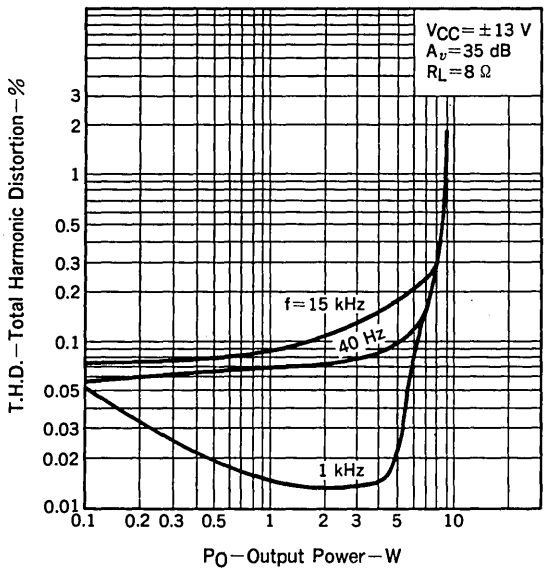
OUTPUT POWER vs. FREQUENCY



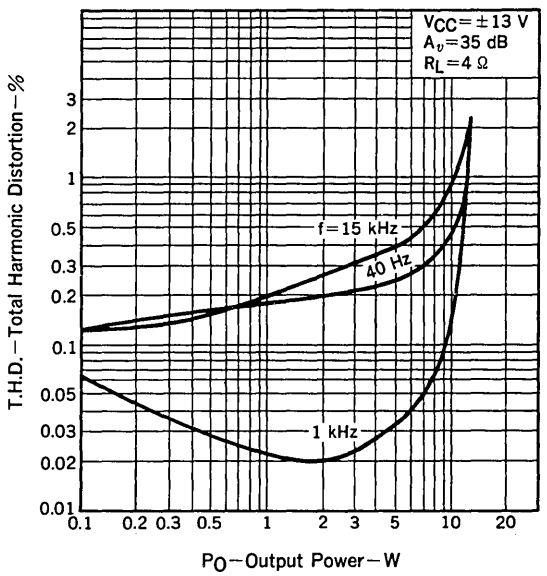
VOLTAGE GAIN vs. FREQUENCY



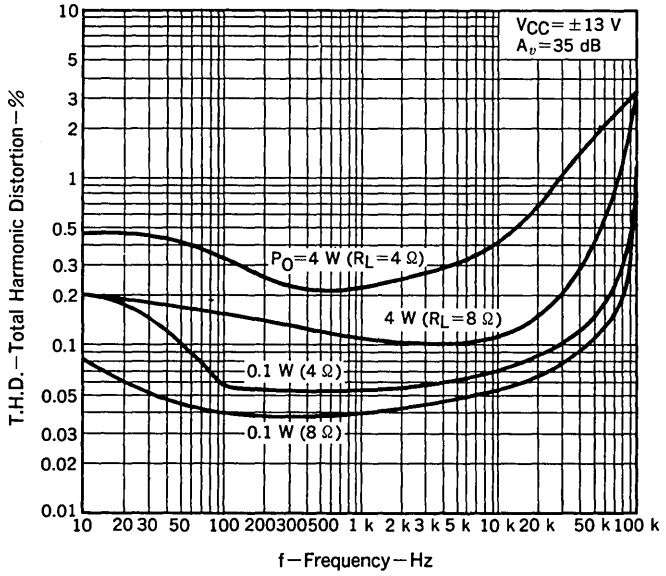
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



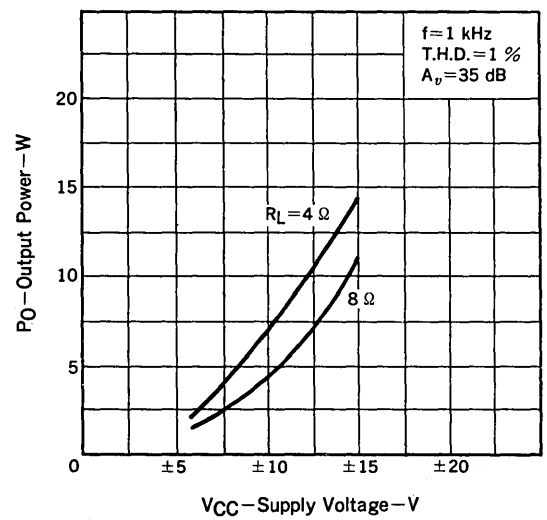
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



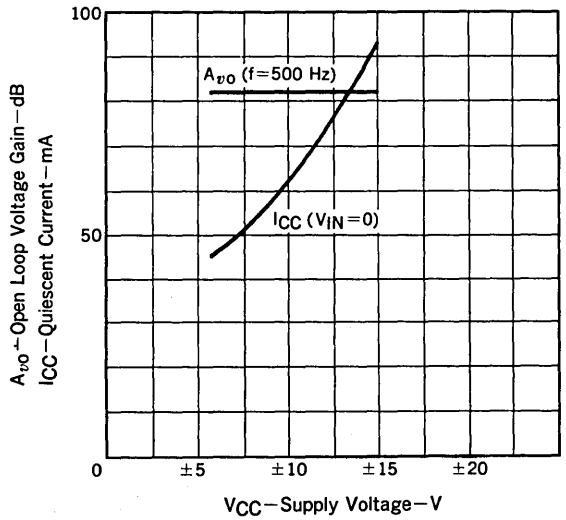
TOTAL HARMONIC DISTORTION vs. FREQUENCY



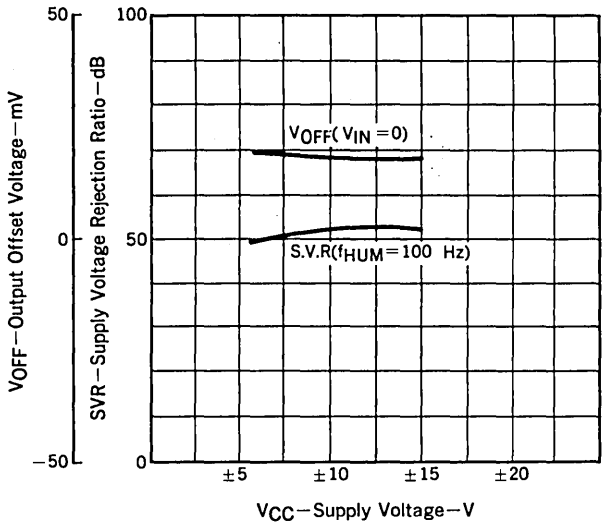
OUTPUT POWER vs. SUPPLY VOLTAGE



OPEN LOOP VOLTAGE GAIN, CIRCUIT CURRENT vs. SUPPLY VOLTAGE



OUTPUT OFFSET VOLTAGE, SUPPLY VOLTAGE REJECTION RATIO vs. SUPPLY VOLTAGE



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1225H

30-50 W POWER AMPLIFIER DRIVER

DESCRIPTION

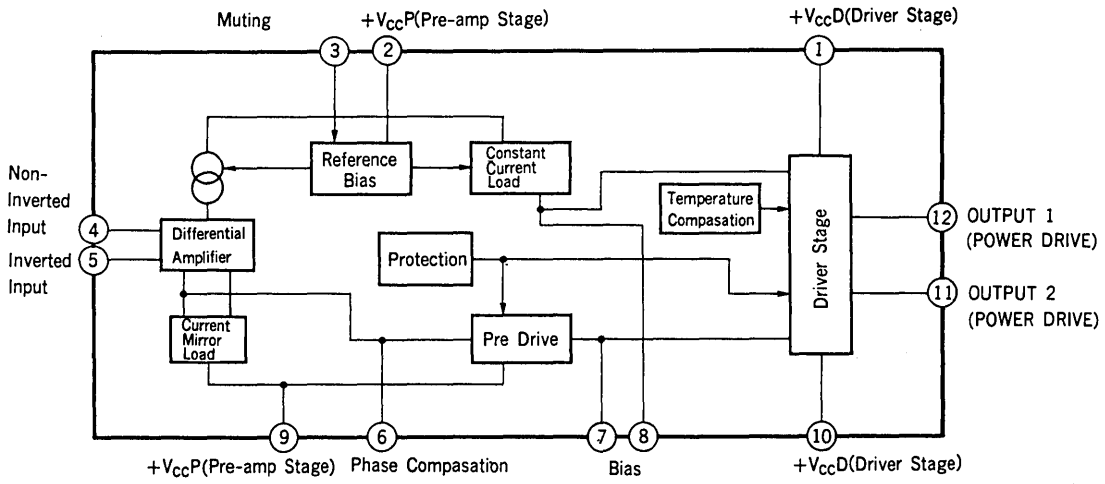
μPC1225H is designed for use with a Hi-Fi power amplifier driver. It is composed of a differential amplifier, a pre driver, a driver and protection circuit.

It is in a 12 pin small power SIP. (Single In Line)

FEATURES

- Excellent Low Distortion
  0.002 % TYP. (V_{CC} = ±36 V, f = 1 kHz, A_V = 30 dB, P_O = 30 W, R_L = 8 Ohms)
  0.006 % TYP. (V_{CC} = ±36 V, f = 20 kHz, A_V = 30 dB, P_O = 30 W, R_L = 8 Ohms)
- Wide Frequency Band
  900 kHz TYP. (-3 dB)
- Wide Power Band Width
  90 kHz TYP. (P_O = 25 W, T.H.D. = 0.1 %)
- Excellent Low POP ON/OFF Noise

BLOCK DIAGRAM



NOTE: The protection circuit is for this IC and cannot protect external Power Transistors. Thus, design a P_O Tr protection circuit besides.

ABSOLUTE MAXMUM RATINGS (Ta = 25 °C)

Supply Voltage (Quiscent)	V_{CC1}	±50	V
Supply Voltage (Operational)	V_{CC2}	±45	V
Quiscent Circuit Current	I_{CC}	200	mA
Allowable Package Dissipation	P_D	4.1*	W
Operational Temperature	T_{opt}	-20 to +75	°C
Storage Temperature	T_{stg}	-40 to +150	°C

*T_a = 75 °C
Using an aluminum heat sink 100 x 100 x 1 mm

RECOMMENDED OPERATING CONDITION

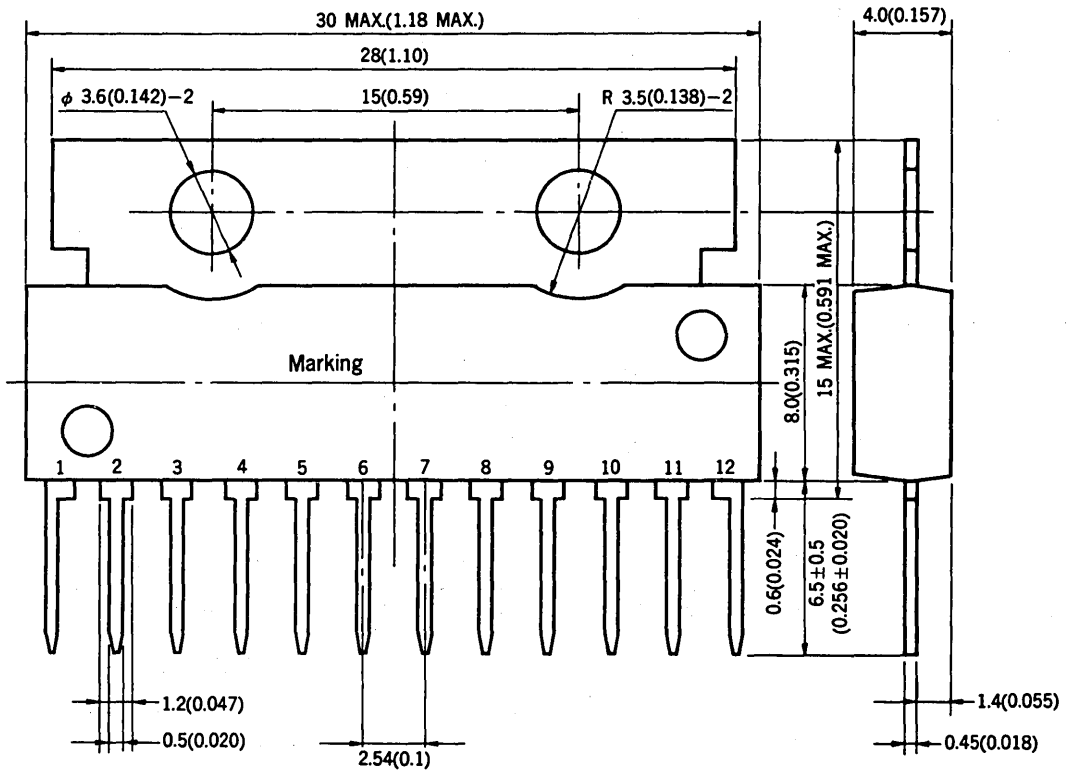
Supply Voltage (Operational)	V_{CC} = ±18 to ±36 V at Max Power Output
Input Bias Resistance	R_{IN} = 1 to 50 to 100 kohms
Power Transistor h_{FE}	h_{FE} = 50 at Max Power Output
Closed Loop Voltage Gain	A_V = 26 to 30 dB

ELECTRICAL CHARACTERISTICS (V_{CC} = ±36 V, A_v = 30 dB, Use Standard Test Circuit, Ta = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Output Offset Voltage	V_{OFF}		±5	±100	mV	SEE TEST CIRCUIT 1
Quiscent Circuit Current	I_{CC}		20	40	mA	V_{IN} = 0
Maximum Output Voltage	V_{OM}	20	23		V	T.H.D. = 0.05 % f = 20 to 20 kHz
Open Loop Voltage Gain	A_{vo}	80	95		dB	V_o = 1.5 V, f = 1 kHz
Output Noise Voltage	V_{NO}		0.07	0.14	mV	R_G = 10 kohms
Power Band Width	P.B.W.		900		kHz	V_o = 1.5 V, -3 dB
Supply Voltage Rejection Ratio	S.V.R.	55	70		dB	R_G = 2 kohms, f = 100 Hz

PACKAGE DIMENSIONS

in millimeters (inches)

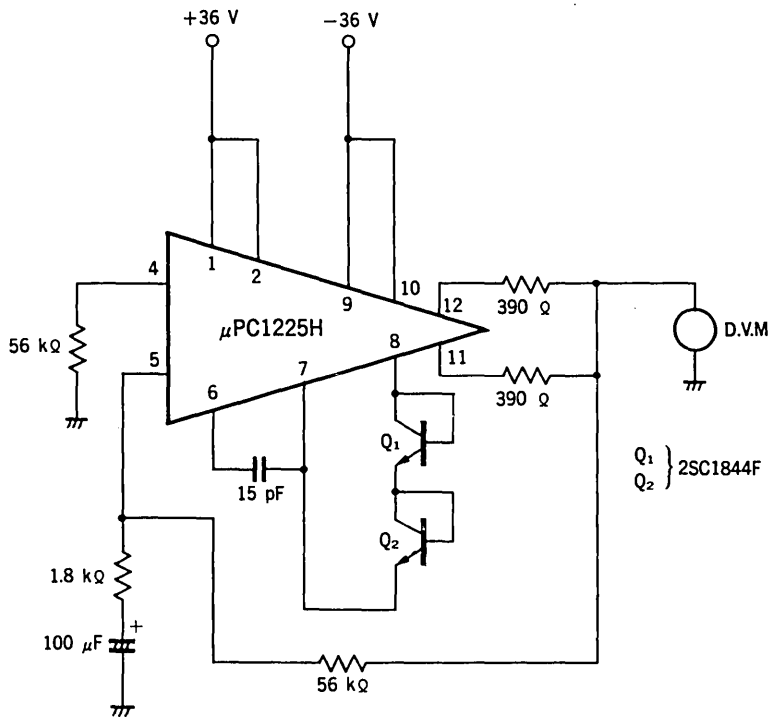


Typical dimensions unless specified otherwise.

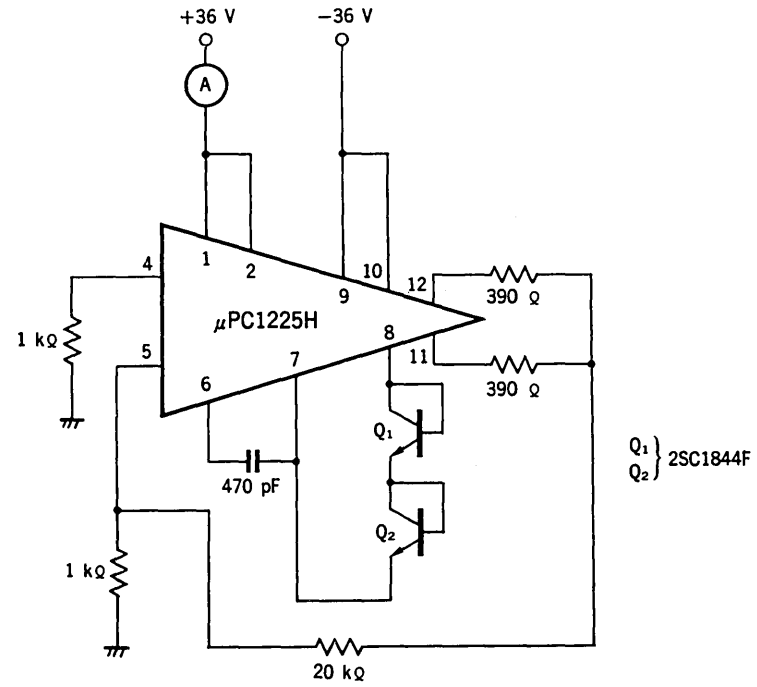
PIN CONNECTION DIAGRAM

Pin No.	Pin connection
1	$+V_{CCD}$ (for Driver)
2	$+V_{CCP}$ (for Preamp)
3	MUTING
4	INPUT
5	NFB
6	PHASE COMP
7	BIAS
8	BIAS
9	$-V_{CCP}$ (for Preamp)
10	$-V_{CCD}$ (for Driver)
11	LOWER OUTPUT
12	UPPER OUTPUT

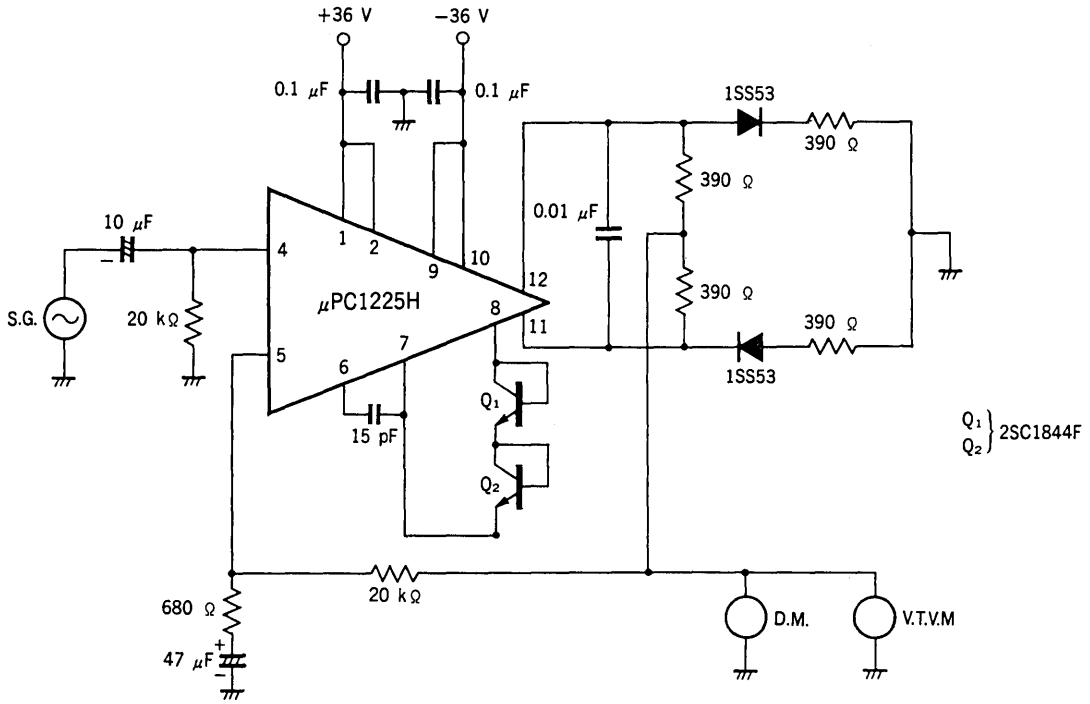
TEST CIRCUIT 1 (V_{OFF})



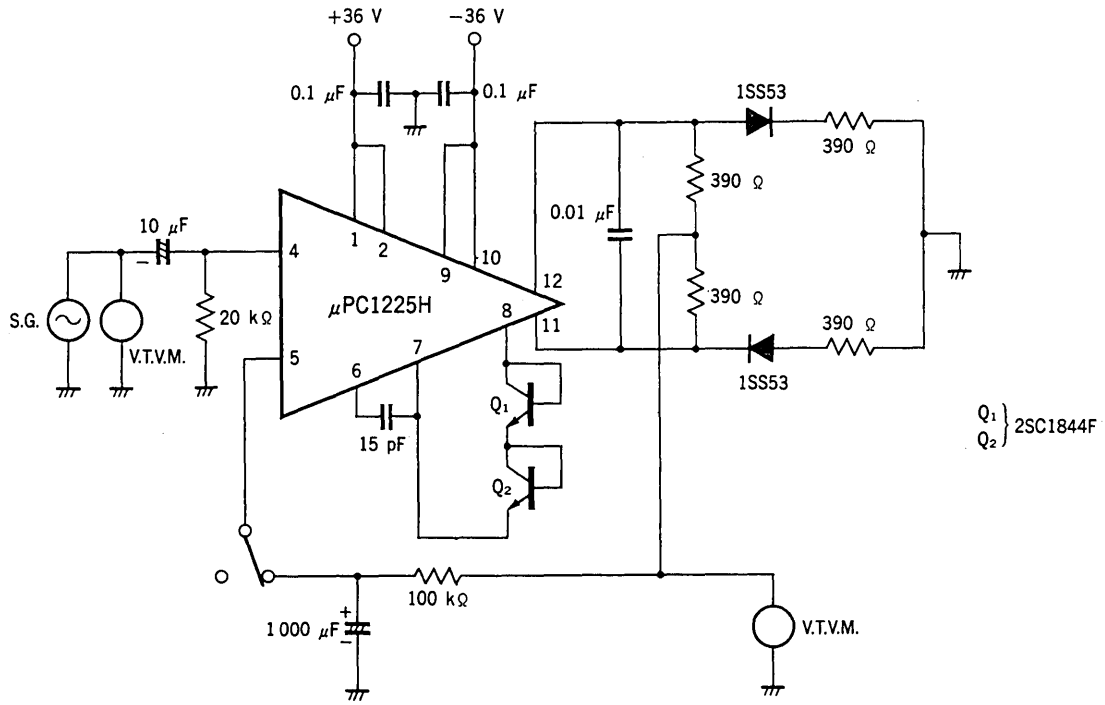
TEST CIRCUIT 2 (I_{CC})



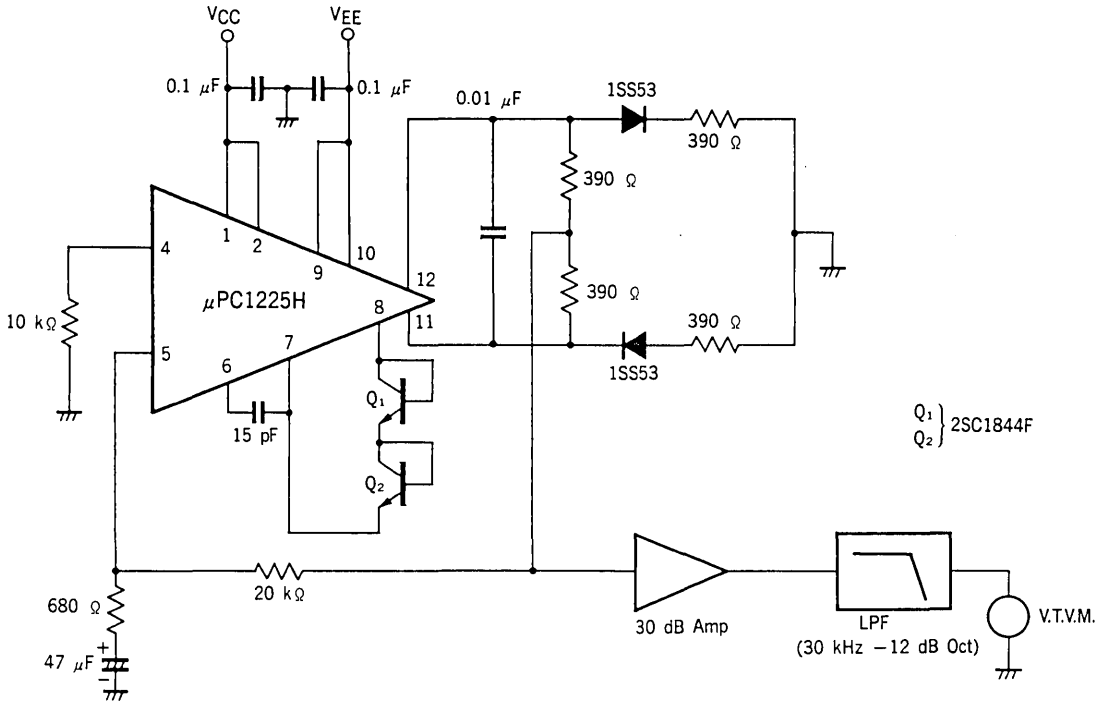
TEST CIRCUIT 3 (V_{OM})



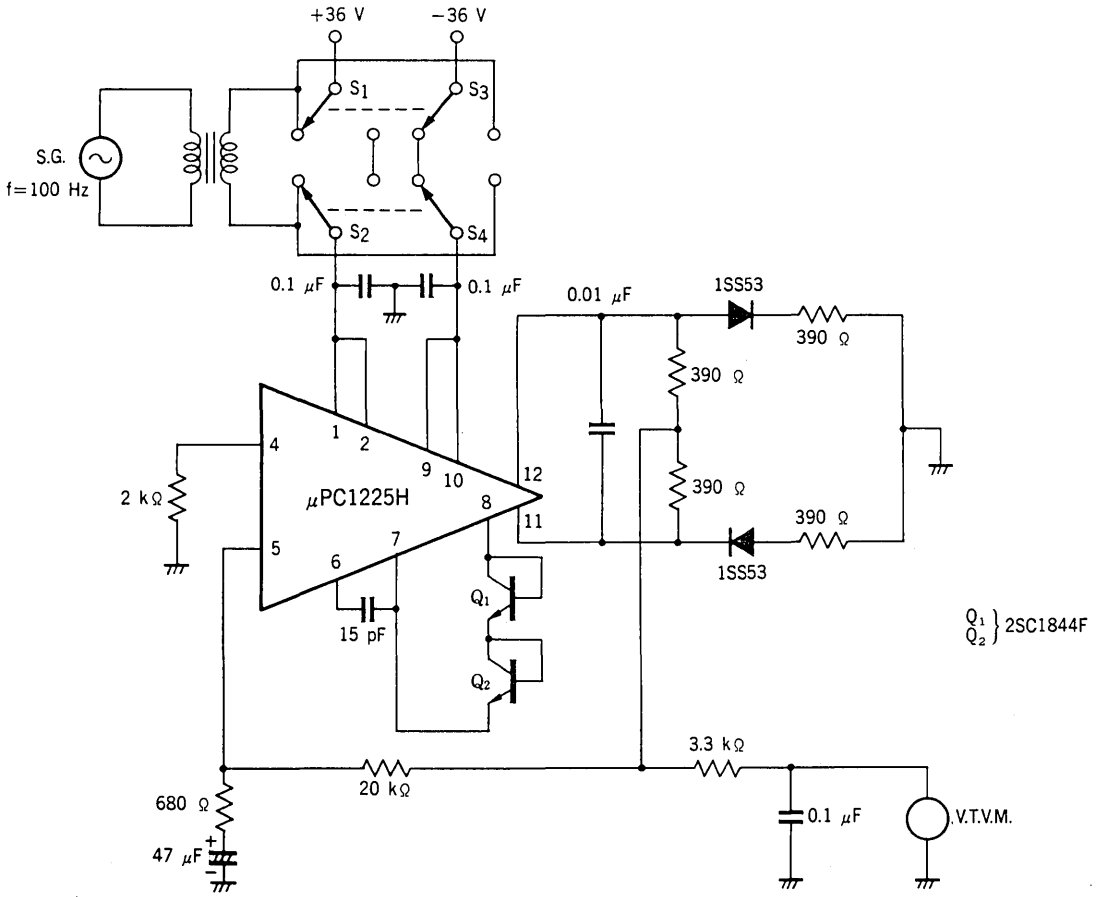
TEST CIRCUIT 4 (A_{VO})



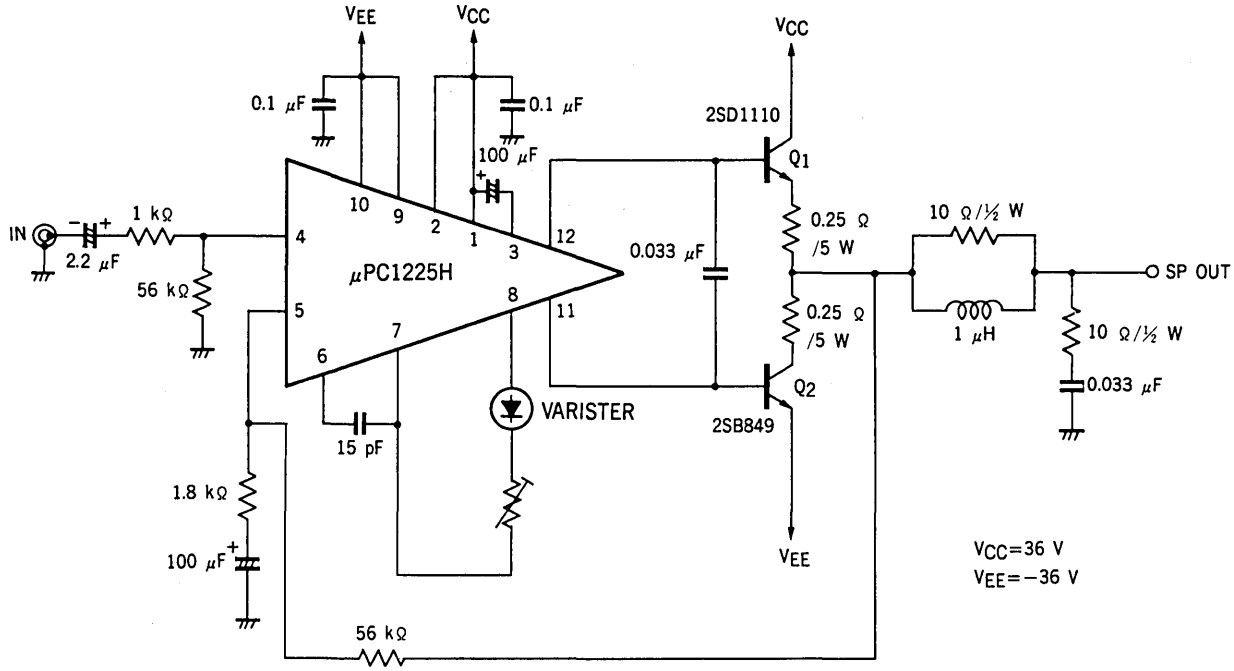
TEST CIRCUIT 5 (V_{NO})

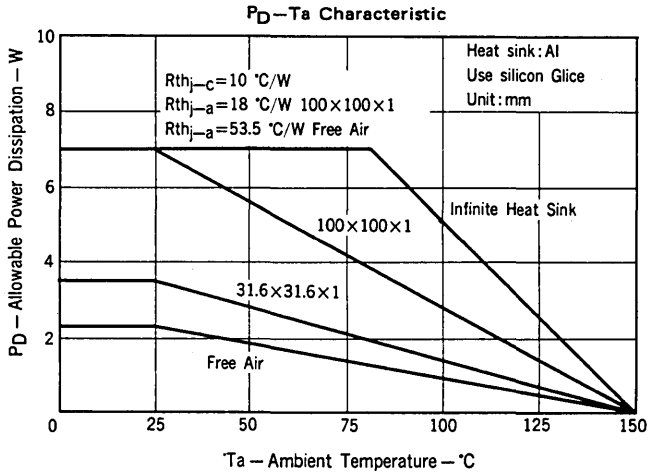


TEST CIRCUIT 6 (S.V.R.)

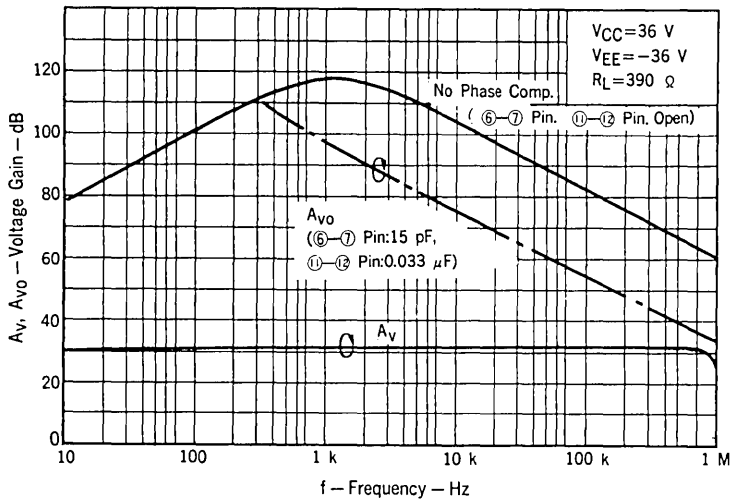


TYPICAL APPLICATION CIRCUIT

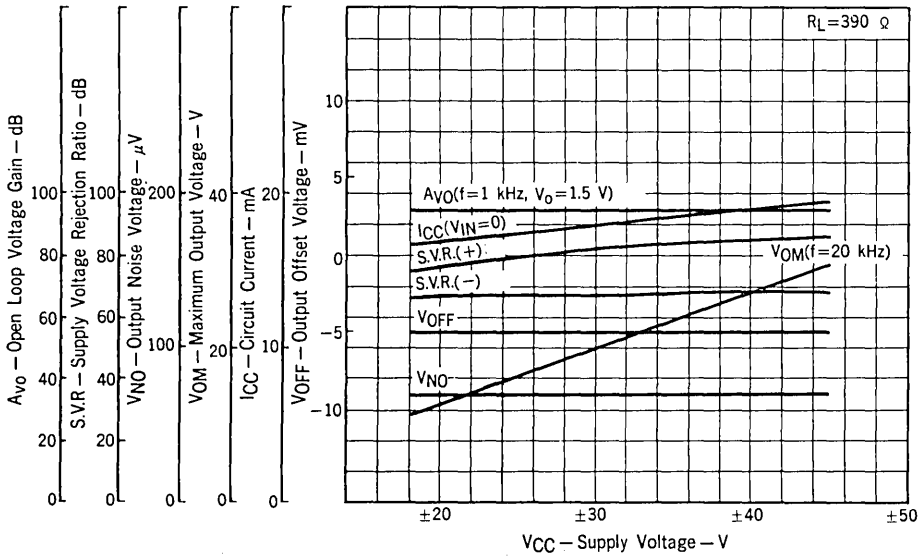




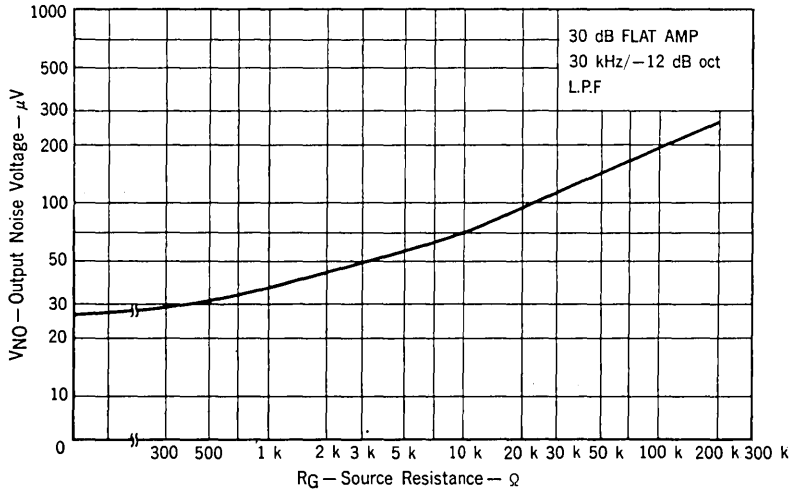
VOLTAGE GAIN vs. FREQUENCY



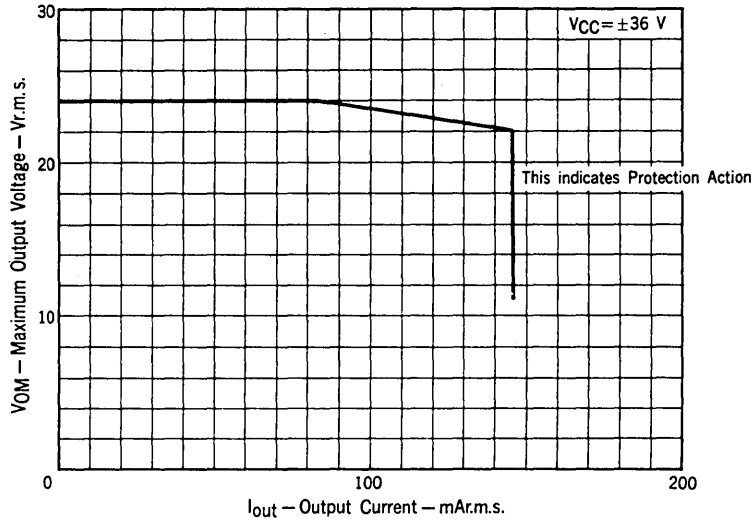
OPEN LOOP VOLTAGE GAIN
SUPPLY VOLTAGE REJECTION RATIO
OUTPUT NOISE VOLTAGE
CIRCUIT CURRENT
OUTPUT OFFSET VOLTAGE
vs. SUPPLY VOLTAGE



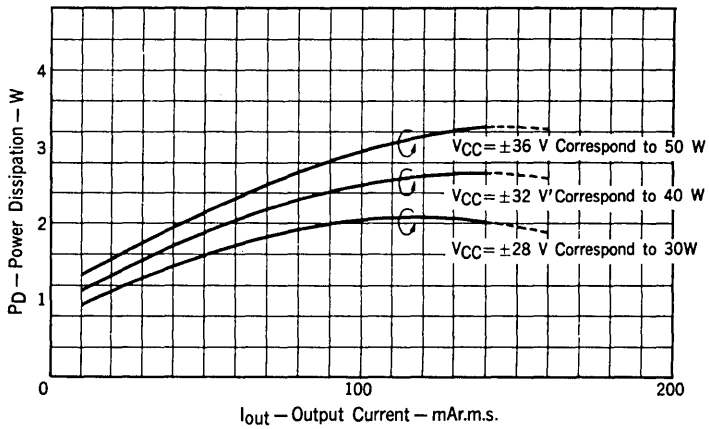
OUTPUT NOISE VOLTAGE
vs. SOURCE RESISTANCE



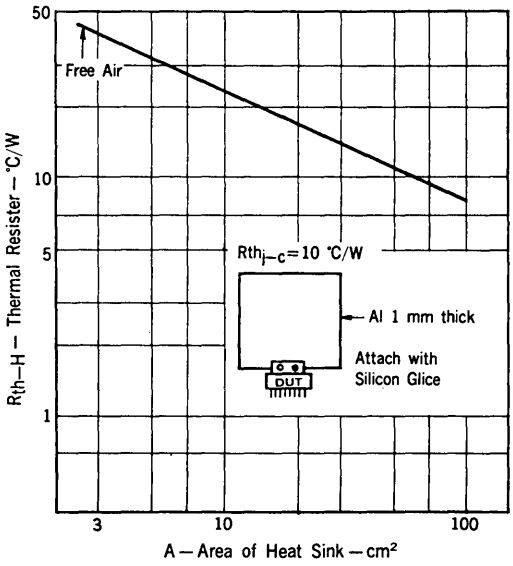
MAXIMUM OUTPUT VOLTAGE vs.
OUTPUT CURRENT



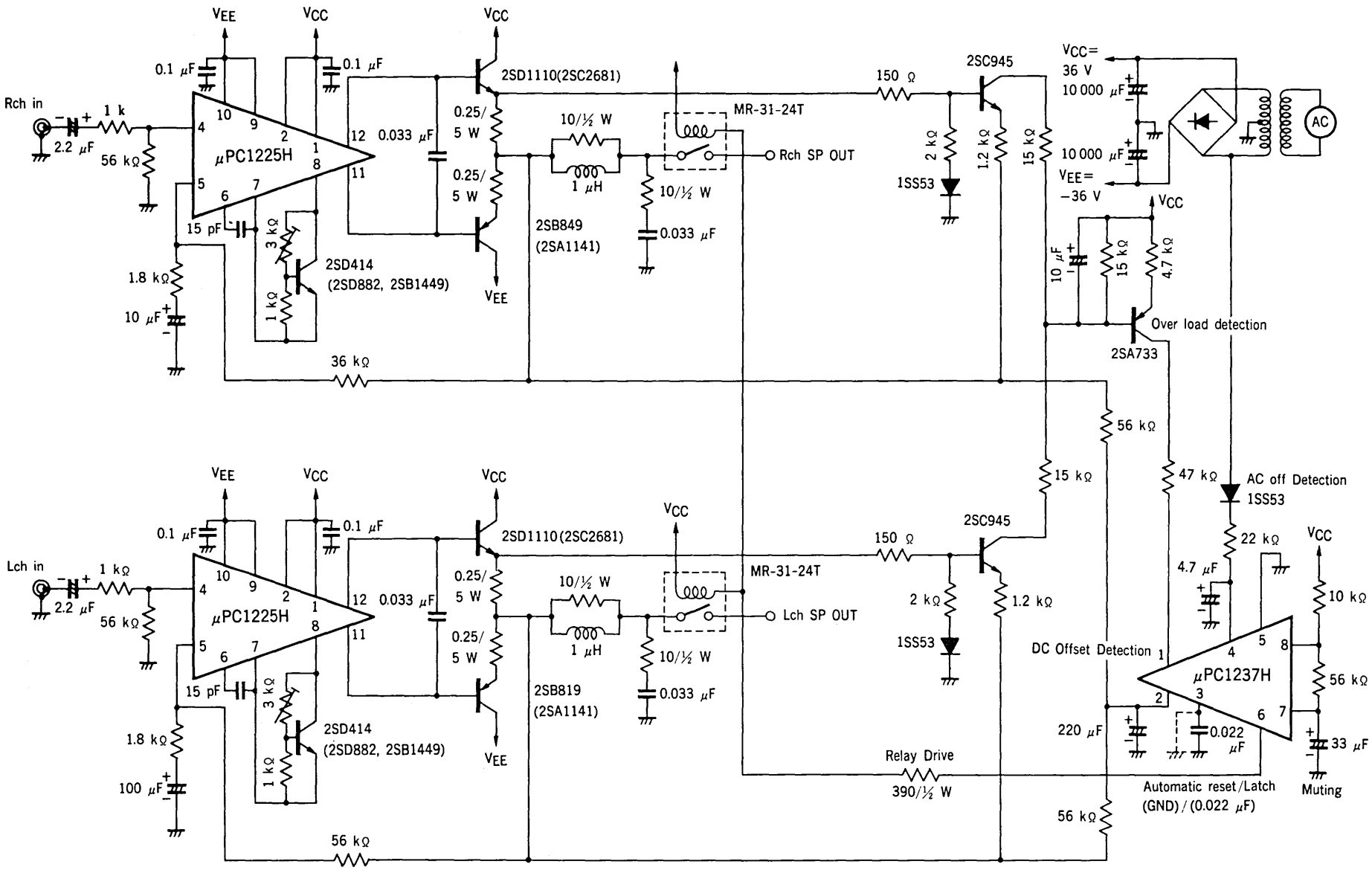
POWER DISSIPATION vs. OUTPUT CURRENT



THERMAL RESISTER vs. AREA OF HEAT SINK

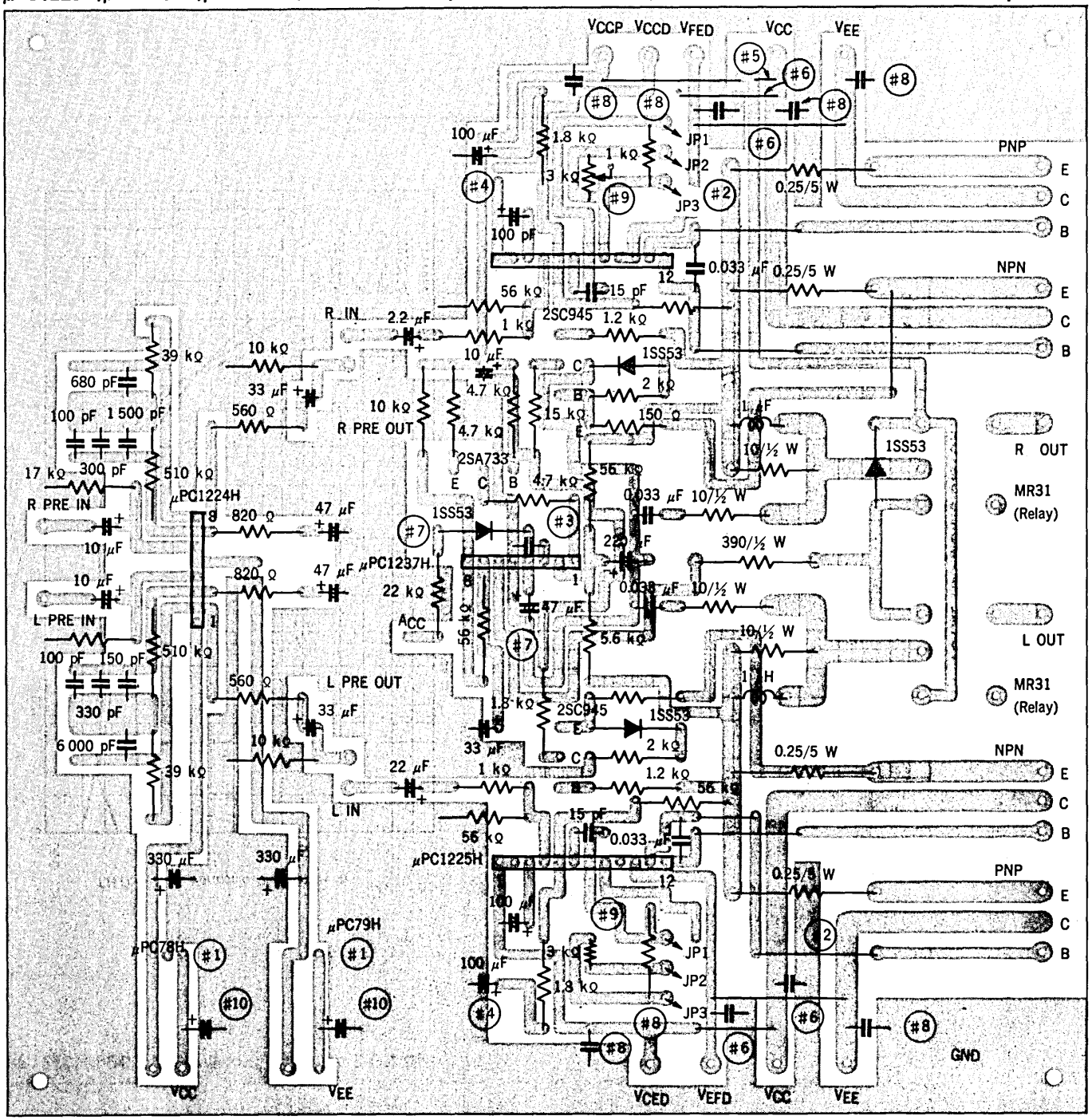


μPC1225H/μPC1237H/MP–80 EVALUATION CIRCUIT



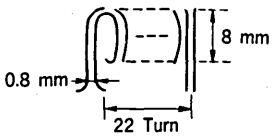
Note: Attach 2SD414 on P_O Tr Heat Sink.
Attach Al Heat Sink, which is larger than 60 mm X 60 mm X 1 mm, with μPC1225H.

μPC1225H/μPC1237H/μPC1224H/MP-80 (2SC849, 2SD1110 or 2SA2681, 2SC1141) Evaluation Circuit Board Component Arrangement



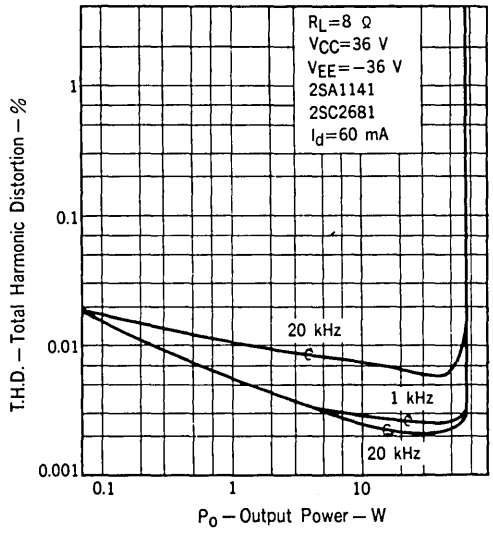
Note:

- #1 These terminals are for 3-terminals regulators (μPC7818H, μPC7918H) as a μPC1224H power supply.
- #2 These terminals are for JP— lines to a temperature Compensation transistor (2SD414 or others).
- #3 Use 0.02 μF capacitance in case of using μPC1237H at latching function, while connect each other at automatic resetting.
- #4 This capacitance is for preventing POP ON/OFF noise.
  Thus, neglect it in case of using a relay.
- #5 These terminals are for JP—lines in case of using the same power supply (μPC1237H and Power Amplifier)
- #6 These terminals are for JP— lines in case of using the same power supply (μPC1225H and Power Tr)
- #7 This terminal is for AC-OFF Detection. Thus, use 8.2 k ohms instead of 22 k ohms, neglect 1SS53 and connect these 1SS53's terminals and neglect 4.7 μF in case of using DC power supply.
- #8 These capacitances are for preventing a parastic oscillation. Use a 0.1 μF.
- #9 These trimmers are for adjusting an idling current. Recommend Neo-Pot PS61 Series.
- #10 These capacitance are for the 3-terminals regulator input.
- #11 Design of 1 μH (example)

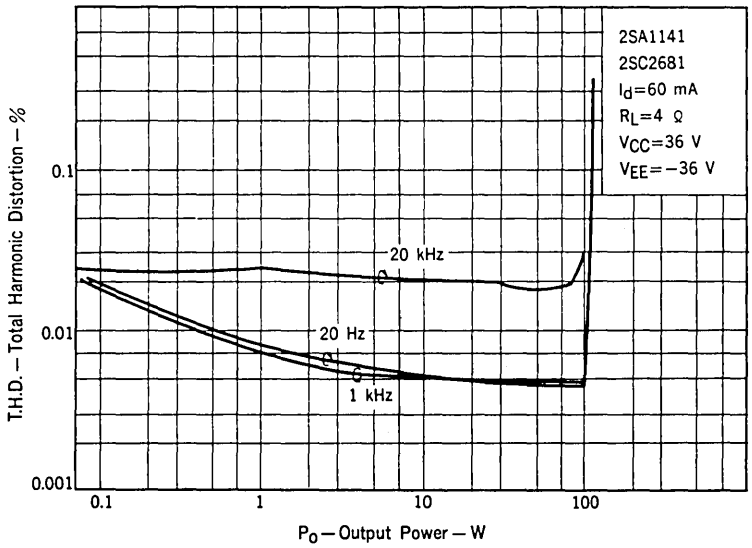


- #12 This indicates a copper board pattern

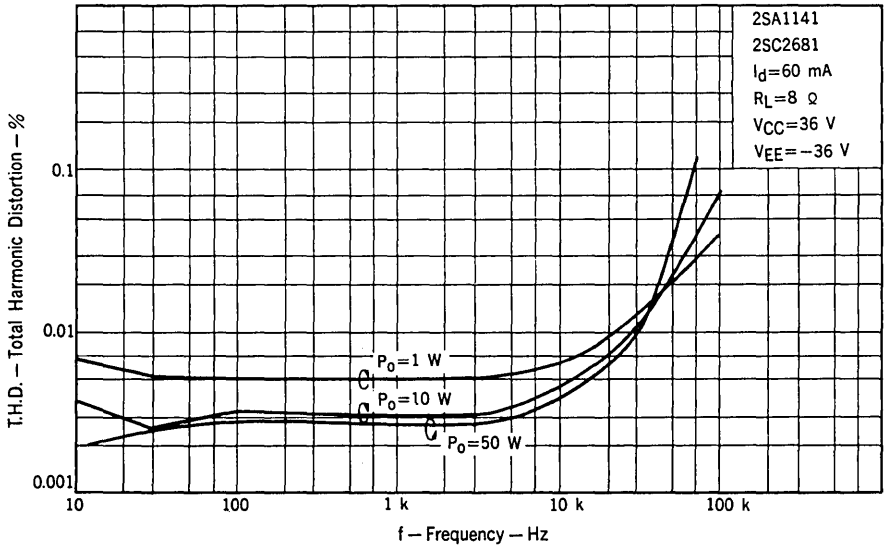
TOTAL HARMONIC DISTORTION
vs. OUTPUT POWER



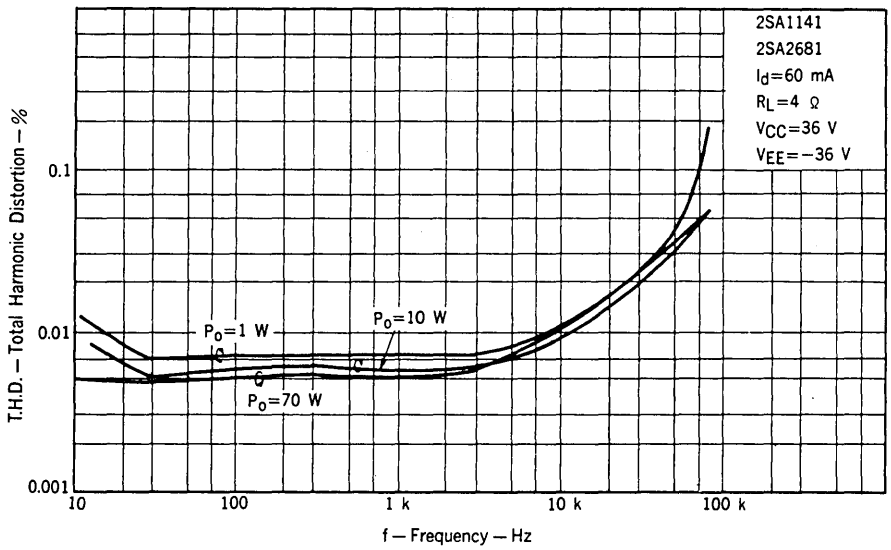
TOTAL HARMONIC DISTORTION
vs. OUTPUT POWER



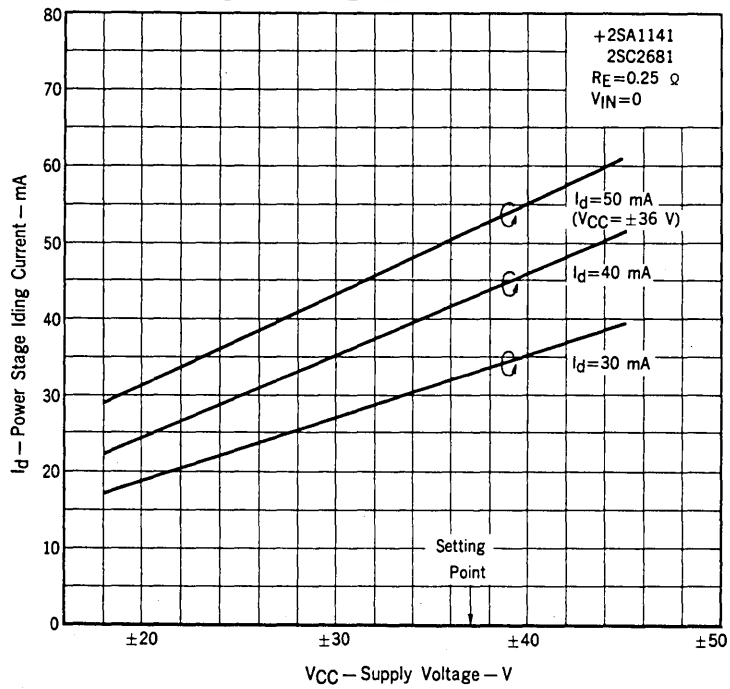
TOTAL HARMONIC DISTORTION
vs. FREQUENCY



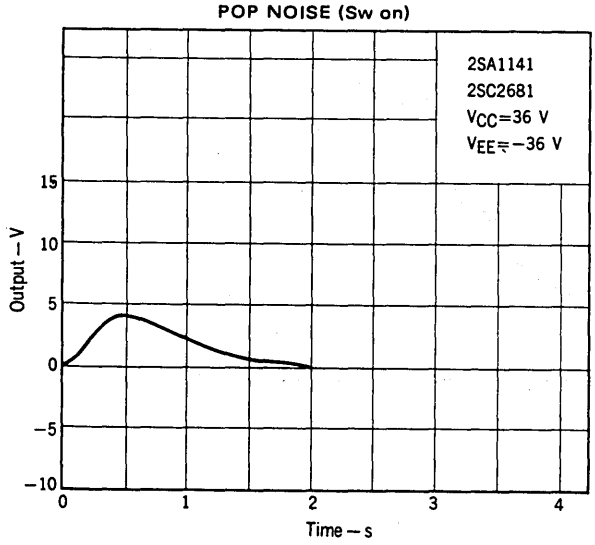
TOTAL HARMONIC DISTORTION
vs. FREQUENCY



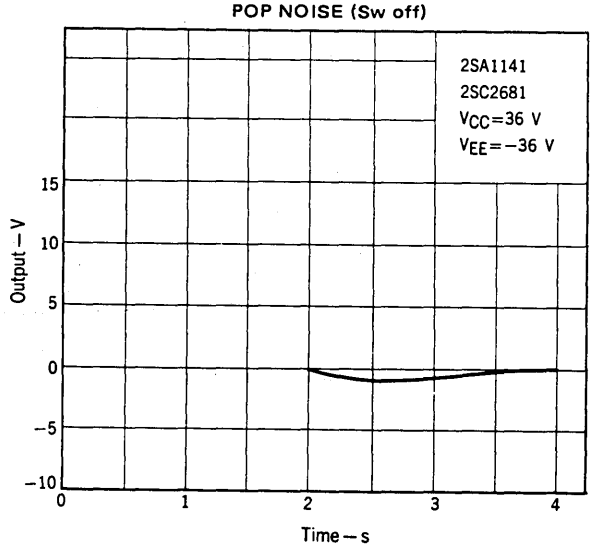
POWER STAGE IDLING CURRENT
vs. SUPPLY VOLTAGE



POP NOISE (Sw on)



POP NOISE (Sw off)



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1237H

PROTECTOR IC FOR STEREO POWER AMPLIFIER

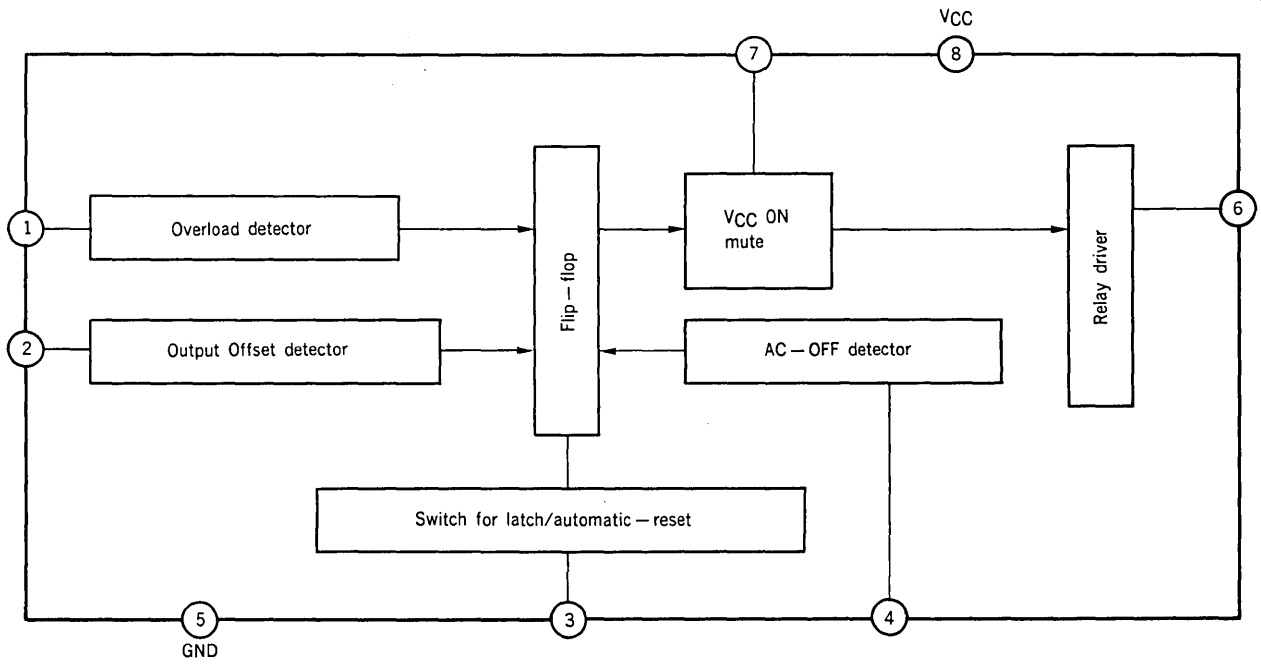
DESCRIPTION

μPC1237H is a monolithic integrated circuit designed for protecting stereo power amplifiers and loudspeakers, and is in an 8 pin single in-line package.

FEATURES

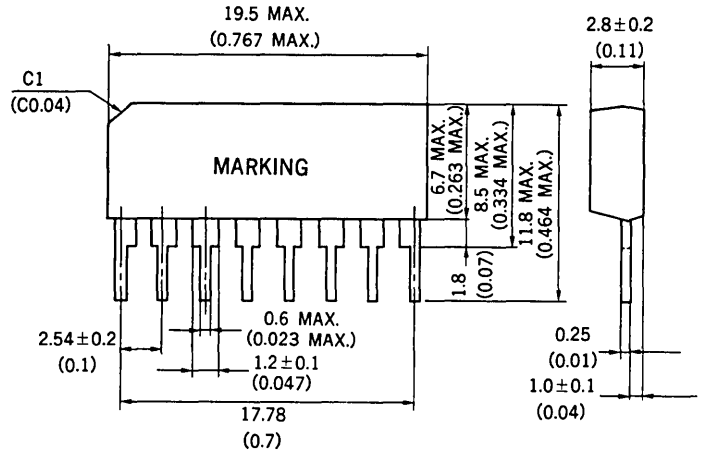
- Work stably within a wide power supply voltage range. (V_{CC} = 25 to 60 V)
- Contain a relay driver. (Max. I_6 = 80 mA)
- Work as either latching function or automatic resetting function by using pin 3. (In both overload detection and output offset detection, either function can be selected.)
- Need only single power supply.
- Both positive and negative output offset can be detected through the same pin. (Output offset detection through pin 2)
- AC voltage can be detected. (For AC-power-OFF mute through pin 4)
- The time delay from amplifier power ON to relay ON can be freely set by selecting external components. (For AC-power-ON mute through pin 7)
- The moment that amplifier-power is turned off, it can make relay broken OFF and then loudspeaker disconnected from amplifier to prevent a shock off noise.

BLOCK DIAGRAM



PACKAGE DIMENSIONS

in millimeters (inches)



Typical dimension unless specified otherwise.

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Power Supply Voltage	V_{CC}	60	V
Allowable Power Dissipation	P_D	320*	mW
Operational Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C
Pin 6 Maximum Current	I_6 max	80	mA
Pin 4 Maximum Voltage	V_4 max	10	V
Pin 8 Maximum Voltage	V_8 max	8	V
Pin 1 Maximum Current	I_1 max	3	mA
Pin 2 Maximum Current	I_2 max	±3	mA
Pin 7 Maximum Voltage	V_7 max	8	V

*Ta = 75 °C

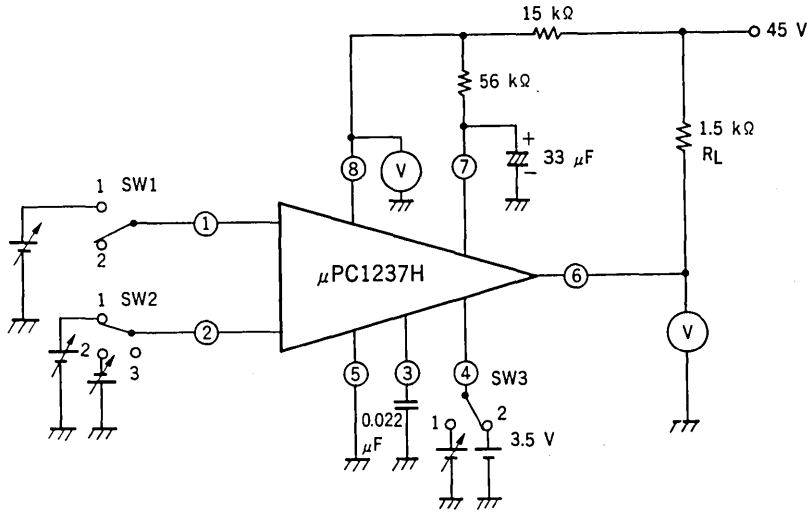
RECOMMENDED OPERATING CONDITIONS

Supply Voltage V_{CC} = 25 to 45 to 60 V

ELECTRICAL CHARACTERISTICS (V_{CC} = 45 V, Ta = 25 °C, State using latching function)

CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX.	UNIT	CONDITION
Pin 1 Threshold Voltage	Vth 1	0.58	0.67	0.76	V	level to invert at pin 6
Pin 2 Positive Threshold Voltage	Vth+2	0.54	0.62	0.70	V	level to invert at pin 6
Pin 2 Negative Threshold Voltage	Vth−2	−0.12	−0.17	−0.23	V	level to invert at pin 6
Pin 4 Threshold Voltage	Vth 4	0.60	0.74	0.90	V	level to invert at pin 6
Pin 8 Reference Voltage	V8	3.0	3.4	3.8	V	R_L = 1.5 kΩ

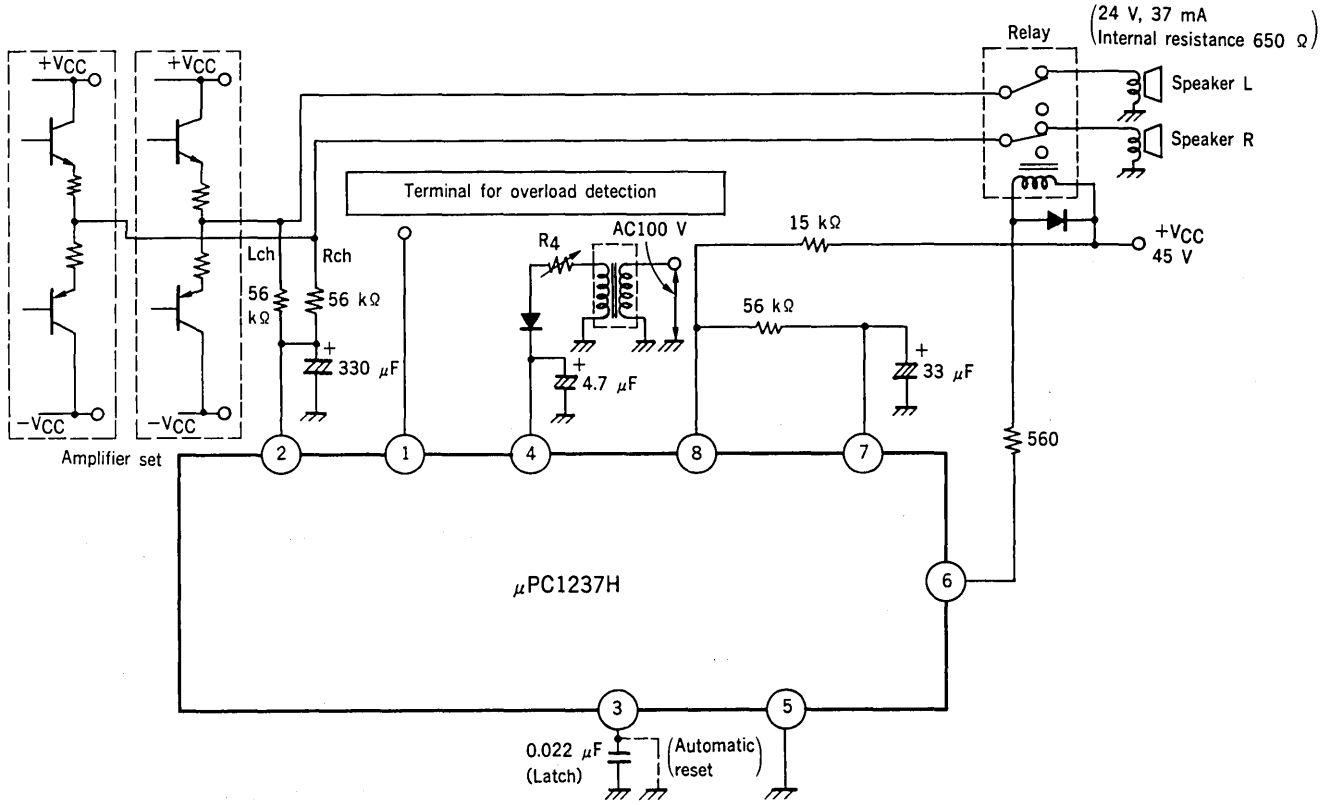
TEST CIRCUIT (State using latchung function)



Switch positions

Item	SW 1	SW 2	SW 3
Vth 1	1	3	2
Vth+2	2	1	2
Vth−2	2	2	2
Vth 4	2	3	1
V8	2	3	2

TYPICAL APPLICATION CIRCUIT



NOTE FOR USING μPC1237H

1. FUNCTION FOR OUTPUT OFFSET DETECTION (pin 2)

1) If too much DC current flows through a speaker voice coil due to large output offset DC level, the voice coil might be overheated and the speaker might be broken. To prevent the damage, it is necessary to detect the Output Offset DC level and to disconnect the speaker from the power amplifier by breaking off a relay if the detected DC level is shifted beyond a threshold level. μPC1237H has a function to detect both the positive and the negative Output Offset DC level with its single power supply. As shown below, you can easily make the positive and the negative threshold level equivalent and also set up their level by choosing proper resistances.

2) How to determine the threshold levels of Output Offset detection. (±Vth)

[1] The threshold level of positive output offset detection (+Vth) is given by Eq. (1).

$$+Vth = (2 + \frac{R_A}{R_C}) \cdot Vth^{+}2, \quad \cdots\cdots (1)$$

where $Vth^{+}2$ is the original positive threshold level of pin 2, and $Vth^{+}2 = 0.62$ V TYP.

[2] The threshold level of negative Output Offset detection (−Vth) is given by Eq. (2).

$$-Vth = -\left\{-Vth^{-}2 \cdot (2 + \frac{R_A}{R_C}) + I_{c2} \cdot R_A\right\}, \quad \cdots\cdots (2)$$

where $Vth^{-}2$ is the original negative threshold level of pin 2, and
$Vth^{-}2 = -0.17$ V TYP.
and I_{c2} is the current from μPC1237H and,
$I_{c2} = 12.5\ \mu A$ TYP.
at nearly −Vth.

3) You can easily find how to make ±Vth level equivalent as shown below

$$(2 + \frac{R_A}{R_C}) \cdot Vth^{+}2 = -\left\{-Vth^{-}2 \cdot (2 + \frac{R_A}{R_C}) + I_{c2} \cdot RA\right\}, \quad \cdots\cdots (3)$$

therefore determine R_A, R_B and R_C from Eq. (3)

Attention; The original positive and negative threshold level at pin 2 without any resistances are unbalanced; +Vth = 0.62 V TYP. and −Vth = −0.17 V TYP.

Example of design

If you need the output offset threshold level ±Vth to be ±2.0 V, determine R_A, R_B and R_C as shown below.

[1] Substitute 2.0 to +Vth in Eq. (1) and obtain R_A / R_C.

$$2.0 = (2 + \frac{R_A}{R_C}) \times 0.62$$

$$\frac{R_A}{R_C} \fallingdotseq 1.226$$

[2] Substitute −2.0 to −Vth in Eq. (2) and obtain R_A (R_B) and R_C.

$-2.0 = -0.17\ (2 + 1.226) - 12.5\ (\mu A) \times R_A\ (k\Omega)$ (V)

$R_A = 116.1\ k\Omega$

$R_C = 94.7\ k\Omega$

Therefore, if you need ±Vth to be 2.0 volts, choose R_A, R_B and R_C as shown below.

$R_A = R_B = 120\ k\Omega$ and $R_C = 91\ k\Omega$

The lower limits of R_A and R_B are given by the maximum rating (±3 mA) of pin 2 and

$$\frac{\pm V_{CC}}{R_A(B)} < \pm 3\ (mA)$$

In case of recommended condition, that is $R_A = R_B = 56\ k\Omega$ and $R_C = \infty$, ±Vth can be obtained as shown below.

[1] $+Vth = (2 + \frac{56\ (k\Omega)}{\infty})\ \ 0.62 = 1.24$ (V)

[2] $-Vth = -0.17\ (2 + \frac{56\ (k\Omega)}{\infty}) - 12.5\ (\mu A) \times 56\ (k\Omega) = -1.04$ (V)

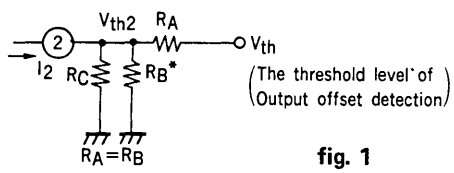


fig. 1

* Rch power amplifier output terminal is usually an imaginally GND as seen from Lch power amplifier, so that the equivalent circuit can be obtained as shown above.

2. FUNCTION OF AC LEVEL DETECTION

When you turn off the power switch, it sometimes causes a shock-off noise, therefore it is necessary to break off the relay and then to keep the power amplifier apart from loud speaker at the moment that power switch is turned off. In other words, the protection circuit is required to have a function to detect that power-off time. However, in fact, it is difficult to detect that power-off time from actual DC supply voltage line. Because it cannot be turned 0 V instantaneously due to a large capacitance inserted between the power supply line and GND. In case of μPC1237H, it can detect this power-off time from AC power supply directly, that is, this is a function to detect AC level.

The AC power supply level (usually 50 Hz or 60 Hz) can be transmitted to pin 4 through a half-wave rectification circuit as shown below.

And it works within a wide range of AC level by choosing a proper resistance as R4 (Refer to the characteristic curve shown as fig.5 for the choice of R4). If power switch is turned off while the relay is being made ON and the speaker is being connected to the power amplifier output, the relay will be broken OFF to disconnect the speaker after a time delay (AC OFF mute) according to the discharge time constant determined by the voltage on pin 4, the external capacitance C4, and the internal resistance of the IC.

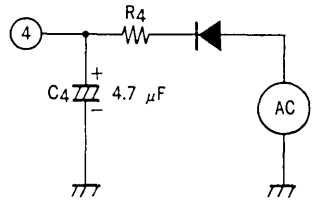


fig. 2

3. FUNCTION OF OVERLOAD DETECTION (pin 1)

The original threshold level of pin 1 is 0.67 V TYP. In case of using a constant-current drive, as the means of detection, the threshold current level is 110 μA TYP. When current which is larger than 110 μA flows to the IC, the relay will be broken OFF.

Note ; The overload detecting circuit is not included in the IC because of patent problems. Use the external circuit as an overload detection.

4. FUNCTION OF LATCHING AND AUTOMATIC RESETTING (pin 3)

If the IC detects the abnormal condition such as the larger output offset level or the overload, the IC can make the relay broken OFF. And then, two functions can be selected after the condition returns to the normal state. One is that the relay is made ON automatically and the other is that it keeps the relay broken off until once the power switch is turned off and then is turned on again.

The former is a function of automatic resetting and the latter is a function of latching. μPC1237H has both functions and can be selected either function by using pin 3. In case of latching, connect pin 3 to the ground through the capacitor, which is for preventing misoperation. For automatic resetting, connect it to the ground directly. This function is valid for both overload detection and output offset detection.

5. TIME DELAY FROM POWER AMPLIFIER POWER SWITCH ON TO RELAY ON (power-on mute at pin 7)

To suppress shock-on noise generated by power ON, a time delay is provided by connecting a circuit with a time constant. This time delay is set to make relay ON to connect speakers after enough time for the power amplifier and the preamplifier to reach a stable operating condition. The ON mute time is determined as follows,

$$T\ (\text{ON mute}) = -C_7 \cdot R_7 \cdot \ell n \frac{V_8 - V_7}{V_8},$$

where V_8 is reference voltage at pin 8, 3.40 volts, TYP. and V_7 is threshold level at pin 7, 2.06 volts, TYP.

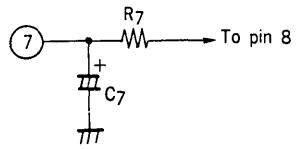


fig. 3

6. HOW TO MAKE IT WORK WITHIN A WIDE RANGE OF POWER SUPPLY VOLTAGE (pin 8)

By choosing a proper resistance R_8 connected to pin 8, the IC can work within a wide range of power supply voltage V_{CC} from 25 to 60 volts.

In case that pin 8 is directly driven by a regulated power supply, set V_8 to 3.40 volts, TYP. As for the choice of R_8 value, refer to the characteristic curve shown as fig.6.

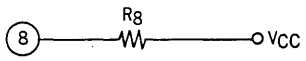
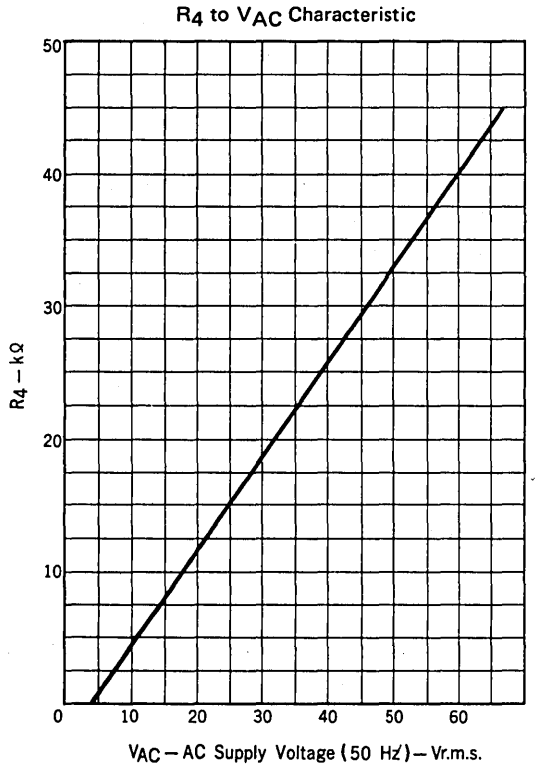
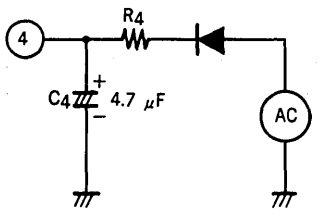


fig. 4

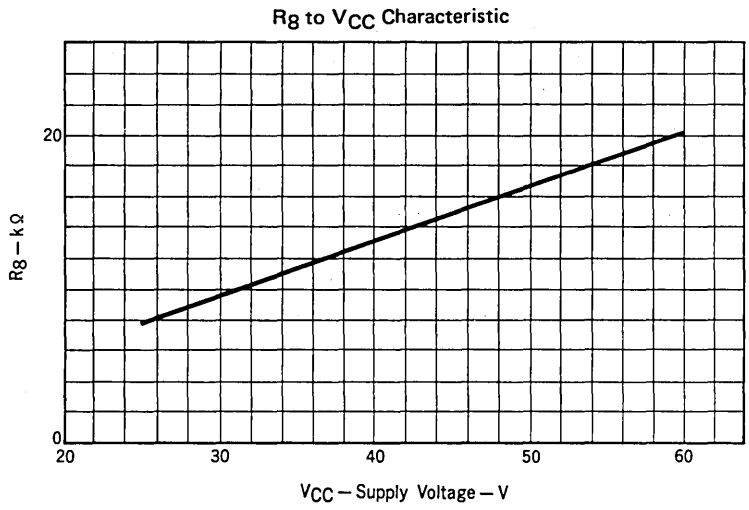
fig. 5 OPTIMUM VALUE OF EXTERNAL RESISTANCE R_4

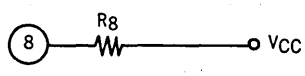




Example) Use of E-24 series.
Select 24 kΩ R_4 for 40 volts r.m.s. V_{AC}.
If no resistance of specified value is available,
choose a resistance which is as close as possible
to and lower than the value specified by the diagram.

fig. 6 OPTIMUM VALUE OF EXTERNAL RESISTANCE R_8

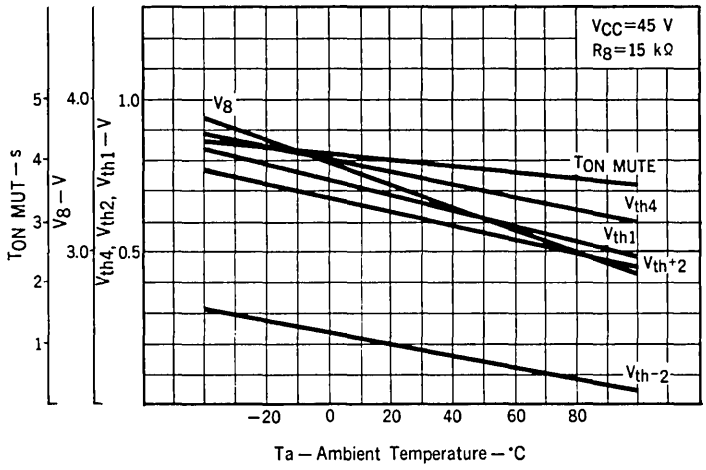




Example) Use of E-24 series.
Select 15 kΩ R_8 for 45 volts Vcc.
If no resistance of specified value is available,
choose a resistance which is as close as possible
to and lower than the value specified by the diagram.

TEMPERATURE CHARACTERISTIC

V8, TON mut, Vth4, Vth+2, and Vth1 to Ta Characteristics



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1180C

DOLBY B-TYPE NOISE REDUCTION PROCESSOR

DESCRIPTION

The μPC1180C is a monolithic integrated circuit specifically designed to realize the Dolby B-Type Noise Reduction System.

The device consists of a Buffer Amplifier (B.A.), a Noise Reduction Processor (N.R.Processor) consisting of an Inverter Amplifier (INV), a Side Chain Amplifier (SCA), an Overshoot Suppression Circuit (OS), a Voltage Control Amplifier (VCA), an Integration Circuit (INT), a Hi-Pass Filter (HPF), and a Detector Circuit (DET).

The IC is encapsulated in a 16 pin, dual-in-line plastic package.

Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, from whom licensing and application information must be obtained.

"Dolby" and the Double-D symbol are trade marks of Dolby Laboratories.

FEATURES

- Very close matching to standard Dolby Characteristics
- Uses Low Noise Devices

Buffer Amp. Noise Level (6 dB gain)	−98 dBv	(CCIR/ARM)
Noise Reduction Processor Noise Level	−80 dBv	(CCIR/ARM)

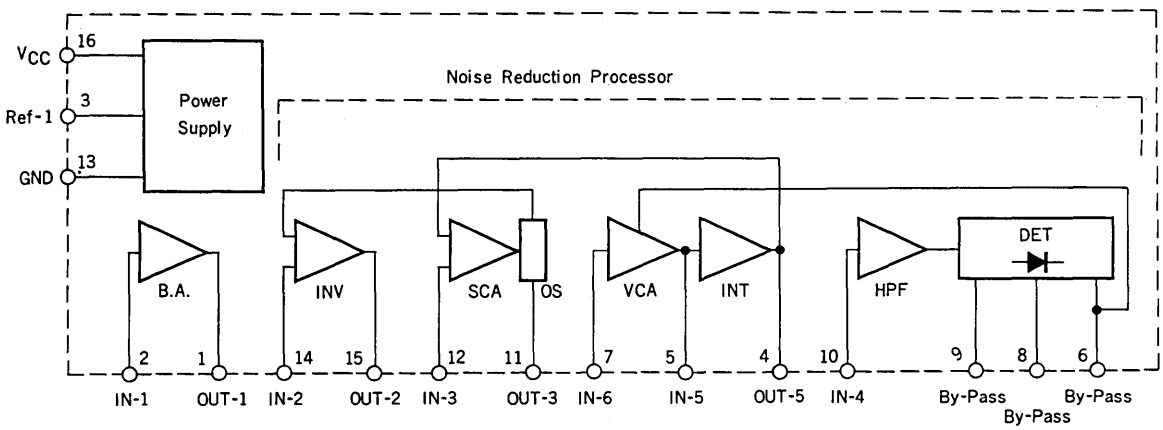
- Low Total harmonic distortion (at Dolby level)

Buffer Amp. Distortion	0.02 %	(f = 10 kHz)
Noise Reduction Processor Distortion	0.03 %	(f = 333 Hz)
Noise Reduction Processor Distortion	0.08 %	(f = 10 kHz)

- Low supply current

I_{CC}	9 mA

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Supply Voltage	V_{CC}	28	V
Power Dissipation	P_D	350*	mW
Operating Temperature Range	T_{opt}	−15 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Lead Temperature	T_L	260**	°C

*Value at Ta = 75 °C
**Soldering at 10 s MAX.

RECOMMENDED OPERATING CONDITIONS (Ta = 25 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	18	24	26	V
Buffer Amp. Gain	A_V−(B.A.)	6		12	dB

ELECTRICAL CHARACTERISTICS [Ta = 25 °C, V_{CC} = 24 V, Dolby Level = 1 Vr.m.s. (= 0 dBv)]

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Current	I_{CC}	No Signal		9	12.5	mA
Buffer Amp.						
Signal Handling	V_{om}(1)	f = 10 kHz, T.H.D. = 1 %, R_L = 5 kΩ	15	17		dBv
Distortion	T.H.D.(1)	f = 10 kHz, V_o = 6 dBv, R_L = 5 kΩ		0.02	0.07	%
Noise Level	V_{no}(1)	Input Shorted, Using CCIR/ARM		−98	−88	dBv
INV Amp. Gain	A_V	f = 333 Hz	−0.5	0	0.5	dB
Noise Reduction Processor						
Signal Handling	V_{om}(2)	REC, f = 333 Hz, V_o = 0 dBv, R_L = 10 kΩ	15	17		dBv
Signal Handling	V_{om}(3)	REC, f = 10 kHz, V_o = 0 dBv, R_L = 10 kΩ	12.5	15		dBv
Distortion	T.H.D.(2)	P.B, f = 333 Hz, V_o = 0 dBv, R_L = 10 kΩ		0.03	0.08	%
Distortion	T.H.D.(3)	REC, f = 10 kHz, V_o = 0 dBv, R_L = 10 kΩ		0.08	0.14	%
Noise Level	V_{no}(2)	REC, R_g = 0, Using CCIR/ARM		−80	−70	dBv
REC Mode Response	F.R(1)	f = 333 Hz, V_{in} = 0 dBv	−0.7	0	+0.7	dBv
REC Mode Response	F.R(2)	f = 1 kHz, V_{in} = −20 dBv	−18.1	−16.7	−15.3	dBv
REC Mode Response	F.R(3)	f = 5 kHz, V_{in} = −20 dBv	−18.0	−16.8	−15.6	dBv
REC Mode Response	F.R(4)	f = 5 kHz, V_{in} = −40 dBv	−30.4	−29.7	−28.8	dBv
Cross Talk	V_{crs}	REC, f = 333 Hz, B.A. to N.R.Processor, V_o = 15 dBv			−70	dBv

For alignment instruction see section 3.8 of licence information manual.

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1252H2

VCA FOR dbx NOISE REDUCTION SYSTEM

DESCRIPTION

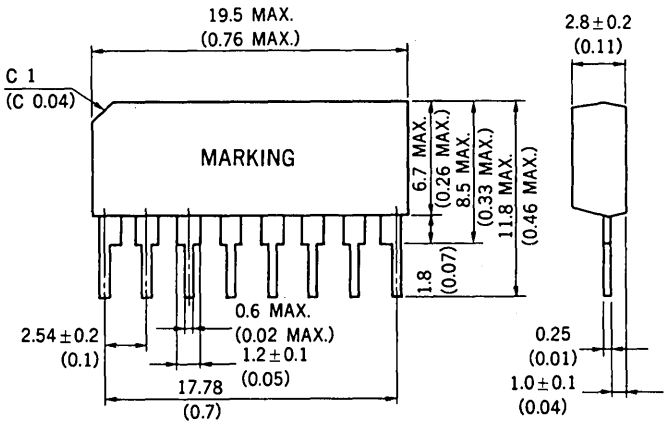
The μPC1252H2 is dbx noise reduction system VCA (Voltage Controlled Amplifier), used in tape deck and other audio equipment.

The μPC1252H2 features excellent lineality VCA for wider input level due to NEC's super low noise and high h_{FE} NPN/PNP, complementary process.

Since the package is 8 pin SIP. It can be built in a compact set.

PACKAGE DIMENSIONS

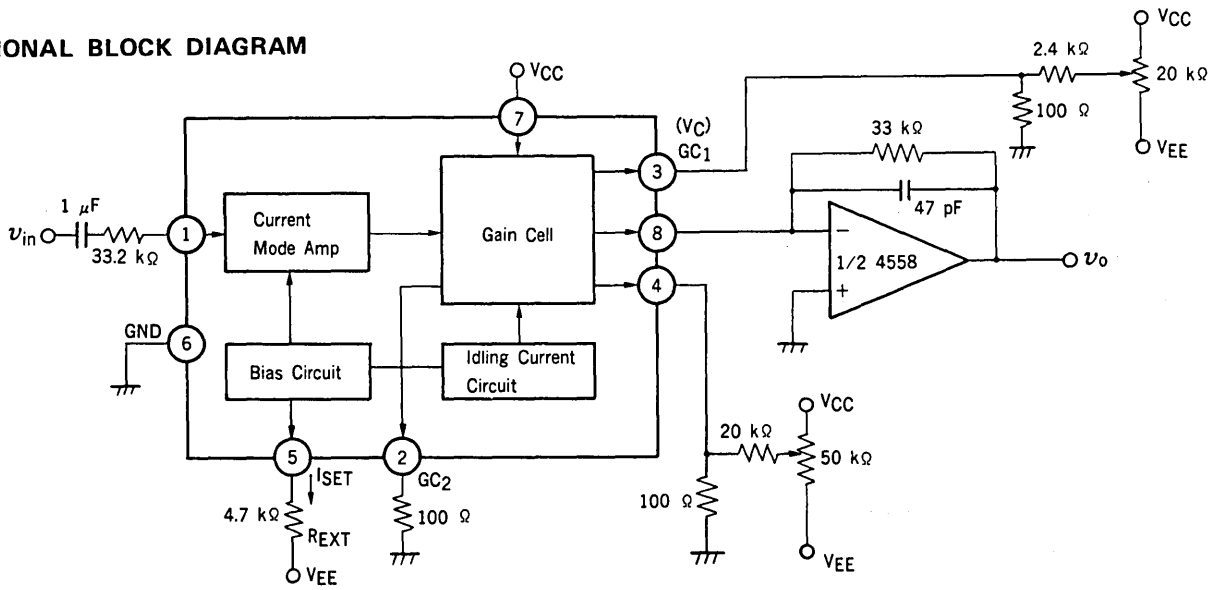
in millimeters (inches)



FEATURES

- Wide operating supply voltage — V_{CC} = ±4 to ±15 V (TYP. ±12 V)
- Excellent lineality Control Constant — V_C = −5.9 mV/dB (A_V = −30 dB to +30 dB)
- Low total hamonic distortion — T.H.D. = 0.01 % TYP. (V_{CC} = ±12 V, f = 1 kHz, V_O = 0 dBV)
- Low noise — NV_O = −94 dBV TYP. (V_{CC} = ±12 V, R_{IN} = 33.2 kΩ, A_V = 0 dB, BPF = 10 Hz to 20 kHz)

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{CC}, V_{EE}	+15	V
Supply Current	I_{CC}	30	mA
Power Dissipation	P_D	330*	mW
Operating Temperature Range	T_{opt}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C

* Value at T_a = 75 °C

RECOMMENDED OPERATING CONDITIONS

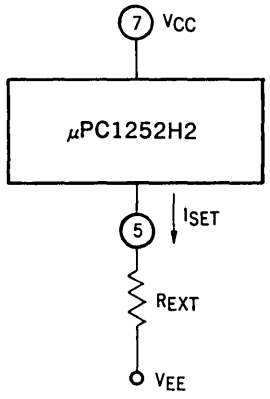
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage	V_{CC}, V_{EE}**	±4	±12	±15	V
Bias Current	I_{SET}	—	2.0	—	mA
Input Level Range	v_{in}	−40		+10	dBV

** See Note

ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V_{CC} = +12 V, V_{EE} = −12 V, I_{SET} = 2 mA, R_{IN} = R_{OUT} = 33 kΩ, f = 1 kHz)

CAHRACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Current	I_{CC}	1.0	2.0	3.0	mA	Non Signal
Equivalent Input Bias Current	I_{IN}		6	20	nA	Non Signal
Gain Cell Idling Current	I_{DLE}		20		μA	Non Signal
Gain Cell Offset Voltage	V_{OFF}		±0.5		mV	A_v = 0 dB, T.H.D. ≦ 0.07 %
Control Constant	V_C	−5.8	−5.9	−6.1	mV/dB	A_v = −30 dB to +30 dB
Total Harmonic Distortion	T.H.D.1		0.007	0.07	%	A_v = 0 dB, V_o = 0dBV, BPF = 400 Hz to 5 kHz
Total Harmonic Distortion	T.H.D.2		0.02	0.10	%	A_v = +20 dB, V_o = 0dBV, BPF = 400 Hz to 5 kHz
Total Harmonic Distortion	T.H.D.3		0.02	0.15	%	A_v = −20 dB, V_{in} = 0dBV, BPF = 400 Hz to 5 kHz
Output Noise Level	NV		−94	−84	dBV	A_v = 0 dB, R_{IN} = 33 kΩ, BPF = 10 Hz to 20 kHz
Symmetry Control Voltage	V_{SYM}	−4	0	+4	mV	A_v = 0 dB, T.H.D. ≦ 0.07 %

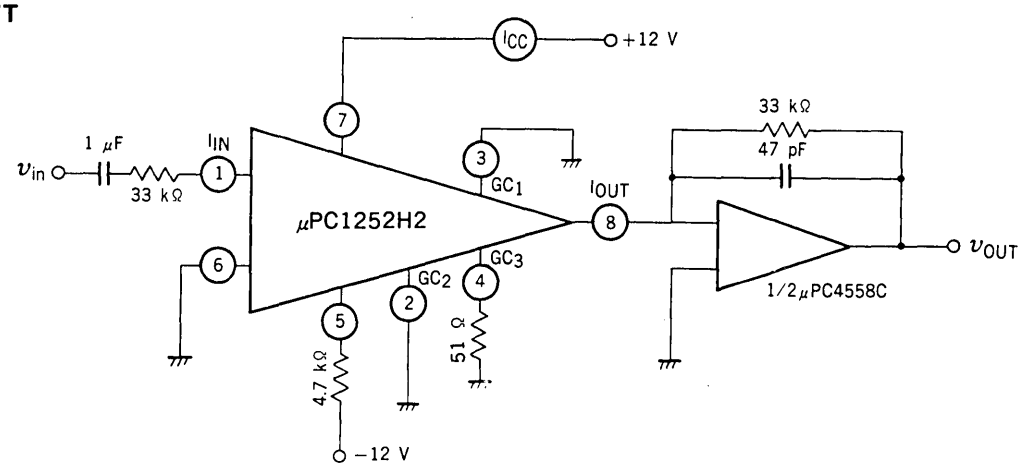
Note) V_{CC}, V_{EE} and I_{SET} are defined as follows.



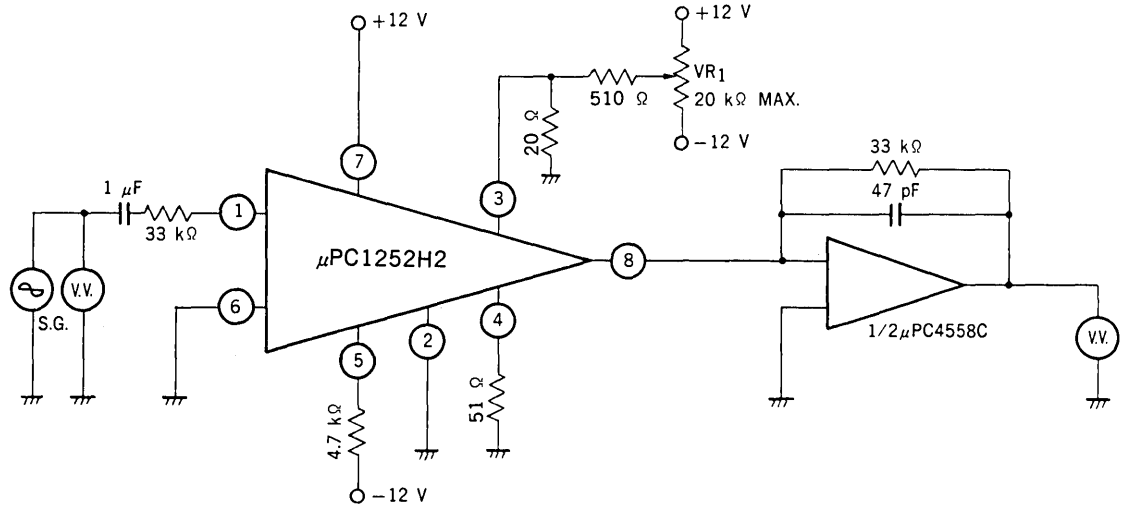
$$I_{SET} = \frac{V_{EE} - 4 \cdot V_{BE}}{R_{EXT}} = \frac{V_{EE} - 2.4}{R_{EXT}} = 2 \text{ mA}$$

TEST CIRCUIT

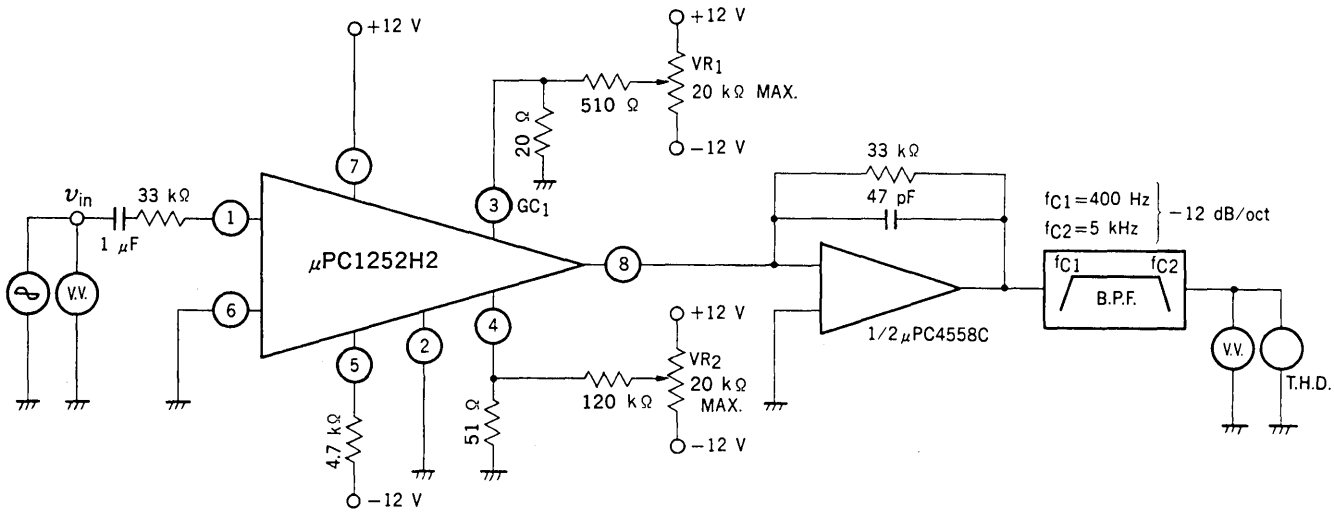
(1) I_{CC}



(2) V_C



(3) T.H.D. $_{1\sim3}$

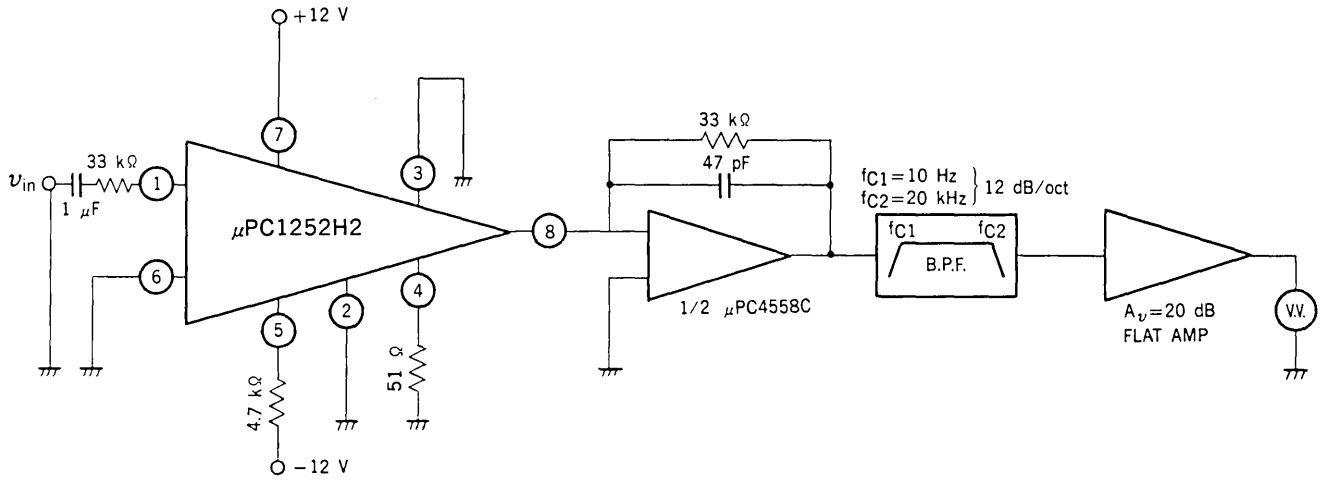


T.H.D.1; Make T.H.D. minimum with VR_2 after adjusting GC1 = 0 mV with VR_1 at V_{in} = 0 dBV

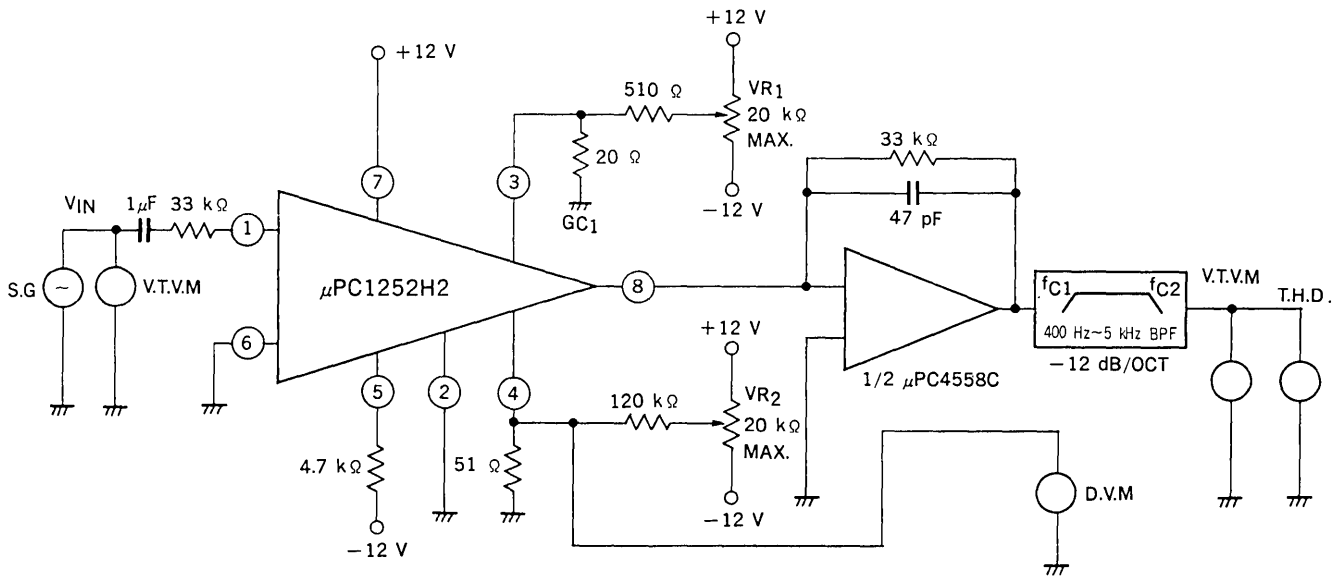
T.H.D.2; Make T.H.D. minimum with VR_2 after adjusting GC1 = −120 mV with VR_1 at V_{in} = −20 dBV

T.H.D.3; Make T.H.D. minimum with VR_2 after adjusting GC1 = +120 mV with VR_1 at V_{in} = 0 dBV

(4) V_{NO}

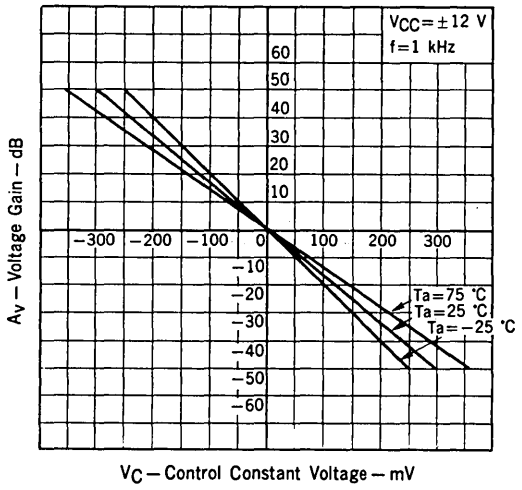


(5) V_{SYM}

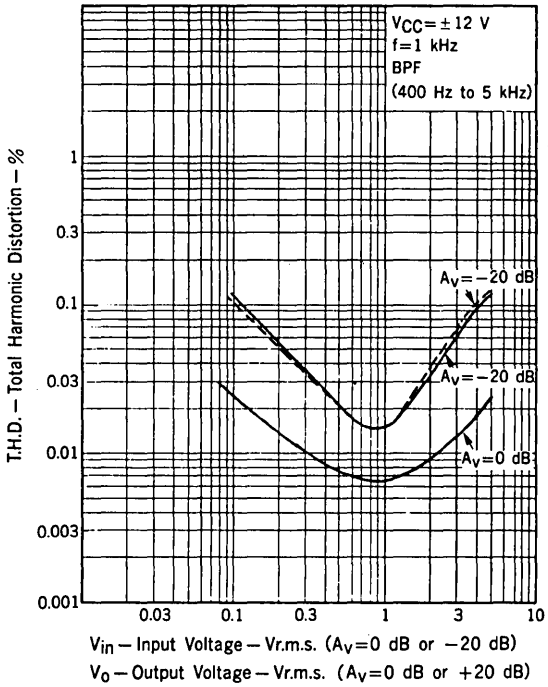


Make T.H.D. minimum with VR_2 after adjusting GC1 = 0 mV with VR_1 at V_{in} = 0 dBV and Measure Symmetry Control Voltage of 4 pin.

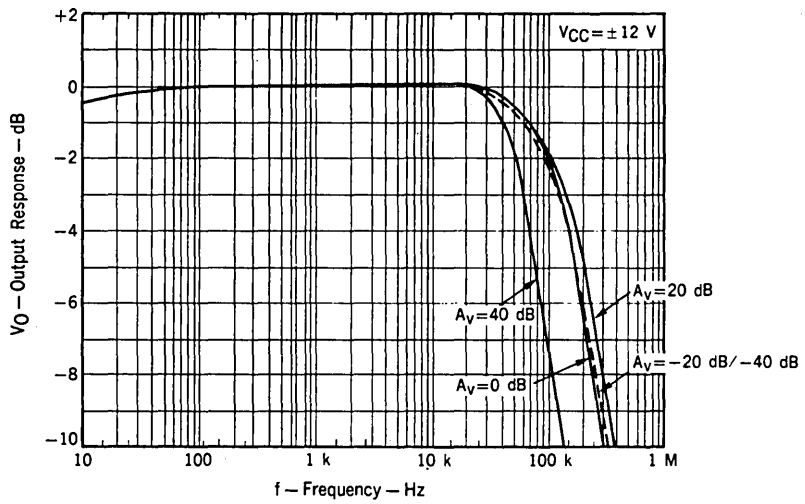
VOLTAGE GAIN vs.
CONTROL CONSTANT VOLTAGE



TOTAL HARMONIC DISTORTION vs.
INPUT VOLTAGE and OUTPUT VOLTAGE



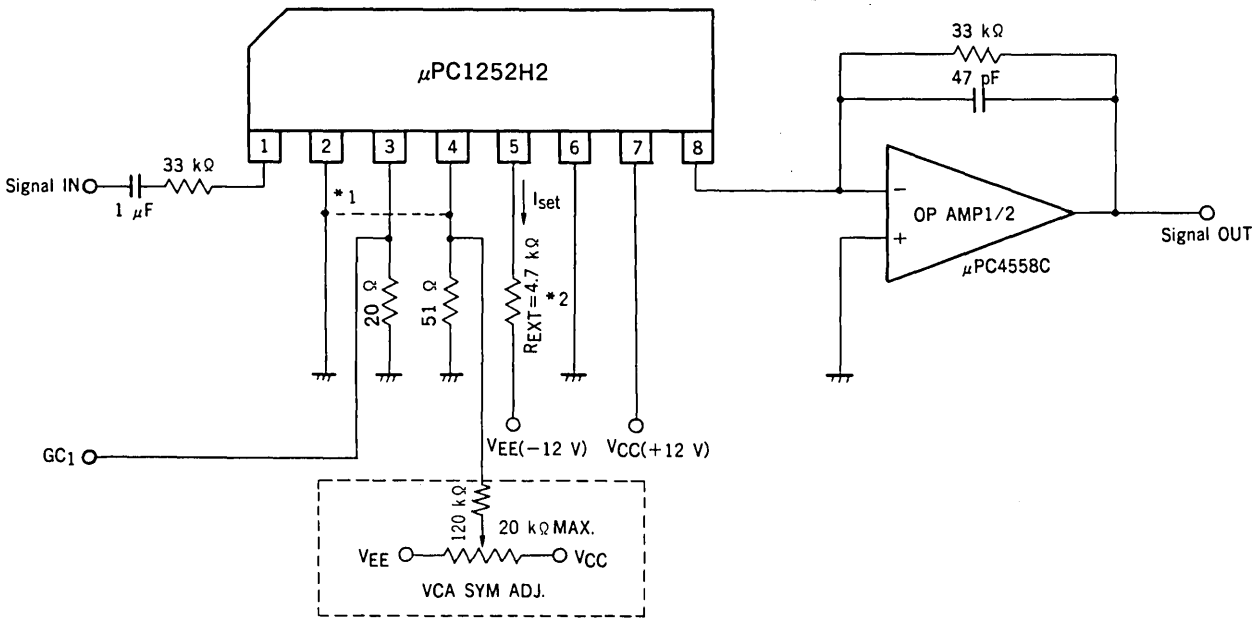
OUTPUT RESPONSE vs. FREQUENCY



Note for use

1. Since μPC1252H2 is designed for Noise Reduction System, recommend to use μPC1252H2 with μPC1253H2 (RMS Revel Sensor), which controls μPC1252H2, in case of composing dbx NR System.
2. Documents issued by dbx, in corporated have priority over NEC, such as application note or data about dbx NR system.
3. If you plan to use μPC1252H2 except dbx NR system, inform NEC of it as soon as possible.

APPLICATION CIRCUIT



*1. Possible to connect 4 pin to GND in case of using this IC at T.H.D. ≧ 0.05 %.

*2. I_{set} is set to be 2 mA at R_{EXT} = 4.7 kΩ, V_{CC} = 12 V, V_{EE} = −12 V, so readjust R_{EXT} in case that supply voltage is different from above.

GC1 is an input terminal of μPC1252H2 control voltage.

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1253H2

RMS LEVEL SENSOR FOR dbx NOISE REDUCTION SYSTEM

DESCRIPTION

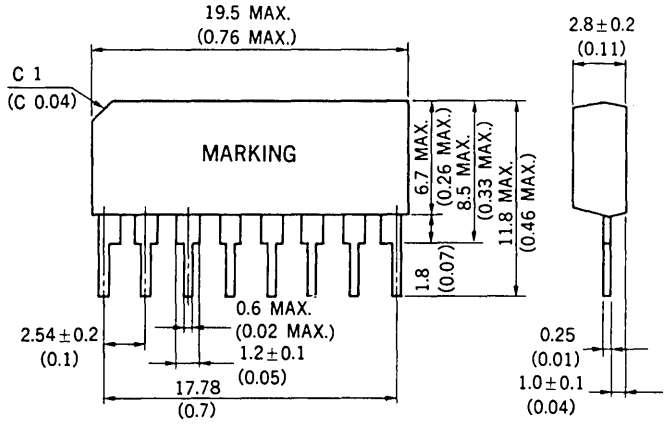
The μPC1253H2 is dbx noise reduction system RMS (Root Mean Square) level sensor, used in tape deck and other audio equipment.

The μPC1253H2 features high accurate RMS level sensor for wide input due to NEC's super low noise and high h_{FE} PNP process.

Since the package is 8 pin SIP, it can be built in a compact set.

PACKAGE DIMENSIONS

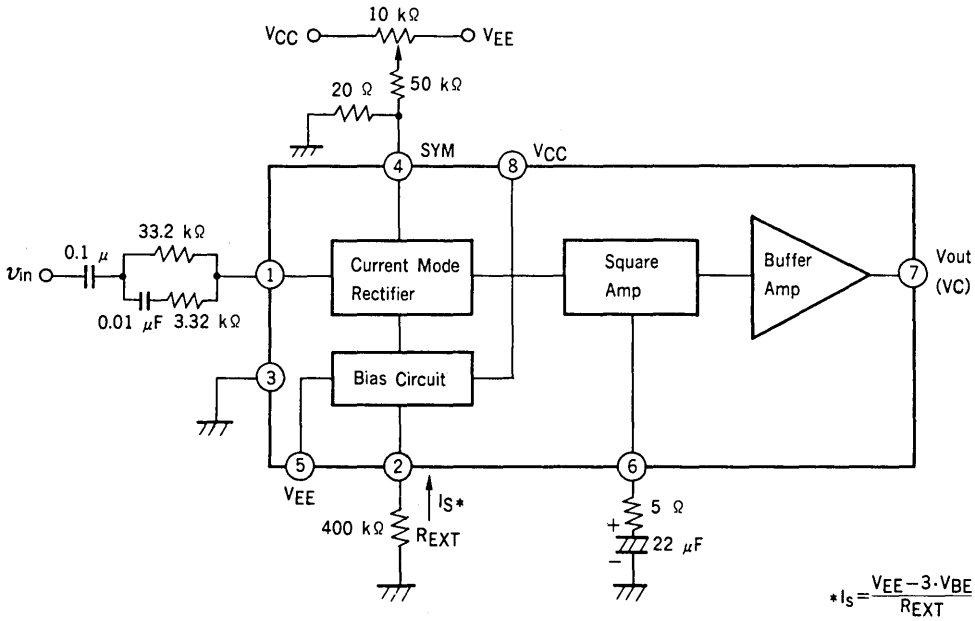
in millimeters (inches)



FEATURES

- Wide operating supply voltage — V_{CC} = ±4 to ±15 V (TYP. ±12 V)
- Excellent lineality Control Constant — V_C = 5.9 mV/dB
- Wider input range — v_{in} = −40 dBV to +10 dBV

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Supply Voltage	V_{CC}, V_{EE}	±15	V
Supply Current	I_{CC}	30	mA
Power Dissipation	P_D	330*	mW
Operating Temperature Range	T_{opt}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C

* Value at Ta = 75 °C

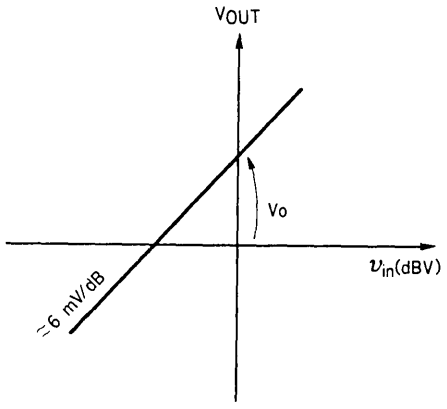
RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage	V_{CC}, V_{EE}	±4	±12	±15	V
Input Level Range	v_{in}	−40		+10	dBV
Bias Current	I_S		24		μA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C, V_{CC} = +12 V, V_{EE} = −12 V, f = 1 kHz, Z_{in} = 33 kΩ)

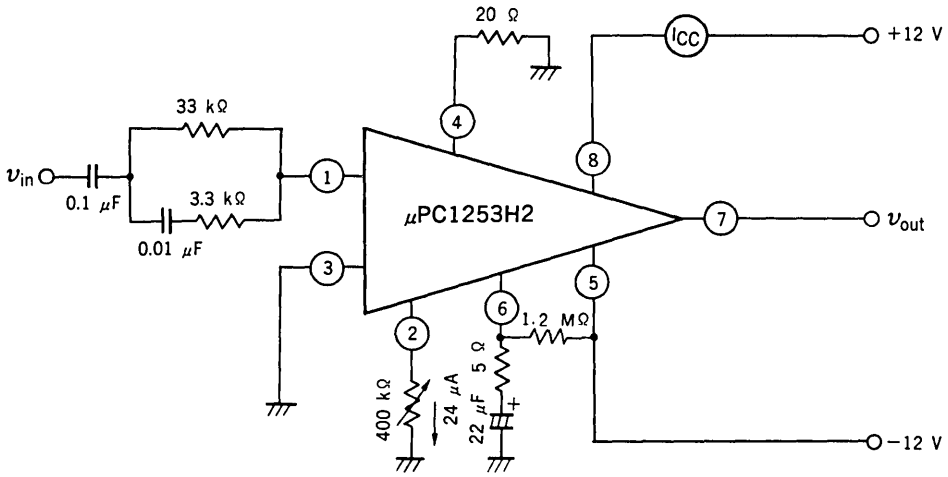
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Current	I_{CC}		0.9	2.0	mA	No Signal
Output Level	V_O*	111	136	161	mV	V_{IN} = 0 dBV
Control Constant	V_C	5.8	5.9	6.1	mV/dB	v_{in} = −40 dBV to +10 dBV

* Output Level is defined as follows.

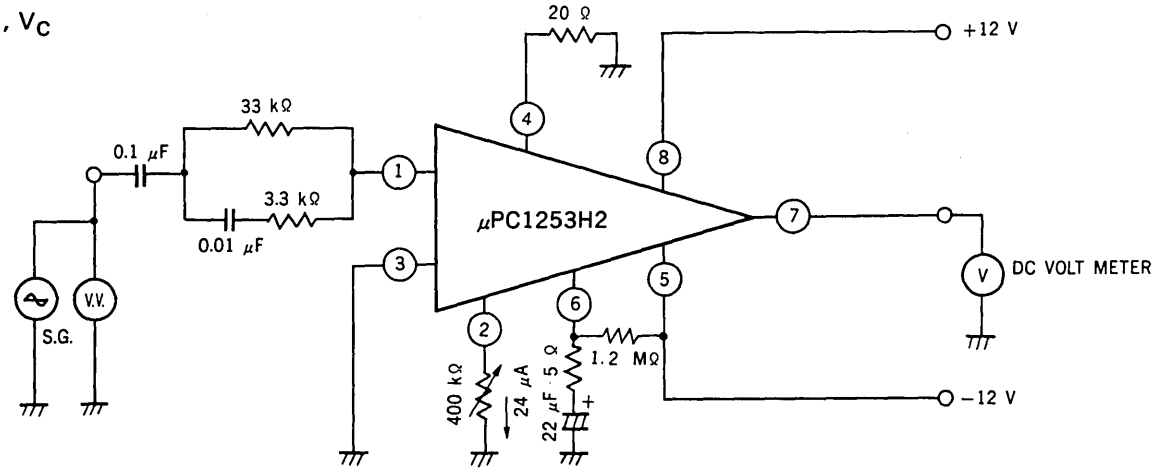


TEST CIRCUIT

(1) I_{CC}



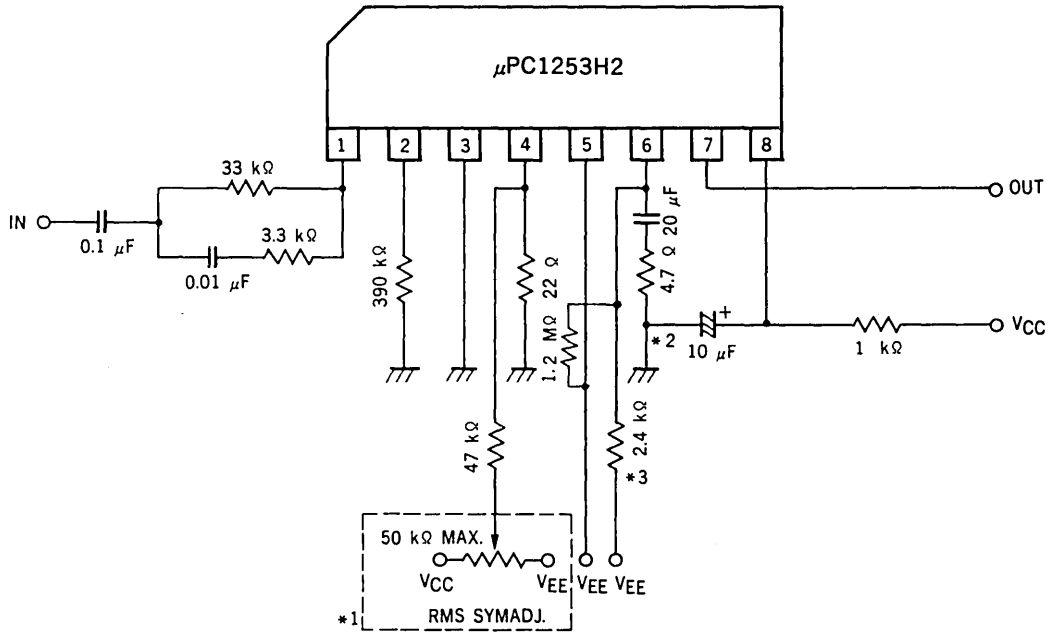
(2) V_O, V_C



Note for use

1. Since μPC1253H2 is designed for dbx Noise Reduction System, recommend to use μPC1253H2 with μPC1252H2 (VCA) in case of composing dbx NR system.
2. Documents issued by dbx incorporated have priority over NEC, such as application note or data about dbx NR system.

APPLICATION CIRCUIT



*1. Possible to omit RMS SYM.ADJ. in case of using this IC with μPC1252H2 at T.H.D. ≧0.05 %.

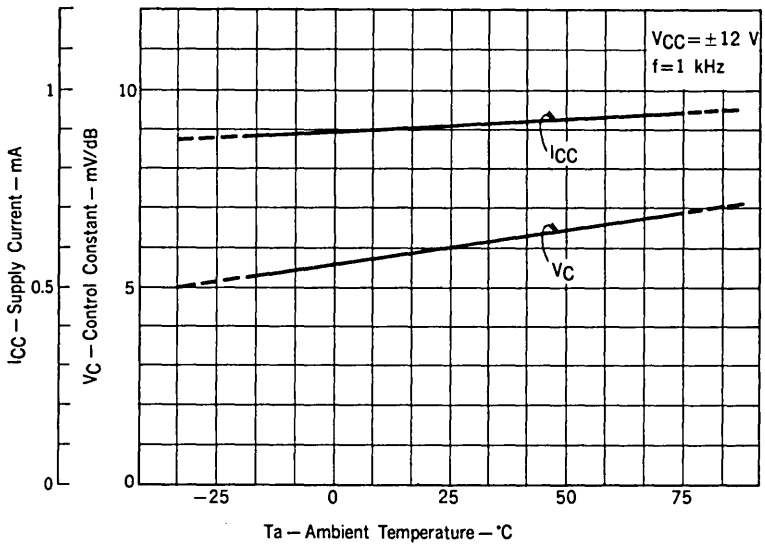
*2. Make GND common about these terminals.

*3. This resistor is for RMS time constant.

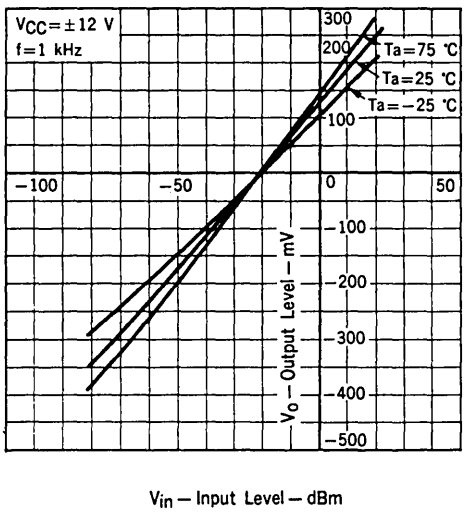
Connect 7 PIN OUT to GC1 of μPC1252H2 (VCA).

TYPICAL CHARACTERISTICS (Ta = 25 °C)

SUPPLY CURRENT, CONTROL CONSTANT vs. AMBIENT TEMPERATURE



OUTPUT LEVEL vs. INPUT LEVEL



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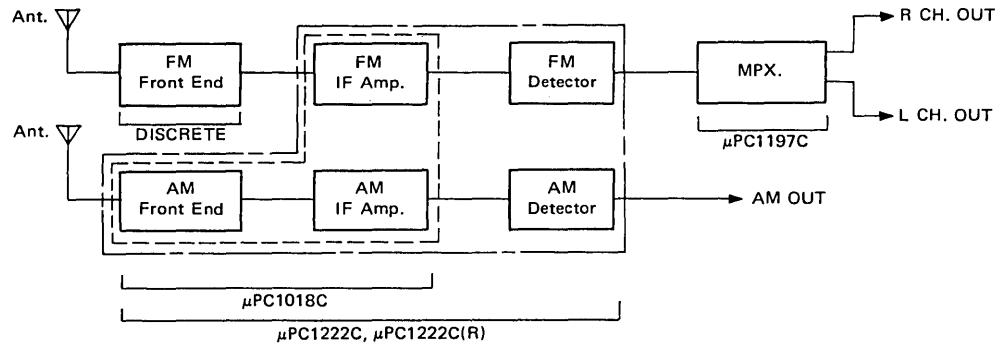
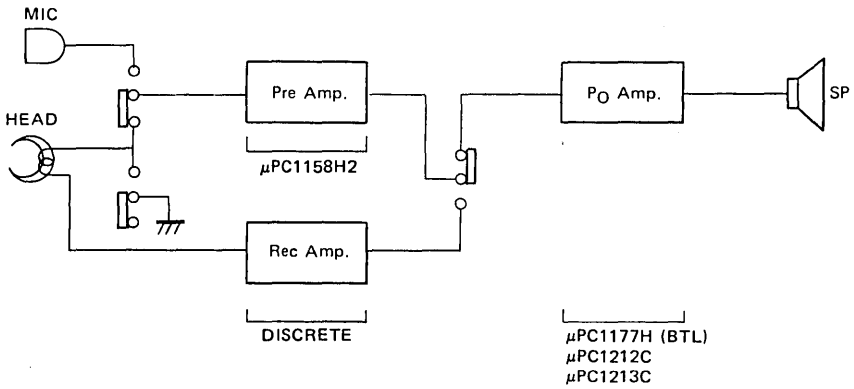
BLOCK DIAGRAM

Tuner Block

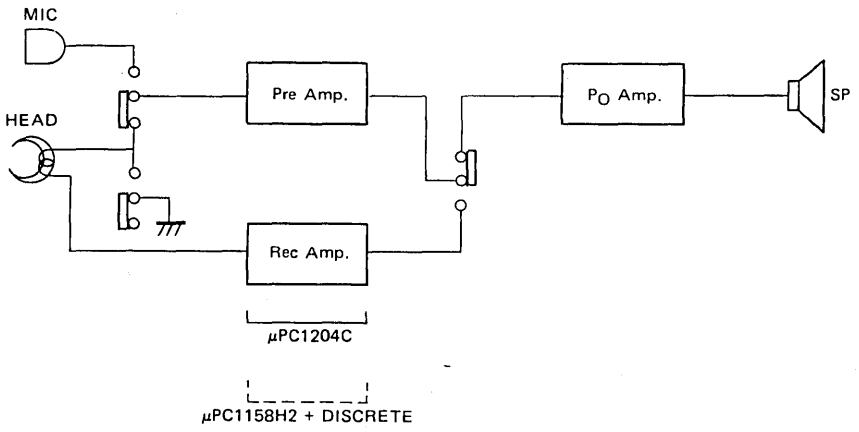


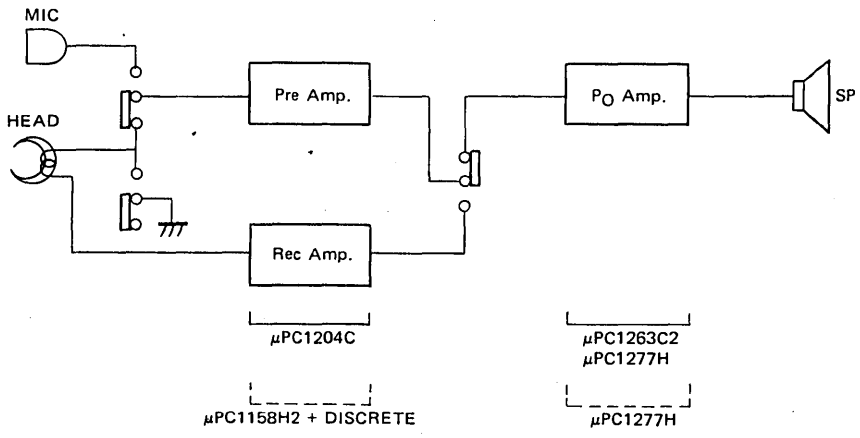
AF Block

(1) Monaural Radio Cassette

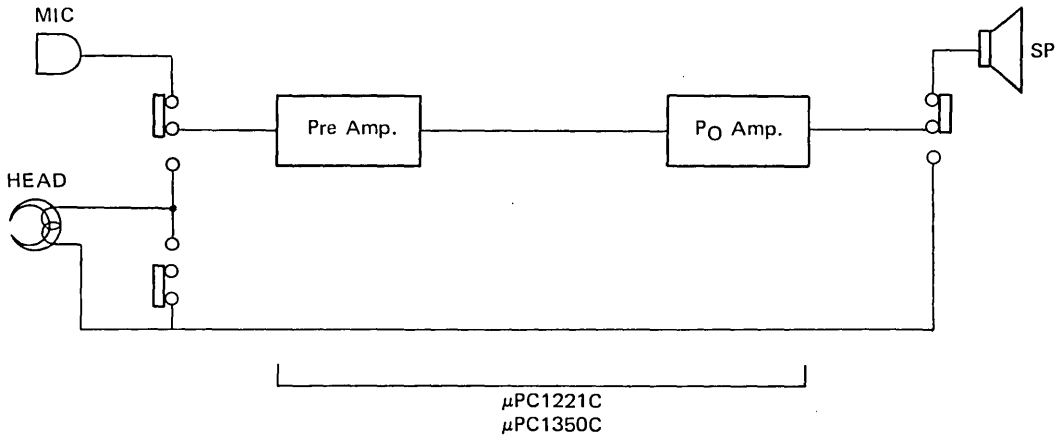


(2) Stereo Radio Cassette

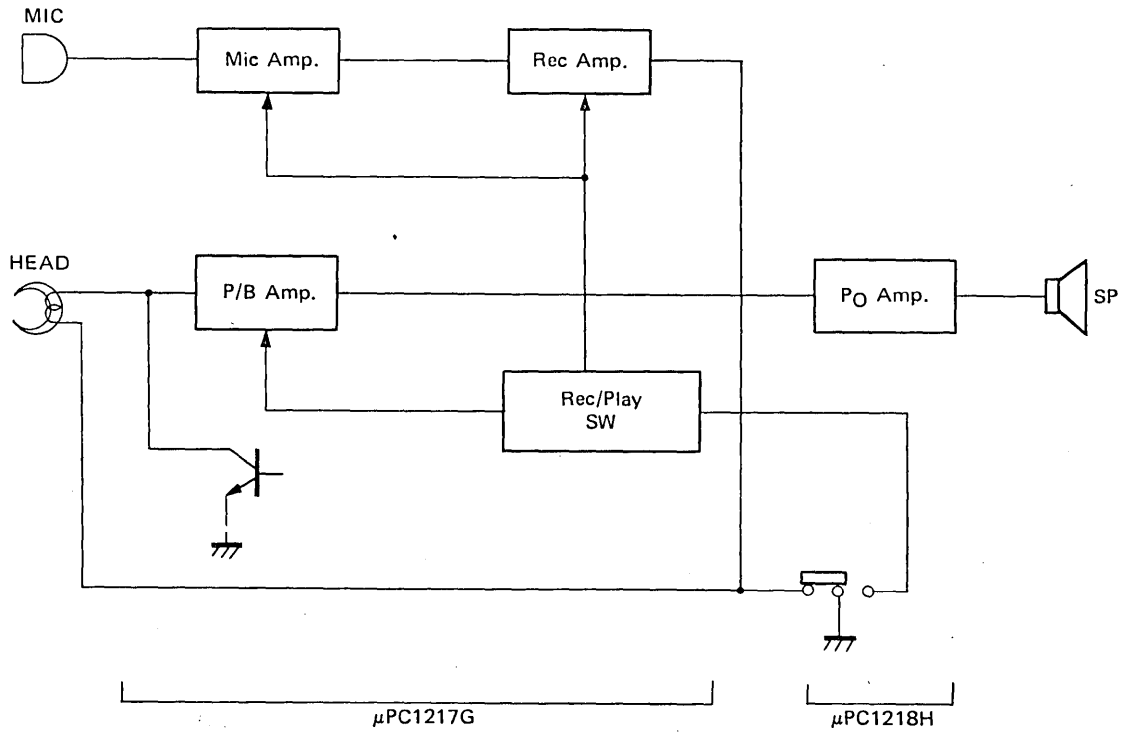




(3) Cassette Tape Recorder



(4) Mini & Micro Cassette



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1018C

AM TUNER, AM/FM-IF AMPLIFIER CIRCUIT
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

DESCRIPTION

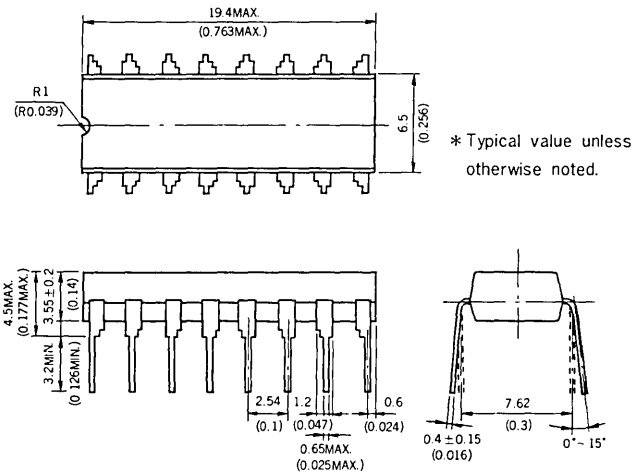
The μPC1018C is a silicon monolithic integrated circuit designed for AM/FM radios and cassette tape recorders with an AM/FM radio.

The μPC1018C contains a AM tuner and FM-IF amplifiers.

FEATURES

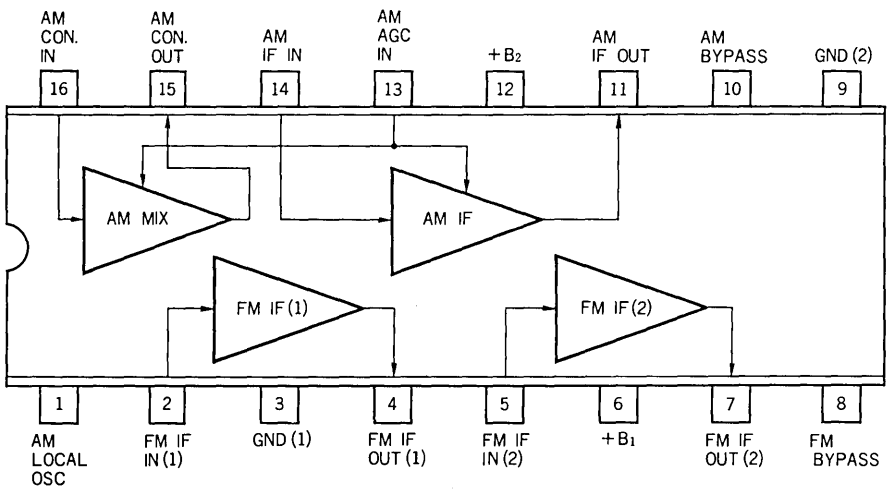
- Wide operating voltage. V_{CC} = 2.5 ~ 6.0V
- Excellent low voltage characteristics.
- High gain FM-IF amplifiers.
- The AM stage is composed of a mixer, a local oscillator, a IF amplifier and an AGC circuit.
- The AM stage has an excellent AGC characteristic and low distortion.

PACKAGE DIMENSIONS in millimeters (inches)



* Typical value unless otherwise noted.

BLOCK DIAGRAM (Top View)



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Supply Voltage	V_{CC}	9.0	V
Package Dissipation	P_D	350*	mW
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

*Ta = 75°C

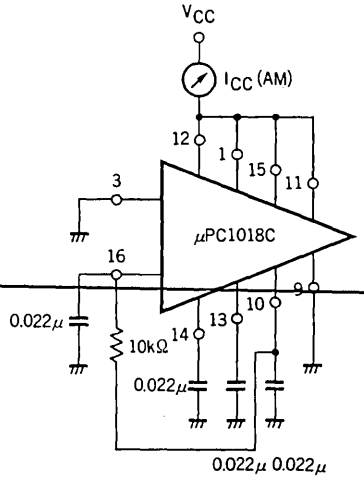
RECOMMENDED OPERATING CONDITION (Ta = 25°C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	2.5	4.0	6.0	V

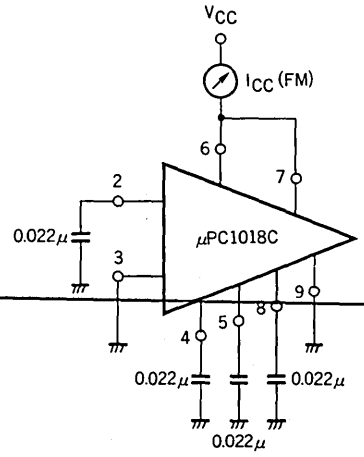
ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{CC} = 4.0V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	TEST CIRCUIT
Circuit Current	I_{CC}(AM)	4.5	8.0	11.5	mA	No Signal (AM)	1
Voltage Gain (MIX)	A_V (MIX)	7.5	11.5	15.5	dB	f=1MHz, R_G=50Ω, R_L=1kΩ (AM)	3
Voltage Gain (IF)	A_V (IF)	44.0	50.0	56.0	dB	f=455kHz, R_G=50Ω, R_L=330Ω (AM)	3
Circuit Current	I_{CC}(FM)	5.0	9.0	13.0	mA	No Signal (FM)	2
Voltage Gain (IF_1)	A_V (IF_1)	38.0	42.0	46.0	dB	f=10.7MHz, R_G=50Ω, R_L=1kΩ (FM)	4
Voltage Gain (IF_2)	A_V (IF_2)	27.0	33.0	39.0	dB	f=10.7 MHz, R_G=50Ω, R_L=330Ω (FM)	4

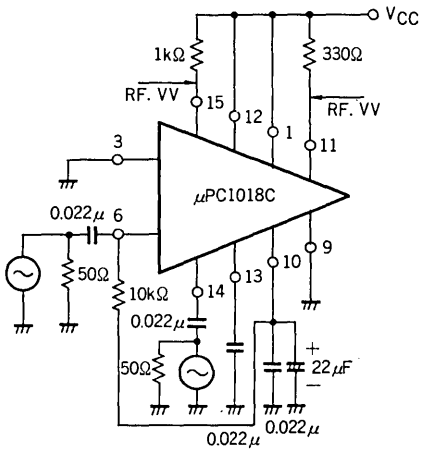
TEST CIRCUIT 1



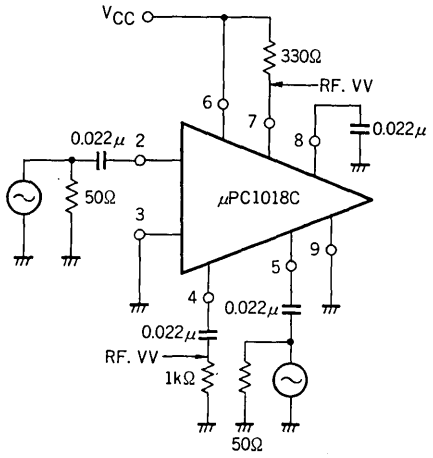
TEST CIRCUIT 2



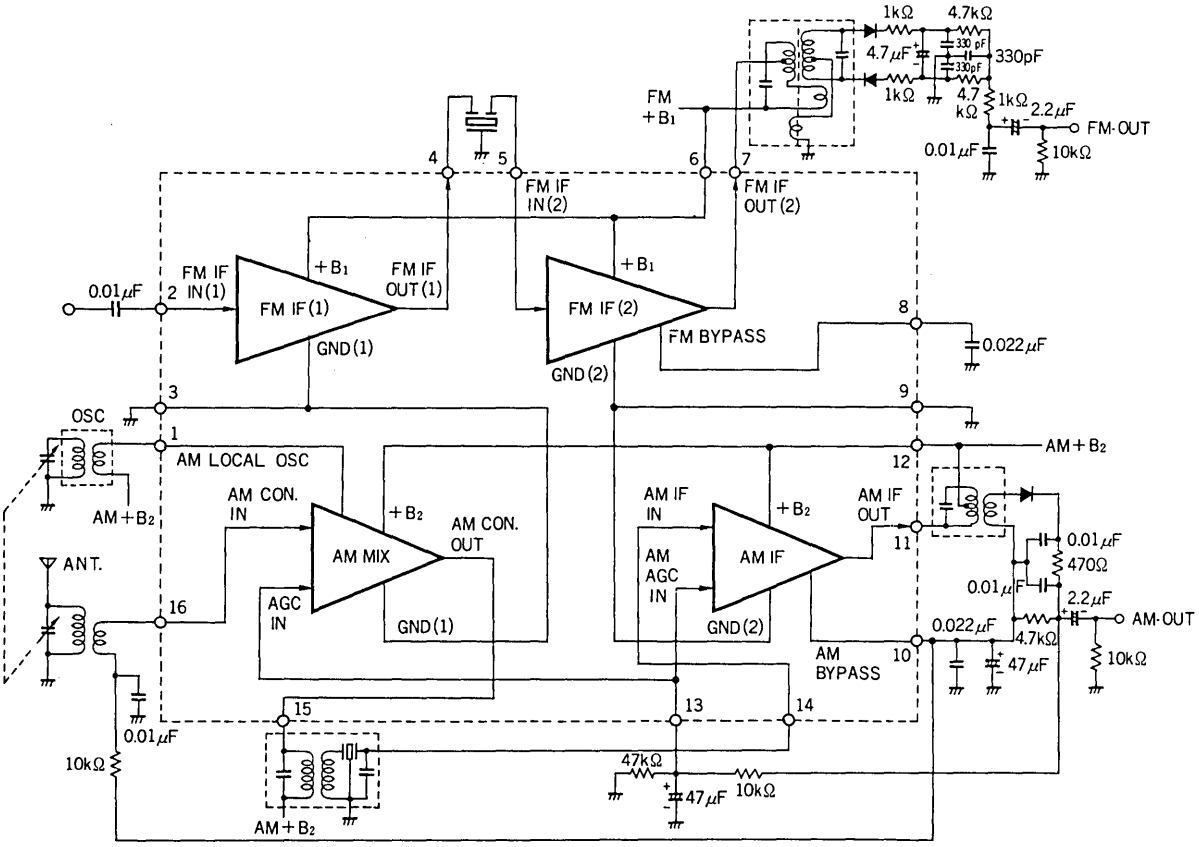
TEST CIRCUIT 3



TEST CIRCUIT 4



TYPICAL APPLICATION

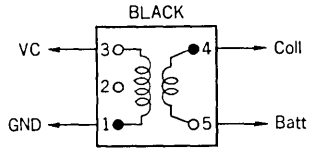


COIL SPECIFICATIONS

① AM LOCAL OSCILATION COIL (MW) 7BR-4398X (TOKO)

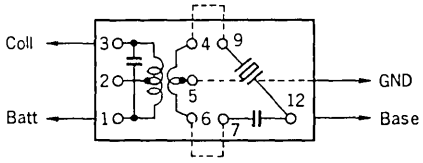
TYPE NO. 7P
BODY COLOR BLACK

1−3 65T
4−6 11T



L=150μH (±6%)
Qu>80 (f=1.4MHz)

② AM IF COIL CFZ-455C (TOKO)

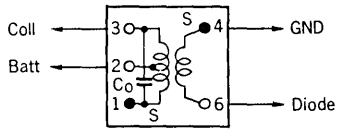


BAND WIDTH 6kHz MIN.
SELECTIVITY (±10kHz DETUNING) 20dB MIN.

③ AM DETECTION COIL (455kHz) 7LC-252222No. (TOKO)

TYPE NO. 7P
BODY COLOR BLACK

1−3 146T
2−3 37T
4−6 33T

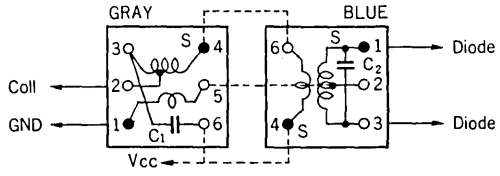


CAPACITOR Co·····180pF
Qu·····70±20%

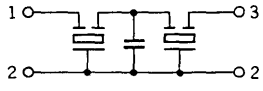
④ FM DETECTION COIL (10.7MHz) (TOKO)

		CAPACITOR						
PLIMARY	119AC-470085L$_8$ (GRAY)	47pF(C_1)	4−2	5½T	2−3	8T	1−5	5½T
SECONDARY	119FC-560061N$_6$ (BLUE)	56pF(C_2)	1−2	6T	2−3	6T	4−6	1T

TYPE NO. 7P



⑤ FM CERAMIC FILTER (10.7MHz) CFS-107M (TOKO)

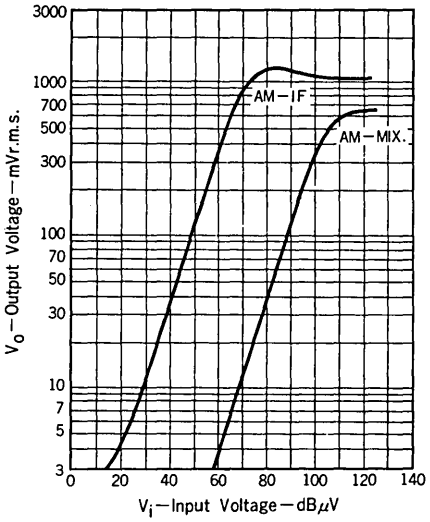


1. INPUT
2. GND
3. OUTPUT

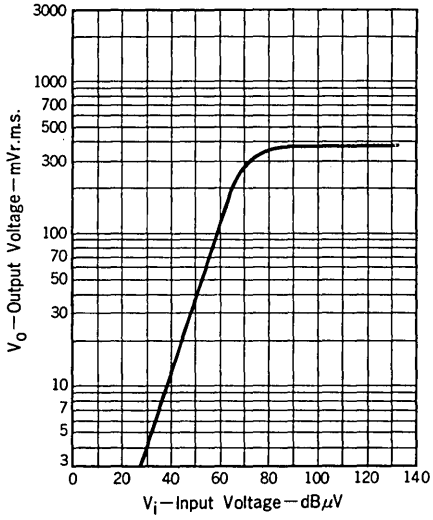
− 3dB BAND WIDTH·····300±50kHz
−20dB BAND WIDTH·····600kHz(MAX.)
INSERTION LOSS·····6dB(MAX.)

TYPICAL CHARACTERISTICS (Ta = 25°C)

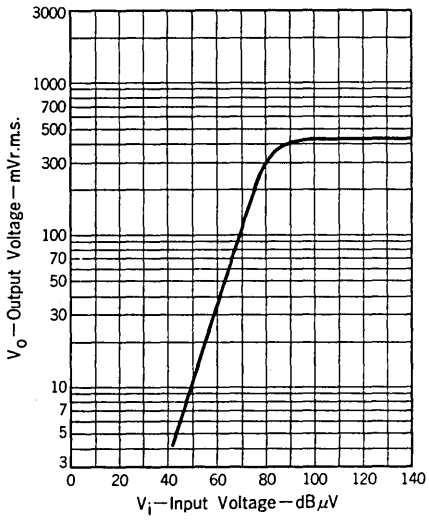
AM–MIX, AM–IF
OUTPUT VOLTAGE vs. INPUT VOLTAGE



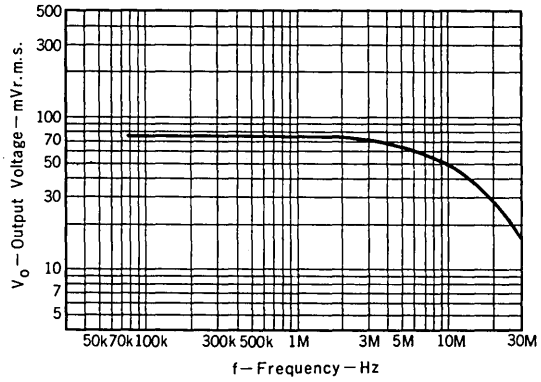
FM–IF$_1$
OUTPUT VOLTAGE
vs. INPUT VOLTAGE



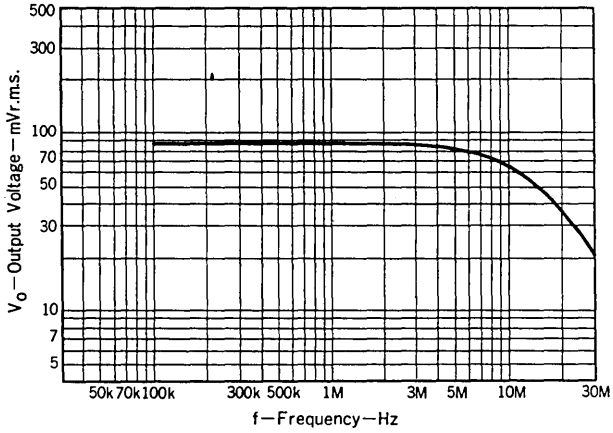
FM–IF$_2$
OUTPUT VOLTAGE vs.
INPUT VOLTAGE



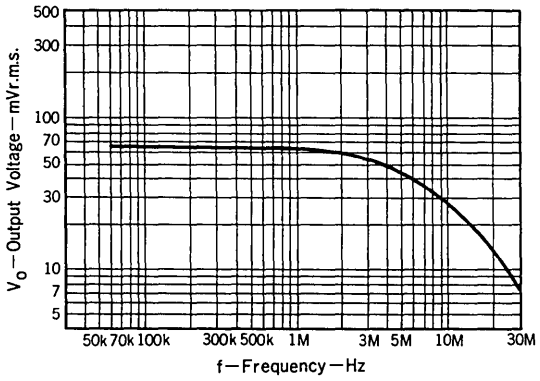
AM–MIX
OUTPUT VOLTAGE vs. FREQUENCY



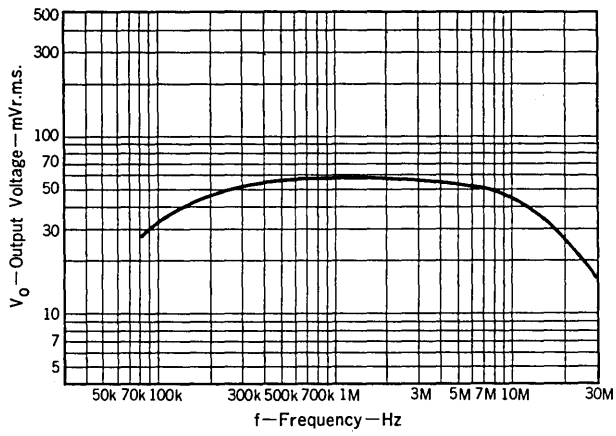
FM–IF$_1$
OUTPUT VOLTAGE vs. FREQUENCY



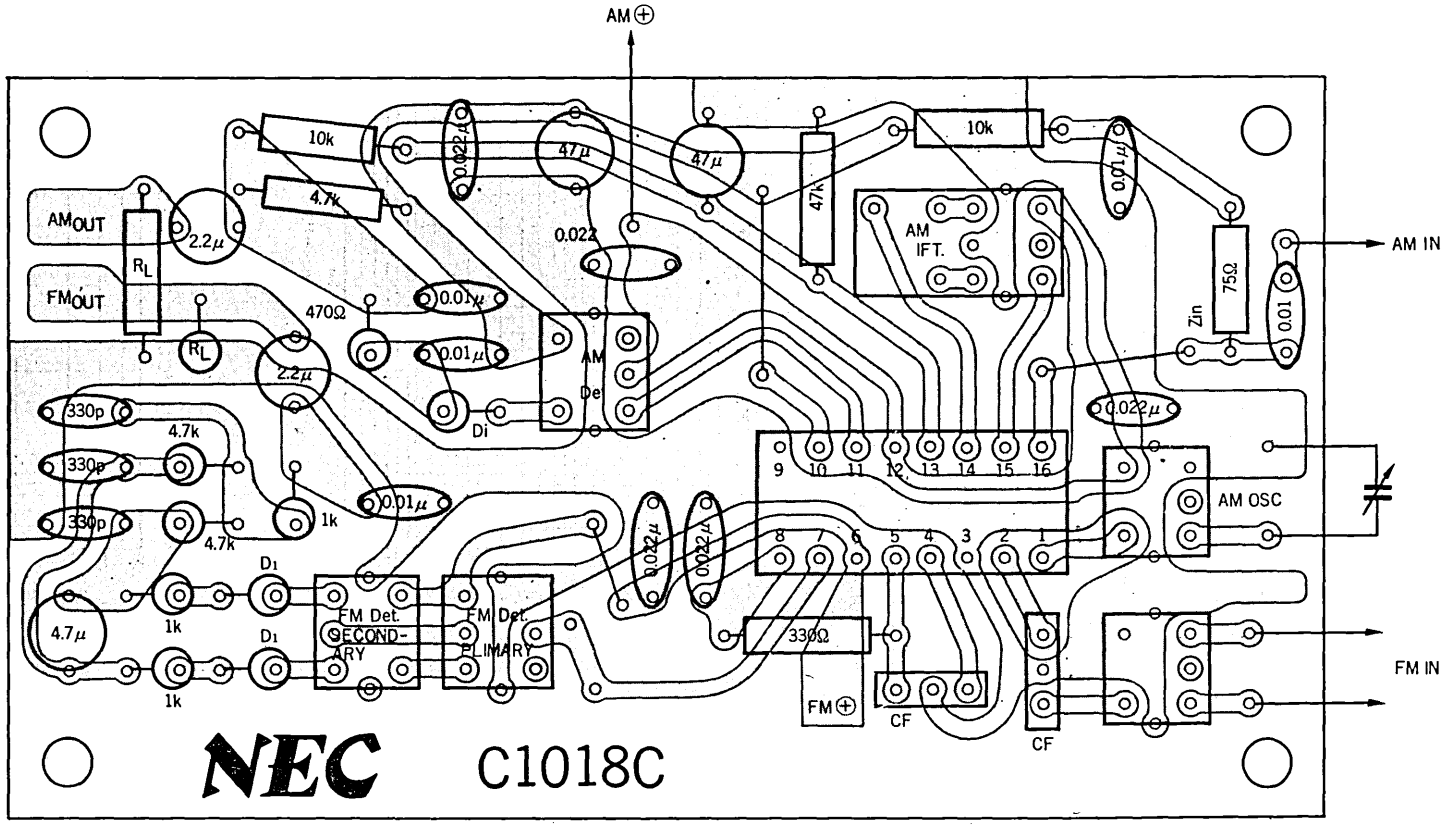
AM–IF
OUTPUT VOLTAGE vs. FREQUENCY



FM–IF
OUTPUT VOLTAGE vs. FREQUENCY



P.W. BOARD PATTERN



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1222C, μPC1222C(R)

AM TUNER, FM IF SYSTEM WITH QUADRATURE DETECTOR SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

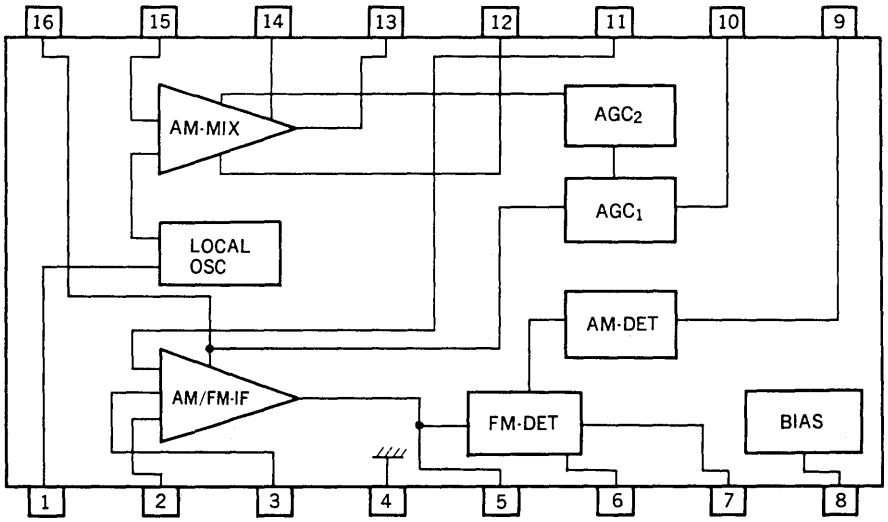
DESCRIPTION

The μPC1222 is a low voltage silicon monolithic IC. It is designed for using in AM tuner and FM-IF. μPC1222 contains an AM Mixer, AM/FM IF amplifier, AM detector, FM detector and also AGC circuit. This IC is suitable for using in AM/FM radio, radio cassette etc..

FEATURES

- Wide operating voltage. V_{CC}=2.0 V–6.0 V
- Excellent low voltage characteristics.
- AM stage is composed a Mixer, local oscillator, IF amplifier, AM detector and AGC circuit.
- FM stage is composed a high gain FM-IF amplifier and FM detector.
- The AM stage has an excellent AGC characteristic and low distortion.
- μPC1222C(R) is designed for upper heterodyne.
- μPC1222C is designed for lower heterodyne.

BLOCK DIAGRAM (Top View)

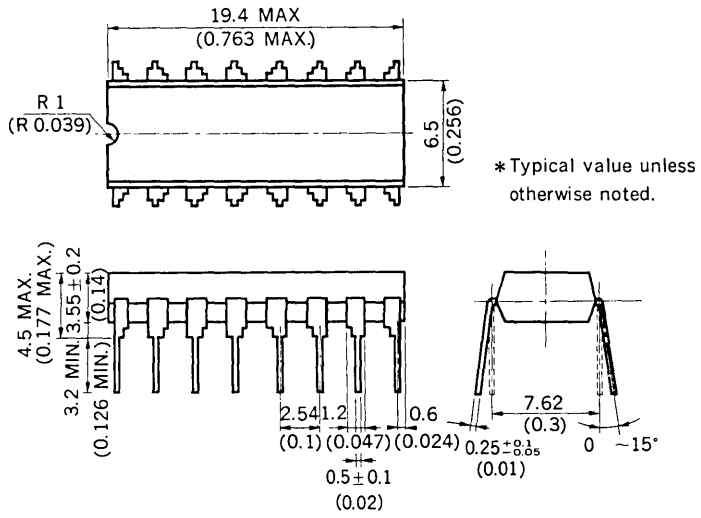


FUNCTION

AM Stage ..... MIXER CIRCUIT
LOCAL OSC
IF AMPLIFIER
DETECTOR CIRCUIT
AGC CIRCUIT

FM Stage ..... IF AMPLIFIER
DETECTOR CIRCUIT

PACKAGE DIMENSIONS in millimeters (inches)



CONNECTION DIAGRAM

Pin No.	CONNECTION	Pin No.	CONNECTION
1	AM LOCAL OSC	9	AM OUTPUT
2	IF BYPASS	10	AGC INPUT
3	FM IF INPUT	11	AM IF INPUT
4	GND	12	AM MIX BIAS
5	DET. INPUT (1)	13	AM MIX OUT
6	DET. INPUT (2)	14	AM RF AGC BYPASS
7	FM OUTPUT	15	AM MIX INPUT
8	V_{CC}	16	AM IF AGC BYPASS

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Supply Voltage	V_{CC}	9.0	V
Package Dissipation	P_D	350*	mW
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C
		*Ta = 75 °C	

RECOMMENDED OPERATING CONDITION (Ta = 25 °C)

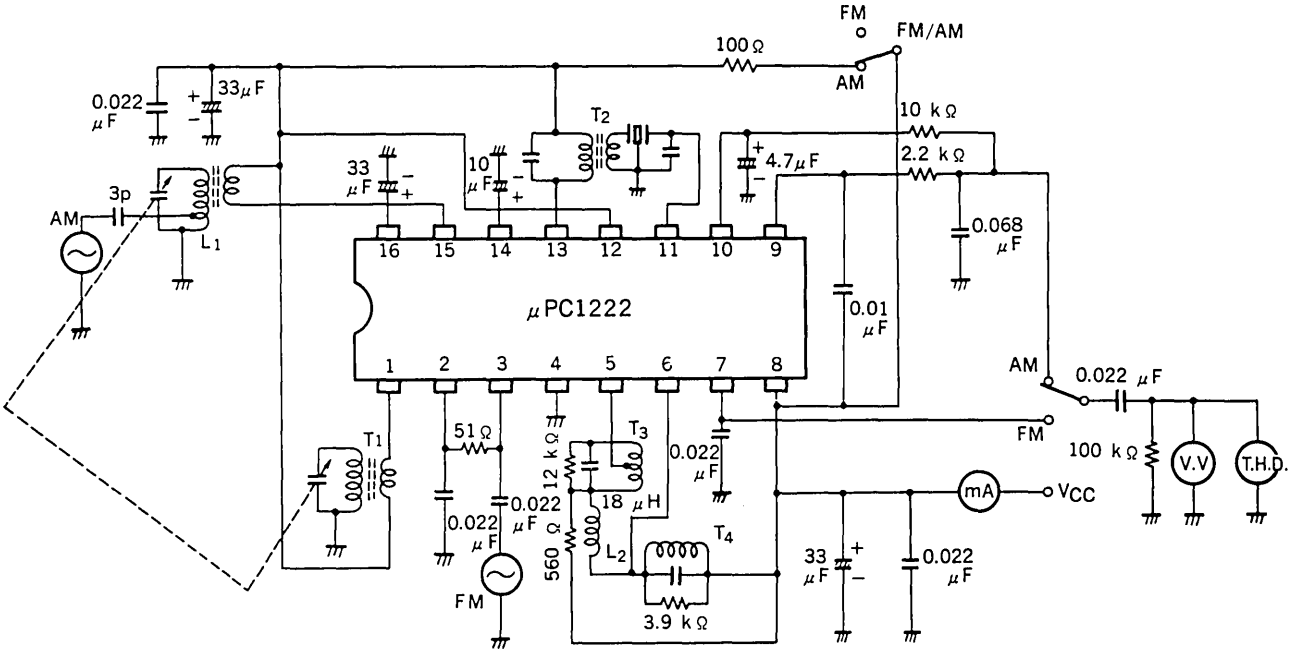
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	2.0	4.0	6.0	V

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

(V_{CC} = 4 V FM: f = 10.7 MHz, Δf = ± 22.5 kHz DEV.
AM: f = 1 MHz, MOD. = 30 % f_{MOD} = 400 Hz)

	CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
FM STAGE	Circuit Current	I_{CC-FM}	6.5	10	15	mA	No Signal
	Detector Output Voltage	V_{O-FM}	35	50	70	mVr.m.s.	V_i = 80 dBμV
	Input Limiting Voltage	$V_{i(lim)}$	33	39	45	dBμV	−3 dB point from V_O with 100 dBμV input
	Signal to Noise Ratio	S/N_{-FM}	50	60		dB	V_i = 80 dBμV
	Total Harmonic Distortion	$T.H.D._{-FM}$		0.2	0.8	%	V_i = 80 dBμV
	AM Rejection Ratio	A.M.R.	25	35		dB	V_i = 80 dBμV AM: 30 % MOD.
	Drop Voltage Gain Loss	ΔA_{V-FM}		1.5	5.0	dB	V_O = 5 mVr.m.s. V_{CC} = 4 → 2 V
AM STAGE	Circuit Current	I_{CC-AM}	6	12	18	mA	No Signal
	MAX. Sensitivity	V_{i-AM}	28	35	42	dBμV	V_O = 10 mVr.m.s.
	Detector Output Voltage	V_{O-AM}	25	34	50	mVr.m.s.	V_i = 100 dBμV
	Signal to Noise Ratio	S/N_{-AM}	45	51		dB	V_i = 100 dBμV
	Oscillation Voltage	V_{OSC}		150		mVr.m.s.	f_{OSC} = 1 455 kHz
	Total Harmonic Distortion	T.H.D.-AM		0.5	2.0	%	V_i = 100 dBμV
	Drop Voltage Gain Loss	ΔA_{V-AM}		5	10	dB	V_O = 10 mVr.m.s. V_{CC} = 4 → 2 V

TEST CIRCUIT



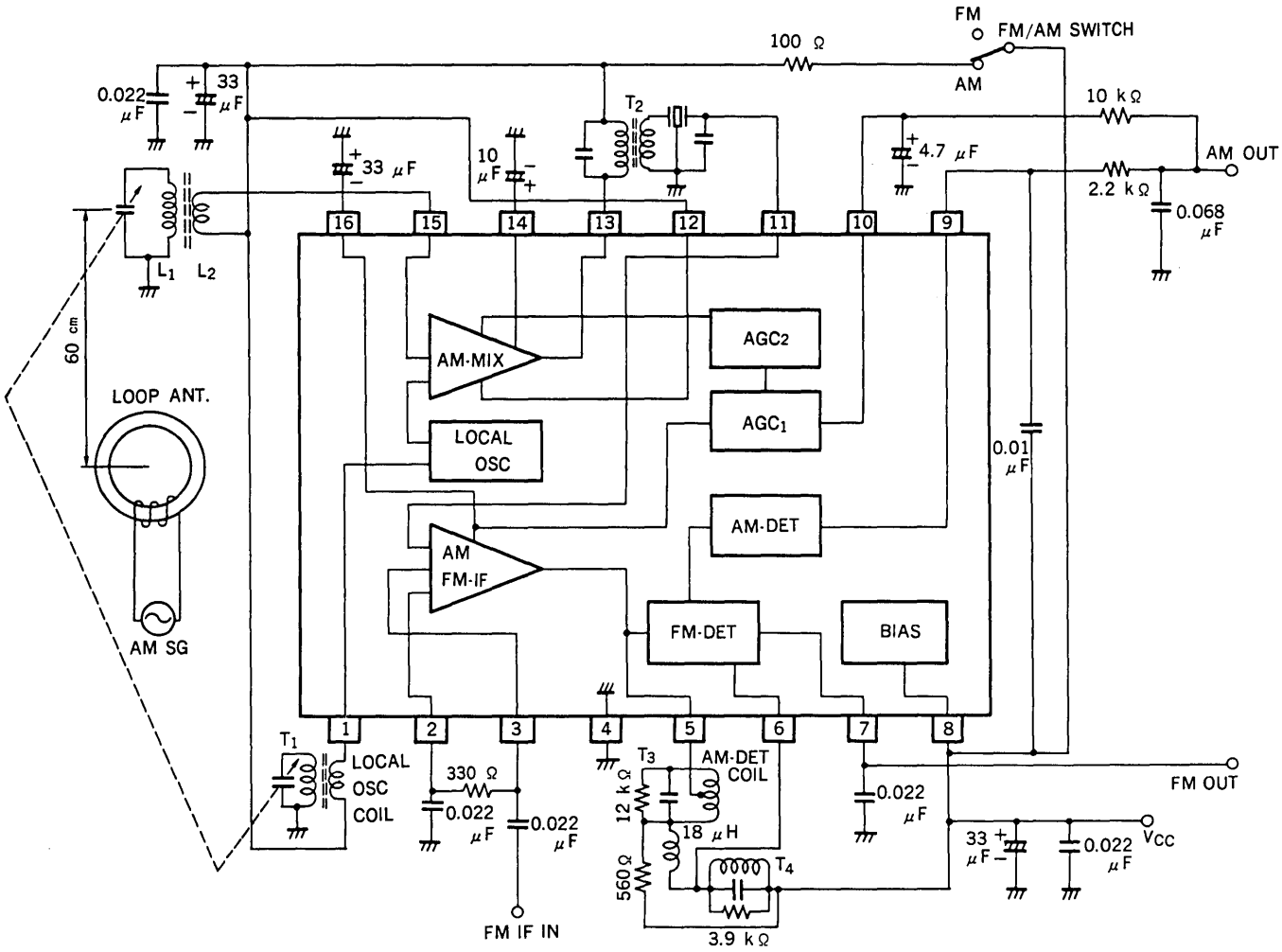
L_1:	AM ANT. COIL	25A-1195-08 (CORIN)
T_1:	AM LOCAL OSCILLATION COIL (MM)	26-1791-13 (CORIN)
T_2:	AM IF COIL	CFZ-455C (TOKO)
T_3:	AM DETECTION COIL (455 kHz)	5251 (TOKO)
T_4:	FM DETECTION COIL (10.7 MHz)	12747 (TOKO)
L_2:	PHASE SHIFT INDUCTOR	7BA 180JH (TOKO)

AM STAGE REFERENCE CHARACTERISTICS

(V_{CC} = 4 V, f = 1 MHz, MOD = 30 %, f_{MOD} = 400 Hz, at APPLICATION CIRCUIT)

CHARACTERISTIC	SYMBOL	TYP.	UNIT	TEST CONDITION
Usable Sensitivity	$V_{i\text{-}S/N}$	48	dBμV/m	S/N=20 dB
Maximum Sensitivity	$V_{i\text{-}AM}$	35	dBμV/m	V_O=10 mVr.m.s.
Detector Output	$V_{O\text{-}AM}$	34	mVr.m.s.	V_i=100 dBμV/m
S/N Ratio	S/N	51	dB	V_i=100 dBμV/m
Total Harmonic Distortion	T.H.D.	0.5	%	MOD=30 %, V_i=100 dBμV/m
Drop Voltage Gain Loss	$\Delta A_{V\text{-}AM}$	5	dB	V_O=10 mVr.m.s., V_{CC}=4 → 2 V

TYPICAL APPLICATION

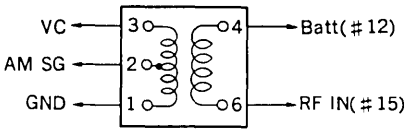


T_1:	AM LOCAL OSCILLATION COIL (MM)	26-1791-13 (CORIN)
T_2:	AM IF COIL	CFZ-455C (TOKO)
T_3:	AM DETECTION COIL (455 kHz)	5251 (TOKO)
T_4:	FM DETECTION COIL (10.7 MHz)	12747 (TOKO)

AM BAR ANT
CORE: ϕ 10 x 80 mm
L_O=600 μH
Q=220
L_1: L_2=107 : 25

COIL SPECIFICATIONS

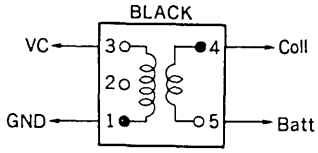
(1) ANTENNA COIL (MW) 25A-1195-08 (CORIN)



L_o = 650 μH
Q_o = 210±20 % (at 796 kHz)
1–2 25T 2–3 82T
1–3 107T 4–6 10T

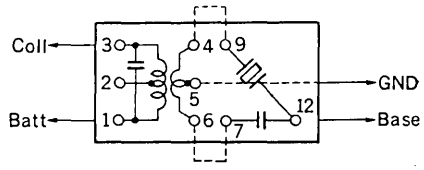
(2) AM LOCAL OSCILLATION COIL (MW) (CORIN)

TYPE NO. 7P 1–3 99T
BODY COLOR BLACK 4–6 11T



L=260 μH (±6 %)
Qu>80 (f=1.4 MHz)

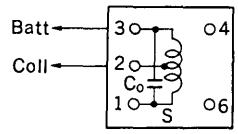
(3) AM IF COIL CFZ-455C (TOKO)



BANDWIDTH 6 kHz MIN.
SELECTIVITY (±10 kHz DETUNING) 20 dB MIN.

(4) AM DETECTION COIL (455 kHz) 5251 (TOKO)

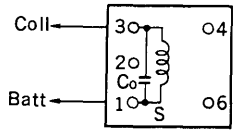
TYPE NO. 7P 1–2:2–3=1:1
BODY COLOR BLACK



CAPACITOR Co ..... 180 pF
Qu ..... 70±20 %

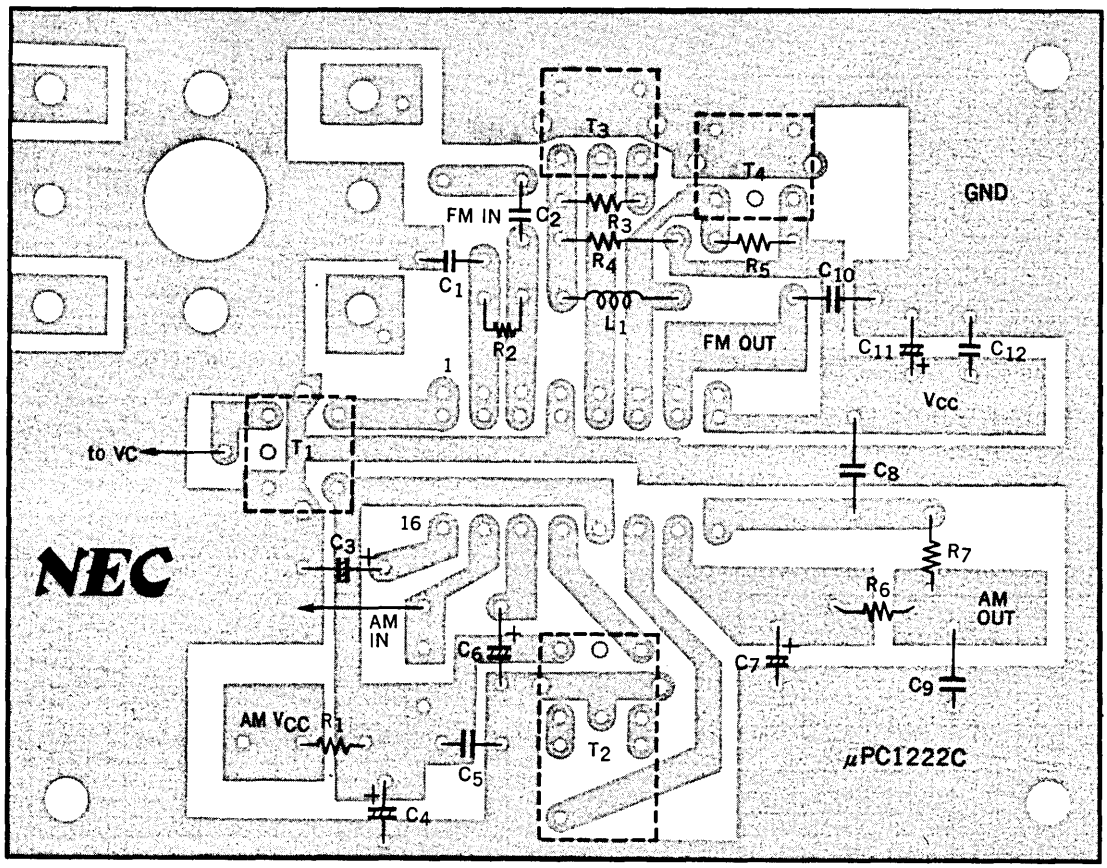
(5) FM DETECTION COIL (10.7 MHz) 12747 (TOKO)

TYPE NO. 7P
BODY COLOR BLACK



CAPACITOR Co ..... 82 pF
Qu ..... 70±20 %

P.C. BOARD PATTERN



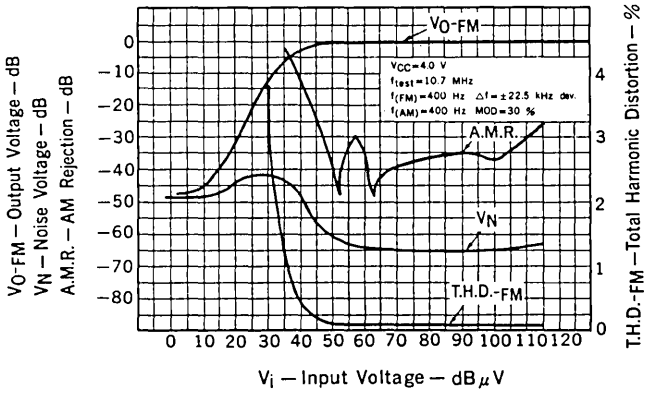
R_1	100 Ω	C_1	0.022 μF
R_2	51 Ω	C_2	0.022 μF
R_3	12 kΩ	C_3	33 μF
R_4	560 Ω	C_4	33 μF
R_5	3.9 kΩ	C_5	0.022 μF
R_6	2.2 kΩ	C_6	10 μF
R_7	10 kΩ	C_7	4.7 μF
		C_8	0.01 μF
		C_9	0.068 μF
		C_{10}	0.022 μF
		C_{11}	33 μF
		C_{12}	0.022 μF

T_1:	AM LOCAL OSC COIL	26-1791-13 (CORIN)
T_2:	AM IF COIL	CFZ-455C (TOKO)
T_3:	AM DET. COIL	5251 (TOKO)
T_4:	FM DET. COIL	12747 (TOKO)
L_1:	PHASE SHIFT INDUCTOR : 7BA 180JH (TOKO)	

TYPICAL CHARACTERISTICS (Ta = 25 °C)

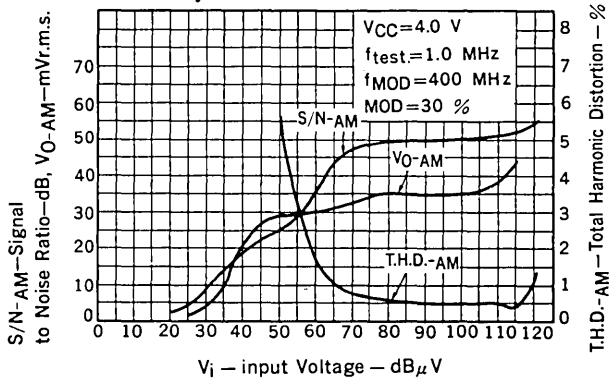
FM STAGE

OUTPUT VOLTAGE, TOTAL HARMONIC DISTORTION, AM Rejection, AND NOISE VOLTAGE vs. INPUT VOLTAGE

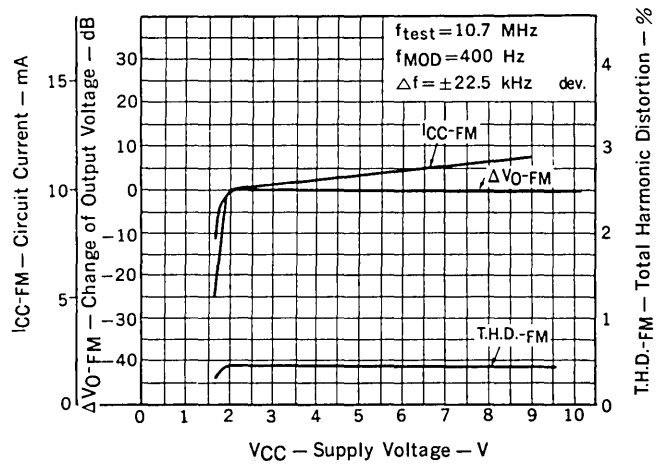


AM STAGE

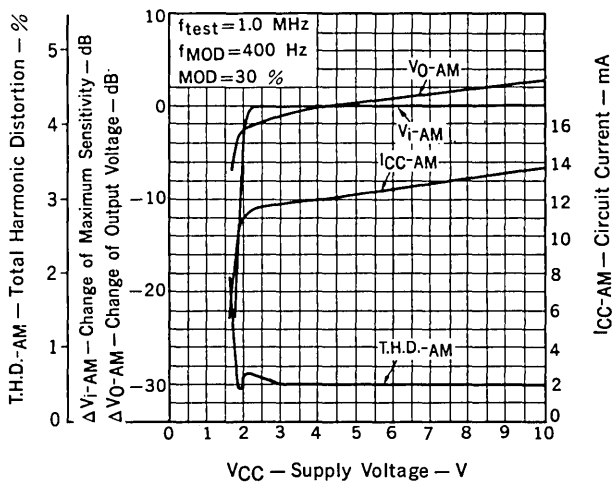
OUTPUT VOLTAGE, TOTAL HARMONIC DISTORTION, SIGNAL TO NOISE RATIO, vs. INPUT VOLTAGE



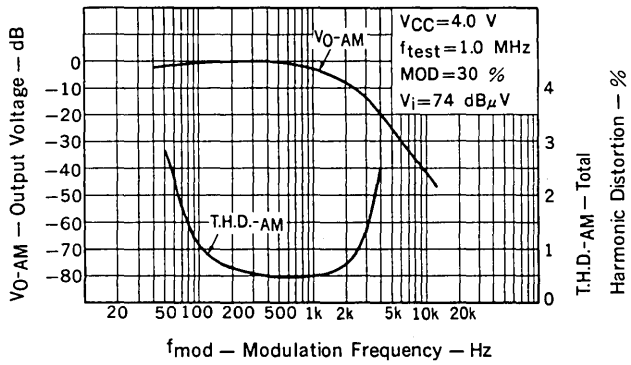
CIRCUIT CURRENT, CHANGE OF OUTPUT VOLTAGE TOTAL HARMONIC DISTORTION vs. SUPPLY VOLTAGE



CHANGE OF OUTPUT VOLTAGE, CHANGE OF MAXIMUM SENSITIVITY vs. SUPPLY VOLTAGE



DETECTOR OUTPUT VOLTAGE, TOTAL HARMONIC DISTORTION vs. MODULATION FREQUENCY



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1197C

FM MULTIPLEX STEREO DEMODULATOR
SILICON MONOLITHIC BIPOLAR INTEGRATED CIRCUIT

DESCRIPTION

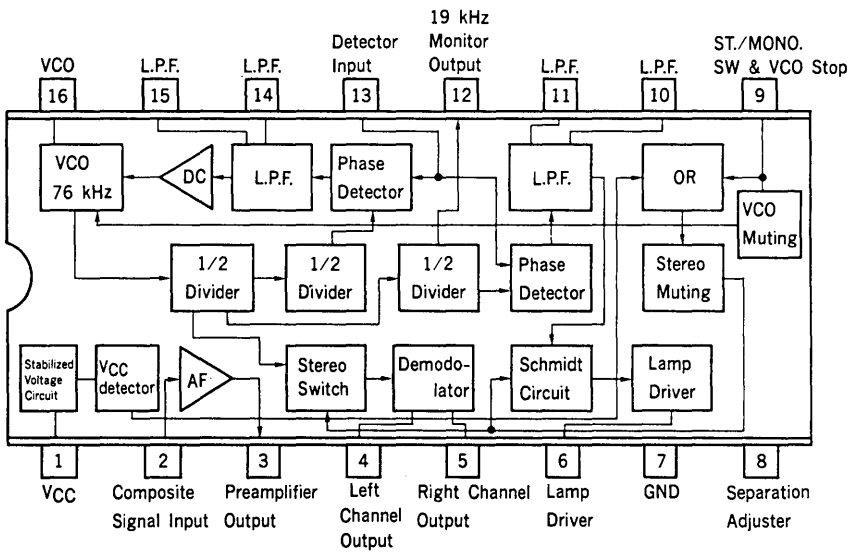
The μPC1197C is a silicon monolithic integrated circuit for FM multiplex demodulator designed for stereo cassette tape recorder with radio receiver, car stereo and car radio operated at a low supply voltage.

The circuit consists of a voltage control oscillator (VCO) for a demodulator and a phase locked loop (PLL), phase comparators, low pass filters (LPF), frequency dividers and a DC amplifier. It also contains accessory circuits such as separation adjustor stereo-monaural switcher, VCO stopper and stereo-monaural switcher in depressed supply voltage.

FEATURES

- No coil is needed due to PLL (Phase Locked Loop) system. The absence of coil, essential component in conventional systems, enable to reduce the number of external components and save manpower for adjustments.
- The circuit provides stability in a wide range of power supply voltage. (V_{CC} = 4 to 16 V)
- A stereo/monaural switch can be controlled by a DC voltage obtained from IF signal by smoothing. It is also designed to provide very small shock noise generated when the stereo/monaural is switched.
- VCO, an unnecessary function for AM reception, can be stopped simply by connecting the control terminal to the power supply. (V_{CC} – 3.0 V)
- When the power supply voltage is depressed the mode is forced to shift to monaural. (Forced monaural reception; V_{CC} – 3.5 V)
- Separation adjustment terminal enables to adjust optimum channel separation.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Power Supply Voltage	V_{CC}	16	V
Allowable Power Dissipation	P_D	350*	mW
Operational Temperature	T_{opt}	−20 to + 75	°C
Storage Temperature	T_{stg}	−40 to + 125	°C

*Ta = 75 °C

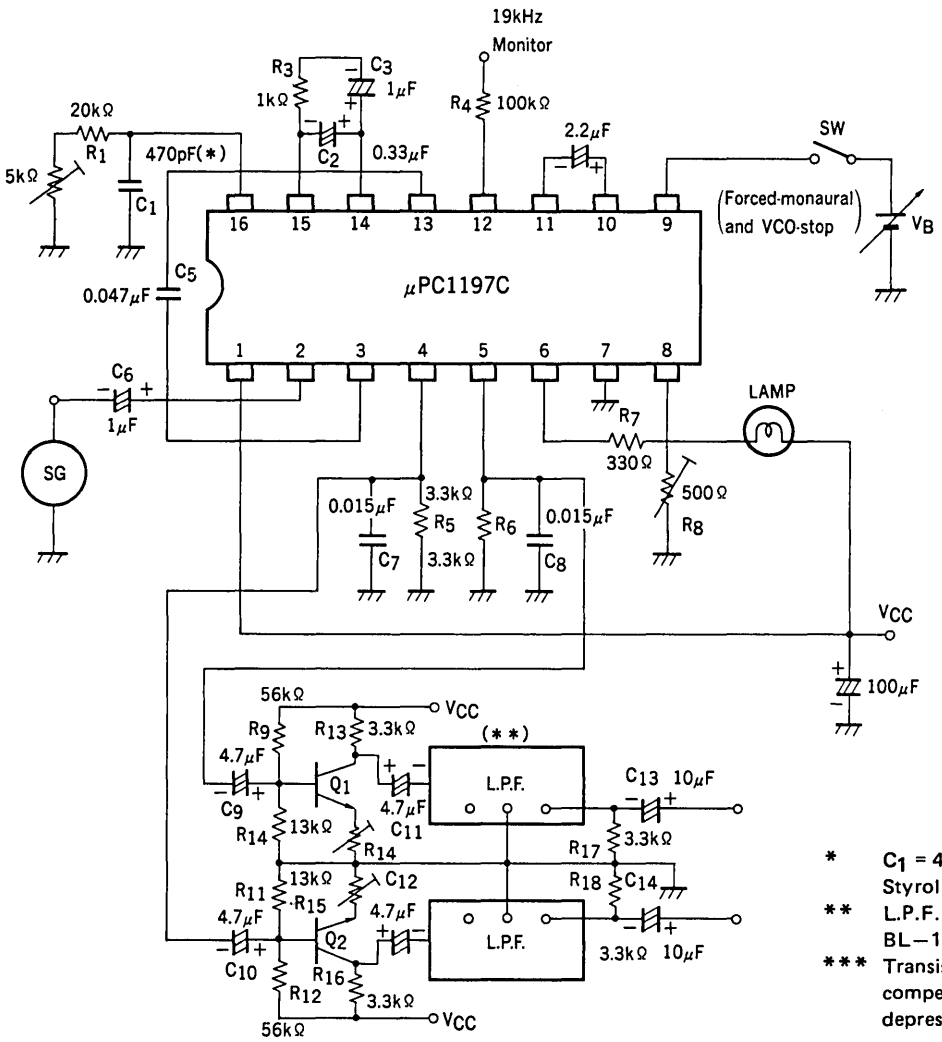
RECOMMENDED OPERATION CONDITIONS (Ta = 25 °C)

Supply Voltage Range	V_{CC}	4 to 16 V
Operating Voltage	V_{CC}	9 V

ELECTRICAL CHARACTERISTICS (Ta = 25 °C, V_{CC} = 9 V, v_i = 200 mV, L = 45 %, R = 45 %, Pilot = 10 %)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Circuit Current	I_{CC}		12		mA	Without signal
Separation	Sep.	30	45		dB	f = 100 Hz
		40	55		dB	f = 1 kHz
		30	45		dB	f = 10 kHz
Monaural Total Harmonic Distortion	T.H.D.		0.3	0.5	%	monaural V_{in} = 200 mV
Stereo Total Harmonic Distortion	T.H.D.		0.2	0.5	%	stereo pilot = 20 mV
Output Voltage	V_O		170		mV	V_i = 200 mV
Channel Balance	Ch. B.	−2	0	2	dB	monaural V_i = 200 mV
Lamp-on Level	LAMP-ON		8		mV	pilot signal
Lamp Hysteresis	Hys. (LAMP)		4		dB	pilot signal
Capture Range	C.R.		±4		%	pilot = 20 mV
Ultrasonic Frequency Rejection	Rej (19)		35		dB	pilot = 20 mV
	Rej (38)		45		dB	pilot = 20 mV
SCA Rejection ratio	Rej (SCA)		70		dB	$\frac{\text{pilot}}{\text{composite}} = \frac{1}{10}$, $\frac{\text{SCA}}{\text{composite}} = \frac{1}{10}$,
Signal to Noise Ratio	S/N		86		dB	V_i = 200 mV
Allowed Maximum Input Level	Vi (MAX)		500		mV	T.H.D. ≦ 2%
Forced-monaural Level	V (MONO)		0.7		V	#9 terminal
VCO-stop level	V (STOP)		3.0		V	#9 terminal
Stereo-monaural Switch-over Voltage	V_{CC} (MONO)		3.5		V	Supply Voltage

TEST CIRCUIT



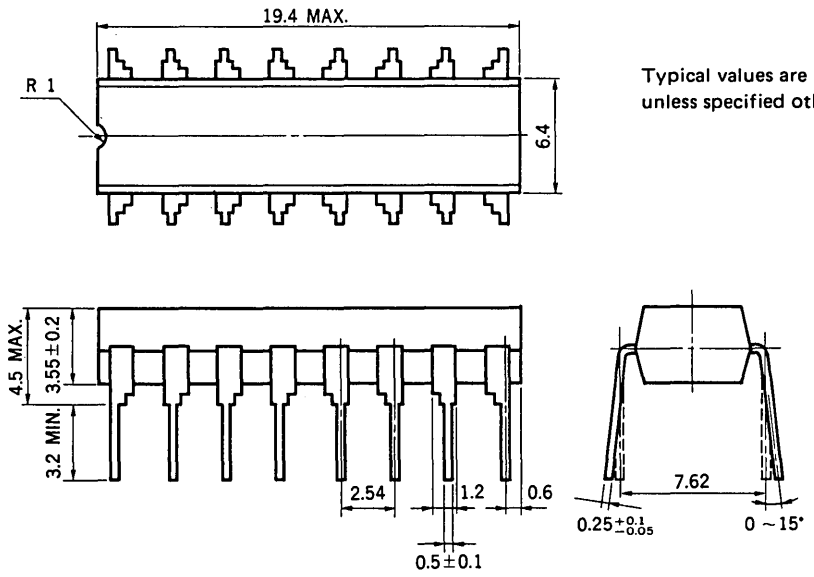
* C_1 = 470 pF
Styrol Capacitor

** L.P.F.
BL–13 (K.K. KORIN)

*** Transistors Q_1 and Q_2 compensate the gain depression through LPF's

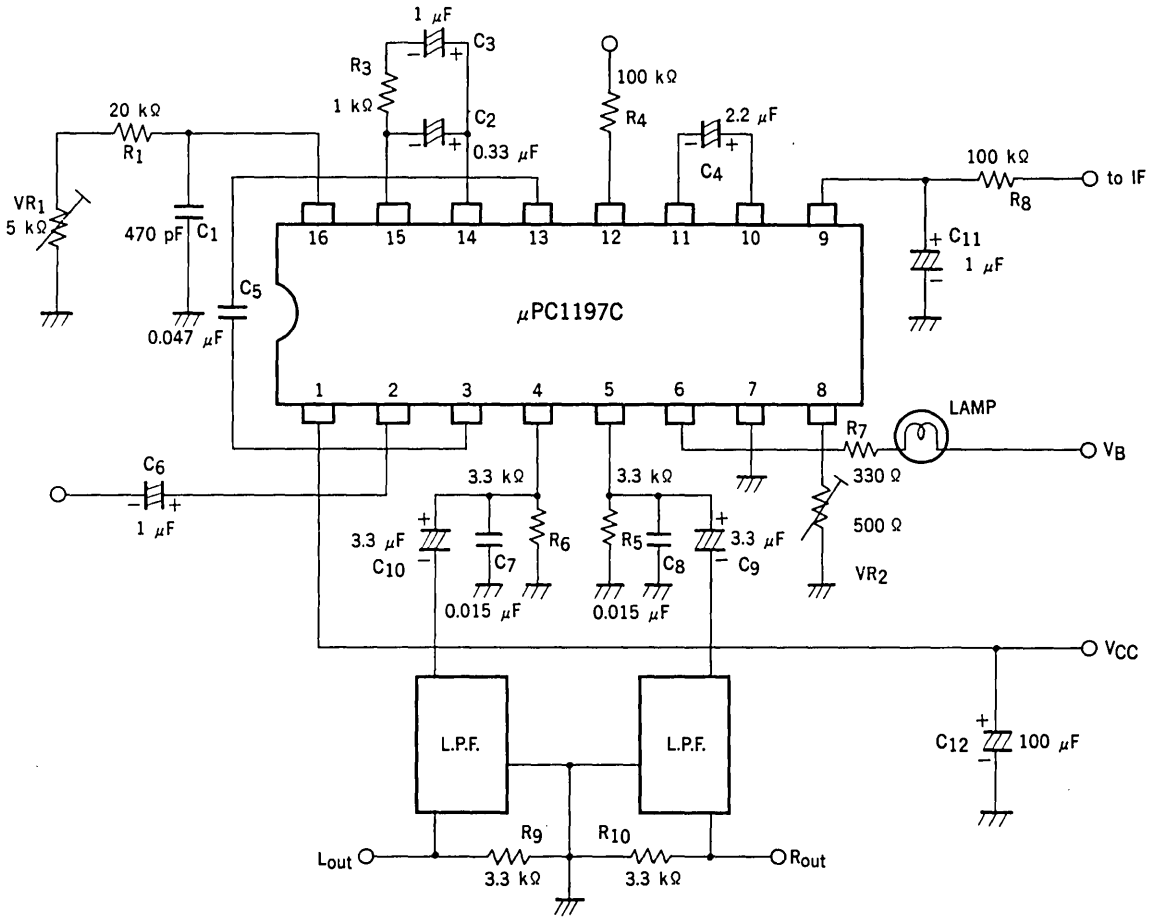
PACKAGE DIMENSIONS

in millimeters (inches)



Typical values are shown unless specified otherwise.

TYPICAL APPLICATION CIRCUIT



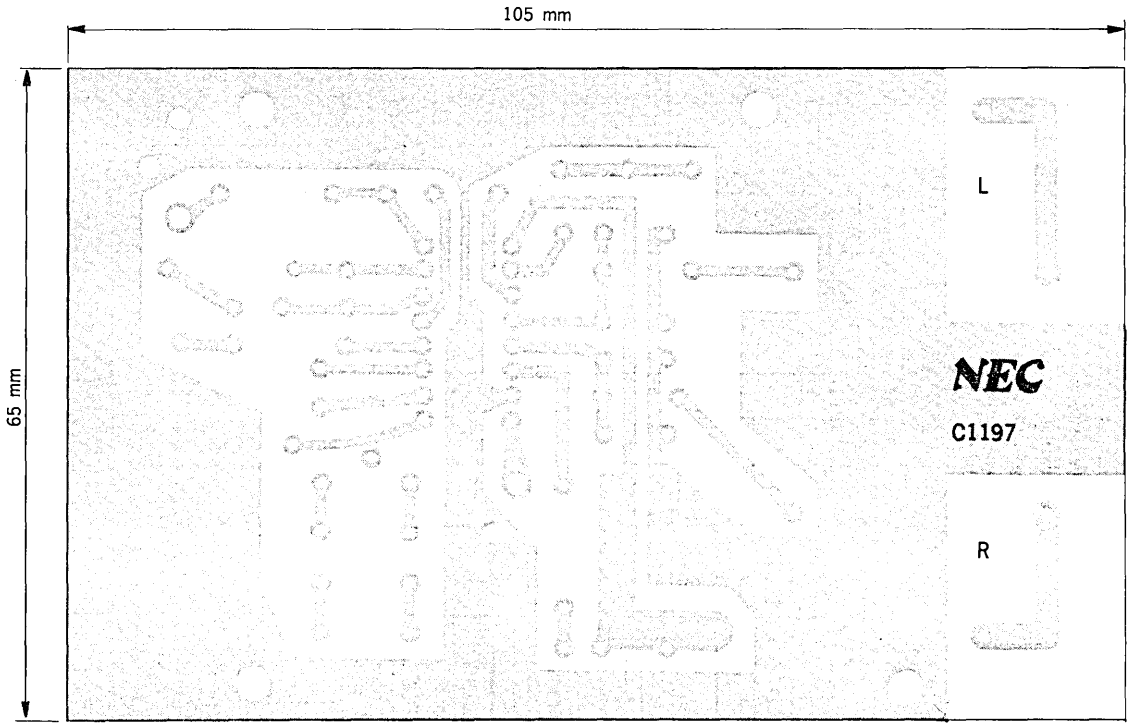
PRECAUTIONS NEEDED IN APPLICATIONS

(1) The μPC1197C is designed to have a temperature coefficient which is equivalent to that of styrol capacitors.

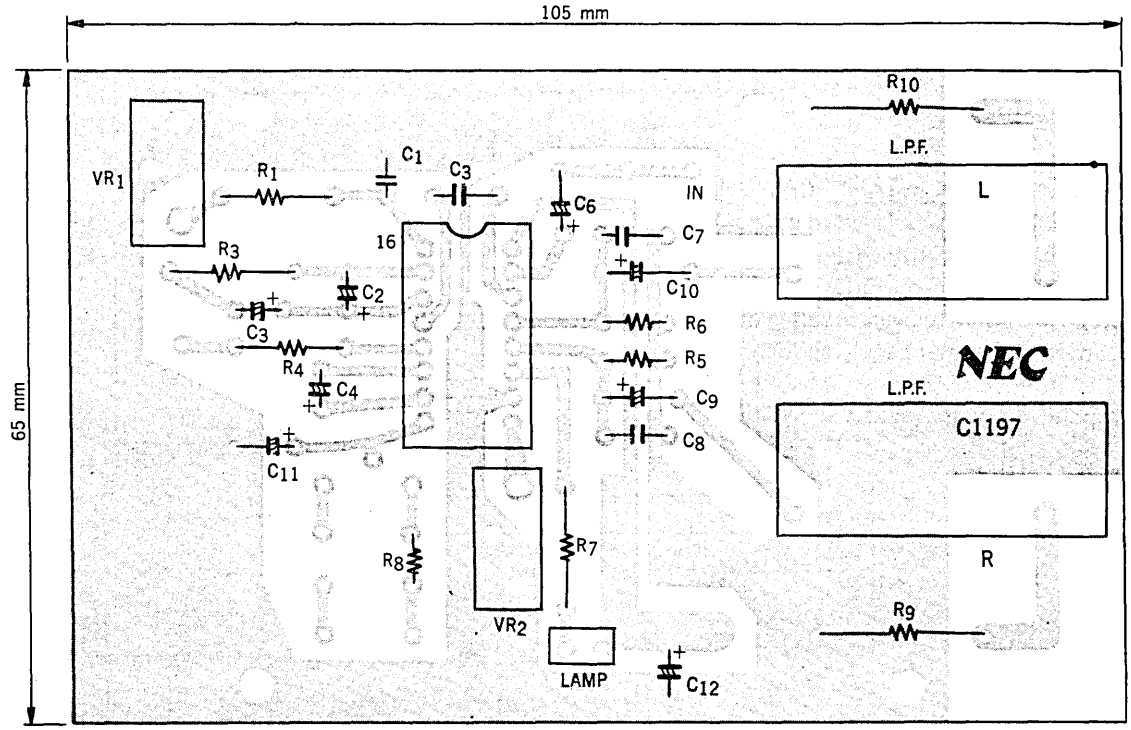
(2) Terminal #9 is provided for forced-monaural switching and VCO stop. If a voltage of 0.7 volt or more is applied to the terminal, the operation is switched over to monaural and if a voltage of 3 volts or more is applied, VCO is stopped. For a power supply voltage higher than 10 volts, insert a resistance satisfying the following formula between the power supply and terminal #9.

1.1 $[V_{CC}(MAX)-10] = R = 2[V_{CC}(MIN)-4]$ (kΩ), where $V_{CC}(MAX)$ and V_{CC} (MIN) and lower limits of power supply voltage that satisfy the voltage regulation sequirement, respectively.

TYPICAL CIRCUIT BOARD ARRANGEMENT (VIEW OF PRINTED WIRING)

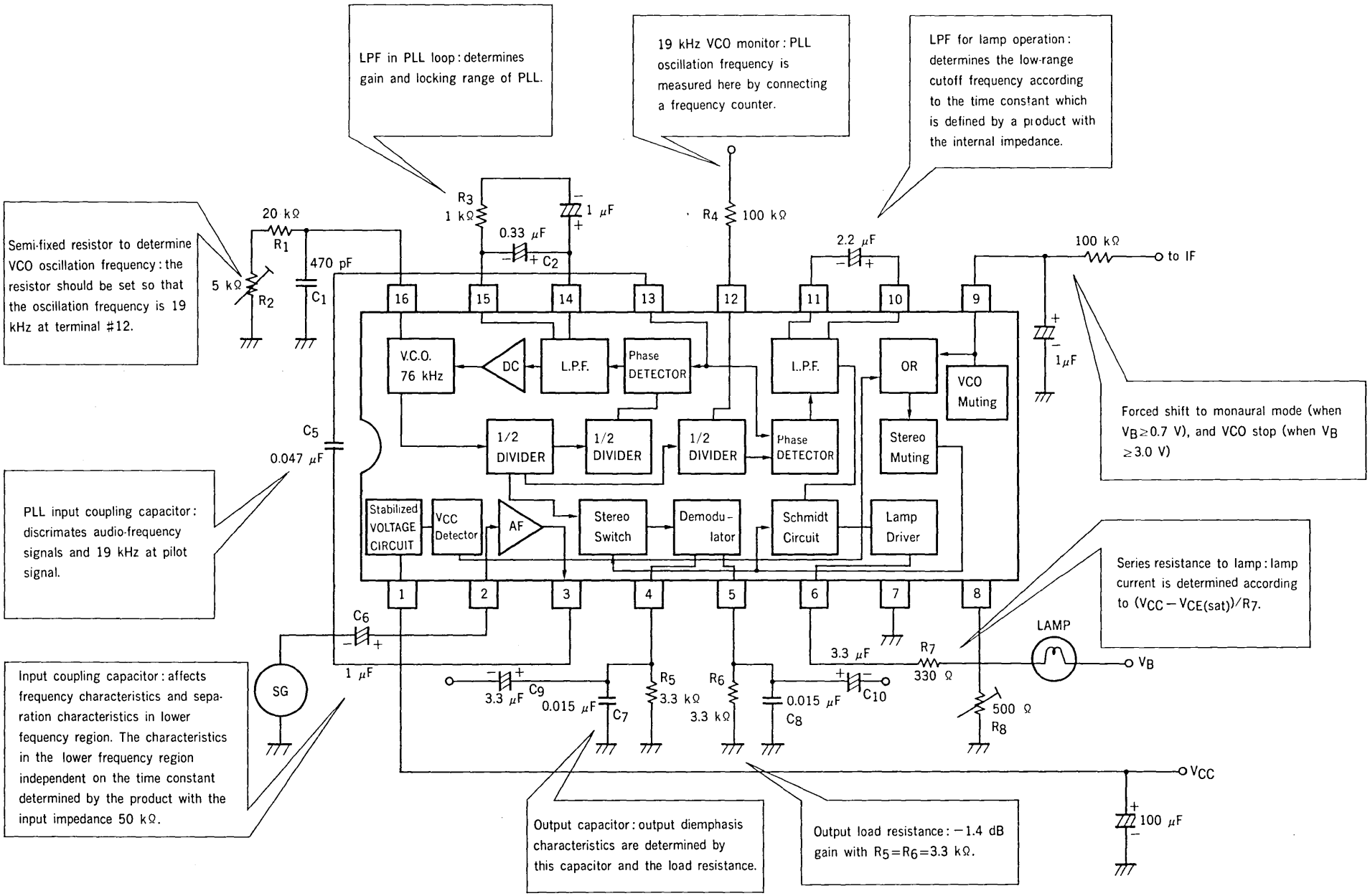


TYPICAL PARTS LOADING (TYPICAL APPLICATION)



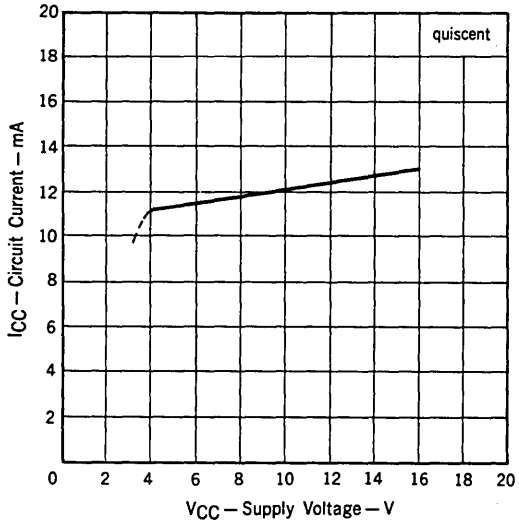
R_1 = 18 kΩ	R_7 = 330 Ω	C_1 = 470 pF (Styrol Capacitor)	C_7 = 0.015 μF
VR_1 = 5 kΩ	R_8 = 100 kΩ	C_2 = 0.33 μF	C_8 = 0.015 μF
R_3 = 1 kΩ	R_9 = 3.3 kΩ	C_3 = 1 μF	C_9 = 3.3 μF
R_4 = 100 kΩ	R_{10} = 3.3 kΩ	C_4 = 2.2 μF	C_{10} = 3.3 μF
R_5 = 3.3 kΩ		C_5 = 0.047 μF	C_{11} = 1 μF
R_6 = 3.3 kΩ		C_6 = 1 μF	C_{12} = 100 μF

DESCRIPTION OF EXTERNALLY LOADED COMPONENT PARTS

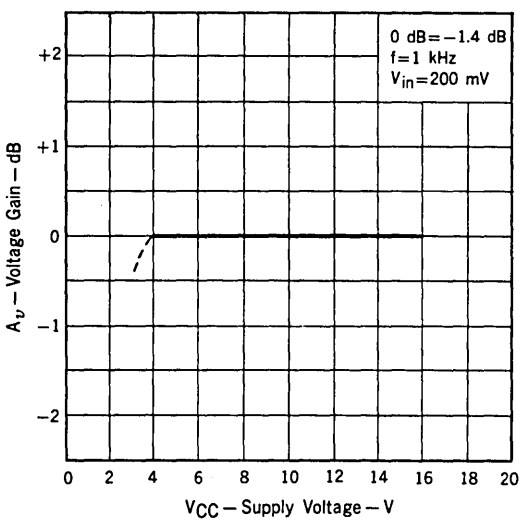


TYPICAL CHARACTERISTICS

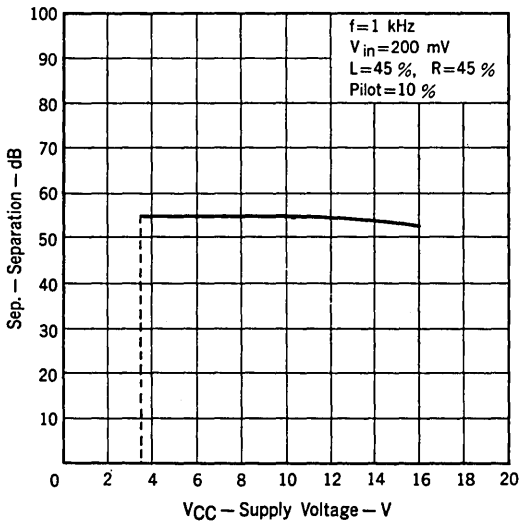
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



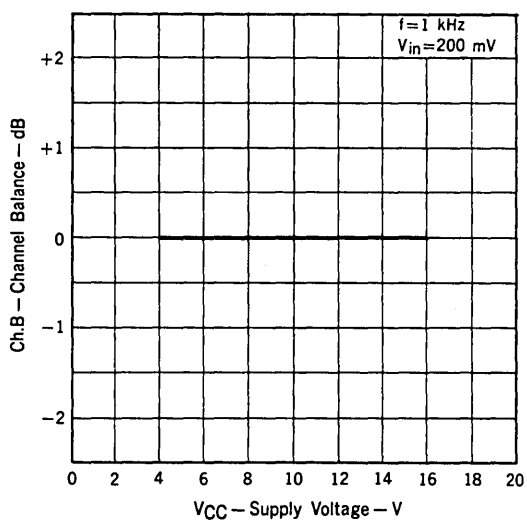
VOLTAGE GAIN vs. SUPPLY VOLTAGE (Monaural)



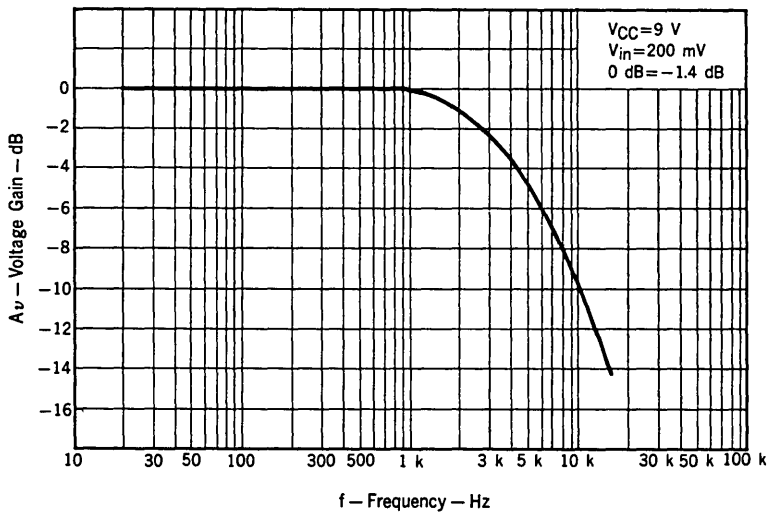
SEPARATION vs. SUPPLY VOLTAGE (Stereo)



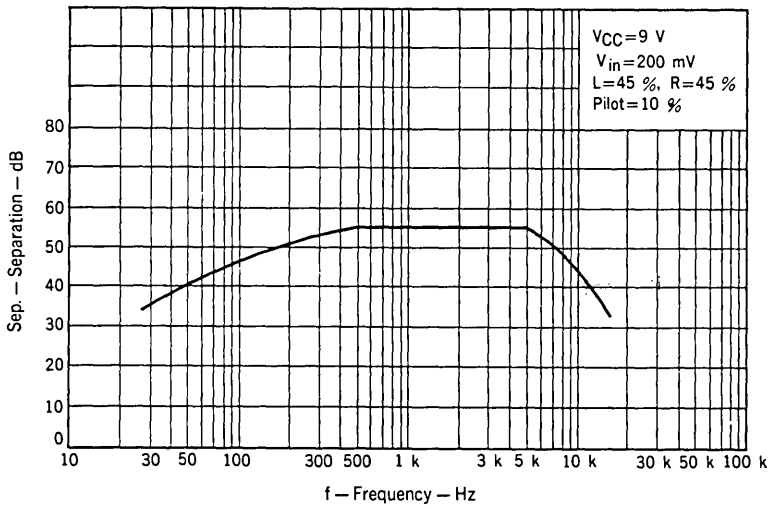
CHANNEL BALANCE vs. SUPPLY VOLTAGE (Monaural)



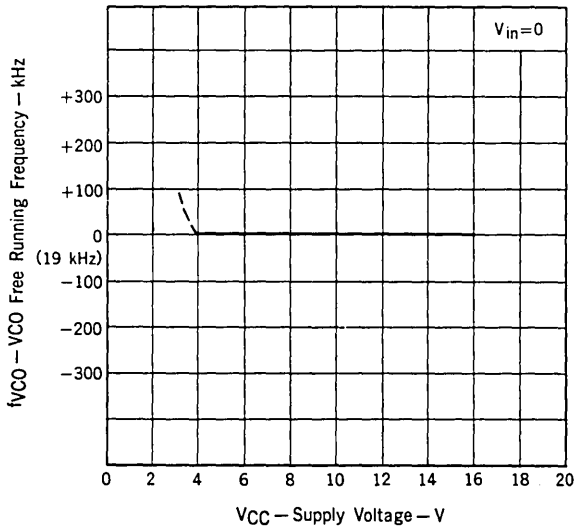
VOLTAGE GAIN vs. FREQUENCY (Monaural)



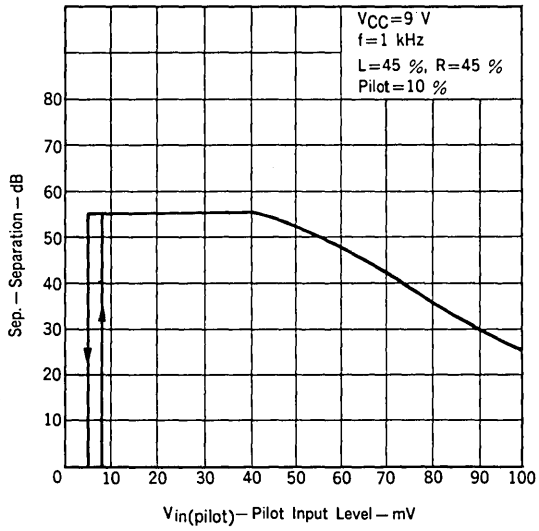
SEPARATION vs. FREQUENCY
(Stereo)



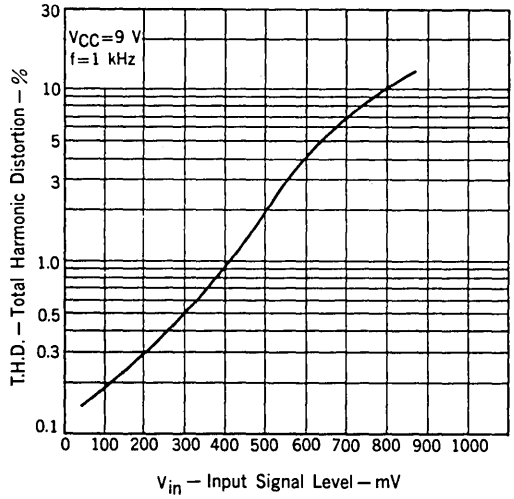
VCO FREE RUNNING FREQUENCY vs.
SUPPLY VOLTAGE



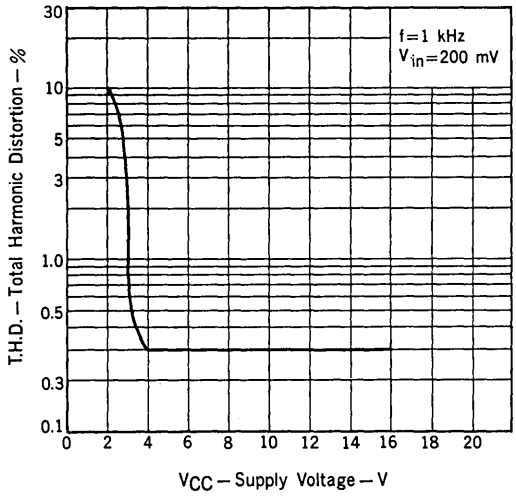
SEPARATION vs. PILOT INPUT LEVEL
(Stereo)



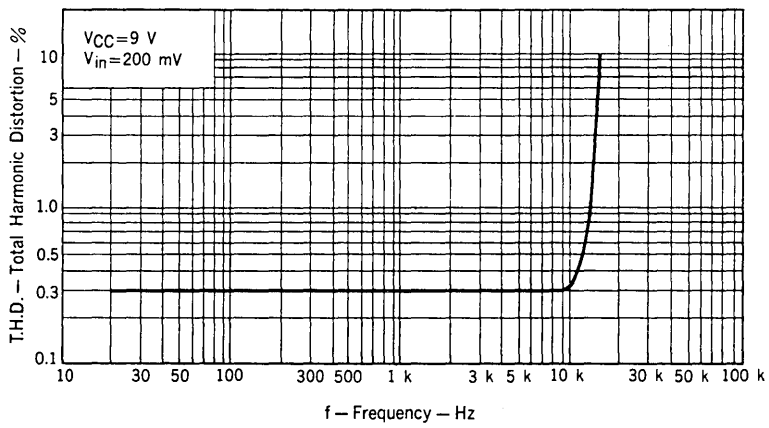
TOTAL HARMONIC DISTORTION vs.
SIGNAL INPUT LEVEL (Monaural)



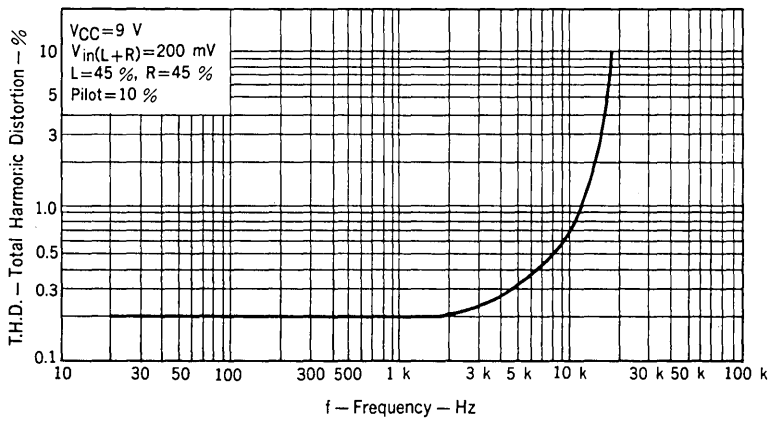
TOTAL HARMONIC DISTORTION vs.
SUPPLY VOLTAGE (Monaural)



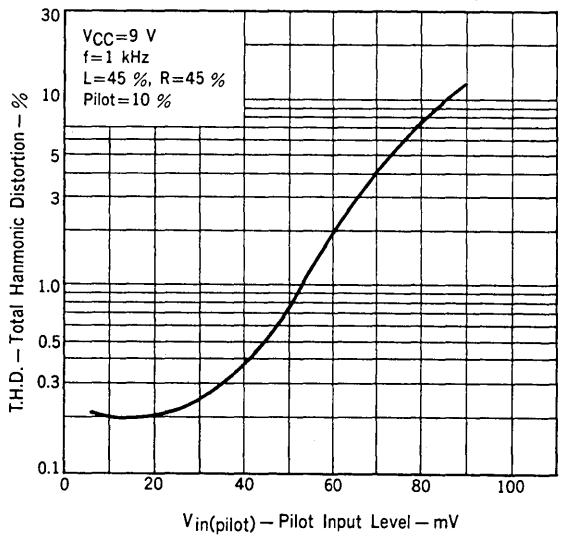
TOTAL HARMONIC DISTORTION vs. FREQUENCY (Monaural)



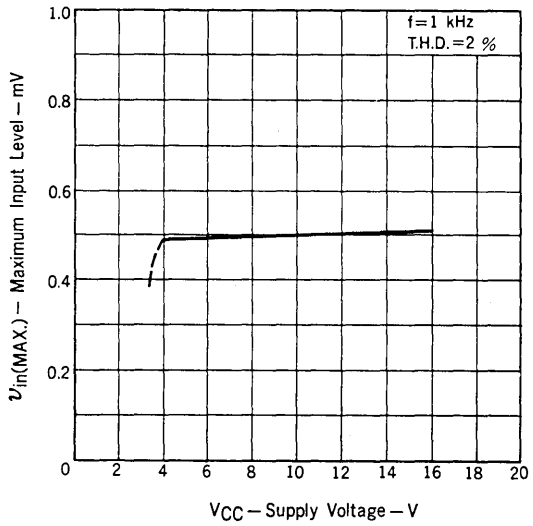
TOTAL HARMONIC DISTORTION vs. FREQUENCY (Stereo)



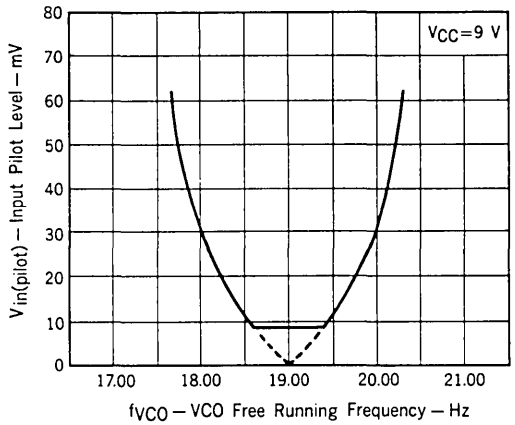
TOTAL HARMONIC DISTORTION vs. PILOT INPUT LEVEL (Stereo)



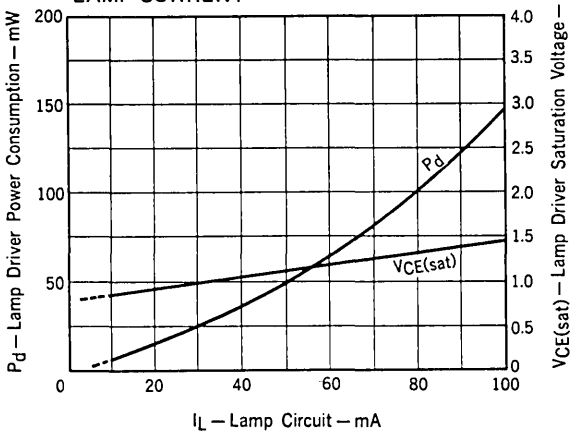
MAXIMUM INPUT LEVEL vs. SUPPLY VOLTAGE (Monaural)



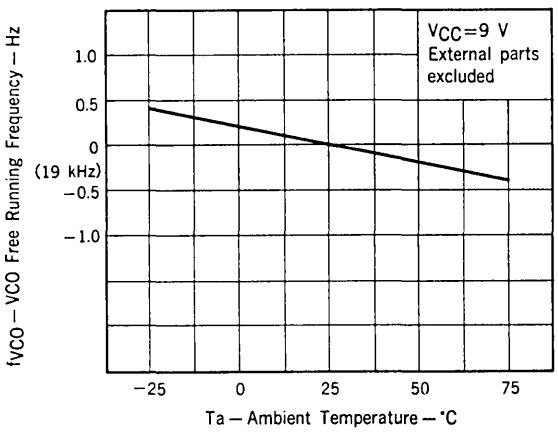
CAPTURE RANGE



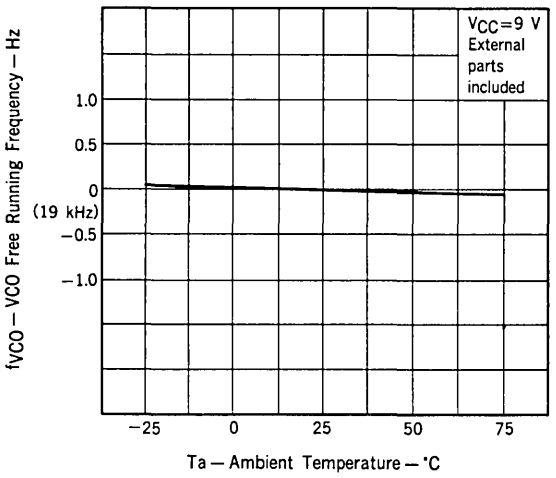
POWER DISSIPATION AND SATURATION VOLTAGE OF LAMP DRIVER vs. LAMP CURRENT



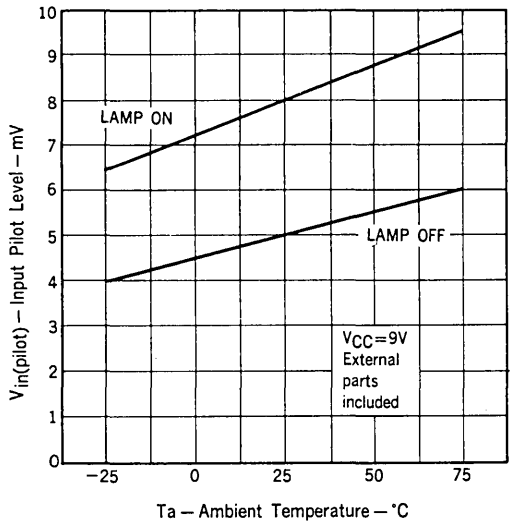
VCO FREE RUNNING FREQUENCY vs. AMBIENT TEMPERATURE



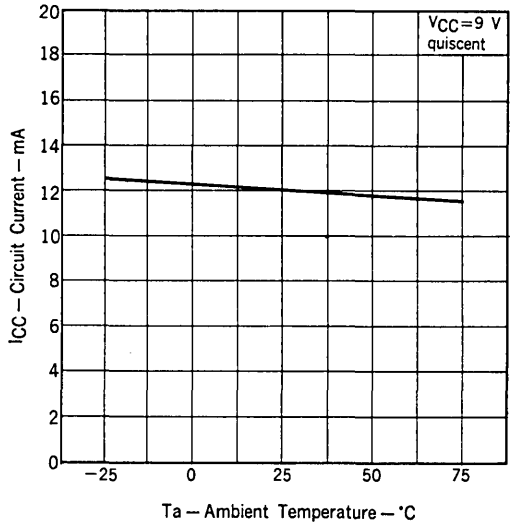
VCO FREE RUNNING FREQUENCY vs. AMBIENT TEMPERATURE



INPUT PILOT LEVEL (LAMP ON–OFF) vs. AMBIENT TEMPERATURE



CIRCUIT CURRENT vs. AMBIENT TEMPERATURE



BIPOLAR ANALOG INTEGRATED CIRCUIT
μPC1158H2

LOW NOISE PREAMPLIFIER WITH AUTOMATIC LEVEL CONTROL
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

DESCRIPTION

The μPC1158H2 is a silicon monolithic integrated circuit designed for high gain, low noise preamplifier with Automatic Level Control (ALC).

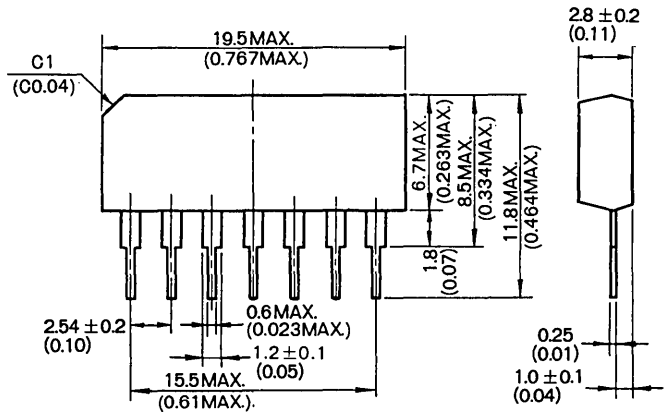
As an advanced production process is used, the device has an excellent feature of very low pulsive noise characteristics.

It is ideally suitable for use as a recording and playing amplifier in a cassette tape recorder.

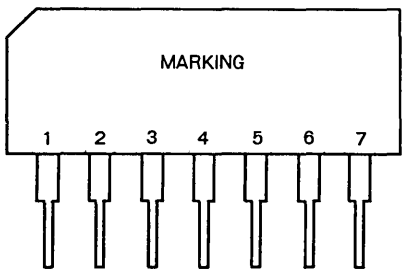
FEATURES

- Low noise, especially low pulsive noise.
- Wide supply voltage range (V_{CC} = 2.2 ~ 15 V).
- High gain: A_{vo} = 70 dB TYP.
- High output voltage: V_{OM} = 1.0 Vr.m.s. TYP.
- Low distortion.
- Wide ALC range.
- SIP assures easy mounting on printed circuit board.
- Fast build up power switch on.

PACKAGE DIMENSIONS
in millimeters (inches)

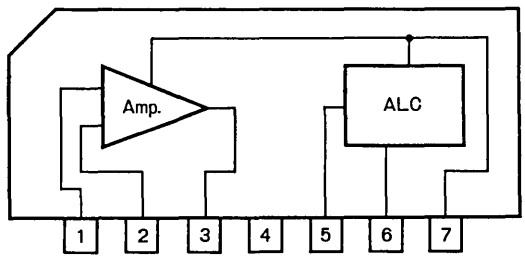


CONNECTION DIAGRAM

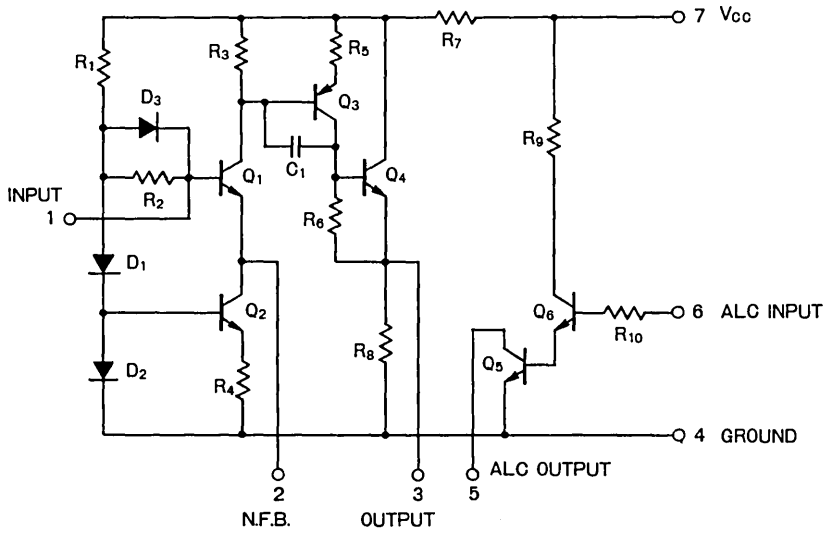


Pin No.	Electrical Connection
1	INPUT
2	N.F.B.
3	OUTPUT
4	GROUND
5	ALC OUTPUT
6	ALC INPUT
7	V_{CC}

BLOCK DIAGRAM



EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Supply Voltage	V_{CC}	15.0	V
Package Dissipation (Ta=75°C)	P_D	270	mW
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

RECOMMENDED CONDITIONS (Ta=25°C)

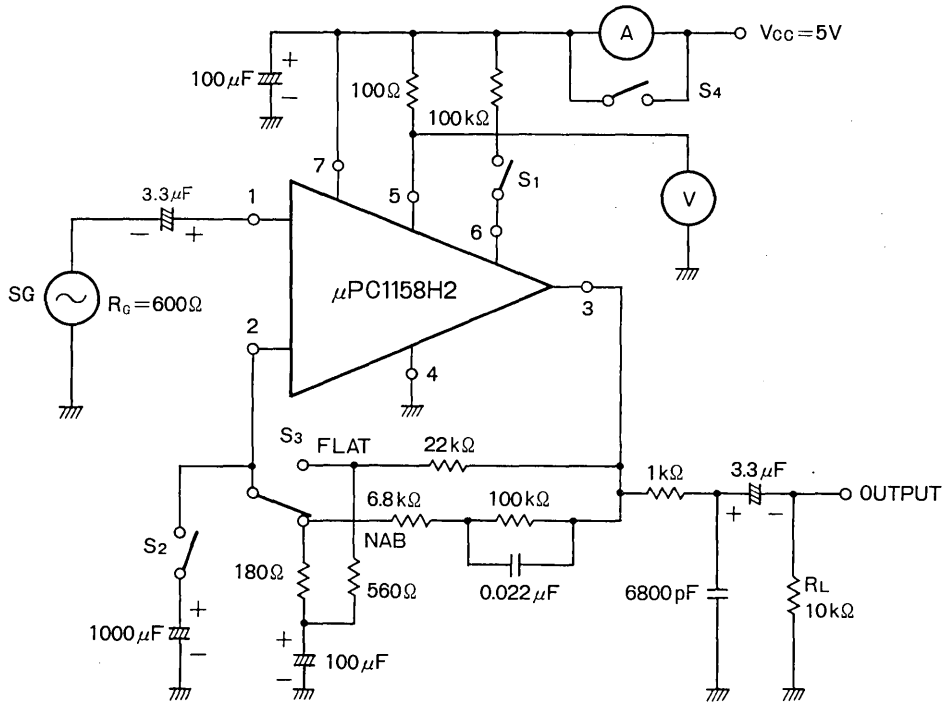
Operating Supply Voltage	5.0	V
Supply Voltage Range	2.2 to 15.0	V

ELECTRICAL CHARACTERISTICS (Ta=25°C, Vcc=5V, f=1kHz, RL=10kΩ)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	I_{CC}	0.9	1.5	2.2	mA	v_{in}=0
Open Loop Voltage Gain	A_{vo}	64	70		dB	v_{in}=−80dBm
Voltage Gain	A_v		33.5		dB	v_{in}=−50dBm
Maximum Output Voltage	V_{OM}	0.7	1.0		V	T.H.D.=1%
Input Impedance	r_i		100		kΩ	f=1kHz
Equivalent Input Noise Voltage	v_{nin}		1.2	2.0	μVr.m.s.	R_G=2.2kΩ, NAB Equalized 15~30kHz BPF+40dB Amp.
Collector Voltage of ALC Transistor	V_5		0.7		V	Pin 7 to Pin 6: 100kΩ Pin 7 to Pin 5: 100Ω

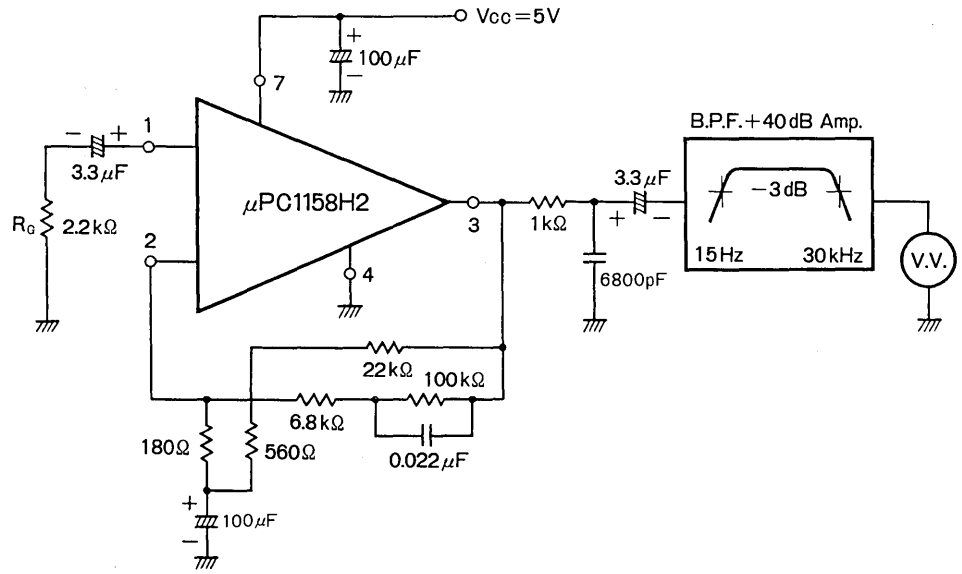
TEST CIRCUITS

Test Circuit for General Characteristics Given in the Table Below.



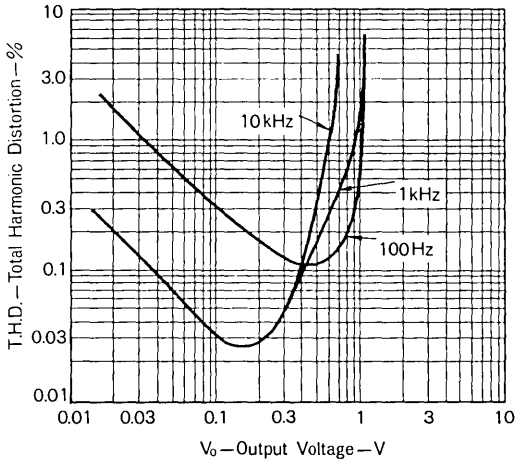
CHARACTERISTIC	SYMBOL	S_1	S_2	S_3	S_4	TEST POINT
Circuit Current	I_{CC}	OFF	OFF	NAB	OFF	Pin 7
Open Loop Voltage Gain	A_{vo}	OFF	ON	FLAT	ON	Pin 3
Voltage Gain	A_v	OFF	OFF	NAB	ON	Pin 3
Maximum Output Voltage	V_{OM}	OFF	OFF	NAB	ON	Pin 3
Collector Voltage of ALC Transistor	V_5	ON	OFF	NAB	ON	Pin 5

Test Circuit for Noise Voltage.

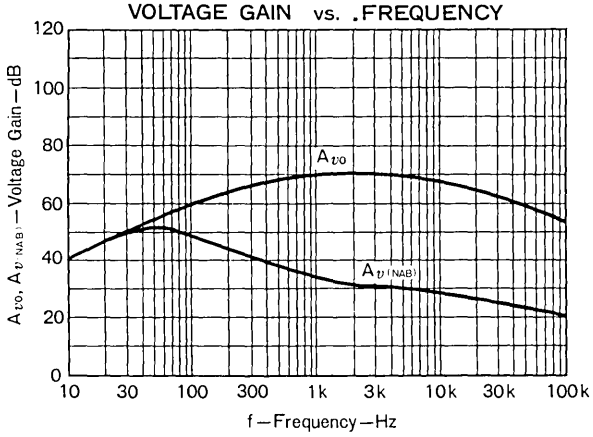


TYPICAL CHARACTERISTICS (Ta=25°C)

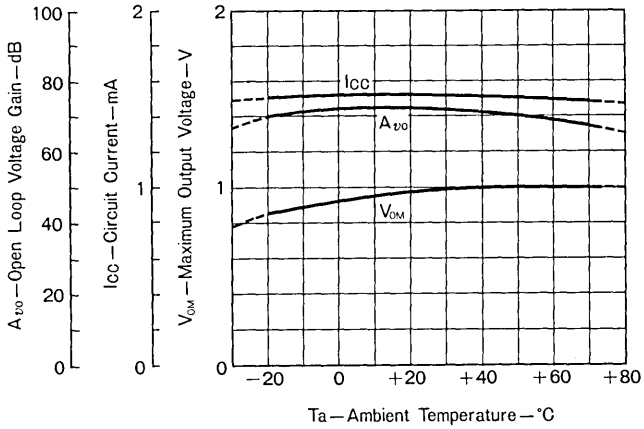
TOTAL HARMONIC DISTORTION vs. OUTPUT VOLTAGE



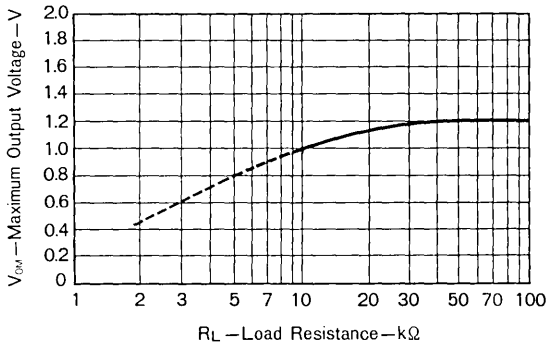
VOLTAGE GAIN vs. FREQUENCY



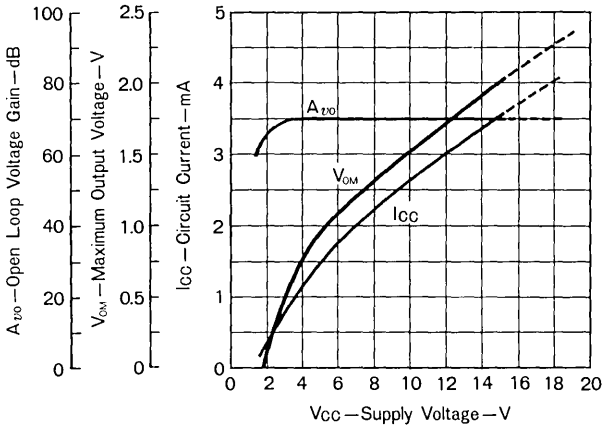
CIRCUIT CURRENT, MAXIMUM OUTPUT VOLTAGE, OPEN LOOP VOLTAGE GAIN vs. AMBIENT TEMPERATURE



MAXIMUM OUTPUT VOLTAGE vs. LOAD RESISTANCE

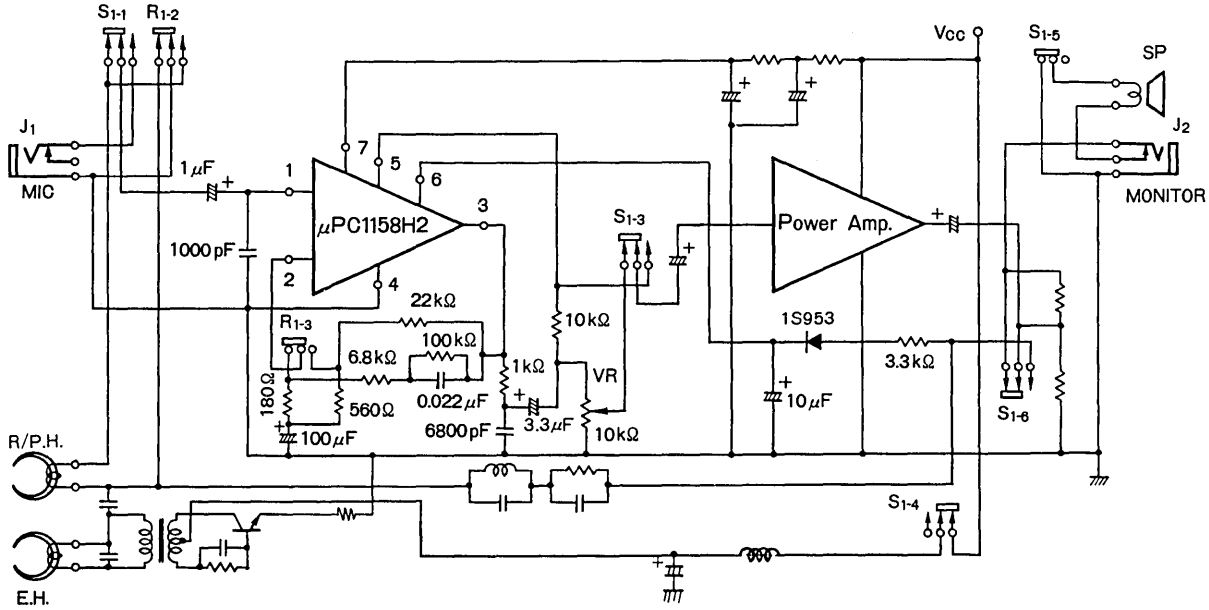


CIRCUIT CURRENT, MAXIMUM OUTPUT VOLTAGE, OPEN LOOP VOLTAGE GAIN vs. SUPPLY VOLTAGE



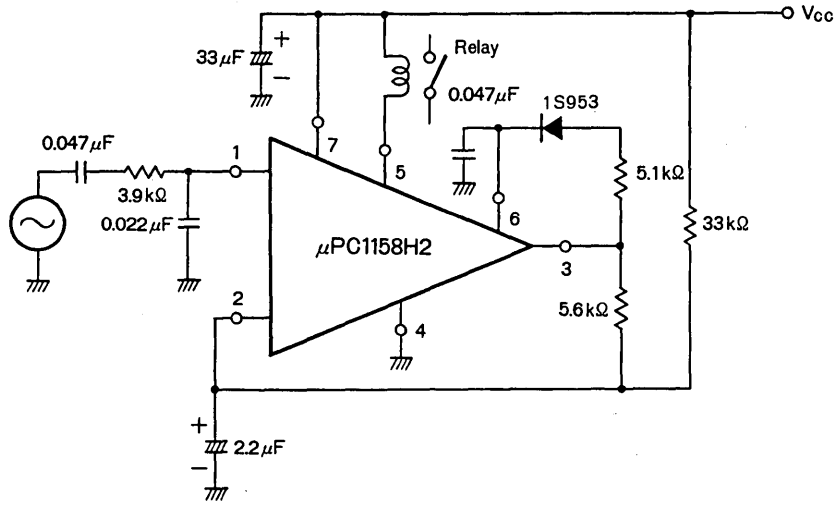
TYPICAL APPLICATIONS

Pre Amplifier for Cassette Tape Recorder.



* Rec./Play Switch S_{1-1} ~ S_{1-7} are shown in play mode.
* Actual D.C. resistance of feed back element between pin 2 and pin 3 is advisable about 18kΩ or more.

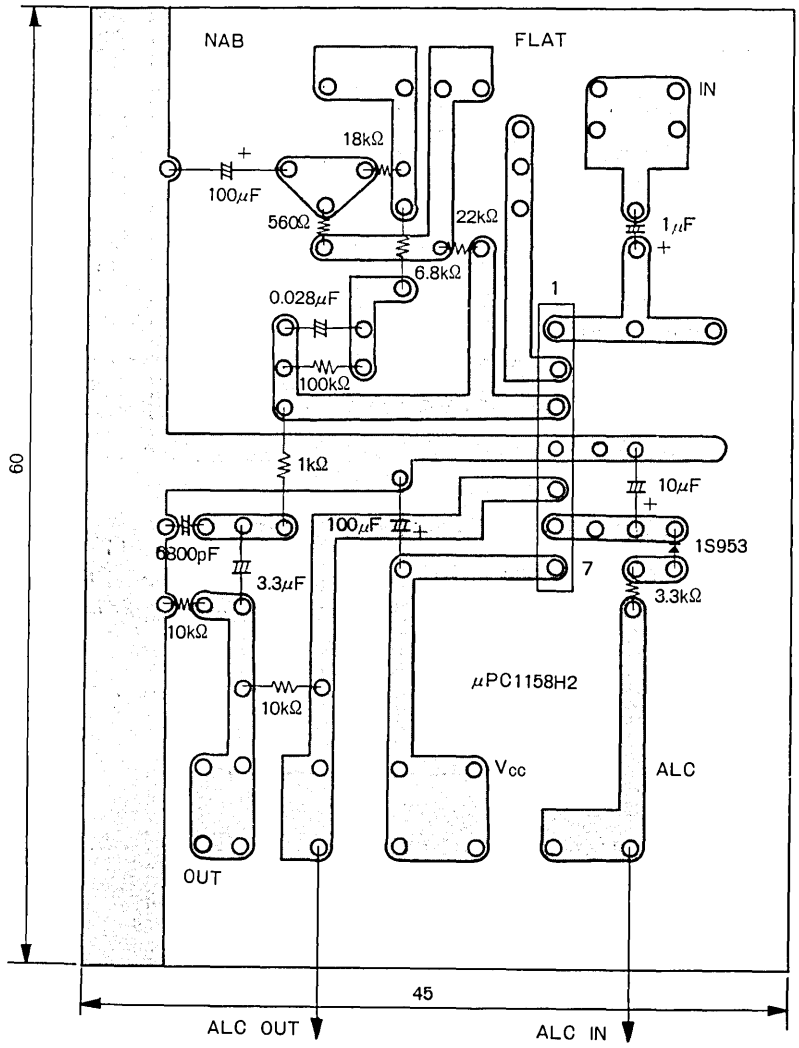
Relay Driver for Radio Control Equipment.



TYPICAL PRINTED CIRCUIT BOARD PATTERN

(1) Pre-Amplifier for Cassette Tape Recorder.

PRINTED CIRCUIT LAYOUT & COMPONENT LAYOUT (BOTTOM VIEW)



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1204C

RECORDING AND PLAY'BACK AMPLIFIER

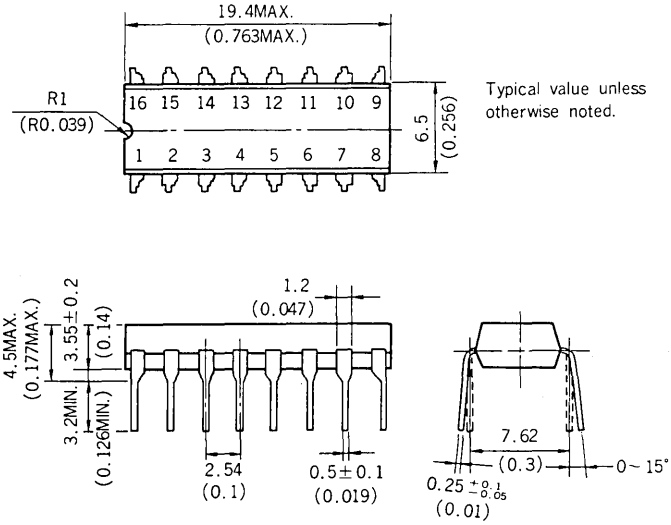
DESCRIPTION

The μPC1204C is a silicon monolithic integrated circuit designed for cassette tape recorders. The μPC1204C contains a pre amplifier, an ALC circuit, a recording amplifier and a meter amplifier. The μPC1204C is encapsulated in an 16 pins dual in-line plastic package.

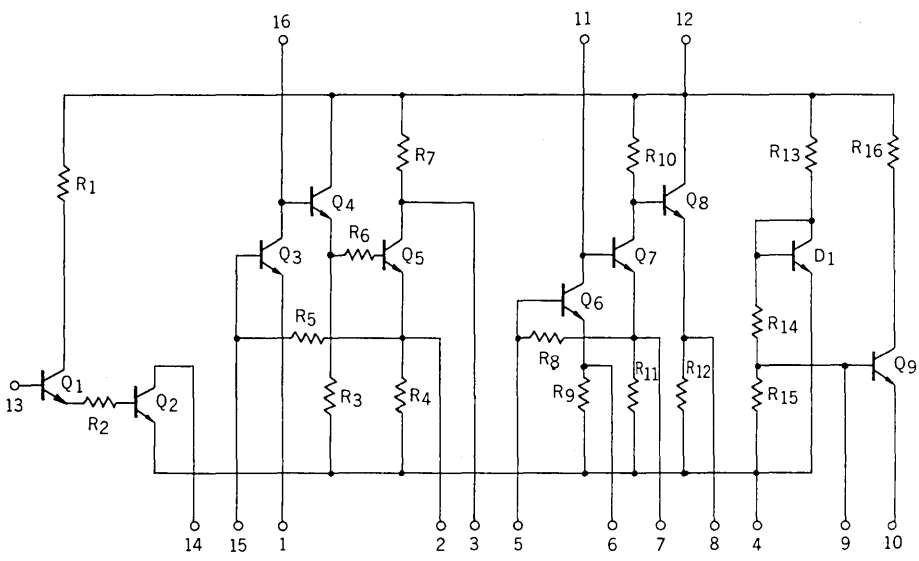
FEATURES

- Wide operating range. Vcc = 8 – 12 – 20V
- Low noise, especially low pulsive noise.
- The pre amplifier and the recording amplifier have high gain and low distortion characteristics.
- Wide ALC range.
- Integrated functions necessary to cassette sound reproducing.
  (a pre amplifier, a recording amplifier, an ALC circuit and a meter amplifier)

PACKAGE DIMENSIONS in millimeters (inches)



EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Supply Voltage	V_{CC}	20	V
Package Dissipation	P_d	350 (Ta = 75°C)	mV
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

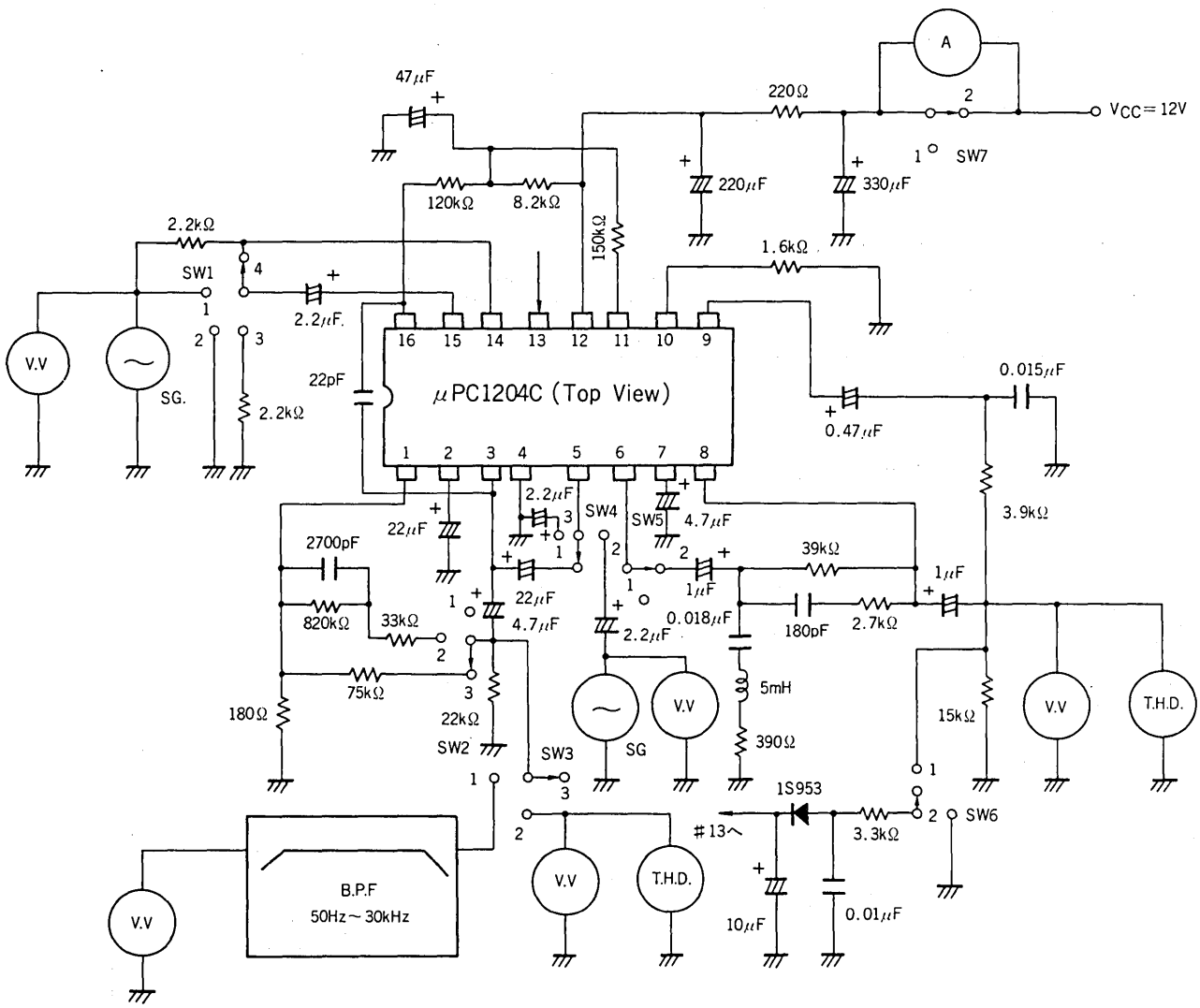
RECOMMENDED OPERATING CONDITION (Ta=25°C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	8	12	20	V

ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=12V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	I_{CC}	2.4	4.0	6.0	mA	No Signal
(PRE AMPLIFIER) 52dB f=1 kHz						
Voltage Gain	A_{vo1}	78	85		dB	V_o= 0.3 Vr.m.s.
Maximum Output Voltage	V_{om1}	1.6	2.5		Vr.m.s.	T.H.D.=1%
Total Harmonic Distortion	T.H.D.		0.3	0.6	%	V_o= 0.3 Vr.m.s.
Equivalent Input Noise Voltage	V_{nin}		1.3	2.0	μVr.m.s.	30 kHz B.P.S., R_G=2.2 kΩ
(RECORDING AMPLIFIER) f=1 kHz						
Voltage Gain	A_{vo2}	47	54		dB	V_o= 0.3 Vr.m.s.
Maximum Output Voltage	V_{om2}	1.9	2.7		Vr.m.s.	T.H.D.=1%
Total Harmonic Distortion	T.H.D.		0.03	0.1	%	V_o= 0.3 Vr.m.s.
(ALC)						
ALC Range	ALC		56		dB	T.H.D.= 3%

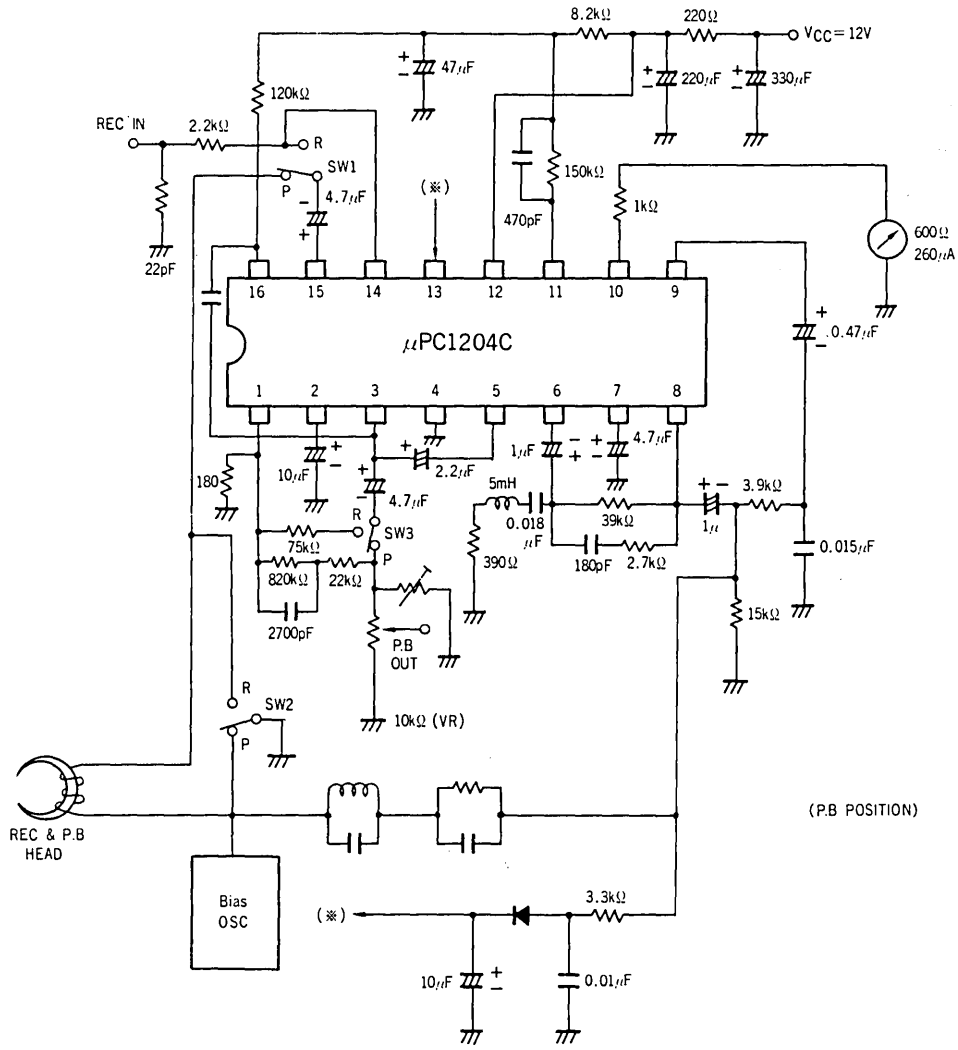
TEST CIRCUIT



SWITCH POSITIONS

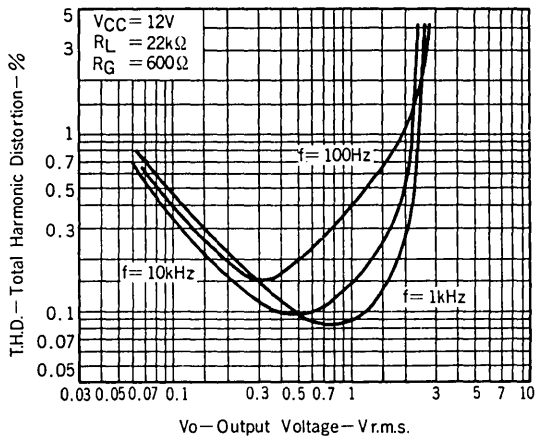
SYMBOL	SW1	SW2	SW3	SW4	SW5	SW6	SW7
I_{CC}	2	3	3	1	2	2	1
A_{vo}	1	1	2	3	2	2	2
V_{om}	1	2	2	3	2	2	2
T.H.D.	1	2	2	3	2	2	2
V_{nin}	3	2	1	3	2	2	2
A_{vo}	2	3	3	2	1	2	2
V_{om}	2	3	3	2	2	2	2
T.H.D.	2	3	3	2	2	2	2
ALC	4	3	3	1	2	1	2

TYPICAL APPLICATION

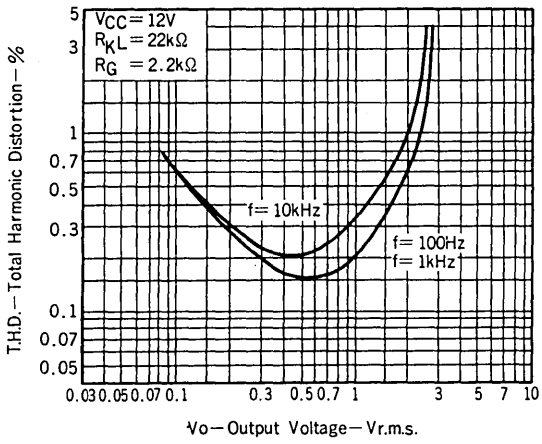


CHARACTERISTICS (Ta=25°C)

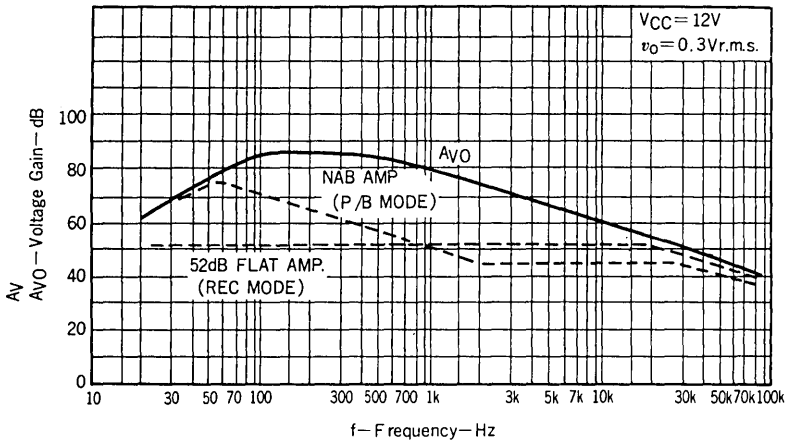
TOTAL HARMONIC DISTORTION
vs. OUTPUT VOLTAGE
(PRE AMP. :P/B-POSITION)



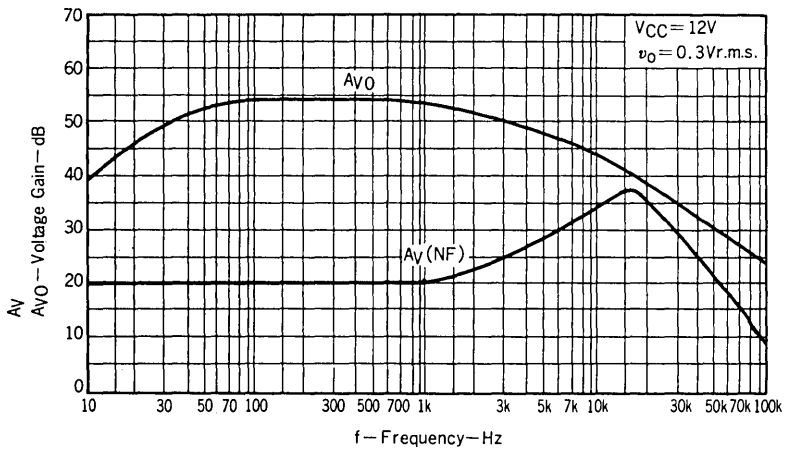
TOTAL HARMONIC DISTORTION
vs. OUTPUT VOLTAGE
(PRE AMP. :REC.-POSITION)



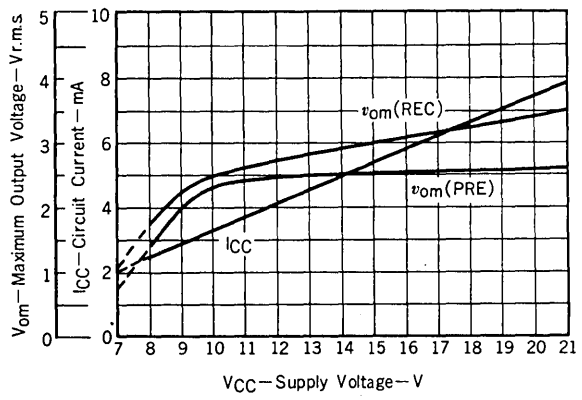
VOLTAGE GAIN vs. FREQUENCY (PRE AMP.)



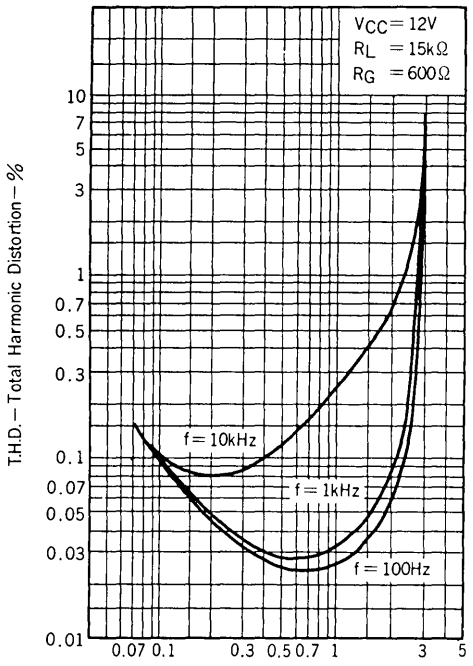
VOLTAGE GAIN vs. FREQUENCY (REC.AMP.)



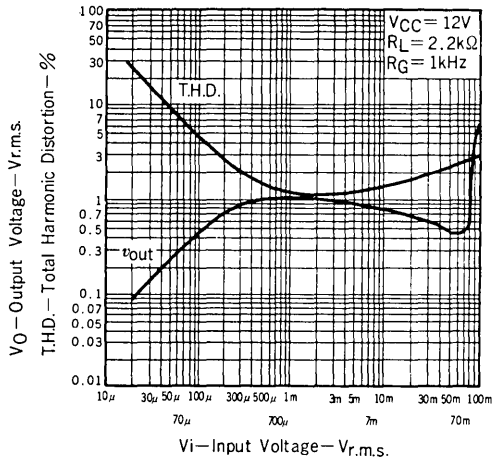
CIRCUIT CURRENT, MAXIMUM OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



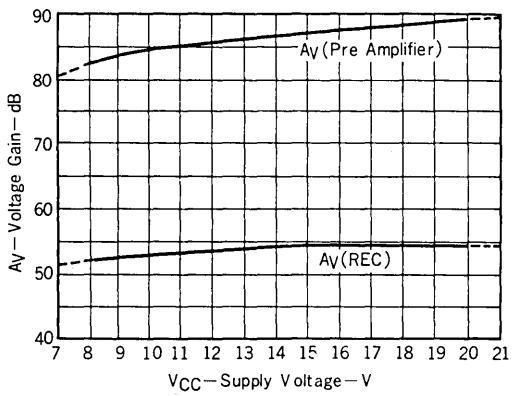
TOTAL HARMONIC DISTORTION vs. OUTPUT VOLTAGE (REC. AMP.)



ALC CHARACTERISTICS (REC. POSITION)



VOLTAGE GAIN vs. SUPPLY VOLTAG



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1217G

RECORDING/PLAY'BACK PREAMPLIFIER SYSTEM

DESCRIPTION

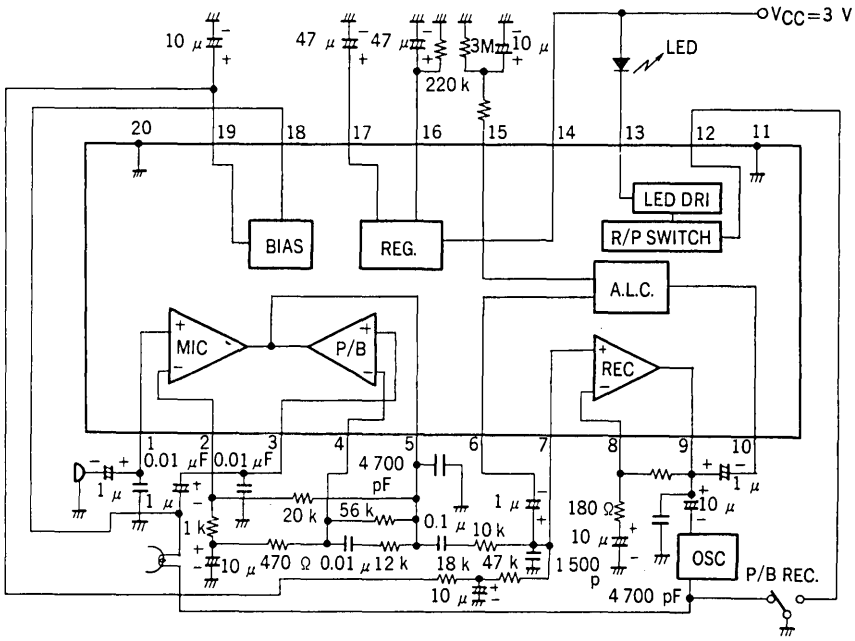
μPC1217G is a monolithic integrated circuit designed for a tape recorder works at low voltage and encapsulated in a smaller package (20-pin MINI FLAT).

μPC1217G has a microphone amplifier, a play'back amplifier, a recording amplifier, a ALC circuit, a LED driver and recording/play'back changeover switch so that is suitable a small tape recorder.

FEATURES

- A recording/play'back changeover switch is built in so that easily design switch circuit.
- Wide operating voltage range. V_{CC} = 1.8 to 3 to 6 V
- Excellent low voltage characteristic.
- New smaller package (20-pin MINI FLAT) so that a small tape recorder is easily designed.
- Only two ICs (μPC1217G, 1218H; Po AMP.) are necessary for a tape recorder.

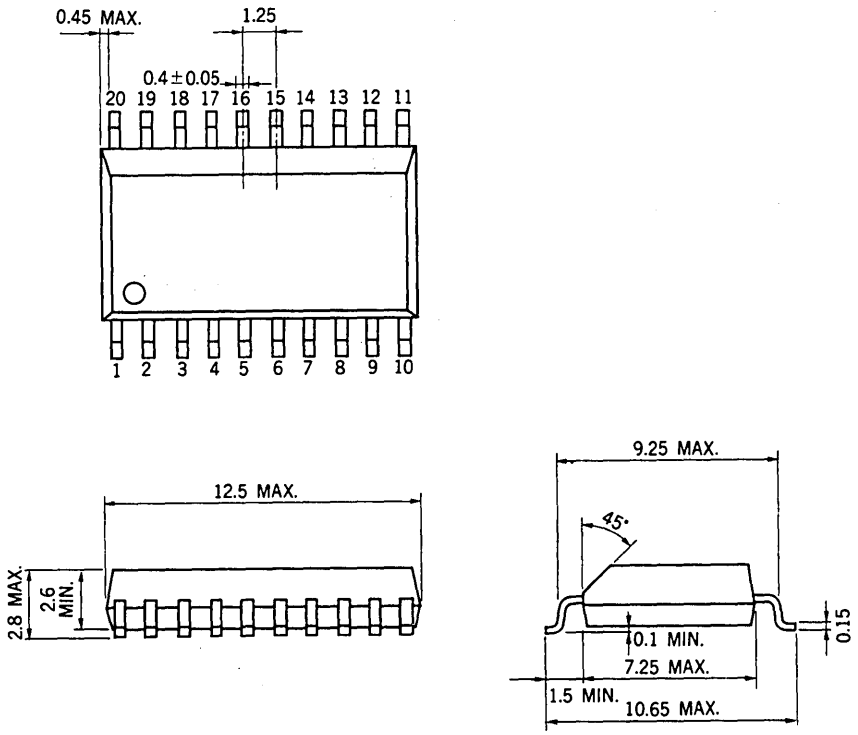
BLOCK DIAGRAM



INTERNAL FUNCTION

- ○ AMPLIFIER – MIC. AMP.
  P/B AMP.
  REC. AMP.
  ALC
- ○ ADDITIONAL FUNCTION – LED DRIVER
  R/P SWITCH

PACKAGE DIMENSIONS (Unit : mm)



CONNECTION DIAGRAM

PIN No.	CONNECTION	PIN No.	CONNECTION
1	Input (MIC.)	11	GND
2	NFB (MIC.)	12	R/P Switch Input
3	Input (P/B)	13	LED Driver Output
4	NFB (P/B)	14	V_{CC}
5	Output (MIC., P/B)	15	ALC Time Constant
6	ALC Output	16	Filter
7	Input (REC.)	17	Filter
8	NFB (REC.)	18	Recording Clamp
9	Output (REC.)	19	Filter & Bias
10	ALC Input	20	GND

ABSOLUTE MAXIMUM RATINGS (Ta=25 °C)

Supply Voltage	V_{CC}	10	V
Package Dissipation	P_D	500	mW
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

RECOMMENDED OPERATING CONDITION (Ta=25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	1.8	3	6	V

ELECTRICAL CHARACTERISTICS (V_{CC}=3 V, f=1 kHz, R_L=10 kΩ, Ta=25 °C)

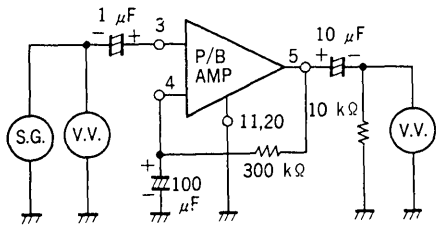
	CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
P/B	Circuit Current	$I_{CC(P/B)}$		6.5	(10.5)	mA	No Signal
	Voltage Gain	$A_{vo(P/B)}$		72		dB	
	Output Maximum Voltage	$v_{OM(P/B)}$	(0.5)	0.8		Vr.m.s.	T.H.D.=1 %
	Total Harmonic Distortion	T.H.D.(P/B)		0.065	(0.7)	%	v_O=0.3 Vr.m.s.
	Input Noise Level	$v_{nin(P/B)}$		1.0	(1.6)	μVr.m.s.	R_G=2.2 kΩ *
	Input Impedance	$R_{in(P/B)}$		36		kΩ	
MIC	Circuit Current	$I_{CC(REC)}$		8.5	(13.5)	mA	
	Voltage Gain	$A_{vo(MIC)}$		52		dB	
	Output Maximum Voltage	$v_{OM(MIC)}$	(0.4)	0.7		Vr.m.s.	T.H.D.=1 %
	Total Harmonic Distortion	T.H.D.(MIC)		0.3	(0.7)	%	v_O=0.3 Vr.m.s.
	Input Noise Level	$v_{nin(MIC)}$		1.0	(1.6)	μVr.m.s.	R_G=2.2 kΩ *
	Input Impedance	$R_{in(MIC)}$		36		kΩ	
REC	Voltage Gain	$A_{vo(REC)}$		70		dB	
	Output Maximum Voltage	$v_{OM(REC)}$	(0.5)	0.9		Vr.m.s.	T.H.D.=1 %
	Total Harmonic Distortion	T.H.D.(REC)		0.2	(0.7)	%	v_O=0.3 Vr.m.s.
	ALC Effect			2.6	(9)	dB	v_{in}=−70 → −40 dBm
	ALC Range		(45)	64		dB	T.H.D. ≤ 3 %
	Ripple Rejection	R.R.R.		70		dB	R_G=2.2 kΩ, f=100 Hz
	LED Current	I_{LED}	(6)	9	(12)	mA	

* f=10 Hz ~ 10 kHz B.P.F. (6 dB/oct)

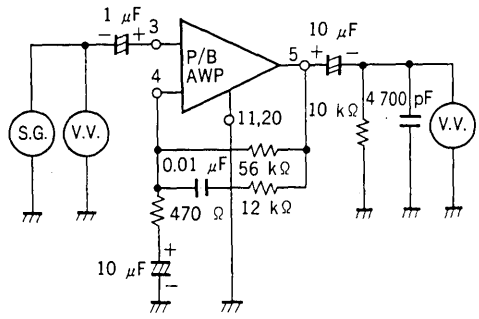
TEST CIRCUIT

TEST CIRCUIT 1

① Voltage Gain (P/B AMP.)

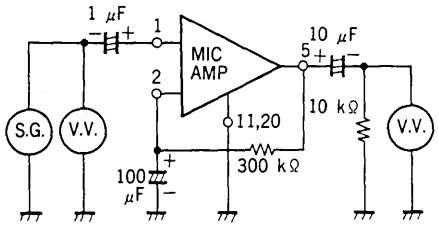


② Frequency Characteristics (P/B AMP.)

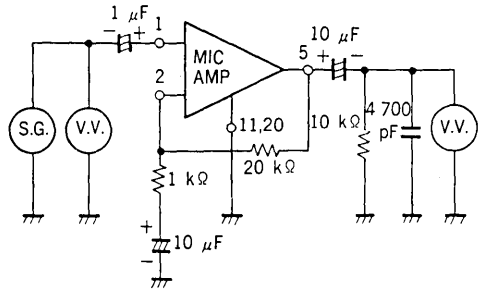


TEST CIRCUIT 2

① Voltage Gain (MIC. AMP.)

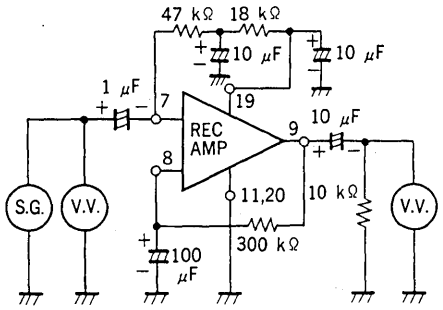


② Frequency Characteristics (MIC. AMP.)

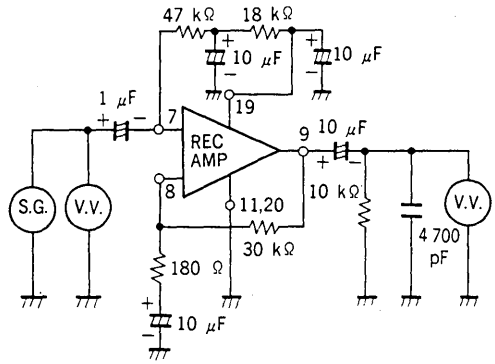


TEST CIRCUIT 3

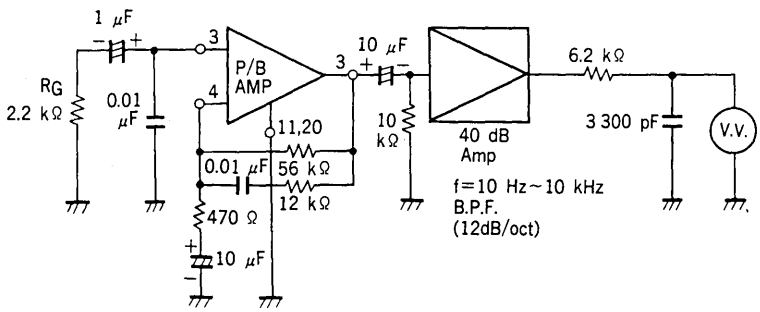
① Voltage Gain (REC. AMP.)



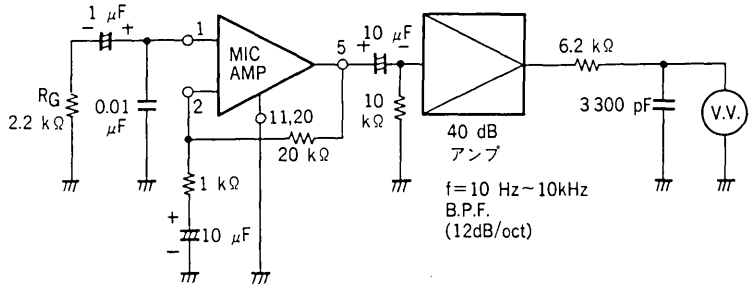
② Frequency Characteristics (REC. AMP.)



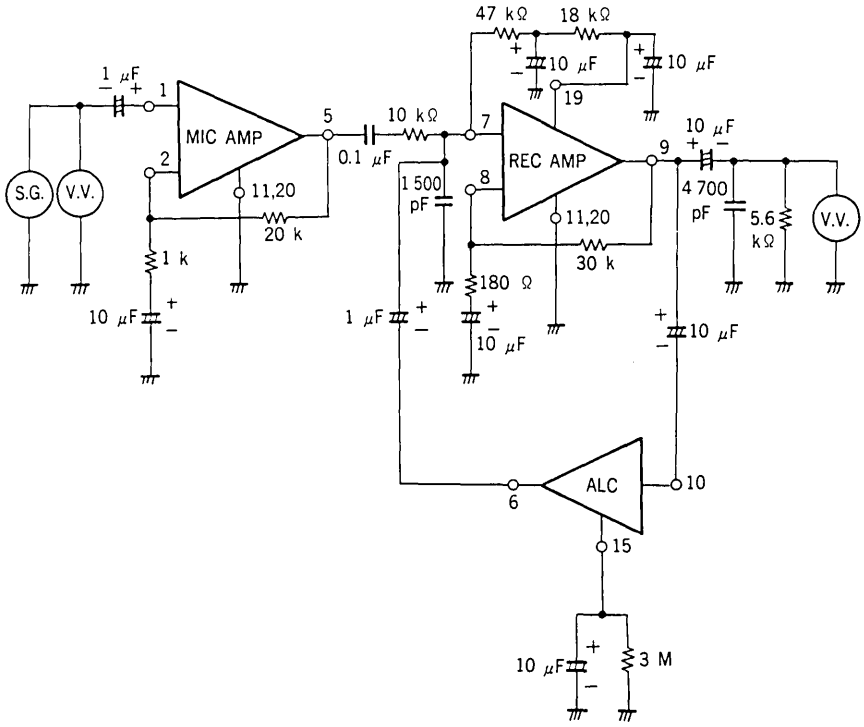
TEST CIRCUIT 4 P/B AMP. Noise



TEST CIRCUIT 5　　MIC. AMP. Noise

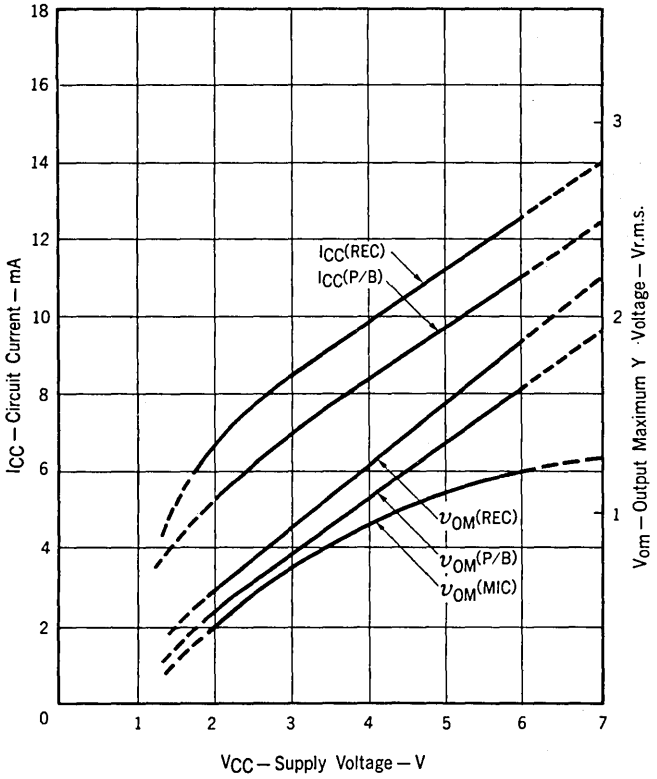


TEST CIRCUIT 6　　ALC Characteristics

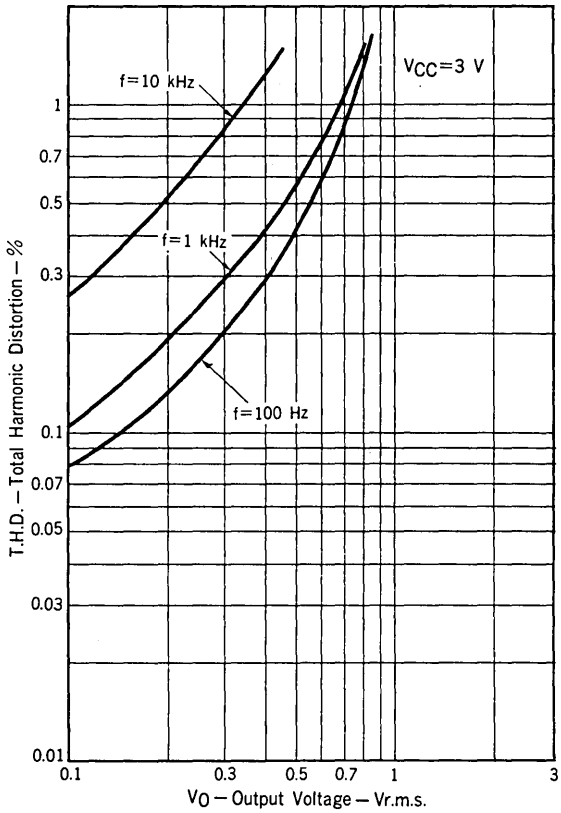


TYPICAL CHARACTERISTICS (Ta=25 °C)

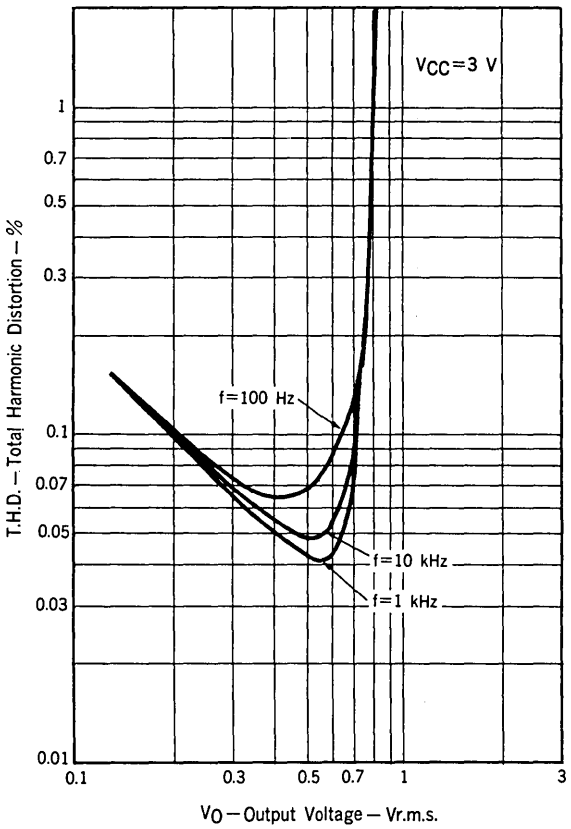
CIRCUIT CURRENT, OUTPUT MAXIMUM VOLTAGE vs. SUPPLY VOLTAGE



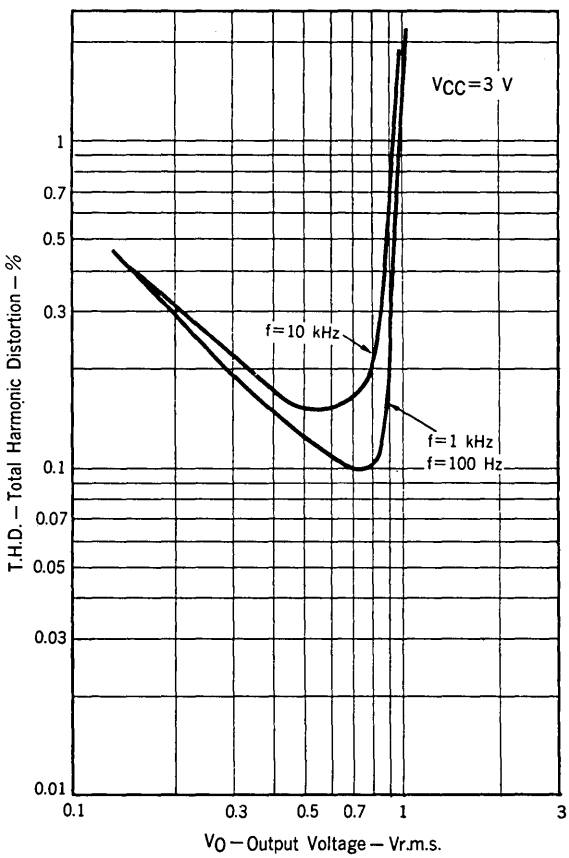
TOTAL HARMONIC DISTORTION vs. OUTPUT VOLTAGE (MIC. AMP.)



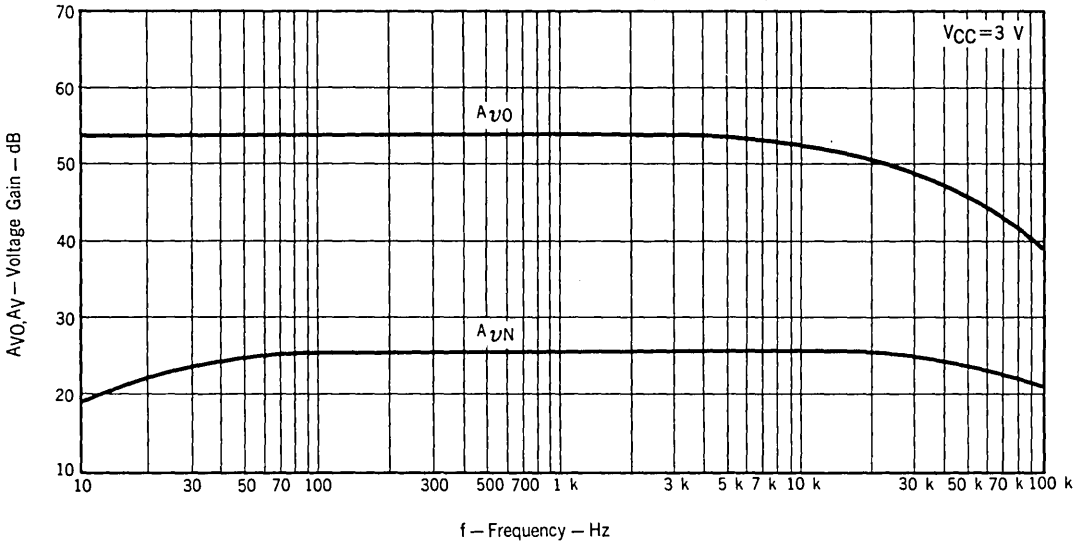
TOTAL HARMONIC DISTORTION vs. OUTPUT VOLTAGE (MIC. AMP.)



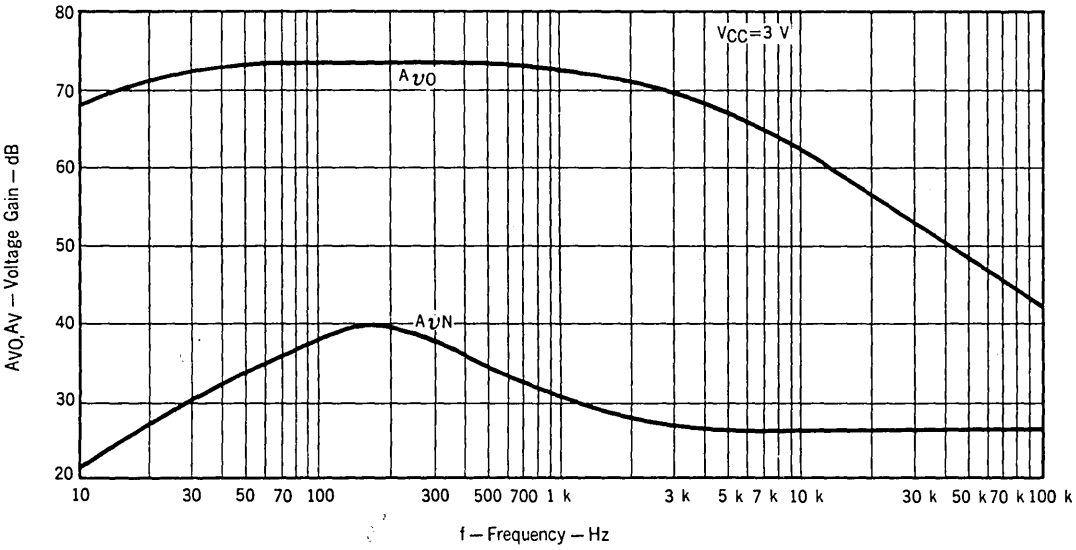
TOTAL HARMONIC DISTORTION vs. OUTPUT VOLTAGE (REC. AMP.)



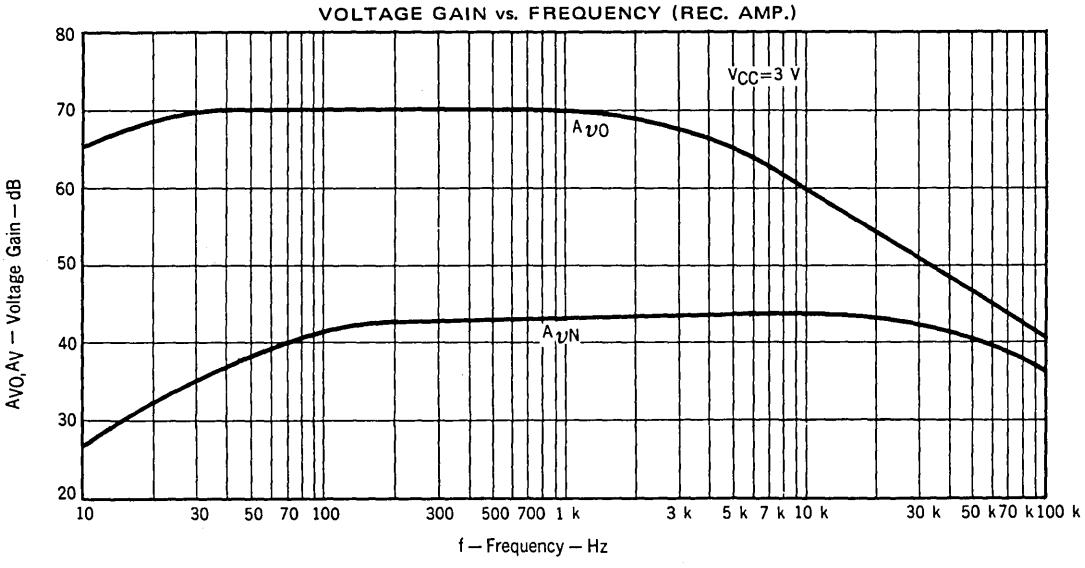
VOLTAGE GAIN vs. FREQUENCY (MIC. AMP.)



VOLTAGE GAIN vs. FREQUENCY (P/B AMP.)



VOLTAGE GAIN vs. FREQUENCY (REC. AMP.)



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1177H

2-CHANNEL AUDIO POWER AMPLIFIER
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

DESCRIPTION

The μPC1177H is a silicon monolithic integrated circuit in a 12-pin single in-line plastic package, designed for audio power amplifier applications in cassette tape recorders or radio recievers which operate at a 6 volt power supply.

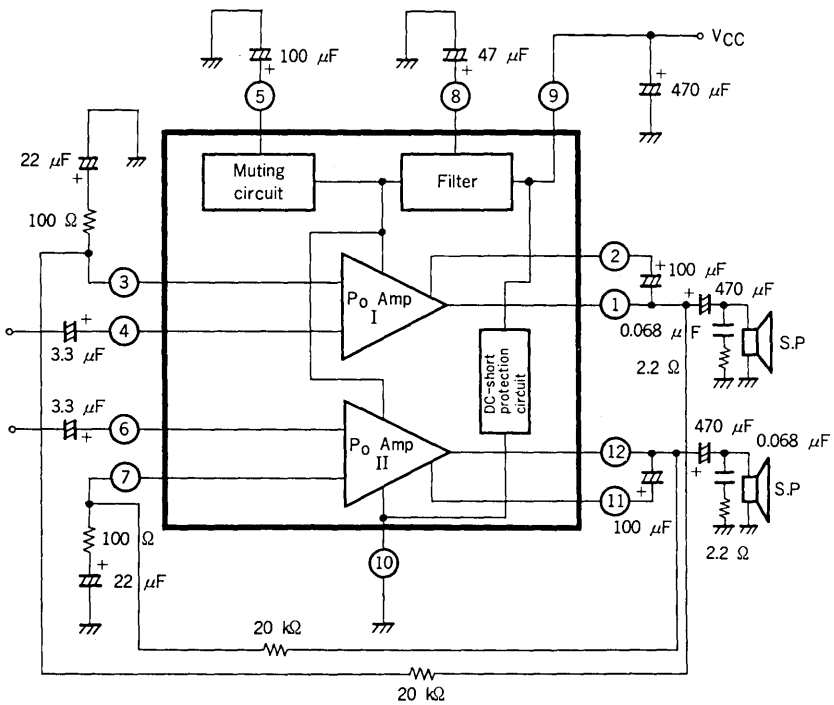
The μPC1177H has two audio power amplification circuits and each of the two provides 1 W output power at 6 V/4 Ω. In addition, the μPC1177H provides 3.5 W output power at 6 V/4 Ω, when it is operated as a BTL amplifier.

FEATURES

- High output power. BTL 3.5 W (TYP.) at 6 V/4 Ω, T.H.D.=10 %
  DUAL 1 W (TYP.) at 6 V/4 Ω, T.H.D.=10 %
- Wide operating voltage range. V_{CC}=3.5 to 10 V
- No shock noise at power supply switch-over.
- Soft clipping wave form.
- High ripple rejection ratio. R.R.R.=55 dB (TYP.)
- DC-short (pin 1, pin 12 to pin 10) protection circuit.
- Excellent low voltage characteristic. ΔA_{VO}=3 dB (TYP.)
  $\Delta A_{VO}=A_{VO}(6\ V)-A_{VO}(3.5\ V)$
- Flat and pierced fin so that an external heat sink can easily be attached.
- A 12-pin single plastic package so that can easily be mounted on PCB.

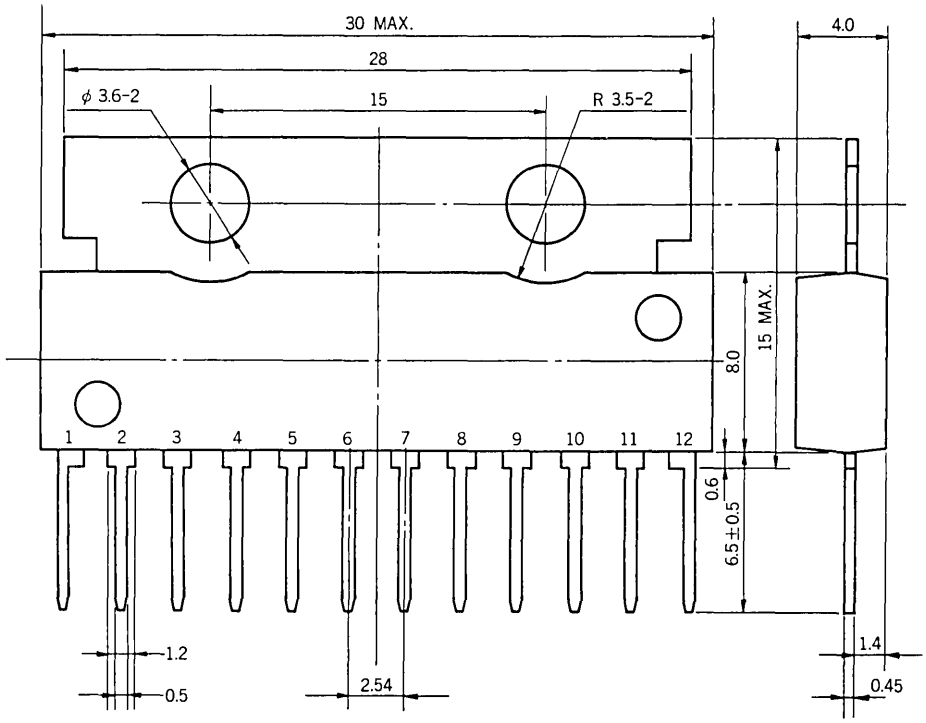
BLOCK DIAGRAM

(External compornents; DUAL amplifier)



PACKAGE DIMENSIONS (Unit: mm)

Typical value unless otherwise noted



CONNECTION DIAGRAM

UNIT	CONNECTION	UNIT	CONNECTION
1	Out (Amp I)	7	Feedback (Amp II)
2	Boot strap (Amp I)	8	Filter
3	Feedback (Amp I)	9	Vcc
4	Input (Amp I)	10	GND
5	Filter	11	Boot strap (Amp II)
6	Input (Amp II)	12	Out (Amp II)

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Supply Voltage	V_{CC}	10	V
Package Dissipation	P_D	4.3	W
Circuit Current	$I_{CC\ (peak)}$	2	A
Operating Temperature	T_{opt}	−20 to 75	°C
Storage Temperature	T_{stg}	−40 to 150	°C

RECOMMENDED CONDITIONS (Ta = 25 °C)

Operating Supply Voltage	V_{CC}=6 V
Load Impedance	R_L=4 Ω to 8 Ω

ELECTRIC CHARACTERISTICS

(BTL OPERATION)

V_{CC} = 6 V, R_L = 4 Ω, f = 1 kHz, Ta = 25°C
with a 100 x 100 x 1 mm Al heat sink

ITEM	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Circuit Current	I_{CC}	V_{in} = 0	(15)	30	(50)	mA
Open Loop Voltage Gain	A_{VO}	P_O = 0.5 W	(61)	68	(75)	dB
Voltage Gain	A_V	P_O = 0.5 W		46		dB
Output Power	P_O	T.H.D. = 10 %	(2.7)	35		W
Total Harmonic Distortion	T.H.D.	P_O = 0.5 W		0.5	(1.5)	%
Output Noise Level	NL	R_G = 0		0.3	(1.0)	mVr.m.s.
Ripple Rejection Ratio	R.R.R.	R_G = 0 fripple = 100 Hz Vripple = 0.3 Vr.m.s.	(45)	55		dB
Input Impedance	R_{in}			20		kΩ

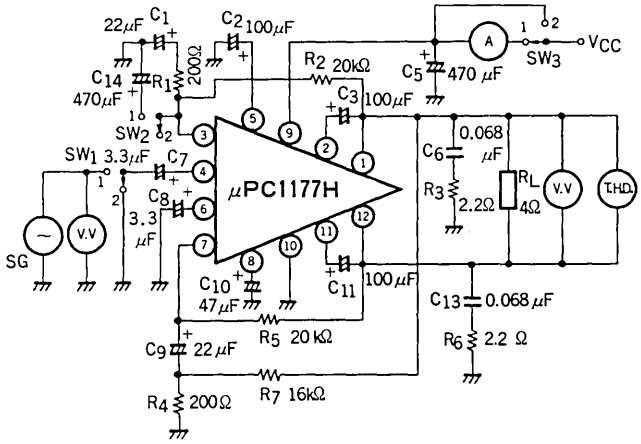
(DUAL OPERATION)

V_{CC} = 6 V, R_L = 4 Ω, f = 1 kHz, Ta = 25°C
with a 100 x 100 x 1 mm Al heat sink

Open Loop Voltage Gain	A_{VO}	P_O = 0.25 W	(57)	64	(71)	dB
Voltage Gain	A_V	P_O = 0.25 W		46		dB
Output Power	P_O	T.H.D. = 10 %	(0.8)	1.0		W
Total Harmonic Distortion	T.H.D.	P_O = 0.25 W		0.4	(1.5)	%
Output Noise Level	NL	R_G = 0		0.2	(0.8)	mVr.m.s.
Ripple Rejection Ratio	R.R.R.	R_G = 0 fripple = 100 Hz Vripple = 0.3 Vr.m.s.	(45)	55		dB
Cross Talk	C.T.	R_G = 0 P_O = 0.25 W	(40)	55		dB
Voltage Gain Change	ΔA_{VO}	V_O = −10 dBm A_{VO} (6 V) − A_{VO} (3.5 V)		3	(6)	dB

TEST CIRCUIT

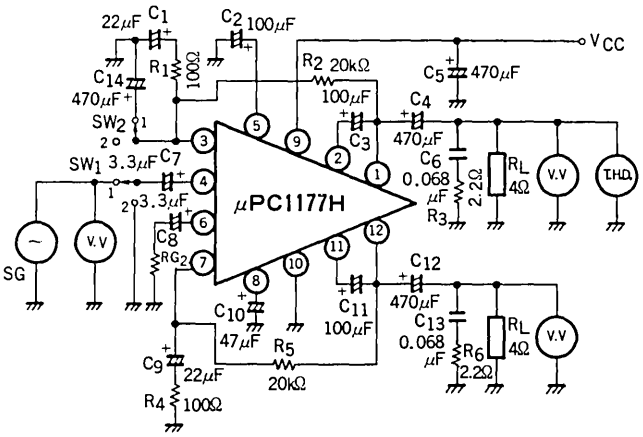
(BTL OPERATION)



SWITCH POSITION

ITEM	SYMBOL	SW1	SW2	SW3
Circuit Current	I_{CC}	2	2	1
Open Loop Voltage Gain	A_{VO}	1	1	2
Voltage Gain	A_V	1	2	2
Output Power	P_O	1	2	2
Total Harmonic Distortion	T.H.D.	1	2	2
Output Noise Level	NL	2	2	2

(DUAL OPERATION)

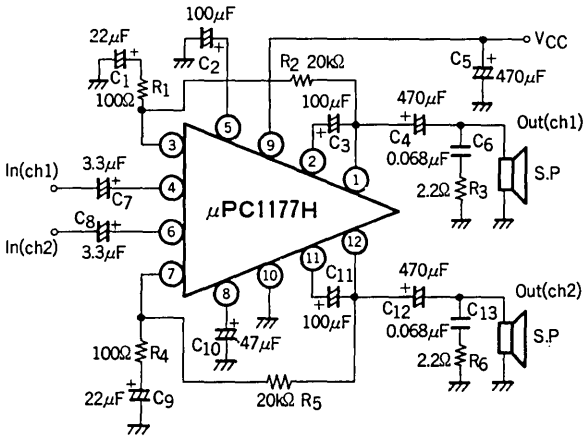


SWITCH POSITION

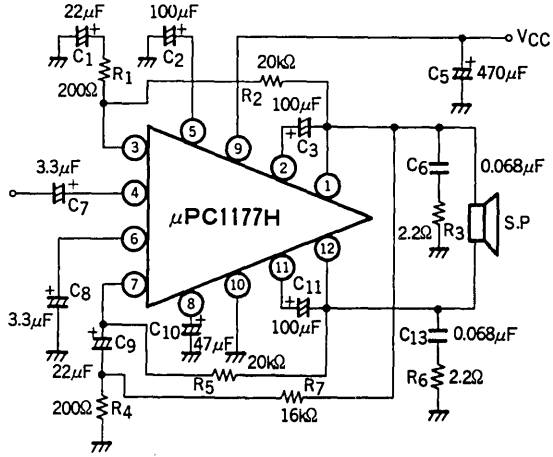
ITEM	SYMBOL	SW1	SW2
Open Loop Voltage Gain	A_{VO}	1	1
Voltage Gain	A_V	1	2
Output Power	P_O	1	2
Total Harmonic Distortion	T.H.D.	1	2
Output Noise Level	NL	2	2
Cross Talk	C.T.	1	2

TYPICAL APPLICATION

(DUAL OPERATION)



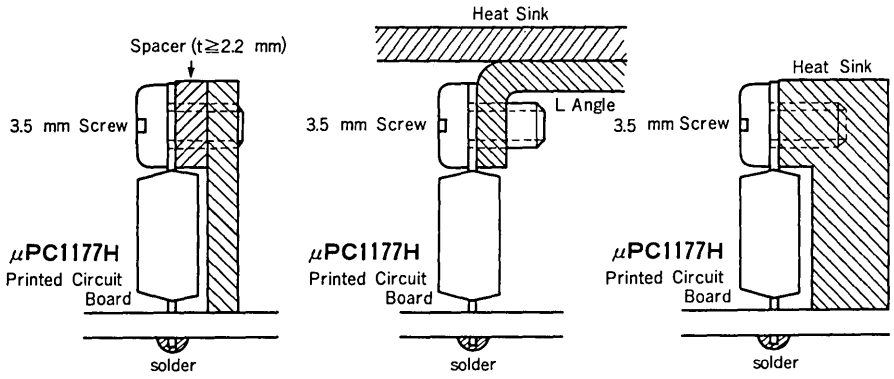
(BTL OPERATION)



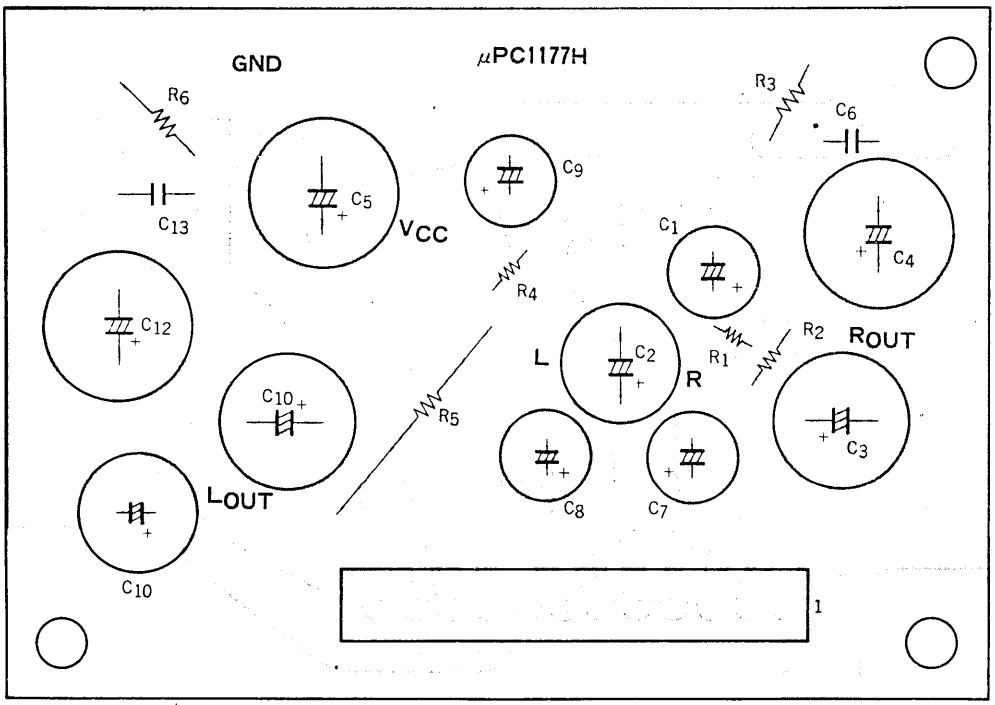
NOTES FOR USE

1. About external components.
   1–1. Capacitor C_1 and C_9 are concerned in low cut-off frequency, rising time and shock noise at power supply swich-over, so that are recommended 22 μF as their values.
   1–2. Capacitor C_2 rejects shock noise at power supply switch-over and works as a ripple filter. Use 100 μF as its value.
   1–3. Attach the (–) lead of capacitor C_5 near the point that 10 pin of μPC1177H is attached on a PCB.
   1–4. Capacitor C_6, C_{13} and resistor R_3, R_6 prevent parasitic oscillations.
   Maylor capacitors are recommended as C_6, C_{13}.
   Use larger capacitor as C_6, C_{13} if a parasitic oscillation may occur due to an earthing on a PCB.

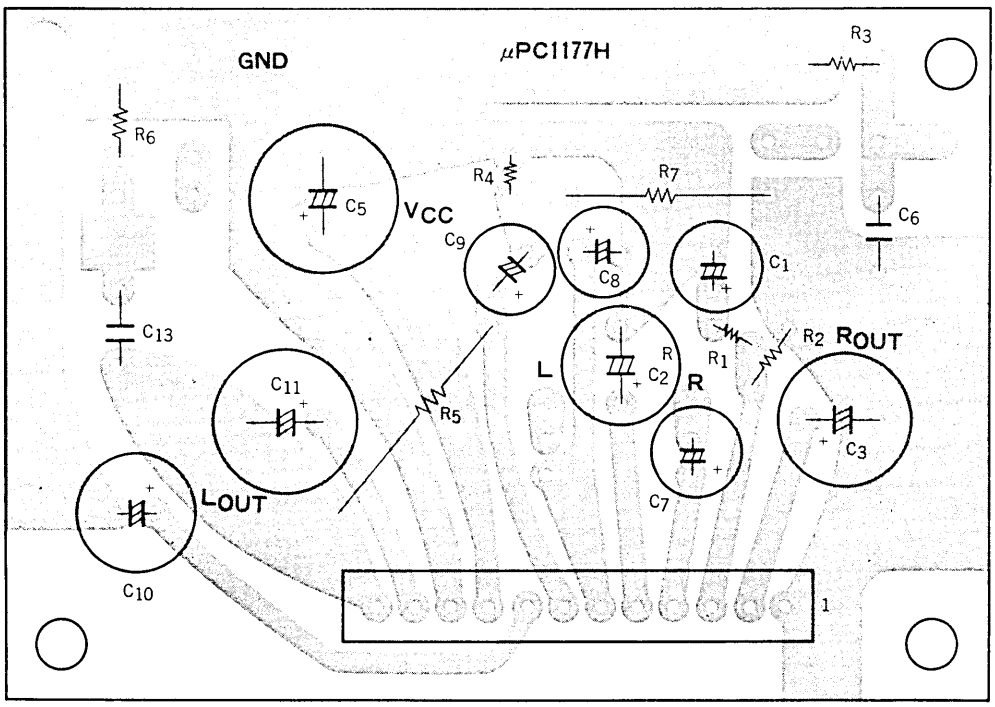
2. Suggested mounting.
   2–1. Use sillicon grease.
   2–2. Use a torque of 4 to 6 kg-cm.



TYPICAL PWB (Copper side)



(DUAL OPERATION)

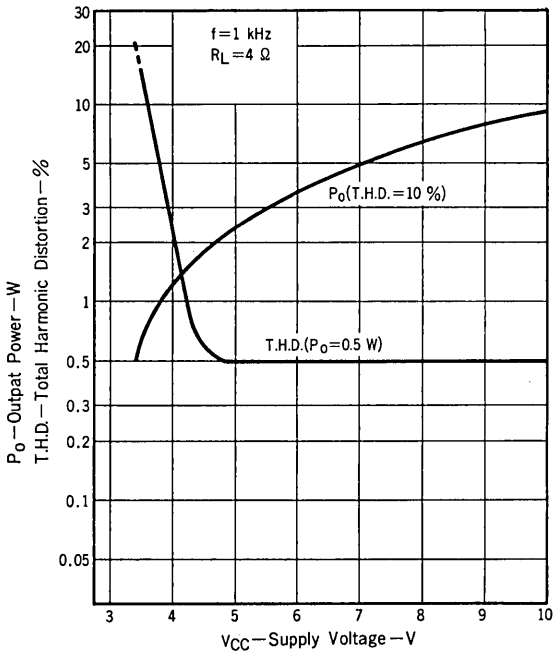


(BTL OPERATION)

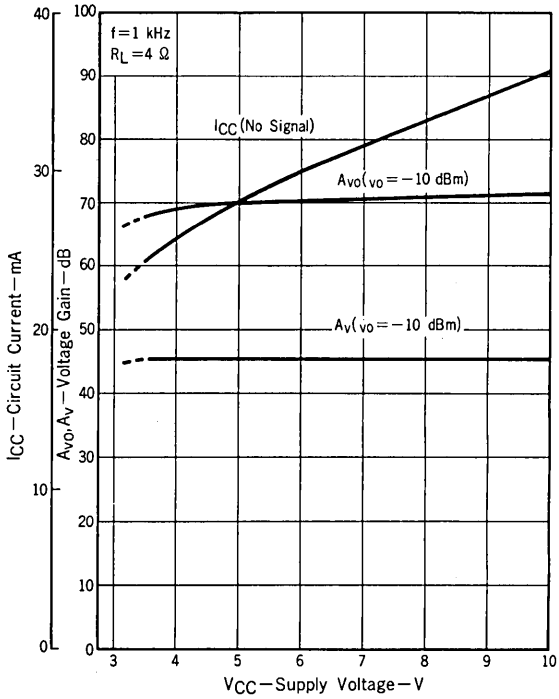
TYPICAL CHARACTERISTICS (Ta = 25 °C)

(BTL OPERATION) V_{CC}=6 V, R_L=4 Ω, f=1 kHz,
with a 100 x 100 x 1 mm³ heat sink

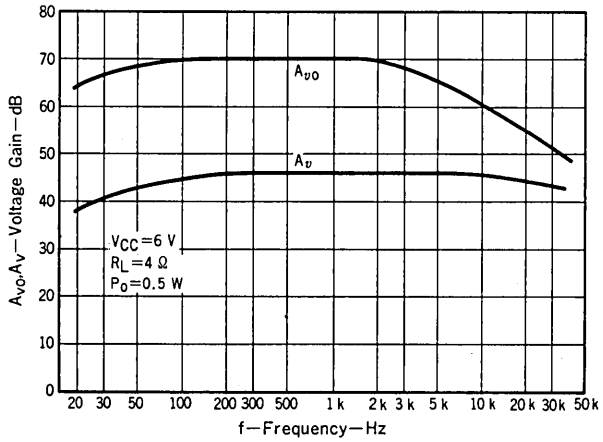
OUTPUT POWER, TOTAL HARMONIC DISTORTION vs. SUPPLY VOLTAGE



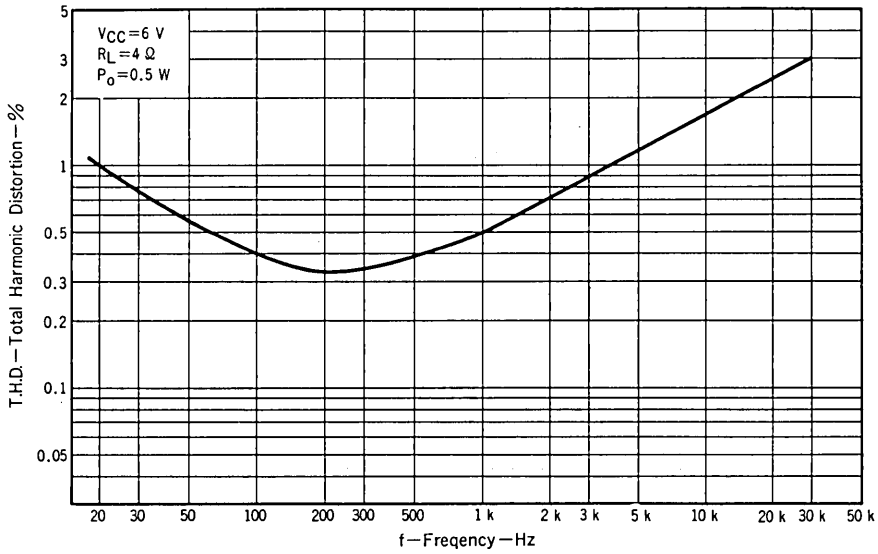
CIRCUIT CURRENT, VOLTAGE GAIN vs. SUPPLY VOLTAGE



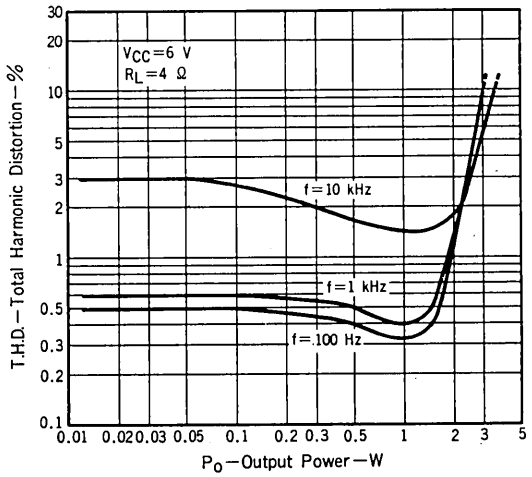
VOLTAGE GAIN vs. FREQENCY



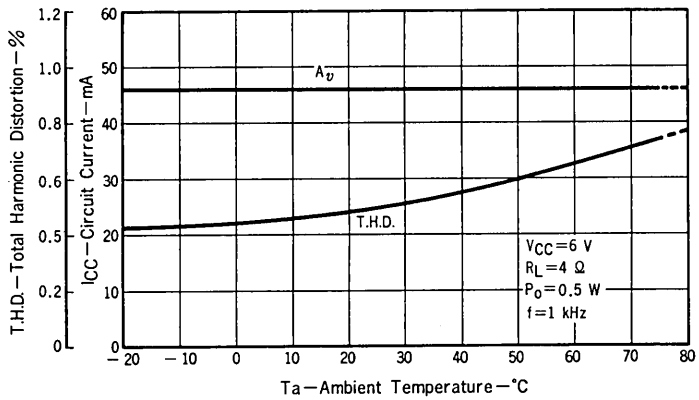
TOTAL HARMONIC DISTORTION vs. FREQENCY



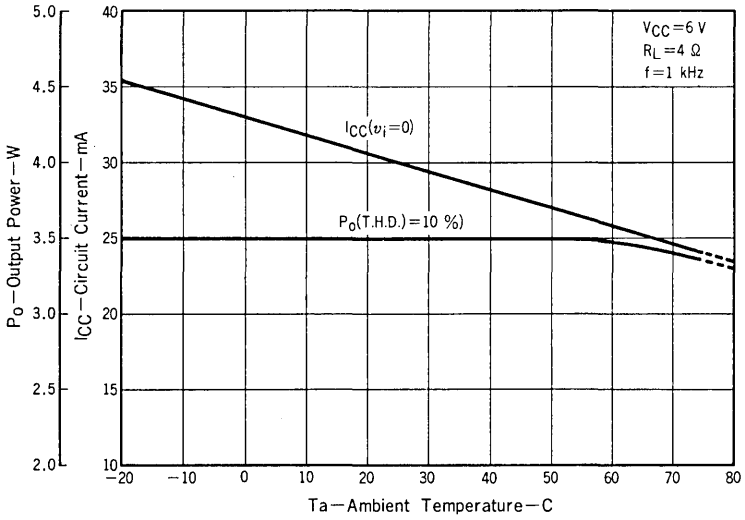
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



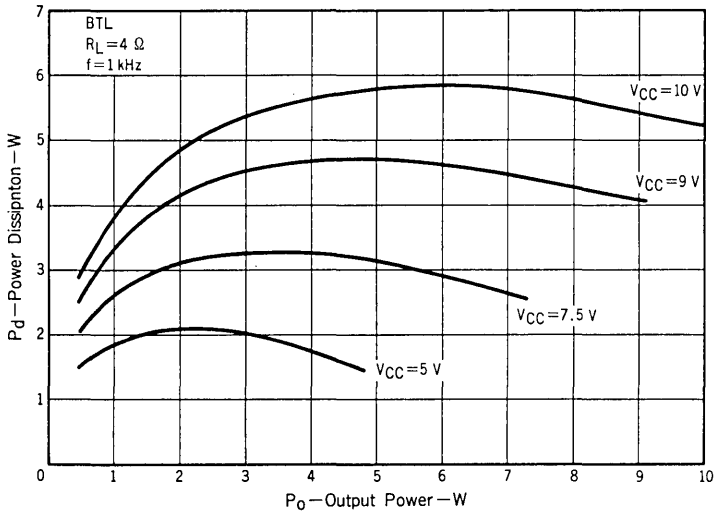
VOLTAGE GAIN, TOTAL HARMONIC DISTORTION vs. AMBIENT TEMPERATURE



CIRCUIT CURRENT, OUTPUT POWER vs. AMBIENT TEMPERATURE

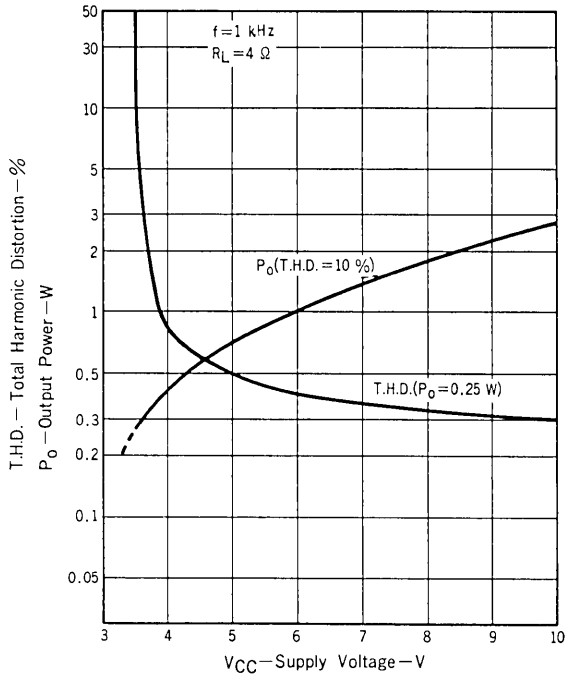


POWER DISSIPATION vs. OUTPUT POWER

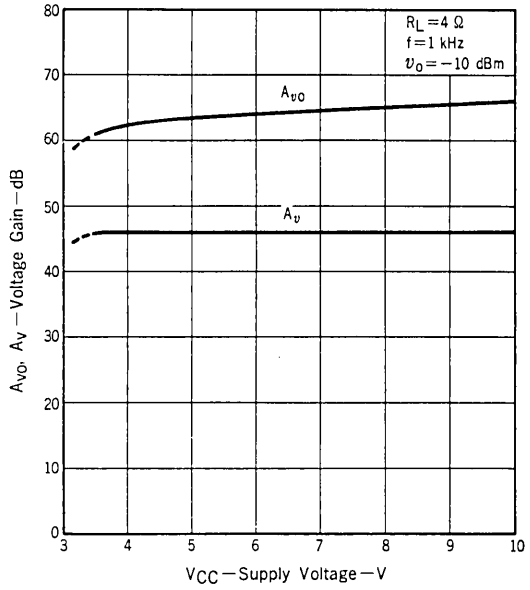


(DUAL OPERATION) V_{CC}=6 V, RL=4 Ω, f=1 kHz,
with a 100 x 100 x 1 mm^3 Al heat sink

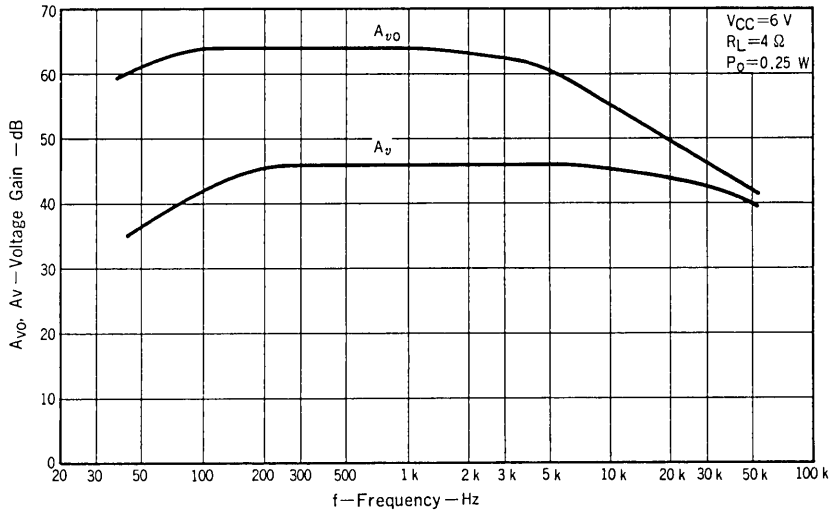
OUTPUT POWER, TOTAL HARMONIC DISTORTION vs. SUPPLY VOLTAGE



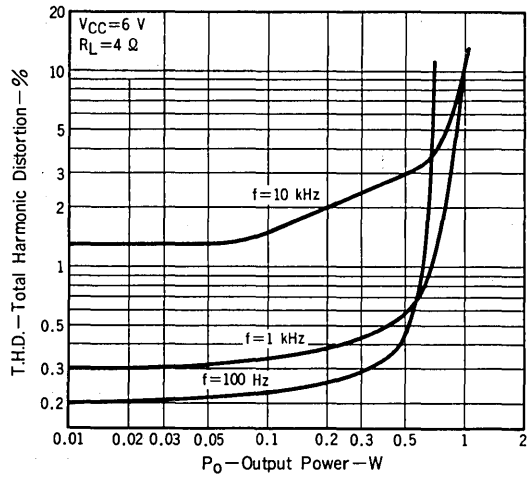
VOLTAGE GAIN vs. SUPPLY VOLTAGE



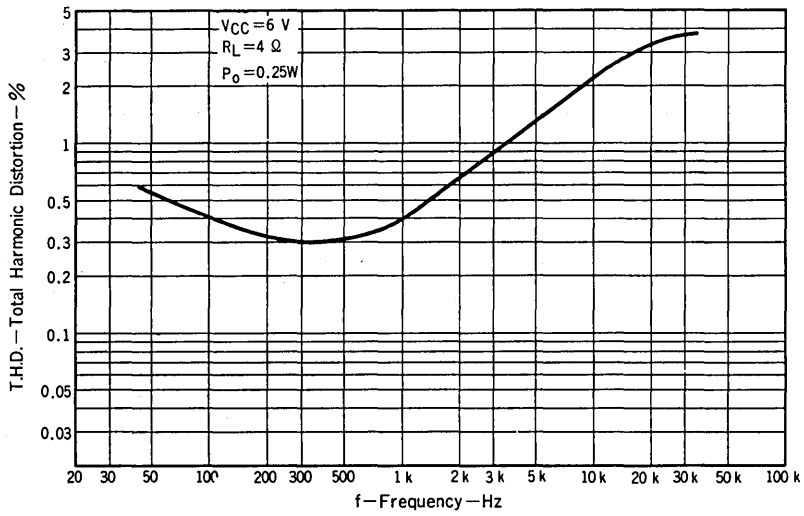
VOLTAGE GAIN vs. FREQENCY



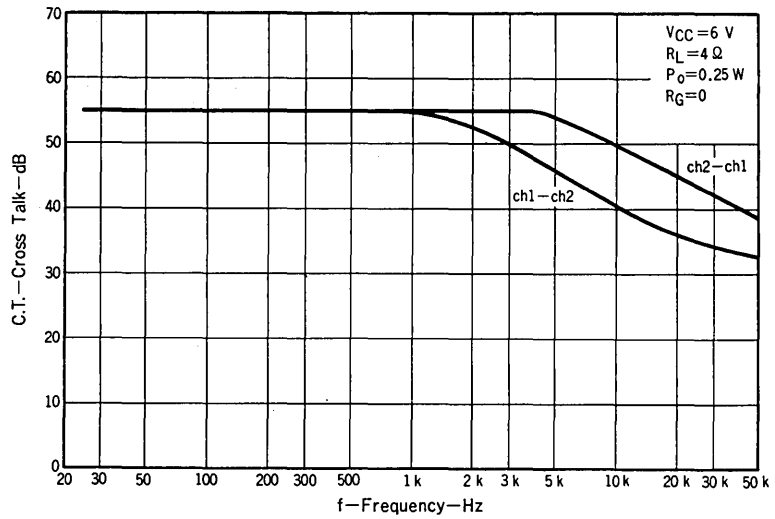
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



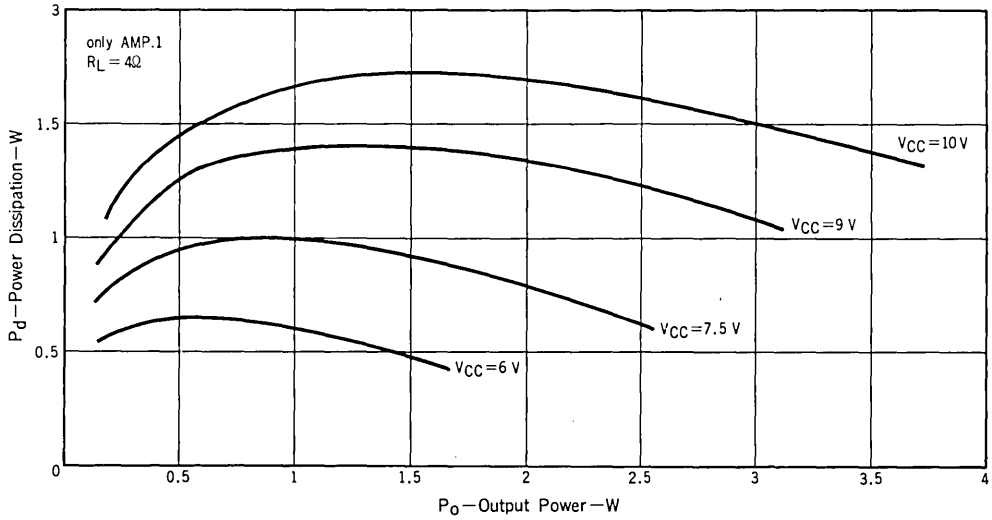
TOTAL HARMONIC DISTORTION vs. FREQENCY



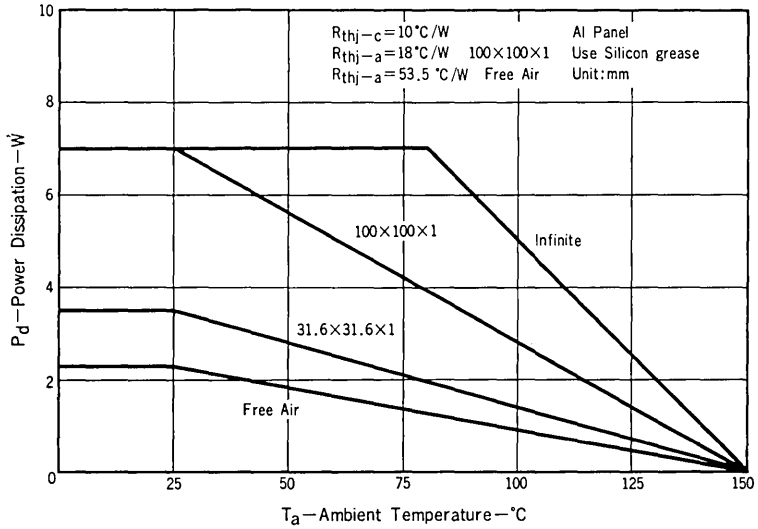
CROSS TALK vs. FREQENCY



POWER DISSIPATION vs. OUTPUT POWER



POWER DISSIPATION vs. AMBIENT TEMPERATURE



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1212C

AUDIO POWER AMPLIFIER

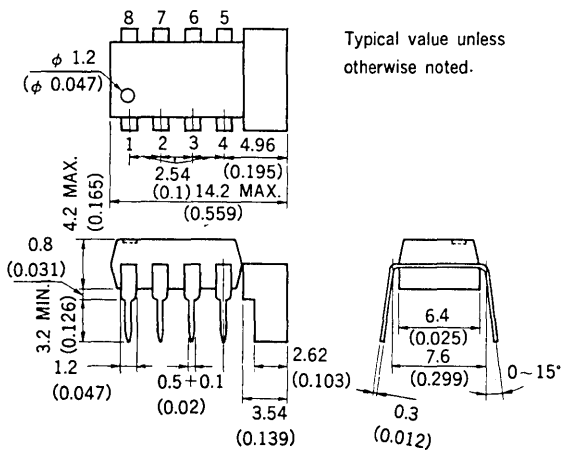
DESCRIPTION

The μPC1212C is a silicon monolithic integrated circuit designed for an audio power amplifier used in a portable radio receiver or a portable cassette tape recorder which works at 6-volt power supply.

The μPC1212C is encapsulated in an 8-pin dual in line plastic package with a tab.

PACKAGE DIMENSIONS

in millimeters (inches)



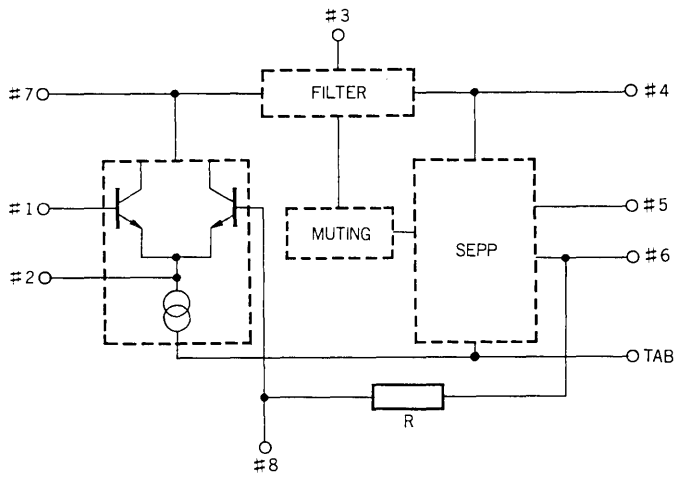
FEATURES

- High output power. P_o = 1 W (TYP.)
  at V_{CC} = 6 V, R_L = 4 Ω, T.H.D. = 10 %
- Wide operating voltage range.
  V_{CC} = 3.5 to 6 to 9 V
- High ripple rejection ratio.
  R.R.R. = 55 dB (TYP.)
- Soft clipping waveform.
- Have a muting circuit so that no shock noise at power supply switch on and off.
- Have a terminal to reject interference noise in strong electric field. (pin 2)

CONNECTION DIAGRAM

No.	CONNECTION	No.	CONNECTION
1	INPUT	5	BOOTSTRAP
2		6	OUTPUT
3	FILTER	7	FILTER
4	V_{CC}	8	N. F. B.
TAB	GND		

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{CC1}	(No Signal)	11	V
Supply Voltage	V_{CC2}	(Operating)	9	V
Allowable Power Dissipation	P_d	*	2.4	W
Operating Temperature	T_{opt}	−20 to 70		°C
Storage Temperature	T_{stg}	−40 to 150		°C

* 50 x 50 x 0.035 mm copper heat sink on P.C.B.

RECOMMENDED CONDITIONS (T_a = 25 °C)

Supply Voltage	V_{CC} = 3.5 to 6 to 9 V
Load Impedance	R_L = 4 Ω

ELECTRIC CHARACTERISTICS (T_a = 25 °C)

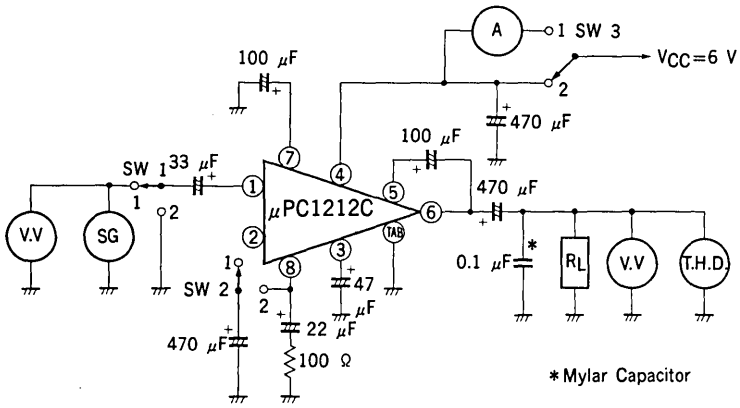
(Refer to the test circuits V_{CC}=6 V, R_L=4 Ω, 50 X 50 X 0.035 mm copper heat sink on P.C.B. unless otherwise specified)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Quiscent Circuit Current	I_{CC}	8	15	25	mA	No Signal
Open Loop Voltage Gain	A_{VO}	55	65		dB	P_O=0.25 W, f=1 kHz
Voltage Gain (Closed Loop)	A_V	41	45	48	dB	R_f=100 Ω f=1 kHz
			34			R_f=360 Ω f=1 kHz
Output Power	P_O					T.H.D.=10 %
			2.4			f=1 kHz, R_f=100 Ω V_{CC}=9 V, R_L=4 Ω
			1.3			V_{CC}=9 V, R_L=8 Ω
		0.7	1.0		W	V_{CC}=6 V, R_L=4 Ω
			0.54			V_{CC}=6 V, R_L=8 Ω
			0.41			V_{CC}=4 V, R_L=4 Ω
			0.22			V_{CC}=4 V, R_L=8 Ω
Input Sensitibity	$V_{i(rms)}$					P_O=1 W R_L=4 Ω, f=1 kHz
			16.4			R_f=100 Ω (A_V=45 dB)
			47.4		mV	R_f=360 Ω (A_V=34 dB)
Input Sensitivity	$V_{i(rms)}$					P_O=50 mW R_L=4 Ω, f=1 kHz
			2.5			R_f=100 Ω (A_V=45 dB)
			8.9		mV	R_f=360 Ω (A_V=34 dB)
Total Harmonic Distortion	T.H.D.		0.4	1.5	%	P_O=0.25 W
Output Noise Voltage	NL		0.2	0.8	$mV_{r.m.s.}$	R_G=0
Supply Voltage Rejection Ratio	S.V.R.	40	55		dB	R_G=0, f_{ripple}=100 Hz V_{ripple}=0.3 $V_{r.m.s.}$
Input Impedance	R_i	10	20		kΩ	

NOTE: In case that only a TYP. value is specified, this specification is for helping to design.

TEST CIRCUIT

Fig. 1 TEST CIRCUIT



SWITCH POSITION

ITEM \ SWITCH		SW1	SW2	SW3
Circuit Current	I_{CC}	2	1	1
Open Loop Voltage Gain	A_{VO}	1	2	2
Voltage Gain	A_V	1	1	2
Output Power	P_O	1	1	2
Total Harmonic Distortion	T.H.D.	1	1	2
Output Noise Voltage	NL	2	1	2

TYPICAL APPLICATION

Fig. 2 SINGLE OPERATION

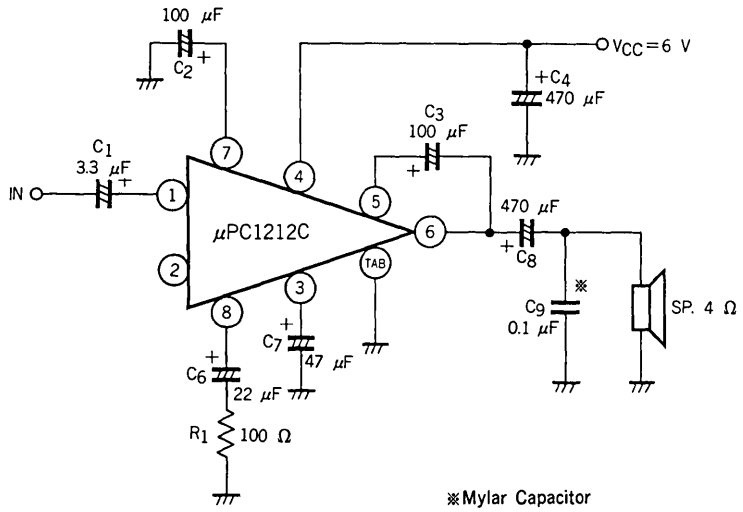


Fig. 3 BTL OPERATION

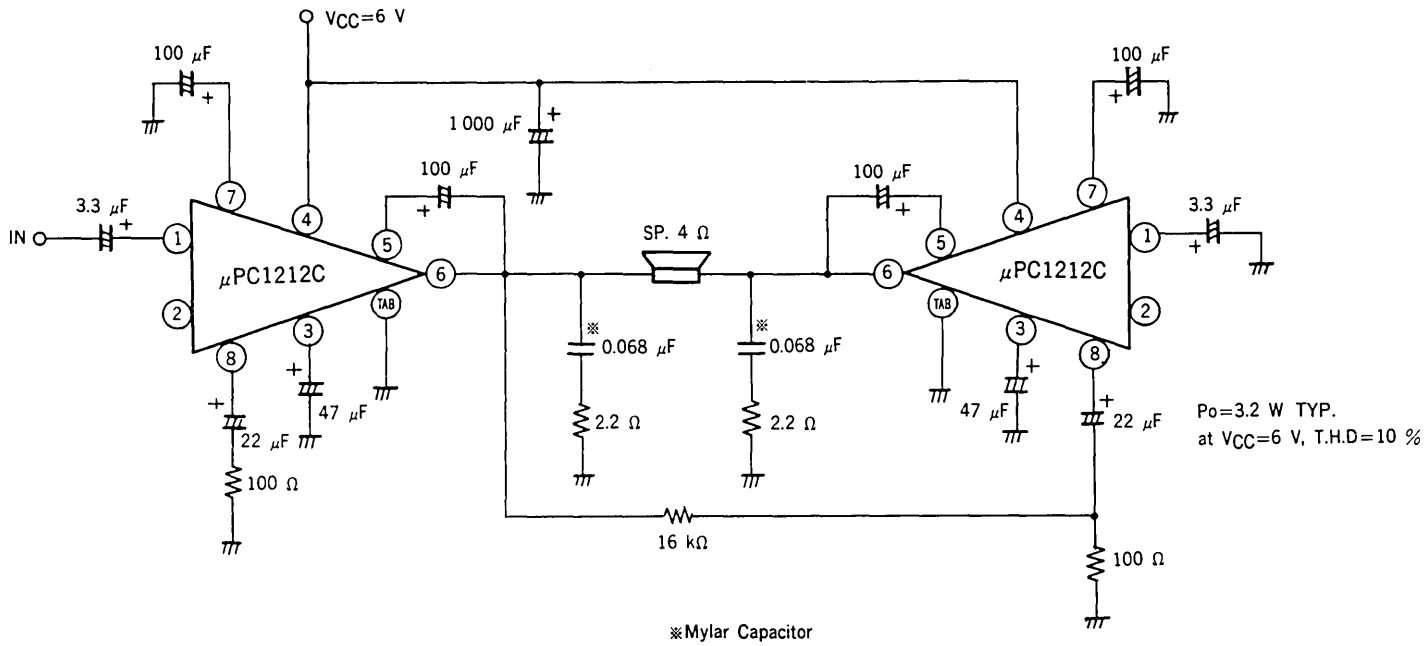
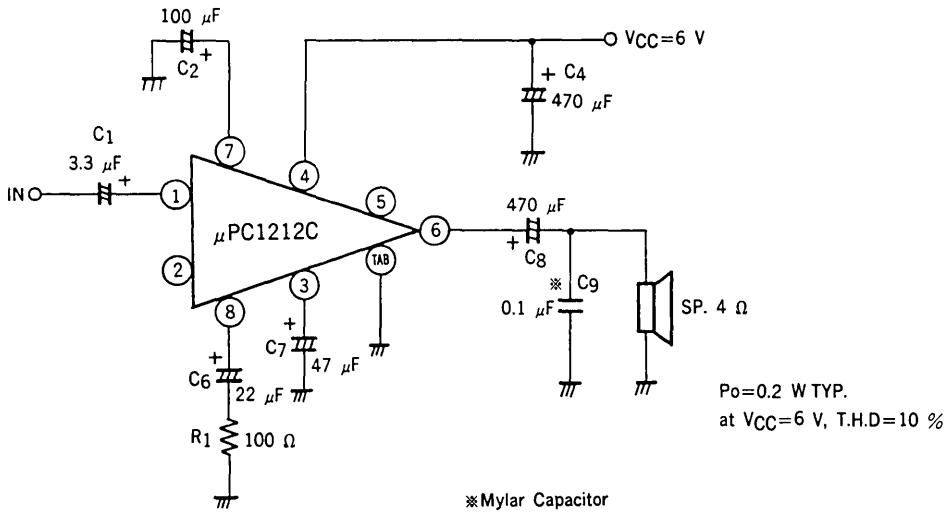


Fig. 4 SINGLE OPERATION WITHOUT BOOTSTRAP



NOTE FOR USE

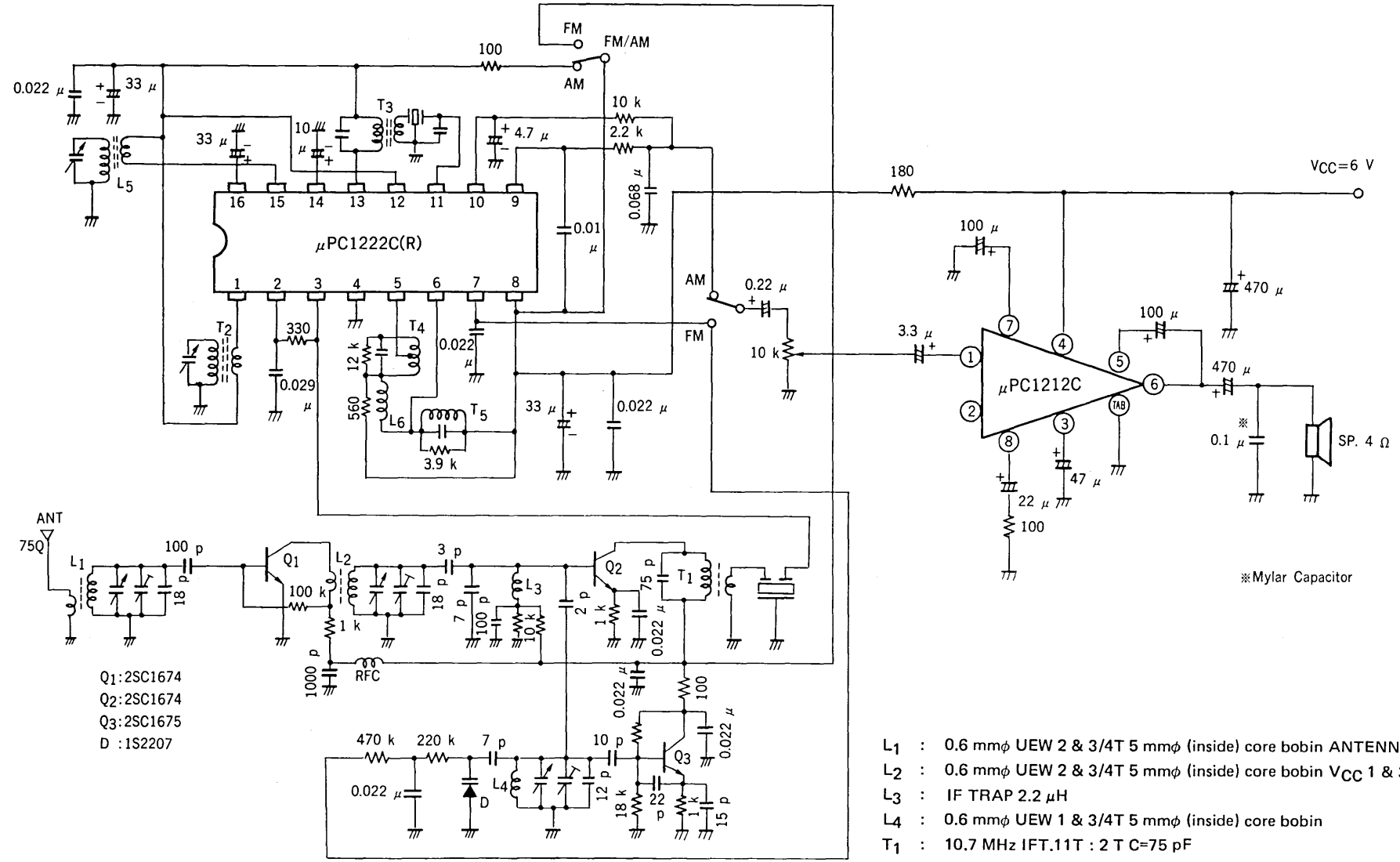
(1) Capacitor C_9 is for preventing the parastic oscillation. A mylar capacitor is recommended for this position.

(2) The ground side of C_4, C_9 and the loud speaker should be attached at the place of the copper foil close to the tab of μPC1212C.

(3) Interference noise rejection in a strong electric field can be achieved by adding a capacitor (about 1 000 pF) between pin 1 and pin 2.

APPLICATION INFORMATION

Fig. 5 LOW COST FM-AM RADIO WITH 1.0 W OUTPUT POWER (V_{CC}=6 V)



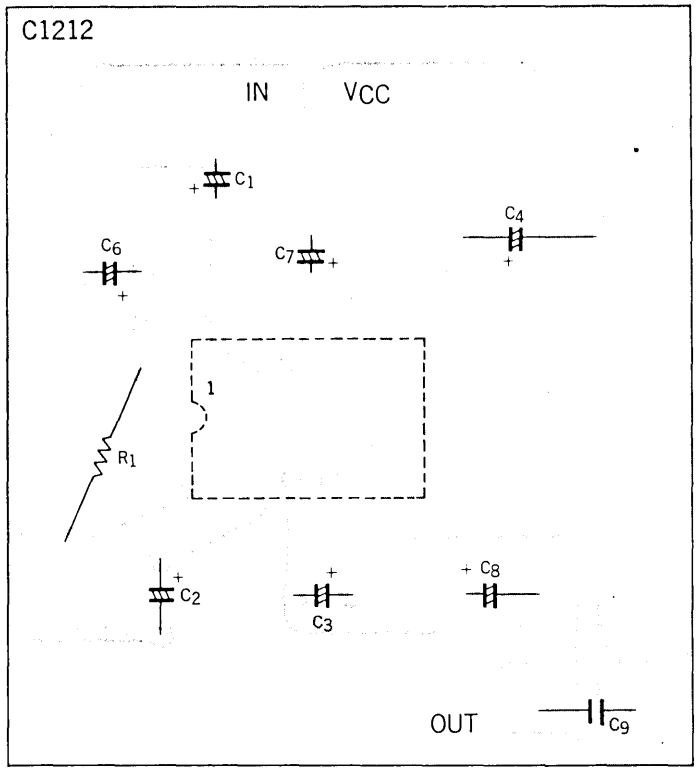
※Mylar Capacitor

Q1:2SC1674
Q2:2SC1674
Q3:2SC1675
D :1S2207

UNIT : Capacitance F
Resistance Ω

L_1 : 0.6 mmϕ UEW 2 & 3/4T 5 mmϕ (inside) core bobin ANTENNA 3/4T
L_2 : 0.6 mmϕ UEW 2 & 3/4T 5 mmϕ (inside) core bobin V_{CC} 1 & 3/4T
L_3 : IF TRAP 2.2 μH
L_4 : 0.6 mmϕ UEW 1 & 3/4T 5 mmϕ (inside) core bobin
T_1 : 10.7 MHz IFT.11T : 2 T C=75 pF
L_5 : ANTENNA COIL 25A-1195-08 (KOHRIN)
T_2 : AM OSC 26-1791-13 (KOHRIN)
T_3 : AM IFT CFZ-455C (TOKO)
T_4 : AM DET. 5251 (TOKO)
T_5 : FM DET. 12747 (TOKO)
L_6 : PHASE SHIFT COIL 7BA180JH (TOKO)

P.C. BOARD PATTERN (COPPER SIDE)



TYPICAL CHARACTERISTICS (Ta = 25 °C)

Fig. 6 OUTPUT POWER vs. SUPPLY VOLTAGE

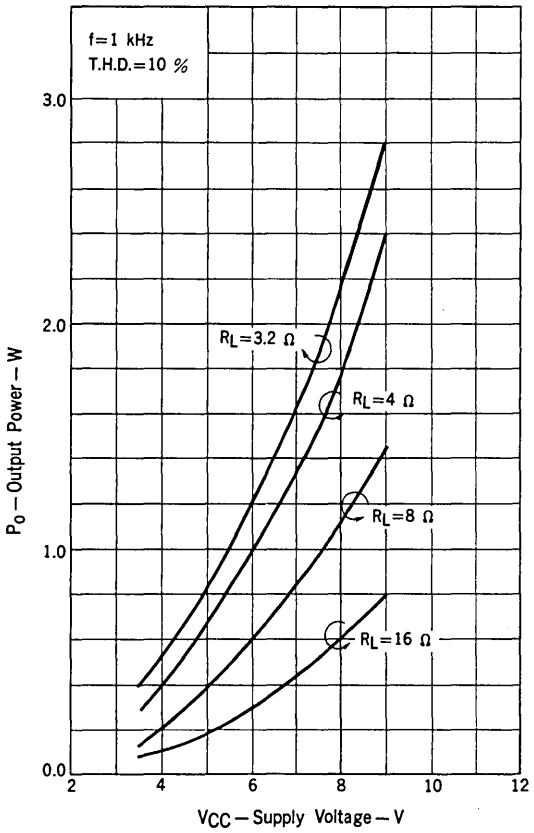


Fig. 7 TOTAL HARMONIC DISTORTION vs. OUTPUT POWER

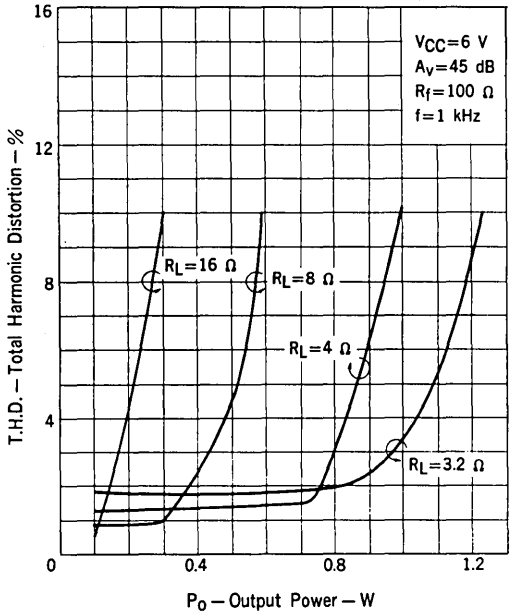


Fig. 8 POWER DISSIPATION AND EFFICIENCY vs. OUTPUT POWER

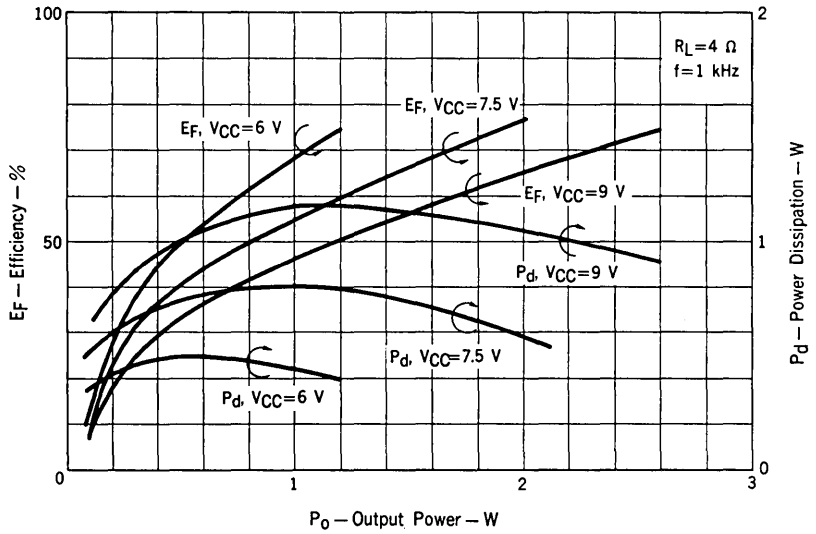


Fig. 9 INPUT SENSITIVITY vs. R_f

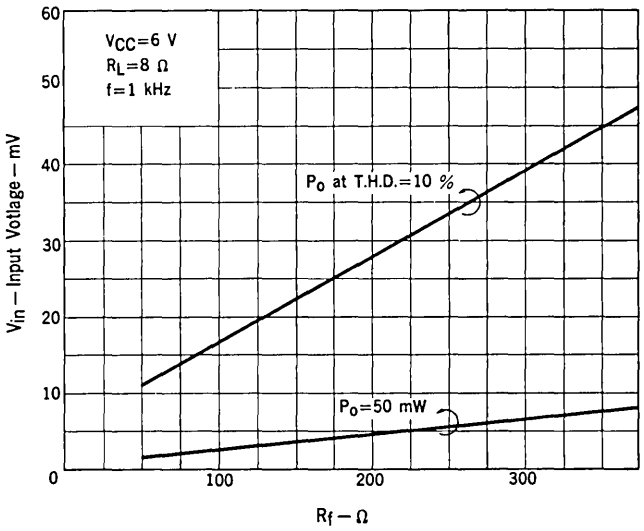


Fig. 10 VOLTAGE GAIN (CLOSED LOOP) vs. R_f

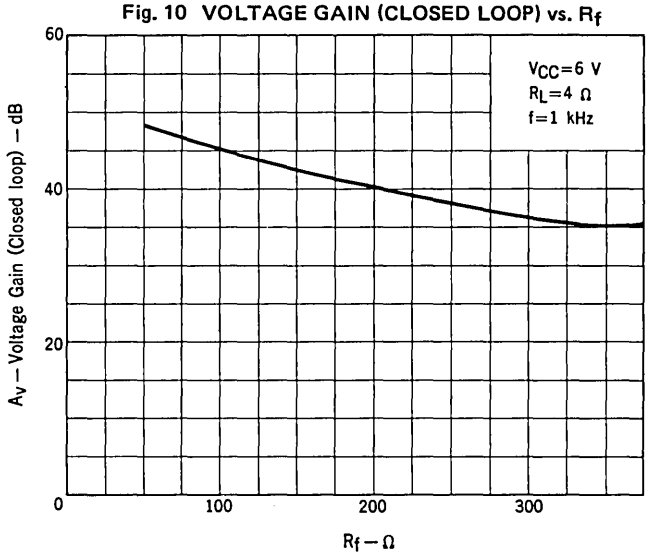


Fig. 11 QUISCENT OUTPUT VOLTAGE AT PIN 6 vs. SUPPLY VOLTAGE

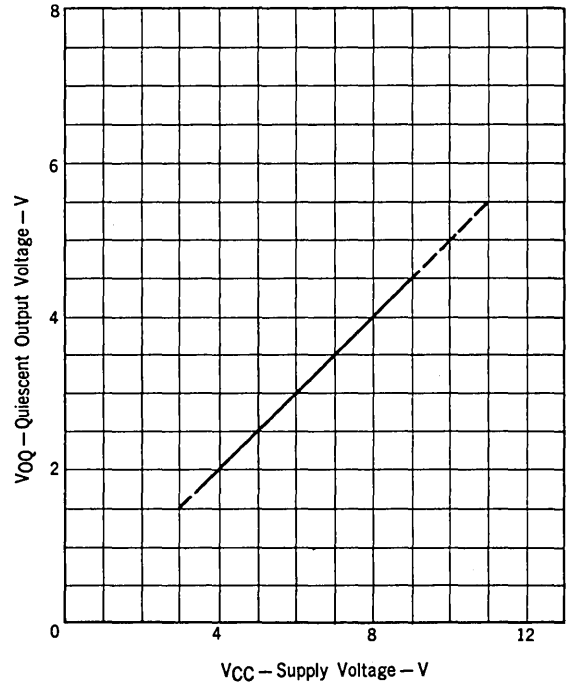


Fig. 12 QUIESCENT CIRCUIT CURRENT vs. SUPPLY VOLTAGE

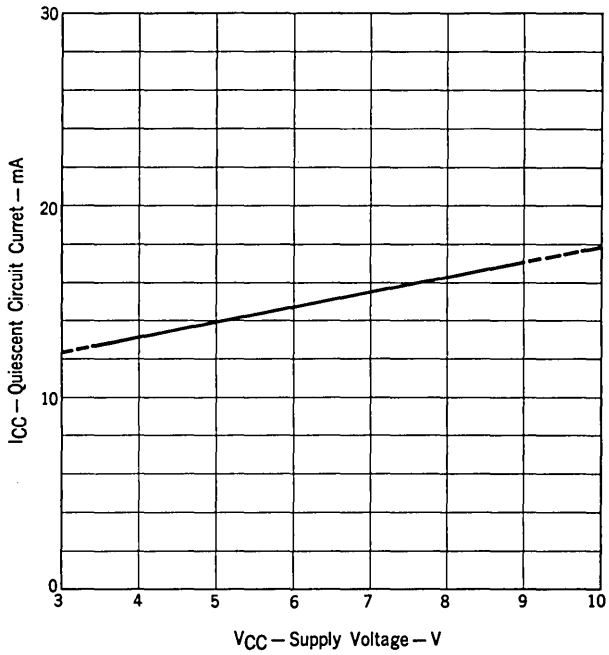


Fig. 13 OPEN LOOP VOLTAGE GAIN, VOLTAGE GAIN vs. FREQUENCY

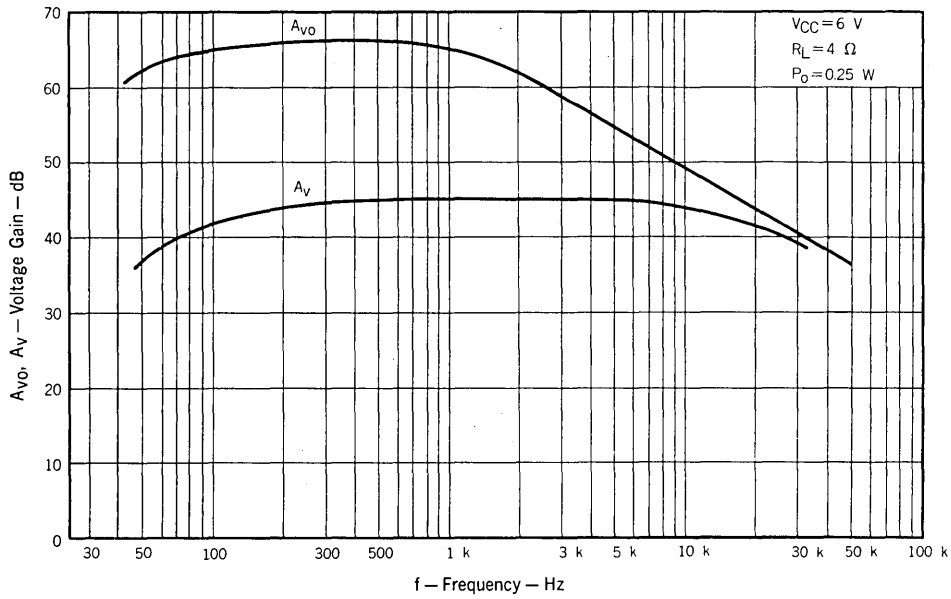


Fig. 14 TOTAL HARMONIC DISTORTION vs. FREQUENCY

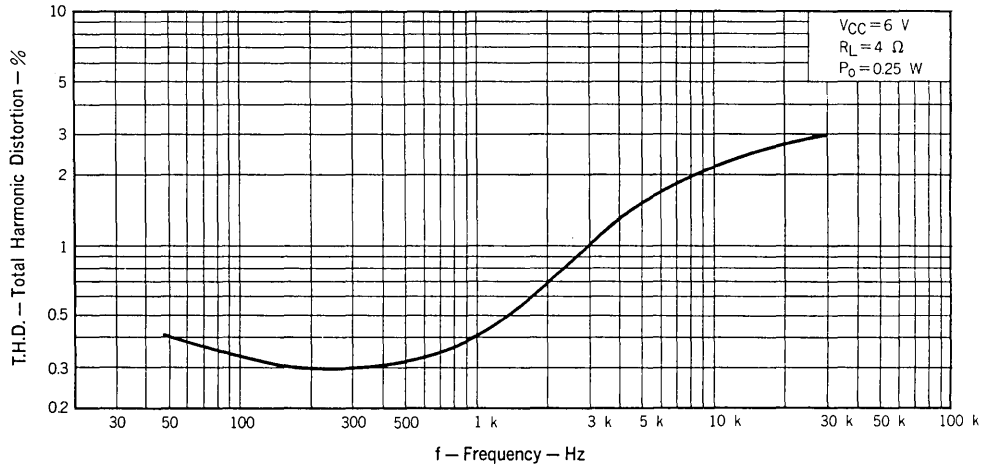


Fig. 15 THERMAL CHARACTERISTICS

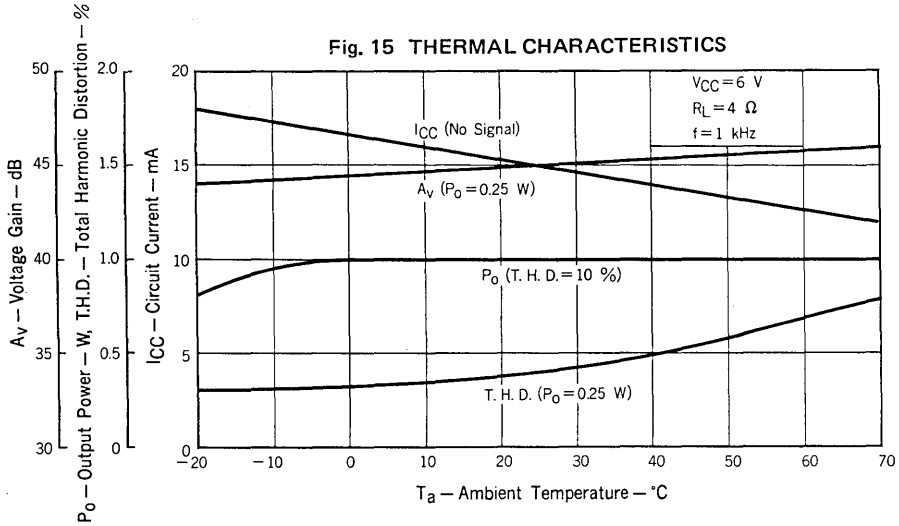


Fig. 16 OPEN LOOP VOLTAGE GAIN, VOLTAGE GAIN vs. SUPPLY VOLTAGE

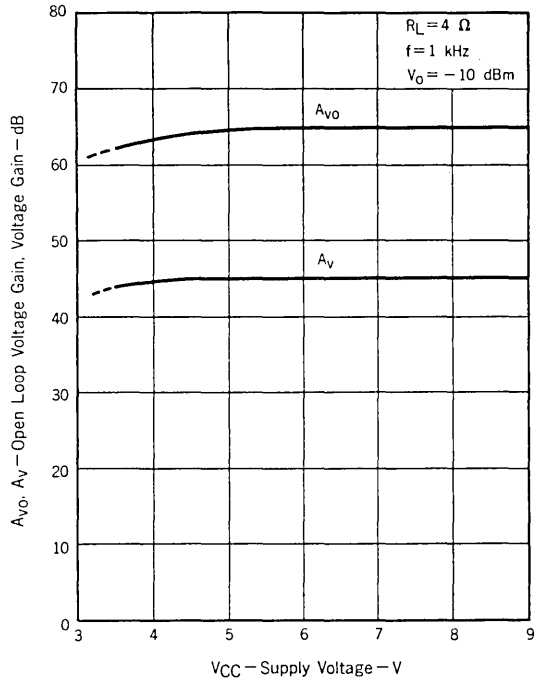


Fig. 17 TOTAL HARMONIC DISTORTION vs. SUPPLY VOLTAGE

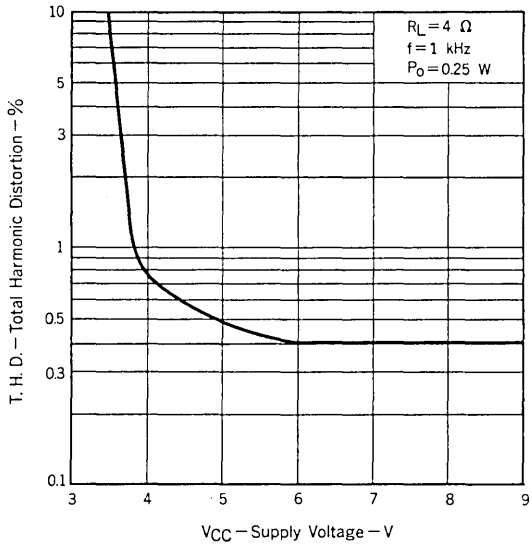
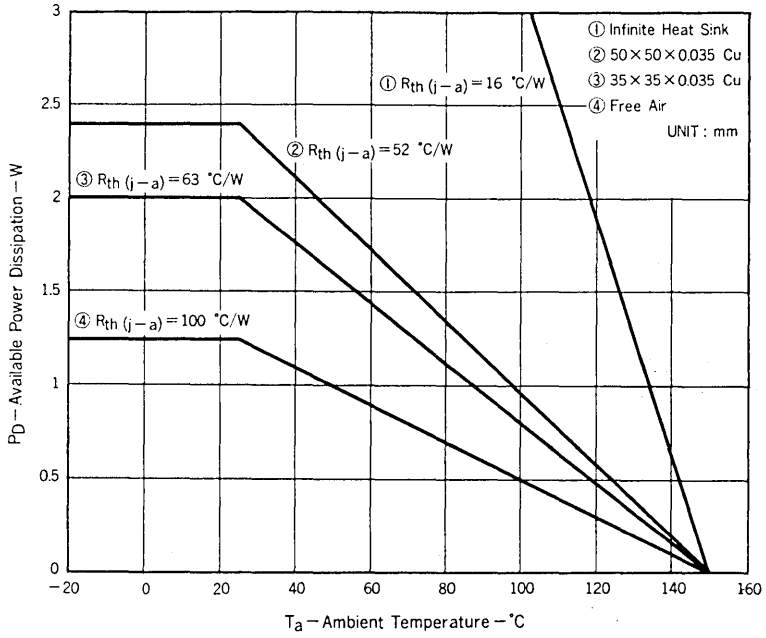


Fig. 18 AVAILABLE POWER DISSIPATION vs. AMBIENT TEMPERATURE



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1213C

AUDIO POWER AMPLIFIR

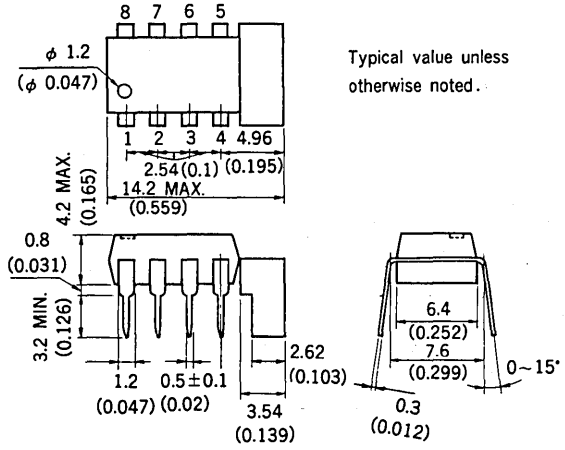
DESCRIPTION

The μPC1213C is a silicon monolithic integrated circuit designed for an audio power amplifier used in a portable radio receiver or a portable cassette tape recorder which works at 9-volt power supply.

The μPC1213C is encapsulated in an 8-pin dual in-line prastic package with a tab.

PACKAGE DIMENSIONS

in millimeters (inches)



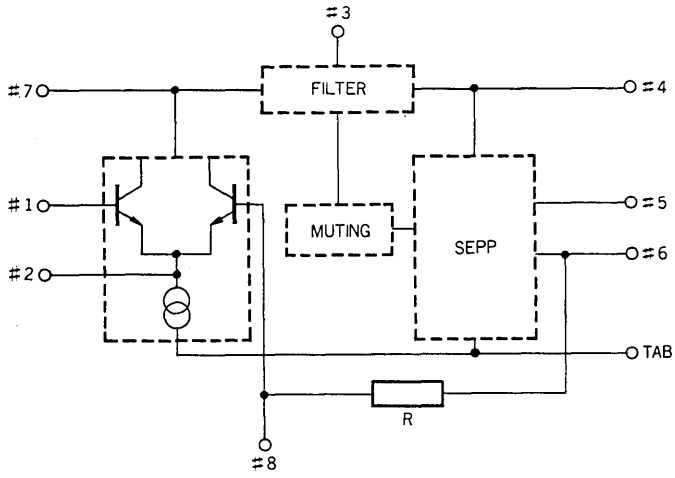
FEATURES

- High output power.
  P_o = 2.4 W (TYP.)
  at V_{CC} = 9 V, R_L = 4 Ω, T.H.D. = 10 %
- Wide operating voltage range.
  V_{CC} = 4.5 to 9 to 11 V
- High ripple rejection ratio.
  R.R.R. = 55 dB (TYP.)
- Soft cripping waveform.
- Have a muting circuit so that no shock noise at power supply switch on and off.
- Have a terminal to reject interference noise in strong electric field. (pin 2)

CONNECTION DIAGRAM

No.	CONNECTION	No.	CONNECTION
1	INPUT	5	BOOTSTRAP
2		6	OUTPUT
3	FILTER	7	FILTER
4	V_{CC}	8	N. F. B.
TAB	GND		

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{CC1}	(No Signal)	16	V
Supply Voltage	V_{CC2}	(Operating)	11	V
Allowable Power Dissipation	P_d	*	2.4	W
Operating Temperature	T_{opt}	−20 to 70		°C
Storage Temperature	T_{stg}	−40 to 150		°C

* 50 x 50 x 0.035 mm copper heat sink on P.C.B.

RECOMMENDED CONDITIONS (T_a = 25 °C)

Supply Voltage	V_{CC} = 4.5 to 9 to 11 V
Load Impedance	R_L = 4 Ω

ELECTRICAL CHARACTERISTICS (T_a=25 °C)

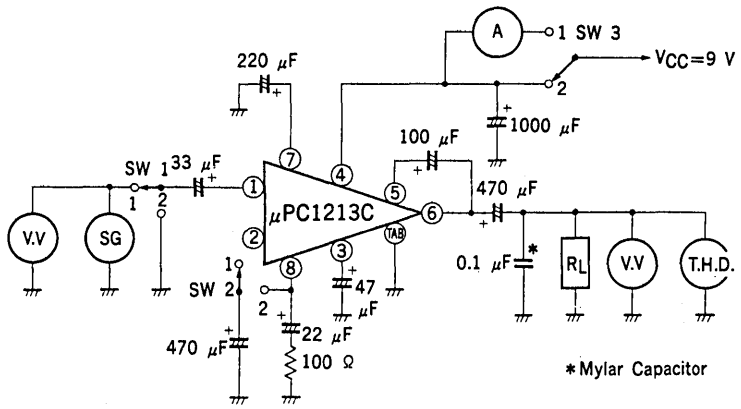
(V_{CC} = 9 V, R = 4Ω, f = 1 kHz, Refer to the test circuit
50 x 50 x 0.035 mm copper heat sink on P.C.B. unless otherwise specified)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Quiscent Circuit Current	I_{CC}	8	15	25	mA	No Signal
Open Loop Voltage Gain	A_{vo}	55	65		dB	P_o=0.25 W
Voltage Gain (Closed Loop)	A_v	41	45	48	dB	R_f=100 Ω
			34			R_f=360 Ω
Output Power	P_o					T.H.D.=10 % R_f=100 Ω
			3.6			V_{CC}=11 V, R_L=4 Ω
			2.2			V_{CC}=11 V, R_L=8 Ω
		1.8	2.4		W	V_{CC}=9 V, R_L=4 Ω
			1.3			V_{CC}=9 V, R_L=8 Ω
			1.0			V_{CC}=6 V, R_L=4 Ω
			0.54			V_{CC}=6 V, R_L=8 Ω
Input Sensitibity	$V_{i(rms)}$					P_o=2.4 W R_L=4 Ω
			19.5			R_f=100 Ω (A_V=45 dB)
			47.3		mV	R_f=360 Ω (A_V=34 dB)
Input Sensitivity	$V_{i(rms)}$					P_o=50 mW R_L=4 Ω
			2.5			R_f=100 Ω (A_V=45 dB)
			8.9		mV	R_f=360 Ω (A_V=34 dB)
Total Harmonic Distortion	T.H.D.		0.4	1.5	%	P_o=0.25 W
Output Noise Voltage	NL		0.2	0.8	$mV_{r.m.s.}$	R_G=0
Supply Voltage Rejection Ratio	S.V.R.	40	55		dB	R_G=0, f_{ripple}=100 Hz V_{ripple}=0.3 $V_{r.m.s.}$
Input Impedance	R_i	10	20		kΩ	

NOTE: In case that only a TYP. value is specified, this specification is for helping to design.

TEST CIRCUIT

Fig. 1 TEST CIRCUIT



SWITCH POSITION

ITEM \ SWITCH		SW1	SW2	SW3
Circuit Current	I_{CC}	2	1	1
Open Loop Voltage Gain	A_{VO}	1	2	2
Voltage Gain	A_V	1	1	2
Output Power	P_O	1	1	2
Total Harmonic Distortion	T.H.D.	1	1	2
Output Noise Voltage	NL	2	1	2

TYPICAL APPLICATION

Fig. 2 SINGLE OPERATION

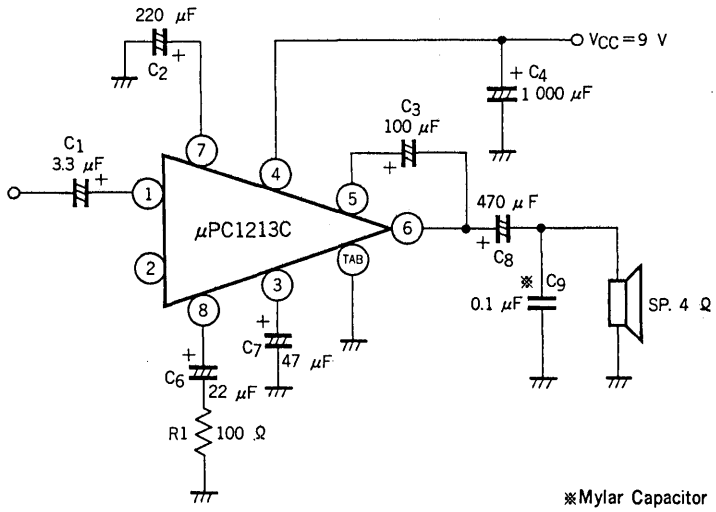
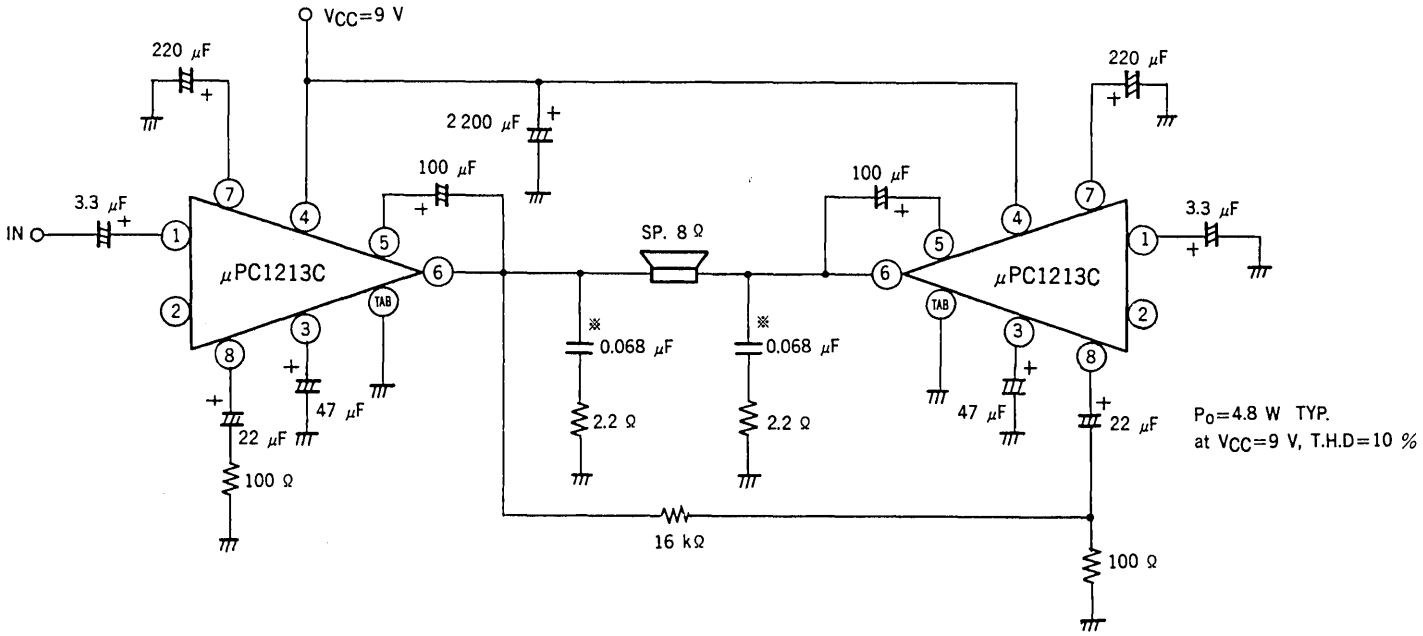
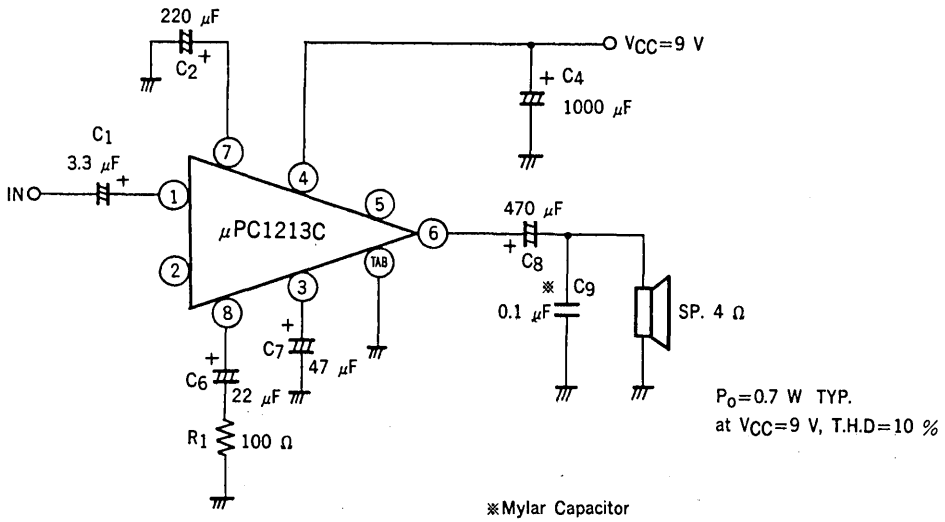


Fig. 3 BTL OPERATION



※Mylar Capacitor

Fig 4 SINGLE OPERATION WITHOUT BOOTSTRAP



※Mylar Capacitor

NOTE FOR USE

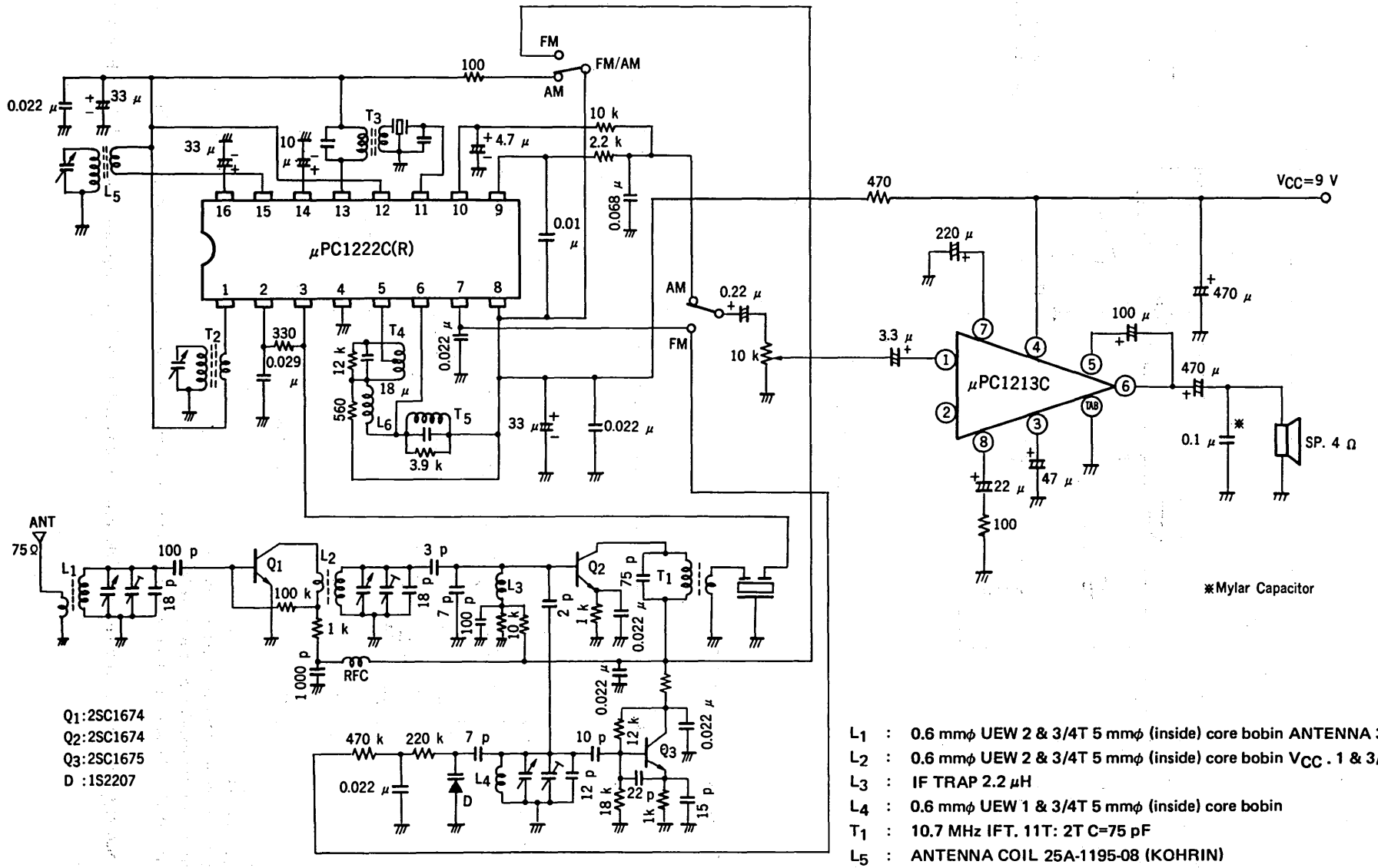
(1) Capacitor C_9 is for preventing the parastic oscillation.
A mylar capacitor is recommended for this position.

(2) The ground side of C_4, C_9 and the loud speaker should be attached at the place of the copper foil close to the tab of μPC1212C.

(3) Interference noise rejection in a strong electric field can be achieved by adding a capacitor (about 1 000 pF) between pin 1 and pin 2.

APPLICATION INFORMATION

Fig. 5 LOW COST FM-AM RADIO WITH 2.4 W OUTPUT POWER (V_{CC} = 9 V)

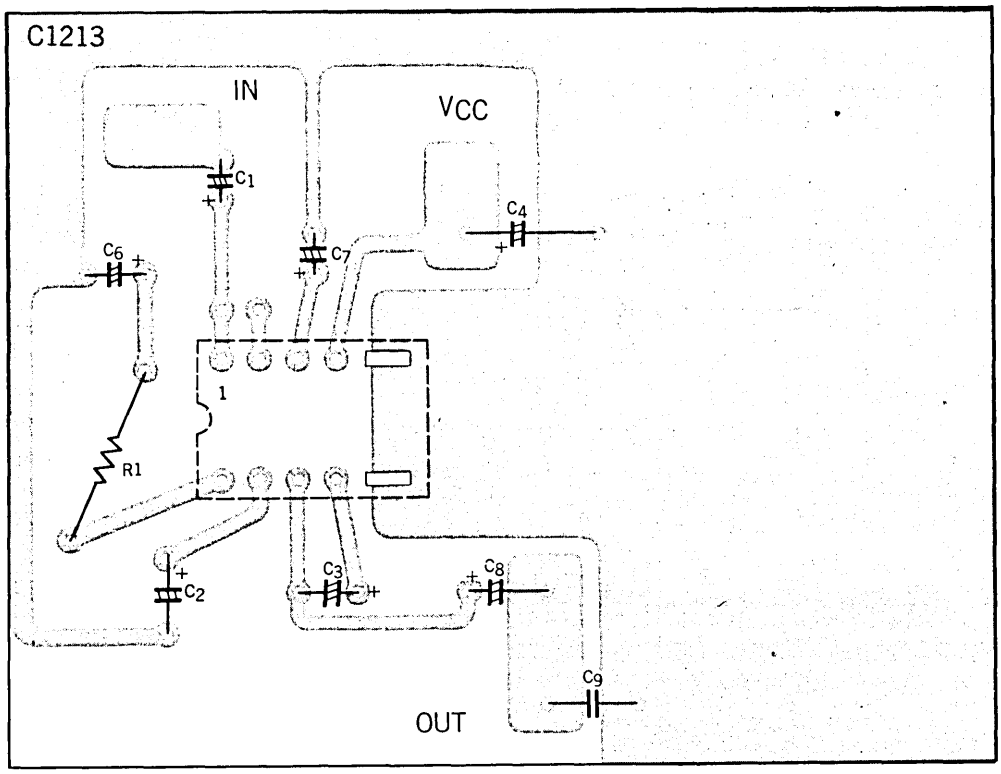


Q1:2SC1674
Q2:2SC1674
Q3:2SC1675
D :1S2207

UNIT : Capacitance F
Resistance Ω

L_1 : 0.6 mmϕ UEW 2 & 3/4T 5 mmϕ (inside) core bobin ANTENNA 3/4T
L_2 : 0.6 mmϕ UEW 2 & 3/4T 5 mmϕ (inside) core bobin V_{CC} . 1 & 3/4T
L_3 : IF TRAP 2.2 μH
L_4 : 0.6 mmϕ UEW 1 & 3/4T 5 mmϕ (inside) core bobin
T_1 : 10.7 MHz IFT. 11T: 2T C=75 pF
L_5 : ANTENNA COIL 25A-1195-08 (KOHRIN)
T_2 : AM OSC 26-1791-13 (KOHRIN)
T_3 : AM IFT CFZ-455C (TOKO)
T_4 : AM DET. 5251 (TOKO)
T_5 : FM DET. 12747 (TOKO)
L_6 : PHASE SHIFT COIL 7BA180JH (TOKO)

P.C. BOARD PATTERN (COPPER SIDE)



TYPICAL CHARACTERISTICS (T_a = 25 °C)

Fig. 6 OUTPUT POWER vs. SUPPLY VOLTAGE

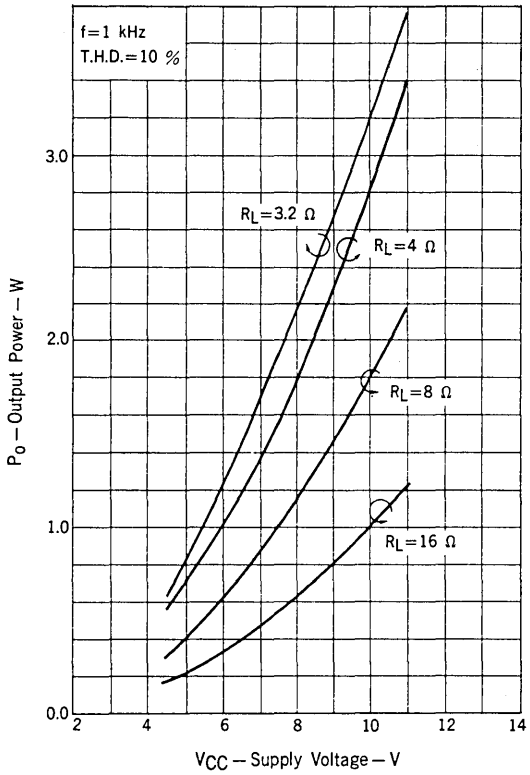


Fig. 7 TOTAL HARMONIC DISTORTION vs. OUTPUT POWER

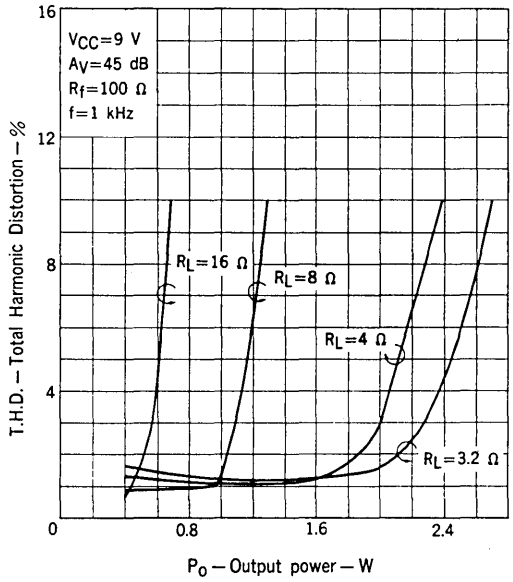


Fig. 8 POWER DISSIPATION AND EFFICIENCY vs. OUTPUT POWER

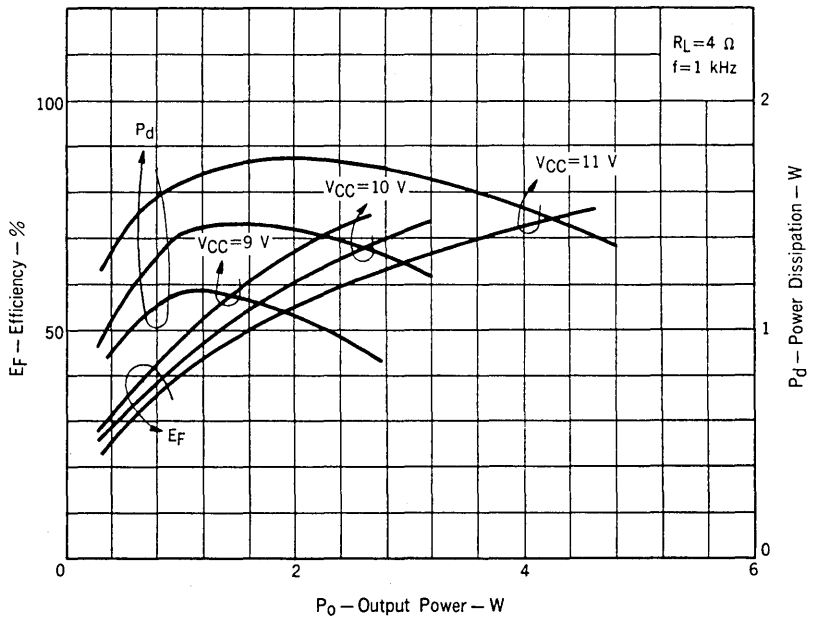


Fig. 9 VOLTAGE GAIN (CLOSED LOOP) vs. R_f

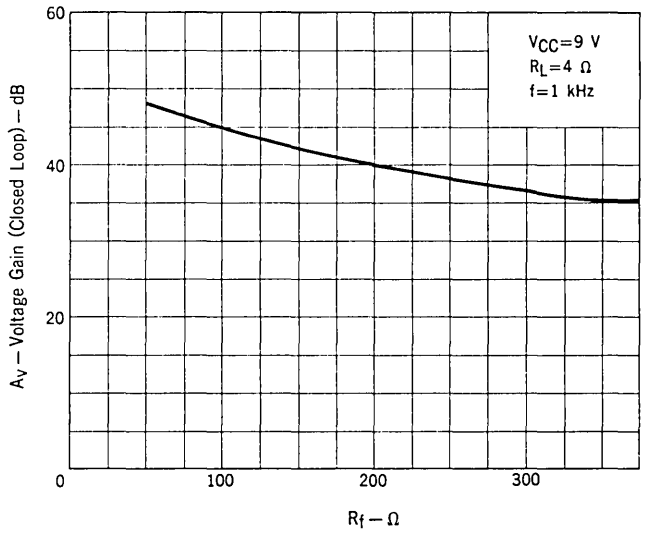


Fig. 10 QUISCENT OUTPUT VOLTAGE AT PIN 6 vs. SUPPLY VOLTAGE

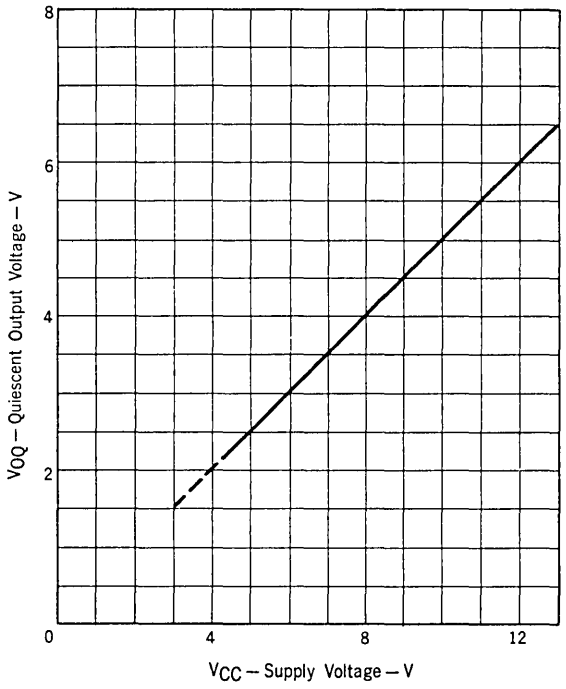


Fig. 11 INPUT SENSITIVITY vs. R_f

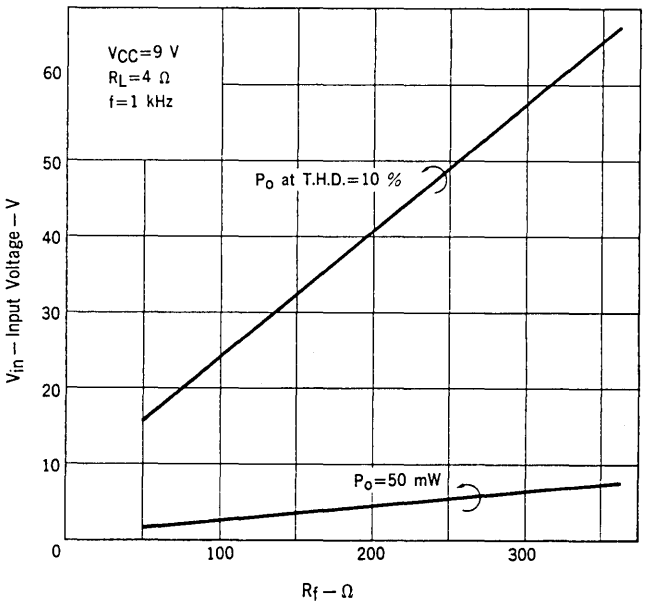


Fig. 12 QUIESCENT CIRCUIT CURRENT vs. SUPPLY VOLTAGE

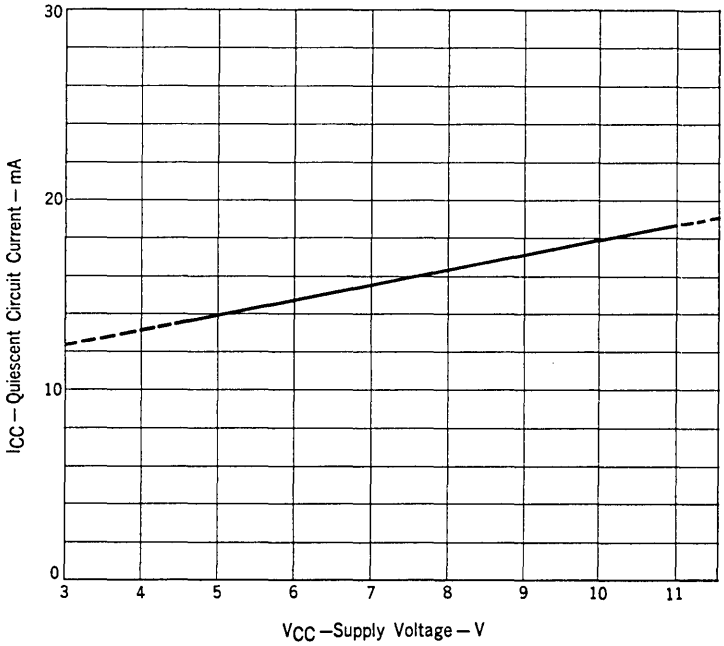


Fig. 13 OPEN LOOP VOLTAGE GAIN, VOLTAGE GAIN vs. FREQUENCY

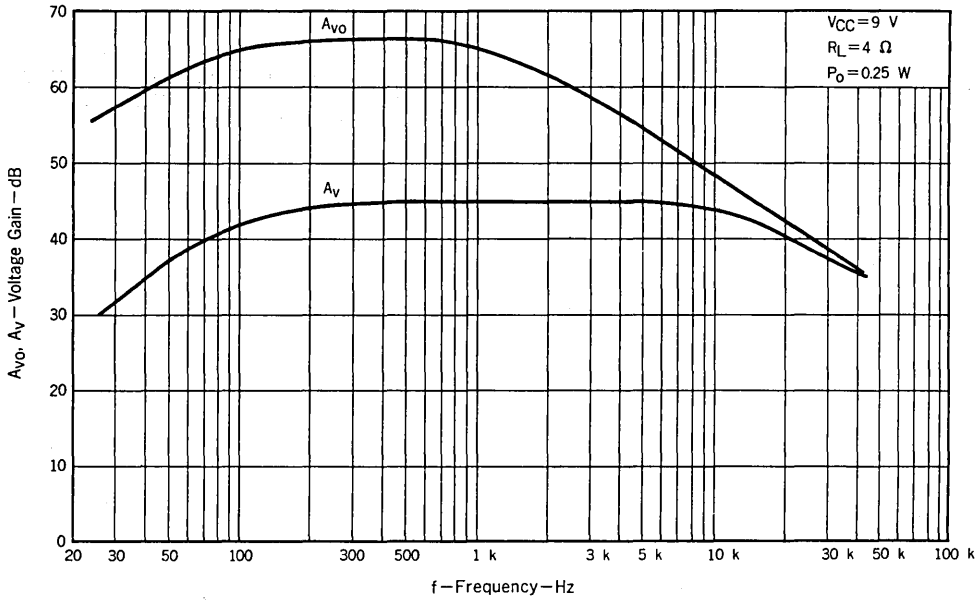


Fig. 14 TOTAL HARMONIC DISTORTION vs. FREQUENCY

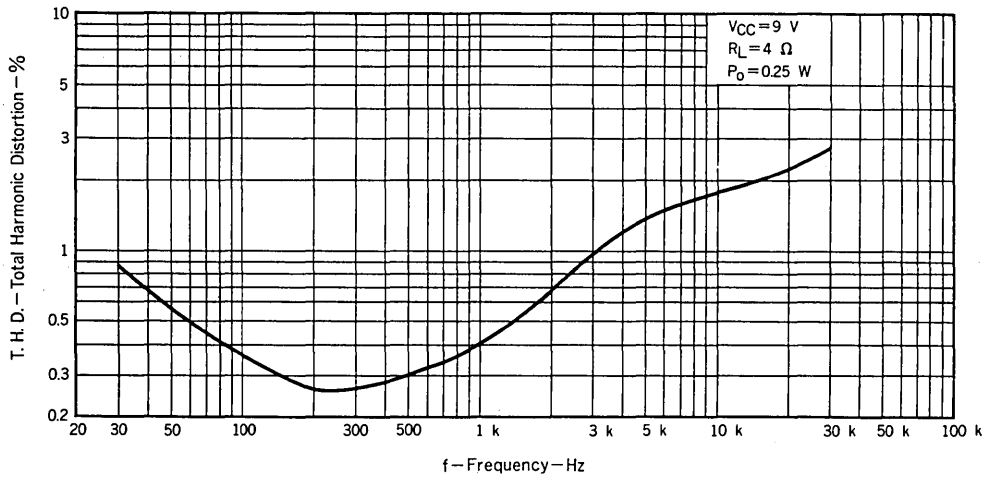


Fig. 15 TOTAL HARMONIC DISTORTION vs. OUTPUT POWER

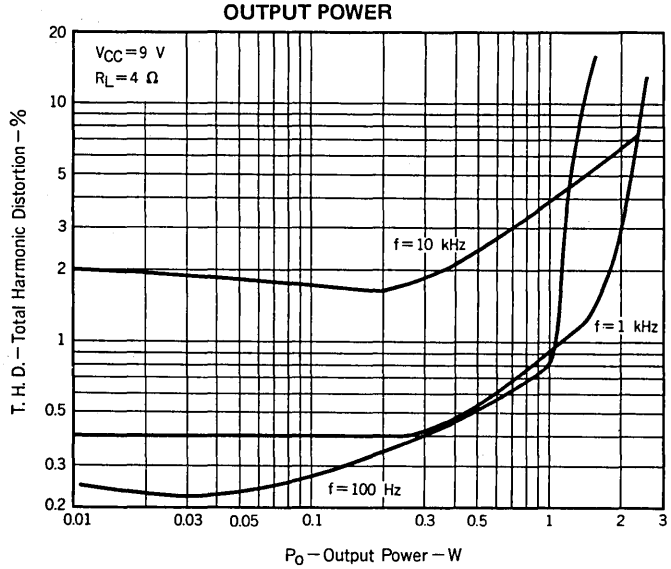


Fig. 16 THERMAL CHARACTERISTICS

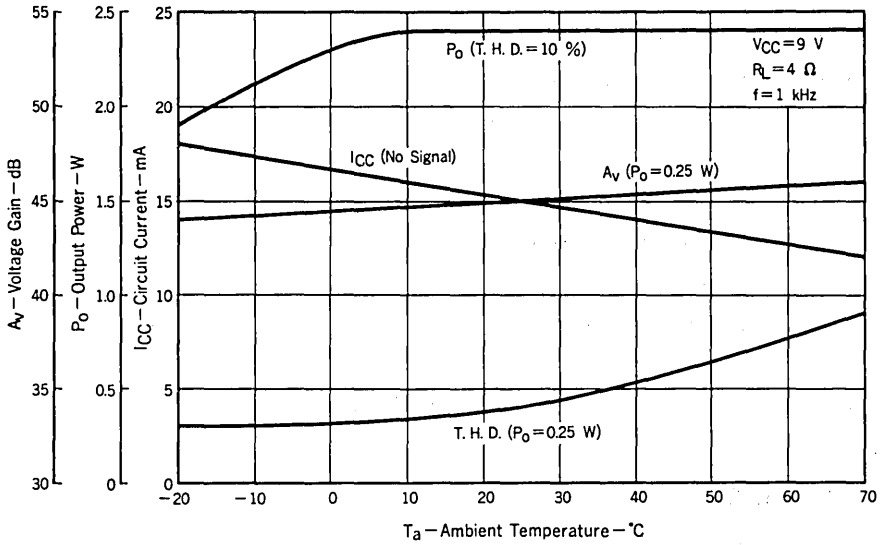


Fig. 17 OPEN LOOP VOLTAGE GAIN, VOLTAGE GAIN vs. SUPPLY VOLTAGE

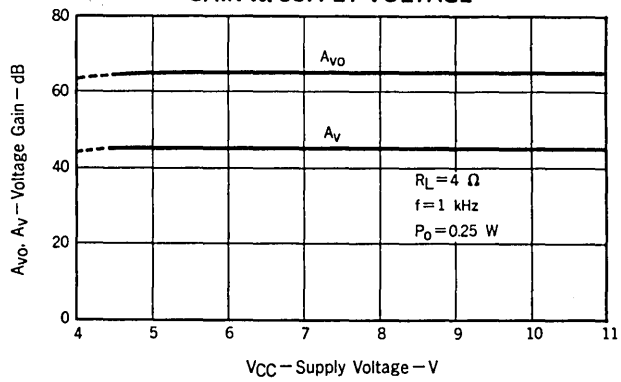
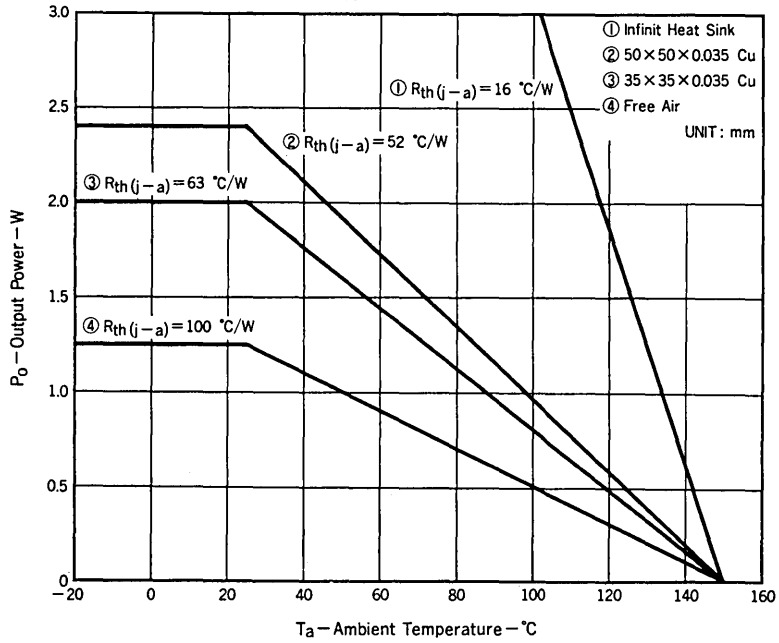


Fig. 18 AVAILABLE POWER DISSIPATION vs. AMBIENT TEMPERATURE



DESIGN OF HEAT SINK

Keep much margin at the design of heat sink.

The heat sink shown the folling sentence is nessesary when the μPC1213C is operated under next conditions.

Conditions : Maximum Operating Voltage 10 V
Maximum Ambient Temperature 70 °C
Load Impedance 4 Ω

There is the equation between junction temperature and thermal resistance.

$$T_j = Ta + R_{th(j-a)} \times P_d \quad (1)$$

T_j : Junction Temperature
Ta : Ambient Temperature
$R_{th(j-a)}$: Thermal Resistance (Junction to Ambient)
P_d : Power Dissipation

According to Fig. 8, P_d(MAX.) = 1.42 W at V_{CC} = 10 V

And absolute maximum rating shows, $T_j < 150$ °C

From the equation (1) and those values,

$$R_{th(j-a)} < 56.3 \text{ °C/W} \quad (2)$$

According to Fig. 18, copper size on P.C.B. satisfying the inequality (2) is 50 x 50 x 0.035 mm.

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1218H

0.25 W AUDIO POWER AMPLIFIER

DESCRIPTION

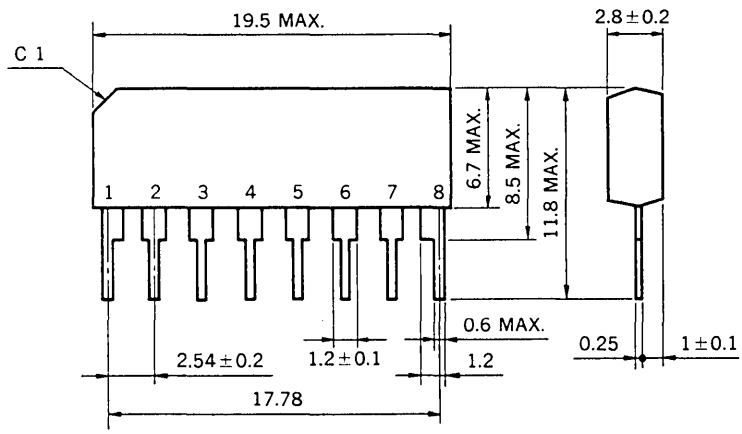
μPC1218H is an audio power amplifier in an 8-pin single in-line plastic package.

μPC1218H is composed a BTL power amplifier and a muting circuit, suitable to a tape recorder works at 3 V power supply.

FEATURES

- High output power. 0.25 W (TYP.) V_{CC} = 3 V, R_L = 8 ohms
- Low voltage operation. V_{CC} = 1.8 to 3 to 5 V
- A muting circuit is built in. Connect pin 7 to GND.
- No shock noise at power supply switch on and off.

PACKAGE DIMENSIONS (Unit : mm)



CONNECTION DIAGRAM

No.	CONNECTION
1	Input
2	NFB
3	High Cut
4	Output 1
5	GND
6	Output 2
7	Filter & Muting
8	V_{CC}

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Supply Voltage	V_{CC}	10	V
Package Dissipation	P_D	830	mW
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

RECOMMENDED OPERATING CONDITION (Ta = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	1.8	3	5	V

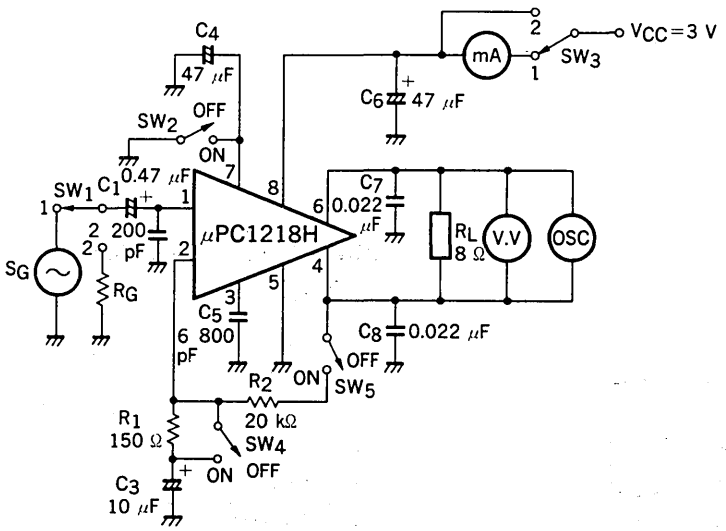
ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

(V_{CC} = 3 V, f = 1 kHz, R_L = 8 Ω, A_V = 45 dB)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Supply Voltage	I_{CC}	(10)	23	(36)	mA	No Signal
Voltage Gain	A_{VO}	(65)	75		dB	P_O = 50 mW
Voltage Gain	A_V		45		dB	P_O = 50 mW
Output Power	P_O	(200)	250		mW	T.H.D. = 10 %
Total Harmonic Distortion	T.H.D.		1.3	(3)	%	P_O = 50 mW
Input Impedance	R_{in}	(10)	17		kΩ	
Output Noise Voltage	NL		0.2	(0.8)	mVr.m.s.	R_g = 2.2 kΩ *
Muting Current	I_M		0.17	(0.6)	mA	Pin 7 : GND

* f = 10 Hz ~ 10 kHz B.P.F. (6 dB/oct)

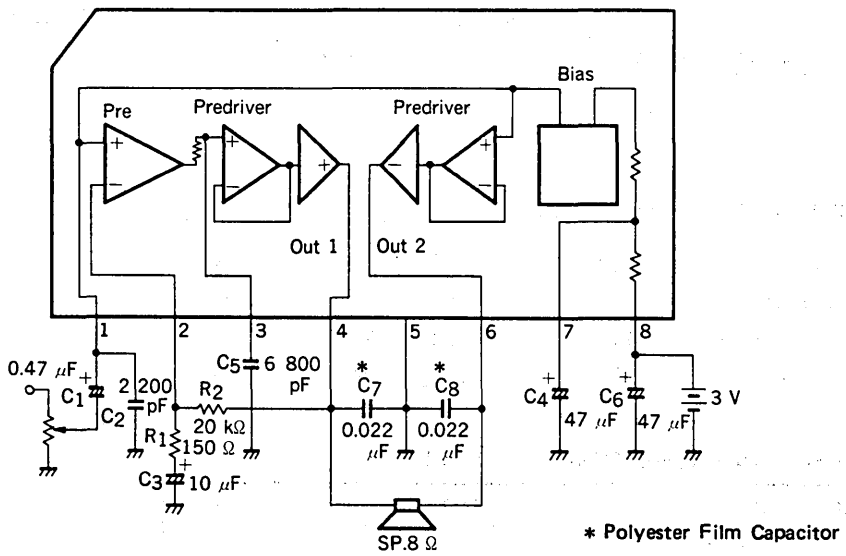
TEST CIRCUIT



SWITCH POSITION

SYMBOL	SW_1	SW_2	SW_3	SW_4	SW_5
I_{CC}	2	OFF	1	OFF	ON
A_{VO}	1	OFF	2	ON	OFF
A_V	1	OFF	2	OFF	ON
P_O	1	OFF	2	OFF	ON
T.H.D.	1	OFF	2	OFF	ON
NL	2	OFF	2	OFF	ON
I_M	2	ON	2	OFF	ON

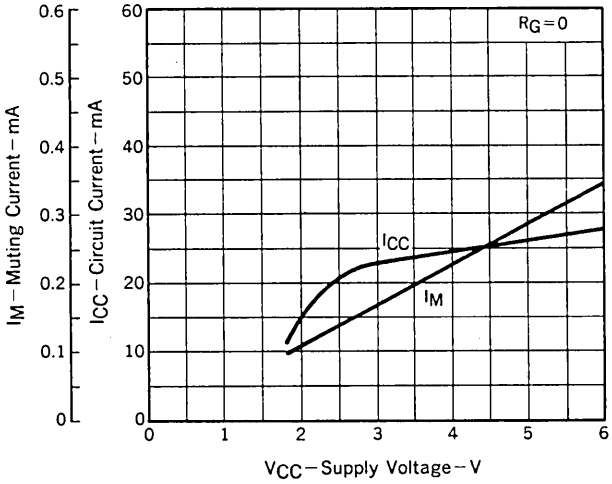
TYPICAL APPLICATION



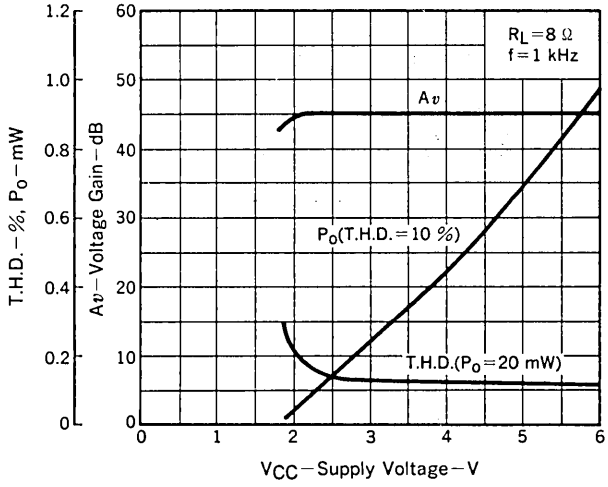
* Polyester Film Capacitor

Note 1) Connect pin #7 to GND in case of keeping μPC1218H mute.
Note 2) Reduce the value of R2 if you want less gain than above.

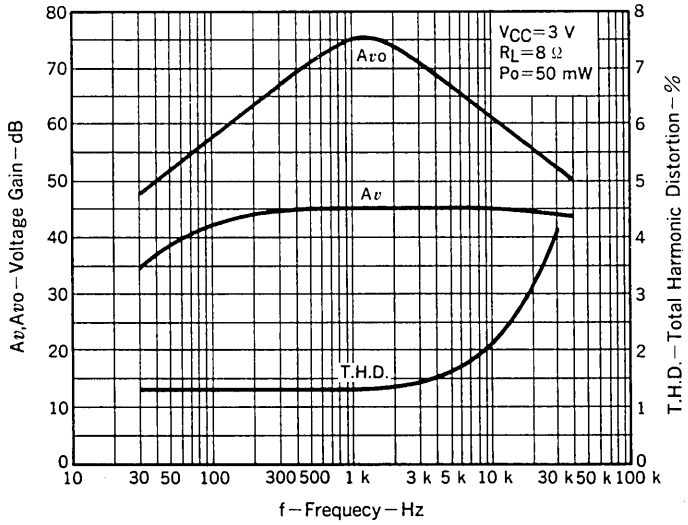
CIRCUIT CURRENT, MUTING CURRENT vs. SUPPLY VOLTAGE



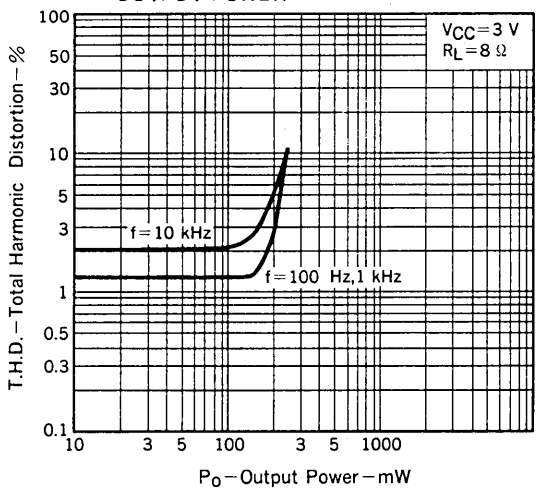
VOLTAGE GAIN, OUTPUT POWER, TOTAL HARMONIC DISTORTION vs. SUPPLY VOLTAGE



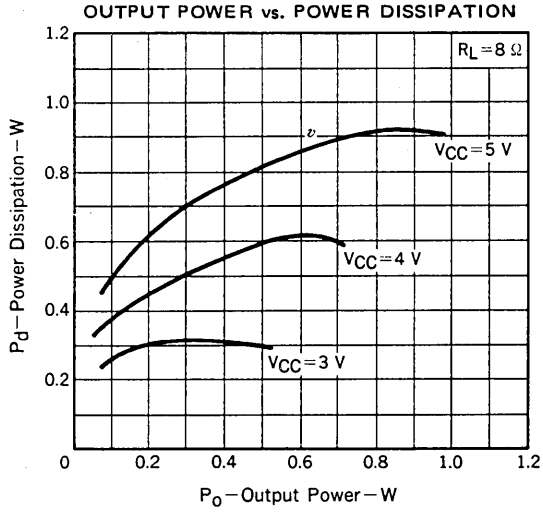
VOLTAGE GAIN vs. FREQUENCY



TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



OUTPUT POWER vs. POWER DISSIPATION



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1221C

1 W AF POWER AMPLIFIER WITH PRE AMPLIFIER AND ALC CIRCUIT SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

DESCRIPTION

The μPC1221C is a silicon monolithic integrated circuit designed for an audio power amplifier application at 6 volts power supply.

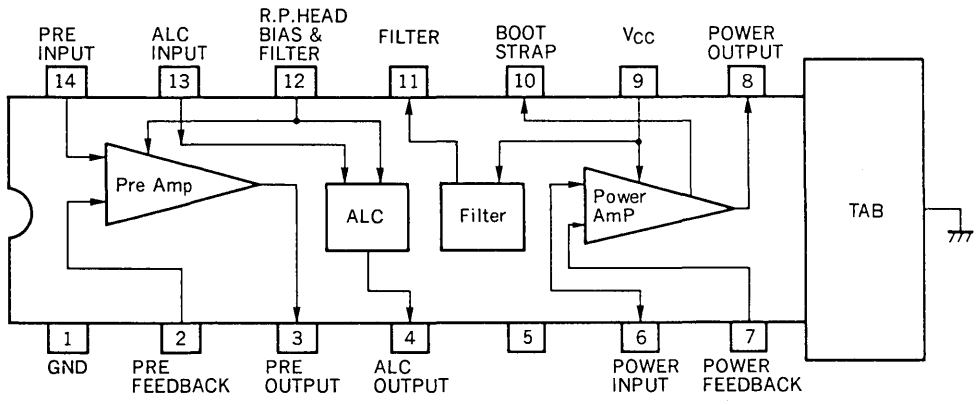
The device contains a high gain low noise preamplifier, an automatic level control (ALC) and a high gain low distortion power amplifier.

The perfect audio circuit of a cassette tape recorder is obtained with the device.

FEATURES

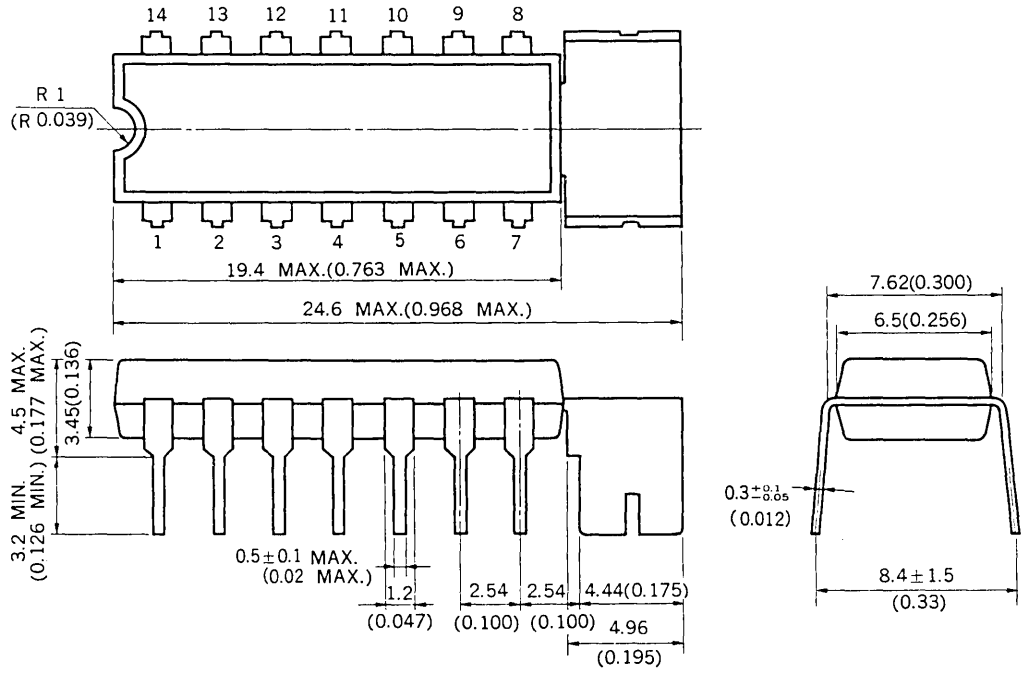
- All functions of a preamplifier, an ALC circuit and a power amplifier are encapsulated in a 14-pins dual in-line package with heat sink TAB.
- Low noise, especially low pulsive noise.
- Power amplifier stage has high gain, high output power and low distortion characteristics.
- Preamplifier stage has high gain and low distortion characteristics.
- Wide ALC range: output voltage change 1.5 dB TYP., ALC range 60 dB TYP.
- Wide supply operating voltage range: V_{CC}=3.5 to 9 V.
- Low spurious radiation when driven to output clipping level.

BLOCK DIAGRAM



PACKAGE DIMENSIONS AND CONNECTION DIAGRAM (Top View)

in millimeters (inches)



Pin No.	ELECTRICAL CONNECTIONS	Pin No.	ELECTRICAL CONNECTIONS
1	GND	8	Power; Output
2	Pre.; Feedback	9	Power Supply V_{CC}
3	Pre.; Output	10	Boot Strap
4	ALC Output	11	Filter
5	※	12	R.P. Head Bias & Filter
6	Power; Input	13	ALC Input
7	Power; Feedback	14	Pre.; Input

※ Pin 5 is terminal to reject radiations in strong electric field.

ABSOLUTE MAXIMUM RATINGS (Ta=25 °C)

Supply Voltage (DC)	V_{CC1}	13	V
Supply Voltage (AC)	V_{CC2}	9	V
Circuit Current	$I_{CC\,(peak)}$	1	A
Package Dissipation	P_D	2.4*	W
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

* Mounted and soldered on a 50 mm x 50 mm copper foil of a printed circuit board (XXX3 grade).

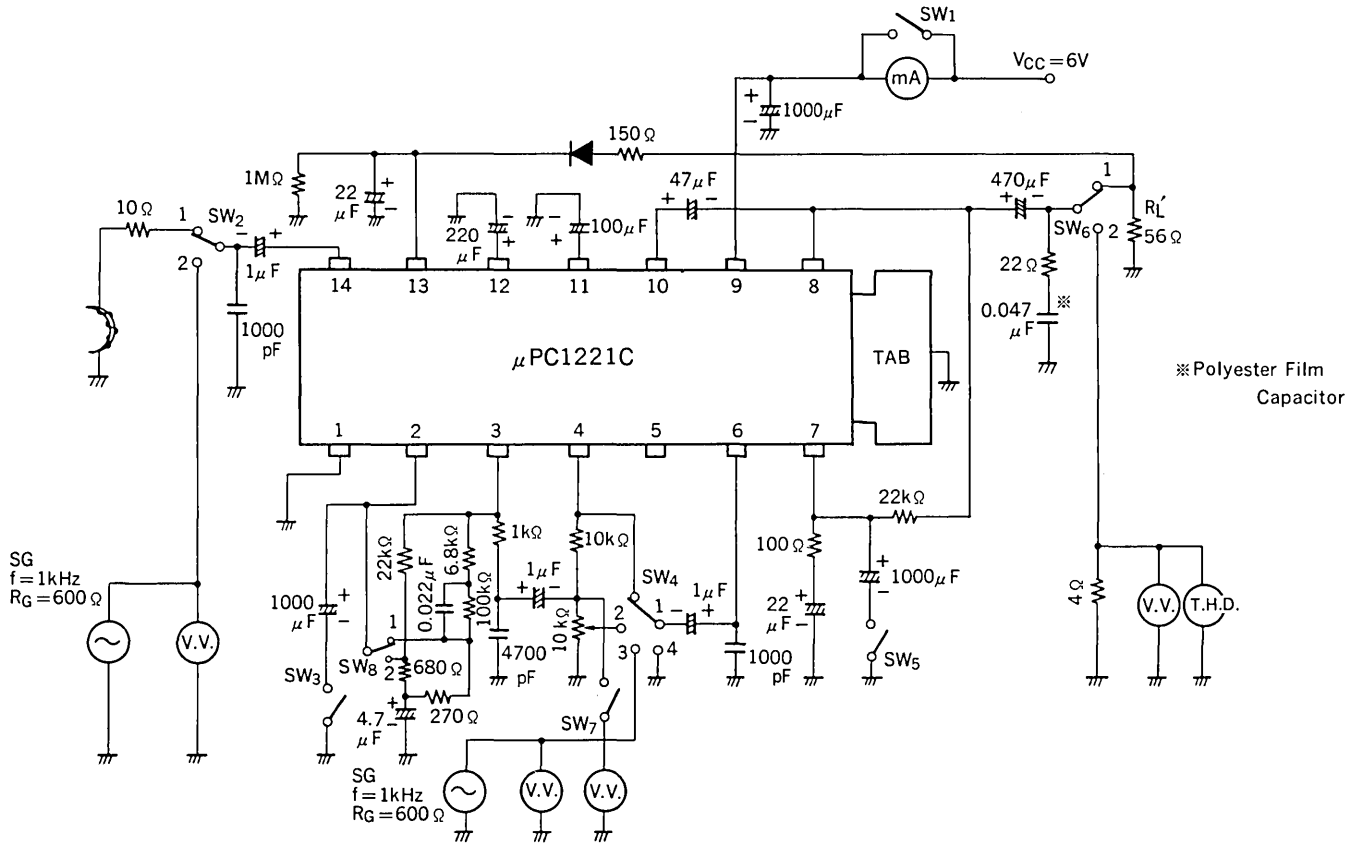
RECOMMENDED OPERATING CONDITIONS (Ta=25 °C)

Operating Supply Voltage	6 V
Supply Voltage Range	3.5 to 9 V

ELECTRICAL CHARACTERISTICS (Ta=25 °C, V_{CC}=6 V, f=1 kHz, NAB, $R_{L\,(pre)}$=10 kΩ, $R_{L(power)}$=4 Ω)

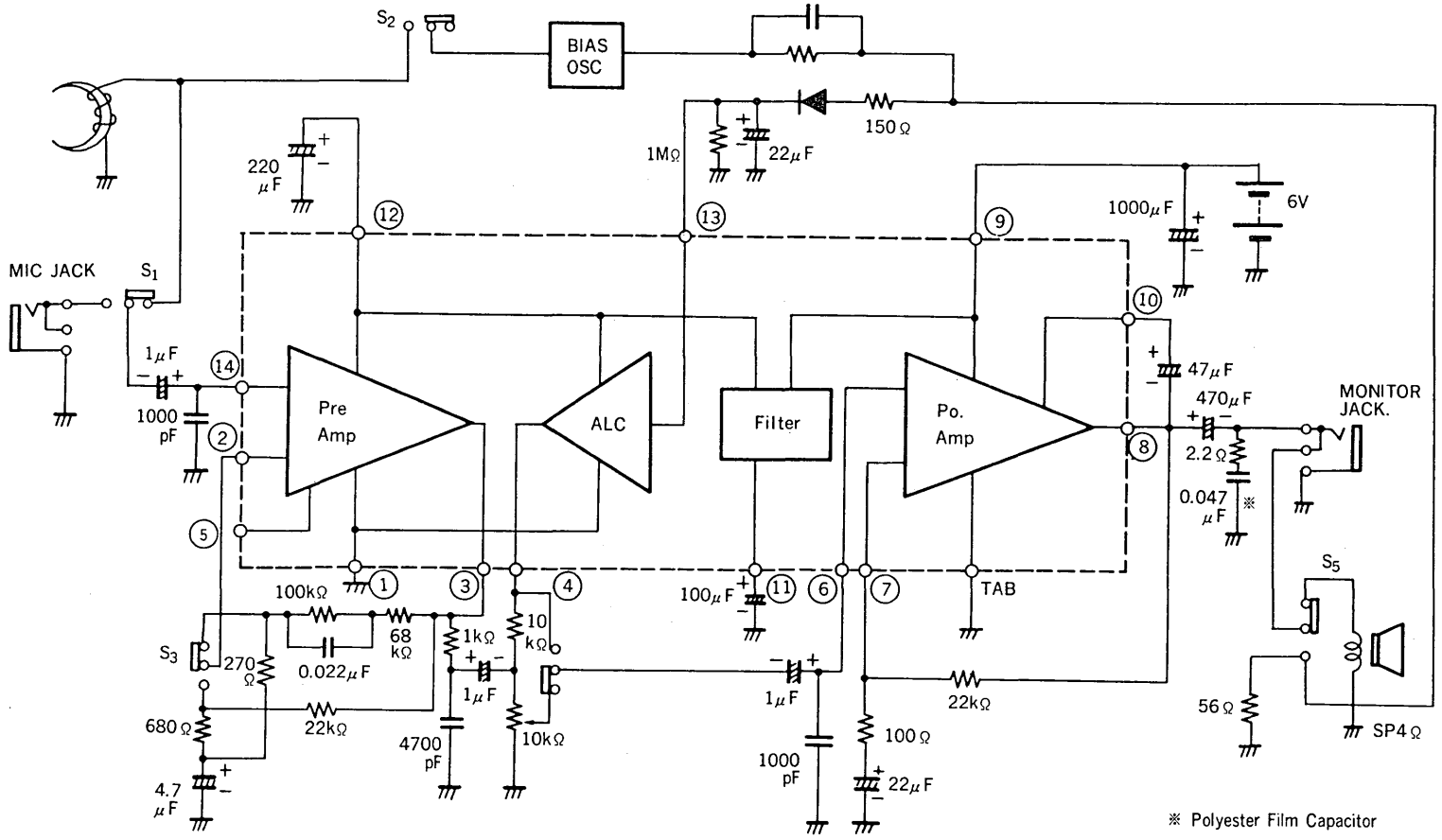
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
[OVER ALL CHARACTERISTIC]						
Circuit Current	I_{CC}	10	25	40	mA	No Signal
Output Power	P_O	0.8	1		W	V_R→MAX. T.H.D.=10 %
Total Harmonic Distortion	T.H.D.		1.0	2.0	%	V_R→MAX. P_O=0.5 W
Output Noise Level	NL_1		9	20	mVr.m.s.	Using P. head as an R_G. V_R→MAX.
ALC Characteristic	ALC_1		1.5	9	dB	V_i=−70~−40 dBm, R_L'=56 Ω
ALC Range	ALC_2		60		dB	T.H.D.≦3 %, R_L'=56 Ω
[PRE AMPLIFIER STAGE]						
Open Loop Voltage Gain	A_{vo1}	55	65		dB	$R_{L(pre)}$=10 kΩ, V_O=0.3 Vr.m.s.
Voltage Gain	A_{v2}		30.8		dB	NAB, V_O=0.3 Vr.m.s.
Maximum Output Voltage	V_{OM}	0.5	0.7		Vr.m.s.	$R_{L(pre)}$=10 kΩ, T.H.D.=1 %
Input Impedance	R_{i1}	18	27		kΩ	
[POWER AMPLIFIER STAGE]						
Open Loop Voltage Gain	A_{vo2}	63	70		dB	P_O=50 mW
Voltage Gain	A_{v2}	44	46		dB	P_O=50 mW
Output Noise Level	NL_2		0.4	2.0	mVr.m.s.	V_R→MIN. (R_G=0)
Ripple Rejection Ratio	R.R.R.	40	50		dB	R_G=0
Input Impedance	R_{i2}	15	25		kΩ	

TEST CIRCUIT



ITEM		SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
ALL	I_{CC}	OFF	1	OFF	2	OFF	2	OFF	1
	Po	ON	2	OFF	2	OFF	2	OFF	1
	T.H.D.	ON	2	OFF	2	OFF	2	OFF	1
	N_L	ON	1	OFF	2	OFF	2	OFF	1
	ALC	ON	2	OFF	1	OFF	1	OFF	1
PRE	A_{vo}	ON	2	ON	4	OFF	2	ON	2
	A_v	ON	2	OFF	4	OFF	2	ON	2
	v_{om}	ON	2	OFF	4	OFF	2	ON	2
POWER	A_{vo}	ON	1	OFF	3	ON	2	OFF	2
	A_v	ON	1	OFF	3	OFF	2	OFF	2
	N_L	ON	1	OFF	4	OFF	2	OFF	2
	R.R.R.	ON	1	OFF	4	OFF	2	OFF	2

μPC1221C TYPICAL APPLICATION

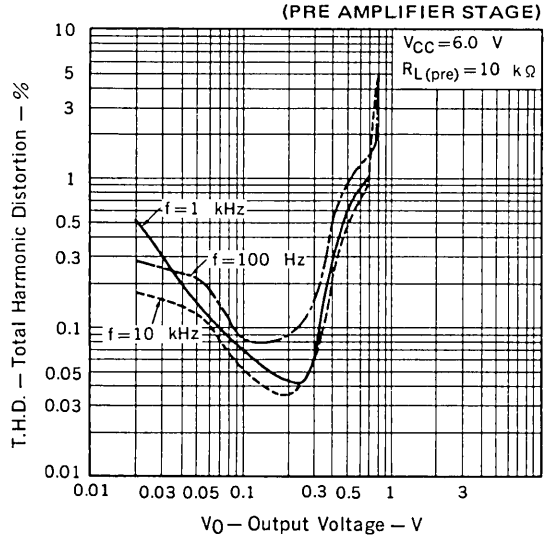


Insurt a capacitor (about 1000 pF) between pin 5 and pin 14 when the μPC1221C is affected by radiations in strong electric field.

CHARACTERISTICS

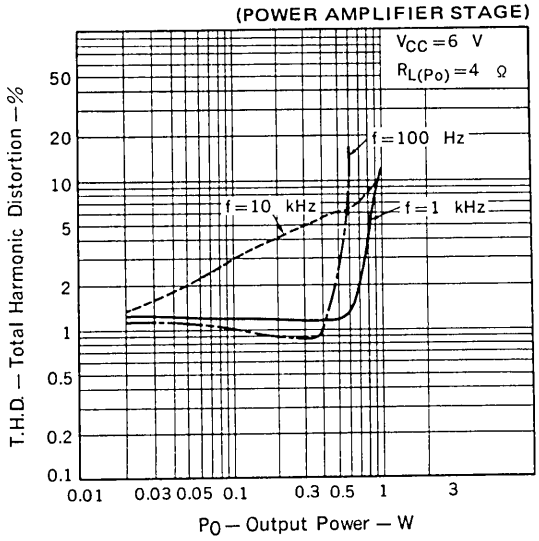
TOTAL HARMONIC DISTORTION vs. OUTPUT VOLTAGE

(PRE AMPLIFIER STAGE)



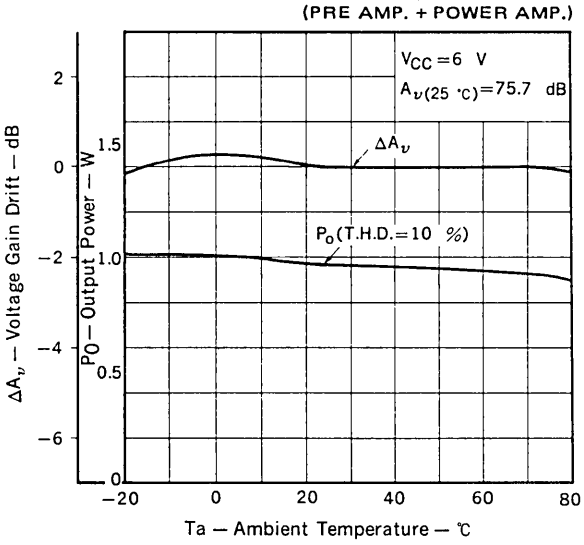
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER

(POWER AMPLIFIER STAGE)



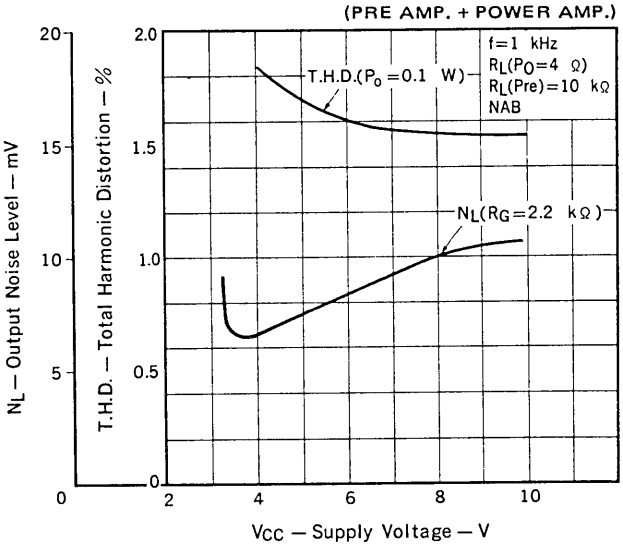
OUTPUT POWER, OUTPUT VOLTAGE GAIN vs. AMBIENT TEMPERATURE

(PRE AMP. + POWER AMP.)

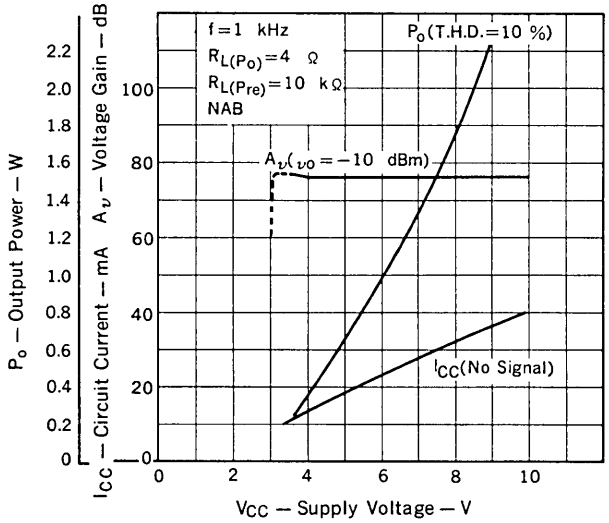


OUTPUT NOISE LEVEL, TOTAL HARMONIC DISTORTION vs. SUPPLY VOLTAGE

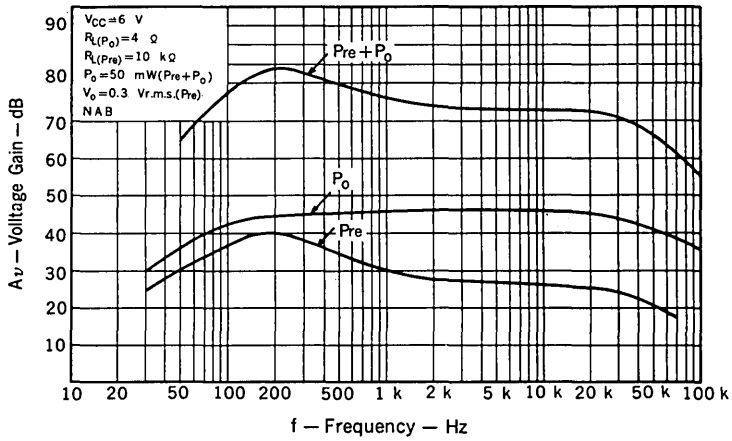
(PRE AMP. + POWER AMP.)



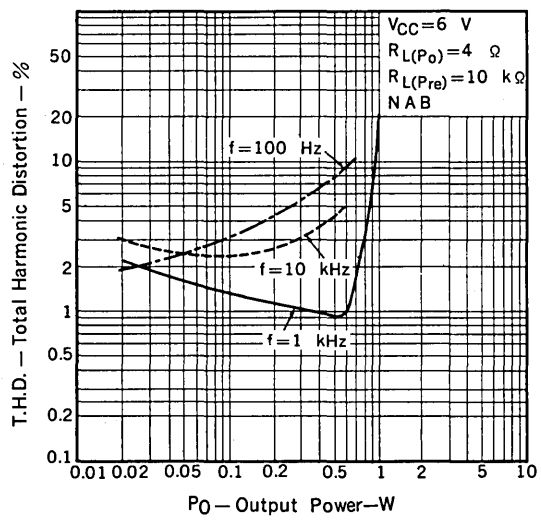
CIRCUIT CURRENT, OVER ALL VOLTAGE GAIN, OUTPUT POWER, MAXIMUM OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



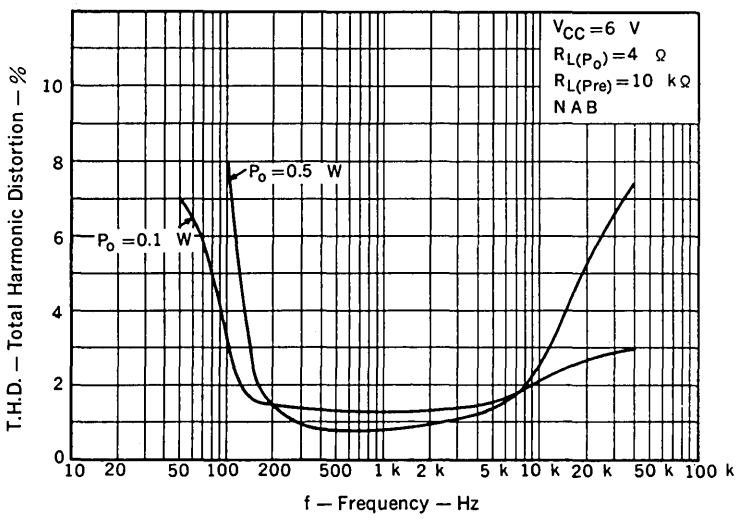
VOLTAGE GAIN vs. FREQUENCY



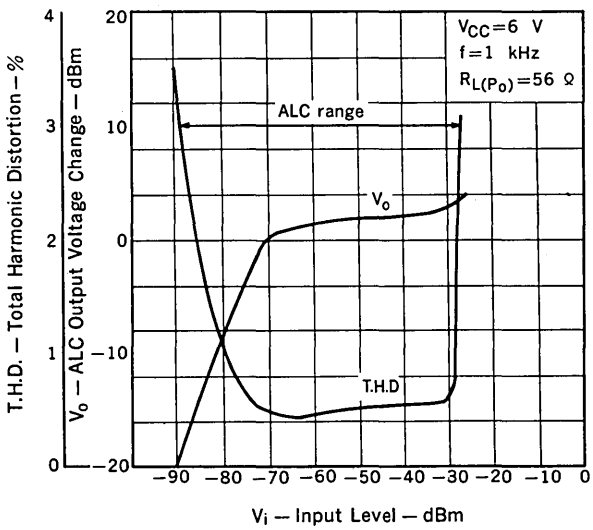
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER (PRE AMP. + POWER AMP.)



TOTAL HARMONIC DISTORTION vs. FREQUENCY (PRE AMP. + POWER AMP.)



T.H.D., ALC OUTPUT VOLTAGE CHANGE vs. INPUT LEVEL



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1263C2

DUAL AUDIO POWER AMPLIFIER

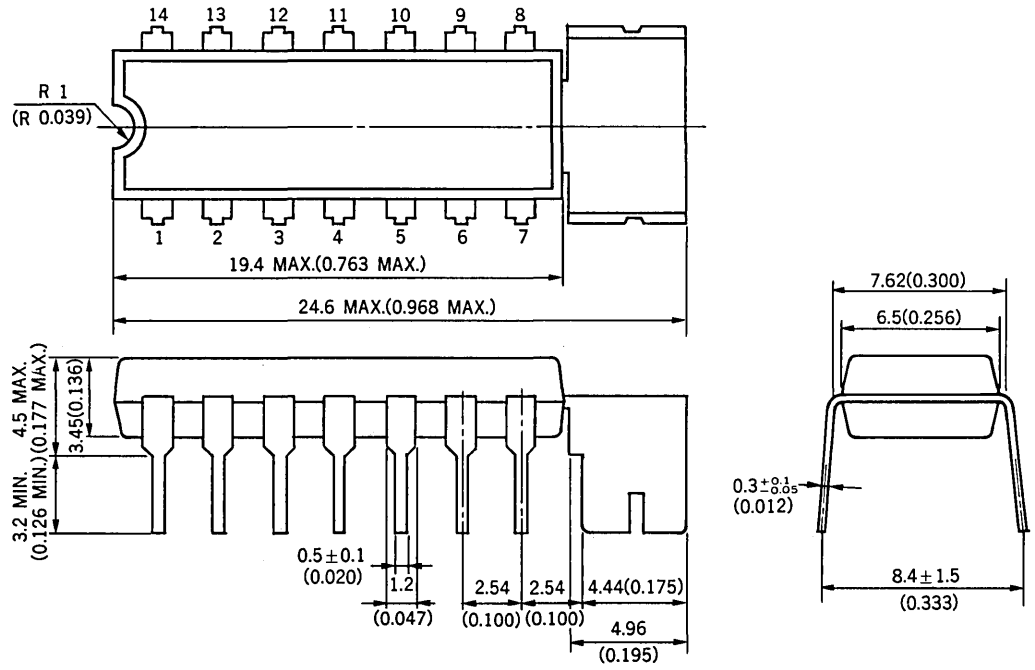
DESCRIPTION

The μPC1263C2 is a dual audio power amplifier in a 14-lead dual in line plastic package, and designed for portable audio sets.

FEATURES

- Wide operating voltage range. V_{CC} = 3 to 16 V
- High output power. P_o = 2 W at 12 V / 8 Ω / 10 %
  P_o = 1.6 W at 9 V / 4 Ω / 10 %
  P_o = 1.2 W at 9 V / 8 Ω / 10 %
  P_o = 0.7 W at 6 V / 4 Ω / 10 %
  P_o = 0.5 W at 6 V / 8 Ω / 10 %
  P_o = 50 mW at 4.5 V / 32 Ω / 10 %
  (V_{CC} / R_L / T.H.D.)
- High ripple rejection ratio. R.R.R. = 50 dB
- Low quiescent current. I_{CC} = 10 mA
- Easy assembly so that two power amplifiers are built in a package.

PACKAGE DIMENSIONS in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

ITEM	SYMBOL	RATING	UNIT
Supply Voltage (No Signal)	V_{CC1}	18	V
Supply Voltage (Operating)	V_{CC2}	16	V
Allowable Power Dissipation	P_D	2.4 *	W
Operating Temperature	T_{opt}	−20 to 70	°C
Storage Temperature	T_{stg}	−40 to 150	°C

* 50 X 50 X 0.035 mm Copper heat sink on PCB.

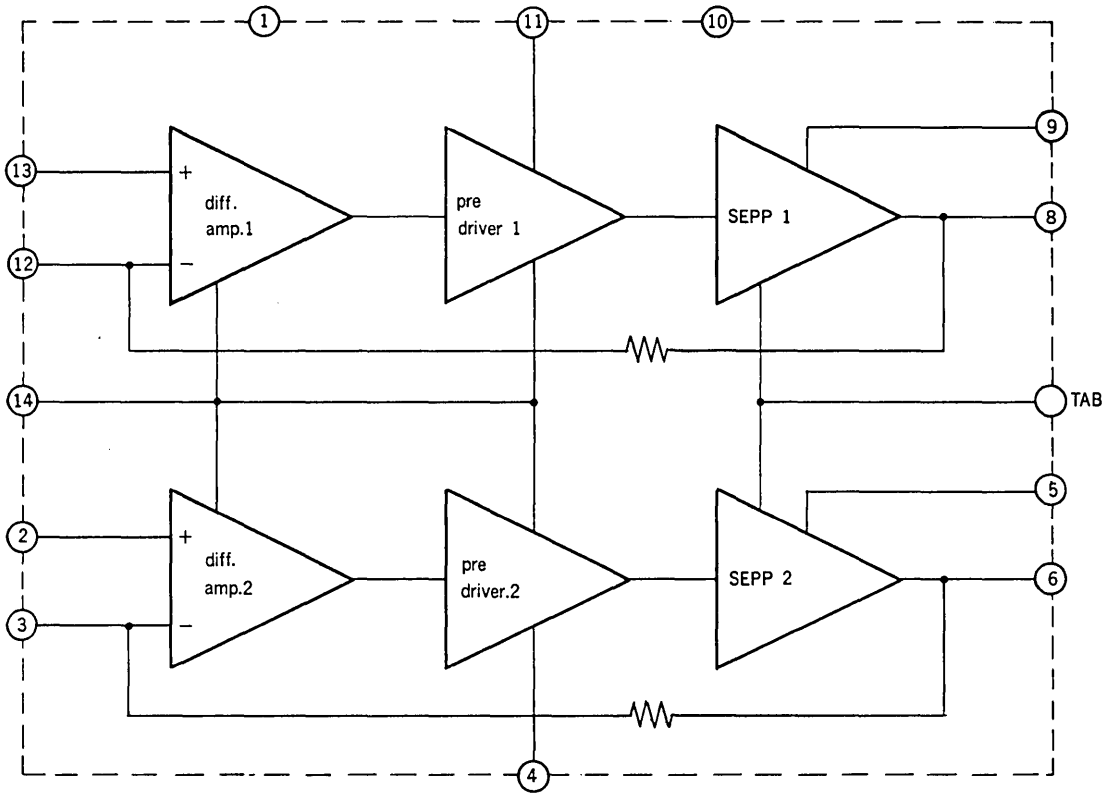
RECOMMENDED OPERATING CONDITIONS (T_a = 25 °C)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage (R_L=16 Ω)	V_{CC} (16)	3		16	V
Supply Voltage (R_L=8 Ω)	V_{CC} (8)	3		13	V
Supply Voltage (R_L=4 Ω)	V_{CC} (4)	3		9	V
Load Impedance	R_L	4	8		Ω
Voltage Gain	G_v	34	44		dB

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)
(V_{CC}=9 V, R_f=33 Ω, f=1 kHz, R_L=8 Ω)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Circuit Current	I_{CC}		10		mA	No Signal
Voltage Gain	G_v1		44		dB	P_o=0.25 W, R_f=33 Ω
	G_v2		34		dB	P_o=0.25 W, R_f=120 Ω
Output Power	P_o1		2		W	V_{CC}=12 V, R_L=8 Ω, T.H.D.=10 %
	P_o2		1.6		W	V_{CC}=9 V, R_L=4 Ω, T.H.D.=10 %
	P_o3	0.9	1.2		W	V_{CC}=9 V, R_L=8 Ω, T.H.D.=10 %
	P_o4		0.7		W	V_{CC}=6 V, R_L=4 Ω, T.H.D.=10 %
	P_o5		0.5		W	V_{CC}=6 V, R_L=8 Ω, T.H.D.=10 %
	P_o6		50		mW	V_{CC}=4.5 V, R_L=32 Ω, T.H.D. = 10%
Total Harmonic Distortion	T.H.D.1		0.8		%	P_o=0.5 W, R_f=33 Ω
	T.H.D.2		0.4		%	P_o=0.5 W, R_f=120 Ω
Output Noise Voltage	NL		0.6		$mV_{r.m.s.}$	R_G=10 kΩ
Ripple Rejection Ratio	R.R.R.		50		dB	R_G=0, f(ripple)=100 Hz, V(ripple)=0.3 $V_{r.m.s.}$
Cross Talk	C.T.		55		dB	R_G=0, P_o=0.25 W
Channel Balance	Ch.B.	−2	0	2	dB	P_o=0.25 W
Input Impedance	Z_{in}		5		MΩ	

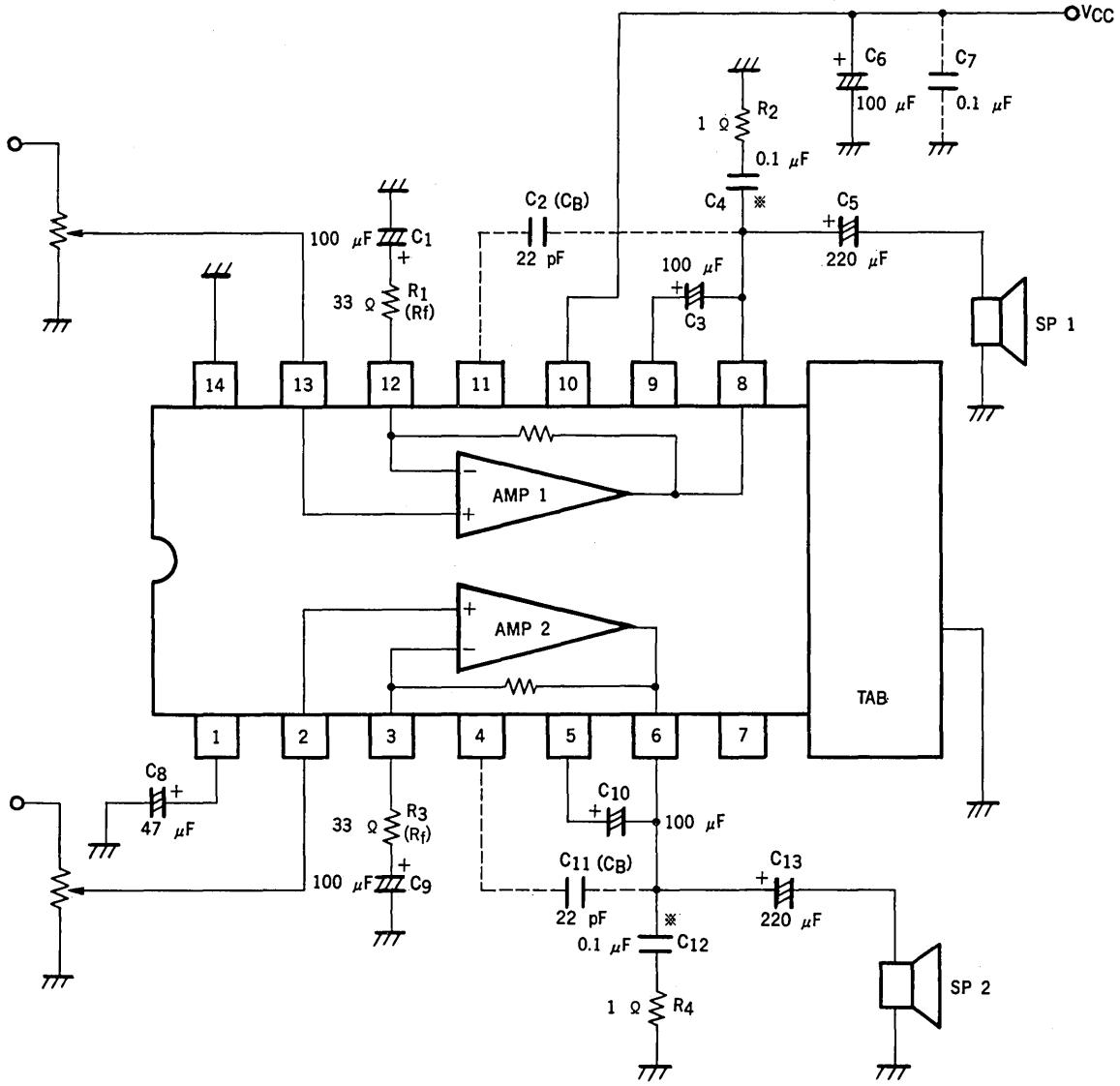
BLOCK DIAGRAM



CONNECTION DIAGRAM

PIN NO.	CONNECTION	PIN NO.	CONNECTION
1	Filter	8	Output 1
2	Input 2	9	Bootstrap 1
3	NFB 2	10	V_{CC}
4	Compensation 2	11	Compensation 1
5	Bootstrap 2	12	NFB 1
6	Output 2	13	Input 1
7	NC	14	GND
TAB	GND		

TYPICAL APPLICATION



※Mylar Capacitor

NOTE FOR USE

(1) Mylar capacitor is recommended as C_4, C_{12}.

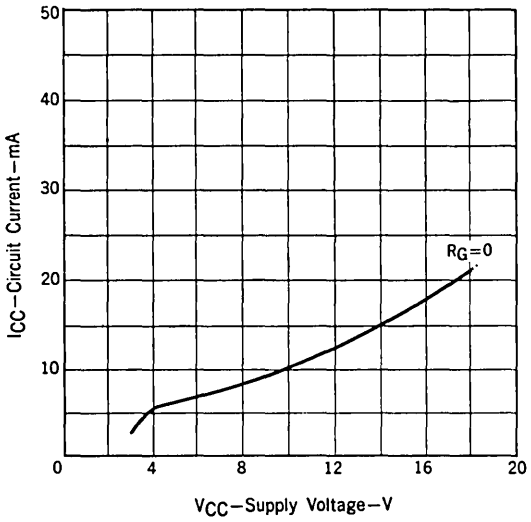
(2) Add C_2, C_{11}, in the case of reducing voltage gain at high frequency.

(3) Add C_7 or increase capacitance of C_4, C_{12}, when a oscillation may occur due to the pattern on PCB.

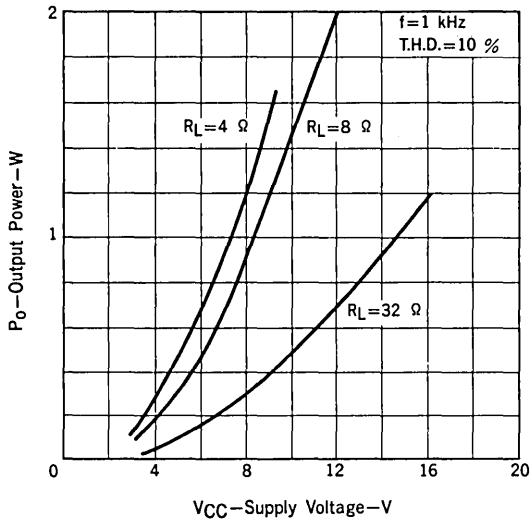
(4) Voltage gain can be changed by value of R_1, R_3.

TYPICAL CHARACTERISTICS (T_a = 25 °C)

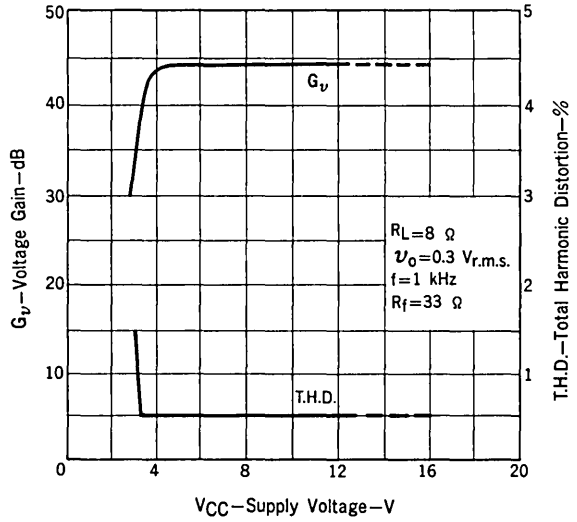
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



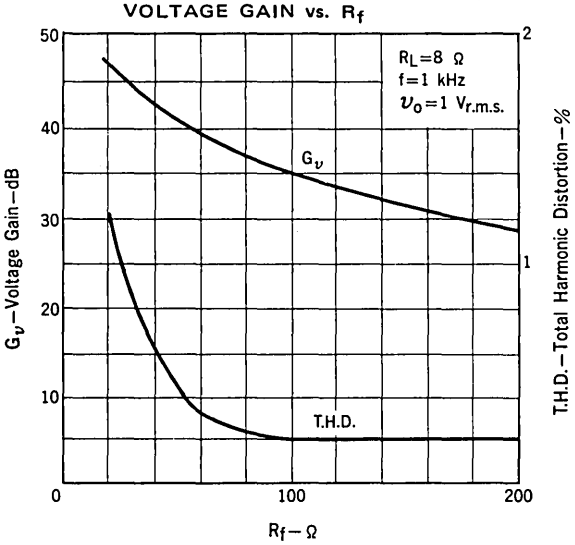
OUTPUT POWER vs. SUPPLY VOLTAGE



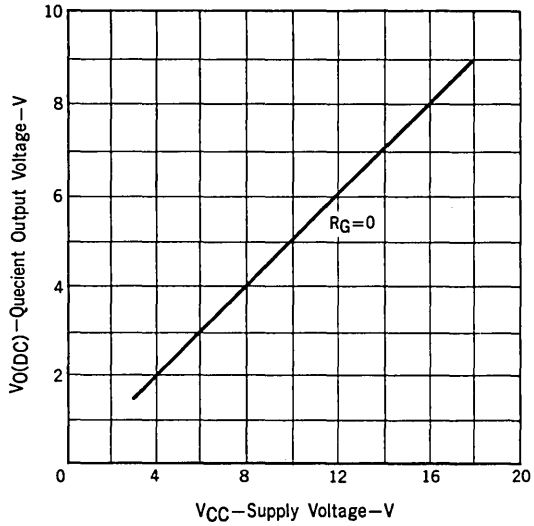
VOLTAGE GAIN vs. SUPPLY VOLTAGE, TOTAL HARMONIC DISTORTION



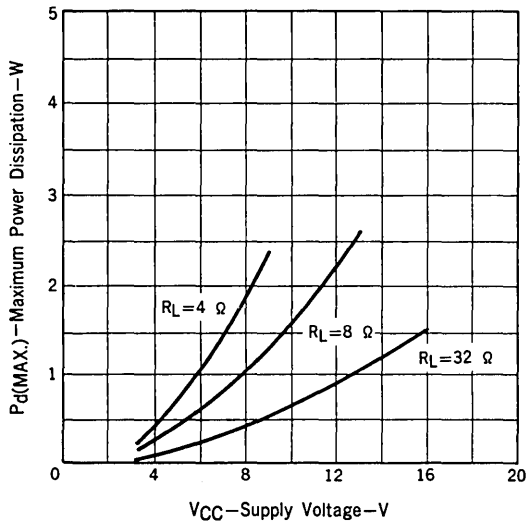
TOTAL HARMONIC DISTORTION, VOLTAGE GAIN vs. R_f



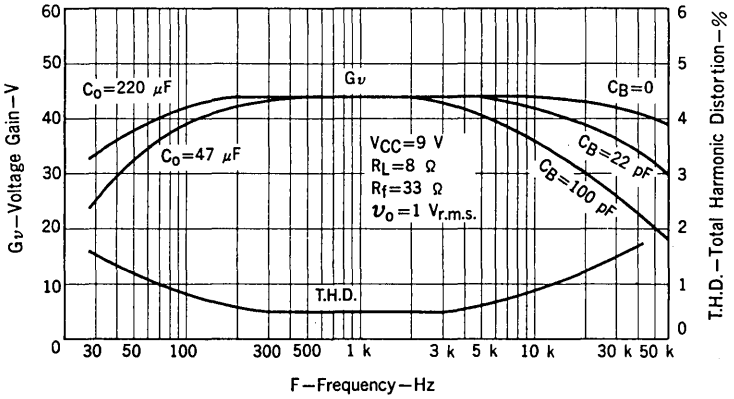
QUECIENT OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



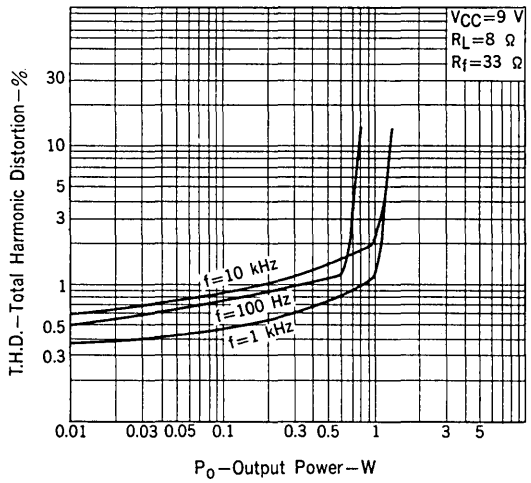
MAXIMUM POWER DISSIPATION vs. SUPPLY VOLTAGE



VOLTAGE GAIN, TOTAL HARMONIC DISTORTION vs. FREQUENCY



TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



PACKAGE DISSIPATION vs. AMBIENT TEMPERATURE

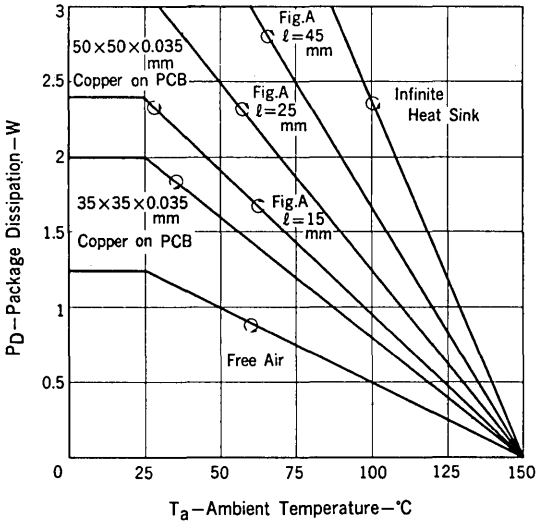
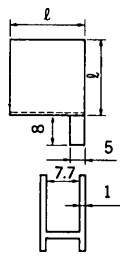


Fig.A



UNIT: mm

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1277H

4.2 W DUAL AUDIO POWER AMPLIFIER

DESCRIPTION

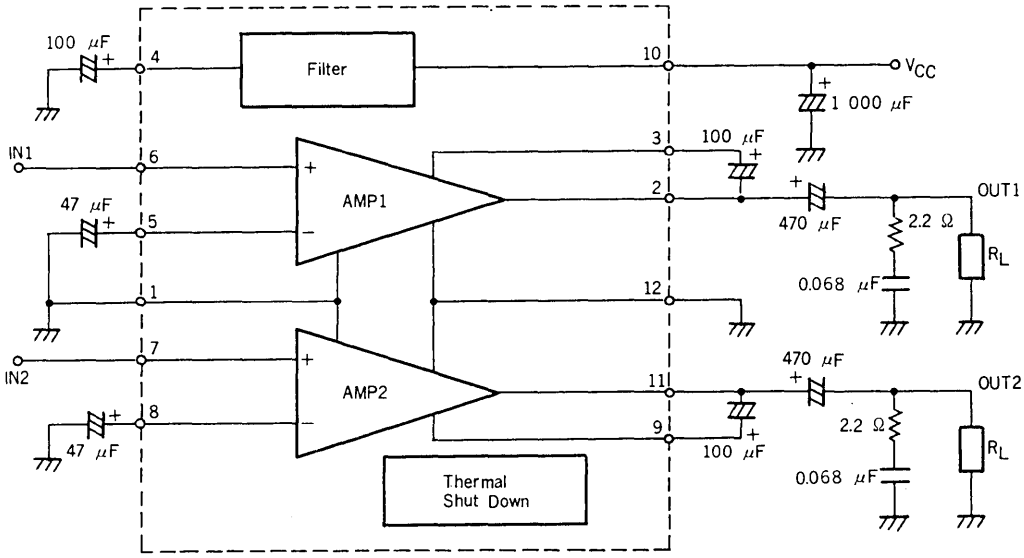
The μPC1277H is a dual audio power amplifier designed for a stereo radio cassette and in a 12-pin power single in line plastic package.

The μPC1277H has two audio power amplifiers and each of the two provides 4.2 W output power at 12 V/4 ohms.

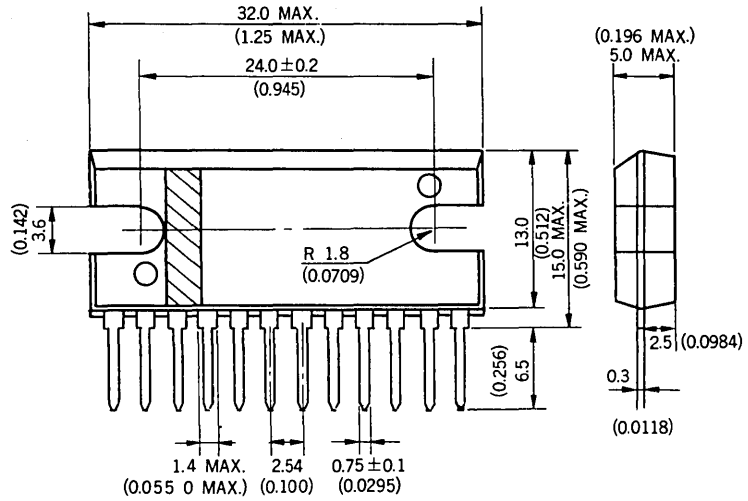
FEATURES

- High output power. 4.2 W/ch (TYP.) V_{CC} = 12 V, R_L = 4 ohms
  5 W/ch (TYP.) V_{CC} = 12 V, R_L = 3 ohms
  2.2 W/ch (TYP.) V_{CC} = 9 V, R_L = 4 ohms
  3 W/ch (TYP.) V_{CC} = 9 V, R_L = 3 ohms
- Wide operating voltage range. V_{CC} = 5 to 16 V
- No shock noise at power supply switch on and off.
- Soft clipping wave form.
- High ripple rejection ratio. R.R.R. = 50 dB (TYP.)
- Few external components. 12 parts
- Thermal shut'down circuit is built in.
- A 12-pin power SIP can easily be mounted on PCB and a external heat sink can easily be attached.

BLOCK DIAGRAM



PACKAGE DIMENSIONS in millimeters (inches)



CONNECTION DIAGRAM

Pin No.	Connection
1	GND (Input)
2	Output 1
3	Boot Strap 1
4	Filter
5	NFB 1
6	Input 1
7	Input 2
8	NFB 2
9	Boot Strap 2
10	V_{CC}
11	Output 2
12	GND (Output)

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Supply Voltage (No Signal)	V_{CC1}	20	V
Supply Voltage (Operating)	V_{CC2}	16	V
Allowable Power Dissipation	P_D	13*	W
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +150	°C

* 100 x 100 x 2 mm³ Al heat sink

RECOMMENDED OPERATING CONDITIONS (Ta = 25 °C)

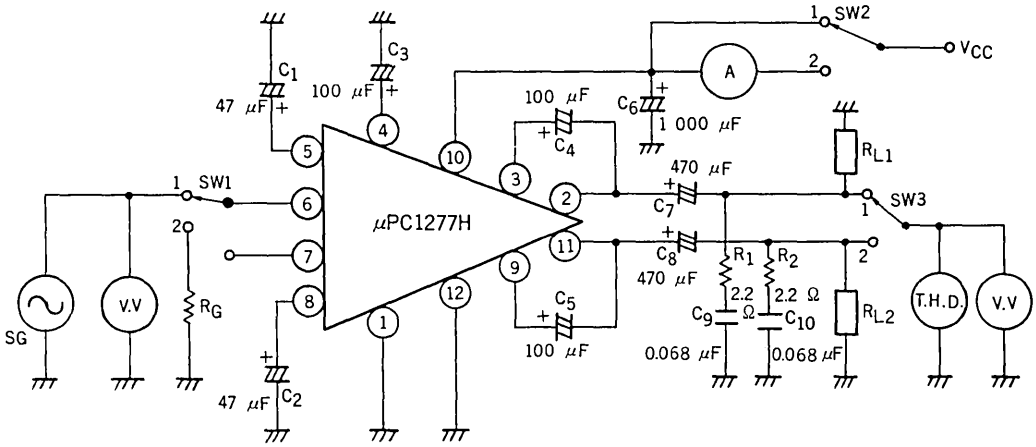
Supply Voltage	V_{CC}	5 to 12 to 16	V
Load Impedance	R_L	3 to 4 to 8	ohms

ELECTRICAL CHARACTERISTICS

(V_{CC} = 12 V, R_L = 4 ohm, f = 1 kHz, Ta = 25 °C,
100 x 100 x 2 mm Al Panel Heat Sink)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Circuit Current	I_{CC}	20	45	90	mA	No Signal
Voltage Gain	A_V	42	45	48	dB	P_O = 1 W
Output Power	P_{O1}	1.8	2.2		W	T.H.D. = 10 % V_{CC} = 9 V, R_L = 4 ohm
	P_{O2}	2.5	3		W	T.H.D. = 10 % V_{CC} = 9 V, R_L = 3 ohm
	P_{O3}	3.2	4.2		W	T.H.D. = 10 % V_{CC} = 12 V, R_L = 4 ohm
	P_{O4}	4	5		W	T.H.D. = 10 % V_{CC} = 12 V, R_L = 3 ohm
Total Harmonic Distortion	T.H.D.		0.2	1	%	P_O = 1 W
Output Noise Voltage	NL		0.6	2	mVr.m.s.	R_G = 10 kohm
Cross Talk	C.T.	45	55		dB	P_O = 1 W other ch. R_G = 10 kohm
Channel Balance	Ch. B.	−2	0	+2	dB	P_O = 1 W
Ripple Rejection	R.R.	40	50		dB	R_G = 0, f = 100 Hz v = 0.3 Vr.m.s.
Input Impedance	Z_{in}	30	50		kohm	

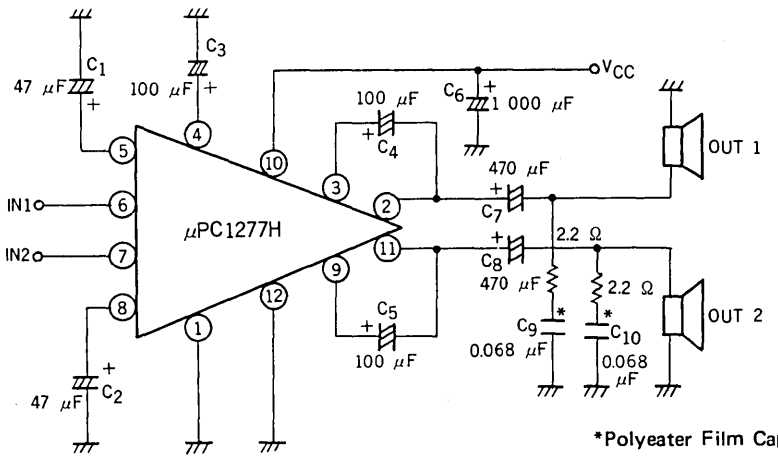
TEST CIRCUIT



SWITCH POSITION (AMP 1 : TEST)

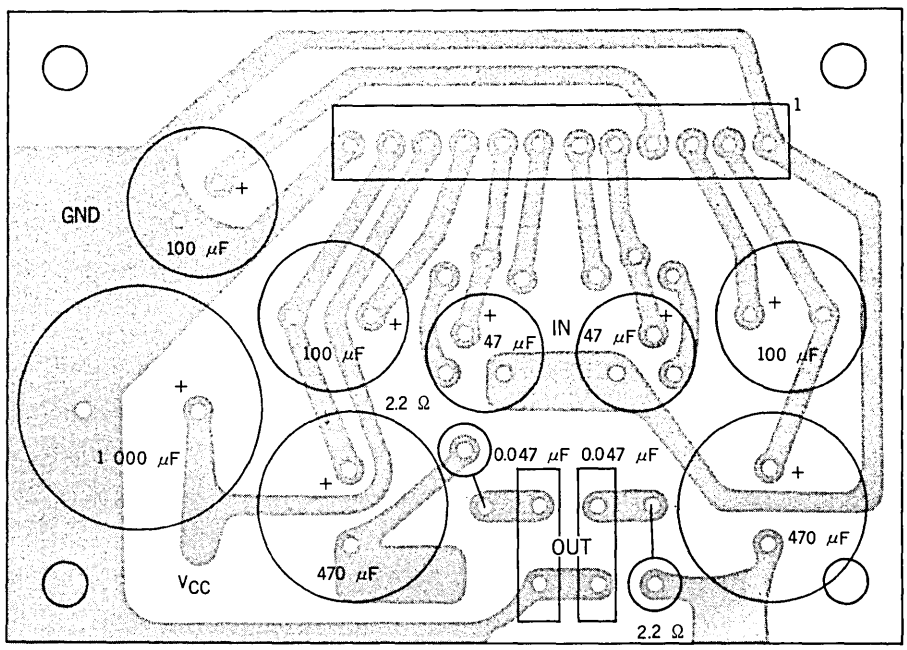
ITEM	SYMBOL	SW 1	SW 2	SW 3
Circuit Current	I_{CC}	2	2	1
Voltage Gain	A_V	1	1	1
Output Power	P_O	1	1	1
Total Harmonic Distortion	T.H.D.	1	1	1
Output Noise Voltage	NL	2	1	1

TYPICAL APPLICATION



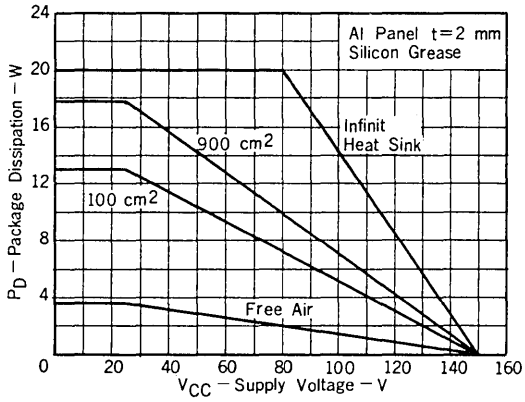
*Polyeater Film Capacitor

TYPICAL PCB (COPPER SIDE)

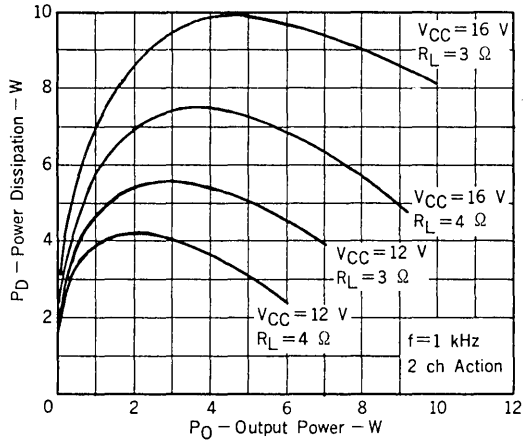


TYPICAL CHARACTERISTICS (Ta = 25 °C)

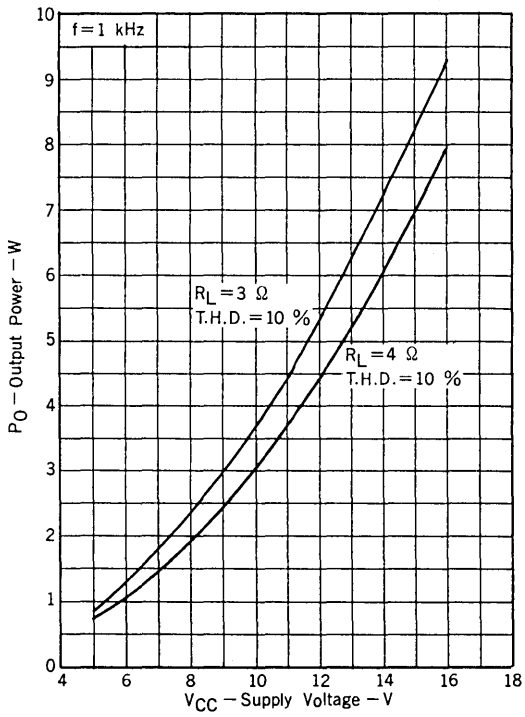
PACKAGE DISSIPATION vs. AMBIENT TEMPERATURE



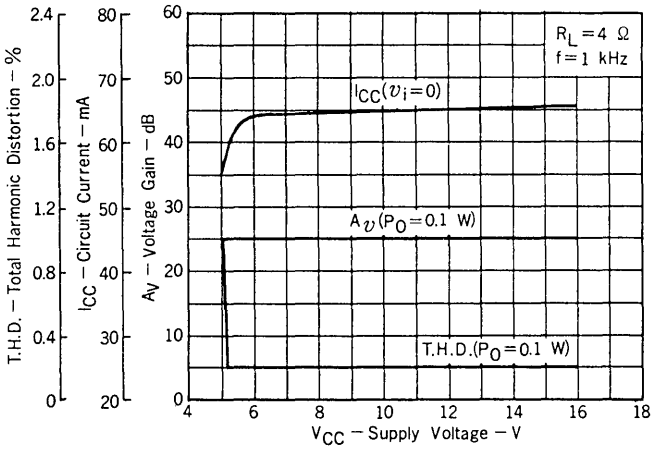
POWER DISSIPATION vs. OUTPUT POWER



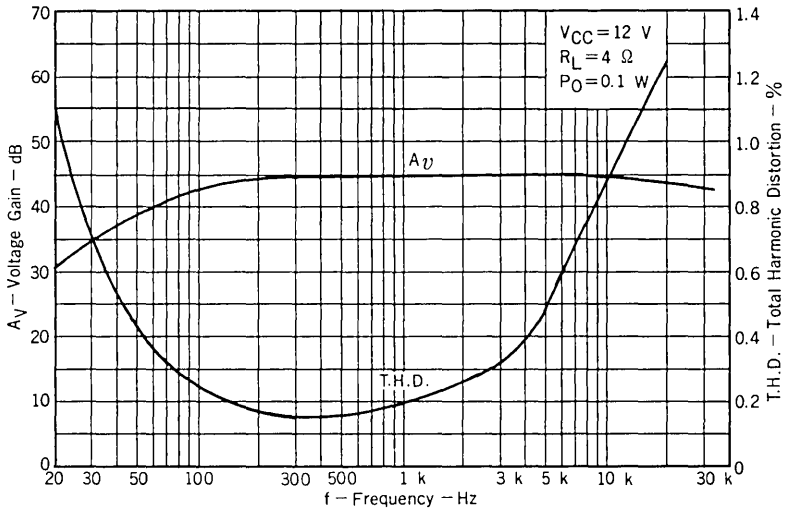
OUTPUT POWER vs. SUPPLY VOLTAGE



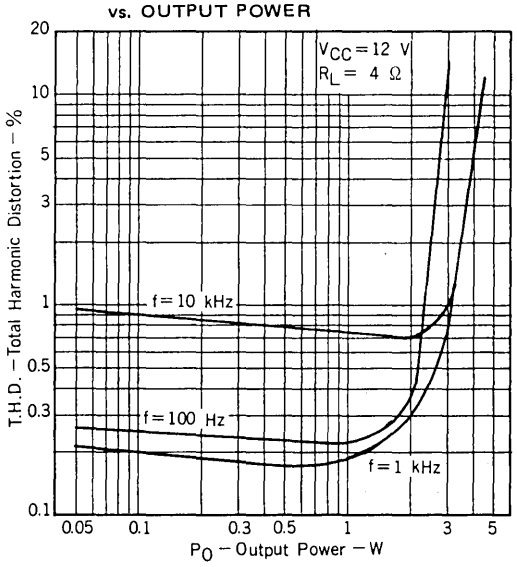
SUPPLY VOLTAGE CHARACTERISTICS



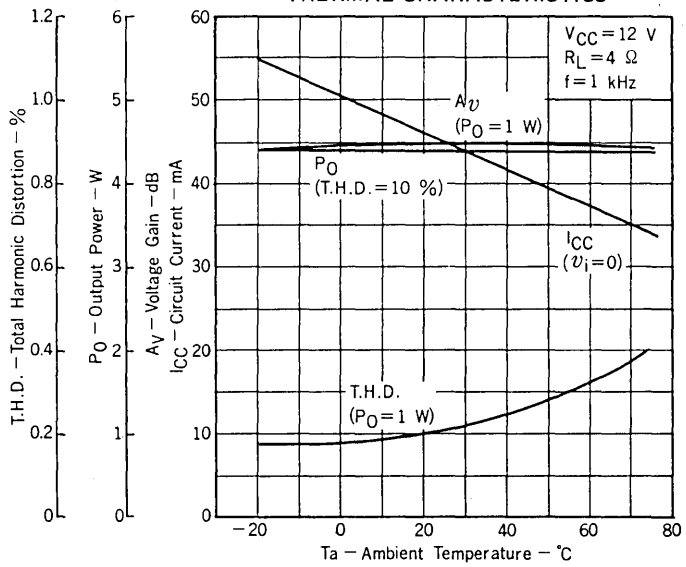
VOLTAGE GAIN, TOTAL HARMONIC DISTORTION vs. FREQUENCY



TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



THERMAL CHARACTERISTICS



Note 1) An inverse connection of the supply voltage pin and the GND pin or a connection of the output pin and either the supply voltage line or GND sometimes causes μPC1277H to break down immediately. Handle it with care.

Note 2) GND pins #1 (input side GND) and #12 (output side GND) are separated inside of the IC, therefore connect them on a PCB. Make the input and output common impedance least when designing a PCB.

Note 3) Recommend a polyeater Film capacitor as a phase compasated capacitance (0.068 μF). Choose larger capacity in case that a long power supply line on a PCB causes the IC a parasitic oscillation.

BIPOLAR ANALOG INTEGRATED CIRCUIT
μPC1350C

450mW AF POWER AMPLIFIER WITH PRE AMPLIFIER AND ALC CIRCUIT SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

DESCRIPTION

The μPC1350C is a silicon monolithic integrated circuit designed for an audio power amplifier application at 6 volts power supply.

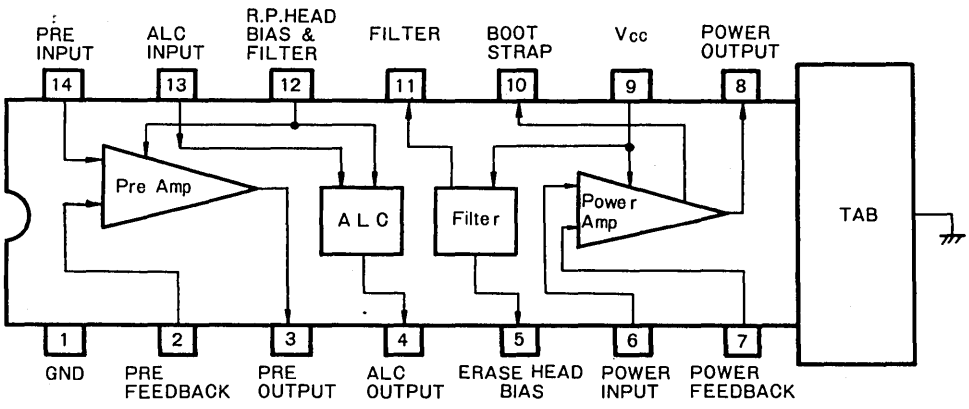
The device contains a high gain low noise preamplifier, an automatic level control (ALC) and a high gain low distortion power amplifier.

The perfect audio circuit of a cassette tape recorder is obtained with the device.

FEATURES

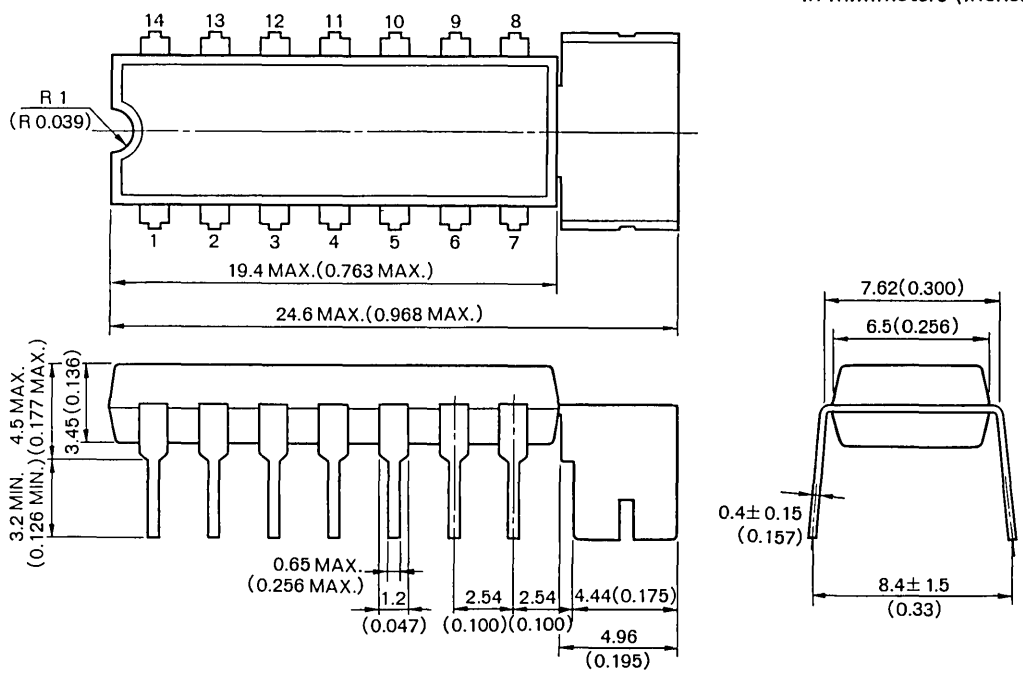
- All functions of a preamplifier, an ALC circuit and a power amplifier are encapsulated in a 14-pins dual in-line package with heat sink TAB.
- Low noise, especially low pulsive noise.
- Power amplifier stage has high gain, high output power and low distortion characteristics.
- Preamplifier stage has high gain and low distortion characteristics.
- Wide ALC range: output voltage change 1.8 V TYP. , ALC range 60 dB TYP.
- Wide supply operating voltage range: V_{CC} = 3.5 to 10 V
- Low spurious radiation when driven to output clipping level.

BLOCK DIAGRAM



PACKAGE DIMENSIONS AND CONNECTION DIAGRAM (Top View)

in millimeters (inches)



Pin No.	Electrical Connections	Pin No.	Electrical Connections
1	GND	8	Power; Output
2	Pre.; Feedback	9	Power Supply V_{CC}
3	Pre.; Output	10	Boot Strap
4	ALC Output	11	Filter
5	Erase; Head Bias	12	R.P. Head Bias & Filter
6	Power; Input	13	ALC Input
7	Power; Feedback	14	Pre.; Input

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Supply Voltage (DC)	V_{CC1}	12	V
Supply Voltage (AC)	V_{CC2}	10	V
Circuit Current	I_{CC}(peak)	500	mA
Package Dissipation	P_D	2.4*	W
Operating Temperature	Topt	−20 to +75	°C
Storage Temperature	Tstg	−40 to +125	°C

* Mounted and soldered on a 50 mm x 50 mm copper foil of a printed circuit board (XXX3 grade).

RECOMMENDED CONDITIONS (Ta = 25 °C)

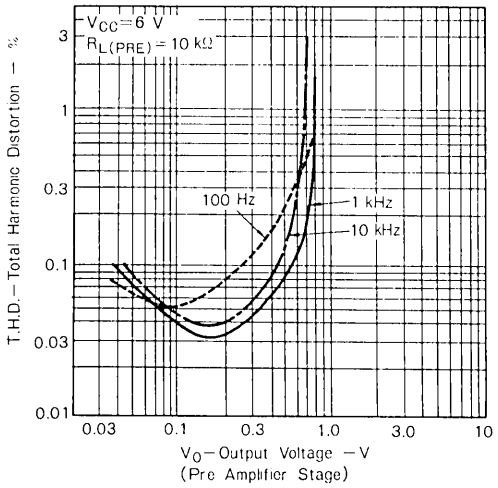
Operating Supply Voltage	6	V
Supply Voltage Range	3.5 to 10	V

ELECTRICAL CHARACTERISTICS (Ta = 25 °C, V_{CC} = 6 V, f = 1 kHz, NAB, R_L(pre) = 10 kΩ, R_L(power) = 8 Ω)

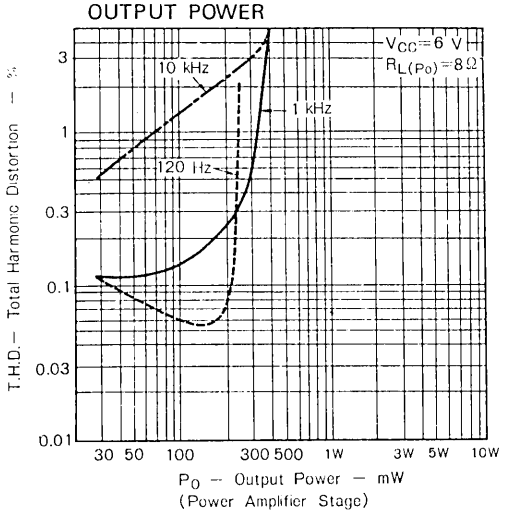
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
[OVER ALL CHARACTERISTIC]						
Circuit Current	I_{CC}	10	20	33	mA	NO SIGNAL
Output Power	Po	400	450	—	mW	V_R→MAX. T.H.D. = 10 %
Total Harmonic Distortion	T.H.D.	—	0.8	2.0	%	V_R→MAX. Po = 50 mW
Output Noise Level	NL_1	—	10	23	$mV_{r.m.s.}$	Using P. head as an R_G. V_R→MAX.
ALC Characteristic	ALC_1	—	1.8	9	dB	V_i = −70 ~ −40 dBm RL' = 56 Ω
ALC Range	ALC2		60		dB	T.H.D. ≦ 3 % R_L' = 56 Ω
[PRE AMPLIFIER STAGE]						
Open Loop Voltage Gain	$A_{v}o1$	55	65	—	dB	R_L(pre) = 10 kΩ Vo = $0.3V_{r.m.s.}$
Voltage Gain	$A_{v}2$		30.8		dB	NAB Vo = $0.3V_{r.m.s.}$
Maximum Output Voltage	V_{OM}		0.8	—	$V_{r.m.s.}$	R_L(pre) = 10 kΩ T.H.D. = 1 %
Input Impedance	Ri1	20			kΩ	
[POWER AMPLIFIER STAGE]						
Open Loop Voltage Gain	$A_{v}o2$	70	81	—	dB	Po = 50 mW
Voltage Gain	$A_{v}2$		46.8		dB	Po = 50 mW
Output Noise Level	NL_2	—	0.4	2.0	$mV_{r.m.s.}$	V_R→MIN. (R_G = 0)
Input Impedance	Ri2	20	28		kΩ	

TYPICAL CHARACTERISTICS (Ta = 25 °C, TEST CIRCUIT)

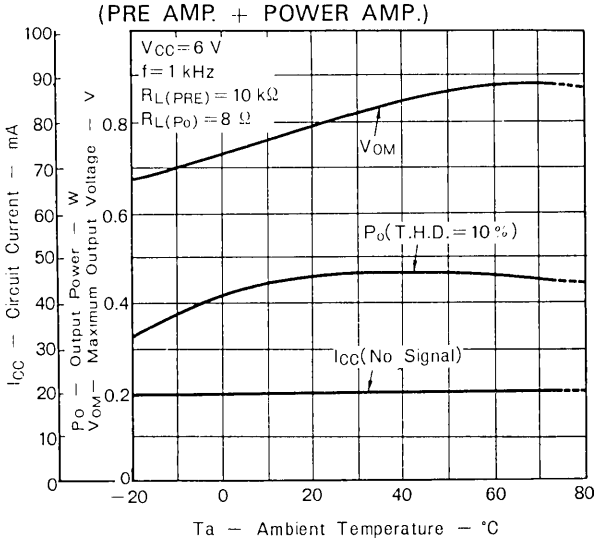
TOTAL HARMONIC DISTORTION vs. OUTPUT VOLTAGE.



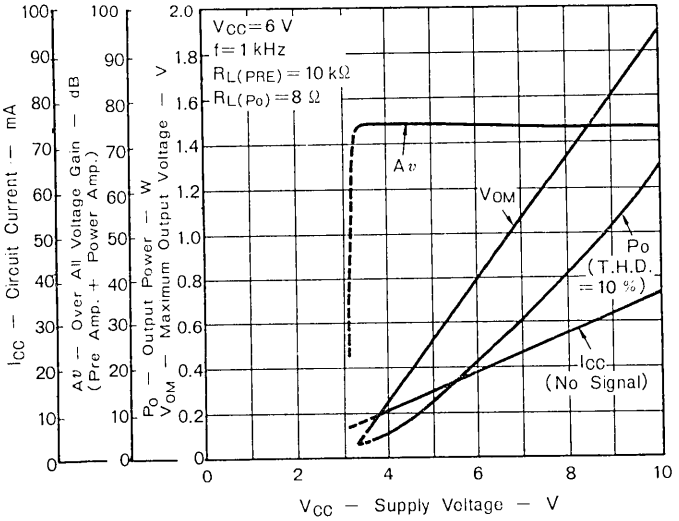
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



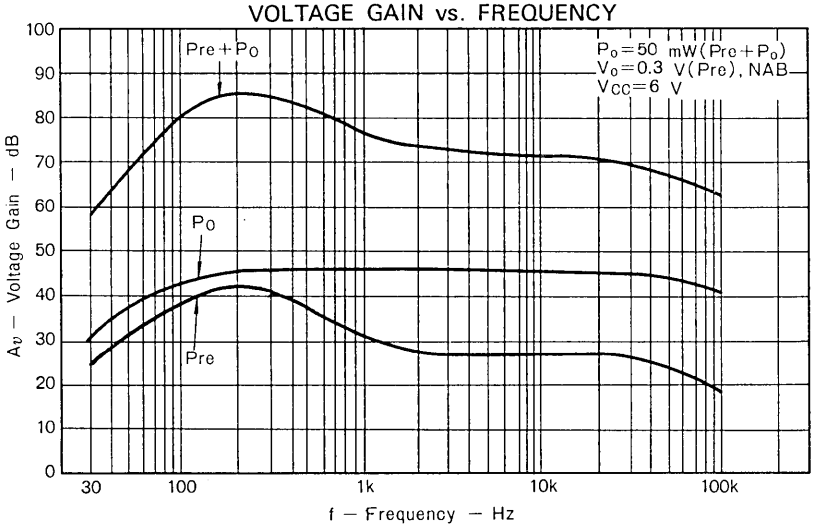
CIRCUIT CURRENT, OUTPUT POWER, MAXIMUN OUTPUT VOLTAGE GAIN vs. AMBIENT TEMPERATURE (PRE AMP. + POWER AMP.)



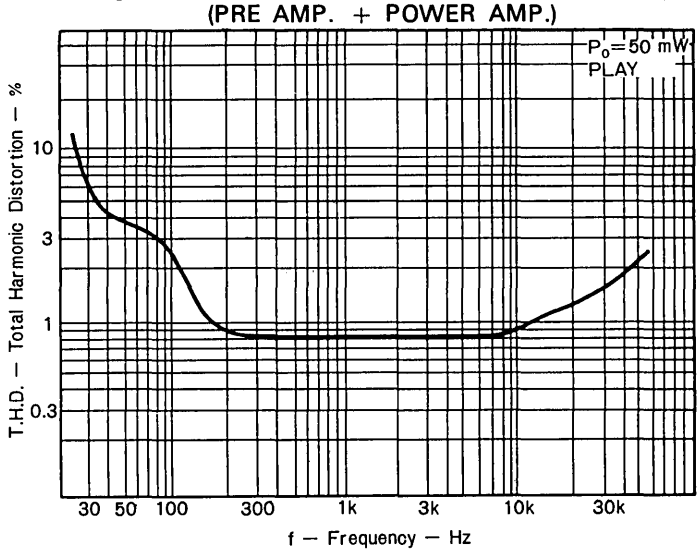
CIRCUIT CURRENT, OVER ALL VOLTAGE GAIN, OUTPUT POWER, MAXIMUM OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



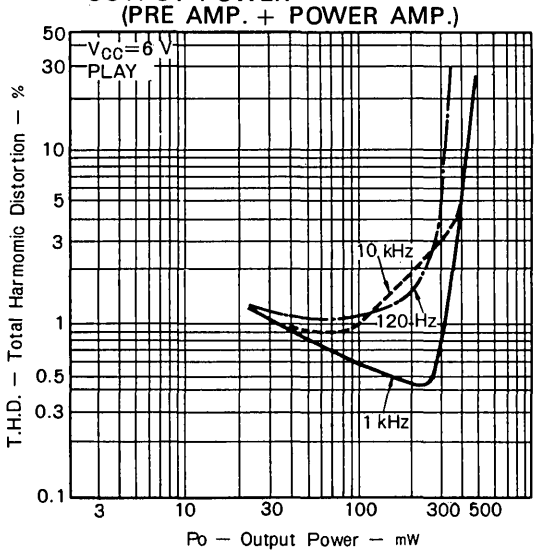
VOLTAGE GAIN vs. FREQUENCY



TOTAL HARMONIC DISTORTION vs. FREQUENCY
(PRE AMP. + POWER AMP.)



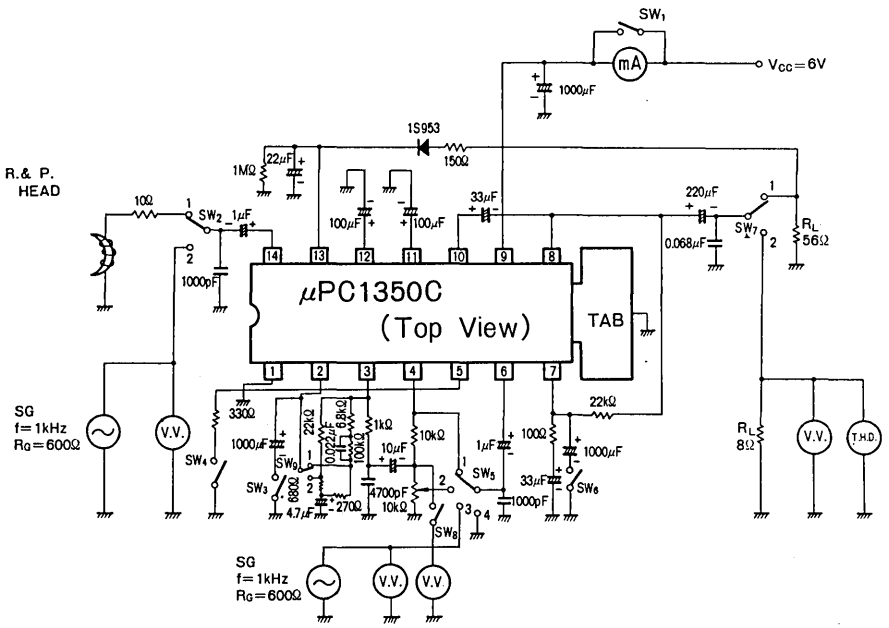
TOTAL HARMONIC DISTORTION vs.
OUTPUT POWER
(PRE AMP. + POWER AMP.)



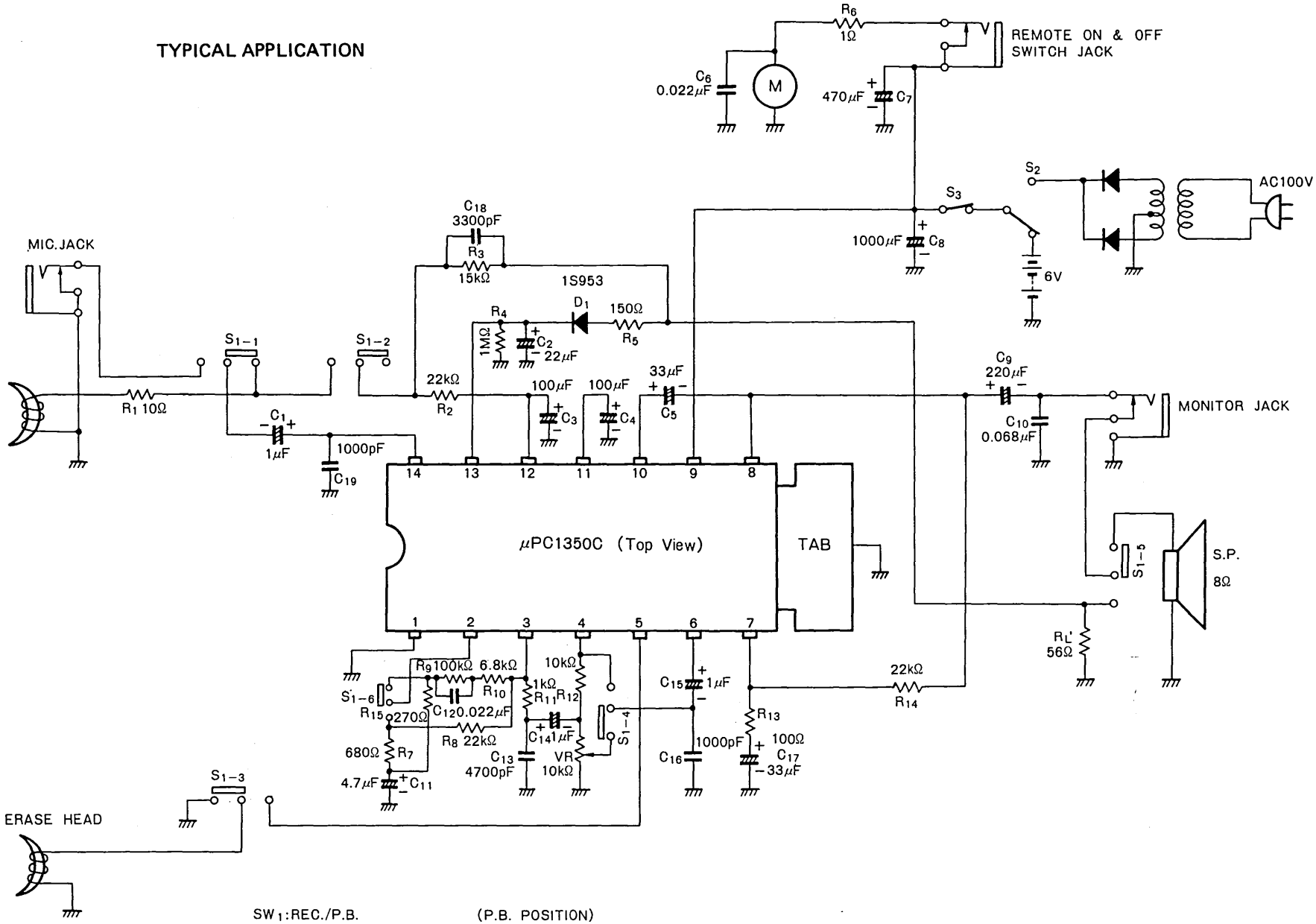
TEST CIRCUIT STATUS

ITEM	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9
ICC	OFF	1	OFF	ON	2	OFF	2	OFF	1
Po	ON	2	OFF	OFF	2	OFF	2	OFF	1
T.H.D.	ON	2	OFF	OFF	2	OFF	2	OFF	1
NL1	ON	1	OFF	OFF	2	OFF	2	OFF	1
ALC	ON	2	OFF	OFF	1	OFF	1	OFF	2
Avo1	ON	2	ON	OFF	4	OFF	2	ON	2
Avo2	ON	1	OFF	OFF	3	ON	2	OFF	2
NL2	ON	1	OFF	OFF	4	OFF	2	OFF	2

TEST CIRCUIT



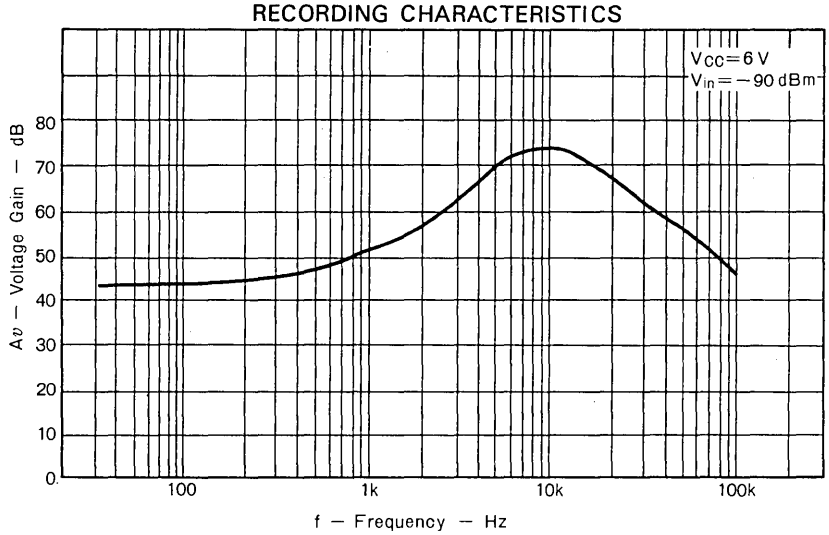
TYPICAL APPLICATION



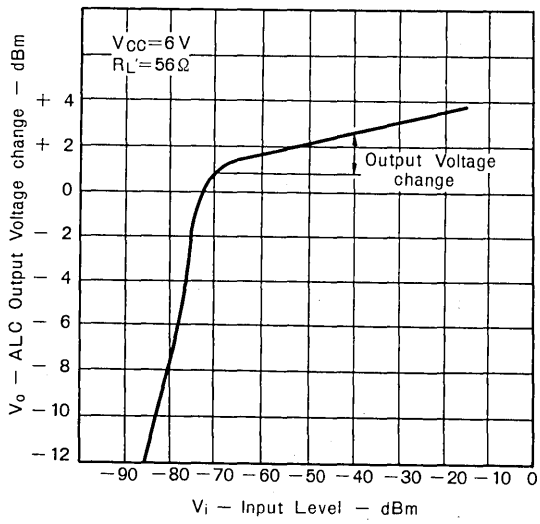
SW1:REC./P.B. (P.B. POSITION)
SW2:AC/DC OPERATION (DC OPERATION)
SW3:Power Switch (ON POSITION)

TYPICAL CHARACTERISTICS (Ta = 25 °C, TYPICAL APPLICATION CIRCUIT)

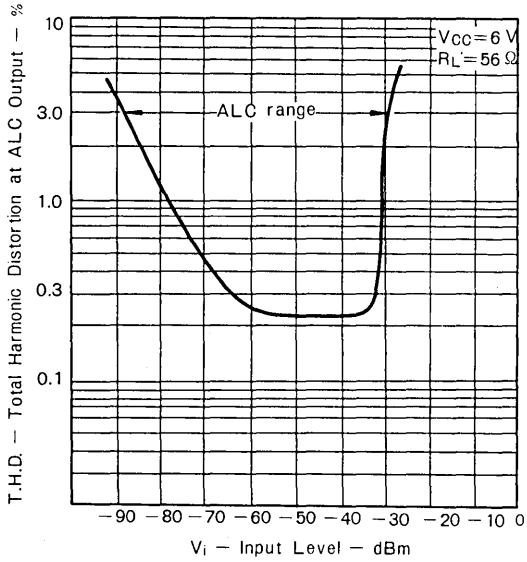
RECORDING CHARACTERISTICS



ALC OUTPUT VOLTAGE CHANGE vs. INPUT LEVEL



T.H.D. AT ALC OUTPUT vs. INPUT LEVEL

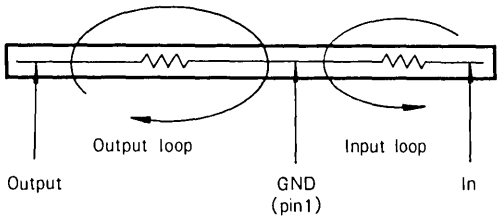


NOTES FOR USE

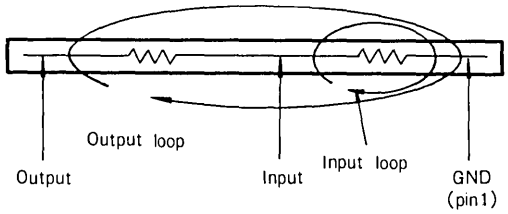
1. About capacitor C10
   To avoid parasitic oscillation at power amplifier stage, apply the suitable capacitor as C10 as follows.
   For a cassette tape recorder, a ceramic capacitor or a Mylar capacitor can be used equally.
   For a cassette tape recorder with radio, use a Mylar capacitor. If a ceramic capacitor is used, a parasitic oscillation may occur caused by feed back as radiation from the capacitor to an RF stage.
2. About recovery time at recording
   A recovery time depends on a time constant of a capacity value of C2 and a pallarel value of R4 and an input impedance of IC at pin 13.
   The recovery time can be adjusted by R4 value.

PRINTED CIRCUIT BOARD DESIGN CONSIDERATION

1. Use the widest possible printed foil for a power supply and a ground.
2. The earthing point of C8, C10 and an output terminal should be located as close as possible to the earthing (ground) pins (pin 1 and TAB).
3. One-point earthing is ideal, but if this is impossible, keep the input loop out of the output loop.



(good example)

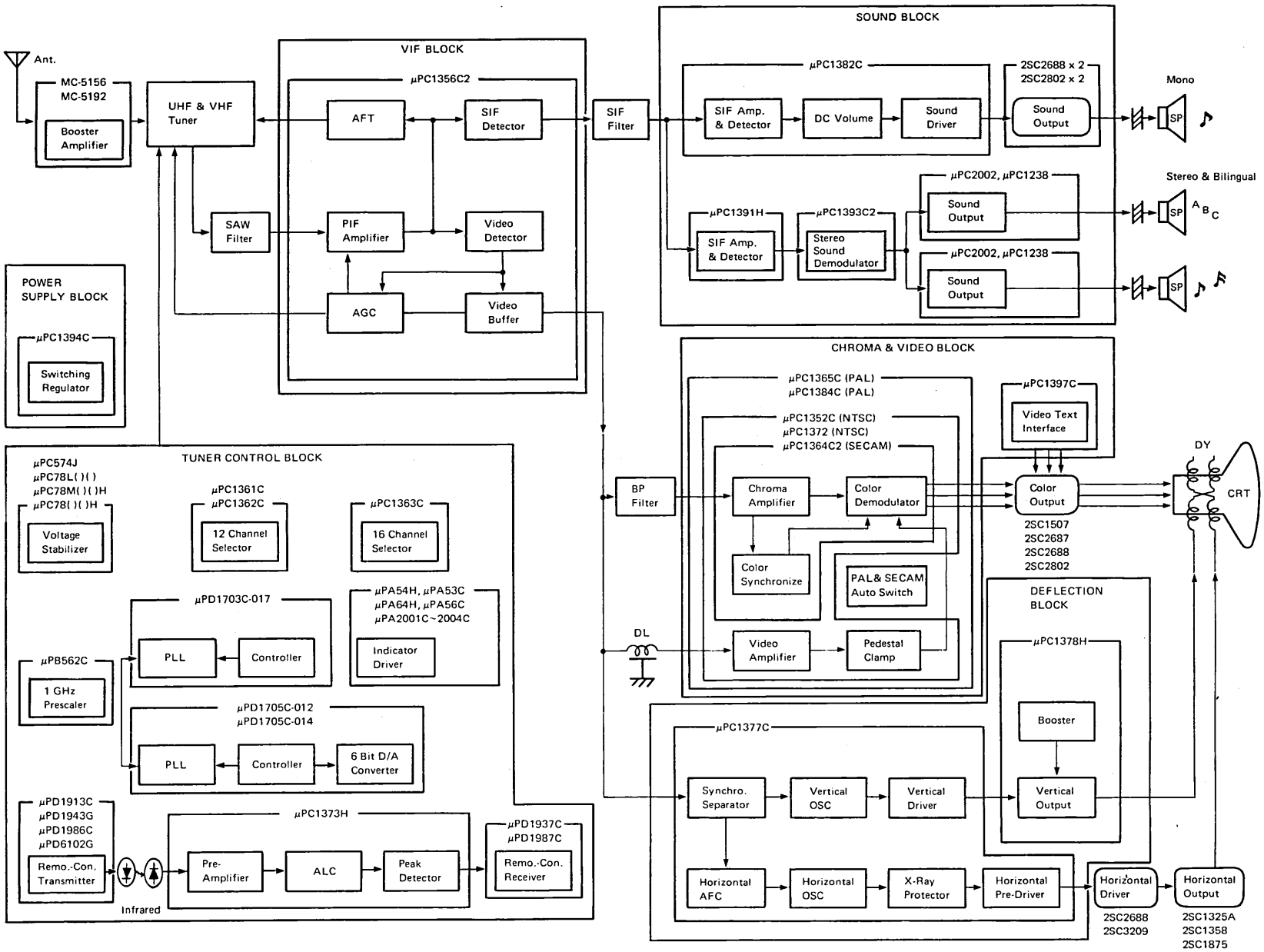


(bad example)

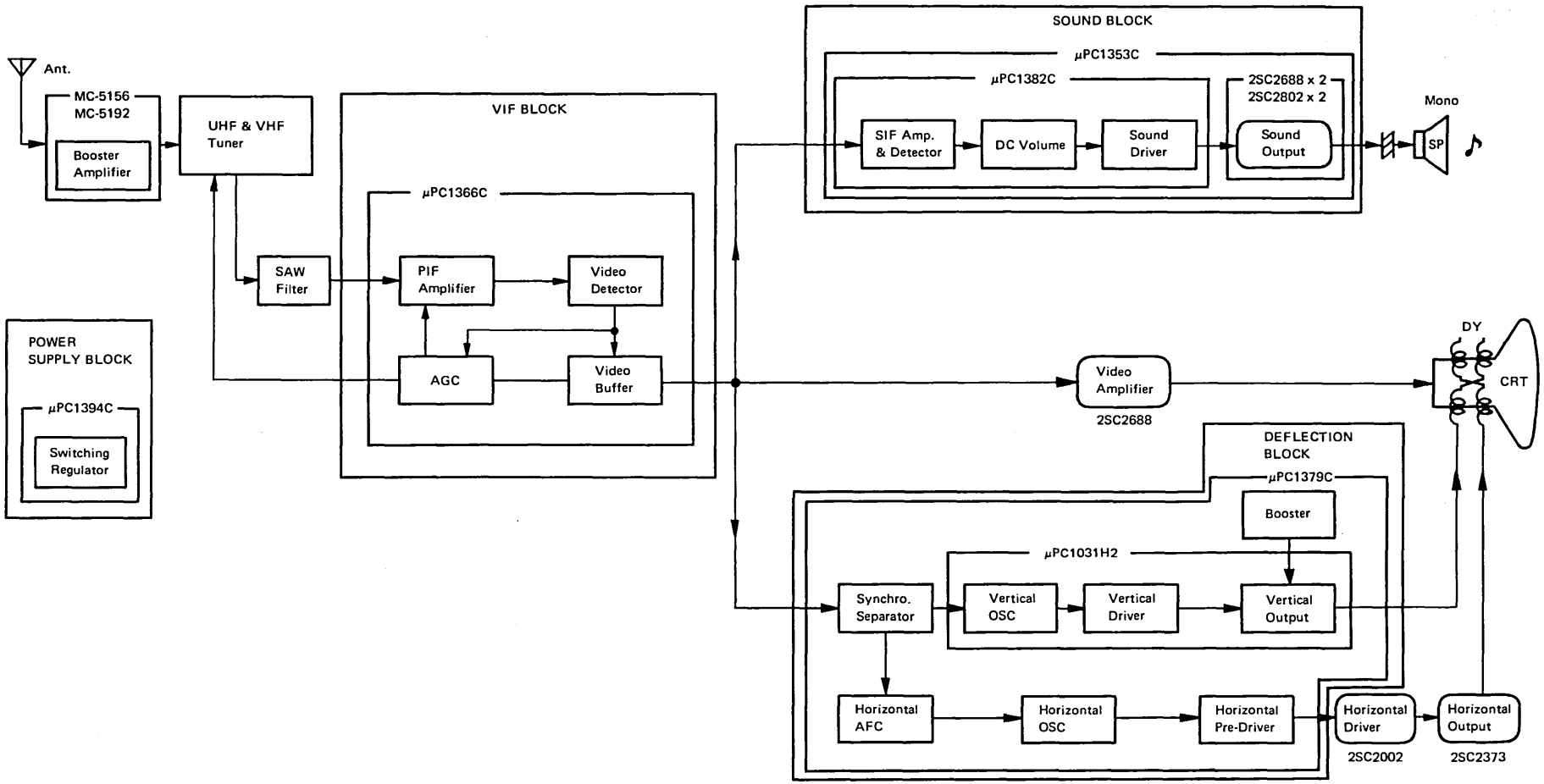
INDEX

BLOCK DIAGRAM

Color TV Block



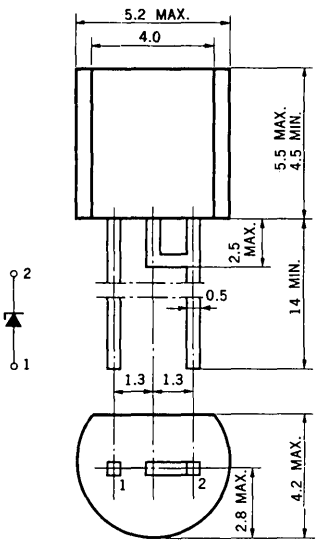
B/W TV Block


Ant.
MC-5156
MC-5192
Booster Amplifier
UHF & VHF Tuner
SAW Filter
VIF BLOCK
μPC1366C
PIF Amplifier
Video Detector
AGC
Video Buffer
POWER SUPPLY BLOCK
μPC1394C
Switching Regulator
SOUND BLOCK
μPC1353C
μPC1382C
SIF Amp. & Detector
DC Volume
Sound Driver
2SC2688 x 2
2SC2802 x 2
Sound Output
Mono
SP
Video Amplifier
2SC2688
DY
CRT
DEFLECTION BLOCK
μPC1379C
Booster
μPC1031H2
Synchro. Separator
Vertical OSC
Vertical Driver
Vertical Output
Horizontal AFC
Horizontal OSC
Horizontal Pre-Driver
Horizontal Driver
2SC2002
Horizontal Output
2SC2373

BIPOLAR ANALOG INTEGRATED CIRCUIT
μPC574J

MONOLITHIC BIPOLAR INTEGRATED CIRCUIT
VOLTAGE STABILIZER FOR ELECTRONIC TUNER

PACKAGE DIMENSIONS
(Unit : mm)



Pin Connection
1. Anode
2. Cathode

The μPC574J is a monolithic integrated voltage stabilizer especially designed as voltage supplier for electronic tuners.

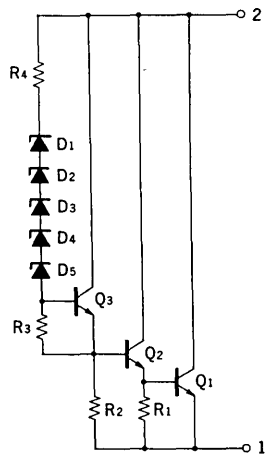
FEATURES

- Low temperature coefficient
- Low dynamic resistance
- Typical reference voltage of 33 V

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Zener Current	I_Z	10	mA
Power Dissipation	P_D	200 (T_a = 75 °C)	mW
Operating Ambient Temperature Range	T_{opt}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C

EQUIVALENT CIRCUIT

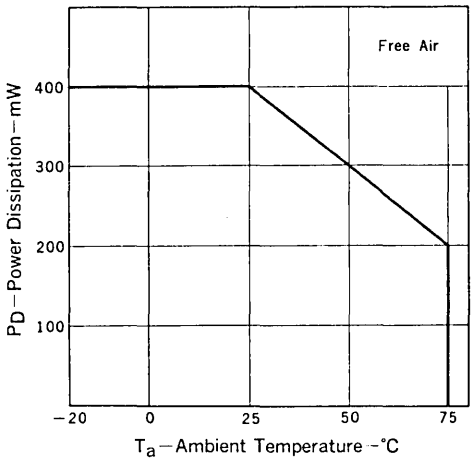


ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

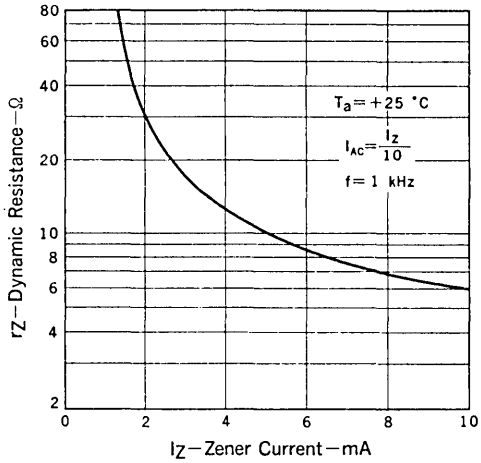
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Stabilized Voltage	V_Z	31		35	V	I_Z = 5 mA
Stabilized Voltage Temperature Drift	$\Delta V_Z/\Delta T$	-1.0	0	1.0	mV/°C	I_Z = 5 mA T_a = −20 to +75 °C
Dynamic Resistance	r_Z		10	25	Ω	I_Z = 5 mA f = 1 kHz I_{AC} = 0.5 mA

TYPICAL CHARACTERISTIC (T_a = 25 °C)

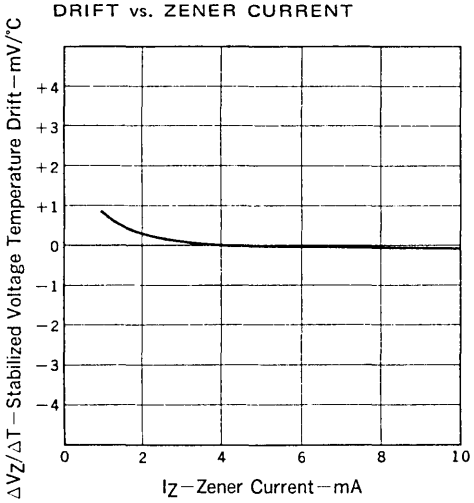
POWER DISSIPATION vs. AMBIENT TEMPERATURE



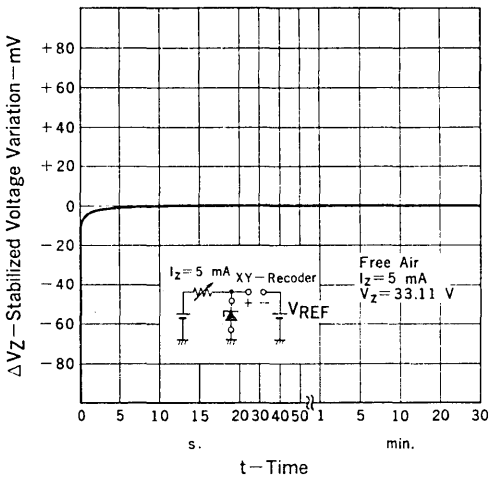
DYNAMIC RESISTANCE vs. ZENER CURRENT



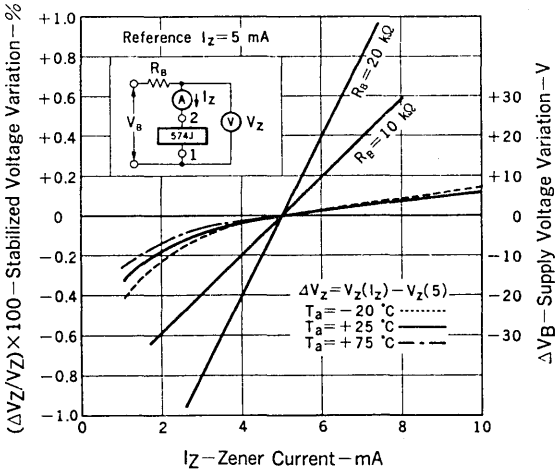
STABILIZED VOLTAGE TEMPERATURE DRIFT vs. ZENER CURRENT



STABILIZED VOLTAGE VARIATION vs. TIME

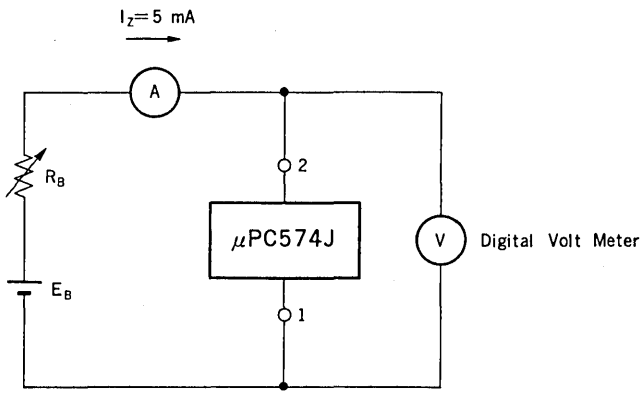


STABILIZED VOLTAGE VARIATION & SUPPLY VOLTAGE VARIATION vs. ZENER CURRENT

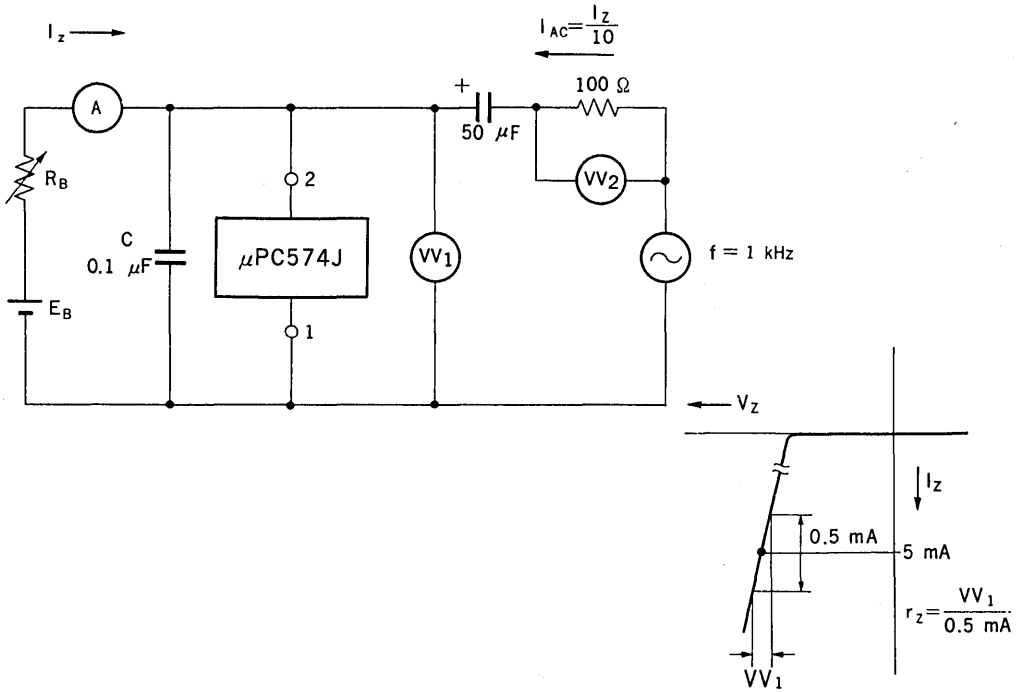


MEASURING CIRCUITS

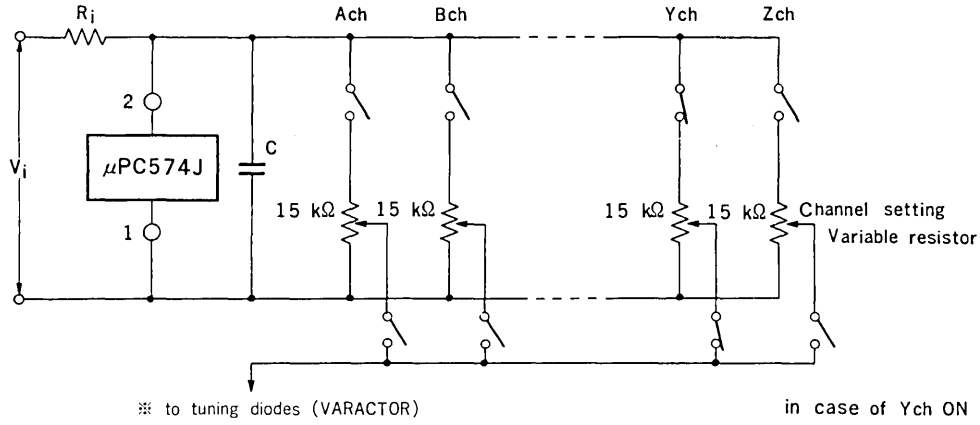
Measuring Circuit for Stabilized Voltage V_Z



Measuring Circuit for Dynamic Resistance r_Z



TYPICAL APPLICATION



BIPOLAR ANALOG INTEGRATED CIRCUIT
μPC1361C

ELECTRONIC CHANNEL SELECTOR

DESCRIPTION

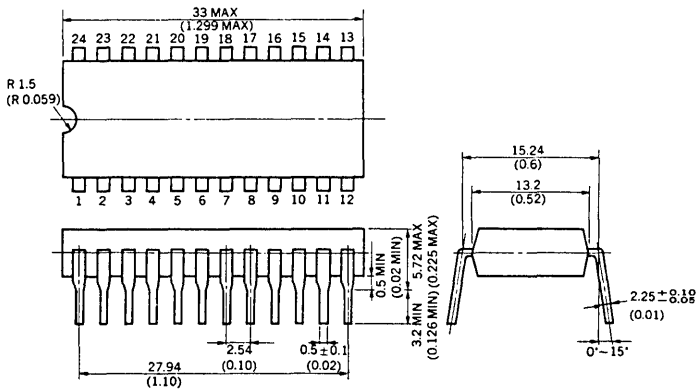
The μPC1361C is an electronic channel selector integrated circuit with 4 bit output. It is capable of selecting up to 12 channels. The output terminals are design to permit the direct driving of LED or neon lamps.

This IC consists of Clock Oscillator circuit, Channel Up and Down circuit, Channel skip circuit, 4 bit Up and Down Counter circuit, 1-12 Decoder circuit, 4 bit Output Buffer circuit and 12 channel Output Buffer circuit, all of which are contained in a 24 pins dual in-line package.

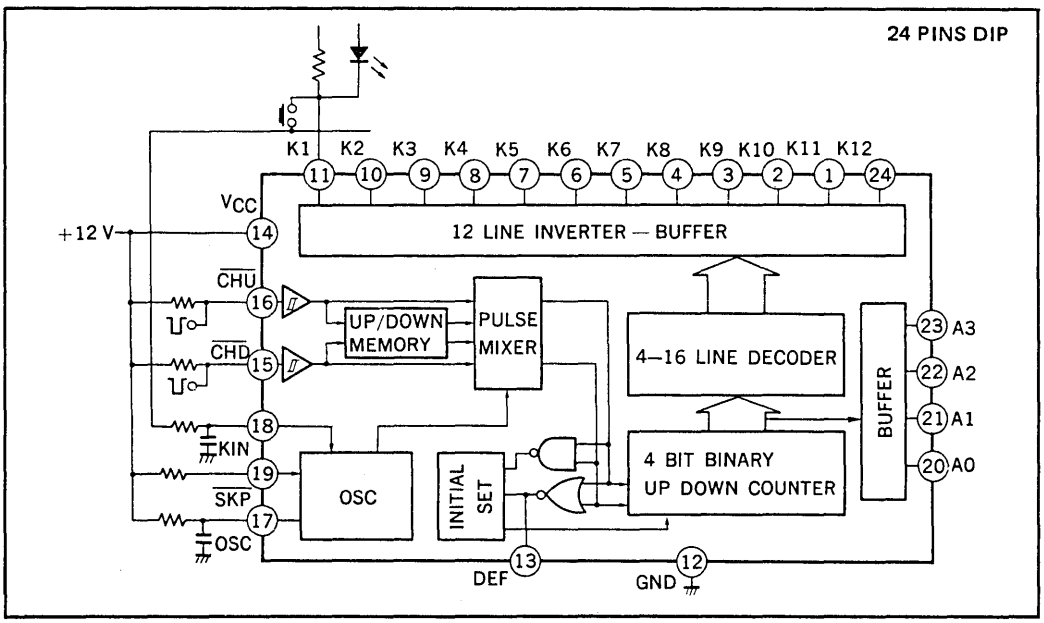
FEATURES

- 4 bit output
- LED, Neon lamps direct drive.
  I_K=5 mA, V_{kSAT} 150 mV MAX.
- Low power consumption.
  V_{CC}=12 V, I_{CC}=9 mA TYP.
- Up to 12 channel selection.
- Internal schmitt trigger circuit. (CHU, CHD INPUT)
- Power ON initial channel set.
- TV, Radio etc. channel selection use.

PACKAGE DIMENSIONS in millimeters (inches)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25 °C)

Supply Voltage	V_{CC}	15.0	V
Input Current to Channel Selection Circuit	$I_{K1\sim11,\ 24}$	−5 to 30	mA
Input Current to Control Circuit	$I_{A0\sim A3}$	−5 to 10	mA
Input Current to Control Circuit	$I_{C18,\ 19}$	−5 to 10	mA
Input Current to Control Circuit	I_{C13}	−5 to 30	mA
*Output Voltage to Channel Selection Circuit	$V_{K1\sim11,\ 20}$	−0.5 to 45	V
*Output Voltage to Control Circuit	$V_{13},\ V_{A0\sim A3}$	−0.5 to 14.4	V
*Input Voltage to Control Circuit	$V_{15,\ 16,\ 17}$	−0.5 to V_{CC}+0.5	V
Power Dissipation	P_d	300	mW
Operating Temperature Range	T_{opt}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C

* At V_{CC}=12 V

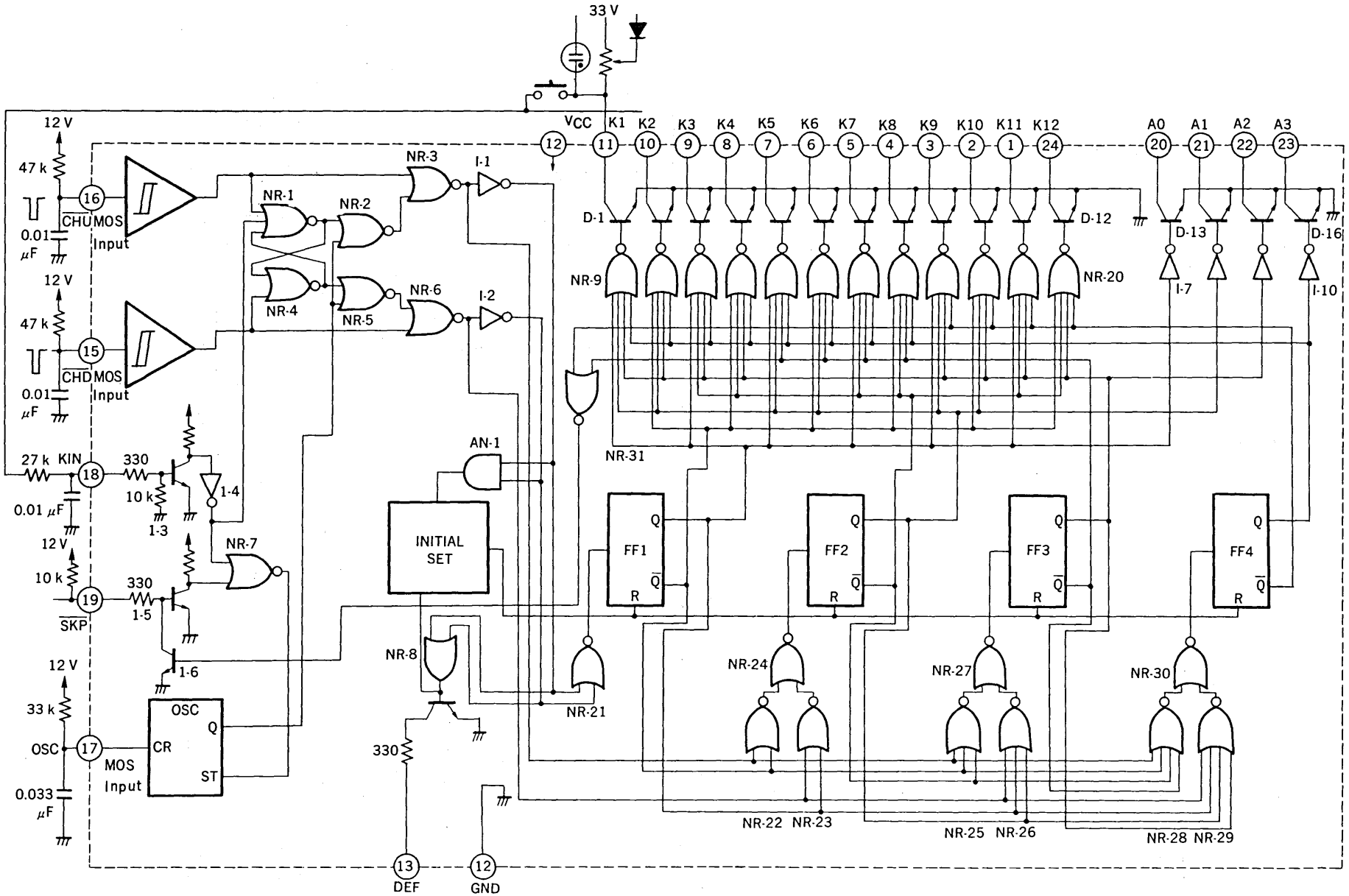
RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	9.6	12.0	14.4	V
Channel Selection Input Current	I_K		5.0		mA
Clock Oscillation Frequency	f_{OSC}		2.0	10.0	kHz

ELECTRICAL CHARACTERISTICS (Ta=25 ±3 °C)

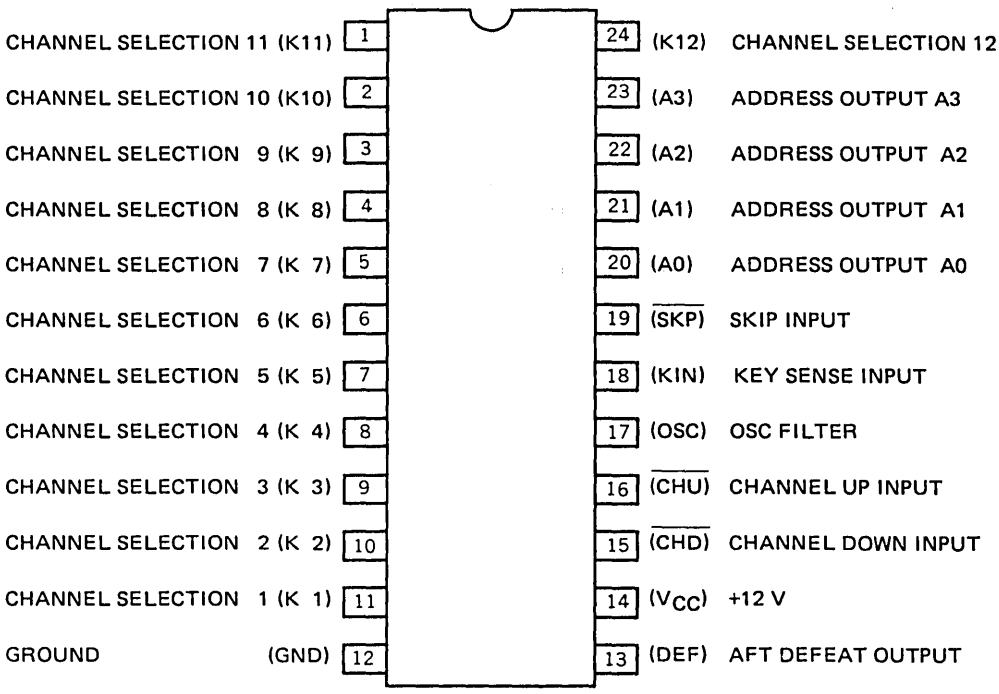
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Current	I_{DD}	2.0	9.0	13.0	mA	V_{CC}=12 V
Channel Selection Saturation Voltage	$V_{OL(K)}$			150	mV	V_{CC}=9.6 V, I_{OL}=5 mA
Channel Selection Leakage Current	$I_{OH(K)}$			10	μA	V_{CC}=14.4 V, V_{OH}=35 V
Address Output Saturation Voltage	$V_{OL(A)}$			0.5	V	V_{CC}=9.6 V, I_{OL}=2 mA
Address Output Leakage Current	$I_{OH(A)}$			10	μA	V_{CC}=14.4 V, V_{OH}=14.4 V
AFT Defeat Output Voltage	$V_{OL(D)}$			6	V	V_{CC}=9.6 V, I_{OL}=12 mA
AFT Defeat Leakage Current	$I_{OH(D)}$			10	μA	V_{CC}=14.4 V, V_{OH}=14.4 V
Channel Input High Threshold Voltage	$V_{TH(CH)}$	7.2		9.0	V	V_{CC}=12 V
Channel Input Low Threshold Voltage	$V_{TL(CH)}$	5.0		8.0	V	V_{CC}=12 V
Channel Input Leakage Current	$I_{CH(CH)}$	−5			μA	V_{CC}=14.4 V, V_{IL}=0 V
Channel Input Leakage Current	$I_{CH(CH)}$			5	μA	V_{CC}=14.4 V, V_{IH}=14.4 V
Key Input Current	$I_{IH(KI)}$	200			μA	V_{CC}=9.6 V
Key Input Leakage Current	$I_{IL(KI)}$	−10			μA	V_{CC}=14.4 V, V_{IL}=0 V
Skip Input Current	$I_{IH(SK)}$	50			μA	V_{CC}=9.6 V
Skip Input Leakage Current	$I_{IL(SK)}$	−5			μA	V_{CC}=14.4 V, V_{IL}=0 V
Channel Hold Voltage	V_{HOLD}	6.5			V	
OSC Frequency	f_{OSC}	1.0	2.0	3.0	kHz	V_{CC}=12 V, R=33 kΩ, C=0.033 μF

EQUIVALENT CIRCUIT



Logic Blocks consist of PMOS technology
Output and Input consist of Bipolar technology.

CONNECTION DIAGRAM (Top View)



PIN FUNCTION

K1 ~ 12 (#11 ~ 1, #24) CHANNEL SELECTION OUTPUT

These are the output terminals constructed of collector-opened transistors, so they can drive potentiometers and indicators, and key output. They have saturation voltage of 150 mV at I_K=5 mA, so they can drive neon or LED lamps directly.

GND (#12) GROUND

DEF (#13) AFT DEFEAT OUTPUT

This terminal is made of open collector transistor output through a resistor of 330 Ω. It is used for AFT (Automatic Fine Tuning ..... TV use) defeat, sound muting and LED indicate erasing.

V_{CC} (#14) +12 V (9.6 ~ 14.4 V)

CHD (#15) CHANNEL DOWN INPUT

Usually pulled up to V_{CC} through a resistor, Channel selector changes at positive going edge of input signal of this terminal and the channel selector works orderly from K12 to K1.

CHU (#16) CHANNEL UP INPUT

Usually pull up to V_{CC} through a resistor, Channel selector changes at positive going edge of input signal of this terminal and the channel selector works orderly from K1 to K12. If CHU and CHD terminals put down to ground at same time, initial channel is selected. So, it is very useful to remote control operation use. These terminals include schmitt trigger circuit. If these terminals are not used as remote control operation, connect these terminals to V_{CC} directry.

OSC (#17) OSC FILTER

When a Channel key is pushed or skip function is operated, oscillator contained in this IC oscillate with C, R connected to this terminal. Typical oscillation frequency is 2 kHz. (R=33 kΩ, C=0.033 μF)

KIN (#18) KEY INPUT

When channel selection key is pushed, as pushed channel is not selected, "High" level of signal is applied to this terminal through a potentiometer resistor. Then channel selector scans terminals of K1 ~ K12. And when sense up this terminal, it pull down the voltage of this terminal and stop the scanning.

SKP (#19) SKIP INPUT

Usually pull up to V_{CC} through resistor. When only 10 channels are used, connect open channel outputs (K11, K12) to this terminal with CR filter.

A0 ~ A3 (#20 ~ 23) ADDRESS OUTPUT A0 ~ A3

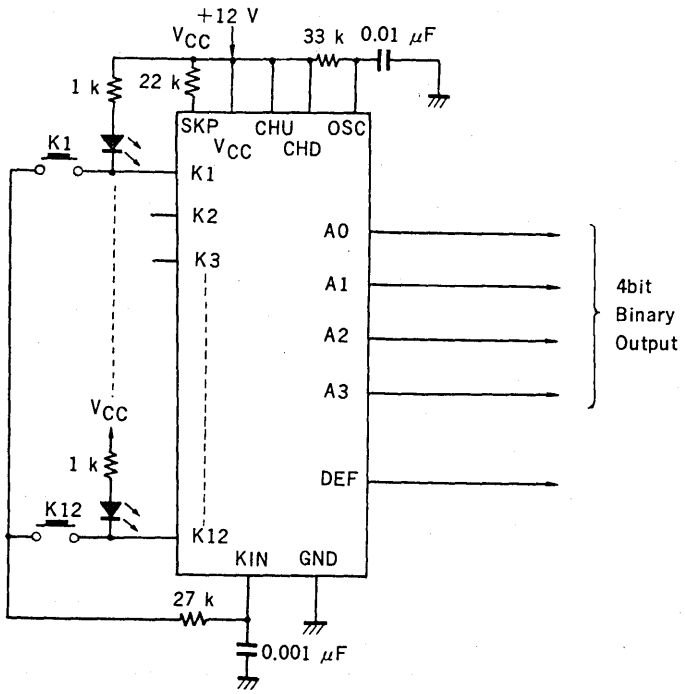
These are internal 4 bit counter output terminals constructed of collector-opened transistors. These output can be used as 7 segment LED display or possition output for MPU reading.

Selectchannel	Address output			
	A0...L	A1...L	A2...L	A3...L
K 1	H	L	L	L
K 2	L	H	L	L
K 3	H	H	L	L
K 4	L	L	H	L
K 5	H	L	H	L
K 6	L	H	H	L
K 7	H	H	H	L
K 8	L	L	L	H
K 9	H	L	L	H
K 10	L	H	L	H
K 11	H	H	L	H
K 12	H	H	L	H

※ L...GND
H...OPEN

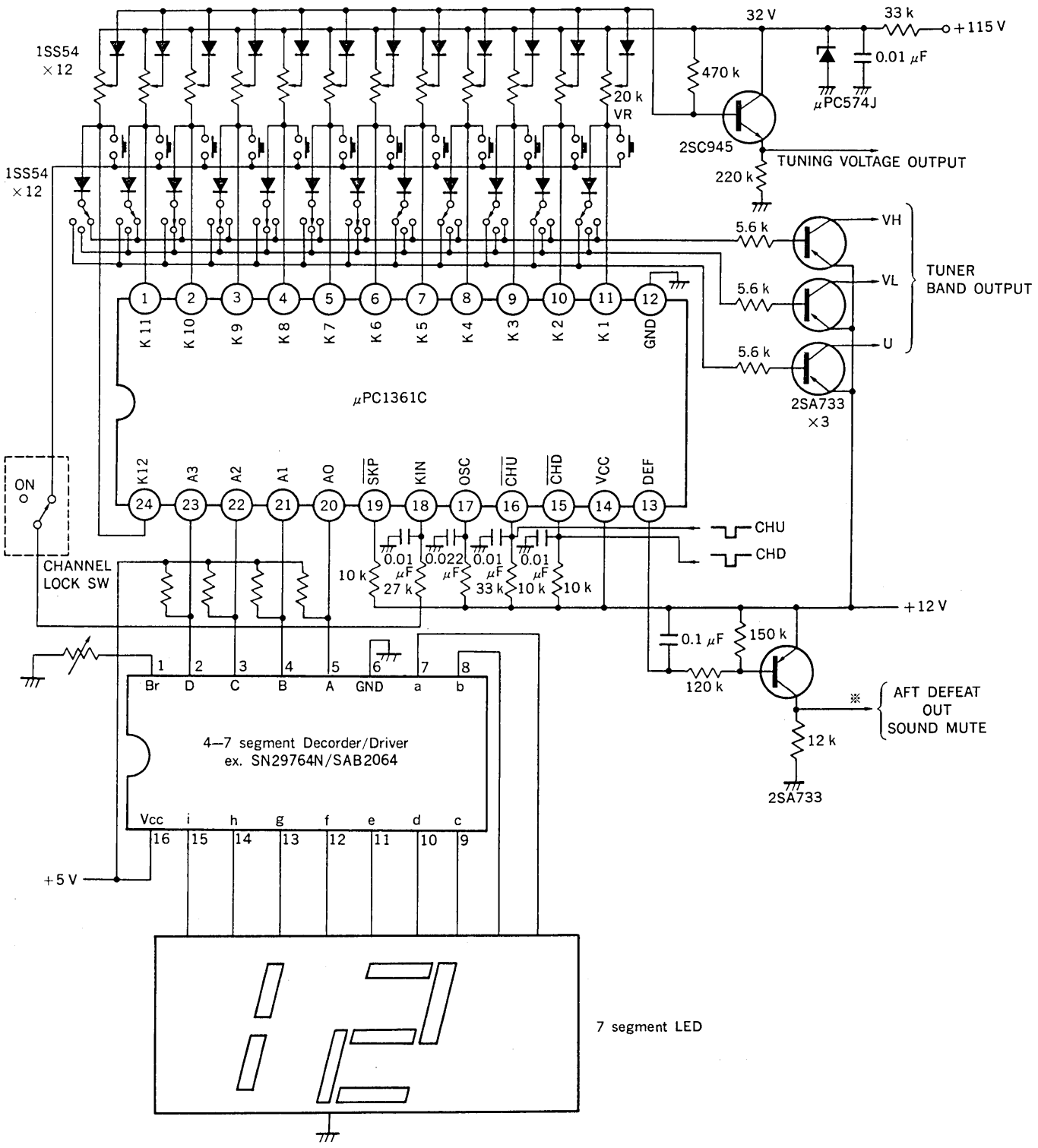
APPLICATION CIRCUIT

12 Position Display/4 bit Encoder Output



APPLICATION CIRCUIT

Example of TV channel selection circuit with 7 segment LED display



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1362C

ELECTRONIC CHANNEL SELECTOR

DESCRIPTION

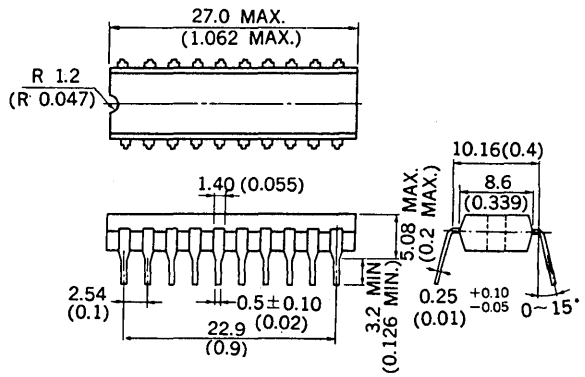
The μPC1362C is an electronic channel selector integrated circuit. It is capable of selecting up to 12 channels. The output terminals are design to permit the direct driving of LED or neon lamps.

This IC consists of Clock Oscillator circuit, Channel Up and Down circuit, Channel skip circuit, 4 bit Up and Down Counter circuit, 1-12 Decoder circuit and 12 channel Output Buffer circuit, all of which are contained in a 20 pins dual in-line package.

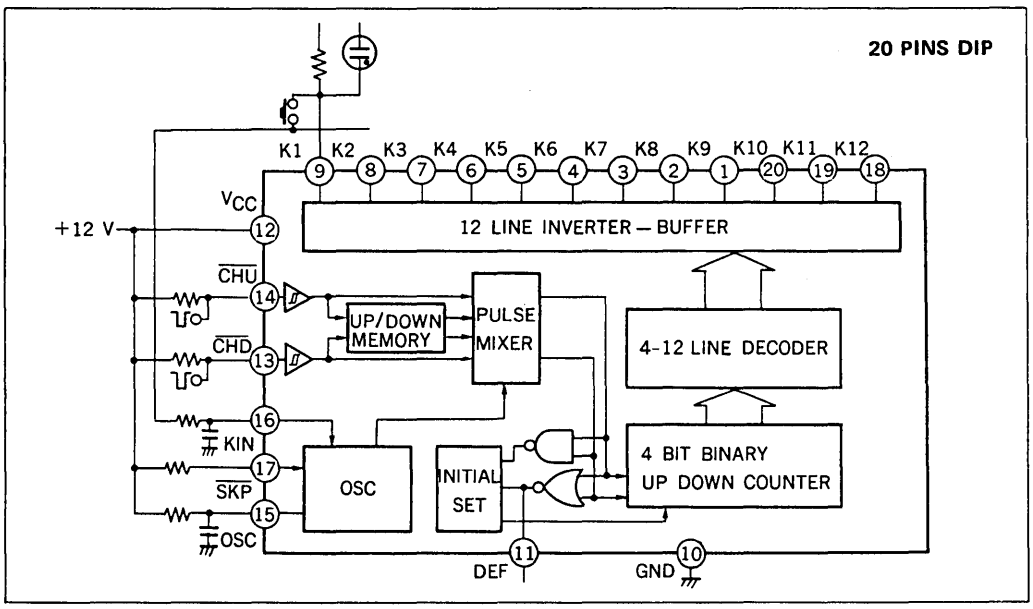
FEATURES

- LED, Neon lamps direct drive.
  I_K=5 mA, V_{kSAT} 150 mV MAX.
- Low power consumption.
  V_{CC}=12 V, I_{CC}=5 mA TYP.
- Up to 12 channel selection.
- Internal schmitt trigger circuit. (CHU, CHD INPUT)
- Power ON initial channel set.
- TV, Radio etc. channel selection use.
- Using with μPD1986C (TX), μPD1937C (RX), direct address remote control system is realized.

PACKAGE DIMENSIONS in millimeters (inches)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25 °C)

Supply Voltage	V_{CC}	15.0	V
Input Current to Channel Selection Circuit	$I_{K1\sim9,\ 18\sim20}$	−5 to 30	mA
Input Current to Control Circuit	$I_{C16,\ 17}$	−5 to 10	mA
Input Current to Control Circuit	I_{C11}	−5 to 30	mA
* Output Voltage to Channel Selection Circuit	$V_{K1\sim9,\ 18\sim20}$	−0.5 to 45	V
* Output Voltage to Control Circuit	V_{11}	−0.5 to 14.4	V
* Input Voltage to Control Circuit	V_{15}	−0.5 to V_{CC}	V
Power Dissipation	P_d	300	mW
Operating Temperature Range	T_{opt}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C

* At V_{CC}=12 V

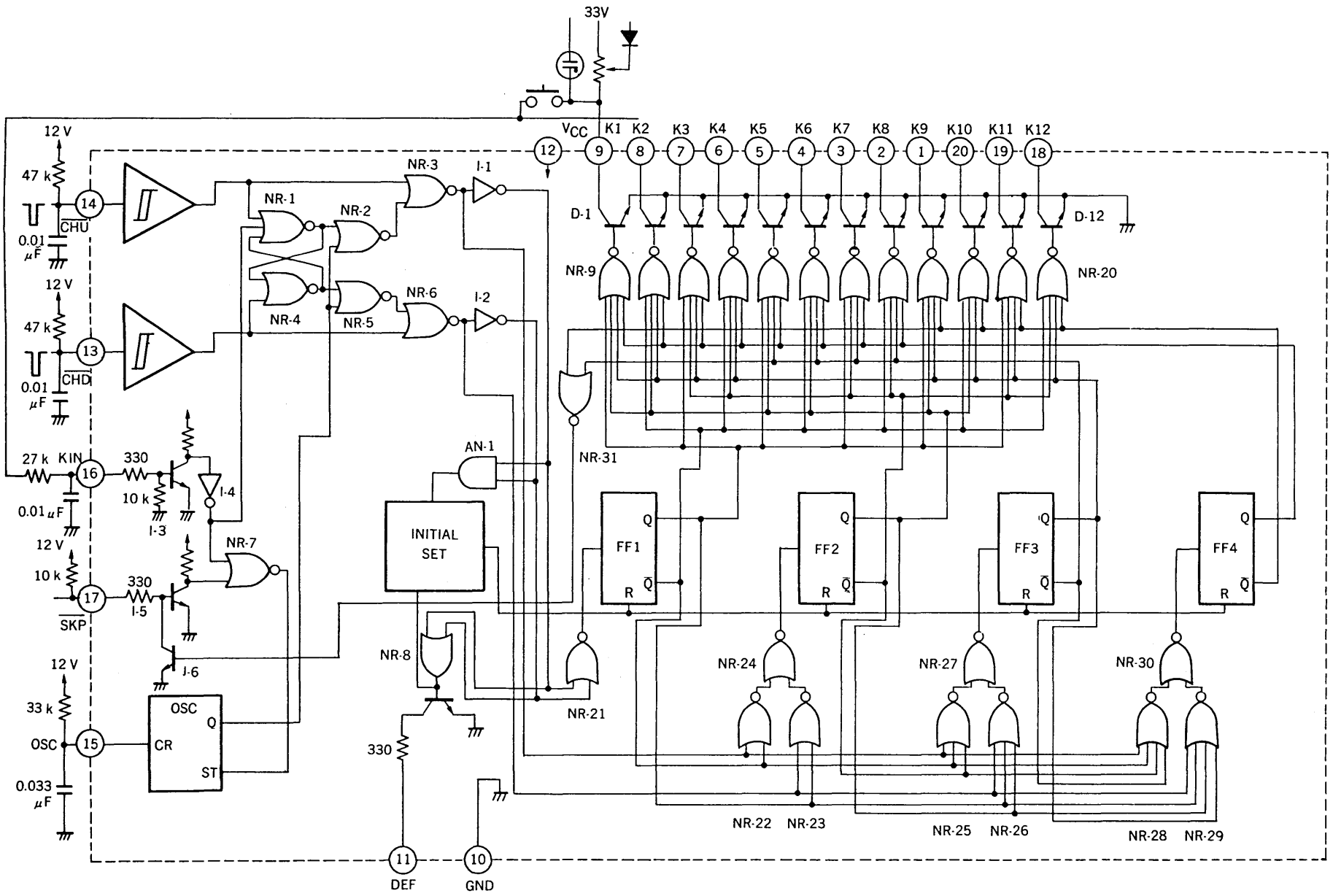
RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	9.6	12.0	14.4	V
Channel Selection Input Current	I_K		5.0		mA
Clock Oscillation Frequency	f_{OSC}		2.0	10.0	kHz

ELECTRICAL CHARACTERISTICS (Ta=25 ±3 °C)

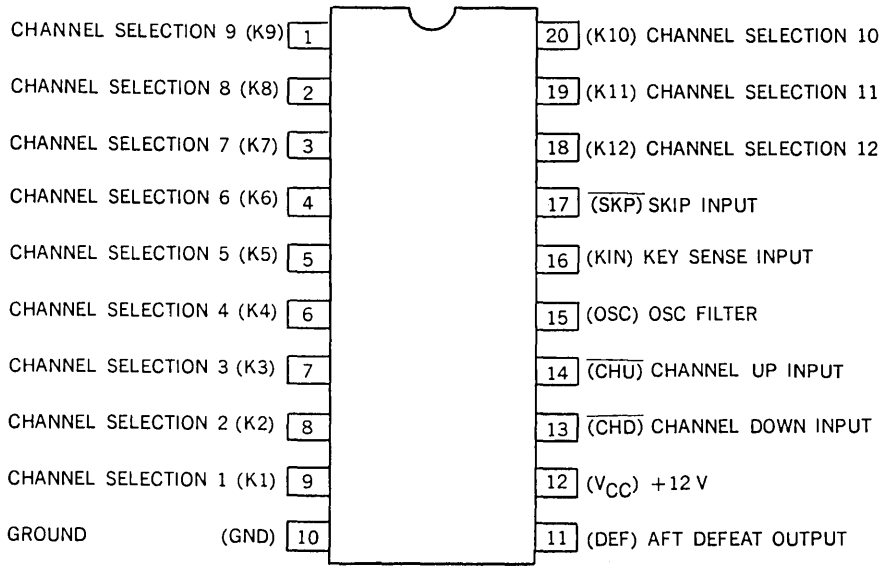
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Current	I_{DD}	2.0	5.0	10.0	mA	V_{CC}=12 V
Channel Selection Saturation Voltage	$V_{OL(K)}$			150	mV	V_{CC}=9.6 V, I_{OL}=5 mA
Channel Selection Leakage Current	$I_{OH(K)}$			10	μA	V_{CC}=14.4 V, V_{OH}=35 V
AFT Defeat Output Voltage	$V_{OL(D)}$			6	V	V_{CC}=9.6 V, I_{OL}=12 mA
AFT Defeat Leakage Current	$I_{OH(D)}$			10	μA	V_{CC}=14.4 V, V_{OH}=14.4 V
Channel Input High Threshold Voltage	$V_{TH(CH)}$	7.2		9.0	V	V_{CC}=12 V
Channel Input Low Threshold Voltage	$V_{TL(CH)}$	5.0		7.0	V	V_{CC}=12 V
Channel Input Leakage Current	$I_{CH(CH)}$	−5			μA	V_{CC}=14.4 V, V_{IL}=0 V
Channel Input Leakage Current	$I_{CH(CH)}$			5	μA	V_{CC}=14.4 V, V_{IH}=14.4 V
Key Input Current	$I_{IH(KI)}$	200			μA	V_{CC}=9.6 V
Key Input Leakage Current	$I_{IL(KI)}$	−10			μA	V_{CC}=14.4 V, V_{IL}=0 V
Skip Input Current	$I_{IH(SK)}$	50			μA	V_{CC}=9.6 V
Skip Input Leakage Current	$I_{IL(SK)}$	−5			μA	V_{CC}=14.4 V, V_{IL}=0 V
OSC Input Current	$I_{IH(OSC)}$	1.5		3.0	mA	V_{CC}=9.6 V, V_{IH}=4 V
Channel Hold Voltage	V_{HOLD}	6.5			V	
OSC Frequency	f_{OSC}	1.0	2.0	3.0	kHz	V_{CC}=12 V, R=33 kΩ, C=0.033 μF

EQUIVALENT CIRCUIT



Logic Blocks consist of PMOS technology
Output,Input circuits consist of Bipolar technology.

CONNECTION DIAGRAM (Top View)



PIN FUNCTION

K1 ~ 12 (#9 ~ 1, #18 ~ 20) CHANNEL SELECTION OUTPUT

These are the output terminals constructed of collector-opened transistors, so they can drive potentiometers and indicators, and key output. They have saturation voltage of 150 mV at I_K = 5 mA, so they can drive neon or LED lamps directly.

GND (#10) GROUND

DEF (#11) AFT DEFEAT OUTPUT

This terminal is made of open collector transistor output through a resistor of 330 Ω. It is used for AFT (Automatic Fine Tuning ····· TV use) defeat, sound muting and LED indicate erasing.

V_{CC} (#12) +12 V (9.6 ~ 14.4 V)

CHD (#13) CHANNEL DOWN INPUT

Usually pulled up to V_{CC} through a resistor, Channel selector changes at positive going edge of input signal of this terminal and the channel selector works orderly from K12 to K1.

CHU (#14) CHANNEL UP INPUT

Usually pull up to V_{CC} through a resistor, Channel selector changes at positive going edge of input signal of this terminal and the channel selector works orderly from K1 to K12. If CHU and CHD terminals put down to ground at same time, initial channel is selected. So, it is very useful to remote control operation use. These terminals include schmitt trigger circuit. If these terminals are not used as remote control operation, connect these terminals to V_{CC} directry.

OSC (#15) OSC FILTER

When a Channel key is pushed or skip function is operated, oscillator contained in this IC oscillate with C, R connected to this terminal. Typical oscillation frequency is 2 kHz. (R=33 kΩ, C=0.033 μF)

KIN (#16) KEY INPUT

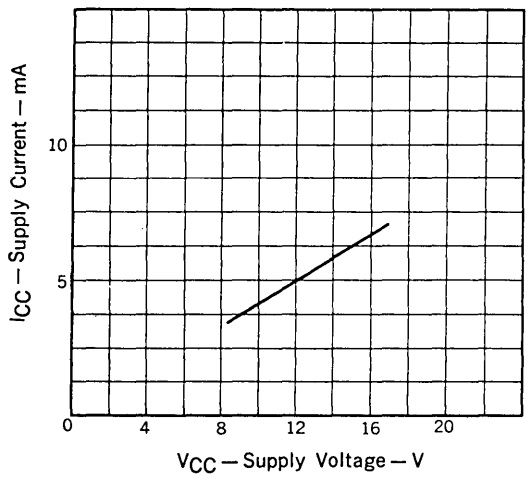
When channel selection key is pushed, as pushed channel is not selected, "High" level of signal is applied to this terminal through a potentiometer resistor. Then channel selector scans terminals of K1 ~ K12. And when sense up this terminal, it pull down the voltage of this terminal and stop the scanning.

SKP (#17) SKIP INPUT

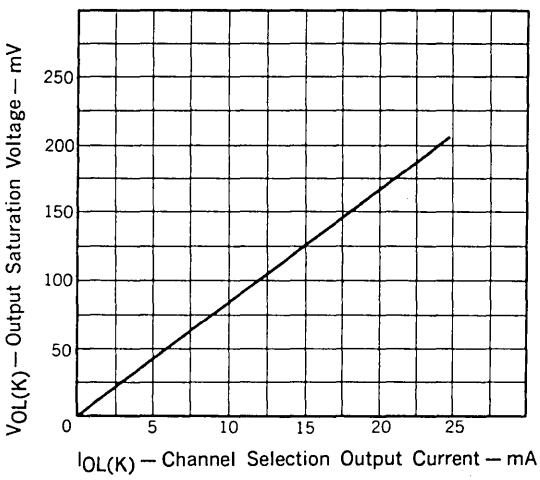
Usually pull up to V_{CC} through resistor. When only 10 channels are used, conect open channel outputs (K11, K12) to this terminal with CR filter.

CHARACTERISTICS

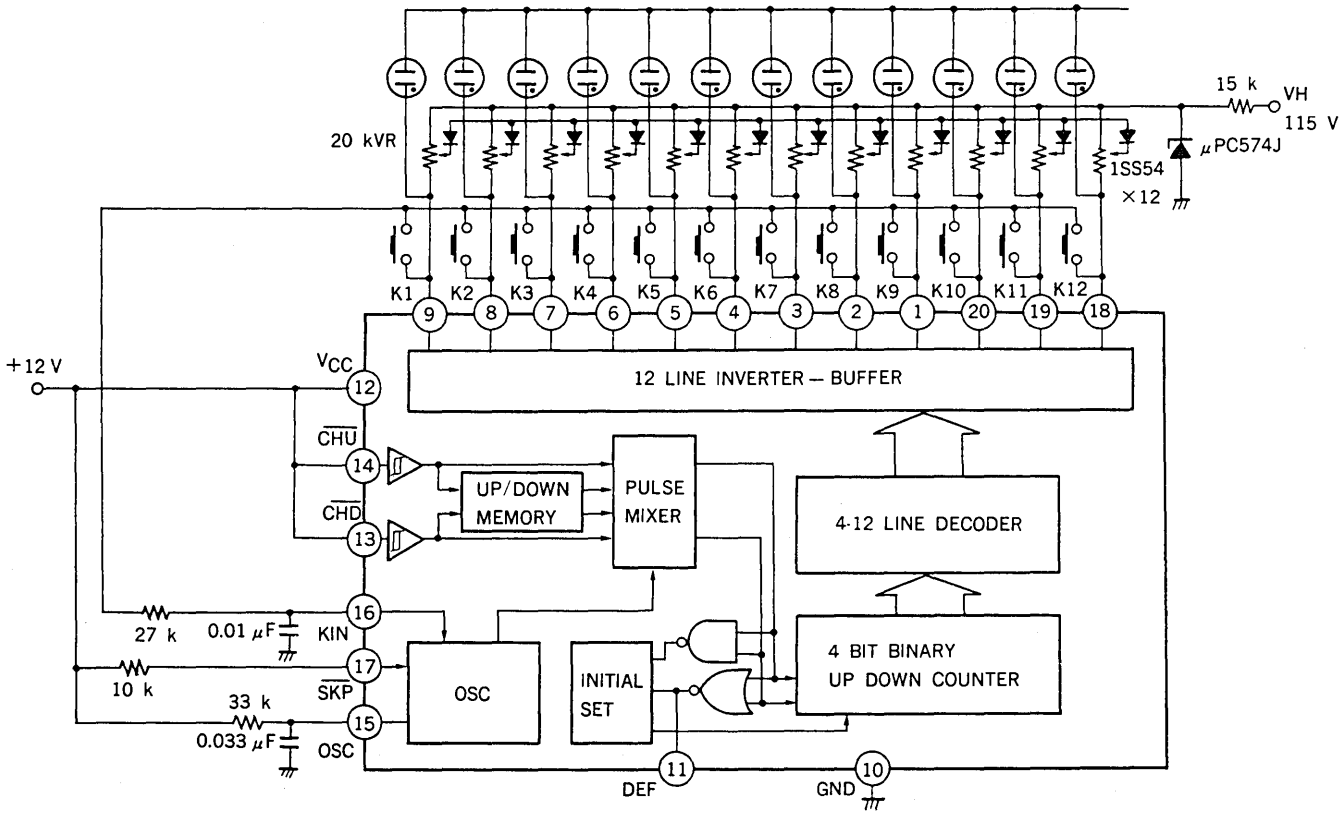
SUPPLY CURRENT vs. SUPPLY VOLTAGE



CHANNEL SELECTION SATURATION VOLTAGE CHARACTERISTIC

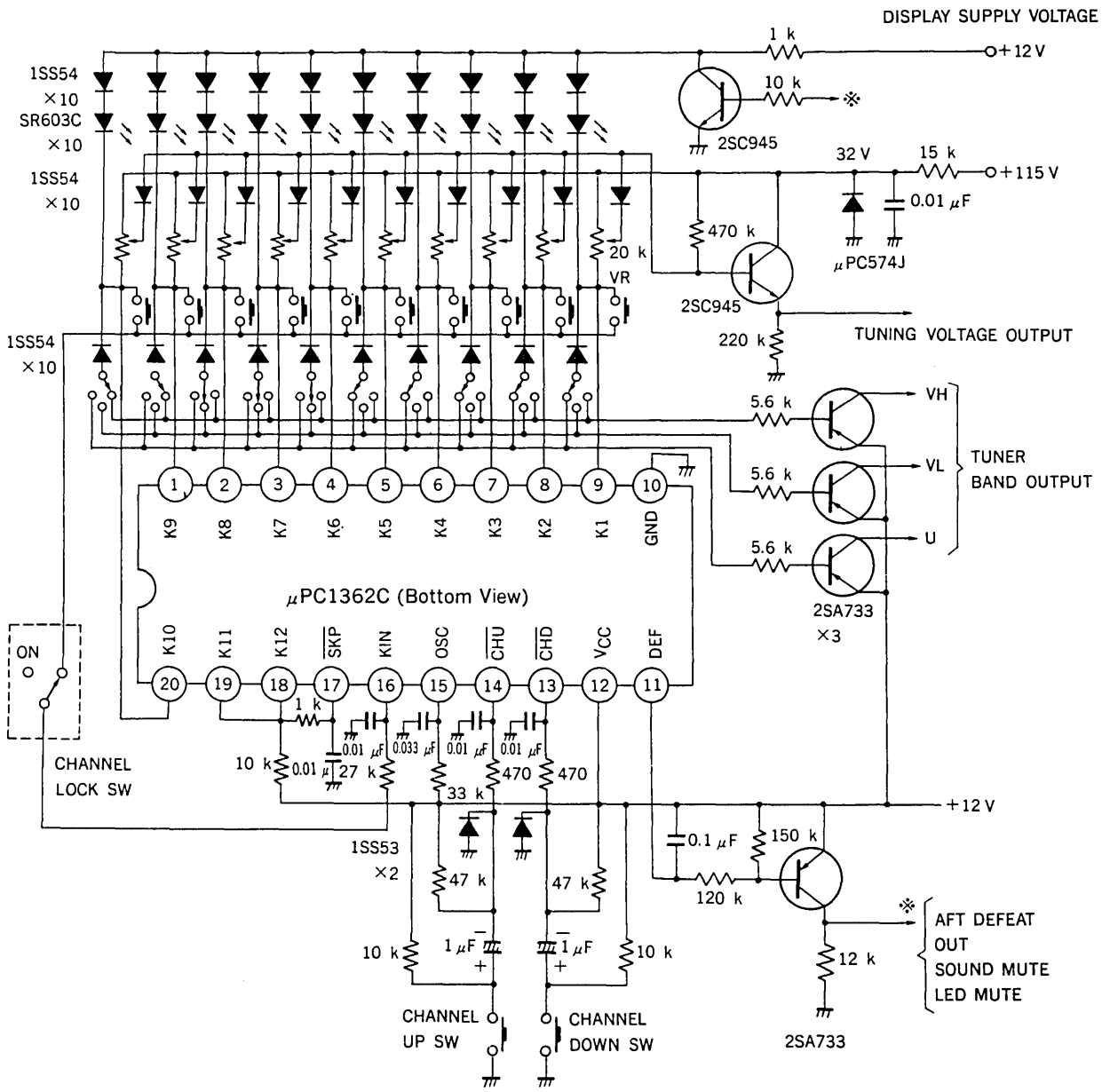


APPLICATION CIRCUIT 1



APPLICATION CIRCUIT 2

EXAMPLE OF TV CHANNEL SELECTION
10 POSITION SELECTION CIRCUIT (2 POSITION IS SKIPED)



BIPOLAR ANALOG INTEGRATED CIRCUIT
μPC1363C

ELECTRONIC CHANNEL SELECTOR

DESCRIPTION

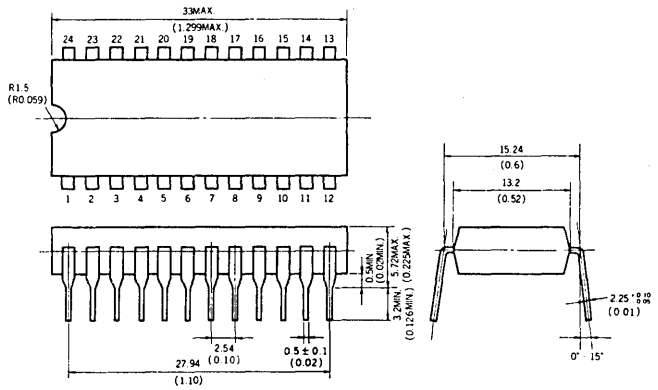
The μPC1363C is an electronic channel selector integrated circuit. It is capable of selecting up to 16 channels. The output terminals are design to permit the direct driving of LED lamps or neon tubes.

This IC consists of Clock Oscillator circuit, Channel Up and Down circuit, Channel skip circuit, 4 bit Up and Down Counter circuit, 1-16 Decoder circuit and 16 channel Output Buffer circuit, all of which are contained in a 24 pins dual in-line package.

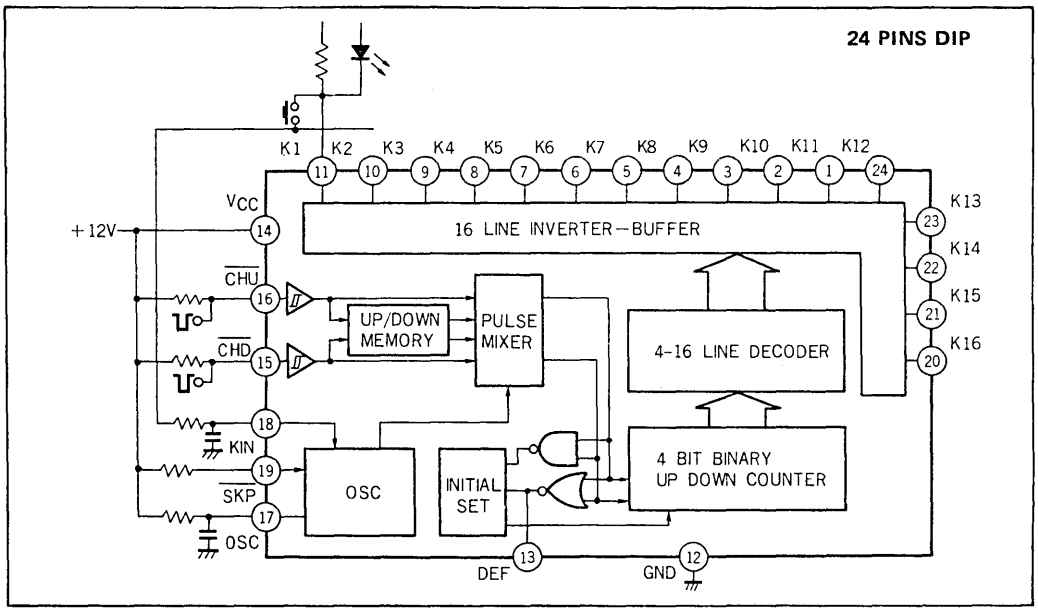
FEATURES

- LED direct drive.
  1k=15mA, V_{kSAT} 150mV MAX.
- Low power consumption.
  V_{CC}=12V, I_{CC}=15mA TYP.
- Up to 16 channel selection.
- Internal schmitt trigger circuit. (CHU, CHD INPUT)
- Power ON initial channel set.
- μPC1360C pin compatible. (V_{CC}=6V)
- TV, Radio etc. channel selection use.
- Using with μPD1986C (TX), μPD1937C (RX), direct address remote control system is realized.

PACKAGE DIMENSIONS in millimeters (inches)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Supply Voltage	V_{CC}	15.0	V
Input Current to Channel Selection Circuit	$I_{K1\sim11,20\sim24}$	−5 to 50	mA
Input Current to Control Circuit	$I_{C15\sim19}$	−5 to 10	mA
Input Current to Control Circuit	I_{C13}	−5 to 20	mA
* Output Voltage to Channel Selection Circuit	$V_{K1\sim11,20\sim24}$	−0.5 to 50	V
* Output Voltage to Control Circuit	V_{13}	−0.5 to 14.4	V
* Input Voltage to Control Circuit	V_{17}	−0.5 to V_{CC}	V
Power Dissipation	P_d	350	mW
Operating Temperature Range	T_{opt}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C

* At V_{CC} = 12V

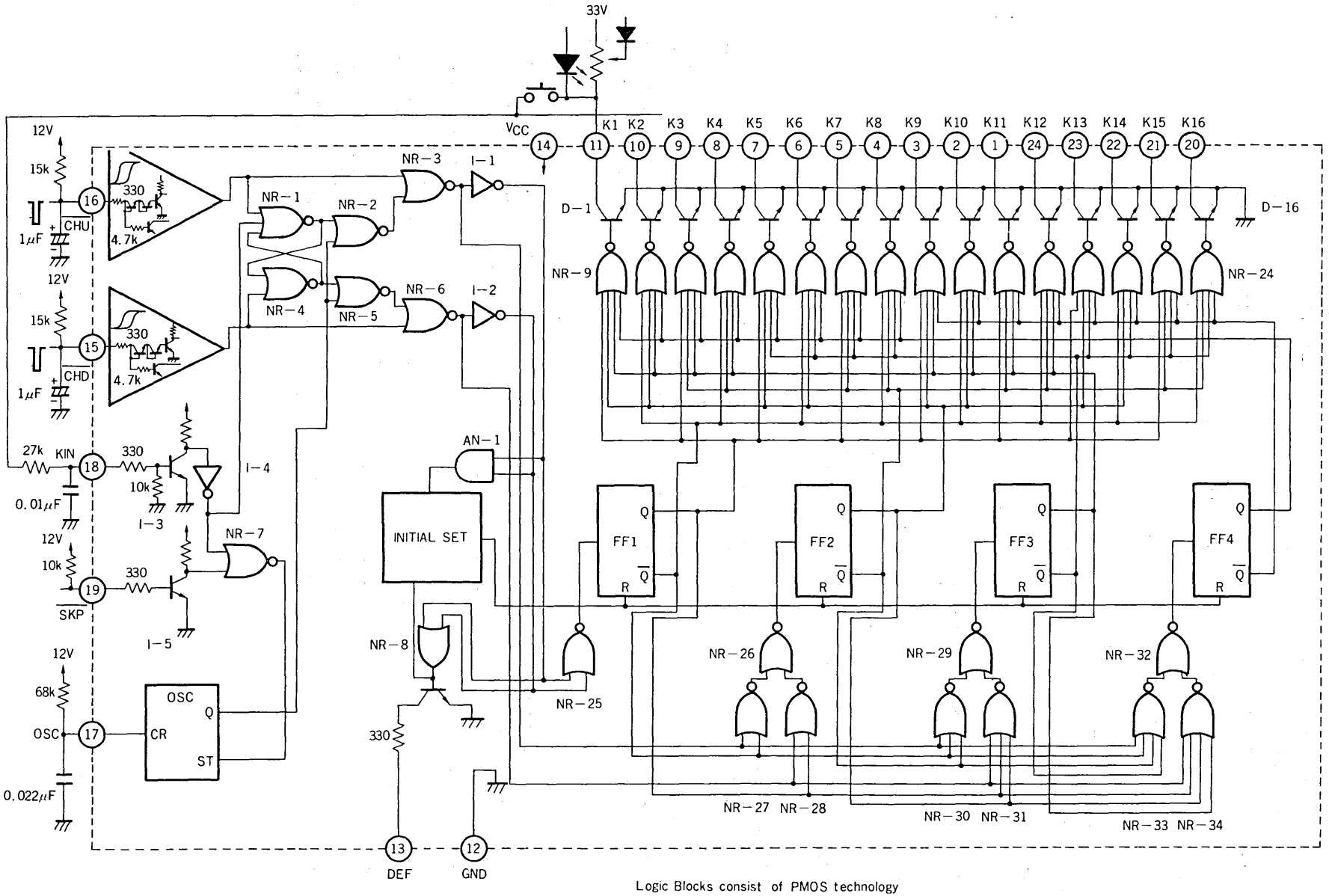
RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	9.6	12.0	14.4	V
Channel Selection Input Current	I_K		15.0		mA
Clock Oscillation Frequency	f_{OSC}		2.0	10.0	kHz

ELECTRICAL CHARACTERISTICS (Ta=25 ±3°C)

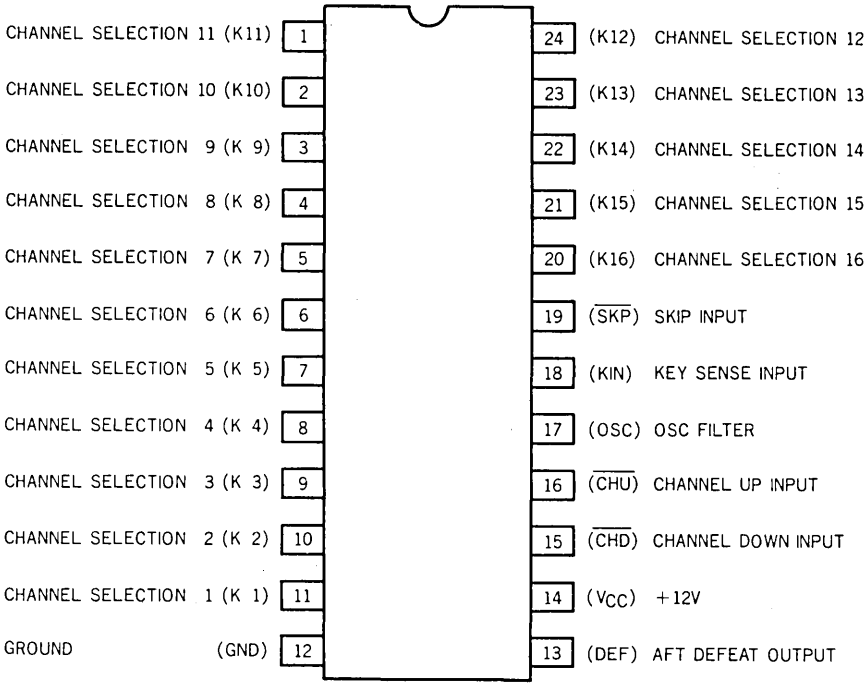
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Current	I_{DD}	7.0	15.0	22.0	mA	V_{CC}=12V
Channel Selection Saturation Voltage	$V_{OL(K)}$			150	mV	V_{CC}=9.6V, I_{OL}=15mA
Channel Selection Leakage Current	$I_{OH(K)}$			10	μA	V_{CC}=14.4V, V_{OH}=35V
AFT Defeat Output Voltage	$V_{OL(D)}$			6	V	V_{CC}=9.6V, I_{OL}=12mA
AFT Defeat Leakage Current	$I_{OH(D)}$			10	μA	V_{CC}=14.4V, V_{OH}=14.4V
Channel Input High Threshold Voltage	$V_{TH(CH)}$	3.5		7.0	V	V_{CC}=12V, R_i=15kΩ
Channel Input Low Threshold Voltage	$V_{TL(CH)}$	1.5		2.5	V	V_{CC}=12V, R_i=15kΩ
Channel Input Leakage Current	$I_{CH(CH)}$	−5			μA	V_{CC}=14.4V, V_{IL}=0V
Key Input Current	$I_{IH(KI)}$	200			μA	V_{CC}=9.6V
Key Input Leakage Current	$I_{IL(KI)}$	−10			μA	V_{CC}=14.4V, V_{IL}=0V
Skip Input Current	$I_{IH(SK)}$	50			μA	V_{CC}=9.6V
Skip Input Leakage Current	$I_{IL(SK)}$	−5			μA	V_{CC}=14.4V, V_{IL}=0V
OSC Input Current	$I_{IH(OSC)}$	1.5		3.0	mA	V_{CC}=9.6V, V_{IH}=4V
OSC Leakage Current	$I_{IL(OSC)}$			10	μA	V_{CC}=14.4V, V_{IL}=1.0V
OSC Frequency	f_{OSC}	1.5		2.5	kHz	V_{CC}=12V, R=68kΩ, C=0.022μF

EQUIVALENT CIRCUIT



Logic Blocks consist of PMOS technology
Output, Input and OSC consist of Bipolar technology.

CONNECTION DIAGRAM (Top View)



PIN FUNCTION

K1～16 (#11～1, #24～20) CHANNEL SELECTION OUTPUT

These are the output terminals constructed of collector-opened transistors, so they can drive potentiometers and indicators, and key output. They have saturation voltage of 150mV at I_K = 15mA, so they can drive LEDs directly.

GND (#12) GROUND

DEF (#13) AFT DEFEAT OUTPUT

This terminal is made of open collector transistor output through a resistor of 330Ω. It is used for AFT (Automatic Fine Tuning ····· TV use) defeat, sound muting and LED indicate erasing.

V_{CC} (#14) +12V (9.6～12V)

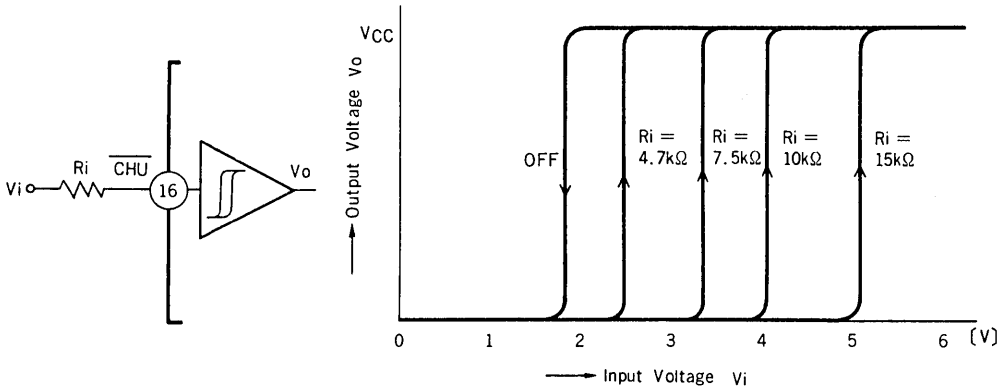
CHD (#15) CHANNEL DOWN INPUT

Usually pulled up to V_{CC} through a resistor, Channel selector changes at positive going edge of input signal of this terminal and the channel selector works orderly from K16 to K1.

CHU (#16) CHANNEL UP INPUT

Usually pull up to V_{CC} through a resistor, Channel selector changes at positive going edge of input signal of this terminal and the channel selector works orderly from K1 to K16. If CHU and CHD terminals put down to ground at same time, initial channel is selected. So, it is very useful to power on channel set or remote control operation use.

These terminals include schmitt trigger circuit and this hysteresis level is controled by external resistors.



CHU, CHD Input Schmitt Characteristic

OSC (#17) OSC FILTER

When a Channel key is pushed or skip function is operated, oscillator contained in this IC oscillate with C, R connected to this terminal. Typical oscillation frequency is 2kHz. (R = 68k, C = 0.022μF)

KIN (#18) KEY INPUT

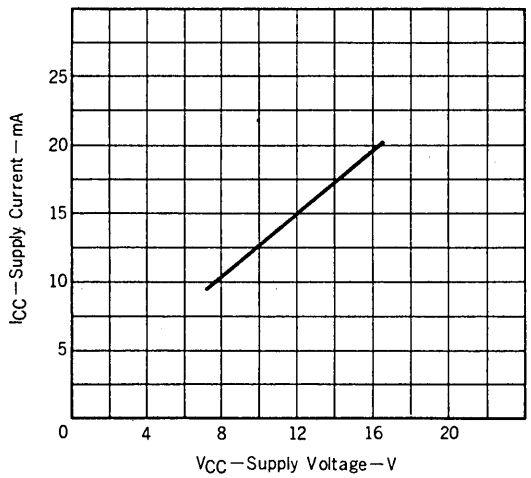
When channel selection key is pushed, as pushed channel is not selected, "High" level of signal is applied to this terminal through a potentiometer. Then channel selector scans terminals of K1 ~ K16. And when sense up this terminal, it pull down the voltage of this terminal and stop the scanning.

SKP (#19) SKIP INPUT

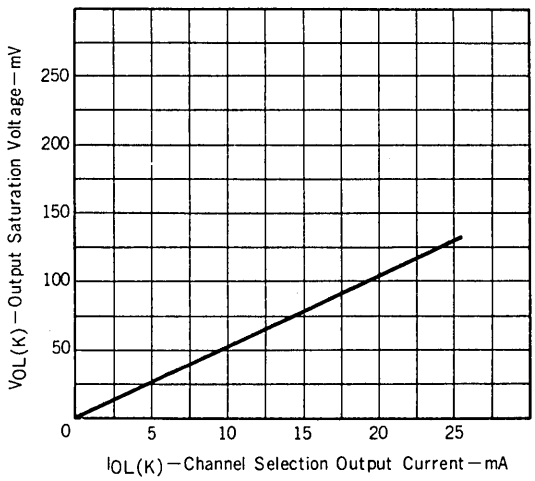
Usually pull up to V_{CC} through resistor. When only 12 channels are used, conect terminals (K13 ~ K16) to this terminal.

CHARACTERISTICS

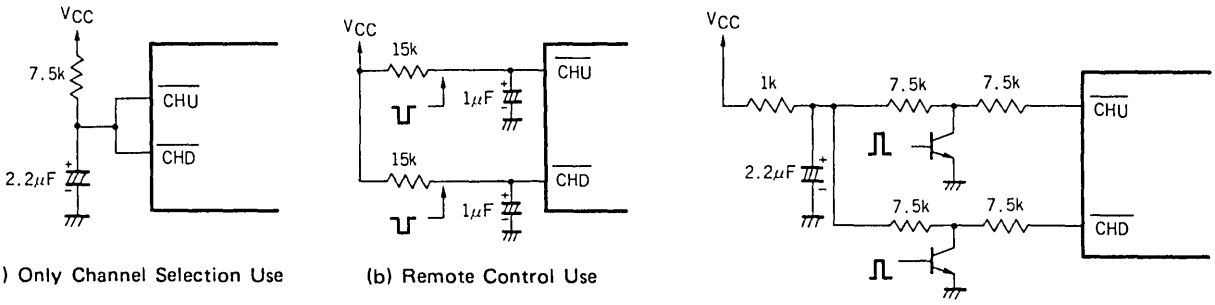
SUPPLY CURRENT vs. SUPPLY VOLTAGE



CHANNEL SELECTION SATURATION VOLTAGE CHARACTERISTIC



INITIAL CHANNEL SET and REMOTE CONTROL CIRCUIT

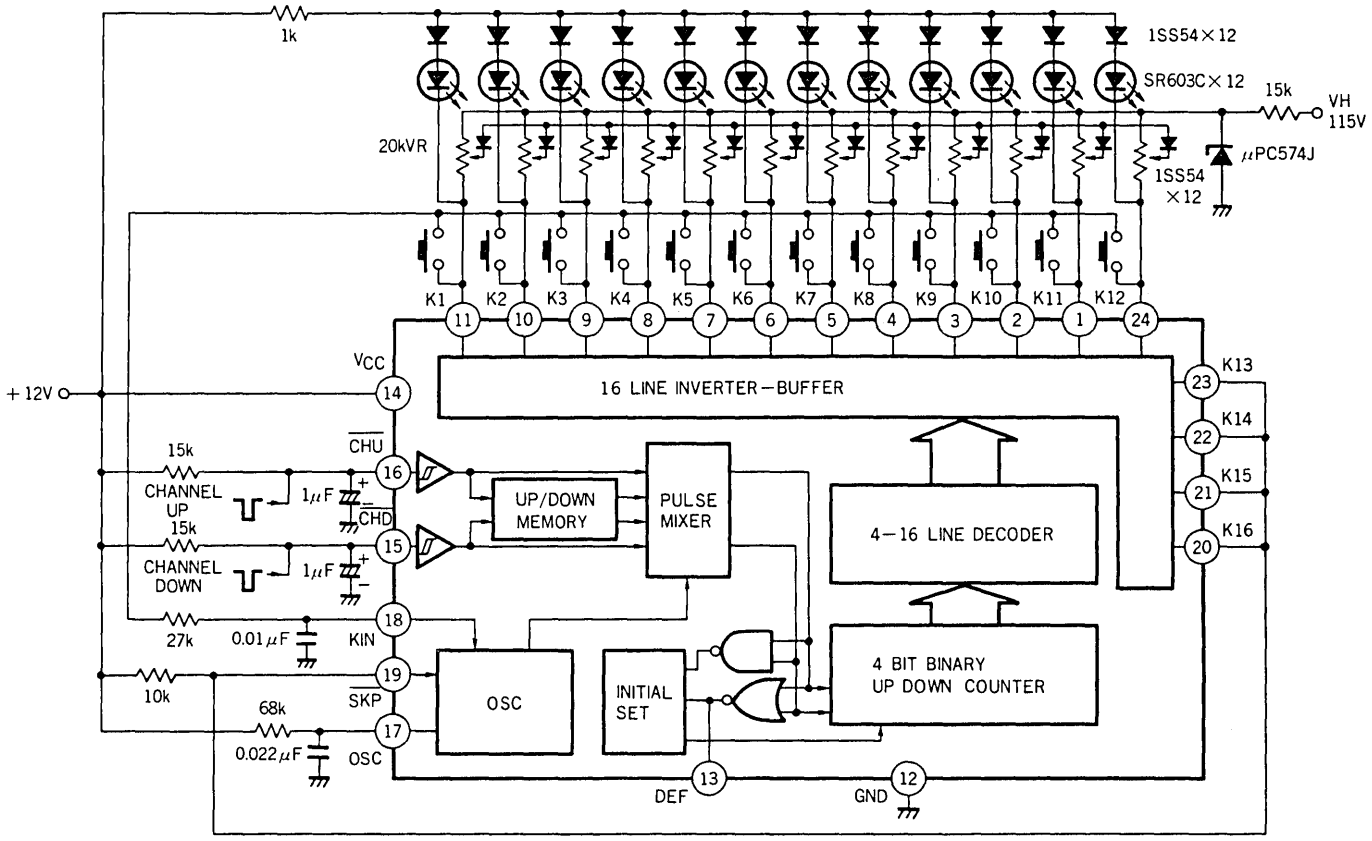


(a) Only Channel Selection Use

(b) Remote Control Use

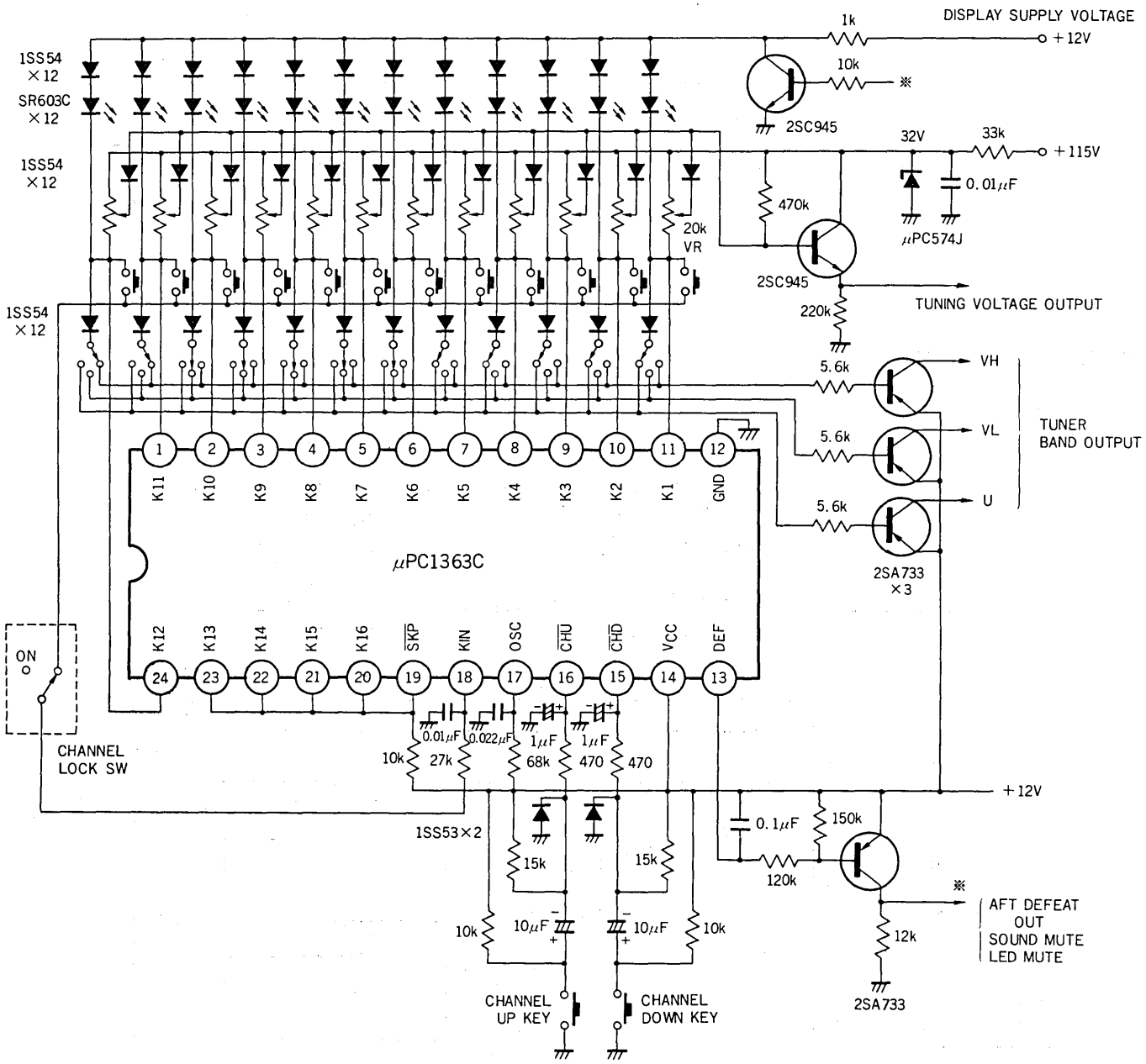
(c) Remote Control Use (Short Pulse Width)

APPLICATION CIRCUIT 1



APPLICATION CIRCUIT 2

EXAMPLE OF TV CHANNEL SELECTION
12 POSITION SELECTION CIRCUIT (4 POSITION IS SKIPED)



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1373H

REMOTE CONTROL PREAMPLIFIER

DESCRIPTION

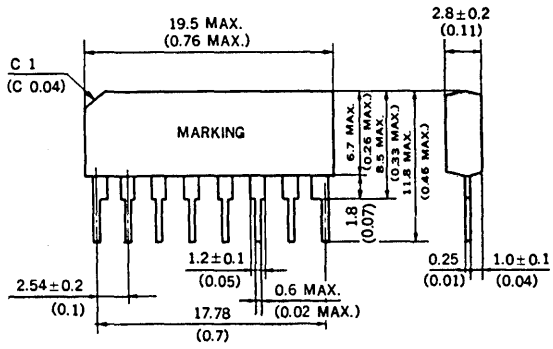
The μPC1373H is a silicon monolithic integrated circuit designed for a remote control preamplifier of infrared signals. This device has features of low power, high sensitivity and wide supply voltage.

FEATURES

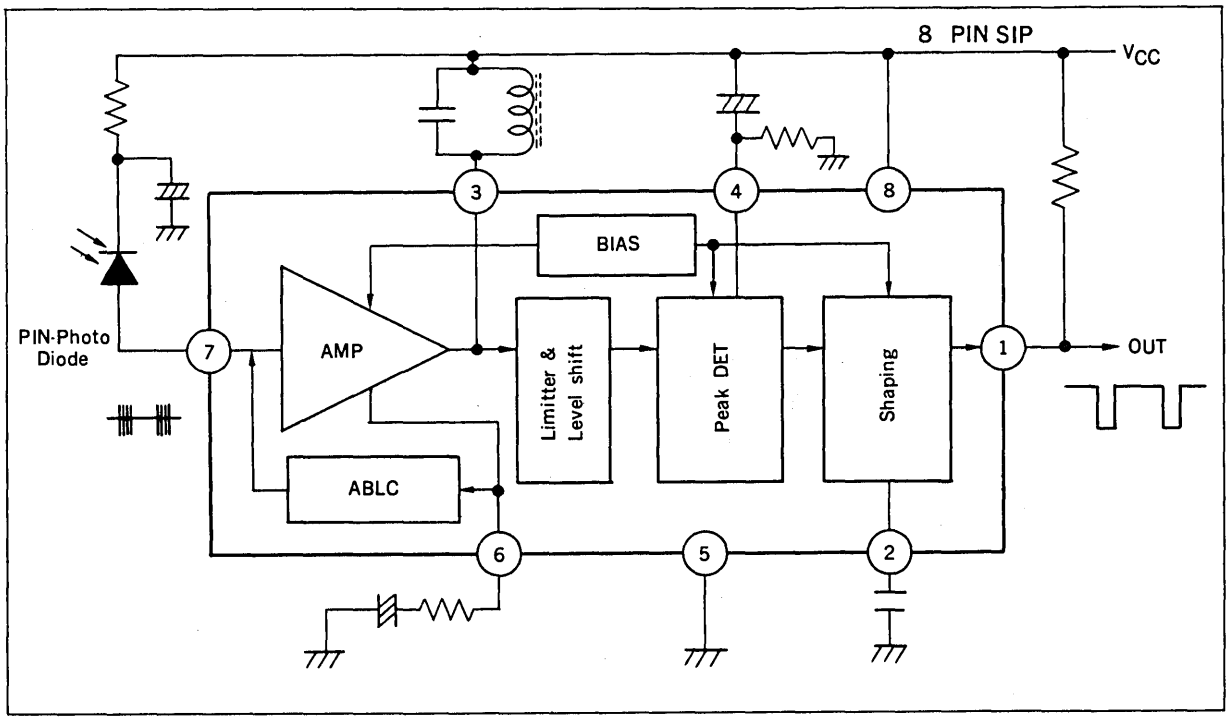
- Wide operation Voltage ..... V_{CC} = 6 to 14.4 V
- Low Power Consumption ..... I_{CC} = 2.5 mA TYP.
- High Input Sensitivity ..... 50 μVp-p TYP.
- Peak Detector
- Small Size Package 8 pin-SIP
- Minimum number of External parts required
- Designed for Use with the μPD1913C, 1943G Remote Control Transmitter IC.

PACKAGE DIMENSIONS

in millimeters (inches)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Supply Voltage	V_{CC}	15	V
Power Dissipation	P_d	270	mW
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

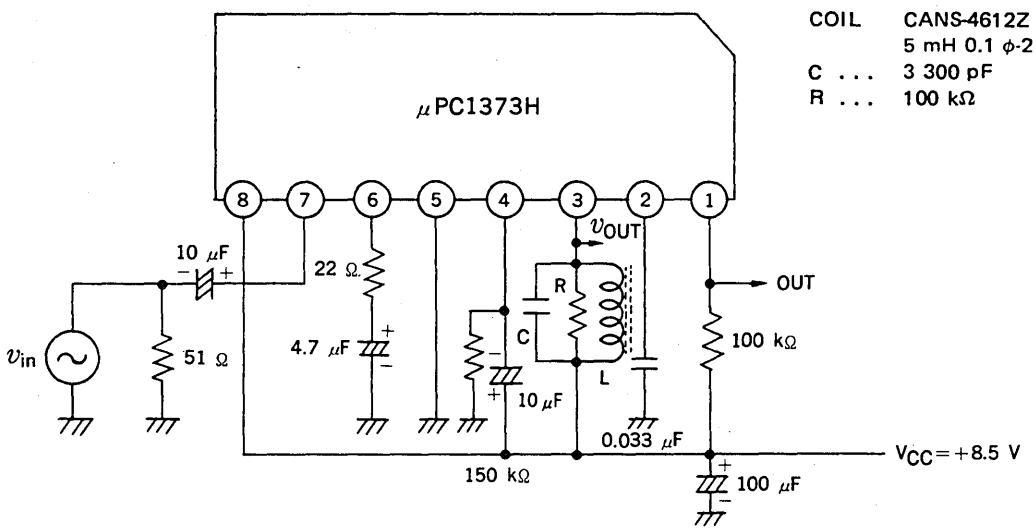
RECOMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power Supply	V_{CC}	6.0	8.5	14.4	V
Input Frequency	f_{in}	30		50	kHz

ELECTRICAL CHARACTERISTICS (Ta = 25 °C, V_{CC} = 8.5 V, f_{in} = 40 kHz)

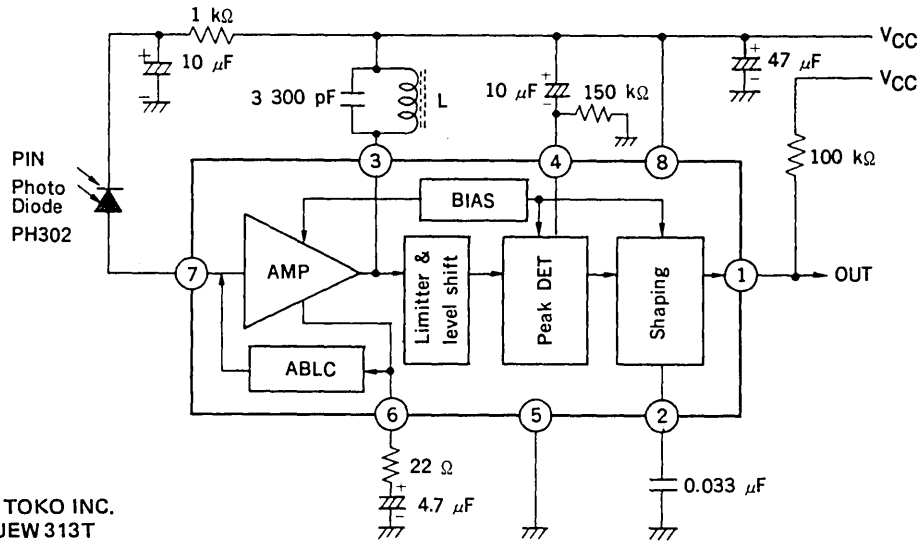
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Current	I_{CC}	1.5	2.5	3.5	mA	
Input Terminal Voltage	$V_{IN\ 1}$	2.1	2.6	3.1	V	
Input Terminal Voltage	$V_{IN\ 2}$	3.4	4.1	4.9	V	I_{in} = 70 μA
1st Stage Voltage Gain	A_{vL}		60		dB	#7 − #3, v_{out} = 500 mVp-p
Detection Input Voltage	v_{in}		50	100	μV	
Input Impedance	r_{in}	40	60	80	kΩ	
Output Voltage	V_{OL}			0.5	V	I_{OL} = 0.1 mA, v_{in} = 1 mVp-p
Output Leak Current	I_{OH}			2	μA	V_{OH} = 14.4 V
Noise		Output Terminal is not fall.				Input Open

TEST CIRCUITS



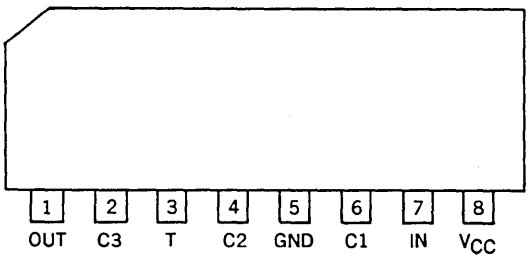
COIL CANS-4612Z TOKO INC.
5 mH 0.1 φ-2 UEW 303T
C ... 3 300 pF
R ... 100 kΩ

STANDARD APPLICATION



COIL 126LNS-6285Z TOKO INC.
5 mH 0.08 φ-2 UEW 313T

CONNECTION DIAGRAM



TERMINAL			
1	OUT	Output
2	C3	Integral Capacitor
3	T	Tuning Coil
4	C2	Peak Hold Capacitor
5	GND	Ground
6	C1	By-pass Capacitor
7	IN	Input
8	V_{CC}	Power Supply

PIN FUNCTION

○ V_{CC} Power Supply . . . . . (#8)

Operation voltage is 6.0 to 14.4 V.

○ IN Input . . . . . (#7)

This input impedance is 60 kΩ typical.

This input has ABLC (Automatic Bias Level Control) circuit for not saturated by violent light, so this terminal voltage is always fixed.

○ T Tuning coil . . . . . (#3)

○ C1 By-pass capacitor . . . (#6)

This 1st amplifier has gain of 60 dB and this gain is determined of impedance of coil and external resistor $R_{\#6}$

$$A_{vL} = \frac{Z_L}{R_{\#6}}$$

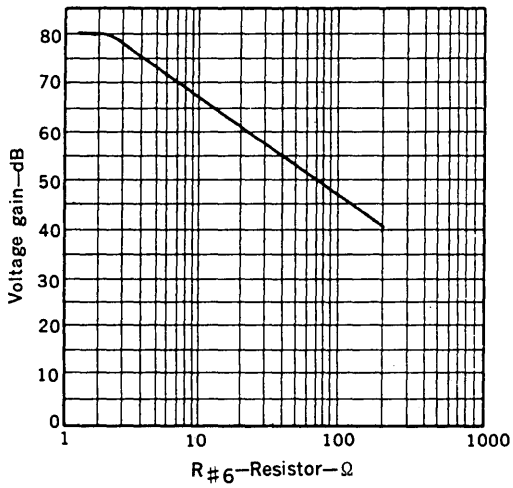


Fig. 1 1st stage amplitude gain

○ C2 Peak hold capacitor . . (#4)

The signal of tuning coil terminal is detected by peak detector circuit. In this case, detecting level depend on input signal strength, so noise wave is suppressed.
Time constant of peak hold is changed by capacitor $C_{\#4}$, and sensitivity is adjusted by resistor $R_{\#4}$. (see Fig. 2)

external resistor $R_{\#4}$

V_{CC} = 12 V . . . 220 kΩ
= 10 V . . . 160 kΩ
= 8.5 V . . . 150 kΩ

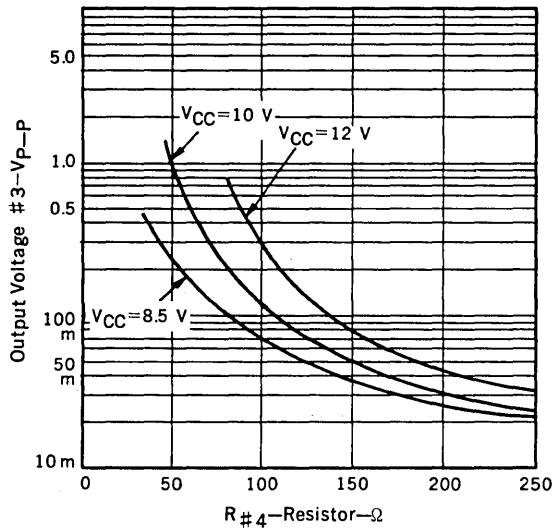


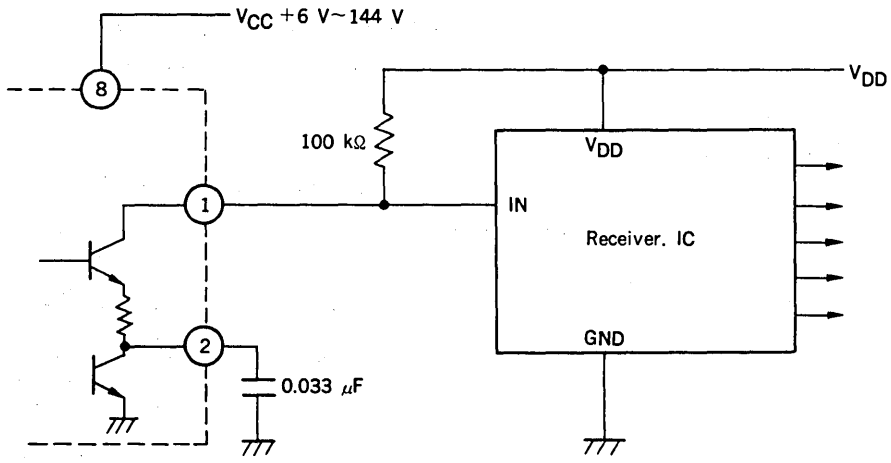
Fig. 2 Sensitivity of peak detector characteristic

○ C3 Integral Capacitor . . . (#2)

Carrier wave through peak detector is integrated by this capacitor.
This time constant is determined of external resistor $R_{\#1}$ and this capacitor $C_{\#2}$.

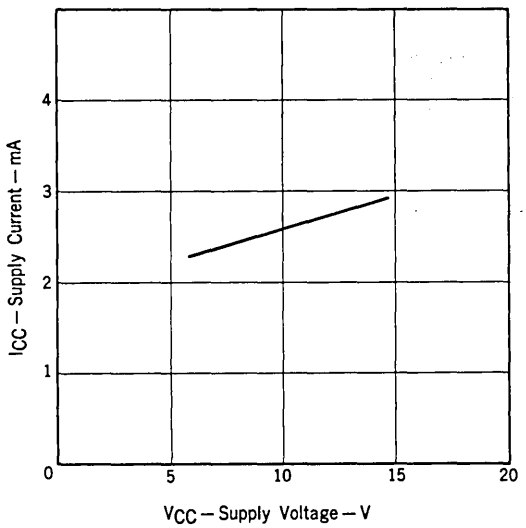
○ OUT Output . . . . . (#1)

Active Low output. This terminal is made of open collector transistor.

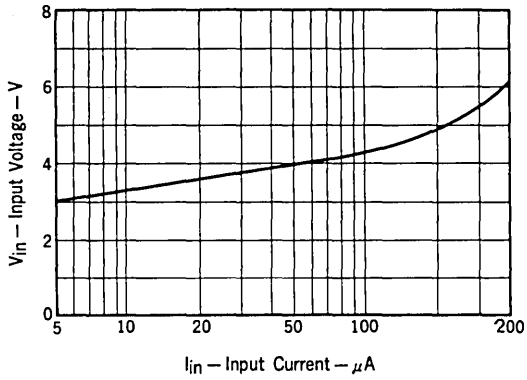


CHARACTERISTIC

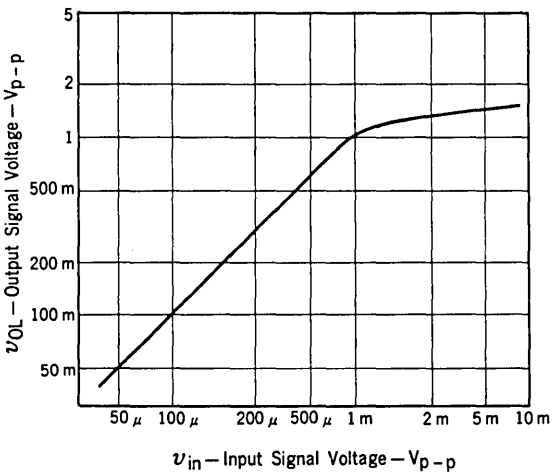
$V_{CC}-I_{CC}$ Characteristic



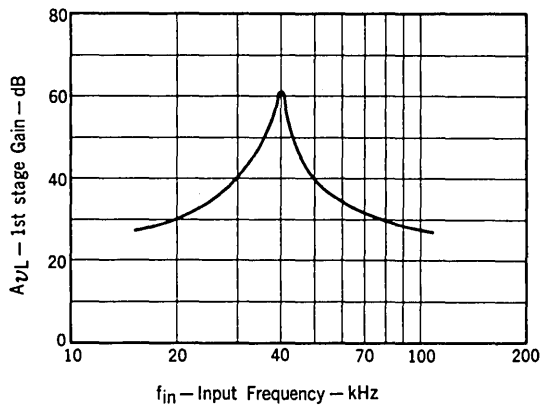
ABLC $I_{in}-V_{in}$ Characteristic



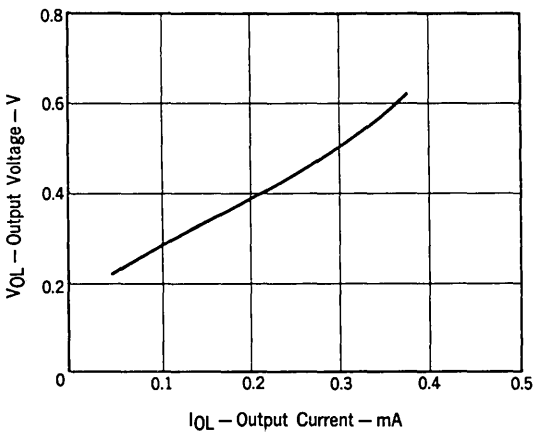
1st Stage $v_{in}-v_{OL}$ Characteristic



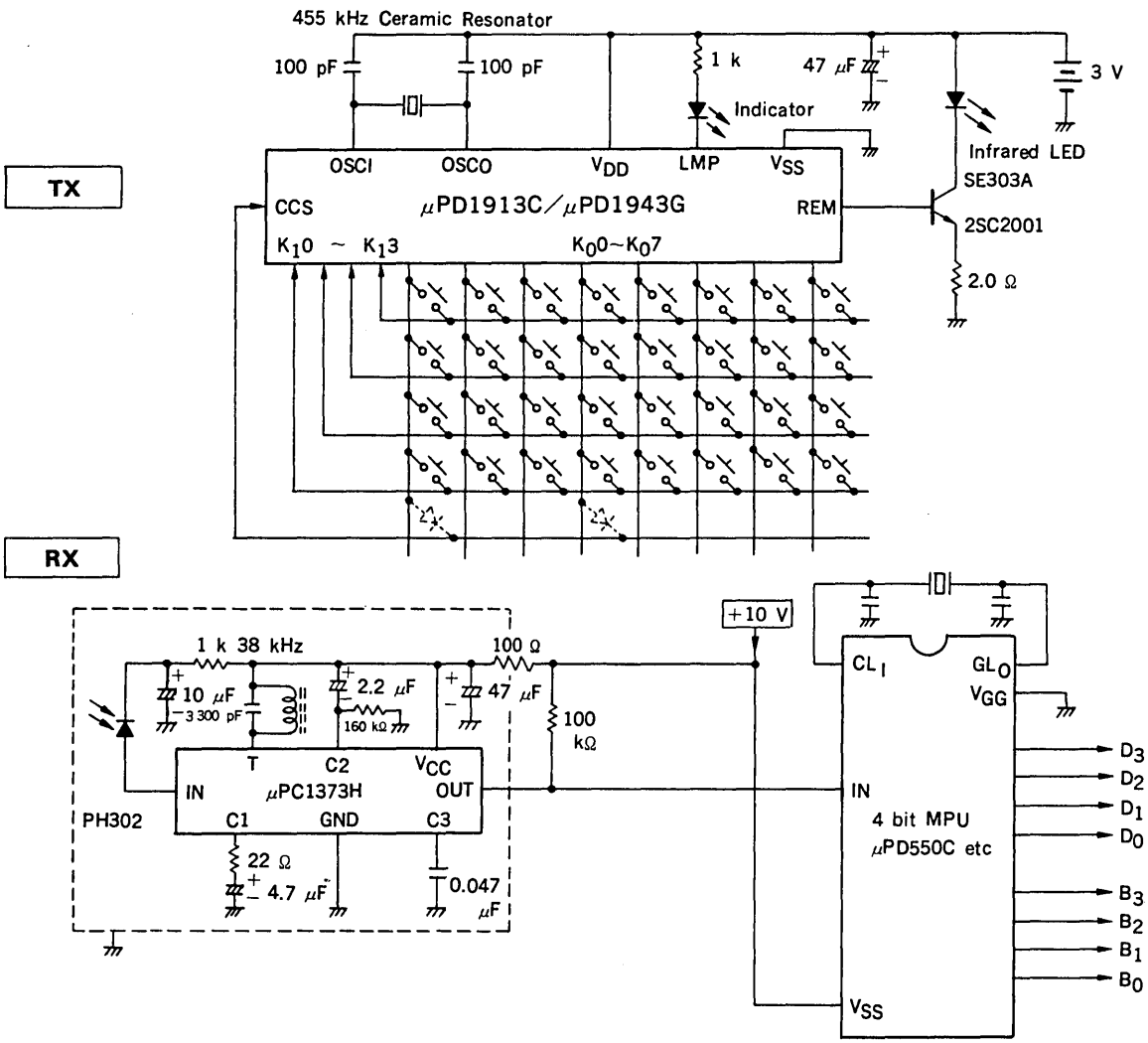
1st Stage $f_{in}-A_{vL}$ Characteristic



Output Saturation Voltage



APPLICATION



MOS DIGITAL INTEGRATED CIRCUITS

μPD1913C, μPD1943G

REMOTE CONTROL TRANSMITTER
CMOS LSI

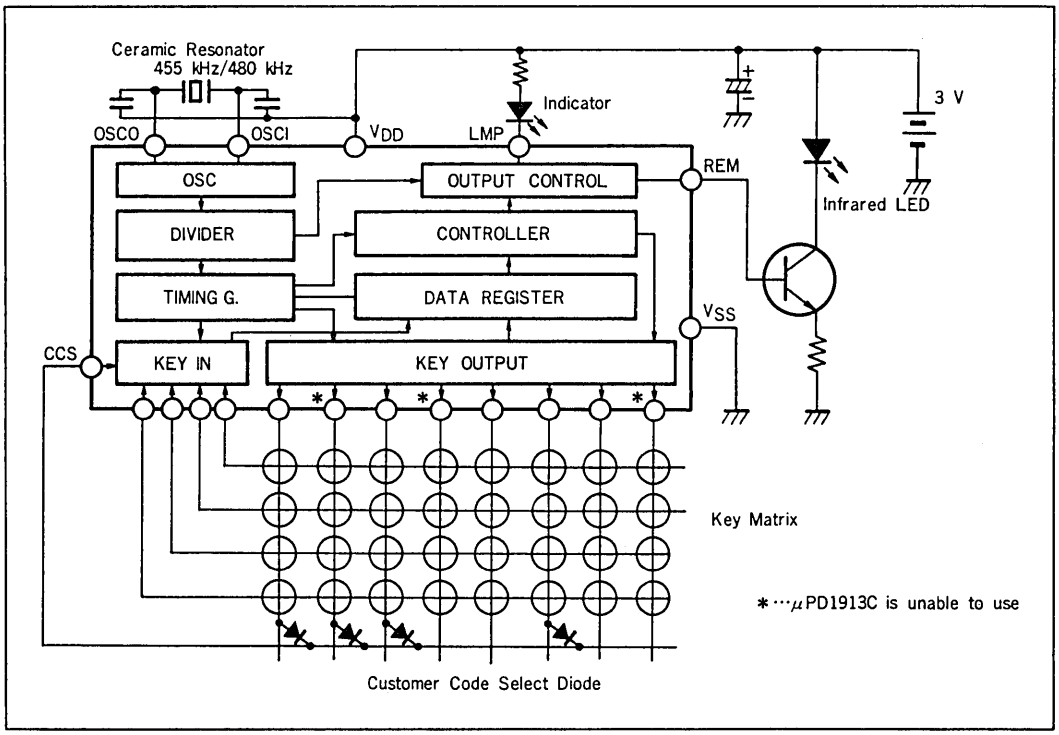
The μPD1913C, μPD1943G are CMOS ICs for control circuits of infrared remote control transmitter which are available for TV, STEREO, VTR and TOY etc.

μPD1943G is designed to transmit 8960 commands [(32 KEY + 3) x 256 custom code] and μPD1913C is able to transmit 736 commands [(20 KEY + 3) x 32 custom code]. For the digital commands, these use a P.P.M system of 16 bit code, which transmit the code twice (invert in the second time) to prevent operation by false codes. These ICs are designed to be received with 4 bit CPU.

FEATURES

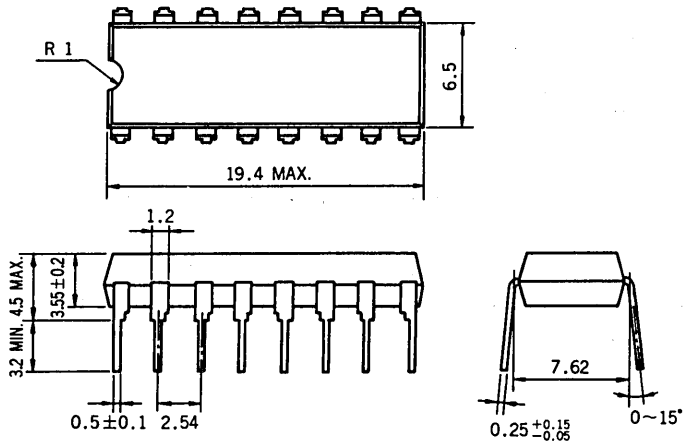
- Low Voltage Operation . . . . . V_{DD} = 2.0 to 3.3 V
- Low Power Consumption (CMOS) . . . I_{DD} < 1 μA at Standby Mode
- 32 Function KEY and 3 dual Action KEY (μPD1913C is 20 Function KEY)
- 256 Custom Codes selected by External Diode (μPD1913C is 32 Custom Codes)
- 16 bit Pulse Position Modulated code
- High Efficiency Transmission . . . . . IR LED ON Duty 3 %
- Indicator Output
- Package
  - μPD1913C . . . 16 PIN DIP
  - μPD1943G . . . 20 PIN MINI FLAT (small size flat package)

BLOCK DIAGRAM

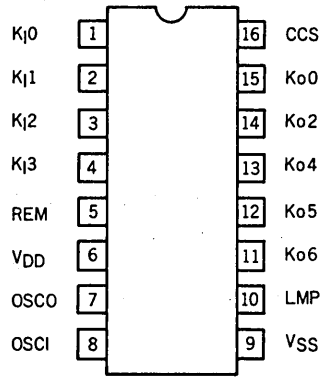


μPD1913C

PACKAGE DIMENSIONS (in millimeters)

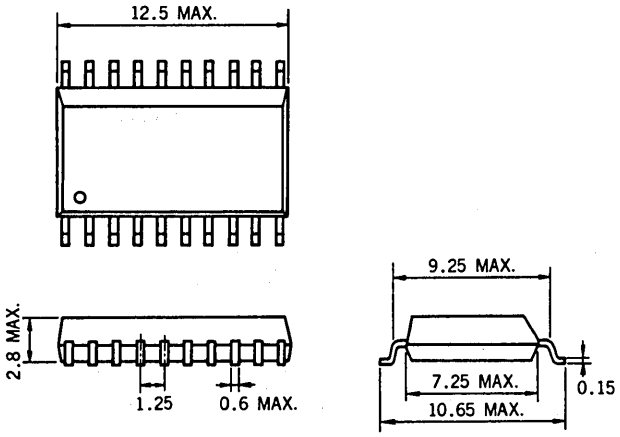


CONNECTION DIAGRAM (Top View)

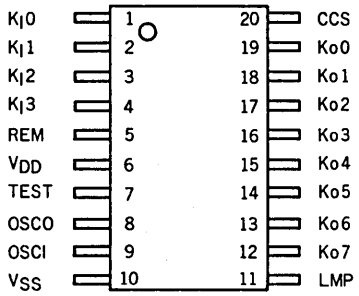


μPD1943G

PACKAGE DIMENSIONS (in millimeters)



CONNECTION DIAGRAM (Top View)



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	$V_{DD} - V_{SS}$	4.0	V
Input Voltage	$V_{IN} - V_{SS}$	−0.3 to V_{DD}	V
Output Current	$I_{OH(REM, LMP)}$	−15.0	mA
Power Dissipation	P_d	250	mW
Operating Temperature Range	T_{opt}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C

RECOMMENDED OPERATING CONDITIONS

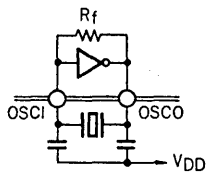
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	2.0	3.0	3.3	V
Oscillation Frequency	f_{OSC}	400	455	500	kHz
Lamp Output Current	$I_{OL(LMP)}$		1		mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V_{DD} = 3.0 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Current	$I_{DD(OP)}$		0.1	1.0	mA	f_{OSC} = 455 kHz
Supply Current	$I_{DD(ST)}$			1	μA	f_{OSC} = STOP
Input High Voltage	$V_{IH(KI)}$	0.7 V_{DD}		V_{DD}	V	
Input Low Voltage	$V_{IL(KI)}$	0		0.3 V_{DD}	V	
Input Pull Down R	R(KI)	150	300	600	kΩ	
Output Current	$I_{OH(REM)}$	−5			mA	$V_{OH(REM)}$ = 1.5 V
Output Low Voltage	$V_{OL(LMP)}$			0.3	V	I_{OL} = 1.0 mA

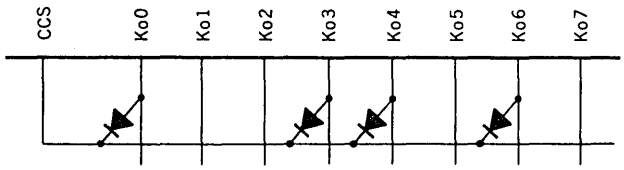
PIN FUNCTION

PIN (μPD1943G)	PIN (μPD1913C)	FUNCTION		
1	1	K_I0	Key Input 0	Internaly Pulldown to V_{SS} by Resistor
2	2	K_I1	Key Input 1	
3	3	K_I2	Key Input 2	
4	4	K_I3	Key Input 3	
5	5	REM	Remote Output	
6	6	V_{DD}	Positive Supply ..... 2.0 to 3.3 V	
7	—	TEST	TEST Terminal ..... normally Open	
8	7	OSCO	Oscillator Output	Ceramic Resonator (400 to 500 kHz)
9	8	OSCI	Oscillator Input	
10	9	LMP	Lamp Output ..... Indicator for Transmission	
11	10	V_{SS}	Ground	
12	—	Ko7	Key Output 7	
13	11	Ko6	Key Output 6	
14	12	Ko5	Key Output 5	
15	13	Ko4	Key Output 4	
16	—	Ko3	Key Output 3	
17	14	Ko2	Key Output 2	
18	—	Ko1	Key Output 1	
19	15	Ko0	Key Output 0	
20	16	CCS	Custom Code Select Input	



Custom Code is selected by diode Connection to Key Output (Ko0 to Ko7)

This terminal is usualy pull up to V_{DD} by internal Resistor.



Custom Code Select

Example . . . C0 to C7 = 1 0 0 1 1 0 1 0

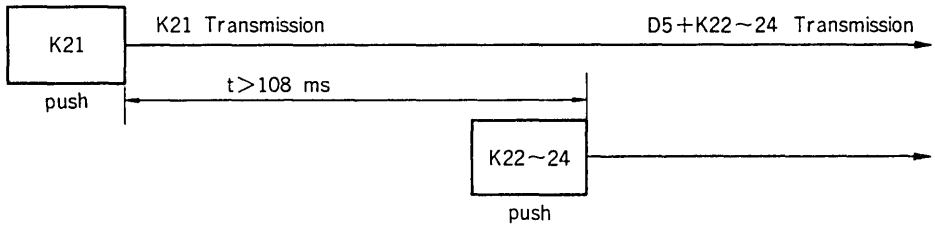
OPERATION OF DUAL ACTION KEY

Keys (K21 to K24) are used for preventing failure caused by mistakes.

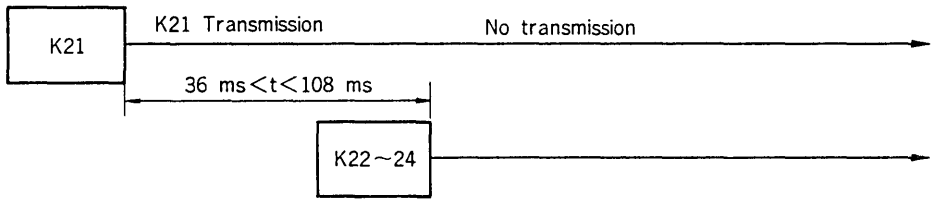
Exsample ; Casset Tape Recorder K21 . . . REC KEY
K22 . . . PLAY KEY

KEY	D0	D1	D2	D3	D4	D5	D6	D7
K21 + K22	1	0	1	0	1	1	0	0
K21 + K23	0	1	1	0	1	1	0	0
K21 + K24	1	1	1	0	1	1	0	0

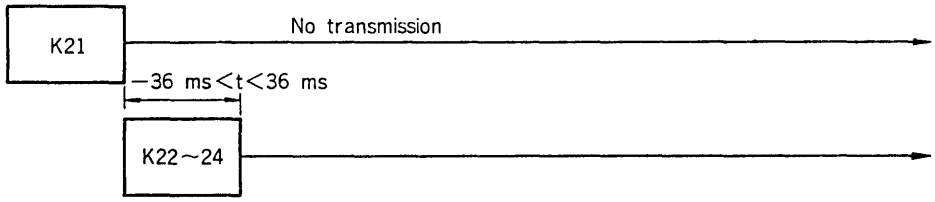
(a) Operation



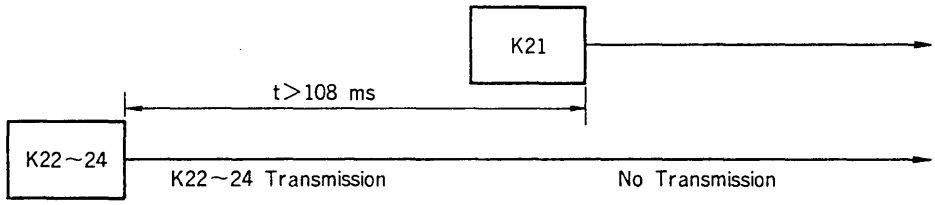
(b) No operation



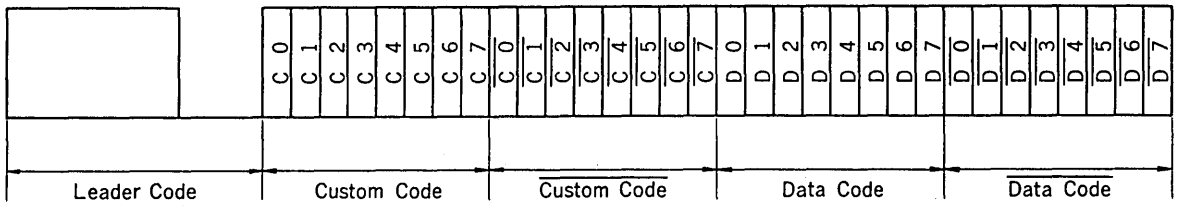
(c) No operation



(d) No operation



Transmission Code



Key Data Code

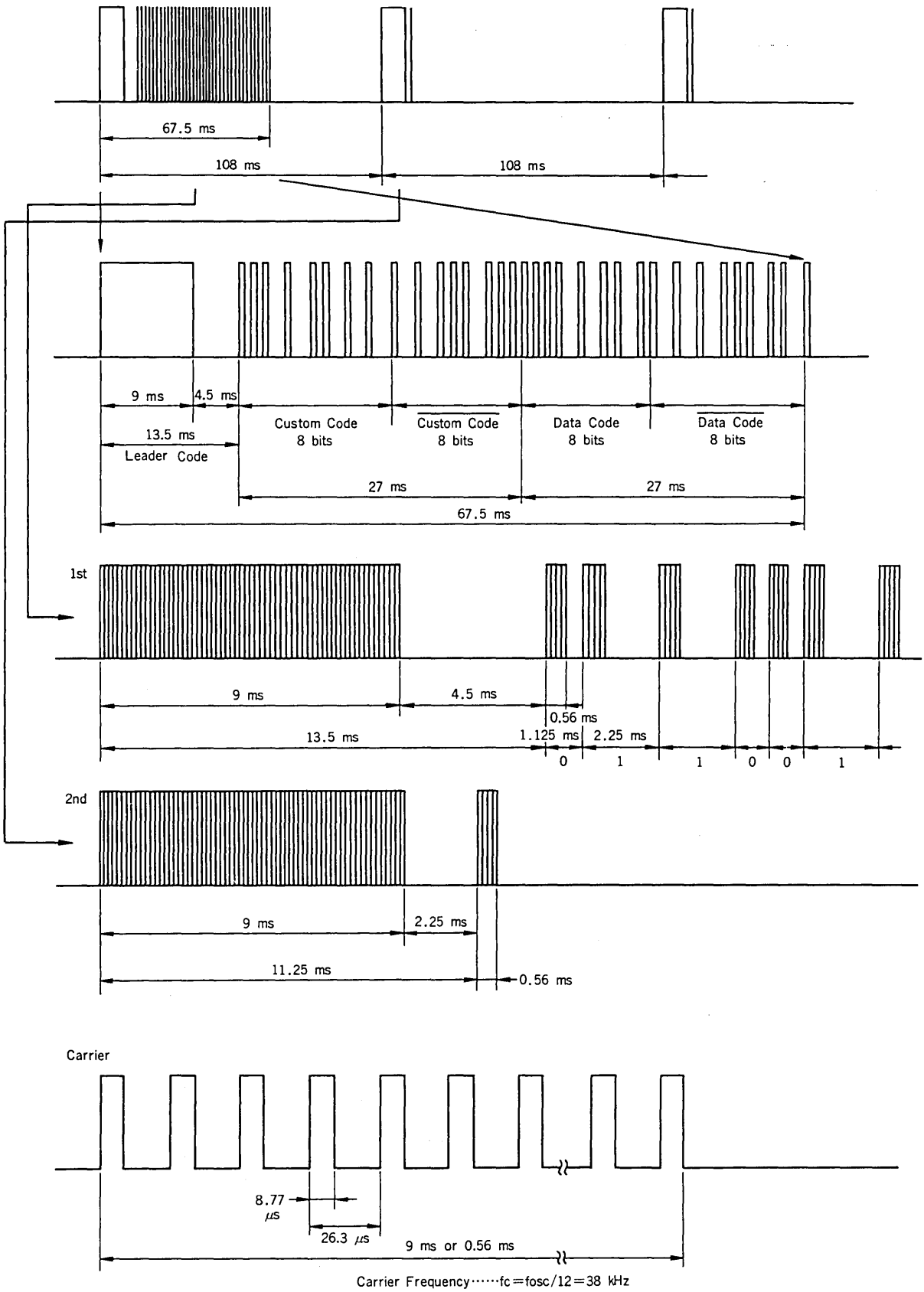
KEY	CONNECTION					DATA CODE								NOTES
	K10	K11	K12	K13	Ko	D0	D1	D2	D3	D4	D5	D6	D7	
K 1	*				Ko0	0	0	0	0	0	0	0	0	
K 2		*				1	0	0	0	0	0	0	0	
K 3			*			0	1	0	0	0	0	0	0	
K 4				*		1	1	0	0	0	0	0	0	
K 5	*				Ko1	0	0	1	0	0	0	0	0	μPD1913C is unable to use
K 6		*				1	0	1	0	0	0	0	0	
K 7			*			0	1	1	0	0	0	0	0	
K 8				*		1	1	1	0	0	0	0	0	
K 9	*				Ko2	0	0	0	1	0	0	0	0	
K10		*				1	0	0	1	0	0	0	0	
K11			*			0	1	0	1	0	0	0	0	
K12				*		1	1	0	1	0	0	0	0	
K13	*				Ko3	0	0	1	1	0	0	0	0	μPD1913C is unable to use
K14		*				1	0	1	1	0	0	0	0	
K15			*			0	1	1	1	0	0	0	0	
K16				*		1	1	1	1	0	0	0	0	
K17	*				Ko4	0	0	0	0	1	0	0	0	
K18		*				1	0	0	0	1	0	0	0	
K19			*			0	1	0	0	1	0	0	0	
K20				*		1	1	0	0	1	0	0	0	
K21	*				Ko5	0	0	1	0	1	0	0	0	
K22		*				1	0	1	0	1	0	0	0	
K23			*			0	1	1	0	1	0	0	0	
K24				*		1	1	1	0	1	0	0	0	
K25	*				Ko6	0	0	0	1	1	0	0	0	
K26		*				1	0	0	1	1	0	0	0	
K27			*			0	1	0	1	1	0	0	0	
K28				*		1	1	0	1	1	0	0	0	
K29	*				Ko7	0	0	1	1	1	0	0	0	μPD1913C is unable to use
K30		*				1	0	1	1	1	0	0	0	
K31			*			0	1	1	1	1	0	0	0	
K32				*		1	1	1	1	1	0	0	0	

Dual Action Key Code

KEY	D0	D1	D2	D3	D4	D5	D6	D7	NOTES
K21 + K22	1	0	1	0	1	1	0	0	
K21 + K23	0	1	1	0	1	1	0	0	
K21 + K24	1	1	1	0	1	1	0	0	

Remote Output Waveforms

Ex. f_{osc} = 455 kHz



MOS DIGITAL INTEGRATED CIRCUIT
μPD1937C

REMOTE CONTROL RECEIVER
P-MOS LSI

DESCRIPTION

The μPD1937C is P-MOS IC for decoding the signal from receiver of remote control system for TV etc.

By using with μPD1986C which is the transmitter control IC, this IC will provide direct channel selection signal. When μPC1363C is used as channel selection IC, complete remote control system can be realized. The package is 16 pins plastic dual in-line.

FEATURES

- Capable to receive 27 commands;

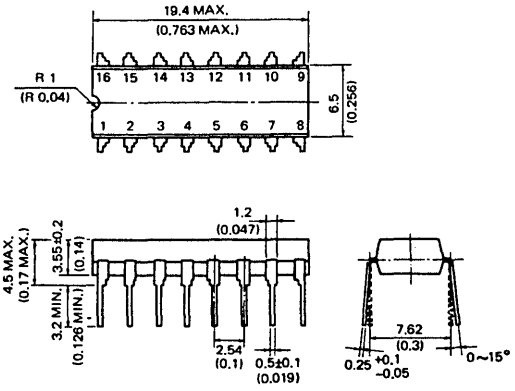
Channel 1 – 20	Channel up, down	Option
Volume up, down	Mute on/off	Power on/off

- Capable to control 5 commands directly;

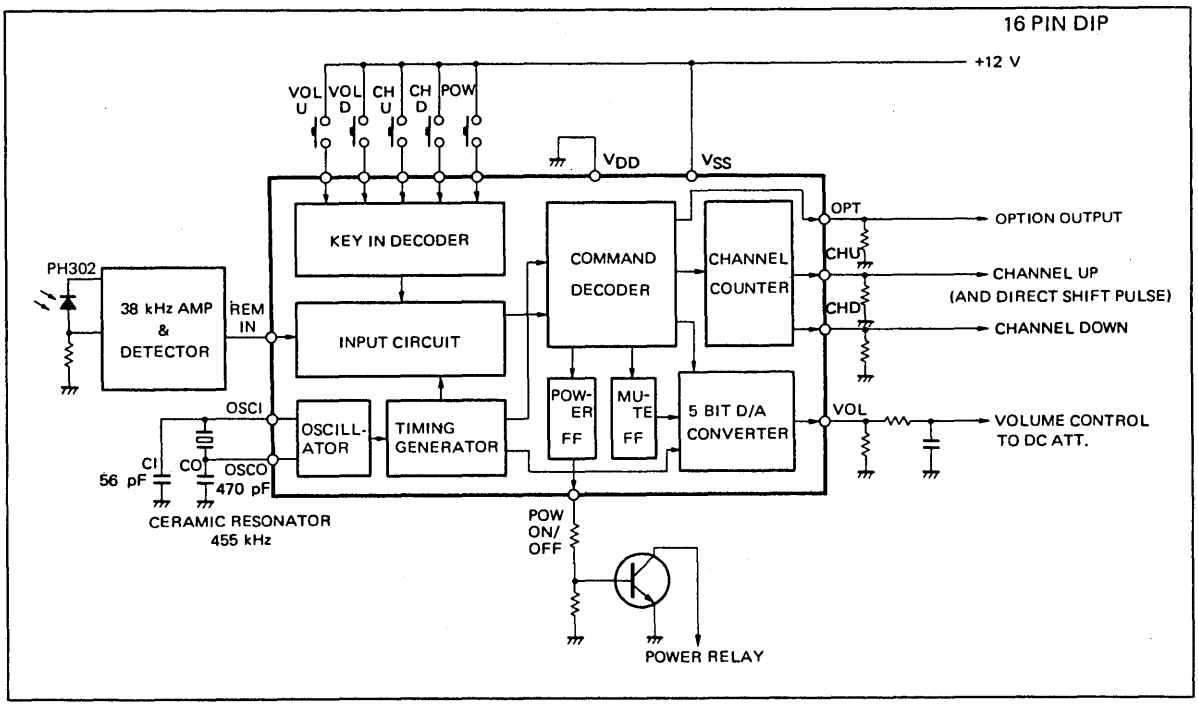
Channel up, down	Volume up, down	Power on/off

- Using with μPC1363C, direct addressing is easily realized.
- Capable to control the volume for 31 steps.

PACKAGE DIMENSIONS
in millimeters (inches)



BLOCK DIAGRAM



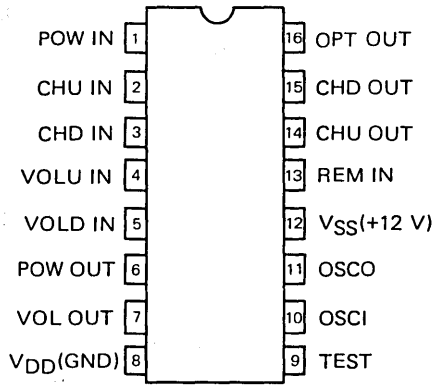
ABSOLUTE MAXIMUM RATINGS (Ta=25 °C)

Supply Voltage	$V_{DD}-V_{SS}$	−15.0 to +0.3	V
Input Voltage	$V_{IN}-V_{SS}$	$-V_{DD}$ to +0.3	V
Output Current	I_{OH} (CHU, CHD, INI)	−5.0	mA
	I_{OH} (VOL, POW)	−10.0	mA
Power Dissipation	P_d	360	mW
Operating Temperature Range	T_{opt}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C

ELECTRICAL CHARACTERISTICS (Ta=−20 to 75 °C, V_{DD}=−9.6 to 14.4 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Voltage	V_{DD}	−9.6	−12.0	−14.4	V	
Supply Current	I_{DD}	−4.0	−10.0	−20.0	mA	Ta=25 °C, OSCI=V_{SS} V_{DD}=−12 V
Input High Voltage	V_{IH} (1~5,13)	0		−1.5	V	
Input Low Voltage	V_{IL} (1~5,13)	−5.0		V_{DD}	V	
Input Pull Down Current	I_{IL} (1~5,13)	5.0		50	μA	Ta=25 °C, V_{IN}=V_{SS} V_{DD}=−12 V
Output High Voltage	V_{OH} (CHU)			−2.5	V	I_{OH}=−1.0 mA
Output High Voltage	V_{OH} (CHD)			−2.5	V	I_{OH}=−1.0 mA
Output High Voltage	V_{OH} (OPT)			−2.5	V	I_{OH}=−1.0 mA
Output High Voltage	V_{OH} (VOL)			−2.5	V	I_{OH}=−5.0 mA
Output High Voltage	V_{OH} (POW)			−2.5	V	I_{OH}=−5.0 mA
Output Low Current	I_{OL} (1~5,13)	0		100	μA	Ta=25 °C, V_{OL}=−11.5 V V_{DD}=−12 V

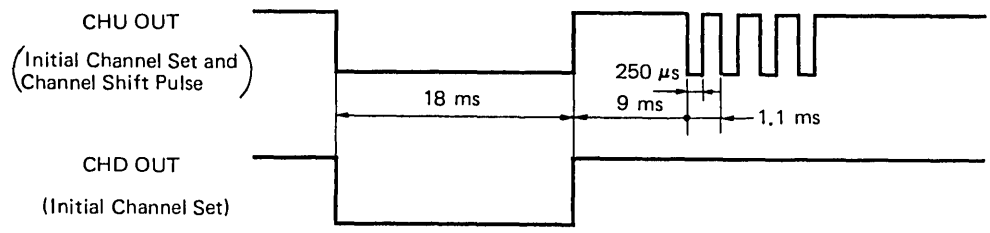
CONNECTION DIAGRAM
(Top View)



PIN	FUNCTION		
8	V_{DD}	Negative supply GND norminal	
12	V_{SS}	Positive supply +12 V norminal (9.6~14.4 V)	
10	OSCI	Oscillator Input	455 kHz Ceramic Resonator CSB455A (MURATA MFG. Co.) is connected to these pins.
11	OSCO	Oscillator Output	
13	REM IN	Remote Signal Input	
1	POW IN	Power ON/OFF Key Input	
2	CHU IN	Channel Up Key Input	
3	CHD IN	Channel Down Key Input	
4	VOLU IN	Volume Up Key Input	
5	VOLD IN	Volume Down Key Input	
6	VOL OUT	Volume Output	This output is in the form of a pulse. Connect to CR filter.
7	POW OUT	Power ON/OFF Output	
14	CHU OUT	Channel Up Pulse Output and Direct Channel Shift Pulse	
15	CHD OUT	Channel Down Pulse Output	
16	OPT OUT	Option Output for free use.	

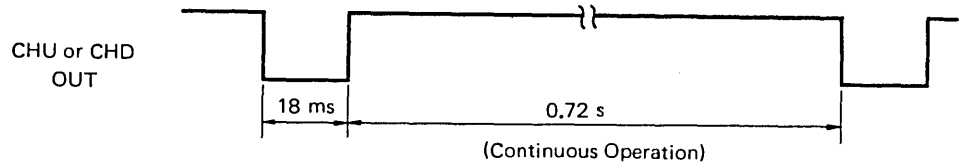
1) CHANNEL SELECTION OUTPUT

- Direct Channel Operation

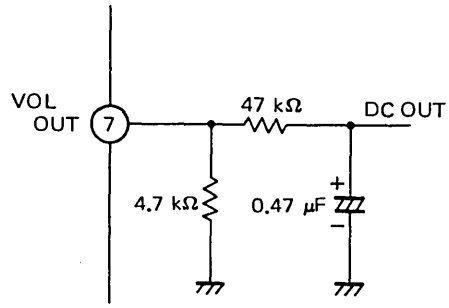


shift pulse = CH number − 1 MAX. 19

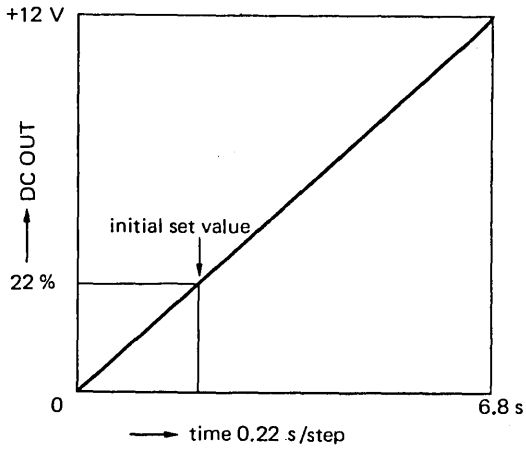
- UP, DOWN Channel Operation



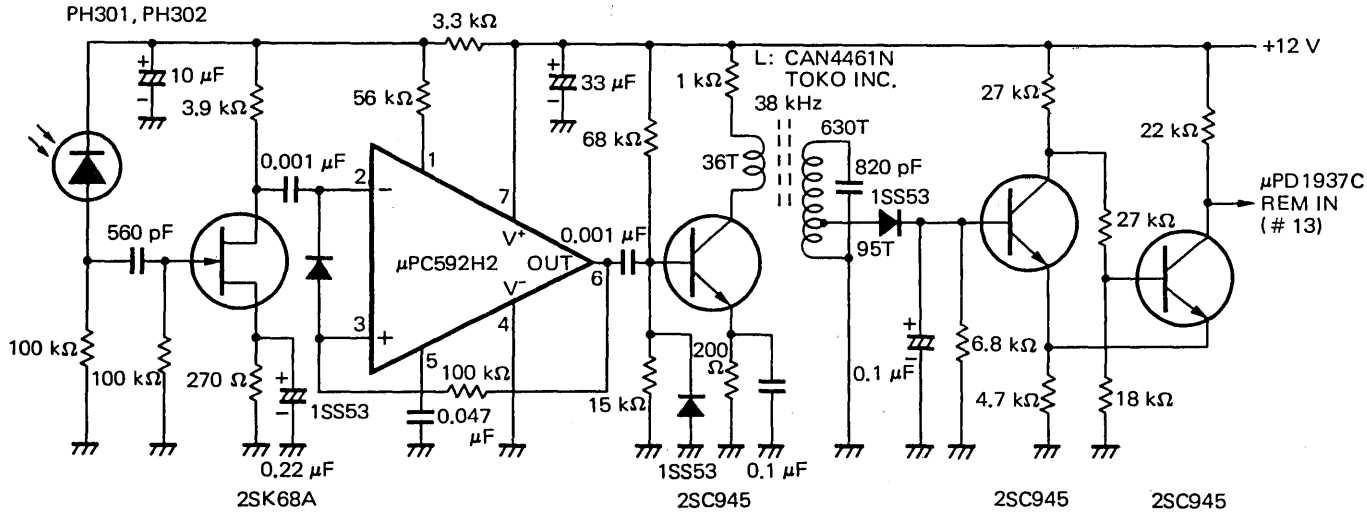
2) VOLUME OUTPUT



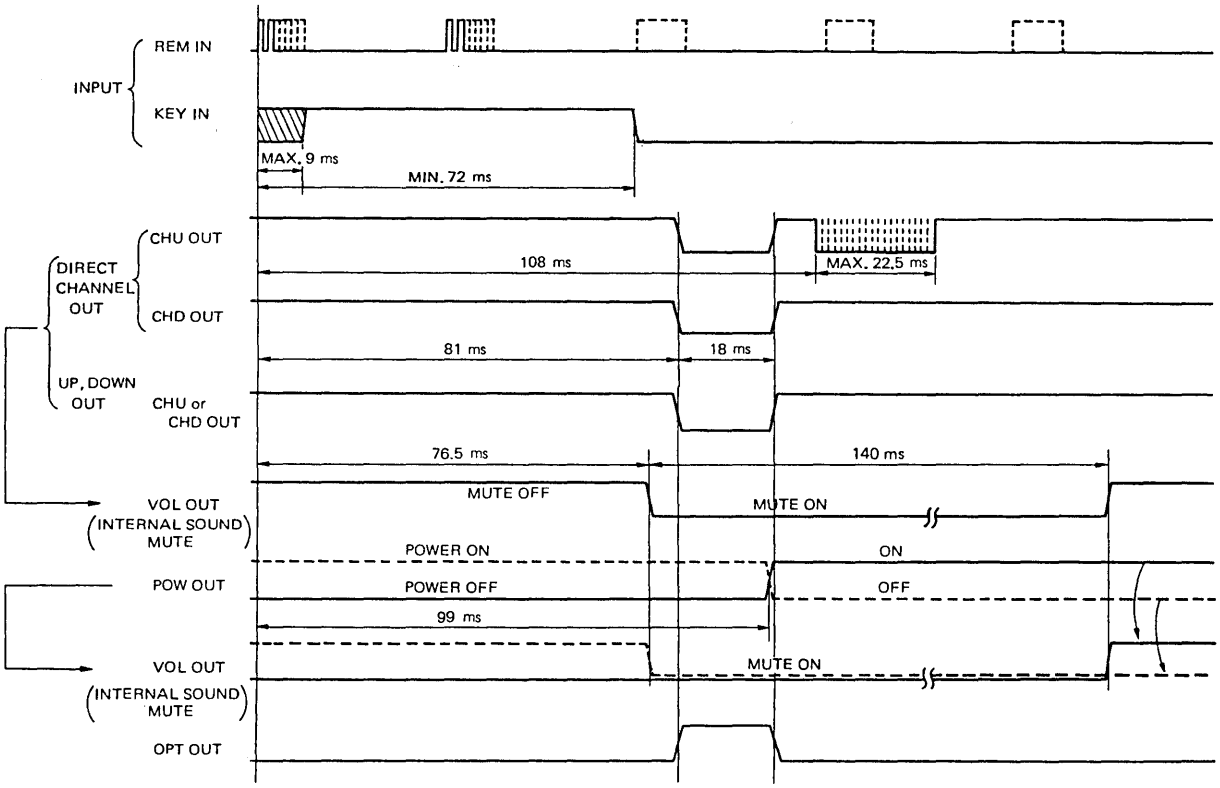
Repetition frequency ..... 3.6 kHz
VOL Steps 31
MIN. to MAX. time ..... 6.8 s



EXAMPLE OF INPUT AMP CIRCUIT

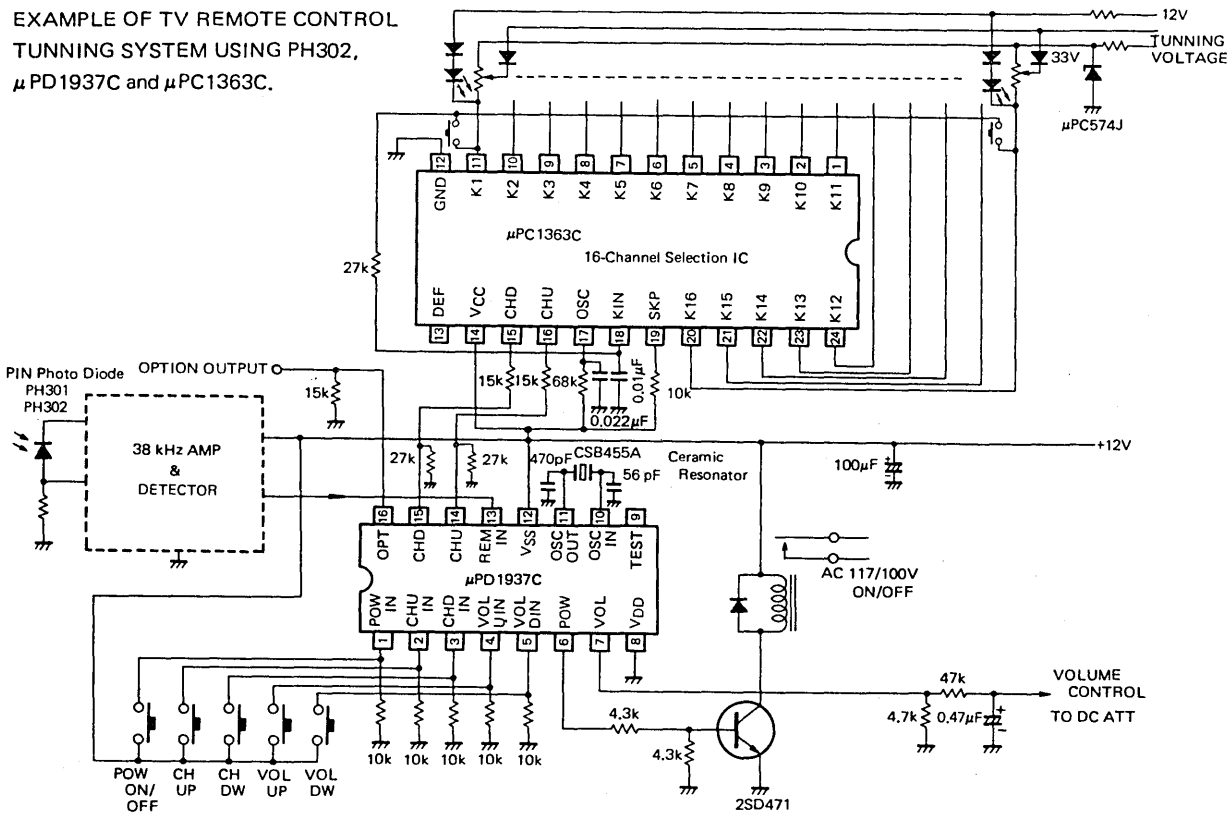


OUTPUT WAVE FORM



APPLICATION CIRCUIT

EXAMPLE OF TV REMOTE CONTROL TUNNING SYSTEM USING PH302, μPD1937C and μPC1363C.



MOS DIGITAL INTEGRATED CIRCUIT
μPD1986C

REMOTE CONTROL TRANSMITTER
CMOS LSI

DESCRIPTION

μPD1986C is CMOS IC for controlling the transmitter of remote control system for TV set etc. By using with μPD1987C which is the receiver control IC, the direct channel control system can be obtained. When infrared emitting diode is used as transmitter element, this system will be very stable against any interference. The package is 16 pins plastic dual in-line package type.

FEATURES

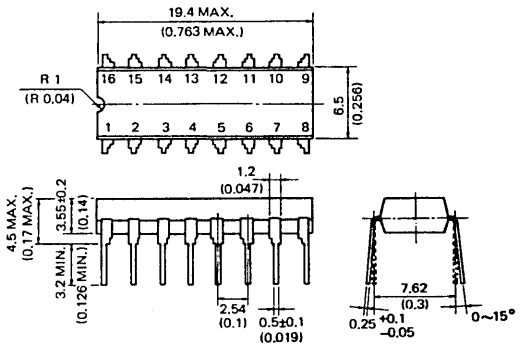
- Capable to transmit 27 commands;

  Channel 1 – 20 Channel up, down Volume up, down

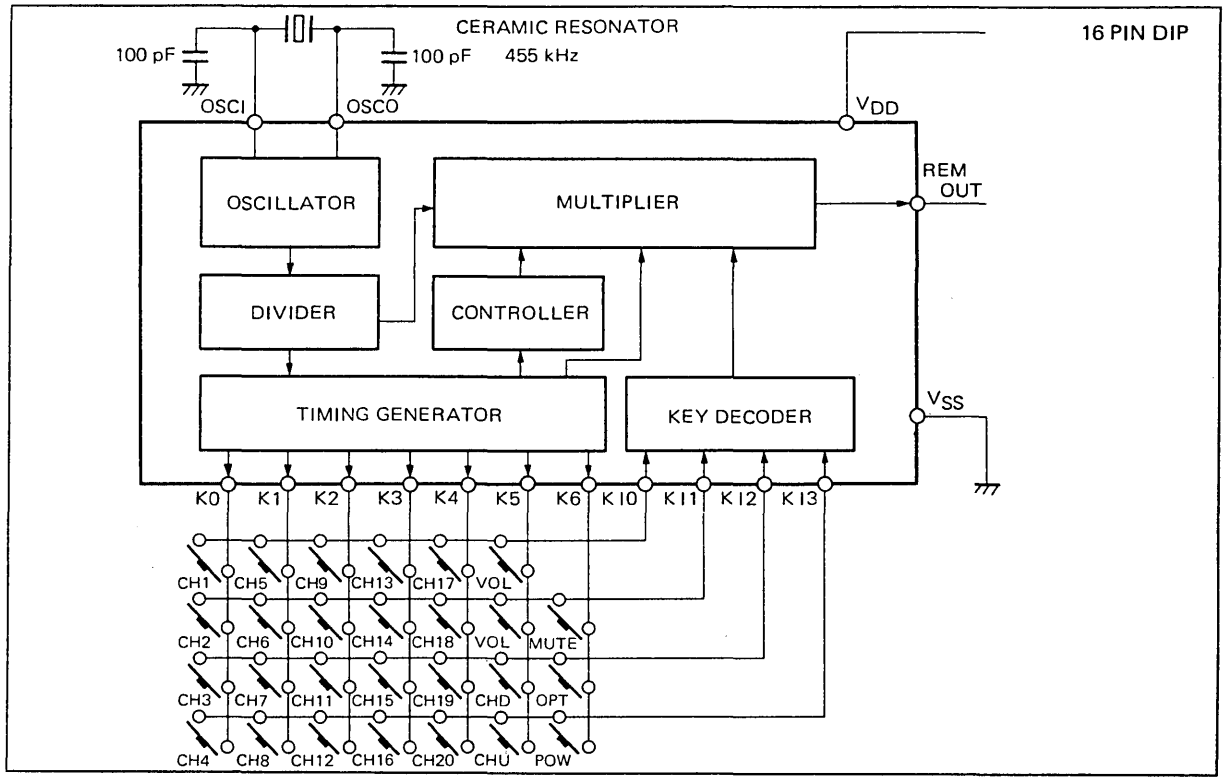
  Mute on/off Power on/off Option*

  * μPD1987C is not able to decode this option code.
- Minimum misoperation by infrared transmission
- Wide operation voltage range (2.2 – 7.2 V)
- Low power consumption (I_{DD} = 1 μA at KEY OFF condition)

PACKAGE DIMENSIONS
in millimeters (inches)



BLOCK DIAGRAM



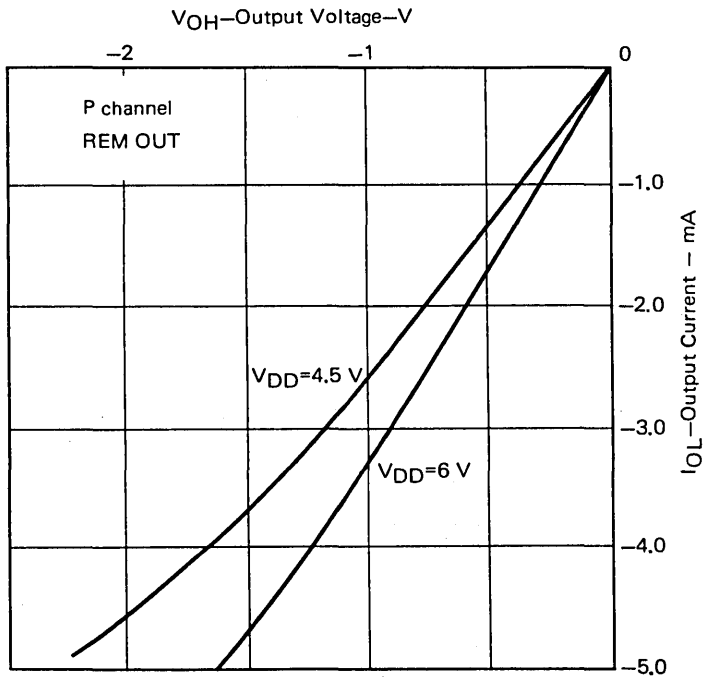
ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Supply Voltage	$V_{DD}-V_{SS}$	−0.3 to +8.0	V
Input Voltage	$V_{IN}-V_{SS}$	−0.3 to V_{DD}	V
Output Current	I_{OH}(REM)	−10.0	mA
Power Dissipation	Pd	360	mW
Operating Temperature Range	Topt	−20 to +75	°C
Storage Temperature Range	Tstg	−40 to +125	°C

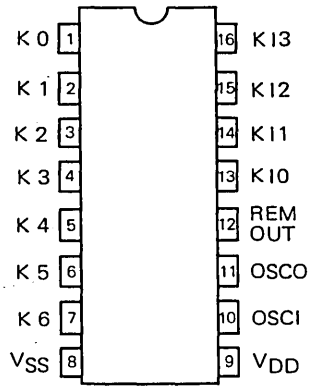
ELECTRICAL CHARACTERISTICS (Ta = −20 to +75 °C, V_{DD} = 6.0 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Voltage	V_{DD}	2.2	6.0	7.2	V	
Supply Current	I_{DD}(OP)		0.3	1.0	mA	OSC=455 kHz
Supply Current	I_{DD}(ST)			1.0	μA	OSC STOP, Ta=25 °C
Input High Voltage	V_{IH}(KI)	0.7V_{DD}		V_{DD}	V	
Input Low Voltage	V_{IL}(KI)	0		0.3V_{DD}	V	
Output High Voltage	V_{OH} (REM)	V_{DD}−1		V_{DD}	V	I_{OL}=−1.0 mA
Input Pulldown Current	I_{IL} (KI)	−10		−100	μA	$V_{IN}=V_{DD}$, Ta=25 °C

REMOUT CHARACTERISTIC ($I_{OL}-V_{OH}$)



CONNECTION DIAGRAM
(Top View)



PIN	FUNCTION		
8	V_{SS}	Ground	
9	V_{DD}	Positive supply 2.2 to 7.2 Volt.	Operating voltage is wideband
10	OSCI	Oscillator Input	455 kHz Ceramic Resonator CSB455A (MURATA MFG. Co.)
11	OSCO	Oscillator Output	
12	REM OUT	Remote Signal Output	See Fig 1 and Table 1
13~16	KI0~KI3	Key Input 0~3	
1~7	K0~K7	Key Output 0~7	

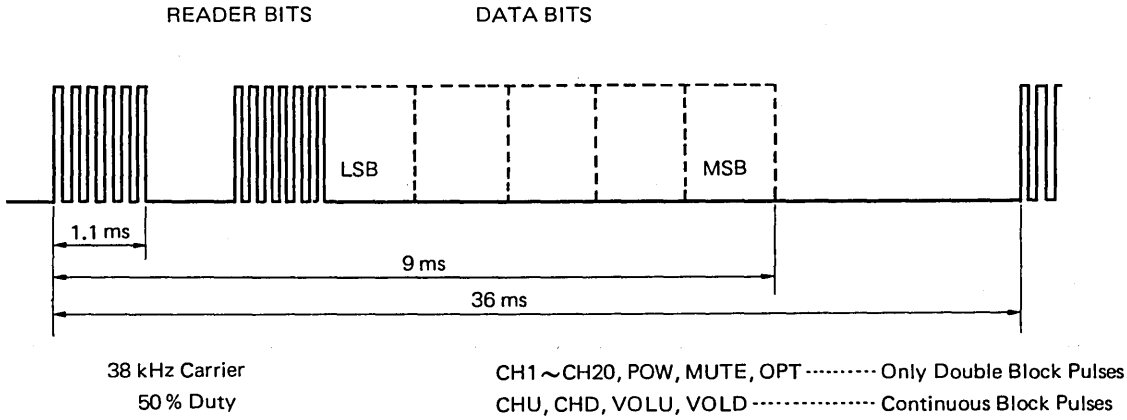


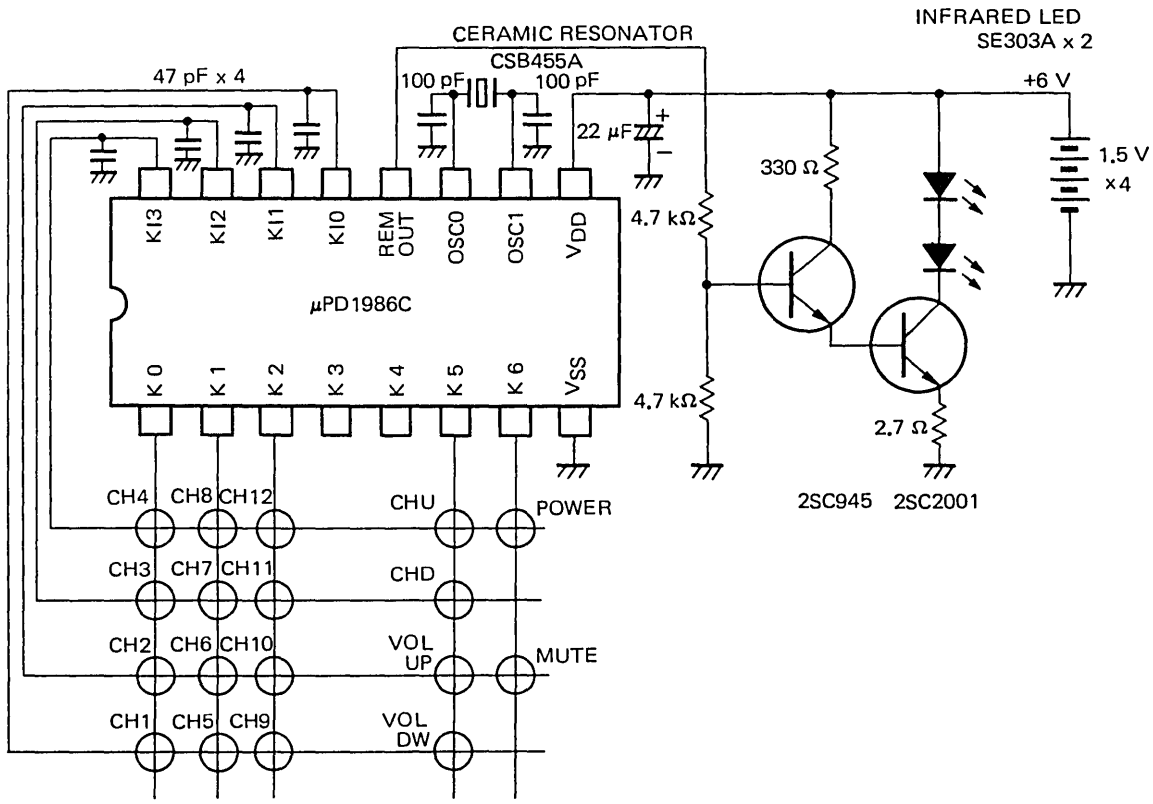
Fig. 1 Remote Signal Output (1 Block)

Table 1 Data bit code

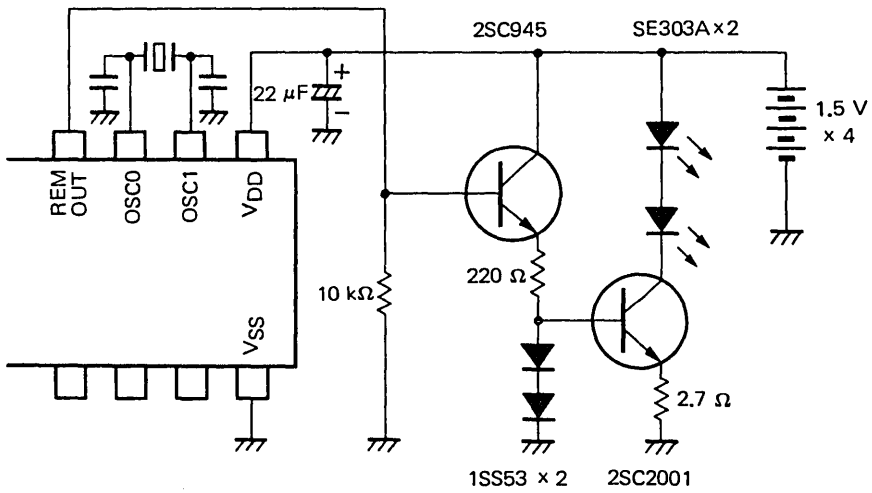
CONNECTION		FUNCTION		DATA BIT CODE				
K IN	K OUT			MSB				LSB
KI0	K 0	CH 1	DIRECT ADDRESS CHANNEL 1	0	0	0	0	0
KI1	K 0	CH 2	DIRECT ADDRESS CHANNEL 2	0	0	0	0	1
KI2	K 0	CH 3	DIRECT ADDRESS CHANNEL 3	0	0	0	1	0
KI3	K 0	CH 4	DIRECT ADDRESS CHANNEL 4	0	0	0	1	1
KI0	K 1	CH 5	DIRECT ADDRESS CHANNEL 5	0	0	1	0	0
KI1	K 1	CH 6	DIRECT ADDRESS CHANNEL 6	0	0	1	0	1
KI2	K 1	CH 7	DIRECT ADDRESS CHANNEL 7	0	0	1	1	0
KI3	K 1	CH 8	DIRECT ADDRESS CHANNEL 8	0	0	1	1	1
KI0	K 2	CH 9	DIRECT ADDRESS CHANNEL 9	0	1	0	0	0
KI1	K 2	CH 10	DIRECT ADDRESS CHANNEL 10	0	1	0	0	1
KI2	K 2	CH 11	DIRECT ADDRESS CHANNEL 11	0	1	0	1	0
KI3	K 2	CH 12	DIRECT ADDRESS CHANNEL 12	0	1	0	1	1
KI0	K 3	CH 13	DIRECT ADDRESS CHANNEL 13	0	1	1	0	0
KI1	K 3	CH 14	DIRECT ADDRESS CHANNEL 14	0	1	1	0	1
KI2	K 3	CH 15	DIRECT ADDRESS CHANNEL 15	0	1	1	1	0
KI3	K 3	CH 16	DIRECT ADDRESS CHANNEL 16	0	1	1	1	1
KI0	K 4	CH 17	DIRECT ADDRESS CHANNEL 17	1	0	0	0	0
KI1	K 4	CH 18	DIRECT ADDRESS CHANNEL 18	1	0	0	0	1
KI2	K 4	CH 19	DIRECT ADDRESS CHANNEL 19	1	0	0	1	0
KI3	K 4	CH 20	DIRECT ADDRESS CHANNEL 20	1	0	0	1	1
KI0	K 5	VOLD	VOLUME DOWN	1	1	0	0	0
KI1	K 5	VOLU	VOLUME UP	1	1	0	0	1
KI2	K 5	CHD	CHANNEL DOWN	1	1	0	1	0
KI3	K 5	CHU	CHANNEL DOWN	1	1	0	1	1
KI1	K 6	MUTE	MUTE ON/OFF	1	1	1	0	1
KI2	K 6	OPT	OPTION	1	1	1	0	0
KI3	K 6	POW	POWER ON/OFF	1	1	1	1	1

APPLICATION CIRCUIT

○ EXAMPLE OF 18 FUNCTION TRANSMITTER CIRCUIT



○ EXAMPLE OF CONSTANT CURRENT LED DRIVE CIRCUIT



MOS DIGITAL INTEGRATED CIRCUIT

μPD1987C

REMOTE CONTROL RECEIVER
P-MOS LSI

DESCRIPTION

The μPD1987C is P-MOS IC for decoding the signal from receiver of remote control system for TV etc.

By using with μPD1986C which is the transmitter control IC, this IC will provide direct channel selection signal. When μPC1360C is used as channel selection IC, complete remote control system can be realized. The package is 16 pins plastic dual in-line.

FEATURES

- Capable to receive 26 commands;

  Channel 1 – 20 Channel up, down

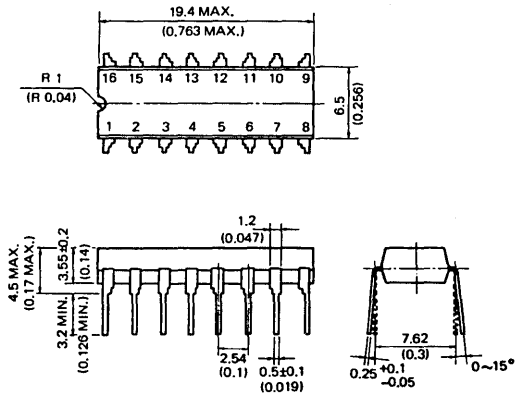
  Volume up, down Mute on/off Power on/off

- Capable to control 5 commands directly;

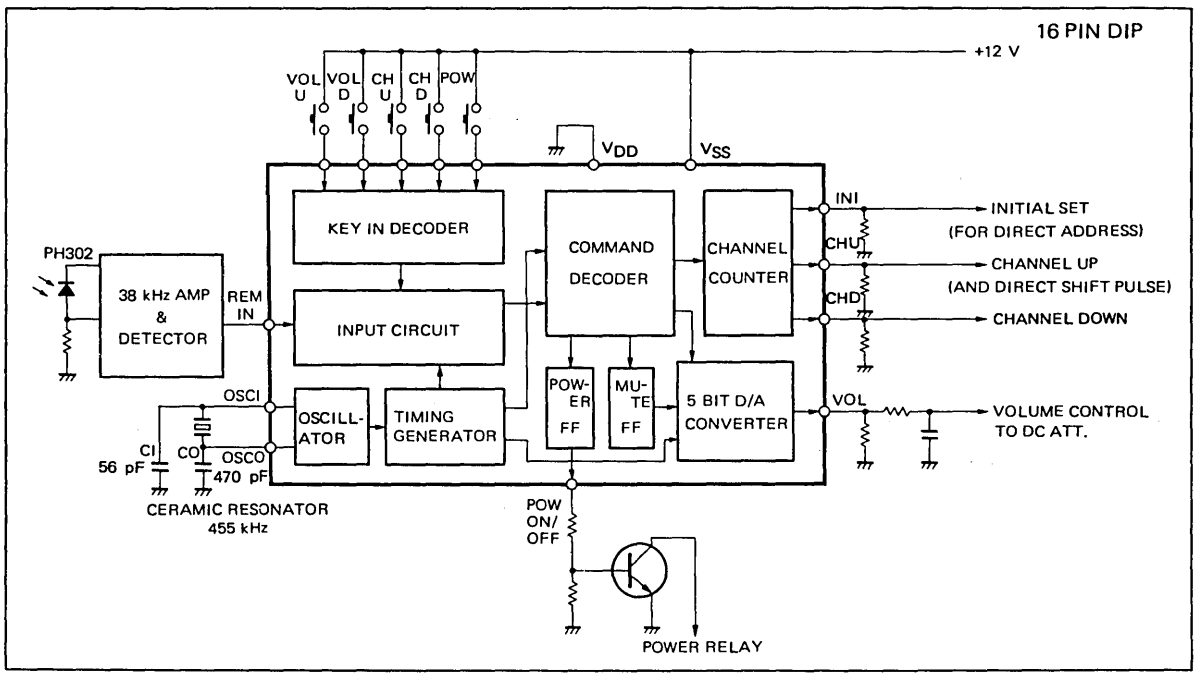
  Channel up, down Volume up, down Power on/off

- Using with μPC1360C, direct addressing is easily realized.
- Capable to control the volume for 31 steps.

PACKAGE DIMENSIONS
in millimeters (inches)



BLOCK DIAGRAM



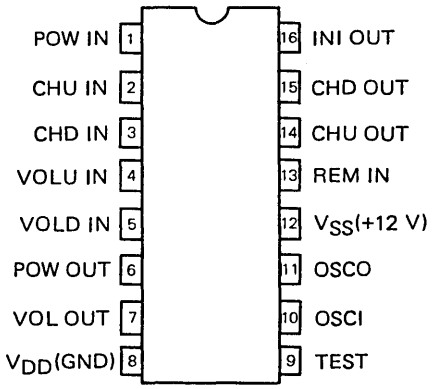
ABSOLUTE MAXIMUM RATINGS (Ta=25 °C)

Supply Voltage	$V_{DD}-V_{SS}$	−15.0 to +0.3	V
Input Voltage	$V_{IN}-V_{SS}$	$-V_{DD}$ to +0.3	V
Output Current	I_{OH} (CHU, CHD, INI)	−5.0	mA
	I_{OH} (VOL, POW)	−10.0	mA
Power Dissipation	P_d	360	mW
Operating Temperature Range	T_{opt}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C

ELECTRICAL CHARACTERISTICS (Ta=−20 to 75 °C, V_{DD}=−9.6 to 14.4 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Voltage	V_{DD}	−9.6	−12.0	−14.4	V	
Supply Current	I_{DD}	−4.0	−10.0	−20.0	mA	Ta=25 °C, OSCI=V_{SS} V_{DD}=−12 V
Input High Voltage	V_{IH} (1~5,13)	0		−1.5	V	
Input Low Voltage	V_{IL} (1~5,13)	−5.0		V_{DD}	V	
Input Pull Down Current	I_{IL} (1~5,13)	5.0		50	μA	Ta=25 °C, V_{IN}=V_{SS} V_{DD}=−12 V
Output High Voltage	V_{OH} (CHU)			−2.5	V	I_{OH}=−1.0 mA
Output High Voltage	V_{OH} (CHD)			−2.5	V	I_{OH}=−1.0 mA
Output High Voltage	V_{OH} (INI)			−2.5	V	I_{OH}=−1.0 mA
Output High Voltage	V_{OH} (VOL)			−2.5	V	I_{OH}=−5.0 mA
Output High Voltage	V_{OH} (POW)			−2.5	V	I_{OH}=−5.0 mA
Output Low Current	I_{OL} (1~5,13)	0		100	μA	Ta=25 °C, V_{OL}=−11.5 V V_{DD}=−12 V

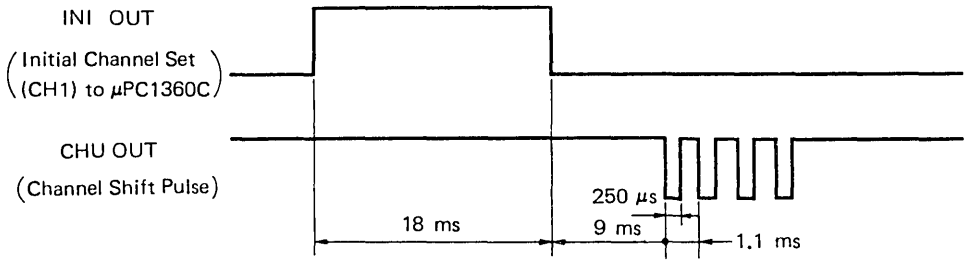
CONNECTION DIAGRAM
(Top View)



PIN	FUNCTION		
8	V_{DD}	Negative supply GND norminal	
12	V_{SS}	Positive supply +12 V norminal (9.6~14.4 V)	
10	OSCI	Oscillator Input	455 kHz Ceramic Resonator CSB455A (MURATA MFG. Co.) is connected to these pins.
11	OSCO	Oscillator Output	
13	REM IN	Remote Signal Input	
1	POW IN	Power ON/OFF Key Input	
2	CHU IN	Channel Up Key Input	
3	CHD IN	Channel Down Key Input	
4	VOLU IN	Volume Up Key Input	
5	VOLD IN	Volume Down Key Input	
6	VOL OUT	Volume Output	This output is in the form of a pulse. Connect to CR filter.
7	POW OUT	Power ON/OFF Output	
14	CHU OUT	Channel Up Pulse Output and Direct Channel Shift Pulse	
15	CHD OUT	Channel Down Pulse Output	
16	INI OUT	Option Output for free use.	

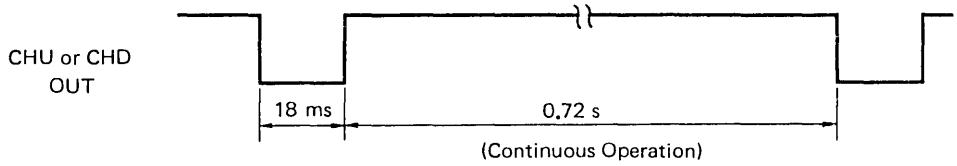
1) CHANNEL SELECTION OUTPUT

- Direct Channel Operation

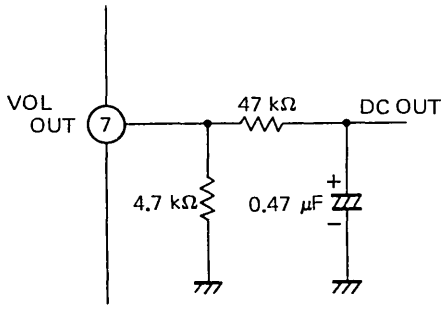


shift pulse = CH number − 1 MAX. 19

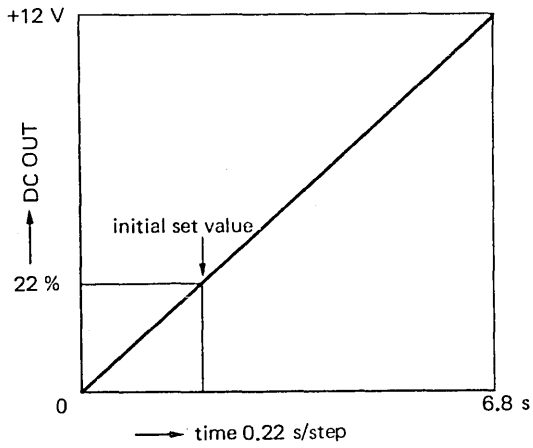
- UP, DOWN Channel Operation



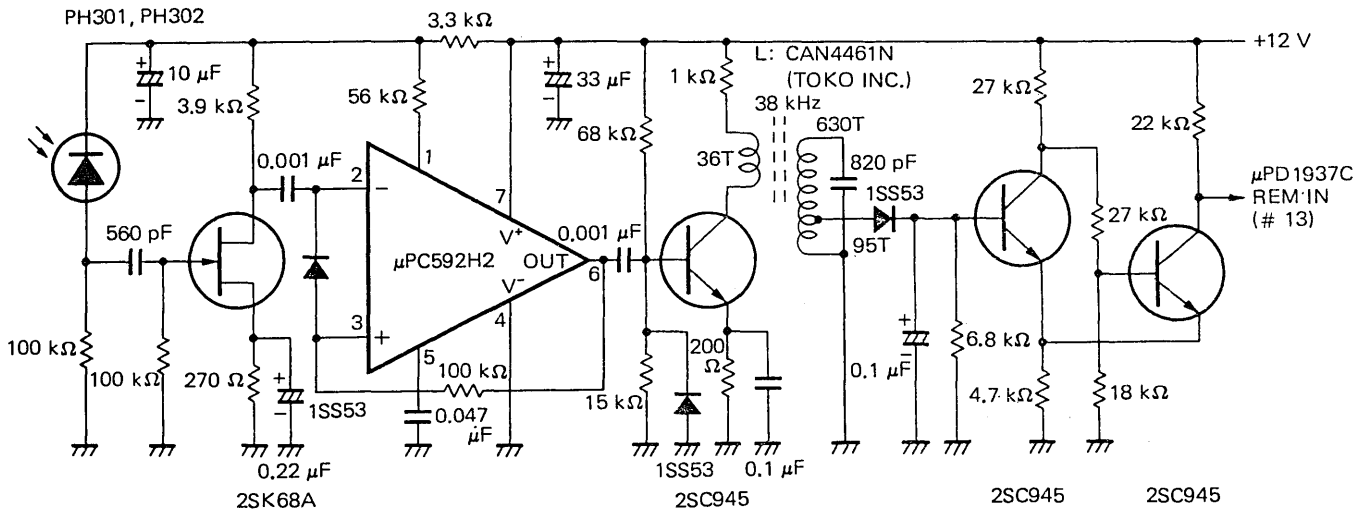
2) VOLUME OUTPUT



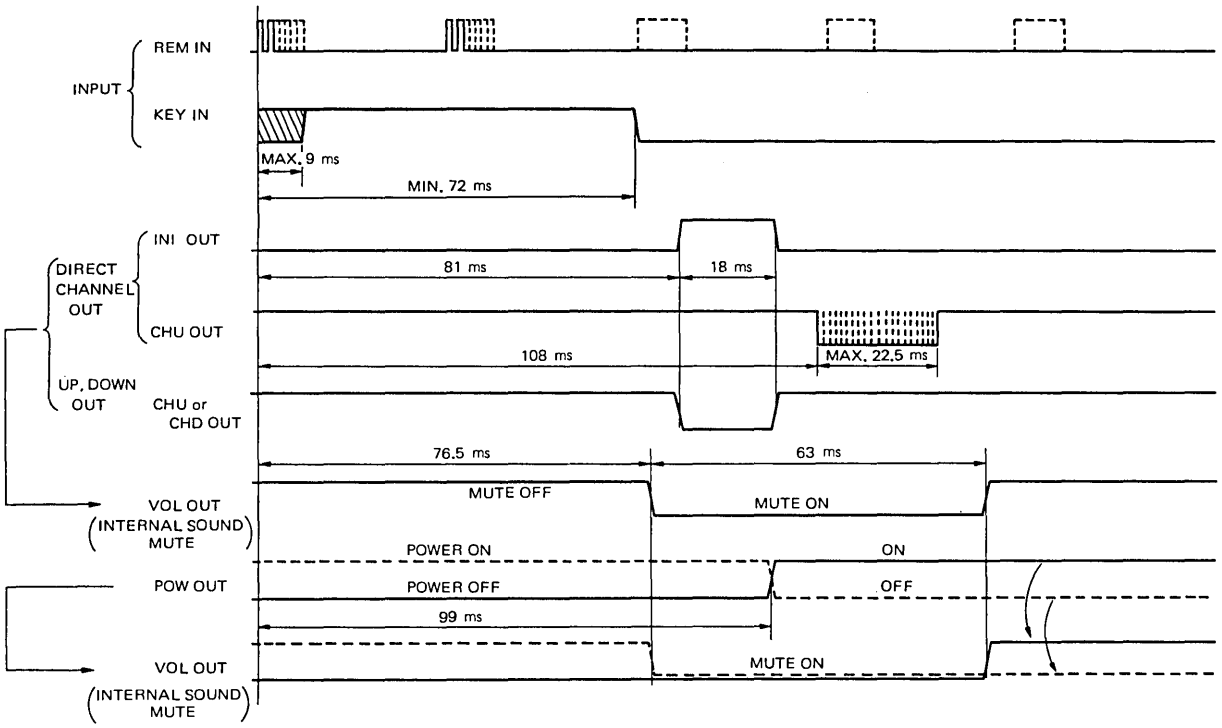
Repetition frequency ..... 3.6 kHz
VOL Steps 31
MIN. to MAX. time ..... 6.8 s



EXAMPLE OF INPUT AMP CIRCUIT

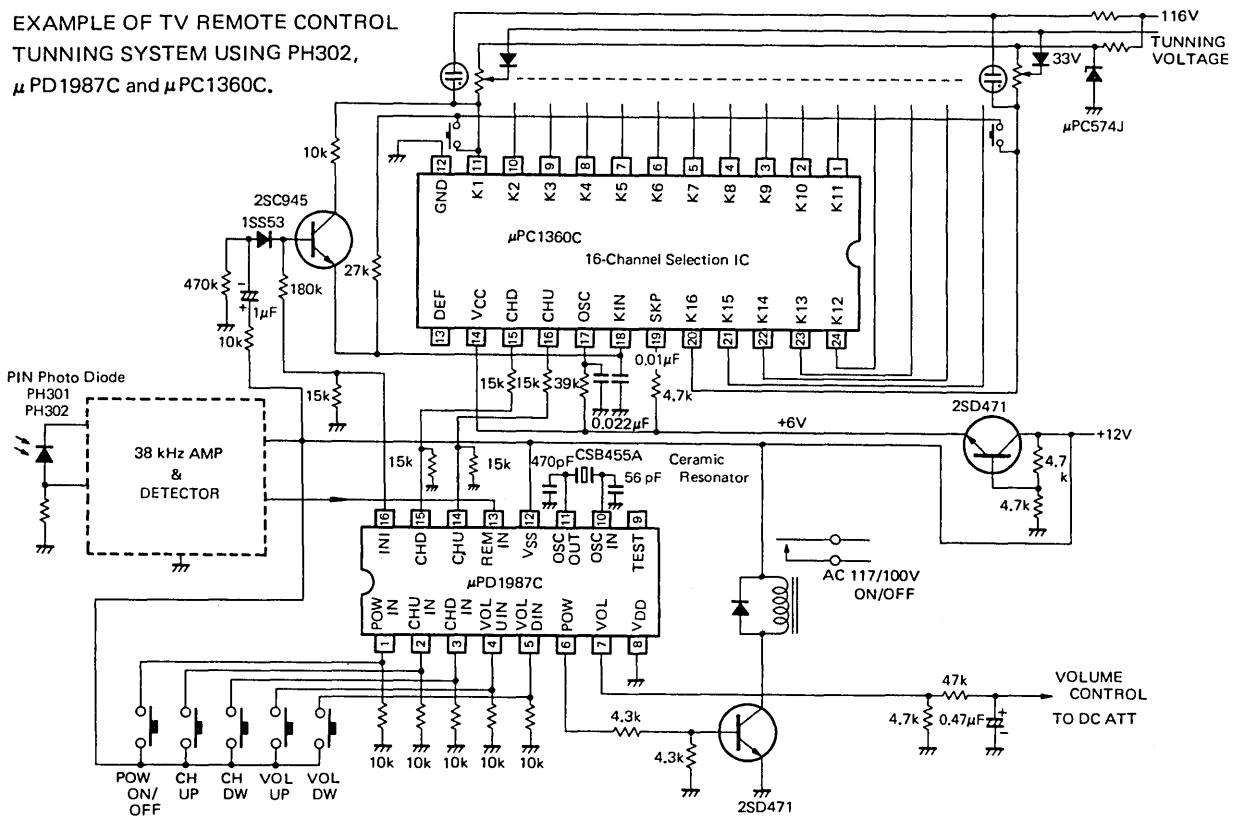


OUTPUT WAVE FORM



APPLICATION CIRCUIT

EXAMPLE OF TV REMOTE CONTROL TUNNING SYSTEM USING PH302, μPD1987C and μPC1360C.



MOS DIGITAL INTEGRATED CIRCUIT
μPD6102G

MULTI-PURPOSE REMOTE CONTROL TRANSMITTER IC
CMOS LSI

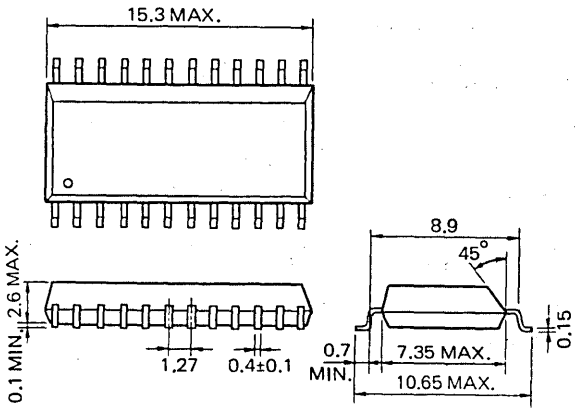
DESCRIPTION

The μPD6102G is a versatile remote control infrared transmitter (TX) integrated circuit for TV, VCR, stereo, air conditioner and many other applications. The maximum of 34304 commands are available with the custom code selection by external diodes. This enables effective control of various apparatus without interference. The transmitting code consisting of 16 bits can be directly decoded by a 4-bit MPU, thus giving a wide application. The package is a 24-Pin MINI FLAT that is the best suited for miniaturization of apparatus.

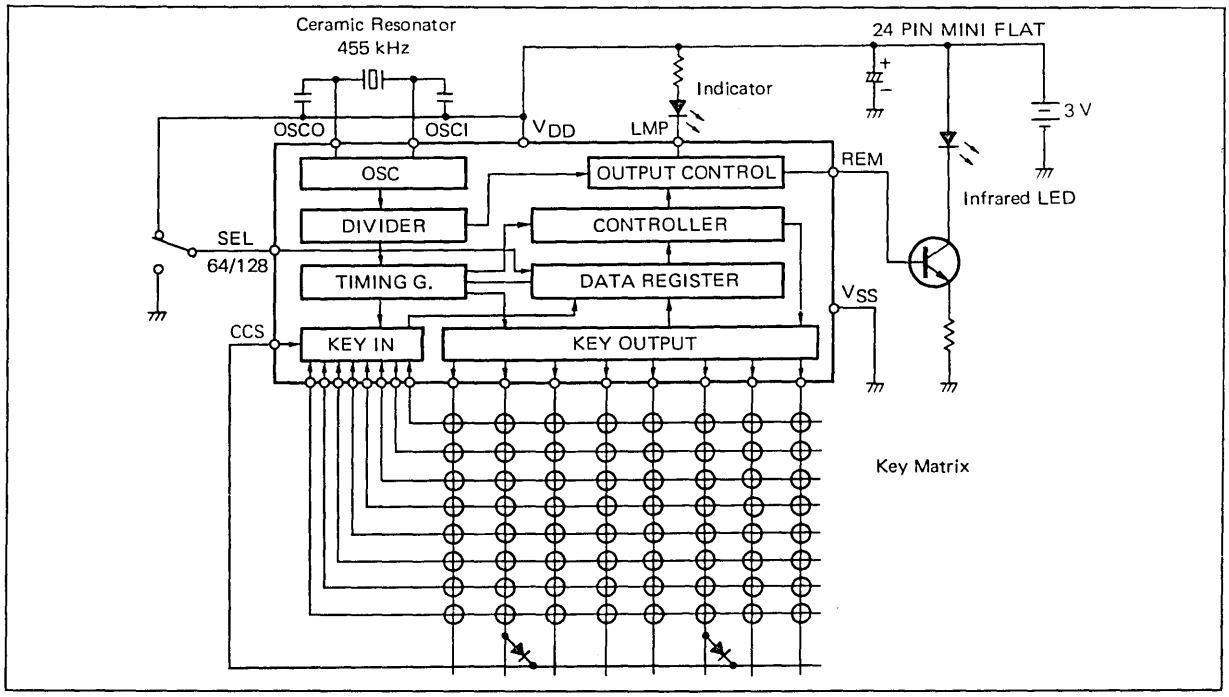
FEATURES

- Low Voltage Operation . . . . . V_{DD} = 2.0 to 3.3 V
- Low Power Consumption . . . I_{DD} < 1 μA at Standby Mode
- 64 Function KEYs and 3 dual Action KEY
- 256 Custom Codes selected by External Diode
- 16 bit Pulse Position Modulated code
- High Transmission Efficiency . . IR LED ON Duty 3 %
- Indicator Output
- Package . . . 24 Pin MINI FLAT
- Transmit 128 Data Code
- μPD1913C (20 key) } Code Compatible
  μPD1943G (32 key) }

PACKAGE DIMENSIONS (in millimeters)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	$V_{DD} - V_{SS}$	4.0	V
Input Voltage	$V_{IN} - V_{SS}$	−0.3 to V_{DD}	V
Output Current	$I_{OH(REM, LMP)}$	−15.0	mA
Power Dissipation	Pd	250	mW
Operating Temperature Range	T_{opt}	−20 to +75	° C
Storage Temperature Range	T_{stg}	−40 to +125	° C

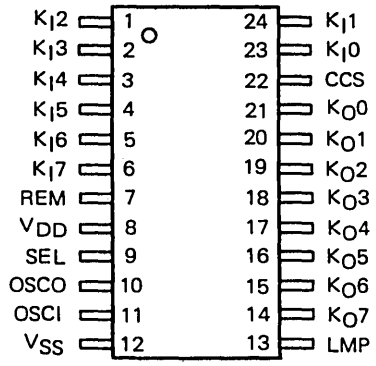
RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	2.0	3.0	3.3	V
Oscillation Frequency	f_{osc}	400	455	500	kHz
Lamp Output Current	$I_{OL(LMP)}$		1		mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V_{DD} = 3.0 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Current	$I_{DD(OP)}$		0.1	1.0	mA	f_{OSC} = 455 kHz
Supply Current	$I_{DD(ST)}$			1	μA	f_{OSC} = STOP
Input High Voltage	$V_{IH(KI)}$	0.7 V_{DD}		V_{DD}	V	
Input Low Voltage	$V_{IL(KI)}$	0		0.3 V_{DD}	V	
Input Pull Down Resister	R(KI)	150	300	600	kΩ	
Output Current	$I_{OH(REM)}$	−5	−13		mA	$V_{OH(REM)}$ = 1.5 V
Output Low Voltage	$V_{OL(LMP)}$		0.17	0.3	V	I_{OL} = 1.0 mA

Connection Diagram (Top View)



Terminal		
1	K_I2	Key Input 2
2	K_I3	Key Input 3
3	K_I4	Key Input 4
4	K_I5	Key Input 5
5	K_I6	Key Input 6
6	K_I7	Key Input 7
7	REM	Remote Output
8	V_{DD}	3 V
9	SEL	64/128 Data Select
10	OSCO	Oscillator Output
11	OSCI	Oscillator Input
12	V_{SS}	
13	LMP	Lamp Output
14	K_O7	Key Output 7
15	K_O6	Key Output 6
16	K_O5	Key Output 5
17	K_O4	Key Output 4
18	K_O3	Key Output 3
19	K_O2	Key Output 2
20	K_O1	Key Output 1
21	K_O0	Key Output 0
22	CCS	Custom Code Select Input
23	K_I0	Key Input 0
24	K_I1	Key Input 1

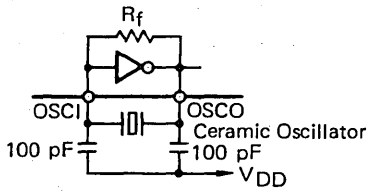
1. Key In & Out Pins $K_I0 \sim K_I7$, $K_O0 \sim K_O7$

Pull down resistors are connected between key input pins and V_{SS}. Simultaneous pressing of several keys activates the multiple input inhibiting circuit, thus making no transmission. Two key inputs with the interval of less than 36 ms is regarded as simultaneous. Priority of two inputs separating more than 36 ms is given on the first-pressed-first-served or longer-pressed-first-served basis.

Reading of the custom and key data codes starts at the press of a key, and 36 ms later REM output starts. One transmission is given if the key is kept pressed during this 36 ms. If the key is pressed for more than 108 ms, the leader code is only transmitted continuously. A very fast response is assured as the minimum ON-to-ON interval of 108 ms is discernible.

2. Oscillation Pins OSCI, OSCO

The oscillation circuit is only activated by a key input. Adjustment works can be saved if a 400-500 kHz ceramic resonator is used.

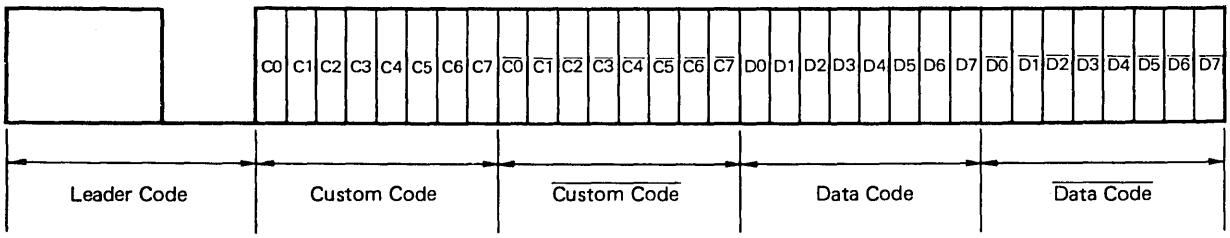


3. Power Supply Pins V_{DD}, V_{SS}

The standard voltage is 3 V or two dry cells. The workable range is 2.0 to 3.3 V. The stand-by current drain is only 1 μA as oscillation is only activated by the press of a key.

4. Remote Output REM

The transmission output consists of the leader code, 8-bit custom code, another 8-bit data code and the complementary codes of custom and data totalling 32 bits as shown below.



The leader code consists of 9 ms carrier and 4.5 ms OFF wave forms and works as the leader of the succeeding codes. This enables effective usage of time relations between reception detection and other processings when the receiver is micro-computerized. The succeeding codes are pulse position modulated (P.P.M.) and the 1 or 0 state depends on the time between pulses. Each code consists of eight bits and their complementary codes are simultaneously transmitted. This assures very low failure rate operation.

The data code has eight bits and D_0 to D_6 except D_5 can be selected by the key matrix K_1 to K_{64}. On double key pressing D_5 is given 1.

When the same key remains pressed the leader code is only transmitted repeatedly for saving of the infrared LED power drain. In this case the leader code transmission duty is predominant and the average power drain of the LED is about 3 % of I (peak). In case of 455 kHz oscillation the signal is modulated by 1/3 duty 38 kHz.

5. DATA 7 Select SEL

D7 is controlled by the SEL pin enabling the transmission of 128 codes. The SEL pin connected to V_{DD} and V_{SS} gives 0 and 1 to D7 respectively.

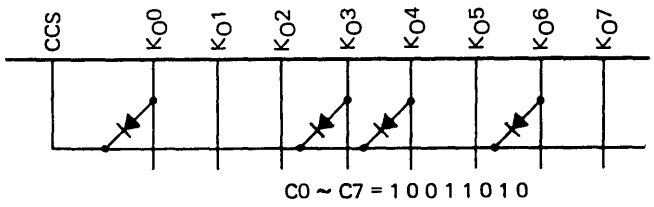
SEL V_{DD} . . . . . $D_7 = 0$
V_{SS} . . . . . $D_7 = 1$

6. Custom Code Select CCS

Available at REM output pin are 256 custom codes (C_0 to C_7) depending on external diodes connected between CCS (Custom Code Select) pin and key output pins.

Our customer who likes to use the code other than "00000000" (no diodes connected) may get our suggestion of customer codes for the prevention of interference with other customers' products. Custom codes is common between NEC's IC μPD1913C, μPD1943G and μPD6102G.

Example of Custom Code



C0 ~ C7 = 1 0 0 1 1 0 1 0

Key Data Code

KEY	CONNECTION					DATA CODE								NOTES
	K_I0	K_I1	K_I2	K_I3	K_O	D0	D1	D2	D3	D4	D5	D6	D7	
K1	*				K_O0	0	0	0	0	0	0	0	0/1	
K2		*				1	0	0	0	0	0	0	0/1	
K3			*			0	1	0	0	0	0	0	0/1	
K4				*		1	1	0	0	0	0	0	0/1	
K5	*				K_O1	0	0	1	0	0	0	0	0/1	N/A for μPD1913C
K6		*				1	0	1	0	0	0	0	0/1	
K7			*			0	1	1	0	0	0	0	0/1	
K8				*		1	1	1	0	0	0	0	0/1	
K9	*				K_O2	0	0	0	1	0	0	0	0/1	
K10		*				1	0	0	1	0	0	0	0/1	
K11			*			0	1	0	1	0	0	0	0/1	
K12				*		1	1	0	1	0	0	0	0/1	
K13	*				K_O3	0	0	1	1	0	0	0	0/1	N/A for μPD1913C
K14		*				1	0	1	1	0	0	0	0/1	
K15			*			0	1	1	1	0	0	0	0/1	
K16				*		1	1	1	1	0	0	0	0/1	
K17	*				K_O4	0	0	0	0	1	0	0	0/1	
K18		*				1	0	0	0	1	0	0	0/1	
K19			*			0	1	0	0	1	0	0	0/1	
K20				*		1	1	0	0	1	0	0	0/1	
K21	*				K_O5	0	0	1	0	1	0	0	0/1	
K22		*				1	0	1	0	1	0	0	0/1	
K23			*			0	1	1	0	1	0	0	0/1	
K24				*		1	1	1	0	1	0	0	0/1	
K25	*				K_O6	0	0	0	1	1	0	0	0/1	
K26		*				1	0	0	1	1	0	0	0/1	
K27			*			0	1	0	1	1	0	0	0/1	
K28				*		1	1	0	1	1	0	0	0/1	
K29	*				K_O7	0	0	1	1	1	0	0	0/1	N/A for μPD1913C
K30		*				1	0	1	1	1	0	0	0/1	
K31			*			0	1	1	1	1	0	0	0/1	
K32				*		1	1	1	1	1	0	0	0/1	
KEY	COEENCTION					DATA CODE								NOTES
	K_I4	K_I5	K_I6	K_I7	K_O	D0	D1	D2	D3	D4	D5	D6	D7	
K33	*				K_O0	0	0	0	0	0	0	1	0/1	N/A for μPD1943G μPD1913C
K34		*				1	0	0	0	0	0	1	0/1	
K35			*			0	1	0	0	0	0	1	0/1	
K36				*		1	1	0	0	0	0	1	0/1	
K37	*				K_O1	0	0	1	0	0	0	1	0/1	N/A for μPD1943G μPD1913C
K38		*				1	0	1	0	0	0	1	0/1	
K39			*			0	1	1	0	0	0	1	0/1	
K40				*		1	1	1	0	0	0	1	0/1	
K41	*				K_O2	0	0	0	1	0	0	1	0/1	N/A for μPD1943G μPD1913C
K42		*				1	0	0	1	0	0	1	0/1	
K43			*			0	1	0	1	0	0	1	0/1	
K44				*		1	1	0	1	0	0	1	0/1	
K45	*				N_O3	0	0	1	1	0	0	1	0/1	N/A for μPD1943G μPD1913C
K46		*				1	0	1	1	0	0	1	0/1	
K47			*			0	1	1	1	0	0	1	0/1	
K48				*		1	1	1	1	0	0	1	0/1	
K49	*				K_O4	0	0	0	0	1	0	1	0/1	N/A for μPD1943G μPD1913C
K50		*				1	0	0	0	1	0	1	0/1	
K51			*			0	1	0	0	1	0	1	0/1	
K52				*		1	1	0	0	1	0	1	0/1	
K53	*				K_O5	0	0	1	0	1	0	1	0/1	N/A for μPD1943G μPD1913C
K54		*				1	0	1	0	1	0	1	0/1	
K55			*			0	1	1	0	1	0	1	0/1	
K56				*		1	1	1	0	1	0	1	0/1	
K57	*				K_O6	0	0	0	1	1	0	1	0/1	N/A for μPD1943G μPD1913C
K58		*				1	0	0	1	1	0	1	0/1	
K59			*			0	1	0	1	1	0	1	0/1	
K60				*		1	1	0	1	1	0	1	0/1	
K61	*				K_O7	0	0	1	1	1	0	1	0/1	N/A for μPD1943G μPD1913C
K62		*				1	0	1	1	1	0	1	0/1	
K63			*			0	1	1	1	1	0	1	0/1	
K64				*		1	1	1	1	1	0	1	0/1	

N/A = Not Available

7. Double Key Operation

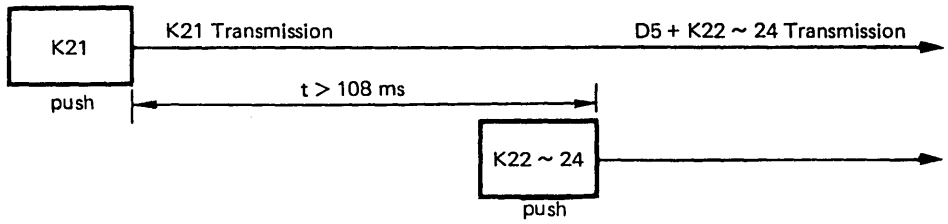
Double key input activates the multiple input inhibiting circuit except K21 to K24.

When a pair of key inputs, K21+K22, K21+K23 or K21+K24, gives 1 to D_5. But this function is assured only when one of the key K22 to K24 is pressed 108 ms at the minimum after K21.

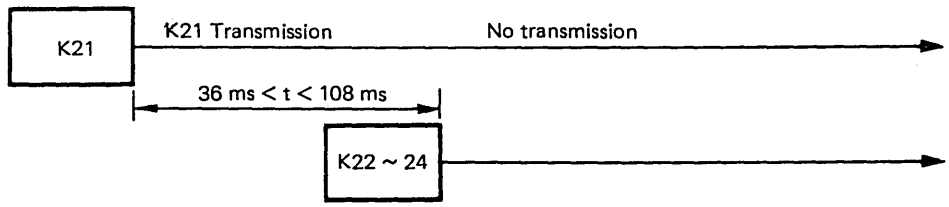
The inhibiting function assures the prevention of malfunction of, say, a tape deck in recording.

KEY	D0	D1	D2	D3	D4	D5	D6	D7
K21 + K22	1	0	1	0	1	1	0	0
K21 + K23	0	1	1	0	1	1	0	0
K21 + K24	1	1	1	0	1	1	0	0

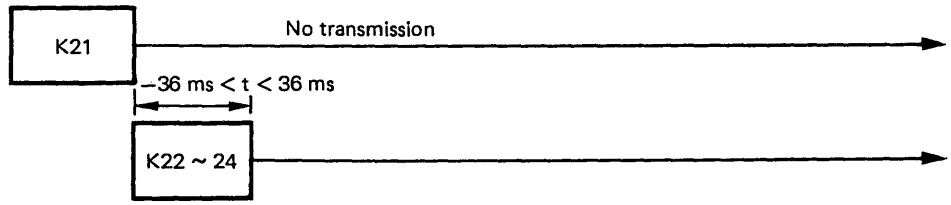
(a) Operation



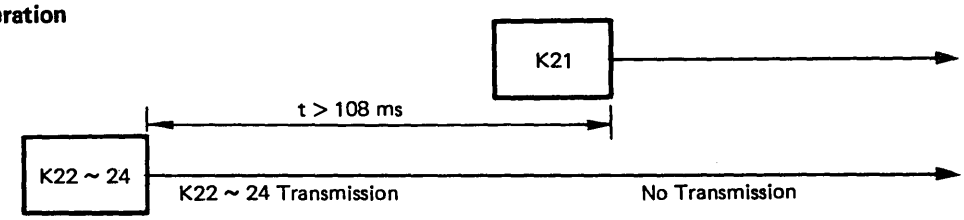
(b) No operation



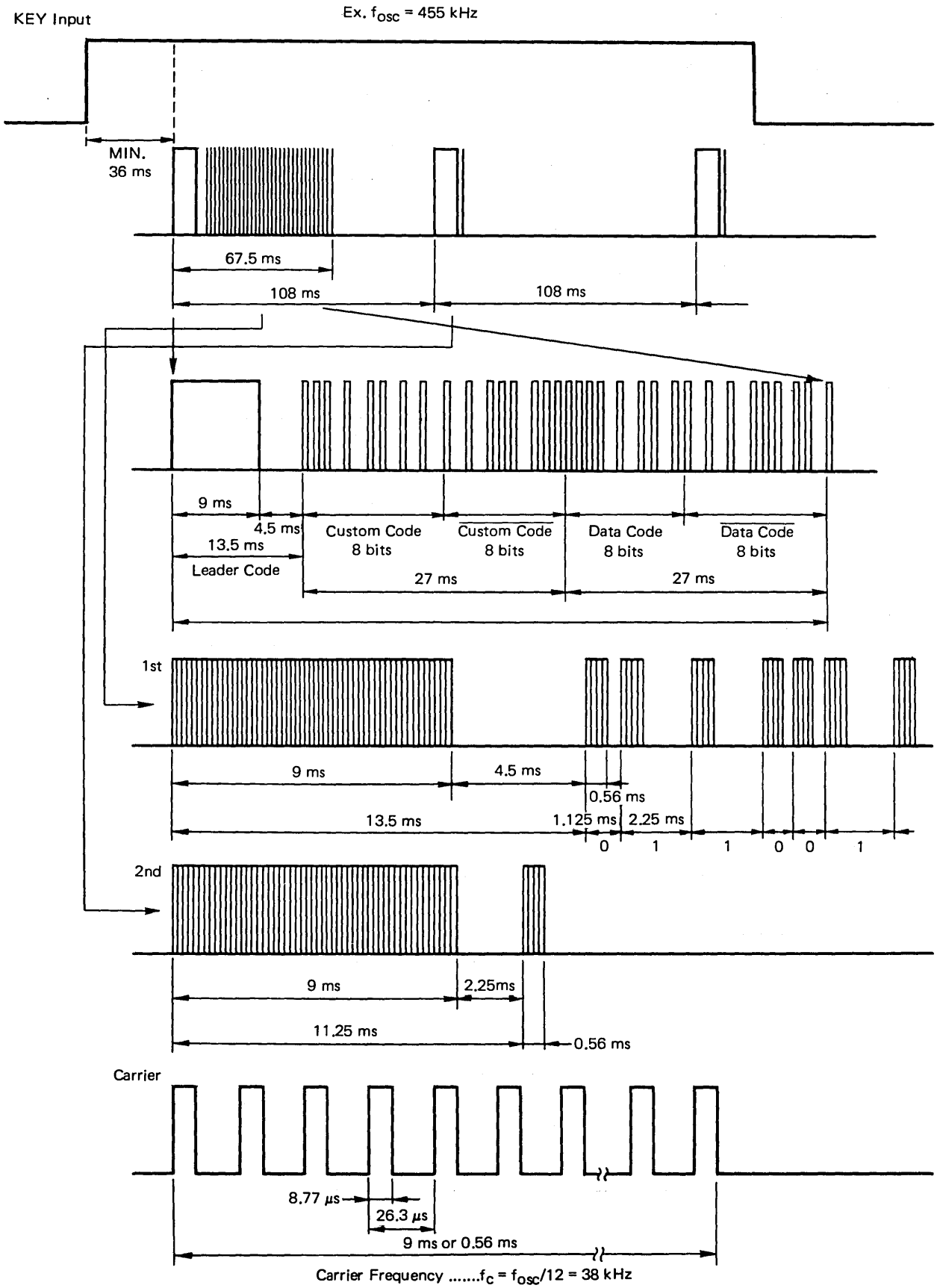
(c) No operation



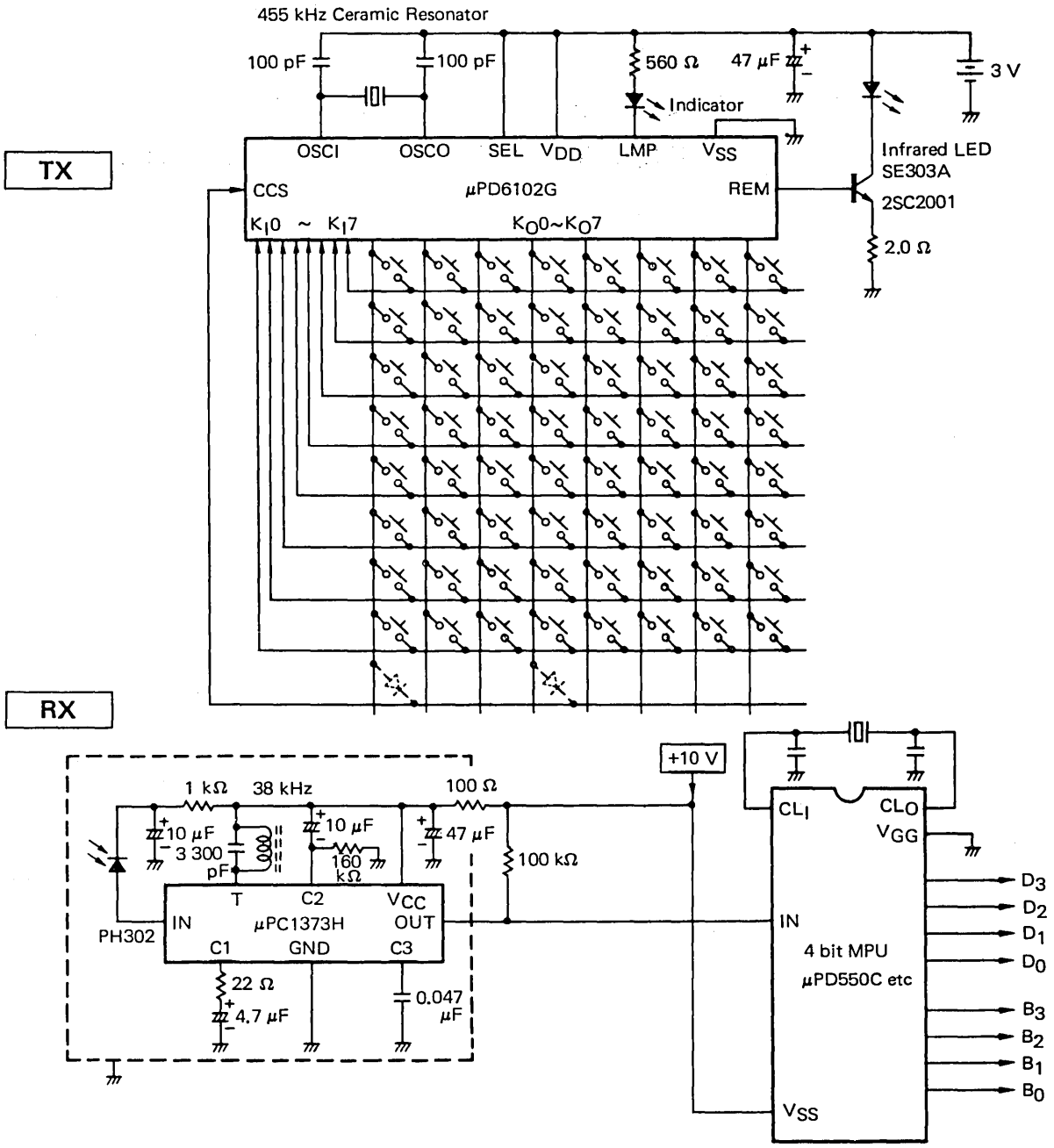
(d) No operation



Remote Output Waveforms



APPLICATION



SE303A . . . . . Infrared LED
PH302 . . . . . PIN Photo Diode
μPC1373H . . . . . Preamplifier for Remote Control
RX IC . . . . . TV use
PLL . . . . μPD1700 Series
VTR, VIDEODISC, STEREO, AIRCONTROL, OTHERS
4 bit CPU . . . μcom 43 series
μcom 7500 series
8 bit CPU μPD8048, 8049
μPD7800 series

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1356C2

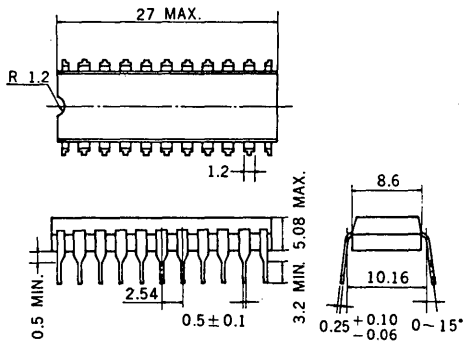
COMPLETE PICTURE IF IC FOR COLOR TV
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

The μPC1356C2 is a silicon monolithic integrated circuit for PIF section in Color Television receivers. As it contains picture detector and sound IF detector separatedly, it can offer excelent low buzz characteristics. This IC has all functions including picture IF amplifier (4th), picture low-level detector, sound IF detector, AFC detector, IF AGC, RF AGC and picture amplifier.

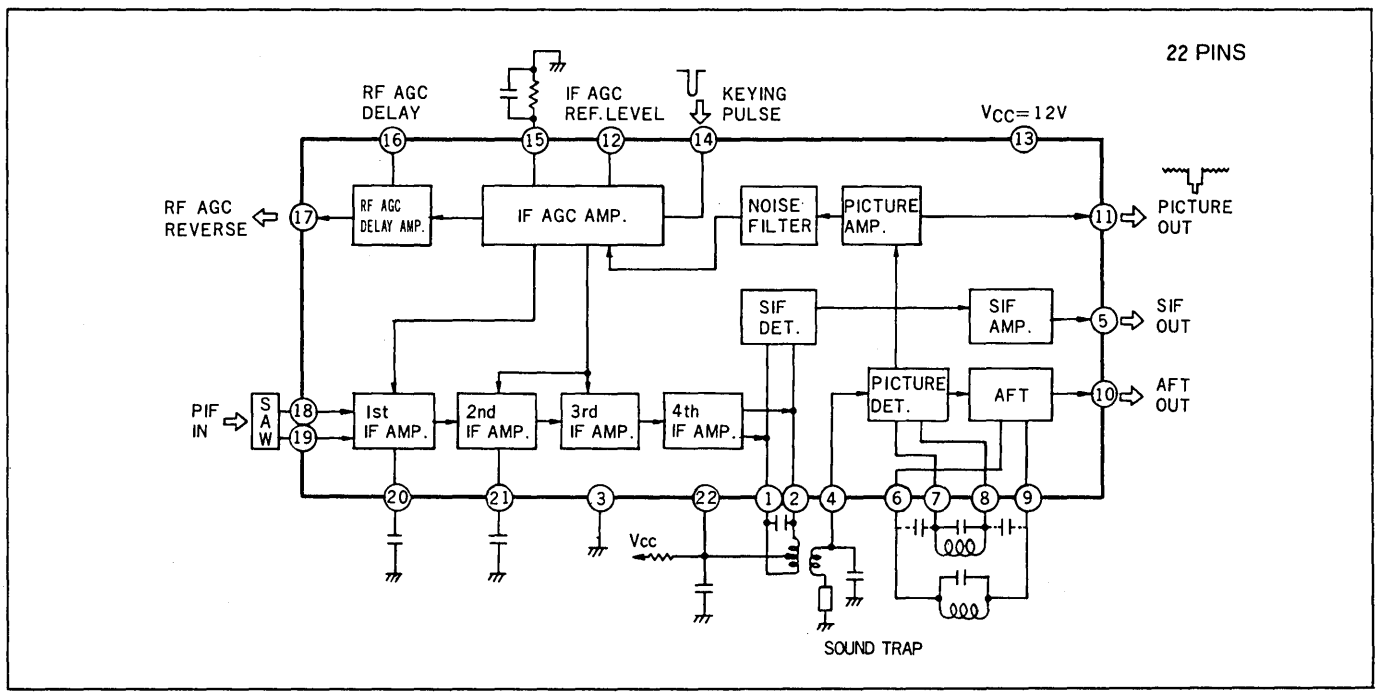
FEATURES

- As it contains picture detector and sound IF detector separatedly, it can offer excellent low buzz characteristics for Audio Multiptex TV.
- High input sensitivity; TYP. 32 dBμ
- The AGC control range is wide; TYP. 70 dB
- As input is differential mode, it can be used with SAW filter.

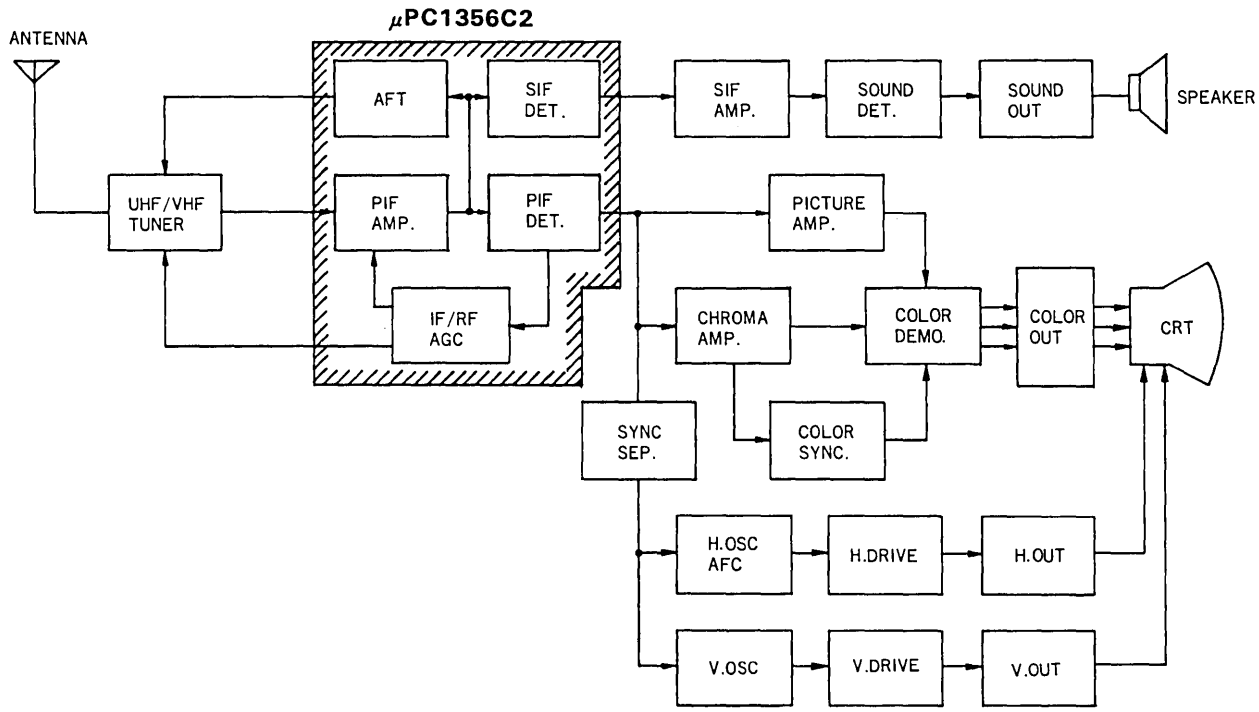
PACKAGE DIMENSIONS (Unit: mm)



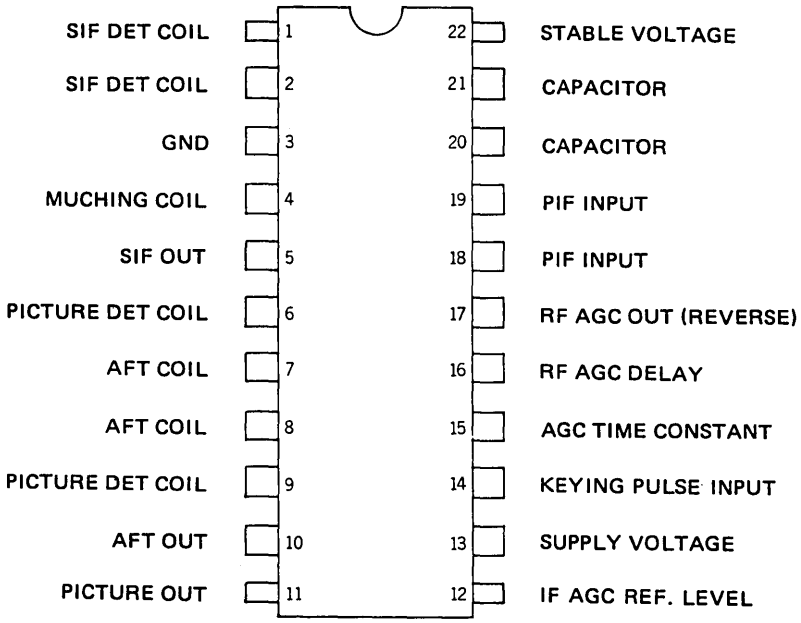
BLOCK DIAGRAM



TV BLOCK DIAGRAM



CONNECTION DIAGRAM (Top View)



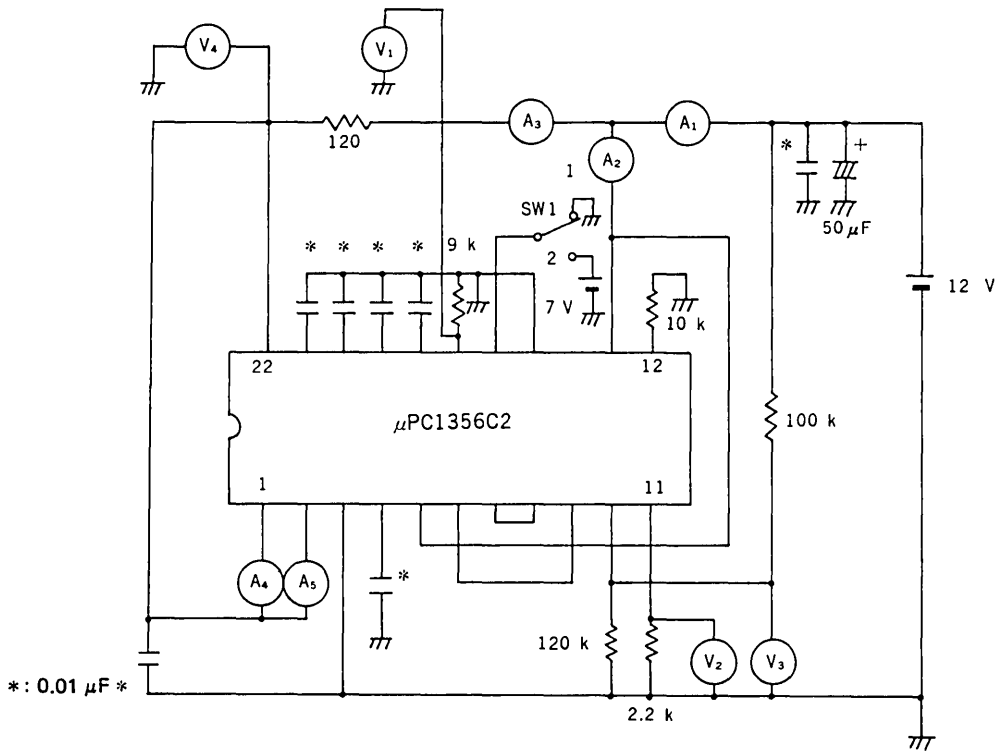
ABSOLUTE MAXIMUM RATINGS (Ta = 25 ±3 °C)

Supply Voltage Pin-13	$V_{13MAX.}$	15	V
Terminal 22 Current	$I_{22MAX.}$	100	mA
Terminal 14 Current	$I_{14MAX.}$	±3	mA
Power Dissipation	P_d	900 (Ta ≦ 65 °C)	mW
Operating Temperature	T_{opt}	−15 to +65	°C
Storage Temperature	T_{stg}	−40 to +125	°C

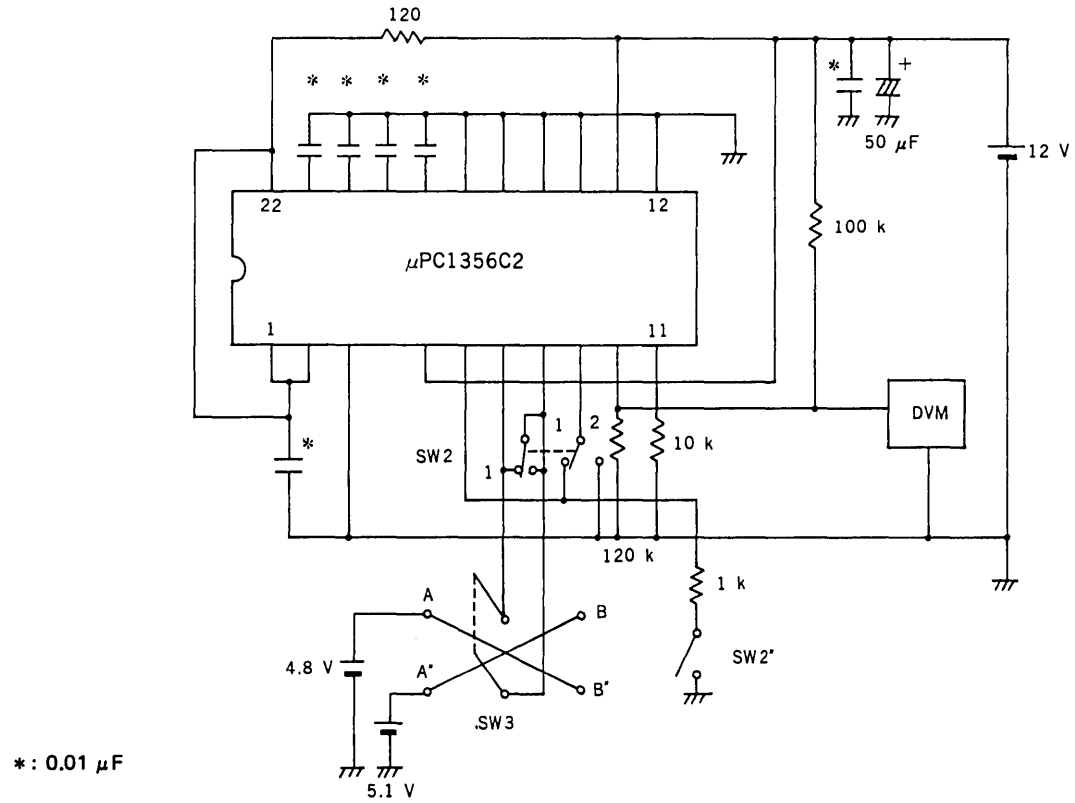
ELECTRICAL CHARACTERISTICS (Ta = 25 °C, V_{CC} = 12 V, R_A = 120 Ω, f_P = 58.75 MHz)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Total Supply Current	I_{CC}	1	55	70	90	mA	Zero Carrier
Terminal 13 Current	I_{13}	1	20	30	40	mA	Zero Carrier
Terminal 22 Current	I_{22}	1	35	40	50	mA	Zero Carrier
Terminal 22 Voltage	V_{22}	1	6.6	7.2	7.6	V	
Maximum RF AGC Voltage	V_{17H}	1	9.0	9.2	10.0	V	V_{16} = 7 V
Minimum RF AGC Voltage	V_{17L}	1		0	0.5	V	V_{16} = 0 V
Terminal 11 Voltage	V_{11}	1	3.7	4.1	4.7	V	
Terminal 10 Voltage	V_{10}	2	5.0	6.5	7.7	V	
Maximum AFT Out Voltage	V_{10H}	2	11.0			V	V_7 = 4.8 V V_8 = 5.1 V
Minimum AFT Out Voltage	V_{10L}	2			1.0	V	V_7 = 5.1 V V_8 = 4.8 V
Input Sensitivity	$v_{i(lim)}$	3	25	32	41	dBμ	fm = 400 Hz m = 40 % v_o = 0.8 Vp-p
AGC Range	G.R	3	60	80		dB	fm = 10 kHz m = 40 % v_o = 0.8 Vp-p
Maximum Input Voltage	$v_{i(MAX)}$	3	100	55		mVr.m.s.	fm = 10 kHz m = 40 % v_o = 0.8 Vp-p
Signal To Noise Ratio	S/N	3	50			dB	fm = 15.75 kHz m = 80 % v_o = 1.5 Vp-p v_i = 10 mVr.m.s.
SIF Output Voltage	$v_{o(SIF)}$	3	12	25	50	mVrms	fm = 400 Hz m = 40 % $v_{i(P)}$ = 3 mVr.m.s. fs = 54.25 MHz $v_{i(s)}$ = 300 μVr.m.s.
Carrier Leak	$CL_{(DET)}$	3		5	50	mVr.m.s.	v_i = 20 mVr.m.s.
Picture Frequency Response	f_C	3	5	13		MHz	m = 40 % v_i = 20 mVr.m.s.
Differential Gain	DG	3		5		%	fp = 58.75 MHz Stair Step fm = 3.58 MHz m = 85 % 14 % Modulated White To Sync Level $v_{o(DET)}$ = 1.4 Vp-p
Differential Phase	DP	3		5		deg	
AFT Control Sensitivity	Sf	3	50	150		mV/kHz	fm = 400 Hz m = 40 % v_o = 0.8 Vp-p
AFT Band Width	BW	3	0.2	1.1	2.1	MHz	fm = 400 Hz m = 40 % v_o = 0.8 Vp-p
PIF Input Resistance	R_i	4		1.5		kΩ	
PIF Input Capacitance	C_i	4		3.5		pF	

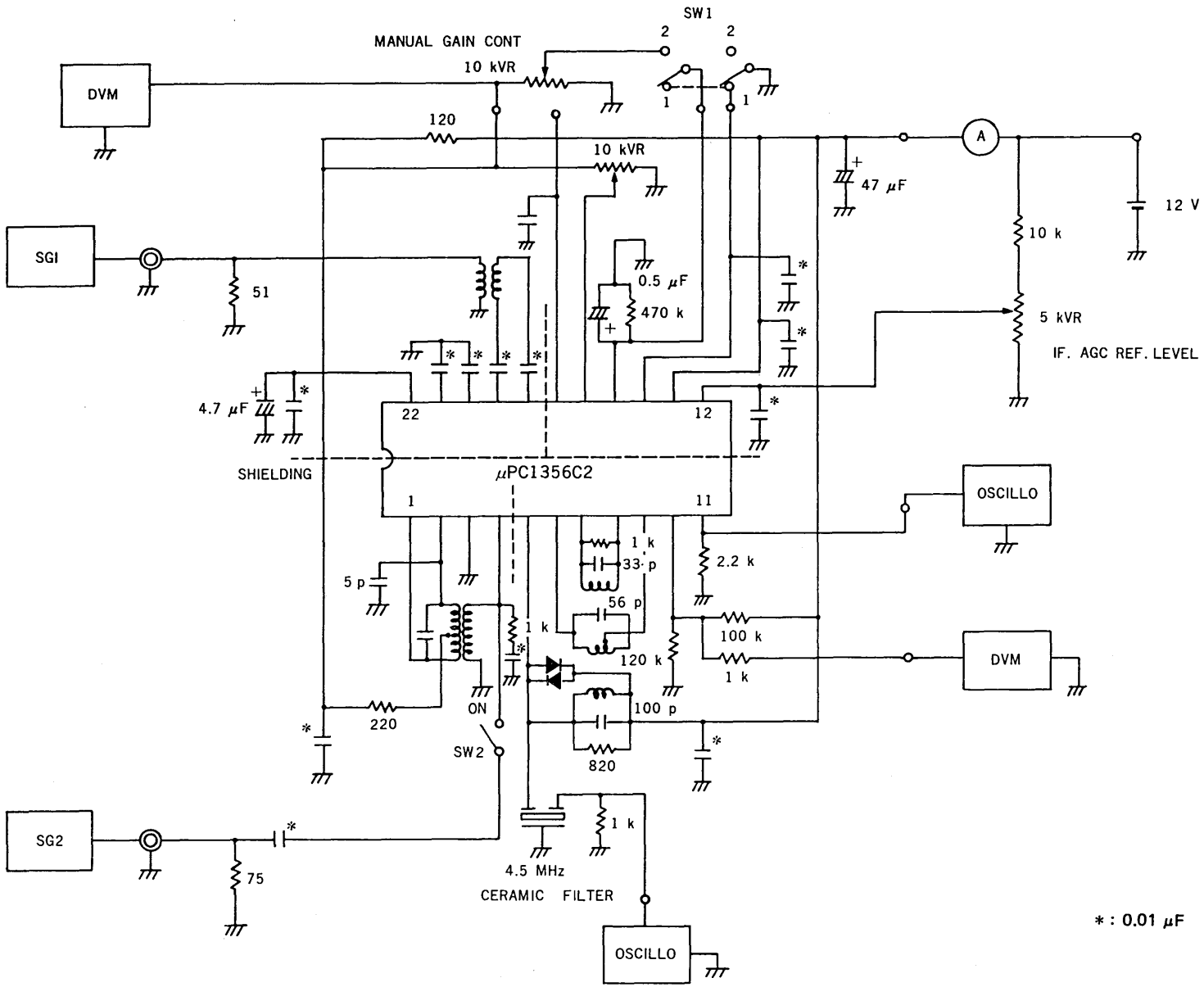
TEST CIRCUIT 1



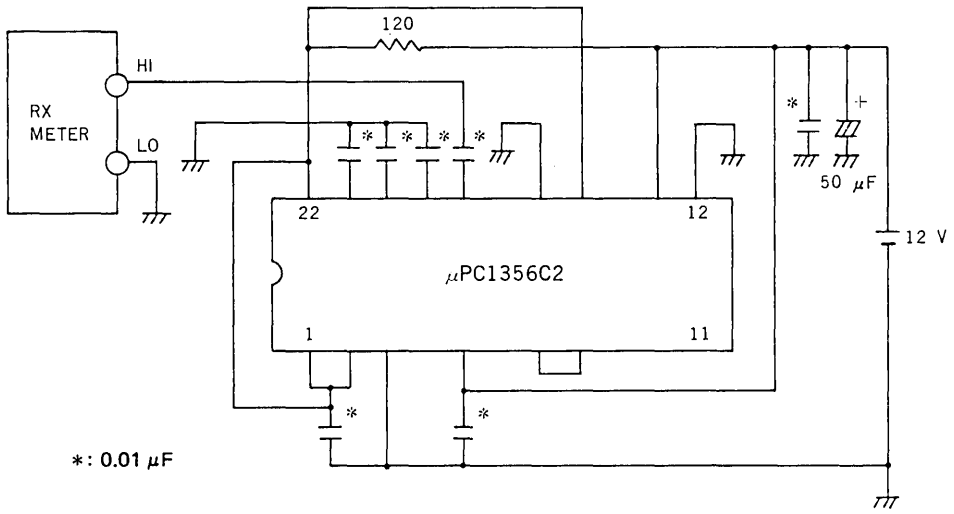
TEST CIRCUIT 2



TEST CIRCUIT 3



TEST CIRCUIT 4



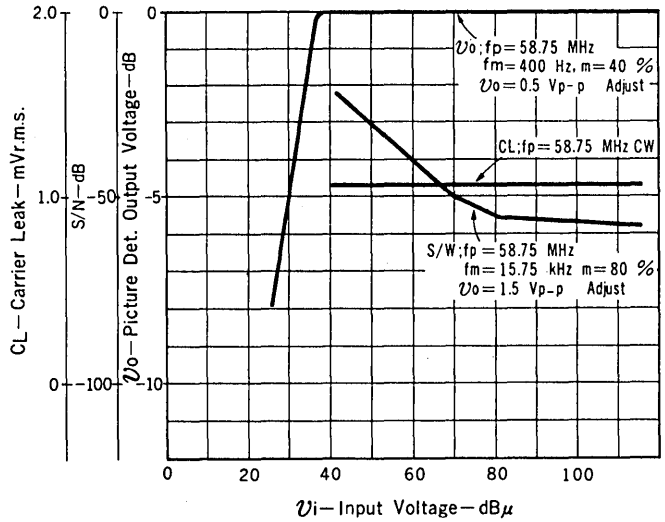
SWITCH TABLE

ITEM	I_{CC}	I_{13}	I_{22}	V_{22}	I_1, I_2	ΔI	V_{17H}	V_{17L}	V_{11}	V_{10}	V_{10H}	V_{10L}
TEST CIRCUIT	1	1	1	1	1	1	1	1	1	2	2	2
SW1	1	1	1	1	1	1	2	1	1	–	–	–
SW2	–	–	–	–	–	–	–	–	–	1 SW2 OFF	2	2
SW3	–	–	–	–	–	–	–	–	–	OFF	AA'	BB'
METER	A_1	A_2	A_3	A_4	A_4A_5	A_4A_5	V_1	V_1	V_2	V_3	V_3	V_3

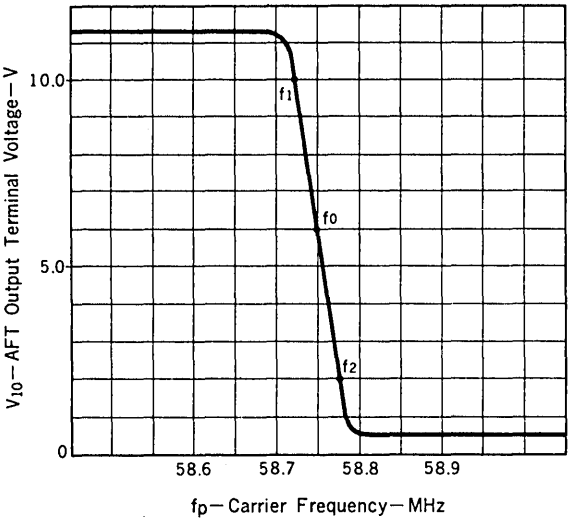
ITEM	$V_{i(Jm)}$	G.R.	V_{iMAX}	S/N	$V_{o(SIF)}$	$CL_{(DET)}$	f_C	D.G.	D.P.	S_f	B	R_i	C_i
TEST CIRCUIT	3	3	3	3	3	3	3	3	3	3	3	4	4
SW1	1	1	1	2	1	2	2	2	2	2	2	–	–
SW2	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON	ON	–	–
MGCVR				VARIABLE		MGC GAIN MIN	MGC GAIN MIN	MGC GAIN MIN	MGC GAIN MIN	MGC GAIN MIN	MGC GAIN MIN		
SG	SG_1	SG_1	SG_1	SG_1	SG_1	SG_2	SG_2	SG_2	SG_2	SG_2	SG_2	–	–
METER	OSCILLO	OSCILLO	OSCILLO	NOISE METER	OSCILLO	VTVM	OSCILLO	DG/DP METER	DG/DP METER	DIGIT VOLT METER	DIGIT VOLT METER	RX METER	RX METER

TYPICAL CHARACTERISTICS (Ta = 25 °C)

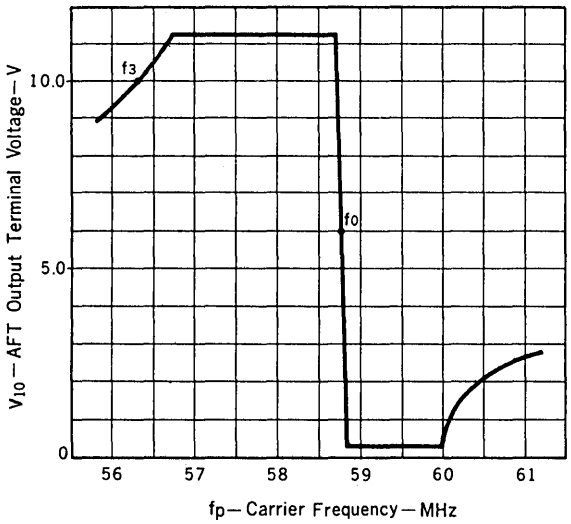
PICTURE DET. OUTPUT VOLTAGE, S/N, CARRIER LEAK vs. INPUT VOLTAGE



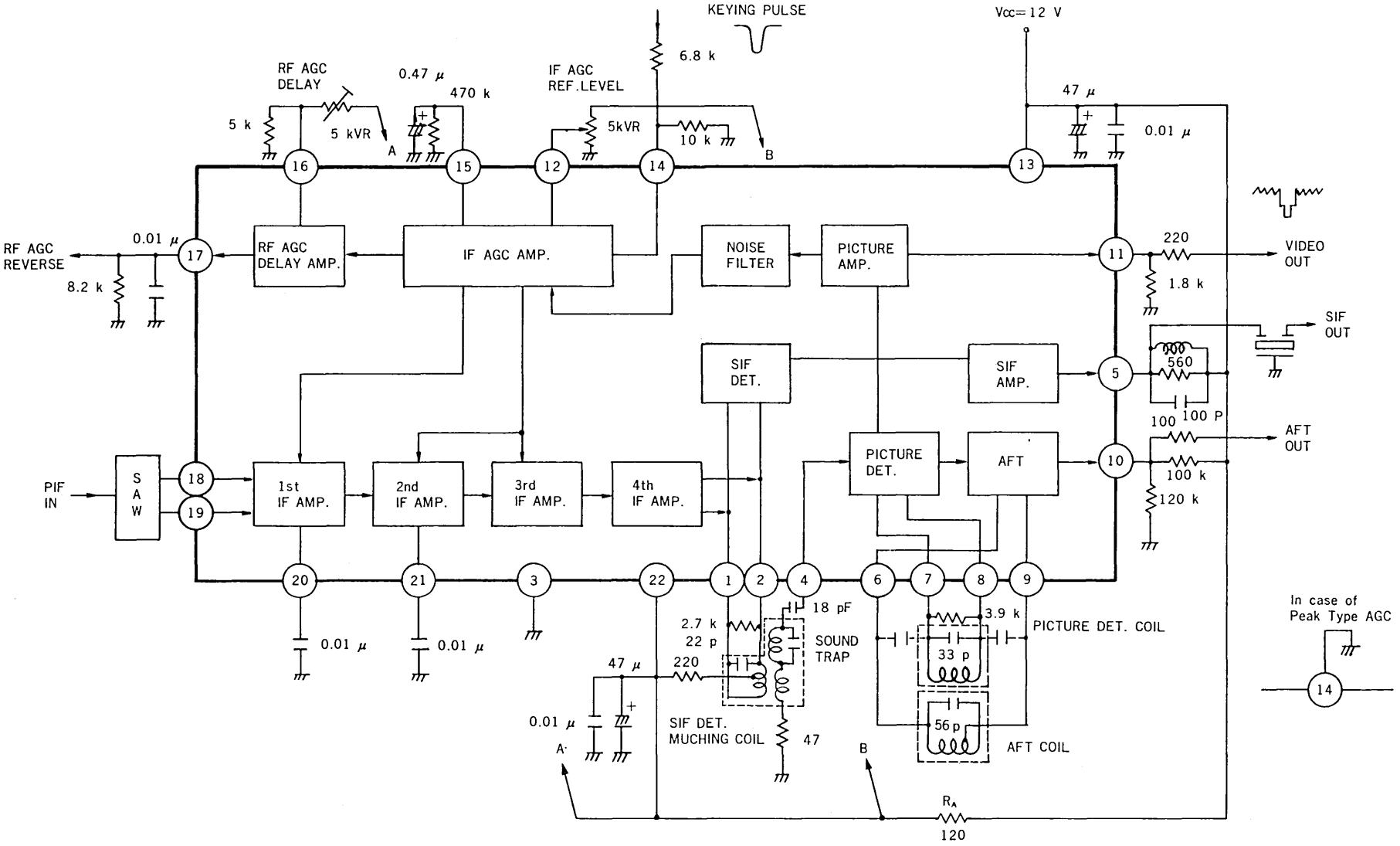
AFT OUTPUT TERMINAL VOLTAGE vs. CARRIER FREQUENCY – 1



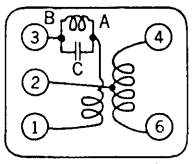
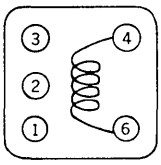
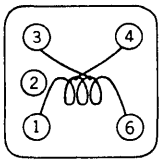
AFT OUTPUT TERMINAL VOLTAGE vs. CARRIER FREQUENCY – 2



STANDARD APPLICATION CIRCUIT



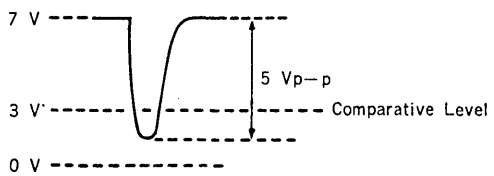
COIL SPEC. (COIL MAKER; TOKO, INC.)

COIL DRAWING (BOTTOM VIEW)	ITEM	f_P = 57 MHz SPEC.	f_P = 45 MHz SPEC.
SIF DET. MUCHING COIL 	TYPE No.	13 TD	13 TD
	COIL No.	TV4BVC – 21132AFQ	TV4BVC – 21135AFQ
	TURN	4–6 5½ T 6–2 2½ T 2–4 3 T 1–A 4½ T A–B 3 T C 100 pF	4–6 7½ T 6–2 3½ T 2–4 4 T 1–A 5½ T A–B 5 T C 100 pF
	WIRE	0.2 φ 2 UEW A–B 1.0 φ TINNED WIRE	0.2 φ 2 UEW A–B 1.0 φ TINNED WIRE
PICTURE DET. COIL 	TYPE No.	10 KN	10 KN
	COIL No.	180PNA – 10212BS	180PNA – 10223BS
	MUCHING C.	33 pF	40 pF
	NO LOAD Q.	96 ± 20 %	95 ± 20 %
	TURN	4–6 6 T	4–6 6½ T
	WIRE	0.16 φ 2 UEW	0.16 φ 2 UEW
AFT COIL 	TYPE No.	10KN	10KN
	COIL No.	180PNAS – 10232ALR	180PNAS – 10235ALR
	MUCHING C.	33 pF	33 pF
	NO LOAD Q.	93±20 %	97±20 %
	TURN	6–1 5 T 6–3 1¾ T 6–4 3¼ T	6–1 7 T 6–3 2¾ T 6–4 4 T
	WIRE	0.23 φ 2 UEW	0.23 φ 2 UEW

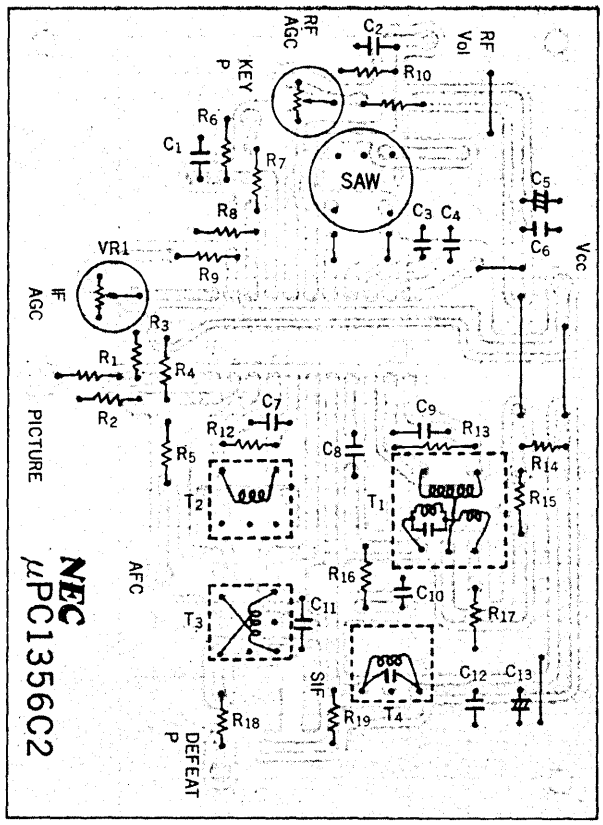
STANDARD USING CONDITION (Ta = 25 °C)

Supply Voltage	V_{CC}	12	V
PIF Input Voltage	v_i	10	mVr.m.s.
Keying Pulse		*5	V_{p-p}
RF AGC Voltage	V_6	2~5	V

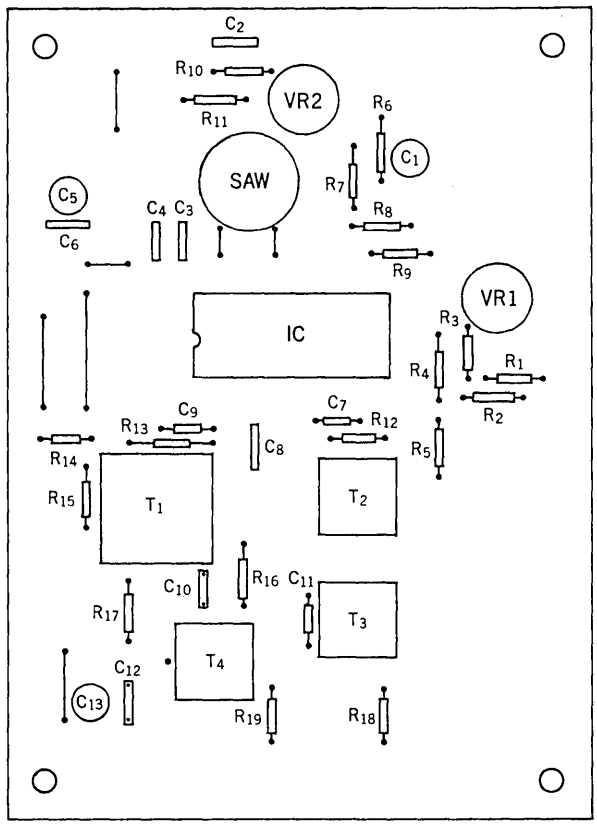
*Keying Pulse



● P.C. BOAD PATTERN



COMPONENTS LAYOUT



COMPONENTS (For f_P = 57 MHz)

SYMBOL	SPEC.	SYMBOL	SPEC.	
R_1	220 Ω	C_1	0.47 μF	10V
R_2	120 kΩ	C_2	0.01 μF	
R_3	1.8 kΩ	C_3	0.01 μF	
R_4	100 kΩ	C_4	0.01 μF	
R_5	100 Ω	C_5	47 μF	16V
R_6	470 kΩ	C_6	0.01 μF	
R_7	6.8 kΩ	C_7	20 pF	
R_8	10 kΩ	C_8	20 pF	
R_9	10 kΩ	C_9	20 pF	
R_{10}	8.2 kΩ	C_{10}	0.01 μF	
R_{11}	5 kΩ	C_{11}	33 pF	
R_{12}	3.9 kΩ	C_{12}	0.01 μF	
R_{13}	2.7 kΩ	C_{13}	47 μF	10V
R_{14}	120 Ω			
R_{15}	220 Ω	VR_1	5 kΩ-B	
R_{16}	1 kΩ	VR_2	5 kΩ-B	
R_{17}	47 Ω			
R_{18}	200 Ω	T_1	TO-KO	TV4BVC-21132AFQ
R_{19}	560 Ω	T_2	TO-KO	180PNA-10212BS
		T_3	TO-KO	180PNAS-10232ALR
		T_4	TO-KO	MTKAC-19951Z

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1366C

VIDEO IF PROCESSOR FOR B/W TV

DESCRIPTION

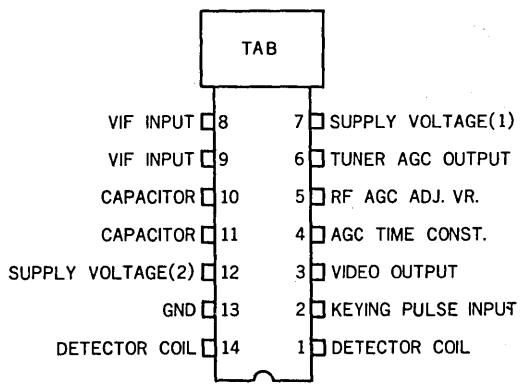
The μPC1366C is a silicon monolithic integrated circuit designed for VIF section in B/W television receivers. This IC has all functions including video IF amplifier, video low-level detector, RF AGC, IF AGC and noise canseller.

This IC is encapsulated in 14 pin dual in-line package with heat tab.

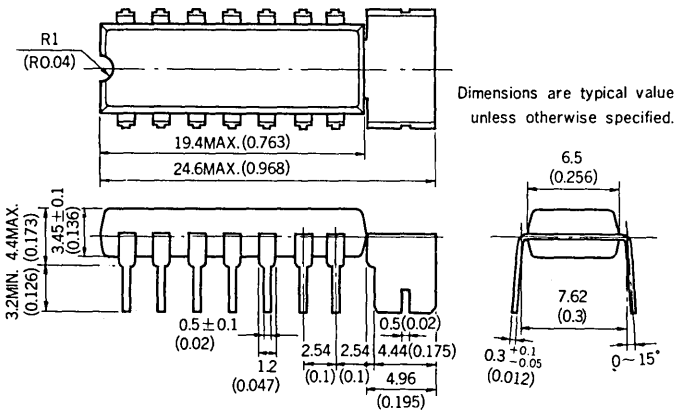
FEATURES

- High input sensitivity; TYP. 30dBμ.
- It can be used both of keyed type AGC and peak type AGC.
- It can be operated with the power supply voltage above 7V.
- Since the video detector has wide bandwidth, it's suitable for the sound carrier frequency of 4.5, 5.5, 6.0, 6.5MHz.
- As input is differential mode, it can be used with SAW filter.
- All functions for VIF stage are provided by this single chip IC and this IC will realize reduction of assembly cost as well as reduction of number of external components.

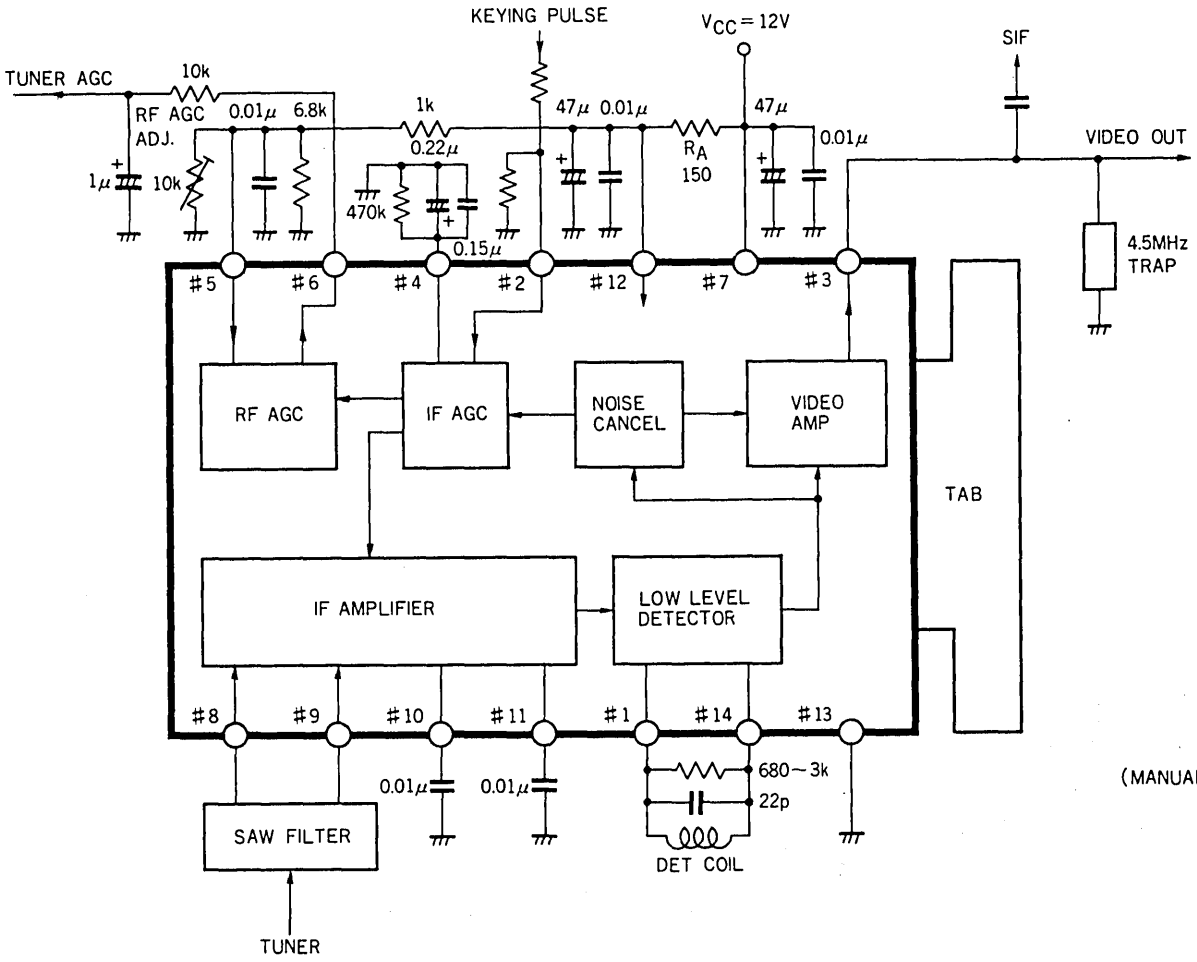
CONNECTION DIAGRAM (Top View)

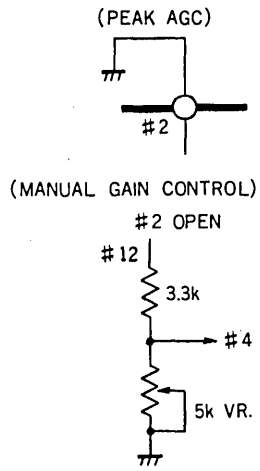


PACKAGE DIMENSIONS in millimeters (inches)



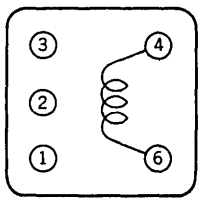
BLOCK DIAGRAM





DETECTOR COIL SPEC

TOKO 10KN TYPE 180PNA – 10212BS
frequency : 57MHz (C = 33pF±3%)
No load Q : 96±20%
Turn : 4 – 6 6T
Wire : 0.16φ 2UEW



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

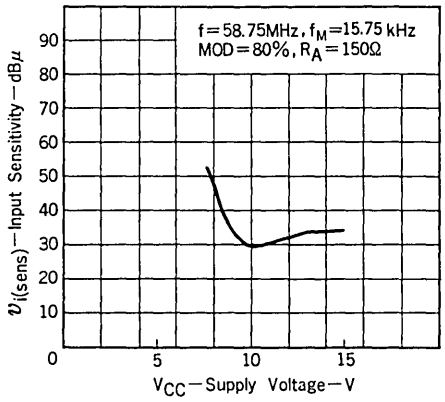
Supply Voltage Pin-7	V_7	15	V
Input Signal Voltage	V_8 V_9	3	Vp-p
Power Dissipation	P_d	875 (Ta = 75°C) Free Air	mW
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12V, Ta = 25±3°C, f = 58.75MHz, f_M = 15.75kHz)

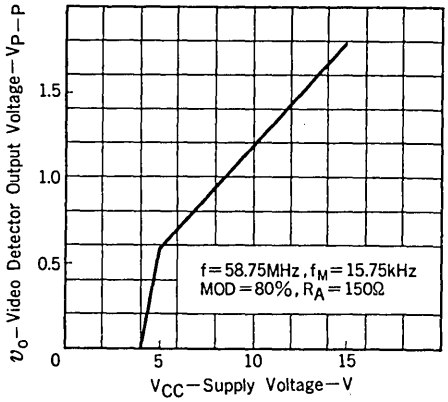
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Total Supply Current	I_{CC}	40	50	60	mA	I_7+I_{12}, R_A = 150Ω
Input Sensitivity	$v_{i(sens)}$		30	35	dBμ	MOD = 80%, v_o = 1.4Vp-p
Maximum Input Voltage	$v_{i(max.)}$	100			dBμ	MOD = 80%, −1dB Point
Video Output Voltage	v_o	1.0	1.4	1.7	Vp-p	MOD = 80%, v_i = 3mVr.m.s.
Video Output DC Voltage	V_o	3.3	3.8	4.3	V	No Signal
Signal to Noise Ratio	S/N	40	50		dB	MOD=80%~0%, v_i=3mVr.m.s.
RF AGC Voltage (High)	V_{6H}	8	9	11	V	V_5 = 0V
RF AGC Voltage (Low)	V_{6L}		0	0.5	V	V_5 = 7V
Differential Gain	D.G.			10	%	Stair Step f_M = 3.58MHz
Differential Phase	D.P.			10	deg	Stair Step f_M = 3.58MHz
Video Detector Band Width	BW	5.5			MHz	−3dB Point
Input Resistance	Rin		1.5		kΩ	
Input Capacitance	Cin		3.3		pF	

TYPICAL CHARACTERISTICS (Ta = 25°C)

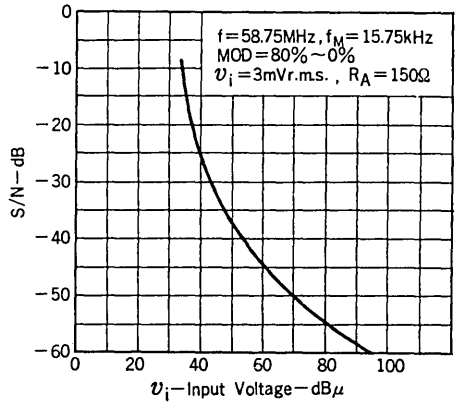
INPUT SENSITIVITY vs. SUPPLY VOLTAGE



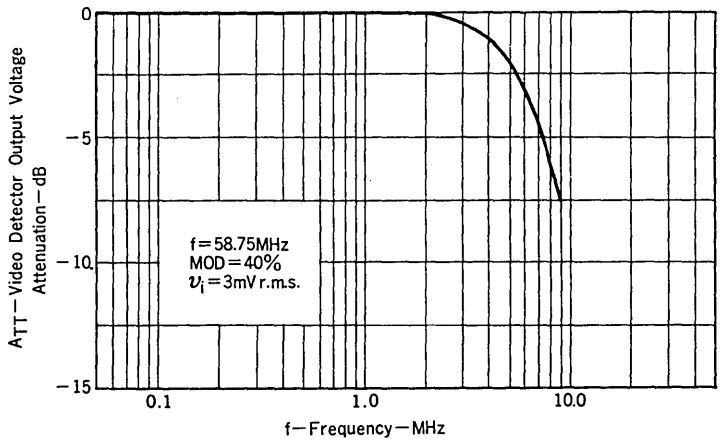
VIDEO DETECTOR OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



S/N vs. INPUT VOLTAGE



VIDEO DETECTOR OUTPUT VOLTAGE ATTENUATION vs. FREQUENCY



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1353C

2.4 WATTS AUDIO AMPLIFIER, SIF AMPLIFIER AND DETECTOR FOR TV SILICON MONOLITHIC BIPOLAR INTEGRATED CIRCUIT

DESCRIPTION:

The μPC1353C is a silicon monolithic integrated circuit designed for SIF and Audio section in television receivers. This IC has all functions including sound IF Amplifier, FM Detector, DC volume control circuit, Audio Output amplifier with 2.4 Watts output power and voltage regulator.
This IC is encapsulated in 14 pin dual in-line package with heat tab.

FEATURES:

1. All functions for SIF and audio stage are provided by this one-chip IC and this IC will realize reduction of assembly cost as well as reduction of number of other components.

2. Audio output power is controlled by electronic attenuation circuit which operate at DC. Therefore, unnecessary radiation, oscillation etc. are eliminated. Due to DC control, shielded wire is not required and variable resistor will be placed anywhere required.

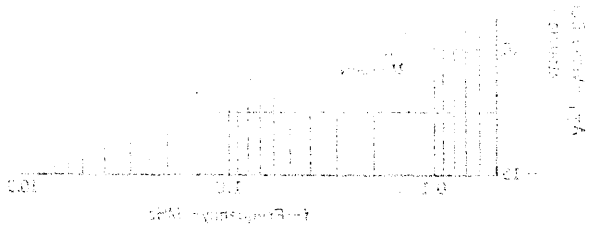
3. Electronic attenuator has enough attenuation (Typ. 80dB) by the adoption of squelch circuit.
   In addition, as attenuation characteristic is same with resistance change of variable resistor, suitable variable resistor will be selected easily.

4. As Peak differencial detection method is adopted for FM detection, outside circuitry can be very simple and circuit adjustment will be very easy.

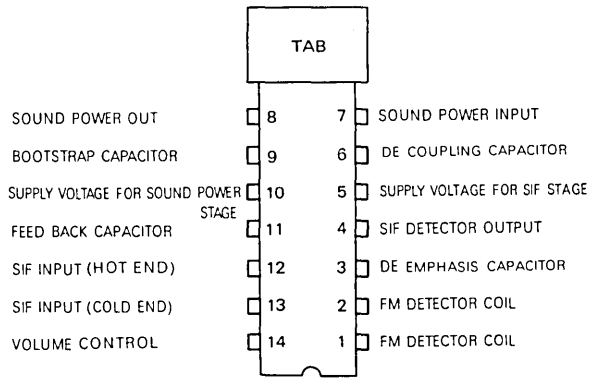
5. As operation voltage (Vcc) range for output stage is very wide (9-18V), suitable Vcc can be freely determined for required output level.

   For example:

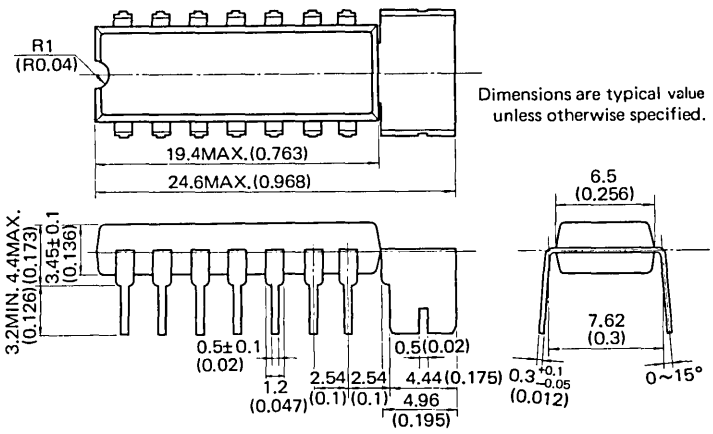
   Po = 2.4W at Vcc = 18V, R_L = 8 Ohms
   Po = 1.2W at Vcc = 12V, R_L = 8 Ohms



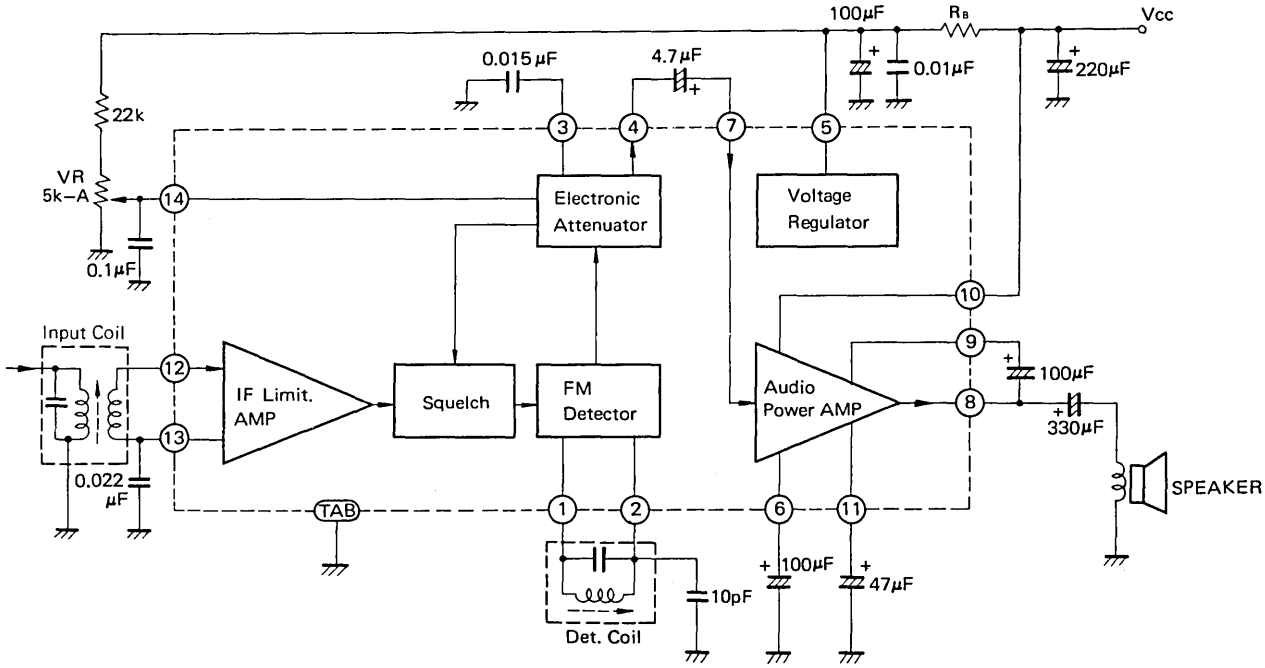
CONNECTION DIAGRAM (Top View)



PACKAGE DIMENSIONS in millimeters (inches)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Supply Voltage Pin 10	V_{10}	20	V
Supply Current Pin 10	I_{10}	1	A
Supply Current Pin 5	I_5	100	mA
Input Signal Voltage	Vi	3	V_{P-P}
Power Dissipation	P_{d1}	0.8 (Ta=75°C) FREE AIR	W
Power Dissipation	P_{d2}	1.4*	W
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +150	°C

* PRINTED CIRCUIT COPPER AREA 50x50 mm^2

ELECTRICAL CHARACTERISTICS (Ta=25±3°C)

1 IF STAGE (V_{CC}=12V R_B=100Ω R_g=50Ω V_{14}≥1.3V f_o=4.5MHz f_M=400Hz f=±25kHz)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Pin 5 Voltage	V_{5A}	7.5	8.0	8.5	V	
Pin 5 Voltage	V_{5B}	7.5	8.0	8.5	V	V_{CC}=18V R_B=330Ω
Pin 10 Current	I_{10A}	14	19	24	mA	NO INPUT SIGNAL
Pin 10 Current	I_{10B}	16	28	35	mA	V_{CC}=18V R_B=330Ω NO INPUT SIGNAL
IF Limiting Voltage	Vi(lim)		200	400	μVr.m.s.	V_{OAF}(Vi=10mVr.m.s.) −3dB
Detector Output Voltage	V_{oAF}	300	360		mVr.m.s.	Vi=10mVr.m.s.
Detector Distortion	T.H.D.$_1$		0.7		%	Vi=10mVr.m.s.
AM Rejection	AMR	−40	−50		dB	AM MOD 30% f_M= 400Hz Vi=10mVr.m.s.
Maximum Attenuation	ATT_{max}	−60	−80		dB	V_{14}=0V

2 SOUND POWER STAGE (V_{CC}=12V R_B=100Ω R_L=8Ω f=400Hz R_G=600Ω)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Sound Stage Voltage Gain	G_{VAF}	33	37	41	dB	Vi=30mVr.m.s.
Sound Output Power	PoA	0.9	1.2		W	T.H.D.=10%
Sound Output Power	PoB	2.0	2.4		W	V_{CC}=18V R_B=330Ω T.H.D.=10%
Sound Output Distortion	T.H.D.2A		0.6	2.0	%	Po=0.5W
Sound Output Distortion	T.H.D.2B		0.5	2.0	%	V_{CC}=18V R_B=330Ω Po=0.5W

3 IF STAGE + SOUND POWER STAGE

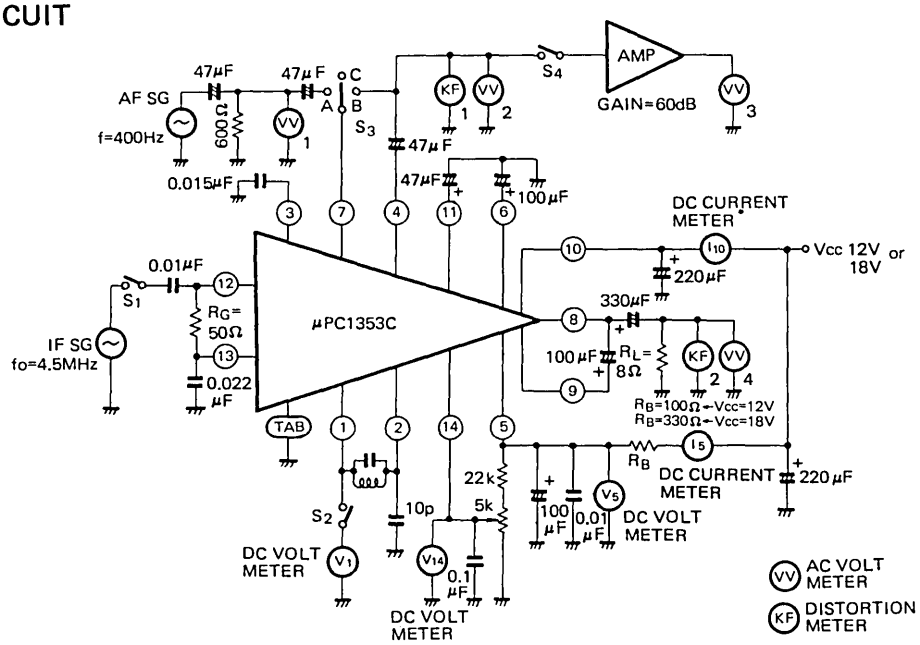
Over All Sound Output Distortion	T.H.D.$_3$		1.5	4.0	%	P_o = 0.5W Vi= 10mVr.m.s.

4 REFERENCE DATA

CHARACTERISTIC	SYMBOL		UNIT	TEST CONDITIONS
Pin 10 Current	I_{10}	200 ~ 210	mA	T.H.D.$_{2A}$=10%
Pin 10 Current	I_{10}	270 ~ 280	mA	T.H.D.$_{2B}$=10%
Sound Output Power	PoA'	1.1	W	T.H.D.=3%
Sound Output Power	PoB'	2.0	W	V_{CC}=18V R_B=330Ω T.H.D.=3%
Sound Stage Band Width	BW	50 ~ 50k	Hz	−3dB

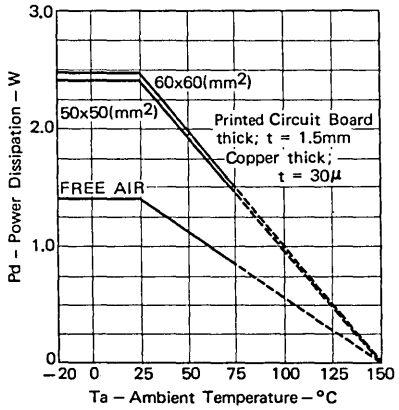
PIN INPEDANCE	fo=4.5 MHz		5.5 MHz		6.0 MHz		6.5 MHz		UNIT
	R	C	R	C	R	C	R	C	
Pin 12 IF Input	2	9.5	2	9.4	1.9	9.4	1.9	9.4	kΩ/pF
Pin 1 Detector Connect	2.4	6.3	2.4	6.2	2.4	6.1	2.4	6.1	kΩ/pF
Pin 2 Detector Connect	11.5	9	9	8.5	8.5	8.3	7.8	8.1	kΩ/pF

TEST CIRCUIT

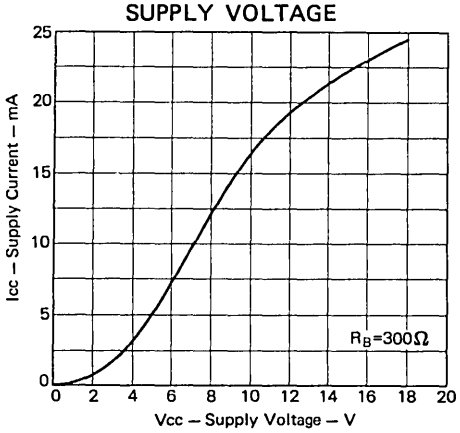


CHARACTERISTICS

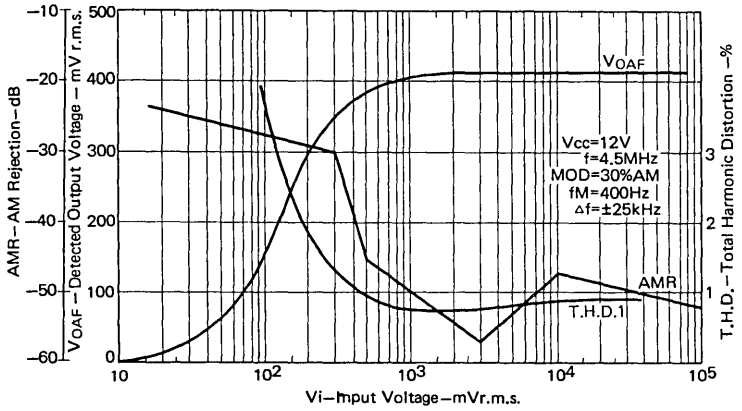
POWER DISSIPATION vs. AMBIENT TEMPERATURE



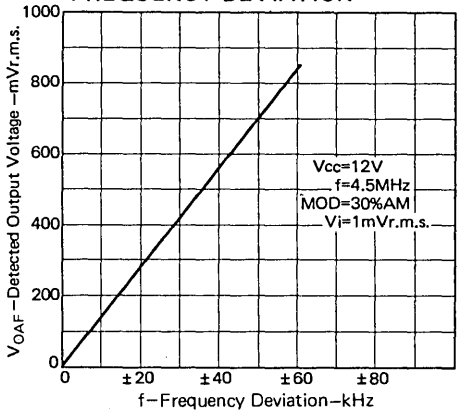
SUPPLY CURRENT vs. SUPPLY VOLTAGE



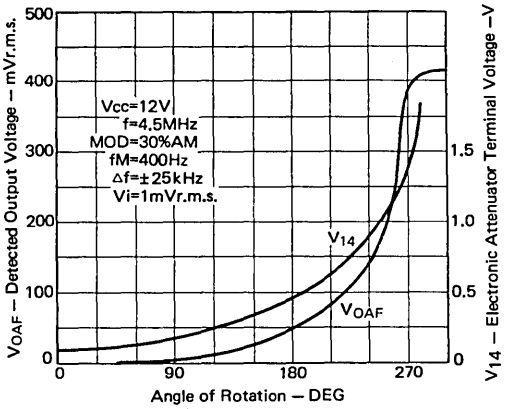
DETECTED OUTPUT VOLTAGE, AM REJECTION, TOTAL HARMONIC DISTORTION vs. INPUT VOLTAGE



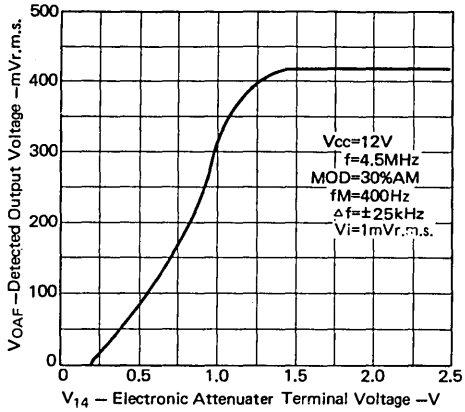
DETECTED OUTPUT VOLTAGE vs. FREQUENCY DEVIATION



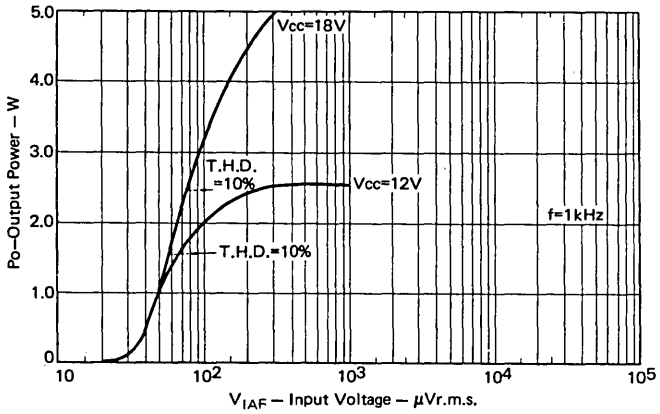
DETECTED OUTPUT VOLTAGE, ELECTRONIC ATTENUATER TERMINAL VOLTAGE vs. ANGLE OF ROTATION (A CURVE VOLUME)



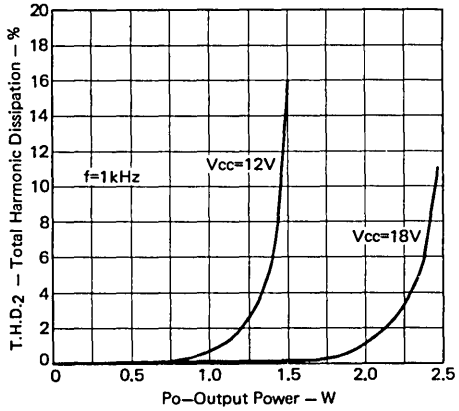
DETECTED OUTPUT VOLTAGE vs. ELECTRONIC ATTENUATER TERMINAL VOLTAGE



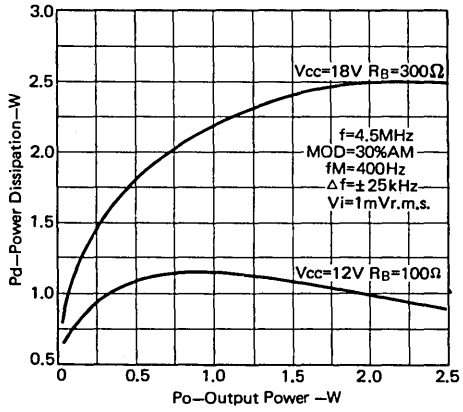
OUTPUT POWER vs. INPUT VOLTAGE (AUDIO AMPLIFIER STAGE)



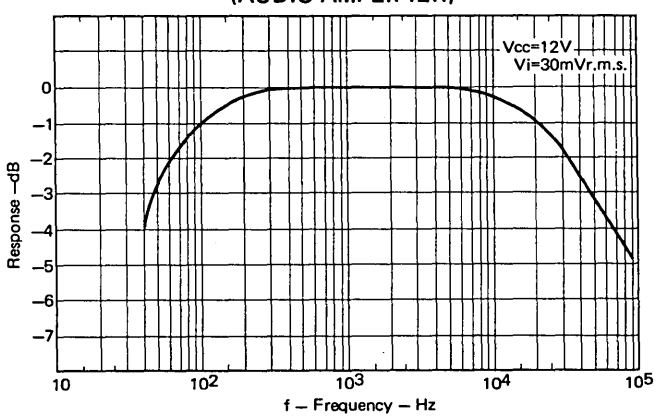
TOTAL HARMONIC DISTORTION (AUDIO AMPLIFIER STAGE) vs. OUTPUT POWER



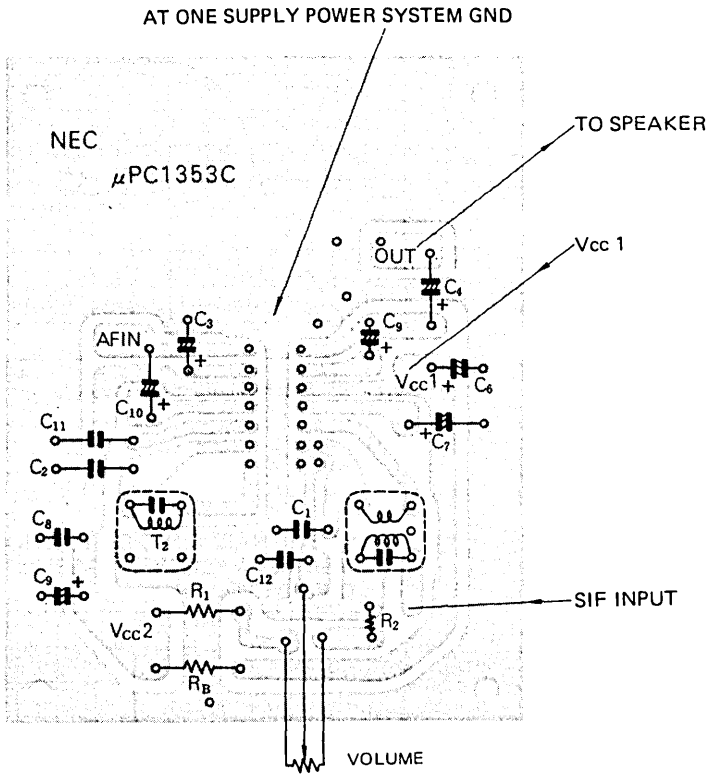
POWER DISSIPATION vs. OUTPUT POWER



FREQUENCY RESPONSE (AUDIO AMPLIFIER)



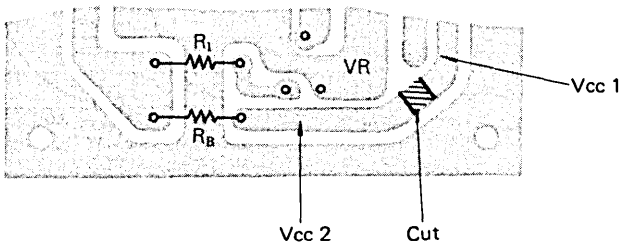
PRINTED CIRCUIT BOARD AND COMPONENTS TABLE



SYMBOL	CHARACTERISTIC
C1	CERAMIC 0.022 μF
C2	CERAMIC 10 pF
C3	CHEMICAL 100μF 10V
C4	CHEMICAL 330μF 25V
C5	CHEMICAL 100μF 25V
C6	CHEMICAL 220μF 25V
C7	CHEMICAL 47μF 10V
C8	CERAMIC 0.01μF
C9	CHEMICAL 100μF 10V
C10	CHEMICAL 4.7μF 10V
C11	CERAMIC 0.015μF
C12	CERAMIC 0.1μF

VR	5k-A Curve
T_1	INPUT COIL
T_2	DET. COIL

AT TWO SUPPLY POWER SYSTEM

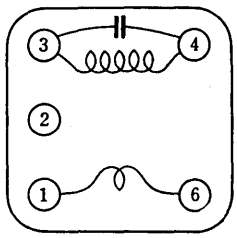


SYMBOL	CHARACTERISTIC
R_1	22k 1/4W
R_2	270 1/4W
R_B	100Ω or 330Ω 1/2W

COIL SPEC.

INPUT COIL

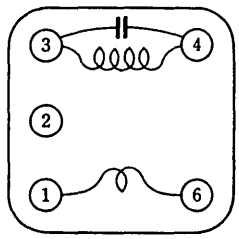
FOR 4.5MHz



3 – 4 20T
1 – 6 5T

C 82pF
fo 4.5MHz
Q_u 110±20%
Coil Material
0.1φ OUEW

FOR 5.5MHz

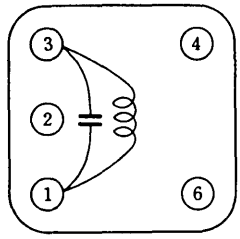


3 – 4 28T
1 – 6 4T

C 82pF
fo 5.5MHz
Q_u 59±20%
Coil Material
0.1φ OUEW

DETECTOR COIL

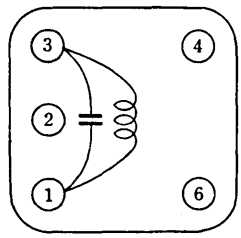
FOR 4.5MHz



1 – 3 24T

C 82pF
fo 4.5MHz
Qu 108±20%
Coil Material
0.1φ OUEW

FOR 5.5MHz

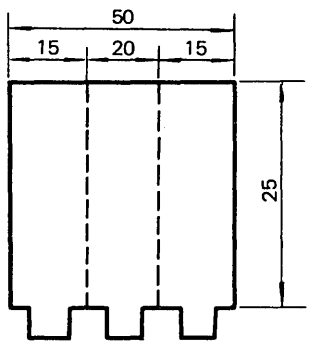


1 – 3 29T

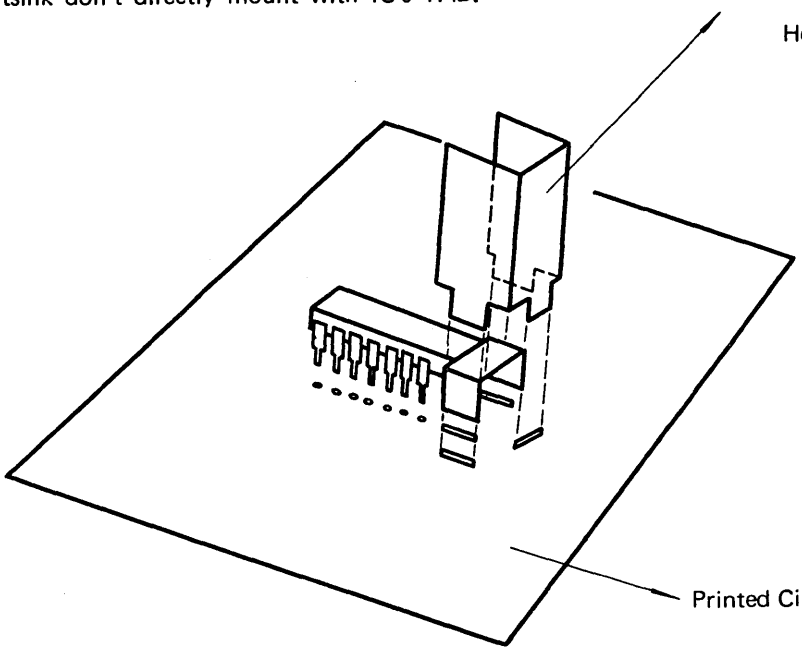
C 76pF
fo 5.5MHz
Q_u 49±20%
Coil Material
0.1φ OUEW

MOUNTING HEATSINK

The method of mounting the heatsink show below, in the case of heatsink need, when sound output power will be larger and the heatsink don't directly mount with IC's TAB.



Heat sink



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1382C

TV SOUND IF PROCESSOR AND ATTENUATOR

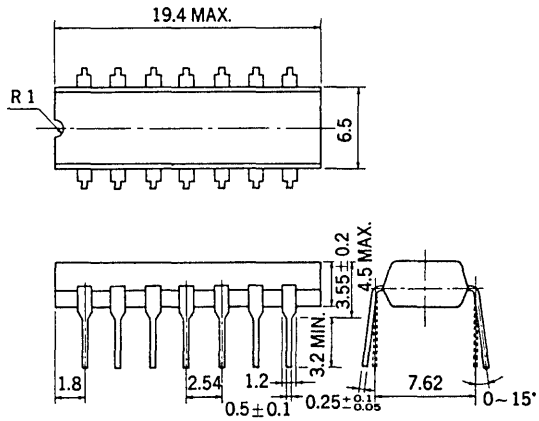
DISCRIPTION

μPC1382C is a TV sound IC. It can be operated with no adjustment, using ceramic filters externally. It contains a DC controlled attenuator, which has wide effective area and gentle characteristic in the chainging, so it is convenient especially for a remote controlled set.

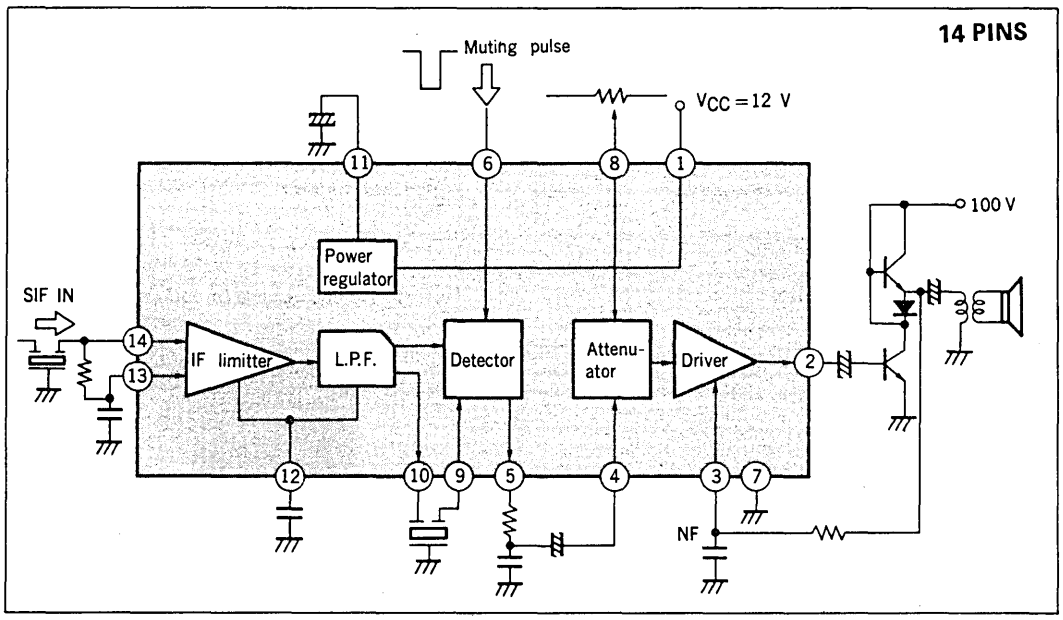
FEATURES

- Gentle chainging DC controlled attenuator is convenient for remote controlled sets.
- Operation with ceramic filters makes TV sound circuit no adjustment completely.
- SRPP output circuit can be driven directly.
- Muting works quickly.
- Low distortion demodulation.

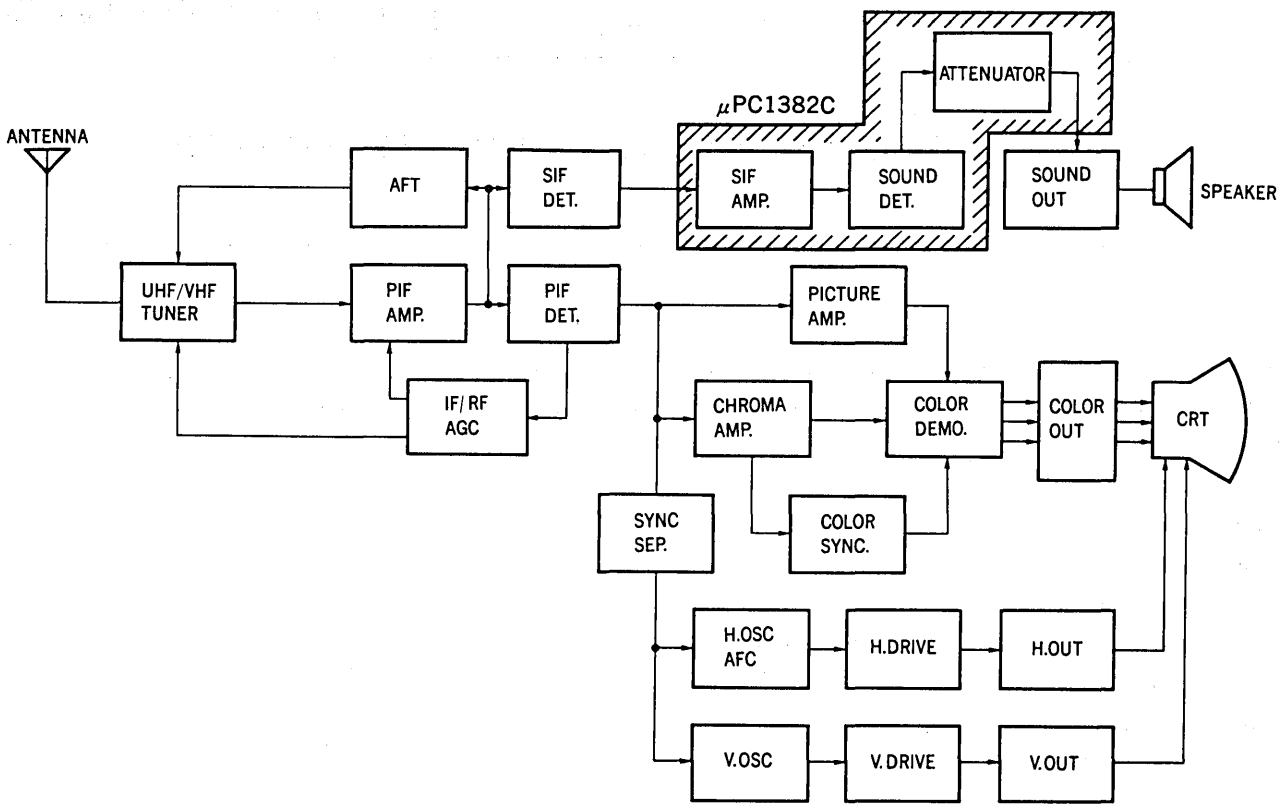
PACKAGE DIMENSIONS (Unit : mm)



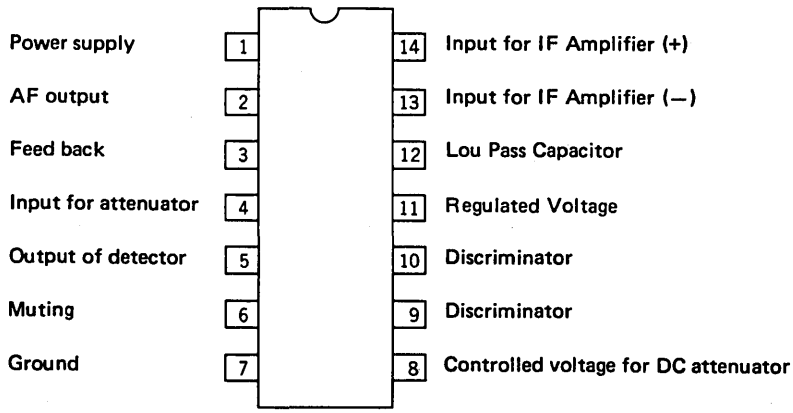
BLOCK DIAGRAM



TV BLOCK DIAGRAM



CONNECTION DIAGRAM (Top View)



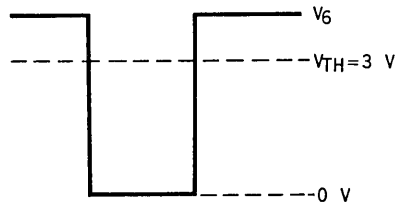
ABSOLUTE MAXIMUM RATINGS (Ta=25 °C)

Power supply voltage	V_{CC}	0 15	V
Pin 13, 14 voltage	V_{13}, V_{14}	0 5	V
Pin 2 output current	I_2	0 20	mA
Power dissipation	P_d	350 (Ta=75 °C)	mW
Operating temperature	T_{opt}	−20 to +75	°C
Storage temperature	T_{stg}	−40 to +125	°C

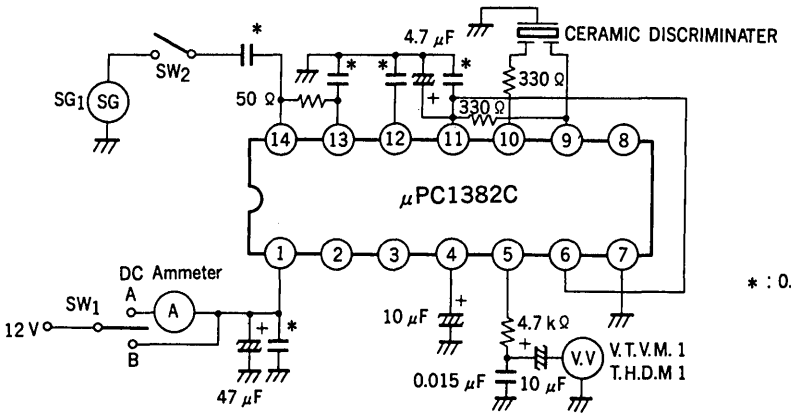
ELECTRICAL CHARACTERISTICS (V_{CC}=12 V, Ta=25±3 °C) *Mark f=4.5 MHz, Δf=±25 kHz, f_M=400 Hz, AMMOD=30 %

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CKT	CONDITION
Total supply current	I_{CC}	15	20	25	mA	1	V_{CC}=12 V Zero carrier
IF limitting voltage	$v_{i(lim)}$	–	200	400	μVr.m.s.	1	*−3 dB point
Detector output voltage	$v_{O\ AF}$	450	600	750	mVr.m.s.	1	* v_i=10 mVr.m.s.
Detector output distortion	$T.H.D._{DET}$	–	0.4	1.0	%	1	* v_i=10 mVr.m.s.
AM rejection	AMR	−44	−55	–	dB	1	* $v_i \geq 3$ mVr.m.s.
DC VR maximum attenuation	ATT_{VR}	70	80	–	dB	2	f_{in}=400 Hz, v_i=600 mVr.m.s.
DC VR distortion	$T.H.D._{VR}$	–	0.4	1.0	%	2	f_{in}=400 Hz, v_i=600 mVr.m.s. $V_8 \geq 5$ V
AF voltage gain	G_{VAF}	11.5	15.0	–	dB	2	f_{in}=400 Hz, v_i=100 mV.r.m.s. R_3=1 kΩ
IF input resistance	R_{in}		1.5		kΩ	3	
IF input capacitance	C_{in}		2.0		pF	3	
Pin 4 input resistance	R_{in4}		20		kΩ	3	
Pin 4 input capacitance	C_{in4}		2.8		pF	3	

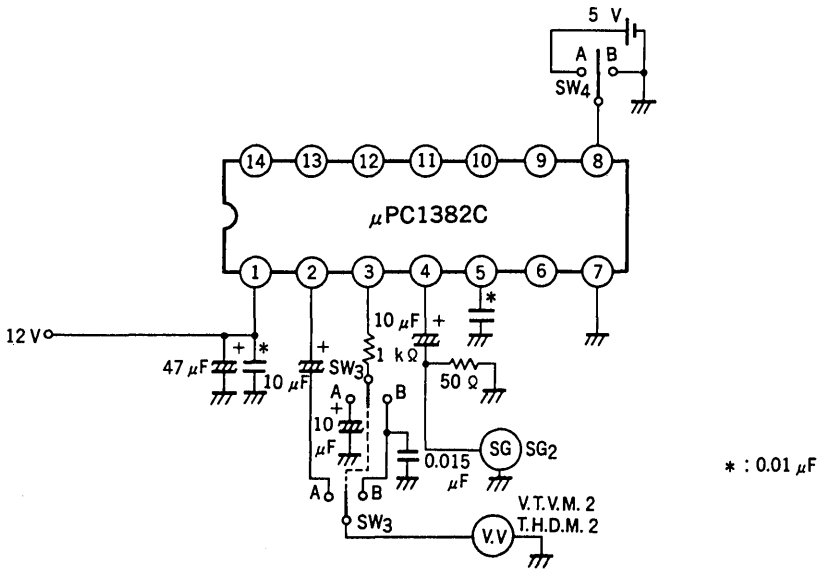
MUTING CHARACTERISTIC



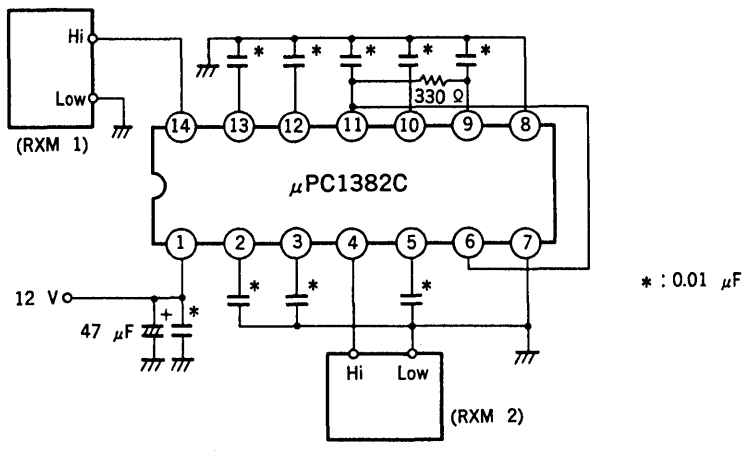
TEST CIRCUIT 1



TEST CIRCUIT 2



TEST CIRCUIT 3



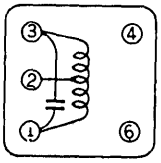
SWITCH TABLE

ITEM	CKT	SG	CONDITION	SW_1	SW_2	SW_3	SW_4	VV_1	VV_2	T.H.D. M1	T.H.D. M2	RX M1
I_{CC}	1	–	V_{CC}=12 V Zero carrier	A	OFF	–	–	O	–	–	–	–
$v_{i(lim)}$	1	SG_1	* –3dB point	B	ON	–	–	O	–	–	–	–
v_{OAF}	1	SG_1	* v_i=10 mVr.m.s.	B	ON	–	–	O	–	–	–	–
T.H.D.$_{DET}$	1	SG_1	* v_i=10 mVr.m.s.	B	ON	–	–	–	–	O	–	–
AMR	1	SG_1	* $v_i \geqq$ 3mVr.m.s.	B	ON	–	–	O	–	–	–	–
ATT_{VR}	2	SG_2	f_M=400 Hz, v_i=600 mVr.m.s.	–	–	B	A→B	–	O	–	–	–
T.H.D.$_{VR}$	2	SG_2	f_M=400 Hz, v_i=600 mVr.m.s.	–	–	B	A	–	–	–	O	–
G_{VAF}	2	SG_2	f_{in}=400 Hz, v_i=100 mVr.m.s.	–	–	A	A	–	O	–	–	–
R_{in}	3	–		–	–	–	–	–	–	–	–	1
C_{in}	3	–		–	–	–	–	–	–	–	–	1
R_{in4}	3	–		–	–	–	–	–	–	–	–	2
C_{in4}	3	–		–	–	–	–	–	–	–	–	2

* f=4.5 MHz, Δf=±25 kHz, f_M=400 Hz, AMMOD=30 %

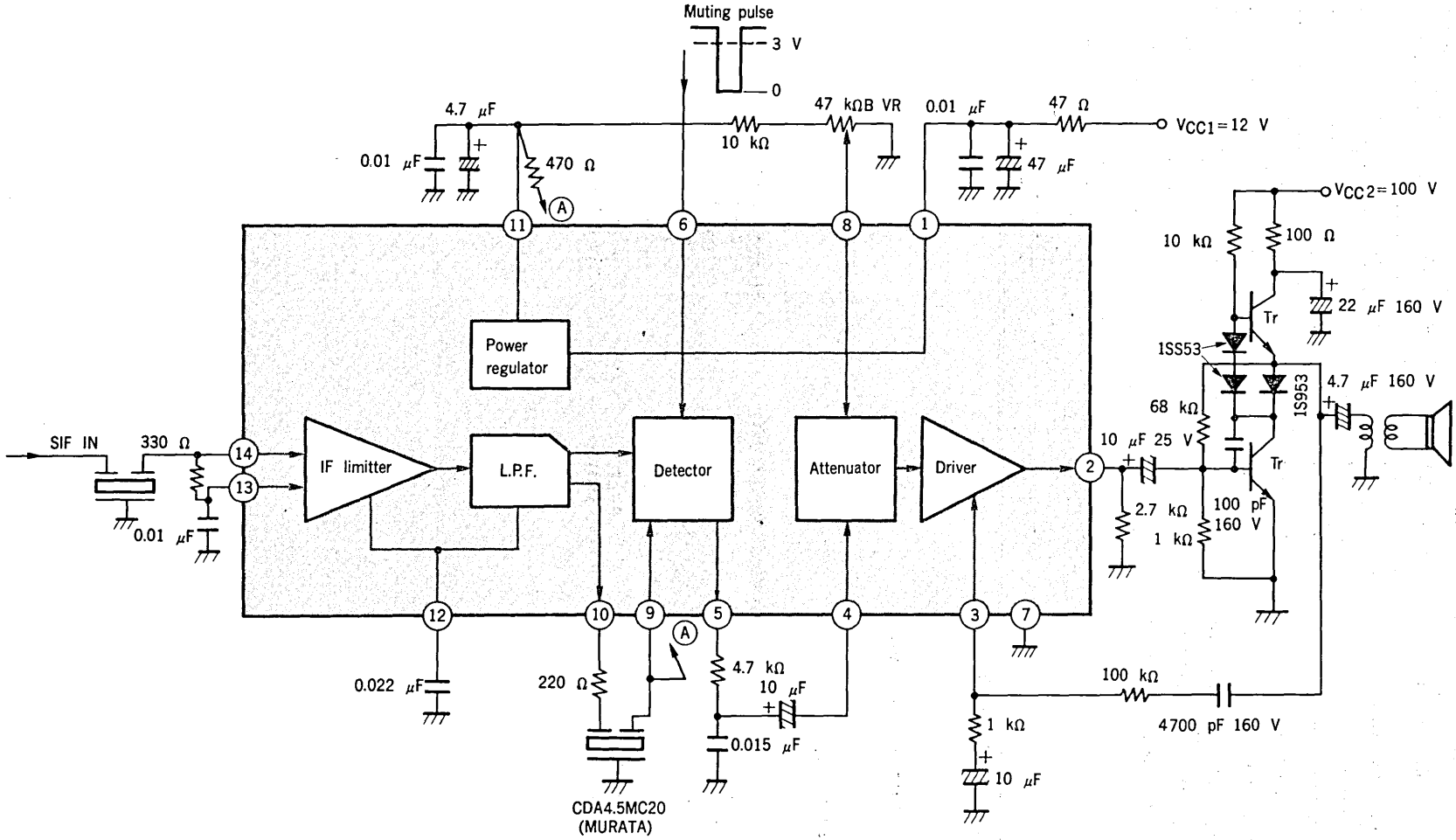
CERAMIC DISCRIMINATOR MURATA CDA4.5MC 20

SPECIFICATION OF DETECTION COIL

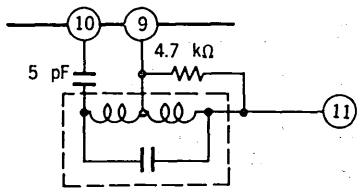


	TOKO TKAC-27071BY	TOKO TKAC-26984Y
Frequency	4.5 MHz	5.5 MHz
No loading Q	68 ± 20 %	60 ± 20 %
Turn	1–3 31¼ T	26 T
	1–2 15¼ T	13 T
	2–3 16 T	13 T
Internal C	82 pF	82 pF
Wire	0.12 ϕ OUEW	0.12 ϕ OUEW

μPC 1382C APPLICATION CIRCUIT



Example using IFT



OUTPUT POWER TRANSISTOR

3.5 W	Tr : 2SD401
2.0 W	Tr : 2SC2371
1.0 W	Tr : 2SC1941

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1391H

SOUND IF PROCESSOR FOR SOUND MULTIPLEX TV

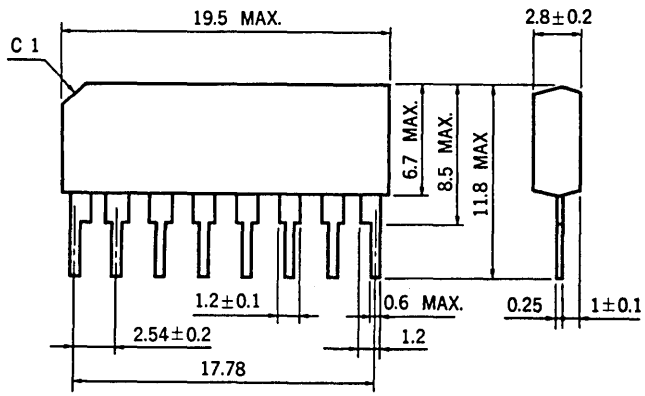
DISCRIPTION

μPC1391H is sound IF processor for sound multiplex TV. It can be operated with no adjustment, using ceramic filters externally. The quadrature detector realizes excellent low distortion. It is included in a 8 pins SIL package.

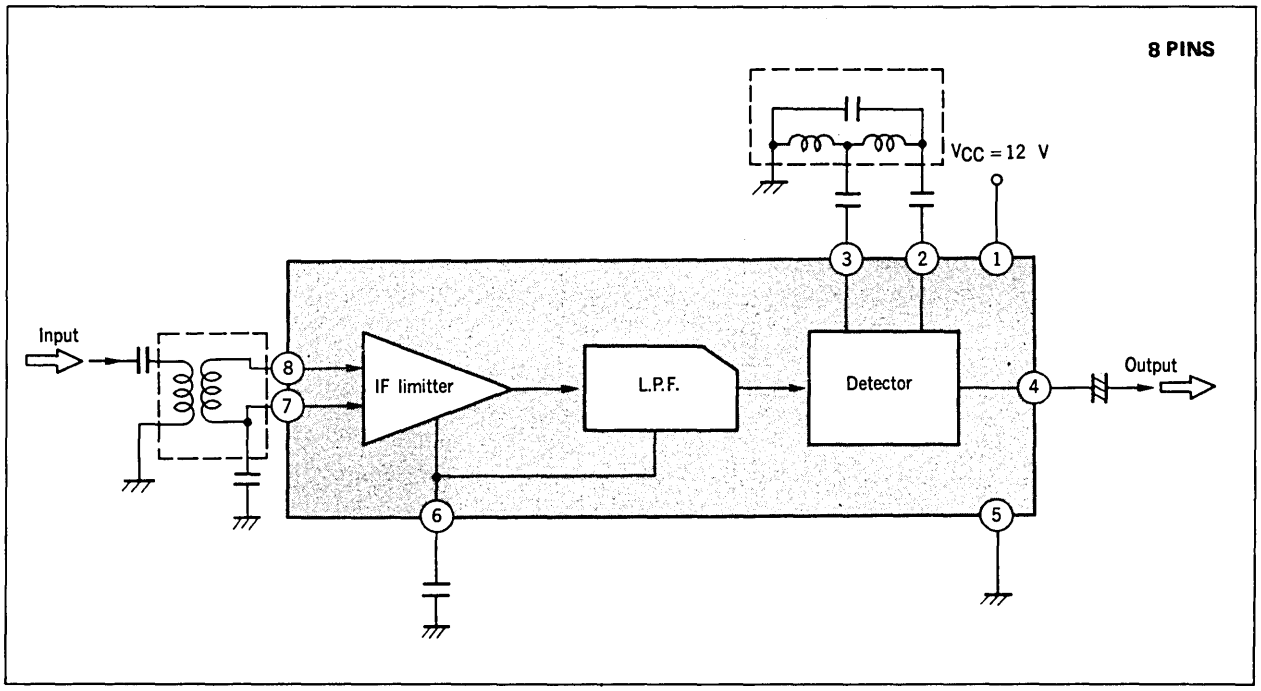
FEATURES

- Operation with ceramic filters makes TV sound circuit no adjustment completely.
- Low distortion . . . . . 0.2 %
- High sensitivity . . . . . 200 μVr.m.s.
- Excellent AMR . . . . . −55 dB (TYP.)

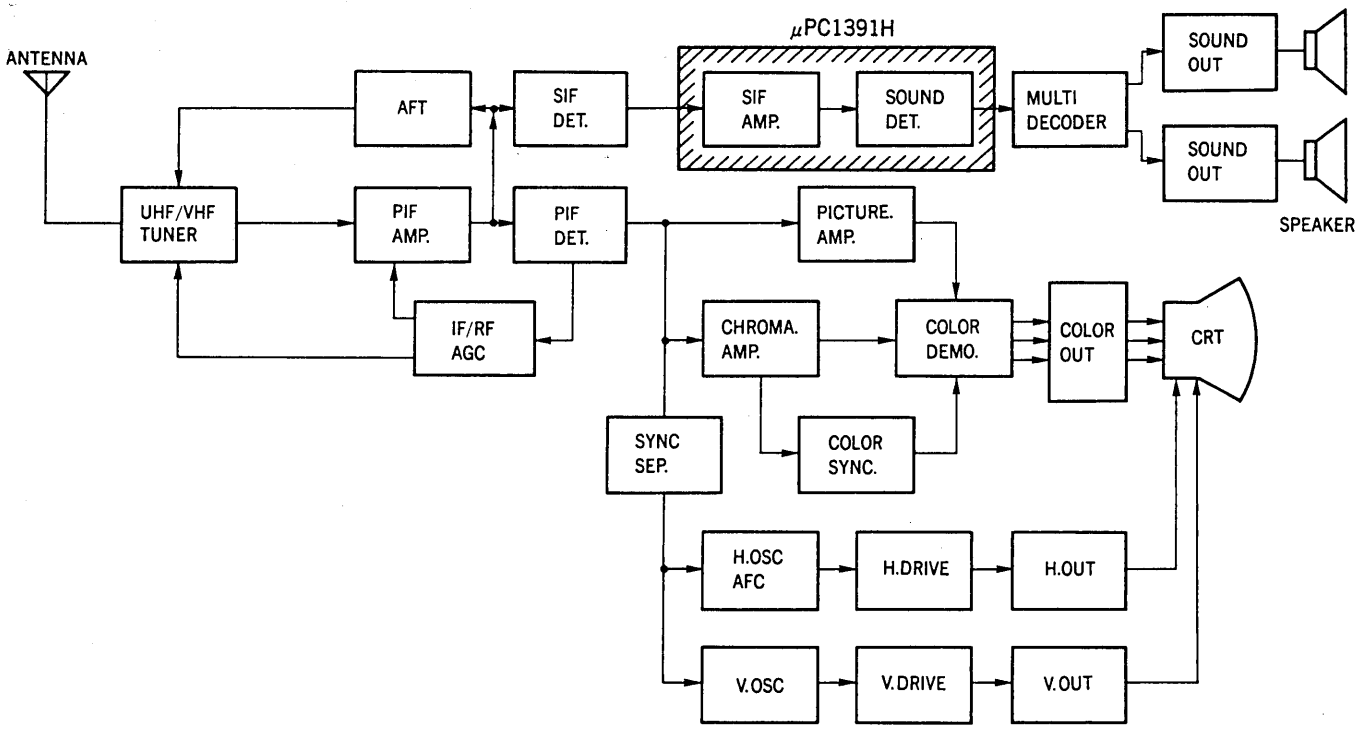
PACKAGE DIMENSIONS (Unit : mm)



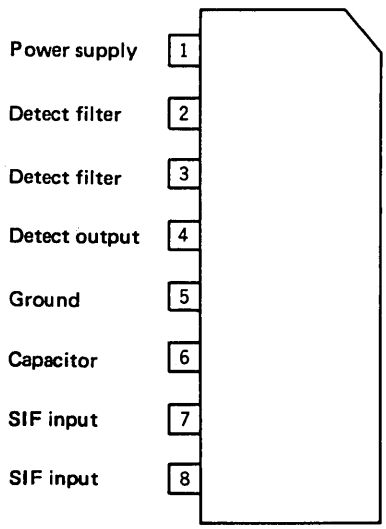
BLOCK DIAGRAM



TV BLOCK DIAGRAM



CONNECTION DIAGRAM (Top View)



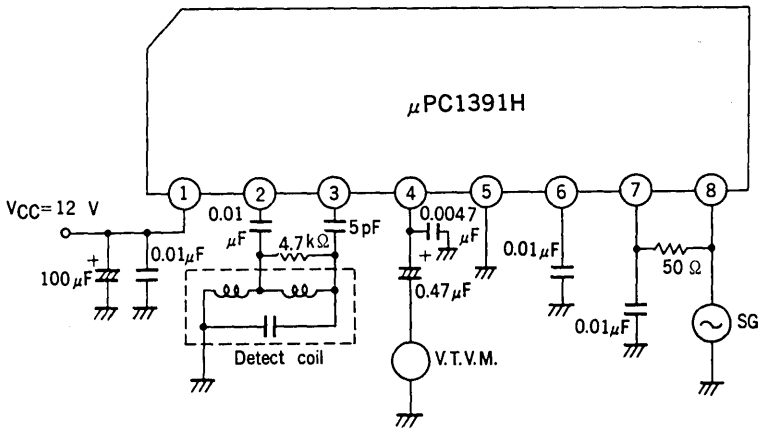
ABSOLUTE MAXIMUM RATINGS (Ta=25 °C)

Power Supply Voltage	V_{CC}	15	V
Pin 7, 8 Input Voltage	V_7, V_8	3	$V_{p\text{-}p}$
Power Dissipation	P_d	270 (Ta=75 °C)	mW
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

ELECTRICAL CHARACTERISTICS (V_{CC}=12 V, Ta=25±3 °C, f=4.5 MHz, f_M=400 Hz, AM MOD=30 %)

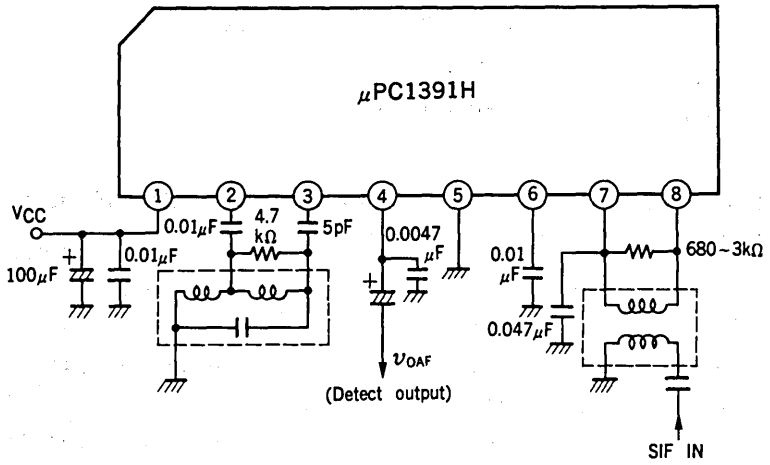
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Total Supply Current	I_{CC}	8.0	16.0	24.0	mA	Zero carrier
IF Limitting Voltage	$v_{i(lim)}$	–	180	360	μVr.m.s.	v_{OAF} (v_i=3 mVr.m.s.), −3 dB point
Detecter Output Voltage – 1	v_{OAF1}	150	200	–	mVr.m.s.	v_i=3 mVr.m.s., Δf=±25 kHz
Detecter Output Voltage – 2	v_{OAF2}	320	410	–	mVr.m.s.	v_i=3 mVr.m.s., Δf=±50 kHz
Detecter Output Distortion – 1	T.H.D.1	–	0.2	0.5	%	v_i=3 mVr.m.s., Δf=±25 kHz
Detecter Output Distortion – 2	T.H.D.2	–	0.6	1.5	%	v_i=3 mVr.m.s., Δf=±50 kHz
AM Rejection	AMR	−45	−55	–	dB	v_i=3 mVr.m.s., Δf=±25 kHz

TEST CIRCUIT

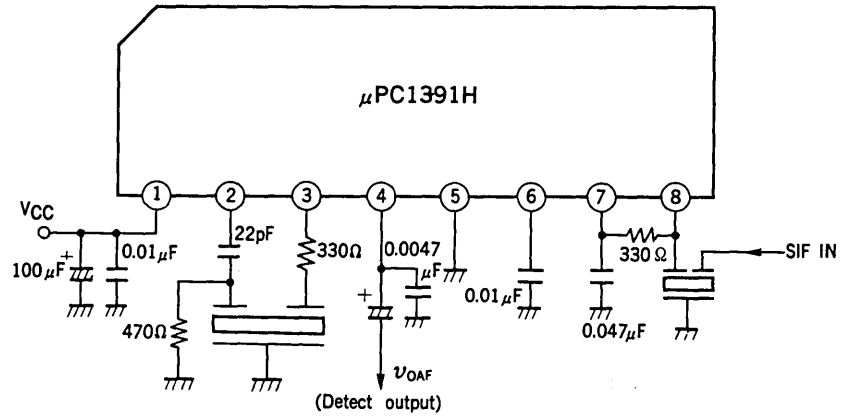


APPLICATION CIRCUIT

Using IFT

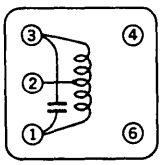


Using ceramic filter **(MURATA CDA4.5MC19)**



DETECTION COIL SPECIFICATION

TOKO 10KN TYPE TKAC-27071BY



Frequency	:	4.5 MHz
No loading Q	:	68±20 %
Turn	:	1 – 3 31¼ T
		1 – 2 15¼ T
		2 – 3 16 T
Internal C	:	82 pF
Wire	:	0.12 φ OUEW

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1352C

CHROMINANCE AND LUMINANCE PROCESSOR FOR NTSC COLOR TV

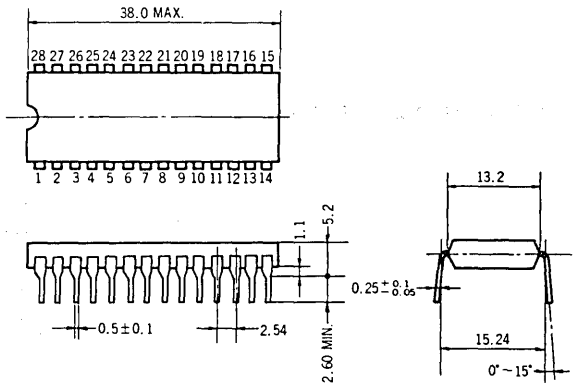
DESCRIPTION

μPC1352C is an integrated circuit for NTSC system to process both color and luminance signals of the color televisions. It is an MSI contained in a 28 pins dual in line package and provides two functions. One is the processing of color signal for the band pass amplifier, color synchronizer, demodulator circuits, and the other is the processing of luminance signal for the luminance amplifier and pedestal clamp circuits, the number of peripheral parts and controls can be minimized, and the manhours required for the assembling can be considerbly reduced.

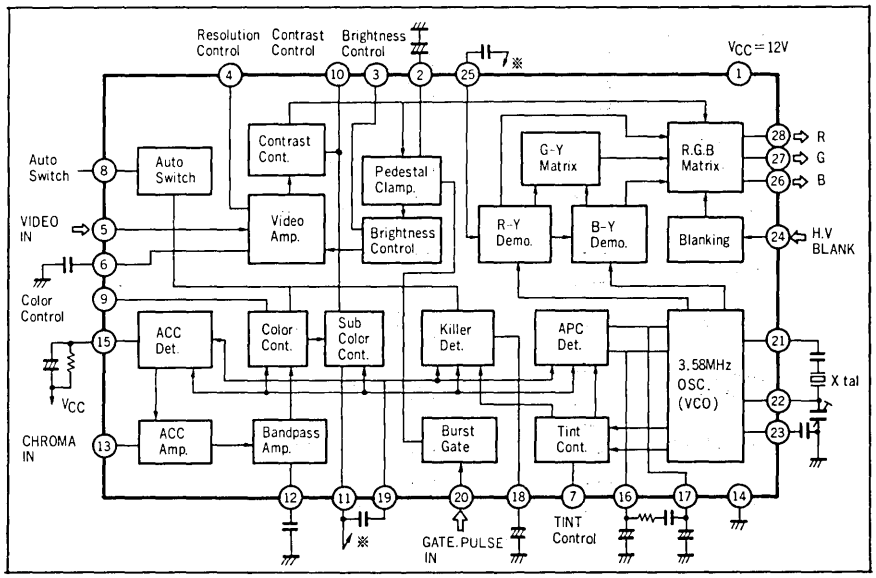
FEATURES

- It needs very few external components, and minimize the adjustments.
- DC controlled circuits make aremote controlled system easy.
- Protection diodes in every input terminals and output terminals.
- "Color killer" does not need any adjustments.
- "Contrast" control does not prevent the natural color of the picture any more, as the color saturation level changes simultaneously.
- ACC (Automatic color controller) circuit operates very smoothly with peak level detector.
- "Brightness control" terminal can be used for ABL (Automatic beam limitter) also.

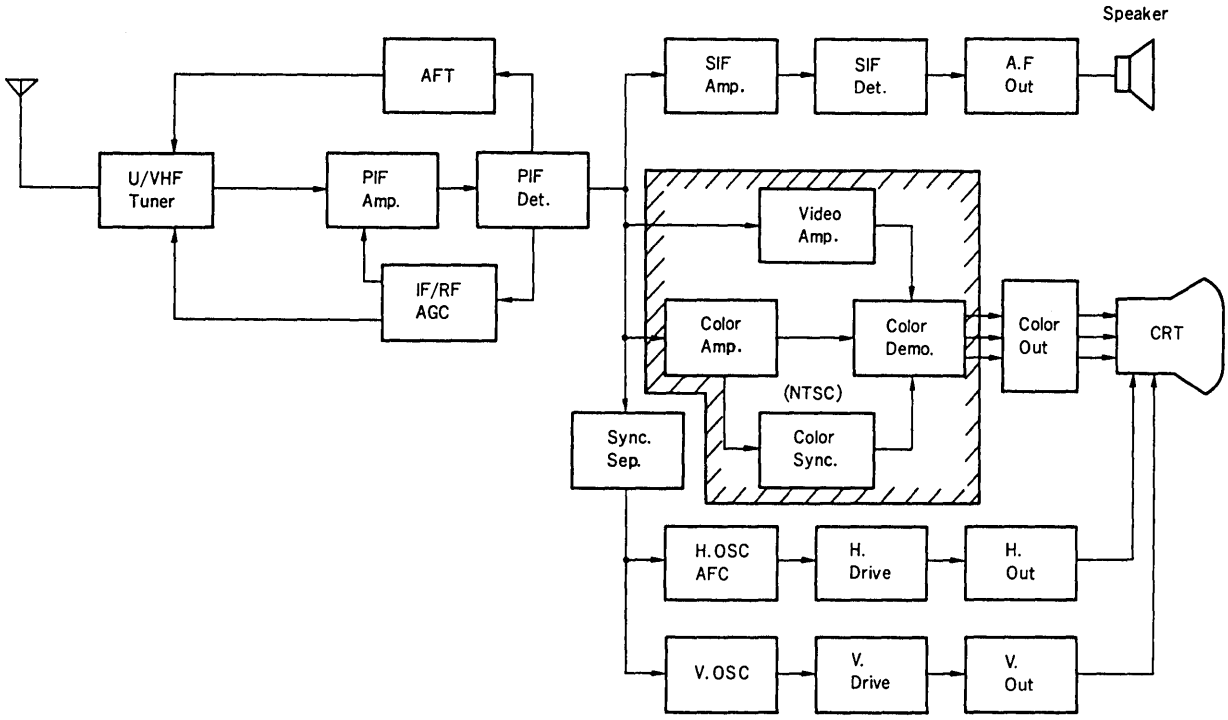
PACKAGE DIMENSIONS in millimeters



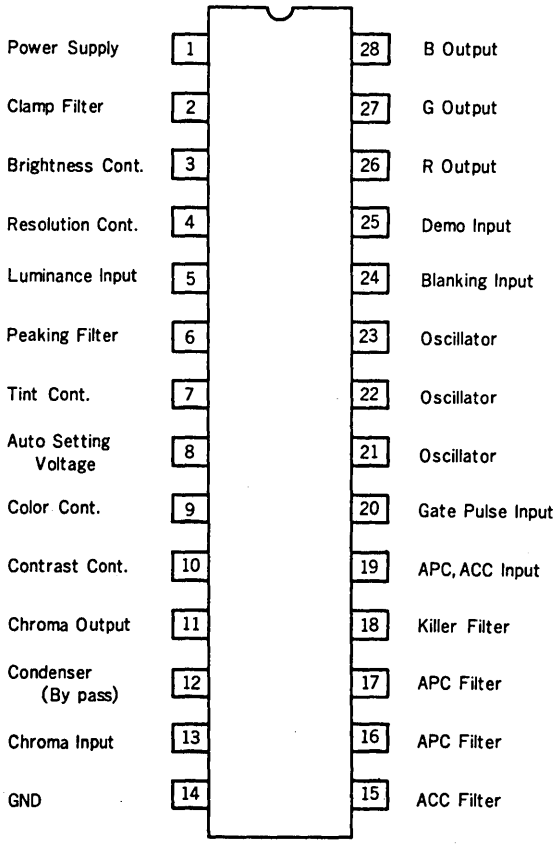
BLOCK DIAGRAM



TV BLOCK DIAGRAM



PIN CONNECTION (Top View)



THE STANDARD OPERATING CONDITIONS

Characteristic	Value	Unit
Supply Voltage	12	V
Chrominance Input Voltage (Burst signal level)	150	mVp-p
Luminance Input Voltage (Sync White Level)	1.0	Vp-p
Burst Gate Pulse Input Voltage	3.0	Vp
Blanking Pulse Input Voltage	2.5	Vp
Color saturation controlling Voltage Range	0~5.7 (at V_{CC}=12 V)	V
Tint controlling Voltage Range	0~5.7 (at V_{CC}=12 V)	V
Contrast controlling Voltage Range	0~12 (at V_{CC}=12 V)	V
Resolution controlling Voltage Range	0~12 (at V_{CC}=12 V)	V
Brightness controlling Voltage Range	8~10 (at V_{CC}=12 V)	V

Note: In case of operating in V_{CC}=14.4 V, Set the surrounding temperature Ta to be 67 °C.

ABSOLUTE MAXIMUM RATINGS (Ta=+25 °C)

Supply Voltage	V_{CC}	14.4	V
Brightness Controlling Voltage	V3	14.4	V
Resolution Controlling Voltage	V4	14.4	V
Contrast Controlling Voltage	V10	14.4	V
Tint Controlling Voltage	V7	14.4	V
Color Controlling Voltage	V9	14.4	V
Auto Controlling Voltage	V8	14.4	V
Luminance Input Signal Voltage	V5	+5	V
Chrominance Signal Input Voltage	V13	+2.5	V
Demodulator Input Signal Voltage	V25	+5	V
R.G.B Output Current	I26,I27,I28	−40	mA
Gate Pulse Input Voltage	V20	+5	V
Gate Pulse Output Current	I20	−10	mA
Blanking Pulse Input Voltage	V24	±6	V
Power Dissipation	Pd1 (Ta=25 °C)	1.2	W
Power Dissipation	Pd2 (Ta=70 °C)	750	mW
Operating Temperature	T_{opt}	−20~+70	°C
Storage Temperature	T_{stg}	−40~+125	°C

Test Conditions (V_{CC}=12 V)

Characteristic	MIN.	TYP.	MAX.
Color saturation controlling terminal 9	0 V	V8/2 V	V8 V
Tint controlling terminal 7	0 V	V8/2 V	V8 V
Contrast controlling terminal 10	0 V	V_{CC} x 0.78 V	V_{CC} V
Resolution controlling terminal 4	0 V	—	V_{CC} V

ELECTRICAL CHARACTERISTICS (Ta=25 °C unless otherwise noted V_{CC}=12 V)

Color control is manual state and tint is center for the items not specifically specified

No.	Characteristic	Symbol	Test Ckt.	Test Condition	MIN.	TYP.	MAX.	Unit
1	Supply Current	I_{CC}	1		32	43	54	mA
2	Burst Output Voltage	e_b	3	Rainbow color bar signal input 150 mVp-p, Color auto center, Contrast max.	0.5	0.7	0.9	Vp-p
3	ACC Range 1	ACC1	3	Rainbow color bar signal input 300 mVp-p, Burst Output Voltage/e_b	0.9	1.0	1.1	times
4	ACC Range 2	ACC2	3	Rainbow color bar signal input 15 mVp-p, Burst Output Voltage/e_b	0.6	0.8	1.0	times
5	Chroma Output Voltage 1	e_{c1}	3	Rainbow color bar signal input 150 mVp-p, Color min, Contrast max.	0.5	0.7	0.9	Vp-p
6	Chroma Output Voltage 2	e_{c2}	3	Rainbow color bar signal input 150 mVp-p, Color min, Contrast max.	–	–	5	mVp-p
7	Chroma Output Voltage 3	e_{c3}	3	Rainbow color bar signal input 150 mVp-p, Color center, Contrast max.	120	190	260	mVp-p
8	Chroma Output Voltage 4	e_{c4}	3	Rainbow color bar signal input 150 mVp-p, Color auto center, Contrast max.	130	190	260	mVp-p
9	Variable Range of Chroma Output Voltage at auto	Δe_{ca}	3	Rainbow color bar signal input 150 mVp-p, Color auto max min, Contrast max.	+25 –25	+35 –35	+45 –45	%
10	Free running Frequency	f_o	2	No input signal to Terminal 19 Be trimed 3.579545 MHz by using a trimer capasitor for standard sample, Deviation from f; 3.579545 MHz	–	–	±150	Hz
11	Oscillator controlling sensitivity	β	2	Burst signal input 0.7 Vp-p, Converted from V16–17 in case of 100 Hz burst frequency variation	1.0	1.5	2.0	Hz/mV
12	Phase detector sensitivity	μ	2	Burst signal input 0.7 Vp-p, Converted from phase error and V16–17 in case of 100 Hz burst frequency variation	25	45	65	mV/ degree
13	Phase error	$\Delta\phi$	2	Burst signal input 0.7 Vp-p, Phase error to 100 Hz of burst frequency variation	–	1.5	3.0	degree /100 Hz
14	A.P.C. pull-in frequency range	f_p	2	Burst signal input 0.7 Vp-p, Mesured by changing the burst frequency	±350	±500	–	Hz
15	Variable Range of Tint	$\Delta\theta 1$	2	Burst signal input 0.7 Vp-p, Tint; max min, manual, Tint center, Range from O as a standard	+37 –37	+45 –45	+53 –53	degree
16	Variable Range of Tint at auto	$\Delta\theta 2$	2	Burst signal input 0.7 Vp-p, Tint; max min, auto Tint center, Range from O as a standard	12 –12	+17 –17	+22 –22	degree

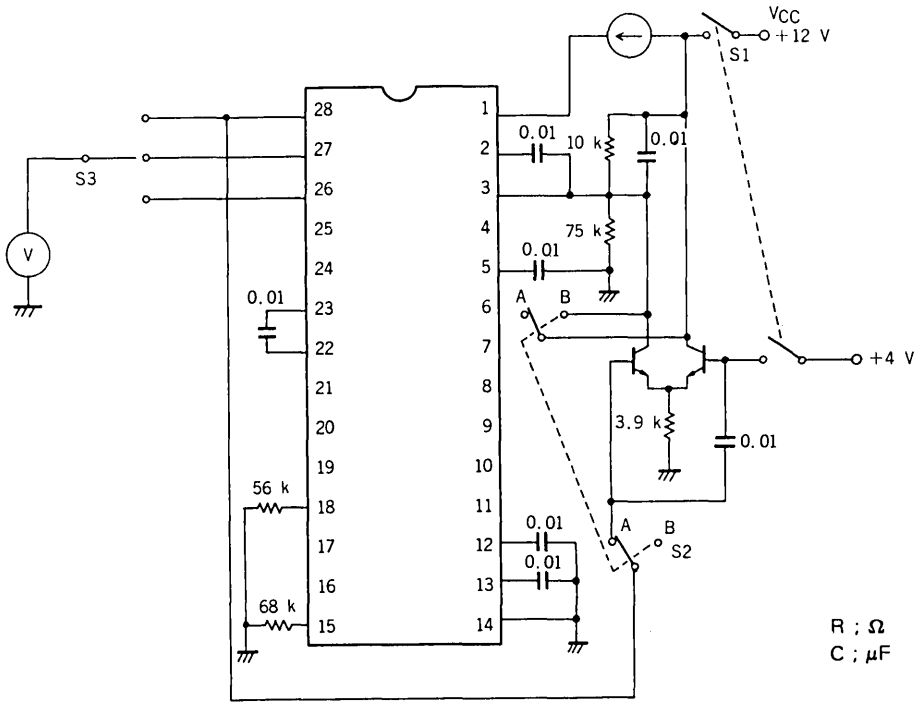
(continued on next page)

No.	Characteristic	Symbol	Test Ckt.	Test Condition	MIN.	TYP.	MAX.	Unit
17	B-Y Output Voltage	e_{o1}	3	Dem. input 0.2 Vp-p, f=3.59 MHz, Bright VR was set to be V26=3.5 V(DC) No blanking input	1.5	2.0	2.5	Vp-p
18	Ratio of R-Y to B-Y	R/B	3	Dem. input 0.2 Vp-p, f=3.59 MHz, R Output Voltage/e_{o1} Bright VR was set to be V26=3.5 (DC) No blanking input	0.86	0.94	1.04	times
19	Ratio of G-Y to B-Y	G/B	3	Dem. input 0.2 Vp-p, f=3.59 MHz, G Output Voltage/e_{o1} Bright VR was set to be V26=3.5 V(DC) No blanking input	0.25	0.30	0.35	times
20	Relative Output phase G-Y to R-Y	∠R	3	Dem. input 0.2 Vp-p, f=3.59 MHz, B=O degree, phase difference Bright VR was set to be V26=3.5 V(DC) No blanking input	94	97.5	102	degree
21	Relative Output phase G-Y to B-Y	∠G	3	Dem. input 0.2 Vp-p, f=3.59 MHz, B=O degree, phase difference Bright VR was set to be V26=3.5 V(DC) No blanking input	228	235	242	degree
22	Maximum Color difference Output Voltage	e_{o2}	3	Dem. input 1.2 Vp-p, f=3.59 MHz, Bright VR was set to be V26=3.5 V(DC) No blanking input	4.8	5.7	—	Vp-p
23	Residual Carrier	e_{car}	3	No signal input, Output; 3.58 MHz each, Carrier leak component, Bright VR was set to be V26=3.5 V(DC) No blanking input	—	—	100	mVp-p
24	Demodulation frequency characteristic	e_{of}	3	Attenuation factor of demodulation output at f=500 kHz, Dem. input 0.2 Vp-p, f=3.08 MHz, Assuming the output at f=10 kHz is 0 dB	−1.5	−0.9	−0.4	dB
25	Overall Color difference Output Voltage	e_{o3}	3	Rainbow color bar signal input 150 mVp-p, Color auto center, Contrast max, in R output	1.0	1.7	2.4	Vp-p
26	Overall Color difference Output Variable Range by Contrast	Δe_{oc}	3	Rainbow color bar signal input 150 mVp-p, Color auto center, Contrast max/min, in R output	3.4	3.85	4.3	Vp-p
27	Color killer talerance	e_k	3	Burst input Voltage at terminal 13 150 mVp-p=0 dB, Attenuation value in operating the killer	−27	−32	−40	dB
28	Luminance Gain	Av1	3	R,G,B Output each, Studio color bar input 1 Vp-p in white level, Contrast max, Resolution min, Pedestal of terminal 26 is 2 V, Bright VR was set	4.5	5.0	5.5	times
29	Luminance Gain Variable Range by Contrast	Δe_{vc}	3	Studio color bar input 1 Vp-p in white level, Contrast max/min, Resolution min, in B output	4.0	4.5	5.0	times

(continued on next page)

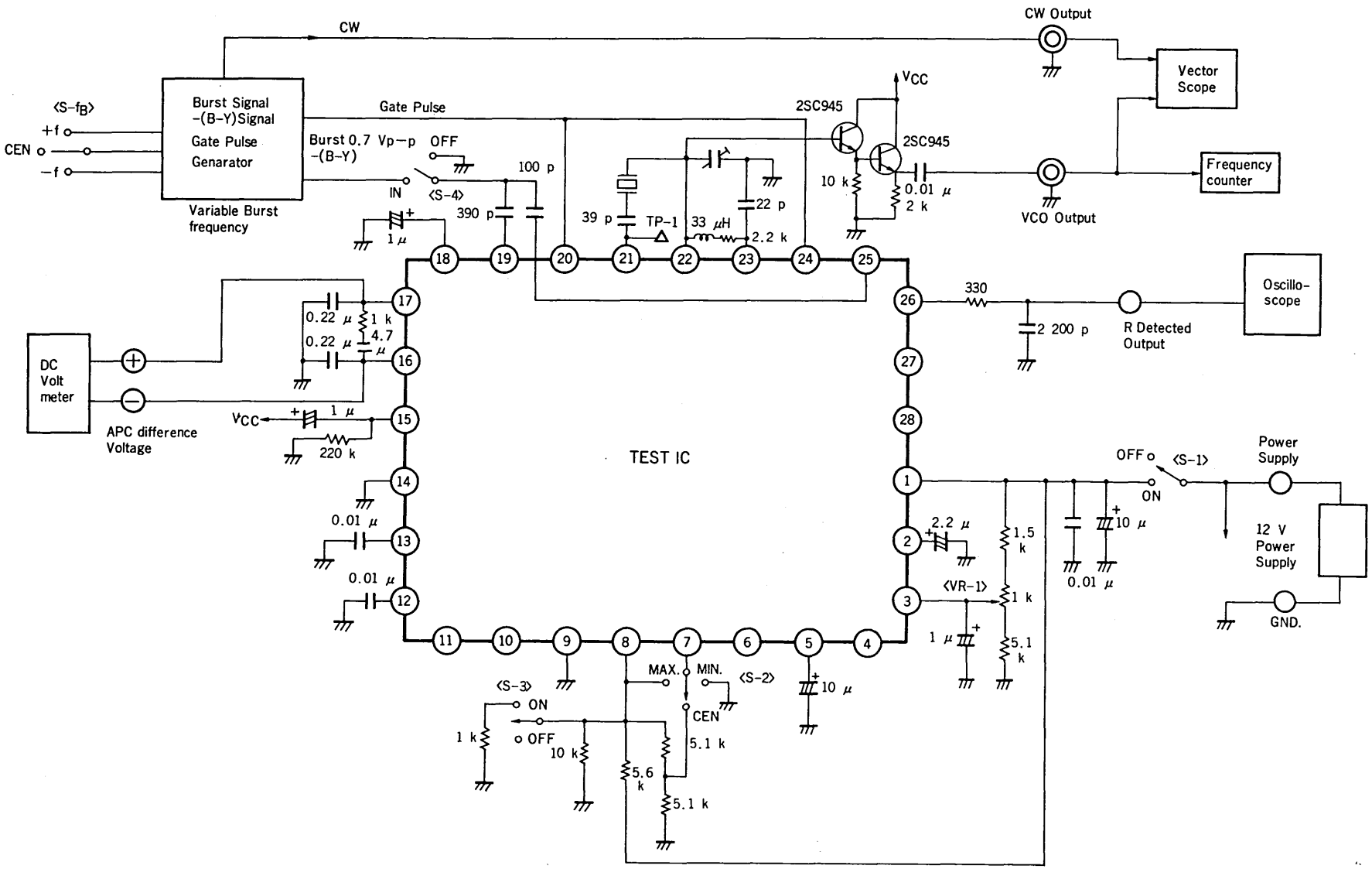
No.	Characteristic	Symbol	Test Ckt.	Test Condition	MIN.	TYP.	MAX.	Unit
30	Luminance Amp. frequency characteristic	f_V	3	Sine wave signal input 0.1 Vr.m.s. Input frequency at Av1=−6 dB Resolution min, in B output, Bright VR was set to be V26=3.5 V(DC) No blanking input, 0 dB=16 kHz Output	5	6	–	MHz
31	Resolution Variation Range	Δf_{VP}	3	Sine wave signal 0.1 Vr.m.s., f=2 MHz Contrast max, Resolution min~max, in B Output max/min	5.0	7.0	9.0	dB
32	DC Restored	T_{DC}	3	Stair Step signal input 1 Vp-p, APL 10~90 % in B Output	65	75	85	%
33	Brightness controlling sensitivity	BR	3	$\Delta E_O/\Delta V_3$, E_O=2 V~5 V, R,G,B Output each	4.0	4.5	5.0	–
34	Maximum R,G,B Output Voltage	E_{OM}	1	R.G.B Output Voltage each at V3=12 V	7.0	–	–	V
35	Differential Gain	D.G.	3	Stair Step signal input 1 Vp-p, f=3.58 MHz, APL=50 %, Contrast max, Resolution min, Pedestal of terminal 26 is 2 V, Bright VR was set	–	–	5.0	%
36	Queiscent Output Voltage	E_O	3	R,G,B Output each, Bright VR was set to be V3=9 V, No Luminance signal input, Contrast max, VCO is operating, Blanking	2.5	3.5	4.5	V
37	E_O Supply Voltage Coefficient	E_{O-V}	3	V_{CC}=12 V ±20 %, V26=3.5 V (V_{CC}=12 V), R, G, B Output each Blanking	0.2	0.25	0.3	V/V
38	E_O Temperature Cofficient	ΔE_{O-t}	3	Ta=−20~+70 °C, V26=3.5 V (Ta=25 °C) R,G,B Output each	−4.0	−2.0	0	mV/°C
39	Difference Output Voltage	ΔE_{R-G} ΔE_{G-B} ΔE_{B-R}	3	V26=3.5 V VCO is operating, R,G,B Output each, No blanking input	–	0	300	mV

Test Circuit 1



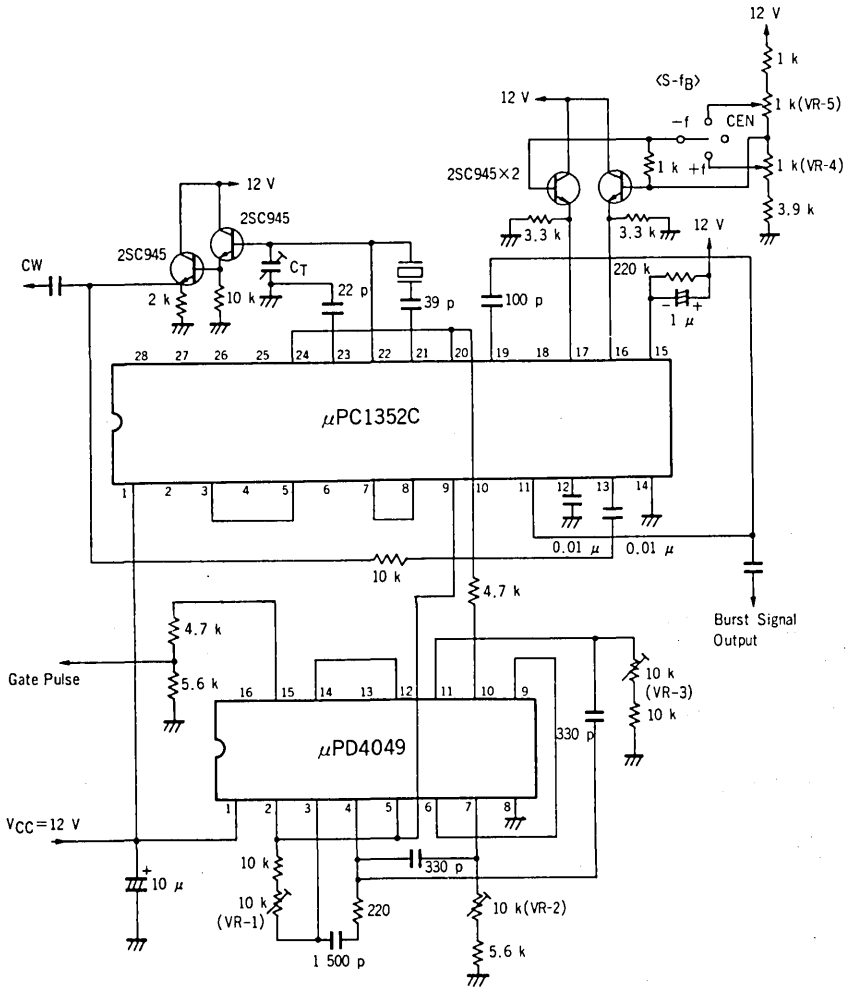
Supply Current	I_{CC}	S1 ; ON	S2 ; Side A	
Maximum R,G,B Output Voltage	E_{oM}	S1 ; ON	S2 ; Side B	S3 ; Each

Test Circuit 2



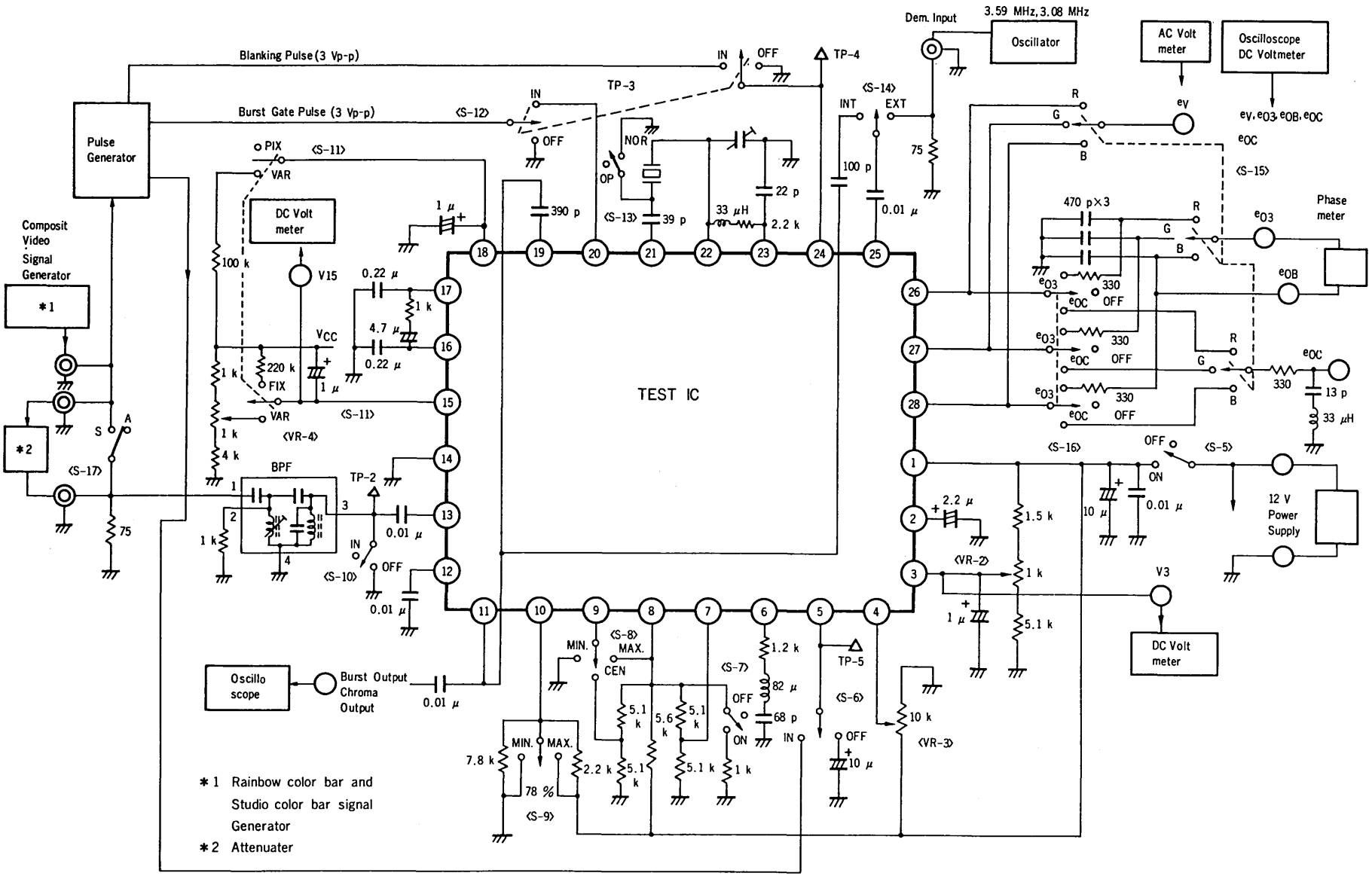
Burst Signal
–(B-Y) Signal
Gate Pulse Generator

Test Circuit 2

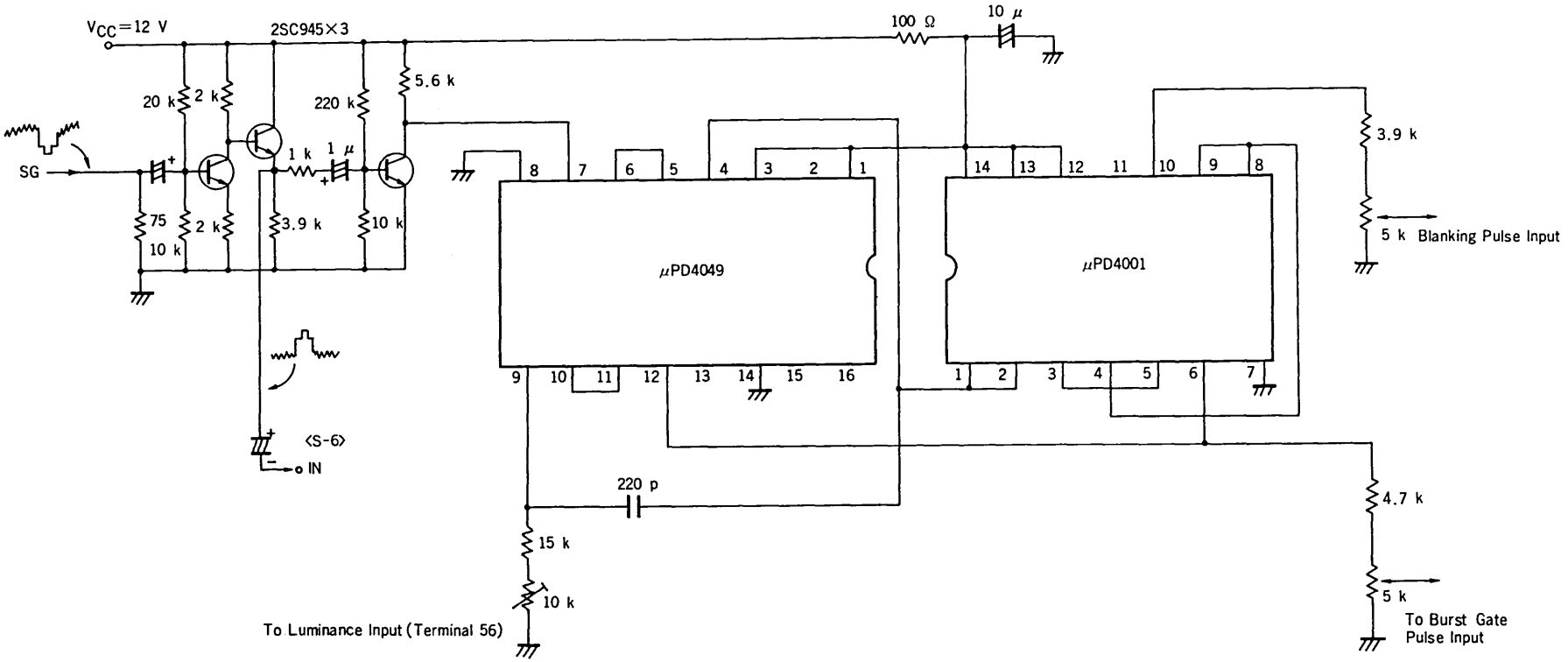


VR-1 Set to f_H = 15.75 kHz.
VR-2 Set to Burst width (10 cycle)
VR-3 Set to Gate Pulse width = 3.5 μs.
VR-4 +f
VR-5 –f Be trimed f_O = 3579545 Hz by C_T at the VR are center.

Test Circuit 3



Pulse Generator Circuit (Test Circuit 3)



Characteristic	Symbol	Test CKt	1	2	3	4	f_B	5	6	7	8	9	10	11	12	13	14	15	16	17	1	2	3	4	Measuring Apparatus
			Power Supply	Tint	Auto	Burst -(B-Y) Input	Burst frq	Power Supply	Lumi-nance Input	Auto	Color	Cont-rast	Chro-ma Input	ACC	Pulse Input	VCO	Demo Input	R G B	Demo Output	Attenuator	Bright-ness	Bright-ness	Resolu-tion	ACC Level	
Burst Output Voltage	e_b	3						OFF ↓ ON	OFF	ON	CEN	MAX	IN	FIX	IN	OP	INT	–	e_{o3}	A TP-2 150 mVp-p		–	MIN	–	Osciroscope Burst signal
ACC Range 1	ACC1	3						OFF ↓ ON	OFF	ON	CEN	MAX	IN	FIX	IN	OP	INT	–	e_{o3}	A TP-2 300 mVp-p		–	MIN	–	Osciroscope Burst signal
ACC Range 2	ACC2	3						OFF ↓ ON	OFF	ON	CEN	MAX	IN	FIX	IN	OP	INT	–	e_{o3}	A TP-2 150 mVp-p		–	MIN	–	Osciroscope Burst signal
Chroma Output Voltage	e_{c1}	3						OFF ↓ ON	OFF	OFF	MAX	MAX	IN	FIX	IN	OP	INT	–	e_{03}	A TP-2 150 mVp-p		–	MIN	–	Osciroscope Chroma signal
Chroma Output Voltage	e_{c2}	3						OFF ↓ ON	OFF	OFF	MIN	MAX	IN	FIX	IN	OP	INT	–	e_{o3}	A TP-2 150 mVp-p		–	MIN	–	Osciroscope Chroma signal
Chroma Output Voltage	e_{c3}	3						OFF ↓ ON	OFF	OFF	CEN	MAX	IN	FIX	IN	OP	INT	–	e_{o3}	A TP-2 150 mVp-p		–	MIN	–	Osciroscope Chroma signal
Chroma Output Voltage	e_{c4}	3						OFF ↓ ON	OFF	ON	CEN	MAX	IN	FIX	IN	OP	INT	–	e_{o3}	A TP-2 150 mVp-p		–	MIN	–	Osciroscope Chroma signal
Variable Range of Chroma Output Voltage at auto	Δe_{ca}	3						OFF ↓ ON	OFF	ON	MAX ↓ MIN	MAX	IN	FIX	IN	OP	INT	–	e_{o3}	A TP-2 150 mVp-p		–	MIN	–	Osciroscope Variation of Chroma signal
Free running Frequency	f_o	2	OFF ↓ ON	CEN	ON	OFF	–														–				Frequency Counter
Oscillator controlling sensitivity	β	2	OFF ↓ ON	CEN	ON	IN	+f CEN −f														–				D.C. Voltage Meter
Phase Det. sensitivity	μ	2	OFF ↓ ON	CEN	ON	IN	+f CEN −f														–				Vector Scope D.C. Vol. Mete Difference APC Voltage
Phase error	$\Delta\phi$	2	OFF ↓ ON	CEN	ON	IN	+f CEN −f														–				Vector Scope
A.P.C. pull-in Freq. range	f_p	2	OFF ↓ ON	CEN	ON	IN	+f CEN −f														–				Oscilloscope
Variable Range of Tint	$\Delta\theta 1$	2	OFF ↓ ON	MAX ↓ MIN	OFF	IN	CEN														–				Vector Scope
Variable Range of Tint at auto	$\Delta\theta 2$	2	OFF ↓ ON	MAX ↓ MIN	OFF	IN	CEN														–				Vector Scope
B-Y Output Voltage	e_{o1}	3						OFF ↓ ON	OFF	–	–	–	OFF	FIX	OFF	OP	EXT 0.2 Vp-p f=3.59	B	e_{o3}	–		V26= 3.5 V	MIN	–	Oscilloscope Demo. Output Voltage B

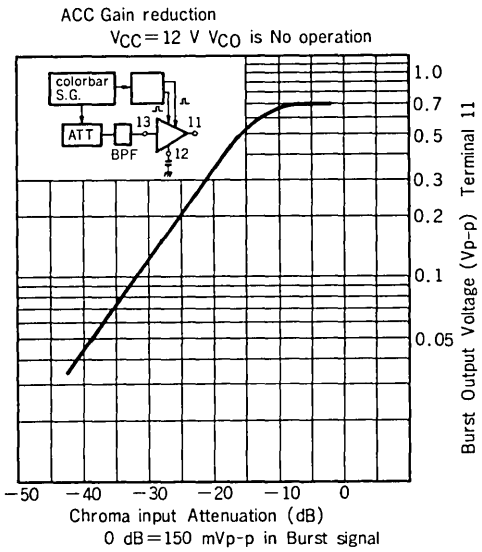
(continued on next page)

Characteristic	Symbol	Test Ckt	1 Power Supply	2 Tint	3 Auto	4 Burst -(B-Y) Input	f_B Burst frq.	5 Power Supply	6 Luminance Input	7 Auto	8 Color	9 Contrast	10 Chroma Input	11 ACC	12 Pulse Input	13 VCO	14 Demo Input	15 R G B	16 Demo Output	17 Attenuater	1 Brightness	2 Brightness	3 Resolution	4 ACC Level	Measuring Apparatus
Ratio of R-Y to B-Y	R/B	3						OFF ↓ ON	OFF	–	–	–	OFF	FIX	OFF	OP	EXT 0.2 Vp-p f=3.59	B R	e_{o3}	–		V26= 3.5 V	MIN	–	Oscilloscope Demo. Output Voltage R B
Ratio of G-Y to B-Y	G/B	3						OFF ↓ ON	OFF	–	–	–	OFF	FIX	OFF	OP	EXT 0.2 Vp-p f=3.59	G I	e_{o3}	–		V26= 3.5 V	MIN	–	Oscilloscope Demo. Output Voltage G B
Relative Output phase B-Y to R-Y	∠R	3						OFF ↓ ON	OFF	–	–	–	OFF	FIX	OFF	OP	EXT 0.2 Vp-p f=3.59	B R	e_{o3}	–		V26= 3.5 V	MIN	–	Phase Meter Relative phase R B
Relative Output phase G-Y to B-Y	∠G	3						OFF ↓ ON	OFF	–	–	–	OFF	FIX	OFF	OP	EXT 0.2 Vp-p f=3.59	B G	e_{o3}	–		V26= 3.5 V	MIN	–	Phase. Meter Relative phase B G
Maximum Detected Output Voltage	e_{o2}	3						OFF ↓ ON	OFF	–	–	–	OFF	FIX	OFF	OP	EXT 1.2 Vp-p f=3.59	B R	e_{o3}	–		V26= 3.5 V	MIN	–	Oscilloscope Demo. Output Voltage B R
Residual Carrier	e_{car}	3						OFF ↓ ON	OFF	–	–	–	OFF	FIX	OFF	OP	EXT No.	R G B	e_{oc}	–		V26= 3.5 V	MIN	–	Oscilloscope Output 3.58M Carrior
Demodulation frequency characteristic	e_{of}	3						OFF ↓ ON	OFF	–	–	–	OFF	FIX	OFF	OP	EXT 0.2 Vp-p f=3.08	R G B	OFF	–		V26= 3.5 V	MIN	–	A.C. Voltage Meter
Overall Detected Output Vol.	e_{o3}	3						OFF ↓ ON	OFF	ON	CEN	MAX	IN	FIX	IN	OP	INT	R	e_{o3}	A TP-2 150 mVp-p		V26= 3.5 V	MIN	–	Oscilloscope Demo. Output Voltage R
Overall Detected Output Variable Range by Cont. controlling	Δe_{oc}	3						OFF ↓ ON	OFF	ON	CEN	MAX ↓ MIN	IN	FIX	IN	OP	INT	R	e_{o3}	A TP-2 150 mVp-p		V26= 3.5 V	MIN	–	Oscilloscope Demo. Output Voltage R
Collor killer talerance	e_k	3						OFF ↓ ON	OFF	–	–	–	IN	FIX	IN	OP	INT	R	e_{o3}	A TP-2 150 mVp-p		V26= 3.5 V	MIN	–	Oscilloscope Demo. Output Voltage R
Luminance Gain 1	AV1	3						OFF ↓ ON	IN Studio Color Bar White 1 Vp-p			MAX	OFF	VAR	IN	NOP	EXT NO.	R G B	OFF	–		Terminal 26 Pedestal 2 V	MIN	V15= 8 V	Oscilloscope ev
Luminance Gain Variable Range by Contrast cont.	Δe_{ve}	3						OFF ↓ ON	IN Studio Color Bar White 1 Vp-p			MAX	OFF	VAR	IN	NOP	EXT NO.	B	OFF	–		Terminal 26 Pedestal 2 V	MIN	V15= 8 V	Oscilloscope ev
Luminance Amp. Frequency characteristic	f_v	3						OFF ↓ ON	IN Sine Wave 0.1 Vr.m.s.			MAX	OFF	VAR	OFF	NOP	EXT NO.	B	OFF	–		V26= 3.5 V	MIN	V15= 8 V	A.C. Voltage Meter 0 dB= 16 kHz ev
Resolution Variation Range	Δf_{vp}	3						OFF ↓ ON	IN Sine Wave 2M 0.1 Vr.m.s.			MAX	OFF	VAR	OFF	NOP	EXT NO.	B	OFF	–		V26= 3.5 V	MIN MAX	V15= 8 V	A.C. Voltage Meter ev

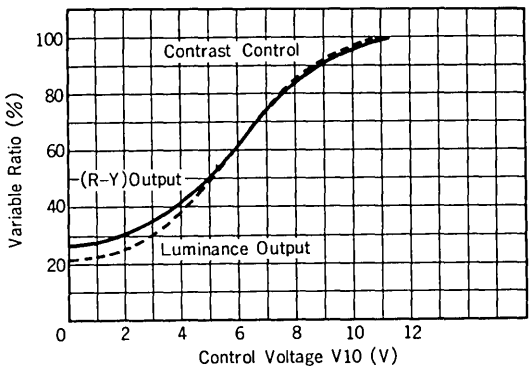
(continued on next page)

Characteristic	Symbol	Test Ckt	1 Power Supply	2 Tint	3 Auto	4 Burst -(B-Y) Input	f_B Burst frq	5 Power Supply	6 Lumi-nance Input	7 Auto	8 Color	9 Cont-rast	10 Chro-ma Input	11 ACC	12 Pulse Input	13 VCO	14 Demo Input	15 RGB	16 Demo Output	17 Attenuater	1 Bright-ness	2 Bright-ness	3 Resolu-tion	4 ACC Level	Measuring Apparatus
D.C. Transfer	T_{DC}	3						OFF ↓ ON	IN Stair step 1 Vp-p APL 90%			MAX	OFF	VAR	IN	NOP	EXT NO.	B	OFF	–		Termi-nal 26 Pedestal 2 V	MIN	V15= 8 V	Oscilloscope ev
Brightness Controlling Sensitivity	BR	3						OFF ↓ ON	OFF	–	–	MAX	OFF	VAR	IN	OP	EXT NO.	RGB	e_{o3}	–		e_{o3} D.C. 2–5 V	MIN	V15= 8 V	V3 e_{o3} D.C. Voltage Meter
Differential Gain	D.G.	3						OFF ↓ ON	IN Stair step APL 50%			MAX	OFF	VAR	IN	NOP	EXT NO.	B	OFF	–		Termi-nal 26 Pedestal 2 V	MIN	V15= 8 V	Vector Scope ev
Queiscent Output Voltage	E_o	3						OFF ↓ ON	OFF	–	–	MAX	OFF	FIX	IN	OP	EXT NO.	RGB	e_{o3}	–		V3= 9 V	MIN	–	D.C. Voltage Meter
E_o Supply Vol. Coeffisient	$E_{o\text{-}v}$	3						OFF ↓ ON	OFF	–	–	–	OFF	FIX	IN	OP	EXT NO.	RGB	e_{o3}	–		V3= 9 V	MIN	–	D.C. Voltage Meter
E_o Temperature Coefficient	$E_{o\text{-}t}$	3						OFF ↓ ON	OFF	–	–	–	OFF	FIX	IN	OP	EXT NO.	RGB	e_{o3}	–		V3= 9 V	MIN	–	D.C. Voltage Meter
Difference Output Voltage	$E_{R\text{-}G}$ $E_{G\text{-}B}$ $E_{B\text{-}R}$	3						OFF ↓ ON	OFF	–	–	–	OFF	FIX	OFF	OP	EXT NO.	RGB	e_{o3}	–		V26= 3.5 V (V_{CC}= 12 V)	MIN	–	D.C. Voltage Meter

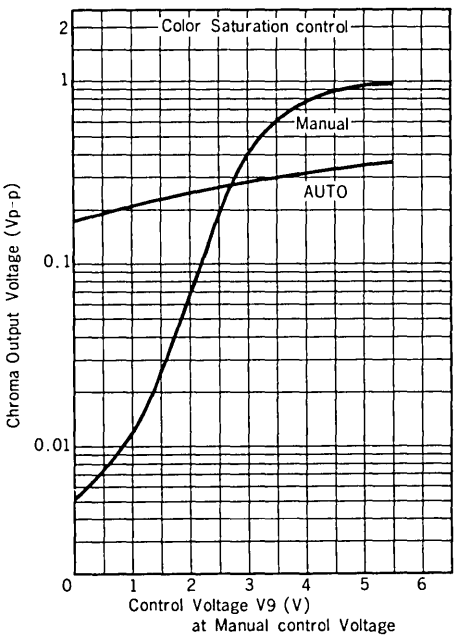
ACC Characteristic



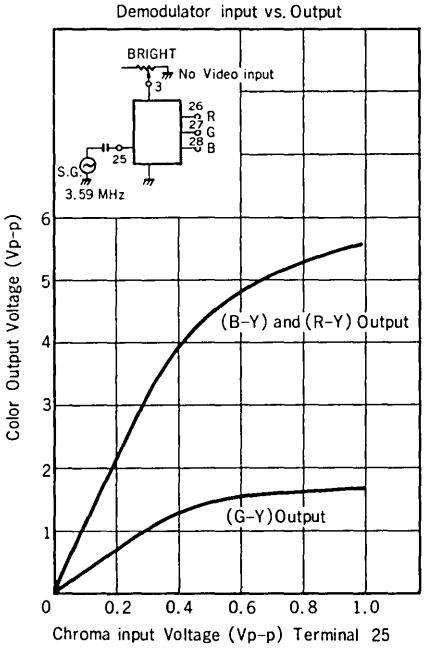
Contrast Control Characteristic



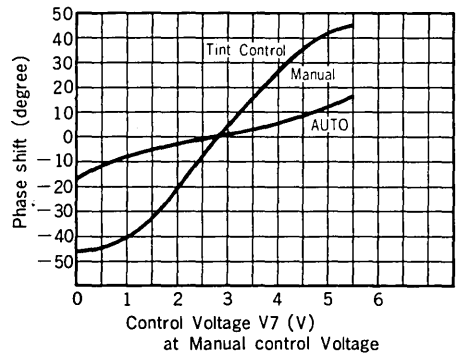
Color Control Characteristic



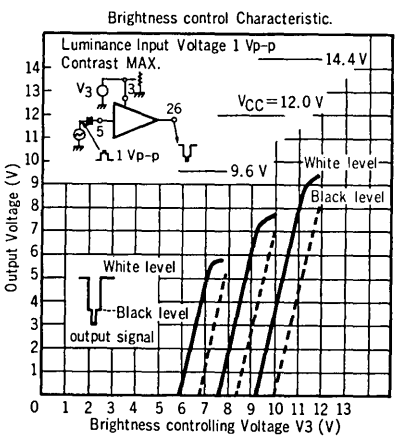
Brightness Control Characteristic



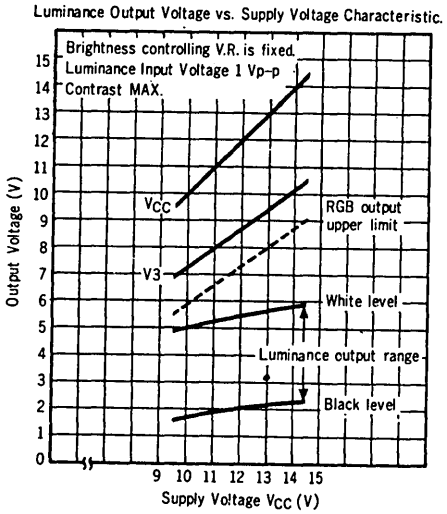
Tint Control Characteristic



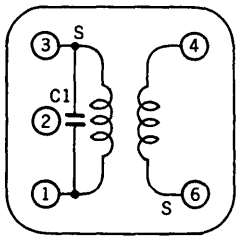
Demodulator Input-Output



R.G.B. Output Stage Dynamic Page



μPC1352C BAND PASS COIL

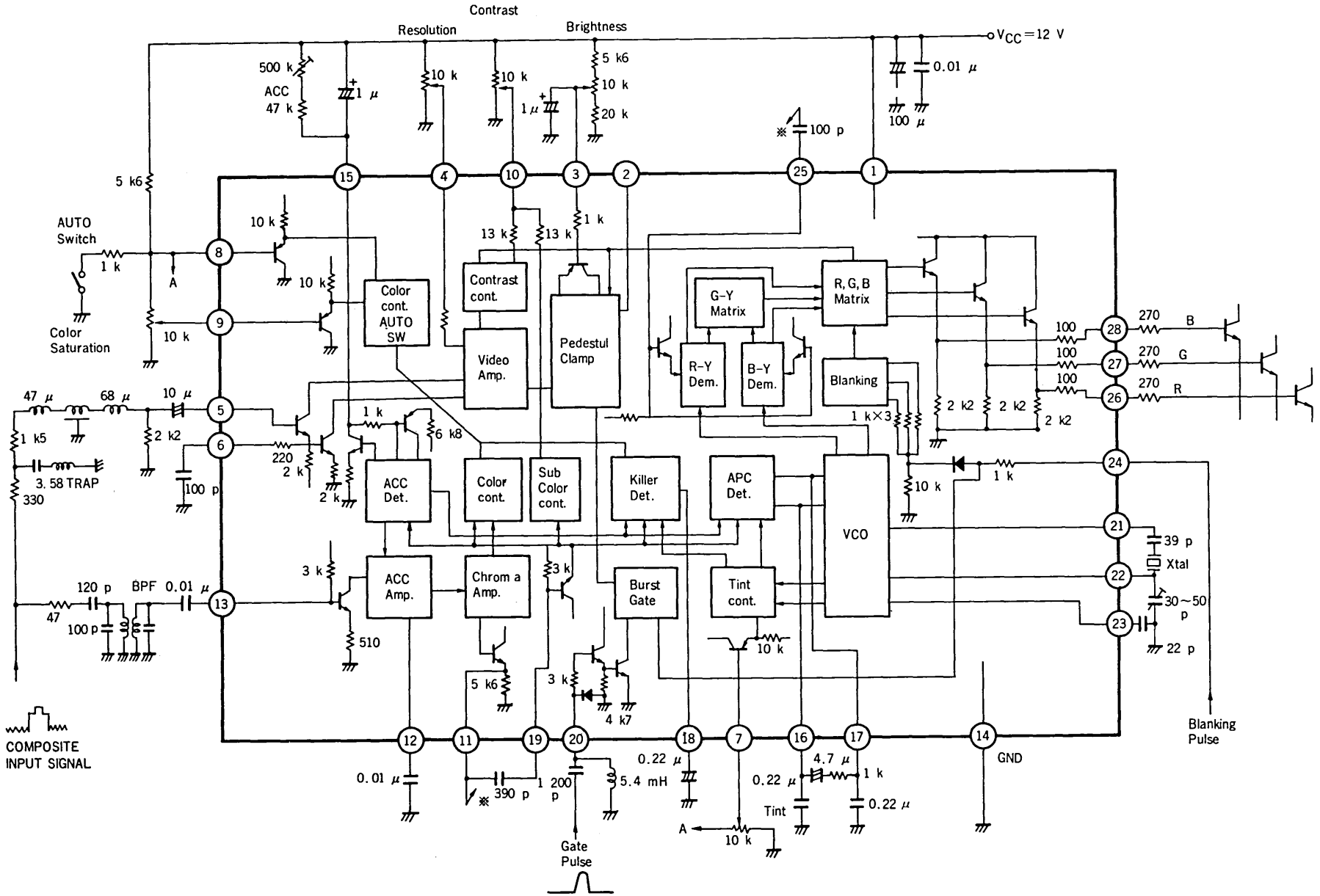


Pin Connection

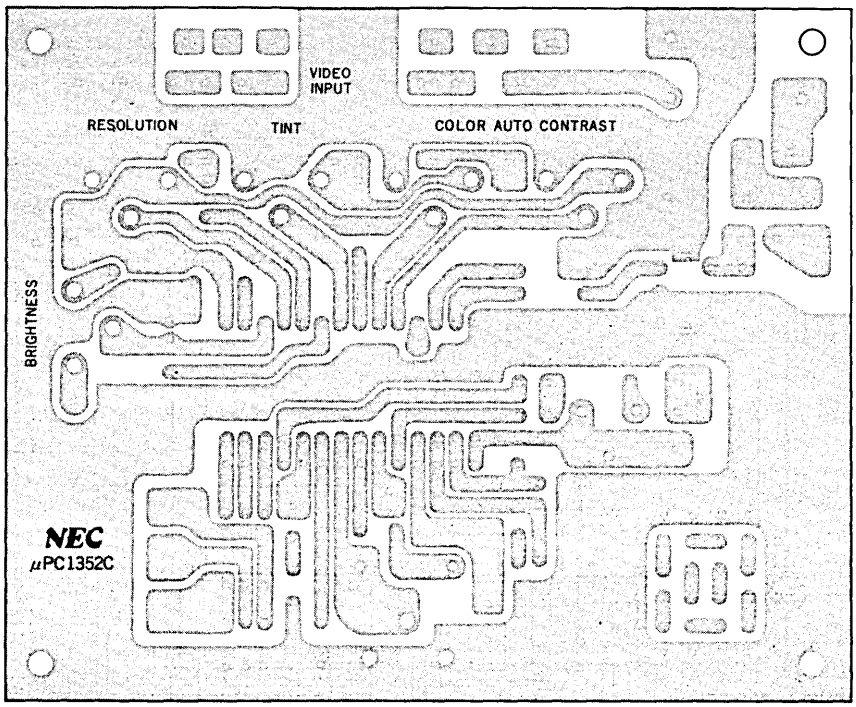
①–③ 88T Qu 15±20 % at f=3.58 MHz
④–⑥ 43-1/4T Qu 24±20 % at f=3.58 MHz

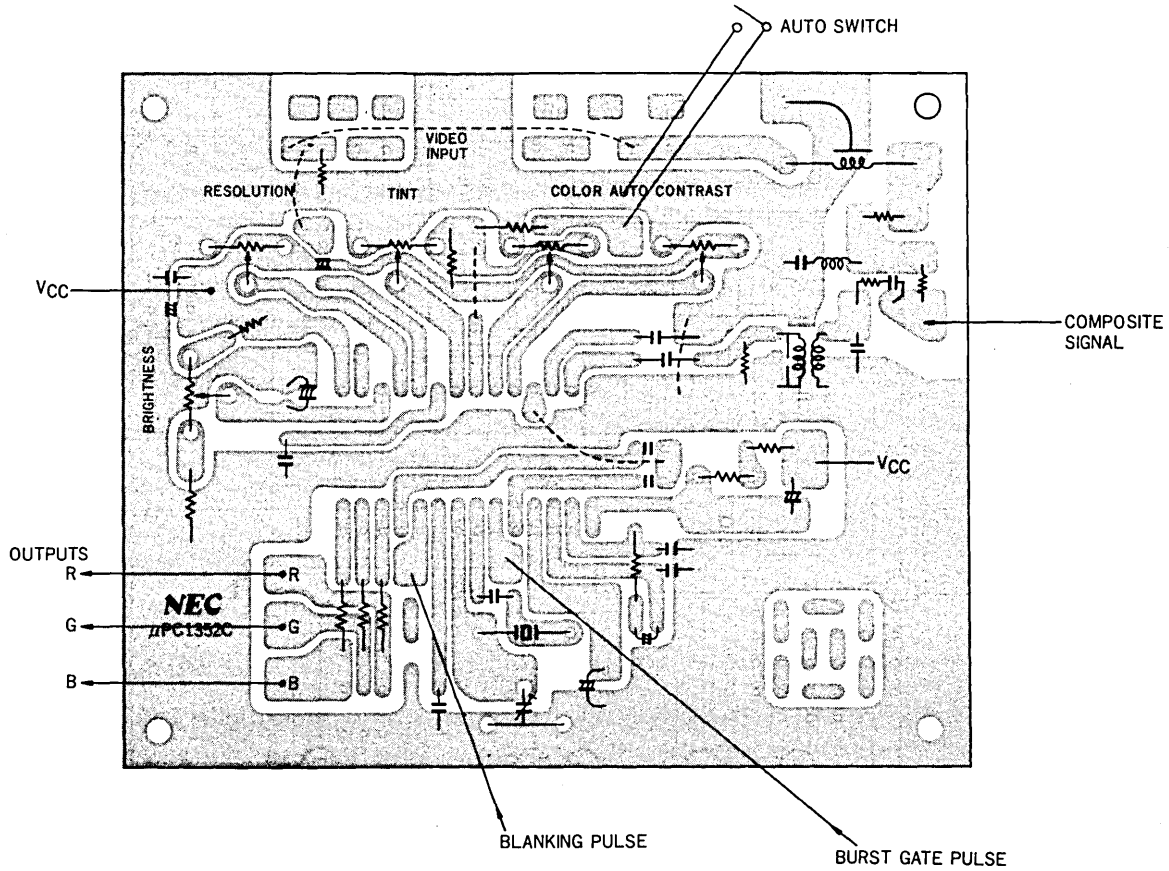
WIRE MATERIAL
0.12 φ OUEW
INSIDE CAPACITOR
C_1 = 47 pF

APPLICATION CIRCUIT



μPC1352C PRINTED CIRCUIT BOARD PATTERN (BOTTOM VIEW)





BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1364C2

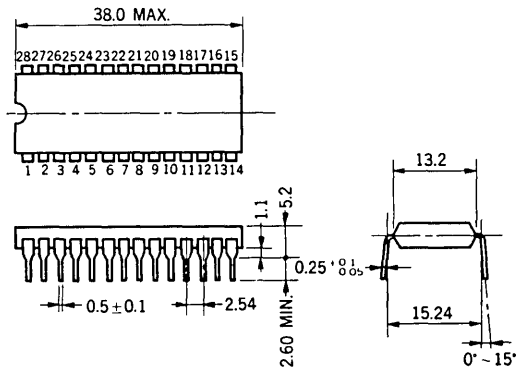
CHROMINANCE PROCESSOR FOR SECAM COLOR TV
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

μPC1364C2 is an integrated circuit for the chrominance signal processing of SECAM system receivers. This IC in 28 pins dual in line package has the functions required for the chrominance signal processing such as limitters, (R-Y)/(B-Y) demodulators, SECAM switch, identification circuit, killer, color control, clamp and R/G/B matrix circuit. The outputs are available in original R, G, B color signals. In addition, by the combination with NEC's PAL chrominance IC – μPC1365C, PAL/SECAM dual system can be realized.

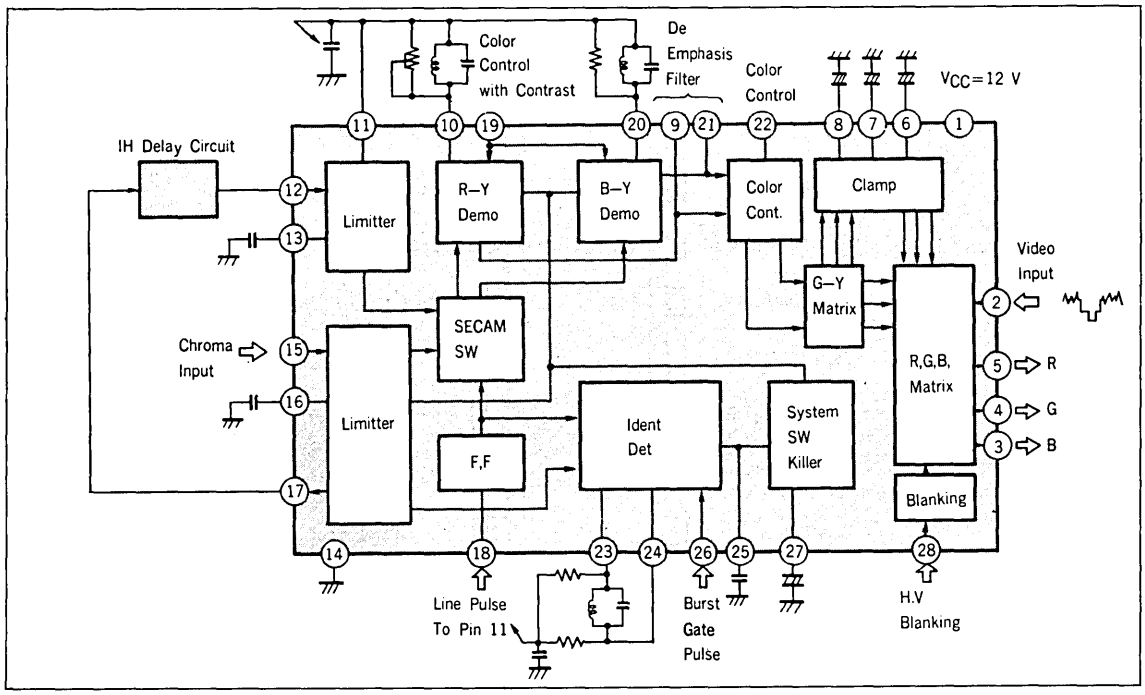
FEATURES

- R, G, B outputs in original color signals.
- PAL/SECAM dual system capability by the combination of μPC1364C2 and μPC1365C.
- Excellent white balance and crosstalk characteristics.
- Simple adjustment for contrast level and color control.

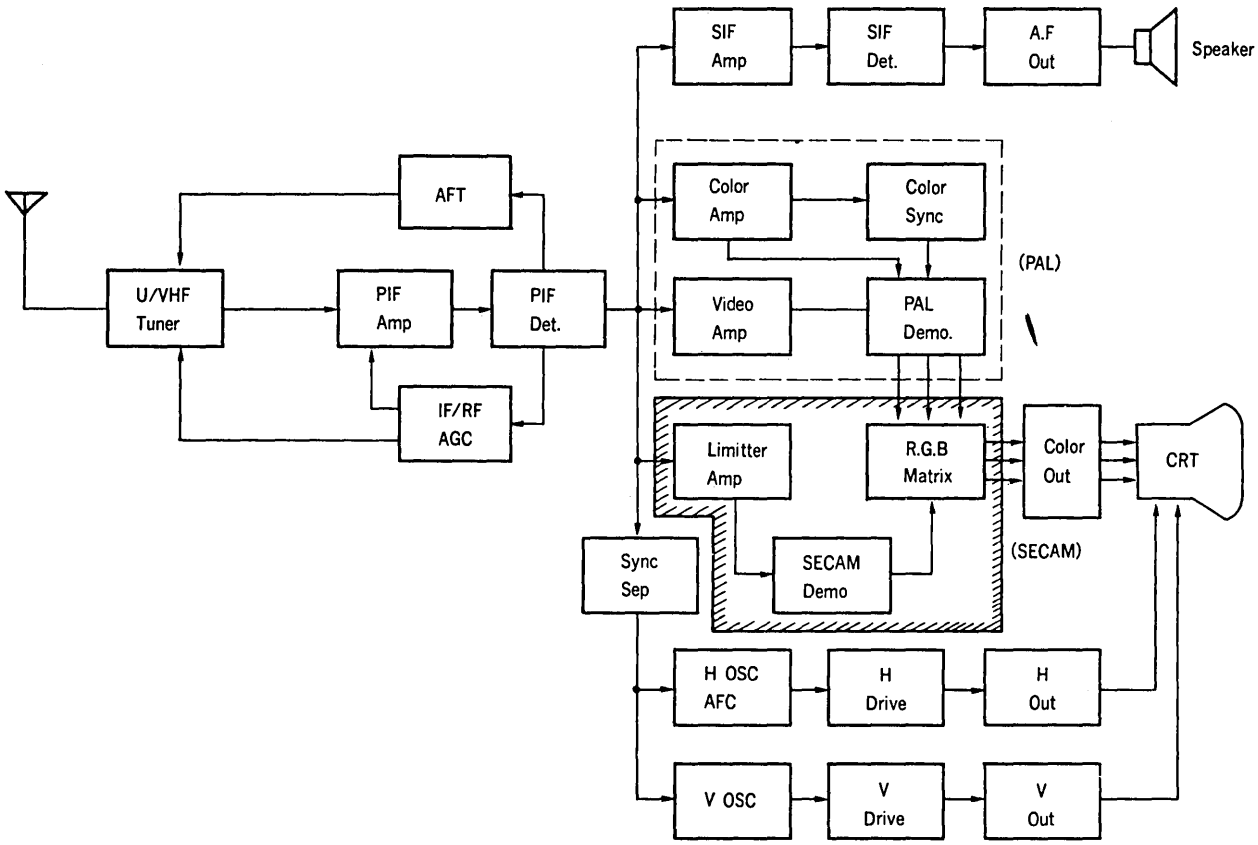
PACKAGE DIMENSIONS in millimeters



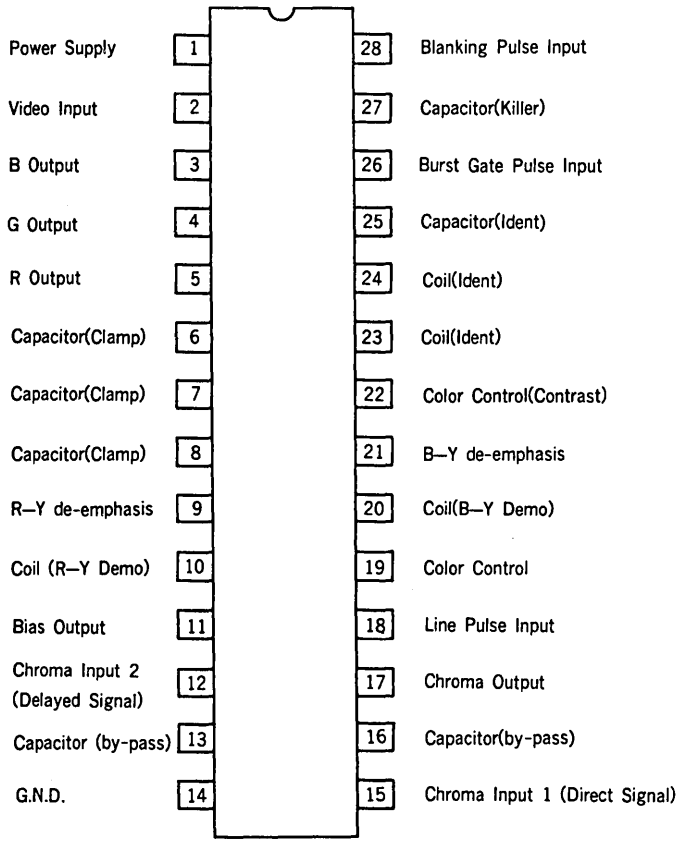
BLOCK DIAGRAM



TV BLOCK DIAGRAM (PAL-SECAM DUAL SYSTEM)



PIN CONNECTION (Top View)



STANDARD USING CONDITIONS

Supply Voltage	12	V
Chroma Input Signal (Burst Signal)	200	mV_{p-p}
Video Input Signal	1	V_{p-p}
Video Input Signal (Black Level)	10	V_{DC}
Burst Gate Pulse	3	V_p
Line Pulse	3	V_p
Blanking Pulse	3	V_p
R.G.B. Output Black Level	2	V
Color Controlling Voltage (Pin 19)	5.2 to 6.7 to 8.2	V
Color Controlling Voltage (Pin 22) (Relative Contrast)	5.9 to 7.4 to 8.9	V

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C Unless otherwise)

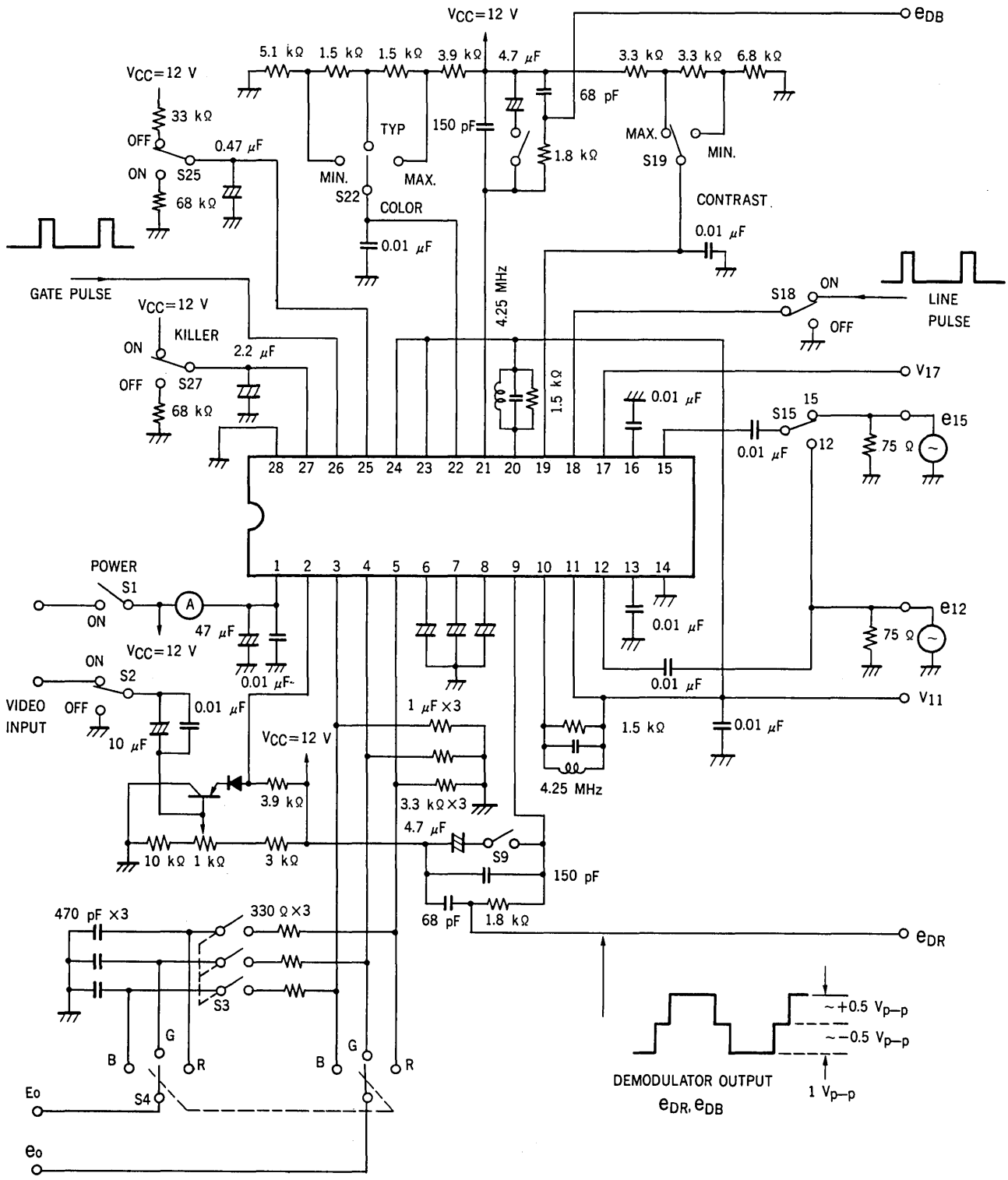
Supply Voltage	V_{CC}		15	V
Signal Input Voltage	e_i		5	V_{p-p}
Pulse Input Voltage	e_p		±6	V
Power Dissipation	P_d	(Ta = +70° C)	750	mW
Operating Temperature	T_{opt}		-20 to +70	°C
Storage Temperature	T_{stg}		-40 to +125	°C

ELECTRICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted, V_{CC} = 12 V) Contrast max, Color typ.

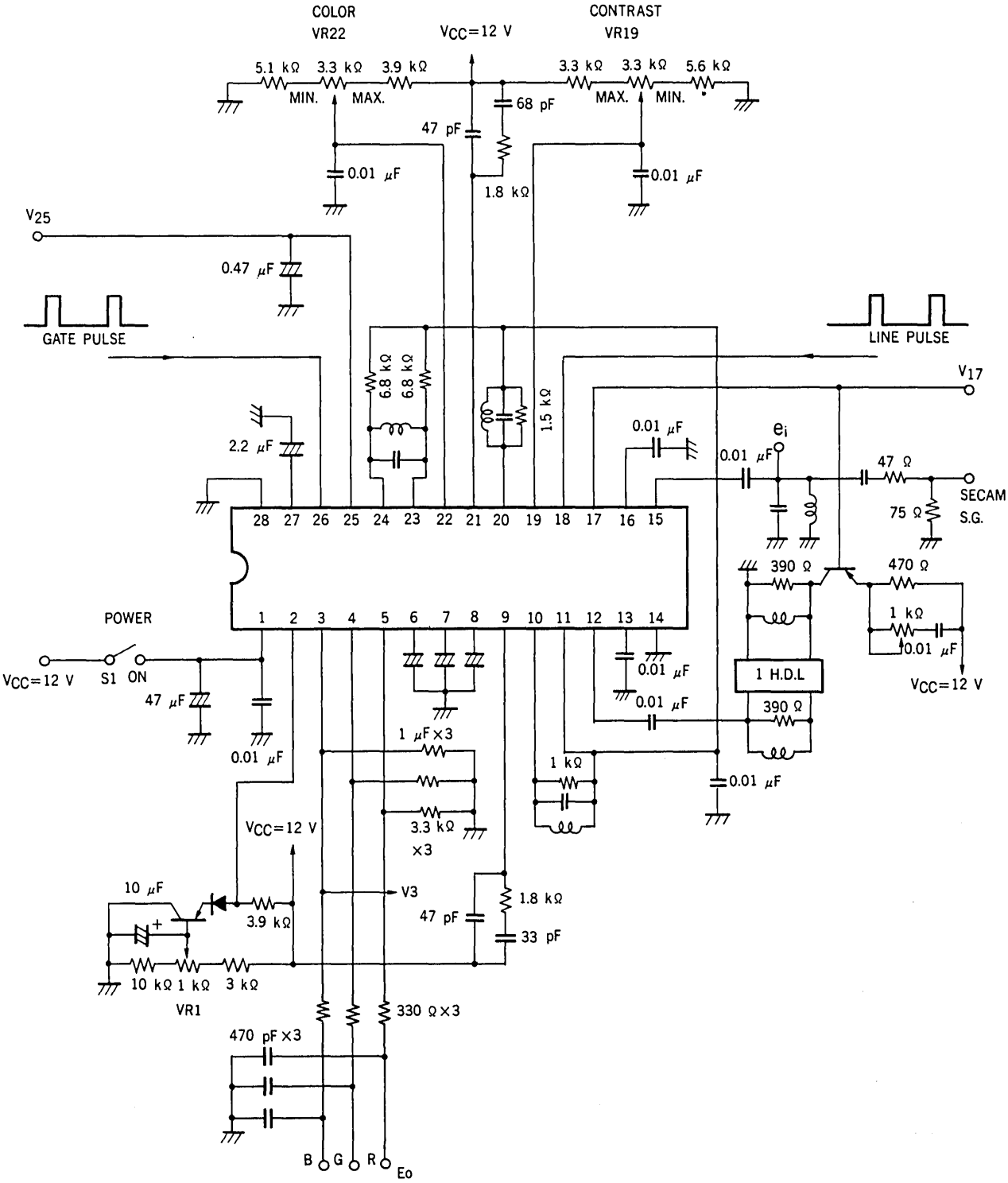
NO	CHARACTERISTIC	SYMBOL	TEST CKT	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
1	Supply Current	I_{CC}	1	33	45	57	mA	No Input Signal, Killer on V3 = 3.5 V
2	Pin 11 Voltage	V_{11}	1	1.9	2.3	2.7	V	Same as No. 1
3	Pin 17 Voltage (Killer off)	V_{17}	1	8.0	8.6	9.2	V	Same as No. 1, Killer off
4	Pin 17 Voltage (Killer on)	V_{17k}	1	11.0	11.3	11.6	V	Same as No. 1, Killer on
5	Demodulator Output	e_{DB}, e_{DR}	1	0.6	0.9	1.3	V_{p-p}	f12 = 4.02 MHz, f15 = 4.48 MHz, $e_{12} = e_{15}$ = 200 mV_{p-p}
6	Limitting Sensitivity	e_L	1	2.5	5	10	mV_{p-p}	f_{15} = 4.25 MHz ±230 kHz, e_{DB} = −3 dB
7	A.M. Reject Ratio	AMR	1	34	40	—	dB	f15 = 4.25 MHz, AM mod = 30 %, fm = 1 kHz, e_{15} = 200 mV_{p-p}, Line Pulse off, Compare with e_{DB}
8	Cross talk Level	CT	1	37	43	—	dB	f12 = 4.30 MHz, f15 = 4.25 MHz beat frq. = 50 kHz, Compare with e_{DB}, e_{DR}
9	Residual Carrier Level	e_{car}	1	—	100	200	mV_{p-p}	$e_{12} = e_{15}$ = 200 mV_{p-p}, f12 = f15 = 4.25 MHz
10	Maximum Color Differential Output	e_{OM}	1	4.5	5.7	—	V_{p-p}	Set $e_{DB} = e_{DR}$ = 1 V_{p-p} (±0.5 V_{p-p}) by f12, f15, Color max.
11	(B-Y), (R-Y) Color Differential Output	e_{OB}, e_{OR}	1	2.0	3.0	4.0	V_{p-p}	Same as No. 10 Color typ.
12	Demodulator (G-Y)/(B-Y) Ratio	G/B	1	0.17	0.19	0.21	times	Same as No. 11, e_{DR} = 0 V_{p-p}
13	Demodulator (G-Y)/(R-Y) Ratio	G/R	1	0.46	0.51	0.56	times	Same as No. 11, e_{DB} = 0 V_{p-p}
14	Maximum Color Gain	A_{CR}, A_{CB}	1	17	19	21	dB	Set $e_{DB} = e_{DR}$ = 0.3 V_{p-p} by f12, f15 Color max.
15	Color Gain Relative Ratio	A_{CR}/A_{CB}	1	—	0	±7	%	Same as No. 14
16	Contrast Cont. Range	e_{OC}	1	15	17	19	dB	Contrast max. to min., Color typ. Set $e_{OB} = e_{OR}$ = 1 V_{p-p} by f12, f15 at Contrast max.
17	Residual Color Level (Killer on)	e_{OK}	1	—	—	30	mV_{p-p}	Set $e_{OB} = e_{OR}$ = 1 V_{p-p} by f12, f15, at Killer off, Killer on
18	DC Output Voltge	Eo	1	2.7	3.5	4.3	V	No Input Signal, Killer on, V2 = 10.3 V
19	DC Output Difference Voltage	Ex-y	1	−200	0	200	mV	No Input Signal, Killer on, V3 = 3.5 V
20	Eo Temperature Coefficient	ΔEo/ΔT	1	−2	0	+2	mV/°C	V3 = 3.5 V at Ta = 25 °C, Ta = -20 to +70 °C
21	Ex-y Temperature Coefficient	ΔEx-y (T)	1	—	0	±60	mV	Same as No. 20
22	Ex-y Supply Voltage Coefficient	ΔEx-y (V)	1		0	±60	mV	V3 = 3.5 V at V_{CC} = 12 V, V_{CC} = 12 V ± 20 %
23	Y Amp. Voltage Gain	Ay	1	4.3	4.8	5.3	times	e_y = 0.5 V_{p-p}, f = 10 kHz, V3 = 3.5 V, Killer on
24	Y Amp. Frequency Characteristic	f_y	1	5	6	—	MHz	e_y = 0.5 V_{p-p}, 0 dB = Ay, −3 dB
25	Over all Color Differential Output Voltage	e_{OT}	2	2.5	3.6	5.0	V_{p-p}	e_{in} = 200 mV_{p-p}, Color bar Signal, Color typ., Contrast max., B Output
26	Killer Sensitivity	e_k	2	28	34	40	dB	0 dB = e_{in} 200 mV_{p-p}, Color bar Signal, Attenuator Level at Killer on
27	White Balance Changing Level By Input	ΔEx-y (IN)	2		—	±60	mV	e_{in} = 20 to 400 mV_{p-p}, White Signal
28	White Balance Changing Level By Color Cont.	ΔEx-y (Color)	2		0	±60	mV	e_{in} = 200 mV_{p-p}, White Signal, Contrast max., Color max. to min.

NO	CHARACTERISTIC	SYMBOL	TEST CKT	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
29	White Balance Changing Level by Contrast Cont	ΔEx-y (Contrast)	2		0	±60	mV	e_{in} = 200 mV_{p-p}, White Signal, Color typ., Contrast max. to min.
30	Pin 15 Input Impedance	Ri_{15} Ci_{15}	3	2.8 4.5	4 6.6	5.6 9.5	kΩ pF	f = 4.4 MHz, 100 mV_{p-p}
31	Pin 12 Input Impedance	Ri_{12} Ci_{12}	3	2.8 3.7	4 5.5	5.6 8.0	kΩ pF	f = 4.4 MHz, 100 mV_{p-p}
32	Pin 10 Input Impedance	Ri_{10} Ci_{10}	3		17 15		kΩ pF	Same as No. 31
33	Pin 20 Input Impedance	Ri_{20} Ci_{20}	3		17 15		kΩ pF	Same as No. 31
34	Pin 23, 24 Input Impedance	$Ri_{23, 24}$ $Ci_{23, 24}$	3		25 13		kΩ pF	Same as No. 31
35	Pin 17 Output Resistance	Ro_{17}	–	120	180	270	Ω	
36	Pin 9, 21 Output Resistance	$Ro_{9, 21}$	–	4.0	6.0	8.0	kΩ	
37	Minimum Gate Pulse Voltage	$V_{C\ (min)}$				1.5	V	
38	Minimum Trigger Pulse Voltage	V_{FF}				1.5	V	
39	Minimum Blanking Pulse Voltage	V_{BLK}			–	2.0	V	

TEST CIRCUIT 1



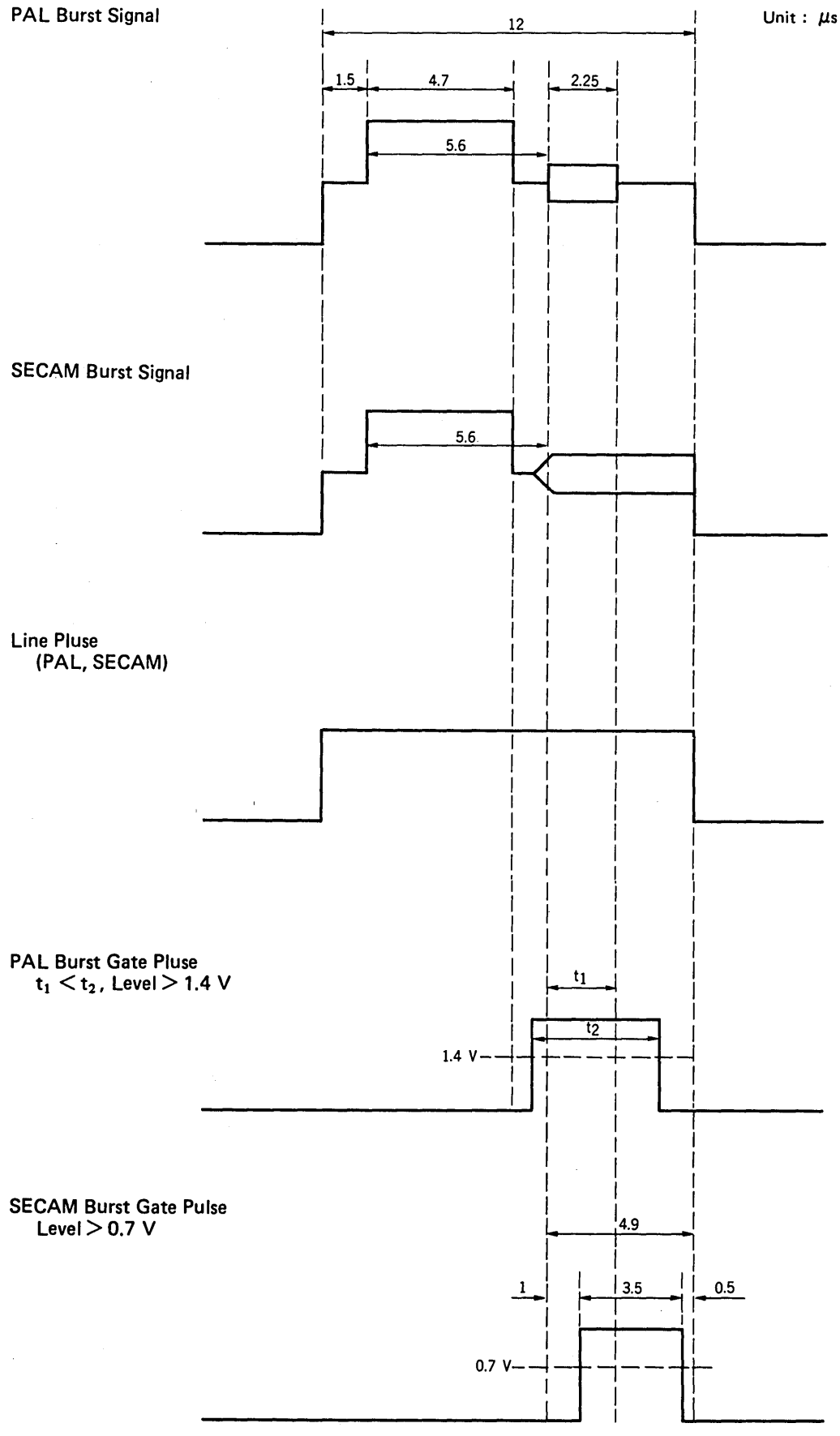
TEST CIRCUIT 2

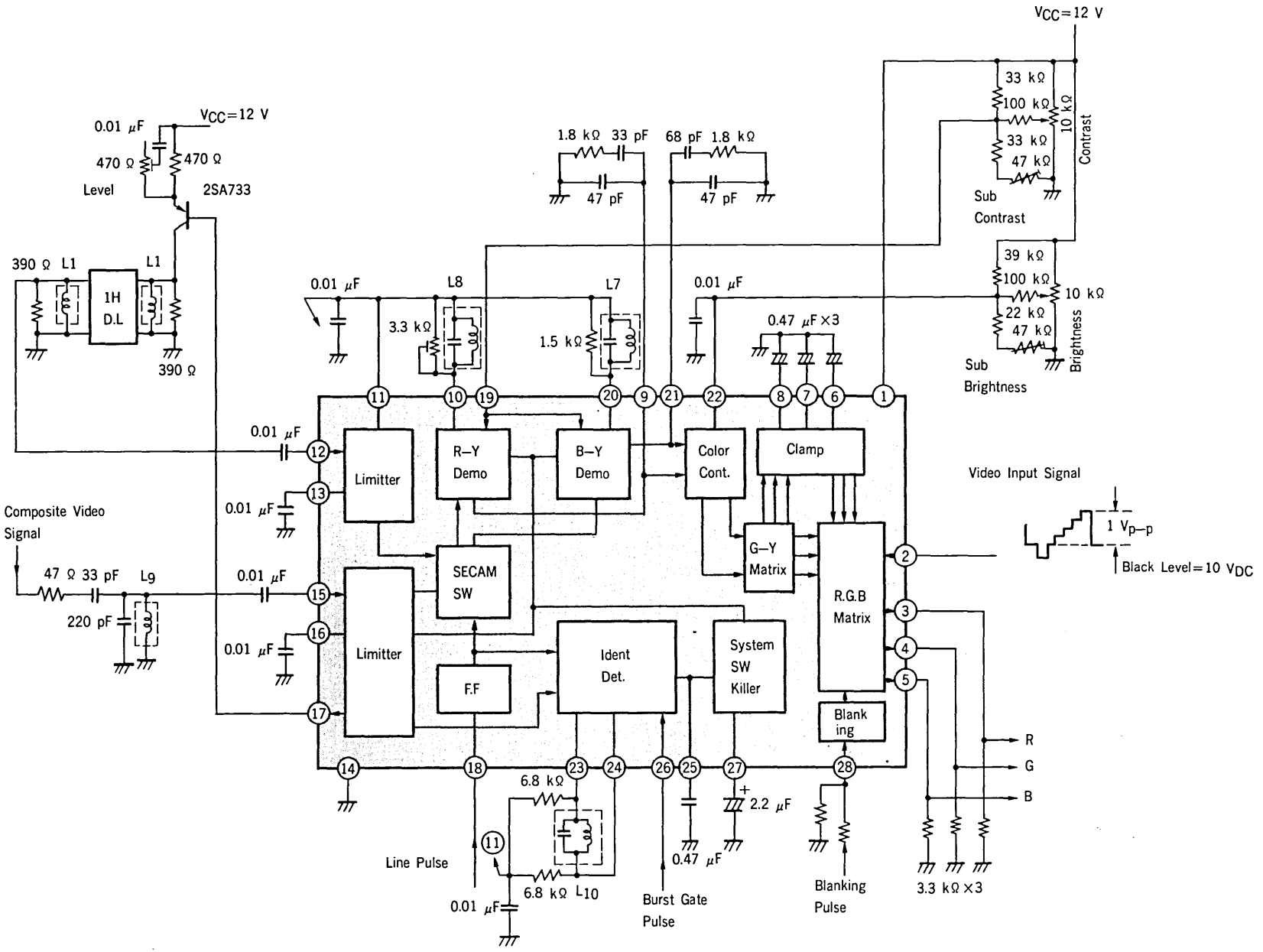


No.	SYMBOL	Test Circuit	S1 Power	S2 Video Input	S3 LPF	S4 RGB	S9 R-Y Detect	S15 Chrome Input	S18 Line Pulse Input	S19 Contrast	S21 B-Y Detect	S22 Color	S25 Reset	S27 Color Killer	VR2 Video DC Input	VR19 Contrast Linked	VR22 Color Control	Input level and etc.	Measuring point and instrument
1	I_{CC}	1	OFF→ON	OFF	ON	R	OFF	15	ON	MAX	OFF	TYP	OFF	ON	V_3 = 3.5 V	–	–	$e_{15} = e_{12} = 0\ mV_{p\text{-}p}$	Pin 1 (DC Ammeter)
2	V_{11}	1	OFF→ON	OFF	ON	R	OFF	15	ON	MAX	OFF	TYP	OFF	ON	V_3 = 3.5 V	–	–	$e_{15} = e_{12} = 0\ mV_{p\text{-}p}$	Pin 11 (Digital Voltmeter)
3	V_{17}	1	OFF→ON	OFF	ON	R	OFF	15	ON	MAX	OFF	TYP	OFF	OFF	V_3 = 3.5 V	–	–	$e_{15} = e_{12} = 0\ mV_{p\text{-}p}$	Pin 17 (Digital Voltmeter)
4	V_{17K}	1	OFF→ON	OFF	ON	R	OFF	15	ON	MAX	OFF	TYP	OFF	ON	V_3 = 3.5 V	–	–	$e_{15} = e_{12} = 0\ mV_{p\text{-}p}$	Pin 17 (Digital Voltmeter)
5	e_{DB}, e_{DR}	1	OFF→ON	OFF	ON	R	OFF	15	ON	MAX	OFF	TYP	OFF	OFF	V_3 = 3.5 V	–	–	e_{15} = 200 $mV_{p\text{-}p}$ (4.48 MHz) e_{12} = 200 $mV_{p\text{-}p}$ (4.02 MHz)	e_{DB}, e_{DR} Output (Oscilloscope)
6	e_L	1	OFF→ON	OFF	ON	R	OFF	15	OFF	MAX	OFF	TYP	ON	OFF	V_3 = 3.5 V	–	–	e_{15} = 200 $mV_{p\text{-}p}$ (4.25 MHz, Δf = ±230 kHz) $e_{12} = 0\ mV_{p\text{-}p}$	e_{15} input level providing −3 dB of regular e_{DB} output (Oscilloscope)
7	AMR	1	OFF→ON	OFF	ON	R	OFF	15	OFF	MAX	OFF	TYP	ON	OFF	V_3 = 3.5 V	–	–	e_{15} = 200 $mV_{p\text{-}p}$ (4.25 MHz, AM 30% MOD, f_M = 1 kHz) $e_{12} = 0\ mV_{p\text{-}p}$	Calculate ratio of values of e_{DS} among this condition and No.5 condition (Oscilloscope)
8	CT	1	OFF→ON	OFF	ON	R	OFF	15	OFF	MAX	OFF	TYP	ON	OFF	V_3 = 3.5 V	–	–	e_{15} = 200 $mV_{p\text{-}p}$ (4.25 MHz) e_{12} = 200 $mV_{p\text{-}p}$ (4.30 MHz)	Calculate ratio among the beat output of e_{DB}, e_{DR}, and No.5 values (Oscilloscope)
9	e_{car}	1	OFF→ON	OFF	OFF	RGB	OFF	12	ON	MAX	OFF	TYP	OFF	OFF	V_3 = 3.5 V	–	–	e_{15} = 200 $mV_{p\text{-}p}$ (4.25 MHz) e_{12} = 200 $mV_{p\text{-}p}$ (4.25 MHz)	Remain carrier level of e_{01} in tracing period (Oscilloscope)
10	e_{OM}	1	OFF→ON	OFF	ON	RB	OFF	15	ON	MAX	OFF	MAX	OFF	OFF	V_3 = 3.5 V	–	–	Set $e_{DB} = e_{DR}$ = 1 $V_{p\text{-}p}$ e_{15} = 200 $mV_{p\text{-}p}$ (roughly 4.48 MHz) e_{12} = 200 $mV_{p\text{-}p}$ (roughly 4.02 MHz)	e_{01} output (Oscilloscope)
11	e_{OB}, e_{OR}	1	OFF→ON	OFF	ON	RB	OFF	15	ON	MAX	OFF	TYP	OFF	OFF	V_3 = 3.5 V	–	–	Set $e_{DB} = e_{DR}$ = 1 $V_{p\text{-}p}$ e_{15} = 200 mV (roughly 4.48 MHz) e_{12} = 200 mV (roughly 4.02 MHz)	e_{01} Output (Oscilloscope)
12	G/B	1	OFF→ON	OFF	ON	GB	ON	15	ON	MAX	OFF	TYP	OFF	OFF	V_3 = 3.5 V	–	–	Set $e_{DB} = e_{DR}$ = 1 $V_{p\text{-}p}$ e_{15} = 200 mV (roughly 4.48 MHz) e_{12} = 200 mV (roughly 4.02 MHz)	e_{01} Output (Oscilloscope) Calculate ratio of G/B
13	G/R	1	OFF→ON	OFF	ON	RG	OFF	15	ON	MAX	ON	TYP	OFF	OFF	V_3 = 3.5 V	–	–	Set $e_{DB} = e_{DR}$ = 1 $V_{p\text{-}p}$ e_{15} = 200 $mV_{p\text{-}p}$ (roughly 4.48 MHz) e_{12} = 200 $mV_{p\text{-}p}$ (roughly 4.02 MHz)	e_{01} Output (Oscilloscope) Calculate ratio of G/R
14	A_{CR}, A_{CB}	1	OFF→ON	OFF	ON	RB	OFF	15	ON	MAX	OFF	MAX	OFF	OFF	V_3 = 3.5 V	–	–	Set $e_{DB} = e_{DR}$ = 0.3 $V_{p\text{-}p}$ e_{15} = 200 $mV_{p\text{-}p}$ (roughly 4.32 MHz) e_{12} = 200 $mV_{p\text{-}p}$ (roughly 4.18 MHz)	e_{01} output (oscilloscope) Calculate gain in case of $e_{DB} = e_{DR}$ = 0.3 $V_{p\text{-}p}$
15	A_{CR}/A_{CB}	1	OFF→ON	OFF	ON	RB	OFF	15	ON	MAX	OFF	MAX	OFF	OFF	V_3 = 3.5 V	–	–	Set $e_{DB} = e_{DR}$ = 0.3 $V_{p\text{-}p}$ e_{15} = 200 $mV_{p\text{-}p}$ (roughly 4.32 MHz) e_{12} = 200 $mV_{p\text{-}p}$ (roughly 4.18 MHz)	Calculate ratio among A_{CR} and A_{CB} of No. 5

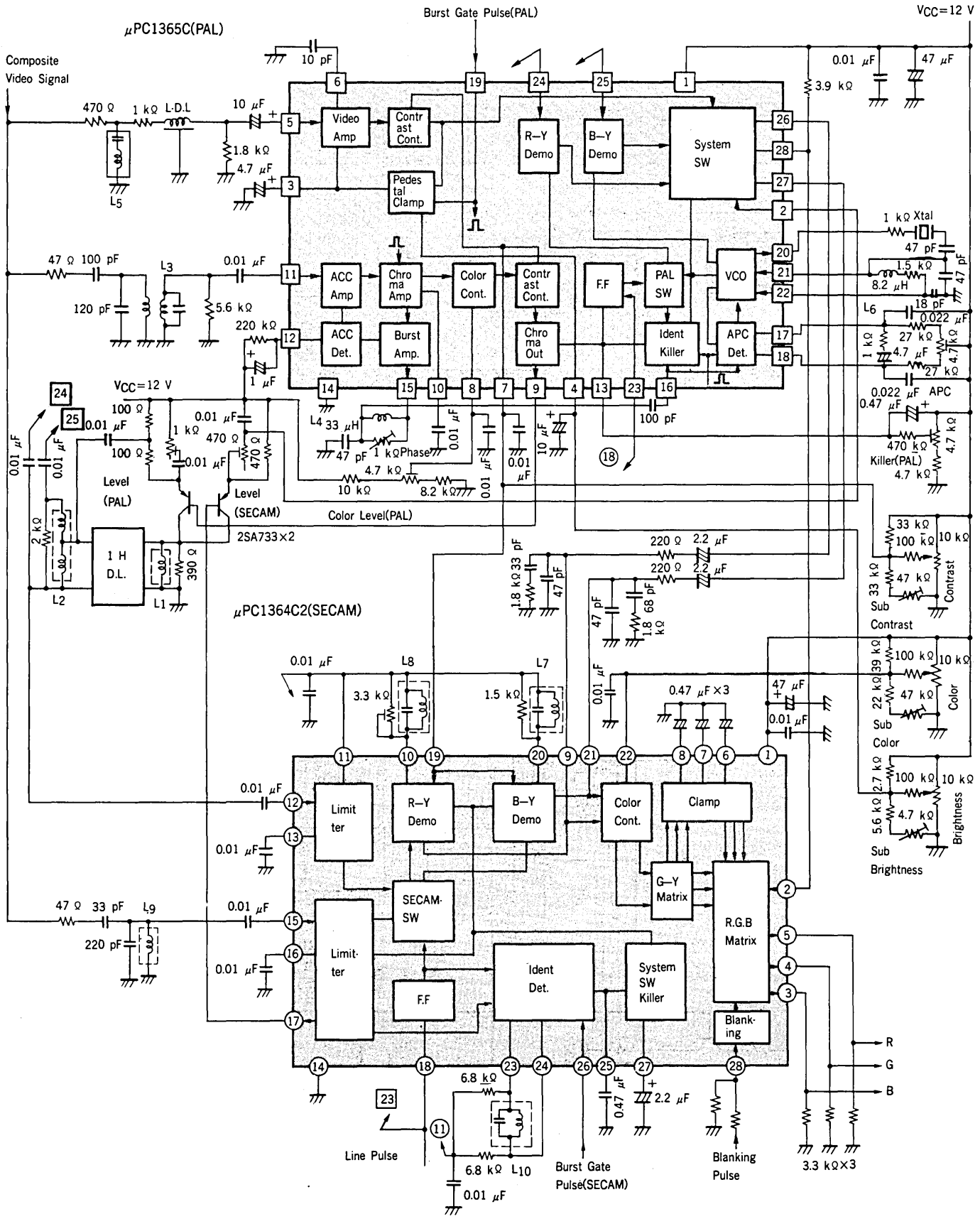
No. / SYMBOL	Test Circuit	S1 Power	S2 Video Input	S3 LPF	S4 RGB	S9 R-Y Detect	S15 Chrome Input	S18 Line Pulse Input	S19 Contrast	S21 B-Y Detect	S22 Color	S25 Reset	S27 Color Killer	VR2 Video DC Input	VR19 Contrast Linked	VR22 Color Control	Input level and etc.	Measuring point and instrument
16 e_{OC}	1	OFF→ON	OFF	ON	RB	OFF	15	ON	MAX ↓ MIN	OFF	TYP	OFF	OFF	V_3 = 3.5 V	–	–	Set $e_{DB} = e_{DR}$ = 1 $V_{p\text{-}p}$ e_{15} = 200 $mV_{p\text{-}p}$ (roughly 4.48 MHz) e_{12} = 200 $mV_{p\text{-}p}$ (roughly 4.02 MHz)	Calculate ratio of values of e_{01} output between MAX and MIN of contrast (Oscilloscope)
17 e_{OK}	1	OFF→ON	OFF	ON	RB	OFF	15	ON	MAX	OFF	TYP	OFF	ON	V_3 = 3.5 V	–	–	Color killer is OFF Set $e_{DB} = e_{DR}$ = 1 $V_{p\text{-}p}$ e_{15} = 200 mV (roughly 4.48 MHz) e_{12} = 200 mV (roughly 4.02 MHz)	Color killer ON e_{01} output (Oscilloscope)
18 E_o	1	OFF→ON	OFF	ON	RGB	OFF	15	ON	MAX	OFF	TYP	OFF	ON	V_2 = 10.3 V	–	–	$e_{15} = e_{12}$ = 0 $mV_{p\text{-}p}$ Set V_3 = 10.3 V by VR2	e_{01} DC output voltage (Digital Voltmeter)
19 $E_{x\text{-}y}$	1	OFF→ON	OFF	ON	RGB	OFF	15	ON	MAX	OFF	TYP	OFF	ON	V_3 = 3.5 V	–	–	$e_{15} = e_{12}$ = 0 $mV_{p\text{-}p}$	Difference among two values of RGB output DC voltage of No. 18 (Digital voltmeter)
20 $\Delta E_o/\Delta T$	1	OFF→ON	OFF	ON	RGB	OFF	15	ON	MAX	OFF	TYP	OFF	ON	V_3 = 3.5 V	–	–	$e_{15} = e_{12}$ = 0 $mV_{p\text{-}p}$ Set V_3 = 3.5 V at Ta = 25 °C Ta = −20 °C to +70 °C	e_{01} DC output voltage Calculate temperature coefficient of E_o (Digital voltmeter)
21 $\Delta E_{x\text{-}y}(T)$	1	OFF→ON	OFF	ON	RGB	OFF	15	ON	MAX	OFF	TYP	OFF	ON	V_3 = 3.5 V	–	–	$e_{15} = e_{12}$ = 0 $mV_{p\text{-}p}$ Set V_3 = 3.5 V at Ta = 25 °C Ta = −20 °C to +70 °C	e_{01} DC output voltage Maximum change of $E_{x\text{-}y}$ against Ta (Digital voltmeter)
22 $\Delta E_{x\text{-}y}(V)$	1	OFF→ON	OFF	ON	RGB	OFF	15	ON	MAX	OFF	TYP	OFF	ON	V_3 = 3.5 V	–	–	$e_{15} = e_{12}$ = 0 $mV_{p\text{-}p}$ Set V_3 = 3.5 V at V_{CC} = 12 V V_{CC} = 12 V ± 20 %	e_{01} DC output voltage Maximum change of $E_{x\text{-}y}$ against V_{CC} (Digital voltmeter)
23 Ay	1	OFF→ON	ON 0.5 $V_{p\text{-}p}$ 10 MHz	OFF	RGB	OFF	15	ON	MAX	OFF	TYP	OFF	ON	V_3 = 3.5 V	–	–	$e_{15} = e_{12}$ = 0 $mV_{p\text{-}p}$ e_y = 0.5 $V_{p\text{-}p}$ (10 kHz)	e_{02} (AC voltmeter) Calculate gain in case of input level is 0.5 $V_{p\text{-}p}$
24 fy	1	OFF→ON	ON 0.5 $V_{p\text{-}p}$ 10 MHz	OFF	RGB	OFF	15	ON	MAX	OFF	TYP	OFF	ON	V_3 = 3.5 V	–	–	$e_{15} = e_{12}$ = 0 $mV_{p\text{-}p}$ e_y = 0.5 $V_{p\text{-}p}$	Input frequency (frequency counter) in case of Ay is −3 dB of No. 23
25 e_{OT}	2	OFF→ON	–	–	–	–	–	–	–	–	–	–	–	V_3 = 3.5 V	MAX	TYP V_{22} = 6.6 V	SECAM Signal (Color bar) Input level 200 $mV_{p\text{-}p}$	B output (Oscilloscope)
26 e_k	2	OFF→ON	–	–	–	–	–	–	–	–	–	–	–	V_3 = 3.5 V	MAX	TYP V_{22} = 6.6 V	SECAM Signal (Color bar) 0 dB: Adjust V_{25} to maximum at input level is 200 $mV_{p\text{-}p}$ (Identification coil)	Color killer is ON $V_{17} \geqq$ 11 V (Digital voltmeter) Attenuation (Attenuator) SECAM Input signal level
27 $\Delta E_{x\text{-}y}(IN)$	2	OFF→ON	–	–	–	–	–	–	–	–	–	–	–	V_3 = 3.5 V	MAX	TYP V_{22} = 6.6 V	Adjust white level of R and B at SECAM signal (White) input level is 200 $mV_{p\text{-}p}$ (R−Y, B−Y Detection coil)	Difference among RGB (Digital voltmeter) Maximum change of $E_{x\text{-}y}$ between 20 and 400 $mV_{p\text{-}p}$ of input level
28 $\Delta E_{x\text{-}y}$(Color)	2	OFF→ON	–	–	–	–	–	–	–	–	–	–	–	V_3 = 3.5 V	MAX to MIN	MAX to MIN	Adjust white level of R and B at SECAM signal (White) input level is 200 $mV_{p\text{-}p}$ (R−Y, B−Y Detection coil)	Difference among RGB (Digital voltmeter) Maximum change of $E_{x\text{-}y}$ between MIN and MAX of Color Control
29 $\Delta E_{x\text{-}y}$(Contrast)	2	OFF→ON	–	–	–	–	–	–	–	–	–	–	–	V_3 = 3.5 V	MAX to MIN	TYP V_{22} = 6.6 V	Adjust white level of R and B at SECAM signal (White) input level is 200 $mV_{p\text{-}p}$ Contrast is MAX (R−Y, B−Y Detection Coil)	Difference among RGB (Digital voltmeter) Maximum change of $E_{x\text{-}y}$ between MIN and MAX of Contrast Control

μPC1364C2 (SECAM), μPC1365C (PAL) INPUT SIGNAL AND PULSE TIME RELATION

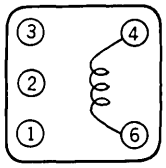



VCC=12 V
0.01 μF
470 Ω
470 Ω
Level
2SA733
390 Ω L1
L1
1H
D.L
390 Ω
1.8 kΩ 33 pF
47 pF
68 pF 1.8 kΩ
47 pF
33 kΩ
100 kΩ
10 kΩ
Contrast
33 kΩ
47 kΩ
Sub
Contrast
39 kΩ
100 kΩ
10 kΩ
22 kΩ
47 kΩ
Brightness
Sub
Brightness
0.01 μF
L8
3.3 kΩ
L7
1.5 kΩ
0.01 μF
0.47 μF×3
11
10
19
20
9
21
22
8
7
6
1
0.01 μF
12
Limitter
R–Y
Demo
B–Y
Demo
Color
Cont.
Clamp
Video Input Signal
1 Vp–p
Black Level=10 VDC
13
0.01 μF
Composite Video
Signal
47 Ω 33 pF
L9
220 pF
0.01 μF
15
SECAM
SW
G–Y
Matrix
R.G.B
Matrix
2
3
4
5
0.01 μF
16
Limitter
F.F
Ident
Det.
System
SW
Killer
Blank
ing
17
R
G
B
14
18
23
24
26
25
27
28
6.8 kΩ
2.2 μF
11
Line Pulse
6.8 kΩ
L10
0.01 μF
0.47 μF
Burst Gate
Pulse
Blanking
Pulse
3.3 kΩ×3

PAL-SECAM DUAL SYSTEM



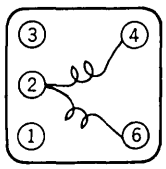
L1 1H D.L. Matching
Input Coil
(PAL, SECAM)



Type No. TKRNS – 24984NK (Pink Core)
Toko Corp.

fo ; 4.43 MHz
6 - 4 ; 18 T
C out ; 330 pF (4 - 6)
Qu ; 59 ± 20 %
Wire Material ; 0.1/UEW

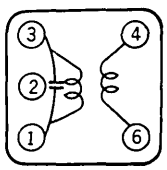
L2 1H D.L. Matching
Output Coil
(PAL, SECAM)



Type No. TKRNS – 24985VN (Black Core)
Toko Corp.

fo ; 4.43 MHz
4 - 2 ; 18 T
2 - 6 ; 18 T
C out ; 75 pF (4 - 6)
Qu ; 44 ± 20 %
Wire Material ; 0.1/UEW

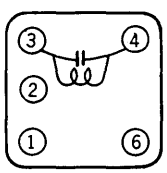
L3 Chroma Input Coil
(PAL)



Type No. 163NEF – 1148 WWJ (No Core)
Toko Corp.

fo ; 4.43 MHz
6 - 4 ; 35 ¼ T
3 - 1 ; 76 T
C in ; 47 pF
Wire Material ; 0.1/UEW

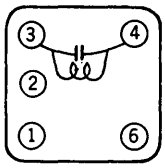
L7 (B-Y) Demodulator
(SECAM)



Type No. TKRES – 25656AYC (Yellow Core)
Toko Corp.

fo ; 4.25 MHz
3 - 4 ; 33 ½ T
C in ; 82 pF (3 - 4)
Qu ; 75 ± 20 %
Wire Material ; 0.1/OUEW

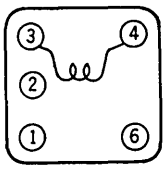
L8 (R-Y) Demodulator
(SECAM)



Type No. TKRES – 25658AYK (Green Core)
Toko Corp.

fo ; 4.406 MHz
3 - 4 ; 32 ½ T
C in ; 82 pF
Qu ; 75 ± 20 %
Wire Material ; 0.1/OUEW

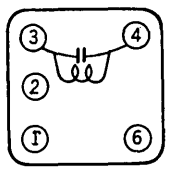
L9 Bell Filter
(SECAM)



Type No. TKRNS – 25657AYC (Red Core)
Toko Corp.

3 - 4 ; 19 ½ T
C out ; 220 pF
Qu ; 70 ± 20 %
Wire Material ; 0.12/OUEW

L10 Ident Detector



Type No. TKRES – 25659AYC (Orange Core)
Toko Corp.

fo ; 4.406 MHz
3 - 4 ; 39 ½ T
C in ; 68 pF
Qu ; 63 ± 20 %
Wire Material ; 0.1/OUEW

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1365C

PAL CHROMINANCE AND LUMINANCE PROCESSOR
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

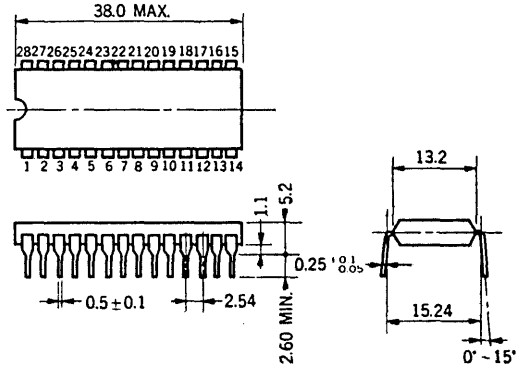
DESCRIPTION

μPC1365C is a luminance and chrominance stage LSI for PAL system TV sets. It contains luminance amplifier, chroma IF amplifier, sub-carrier oscillator, PAL switching circuit, chroma demodulator, matrix circuit, and the other necessary additions. It puts out R,G,B primary colors. This LSI restores 100 % of the DC level. And it is easy to adapt remote control system to "BRIGHTNESS", "CONTRAST", and "COLOR SATURATION", as the control terminals are designed to high impedance.

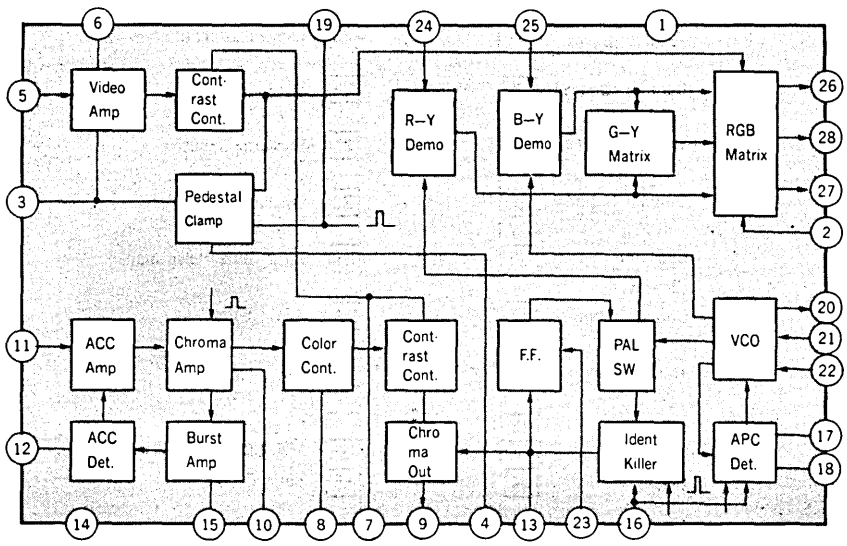
FEATURES

- This LSI has built-in function for PAL-SECAM dual system.
  1) Two ICs construction by NEC's SECAM IC μPC1364C2.
  2) Only one 1-H delay line is required for dual system.
  3) Automatically switchable function for PAL/SECAM signals.
- This LSI can process both of the chrominance and the luminance signals.
- Due to DC control method for color, contrast, and brightness control, the wiring is rather easy and the expansion to remote control receiver are also rather easy.
- The level of color killer circuit can be adjusted from the outside and the color killer circuit has proper hysterisis characteristics.
- The input circuit requires only a band pass filter and 4.43 MHz trap. Furthermore, the demodulated outputs are R,G,B signals. So that the chroma output stages are quite simplified.
- The contrast control can automatically adjust the levels of chroma and contrast- luminance signal under the relation that the normal picture is always kept.
- The output terminals of demodulated chroma signals and all input circuits are protected by the surge protection diode.

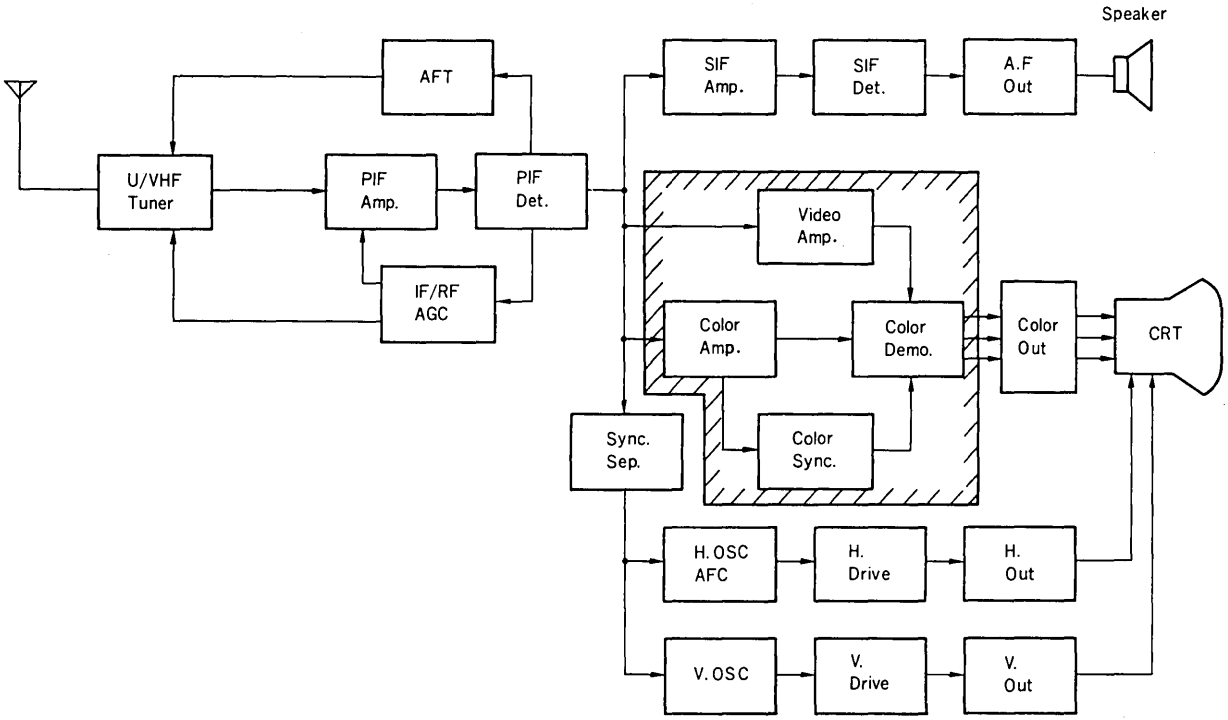
PACKAGE DIMENSIONS in millimeters



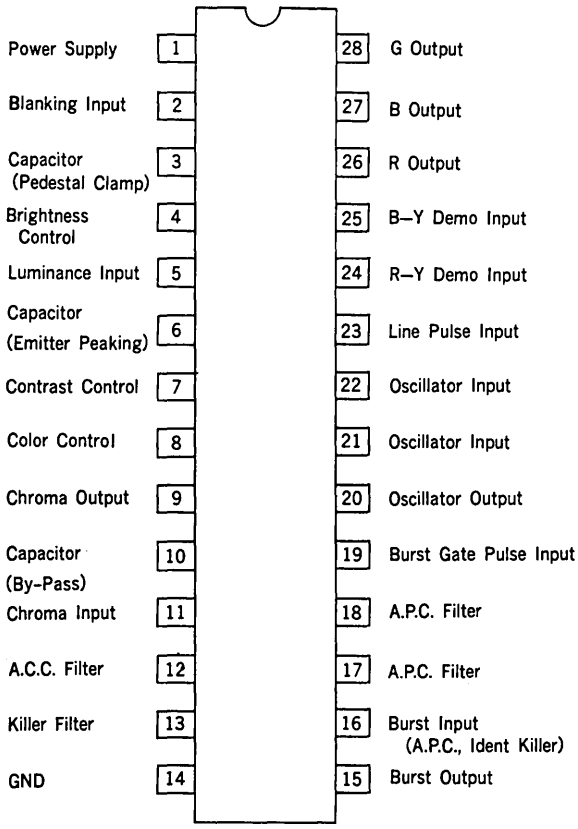
IC BLOCK DIAGRAM



TV BLOCK DIAGRAM



PIN CONNECTION (Top View)



μPC1365C Standard Using Conditions		
Supply Voltage	12	V
Chrominance Input Signal		
(Burst Signal Level)	100	mV_{p-p}
Luminance Input Signal	1	V_{p-p}
Gate Pulse Input Level	3	V_p
H. Pulse Input Level	3	V_p
Blanking Pulse Input Level	3	V_p
Demodulator Chrominance Input Signal	0.2	V_{p-p}
R,G,B Output Voltage (Black Level)	2.0	V
Color Saturation Controlling Voltage	0 to 12	V
Contrast Controlling Voltage	0 to 12	V
Brightness Controlling Voltage	0 to 12	V

ABSOLUTE MAXIMUM RATINGS (Ta = +25 °C Unless otherwise)

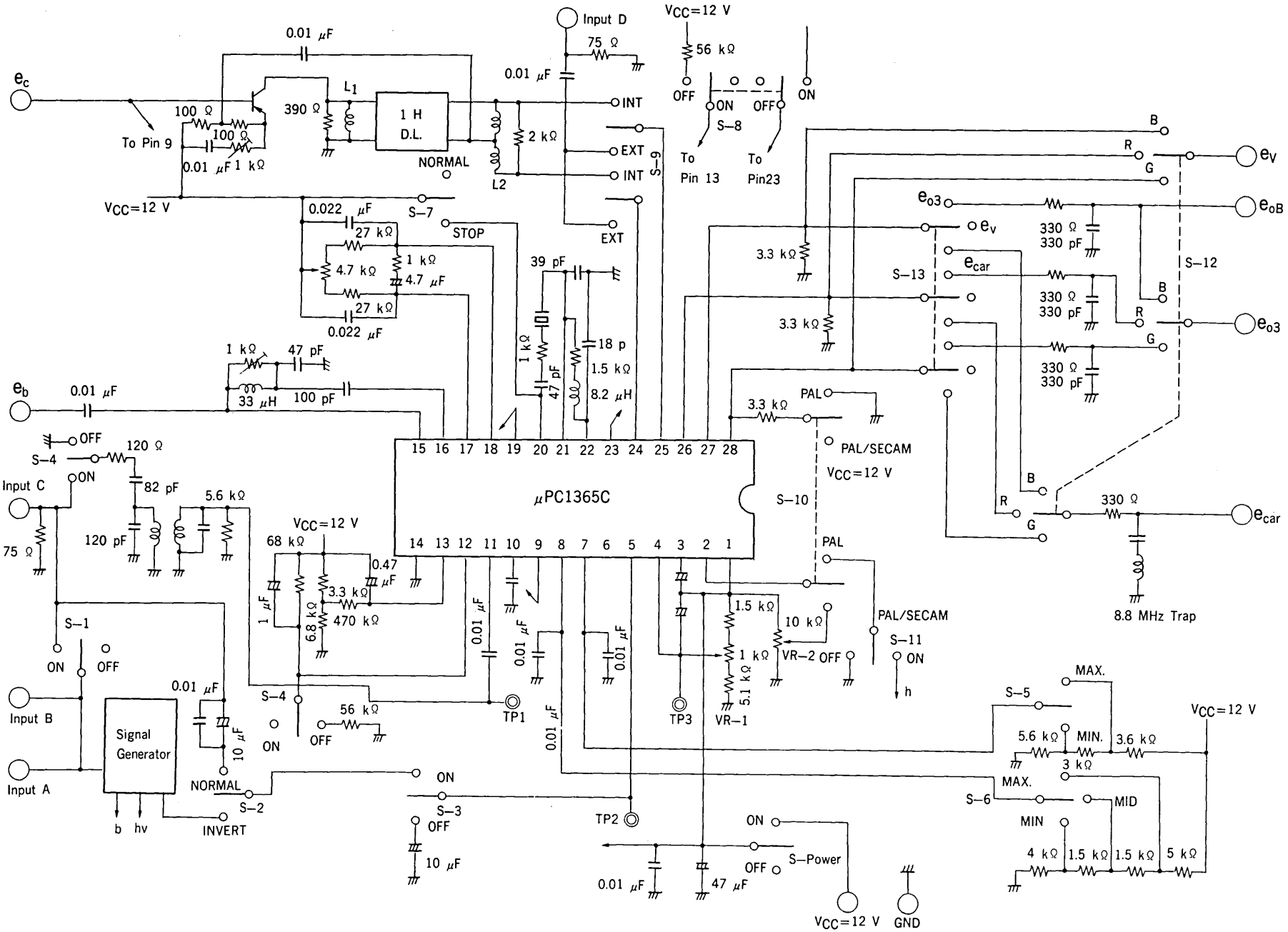
Supply Voltage	V_{CC}		15	V
Power Dissipation	Pd	(Ta = +70 °C)	750	mW
Signal Input Voltage	e_i		5	V_{p-p}
Pulse Input Voltage	e_p		±6	V
Operating Temperature	T_{opt}		-20 to + 70	°C
Storage Temperature	T_{stg}		-40 to + 125	°C

ELECTRICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted, V_{CC} = 12 V)

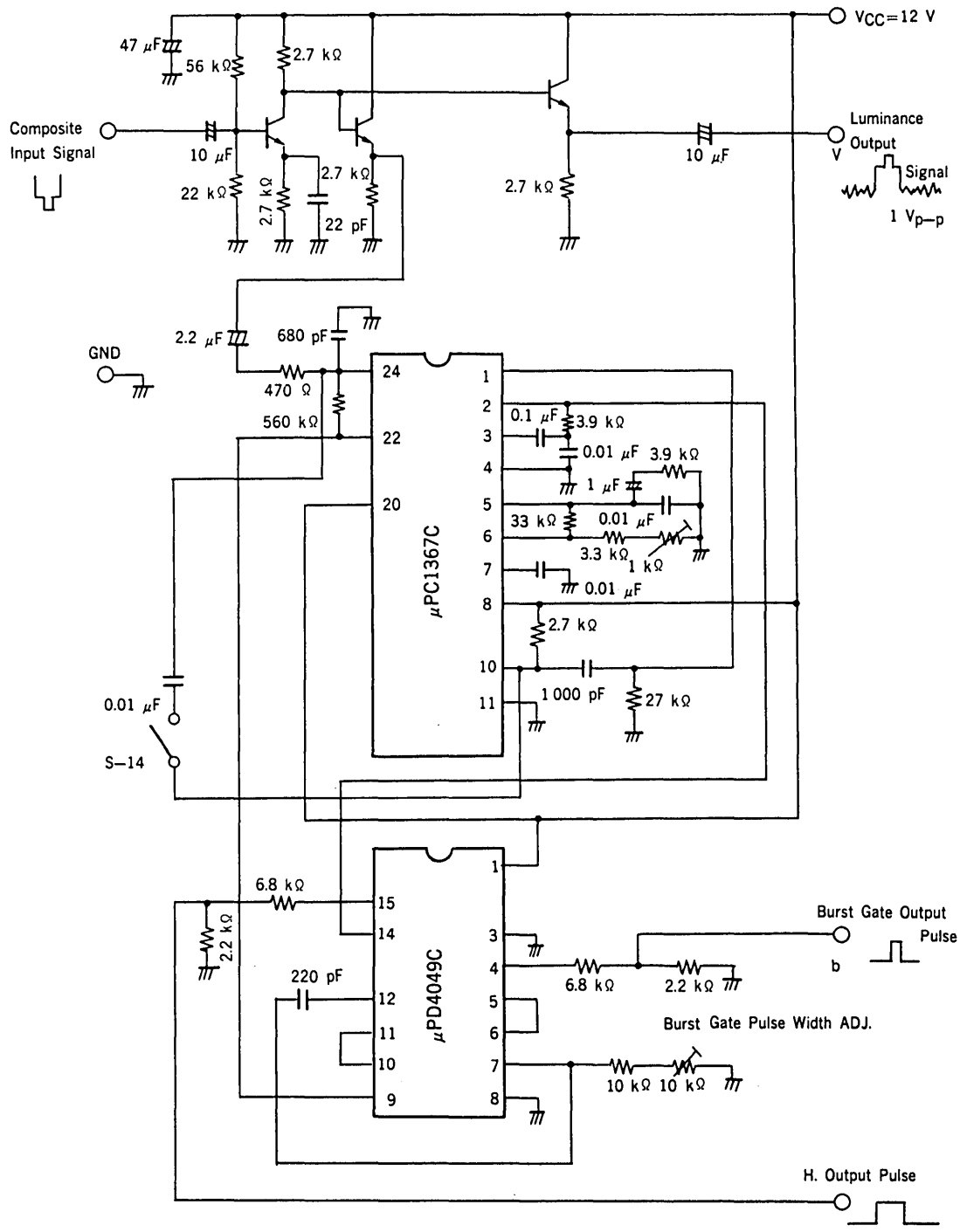
NO	CHARACTERISTIC	SYMBOL	TEST CKT	MIN.	TYP.	MAX	UNIT	TEST CONDITION
1	Burst Output Voltage	e_b	1	0.9	1.2	1.6	V_{p-p}	Input 100 mV_{p-p} Rainbow color bar signal
2	ACC Range	ACC	1	0.6	0.8	1.0	times	Input 10 mV_{p-p} Burst Output/ e_b
3	Chroma Output Voltage 1	e_{c1}	1	0.5	0.7	1.0	V_{p-p}	Input 100 mV_{p-p} Rainbow color bar signal Saturation control MAX
4	Chroma Output Voltage 2	e_{c2}	1		0.2		V_{p-p}	Input 100 mV_{p-p} Rainbow color bar signal Saturation control MID
5	Chroma Output Voltage 3	e_{c3}	1			6	mV_{p-p}	Input 100 mV_{p-p} Rainbow color bar signal Saturation control MIN
6	Killer Sensitivity	e_k	1	−34	−40	−46	dB	0 dB = Input 100 mV_{p-p} Rainbow color bar signal Killer ON Input level
7	Killer Hysterisis	e_{kh}	1	—	1	2	dB	Killer ON-OFF Input level
8	Oscillator Controlling Sensitivity	β	2	1.3	1.8	2.3	Hz/mV	Measure Vp Voltage at Burst frequency fo ± 100 Hz
9	Phase Detector Sensitivity	μ	2	20	40	60	mV/degree	Measure Vp Voltage at Burst frequency fo ± 100 Hz
10	Phase error	$\Delta\phi$	2	—	1.5	3.0	degree/100 Hz	Burst frequency fo ± 100 Hz
11	APC Pull-in frequency Range	f_p	2	±300	±500	—	Hz	Changing frequency of Burst signal
12	APC Detector Output balance Voltage	V_p	2	−100	0	+100	mV	No Input signal at Pin 16
13	B-Y Output Voltage	e_{o1}	1	1.5	2.0	2.5	V_{p-p}	Input 0.2 V_{p-p} f = 4.44 MHz 10 kHz beat Output signal
14	Ratio of R-Y to B-Y	R/B	1	0.49	0.56	0.63	times	Input 0.2 V_{p-p} f = 4.44 MHz 10 kHz beat Output signals
15	Ratio of G-Y to B-Y	G/B	1	0.30	0.34	0.38	times	Input 0.2 V_{p-p} f = 4.44 MHz 10 kHz beat Output signals
16	Relative Output Phase B-Y to R-Y	∠R	1	85	90	95	degree	Input 0.2 V_{p-p} f = 4.44 MHz
17	Relative Output Phase B-Y to G-Y	∠G	1	228	236	244	degree	Input 0.2 V_{p-p} f = 4.44 MHz
18	Maximum Color Difference Output Voltage	e_{o2}	1	4.5	5.5	—	V_{p-p}	Input 1.2 V_{p-p} f = 4.44 MHz 10 kHz beat Output signal at B-Y Output Pin
19	Output Residual Carrier level	e_{car}	1	—	—	100	mV_{p-p}	No Input signal at Pin 24 and 25
20	Overall color Difference Output Voltage at B-Y signal	e_{o3}	1	1.0	1.7	2.5	V_{p-p}	Saturation control MID Input 100 mV_{p-p} Rainbow color bar signal Contrast control MAX
21	Overall color Difference Output Variable Range by.Contrast	e_{oc}	1	15	17	19	dB	Input 100 mV_{p-p} Rainbow color bar signal Contrast control MAX/MIN
22	Luminance Gain	Av1	1	4.1	4.6	5.1	times	Input 1 V_{p-p} Color bar 100 % White signal Contrast control MAX

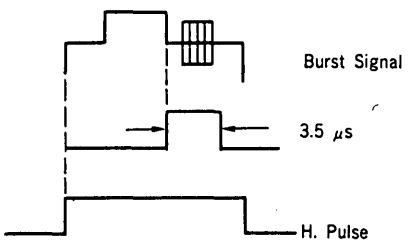
NO	CHARACTERISTIC	SYMBOL	TEST CKT	MIN.	TYP.	MAX	UNIT	TEST CONDITION
23	Relative Ratio of Luminance Gain	ΔAv1	1	–	1.0	1.1	times	Input 1 V_{p-p} Color bar 100 % White signal Contrast control MAX
24	Luminance Gain Variable Range by Contrast	e_{vc}	1	15	17	19	dB	Input 1 V_{p-p} Color bar 100 % White signal Contrast control MAX/MIN
25	Differential Gain	D.G.	1	–	–	6	%	Input 1 V_{p-p} Stair step signal RGB Output, Black level = 2 V
26	DC Restoration	T_{DC}	1	90	95	100	%	Input 1 V_{p-p} Stair step signal APL = 10 to 90 %
27	Luminance Amp Frequency Characteristic	f_v	1	4.0	5.5	–	MHz	Input 0.1 Vr.m.s. Sine wave signal, –3 dB down Pin 6 open
28	Brightness Controlling Sensitivity	BR	1	3.8	4.3	4.8	–	Quiescent Output Voltage = 2 to 5V, (V26, V27, V28) Sensitivity 3 V/ΔV4
29	Maximum R,G,B Output Voltage	E_{OM}	1	7	–	–	V	Brightness Controlling Voltage = 12 V
30	Quiescent Output Voltage	Eo	1	2.5	3.3	4.1	V	No Luminance Input signal Brightness V4 = 9 V Contrast MAX VCO operating
31	Quiecent Output Voltage Temperature Coefficient	E_{O-T}	1	–2	0	+2	mV/°C	R,G,B Output Ta = –20 to +70 °C V26 = 3.5 V at Ta = 25 °C
32	Difference Output Voltage	E_{R-G} E_{G-B} E_{B-R} E_{x-y}	1	–300	0	+300	mV	V26 = 3.5 V VCO operating
33	Difference Output Voltage Temperature Coefficient	$\Delta E_{x-y}/\Delta T$	1	–	0	60	mV	26 = 3.5 V at Ta = 25 °C Ta = –20 to +70°C
34	Supply Current	I_{CC}	3	32	43	54	mA	V_{CC} = 12 V
35	Changing Black level by Contrast	ΔEoc	1	–100	0	+100	mV	No Luminance Input signal V26 = 2 V at Contrast MAX Contrast control MAX/MIN
36	Minimum Gate Pulse Input Voltage	$V_{G\ (min)}$		–	–	2	V	Pin 19
37	Blanking Pulse Input Voltage Range	V_B		1.8	–	5	V	Pin 2
38	Minimum FF Trigger Input Voltage	$V_{FF\ (min)}$		–	–	1.5	V	Pin 23

μPC1365C TEST CIRCUIT 1

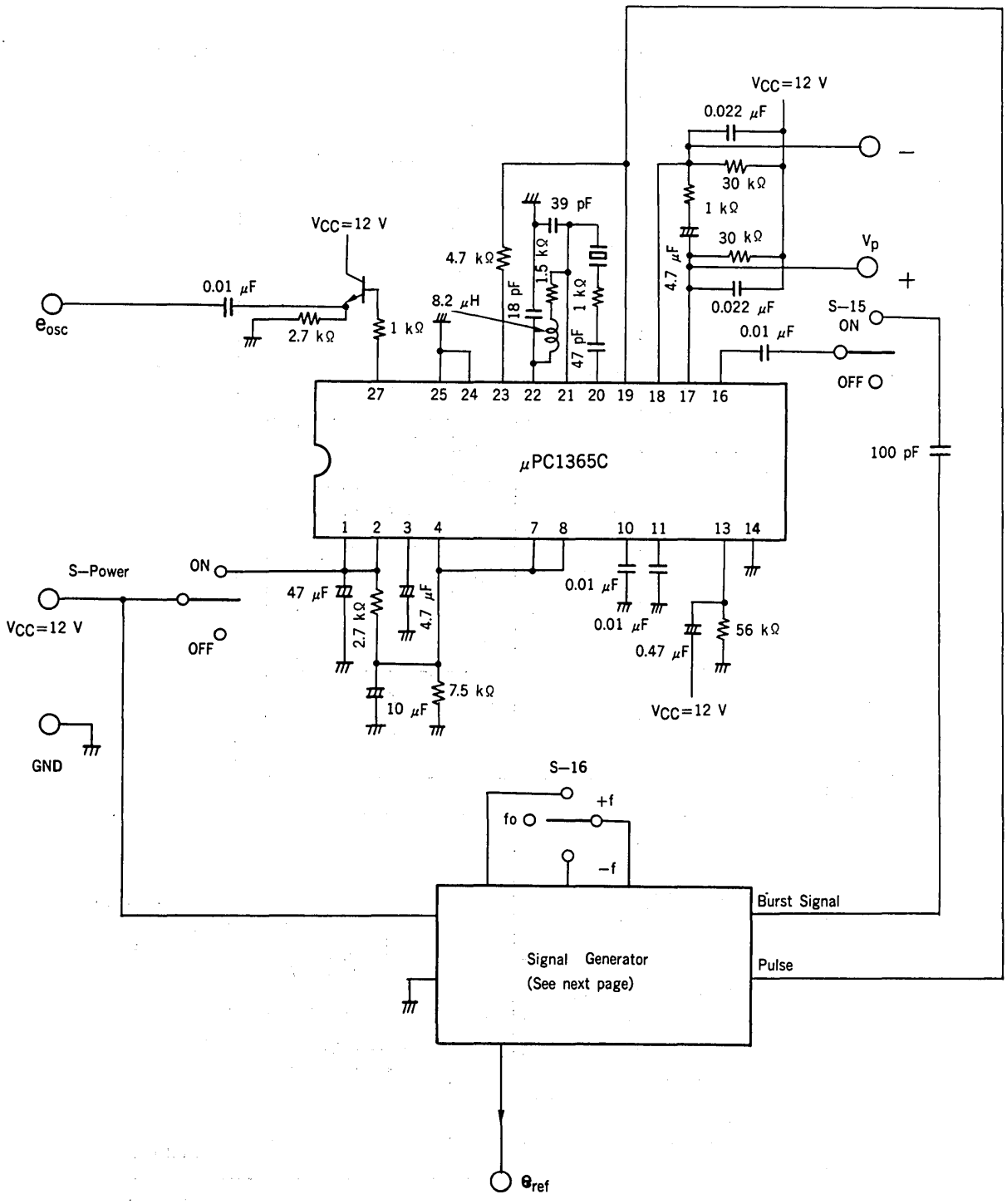


μPC1365C Signal Generator (TEST CIRCUIT 1)

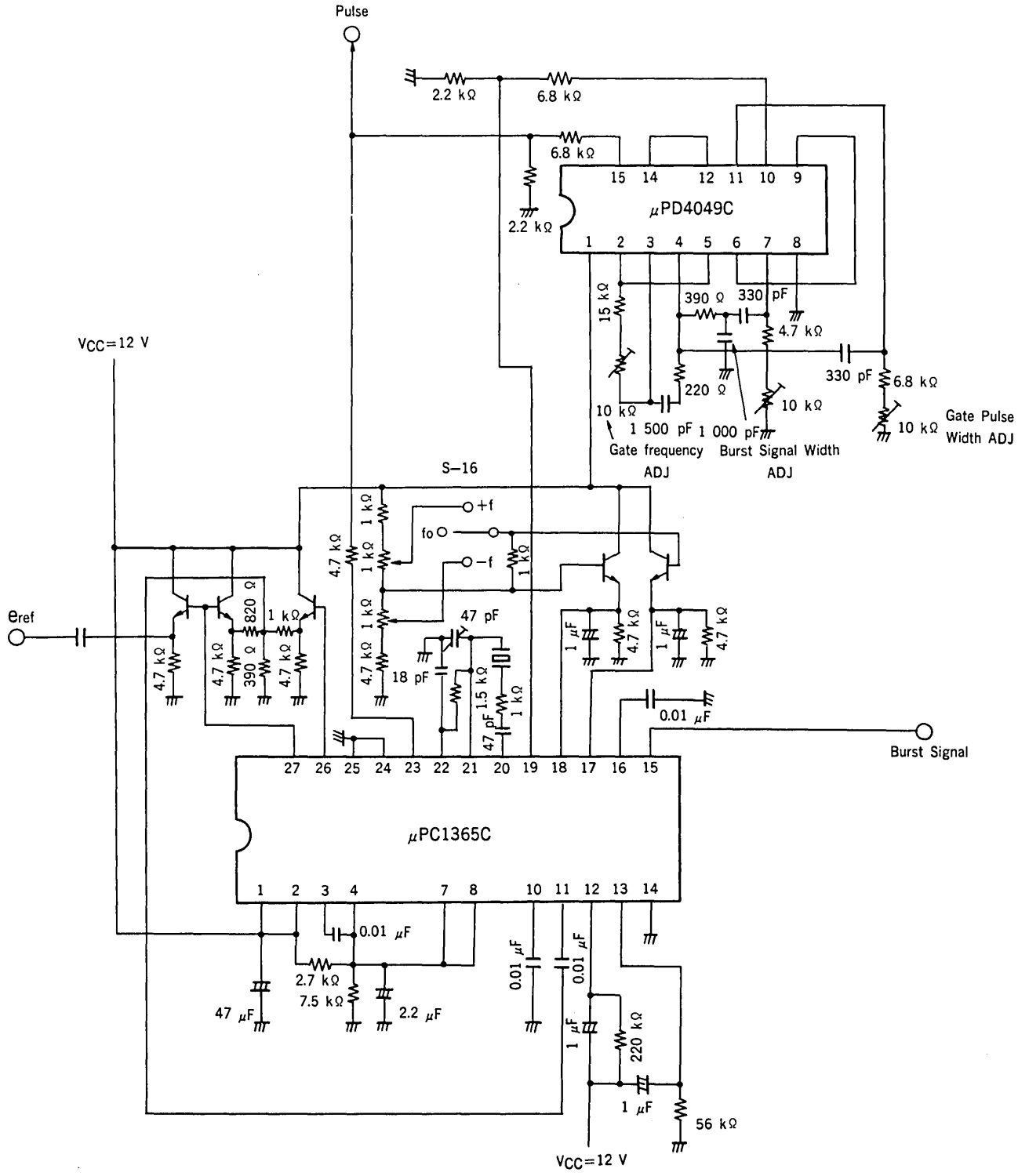




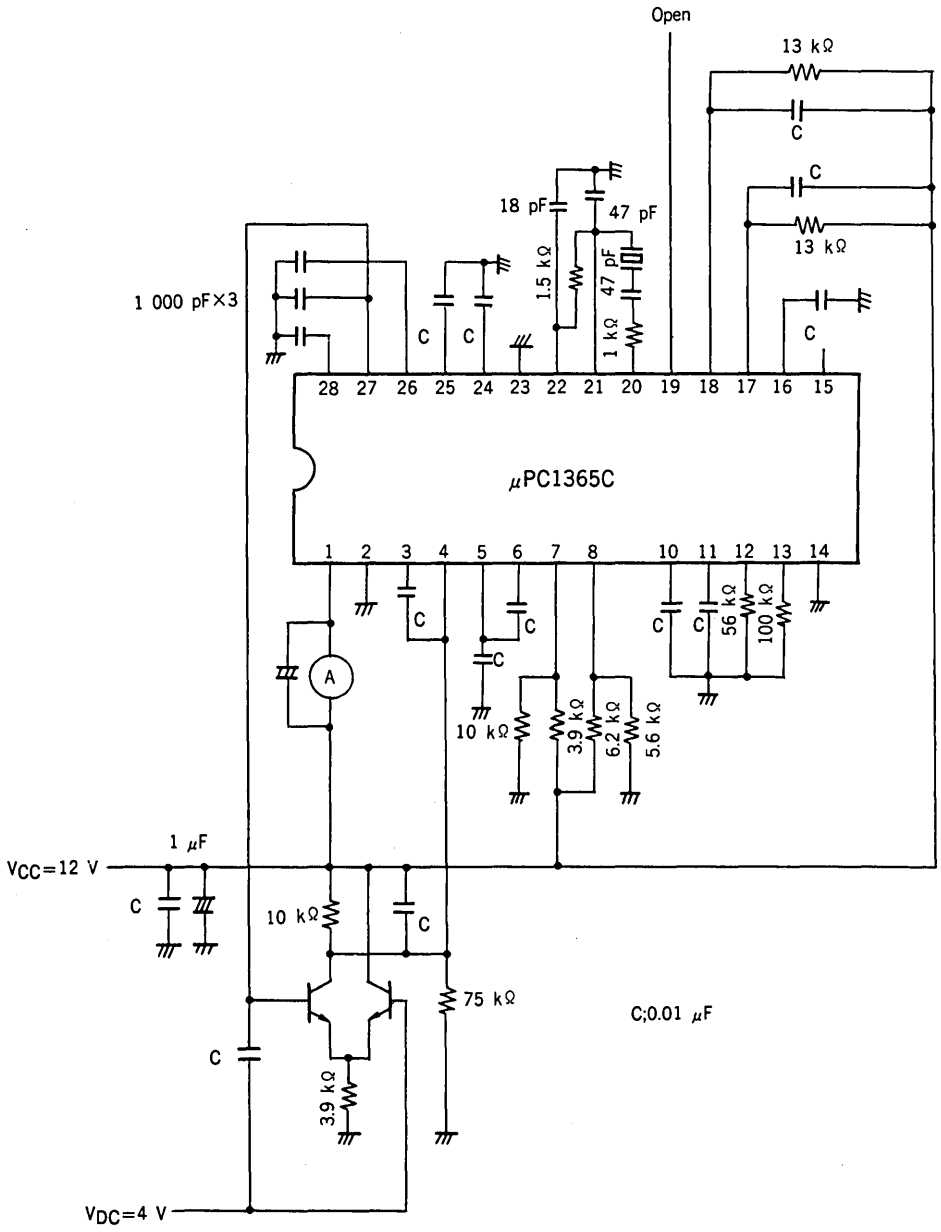
μPC1365C TEST CIRCUIT 2



μPC1365C Signal Generator (TEST CIRCUIT 2)



μPC1365C TEST Circuit 3



	e_b	ACC	e_{c1}	e_{c2}	e_{c3}	e_k, e_{kh}	e_{o1}	R/B	G/B	∠R
S-1 Input	ON	OFF	ON	ON	ON	OFF	ON	ON	ON	ON
S-2 Lum	INV	INV	INV	INV	INV	INV	INV	INV	INV	INV
S-3 Lum	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
S-4 Chro.	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF
S-5 Cont.	MAX	MAX	MAX	MAX	MAX	MAX	MAX	MAX	MAX	MAX
S-6 Satu.	MID	MID	MAX	MID	MIN	MID	MID	MID	MID	MID
S-7 VCO	NORM	NORM	NORM	NORM	NORM	NORM	NORM	NORM	NORM	NORM
S-8 FF.	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF
S-9 Dem.	INT	INT	INT	INT	INT	INT	EXT	EXT	EXT	EXT
S-10 Syst.	PAL	PAL	PAL	PAL	PAL	PAL	PAL	PAL	PAL	PAL
S-11 Blk	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
S-12 Output	B	B	B	B	B	B	B	R	G	R
S-13 Output	e_{o3}	e_{o3}	e_{o3}	e_{o3}	e_{o3}	e_{o3}	e_{o3}	e_{o3}	e_{o3}	e_{o3}
S-14	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON
VR-1	Be trimmed V26 = 3.5 V by Brightness VR (VR-1)									
VR-2										
Input	A	A = SG B – C = ATT	A	A	A	A = SG B – C = ATT	D = SG	D = SG	D = SG	D = SG
SG	Rainbow						f = 4.44 MHz			
Measure Point	e_b	e_b	e_c	e_c	e_c	e_c	e_{oB}	e_{oB}, e_{o3}	e_{oB}, e_{o3}	e_{oB}, e_{o3}
	Oscilloscope									Phase Meter
		ATT				ATT		AC Volt meter		

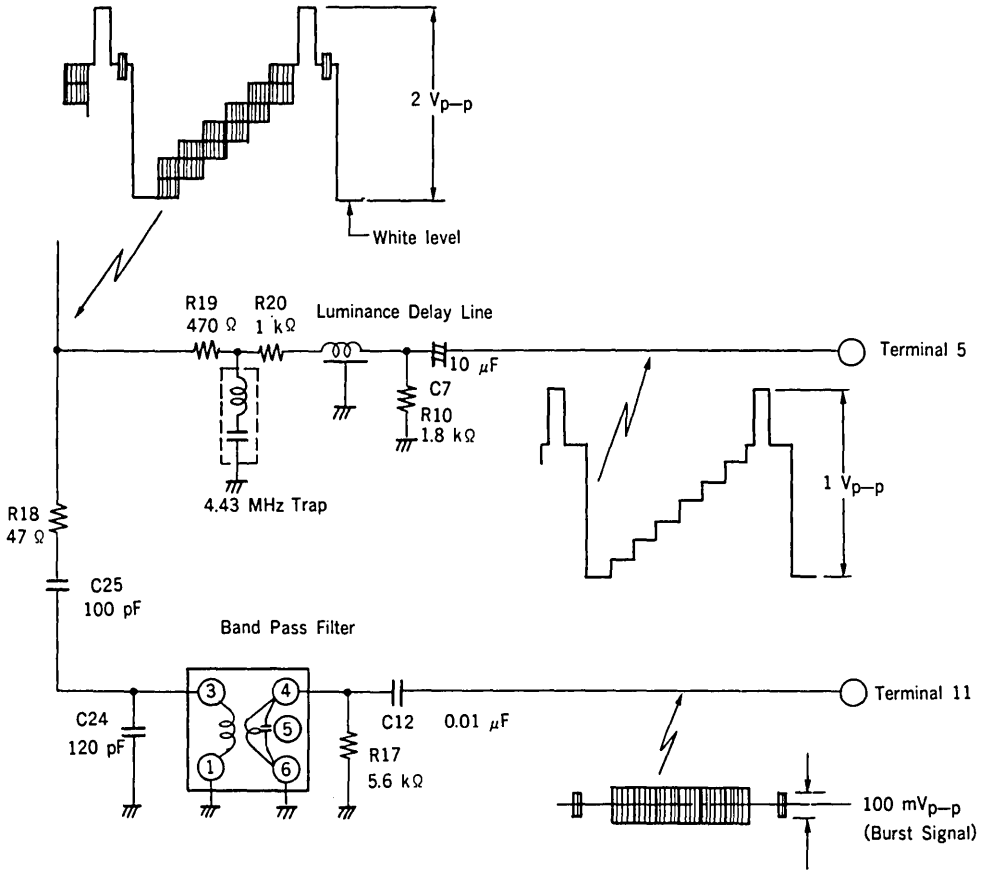
	∠ G	e_{o2}	e_{car}	e_{o3}	e_{oc}	Av1, ΔAv1	e_{vc}	DG	T_{DC}	f_v
S-1 Input	ON	ON	ON	ON	ON	ON	ON	ON	ON	OFF
S-2 Lum.	INV	INV	INV	INV	INV	INV	INV	INV	INV	NORM
S-3 Lum.	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON
S-4 Chro.	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF
S-5 Cont.	MAX	MAX	MAX	MAX	MAX, MIN	MAX	MAX, MIN	MAX	MAX	MAX
S-6 Satu.	MID	MID	MID	MID	MID	MID	MID	MID	MID	MID
S-7 VCO	NORM	NORM	NORM	NORM	NORM	STOP	STOP	STOP	STOP	STOP
S-8 FF.	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF
S-9 Dem.	EXT	EXT	EXT	INT	INT	EXT	EXT	EXT	EXT	EXT
S-10 Syst.	PAL	PAL	PAL	PAL	PAL	PAL	PAL	PAL	PAL	PAL
S-11 Blk	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
S-12 Output	G	B	BRG	B	B	BRG	B	BRG	B	BRG
S-13 Output	e_{o3}	e_{o3}	e_{o3}	e_{o3}	e_{o3}	e_v	e_v	e_v	e_v	e_v
S-14	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON
VR-1	Be trimmed V26 = 3.5 V by Brightness VR (VR-1)					Be trimmed V26 = 2 V by Brightness VR (VR-1)				V26 = 3.5 V
VR-2										
Input	D = SG	D = SG	–	A	A	A	A	A	A	C = SG
SG	f = 4.44 MHz		–	Rainbow		Video SG 100 % White		Stair Step		SG = CW
Measure Point	e_{oB}, e_{o3}	e_{oB}	e_{car}	e_{o3}	e_{o3}	e_v	e_v	e_v	e_v	e_v
	Phase Meter	Oscilloscope						Vector scope	Oscillo-scope	RF Volt meter

	BR	E_{oM}	E_o, $E_{o\text{-}T}$	$*\frac{E_{x\text{-}y}}{\Delta E_{x\text{-}y}/\Delta T}$	ΔE_{oc}	$V_{G\ (min)}$	V_B	V_{FF}
S-1 Input	ON	ON	ON	ON	ON			
S-2 Lum.	INV	INV	INV	INV	INV			
S-3 Lum.	OFF	OFF	OFF	OFF	OFF			
S-4 Chro.	OFF	OFF	OFF	OFF	OFF			
S-5 Cont.	MAX	MAX	MAX	MAX	MAX, MIN			
S-6 Satu.	MID	MID	MID	MID	MID			
S-7 VCO	NORM	NORM	NORM	NORM	NORM			
S-8 FF.	OFF	OFF	OFF	OFF	OFF			
S-9 Dem.	EXT	EXT	EXT	EXT	EXT			
S-10 Syst.	PAL	PAL	PAL	PAL	PAL	PAL	PAL	PAL
S-11 Blk	OFF	OFF	OFF	OFF	OFF			
S-12 Output	BRG	BRG	BRG	RG	B			
S-13 Output	e_{o3}	e_{o3}	e_{o3}	e_{o3}	e_{o3}			
S-14	ON	ON	ON	ON	ON			
VR-1	See TEST Condition	TP = V_{CC}	TP = 9 V	V26 = 3.5 V	V 26 = 2 V			
VR-2								
Input								
SG								
Measure Point	E_{o3}	e_{o3}	e_{o3}	e_{o3}, e_{ov}	e_{o3}			
	DC Voltmeter							

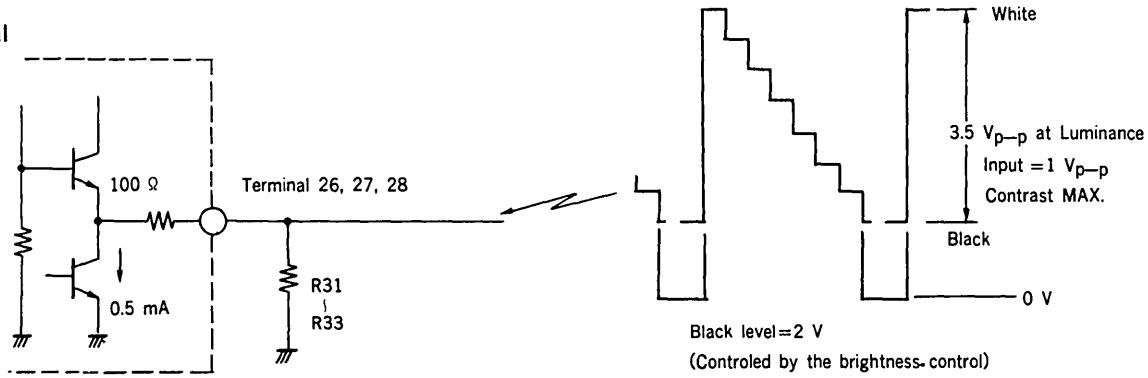
	β	μ	$\Delta\phi$	f_p	Vp
S-15 fo ± f	ON	ON	ON	OFF ON ON OFF	OFF
S-16 Burst	+f (100 Hz) −f (100 Hz)			+f (300 Hz) −f (300 Hz)	f_o
Measure Point	Vp e_{ref}	Vp e_{ref}, e_{osc}	e_{ref}, e_{osc}	e_{ref}	Vp
	f.Counter DC Voltmeter	Phase Meter f.Counter DC Voltmeter	Phase Meter f.Counter	f.Counter	DC Voltmeter

μPC1365C Input and Output signals

Luminance Input Signal



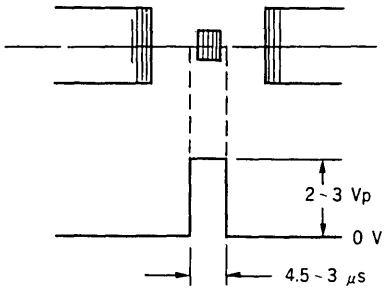
Output Signal

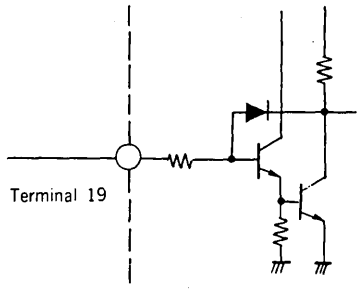


μPC1365C Input Pluse

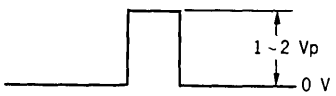
Burst Gate Pulse

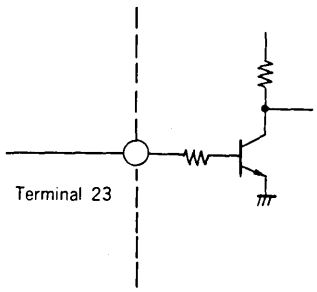
Burst signal = 100 ~ 200 mVp-p
at Terminal 11



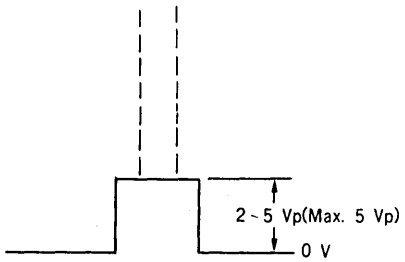


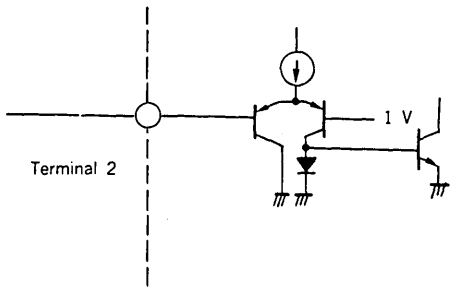
Line Pulse



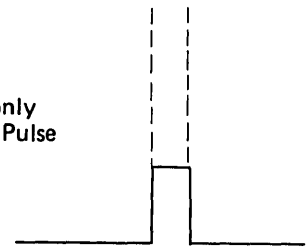


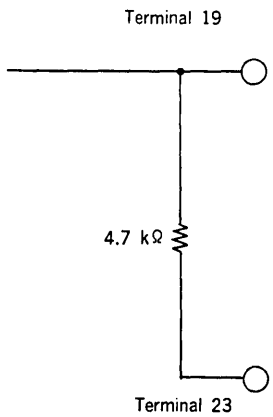
Blanking Pulse
(Line Pulse and
Field Pulse)





In case of commonly
using of Input Pulse

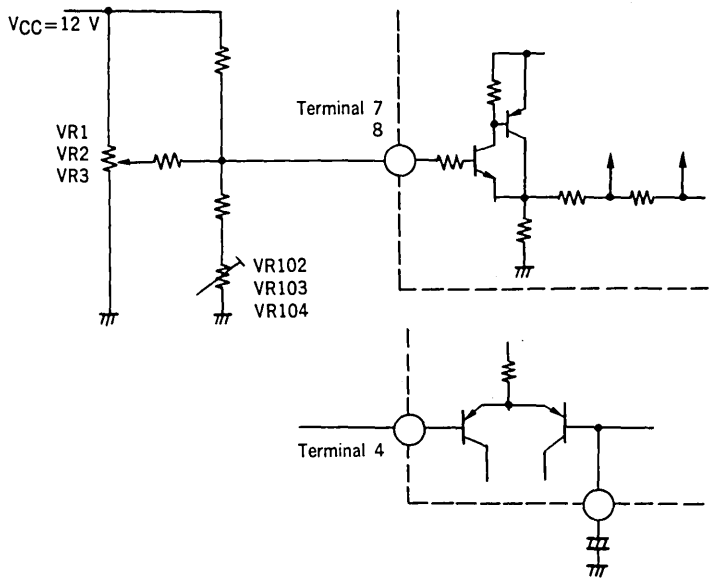




μPC1365C

*Color, Contrast and Brightness controlling circuit

VR1 ; Brightness Control
VR102 ; Sub Brightness
VR2 ; Contrast Control
VR103 ; Sub Contrast
VR3 ; Color Control
VR104 ; Sub Color



V7 (Contrast) 5.5 to 7.0 to 8.5 V
V8 (Color) 4.0 to 5.5 to 7.0 V
V2 (Brightness) 8.2 to 8.7 to 9.2 V

*Color Killer Setting VR105

*APC Setting

Method; 1; Connect Resistor (100 kΩ) between the Terminal 13 and GND as shown Fig. 1 (Killer OFF)

2; Connect Capacitor (0.01 μF) between the Terminal 16 and GND as shown Fig. 2 (Burst Input OFF)

3; Trim 4.433 618 MHz by using VR107

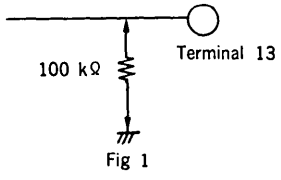


Fig 1

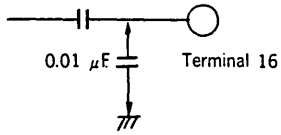
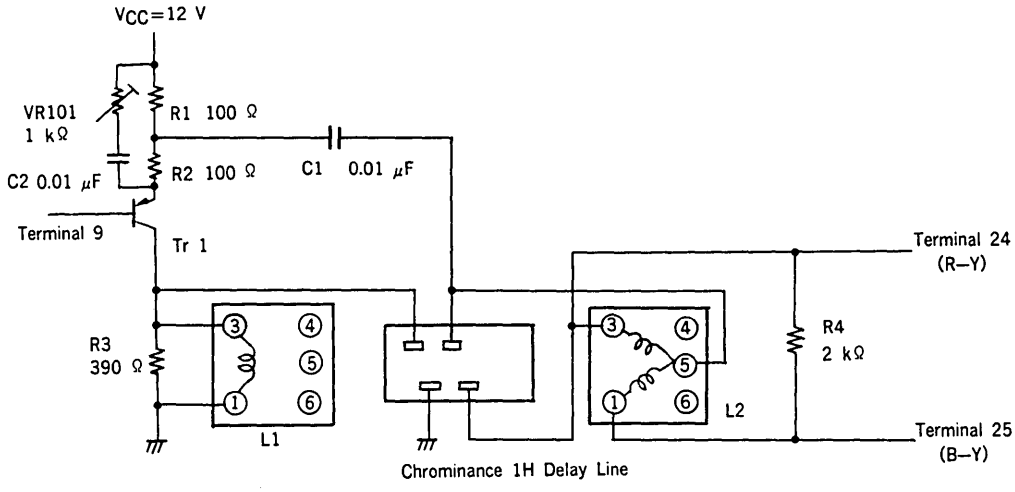


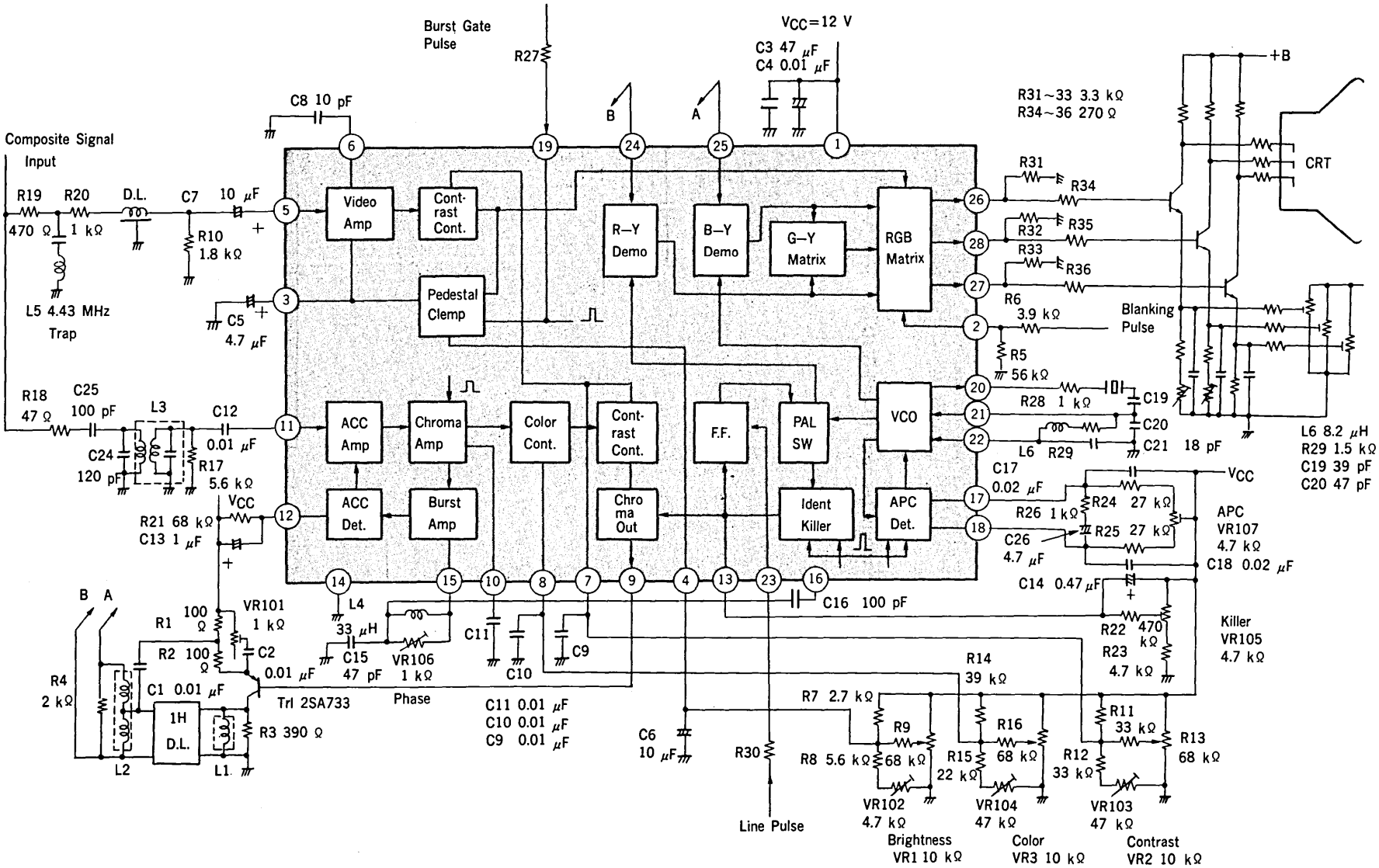
Fig 2

*1H Delay Line Circuit

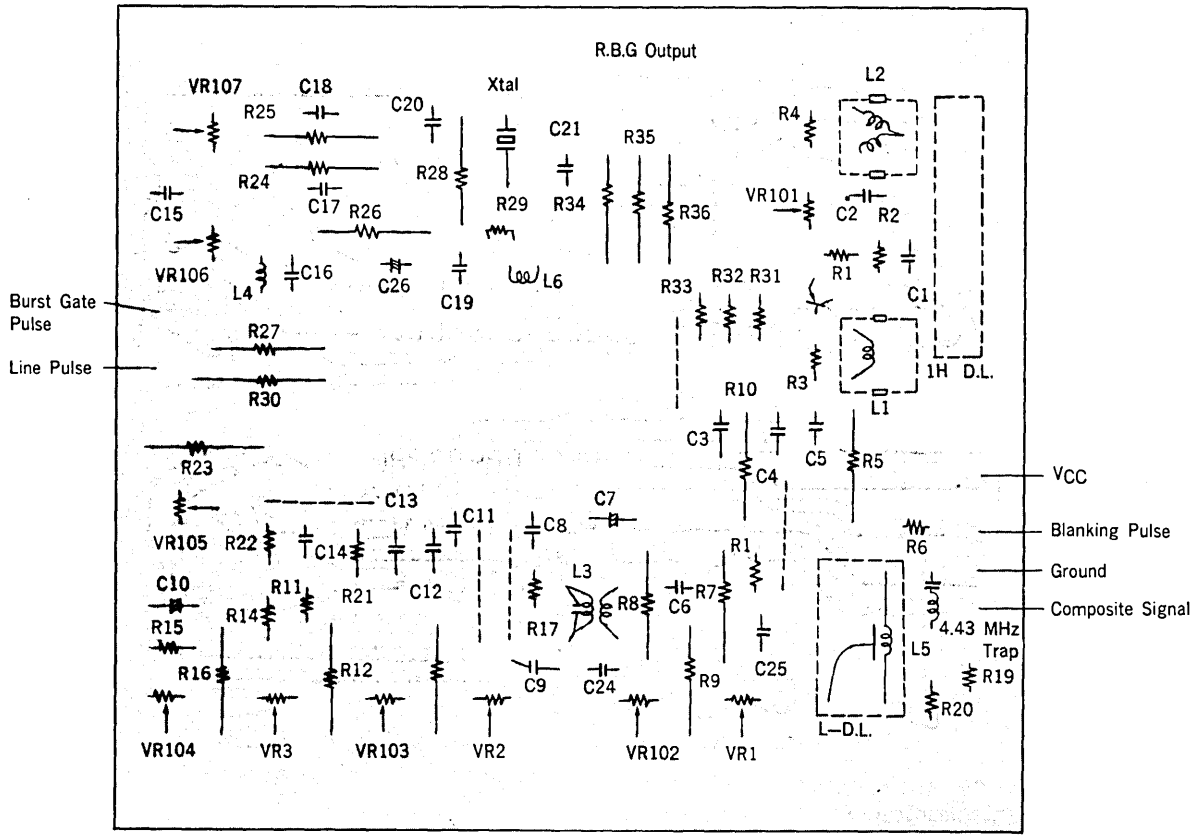


L1 ; Pre Chrominance Delay Line Terminating Coil
L2, VR101 ; Delay Phase and Amplitude Adjustment
VR106 ; Sub carrier Phase Adjustment

The Block Diagram and External Components for μPC1365C



Printed Circuit Board Pattern (Bottom View)



μPC1365C Table of the external components

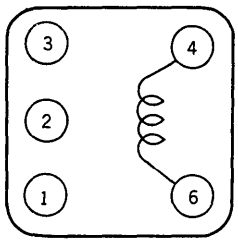
Symbol	Value
R1	100 Ω
R2	100 Ω
R3	390 Ω
R4	2 kΩ
R5	(56 kΩ)
R6	(3.9 kΩ)
R7	2.7 kΩ
R8	5.6 kΩ
R9	68 kΩ
R10	1.8 kΩ
R11	33 kΩ
R12	33 kΩ
R13	68 kΩ
R14	39 kΩ
R15	22 kΩ
R16	68 kΩ
R17	5.6 kΩ
R18	47 Ω
R19	470 Ω
R20	1 kΩ
R21	68 kΩ
R22	470 kΩ
R23	4.7 kΩ
R24	27 kΩ
R25	27 kΩ
R26	1 kΩ
R27	(1.2 kΩ)
R28	1 kΩ
R29	1.5 kΩ
R30	(1.2 kΩ)
R31	3.3 kΩ
R32	3.3 kΩ
R33	3.3 kΩ
R34	270 Ω
R35	270 Ω
R36	270 Ω

Symbol	Value
C1	0.01 μF
C2	0.01 μF
C3	47 μF
C4	0.01 μF
C5	4.7 μF
C6	10 μF
C7	10 μF
C8	10 pF
C9	0.01 μF
C10	0.01 μF
C11	0.01 μF
C12	0.01 μF
C13	1 μF
C14	0.47 μF
C15	47 pF
C16	100 pF
C17	0.022 μF
C18	0.022 μF
C19	39 pF(Xtal C_L=16 pF), 68 pF(Xtal C_L=20 pF)
C20	47 pF
C21	18 pF
C22	—
C23	—
C24	120 pF
C25	100 pF
C26	4.7 μF

Symbol	Value
VR–1	10 kΩ Brightness
VR–2	10 kΩ Contrast
VR–3	10 kΩ Color Saturation
VR101	1 kΩ D'. Level
VR102	4.7 kΩ Sub Brightness
VR103	47 kΩ Sub Contrast
VR104	47 kΩ Sub Color Saturation
VR105	4.7 kΩ Killer Adj
VR106	1 kΩ Phase Adj
VR107	4.7 kΩ APC Adj
L1	D.L. Matching Coil Type No TKRNS 24984NK (Toko Corp.)
L2	D.L. Matching Coil Type No TKRNS 24985VN (Toko Corp.)
L3	Band Pass Filter Type No 163NEF1148WWJ (Toko Corp.)
L4	33 μH
L5	4.43 MHz Trap Type No LCS2H1H-102 (TDK Corp.)
L6	8.2 μH
Tr1	2SA733 (NEC)
Xtal	4.43 MHz C_L=16 pF or 20 pF
L-D.L.	Luminance Delay Line Type No CTS-1804C (Showa Densei Corp.)
1 H D.L.	1 H Delay Line Type No EFD EN (Matsushita Corp.)

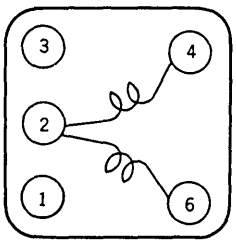
1 H Delay Line Matching Coil Specification

L1 Input Coil
(PAL)



Type No. TKRNS – 24984NK
Product TOKO Corp.
f_o ; 4.43 MHz
6 –4 ; 18 T
Cout ; 330 pF (4 –6)
Qu ; 59 ± 20 %
Wire Material ; 0.1 / UEW

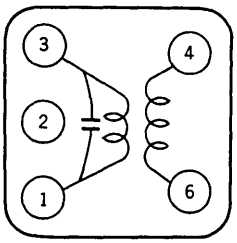
L2 Output Coil



Type No. TKRNS – 24985VN
Product TOKO Corp.
f_o ; 4.43 MHz
4 –2 ; 18 T
2 –6 ; 18 T
Cout ; 75 pF (4 –6)
Qu ; 44 ± 20 %
Wire Material ; 0.1 / 2UEW

Chrominance Input Coil Specification

L3 Input Coil
(PAL)



Type No. 163NEF – 1148WWJ
Product TOKO Corp.
f_o ; 4.43 MHz
6 –4 ; 35 1/4 T
3 –1 ; 76 T
Cout ; PH 47 pF
Wire Material ; 0.1 / UEW

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1384C

PAL CHROMINANCE AND LUMINANCE PROCESSOR
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

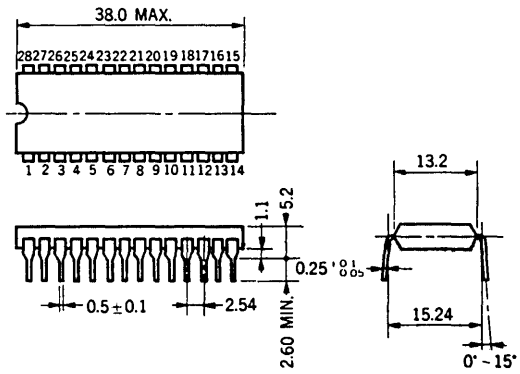
DESCRIPTION

μPC1384C is a luminance and chrominance stage LSI for PAL system TV sets. It contains luminance amplifier, chroma IF amplifier, sub-carrier oscillator, PAL switching circuit, chroma demodulator, matrix circuit, and the other necessary additions. It puts out R,G,B primary colors. This LSI restores 75 % of the DC level. And it is easy to adapt remote control system to "BRIGHTNESS", "CONTRAST", and "COLOR SATURATION", as the control terminals are designed to high impedance.

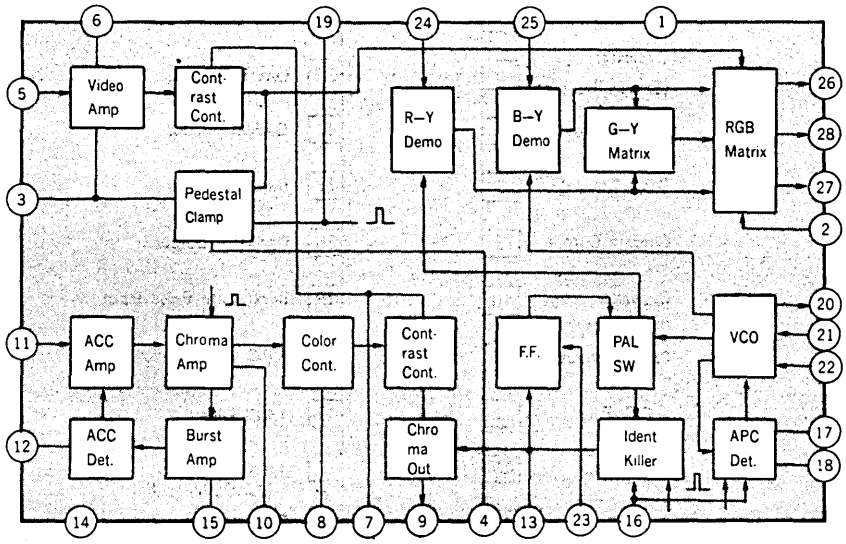
FEATURES

- This LSI has built-in function for PAL-SECAM dual system.
  1) Two IC's construction by NEC's SECAM IC μPC1364C2.
  2) Only one 1-H delay line is required for dual system.
  3) Automatically switchable function for PAL/SECAM signals.
- The black level moved by the contrast control circuit.
- Luster is provided even in a vacant channel by the 75 % DC restoration.
- This LSI can process both of the chrominance and luminance signals.
- Due to DC control method for color, contrast, and brightness control, the wiring is rather easy and the expansion to remote control receiver are also rather easy.
- The contrast control can automatically adjust the levels of chroma and contrast-luminance signal under the relation that the normal picture is always kept.
- The output terminals of demodulated chroma signals and all input circuits are protected by the surge protection diode.

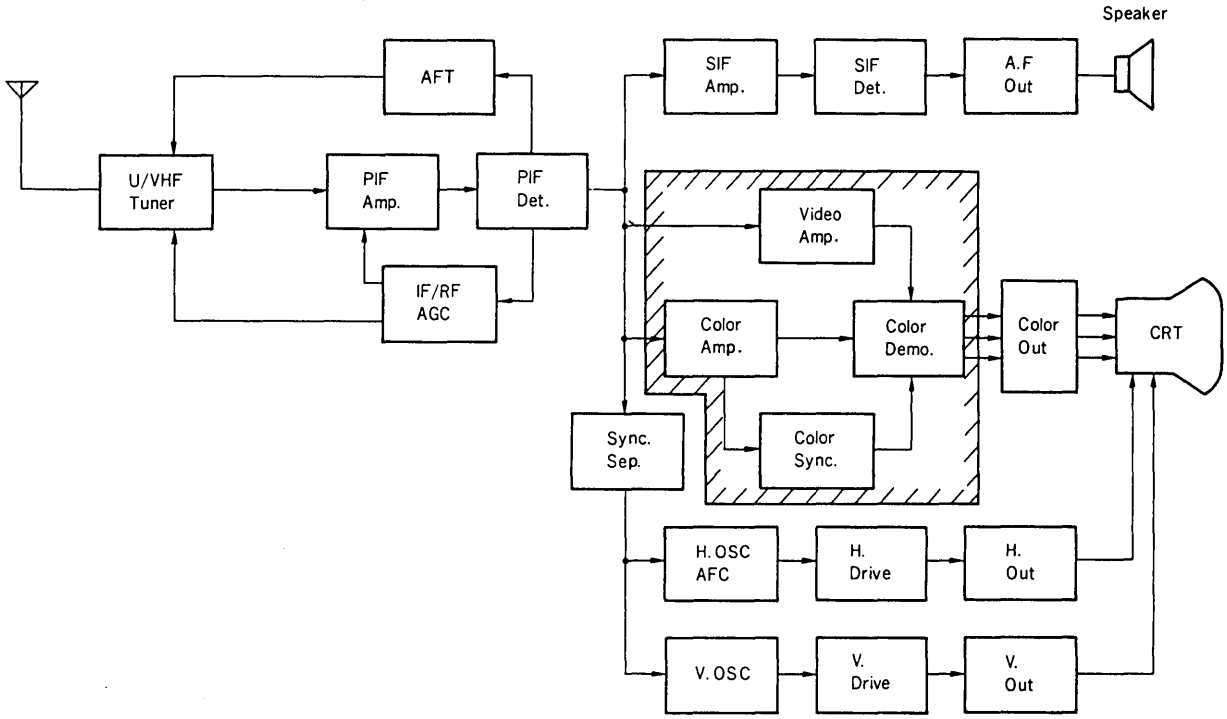
PACKAGE DIMENSIONS in millimeters



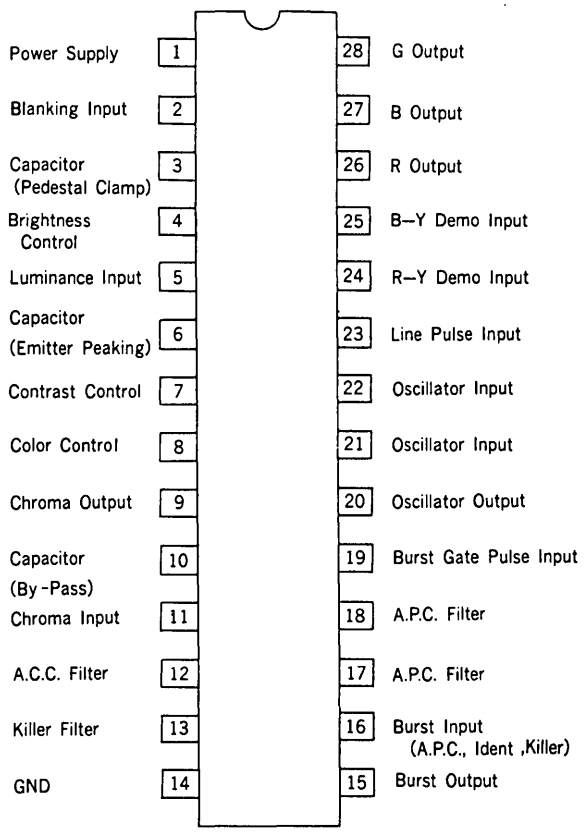
IC BLOCK DIAGRAM



TV BLOCK DIAGRAM



PIN CONNECTION (Top View)



μPC1384C Standard Using Conditions

Supply Voltage	12	V
Chrominance Input Signal (Burst Signal Level)	100	m V_{p-p}
Luminance Input Signal	1	V_{p-p}
Gate Pulse Input Level	3	V_p
H. Pulse Input Level	3	V_p
Blanking Pulse Input Level	3	V_p
Demodulator Chrominance Input Signal	0.2	V_{p-p}
R,G,B Output Voltage (Black Level)	2.0	V
Color Saturation Controlling Voltage	0 to 12	V
Contrast Controlling Voltage	0 to 12	V
Brightness Controlling Voltage	0 to 12	V

ABSOLUTE MAXIMUM RATINGS (Ta = +25 °C Unless otherwise)

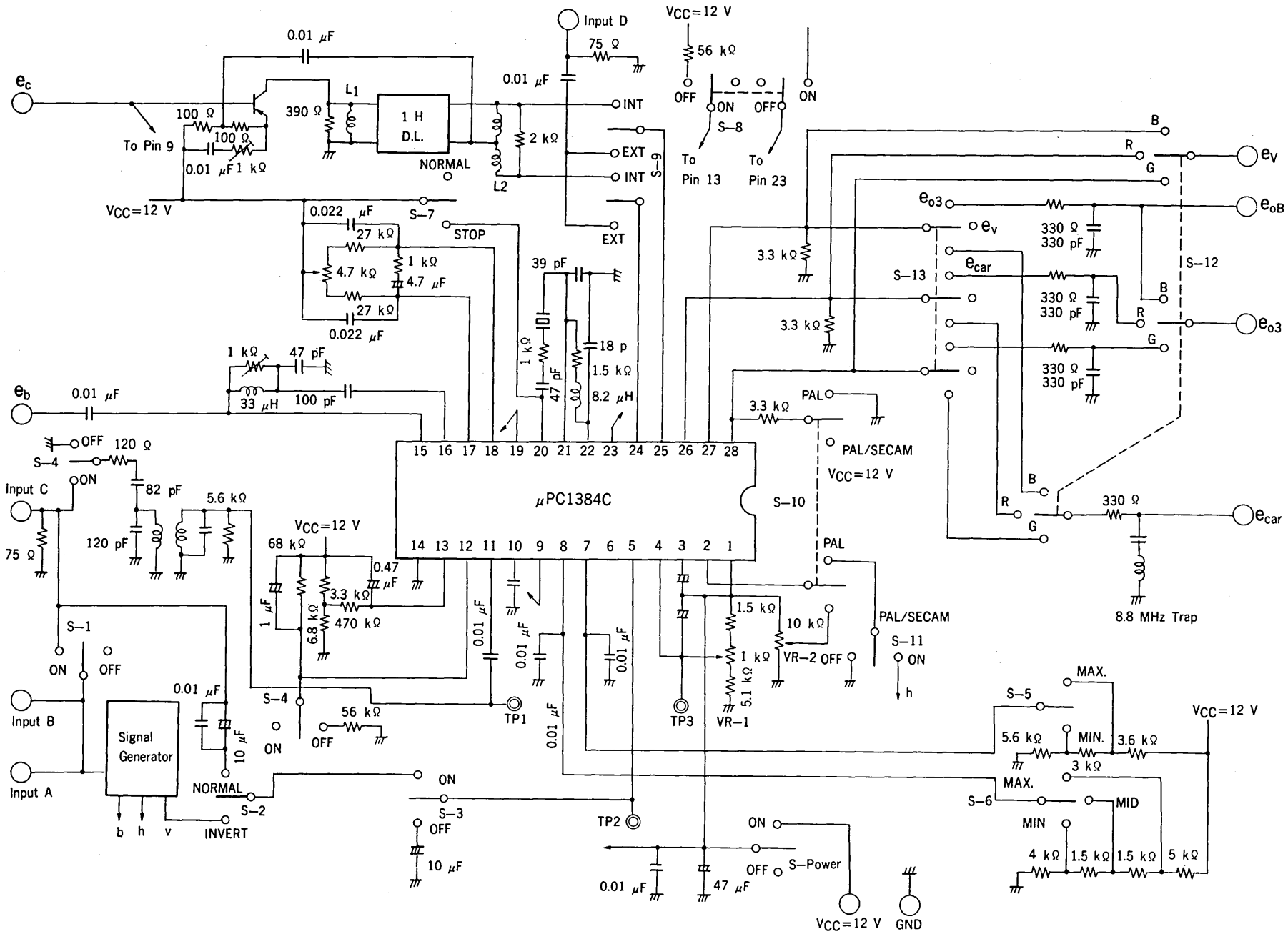
Supply Voltage	V_{CC}		15	V
Power Dissipation	Pd	(Ta = +70 ° C)	750	mW
Signal Input Voltage	e_i		5	V_{p-p}
Pulse Input Voltage	e_p		±6	V
Operating Temperature	T_{opt}		-20 to +70	°C
Storage Temperature	T_{stg}		-40 to +125	°C

ELECTRICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted, V_{CC} = 12 V)

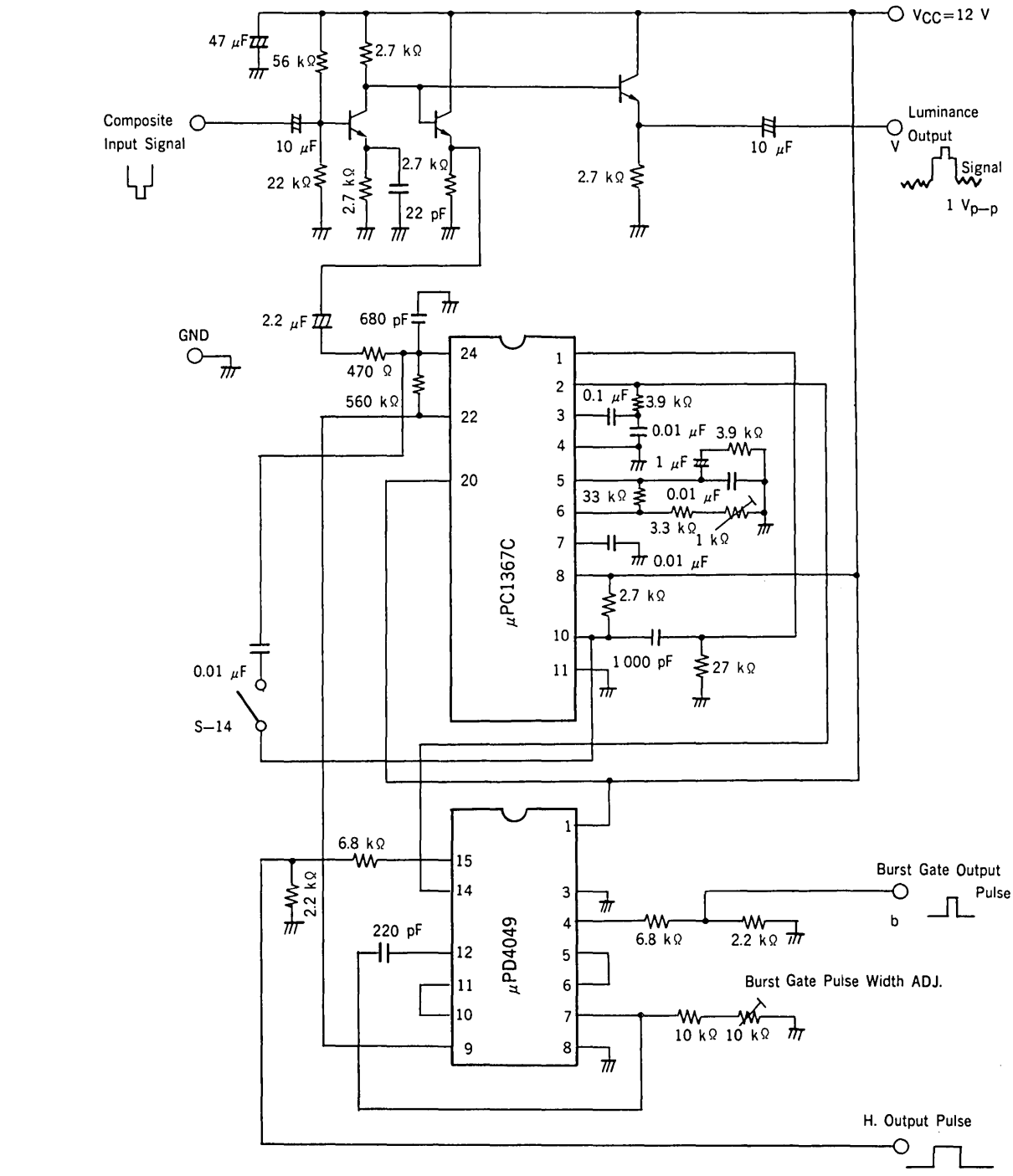
NO	CHARACTERISTIC	SYMBOL	TEST CKT	MIN.	TYP.	MAX	UNIT	TEST CONDITION
1	Burst Output Voltage	e_b	1	0.9	1.2	1.6	V_{p-p}	Input 100 mV_{p-p} Rainbow color bar signal
2	ACC Range	ACC	1	0.6	0.8	1.0	times	Input 10 mV_{p-p} Burst Output/e_b
3	Chroma Output Voltage 1	e_{c1}	1	0.5	0.7	1.0	V_{p-p}	Input 100 mV_{p-p} Rainbow color bar signal Saturation control MAX
4	Chroma Output Voltage 2	e_{c2}	1		0.2		V_{p-p}	Input 100 mV_{p-p} Rainbow color bar signal Saturation control MID
5	Chroma Output Voltage 3	e_{c3}	1			6	mV_{p-p}	Input 100 mV_{p-p} Rainbow color bar signal Saturation control MIN
6	Killer Sensitivity	e_k	1	−34	−40	−46	dB	0 dB = Input 100 mV_{p-p} Rainbow color bar signal Killer ON Input level
7	Killer Hysterisis	e_{kh}	1	—	1	2	dB	Killer ON-OFF Input level
8	Oscillator Controlling Sensitivity	β	2	1.3	1.8	2.3	Hz/mV	Measure V_p Voltage at Burst frequency fo ± 100 Hz
9	Phase Detector Sensitivity	μ	2	20	40	60	mV/degree	Measure V_p Voltage at Burst frequency fo ± 100 Hz
10	Phase error	$\Delta\phi$	2	—	1.5	3.0	degree/100 Hz	Burst frequency fo ± 100 Hz
11	APC Pull-in frequency Range	f_p	2	±300	±500	—	Hz	Changing frequency of Burst signal
12	APC Detector Output balance Voltage	Vp	2	−100	0	+100	mV	No Input signal at Pin 16
13	B-Y Output Voltage	e_{o1}	1	1.5	2.0	2.5	V_{p-p}	Input 0.2 V_{p-p} f = 4.44 MHz 10 kHz beat Output signal
14	Ratio of R-Y to B-Y	R/B	1	0.71	0.78	0.85	times	Input 0.2 V_{p-p} f = 4.44 MHz 10 kHz beat Output signals
15	Ratio of G-Y to B-Y	G/B	1	0.30	0.34	0.38	times	Input 0.2 V_{p-p} f = 4.44 MHz 10 kHz beat Output signals
16	Relative Output Phase B-Y to R-Y	∠ R	1	85	90	95	degree	Input 0.2 V_{p-p} f = 4.44 MHz
17	Relative Output Phase B-Y to G-Y	∠ G	1	228	236	244	degree	Input 0.2 V_{p-p}
18	Maximum Color Difference Output Voltage	e_{o2}	1	4.5	5.5	—	V_{p-p}	Input 1.2 V_{p-p} f = 4.44 MHz 10 kHz beat Output signal at B-Y Output Pin
19	Output Residual Carrier level	e_{car}	1	—	—	100	mVp-p	No Input signal at Pin 24 and 25
20	Overall color Difference Output Voltage at B-Y signal	e_{o3}	1	1.0	1.7	2.5	V_{p-p}	Saturation control MID Input 100 mV_{p-p} Rainbow color bar signal Contrast control MAX
21	Overall color Difference Output Variable Range by Contrast	e_{oc}	1	15	17	19	dB	Input 100 mV_{p-p} Rainbow color bar signal Contrast control MAX/MIN
22	Luminance Gain	Av1	1	4.1	4.6	5.1	times	Input 1 V_{p-p} Color bar 100 % White signal Contrast control MAX

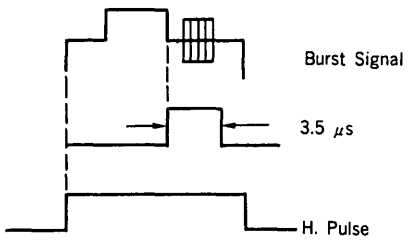
NO	CHARACTERISTIC	SYMBOL	TEST CKT	MIN.	TYP.	MAX	UNIT	TEST CONDITION
23	Relative Ratio of Luminance Gain	$\Delta Av1$	1	–	1.0	1.1	times	Input 1 V_{p-p} Color bar 100 % White signal Contrast control MAX
24	Luminance Gain Variable Range by Contrast	e_{vc}	1	15	17	19	dB	Input 1 V_{p-p} Color bar 100 % White signal Contrast control MAX/MIN
25	Differential Gain	D.G.	1	–	–	6	%	Input 1 V_{p-p} Stair step signal RGB Output, Black level = 2 V
26	DC Restoration	T_{DC}	1	68	75	82	%	Input 1 V_{p-p} Stair step signal APL = 10 to 90 %
27	Luminance Amp Frequency Characteristic	f_V	1	4.0	5.5	–	MHz	Input 0.1 Vr.m.s. Sine wave signal, –3 dB down Pin 6 open
28	Brightness Controlling Sensitivity	BR	1	3.8	4.3	4.8	–	Quiescent Output Voltage = 2 to 5 V, (V26, V27, V28) Sensitivity 3 V/ΔV4
29	Maximum R,G,B Output Voltage	E_{OM}	1	7	–	–	V	Brightness Controlling Voltage = 12 V
30	Quiescent Output Voltage	Eo	1	2.7	3.5	4.3	V	No Luminance Input signal Brightness V4 = 9 V Contrast MAX VCO operating
31	Quiecent Output Voltage Temperature Coefficient	E_{O-T}	1	–2	0	+2	mV/°C	R,G,B Output Ta = –20 to +70°C V26 = 3.5 V at Ta = 25 °C
32	Difference Output Voltage	E_{R-G} E_{G-B} E_{B-R} E_{x-y}	1	–300	0	+300	mV	V26 = 3.5 V VCO operating
33	Difference Output Voltage Temperature Coefficient	$\Delta E_{x-y}/\Delta T$	1	–	0	60	mV	V26 = 3.5 V at Ta = 25 °C Ta = –20 to +70°C
34	Supply Current	I_{CC}	3	32	43	54	mA	V_{CC} = 12 V
35	Changing Black level by Contrast	ΔEoc	1	–100	0	+100	mV	No Luminance Input signal V26 = 2 V at Contrast MAX Contrast control MAX/MIN
36	Minimum Gate Pulse Input Voltage	$V_{G\ (min)}$		–	–	2	V	Pin 19
37	Blanking Pulse Input Voltage Range	V_B		1.8	–	5	V	Pin 2
38	Minimum FF Trigger Input Voltage	$V_{FF\ (min)}$		–	–	1.5	V	Pin 23

μPC1384C TEST CIRCUIT 1

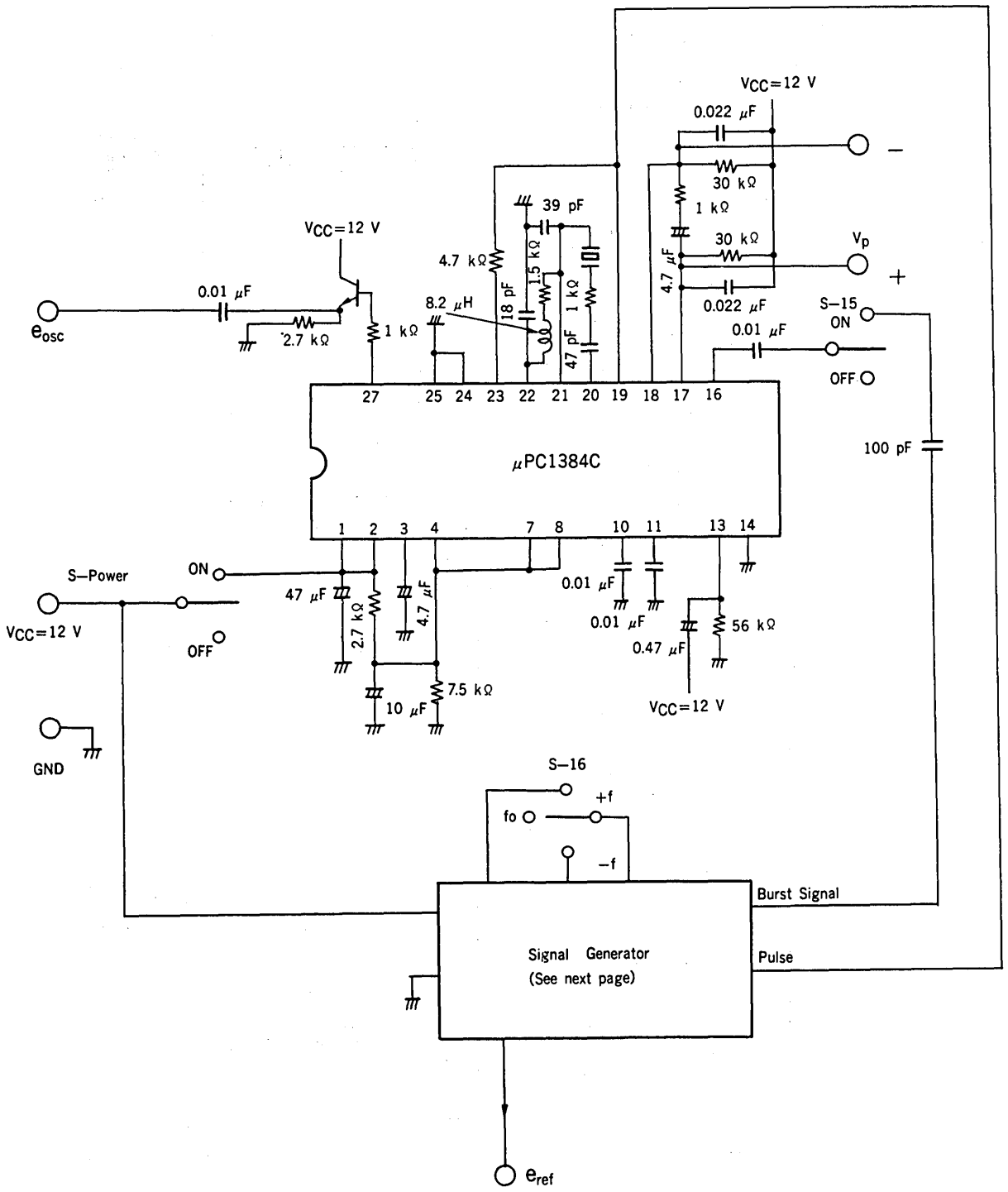


μPC1384C Signal Generator (TEST CIRCUIT 1)

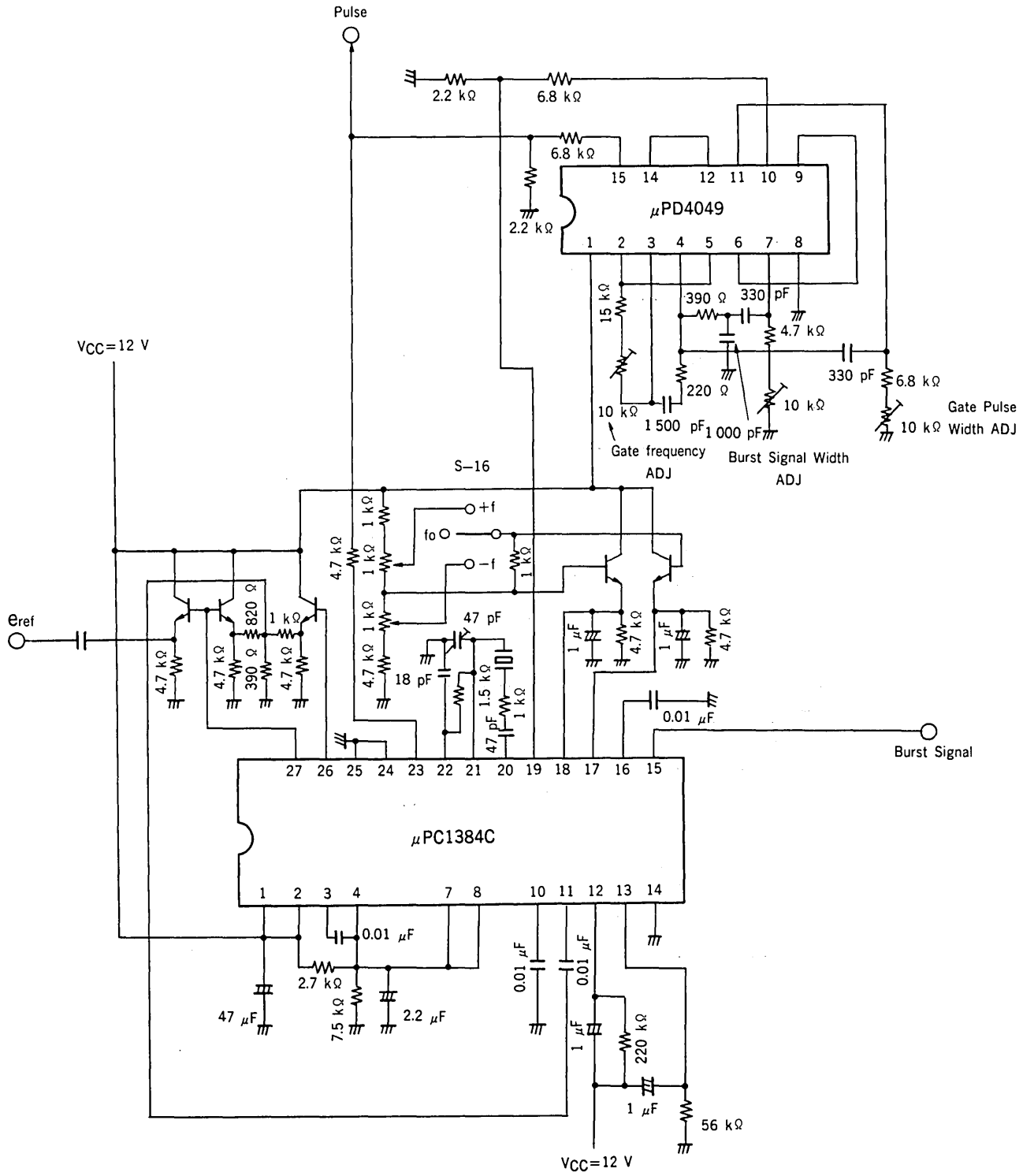




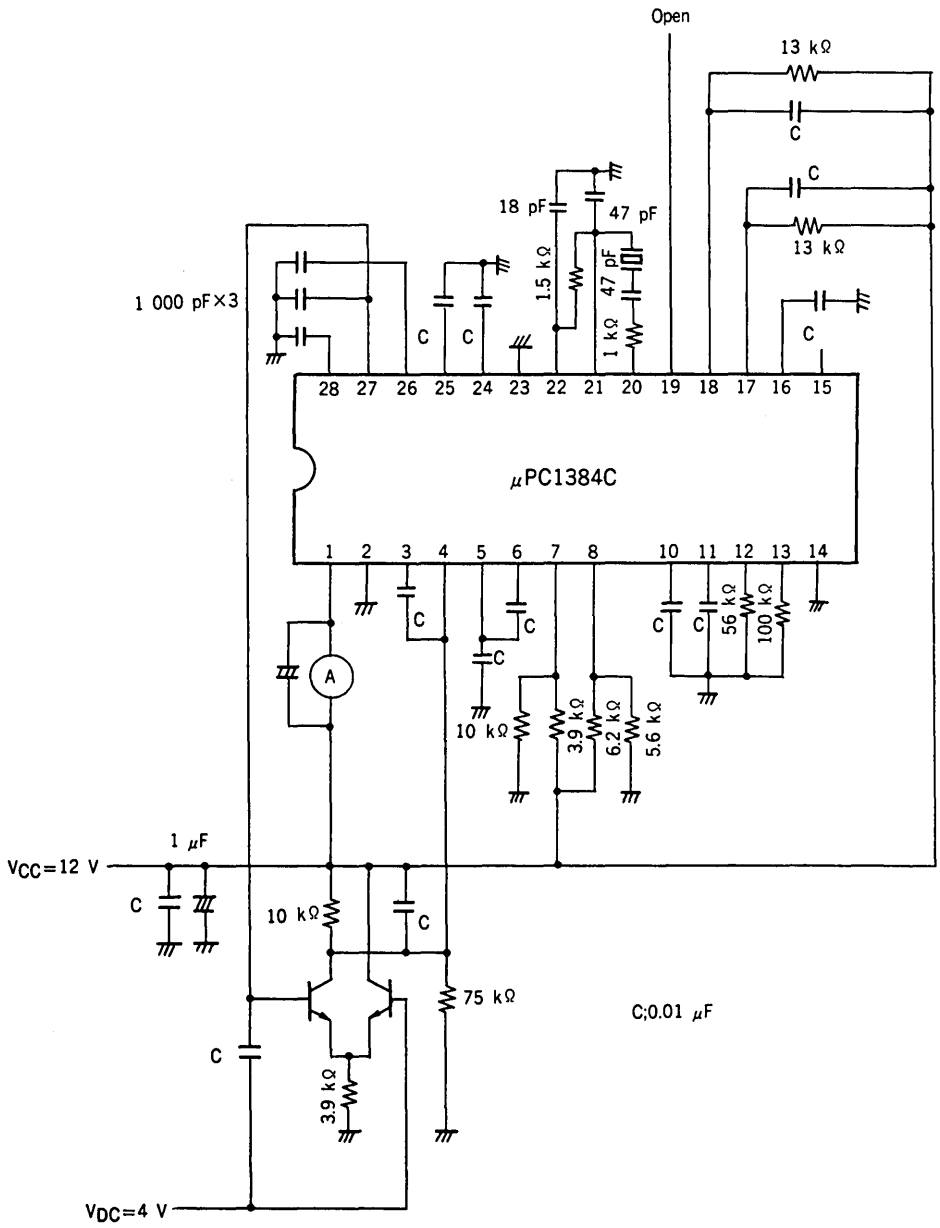
μPC1384C TEST Circuit 2



μPC1384C Signal Generator (TEST Circuit 2)



μPC1384C TEST Circuit 3



	e_b	ACC	e_{c1}	e_{c2}	e_{c3}	e_k, e_{kh}	e_{o1}	R/B	G/B	∠R
S-1 Input	ON	OFF	ON	ON	ON	OFF	ON	ON	ON	ON
S-2 Lum	INV	INV	INV	INV	INV	INV	INV	INV	INV	INV
S-3 Lum	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
S-4 Chro.	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF
S-5 Cont.	MAX	MAX	MAX	MAX	MAX	MAX	MAX	MAX	MAX	MAX
S-6 Satu.	MID	MID	MAX	MID	MIN	MID	MID	MID	MID	MID
S-7 VCO	NORM	NORM	NORM	NORM	NORM	NORM	NORM	NORM	NORM	NORM
S-8 FF.	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF
S-9 Dem.	INT	INT	INT	INT	INT	INT	EXT	EXT	EXT	EXT
S-10 Syst.	PAL	PAL	PAL	PAL	PAL	PAL	PAL	PAL	PAL	PAL
S-11 Blk	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
S-12 Output	B	B	B	B	B	B	B	R	G	R
S-13 Output	e_{o3}	e_{o3}	e_{o3}	e_{o3}	e_{o3}	e_{o3}	e_{o3}	e_{o3}	e_{o3}	e_{o3}
S-14	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON
VR-1	Be trimmed V26 = 3.5 V by Brightness VR (VR-1)									
VR-2										
Input	A	A = SG B – C = ATT	A	A	A	A = SG B – C = ATT	D = SG	D = SG	D = SG	D = SG
SG	Rainbow						f = 4.44 MHz			
Measure Point	e_b	e_b	e_c	e_c	e_c	e_c	e_{oB}	e_{oB}, e_{o3}	e_{oB}, e_{o3}	e_{oB}, e_{o3}
	Oscilloscope	ATT				ATT		AC Volt meter		Phase Meter

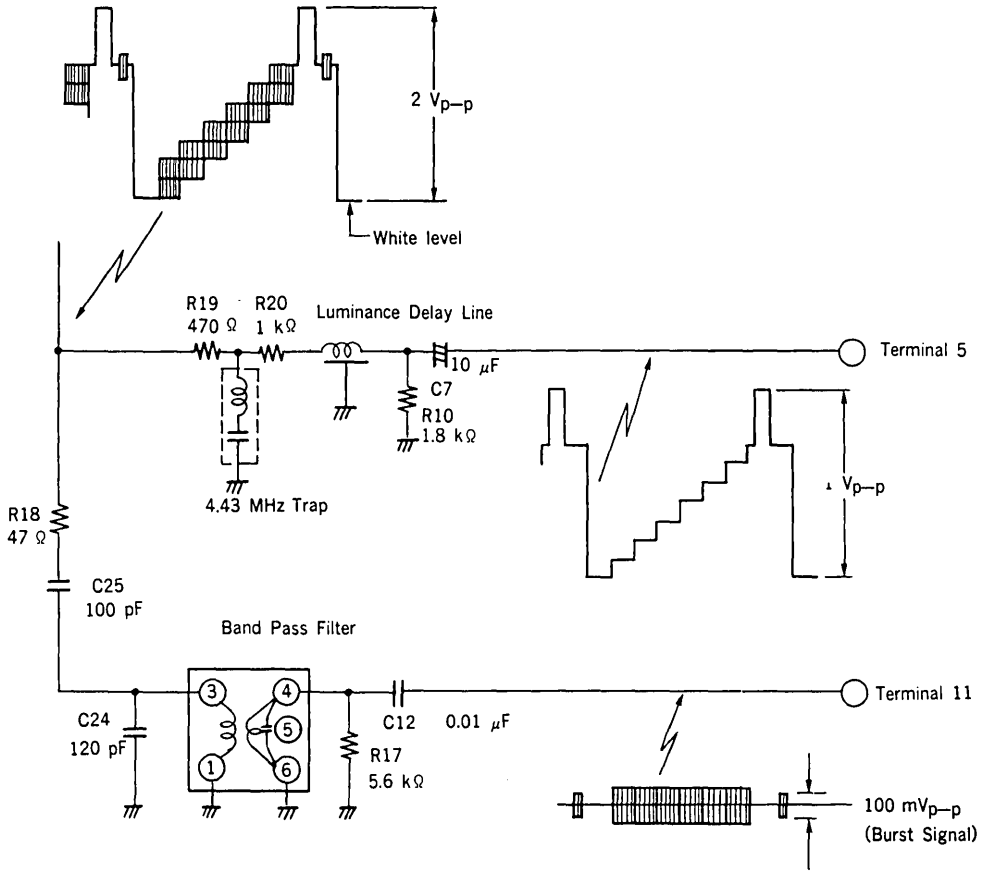
	∠G	e_{o2}	e_{car}	e_{o3}	e_{oc}	Av1, ΔAv1	e_{vc}	DG	T_{DC}	f_v
S-1 Input	ON	ON	ON	ON	ON	ON	ON	ON	ON	OFF
S-2 Lum.	INV	INV	INV	INV	INV	INV	INV	INV	INV	NORM
S-3 Lum.	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON
S-4 Chro.	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF
S-5 Cont	MAX	MAX	MAX	MAX	MAX, MIN	MAX	MAX, MIN	MAX	MAX	MAX
S-6 Satu.	MID	MID	MID	MID	MID	MID	MID	MID	MID	MID
S-7 VCO	NORM	NORM	NORM	NORM	NORM	STOP	STOP	STOP	STOP	STOP
S-8 FF.	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF
S-9 Dem.	EXT	EXT	EXT	INT	INT	EXT	EXT	EXT	EXT	EXT
S-10 Syst.	PAL	PAL	PAL	PAL	PAL	PAL	PAL	PAL	PAL	PAL
S-11 Blk	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
S-12 Output	G	B	BRG	B	B	BRG	B	BRG	B	BRG
S-13 Output	e_{o3}	e_{o3}	e_{o3}	e_{o3}	e_{o3}	e_v	e_v	e_v	e_v	e_v
S-14	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON
VR-1	Be trimmed V26 = 3.5 V by Brightness VR (VR-1)					Be trimmed V26 = 2 V by Brightness VR (VR-1)				V26 = 3.5 V
VR-2										
Input	D = SG	D = SG	—	A	A	A	A	A	A	C = SG
SG	f = 4.44 MHz		—	Rainbow		Video SG 100 % White		Stair Step		SG = CW
Measure Point	e_{oB}, e_{o3}	e_{oB}	e_{car}	e_{o3}	e_{o3}	e_v	e_v	e_v	e_v	e_v
	Phase Meter	Oscilloscope						Vector scope	Oscillo-scope	RF Volt meter

	BR	E_{oM}	E_o, E_{o-T}	$*E_{x-y}$ $\Delta E_{x-y}/\Delta T$	ΔE_{oc}	V_G (min)	V_B	V_{FF}
S-1 Input	ON	ON	ON	ON	ON			
S-2 Lum.	INV	INV	INV	INV	INV			
S-3 Lum.	OFF	OFF	OFF	OFF	OFF			
S-4 Chro.	OFF	OFF	OFF	OFF	OFF			
S-5 Cont.	MAX	MAX	MAX	MAX	MAX, MIN			
S-6 Satu.	MID	MID	MID	MID	MID			
S-7 VCO	NORM	NORM	NORM	NORM	NORM			
S-8 FF	OFF	OFF	OFF	OFF	OFF			
S-9 Dem.	EXT	EXT	EXT	EXT	EXT			
S-10 Syst.	PAL	PAL	PAL	PAL	PAL	PAL	PAL	PAL
S-11 Blk	OFF	OFF	OFF	OFF	OFF			
S-12 Output	BRG	BRG	BRG	RG	B			
S-13 Output	e_{o3}	e_{o3}	e_{o3}	e_{o3}	e_{o3}			
S-14	ON	ON	ON	ON	ON			
VR-1	See TEST Condition	TP = V_{CC}	TP = 9 V	V26 = 3.5 V	V 26 = 2 V			
VR-2								
Input								
SG								
Measure Point	e_{o3}	e_{o3}	e_{o3}	e_{o3}, e_{ov}	e_{o3}			
	DC Voltmeter							

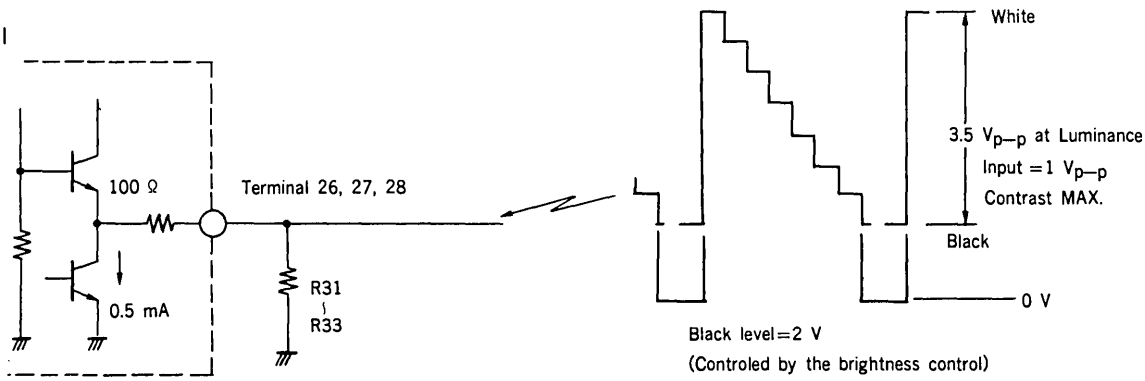
	β	μ	$\Delta\phi$	f_p	Vp
S-15 fo ± f	ON	ON	ON	OFF ON ON OFF	OFF
S-16 Burst	+f (100 Hz) −f (100 Hz)			+f (300 Hz) −f (300 Hz)	fo
Measure Point	Vp e_{ref}	Vp e_{ref}, e_{osc}	e_{ref}, e_{osc}	e_{ref}	V_p
	f.Counter DC Voltmeter	Phase Meter f.Counter DC Voltmeter	Phase Meter f.Counter	f.Counter	DC Voltmeter

μPC1384C Input and Output Signals

Luminance Input Signal



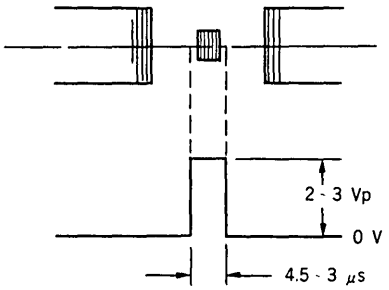
Output Signal

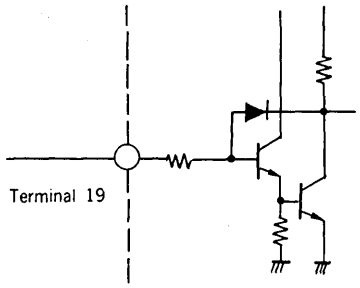


μPC1384C Input Pulse

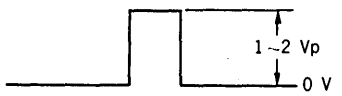
Burst Gate Pulse

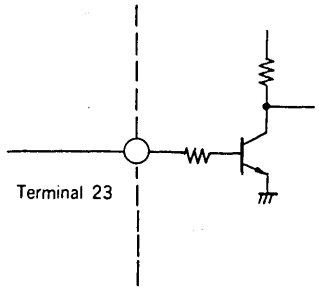
Burst signal = 100 ~ 200 mVp-p
at Terminal 11



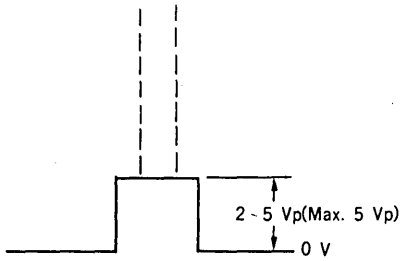


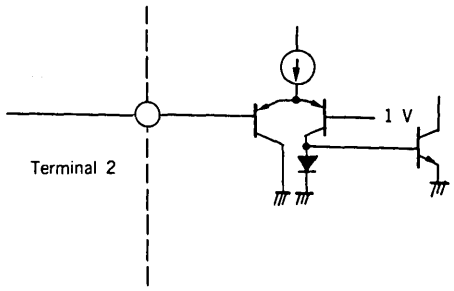
Line Pulse



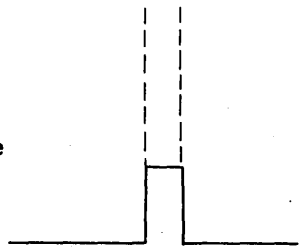


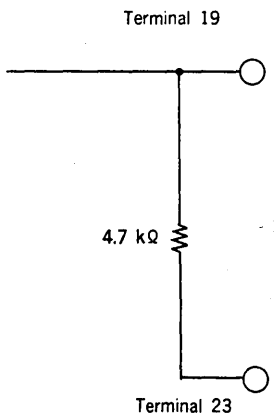
Blanking Pulse (Line Pulse and Field Pulse)





In case of commonly using of Input Pulse

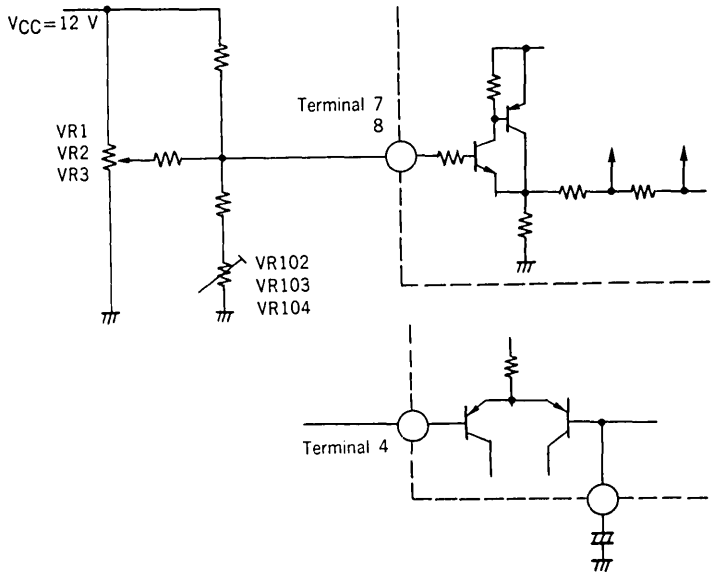




μPC1384C

*Color, Contrast and Brightness controlling circuit

VR1 ; Brightness Control
VR102 ; Sub Brightness
VR2 ; Contrast Control
VR103 ; Sub Contrast
VR3 ; Color Control
VR104 ; Sub Color



V7 (Contrast) 5.5 to 7.0 to 8.5 V
V8 (Color) 4.0 to 5.5 to 7.0 V
V2 (Brightness) 8.2 to 8.7 to 9.2 V

*Color Killer Setting VR105

*APC Setting

Method; 1; Connect Resistor (100 kΩ) between the Terminal 13 and GND as shown Fig. 1 (Killer OFF)

2; Connect Capacitor (0.01 μF) between the Terminal 16 and GND as shown Fig. 2 (Burst Input OFF)

3; Trim 4.433618 MHz by using VR107

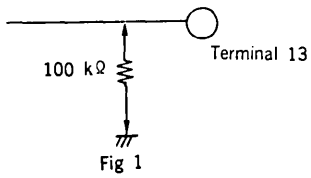


Fig 1

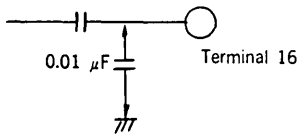
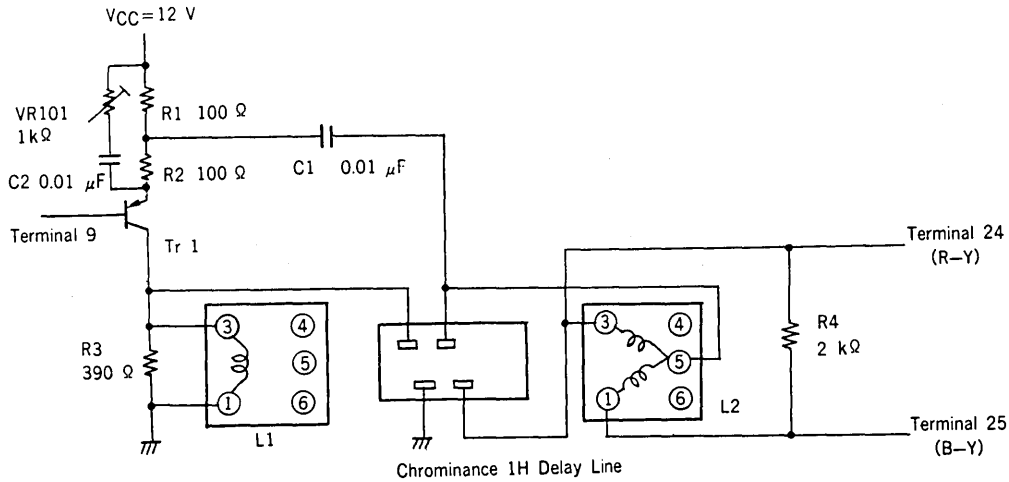


Fig 2

*1H Delay Line Circuit

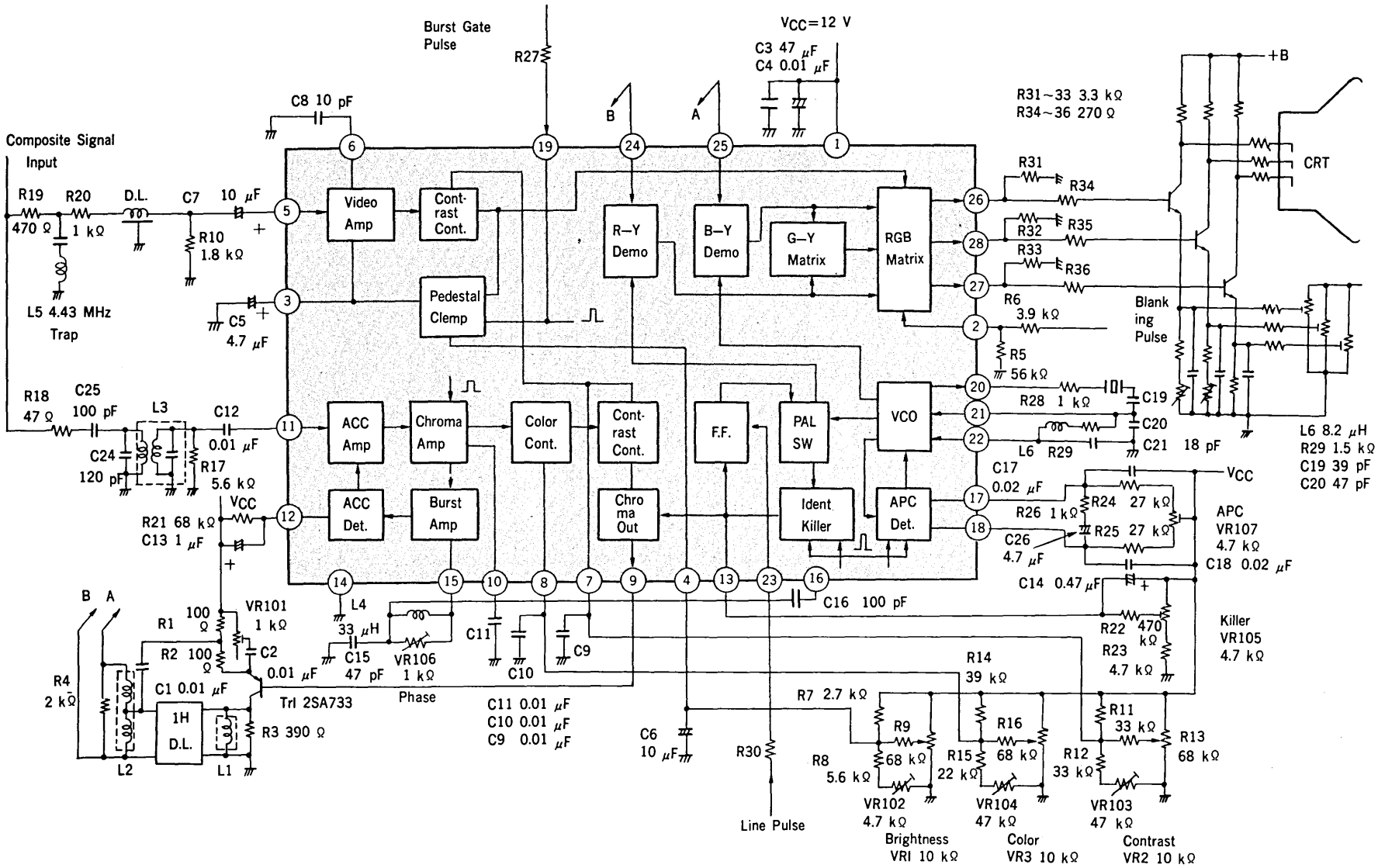


L1 ; Pre Chrominance Delay Line Terminating Coil

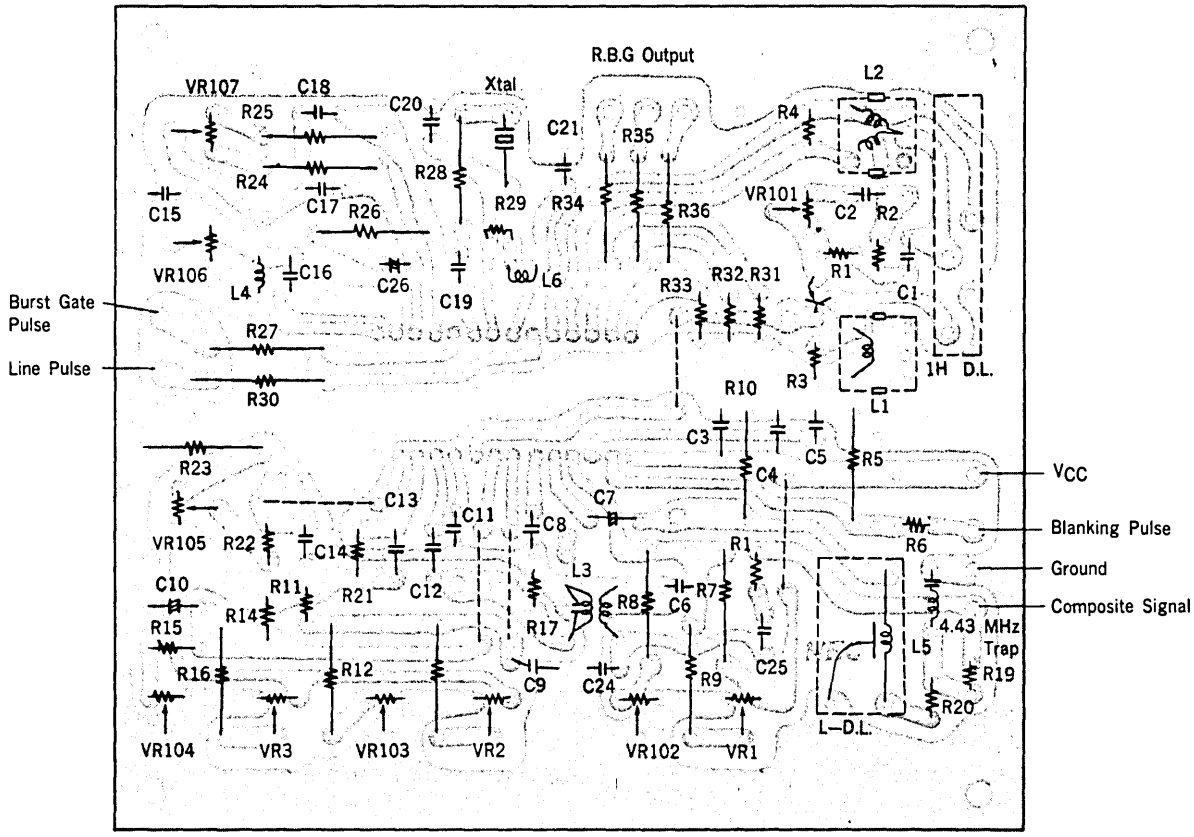
L2, VR101 ; Delay Phase and Amplitude Adjustment

VR106 ; Sub carrier Phase Adjustment

The Block Diagram and External Components for μPC1384C



Printed Circuit Board Pattern (Bottom View)



μPC1384C Table of the external components

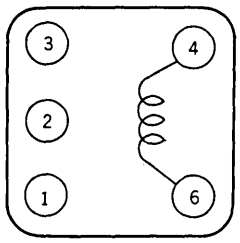
Symbol	Value
R1	100 Ω
R2	100 Ω
R3	390 Ω
R4	2 kΩ
R5	(56 kΩ)
R6	(3.9 kΩ)
R7	2.7 kΩ
R8	5.6 kΩ
R9	68 kΩ
R10	1.8 kΩ
R11	33 kΩ
R12	33 kΩ
R13	68 kΩ
R14	39 kΩ
R15	22 kΩ
R16	100 kΩ
R17	5.6 kΩ
R18	47 Ω
R19	470 Ω
R20	1 kΩ
R21	68 kΩ
R22	470 kΩ
R23	4.7 kΩ
R24	27 kΩ
R25	27 kΩ
R26	1 kΩ
R27	(1.2 kΩ)
R28	1 kΩ
R29	1.5 kΩ
R30	(1.2 kΩ)
R31	3.3 kΩ
R32	3.3 kΩ
R33	3.3 kΩ
R34	270 Ω
R35	270 Ω
R36	270 Ω

Symbol	Value
C1	0.01 μF
C2	0.01 μF
C3	47 μF
C4	0.01 μF
C5	4.7 μF
C6	10 μF
C7	10 μF
C8	10 pF
C9	0.01 μF
C10	0.01 μF
C11	0.01 μF
C12	0.01 μF
C13	1 μF
C14	0.47 μF
C15	47 pF
C16	100 pF
C17	0.022 μF
C18	0.022 μF
C19	39 pF(Xtal C_L=16 pF), 68 pF(Xtal C_L=20 pF)
C20	47 pF
C21	18 pF
C22	—
C23	—
C24	120 pF
C25	100 pF
C26	4.7 μF

Symbol	Value
VR–1	10 kΩ Brightness
VR–2	10 kΩ Contrast
VR–3	10 kΩ Color Saturation
VR101	1 kΩ D.L. Level
VR102	4.7 kΩ Sub Brightness
VR103	47 kΩ Sub Contrast
VR104	47 kΩ Sub Color Saturation
VR105	4.7 kΩ Killer Adj
VR106	1 kΩ Phase Adj
VR107	4.7 kΩ APC Adj
L1	D.L. Matching Coil Type No TKRNS 24984NK (Toko Corp.)
L2	D.L. Matching Coil Type No TKRNS 24985VN (Toko Corp.)
L3	Band Pass Filter Type No 163NEF1148WWJ (Toko Corp.)
L4	33 μH
L5	4.43 MHz Trap Type No LCS2H1H-102 (TDK Corp.)
L6	8.2 μH
Tr1	2SA733 (NEC)
Xtal	4.43 MHz C_L=16 pF or 20 pF
L-D.L.	Luminance Delay Line Type No CTS-1804C (Showa Densei Corp.)
1 H D.L.	1 H Delay Line Type No EFD EN (Matsushita Corp.)

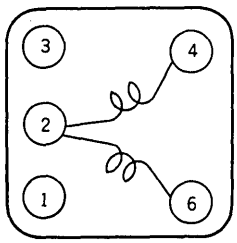
1 H Delay Line Matching Coil Specification.

L1 Input Coil
(PAL)



Type No. TKRNS – 24984NK
Product TOKO Corp.
f_o ; 4.43 MHz
6 –4 ; 18 T
Cout ; 330 pF (4 –6)
Qu ; 59 ± 20 %
Wire Material ; 0.1 / UEW

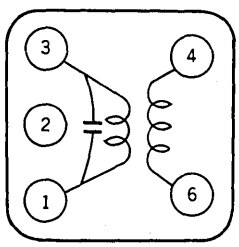
L2 Output Coil



Type No. TKRNS – 24985VN
Product TOKO Corp.
f_o ; 4.43 MHz
4 –2 ; 18 T
2 –6 ; 18 T
Cout ; 75 pF (4 –6)
Qu ; 44 ± 20 %
Wire Material ; 0.1 / 2UEW

Chrominance Input Coil Specification.

L3 Input Coil
(PAL)



Type No. 163NEF – 1148WWJ
Product TOKO Corp.
f_o ; 4.43 MHz
6 –4 ; 35 1/4 T
3 –1 ; 76 T
Cout ; PH 47 pF
Wire Material ; 0.1 / UEW

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1397C

ANALOG INTERFACE CIRCUIT FOR TELETEXT SYSTEM

The μPC1397C is a monolithic integrated circuit for the interface stage between the external analog signals and chroma stage. This IC is packaged in 22 pins dual in package. This is most suitable interface IC for view data and CRT display application because of clamping circuit built in R, G and B circuit separately and excellent switching characteristics of video/data switch-circuit. Contrast function can control both of video signal and data signal, and brightness function also can do it. White peak level can set by external voltage applied to pin 15.

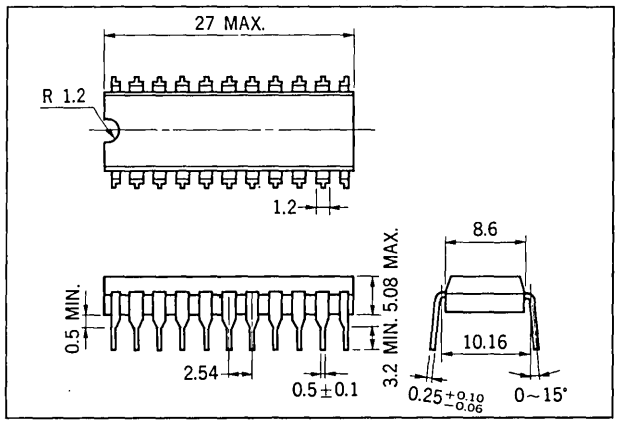
FEATURES

- External analog inputs are acceptable as well as digital.
- High data switching speed.

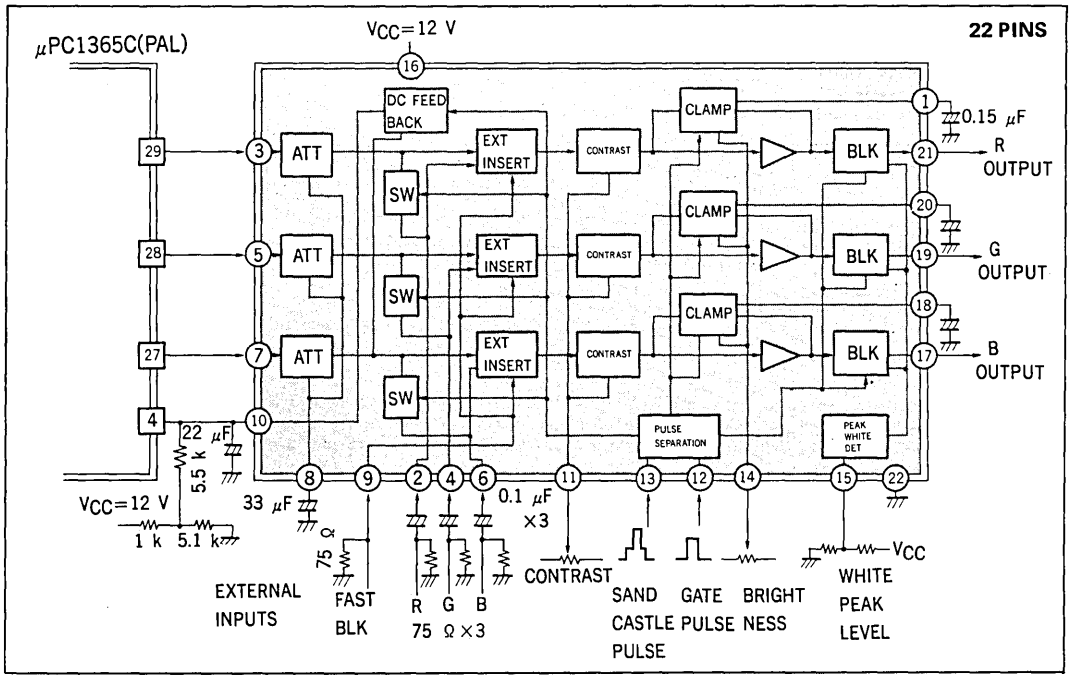
	R,G,B	Blanking	
The rise time	35	35	ns
The fall time	35	35	ns
The delay time	20	20	ns

- Contrast and Brightness can be controlled commonly on TV and external signals.
- Can be connected directly to R,G,B, output TV-signals of any IC's.

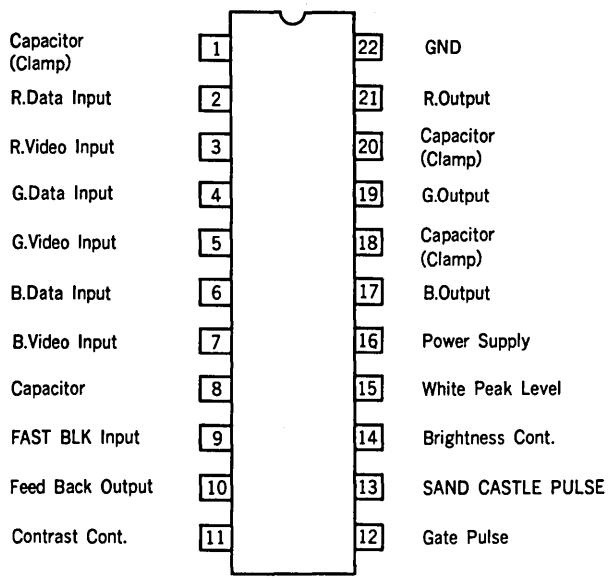
PACKAGE DIMENSIONS (Unit : mm)



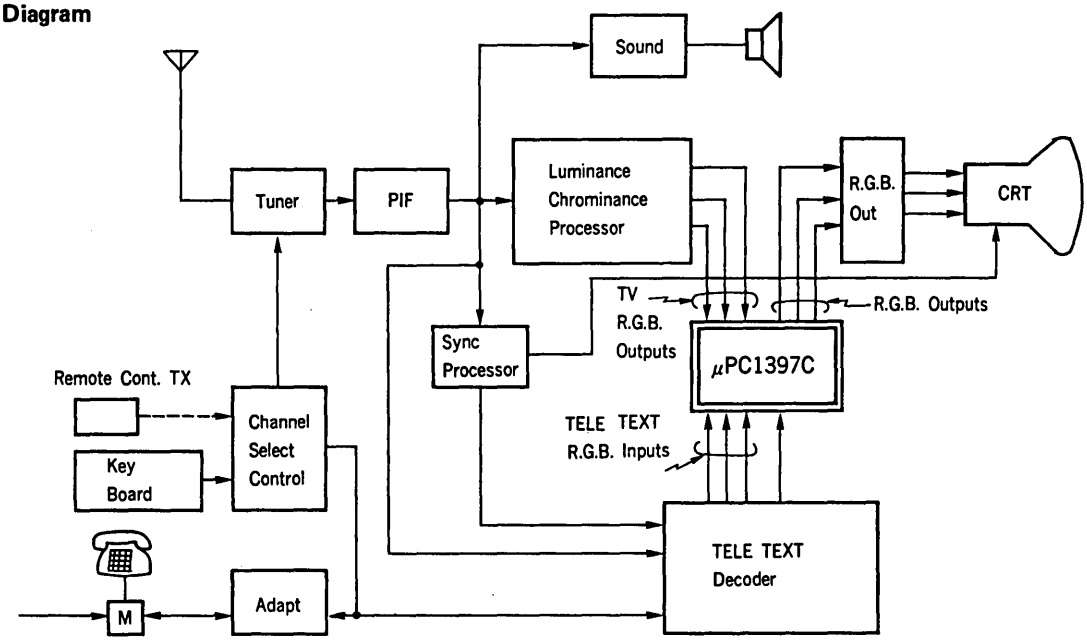
BLOCK DIAGRAM



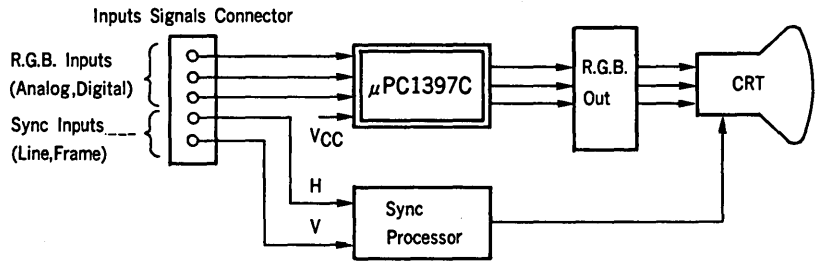
PIN CONNECTION DIAGRAM (22 Pin Dual In Line Package)



1 TV SET Block Diagram



2 CRT DISPLAY SET Block Diagram



ABSOLUTE MAXIMUM RATINGS (T_a = +25 °C unless otherwise)

Supply Voltage	V_{CC}		15	V
Power Dissipation	P_d	T_a = +70 °C	850	mW
RGB (VIDEO) Input	E_{RGB}		0 to V_{CC}	V_{DC}
RGB (DATA) Input	E_{DATA}		0 to V_{CC}	V_{DC}
SAND CASTLE Pulse	E_{SCP}		-6 to V_{CC}	V_{DC}
Gate Pulse	E_{GP}		-6 to V_{CC}	V_{DC}
Fast BLK Pulse	$E_{F.BLK}$		0 to V_{CC}	V_{DC}
Control Voltage	E_{cont}		0 to V_{CC}	V_{DC}
Operating Temperature	T_{opt}		-20 to +70	°C
Storage Temperature	T_{stg}		-40 to +125	°C

RECOMMENDED OPERATING CONDITIONS

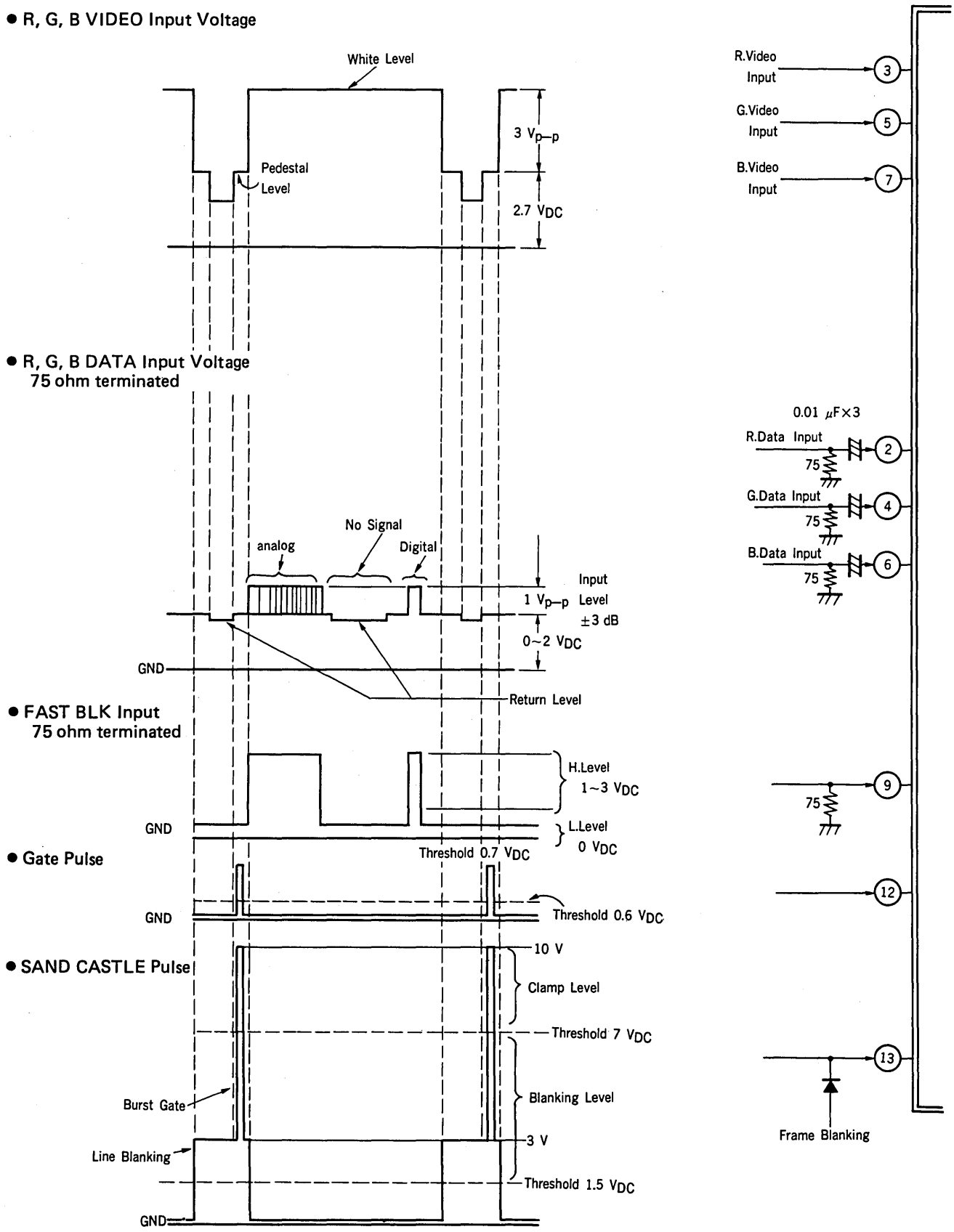
CHARACTERISTIC	SYMBOL		UNIT
Supply Voltage	V_{CC}	12 ± 10 %	V
RGB (VIDEO) Input Voltage	ein B ~ W	3	Vp-p
Black level of RGB (VIDEO) Input Voltage	Ein BK	2.7 (at feed back)	V_{DC}
RGB (DATA) Input Voltage	ein RGB	1 Vp-p ± 3 dB 75 ohm terminated	
Black level of RGB (DATA) Input Voltage	Ein BK	0 ~ 2	V_{DC}
Return level of RGB (DATA) (Line, Frame)	Ein BK (R)	Less than ein RGB X Max. 1 %	V_{DC}
Fast BLK Input, H. Level L. Level	$V_{F.BLK (H)}$ $V_{F.BLK (L)}$	1 ~ 3 0	V_{DC} V_{DC}
Gate Input Pulse Voltage	V_G	3	Vp
SAND CASTLE Pulse BLK Level Gate Level	V_{SCP}	 2 ~ 6 more than 8	 V_{DC} V_{DC}
Brightness Control Voltage	$V_{C BR}$	1 ~ 2 ~ 4	V_{DC}
White Peak Supression Setting Voltage	V_{WPS}	4 ~ 9	V_{DC}

ELECTRICAL CHARACTERISTICS (T_a = 25 °C unless otherwise noted, V_{CC} = 12 V)

NO	CHARACTERISTIC	SYMBOL	TEST CKT	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
1	Supply Current	I_{CC}			43		mA	V_{CC} = 12 V No Input; RGB (VIDEO), RGB (DATA) Clamp Gate Pulse
2	RGB (VIDEO) Gain	$G_V\begin{pmatrix}R\\G\\B\end{pmatrix}$		0.9	1.17	1.5	times	RGB (VIDEO) Input; B ~ W=3 Vp-p Bk. Level = 2 V_{DC} Set; Bk. Out Level = 2 V_{DC} Contrast = Max, WPS Level = V_{CC}
3	Relative Ratio Gv $\begin{pmatrix}R\\G\\B\end{pmatrix}$	ΔGvx-y		0.85	1.0	1.15	times	Same as No. 2
4	RGB (DATA) Gain	$G_e\begin{pmatrix}R\\G\\B\end{pmatrix}$		2.9 1.3	3.5 1.5	4.1 1.7	times times	RGB (DATA) Input; Contrast = Max. B ~ W = 1 Vp-p Set; Bk. Out Level = Contrast = Typ. 2 V_{DC}
5	Relative Ratio Ge $\begin{pmatrix}R\\G\\B\end{pmatrix}$	ΔGex-y		0.85	1.0	1.15	times	Same as No. 4
6	Relative Ratio Ge/Gv	Ge/Gv		2.7	3.0	3.3	times	Same as No. 2, 4
7	RGB (VIDEO), RGB (DATA) Frequency Characteristic	$fe_v\begin{pmatrix}R\\G\\B\end{pmatrix}$		6.0	–	–	MHz	RGB (VIDEO), RGB (DATA) Input; 0.5 Vp-p. 0 dB frq. = 100 kHz –3 dB, Contrast = Max.
8	RGB Quiescent Output Voltage	$E_o\begin{pmatrix}R\\G\\B\end{pmatrix}$		3.2	3.5	3.8	V_{DC}	RGB (VIDEO) Input; B ~ W = 0 Vp-p Bk. Level = 2.7 V_{DC} BRT Cont = 3.5 V_{DC}
9	$E_o\begin{pmatrix}R\\G\\B\end{pmatrix}$ Supply Voltage Coefficient	$\Delta E_{o\text{-}v}\begin{pmatrix}R\\G\\B\end{pmatrix}$		–	0.3	–	V/V	V_{CC} = 12 V ± 20 % EoB = 3.5 V_{DC} (at V_{CC} = 12 V)
10	$E_o\begin{pmatrix}R\\G\\B\end{pmatrix}$ Temperature Coefficient	$\Delta E_{o\text{-}T}\begin{pmatrix}R\\G\\B\end{pmatrix}$		–2	0	+2	mV/°C	T_a = –20 ~ +70 °C EoB = 3.5 V_{DC} (at T_a = +25 °C)
11	Difference Output Voltage	ΔEox-y		–100	0	100	mV_{DC}	RGB (VIDEO) Input; B ~ W = 0 Vp-p Bk. Level = 2.7 V_{DC}, BRT Cont = 3.5 V_{DC}
12	Eox-y Temperature Coefficient	Eox-y (T)		–	0	60	mV_{DC}	T_a=–20 ~ +70 °C Maximum Changing Level
13	Maximum Output Voltage	EoM		8.5	–	–	V	RGB (VIDEO) Input; B ~ W = 3 Vp-p, Bk. Level = 2.7 V_{DC}, White Clip Level, Cont. = Max. BRT = 2 ~ 6 V_{DC}, WPS Level = V_{CC}
14	Changing Bk. Level RGB (VIDEO)/RGB (DATA)	V_{BK}		–	–	60	mV_{DC}	RGB (VIDEO) Input; B ~ W = 3 Vp-p, Bk. Level = 2.7 V_{DC}, RGB (DATA) Input; B ~ W = 1 Vp-p, Set; Bk. Out Level = 2 V_{DC}
15	DC Restored (VIDEO), (DATA)	$T_{DC}\begin{pmatrix}V\\D\end{pmatrix}$		90	95	100	%	RGB (VIDEO) Input; B ~ W = 3 Vp-p Bk. Level = 2.7 V_{DC}, APL = 10 ~ 90 % No Blanking, Set; Bk. Out Level = 2 V_{DC}
16	Brightness Control Sensitivity	BR		0.9	1.0	1.1	V/V	BRT Cont. Voltage = 1.5 ~ 2.5 V_{DC} Changing Bk. Level
17	Contrast Cont. Range	Rcont.		15	17	19	dB	RGB (VIDEO) Input; B ~ W = 3 Vp-p Bk. Level = 2.7 V_{DC}, RGB (DATA): B ~ W = 1 Vp-p, Cont. = Max./Min. Set; Bk. Out Level = 2 V_{DC}

NO	CHARACTERISTIC	SYMBOL	TEST CKT	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
18	Maximum Changing Black Level by Contrast	Eoc		−50	0	+50	mV_{DC}	RGB (VIDEO) Input; B ~ W = 0 Vp-p Bk. Level = 2.7 V_{DC}, Set; Bk. Level = 2 V_{DC} Contrast = Max. ~ Min.
19	White Suppression Output Voltage	WS(R/G/B)		6.5	7.0	7.5	V_{DC}	RGB (VIDEO) Input; B ~ W = 3 Vp-p Bk. Level = 2.7 V_{DC}, Set; WS Level = 7 V_{DC} BRT Cont. = 2 ~ 6 V_{DC}
20	Gate Pulse Minimum Input Voltage	V_{GPM}		—	—	1	Vp	
21	SAND CASTLE Pulse Input BLK	Vsc th (BLK)		1.0	1.5	2.0	V	
	Threshold Level GATE	Vsc th (GATE)		6.5	7.0	7.5	V	
22	Fast BLK Pulse Input Threshold Level	Vth (F.BLK)		0.5	0.7	0.9	V	Input Level RGB Output Less than Vth (F.BLK) RGB (VIDEO) More than Vth (F.BLK) RGB (DATA)
23	Fast BLK SW Time Rise, Fall	tr, f sw		—	35	60	ns	RGB (VIDEO) Input; W = 3 Vp-p, Bk. Level = 2.7 V_{DC}, RGB (DATA) =
	Relative Rise, Fall Time	Δtr, f sw		—	0	20	ns	No Input, Cont. = Max. Set Bk. Out Level = 2 V_{DC}
24	Fast BLK SW Time Delay	td sw		—	20		ns	Same as No. 23
	Relative Delay Time	Δtd sw		—	—	20	ns	Load Condition; 3.3 kΩ/10 pF at Fall Time Only
25	RGB (DATA) SW Time Rise, Fall	tr, f(R/G/B)		—	35	60	ns	RGB (VIDEO) Input; B ~ W = 0 Vp-p Bk. Level = 2.7 V_{DC}, RGB (DATA)
	Relative Rise, Fall Time	Δtr, f(R/G/B)		—	—	20	ns	Input; B ~ W = 1 Vp-p, Cont. = Max. Set Bk. Out Level = 2 V_{DC}
26	RGB (DATA) SW Time Delay	td(R/G/B)		—	20		ns	Same as No. 25
	Relative Delay Time	Δtd(R/G/B)		—	—	20	ns	Load Condition; 3.3 kΩ/10 pF at Fall Time only

μPC1397C INPUT SIGNAL LEVEL



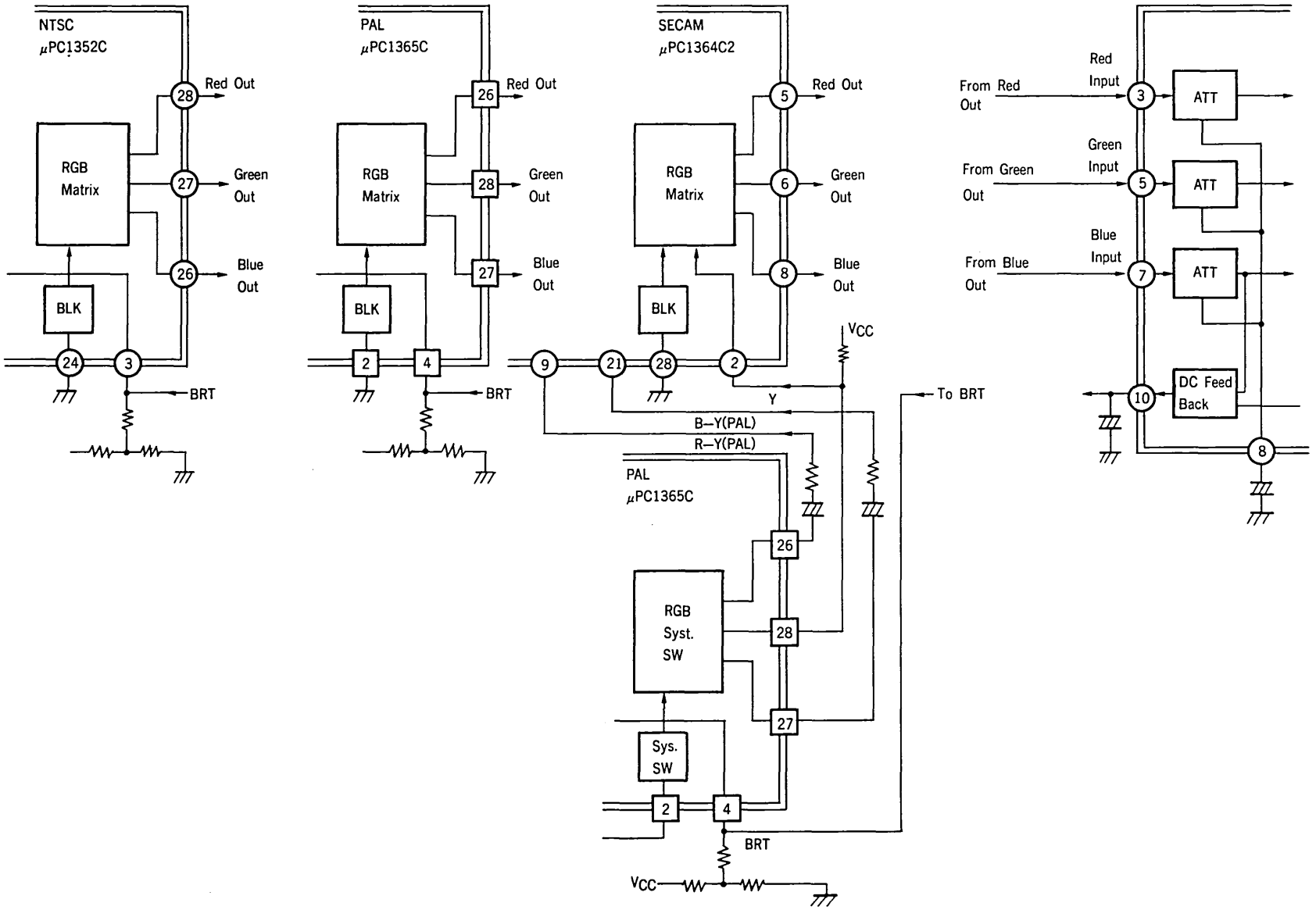
APPLICATION

NTSC System
Japan. CAPTAIN.
USA TELETEXT

PAL System
U.K. TELETEXT, Prestel

PAL – SECAM System
W.G. Video Text, Bildshirmzeitung
FRANCE, Antiope

Interface IC
μPC1397C



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1031H2

VERTICAL DEFLECTION DEVICE FOR MONOCHROME TV AND SMALL-SIZED COLOR TV

DESCRIPTION

The μPC1031H2 is a semiconductor integrated circuit for use in vertical-deflection circuit of monochrome TV and small sized color TV.

It oscillates Vertical signal synchronizing with Vertical synchronization signal, and puts out the Vertical Deflection current with the single chip.

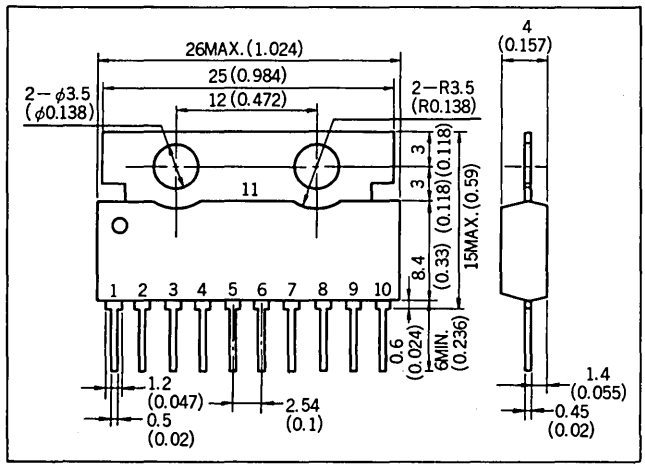
And as it has some compensating circuits against the effect of temperature in it, it shows excellent characteristics.

It uses a Single In-line Package easily mountable on heatsink.

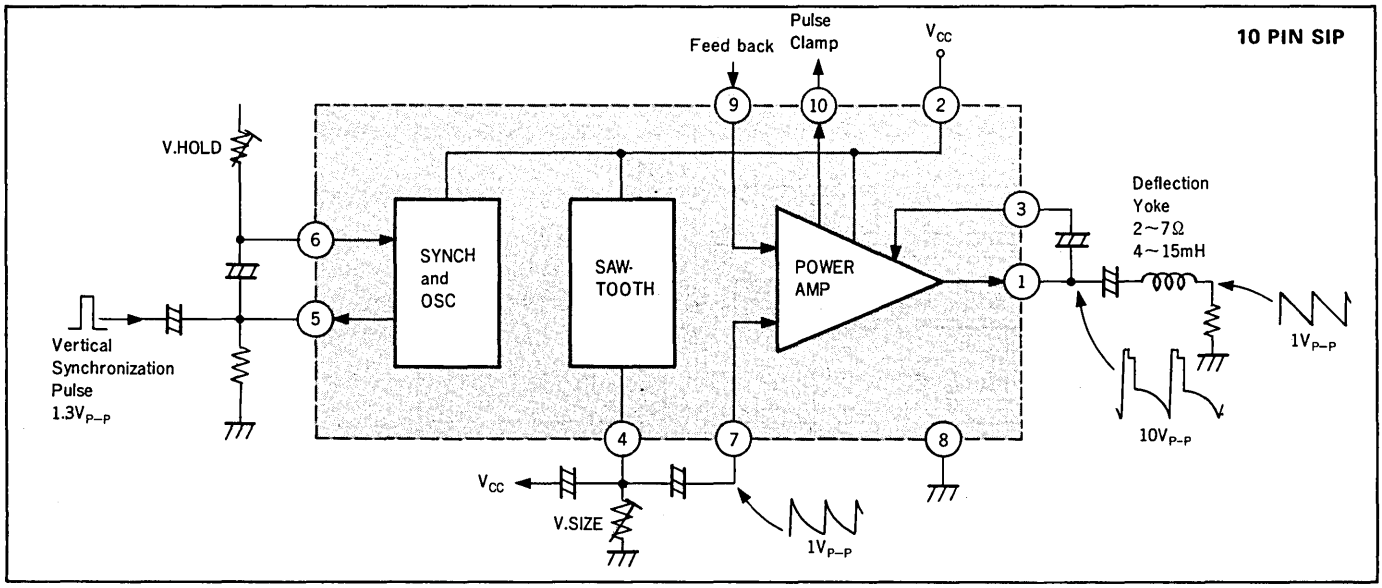
FEATURES

- Less number of required, external components.
- Wide range of operational voltage (9 to 18 volts).
- Freely adjustable pull-in range (by the resistor be put between terminal 5 and the ground, and presenting time constant of integrating circuit).
- Adjustable blanking pulse-width.
- Large output current-capacity (2 $A_{p\text{-}p}$).
- Built-in adjusting circuit for flyback time.
- Easy mounting on printed circuit boad.

PACKAGE DIMENSIONS in millimeters (inches)



BLOCK DIAGRAM



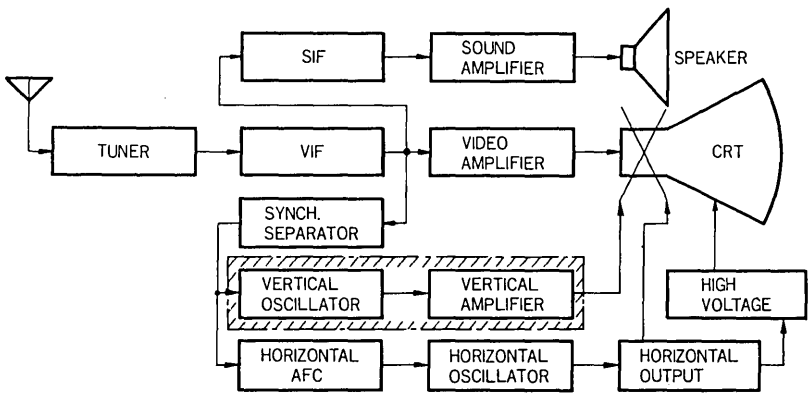
ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Power Supply Voltage	V_{CC}	20	V
Output Current	$I_{p\text{-}p}$	2	$A_{p\text{-}p}$
Power Dissipation	Pd1	1.5 (Ta=+75°C) Without heatsink	W
Power Dissipation	Pd2	2.15 (Ta=+75°C) With aluminum heatsink (31.6 x 31.6 x 1mm t)	W
Operating Temperature Range	Topt	-20 to +75	°C
Storage Temperature Range	Tstg	-40 to +150	°C

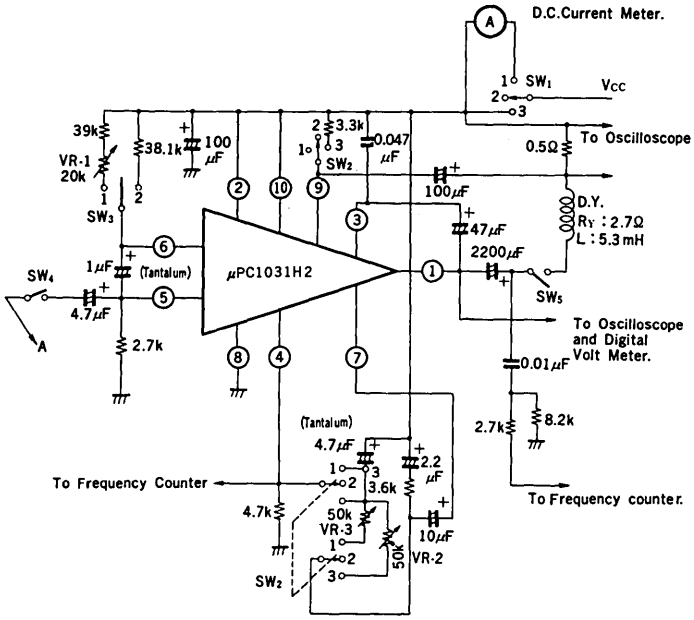
ELECTRICAL CHARACTERISTICS (V_{CC}=12V, Ta=+25±3°C)

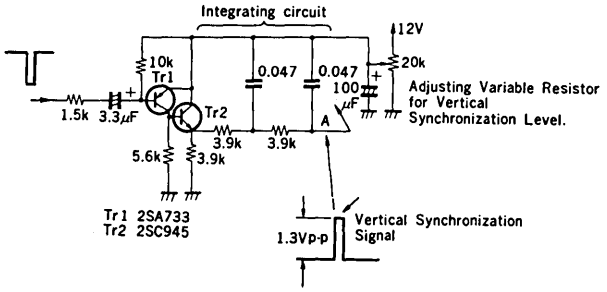
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CKT.	TEST CONDITIONS
Circuit Current	I_{CC}	15	30	46	mA	1	No input signal and no load condition
Output Terminal Voltage	V_N	5.6	6.0	6.4	V	1	No input signal and no load condition
Vertical Oscillation Frequency	f_{IV}		50/60		Hz	1	Synchronization signal voltage applied at terminal 5 is 1.3 $V_{p\text{-}p}$
Free-running Frequency	f_{VO}	53	60	67	Hz	1	Oscillation capacitor; 1 μF (Tantalum) resistor; 38.1 k ohms
Pull-in Range	f_P	−10	−12		Hz	1	With specified integration circuit, applied voltage of synchronization signal is 1.3 $V_{p\text{-}p}$ at terminal 5
Drift of Free-running Frequency vs. Power Supply Voltage	Δf_{VO}			±1.0	Hz	1	Frequency drift from standard frequency (f_{VO} 60 Hz at V_{CC}=12 V) vs. power supply voltage (V_{CC}=12 ±2 V)
Deviation of Pull-in Range vs. Power Supply Voltage	Δf_P			∓3.0	Hz	1	Deviation from the frequency range for pull in (at V_{CC}=12 V) vs. power supply voltage (V_{CC}=12 ±2 V)
Output Saturation Voltage	V_{sat}		1.3	1.6	V	1	Output current : 0.7 A
Output pulse width of terminal 4	T_o	300	420	600	μs	1	Oscillation capacitor; 1 μF (Tantalum) resistor; 38.1 k ohms

FUNCTION

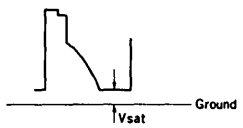
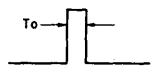


TEST CIRCUIT



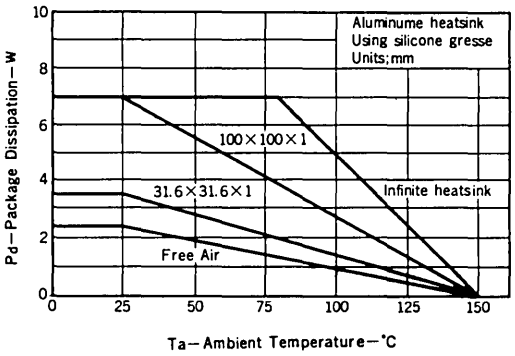


SWITCH POSITION

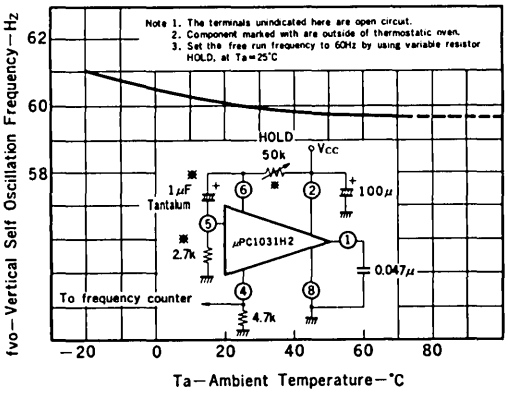
CHARACTERISTIC	SYMBOL	SWITCH POSITION					MEASUREMENT METHOD
		SW1	SW2	SW3	SW4	SW5	
Circuit current	I_{CC}	1	2	2	OFF	OFF	–
Output terminal voltage	V_N	1	2	2	OFF	OFF	Measure the voltage at terminal 1, by using a digital voltmeter.
Vertical oscillation frequency	f_V	3	1	1	ON	ON	Apply the synchronization signal of 1.3 $V_{p\text{-}p}$ to terminal 5.
Free-running oscillation frequency	f_{VO}	3	1	2	OFF	ON	–
Pull-in range	f_P	3	1	1	↓OFF ON	ON	Adjust the pull in frequency, by using VR-1, after SW4 has been turned to the OFF position, and then confirm that the perfect synchronization is obtained when SW4 has been turned to the ON position.
Drift of free-running frequency vs. power supply voltage	Δf_{VO}	3	1	2	OFF	ON	Vary the power supply voltage in the range of V_{CC} = 12 ±2 V.
Deviation of frequency range for pull in vs. power supply voltage	Δf_P	3	1	1	↓OFF ON	ON	Vary the power supply voltage in the range of V_{CC} = 12 ±2 V.
Output saturation voltage	V_{sat}	3	3	1	ON	ON	Adjust VR-2 so that the terminal voltage across the resistor of 0.5 ohms may be 0.7 $V_{p\text{-}p}$, and then measure the waveform at the output terminal. 
Output pulse width of terminal 4	T_O	3	2	2	OFF	ON	Measure the output pulse width at terminal 4, by using an oscilloscope. 

TYPICAL CHARACTERISTICS (Ta = 25°C)

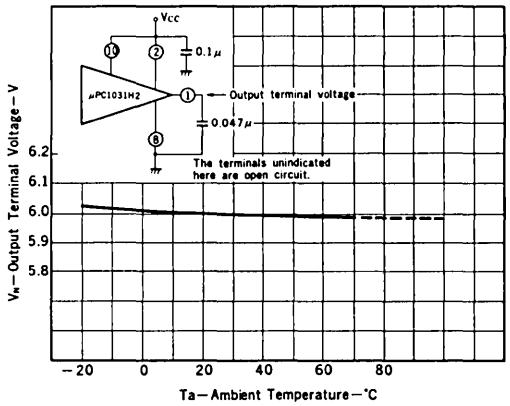
POWER DISSIPATION vs.
AMBIENT TEMPERATURE



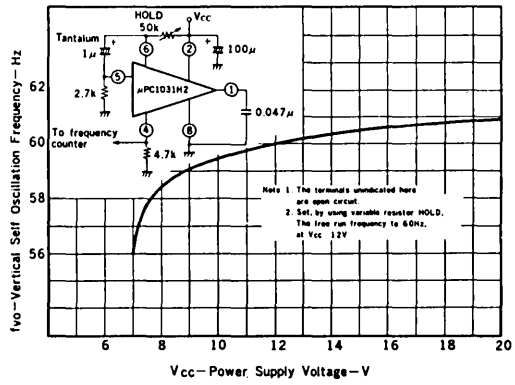
FREE-RUNNING OSCILLATION FREQUENCY
vs. AMBIENT TEMPERATURE



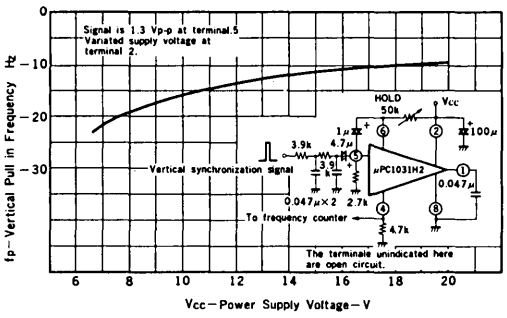
OUTPUT TERMINAL VOLTAGE
vs. AMBIENT TEMPERATURE



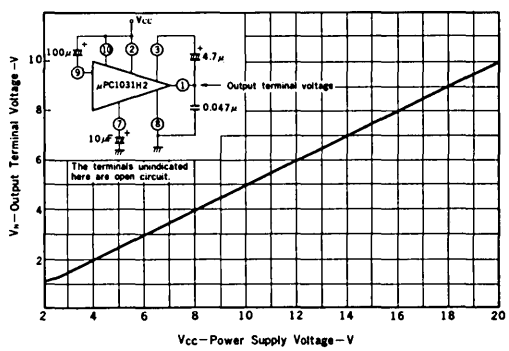
FREE-RUNNING OSCILLATION FREQUENCY
vs. POWER SUPPLY VOLTAGE



VERTICAL PULL IN FREQUENCY
vs. POWER SUPPLY VOLTAGE



OUTPUT TERMINAL VOLTAGE
vs. POWER SUPPLY VOLTAGE



ADJUSTMENT METHODS OF FLYBACK TIME FOR THE μPC1031H2

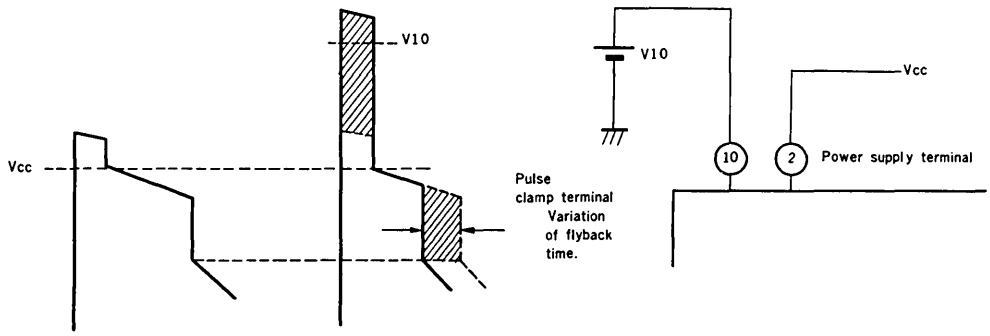
Since the flyback time of the vertical output voltage is sometimes elongated excessively by the constant of the deflection yoke, a part of the flyback time appears in the television picture. For the prevention of this elongation, the following methods are available.

The confirmation experiment is requested beforehand, since the adjustment of the flyback time is depend on the constant of the deflection yoke used in the TV set.

Method 1. Adjustment of the clamping level of the flyback pulse at terminal 10.

The blanking pulse level is normally clamped by the power supply voltage connected to terminal 10.

The flyback time, however, can be adjusted by the change of the voltage at terminal 10. Adjust the clamping voltage at terminal 10 between the power supply voltage and 18 volts.



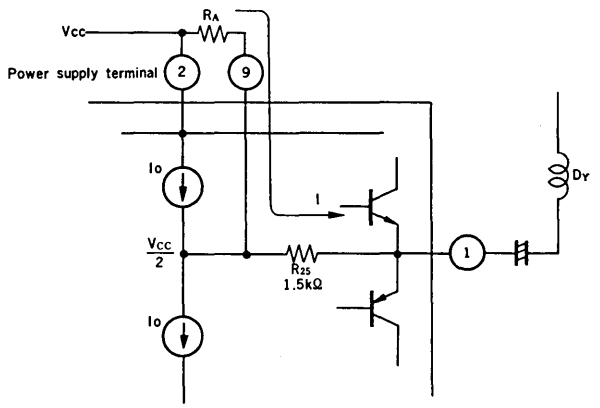
Method 2. Adjustment through decreasing of middle potential of the output by a resistor connected between terminal 2 and 9.

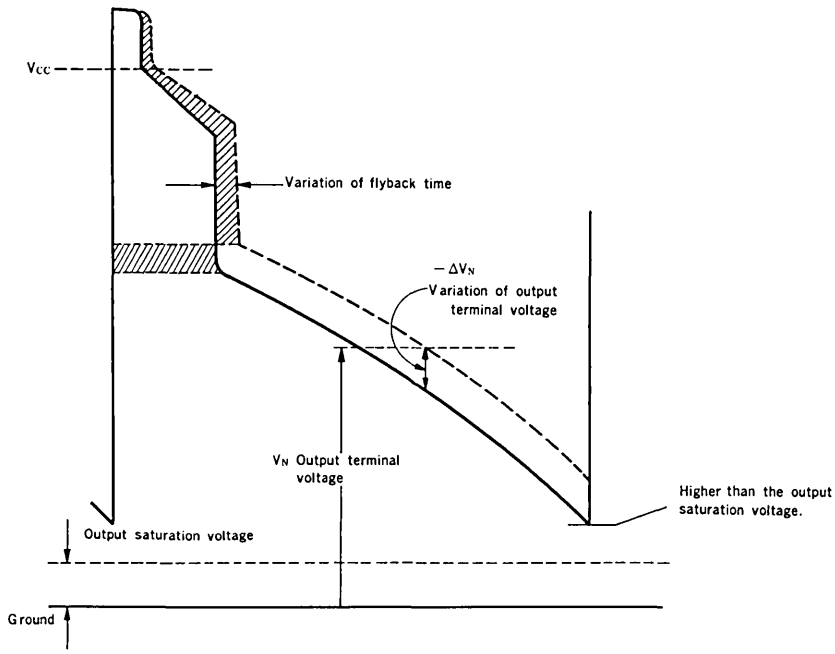
The voltage at terminal 9 is a half of the power supply voltage. The middle potential of the output, however, can be decreased by the voltage drop across resistor R_{25}, when the current is supplied to R_{25} through a resistor be put between terminals 2 and 9.

The potential variation, due to R_A, for the middle potential of the output is given by the following equation that has a temperature coefficent.

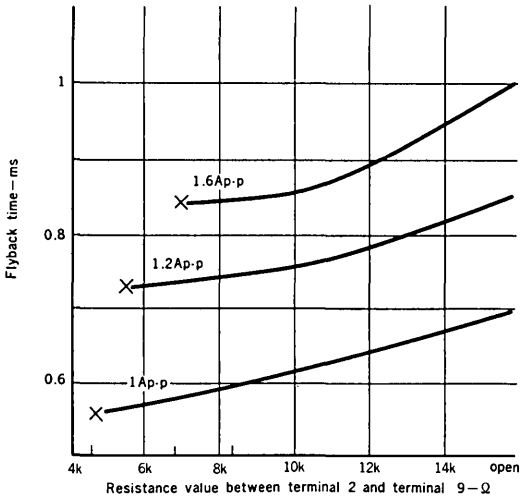
$$-\Delta V_N = \frac{V_{CC}\, R_{25}}{2\, R_A} [1 + 0.002\,(T_{opt} - 25)]$$

The adjustment should be made so that the waveform amplitude of the output may not be clipped by the saturation voltage level of the output in the operating temperature range.

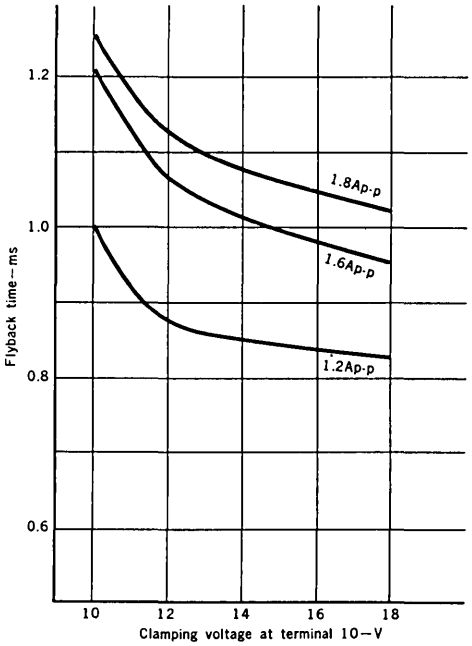




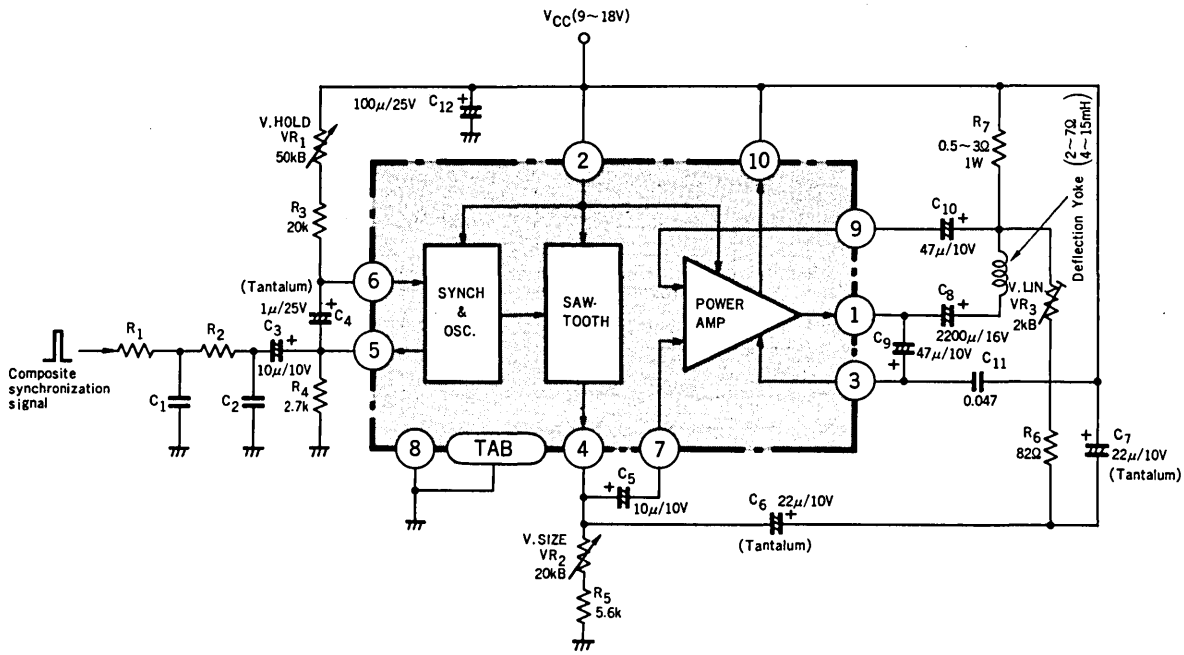
Typical Variation Characteristic of Flyback Time vs. Resistance Value between Terminal 2 and 9.



Typical Variation Characteristic of Flyback Time vs. Clamping Voltage at Terminal 10.

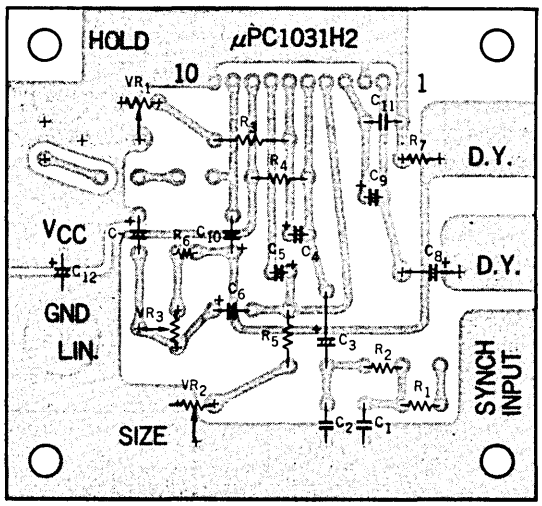


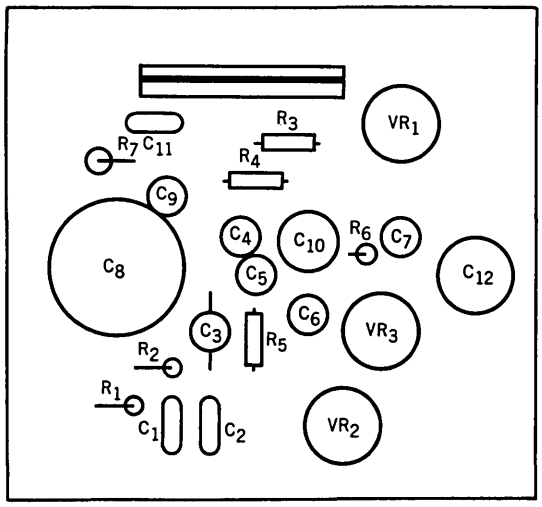
EXAMPLE OF PERIPHERAL CIRCUIT FOR THE μPC1031H2



Typical Example of Components Layout with the μPC1031H2 on P.C. Board

P.C. Board Pattern and Components Layout.



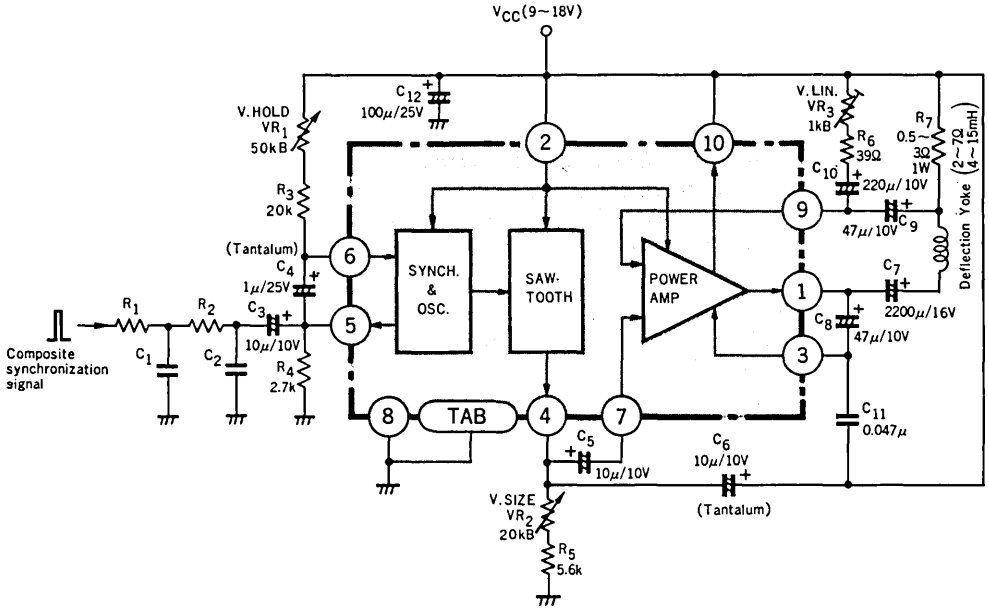


COMPONENTS

SYMBOL	SPECIFICATION	
R_1	—	
R_2	—	
R_3	20 kΩ	1/4 W
R_4	2.7 kΩ	1/4 W
R_5	5.6 kΩ	1/4 W
R_6	82 Ω	1/4 W
R_7	0.5 to 3 Ω, 1 to 2 W	
C_1	—	
C_2	—	
C_3	10 μF	10 V
C_4	1 μF	25 V (Tantalum)

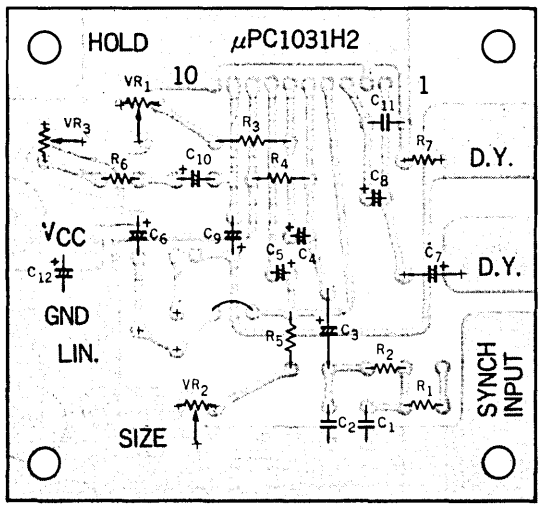
SYMBOL	SPECIFICATION	
C_5	10 μF	10 V
C_6	22 μF	10 V (Tantalum)
C_7	22 μF	10 V (Tantalum)
C_8	2200 μF	16 V
C_9	47 μF	10 V
C_{10}	47 μF	10 V
C_{11}	0.047 μF	
C_{12}	100 μF	25 V
VR_1	50 kΩ-B	
VR_2	20 kΩ-B	
VR_3	2 kΩ-B	

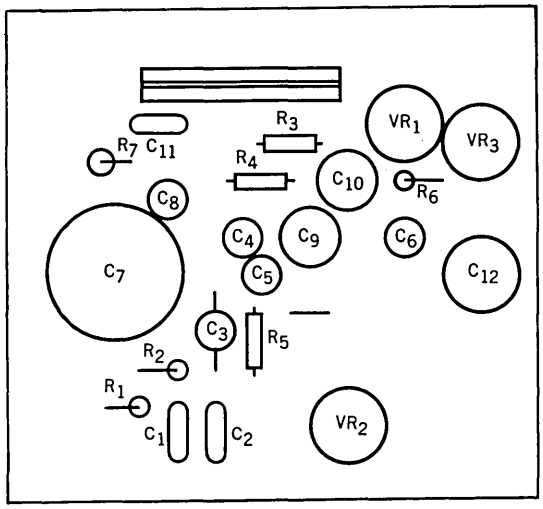
EXAMPLE OF PERIPHERAL CIRCUIT FOR THE μPC1031H2



Typical Example of Components Layout with the μPC1031H2 on P.C. Board

P.C. Board Pattern and Components Layout





COMPONENTS

SYMBOL	SPECIFICATION	
R_1	—	
R_2	—	
R_3	20 kΩ	1/4 W
R_4	2.7 kΩ	1/4 W
R_5	5.6 kΩ	1/4 W
R_6	39 Ω	1/4 W
R_7	0.5 to 3 Ω, 1 to 2 W	
C_1	—	
C_2	—	
C_3	10 μF	10 V
C_4	1 μF	25 V (Tantalum)

SYMBOL	SPECIFICATION	
C_5	10 μF	10 V
C_6	10 μF	10 V (Tantalum)
C_7	2200 μF	16 V
C_8	47 μF	10 V
C_9	47 μF	10 V
C_{10}	220 μF	10 V
C_{11}	0.047 μF	
C_{12}	100 μF	25 V
VR_1	50 kΩ-B	
VR_2	20 kΩ-B	
VR_3	1 kΩ-B	

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1377C

SYNCHRONIZATION SIGNAL PROCESSOR OF COLOR TV

DESCRIPTION

The μPC1377C is a silicon monolithic integrated circuit designed for horizontal deflection circuit and vertical deflection circuit of color TV set.

It consists two synchronization signal separators, vertical oscillator, vertical saw tooth shaper, vertical pre-drive, vertical retrace blanking pulse generator, horizontal AFC, horizontal oscillator, horizontal pre-driver and abnormal high voltage prevention circuit, in it.

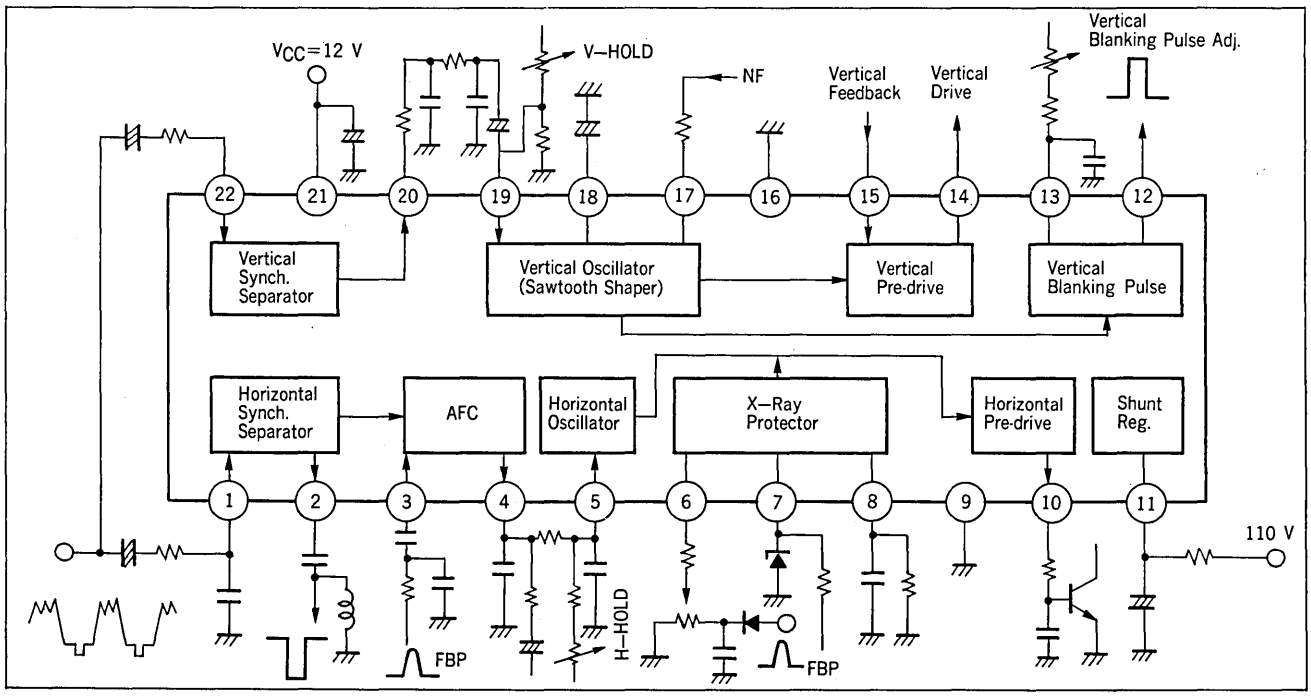
The horizontal part can take the operation current from high +B line as it has a shunt type regulator in it.

The synchronization signal separators are provided for horizontal signal and vertical one independently, so it works very stable even in the ghost phenomenon, weak electrical field and etc.

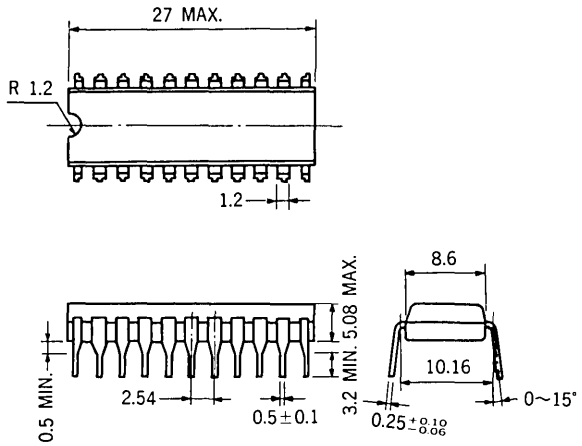
FEATURES

- Provided two synchronous signal separators realizes very stable synchronization, as they are provided each of horizontal signal and vertical one independently.
- Remarkably improved interlace tracking brought by the completely separated wiring in horizontal part and vertical one.
- Vertical retrace blanking time can be set freely and strictly by the adjust terminal.
- Very low drift of oscillation frequency of vertical oscillator and horizontal one against ambient temperature.

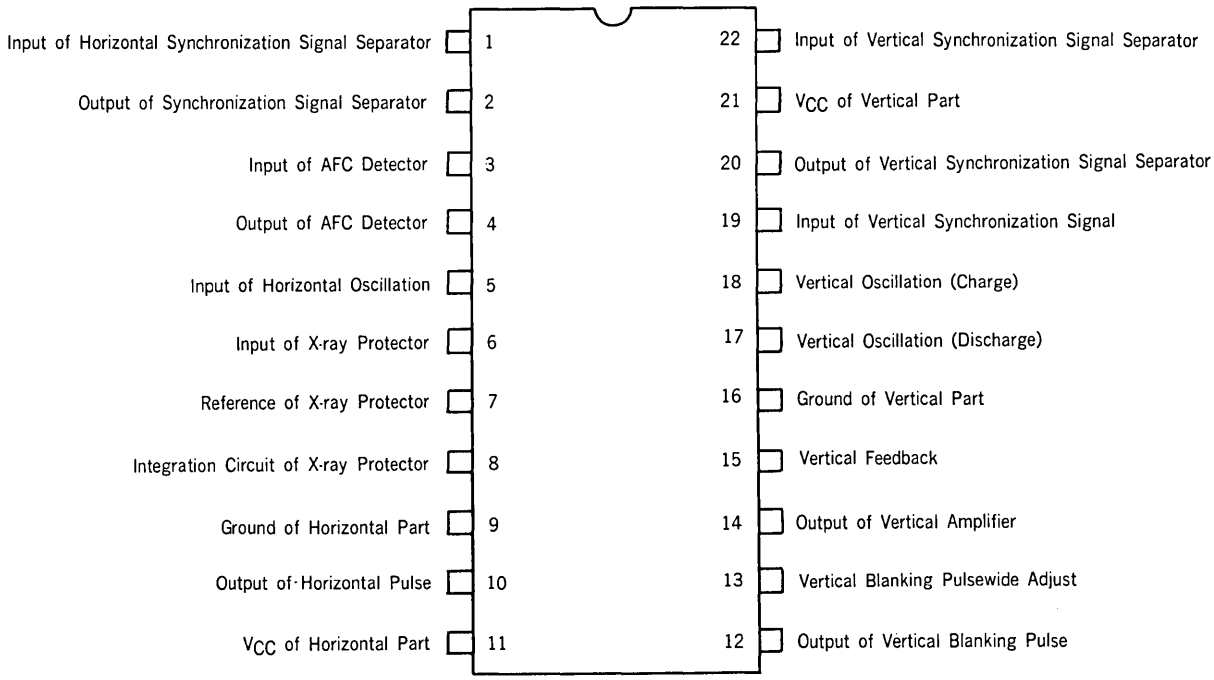
BLOCK DIAGRAM



PACKAGE DIMENSIONS (Unit : mm)



CONNECTION DIAGRAM (Top View)



Mark (+) of current expresses that the current is flowing into the terminal. Mark (-) of current expresses that the current is flowing out from the terminal.

ABSOLUTE MAXIMUM RATINGS (T_a=25 ± 3 °C)

Power Supply Voltage for Vertical Part	V_{21}	15		V
Power Supply Current Drain for Horizontal Part	V_{11}	30		mA
Vertical Output Current	I_{14}	−30 to +0		mA
Horizontal Output Current	I_{10}	−10 to +10		mA
Power Dissipation	P_D	600	(T_a=75 °C)	mW
Operating Temperature	T_{opt}	−20 to +75		°C
Storage Temperature	T_{stg}	−40 to +125		°C

RECOMMENDED CONDITIONS (T_a=25 °C)

Power Supply Voltage for Vertical Part	V_{21}	12	V
Power Supply Current Drain for Horizontal Part	I_{11}	15	mA

ELECTRICAL CHARACTERISTICS (T_a=25 °C)

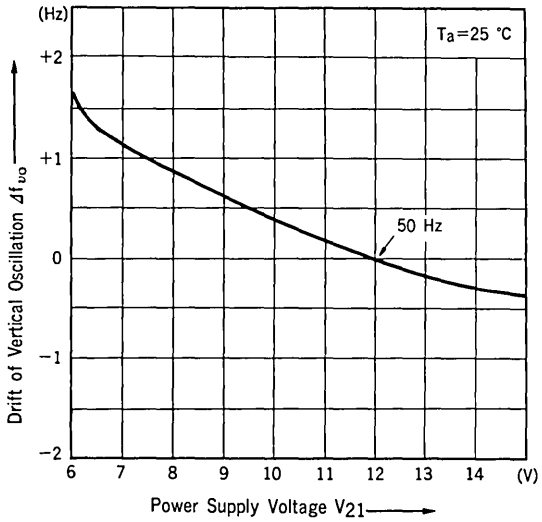
(V_{21} = 12 V, I_{11} = 15 mA, Standard Circuit)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Power Supply Current for Vertical Part	I_{21}	10.5	14	17.5	mA	V_{21}=12 V
Power Supply Voltage for Horizontal Part	V_{11}	12.0	13.0	14.5	V	I_{11}=15 mA
Vertical Free-running Frequency	f_{vo}	48	50	53	Hz	C_{18}=1 μF, R_{17}=33 kΩ
Drift of Vertical Free-running Frequency	$\Delta f_{vo}(V_{CC})$	0	0.8	1.0	Hz	$\Delta f_{vo}(V_{CC})=\lvert f_{vo}(9.6\ V)-f_{vo}(14.4\ V)\rvert$
Drift of Vertical Free-running Frequency	$\Delta f_{vo}(T_a)$	0	0.6	1.0	Hz	$\Delta f_{vo}(T_a)=\lvert f_{vo}(-20\ °C)-f_{vo}(+75\ °C)\rvert$
Vertical Synchronizing Capture Frequency	f_{pv}	46	48	50	Hz	
Output Middle Voltage	V_{MID}	12	13	14	V	Output Power: μPC1378H
Drift of Output Middle Voltage	$\Delta V_{MID}(T_a)$	0		1.0	V	$\Delta V_{MID}(T_a)=\lvert V_{MID}(-20\ °C)-V_{MID}(+75\ °C)\rvert$
Retrace Pulse Width (1)	RPW(1)	0.95	1.0	1.05	ms	C_{13}=0.047 μF, R_{13}=30.75 kΩ
Retrace Pulse Width (2)	RPW(2)	1.9	2.0	2.1	ms	C_{13}=0.1 μF, R_{13}=28.5 kΩ
Retrace Pulse Voltage	RPV	10	11		V_{p-p}	
Drift of Horizontal Power Supply Voltage	$\Delta V_{11}(T_a)$			130	mV	$\Delta V_{11}(T_a)=\lvert\Delta V_{11}(-20\ °C)-\Delta V_{11}(+75\ °C)\rvert$
Horizontal Synchronizing Capture Frequency	f_{PH}	±500	±700	±900	Hz	C_5=5 600 pF
Efficiency of Horizontal Oscillation Control	β	38	40	45	Hz/μA	
Gain of AFC Detector	μ	190	300	420	μA/rad	
Horizontal Free-running Frequency	f_{HO}	15.00	15.75	16.50	kHz	C_5=5 600 pF, R_5=14.5 kΩ
Drift of Horizontal Free-running Frequency	$\Delta f_{HO}(I_{11})$	0		50	Hz	$\Delta f_{HO}(I_{11})=\lvert f_{HO}(15\ mA)-f_{HO}(9\ mA)\rvert$
Drift of Horizontal Free-running Frequency	$\Delta f_{HO}(T_a)$	0	40	100	Hz	$\Delta f_{HO}(T_a)=\lvert f_{HO}(-20\ °C)-f_{HO}(+75\ °C)\rvert$
Horizontal Output Pulse Width	PWH	24.5	26	27.5	μs	
Horizontal Output Pulse Voltage	PWV	10	11		V_{p-p}	
Horizontal Output Current	I_{10}	−3.5	−4.5	−6.0	mA	
Input Voltage of X-ray Protector	V_6	−0.1		0.1	V	V_7 = 6.2 V

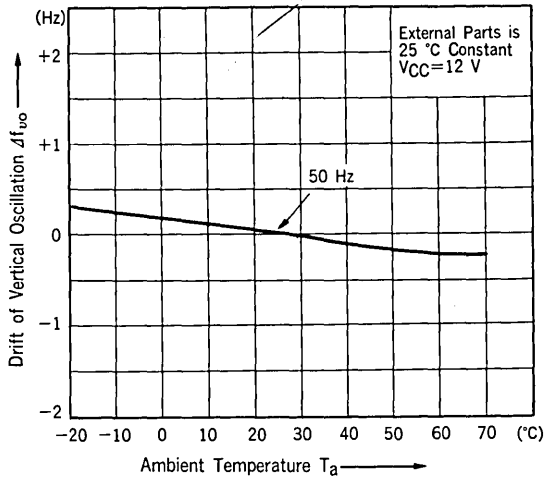
TYPICAL CHARACTERISTICS (T_a = 25 °C)

1. Vertical part

DRIFT OF VERTICAL OSCILLATION AGAINST POWER SUPPLY VOLTAGE

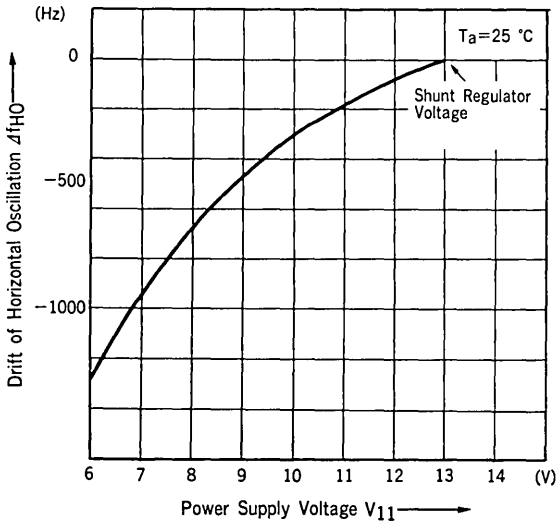


DRIFT OF VERTICAL OSCILLATION AGAINST AMBIENT TEMPERATURE

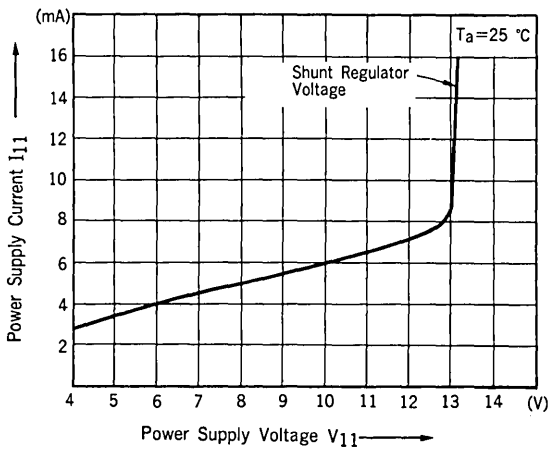


2. Horizontal part

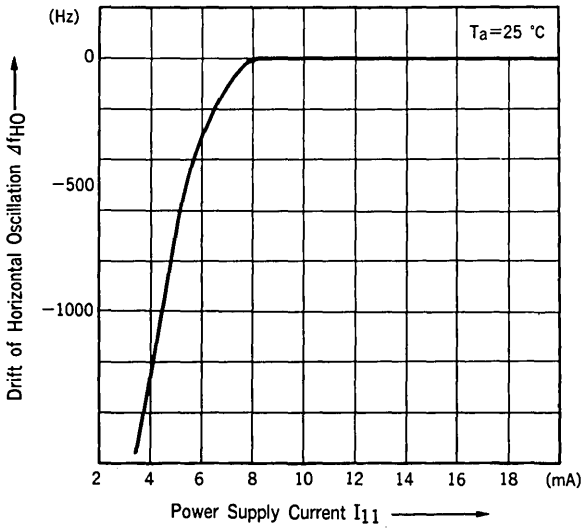
DRIFT OF HORIZONTAL OSCILLATION AGAINST POWER SUPPLY CURRENT



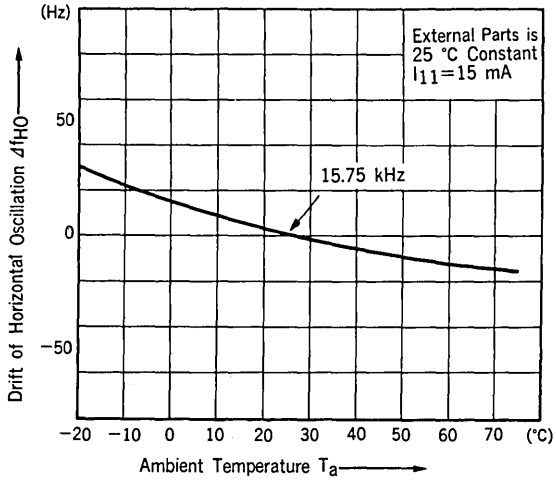
POWER SUPPLY CURRENT vs. POWER SUPPLY VOLTAGE



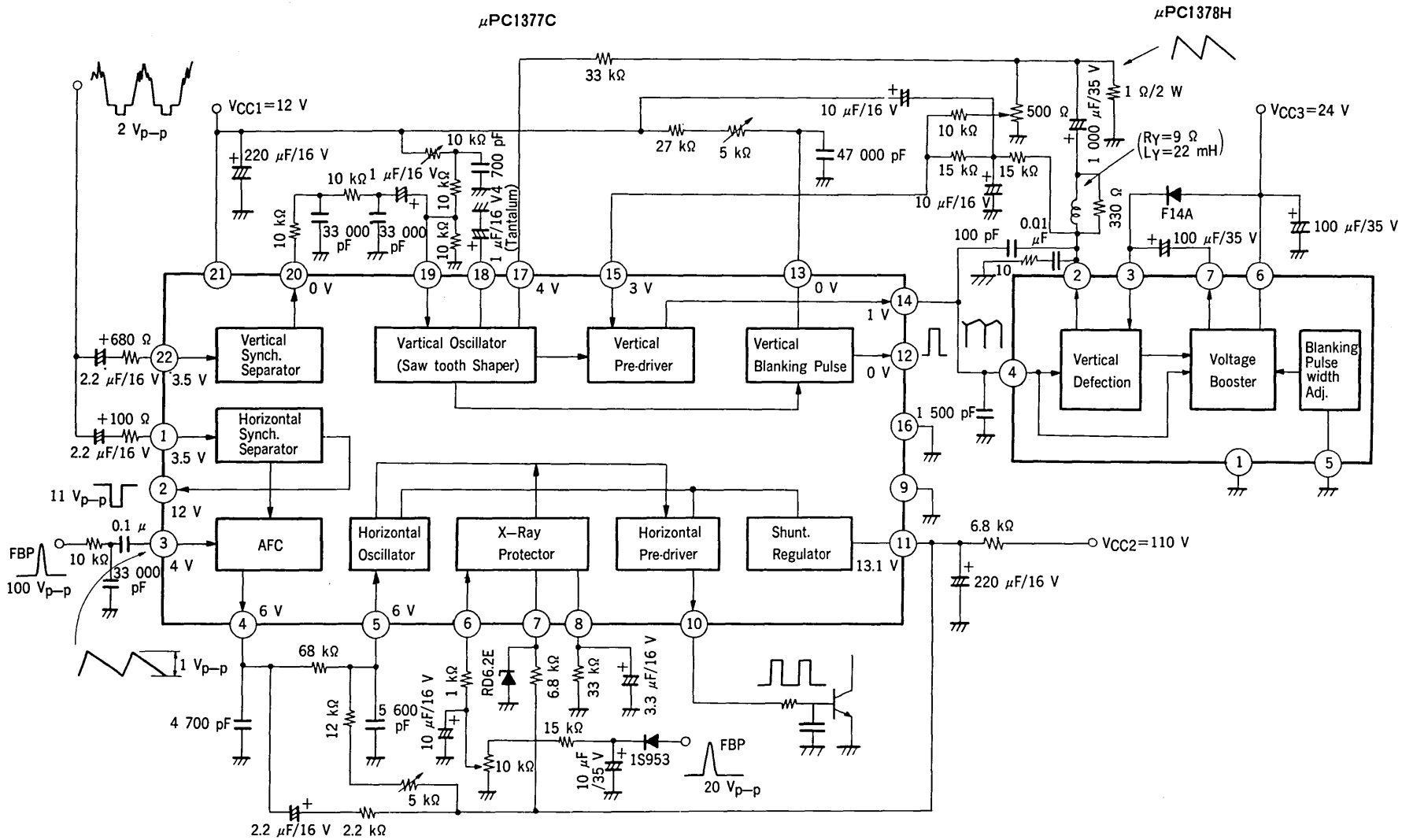
DRIFT OF HORIZONTAL OSCILLATION AGAINST POWER SUPPLY VOLTAGE



DRIFT OF HORIZONTAL OSCILLATION AGAINST TEMPERATURE



TYPICAL APPLICATIONS



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1378H

VERTICAL DEFLECTION CIRCUIT OF COLOR TV

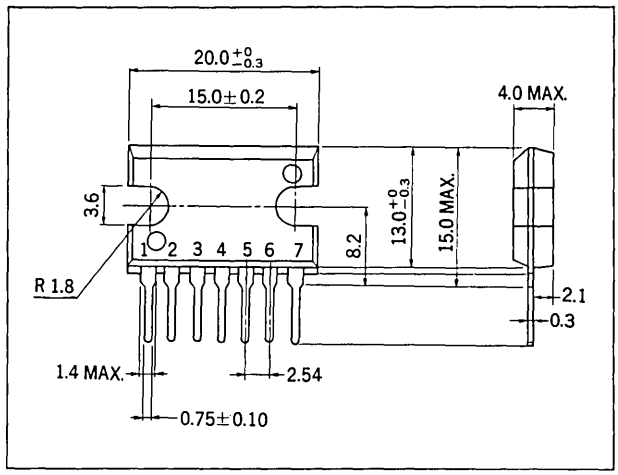
The μPC1378H is a vertical deflection circuit suitable for color CRTs from 9 inches 90° deflection angle to 20 inches 100° deflection angle.

It is available for any color TV using IC or descrete components in the vertical ramp generator.

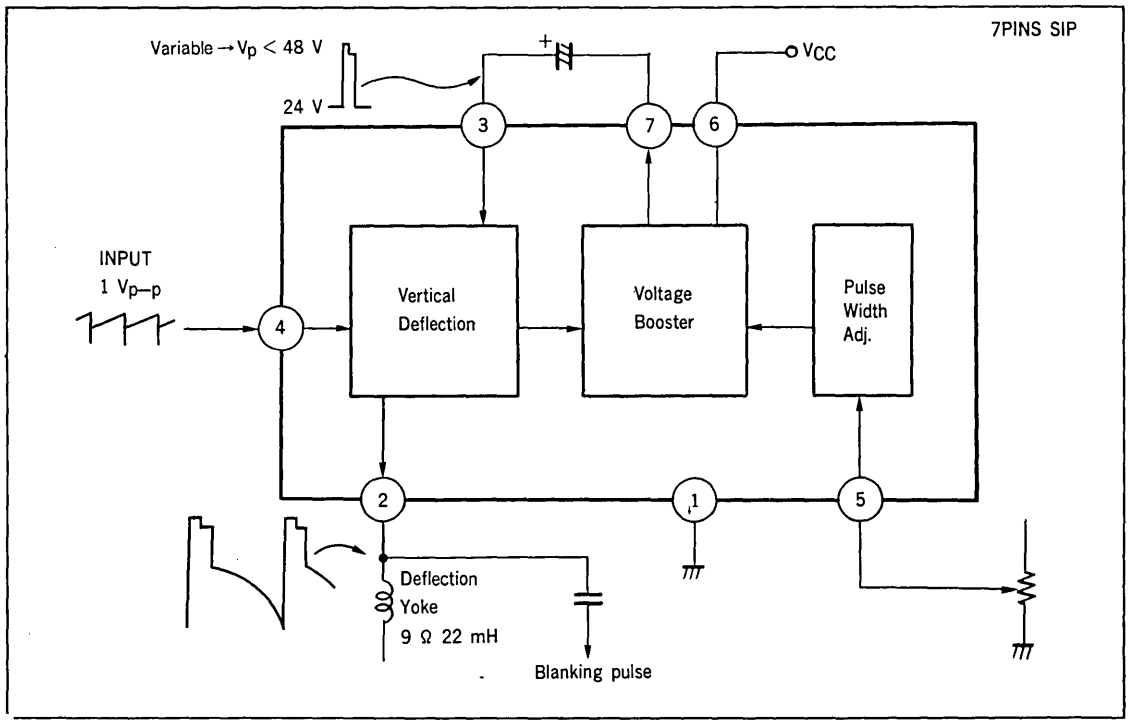
FEATURES

- The voltage booster circuit realizes particular high efficiency (24 V, 170 mA at 20 inches 100 degrees deflection angle set).
- Able to couple with any ramp generator, as it needs only ramp signal.
- Blanking pulse width is variable with a external bias circuit.

PACKAGE DIMENSIONS (Unit : mm)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Power Supply Voltage	V_{CC} (V_6)	27	V
Power Supply Current Drain	I_{CC}	350	mA
Terminal 3 Voltage	V_3	60	V
Input Voltage	V_4	2.5	V
Pulse Adjust Voltage	V_5	V_6	V
Output Current	I_{DEF} (I_2)	−1.1 to +1.1	A_{peak}
Booster Output Current	I_7	−1.1 to +0.2	A_{peak}
Terminal 7 Voltage	V_7	V_6	V
Power Dissipation	P_D	4.5 W (T_c=129 °C)	W
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +150	°C
Junction Temperature	T_j	+150	°C
Thermal Resistance	$R_{th(j-c)}$	4.5 (T_c=25 °C)	°C/W
Thermal Resistance	$R_{th(j-a)}$	43 (T_a=25 °C)	°C/W

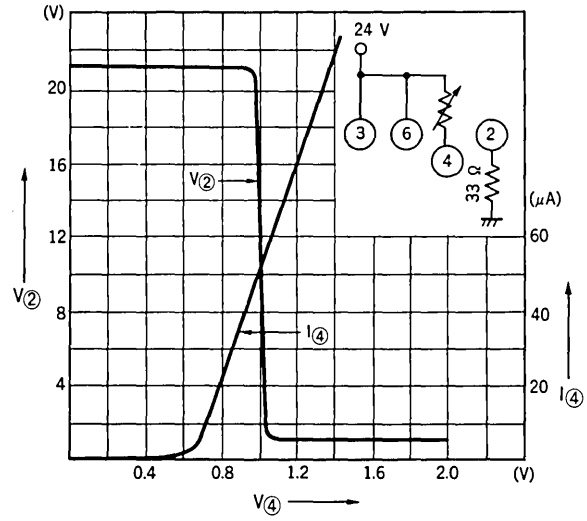
ELECTRICAL CHARACTERISTICS (T_a=25 °C, V_{CC}=24 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	PIN	CONDITION
Power Supply Current Drain	I_{CC}	165	200	240	mA	3+6	Standard Operation
Output Current	I_{DEF}	1.1	1.2	1.3	A	2	Standard Operation
Output DC Voltage	V_{ODC}	11.0	11.5	12.0	V	2	Standard Operation
Retrace Pulse Voltage–1	$V_{2p(1)}$	46	49	54	V	2	V_5=0 V
Retrace Pulse Voltage–2	$V_{2p(2)}$	38	42	45	V	2	V_5=8 V
Retrace Pulse Width–1	$T_{2p(1)}$	790	950	1150	μs	2	V_5=0 V
Retrace Pulse Width–2	$T_{2p(2)}$	960	1160	1400	μs	2	V_5=8 V
Idling Current	I_Q	20	35	50	mA	3	I_3, No Output
Booster Charging Saturation	V_{S7-1}		1.5	2.0	V	7	24 V – 2 MΩ – Pin 4 24 V – 1.2 kΩ – Pin 7
Booster Discharging Saturation	V_{S6-7}	1.5	2.5	4.0	V	7	Pin 4 = Open Pin 7 – 33 Ω – GND.
Booster Charging Current–1	$I_{7(1)}$	60	90	120	mA	7	24 V – 2 MΩ – Pin 4
Booster Charging Current–2	$I_{7(2)}$	60	90	120	mA	7	V_4=1.0 V
Output Saturation–1	$V_{S2-1(1)}$		0.9	1.5	V	2	24 V – 220 kΩ – Pin 4 24 V – 33 Ω – Pin 2
Output Saturation–2	$V_{S2-1(2)}$		0.9	1.5	V	2	V_4 = 2.0 V 24 V – 33 Ω – Pin 2
Output Saturation–3	V_{S3-2}	2.0	3.0	4.5	V	2	Pin 4 = Open Pin 2 – 33 Ω – GND.
Input Saturation	V_{S4}	0.5	1.0	2.5	V	4	24 V – 220 kΩ – Pin 4
Voltage Gain	A_{VO}		70		dB		f_{in}=1 kHz, R_L=1 Ω
Input Resistance	R_{in}		7		kΩ	4	V_{4DC}=1.1 V

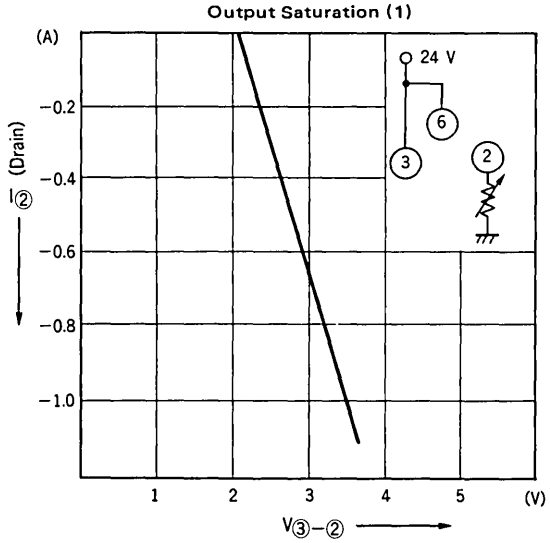
TYPICAL CHARACTERISTICS (T_a=25 °C)

1. Deflection Amplifier

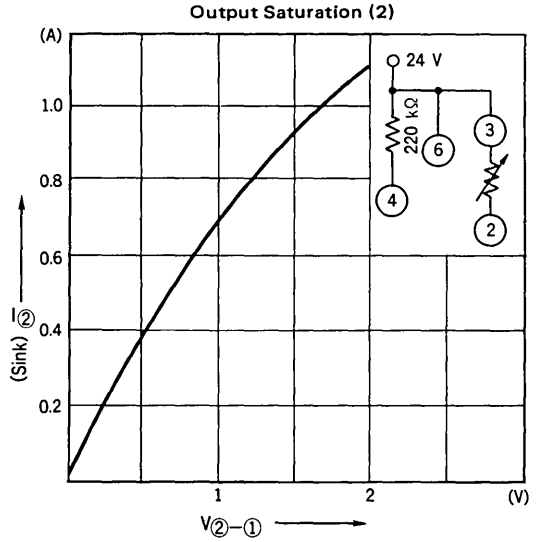
Input–Output Characteristic



Output Saturation (1)

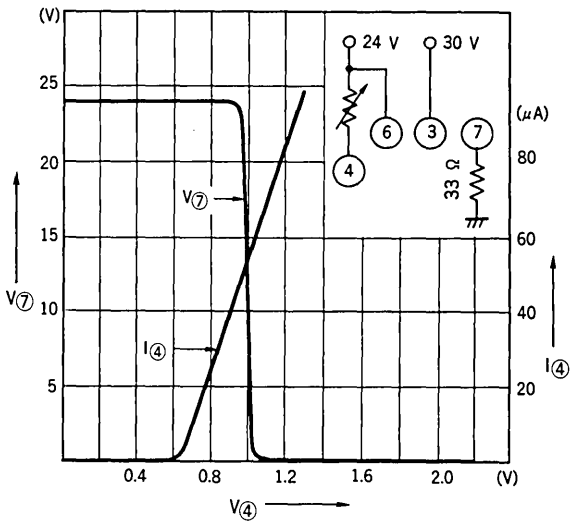


Output Saturation (2)

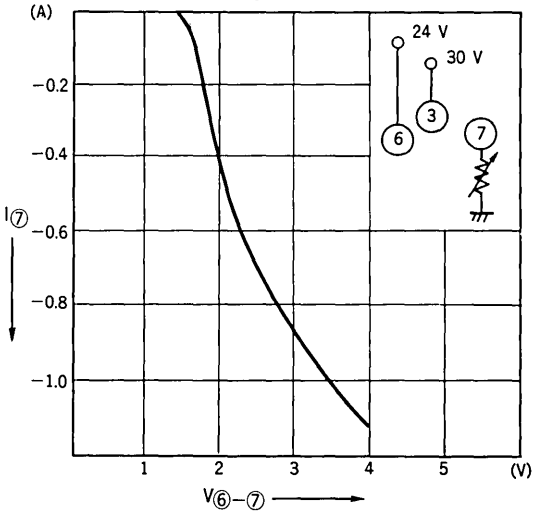


2. Voltage Booster

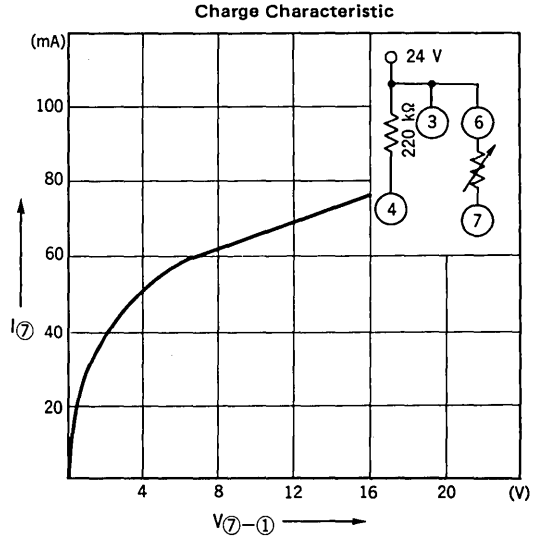
Input–Output Characteristic



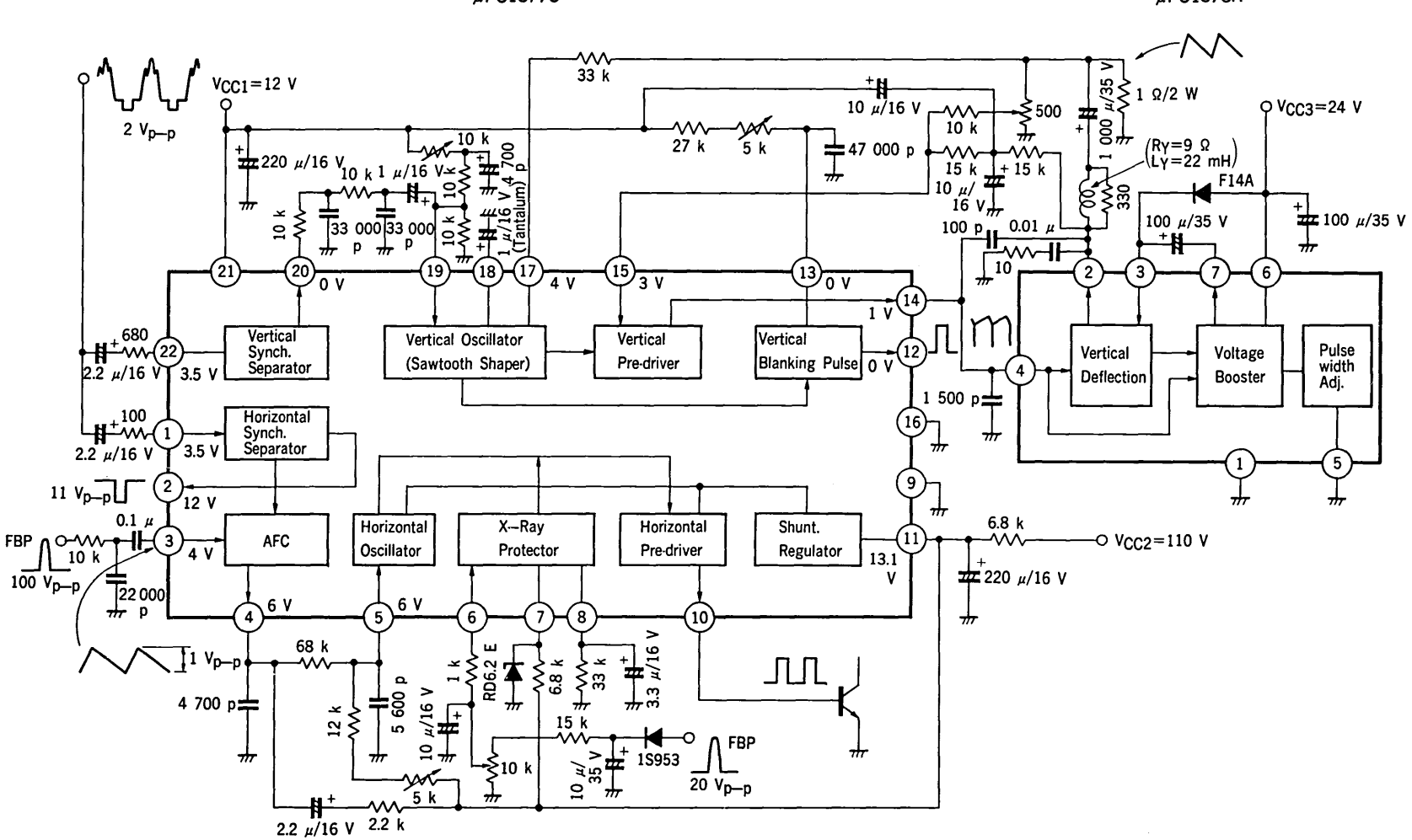
Discharge Characteristic



Charge Characteristic



APPLICATIONS



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1379C

SYNCHRONIZATION SIGNAL PROCESSOR FOR B/W TV AND SMALL-SIZED COLOR TV

μPC 1379C is a bipolar analog integrated circuit designed for mono-chrome TV and small size color TV.

It contains synchronous signal separator, vertical deflection signal generator, vertical power stage, and horizontal deflection signal generator in a molded 16 pins dual in-line package.

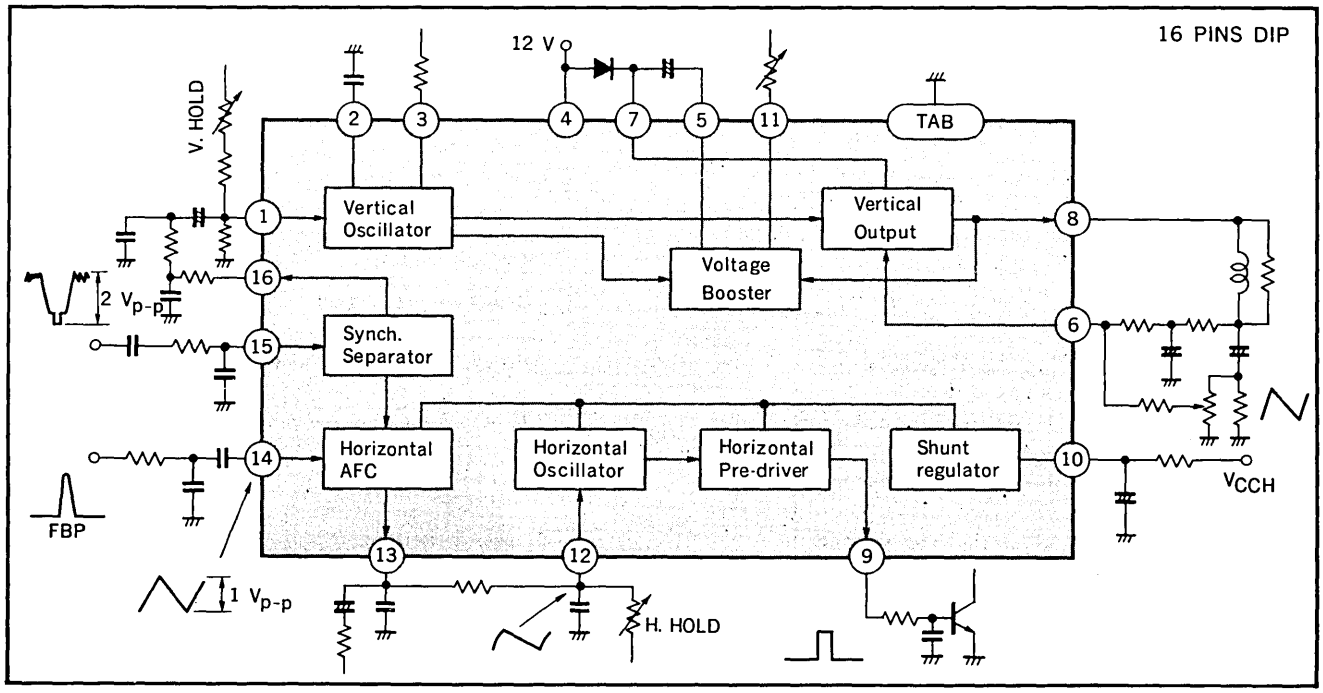
The package has a tab attaching to the end.

The vertical stage reduces the power consumption remarkably by the built-in voltage booster circuit. The horizontal signal part can take the working power from any voltage power supply higher than 8 volts, as it equips shunt type power regulator itself. So, it can take the power even from 110 volt power line through only one resistor.

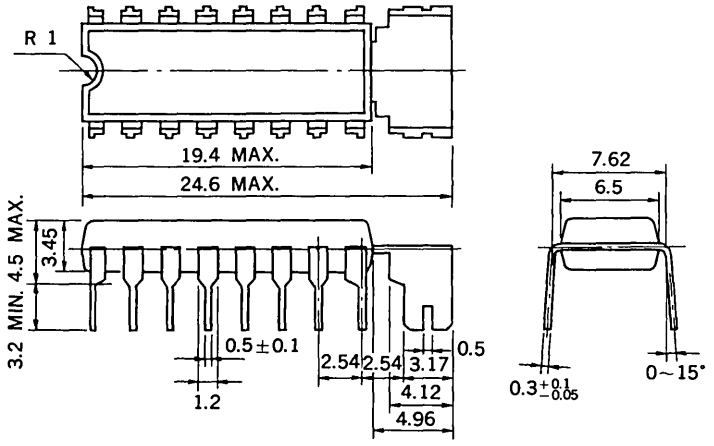
FEATURES

- Built-in vertical power stage remarkably low power vertical deflection realized by the built-in voltage booster.
- Vertical fly-back pulse width is freely adjustable by the exclusive terminal.
- Any supply voltage is available for the horizontal part, as it equips shunt type power regulator itself.

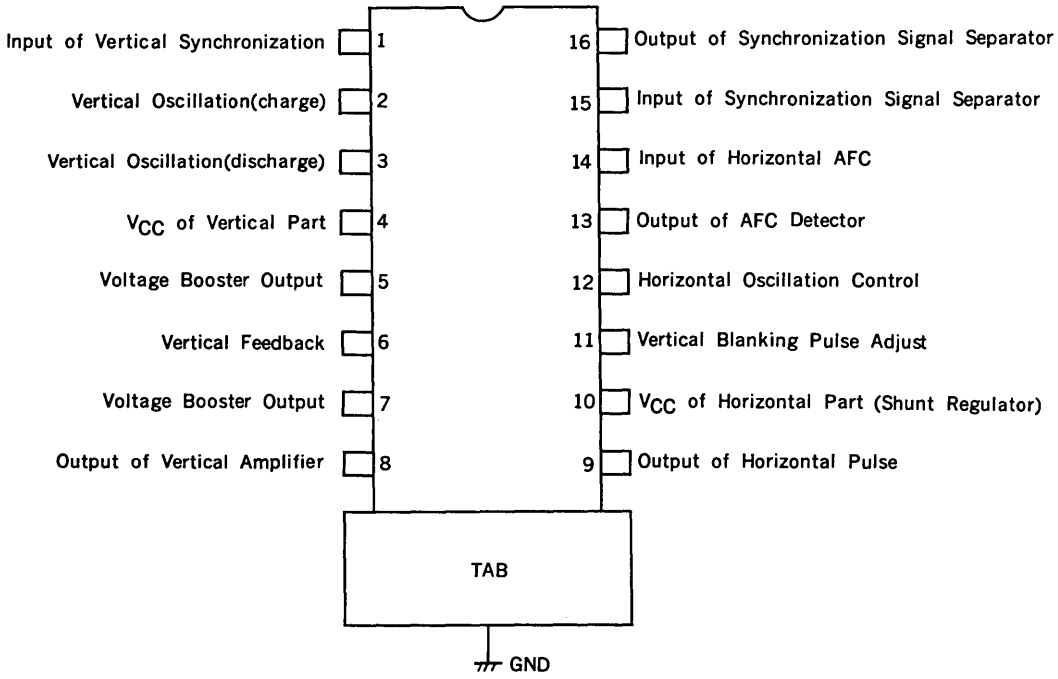
BLOCK DIAGRAM



PACKAGE DIMENSIONS (Unit : mm)



CONNECTION DIAGRAM (Top View)



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

(Mark(+) of current expresses that the current is flowing into the terminal. Mark(−) of current expresses that the current is flowing out from the terminal.)

Power Supply Voltage for Vertical Part	V_4	15	V
Power Supply Current for Horizontal Part	I_{10}	30	mA
Video Input Voltage	V_{15}	V_4	V
Synch Output Current	I_{16}	−10 to +10	mA
Voltage Booster Charge Voltage	V_{11}	V_4	V
Booster Output Current	I_5	−500 to +150	mApeak
Deflection Current	I_8	−500 to +150	mApeak
Vertical Feedback Voltage	V_6	V_4	V
AFC Input Voltage	V_{14}	V_{10}	V
Horizontal Output Current (Pulse)	I_9	−5 to +5	mA
Power Dissipation	P_D	1.3 (T_{tab} = 98 °C)	W
Thermal Resistance (J-tab)	$R_{th(j\text{-}tab)}$	40 (T_{tab} = 25 °C)	°C/W
Thermal Resistance (J-a)	$R_{th(j\text{-}a)}$	70 (T_a = 25 °C)	°C/W
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +150	°C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power Supply Voltage for the Vertical Part	V_4	9.6	12	14.4	V
Deflection Current	I_{DEF}	400	500	600	mAp-p
Power Supply Current for Horizontal Part	I_{10}	6.5	12	18	mA

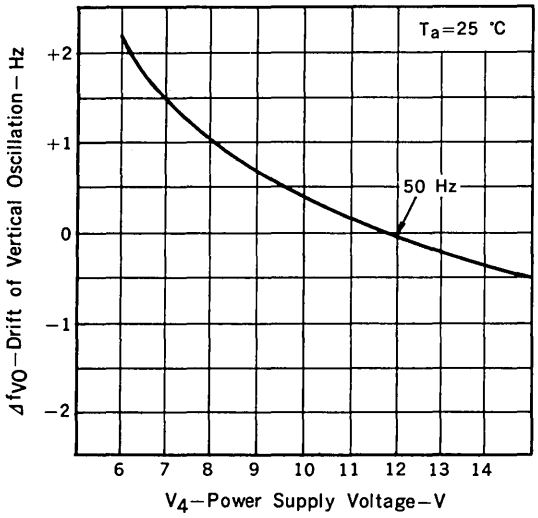
ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V_4 = 12 V, I_{DEF} = 500 $mA_{p\text{-}p}$, I_{10} = 12 mA)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Power Supply Current for Vertical Part	$I_{4(1)}$		85	100	mA	standard circuit
Power Supply Current for Vertical Part	$I_{4(2)}$	6	12	20	mA	standard circuit (Idling Current)
Vertical Free-running Frequency	f_{VO}	46	50	54	Hz	standard circuit
Drift of Vertical Free-running Frequency	$\Delta f_{VO}(V_{CC})$		0.8	2.0	Hz	$\Delta f_{VO}(V_{CC}) = \lvert f_{VO}(9.6\ V) - f_{VO}(14.4\ V) \rvert$
Drift of Vertical Free-running Frequency	$\Delta f_{VO}(T_a)$		1.5	2.0	Hz	$\Delta f_{VO}(T_a) = \lvert f_{VO}(-20\ °C) - f_{VO}(+75\ °C) \rvert$
Vertical Synchronizing Capture Frequency	f_{PV}	47	50		Hz	$f_{V(in)}$ = 60 Hz
Middle Voltage of Vertical Output	V_{MID}	5.3	5.8	6.3	V	standard circuit
Flyback Pulse Peak Voltage	RPV	20	23	26	V	standard circuit
Flyback Pulse Width	RPW	790	850	910	μs	standard circuit
Deflection Current	I_{DEF}	450	500	550	$mA_{p\text{-}p}$	standard circuit
Supply Voltage for Horizontal Part	V_{10}	6.2	6.7	7.2	V	I_{10} = 12 mA
Horizontal Free-running Frequency	f_{HO}	15.0	15.75	16.5	kHz	standard circuit
Drift of Horizontal Free-running Frequency	$\Delta f_{HO}(T_a)$		190	250	Hz	$\Delta f_{HO}(T_a) = \lvert f_{HO}(-20\ °C) - f_{HO}(+75\ °C) \rvert$
Horizontal Output Pulse Width	PWH	23	25	27	μs	standard circuit
Horizontal Output Current	I_9	0.8	1.3	2.0	mA	standard circuit
Horizontal Synchronizing Capture Freq.	f_{PH}	±650	±900	±1150	Hz	standard circuit
Horizontal AFC Output Current	I_{13}	0.28	0.45	0.74	mA	standard circuit
Gain of AFC Detector	μ	89	143	236	μA/rad	standard circuit
Efficiency of Horizontal Oscillation Control	β	66	72	78	Hz/μA	standard circuit

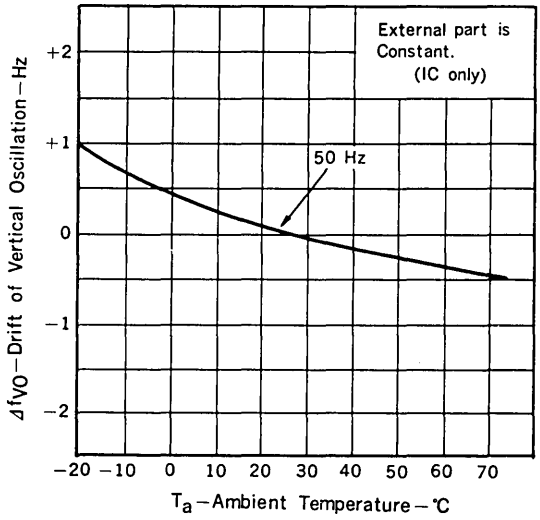
TYPICAL CHARACTERISTICS (T_a = 25 °C)

1. Vertical part

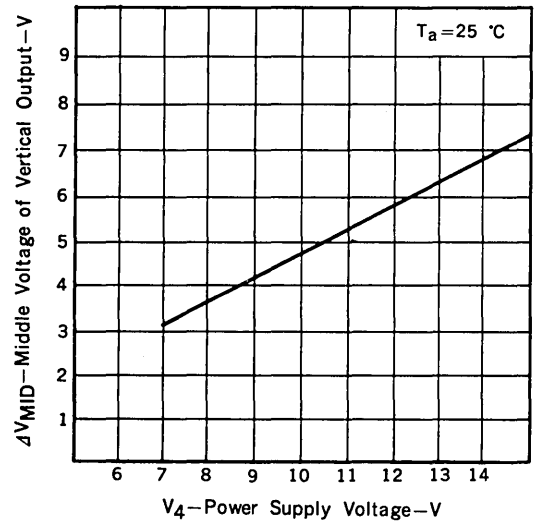
DRIFT OF VERTICAL OSCILLATION AGAINST POWER SUPPLY VOLTAGE



DRIFT OF VERTICAL OSCILLATION AGAINST AMBIENT TEMPERATURE

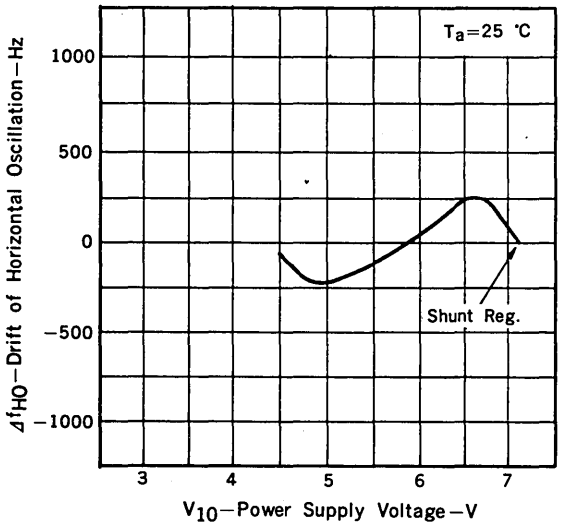


DRIFT OF VERTICAL MIDDLE VOLTAGE AGAINST POWER SUPPLY VOLTAGE

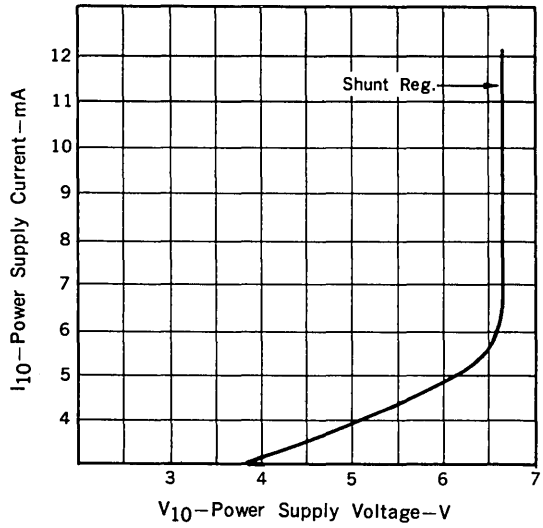


2. Horizontal part

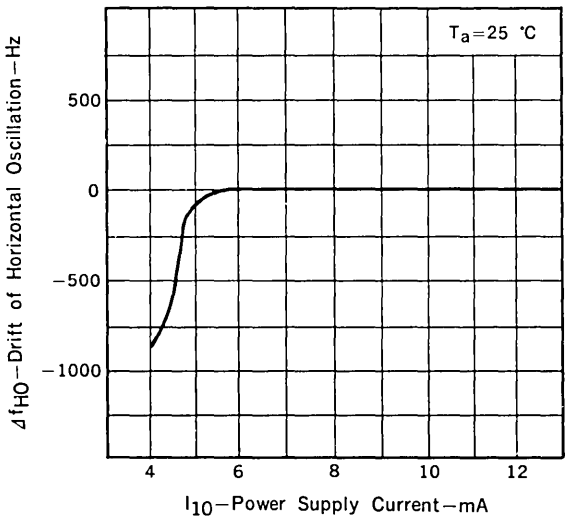
DRIFT OF HORIZONTAL OSCILLATION AGAINST POWER SUPPLY VOLTAGE



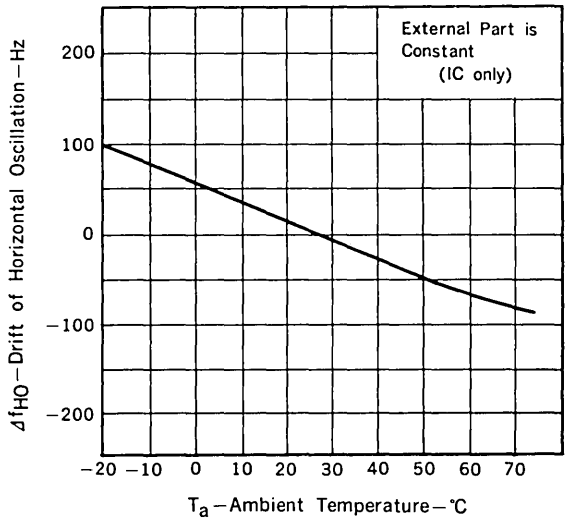
HORIZONTAL POWER SUPPLY CURRENT VERSUS VOLTAGE



DRIFT OF HORIZONTAL OSCILLATION AGAINST POWER SUPPLY CURRENT

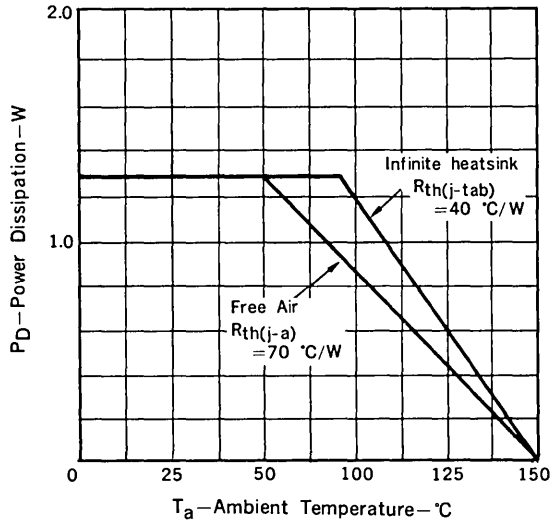


DRIFT OF HORIZONTAL OSCILLATION AGAINST TEMPERATURE

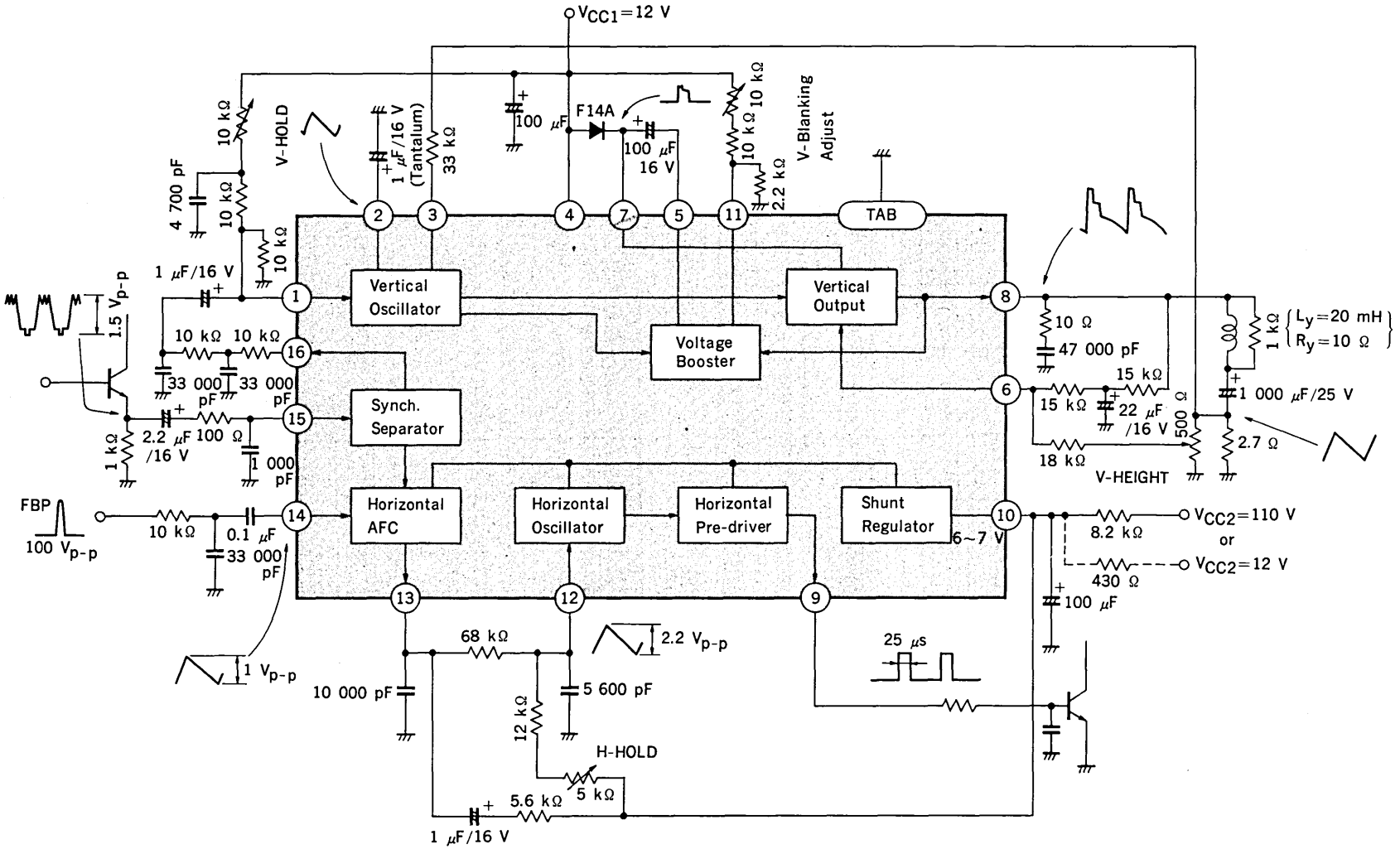


3. $P_D - T_a$ Characteristic

POWER DISSIPATION vs. AMBIENT TEMPERATURE



APPLICATION CIRCUIT



INDEX

BIPOLAR DIGITAL INTEGRATED CIRCUIT
μPB553AC

150MHz DIVIDE-BY-16/17 LOW POWER PRESCALER

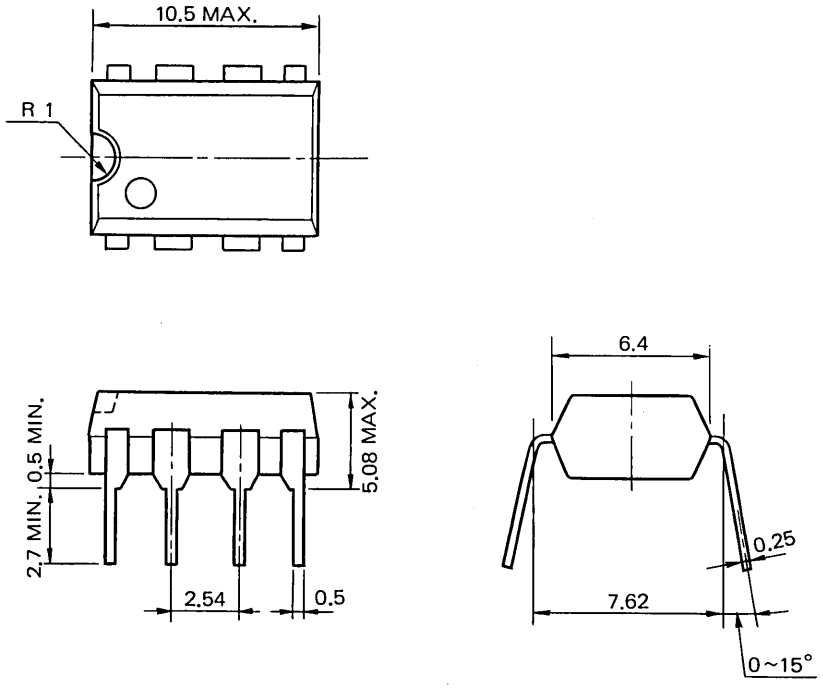
DESCRIPTION

The μPB553AC is a VHF two-modulus prescaler intended for use in PLL Digital Tuning Systems in conjunction with μPD1700 series. Advanced bipolar process technology is utilized to realize high frequency operation with extremely low power consumptions. The device provides ÷16 and ÷17 division ratio for NEC's original pulse swallowing method, and is guaranteed to operate up to 130 MHz over the −35 °C to +75 °C temperature range with a V_{CC} variation from +4.5 V to +5.5 V. An included amplifier allows it to be operated with small amplitude signal of 150 mVp-p.

FEATURES

- High frequency operation: 150 MHz (÷16)
  130 MHz (÷17)
- NEC's original pulse swallowing operation: ÷16/÷17
- Small input amplitude: Vin = 150 m Vp-p (MIN.)
- Single supply voltage: V_{CC} = 5.0 V ±10 %
- Low supply current: I_{CC} = 8.9 mA (TYP.)
- Incorporated buffer amplifier: V_O=1.2 Vp-p (TYP.)
- Small package: 8 pin plastic dual in-line package (DIP)

PACKAGE DIMENSIONS (Unit: mm)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{CC}	−0.5 to 6.0	V
Input Voltage	V_i	−0.5 to V_{CC}	V
Output Current	I_O	10	mA
Junction Temperature	T_j	+125	°C
Storage Temperature	T_{stg}	−55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

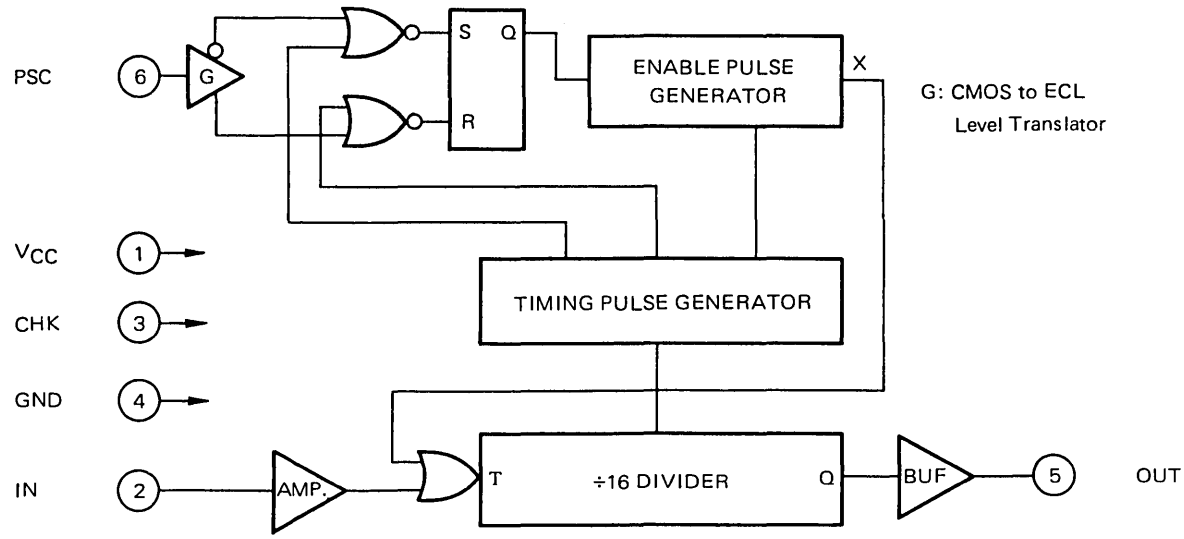
Supply Voltage Range	V_{CC}	4.5 to 5.5	V
Ambient Temperature	Ta	−35 to +75	°C
Output Load Capacitance	C_L	less than 10 picofarad	

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ±10 %, Ta = −35 to +75 °C)

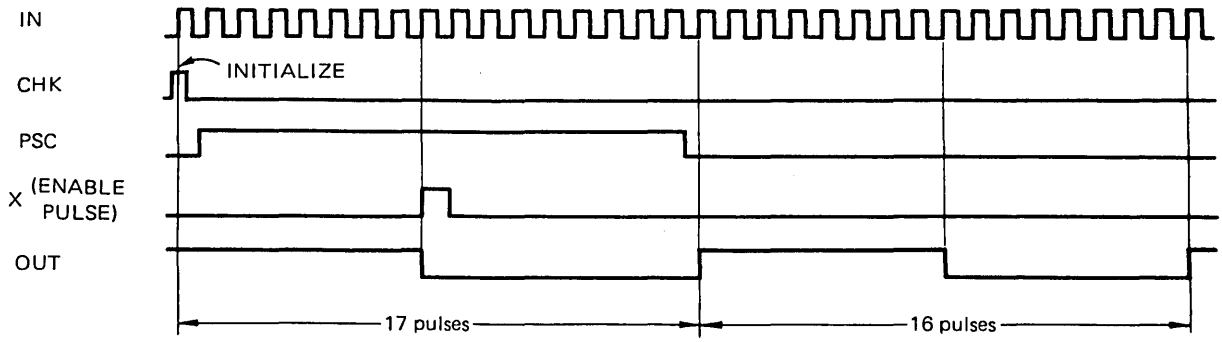
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Power Supply Current	I_{CC}		8.9	12.7	mA	V_{CC} = 5.0 V
Power Consumption	P_C		44.5		mW	Ta = 25 °C
Frequency Response	fin	1.0		150	MHz	Vin ≧ 0.15 Vp-p, ÷16
Frequency Response	fin	1.0		130	MHz	Vin ≧ 0.15 Vp-p, ÷17
Output Voltage	V_O	0.9	1.2		Vp-p	OUT terminal
Input Voltage	V_{in}	0.15		2.0	Vp-p	IN terminal
High Level Input Voltage	V_{IH}	0.8V_{CC}			V	PSC terminal
Low Level Input Voltage	V_{IL}			0.2V_{CC}	V	PSC terminal

Note: CHK terminal should be connected to GND.

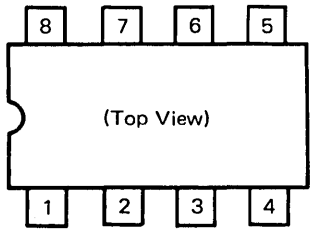
BLOCK DIAGRAM (Top View)



TIMING CHART



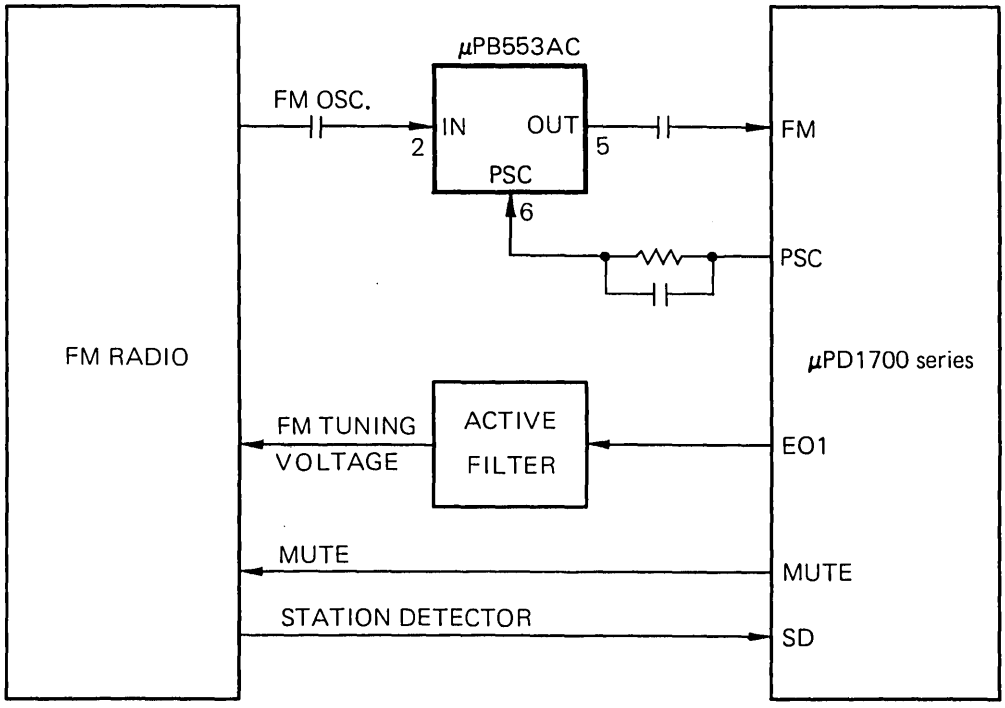
CONNECTION DIAGRAM



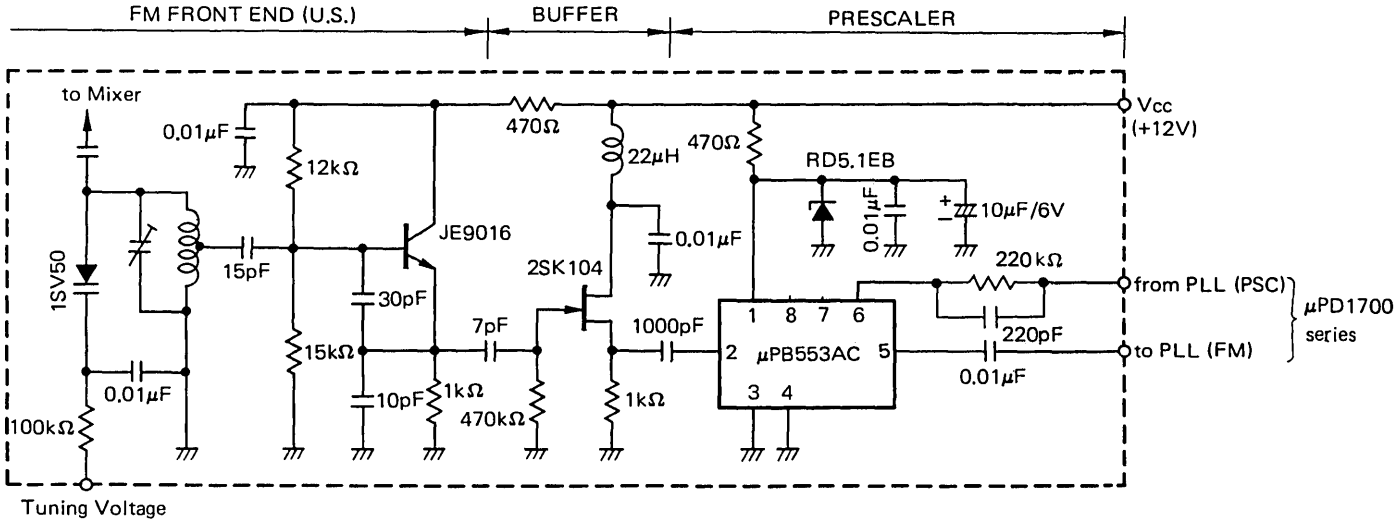
Pin Number	Symbol	Function
1	V_{CC}	Power Supply (V_{CC})
2	IN	Signal Input
3	CHK	Check (Normally to GND)
4	GND	GND
5	OUT	Output
6	PSC	Division Ratio Control*
7	NC	No Connection
8	NC	No Connection

*: When PSC terminal fixed high or low level, the μPB553AC functions as a ÷/16 prescaler.

APPLICATION-1



APPLICATION-2



BIPOLAR DIGITAL INTEGRATED CIRCUIT

μPB556C

150 MHz DIVIDE-BY-16/17 LOW POWER PRESCALER

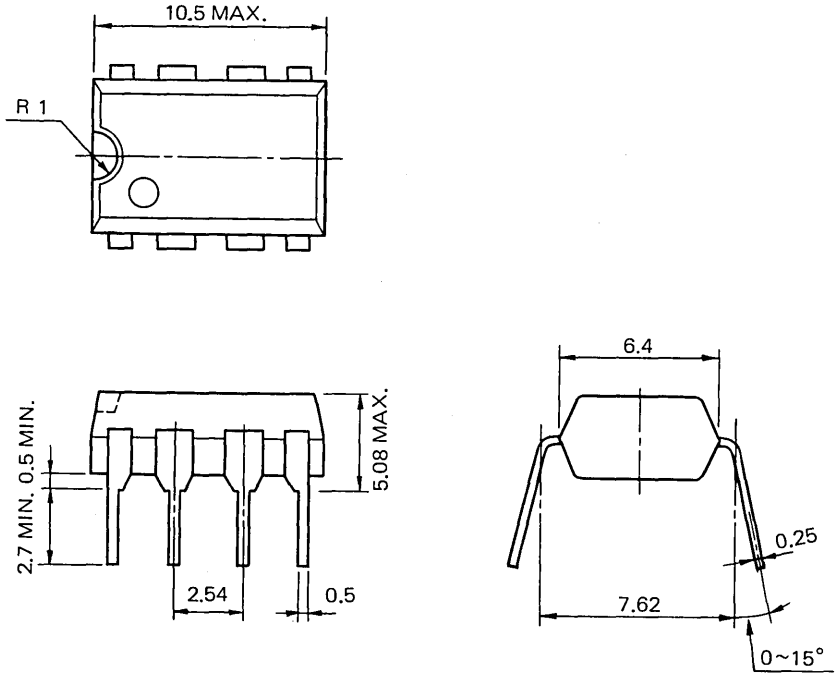
DESCRIPTION

The μPB556C is a VHF two-modulus prescaler intended for use in PLL Digital Tuning Systems in conjunction with μPD1700 series. Advanced bipolar process technology is utilized to realize high frequency operation with extremely low power consumptions. The device provides ÷16 and ÷17 division ratio for NEC's original pulse swallowing method, and is guaranteed to operate up to 130 MHz over the −35 °C to +75 °C temperature range with a V_{CC} variation from +2.55 V~+4.5 V. An included amplifier allows it to be operated with small amplitude signal of 150 mVp-p.

FEATURES

- High frequency operation: 150 MHz (÷16)
  130 MHz (÷17)
- NEC's original pulse swallowing operation: ÷16/÷17
- Small input amplitude: V_{in} = 150 m Vp-p (MIN.)
- Single supply voltage: V_{CC} = 2.55 V~4.5 V
- Low supply current: I_{CC} = 9.4 mA (TYP.)
- Incorporated buffer amplifier: V_O = 1.2 Vp-p (TYP.)
- Small package: 8 pin plastic dual in-line package (DIP)

PACKAGE DIMENSIONS (Unit: mm)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{CC}	−0.5 to 6.0	V
Input Voltage	V_i	−0.5 to V_{CC}	V
Output Current	I_O	10	mA
Junction Temperature	T_j	+125	°C
Storage Temperature	T_{stg}	−55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

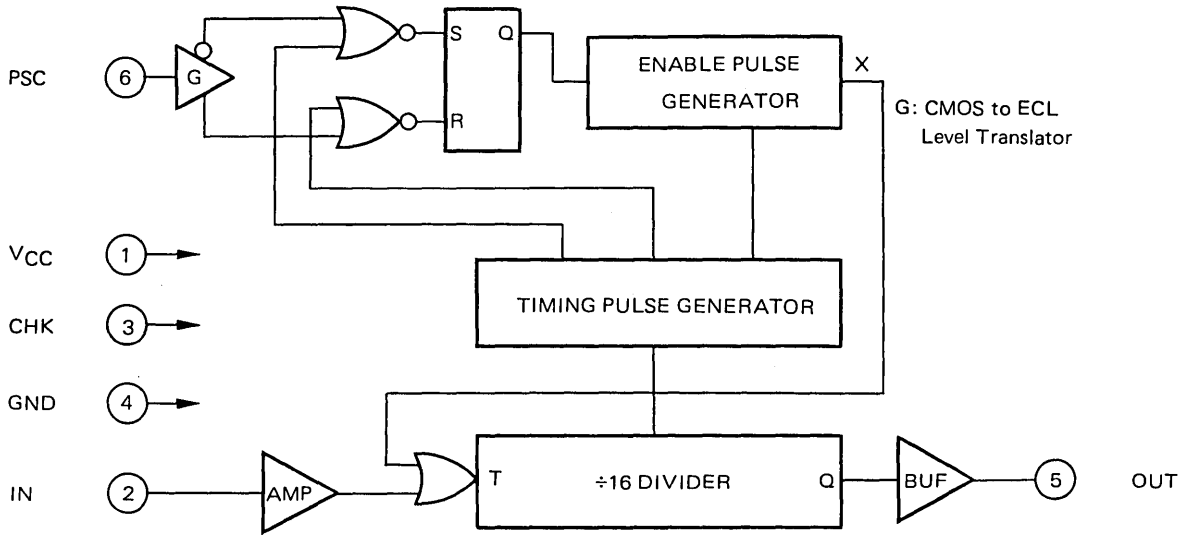
Supply Voltage Range	V_{CC}	2.55 to 4.5	V
Ambient Temperature	T_a	−35 to +75	°C
Output Load Capacitance	C_L	less than 10 pF	

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.55~4.5 V, T_a = −35 to +75 °C)

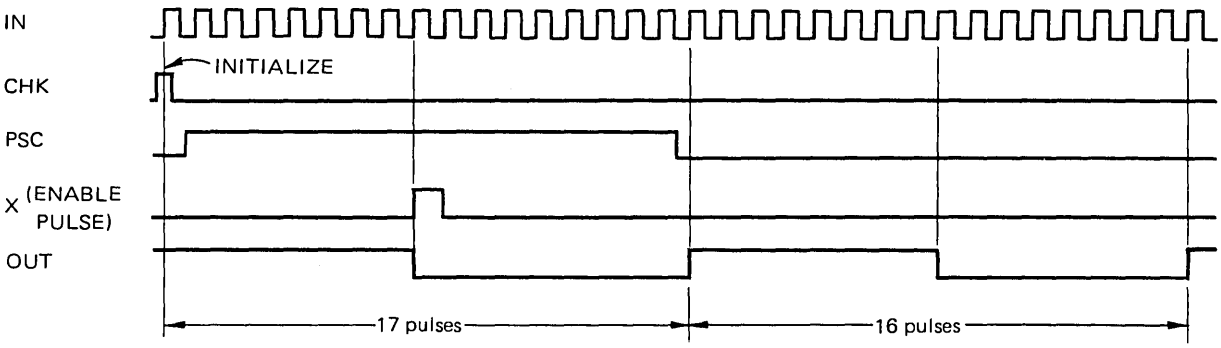
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Power Supply Current	I_{CC}		9.4		mA	V_{CC} = 5.0 V
Power Consumption	P_C		28		mW	T_a = 25 °C
Frequency Response	f_{in}	1.0		150	MHz	$V_{in} \geqq 0.15$ Vp-p, ÷16
Frequency Response	f_{in}	1.0		130	MHz	$V_{in} \geqq 0.15$ Vp-p, ÷17
Output Voltage	V_O	0.9	1.2		Vp-p	OUT terminal
Input Voltage	V_{in}	0.15		2.0	Vp-p	IN terminal
High Level Input Voltage	V_{IH}	0.8V_{CC}			V	PSC terminal
Low Level Input Voltage	V_{IL}			0.2V_{CC}	V	PSC terminal

Note: CHK terminal should be connected to GND.

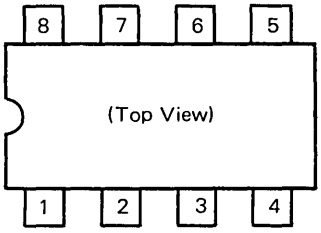
BLOCK DIAGRAM (Top View)



TIMING CHART



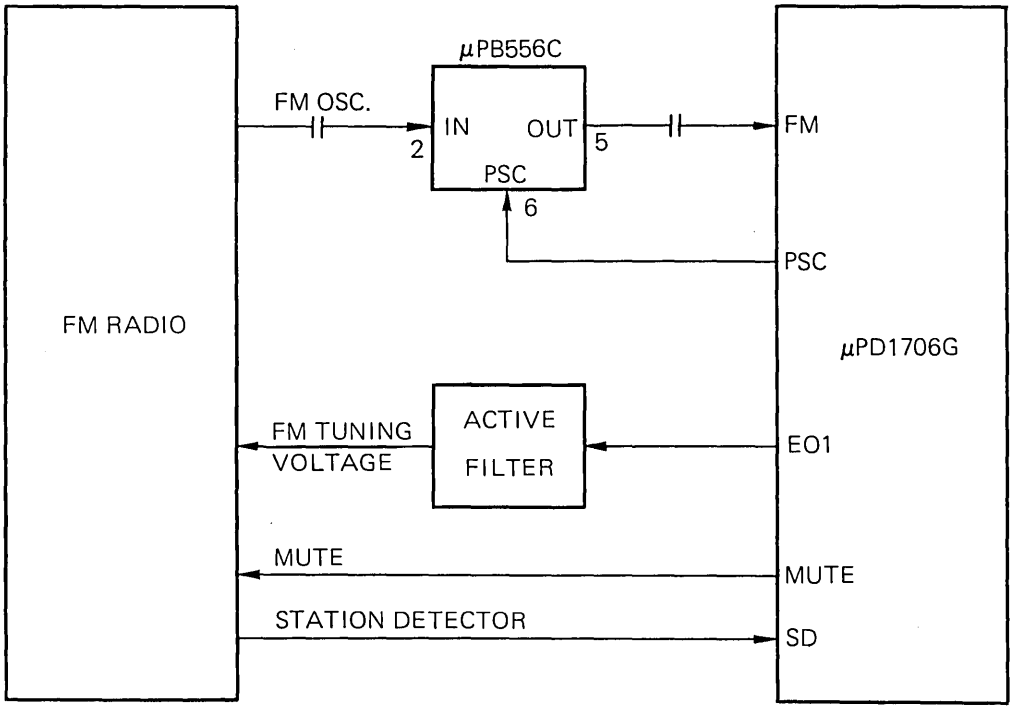
CONNECTION DIAGRAM



Pin Number	Symbol	Function
1	V_{CC}	Power Supply (V_{CC})
2	IN	Signal Input
3	CHK	Check (Connect to GND)
4	GND	GND
5	OUT	Output
6	PSC	Division Ratio Control*
7	NC	No Connection
8	NC	No Connection

*: When PSC terminal fixed high or low level, the μPB556C functions as a ÷/16 prescaler.

APPLICATION



BIPOLAR DIGITAL INTEGRATED CIRCUIT
μPB562C

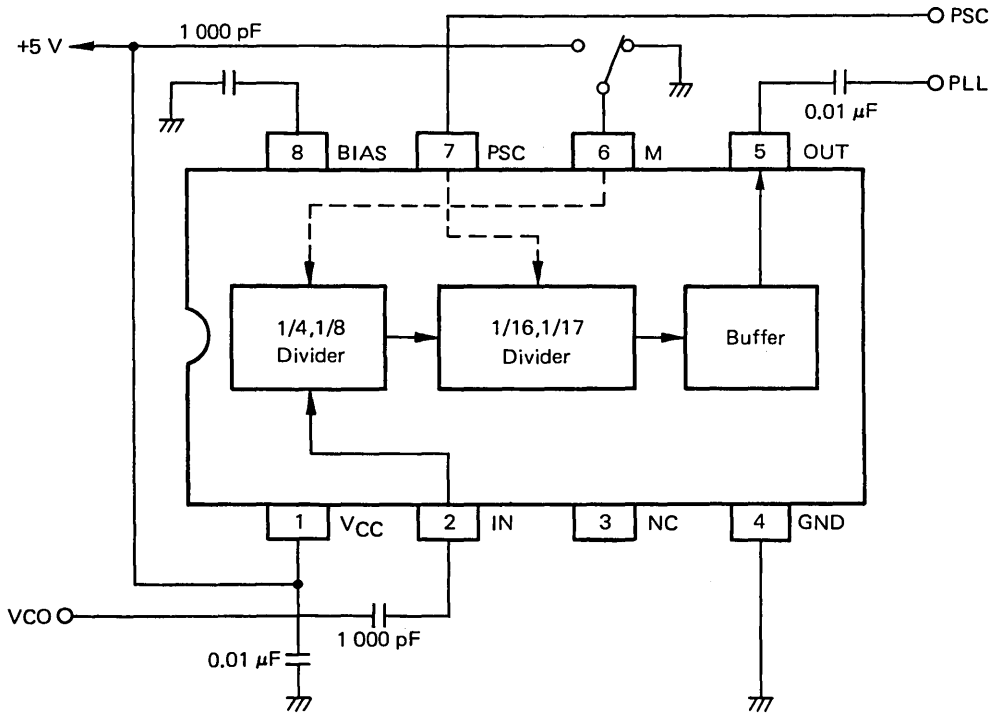
1 GHz DIVIDE-BY-128/136 LOW POWER PRESCALER

The μPB562C is a ECL two-modulus prescaler for operation at input frequency up to 1 GHz. It is intended for use in TV PLL Digital Tuning Systems with the μPD1700 series. This prescaler divides by either 128 or 136, as determined by the signal form the μPD1700 series (EX. μPD1703C-017) applied to the Pulse Swallow Control Input (PSC).

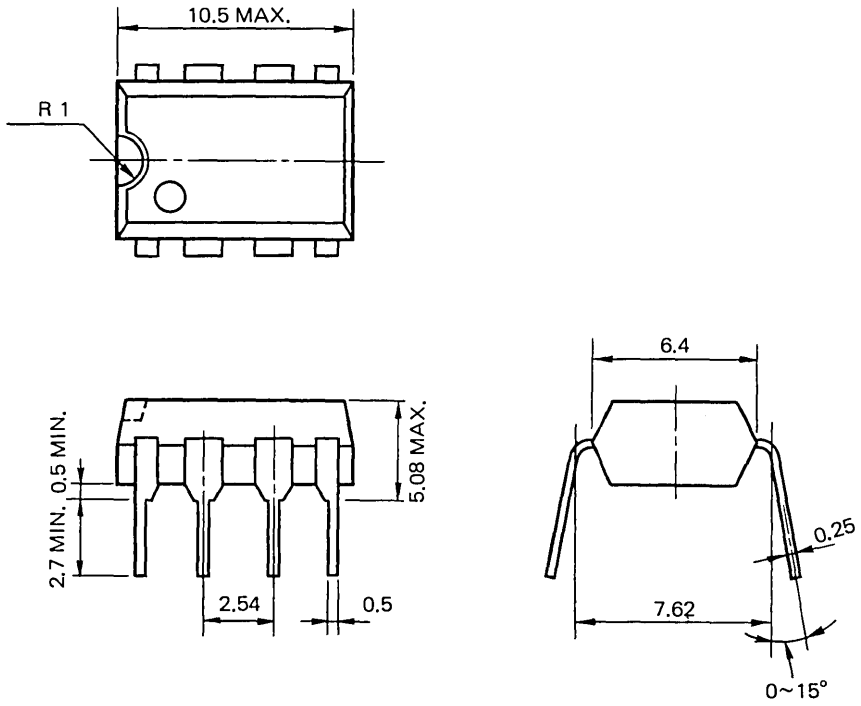
FEATURES

- High frequency operation : 1 GHz
- Dual mode operation with NEC's original pulse swallowing method
  - 128/136 ..... up to 1 GHz
  - 64/68 ..... up to 500 MHz
- Single supply voltage : V_{CC} = 5.0 V ± 10 %
- Low supply current : I_{CC} = 23.0 mA (TYP.)
- Incorporated buffer amplifier : Vo = 1.2 Vp-p (TYP.)
- Small package : 8 pin plastic dual in-line package (DIP)

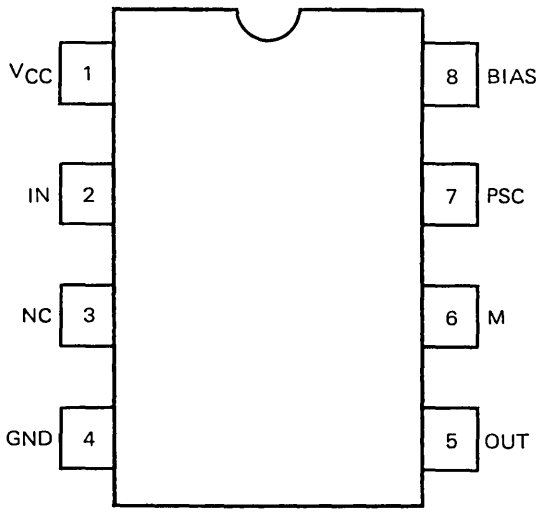
BLOCK DIAGRAM



PACKAGE DIMENSIONS (Unit: mm)



CONNECTION DIAGRAM (Top View)



1	V_{CC}	Power Supply (+5 V)
2	IN	Signal Input
3	NC	
4	GND	Ground
5	OUT	Signal Output
6	M	Division Ratio Control (V_{CC}: 64/68, GND: 128/136)
7	PSC	Pulse Swallow Control
8	BIAS	Bias

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{CC}	−0.5 to 6.0	V
Input Voltage	Vin	−0.5 to V_{CC} +0.5	V
Output Current	Io	−10.0	mA
Storage Temperature	Tstg	−55 to +125	°C

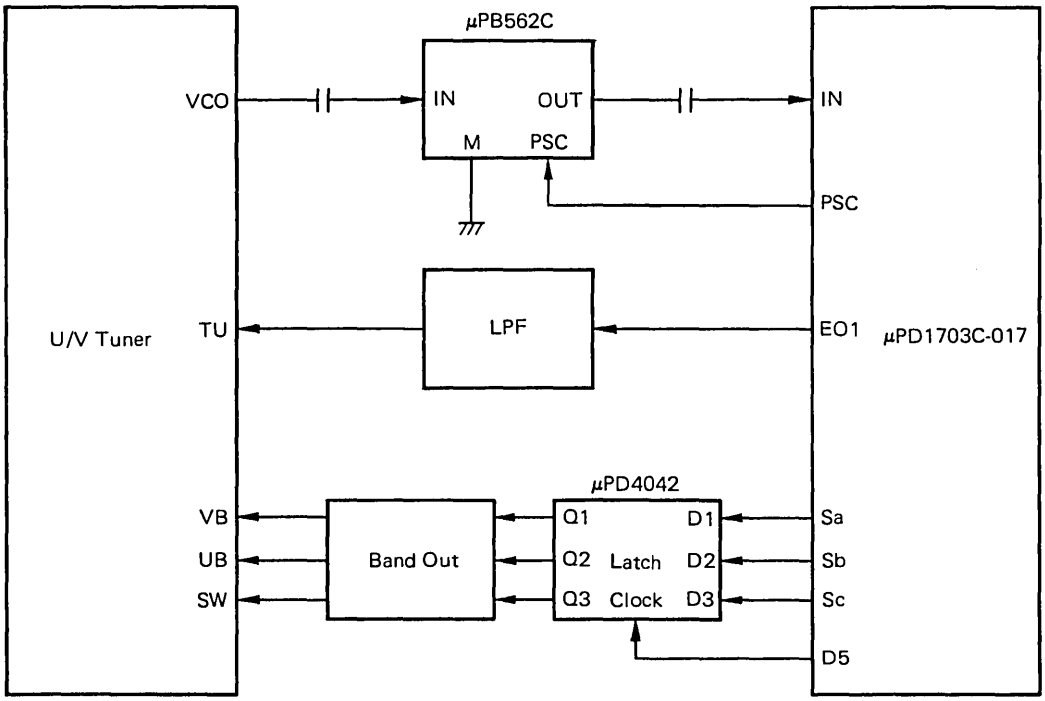
RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range		4.5 to 5.5	V
Ambient Temperature	Ta	−35 to +75	°C
Output Load Capacitance	CL	Less than 30 pF	

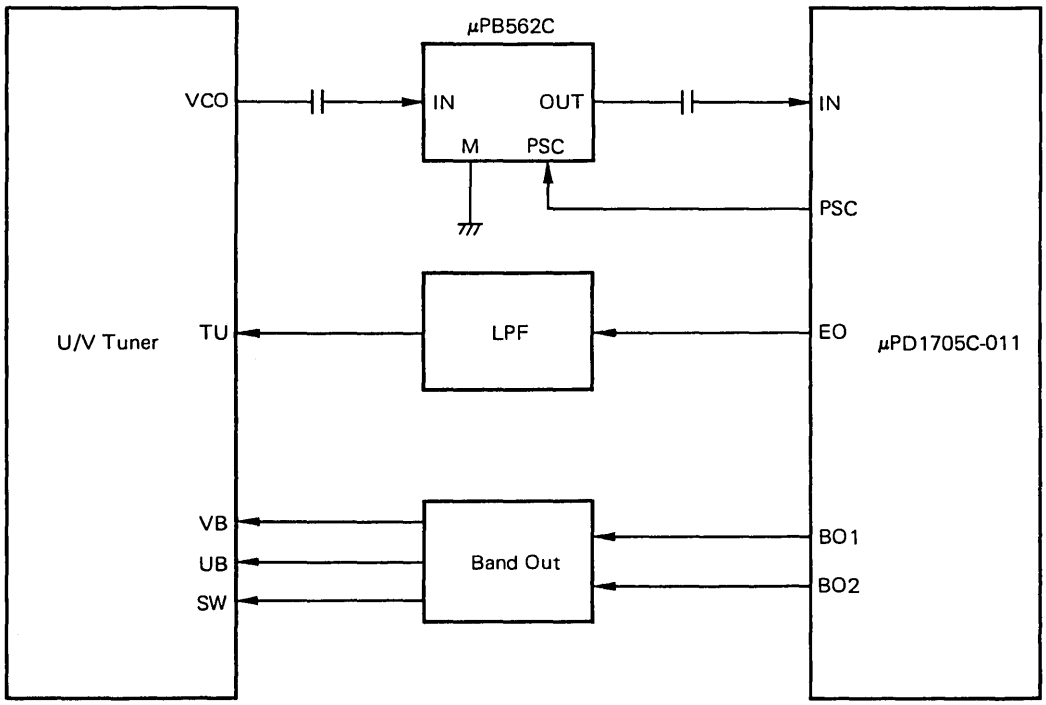
ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ±10 %, Ta = −35 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Power Supply Current	I_{CC}		23.0	30.0	mA	V_{CC}=5.0 V, Ta=25 °C
Output Voltage	V_o	1.0	1.2		Vp-p	OUT terminal
Input Voltage	V_{in}	0.4		1.5	Vp-p	IN terminal
High Level Input Voltage	V_{IH}	0.7V_{CC}			V	PSC terminal
Low Level Input Voltage	V_{IL}			0.3 V_{CC}	V	PSC terminal
High Level Input Current 1	$I_{IH\,1}$			10.0	μA	PSC terminal
High Level Input Current 2	$I_{IH\,2}$			40.0	μA	M terminal
Frequency Response 1	$f_{in\,1}$	100		1000	MHz	$V_{in} \geqq 0.4$Vp-p, M=GND
Frequency Response 2	$f_{in\,2}$	100		500	MHz	$V_{in} \geqq 0.4$Vp-p, M=V_{CC}

APPLICATION 1



APPLICATION 2



MOS DIGITAL INTEGRATED CIRCUIT
μPD1701C-011

PHASE LOCKED LOOP FREQUENCY SYNTHESIZER
LW/MW/FM DIGITAL TUNING SYSTEM CONTROLLER
CMOS LSI

DESCRIPTION

The μPD1701C-011 is a single chip CMOS LSI designed for using as a PLL Frequency Synthesizer Digital Tuning System Controller.
The μPD1701C-011 is packaged in a 28 pin slim dual in-line package (DIP).

FEATURES

- Clock, PLL and Controller is realized in a single chip.
- LW, MW and FM bands for Europe
- High reference frequency (FM: 25 kHz) It results in a high carrier to noise ratio.
- External programmable IF offset for FM band (10.650 MHz, 10.675 MHz, 10.700 MHz, 10.725 MHz)
- High speed and low power consumption due to CMOS.
- Stand-by mode . . .supply current I_{DD} = 0.5 mA (TYP.)
- Display brightness control (DIMMER)

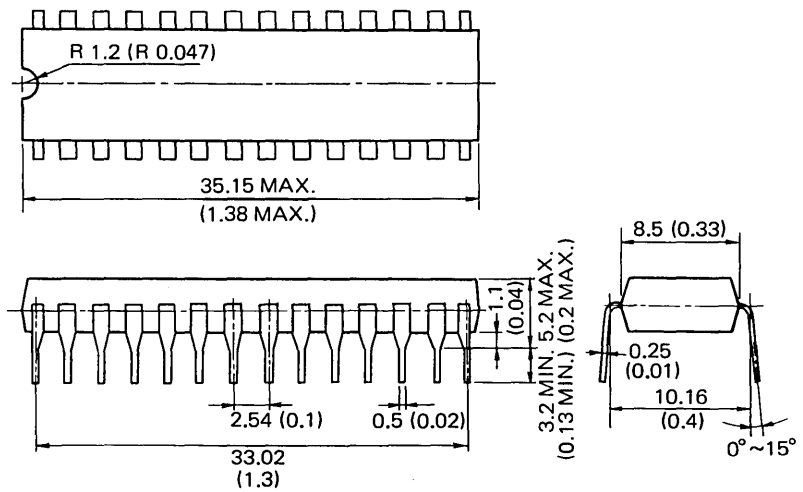
FUNCTION OF RADIO

- Automatic up search (SEEK ARI/STEREO)
- Automatic down search (SEEK ARI/STEREO)
- Manual up search
- Manual down search
- Preset station memory . . . . . FM: 6 stations, MW: 6 stations
- Last station memory . . . . . FM: 1 station, MW: 1 station, LW: 1 station

FUNCTION OF CLOCK

- 24 hour display format . . . . hours, minutes, colon
- Leading-zero blanking
- Hours and minutes set controls
- Minutes and seconds reset control

PACKAGE DIMENSIONS in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{DD}	−0.3 to +6.0	V
Input Voltage	V_I	−0.3 to V_{DD}	V
Output Voltage	V_O	−0.3 to V_{DD}	V
Output Current	I_{OH}	−10	mA
Storage Temperature	Tstg	−55 to +125	°C
Operation Temperature	Topt	−35 to +75	°C

ELECTRICAL CHARACTERISTICS (Ta=−35 to +75 °C, V_{DD}=4.5 to 5.5 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
High Level Input Voltage	V_{IH1}	$0.8V_{DD}$		V_{DD}	V	SD terminal
	V_{IH2}	$0.7V_{DD}$		V_{DD}	V	CE terminal
	V_{IH3}	$0.6V_{DD}$		V_{DD}	V	K0 to K3 terminals.
Low Level Input Voltage	V_{IL1}	0		$0.3V_{DD}$	V	CE terminal
	V_{IL2}	0		$0.2V_{DD}$	V	SD, K0 to K3 terminals.
High Level Output Voltage	V_{OH1}	4.0			V	EO, D, MUTE: I_{OH}=−0.5 mA
	V_{OH2}	4.0			V	SEG: I_{OH}=−1.0 mA
	V_{OH3}	4.0			V	PSC: I_{OH}=−0.2 mA
Low Level Output Voltage	V_{OL1}			0.5	V	EO: I_{OL}=0.5 mA
	V_{OL2}			0.5	V	D,SEG,MUTE,PSC: I_{OL}=0.2 mA
High Level Input Current	I_{IH}	5.0	25	100	μA	K: V_I=V_{DD}=5.0 V
Frequency Response	fin1	0.5		2.5	MHz	AM: vi=1.0 Vp-p, DC cut, sine wave
	fin2	0.5		8.8	MHz	FM: vi=0.8 Vp-p, DC cut, square wave
Supply Voltage Rise Time	Tr			0.5	s	V_{DD}: 0 → 4.5 V
Supply Current	I_{DD}		0.5	2.0	mA	CE: Low Level

SYSTEM DESCRIPTION

NEC's Digital Tuning System provides full electronic control of a vari-cap tuned FM/AM radio receiver and stereo. The block diagram of the system is shown in Fig. 1. This is a Phase Locked Loop Digital Tuning System which consists of two integrated circuits; controller plus PLL in a single chip, and two-modulus prescaler.

The controller (μPD1701C-011) provides Phase Locked Loop capability with on-chip frequency division, a reference oscillator whose frequency is controlled by an external crystal of 4.5 MHz, and phase comparator circuitry. It accepts directly an AM local oscillator signal and an FM signal from two-modulus prescaler (μPB553AC), and outputs control signals for closed loop operation of these oscillators. The outputs drives filters for supplying analog voltages to the vari-cap tuners. The controller also provides the signals to drive the display. The frequency of the tuned station is displayed on a 3.5 digit multiplexed display. Six favorite stations on each band can be stored as well as "last stations tuned" information.

The two-modulus prescaler (μPB553AC) is suitable for pulse swallowing in this system.

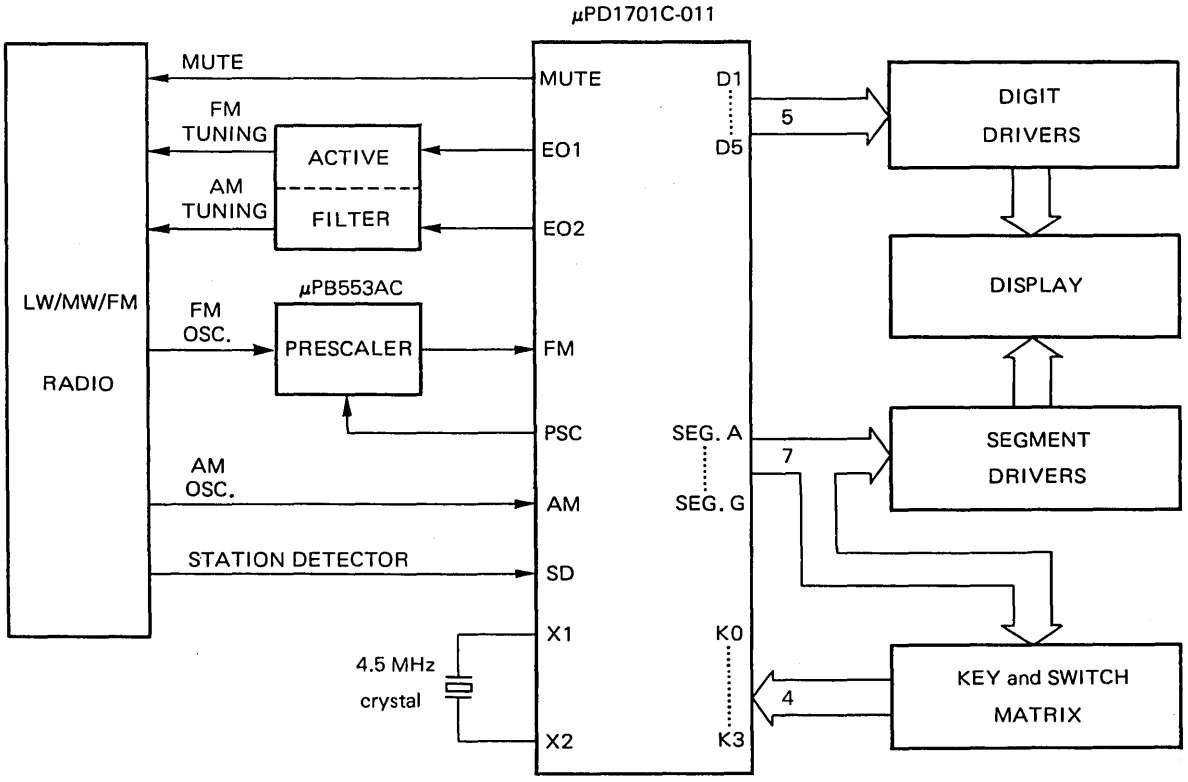
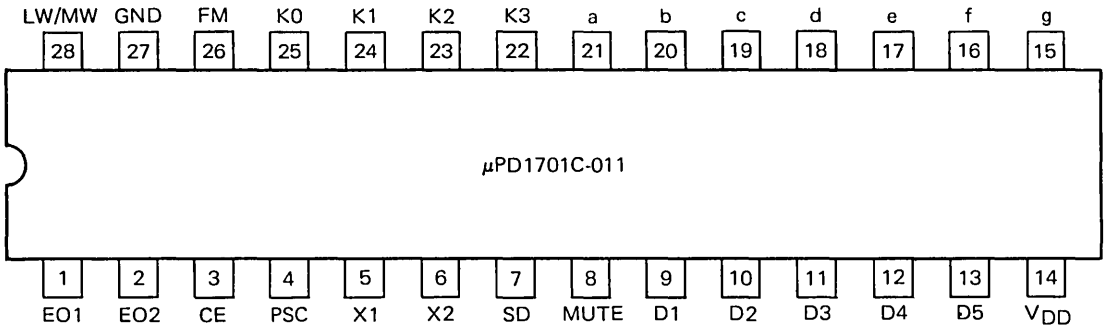


Fig. 1 BLOCK DIAGRAM

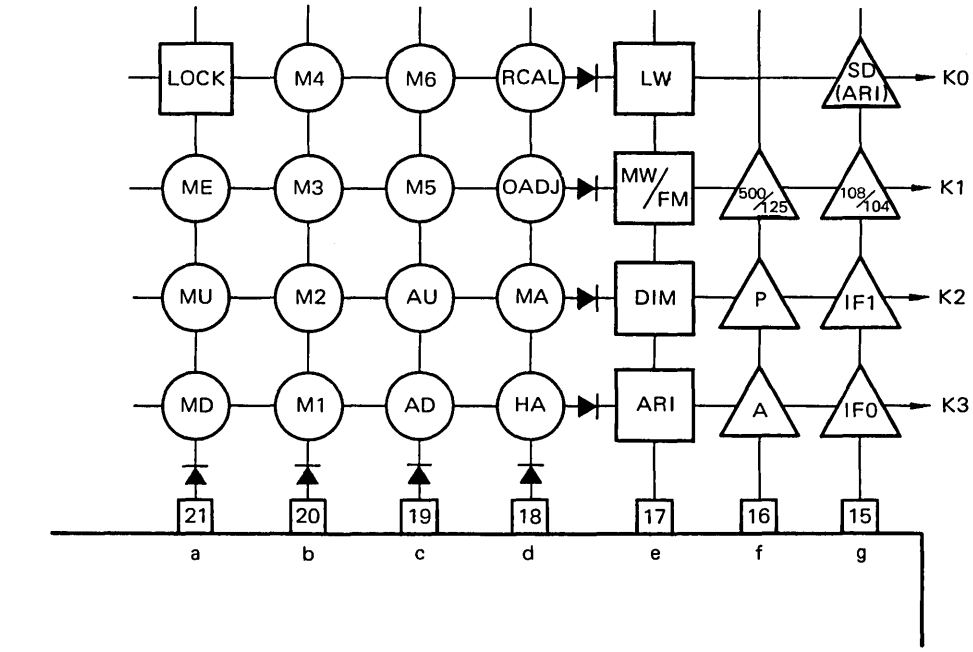
PIN CONNECTION (Top View)



EXPLANATION OF INPUT AND OUTPUT TERMINALS

EO1 EO2	These three-state outputs are used (via active filters) to supply analog voltages to the tuner vari-cap for controlling the local osc.
CE	This input is used to designate the stand-by mode to the chip. It is low to designate the stand-by mode. (Display: off, PLL: disabled)
PSC	This output is used to control the division ratio of the FM two-modulus prescaler (μPB553AC).
X1, X2	These inputs are for connection to a 4.5 MHz crystal.
SD	This input is used to control the station searching operation (AU/AD). It is high to indicate the presence of a station and the operation is terminated.
MUTE	This output line is high to mute the radio in the case of station change, band change, and so on.
D1 to D5	These outputs are used as digit drivers for the display.
V_{DD}	This is a 4.5 to 5.5 volt supply for the chip.
a to g	These outputs are used as segment drivers for the display. They are also used as vertical drive for the control key and mode switch matrix.
K0 to K3	These inputs are from seven by four matrix. Various functions are entered through the matrix. See Fig. 2 for the matrix assignments.
FM	This is the FM band local oscillator input. The frequency is divided by 16/17 using a two-modulus prescaler (μPB553AC).
GND	System ground.
LW/MW	This input is the LW/MW band local oscillator input.

CONTROL KEY AND MODE SWITCH MATRIX



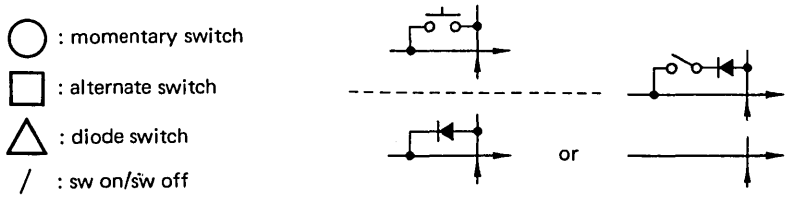


Fig. 2

* **Manual up or down search**

  MU, MD A momentary depression will tune to next channel, and continuous depression more than 0.5 second allows traversing up or down the entire band until the key is released.

* **Automatic up or down search**

  AU, AD (SEEK) A momentary depression causes automatic up or down search which is terminated by activation of SD terminal (active high).

* **Preset of the station**

  ME The tuning information is stored into internal RAM by depressing ME key and then the desired memory key within 5 seconds from the time ME key was initially depressed. If any key is depressed in this period, the ME function is cancelled.

  M1 to M6 Six favorite stations can be recalled from internal RAM for each band. When it is switched from one band to another band, it will tune to "last-tuned-to station" on that band. Each time a station is changed, the controller provides a signal to mute the radio.

* **Clock function**

HA, MA These keys are used for hours and minutes setting. (See note)

OADJ A momentary depression resets minutes and seconds.

NOTE: MU and MD keys can be used to set minutes and hours, keeping depressing ME key when time is displayed.

* **Switching-over the display**

RCAL A momentary depression will change the display mode when radio is on.

A ON: Frequency is given priority for the display.
OFF: Clock is given priority for the display.

P ON: There is a priority on the display.
When RCAL key depressed, the display returns to the prior matter after 5,sec display of another.
OFF: There is no priority on the display.

DIMMER ON: Display brightness is reduced (duty: 20 % of normal brightness).
OFF: Display brightness is normal.

* **ARI/STEREO search**

ARI OFF: Normal automatic search (AU, AD)
ON: In the case of FM band, ARI/STEREO search is possible.
A momentary depression of AU/AD key causes up or down ARI/STEREO search which is terminated by activation of SD terminal and ARI SD switch. (Timing diagram is shown below.)

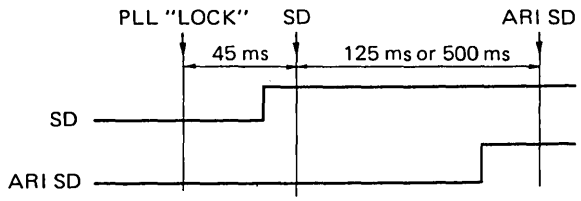


Fig. 3

500/125 This switch is for a selection of timing in the case of ARI/STEREO search.
ON: The controller waits 500 ms from the activation of SD terminal.
OFF: The controller waits 125 ms from the activation of SD terminal.

ARI SD This switch is normally a transistor switch. In the case of ARI/STEREO search, ARI (SK, BK or DK) or STEREO SD signal is read from this switch.

* **Selection of the radio band**

LW, MW/FM These switches are for selection of the radio band (LW, MW, FM).

LW	MW/FM	BAND	Receiving Frequency	Channel Spacing	Intermediate Frequency
ON	x	LW	155 to 281 kHz	9 kHz	450 kHz
OFF	ON	MW	531 to 1602 kHz	9 kHz	450 kHz
OFF	OFF	FM	87.5 to 104/108 MHz*	50 kHz	**

x : Don't care.

Table 1

IF0, IF1** Two external diodes program the chip to accept 4 different frequencies from 10.650 MHz to 10.725 MHz in 25 kHz steps.

IF0	IF1	Intermediate Frequency
OFF	ON	10.650 MHz
ON	ON	10.675 MHz
OFF	OFF	10.700 MHz
ON	OFF	10.725 MHz

Table 2

108/104* This switch is used to preset the FM receiving band.

108/104	Receiving Frequency
ON	87.50 MHz to 108.00 MHz
OFF	87.50 MHz to 104.00 MHz

Table 3

* **Display interface**

The center frequency of tuned station is displayed on a 3.5 digit LED display. The segment outputs a, b, c, d, e, f, and g are also used as inputs for 7 segment drivers. The segment output go to common collector NPN transistor array (μPA56C) to drive the segments of the common cathode 7 segment LED display. The digit outputs go to NPN darlington transistor array (μPA53C) to drive the LED display.

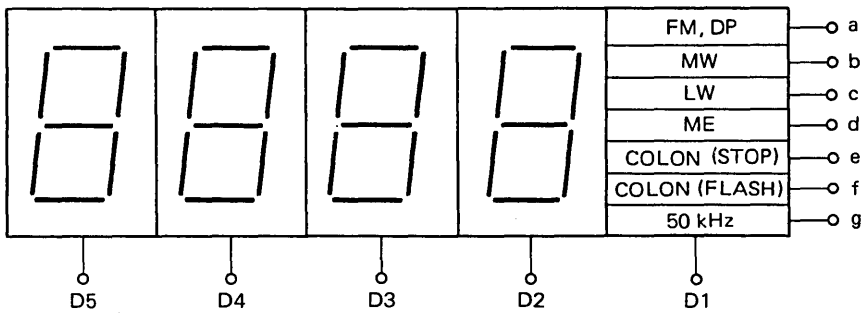
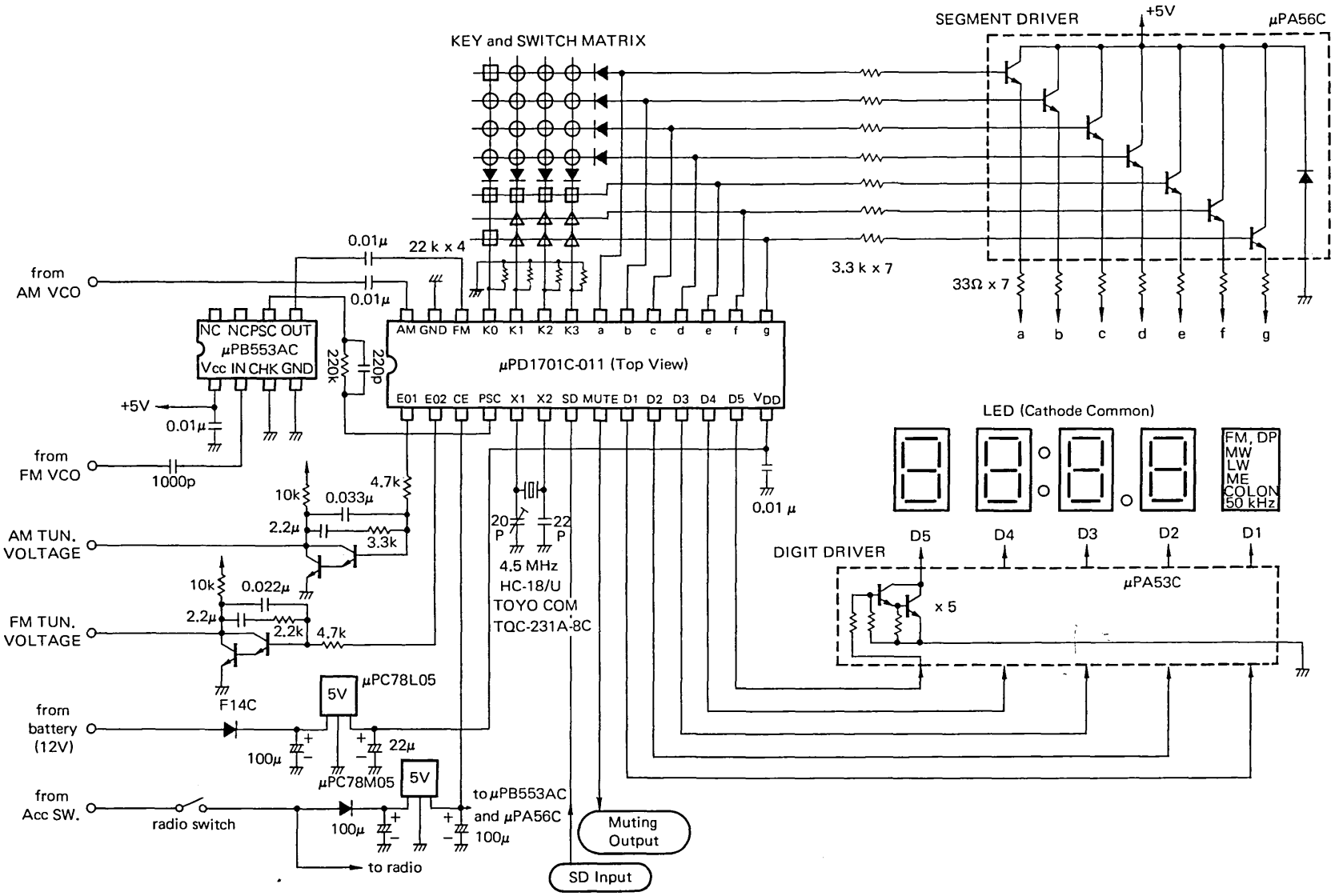


Fig. 4

Fig. 5 APPLICATION CIRCUIT



MOS DIGITAL INTEGRATED CIRCUIT
μPD1701C-013

PHASE LOCKED LOOP FREQUENCY SYNTHESIZER FM/AM DIGITAL TUNING SYSTEM CONTROLLER CMOS LSI

The μPD1701C-013 is a single chip CMOS controller designed for using as a Phase Locked Loop Frequency Synthesizer Digital Tuning System Controller.

The μPD1701C-013 is packaged in a 28 pin slim dual in-line package (DIP).

FEATURES

- PLL, swallow counter and system controller are realized in a single chip.
- FM and AM bands ——— Japan and U.S. bands.
- High reference frequency. (FM: 25 kHz, AM: 9/10 kHz)
  It results in a high carrier to noise ratio.
- External programmable IF offset for FM band.
- High speed and low power consumption due to CMOS.
- Stand-by mode ——— Supply current I_{DD} = 0.5 mA (TYP.)
- Display brightness control (DIMMER) ——— Duty ratio 1 : 4
- Internal display decorder for 3.5 digit multiplexed display.
- Automatic power-on clear without any external components.

FUNCTION OF RADIO

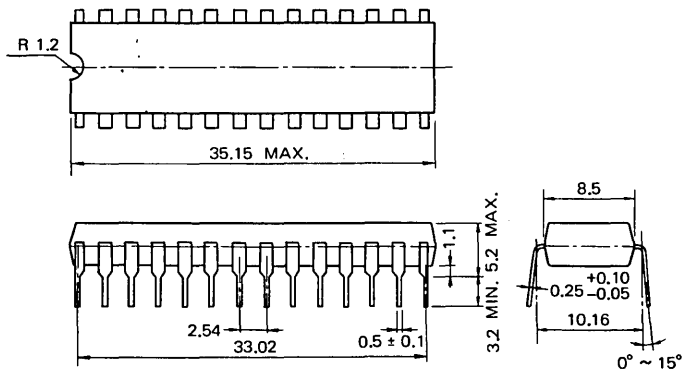
- Automatic up search (SEEK)
- Automatic audition (SCAN)
- Manual up or down search
- Preset station memory call
- Preset station memory ——— FM: 6 stations, AM: 6 stations
- Last tuned station memory ——— FM: 1 station, AM: 1 station

FUNCTION OF CLOCK

- 12 hour display format ——— hours, minutes, AM/PM, colon
- Leading-zero blanking
- Hours and minutes set controls
- Minutes and seconds reset control

PACKAGE DIMENSIONS

in millimeters



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{DD}	−0.3 to +6.0	V
Input Voltage	V_I	−0.3 to V_{DD}	V
Output Voltage	V_O	−0.3 to V_{DD}	V
Output Current	I_{OH}	−10	mA
Storage Temperature	Tstg	−55 to +125	°C
Operation Temperature	Topt	−35 to +75	°C

ELECTRICAL CHARACTERISTICS (Ta= −35 to +75 °C, V_{DD}= 4.5 to 5.5 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
High Level Input Voltage	V_{IH1}	$0.8V_{DD}$		V_{DD}	V	SD terminal
	V_{IH2}	$0.7V_{DD}$		V_{DD}	V	CE terminal
	V_{IH3}	$0.6V_{DD}$		V_{DD}	V	K0 to K3 terminals
Low Level Input Voltage	V_{IL1}	0		$0.3V_{DD}$	V	CE terminal
	V_{IL2}	0		$0.2V_{DD}$	V	SD, K0 to K3 terminals
High Level Output Voltage	V_{OH1}	4.0			V	EO, D, MUTE: I_{OH}=−0.5 mA
	V_{OH2}	4.0			V	SEG: I_{OH}=−1.0 mA
	V_{OH3}	4.0			V	PSC: I_{OH}=−0.2 mA
Low Level Output Voltage	V_{OL1}			0.5	V	EO: I_{OL}=0.5 mA
	V_{OL2}			0.5	V	D,SEG,MUTE,PSC: I_{OL}= 0.2 mA
High Level Input Current	I_{IH}	5.0	25	100	μA	K: V_I=V_{DD}=5.0 V
Frequency Response	fin1	0.5		2.5	MHz	AM: vi=1.0 Vp-p, DC cutsine wave
	fin2	0.5		8.8	MHz	FM: vi=0.8 Vp-p, DC cut square wave
Supply Voltage Rise Time	Tr			0.5	s	V_{DD}: 0→ 4.5 V
Supply Current	I_{DD}		0.5	2.0	mA	CE: Low Level

SYSTEM DESCRIPTION

NEC's Digital Tuning System provides full electronic control of a vari-cap tuned FM/AM radio receiver and stereo. The block diagram of the system is shown in Fig. 1. This is a Phase Locked Loop Digital Tuning System which consists of two integrated circuits; controller plus PLL in a single chip, and two-modulus prescaler.

The controller chip (μPD1701C-013) provides Phase Locked Loop capability with on-chip frequency division, a reference oscillator whose frequency is controlled by an external crystal of 4.5 MHz, and phase comparator circuitry. It accepts directly an AM local oscillator signal and an FM signal from two-modulus prescaler (μPB553AC), and outputs control signals for closed loop operation of these oscillators. The outputs drives filters for supplying analog voltages to the vari-cap tuners. The controller also provides the signals to drive the display. The frequency of the tuned station is displayed on a 3.5 digit multiplexed display. Six favorite stations on each band can be stored as well as "last stations tuned" information.

The two-modulus prescaler (μPB553AC) is suitable for pulse swallowing in this system.

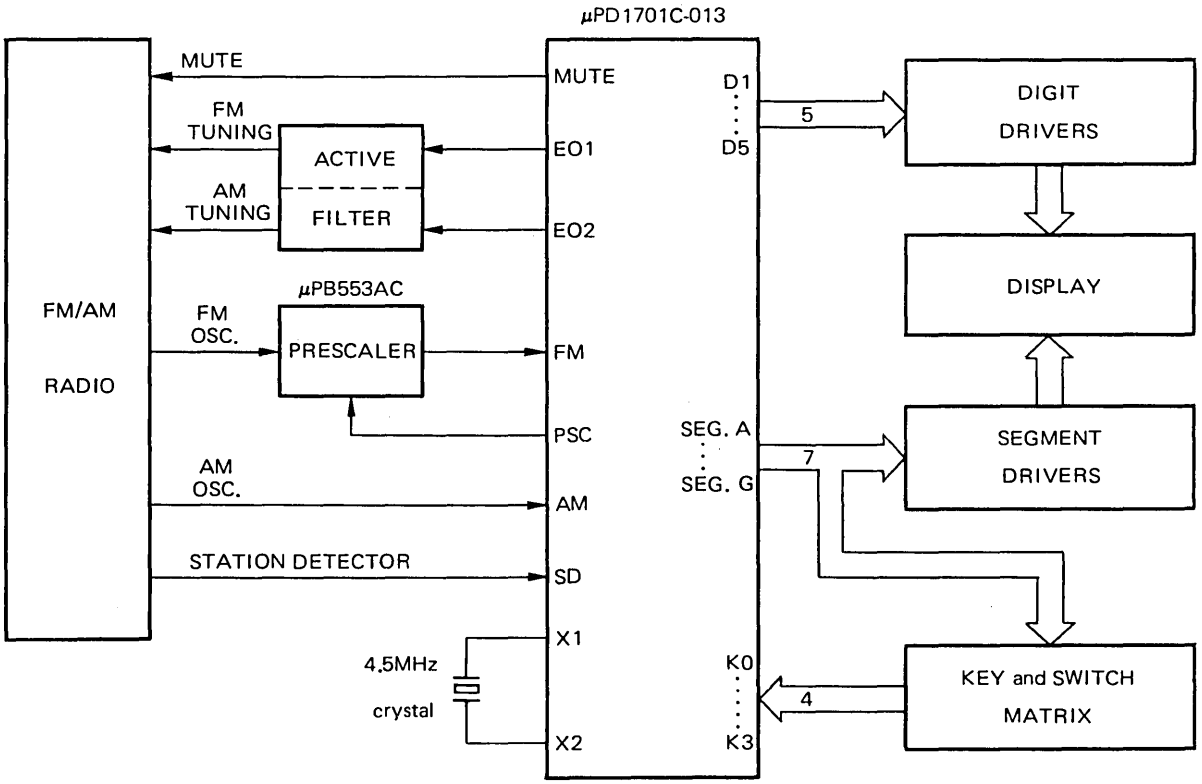
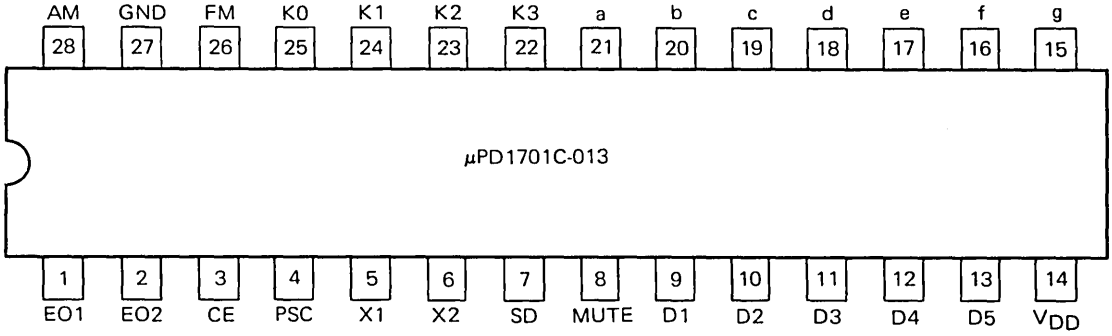


Fig. 1 Block Diagram

PIN CONNECTION (Top View)



EXPLANATION OF INPUT AND OUTPUT TERMINALS

EO1 EO2	These three-state outputs are used (via active filters) to supply analog voltages to the tuner varicap for controlling the local oscillators.
CE	This input is used to designate the stand-by mode to the chip. It is low to designate the stand-by mode. (display: off, PLL: disable)
PSC	This output is used to control the division ratio of the FM two-modulus prescaler (μPB553AC).
X1 , X2	These inputs are for connection to a 4.5MHz crystal.
SD	This input is used to control the automatic station searching operation. It is high to indicate the presence of a station.
MUTE	This output line is high to mute the radio in the case of station change, band change, and so on.
D1 to D5	These outputs are used as digit drivers for the display. (Active high)
V_{DD}	This is a 4.5 to 5.5 volt supply for the chip.
a to g	These outputs are used as segment drivers for the display. They are also used as vertical drive for the control key and mode switch matrix. (Active high)
K0 to K3	These inputs are from seven by four matrix. Various functions are entered through the matrix. See Fig. 2 for the matrix assignments.
FM	This is the FM band local oscillator input. The frequency is divided by 16/17 using a two-modulus prescaler (μPB553AC).
GND	System ground.
AM	This is the AM band local oscillator input.

CONTROL KEY AND MODE SWITCH MATRIX

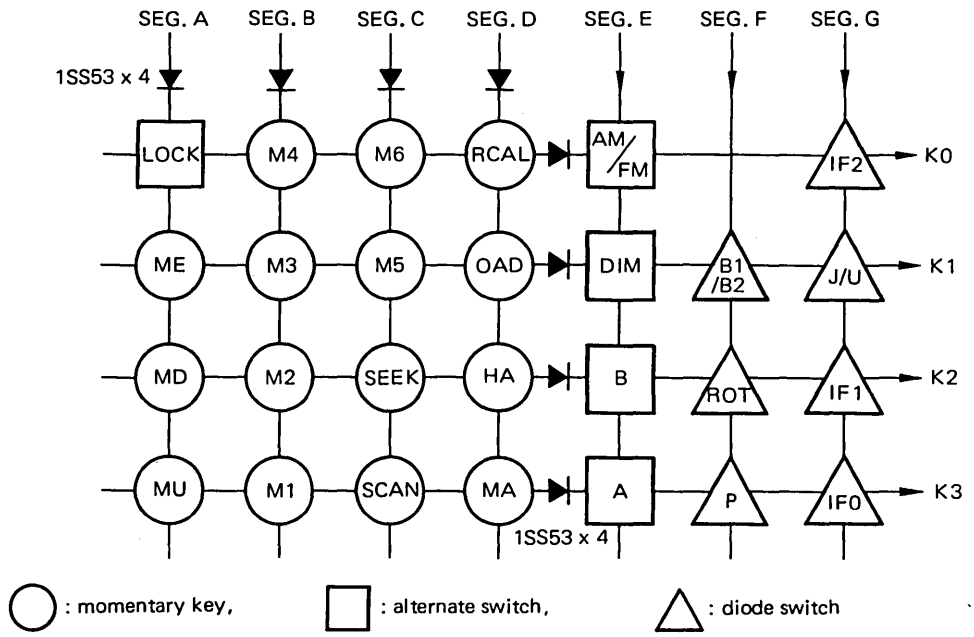


Fig. 2 Control Key and Mode Switch Matrix

* **Manual up or down search**

MU, MD A momentary depression will tune to next channel, and continuous depression more than 0.5 second allows traversing up or down the entire band until the key is released.

* **Automatic up search (Saw-tooth search)**

SEEK A momentary depression causes automatic up search which is terminated by activation of SD terminal (active high).

SCAN A momentary depression causes automatic station-to-station search.

* **Preset of the station**

ME The tuning information is stored into the internal RAM by depressing ME key and then the desired memory key (M1 to M6) within 5 seconds from the time ME key was initially depressed. If any other key is depressed in this period, the ME function is cancelled.

M1 to M6 Six favorite stations can be recalled from internal RAM for each band. When it is switched from one band to the other, it will tune to "last-tuned-to station" on that band .
Each time a station is changed, the controller provides a signal to mute the radio.

* **Clock set controls**

HA, MA These keys are used for hours and minutes setting. (See note)

OAD A momentary depression will reset minutes and seconds.

Note MU and MD keys can be used to set minutes and hours, keeping depressing ME key when time is displayed.

* **Switching-over the display between radio and clock**

A, B, P
RCAL

Display mode switches A, B initial switch P and control key RCAL control the display mode as follows.

1. A: ON, B:ON, P:ANY
   No priority on the display. A momentary depression of RCAL key causes alternate display change between time and frequency whenever it is performed. Whenever frequency is handled, frequency is displayed.
2. A: ON, B: OFF, P:OFF
   Clock display is prior to frequency. A momentary depression of RCAL key causes alternative display chnage. When time is displayed, a depression of RCAL or one of the frequency handling key recalls frequency information on the display for 5 seconds. After that, the display turns back to clock automatically.
3. A: ON, B: OFF, P: ON
   Frequency is prior to the clock. A momentary depression of RCAL key causes the alternative display change. When frequency is displayed, a momentary depression of RCAL key recalls clock display and it remains there for 5 seconds. If any other key is handled when time is displayed, handling of one of the time adjust keys (HA, MA, OAD) keeps the time display, the display turns back to frequency automatically 5 seconds after the time adjust is completed. Whenever frequency is handled, frequency is displayed.
4. A: OFF, B: OFF, P: ANY
   Clock only.
5. A: OFF, B: ON, P: ANY
   Disabled.

* **Switching-over the Manual UP/DOWN signal generator**

ROT

ON: Pulse repetition rate more than 6 milisecond will be acceptable as MU or MD signal for an application of the endless-rotary switch as the signal generator.

OFF: Pulse repetition rate more than 60 milisecond will be acceptable preventing from miscounting by chattering of the momentary switches applied for UP/DOWN signal generator.

* **Protection from the miss key input**

LOCK

This switch is for protection from miss key input.

ON ..... All of the key input is disabled.

OFF ..... All of the key input is enabled.

* **Protection from the key chattering**

Key make time ..... less than 15 ms

Key break time ..... less than 15 ms

* **Selection of the radio band**

J/U This switch is for selection of the district.

AM/FM This switch is for selection of the radio band.

Band Switch		Selected Band	
J/U	AM/FM		
off	off	FM U.S.	87.9 to 107.9 MHz, channel spacing 200 kHz
	on	AM U.S.	530 to 1 620 kHz, channel spacing 10 kHz *3
on	off	FM Japan	76.1 to 89.9 MHz, channel spacing 100 kHz
	on	AM Japan	531 to 1 602 kHz, channel spacing 9 kHz

*3: See AM band IF offset

Table 2

* **FM band IF offset**

IF0, IF1 These switches program the chip to accept 4 different intermediate frequencies.

IF0	IF1	Intermediate Frequency	
		Japan	U.S.
on	off	10.750 MHz	10.650 MHz
on	on	10.725 MHz	10.675 MHz
off	off	10.700 MHz	10.700 MHz
off	on	10.675 MHz	10.725 MHz

Table 3

* **AM band IF offset**

IF2 This switch programs the chip to accept 2 different intermediate frequencies.

B1/B2 This switch is for selection of the receiving band and channel spacing of AM radio for U.S. band.

J/U	B1/B2	IF2	Intermediate Frequency	Receiving Frequency	Channel Spacing
on	X	on	261 kHz	531 to 1 602 kHz	9 kHz
		off	450 kHz		
off	on	on	261 kHz	531 to 1 602 kHz	9 kHz
		off	450 kHz		
	off	on	260 kHz	530 to 1 620 kHz	10 kHz
		off	450 kHz		

Table 4

* **Display interface**

The center frequency of tuned station is displayed on a 3.5 digit LED display. The segment outputs a, b, c, d, e, f, and g are also used as inputs for 7 segment drivers. The segment outputs go to common collector NPN transistor array (μPA56C) to drive the segments of the common cathode 7 segment LED display. The digit outputs go to NPN darlington transistor array (μPA53C) to drive the LED display.

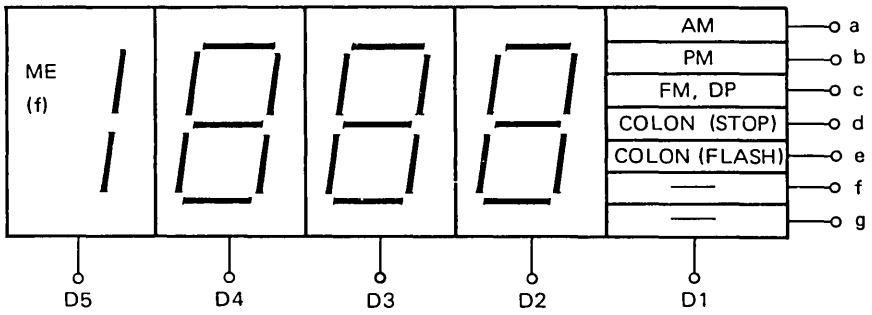
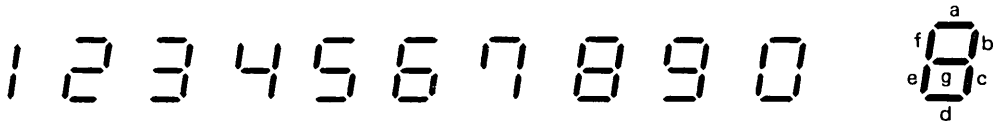


Fig. 4

* **Display format**

○ Segment Pattern



* **Display brightness control (DIMMER)**

DIM This switch is for selection of display brightness.

ON – – – – Display brightness is reduced. (Duty factor: 1/32)

OFF ——— Display brightness is ordinary. (Duty factor: 1/8)

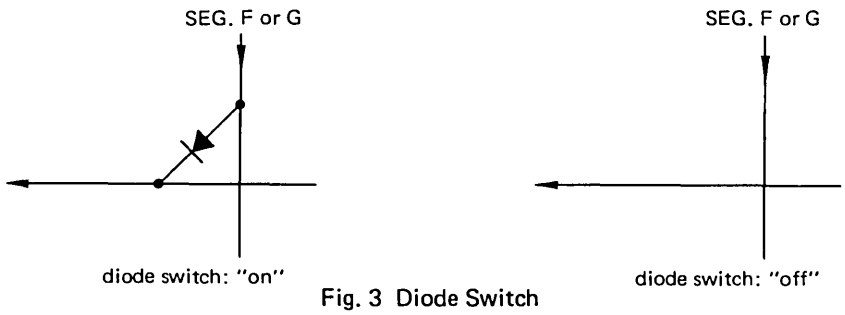


Fig. 3 Diode Switch

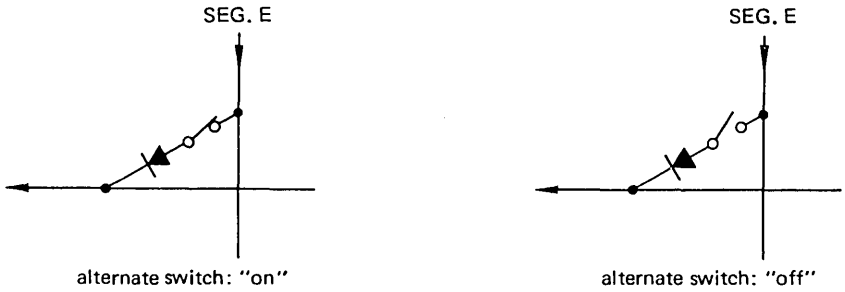
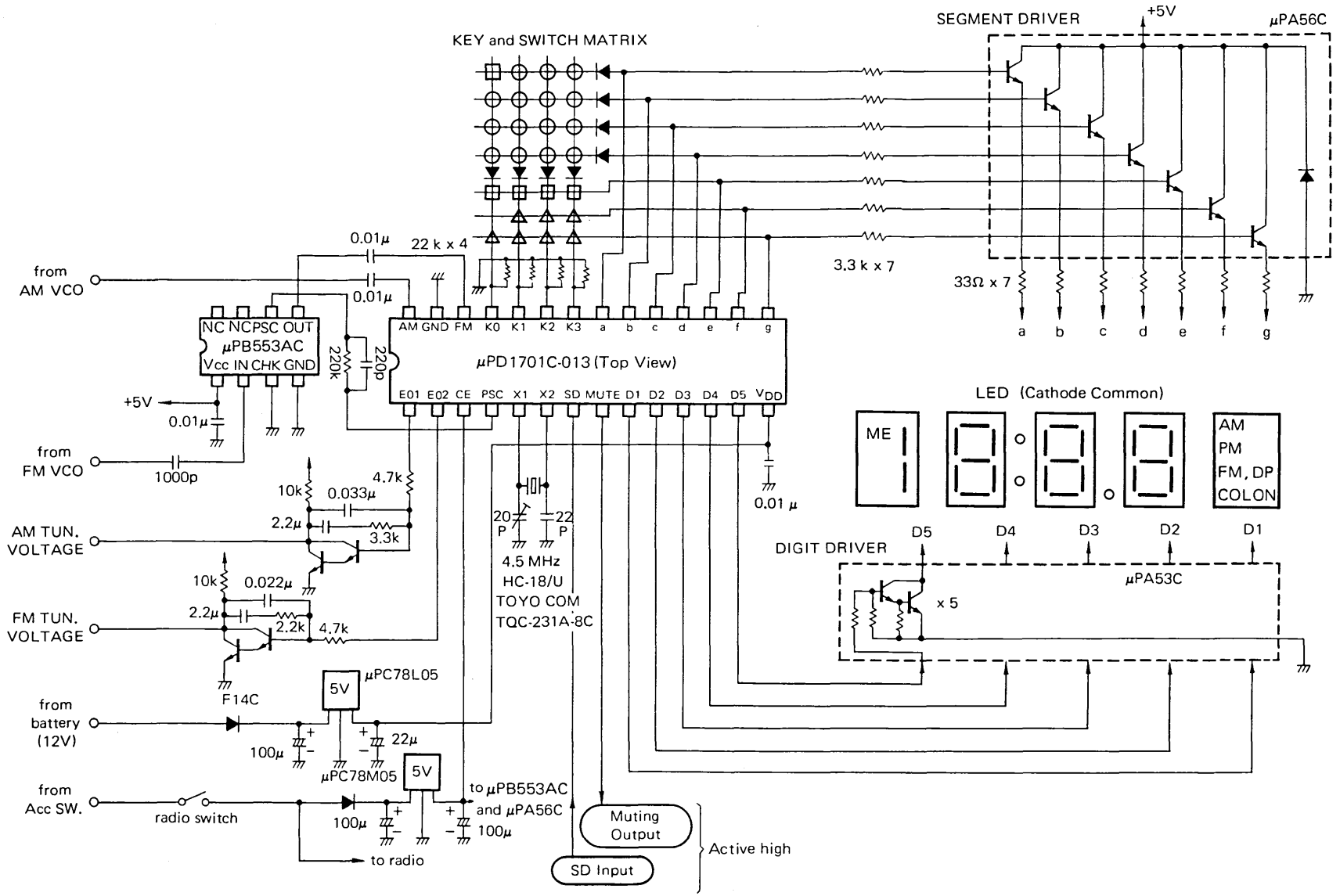


Fig. 4 Alternate Switch

Fig. 5 APPLICATION CIRCUIT



MOS DIGITAL INTEGRATED CIRCUIT
μPD1701C-014

PHASE LOCKED LOOP FREQUENCY SYNTHESIZER FM/AM DIGITAL TUNING SYSTEM CONTROLLER CMOS LSI

The μPD1701C-014 is a single chip CMOS controller designed for using as a Phase Locked Loop Frequency Synthesizer Digital Tuning System Controller.

The μPD1701C-014 is packaged in a 28 pin slim dual in-line package (DIP).

FEATURES

- PLL, swallow counter and system controller are realized in a single chip.
- FM and AM bands ——— Japan, U.S. and Europe bands.
- High reference frequency. (FM: 25 kHz, AM: 9/10 kHz)
  It results in a high carrier to noise ratio.
- External programmable IF offset for FM band.
- High speed and low power consumption due to CMOS.
- Stand-by mode ——— Supply current I_{DD} = 0.5 mA (TYP.)
- Display brightness control (DIMMER) ——— Duty ratio 1 : 4
- Internal display decorder for 3.5 digit multiplexed display.
- Automatic power-on clear without any external components.

FUNCTION OF RADIO

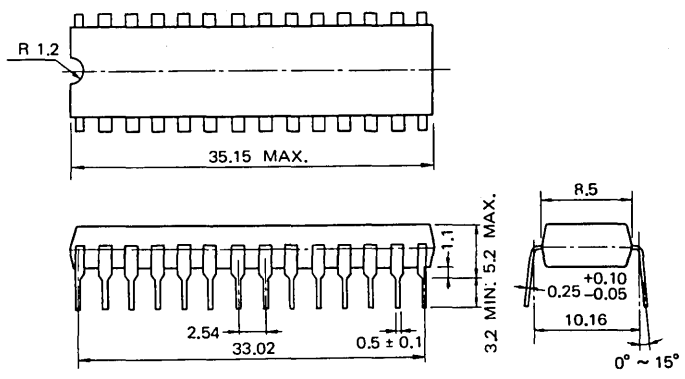
- Automatic up search (SEEK)
- Automatic audition (SCAN)
- Manual up or down search
- Preset station memory call
- Preset station memory ——— FM: 6 stations, AM: 6 stations
- Last tuned station memory ——— FM: 1 station, AM: 1 station

FUNCTION OF CLOCK

- 12 hour display format ——— hours, minutes, AM/PM, colon
- Leading-zero blanking
- Hours and minutes set controls
- Minutes and seconds reset control

PACKAGE DIMENSIONS

in millimeters



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{DD}	−0.3 to +6.0	V
Input Voltage	V_I	−0.3 to V_{DD}	V
Output Voltage	V_O	−0.3 to V_{DD}	V
Output Current	I_{OH}	−10	mA
Storage Temperature	Tstg	−55 to +125	°C
Operation Temperature	Topt	−35 to +75	°C

ELECTRICAL CHARACTERISTICS (Ta= −35 to +75 °C, V_{DD}= 4.5 to 5.5 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
High Level Input Voltage	V_{IH1}	$0.8V_{DD}$		V_{DD}	V	SD terminal
	V_{IH2}	$0.7V_{DD}$		V_{DD}	V	CE terminal
	V_{IH3}	$0.6V_{DD}$		V_{DD}	V	K0 to K3 terminals
Low Level Input Voltage	V_{IL1}	0		$0.3V_{DD}$	V	CE terminal
	V_{IL2}	0		$0.2V_{DD}$	V	SD, K0 to K3 terminals
High Level Output Voltage	V_{OH1}	4.0			V	EO, D, MUTE: I_{OH}=−0.5 mA
	V_{OH2}	4.0			V	SEG: I_{OH}=−1.0 mA
	V_{OH3}	4.0			V	PSC: I_{OH}=−0.2 mA
Low Level Output Voltage	V_{OL1}			0.5	V	EO: I_{OL}=0.5 mA
	V_{OL2}			0.5	V	D,SEG,MUTE,PSC: I_{OL}= 0.2 mA
High Level Input Current	I_{IH}	5.0	25	100	μA	K: V_I=V_{DD}=5.0 V
Frequency Response	fin1	0.5		2.5	MHz	AM: vi=1.0 Vp-p, DC cut sine wave
	fin2	0.5		8.8	MHz	FM: vi= 0.8 Vp-p, DC cut square wave
Supply Voltage Rise Time	Tr			0.5	s	V_{DD}: 0→ 4.5 V
Supply Current	I_{DD}		0.5	2.0	mA	CE: Low Level

SYSTEM DESCRIPTION

NEC's Digital Tuning System provides full electronic control of a vari-cap tuned FM/AM radio receiver and stereo. The block diagram of the system is shown in Fig. 1. This is a Phase Locked Loop Digital Tuning System which consists of two integrated circuits; controller plus PLL in a single chip, and two-modulus prescaler.

The controller chip (μPD1701C-014) provides Phase Locked Loop capability with on-chip frequency division, a reference oscillator whose frequency is controlled by an external crystal of 4.5 MHz, and phase comparator circuitry. It accepts directly an AM local oscillator signal and an FM signal from two-modulus prescaler (μPB553AC), and outputs control signals for closed loop operation of these oscillators. The outputs drives filters for supplying analog voltages to the vari-cap tuners. The controller also provides the signals to drive the display. The frequency of the tuned station is displayed on a 3.5 digit multiplexed display. Six favorite stations on each band can be stored as well as "last stations tuned" information.

The two-modulus prescaler (μPB553AC) is suitable for pulse swallowing in this system.

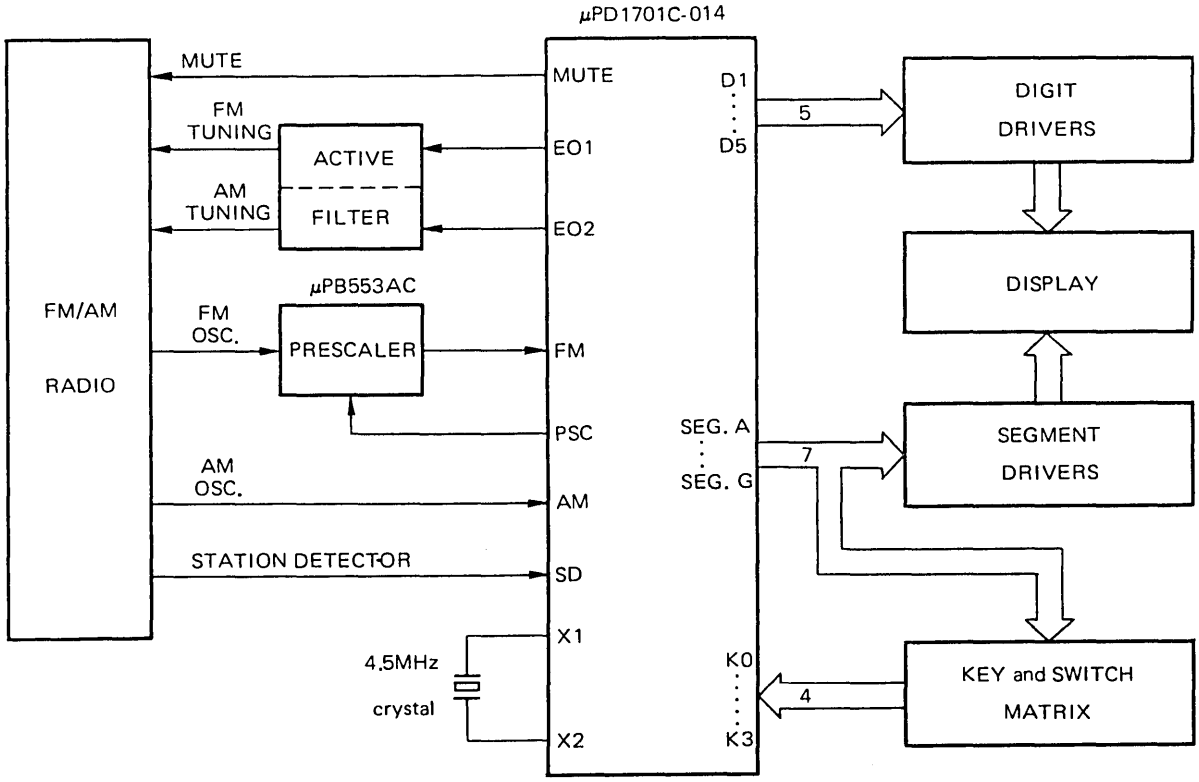
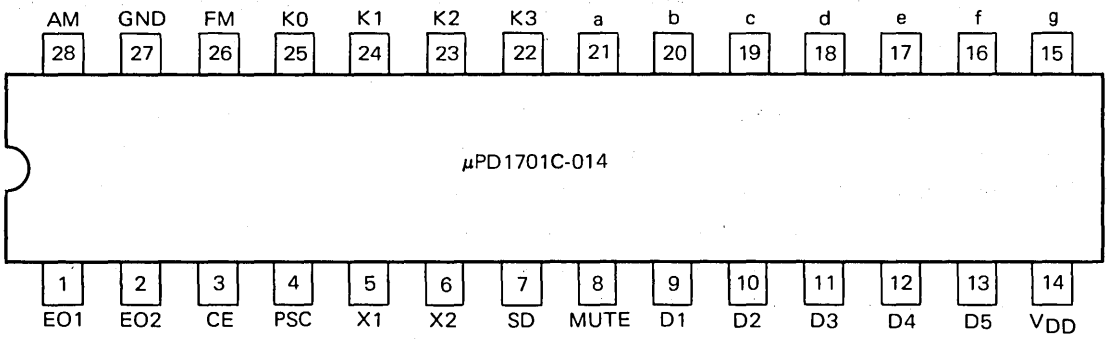


Fig. 1 Block Diagram

PIN CONNECTION (Top View)



EXPLANATION OF INPUT AND OUTPUT TERMINALS

EO1 EO2	These three-state outputs are used (via active filters) to supply analog voltages to the tuner varicap for controlling the local oscillators.
CE	This input is used to designate the stand-by mode to the chip. It is low to designate the stand-by mode. (display: off, PLL: disable)
PSC	This output is used to control the division ratio of the FM two-modulus prescaler (μPB553AC).
X1 , X2	These inputs are for connection to a 4.5MHz crystal.
SD	This input is used to control the automatic station searching operation. It is high to indicate the presence of a station.
MUTE	This output line is high to mute the radio in the case of station change, band change, and so on.
D1 to D5	These outputs are used as digit drivers for the display. (Active high)
V_{DD}	This is a 4.5 to 5.5 volt supply for the chip.
a to g	These outputs are used as segment drivers for the display. They are also used as vertical drive for the control key and mode switch matrix. (Active high)
K0 to K3	These inputs are from seven by four matrix. Various functions are entered through the matrix. See Fig. 2 for the matrix assignments.
FM	This is the FM band local oscillator input. The frequency is divided by 16/17 using a two-modulus prescaler (μPB553AC).
GND	System ground.
AM	This is the AM band local oscillator input.

CONTROL KEY AND MODE SWITCH MATRIX

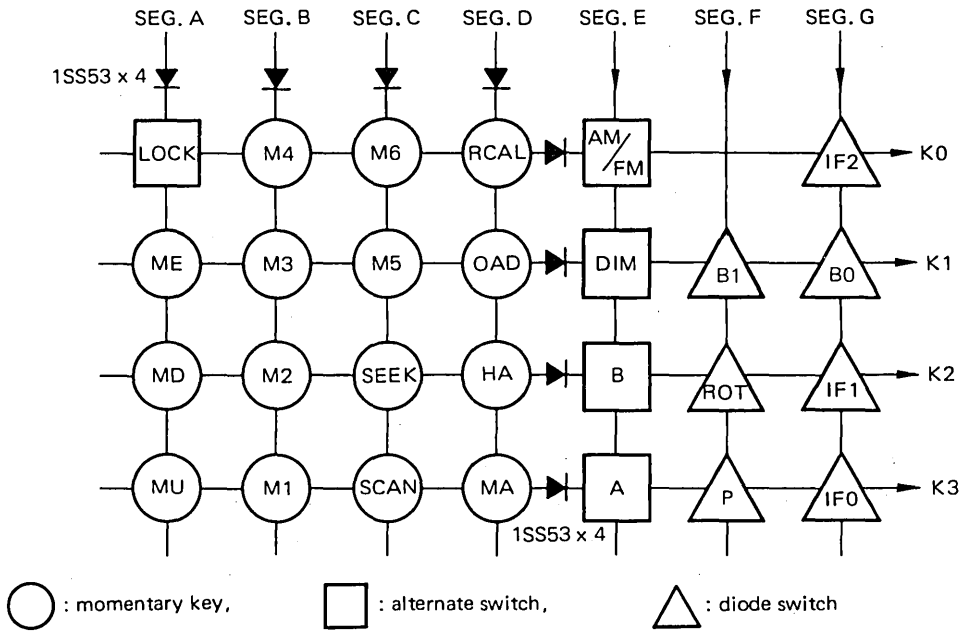


Fig. 2 Control Key and Mode Switch Matrix

* **Manual up or down search**

MU, MD A momentary depression will tune to next channel, and continuous depression more than 0.5 second allows traversing up or down the entire band until the key is released.

* **Automatic up search (Saw-tooth search)**

SEEK A momentary depression causes automatic up search which is terminated by activation of SD terminal (active high).

SCAN A momentary depression causes automatic station-to-station search.

* **Preset of the station**

ME The tuning information is stored into the internal RAM by depressing ME key and then the desired memory key (M1 to M6) within 5 seconds from the time ME key was initially depressed. If any other key is depressed in this period, the ME function is cancelled.

M1 to M6 Six favorite stations can be recalled from internal RAM for each band. When it is switched from one band to the other, it will tune to "last-tuned-to station" on that band .
Each time a station is changed, the controller provides a signal to mute the radio.

* **Clock set controls**

HA, MA These keys are used for hours and minutes setting. (See note)

OAD A momentary depression will reset minutes and seconds.

Note MU and MD keys can be used to set minutes and hours, keeping depressing ME key when time is displayed.

* **Switching-over the display between radio and clock**

A, B, P
RCAL

Display mode switches A, B initial switch P and control key RCAL control the display mode as follows.

1. A: ON, B: ON, P:ANY
   No priority on the display. A momentary depression of RCAL key causes alternate display change between time and frequency whenever it is performed. Whenever frequency is handled, frequency is displayed.
2. A: ON, B: OFF, P: OFF
   Clock display is prior to frequency. A momentary depression of RCAL key causes alternative display change. When time is displayed, a depression of RCAL or one of the frequency handling key recalls frequency information on the display for 5 seconds. After that, the display turns back to clock automatically.
3. A: ON, B: OFF, P: ON
   Frequency is prior to the clock. A momentary depression of RCAL key causes the alternative display change. When frequency is displayed, a momentary depression of RCAL key recalls clock display and it remains there for 5 seconds. If any other key is handled when time is displayed, handling of one of the time adjust keys (HA, MA, OAD) keeps the time display, the display turns back to frequency automatically 5 seconds after the time adjust is completed. Whenever frequency is handled, frequency is displayed.
4. A: OFF, B: OFF, P: ANY
   Clock only.
5. A: OFF, B: ON, P:ANY
   Disabled.

* **Switching-over the Manual UP/DOWN signal generator**

ROT

ON: Pulse repetition rate more than 6 milisecond will be acceptable as MU or MD signal for an application of the endless-rotary switch as the signal generator.

OFF: Pulse repetition rate more than 60 milisecond will be acceptable preventing from miscounting by chattering of the momentary switches applied for UP/DOWN signal generator.

* **Protection from the miss key input**

LOCK

This switch is for protection from miss key input.

ON ..... All of the key input is disabled.

OFF ..... All of the key input is enabled.

* **Protection from the key chattering**

Key make time ..... less than 15 ms

Key break time ..... less than 15 ms

* **Selection of the radio band**

B0, B1 These switches are for selection of the district.

AM/FM This switch is for selection of the radio band.

Band Switch			Selected Band	Receiving Frequency	Channel Spacing	Reference Frequency
B0	B1	AM/FM				
on	X	on	AM Japan	531 to 1 602 kHz	9 kHz	9 kHz
		off	FM Japan	76.1 to 89.9 MHz	100 kHz	25 kHz
off	on	on	AM Europe	531 to 1 602 kHz	9 kHz	9 kHz
		off	FM Europe	87.9 to 107.9 MHz	100 kHz	25 kHz
off	on	on	AM U.S. *3	531 to 1 602 kHz	9 kHz	9 kHz
		off	FM U.S.	87.9 to 107.9 MHz	100 kHz	25 kHz
	off	on	AM U.S. *3	530 to 1 620 kHz	10 kHz	10 kHz
		off	FM U.S.	87.9 to 107.9 MHz	100 kHz	25 kHz

*3: See AM band IF offset

Table 2

* **FM band IF offset**

IF0, IF1 These switches program the chip to accept 4 different intermediate frequencies.

IF0	IF1	Intermediate Frequency		
		Japan Band	Europe Band	U.S. Band
on	off	10.750 MHz	10.650 MHz	10.650 MHz
on	on	10.725 MHz	10.675 MHz	10.675 MHz
off	off	10.700 MHz	10.700 MHz	10.700 MHz
off	on	10.675 MHz	10.725 MHz	10.725 MHz

Table 3

* **AM band IF offset**

IF2 This switch programs the chip to accept 2 different intermediate frequencies.

B1 This switch is for selection of the receiving band and channel spacing of AM radio for U.S. band.

B0	B1	IF2	Intermediate Frequency	Receiving Frequency	Channel Spacing
off	on	on	261 kHz	531 to 1 602 kHz	9 kHz
		off	450 kHz		
	off	on	260 kHz	530 to 1 620 kHz	10 kHz
		off	450 kHz		

Table 4

* **Display interface**

The center frequency of tuned station is displayed on a 3.5 digit LED display. The segment outputs a, b, c, d, e, f, and g are also used as inputs for 7 segment drivers. The segment outputs go to common collector NPN transistor array (μPA56C) to drive the segments of the common cathode 7 segment LED display. The digit outputs go to NPN darlington transistor array (μPA53C) to drive the LED display.

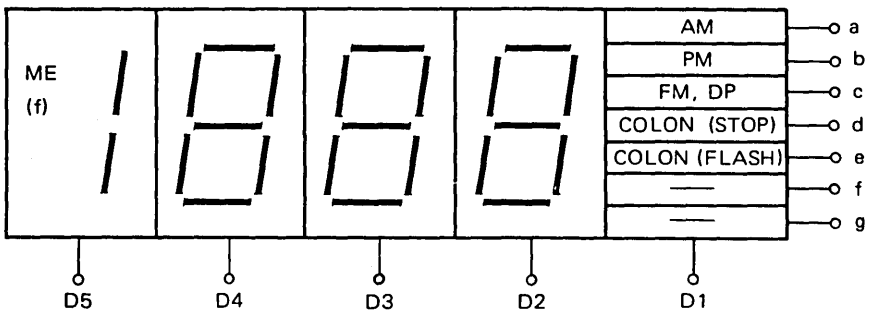
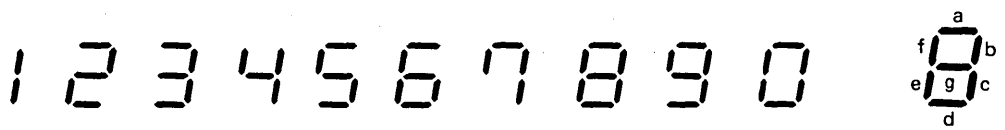


Fig. 4

* **Display format**

○ Segment Pattern



* **Display brightness control (DIMMER)**

DIM This switch is for selection of display brightness.

ON – – – – Display brightness is reduced. (Duty factor: 1/32)

OFF ––––– Display brightness is ordinary. (Duty factor: 1/8)

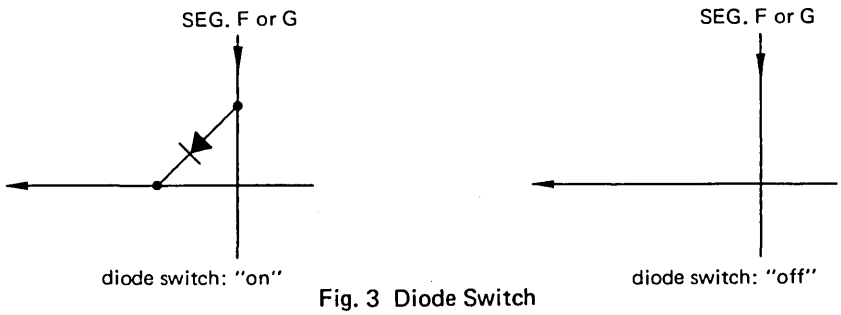


Fig. 3 Diode Switch

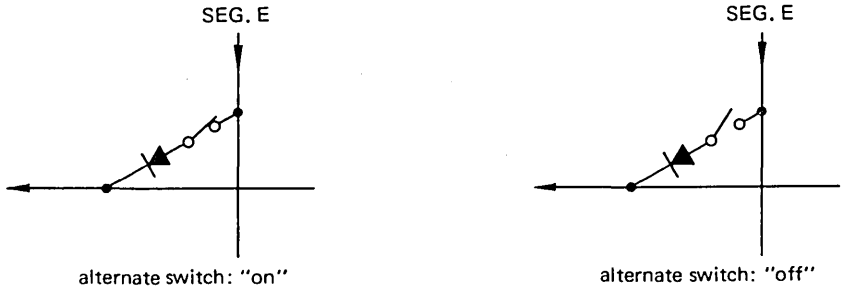
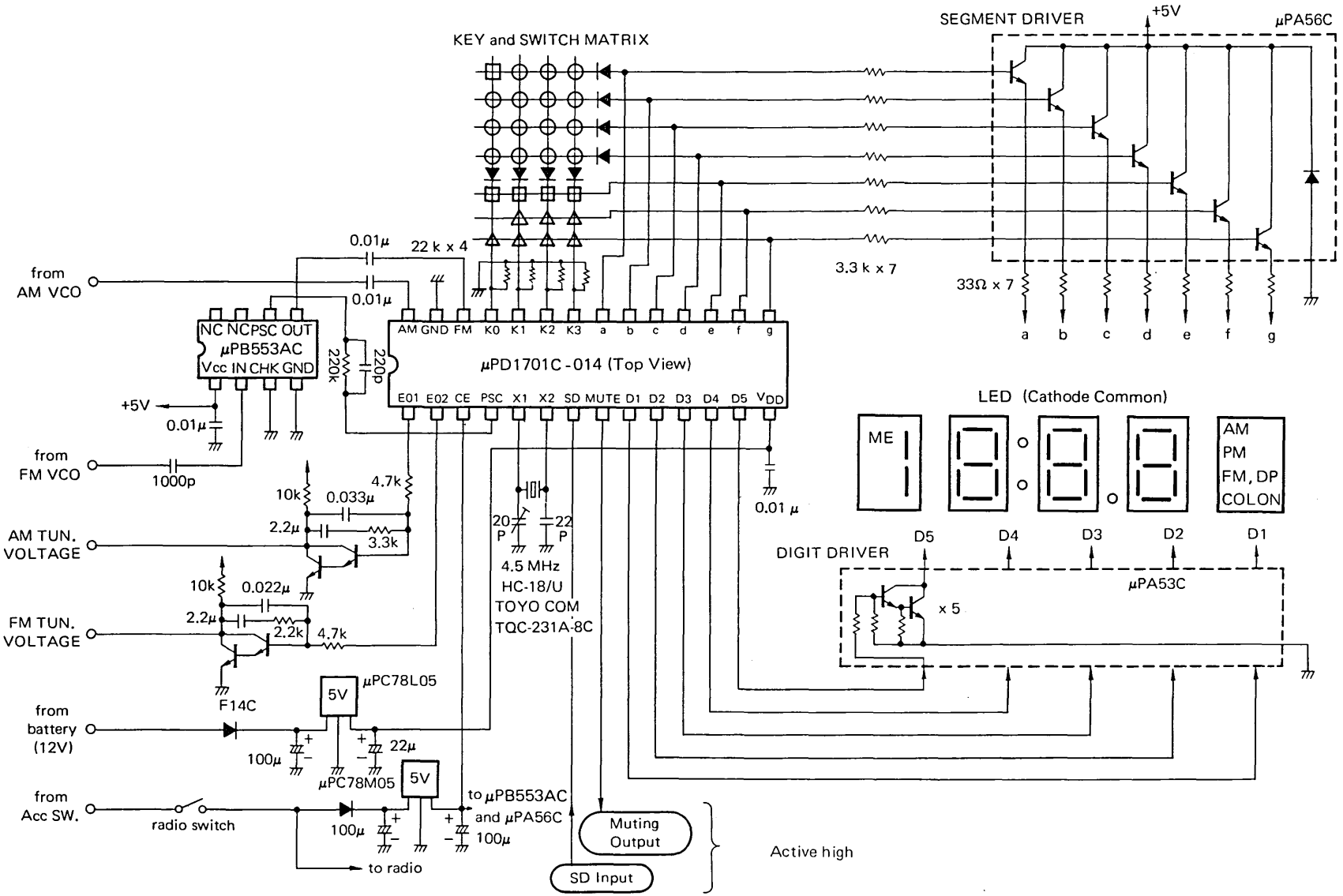


Fig. 4 Alternate Switch

Fig. 5 APPLICATION CIRCUIT



MOS DIGITAL INTEGRATED CIRCUIT
μPD1703C-017

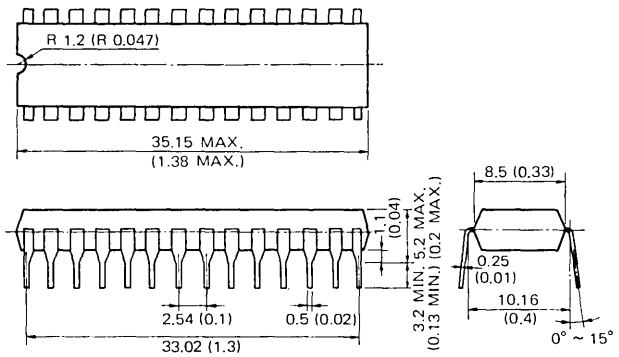
PHASE LOCKED LOOP FREQUENCY SYNTHESIZER
TV DIGITAL TUNING SYSTEM CONTROLLER
CMOS LSI

The μPD1703C-017 is a Single chip CMOS controller designed for using as a Phase Locked Loop Frequency Synthesizer Digital Tuning System Controller for TV. It consists of a PLL and system controller.

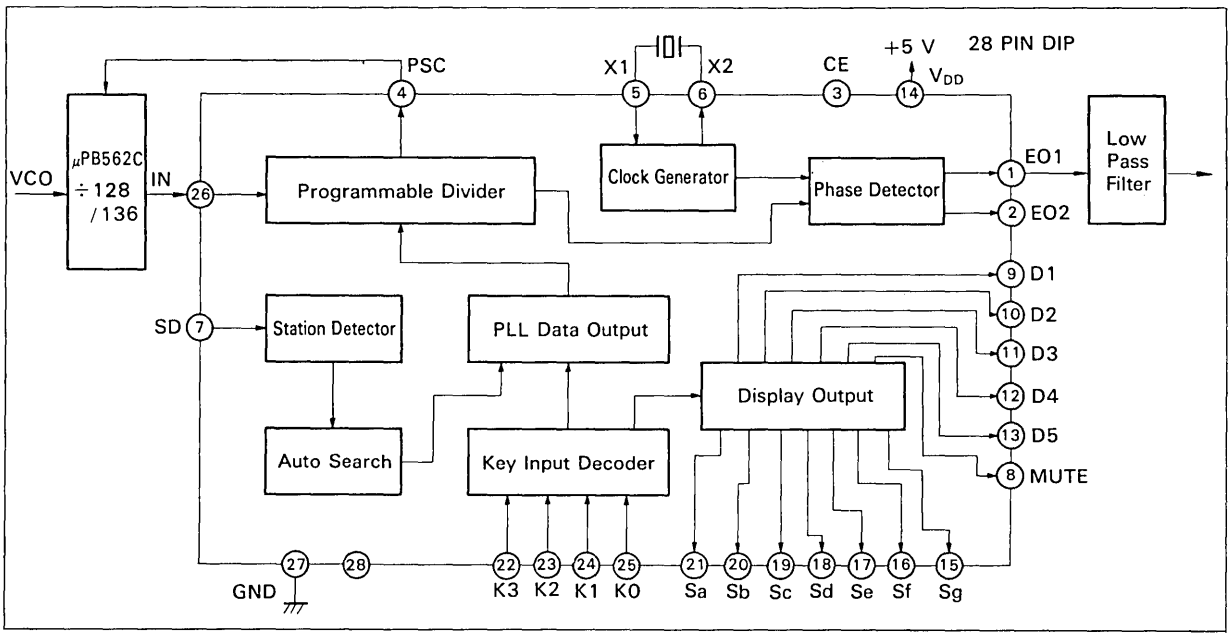
FEATURES

- PLL and Controller is realized in a single chip
- Pulse Swallowing Method using the μPB562C
- VHF/UHF/CATV in U.S. and CANADA
- Direct tuning by 10 keys and automatic up or down search
- Last station memory
  TV: 1 station, CATV: 1 station (M/S . . . off)
- Manual fine tuning (1 step: 40 kHz ±2 MHz MAX.)
  Fine tuned station memory in VHF and CATV
- Function of remote control
- 28 pin slim dual in-line package (DIP)
- High speed and low power consumption due to CMOS
- Single power supply: V_{DD} = 5 ± 0.5 V
- Low stand-by current . . . . . less than 10 μA(CE . . . low)

PACKAGE DIMENSIONS in millimeters (inches)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{DD}	-0.3 to +6.0	V
Input Voltage	V_I	-0.3 to V_{DD}	V
Output Voltage	V_O	-0.3 to V_{DD}	V
Output Breakdown Voltage *	V_{BDS}	-35	V
Output Current	I_{OH}	-10	mA
Storage Temperature	Tstg	-55 to +125	°C
Operation Temperature	Topt	-35 to +75	°C

*: Segment Output Terminals (P-ch open drain)

ELECTRICAL CHARACTERISTICS (Ta=-35 to +75°C, V_{DD}=4.5 to 5.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
High Level Input Voltage	V_{IH1}	0.8V_{DD}		V_{DD}	V	SD terminal
	V_{IH2}	0.7V_{DD}		V_{DD}	V	CE terminal
	V_{IH3}	0.6V_{DD}		V_{DD}	V	K0 to K3 terminals
Low Level Input Voltage	V_{IL1}	0		0.3V_{DD}	V	CE terminal
	V_{IL2}	0		0.2V_{DD}	V	SD, K0 to K3 terminals
High Level Output Voltage	V_{OH1}	4.0			V	EO,D,MUTE: I_{OH}=-0.5 mA
	V_{OH2}	3.0			V	SEG: I_{OH}=-0.5 mA
	V_{OH3}	4.0			V	PSC: I_{OH}=-0.2 mA
Low Level Output Voltage	V_{OL1}			0.5	V	EO: I_{OL}=0.5 mA
	V_{OL2}			0.5	V	D,MUTE,PSC: I_{OL}=0.2 mA
High Level Input Current	I_{IH}	5.0	25	100	μA	K: V_I=V_{DD}=5.0 V
Frequency Response	fin	0.5		8.8	MHz	vi=0.8 Vp-p, DC cut
Supply Voltage Rise Time	Tr			0.5	s	V_{DD}: 0 → 4.5 V
Supply Current	I_{DD}			10	μA	CE: Low Level
Output Off Leak Current	I_{OFF}			-5.0	μA	SEG: V_{DS}=-30 V

OUTLINE OF FUNCTIONS

(1) BANDS

VHF/UHF/CATV in U.S. and CANADA

- M/S . . . off

  VHF : 2 ch – 13 ch
  UHF : 14 ch – 83 ch
  CATV : A ch – W ch

- M/S . . . on

  VHF : 2 ch – 13 ch
  UHF : 14 ch – 83 ch
  CATV : A ch – I ch

(2) FUNCTION OF TUNING

- Direct tuning by 10 keys
- Automatic up or down search

(3) MANUAL FINE TUNING (MFT)

- 1 step: 40 kHz ± 2 MHz MAX
- Fine tuned station memory in VHF and CATV

  M/S: on . . . VHF (2 ch – 13 ch) and mid-band (A ch – I ch)
  M/S: off . . . mid-band and super-band (A ch – W ch)

(4) AUTO FINE TUNING (AFT)

- 1 step: 40 kHz ± 2 MHz MAX
- 1 cycle: 5 ms

(5) FUNCTION OF REMOTE CONTROL

- Use of the μPD1986C (transmitter) and the μPD1937C (receiver)

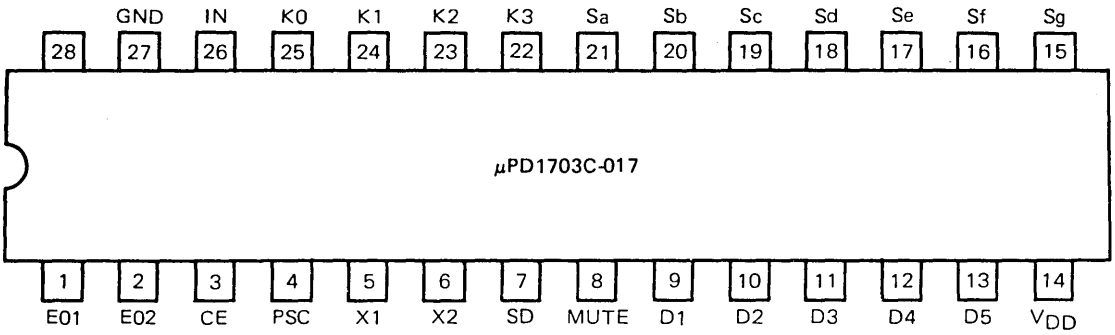
(6) DISPLAY

- Dynamic display of 3 digits (cycle: 150 Hz)

(7) REFERENCE FREQUENCY

- 5 kHz

PIN CONNECTION (Top View)



EXPLANATION OF INPUT AND OUTPUT TERMINALS

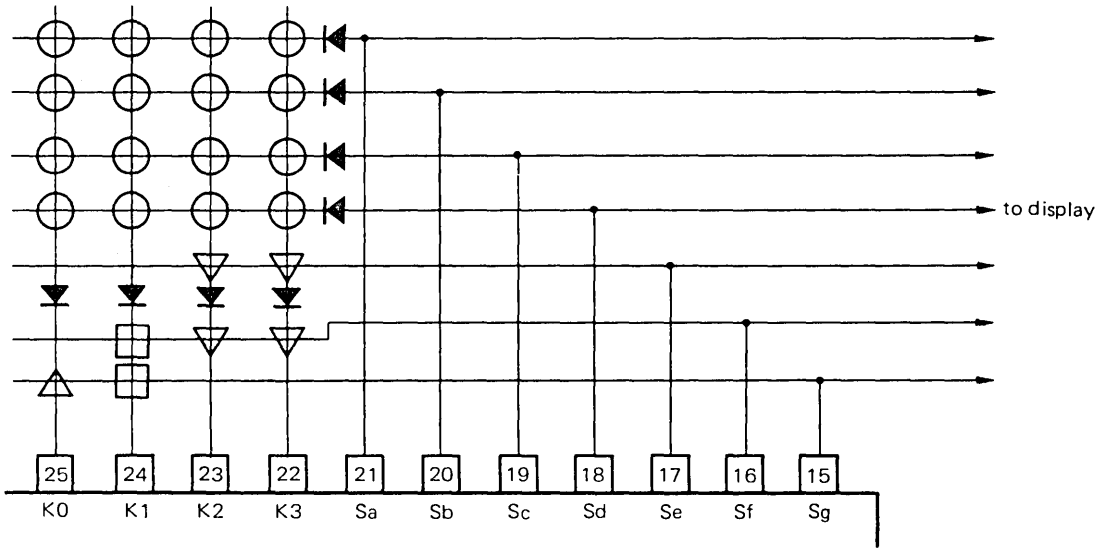
EO1 EO2	These three-state outputs are used (via active filters) to supply analog voltages to the tuner varicap for controlling the local osc.
CE	This input is used to designate the stand-by mode to the chip. It is low to designate the stand-by mode (display: off, PLL: off, system clock: stop).
PSC	This output is used to control the division ratio of the two-modulus prescaler (μPB562C).
X1,X2	These inputs are for connection to a 4.5 MHz crystal.
SD	This input is used to control the station searching operation (CHU/CHD). It is high to indicate the presence of a station and the operation is terminated.
MUTE	This output line is high to mute the TV set in the case of station change, band change, and so on.
D1 to D5	These outputs are used as digit drivers for the display.
V_{DD}	This is a 4.5 to 5.5 volt supply for the chip.
Sa to Sg	These outputs are used as segment drivers for the display. They are also used as vertical drive for the control key and mode switch matrix.
K0 to K3	These inputs are from seven by four matrix. Various functions are entered through the matrix. These inputs are provided with internal pull down resistors.
IN	This is the local oscillator input.
GND	System ground.

* Please keep 28 pin open because it is pulled up internally.

COMPOSITION OF KEYS

	K3 (22)	K2 (23)	K1 (24)	K0 (25)
Sa (21)	1	2	3	CLR
Sb (20)	4	5	6	FTU
Sc (19)	7	8	9	FTD
Sd (18)	CHD	0	CHU	FTR
Se (17)	RCD	RCU		
Sf (16)	AFTD	AFTU	AFT	
Sg (15)			CATV/TV	M/S

CONNECTION TO THE MATRIX OF KEYS

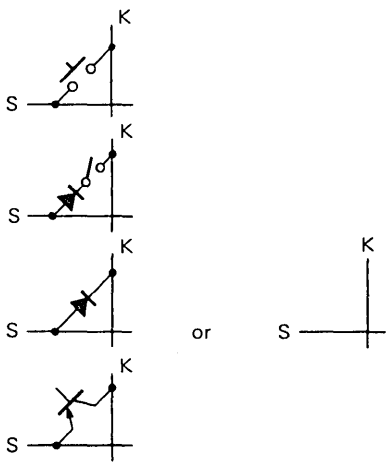


momentary key switch

alternate switch

diode

transistor



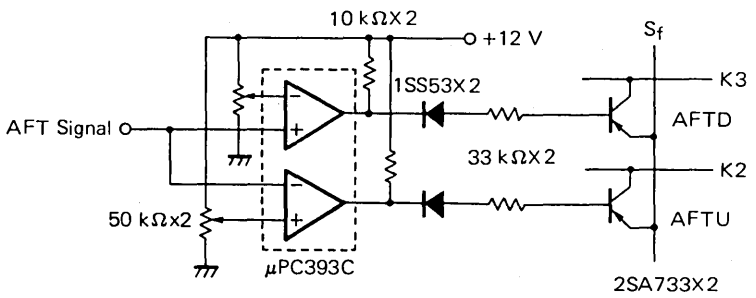
EXPLANATION OF CONTROL KEYS

- 0–9 (10 keys) — These keys are used for direct tuning. Each station is tuned by using two keys within them (EX, 8 ch: 0, 8, 12 ch: 1, 2). If a second key is not depressed within 4 seconds from when a first key was depressed, a first key is cancelled. If wrong ch is selected, the μPD1703C-017 shows the error.
- CLR (Clear) — This key is used for cancelling a first key when a wrong key (within 10 keys) is depressed first (EX. 8 ch: 8, CLR, 0, 8).
- FTU, FTD (Fine Tuning Up) (Fine Tuning Down) — These keys are used for manual fine tuning. While these keys are depressed, tuning frequency increases (or decreases) by 40 kHz at every 125 ms. The range is ±2 MHz. In VHF and CATV bands (M/S: off . . . mid-band and super band, M/S: on . . . VHF band and mid band), fine tuning condition can be memorized at each channel (1 step: 320 kHz). In UHF band, it returns to each initial condition when other channels are selected.
- CHU, CHD (Channel Up) (Channel Down) — These keys are used for automatic up (or down) search. While these keys are depressed, tuning frequency increases (or decreases) to the next station at every 750 ms. Interval time can be shortened by repeating the depressing of them.
- FTR (Fine Tuning Reset) — This key is used for resetting fine tuning condition of a current channel.

EXPLANATION OF MODE SWITCHES

- AFT (Auto Fine Tuning) — This switch is used for selecting the mode of fine tuning. While this is on, AFT is effective but MFT is ineffective. In this case, frequency changes automatically by 40 kHz according to the external AFT signal. While this is off, AFT is ineffective but MFT is effective.
- CATV/TV (Band Switch) — This switch is used for selecting CATV or TV band. While this is on, VHF and CATV bands are selected. While this is off, VHF and UHF bands are selected.

APPLICATION OF AFT



* Please keep the time constant of AFT signal less than 5 ms.

EXPLANATION OF A DIODE

M/S	FUNCTION
off	VHF and UHF or mid-band and super-band can be tuned with CATV/TV switch.
on	VHF, UHF and mid-band can be tuned without CATV/TV switch.

* RELATION BETWEEN CATV CHANNEL AND INPUT CHANNEL NUMBER

●M/S : off

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W
14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36

●M/S : on

A	B	C	D	E	F	G	H	I
84	85	86	87	88	89	90	91	92

EXPLANATION OF BAND SIGNAL OUTPUTS

Band signals are out from four segment outputs (Sa, Sb, Sc and Sd) when D_5 is on.

segment / band	Sa	Sb	Sc	Sd
VL	H	L	L	L
VH,MB	L	H	L	L
SB	L	H	L	H
UB	L	L	H	L

H: high level, L: low level

EXPLANATION OF REMOTE CONTROL SYSTEM

The μPD1703C-017 can be remotely controlled by using the μPD1986C (transmitter) and the μPD1937C (receiver).

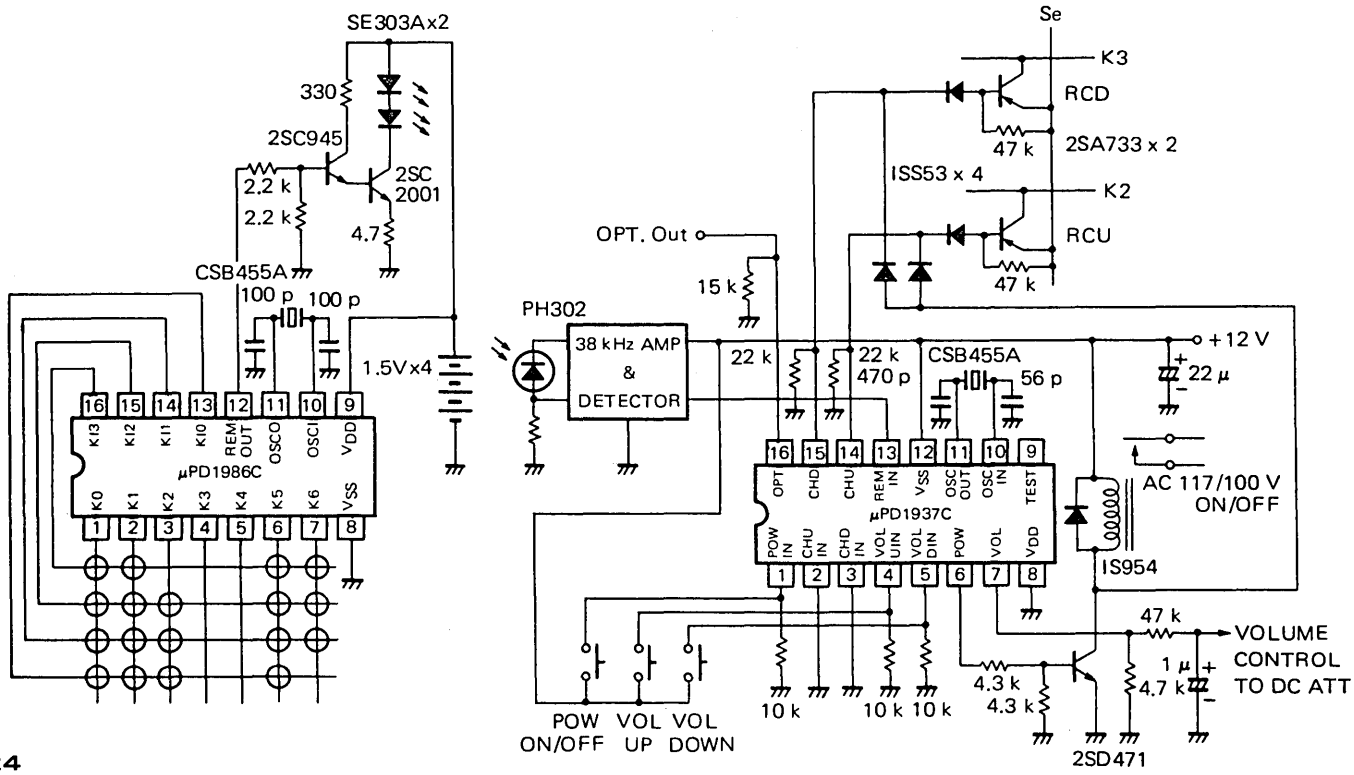
* OUTLINE OF FUNCTIONS

- Direct tuning by 10 keys
- Automatic up or down search
- Function of clear (CLR)
- Power on/off
- Muting on/off
- Volume up/down (32 step)
- One option

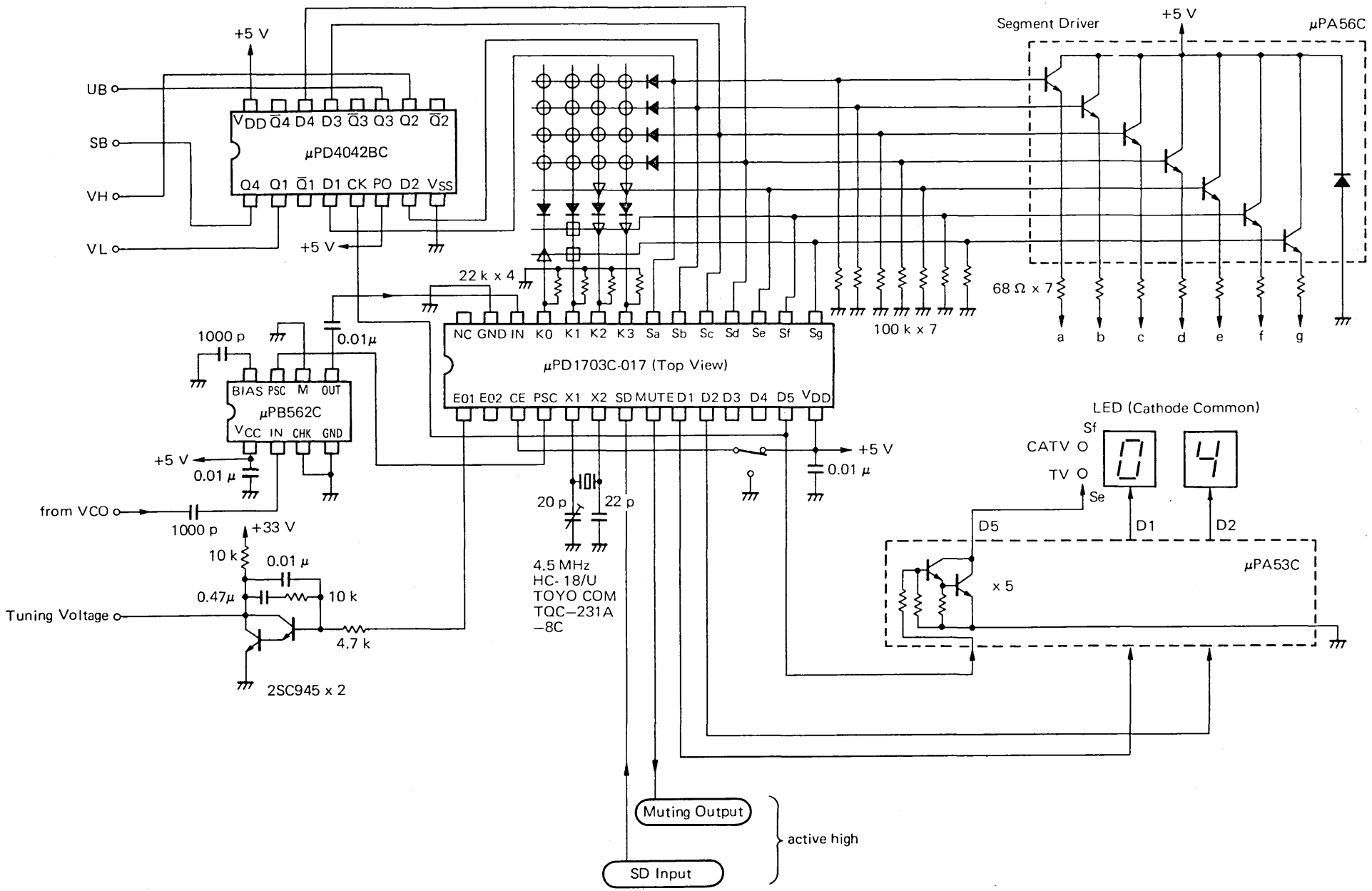
* COMPOSITION OF KEYS AT THE μPD1986C

	K13 (16)	K12 (15)	K11 (14)	K10 (13)
K0 (1)	3	2	1	0
K1 (2)	7	6	5	4
K2 (3)		CLR	9	8
K3 (4)				
K4 (5)				
K5 (6)	CHU	CHD	VOLU	VOLD
K6 (7)	POW	OPT	MUTE	

APPLICATION OF REMOTE CONTROL SYSTEM



APPLICATION CIRCUIT



MOS DIGITAL INTEGRATED CIRCUIT
μPD1703C-018

PLL FREQUENCY SYNTHESIZER AND CONTROLLER FOR LW,MW AND FM TUNERS

The μPD1703C-018 is CMOS LSI with built-in PLL and controller capable of receiving LW/MW/FM in U.S.A.,.Europe and Japan.

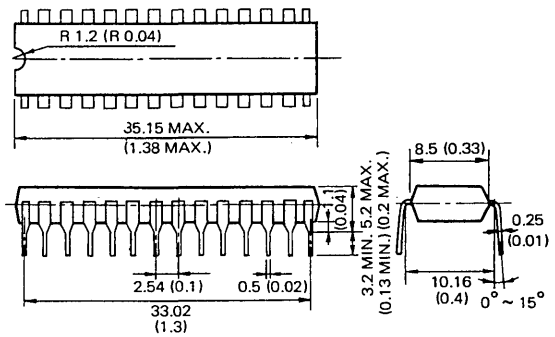
The μPD1703C-018 is provided in a shape of 28-pin Slim DIP (Dual In-Line Package) with less substrate occupying area.

In combination with a dedicated prescaler μPB553AC, μPD1703C-018 is capable of composing high-fidelity LW/MW/FM digital synthesizer tuners for stereo systems such as home stereo systems.

FEATURES

- FIP (Fluorescent Indicator Panel) direct drive capability (segment only).
- Built-in PLL, swallow counter and controller.
- Low data retention current (10 μA or less)
- Capable of preset station display (dot display by LED).
- FM reference frequency is as high as 25 kHz (the pulse swallowing method is employed).
- LW/MW/FM in U.S.A., Europe and Japan are selectable by the initialization switch.
- 9N/9N + 2 switching of LW is possible (9N . . . 153 – 351 kHz, 9N + 2 . . . 155 – 353 kHz).
- Seven (7) buttons-Fourteen (14) preset station memories (7 for FM and 7 for LW + MW).
- Momentary or alternate switches can be used as a preset station key and band selector key (MW·FM).
- Last channel memory is available for each LW/MW/FM band.
- AUTO and MANUAL UP/DOWN selection is possible (saw tooth wave tuning).
- FM IF offset capability (4 ways by 25 kHz step)
- Built-in frequency preset function for adjustment at time of mass production of a set.
- European FM band 4.1/2 digit display (other bands are displayed in 4 digits).
- 28-Pin Slim plastic DIP; saves board area.
- A single power supply of 5 V ± 10 %.

PACKAGE DIMENSIONS in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{DD}	−0.3 to +6.0	V
Input Voltage	V_I	−0.3 to +V_{DD}	V
Output Voltage	V_O	−0.3 to +V_{DD}	V
Output Absorption Current	I_O	10	mA
Operating Temperature	T_{OPT}	−35 to +75	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Output Breakdown Voltage	V_{BDS}	Sa-Sg terminals −35 (Drain source voltage)	V

RECOMMENDED OPERATION CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
RAM Retention Voltage	V_{RAM}	2.5			V	CE terminal = 0
Output Breakdown Voltage	V_{BDS}			−30	V	Sa-Sg terminals (Drain source voltage) I_{OFF}=−5 μA
Supply Voltage Rise Time	T_{rise}			500	ms	V_{DD} = 0 to 4.5 V

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
High Level Input Voltage	V_{IH1}	0.8V_{DD}		V_{DD}	V	SD terminal
"	V_{IH2}	0.7V_{DD}		V_{DD}	V	CE terminal
"	V_{IH3}	0.6V_{DD}		V_{DD}	V	K_0–K_3 terminals
Low Level Input Voltage	V_{IL1}	0		0.3V_{DD}	V	CE terminal
"	V_{IL2}	0		0.2V_{DD}	V	SD, K_0–K_3 terminal
High Level Output Voltage	V_{OH1}	4.0			V	PSC, MUTE, $\overline{D_1}$ – $\overline{D_5}$ terminal I_{OH} = −0.2 mA
"	V_{OH2}	4.0			V	EO_1, EO_2 terminals I_{OH} = −0.5 mA

High Level Output Voltage	V_{OH3}	3.0			V	Sa – Sg terminals I_{OH} = –0.5 mA
Low Level Output Voltage	V_{OL1}			0.5	V	EO_1, EO_2 terminals I_{OL} = 0.5 mA
"	V_{OL2}			0.5	V	MUTE, $\overline{D_1}$ – $\overline{D_5}$, PSC terminals I_{OL} = 0.2 mA
High Level Input Current	$+I_{IH1}$	5.0	25	100	μA	K_O – K_3 terminals $V_{IN} = V_{DD}$ = 5.0 V
"	$+I_{IH2}$		300		μA	X_1 terminal $V_{IN} = V_{DD}$ = 5.0 V
Low Level Input Current	$-I_{IL1}$		300		μA	AM, FM terminals V_{IN} = OV, V_{DD} = 5.0 V
Output Leakage Current	I_L		10^{-3}	1	μA	EO_1, EO_2 terminals $V_O = V_{DD}$ = 5.0 V
AC Input Voltage	Vin	1.0		V_{DD}	V_{P-P}	AM, FM terminals
Response Frequency	f_{AM}	0.5		2.5	MHz	AM terminal, V_{in}=1.0 V_{P-P} (MIN.), DC cut
"	f_{FM}	0.5		8.8	MHz	FM terminal, V_{in}=0.8 V_{P-P} (MIN.), square wave, DC cut
Operating current	I_{DD1}		3		mA	Normal operation (excluding display current)
"	I_{DD2}			10	μA	CE terminal = 0 Ta = 25 °C, V_{DD} = 5 V
RAM Retention Voltage	V_{RAM}	2.5			V	CE terminal = 0
Output Breakdown Voltage	V_{BDS}			–30	V	Sa – Sg terminals (Drain source voltage), I_{OFF}=–5 μA

OUTLINE OF FUNCTION

Receiving Frequency, Channel Spacing, Reference Frequency, Intermediate Frequency

		Frequency Range	Channel Spacing	Reference Frequency	IF
U.S.A.	MW1	530 ~ 1 620 kHz	10 kHz	10 kHz	450 kHz
	MW2	522 ~ 1 611 kHz	9 kHz	9 kHz	
	FM	87.9 ~ 107.9 MHz	200 kHz	25 kHz	10.650, 10.675, 10.700, 10.725 MHz
Europe	MW	522 ~ 1 611 kHz	9 kHz	9 kHz	450 kHz
	LW1	155 ~ 353 kHz	9 kHz	1 kHz	
	LW2	153 ~ 351 kHz	9 kHz	1 kHz	
	FM	87.50 ~ 108.00 MHz	50 kHz	25 kHz	10.650, 10.675, 10.700, 10.725 MHz
Japan	MW	522 ~ 1 611 kHz	9 kHz	9 kHz	450 kHz
	FM	76.1 ~ 89.9 MHz	100 kHz	25 kHz	10.675, 10.700, 10.725, 10.750 MHz

Tuning Functions

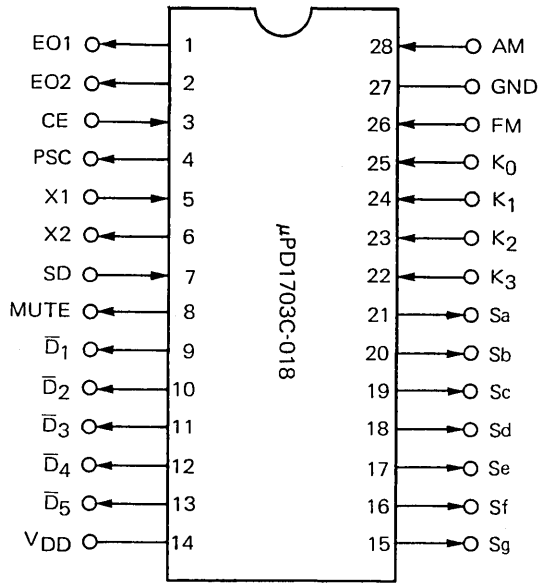
(1) AUTO UP/DOWN TUNING (Saw Tooth Wave Mode).
When a high level is input at SD terminal, the auto tuning is stopped and signal from that station is continuously received.

(2) MANUAL UP/DOWN TUNING (Saw Tooth Wave Mode)
Step forwarding by the momentary switch. Further, when the switch is kept depressed for more than 0.5 sec., the receiving frequency is continuously forwarded till the switch is released.

(3) Preset Memory Calling
FM . . . . . 7 channels (M1 – M7)
LW + MW . . . . . 7 channels (M1 – M7)
FM and LW+MW are of 7 channels independent preset type. LW and MW are of total 7 channels random access preset type.

DESCRIPTION OF TERMINALS

Terminal Configuration Diagram (Top View)



Terminal No.	Symbol	Terminal Name	Description
1 2	EO_1 EO_2	Error Out	Charge pump output from the phase detector composing PLL. When the divided oscillation frequency is higher than the reference frequency, these terminals go high, and when lower than reference frequency, low level is output. When both are in accord with each other, the terminal become floating. As the same signal is simultaneously output on EO_1 and EO_2, these terminals may be connected to either LPF (Low Pass Filter) of MW, LW or FM.
3	CE	Chip Enable	Activation of this device is controlled by this terminal. When the device is to be normally operated, set this terminal at the high level, and when the device is not used, set at the low level. High level . . . Normal operation Low level . . . Memory retantion state (stand-by current is 10 μA or less. Display is OFF, PLL is stopped functioning, internal clock generator is stopped.) Note that CE terminal only accepts the pulse that is longer than 134 μs. Be sure to force this terminal high after the V_{DD} terminal is 4.5 V or above.
4	PSC	Prescaler Control	This terminal outputs a signal to switch the modulo of the two-modulus prescaler when a pulse swallowing method is used for frequency division (in case of FM). This terminal should be connected to PSC terminal of a dedicated two-modulus prescaler μPB533AC.
5 6	X1 X2	X'tal	The X'tal oscillator terminals. A 4.5 MHz X'tal should be connected to these terminals. (Toyo Tsushinki: TQC-231A-8A is recommended)
7	SD	Station Detector	When this terminal is forced to high level in AUTO TUNING (AUTO UP/DOWN) mode, the scanning is quitted. A high level signal should be input within 75 ms after PLL is locked.
8	MUTE	MUTE	This terminal outputs an active-high signal for muting shock noise when PLL is out of lock. When CE terminal is forced to low level (back-up state), this terminal is forced to low level unconditionally. The length of the muting signals are as follows. At time of LW/MW/FM switching . . . 700 ms (TYP.) At time of MANUAL UP/DOWN . . . 200 ms (TYP.) (1 step operation) At time of AUTO UP/DOWN . . . 200 ms (TYP.) (after SD terminal is forced to high level.) At time of Preset Memory calling . . . 450 ms (TYP.) Above show the muting signal which is output just after PLL data are changed. Actually, premuting time of 50 ms (before PLL data change) is added for. (For details, see MUTE Timing Chart on Page 645.)

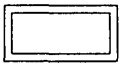
9 ~ 13	$\overline{D}_1 - \overline{D}_5$	Digit Outputs	These terminals are the display digital signal outputs and are active-low. (For details, see the display connection diagram on Page 640.)
14	V_{DD}	V_{DD}	This is the power supply terminal of the device. When the device is in operation, 5 V±10 % should be supplied. Under the preset memory back-up condition, supply voltage can be reduced to 2.5 V. Note that the rise time of supply voltage V_{DD} must be 500 ms or less. If the rise time is excessively long, the initialization will not be operate properly.
15 ~ 21	Sa – Sg	Segment Outputs	These terminals are the display segment signal outputs and key return signal source terminals, and are active-high. (For configuration of key matrix see Page 632.) As these terminals withstand voltage up to –30 V, they can be directly connected to the segment terminal of FIP (Fluorescent Indicator panel). (For details see the display connection diagram on Page 640.)
22 – 25	$K_0 - K_3$	Key Return Signal Inputs	These terminals are the input terminals of key return signals from the external key matrix. (For details see the key matrix configuration shown on Page 637.)
26	FM	FM Local Oscillator Signal Inputs	FM local oscillator divided in 1/16 or 1/17 by the prescaler μPB553AC is input into this terminal. As an AC amplifier is built in, signals should be input after DC is cut by a capacitor.
27	GND	GND	This terminal should be connected to a system ground.
28	AM	AM Local Oscillator Signal Inputs	Signals from MW and LW local oscillator are input to this terminal. As an AC amplifier is built in, signals should be input after DC is cut.

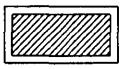
1. CONFIGURATION OF KEY MATRIX

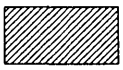
1-1 Arrangement of Key Matrix

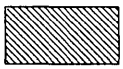
Input Terminal / Output Terminal	K0 (25)	K1 (24)	K2 (23)	K3 (22)
Sa (21)	DOWN	UP	MEMORY	TRACKING POINT PRESET
Sb (20)	M4	M3	M2	M1
Sc (19)		M7	M6	M5
Sd (18)		LW	FM	MW
Se (17)				
Sf (16)	9 kHz/10 kHz	9N/9N + 2	AUTO/MANUAL	
Sg (15)	BAND0	BAND1	IF1	IF0

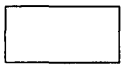
( ) is Terminal No.


: Momentary Switch

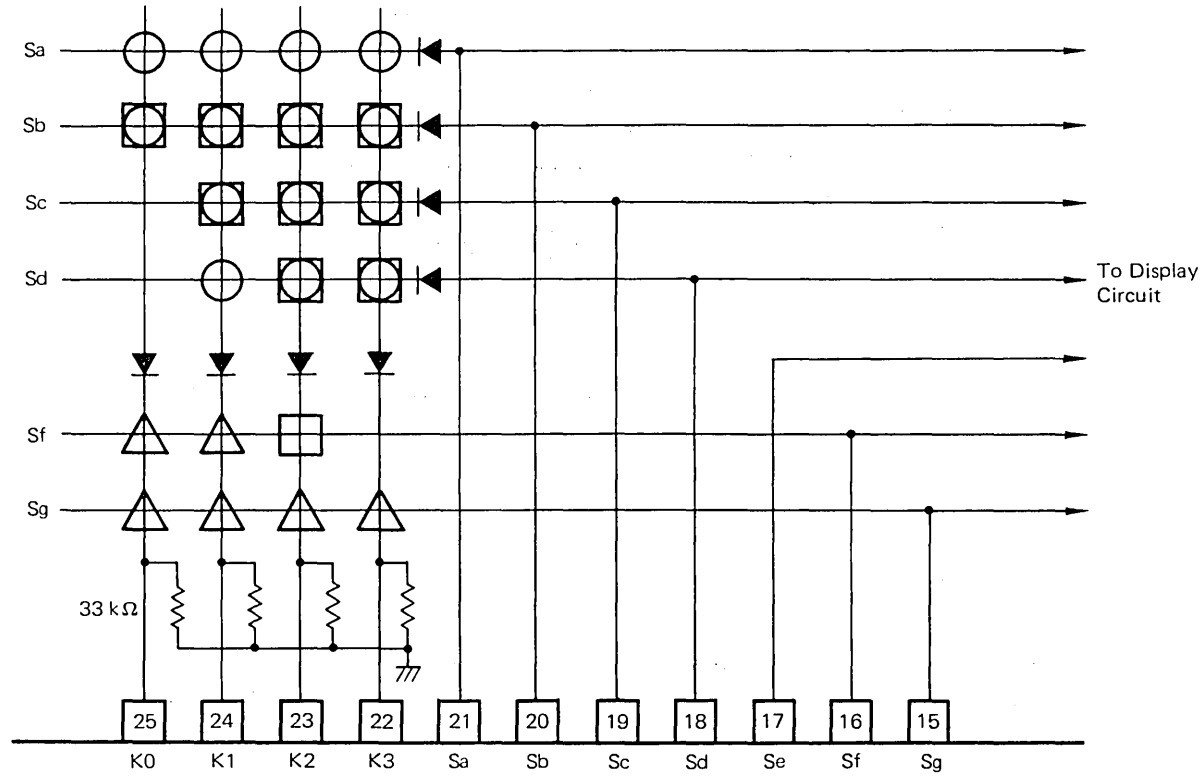

: Momentary or Alternate Switch

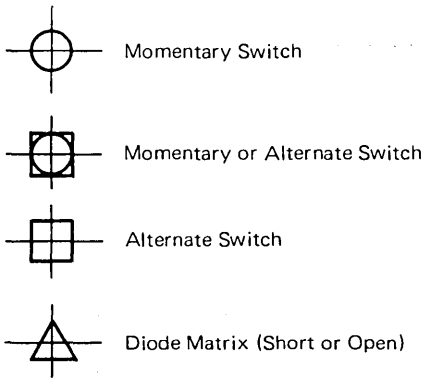

: Alternate Switch

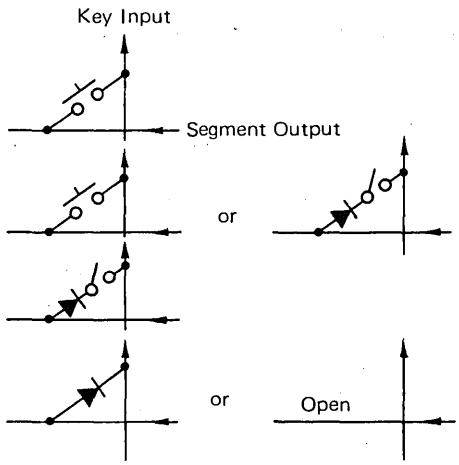

: Diode Matrix (Short or Open by Diode)


: Open

1-2. Connection of Key Matrix and Type of Switch



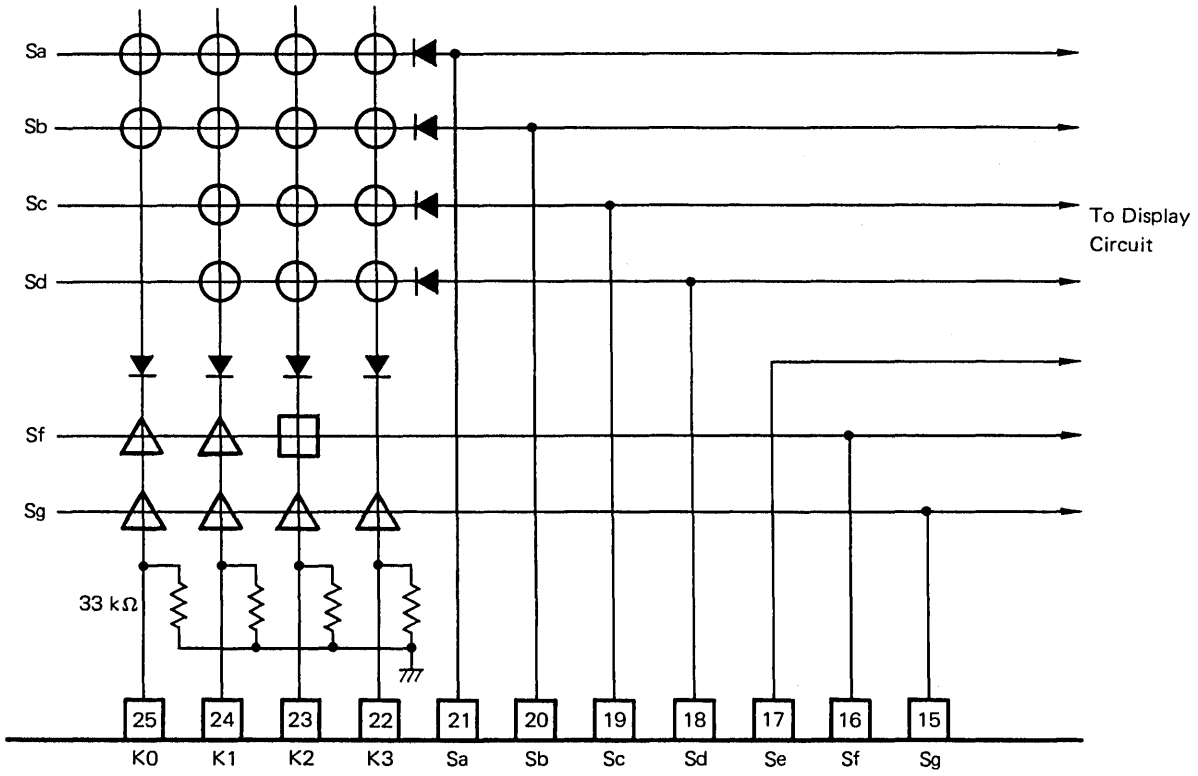




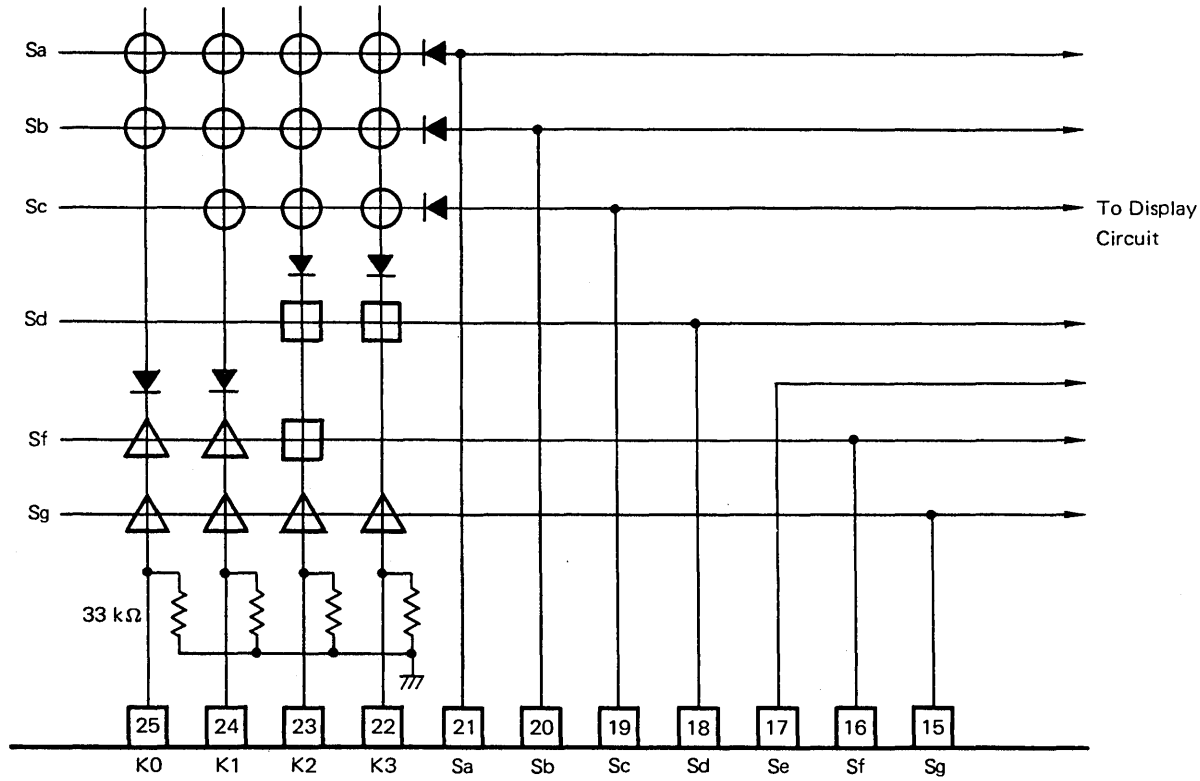
As the preset station Keys (M1 – M7) and Band Selector Keys (FM, MW), either Momentary or Alternate Switch can be used. However depending upon which switch is used, an inserting position of diodes (for preventing turn-around of key return signal) may differ.

The following shows the examples;

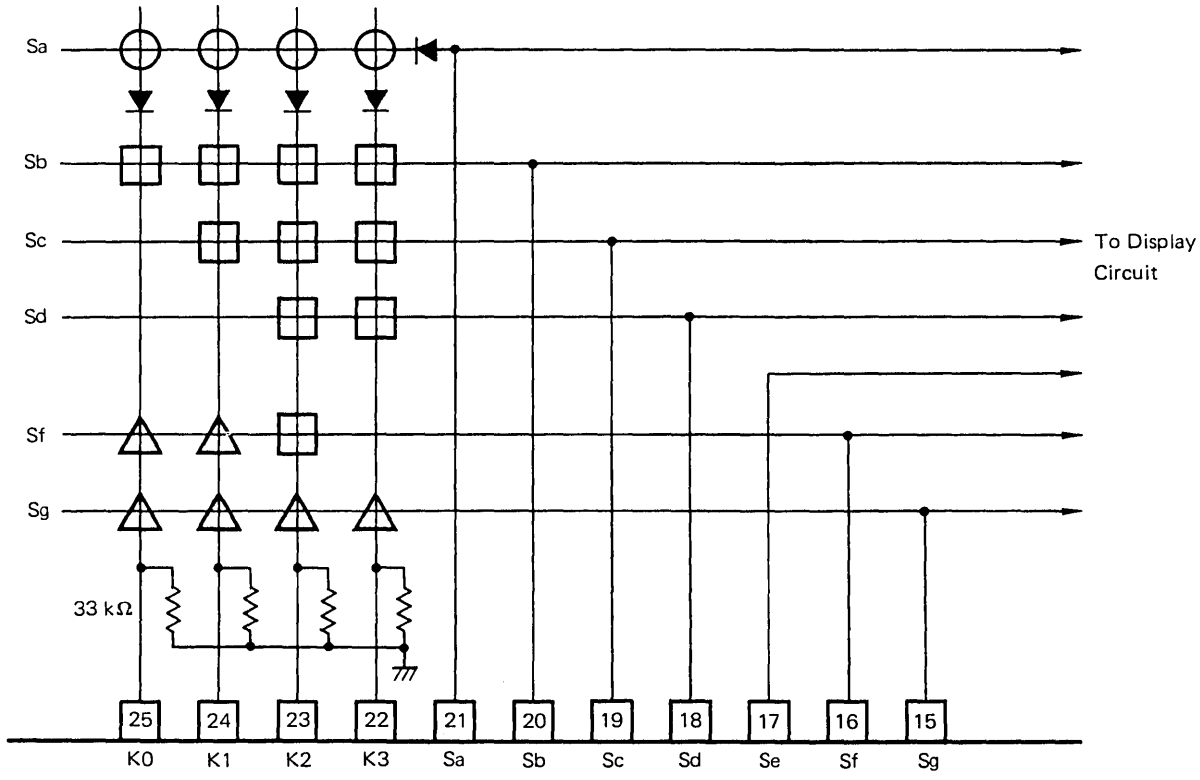
Example 1: When Momentary switches are used as Preset station Keys and Band Selector Keys.



Example 2: When Alternate Switches are used as Band Selector Switches.



Example 3: When Alternate Switches are used as Preset station Keys and Band Selector Keys.



(Note) LW Key cannot be used as Alternate Switch.

2. DESCRIPTION OF KEY MATRIX

2-1. Initialization Diode Matrix

Initialization Diode Matrix is available in 4 types as shown below. These matrixes are read in when power is initially supplied to V_{DD} (initialize) and when CE terminal is changed from low level to high level. However, the 9 kHz/10 kHz and 9N/9N+2 Switches are constantly read in. Even in this case, PLL data and display are changed only when a momentary switch (UP, DOWN, M1 – M7 Switches) is depressed.

(1) Switches for specifying IF offset of FM

IF1, IF0

(2) Switches for specifying FM band area (U.S.A., Europe, Japan)

BAND 1, BAND 0

(3) Switches for specifying MW band channel spacing and reference frequency

9 kHz/10 kHz

(4) Switche for selecting LW band frequency range

9N/9N+2

These initializations will be performed by shorting or opening the intersecting points on the matrix by Diode. (In the following table, "1" means shorting by Diode and "0" means opening.)

<table>
<tr><th>Symbol</th><th>Description of Function</th></tr>
<tr><td>IF1

IF0</td><td>Switches for specifying IF offset frequency of FM.
IF offset can be varied in 4 levels, as shown below, by 25 kHz step without changing indicated frequency:
<table>
<tr><th>IF1</th><th>IF0</th><th>U.S.A. Band</th><th>European Band</th><th>Japanese Band</th></tr>
<tr><td>0</td><td>0</td><td>10.700 MHz</td><td>10.700 MHz</td><td>10.700 MHz</td></tr>
<tr><td>0</td><td>1</td><td>10.725</td><td>10.725</td><td>10.675</td></tr>
<tr><td>1</td><td>0</td><td>10.650</td><td>10.650</td><td>10.750</td></tr>
<tr><td>1</td><td>1</td><td>10.675</td><td>10.675</td><td>10.725</td></tr>
</table></td></tr>
<tr><td>BAND1

BAND0</td><td>Switches for specifying FM band areas.
One of FM bands of U.S.A., Europe and Japan can be selected.
<table>
<tr><th>BAND1</th><th>BAND0</th><th>Band Area</th><th>Frequency Range</th><th>Channel Spacing</th></tr>
<tr><td>0</td><td>0</td><td>U.S.A. Band</td><td>87.9 – 107.9 MHz</td><td>200 kHz</td></tr>
<tr><td>0</td><td>1</td><td>European Band</td><td>87.50 – 108.00 MHz</td><td>50 kHz</td></tr>
<tr><td>1</td><td>0</td><td>Japanese Band</td><td>76.1 – 89.9 MHz</td><td>100 kHz</td></tr>
<tr><td>1</td><td>1</td><td>Prohibited *</td><td></td><td></td></tr>
</table>
*Both BAND1 and BAND0 must not be ON (1). If both are ON, the band area will not be properly set.</td></tr>
<tr><td>9 kHz/10 kHz</td><td>Switch for specifying MW band channel spacing, reference frequency and frequency range.
The setting can be independently made regardless of FM band areas (BAND1, BAND0).
<table>
<tr><th>9 kHz/10 kHz</th><th>Frequency Range</th><th>Channel Spacing</th><th>Reference Frequency</th></tr>
<tr><td>0</td><td>530 – 1 620 kHz</td><td>10 kHz</td><td>10 kHz</td></tr>
<tr><td>1</td><td>522 – 1 611 kHz</td><td>9 kHz</td><td>9 kHz</td></tr>
</table></td></tr>
</table>

<table>
<tr><td></td><td>This switch is always read in. However, PLL data and indication will change only when a momentary switch (UP, DOWN, M1 – M7, etc.) is depressed.</td></tr>
<tr><td>9N/9N + 2</td><td>Switch for selecting LW band frequency range.
<table>
<tr><th>9N/9N+2</th><th>Frequency Range</th><th>Channel Spacing</th><th>Reference Frequency</th></tr>
<tr><td>0</td><td>155 – 353 kHz</td><td>9 kHz</td><td>1 kHz</td></tr>
<tr><td>1</td><td>153 – 351 kHz</td><td>9 kHz</td><td>1 kHz</td></tr>
</table>
This switch is always read in. However, PLL data and indication will change only when a momentary switch (UP, DOWN, M1 – M7, etc.) is depressed.</td></tr>
</table>

2-2 Alternate Switch

Symbol	Description of Function
AUTO/ MANUAL	This is an AUTO/MANUAL tuning selector switch. ON (1) . . . AUTO Tuning OFF (0) . . MANUAL Tuning AUTO/MANUAL tuning starts when UP or DOWN momentary switch is depressed after this switch is set at ON or OFF position. (For details see Momentary and Alternate Switches on Page 632.) (Note 1) AUTO tuning operation does not stop even when this switch is changed to MANUAL Tuning during AUTO Tuning operation. If it is desirable to stop AUTO tuning simultaneously with the switching to MANUAL tuning, a system should be so configured that high level signal is constantly supplied to SD terminal during MANUAL tuning. (Note 2) In Auto tuning mode, the μPD1703–018 increases or decreases frequency step by step corfirming that the PLL system is completely locked, in order to scan the band as fast as possible. Therefore if the PLL system is malfunctioning and is not locked, the μPD1703–018 halts the AUTO tuning operation and waites for the PLL to be locked. In this condition, all the keys are not accepted. To escape this condition, force CE terminal to low level then high level, and the frequency can be varied by manual tuning. In the recomended application, the CE terminal is to be connected to the main-power-supply of the set. So the end user can vary the frequency after operating the power-supply-switch, even if the above malfunction occurs.

2.3 Momentary and Alternate Switches

Either momentary Switch or Alternate Switches can be used as Preset Keys (M1 – M7) or Band Selector Keys (MW, FM).

When Alternate Switches are used for Preset station Key, the interlocking including UP and DOWN Keys is required.

<table>
<tr><th>Symbol</th><th>Description of Function</th></tr>
<tr><td>TRACKING
POINT
PRESET</td><td>
This switch is used to write frequencies for tracking adjustment at factory into the preset memories. When this switch is depressed, following frequencies are written into the preset memories (M1 – M7):
FM
(1) When U.S.A. Band (BAND1=0, BAND0=0) is set:
<table>
<tr><td>M1</td><td>M2</td><td>M3</td><td>M4</td><td>M5</td><td>M6</td><td>M7</td></tr>
<tr><td>89.7 MHz</td><td>101.7 MHz</td><td>87.9 MHz</td><td>87.9 MHz</td><td>92.9 MHz</td><td>–</td><td>–</td></tr>
</table>
(2) When European Band (BAND1=0, BAND0=1) is set:
<table>
<tr><td>M1</td><td>M2</td><td>M3</td><td>M4</td><td>M5</td><td>M6</td><td>M7</td></tr>
<tr><td>88.40 MHz</td><td>94.40 MHz</td><td>100.40 MHz</td><td>106.0 MHz</td><td>90.0 MHz</td><td>–</td><td>–</td></tr>
</table>
(3) When Japanese Band (BAND1=1, BAND0=0) is set:
<table>
<tr><td>M1</td><td>M2</td><td>M3</td><td>M4</td><td>M5</td><td>M6</td><td>M7</td></tr>
<tr><td>77.0 MHz</td><td>83.0 MHz</td><td>89.0 MHz</td><td>76.1 MHz</td><td>78.6 MHz</td><td>–</td><td>–</td></tr>
</table>
MW
(1) When Channel Spacing 9 kHz (9 kHz/10 kHz=1) is set:
<table>
<tr><td>M1</td><td>M2</td><td>M3</td><td>M4</td><td>M5</td><td>M6</td><td>M7</td></tr>
<tr><td>612 kHz</td><td>1503 kHz</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td></tr>
</table>
(2) When Channel Spacing 10 kHz (9 kHz/10 kHz=0) is set:
<table>
<tr><td>M1</td><td>M2</td><td>M3</td><td>M4</td><td>M5</td><td>M6</td><td>M7</td></tr>
<tr><td>630 kHz</td><td>1620 kHz</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td></tr>
</table>
– indicates "Don't Care" (previously stored content is called).
</td></tr>
<tr><td>MEMORY</td><td>This switch is used to write the currently received frequency into Preset Memory.When either one of M1 – M7 Keys is pushed within 5 sec. after this key is pressed, the frequency displayed is written into a memory corresponding to the key pressed.
To release the memory-write-enable state before the 5 sec. push UP/DOWN key or switch LW, MW, FM Bands.</td></tr>
</table>

M1 – M7	These are the preset memory writing and calling keys. It is possible to store FM and MW or LW stations per one button. As MW and LW are of random preset type, storage in optional location in total 7 channels M1 – M7 is possible. (1) Write When either one of M1 – M7 keys is pushed within 5 sec. after MEMORY key is pressed, the frequency currently received is written into a memory corresponding to the key pressed. (2) Calling When either one of M1 – M7 keys is pressed, content (frequency) of a memory corresponding to the key pressed is called out. When a preset key is pressed, a mute signal of approximately 450 ms is output. And when frequency bands are switched (LW ⟶ MW or MW ⟶ LW), a mute signal of approximately 750 ms is output. (For details see MUTE Timing Chart on Page 645.)
UP DOWN	These are AUTO and MANUAL tuning keys. When these keys are pressed, the following operations are executed: (1) When AUTO/MANUAL Switch is set at AUTO: ○When UP key is pressed, frequency is continuously kept going up in saw tooth wave form. If a high level is input in SD terminal at this time, AUTO UP operation is stopped. When DOWN key is pressed during AUTO UP mode, the mode changes to AUTO DOWN operations. ○The operation of DOWN key is almost the same as UP key. The only difference is that this key decreases the frequency. *1. In AUTO UP or DOWN operation, frequency is going up or down at the speed of 80 ms/step. *2. When UP key is pressed in AUTO UP operation or DOWN key in AUTO DOWN operation, AUTO UP/DOWN operation is kept continued. In addition, when UP or DOWN key is kept pressed, AUTO UP or DOWN operation does not stop even when the SD terminal is forced to highllevel.
MW FM LW	These are FM, MW and LW band selector switches. Alternate Switches may be used for FM and MW. (Alternate Switch cannot be used for LW.) When the bands are switched, a MUTE signal of approx. 750 ms is output through MUTE terminal.

3. DESCRIPTION OF DISPLAY

3-1 Desplay Connection Diagram

The display connection diagram is shown below. D1 – D5 and Sa – Sg correspond to the digit terminals ($\overline{D1}$ – $\overline{D5}$) and the segment terminals (Sa – Sg) of μPD1703C-018.

The segment terminals of μPD1703C-018 are capable of withstanding voltage up to −30 V (P-ch open drain output) and it is therefore possible to connect these terminals direct to FIP (Fluorescent Indicator Panel).

The digit lines should be connected to FIP via one-stage buffers (PNP transistor), because those outputs are CMOS-complementary-type and active-low.

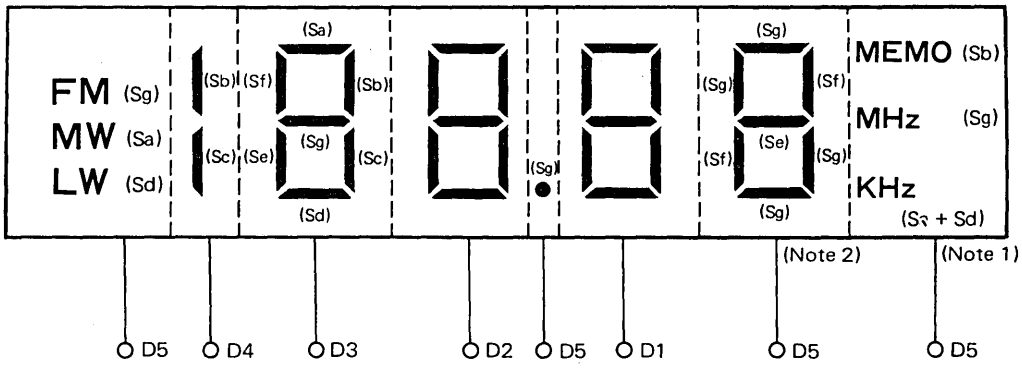


Fig. 1 Display Connection Diagram

(Note 1) Display of "kHz" is made by OR signal of Sa and Sd. If no LW is available, "kHz" can be displayed by Sa only.

(Note 2) This is the digit for "50 kHz" in Europe an FM. Note that this digit is controlled by only 3 segment lines; Se, Sf and Sg, and organized the number "5" and "0".
In MW and LW, nothing is displayed here. For FM in U.S.A. and Japan, don't connect the D5 or Sg line in this digit.

3-2 Examples of Display

Shown below are examples of display when FIP shown in Fig. 1 is used.

(1) FM in U.S.A.

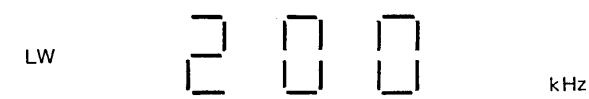
(2) FM in Europe

(3) FM in Japan

(4) **MW** (Channel Spacing 10 kHz)

(5) **MW** (Channel Spacing 9 kHz)

(6) LW in Europe



* MEMO Display lights up for 5 sec. after the momentary key MEMORY is pressed.

When Preset Station key M1 – M7 is pressed following the MEMORY key, the currently received frequency is written and then the MEMO display disappears.

4. PRESET STATION INDICATORS*

An example of the preset station indicator circuit is shown in Fig. 2. The timing chart at this time is shown in Fig. 3.

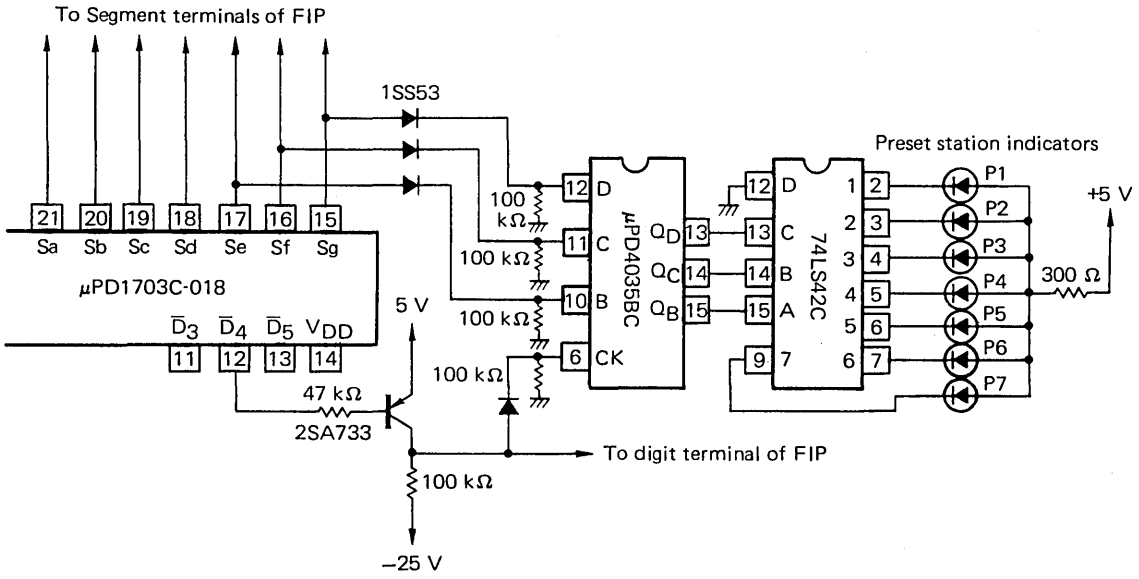


Fig. 2 Example of Preset Station Display Connection

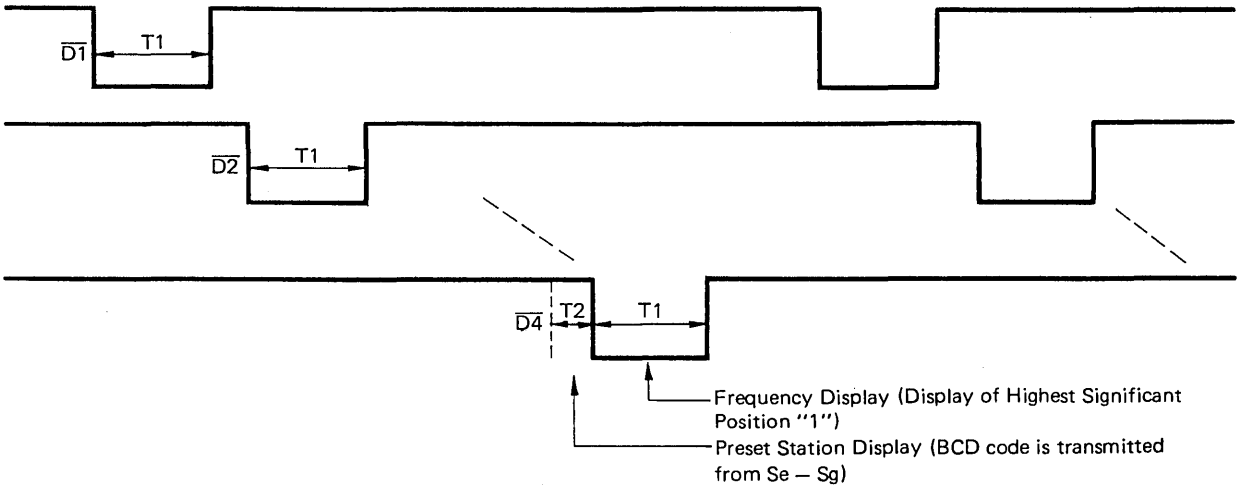


Fig. 3 Timing Chart

In this system, the most significant digit of display is to be connected to two segment lines Sb and Sc, and it displays "1" or blank

By using the remaining segment lines at the most significant digit timing, data for the preset station indicator are output. The preset data are output on the Se-Sg lines at the rising edge of $\overline{D4}$ (most significant digit signal) in BCD form. The μPD4035BC in Fig. 2 latches the BCD preset station data at the rising edge of $\overline{D4}$, and the μPB74LS42 decodes the BCD data and then drives the LEDs. Consequently preset station indicators are displayed in static.

* Preset station indicator shows which preset memory is selected.

Output Status Through Segment Terminals Sa – Sg
at Timing T1 and T2 of Digit Signal D4

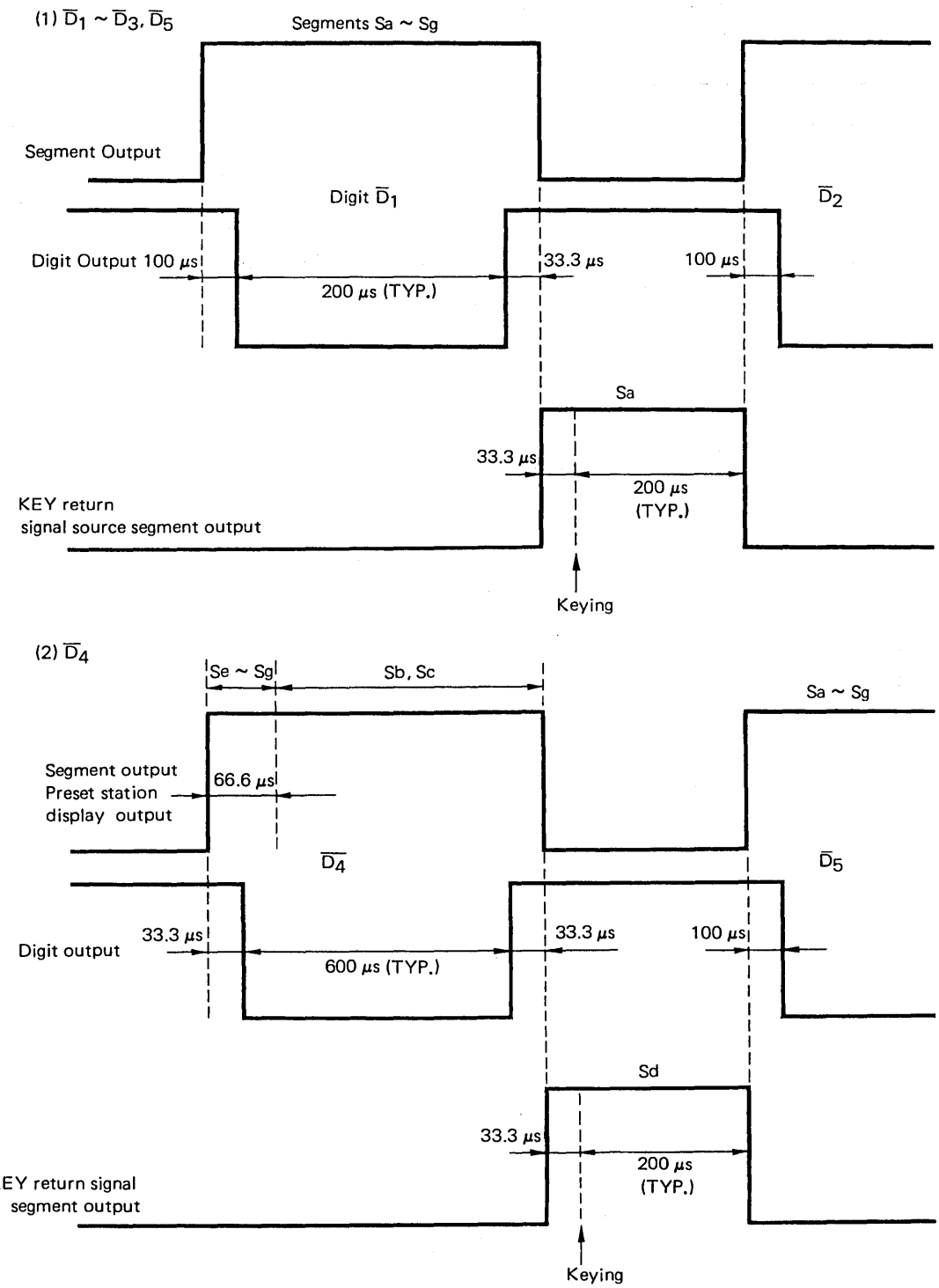
Timing \ Segment	Sa	Sb	Sc	Sd	Se	Sf	Sg
T1	Blank	Highest Significant Position "I" Display or Blank		Blank	Blank	Blank	Blank
T2	Blank	Blank	Blank	Blank	BCD Code Output		

Preset Station BCD Code Output

Sg	Sf	Se	Preset Station
0	0	1	P1 (M1 Key)
0	1	0	P2 (M2 Key)
0	1	1	P3 (M3 Key)
1	0	0	P4 (M4 Key)
1	0	1	P5 (M5 Key)
1	1	0	P6 (M6 Key)
1	1	1	P7 (M7 Key)

5. TIMING CHART

5-1 Display and Keying



5-2 MUTE Timing Chart

(1) KEY ON chattering preventing time

(2) MUTE first-out time

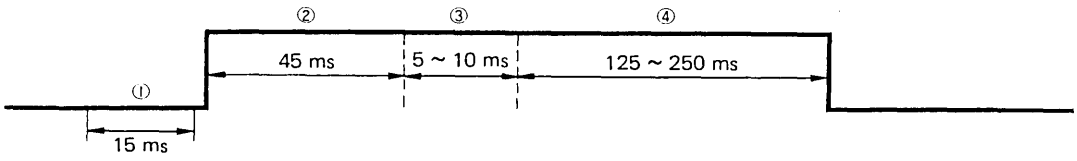
(3) Division ratio setting and display content updating time

(4) MUTE last-out time

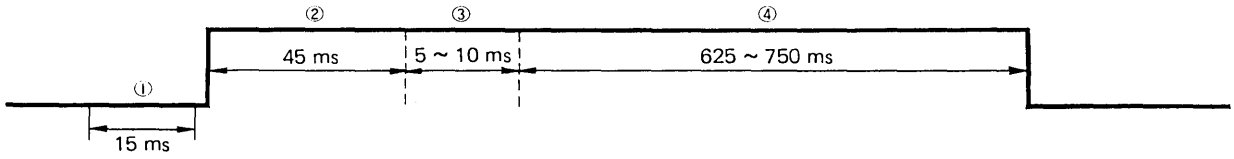
(5) Scan time

(6) PLL lock time

(1) MANUAL UP/DOWN

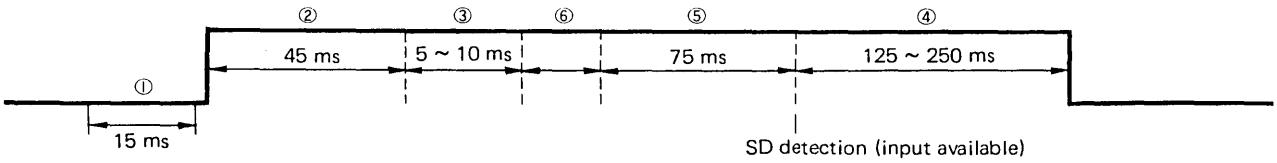


Band Edge (Max. Frequency → Min. Frequency, Min. Frequency → Max. Frequency)

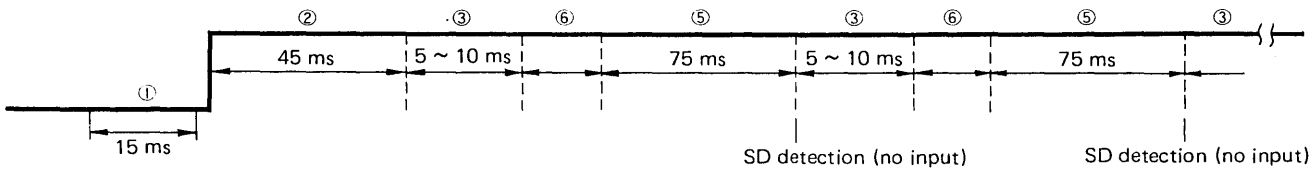


(2) AUTO UP/DOWN

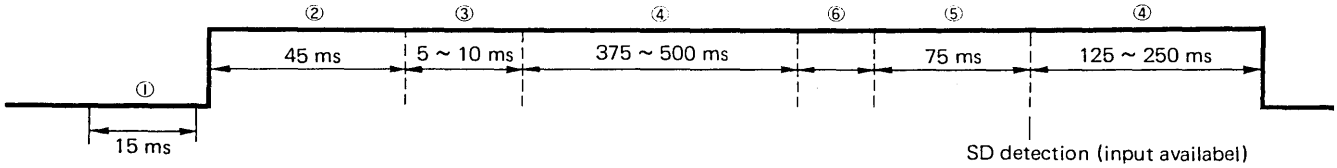
When SD signal is input



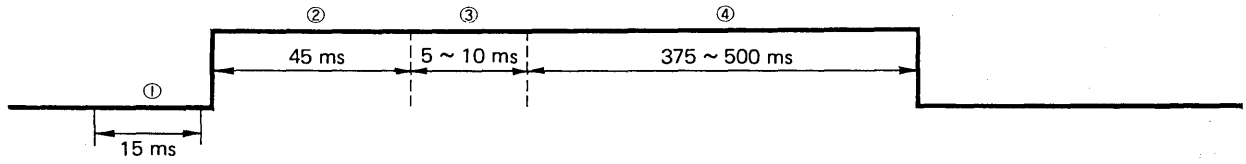
When no SD signal is input.



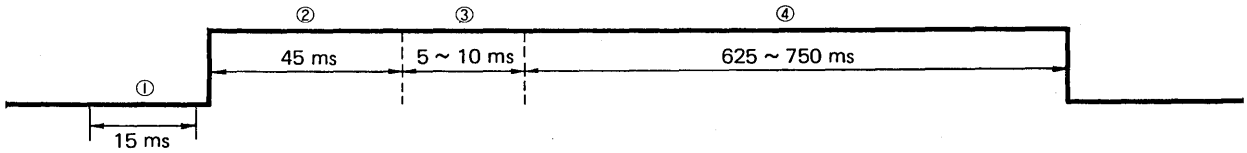
Band Edge (Max. Frequency → Min. Frequency, Min. Frequency → Max. Frequency)



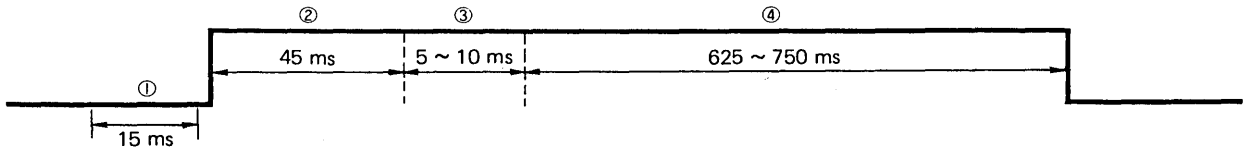
(3) PRESET MEMORY CALL



When the band is changed (MW → LW, LW → MW)



(4) When FM/MW/LW are switched and Power is ON (CE = Low → High)

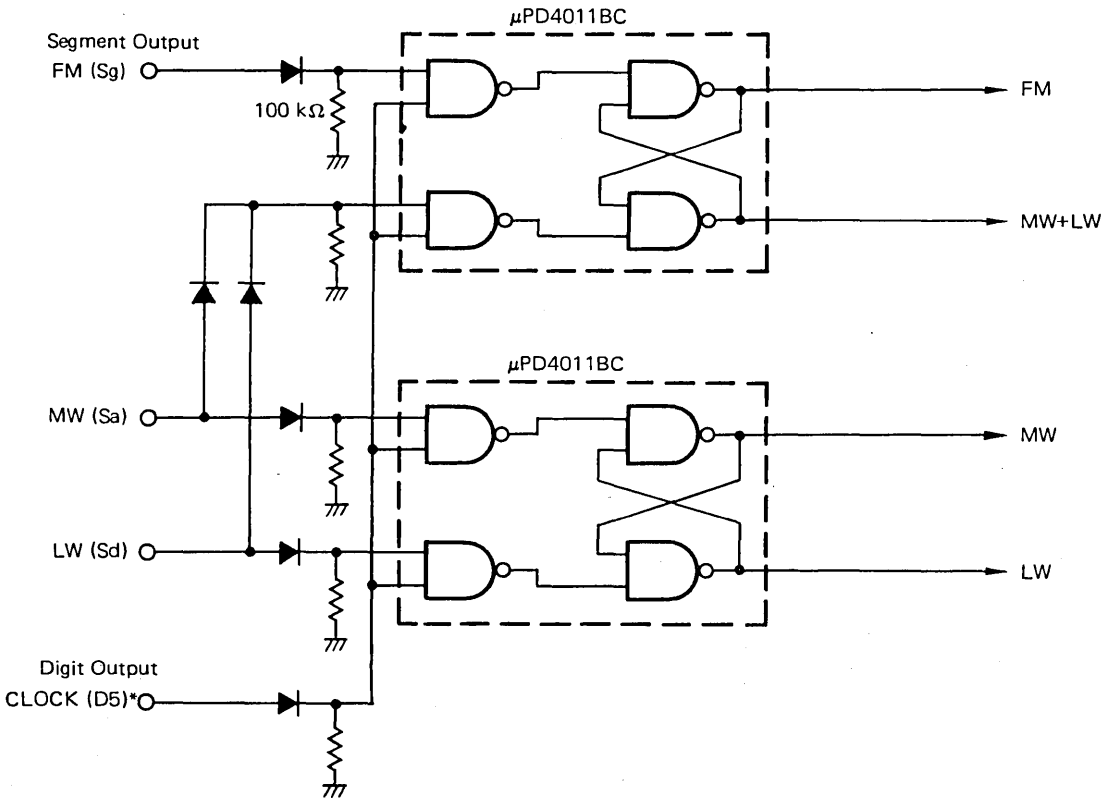


6. EXAMPLES OF FM/MW/LW POWER SUPPLY SWITCHING CIRCUIT

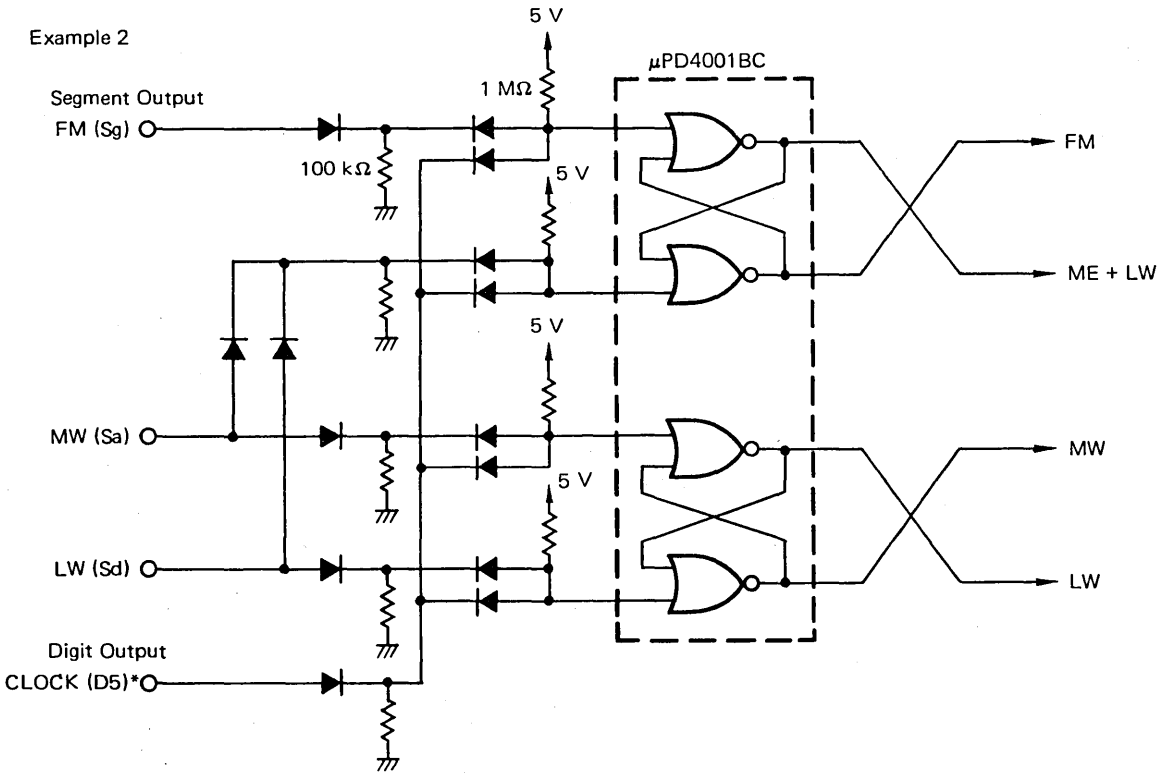
When Momentary Switch is used as a FM, MW, LW band selector switch, the tuner side power supply switching should be performed externally by the circuits shown below.

Input signal in the following diagram utilizes symbol of display ("FM", "MW", "LW") signals.

Example 1

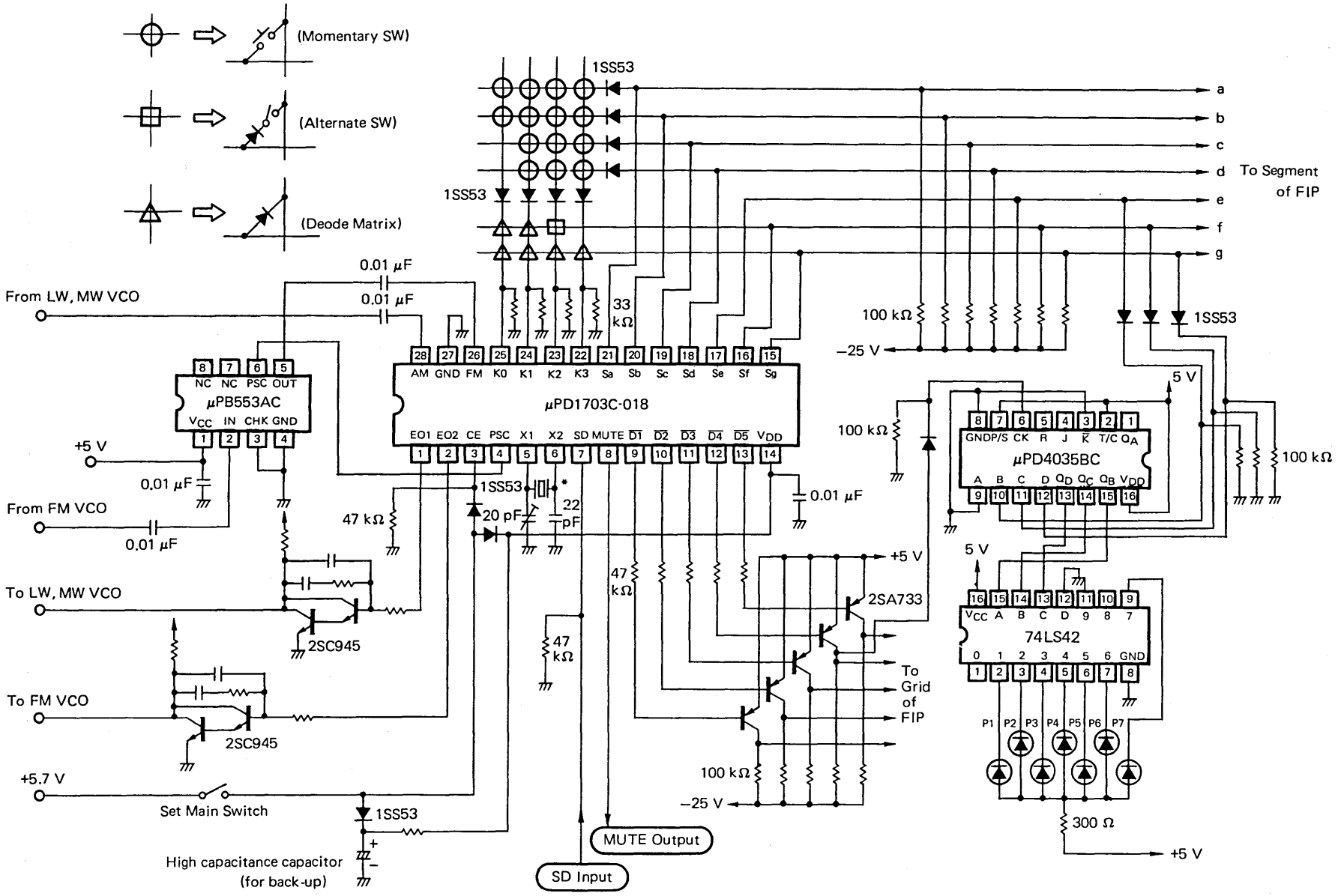


Example 2



*Note: CLOCK (D5) is the inverted signal of $\overline{D5}$ terminal from μPD1703–018. Output of digit buffer can be used as this signal.

APPLICATION EXAMPLE OF CIRCUIT DIAGRAM



*4.5 MHz X'tal (Toyo Tsuhinki: TQC-231A-8C)

The applied circuits and circuit constants listed in this material are not intended for mass production design with deviations and temperature characteristics of component parts considered. Further, this company will not assume any responsibllity as regards the patents on the circuits listed in this material.

MOS DIGITAL INTEGRATED CIRCUIT
μPD1703C-020

PLL TUNING RADIO CONTROLLER AND 24 HOUR DISPLAY FORMAT TIMEPIECE WITH TIMER CIRCUIT

The μPD1703C-020 is a CMOS LSI with 24 Hour display format timepiece built-in with timer circuit and PLL controller capable of receiving LW/MW/FM in U.S.A., Europe and Japan.

In combination with a prescaler μPB553AC, μPD1703C-020 can provide LW/MW/FM digital synthesizer tuner with timer clock.

Since the package of μPD1703C-020 is slim DIP (Dual In-Line Package), it greatly simplify Clock-Radio in design and assembly.

FEATURES

Clock part

- 24 hour display format clock. ([Hour], [Minute])
- Control timer with snooze timer.
- Duration of control timer and sleep timer is 64 minutes.
- Duration of snooze timer is 4 minutes.
- Program tuning (ie. To receive the programed station at the control time set in advance) is possible.

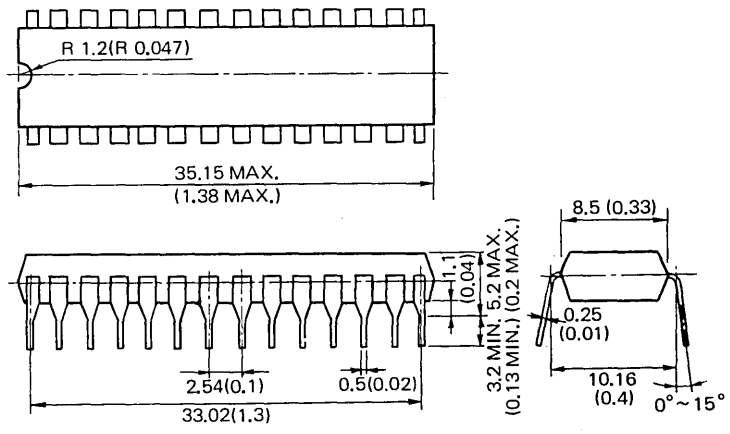
Radio part

- Auto up/down tuning.
- Manual up/down tuning.
- Last channel memories are available for each LW/MW/FM band.
- Six (6) preset station memories for MW/FM band.
- Built-in PLL swallow counter and controller.

Common features

- FIP (Fluorescent Indicator Panel) direct drive capability. (Segment only)
- 28 Pin slim plastic DIP.
- A single power supply of 5 V±10 %.

PACKAGE DIMENSIONS in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

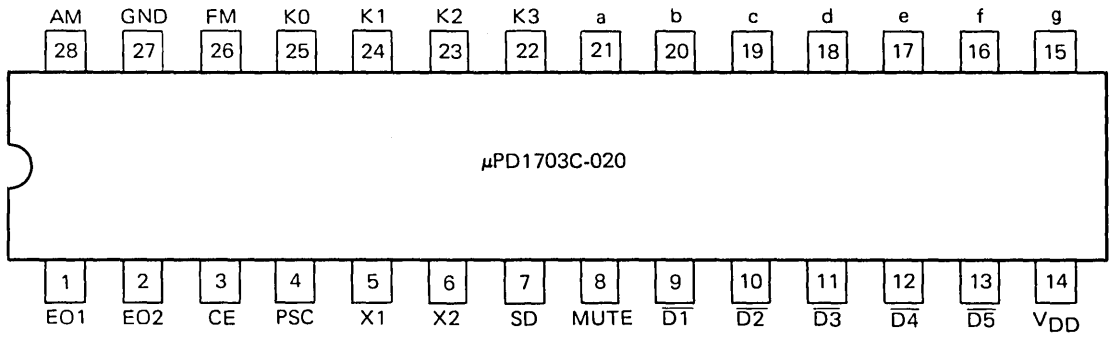
Supply Voltage	V_{DD}	−0.3 to +6.0	V
Input Voltage	V_I	−0.3 to V_{DD}	V
Output Voltage	V_O	−0.3 to V_{DD}	V
Output Breakdown Voltage *	V_{BDS}	−35	V
Output Current	I_{OH}	−10	mA
Storage Temperature	Tstg	−55 to +125	°C
Operating Temperature	Topt	−35 to +75	°C

* : Segment Output Terminals (P-ch open drain)

ELECTRICAL CHARACTERISTICS (Ta=−35 to +75 °C, V_{DD}=4.5 to 5.5 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
High Level Input Voltage	V_{IH1}	0.8 V_{DD}		V_{DD}	V	SD terminal
	V_{IH2}	0.7 V_{DD}		V_{DD}	V	CE terminal
	V_{IH3}	0.6 V_{DD}		V_{DD}	V	K0 to K3 terminals
Low Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	CE terminal
	V_{IL2}	0		0.2 V_{DD}	V	SD, K0 to K3 terminals
High Level Output Voltage	V_{OH1}	4.0			V	EO, D, MUTE: I_{OH}=−0.5 mA
	V_{OH2}	3.0			V	SEG: I_{OH}=−0.5 mA
	V_{OH3}	4.0			V	PSC: I_{OH}=−0.2 mA
Low Level Output Voltage	V_{OL1}			0.5	V	EO: I_{OL}=0.5 mA
	V_{OL2}			0.5	V	D, MUTE, PSC: I_{OL}=0.2 mA
High Level Input Current	I_{IH}	5.0	25	100	μA	K: V_I=V_{DD}=5.0 V
Frequency Response	fin1	0.5		2.5	MHz	AM: vi=1.0 Vp-p, DC cut sine wave
	fin2	0.5		8.8	MHz	FM: vi=0.8 Vp-p, DC cut square wave
Supply Voltage Rise Time	Tr			0.5	s	V_{DD}: 0→4.5 V
Supply Current	I_{DD}		500		μA	CE: Low Level
Output Off Leak Current	I_{OFF}			−5.0	μA	SEG: V_{DS}=−30 V

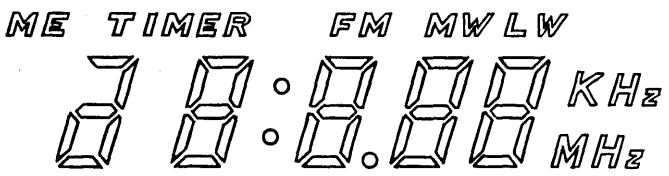
PIN CONNECTION (Top View)



EXPLANATION OF INPUT AND OUTPUT TERMINALS

EO1 EO2	These three-state outputs are used (via active filters) to supply analog voltages to the tuner varicap for controlling the local oscillators.
CE	This input is used to designate the stand-by mode to the chip. It is low to designate the stand-by mode. (display: off, PLL: disabled)
PSC	This output is used to control the divison ratio of the FM two-modulus prescaler (μPB553AC).
X1, X2	These inputs are for connection to a 4.5 MHz crystal.
SD	This input is used to control the automatic station searching operation. It is high to indicate the presence of a station.
MUTE	This output line is high to mute the radio in the case of station change, bnad change, and so on.
$\overline{D1}$ to $\overline{D5}$	These outputs are used as digit drivers for the display. (Active low)
V_{DD}	This is a 4.5 to 5.5 volt supply for the chip.
a to g	These outputs are used as segment drivers for the display. They are also uses as vertical drive for the control key and mode switch matrix. (P-ch open drain, Active high)
K0 to K3	These inputs are from seven by four matrix. Various functions are entered through the matrix.
FM	This is the FM band local oscillator input. The frequency is divided by 16/17 using a two-modulus prescaler (μPB553AC).
GND	System ground.
AM	This is the AM band local oscillator input.

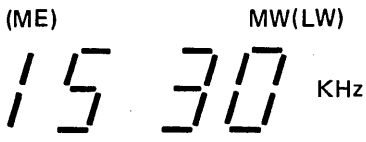
DISPLAY



DISPLAY FORMAT

FREQUENCY DISPLAY

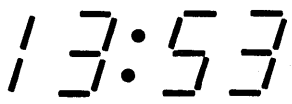
MW, LW



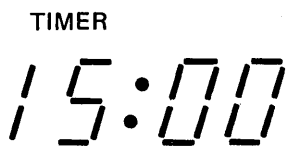
FM

CLOCK DISPLAY

STANDARD TIME



TIMER



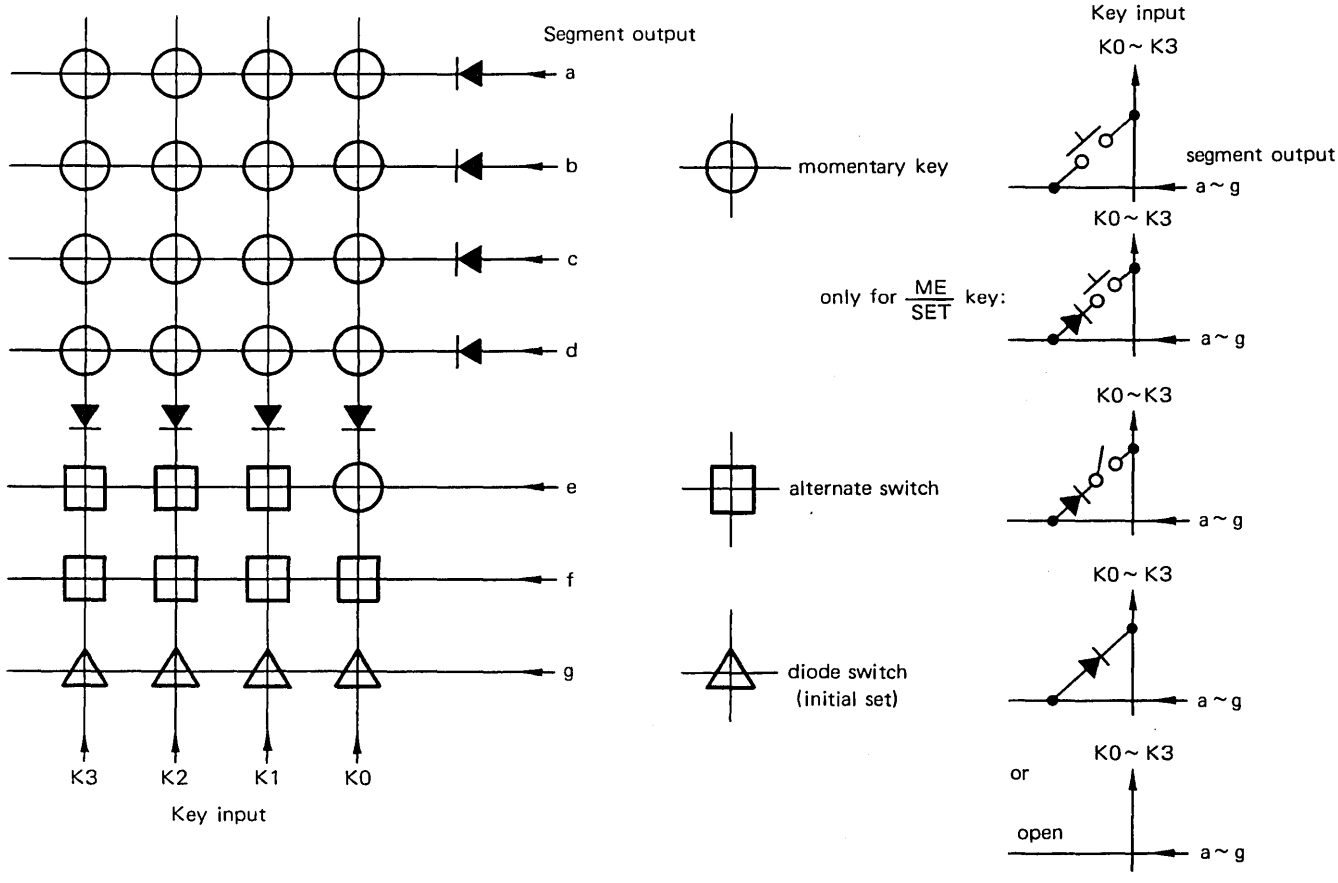
Note: ME flag is indicated the conditions enable to preset for the memory.
( ) marks are indicated the conditions provided to display functions, but be not lit for the lamps.

CONTROL KEY AND MODE SWITCH MATRIX

OUTPUT \ INPUT	K3	K2	K1	K0
a	$\frac{MUP}{HAD}$ ○	$\frac{MDW}{MAD}$ ○	M5 ○	M6 ○
b	M1 ○	M2 ○	M3 ○	M4 ○
c	ASKUP ○	ASKDW ○	SLI ○	CSS ○
d	TIM ○	FRQ ○	CNT ○	SNZ ○
e	CLOCK □	AM/FM □	LW/MW □	$\frac{ME}{SET}$ ○
f	DIMMER □	CNDI □	LOCK □	PRO □
g	IFO △	IF1 △	USA/JAP △	EUR/JAP △

○ momentary key
□ alternate switch
△ diode switch (initial set)

KEY MATRIX CONNECTIONS AND SWITCH TYPES



DESCRIPTION OF KEY MATRIX

Initialization Diode Matrix

Initialization Diode Matrix is available in 2 types as shown below. These matrixes are read in when power is initially supplied to V_{DD} (initialize) and when CE terminal is changed from low level to high level.

These initializations will be performed by shorting or opening the intersecting points on the matrix by Diode. (In the following table, "1" means shorting by Diode and "0" means opening.)

(1) Switches for specifying IF offset of FM

IF1, IF0

IF offset can be varied in 4 levels, as shown below, by 25 kHz step without changing indicated frequency:

IF1	IF0	U.S.A. Band	European Band	Japanese Band
0	0	10.700 MHz	10.700 MHz	10.700 MHz
0	1	10.725	10.725	10.675
1	0	10.650	10.650	10.750
1	1	10.675	10.675	10.725

Note: IF offset frequency of LW/MW is 450 kHz only.

(2) Switches for specifying band regions (U.S.A., Europe, Japan)

USA/JAP, EUR/JAP

USA/JAP	EUR/JAP	Area	Band		Channel Space
OFF	OFF	JAPAN	FM	76.1~89.9 MHz	100 kHz
			MW	531 ~1602 kHz	9 kHz
OFF	ON	EUROPE	FM	87.5~108.0 MHz	50 kHz
			MW	531~1602 kHz	9 kHz
			LW	155~290 kHz	9 kHz
ON	OFF	U.S.A.	FM	87.9~107.9 MHz	100 kHz
			MW	530~1620 kHz	10 kHz
ON	ON	Prohibited *			

* Both USA/JAP and EUR/JAP must not be ON (1). If both are ON, the band area will not be properly set.

○ Mode change over switch (Alternate Switch)

These switches are always changeable.

- Clock

The radio control function is stopped and radio control key input is rejected.

At the frequency display, clock is returned to the standard clock display.

ON ..... Only operated for clock function. PLL function is stopped and current consumption becomes low.

Muting signal (active high) is switched ON.

OFF ..... Radio control is enabled.

When the clock switch is changed over from ON to OFF, (at the radio control function restarted) the condition becomes to the frequency display at automatically and muting signal is switched OFF after approximately 500 ms.

- AM/FM, LW/MW

  Switches for sellecting the band (LW, MW, FM)

AM/FM	LW/MW	Band
OFF	OFF	FM
ON	OFF	MW
ON	ON	LW

  At transferred, the muting signal for approximately 500 ms. is outputed and at the same time frequency display is indicated.

- DIMER (Dimmer)

  By switching ON with dimmer switch, the brightness transfers to approximately 1/10.

  ON ..... Dark

  OFF ..... Bright

- CNDI (Control Disable)

  If control timer is not requried and the switch is turned ON, in spite of maching with the control timer setting value to standard clock value, no control output is delivered.

  ON ..... Control timer function is not operated.

  OFF ..... Normal operation.

- LOCK

  Without regard to that at the recording time and like the receiving channel have varied or the control output have cut by accident, in the event of this switch is being turned on, inputs of the channel exchange switch and the control switch for control output may be prohibited.

  ON ..... Each key MUP, MDW, M_1~M_6, ASKUP, ASKDW, SLI, CSS, and SNZ is rejected.

  OFF ..... Normal condition.

- PRO (Program)

  This is the interrupting receiving switch. When the switch is maintained "ON", maching with the control timer setting value to the standard clock time, the radio receiving channel can be changed to the channel preset to memory 1 (correspond to M_1) of the receiving band. (AM or FM)

  Also, at the radio is turned on by the control function, the channel corresponded to M_1 can be received automatically. (no relation to last channel)

  However, if LOCK switch is being turned on, these functions can not be operated even if PRO switch is turned on.

○ Momentary Switch

- MUP/HAD (Channel Manual Up/Hour Advance)

  MUP/HAD switch is used for manual up of the receiving channel and setting of "o'clock" on the standard clock and control timer.

  Manual up of the receiving channel is performed with MUP/HAD switch after changing to frequency display by means of FRQ switch is turned once on.

  At the same time, if MUP/HAD switch is one time switched on, the channel is advanced only one step. If MUP/HAD switch is kept "ON", the channel is automatically stepped up at intervals of approximately 45 ms. When the LOCK switch is being switched on, adjustment of channel is impossible. (during a station seek up, muting signal is outputed.)

  Adjustment of the "o'clock" on the standard clock is performed by MUP/HAD key, keeping ME/SET

key switch "ON" condition at the standard clock display. In this condition, when MUP/HAD switch is one time switched "ON", the time will be advanced at one hour. Also, when MUP/HAD switch is kept "ON", the time will be advanced at an interval of one hour per approximately 250 ms.

Before the setting of the control timer, one time the ALM Key is switched on as a result the control timer display is indicated, then the setting is performed with the same manner on "o'clock" adjustment of the standard clock, However, ME/SET Key is not required as "ON".

- MDW/HAD (Channel Manual Down/Minute Advance)

  The switch is used for the manual down of receiving channel and settings of "Minute" on the standard clock and control timer.

  Adjustment menas is the same manner as the switch MUP/HAD, however, in case the standard clock, every adjusted by MDW/MAD key, "second" is reset. (00 second)

- $M_1 \sim M_6$ (Memory 1 – Memory 6)

  These keys switches is used for call and write of the preset memory on each AM and FM six stations corresponded to $M_1 \sim M_6$ Key.

  When any key of $M_1 \sim M_6$ is switched on, the call of the preset memory can be performed to call the station preset in the memory corresponded to the specified key.

  Before the write of preset memory, at the frequency display condition, ME/SET switch is tunred on, and becomes the state of the write prepared. (ME lamp is lit.)

  Then, by menas of some one of these keys $M_1 \sim M_6$ is switched on, the write can be perfomred the channel indicated in the memory corresponded to the specified key.

  At the same time, ME lamp is not lit and it indicates to write in the memory.

- ASKUP (Auto Seak Up)

  ASKUP switch is used for automatic seek up for a station. (up direction)

  When the key switch is turned on, it becomes the frequency display is automatically and ups the channel at intervals of approximately 10 ms.

  In case a radiocasting catched, the channel up is stopped, as a result the radiocasting is received.

- ASKDW (Auto Seek Down)

  ASKDW switch is used for automatic seek down for a station. (down direction)

  Operating means is the same manner as the switch ASKUP.

- SLI (Sleep In)

  When the key is one time switched on, the sleep control timer (approx. 64-minute) is turned on. (If LOCK switch is being turned on, the sleep control timer is not operated.)

- CSS (Control timer Sleep timer Stop)

  No control output is delivered.

- SNZ (Snooze Timer)

  When control output is delivered by means of matching with the control timer setting value to the standard clock time, if the switch is turned on, no control output is delivered and after for four minutes the control output is delivered again.

  In this case, repeat of the snooze function is possible for many times.

  In this case, repeat of the snooze function is possible for many times.

  The control output, becomes off after for 60-minute from at switched on again.

- TIM (Standard Timer Display)

  The key is used for call the standard time display. In case the key is one time tunred on, it becomes the standard time display.

- FRQ (Frequency Display)

  The frequency display is called by onettime on of FRQ switch.

- CNT (Control Time Display)

  The control timer display is called by one time on of CNT switch.

DESCRIPTION OF DISPLAY

Display Connection Diagram

The display connection diagram is shown below. $\overline{D1}$–$\overline{D5}$ and a–g are corresponding to the digit terminals ($\overline{D1}$–$\overline{D5}$) and the segment terminals (a–g) of μPD1703C-020.

The segment terminals of μPD1703C-020 are capable of withstanding voltage upto –30 V (P-ch open drain output) and it is therefore possible to connect these terminals direct to FIP (Fluorescent Indicator Panel).

The digit lines should be connected to FIP via a one-stage buffers (PNP transistor), because those outputs are CMOS compremental-type and active-low.

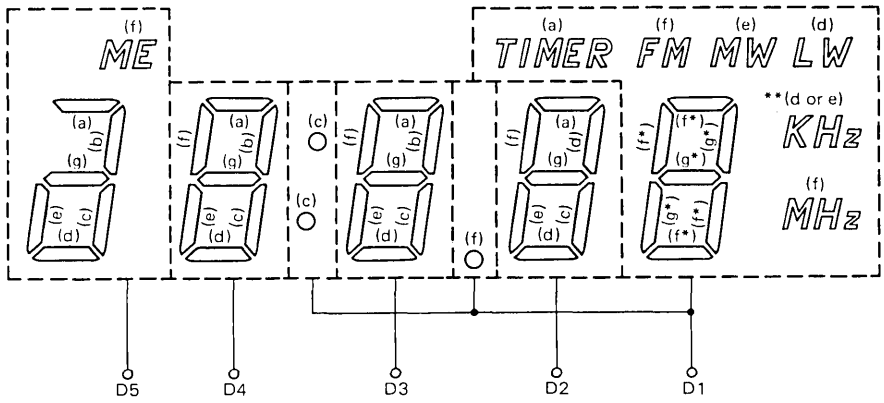


Fig. 1 Display Connecting Diagram

** Display of "kHz" is made by OR signal of Sa and Sd. If no LW is available, "kHz" can be displayed by Sa only. (See Fig. 2)

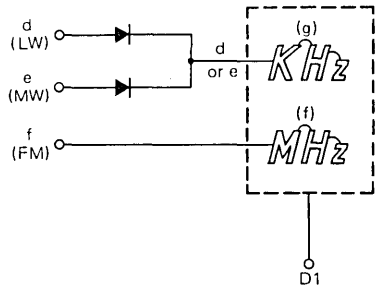


Fig. 2

* This is the digit for "50 kHz" in Europe FM. Note that this digit is controlled by following circuit; f, g and $\overline{g}$, and organizes the number "5" and "0". (See Fig. 3)
In MW and LW, nothing is displayed here. For FM in U.S.A. and Japan, don't connect the D5 or Sg line in this digit.

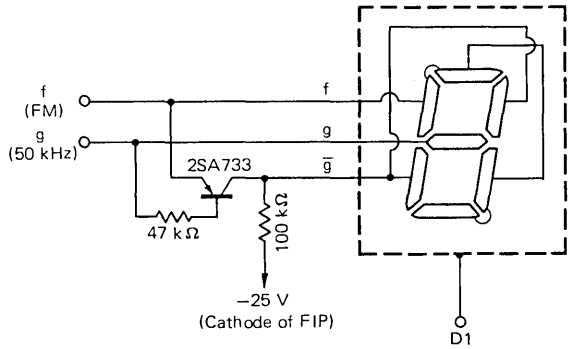
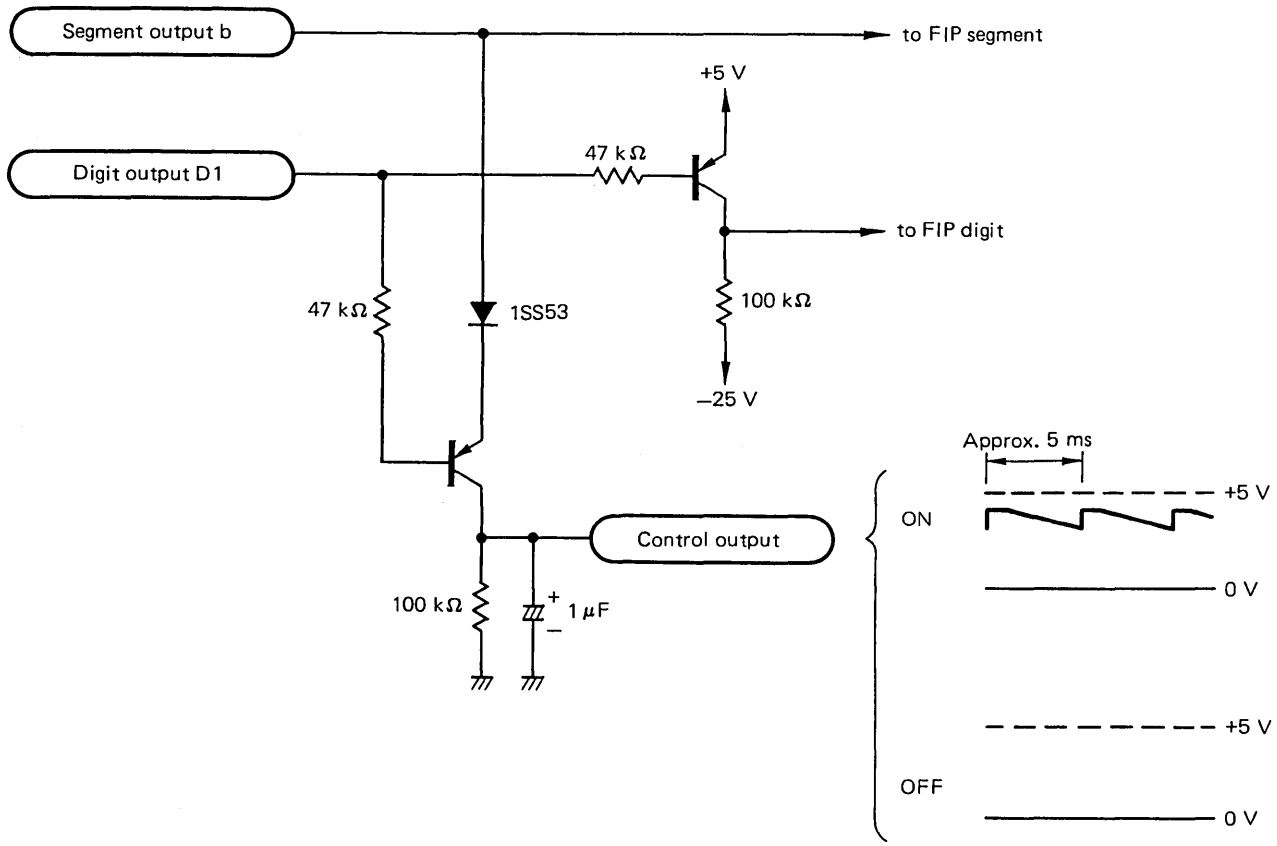
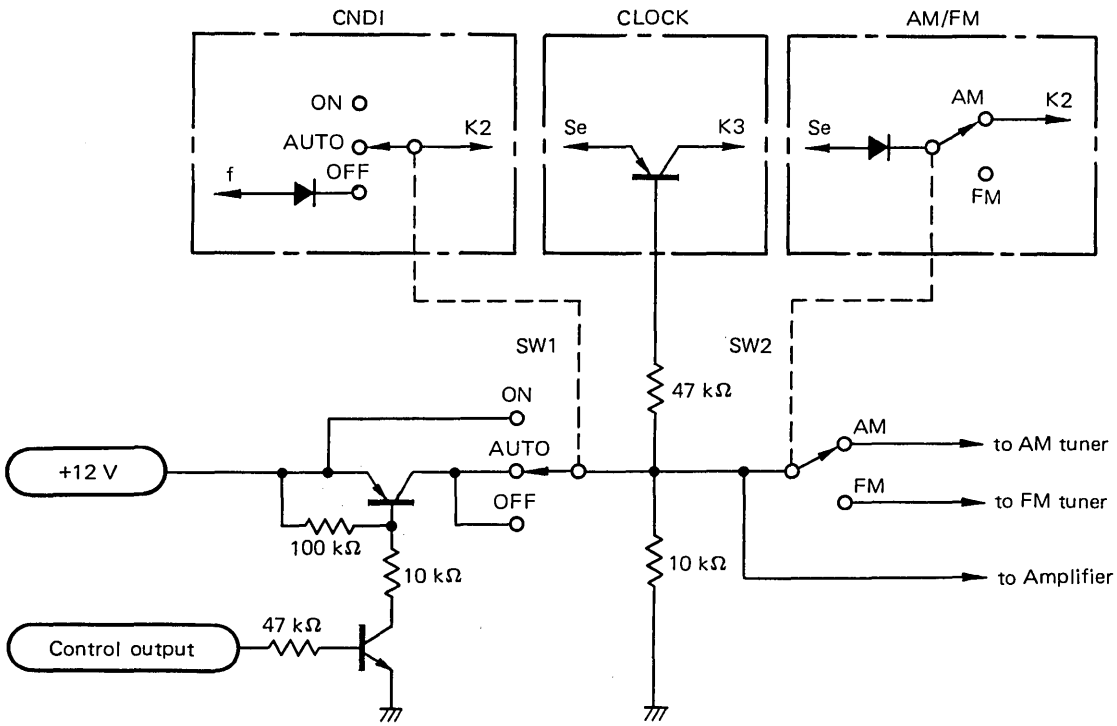


Fig. 3

CIRCUIT OF CONTROL OUTPUT

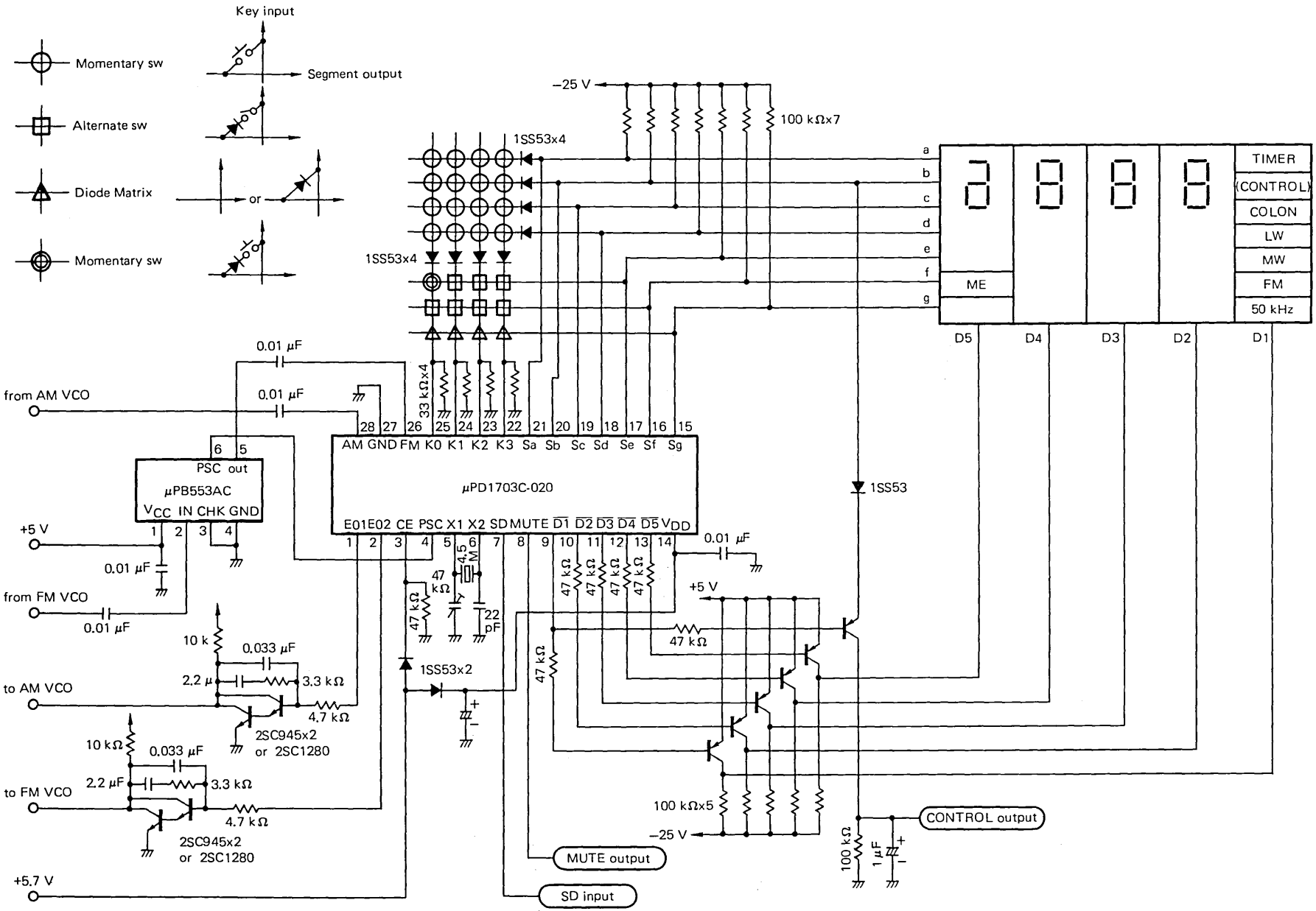


APPLICATION TO RADIO SET



SW1 : ON ····· EVER ON
AUTO ····· Radio set is controled by control or sleep timer function.
OFF ····· Radio set is controled only by sleep timer function.

APPLICATION CIRCUIT



MOS DIGITAL INTEGRATED CIRCUIT
μPD1704C-011

PLL FREQUENCY SYNTHESIZER AND CONTROLLER FOR AM/FM TUNER

The μPD1704C-011 is a single chip AM and FM band PLL frequency synthesizer plus controller for the U.S.A., Europe and Japan with a 24-Hour clock and three source-programmable timers. By using μPD1987C (remote control transmitter) and μPD1937C (remote control receiver) as peripherals, the μPD1704C-011 can be remote-controlled through infrared ray.

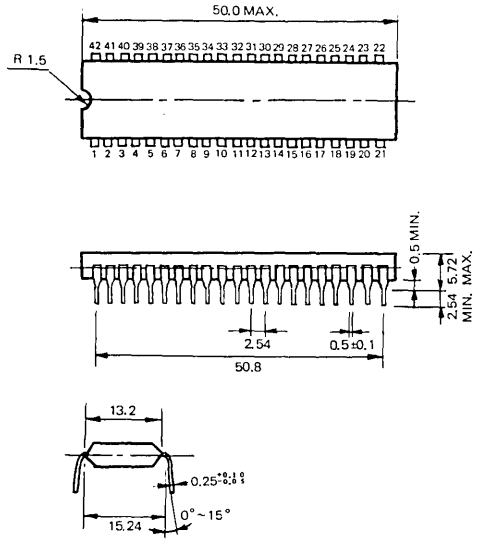
Since the μPD1704C-011 employing pulse-swallowing method in FM band tuning by using μPB553AC prescaler, the reference frequency of FM is as high as 25 kHz. Therefore, the μPD1704C-011 can constitute a multifunctional high performance AM/FM digital tuning system for home stereos and receivers.

The μPD1704C-011 is fablicated with advanced CMOS process and is packaged in 42-pin DIP.

FEATURES

- Single chip PLL + Controller
- Single power supply; +5 V±10 %
- Compatible with AM and FM band receivers for the U.S.A., Europe and Japan
- FM reference frequency is as high as 25 kHz (the pulse swallowing method is employed)
- Built-in 24 hour clock
- Built-in three sets of source programmable timers. (ONCE, EVERYDAY 1 and 2)
- Sixteen preset channel memories (8 for AM and 8 for FM)
- Two last channel memories; AM(1) + FM(1)
- Auto up/down seek tuning (Saw-tooth mode)
- Manual up/down tuning (Saw-tooth mode)
- Auto preset channel scanning (Holding 5 sec for each preset)
- Compatible with remote control system of μPD1986C and μPD1937C
- Source selector function (PHONO, TAPE, AUX)
- FM intermediate frequency compensating capability (4 ways by 25 kHz step)
- Wide variety of function selectability by diode matrix; FM ONLY, NO CLOCK etc.
- FIP (Fluorescent Indicator Panel) direct drive capability. (Segment lines only)
- 5-digit frequency display
- 10-key clock adjusting
- Low-power battery back up capability ($\leq 10\mu A$: only in No CLOCK mode).
- 42-pin DIP package

PACKAGE DIMENSIONS in millimeters



Note: Typical values are shown unless other use specified.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	V_{DD}	−0.3 to +6.0	V
Input Voltage	V_I	−0.3 to +V_{DD}	V
Output Voltage	V_O	−0.3 to +V_{DD}	V
Output Absorbing Current	I_O	10	mA
Operation Temperature	Topt	−35 to +75	°C
Storage Temperature	Tstg	−55 to +125	°C
Output Breakdown Voltage	V_{BDS}	−35 across Sa − Sg terminals (drain-source voltage)	V

RECOMMENDED OPERATION CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Power Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
Data (RAM) Retention Voltage	V_{RAM}	2.5		5.5	V	CE=0, CKSTP Instruction Executed
Oscillation Stop Voltage	V_{OSS}		3.2	3.8	V	
Output Breakdown Voltage	V_{BDS}			−30	V	I_{OH}=−5 μA Across Sa−Sg Terminals (Drain-Source Voltage)
Rise Time of Power Supply Voltage	Trise			500	ms	V_{DD}=0→4.5 V

ELECTRICAL CHARACTERISTICS (V_{DD}=4.5 to 5.5 V, Ta=−35 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
High-Level Input Voltage	V_{IH1}	0.8 V_{DD}		V_{DD}	V	SD, $\overline{RMC}$ Terminals
"	V_{IH2}	0.7 V_{DD}		V_{DD}	V	I/O Ports, CE Terminal (Note)
"	V_{IH3}	0.6 V_{DD}		V_{DD}	V	K_0 to K_3 Terminal
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	I/O Ports, CE Terminal
"	V_{IL2}	0		0.2 V_{DD}	V	K_0 to K_3, SD, $\overline{RMC}$ Terminals
High-Level Output Voltage	V_{OH1}	4.0			V	EO_1, EO_2 Terminals I_{OH}=−0.3 mA
"	V_{OH2}	4.0			V	$\overline{D_1}$ to $\overline{D_6}$, MUTE, I/O Ports I_{OH}=−0.2 mA
"	V_{OH3}	4.0			V	PSC Terminal I_{OH}=−0.1 mA
"	V_{OH4}	3.0			V	Sa to Sg Terminals. I_{OH}=−0.5 mA
Low-Level Output Voltage	V_{OL1}			0.5	V	EO_1, EO_2 Terminals, I/O Ports. I_{OL}=0.5 mA
"	V_{OL2}			0.5	V	$\overline{D_1}$ to $\overline{D_6}$, MUTE, PSC Terminals I_{OL}=0.2 mA
High-Level Input Current	$+I_{IH2}$	10	40	100	μA	K_0 to K_3 Terminals V_{IN}=V_{DD}=5.5 V
"	$+I_{IH2}$		300		μA	X_1 Terminal (during pull down) V_{IN}=V_{DD}=5.0 V
Low-Level Input Current	$-I_{IL1}$		300		μA	AM, FM Terminals (during pull up) V_{IN}=0,V_{DD} =5.0 V
Output Leakage Current	I_L		10^{-3}	1	μA	EO_1, EO_2 Terminals, Ta =25 °C
Response Frequency	f_{AM}	0.5		2.5	MHz	AM Terminal, Vin=1.0 Vp-p (Mim.), Dc Cut
"	f_{FM}		3		mA	FM Terminal, Vin=0.8 V_{p-p} (Mim.), Rectangular wave, Dc Cut
Operation Current	I_{DD1}		3		mA	Input/Output Currents from Input/Output Terminals Excluded
Data (RAM) Retention Current	I_{DD2}		10	10	μA	CE=0, CKSTP instruction executed, Ta=25 °C, V_{DD} =5.0 V
Clock Operation Current	I_{DD3}		600		μA	CE=0 V_{DD}=5.0 V

Note: I/O ports include AC OUT, FM/AM, selection terminals (AUX, TAPE, PHONO, TUNER) A to D, $\overline{DP}$, and $\overline{COLON}$.

FUNCTIONAL OUTLINE

Receiving frequency range, channel spacing, reference frequency, and intermediate frequency.

		Frequency Range	Channel Spacing	Reference Frequency	Intermediate Frequency
U.S.A.	AM	530–1620 kHz	10 kHz	10 kHz	450 kHz
	FM	87.9–107.9 MHz	200 kHz	25 kHz	10.650, 10.675, 10.700, 10.725 MHz
Europe	AM	522–1611 kHz	9 kHz	9 kHz	450 kHz
	FM	87.50–108.00 MHz	50 kHz	25 kHz	10.650, 10.675, 10.700, 10.725 MHz
Japan	AM	522–1611 kHz	9 kHz	9 kHz	450 kHz
	FM	76.1–89.9 MHz	100 kHz	25 kHz	10.675, 10.700, 10.725, 10.750 MHz

Channel Selection

(1) Auto tuning (saw-tooth wave mode)
Auto up-channel tuning
Auto down-channel tuning . . . . . Channel once received is held.

(2) Manual tuning (saw-tooth wave mode)
Manual up-channel tuning . . . . . Stepwise action through momentary switch. When held depressed for 0.5 second or more, fast action continued until the switch is released.
Manual down-channel tuning

(3) Preset scan . . . . . Preset channels from 1CH. to 8CH. are repeatedly scanned with holding for 5 seconds at each channel. To stop scanning at the currently received station, press the preset station key currently selected.

(4) Recall preset memory . . . . . 8 channels each for AM and FM through 8 button switches.

Timer

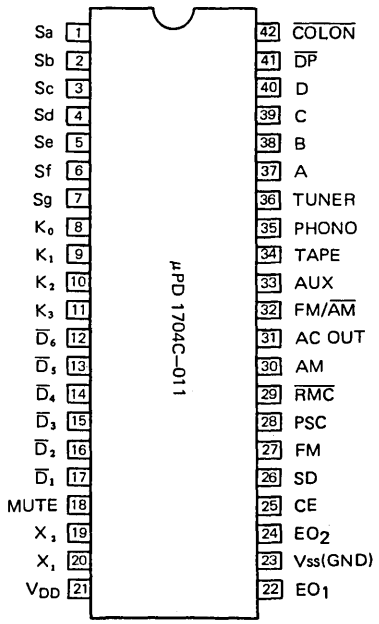
(1) EVERYDAY (for two systems) . . . . . By setting both ON and OFF time with a source, the specified source is switched ON at the ON-time and the whole system is switched OFF at the OFF-time. These action will be repeatedly performed everyday.

(2) ONCE (for one system) . . . . . By setting both ON and OFF-time with a source, the specified source is switched ON at the ON-time, and the whole system is switched OFF at the OFF-time.
In this case, the timer action is performed only once. And after the action, the ONCE-Timer data are cleared.

Remote Control

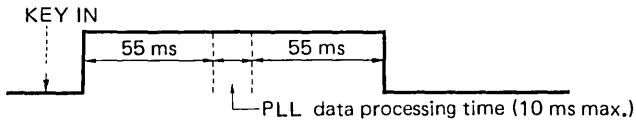
By attaching μPD1986C (transmitter) and μPD1937C (receiver), functions including power ON/OFF, AM/FM switching, preset channel call, and source selection can be remote controlled by infrared ray.

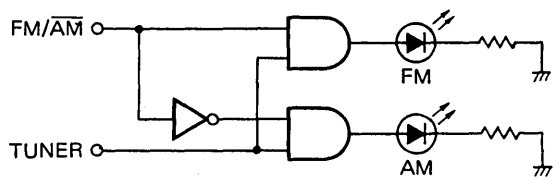
TERMINAL CONFIGURATION (Top View)



DESCRIPTION OF TERMINALS

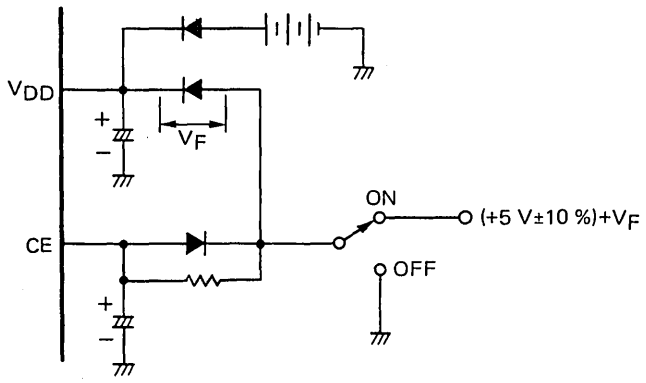
Terminal Number	Symbol	Terminal Name	Description
1–7	Sa–Sg	Segment Outputs	Terminals for display segment signals and for key return signal source; active high. (For details, see 1. KEY MATRIX CONFIGURATION.) These terminals are open-drain outputs and it is provided with dielectric strength of –30 V max. So it can be directly connected to segment terminals of FIP (fluorescent indicator panel) with pull-down resistances. (For the connections, see 3-1. Display Connection Diagram)
8–11	K_0–K_3	Key Return Signal Inputs	Input terminals for key return signals from externally connected key matrix. As the key return signal sources, segment terminals Sa-Sg and AND signal of TUNER and PHONO terminals are used. (See 1. KEY MATRIX CONFIGURATION.)
12–17	$\overline{D}_1$–$\overline{D}_6$	Digit Outputs	Display digit signal outputs; active low. To interface to a FIP (fluorescent indicator panel), single stage buffers using PNP transistors (2SA733 or equivalent) should be inserted between them. (For details, see 3–1. Display Connection Diagram.)

18	MUTE	mute	Muting signal output to cancel shock noises when PLL is momentarily unlocked; active high. This line goes high before 55 ms to PLL data (content of programmable counter) changes, and it goes low after 55 ms from the completion of the data change. Mute signal is issued while in either of the following cases. ○ AM/FM and selector switchings ○ MANUAL UP/DOWN ○ AUTO UP/DOWN ○ Preset memory call (including preset scan) ○ Switching from CLOCK set to RADIO.  The signal is continuously issued in either of the following cases. ○ OFF key is depressed. (OFF mode) ○ When the following mode is set through MODE SW; TIMER READ, TIMER WRITE, TIMER CANCEL ○ CE terminal is forced low.
19 20	X1 X2	X'tal	Terminal to which crystal oscillator is connected. The oscillation frequency of the crystal should be 4.5 MHz. (Type TQC-231A-8S manufactured by Tōyō Tsūshinki is recommended.)
21	V_{DD}	Power Supply	Terminal for power supply to the device. (5 V±10 %.) The voltage can be lowered to 2.5 V in data retention mode. (When device CLOCK is stopped, i,e, when NONCLOCK is specified through the diode matrix and CE=0). The rise time of V_{DD} should be 500 ms or less (for 0 → 4.5 V). If the rise time is excessively long, the initialization will not operate ploperly.
22 24	EO_1 EO_2	Error Out	Output terminals of charge pump in the phase detector of PLL section (3-state). Comparing the reference frequency with the oscillation frequency divided by the programmable divider, these terminals go high if the divided oscillation frequency is higher than the reference frequency. And go low if it is lower than the reference frequency. If they are the same, these outputs becomes high-impedance. Since EO1 and EO2 output the same signal at the same time, either of them can be connected to the LPF (low pass filter) of either AM or FM.
23	GND	Ground	Terminal to be connected to system ground.
25	CE	Chip Enable	Terminal for input selection signal to device. The terminal voltage has to be high level to operate the device normally and low level to leave the device idle. (1) When NONCLOCK is set through the initial setting diode matrix. CE = High ..... normal operation. CE = Low ..... display OFF, PLL operation stopped, internal clock generator stopped; current consumption 10 μA or less, V_{DD} = 5 V. (2) When NONCLOCK is not set through the initial setting diode matrix. CE = High ..... normal operation CE = Low ..... display OFF, PLL operation stopped; current consumption 500 μA typical, V_{DD} = 5 V.

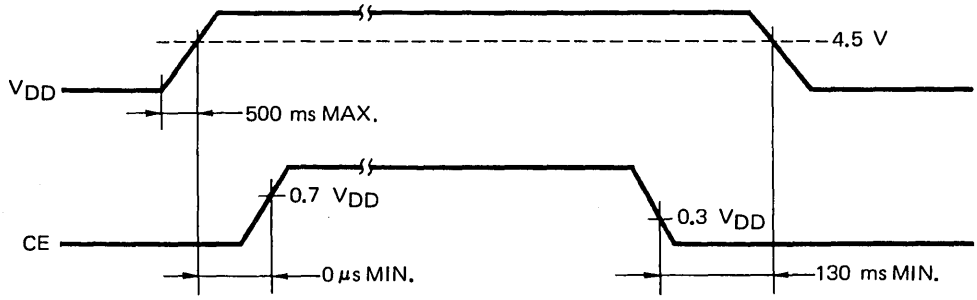
			High level or low level for 134 μs or shorter cannot be accepted. When NONCLOCK is selected through the initial setting switch, CE terminal should be forced to high level after the rise up of V_{DD}, and forced to low level 200 ms before V_{DD} falls. (See Note 1.)
26	SD	Station Detector	Input terminal of station detection for auto tuning (AUTO UP/DOWN). The auto tuning is stopped on receiving high level. To avoid missing the station, this input should be forced to high level within 50 ms after PLL is locked.
27	FM	FM Local Oscillator Signal Inputs	Input terminal of FM programmable counter. This terminal is normally connected to the output of the two-modulus prescaler μPB553AC. Since an ac amplifier is employed inside, the input signal should be fed through a dc-cut capacitor.
28	PSC	Pulse Swallow Control	Terminal for output signal to switch frequency dividing ratio of prescaler when pulse swallowing method is used in frequency dividing (i.e. for FM signal reception). Connect to PSC terminal of special prescaler μPB553AC. The frequency dividing ratios of μPB553AC are 1/16 and 1/17.
29	$\overline{RCM}$	Remote Control Inputs	Input terminal of remote control signal. Connect to CHU OUT terminal of receiving remote control IC μPD1937C. The remote control action is discriminated by the number or input pulses to this terminal. (For details, see 2–4. Transistor Switch)
30	AM	AM Local Oscillator Signal Inputs	Input terminal of AM programmable counter. It accepts the output signal (VCO) from AM local oscillator. Since an ac amplifier is employed inside, the input signal should be fed through a dc-cut capacitor.
31	ACOUT	AC Outlet Control	Terminal for AC service outlet control. This terminal is used to control the cut-out relay for the main power supply of the receiver set. This goes high level whenever either one of the source selector terminals (TUNER, PHONO, TAPE, and AUX) is to be turned on. When the OFF key is pressed, it becomes low level. Since this terminal becomes high impedance when the CE terminal is shifted to low level under the NONCLOCK conditions, a pull-down resistor should be used if NONCLOCK specification is required. (See Note 3.)
32	FM/$\overline{AM}$	FM/AM Power Supply Control	Terminal for switching power supply to tuner's FM or AM section. High level output is issued to operate FM and low level output to operate AM. This is also used in conjunction with the TUNER terminal to issue an ACKNOWLEDGE signal of AM and FM source selection in TIMER READ and TIMER WRITE modes. The schematic of the ACKNOWLEDGE signal generator is as follows. 

<table>
<tr><td></td><td></td><td></td><td>When FM or AM key is depressed in TIMER WRITE mode with the circuit shown above, the LED corresponding to the specified band will be turned on for 50 ms.
In TIMER READ mode, the LED, corresponding to the band set in WRITE mode, will be turned on for 5 seconds.</td></tr>
<tr><td>33
34
35
36</td><td>AUX
TAPE
PHONO
TUNER</td><td>Source Selector Outputs</td><td>Source selector outputs for TUNER, PHONO, TAPE, and AUX. TUNER terminal goes to high level when FM, AM, or preset key is depressed, and PHONO, TAPE, and AUX terminals goes to high level when PHONO, TAPE, and AUX keys are depressed, respectively.
When OFF key is depressed, all terminals are forced to low level. (See Note 3.)</td></tr>
<tr><td>37–40</td><td>A
B
C
D</td><td>Preset Station Indicator Outputs</td><td>Output terminals of BCD signals to indicate the preset channel memorys. The output combinations for preset stations are shown in the table below.
<table><tr><td>PRESET STATION</td><td>D</td><td>C</td><td>B</td><td>A</td></tr><tr><td>NON PRESET</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>P1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr><tr><td>P2</td><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>P3</td><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>P4</td><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>P5</td><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>P6</td><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>P7</td><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>P8</td><td>1</td><td>0</td><td>0</td><td>0</td></tr></table>1: High level Output
0: Low Level Output
By connecting μPB74LS42 (BCD-to-decimal decoder) to these terminals, the dot pattern display of preset station can be made with LEDs. (See Note 3.)</td></tr>
<tr><td>41</td><td>$\overline{DP}$</td><td>Decimal Point</td><td>Terminal to output a decimal point indication signal to the display for FM frequency; active low.
$\overline{DP}$ as well as $\overline{COLON}$ terminals cannot be directly connected to fluorescent indicator panel. Insert a buffer for the purpose. (See Note 3.)</td></tr>
<tr><td>42</td><td>$\overline{COLON}$</td><td>COLON</td><td>Terminal to output a colon indication signal in CLOCK display mode; active low. (See the discription of DP terminal above.)</td></tr>
</table>

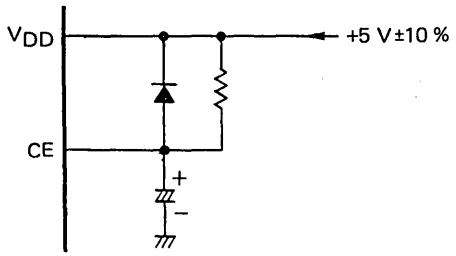
(Note 1) When no clock function is necessary, turn the NONCLOCK switch ON. And if, in this mode of operation, low-power-data-retention is required while radio is off, do not use OFF key, which will be described later, to turn system power supply off, but use CE terminal. The example circuit is shown below.



The value of CR connected to CE terminal should be set so that the following condition is satisfied.



(Note 2) If NONCLOCK is not specified, CE terminal should be connected to V_{DD} as shown below.



(Note 3) AC OUT, A, B, C, D, AUX, TAPE, PHONO, TUNER, and DP terminals are shifted to low level or high impedance status dependent on the internal conditions when CE terminal is changed to low level under the NONCLOCK (refer to 2. Description of Key Matrix) conditions.

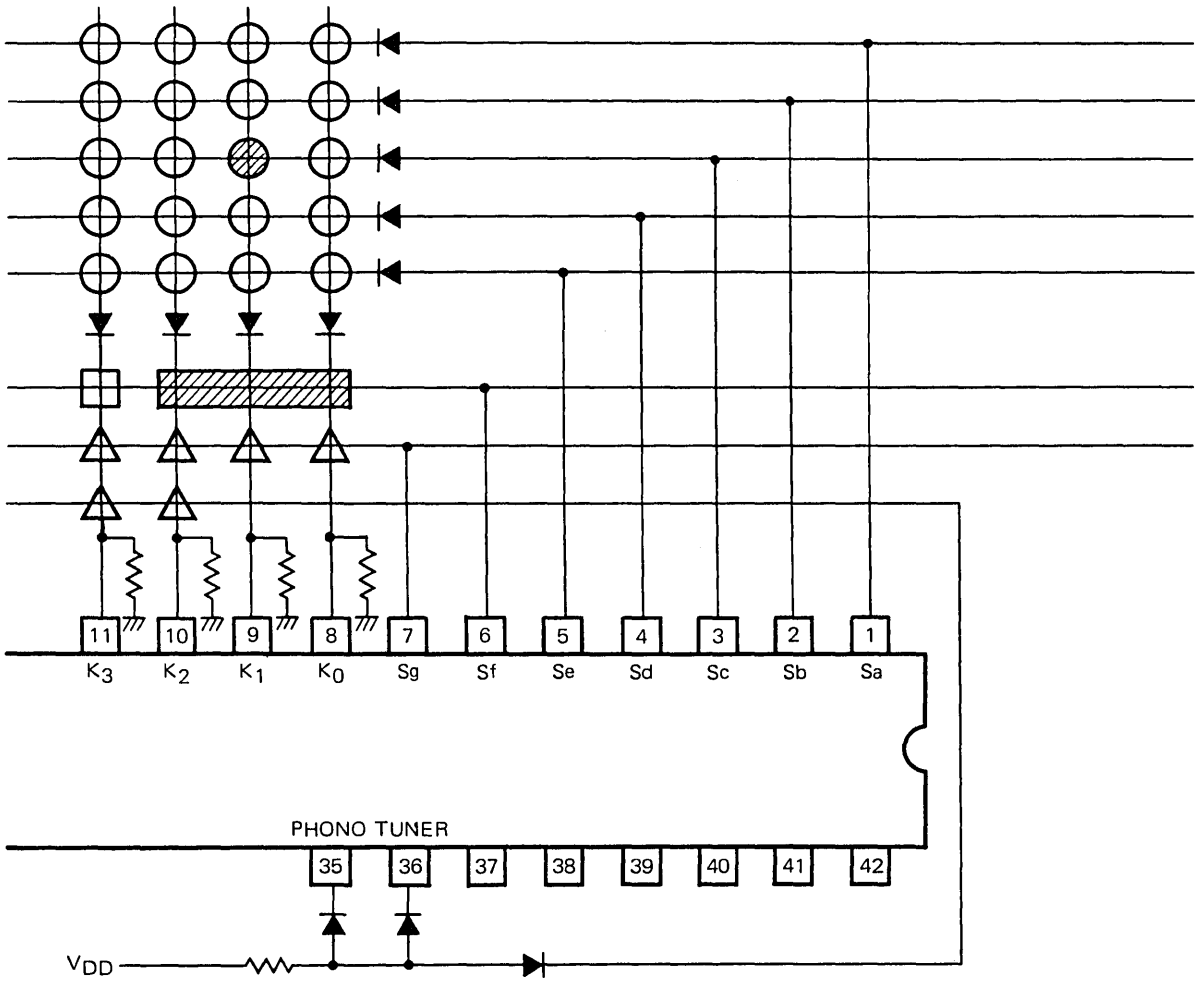
1. KEY MATRIX CONFIGURATION

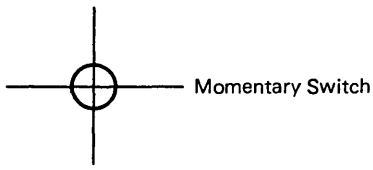
1-1. Key Matrix Configuration

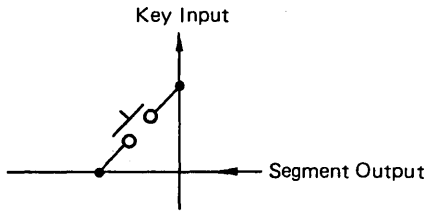
	K_3(11)	K_2(10)	K_1(9)	K_0(8)	Type of Key
Sa(1)	0 (AM)	1 EVERYDAY1 ON	2 EVERYDAY1 OFF	3 EVERYDAY2 ON	Momentary (Normally OFF) * Transistor Switch
Sb(2)	4 EVERYDAY2 OFF	5 ONCE ON	6 ONCE OFF	7	
Sc(3)	8	9 (FM)	REMCON*	OFF	
Sd(4)	CLK CALL	CH SCAN	DOWN	UP	
Se(5)	MEMORY	PHONO	TAPE	AUX	
Sf(6)	AUTO/MANUAL	MODSW2 (note)	MODSW1 (note)	MODSW0 (note)	MODSW . . . Rotary Switch AUTO /MANUAL ...: Alternate Switch
Sg(7)	IF0	IF1	BAND1	BAND0	Initially Set Diode Matrix
TUNER & PHONO	NONCLOCK	FM ONLY			

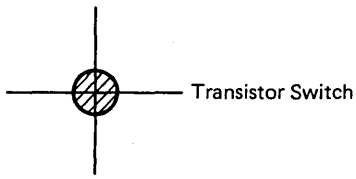
(Note) Rotary switch to be used as mode switch should be of shorting type.

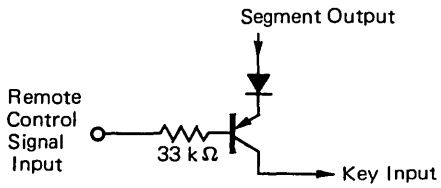
1-2. Connection of Keys and Switch Types on Key Matrix

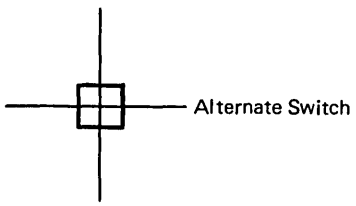


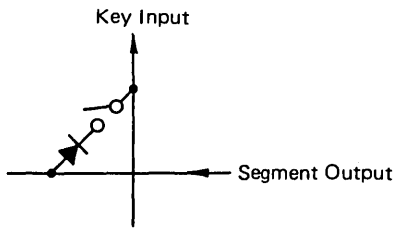

Momentary Switch

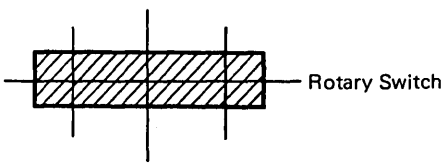

Key Input
Segment Output

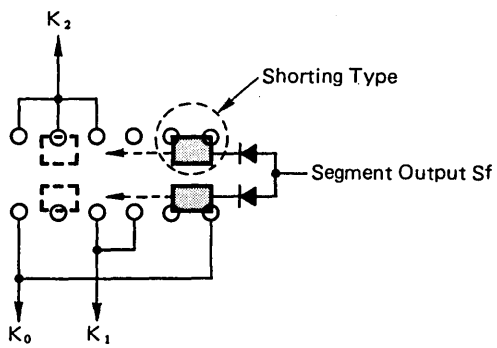

Transistor Switch

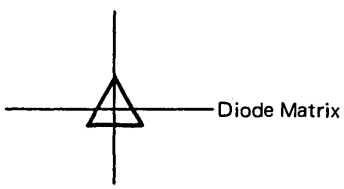

Segment Output
Remote
Control
Signal
Input
33 kΩ
Key Input

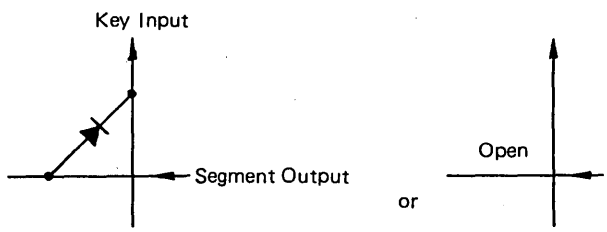

Alternate Switch


Key Input
Segment Output


Rotary Switch


K₂
Shorting Type
Segment Output Sf
K₀
K₁


Diode Matrix


Key Input
Segment Output
or
Open

2. DESCRIPTION OF KEY MATRIX

2-1. Initial Setting Diode Matrix

There are four types of initial setting matrices as described below. They are read in when V_{DD} is first fed with power (initializing) or when CE terminal is forced to high level from low level.

(1) Switches for setting IF offset value of FM.
IF1, IF0

(2) Switches to specify the BAND range for the target area. (American, European, or Japanese)
BAND1, BAND0

(3) Switch to kill the clock function.
NONCLOCK

(4) Switch to meet the FM single receiver.
FM ONLY

These settings are done by shorting with a diode or by opening the crosspoint on key matrix. (In the following table, ON means short-circuiting with a diode and OFF means opening.)

<table>
<tr><th>Symbol</th><th>Functional Description</th></tr>
<tr><td>IF1
IF0</td><td>Switches to set IF offset value of FM.
Intermediate frequency can be set in for ways, 25 kHz apart from each other, without changing the frequency displayed.
<table>
<tr><th>IF1</th><th>IF0</th><th>American band</th><th>European band</th><th>Japanese band</th></tr>
<tr><td>OFF</td><td>OFF</td><td>10.700 MHz</td><td>10.700 MHz</td><td>10.700 MHz</td></tr>
<tr><td>OFF</td><td>ON</td><td>10.725</td><td>10.725</td><td>10.675</td></tr>
<tr><td>ON</td><td>OFF</td><td>10.650</td><td>10.650</td><td>10.750</td></tr>
<tr><td>ON</td><td>ON</td><td>10.675</td><td>10.675</td><td>10.725</td></tr>
</table></td></tr>
<tr><td>BAND1
BAND0</td><td>Switches to specify the BAND range for the target area.
Either American, European, or Japanese band can be selected.
<table>
<tr><th>BAND1</th><th>BAND0</th><th>Found Area</th></tr>
<tr><td>OFF</td><td>OFF</td><td>American band</td></tr>
<tr><td>OFF</td><td>ON</td><td>Japanese band</td></tr>
<tr><td>ON</td><td>OFF</td><td>European band</td></tr>
<tr><td>ON</td><td>ON</td><td>Prohibited *</td></tr>
</table>
* Do not turn both BAND1 and BAND0 ON. If both are turned ON, receiving band cannot be set duly.</td></tr>
<tr><td>NONCLOCK</td><td>Switch to kill the clock function.
When no clock function is required, make this switch ON.
Then, data retantion is capable with a low current consumption (10 μA or less).
(Refer to Notes 1 and 2 of Terminal Descriptions.)
ON ..... With Clock Function
OFF ..... With Clock Function</td></tr>
<tr><td>FM ONLY</td><td>Switch to set receiving band to FM only.
When this switch is ON, AM band is not received even if '0(AM)' key is pressed. Then band switching keys 'FM' and 'AM' can be accepted only as '9' and '0' for time adjustment.
ON ..... FM only
OFF ..... FM and AM</td></tr>
</table>

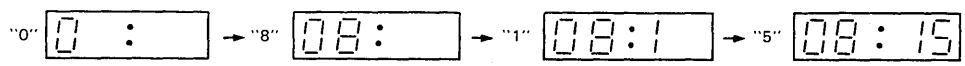
2-2. Alternate Switches

There are two kinds of alternate switches. They can be switched any time.

(1) Switch to select auto tuning or manual tuning.
AUTO/MANUAL

(2) Programmable mode switches to specify operation modes; CLOCK SET, TIMER WRITE, TIMER CANCEL, etc.
MODSW2, MODSW1, MODSW0

<table>
<tr><th>Symbol</th><th>Description of Function</th></tr>
<tr><td>AUTO/
MANUAL</td><td>Switch to select auto tuning or manual tuning.
ON . . . . . Auto Tuning
OFF . . . . . Manual Tuning
Auto or manual tuning starts when the momentary switch of UP or Down is pressed after the setting of this switch.
In the auto tuning operation, the frequency is scanned step by step after confirming that the PLL system is locked. Therefore, in the long lock-up time PLL system, the scanning speed will be slower than the short one. And if the PLL feedback loop is malfunctioned and the PLL is never locked, the scanning will not be started or be stopped.</td></tr>
<tr><td>MODSW2
MODSW1
MODSW0</td><td>Programmable mode switches to specify modes such as CLOCK SET, TIMER WRITE, TIMER CANCEL.
Use shorting-type rotary switch with two circuits and six positions for these switches. (For connections, see 1–2 "Connection of Keys and Switch Types for Key Matrix".)

<table>
<tr><th>MODSW2</th><th>MODSW1</th><th>MODSW0</th><th>Programmable Mode</th></tr>
<tr><td>1</td><td>0</td><td>1</td><td>CLOCK SET</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>RADIO</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>TIMER OPERATION</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>TIMER READ</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>TIMER WRITE</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>TIMER CANCEL</td></tr>
</table>
(Note) 1 and 0 in the table means ON (short) and OFF (open) respectively. Since the mode switch code is modified gray code, the sequence of the codes cannot be changed to others than the above.
1. CLOCK SET mode
Mode to set present time.
μPD1704C-011 is provided with a 24-hour clock system (0:00–23:59). The time can be set by the following procedure.
① Set time in 4-digit input using ten-key 0–9.
(Ex. Setting to 8:15 A.M.)


(Note) If some wrong key was pressed, finish the 4-digit keying and then start keying again from the first digit.

② Turn the programmable mode switch to RADIO coincidentally to time signal. The clock function starts to operate at the moment of switching over to RADIO.
(Note 1) If clock setting is performed while listening to the radio, radio broadcast frequency is indicated when the mode switch is returned to RADIO.
If the similar process is followed in PHONO, TAPE, or AUX mode, the time is indicated, but zero (0) in the most significant digit will be suppressed to blank as shown below.</td></tr>
</table>

2) At the time when V_{DD} (5 V ±10 %) is supplied to the device, "E" is indicated.

3) When the mode switch is in the position of CLOCK SET mode, the internal clock stops functioning. The clock starts functioning when the mode switch is turned to another, and the value of second is set to "0" internally.

2. RADIO mode

In this mode, the tuner functions such as write and call of AM/FM preset memory, UP/DOWN tuning in AUTO/MANUAL, and preset memory scan etc.) and source selection (PHONO, TAPE, or AUX) can be performed.

3. TIMER OPERATION mode

Mode for executing instructions of time and source (AM, FM, PHONO, TAPE, or AUX) specified in TIMER WRITE mode.

Each of three timer systems, EVERYDAY1, EVERYDAY2, and ONCE, is respectively executed (ON or OFF) at the programmed time. Once programmed in ON/OFF-time and source, EVERYDAY1 and EVERYDAY2, repeat the ON and OFF operation to the programmed source everyday at the programmed time, while ONCE is automatically erased after the execution of ON and OFF operation and it will not be executed next day.

MODSW2
MODSW1
MODSW0

Among these three systems, the priority sequence ONCE, EVERYDAY2, EVERYDAY1 is established. (For details, see 4 Description of Programmable Timer Performance)

When timer is executed, one of the following terminals is to be activated corresponding to the programmed source.

Programmed Source	Terminals to be activated
FM	FM/$\overline{AM}$=High, TUNER=High, AC OUT=High
AM	FM/$\overline{AM}$=Low, TUNER=High, AC OUT=High
PHONO	PHONO=High, AC OUT=High
TAPE	TAPE=High, AC OUT=High
AUX	AUX=High, AC OUT=High

If the timer of either one of the systems is ON, all key and remote controlled inputs in this mode cannot be accepted because of protection against wrong operations. Such a manual input operation should be done after switching to RADIO mode if desired.

4. TIMER READ mode

Mode to confirm ON/OFF time and source programmed in TIMER WRITE mode. The procedure is as follows;

① Set the programmable mode switch to TIMER READ mode. Then source selector terminals (TUNER, PHONO, TAPE, and AUX) and AC OUT terminal are forced to low level, and the present time is indicated.

② Press ON key of either of EVERYDAY1, EVERYDAY2, or ONCE, Programmed ON-time, source selector terminal and the preset station are indicated for about 5 seconds. After that, the present time indication is recovered.

③ Press OFF key of EVERYDAY1, EVERYDAY2, or ONCE. Programmed OFF time is indicated for about 5 seconds. After that, the present time indication is recovered.

(Note) If ON or OFF time is not programmed, only colon (:) is indicated for about 5 seconds.

5. TIMER WRITE mode

Mode for programming ON and OFF times and source to be operated. Note that OFF-time must be set whenever the ON-time is to be set. If OFF-time is not set, timer-ON action will never be performed and the ON-time which was set alone will be erased. This function is provided to avoid accidents caused by the timer which will never be turned off. Since such a

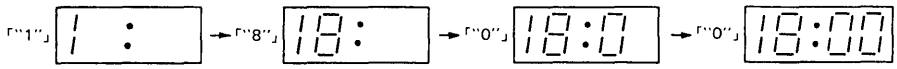
MODSW2
MODSW1
MODSW0

OFF-time checking is performed when the ON-time is encountered, OFF-time should be set at least before the ON-time.
In otherwise, if only OFF-time is set, the timer-OFF action will function properly. That is, OFF-time has a higher priority than the ON-time.
Five sources, AM, FM, PHONO, TAPE, and AUX, are programmable. The programming procedure is as follows.

① Set programmable mode switch to TIMER WRITE mode. Then the present time is indicated.

② Press the desired ON-key of EVERYDAY1, EVERYDAY2, or ONCE. Then the colon is displayed, and a preset station indicater LED corresponding to the depressed ON-key turns on for about 60 ms.

③ Set time in 4-digit input by using ten-keys 0–9 of momentary switches just similar to the clock set.
(Ex.) Setting 6:00 p.m.

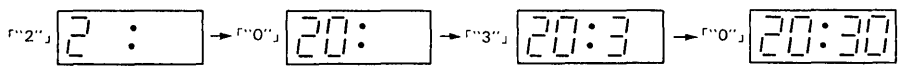


④ Press key corresponding to the desired source (FM, AM, PHONO, TAPE, or AUX). (Even if FM ONLY is specified, you must input FM.)
In cases that PHONO, TAPE, or AUX key is pressed, the corresponding source selector terminal goes High for about 500 ms.
In cases that FM or AM key is pressed, TUNER terminal goes High and FM/AM terminal is activated until a preset station key (1–8) is pressed. By using the statuses of the TUNER and FM/AM terminals, source selection ACKNOWLEGE signal can be generated (refer to description of AM/FM terminal).
When PHONO, TAPE, or AUX key is pressed, present time will be indicated after about 500 ms (the source selector terminal goes High level for that 500 ms), whereas the programmed ON time is indicated until preset station key is pressed when FM or AM key is pressed.

⑤ When FM or AM is selected as a source in ④, the next step to press the desired preset station key (1–8) is required. Then, preset station indicator LED corresponding to the pressed key turns on for about 60 ms. After that, the display will be changed from the programmed ON time to the present time.
(Note) If any wrong time is set or wrong source is selected, switch the programmable mode switch to another mode, and, restart programming from ① or restart programming from ② after finishing ④ or ⑤.

⑥ Press OFF key that corresponds to the ON key pressed in ②.
Then, only colon is indicated. The preset station indicator LED corresponding to the pressed OFF key turns on for about 60 ms.

⑦ Set time in 4-digit number by using ten-keys 0–9 of momentary switch.
(Ex.) Setting 8:30 p.m.



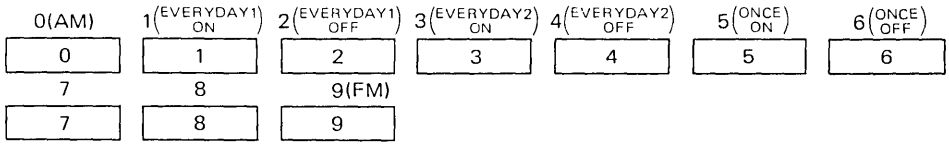
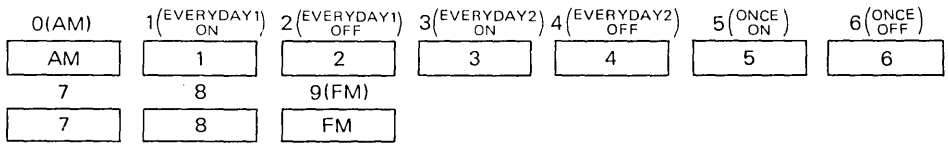
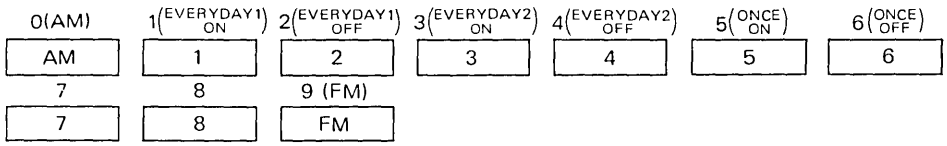
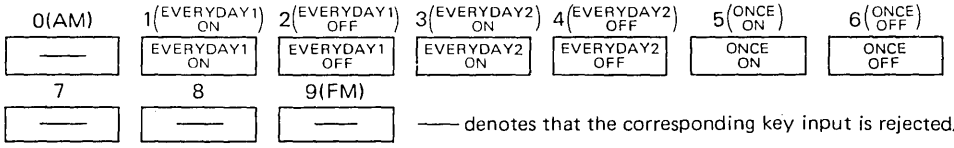
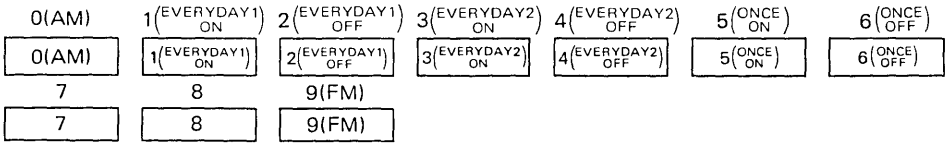
When the input of the fourth digit is over, the above display is changed to the present time indication.
(Note) When any key is wrongly pressed, finish the process up to the fourth digit and then restart the process from ⑥.

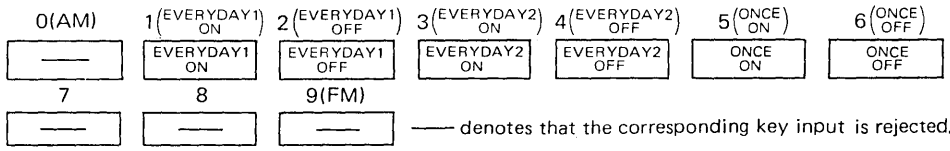
⑧ Set programmable mode switch to TIMER-OPERATION. Then the present time is indicated.
(Note) If timer operation is desired, be sure to set programmable mode switch to TIMER OPERATION. Otherwise timer does not function.

6. TIMER CANCEL mode
Mode for canceling programmed times ON/OFF times and source. Follow the process described below.

MODSW2 MODSW1 MODSW0	① Set programmable mode switch to TIMER CANCEL. Then the present time is indicated. ② Press the ON key of timer to be canceled. (EVERYDAY1, EVERYDAY2, or ONCE). Then colon is indicated momentarily, the programmed ON time and source are canceled, and, immediately, the present time indication is recovered. ③ Press OFF key that corresponds to the ON key pressed in procedure ②. As in ②, colon is indicated momentarily, the programmed OFF time is canceled, and, immediately, the present time indication is recovered.

2-3. Momentary Switches

Symbol	Description of Function
0–9	These keys are multiple function keys. Their functions varies dependent on the positions of programmable mode switches (MODSW0,1,2). (1) In the CLOCK SET mode.  When CLOCK SET mode is selected, the keys are used as ten-keys for setting time. (2) In the RADIO mode  When RADIO mode is selected, the keys are used for AM/FM band switching and as preset station keys. (3) In the TIMER OPERATION mode.  The functions of the keys are almost the same as those in the RADIO mode. Only difference is that the keys are not accepted during timer operation. (4) In the TIMER READ mode.  —— denotes that the corresponding key input is rejected. When TIMER READ mode is selected, only ON/OFF keys of EVERYDAY1, EVERYDAY2, and ONCE are in effect to confirm programmed timer times and source. (5) In the TIMER WRITE mode  When TIMER WRITE mode is selected, the functions of the keys are differently dependent on the sequence of key operation. (For details, see 2-2. Alternate Switches) (6) In the TIMER CANCEL mode.

0 – 9	 When TIMER CANCEL mode is selected, depressing ON/OFF keys of EVERYDAY1, EVERYDAY2, or ONCE cancels the programmed timer times and sources.
OFF	This is the key to cut off power supply relay. By depressing this key, AC OUT terminal and select or terminals (AUX, TAPE, PHONO, and TUNER) are forced to low level and get indication of time on the display. To turn on the power Supply relay, depress one of the AM, FM, preset station keys (1–8) or source selector keys (TAPE, PHONO or AUX) in the RADIO mode.
CLKCAL	Key to call present clock time during frequency display. When this key is pressed, the present clock time is indicated for five seconds and then the frequency display is recovered.
CHSCAN	Key to scan preset channels. When this keys is pressed, the memorized preset stations (1–8) are in turn scanned from "1", holding for 5 sec at each preset station. To stop scanning at the currently received station, press the preset station key currently selected.
UP DOWN	Kyes for auto and manual tunings. When either key is pressed, the following functions are performed. (1) When AUTO/MANUAL switch is set to AUTO. Keying of UP increases frequency in saw-tooth wave mode. If the SD terminal is forced to high level during this process, the automatic upward searching is stopped. Keying of DOWN brings about automatic downward searching. Function of the DOWN key is almost the same as that of the UP key. Only difference is that the DOWN key decreases the frequency. *1 Automatic upward or downward searching is performed at the rate of 60 ms/step (MIN). This rate will varies depending on the lock-up time of the PLL system. *2 If UP or DOWN key is pressed during automatic searching is carried on, the automatic upward/downward searching is kept going on. (2) When AUTO/MANUAL switch is set to MANUAL. When UP or DOWN key is momentarily pressed, frequency is shifted by one step (channel space) upward or downward. When UP or DOWN key is kept pressed for 0.5 second or more, the frequency shift is continued upward or downward at the rate of 60 ms/step (TYP.) until the key is released. (Note) Even if the AUTO/MANUAL switch is turned to MANUAL during auto process, the auto tuning is not intercepted. If the auto-tuning is required to be stopped immediately by switching to MANUAL, formulate the system in such a way that SD terminal is forced to high level whenever the AUTO/MANUAL Switch is turned to MANUAL.
MEMORY	Key used to write currently received frequency into a preset memory. When either of keys 1–8 is depressed within 5 seconds after this key is pressed, the currently received frequency is written into the memory corresponding to the keyed-in switch (1–8). The memory write-enable state lasts 5 sec. from the time when the MEMORY key is pressed. To cancel this state within the 5 sec., press a key other than preset channel keys (1–8) or change the mode switches (MODSW0, 1, 2).
PHONO TAPE AUX	Keys to select a source. When programmable mode switches (MODSW0, 1, 2) are set to RADIO, keying one of these switch will force AC OUT terminal and the source select or terminal corresponding to the pressed key to high level. When programmable mode switches are set to TIMER WRITE, the deying-in of either switch will shift the corresponding select terminal to high level for about 500 ms.

2-4. Transistor Switch

Remote control signal is input to this switch. (For configuration, see 1–2, Connection of Keys and Switch Types on Key Matrix.) The remote control signal should also be input to the $\overline{RMC}$ terminal at the same time.

Fig. 1 shows the wave form of remote control signal. The first 10 ms low level stands for initializing signal. The number of the following pulses determines the type of operation.

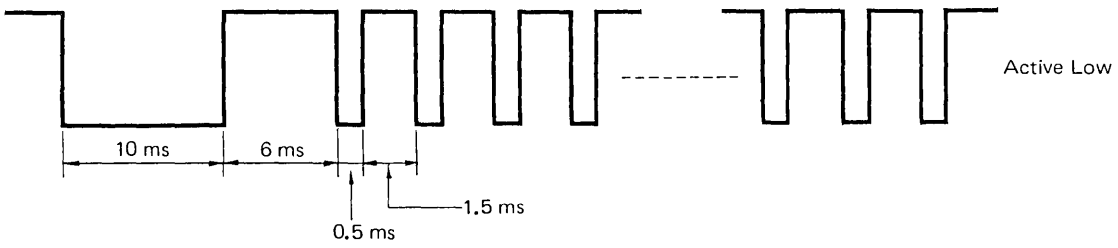


Fig. 1 Timing Waveform of Remote Control Signal

The signal discriminated by key input (K_1 terminal) via the transistor switch is the initializing signal only. The following pulse train is discriminated by $\overline{RMC}$ terminal.

Table 1 shows the correspondence between pulse counts and operations.

Table 1 Number of Pulses and Related Operation

Number of Pulses	Operation
0–7	Preset CH (1–8)
8–10	Don't care
11	AUX
12	PHONO
13	FM
14	TAPE
15	AM

3. DESCRIPTION OF DISPLAY

3-1. Display Connection Diagram

Fig. 2 shows the connection of the display. D1–D6, Sa–Sg, COLON, and DP (decimal point) correspond to digit terminals ($\overline{D1}$–$\overline{D6}$), segment terminals (Sa–Sg), $\overline{COLON}$ terminal, and $\overline{DP}$ terminal of μPD1704C-011, respectively.

Since the segment terminals of μPD1704C-011 have breakdown voltage of 30 V (corresponding to Pch open drain output voltage), they can be directly connected to FIP (fluorescent indicator panel). Digits ($\overline{D1}$–$\overline{D6}$), $\overline{COLON}$, and $\overline{DP}$ are complementary outputs and they are output in active low. Hence one stage of buffer (with PNP transistor 2SA733 or equivalent) is required.

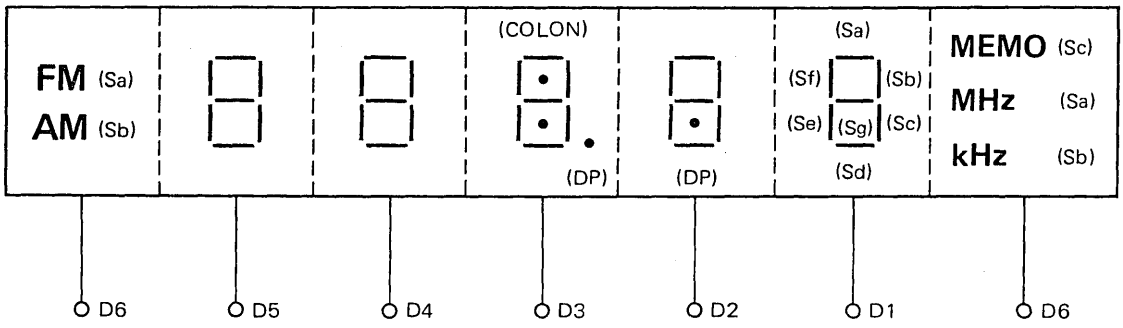


Fig. 2 Example of Indicator Display

3-2. Examples of Displays

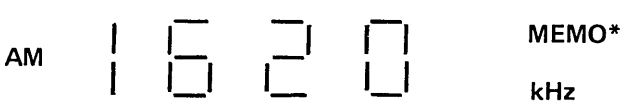
The typical displays are as follows.

(1) FM in the U.S.A.

(2) FM in Europe

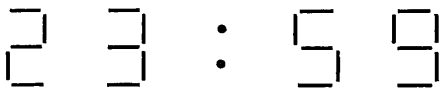
(3) FM in Japan

(4) AM in the U.S.A.



(5) AM in Europe or in Japan

(6) Clock display



* Display of MEMO is turned on for 5 seconds when the momentary key MEMORY is pressed, i.e. when the key is pressed in order to write the current frequency into the memory. If preset key either of 1–8 is pressed within that 5 seconds, the new frequency is memorized and the indication MEMO goes off.

4. DESCRIPTION OF PROGRAMMABLE TIMER OPERATIONS

There are three sets of programmable timers; EVERYDAY1, EVERYDAY2, and ONCE.

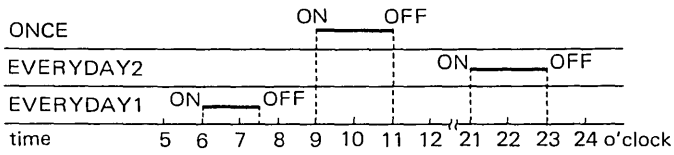
Once programmed with ON/OFF times and source, EVERYDAY1 and EVERYDAY2, execute everyday ON and OFF of the programmed source at the programmed ON/OFF times.

While, in ONCE, programmed source and ON/OFF times are canceled after the source ON/OFF execution is performed.

The priority of these timers is in the sequence of ONCE, EVERYDAY2, and EVERYDAY1. In each timer system, OFF has higher priority than ON. Hence the following performance patterns are realized according to the timing relationship.

① ON and OFF times are not crossed over.

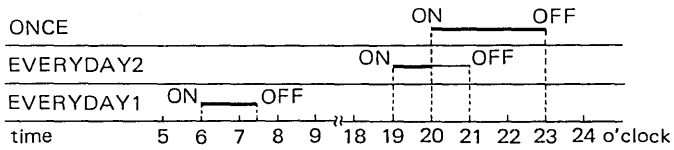
	ON time	OFF time
ONCE	9:00	11:00
EVERYDAY2	21:00	23:00
EVERYDAY1	6:00	7:30



(Note) — Denotes timer in operation.

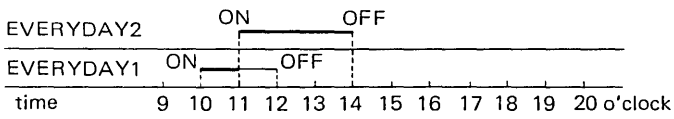
② ONCE goes ON during EVERYDAY2 is in operation.

	ON time	OFF time
ONCE	20:00	23:00
EVERYDAY2	19:00	21:00
EVERYDAY1	6:00	7:30



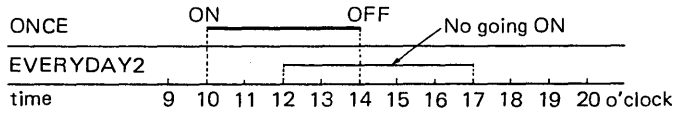
③ EVERYDAY2 goes ON during EVERYDAY1 is in operation.

	ON time	OFF time
EVERYDAY2	11:00	14:00
EVERYDAY1	10:00	12:00



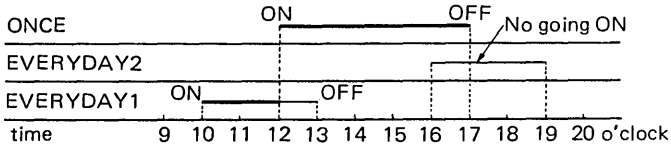
④ EVERYDAY2 goes ON during ONCE is in operation.

	ON time	OFF time
ONCE	10:00	14:00
EVERYDAY2	12:00	17:00



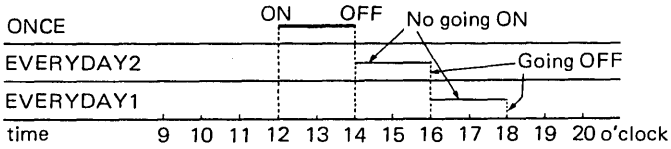
⑤ ONCE goes ON during EVERYDAY1 is in operation, and, EVERYDAY2 goes ON during ONCE is in operation.

	ON time	OFF time
ONCE	12:00	17:00
EVERYDAY2	16:00	19:00
EVERYDAY1	10:00	13:00



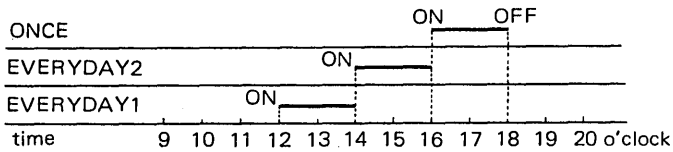
⑥ Continuously programmed in the sequence of ONCE, EVERYDAY2, and EVERYDAY1.

	ON time	OFF time
ONCE	12:00	14:00
EVERYDAY2	14:00	16:00
EVERYDAY1	16:00	18:00



⑦ Reversed sequence of ⑥

	ON time	OFF time
ONCE	16:00	18:00
EVERYDAY2	14:00	16:00
EVERYDAY1	12:00	14:00



5. TYPICAL APPLICATIONS

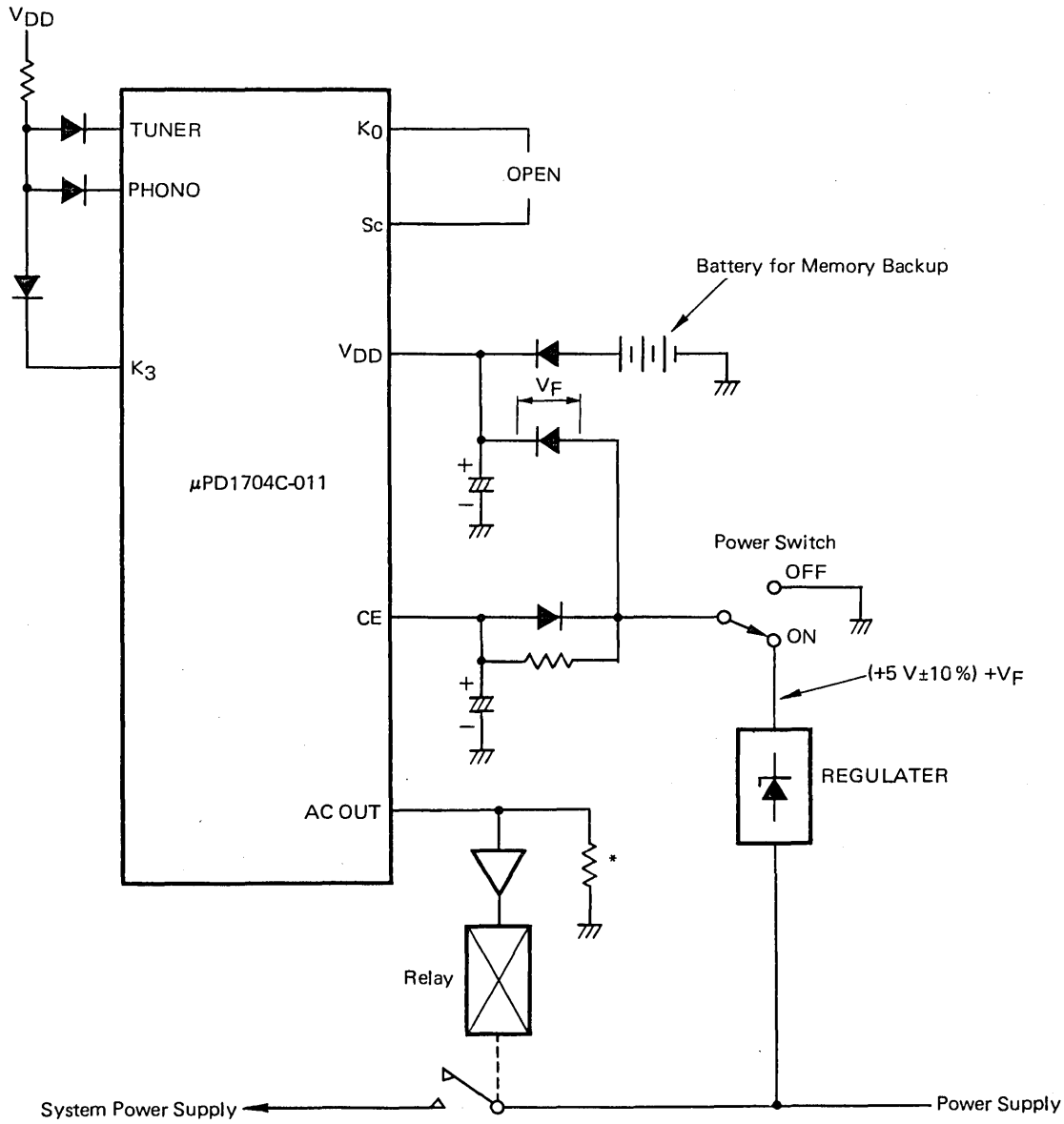
A wide variety of set models can be developed by combining initial setting diode matrix, NONCLOCK and FM ONLY and remote control function. The following table shows some examples of the variations and effective keys on each variation.

LEGEND on symbols

(key) ○ : Function effective　　× : Function ineffective
● : All the key functions diffective　　AM : Only AM effective
FM : Only FM effective　　– : Ineffective (prohibited)

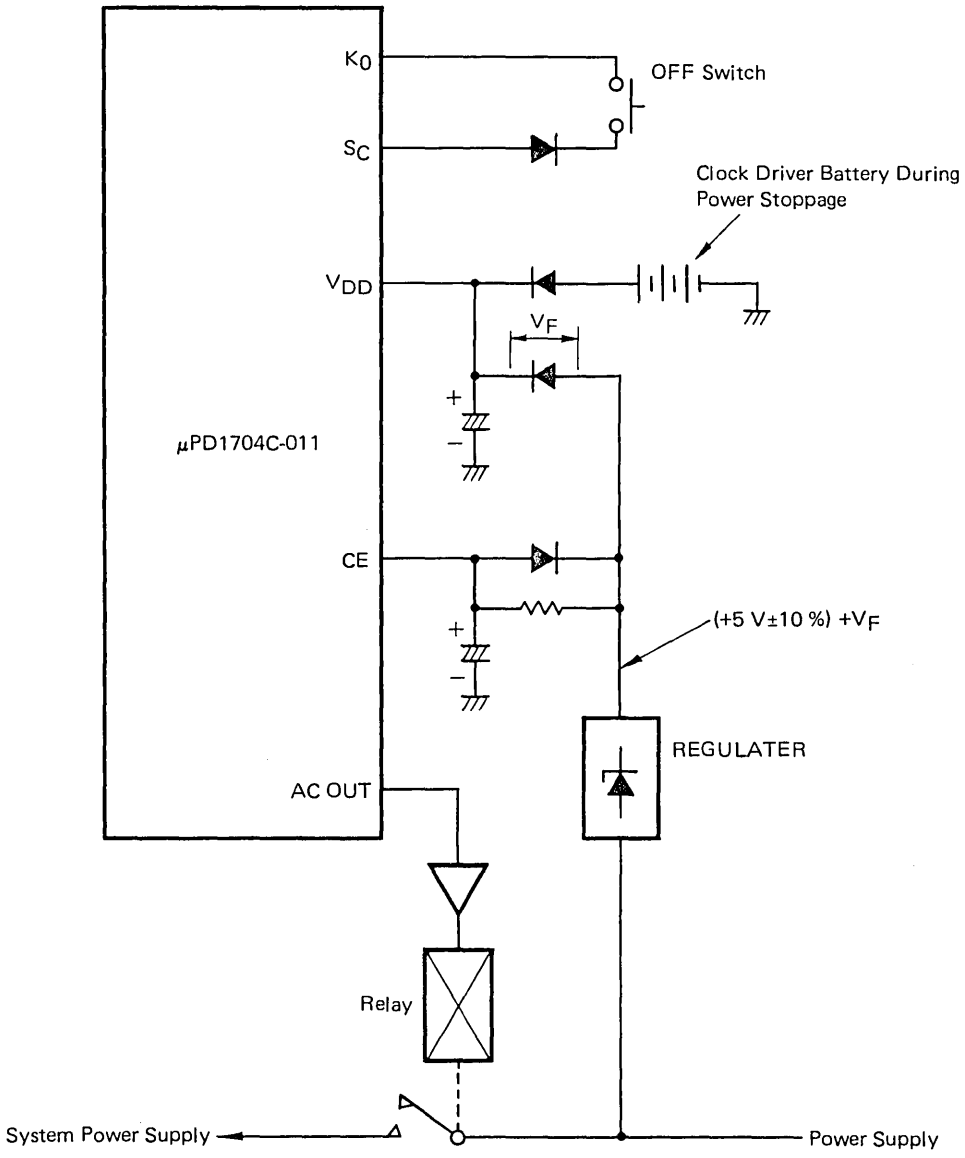
KEY \ Type Number		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Initial Setting Switch	NONCLOCK	ON	OFF		ON	OFF		ON	OFF		ON	OFF		ON	OFF		ON	OFF		ON	OFF		ON	OFF	
	FM ONLY	OFF												ON											
Function	BAND	Both AM and FM												FM Only											
	Remote Control	×						○						×						○					
	Source Selector	×			○			×			○			×			○			×			○		
	Clock	×	○		×	○		×	○		×	○		×	○		×	○		×	○		×	○	
	Timer	×	×	○	×	×	○	×	×	○	×	×	○	×	×	○	×	×	○	×	×	○	×	×	○
Effective Keys or Switches	0 (AM)	AM	●		AM	●		AM	●		AM	●		–	0		–	0		–	0		–	0	
	1 (EVERYDAY1 ON)	1	●		1	●		1	●		1	●		1	●		1	●		1	●		1	●	
	2 (EVERYDAY1 OFF)	2	●		2	●		2	●		2	●		2	●		2	●		2	●		2	●	
	3 (EVERYDAY2 ON)	3	●		3	●		3	●		3	●		3	●		3	●		3	●		3	●	
	4 (EVERYDAY2 OFF)	4	●		4	●		4	●		4	●		4	●		4	●		4	●		4	●	
	5 (ONCE ON)	5	●		5	●		5	●		5	●		5	●		5	●		5	●		5	●	
	6 (ONCE OFF)	6	●		6	●		6	●		6	●		6	●		6	●		6	●		6	●	
	7	7																							
	8	8																							
	9 (FM)	FM	●		FM	●		FM	●		FM	●		–	9	●	–	9	●	–	9	●	–	9	●
	REMCON	–						●						–						●					
	OFF	–	●		–	●		–	●		–	●		–	●		–	●		–	●		–	●	
	CLKCAL																								
	CHSCAN	●																							
	UP																								
	DOWN																								
	MEMORY																								
	PHONO	–			●			–			●			–			●			–			●		
	TAPE																								
	AUX																								
MODE SW	CLOCK SET	–	●		–	●		–	●		–	●		–	●		–	●		–	●		–	●	
	RADIO	●																							
	TIMER OPE	–	●		–	●		–	●		–	●		–	●		–	●		–	●		–	●	
	TIMER READ																								
	TIMER WRITE																								
	TIMER CANCEL																								

5-1. Example of types without remote control nor clock (Corresponding type numbers : 1, 4, 13, and 16)

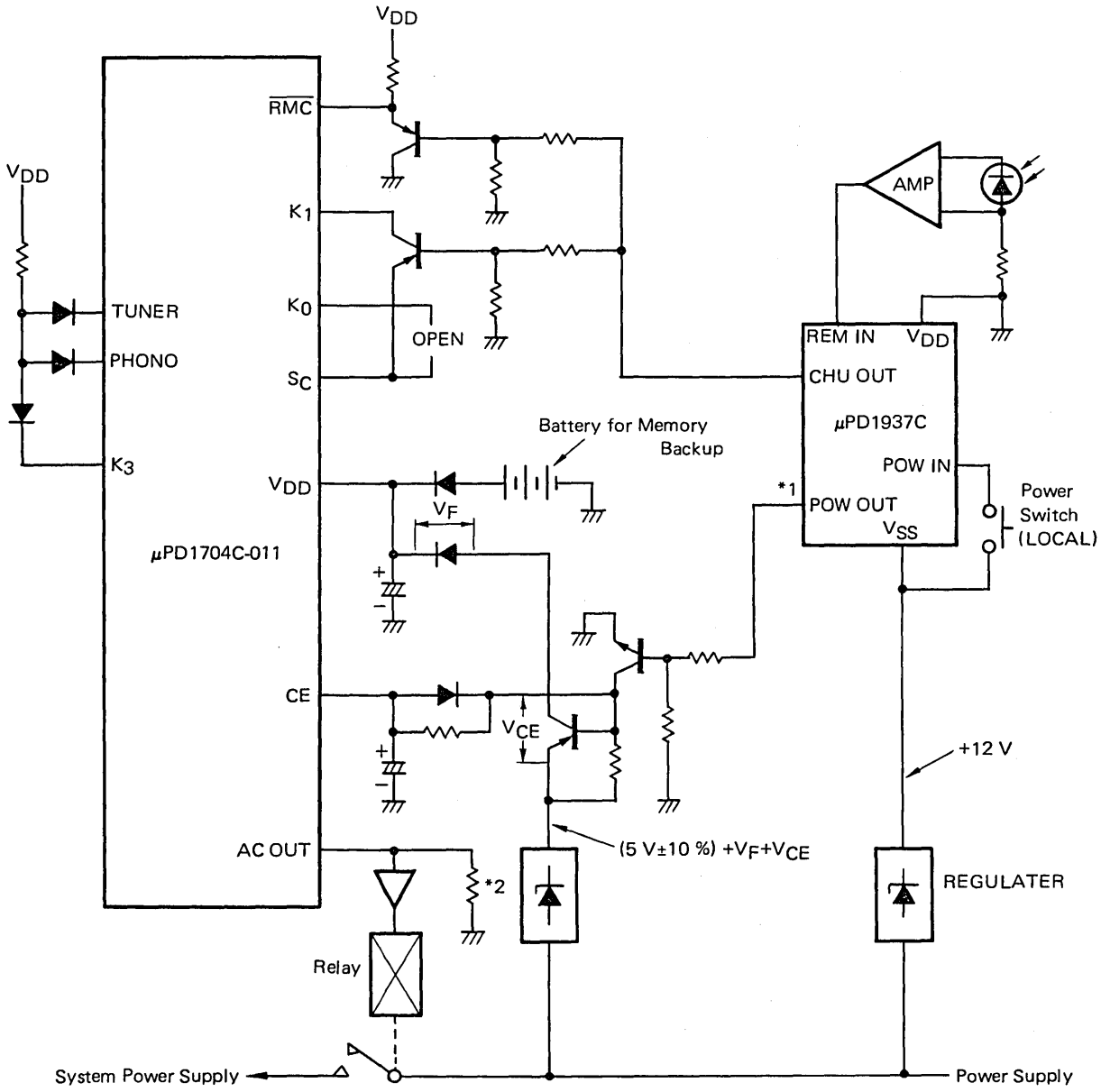


* AC OUT terminal might become high impedance when power switch is OFF. Hence be certain to insert a pull-down resistance.

5-2. Example of types with clock but without remote control
(Corresponding type numbers : 2, 3, 5, 6, 14, 15, 17, and 18)



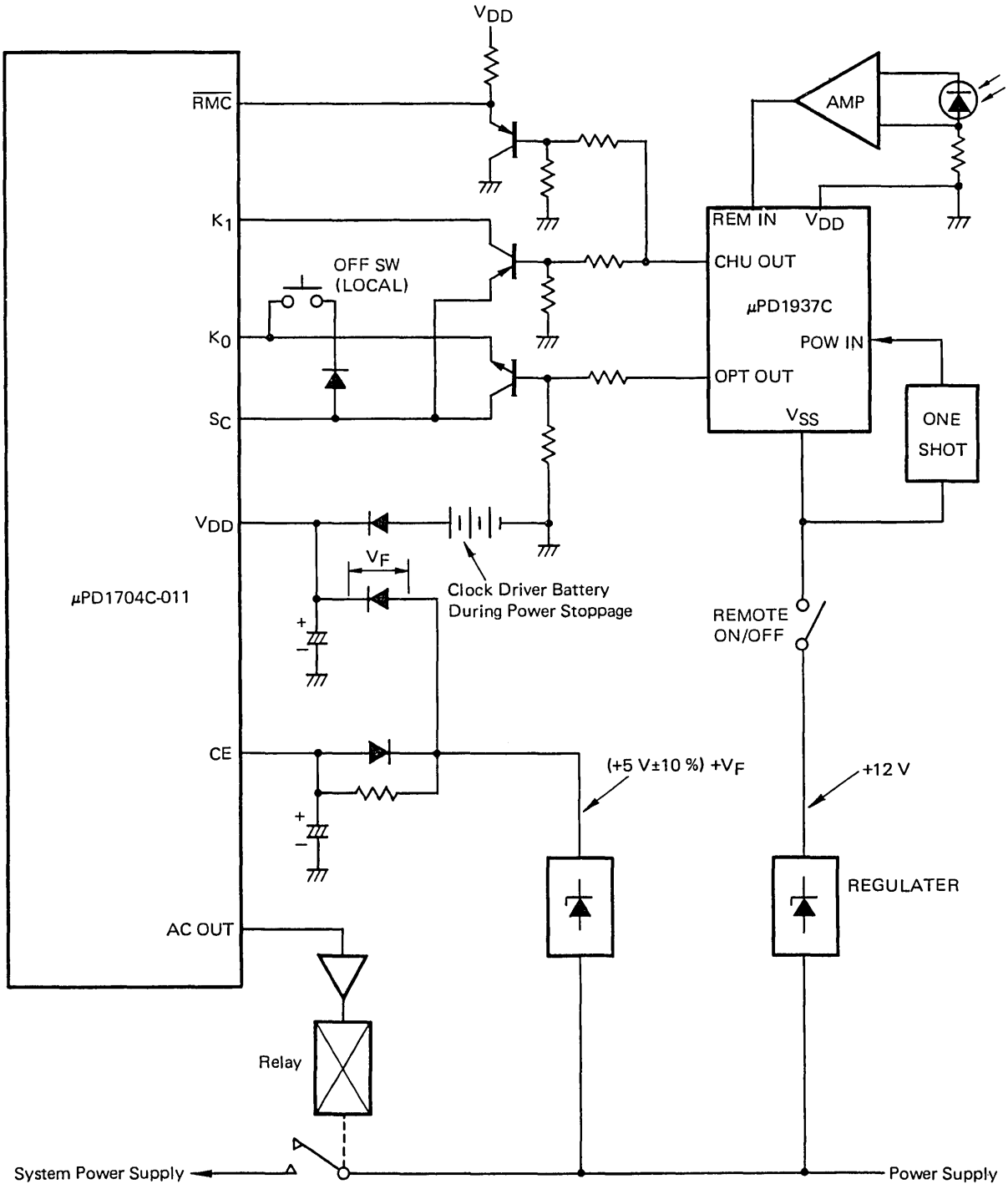
5-3. Example of types with remote control but without clock (Corresponding type numbers : 7, 10, 19, 22)



* Note 1.) To turn system ON/OFF by remote control, use POW switch of transmitter (μPD1986C)

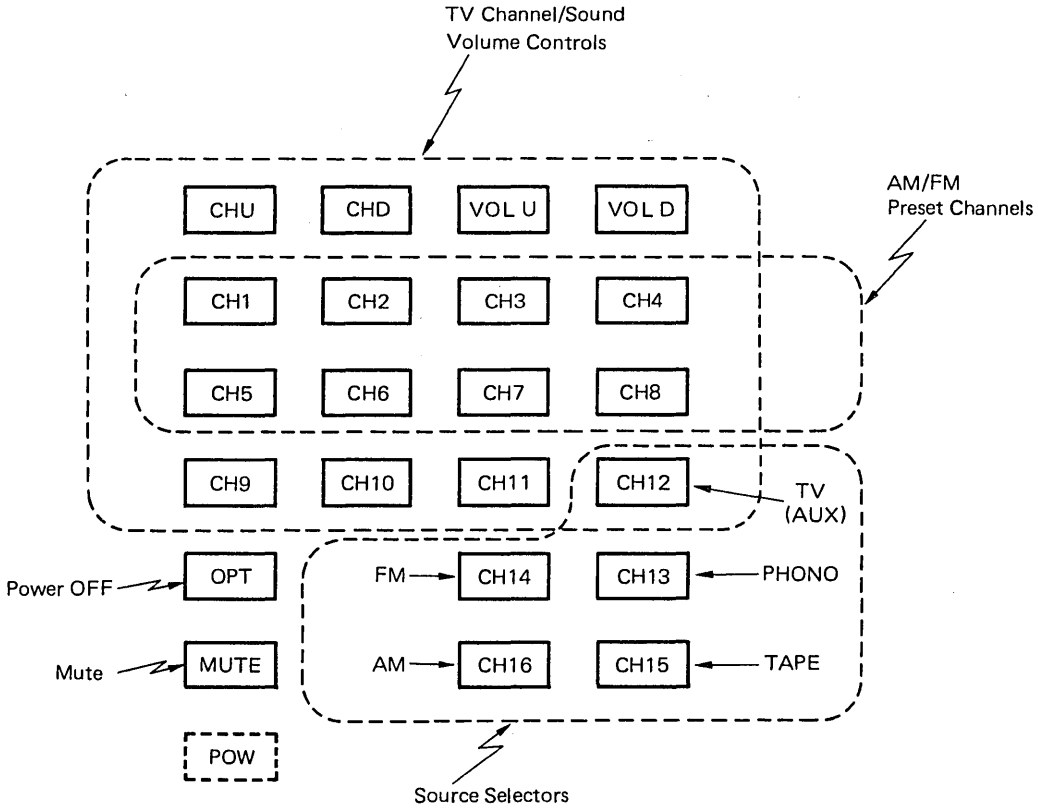
2.) AC OUT terminal might become high impedance when power switch is OFF. Hence be certain to insert a pull-down resistance.

5-4. Example of type with both remote control and clock
(Corresponding type numbers : 8, 9, 11, 12, 20, 21, 23, 24)



Note) To turn system OFF by remote control, use OPT switch of transmitter (μPD1986C). Never use POW switch.

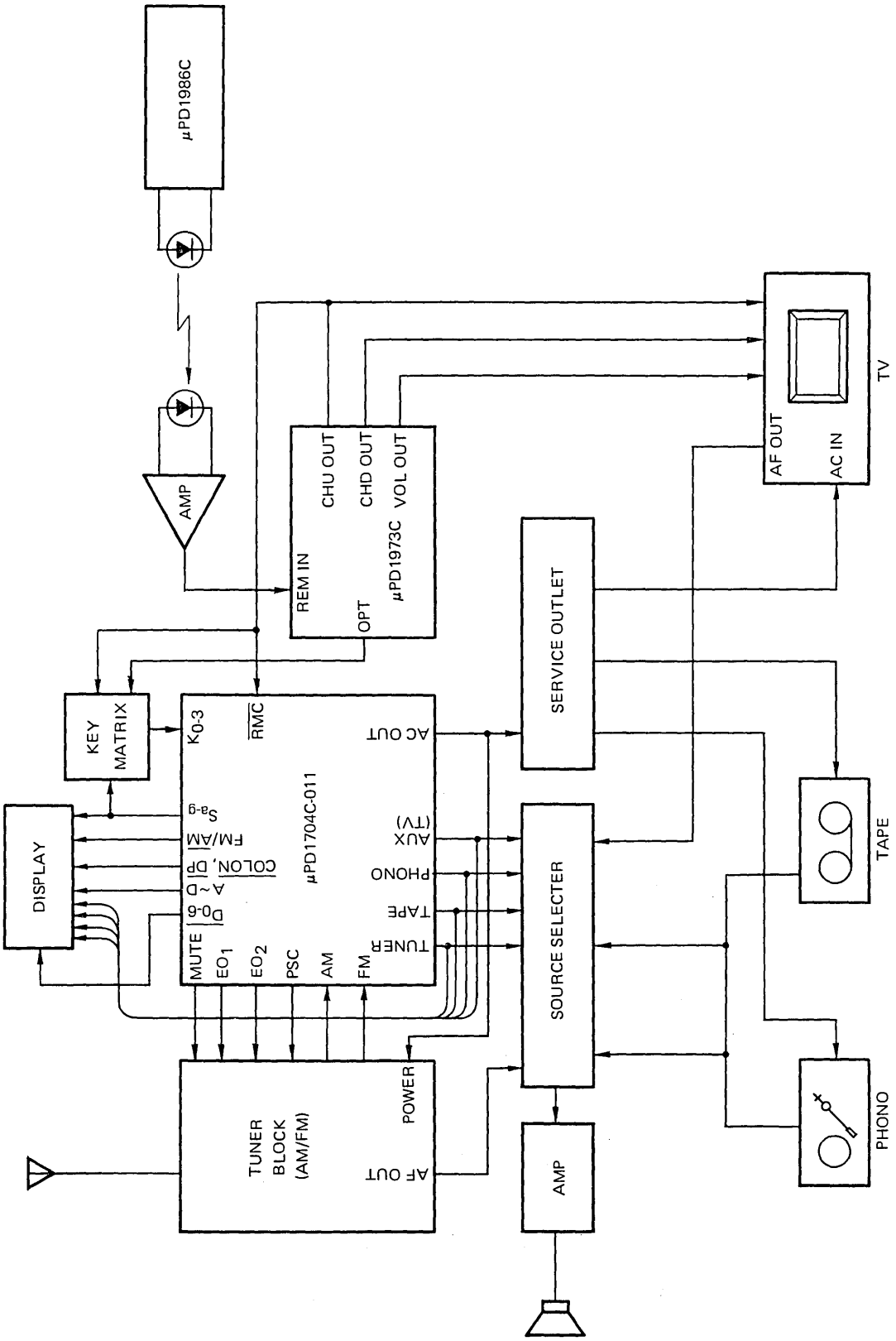
5-5. Key Allocation for Remote Control Transmitter (μPD1986C) (To be used in model types with clock)



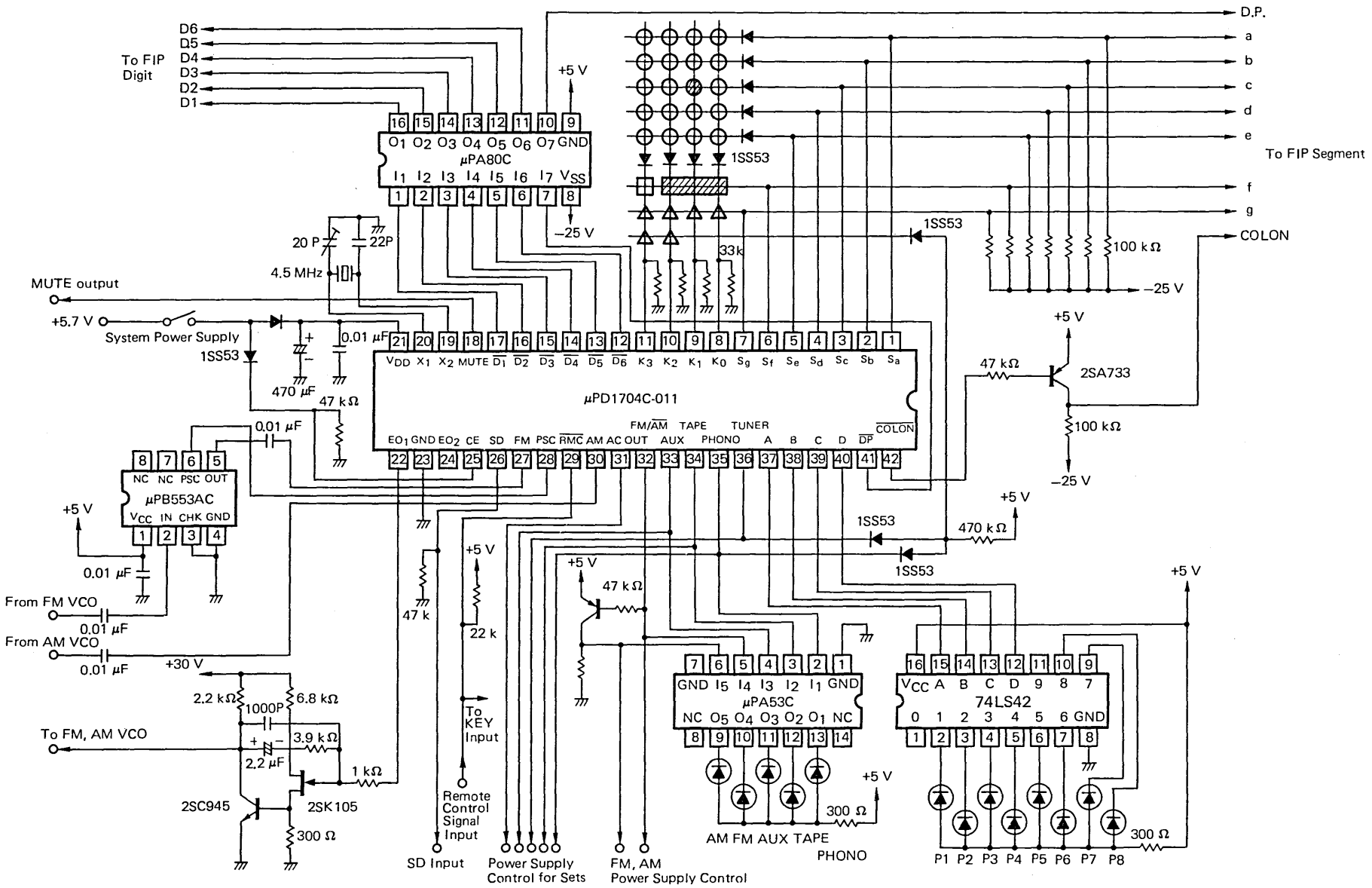
Note 1) In models with clock, POW switch of the remote control transmitter is not used. In models without clock, POW switch is used instead of OPT switch shown in the diagram.

Note 2) The symbols inside the square (▭) are those used in the specification of μPD1986C.

5-6. Multiplexed Stereo Sound TV Receiver Model with Remote Control/Clock
Example of application to music center



APPLICATION EXAMPLE OF CIRCUIT DIAGRAM



MOS DIGITAL INTEGRATED CIRCUIT
μPD1705C-012

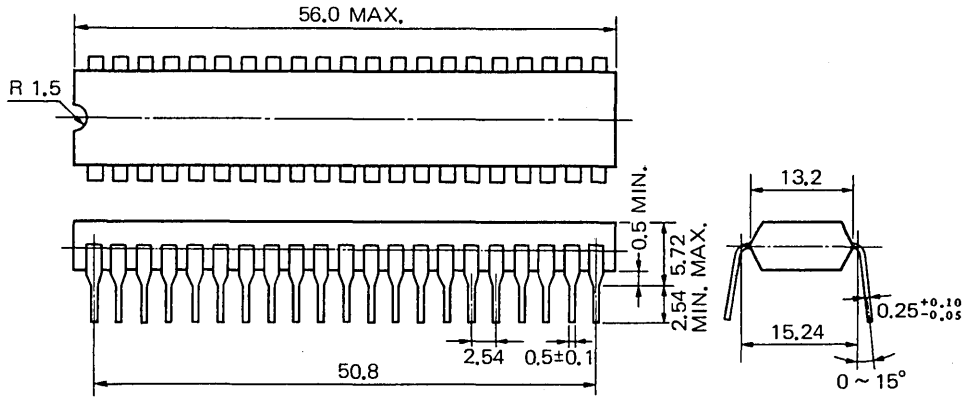
PHASE LOCKED LOOP FREQUENCY SYNTHESIZER
TV DIGITAL TUNING SYSTEM CONTROLLER
CMOS LSI

μPD1705C-012 is a CMOS LSI developed for television receivers of PLL frequency synthesizer system designed to U.S.A. and Canada. PLL and controller are contained on a single chip. This LSI, with the pre-scaler μPB562C, constitutes a high performance PLL television receiver system. Since PLL section uses pulse-swallowing system, fine tuning can be easily done with a high precision. Furthermore, it is provided with functions of remote control, clock, and timer.

FEATURES

- PLL and controller are packed in one chip.
- Multifarious station selection modes are provided.
  - 10-key direct selection ..... with automatic/manual switching
  - channel up/down selection ..... with automatic/manual switching
- High precision fine tuning capable by the use of pulse-swallowing system (1 step 40 kHz ± 2.2 MHz, max.)
- CATV stations can be selected.
- 12-hour system clock and ON/OFF timer contained within.
- Remote control receiver contained. (μPD1913C and μPC1373H are used.)
- Provided with the function to output BCD channel number to CRT display interface.
- CMOS structure with low power consumption.
- Single power supply of +5 V.
- 42-pin dual in-line package (DIP)

PACKAGE DIMENSIONS in millimeters



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{DD}	−0.3~+6.0	V
Input Voltage	V_I	−0.3~+V_{DD}	V
Output Voltage	V_O	−0.3~+V_{DD}	V
Output Current	I_O	10	mA
Operation Temperature	T_{opt}	−35~+75	°C
Strage Temperature	T_{stg}	−55~+125	°C
Output Breakdown Voltage	V_{BDS1}	Sa–Sg terminal: −35	V
Output Breakdown Voltage	V_{BDS2}	CH0–CH3, MS terminal: −15	V
Output Breakdown Voltage	V_{BDS3}	B01, B02 terminal: +15	V

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
Output Breakdown Voltage	V_{BDS1}			−30	V	Sa–Sg terminal: I_{OFF}=−5 μA
Output Breakdown Voltage	V_{BDS2}			−11	V	CH0–CH3,MS terminal: I_{OFF}=−10 μA
Output Breakdown Voltage	V_{BDS3}			13	V	BO1,BO2 terminal: I_{OFF}=−5 μA
Supply Voltage Rise Time	Trise			500	ms	V_{DD}=0→4.5 V

ELECTRICAL CHARACTERISTICS (Ta=−35 to +75 °C, V_{DD}=4.5 to 5.5 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
High Level Input Voltage	V_{IH1}	0.8V_{DD}		V_{DD}	V	$\overline{REM}$ terminal
High Level Input Voltage	V_{IH2}	0.7V_{DD}		V_{DD}	V	AFTU,AFTD,$\overline{SD}$,CE terminal
High Level Input Voltage	V_{IH3}	0.6V_{DD}		V_{DD}	V	K0–K3 terminal
Low Level Input Voltage	V_{IL1}	0		0.3V_{DD}	V	AFTU,AFTD,$\overline{SD}$,CE terminal
Low Level Input Voltage	V_{IL2}	0		0.2V_{DD}	V	K0–K3,$\overline{REM}$ terminal
High Level Output Voltage	V_{OH1}	4.0			V	EO,VOL terminal: I_{OH}=−0.5 mA
High Level Output Voltage	V_{OH2}	4.0			V	D1–D5,MUTE,PSC,LMP terminal: I_{OH}=−0.2 mA
High Level Output Voltage	V_{OH3}	3.0			V	Sa–Sg terminal: I_{OH}=−0.5 mA
High Level Output Voltage	V_{OH4}	2.5			V	CH0–CH3,MS,POW terminal: I_{OH}=−2.0 mA
Low Level Output Voltage	V_{OL1}			0.5	V	EO,VOL,LMP terminal: I_{OL}=0.5 mA
Low Level Output Voltage	V_{OL2}			0.5	V	D1–D5,MUTE,PSC terminal: I_{OL}=0.2 mA
Low Level Output Voltage	V_{OL3}			2.0	V	BO1,BO2 terminal: I_{OL}=2.0 mA
High Level Input Current	$+I_{IH1}$	10	40	100	μA	K0–K3 terminal: V_{IN}=V_{DD}=5.0 V
High Level Input Current	$+I_{IH2}$		300		μA	X1 terminal (Pull Down): V_{IN}=V_{DD}=5.0 V
Low Level Input Current	$-I_{IL}$		300		μA	IN terminal (Pull Up): V_{IN}=0 V, V_{DD}=5.0 V
High Level Input Leak Current	$+I_{LIH}$			10	μA	CE,$\overline{REM}$,AFTU,AFTD,$\overline{SD}$ terminal: V_{IN}=V_{DD}=5.0 V
Low Level Input Leak Current	$-I_{LIL}$			10	μA	CE,$\overline{REM}$,AFTU,AFTD,$\overline{SD}$,K0–K3 terminal: V_{IN}=0 V
Output Off Leak Current	I_L		10^{-3}		μA	EO terminal: V_O=V_{DD}, V_O=0 V
Frequency Response	f_{IN}	0.5		8.8	MHz	IN terminal: V_{IN}=0.7 $V_{p\text{-}p}$(MIN.),DC
Supply Current	I_{DD1}		3		mA	Normal Operation
Supply Current	I_{DD2}		0.6		mA	CE terminal=0 V, V_{DD}=5 V
Oscillation Stop Voltage	V_{DDS}		3.2	3.8	V	

OUTLINE OF FUNCTIONS

(1) BANDS

VHF/UHF/CATV in U.S. and CANADA

- VHF : 2 ch – 13 ch
- UHF : 14 ch – 83 ch
- CATV : A ch – W ch

(2) FUNCTION OF TUNING

- 10-key direct selection with automatic/manual switching.
- channel up/down selection with automatic/manual switching.

(3) MANUAL FINE TUNING (MFT)

- 1 step : 40 kHz ± 2.2 MHz MAX.
- 1 cycle : 125 ms

(4) AUTO FINE TUNING (AFT)

- 1 step : 40 kHz ± 2.2 MHz MAX.
- 1 cycle : 8 ms

(5) FUNCTION OF CLOCK AND TIMER

- 12-hour clock (AM or PM is displayed)
- On-off timer in every 24 hours

(6) FUNCTION OF REMOTE CONTROL

- Contains remote control receiver
- Using the μPD1913C (transmitter) and the μPC1373H (pre-amplifier)

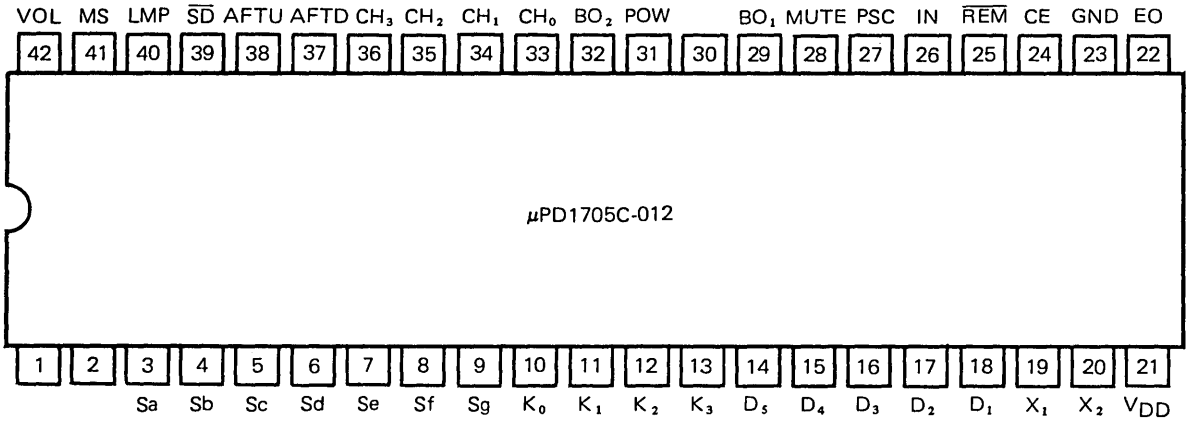
(7) DISPLAY

- Dynamic display in 5 digits (at 130 Hz)
  Channel ..... 2 digits and a display of CATV, panel locked, or remote controlled reception.
  Clock ..... 4 digits and a display of AM, PM, panel locked reception, or remote controlled reception.
- BCD output terminal for CRT display interface is provided to be connected via μPD4508C to MM58146.

(8) REFERENCE FREQUENCY

f_r = 5 kHz

PIN CONNECTION (Top View)



EXPLANATION OF INPUT AND OUTPUT TERMINALS

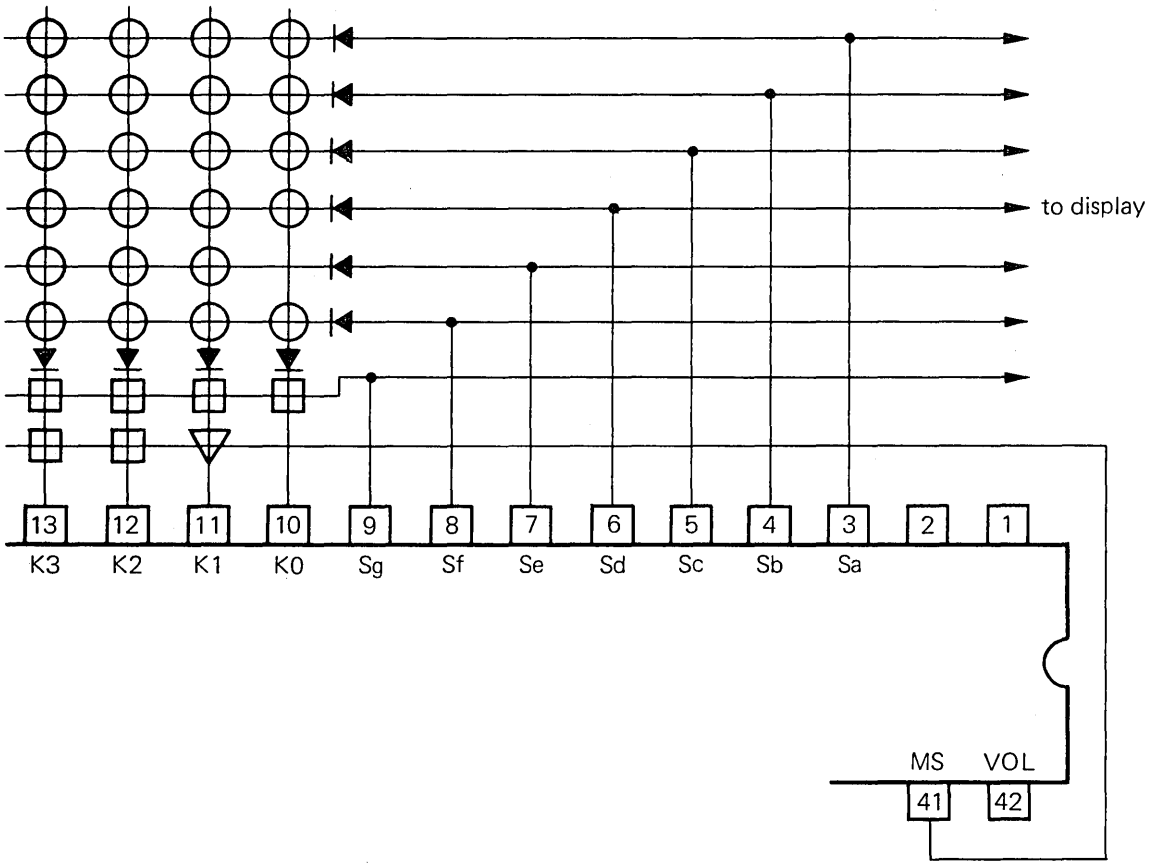
Pin Number	Symbol	Name of Terminal	Descriptions
3–9	Sa–Sg	Segment	7-segment display output, also used as output for key-matrix. High dielectric strength (–30 V). Active high.
10–13	K0–K3	Key	Input of key-matrix return signal.
14–18	D5–D1	Digit	Output of digit signal for display, also used for latch pulses for BCD output to CRT display (D3, D4). Active high.
19, 20	X1, X2	Reference Frequency Oscillator	Crystal oscillator of 4.5 MHz is connected here. Feedback resistance is contained.
21	V_{DD}	Power Supply	Voltage of +5 V ±10 % is supplied here. V_{DD} rise time of 500 ms or less is required. For too long rise time, initializing may not be normally performed.
22	EO	Phase Detection Output	Charge pumping output from phase detector. This output supplys tuning voltage to varactor of tuner via a low-pass filter.
23	GND	Grounding	Connected to the ground of system.
24	CE	Chip Enable	High : Normal operation Low : Memory retention (display off, PLL function disabled). Low level signal less than 134 μs is neglected.
25	$\overline{REM}$	Remote Control Signal Input	Input terminal for remote control signal. The output of preamplifier μPC1373H is connected here. Active low.
26	IN	Local Oscillator Input	Tuner local oscillation signal is input here via prescaler μPB562C. An a.c. anplifier is contained. So input should be connected through a capacitor.
27	PSC	Pulse Swallow Control	Output terminal of pulse swallow control signal. Connected to PSC terminal of prescaler μPB562C.
28	MUTE	Muting	Output terminal of signal to cut noises when PLL is unlocked. Active high.

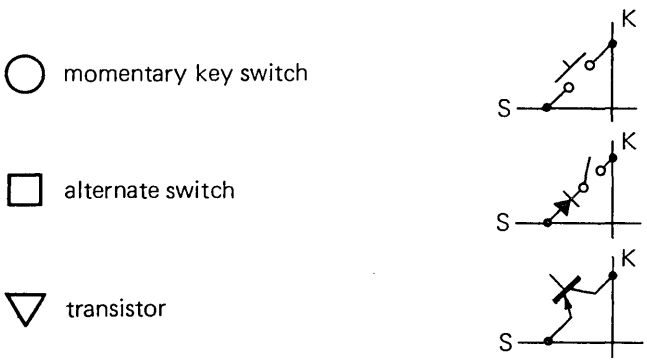
Pin Number	Symbol	Name of Terminal	Descriptions
29 32	BO1 BO2	Band	Output terminal of tuner band switching signal. The form of the signal is shown below. VL: BO1 = L, BO2 = H MB, VH: BO1 = H, BO2 = H SB: BO1 = H, BO2 = L UB: BO1 = L, BO2 = L
31	POW	Power	Output terminal for controlling power supply.
33–36	CH0–CH3	Channel Number Output	Output terminals for BCD data to CRT display interface. The number of receiving channel is output in 2-digit dynamic BCD signal.
37, 38	AFTU AFTD	AFT Input	Input terminal for AFT signal. AFT signal converted in binary form by comparator μPC393C is supplied here.
39	$\overline{SD}$	Station Detector	Input terminal for stop signal during auto tuning. Active low. However, it is necessary that it turns to low level within 100 ms after PLL locking.
40	LMP	Lamp	Output terminal for displaying remote control signal reception. A pulse of 20 ms duration is output when remote control signal is received.
41	MS	Mode Switch	Output terminal of return signal for sensing CATV/TV and AUT/MAN switching.
42	VOL	Volume	Output terminal of varialbe-duty pulses to control volume. The signal is input to d.c. attenuator via an external lowpass filter.

CONNECTION TO THE MATRIX OF KEYS

	K3 (13)	K2 (12)	K1 (11)	K0 (10)
Sa (3)	0	1	2	3
Sb (4)	4	5	6	7
Sc (5)	8	9	CLEAR	RECALL
Sd (6)	FTU	CHU	VOLU	MUTE
Se (7)	FTD	CHD	VOLD	–
Sf (8)	HADJ	MADJ	PL	POWER
Sg (9)	CLOCK	ONTIM	OFTIM	TIMER
MS (41)	CATV/TV	AUT/MAN	SDCONT	–

COMPOSITION OF KEYS





EXPLANATION OF CONTROL KEYS

Symbol	Function
0–9 (Number Key)	Used for direct channel selection. For direct channel selection, input the number of desired channel in two digits. (Channel 8 or 12 is selected by keying (0), (8) or (1), (2), respectively.) When, after keying the first digit in either of 2–9, the second keying is delayed more than 2–3 seconds, the channel corresponding to the first keyed number is selected. (keying of only (3) selects Channel 3.) If some non-existing channel number is keyed-in, no channel selection is done, and the display recovers the preceding channel number. In auto-mode (when AUT/MAN switch is on), when no station is detected in the channel specified by keying, the channel automatically shifts up as far as the channel where station can be detected.
CLEAR	If the first keying has been done wrong for direct channel selection, depress this key to recover the original state immediately. Then, follow the selection process from the beginning.
RECALL	This key switches display modes. Every time when this key is depressed, clock or channel is alternatingly displayed.
CHU (up-channel selection)	In auto-mode (when AUT/MAN switch is on), when this key is depressed, the channel shifts up until the channel transmitting wave is found. When this key is further kept pressed down, the reception of the selected channel will be kept for 600 ms and then the channel will shift up again until another station is received. This procedure is repeated until the key is released. In manual mode (when AUT/MAN switch is off), when this key is kept depressed, the channel again shifts up by 1 after a waiting time of 600 ms. This procedure is repeated until the key is released.
CHD (down-channel selection)	This key is only different from CHU in the shifting down-channel, instead of up-channel. Others are the same as CHU.
FTU (fine tuning upward)	This key serves for fine tuning. It is enabled only in manual mode. Depressing this key and then releasing within 500 ms makes the tuning frequency shift upward by 40 kHz. After the depression is kept for 500 ms, the tuning frequency is raised by 40 kHz, once after every 125 ms. When the upper limit (+2.2 MHz) is reached by this procedure, the frequency goes down to the lower limit (−2.2 MHz) and again the upward shifting starts. When other channel is selected, the fine tuning condition is resetted.
FTD (fine tuning downward)	This key is only different from FTU in the frequency shift downward instead of upward. Other features are the same as FTU.
VOLU (increase volume)	This is the key to control sound level. When this key is depressed the sound level is raised by 1 step in every 100 ms until the key is released. The total number of steps is 64, (duty ratios are 0, 3/67–65/67) so as to adjust the sound level smoothly.
VOLD (decrease volume)	This key is only different from VOLU in the volume level attenuating instead of raising. Other features are the same as VOLU.
MUTE (muting)	This key is used to mute sound. Every time when this key is depressed, mute output is reversed. The muting is released when power is turned on, when a volume control key (VOLU or VOLD) is operated, or when any channel is selected.
POW (power)	This key controls the power source. Every time when this key is depressed, power output is reversed. When power is in off-state, only POW key, PL key, time adjuster key and switch is in enabled condition. When power is turned on, channel is on display, while it is turned off, clock is displayed.
PL (panel lock)	This key prevents misoperation. When panel lock is on, keys other than POW key and PL key are ineffective. When power is on, panel lock is released.

Symbol	Function
HADJ (hour adjust)	This key is used to adjust hour. This is effective only when a time adjuster switch (CLOCK, ONTIM, or OFTIM) is on position. When this key is depressed and then released within 500 ms, the hour is advanced by 1 hour. If the depression is held longer than 500 ms, the hour is further advanced by1 hour once every 250 ms after the 500 ms until the key is released.
MADJ (minute adjust)	This key is used to adjust minute. The performance is basically the same as HADJ. When the advancement reaches 60 minutes, it returns to zero without counting up in hour.
CLOCK (clock adjustment)	This is the clock adjustment mode switch. When this is turned on, clock is displayed and HADJ and MADJ keys are available. While this is on, the clock is stopped, and, when the switch is turned off, the clock start from 0 second. When panel lock is on, the clock cannot be adjusted by turning this switch on, but, it should be noted that second is reset to 0 by this switch.
ONTIM (on-timer adjustment)	This is the on-timer adjustment mode switch. When this switch is turned on, the on-timer mode is displayed and the on-timer can be adjusted to the desired setting by using HADJ and MADJ keys.
OFTIM (off-timer adjustment)	This is the off-timer adjustment mode switch. When this switch is turned on, the off-timer mode is displayed and the off-timer can be adjusted to the desired setting by using HADJ and MADJ keys.
TIMER (timer)	This is the timer selection switch. When this switch is turned on, the timer acts at the preset time. When it is off, the timer does not act at the preset time.
CATV/TV (band switching)	This is the band selection switch. When the switch is on, CATV is selected, and when off, TV is selected. When CATV is selected, Channels 2–36 (Channels 2–13: VHF, and, Channels 14–36: CATV) can be received, while TV is selected, Channels 2–83 (Channels 2–13: VHF, and, Channels 14–83: UHF) can be received. The switching initialize the channel to Channel 2.
AUT/MAN (auto/manual)	This is the mode selection switch for channel selection and fine tuning. When this is on, auto mode is taken, and when off, manual mode is taken. In auto mode, the channel selection is accompanied by the detection of broadcast signal and AFT acts always. In manual mode, no signal detection is performed. At the same time, MFT mode is taken and FTU and FTD keys are effective.
SDCONT (station detect control)	This is the broadcast signal detection time adjustment switch. Usually it is off where the station signal detection is started about 100 ms after PLL lock. When it is on, the time for detection is prolonged by the unit of 100 ms until the switch is turned off. Therefore it is possible to control station signal detection time by external signal using transistor switch.

RELATION BETWEEN CATV CHANNEL AND INPUT CHANNEL NUMBER

The correspondence of CATV channels to actually keyed-in channel numbers as well as displayed channel numbers is shown in the following table.

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W
14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36

EXPLANATION OF REMOTE CONTROL SYSTEM

The μPD1705C-012 contains remote-control receiver. Combined with μPD1913C (transmitter) and μPC1373H (receiver preamplifier), it can be remote controlled.

Functions enabled by the remote control are:

- direct channel selection with 10-key (auto/manual)
- channel up/down selection (auto/manual)
- channel selection clearing (see the description above of CLEAR key)
- Power on/off
- muting on/off
- panel lock on/off
- volume up/down (in 64 steps)····initial level 25 %
- remote-controlled reception identification signal (on LMP terminal)

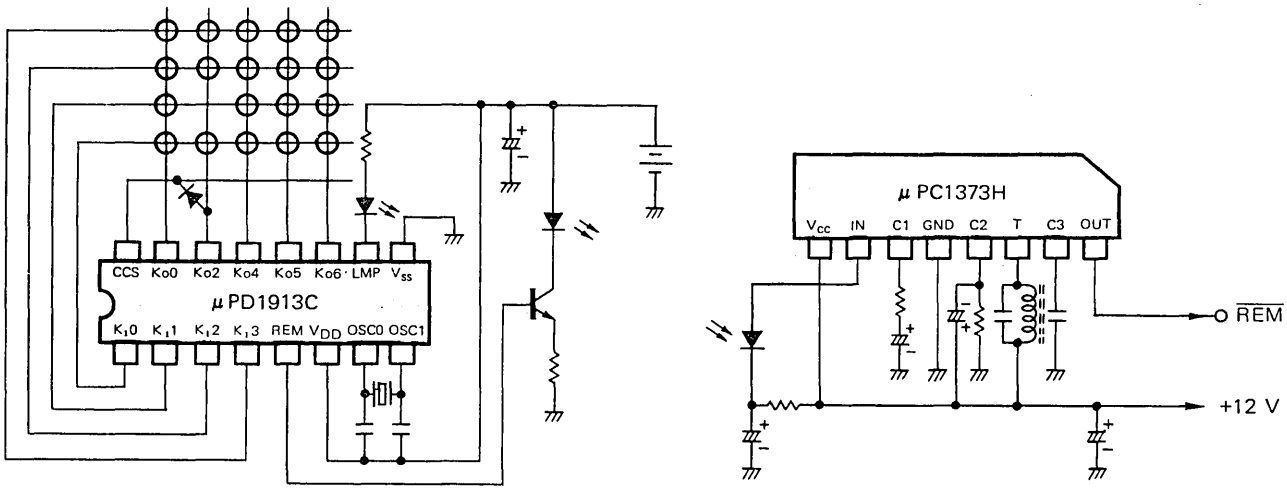
Note : When the μPD1705C-012 receives remote control signal the reception identification pulse of about 20 ms is issued from LMP terminal. Use this pulse externally with some external time constnat.

Note : The custom code of C0 – C7 = 00100000 is used for transmission. The function does not start with codes other than this. For details of custom code, see the catalogue for μPD1913C.

*COMPOSITION OF KEYS AT THE μPD1913C

	KI0 (1)	KI1 (2)	KI2 (3)	KI3 (4)
KO0 (15)	CHU	CHD	VOLU	VOLD
KO2 (14)	POWER	MUTE	MUTE	PL
KO4 (13)	0	1	2	3
KO5 (12)	4	5	6	7
KO6 (11)	8	9	CLEAR	RECALL

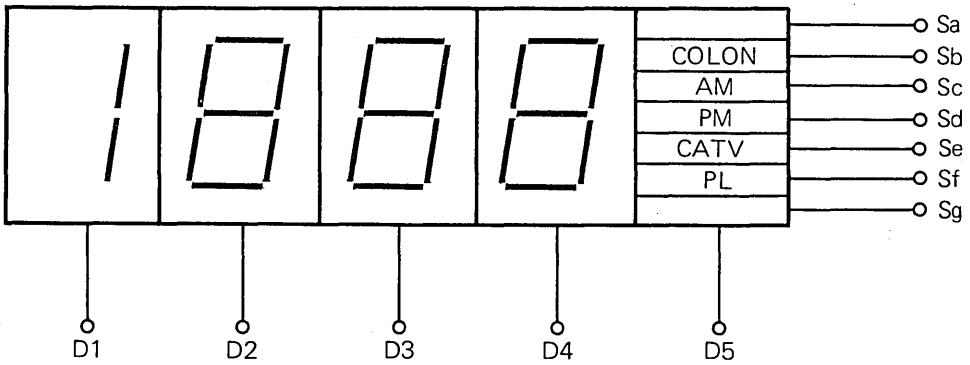
APPLICATION OF REMOTE CONTROL SYSTEM



DISPLAY FORMAT

Display format is 7-segment 5-digit dynamic display. (repetition frequency: 130 Hz and duty ratio: 15 %)

Display is connected in the following fashion.



CLOCK DISPLAY

Clock is displayed in 4 digits of numerics and 1 digit of dot (AM or PM, COLON, and PL).

CHANNEL DISPLAY

Channel is displayed in 2 digits of numerics and 1 digit of dot (CATV and PL). The digit of ten is displayed at D_3 timing and the digit of one at D4 timing.

Note : Channel and clock are alternatingly displayed by operating RECALL key. When power line is connected or when power switch is turned off, clock is displayed. Whereas, when power switch is turned on or when selection key (0–9, CHU, CHD) or CATV/TV switch is operated, channel is displayed. Furthermore, when clock adjustment switch (CLOCK, ONTIM, and OFTIM) is on, clock is displayed.

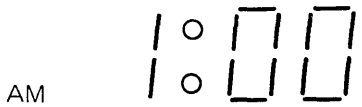
OPERATION OF CLOCK AND TIMER

CLOCK

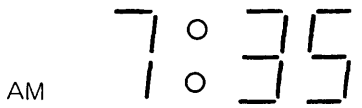
Clock should be adjusted following the schedule below.

1) Turn CLOCK switch on. Only clock is displayed. When no adjustment is done before, only AM and COLON are displayed.

2) Press HADJ key to adjust hour. The display of AM1:00 appears at the moment of key depression. The display continues to advance until the key is released.



3) Press MADJ key to adjust minute. The displayed minute continues to advance until the key is released. No counting up occurs in hour if the minute reaches 60.



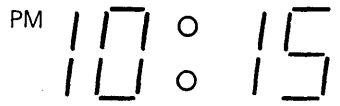
4) Turn CLOCK switch off coincidentally with other clock or time signal. The clock starts from 0 second at the moment of switch off.

TIMER

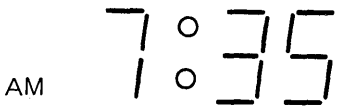
Adjust timer according to the following procedure.

1) Turn ONTIM (OFTIM) switch on. Timer is displayed.

2) Adjust timer to the desired time in the same procedure as clock adjustment.



3) Turn ONTIM (OFTIM) switch off. The display is changed to clock.



4) Turn TIMER switch on.

Note : During panel lock, clock cannot be adjusted. But when CLOCK switch is turned on/off, clock is reset to 0 second.

Note : When both on-timer and off-timer are set to the same time, off-timer is dominating.

Note : While CLOCK switch is on, clock does not advance.

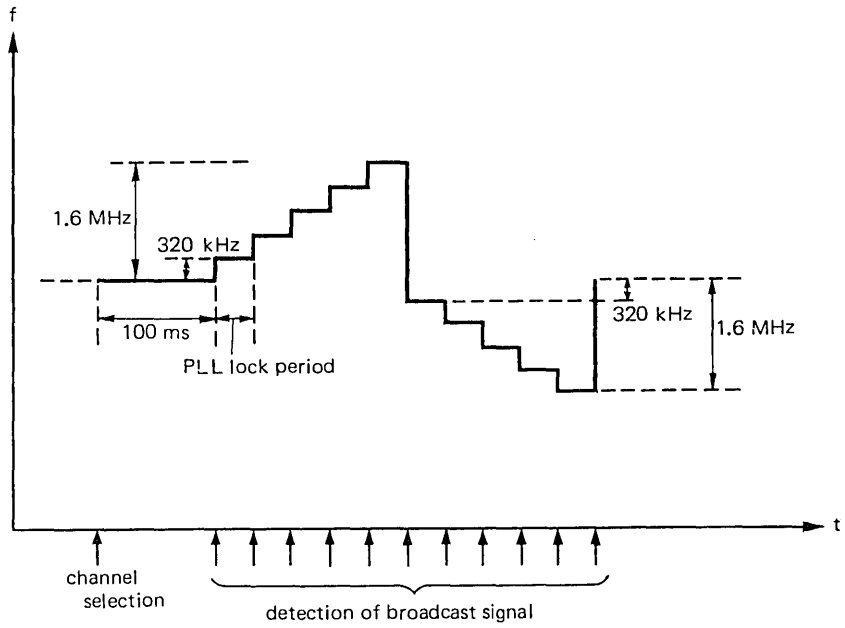
Note : While one of time adjustment switches is on, remote control is ineffective.

Note : Do not turn on two or more time adjustment switches at a time.

AUTO-SEARCH FUNCTION

μPD1705C-012 is provided for channel selection with a function to tune in automatically to a transmitting station by detecting the presence of the wave (when in auto mode). The searching of channels are performed in an specified derection (up-channel for up-channel selection, or down-channel for down-channel selection), or, in up-channel direction when direct selection is performed.

If there were a deviation in the frequency of wave transmitted by a station, the reception of signal at the right frequency might be impossible. In such cases, the receiving frequency is shifted by 320 kHz as far as ±1.6 MHz to be tuned in the transmitted signal. When a signal is detected half ways, the searching is finished. When the detection is not completed in ±1.6 MHz range, the next channel will be sought. The searching procedure within a channel is shown in the following figure.



FINE TUNING

μPD1705C-012 has a high precision fine tuning function to correspond to frequency shift of station. In virtue of this feature, the shift in receiving frequency can be easily compensated to keep the optimum receiving condition. Two types of fine tuning functions are available; manual (MFT) and auto (AFT).

1) MFT (manual fine tuning)

This tuning is operated with FTU or FTD key. Selection of another channel resets the fine tuning status. FTU and FTD keys are effective only when AUT/MAN switch is off (in manual mode). The fine tuning is done in 40 kHz step at every 125 ms and the limit of frequency shift is ±2.2 MHz.

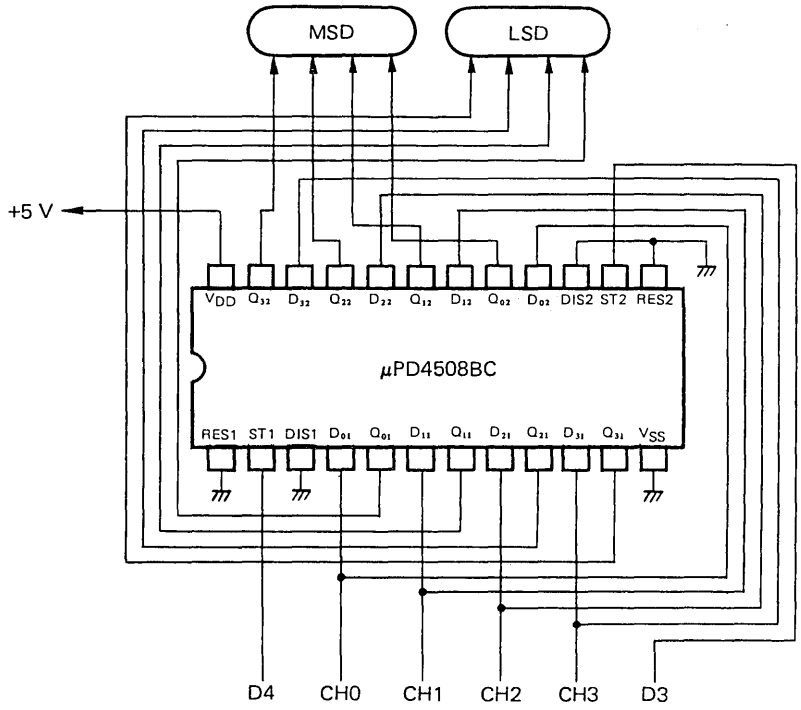
2) AFT (auto fine tuning)

It is effective only when AUT/MAN switch is on (in auto mode). This is operated by external AFT signal and it always follows the change in AFT signal. However, it is ineffective during channel selection. The fine tuning is done in 40 kHz step at every 8 ms and the limit of frequency change is ±2.2 MHz. AFT is operated by the signal applied to AFTU or AFTD terminal. When AFTU terminal is at high level, the tuning frequency is raised, while AFTD terminal is at high level, the frequency is lowered. When both AFTU and AFTD terminals are assigned with low level, the operation is stopped.

Note : In either AFT or MFT, when the frequency is shifted as far as the upper or lower limit respectively, the frequency is shifted back to the lower or upper limit. Thus the fine tuning is continued cyclically.

CRT DISPLAY

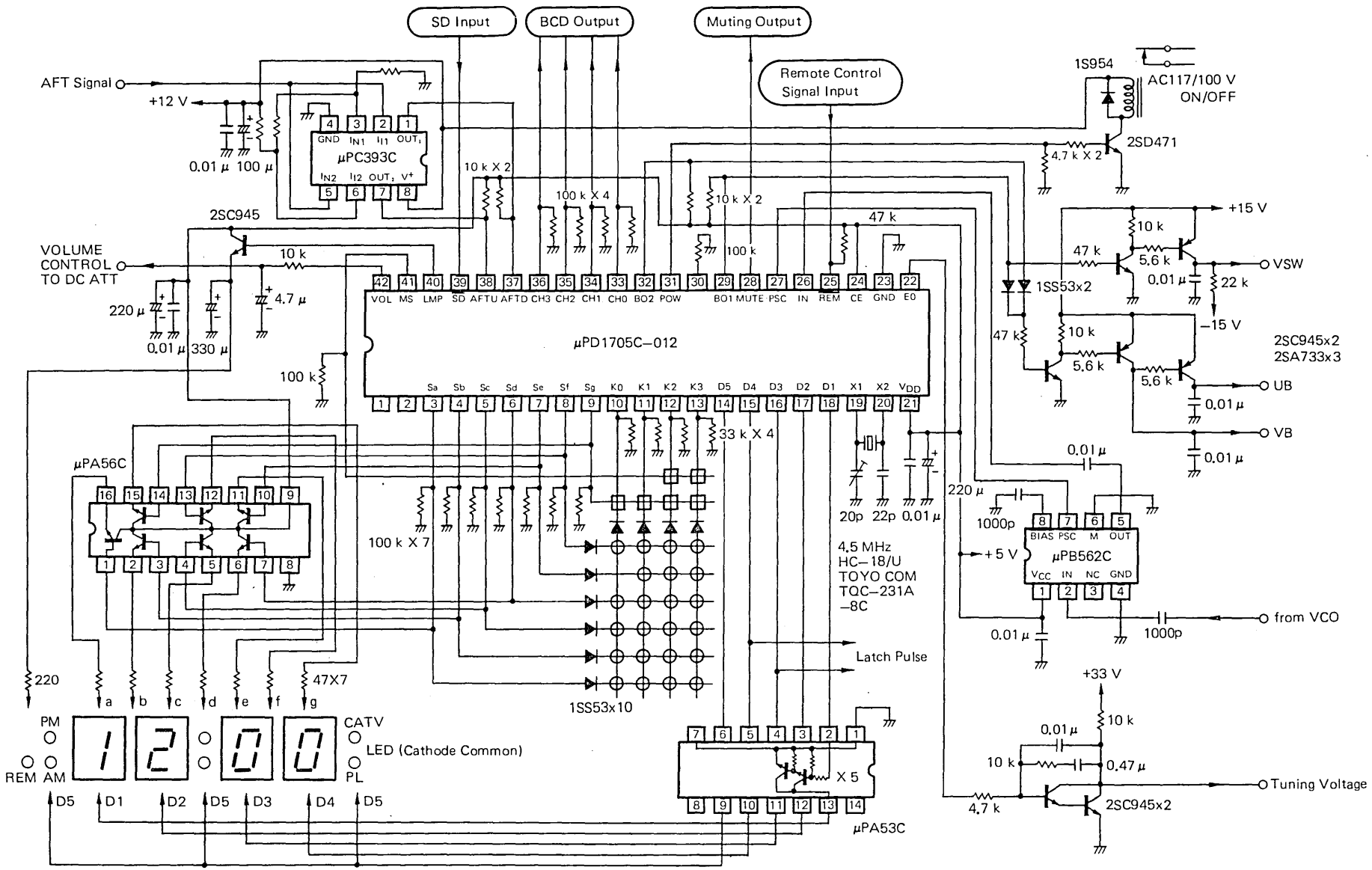
μPD1705C-012 is provided with terminals (CH0–CH3) for output of BCD channel number for CRT display. This output is presented in dynamic format which is the same as the display format (that is, digit of 10 is output at the timing of D3 and digit of 1 is output at the timing of D4). Therefore, by providing a latch (μPD4508BC) externally, the output can be taken outside.



OUTPUT PATTERN

numeric	BCD output
0	0 0 0 0
1	0 0 0 1
2	0 0 1 0
3	0 0 1 1
4	0 1 0 0
5	0 1 0 1
6	0 1 1 0
7	0 1 1 1
8	1 0 0 0
9	1 0 0 1
	1 1 1 1

APPLICATION CIRCUIT



MOS DIGITAL INTEGRATED CIRCUIT
μPD1706G-011

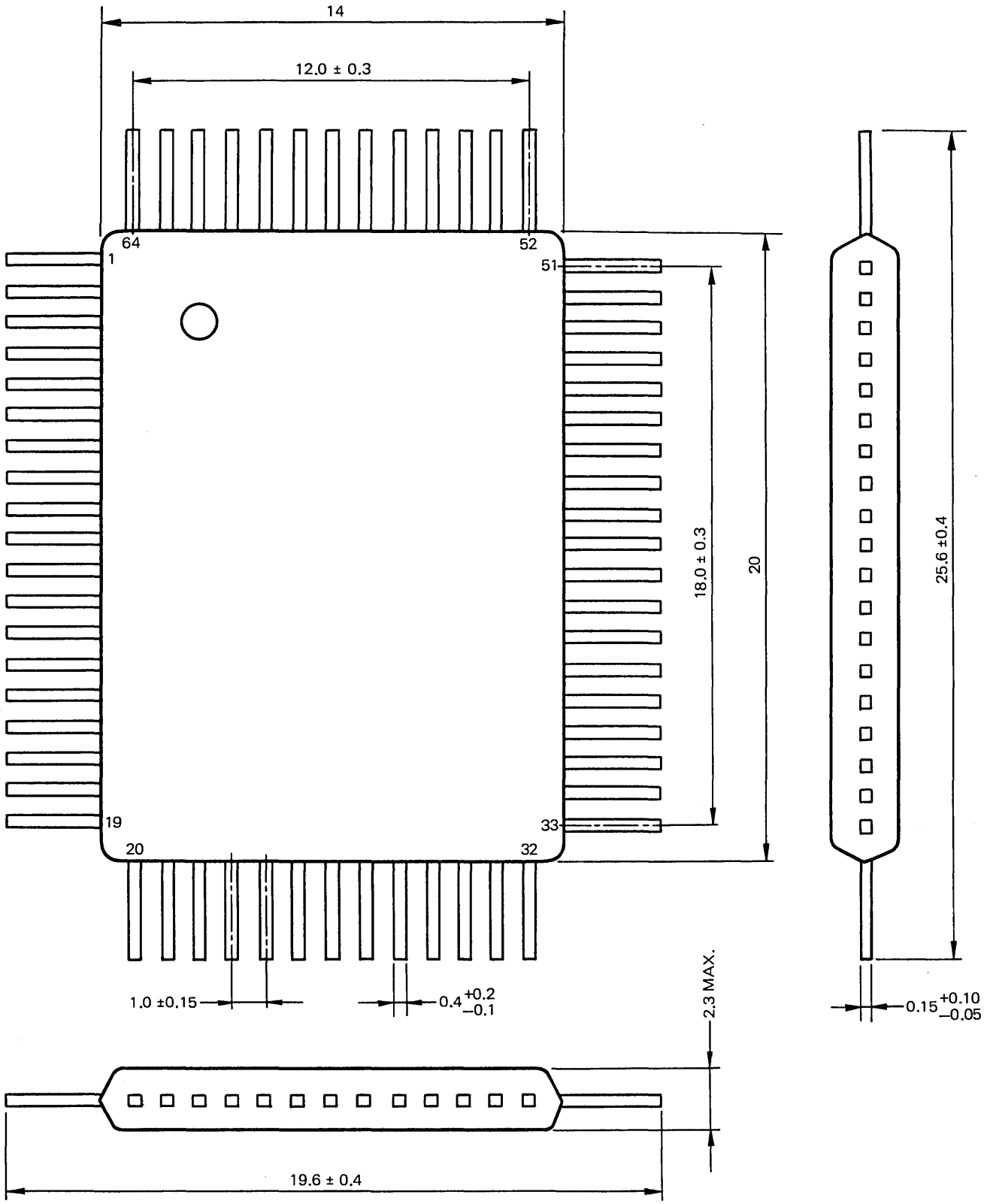
PLL SYNTHESIZER CONTROLLER FOR LW/MW/FM/SW
with built-in LCD driver

The μPD1706G-011 is a 6-band (LW/MW/FM/SW1/SW2/SW3) PLL synthesizer controller with a timer, developed specifically for use in radio cassettes intended for Japan/U.S./Europe. Since it has a built-in LCD driver for display, LCD (Liquid Crystal Display) can be directly driven. By combining it with a low voltage drive prescaler μPB556C designed for the purpose, therefore, you can build a low-voltage, low-power-consumption LCD drive digital tuning system.

FEATURES

- PLL and controller in a chip
- LCD direct drive (1/3 duty, 1/3 bias)
- Single 3 V ±10 % supply
- Low power consumption: due to CMOS
- Capable of receiving six bands (LW/MW/FM/SW1/SW2/SW3)
- Pulse swallowing method (FM/SW2/SW3)
- Capable of controlling radio cassette (with radio/tape switching terminal)
- Main power control terminal provided
- Power on reset circuit self-contained (no external parts required)
- Clock function self-contained (12 hour/24 hour display switching possible)
- Alarm timer self-contained (buzzer modulation signal output possible: 3 kHz + 4 Hz + 0.5 Hz modulation)
- Sleep timer self-contained (60 minutes maximum . . . Time can be set in the unit of five minutes.)
- A variety of tuning modes
  - ★ Manual up/down search (saw-tooth mode): 125 ms/1ch., 125 ms/10ch.
  - ★ Automatic up/down search (saw-tooth mode): 60 ms/1ch.
  - ★ Preset channel tuning: Random preset system
  - ★ Direct frequency tuning: With error display
- 10 preset channels can be stored in memory. (Random system)
- Last one memory (when power is OFF) and last preset channel memory (when bands are switched over) functions self-contained
- Uses 150 kHz crystal
- Uses 64-pin flat package which allows thinner assembly
- Allows IF offset of FM (four different IFs spaced 25 kHz apart).
- Employs quasi static key scan system (no key scan noise generated).
- All output terminals N-ch open drain (breakdown voltage 8.5 V MIN.) (except KS_0 through KS_9, $E0_1$, $E0_2$, PSC, COM0 through 2, 1a through 9a)

PACKAGE DIMENSIONS (Unit: mm)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{DD}	−0.3 to +6.0	V
Input Voltage	V_I	−0.3 to V_{DD}	V
Output Voltage	V_O	+10.5 ($\overline{SW1S}$,$\overline{SW2S}$,$\overline{SW3S}$,$\overline{FMS}$, $\overline{MWS}$,$\overline{LWS}$,MUTE,$\overline{PWROUT}$ PLS terminal)	V
Output Current	I_O	10	mA
Operation Temperature	T_{opt}	−35 to +75	°C
Storage Temperature	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (Test Condition unless otherwise specified: T_{opt}=−35 ~ +75 °C, V_{DD}=2.55~3.3 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Supply Voltage	V_{DD1}	2.7	3.0	3.3	V	CPU and PLL operation
Supply Voltage	V_{DD2}	2.55	3.0	3.3	V	CPU operation, PLL stop
Supply Current	I_{DD1}		2.0		mA	FM terminal 8.5 MHz input
Supply Current	I_{DD2}		8.5		μA	CPU operation, PLL stop
Supply Voltage Rise Time	t_r			100	ms	
Oscilation Start Voltage	V_{DOS}	2.7			V	C_L=20 pFx2
Output Breakdown Voltage	V_O	8.5			V	$\overline{SW1S}$, $\overline{SW2S}$, $\overline{SW3S}$, $\overline{FMS}$, $\overline{MWS}$, $\overline{LWS}$, MUTE, $\overline{PWROUT}$, BUZ terminal
Low Level Output Current	I_{OL2}			0.6	mA	" (V_{OL}=0.5 V)
High Level Output Voltage	V_{OH1}	V_{DD}−0.4			V	KS_8, KS_9 terminal (I_{OH}=−400 μA)
Low Level Output Voltage	V_{OL1}			0.4	V	" (I_{OL}=400 μA)
High Level Input Voltage	V_{IH1}	0.7 V_{DD}			V	" CE terminal
Low Level Input Voltage	V_{IL1}			0.3 V_{DD}	V	" "
High Level Output Current	I_{OH2}	1.0			mA	EO_1, EO_2, terminal(V_{OH}=0.6V_{DD})
Low Level Output Current	I_{OL2}			−1.0	mA	" (V_{OL}=0.4 V_{DD})
High Level Output Voltage	V_{OH4}	V_{DD}−0.4			V	KS_0~KS_7 (I_{OH}=−200 μA)
Low Level Output Voltage	V_{OL4}			0.5	V	" (I_{OL}=8 μA)
High Level Input Voltage	V_{IH4}	0.6 V_{DD}			V	K_0~K_3
Low Level Input Voltage	V_{IL4}			0.2 V_{DD}	V	"
High Level Input Current	I_{IL4}	6		40	μA	" (V_{DD}=V_{IH}=3.3 V)
High Level Input Voltage	V_{IH5}	0.8 V_{DD}			V	SD terminal
Low Level Input Voltage	V_{IL5}			0.2 V_{DD}	V	"
High Level Output Voltage	V_{OH6}	0.8 V_{DD}			V	PSC terminal (I_{OH}=−0.1 mA)
Low Level Output Voltage	VOL6			0.2 V_{DD}	V	" (I_{OL}=0.2 mA)
AM Response Frequency	f_{AM}	0.5		6.2	MHz	V_{IN}= 1 V_{P-P} sine wave (DC cut)
FM Response Frequency	f_{FM}	0.5		8.5	MHz	V_{IN}=0.8 V_{p-p} sine wave (DC cut)
Output Off Leak Current	$\|I_L\|$		10^{-3}	1	μA	EO_1, EO_2, terminal
Output Voltage for LCD	V_O	0		0.2	V	1a~9a,COM0~2 terminal(V_{DD}=3 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Output Voltage for LCD	V_1	0.8	1.0	1.2	V	1a~9a, COM0~2 terminal (V_{DD}=3 V)
"	V_2	1.8	2.0	2.2	V	"
"	V_3	2.8		3.0	V	"
Pull-down Current	I_{PD1}		400		μA	AM,FM terminal (V_{DD}=V_{IH}=3.0 V)
"	I_{PD2}		300		μA	XI terminal (")
High Level Input Current	I_{IH1}		2		μA	AM, FM terminal (")
Low Level Input Current	I_{IL1}		−2		μA	"

1. GENERAL DESCRIPTION OF FUNCTIONS

1-1. Receiving frequencies

Band	Receiving Frequency Range	Channel Spacing	Reference Frequency	Intermediate Frequency
LW	153~281 kHz	1 kHz	1 kHz	450 kHz
MW	522~1611 kHz	9 kHz	3 kHz	450 kHz
	530~1610 kHz	10 kHz	5 kHz	
FM	87.5~108.0 MHz	200 kHz	25 kHz	(Note) 10.650, 10.655, 10.700, 10.725 MHz
		50 kHz		
	76.1~108.0 MHz	50 kHz		(Note) −10.675, −10.700, −10.725, −10.750 MHz
SW1	2.300~2.935 MHz	5 kHz	5 kHz	450 kHz
	2.940~3.575 MHz			
	3.580~4.215 MHz			
	4.540~5.175 MHz			
SW2	5.820~6.455 MHz			
	7.100~7.735 MHz			
	9.500~10.135 MHz			
	11.580~12.215 MHz			
SW3	15.100~15.735 MHz			
	17.500~18.135 MHz			
	21.340~21.975 MHz			
	25.500~26.135 MHz			

Note) Selectable by diode matrix

(For details, see P. 11)

1-2. Tuning functions

(1) Automatic tuning (saw-tooth mode)

○Automatic up
○Automatic down
} .... Once a station is received, the station is retained.

(2) Manual tuning (saw-tooth mode)

○Manual up
○Manual down
} .....Step feed by momentary switch.
If key continues to be depressed for more than 0.5 sec., fast feed is made until key is released. If FAST key is doubly depressed, ultra fast feed is made.

(3) Direct frequency key in ..... Frequency is directly input by 10 keys.

(4) Preset memory call ..... Common to all bands, 10 stations in total

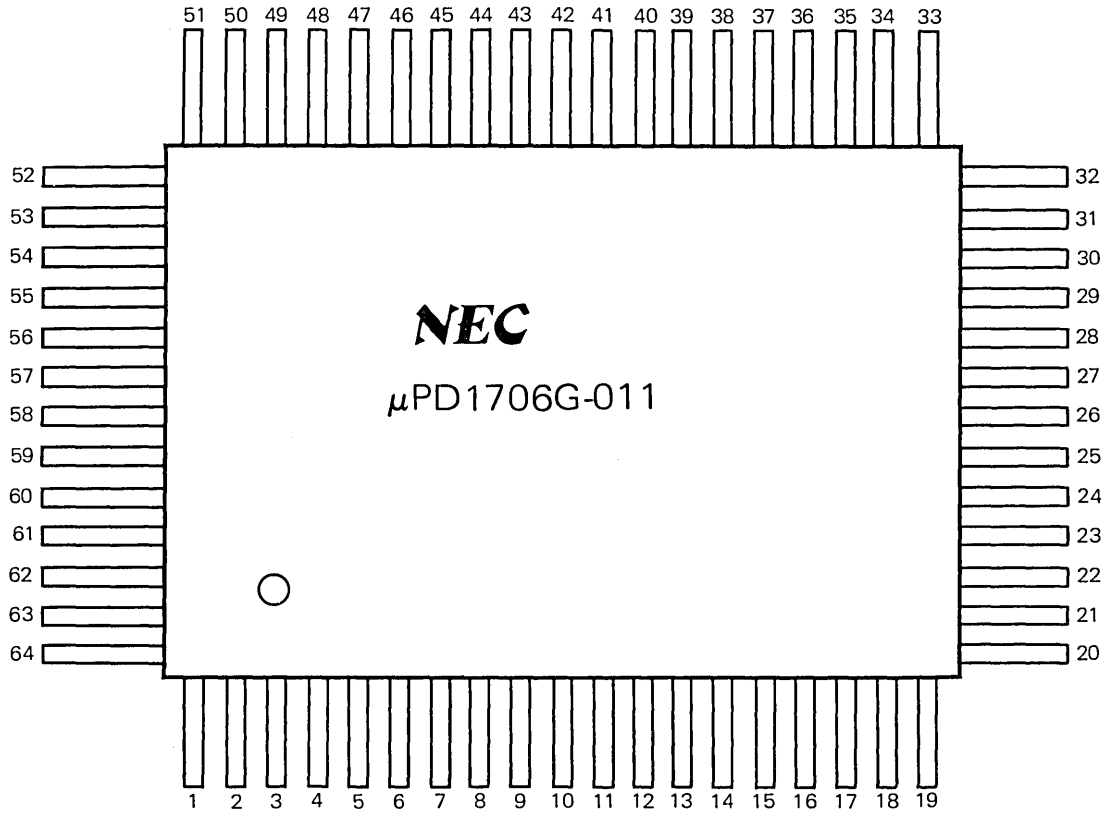
1-3. Timer functions

(1) Alarm ..... When preset time arrives, buzzer pulse is output. At the same time, power is turned on. The ON state lasts for 120 minutes, and then both are forced to the OFF state. (Daily timer)

(2) Sleep ..... Can be set to 60 minutes maximum five minutes apart.

2. PIN DESCRIPTION

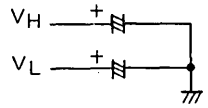
2-1. Pin Configuration (Top View)



Pin. No.	Symbol	Pin. No.	Symbol	Pin. No.	Symbol	Pin. No.	Symbol
1	NC	17	1c	33	$\overline{SW2S}$	49	XI
2	8a	18	1b	34	$\overline{SW3S}$	50	XO
3	7c	19	1a	35	$\overline{FMS}$	51	K_3
4	7a	20	7b	36	$\overline{MWS}$	52	K_2
5	6a	21	9a	37	$\overline{LWS}$	53	K_1
6	5c	22	V_L	38	MUTE	54	K_0
7	5b	23	V_H	39	$\overline{PWROUT}$	55	PSC
8	5a	24	COM2	40	BUZ	56	AM
9	3b	25	COM1	41	KS_0	57	FM
10	4c	26	V_{DD}	42	KS_1	58	V_{DD}
11	4b	27	COM0	43	KS_2	59	SD
12	4a	28	KS_9	44	KS_3	60	PWRIN
13	3a	29	KS_8	45	KS_4	61	TEST
14	2c	30	$T/\overline{R}$	46	KS_5	62	EO_1
15	2b	31	PWRSW	47	KS_6	63	EO_2
16	2a	32	$\overline{SW1S}$	48	KS_7	64	GND

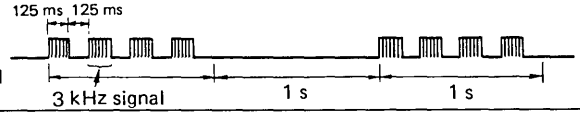
(NC : No Connection)

2-2. Pin Description

Pin No.	Symbol	Pin Name	Description
2~21	1a~9a	LCD SEGMENT SIGNAL	LCD segment signal output terminals (LCD of 1/3 duty and 1/3 bias to be used. See note.)
22 23	V_L V_H	Intermediate voltage output terminals for LCD	Of power voltages for LCD, intermediate ones are output to these pins. If these intermediate potentials do not stabilize when a large-size LCD is to be driven, connect large capacity capacitors between V_H, V_L and GND. Normally opened. 
24,25,27	COM0~2	LCD COMMON SIGNAL	LCD common signal output terminals
26 58	V_{DD}	POWER SUPPLY	Device power terminals 3 V±10 % voltage supplied when device is operated. Power can be supplied to either pin 26 or 58 only. V_{DD} rise time must be less than 100 ms (0 to 2.7 V). Extremely long rise time might result in failure of proper initialization. When V_{DD} does not fall completely to 0 V and rises again to 2.7 V, reset is not assured. In such a case, reset must be made from outside using PWRIN terminal.
28 29 41	KS_9 KS_8 KS_0	KEY RETURN SIGNAL SOURCE FOR ALTERNATE SWITCH	Key return signal source output terminals for initialization diode matrix on key mtarix and alternate switch. To input these outputs to terminals K_0 through K_3, make sure that diodes for prevention of counter flow are inserted. (Refer to Key Matrix Configuration of P. 713)
42~48	KS_1 ~ KS_7	KEY RETURN SIGNAL SOURCE FOR MOMENTARY SWITCH	Key return signal source output terminals for momentary switches on key matrix.
51~54	K_3 ~ K_0	KEY RETURN SIGNAL INPUT	Key return signal input pins for key matrix. (For details, refer to Key Matrix Configuration on P. 713)
30	$T/\overline{R}$	TAPE/RADIO SWITCHING INPUT	TAPE and RADIO switching signal input terminal. To be combined with TAPE/RADIO switch of set. Input as follows: When TAPE is selected: High level (PLL stopped, time displayed) When RADIO is selected: Low level (PLL operated, time or frequency displayed) $\overline{PWROUT}$ terminal should be directly connected when RADIO is selected. (For details, refer to Application on P. 737)

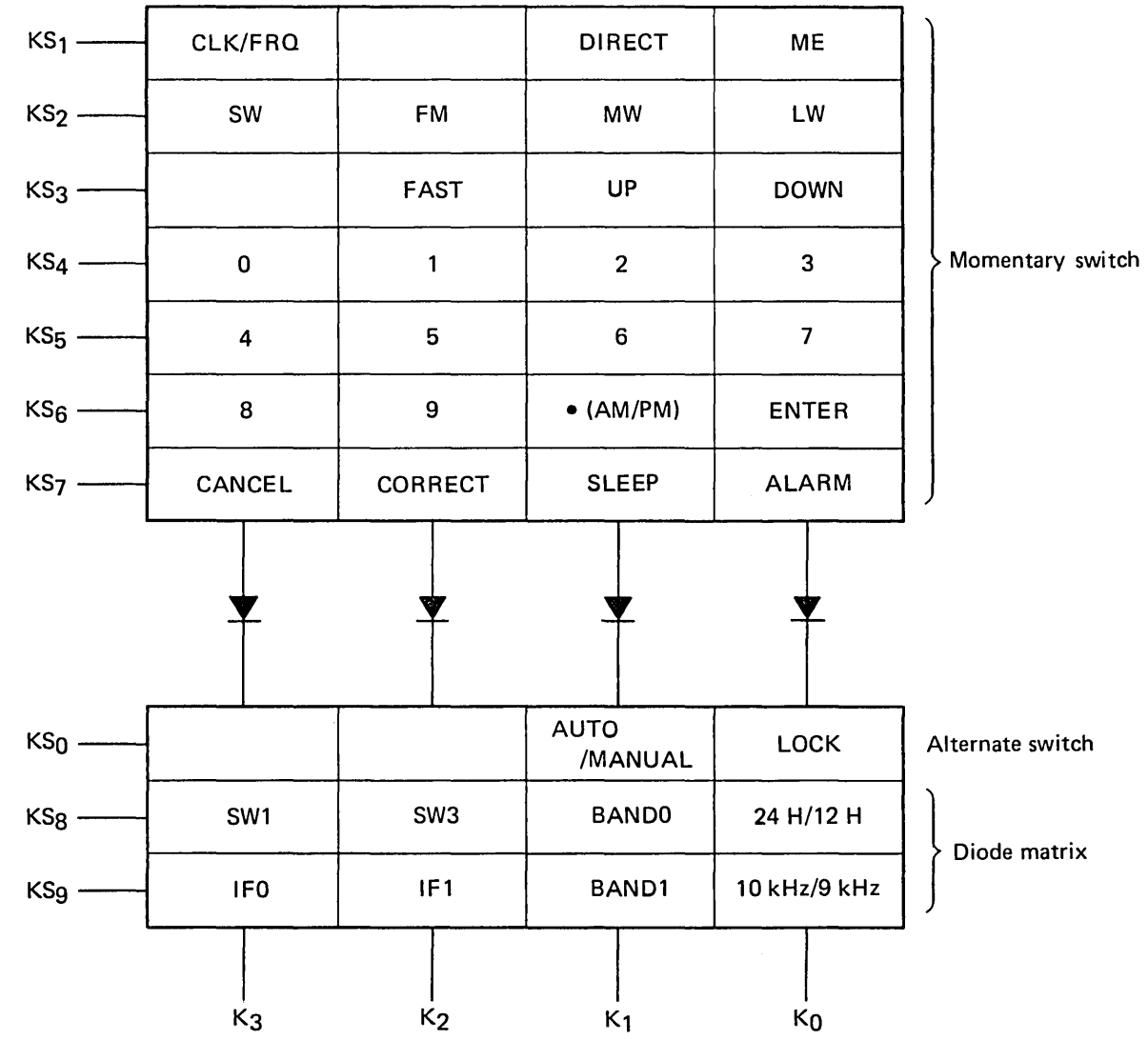
Note) Recommended LCDs:

- EPSON KT-104
- ALPS ELECTRIC CO., LTD. PAD32901
- HITACHI LTD. LP031-C

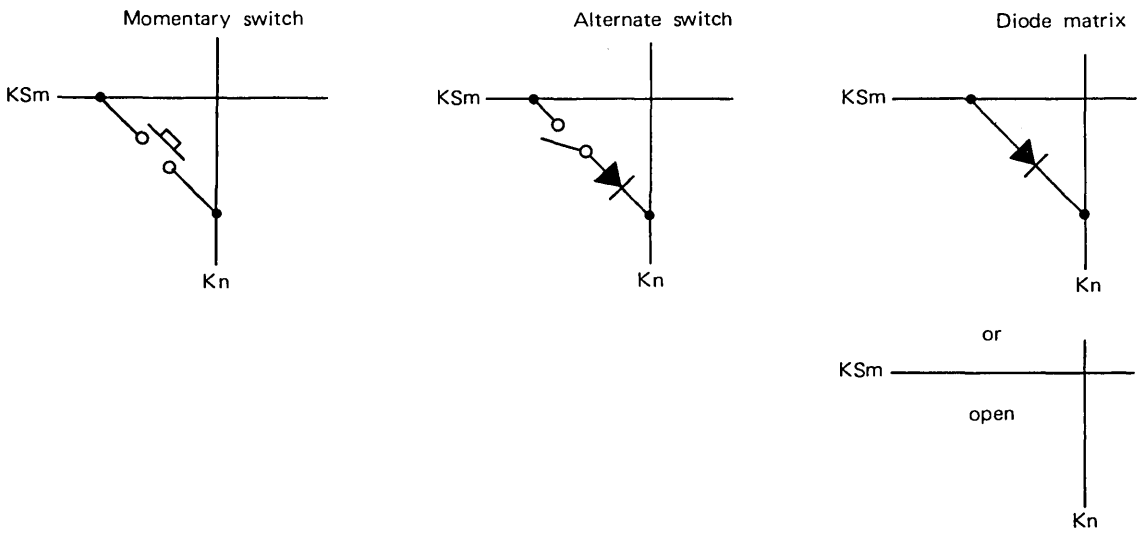
Pin No.	Symbol	Pin Name	Description
31	PWRSW	MAIN SWITCH ON/OFF REQUEST INPUT	Input pin for ON/OFF detection of main switch of set. When main power is to be turned on by $\overline{\text{PWROUT}}$ output, input high level. When it is to be turned off, input low level. When high level is input, low level is output to $\overline{\text{PWROUT}}$ terminal and PLL operates. When low level is input, high level is output to $\overline{\text{PWROUT}}$ terminal, and PLL stops (For details, refer to Application on P. 737.)
32 37	$\overline{\text{SW1S}}$ $\overline{\text{SW2S}}$ $\overline{\text{SW3S}}$ $\overline{\text{FMS}}$ $\overline{\text{MWS}}$ $\overline{\text{LWS}}$	VCO SELECT SIGNAL OUTPUT	VCO select signal output terminal, and active low output. Since it is N-channel open drain output, external pull-up resistor is required. Output breakdown voltage is 8.5 V maximum.
38	MUTE	MUTE OUTPUT	Muting signal output terminal for killing shock noise which may otherwise be produced when PLL is out of lock. Active high. Since it is N-channel open drain output, external pull-up resistor is required. Output breakdown voltage is 8.5 V max. For details of timing, refer to Mute Timing Chart on P. 732.
39	$\overline{\text{PWROUT}}$	MAIN POWER SWITCHING OUTPUT	Output terminal for ON/OFF switching signal of main power of set. Normally this terminal is used so that main power will be turned on when this terminal is low and turned off when this terminal is high. Since it is N-channel open drain output, external pull-up resistor is required. Output breakdown voltage is 8.5 V max. (For details, refer to Application on P. 737.) $\overline{\text{PWROUT}}$ terminal varies with the state of PWRIN terminal and condition of ALARM and SLEEP. When it varies, however, MUTE signal is always output at least 250 ms beforehand to minimize power ON/OFF shock noise.
40	BUZ	BUZZER OUTPUT	Buzzer modulation signal output terminal. Outputs 3 kHz signal modulated by 4 Hz and 0.5 Hz when ALARM is ON. (For details, refer to illustration shown below.) Since it is N-channel open drain output, pull-up resistor is required. 
49 50	XI XO	CRYSTAL	Crystal connection terminals. Connect 150 kHz crystal. Recommended crystals: • KYOTO CERAMICS KF-38Z • TOYO TSUSHINKI TQC-122A-7C • KINSEKI P3-150

Pin No.	Symbol	Pin Name	Description
55	PSC	PRESCALER CONTROL	Outputs signal for switching the frequency dividing ratio of prescaler (μPB556C) in modes (FM, SW2 or SW3) where pulse swallowing system is employed for frequency division. Connect this terminal to PSC terminal of the prescaler μPB556C. The dividing ratio of μPB556C is 1/16 and 1/17.
56	AM	VCO INPUT FOR LW, MW and SW1	Terminal for inputting LW, MW or SW1 local oscillation outputs. An AC amplifier is incorporated, and DC should be cut with a capacitor.
57	FM	VCO INPUT FOR SW2, SW3 and FM	Terminal for inputting FM, SW2 or SW3 local oscillation outputs frequency-divided into 1/16 and 1/17 by the prescaler μPB556C. An AC amplifier is incorporated, and DC should be cut with a capacitor.
59	SD	STATION DETECTOR	Terminal for inputting signal for detecting whether broadcast station has been received during automatic tuning (automatic up/down). High level should be input when a station is received. It must be input in less than 30 ms after frequency dividing ratio has changed. (Refer to P. 734)
60	PWRIN	MAIN POWER ON/OFF REQUEST INPUT	Input terminal for detecting main power ON/OFF of the set. Connect this terminal to main power. If this terminal is LOW, no alarm operation is performed. Avoid creating contradictory state where PWRSW terminal is HIGH and PWRPIN terminal is LOW. When reset is to be made using PWRIN terminal, input high level after it has been set LOW. This terminal however, does not accept pulses shorter than 140 μs. When reset is made using this terminal, state of diode switch at initialization is loaded.
61	TEST	DEVICE TEST TERMINAL	Device test terminal. Normally connected to GND.
62 63	EO_1 EO_2	ERROR OUT	Charge pump output of phase detector constituting PLL. If divided oscillation frequency is higher than reference frequency, these pins output high level. When it is lower, on the other hand, terminals output low level. If they coincide, the terminals enter floating state. Since EO_1 and EO_2 output same signal simultaneously, they may be connected to LPF (Low Pass Filter) of any of LW, MW, FM, SW1, SW2 or SW3.
64	GND	GROUND	Connect to GND of the set.

3. KEY MATRIX CONFIGURATION



Switch Connections



4. DESCRIPTION OF KEY MATRIX

4-1. Initialization Diode Matrix

Initialization diode matrices are of the following five kinds. All of them are loaded when power is applied to V_{DD} for the first time (at initialization) or when PWRIN changes from LOW to HIGH.

(1) Switch for setting IF offset values of FM

IF0 IF1

(2) Switch for setting FM band areas (the US., Europe, Japan)

BAND0 BAND1

(3) Switch for setting MW band channel spacing and reference frequency

10 kHz/9 kHz

(4) Switch for selecting SW bands

SW1, SW3

(5) Switch for selecting 12/24 hour systems of clock

24H/12H

These should be set by shorting or opening intersecting points on the matrix with diodes. (on the following table, "1" means shorting by Diode and "0" means opening.)

<table>
<tr><th>SWITCH</th><th>FUNCTION DESCRIPTION</th></tr>
<tr><td>IF1
IF0</td><td>Switches for setting IF offset values of FM.
Four different IFs spaced 25 kHz apart can be set without changing displayed frequencies.

<table>
<tr><th>IF1</th><th>IF0</th><th>U.S. band</th><th>European band</th><th>Japanese band</th></tr>
<tr><td>0</td><td>0</td><td>10.700 MHz</td><td>10.700 MHz</td><td>−10.700 MHz</td></tr>
<tr><td>0</td><td>1</td><td>10.725 MHz</td><td>10.725 MHz</td><td>−10.675 MHz</td></tr>
<tr><td>1</td><td>0</td><td>10.650 MHz</td><td>10.650 MHz</td><td>−10.750 MHz</td></tr>
<tr><td>1</td><td>1</td><td>10.675 MHz</td><td>10.675 MHz</td><td>−10.725 MHz</td></tr>
</table></td></tr>
<tr><td>BAND1
BAND0</td><td>Switches for setting FM band areas.
U.S., European or Japanese FM band can be selected.
<table>
<tr><th>BAND1</th><th>BAND0</th><th>Band area</th><th>Receiving frequency range</th><th>Channel spacing</th></tr>
<tr><td>0</td><td>0</td><td>Japanese band</td><td>76.10~108.00 MHz</td><td>50 kHz</td></tr>
<tr><td>0</td><td>1</td><td>European band</td><td>87.50~108.00 MHz</td><td>50 kHz</td></tr>
<tr><td>1</td><td>0</td><td>Inhibited*</td><td></td><td></td></tr>
<tr><td>1</td><td>1</td><td>U.S. band</td><td>87.5~107.9 MHz</td><td>200 kHz</td></tr>
</table>
* Do not set switches as shown, as correct band (area) cannot be set.</td></tr>
<tr><td>10 kHz/
9 kHz</td><td>Switch for setting MW band channel spacing, reference frequency and frequency range.
Can be set independently regardless of FM band areas (BAND1, BAND0).

<table>
<tr><th>10 kHz/9 kHz</th><th>Receiving frequency range</th><th>Channel spacing</th><th>Reference frequency</th></tr>
<tr><td>0</td><td>522~1611 kHz</td><td>9 kHz</td><td>3 kHz</td></tr>
<tr><td>1</td><td>530~1610 kHz</td><td>10 kHz</td><td>5 kHz</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Switch</th><th>Function Description</th></tr>
<tr><td>SW3
SW1</td><td>Switches for inhibiting receiving bands of SW bands.
<table>
<tr><th>SW3</th><th>SW1</th><th>Receiving band</th></tr>
<tr><td>0</td><td>0</td><td>SW1, SW2, SW3</td></tr>
<tr><td>0</td><td>1</td><td>SW2, SW3</td></tr>
<tr><td>1</td><td>0</td><td>SW1, SW2</td></tr>
<tr><td>1</td><td>1</td><td>SW2</td></tr>
</table></td></tr>
<tr><td>24H/12H</td><td>Switch for selecting 24/12 hour system.
<table>
<tr><th>24H/12H</th><th>Display</th></tr>
<tr><td>0</td><td>12-hour display (combined AM/PM display)</td></tr>
<tr><td>1</td><td>24-hour display</td></tr>
</table></td></tr>
</table>

4-2. Alternate Switches

The alternate switches are of the following two kinds. These are always switchable.

(1) Switch for switchover between automatic tuning and manual tuning

AUTO/MANUAL

(2) Switch for locking all switches on key matrix

LOCK

Switch	Function Description
AUTO/ MANUAL	Switch for switchover between automatic tuning and manual tuning. ON . . . Automatic tuning (automatic seek operation) OFF . . . Manual tuning Automatic and manual tuning operations are initiated by depressing the UP or DOWN momentary switch after setting AUTO/MANUAL switch. (For details, refer to Description of UP and DOWN keys on P. 716) Even if this switch is changed over to MANUAL during automatic tuning, tuning operation does not stop. To stop operation on switchover to MANUAL, compose the circuit so that high level will be input to SD terminal whenever switchover is made to MANUAL.
LOCK	To prevent accidentally changing receiving frequency or cutting off PWROUT output as during a recording, set this switch to ON, and all switch inputs on the key matrix will be inhibited. ON . . . Switch locked OFF . . . Normal operation

4-3. Momentary Switches

Symbol	Function Description
CLK/FRQ	Present time and frequency display switching key. This key is enabled only during the radio operating mode. When this key is pushed while present time display is ON, switchover is made to frequency display. When this key is pushed while frequency display is ON, switchover is made to current time display.
DIRECT	Key for setting direct frequency input mode. When this key is pushed during the radio operating mode, the direct frequency input mode is created, allowing a frequency to be directly keyed in by 10 keys and the set to be tuned in on the frequency. (For details, refer to Operating Procedures on P. 720)
ME	Use this key to write a new frequency to preset channel memory. This key is enabled only during the radio operating mode. Push any one of the 10 keys in less than five seconds after pushing this key, and the frequency being received at the moment can be preset to the preset channel memory corresponding to the key pushed. (For details, refer to the Operating Procedures on P. 725)
LW MW FM SW	Switches for selecting LW, MW, FM and SW bands. During the radio operating mode, push any one of these keys, and switchover will be made to the selected band. If there is a channel previously written to preset channel memory of the selected band, the set is tuned to the last received preset channel. If the preset channel memory has no written channel for the band, the set is tuned to the lowest channel of the band. (Refer to P. 725)
FAST	Ultra fast key for manual UP/DOWN. After the UP or DOWN key has been depressed during the radio reception, depress this key simultaneously, and ultra-fast operation of 125 ms/10ch will take place.
UP DOWN	Automatic and manual tuning keys. When these keys are pushed, the following operations will be performed. (1) AUTO/MANUAL switch in AUTO position Pushing the UP key will sustain up-tuning operation in sawtooth mode, whereas pushing the DOWN key will sustain down-tuning operation. If high level is input to SD terminal during the period, automatic tuning operation will stop. (2) AUTO/MANUAL switch in MANUAL position Each time the UP or DOWN key is pushed, up or down tuning to another channel a step (channel space) apart will be made. If the UP or DOWN key continues to be pushed for more than 0.5 second, up or down tuning will continue at a speed of 125 ms/1ch until the key is released. (Note) Even if the AUTO/MANUAL switch is changed over to MANUAL during automatic tuning, the automatic tuning operation does not stop. To stop the operation on switchover to MANUAL, compose the circuit so that high level will be input to SD terminal whenever switchover is made to MANUAL.

Symbol	Function Description
0 1 2 3 4 5 6 7 8 9	Numeric keys or preset channel memory write/call keys. (1) As numeric keys (10 keys) When the present time or alarm time is to be corrected, push the CORRECT key and then directly key in a desired time. In the direct frequency input mode, a desired frequency can be keyed in directly by these keys. (2) As preset channel memory keys During the radio operating mode these keys correspond to the preset channel memory on 1:1 basis. ○ To write In less than five seconds after ME key has been pushed, push any one of keys from 0 through 9, and a new channel will be written to memory corresponding to the key pushed. ○ To call When any one of the keys 0 through 9 is pushed during the radio operating mode,the channel corresponding to the key pushed will be called.
•(AM/PM)	Operates as decimal point key or AM/PM switching key. In the direct frequency input mode, this key operates as the decimal point key. When time is corrected during 12-hour display, the key operates as the AM/PM switching key.
ENTER	(1) Direct tuning After a channel has been directly keyed in by 10 keys, push this key, and the set will be tuned to this channel. (2) To correct present time and alarm time After a desired time has been directly keyed in by 10 keys, push this key, and the time will be set. In correcting the present time, correction will begin with 0 second when this key is pushed.
CANCEL	When this key is pushed during the direct tuning, present time correction or alarm time correction mode, the mode is cancelled. When this key is pushed during an alarm or sleep operation, the operation is cancelled.
CORRECT	Present time correction key. When this key is pushed while present time display is ON, the present time correction mode is created. In this case, the LCD presents "CORRECT" display, whereas flashing display of second stops.
SLEEP	Accepted only when PWRSW terminal is LOW and when ALARM is not ON. When this key is pushed while there is no "SLEEP" display on the LCD, the set enters the sleep state, and "SLEEP" display is presented. At this point, the sleep time is set to 60 minutes, and the $\overline{\text{PWROUT}}$ output will be forced to the OFF state 60 minutes later. This key can also be used to check the remaining sleep time. When the key is pushed, the remaining time (in minutes) will be displayed on the LCD. When the SLEEP key is pushed while the sleep time is being displayed on the LCD, the sleep time is reduced by five minutes.
ALARM	When this key is pushed, the alarm time is displayed. Alarm time correction can be made by depressing 10 keys or AM/PM key while the alarm time is on display. The time on display is set when the ENTER key is pushed. When the alarm time arrives while "ALARM" display is ON, the $\overline{\text{PWROUT}}$ and BUZ terminals are caused to be ON. To put out the "ALARM" display, push the ALARM key and then push the CANCEL key.

5. CONTROL TERMINALS

By terminals PWRIN, PWRSW, $\overline{\text{PWROUT}}$ and T/$\overline{\text{R}}$, modes are set as shown below.

(In the following table, 0 denotes low level, 1 denotes high level, and X denotes low or high level.)

PWRIN	PWRSW	$\overline{\text{PWROUT}}$	T/$\overline{\text{R}}$	Mode		Display (Note 1)
X	0	0	0	Power ON through alarm or sleep operation	RADIO	FREQ.(Note 2)/TIME
X	0	0	1		TAPE	TIME
X	0	1	0	Inhibited (When PWRSW is LOW, T/$\overline{\text{R}}$ must always be HIGH.)		
X	0	1	1	Power OFF for both RADIO and TAPE		TIME
1	1	0	0	Normal operation	RADIO	FREQ.(Note 3)/TIME
1	1	0	1		TAPE	TIME
1	1	1	0	Impossible modes (when high level is input to PWRSW pin, $\overline{\text{PWROUT}}$ pin always outputs low level. When PWRIN pin is LOW, do not input high level to PWRSW.)		
1	1	1	1			
0	1	X	X			

(Note 1) FREQ. and TIME displays mean the following displays.

TIME: Display of time (present time, alarm time, sleep time)

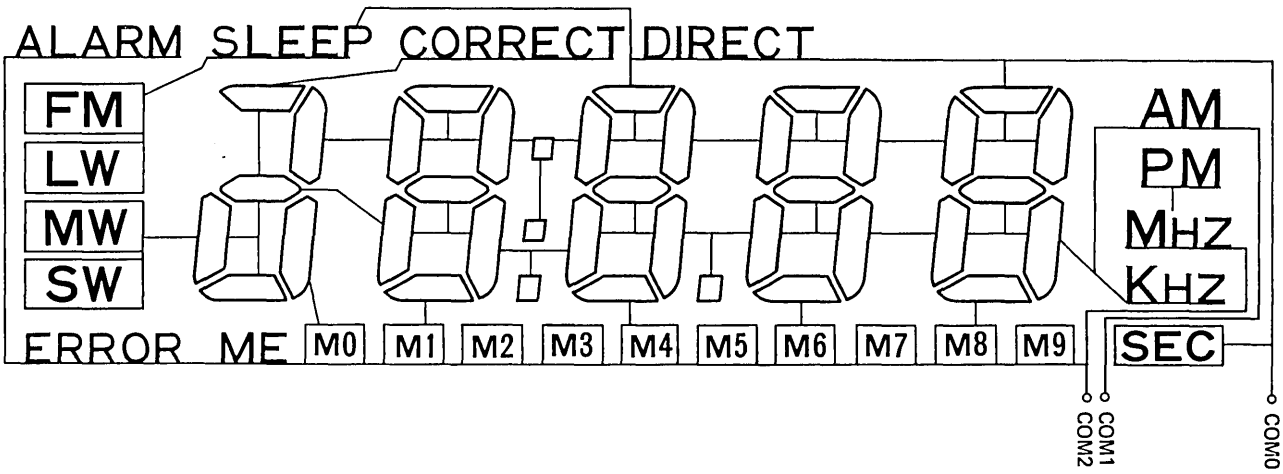
FREQ./TIME: Display of above-mentioned time or receiving frequency

(Note 2) In alarm or sleep mode, time display is given priority. For example, when the radio is turned on in the alarm or sleep mode, the channel will be displayed for the first five seconds only and the time displayed thereafter. When the CLK/FRQ key is pushed while the time display is ON after the radio has been turned on, the channel will be displayed for five seconds only and the time displayed thereafter.

(Note 3) In the normal operating mode where the timer is not used, the channel will be displayed while the radio is ON, and the time displayed during other modes. If the CLK/FREQ key is pushed while the radio is ON, the display will change to time display. The time display will be retained until other keyes or switches are operated.

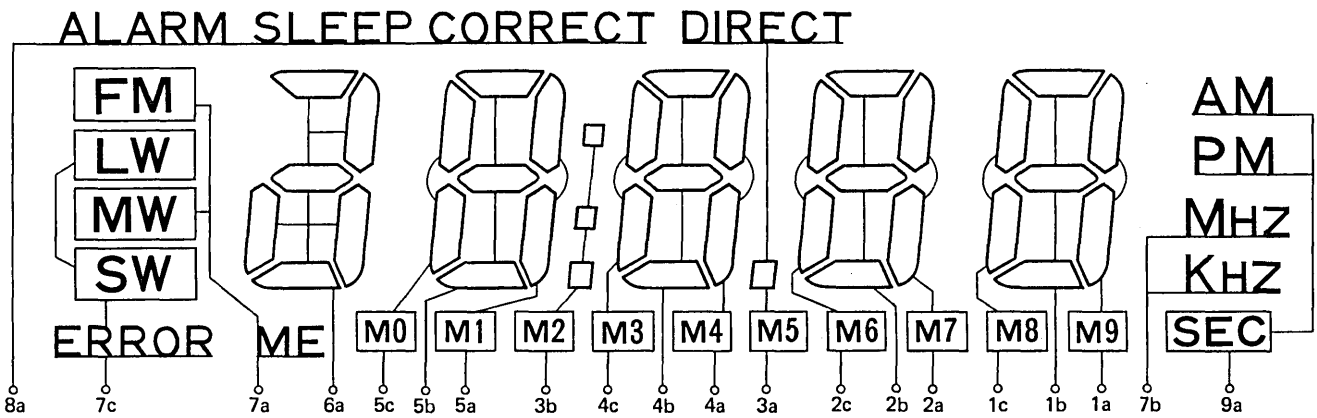
6. LCD PATTERN

COMMON LINES



LCD PATTERN

SEGMENT LINES



7. OPERATING PROCEDURES

7-1. Station selection

1. Manual Up/Down

Set the AUTO/MANUAL switch to MANUAL and depress the UP key or the DOWN key.

Continue the depression for more than 0.5 second, and the UP or DOWN operation occurs at a speed of 125 ms/1ch or so (Fast feed).

At this time, the MUTE of about 60 ms is output by each 1 ch of up or down operation, while no output is given for the remaining 60 ms. (Intermittent MUTE)(See the description on P. 30.)

Depress the UP or DOWN key and the FAST key at the same time, and the up or the down operation is executed at a speed of 125 ms/10ch. (Ultra fast feed)

While the ultra rapid feed is under way, the MUTE is being continually output. Release the FAST key, and the operation of fast feed is restored. If you release the UP or the DOWN key while depressing the FAST key, the UP/DOWN operation stops.

2. Auto Up/Down

Depress the UP or the DOWN key while the AUTO/MANUAL switch is set to AUTO, and the frequency shifts to the UP or the DOWN direction by 1 channel stepwise and whether input (high level) is fed to the SD terminal or not is checked. If there is input, the shift stops at that frequency. If no input is fed, the frequency continues to shift stepwise.

While automatic scanning is under way, the MUTE output continues to be fed. (As to detailed timing, refer to the description on P. 31)

To stop the automatic scanning half-way, depress the UP key, the DOWN key, or the FAST key.

3. Direct station selection

The frequency to be tuned may be directly input by 10 key. Depress the DIRECT key while the radio is on, then "DIRECT" is displayed showing that direct station selection can be accepted. Next, input the desired frequency within the existing band range by the 10 key and the decimal point key. Fianlly, depress the ENTER key, and the set will be tuned to that frequency.

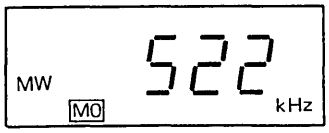
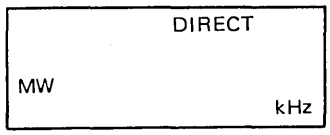
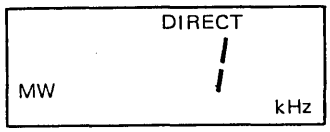
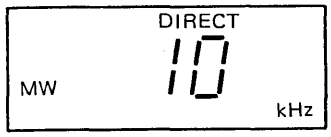
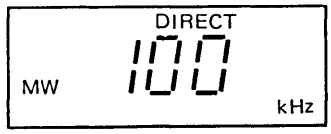
In case the input frequency is outside the existing frequency band, "ERROR" is displayed for 5 seconds. Thereafter the frequency to which the circuit was tuned before the DIRECT key was depressed will be restored. In case, further, the input frequency does not coincide with the channel frequencies within the existing frequency band, then tuning is made to the frequency of a channel just below the desired frequency.

During the time from depression of the direct key till depression of the ENTER key is depressed, and while "ERROR" is being displayed, the radio will continue to be tuned to the frequency received just before the direct key is depressed.

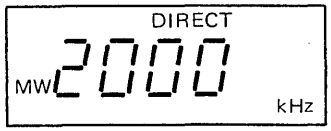
To cancel the direct station selection after depressing the DIRECT key and before depressing the ENTER key, simply depress the CANCEL key.

In case, further, you realized an error in the input frequency before depressing the ENTER key, then depress the DIRECT key for a second time. By doing so, exactly the same state as when you first depressed the direct key is restored. Thereafter, you may repeat the input of the correct frequency.

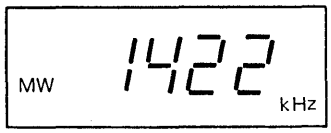
EXAMPLE 1) Correct station selection of MW band (Japan)

Key	Display	Frequency being received	Description
		522 kHz	The preset 0 ch is being received.
DIRECT		522 kHz	The direct station selection is started. The frequency display goes out and "DIRECT" is displayed instead.
1		522 kHz	Optional frequency is input by 10 key. The frequency is displayed at the right-hand end.
0		522 kHz	Id
0		522 kHz	Id.
8		522 kHz	Id.
ENTER		1008 kHz	"DIRECT" display goes out and the circuit is tuned to 1008 kHz. The display is shifted to the right by one unit.

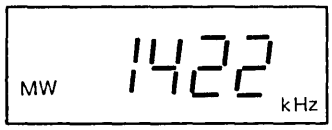
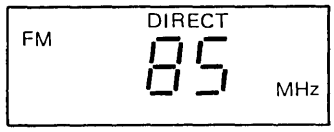
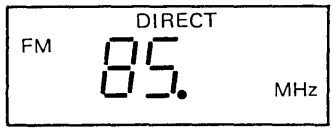
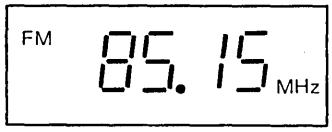
EXAMPLE 2) A frequency outside the MW (Japan) band is input

Key	Display	Frequency being received	Description
		1008 kHz	1008 kHz is being received.
DIRECT 2 0 0 0		1008 kHz	You would like to have the circuit tuned to 2000 kHz by direct station selection.
ENTER		1008 kHz	2000 kHz is outside the MW band. So, "ERROR" is displayed.
(5 seconds after)		1008 kHz	The original frequency of 1008 kHz is displayed after 5 seconds.

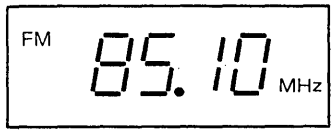
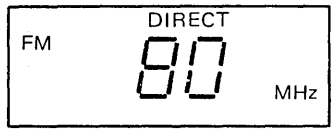
EXAMPLE 3) A frequency other than the channel frequencies in the MW (Japan) band is input

Key	Display	Frequency being received	Description
		1008 kHz	1008 kHz is being received.
DIRECT 1 4 2 5		1008 kHz	You would like to have the circuit tuned to 1425 kHz by direct station selection.
ENTER		1008 kHz	1425 kHz does not coincide with the channel frequencies. So, the circuit is tuned to 1422 kHz which is obtained by disregarding the lowest unit.

EXAMPLE 4) Correct station selection within the FM (Japan) band (Fraction of unit are input)

Key	Display	Frequency being received	Description
		1422 kHz	1422 kHz in MW frequency band is being received.
FM		80 MHz	Band is changed over, cH 5 has been preset on the last preset memory of FM band.
DIRECT 8 5		80 MHz	You would like to have the circuit tuned to 85.15 MHz by direct station selection.
•		80 MHz	Input the decimal point, and the display is shifted to the left.
1 5		80 MHz	The fractional units are input one after another beginning from the tenth unit. After two fractional units are fed, the 10 Key is rejected.
ENTER		85.15 MHz	"Direct" display goes out, and the circuit is tuned to 85.15 MHz.

EXAMPLE 5) Correct station selection within FM (Japan) band (in case fractional units are not fed)

Key	Display	Frequency being received	Description
		85.1 MHz	85.1 MHz within the FM band is being received.
DIRECT 8 0		85.1 MHz	You would like to have the circuit tuned to 80 MHz by direct station selection.
ENTER		80 MHz	"DIRECT" display goes out, and the decimal point and "00" are indicated at the fractional units and the tuning is made to 80 MHz.

(Caution) With regard to the FM and SW bands, the fractional units of the frequencies are displayed together with the decimal point in terms of MHz.
In respect of the LW and MW bands, the frequencies are displayed in terms of kHz without the indication of fractional units. So, the decimal point key is rejected when you are selecting a frequency.

4. Preset channel

The preset channel is based upon random preset system, and a total of 10 stations can be preset. Each of the 10 keys 0~9 corresponds to each of the memories.

○ How to preset

Depress the ME key while the frequency is being displayed, and "ME" is shown. After about 5 seconds, the "ME" indication goes out and the original state is restored. Depress one of the keys 0~9 as required while the "ME" indication is on and the frequency under reception is preset on the channel corresponding to the depressed key. Then the "ME" display goes out and the preset channel number is displayed instead.

○ Preset channel calling

Depress the required key while the radio is on, and the corresponding preset channel is selected and the circuit tunes to the frequency of that channel.

In case the frequency band of the required preset channel is different from that of the channel under reception just before the selection is made, then the band is also changed over automatically.

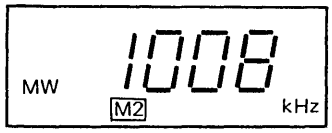
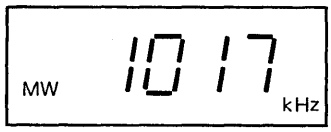
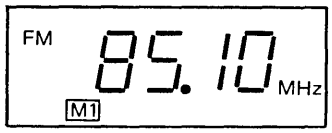
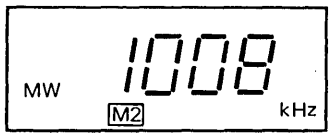
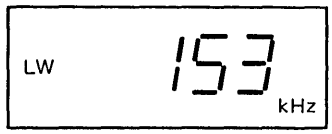
5. Last one memory

This memory is used when the radio power supply is disconnected. When the power supply comes on again, the circuit is tuned to the same frequency as when the power supply was cut off.

6. Last preset channel memory

This memory is used when the bands are changed over. If there exists a frequency already written into the preset memory within the frequency band when the band is selected, the circuit will be tuned to the preset channel within the band being received just before the band is changed over. In case the frequency within the band is not written in the preset memory, the tuning is made to the lowest frequency within the band.

EXAMPLE) Band selection

Key	Display	Description
		1008 kHz of MW band is being received by the preset channel (2 ch).
UP		The frequency is shifted upward by one step and 1017 kHz is received.
FM		The FM band is selected. The preset channel within the FM band received at the last reception (1 ch) is called out.
MW		The MW band is selected. The preset channel received at the last reception (2 ch) is called out. (Note: 1017 kHz which was received at the last reception within the MW band is not called out as it was not preset.)
LW		The LW band is selected. No frequency is preset in LW band. So, the lowest frequency is called out.

7-2. How to adjust the current time

The current time may be changed only when it is being displayed. To change it when the frequency is shown, first depress the CLK/FRQ key so that the time is displayed.

Next, depress the CORRECT key, then the time display goes out and "CORRECT" and ":" (colon) are then displayed, and the flashing of the seconds is interrupted. (In the case of a time display of a 12-hour system, AM or PM is also displayed.)

Input the required time by 10 key. In the case of a 12-hour system time display, AM and PM may be included by the AM/PM key.

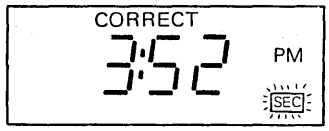
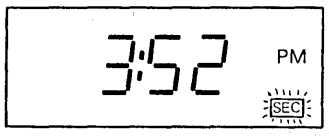
Depress the ENTER key after the input of the new time has finished and the newly set time is displayed. The flashing of seconds is also restored, starting from zero.

In case the input time is not correct, or in case a wrong key (i.e., any key other than 10 key, AM/PM key and CANCEL key) is depressed, "ERROR" is displayed for 5 seconds and the frequency shows while the radio is on. In other cases, however, the time is displayed. If a mistake is made, there is no need to adjust the time since the mechanism continues as normal.

To cancel the change of the time display after depressing the CORRECT key, you should again depress the CANCEL key. No time adjustment is necessary.

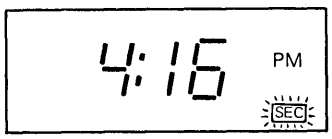
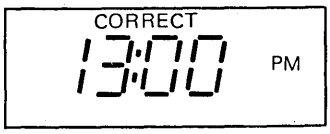
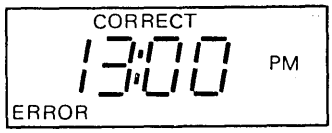
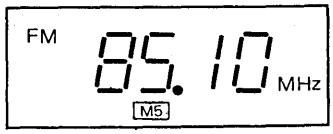
EXAMPLE 1) How to adjust the current time (in the case of a 12-hour display system)

Key	Display	Description
	MW 1008 kHz	Radio is under operation (1008 kHz within the MW band is being received)
CLK/FRQ	11:56 AM SEC	Current time is indicated. (by 12-hour system) Second is flashing.
CORRECT	CORRECT : AM	The correction of current time starts. The time display goes out and "CORRECT" is indicated.
3	CORRECT : 3 AM	The time is fed by 10 key. The display is at the right hand end.
5	CORRECT :35 AM	The numerals are shifted by one unit to the left. (Note) When the input contains 4 or more digits only 1 or 2 is displayed at the uppermost unit.
2	CORRECT 3:52 AM	

Key	Display	Description
AM/PM		Change AM/PM.
ENTER		The 0 second starts at the time when the ENTER key is depressed and the second start flashing.

(Note) In the sequence described above, an optional order may be selected between the work of time input and that of the selection between AM/PM.

EXAMPLE 2) In case erroneous time is fed. (in a 12-hour display system)

Key	Display	Description
		Radio reception is under way. (85.1 MHz is received by the preset 5 ch within FM band)
CLK/FRQ		The current time is being displayed. (12-hour system) . The second is flashing.
CORRECT 1 3 0 0		The time is supplied by 10 key.
ENTER		13:00 in a 12-hour system is an erroneous time. So, "ERROR" is indicated.
(After 5 seconds)		As the radio reception is under way, the frequency display is restored after 5 seconds.

(Note) In doing this, the time before depressing the CORRECT key is maintained in a correct manner.

7-3. Alarm operation

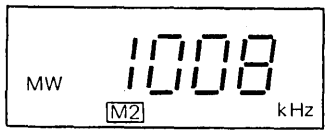
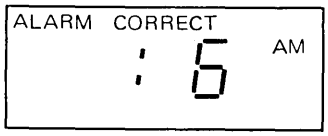
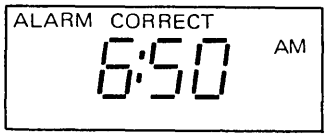
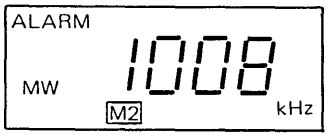
1. How to enter the alarm time

The alarm time may be corrected only when it is being displayed. Depress the ALARM key. The alarm time and "ALARM" are then displayed after 5 seconds or so. (The second does not flash.)

Depress the 10 key or the AM/PM key while the alarm time is displayed, and the alarm time correction mode is obtained and "CORRECT" is displayed.

Depress the ENTER key after finishing the time input. When the radio is on, the frequency is displayed. In other cases, however, the current time is displayed. At the same time "ALARM" is displayed.

EXAMPLE 1) Change of alarm time (12-hour display system)

Key	Display	Description
		1008 kHz within MW band is being received by preset channel 2 ch.
ALARM		Alarm time display. "ALARM" is lit. Second does not flash.
6		Depress the 10 key (or AM/PM key) within 5 seconds after depressing the ALARM key, and the alarm time can be changed. At the same time, "CORRECT" is displayed.
5 0		The time is displayed on the right side and shifts to the left stepwise every time you feed one unit.
ENTER		Depress the ENTER key, and the alarm time is set to 6:50AM. The frequency is displayed when the radio is on. And the "ALARM" display is left to be lit.

2. Alarm operation

When the alarm time coincides with the existing time during "ALARM" is displayed, the alarm becomes ON. In other words, the $\overline{\text{PWROUT}}$ terminal comes to low level and the BUZ terminal is set on. The pulse of 3 kHz modulated by 4 Hz and 0.5 Hz is output from the BUZ terminal. (Refer to the BUZ terminal output chart on P. 8.) However the alarm operation is not made if the PWRIN terminal is at the low level.

In case the T/R terminal is at the low level when the alarm becomes on the radio is actuated at the same time and the last channel is called out.

In case any key is not operated after actuation of the alarm, the alarm goes off after 120 minutes. In other words, at this time, the $\overline{\text{PWROUT}}$ terminal comes to high level and the BUZ terminal comes to low level. If the radio has been selected, it also stops.

In case you would like to stop the alarm before 120 minutes elapse, invert the input of the PWRSW terminal, and the alarm goes OFF. Also you may stop the alarm by depressing the CANCEL key.

While the alarm is on, the time display has priority. If, therefore, the radio is on in the 120 minutes while the alarm is set ($T/\overline{R}$ terminal is at low level) and the keys related to the radio (including CLK/FRQ key) are depressed and the frequency is displayed, the time display is restored after 5 seconds or so. If the ME key is depressed while frequency is displayed, "ME" and frequency are displayed for the first 5 seconds, and the frequency is further displayed for 5 seconds after "ME" goes out.

3. Alarm timer set off

While "ALARM" is displayed, the alarm is always set when the alarm time corresponds to the current time. (Provided, however, the PWRIN terminal is at the high level.)

To eliminate the "ALARM" display, depress the CANCEL key within 5 seconds after depressing the ALARM key. In other words, by depressing the CANCEL key while the alarm time is displayed, the "ALARM" display goes out and the alarm operation is not actuated even when the alarm time coincides with the current time.

4. Alarm timer setting

To see the alarm time, depress the ALARM key. In case, you would like to actuate the alarm at that time, depress the ENTER key within 5 seconds after depressing the ALARM key. In other words,, by depressing the ENTER key while the alarm time is displayed, "ALARM" is displayed and the alarm is actuated when the alarm time coincides with the current time. It is necessary, however, that the PWRIN terminal has been at the high level.

7-4. Sleep operation

1. Sleep time setting

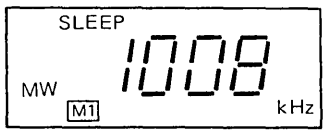
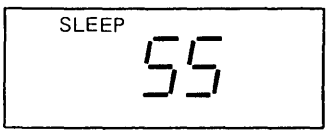
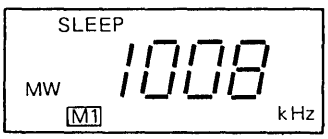
The sleep timer is of such a structure that the power is supplied only during the set time, while the power supply is turned off at other times. The sleep time is divided by 5 minutes intervals and the maximum set time is 60 minutes.

Depress the SLEEP key, and the sleep timer is set and "SLEEP" is displayed. However, this only occurs when the PWRIN terminal accepting the sleep key is at the high level and the PWRSW is at the low level. Further, the alarm timer has priority over the sleep timer. So, the SLEEP key is rejected while the alarm timer is on (PWROUT terminal is at the low level).

"SLEEP" is displayed while the sleep timer is in operation and the radio is operated when the T/$\overline{R}$ terminal is at the low level.

If the sleep key is depressed while "SLEEP" is displayed, the remaining time of the sleep timer is displayed. If the sleep key is again depressed while the indication of remaining time of the sleep timer is displayed, the sleep time is reduced by 5 minutes.

EXAMPLE) How to set the sleep time

Key	Indication	Description
		PWRIN terminal = High level PWRSW terminal = Low level T/$\overline{R}$ terminal = Low level Current time is displayed.
SLEEP		Sleep timer is set on and "SLEEP" is displayed. By doing so, the sleep time is set to 60 minutes and the last channel is called out.
SLEEP		The remaining time of the sleep time is displayed (in terms of minutes). After 5 seconds, the frequency is displayed if the radio is in operation. In other cases, the time display is restored.
SLEEP		Depress the SLEEP key within 5 seconds after the operation described above and the sleep time is reduced by 5 minutes.
(After 5 seconds)		5 seconds after depressing the sleep key, the frequency is displayed when the radio is in operation. In other cases, the time display is restored.

2. Suspending sleep operation

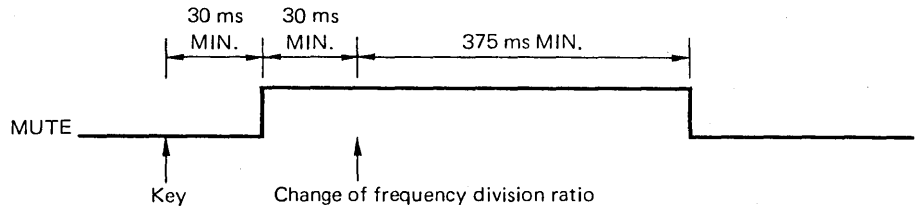
To suspend the sleep operation while the sleep timer is set, either depress the CANCEL key or set either depress the CANCEL key or set the PWRSW terminal to high level.

Note: The alarm timer has priority over the sleep timer. So, when the alarm timer is actuated while the sleep operation is under way, the sleep operation is suspended at that time.

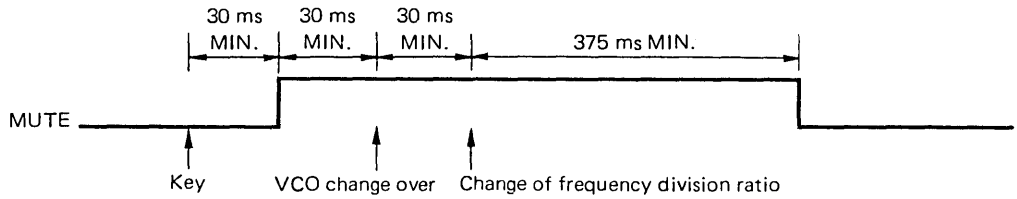
8. MUTE TIMING

8-1. Preset channel calling

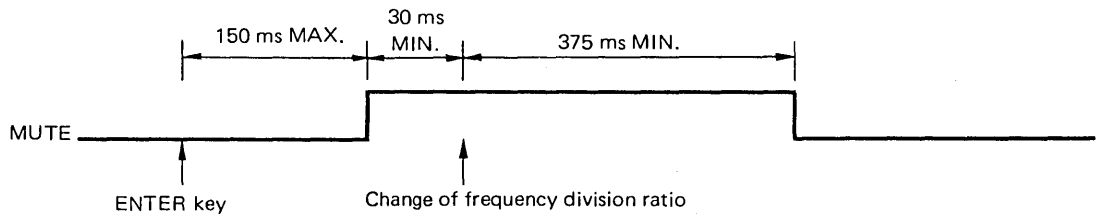
1) In case VCO is not changed over



2) In case VCO is changed over

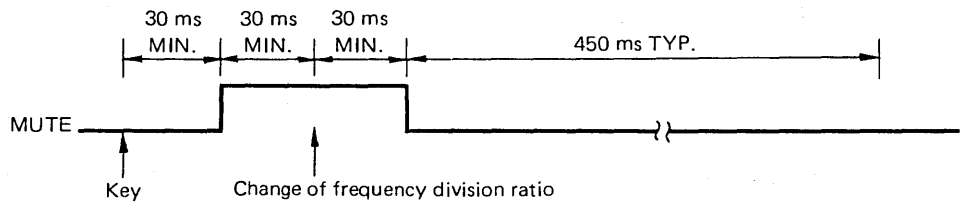


8-2. Direct selection

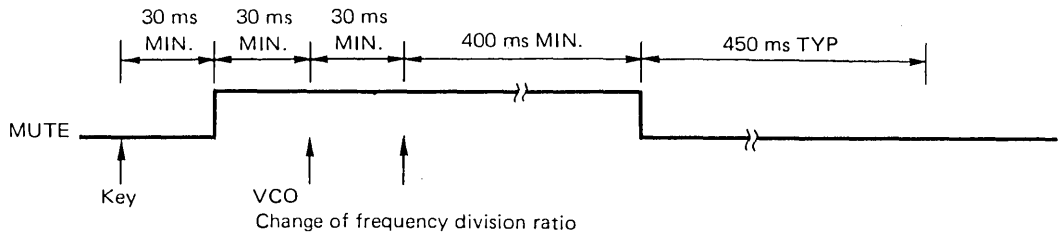


8-3. Manual UP/DOWN

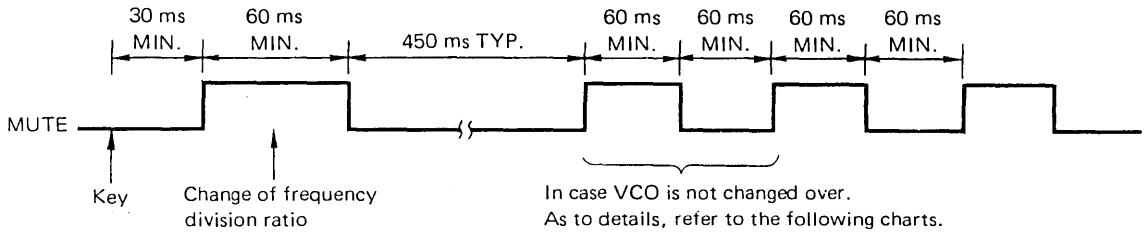
1) 1 channel UP/DOWN (In case VCO is not changed over)



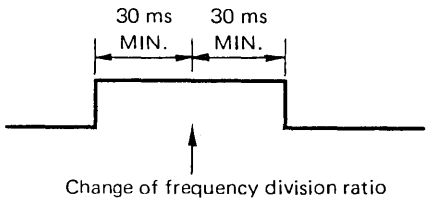
2) 1 channel UP/DOWN (In case VCO is changed over)



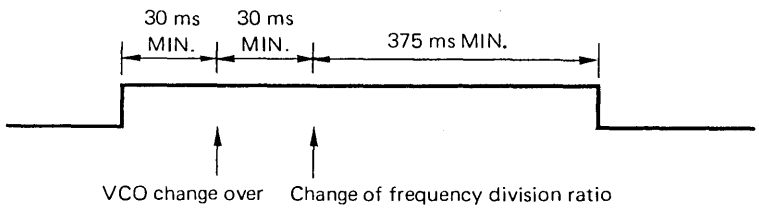
3) Rapid feed UP/DOWN



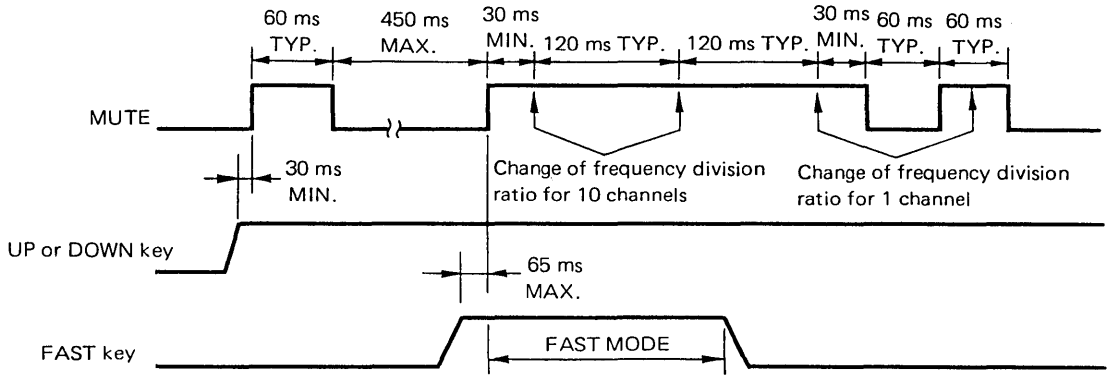
a) In case VCO is not changed over



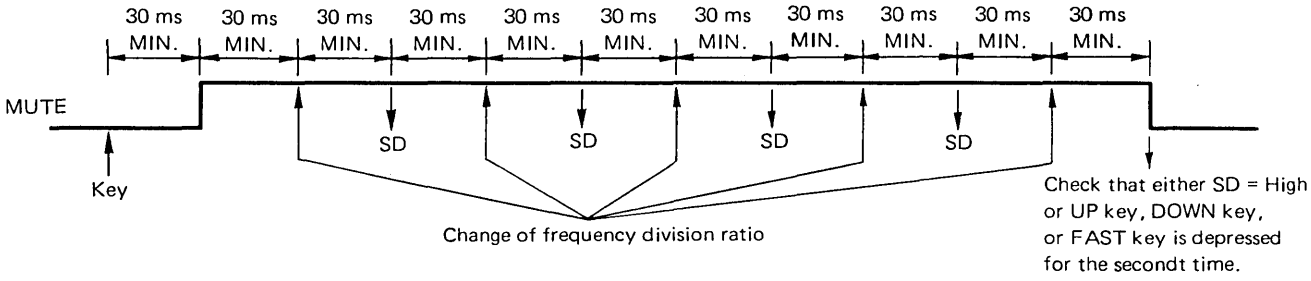
b) In case VCO is changed over



4) Ultra rapid feed UP/DOWN

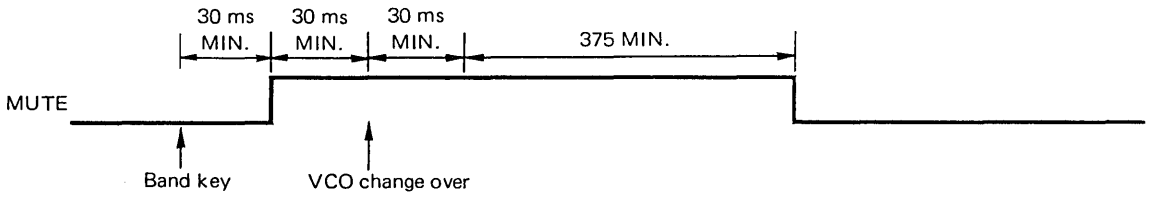


8-4. Auto UP/DOWN

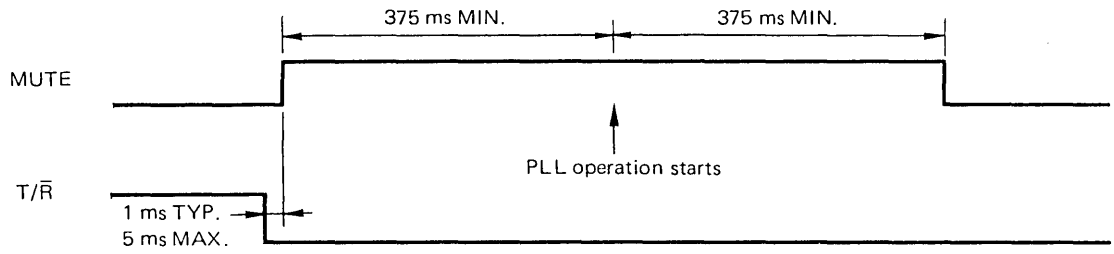


Note) $\overset{\downarrow}{SD}$ indicates the timing of SD terminal check.

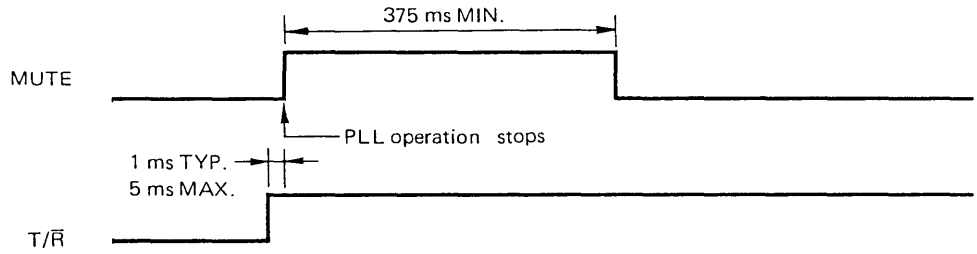
8-5. Frequency band change-over



8-6. Change-over from Tape to Radio



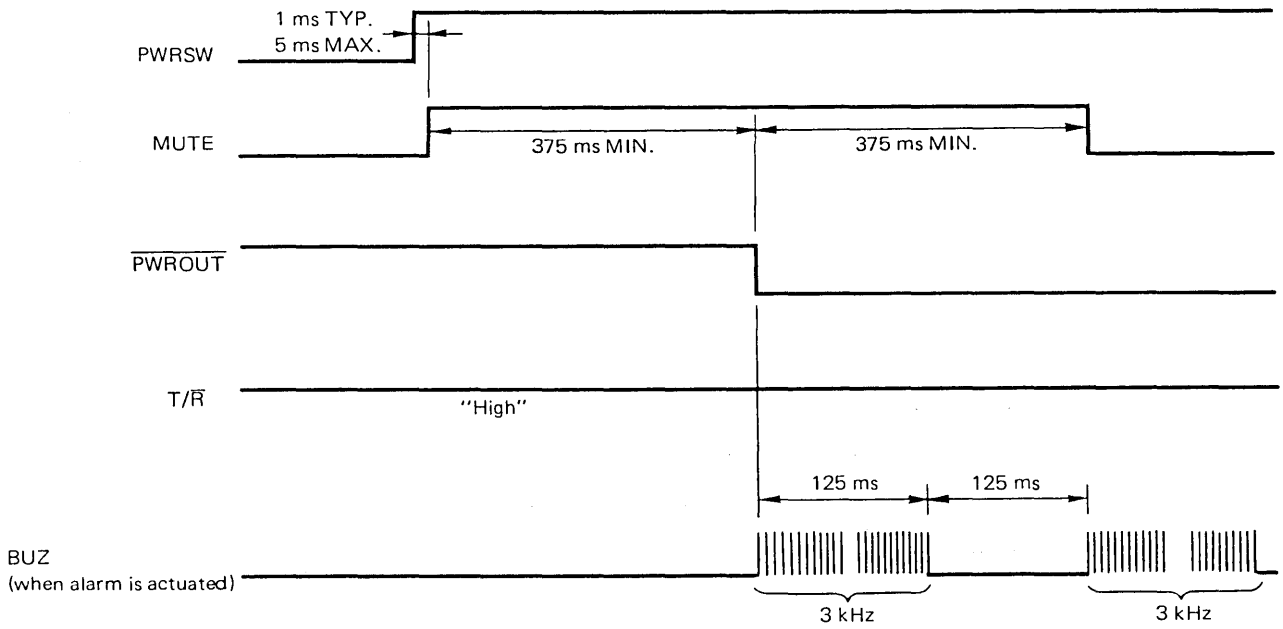
8-7. Change-over from Radio to Tape



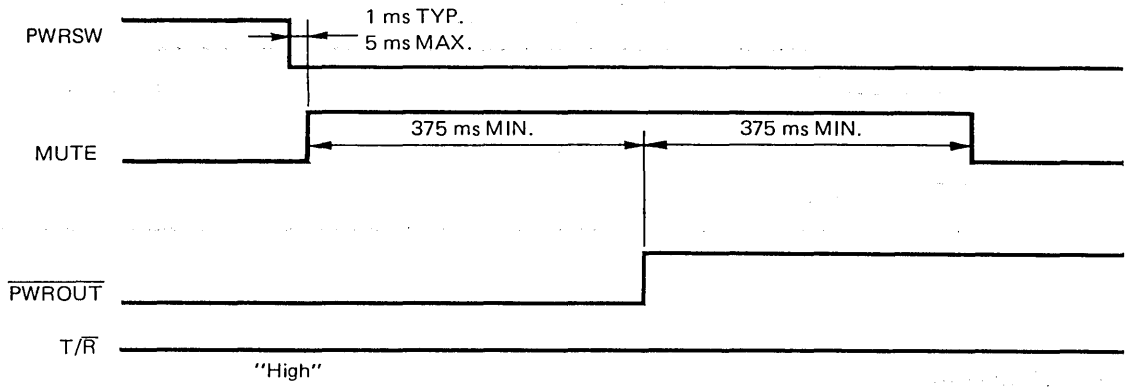
8-8. Power Supply Switch Operation

(The Power supply ON/OFF operation by Alarm/Sleep operation is also in the same timing.)

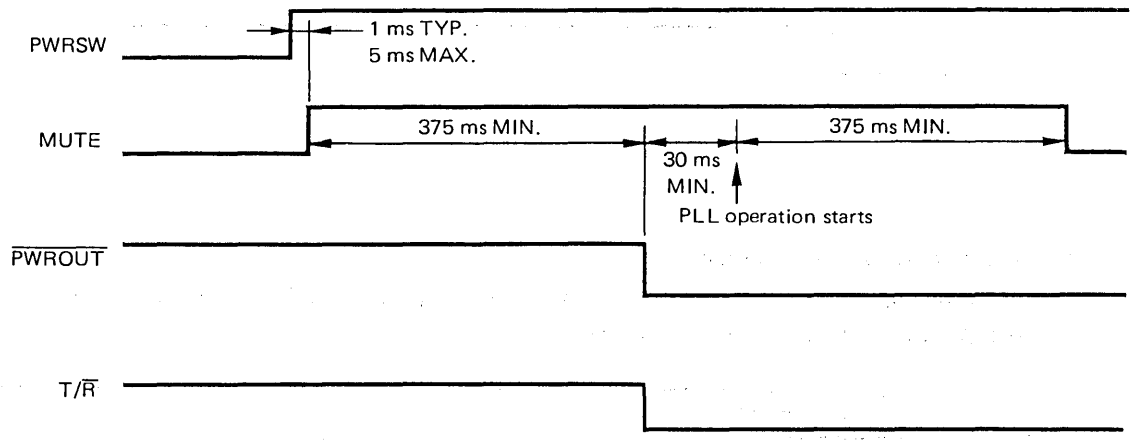
1) PWRSW OFF → ON (Low → High) (Tape)



2) PWRSW ON → OFF (High → Low) (Tape)

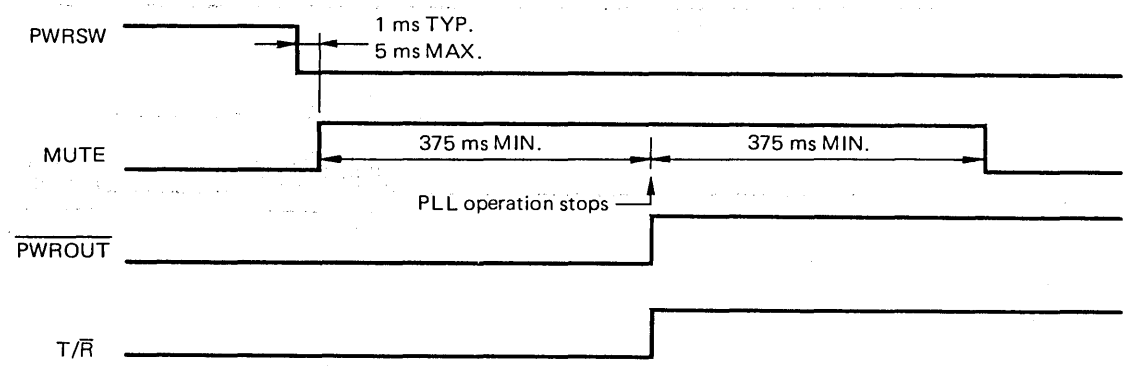


3) PWRSW OFF → ON (Low → High) (For radio)

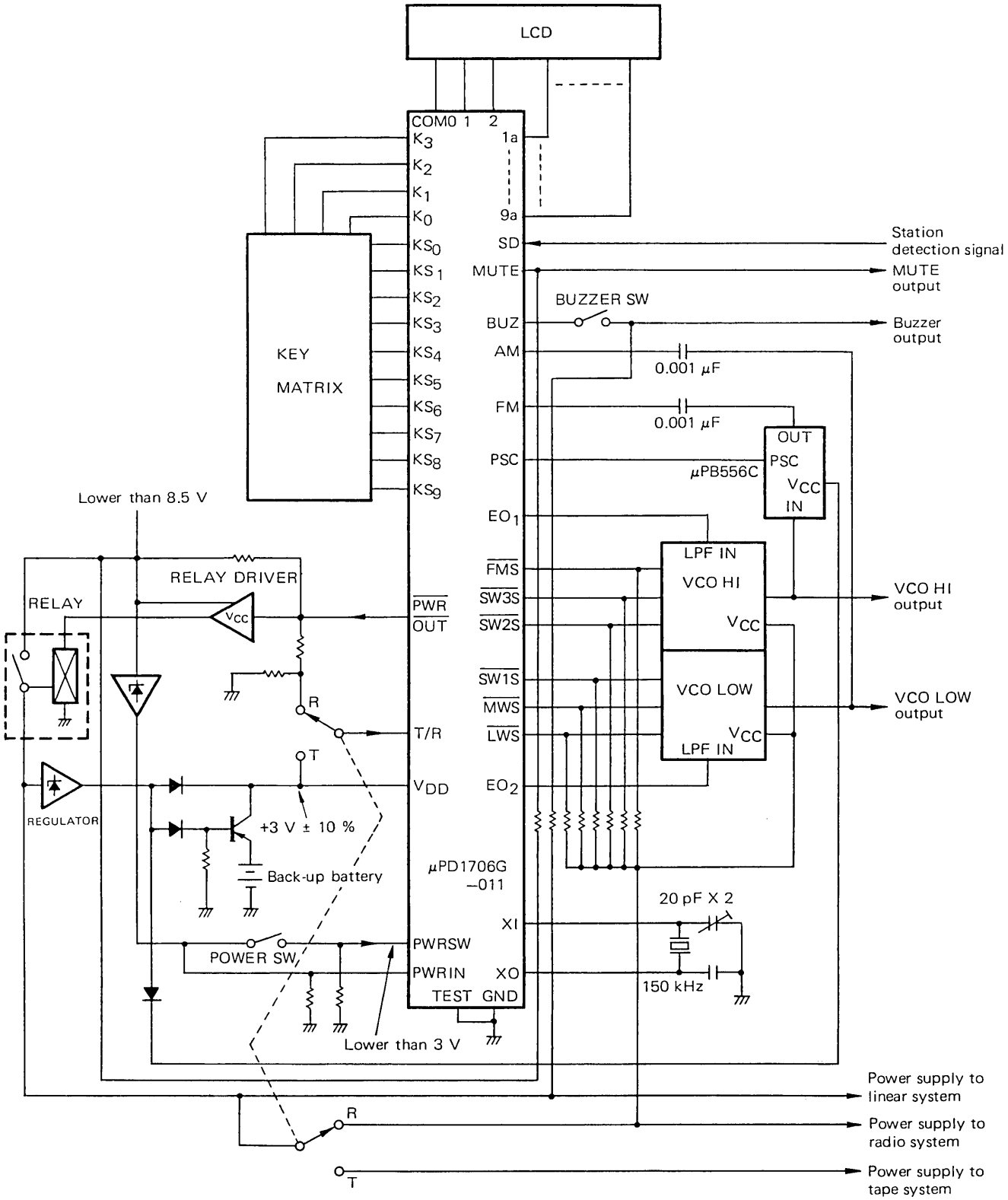


Note) When the TAPE/RADIO select switch is thrown to the RADIO side, it is interlocked with PWROUT.

4) PWRSW ON → OFF (High → Low) (For radio)



9. EXAMPLE OF APPLIED CIRCUIT



INDEX

MOS DIGITAL INTEGRATED CIRCUIT
μPD832G, μPD833G

8-CHANNEL DIGITAL LIQUID CRYSTAL DISPLAY, TIMEPIECES AND TIMER CIRCUIT WITH 4MHz OR 32kHz CRYSTAL OSCILLATOR OPERATION.

GENERAL DESCRIPTION

The μPD832G and μPD833G are CMOS LSI operating at the reference frequency of either 4.2 MHz or 32 kHz crystal oscillation, for use as multi-purpose electronic timepieces (clock & watch) and timers of 4-digit liquid crystal display type.

Composition of 8-Channel Digital Timepieces (clock & watch) and Timer

1. Standard time
2. Alarm timer
3. Snooze timer
4. Sleep timer
5. Control timer
6. Dual time
7. Stopwatch
8. Counter

FEATURES

1. Hours, minutes, seconds, AM and PM can be displayed.
2. Selection of either 12-hour or 24-hour display format is possible.
3. Instantaneous second correction is possible within an error of ±30 seconds.
4. Minutes and hours can be set independently. (at 1 pps or one push per one word step.)
5. That the tens digit of minutes, AM and PM can be set independently for alarm time (or control time) or dual time is very convenient.
6. Provided with a fine alarm tone.
7. Alarm timer offers the 4-minute duration alarm. By using the SNZ (snooze) terminal, the timer can offer the alarm every four minutes through the CANCEL-REFRESH method.
8. The trial sounding of alarm can be made.
9. The duration of control timer and sleep timer can be set in four ways at 15 minutes, 30 minutes, 60 minutes and 120 minutes.
10. The application as an multi-timer is possible with its two-phase control timer signal.
11. Since the dual time is available, it can be used as displaying second time zone or elapsed time.
12. The stopwatch can count up to 24 min.
13. The counter can count up to 1440 counts.

14. All memory sections excluding the LCD driver section with V_{SH} series (3.0 to 6.0 V) are composed of V_{SS} series. Thus, the system design is very simple with this device.

15. The source voltage for the alarm out, control out and sleep out terminals is variable from 1.5 to 6.0 V through the employment of open drain P-channel transistor.

16. (i) Standard time, dual time, and sleep timer or (ii) Standard time, stopwatch and sleep timer can be used in parallel independently.

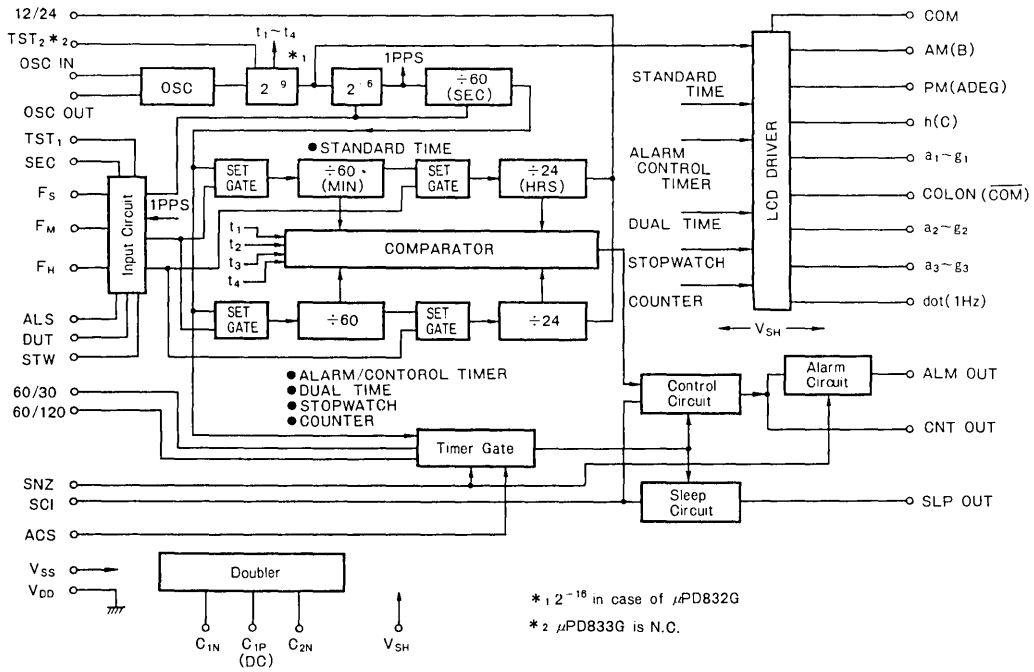
APPLICATIONS

- Digital alarm clock
- Sleep timer
- Snooze timer
- Traveller's watch
- Appliance timers
- Measuring timer for the distance covered
- Clock and watch displaying different time zone (World time)
- Sequential controller
- Desk timer
- Portable timer for miscellaneous controls

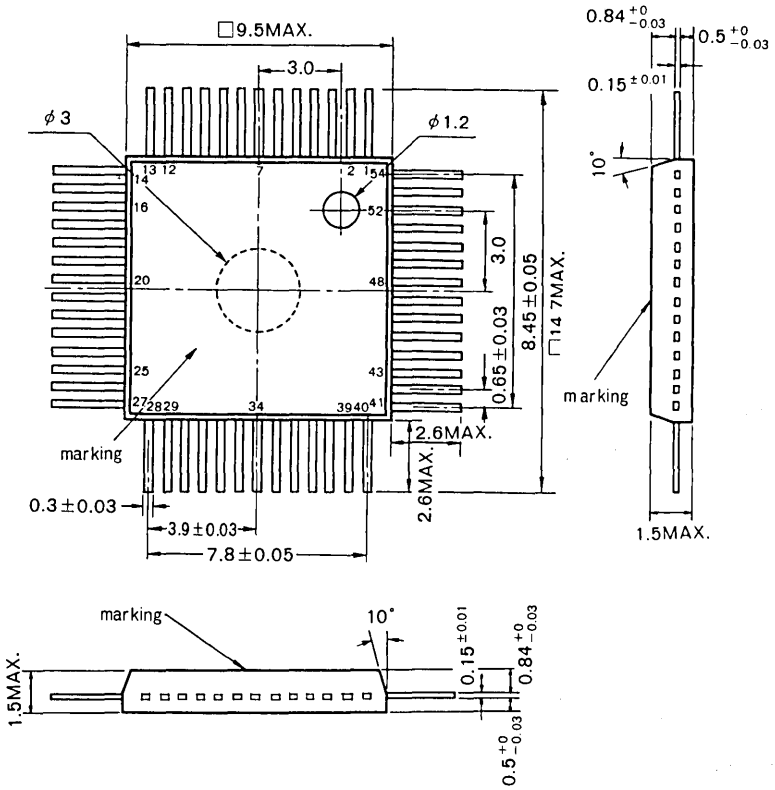
TYPES

Type No.	Frequency of the crystal
μPD832G	4.194304 MHz
μPD833G	32.768 kHz

BLOCK DIAGRAM



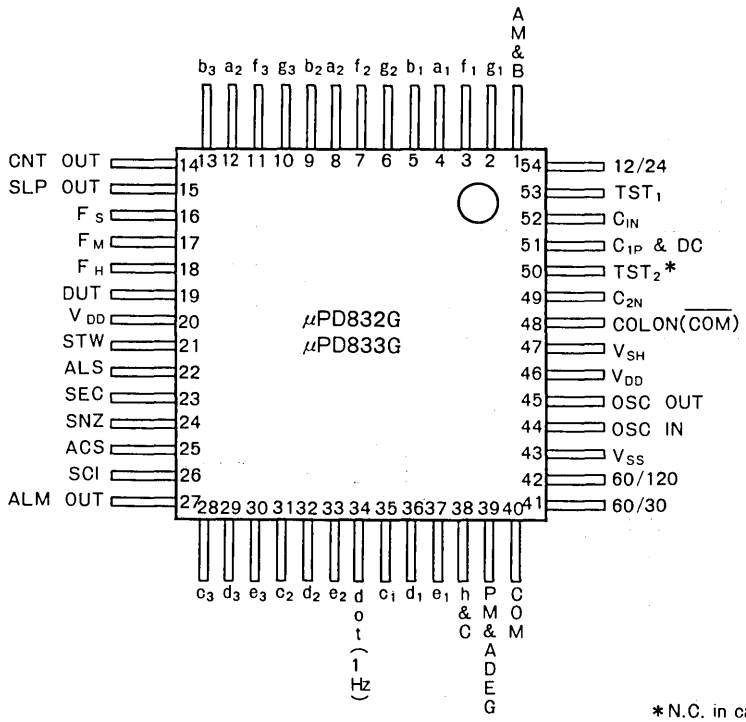
PACKAGE DIMENSIONS (Unit: mm)



PIN CONNECTION

PIN NO.	Designation	PIN NO.	Designation
1	AM & B	28	c_3
2	g_1	29	d_3
3	f_1	30	e_3
4	a_1	31	c_2
5	b_1	32	d_2
6	g_2	33	e_2
7	f_2	34	dot(1Hz)
8	a_2	35	c_1
9	b_2	36	d_1
10	g_3	37	e_1
11	f_3	38	h & C
12	a_3	39	PM & ADEG
13	b_3	40	COM
14	CNT OUT	41	60/30
15	SLP OUT	42	60/120
16	F_S	43	V_{SS}
17	F_M	44	OSC IN
18	F_H	45	OSC OUT
19	DUT	46	V_{DD}
20	V_{DD}	47	V_{SH}
21	STW	48	COLON($\overline{COM}$)
22	ALS	49	C_{2N}
23	SEC	50	TST_2*
24	SNZ	51	C_{1P} & DC
25	ACS	52	C_{IN}
26	ACI	53	TST_1
27	ALM OUT	54	12/24

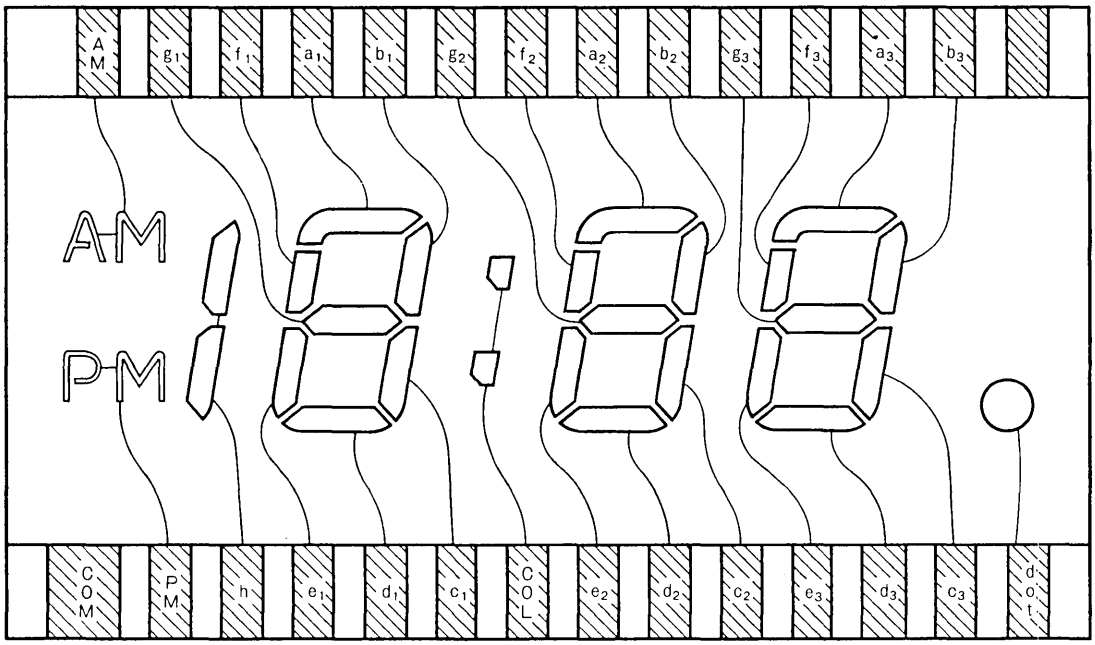
CONNECTION DIAGRAM



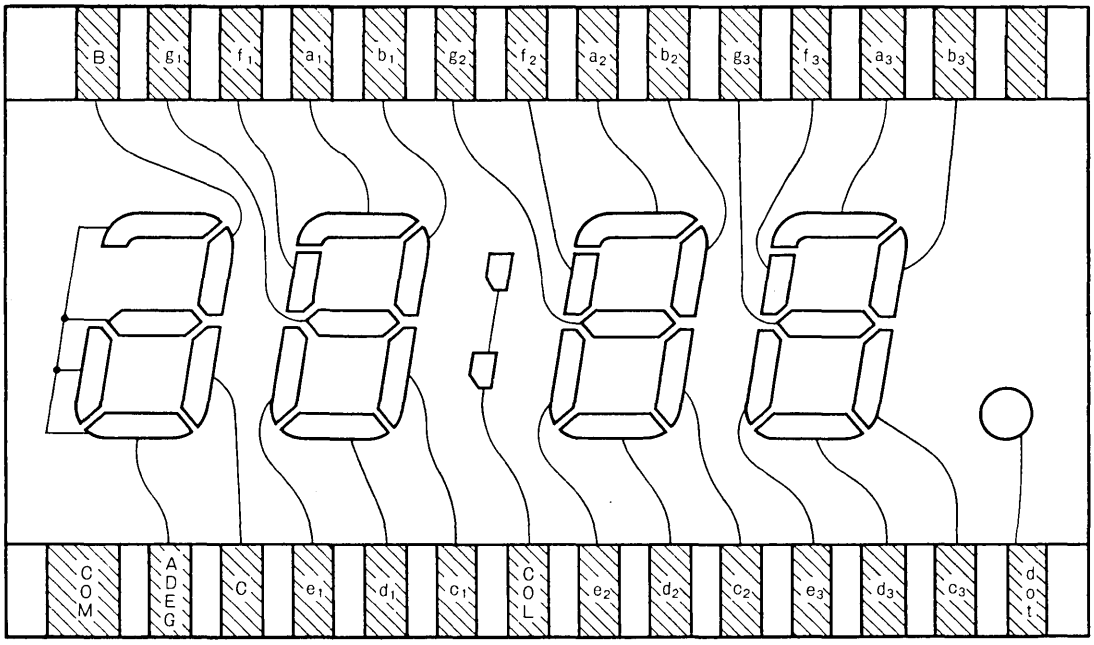
*N.C. in case of μPD833G

FIELD EFFECT LCD

12 hour display format



24 hour display format



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

CHARACTERISTIC	SYMBOL	RATINGS	UNIT
Operating Voltage	V_{SS}	− 3.0	V
Operating Voltage	V_{SH}	− 7.0	V
Operating Temperature	Topt	−20 to +75	°C
Storage Temperature	Tstg	−40 to +125	°C

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

μPD832G (f=4.194304 MHz, V_{DD}=Common, V_{DD}–V_{SS}=1.5 V, C_G=C_D=15 pF)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Voltage	V_{DD}–V_{SS}	1.2	1.5	1.9	V	Ta = −20 ~ +75 °C
Current Consumption	I_{SST}		30	90	μA	C_1=C_2=0.1 μF, NO DISPLAY

μPD833G (f=32.768 kHz, V_{DD}=Common, V_{DD} − V_{SS}=1.5 V, C_D=5~40 pF, C_G=5~30 pF)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Voltage	V_{DD}–V_{SS}	1.1	1.5	2.0	V	Ta = −20~+75 °C
Current Consumption	I_{SST}		2.0	5.0	μA	C_1=C_2=0.1 μF, NO DISPLAY

μPD832G, μPD833G

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Voltage	V_{DD}–V_{SH}	2.2	3.0	6.5	V	Ta = −20 ~ +75 °C
LCD Common Output Current	I_n & I_P	30			μA	V_{DD}–V_{SH}=2 V, V_{DS}=0.1 V
LCD Segment Output Current	I_n & I_P	5			μA	V_{DD}–V_{SH}=2 V, V_{DS}=0.1 V
DC, $\overline{DC}$ Output Current	I_n & I_P	100			μA	V_{DD}–V_{SS}=1.5 V, V_{DS}=0.5 V
ALARM/CONTROL/SLEEP Output Current	I_P	100			μA	V_{DD}–V_{SS}=1.5 V, V_{DS}=0.5 V
Doubler	V_{SHD}	3.0			V	V_{DD}–V_{SS}=1.55 V, RL=3 MΩ C_1=C_2=0.1 μF

PULL DOWN RESISTANCES (Internally connected to −V_{SS})

TERMINALS	$V_{DD}-V_{SS}$	RESISTANCE	UNIT
F_S	1.5 V	0.01 ~ 1.0	MΩ
F_M	1.5 V	0.01 ~ 1.0	MΩ
F_H	1.5 V	0.01 ~ 1.0	MΩ
SNZ	1.5 V	0.01 ~ 1.0	MΩ
ACS	1.5 V	0.01 ~ 1.0	MΩ
SCI	1.5 V	0.01 ~ 1.0	MΩ
TST	1.5 V	0.01 ~ 1.0	MΩ
DUT	1.5 V	OPEN	
STW	1.5 V	OPEN	
ALS	1.5 V	OPEN	
SEC	1.5 V	OPEN	
60/30	1.5 V	OPEN	
60/120	1.5 V	OPEN	
12/24	1.5 V	OPEN	

FUNCTIONAL DESCRIPTION

1. Segment Terminal

The frequency antiphase to 64 MHz frequency at COMMON terminal is present at the segment terminal displayed. At the segment terminal not displayed, the frequency is inphase to 64 MHz frequency at Common terminal. (Refer to Fig. 1)

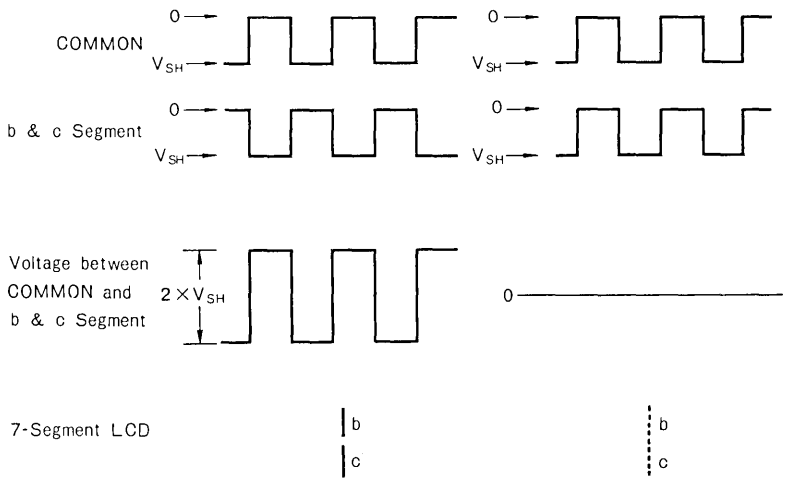


Fig. 1

2. Display Format

(1) Standard Time

DISPLAY MODE	12-Hour Format	24-Hour Format	ACTIVE terminal
ⓘ NORMAL	HRS MIN AM 10:53◐ PM	HRS MIN 22:53◐	
ⓘ SECOND	MIN SEC 3:26◐	MIN SEC 3:26◐	SEC

(2) Memory

DISPLAY MODE	12-Hour Format	24-Hour Format	ACTIVE terminal
ⓘ ALARM / CONTROL Timer	HRS MIN AM 2:30● PM	HRS MIN 14:30●	ALS
ⓘ DUAL TIME	HRS MIN AM 2:30◐ PM	HRS MIN 14:30◐	DUT ALS
ⓘ STOPWATCH	MIN SEC AM 0:00● PM	MIN SEC 0:00●	STW ALS
ⓘ COUNTER	Count 0:00●	Count 0:00●	STW ALS

◐ means flashing dot.

● means dot "on" cont'ly.

● means colon "on" cont'ly
●

Active Terminal: Sets the designated input terminal to V_{DD} level.

Fig.2

3. Designation and Definition of Every Input and Output Terminal (Excluding Segment)

(1) Input Terminal

Normally every input terminal is set to the V_{SS} level (−1.5 V). An input terminal with internal pull-down resistors allow use of simple SPST switches to select the functional Mode. (Refer to the table for Pull-down resistor incorporated for input terminal.)

Therefore, when operating an input terminal, set it to the ACTIVE "H" ie V_{DD} level (0 V).

F_S (Fast Second)

The second setting terminal which, with respect to K minutes, discards the gain of 01 to 29 seconds to 00 second and carries the delay of 00 to 30 seconds to the succeeding minutes K minutes. This terminal operates instantaneously. In other words, by connecting the terminal F_S to V_{DD} in accordance with the time signal, the second is reset to "00". The second digit starts working. When the second counts "30" to "59" and F_S is connected to V_{DD} one minute and the second instantaneously return to "00". The error for this adjustment is smaller than 31 ms to K minutes 00 second.

On the other hand, when using this input terminal at V_{DD} level for an alarm/control time (ALS) or dual time (DUT, ALS), the function with respect to the setting is changed service of shifting digit to be called as F_S (Fast Shift). In other words, if the terminal F_M is connected to V_{DD} after setting the terminal F_S to V_{DD} level, only the tens of minutes is independently advanced fast at 1 pps.

When the terminal F_H is connected to V_{DD} after setting the terminal F_S to V_{DD} level, the AM or PM indication is shifted independently at 1 pps. rate. The repeated ON (at V_{DD} level)⇄OFF operation of minutes or the display of AM or PM at the speed of hand-operating.

F_M (Fast Minute)

The terminal for the setting of minutes which advances the minutes independently at 1 pps when connects to V_{DD} (later called set to ON). When this terminal is repeatedly on and off, the minutes can be advanced the speed of hand-operating.

In case of stopwatch (STW, ALS), the ON operation of this terminal resets the display to 0 min, 00 sec.

F_H (Fast Hour)

The terminal for the setting of hours which advanced the hours independently at 1 pps when set to V_{DD} level. The repeated ON-OFF operation of this switch is advanced the hours at the speed of hand's movement.

In case of stopwatch (STW, ALS), if this terminal is on, the function is shifted Start-Stop (Hold).

SNZ (SNooZe)

The SNOOZE terminal which stops the alarm tone when it is on. Alarm tone starts again after 4^{+0}_{-1} minutes after the terminal SNZ is off.

This terminal is operated on the basis of cancel-refresh method in which the alarm tone starts 3 or 4 minutes after setting the terminal to ON.

The effective period of cancel-refresh method is extended with every cancellation of alarm tone with the terminal SNZ.

On the other hand, the control output (CNT OUT) and the sleep output (SLP OUT) is not off with the on operation of SNZ terminal but, the duration of control output and sleep output is reset. Therefore, the terminal SNZ is provided with a function as snooze timer with respect to the alarm output, in addition to the above function, it has the function to extend the time interval with respect to the control output and sleep output.

ACS (Alarm Control Sleep Stop)

This terminal is used for the cancellation of the alarm, control and sleep terminals. When this terminal is on, all output the alarm, control and sleep are off immediately.

SCI (Sleep Control Input)

This terminal is used for the sleep setting or two-phase control setting. When this terminal is on, the sleep output can be obtained from the terminal SLP OUT. In this case, the control output can be also obtained through the terminal CNT OUT. Therefore, if the control time is set after the duration of control time, the 2-phase control output can be obtained.

The SCI signal is converted into a single pulse of approximately 8-ms pulse width inside the LSI.

TST (TeST)

This terminal is used for the test. This terminal, when set to V_{DD} level, permits the high speed test of LSI in combination with the aforementioned terminals F_S, F_M and F_H set to ON.

All of above-mentioned input terminals has their own built-in resistor for the prevention of floating.

DUT (DUal Time)

This terminal is used to set the dual time and normally set to V_{DD} level. Moreover, when the terminal ALS in on, the display of dual time can be observed. Thus, this terminal is operated in combination with the terminal F_S, F_M and F_H to form a world timer (dual zone time) or timer to be used for the measurement of elapsed time.

STW (STop Watch)

This terminal is used to set the stopwatch and is normally set to V_{DD} level. With the terminal ALS set to ON, the display of a stopwatch is available. Thus, this terminal is on in combination with the F_M and F_H terminals.

ALS (Alarm controL Set)

This terminal is used for the alarm or control setting. When this terminal is on, the hours subjected to the alarm tone and control operation can be displayed. This terminal is used in combination with the terminals F_S, F_M and F_H.

On the other hand, if this terminal is used with the DUT terminal, the dual time can be set. This terminal can be used to set a stopwatch when operated in combination with the STW terminal (Refer to Fig. 2.)

SEC (SECond)

This terminal is used to set the seconds. When this terminal is on, the seconds of the standard time can be displayed.

60/30 (60 minutes/30 minutes)

This terminal is used for the switching over between 60-minutes duration and 30-minutes duration to set the duration of control or sleep signal. This terminal is normally set to V_{SS} level (−1.5 V) for the 60-minutes duration. When this terminal is connected to V_{DD}, the time interval is changed to 30 minutes. The 60-minutes duration is exactly the time interval of up to 64-minutes and the 30-minutes duration is exactly 32-minutes duration.

60/120 (60 minutes/120 minutes)

This terminal is used for the switching over between 60-minutes duration and 120-minutes duration to set the duration of control or sleep signal. This terminal is normally set to V_{SS} level (−1.5 V) for 60-minutes duration. When this terminal is connected to V_{DD}, the time interval is change to 120 minutes (exactly to 128 minutes). When both terminals 60/30 and 60/120 are connected to V_{DD}, the 15-minutes duration can be obtained. This is exactly the time interval of up to 16-minutes.

12/24 (12 hours/24 hours)

This terminal is used for the switching over between 12-hour indication and 24-hour indication to set the standard time, alarm timer and control timer. This terminal is also used to determine the switching over of the hour display format of dual time. This terminal is normally set to V_{SS} level (−1.5 V) for 12-hour indication. When this terminal is connected to V_{DD}, the indication is shifted to 24-hour.

* Since the above-mentioned input terminals (DUT-12/24) are open ones, be sure to set the signal pole double throw switches (snap switches).

When single pole single throw pushbutton switches are used, be sure to insert the pull-down resistor into every terminal. In this case, note that if every terminal is connected to V_{DD}, the current at (1.5 (V)/Rpd(MΩ)) A is present in accordance with Ohm's law from $V_{DD} - V_{SS} = 1.5$ V and pull-down resistance Rpd.

The pull-down resistance Rpd should be determined on the basis of the grounding capacity of clocks or watches and the capacity of battery.

(2) Output Terminal

Every output terminal is provided with P channel open drain transistor.

CNT OUT (CoNTrol Out)

This is the control output terminal and is set to V_{DD} level (0 V) when it is on. The selection of one of four durations, 15-minute, 30-minute, 60-minute and 120-minute is possible as explained before.

SLP OUT (SLeeP Out)

This is the sleep output terminal and is set to V_{DD} level (0 V) when it is on. The selection of one of four durations, 15-minute, 30-minute, 60-minute and 120-minute is possible as explained above.

ALM OUT (ALarM Out)

This is the alarm output terminal. When it is on, 2.048 kHz signal modulated by 8 Hz frequency is produced every other second. The alarm signal stops automatically after four minutes from the beginning.

However, if the terminal SNZ (snooze) is on, the alarm signal stops immediately. Then, the alarm signal starts again after 4^{+0}_{-1} minutes from the disconnection of the terminal SNZ. This operation is called Cancel-Refresh system.

4. Power Supply Circuit

The integral parts (memory and control circuits) of this LSI is composed of the components of V_{SS} system. The V_{SS} system supplies $V_{DD} - V_{SS} = 1.5$ V. The V_{SH} system for the liquid crystal driver voltage supplies $V_{DD} - V_{SH} = 2.2 \sim 6.5$ V. The LSI is provided with voltage doubler circuit in its inside.

The application of those circuits are as follows:

○ Voltage Doubler Circuit

To establish the voltage doubler circuit, connect the capacitor C_1 between the terminals C_{IN} and C_{IP} and the capacitor C_2 between the terminals C_{2N} and V_{DD}. Then, the voltage approximately twice as large as $V_{DD} - V_{SS} = 1.5$ V is present at the C_{2N} terminal.

Finally, connect the terminals C_{2N} and V_{SH}.

* Capacitors C_1, C_2 are of 0.1 to 0.68 μF with small leak and of favorable temperature characteristics. The liquid crystal driver voltage (C_{2N}) from the voltage doubler circuit permits the direct operation of liquid crystal whose letter height is up to approximately 1 inch (2.54 cm).

It can be introduced another supply voltage (2.2 ~ 6.5 V) into V_{SH}.

5. Oscillator Circuit

This oscillator circuit has its built-in feedback bias resistor.

In case of μPD833G connect the quartz oscillator of the particular frequency of 32.768 kHz between the terminals OSC IN and OSC OUT. Connect OSC IN to V_{DD} or V_{SS} through capacitor C_G (5~30 pF) and OSC OUT to V_{DD} or V_{SS} through capacitor C_D(20~40 pF). Although the temperature characteristics and voltage drop characteristics differ with the type of quartz oscillator they are favorable with exact oscillator frequency of 32.768 kHz when C_G is between the values CD/5 and CD/2.

In case of μPD832G connect the quartz oscillator of particular frequency of 4.194304 MHz between the terminals OSC IN and OSC OUT. Then, connect OSC IN and V_{DD} through C_G and OSC OUT and V_{DD} or V_{SS} through C_D. (C_G = C_D = 10 to 20 pF)

Quartz oscillators of around 4 MHz frequency are of AT cut with favorable temperature characteristics.

6. Operation of each Terminal

6–1. Standard Time

1. Indication

With each input terminal set to V_{SS} level, the normal display is made on the standard time as shown in Fig. 2, (1), ⓘ. The indication is for hours and minutes, and AM and PM are displayed for 12-hour indication.

When the display of seconds is required, connects the terminal SEC to V_{DD} (later this operation is referred simply to "on"). Then, the units digit of minutes and seconds can be obtained as shown in Fig. 2, (1), ⓘⓘ. To reset the display of seconds, set the terminal SEC to OFF.

2. Setting of Time

To set the time, use the terminals F_S, F_M and F_H. Normally the standard time is set to the present time. First, set seconds with the terminal F_S. When the gain is between 01 to 29 seconds, it is discarded to 00 seconds through the ON operation of F_S terminal and when the indication is between 30 to59 seconds (delay in 01 to 30 seconds), it is set to be added one minute, and to 00 second. Then the second digit starts working immediately.

The accuracy in setting the time is within ±31 ms excluding the error in hand-operating. The correction of seconds is applicable to the normal display (Fig. 2, (1), ⓘ) and the second display (Fig. 2, (1), ⓘⓘ). The correction of seconds is not applicable to the displays other than above.

Next, set minutes with the terminal F_M. While the minutes are set, the overflown seconds are carried to minutes, but the overflown minutes are not carried to hours.

Last, set hours with the terminal F_H. While hours are set, overflown minutes are carried to hours. Only in case of 12-hour indication, overflown hours are shifted from AM to PM and vice versa. From both the terminals F_M and F_H, when kept on, the advancing signal is sent at 1 pps. But therepeated ON-OFF operation of those terminals offers setting of hours and minutes at the speed of hand-operating.

The setting of minutes and hours is effective for the normal display (Fig. 2, (1), ⓘ), and no setting of minutes and hours is applicable for the displays other than above.

* In case of using the quartz as an oscillator signal frequency source, the loss/gain at normal temperature range is within ±0.1 to ±0.5 seconds a day. Therefoe, the standard time is convenient for use through the instantaneous operation of the terminal F_S to make the correction.

The terminals F_S, F_M and F_H should usually be in non-sensitive status for the displays for minutes and seconds (Fig 2, (1), ⓘ and ⓘⓘ).

6–2. Alarm Timer

6–3. Control Timer

1. Display

With every input terminal set to the V_{SS} level, the memory offers the operation of alarm timer or control timer.

When setting the alarm time or control time for an electronic instrument, set the terminal ALS ON. Then the alarm or control time (Fig. 2, (2), ⓘ) is displayed even if represented the standard time (Fig. 2, (1), ⓘ and ⓘⓘ).

* Note that alarm time and control time are displayed in same way.

2. How to set the alarm time (or control time)

To set the alarm (or control) time, first set the terminal ALS on. Then, with the terminals F_M, F_H and F_S, set the alarm time (or control time), to obtain the display of alarm or control time as shown in Fig. 2, (2), ⓘ. accoriding to same methods to set the present time.

2.1 Setting of minutes

① With the terminal F_M set to ON, the minutes can be automatically set to the desired figures at 1 pps. If you are required to set it faster, repeat the ON-OFF operation of the terminal F_M. Then, minutes can be set at the speed of hand-operating. (one push one word method).
As shown in the Fig. 3, the minutes are not to be carried to hours when minutes are overflown.

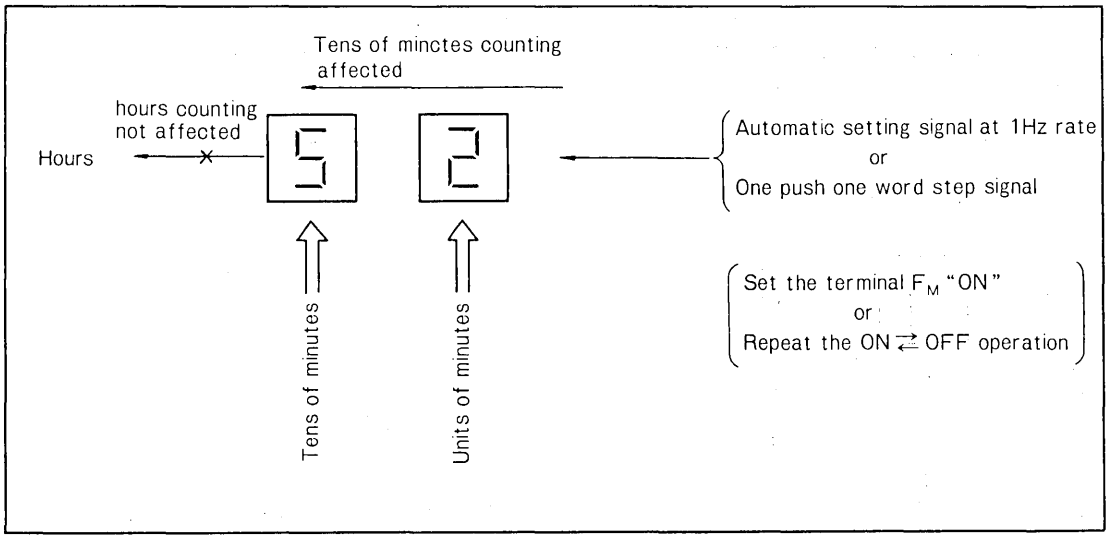


Fig.3

② When you are required to set the minutes faster, proceed with the following steps.
First, set the terminal F_S on, and set the terminal F_M on. Then, the tens digit of minutes can be set at 1 pps. Thus, the tens digit of minute can be set faster.
If you want to set minutes faster than above, keep the terminal F_S set to on, and repeat ON-OFF

operation of the F_M terminal. Then, the tens digit of minutes can be set at the speed of hand-operating. As shown in the Fig. 4, the display of minutes is not to be carried to hour when the minutes are over-flown.

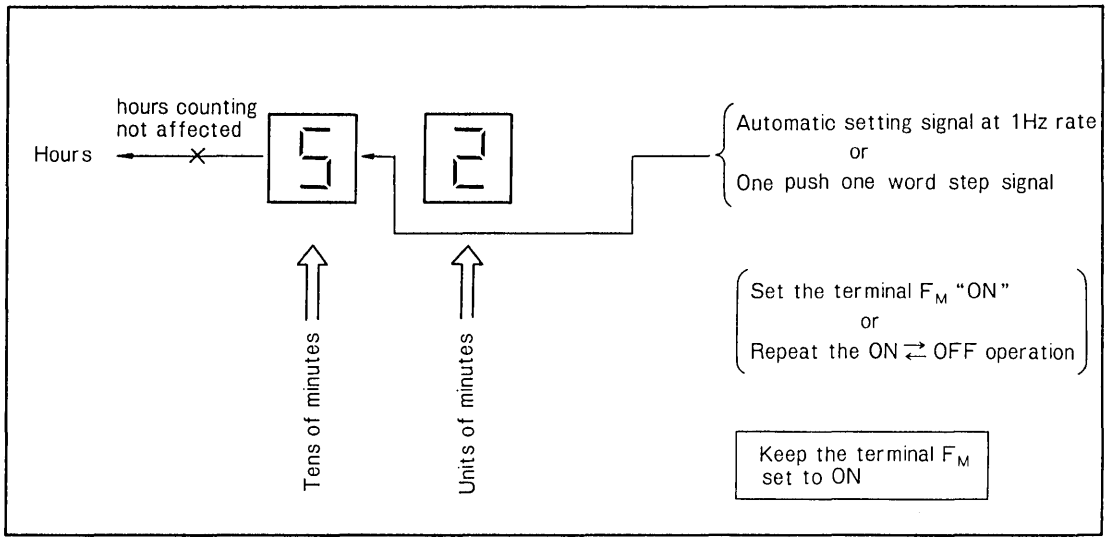


Fig.4

* Let us give an explanation of how to set minutes. Presuppose the display of minutes is 52. And you want to correct it to 41. First following the method 1 above, set the units digit to 1. In this case, the units digit is carried to tens digit due to the overflowing of the untis digit. This can be ignored. Then, set tens digit to 4. According to this method 2, the automatic setting at 1 pps completes within 14 seconds in case where there is no erroneous setting. The setting of minutes with one push one word signal completes within four seconds.

2.2 How to set Hours

① Set the terminal F_H on, then, the setting can be made to the desired figures at 1 pps.
When you are required to set hours faster, repeat the ON-OFF operation of the terminal F_H. Then, hours can be set at the speed of hand-operating. Refer to the Fig. 5.

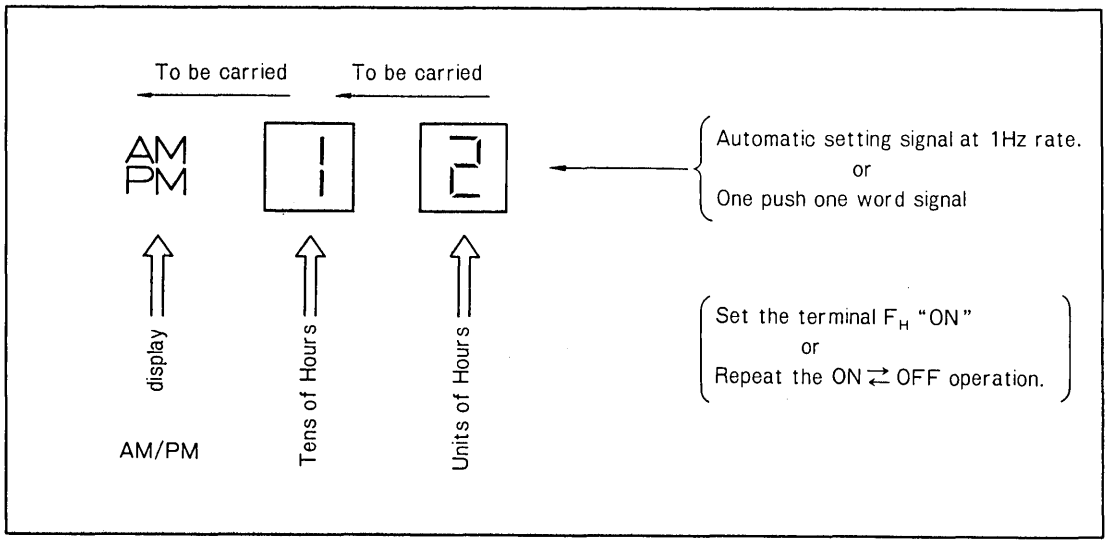


Fig.5

* The shifting of AM to PM and vice versa is made at 12 hours for the 12-hour indication.

② If you want to set hours faster for 12-hour indication, proceed with the following methods.
First, set the terminal F_S on and the terminal F_H on. Then, the AM/PM display can be set automatically at 1 pps. In other words, is shifted to PM and vice versa automatically.
If you are required to set AM/PM display faster than above, repeat the ON-OFF operation of the F_M terminal set to ON. Then, AM/PM display can be set at the speed of hand-operating.
Refer to the Fig. 6.

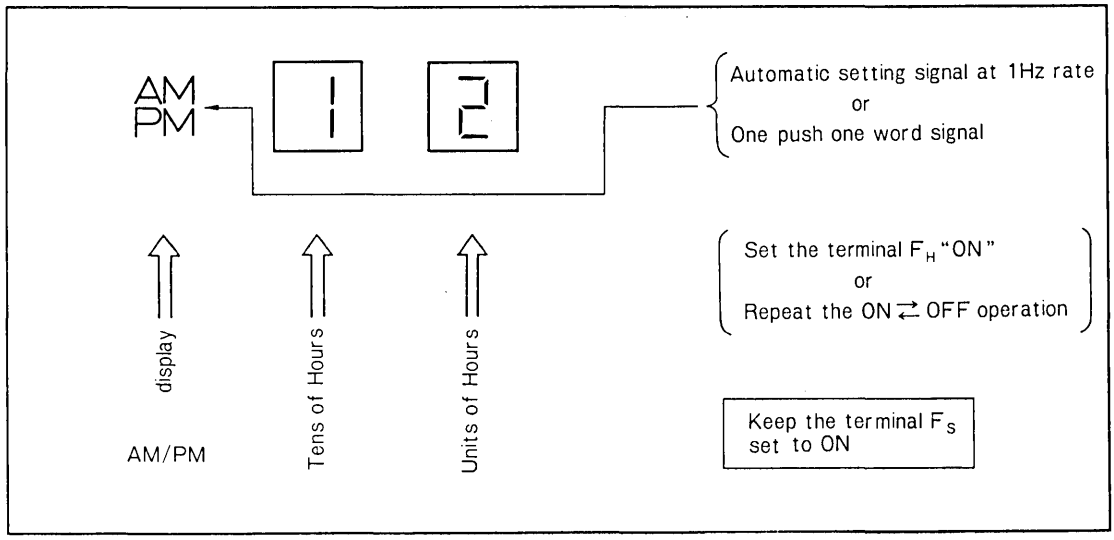


Fig.6

* An example of the setting of hours is given below for 12-hour indication.
Presuppose the display of hours is AM 11 and you want to correct it to AM 10. Fist, make the setting so that the display of hours becomes 10 in accordance with method 1 above. In this case, the display AM is shifted to FM with the overflown hours. This can be neglected. Then, set the display to AM in accordance with method 2 above. Through this operation with automatic setting signal at 1 pps, hours can be set within 13 seconds, in case where there is no erroneous setting. With the one push one word signal, hours can be set to the desired figure within 3 seconds.
As explained above, the setting of alarm time or control time for an electronic instrument requires only 7 seconds to complete even in the case of the longest set span.

3. Relationship between Ordinary Expression of Time and Expression of Time for μPD832G Series

The time can be displayed with μPD832G series either by 22-hour indication or by 24-hour indication. Table 1 shows the relationship between ordinary expression of time and expressions of times in 1-hour indication and 24-hour indication of μPD832G series.

Relationship between ordinary expression of time and
Expressions of times in 12-hour and 24-hour Indication

Ordinary expression of time	Forenoon	Afternoon
12 hours format	12 : 00AM~11 : 59AM	12 : 00PM~11 : 59PM
24 hours format	0 : 00 ~11 : 59	12 : 00 ~23 : 59

Ordinary expression of time	Twelve O'clock midnight	One O'clock in the morning	Two O'clock in the morning	Eleven O'clock in the morning	Twelve noon
12 hours format	12 : 00AM	1 : 00AM	2 : 00AM	11 : 00AM	12 : 00PM
24 hours format	0 : 00	1 : 00	2 : 00	11 : 00	12 : 00

One O'clock in the afternoon	Two O'clock in the afternoon	Three O'clock in the afternoon	Eight O'clock in the afternoon	Eleven O'clock in the afternoon	Twelve O'clock midnight
1 : 00PM	2 : 00PM	3 : 00PM	8 : 00PM	11 : 00PM	12 : 00AM
13 : 00	14 : 00	15 : 00	20 : 00	23 : 00	0 : 00

Table. I

4 Trial Sounding of Alarm Tone

Since the alarm time is set in accordance with methods 1 through 3 above, the alarm tone begins to be generated immediately from the terminal ALM OUT when the display corresponds to the present time of standard time in the course of setting of the hours with the terminals F_M, F_H and F_S. At this time, control signal (V_{DD} level) is also present at the CONT OUT terminal. But, in the course of further setting, if the display is deviated from the present time, the alarm tone stops sounding, and, at the same the control signal is also off.

On the contrary, with alarm time (or control time) fixed, if the standard time is set through the operation of the terminals F_M, F_H and F_S, the alarm tone begins to sound when the display corresponds to the alarm time fixed, and stops sounding when the display deviates from the alarm time fixed. This operation can be applied also to the control signal.

Such sounding of alarm tone as explained above may be called a very convinient trial sound of alarm.

* In other words, when the alarm is generated (at the same time, the control signal is also generated,) the alarm output (or control signal output) can be cancelled before the duration ends through the ON operation of the terminal F_M or F_H.

The cancellation of alarm tone is effective with the terminals F_M and F_H of either standard time or alarm timer.

The terminals F_S can generate alarm tone (or control signal) when the two hours correspond, but can not cancell the alarm tone (or control signal). There are the cases where the alarm tone (or control signal is off at the end of the duration brought by the carried minutes display when the time is between 30 and 50 minutes.

5. Setting of Alarm Time (or Control Time)

The alarm time (or control time) can be set to the any hours at an interval of one minute (resolusion: 1 minute). Once the alarm time is set, the alarm tone (or control signal) can be obtained every 24 hours at the preset time.

6. Durations of Alarm Tone or Control Signal

When the time of the alarm tone (or control signal) corresponds to the hours of standard time, the alarm tone of 2048 Hz frequency modulated by 8 Hz frequency is emitted every other second. The duration of alarm tone is 4 minutes. The alarm tone stops automatically at the end of duration and starts again at the same hours after 24 hours. The output waveform of the alarm tone is shown in Fig. 7.

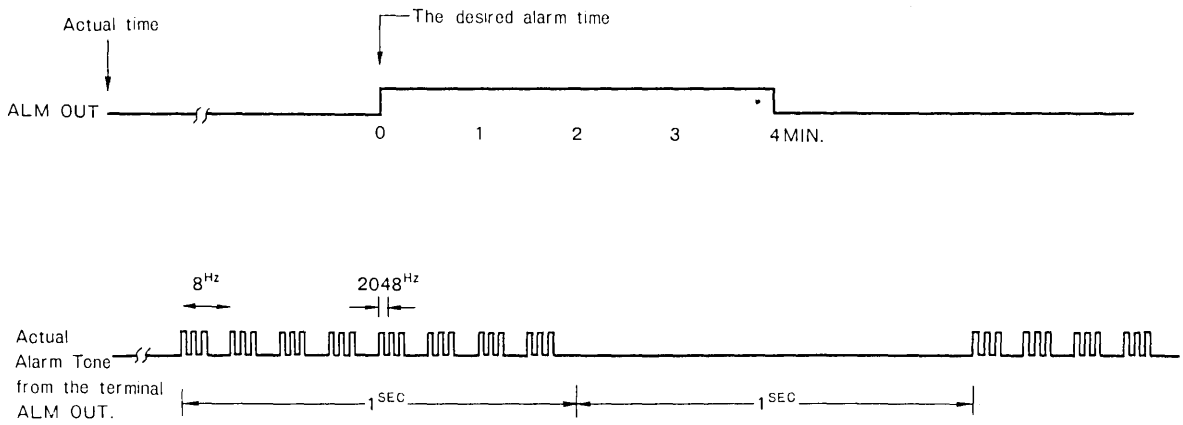


Fig.7

On the other hand, the control signal is present at the terminal CNT OUT. As shown in Table 2, there are four types of control duration, 16-minute, 32-minute, 64-minute and 128-minutes-durations. One of the four control durations can be selected in combination with the input terminals 60/30 and 60/120. Therefore, with those control signals, the recording is possible for 15-minute audio cassette tape to 2-hour video tape.

Terminal 60/30	L	H	L	H
Terminal 120/30	L	L	H	H
Duration (MIN)	64	32	128	16

L = V_{SS} level

H = V_{DD} level

Table 2

The relationship between the output waveforms at the ALM OUT and CONT OUT is shown in Fig. 8. In this case, the terminal SNZ is not operated. When the duration of control signal ends, the control signal stops and does not start again until the pre-set time reaches after 24 hours.

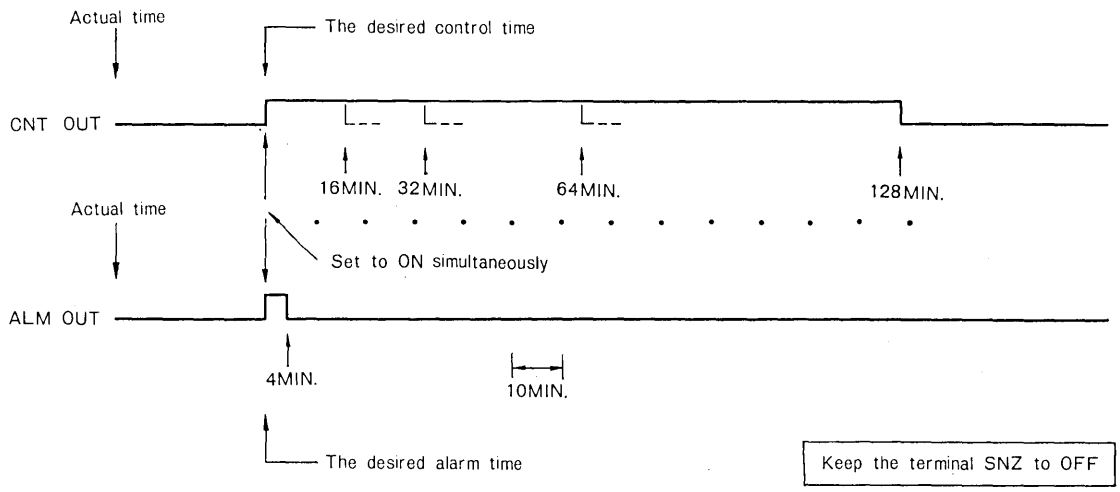


Fig.8

7. Relationship between SNZ Terminal and Alarm Tone (Control Signal)

When the hours of standard time corresponds to the pre-set hours for the alarm time, the alarm tone (or control signal) is generated. The alarm is automatically off in four minutes. The control signal is off at the end of pre-set duration (15 minutes, 30 minutes, 60 minutes and 120 minutes). If you want to take a snooze while the alarm tone is on, set the terminal SNZ to on, then, the alarm is simultaneously off. The alarm tone is on again after 4^{+0}_{-1} minutes from the OFF operation of the terminal SNZ. The operation of the terminal SNZ to stop the alarm tone and start it again three or four minutes later as explained above is referred to as the cancel-refresh method.

The duration of cancel-refresh operation of alarm tone is extended every terminal SNZ operation. Even though the cancel-refresh method is employed, the alarm tone is not on again if it is lasts fully for four minutes.

The cancel-refresh method is to be applied to the protable alarm timer (or traveller's watch) with its built-in μPD832G series which is expected to be commercialized in feature for the purpose of preventing the battery from discharging uselessly while the user keeps the timer away, levaing it on.

The relationship in operation between the terminals ALM OUT and SNZ is shown in Fig. 9.

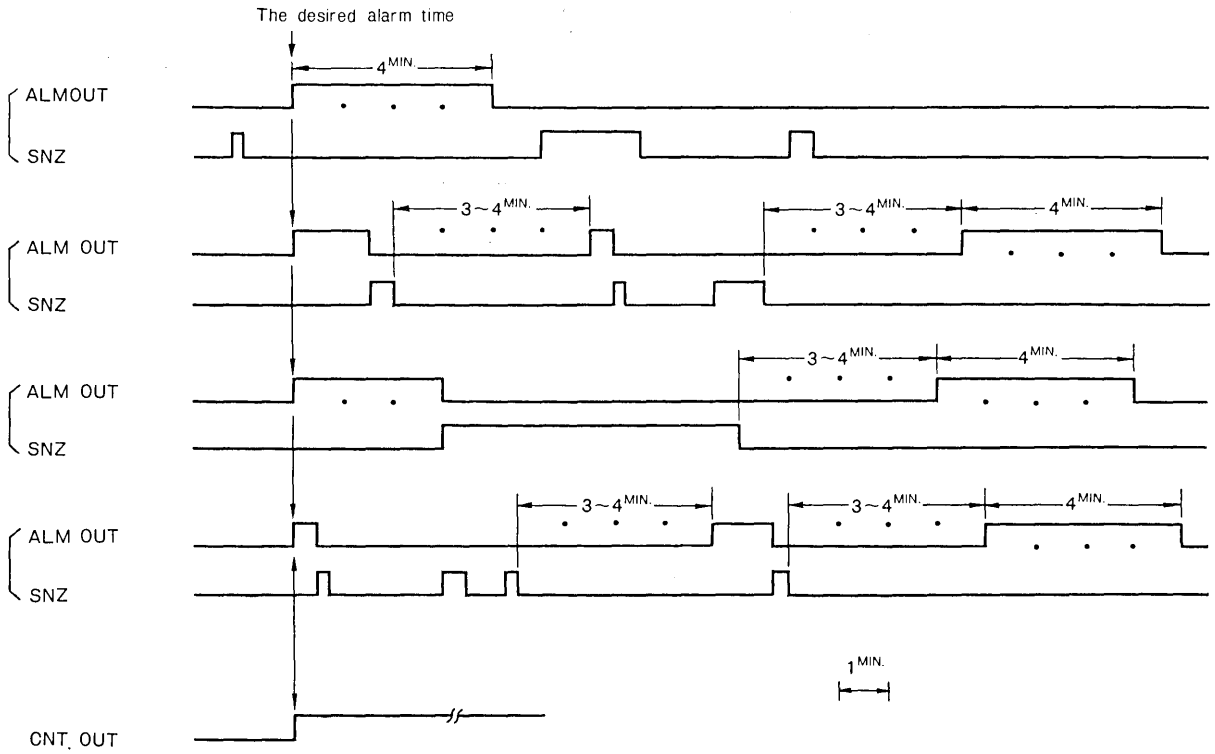


Fig 9. Relationship in operation between the terminals ALM OUT and SNZ.

Even though the control signal from the terminal CNT OUT is not off through the ON operation of the terminal SNZ, the duration of control-signal is extended. In other words, the ON operation of the terminal SNZ resets the duration circuit for the control signal. From the instance the terminal SNZ is off, the counting of control signal duration starts. The counting is effective up to 16^{+0}_{-1} minutes for the 15-minute duration, 32^{+0}_{-1} minutes for the 30-minute duration, 64^{+0}_{-1} minutes for the 60-minute duration and 128^{+0}_{-1} minutes for the 120-minute duration.

Fig. 10 shows the relationship in operation between the terminals CNT OUT and SNZ on the basis of 32-minute duration. As can be understood from the figure, the duration of control signal can be extended through the ON operation of the terminal SNZ.

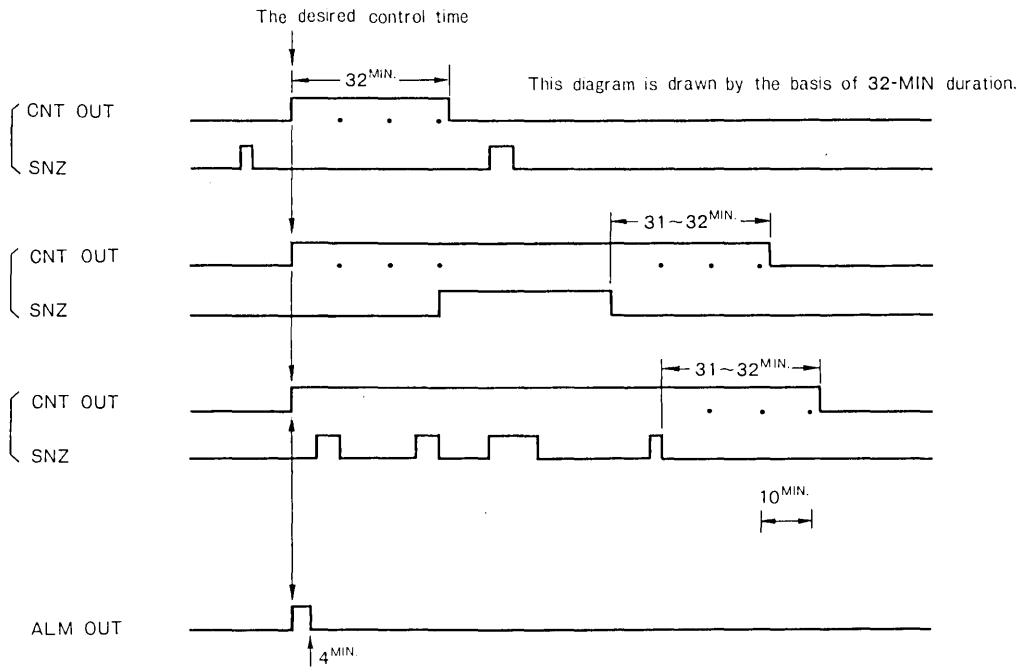


Fig. 10. Relationship in between the terminals CNT OUT and SNZ.

8. Stopping the Alarm Tone (or Control Signal)

When you need to stop and clear the alarm tone (or control signal) completely, set the terminal ACS to ON.

If the terminal ACS is off after clearing the alarm tone (or control signal), it is on again at the pre-set hours after 24 hours.

* If the alarm tone (or control signal) is not required every 24 hours, proceed with the following steps.

1. Disconnect the terminal ALM OUT from the alarm tone source.
2. Set the volume of alarm tone to the minimum.
3. Disconnect the terminal CNT OUT from the controlled electronic instrument.
4. Keep the terminal DUT set to V_{DD} level.
   ..... In this case, the memory operates as dual time.
5. Keep the terminal STW set to V_{DD} level.
   ..... In this case, the memory operates as stopwatch.

* While the sleep timer is in use, the alarm timer can not be used. (In this time, the control signal is also on from the terminal CNT OUT.) In other words, while the sleep timer is in operation, the alarm timer does not emit the alarm tone even though the pre-set time corresponds to present hours.

6–4. Snooze Timer

When you want to take a snooze a little longer after the alarm tone starts, set the terminal SNZ to ON. Then, you can take a snooze for three to four minutes.

In addition to the application and operation previously explained in the preceeding paragraph for the alarm timer, the snooze timer is applicable to the follwings.

By making the oscillator frequency programable with μPD833G a notifying tone (or calling bell) can be produced at a regular interval. When the notifying tone is heard, set the terminal

SNZ ON and OFF.

The main oscillator signal frequencies and duration of notifying tone are as shown in Table below.

Oscillator Frequency	Interval of Notifying Tone	Pulse at ALM OUT Terminal
65.536 kHz	Every 2 minutes	8-burst pulse every 0.5 Sec
32.768 kHz	Every 4 minutes	8-burst pulse every other Sec
16.384 kHz	Every 8 minutes	8-burst pulse every2.0 Sec
8.192 kHz	Every 16 minutes	8-burst pulse every 4.0 Sec
4.906 kHz	Every 32 minutes	8-burst pulse every 8.0 Sec
2.048 kHz	Every 53 minutes (Approx. 1 hrs.)	8-burst pulse every 16 Sec
1.024 kHz	Every 128 minutes (Approx. 2 hrs.)	8-burst pulse every 32 Sec
512 kHz	Every 256 minutes (Approx. 4 hrs.)	8-burst pulse every 64 Sec
256 Hz	Every 512 minutes (Approx. 8.5 hrs.)	8-burst pulse every 128 Sec
.	.	.
.	.	.
.	.	.
.	.	.

Be sure to set the terminal SNZ ON and OFF. Then, the notifying tone stops immediately. In this case, the notifying tone can be heard again after the specified interval. (In case of 1.024 signal frequency, the notifying tone is heard again after two hours.)

The snooze timer is effective for use as a timer to notify such regular interval of hours as required for the application of drops to a patient, the sackling of an infant, the medication to a patient, etc.

6–5. Sleep Timer

The sleep timer offers such conveniecnes that the user can sleep listening in mood music or classic music, or appreciating a theatrical performance through the radio or television.

1. How to set Sleep Timer

To set the sleep timer, connect the terminal SLP OUT to such electronic instrument as television, radio, etc. Then, switch the electronic instrument on. Next, set the terminal SCI to ON. The sleep timer automatically controls the electronic instrument at the end of pre-set duration (15 minutes, 30 minutes, 60 minutes or 120 minutes).

Even though the terminal SCI is kept to ON, the SCI signal inside the LSI is driven by the single pulse of approximately 8-ms width. Thus, the button switch (single pole single through switch) should be used. The duration is similar to that of control signal. When determining the duration, use the 60/30 and 60/120 terminals as shown in Table 3.

Terminal 60/30	L	H	L	H
Terminal 60/120	L	L	H	H
Duration with the use of the terminal SCI (MIN)	63~64	31~32	127~128	15~16

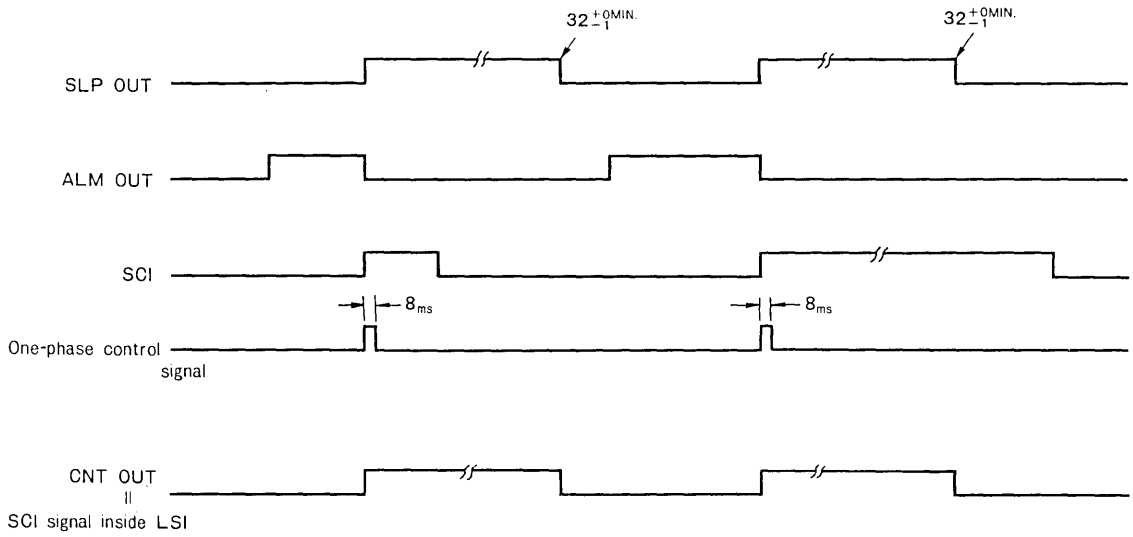
Table 3.

L = V_{SS} level

H = V_{DD} level

The available durations ranging from 15 to 120 minutes offers the conveniences so much to the users.

The sleep timer has the priority in setting the hours over the alarm timer. Thus, the alarm tone stops immediately after the ON operation of the terminal SCI, and the sleep signal is emitted instead from the terminal SLP OUT. At the same time, the control signal (one phase control signal) is emitted from the terminal CNT OUT. Refer to Fig. 11 for the time chart of the signals to be emitted.



This diagram is drawn by the basis of 32MIN duaration

Fig. 11

If you want to stop and clear the sleep timer completely, during the application, set the terminal ACS to ON.

* The sleep timer has no display for the lapse of hours. If the memory is set so that the time is used as dual time or stopwatch and let it start counting instanteneously after the terminal SCI is on, the lapse of hours can be displayed for the sleep timer.

* When the alarm timer is used, it should be set to the time one minute or more later than the end of duration for the sleep timer. Then, the sleep timer and alarm timer can be set together.

* When the alarm timer is set to a certain hours in the duration of sleep timer, if the standard time corresponds to the alarm time, the alarm is not on until it reaches again at same hours after 24 hours. The sleep timer does not operate, unless the terminal SCI is set to ON, whenever using the sleep timer.

* The sleep timer is effective, when the memory is not used as alarm timer (or control timer for electronic instrument), as dual timer (with the terminal DUT set to V_{DD} level) or stopwatch (with the terminal STW set to V_{DD} level). In other words, the sleep timer can be used as independent 3-channel timer in parallel with the combinations of 1 standard time, dual timer and sleep timer, and 2 standard time, stopwatch and sleep timer.

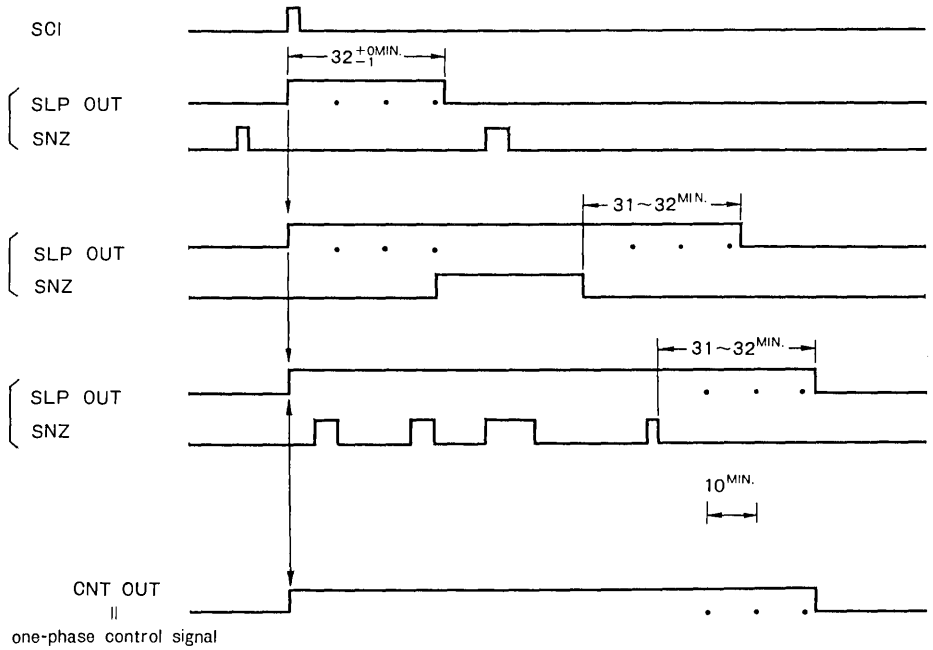
2. Applications of Sleep Timer

In addition to its proper applications as sleep timer, it can be used for slot machines to determine the duration of service with the coin or the equivalent in shape. Among those slot machines are massaging machine, cooler, gas range, game machine, telescope, etc. of coin timer type.

3. Relationship between Terminal SNZ and Sleep Signal

The ON operation of the terminal SNZ does not disconnect the sleep signal, but it extends its duration. In other words, the ON operation of the terminal SNZ resets the duration circuit for the sleep signal.

From the instance the sleep signal is off, the duration for the control signal is counted. The counting is effective for 16^{+0}_{-1} minutes for 15-minute duration, 32^{+0}_{-1} minutes for 30-minute, 60^{+0}_{-1} minutes for 60-minute and 128^{+0}_{-1} minutes for 120-minute. This operation of terminal SNZ is quite similar to that of terminal CNT OUT explained in the preceeding paragraph. Fig. 12 shows the relationship in operation between the terminals SLP OUT and SNZ on the basis of 32-minute duration.



This diagram is drawn by the basis of 32MIN duration

Fig. 12

4. 2-Phase Control Signal

The ON operation of the terminal SCI produces the sleep signal from the terminal CNT OUT. In addition to the sleep signal, the control signal (one-phase control signal) is also obtained from the terminal CNT OUT. Therefore, if the control time is set to the hours out of the duration of the one-phase control signal, the two-phase control signal can be obtained as shown in Fig. 13. Thus, a multitimer can be established. In this case, sleep signal, one-phase control signal and two-phase control signal are same in duration. In other words, the duration is determined in combination with terminals 60/30 and 60/120. Refer to Table 2 and 3.

The multi-timer which can be obtained by triggering the terminal SCI with the trigger pulse signal produced by the separate IC is shown in Fig. 13.

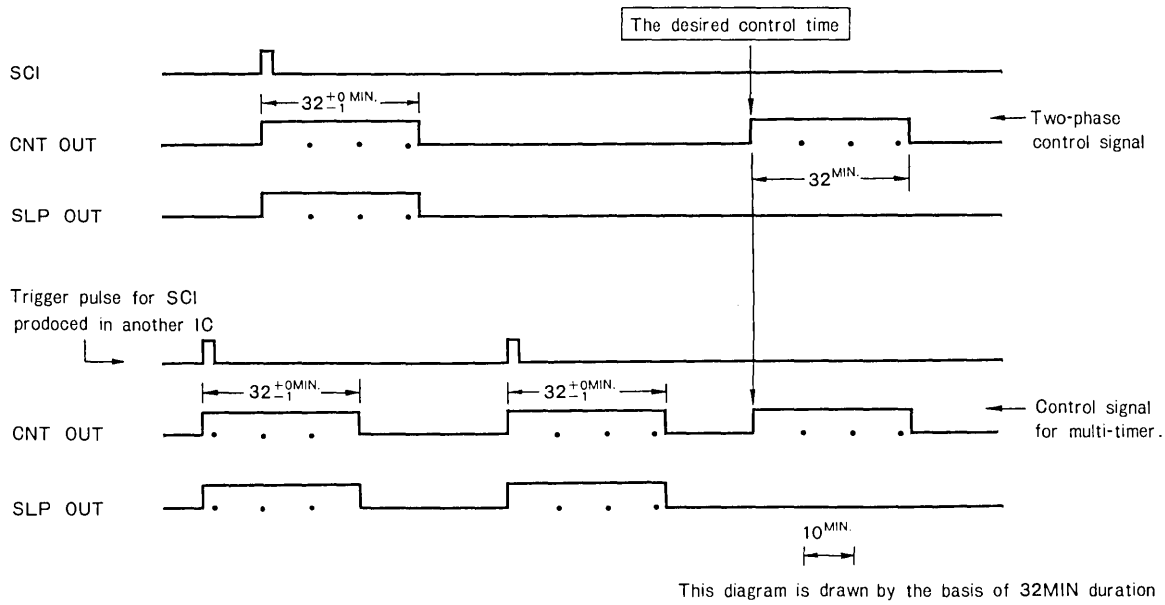


Fig. 13

* The durations of one-phase control signal and 2-phase control signal are extended when the terminal SNZ is set to ON. This is same in operation as explained in the preceeding paragraph.

6–6. Dual Time

1. Display

With the terminal DUT set to V_{DD} level, the memory is used as dual time. If you want to see the ALS terminal to ON. Then, the dual time (Fig. 2, (2), ii) is displayed regardless of the displays for Normal and seconds (Fig. 2, (1), i and ii).

In case of alarm timer (or control timer), a statical display of hours are presented with the dot illuminating. But the dot flashing every other second for the dual time. The dual timer has no display for seconds. The resolution as the dural time is one minute.

2. How to set the Dual Time

The method of time setting is similar to that of alarm timer (or control timer as explained in Item 2 of Paragraph 6–3).

3. Applications of Dual Time

(1.) Dual time is an optimum traveller's watch when it is used as a time for displaying the time differential (or as a part of world timer).
It can be used to constitute an independent 3-channel timer in combination with standard timer and sleep timer.

(2.) Dual time can be used as a time to measure the lapse of hours. In case of 12-hour indication, AM 12 hours are interpreted as 0 (zero) hour. If the display on the dual time is AM 3 hours 25 minutes, the amount of lapse of time is 3 hours and 25 minutes, and if the dual time displays PM 12 hours 40 minutes, it indicates that 12 hours and 40 minutes have passed.
The display succeeding PM 1 should be added 12 hours for the counting of the amount of laspe of time. For examle, it the display on the dual time is PM 3 hours 58 minutes, the amount of laspe of time is 15 hours 58 minutes (3 hours 58 minutes +12 hours).
In case of 24-hour indication, the counting is made from 0 hour as the cardinal point. Thus, no addition is required to obtain amount of lapse of time. Table 4 shows the relationship between 12-hour indication and 24-hour indication for the display of amount of laspe of time.

12-hour format (HRS)	AM 12	AM 1	AM 2	AM 3	AM 4	AM 5	AM 6	AM 7	AM 8	AM 9	AM 10	AM 11
24-hour format (HRS)	0	1	2	3	4	5	6	7	8	9	10	11

PM 12	PM 1	PM 2	PM 3	PM 4	PM 5	PM 6	PM 7	PM 8	PM 9	PM 10	PM 11
12	13	14	15	16	17	18	19	20	21	22	23

Table.4

6–7. Stopwatch

1. Display

When the terminal STW is set to V_{DD} level, the memory is provided with the function of stopwatch. To see the display of stopwatch, set the terminal ALS to ON. Then, the stopwatch (Fig. 2, (2), iii) is displayed regardless of displays on the standard time (Fig. 2, (1), i and ii). The stopwatch is provided with displays of seconds and minutes. The minutes is displayed on the space for hours and the seconds, on the space for minutes.

The dot flashing every other second for the display of seconds on the standard time. But the colon is illuminated for the stopwatch.

2. Application of Stopwatch

When using the stopwatch, keep the terminal STW set to V_{DD} level and set the terminal ALM to ON. Then, the stopwatch is ready for operation. At this time, if the F_M terminal is set to ON, the display is reset to 00 minute 00 seconds and hold as it is. The start-stop operation is made through the use of the terminal F_H. The stopwatch can count up to 23 minutes 59 seconds.

In case of 12-hour indication, the display succeeding to 9 minutes 59 seconds is ^{AM}10 minutes 00 second, and AM indicates that the count reaches 10 minutes. The display $^{AM}_{FM}$0 minute 00 second comes next to ^{AM}19 minutes 59 seconds. In this case, $^{AM}_{PM}$ represents 20 minutes. Fig. 14 will help you understand the method of display explained above.

In case of 24-hour indication, the display is made in digit from 0 minute 00 second to 23 minutes 59 seconds.

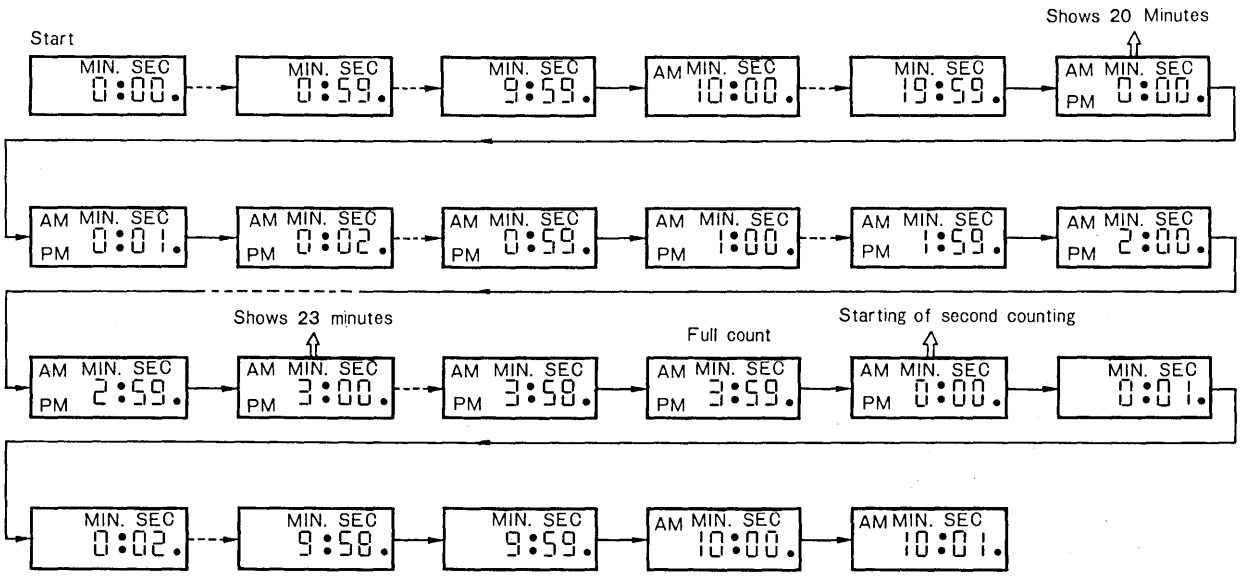


Fig. 14

* Since the terminal F_H offers the start-stop (hold) operation of stopwatch, the measurement can be made without counting the time wasted.

6–8. Counter

Counter is an article used in reckoning and can keep counting the number of people entered in a certain place, quantity of items unloaded, amount of traffic at the specific place, calling a roll of pupils, etc.

The function of counter is not designed independently, but is incidentally produced from the stopwatch explained in Paragraph 6–7. Therefore, its capacity is 720 counts (12 x 60) for 12-hour indication and 1440 counts (24 x 60) for 24-hour indication.

The counter for 24-hour indication which is provided with re-cycle count mechanism may be more convinient to use than that for 12-hour indication.

1. Application

First keep the terminal ALS set to V_{DD} level. In this case, the alarm (or control) time is displayed for any hours.

Then, set the terminal STW to ON to obtain the display of stopwatch, and perform ON-OFF operation of the terminal F_M to obtain indication shown in Fig. 2, (2), iv. Finally, set the terminal STW to OFF. The counter is ready for use.

The terminal STW is set to ON for every counting. The stopwatch starts operating when the terminal STW is switched over from OFF to ON. Thus, the terminal STW should be set to the OFF when the stopwatch is not in use.

Be sure to insert the circuit for preventing the terminal STW from chattering into its input circuit as shown in Fig. 15. The use of common terminal for the signal to drive the liquid crystal is required for the synchronization on the LSI circuit to shift the display from 19:59 to 20:00 count for 24-hour indication.

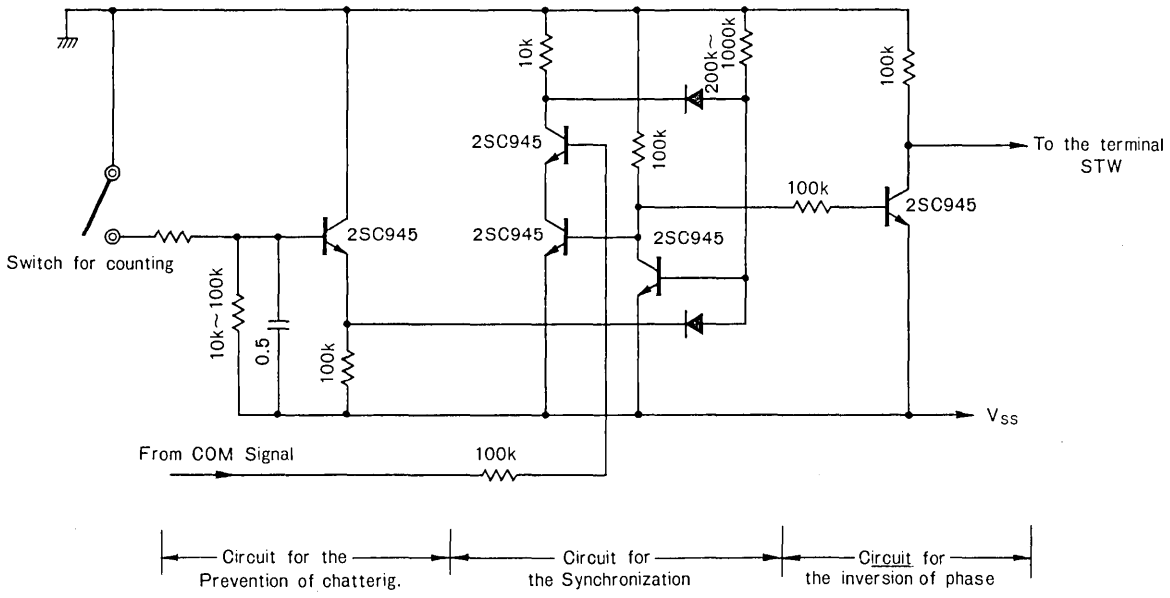


Fig. 15

As the summary to the explanation for every channel, Fig. 16 shows the relationships between the terminal DUT and dual time, that terminal STW and stopwatch, the terminal ALS and alarm (or control) timer, and the terminal SEC and standard time.

Input terminal	Memory															
	Alarm timer or Control timer				Dual time								Stopwatch			
DUT	L		L		H		H		H		H		L		L	
STW	L		L		L		H		L		H		H		H	
ALS	L		H		L		L		H		H		L		H	
SEC	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
	MIN • HRS	MIN • SEC	Alarm or Control Time		MIN • HRS	MIN • SEC	MIN • HRS	MIN • SEC	Another Time		Another Time		MIN • HRS	MIN • SEC	Stopwatch	
	Standard Time				Standard Time		Standard Time						Standard Time			
The state of Display																

H=V_{DD} level
L=V_{SS} level

Fig. 16

7. Test

Set the every inpt terminal to V_{SS} level and insert the specified oscillator frequency into OSC IN, (42 MHz for μPD832G and 32 kHz for μPD833G), and set the terminal TST_1 to ON. Then, the LSI is ready for test.

① Set the terminal F_S to ON. Then, the standard time and memory are reset (completely cleared). In this case, standard time and alarm timer display 1 hour 00 minute (00 second) for 12-hour indication and 0 hour 00 minute (00 second) for 24 hour indication.

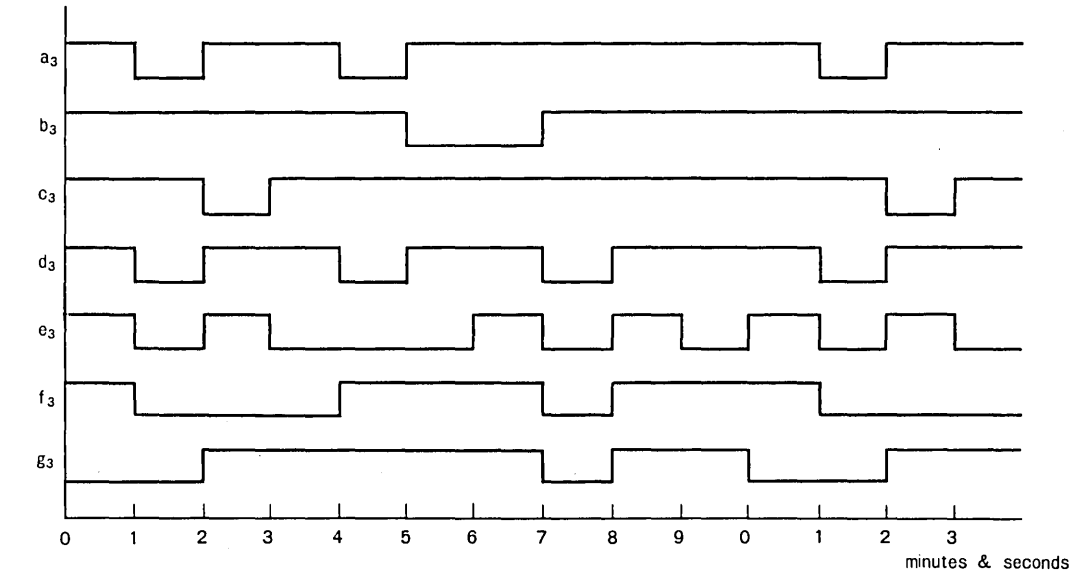
② Set the terminal F_S to OFF and the terminal F_M to ON. Then, the frequency 32 kHz is directly applied to the divider (5-th stage) whose proper input signal is 2.048 kHz. As a result, the second counter of standard time is carried fast at approximately 16 Hz for test.

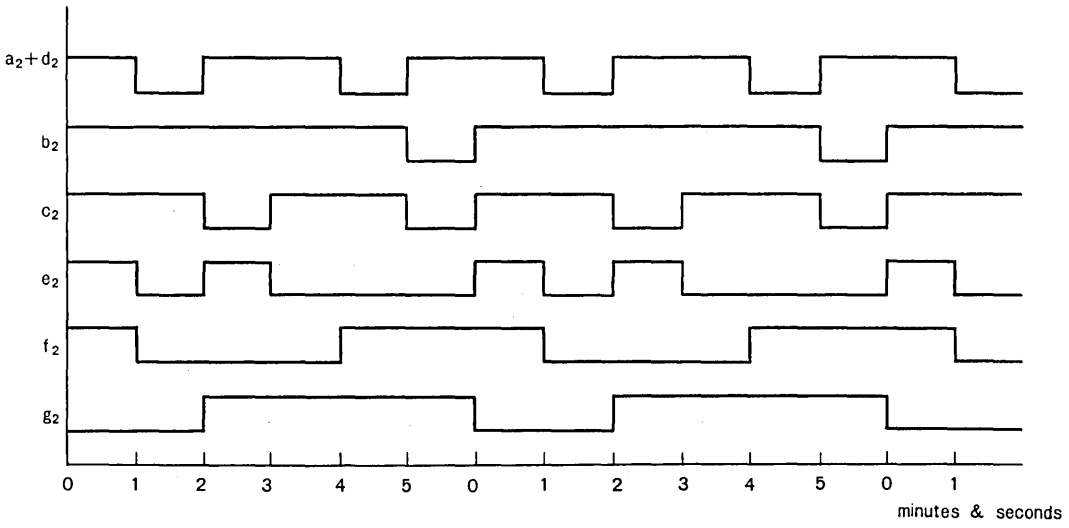
③ Set the terminal F_M OFF and the terminal F_H ON. Then, the second counter of standard timer can be tested at a high speed at approximately 2.048 kHz and the fast shifting of minute counter can be tested at approximately 30 Hz. In this case, if the terminals DUT and ALT are set to ON. The minute counter of memory can be tested fast with 30 kHz frequency. Then, the hour counter is tested at approximately 0.57 Hz.

④ When the terminals F_M and F_H are on, the high speed test of second counter can be tested at 32.768 kHz the high speed test of minute counter tested at approx. 500 Hz and the high speed test of hour counter test at about 9 Hz. In this case, if the terminals DUT and ALS are on, the high speed test of minute counter of memory can be made at approximately 500 Hz. The high speed test of hour counter of memory can be made at approx. 9 Hz.

⑤ In case of μPD832G the output is available the frequency 32.768 kHz from the terminal TST_2 that it is one cycle of the oscillator frequency divided by 27.
And then, the terminal TST_2 is provided which facilitates high-speed testing too. High-frequency pulses driving the TST_2 input allow for high-speed testing of the seconds, minutes and hours counters.

Minute & Second Display

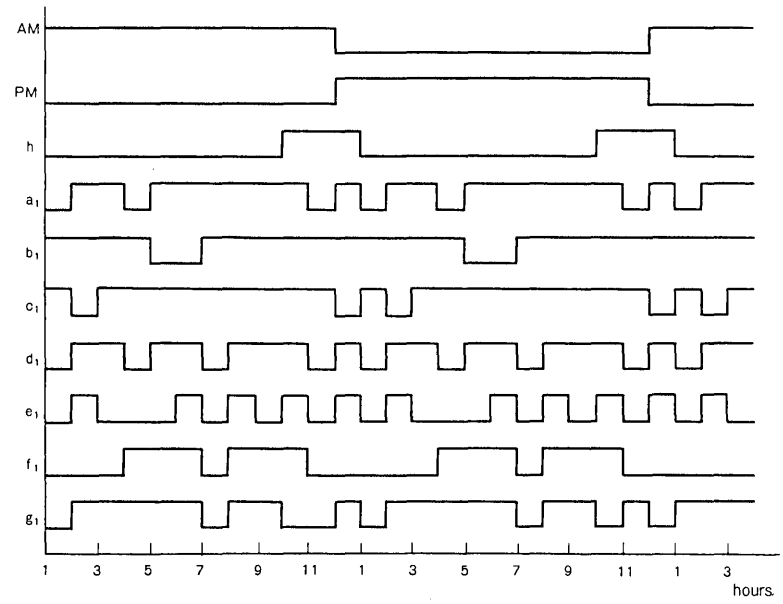




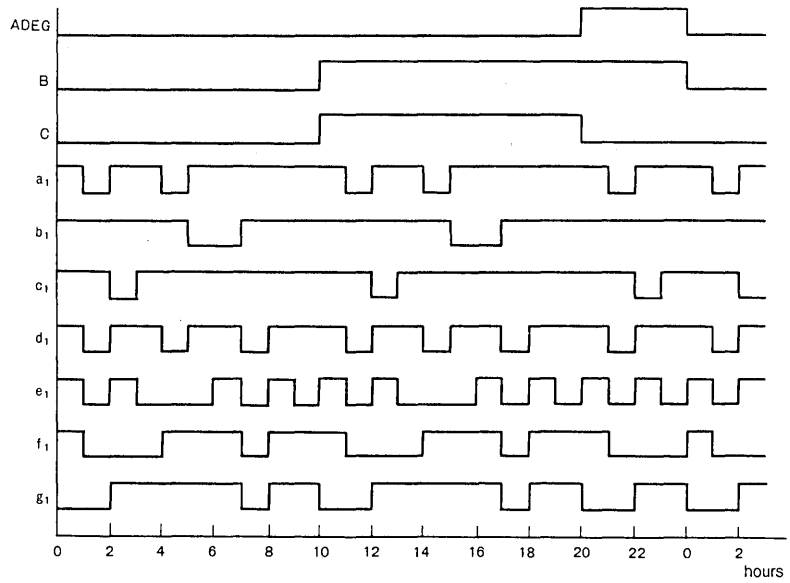
Output waveforms of segments

(When the level is "H", 32Hz of opposite phase to COMMON is outputed for the segments, and when the level is "L", 32Hz of the same phase is outputed.)

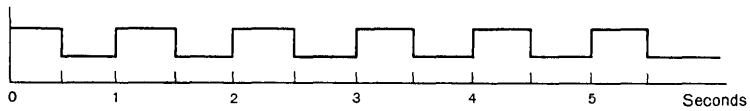
Hours Display of 12 Hour Format



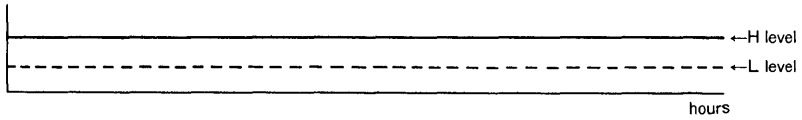
Hours Display of 24 Hour Format



Dot(1 Hz)

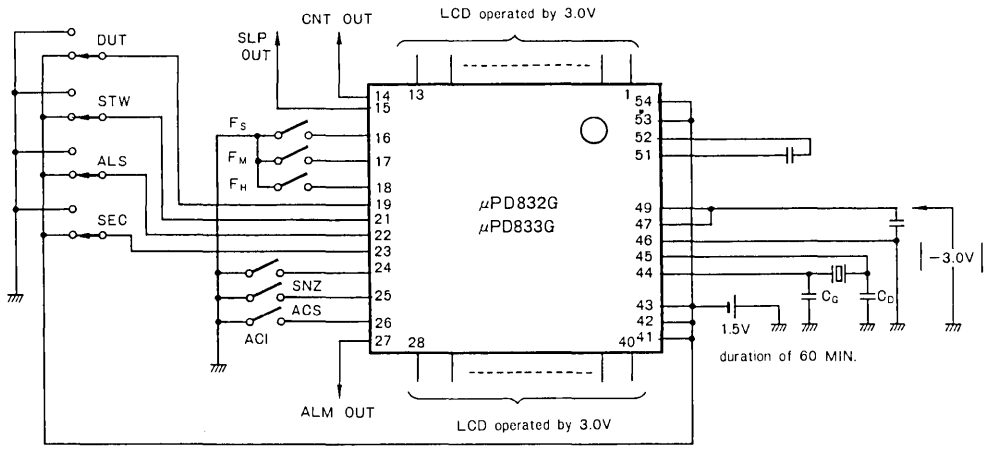


COLON($\overline{COM}$)

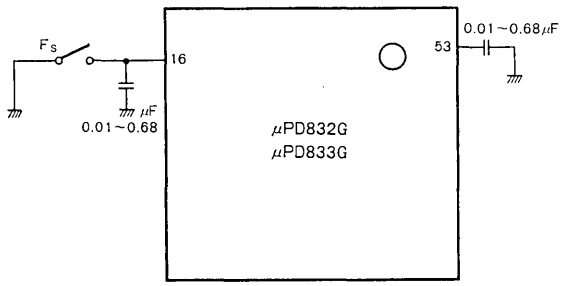


APPLICATION

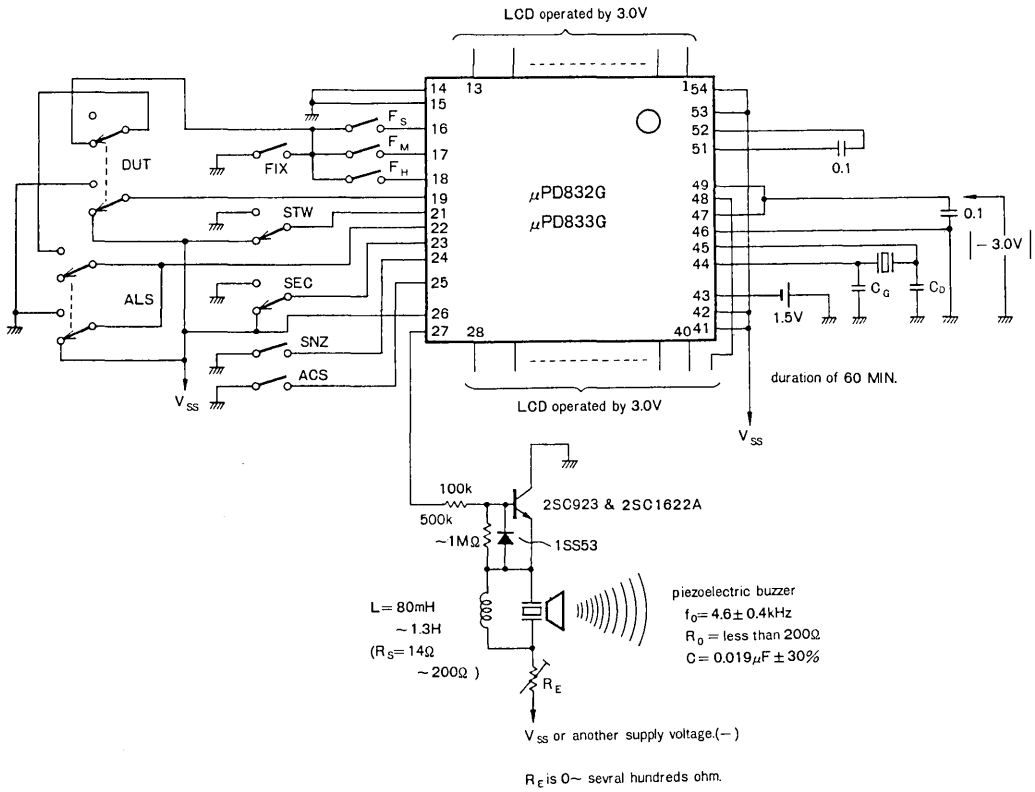
1. Application circuit for doubler



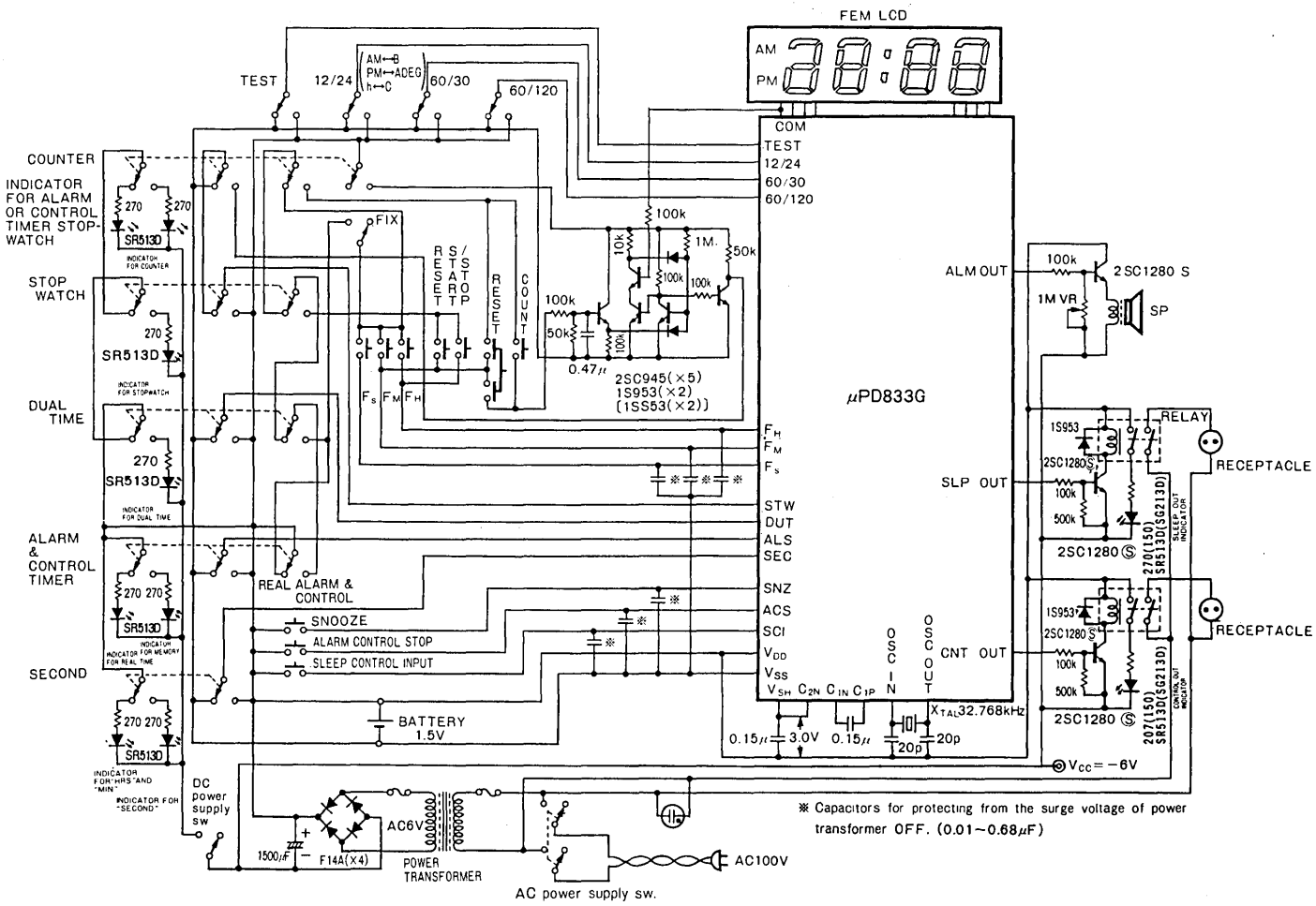
2. How to operate auto clear



3. Application circuit for alarm clock with dual time and stopwatch



4 Application circuit for 8 channel function



MATTERS DEMAND SPECIAL ATTENTION !

① Make μPD832G and μPD833G pack by aluminum foil certainly when be carred or be kept.

② The input terminals be unused connect to V_{SS} always.

MOS DIGITAL INTEGRATED CIRCUIT
μPD2006G

QUARTZ-OPERATED ELECTRONIC CLOCK
CMOS LSI

The captioned Model 2006G CMOS LSI has been developed for FIP (Fluorescent Indicator Panel)/LED-operated quartz clock, which is operated at the reference frequency of 32.768 kHz.
The model μPD2006G allows the direct operation of both FIP and LED.
The package type is 54 pin flat package.

FEATURES

- Direct FIP/LED operation.
- Clock counter is operated with 1.5 V, and can be backed up by battery.
- Alarm timer, sleep timer, control timer, stop watch and dual time functions are provided.
- Control time limit can be set to 16, 32, 64 or 128 minutes.
- Time signal tone can be output.

FUNCTIONS

1. Standard Time
2. Alarm Time
3. Snooze Timer
4. Sleep Timer
5. Control Timer
6. Dual Time
7. Stop Watch

ABSOLUTE MAXIMUM RATINGS (Ta=25 °C, V_{DD}=Common)

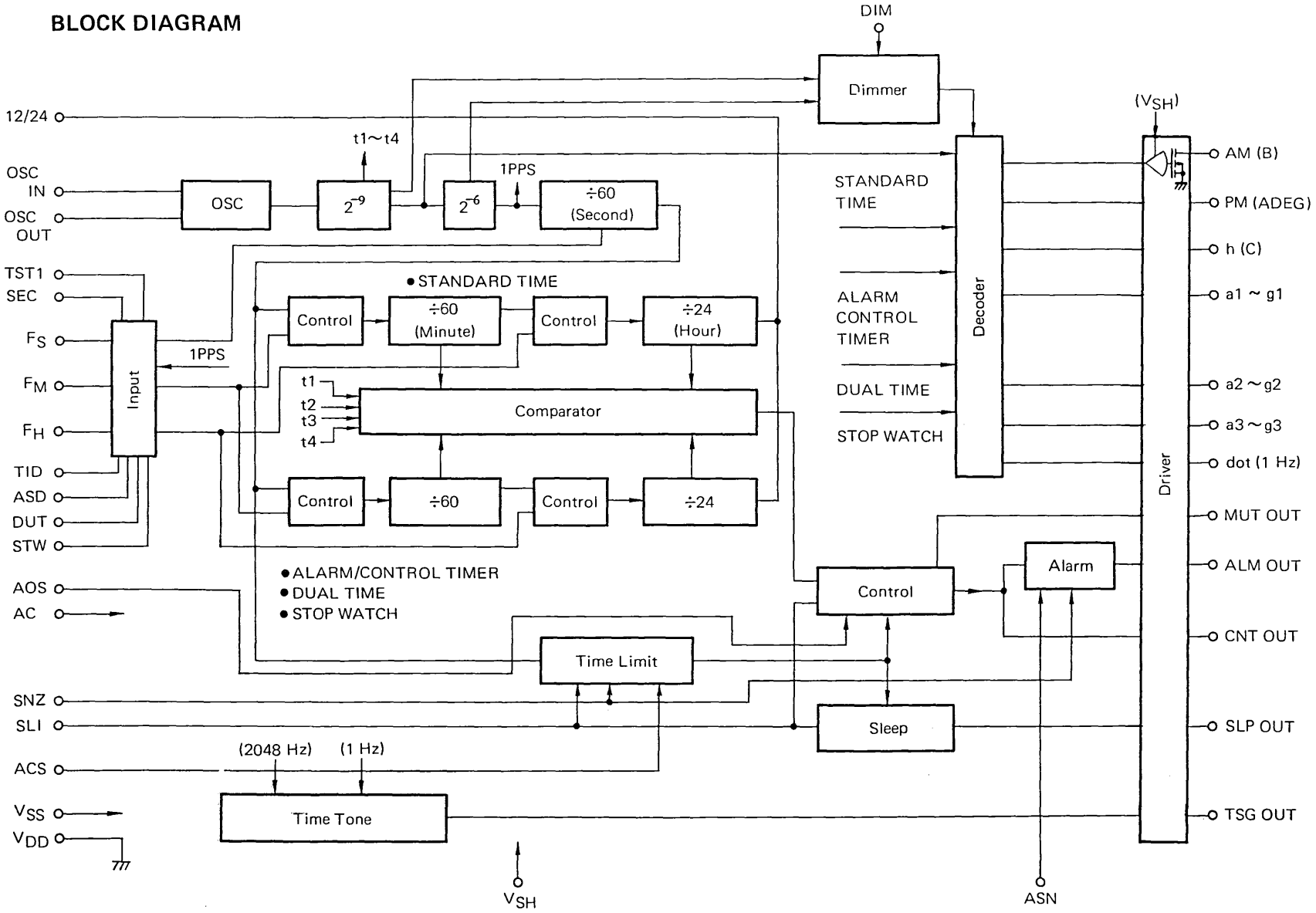
Supply Voltage	V_{SS}	−3.0	V
Supply Voltage	V_{SH}	−30.0	V
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

(f=32.768 kHz, V_{DD}=Common, V_{DD}-V_{SS}=1.5 V, C_D = 5 ~ 40 pF, C_G = 5 ~ 30 pF)

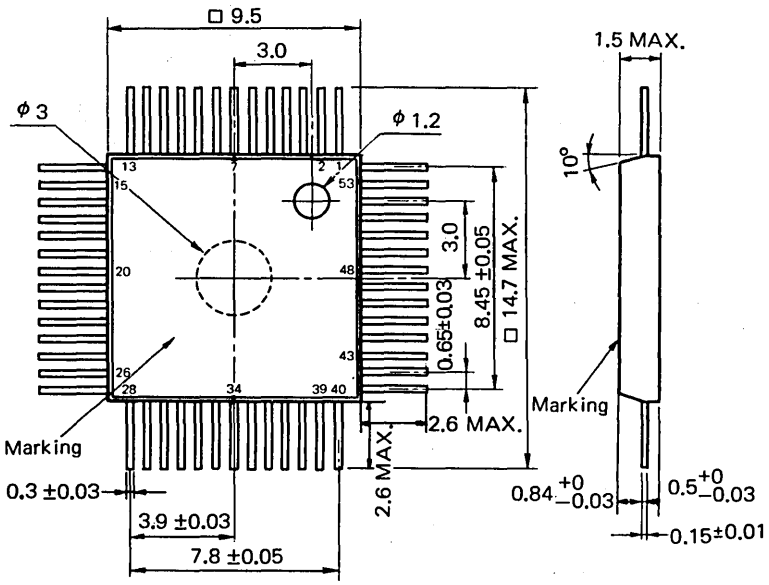
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Operating Voltage	$V_{DD}-V_{SS}$	1.2	1.5	2.0	V	Ta=−20 to +75 °C
Total Current Consumption	I_{SST}		2.0	5.0	μA	No load
Osc. Start Voltage	V_{STA}			1.35	V	T_{STA} = 10 s, C_G = C_D = 20 pF
Operating Voltage	$V_{DD}-V_{SH}$	9		26	V	Ta=−20 to +75 °C
Segment Out Current	I_P	5			mA	V_{DD}-V_{SH}=20 V, V_{DS}=2 V
h & 1Hz Seg. Out Current	I_P	8			mA	V_{DD}-V_{SH}=20 V, V_{DS}=2 V
PM Seg. Out Current	I_P	16			mA	V_{DD}-V_{SH}=20 V, V_{DS}=2 V
Alarm & Control & Sleep Output Current	I_P	500			μA	V_{DD}-V_{SH}=20 V, V_{DS}=2 V
MUT & Time Tone Output Current	I_P	500			μA	V_{DD}-V_{SH}=20 V, V_{DS}=2 V

BLOCK DIAGRAM



PACKAGE DIMENSIONS

(Unit: mm)

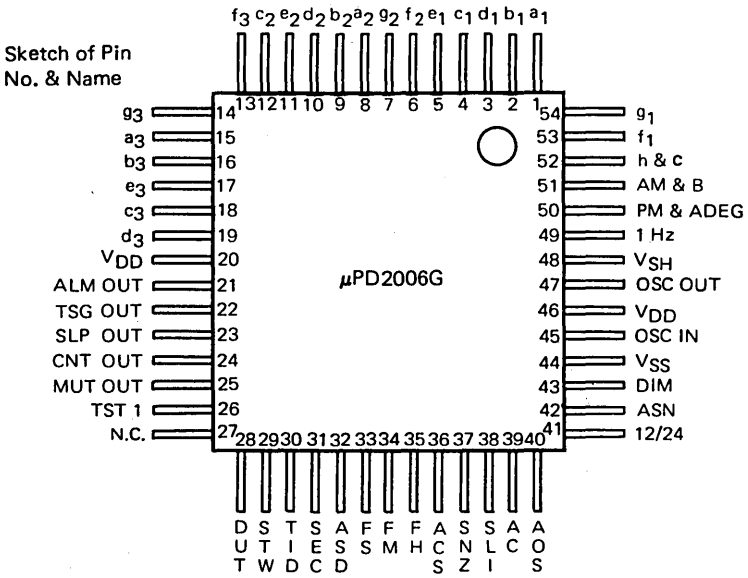


Terminal No. & Name

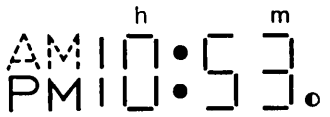
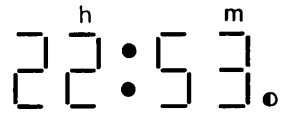
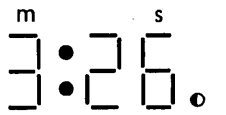
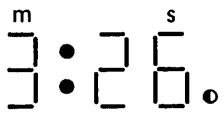
No.	Name	No.	Name
1	a_1	28	DUT
2	b_1	29	STW
3	d_1	30	TID
4	c_1	31	SEC
5	e_1	32	ASD
6	f_2	33	FS
7	g_2	34	FM
8	a_2	35	FH
9	b_2	36	AOS
10	d_2	37	SNZ
11	e_2	38	SLI
12	c_2	39	AC
13	f_3	40	AOS
14	g_3	41	12/24
15	a_3	42	ASN
16	b_3	43	DIM
17	e_3	44	V_{SS}
18	c_3	45	OSC IN
19	d_3	46	V_{DD}
20	V_{DD}	47	OSC OUT
21	ALM OUT	48	V_{SH}
22	TSG OUT	49	1 Hz
23	SLP OUT	50	PM & ADEG
24	CNT OUT	51	AM & B
25	MUT OUT	52	h & C
26	TST 1	53	f1
27	N.C.	54	g1

N.C. = No Connection

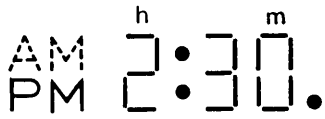
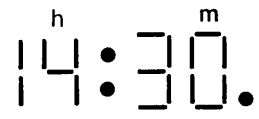
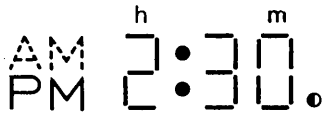
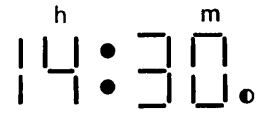
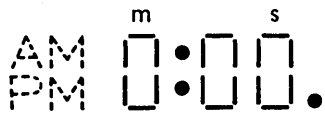
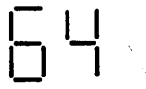
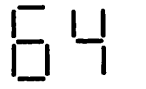
Sketch of Pin No. & Name



(1) Standard Time

Display	12-Hour Display	24-Hour Display	Active Term.
(1) Ordinary Display			
(2) Second Display			SEC

(2) Memory

Display	12-Hour Display	24-Hour Display	Active Term.
(i) Alarm/Control Time			ASD
(ii) Dual Time			DUT ASD
(iii) Stop Watch			STW ASD
(iv) Time Limit			TID

◐ indicates an intermittent display of the dot every second.

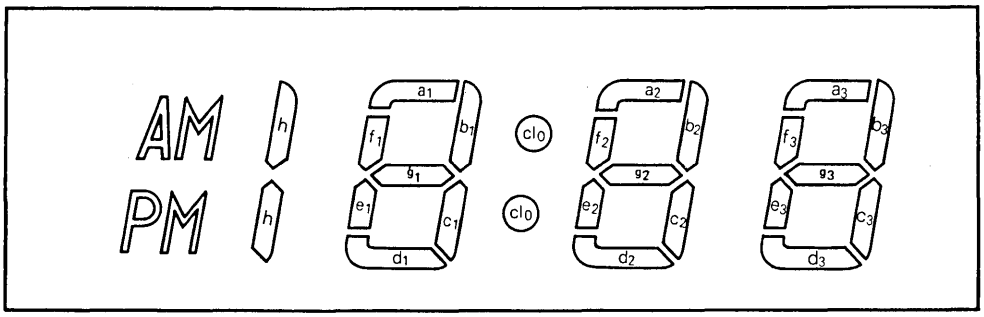
● indicates the dot kept on.

: } indicates the colon kept on.

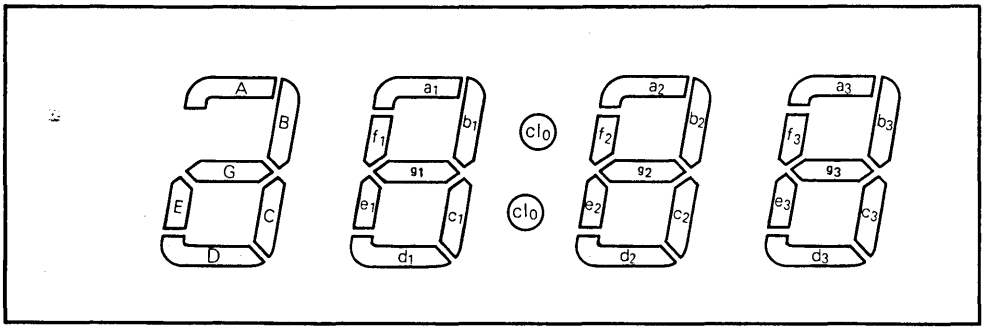
Active Terminal means to set any specified input terminal to the V_{DD} level.

Fluorescent Indicator Panel (FIP®)

(1) 12 hour display format



(2) 24 hour display format



Note: The suffixes of segments differ from those of Fluorescent Indicator Panel catalog as following.

μPD2006G		FIP5D15S
h	———	a_4/b_4
a_1	———	a_3
a_2	———	a_2
a_3	———	a_1

TIMER FUNCTION

Sleep Timer:

It can be operated by an SLI input, SLP OUT – ON, and can be turned off at the preset time limit.

SLP OUT, CNT OUT, ALM OUT and MUT OUT will be turned off by an ACS input.

Alarm Timer (Control Timer):

It will be operated by matching the current time and the alarm time.

ALM OUT . . . 2048 + 8 + 0.5 Hz output	To be turned off after 4 minutes.
MUT OUT . . . ON	To be turned off after 4 minutes.
CNT OUT . . . ON	To be turned off at the preset time limit.
ALM OUT by an SNZ input	To be held for 4^{+0}_{-1} min. and kept outputting for another 4 minutes.

ALM OUT & MUT OUT – OFF by an AOS input,

ALM OUT, MUT OUT, CNT OUT & SLP OUT – OFF by an ACS input.

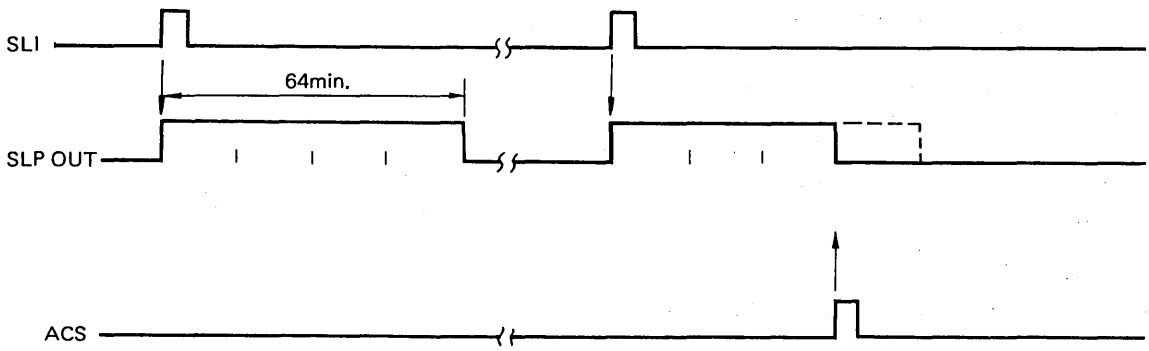
TIME SIGNAL TONE FUNCTION

2048 Hz is output from TSG OUT for one second at every 00 min. 00 sec.

Timer Output

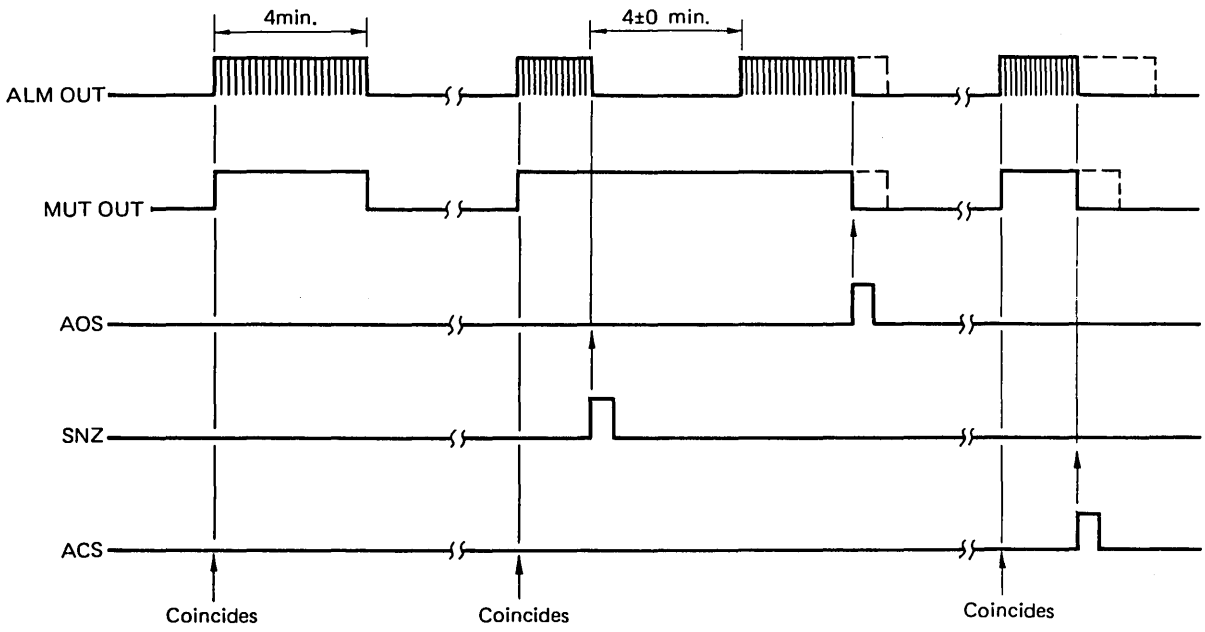
Sleep Timer

(Time limit: 64min.)



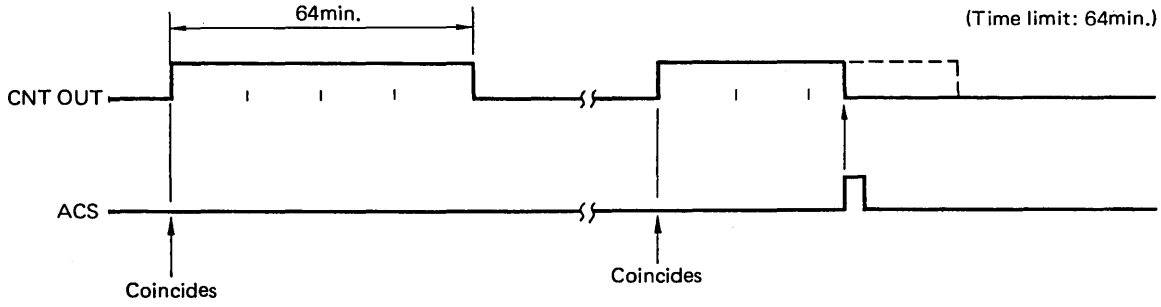
Alarm Timer

(Time limit: 64min.)



Control Timer

(Time limit: 64min.)



DISPLAY ELEMENT

Static Driving	4 digits FIP, LED	
Adaptable FIP	FIP4A15S	FIP5A15S
	FIP4B15S	FIP5D15S
	FIP4A13S	FIP5B13S

FUNCTION

Stardard Time	Hour, Minute, Second Display changeable between 12 & 24 hours.
Memory	
Alarm Timer	Hour, Minute (control timer)
Dual Time	Hour, Minute
Stop Watch	Minute, Second (max. 24 minutes)
Any of these 3 memories can be selected for use.	
Time Limit	4 types (16, 32, 64 or 128 minutes)
Timer	Sleep Timer

TERMINAL FUNCTION

Input Terminal	
ASD	To call the memory display (alarm timer, stop watch or dual time)
SEC	To call the second display
TID	To call the time limit display of sleep timer (control timer)
DUT	To set the memory to the dual time function
STW	To set the memory to the stop watch function
SLI	Input of the sleep timer start & time limit selection
FS	To reset +29/—30 seconds to zero
FM	To adjust minutes by shifting 1 pps or 1 push 1 word
FH	To adjust hours by shifting 1 pps or 1 push 1 word
ACS	Input to stop the alarm timer, control timer and sleep timer
SNZ	To halt alarm tone output (4^{+0}_{-1} min.) (snooze input)
AOS	Input to stop ALM OUT & MUT OUT (CNT OUT or SLP OUT is not affected)
ANS	To delete the alarm tone waveform (2048+8+0.5 Hz) from ALM OUT
DIM	To switch over the segment output duty to 1/16
12/24	To switch over the 12-hour and 24-hour format.
Output Terminal	
a_1 to g_1	All for segment output
a_2 to g_2	
a_3 to g_3	
AM & B	
PM & ADEG	
h & C	
1Hz (dot)	
ALM OUT	To output the alarm tone waveform (2048+8+0.5 Hz) for 4 minutes
TSG OUT	To output the time tone waveform (2048 Hz) for 1 second.
SLP OUT	To output sleep timer
CNT OUT	To output control timer
MUT OUT	To output mute
Oscillation Terminals	
OSC IN	X tal Connection Terminals
OSC OUT	

Power Terminals

V_{DD}	Common Line ($+V_{DD}$)
V_{SS}	Clock counter power line ($-V_{SS}$)
V_{SH}	Output driver power line ($-V_{SH}$)

Input Terminal Pull-Down Resistance

Input Terminal	$V_{DD} - V_{SS}$	Resistance	Unit
FS	1.5 V	0.01 – 1.0	MΩ
FM	1.5 V	0.01 – 1.0	MΩ
FH	1.5 V	0.01 – 1.0	MΩ
SNZ	1.5 V	0.01 – 1.0	MΩ
ACS	1.5 V	0.01 – 1.0	MΩ
SLI	1.5 V	0.01 – 1.0	MΩ
TST 1	1.5 V	0.01 – 1.0	MΩ
AC	1.5 V	0.01 – 1.0	MΩ

ADJUSTMENT FUNCTION

Standard Time

FH · · · Hour — 1 pps or 1 push 1 word
FM · · · Minute — 1 pps or 1 push 1 word
FS · · · Second — Reset +29 s/–30 s to zero

Memory

Alarm Time

FH · · · Hour
FM · · · Minute
FS ┬ FH · · · updating AM/PM only,
└ FM · · · updating 10th digit of a minute only.

Dual Time

FH · · · Hour
FM · · · Minute
FS ┬ FH · · · updating AM/PM only.
└ FM · · · updating 10th digit of a minute only.

Stop Watch

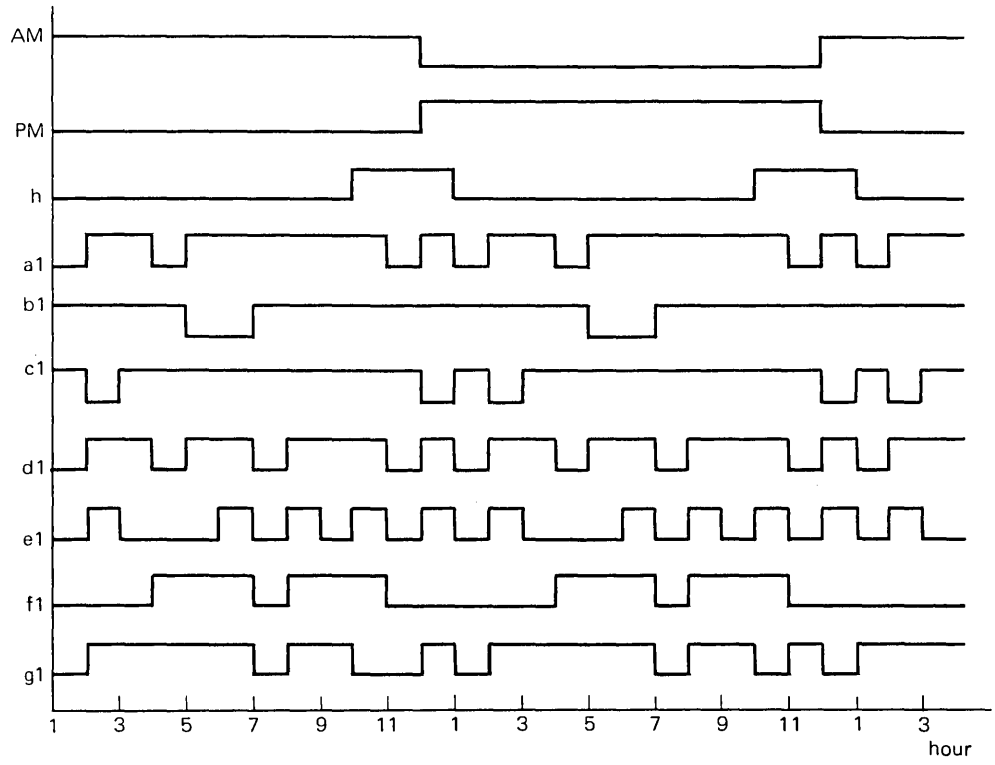
FH · · · Start/Stop
FM · · · Reset

Time Limit

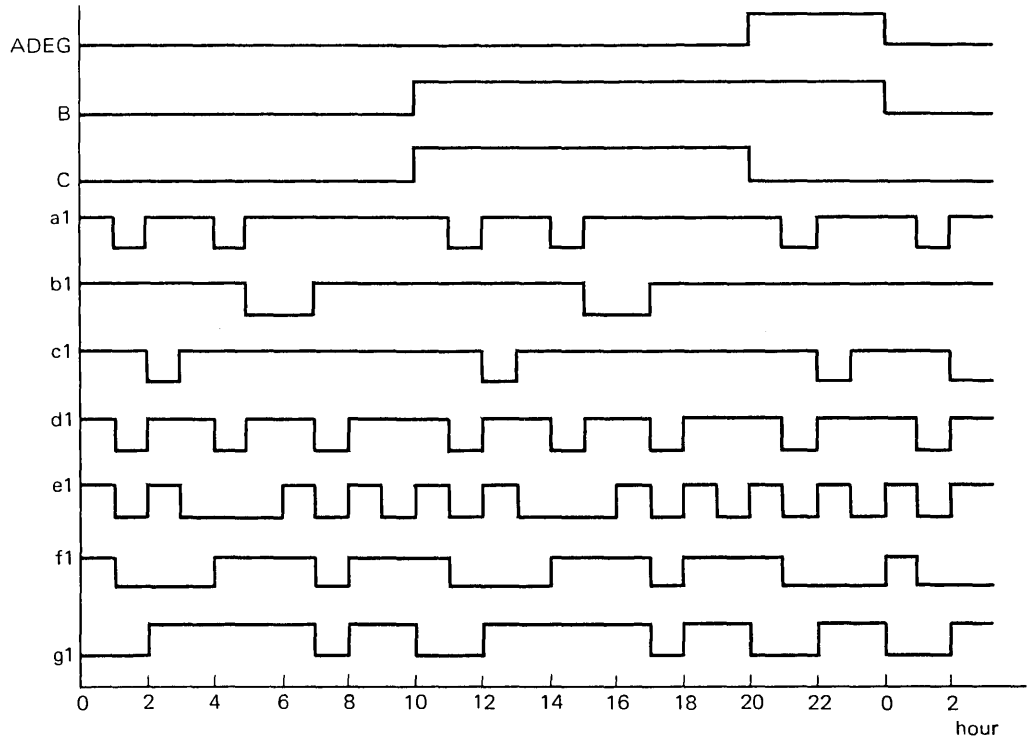
SLI · · · Time Limit Selection in case of the time limit display.
64 min. → 128 min. → 16 min. → 32 min. → 64 min. → 128 min.

Segment Output Waveform

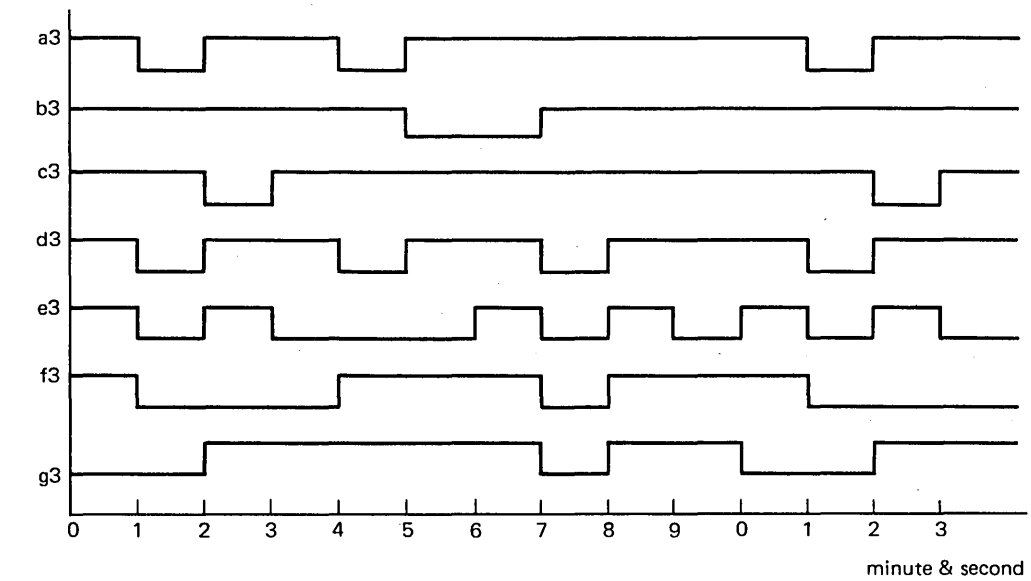
Display of Hours for 12-Hour Format

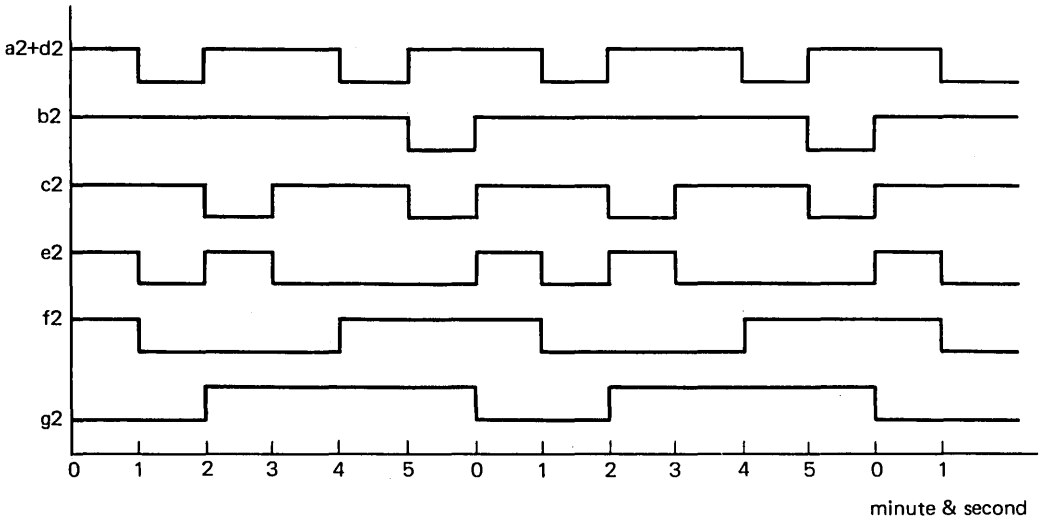


Display of Hours for 24-Hour Format

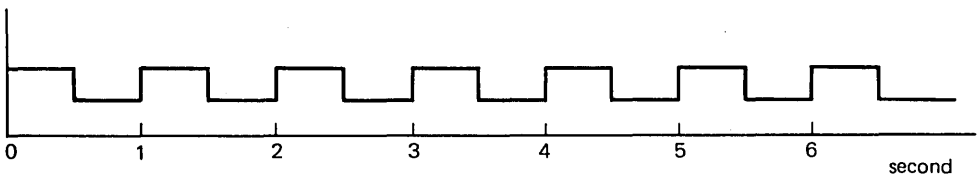


Display of Minutes & Seconds

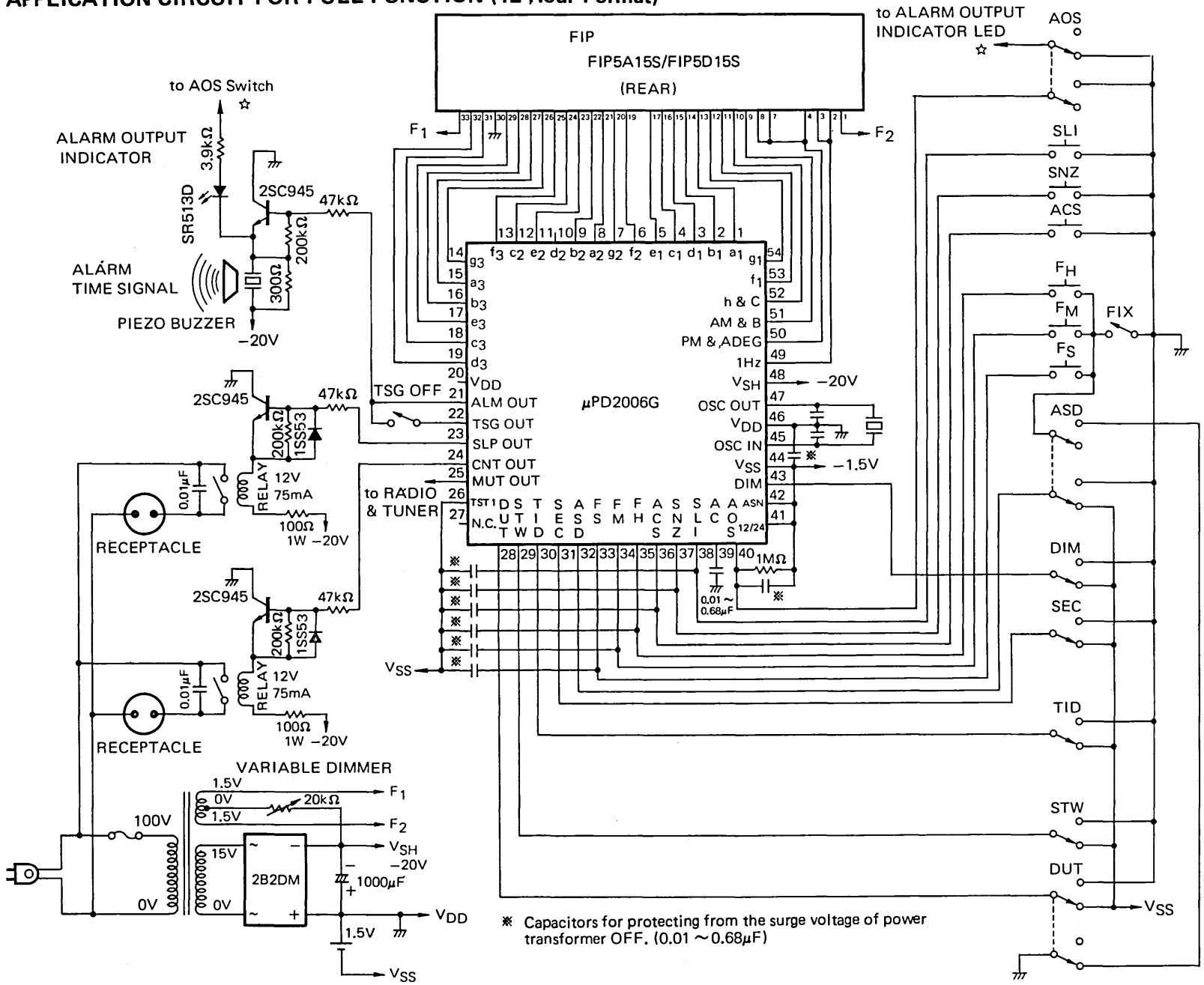




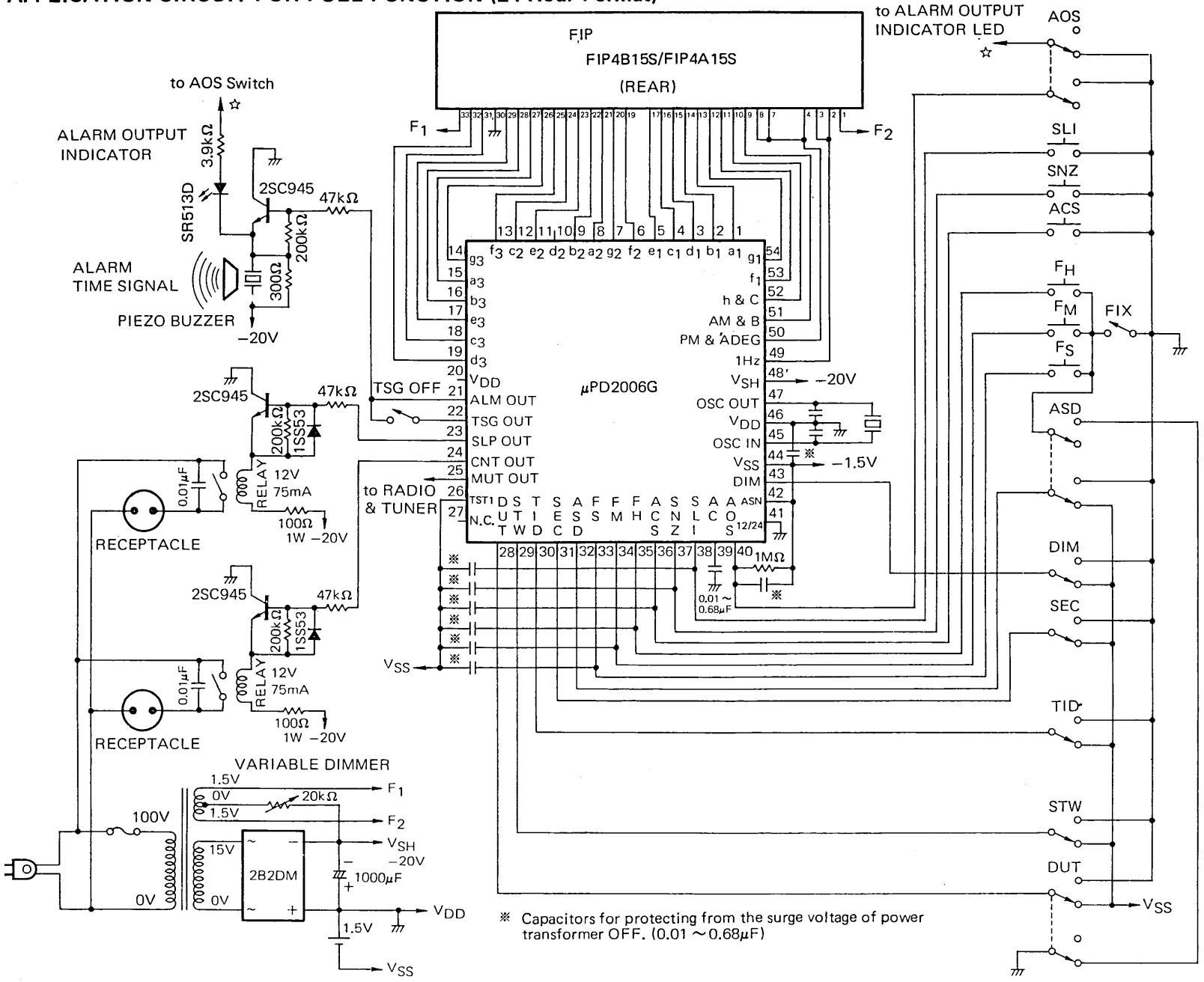
Dot (1Hz) Display

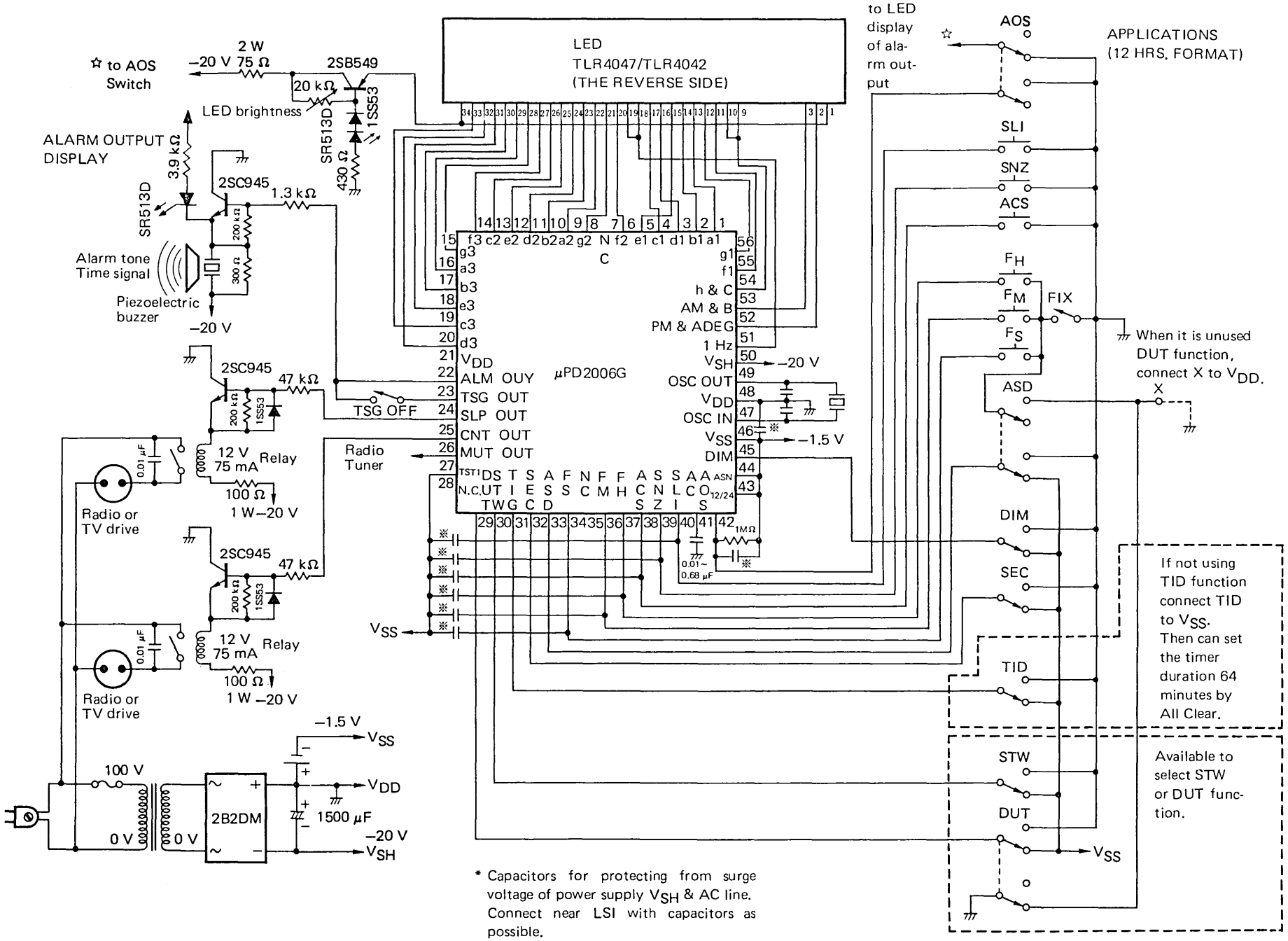


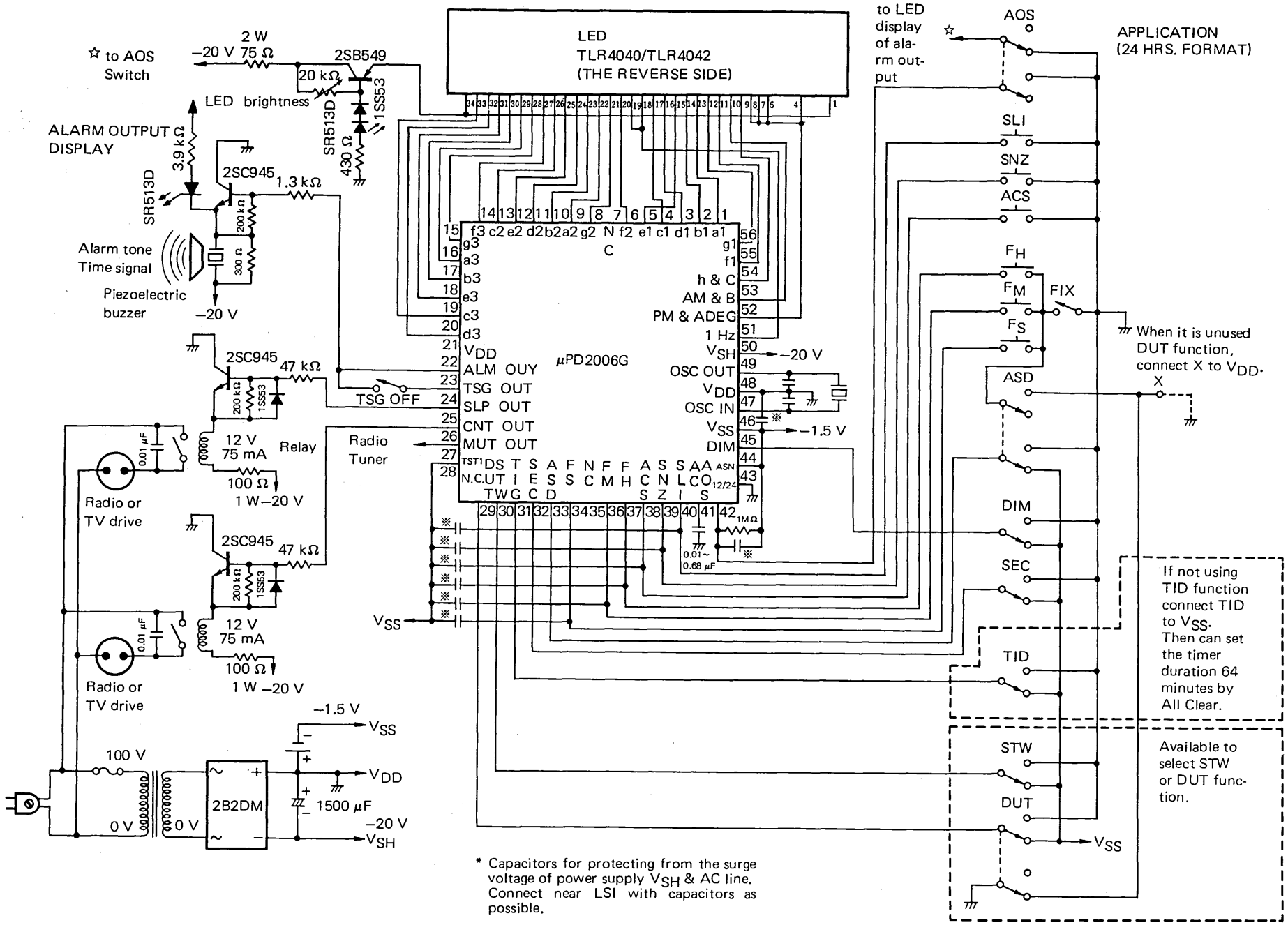
APPLICATION CIRCUIT FOR FULL FUNCTION (12 Hour Format)



APPLICATION CIRCUIT FOR FULL FUNCTION (24 Hour Format)




LED
TLR4047/TLR4042
(THE REVERSE SIDE)
to LED display of alarm output
APPLICATIONS (12 HRS. FORMAT)
AOS
SLI
SNZ
ACS
FH
FM
FS
FIX
ASD
DIM
SEC
TID
STW
DUT
When it is unused DUT function, connect X to VDD.
If not using TID function connect TID to VSS. Then can set the timer duration 64 minutes by All Clear.
Available to select STW or DUT function.
μPD2006G
☆ to AOS Switch
2 W
−20 V 75 Ω
2SB549
20 kΩ
LED brightness
1SS53
SR513D
430 Ω
ALARM OUTPUT DISPLAY
3.9 kΩ
2SC945
1.3 kΩ
200 kΩ
300 Ω
Alarm tone Time signal
Piezoelectric buzzer
−20 V
47 kΩ
TSG OFF
Radio Tuner
12 V 75 mA Relay
100 Ω 1 W
0.01 μF
Radio or TV drive
100 V
0 V
2B2DM
−1.5 V
VSS
VDD
1500 μF
−20 V
VSH
VDD
ALM OUY
TSG OUT
SLP OUT
CNT OUT
MUT OUT
OSC OUT
OSC IN
DIM
1 Hz
h & C
AM & B
PM & ADEG
1MΩ
0.01~0.68 μF
* Capacitors for protecting from surge voltage of power supply VSH & AC line. Connect near LSI with capacitors as possible.


LED
TLR4040/TLR4042
(THE REVERSE SIDE)
to LED display of alarm output
APPLICATION
(24 HRS. FORMAT)
AOS
SLI
SNZ
ACS
FH
FM
FS
FIX
ASD
DIM
SEC
TID
STW
DUT
X
When it is unused DUT function, connect X to VDD.
If not using TID function connect TID to VSS. Then can set the timer duration 64 minutes by All Clear.
Available to select STW or DUT function.
☆ to AOS Switch
2 W
−20 V 75 Ω
2SB549
20 kΩ
LED brightness
1SS53
SR513D
430 Ω
ALARM OUTPUT DISPLAY
3.9 kΩ
2SC945
1.3 kΩ
200 kΩ
300 Ω
Alarm tone
Time signal
Piezoelectric buzzer
−20 V
47 kΩ
TSG OFF
12 V
75 mA
Relay
100 Ω
1 W−20 V
Radio or TV drive
0.01 μF
Radio Tuner
μPD2006G
VDD
ALM OUY
TSG OUT
SLP OUT
CNT OUT
MUT OUT
VSS
VSH
OSC OUT
OSC IN
DIM
1 Hz
PM & ADEG
AM & B
h & C
−20 V
−1.5 V
1MΩ
0.01~ 0.68 μF
100 V
0 V
2B2DM
1500 μF
* Capacitors for protecting from the surge voltage of power supply VSH & AC line. Connect near LSI with capacitors as possible.

MOS DIGITAL INTEGRATED CIRCUIT
μPD6529C

AUTOMOTIVE CLOCK
CMOS LSI

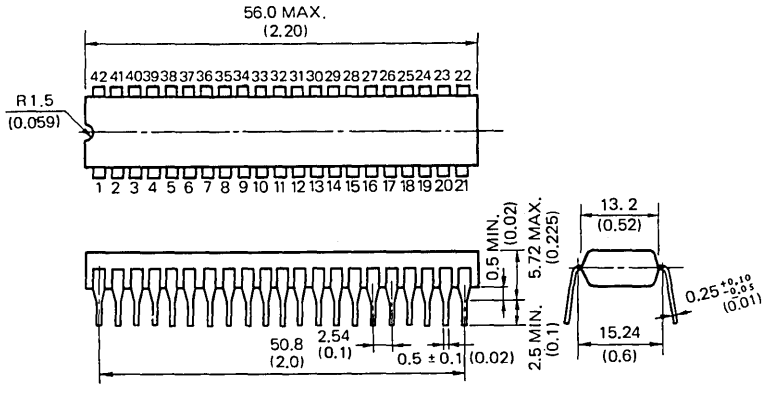
GENERAL DESCRIPTION

The μPD6529C is a monolithic CMOS LSI for crystal controlled automative clocks. The circuits interface directly with fluorescent indicator panel. The display format is 12 hours. It is also provided with a 4-ways display brightness control function and can be driven by an external clock signal.

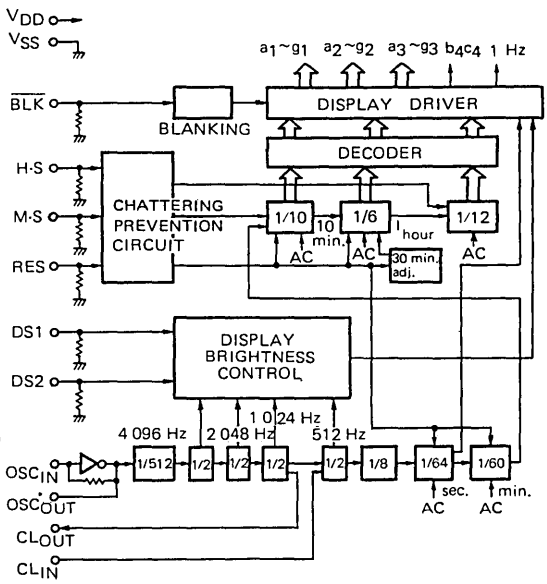
FEATURES

- Crystal controlled oscillator (4.194 304 MHz)
- Direct interface to fluorescent indicator panel (FIP4E8S)
- 12 hours display format
- 4-ways display brightness control (duty controlled dimmer 1, 1/4, 1/8, 1/16)
- External clock drive possible (1 024 Hz)
- Separated hours and minutes set controls (2 Hz)
- On the hour adjustment control (±30minutes)
- 1 024 Hz output
- 42 Pin DIP mold

PACKAGE DIMENSIONS
in millimeters (inches)

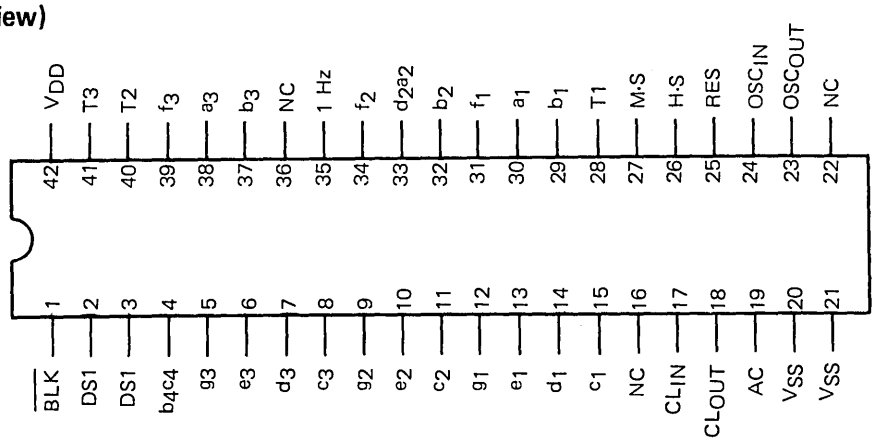


BLOCK DIAGRAM



CONNECTION DIAGRAM

(Top View)



PIN NO.	SYMBOL INPUT	SYMBOL OUTPUT	PIN NAME	INTERNAL STATE
1	$\overline{BLK}$		Blanking input	Pull down
2	DS1		Dimmer input 1	↓
3	DS2		Dimmer input 2	↓
4		b_4c_4	Segment output	P-ch Open Drain
5		g_3	↓	↓
6		e_3	↓	↓
7		d_3	↓	↓
8		c_3	↓	↓
9		g_2	↓	↓
10		e_2	↓	↓
11		c_2	↓	↓
12		g_1	↓	↓
13		e_1	↓	↓
14		d_1	↓	↓
15		c_1	↓	↓
16	NC			
17	CL_{IN}		Ex. Clock input	
18		CL_{OUT}	Clock output	
19	AC		Clear input	Pull down
20	V_{SS}		–Power supply	
21	V_{SS}		↓	

PIN NO.	SYMBOL INPUT	SYMBOL OUTPUT	PIN NAME	INTERNAL STATE
22	NC			
23		OSC_{OUT}	OSC output	
24	OSC_{IN}		OSC input	
25	RES		RES input	Pull down
26	H·S		Hour adj. input	↓
27	M·S		Minute adj. input	↓
28	T1		Test pin 1	
29		b_1	Segment output	P-ch Open Drain
30		a_1	↓	↓
31		f_1	↓	↓
32		b_2	↓	↓
33		$d_2{\cdot}a_2$	↓	↓
34		f_2	↓	↓
35		1 Hz	1 Hz signal	↓
36	NC			
37		b_3	Segment output	P-ch Open Drain
38		a_3	↓	↓
39		f_3	↓	↓
40	T2		Test pin 2	
41	T3		Test pin 3	
42	V_{DD}		+Power supply	

ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Power supply voltage	$V_{DD}-V_{SS}$	−0.3	to	+8.0	V
Input voltage	V_{IN}	V_{SS}−0.3	to	V_{DD}+0.3	V
Output voltage	V_{OUT}	V_{DD}−20	to	V_{DD}+0.3	V
Operating temperature	T_{opt}	−40	to	+85	°C
Storage temperature	T_{stg}	−55	to	+125	°C

RECOMMENDED OPERATING CONDITIONS

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power Supply Voltage	$V_{DD}-V_{SS}$	3.0	−	7.0	V
High Level Input Voltage	V_{IH}	0.7 V_{DD}	−	V_{DD}	V
Low Level Input Voltage	V_{IL}	V_{SS}	−	0.3 V_{DD}	V
External Clock Duty	CL_D	40	50	60	%

ELECTRICAL CHARACTERISTICS 1 (Unless otherwise noted $V_{DD}-V_{SS}$=6.0 V, T_a=25 °C, RH≤70 %, C_D=C_G=15 pF, Xtal=4.194 304 MHz)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power Supply Current	I_{DD}	No output loads	−	−	1	mA
High Level Output Current 1, Note 1	$\|I_{OH1}\|$	$V_{DD}-V_{SS}$=3.0 V, $V_{DD}-V_{OUT}$=0.5 V	300	−	−	μA
High Level Output Current 2, Note 2	$\|I_{OH2}\|$	$V_{DD}-V_{SS}$=3.0 V, $V_{DD}-V_{OUT}$=0.5 V	500	−	−	μA
AC Response Time	T_{AC}	$V_{DD}-V_{SS}$=3.0~7.0 V V_{IN}=0.7 V_{DD}~V_{DD}	−	−	100	μS
Low Level Output Current, Note 3	I_{OL}	$V_{DD}-V_{SS}$=3.0 V, $V_{OUT}-V_{SS}$=0.5 V	500	−	−	μA
High Level Input Current 1, Note 4	I_{IH1}	V_{IN}=V_{DD}	−	15	30	μA
High Level Input Current 2, Note 5	I_{IH2}	V_{IN}=V_{DD}	−	120	600	μA
Low Level Input Current	$\|I_{IL}\|$	V_{IN}=V_{SS}	−	−	50	μA
External Clock Duty	CL_D		40	50	60	%

ELECTRICAL CHARACTERISTICS 2 (Unless otherwise noted $V_{DD}-V_{SS}$=3.0 to 7.0 V, T_a=−40 to +85 °C, RH≤70 %, C_D=C_G=15 pF, Xtal=4.194 304 MHz)

CHARACTERISTIC	SYMBOL	TEST CONDITONS	MIN.	TYP.	MAX.	UNIT
Power Supply Current	I_{DD}	No output loads	−	−	2	mA
High Level Output Current 1, Note 1	$\|I_{OH1}\|$	$V_{DD}-V_{SS}$=3.0 V, $V_{DD}-V_{OUT}$=0.5 V	250	−	−	μA
High Level Output Current 1, Note 2	$\|I_{OH2}\|$	$V_{DD}-V_{SS}$=3.0 V, $V_{DD}-V_{OUT}$=0.5 V	400	−	−	μA

Note 1) for segments other than those specified in Note 2

Note 2) for segments b4C4 and a2d2, 1 Hz and CL_{OUT}

Note 3) for CL_{OUT}

Note 4) for DS1, DS2, RES, H·S, M·S, and $\overline{BLK}$

Note 5) for T1, T2, T3 and AC

INTERFACE SIGNAL DESCRIPTION

[1] H·S input (pin 26)

Put this pin (26) to High Level (V_{DD}) and the Hour counter is fast fed at 2 Hz. No counting up from Minutes to Hours is provided.

[2] M·S input (pin 27)

Put this pin (27) to High Level (V_{DD}) and the Minutes counter is fast fed at 2 Hz. No counting up from Seconds to Minutes is provided.

[3] RES input (pin 25)

Put this pin (25) to High Level (V_{DD}) and the adjustment to a right o'clock is made within ±30 minutes range, as shown below.

① XX o'clock 00 minute 00 second
⇩
XX o'clock 29 minutes 59 seconds
RES ⇨ XX o'clock 00 minute 00 second

② XX o'clock 30 minutes 00 second
⇩
XX o'clock 59 minutes 59 seconds
RES ⇨ (XX+1) o'clock 00 minute 00 second

[4] $\overline{BLK}$ input (pin 1)

Put this pin (25) to Low Level (open) and the display outputs are turned off (Blanking).

During Blanking, H·S, M·S and RES inputs are ineffective.

Return this pin to High Level and the display outputs are recovered.

[5] DS1 input (pin 2) and DS 2 input (pin 3)

Combine DS1 and DS2 as shwn below and the display brightness is dimmed accordingly.

DS2	DS1	Output ON Duty Ratio	Clock Mode
L	L	1	Internal, External
L	H	1/4	↓
H	L	1/8	
H	H	1/16	

Dimmer Freqency : 512 Hz

- Internal Clock Mode
  4.194 304 MHz crystal oscillator is used.
- External Clock Mode
  1 024 Hz signal is input to CL_{IN} pin.

[6] AC input (pin 19)

Put this pin to High Level (V_{DD}) and this IC is reset to display 1 o'clock 00 minute (00 second).

[7] CL_{IN} input (pin 17)

When this IC is to be driven by a crystal oscillator, put this pin to Low Level (V_{SS}).

When this IC is to be driven by an external clock, input a 1 024 Hz signal voltage within the specified input voltage range.

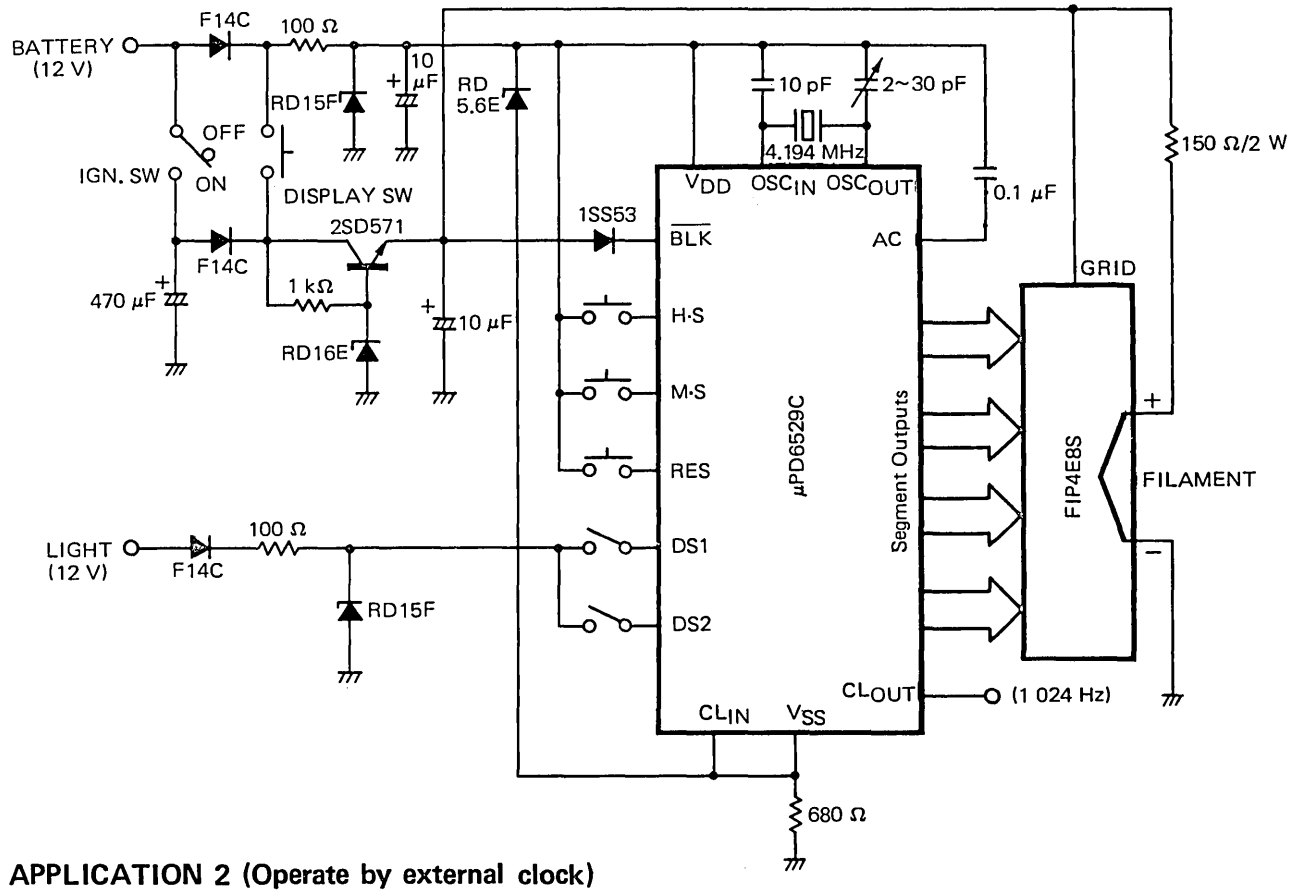
[8] CL_{OUT} output (pin 18)

A 1 024 Hz signal with 50 % duty is output on this pin (as a CMOS output). When this IC is operated on an external clock, this output is suppressed.

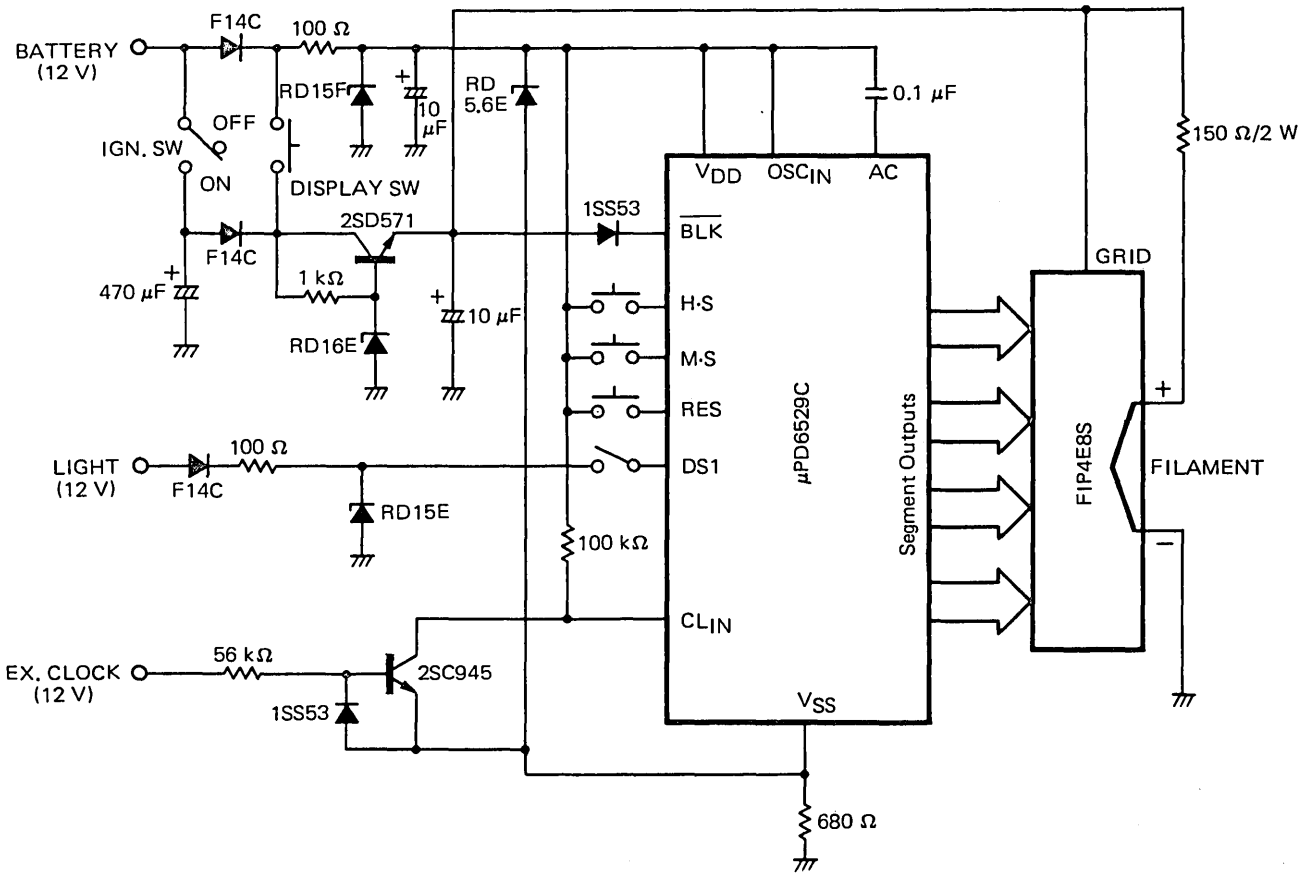
[9] T1 (pin 28), T2 (pin 40) and T3 (pin 41)

These pins are provided for the LSI testing and should be kept on Low Level (V_{SS}) during operation.

APPLICATION 1



APPLICATION 2 (Operate by external clock)



MOS DIGITAL INTEGRATED CIRCUIT
μPD1990AC

SERIAL I/O CALENDAR & CLOCK
CMOS LSI

The μPD1990AC is a CMOS integrated circuit having a clock function, which has been designed with the intent of connecting to microcomputer.

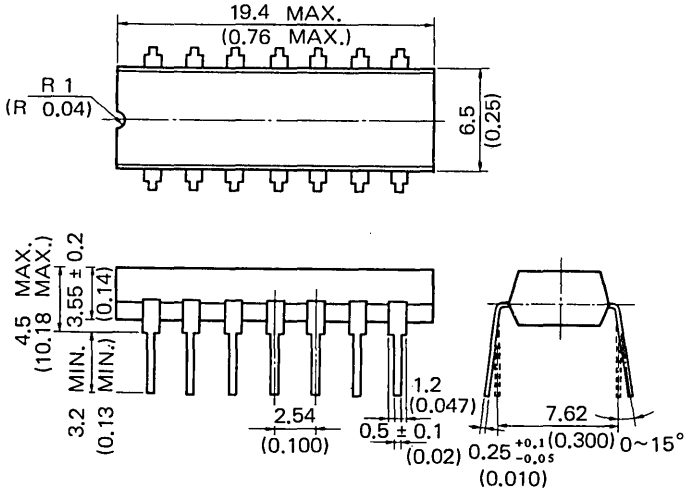
This IC counts independently the month, date, day of the week, hour, minute and second, and is able to have the output and input of these time data freely upon command from the microcomputer. By employing this IC, the microcomputer is freed from performing clock functions, and will be able to be use exclusively to other complicated operations.

The μPD1990AC employs the oscillation of a 32.768 kHz crystal as a reference. And all functions are enclosed in a 14 pin dual in-line package.

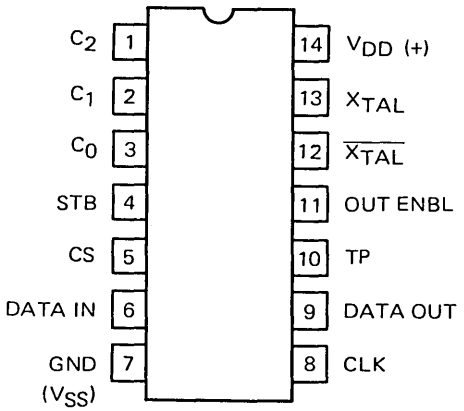
FEATURES

- Timekeeping (hours, minutes and seconds) and calendar (months, date and day of the week).
- Serial input and output of date.
  (Input & output code: All digits Binary Coded Decimal, except "Month" which is Hexa-Decimal Code)
- Reference frequency is 32.768 kHz, which is generated by a crystal oscillator circuit.
- Provided with timing pulse outputs. (Selection of 64 Hz, 256 Hz or 2 048 Hz is possible.)
- By using CS (chip selection) terminal, multi-chip applications are possible.

PACKAGE DIMENSIONS
in millimeters (inches)

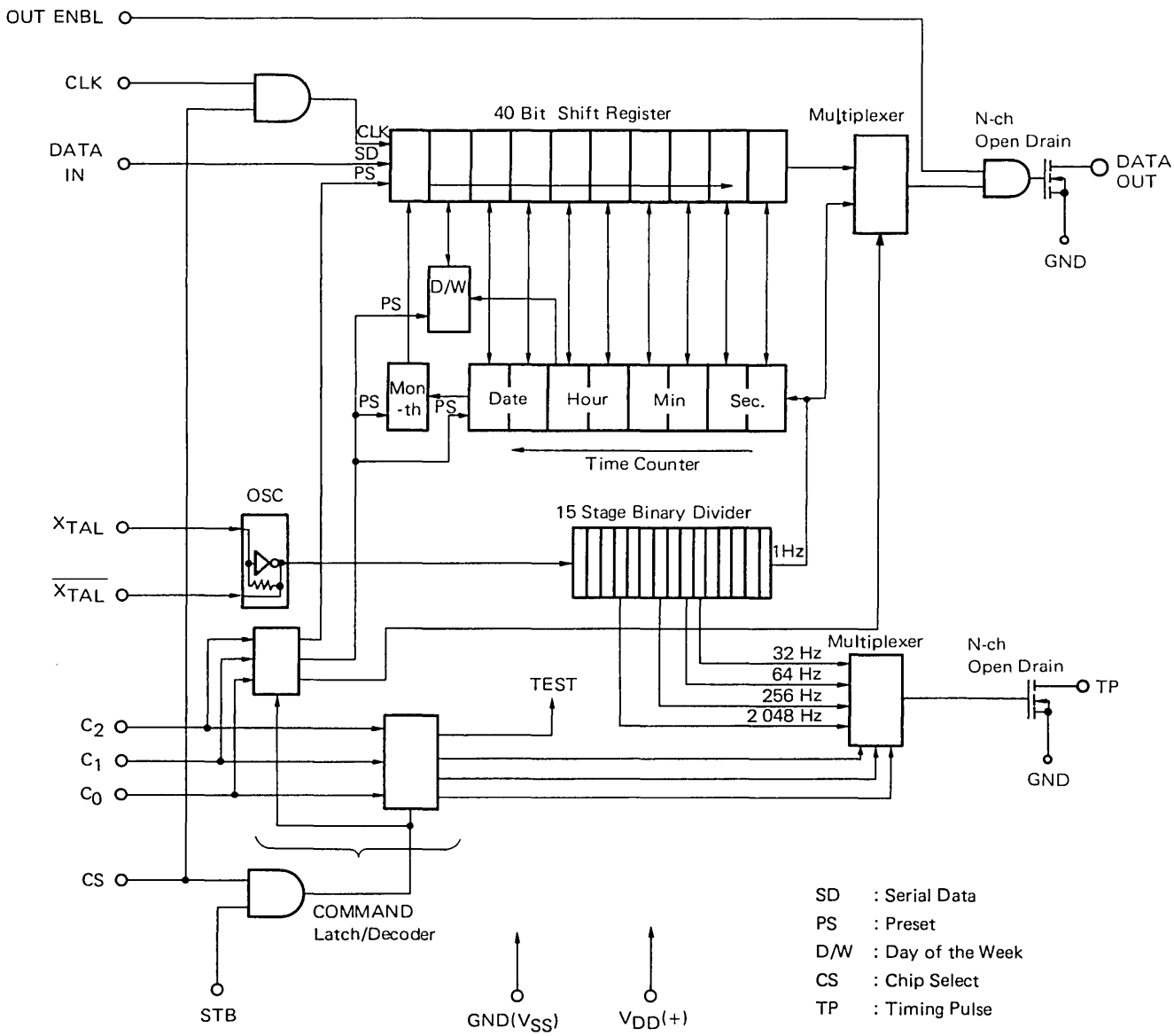


CONNECTION DIAGRAM (Top View)



NO.	Terminology	NO.	Terminology
1	C_2	8	CLK
2	C_1	9	DATA OUT
3	C_0	10	TP
4	STB	11	OUT ENBL
5	CS	12	$\overline{X_{TAL}}$
6	DATA IN	13	X_{TAL}
7	GND(V_{SS})	14	V_{DD} (+)

SERIAL I/O CALENDAR BLOCK DIAGRAM



f_{osc} = 32.768 kHz
V_{DD} = 2.0 to 5.5 V

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$V_{DD}-V_{SS}$	6.0	V
Input Voltage	V_{IN}	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Operating Temperature Range	T_{opt}	−40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Output Terminal Voltage	V_{OUT}	$V_{SS}-0.3$ to 6.0	V

ELECTRICAL CHARACTERISTICS (f=32.768 kHz, $C_G=C_D$=20 pF, Xtal R_S=20 kΩ, Ta=25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Operating Voltage	$V_{DD}-V_{SS}$	2.00		5.50	V	
Current Consumption	I_{SS}		20	50	μA	$V_{DD}-V_{SS}$=3.60 V
Low Level Output Current	I_{OL}	*500			μA	$V_{DD}-V_{SS}$=2.0 V V_{OL}=0.4 V
CLK Input Frequency	f_{CLK}	DC		100	kHz	$V_{DD}-V_{SS}$=2.0 V, Duty 50 %
Input Leakage Current	I_{IN}			1	μA	$V_{DD}-V_{SS}$=3.60 V
High Level Input Voltage	V_{IH}	$0.8V_{DD}$		V_{DD}	V	
Low Level Input Voltage	V_{IL}	V_{SS}		$0.2V_{DD}$	V	
Oscillation Starting Voltage	V_{STA}	2.0			V	T_{STA}=10 s

* TP and DATA OUT are N-channel open drain output.

A.C. ELECTRICAL CHARACTERISTICS (FOR REFERENCE --- NOT SPECIFIED)

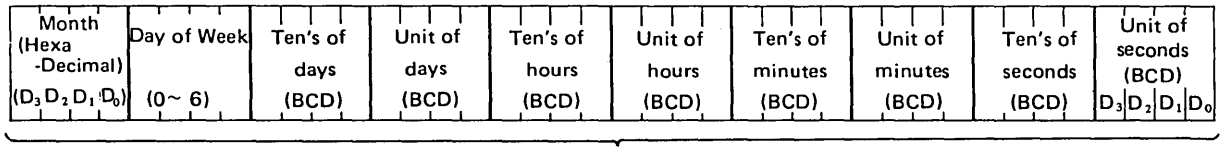
(f=32.768 kHz, $V_{DD}-V_{SS}$=2.0 V, Ta=25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_0~2, CS–STB Set-up Time	t_{SU}	2			μs	
STB Pulse Width	T_{STB}	2			μs	
C_0~2, CS–STB Hold Time	T_{HLD}	2			μs	
STB LATCH Delay Time	t_{d1}			*4	μs	except Time Read mode
CLK–DATA OUT Delay Time	t_{dc-o}			2	μs	R_L=33 kΩ, C_L=15 pF
DATA IN Set-up Time	t_{DSU}	2			μs	
DATA IN Hold Time	t_{DHLD}	2			μs	

* Note: When group 0 is Time Read mode, STB LATCH delay time is 40 μs MAX. (t_{d2}).

FUNCTION SPECIFICATIONS

- Reference frequency (X tal osc.).
  - 32.768 kHz
- Data.
  - Hours, Minutes, Seconds, Months, Date and Days of the Week ("Hours" 24 hour form) (Automatic adjustment of long and short months). The data is output in order to "Second", "Minute", "Hour", "Day", "Day of Week", "Month". Refer to Fig. 1.
- Data format
  - Binary Coded Decimal (except "Month" which is Hexa-Decimal Code)
- Data input-output and Clock.
  - Serial input, serial output.
  - Data input and output in synchronization with the clock input from the CLK.
- Timing pulse output.
  - One of 64 Hz, 256 Hz or 2 048 Hz can be selected by command.
- Mode selection.
  - Selected according to input to C_0, C_1, C_2.
    Group "0" C_2=0 Register control (control of data input-output).
    Group "1" C_2=1 Tp selection (Selection of timing pulses) and TEST MODE setting.
  - Commands of group "0" and those of group "1" are independently latched by the STB input.
- Chip select.
  - CLK and STB inputs prohibited by connecting CS input to GND(V_{SS}) level.
- Prohibition of output of data.
  - Making OUT ENBL input GND level DATA OUT terminal become high impedance.
- Leap year
  - The correction for length of the month is automatically performed and leap year is not automatically performed. But it is possible to set calendar FEB. 29, and the day after, it will be Mar. 1.



* DATA of 40 Bit Shift Register appears on DATA OUT terminal from LSB of Second.

Fig. 1

TERMINALS

- Input terminals.
  - DATA IN — Data input of 40 bit shift register.
  - CLK — Shift clock input of 40 bit shift register.
  - C_0~C_2 — Command input (3 bit).
  - STB — Strobe input.
  - CS — Chip select input (Prohibits CLK & STB).
  - OUT ENBL — Output control input (Makes the DATA OUT high impedance by inputting low level).
- Output terminals. (N-channel Open Drain)
  - DATA OUT — Data output of 40 bit shift register.
  - TP — Time pulse output.
- Oscillation terminals.
  - XTAL — Oscillation inverter input (OSC IN).
  - $\overline{XTAL}$ — Oscillation inverter output (OSC OUT).
- Power supply terminals.
  - V_{DD} — Plus power supply.
  - GND (V_{SS}) — Common line.

COMMAND SPECIFICATIONS

Group	C_2	C_1	C_0	FUNCTION	
0	0	0	0	Register Hold (TEST MODE is released)	DATA OUT = 1 Hz
	0	0	1	Register Shift	DATA OUT = [LSB]
	0	1	0	Time Set & Counter Hold	DATA OUT = [LSB]
	0	1	1	Time Read	DATA OUT = 0.5 Hz
1	1	0	0	TP = 64 Hz Set (TEST MODE is released)	
	1	0	1	TP = 256 Hz Set (TEST MODE is released)	
	1	1	0	TP = 2 048 Hz Set (TEST MODE is released)	
	1	1	1	TEST MODE Set	

* Groups "0" and "1" hold their functions independently, in other word, the command of the group "0" ("1") can change the group "0" ("1") function mode only. Then you must release the μPD1990AC from TEST MODE by setting commands of TP selection (group "1") or Register Hold Mode.

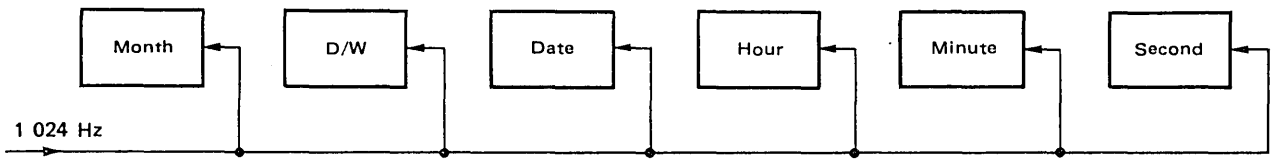
- Command input.
  - 3 bit, binary code input. C_0, C_1, C_2
- Number of commands.
  - Register control — 4
  - TP control — 3
  - TEST MODE set — 1

  (4 + 3 + 1 = 8)

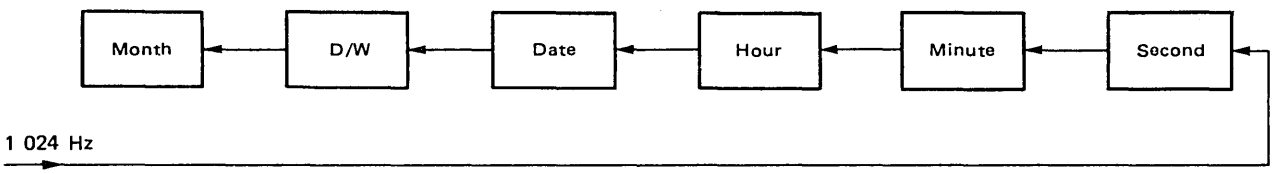
- Commands.
  - Register control [Group "0"]
    - ★ Register Hold MODE [0 0 0]
      Holds the 40 Bit Shift Register.
      The data is held, and shifting of the data becomes impossible.
      1 Hz is output from the DATA OUT terminal. The TEST MODE is released by this command.
    - ★ Shift MODE [0 0 1]
      Shifting of data of the 40 Bit Shift Register becomes possible.
      Data is shifted in synchronization with the clock input on CLK terminal.
      DATA OUT terminal outputs data from [LSB] of the 40 Bit Shift Register.
    - ★ Time set MODE [0 1 0]
      Presets the data of the 40 Bit Shift Register in the Time Counter.
      Resets the Flip-Flop (F/F) of 11 to 15 bits of the 15 Stage Binary Divider and hold the Time Counter.
      By setting other command of group "0", the Time Counter is released from the reset and the hold.
      [LSB] is output from the DATA OUT terminal.
      Shifting of data becomes impossible.
    - ★ Time read MODE [0 1 1]
      Reads into the 40 Bit Shift Register the data of the Time Counter.
      DATA OUT terminal outputs the data of [LSB] ([LSB]=0.5 Hz). Shifting of data becomes impossible.
  - TP control [Group "1"]
    - ★ TP = 64 Hz set MODE [1 0 0]
      64 Hz (duty 50 %) is output from the TP terminal.
    - ★ TP = 256 Hz set MODE [1 0 1]
      256 Hz (duty 50 %) is output from the TP terminal.
    - ★ TP = 2048 Hz set MODE [1 1 0]
      2048 Hz (duty 50 %) is output from the TP terminal.
    - ★ TEST MODE set MODE [1 1 1]
      Sets up the TEST MODE (Not used for ordinary operation). When TEST MODE is released by Register Hold MODE [000], TP terminal is 64 Hz output.

- TEST MODE (Set by command of TEST mode (111))
  In this mode DATA OUT terminal is enabled in spite of OUT ENBL input.
  There are 2 type TEST MODE selected by OUT ENBL terminal.

  TEST MODE 1 ; OUT ENBL = 0
  In this mode every Counter ("Month", "Day of Week", "Date", "Hour", "Minute", "Second") is advanced at a 1024 Hz in parallel. In this case overflow carry of each counter is not affect to the next counter.



  TEST MODE 2 ; OUT ENBL = 1
  In this mode TIME COUNTER is advanced at 1024 Hz in stead of 1 Hz from "Second" counter input.



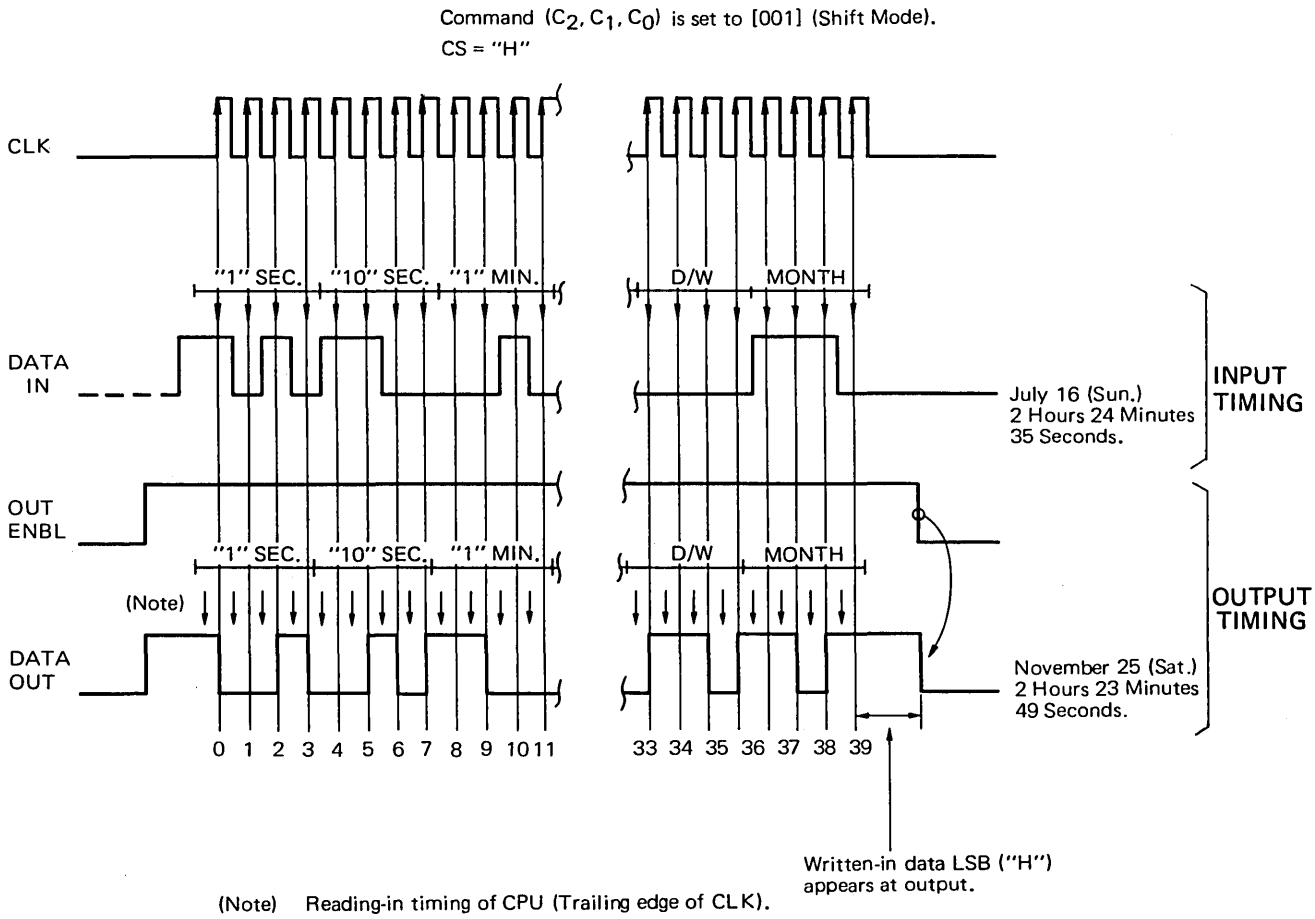
Following table shows the signals appeared on DATA OUT and TP terminals during the μPD1990AC is in the TEST MODE.

MODE	CODE C_2 C_1 C_0	DATA OUT	TP	OTHERS	
REGISTER HOLD	0 0 0	1 Hz	64 Hz	*By this command, TEST MODE is released.	
REGISTER SHIFT	0 0 1	LSB of 40 Bit S/R "0" or "1"	32 Hz	TEST MODE is remained.	T/C is advanced at 1 024 Hz in parallel or serial.
TIME SET	0 1 0	LSB of 40 Bit S/R "0" or "1"	32 Hz		
TIME READ	0 1 1	512 Hz	32 Hz		T/C is advanced at 1 024 Hz in parallel or serial.

S/R = Shift Register
T/C = Time Counter

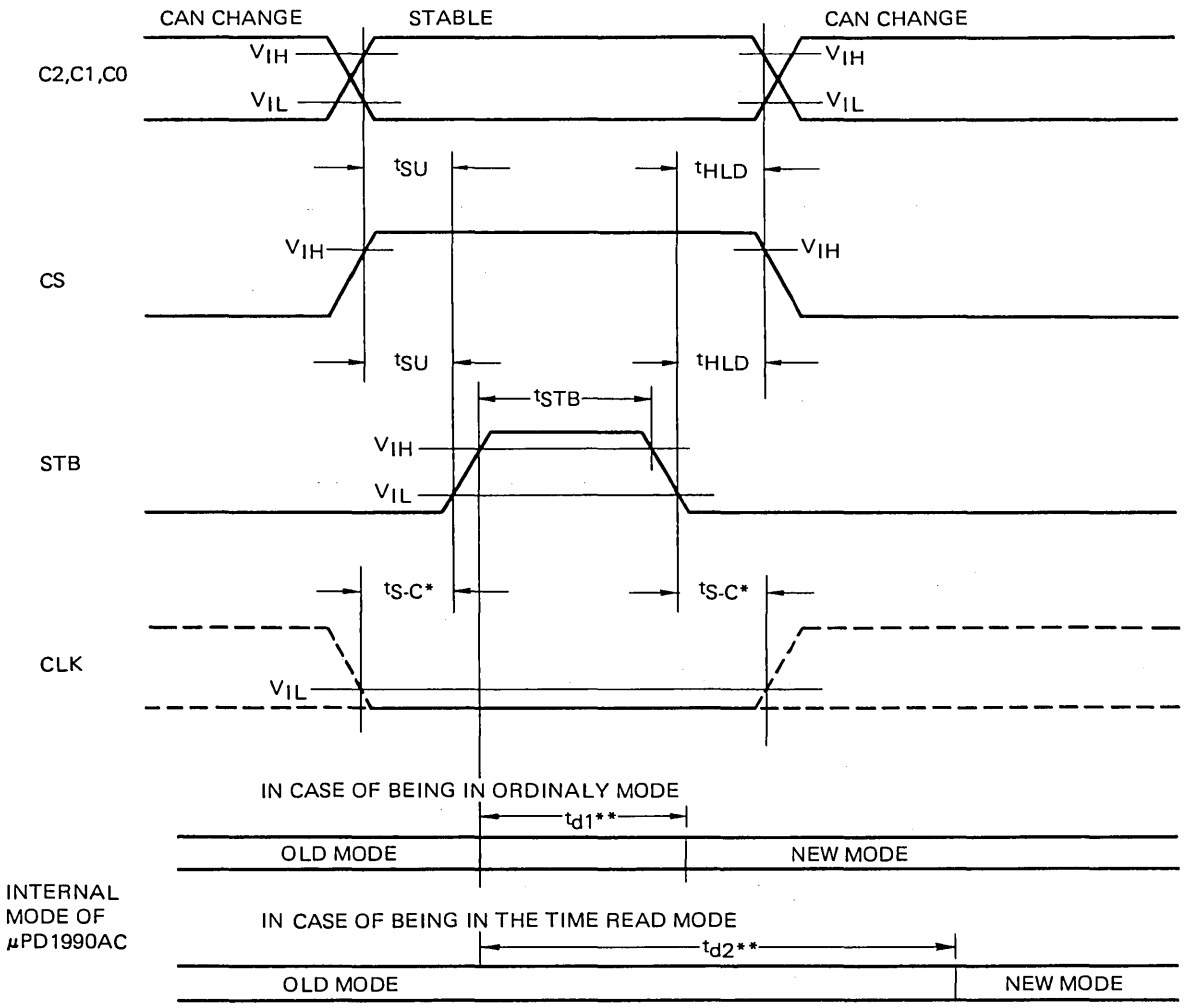
*Note: While μPD1990AC is TEST Mode, by setting the Register Hold mode (Group "0" mode), Test Mode changes TP=64 Hz mode in group "1" and as a result Register Hold mode is set. 1 Hz appears on DATA OUT terminal and 64 Hz appears on TP terminal.

DATA INPUT/OUTPUT TIMING DIAGRAM



(Note) Reading-in timing of CPU (Trailing edge of CLK).

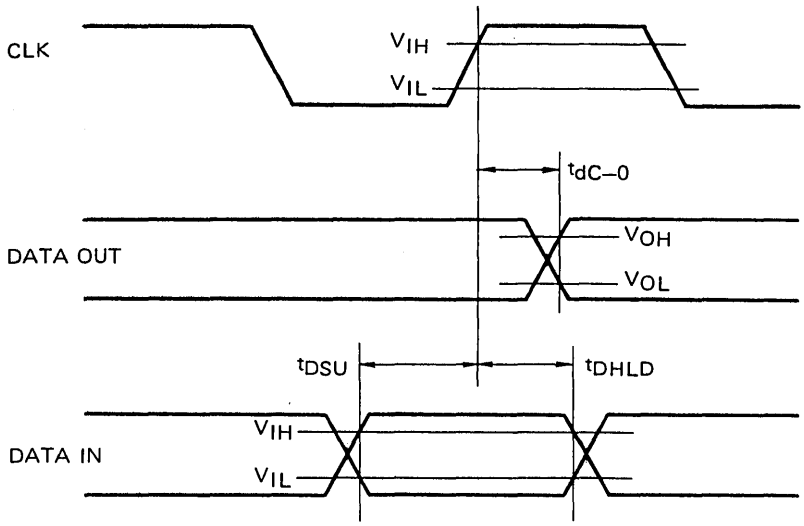
TIMING DIAGRAM FOR SETTING COMMANDS



t_{SU} = 2 μs MIN.
t_{HLD} = 2 μs MIN.
t_{STB} = 2 μs MIN.
t_{d1} = 4 μs MAX. (In case of being in ordinaly mode.)
t_{d2} = 40 μs MAX. (In case of being in the Time Read mode.)
t_{S-C} = 2 μs MIN.

Note: * Setting Register Shift command (001), input level of the CLK must be low level.
** The delay time until new mode becomes valid is 4 μs. MAX. (t_{d1}). But in the case of μPD1990AC being in the Time Read mode, it takes 40 μs MAX. (t_{d2}).

TIMING DIAGRAM OF DATA INPUT AND OUTPUT

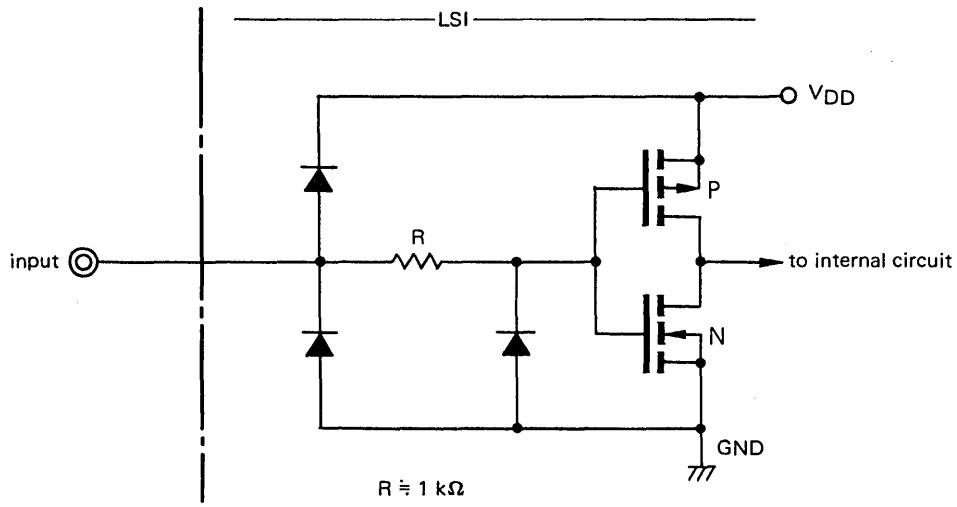


t_{dC-0} : 2 μs MAX. (RL=33 kΩ, CL=15 pF)
t_{DSU} : 2 μs MIN.
t_{DHLD} : 2 μs MIN.

INPUT AND OUTPUT CIRCUITS FOR μPD1990AC

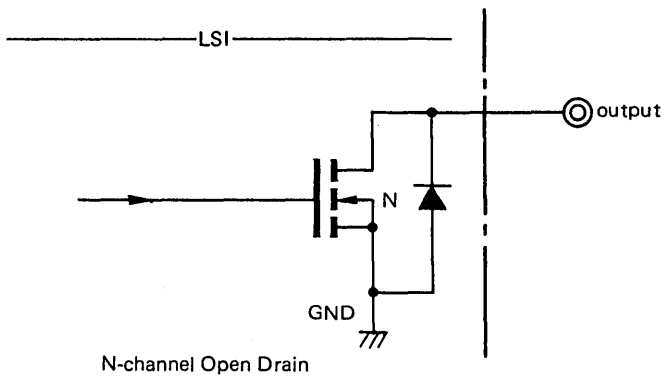
Input circuits

(for C2, C1, C0, STB, DATA IN, CLK, OUT ENBL, CS)



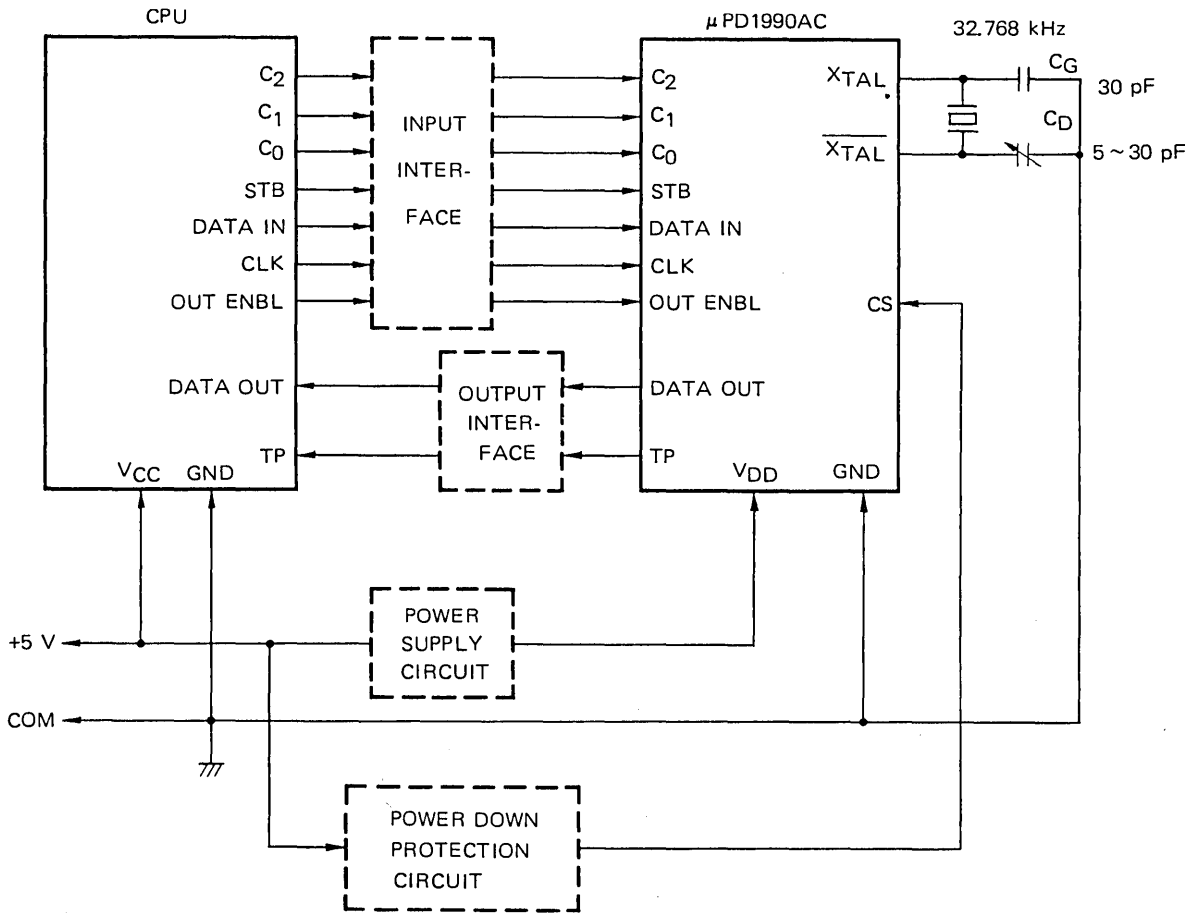
Output circuits

(for DATA OUT, TP terminals)

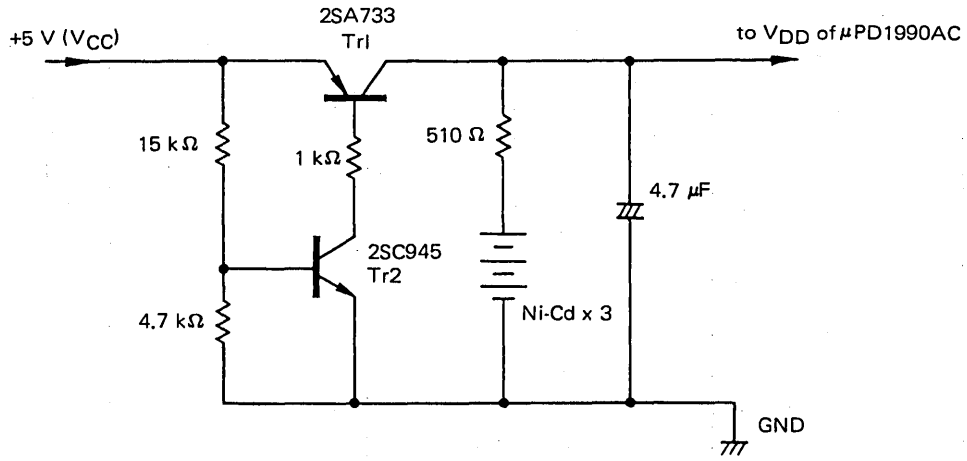


N-channel Open Drain

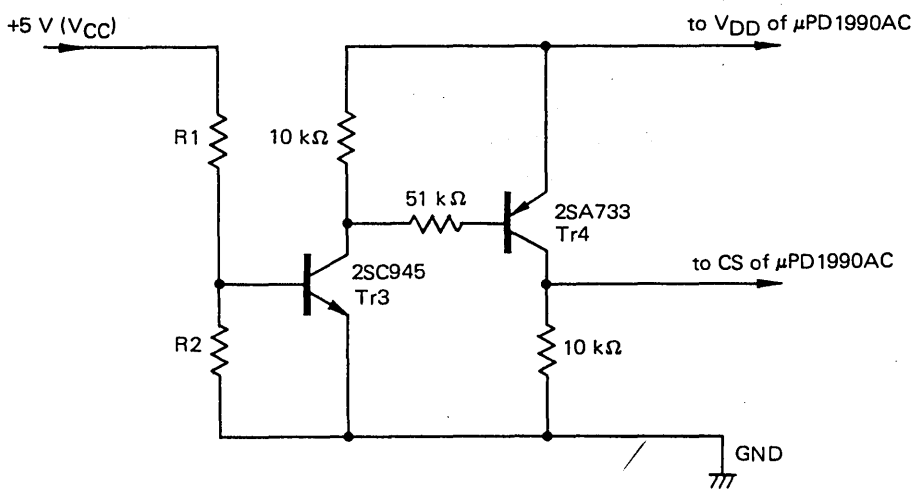
APPLICATION CIRCUIT



POWER SUPPLY CIRCUIT



POWER DOWN PROTECTION CIRCUIT

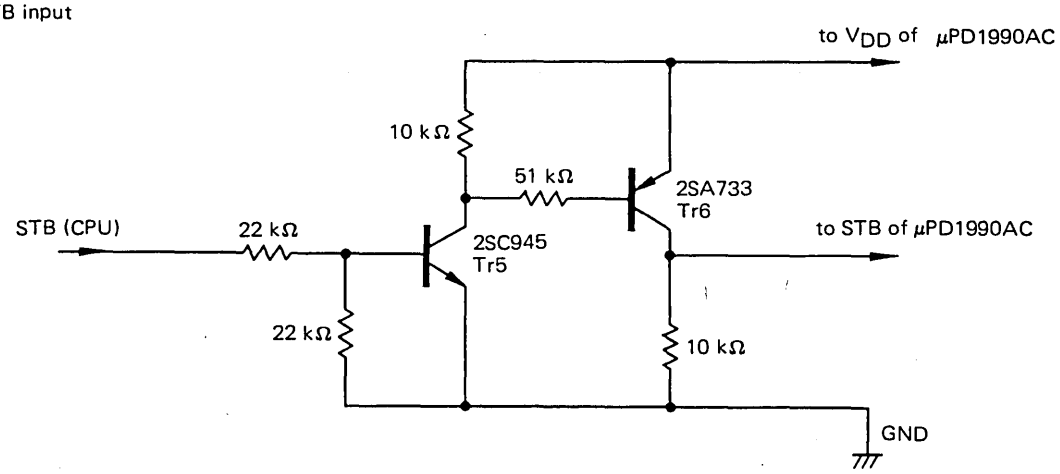


The Power Down of V_{CC} line makes CS terminal inactive, with R1 and R2 resistors. The trigger level of this circuit is calculated as following.

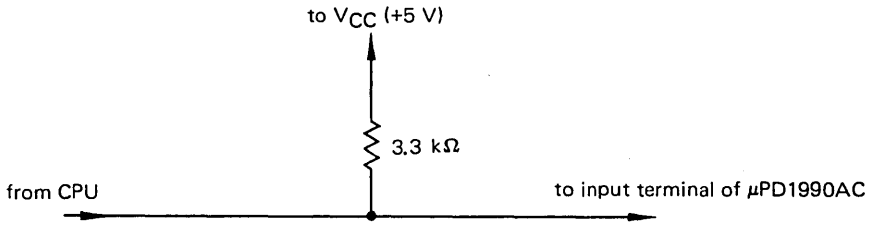
$$V_{trigger} = \frac{(R1+R2)\cdot V_{BE}Tr3}{R2}$$

INPUT INTERFACE

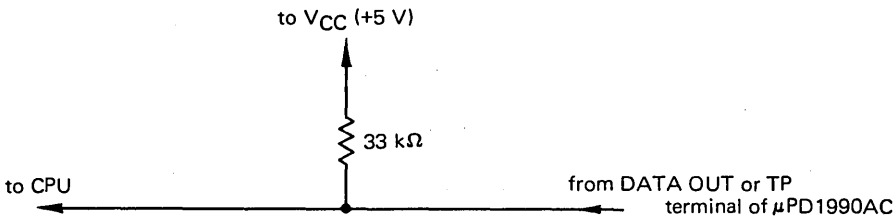
For STB input



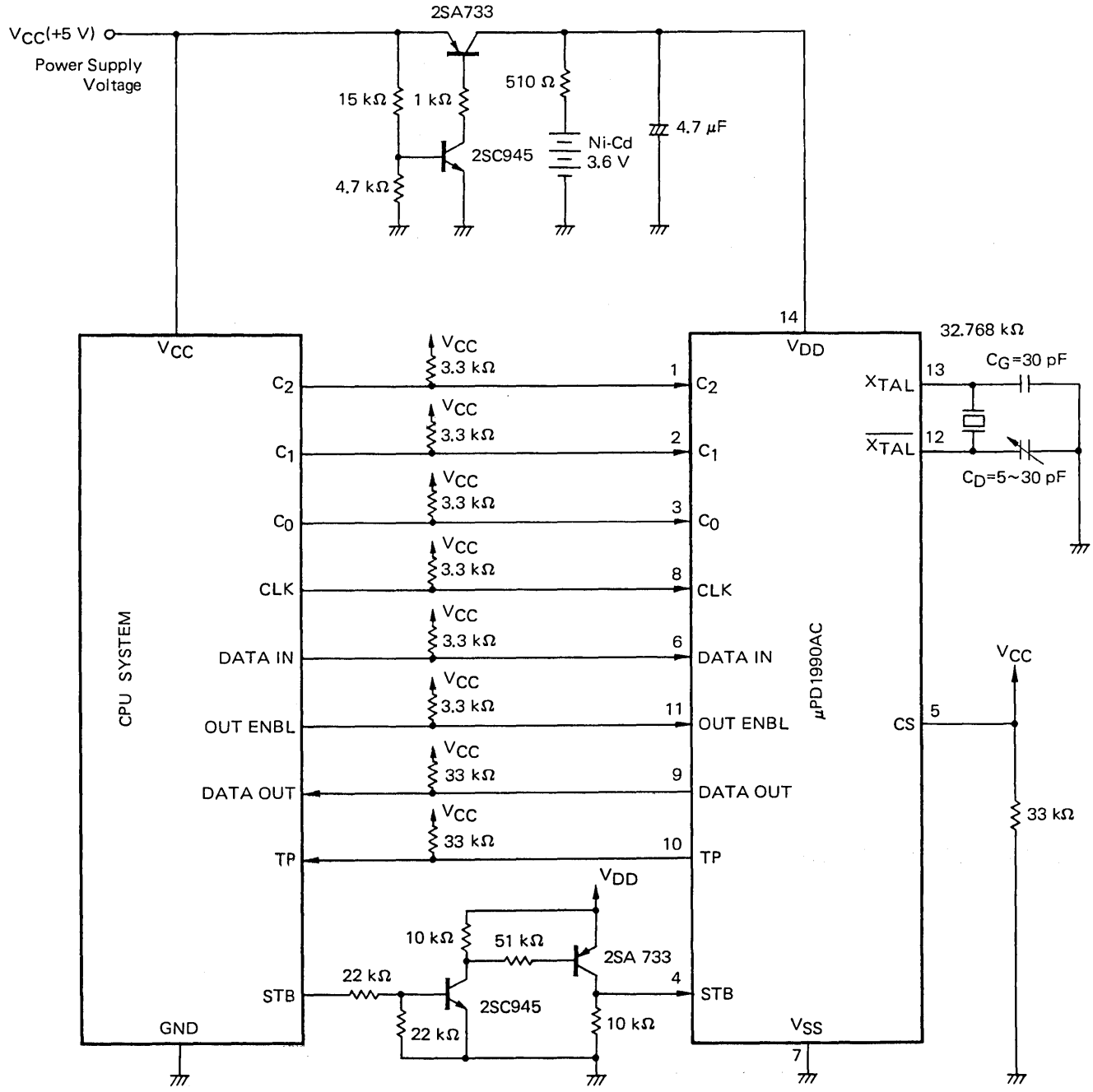
For other input (C2, C1, C0, DATA IN, CLK, OUT ENBL)



OUTPUT INTERFACE (DATA OUT, TP)



APPLICATION



MOS DIGITAL INTEGRATED CIRCUIT

μPD6517P3

3.5 DIGIT MULTIPLEXED LCD QUARTZ WATCH

CMOS LSI

*** This LSI is supplied in dice form only.**

The μPD6517P3 is a CMOS LSI for an electronic wrist watch operated on the oscillation source of 32.768 kHz. A multiplexed (1/2 duty and 1/2 bias) 3.5-digit liquid crystal display element in 12-hour or 24-hour system is used with the LSI.
The functions of basic time ('hour', 'minute', and 'second' and calendar ('month' and 'date') are provided.

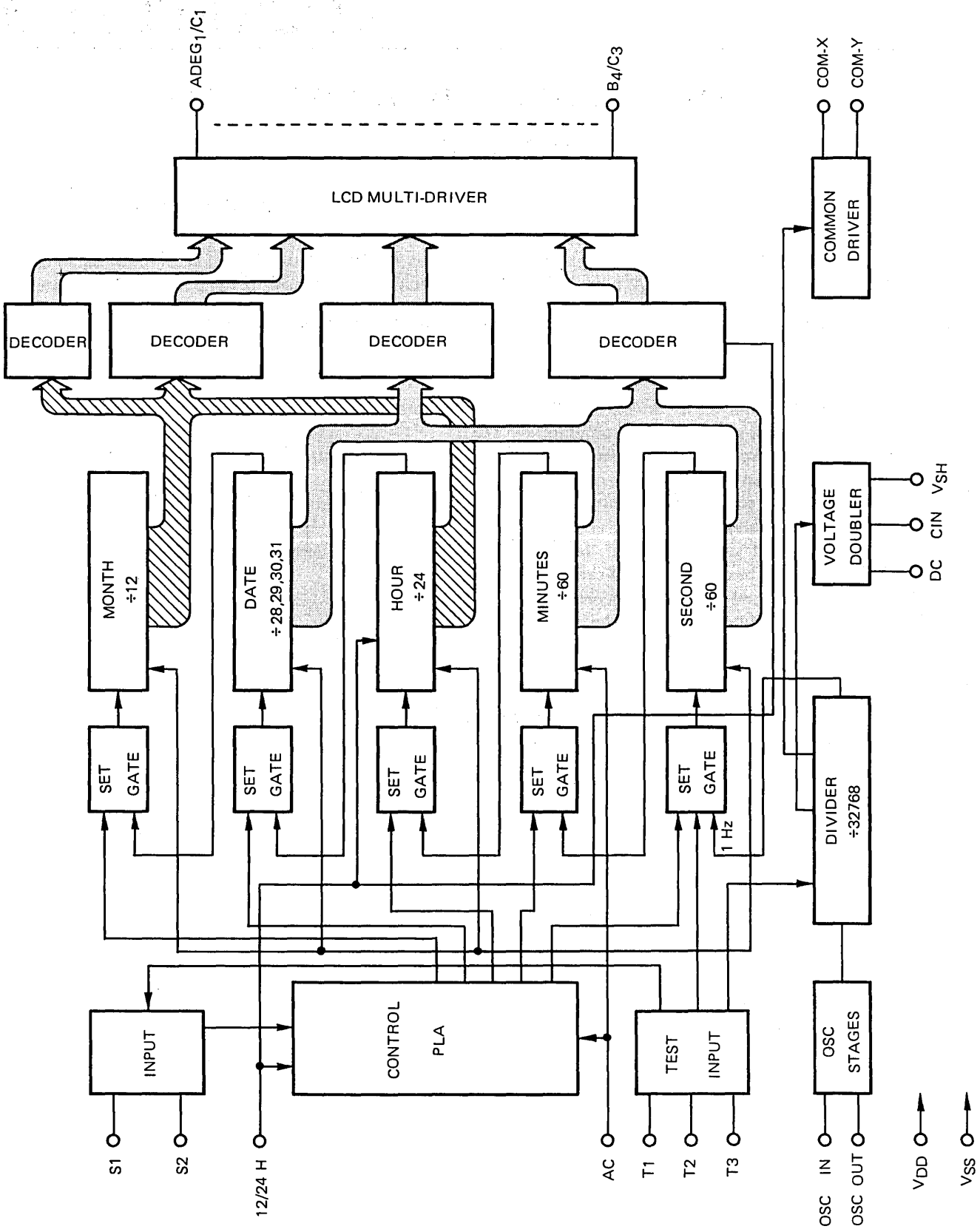
FEATURES

(1) All output terminals for driving liquid crystal elements are arranged on one side of the chip.
(2) The display is standard 3.5 digit multiplexed LCD.
(3) Basic time displays 'hour and minute'. By operating switches, 'month and date' or 'second' can be displayed.
(4) Two operation switches are provided.
(5) The display automatically returns to 'hour and minute' display about 2 seconds after performing 'month and date' display.
(6) Correction of 'second', 'minute', 'hour', 'date', and 'month' can be done separately.
(7) The place to be corrected is indicated by blinking.
(8) One touch correction of ±30 seconds.
(9) 12-hour or 24-hour system can be optionally selected by bonding.
(10) Voltage doubler circuit is integrated within.

Outline of Functions

(1) Normal display	'hour and minute'
(2) Calendar display	'month and date'
(3) Second display	'second'

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (T_a=25 °C)

Supply Voltage (1)	$V_{DD}-V_{SS}$	−0.3 to +5.0	V
Supply Voltage (2)	$V_{DD}-V_{SH}$	−0.3 to +5.0	V
Operating Temperature	Topt	−10 to +60	°C
Storage Temperature	Tstg	−40 to +125	°C

RECOMMENDED OPERATING CONDITIONS

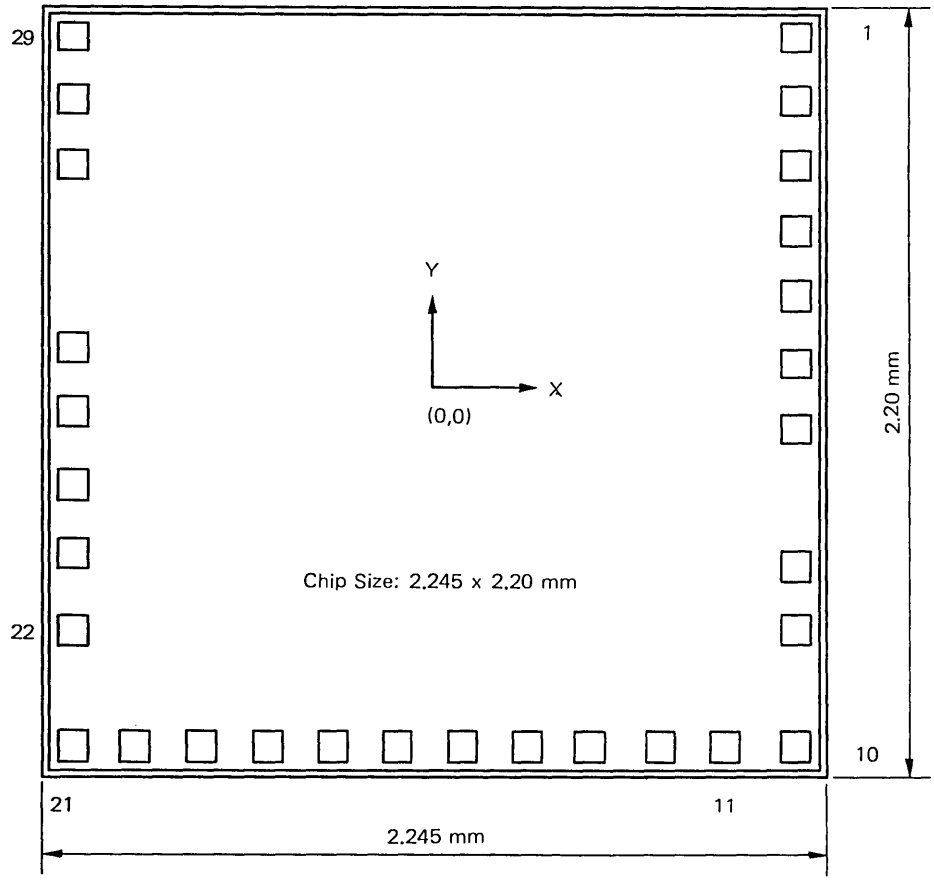
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating Voltage 1	$V_{DD}-V_{SS}$	1.3	1.55	1.7	V
Operating Voltage 2	$V_{DD}-V_{SH}$	2.2	3.0	3.4	V

ELECTRICAL CHARACTERISTICS

(V_{DD}=common, $V_{DD}-V_{SS}$=1.55 V, $V_{DD}-V_{SH}$=3.1 V, f_o=32.768 kHz, CI=30 kΩ, C_G=33 pF, C_D: integrated within T_a=25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDIITON
Operating Voltage Range 1	$V_{DD}-V_{SS}$	1.2	1.55	1.8	V	Functional Operation
Operating Voltage Range 2	$V_{DD}-V_{SH}$	2.0	3.0	3.6	V	Functional Operation
Current Consumption	I_{DD}		0.8	1.5	μA	C_1=C_2=0.1 μF no load
Oscillation Start Voltage	V_{STA}			1.4	V	t_{STA}≤10 s
Frequency Stability	$\lvert\Delta f/f_o\rvert$:($V_{DD}-V_{SS}$)			3	ppm	C_G=20 pF, $V_{DD}-V_{SS}$= 1.45 to 1.55 V
Frequency Adjustment Range	$\lvert\Delta f/f_o\rvert$: C_G	50			ppm	C_G=5 to 33 pF
S1, S2 Input Current	I_{IN}	3	10	60	μA	$V_{DD}-V_I$=0V
T1 T3, AC Input Current	I_{IN}	50	150	400	μA	$V_{DD}-V_I$=0 V
Common Output Current	I_P, I_N	3	16		μA	$V_{DD}-V_O$=0.2 V
Segment Output Current	I_P, I_N	0.5	5		μA	$V_{DD}-V_O$=0.2 V
Doubler Voltage	V_{SHD}	2.8			V	R_L=3 MΩ, C_1=C_2= 0.1 μF
Integrated Capacitor	C_D		20		pF	f=10 kHz, Vp-p=0.1 V

TERMINOLOGY AND COORDINATES OF PAD



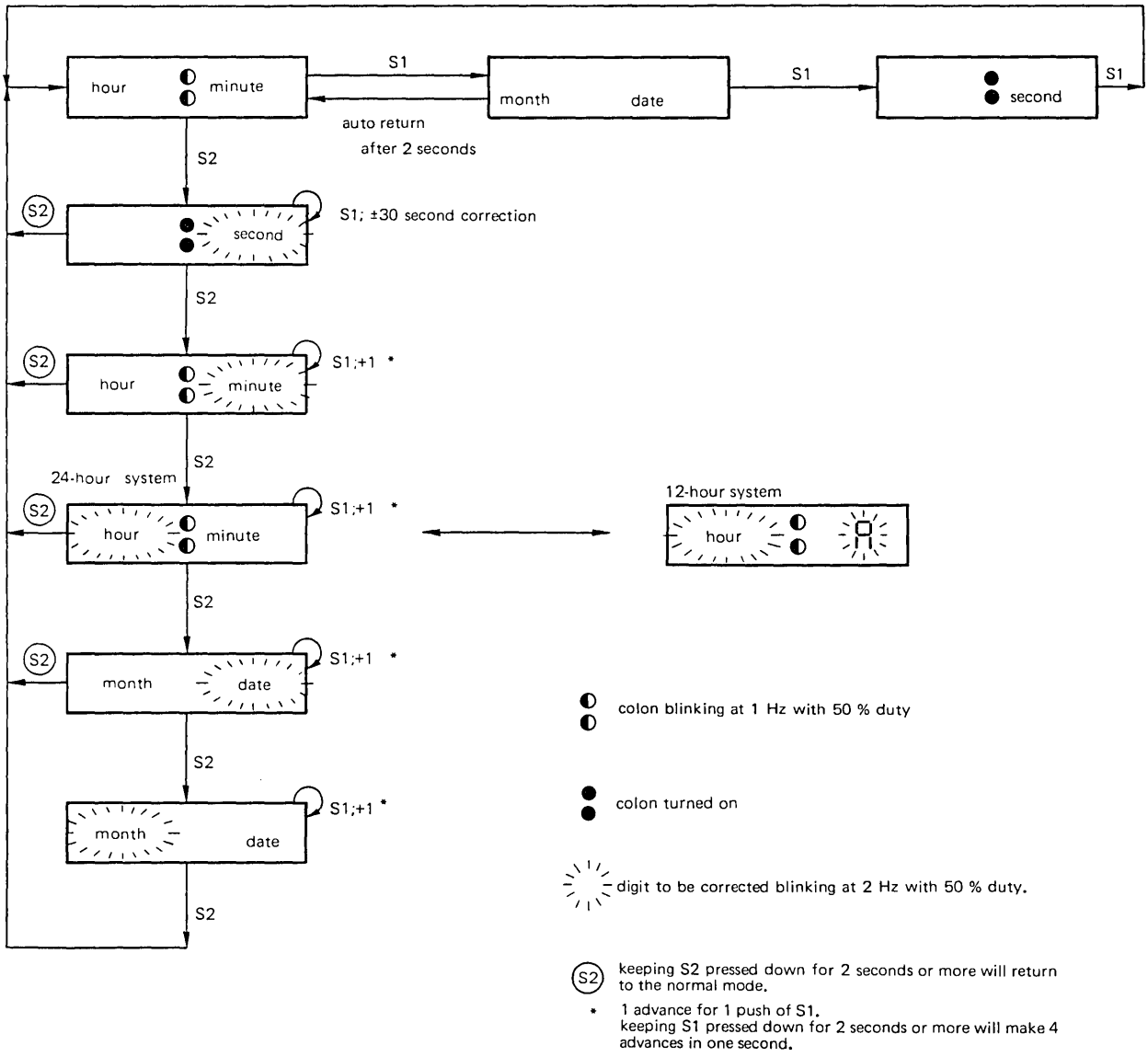
The origin of coordinates is the center of chip.

PAD NO.	TERMINOLOGY	COORDINATES X	COORDINATES Y
1	T3	1003	982
2	T2		799
3	T1		617
4	VSS		435
5	12/24		253
6	VDD		71
7	OSC IN		−111
8	OSC OUT		−487
9	COM Y		−669
10	C1/ADEG1		−982
11	D2/B1	818	
12	E2/F2	635	
13	G2/A2	453	
14	C2/B2	271	
15	D4/COL	89	

PAD NO.	TERMINOLOGY	COORDINATES X	COORDINATES Y
16	E3/F3	−92	−982
17	G3/AD3	−275	
18	C3/B3	−457	
19	E4/F4	−639	
20	G4/A4	−821	
21	C4/B4	−1003	
22	COM X		−669
23	S1		−453
24	S2		−270
25	AC		−73
26	C1N		108
27	DC		617
28	C2N(VSH)		799
29	VDD		982

(Unit: μm)

OPERATION DIAGRAM



☆ Time after all clear has been performed (AC on)
12-hour system: January 1st 1 o'clock 00 minute 00 second (set to AM 1 o'clock)
24-hour system: January 1st 0 o'clock 00 minute 00 second.

☆ Date can be set to any one of 1 to 31 regardless of the month.
When "hour-minute" display is recovered after the calendar correction, non existing date (e.g. February 31) is corrected to the first day of the next month.

☆ In this watch, February ends at 28th.
But, the date February 29 which has been set in 'date' correction mode, is preserved when 'month-date' display mode is recovered.

☆ When 'hour' digit is being corrected in 12-hour system, 'A' or 'P' will be displayed corresponding to AM ro PM.

FUNCTIONS OF PADS

(1) AC Pad

By connecting this AC pad to V_{DD}, all counters are all-cleared to January 1, 1 o'clock 00 minute 00 second (i.e. set to AM 1'clock) in 12-hour system, or January 1, 0 o'clock 00 minute 00 second in 24-hour system.

The AM or PM mark for 12-hour system is only displayed in correction mode.

If a capacitor of 0.01–0.1 μF is connected between this pad and V_{DD}, all counters are cleared every time when power is turned on.

Some disorder in the display may happen after the power is turned on, but the functional display is recovered by correcting time and calendar.

(2) DC, C_{1N}, V_{SH} Pad

A voltage doubler is contained inside.

The double voltage is avaialble on Pad V_{SH} if capacitor of 0.047–0.33 μF is connected from outside between Pad DC and Pad C_{1N}, and between Pad V_{SH} and V_{DD}.

The doubled voltage is supplied to liquid crystal driving power source.

(3) S1 Pad

When this Pad is connected to V_{DD}, either of the following actions is performed.

(i) In the case of ordinary display function, change-over between the display functions of the ordianry display is performed.

(ii) In correction modes, every time when S1 is connected to V_{DD}, the content of the blinking digit advances by 1 (1 push 1 advance), except for 'second'. When 1 push reset to 00 second if the second is displayed between 01 and 29 seocnd, and advance to 1 minute if the secodn is displayed between 30 and 59 second. When this pad is kept connected to V_{DD} for 2 seconds, the content of the blinking digit advances by 4 in a second (4 pulses per second).

(iii) When normal display mdoe is changed from 'hour and minute' to 'month and date', the display automatically returns to 'hour and minute' display after about 2 seconds.

(4) S2 Pad

When this pad is connected to V_{DD}, either of the following actions is performed.

(i) In normal display mode, 'second' starts to blink to indicate that 'second' correction mode is taken.

(ii) In correction mode, the digit to be corrected is changed from one to another.

(iii) In correction mode, holding this pad connected to V_{DD} for 2 seconds or more makes 'hour and minute' of normal display mode be recovered.

(5) 12/24 Pad

Connection of this pad to V_{DD} makes 12-hour system operate and to V_{SS} makes 24-hour system operate.

(6) T1, T2, and T3 Pad

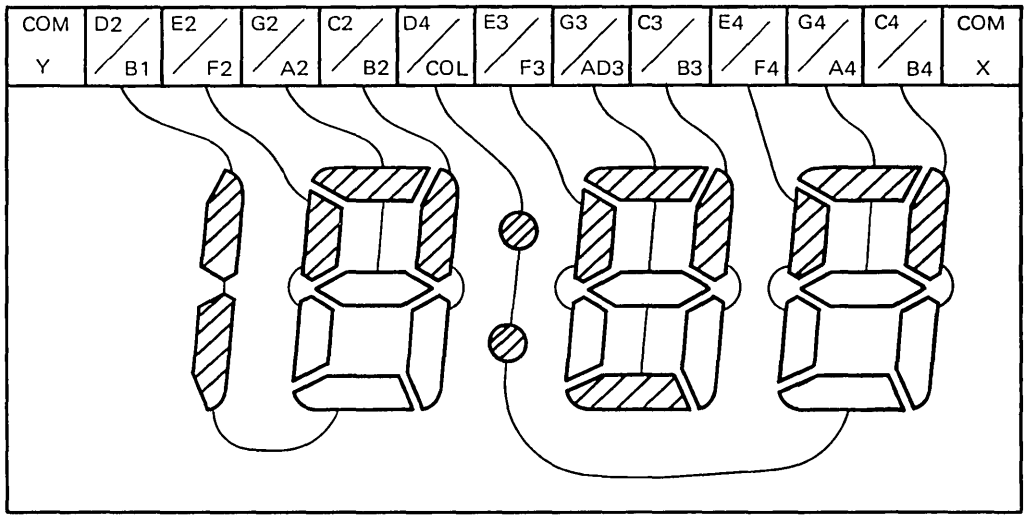
(i) These pad are provided for testing.
In normal operations they should be kept open.

(ii) These pads are used to test with an IC tester, tests cannot be done with liquid crystal elements loaded because the liquid crystal elements should be driven by DC voltaege (i.e. High or Low level).

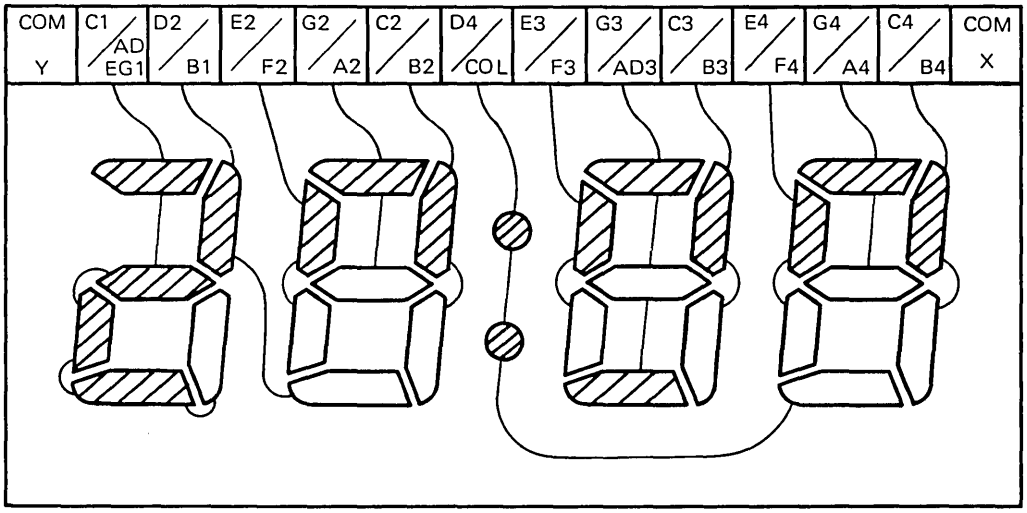
(iii) The process and test patterns for testing with an IC tester should be consulted with the respective separate specifications.

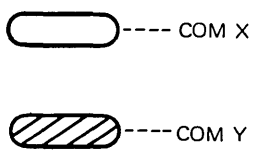
LCD FORMAT

12-Hour System Display

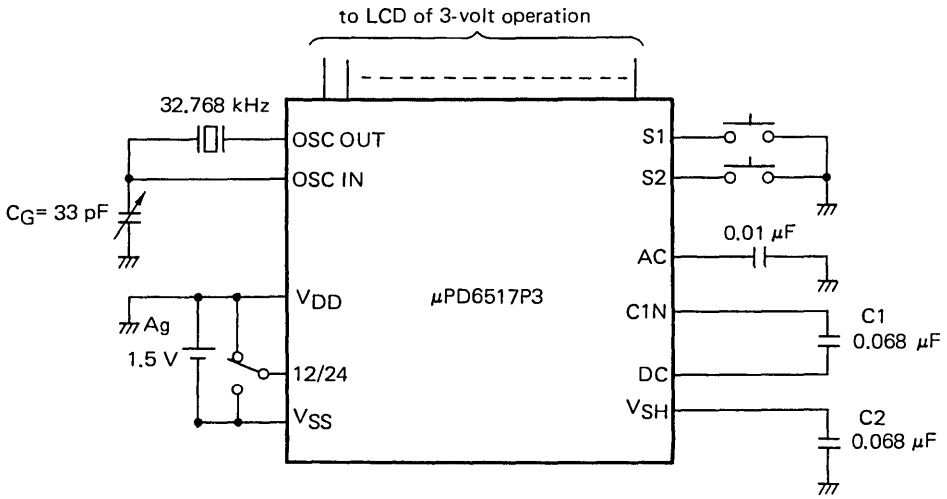


24-Hour System Display





APPLICATION CIRCUIT



INDEX

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC494C

SWITCHING REGULATOR CONTROL CIRCUIT
SILICON MONOLITHIC BIPOLAR INTEGRATED CIRCUIT

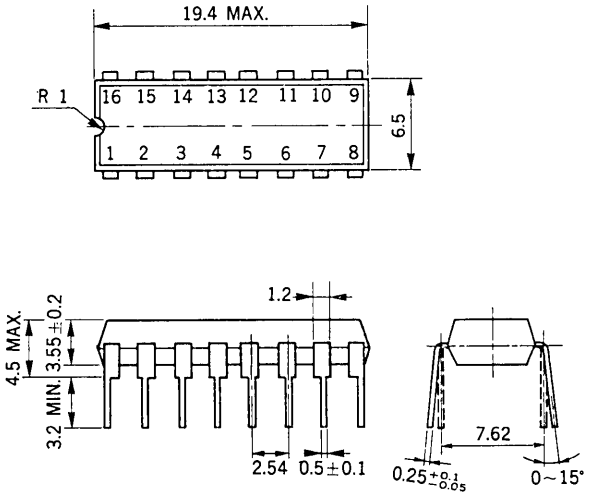
DESCRIPTION

The μPC494C is an inverter control unit which provides all the control circuitry for PWM type switching regulators. Included in this device is the voltage reference, dual error amplifiers, oscillator, pulse width modulator, pulse steering flip flop, dual alternating output switches and dead time control.

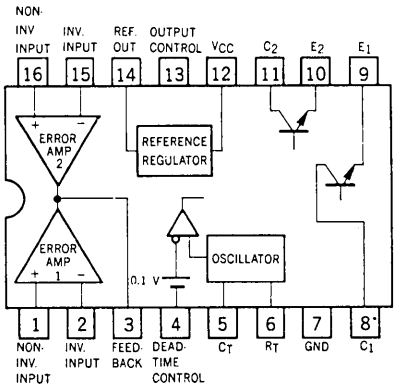
FEATURES

- Complete PWM Power Control Circuit.
- Adjustable Dead-time (0 to 100 %).
- No Double pulsing of same output during load transient condition.
- Dual error amplifiers have wide common mode input voltage capability (−0.3 V to V_{CC}−2 V).
- Circuit architecture provides easy synchronization.
- Uncommitted outputs for 250 mA sink or source.
- With Miss-operation Prevention Circuit for low level supply voltage.
- Full Pin-Compatible TL494C.

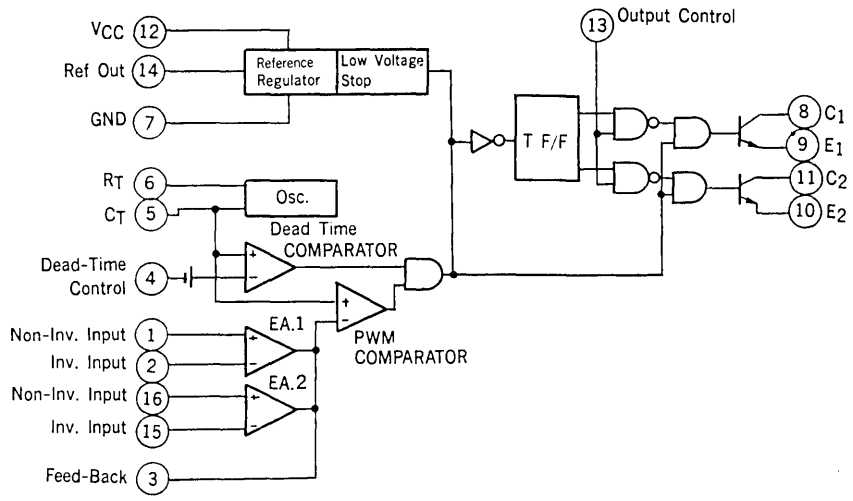
PACKAGE DIMENSIONS (Unit : mm)



CONNECTION DIAGRAM (Top View)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Supply Voltage	V_{CC}	41	V
Error Amplifier Input Voltage	V_{ICM}	V_{CC}+0.3	V
Output Voltage	V_{CER}	41	V
Output Current	I_C	250	mA
Total Power Dissipation	$P_{T(T_a=25\,°C)}$	1000	mW
Operating Temperature Range	T_{opt}	−20 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	7		40	V
Output Voltage	V_{CER}	−0.3		40	V
Output Current	I_C			200	mA
Error Amplifier Sink Current	I_{OAMP}			−0.3	mA
Timing capacitor	C_T	0.47		10000	nF
Timing Resistance	R_T	1.8		500	kΩ
Oscillation Frequency	f_{osc}	1		300	kHz
Operating Temperature	T_{opt}	−20		+70	°C

ELECTRICAL CHARACTERISTICS (V_{CC}=15 V, f=10 kHz, −20 ≦ T_a ≦ +70 °C, unless otherwise noted)

BLOCK	CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Reference Section	Output Voltage		V_{ref}	4.75	5	5.25	V	I_{ref}=1 mA, T_a=25 °C
	Line Regulation		REG_{IN}		8	25	mV	7 V≦V_{CC}≦40 V I_{ref}=1 mA, Ta=25 °C
	Load Regulation		REG_L		1	15	mV	1 mA≦I_{ref}≦10 mA, T_a=25 °C
	Temperature Coefficient		V_{ref}		0.01	0.03	%/°C	−20 °C≦T_a ≦ +85 °C I_{ref}=1 mA
	(Note 2) Short Circuit Output Current		I_{short}		50		mA	V_{ref}=0, T_a=25 °C
Oscillator Section	Frequency		f_{osc}		10		kHz	C_T=0.01 μF, R_T= 12 kΩ, T_a=25 °C
	(Note 1) Standard Deviation of Frequency				10		%	7 V≦V_{CC}≦40 V, C_T, R_T, const. T_a=25 °C
	Frequency Change with Temperature				1	2	%	0 °C≦T_a≦70 °C, C_T=0.01 μF R_T=12 kΩ
	Frequency Change with Voltage					1	%	7V≦V_{CC}≦40 V, C_T=0.01 μF T_a=25 °C, R_T=12 kΩ
Dead-time Control Section	Input Bias Current				−2	−10	μA	0≦V_I≦5.25 V
	Maximum Duty Cycle (Each Output)			45	49		%	V_I=0
	Input Threshold Voltage		V_{th}		3	3.3	V	Zero duty cycle
				0				Maximum duty cycle
Error Amplifier Section	Input Offset Voltage		V_{IO}		2	10	mV	V_{OAMP}=2.5 V
	Input Offset Current		I_{IO}		25	250	nA	V_{OAMP}=2.5 V
	Input Bias Current				0.2	1	μA	V_{OAMP}=2.5 V
	Common Mode Input Voltage	Low	V_{ICM}	−0.3			V	7 V≦V_{CC}≦40 V
		High		V_{CC}-2				
	Open-loop Voltage Amplification		A_V	60	80		dB	V_{OAMP}=0.5 V to 3.5 V, T_a=25 °C
	Unity Gain Bandwidth			500	830		kHz	T_a=25 °C
	Common Mode Rejection Radio		CMR	65	80		dB	V_{CC}=40 V, T_a=25 °C
	Output Sink Current			0.3	0.7		mA	V_{OAMP}=0.7 V
	Output Source Current			−2	−10		mA	V_{OAMP}=3.5 V

Note 1: Standard deviation is a measure of the statistical distribution about the mean as derived from the formula;

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (X_n - \bar{X})^2}{N-1}}$$

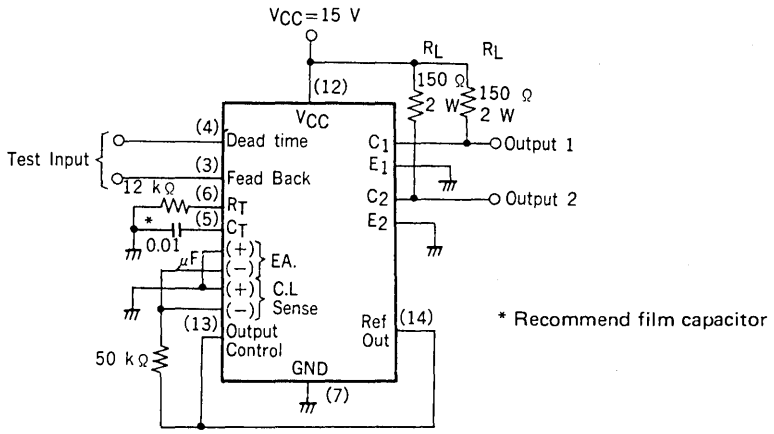
Calculation expression of frequency f_{osc} is as follows

$$f_{osc} \fallingdotseq \frac{1}{0.817\, R_T \cdot C_T + 1.42 \cdot 10^{-6}} \text{ (Hz)} \qquad [R_T] = \Omega,\ [C_T] = F$$

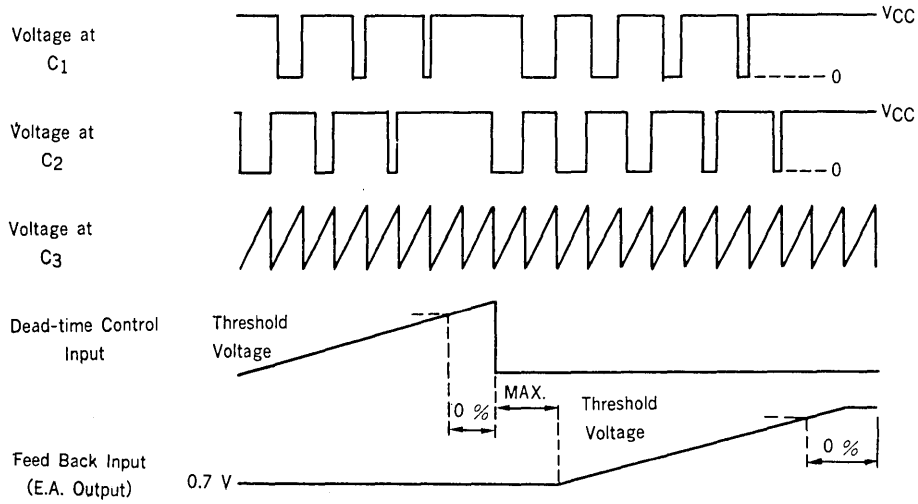
Note 2: Maximum duration of short circuit cond. is one second. (non repetitive)

BLOCK	CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
PWM Section	Input Threshold Voltage				4	4.5	V	Zero Duty Cycle
	Input Sink Current			0.3	0.7		mA	$V_{(pin\ 3)}$=0.7 V
Output Section	Collector Cutoff Current		I_{CER}		2	100	μA	V_{CE}=40 V, V_{CC}=40 V
	Emitter Cutoff Current					−100	μA	V_{CC}=V_C=40 V
	Collector Saturation Voltage		$V_{CE(sat)}$		0.95	1.3	V	I_C=200 mA, V_E=0, Common Emitter
			$V_{CE(ON)}$		1.6	2.5	V	I_E=200 mA, V_C=15 V Emitter follower
	Output Voltage Rise Time	common Emitter	t_r		100	200	ns	V_{CC}=15 V, R_L≒150 Ω I_O=100 mA T_a=25 °C
		Emitter follower			100	200	ns	
	Output Voltage Fall Time	common Emitter	t_f		70	200	ns	
		Emitter follower			70	200	ns	
Total Device	Standby Current		$I_{CC(S.B)}$		8	12.5	mA	V_{CC}=15 V all other inputs and outputs open
	Bias Current		$I_{CC(Bl.)}$		10		mA	$V_{(pin\ 4)}$=2 V, see Fig. 1

Fig. 1 Test Circuit



Voltage Waveform

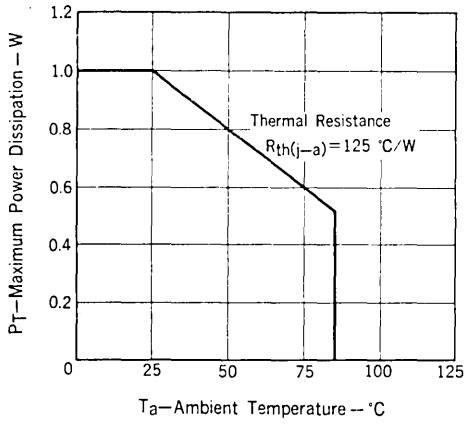


FUNCTION TABLE

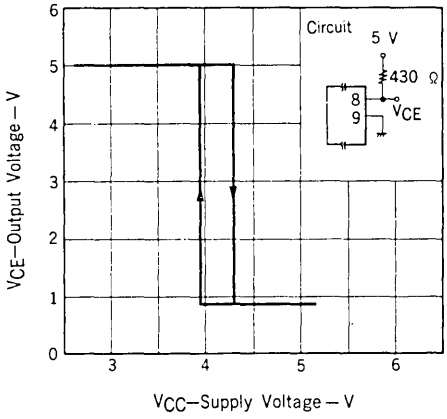
OUTPUT CONTROL INPUT (13 pin)	OUTPUT FUNCTION
At Ref-Out	Normal push-pull operation
Grounded	Single-ended or parallel output

TYPICAL PERFORMANCE CHARACTERISTICS (T_a=25 ± 2 °C, V_{IN}=15 V)

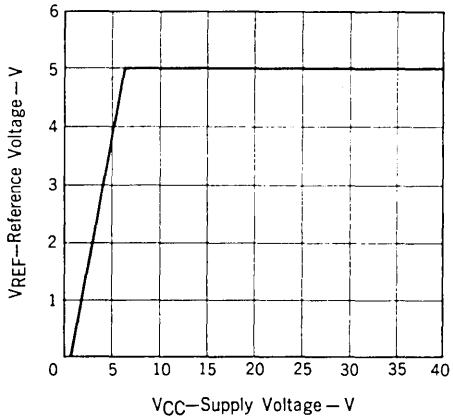
MAXIMUM POWER DISSIPATION



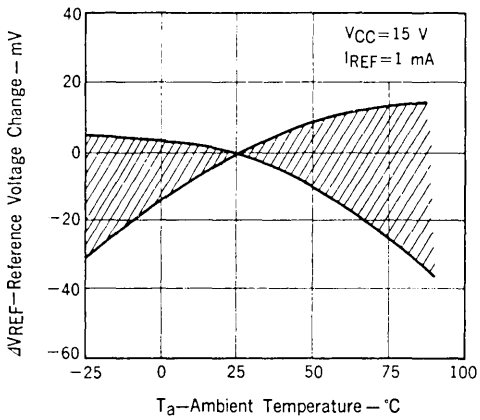
MISS-OPERATION PREVENTION CIRCUIT CHARACTERISTICS



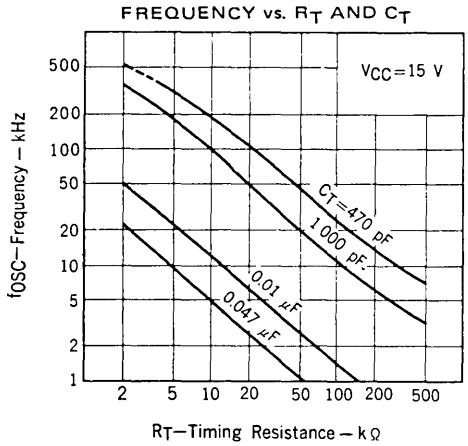
REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



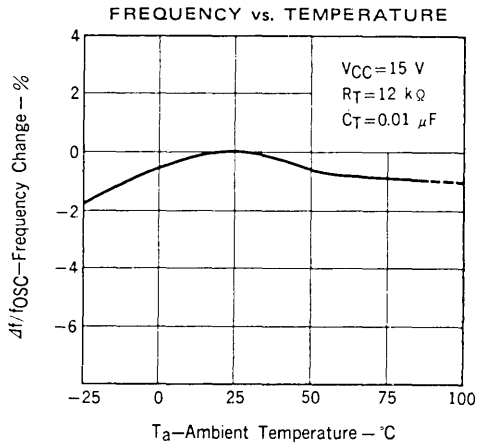
REFERENCE VOLTAGE vs. TEMPERATURE



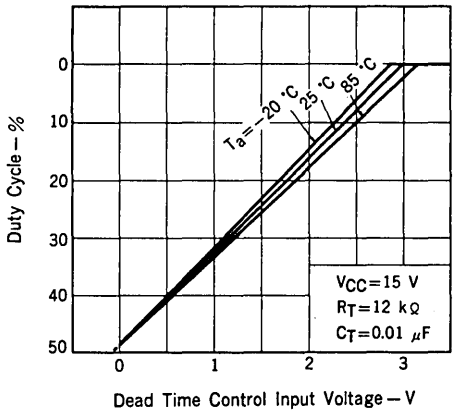
FREQUENCY vs. R_T AND C_T



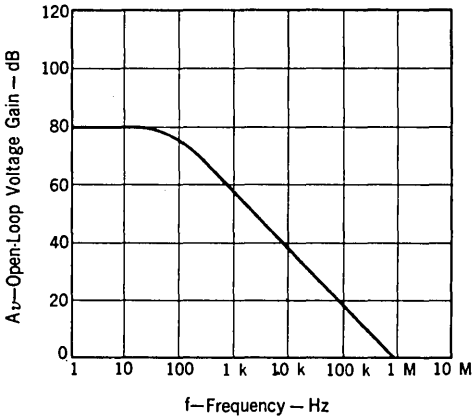
FREQUENCY vs. TEMPERATURE



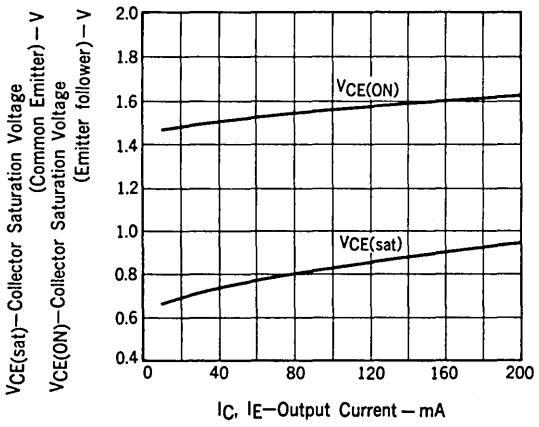
DUTY CYCLE vs. DEAD TIME CONTROL INPUT VOLTAGE



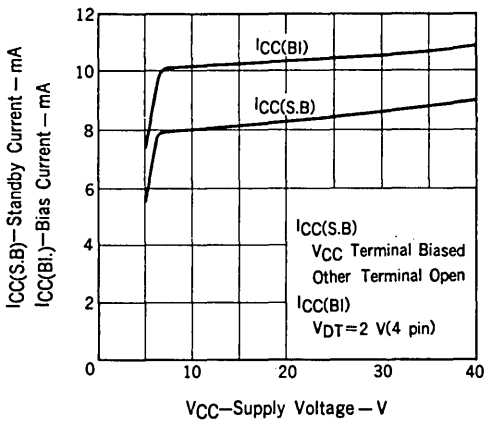
OPEN-LOOP VOLTAGE GAIN vs. FREQUENCY



COLLECTOR SATURATION VOLTAGE vs. OUTPUT CURRENT

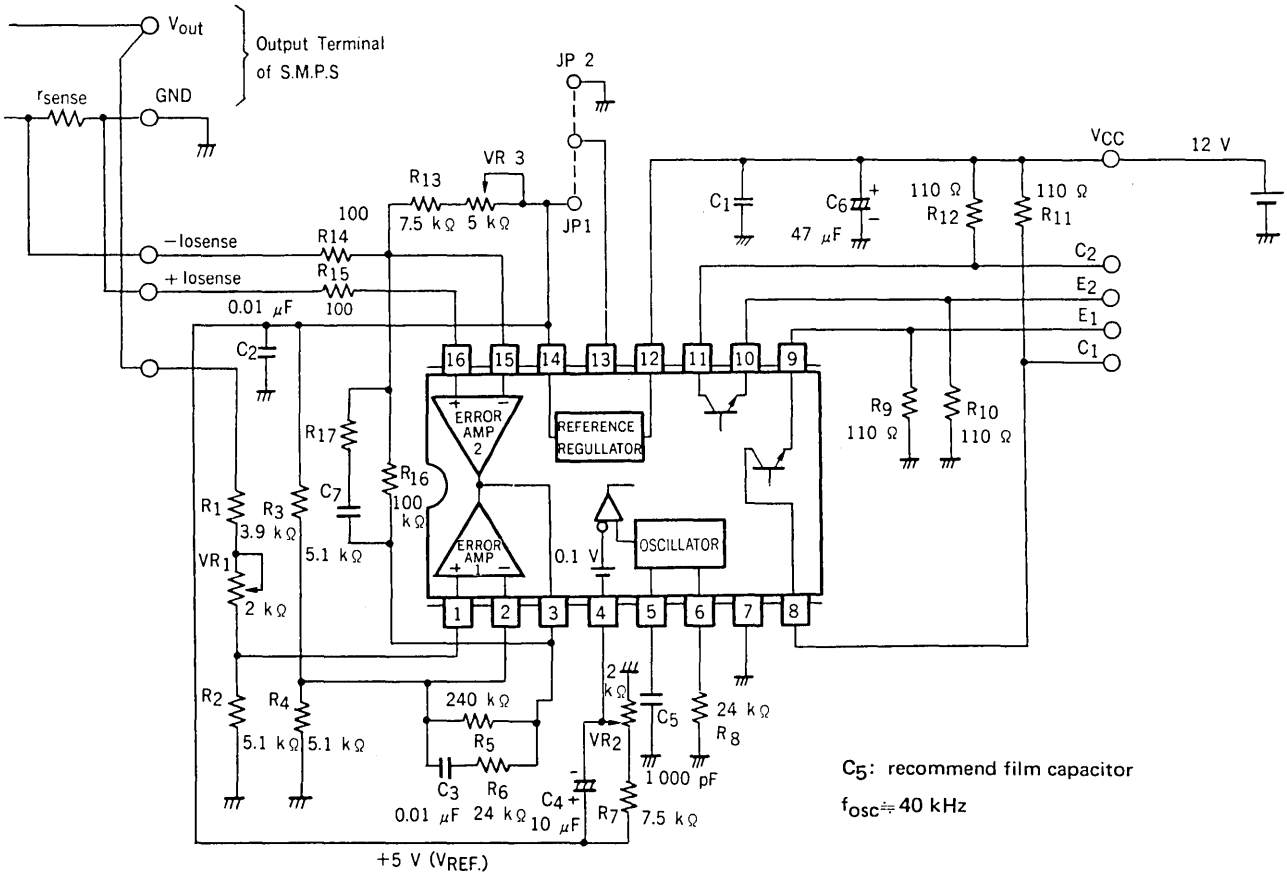


STANDBY AND BIAS CURRENT vs. SUPPLY VOLTAGE



BASIC APPLICATION CIRCUIT

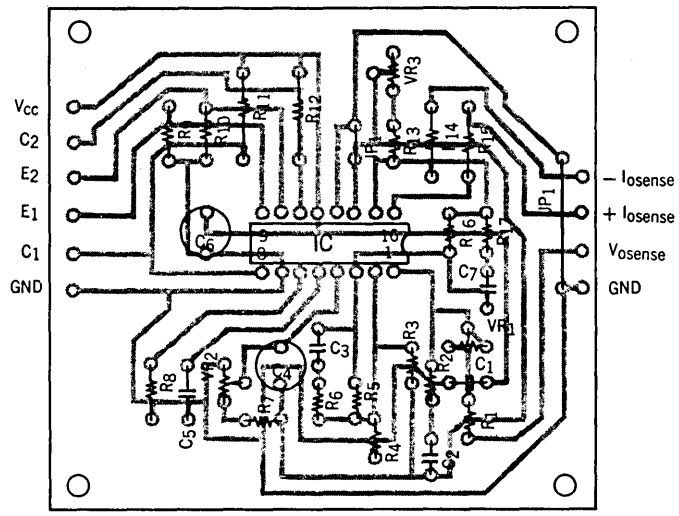
Fig. 2 Circuit



CONNECTION DIAGRAM

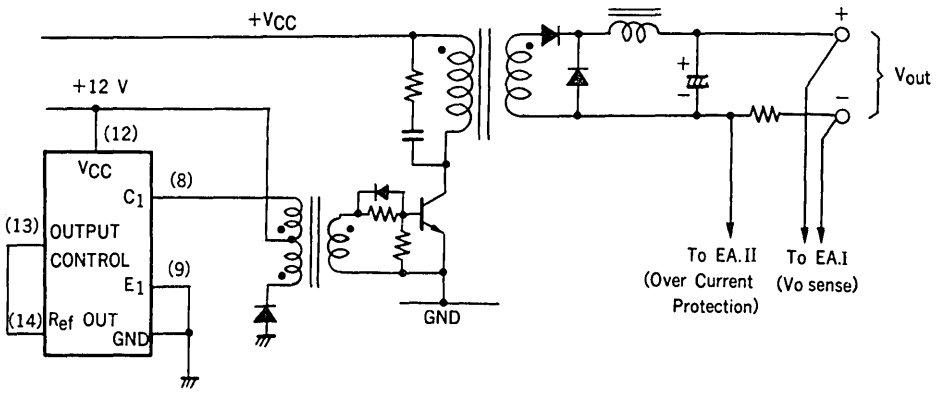
OUTPUT FUNCTION	OUTPUT CONTROL INPUT (13 pin)	OUTPUT MODE	OUTPUT VOLTAGE WAVEFORM
Push-Pull Operation	At Ref-Out (JP1 Wired)	Open Collector (R_9, R_{10} 0 Ω)	C1 C2
		Emitter Follower (R_{11}, R_{12} 0 Ω)	E1 E2
Single-Ended or Parallel Output	Grounded (JP2 Wired)	Open Collector (R_9, R_{10} 0 Ω)	C1,C2
		Emitter Follower (R_{11}, R_{12} 0 Ω)	E1, E2

Printed Pattern (Pattern Side, Actual Size)



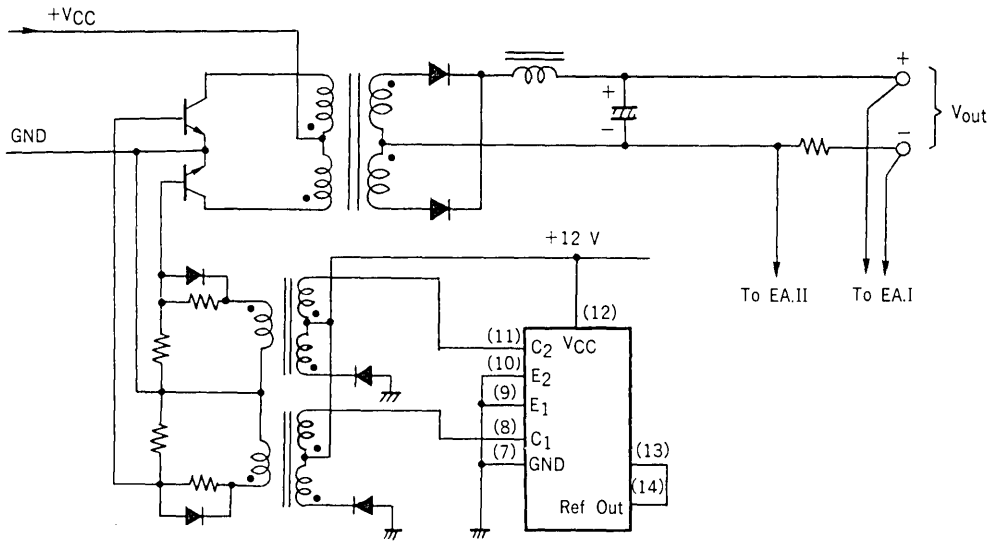
TYPICAL EXAMPLE OF APPLICATION CIRCUITS

1) Forward Type

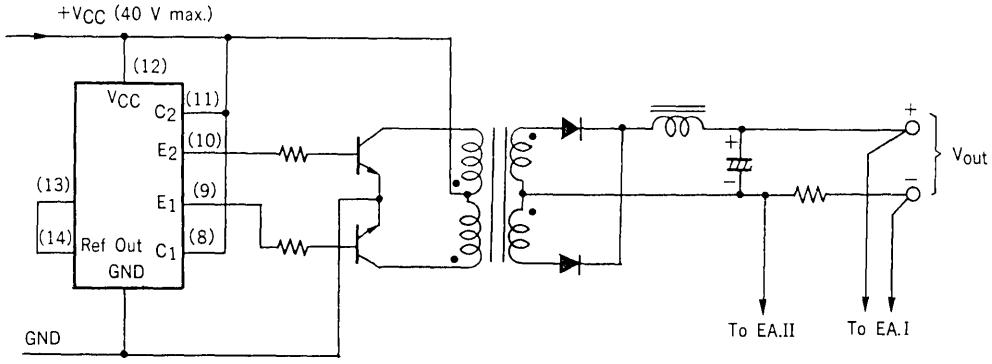


2) Push-Pull Type

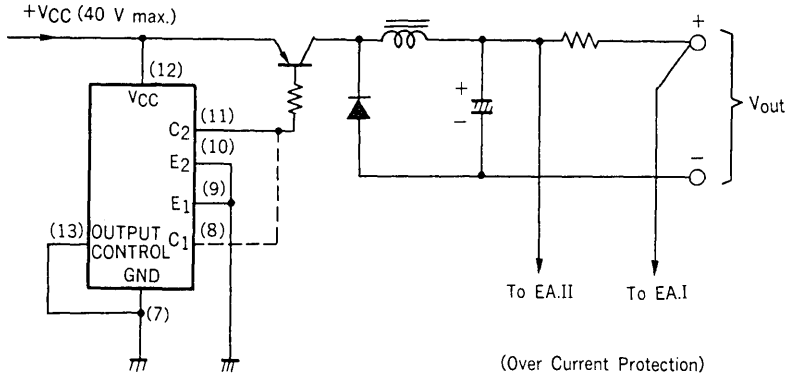
(Isolated)



(Non Isolated)



3) Stepdown Chopper

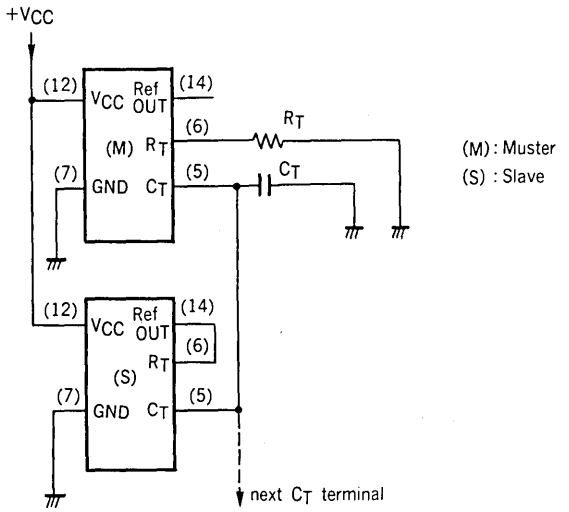


(Over Current Protection)

SYNCRONIZED OPERATION

If syncronized operation is needed, muster-slave circuit can be used. This circuit is shown bellow.

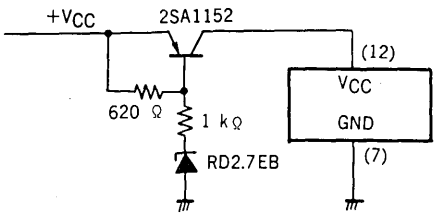
Initially, R_T terminal of slave IC is connected to Pin 14 (Ref Out) and internal oscillator is stopped.



MISS-OPERATION PREVENTION METHOD

If supply voltage (V_{CC}) level drops bellow 2 V to 2.5 V, Miss-Operation Prevention Circuit is stops. But, internal toggle flip-flop is still active condition, and each outputs section are on condition.

So, if prevention circuit from such operation is required, next circuit will be available.



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC494G

SWITCHING REGULATOR CONTROL CIRCUIT
SILICON MONOLITHIC BIPOLAR INTEGRATED CIRCUIT

DESCRIPTION

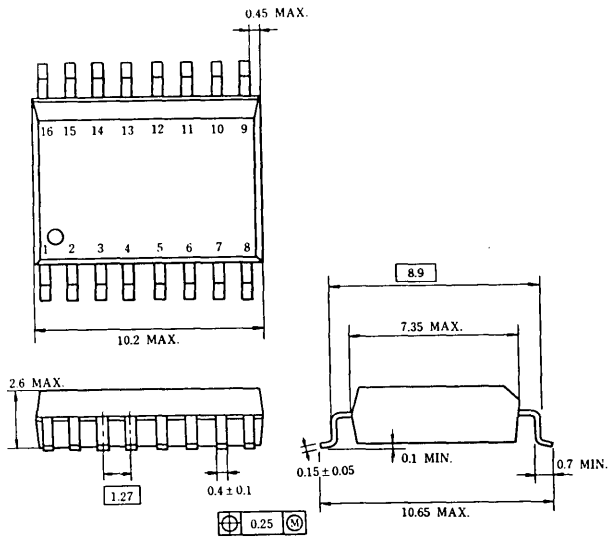
The μPC494G is an inverter control unit which provides all the control circuitry for PWM type switching regulators.

Included in this device is the voltage reference, dual error amplifiers, oscillator, pulse width modulator, pulse steering flip flop, dual alternating output switches and dead time control.

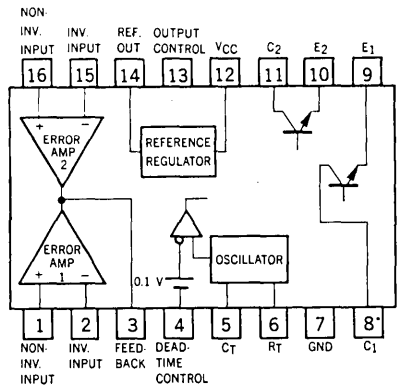
FEATURES

- Complete PWM Power Control Circuit.
- Adjustable Dead-time (0 to 100 %).
- No Double pulsing of same output during load transient condition.
- Dual error amplifiers have wide common mode input voltage capability (−0.3 V to V_{CC}−2 V).
- Circuit architecture provides easy synchronization.
- Uncommitted outputs for 250 mA sink or source.
- With Miss-operation Prevention Circuit for low level supply voltage.
- Equivalent to TL494C.
- Very Small Package. (SO-16L)

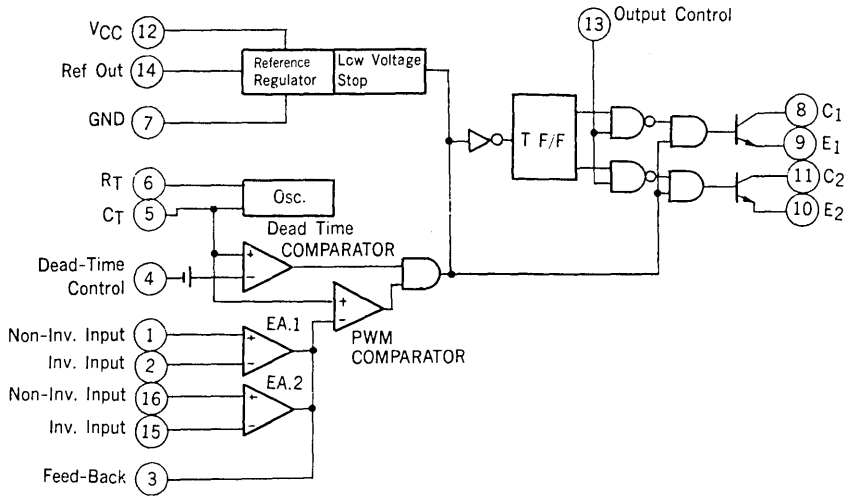
PACKAGE DIMENSIONS (Unit : mm)



CONNECTION DIAGRAM (Top View)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Supply Voltage	V_{CC}	41	V
Error Amplifier Input Voltage	V_{ICM}	V_{CC}+0.3	V
Output Voltage	V_{CER}	41	V
Output Current	I_C	250	mA
Total Power Dissipation	$P_{T(T_a=25\,°C)}$	780*	mW
Operating Temperature Range	T_{opt}	−20 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

* 5 cm x 5 cm Glass-Epoxy PC board is used. (thickness t=1.6 mm)

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	7		40	V
Output Voltage	V_{CER}	−0.3		40	V
Output Current	I_C			200	mA
Error Amplifier Sink Current	I_{OAMP}			−0.3	mA
Timing capacitor	C_T	0.47		10000	nF
Timing Resistance	R_T	1.8		500	kΩ
Oscillation Frequency	f_{osc}	1		300	kHz
Operating Temperature	T_{opt}	−20		+70	°C

ELECTRICAL CHARACTERISTICS (V_{CC}=15 V, f=10 kHz, −20 ≦ T_a ≦ +70 °C, unless otherwise noted)

BLOCK	CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Reference Section	Output Voltage		V_{ref}	4.75	5	5.25	V	I_{ref}=1 mA, T_a=25 °C
	Line Regulation		REG_{IN}		8	25	mV	7 V≦V_{CC}≦40 V I_{ref}=1 mA, Ta=25 °C
	Load Regulation		REG_L		1	15	mV	1 mA≦I_{ref}≦10 mA, T_a=25 °C
	Temperature Coefficient		V_{ref}		0.01	0.03	%/°C	−20 °C≦T_a ≦+85 °C I_{ref}=1 mA
	(Note 2) Short Circuit Output Current		I_{short}		50		mA	V_{ref}=0, T_a=25 °C
Oscillator Section	Frequency		f_{osc}		10		kHz	C_T=0.01 μF, R_T= 12 kΩ, T_a=25 °C
	(Note 1) Standard Deviation of Frequency				10		%	7 V≦V_{CC}≦40 V, C_T, R_T, const. T_a=25 °C
	Frequency Change with Temperature				1	2	%	0 °C≦T_a≦70 °C, C_T=0.01 μF R_T=12 kΩ
	Frequency Change with Voltage					1	%	7V≦V_{CC}≦40 V, C_T=0.01 μF T_a=25 °C, R_T=12 kΩ
Dead-time Control Section	Input Bias Current				−2	−10	μA	0≦V_I≦5.25 V
	Maximum Duty Cycle (Each Output)			45	49		%	V_I=0
	Input Threshold Voltage		V_{th}		3	3.3	V	Zero duty cycle
				0				Maximum duty cycle
Error Amplifier Section	Input Offset Voltage		V_{IO}		2	10	mV	V_{OAMP}=2.5 V
	Input Offset Current		I_{IO}		25	250	nA	V_{OAMP}=2.5 V
	Input Bias Current				0.2	1	μA	V_{OAMP}=2.5 V
	Common Mode Input Voltage	Low	V_{ICM}	−0.3			V	7 V≦V_{CC}≦40 V
		High		V_{CC}-2				
	Open-loop Voltage Amplification		A_V	60	80		dB	V_{OAMP}=0.5 V to 3.5 V, T_a=25 °C
	Unity Gain Bandwidth			500	830		kHz	T_a=25 °C
	Common Mode Rejection Radio		CMR	65	80		dB	V_{CC}=40 V, T_a=25 °C
	Output Sink Current			0.3	0.7		mA	V_{OAMP}=0.7 V
	Output Source Current			−2	−10		mA	V_{OAMP}=3.5 V

Note 1: Standard deviation is a measure of the statistical distribution about the mean as derived from the formula;

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (X_n - \bar{X})^2}{N-1}}$$

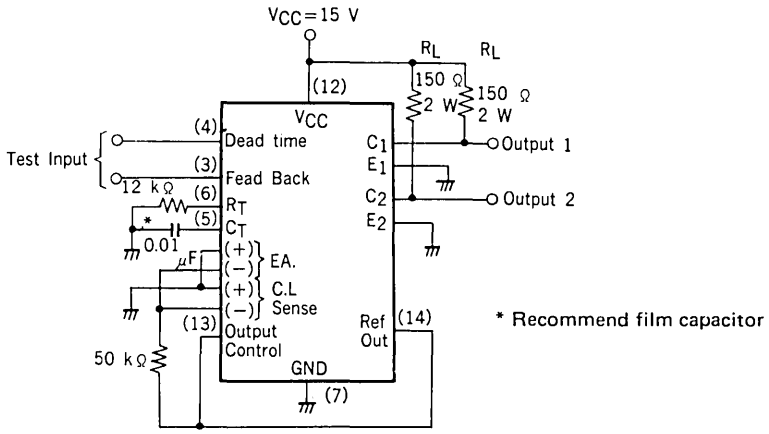
Calculation expression of frequency f_{osc} is as follows

$$f_{osc} \fallingdotseq \frac{1}{0.817\, R_T \cdot C_T + 1.42 \cdot 10^{-6}} \text{ (Hz)} \qquad [R_T] = \Omega,\ [C_T] = \text{F}$$

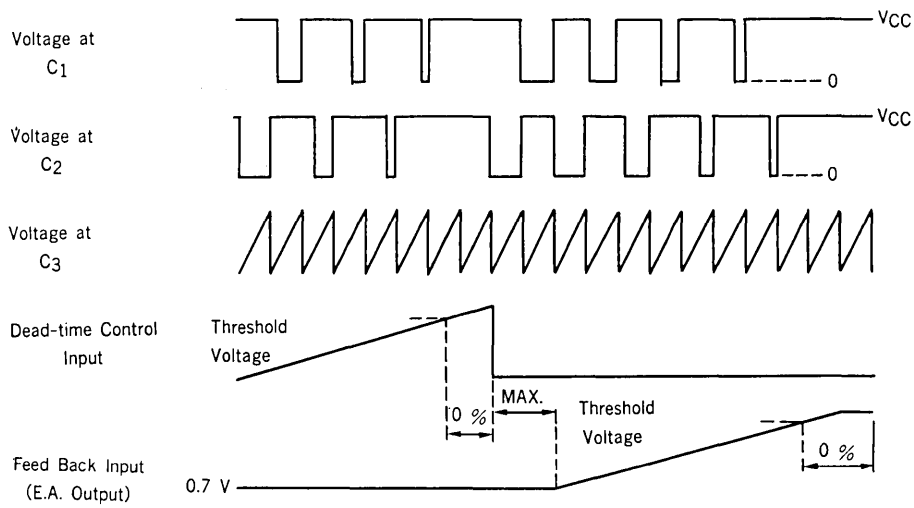
Note 2: Maximum duration of short circuit cond. is one second. (non repetitive)

BLOCK	CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
PWM Section	Input Threshold Voltage				4	4.5	V	Zero Duty Cycle
	Input Sink Current			0.3	0.7		mA	$V_{(pin\ 3)}$=0.7 V
Output Section	Collector Cutoff Current		I_{CER}		2	100	μA	V_{CE}=40 V, V_{CC}=40 V
	Emitter Cutoff Current					−100	μA	V_{CC}=V_C=40 V
	Collector Saturation Voltage		$V_{CE(sat)}$		0.95	1.3	V	I_C=200 mA, V_E=0, Common Emitter
			$V_{CE(ON)}$		1.6	2.5	V	I_E=200 mA, V_C=15 V Emitter follower
	Output Voltage Rise Time	common Emitter	t_r		100	200	ns	V_{CC}=15 V, R_L≒150 Ω I_O=100 mA T_a=25 °C
		Emitter follower			100	200	ns	
	Output Voltage Fall Time	common Emitter	t_f		70	200	ns	
		Emitter follower			70	200	ns	
Total Device	Standby Current		$I_{CC(S.B)}$		8	12.5	mA	V_{CC}=15 V all other inputs and outputs open
	Bias Current		$I_{CC(Bl.)}$		10		mA	$V_{(pin\ 4)}$=2 V, see Fig. 1

Fig. 1 Test Circuit



Voltage Waveform



FUNCTION TABLE

OUTPUT CONTROL INPUT (13 pin)	OUTPUT FUNCTION
At Ref-Out	Normal push-pull operation
Grounded	Single-ended or parallel output

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1394C

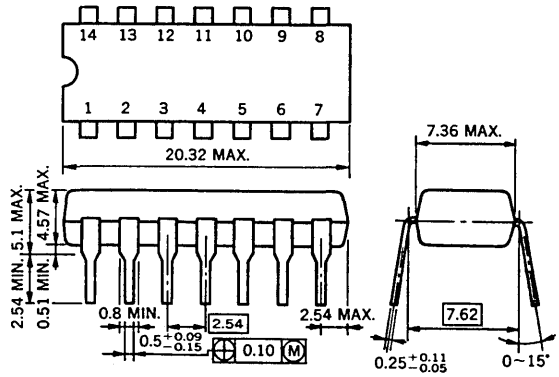
SWITCHING REGULATOR IC FOR TV SET

The μPC1394C is a switching regurator IC especially designed for TV sets. It can be used for both type of TV sets, insulated type and no insulated type.
It operates in synchronizing with the horizontal retrace pulse, so does not generates any visual noise in the picture on CRT.
The output transistor in a powersupply circuit is protected doubly by the internal protection circuit for over load.
ON/OFF operation of the powersupply is able to operated easily without any mechanical relay using provided terminal. So timer operation, remote control and etc. are very easy.

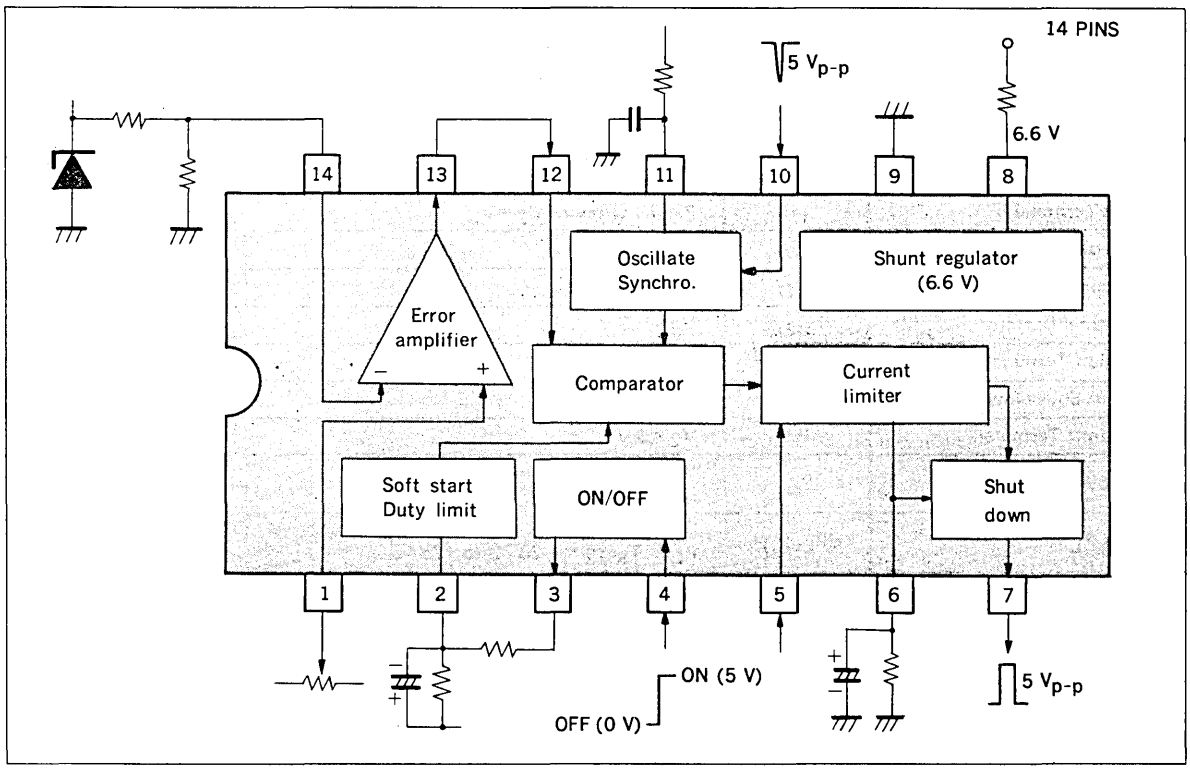
FEATURES

- Wide range of regulating input line voltage.
  : AC 80 to 280 V
- The output power transistor is doubly protected by the current limitter and the shut down circuit.
- No visual noise due to horizontal synchronous operation.
- A terminal for remote control, timer operation and etc. of the powersupply is provided.
- Shut down circuit is easily resetable using ON/OFF terminal.
- Low stand-by and starting current. (2 mA)

PACKAGE DIMENSIONS in millimeters



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

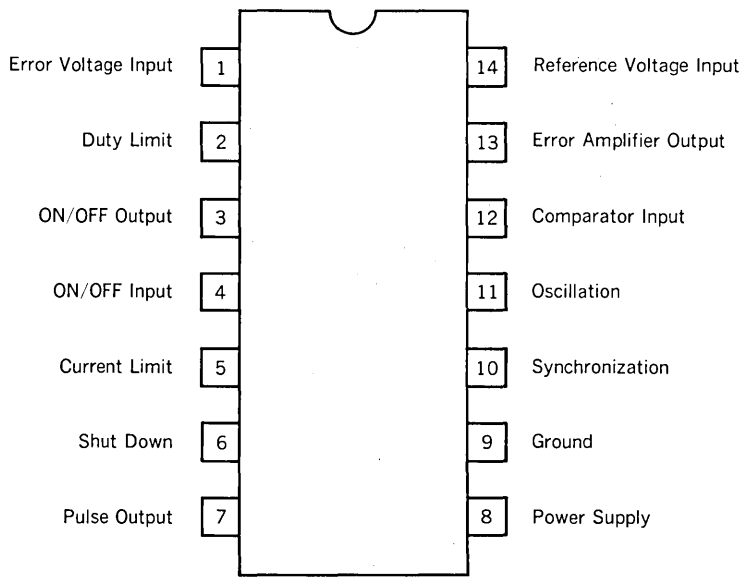
Supply Current	I_8	30	mA
Sink of Output Terminal	I_7	10	mA
Input Voltage of Current Limitter	V_5	3.0	V
Input Voltage of ON/OFF Circuit	V_4	V_8	V
Sink of ON/OFF Circuit	I_3	1.5	mA
Input Voltage of Duty Limit Circuit	V_2	V_8	V
Input Voltage of Synchronous Circuit	V_{10}	−5 to V_8	V
External Oscillation Resistor	R_o	5 to ∞	kΩ
External Oscillation Capacitor	C_o	0 to 1	μF
Input Voltage of Error Amplifier	V_1	V_8	V
Reference Voltage	V_{14}	V_8	V
Drain of Error Amplifier	I_{13}	−2 to 0	mA
Input Voltage of Shut Down Circuit	V_{12}	V_8	V
Integration Voltage of Shut Down Circuit	V_6	V_8	V
Power Dissipation	P_D	150 (T_a = 75 °C)	mW
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

ELECTRICAL CHARACTERISTICS (T_a = 25°C)

CHARACTERISTICS	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Terminal Voltage	V_8	I_8 = 12 mA	6.1	6.6	7.1	V
Thermal Drift of V_8	$dV_{8(T_a)}$	Difference of MIN. and MAX. of V_8 in T_a from −20 °C to +75 °C			200	mV
Starting Supply Current (1)	$I_{8(1)}$	V_8 = 3 V, Pin 7 : Open		1.0	1.5	mA
Starting Supply Current (2)	$I_{8(2)}$	V_8 = 3 V, Pin 7 : Ground		3.0	4.2	mA
Starting Pulse Height	$P_{7(S)}$	V_8 = 3 V, Pin 7 : Open, Pin 6 : Ground	1.5	2.3	3.0	V_{p-p}
Starting Supply Terminal Voltage	$V_{8(S)}$	Pin 7 : Open, Pulse of Pin 7 = 1.5 V_{p-p}	2.0	2.6	3.0	V
Starting Oscillation Frequency	$f_{o(S)}$	V_8 = 3 V, Pin 10 : Open	10	13	20	kHz
Output Pulse Height	P_7	Pin 7 : Open, Pin 6 : Ground	5.0	6.0	7.1	V_{p-p}
Drain of Output Terminal	I_7	Pin 7 : Ground, $V_2 = V_8$	−6.3	−5.0	−3.7	mA
Saturation Voltage of Output Terminal	$V_{7(sat)}$	I_7 = 5 mA			0.3	V
Integration Terminal Current (1)	$I_{6(1)}$	I_5 = 100 μA	−700	−500	−300	μA
Integration Terminal Current (2)	$I_{6(2)}$	V_5 = 0.8 V	−700	−500	−300	μA
Leak of Integration Terminal	I_{6L}	V_5 = 0.3 V	−10		0	μA
Trigger Voltage of Shut Down Circuit	V_{6T}	P_7 < 100 mV_{p-p}	2.5		3.5	V
Drain of Duty Limit Terminal	I_2	V_2 = 3 V	−20		0	μA
Pulse Width set by Pin 2 Voltage	P_L	V = 2.33 V, frequency : 15.75 kHz, Low level period	25	30	35	μs
Thermal Drift of P_L	$dP_{L(T_a)}$	V_2 = 2.33 V, Difference of MIN. and MAX. of P_L in T_a from −20 °C to +75 °C			2	μs
ON Voltage of Pin 4	$V_{4(ON)}$	I_3 = 3 mA, V_3 = 0.3 V	1.5	2.5	3.5	V
ON Current of Pin 4	$I_{4(ON)}$	I_3 = 3 mA, V_3 = 0.3 V			200	μA
Output Saturation of ON/OFF Circuit	$V_{3(sat)}$	I_3 = 3 mA, V_4 = 3.5 V			300	mV
Leak of ON/OFF Output	I_{3L}	V_4 = 1.5 V, $V_3 = V_8$			1	μA
Offset Voltage of Error Amplifier	$V_{(OS)}$	Absolute Value		8	20	mV
Opened Gain of Error Amplifier	A_{VO}	f : 1 kHz, Signal of Pin 13 : 1 V_{p-p}	45	53	80	dB
Current of Pin 1	I_1	Pin 1 : Ground			−10	μA

CHARACTERISTICS	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Current of Pin 14	I_{14}	Pin 14 : Ground			−10	μA
Maximum Voltage of Error Amplifier Output	$V_{13(MAX.)}$	V_1 = 3.5 V, V_{14} = 3.0 V	5.0	5.7		V
Minimum Voltage of Error Amplifier Output	$V_{13(MIN.)}$	V_1 = 2.5 V, V_{14} = 3.0 V		50	300	mV
Sink of Error Amplifier Output	I_{13}	V_1 = 2.5 V, V_{14} = 3.0 V, V_{13} = 3.0 V	50	100	250	μA
Free Running Oscillation Amplitude	V_{fo}	Pin 10 : Open	V_{so}	3.3	4.0	V_{p-p}
Starting Oscillation Amplitude	$V_{fo(S)}$	V_8 = 3.0 V	0.5	1.5		V_{p-p}
Free Running Oscillation Frequency	f_o	Pin 10 : Open	12.3	13.3	14.3	kHz
Thermal Drift of f_o	$df_o(T_a)$	Pin 10 : Open, Difference of MIN. and MAX. of f_o in T_a from −20 °C to +75 °C			500	Hz
Synchronous Oscillation Amplitude	V_{so}	Synchronous Frequency : 15.75 kHz	2.7	3.0	3.3	V_{p-p}
Thermal Drift of V_{so}	$dV_{so}(T_a)$	Difference of MIN. and MAX. of V_{so} in T_a from −20 °C to +75 °C			150	mV
High level of Oscillation	V_{OH}			3.8	4.5	V
Starting V_{OH}	$V_{OH(S)}$	V_8 = 3.0 V	1.0	1.8		V
Thermal Drift of V_{OH}	$dV_{OH}(T_a)$	Difference of MIN. and MAX. of V_{OH} in T_a from −20 °C to +75 °C			100	mV
Synchronous Signal Voltage	V_s	Oscillation is synchronizing. (15.75 kHz)	−1.0		+0.3	V
Synchronous Signal Current	I_s	Oscillation is synchronizing. (15.75 kHz)	−200	−40		μA

CONNECTION DIAGRAM (Top View)



○#1 (Error Voltage Input)
This terminal is an inversion input of error amplifier. A feedback voltage of output is applied to this.

○#2 (Duty Limit)
This terminal is for setting maximum value of output transistor's on time. This value is decided by setting the ratio of the resistance value between terminal 2 and V_{CC} to one between terminal 2 and 3.
This terminal can also be used for soft-start function on applying the primary voltage.

○#3 (ON/OFF Output)

○#4 (ON/OFF Input)
These terminals are used for ON/OFF control of output, so that it is conviniently used for remote control of the power source of the set.
When terminal 3 is low level, the output is on and when it is high, the output is off. It can be directly driven for low active control signal, but for high active signal, it is convinient to use built-in ON/OFF circuit.

○#5 (Current Limit)
This terminal is used for protecting the control transistor from instantaneous overload. As input to this terminal, a waveform similar to emitter current of the output transistor, when operating the over current limiting function, terminal 7 is kept on a high level but a pulse is out again in the next period.

○#6 (Shut Down)
This terminal is used for shutting down the output when the overcurrent limiting function is operated. The voltage of this terminal is rising up gradually when operating the overcurrent limiting function and it rises up certain voltage (about 3 V), shut down function is operated.
If output shut down operation is unnecessary, terminal 6 is grounded.

○#7 (Pulse Output)
This is a Pulse output terminal for controling the output transistor. The low level is on timing of the controller. Therefore, when overcurrent limit and shut down circuit operate, output is pulled up to high level.

○#8 (Power Supply)
This is a power supply terminal, as a shunt regulator is built in, this terminal can be connected to the primary voltage through a resistance, the recommended range of input current is 10 to 15 mA.

○#9 (Ground)

○#10 (Synchronization)
This terminal is used for synchronizing the operation to external signal. Horizontal fly-back pulse can usually be used for this. When synchronization is not needed, terminal 10 is left open.

○#11 (Oscillation)

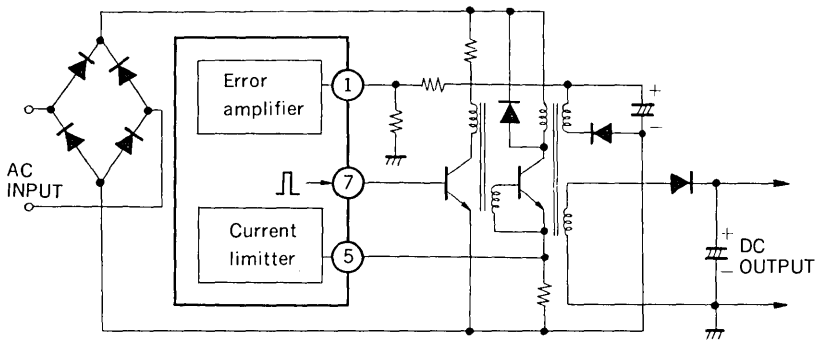
○#12 (Comparator Input)
Output of error amplifier is input to this terminal. The change of input voltage is converted to the change of pulse width and it controls the output pulse width of terminal 7.

○#13 (Error Amplifier Output)

○#14 (Reference Voltage Input)
This terminal is a non-inversion input of error amplifier. For reference voltage, it is suitable to divide a zener diode of about 6 V into two. It can be used to the voltage of terminal 8.

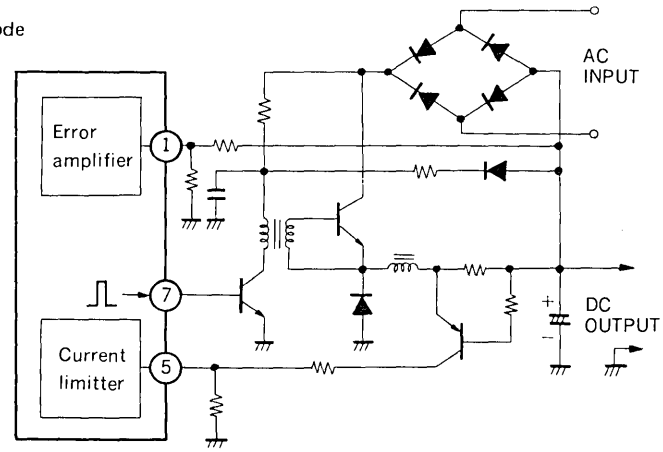
EXAMPLE OF APPLICATIONS

1. Isolated type

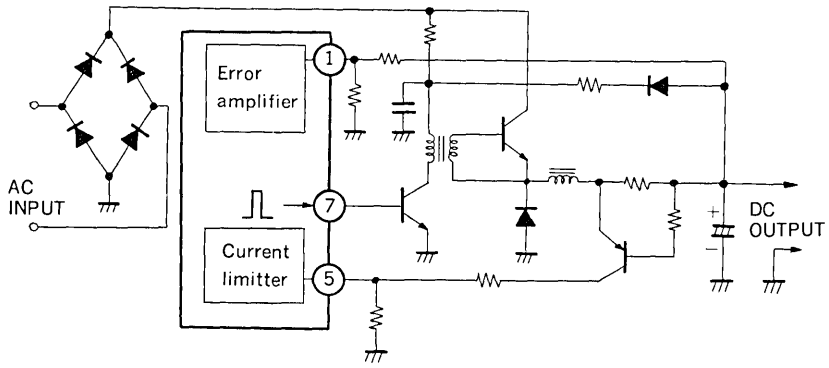


2. No isolated type

2–1 Inverting mode

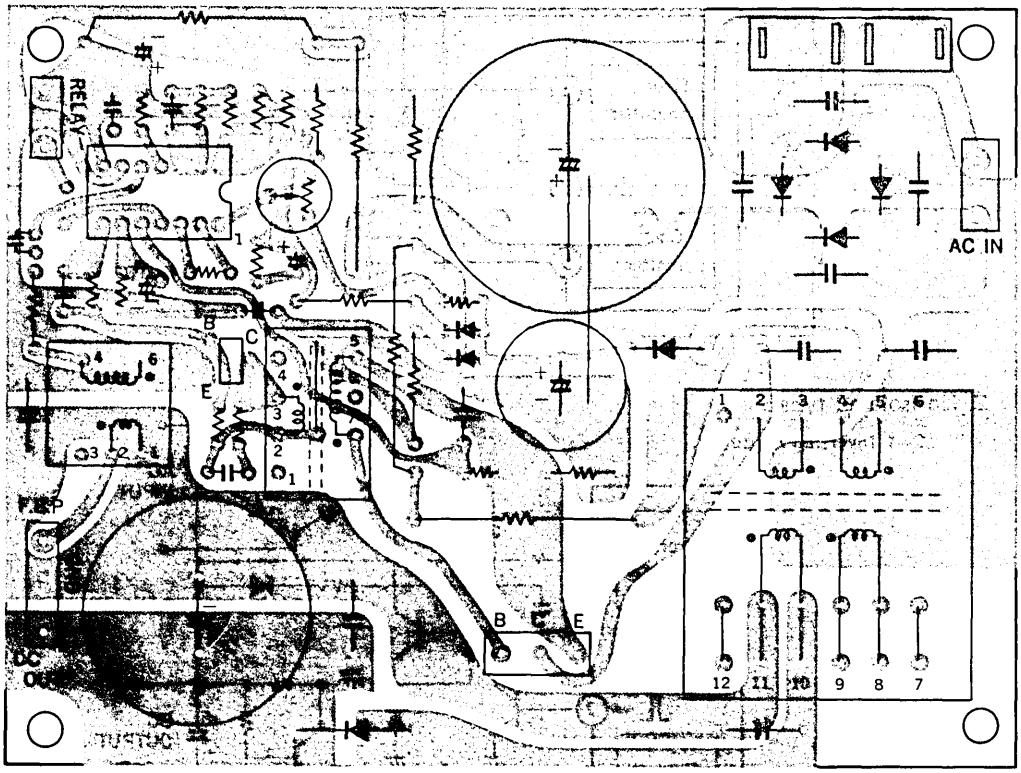


2–2 No inverting mode

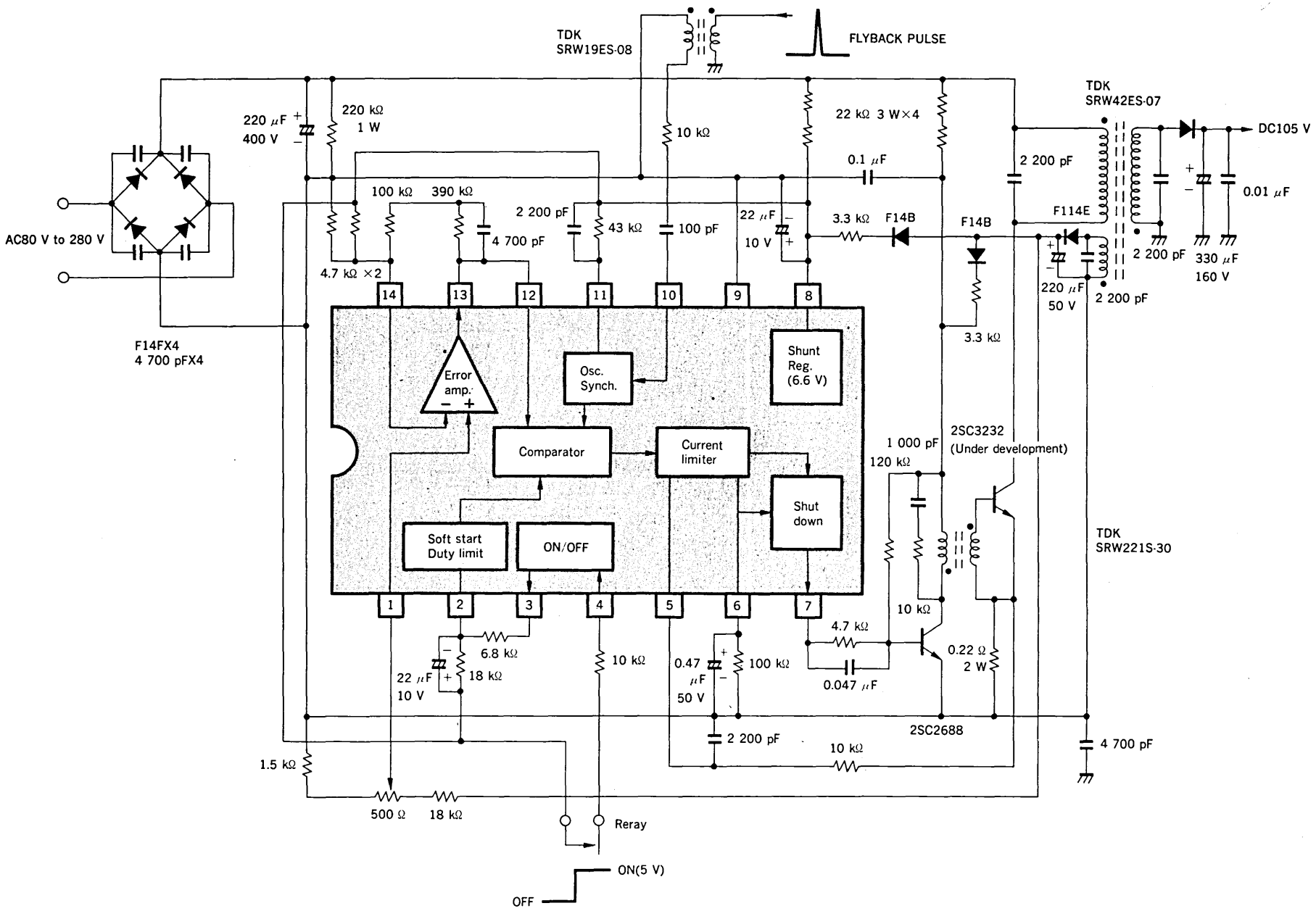


PATTERN OF PRINTED WIRING BOARD (Bottom View)

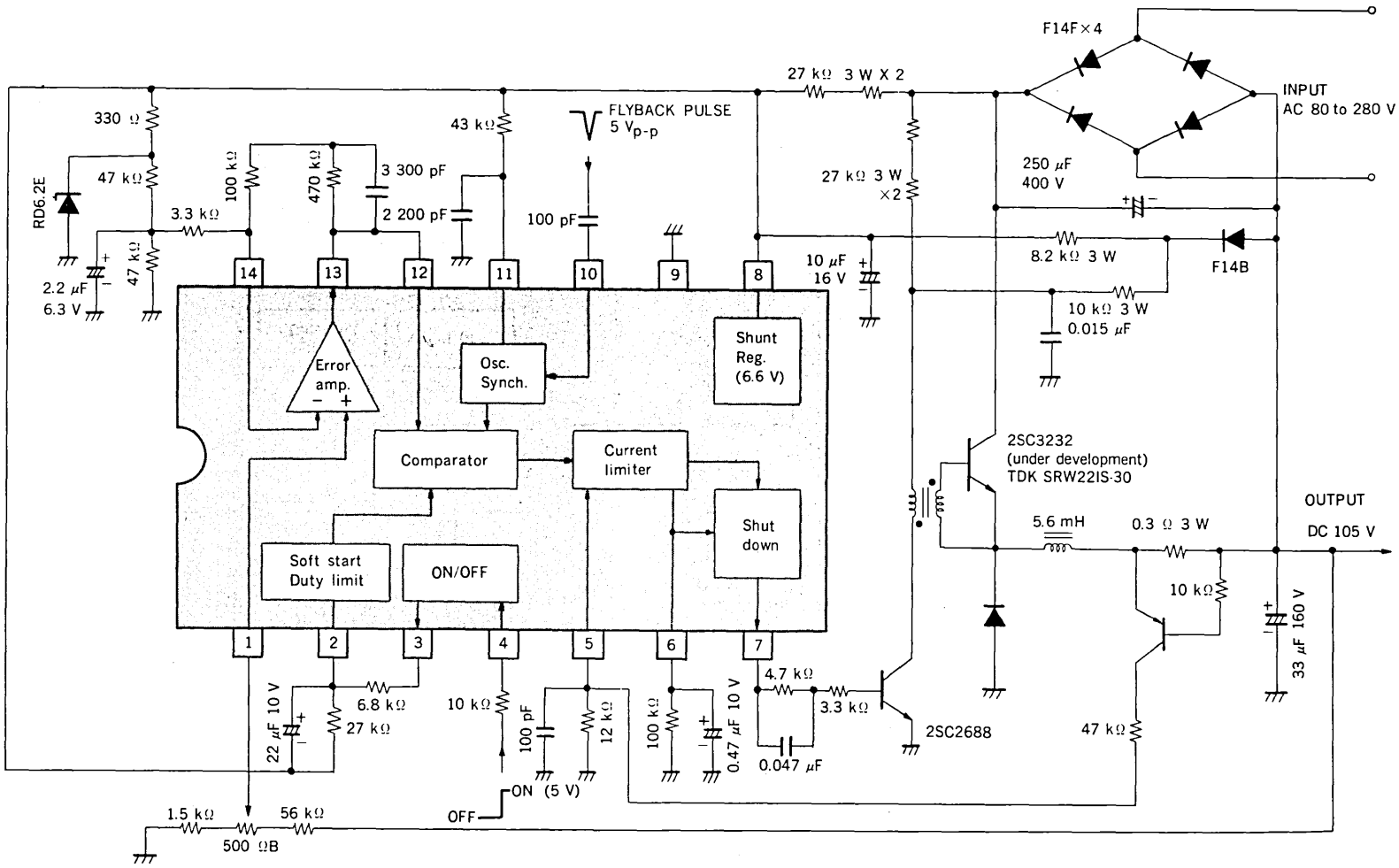
This printed wiring board is designed for the circuit of application 1



APPLICATION 1 (Isolated type)



APPLICATION 2 (No Isolated type)



BIPOLAR ANALOG INTEGRATED CIRCUITS

μPC78L00 SERIES

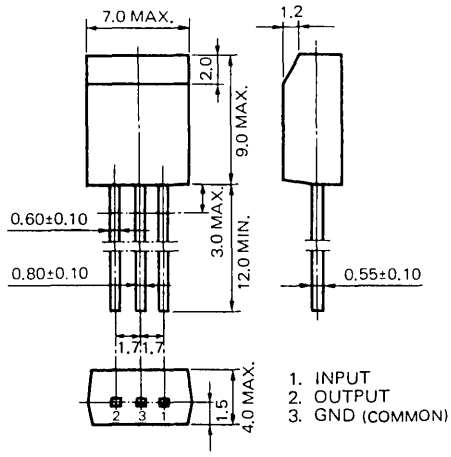
THREE TERMINAL POSITIVE VOLTAGE REGULATORS

The μPC78L00 series are monolithic three terminal positive regulators which employ internally current limiting, thermal shut down, make them essentially indestructible. They are intended as fixed-voltage regulators in a wide range of application includingl local on card regulation for elimination of distribution problems associated with single point regulation.

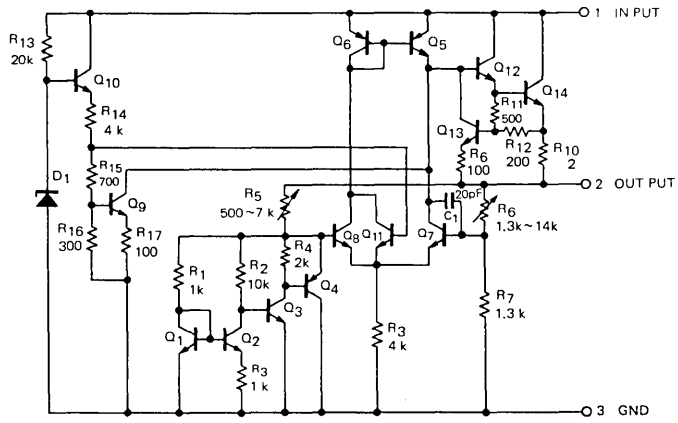
FEATURES

- Output current in excess of 100 mA
- No external component required
- Internal thermal overload protection
- Internal short circuit current limiting

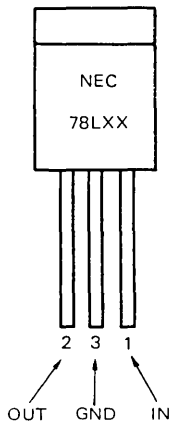
PACKAGE DIMENSIONS (Unit: mm)



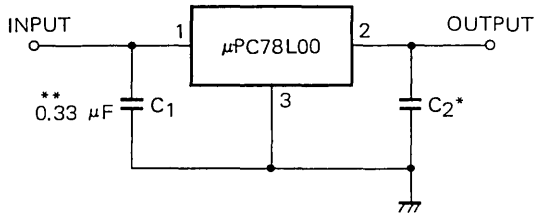
EQUIVALENT CIRCUIT



CONNECTION DIAGRAM



TYPICAL APPLICATION



Notes: * Although no output capacitor is needed for stability, it does improve transient response.
** Required if regulator is located an appreciable distance from power supply filter.

ABSOLUTE MAXIMUM RATINGS

Input Voltage	μPC78L05, 78L08	30	V
	μPC78L10, 78L12, 78L15	35	V
Internal Power Dissipation		800	mW
Operating Temperature Range		−20 to +80	°C
Storage Temperature Range		−55 to +150	°C
Lead Temperature		(Soldering 10 sec) 260	°C
Operating Junction Temperature Range		−20 to 150	°C

ELECTRICAL CHARACTERISTICS μPC78L05

(V_{IN}=10 V, I_{OUT}=40 mA, 0 °C≦T_j≦125 °C, C_{IN}=0.33 μF, C_{OUT}=0.1 μF)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Output Voltage	V_O	4.6	5.0	5.4	V	T_j=25 °C	
Line Regulation	REG_{IN}		55	200	mV	T_j=25 °C	7 V≦V_{IN}≦20 V
			45	150	mV		8 V≦V_{IN}≦20 V
Load Regulation	REG_L		11	60	mV	T_j=25 °C	1 mA≦I_{OUT}≦100 mA
			5.0	30	mV		1 mA≦I_{OUT}≦40 mA
Output Voltage	V_O	4.5		5.5	V	7 V≦V_{IN}≦20 V, 1 mA≦I_{OUT}≦40 mA	
		4.5		5.5	V	V_{IN}=10 V, 1 mA≦I_{OUT}≦70 mA	
Quiescent Current	I_{BIAS}		3.8	6.0	mA	T_j=25 °C	
				5.5	mA	T_j=125 °C	
Quiescent Current Change	ΔI_{BIAS}			1.5	mA	8 V≦V_{IN}≦20 V, I_{OUT}=40 mA	
				0.2	mA	V_{IN}=10 V, 1 mA≦I_{OUT}≦40 mA	
Output Noise Voltage	NL		30		μV	Ta=25 °C, 10 Hz≦f≦100 kHz	
Ripple Rejection		40	50		dB	f=120 Hz, 8 V≦V_{IN}≦18 V, T_j=25 °C	
Temperature Coefficient of Output Voltage	$V_O/\Delta T$		−0.65		mV/°C	I_{OUT}=5 mA	
Dropout Voltage			1.7		V	T_j=25 °C	
Short Circuit Current	I_{oshort}		150		mA	T_j=25 °C	

ELECTRICAL CHARACTERISTICS μPC78L08

(V_{IN}=14 V, I_{OUT}=40 mA, 0 °C≦T_j≦125 °C, C_{IN}=0.33 μF, C_{OUT}=0.1 μF)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Voltage	V_O	7.36	8.0	8.64	V	T_j=25 °C
Line Regulation	REG_{IN}		80	200	mV	T_j=25 °C, 10.5 V≦V_{IN}≦23 V
			70	150	mV	T_j=25 °C, 11 V≦V_{IN}≦23 V
Load Regulation	REG_L		15	80	mV	T_j=25 °C, 1 mA≦I_{OUT}≦100 mA
			8.0	40	mV	T_j=25 °C, 1 mA≦I_{OUT}≦40 mA
Output Voltage	V_O	7.2		8.8	V	10.5V≦V_{IN}≦23 V, 1 mA≦I_{OUT}≦40 mA
		7.2		8.8	V	V_{IN}=14 V, 1 mA≦I_{OUT}≦70 mA
Quiescent Current	I_{BIAS}		3.9	6.0	mA	T_j=25 °C
				5.5	mA	T_j=125 °C
Quiescent Current Change	ΔI_{BIAS}			1.5	mA	12 V≦V_{IN}≦23 V, I_{OUT}=40 mA
				0.2	mA	V_{IN}=14 V, 1 mA≦I_{OUT}≦40 mA
Output Noise Voltage	NL		60		μV	T_a=25 °C, 10 Hz≦ f≦100 kHz
Ripple Rejection		38	45		dB	f=120 Hz, 12 V≦V_{IN}≦22 V, T_j=25 °C
Temperature Coefficient of Output Voltage	$V_O/\Delta T$		−0.8		mV/°C	I_{OUT}=5 mA
Dropout Voltage			1.7		V	T_j=25 °C
Short Circuit Current	$I_{O\ short}$		150		mA	T_j=25 °C

ELECTRICAL CHARACTERISTICS μPC78L10

(V_{IN}=17 V, I_{OUT}=40 mA, 0 °C≦T_j≦125 °C, C_{IN}=0.33 μF, C_{OUT}=0.1 μF)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Voltage	V_O	9.2	10	10.8	V	T_j=25 °C
Line Regulation	REG_{IN}		100	230		T_j=25 °C, 12.5 V≦V_{IN}≦25 V
			80	170	mV	T_j=25 °C, 13 V≦V_{IN}≦25 V
Load Regulation	REG_L		18	90	mV	T_j=25 °C, 1 mA≦I_{OUT}≦100 mA
			9	45	mV	T_j=25 °C, 1 mA≦I_{OUT}≦40 mA
Output Voltage	V_O	9.0		11.0	V	12.5 V≦V_{IN}≦25 V, 1 mA≦I_{OUT}≦40 mA
		9.0		11.0	V	V_{IN}=17 V, 1 mA≦I_{OUT}≦70 mA
Quiescent Current	I_{BIAS}		4.0	6.0	mA	T_j=25 °C
				5.5	mA	T_j=125 °C
Quiescent Current Change	ΔI_{BIAS}			1.5	mA	13 V≦V_{IN}≦25 V, I_{OUT}=40 mA
				0.2	mA	V_{IN}=17 V, 1 mA≦I_{OUT}≦40 mA
Output Noise Voltage	NL		70		μV	T_a=25 °C, 10 Hz ≦f≦100 kHz
Ripple Rejection		37	44		dB	f=120 Hz, 14 V≦V_{IN}≦24 V, T_j=25 °C
Temperature Coefficient of Output Voltage	$V_O/\Delta T$		−0.9		mV/°C	I_{OUT}=5 mA
Dropout Voltage			1.7		V	T_j=25 °C
Short Circuit Current	$I_{O\ short}$		150		mA	T_j=25 °C

ELECTRICAL CHARACTERISTICS μPC78L12

(V_{IN}=19 V, I_{OUT}=40 mA, 0 °C≦T_j≦125 °C, C_{IN}=0.33 μF, C_{OUT}=0.1 μF)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Output Voltage	V_O	11.1	12	12.9	V	T_j=25 °C	
Line Regulation	REG_{IN}		120	250	mV	T_j=25 °C	14.5 V≦V_{IN}≦27 V
			100	200	mV		16 V≦V_{IN}≦27 V
Load Regulation	REG_L		20	100	mV	T_j=25 °C	1 mA≦I_{OUT}≦100 mA
			10	50	mV		1 mA≦I_{OUT}≦40 mA
Output Voltage	V_O	10.8		13.2	V	14.5 V≦V_{IN}≦27 V, 1 mA≦I_{OUT}≦40 mA	
		10.8		13.2	V	V_{IN}=19V, 1 mA≦I_{OUT}≦70 mA	
Quiescent Current	I_{BIAS}		4.2	6.5	mA	T_j=25 °C	
				6.0	mA	T_j=125 °C	
Quiescent Current Change	ΔI_{BIAS}			1.5	mA	16 V≦V_{IN}≦27 V, I_{OUT}=40 mA	
				0.2	mA	V_{IN}=19 V, 1 mA≦I_{OUT}≦40 mA	
Output Noise Voltage	NL		80		μV	T_a=25 °C, 10 Hz ≦f≦100 kHz	
Ripple Rejection		36	42		dB	f=120 Hz, 15 V≦V_{IN}≦25 V, T_j=25 °C	
Temperature Coefficient of Output Voltage	$V_O/\Delta T$		−1.0		mV/° C	I_{OUT}=5 mA	
Dropout Voltage			1.7		V	T_j=25 °C	
Short Circuit Current	$I_{O\ short}$		150		mA	T_j=25 °C	

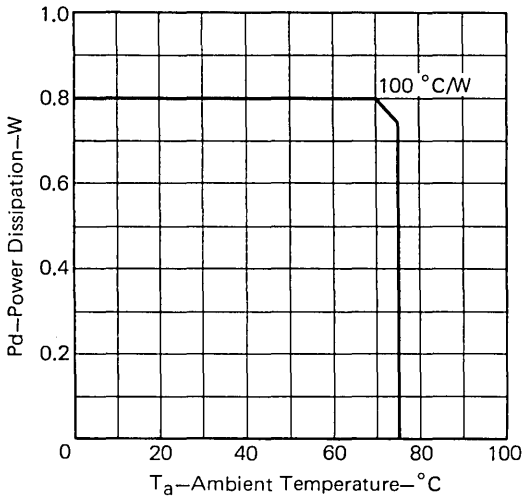
ELECTRICAL CHARACTERISTICS μPC78L15

(V_{IN}=23 V, I_{OUT}=40 mA, 0 °C≦T_j≦125 °C, C_{IN}=0.33 μF, C_{OUT}=0.1 μF)

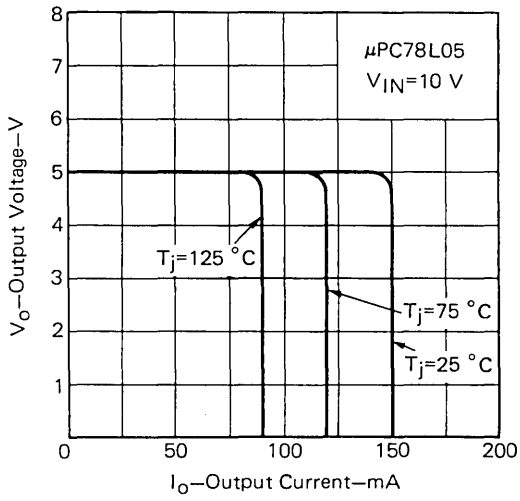
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Output Voltage	V_O	13.8	15	16.2	V	T_j=25 °C	
Line Regulation	REG_{IN}		130	300	mV	T_j=25 °C	17.5 V≦V_{IN}≦30 V
			110	250	mV		20 V≦V_{IN}≦30 V
Load Regulation	REG_L		25	150	mV	T_j=25 °C	1 mA≦I_{OUT}≦100 mA
			12	75	mV		1 mA≦I_{OUT}≦40 mA
Output Voltage	V_O	13.5		16.5	V	17.5 V≦V_{IN}≦30 V, 1 mA≦I_{OUT}≦40 mA	
		13.5		16.5	V	V_{IN}=23 V, 1 mA≦I_{OUT}≦70 mA	
Quiescent Current	I_{BIAS}		4.4	6.5	mA	T_j=25 °C	
				6.0	mA	T_j=125 °C	
Quiescent Current Change	ΔI_{BIAS}			1.5	mA	20 V≦V_{IN}≦30 V, I_{OUT}=40 mA	
				0.2	mA	V_{IN}=23 V, 1 mA≦I_{OUT}≦40 mA	
Output Noise Voltage	NL		90		μV	T_a=25 °C, 10 Hz≦f ≦100 kHz	
Ripple Rejection		33	39		dB	f=120 Hz, 18.5 V≦V_{IN}≦28.5 V, T_j=25 °C	
Temperature Coefficient of Output Voltage	$V_O/\Delta T$		−1.3		mV/° C	I_{OUT}=5 mA	
Dropout Voltage			1.7		V	T_j=25 °C	
Short Circuit Current	$I_{O\ short}$		150		mA	T_j=25 °C	

TYPICAL CHARACTERISTICS (T_a=25 °C)

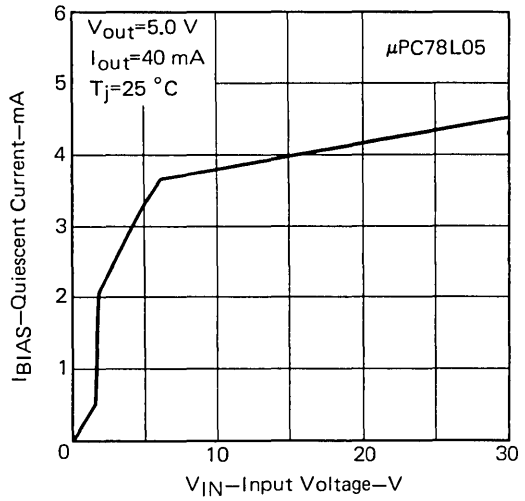
WORST CASE POWER DISSIPATION vs. AMBIENT TEMPERATURE



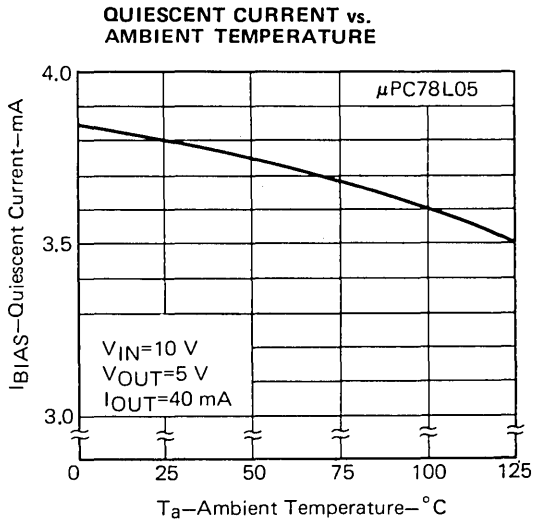
CURRENT LIMITING CHARACTERISTICS



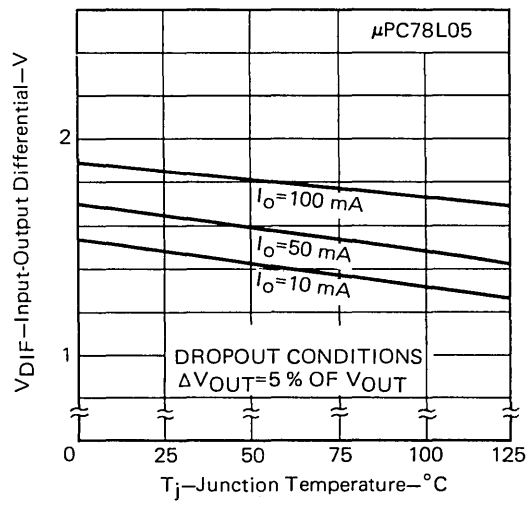
QUIESCENT CURRENT vs. INPUT VOLTAGE



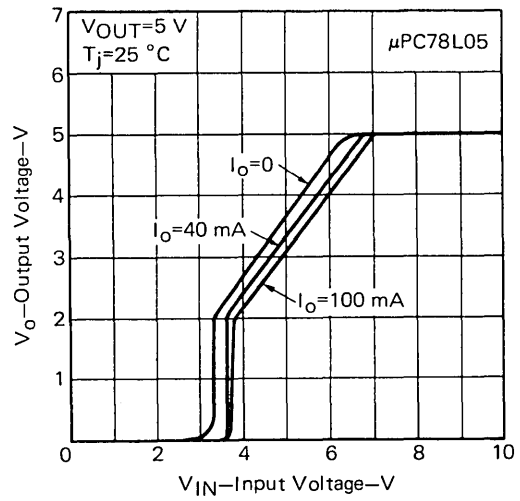
QUIESCENT CURRENT vs. AMBIENT TEMPERATURE



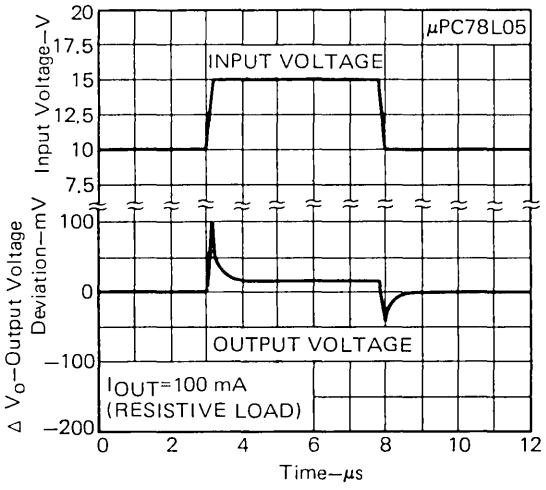
DROPOUT VOLTAGE vs. JUNCTION TEMPERATURE



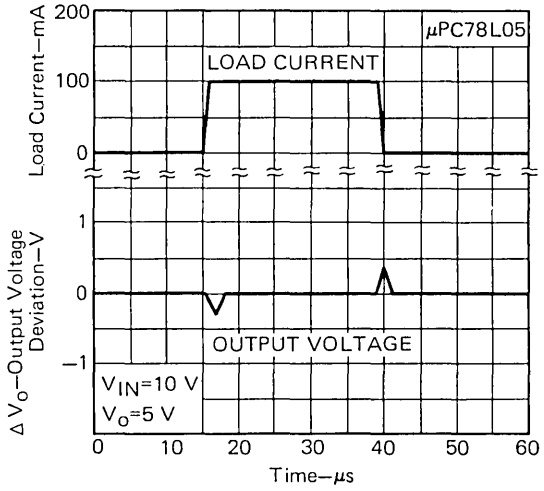
DROPOUT CHARACTERISTICS



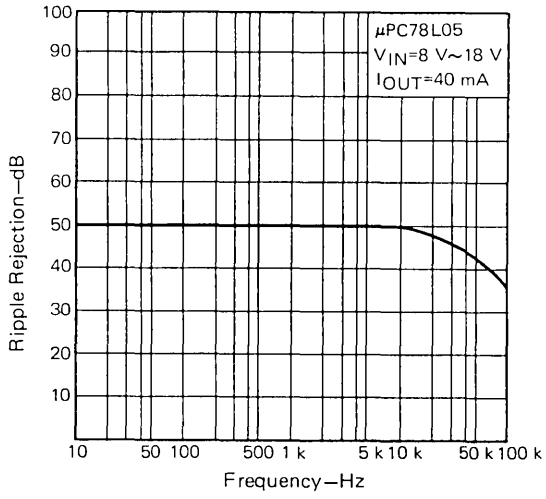
LINE TRANSIENT RESPONSE



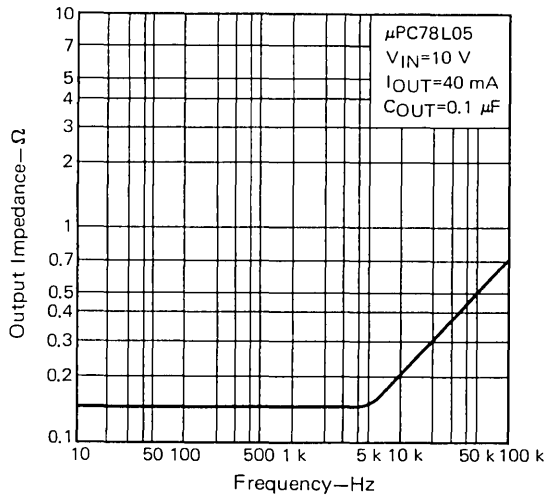
LOAD TRANSIENT RESPONSE



RIPPLE REJECTION vs. FREQUENCY



OUTPUT IMPEDANCE vs. FREQUENCY



BIPOLAR ANALOG INTEGRATED CIRCUITS

μPC78M00H SERIES

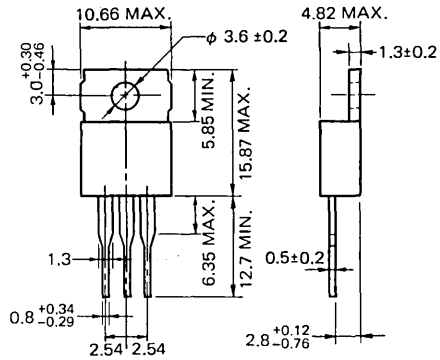
THREE TERMINAL POSITIVE VOLTAGE REGULATORS

The μPC78M00H series are monolithic three terminal positive regulators which employ internally current limiting, thermal shut down, and safe-area compensation, make them essentially indestructible. They are intended as fixed-voltage regulators in a wide range of application including local on card regulation for elimination of distribution problems associated with single point regulation.

FEATURES

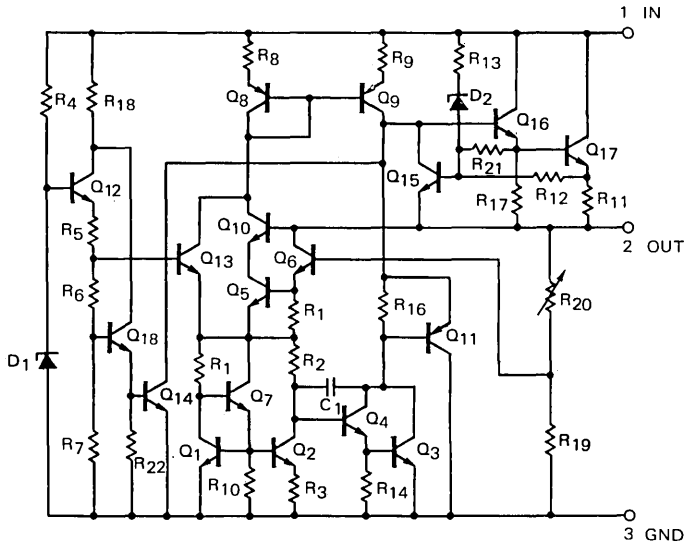
- Output current in excess of 0.5 A
- No external component required
- Internal thermal overload protection
- Internal short circuit current limiting

PACKAGE DIMENSIONS (Unit: mm)

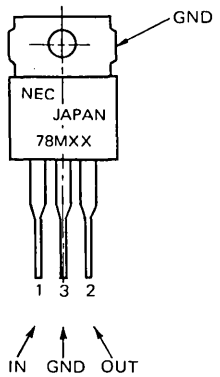


JEDEC : TO–220AB
IEC : –

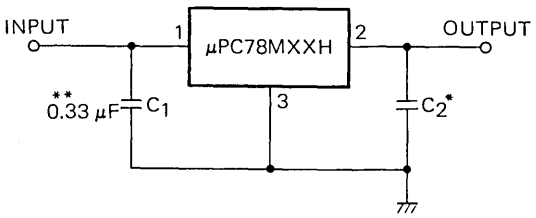
EQUIVALENT CIRCUIT



CONNECTION DIAGRAM



TYPICAL APPLICATION



Notes: * Although no output capacitor is needed for stability, it does improve transient response.
** Required if regulator is located an appreciable distance from power supply filter.

ABSOLUTE MAXIMUM RATINGS

Input Voltage	μPC78M05H/08H/10H/12H/15H/18H	35	V
	μPC78M24H	40	V
Internal Power Dissipation		Internally Limited	
Operating Temperature Range		−20 to +80	°C
Storage Temperature Range		−55 to +150	°C
Lead Temperature		Soldering 10 sec 230	°C
Operating Junction Temperature Rang		0 to 125	°C (Continuous)
Operating Junction Temperature Rang		0 to 200	°C (short term, 30 min. MAX.)

ELECTRICAL CHARACTERISTICS μPC78M05H (V_{IN}=10 V, I_O=350 mA, 0 °C ≦ Tj ≦ 125 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Voltage	V_O	4.8	5.0	5.2	V	Tj=25 °C
		4.75		5.25		7 V≦V_{IN}≦20 V, 5 mA≦I_O≦350 mA
Line Regulation	REG_{IN}		3	100	mV	Tj=25 °C, 7 V≦V_{IN}≦25 V, I_O=200 mA
			1	50		Tj=25 °C, 8 V≦V_{IN}≦25 V, I_O=200 mA
Load Regulation	REG_L		20	100	mV	Tj=25 °C, 5 mA≦I_O≦500 mA
			10	50		Tj=25 °C, 5 mA≦I_O≦200 mA
Quiescent Current	I_{BIAS}		4.5	6.0	mA	Tj=25 °C
Quiescent Current Change	ΔI_{BIAS}			0.8	mA	8 V≦V_{IN}≦25 V, I_O=200 mA
				0.5		5 mA≦I_O≦350 mA
Output Noise Voltage	N_L		40		μV	Ta=25 °C, 10 Hz≦f≦100 kHz
Ripple Rejection		62	80		dB	Tj=25 °C, f=120 Hz, 8 V≦V_{IN}≦18 V, I_O=300 mA
Dropout Voltage			2.0		V	Ta=25 °C
Short Circuit Current	I_{oshort}		250		mA	Tj=25 °C, V_{IN}=35 V
Peak Output Current	I_{opeak}		1.0		A	Tj=25 °C
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$		−1.0		mV/°C	I_O=5 mA

ELECTRICAL CHARACTERISTICS μPC78M08H (V_{IN}=14 V, I_O=350 mA, 0 °C ≦ Tj ≦ 125 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Voltage	Vo	7.7	8.0	8.3	V	Tj=25 °C
		7.6		8.4		10.5 V≦V_{IN}≦23 V, 5 mA≦I_O≦350 mA
Line Regulation	REG_{IN}		6.0	100	mV	Tj=25 °C, 10.5 V≦V_{IN}≦25 V, I_O=200 mA
			2.0	50		Tj=25 °C, 11 V≦V_{IN}≦25 V, I_O=200 mA
Load Regulation	REG_L		25	160	mV	Tj=25 °C, 5 mA≦I_O≦500 mA
			10	80		Tj=25 °C, 5 mA≦I_O≦200 mA
Quiescent Current	I_{BIAS}		4.6	6.0	mA	Tj=25 °C
Quiescent Current Change	ΔI_{BIAS}			0.8	mA	10.5 V≦V_{IN}≦25 V, I_O=200 mA
				0.5		5 mA≦I_O≦350 mA
Output Noise Voltage	N_L		52		μV	Ta=25 °C, 10 Hz≦f≦100 kHz
Ripple Rejection		56	80		dB	Tj=25 °C, f=120 Hz, 11.5 V≦V_{IN}≦21.5 V I_O=300 mA
Dropout Voltage			2.0		V	Ta=25 °C
Short Circuit Current	I_{oshort}		250		mA	Tj=25 °C, V_{IN}=35 V
Peak Output Current	I_{opeak}		1.0		A	Tj=25 °C
Temperature Coefficient of Output Voltage	ΔVo/ΔT		−1.0		mV/°C	I_O=5 mA

ELECTRICAL CHARACTERISTICS μPC78M10H (V_{IN}=17 V, I_O=350 mA, 0 °C≦ Tj≦125 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Voltage	Vo	9.6	10	10.4	V	Tj=25 °C
		9.5		10.5		12.5 V≦V_{IN}≦25 V, 5 mA≦I_O≦350 mA
Line Regulation	REG_{IN}		7.0	100	mV	Tj=25 °C, 12.5 V≦V_{IN}≦28 V, I_O=200 mA
			2.0	50		Tj=25 °C, 14 V≦V_{IN}≦28 V, I_O=200 mA
Load Regulation	REG_L		25	200	mV	Tj=25 °C, 5 mA≦I_O≦500 mA
			10	100		Tj=25 °C, 5 mA≦I_O≦200 mA
Quiescent Current	I_{BIAS}		4.5	6.0	mA	Tj=25 °C
Quiescent Current Change	ΔI_{BIAS}			0.8	mA	12.5 V≦V_{IN}≦28 V, I_O=200 mA
				0.5		5 mA≦I_O≦350 mA
Output Noise Voltage	N_L		70		μV	Ta=25 °C, 10 Hz≦f≦100 kHz
Ripple Rejection		55	80		dB	Tj=25 °C, f=120 Hz, 13 V≦V_{IN}≦23 V, I_O=300 mA
Dropout Voltage			2.0		V	Ta=25 °C
Short Circuit Current	I_{oshort}		250		mA	Tj=25 °C, V_{IN}=35 V
Peak Output Current	I_{opeak}		1.0		A	Tj=25 °C
Temperature Coefficient of Output Voltage	ΔVo/ΔT		−1.0		mV/°C	I_O=5 mA

ELECTRICAL CHARACTERISTICS μPC78M12H (V_{IN}=19 V, I_O=350 mA, 0 °C ≦ Tj ≦ 125 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Voltage	Vo	11.5	12.0	12.5	V	Tj=25 °C
		11.4		12.6		14.5 V≦V_{IN}≦27 V, 5 mA≦I_O≦350 mA
Line Regulation	REG_{IN}		8.0	100	mV	Tj=25 °C, 14.5 V≦V_{IN}≦30 V, I_O=200 mA
			2.0	50		Tj=25 °C, 16 V≦V_{IN}≦30 V, I_O=200 mA
Load Regulation	REG_L		25	240	mV	Tj=25 °C, 5 mA≦I_O≦500 mA
			10	120		Tj=25 °C, 5 mA≦I_O≦200 mA
Quiescent Current	I_{BIAS}		4.8	6.0	mA	Tj=25 °C
Quiescent Current Change	ΔI_{BIAS}			0.8	mA	14.5 V≦V_{IN}≦30 V, I_O=200 mA
				0.5		5 mA≦I_O≦350 mA
Output Noise Voltage	N_L		75		μV	Ta=25 °C, 10 Hz≦f≦100 kHz
Ripple Rejection		55	80		dB	Tj=25 °C, f=120 Hz, 15 V≦V_{IN}≦25 V Io=300 mA
Dropout Voltage			2.0		V	Ta=25 °C
Short Circuit Current	I_{oshort}		250		mA	Tj=25 °C, V_{IN}=35 V
Peak Output Current	I_{opeak}		1.0		A	Tj=25 °C
Temperature Coefficient of Output Voltage	ΔVo/ΔT		−1.0		mV/°C	Io=5 mA

ELECTRICAL CHARACTERISTICS μPC78M15H (V_{IN}=23 V, I_O=350 mA, 0 °C ≦ Tj ≦ 125 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Voltage	Vo	14.4	15	15.6	V	Tj=25 °C
		14.25		15.75		17.5 V≦V_{IN}≦30 V, 5 mA≦I_O≦350 mA
Line Regulation	REG_{IN}		10	100	mV	Tj=25 °C, 17.5 V≦V_{IN}≦30 V, I_O=200 mA
			3.0	50		Tj=25 °C, 20 V≦V_{IN}≦30 V, I_O=200 mA
Load Regulation	REG_L		25	300	mV	Tj=25 °C, 5 mA≦I_O≦500 mA
			10	150		Tj=25 °C, 5 mA≦I_O<200 mA
Quiescent Current	I_{BIAS}		4.8	6.0	mA	Tj=25 °C
Quiescent Current Change	ΔI_{BIAS}			0.8	mA	17.5 V≦V_{IN}≦30 V, I_O=200 mA
				0.5		5 mA≦I_O≦350 mA
Output Noise Voltage	N_L		90		μV	Ta=25 °C, 10 Hz≦f≦100 kHz
Ripple Rejection		54	70		dB	Tj=25 °C, f=120 Hz, 18.5 V≦V_{IN}≦28.5 V I_O=300 mA
Dropout Voltage			2.0		V	Ta=25 °C
Short Circuit Current	I_{oshort}		250		mA	Tj=25 °C, V_{IN}=35 V
Peak Output Current	I_{opeak}		1.0		A	Tj=25 °C
Temperature Coefficient of Output Voltage	ΔVo/ΔT		−1.0		mV/°C	I_O=5 mA

ELECTRICAL CHARACTERISTICS μPC78M18H (V_{IN}=27 V, I_O=350 mA, 0 °C ≦ Tj ≦ 125 °C)

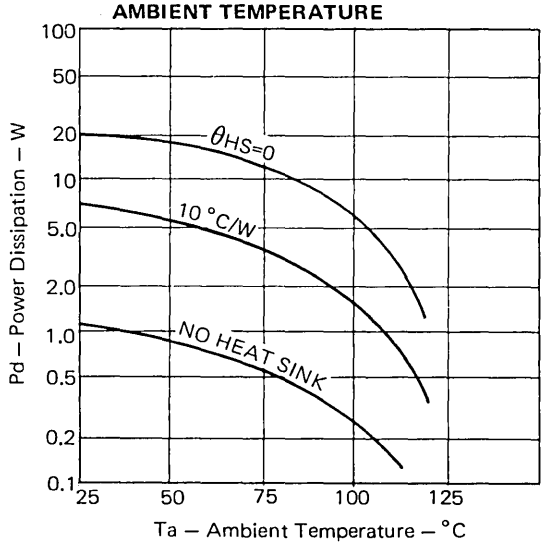
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Voltage	Vo	17.3	18.0	18.7	V	Tj=25 °C
		17.1		18.9		21 V≦V_{IN}≦33 V, 5 mA≦I_O≦350 mA
Line Regulation	REG_{IN}		10	100	mV	Tj=25 °C, 21 V≦V_{IN}≦33 V, I_O=200 mA
			4.0	50		Tj=25 °C, 24 V≦V_{IN}≦30 V, I_O=200 mA
Load Regulation	REG_L		30	360	mV	Tj=25 °C, 5 mA≦I_O≦500 mA
			10	180		Tj=25 °C, 5 mA≦I_O≦200 mA
Quiescent Current	I_{BIAS}		4.8	6.0	mA	Tj=25 °C
Quiescent Current Change	ΔI_{BIAS}			0.8	mA	27 V≦V_{IN}≦38 V, I_O=200 mA
				0.5		5 mA≦I_O≦350 mA
Output Noise Voltage	N_L		100		μV	Ta=25 °C, 10 Hz≦f≦100 kHz
Ripple Rejection		53	70		dB	Tj=25 °C, f=120 Hz, 22 V≦V_{IN}≦32 V I_O=300 mA
Dropout Voltage			2.0		V	Ta=25 °C
Short Circuit Current	I_{oshort}		250		mA	Tj=25 °C V_{IN}=35 V
Peak Output Current	I_{opeak}		1.0		A	Tj=25 °C
Temperature Coefficient of Output Voltage	ΔVo/ΔT		−1.0		mV/°C	I_O=5 mA

ELECTRICAL CHARACTERISTICS μPC78M24H (V_{IN}=33 V, I_O=350 mA, 0 °C ≦ Tj ≦ 125 °C)

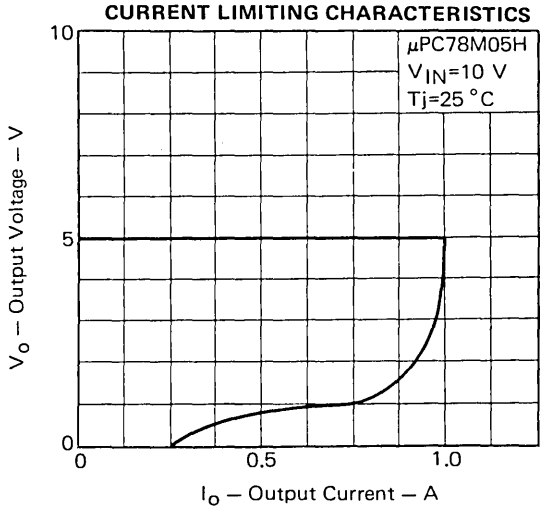
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Voltage	Vo	23	24	25	V	Tj=25 °C
		22.8		25.2		27 V≦V_{IN}≦38 V, 5 mA≦I_O≦350 mA
Line Regulation	REG_{IN}		10	100	mV	Tj=25 °C, 27 V≦V_{IN}≦38 V, I_O=200 mA
			5.0	50		Tj=25 °C, 28 V≦V_{IN}≦38 V, I_O=200 mA
Load Regulation	REG_L		30	480	mV	Tj=25 °C, 5 mA≦I_O≦500 mA
			10	240		Tj=25 °C, 5 mA≦I_O≦200 mA
Quiescent Current	I_{BIAS}		5.0	6.0	mA	Tj=25 °C
Quiescent Current Change	ΔI_{BIAS}			0.8	mA	27 V≦V_{IN}≦38 V, I_O=200 mA
				0.5		5 mA≦I_O≦350 mA
Output Noise Voltage	N_L		170		μV	Ta=25 °C, 10 Hz≦f≦100 kHz
Ripple Rejection		50	70		dB	Tj=25 °C, f=120 Hz, 28 V≦V_{IN}≦38 V I_O=300 mA
Dropout Voltage			2.0		V	Ta=25 °C
Short Circuit Current	I_{oshort}		250		mA	Tj=25 °C, V_{IN}=35 V
Peak Output Current	I_{opeak}		1.0		A	Tj=25 °C
Temperature Coefficient of Output Voltage	ΔVo/ΔT		−1.2		mV/°C	I_O=5 mA, 0 °C≦Tj≦125 °C

TYPICAL CHARACTERISTICS (Ta=25 °C)

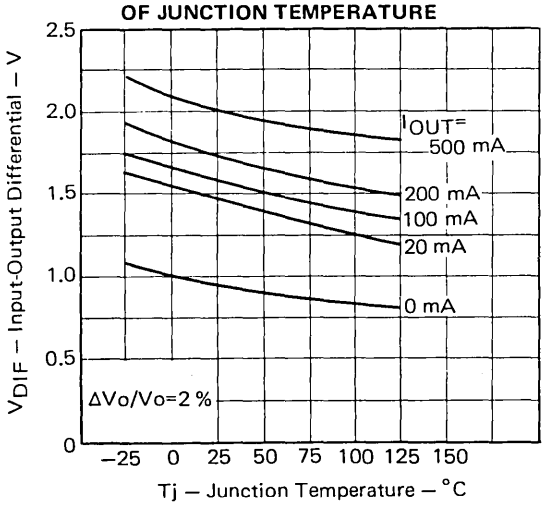
WORST CASE POWER DISSIPATION vs. AMBIENT TEMPERATURE



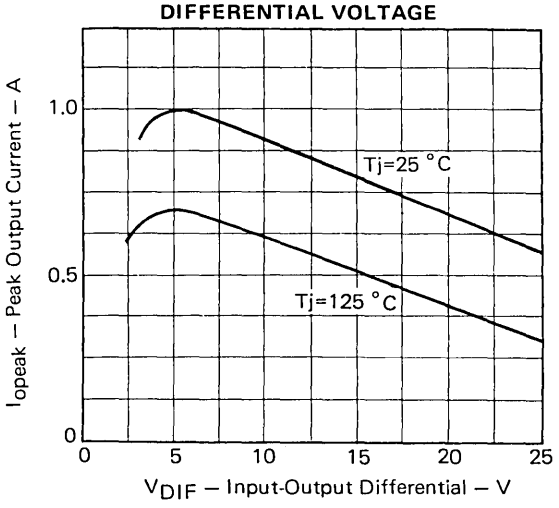
CURRENT LIMITING CHARACTERISTICS



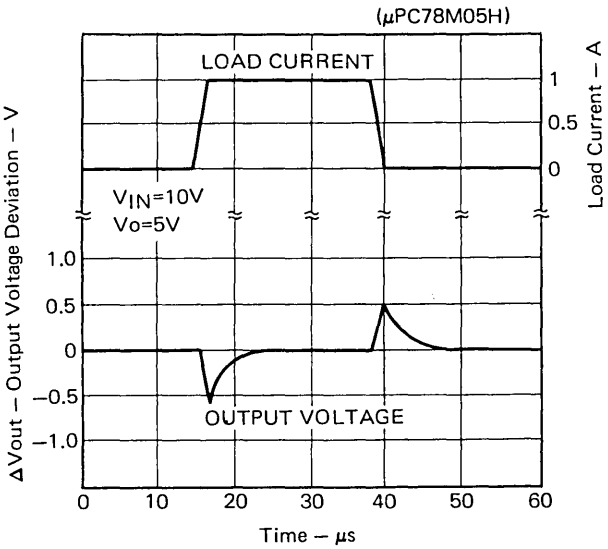
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



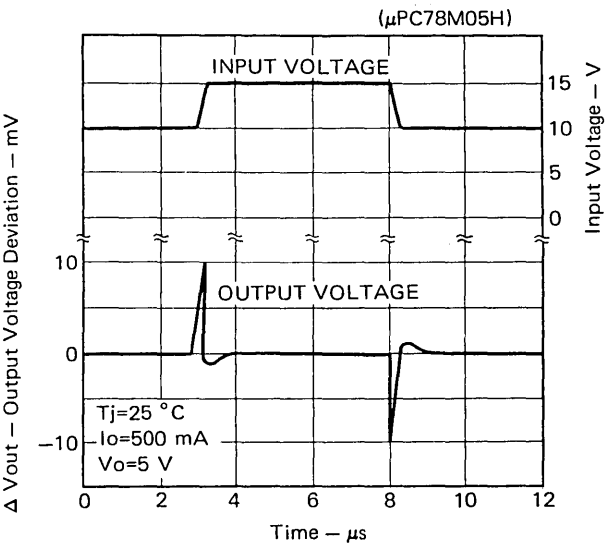
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT/OUTPUT DIFFERENTIAL VOLTAGE



LOAD TRANSIENT RESPONSE (μPC78M05H)



LINE TRANSIENT RESPONSE (μPC78M05H)



BIPOLAR ANALOG INTEGRATED CIRCUITS

μPC7800H SERIES

THREE TERMINAL POSITIVE VOLTAGE REGULATORS

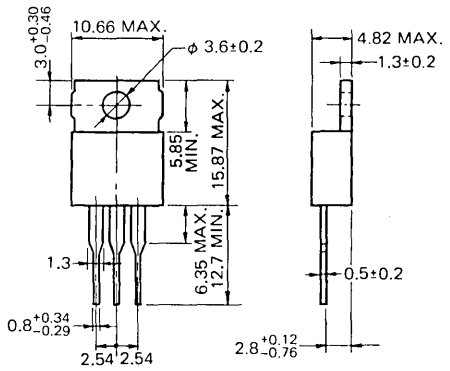
The μPC7800H series are monolithic three terminal positive regulators which employ internally current limiting, thermal shut down, and safe-area compensation, make them essentially indestructible. They are intended as fixed-voltage regulators in a wide range of application including local on card regulation for elimination of distribution problems associated with single point regulation.

FEATURES

- Output current in excess of 1 A
- No external component required
- Internal thermal overload protection
- Internal short circuit current limiting
- Low output resistance 17 mΩ

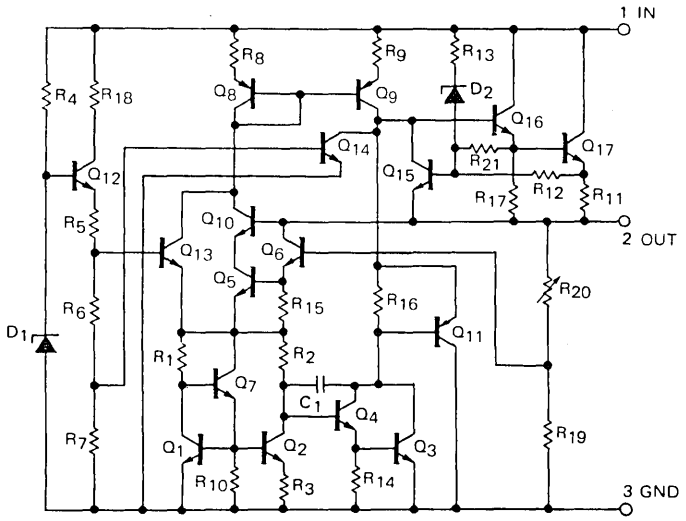
PACKAGE DIMENSIONS (Unit: mm)

Typical values unless specified

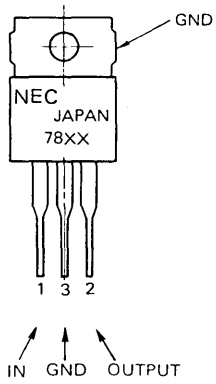


JEDEC : TO–220AB
IEC : –

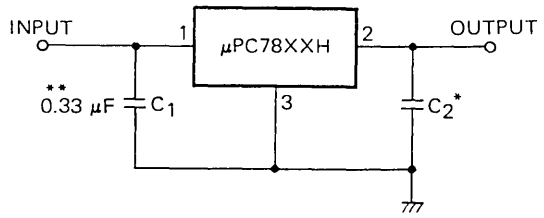
EQUIVALENT CIRCUIT



CONNECTION DIAGRAM



TYPICAL APPLICATION



Notes: * Although no output capacitor is needed for stability, it does improve transient response.
** Required if regulator is located an appreciable distance from power supply filter.

ABSOLUTE MAXIMUM RATINGS

Input Voltage	(5 V through 18 V) 35	V
	(24 V) 40	V
Internal Power Dissipation	Internally Limited	
Operating Temperature Range	−20 to +80	°C
Storage Temperature Range	−55 to +150	°C
Lead Temperature	Soldering 10 s 230	°C
Operating Junction Temperature Range	0 to 125	°C (Continuous)
Operating Junction Temperature Range	0 to 200	°C (short term, 30 min. MAX.)

ELECTRICAL CHARACTERISTICS μPC7805H (V_{IN}=10 V, I_O=500 mA, 0 °C ≦ T_j ≦ 125 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITONS
Output Voltage	V_O	4.8	5.0	5.2	V	T_j=25 °C
		4.75		5.25		7 V≦V_{IN}≦20 V, 5 mA≦I_O≦1.0 A, P_T≦15 W
Line Regulation	REG_{IN}		3	100	mV	T_j=25 °C, 7 V≦V_{IN}≦25 V
			1	50		T_j=25 °C, 8 V≦V_{IN}≦12 V
Load Regulation	REG_L		15	100	mV	T_j=25 °C, 5 mA≦I_O≦1.5 A
			5	50		T_j=25 °C, 250 mA≦I_O≦750 mA
Quiescent Current	I_{BIAS}		4.2	8.0	mA	T_j=25 °C
Quiescent Current Change	ΔI_{BIAS}			1.3	mA	7 V≦V_{IN}≦25 V
				0.5		5 mA≦I_O≦1.0 A
Output Noise Voltage	N_L		40		μV	T_a=25 °C, 10 Hz≦f≦100 kHz
Ripple Rejection		62	78		dB	f=120 Hz, 8 V≦V_{IN}≦18 V
Dropout Voltage			2.0		V	I_O=1.0 A, T_j=25 °C
Output Resistance	R_O		17		mΩ	f=1 kHz
Short Circuit Current	I_{oshort}		750		mA	T_j=25 °C
Peak Output Current	I_{opeak}		2.2		A	T_j=25 °C
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$		−1.1		mV/°C	I_O=5 mA, 0 °C≦T_j≦125 °C

ELECTRICAL CHARACTERISTICS μPC7808H (V_{IN}=14 V, I_O=500 mA, 0 °C ≦ T_j ≦ 125 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Voltage	V_O	7.7	8.0	8.3	V	T_j=25 °C
		7.6		8.4		10.5 V≦V_{IN}≦23 V, 5 mA≦I_O≦1.0 A, P_T≦15 W
Line Regulation	REG_{IN}		6.0	160	mV	T_j=25 °C, 10.5 V≦V_{IN}≦25 V
			2.0	80		T_j=25 °C, 11 V≦V_{IN}≦17 V
Load Regulation	REG_L		12	160	mV	T_j=25 °C, 5 mA≦I_O≦1.5 A
			4.0	80		T_j=25 °C, 250 mA≦I_O≦750 mA
Quiescent Current	I_{BIAS}		4.3	8.0	mA	T_j=25 °C
Quiescent Current Change	ΔI_{BIAS}			1.0	mA	10.5 V≦V_{IN}≦25 V
				0.5		5 mA≦I_O≦1.0 A
Output Noise Voltage	N_L		52		μV	T_a=25 °C, 10 Hz≦f≦100 kHz
Ripple Rejection		56	72		dB	f=120 Hz, 11.5 V≦V_{IN}≦21.5 V
Dropout Voltage			2.0		V	I_O=1.0 A, T_j=25 °C
Output Resistance	R_O		18		mΩ	f=1 kHz
Short Circuit Current	I_{opeak}		350		A	T_j=25 °C
Peak Output Current	I_{opeak}		2.2		A	T_j=25 °C
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$		−0.8		mV/°C	I_O=5 mA, 0 °C≦T_j≦125 °C

ELECTRICAL CHARACTERISTICS μPC7812H (V_{IN}=19 V, I_O=500 mA, 0 °C ≦ T_j ≦ 125 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Voltage	V_O	11.5	12.0	12.5	V	T_j=25 °C
		11.4		12.6		14.5 V≦V_{IN}≦27 V, 5 mA≦I_O≦1.0 A, P_T≦15 W
Line Regulation	REG_{IN}		10	240	mV	T_j=25 °C, 14.5 V≦V_{IN}≦30 V
			3.0	120		T_j=25 °C, 16 V≦V_{IN}≦22 V
Load Regulation	REG_L		12	240	mV	T_j=25 °C, 5 mA≦I_O≦1.5 A
			4.0	120		T_j=25 °C, 250 mA≦I_O≦750 mA
Quiescent Current	I_{BIAS}		4.3	8.0	mA	T_j=25 °C
Quiescent Current Change	ΔI_{BIAS}			1.0	mA	14.5 V≦V_{IN}≦30 V
				0.5		5 mA≦I_O≦1.0 A
Output Noise Voltage	N_L		75		μV	T_a=25° C, 10 Hz≦f≦100 kHz
Ripple Rejection		55	71		dB	f=120 Hz, 15 V≦V_{IN}≦25 V
Dropout Voltage			2.0		V	I_O=1.0 A, T_j=25 °C
Output Resistance	R_O		18		mΩ	f=1 kHz
Short Circuit Current	I_{oshort}		350		mA	T_j=25 °C
Peak Output Current	I_{opeak}		2.2		A	T_j=25 °C
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$		−1.0		mV/°C	I_O=5 mA, 0 °C≦T_j≦125 °C

ELECTRICAL CHARACTERISTICS μPC7815H (V_{IN}=23 V, I_O=500 mA, 0 °C ≦ T_j ≦ 125 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Voltage	V_O	14.4	15.0	15.6	V	T_j=25 °C
		14.25		15.75		17.5 V≦V_{IN}≦30 V, 5 mA≦I_O≦1.0 A, P_T≦15 W
Line Regulation	REG_{IN}		11	300	mV	T_j=25 °C, 17.5 V≦V_{IN}≦30 V
			3.0	150		T_j=25 °C, 20 V≦V_{IN}≦26 V
Load Regulation	REG_L		12	300	mV	T_j=25 °C, 5 mA≦I_O≦1.5 A
			4.0	150		T_j=25 °C, 250 mA≦I_O≦750 mA
Quiescent Current	I_{BIAS}		4.4	8.0	mA	T_j=25 °C
Quiescent Current Change	ΔI_{BIAS}			1.0	mA	17.5 V≦V_{IN}≦30 V
				0.5		5 mA≦I_O≦1.0 A
Output Noise Voltage	N_L		90		μV	T_a=25 °C, 10 Hz≦f≦100 kHz
Ripple Rejection		54	70		dB	f=120 Hz, 18.5 V≦V_{IN}≦28.5 V
Dropout Voltage			2.0		V	I_O=1.0 A, T_j=25 °C
Output Resistance	R_O		19		mΩ	f=1 kHz
Short Circuit Current	I_{oshort}		230		mA	T_j=25 °C
Peak Output Current	I_{opeak}		2.1		A	T_j=25 °C
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$		−1.0		mV/°C	I_O=5 mA, 0 °C≦T_j≦125 °C

ELECTRICAL CHARACTERISTICS μPC7818H (V_{IN}=27 V, I_O=500 mA, 0 °C ≦ T_j ≦ 125 °C)

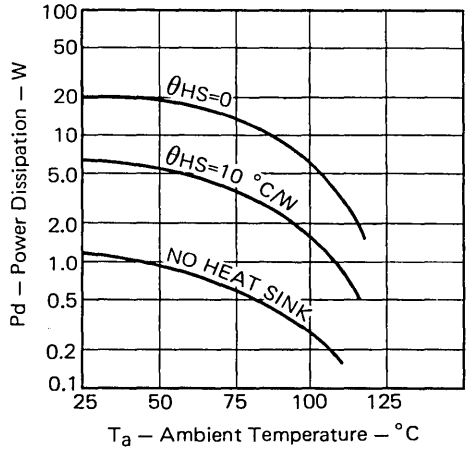
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Voltage	V_O	17.3	18.0	18.7	V	T_j=25 °C
		17.1		18.9		21 V≦V_{IN}≦33 V, 5 mA≦I_O≦1.0 A, P_T≦15 W
Line Regulation	REG_{IN}		15	360	mV	T_j=25 °C, 21 V≦V_{IN}≦33 V
			5.0	180		T_j=25 °C, 24 V≦V_{IN}≦30 V
Load Regulation	REG_L		12	360	mV	T_j=25 °C, 5 mA≦I_O≦1.5 A
			4.0	180		T_j=25 °C, 250 mA≦I_O≦750 mA
Quiescent Current	I_{BIAS}		4.5	8.0	mA	T_j=25 °C
Quiescent Current Change	ΔI_{BIAS}			1.0	mA	21 V≦V_{IN}≦33 V
				0.5		5 mA≦I_O≦1.0 A
Output Noise Voltage	N_L		110		μV	T_a=25 °C, 10 Hz≦f≦100 kHz
Ripple Rejection		53	69		dB	f=120 Hz, 22 V≦V_{IN}≦32 V
Dropout Voltage			2.0		V	I_O=1.0 A, T_j=25 °C
Output Resistance	R_O		22		mΩ	f=1 kHz
Short Circuit Current	I_{oshort}		200		mA	T_j=25 °C
Peak Output Current	I_{opeak}		2.1		A	T_j=25 °C
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$		−1.0		mV/°C	I_O=5 mA, 0 °C≦T_j≦125 °C

ELECTRICAL CHARACTERISTICS μPC7824H (V_{IN}=33 V, I_O=500 mA, 0 °C ≦ T_j ≦ 125 °C)

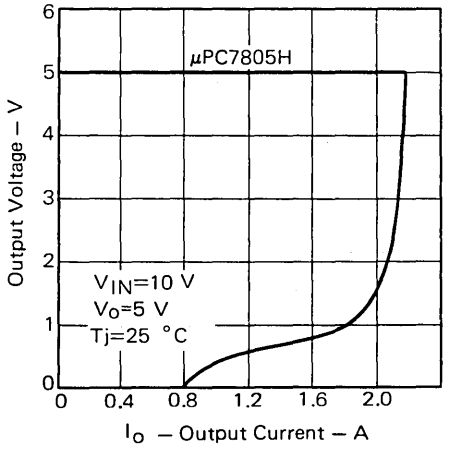
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Voltage	V_O	23.0	24.0	25.0	V	T_j=25 °C
		22.8		25.2		27 V≦V_{IN}≦38 V, 5 mA≦I_O≦1.0 A
Line Regulation	REG_{IN}		18	480	mV	T_j=25 °C, 27 V≦V_{IN}≦38 V
			6	240		T_j=25 °C, 30 V≦V_{IN}≦36 V
Load Regulation	REG_L		12	480	mV	T_j=25 °C, 5 mA≦I_O≦1.5 A
			4.0	240		T_j=25 °C, 250 mA≦I_O≦750 mA
Quiescent Current	I_{BIAS}		4.6	8.0	mA	T_j=25 °C
Quiescent Current Change	ΔI_{BIAS}			1.0	mA	27 V≦V_{IN}≦38 V
				0.5		5 mA≦I_O≦1.0 A
Output Noise Voltage	N_L		170		μV	T_a=25° C, 10 Hz≦f≦100 kHz
Ripple Rejection		50	66		dB	f=120 Hz, 28 V≦V_{IN}≦38 V
Dropout Voltage			2.0		V	I_O=1.0 A, T_j=25 °C
Output Resistance	R_O		28		mΩ	f=1 kHz
Short Circuit Current	I_{oshort}		150		mA	T_j=25 °C
Peak Output Current	I_{opeak}		2.1		A	T_j=25 °C
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$		−1.5		mV/° C	I_O=5 mA, 0 °C≦T_j≦125 °C

TYPICAL CHARACTERISTICS (T_a=25 °C)

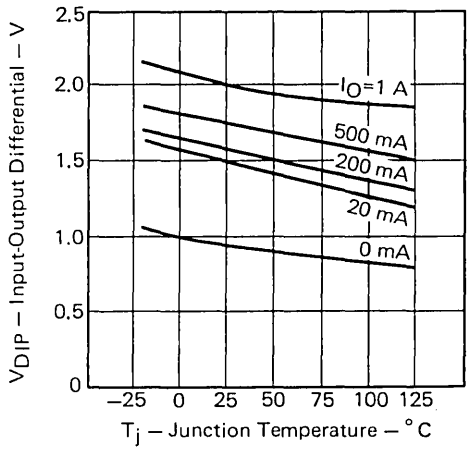
WORST CASE POWER DISSIPATION vs. AMBIENT TEMPERATURE



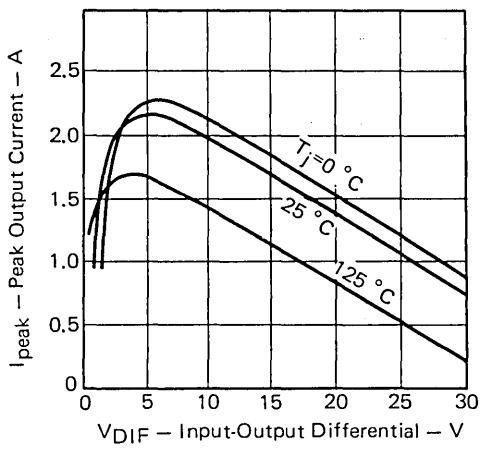
CURRENT LIMITING CHARACTERISTICS



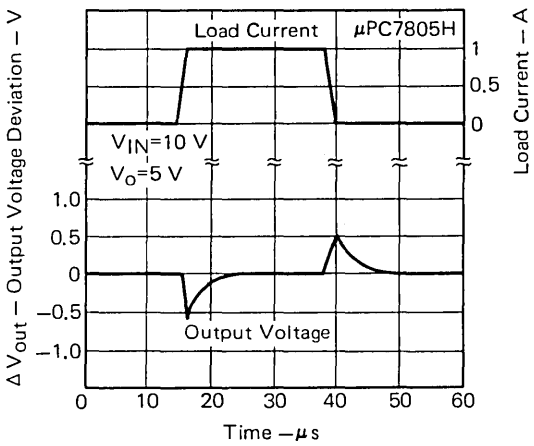
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



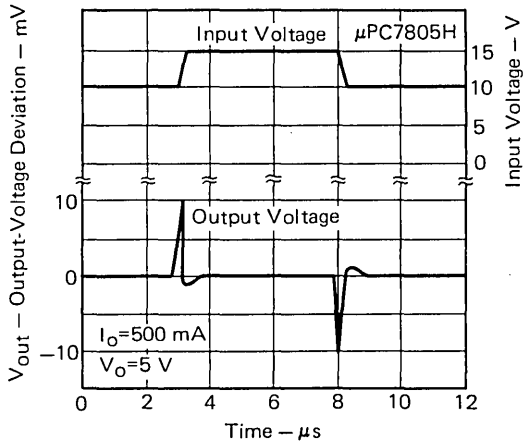
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT/OUTPUT DIFFERENTIAL VOLTAGE



LOAD TRANSIENT RESPONSE



LINE TRANSIENT RESPONSE



BIPOLAR ANALOG INTEGRATED CIRCUITS

μPC7900H SERIES

THREE TERMINAL NEGATIVE VOLTAGE REGULATORS

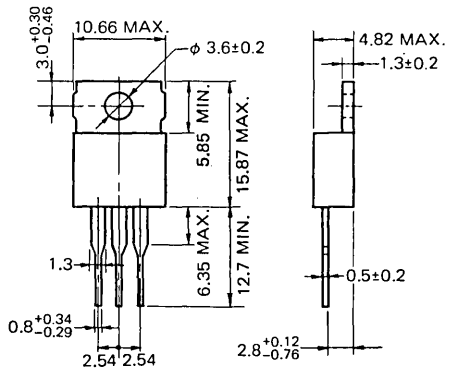
The μPC7900H series are monolithic three terminal negative regulators which employ internally current limiting, thermal shut down, and safe-area compensation, make them essentially indestructible. They are intended as fixed-voltage regulators in a wide range of application including local on card regulation for elimination of distribution problems associated with single point regulation.

FEATURES

- Output current in excess of 1 A
- No external component required
- Internal thermal overload protection
- Internal short circuit current limiting
- Low output resistance 70 mΩ

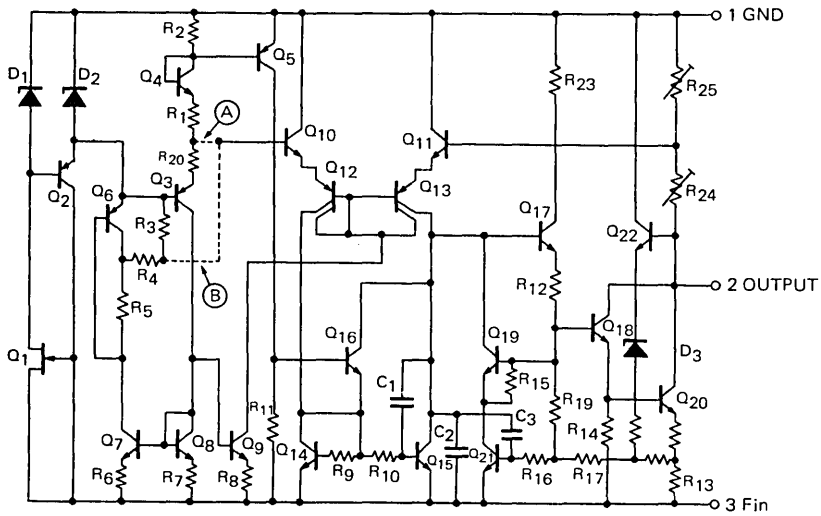
PACKAGE DIMENSIONS (Unit: mm)

Typical values unless specified



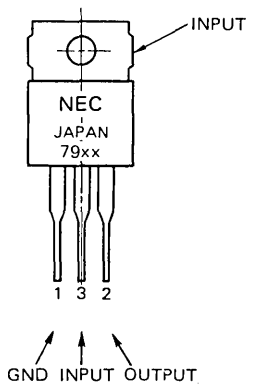
JEDEC : TO–220AB
IEC : –

EQUIVALENT CIRCUIT

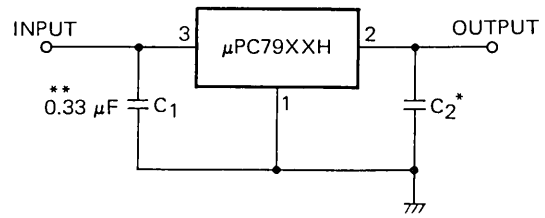


NOTE: Ⓐ –5 V to –8 V OPTIONS
Ⓑ –12 V to –24 V OPTIONS

CONNECTION DIAGRAM



TYPICAL APPLICATION



Notes: * Although no output capacitor is needed for stability, it does improve transient response.
** Required if regulator is located an appreciable distance from power supply filter.

THERMAL RESISTANCE

$R_{TH(j-c)}$	4 °C/W TYP.
$R_{TH(j-a)}$	83 °C/W TYP.

ABSOLUTE MAXIMUM RATINGS

Input Voltage	μPC7905H, 08H, 12H, 15H, 18H, 24H	−35	V
	μPC7924H	−40	V
Internal Power Dissipation		Internally Limited	
Operating Temperature Range		−20 to +80	°C
Storage Temperature Range		−55 to +150	°C
Lead Temperature		Soldering 10 s 230	°C
Operating Junction Temperature Range		0 to 125	°C (Continuous)
Operating Junction Temperature Range		0 to 200	°C (short term, 30 min. MAX.)

ELECTRICAL CHARACTERISTICS μPC7905H (V_{IN}=−10 V, I_O=500 mA, 0 °C ≦ Tj ≦ 125 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Voltage	Vo	−4.8	−5.0	−5.2	V	Tj=25 °C
		−4.75		−5.25		−7 V≦V_{IN}≦−20 V, 5 mA≦I_O≦1.0 A, P_T≦15 W
Line Regulation	REG_{IN}		3	100	mV	Tj=25 °C, −7 V≦V_{IN}≦−25 V
			1	50		Tj=25 °C, −8 V≦V_{IN}≦−12 V
Load Regulation	REG_L		70	150	mV	Tj=25 °C, 5 mA≦I_O≦1.5 A
			20	80		Tj=25 °C, 250 mA≦I_O≦750 mA
Quiescent Current	I_{BIAS}		1.0	2.0	mA	Tj=25 °C
Quiescent Current Change	ΔI_{BIAS}			1.3	mA	−7 V≦V_{IN}≦−25 V
				0.5		5 mA≦I_O≦1.0 A
Output Noise Voltage	N_L		100		μV	Ta=25 °C, 10 Hz≦f≦100 kHz
Ripple Rejection		54	62		dB	f=120 Hz, −8 V≦V_{IN}≦−18 V, I_O=500 mA
Dropout Voltage			1.1		V	I_O=1.0 A, Tj=25 °C
Peak Output Current	I_{opeak}		2.1		A	Tj=25 °C
Temperature Coefficient of Output Voltage	ΔVo/ΔT		−0.4		mV/°C	I_O=5 mA, 0 °C≦Tj≦125 °C

ELECTRICAL CHARACTERISTICS μPC7908H (V_{IN}=−14 V, I_O=500 mA, 0 °C ≦ Tj ≦ 125 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Voltage	Vo	−7.7	−8.0	−8.3	V	Tj=25 °C
		−7.6		−8.4		−10.5 V≦V_{IN}≦−23 V, 5 mA≦I_O≦1.0 A, P_T≦15 W
Line Regulation	REG_{IN}		6.0	160	mV	Tj=25 °C, −10.5 V≦V_{IN}≦−25 V
			2.0	80		Tj=25 °C, −11 V≦V_{IN}≦−17 V
Load Regulation	REG_L		80	200	mV	Tj=25 °C, 5 mA≦I_O≦1.5 A
			30	100		Tj=25 °C, 250 mA≦I_O≦750 mA
Quiescent Current	I_{BIAS}		1.0	2.0	mA	Tj=25 °C
Quiescent Current Change	ΔI_{BIAS}			1.0	mA	−10.5 V≦V_{IN}≦−25 V
				0.5		5 mA≦I_O≦1.0 A
Output Noise Voltage	N_L		200		μV	Ta=25 °C, 10 Hz≦f≦100 kHz
Ripple Rejection		54	62		dB	f=120 Hz, −11.5 V ≦ V_{IN} ≦ −21.5 V, I_O=500 mA
Dropout Voltage			1.1		V	I_O=1.0 A, Tj=25 °C
Peak Output Current	I_{opeak}		2.1		A	Tj=25 °C
Temperature Coefficient of Output Voltage	ΔVo/ΔT		−0.6		mV/°C	I_O=5 mA, 0 °C≦Tj≦125 °C

ELECTRICAL CHARACTERISTICS μPC7912H (V_{IN}=−19 V, I_O=500 mA, 0 °C ≦ Tj ≦ 125 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Voltage	Vo	−11.5	−12.0	−12.5	V	Tj=25 °C
		−11.4		−12.6		−14.5 V≦V_{IN}≦−27 V, 5 mA≦I_O≦1.0 A, P_T≦15 W
Line Regulation	REG_{IN}		10	240	mV	Tj=25 °C, −14.5 V≦V_{IN}≦−30 V
			3.0	120		Tj=25 °C, −16 V≦V_{IN}≦−22 V
Load Regulation	REG_L		85	240	mV	Tj=25 °C, 5 mA≦I_O≦1.5 A
			30	120		Tj=25 °C, 250 mA≦I_O≦750 mA
Quiescent Current	I_{BIAS}		1.5	3.0	mA	Tj=25 °C
Quiescent Current Change	ΔI_{BIAS}			1.0	mA	−14.5 V≦V_{IN}≦−30 V
				0.5		5 mA≦I_O≦1.0 A
Output Noise Voltage	N_L		300		μV	Ta=25 °C, 10 Hz≦f≦100 kHz
Ripple Rejection		54	62		dB	f=120 Hz, −15 V≦V_{IN}≦−25 V, I_O=500 mA
Dropout Voltage			1.1		V	I_O=1.0 A, Tj=25 °C
Peak Output Current	I_{opeak}		2.1		A	Tj=25 °C
Temperature Coefficient of Output Voltage	ΔVo/ΔT		−0.8		mV/°C	I_O=5 mA, 0 °C≦Tj≦125 °C

ELECTRICAL CHARACTERISTICS μPC7915H (V_{IN}=–23 V, I_O=500 mA, 0 °C ≦ Tj ≦ 125 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Voltage	Vo	–14.4	–15.0	–15.6	V	Tj=25 °C
		–14.25		–15.75		–17.5 V≦V_{IN}≦–30 V, 5 mA≦I_O≦1.0 A, P_T≦15 W
Line Regulation	REG_{IN}		11	300	mV	Tj=25 °C, –17.5 V≦V_{IN}≦–30 V
			3.0	150		Tj=25 °C, –20 V≦V_{IN}≦–26 V
Load Regulation	REG_L		90	300	mV	Tj=25 °C, 5 mA≦I_O≦1.5 A
			30	150		Tj=25 °C, 250 mA≦I_O≦750 mA
Quiescent Current	I_{BIAS}		1.5	3.0	mA	Tj=25 °C
Quiescent Current Change	ΔI_{BIAS}			1.0	mA	–17.5 V≦V_{IN}≦–30 V
				0.5		5 mA≦I_O≦1.0 A
Output Noise Voltage	N_L		375		μV	Ta=25 °C, 10 Hz≦f≦100 kHz
Ripple Rejection		54	60		dB	f=120 Hz, –18.5 V≦V_{IN}≦–28.5 V, I_O=500 mA
Dropout Voltage			1.1		V	I_O=1.0 A, Tj=25 °C
Peak Output Current	I_{opeak}		2.1		A	Tj=25 °C
Temperature Coefficient of Output Voltage	ΔVo/ΔT		–1.0		mV/°C	I_O=5 mA, 0 °C≦Tj≦125 °C

ELECTRICAL CHARACTERISTICS μPC7918H (V_{IN}=–27 V, I_O=500 mA, 0 °C ≦ Tj ≦ 125 °C)

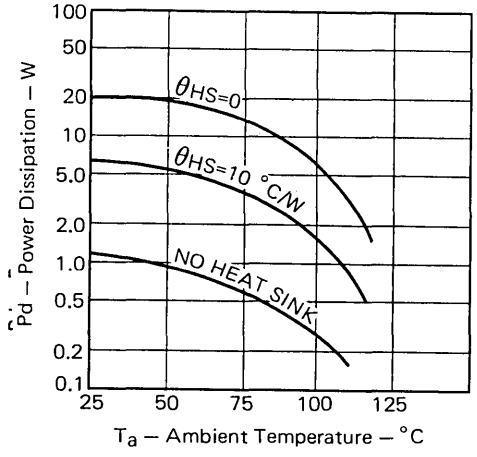
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Voltage	Vo	–17.3	–18.0	–18.7	V	Tj=25 °C
		–17.1		–18.9		–21 V≦V_{IN}≦–33 V, 5 mA≦I_O≦1.0 A, P_T≦15 W
Line Regulation	REG_{IN}		15	360	mV	Tj=25 °C, –21 V≦V_{IN}≦–33 V
			5.0	180		Tj=25 °C, –24 V≦V_{IN}≦–30 V
Load Regulation	REG_L		90	360	mV	Tj=25 °C, 5 mA≦I_O≦1.5 A
			30	180		Tj=25 °C, 250 mA≦I_O≦750 mA
Quiescent Current	I_{BIAS}		1.5	3.0	mA	Tj=25 °C
Quiescent Current Change	ΔI_{BIAS}			1.0	mA	–21 V≦V_{IN}≦–33 V
				0.5		5 mA≦I_O≦1.0 A
Output Noise Voltage	N_L		450		μV	Ta=25 °C, 10 Hz≦f≦100 kHz
Ripple Rejection		54	60		dB	f=120 Hz, –22 V≦V_{IN}≦–32 V, I_O=500 mA
Dropout Voltage			1.1		V	I_O=1.0 A, Tj=25 °C
Peak Output Current	I_{opeak}		2.1		A	Tj=25 °C
Temperature Coefficient of Output Voltage	ΔVo/ΔT		–1.0		mV/°C	I_O=5 mA, 0 °C≦Tj≦125 °C

ELECTRICAL CHARACTERISTICS μPC7924H (V_{IN}=−33 V, I_O=500 mA, 0 °C ≦ Tj ≦ 125 °C)

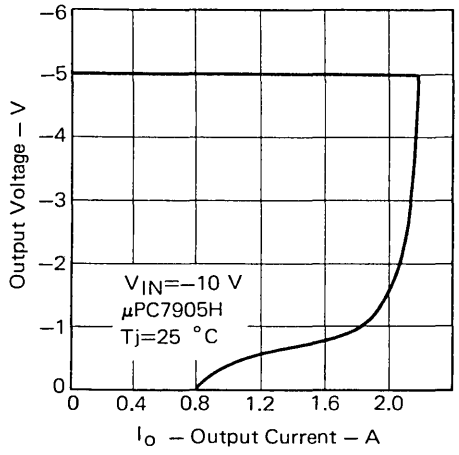
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Voltage	Vo	−23.0	−24.0	−25.0	V	Tj=25 °C
		−22.8		−25.2		−27 V≦V_{IN}≦−38 V, 5 mA≦I_O≦1.0 A
Line Regulation	REG_{IN}		18	480	mV	Tj=25 °C, −27 V≦V_{IN}≦−38 V
			6	240		Tj=25 °C, −30 V≦V_{IN}≦−36 V
Load Regulation	REG_L		90	480	mV	Tj=25 °C, 5 mA≦I_O≦1.5 A
			30	240		Tj=25 °C, 250 mA≦I_O≦750 mA
Quiescent Current	I_{BIAS}		1.5	3.0	mA	Tj=25 °C
Quiescent Current Change	ΔI_{BIAS}			1.0	mA	−27 V≦V_{IN}≦−38 V
				0.5		5 mA≦I_O≦1.0 A
Output Noise Voltage	N_L		600		μV	Ta=25 °C, 10 Hz≦f≦100 kHz
Ripple Rejection		51	59		dB	f=120 Hz, −28 V ≦ V_{IN} ≦ −38 V, I_O=500 mA
Dropout Voltage			1.1		V	I_O=1.0 A, Tj=25 °C
Peak Output Current	I_{opeak}		2.1		A	Tj=25 °C
Temperature Coefficient of Output Voltage	ΔVo/ΔT		−1.0		mV/°C	I_O=5 mA, 0 °C≦Tj≦125 °C

TYPICAL CHARACTERISTICS (Ta=25 °C)

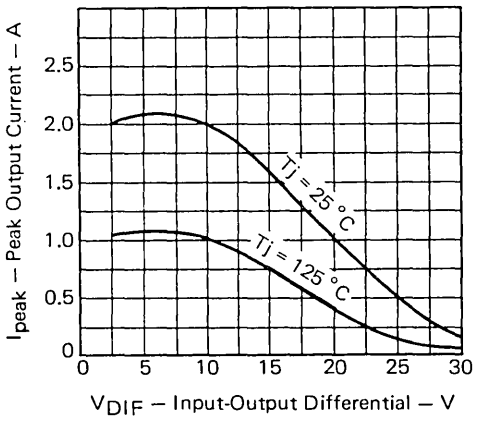
WORST CASE POWER DISSIPATION vs. AMBIENT TEMPERATURE



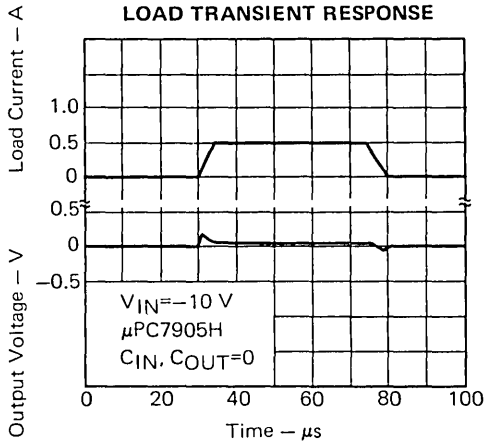
CURRENT LIMITING CHARACTERISTICS



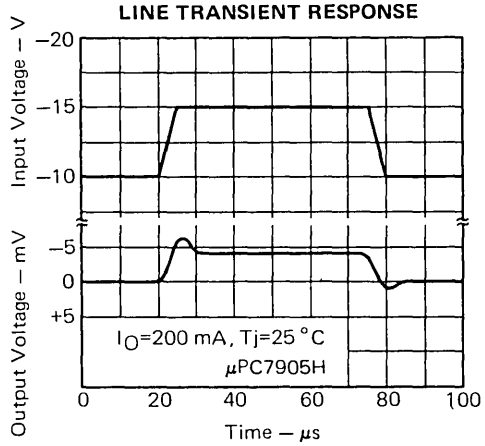
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT/OUTPUT DIFFERENTIAL VOLTAGE



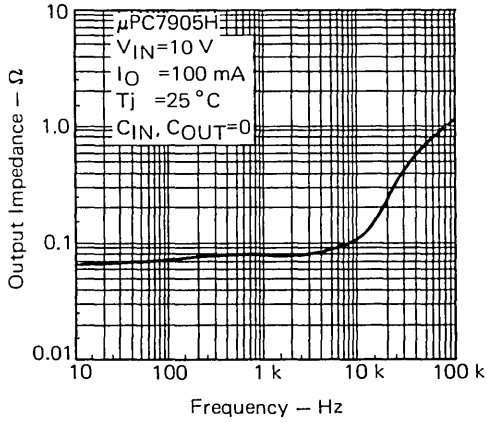
LOAD TRANSIENT RESPONSE



LINE TRANSIENT RESPONSE



OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY



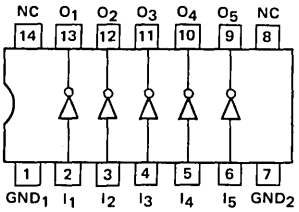
INDEX

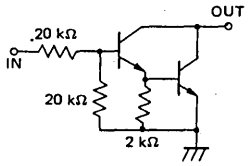
■ TRANSISTOR ARRAYS

μPA53C:
LED, LAMP, PRINTER HUMMER DRIVER

ABSOLUTE MAXIMUM RATINGS			ELECTRICAL CHARACTERISTICS			
SYMBOL	RATINGS	UNIT	SYMBOL	TYP.	UNIT	TEST CONDITIONS
V_{CEO}	30	V	h_{FE}	3200	–	V_{CE}=5.0 V I_C=200 mA
I_C	0.4	A/unit	$V_{CE(sat)1}$	0.9	V	I_C=100 mA V_{IN}=5.0 V
P_D*	1.2	W/pkg	$V_{CE(sat)2}$	1.3	V	I_C=400 mA V_{IN}=20 V

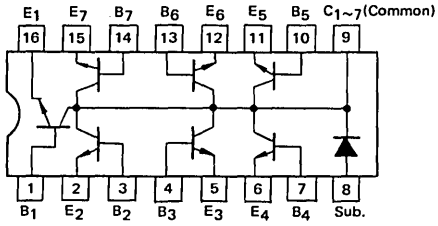
* PW=10 ms, duty cycle ≦ 10 %





μPA56C:
LED, LAMP DRIVER

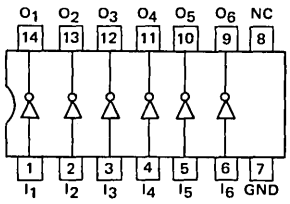
ABSOLUTE MAXIMUM RATINGS			ELECTRICAL CHARACTERISTICS			
SYMBOL	RATINGS	UNIT	SYMBOL	TYP.	UNIT	TEST CONDITIONS
V_{CEO}	40	V	h_{FE2}	200	–	V_{CE}=1.0 V I_C=50 mA
I_C	0.1	A/unit	$V_{CE(sat)2}$	0.2	V	I_C=50 mA I_B=5 mA
P_D	0.55	W/pkg	$V_{BE(sat)}$	0.86	V	I_C=50 mA I_B=5 mA

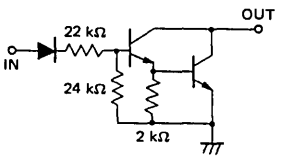


μPA67C:
PRINTER HUMMER DRIVER

ABSOLUTE MAXIMUM RATINGS			ELECTRICAL CHARACTERISTICS			
SYMBOL	RATINGS	UNIT	SYMBOL	MIN./MAX.	UNIT	TEST CONDITIONS
V_O	30	V	I_{ON}	100/–	mA	V_{IH} ≧ 5.0 V V_{CC}=2.0 V
I_O*	0.15	A/unit	I_{OFF}	–/10	μA	V_{IL} ≦ 1.0 V V_{CC}=20 V
P_D	0.55	W/pkg	V_{OL}	–/1.3	V	V_I=13 V I_O=100 mA

* PW=20 ms, duty cycle ≦ 10 % (All units turned on)

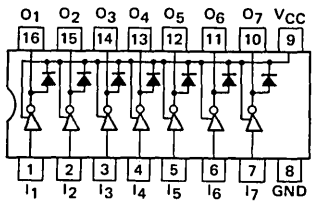


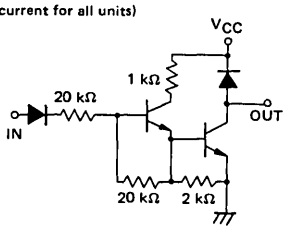


μPA79C:
PRINTER HUMMER DRIVER

ABSOLUTE MAXIMUM RATINGS			ELECTRICAL CHARACTERISTICS			
SYMBOL	RATINGS	UNIT	SYMBOL	TYP./MAX.	UNIT	TEST CONDITIONS
V_O	20	V	h_{FE}	2500/–	–	V_{CC}=5 V V_{CE}=1 V I_O=120 mA
I_O*	0.15	A/unit	$V_{CE(sat)}$	–/0.6	V	V_{CC}=5 V I_O=120 mA I_I=0.2 mA
P_D	0.55	W/pkg	V_I	–/4.0	V	V_{CC}=5 V V_{CE}=1 V I_O=120 mA

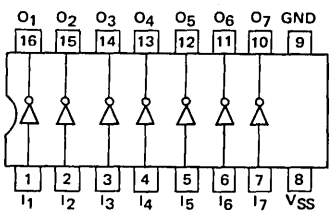
* PW ≦ 30 ms, duty cycle ≦ 10 % (The same current for all units)

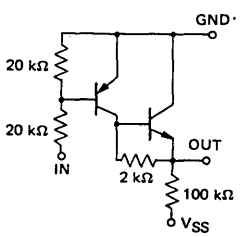




μPA80C:
FIP, LED DRIVER

ABSOLUTE MAXIMUM RATINGS			ELECTRICAL CHARACTERISTICS			
SYMBOL	RATINGS	UNIT	SYMBOL	TYP.	UNIT	TEST CONDITIONS
V_{SS}	–60	V	h_{FE1}	280	–	V_{CE}=2.0 V I_O=20 mA
I_O	50	mA/unit	h_{FE2}	450	–	V_{CE}=2.0 V I_O=40 mA
P_D	0.55	W/pkg	$V_{CE(sat)}$	0.95	V	I_O=20 mA I_I=0.3 mA

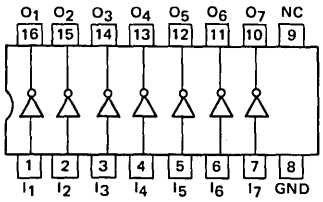


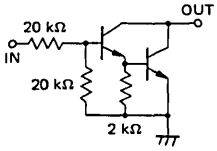


μPA81C:
LED, LAMP, PRINTER HUMMER DRIVER

ABSOLUTE MAXIMUM RATINGS			ELECTRICAL CHARACTERISTICS			
SYMBOL	RATINGS	UNIT	SYMBOL	TYP.	UNIT	TEST CONDITIONS
V_{CC}	45	V	h_{FE}	2500	–	V_{CE}=2.5 V I_O=200 mA
I_O*	0.4	A/unit	$V_{CE(sat)1}$	0.82	V	I_O=100 mA V_I=13 V
P_D	0.8	W/pkg	$V_{CE(sat)3}$	1.2	V	I_O=400 mA V_I=13 V

* PW=10 ms, duty cycle ≦ 10 % (All units turned on)

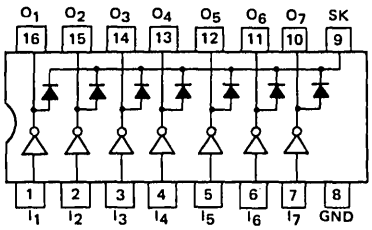




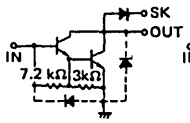
μPA2001C, 2002C, 2003C, 2004C:
LED, LAMP, RELAY, PRINTER HUMMER DRIVER

ABSOLUTE MAXIMUM RATINGS			ELECTRICAL CHARACTERISTICS			
SYMBOL	RATINGS	UNIT	SYMBOL	TYP.	UNIT	TEST CONDITIONS
V_{CC}	60	V	h_{FE}	2800	–	V_{CE}=2.0 V I_O=350 mA
I_O	0.5	A/unit	$V_{CE(sat)1}$	0.9	V	I_O=100 mA I_I=250 μA
P_D*	2.5	W/pkg	$V_{CE(sat)3}$	1.2	V	I_O=350 mA I_I=500 μA

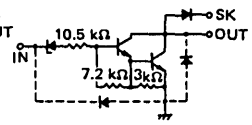
* PW≦20 ms, duty cycle ≦10 % (The same current for all units)



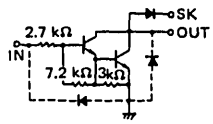
μPA2001C



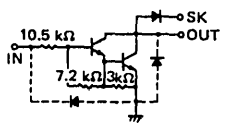
μPA2002C



μPA2003C



μPA2004C

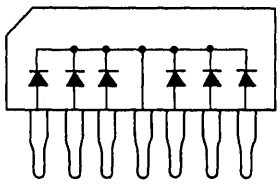


■ DIODE ARRAYS

μPA54H:
HIGH SPEED SWITCHING

ABSOLUTE MAXIMUM RATINGS			ELECTRICAL CHARACTERISTICS			
SYMBOL	RATINGS	UNIT	SYMBOL	TYP.	UNIT	TEST CONDITIONS
V_{RM}	75	V	V_F	0.8	V	I_F=30 mA
V_R	50	V	I_R	0.01	μA	V_R=30 V
I_O	0.1	A/unit	C_t*	2.0	pF	V_R=0 f=1.0 MHz
P_D	0.3	W/pkg	t_{rr}	1.3	ns	Refer to the individual catalogue.

* 1 unit

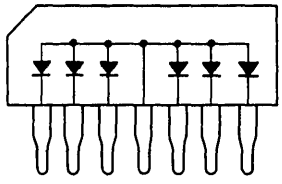


(Common Cathode)

μPA64H:
HIGH SPEED SWITCHING

ABSOLUTE MAXIMUM RATINGS			ELECTRICAL CHARACTERISTICS			
SYMBOL	RATINGS	UNIT	SYMBOL	TYP.	UNIT	TEST CONDITIONS
V_{RM}	75	V	V_F	0.8	V	I_F=30 mA
V_R	50	V	I_R	0.005	μA	V_R=30 V
I_O	0.1	A/unit	C_t*	5.0	pF	V_R=0 f=1.0 MHz
P_D	0.3	W/pkg	t_{rr}	4.0	ns	Refer to the individual catalogue.

* 1 unit



(Common Anode)

TRANSISTOR ARRAY
μPA53C

LED, LAMP DRIVER
NPN SILICON EPITAXIAL DARLINGTON TRANSISTOR ARRAY

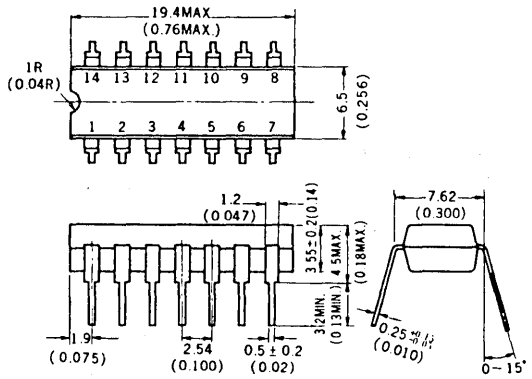
DESCRIPTION

The μPA53C is a monolithic array of five darlington transistors.

Applications are printer hummer driver and LED display driver with MOS output signal.

PACKAGE DIMENSIONS

in millimeters (inches)



FEATURES

- High DC Current Gain
- High Output Drive Current
- Package is 14pin PLASTIC DIP.

ABSOLUTE MAXIMUM RATINGS

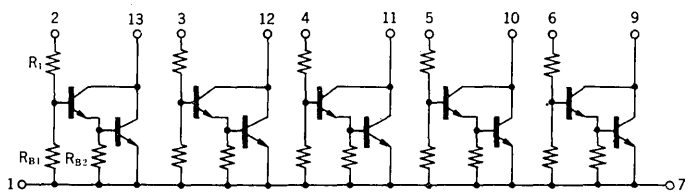
Maximum Voltages and Currents (Ta = 25°C)			
Collector to Base Voltage ($R_{BE}=\infty$)	V_{CBO}	30	V
Collector to Emitter Voltage (Open Base)	V_{CEO}	30	V
Input Voltage	V_{IN}	30	V
Continuous Collector Current	$I_{C(DC)}$	0.4	A/unit
Peak Collector Current	I_C*	2.0	A/package
Maximum Power Dissipation			
Total Power Dissipation	P_T*	1.2	W/package
Maximum Temperature			
Storage Temperature	T_{stg}	-40 to +125	°C
Operating Temperature	T_{opt}	-25 to + 75	°C

*PW = 10ms, duty cycle ≦ 10%

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

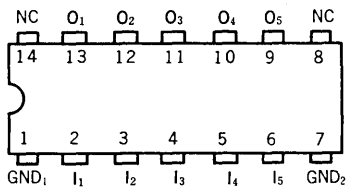
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	I_L		0.5	100	μA	V_{CE}=20V, V_{IN}=0
DC Current Gain	h_{FE}	2000	3200			V_{CE}=5.0V, I_C=200mA
Collector Saturation Voltage	$V_{CE(sat)1}$		0.9	1.3	V	I_C=100mA, V_{IN}=5.0V
Collector Saturation Voltage	$V_{CE(sat)2}$		1.3	2.2	V	I_C=400mA, V_{IN}=20V

EQUIVALENT CIRCUIT



R_1 20kΩ
R_{B_1} 20kΩ
R_{B_2} 2kΩ

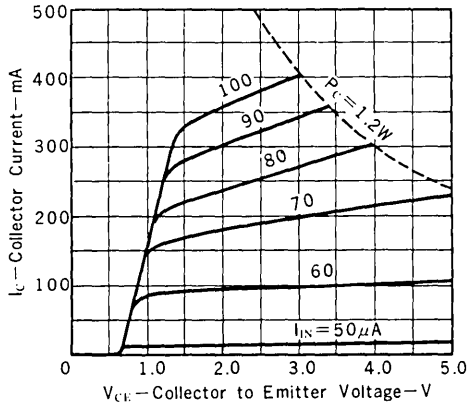
CONNECTION DIAGRAM (Top View)



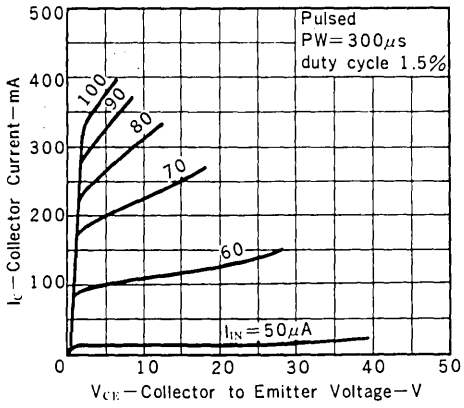
I : Input(Base)
O : Output(Collector)
GND(Common Emitter)

TYPICAL CHARACTERISTICS (Ta = 25°C)

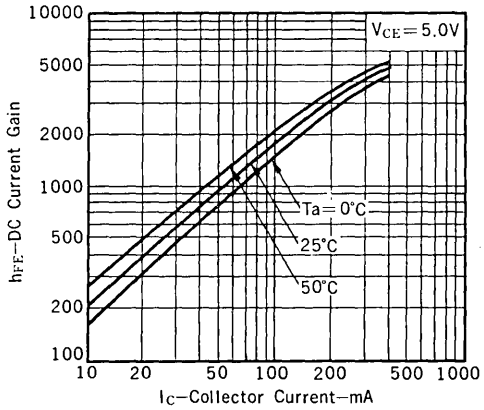
COLLECTOR CURRENT vs.
COLLECTOR TO EMITTER VOLTAGE



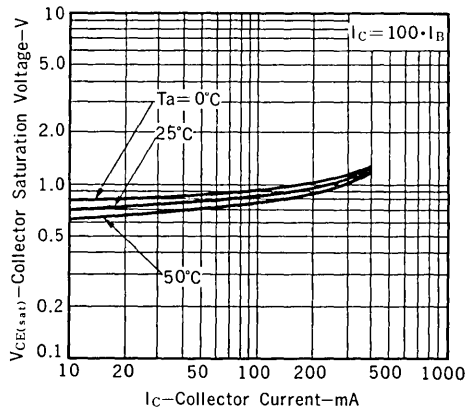
COLLECTOR CURRENT vs.
COLLECTOR TO EMITTER VOLTAGE



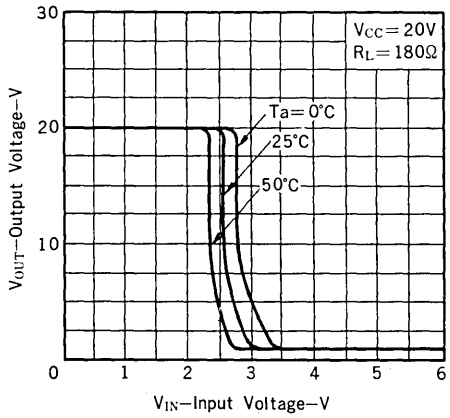
DC CURRENT GAIN vs.
COLLECTOR CURRENT



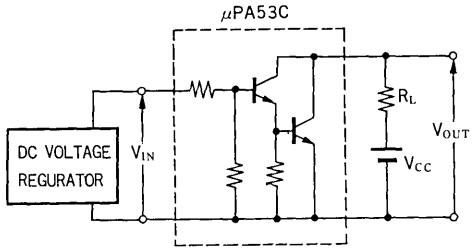
COLLECTOR SATURATION VOLTAGE
vs. COLLECTOR CURRENT



OUTPUT VOLTAGE vs.
INPUT VOLTAGE



V_{OUT}-V_{IN} TEST CIRCUIT



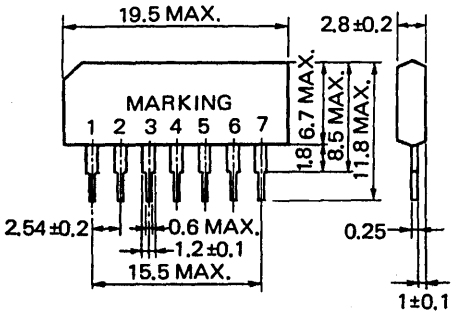
DIODE ARRAY
μPA54H

HIGH SPEED SWITCHING
SILICON EPITAXIAL DIODE ARRAY

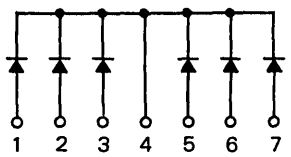
DESCRIPTION

The μPA54H is a common cathode monolithic array of six high speed switching diodes.

PACKAGE DIMENSIONS
in millimeters



PIN CONNECTION



Common Cathode

FEATURES

- High Speed Switching Time — t_{rr} 1.3 ns TYP.
- Small Terminal Capacitance — C_t 2.0 pF TYP.
- Small Size enables High Density Mounting
- Good Electrical Thermal Balance of Six Diodes due to 1 Chip Structure
- Package is 7 pin PLASTIC SIP.

ABSOLUTE MAXIMUM RATINGS

Maximum Voltages and Currents (Ta = 25 °C)			
Peak Reverse Voltage	V_{RM}	75	V
Reverse Voltage	V_R	50	V
Peak Forward Surge Current (1 μs)	$I_{F(surge)}$	1.0*	A
Peak Forward Current	I_{FM}	200*	mA
Average Rectified Current	I_o	100*	mA
Maximum Power Dissipation (Ta=25 °C)			
Power Dissipation	P	300**	mW
Maximum Temperatures			
Junction Temperature	T_j	125	°C
Storage Temperature	T_{stg}	−55 to +125	°C

*1 Unit **Package

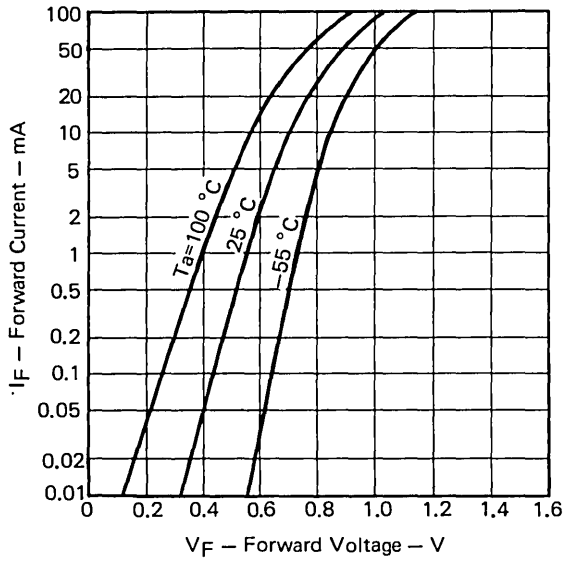
ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP	MAX.	UNIT	TEST CONDITIONS
Forward Voltage	V_F		0.8	1.0	V	I_F=30 mA
Reverse Current	I_R		0.01	0.1	μA	V_R=30 V
Terminal Capacitance *	C_t		2.0	4.0	pF	V_R=0, f=1.0 MHz
Reverse Recovery Time	t_{rr}		1.3	3.0	ns	See trr Reverse Recovery Time Test Circuit

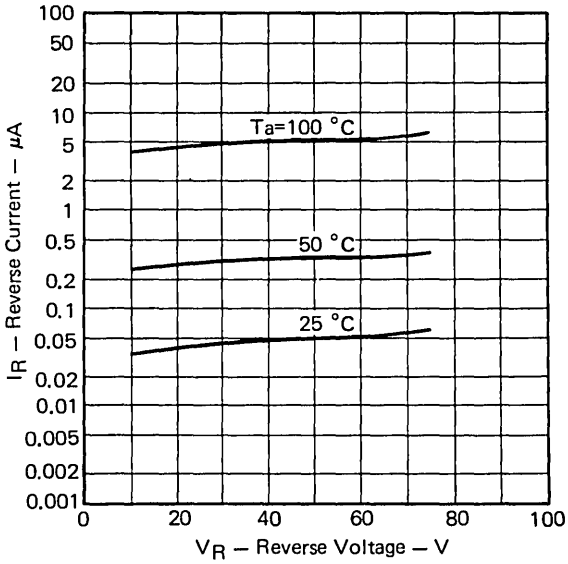
* 1 Unit

TYPICAL CHARACTERISTICS (Ta=25 °C)

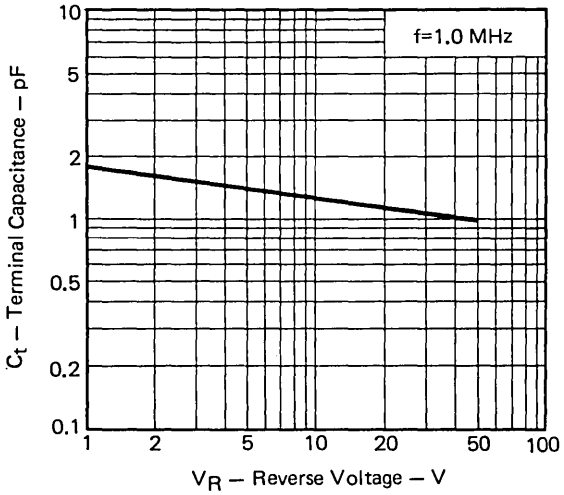
FORWARD CURRENT vs.
FORWARD VOLTAGE



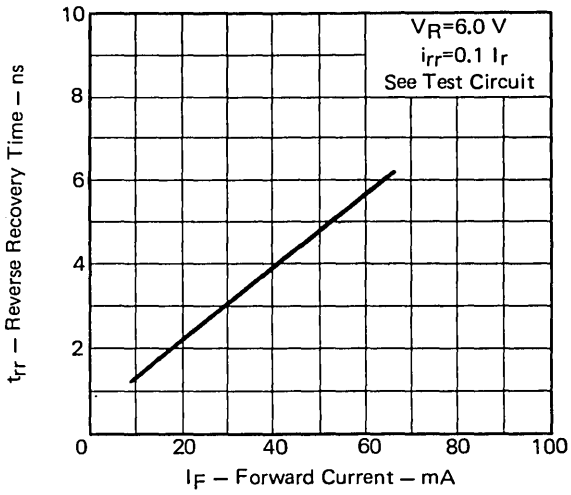
REVERSE CURRENT vs.
REVERSE VOLTAGE



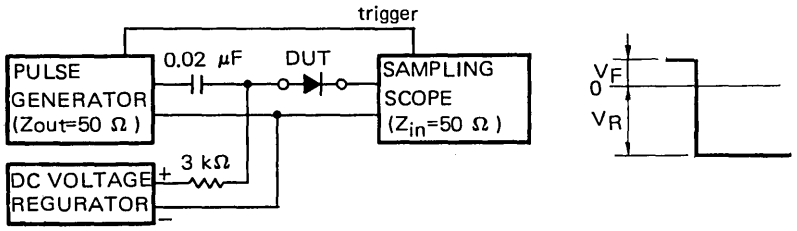
TERMINAL CAPACITANCE vs.
REVERSE VOLTAGE

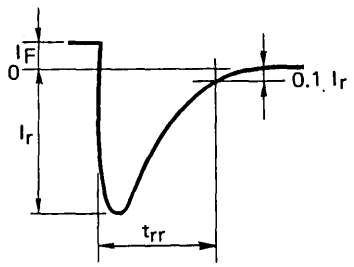


REVERSE RECOVERY TIME vs.
FORWARD CURRENT



t_{rr} REVERSE RECOVERY TIME TEST CIRCUIT





Test Conditions: I_F=10 mA, V_R=6 V, R_L=100 Ω i_{rr}=0.1 I_r

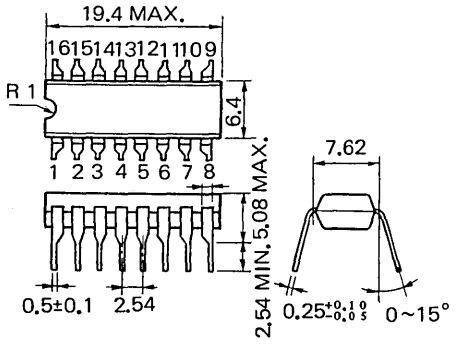
TRANSISTOR ARRAY
μPA56C

SEGMENT DRIVER
NPN SILICON EPITAXIAL TRANSISTOR ARRAY

DESCRIPTION

The μPA56C is a monolithic array of seven transistors.
This device is especially suited for driving common cathode seven segment LED, relays, and lamps.

PACKAGE DIMENSIONS
in millimeters



FEATURES

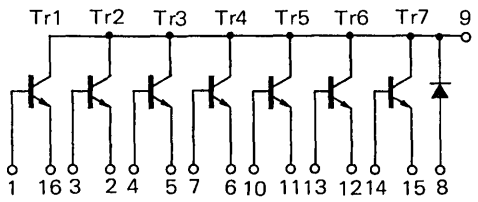
- High Voltage Ratings V_{CBO}=60 V
- Package is 16 Pin PLASTIC DIP.

ABSOLUTE MAXIMUM RATINGS

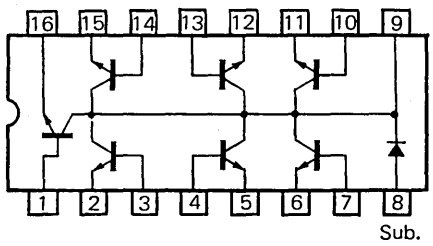
Maximum Voltages and Currents (T_a = 25 °C)

Collector to Base Voltage	V_{CBO}	60	V
Collector to Emitter Voltage	V_{CEO}	40	V
Emitter to Base Voltage	V_{EBO}	5.0	V
Continuous Collector Current	$I_{C(DC)}$	100	mA/unit
Continuous Collector Current	$I_{C(DC)}$	550	mA/package
Maximum Power Dissipation			
Total Power Dissipation	P_d	550	mW/package
Maximum Temperature			
Operating Temperature	T_{opt}	−25 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM (Top View)



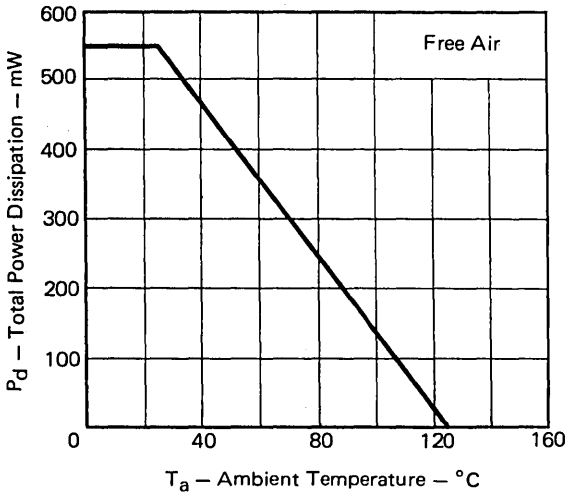
Note: Sub. —terminal is to be connected to the lowest voltage level in the application.

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

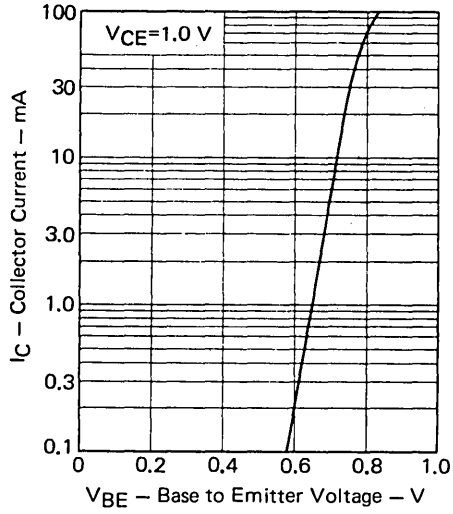
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Collector Cutoff Current	I_{CBO}		0.001	0.1	μA	V_{CB}=40 V, I_E=0
Emitter Cutoff Current	I_{EBO}		0.001	0.1	μA	V_{EB}=3.0 V, I_C=0
DC Current Gain	h_{FE1}	50	250			V_{CE}=1.0 V, I_C=10 mA
DC Current Gain	h_{FE2}	40	200			V_{CE}=1.0 V, I_C=50 mA
Collector Saturation Voltage	$V_{CE(sat)1}$		0.07	0.3	V	I_C=10 mA, I_B=1.0 mA
Collector Saturation Voltage	$V_{CE(sat)2}$		0.2	0.6	V	I_C=50 mA, I_B=5.0 mA
Base Saturation Voltage	$V_{BE(sat)}$		0.86	1.0	V	I_C=50 mA, I_B=5.0 mA
Gain Bandwidth Product	f_T		320		MHz	V_{CE}=10 V, I_E=−10 mA
Output Capacitance	C_{ob}		4.0		pF	V_{CB}=10 V, I_E=0, f=1.0 MHz
Turn On Time	t_{on}		40		ns	See Switching Time Test Circuit
Storage Time	t_{stg}		200		ns	
Turn Off Time	t_{off}		230		ns	

TYPICAL CHARACTERISTICS (T_a = 25 °C)

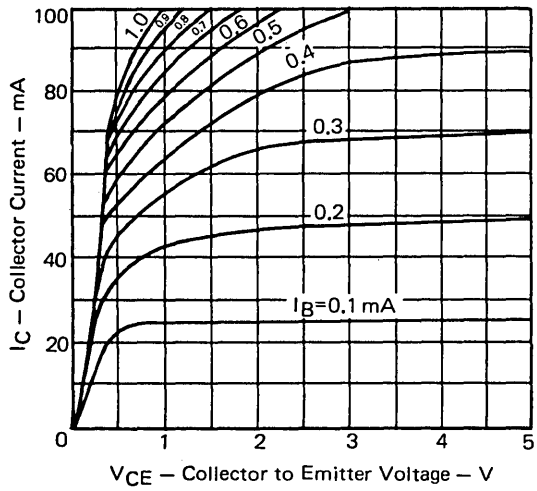
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



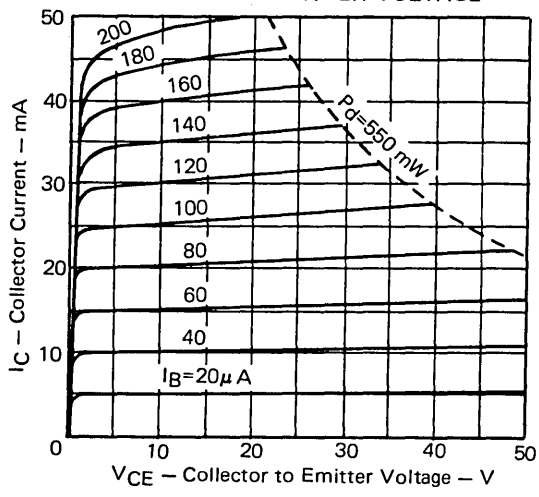
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



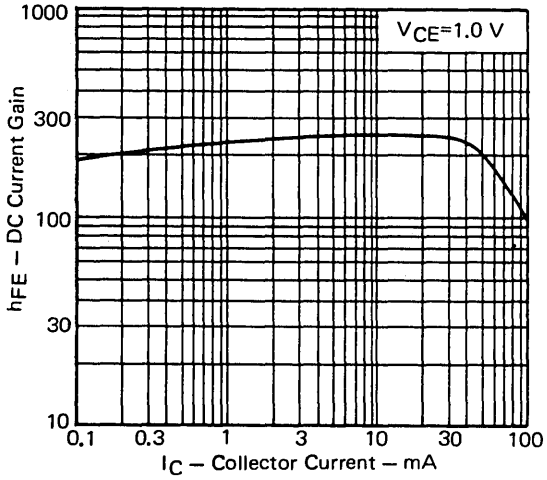
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



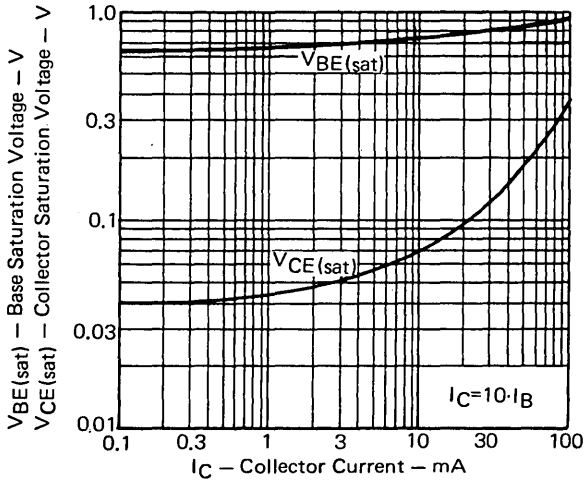
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



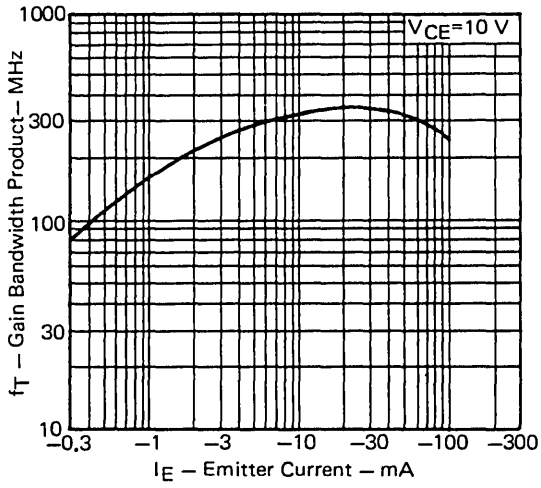
DC CURRENT GAIN vs. COLLECTOR CURRENT



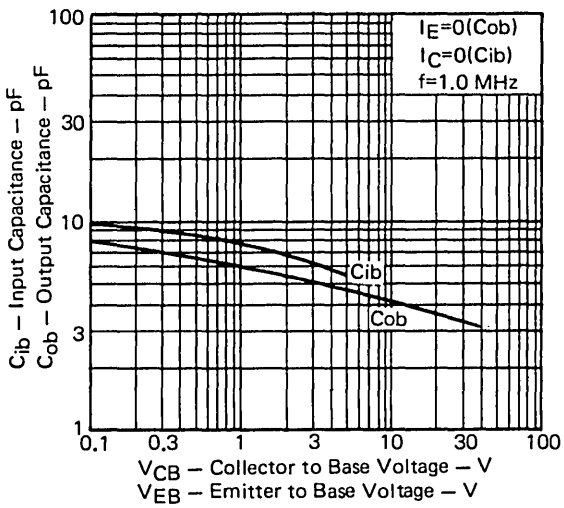
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



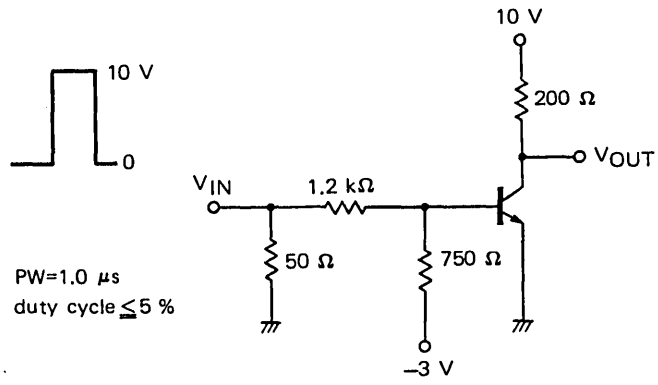
GAIN BANDWIDTH PRODUCT vs.
EMITTER CURRENT



INPUT AND OUTPUT CAPACITANCE vs.
REVERSE VOLTAGE



SWITCHING TIME TEST CIRCUIT



DIODE ARRAY
μPA64H

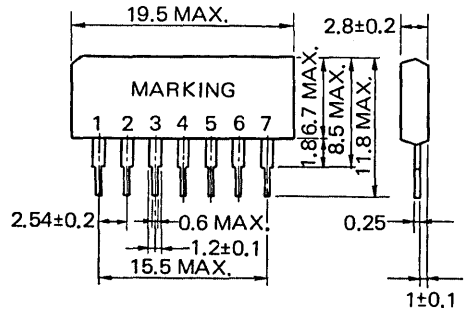
HIGH SPEED SWITCHING
SILICON EPITAXIAL DIODE ARRAY

DESCRIPTION

The μPA64H is a common anode monolithic array of six high speed switching diodes.

PACKAGE DIMENSIONS

in millimeters



FEATURES

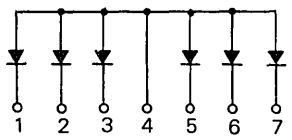
- High Speed Switching Time — t_{rr} 4.0 ns TYP.
- Small Terminal Capacitance — Ct 5.0 pF TYP.
- Small Size enables High Density Mounting
- Good Electrical Thermal Balance of Six Diode due to 1 Chip Structure
- Package is 7 pin PLASTIC SIP.

ABSOLUTE MAXIMUM RATINGS

Maximum Voltages and Currents (T_a = 25 °C)			
Peak Reverse Voltage	V_{RM}	75	V
Reverse Voltage	V_R	50	V
Peak Forward Surge Current (1 μs)	$I_{F\ (surge)}$	1.0*	A
Peak Forward Current	I_{FM}	200*	mA
Average Rectified Current	I_O	100*	mA
Maximum Power Dissipation (Ta=25 °C)			
Power Dissipation	P	300**	mW
Maximum Temperatures			
Junction Temperature	T_j	125	°C
Storage Temperature	T_{stg}	−55 to +125	°C

* 1 Unit ** Package

PIN CONNECTION



Common Anode

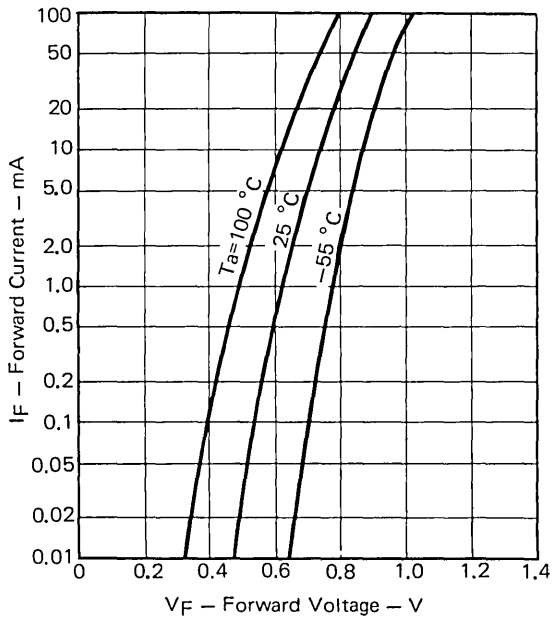
ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Forward Voltage	V_F		0.8	1.0	V	I_F=30 mA
Reverse Current	I_R		0.005	0.1	μA	V_R=30 V
Terminal Capacitance*	Ct		5.0	8.0	pF	V_R=0, f=1.0 MHz
Reverse Recovery Time	t_{rr}		4.0	8.0	ns	See t_{rr} Reverse Recovery Time Test Circuit

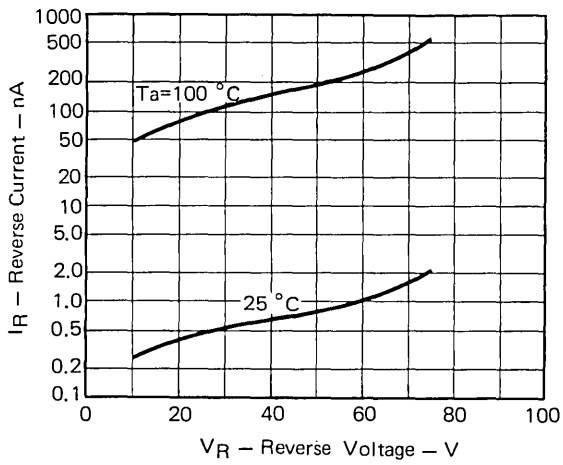
* 1 Unit

TYPICAL CHARACTERISTICS (Ta = 25 °C)

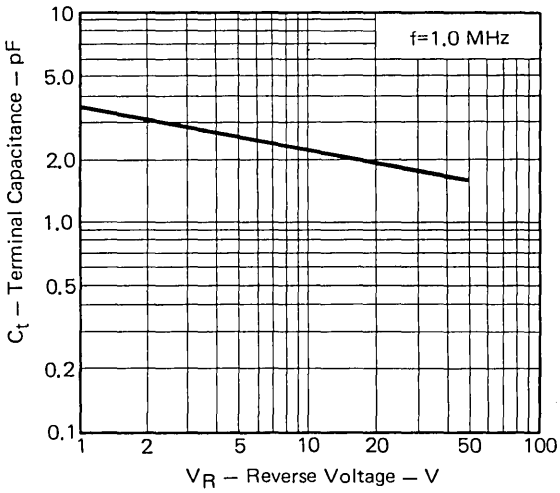
FOWARD CURRENT vs.
FORWARD VOLTAGE



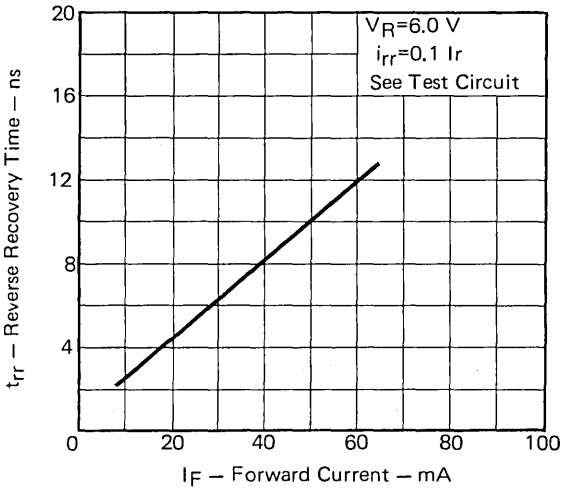
REVERSE CURRENT vs.
REVERSE VOLTAGE



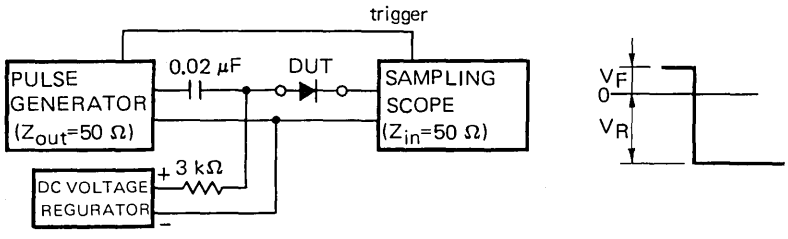
TERMINAL CAPACITANCE vs.
REVERSE VOLTAGE

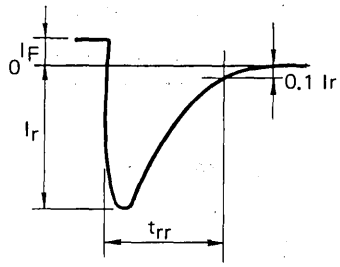


REVERSE RECOVERY TIME vs.
FORWARD CURRENT



trr REVERSE RECOVERY TIME TEST CIRCUIT





Test Conditions : I_F=10 mA, V_R=6 V, R_L=100 Ω, i_{rr}=0.1 Ir

TRANSISTOR ARRAY
μPA67C

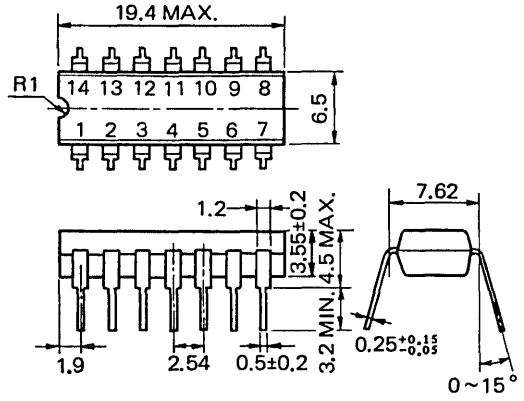
MINI PRINTER DRIVER
NPN SILICON EPITAXIAL DARLINGTON TRANSISTOR ARRAY

DESCRIPTION

The μPA67C is a monolithic array of six darlington transistors.
This device is especially suited for driving miniprinter hummer with up to 0.1 A output current per unit.

PACKAGE DIMENSIONS

in millimeters



FEATURES

- High DC Current Gain
- Package is 14 pin PLASTIC DIP.

ABSOLUTE MAXIMUM RATINGS

Maximum Voltages and Currents (Ta = 25 °C)

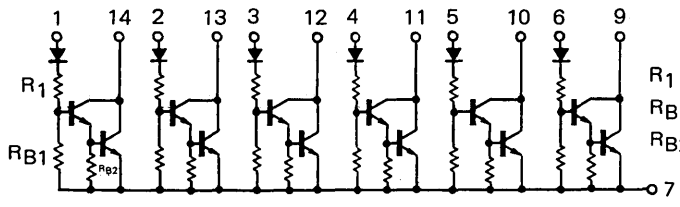
Output Voltage	V_O	30	V
Input Voltage	V_I	−40 to + 30	V
Peak Output Current	I_O**	150	mA/unit
Continuous Collector Current	I_O*	70	mA/unit
Maximum Power Dissipation			
Total Power Dissipation	Pd	550	mW/package
Maximum Temperature			
Operating Temperature	T_{opt}	−25 to + 75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

** PW=20 ms, duty cycle≦10 % (All units turned on)
* DC (All units turned on)

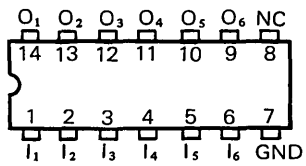
ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Leakage Current	I_L			10	μA	V_{CE}=20 V, V_I=0
Output On Current	I_{ON}	100			mA	V_{IH}≧5.0 V, V_{CE}=2.0 V
Output Off Current	I_{OFF}			10	μA	V_{IL}≦1.0 V, V_{CE}=20 V
Input Current	I_I			1.3	mA	V_I=20 V, V_{CE}=0
Input Reverse Current	$I_{I(R)}$			−10	μA	V_I=−30 V, V_{CE}=0
Low Level Output Voltage	V_{OL}			1.3	V	V_I=13 V, I_O=100 mA

EQUIVALENT CIRCUIT



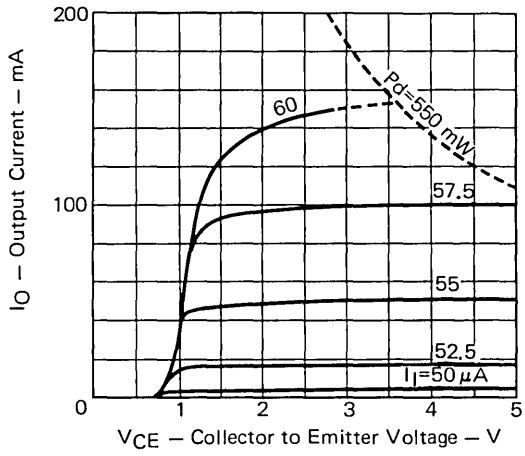
CONNECTION DIAGRAM (Top View)



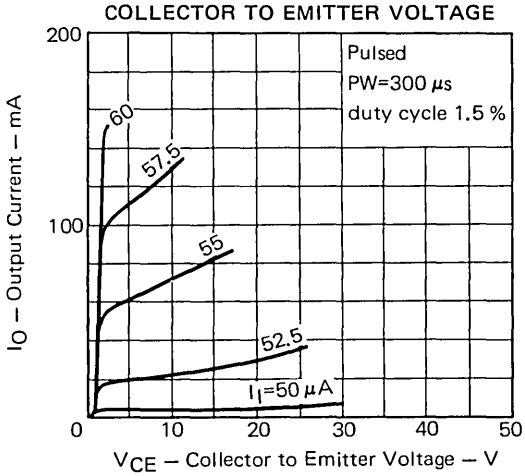
I : Input (Base)
O : Output (Collector)
GND : (Common Emitter)

TYPICAL CHARACTERISTICS (Ta = 25 °C)

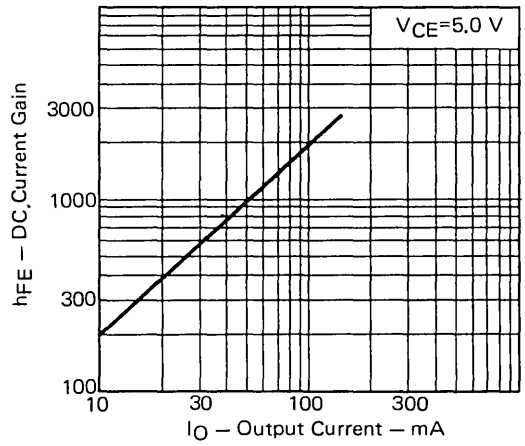
OUTPUT CURRENT vs.
COLLECTOR TO EMITTER VOLTAGE



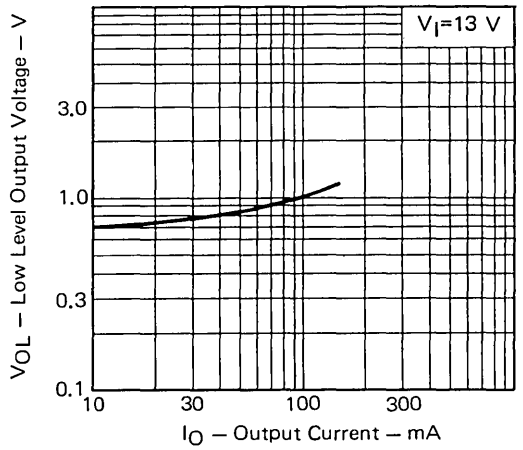
OUTPUT CURRENT vs.
COLLECTOR TO EMITTER VOLTAGE



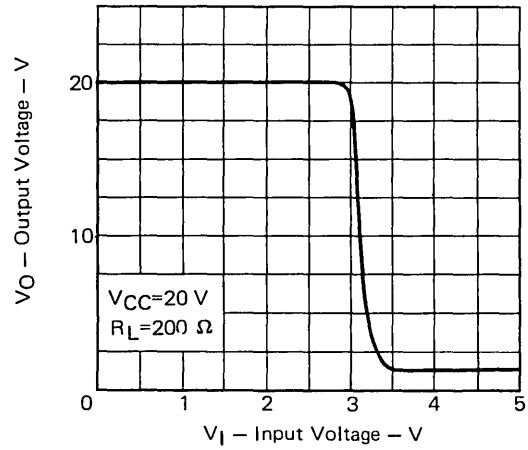
DC CURRENT GAIN vs.
OUTPUT CURRENT



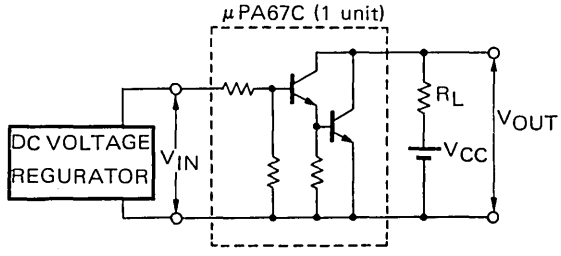
LOW LEVEL OUTPUT VOLTAGE vs.
OUTPUT CURRENT



OUTPUT VOLTAGE vs.
INPUT VOLTAGE



V_O–V_I TEST CIRCUIT



TRANSISTOR ARRAY
μPA79C

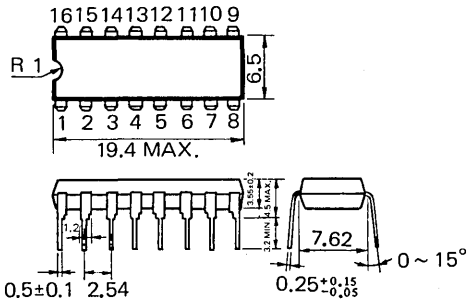
MINI PRINTER DRIVER
NPN SILICON EPITAXIAL TRANSISTOR ARRAY

DESCRIPTION

The μPA79C is a monolithic array of seven transistors.
This device is especially suited for driving low supply voltage printer with up to 0.1 A output current per unit.

PACKAGE DIMENSIONS

in millimeters



FEATURES

- Low Saturation Voltage → $V_{CE(sat)} \leqq 0.6$ V
- High DC Current Gain → $h_{FE} \geqq 1000$
- Reverse Bias Protected Inputs
- Transient Protected Outputs
- Package is 16 pin PLASTIC DIP

ABSOLUTE MAXIMUM RATINGS

Maximum Voltages and Currents (Ta = 25 °C)

Supply Voltage	V_{CC}	20	V
Input Voltage	V_I	−40 to + 30	V
Output Voltage	V_O	20	V
Continuous Output Current	$I_{C(DC)}$**	200	mA/unit
Peak Output Current	I_C*	150	mA/unit
Maximum Power Dissipation			
Total Power Dissipation	Pd	550	mW/package
Maximum Temperature			
Operating Temperature	T_{opt}	−25 to + 75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

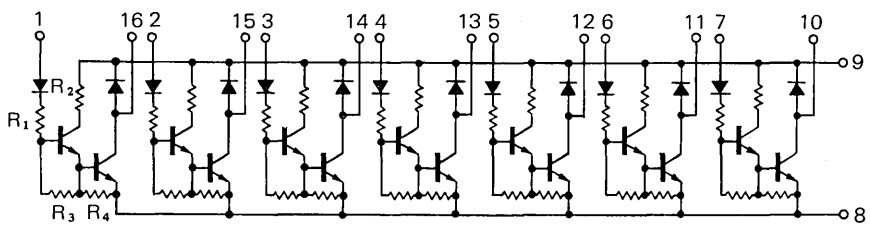
**DC (1 unit)

* PW ≦ 30 ms, duty cycle ≦ 10 % (The same current for all units)

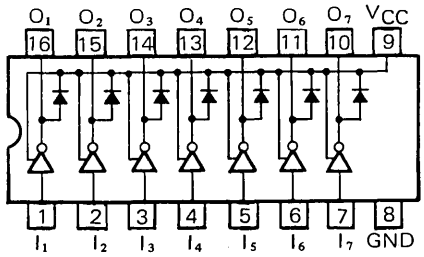
ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Leakage Current	I_{L1}			10	μA	V_{CC}=20 V, V_I=0
DC Current Gain	h_{FE}	1000	2500			V_{CC}=5 V, V_{CE}=1 V, I_O=120 mA
Collector Saturation Voltage	$V_{CE(sat)}$			0.6	V	V_{CC}=5 V, I_O=120 mA, I_I=0.2 mA
Output Leakage Current	I_{L2}			10	μA	V_{CC}=V_{CE}=5 V, V_I=1.5 V
Input Voltage	V_I			4.0	V	V_{CC}=5 V, V_{CE}=1 V, I_O=120 mA
Forward Voltage (Clamp Diode)	V_F			2.0	V	I_F=120 mA

EQUIVALENT CIRCUIT

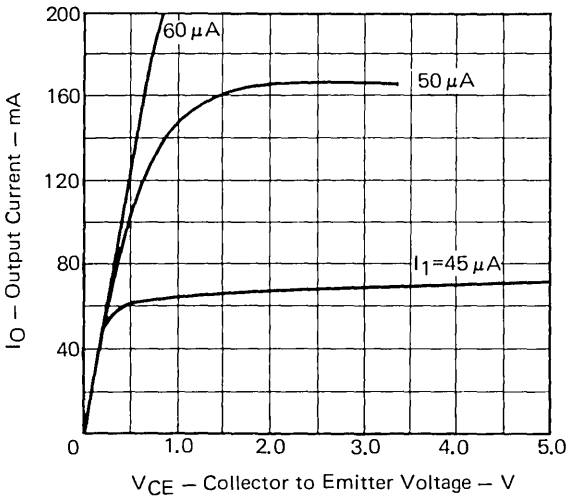


CONNECTION DIAGRAM (Top View)

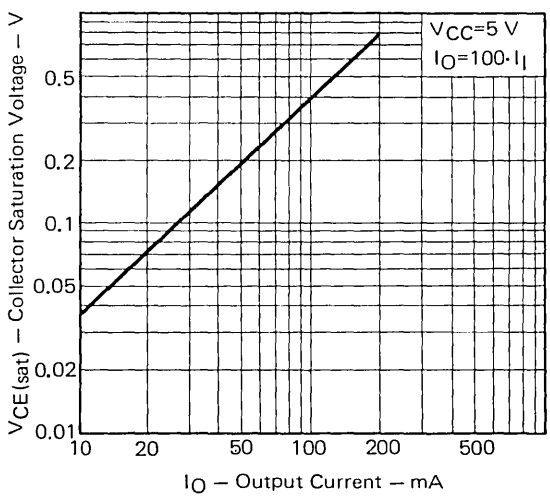


TYPICAL CHARACTERISTICS (Ta = 25 °C)

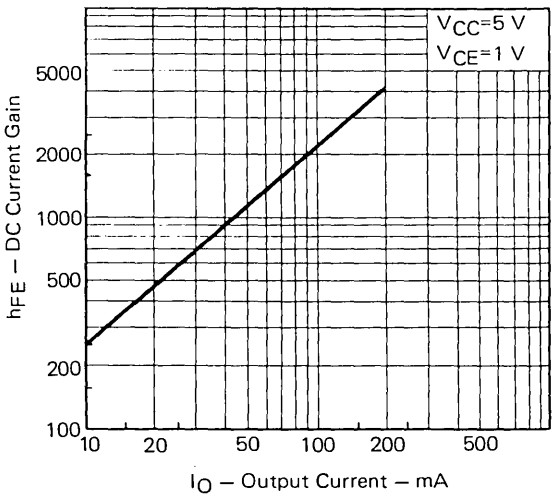
OUTPUT CURRENT vs.
COLLECTOR TO EMITTER VOLTAGE



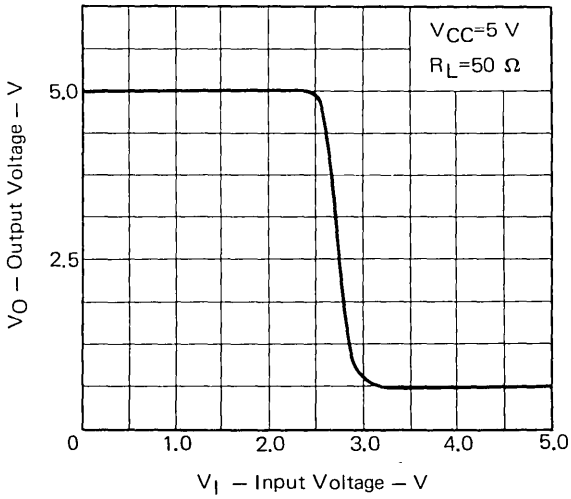
COLLECTOR SATURATION VOLTAGE vs.
OUTPUT CURRENT



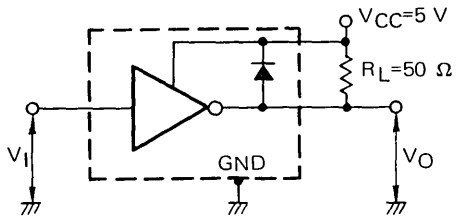
DC CURRENT GAIN vs.
OUTPUT CURRENT



OUTPUT VOLTAGE vs.
INPUT VOLTAGE



VO–VI TEST CIRCUIT



TRANSISTOR ARRAY
μPA80C

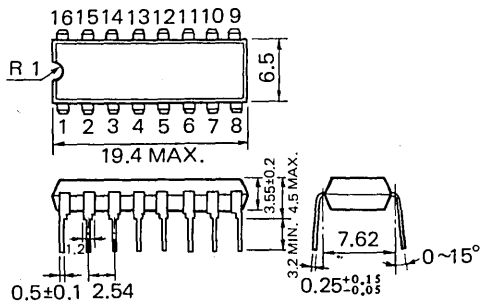
FLUORESCENT INDICATOR PANEL DRIVER
PNP-NPN SILICON EPITAXIAL TRANSISTOR ARRAY

DESCRIPTION

The μPA80C is a monolithic array of seven PNP-NPN structured transistors. This device is especially suited for driving FIP (Fluorescent Indicator Panel).

PACKAGE DIMENSIONS

in millimeters



FEATURES

- High voltage rating V_{SS}: −60 V
- Pull down resistors incorporated
- Base current limiting resistors incorporated
- Package is 16 pin plastic DIP (Dual In-Line Package).

ABSOLUTE MAXIMUM RATINGS

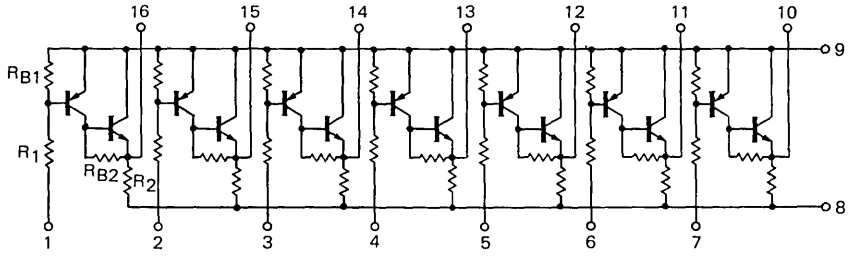
Maximum Voltages and Currents (Ta=25 °C)

Supply Voltage	V_{SS}	−60	V
Input Voltage	V_I	−20	V
Output Current	I_O	50	mA/unit
Maximum Power Dissipation			
Total Power Dissipation	P_d	550	mW
Maximum Temperature			
Storage Temperature	T_{stg}	−40 to +125	°C
Operating Temperature	T_{opt}	−25 to + 75	°C

ELECTRICAL CHARACTERISTICS (Ta=25 °C)

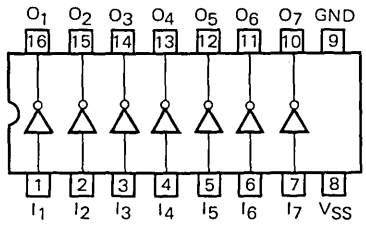
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Leakage Current	I_L			1.0	μA	V_{CE}=50 V
DC Current Gain	h_{FE1}	100	280			V_{CE}=2.0 V, I_O=20 mA
	h_{FE2}	250	450			V_{CE}=2.0 V, I_O=40 mA
Collector Saturation Voltage	$V_{CE(sat)}$		0.95	1.5	V	I_O=20 mA, I_I=0.3 mA
Input Current	I_I			1.0	mA	V_I=−5.0 V

EQUIVALENT CIRCUIT



R_{B1} : 20 kΩ
R_1 : 20 kΩ
R_{B2} : 2 kΩ
R_2 : 100 kΩ

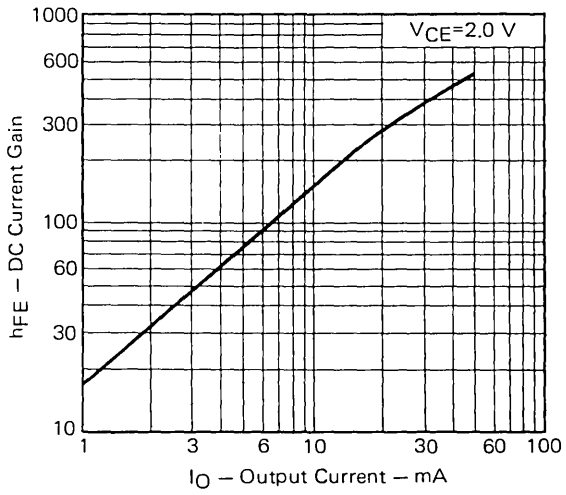
CONNECTION DIAGRAM (Top View)



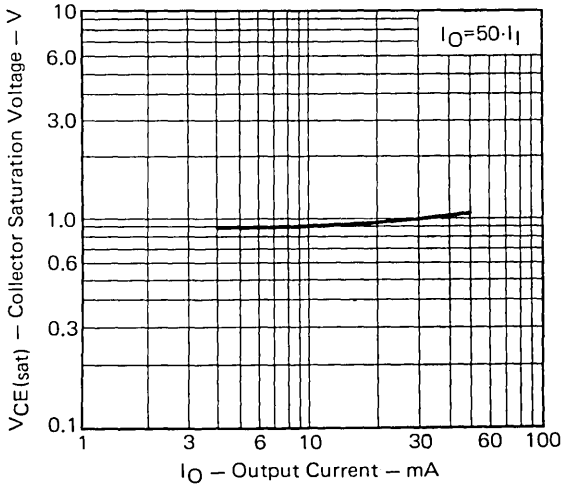
I=Input (Base)
O=Output

TYPICAL CHARACTERISTICS (Ta=25 °C)

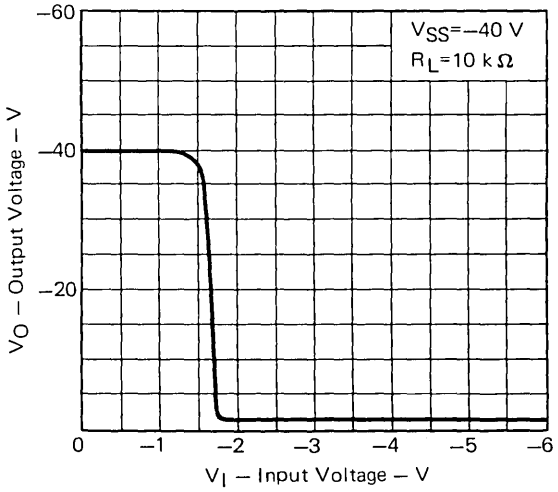
DC CURRENT GAIN vs. OUTPUT CURRENT



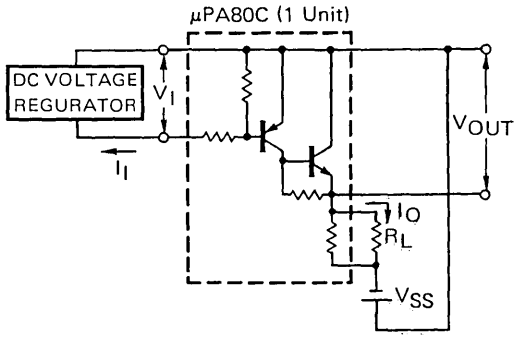
COLLECTOR SATURATION VOLTAGE vs. OUTPUT CURRENT



OUTPUT VOLTAGE vs. INPUT VOLTAGE



V_O–V_I TEST CIRCUIT



TRANSISTOR ARRAY
μPA81C

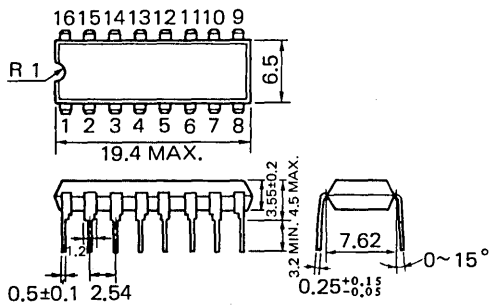
LED,LAMP DRIVER
NPN SILICON EPITAXIAL DARLINGTON TRANSISTOR ARRAY

DESCRIPTION

The μPA81C is a monolithic array of seven darlington transistors. This device is especially suited for driving LED, lamps and printer hummers with MOS output signal.

PACKAGE DIMENSIONS

in millimeters



FEATURES

- High DC current gain.
- High output drive current.
- Package is 16 pin plastic DIP (Dual In-Line Package).

ABSOLUTE MAXIMUM RATINGS

Maximum Voltages and Currents (Ta=25 °C)

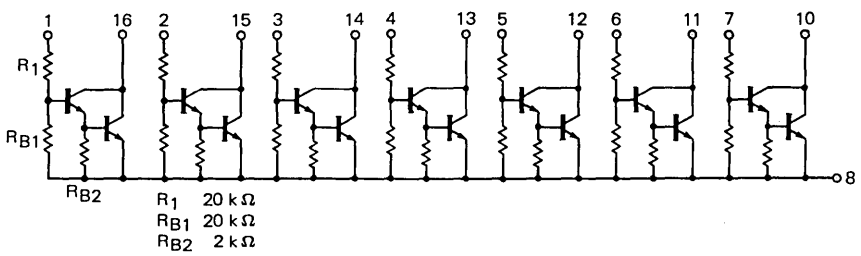
Output Voltage	V_O	45	V
Input Voltage	V_I	45	V
Peak Output Current	I_O*	400	mA/unit
Maximum Power Dissipation			
Total Power Dissipation	Pd	800	mW/package
Maximum Temperature			
Operating Temperature	T_{opt}	−25 to + 75	°C
Storage Temperature	Tstg	−55 to +125	°C

* PW=10 ms, duty cycle ≦10 % (All units turned on)

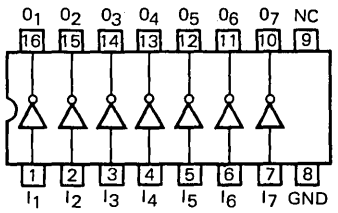
ELECTRICAL CHARACTERISTICS (Ta=25 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Leakage Current	I_L			10	μA	V_{CE}=40 V
DC Current Gain	h_{FE}	1000	2500			V_{CE}=2.5 V, I_O=200 mA
Collector Saturation Voltage	$V_{CE(sat)1}$		0.82	1.2	V	V_I=13 V, I_O=100 mA
Collector Saturation Voltage	$V_{CE(sat)2}$		0.95	1.4	V	V_I=13 V, I_O=200 mA
Collector Saturation Voltage	$V_{CE(sat)3}$		1.2	2.2	V	V_I=13 V, I_O=400 mA
Input Current	I_I			1.5	mA	V_I=17 V, I_O=0

EQUIVALENT CIRCUIT



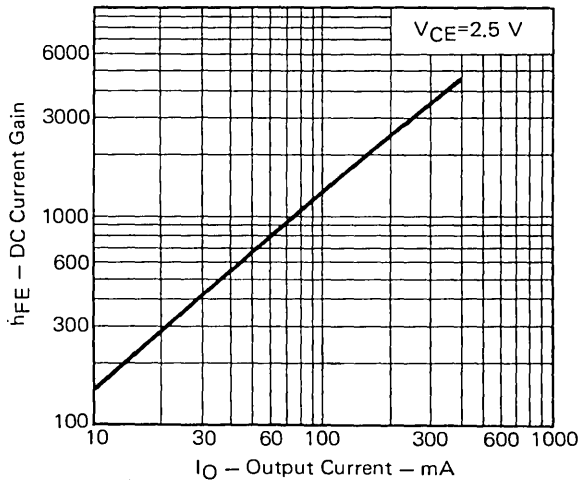
CONNECTION DIAGRAM (Top View)



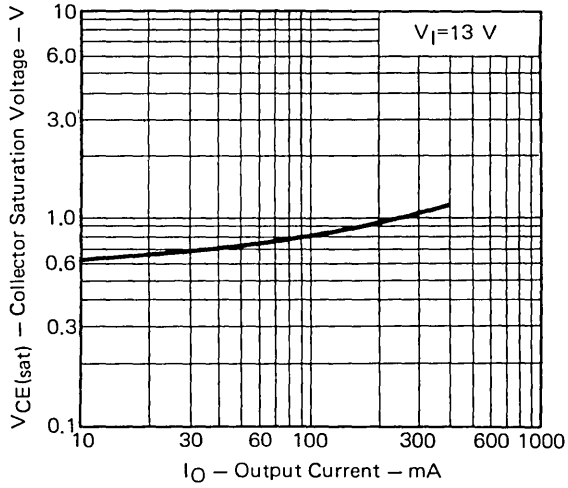
I : Input (Base)
O : Output (Collector)
GND (Common Emitter)

TYPICAL CHARACTERISTICS (Ta=25 °C)

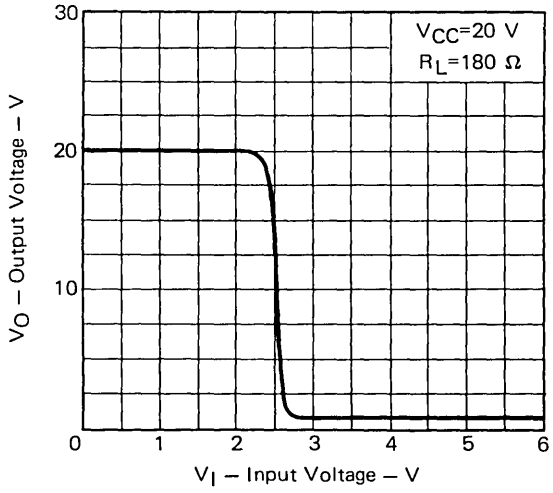
DC CURRENT GAIN vs. OUTPUT CURRENT



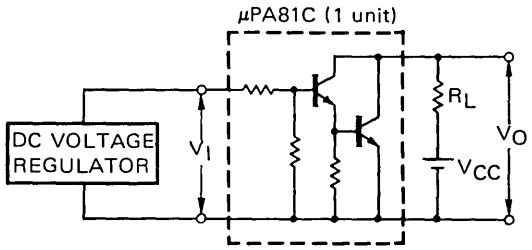
COLLECTOR SATURATION VOLTAGE vs. OUTPUT CURRENT



OUTPUT VOLTAGE vs. INPUT VOLTAGE



V_O–V_I TEST CIRCUIT



TRANSISTOR ARRAYS

μPA2001C, μPA2002C, μPA2003C, μPA2004C

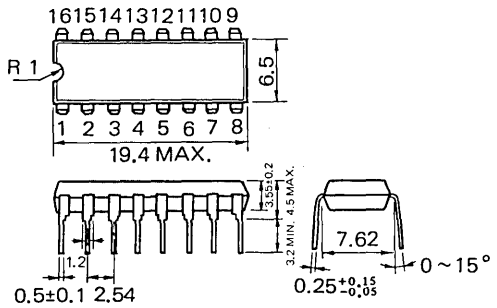
LED, LAMP, RELAY DRIVER
NPN SILICON EPITAXIAL DARLINGTON TRANSISTOR ARRAY

DESCRIPTION

The μPA2001C, 2002C, 2003C and 2004C are monolithic arrays of seven darlington transistors. These devices are especially suited for driving relays, solenoids, LED, lamps, and other devices with up to 0.3 A output current per unit.

PACKAGE DIMENSIONS

in millimeters

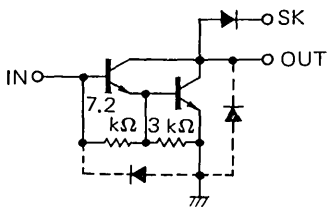


FEATURES

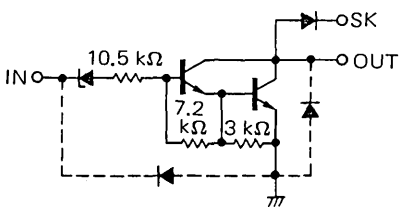
- Transient Protected Outputs
- High DC Current Gain
- High Output Drive Current
- High Output Voltage
- Package is 16 pin PLASTIC DIP.

EQUIVALENT CIRCUIT (1 Unit)

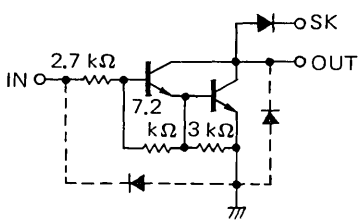
μPA2001C



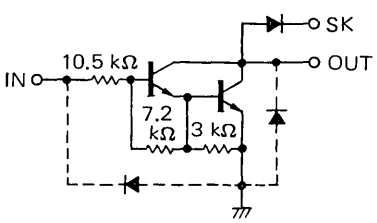
μPA2002C



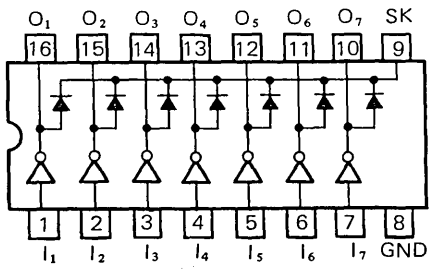
μPA2003C



μPA2004C



CONNECTION DIAGRAM (Top View)



I : Input (Base)
O : Output (Collector)
GND : (Common Emitter)
SK : Surge Killer

ABSOLUTE MAXIMUM RATINGS

Maximum Voltages and Currents (Ta = 25 °C)

Output Voltage	V_O	60	V
Input Voltage (except μPA2001C)	V_I	−0.5 to +30	V
Input Current (only μPA2001C)	I_I	25	mA/unit
Output Current	I_O	500	mA/unit
Output Current	I_O*	2.3	A/package
Reverse Voltage (Clamp Diode)	V_R	60	V
Forward Current (Clamp Diode)	I_F	500	mA/unit

Maximum Power Dissipation

Total Power Dissipation	Pd	900	mW/package
Total Power Dissipation	Pd*	2.5	W/package

Maximum Temperature

Operating Temperature	Topt	−30 to + 75	°C
Storage Temperature	Tstg	−55 to +150	°C

* PW≦20 ms, duty cycle≦10 % (The same current for all units)

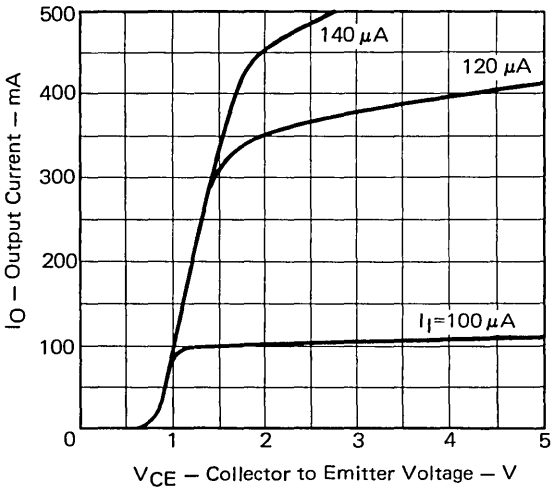
ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output Leakage Current		I_L			10	μA	V_{CE}=50 V
					100	μA	V_{CE}=50 V, Ta=70 °C
DC Current Gain		h_{FE}	1000	2800			V_{CE}=2.0 V, I_O=350 mA
Collector Saturation Voltage		$V_{CE(sat)}$		0.9	1.1	V	I_O=100 mA, I_I=250 μA
				1.0	1.3	V	I_O=200 mA, I_I=350 μA
				1.2	1.6	V	I_O=350 mA, I_I=500 μA
Input Voltage	μPA2002C	V_I			11	V	V_{CE}=2.0 V, I_O=100 mA
					12	V	V_{CE}=2.0 V, I_O=200 mA
					13.5	V	V_{CE}=2.0 V, I_O=350 mA
	μPA2003C				2.0	V	V_{CE}=2.0 V, I_O=100 mA
					2.4	V	V_{CE}=2.0 V, I_O=200 mA
					3.4	V	V_{CE}=2.0 V, I_O=350 mA
	μPA2004C				5.0	V	V_{CE}=2.0 V, I_O=100 mA
					6.0	V	V_{CE}=2.0 V, I_O=200 mA
					8.0	V	V_{CE}=2.0 V, I_O=350 mA
Input Current	μPA2002C	I_I			1.3	mA	V_I=17 V
	μPA2003C				1.35	mA	V_I=3.85 V
	μPA2004C				1.0	mA	V_I=5.0 V
Reverse Current (Clamp Diode)		I_R			50	μA	V_R=50 V
Forward Voltage (Clamp Diode)		V_F			2.0	V	I_F=350 mA
Terminal Capacitance		C_t		15		pF	V_I=0, f=1.0 MHz

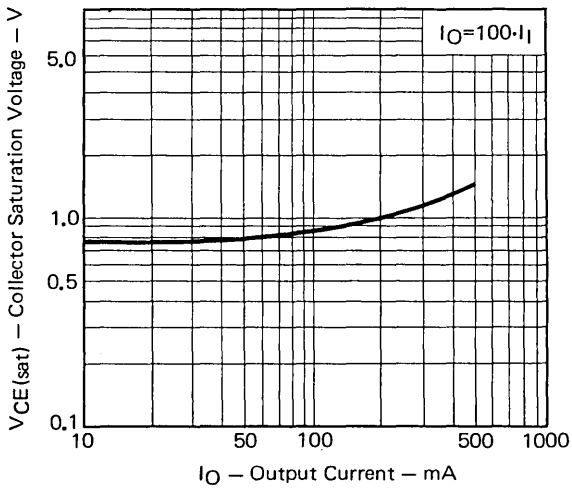
Note: Input Voltage and Current of the μPA2001C depend on external resistor.

TYPICAL CHARACTERISTICS (Ta = 25 °C)

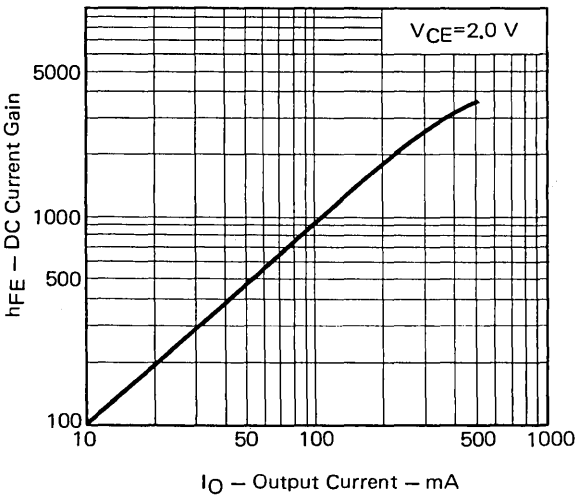
OUTPUT CURRENT vs.
COLLECTOR TO EMITTER VOLTAGE



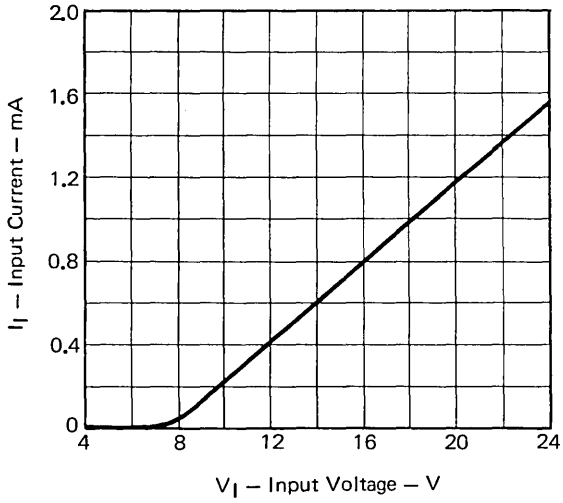
COLLECTOR SATURATION VOLTAGE vs.
OUTPUT CURRENT



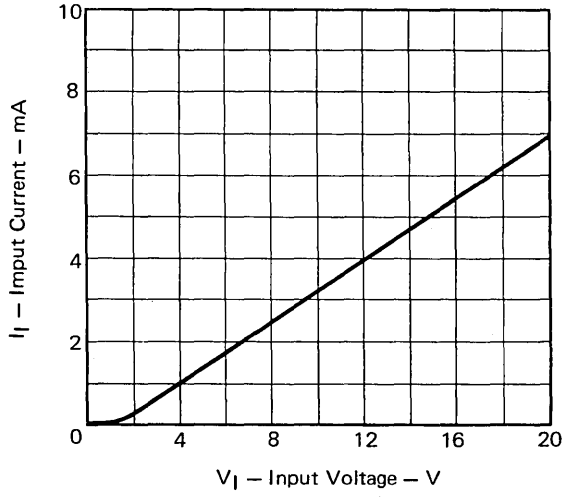
DC CURRENT GAIN vs.
OUTPUT CURRENT



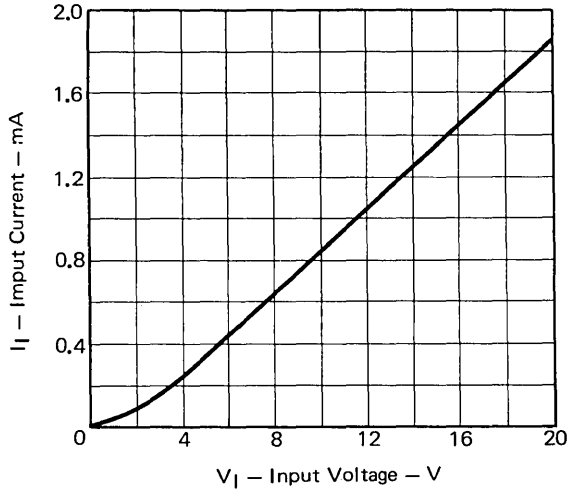
INPUT CURRENT vs.
INPUT VOLTAGE (μPA2002C)



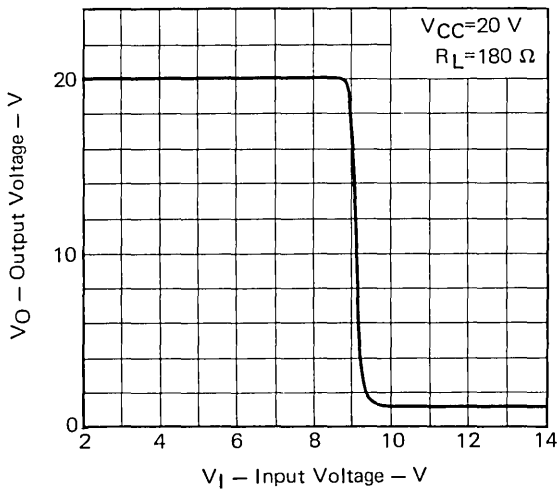
INPUT CURRENT vs.
INPUT VOLTAGE (μPA2003C)



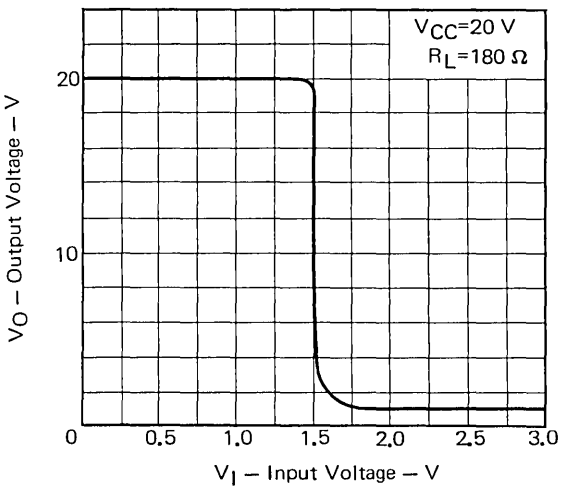
INPUT CURRENT vs.
INPUT VOLTAGE (μPA2004C)



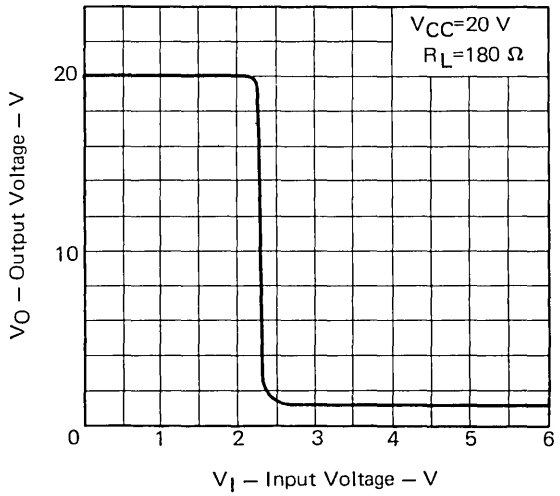
OUTPUT VOLTAGE vs.
INPUT VOLTAGE (μPA2002C)



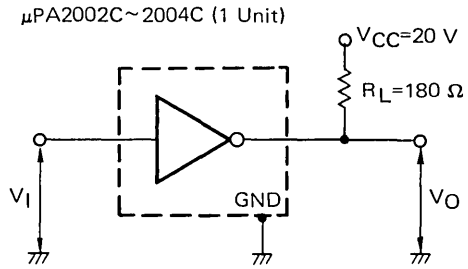
OUTPUT VOLTAGE vs.
INPUT VOLTAGE (μPA2003C)



OUTPUT VOLTAGE vs.
INPUT VOLTAGE (μPA2004C)



V_O–V_I TEST CIRCUIT



INDEX

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1043C

MOTOR CONTROL CIRCUIT
SILICON MONOLITHIC BIPOLAR INTEGRATED CIRCUIT

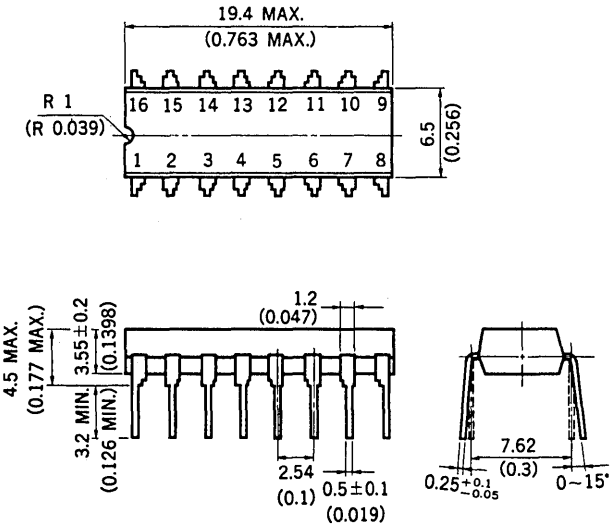
The μPC1043C is a silicon monolithic integrated circuit developed by NEC for Frequency Generator DC Motor speed control of Hi-Fi player and VTR etc.
The package is 16-pin plastic Dual In-Line Package.

FEATURES

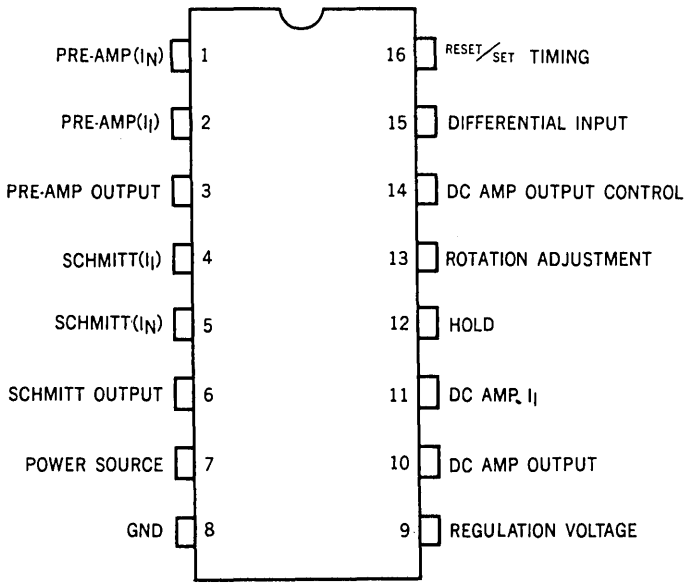
- Operating at wide range supply voltage.
  (V_{CC} = 9 to 28 V)
- Available for wide range FG. Servomotor.
  (f = 20 to 3 000 Hz, v_{in} = 1 to 2 000 m V_{p-p})
- Applicable for any kind of motors by choising the external power transistor.

PACKAGE DIMENSIONS

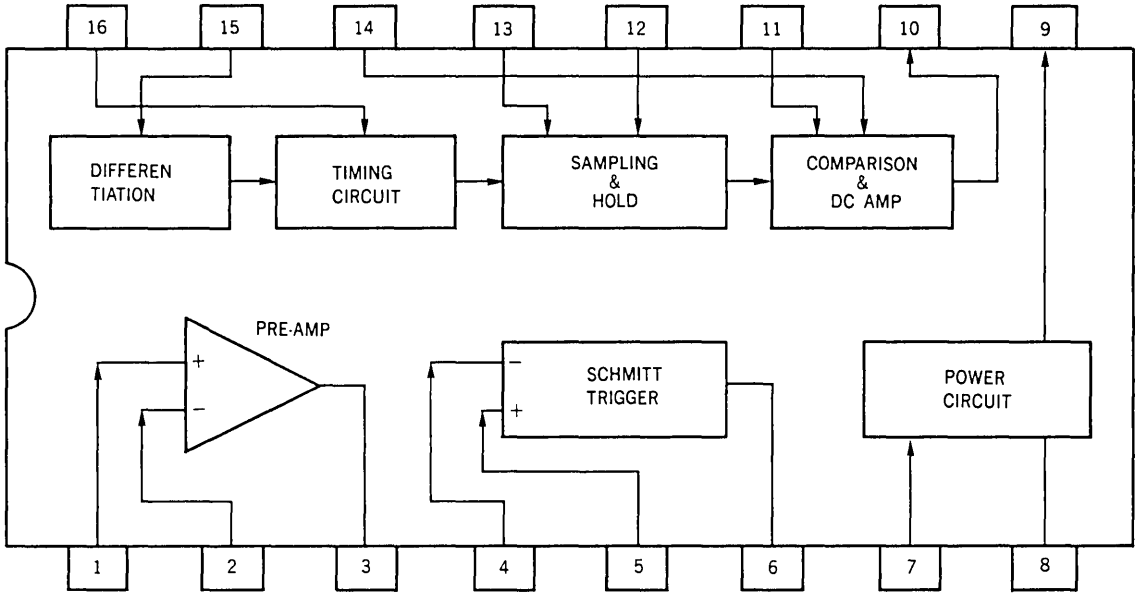
in millimeters (inches)



CONNECTION DIAGRAM (Top View)



BLOCK DIAGRAM (Top View)



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Supply Voltage	V_{CC}	15*	V
Circuit Current	I_{CC}	100	mA
Power Dissipation (Ta = 75 °C)	P_D	350	mW
Operating Temperature Range	T_{opt}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C

* Power source directly applied to No. 7 pin.

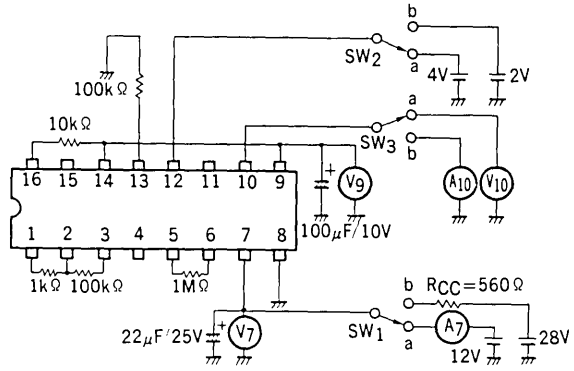
RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage (R_{CC} = 0)	V_{CC1}	9	12	15	V
Supply Voltage (R_{CC} = 560 Ω)	V_{CC2}	19	24	28	V
FG Frequency	f_{ref}	20		3000	Hz
PRE-AMP Voltage Gain	A_V	20		60	dB
Threshold Voltage	V_{TH}	±20		±200	mV
Operating Temperature Range	T_{opt}	−20		+60	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, Ta = 25 °C)

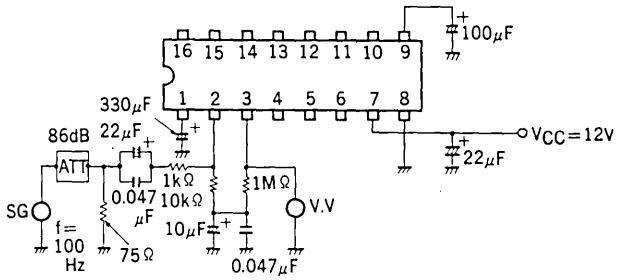
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	I_{CC}	4	7	10	mA	Non-signal input, Output current = 0
Regulation Voltage	V_9	5.1	5.7	6.3	V	Voltage at No. 9 pin
Maximum Output Voltage	$V_{0\ max.}$	3.5	4.25		V	Output Current = 0
Maximum Output Current	$I_{0\ max.}$	8	12	17	mA	Output Voltage = 0
Shunt Regulation Voltage	V_{7ON}	15	16.3	18	V	V_{CC} = 28 V, R_{CC} = 560 Ω
PRE-AMP Voltage Gain	A_{vo}	75	84		dB	f = 100 Hz Test Circuit — 2 S.G. output terminated 700 mVr.m.s.
Rotation Temperature Coefficient	ΔN_A		0	0.02	%/ °C	V_{CC} = 28 V, R_{CC} = 560 Ω Ta = −20 to +60 °C Rotation $N_{max.} - N_{min.}/N(25\ °C)/80\ °C$
Rotation Coefficient Input Voltage	ΔN_V		0	0.02	%/ V	Variation of Rotation at V_{CC} = 19 to 28 V, R_{CC} = 560 Ω
Rotation Drift	ΔN_T		0	0.1	%	Variation of Rotation 10 s to 30 MIN after V_{CC} on at V_{CC} = 24 V, R_{CC} = 560 Ω
Output Ripple Voltage	v_o		20	35	mV_{p-p}	Test Circuit — 4
Schmitt Noise Voltage	V_{TN}		0	0.7	V_{p-p}	Test Circuit — 5
ON Resistance	$R_{Q48\ ON}$		100	300	Ω	Test Circuit — 6

TEST CIRCUIT – 1
(I_{CC}, V_9, $V_{0\ max.}$, $I_{0\ max.}$, $V_{7\ ON}$)



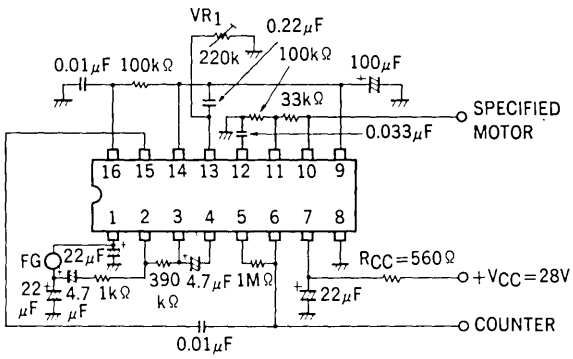
ITEM	SWITCH SW1	SW2	SW3	MEASUREMENT POINT
I_{CC}	a	a	a	A_7
V_9	a	a	a	V_9
$V_{0max.}$	a	b	a	V_{10}
$I_{0max.}$	a	b	b	A_{10}
V_{7ON}	b	a	a	V_7

TEST CIRCUIT – 2 (A_{VO})



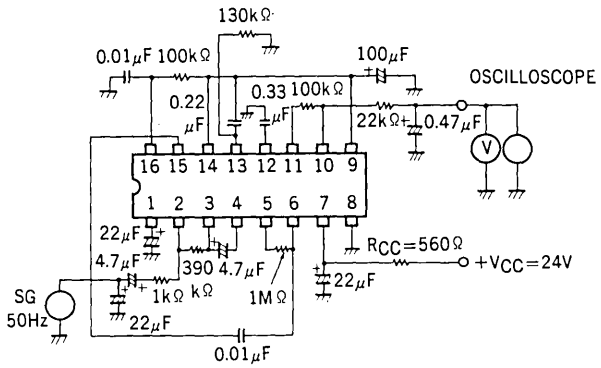
*SG Output Impedance=75 Ω
*ATT Input/Output Impedance=75 Ω

TEST CIRCUIT – 3 (ΔN_A, ΔN_V, ΔN_T)



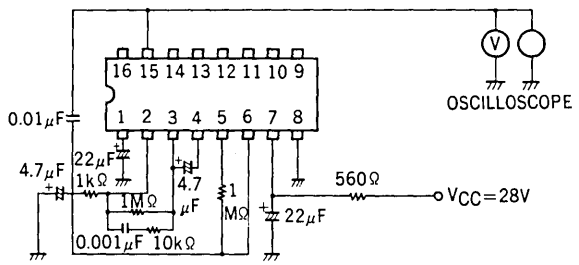
*Adjust VR_1 so that the measured volue by counter becomes 20 ms.

TEST CIRCUIT – 4 (v_o)

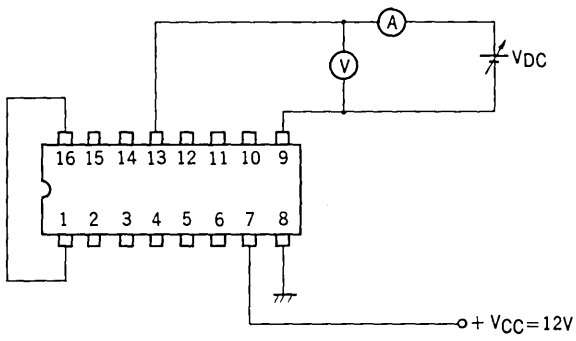


*Adjust SG frequency to obtain 1.4 to 1.5 V DC Voltage on NO. 10 pin, and then measure with oscilloscope.

TEST CIRCUIT – 5 (V_{TN})

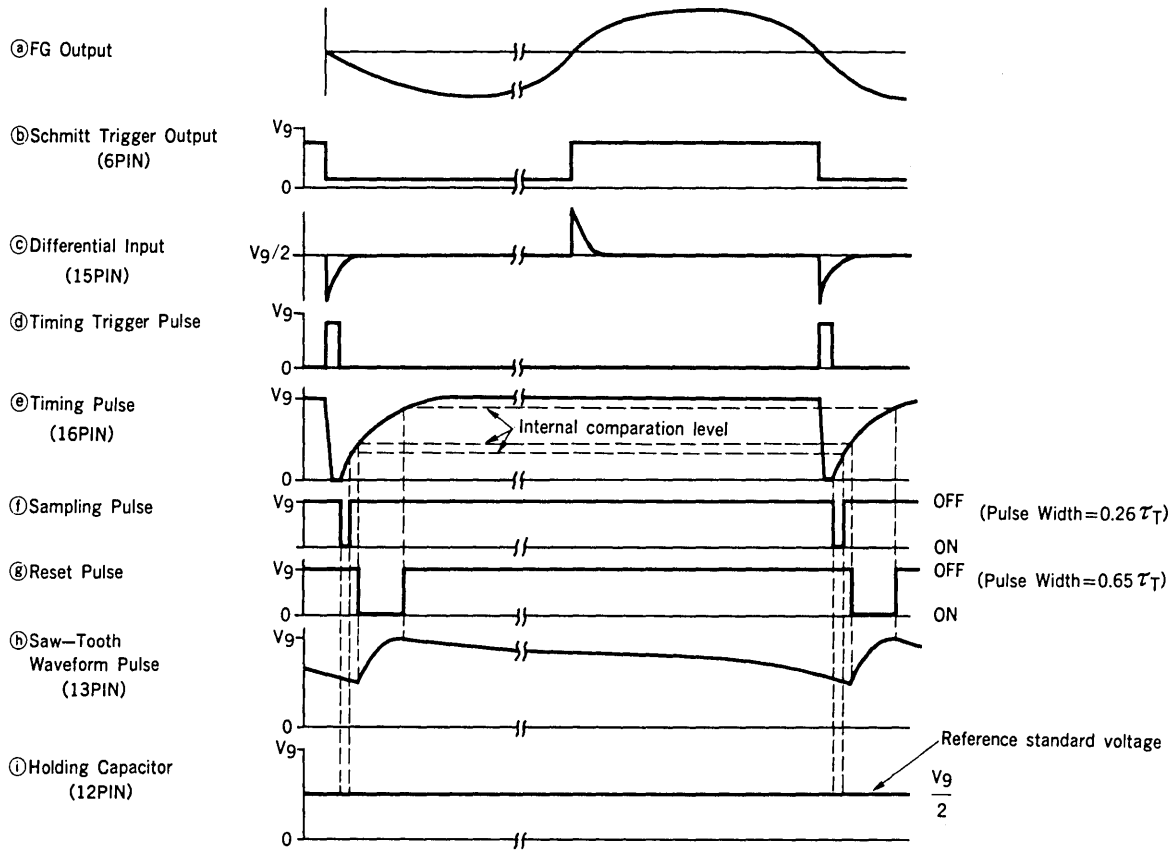


TEST CIRCUIT – 6 ($R_{Q48\ ON}$)

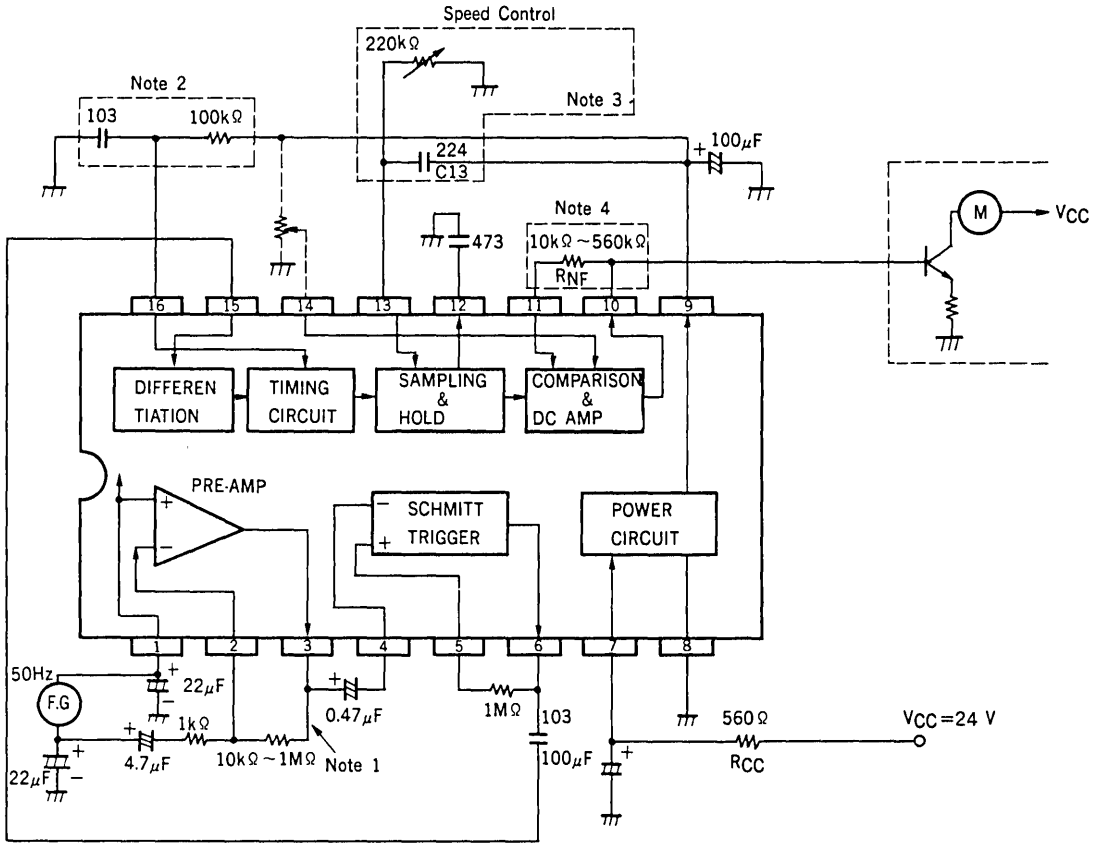


*Adjust V_{DC} to obtain voltage of 1.5 V between NO. 13 and NO. 9 pin, measure current, and calculate by V(1.5 V)/A.

μPC1043C TIMING CHART



APPLICATION CIRCUIT



Note 1: Set preamplifier gain so that about 2 $V_{p\text{-}p}$ voltage is obtained here.

Note 2: Setting timing time constant τ_{16} on No. 16 pin.

$$\tau_{16} = \frac{1}{f_{ref}} \times 0.05 \cdots\cdots \text{(5 \% of FG period)}$$

Note 3: Setting time constant τ_{13} on No. 13 pin for waveform generator.

$$\tau_{13} = \frac{1}{f_{ref} \cdot (-\ell n\ 0.5)} = C_{13} \cdot R_{13}$$

C_{13} can be obtained by the formula.

$$C_{13} \leq \frac{0.65 \cdot \tau_{16}}{3000}$$

Note 4: DC amplifier gain is determined as shown below.

$$A_U = \frac{R_{NF}}{6.8 \times 10^3}$$

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1052V

RECEIVER FOR RADIO-CONTROL SYSTEMS
SILICON MONOLITHIC BIPOLAR INTEGRATED CIRCUIT

DESCRIPTIONS

The μPC1052V is a silicon monolithic integrated circuit developed for receiver for digital-proportional radio-control systems.

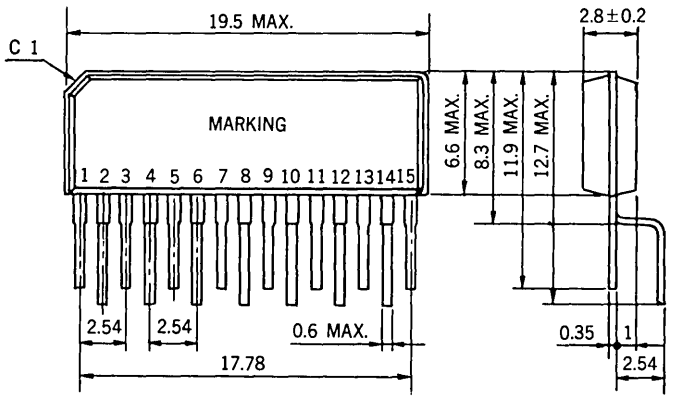
Included in this device is mixer, oscillator, detector, and comparator.

FEATURES

- Operating at wide range supply voltage (V_{CC}=4.2 to 10.5 V)
- Wide AGC range.
- Internal regulation voltage circuit.
- Reduction of the occupation of mounting area in P.W. Board and hand-insertion time, due to the external shape of the V-DIP.

PACKAGE DIMENSIONS

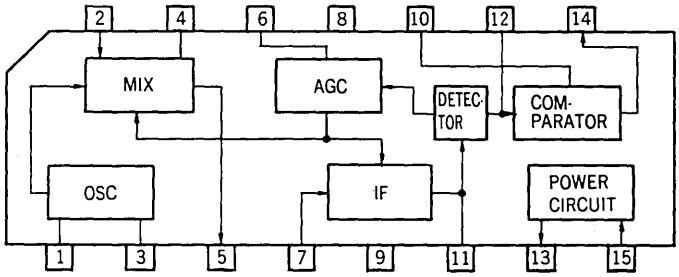
(in millimeters)



CONNECTION DIAGRAM

1.	X tal	2.	MIX. IN
3.	OSC	4.	BY-PASS
5.	MIX. OUT	6.	AGC
7.	IF IN	8.	GND
9.	GND	10.	BY-PASS
11.	IF OUT	12.	BY-PASS
13.	V_R	14.	OUTPUT
15.	V_{CC}		

BLOCK DIAGRAM (Top View)



ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Supply Voltage	V_{CC}	12	V
Power Dissipation	P_D	400	mW
Operating Temperature Range	T_{opt}	−10 to +50	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C

RECOMMENDED OPERATING CONDITION (T_a=25 °C)

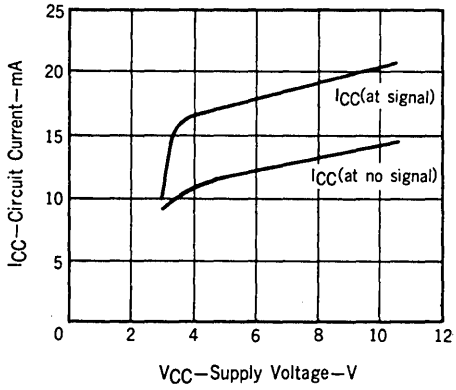
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	4.2	9.0	10.5	V

ELECTRICAL CHARACTERISTICS (V_{CC}=9.0 V, T_a=25 °C)

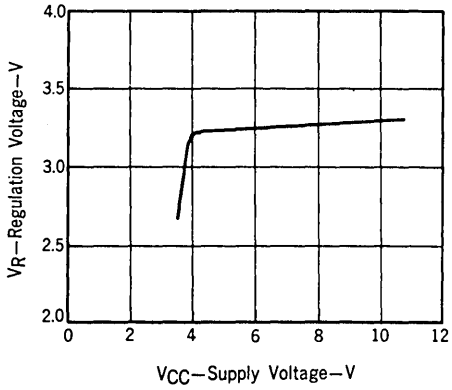
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	I_{CC}	10	14.5	19	mA	At no signal
Maximum Sensitivity	M.S.	22	32	42	dBμV	Output pulse width coefficient = 10 μs
Maximum Sensitivity Coefficient	ΔM.S.		−1	−3	dB	V_{CC}=9 V → 4 V
Output Pulse Width Coefficient (at Large Input Voltage)	ΔP_W		3	6	μs	V_{IN}=110 dBμV
High-Level Output Voltage	V_{OH}	0.7 V_R		V_R	V	R_L=7.5 kΩ
Low-Level Output Voltage	V_{OL}	0		0.4	V	R_L=7.5 kΩ
Regulation Voltage	V_R		3.3		V	At no signal

TYPICAL CHARACTERISTICS (T_a=25 °C)

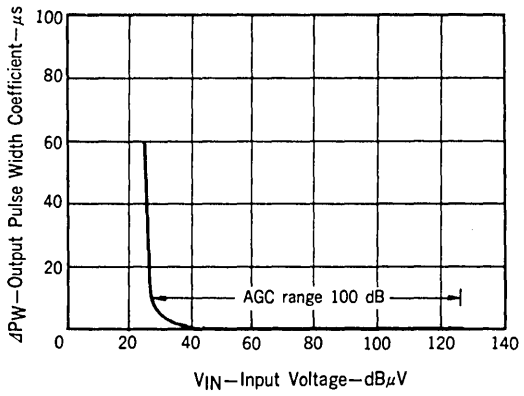
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



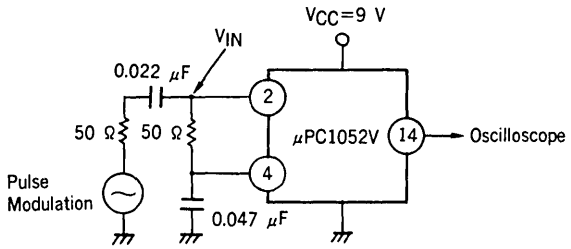
REGULATION VOLTAGE vs. SUPPLY VOLTAGE

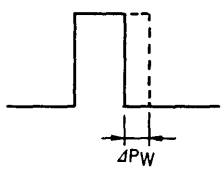


OUTPUT PULSE WIDTH COEFFICIENT vs. INPUT VOLTAGE



TEST CIRCUIT (ΔP_W vs. V_{IN})

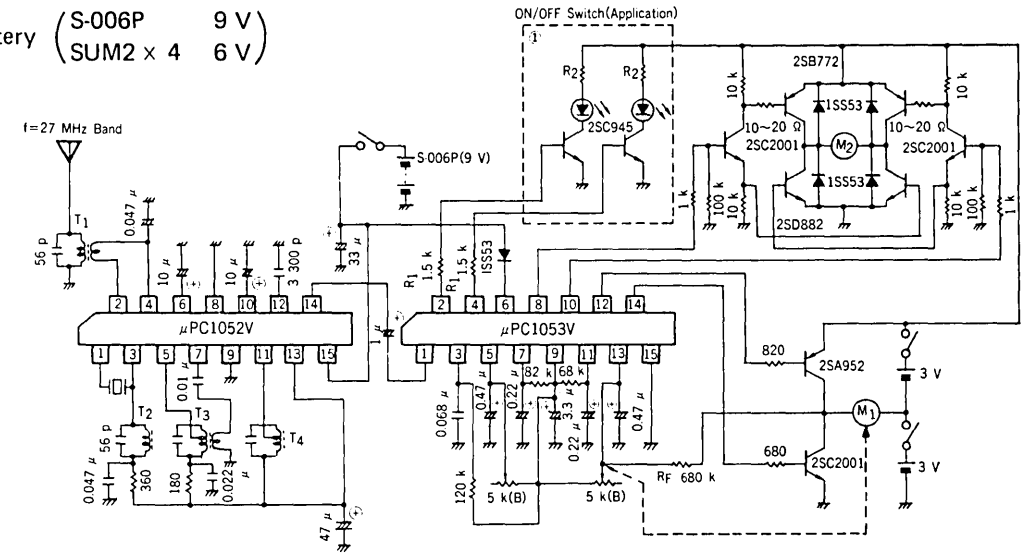


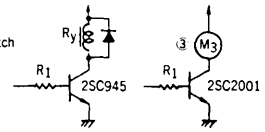


APPLICATION CIRCUIT

(1) RADIO-CONTROL SYSTEM ①

Battery (S-006P 9 V / SUM2 × 4 6 V)



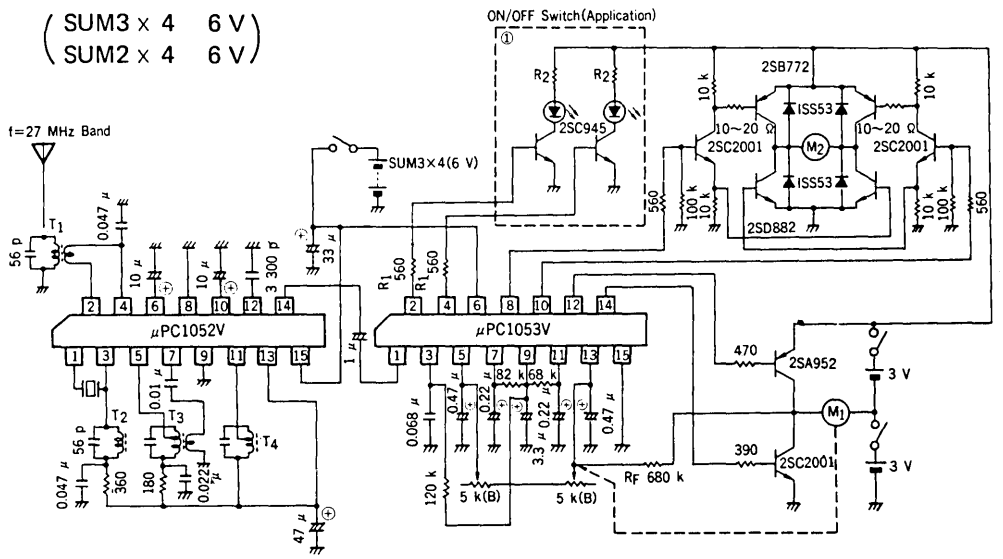


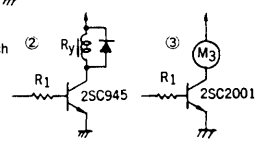
T_1 : TKXN-27185X(TOKO)
T_2 : TKXN-27184Z(TOKO)
T_3 : RMC-162453N9(TOKO)
T_4 : RMC-222633N0(TOKO)

Rf : Feedback Resistance

(2) RADIO-CONTROL SYSTEM ②

Battery (SUM3 × 4 6 V / SUM2 × 4 6 V)





T_1 : TKXN-27185X(TOKO)
T_2 : TKXN-27184Z(TOKO)
T_3 : RMC-162453N9(TOKO)
T_4 : RMC-222633N0(TOKO)

Rf : Feedback Resistance

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1053V

SERVO-AMPLIFIER FOR RADIO-CONTROL SYSTEMS
SILICON MONOLITHIC BIPOLAR INTEGRATED CIRCUIT

DESCRIPTIONS

The μPC1053V is a silicon monolithic integrated circuit developed for servo-amplifier for digital-proportional radio-control systems.

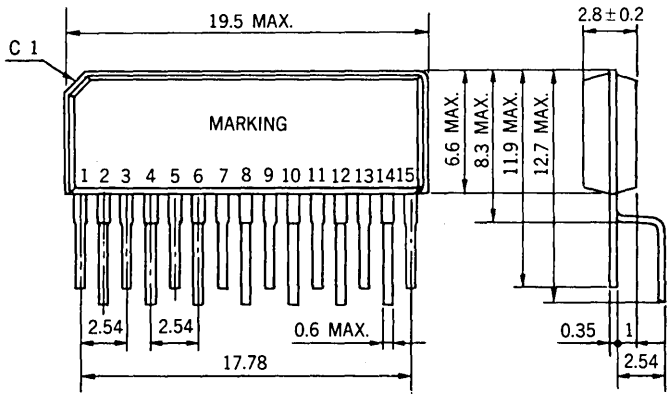
Included in this device is the decoder, gate/latch circuit, and servo-amplifier. It operates stably for a wide range of power supply voltage fluctuation. It can be widely applied to steering control and speed control.

FEATURES

- Internal 2CH servo-circuits and 2CH ON/OFF switch-circuits.
- Operating at wide range supply voltage. (V_{CC}=3.6 to 9.6 V)
- Internal regulation voltage circuit.
- Reduction of the occupation of mounting area in P.W. Board and hand-insertion time, due to the external shape of the V-DIP.

PACKAGE DIMENSIONS

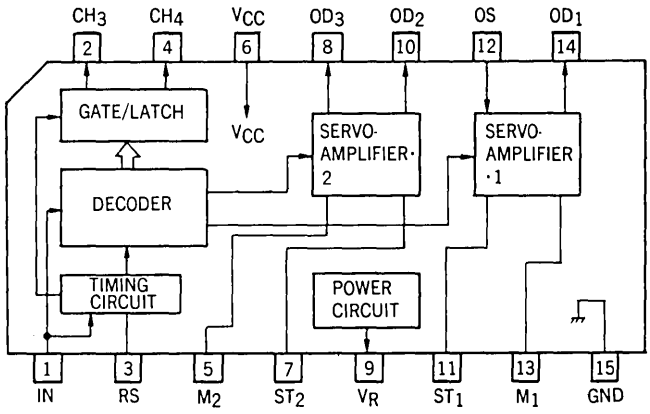
(in millimeters)



CONNECTION DIAGRAM

PIN No.	SYMBOL	CONNECTION
1	IN	Input
2	CH_3	ON/OFF Switch ·3
3	RS	Reset
4	CH_4	ON/OFF Switch ·4
5	M_2	Mono stable multivibrator ·2
6	V_{CC}	Power supply
7	ST_2	Schmitt trigger input ·2
8	OD_3	Drive output ·3
9	V_R	Regulation voltage output
10	OD_2	Drive output ·2
11	ST_1	Schmitt trigger input ·1
12	OS	Sink output
13	M_1	Mono stable multivibrator ·1
14	OD_1	Drive output ·1
15	GND	Ground

BLOCK DIAGRAM (Top View)



ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Supply Voltage	V_{CC}	9.8	V
Output Current ①	I_{OS}, I_{OD1}	20	mA
Output Current ②, ③	I_{OD2}, I_{OD3}	12	mA
ON/OFF Output Current (CH_3, CH_4)	I_3, I_4	12	mA
Power Dissipation	P_D	400	mW
Operating Temperature Range	T_{opt}	−10 to +60	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C

RECOMMENDED OPERATING CONDITION (T_a=25 °C)

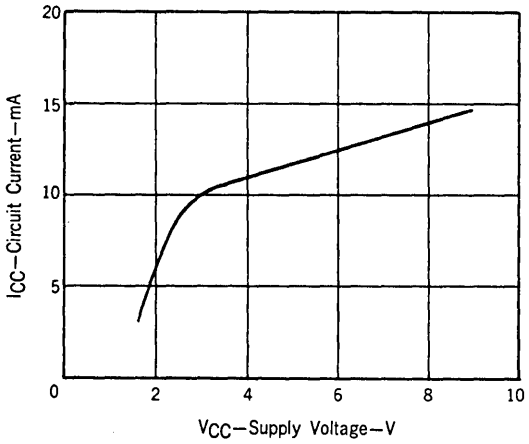
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	3.6	6.0	9.6	V

ELECTRICAL CHARACTERISTICS (V_{CC}=6.0 V, T_a=25 °C)

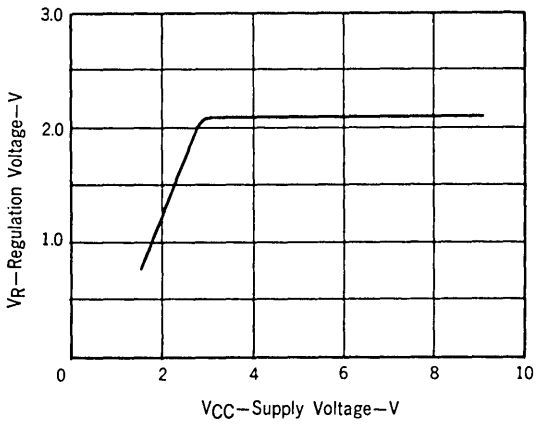
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	I_{CC}		13	24	mA	At no signal
High-Level Input Voltage	V_{IH}	1.5		V_{CC}	V	
Low-Level Input Voltage	V_{IL}	0		0.4	V	
Input Resistance	R_{IN}		11		kΩ	V_{IN}=3.3 V
Sink Output Current ①	I_{OS}	5	10		mA	R_L=470 Ω
Drive Output Current ①	I_{OD1}	5	10		mA	R_L=390 Ω
Drive Output Current ②	I_{OD2}	3	6		mA	R_L=560 Ω
Drive Output Current ③	I_{OD3}	3	6		mA	R_L=560 Ω
Saturation Voltage (CH_3)	$V_{3\ (sat)}$		0.9	2	V	I_O=6 mA
Saturation Voltage (CH_4)	$V_{4\ (sat)}$		0.9	2	V	I_O=6 mA
Regulation Voltage	V_R	1.8	2.1	2.4	V	I_O=0

TYPICAL CHARACTERISTICS (T_a=25 °C)

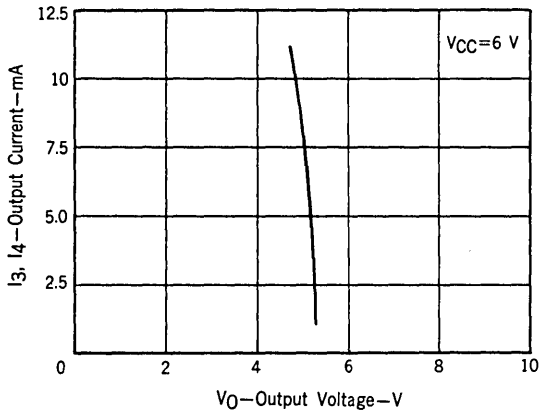
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



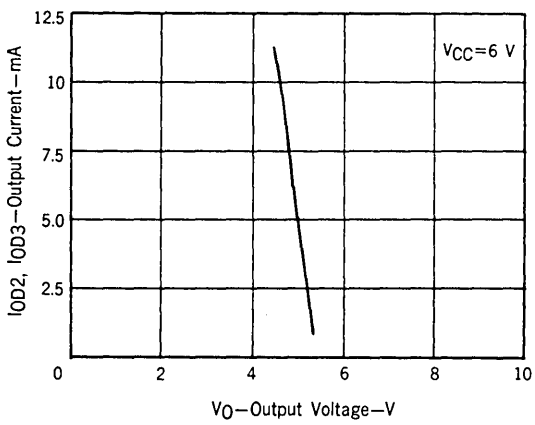
REGULATION VOLTAGE vs. SUPPLY VOLTAGE



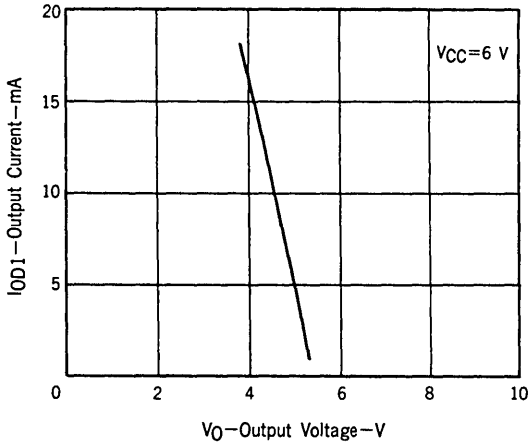
I3, I4 OUTPUT CURRENT vs. OUTPUT VOLTAGE



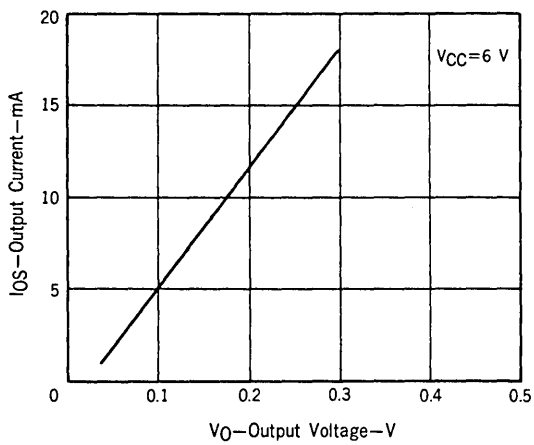
IOD2, IOD3 OUTPUT CURRENT vs. OUTPUT VOLTAGE



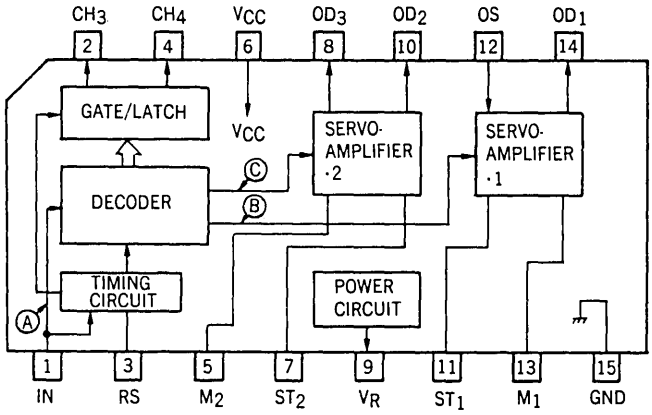
IOD1 OUTPUT CURRENT vs. OUTPUT VOLTAGE

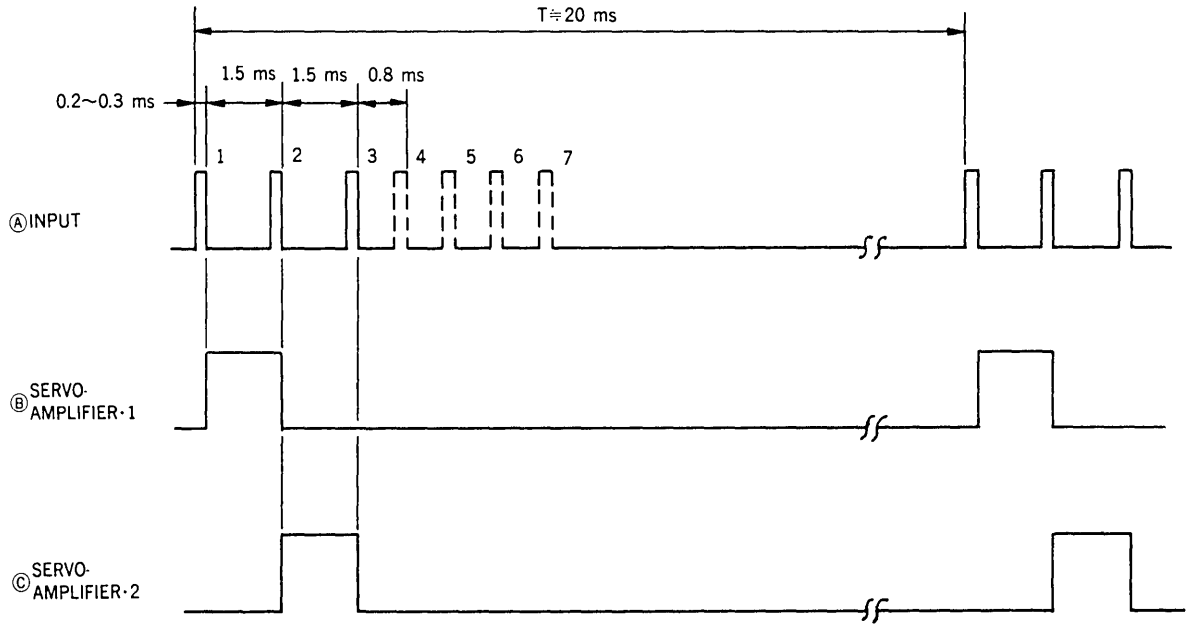


IOS OUTPUT CURRENT vs. OUTPUT VOLTAGE



BLOCK DIAGRAM AND INTERNAL WAVEFORMS (TIMING CHARTS)



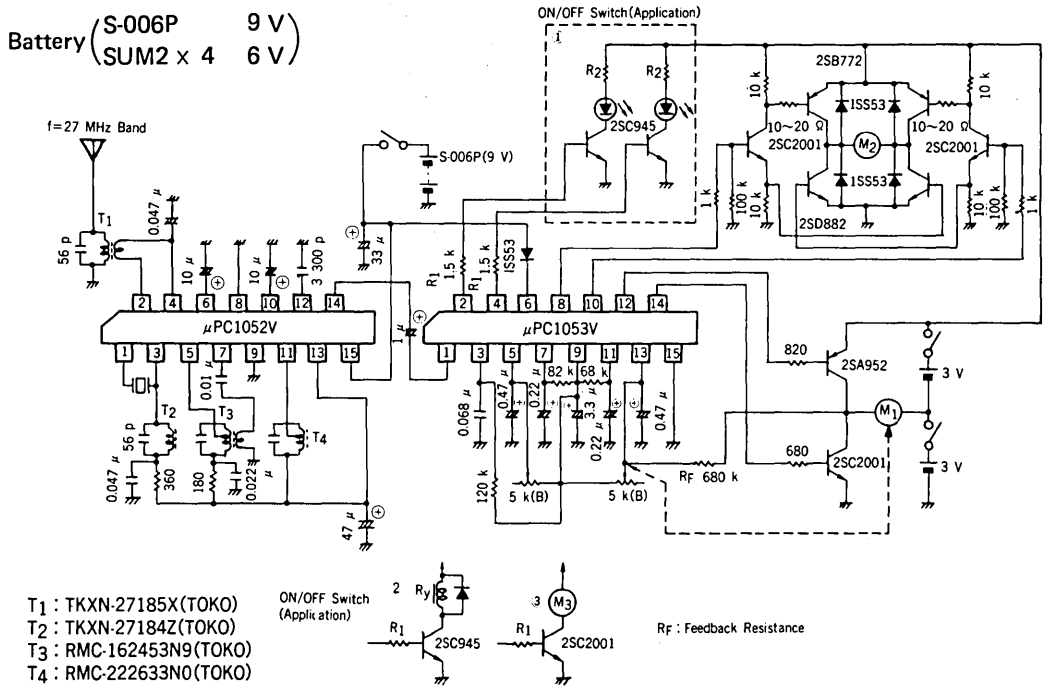


OUTPUT VOLTAGE OF ON/OFF SWITCH (CH_3, CH_4)

Pulse Count	Output Voltage of CH_3	Output Voltage of CH_4
1	Hi	Lo
2	Lo	Hi
3	Hi	Hi
4	Lo	Lo
5	Hi	Lo
6	Lo	Hi
7	Hi	Hi

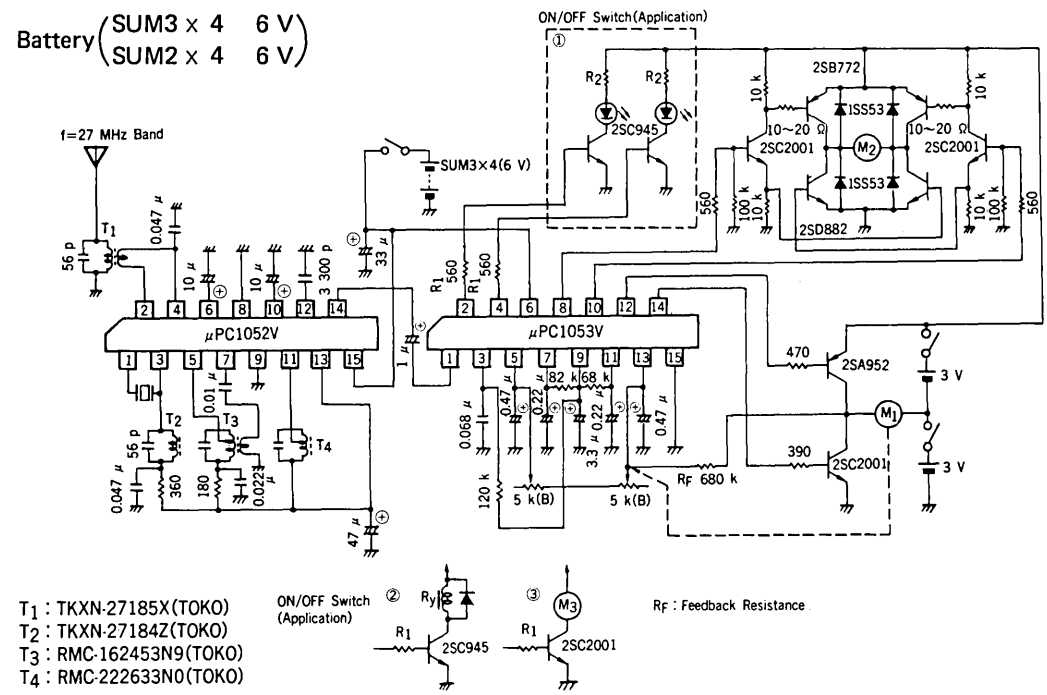
APPLICATION CIRCUIT

(1) RADIO-CONTROL SYSTEM ①



T1 : TKXN-27185X(TOKO)
T2 : TKXN-27184Z(TOKO)
T3 : RMC-162453N9(TOKO)
T4 : RMC-222633N0(TOKO)

(2) RADIO-CONTROL SYSTEM ②



T1 : TKXN-27185X(TOKO)
T2 : TKXN-27184Z(TOKO)
T3 : RMC-162453N9(TOKO)
T4 : RMC-222633N0(TOKO)

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1246C

PREDRIVER FOR 3-PHASES DC BRUSHLESS MOTOR

DESCRIPTION

The μPC1246C is silicon monolithic integrated circuit developed for predriver for 3 phases DC brushless motor.

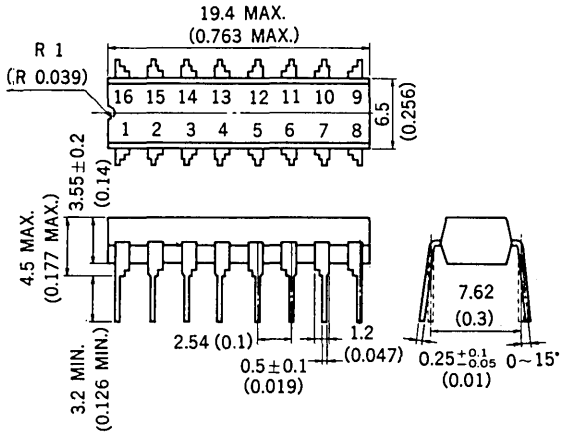
It includes comparators, current switch, rotatory direction switch and drivers in 1 chip. It inputs from hall elements.

FEATURES

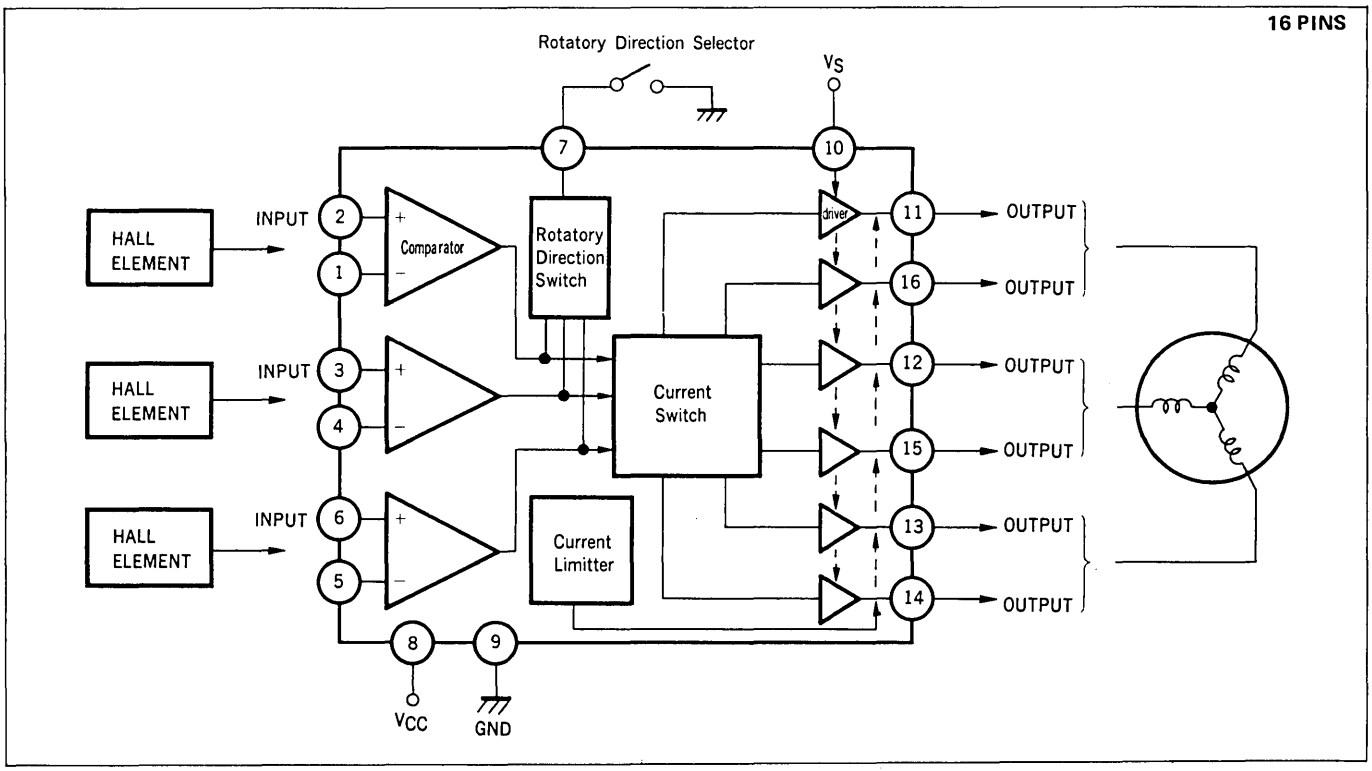
- Current switch.
- Forward/Reverse function.
- Small input/output phase error. −5 ~ 5 deg.
- Low current consumption. I_{CC} = 4.5 mA TYP.

PACKAGE DIMENSIONS

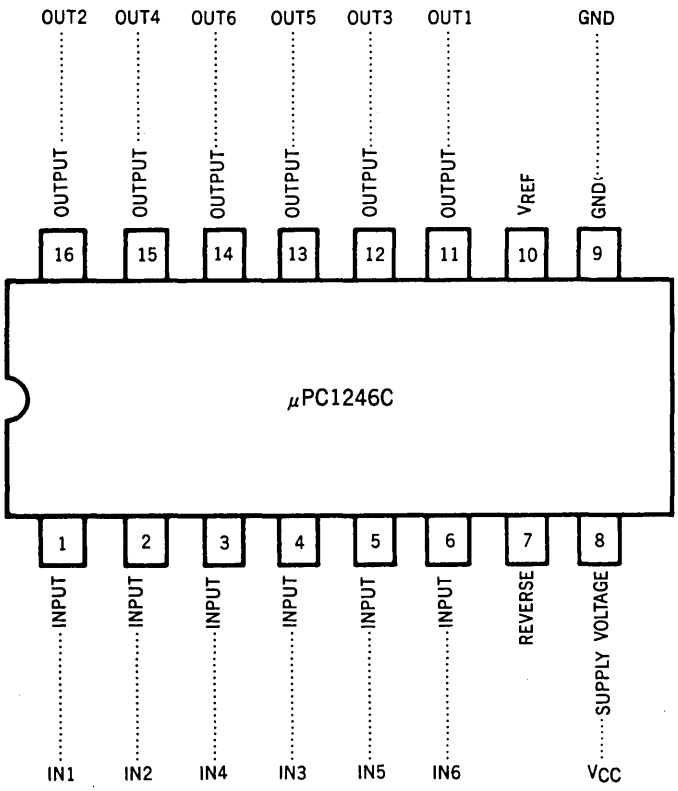
in millimeters (inches)



BLOCK DIAGRAM



CONNECTION DIAGRAM (Top View)



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Supply Voltage	V_{CC}	18	V
Input Voltage to Differential Amp.	V_{ID}	5	V
Common Mode Input Voltage	V_{ICM}	0.3 to V_{CC}	V
Terminal Voltage to V_{REF}	V_{REF}	0 to V_{CC}	V
Reverse Terminal Voltage	V_{REV}	0 to V_{CC}	V
Power Dissipation	P_D Ta = 70 °C	390	mW
Operating Temperature	T_{opt}	−10 to 70	°C
Storage Temperature	T_{stg}	−55 to 125	°C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	9	12	15	V
Common Mode Input Voltage	V_{ICM}	1.5		$V_{CC}-1.5$	V
V_S-Output Current	V_S-I_O	Ref. Fig. 1 ~ 3 Within Area of Obligue Lines			

ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V_{CC} = 12 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Circuit Current	I_{CC}	2	4.5	7.5	mA	V_{REF} = 0
Input/Output Characteristics		−5	0	5	deg	
Input Offset Voltage	V_{OFF}	−4.2	0	4.2	mV	V_{ICM} = 1.5 to 10.5 V
Input Bias Current	I_B	—	50	600	nA	V_{ICM} = 6 V
Propagation Delay Time	T_{pd}	—	3	—	μs	V_I = 5 mV, V_{REF} = 10 V, V_O = 9 V
Output Voltage H (11, 12, 13 PIN)	V_{OH}	8.9	9.3	9.6	V	V_{REF} = 10 V, R_L = 470 Ω
Output Voltage L (14, 15, 16 PIN)	V_{OL}	8.2	8.6	9.0	V	V_{REF} = 8 V, R_L = 470 Ω
Output Leak Current	I_S	—	—	5	μA	Ref. PAGE 916, 918

Fig. 1 OUTPUT CURRENT vs. SERVO VOLTAGE

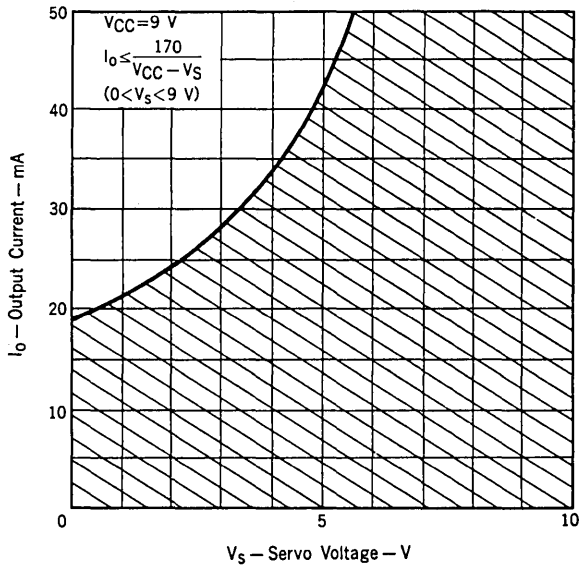


Fig. 2 OUTPUT CURRENT vs. SERVO VOLTAGE

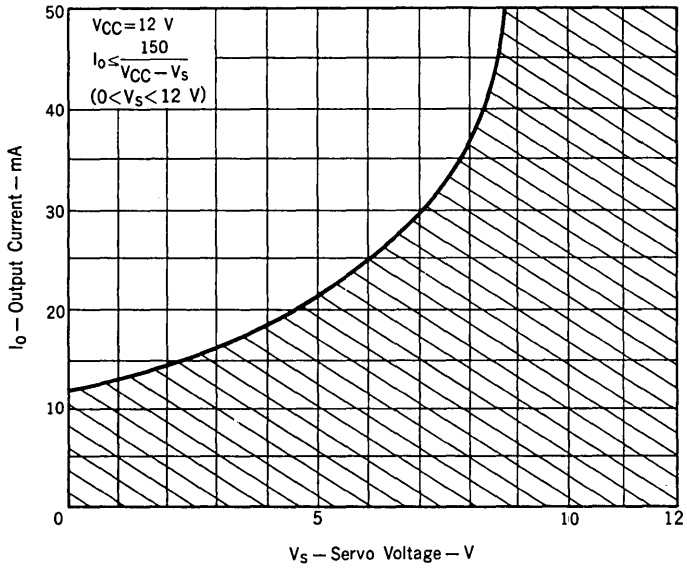
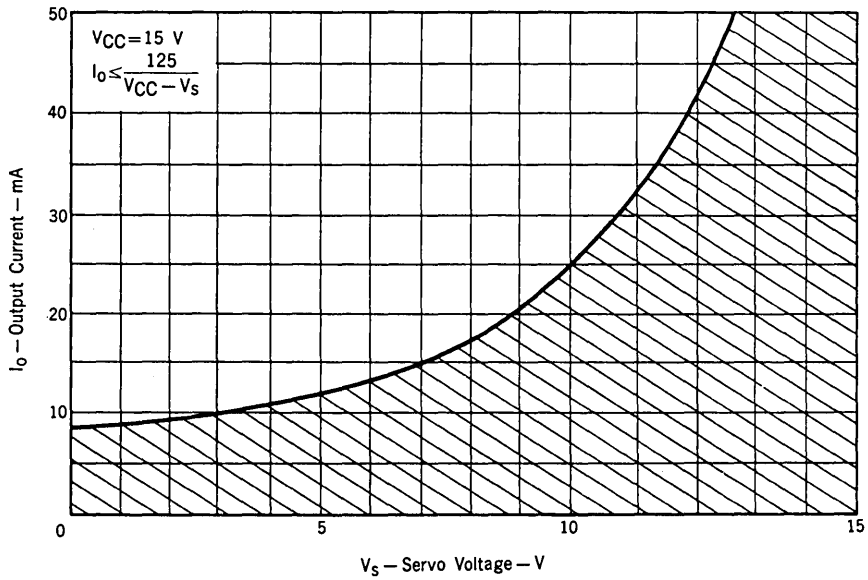
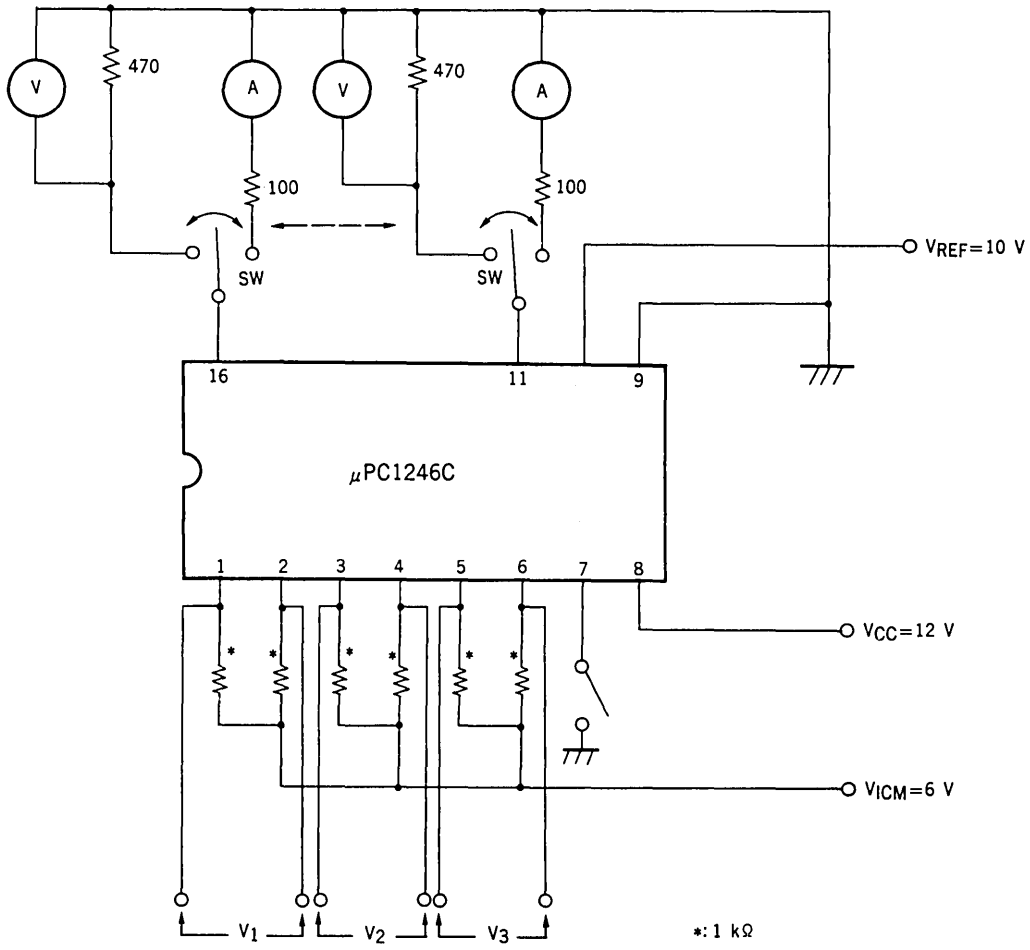


Fig. 3 OUTPUT CURRENT vs. SERVO VOLTAGE



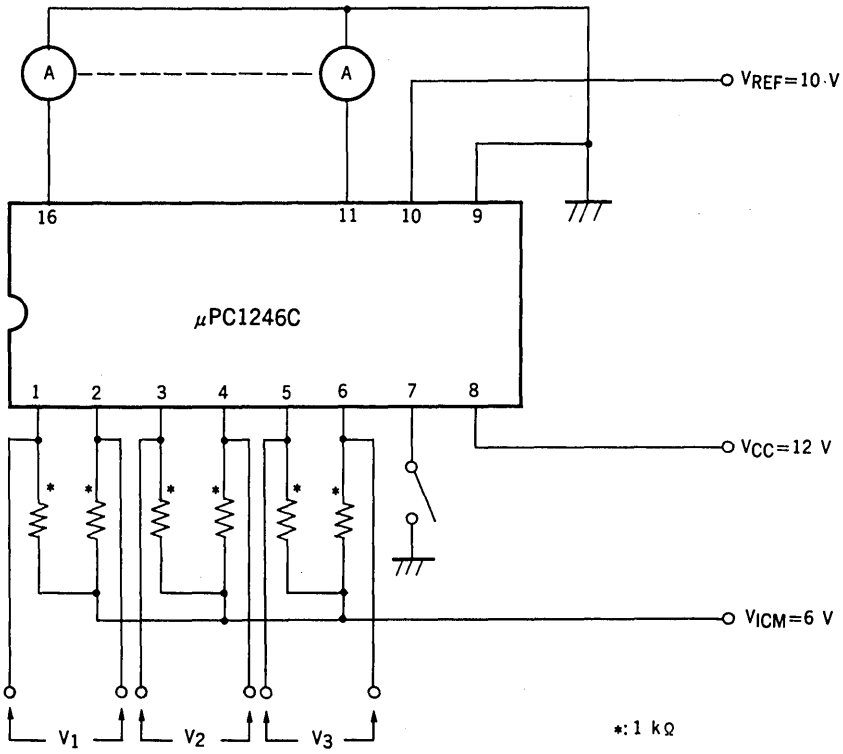
TEST CIRCUIT 1

- INPUT/OUTPUT CHARACTERISTIC
- PROPAGATION DELAY TIME



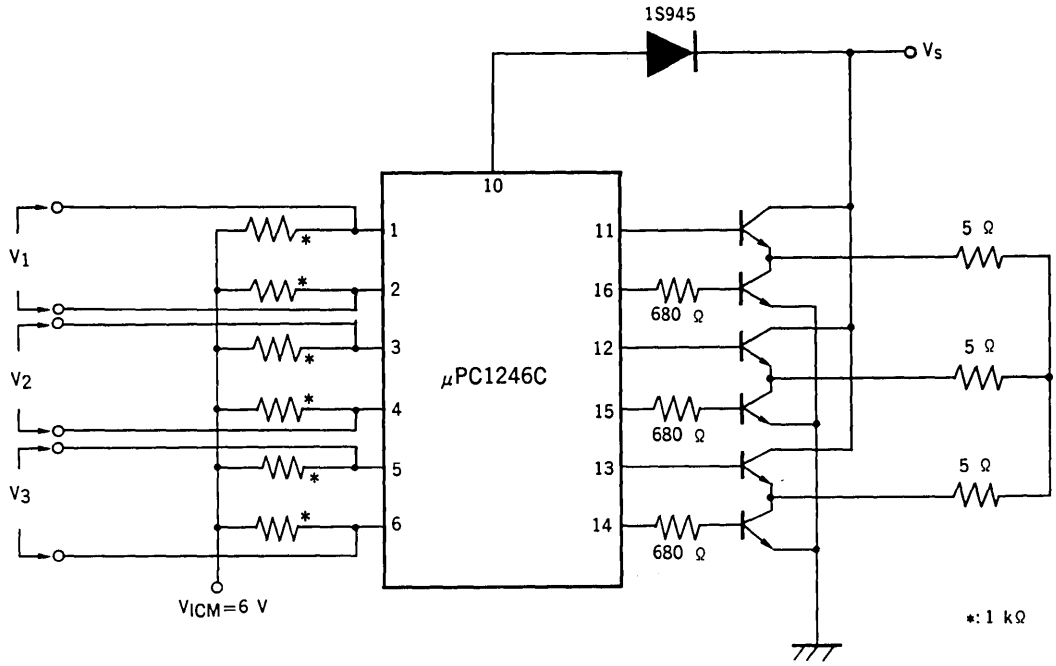
TEST CIRCUIT 2

- OUTPUT LEAKAGE CURRENT I_S

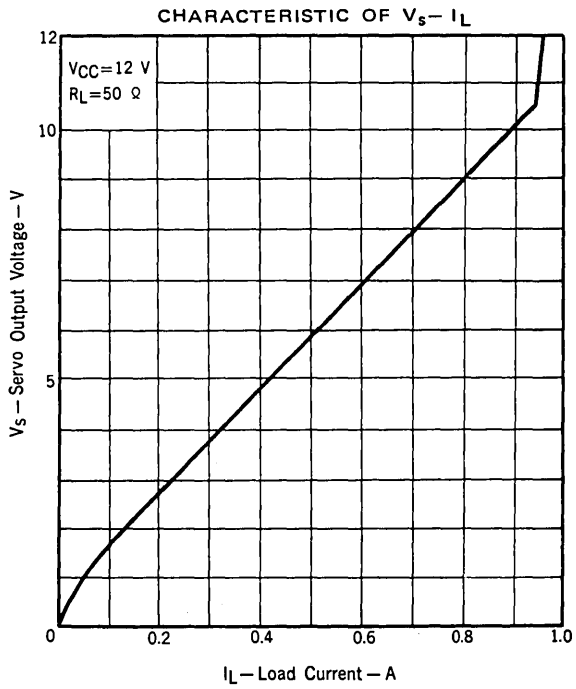


TEST CIRCUIT 3

- CHARACTERISTIC OF
  SERVO VOLTAGE (V_S) – LOAD CURRENT (I_L)



Input Condition is as same as TABLE 1. (See PAGE8)



INPUT CONDITION FOR MEASUREMENT

• INPUT/OUTPUT CHARACTERISTIC

TABLE 1	IN CASE OF 7 PIN OPEN			IN CASE OF 7 PIN SHORT		
TERMINAL OF MEASUREMENT / INPUT CONDITION	V_1	V_2	V_3	V_1	V_2	V_3
11	V_L	V_H		V_H	V_L	
12		V_L	V_H		V_H	V_L
13	V_H		V_L	V_L		V_H
14	V_L		V_H	V_H		V_L
15		V_H	V_L		V_L	V_H
16	V_H	V_L		V_L	V_H	

INPUT LEVEL

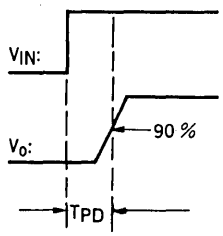
$5\ mV \leq V_H \leq 50\ mV$ OR $-50\ mV \leq V_L \leq 5\ mV$

• PROPAGATION DELAY TIME

TABLE 2	IN CASE OF 7 PIN OPEN			IN CASE OF 7 PIN SHORT		
TERMINAL OF MEASUREMENT / INPUT CONDITION	V_1	V_2	V_3	V_1	V_2	V_3
11	V_{IN}	V_L		V_L	V_{IN}	
12		V_{IN}	V_L		V_L	V_{IN}
13	V_L		V_{IN}	V_{IN}		V_L
14	V_{IN}		V_L	V_L		V_{IN}
15		V_L	V_{IN}		V_{IN}	V_L
16	V_L	V_{IN}		V_{IN}	V_L	

INPUT LEVEL

V_{IN} = 5 mV, f ≤ 10 kHz, Duty 50 % PULSE WAVE $-50\ mV \leq V_L < -5\ mV$



• OUTPUT LEAKAGE CURRENT I_S

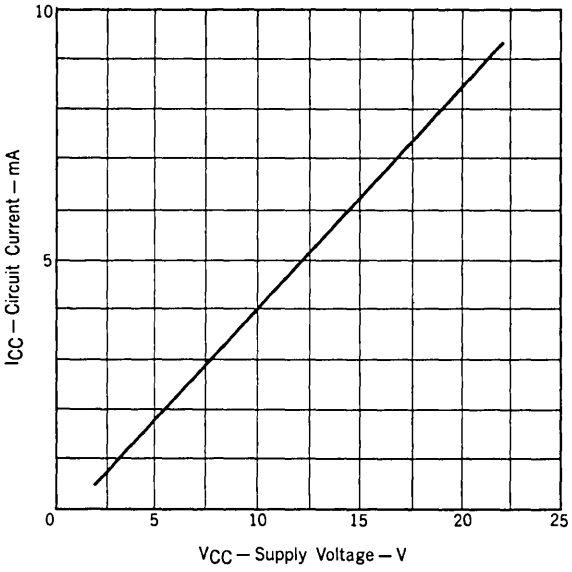
INPUT CONDITION FOR MEASUREMENT

TABLE 3	IN CASE OF 7 PIN OPEN			IN CASE OF 7 PIN SHORT		
TERMINAL OF MEASUREMENT / INPUT CONDITION	V_1	V_2	V_3	V_1	V_2	V_3
11	V_H	V_L		V_L	V_H	
12		V_H	V_L		V_L	V_H
13	V_L		V_H	V_H		V_L
14	V_H		V_L	V_L		V_H
15		V_L	V_H		V_H	V_L
16	V_L	V_H		V_H	V_L	

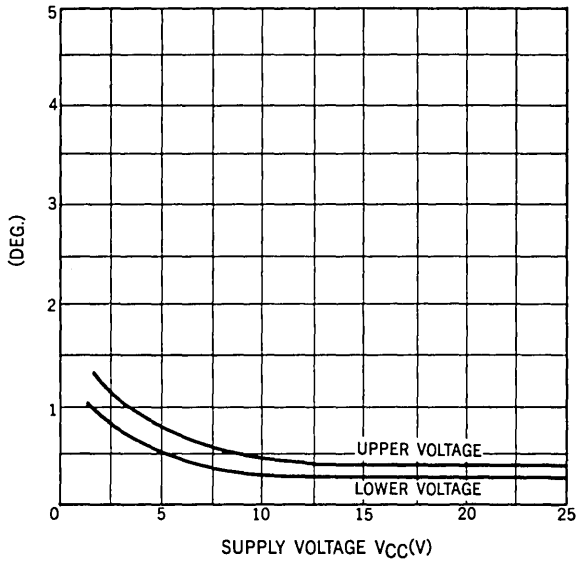
INPUT LEVEL

$-50\ mV \leq V_L \leq -5\ mV$, $5\ mV \leq V_H \leq 50\ mV$

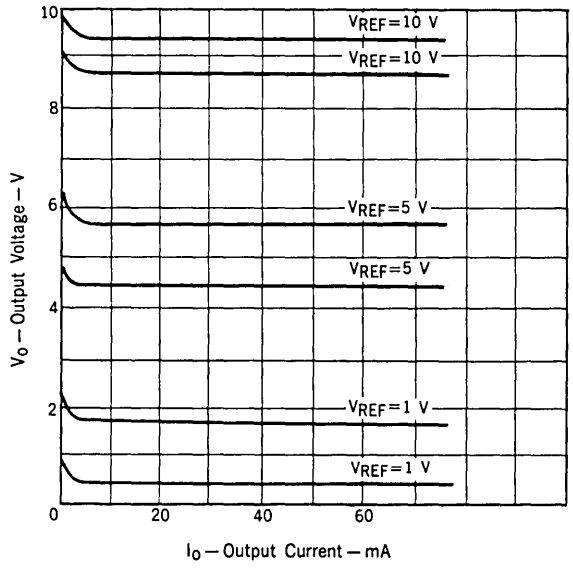
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



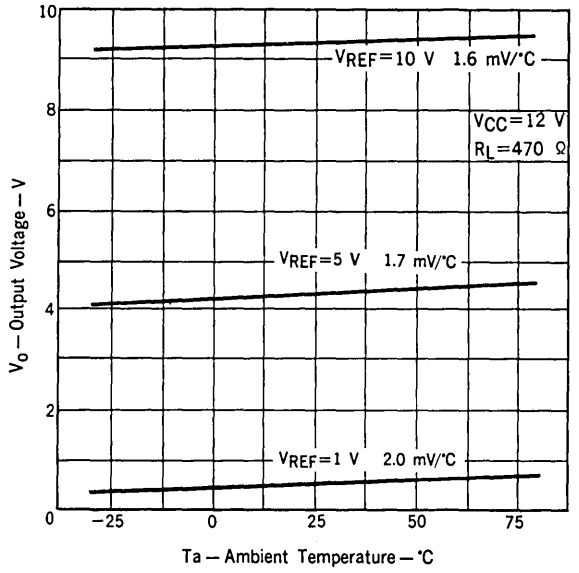
INPUT/OUTPUT CHARACTERISTIC



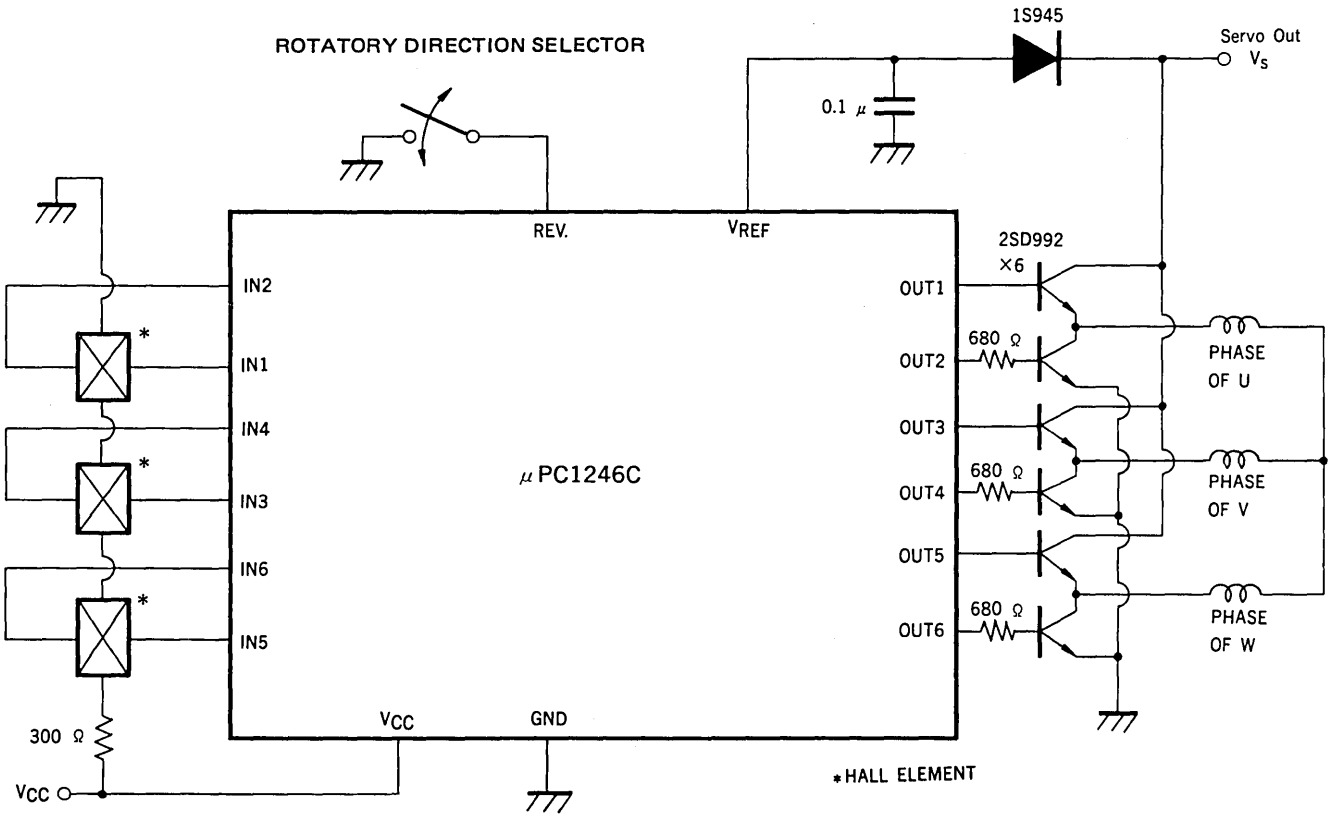
OUTPUT VOLTAGE vs. OUTPUT CURRENT



OUTPUT VOLTAGE vs. AMBIENT TEMPERATURE



APPLICATION



BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1470H

MOTOR SPEED REGULATORS
SILICON MONOLITHIC BIPOLAR INTEGRATED CIRCUIT

DESCRIPTION

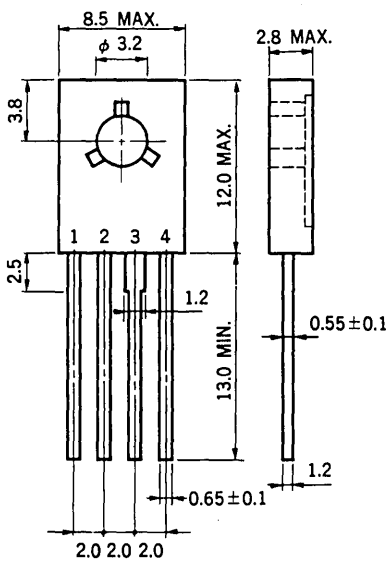
The μPC1470H is a monolithic integrated circuit intended as speed regulators for DC motors of record players, tape and cassette recorders etc. The devices is packaged in a new developed 4-lead quase-TO-126 plastic case.

FEATURES

- Excellent versatility in use.
- High Output current.
- Low Quiescent current.
- Low Reference voltage.
- Excellent parameters stability versus temperature.
- Excellent characteristic at low supply voltage.

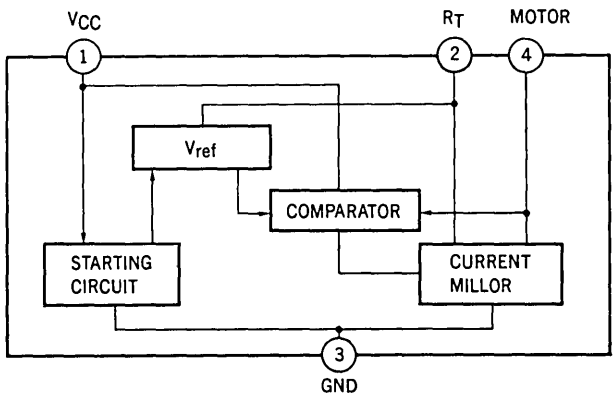
PACKAGE DIMENSIONS

in millimeters



Connection Diagram
1. V_{CC}
2. R_T
3. GND
4. MOTOR

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Supply Voltage	V_{CC}	18	V
Circuit Current	I_4	2*	A
Package Dissipation	P_D	1.2	W
Operating Temperature	Topt	−20 to +75	°C
Storage Temperature	Tstg	−40 to +150	°C

*t ≦ 5s

RECOMMENDED OPERATING CONDITION

Supply Voltage Range	V_{CC}	3.5 to 16	V

ELECTRICAL CHARACTERISTICS (Ta = 25 °C, V_{CC} = 12 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS*	
Reference Voltage	V_{ref}	1.10	1.27	1.40	V	I_4 = 10 mA	Fig. 1
Quiescent Current	I_d	0.5	0.8	1.2	mA	R_M = 180 Ω	Fig. 4
Reflection Coefficient	k	18	20	22		R_{M1} = 44 Ω, R_{M2} = 33 Ω	Fig. 2
Saturation Voltage	$V_{4\ (sat)}$		1.5	2.0	V	V_{CC} = 4.2 V, R_M = 4.4 Ω	Fig. 3
	$\frac{\Delta k}{k}/\Delta V_{CC}$		0.4		%/V	I_4 = 100 mA, V_{CC} = 6.3 ~ 16 V	Fig. 2
Line Regulation	$\frac{\Delta V_{ref}}{V_{ref}}/\Delta V_{CC}$		0.06		%/V	I_4 = 100 mA, V_{CC} = 6.3 ~ 16 V	Fig. 1
	$\frac{\Delta k}{k}/\Delta I_M$		−0.02		%/mA	I_4 = 30 ~ 200 mA	Fig. 2
Load Regulation	$\frac{\Delta V_{ref}}{V_{ref}}/\Delta I_M$		−0.02		%/mA	I_4 = 30 ~ 200 mA	Fig. 1
	$\frac{\Delta k}{k}/\Delta Ta$		0.01		%/°C	I_4 = 100 mA, Ta = −20 ~ +75 °C	Fig. 2
Temperature Coefficient	$\frac{\Delta V_{ref}}{V_{ref}}/\Delta Ta$		0.01		%/°C	I_4 = 100 mA, Ta = −20 ~ +75 °C	Fig. 1

* Pulse Test : PW ≦ 10 ms, Duty Cycle ≦ 2 %

TEST CIRCUIT

Fig. 1

$$\left(V_{ref},\ \frac{\Delta V_{ref}}{V_{ref}}/\Delta V_{CC},\ \frac{\Delta V_{ref}}{V_{ref}}/\Delta I_4,\ \frac{\Delta V_{ref}}{V_{ref}}/\Delta Ta \right)$$

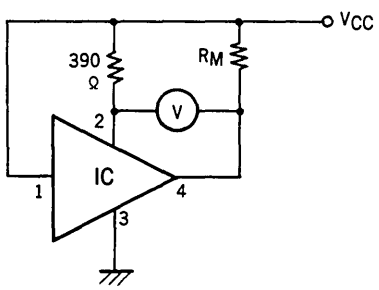
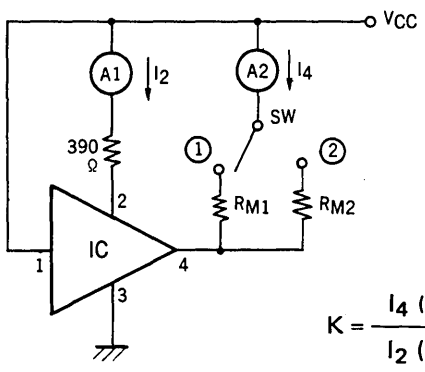


Fig. 2

$$\left(k,\ \frac{\Delta k}{k}/\Delta V_{CC},\ \frac{\Delta k}{k}/\Delta I_4,\ \frac{\Delta k}{k}/\Delta Ta \right)$$



$$K = \frac{I_4\ (SW②) - I_4\ (SW①)}{I_2\ (SW②) - I_2\ (SW①)}$$

Fig. 3

$(V_{4(sat)})$

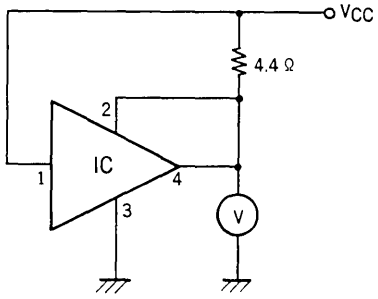
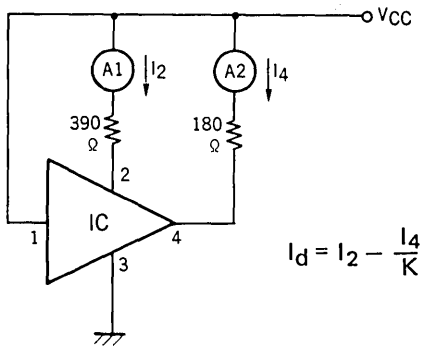


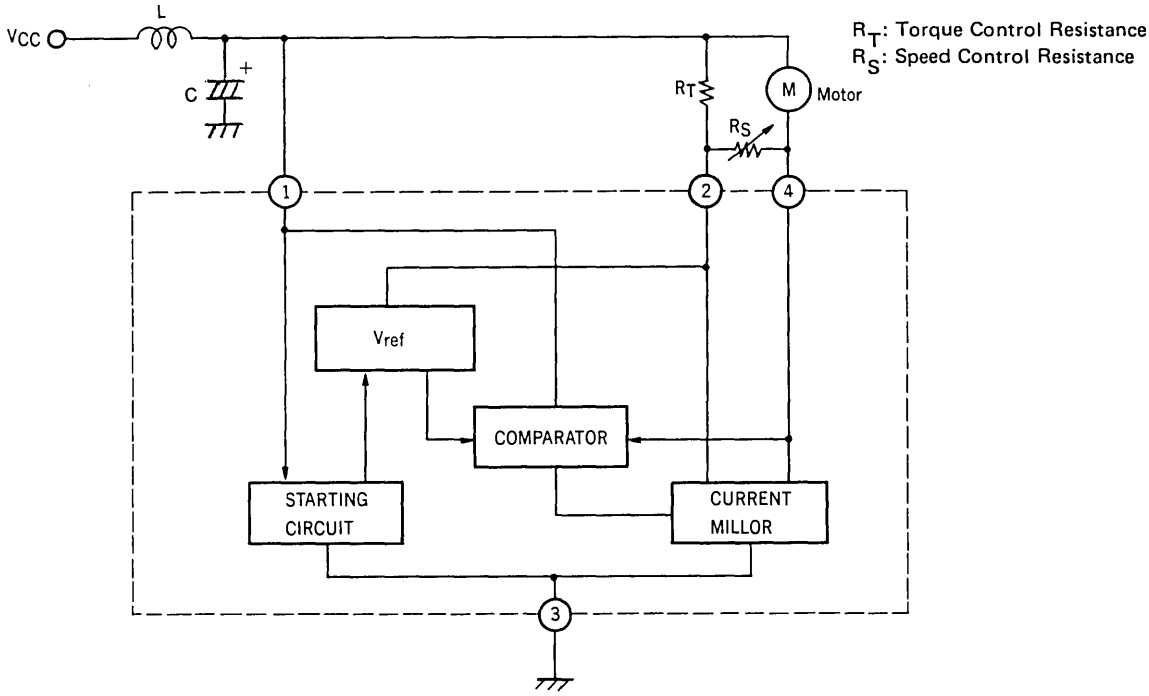
fig. 4

(I_d)



$$I_d = I_2 - \frac{I_4}{K}$$

APPLICATION INFORMATION



R_T: Torque Control Resistance
R_S: Speed Control Resistance

[BASIC EQUATION FOR THE MOTOR]

$$\begin{cases} E_t = V_{ref} + R_T\left(i_2 + \dfrac{V_{ref}}{R_S}\right) \\ i_2 = \dfrac{1}{K} i_4 + i_d \\ i_4 = i_m + \dfrac{V_{ref}}{R_S} \end{cases}$$

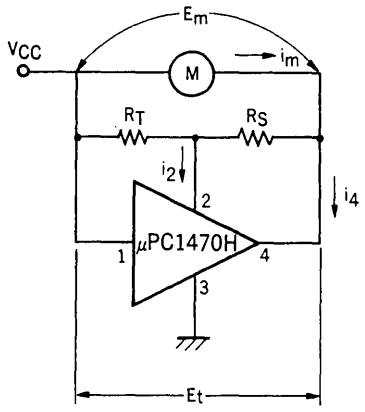
$$E_t = V_{ref} + R_T\left(\frac{1}{K} i_4 + i_d + \frac{V_{ref}}{RS}\right)$$

$$E_t = V_{ref} + R_T\left\{\frac{1}{K}\left(i_m + \frac{V_{ref}}{R_S}\right) + i_d + \frac{V_{ref}}{R_S}\right\}$$

$$E_t = V_{ref}\left\{1 + \frac{R_T}{R_S}\left(1 + \frac{1}{K}\right)\right\} + R_T i_d + \frac{R_T}{K} i_m$$

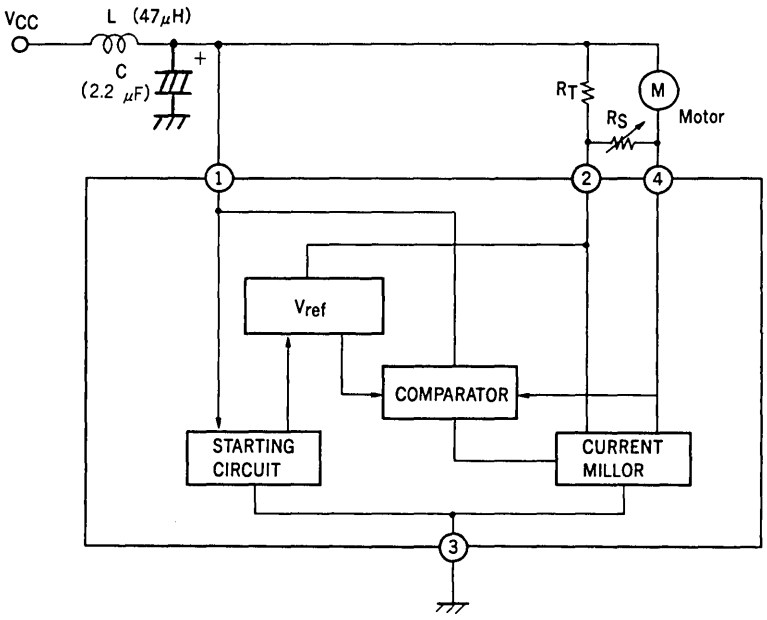
They also give: $E_m = E_o + R_m i_m$

$$\begin{cases} E_o = V_{ref}\left\{1 + \dfrac{R_T}{R_S}\left(1 + \dfrac{1}{K}\right)\right\} + R_T i_d \\ R_m = \dfrac{R_T}{K} \end{cases}$$



E_o : Back Electromotive Force
R_m: Internal Resistance (of the Motor)
K : Reflection Coefficient ($= i_4/i_2$)

APPLICATION CIRCUIT



V_{CC} = 12 V
R_m = 19.5 Ω
R_T = 330 Ω
R_S = 1 kΩ
E_o = 2.3 V
K = 20

Note 1. The motor speed can be adjusted by the variable resistor R_S.

$$R_{S\,min.} = \frac{V_{ref} \cdot R_T}{E_o - V_{ref} - I_d \cdot R_T}$$

Note 2. If $R_{T\,max.} > K \cdot R_{m\,min.}$ instability of the motor may occur.

INDEX

APPLICATION OF ELECTRONICALLY TUNED AM TUNER FOR MOBILE RADIO μPC1215V

1. INTRODUCTION

μPC1215V is a bipolar integrated circuit developed for AM tuners of electronically tuned car radio or car stereo. The circuit contains a mixer, an oscillator, an oscillator buffer, IF amplifiers, a detector and AGC circuits as well as a station detector (SD) that issues seek stop signal during station search. With a varactor tuned FET amplifier provided externally, an electronically tuned car-radio can be formed.

Because it is packed in a newly developed 19-Pin V-DIP, the area needed for loading is small and thus an improved manoeuverability and the prevention of misfitting trouble can be expected.

2. FEATURES

- Suitable for an electronic tuning with a varactor diode.
- Low level of oscillation that can minimize the tracking error due to the varactor diode non-linearity.
- Provided with a large amplitude oscillation output terminal for PLL synthesizer.
- Containing a station detector for the output of auto-scan-seek stop signal.
- Containing a detector circuit and a small number of external components needed.
- Packaged small.

3. BLOCK DIAGRAM

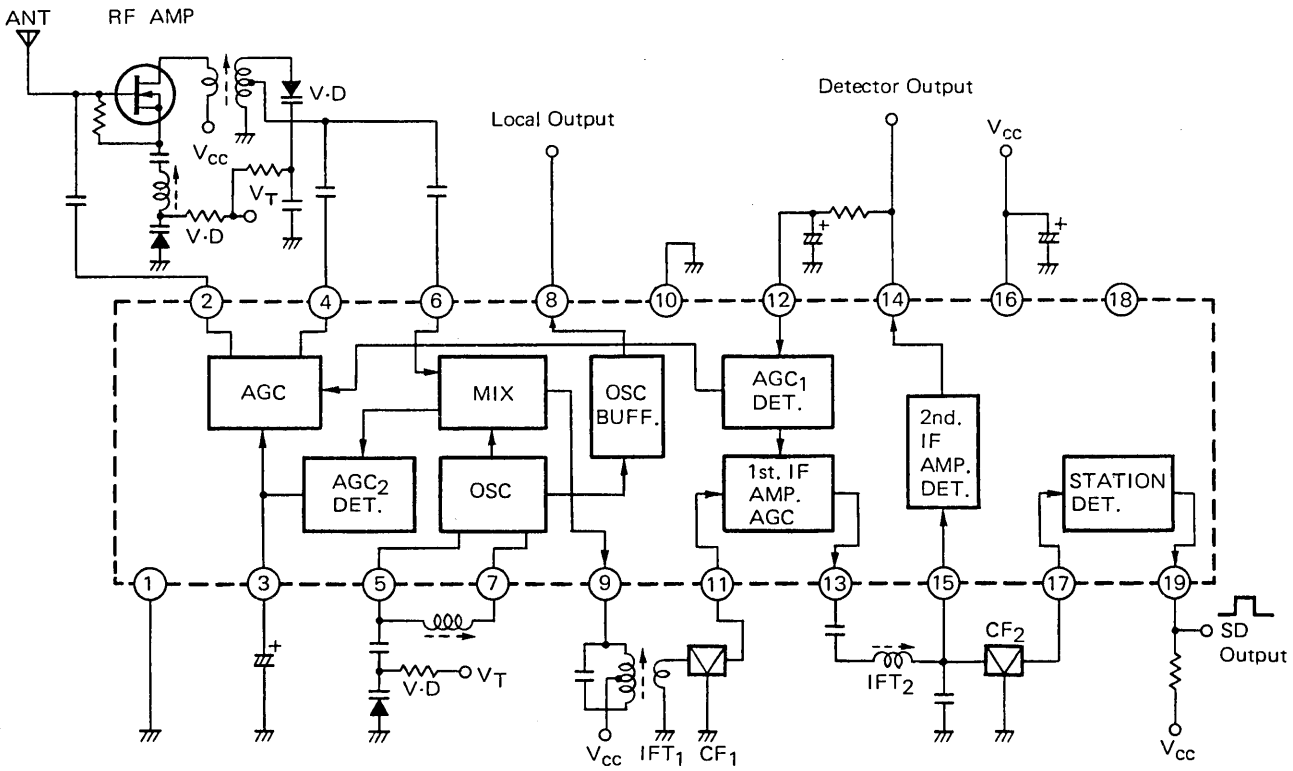


Fig. 1 Block Diagram

4. CIRCUIT DISCRIPTION

4-1 RF Amplifier stage

The antenna of car-radio is capacitive in the AM band, and the capacitive characteristics depend on antenna length and diameter as well as cable length. Therefore it is difficult to form a tuning circuit with a varactor diode in the RF amplifier input stage bacause the varactor is inserted parallel to the antenna equivalent capacitance. In view of this difficulty, an untuned input circuit configuration with some loss in S/N ratio is common. For an untuned RF input circuit, a J-FET is used since it is well matched to the high equivalent impedance of antenna and it has a good linearity. Because of untuned input, the interference is larger. On the other hand, it has an advantage that it does not need any antenna trimmer capacitance adjustment which is indispensable to μ-tuned radios. To use μPC1215V, J-FET2SK195 is needed for the RF amplifier. Pin 2 is provided to μPC1215V for the output of AGC to the RF amplifier.

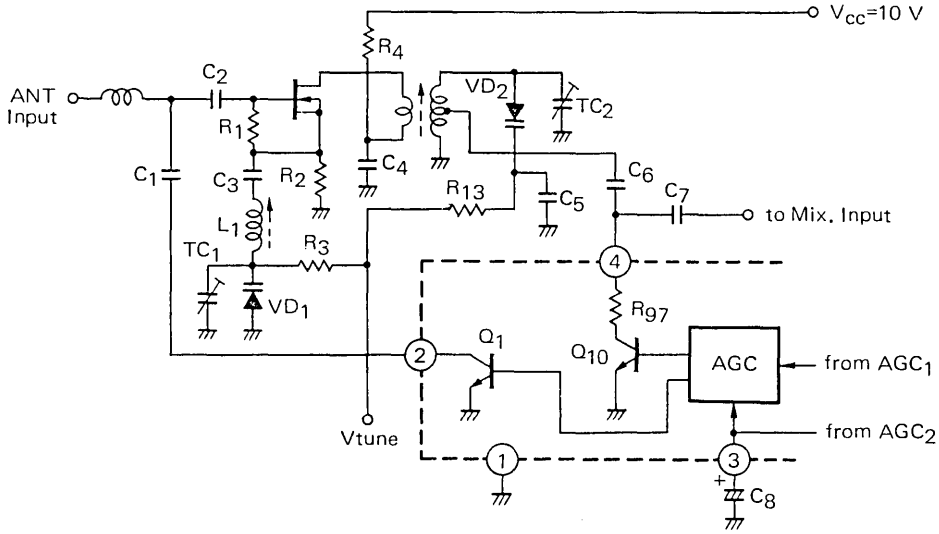


Fig. 2 RF Amplifier

The RF amplifier circuit has the untuned input, a single stage series resonance circuit on the source side, and a single stage parallel resonance circuit on the drain side. The DC gain of the J-FET is maximized by feeding I_{DSS}. The AC gain is maximized to desired signals by means of the source series resonance circuit but it is suppressed to interference signals. Thus this circuit configuration has a very small amount of loss and it is much insensitive to interferences.

The AGC circuit are provided to both the input and the output sides of the FET amplifier. The AGC's have a similar circuit configuration as that of ALC for low frequency signals. It operates on a principle that the signal path is short-circuited with a low impedance (about 50 Ω of the saturated resistance of the AGC transistor) to suppress the signal transfer to the next stage. The increase in input signal first sets the AGC on the side of pin 4 into action to prevent MIX to be saturated. The AGC on pin 4 reduces the gain by about 25 dB through the series resistance of the saturated resistance of Q_{10} and R_{97}. The AGC on pin 2 reduces the gain by as much as 40 dB. Since these AGC circuits can thus maintain the constancy of the output voltage for input voltage variation of as much as 65 dB altogether, good receiving characteristics can be obtained for a wide range of signal intensity. Furthermore, an AGC circuit of ALC type suppresses the signal input to RFA-FET. Therefore the saturation of FET can be suppressed, and, because of the overall signal level reduction, the RF signal applied to the varactor diode is kept low enough to reduce distortions in modulating signals caused by the non-linearity of the varactor diode.

4-2 Frequency Mixer Stage and Local Oscillator

The RF signal from the RF amplifier is delivered to the mixer stage conposed of Q_{13}, Q_{14}, Q_{11}, and Q_{12}. After mixing an IF component is issued from pin 9. The input impedance of the mixer is determined by R_{10} and it is about 2 kΩ // 8 pF.

The local oscillator is composed of Q_{17} and Q_{18}, feedback resistances R_{16} and R_{17}, L_3 of external parallel resonance circuit, and the varactor capacitance. Due to the non-linearity of the varactor diodes, the varactor capacitance varies when an oscillator signal with a large amplitude is superposed. In such a case a tracking error results because of a difference between the varactor capacitance in the mixer and that in the RF stage. Therefore the oscillation level should be maintained low. It is maintained at about 150 mV r.m.s. over the whole frequency range by R_{16} and R_{17}.

The amplifier composed of Q_{19}, Q_{20}, and Q_{21} are a buffer amplifier to deliver the local oscillation into the PLL frequency synthesizer. The output amplitude from this fuffer is 4.0 V_{p-p} and readily delivered to the CMOS LSI.

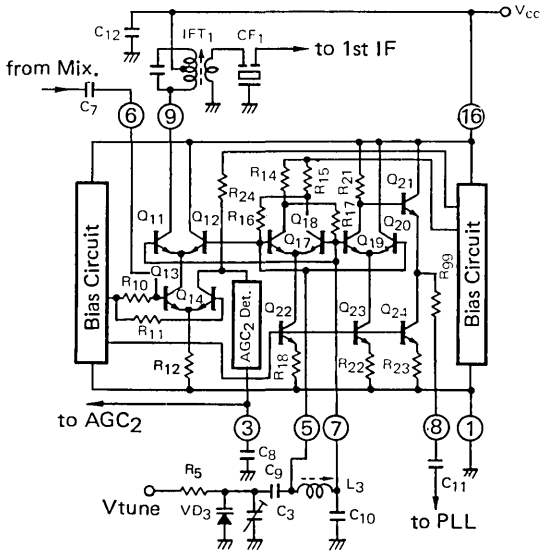


Fig. 3 Mixer and Local Oscillator

4-3 Intermediate-Frequency Amplifier Stage

The 1st IF amplifier stage is composed of an IF amplifier stage and AGC circuit. Inherently it has a gain of about 34 dB by the emitter-grounded amplifier of Q_{34} and the output is drawn out from the emitter follower of Q_{41}. Its gain is controlled by Q_{28}, Q_{29}, and AGC_1 circuit in such a manner that the gain reduction of up to about 27 dB is resulted from the increase of detected AGC_1 voltage. For further input level increase, the before mentioned RF AGC is set into action. The input impedance of the 1st IF amplifier is determined by R_{32} and it is about 2.5 kΩ // 40 pF.

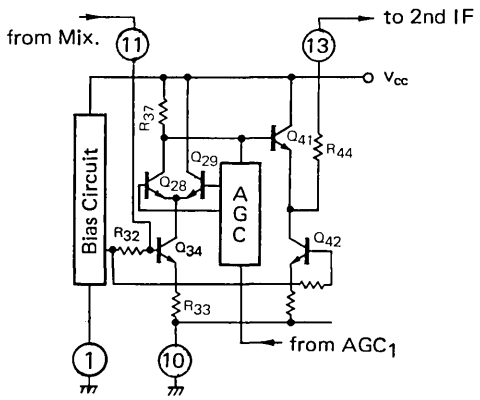


Fig. 4 IF Amplifier

4-4 Detector stage

The detector stage composed of Q_{53} and a smoothing capacitance is located next to the second IF amplifier composed of Q_{47} and Q_{48}. The input impedance to pin 15 is determined by R_{54}, and it is about 4 kΩ // 20 pF.

4-5 AGC Circuit

μPC1215V has two independent AGC detectors and three AGC circuits. The AGC_1 detector supplies an AGC control voltage to the first IF amplifier, and, a somewhat delayed AGC control voltage to the RF AGC, both determined by the DC voltage on pin 12 which is the smoothed detector output.

Since the AGC input voltage on pin 12 is directly coupled with the detected output on pin 14, the detected output and the AGC range can be adjusted by the resistance Rg which is externally connected to pin 14. If Rg is smaller, the AGC input voltage on pin 12 is less and thus the input voltage at which the AGC starts to operate becomes larger to increase the detected output. If Rg is larger, AGC starts to operate at a smaller input voltage and thus the detected output is maintained at a low constant level. The maximum distortionless detected output (with a voltage depression effeet also taken into account) is 150 $mV_{r.m.s.}$ Accondingly, adjust Rg so that an output of about 100 $mV_{r.m.s.}$ is obtained at an input of 74 dBμV for a modulation of 30 %. μPC1215V's are classified into the following ranks according to the needed Rg resistance value in order that the IC's are used at an optimum detected output with a minimum variation.

rank D ..... Rg = 12 kΩ
rank E ..... Rg = 18 kΩ
rank F ..... Rg = 39 kΩ
rank H ..... Rg = ∞

These settings give a detected output of about 100 $mV_{r.m.s.}$, respectively.

On the other hand, the AGC_2 detector shown in Fig. 3 is provided for preventing the saturation of RF amplifier or mixer due to the cutoff of AGC from AGC_1 detector by detuning or due to the interference signal from the adjacent channel. Therefore it is inactive in normal operations.

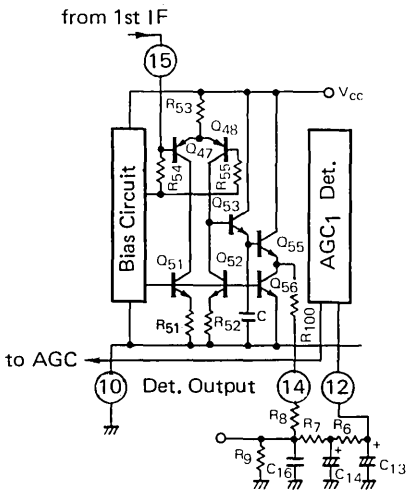


Fig. 5 AM Detector

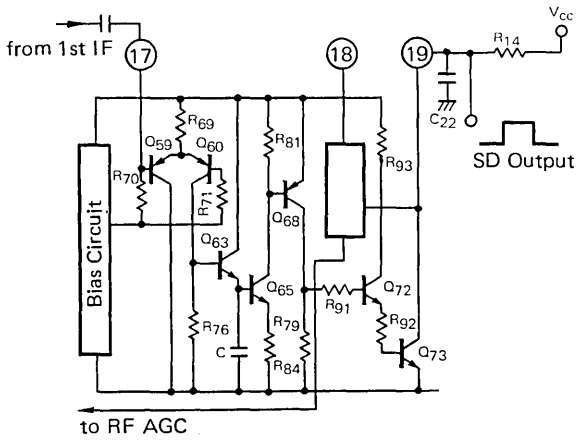


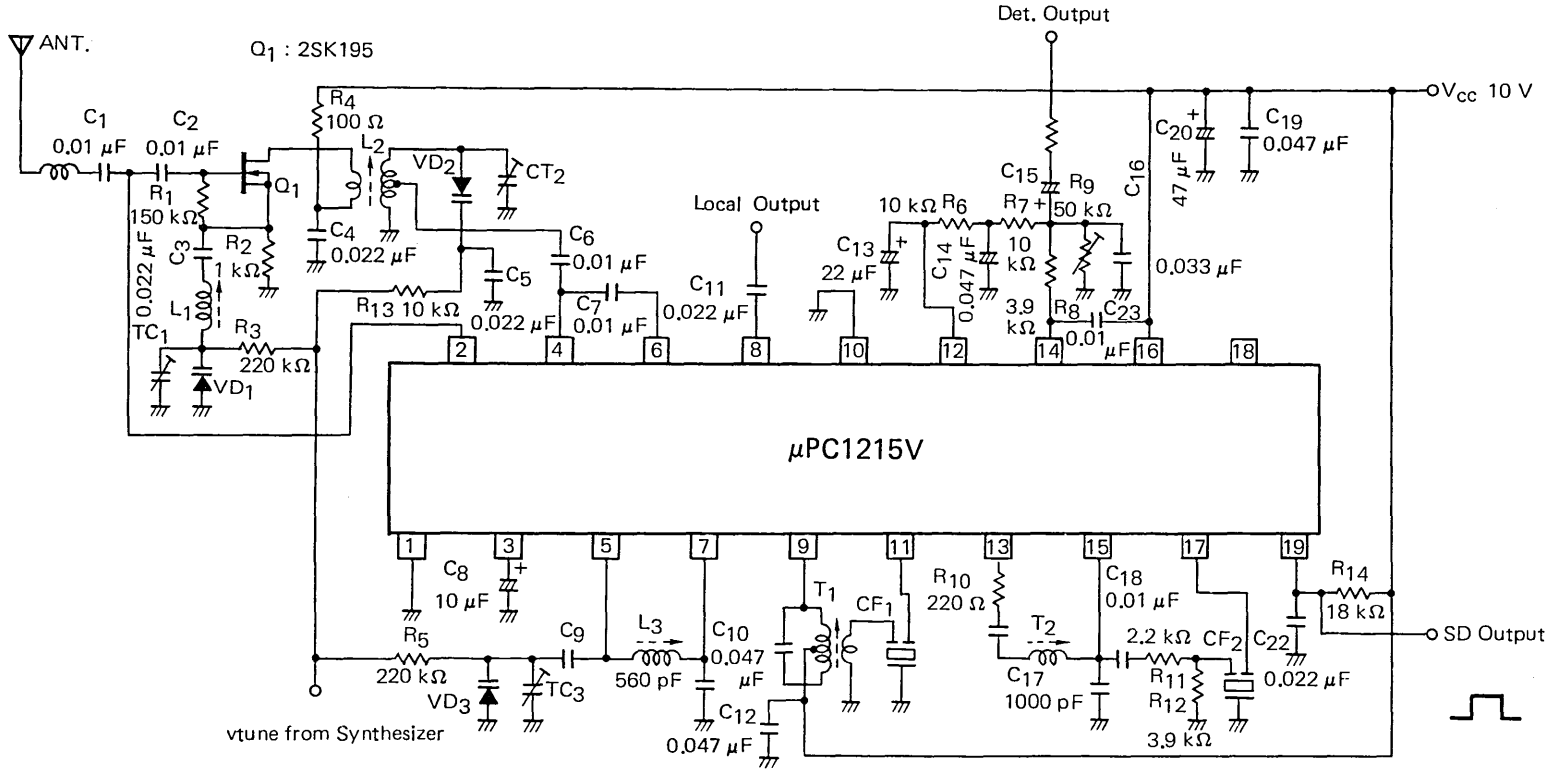
Fig. 6 Station Detector

4-6 Station Detector Stage

The station detector (SD) is provided to stop automatic scan-seeking when a station is found. A high-level DC output is obtained by this detector when a station is found. It has almost the same circuit configuration as the detector shown in Fig. 5. An IF signal of 450 kHz obtained by the IF amplifier is discriminated from that of the adjacent channel by a narrow-band ceramic filter CFM2-450ZL and delivered to this stage through pin 17. After amplified by one stage by Q_{54} and Q_{60}, the signal is demodulated by Q_{36} and a smoothing capacitance, DC-amplified by Q_{65} and Q_{69} to drive Darlington open collector transistors Q_{72} and Q_{73}.

The input impedance on pin 17 is about 1.8 kΩ // 25 pF.

Since the output is obtained from the open-collector transistor Q_{73}, the power supply voltage can be set arbitrarily, for example, to 5 V which is the same as logic system voltage.



L_1, L_2 : 7BR-5407N (Toko) T_1 : 7MC-4718 (Toko) CF_1 : CFM2-450BL

L3 : 7BR-6048Z (Toko) T_2 : 7MC-10100CO (Toko) CF_2 : CFM2-450ZL

$VD_1 \sim VD_3$: Varactor Diode.

C = 500 pF ~ 30 pF TYP.

Fig. 7 Application Circuit 1

5. ELECTRICAL CHARACTERISTICS

Table 1 shows principal electrical characteristics of the IC measured by the circuit showen in Fig. 7.

Table 1 Overall Characteristics (Reference)

(T_a = 25 °C, V_{CC} = 10 V, f = 1 MHz, f_{mod} = 400 Hz, m = 30 %)

CHARACTERISTIC	TEST CONDITION	VALUE	UNIT
Maximum Sensitivity	v_o = 30 $mV_{r.m.s.}$	22	dBμV
Usable Sensitivity	S/N = 20 dB	28	dBμV
Detector Output Voltage	v_i = 74 dBμV	100	$mV_{r.m.s.}$
Total Harmonic Distortion	v_i = 74 dBμV	0.3	%
	v_i = 126 dBμV	0.6	%
	v_i = 74 dBμV, mod. = 80 %	1.2	%
Signal to Noise Ratio	v_i = 74 dBμV	52	dB
IF Rejection Ratio	v_o = 30 $mV_{r.m.s.}$, IF = 450 kHz	56	dB
Image Rejection Ratio	v_o = 30 $mV_{r.m.s.}$, f+2 IF	57	dB
Selectivity	Δf = ±10 kHz	39	dB
Tweet	v_i = 74 dBμV, 2 IF = 900 kHz	40	dB
	v_i = 74 dBμV, 3 IF = 1 350 kHz	50	dB
SD Sensitivity	V_{SD} = 0.5 V_{CC}	25	dBμV
SD Bandwidth	v_i = 74 dBμV, V_{SD} = 0.5 V_{CC}	5.0	kHz
Oscillation Voltage	At terminal 5	150	$mV_{r.m.s.}$
	At terminal 8	4.0	Vp-p

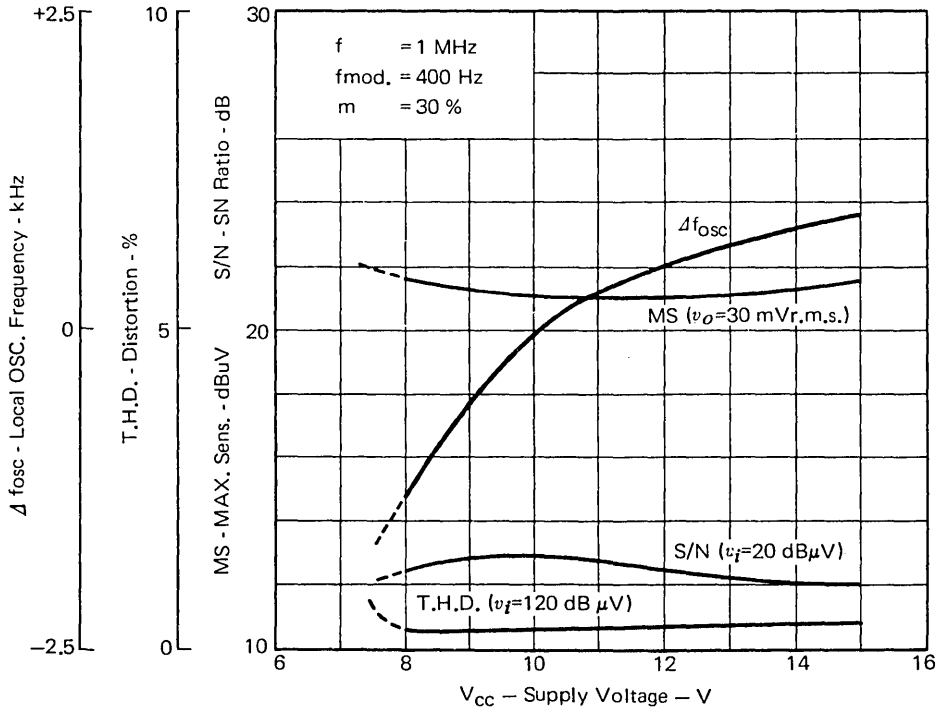


Fig. 8 Dependencies on Power Supply Voltage

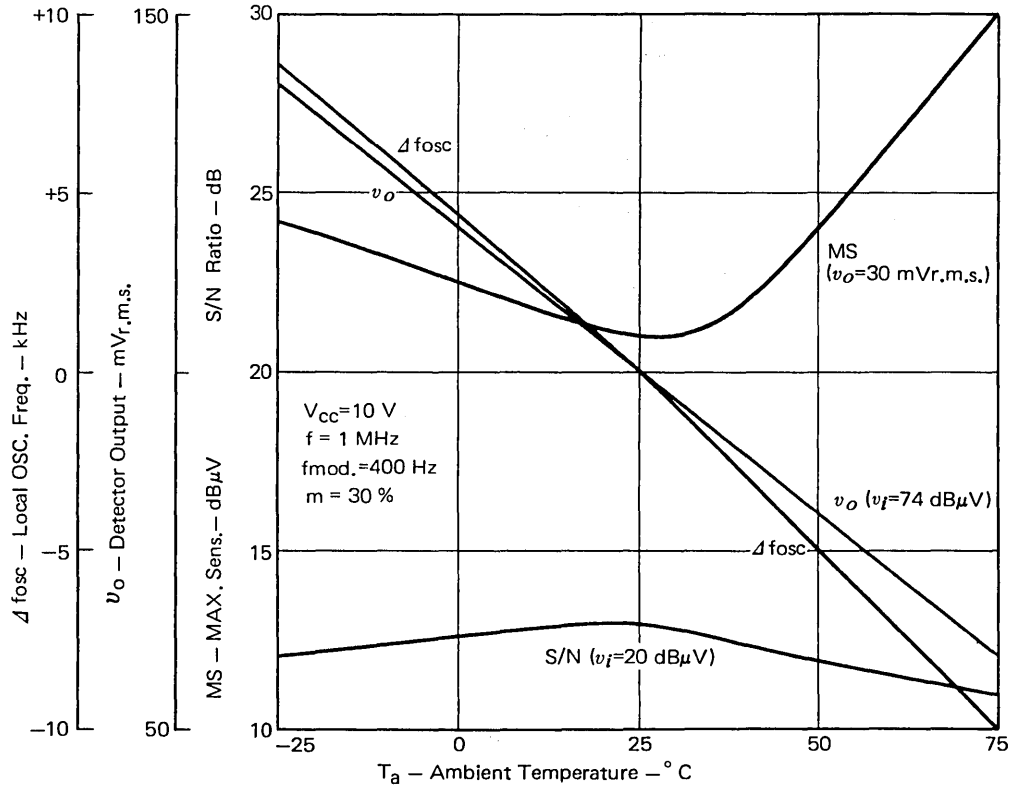


Fig. 9 Temperature Dependencies

Note: The characteristic curves shown above were measured by varying the temperature of the IC only. The externally connected parts were maintained at 25 °C.

6. PRECAUTIONS IS USING μPC1215V

6-1 Varactor Tuning Circuit

Although μPC1215V is designed so that the RF signal to be applied to the varactor is suppressed, it is possible that a large RF signal is applied to the varactor if detuning occurs due to too large signal input to the RF stage. Therefore the use of varactor diode with as good linearity as possible is recommended.

The capacitance which the varactor diode is required to have is about 500 pF at 530 kHz and about 30 pF at 1 620 kHz when specified Toko coils are used. To obtain the minimum tracking errors for the tracking at 600 kHz and 1 400 kHz, set as specified in Table 2.

Table 2

C_{Vmax}	450 pF	500 pF	(7BR-5407N) 170±6 %
C_{Vmin}	30 pF	30 pF	
L_A	192 μH	171 μH	
C_{SA}	20.3 pF	26.3 pF	(7BR-6048BZ) 95±5 %
L_O	109 μH	97.7 μH	
C_{SO}	32 pF	39.3 pF	
C_{pd}	472 pF	529 pF	

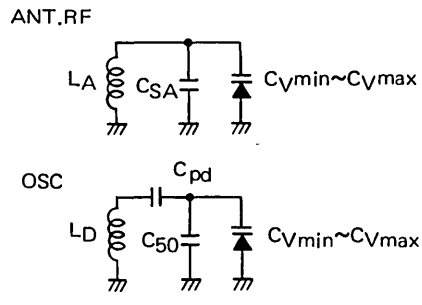


Fig. 10 Resonance Circuit

6-2 J-FET for RF Amp

The practical sensitivity and S/N ratio for weak input depend on the J-FET to be connected externally and not on μPC1215V itself. Use an FET with a good NF and a high gain.

Typically, 2SK193 or 2SK195 of F or H rank is recommended.

6-3 AGC Smoothing Circuit

The detected output on pin 14 is smoothed and delivered to the AGC detector on pin 12. Since the circuit constants of the AGC smoothing circuit determines the time needed for the circuit to reach the equilibrium and affects the build-up of stop signals, it is necessary in the actual circuit application to change the constants on the circuit configurations properly according to the actual conditions. The constants described in the catalogues are specified for the optimum characteristics in the stationary state of operation.

Fig. 11 shows the detected output and the stop signal build up characteristics when AGC constants are:

$\begin{cases} R_7 = 10\,k\Omega, C_{14} = 10\,\mu F, \\ R_6 = 10\,k\Omega, C_{13} = 10\,\mu F. \end{cases}$

In the figure, because of too large AGC time constants and the same constants used in succession, the AGC line oscillates and the stop signal output is once boosted up and then takes the lower level again. An this case, according to the timing of controller checking of stop signal, the presence of station might be neglected and the scan-and-seek motion might not be stopped.

Fig. 12 shows the waveforms obtained for the corrected AGC smoothing circuit constants:

$\begin{cases} R_7 = 10\,k\Omega, C_{14} = 0.47\,\mu F \\ R_6 = 10\,k\Omega, C_{13} = 22\,\mu F. \end{cases}$

The problems such as encountered above are solved. However, the adoption of smaller time constants leads to the some increase in distortion for low-frequency modulating signals.

Fig. 13 shows an example of circuit that can be operated safely even with AGC constants such as used in Fig. 7 and, when the auto-seek reception of a weak station adjacent to a strong station is desired, prevent AGC from being applied by utilizing a mute pulse to avoid the reception at a deeply applied AGC state necessarily resulted from a long discharge time of the AGC circuit. However, in this circuit, because of AGC rise-up after the releasing of mute, sometimes transient signals are heard due to AGC rise-up. Due attentions are needed in the actual disign.

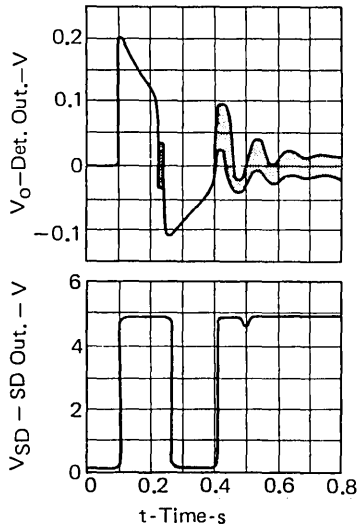


Fig. 11 Rise-up Waveform

AGC Constants

$R_7 = 10\,k\Omega$, $C_{14} = 10\,\mu F$

$R_6 = 10\,k\Omega$, $C_{13} = 10\,\mu F$

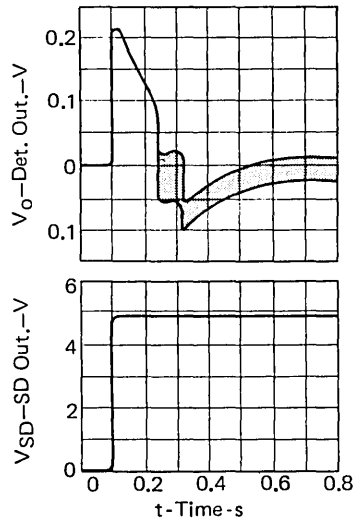


Fig. 12 Rise-up Waveform

AGC Constants

$R_7 = 10\,k\Omega$, $C_{14} = 0.47\,\mu F$

$R_6 = 10\,k\Omega$, $C_{13} = 22\,\mu F$

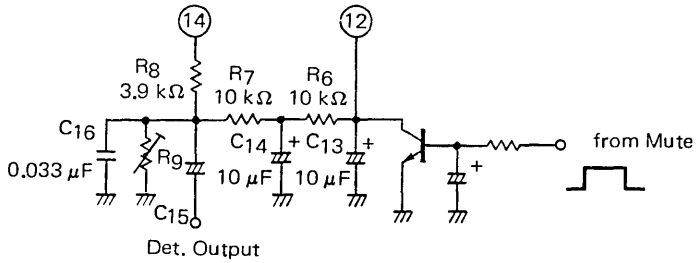


Fig. 13 AGC Smoothing Circuit

6-4 Tweet

Because provided with a detector circuit with little higher harmonics, μPC1215V is superior in low tweet. However, the contained station detector works adversely with respect to the tweet. For suppressing tweet which is especially a source of trouble during weak input reception, insert a capacitance of 0.01 μF between pins 14 and 16, and 0.047 μF between pin 19 and the GND to suppress an AC component on pin 19 for stop-seek output. Also, GND should be located as close to the GND pin 10 of the IC as possible. The station detection, which is only necessary for auto-scan-seek and unnecessary otherwise, may be put inactive during mute off by using mute pulse to forcefully shift the level of DC bias of station detector input on pin 17 with a transistor switch.

7. OTHER TYPICAL APPLICATION CIRCUITS

7-1 Two Stage RF Amplifier

The one-stage series resonance circuit connected to the source of the RF stage FET which is shown in Fig. 7, Typical Application 1 of μPC1215V cannot have high Q because the load Q is determined by the source impedance of the FET. In cases where IF and image interference ratio characteristics are of principal concern, the RF stage can be composed of a double-tuning circuit.

Fig. 16 is an example of M-coupled double-tuning circuit. Table 3 shows the principal electrical characteristics. C-couple double-tuning circuit can also be conceived. In this case it is necessary to design the circuit with the change of coupling coefficient taken into account for varying the varactor capacitance. A two-stage RF amplifier can be used also, with the adjustment of gain balance needed, To reduce IF stage gain, the increase of loss between pins 13 and 15 is also effective.

Table 3 Overall Characteristics (Application Circuit 2)

(T_a = 25 °C, V_{CC} = 10 V, f = 1 MHz, f_{mod} = 400 Hz, m = 30 %)

CHARACTERISTIC	TEST CONDITION	VALUE	UNIT
Maximum Sensitivity	v_o = 30 $mV_{r.m.s.}$	22	dBμV
Usable Sensitivity	S/N = 20 dB	29	dBμV
Detector Output Voltage	v_i = 74 dBμV	100	$mV_{r.m.s.}$
Total Harmonic Distortion	v_i = 126 dBμV	0.5	%
Signal to Noise Ratio	v_i = 74 dBμV	50	dB
IF Rejection Ratio	v_o = 30 $mV_{r.m.s.}$, IF = 450 kHz	72	dB
Image Rejection Ratio	v_o = 30 $mV_{r.m.s.}$, f+2 IF	64	dB

7-2 Application in LW-band

A LW/MW car radio using μPC1215V can be composed by providing respective separate tuning circuits for LW and MW (with two sets of varactor diodes, altogether six in number) which can be selected by a switch. However, to reduce the cost, it is usually to use only three varactor diodes which can be commonly used for LW and MW. The coil selection is done by using switching diodes. This switching system encounters some difficulties in local oscillator which are not suffered by conventional mechanical tuners. However, for the LW receiving frequencies 155-281 kHz, common padding capacitances and oscillation coil can be used in both LW and MW without any increase in tracking error, thus the diode switching is unnecessary. This can be realized by rendering the LW-band tuning voltage coverage a little broader than that for MW-band. For example, if

MW : 530–1 620 kHz be covered by 430–28 pF capacitance

and

LW : 155–281 kHz be covered by 470–25 pF capacitance,

the tracking errors in the both bands are minimized with the constants:

L_{osc} = 103.2 μH, C_{pad} = 470 pF,

stray capacitance for MW C_{SM} = 30.8 pF, and

stray capacitance for LW $C_{SM} + C_S + C_{SL}$ = 435.6 pF.

Thus, the addition of a 408.8 pF capacitance is only necessary to switch over to LW from MW.

Since the FET of RF amplifier is externally connected, the band can be selected by switching diodes as has been done in conventional discrete circuits. When calculated using the above mentioned frequency bands and varactor capacitances for The Application Circuit 2 of Fig. 16, the following data are obtained.

L_{RF-MW} = 206 μH
C_{SM} = 18 pF
L_{RF-LW} = 1 666 μH
C_{SL} = 167.4 pF

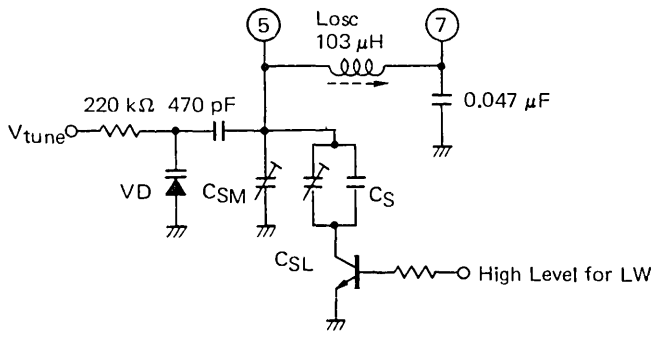


Fig. 14 MW/LW Switching of Local Oscillator

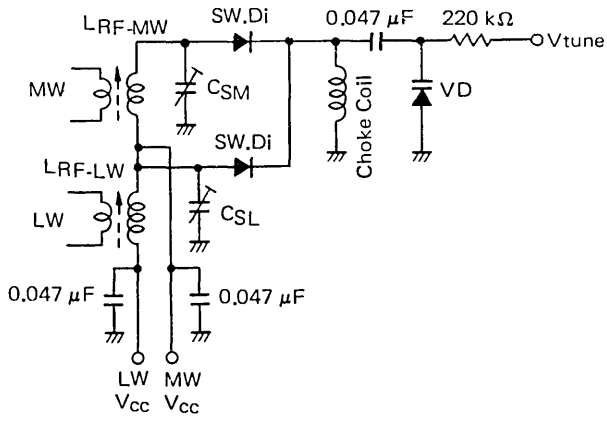
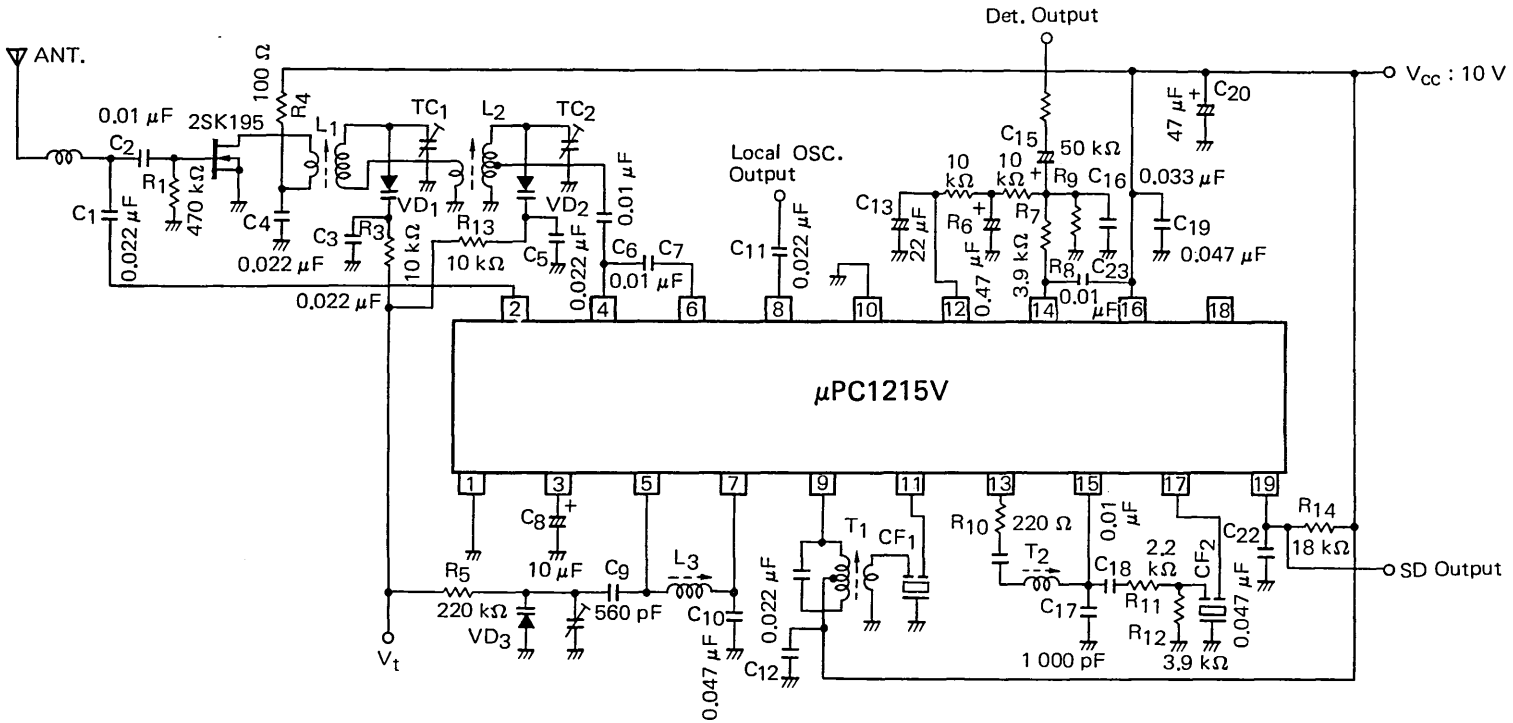
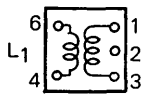
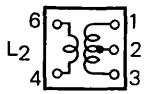


Fig. 15 MW/LW Switching of RF Amplifier





1–3 : 68T, Qu=80 min.
4–6 : 27T L=170 μH



1–2 : 63½T Qu=80 min.
2–3 : 6T L=170 μH
4–6 : 2T

L_3 : 7BR–6048Z, T_1 : 7MC–4718N, T_2 : 7MC–10100CO
CF_1 : CFM_2–450BL
CF_2 : CFM_2–450ZL

$VD_1 \sim VD_3$: Varactor Diode
C=500~30 pF

Fig. 16 Application Circuit 2

APPLICATION OF MOBILE AM TUNER μPC1216V2

1. INTRODUCTION

The μPC1216V2 is a bipolar monolithic IC developed as an AM tuner for a car radio and car stereo, and contains a series of circuits from radio frequency amplifier to AM detector. Since this IC is designed to accomodate ceramic filters for its IF selective elements, an adjustment-free IF stage is achieved. Furthermore, having little dependency of the maximum sensitivity on receiving frequency, it is free from sensitivity decrease toward 1 400 kHz and large increase of inter station noise around 600 kHz.

Because it is packaged in newly developed 19-pin vertical dual in-line package (V-DIP), the IC requires small mounting area. In addition, it can be handled with much more ease and can be free of mismounting due to its lead formation.

This document first describes the performance of each stage, the role of the external components and the characteristics with the changes of those components constants. Finally, an example of circuit application with perfectly adjustment-free IF stage is described with the characteristics of this circuit.

2. FEATURES

- Adjustment-free IF stage
- Little difference in maximum sensitivity on receiving frequency
- Large electrostatic breakdown strength at the antenna input
- Extremely low pop noise
- Low distortion
- Superior two-signal selectivity
- High sensitivity
- Small package

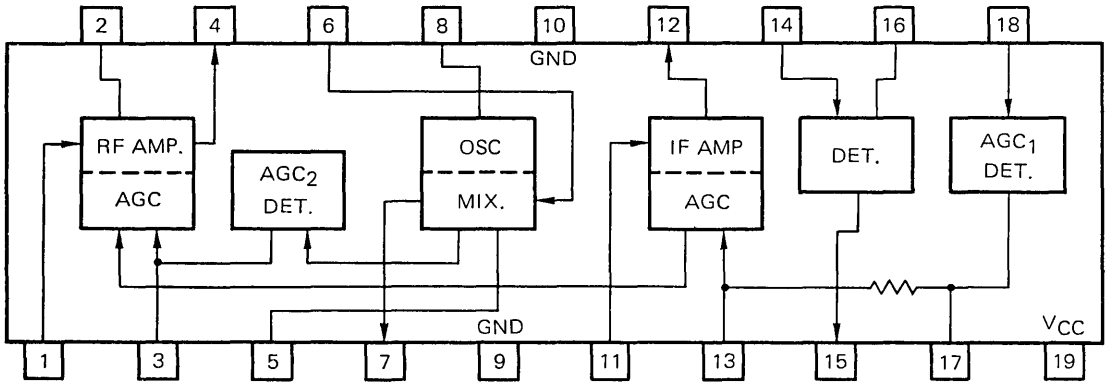
3. ELECTRICAL CHARACTERISTICS

Table 1 is the list of μPC1216V2 pincipal electrical characteristics measured by the Fig. 27 test circuit.

Table 1. TUNER PERFORMANCE CHARACTERISTICS
(T_a = 25 °C, V_{CC} = 13 V, f = 1 MHz, f_{mod} = 400 Hz, MOD = 30 %, R_L = 10 kΩ)

CHARACTERISTIC	TEST CONDITIONS	VALUE	UNIT
Max. Sensitivity	Input Voltage at which Det. Output Voltage is 40 mVr.m.s.	13	dBμV
Usable Sensitivity	Input Voltage at which S/N is 20 dB	23	dBμV
Detector Output	v_i = 74 dBμV	110	mVr.m.s.
Detector Distortion	v_i = 74 dBμV	0.4	%
Signal-to-Noise Ratio	v_i = 74 dBμV	54	dB
Overload Distortion	v_i = 126 dBμV	0.4	%
IF Rejection	f = 1 MHz, v_o = 40 mVr.m.s., IF = 450 kHz	72	dB
Image Rejection	f = 1 MHz, v_o = 40 mVr.m.s., f + 2 IF	74	dB
Selectivity	f = 1 MHz, Δf = ±10 kHz	45	dB
Tweet	v_i = 74 dBμV, 2 IF = 900 kHz	45	dB
	3 IF = 1 350 kHz	50	dB

BLOCK DIAGRAM (Top View)



4. CIRCUIT DESCRIPTION

4-1 RF STAGE

The radio-frequency (RF) stage consists of an RF amplifier and an automatic gain control (AGC) circuit. (see Fig. 1)

At the antenna resonance circuit, the desired station signal is selected from the signals received by the antenna. This signal is introduced into the IC via pin-1, then amplified by transistors $Q_1 \cdot Q_2$ and $Q_5 \cdot Q_6$, and outputted through pin-4. When AGC is not in action, the gain of RF amplifier is about 34 dB (Fig. 2), and its −3 dB cutoff frequency is about 14 MHz (Fig. 3). When a large signal arrives, AGC is set in action to attenuate the gain of the RF amplifier. Fig.4 shows the relationship between AGC voltage and gain attenuation. The voltage gain is approximately 34 dB for AGC voltage less than about 1.4 V, whereas, the gain attenuation in $Q_5 \cdot Q_6$ takes place for an AGC voltage from 1.4 to 1.55 V because the bias voltage of Q_5 begins to decrease. A further large input that brings more than 1.65 V or so will decrease the bias voltage of Q_3 to decrease the gain of $Q_1 \cdot Q_2$. In this way, the output voltage is kept the level constant for input voltage change within about 70 dB. Therefore, a good receiving characteristics are obtained over the wide range from a faint to large input.

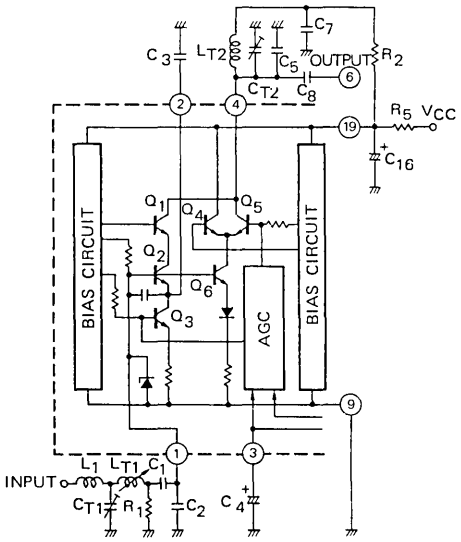


Fig. 1 Equivalent Circuit of RF Stage.

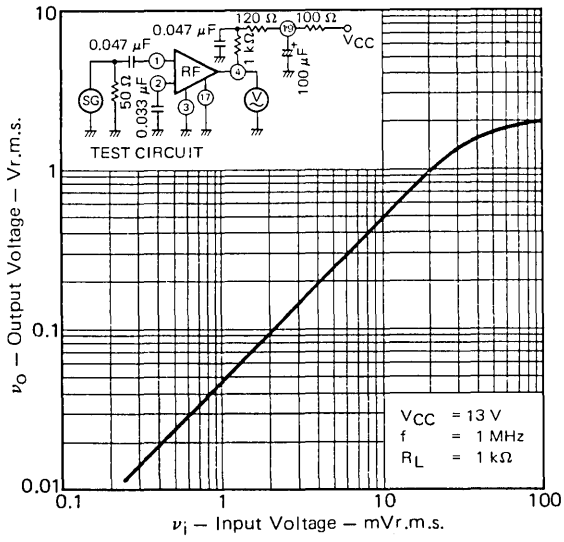


Fig. 2 Voltage Transfer Characteristic of RF Stage.

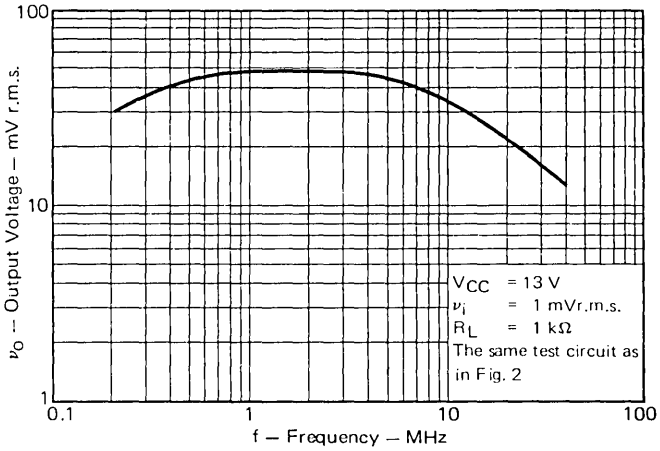


Fig. 3 Frequency Response of RF Stage.

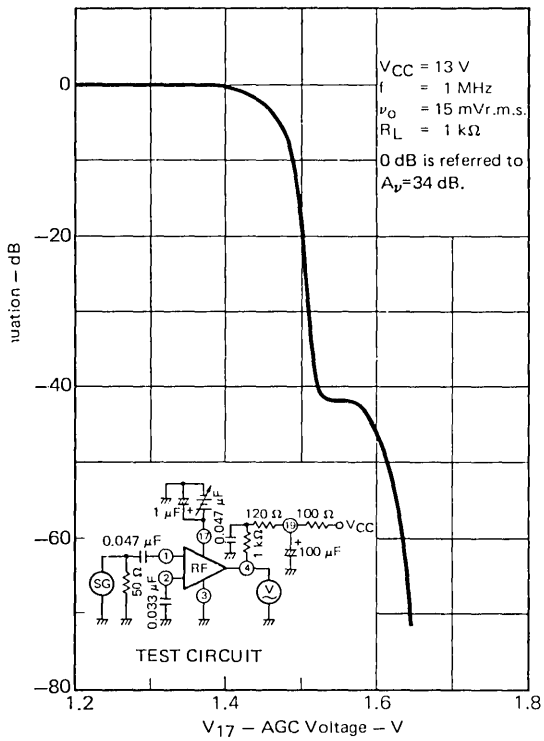


Fig. 4 AGC Characteristic of RF Stage.

4-2 FREQUENCY CONVERTER STAGE

The frequency converter stage contains a local oscillator and a mixer (Fig. 5). The local oscillator is composed of Q_{13}·Q_{14} and its oscillation frequency is determined by an LC circuit connected through pin-8. The mixer consists of Q_8·Q_9·Q_{11}. The RF signal fed through pin-6 is amplified by Q_{11} (A_v=10 dB, see Fig. 6). Then it is mixed with the local oscillation signal within Q_8·Q_9 and converted to an intermediate frequency (IF) signal by the selectors (T_1 and CF_1) connected to pin-7.

A bypass capacitor C_6 is connected to the emitter of Q_{11} (pin-5) for the following purpose. Generally, Q factor of RF resonance circuit, which is the RF load, is inverse proportional to the receiving frequency, that is, Q is lower at higher frequencies than at lower frequencies. In addition, the loss between pin-4 and pin-6 is proportional to the receiving frequency, that is, the loss is larger at higher frequencies. Therefore, the gain of the RF stage in the high frequency region is lower by approximately 15 dB than in the low frequency region. In conventional IC's, sensitivity decrease in the high region and abnormal increase of inter station noise in the low region have been experienced as shown by dotted curves in Fig. 8. Countermeasures such as insertion of a damping resistor parallel to L_{T2} have been taken, but they could not solve the problems satisfactorily. Whereas, in μPC1216V2, the capacitor C_6 compensates that frequency characteristic and minimized frequency dependence of maximum sensitivity as far as possible. The gain increase in high frequency region brings about some deterioration in image rejection, but it brings about the improvement in IF rejection (Fig. 8).

If necessary, the mixer gain, concerned with maximum sensitivity, can be changed by varing the constant of C_6. (Fig. 9) Furthermore, the insertion of a several-hundred-ohm resistor in series to C_6 makes the frequency characteristics flat as shown by dotted curve in Fig. 7. In this case, the frequency characteristics become similar to those of conventional IC's as shown by a dotted curve in Fig. 8.

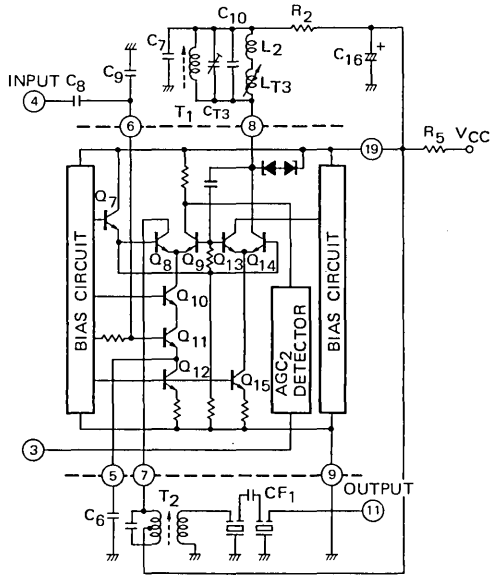


Fig. 5 Equivalent Circuit of Frequency Converter Stage.

Fig. 6 Voltage Transfer Characteristic of Converter Stage

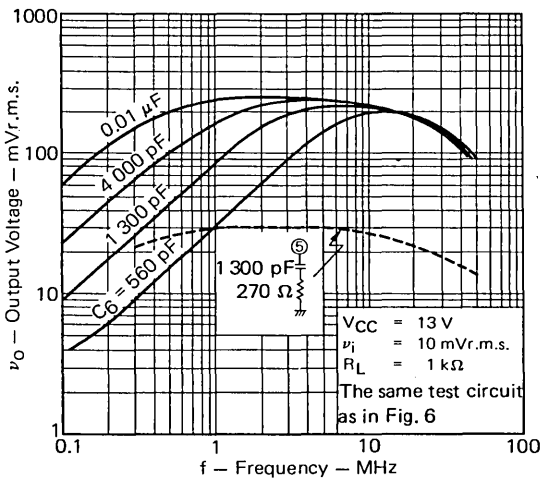


Fig. 7 Frequency Response of Converter Stage.

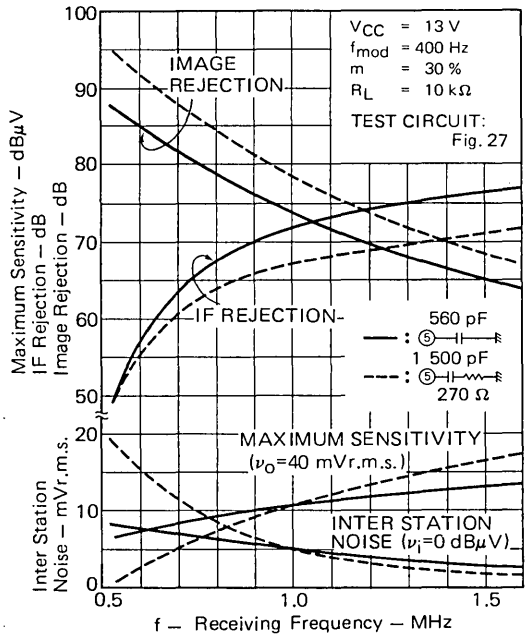


Fig. 8 Effect of C_6 on Receiving Frequency Dependency

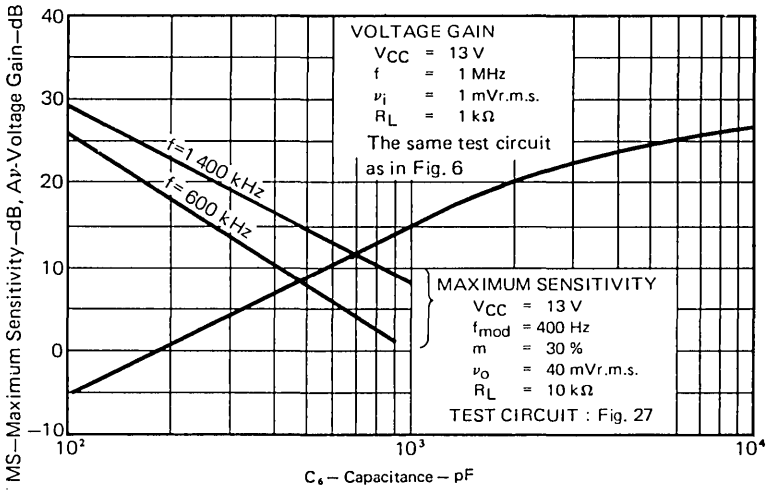


Fig. 9 Maximum Sensitivity and Voltage Gain in Converter vs. Capacitance C_6

4-3 IF STAGE

The IF stage is composed of an IF amplifier and AGC circuit (Fig. 10). The IF signal taken out the converter stage is fed through pin-11 to a differential amplifier $Q_{18} \cdot Q_{19}$. The amplified signal is output to pin-12 via emitter follower transistor Q_{21}. The voltage transfer and frequency characteristics of the IF stage are shown in Figs. 11 and 12, respectively.

When an input signal is increased, AGC circuit operates to lower the Q_{20} base voltage, then the Q_{20} collector current which is the constant current source of $Q_{18} \cdot Q_{19}$ decreases, thus leading to the gain attenuation of IF amplifier. Fig. 13 shows the relationship of the input voltage necessary for a constant output voltage to the AGC voltage (V_{17}). For V_{17} less than approximately 1.3 V the AGC circuit is inactive. For V_{17} at about 1.4 V the circuit starts to work, and the voltage gain is attenuated accordingly to the increase of AGC voltage until V_{17} reaches about 1.5 V, the gain is no longer attenuated for V_{17} more than 1.5 V. In this case, the AGC circuit for the RF stage is set into action instead.

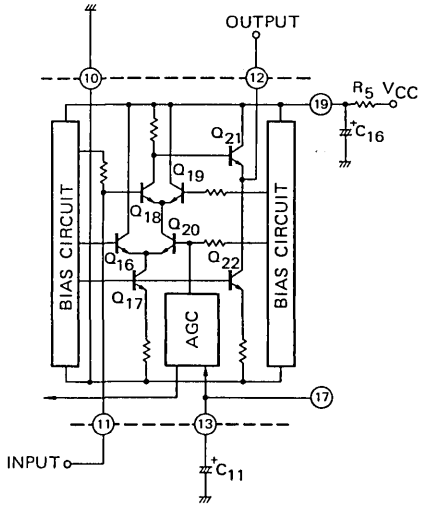


Fig. 10 Equivalent Circuit of IF Stage.

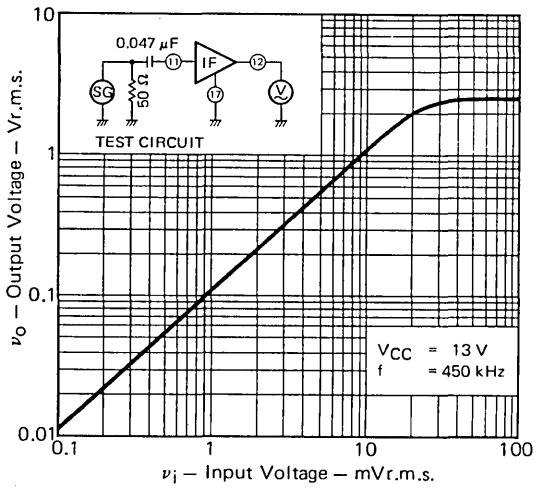


Fig. 11 Voltage Transfer Characteristic of IF Stage.

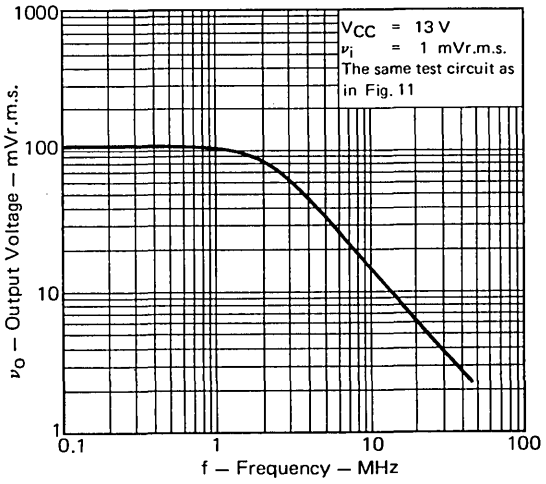


Fig. 12 Frequency Response of IF Stage.

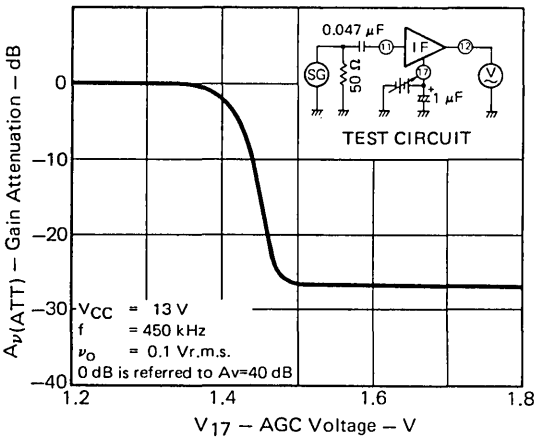


Fig. 13 AGC Characteristic of IF Stage.

4-4 DETECTOR STAGE

The detector stage consists of an IF amplifier, a detector and a switch-on popping noise absorber (Fig. 14).

In order to realized an adjustment-free IF stage, μPC1216V2 is so designed that a ceramic filter can be used instead of conventional detector transformers. Generally a ceramic filter has larger insertion loss than an IF transformer, and requires accurate impedance matching. Therefore, a ceramic filter can not be readily used here in conventional IC's. However, this IC is provided with one stage differential amplifier (Q_{24} · Q_{25}) before the detector, in order to match the impedance with the ceramic filter and to compensate the insertion loss.

The detector is composed of Q_{28} and smoothing capacitor. It demonstrates high recovered output and low distortion with minimum external components. This circuit produces little IF harmonics, resulting in an improvement of tweet characteristic. The voltage transfer characteristic is shown in Fig. 15, the electrical fidelity in Fig. 16 and the characteristic as a function of supply voltages in Fig. 17, respectively. Fig. 18 shows the load resistance dependence of the recovered output. The output impedance of detector stage is approximately 4 kΩ.

The switch-on popping noise absorber is provided for preventing abnormal sounds with irregular waveforms (Fig. 19-(4)) or sudden changes of dc voltage (Fig. 19-(3)) generated when power is turned on. It is so designed that the muting is active for about 0.4 seconds after the turning on the switch (Fig. 19-(2)). In addition, the change of dc voltage on output pin-15 on releasing the muting is devised to be smooth and not stepped to prevent the generation of popping noise (Fig. 19-(1)). The larger is the capacitance of C_{14} connected to pin-16, the smaller is the switch-on popping noise, but the longer the muting time. On the contrary, if the capacitance is reduced, the muting time is shortened at the sacrifice of muting effect, resulting in an unpleasant popping noise at the releasing of the muting or in an output of abnormal sound without being muted. Fig. 20 shows the relationship of popping noise and the switch-on time to the capacitance of C_{14}. When μPC1216V2 is used in an AM receiver without FM tuner and tape player, and when the switch-on time of the power amplifier is longer than that of μPC1216V2, C_{14} may be removed.

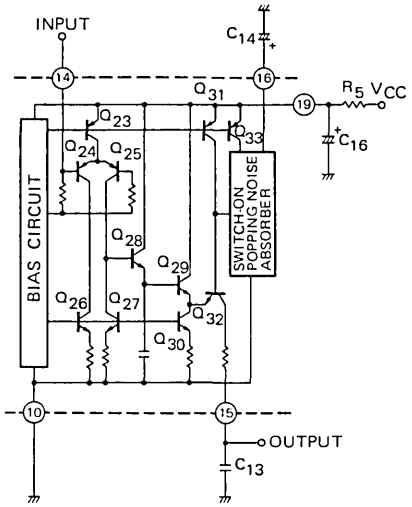


Fig. 14 Equivalent Circuit of Detector Stage

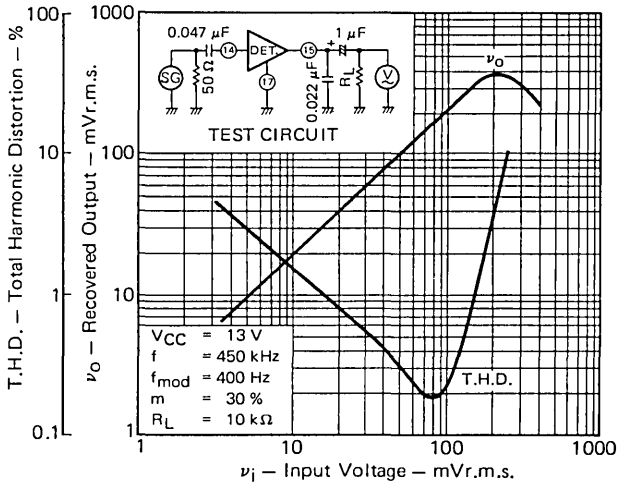


Fig. 15 Voltage Transfer Characteristic of Detector Stage

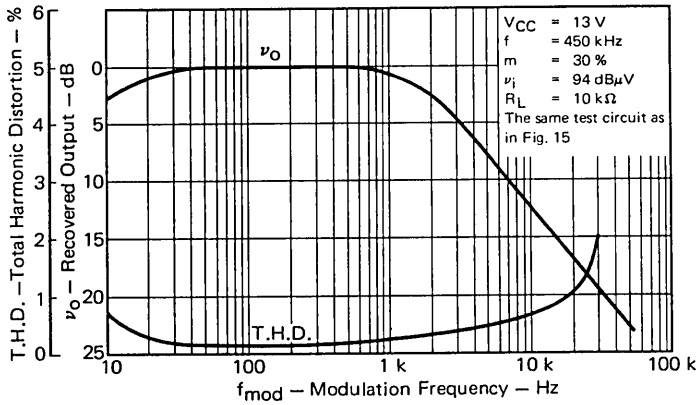


Fig. 16 Electrical Fidelity Characteristic of Detector Stage

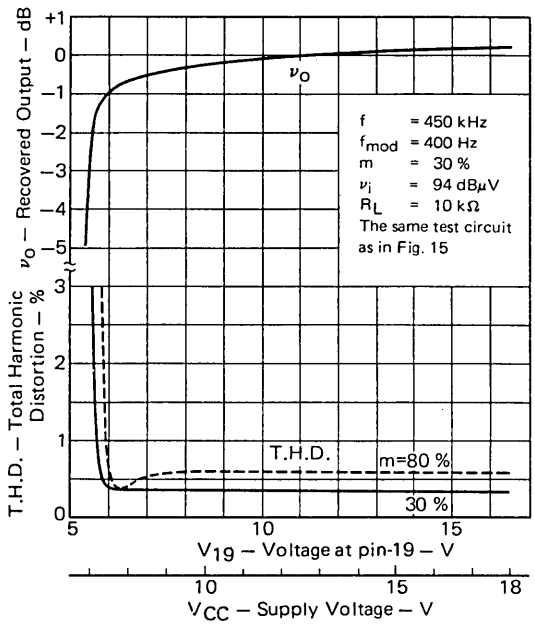


Fig. 17 Characteristics of Detector Stage as a Function of Supply Voltage

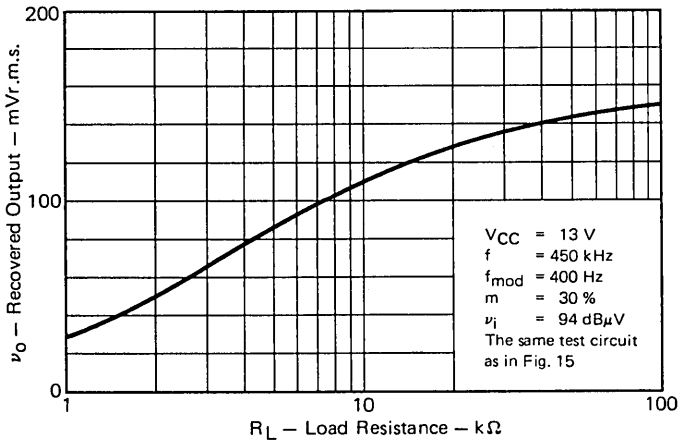


Fig. 18 Recovered Output vs. Load Resistance

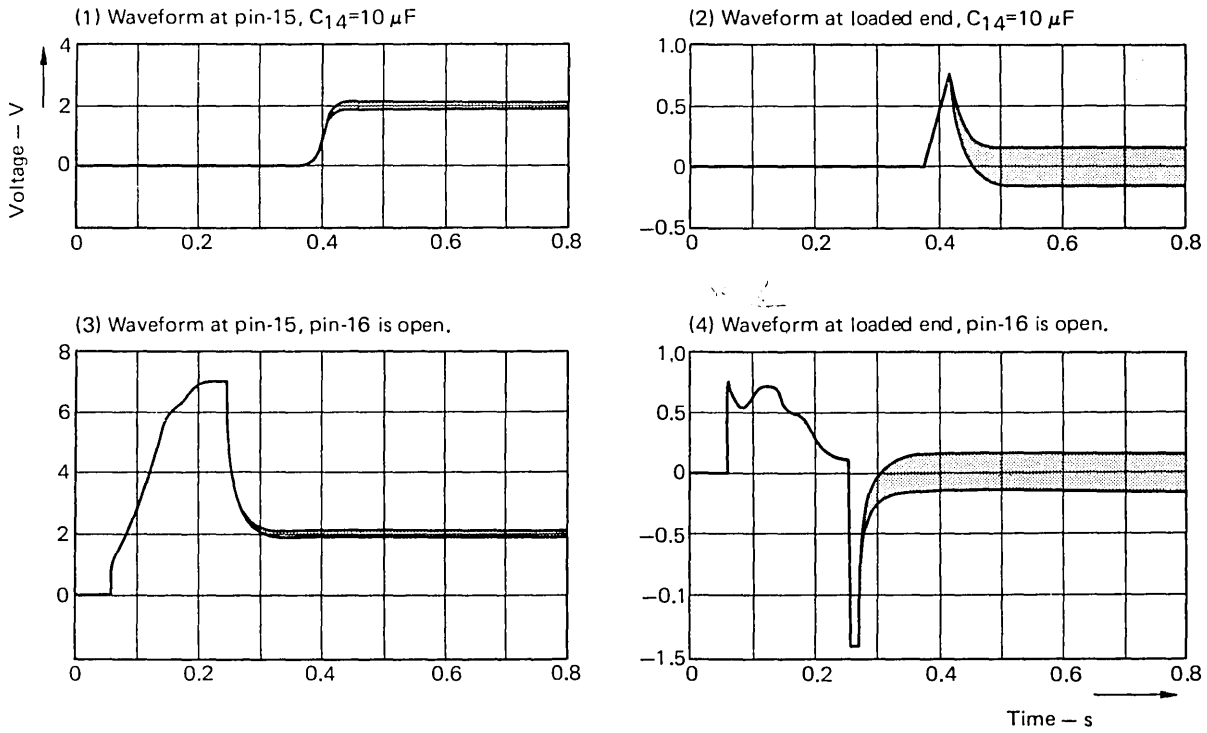


Fig. 19 Switch-on Responce
(V_{CC} = 13 V, f = 1 MHz, f_{mod} = 400 Hz, m = 30 %, ν_i = 74 dBμV, R_L = 10 kΩ TEST CIRCUIT : Fig. 27)

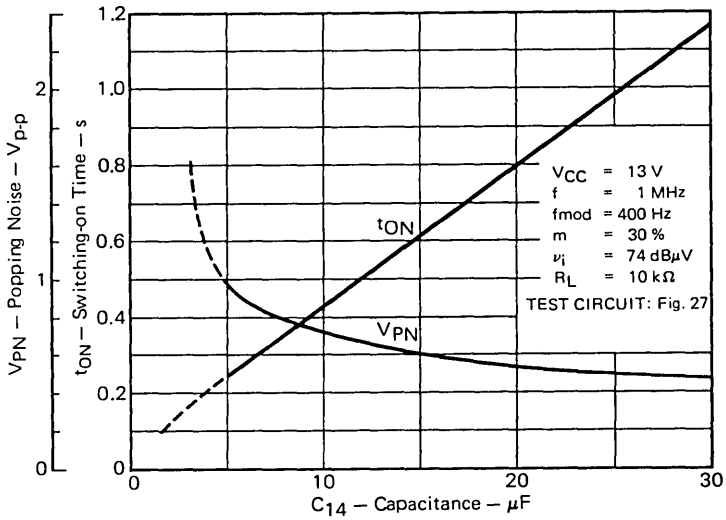


Fig. 20 Relationship of Switch-on Popping Noise and Time to C_{14}

4-5 AGC CIRCUIT

μPC1216V2 has two independent AGC detectors, one working effectively for one-signal reception, another for two-signal (desired and undesired signals) reception. The AGC_1 controls three AGC circuits, two in the RF stage and one in the IF stage, and AGC_2 controls two RF stage AGC circuits.

AGC_1 works on the same principle as that for an AGC adopted in conventional receivers. The difference lies in the detection of AGC_1 voltage. Contrasted with the conventional utilization of detector output as AGC_1 voltage, this IC provides a separate detecting circuit to obtain AGC_1 voltage by rectifying the output of the IF stage before its entrance to the ceramic filter CF_2. This configuration is devised to avoid the widening of tunable region due to large input as well as the possible abnormal operation of AGC_1 circuit due to the use of ceramic filters. Fig. 21 shows the voltage transfer characteristic of the AGC_1 detecting circuit. In this figure, the solid and dashed lines are relationship of AGC_1 voltage V_{17} to input voltage at pin-18 and at the antenna, respectively.

AGC_2 circuit is provided for the protection of the desired signal from the interferences by adjacent signals. For example, assume that the antenna is receiving a distant station at frequency 1 000 kHz with the antenna input of 40 dBμV and there is a interfering station at 1 040 kHz, aparted from the desired frequency by 40 kHz. Fig. 23 shows the interference on the desired signal as a function of the undesired signal strength. In the figure, the solid curve shows how far the desired signal is suppressed with increasing the undesired signal when the desired signal is modulated with 400 Hz 30 %, and the undesired signal is unmodulated. With 22 μF capacitor on pin-5, the output decreases about 5 dB even at the undesired signal of 120 dBμV. However, when AGC_2 circuit is inaction with pin-5 grounded, the output depression is as much as about 20 dB. The dashed curve shows how much interfering signal is output with the increase of undesired signal when the desired signal is unmodulated and the undesired signal is modulated with 400 Hz 30 %. With 22 μF capacitor on pin-5, the desired to interference signal ratio is as much as almost 20 dB even at the undesired signal of 120 dBμV. Whereas, when AGC_2 is not in action, the interference noise output increases with the increase of the undesired signal. The noise output is larger than the desired signal by 10 dB at about 105 dBμV of the undesired signal. Further increase of the undesired signal will saturate the RF amplifier and makes it work as a kind of limiter amplifier, resulting in the decrease of both desired and undesired signal outputs. In other words, if receivers without AGC_2 circuit set close to a transmission antenna of broadcasting station, they will receive this station instead of the desired signal, or produce no sound at all.

The AGC_2 voltage is produced by detecting the output of the frequency converter stage and smoothing it by pin-5. As shown in Fig. 24, when the input signal more than about 94 dBμV comes to pin-6, the voltage V_5 more than 0.6 V is obtained to actuate the AGC_2 circuit.

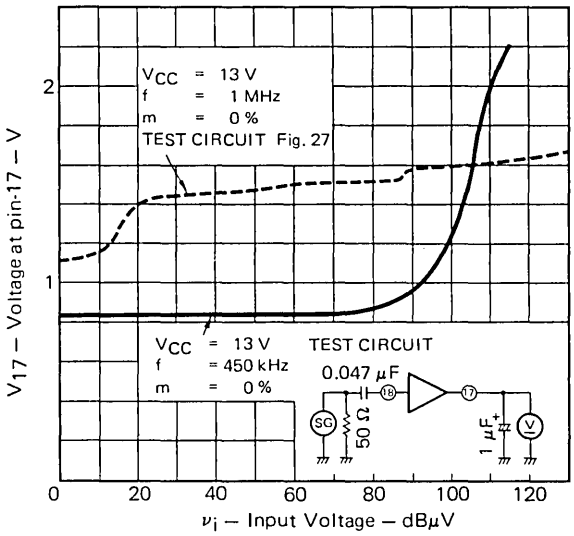


Fig. 21 Voltage Transfer Characteristics of AGC_1 Detector

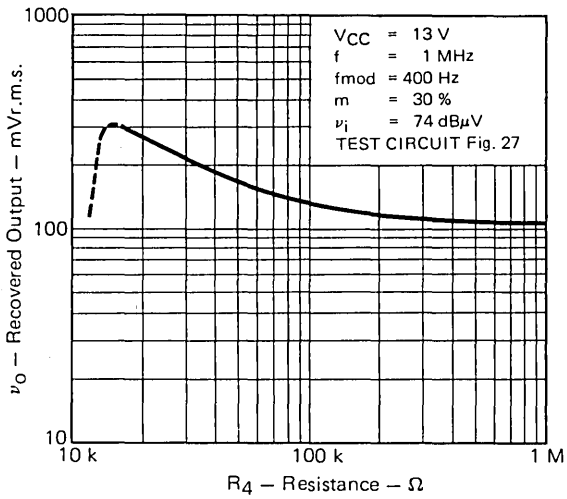


Fig. 22 Recovered Output vs. R_4

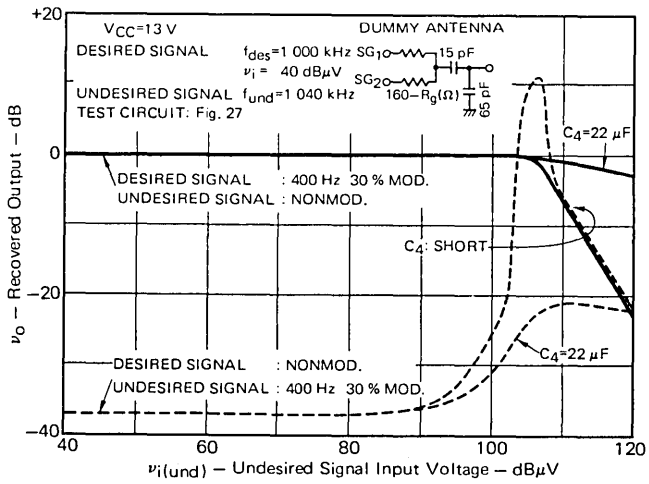


Fig. 23 Two-signal Receiving Characteristics

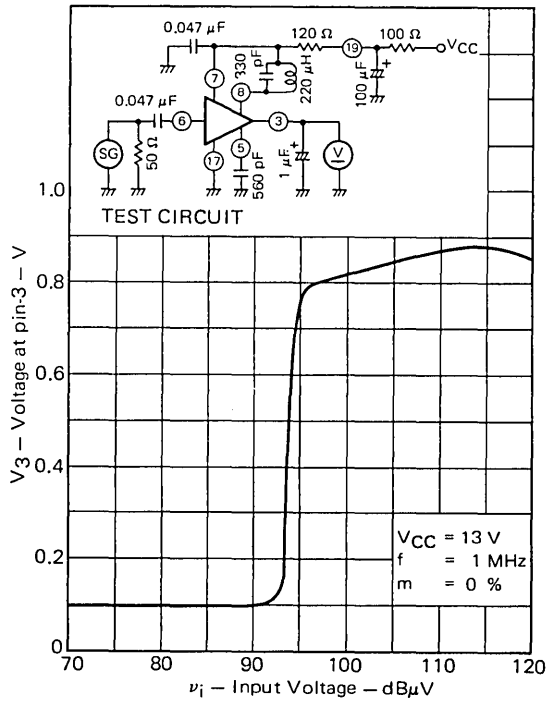


Fig. 24 Voltage Transfer Characteristic of AGC_2 Detector

4-6 OTHERS

Table 2 shows input/output impedance of each stage, and Table 3 DC Voltage of each terminal. Table 4 is a list of external components. The table summarly describes recommended constants and purpose of the external components along with the influences of the change in these constants on the overall characteristics. Fig. 27 shows a typical application of μPC1216V2 which are used to measure overall characteristics.

Table 2 Input and Output Impedance at Terminals

	PIN No.	FUNCTION	TEST FREQ.	TYP.	UNIT
INPUT IMPEDANCE	1	RF AMP.	1 MHz	5.8	kΩ
				34	pF
	6	MIX AMP.	1 MHz	2.5	kΩ
				7	pF
	11	IF AMP.	500 kHz	3.2	kΩ
				4	pF
	14	DET.	500 kHz	2.8	kΩ
				12	pF
	18	AGC_1 DET	500 kHz	7.0	kΩ
				6	pF
OUTPUT IMPEDANCE	12	IF AMP.	450 kHz	160	Ω
				20	pF
	15	DET.	400 Hz	4.3	kΩ

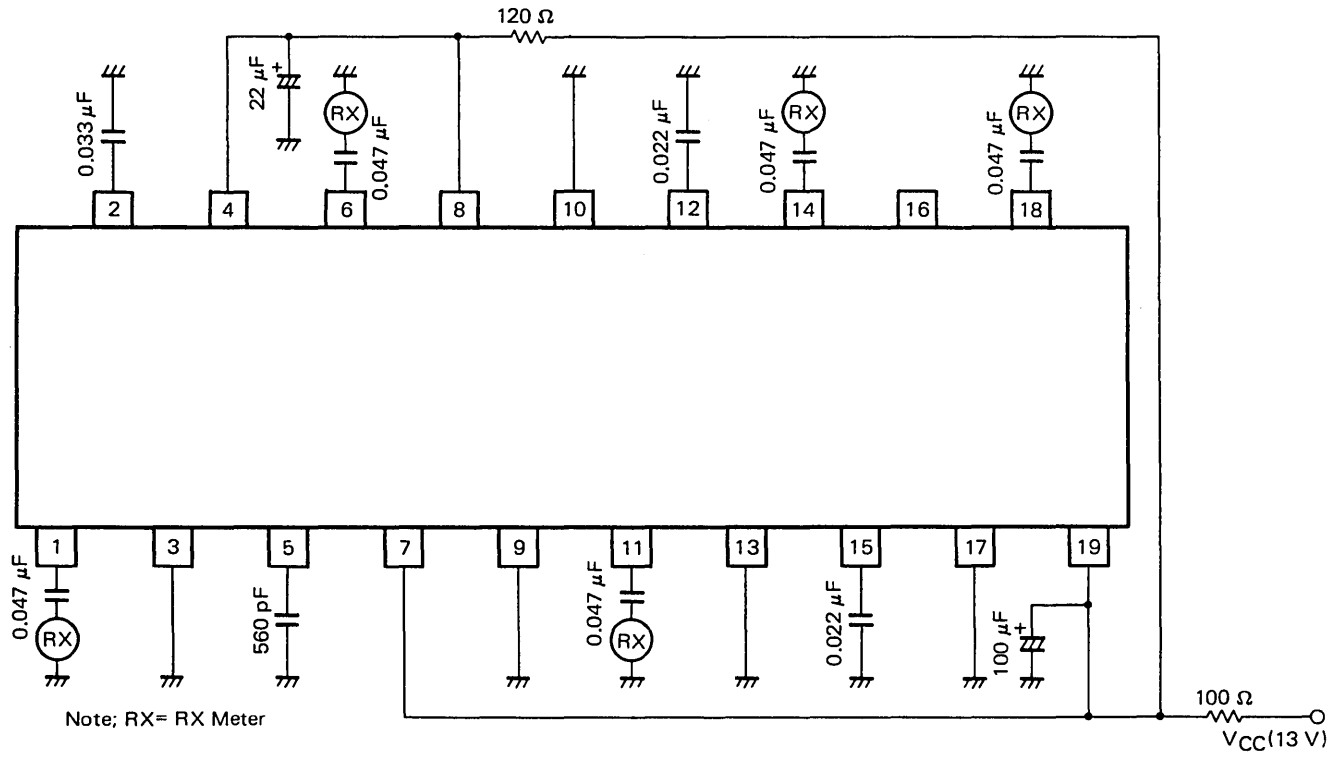
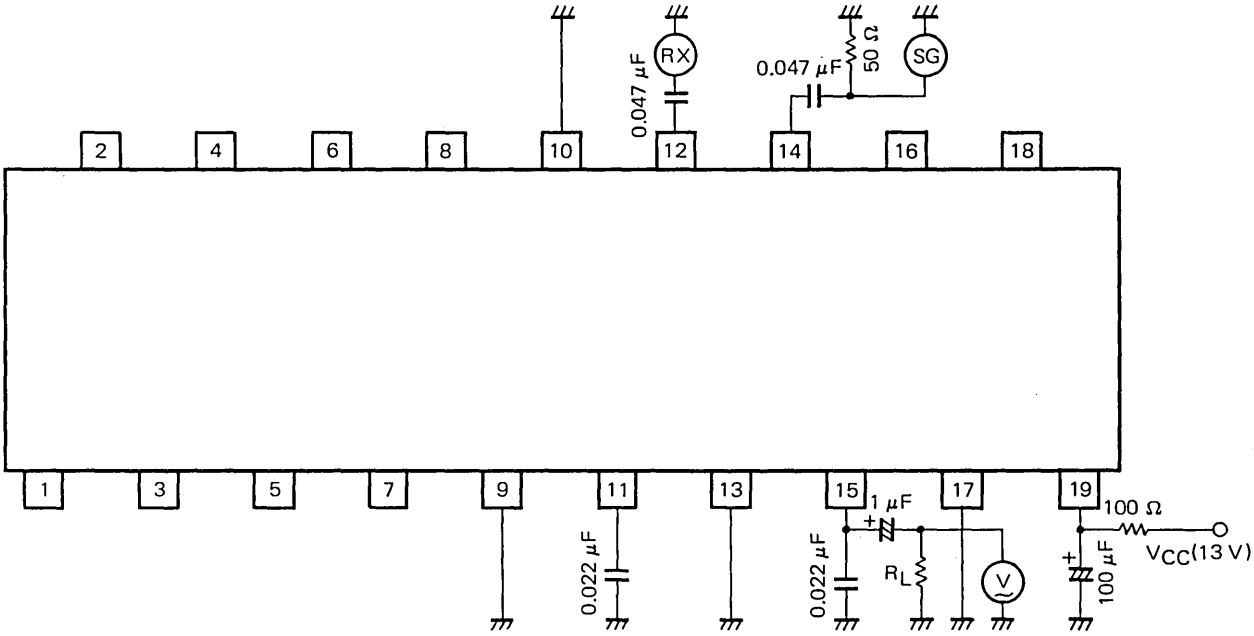


Fig. 25 Input Impedance Test Circuit



Note 1; RX = RX Meter
SG = Signal Generator f=450 kHz, m=30 %, v_i=94 dBμV
V = AC Voltmeter

Note 2; Output impedance at pin-15 is defined equivalently as the R_L which gives an output 6 dB lower than the output voltage that will be obtained for $R_L=\infty$.

Fig. 26 Output Impedance Test Circuit

Table 3 DC Voltage on Terminals (Test circuit : Fig. 27)

PIN No.	1	3	5	7	9	11	13	15	17	19
VOLTAGE (V)	2.8	0	1.3	11	0	3.5	1.1	1.8	1.1	11.5
PIN No.	2	4	6	8	10	12	14	16	18	
VOLTAGE (V)	2.0	11	2.0	11	0	3	9	3	9	

Table 4 External Components List

Comp. No.	Recom. Const.	Function	What happens if the constant is		Remarks
			larger than Recom. Const.	smaller than Recom. Const.	
L_{T1}		ANT Resonance			NIPPON TUNER 5M-S
L_{T2}		RF. Resonance			
L_{T3}		LO. Resonance			
C_{T1}	(50 pF)	ANT. Trimmer			
C_{T2}	(50 pF)	RF. Trimmer			
C_{T3}	(50 pF)	LO. Trimmer			
T_1	220 μH	LO. Coil			7BR-6103A (TOKO)
T_2		Selectivity			7MC-6104N (TOKO)
CF1		Selectivity			SFZ450GL (MURATA)
C_{F2}		Selectivity			SFU450A (MURATA)
L_1	4.7 μH	Noise Reduction	Large Tracking Error	Effect reduced	
L_2	5.6 μH	Tracking	Large Tracking Error	Large Tracking Error	
C_1	0.01 μF	ANT. Coupling	ANT. Gain increased	ANT. Gain decreased	
C_2	3 300 pF	ANT. Resonance	ANT. Gain decreased	Usa. Sens. decreased	
C_3	0.033 μF	RF. Bypass	Increased Intermod	Gain decreased	
C_4	22 μF	AGC_2 Smoothing	AGC_2 Delay increased	T.H.D. increased	
C_5	30 pF	RF. Resonance			
C_6	560 pF	Freq. Char. Compensation	MIX. Gain increased	MIX. Gain decreased	See Fig. 9
C_7	22 μF	Ripple Filter	SVRR decreased	Tweet increased	SVRR; Supply Voltage Ripple Rejection
C_8	100 pF	Coupling	Gain increased	Gain decreased	
C_9	2 200 pF	Cap. Tap with C_8	Gain decreased	Gain increased	
C_{10}	220 pF	LO. Resonance			
C_{11}	22 μF	AGC_1 Smoothing	AGC_1 Delay increased	T.H.D. increased	
C_{12}	0.01 μF	Coupling			
C_{13}	0.022 μF	Output Smoothing	Hi-Freq. cutoff	S/N increased	
C_{14}	10 μF	SW-ON Muting	Long Muting Time	Pop-noise increased	See Fig. 20
C_{15}	3.3 μF	AGC_1 Smoothing	AGC_1 Delay increased	T.H.D. increased	
C_{16}	100 μF	Ripple Filter	SW-ON Time increased	SVRR decreased	
C_{17}	1 μF	Coupling	SW-ON Time increased	Lo-Freq. cutoff	
R_1	4.7 kΩ	Noise Reduction	Effect reduced	Q (ANT.) decreased	
R_2	120 Ω	Ripple Filter	$V_{CC(min.)}$ increased	SVRR decreased	
R_3	3.3 kΩ	Impedance Matching	fo(CF) deviated	Loss increased	
R_4		Output Compensation		$V_{CC(min.)}$ increased	See Fig. 22
R_5	100 Ω	Ripple Filter	$V_{CC(min.)}$ increased	SVRR decreased	

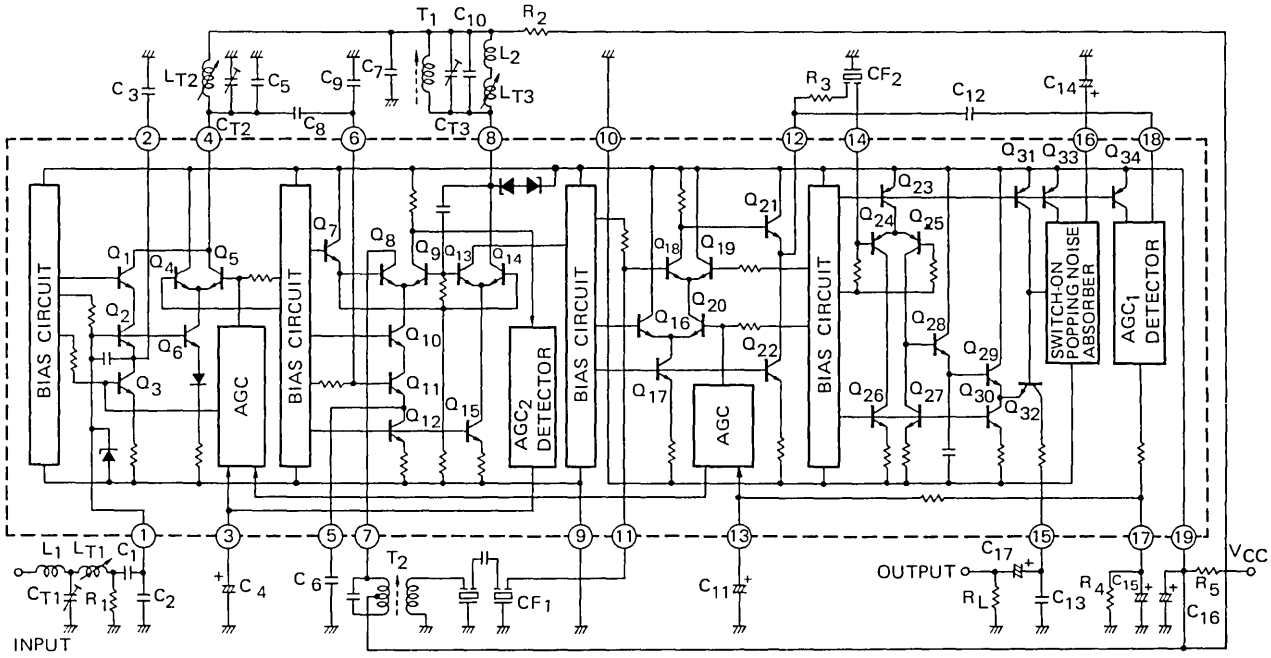
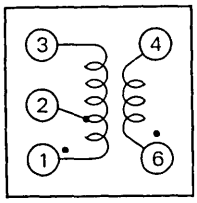


Fig. 27 Test Circuit of Overall Characteristic

COIL DATA

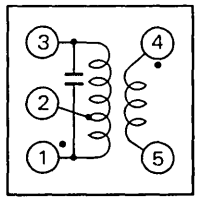
T1: Oscillator Coil 7BR-6103A (TOKO INC.)



①-② ②-③ ④-⑥
8T 70T 20T

L=220 μH ± 6 %
Q_U= over 80 (796 kHz)

T2: IF Transformer 7MC-6104N (TOKO INC.)



①-② ②-③ ④-⑥
73T 73T 10T

f_T=455 kHz ± 3 %
Q_U=115 ± 20 %
C_T=180 pF

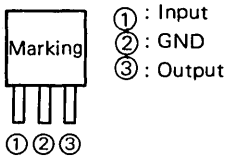
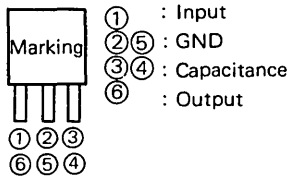
Tuner : NIHON TUNER CO. made 5M-S

Minimum Frequency Cover Range 525 ~ 1 615 kHz

Tuning Capacitor

ANT Coil	150 pF
RF Coil	150 pF
OSC Coil	450 pF

CERAMIC FILTER (MURATA Co.)

CHARACTERISTIC		SFU450A3	SFZ450GL3
Center Frequency		450 kHz	450 kHz
3 dB Band Width		10 kHz	6.5 kHz
Selectivity	−9 kHz	7.5 dB	20 dB
	+9 kHz	5.5 dB	20 dB
Insertion Loss		3 dB	3 dB
			

5. APPLICATION WITHOUT IFT

Fig. 28 shows an example of circuit applied to an AM tuner that does not use IFT's which need adjustments. Fig. 29 to Fig. 34 show its characteristics. Usually, an IFT is connected to the output pin-7 of the frequency converter stage and the adjustment of this IFT is needed. This part is changed to a combination of fixed inductance and capacitance, and the adjustment-free IF amplifier stage is achieved.

Recently various types of ceramic filters are put on the market by many makers. An appropriate selection of ceramic filters suitable for the intended use can produce AM tuners having a variety of characteristics with one type of circuitry, and it will contribute to further labor cost reduction, miniaturization, or cost down.

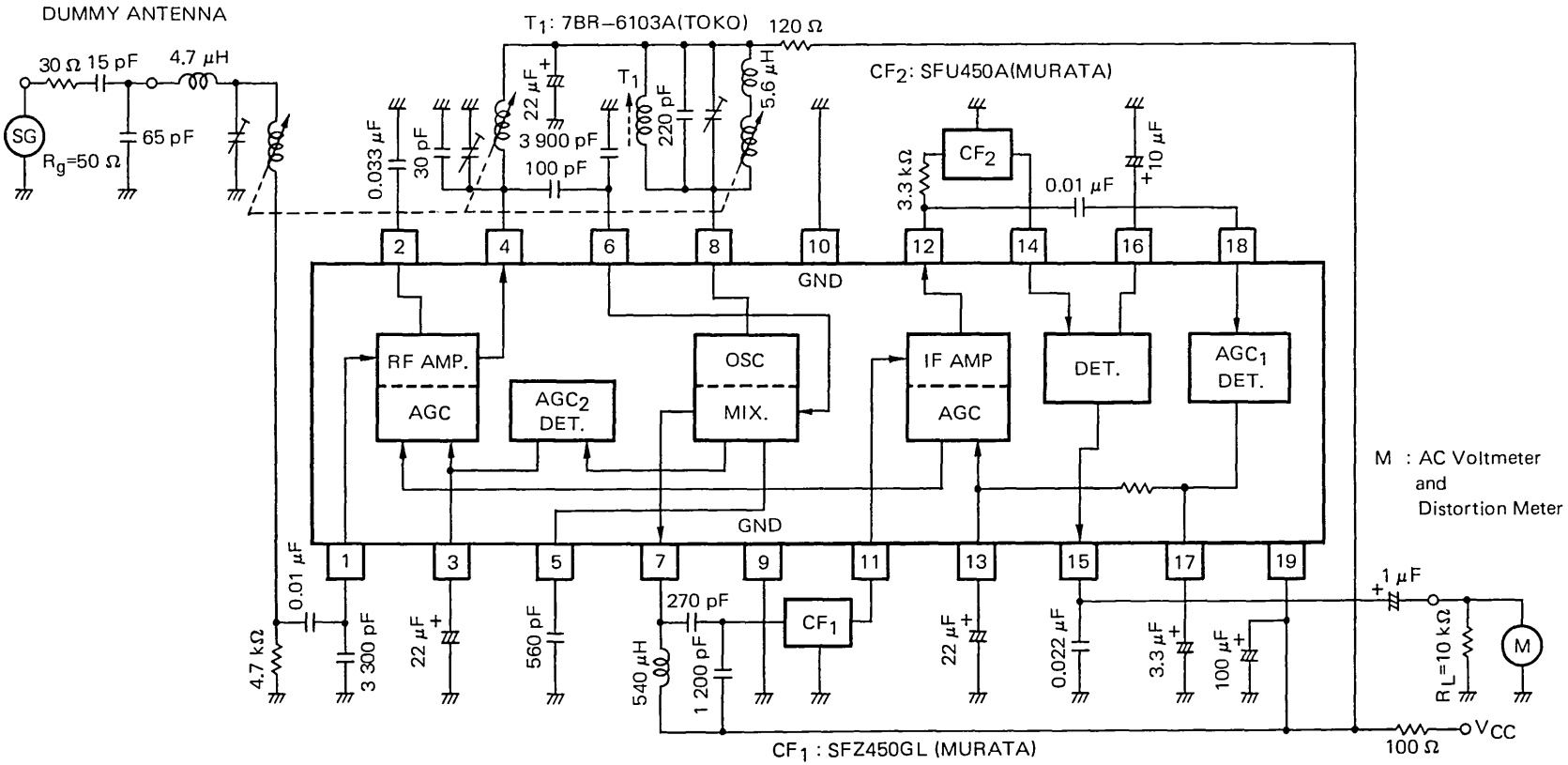


Fig. 28 Application without IFT and Test Circuit

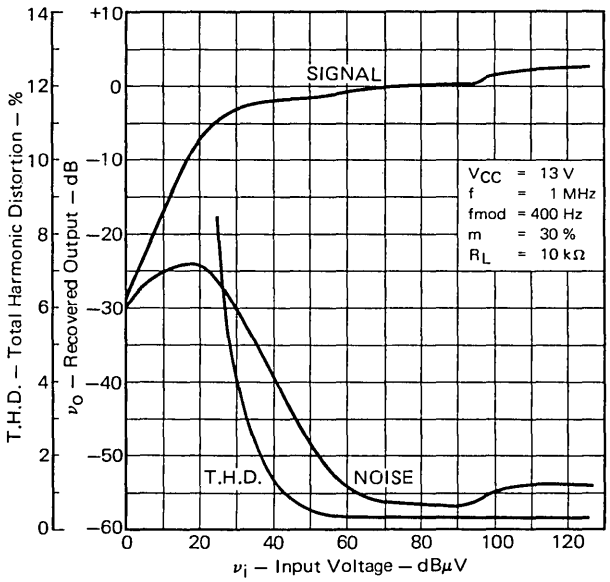


Fig. 29 Recovered Output and Total Harmonic Distortion vs. Input Voltage

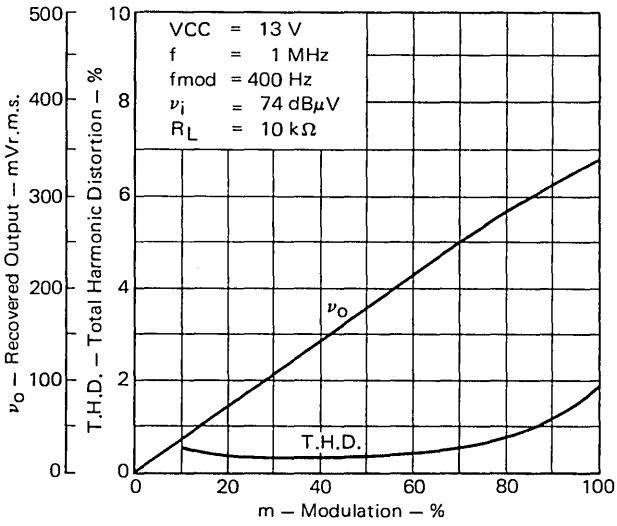


Fig. 30 Recovered Output and Total Harmonic Distortion vs. Modulation

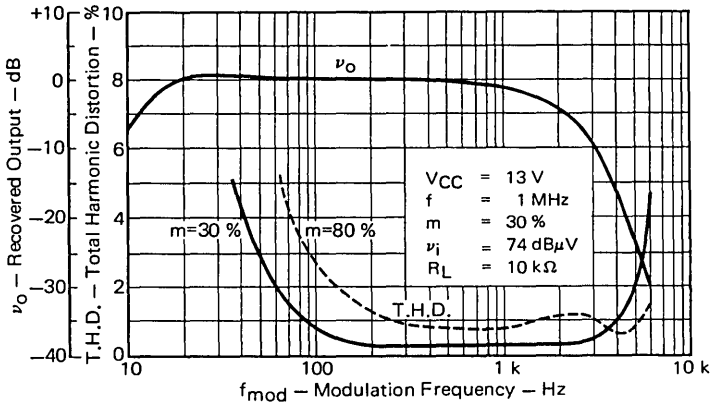


Fig. 31 Electrical Fidelity

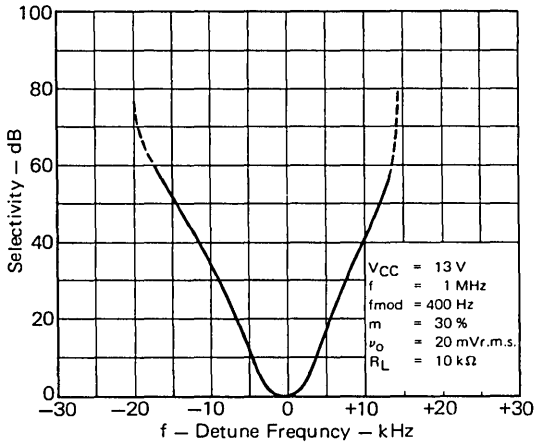


Fig. 32 One-signal Selectivity

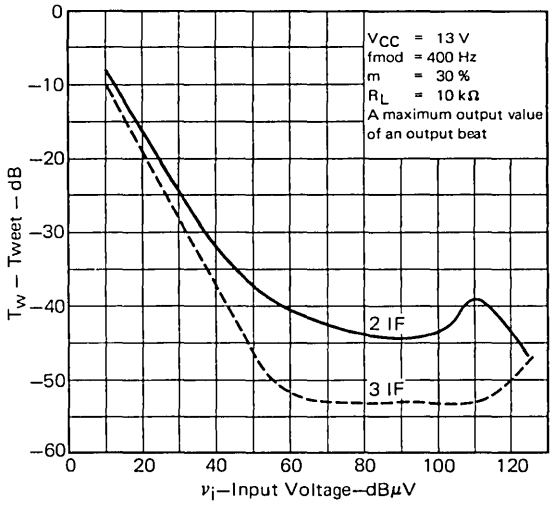


Fig. 33 Tweet Characteristics

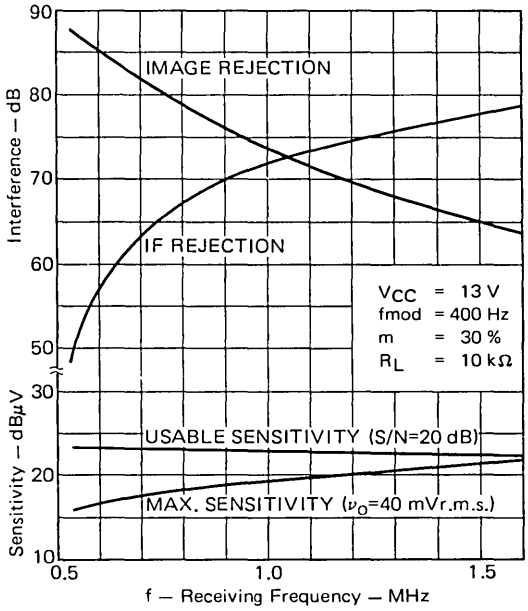
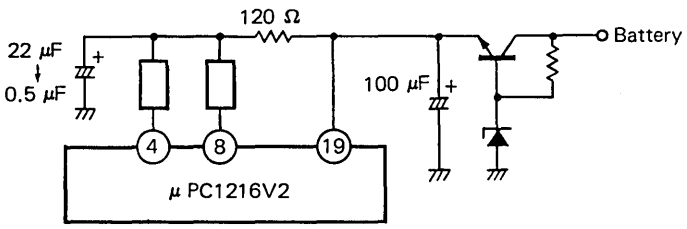


Fig. 34 Receiving Frequency Characteristics

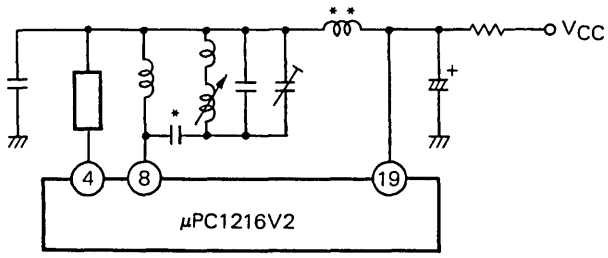
6. CAUTION

6-1. Don't earth the pin-4, pin-8 or power line connected with these pins by mistake. If this is done, the IC may be damaged.

6-2. When the resistance (100 Ω) is not used between pin-19 and battery, the capacitance (22 μF) of RF stage power line should be change for less than 0.5 μF.



(Safety precaution)
The following application is recommended to keep away the above problems.



* Add a capacitor (0.01 μF) between pin-8 and the tuning coil.
** Replace the resistor R_2 (120 Ω) with a coil (22 μH).

6-3. The C_6 should be changed the constant more than 3 300 pF in a long wave application. If the constant is 560 pF, the conversion gain and maximum sensitivity may be insufficient.

6-4. The oscillation amplitude at pin-8 should be more than 3 Vp-p. if not, the deviation of maximum sensitivity will be increase.

6-5. Connect the C_{10} and C_{T3} with the power line instead of GND. If not, some IC's will not oscillate.

6-6. The ceramic filter CF_1 should be selected so that an oscillation signal leakage may be small. A large leakage ceramic filter causes maximum sensitivity drop in appearance, because the AGC circuit operates with the leakage.

6-7. The center tap of IFT T_2 should be used so that the good performance can be obtained at lower supply voltage.

7. DIFFERENCES BETWEEN μPC1216V and μPC1216V2

7-1. The μPC1216V2 is improved in the supply voltage dependencies of detector output voltage, maximum sensitivity and local frequency. (See Fig. 35)

7-2. The μPC1216V2 is improved in the temperature dependencies of detector output voltage and maximum sensitivity. (See Fig. 36)

7-3. The resistance R_4 is not necessary in μPC1216V2 application.

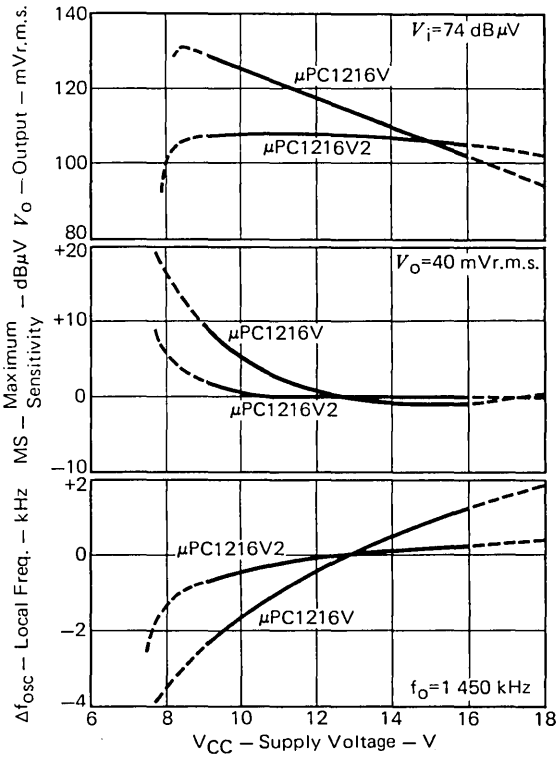


Fig. 35 Supply Voltage Dependencies (f=1 MHz, fmod=400 Hz, m=30 %)

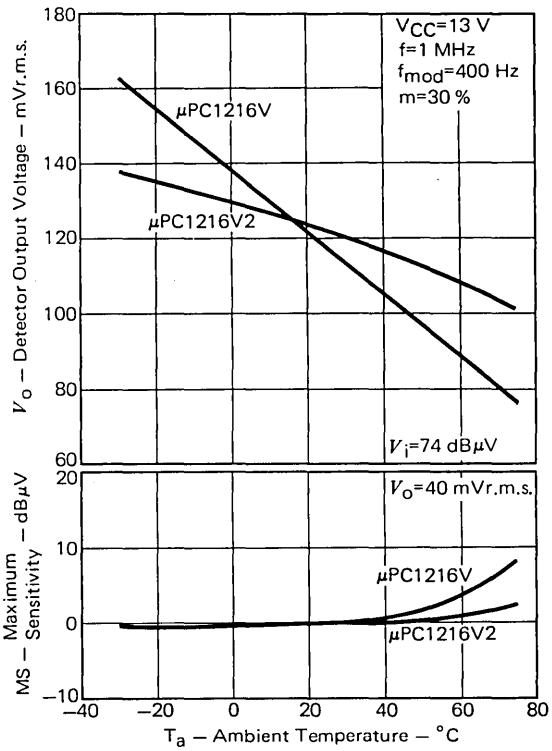


Fig. 36 Ambient Temperature Dependencies

DIFFERENTIAL PEAK FM DETECTOR μPC1028H

1. INTRODUCTION

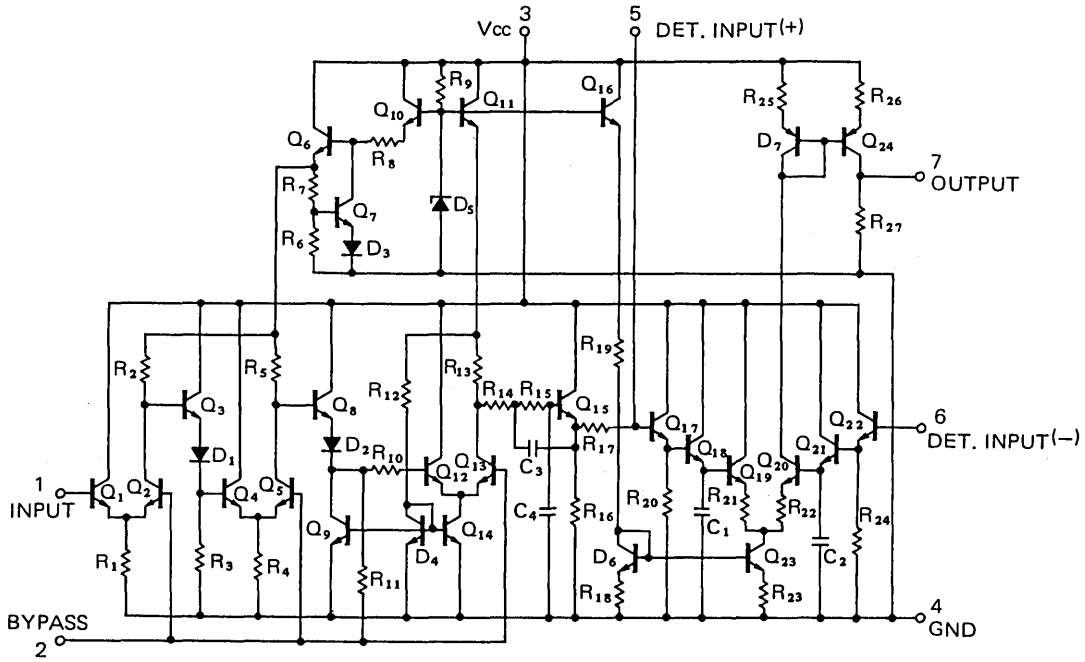
The μPC1028H is a silicon monolithic integrated circuit intended for an FM IF amplifier with a differential peak detector. This detection system is required minimum external components, is easy to adjust and is of cheap overall cost, compared with the other FM detection systems such as the ratio detector, the Foster-Seeley detector, the quadrature detector and so on.

The μPC1028H contains a three-stage direct coupled differential amplifier, a low-pass filter, a differential peak detector and a regulator.

Outline is a 7-lead single in-line package, so that it is suitable for use in automotive radio receivers, where small mounting space is required.

2. DESCRIPTION OF INTERNAL CIRCUIT

Fig. 1 Equivalent Circuit



2-1 FM-IF AMPLIFIER AND LIMITER SECTION

The intermediate frequency (IF) signal taken out from the front end section, passes through the selection devices connected between the front end and IF section, and is applied to the input terminal of the μPC1028H. It is amplified by the differential amplifier Q_1 to Q_5 and Q_{12}, Q_{13} through the emitter follower Q_8. In order to obtain excellent limiting characteristics, the differential amplifier Q_{12} and Q_{13} is of transistor current sink structure. The limiting sensitivity $v_{i\,(lim)}$ of the μPC1028H is 48dBμV TYP. When the level of the IF signal exceeds 48dBμV, the differential amplifier Q_{12} and Q_{13} is pushed into the limiting region and starts limiting action. When the level of the IF signal increases further, not only the differential amplifier Q_{12} and Q_{13}, but the differential amplifier Q_4 and Q_5, and at further higher levels the differential amplifier Q_1 and Q_2 is pushed into the limiter region and the effect of the limiting action is improved.

2-2 LOW-PASS FILTER SECTION

The IF signal amplified by the FM-IF and limiter section contains high harmonic frequency components of the IF signal. These high frequency components are sufficiently attenuated by the low-pass filter composed of R_{14}, R_{15}, R_{16}, C_3 and C_4.

2-3 DIFFERENTIAL PEAK DETECTOR SECTION

After high frequency components are eliminated by the low-pass filter section the IF signal is injected into the FM detector circuit Q_{17} to Q_{23}, through the emitter follower transistor Q_{15}. On the other hand, the IF signal is injected from Q_{15} to the LC circuit; a single tuned coil connected between pin 5 and pin 6, and a capacitor connected between pin 6 and GND. Then the IF signal is transformed into the AM component proportional to a certain frequency deviation, due to the characteristics of the LC circuit. The AM signal is injected into Q_{18} and Q_{21} through the buffer amplifier Q_{17} and Q_{22}. The Q_{18} and Q_{21} work in class AB to half-wave rectify the AM signal. That is, the AM signal is peak detected and smoothed by capacitors C_1 and C_2. The signal which has been turned into a smoothed audio frequency component is amplified by differential amplifier Q_{19} and Q_{20}, and the output is taken out from pin 7 through Q_{24}.

2-4 VOLTAGE REGULATOR

The constant voltage is composed by Q_6, Q_7, Q_{10}, Q_{11}, Q_{16} and D_3 with the standard voltage of Zener diode D_5, and supplies stable bias to the IF amplifier and the detector sections.

3. CHARACTERISTICS

As shown in Fig. 2, the −3dB limiting sensitivity of the μPC1028H is 48dBμV TYP.. The gain distribution of the automotive radio receivers is devised so that a limiting sensitivity of about 10dB will be obtained, when a front end of about 30dB gain, two ceramic filters and one transistor to recover the filter loss are used before the μPC1028H.

The μPC1028H alone shows the excellent characteristics of 0.1% TYP. distortion factor with 30% modulation and 80dBμV input voltage, and 0.3% TYP. distortion factor with 100% modulation. S/N of 65dB TYP. can be obtained.

An AM rejection ratio is 40dB TYP. and 50dB TYP. with AM component of 30%, and a FM component of 30% (±22.5kHz) and 100% (±75kHz) respectively.

Fig. 2 DETECTOR OUTPUT VOLTAGE, AM REJECTION, TOTAL HARMONIC DISTORTION, SN RATIO vs. INPUT VOLTAGE

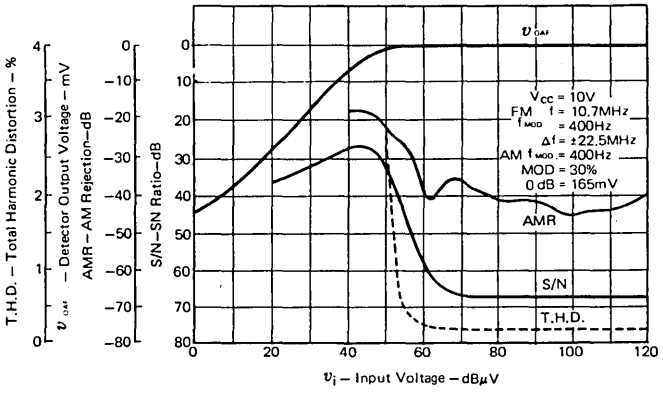
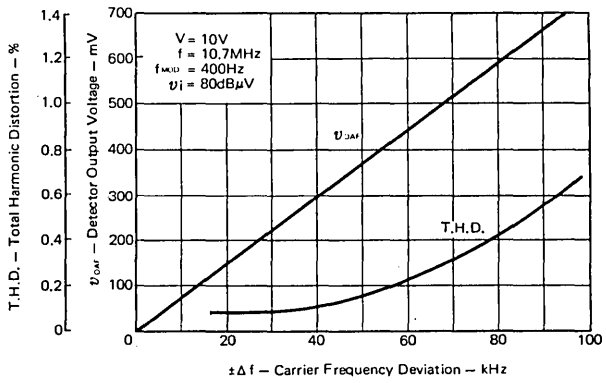


Fig. 3 DETECTOR OUTPUT VOLTAGE, TOTAL HARMONIC DISTORTION vs. CARRIER FREQUENCY DEVIATION



The modulation (modulation frequency deviation) versus detector output characteristics are shown in Fig. 3, the detector shows a high output of 165mV TYP. with 30% modulation, and 550mV TYP. with 100% modulation.

In Fig. 4, the detector output versus modulation frequency characteristic is shown. When applying de-emphasis at the output of the μPC1028H, de-emphasis characteristic of 75 μs can be obtained by connecting a 0.01μF capacitor between pin 7 and GND in combination with the internal impedance. When FM stereo demodulation IC (MPX) is to be used after the μPC1028H, a capacitor of 100 to 200pF should be connected between pin 7 and GND to eliminate the high frequency components of the carrier, and de-emphasis should be applied at the output of the MPX IC.

Fig. 4 DETECTOR OUTPUT VOLTAGE vs. MODULATION FREQUENCY

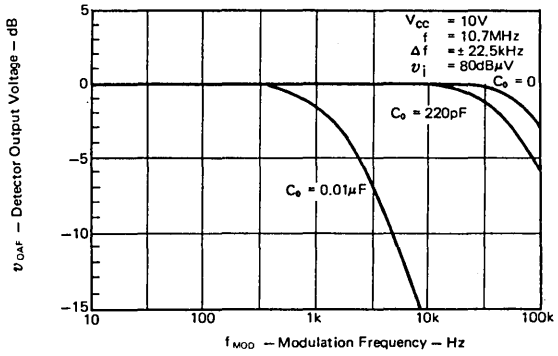


Fig. 5 shows DC output voltage of pin 7 (V_7) versus frequency, and V_7 at 10.7MHz is 3.5V TYP.. This DC output can be utilized as the AFC voltage.

Fig. 5 S-CURVE

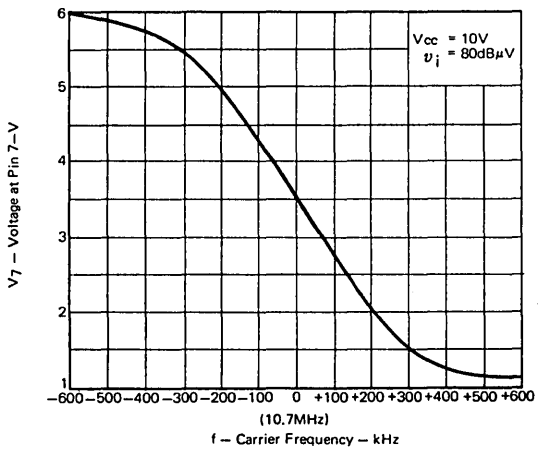
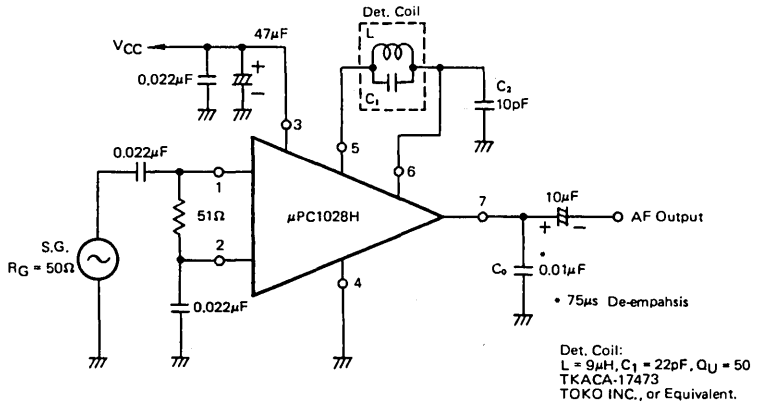
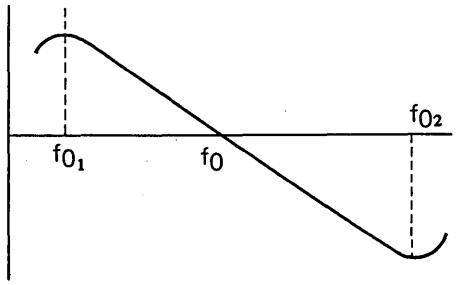


Fig. 6 TEST CIRCUIT



The peak frequencies of Fig. 6 can be determined from the following equations.



$$f_{01} = \frac{1}{2\pi\sqrt{L\,(C_1 + C_2)}}$$

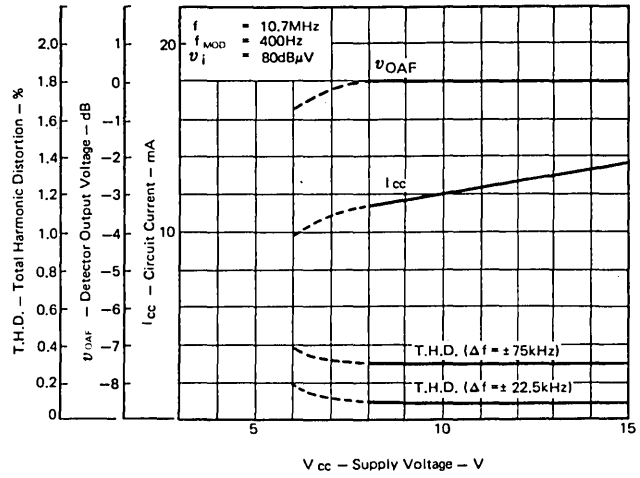
$$f_0 = \frac{1}{2\pi\sqrt{L\,(C_1 + \frac{C_2}{2})}}$$

$$f_{02} = \frac{1}{2\pi\sqrt{LC_1}}$$

f_{01} is the series resonant frequency and gives the lower peak frequency, f_{02} is the parallel resonant frequency and gives the upper peak frequency, f_0 shows the center frequency.

Fig. 7 shows the power supply voltage dependencies of the μPC1028H. The characteristics indicate that operation at 6 or 7V is possible, but giving a safety margin, the recommended operating range has been made 8 to 15V.

Fig. 7 TOTAL HARMONIC DISTORTION, DETECTOR OUTPUT VOLTAGE, CIRCUIT CURRENT vs. SUPPLY VOLTAGE



As can be seen in Fig. 7, the characteristics are smooth and without irregularities within the recommended voltage range, giving stable operation.

Fig. 8 shows the temperature dependencies of the μPC1028H. The circuit of the μPC1028H is designed so that the temperature dependencies have been kept to a minimum.

Fig. 8 LIMITTING SENSITIVITY, DETECTOR OUTPUT VOLTAGE vs. AMBIENT TEMPERATURE

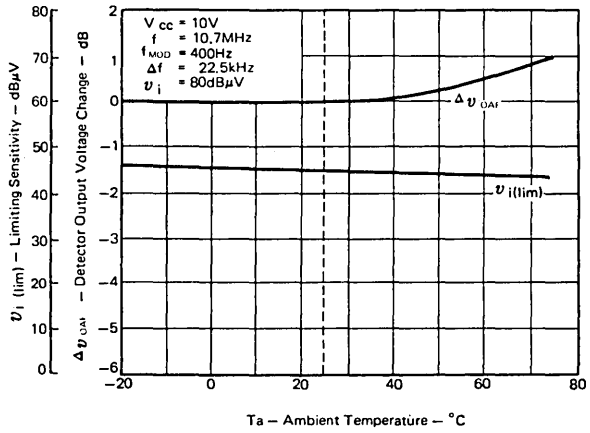
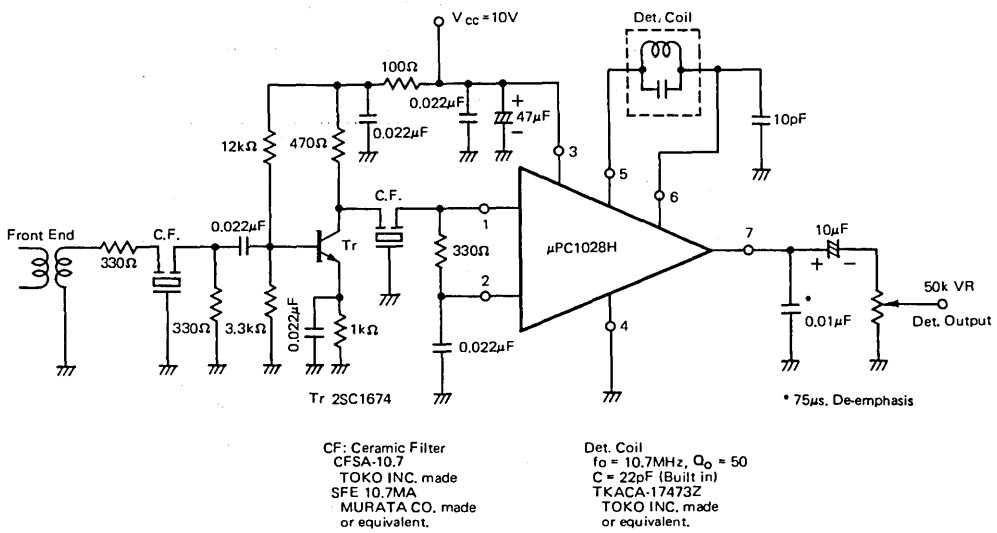


Fig. 9 TYPICAL APPLICATION



One of the application circuits of the μPC1028H is shown in Fig. 9. Two 10.7MHz ceramic filter elements (insertion loss of one element: 12dB) are employed in the stage before the μPC1028H, and the insertion loss of the filter elements is compensated with a transistor. The gain of the filter stage is established at about +6dB, and when a front end of 30 to 35dB gain used, a FM tuner of about 10dB limiting level (−3dB point) can be obtained.

A 0.01μF capacitor is connected to output pin 7 in order to obtain a de-emphasis characteristic of 75μs. When a FM MPX is connected after the μPC1028H, this capacitor should be of 100 to 200pF, and de-emphasis should be applied to the output of the FM MPX.

Typical characteristics of the application circuit of Fig. 9 are shown in Fig. 10 and Fig. 11 for reference.

Fig. 10 v_{OAF}, $v_{i(lim)}$, AMR, T.H.D., S/N, vs. v_i

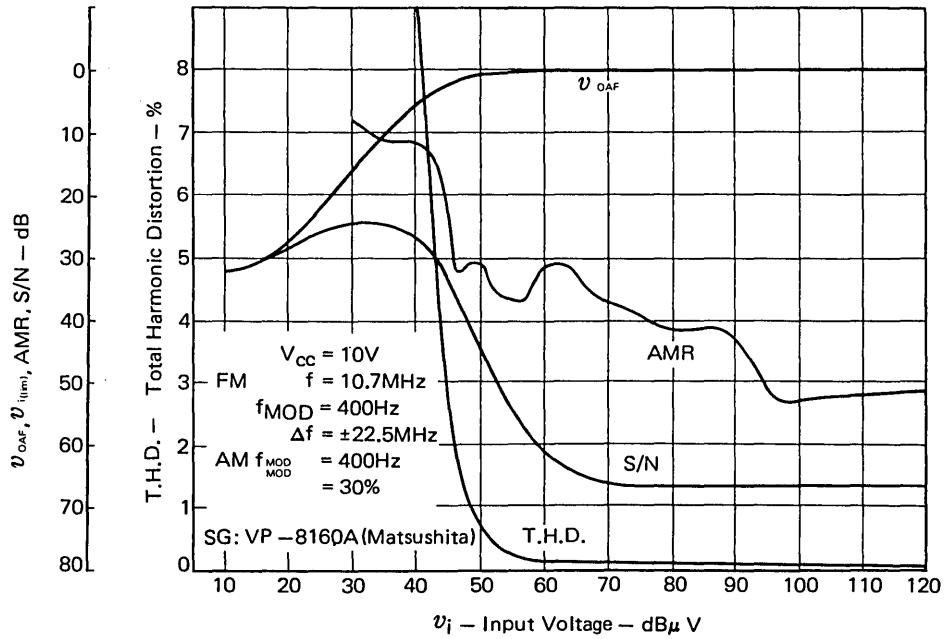
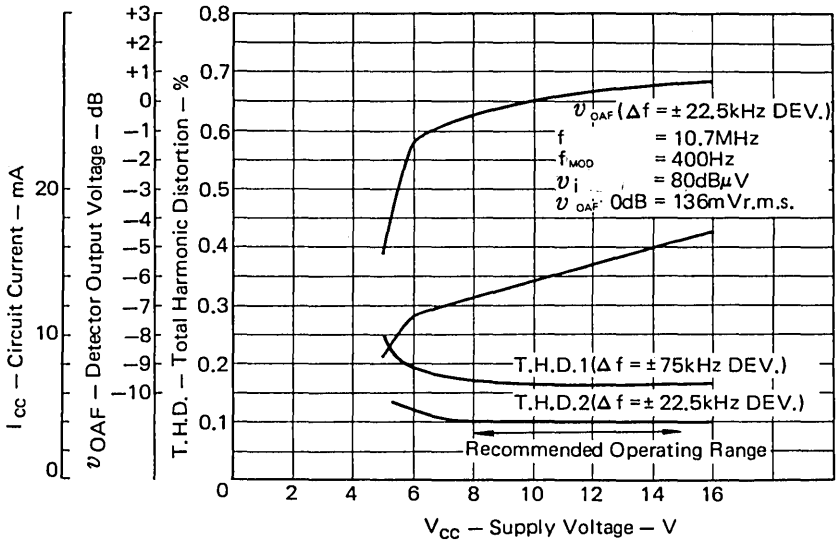


Fig. 11 v_{OAF}, I_{CC}, T.H.D. vs. V_{CC}



APPLICATION OF μPC1200V FM-IF IC FOR CAR RADIO

1. INTRODUCTION

μPC1200V is an FM-IF amplifier employing a quadrature detector.

The IC utilizes a new type of muting circuit to sufficiently reduce white noises from weak signals, detuning noises and side detection outputs occurring in both tuning and detuning. Consequently, this device can combine with an FM noise canceller without causing malfunction of the canceller due to white noises to lead to degradation in characteristics of both devices, thus achieving full performance of the canceller. Unlike ones with conventional muting methods, the IC produces greater outputs as the tuning point is approached, making selection of a program easy.

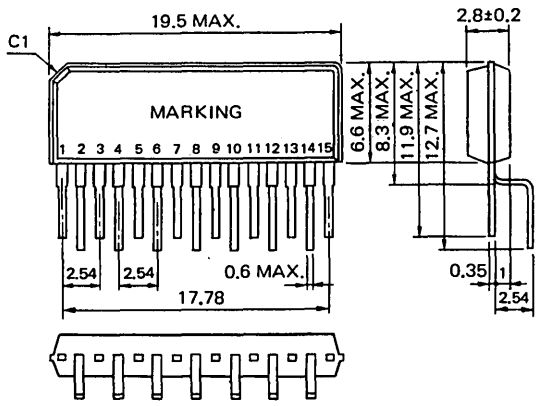
The package is the newly developed 15-pin V-DIP, which greatly reduces mounting area and meets requirements of car radios which calls for high density mounting of parts.

2. FEATURES

- Low undesirable noise level : −60 dB
- Very low lateral uncomfortable sound either upper or lower from the tuning point.
- Capability for effective use of FM noise canceller.
- Occupation of minimum area in P.C. Board.
- Easy to handle because of its V-DIP construction.
- Free of mismounting in P.C. Board due to its lead tuning point.
- Wide range of power supplies : 7 to 12 V

3. GENERAL SPECIFICATION

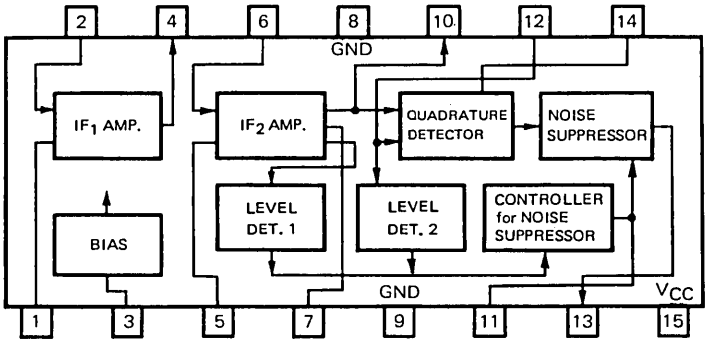
PACKAGE DIMENSION (in millimeters) (Fig. 1)



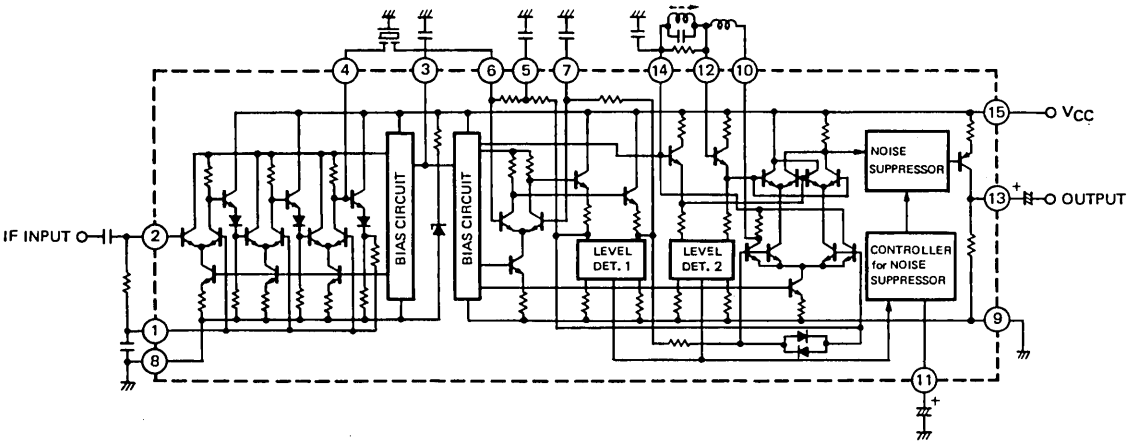
CONNECTION DIAGRAM

Pin No.	Electrical Connection	Pin No.	Electrical Connection
1	BYPASS	2	IF_1 INPUT
3	BYPASS	4	IF_1 OUTPUT
5	BYPASS	6	IF_2 INPUT
7	BYPASS	8	GND
9	GND	10	IF_2 OUTPUT
11	N.S. CONTROL	12	DETECTOR INPUT
13	AUDIO OUTPUT	14	BYPASS
15	V_{CC}		

BLOCK DIAGRAM (Top View) (Fig. 2)



EQUIVALENT CIRCUIT (Fig. 3)



ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Supply Voltage	V_{CC}	15	V
Input Voltage	V_i	3	Vp-p
Package Dissipation at T_a=75 °C	P_d	310	mW
Operating Temperature	T_{opt}	−30 to 75	°C
Storage Temperature	Tstg	−40 to 125	°C

RECOMMENDED OPERATING CONDITIONS (T_a=25 °C)

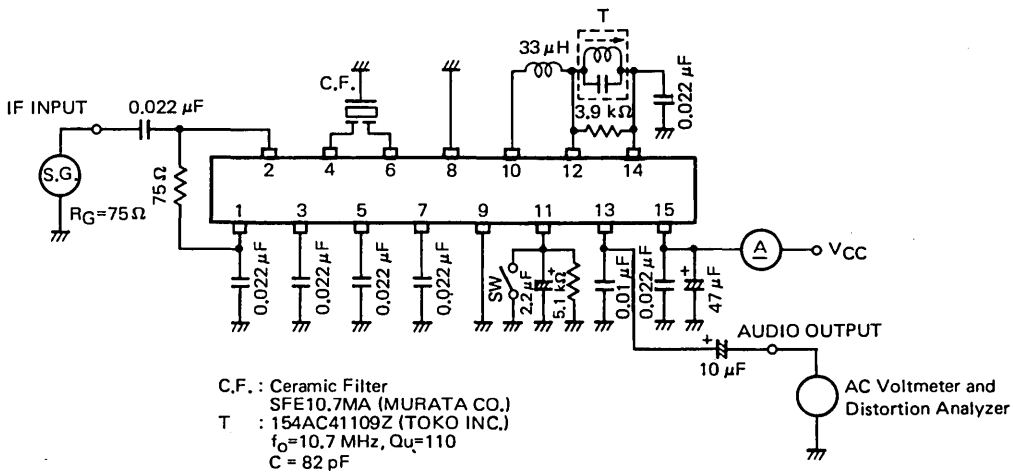
Operating Supply Voltage	V_{CC}	10	V
Supply Voltage Range	V_{CC}	7 to 12	V
Operating Ambient Temperature	T_a	−30 to 75	°C

ELECTRICAL CHARACTERISTICS

(T_a=25 °C, V_{CC}=10 V, f=10.7 MHz, $f_{mod.}$=400 Hz, DEV.=±22.5 kHz)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	I_{CC}	12	19	25	mA	v_i=0 dBμV
Limiting Sensitivity (1)	$v_{i(lim)1}$		47	53	dBμV	−3 dB point, SW : ON
Recovered Audio Voltage	v_o	110	150	200	$mV_{r.m.s.}$	v_i=100 dBμV
AM Rejection	AMR		45		dB	v_i=100 dBμV, AM: $f_{mod.}$=400 Hz, m=30 %
Signal-to-Noise Ratio	S/N		67		dB	v_i=100 dBμV
Total Harmonic Distortion	T.H.D.		0.1	0.5	%	v_i=100 dBμV
Limiting Sensitivity (2)	$v_{i(lim)2}$		50		dBμV	−3 dB point, SW : OFF

TEST CIRCUIT (Fig. 4)



4. DESCRIPTION OF OPERATION

(1) IF Amplifier and Limiter

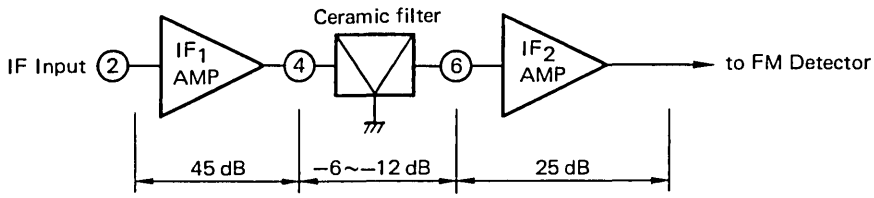


Fig. 5 Block Diagram of IF Amplifier

Intermediate frequency (IF) signals delivered from the front end section is supplied, through a selecting device, to pin 2 of the μPC1200V to be amplified by IF_1 AMP and IF_2 AMP, which consist, respectively, of a three-stage differential amplifiers with 45 dB in voltage gain (R_L=330 Ω) and a single stage differential amplifier with 25 dB in voltage gain (R_L=1 kΩ).

The ceramic filter inserted between pins 4 and 6 is effective in improving signal-to-noise ratios (S/N) and usable sensitivity of a radio receiver. This is because wide bandwidth noises are all amplified by the front end and IF_1 AMP before they are limited to within a bandwidth specified by the ceramic filter. The narrower this bandwidth is, the higher the S/N ratio becomes, ($Vn \propto 1/\sqrt{BW}$).

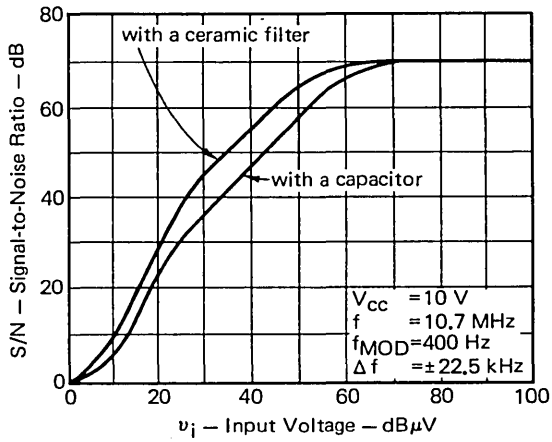


Fig. 6 Signal-to-Noise Ratio vs. Input Voltage

Fig. 6 shows S/N ratios measured by the circuit shown in Fig. 4. Those for the same unit except for the filter between pins 4 and 6 replaced by a 0.022 μF capacitor. This comparison clearly proves the effect of the ceramic filter between pins 4 and 6.

(2) Quadrature FM Detector

μPC1200V employs a well-known quadrature detector which allows easy adjustment with only one tuning coil. Further, the detector has no steep drop in detected output due to variation of ambient temperature which occurs in a ratio detector at high temperature.

(3) Level Detector and Controller

The two types of the level detector are built-in; LEVEL DET. 1 and LEVEL DET. 2. LEVEL DET. 1 detects decrease in input signal level while LEVEL DET. 2 detects deviation from the tuning point. Both outputs are added and converted in the controller to the signals V_{11} required for controlling the noise suppressing circuit. (See Figs. 7 and 8.) The capacitor to be connected to pin 11 takes a part of smoothing AM modulated components. A smaller capacitor makes the response speed of a control circuit fast but gives degraded AM suppression characteristics and larger side peaks.

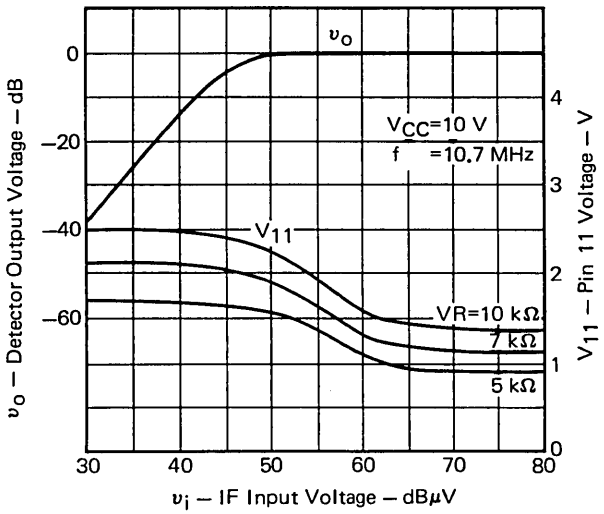


Fig. 7 Pin-11 Voltage vs. Input Voltage

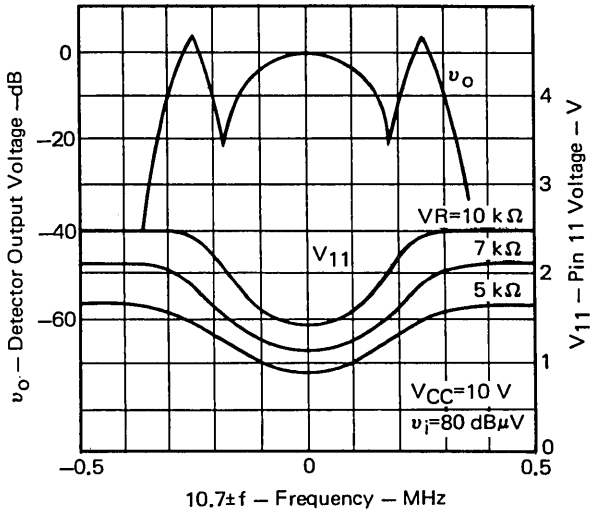


Fig. 8 Pin-11 Voltage vs. Frequency

(4) Noise Supressor

When noise level increases due to decrease in input voltage or due to deviation from a tuning point, this circuit decreases in gain to reduce unconfortable noises to be demodulated by the FM detector.

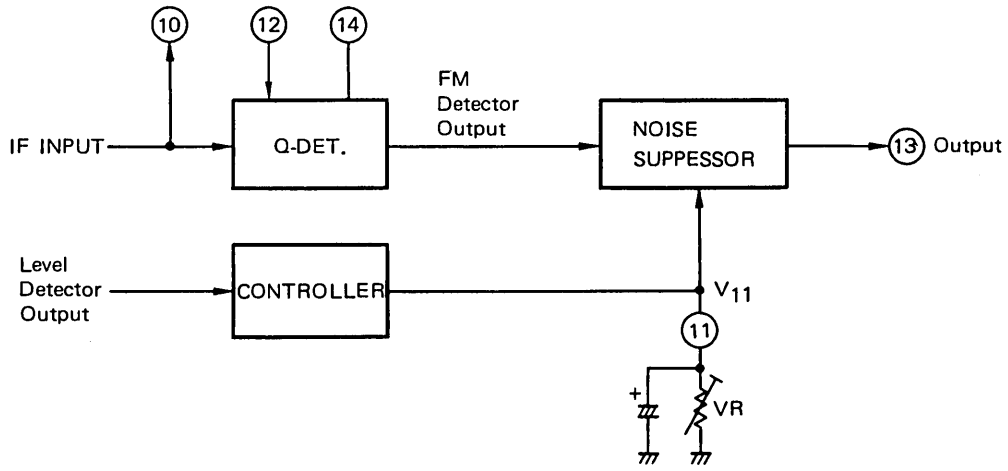


Fig. 9 Block Diagram of Noise Suppressor

Degree of noise suppression depends on the voltage at pin 11, V_{11}: the higher V_{11} produces the greater noise suppression degree. As shown in Figs. 7 and 8. V_{11} increases gradually with decrease in input level or further deviation from the tuning point, generating gradual variation in the output.

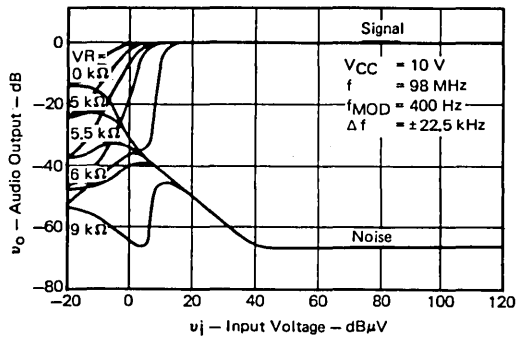


Fig. 10 AUDIO OUTPUT vs. INPUT VOLTAGE

Notes: Figs. 10 and 11 those obtained from application circuit (Fig. 18)

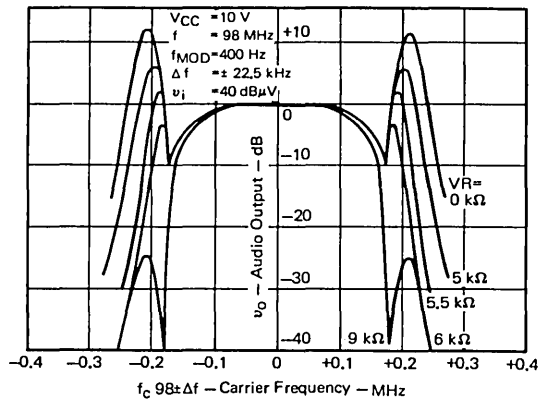


Fig. 11 AUDIO OUTPUT vs. CARRIER FREQUENCY

Setting of noise suppression levels and side peak magnitudes are at customer's proposal by selecting a desirable resistance value of VR to be connected to pin11. VR=0 gives the same characteristics as from conventional ICs, in which limiting sensitivity is maximum while noise levels and side peaks are left not suppressed. Increasing the resistance value of the VR, though lessening the limiting sensitivity to some degree, achieves decreased noise levels and side peaks. This is shown in Figs. 10 and 11. The semi-fixed resistor to be connected to pin11 should be adjusted and set to an appropreate resistance value so that optimum characteristics are obtained.

Unlike car radio units with a conventional muting method where outputs abruptly disappears when input level is smaller than a specified level, μPC1200V does not have such unnatural abruptness but offers an optimal FM tuner for field intensities peculier to a car radio.

5. TYPICAL CHARACTERISTICS

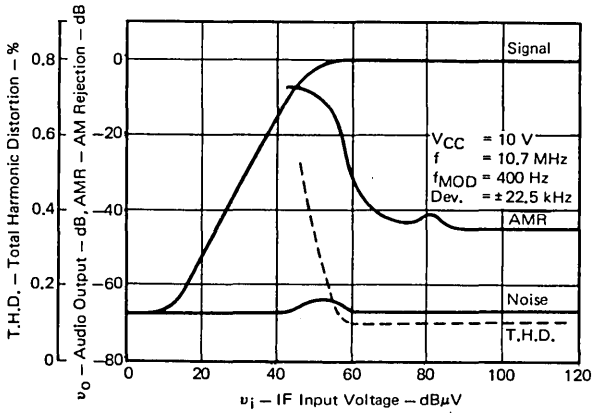


Fig. 12 v_o, AMR, T.H.D. vs. v_i

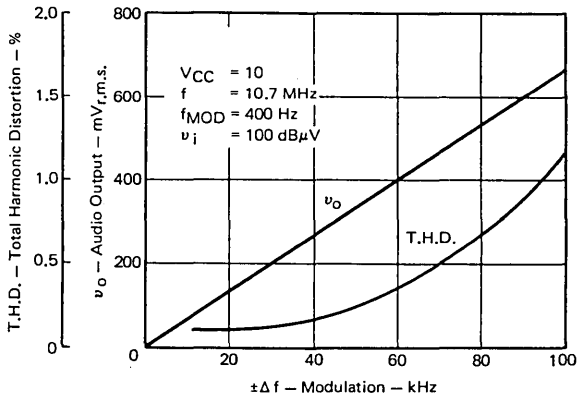


Fig. 13 v_o, T.H.D. vs. Δf

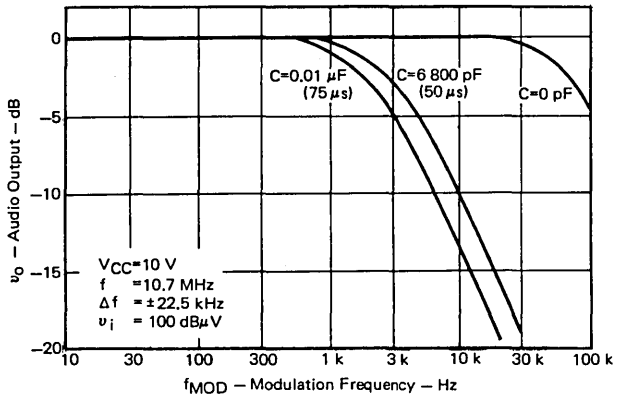


Fig. 14 υ_o vs. f_{MOD}

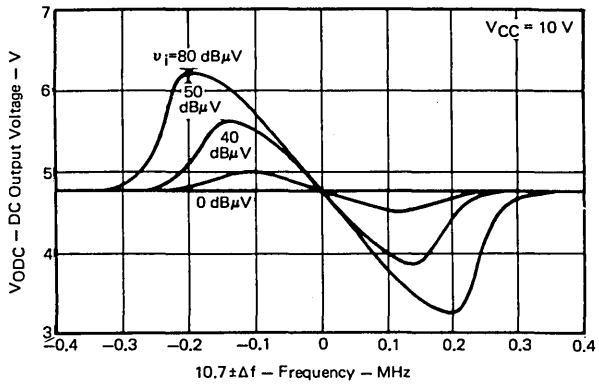


Fig. 15 V_{ODC} vs. Δf

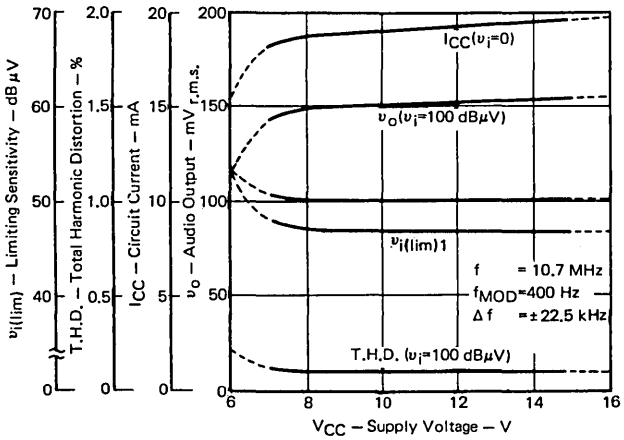


Fig. 16 υ_o, I_{CC}, T.H.D., $\upsilon_{i(lim)}$ vs. V_{CC}

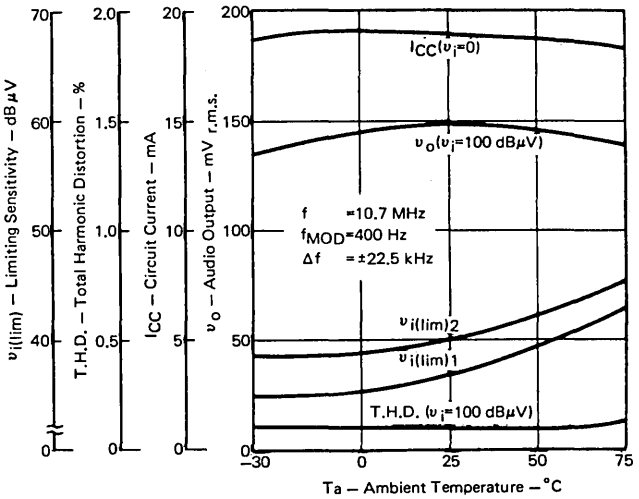
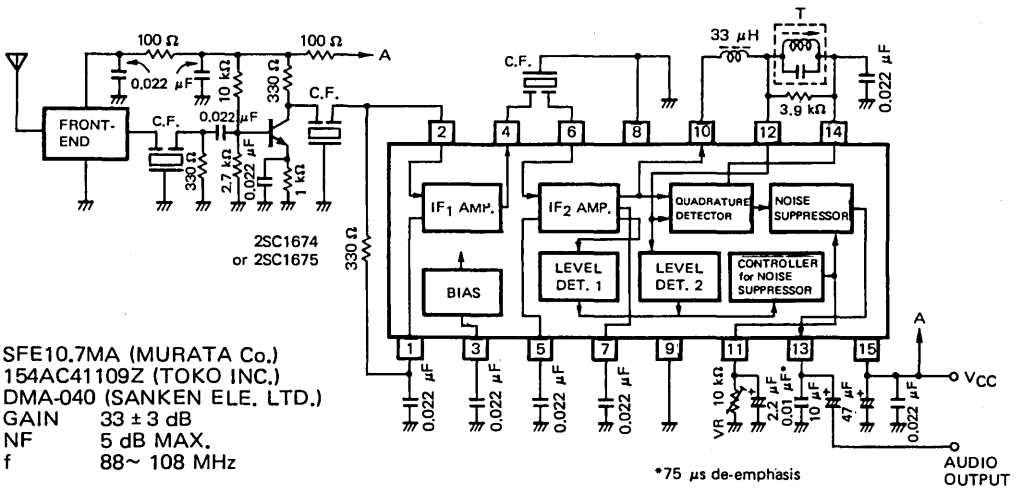


Fig. 17 υ_o, I_{CC}, T.H.D., $\upsilon_{i(lim)}$ vs. T_a

6. TYPICAL APPLICATION



C.F. : SFE10.7MA (MURATA Co.)
T : 154AC41109Z (TOKO INC.)
F/E : DMA-040 (SANKEN ELE. LTD.)
GAIN 33 ± 3 dB
NF 5 dB MAX.
f 88~ 108 MHz

The procedure below should be carefully followed, in order to get the best use of μPC1200V.
1. Limiting sensitivity should be 5 to 10 dBμV
2. FM TUNER should have Noise Figure as low as possible.
3. VR (connected with pin-11) should be adjusted until the optimum point of low lateral sound and high sensitivity is reached.

Fig. 18 TYPICAL APPLICATION

APPLICATION OF THE μPC587C2 AND μPC1026C INTEGRATED CIRCUIT PLL STEREO MULTIPLEX DECODERS

1. INTRODUCTION

The μPC587C2 and μPC1026C are monolithic silicon integrated circuit RC Phase-Locked Loop (PLL) stereo decoders designed for FM stereo multiplex systems. These decoders use a minimum of external components. In addition the stereo decoders require only one adjustment (oscillator frequency) for complete alignment.
The device contains a demodulater system, a voltage controlled oscillator, phase detectors, low pass filters and a DC amplifier. It also includes a stereo-monaural switching circuit and a driver circuit for a stereo indicator lamp.

2. FEATURES

- No coil necessary, all tuning performed with single potentiometer.
- Automatic stereo/monaural switching.
- Operates in a wide range of power supplies: 7 to 16 Volts.
- Low distortion (THD): 0.07% TYP. at monaural operation of the μPC587C2.
- High lamp turn-on sensitivity: 8mV rms; pilot input level of the μPC1026C.
- Lamp driver current-limiting to limit turn on current, prolonging lamp life and protecting the integrated circuit against accidental overload.
- Offers superior stability against the combined effects of temperature, vibration, mechanical shock, and aging.

3. THE DIFFERENCES BETWEEN μPC587C2 AND μPC1026C

Both the μPC587C2 and μPC1026C are supplied in 14-lead dual-in-line plastic package and are pin compatible. Both of them, however, are different as follows;

CHARACTERISTIC	μPC587C2	μPC1026C
Lamp Turn on Sensitivity	16mV	8mV
Voltage gain	−6dB	−1.5dB

From the above, if the gain from the FM front end to the output terminals of the MPX is considered to be fixed, the μPC587C2 can be recommended for the set having a relatively high detector output level, and the μPC1026C for the set of relatively low detector output level.

4. CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Supply Voltage	Vcc	16	V
Package Dissipation (Ta = 75°C)	P_D	350	mW
Lamp Driver Current (Pin 6)	I_L	100	mA
Operating Temperature	Topt	−20 to + 75	°C
Storage Temperature	Tstg	−40 to +125	°C

RECOMMENDED CONDITIONS (Ta = 25°C)

Operating Supply Voltage	Vcc	10	V
Supply Voltage Range		7 to 16	V
Operating Ambient Temperature	Ta	−20 to + 75	°C

ELECTRICAL CHARACTERISTICS

Electrical Characteristics of the μPC587C2

[Ta = 25°C, Vcc = 10V, v_{in} = 300mV $\left(\frac{\text{Pilot}}{\text{Composite}} = \frac{1}{10}\right)$, f = 1kHz, R_L = 3.9kΩ]

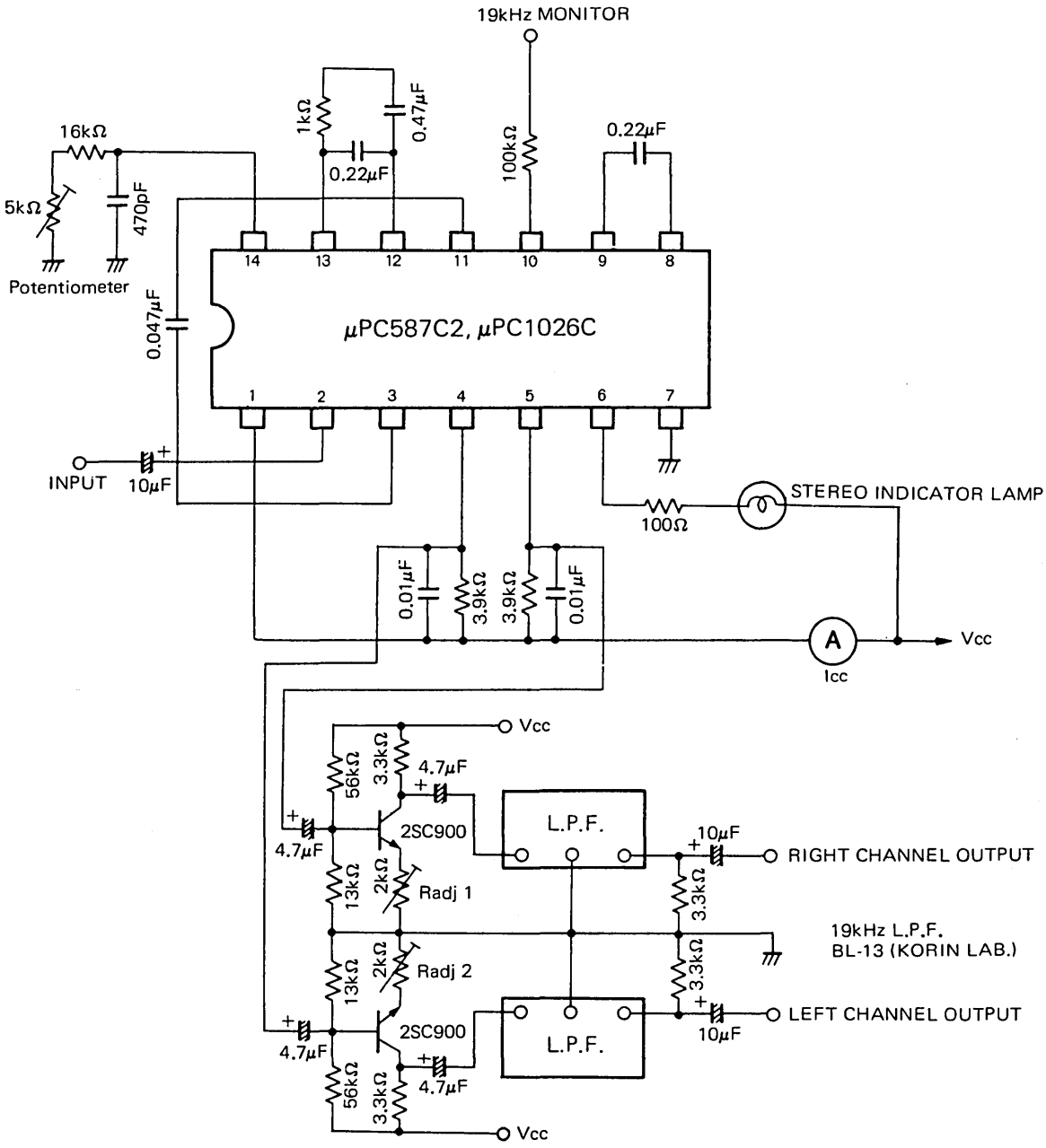
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	Icc	7	13	18	mA	Quiescent
Input Impedance	Zi		50		kΩ	
Stereo Channel Separation	Sep.	30	40		dB	f = 100Hz, $v_{in(pilot)}$ = 30mV
		35	45		dB	f = 1kHz, $v_{in(pilot)}$ = 30mV
		30	40		dB	f = 10kHz, $v_{in(pilot)}$ = 30mV
Voltage Gain	Av	−9	−6		dB	Monaural Input, v_{in}(L+R) = 300mV
Channel Balance	Ch.B.	−1.5	0	1.5	dB	Monaural Input, v_{in}(L+R) = 300mV
	Ch.B.	−1.5	0	1.5	dB	Stereo Input, $v_{in(pilot)}$ = 30mV
Total Harmonic Distortion	T.H.D.		0.07	0.5	%	Monaural Input, v_{in}(L+R) = 300mV
			0.15	0.5	%	Stereo Input, $v_{in(pilot)}$ = 30mV
Lamp Indicator Input Level	LAMP ON	12	16	20	mV	Pilot Level
Lamp Hysteresis		3	6	9	dB	Pilot Level
Capture Range	C.R.	±1.5	±3		%	$v_{in(pilot)}$ = 30mV
Ultrasonic Frequency Rejection	19kHz Rej.		35		dB	19kHz, $v_{in(pilot)}$ = 30mV
	38kHz Rej.		45		dB	38kHz, $v_{in(pilot)}$ = 30mV
SCA Rejection	SCA Rej.		70		dB	$\frac{\text{Pilot}}{\text{Composite}} = \frac{1}{10}$ $\frac{\text{SCA}}{\text{Composite}} = \frac{1}{10}$
Maximum Input Level	v_i	0.7	1		Vr.m.s.	Monaural Input, T.H.D. = 1%

Electrical Characteristic of the μPC1026C

[Ta = 25°C, Vcc = 10V, υ_{in} = 150mV $\left(\frac{\text{Pilot}}{\text{Composite}} = \frac{1}{10}\right)$, f = 1kHz, R_L = 3.9kΩ]

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	Icc	7	13	18	mA	Quiescent
Input Impedance	Zi		50		kΩ	
Stereo Channel Separation	Sep.	30	40		dB	f = 100Hz, $\upsilon_{in(pilot)}$ = 15mV
		35	45		dB	f = 1kHz, $\upsilon_{in(pilot)}$ = 15mV
		30	40		dB	f= 10kHz, $\upsilon_{in(pilot)}$ = 15mV
Voltage Gain	Aυ	−4.5	1.5	2.0	dB	Monaural Input, υ_{in}(L+R) = 150mV
Channel Balance	Ch.B.	−1.5	0	1.5	dB	Monaural Input, υ_{in}(L+R) = 150mV
	Ch.B.	−1.5	0	1.5	dB	Stereo Input, $\upsilon_{in(pilot)}$ = 15mV
Total Harmonic Distortion	T.H.D.		0.15	0.5	%	Monaural Input υ_{in}(L+R) = 150mV
			0.15	0.5	%	Stereo Input, $\upsilon_{in(pilot)}$ = 15mV
Lamp Indicator Input Level	LAMP ON	5	8	11	mV	Pilot Level
Lamp Hysteresis		3	6	9	dB	Pilot Level
Capture Range	C.R.	±1.5	±3		%	$\upsilon_{in(pilot)}$ = 15mV
Ultrasonic Frequency Rejection	19kHz Rej.		35		dB	19kHz, $\upsilon_{in(pilot)}$ = 15mV
	38kHz Rej.		45		dB	38kHz, $\upsilon_{in(pilot)}$ = 15mV
SCA Rejection	SCA Rej.		70		dB	$\frac{\text{Pilot}}{\text{Composite}} = \frac{1}{10}$, $\frac{\text{SCA}}{\text{Composite}} = \frac{1}{10}$
Maximum Input Level	υ_i	0.4	0.6		Vr.m.s.	Monaural Input, T.H.D. = 1%

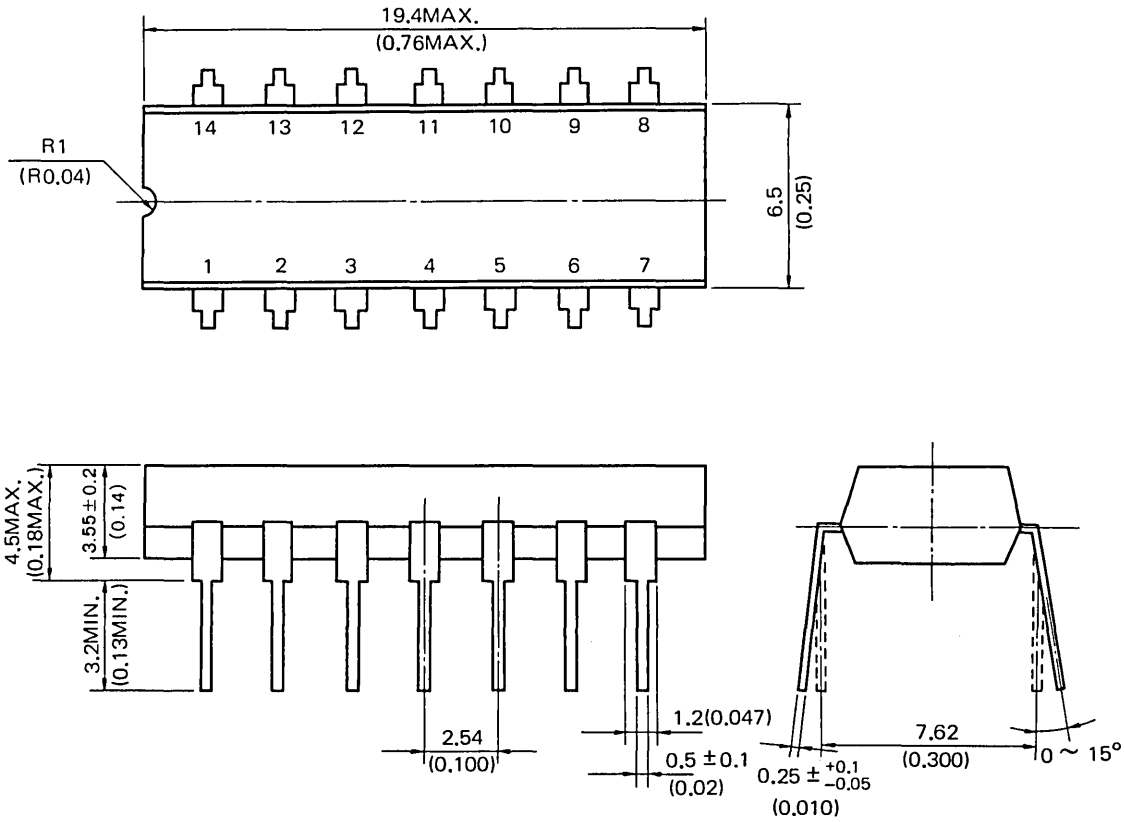
TEST CIRCUIT



1. Use a polystylene capacitor to the 470pF capacitor connected pin 14 for temperature compensation to VCO.
2. Radj 1 and Radj 2 should be set so that, the voltage gain between the output terminal of the IC and the output terminal of the L.P.F. is 0dB.
3. For tuning the VCO, adjust the 5kΩ potentiometer connected pin 14 by reading a frequency of 19kHz at Pin 10.

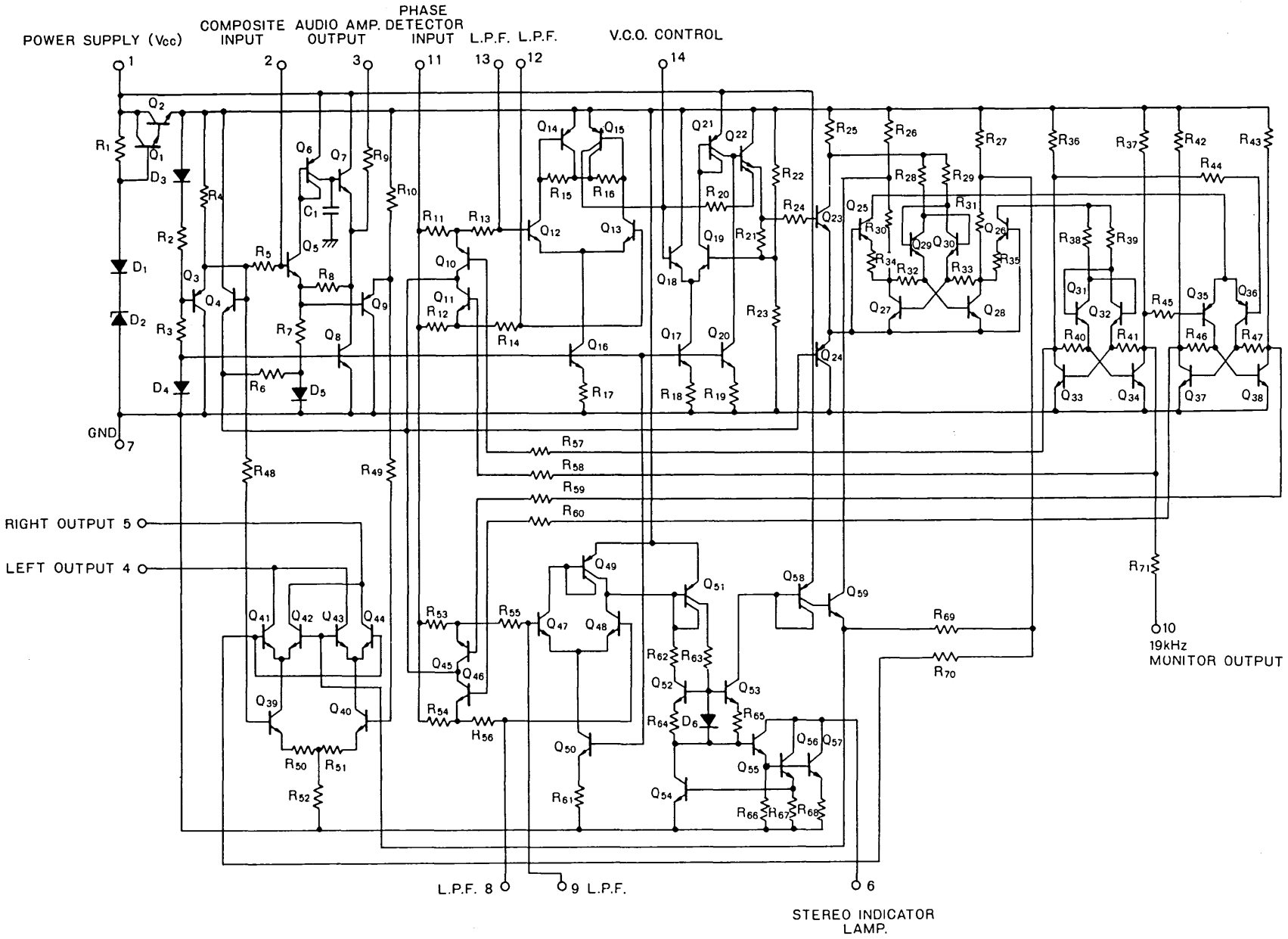
PACKAGE DIMENSIONS AND CONNECTION DIAGRAM (Top View)

in millimeters (inches)



Pin No.	Electrical Connections	Pin No.	Electrical Connections
1	POWER SUPPLY (Vcc)	8	L.P.F.
2	COMPOSITE INPUT	9	L.P.F.
3	AUDIO AMP. OUTPUT	10	19kHz MONITOR OUTPUT
4	LEFT CHANNEL OUTPUT	11	PHASE DETECTOR INPUT
5	RIGHT CHANNEL OUTPUT	12	L.P.F.
6	LAMP DRIVER	13	L.P.F.
7	GND.	14	V.C.O. CONTROL

EQUIVALENT CIRCUIT



Voltages of each pin (Vcc = 10 V, Refer to Test Circuit)

	1.	2.	3.	4.	5.	6.	7.
μPC587C 2	10V	2.8V	4.7V	7.4V	7.4V	10V	0
μPC1026C	10V	2.1V	4.7V	7.4V	7.4V	10V	0

	8.	9.	10.	11.	12.	13.	14.
μPC587C 2	2.1V	2.1V	–	2.1V	2.1V	2.1V	–
μPC1026C	2.1V	2.1V	–	2.1V	2.1V	2.1V	–

5. DESCRIPTION OF CIRCUIT

(1) Input Buffer/Amplifier and Bias Supply.

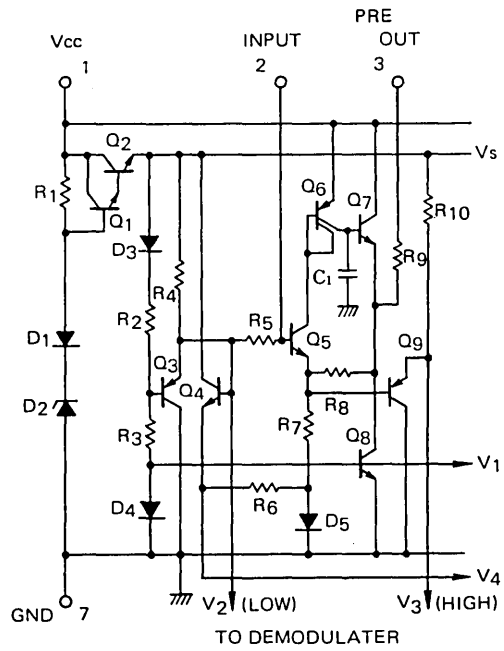


Fig. 5 Bias Supply and Buffer/ Input Amplifier.

The equivalent circuit of the bias supply and input signal amplifier is shown in Fig. 5.

In Fig. 5 the stabilized voltage Vs is expressed by $D_1 + D_2 - V_{BE}(Q_{BE1}) - V_{BE}(Q_{BE2})$ and is constant against variations of the power supply. The various bias voltages are established, based on this stabilized voltage.

Since Q_3 operates as an emitter follower circuit, the bias voltage V_2 of the input amplifier is expressed by the following equation.

$$V_2 = \frac{(R_3 + D_4)}{(D_3 + R_2) + (R_3 + D_4)} \times V_S + V_B$$

On the other hand, the reference voltage V_1 to the DC amplifier and VCO, to be described later, is determined by D_4 attached to the voltage stabilizing circuit.

The input signal amplifier is composed of transistors Q_5, Q_6, Q_7 and resistors R_7, R_8, and R_9, and capacitor C_1. Since Q_6 is a multi-collector transistor, it's collector current is nearly the same as the collector current of Q_5, and the current gain is close to unity. C_1 is for frequency stability, and its value is 5 to 20pF. The voltage gain of the input signal amplifier is determined by the feedback circuit R_7, R_8, and D_5, but since the impedance of D_5 can be neglected, the voltage gain can be approximated by the following equation.

$$Av(AF) = \frac{R_7 + R_8}{R_7}$$

Stereo signals entering pin (2) are amplified by an amount indicated by the above equation, and then introduced to the phase detector of the PLL circuit through terminal (3). Besides the above, stereo signals pass through emitter follower Q_9, from the emitter of Q_5, to be injected into the stereo demodulator circuit.

(2) Demodulator Circuit.

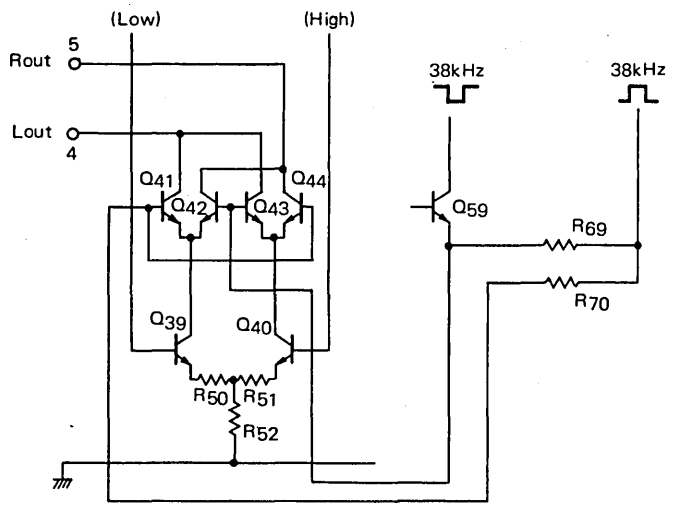


Fig. 6 Demodulator Circuit.

Fig. 6 is a stereo demodulator circuit. The circuit consists of a common double-balanced type detector circuit, and the stereo signal is injected into the lower transistors Q_{39} and Q_{40} while the 38kHz subcarrier is injected into the upper transistors Q_{41}, Q_{42}, Q_{43}, and Q_{44}. Stereo demodulation is accomplished by the subcarrier switching the above transistors. R_{50}, R_{51}, and R_{52} are feedback resistors inserted for the purpose of cancelling the cross talk components produced during switching. The subcarrier is a 50% duty cycle 38kHz wave obtained from a bistable multivibrator (flip-flop) circuit, into which a 76kHz signal produced by the VCO is injected. In both the μPC587C2 and μPC1026C the stereo lamp and stereo demodulation are synchronized and accomplished by Q_{59}. The base of Q_{59} is controlled by the stereo lamp circuit, and when the stereo lamp is turned ON, Q_{59} will also be turned ON and a 38kHz subcarrier of reverse phase will be injected into the demodulation circuit, Q_{41}, Q_{44} and Q_{42}, Q_{43}. On the other hand, when the stereo lamp is turned OFF Q_{59} is also turned OFF, and an in-phase 38kHz subcarrier is injected into Q_{41}, Q_{44}, and Q_{42}, Q_{43} so that a monaural wave is obtained from output terminals (4) and (5).

(3) Lamp Driver.

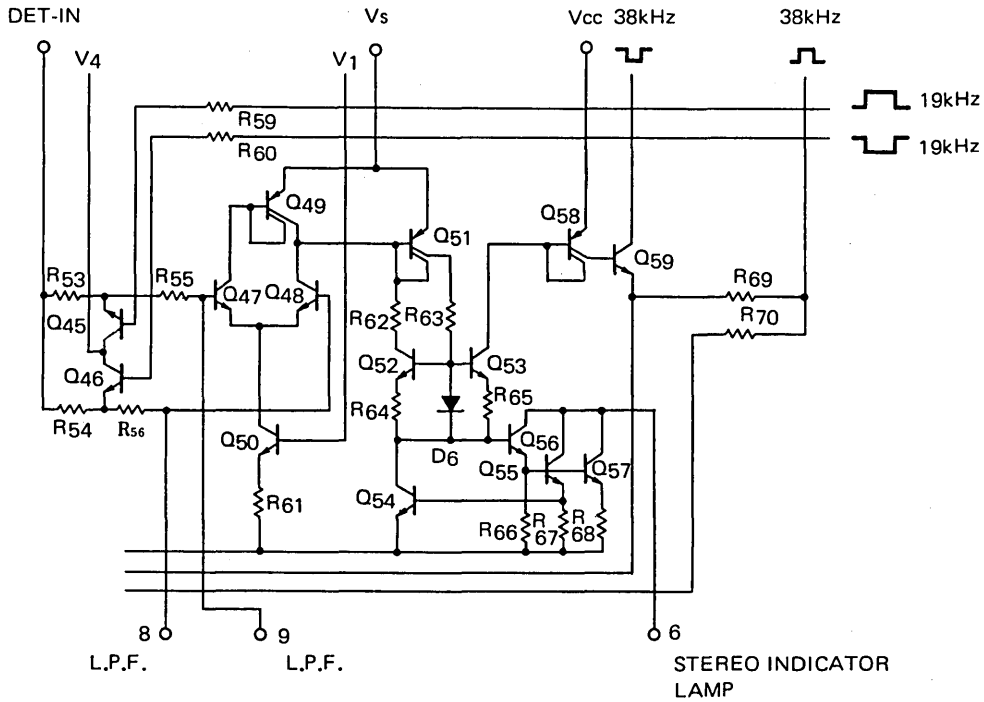


Fig. 7 Lamp Driver Circuit.

Fig. 7 shows a lamp driver circuit with it's auxiliary circuits. Transistors Q_{45} and Q_{46}, resistors R_{53}, R_{54}, R_{55}, R_{56}, R_{59}, and R_{60}, with the addition of external discrete capacitors (8) and (9) form the phase detector circuit and low-pass filter. In the phase detector circuit the product is formed by the 19kHz (obtained by counting down the 76kHz frequency produced by the VCO with a bistable multivibrator (flip-flop)) injected from the bases of Q_{45} and Q_{46} and the pilot signal contained in the stereo signal. The high frequency components of the product are eliminated by the L.P.F., and only terms concerning the phase difference remain. This 19kHz signal differs 90° in phase with the 19kHz signal required by the PLL loop circuit (That is, it is in synchronization with the phase of the pilot signal), and when the phases are precisely in step the DC component obtained through the phase detector circuit and L.P.F. will be at maximum level, and when the phases shift the DC component will decrease. This change in the level of the DC component will move in a positive direction at terminal (8), and a negative direction at terminal (9). This state, when expressed as an equation will take the following form.

Pilot signal $e_{p(t)} = E_p \cos \omega_p t$

19kHz signal $e_{19(t)} = E_{19} \cos(\omega_p + \phi)t$ (Note) (To be precise, 19kHz is a square wave.)

$$e_{p(t)} = e_{19(t)} = \frac{E_p \cdot E_{19}}{2} \left\{ \cos\phi t + \cos(2\omega_p + \phi)t \right\} = \frac{E_p \cdot E_{19}}{2} \cos\phi t \quad \ldots\ldots\ldots \text{Eliminated by L.P.F.}$$

The lamp drive circuit is composed of transistors Q_{47} to Q_{57} and accessory resistors. Q_{47} and Q_{48} compose a circuit for amplifying the control voltage obtained from the L.P.F., and Q_{49} is the active load of this differential amplifier. Now, if the collector current I_{Q47} of Q_{47} and the collector current I_{Q48} of Q_{48} change by ΔIc ($\Delta Ic = I_{Q48} - I_{Q47}$) due to the control current passed through the phase detector, ΔIc will flow intact into the base of Q_{51}. Q_{51} is a multicollector transistor, and it's collector current will amplify the change ΔIc of the base current and D_6 will become biased by this current. And, when this diode is biased transistor Q_{53} will operate causing lamp driving transistor Q_{56} to be turned ON, thus the lamp will light. On the other hand, when Q_{53} turns ON it will draw the base current of Q_{58}, and as a result Q_{58} and Q_{59}, will be turned on and stereo operation will start. Since Q_{51}, Q_{52}, D_6, R_{62}, R_{63}, and R_{64} form a positive feedback loop, when the lamp is turned ON the rise of current will be abrupt. In addition, transistors Q_{54}, Q_{55}, Q_{56}, and resistor R_{68} form a negative feedback circuit, which composes a current limiting circuit for performing current limiting action.

(4) Phase Detector and DC Amplifier.

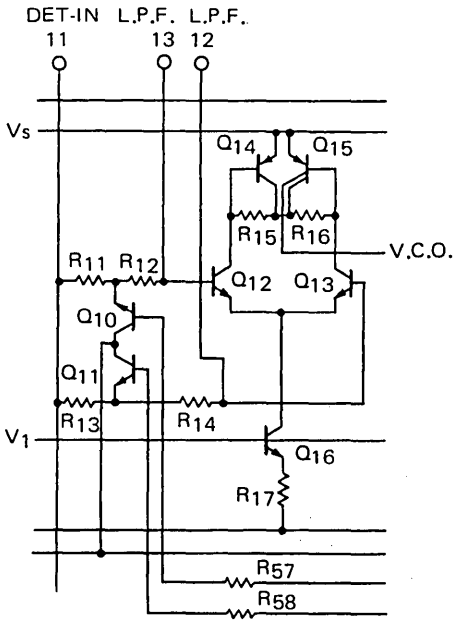


Fig. 8 Phase Detector and DC Amplifier.

Fig. 8 shows the phase detector and DC amplifier. The 19kHz signal obtained through the dividing circuit will switch the pilot signal of the stereo signal coming into terminal (11), and will supply a DC voltage proportional to the phase difference of these to the DC amplifier composed of Q_{12} to Q_{16}. When the phase difference of the 19kHz signal and pilot signal, entering the phase detector, is 90° the control voltage of the PLL circuit will be 0. When the phase of the 19kHz signal advances from the above, a positive control voltage will be produced, and when the 19kHz phase lags a negative control voltage will be produced.

When this state is expressed as an equation, it becomes as follows.

Pilot signal $e_{p(t)} = E_p \cos\omega_p t$

19kHz signal $e_{19(t)}$ $E_{19}\sin(\omega_p + \phi)t$ (Note) (To be precise, 19kHz is a square wave.)

$$e_{p(t)} = e_{19(t)} = \frac{E_p \cdot E_{19}}{2}\left\{\sin\phi t + \sin(2\omega_p + \phi)t\right. \quad = \left.\frac{E_p \cdot E_{19}}{2}\sin\phi t\right\} \ldots\ldots\ldots \text{Eliminated by L.P.F.}$$

The DC amplifier is composed of transistors Q_{12} to Q_{16}, and converts the changes of the control voltage to current to be sent to the VCO.

(5) VCO

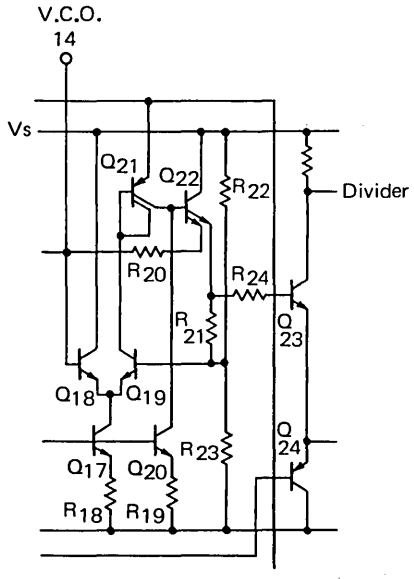


Fig. 9 VCO

Fig. 9 shows the VCO (Voltage Controlled Oscillator).

This circuit is basically a comparator, which produces oscillations through variations of the reference voltage.

Now, when transistor Q_{19} is operating, both Q_{21} and Q_{22} will become conducting and the instantaneous reference voltage of the comparator applied to the base of Q_{19} is expressed as follows.

$$V_H = \left\{V_s - V_{CE(sat)}\ (Q_{22})\right\} \times \frac{R_{23}}{R_{21} + R_{23}}$$

On one hand, current will flow from the emitter of Q_{22}, and this current will charge the external discrete capacitor through R_{20}. The charging time t_1 of this capacitor is expressed as follows:

$$t_1 = R_{20}C\log\frac{V_s - V_L}{V_s - V_H}$$

When the above charging is completed the comparator will be switched-over and Q_{18} will be turned ON. At this point, the reference voltage V_L of the comparator will become as follows.

$$V_L = V_s \times \frac{R_{23}}{R_{22} + R_{23}}$$

The charge accumulated in the external capacitor of terminal (14) will discharge at a rate determined by the external resistor R and capacitor C.

(6) Divider Circuit.

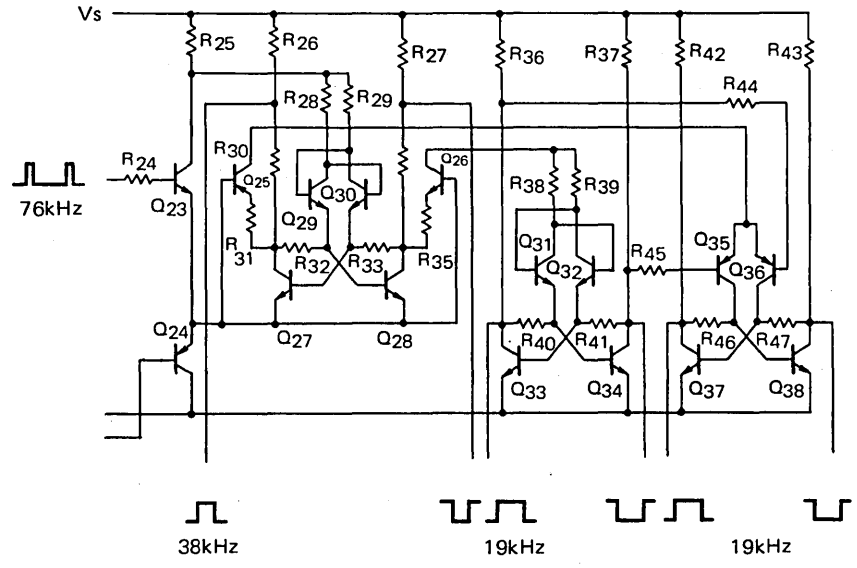


Fig. 10 Divider Circuit.

Fig. 10 shows the divider circuit. This circuit is a bistable multivibrator (flip-flop). This multivibrator serves to produce 38kHz and 19kHz, 50% duty cycle, voltages from the 76kHz voltage generated by the VCO. The 38kHz voltage is the subcarrier required for FM stereo demodulation, the 19kHz having a 90° phase difference with the pilot signal is required as the control voltage of the PLL, and the 19kHz synchronized with the pilot signal is required for driving the stereo lamp and controlling the stereo switch.

6. CIRCUIT APPLICATIONS OF THE PLL-MPX IC

The μPC587C2 and μPC1026C are most suitable for use as the FM multiplex demodulatior circuit of car radio and stereo sets.

Applications of the μPC587C2 shall be described following.

(1) Overriding Stereo-Monaural Switching Circuit.

Stereo multiplex operation on the μPC587C2 becomes possible when the 19kHz pilot signal of an ordinary input synchronizes with the 19kHz generated within the IC, and through this the lamp driver transistor is excited and the gate circuit is turned OFF to inject a 38kHz subcarrier into the demodulation circuit. However, cases can be imagined when stereo ON operation is required regardless of the input conditions of the MPX input circuit.

A general circuit for this case is shown in Fig. 11. As described before, to obtain stereo-ON operation it is necessary to pass current through the base of transistor Q_{51}, but since Q_{47}, Q_{48}, Q_{49}, and Q_{50} consist a differential amplifier circuit, stereo-ON operation can be obtained if the voltage of terminal (8) is kept higher than terminal (9). The overriding switching circuit will differ according whether a plus or ground potential is employed as the control voltage. But, for example, when manual switching of overriding monaural operation is required, this can be obtained by grounding terminal (9).

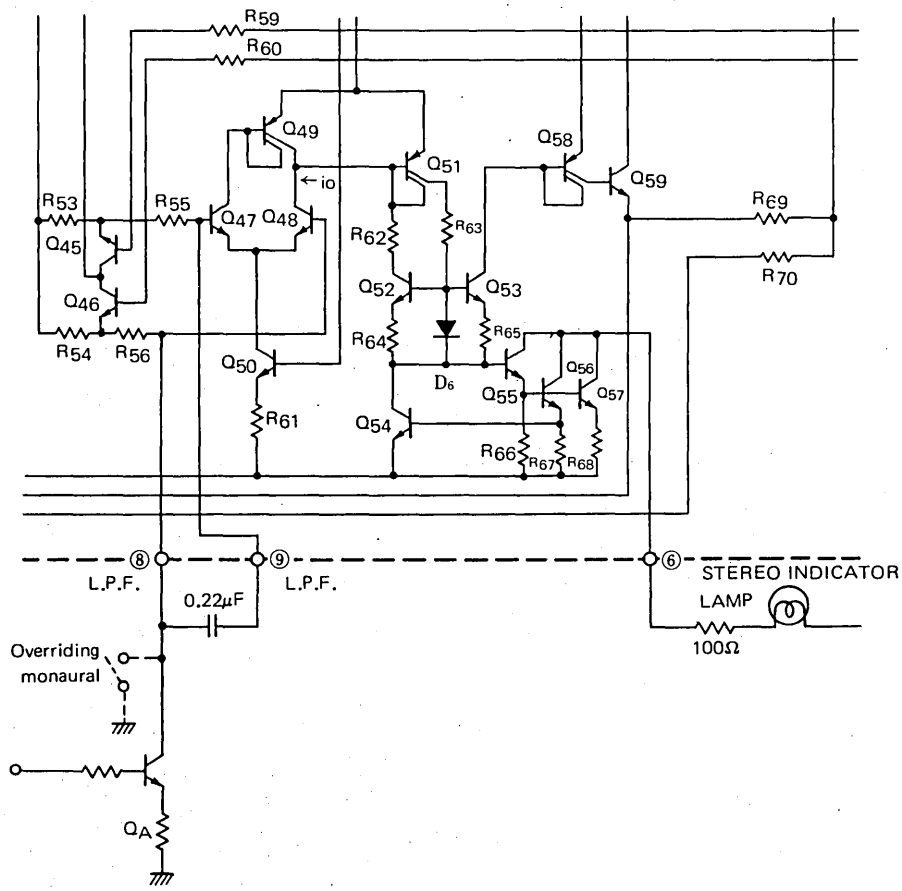


Fig. 11 Overriding Monaural Circuit.

(2) Beat Interference of AM Reception.

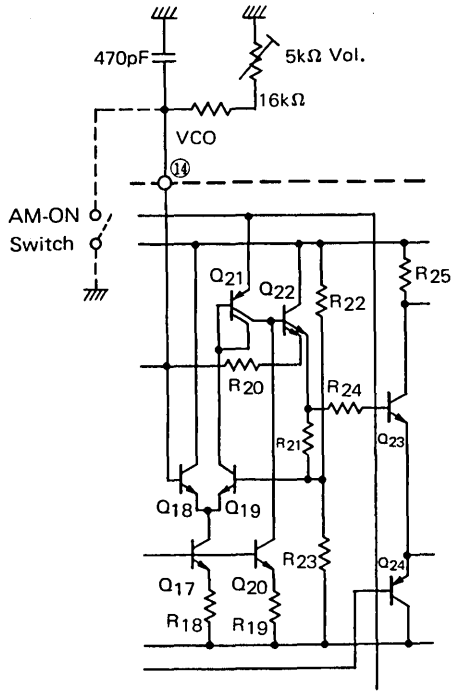


Fig. 12 VCO Stop Circuit.

Differing from conventional coil type stereo demodulation circuits, the μPC587C2 has an internal oscillation circuit, and there are cases when the internal oscillator voltage of the PLL becomes a source of interference during AM reception. To solve this problem it is necessary to stop the VCO. If, as described before, attention is paid to the fact that the VCO is an oscillator circuit utilizing a differential comparator, it can be seen that the VCO can be stopped by grounding the input terminal (14), and the 76kHz oscillation stopped.

(3) Adjustment of the Lighting Level of the Stereo Lamp.

The method of adjusting the lighting level of the stereo lamp is made clear from the characteristics of the circuit of Fig. 7. That is, the lighting level can be changed by varying the input ON level of the differential amplifier composed of transistors Q_{47}, Q_{48}, Q_{49}, and Q_{50}. Ordinary, the base potential of transistor Q_{48} will rise when the 19kHz pilot signal increases, and this ON level will reach a value determined by selecting the collector current of Q_{47} at a value four times that of Q_{48}. Therefore, the lamp lighting level can be changed by varying the offset voltage of the above differential amplifier. Methods of changing this are shown in Figs. 13 and 14.

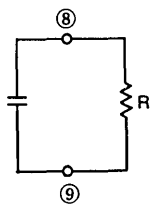


Fig. 13

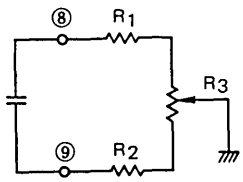


Fig. 14

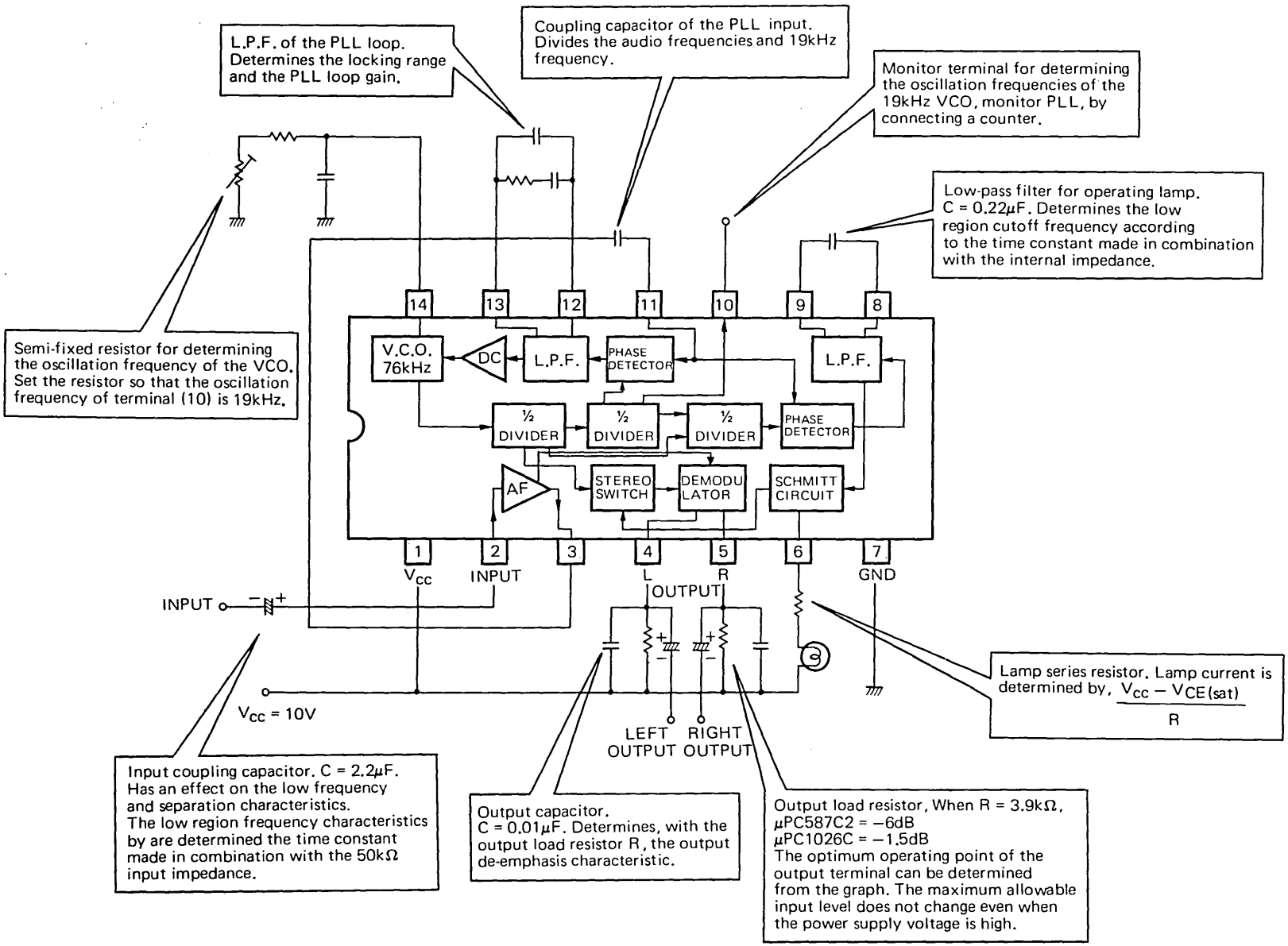
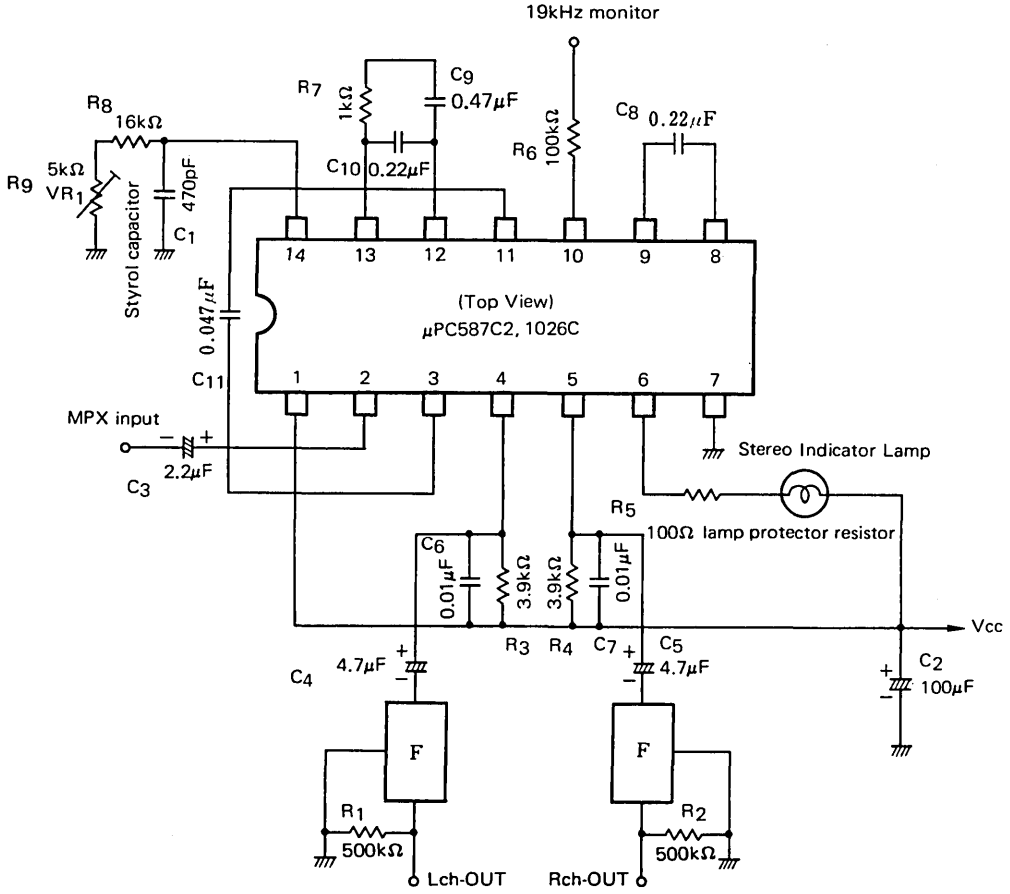
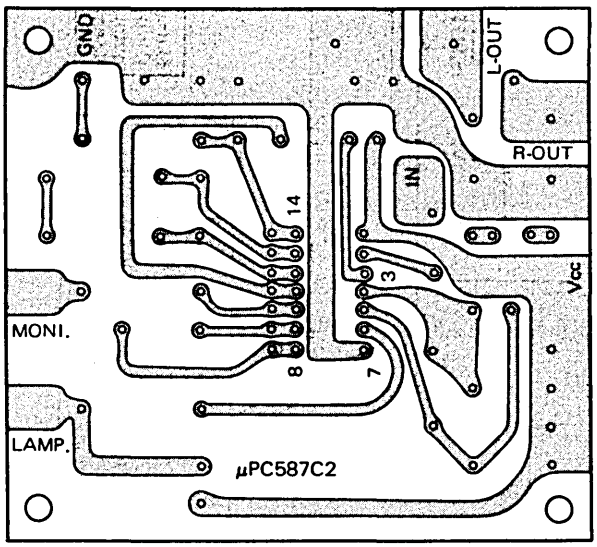


Fig. 15 Description of External Discrete Components of the P.L.L. MPX.

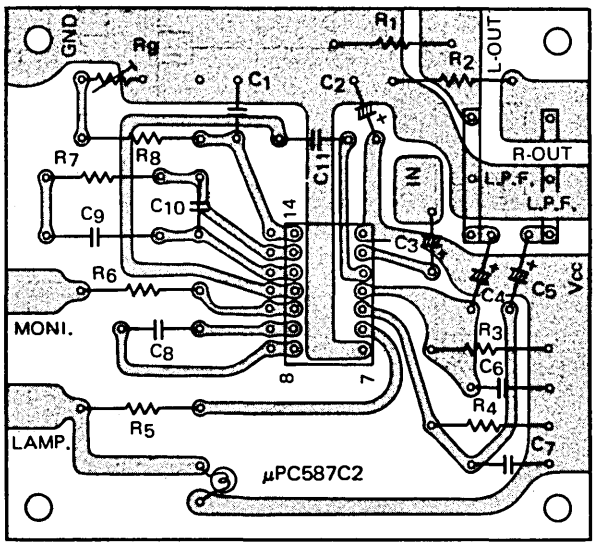
Fig. 16 Application Circuit, Example 1.



Printed Circuit Board



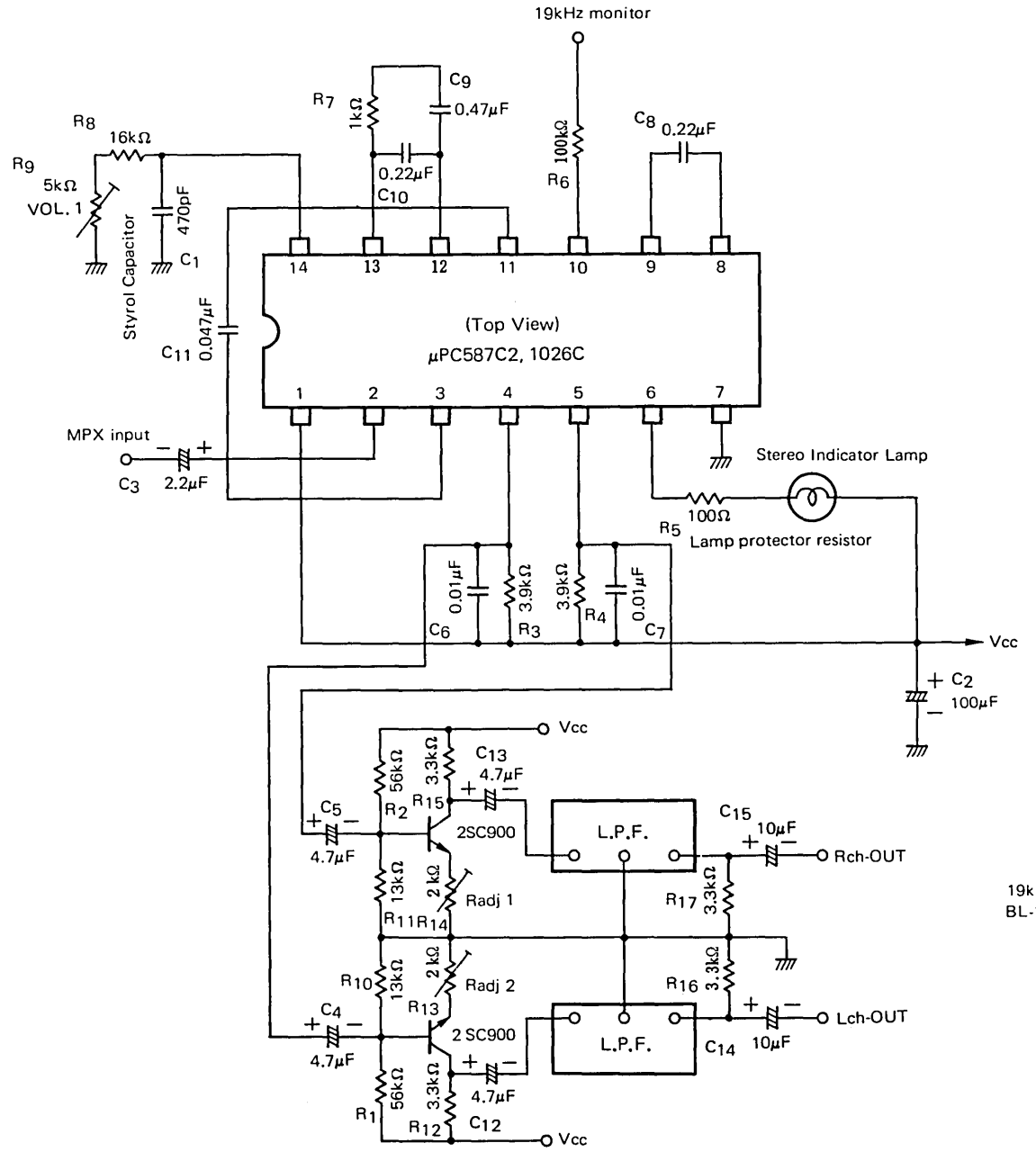
Components Layout for P.W. Assembly (Copper side)



R_1 = 500kΩ
R_2 = 500kΩ
R_3 = 3.9kΩ
R_4 = 3.9kΩ
R_5 = 100Ω
R_6 = 100kΩ
R_7 = 1kΩ
R_8 = 16kΩ
R_9 = 5kΩ Vol.

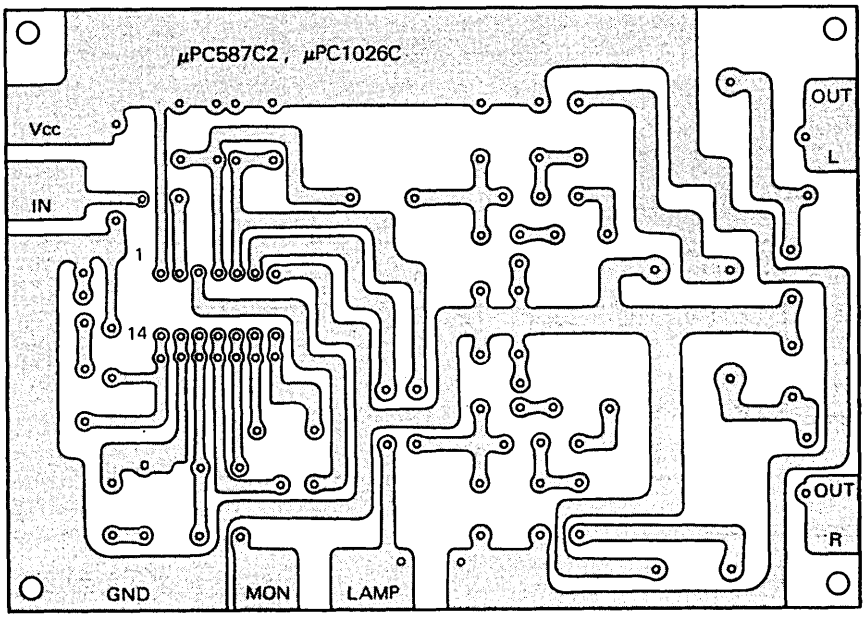
C_1 = 470pF
C_2 = 100μF
C_3 = 2.2μF
C_4 = 4.7μF
C_5 = 4.7μF
C_6 = 0.01μF
C_7 = 0.01μF
C_8 = 0.22μF
C_9 = 0.47μF
C_{10} = 0.22μF
C_{11} = 0.047μF

Fig. 17 Application Circuit, Example 2.

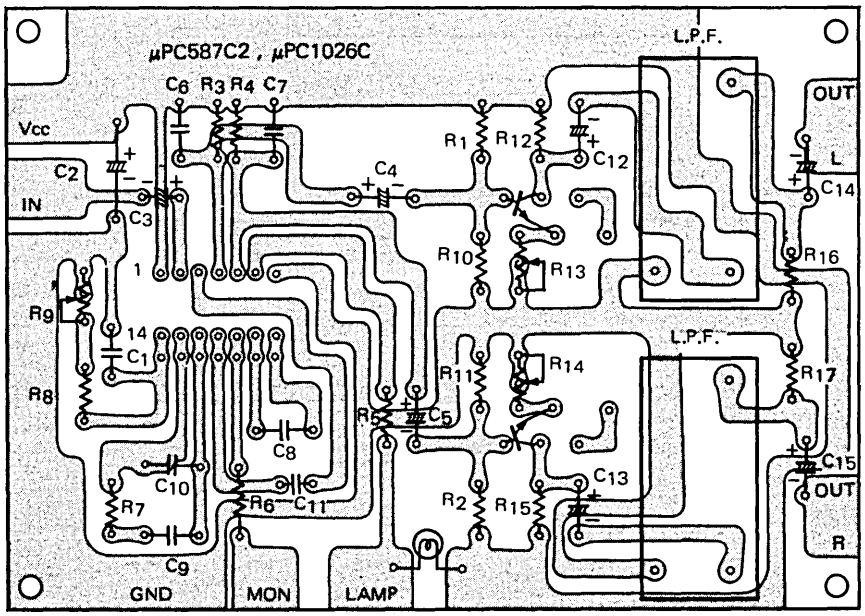


19kHz L.P.F.
BL-13 Korin Giken

Printed Circuit Board



Components Layout for P.W. Assembly (Copper side)



R_1 = 56kΩ	R_7 = 1kΩ	R_{13} = 2kΩ Vol.	C_1 = 470pF	C_7 = 0.01μF	C_{13} = 4.7μF
R_2 = 56kΩ	R_8 = 16kΩ	R_{14} = 2kΩ Vol.	C_2 = 100μF	C_8 = 0.22μF	C_{14} = 10μF
R_3 = 3.9kΩ	R_9 = 5kΩ Vol.	R_{15} = 3.3kΩ	C_3 = 2.2μF	C_9 = 0.47μF	C_{15} = 10μF
R_4 = 3.9kΩ	R_{10} = 13kΩ	R_{16} = 3.3kΩ	C_4 = 4.7μF	C_{10} = 0.22μF	
R_5 = 100Ω	R_{11} = 13kΩ	R_{17} = 3.3kΩ	C_5 = 4.7μF	C_{11} = 0.047μF	
R_6 = 100kΩ	R_{12} = 3.3kΩ		C_6 = 0.01μF	C_{12} = 4.7μF	

7. EXAMPLE OF A FM TUNER EMPLOYING A PLL-MPX IC.

Circuit examples employing the μPC587C2 and μPC1026C as the MPX section are shown in Figs. 16 and 17, respectively. And, in Figs. 62 and 63 are shown examples of overall circuit applications of the μPC587C2 employing the μPC1028H as peak detector and FM-IF amplifier, and the μPC1026C employing the μPC577H as the FM-IF amplifier.

Overall characteristics of the overall circuit application of Fig. 63 are shown in Figs. 62, 64, 65, and 66.

The difference between the μPC587C2 and μPC1026C has been described before, but it should be noted that when the μPC577H is used in the final stage of the FM-IF amplifying circuit, since the detector output is not so large, it is desirable to use the μPC1026C, which has a high lamp lighting sensitivity, as the MPX. And, when the μPC1028H is used as the FM-IF amplifier, since a large detector output can be obtained, it is desirable to used the μPC587C2 as the MPX.

8. TYPICAL CHARACTERISTICS of μPC587C2 (Ta = 25°C)

Fig. 18 CIRCUIT CURRENT vs. SUPPLY VOLTAGE (μPC587C2)

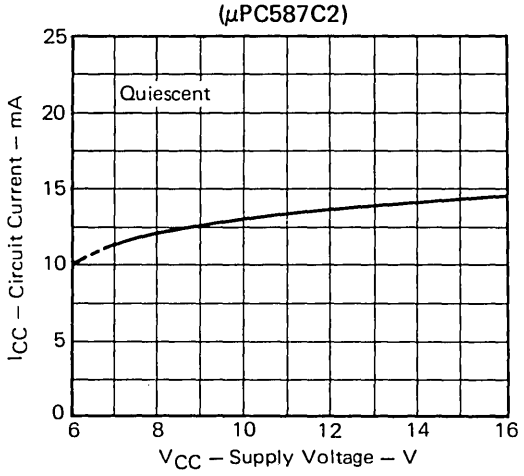


Fig. 19 VOLTAGE GAIN vs. SUPPLY VOLTAGE (Monaural) (μPC587C2)

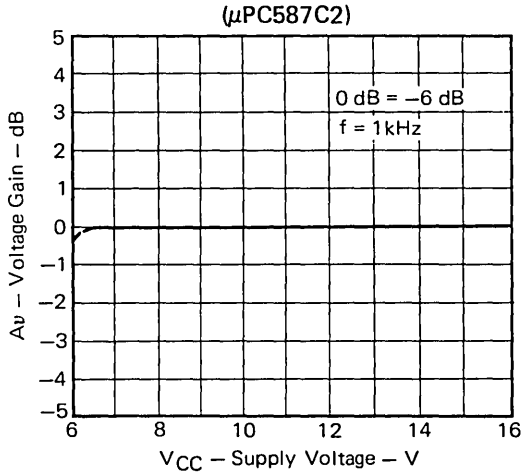


Fig. 20 CHANNEL BALANCE vs. SUPPLY VOLTAGE (Monaural) (μPC587C2)

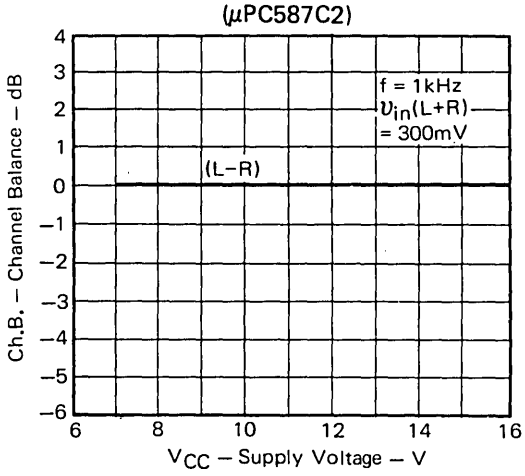


Fig. 21 CHANNEL SEPARATION vs. SUPPLY VOLTAGE (μPC587C2)

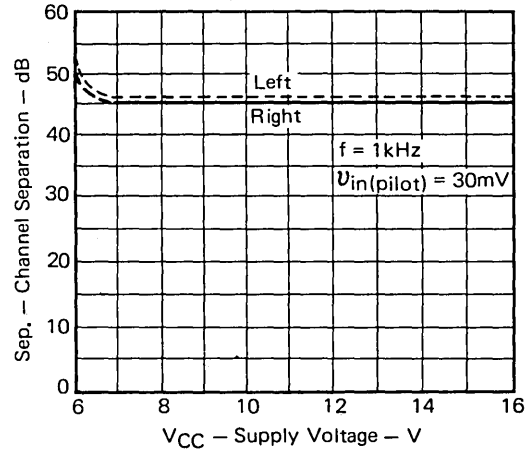


Fig. 22 CHANNEL SEPARATION
vs. PILOT INPUT LEVEL (μPC587C2)

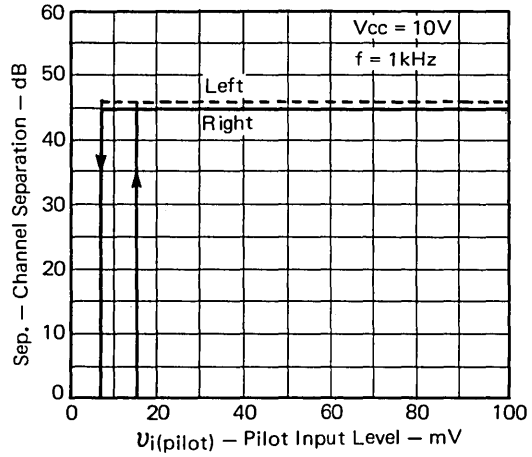


Fig. 23 FREE RUN FREQUENCY CHANGE
vs. SUPPLY VOLTAGE (μPC587C2)

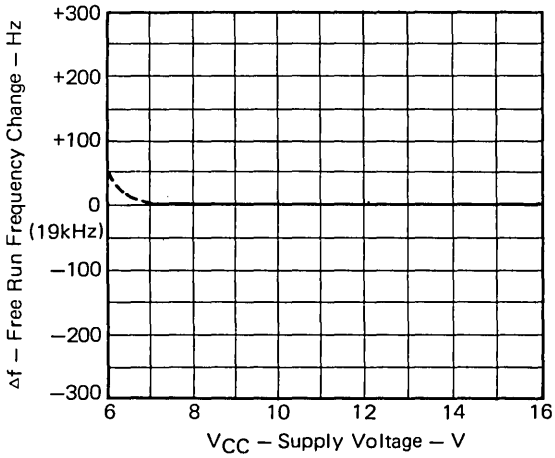


Fig. 24 CHANNEL SEPARATION
vs. FREQUENCY (μPC587C2)

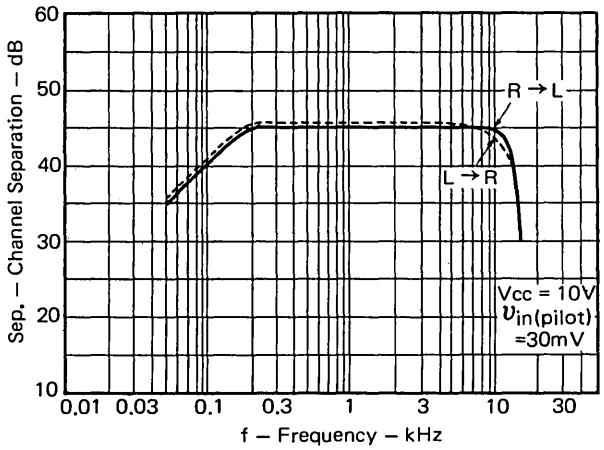


Fig. 25 VOLTAGE GAIN
vs. FREQUENCY (Monaural) (μPC587C2)

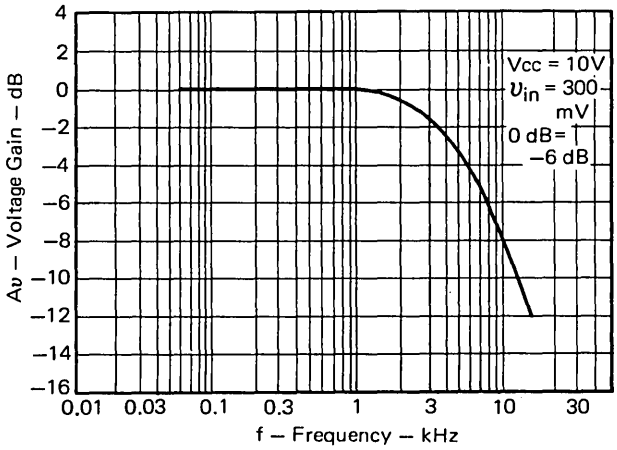


Fig. 26 TOTAL HARMONIC DISTORTION vs. INPUT SIGNAL LEVEL (Monaural)

(μPC587C2)

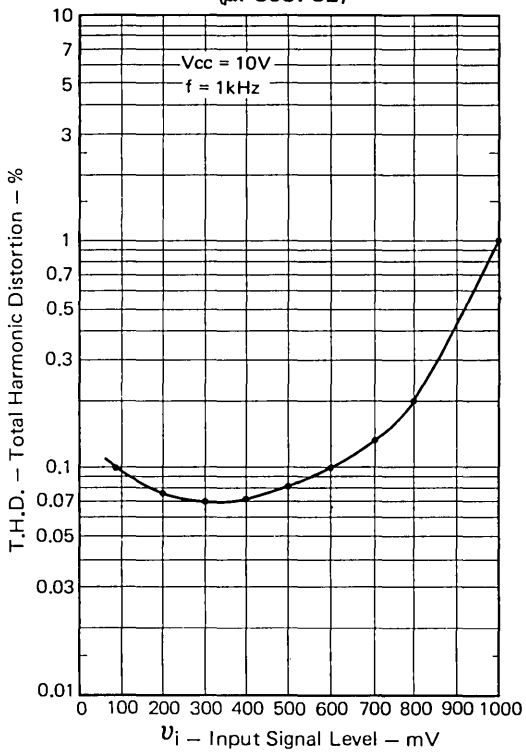


Fig. 27 TOTAL HARMONIC DISTORTION vs. SUPPLY VOLTAGE (Monaural)

(μPC587C2)

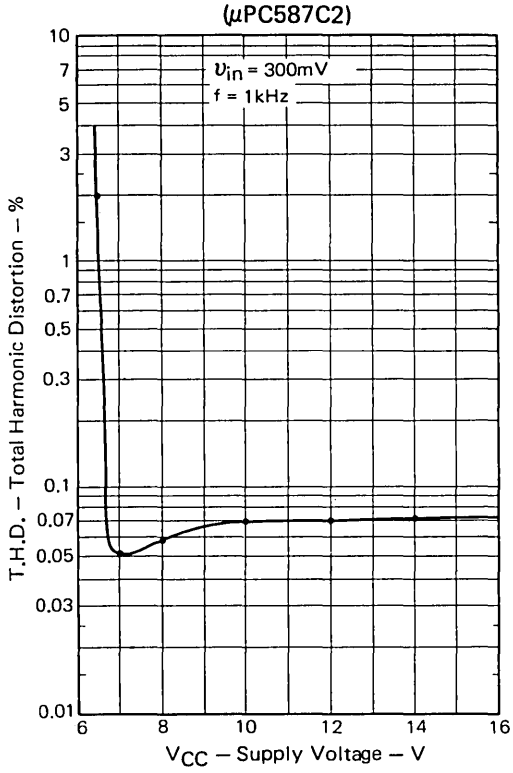


Fig. 28 TOTAL HARMONIC DISTORTION vs. INPUT SIGNAL LEVEL (Stereo)

(μPC587C2)

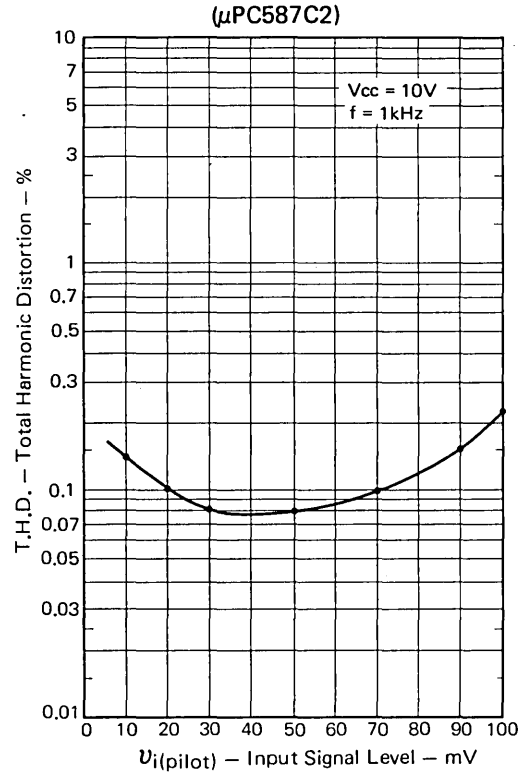


Fig. 29 TOTAL HARMONIC DISTORTION vs. FREQUENCY (Stereo)

(μPC587C2)

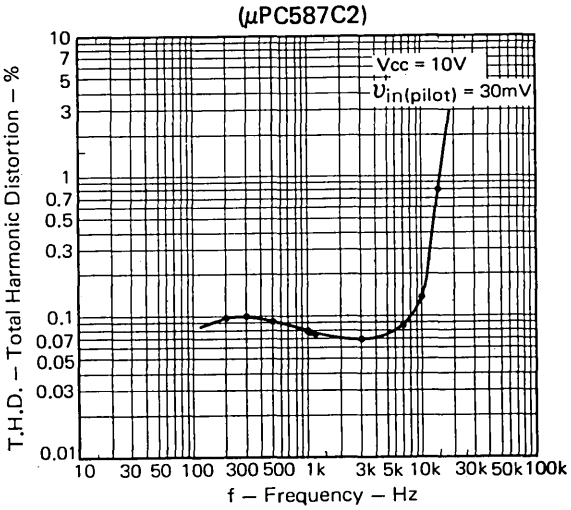


Fig. 30 TOTAL HARMONIC DISTORTION vs. FREQUENCY (Monaural)

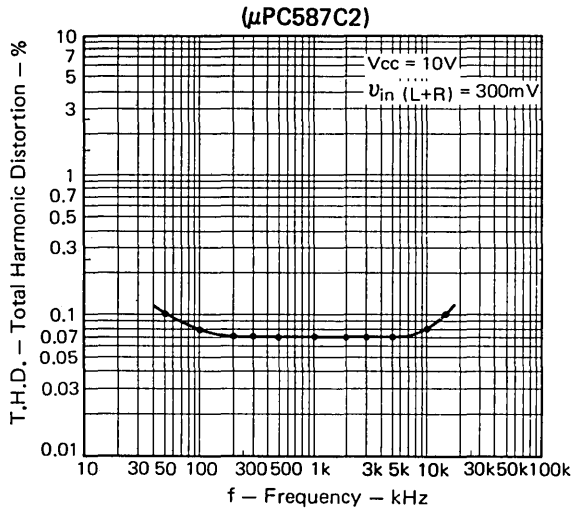


Fig. 31 MAXIMUM INPUT LEVEL vs. SUPPLY VOLTAGE

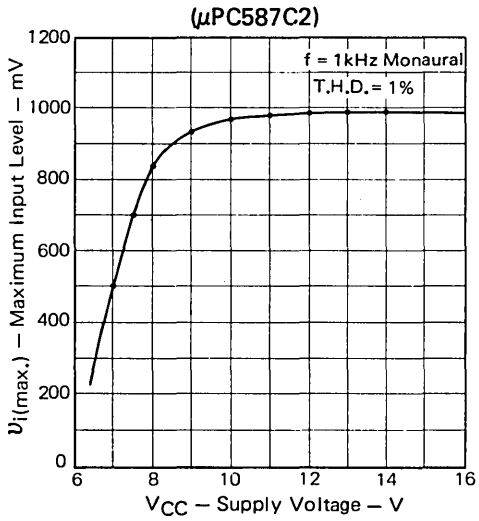


Fig. 32 CHANNEL SEPARATION vs. OSCILLATOR FREE RUNNING FREQUENCY

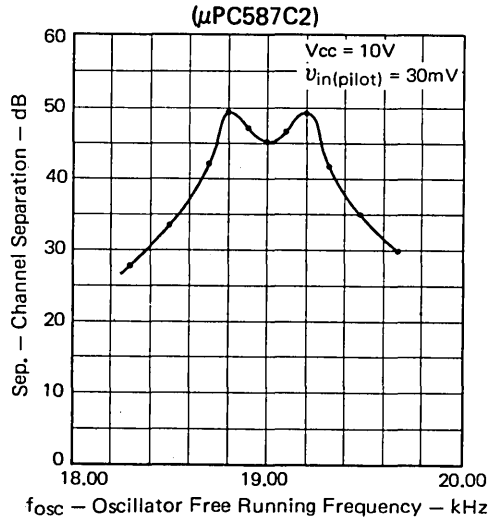


Fig. 33 OSCILLATOR FREE RUNNING FREQUENCY vs. AMBIENT TEMPERATURE

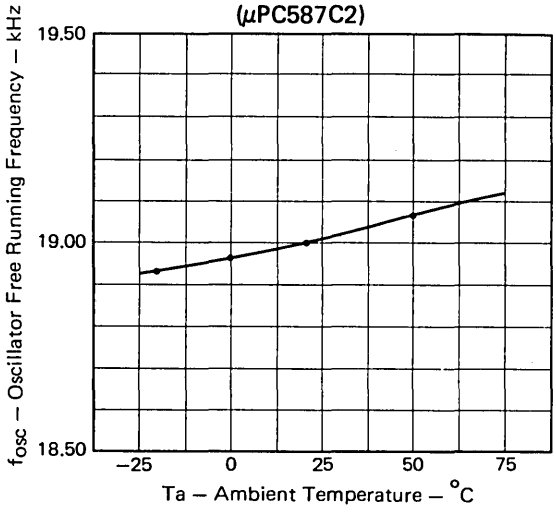


Fig. 34 POWER DISSIPATION OF LAMP DRIVER, SATURATION VOLTAGE OF LAMP DRIVER vs. LAMP CURRENT

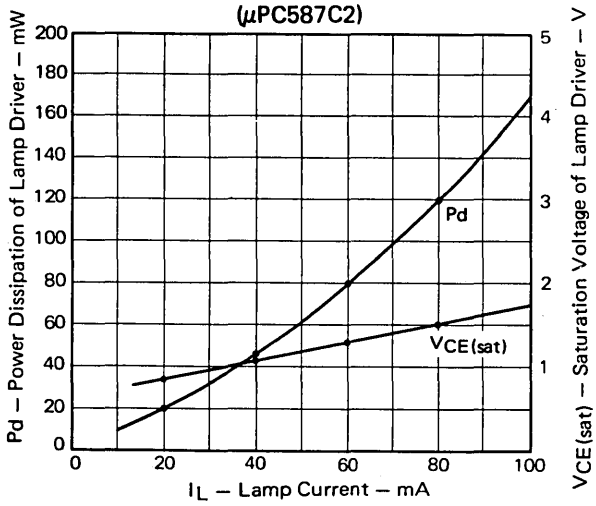


Fig. 35 OSCILLATOR FREE RUNNING FREQUENCY vs. ELAPSING TIME

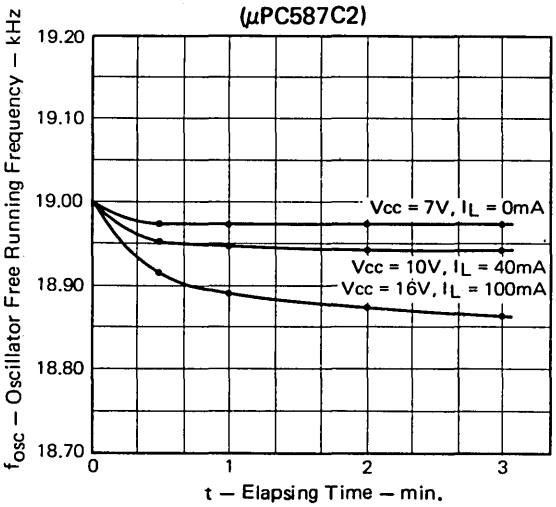


Fig. 36 CAPTURE RANGE vs. AMBIENT TEMPERATURE

(μPC587C2)

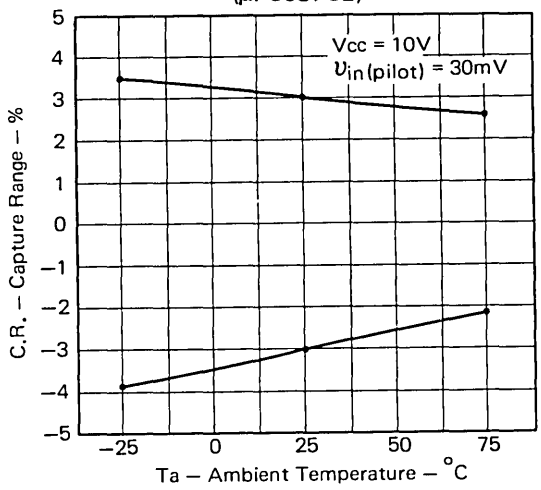


Fig. 37 PILOT LEVEL (Lamp ON-OFF) vs. AMBIENT TEMPERATURE

(μPC587C2)

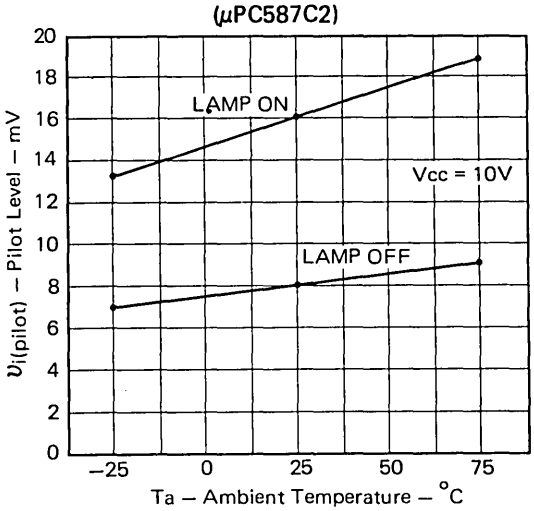


Fig. 38 POWER DISSIPATION vs. SUPPLY VOLTAGE

(μPC587C2)

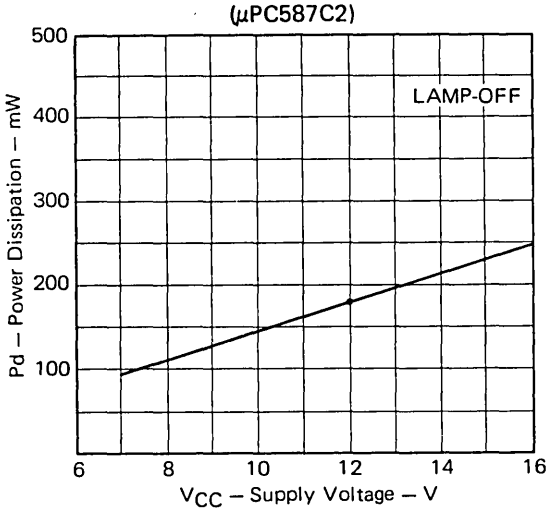
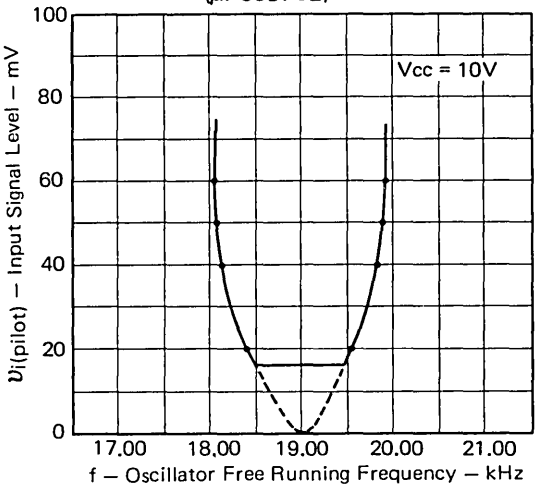


Fig. 39 CAPTURE RANGE

(μPC587C2)



9. TYPICAL CHARACTERISTICS OF μPC1026C (Ta = 25°C)

Fig. 40 CIRCUIT CURRENT vs. SUPPLY VOLTAGE (μPC1026C)

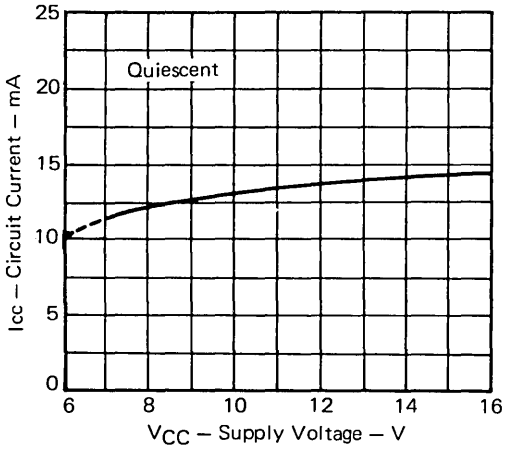


Fig. 41 VOLTAGE GAIN vs. SUPPLY VOLTAGE (Monaural) (μPC1026C)

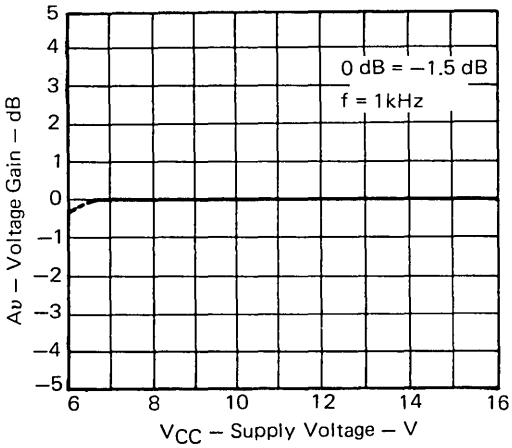


Fig. 42 CHANNEL BALANCE vs. SUPPLY VOLTAGE (Monaural) (μPC1026C)

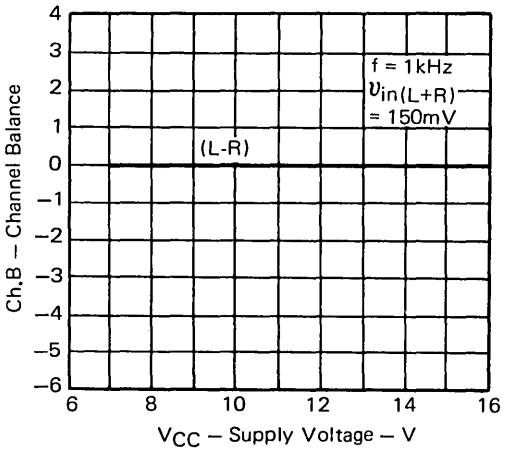


Fig. 43 CHANNEL SEPARATION vs. SUPPLY VOLTAGE (μPC1026C)

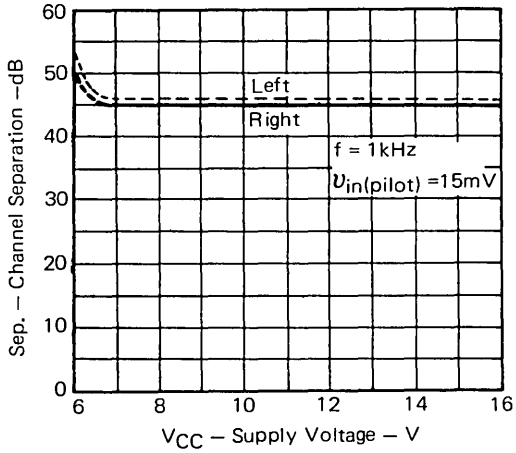


Fig. 44 CHANNEL SEPARATION vs. PILOT INPUT LEVEL (μPC1026C)

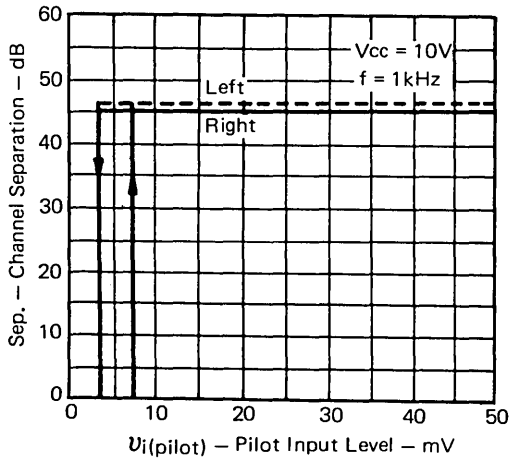


Fig. 45 FREE RUN FREQUENCY CHANGE vs. SUPPLY VOLTAGE (μPC1026C)

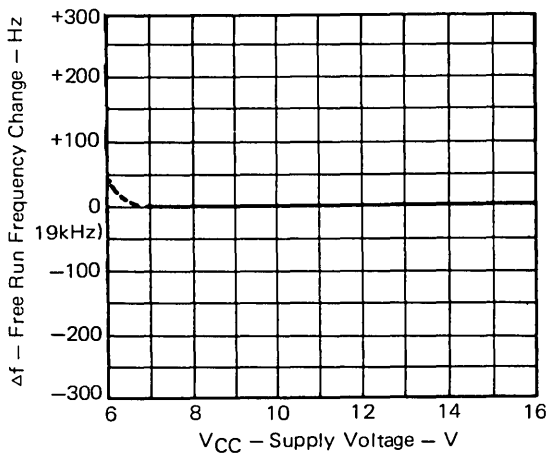


Fig. 46 CHANNEL SEPARATION vs. FREQUENCY (μPC1026C)

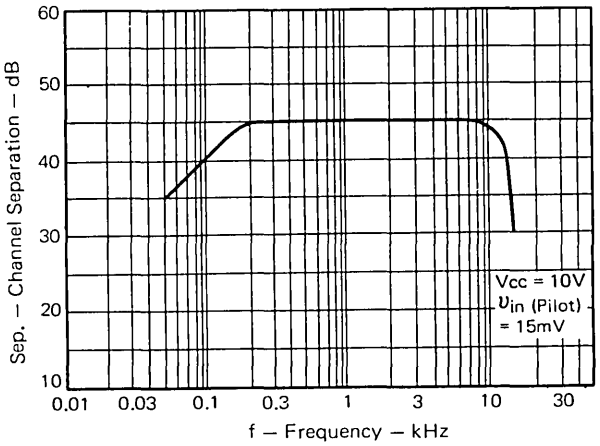


Fig. 47 VOLTAGE GAIN vs. FREQUENCY (Monaural) (μPC1026C)

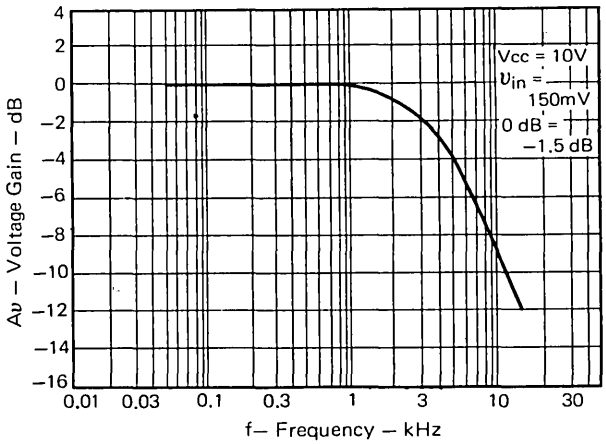


Fig. 48 TOTAL HARMONIC DISTORTION vs. INPUT SIGNAL LEVEL (μPC1026C)

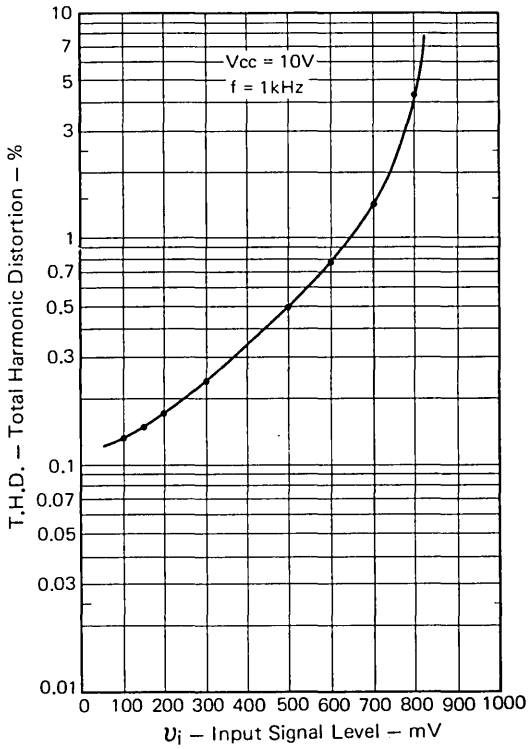


Fig. 49 TOTAL HARMONIC DISTORTION vs. SUPPLY VOLTAGE (μPC1026C)

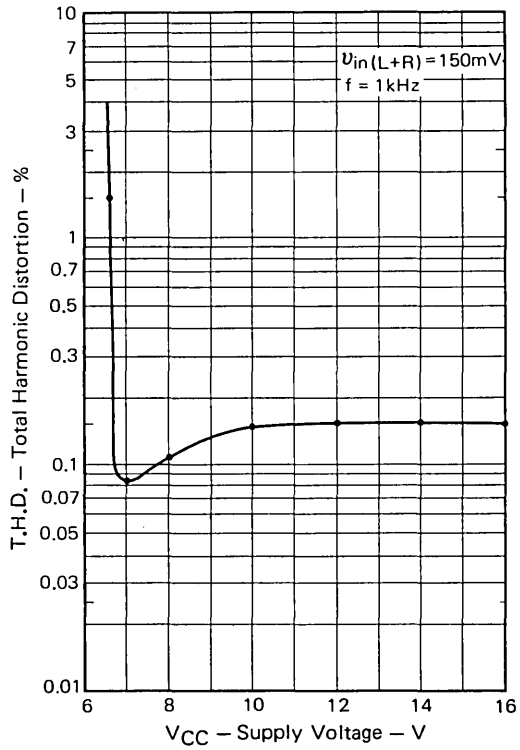


Fig. 50 TOTAL HARMONIC DISTORTION vs. INPUT SIGNAL LEVEL (Stereo) (μPC1026C)

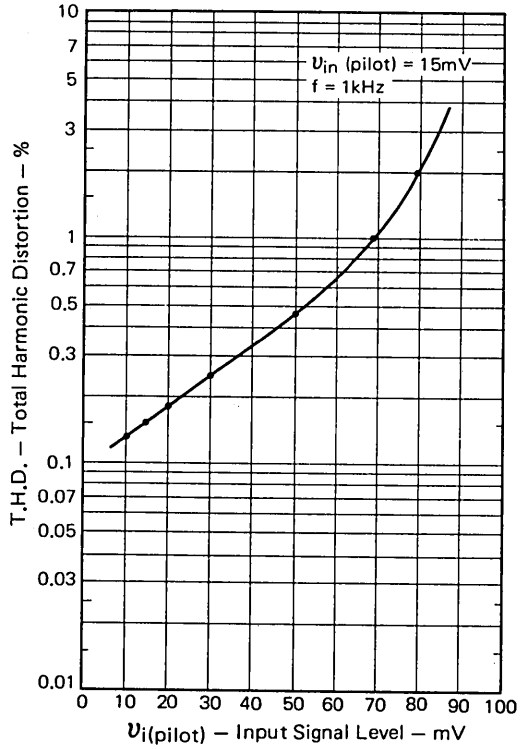


Fig. 51 TOTAL HARMONIC DISTORTION vs. FREQUENCY (Stereo) (μPC1026C)

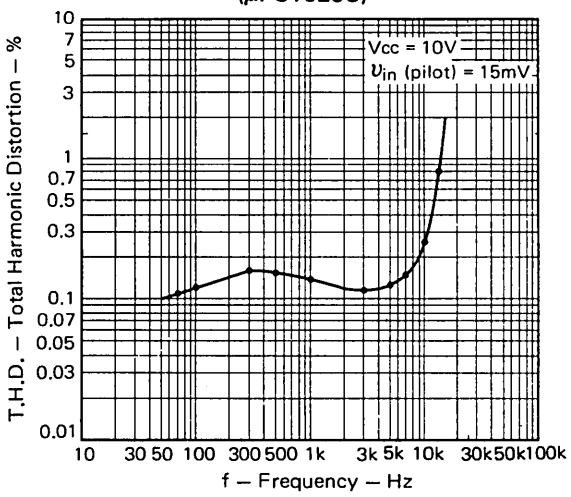


Fig. 52 TOTAL HARMONIC DISTORTION vs. FREQUENCY (Monaural) (μPC1026C)

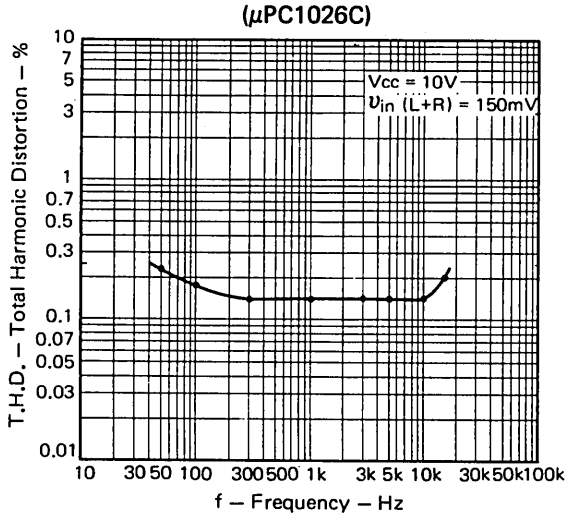


Fig. 53 MAXIMUM INPUT LEVEL vs. SUPPLY VOLTAGE (μPC1026C)

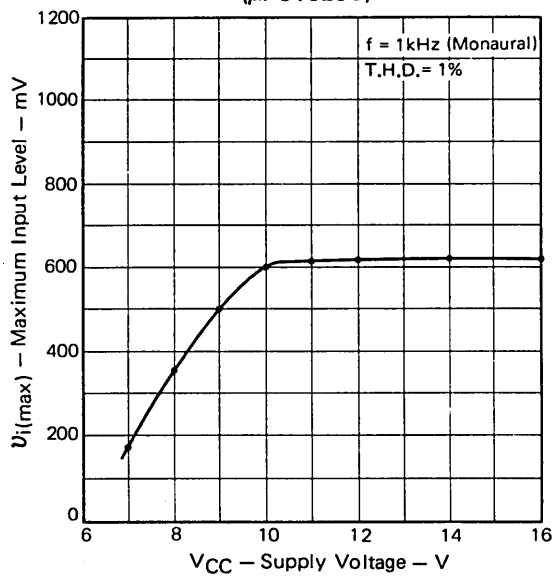


Fig. 54 SEPARATION vs. OSCILLATOR FREE RUNNING FREQUENCY (μPC1026C)

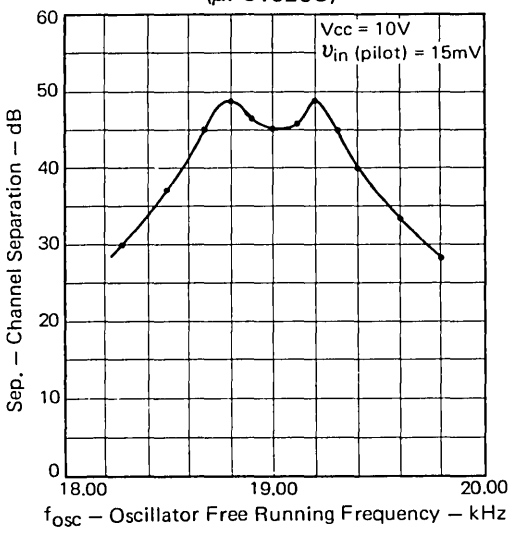


Fig. 55 OSCILLATOR FREE RUNNING FREQUENCY vs. AMBIENT TEMPERATURE (μPC1026C)

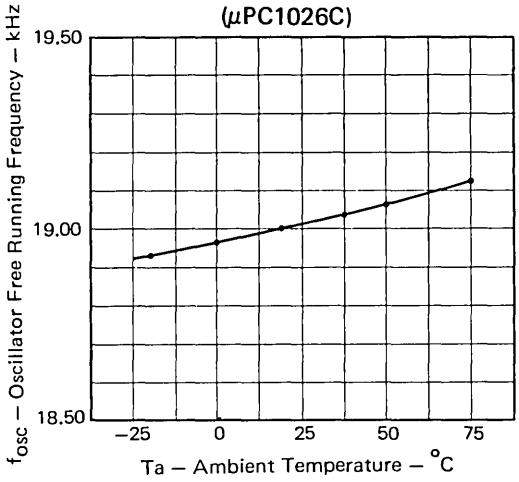


Fig. 56 POWER DISSIPATION AND SATURATION VOLTAGE OF LAMP DRIVER vs. LAMP CURRENT. (μPC1026C)

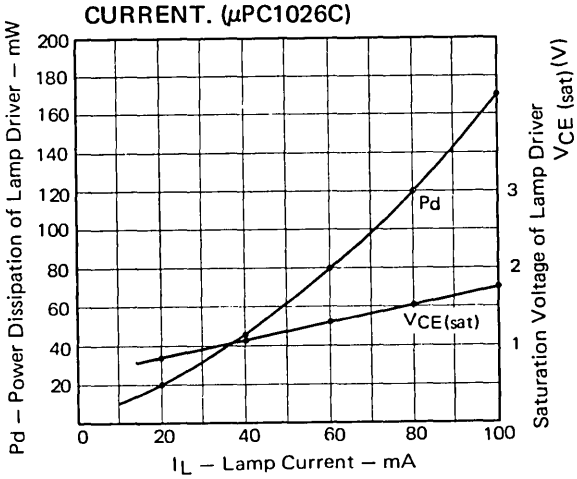


Fig. 57 OSCILLATOR FREE RUNNING FREQUENCY vs. ELAPSING TIME (μPC1026C)

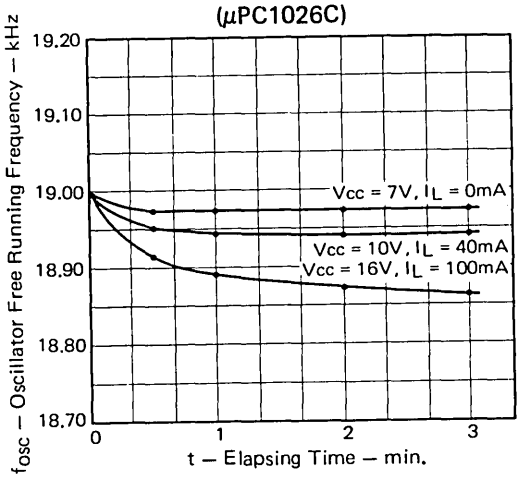


Fig. 58 CAPTURE RANGE vs. AMBIENT TEMPERATURE (μPC1026C)

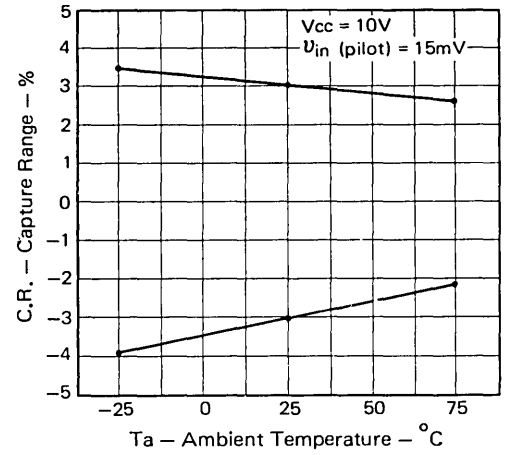


Fig. 59 LAMP TERN ON AND TURN OFF SENSITIVITY vs. TEMPERATURE (μPC1026C)

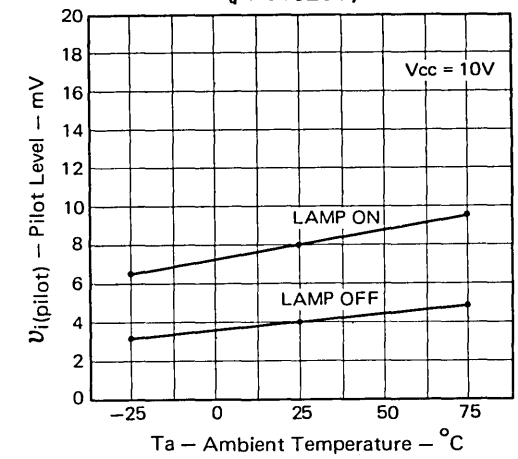


Fig. 60 POWER DISSIPATION vs. SUPPLY VOLTAGE (μPC1026C)

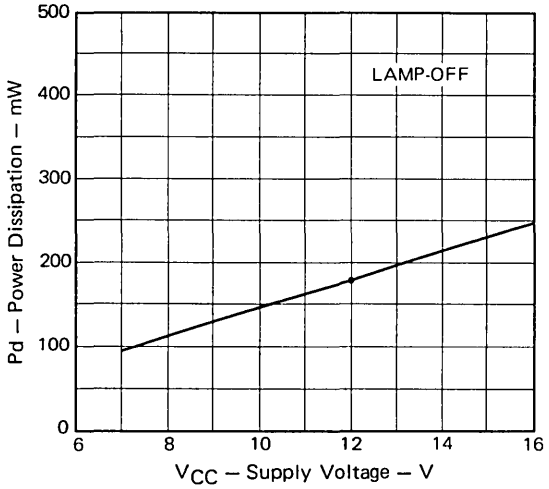


Fig. 61 CAPTURE RANGE (μPC1026C)

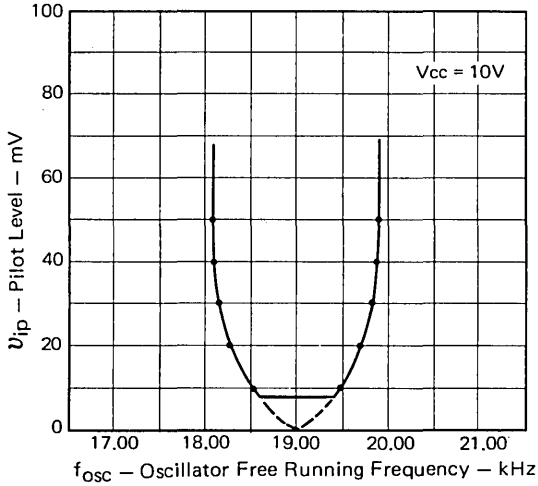


Fig. 62 Typical Application of the μPC587C2

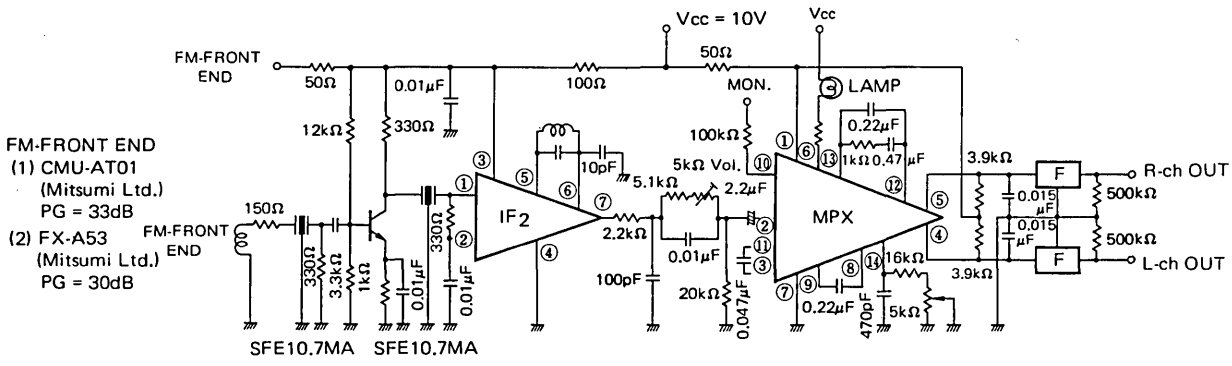


Fig. 63 Typical Application of the μPC1026C

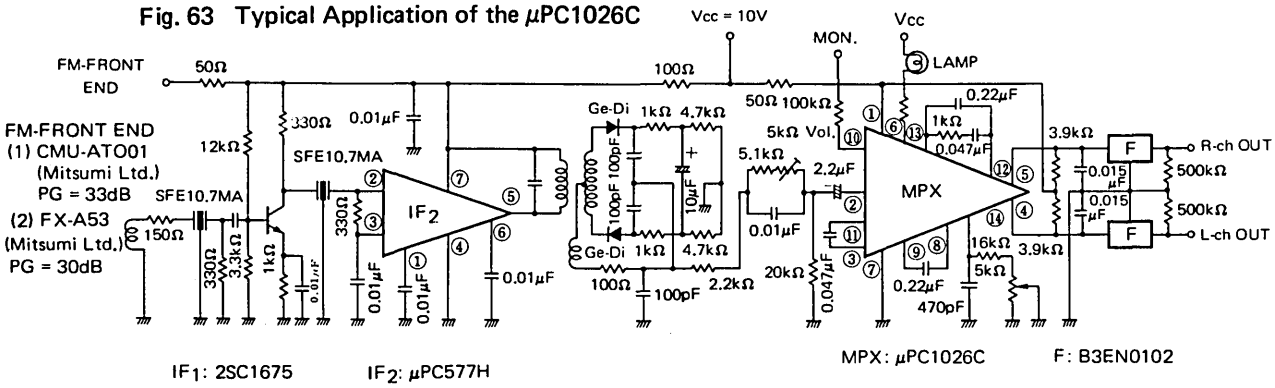


Fig. 64 MPX OUTPUT VOLTAGE vs. ANTENNA INPUT LEVEL

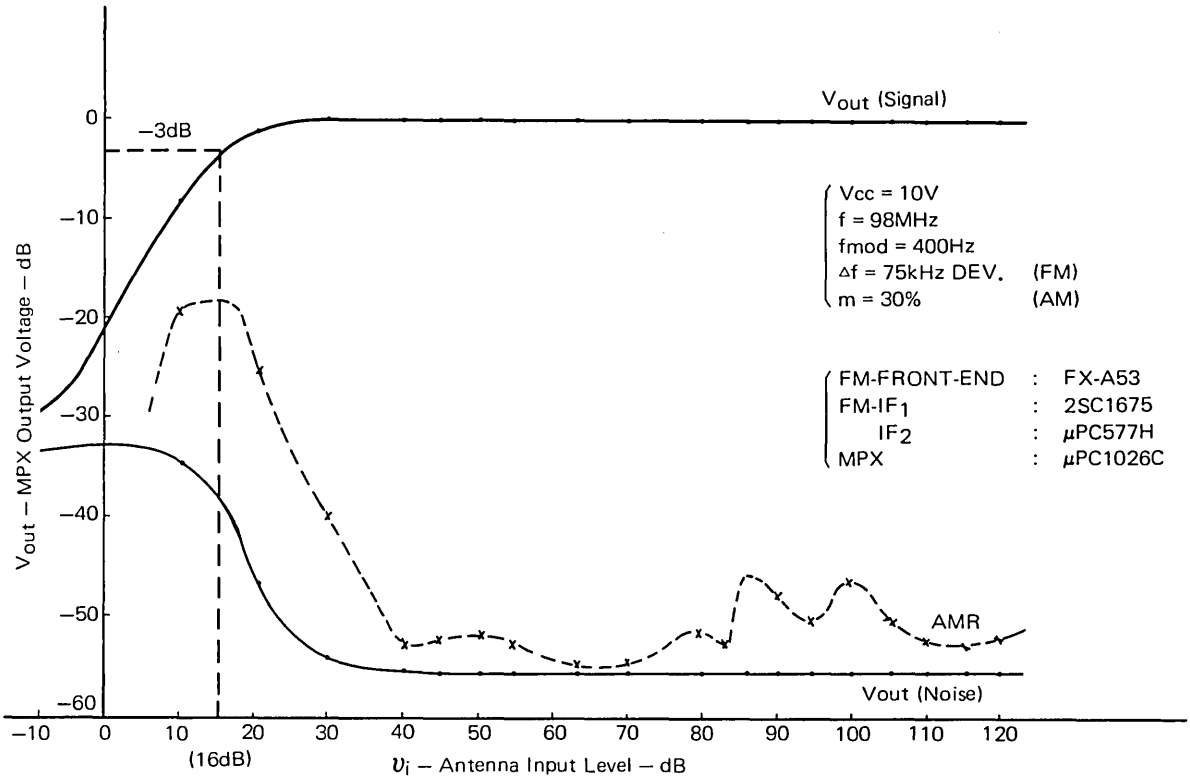


Fig. 65 CHANNEL SEPARATION, TOTAL HARMONIC DISTORTION vs. ANTENNA INPUT LEVEL

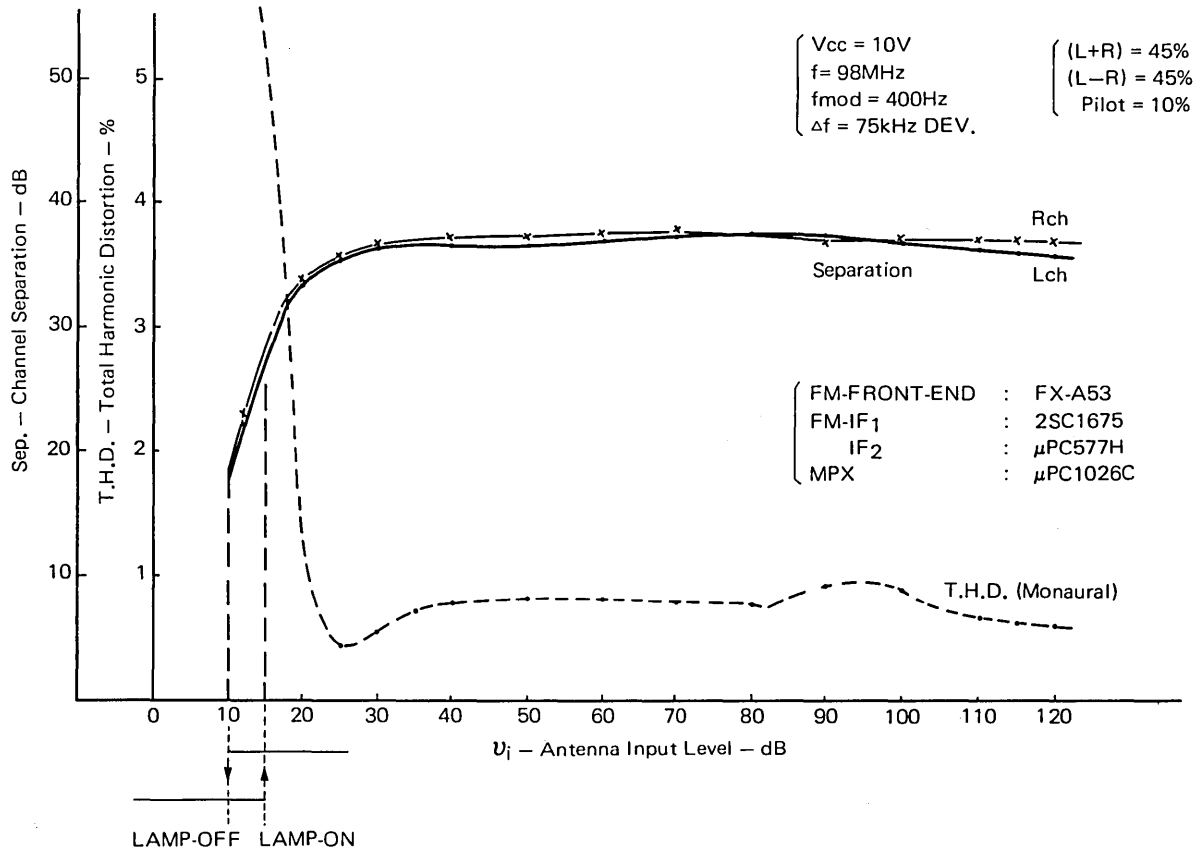
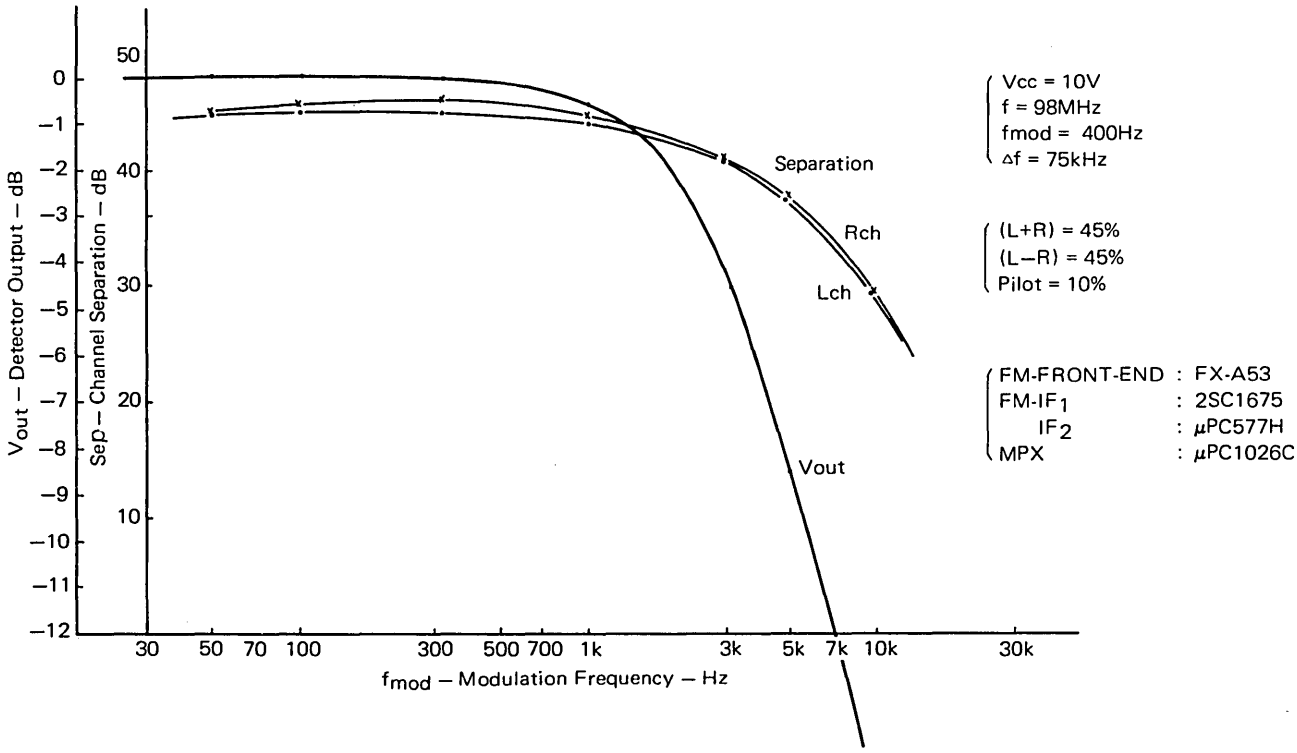


Fig. 66 DETECTOR OUTPUT, CHANNEL SEPARATION vs. MODULATION FREQUENCY



EXPLANATION OF CIRCUIT OPERATION OF FM NOISE CANCELLER IC μPC1176C

1. GENERAL

The automobile-mounted audio equipment (car radio) has come to such a sophisticated, upgraded level that noises originating from the automobile are not negligible and a means is required to protect the car radio from noises. Car noises generated by the ignition system, wipers, alternator, and many other components are radiated into and out of the car or superposed on the power supply line and enter the car radio. Most noises are suppressed by antenna circuits and power filter, but the remainder has to be removed by means of electrical circuit such as this noise canceller.

This pamphlet describes the performance of FM noise canceller IC μPC1176C which is designed to remove these noises in the FM radio.

2. EXPLANATION OF CIRCUIT OPERATION

2-1. Principle of Circuit Operation

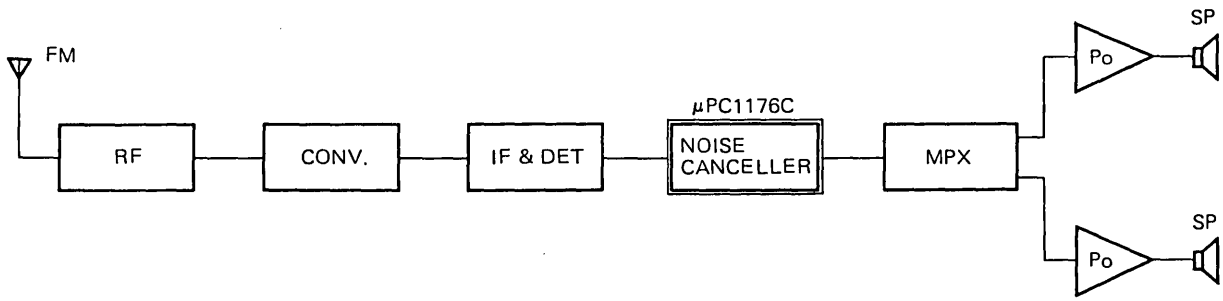


Fig. 1 Block Diagram of FM Radio Using Noise Canceller

As shown in Fig. 1, the noise canceller is placed after the detector and used in the audio frequency band. The principle of the noise canceller is described with reference to Figs. 2 and 3.

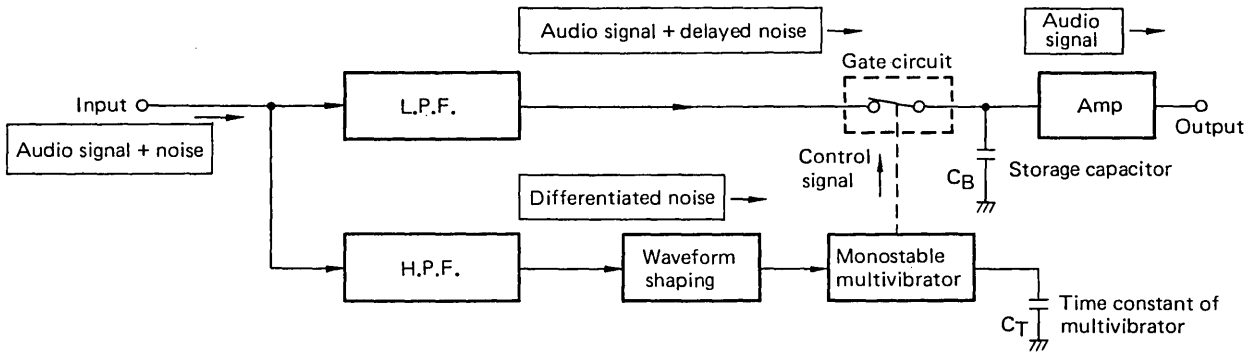


Fig. 2 Principle of Noise Canceller

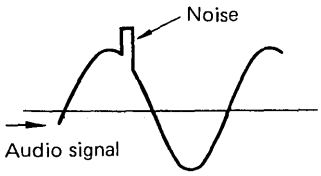


Fig. 3 Audio Signal Waveform with Superposed Noise

Suppose that the input signal has a waveform of audio signal with superposed noise (pulse waveform) as shown in Fig. 3.

(1) The incoming signal is processed first by the LPF to separate high-frequency components and to delay the phase of the superposed noise waveform. (LPF is also called a delay circuit). On passing through the LPF, the signal goes to the normally closed gate and then to the output.

(2) The input signal also branches to the HPF by which the noise waveform is differentiated. (HPF is also called a differentiating circuit.)

(3) On passing through the HPF, the noise waveform goes to the waveform shaping circuit and to the monostable multivibrator which operates when triggered by the leading or trailing edge of the noise waveform.

(4) The output of the monostable multivibrator transmits to the gate circuit control signals to open and close the gate.

On entrance of a noise as shown in Fig. 3, the HPF detects it, causing the multivibrator to generate a control signal to open the gate. The duration (blanking time) in which the gate is kept open is determined by the time constant of C_T.

Thus, the output waveform from the LPF is cut off as long as the noise exists and the noise waveform is eliminated. In order to prevent the partial loss of waveform (as depicted by dotted lines in Fig. 4) from occurring when the gate is held open, the storage capacitor C_B is provided as shown in Fig. 2. This capacitor maintains the level at the time just before the gate is opened and makes the waveform continuous.

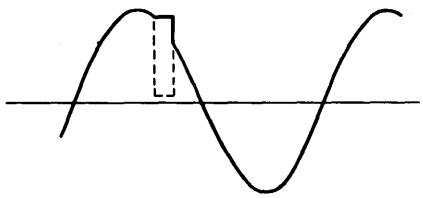


Fig. 4 Continuous Waveform Provided by C_B

The above-mentioned explanation is illustrated by Figs. 5 and 6.

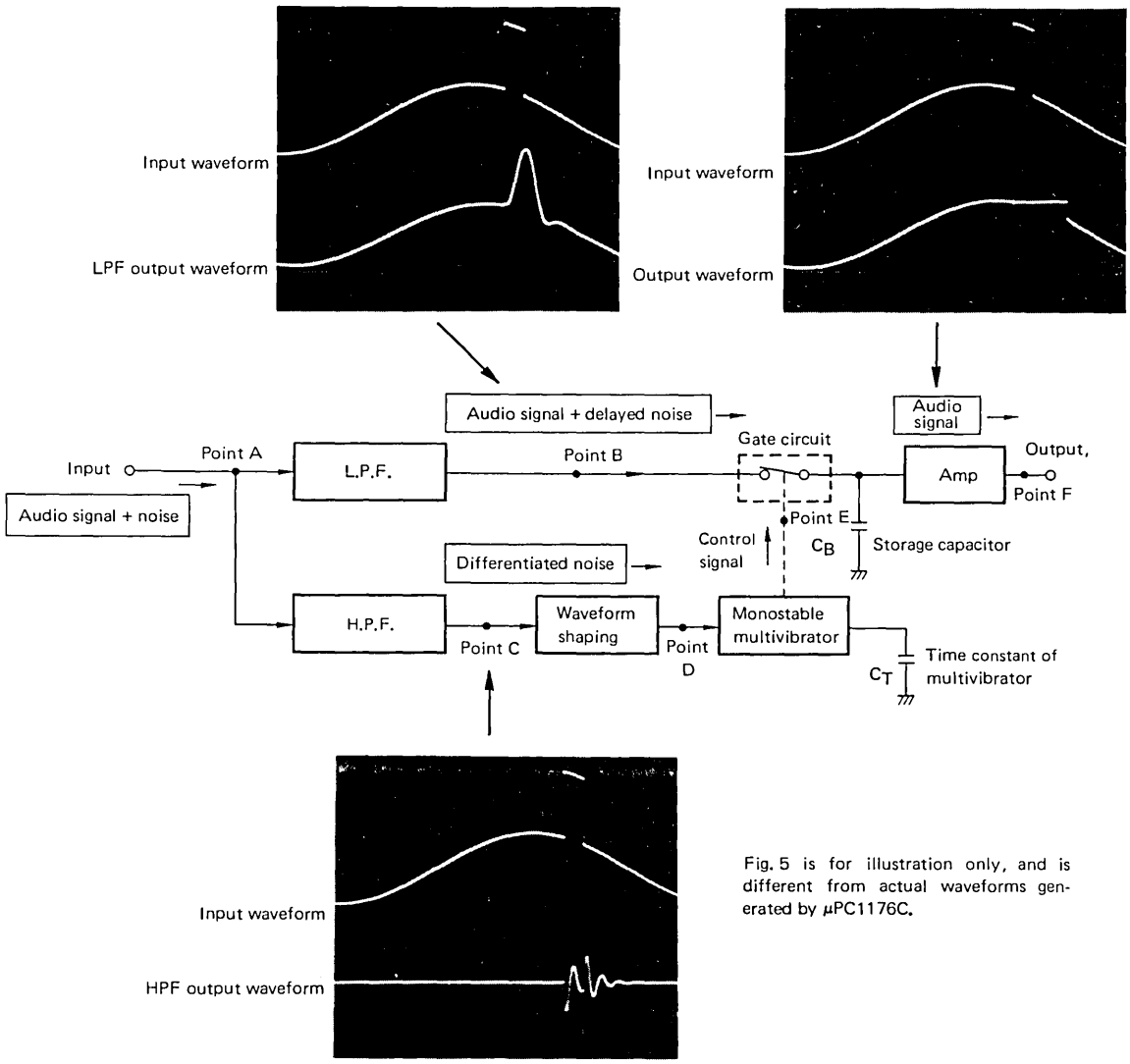


Fig. 5 is for illustration only, and is different from actual waveforms generated by μPC1176C.

Fig. 5 Operation of Noise Canceller

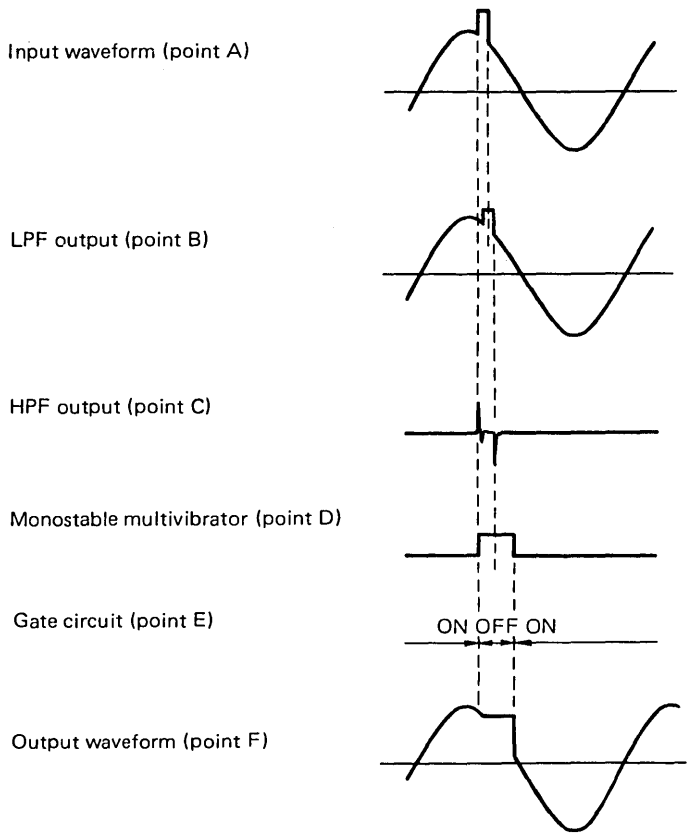


Fig. 6 Timing of Waveforms at Six Points

2.2 Additional Circuits

In addition to the main circuits mentioned in 2.1, μPC1176C contains the following additional circuits.

(1) Continuous noise control circuit

Continuous noises cause the gate circuit to open and close repeatedly, and this in turn causes the original signals (audio signals) to be distorted, with S/N ratio impaired. This circuit decreases the noise detecting sensitivity (trigger sensitivity) on entrance of continuous noises.

(2) Stereo signal holding circuit

The waveform of the pilot signal contained in the input signal of stereophonic broadcasting would be distorted as shown in Fig. 7 if the gate circuit is actuated by a noise in the pilot signal. Such a distorted waveform aggravates the distortion and S/N ratio. To avoid this inconvenience, the stereo signal holding circuit is provided which maintains the waveform of the pilot signal, as indicated by a broken line in Fig. 7, even when the gate is opened.

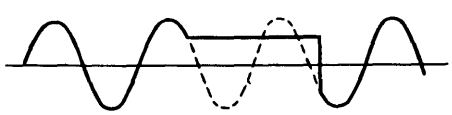


Fig. 7 Waveform of Pilot Signal, with Gate Circuit Opened

3. EXPLANATION OF CIRCUIT OPERATION

This section describes the construction of μPC1176C and its peripheral circuits.

The block diagram of μPC1176C is shown in Fig. 8.

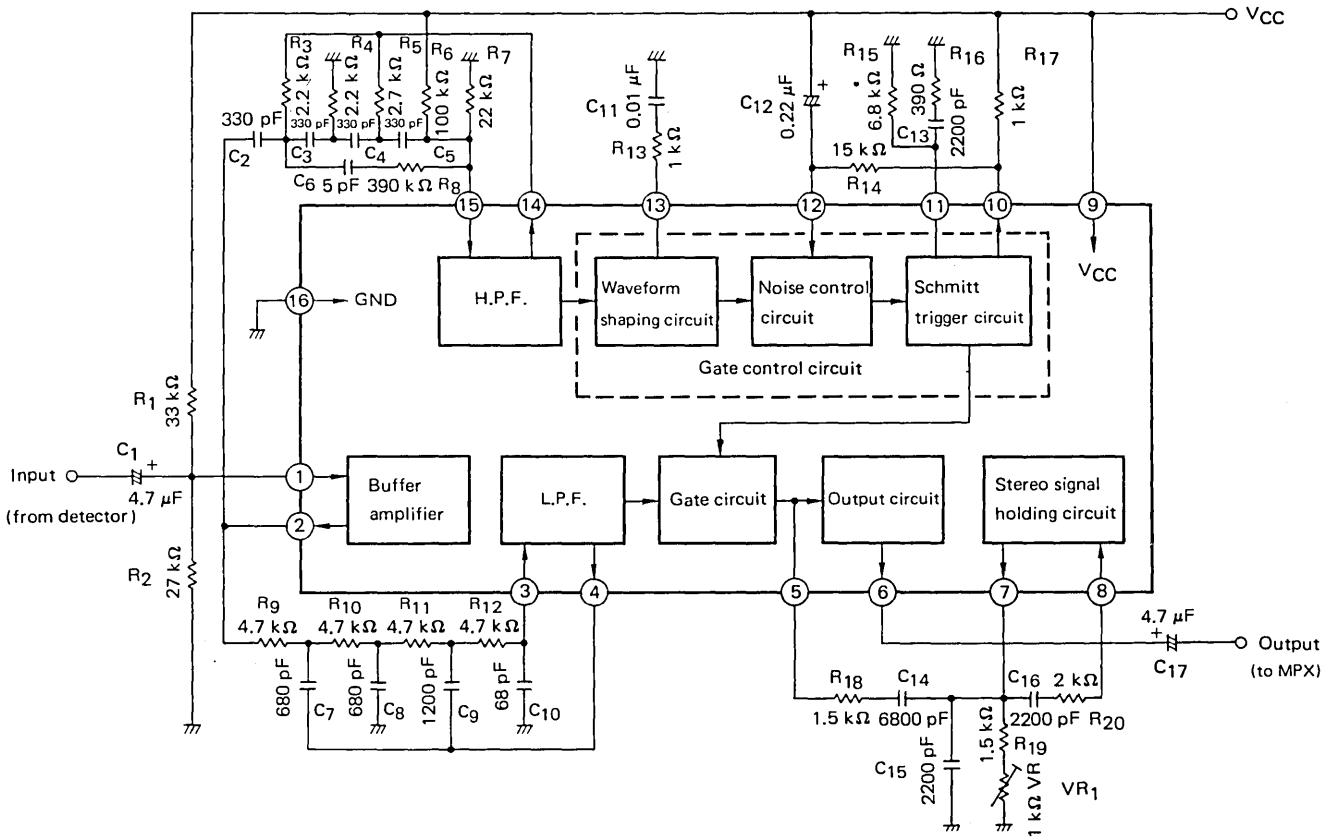


Fig. 8 Block Diagram of μPC1176C and Typical Peripheral Circuits

3.1 Buffer Amplifier

The buffer amplifier is of emitter follower type, as shown in Fig. 9, in which R_1 and R_2 are the bias resistor of the circuit. The input signal entering this buffer amplifier is output from pin 2 which is connected to LPF and HPF.

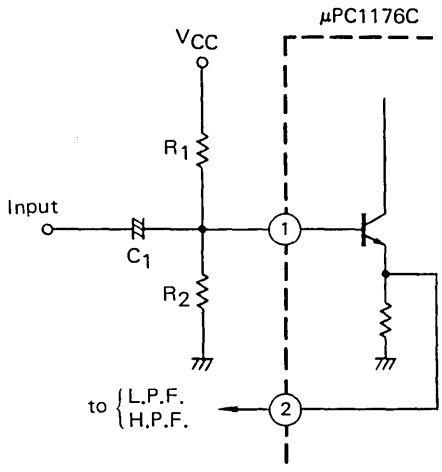


Fig. 9 Buffer Amplifier Circuit

3.2 LPF (Delay Circuit)

The LPF consists of a positive feedback active filter as shown in Fig. 10. The input signal is introduced to the gate circuit through the LPF. Being delayed by the LPF, the noise component in the input signal does not reach the output circuit before the gate is opened. Fig. 11 shows the frequency characteristic of the LPF at the constants shown in Fig. 10 and the cut-off frequency f_H of 75 kHz.

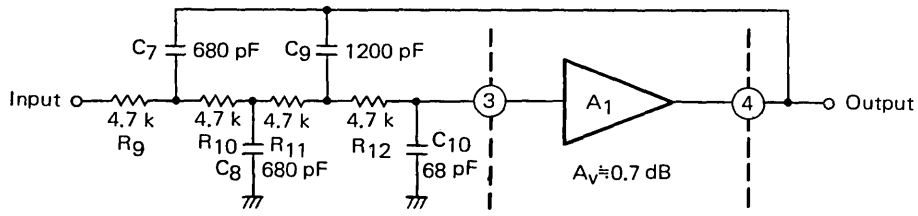


Fig. 10 LPF Circuit

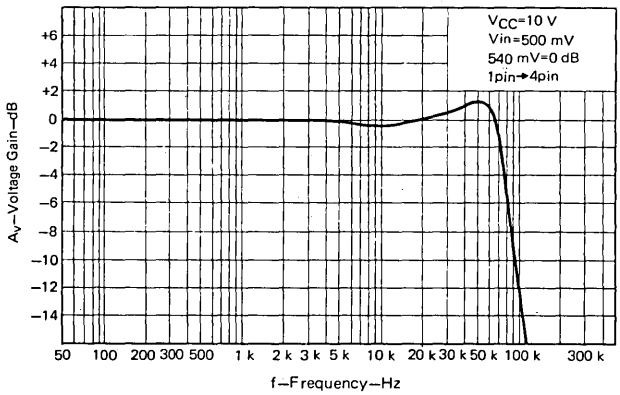


Fig. 11 Frequency Characteristic of LPF

3.3 HPF

As with the LPF, the HPF consists of an active filter. The HPF detects the differentiated noise in the input signal and sends it to the waveform shaping circuit. Fig. 13 shows the frequency characteristic of the HPF at the constants shown in Fig. 12 and the cut-off frequency f_L of 100 kHz.

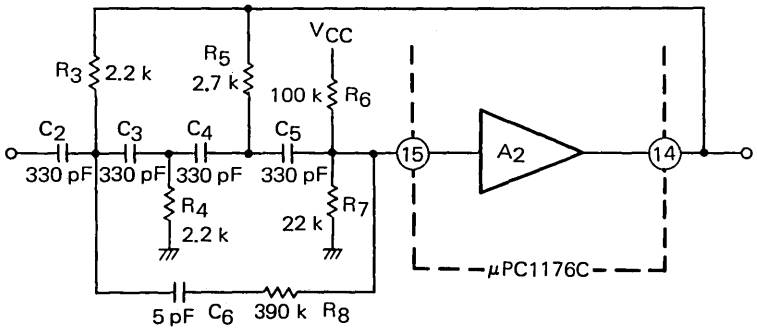


Fig. 12 HPF Circuit

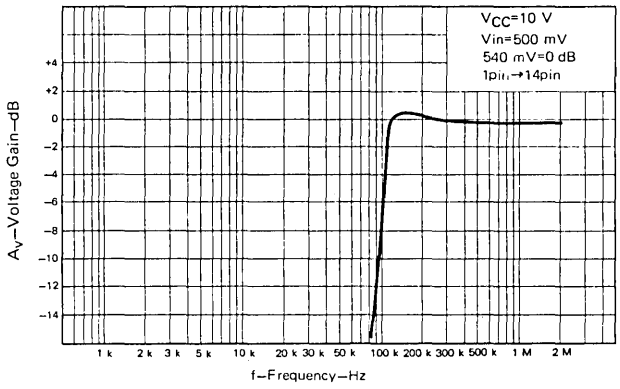


Fig. 13 Frequency Characteristic of HPF

3.4 Waveform Shaping Circuit

The function of this circuit is to raise the level to such an extent as to actuate the monostable multivibrator in the next stage and to shape the waveform so that either positive pulse noise and negative pulse noise will trigger the multivibrator.

As shown in Fig. 14, wave shaping is accomplished by a differential preamplifier, whose gain is adjusted by R_{13} so that a proper level of gate sensitivity (to detect noise and actuate the gate circuit) can be established.

Fig. 15 shows the gate sensitivity vs. resistance R_{13}.

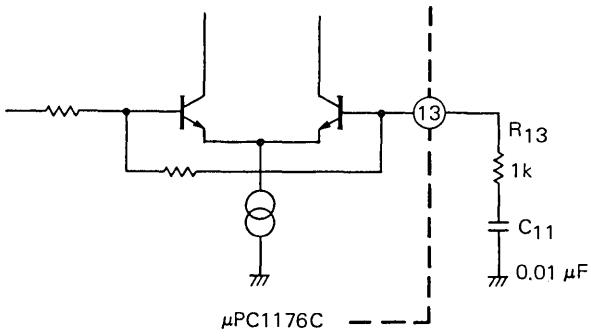


Fig. 14 Waveform Shaping Circuit

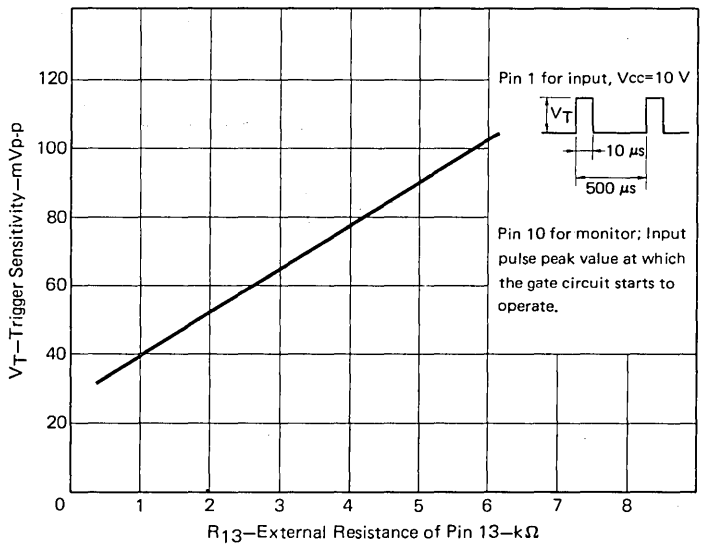


Fig. 15 Trigger Sensitivity vs. Resistance R_{13}

3.5 Continuous Noise Control Circuit

On entrance of noise, the monostable multivibrator operates and issues a control signal to open the gate, and a current proportional to this control signal flows to pin 10. If the noise is repeated at very short intervals (30 μs), the original signals are not allowed to come out. In order to avoid such inconvenience, this circuit is provided, which decreases the trigger sensitivity and closes the gate compulsorily so that the signals are passed as they are.

The detecting element of this circuit is illustrated in Fig. 16. The higher becomes the frequency of repetition of noise, the more is charged capacitor C_{12} at pin 12. Thus, the potential of pin 12 decreases, making TrQ_4 conductive and permitting a control signal to decrease the trigger sensitivity to be generated.

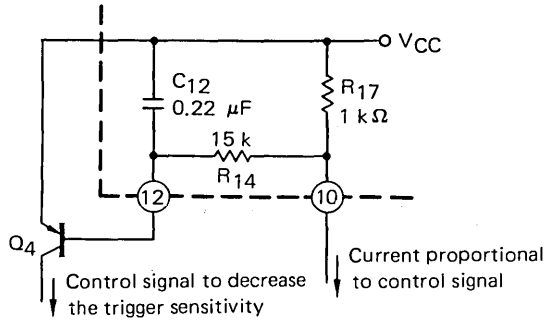


Fig. 16 Peripheral Circuit of Continuous Noise Control Circuit

3.6 Monostable Multivibrator

The monostable multivibrator is actuated by noise which has been detected by HPF and subjected to waveform shaping. On actuation, the monostable multivibrator sends a control pulse to the gate circuit to open the gate and cut off the original signals.

The time in which the gate is open is called blanking time, and its length is determined by the time constant circuit, i.e., C_{13} and R_{16} connected to pin 11.

Fig. 17 shows the blanking time vs. the capacitance C_{13}.

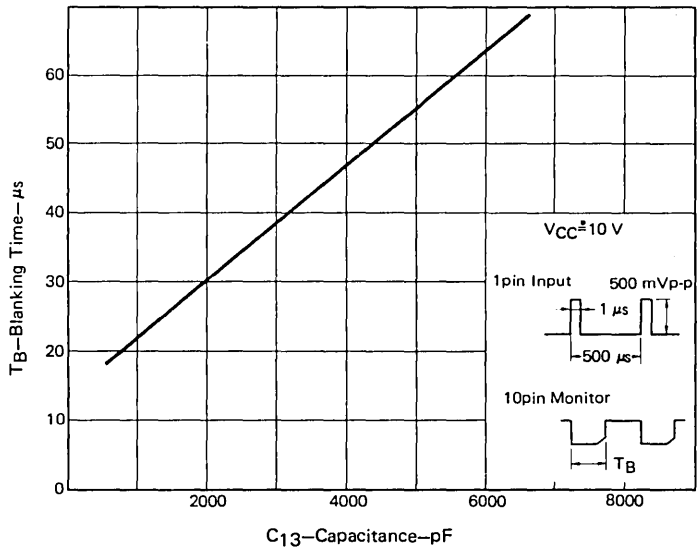


Fig. 17 Blanking Time vs. Capacitance C_{13}

3.7 Gate Circuit and Output Circuit

The gate transistor Q_5 is held conductive under normal conditions so that audio signals are transmitted at low impedance to the output circuit. On entrance of a noise pulse, however, the monostable multivibrator transmits a control signal to cut off the gate transistor so that the audio signal is not transmitted for a predetermined time (blanking time T_B=30 μs TYP). In this period of time, the level at the time just before the gate is opened is maintained by the effect of the storage capacitor C_{14}.

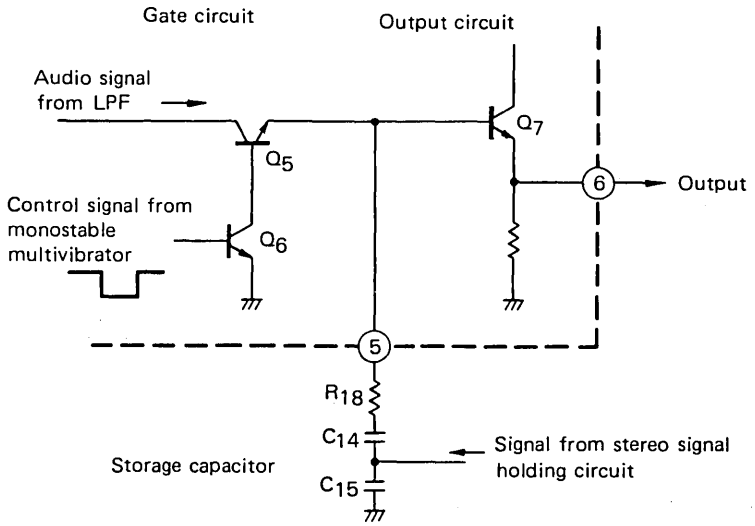


Fig. 18 Gate Circuit and Output Circuit

3.8 Stereo Signal Holding Circuit

As mentioned in Section 2.2, this circuit prevents the pilot signal of stereophonic broadcasting from being broken. The usage of this circuit is described in Section 8.3.

Peripheral circuits and their functions are shown in Fig. 19.

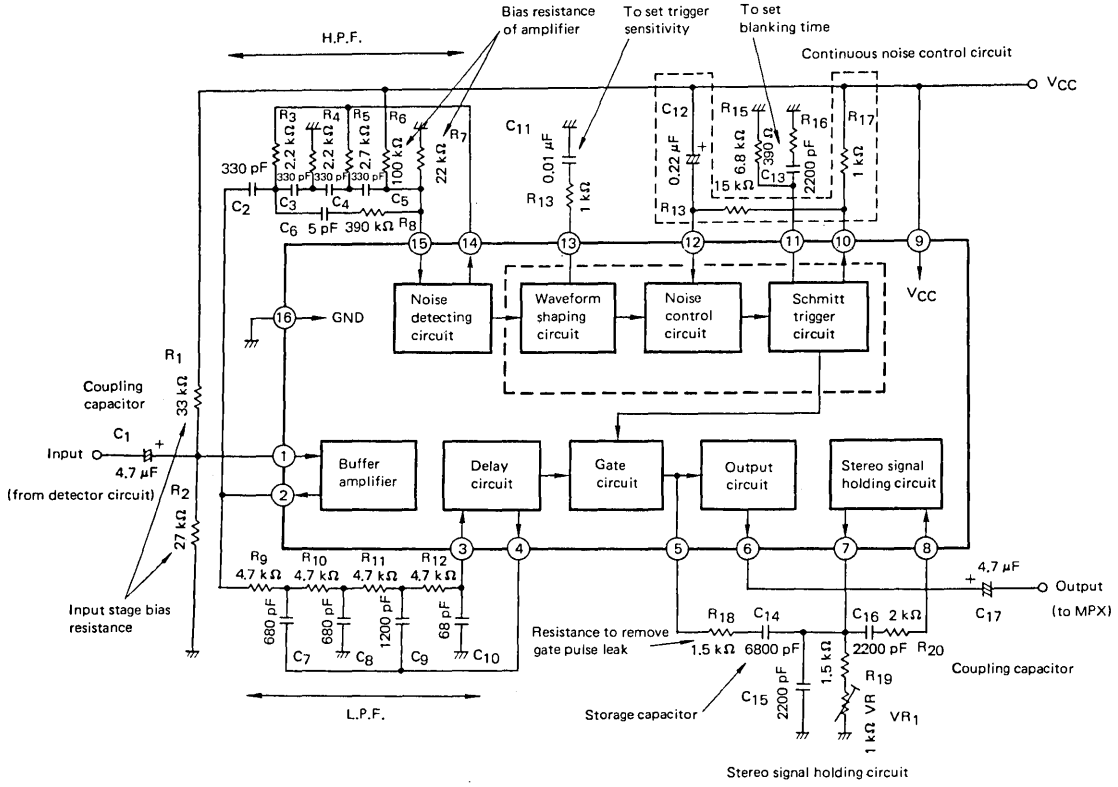


Fig. 19 Peripheral Circuits

3.9 Effect of Noise Canceller

The effect of μPC1176C on noise suppression was evaluated using a spectrum analyzer connected to the network as shown in Fig. 20.

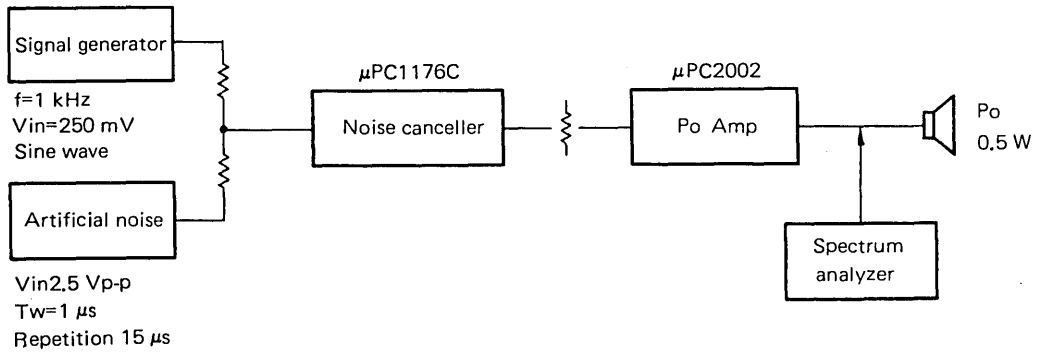


Fig. 20 Block Diagram of Network for Evaluating Noise Suppression by μPC1176C

The result of the evaluation is shown in Fig. 21. This is merely one example, and different results will be obtained depending on the timing of noise.

Photo 1
without artificial pulse;
waveform of power
amplifier alone.

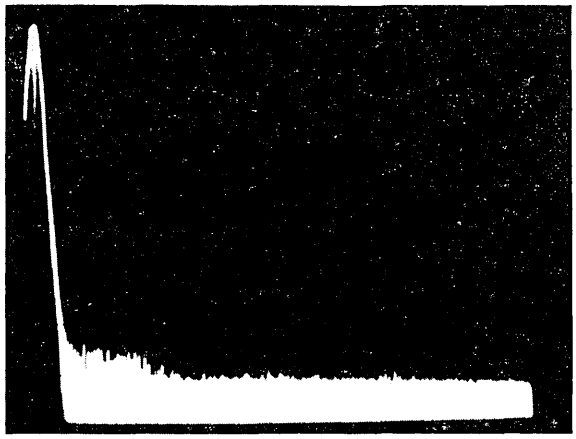


Photo 2
with artificial pulse;
without noise canceller

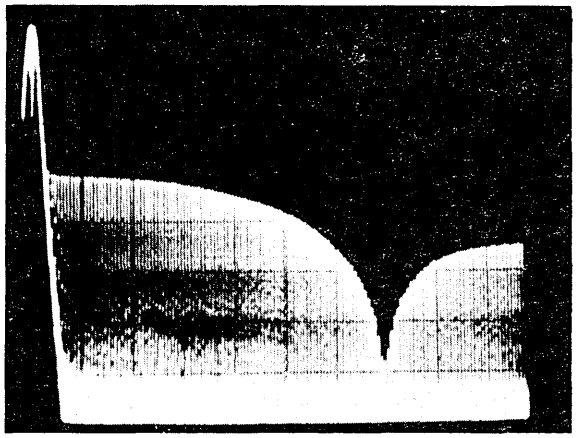
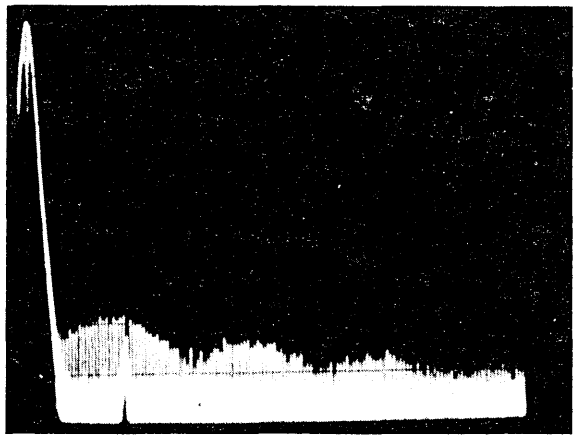


Photo 3
with artificial pulse;
with noise canceller on



SCAN-WIDTH
10 kHz/DIV
BAND-WIDTH 1 kHz
SCAN TIME 0.2 s/DIV

Fig. 21 Effect of μPC1176C on Noise Suppression

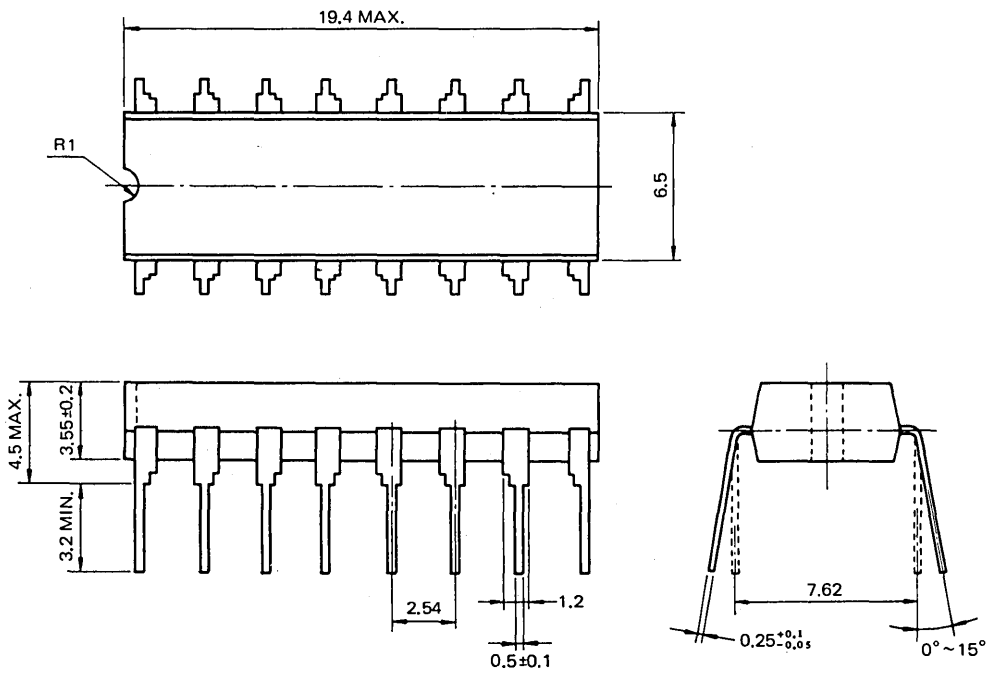
4. ABSOLUTE MAXIMUM RATING OF μPC1176C (Ta=25 °C)

Supply Voltage	V_{CC}	15	V
Package Dissipation	PD	350*	mW
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C
		*Ta=75 °C	

5. ELECTRICAL CHARACTERISTICS OF μPC1176C (Ta=25 °C, V_{CC}=10 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	I_{CC}	13	16.5	23	mA	v_i=0
Voltage Gain	A_V	−0.3	0.7	1.7	dB	v_i=500 mVr.m.s., f=1 kHz
Blanking Time	T_B		30		μs	v_i=500 mVp, f=1 kHz, tw=1 μs
Triggering Voltage	V_T		40		mVp	f=1 kHz, tw=10 μs

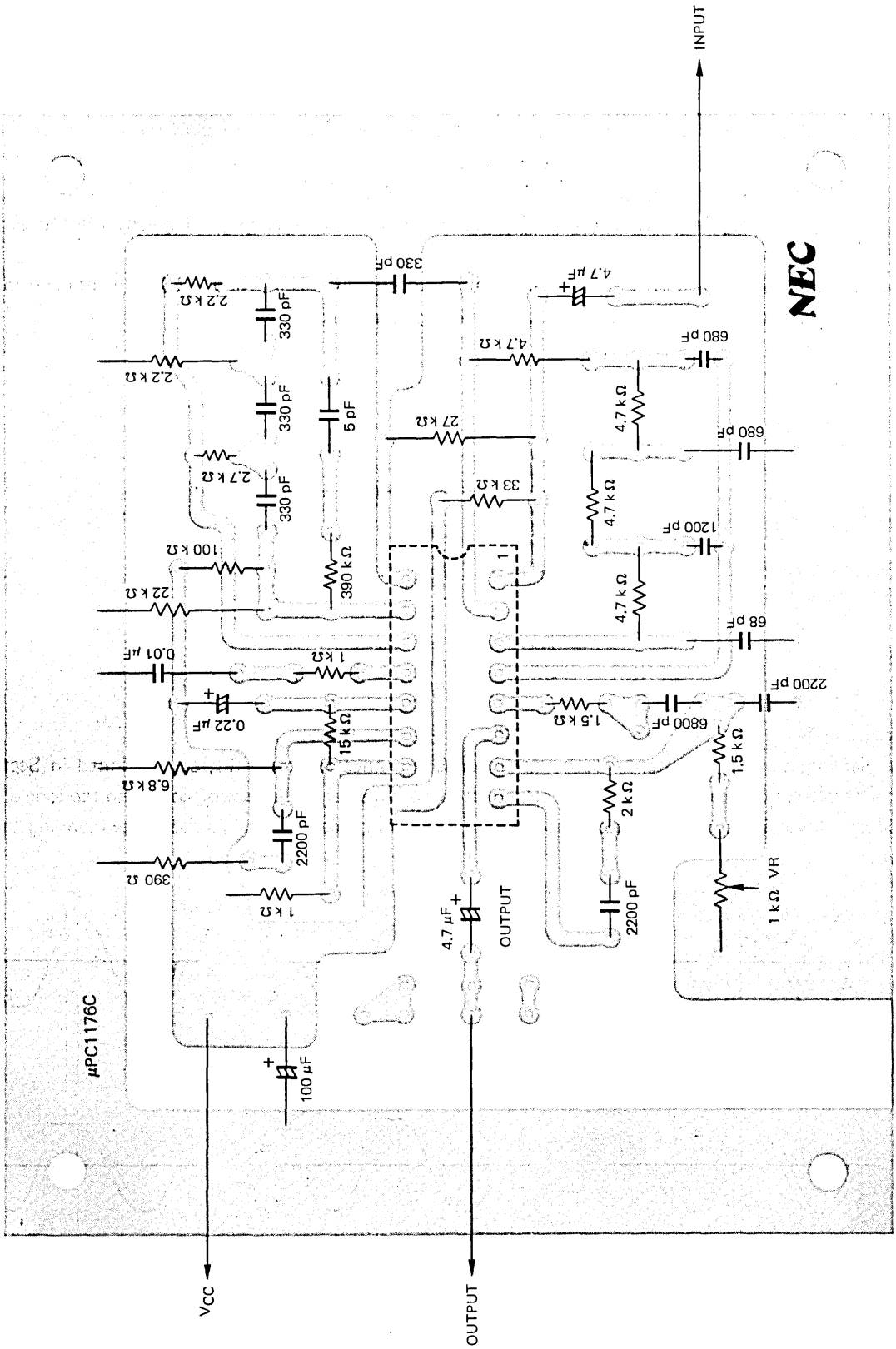
6. PACKAGE DIMENSIONS (in millimeters)



Unless otherwise specified, typical values are given.

7. PRINTED-CIRCUIT BOARD

Example of component mounting (bottom view)



8. PRECAUTIONS FOR USE OF μPC1176C

8.1 FM IF Stage and Detector Stage

As mentioned in Section 3.3, noise is detected by HPF, whose cut-off frequency is set at 100 kHz. Thus, it follows that noise components of higher frequencies than this are detected. Therefore, the FM IF stage should have a bandwidth (200 k to 300 kHz) broad enough to pass not only signal components (50 Hz to 53 kHz) but also noise components.

Noise (white noise) in the IF stage may cause malfunction in the noise canceller and deteriorate the S/N ratio. Due consideration should be made with respect to the noise characteristics of the IF stage including the front end. The noise canceller will be more effective when used in combination with NEC's IF IC μPC1200V or μPC1245V which exhibits a good S/N in weak electric fields.

Noise in the IF stage may be suppressed to some extent by connecting a high-cut filter (500 kHz) to pin 1.

When establishing the trigger sensitivity with resistance R_{13} connected to pin 13, as mentioned in Section 3.4, it is necessary that the front end, IF stage, and detector stage be connected.

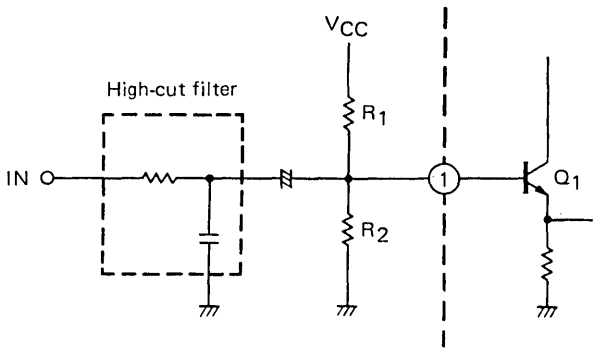
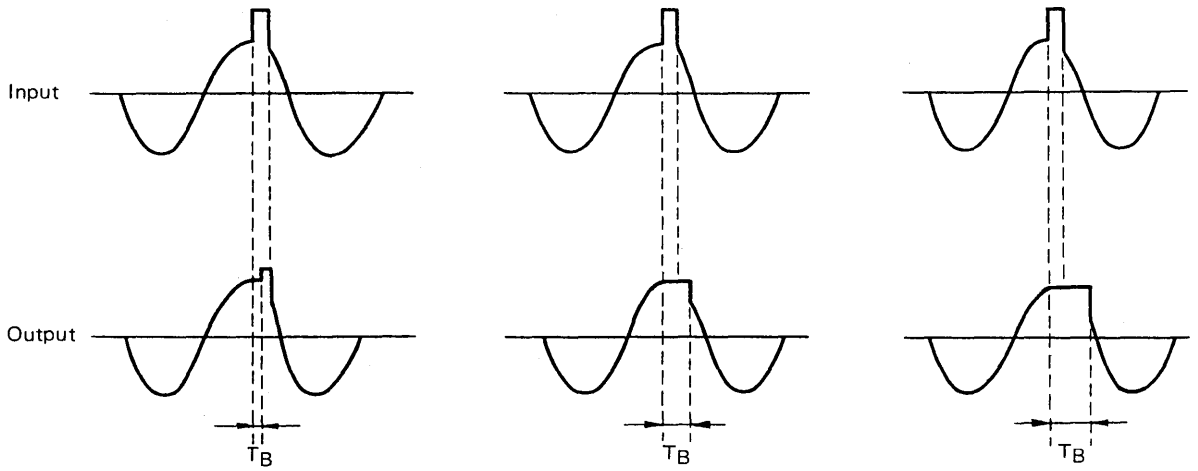


Fig. 22 High-cut Filter to Suppress IF Stage Noise

8.2 Blanking Time

The blanking time T_B is established by capacitor C_{13} connected to pin 11, as mentioned in Section 3.5. Too short a blanking time decreases the cancelling effect due to a partial leakage of noise; and too long a blanking time distorts the original signals and deteriorates the distortion. See Fig. 23. An adequate blanking time is 20 to 40 μs.



Leak of noise due to too short T_B | Adequate T_B | Distortion due to too long T_B

Fig. 23 Noise Pulse vs. Blanking Time

8.3 Stereo Signal Holding Circuit

(1) Holding of 19 kHz pilot signal

The pilot signal contained in stereophonic broadcasting will vary suddenly in its level, as shown in Fig. 7, when the gate is opened due to the presence of noise. This is the cause of parasitic noise. The 19 kHz holding circuit prevents the occurrence of this discontinuity and parasitic noise. The effect of this circuit will be more pronounced when the pilot signal alone is received or in the case where L and R signals are modulated to a lesser extent.

(2) Holding of 38 kHz subcarrier

In stereophonic broadcasting, not only the 19 kHz pilot signal but also the (L-R) subcarrier modulated by 38 kHz DSB (Double Side Band) are superposed on the original signal. Unless this signal is held when the gate is opened, the waveform is distorted after stereophonic demodulation. This effect is apparent when a signal of (L-R) sub, L only, or R only is received.

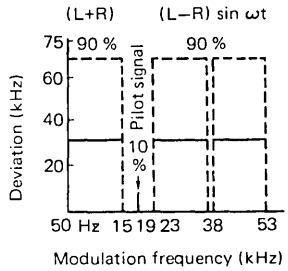


Fig. 24 Frequency Spectrum of Stereophonic Broadcasting

For the best operation of the noise canceller in the reception of stereophonic broadcasting, both 19 kHz pilot signal and 38 kHz subcarrier should be held simultaneously. In actual, however, either of them should be selected for the construction of μPC1176C circuit.

The holding circuit for 38 kHz subcarrier is recommended. Fig. 25 shows three circuit examples with 19 kHz or 38 kHz holding circuit and without holding circuit.

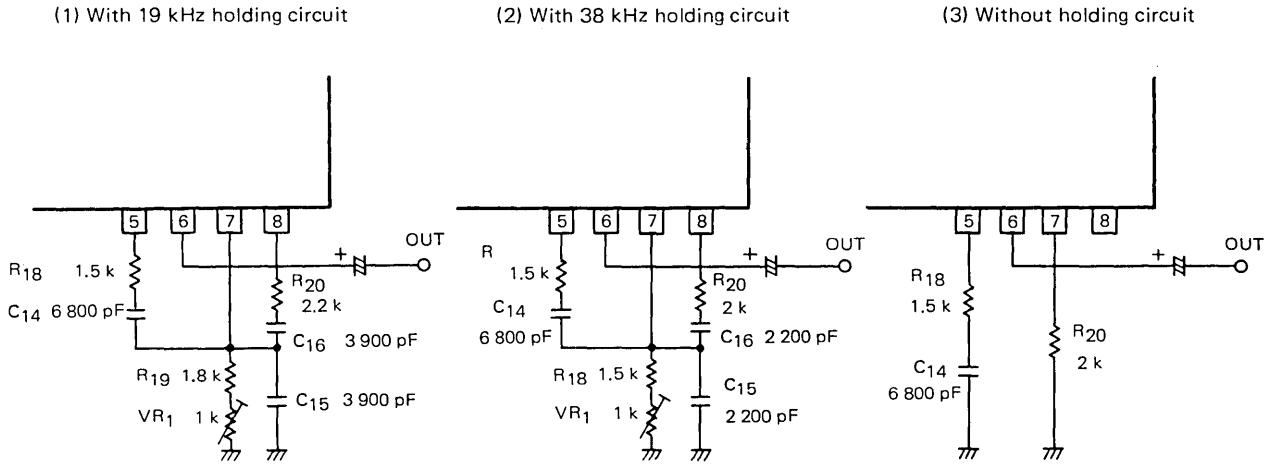
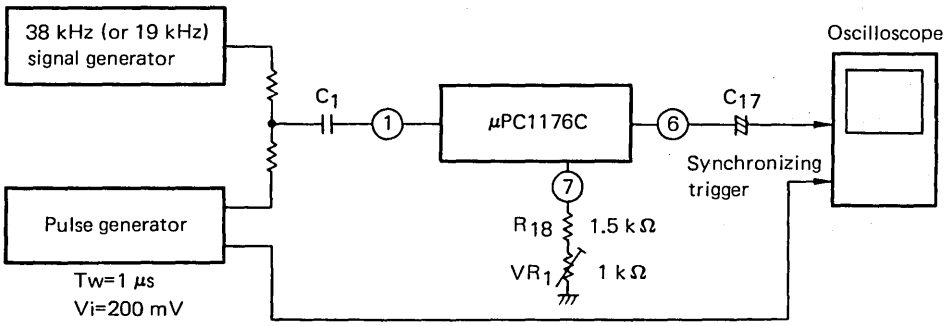


Fig. 25 Use of Holding Circuit

8.4 Adjustment of Stereo Signal Holding Circuit

The holding circuit for either 19 kHz or 38 kHz should be adjusted by VR_1 connected to pin 7 until the waveform becomes flat while watching the waveform on the oscilloscope arranged in the circuit as shown in Fig. 26.



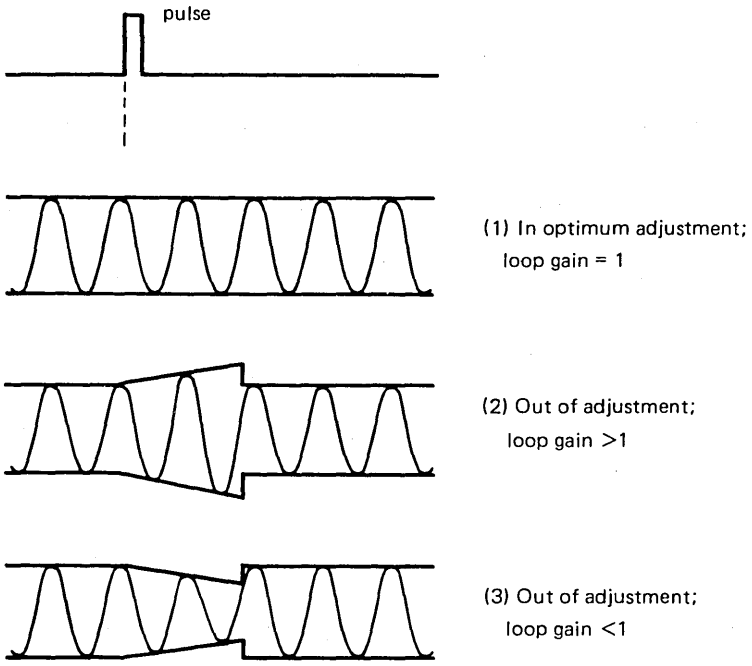


Fig. 26 Adjustment of Stereo Signal Holding Circuit

8.5 Connection with MPX

On processing by the noise canceller, the signal passes through the LPF (delay circuit) and the phase in the high frequency band rotates. In such case, separation becomes poor after stereo demodulation by the next MPX stage. This may be remedied by compensating the high frequency output of the noise canceller. See Fig. 27.

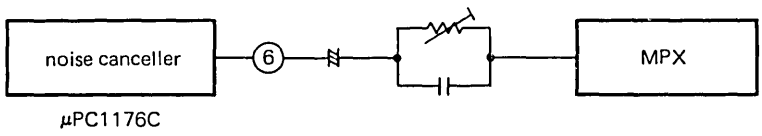


Fig. 27 High Frequency Compensation for Separation Adjustment

If NEC's MPX IC μPC1320C, μPC1187V or μPC1227V is used, good separation is obtained without compensation as shown in Fig. 27, because they are provided with a separation adjusting terminal for compensation.

9. BASIC CHARACTERISTICS OF μPC1176C

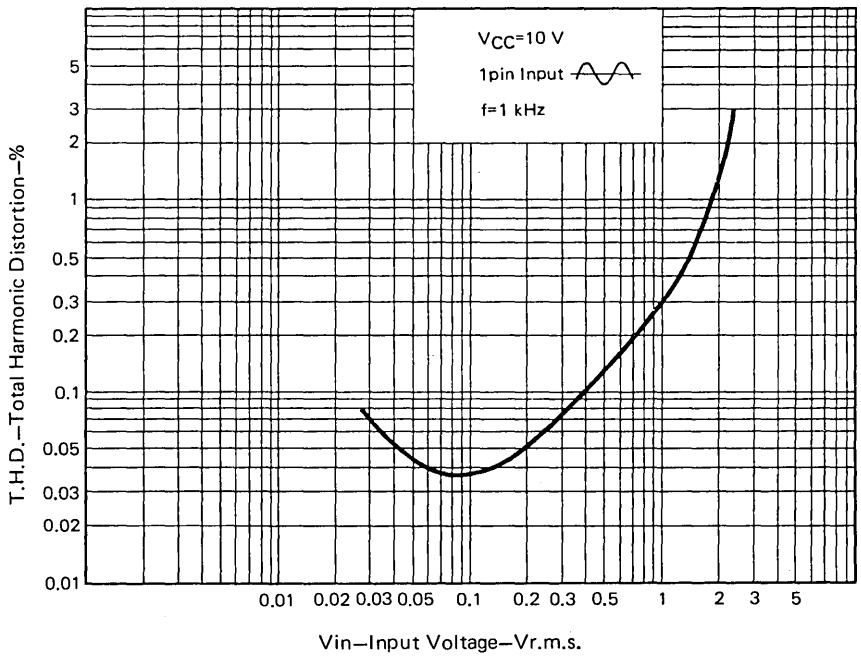


Fig. 28 Total Harmonic Distortion vs. Input Voltage

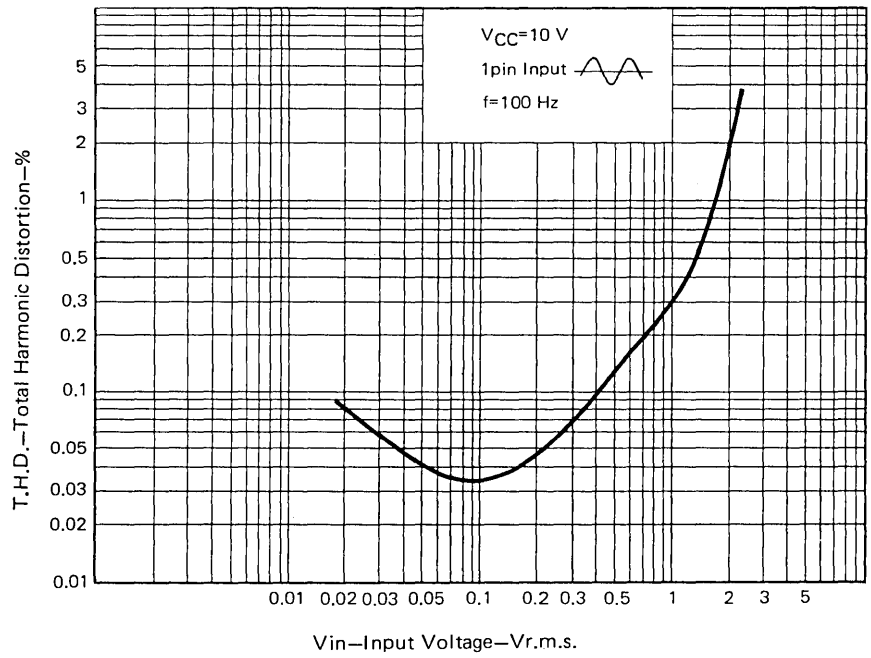


Fig. 29 Total Harmonic Distortion vs. Input Voltage

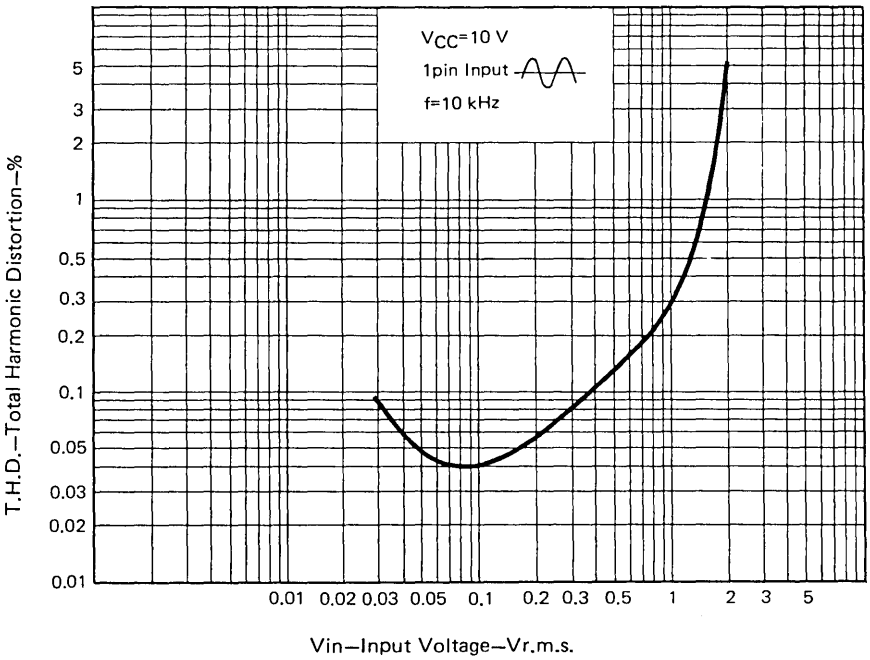


Fig. 30 Total Harmonic Distortion vs. Input Voltage

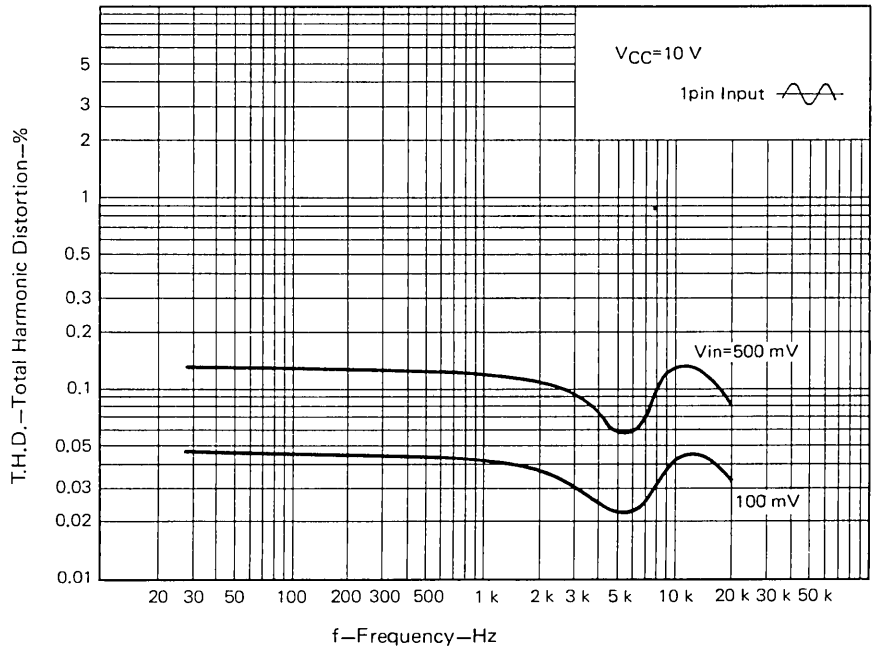


Fig. 31 Total Harmonic Distortion vs. Frequency

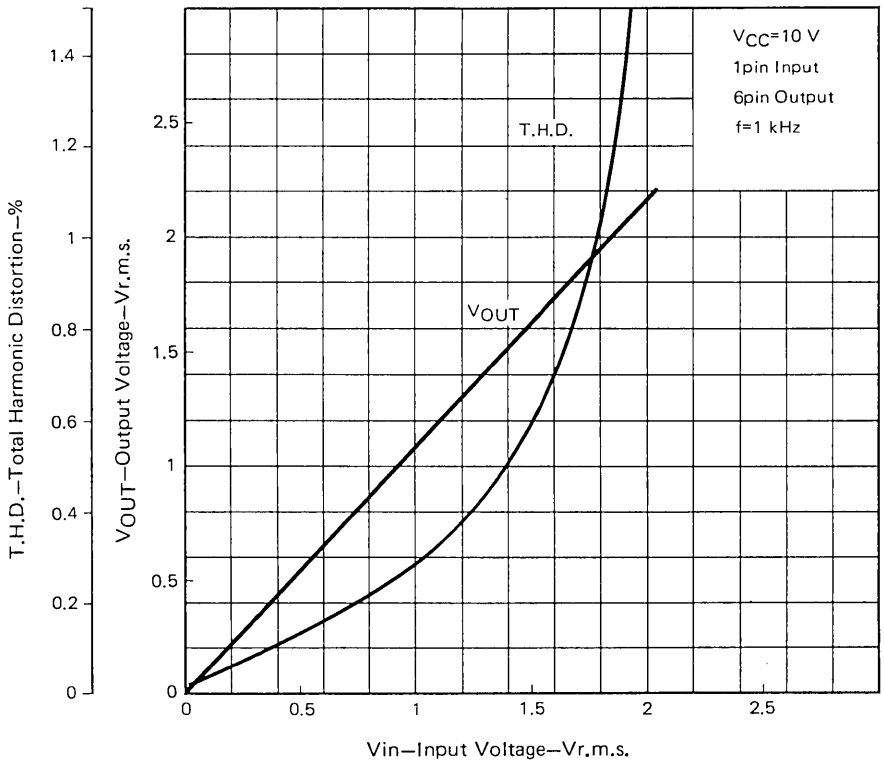


Fig. 32 Total Harmonic Distortion, Output Voltage vs. Input Voltage

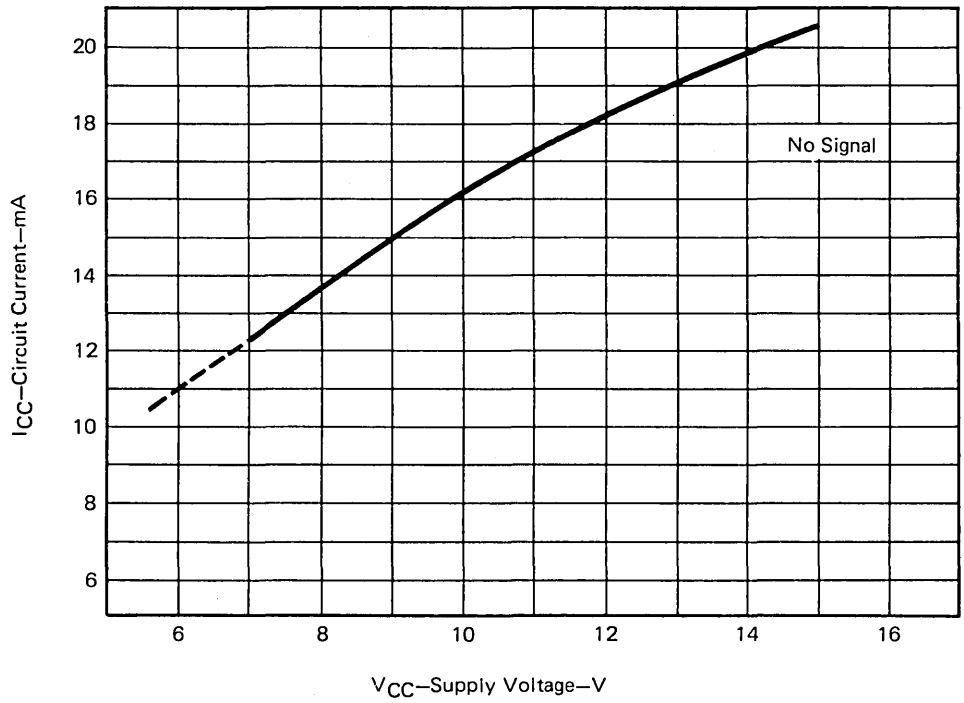


Fig. 33 Circuit Current vs. Supply Voltage

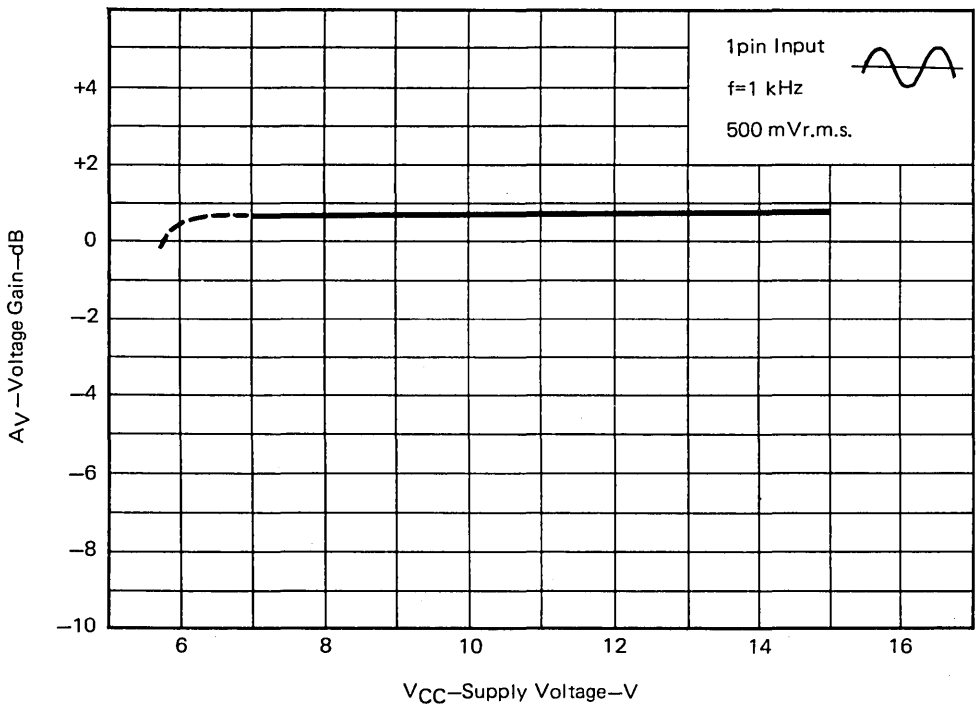


Fig. 34 Voltage Gain vs. Supply Voltage

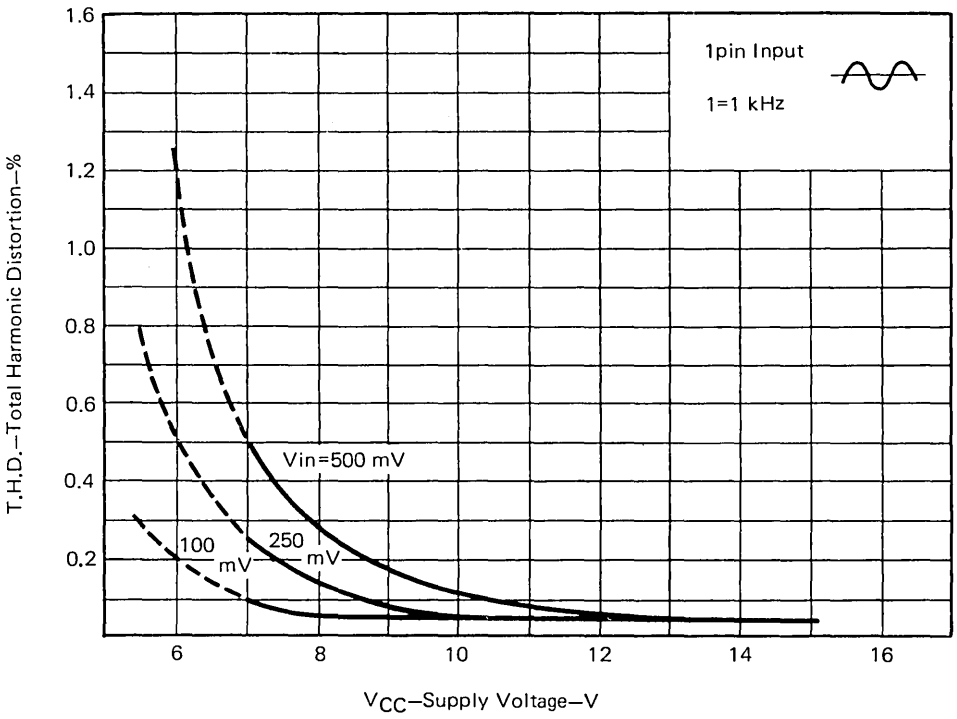


Fig. 35 Total Harmonic Distortion vs. Supply Voltage

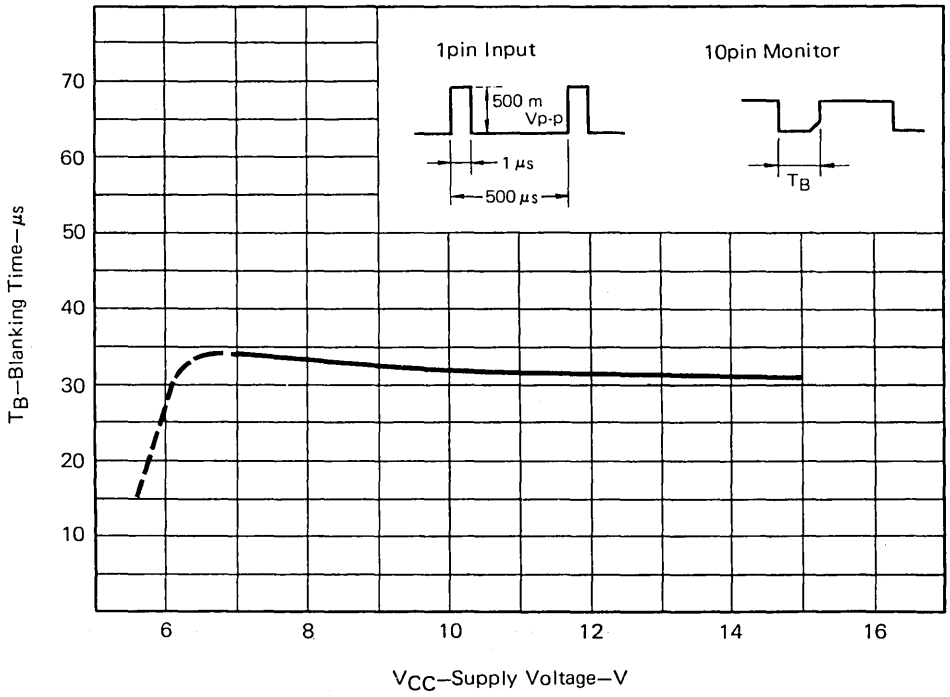


Fig. 36 Blanking Time vs. Supply Voltage

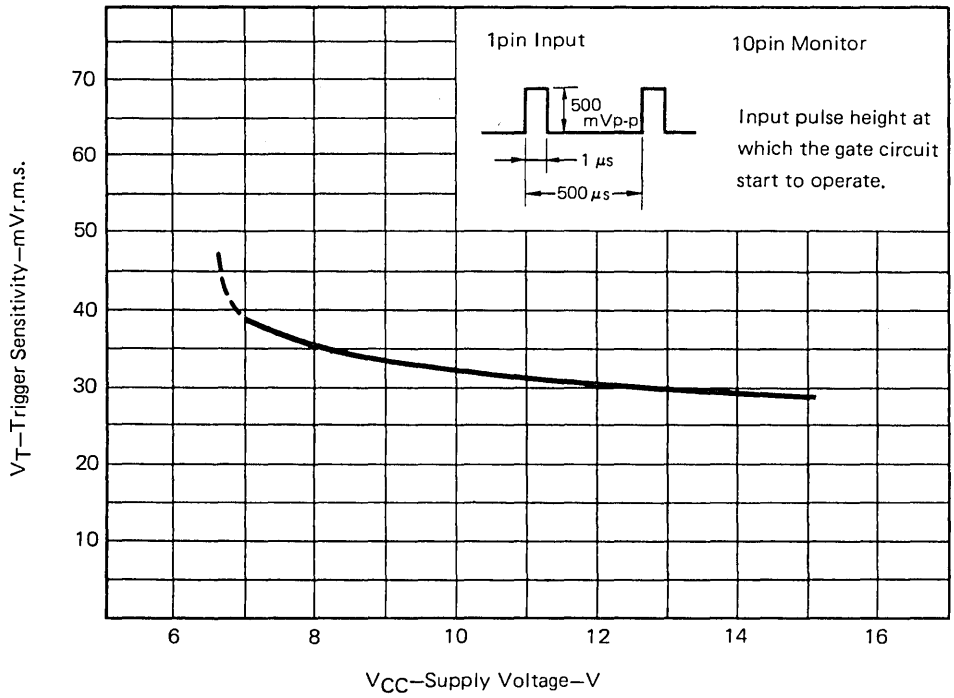


Fig. 37 Trigger Sensitivity vs. Supply Voltage

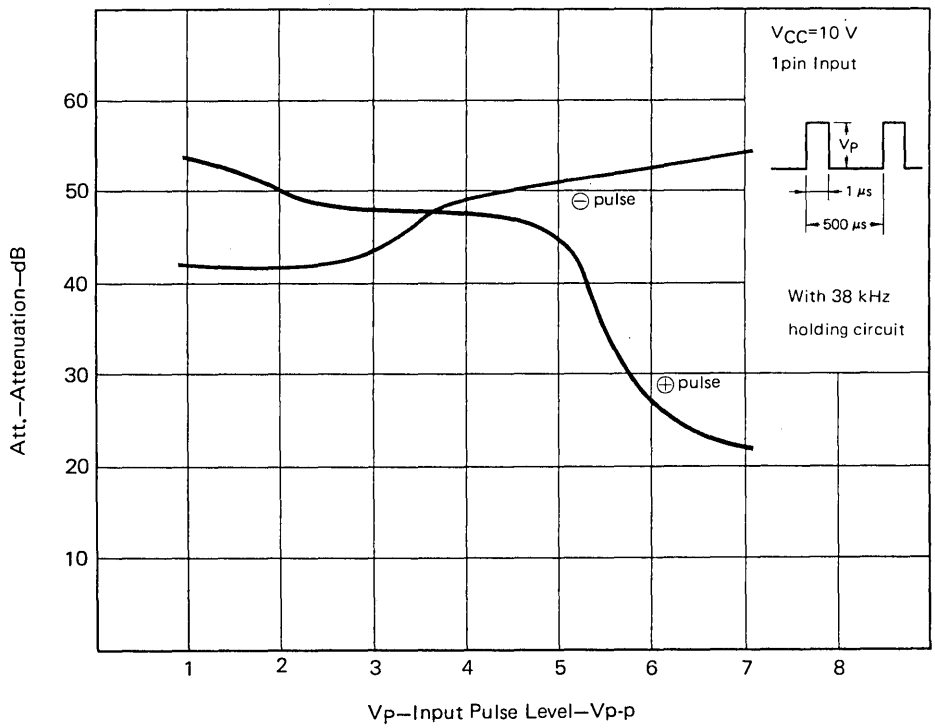


Fig. 38 Attenuation vs. Input Pulse Level

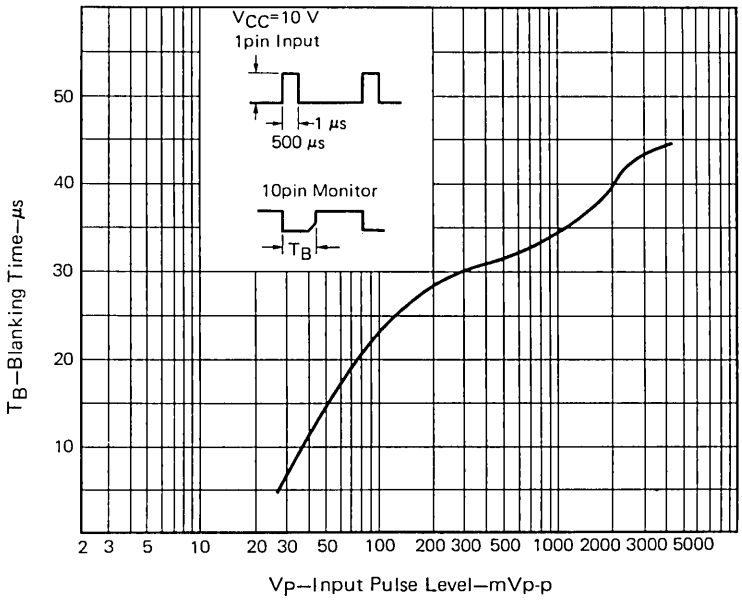


Fig. 39 Blanking Time vs. Input Pulse Level

10. EPILOGUE

Although there is no established method for evaluating the noise canceller, an example is shown in Fig. 40. Actual test on an automobile is also considered to be important.

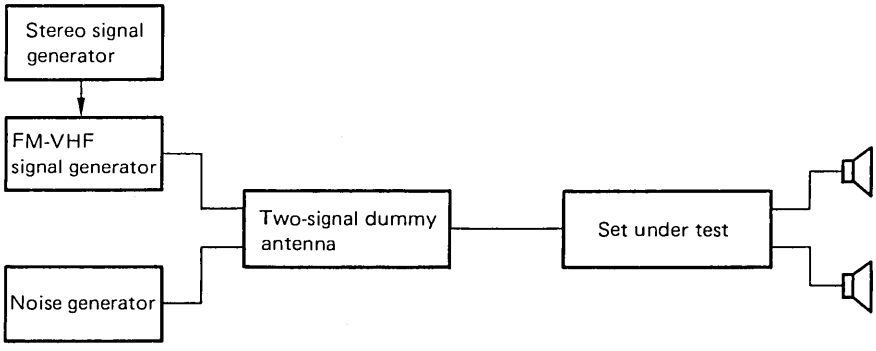


Fig. 40 Block Diagram for Evaluating System

EXPLANATION AND TYPICAL APPLICATIONS OF THE μPC1235C, AN FM MPX IC FOR HIGH CLASS STEREO TUNER

1. EXPLANATION OF THE μPC1235C

1–1. Outline

The μPC1235C is a semiconductor integrated circuit for FM multiplex demodulator developed for high class stereo FM tuners. As the IC adopts a PLL (phase locked loop) system, complexity of control usually experienced when using conventional external coil is eliminated and the demodulator can easily be constructed by simply controlling the external semi-fixed potentiometer.

Internal circuits are composed of a stereo demodulator, a lamp driver, an input stage pre-amplifier that is capable of establishing variable input signal levels, a VCO (voltage controlled oscillator) constituting PLL, a phase comparator, an LPF (low pass filter), a frequency divider, and a DC amplifier.

A stereo-monaural automatic switching circuit, a circuit for manual switching, VCO forced stop circuit etc. are built-in.

1–2. Features and Use

Features

(1) PLL system can reduce the number of external components and controlling procedures.
(2) Stereo-monaural switching can be made either automatically or manually from outside. The shock noise at switching is reduced considerably.
(3) Stereo-monaural switching operation is perfectly synchronized with a stereo indicator lamp.
(4) Total harmonic distortion is largely improved by the adoption of new circuits. Low distortion can give a wide input level.
(5) Fine adjustment of channel separation can be made with an external semi-fixed potentiometer. Channel separation characteristic from low to high pass is improved notably.
(6) Hight signal-to-noise ratio.

Use

FM multiplex demodulator of high class stereo.

2. CHARACTERISTICS OF THE μPC1235C

2–1. Maximum Ratings of the μPC1235C

Table 1 Absolute Maximum Ratings (T_a = 25 °C)

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	15	V
Lamp Current	I_L	75	mA
Package Dissipation	P_D	400*	mW
Operating Temperature	T_{opt}	−20 to +70	°C
Storage Temperature	T_{stg}	−40 to +125	°C

*Ta = 70 °C

2–2. Recommended Operating Condition of the μPC1235C

Table 2 Recommended Operating Condition

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	9	12	15	V

2–3. Electrical Characteristics of the μPC1235C

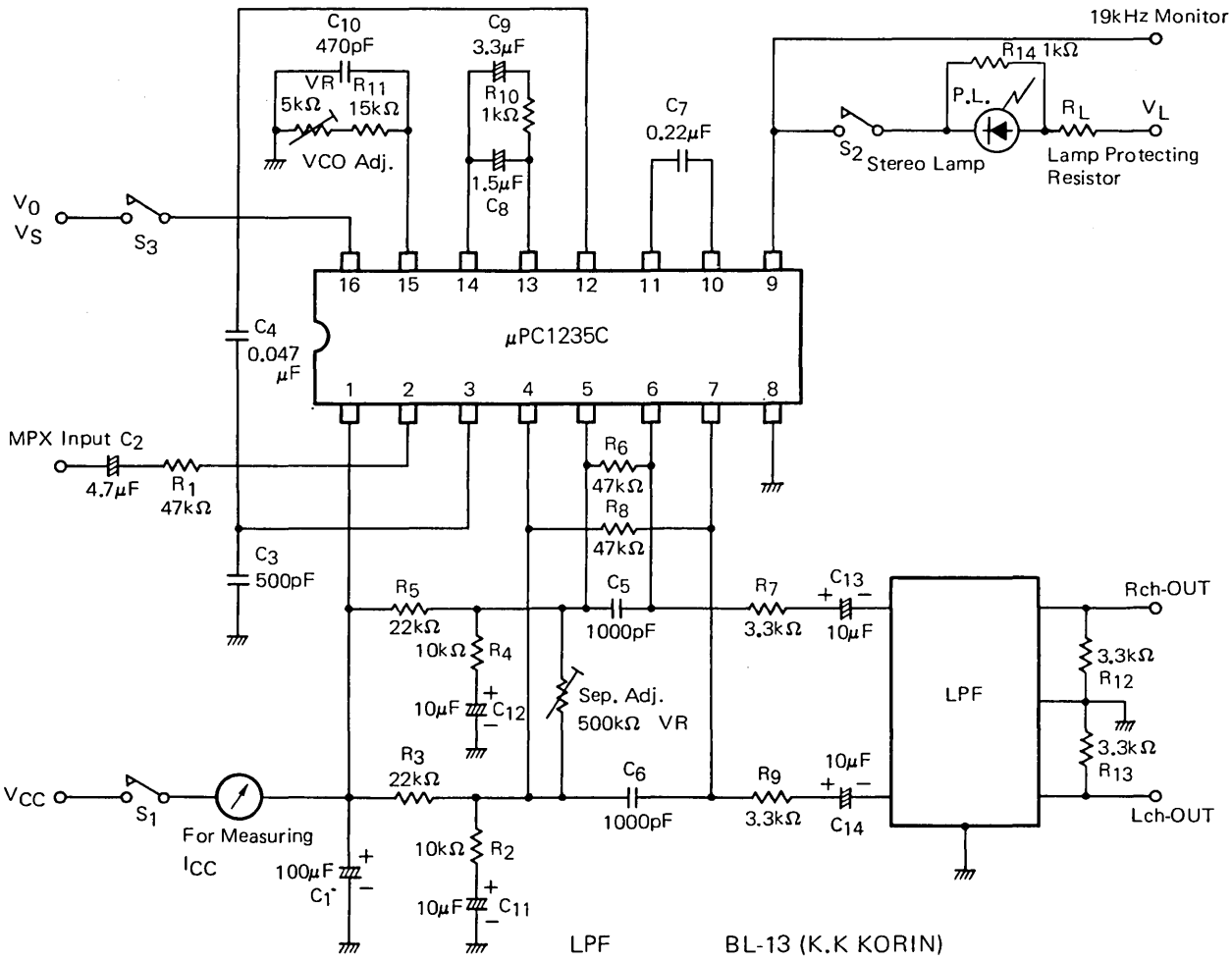
Table 3 Electrical Characteristics (Ta = 25 °C)

[V_{CC} = 12 V, f = 1 kHz, R_1 = 47 kΩ, R + L = 270 mV, Pilot = 30 mV]

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION	
Supply Current	I_{CC}	12	20	30	mA	No.Signal	
Channel Separation	Sep.	40	50		dB	Pilot = 30 mV	f = 100 Hz
		45	55		dB		f = 1 kHz
		35	45		dB		f = 10 kHz
Voltage Gain	A_V	8	12	16	dB	Monaural, *V_{in} = 300 mV	
Channel Balance	C.B.	−1.5	0	1.5	dB	Monaural, V_{in} = 300 mV	
		−1.5	0	1.5	dB	Stereo, Pilot = 30 mV	
Monaural Total Harmonic Distortion	T.H.D.		0.01	0.08	%	V_{in} = 300 mV	
Stereo Total Harmonic Distortion	T.H.D.		0.02		%	R + L = 270 mV Pilot = 30 mV	f = 100 Hz
			0.02	0.1	%		f = 1 kHz
			0.12		%		f = 10 kHz
Pilot Level for Lamp On	L-ON	6	12	20	mVr.m.s.	Pilot Level, R_1 = 47 kΩ	
Stereo Lamp Hysteresis	Hy.		6		dB	Pilot Level	
Capture Range	C.R.	±1.5	±3		%	Pilot = 30 mV	
Ultrasonic Frequency Rejection	19 kHz. Rej.		35		dB	Pilot = 30 mV	
	38 kHz. Rej.		45		dB	Pilot = 30 mV	
SCA Rejection	SCA Rej.		70		dB	Pilot = 30 mV, SCA = 30 mV	
Maximum Input Level	V_{in}		0.9		Vr.m.s.	Monaural, T.H.D. = 1 %	
Signal to Noise Ratio	S/N	81	89		dB	V_{in} = 300 mV, After LPF	
Stereo-Monaural Switching SW-ON Voltage	V_S		1.4	1.6	V	No. 16 Terminal Voltage Where Stereo Lamp-OFF	
VCO Stop Voltage	V_O	7		V_{CC}	V	No. 16 Terminal Voltage Where VCO Stops	

*A_V is from the output level measured at IC output terminal. A_V can be set by R_1, and the input impedance.

2–4. Test Circuit of the μPC1235C



LPF	BL-13 (K.K KORIN)
VCO Adj.	VCO tuning semi-fixed potentiometer
Sep Adj.	Separation adjusting semi-fixed potentiometer
S_1	V_{CC} ON-OFF SW
S_2	SW for 19 kHz monitor
S_3	VCO stop SW

Fig. 1 Test Circuit for Electrical Characteristics (Top View)

NOTES:

1. Use polystyrene capacitors for that connected to No. 15 terminal to compensate the temperature coef. of VCO.
2. For adjusting the VCO oscillation frequency, make S_2 open, connect the frequency counter to No. 9 terminal 19 kHz monitor and then set by varying the semi-fixed potentiometer VCO Adj. connected to No. 15 terminal.
3. For separation adjustment, vary the semi-fixed potentiometer Sep. Adj. connected between terminals No. 4 and No. 5 to set at the best point.

2–5. Package Dimensions of the μPC1235C

NOTE: Numerical values show TYP. values unless otherwise designated.

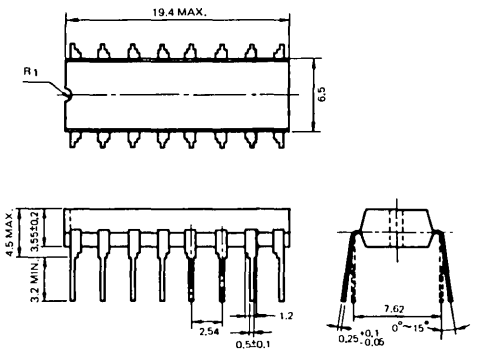


Fig. 2 Package Dimensions of the μPC1235C (Unit: mm)

3. FUNCTIONAL BLOCK DIAGRAM OF THE μPC1235C

3–1. Functional Block Diagram of the μPC1235C

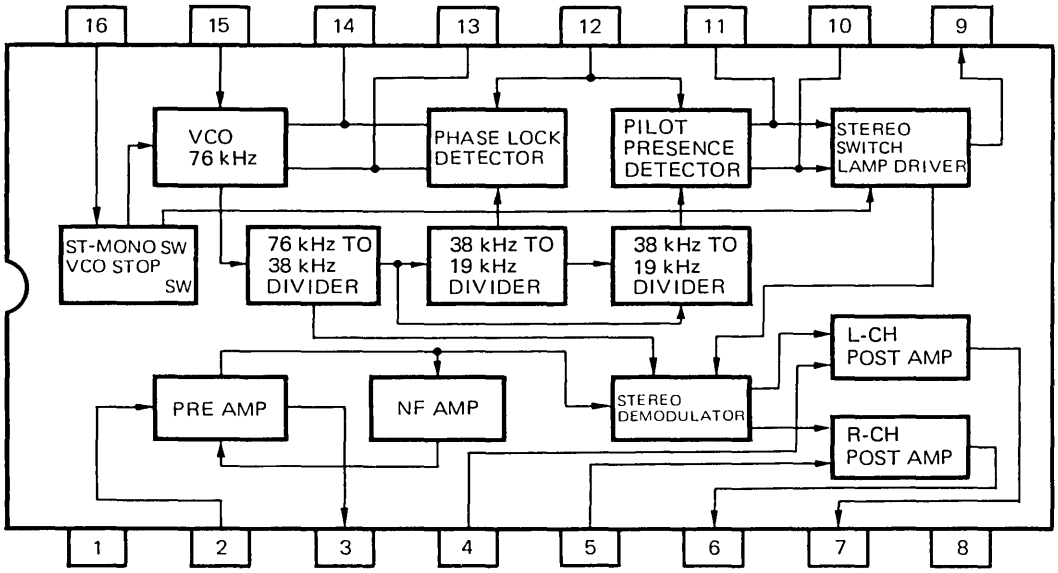


Fig. 3 Functional Block Diagram of the μPC1235C

3–2. Terminal Connection

Table 4 Terminal Connection

No.	Connection	No.	Connection
1	V_{CC}	9	ST. LAMP & 19kHz MONITOR
2	PRE AMP INPUT	10	SWITCH FILTER
3	PRE AMP OUTPUT	11	SWITCH FILTER
4	POST AMP BIAS	12	DETECTOR INPUT
5	POST AMP BIAS	13	LOOP FILTER
6	R-CH OUTPUT	14	LOOP FILTER
7	L-CH OUTPUT	15	OSC RC. NETWORK
8	GND	16	ST.-MONO SW & VCO STOP

3–3. Typical Voltage of Each Terminal

Table 5 Typical Voltage of Each Terminal (V_{CC} = 12 V, Test circuit)

	1	2	3	4	5	6	7	8
μPC1235C	12 V	2.3 V	5.5 V	9.9 V	9.9 V	5.2 V	5.2 V	0

	9	10	11	12	13	14	15	16
μPC1235C	–	2.3 V	2.3 V	2.3 V	2.3 V	2.3 V	3.3 V	0

3–4. Equivalent Circuit of the μPC1235C

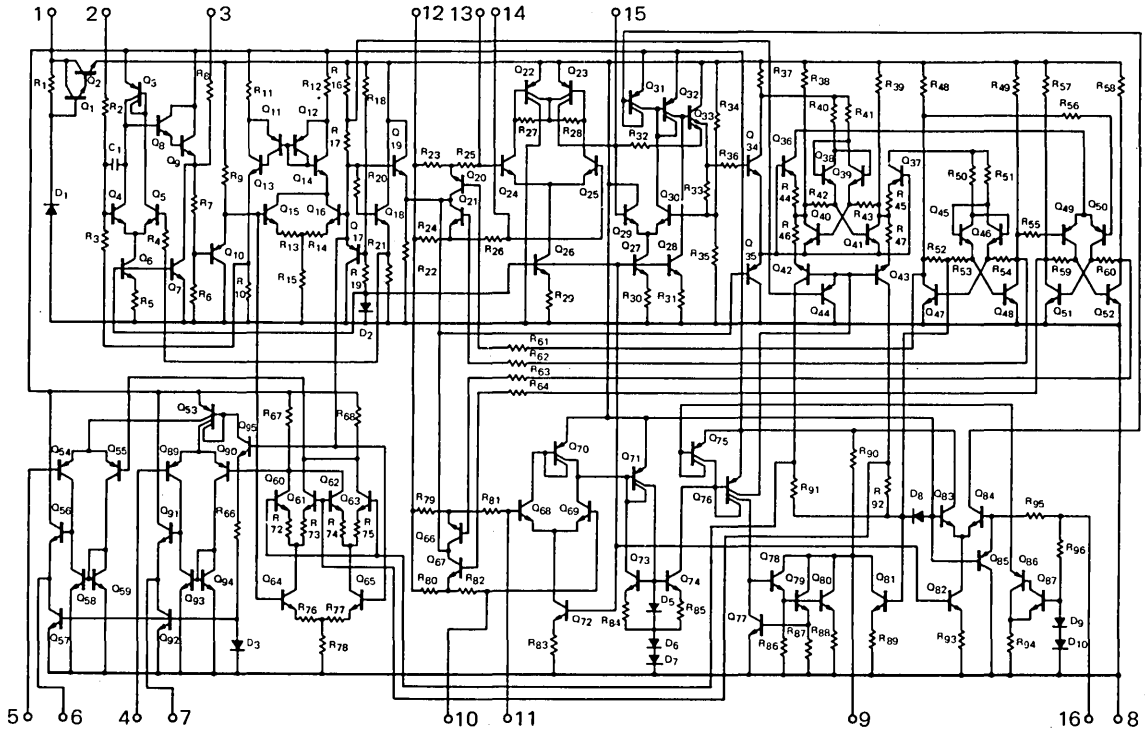


Fig. 4 Equivalent Circuit of the μPC1235C

3–5. Explanation of the Equivalent Circuit

(1) Input amplifier and bias supply circuit.
Bias supply circuit and equivalent circuit of the input amplifier are shown in Fig. 5. Regulated voltage Vs is expressed by

$$V_{D1}-V_{BE}(Q_1)-V_{BE}(Q_2)$$

and constitutes a constant voltage circuit with a diode D_1, transistors Q_1, Q_2 and a resistor R_1. Therefore, Vs is constant to variation of the power supply voltage. The input amplifier is made up of a preamplifier consisting of transistors Q_3 to Q_9, resistors R_2 to R_8 and a capacitor C_1 and an NF amplifier consisting of transistors Q_{11} to Q_{16} and resistors R_{11} to R_{15}.

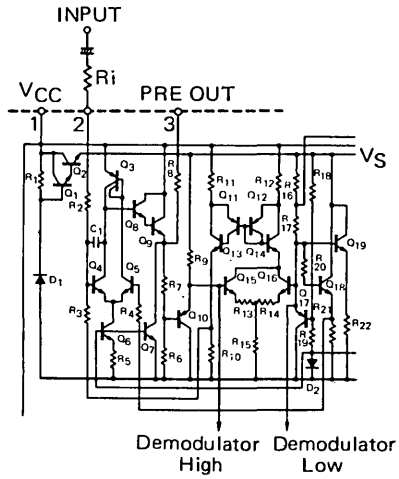


Fig. 5 Bias Supply Circuit and Input Amplifier

Q_4 and Q_5 are differential amplifiers and perform low current operation making the multicollector transistor Q_3, a current mirror circuit, active load and obtain a high circuit gain.
The output of the pre-amplifier is supplied to the base of Q_{15}, i.e. the input of NF amplifier, through Darlington-connected Q_8, Q_9 and feedback from the emitter of Q_{13} by R_3.
Improvement of distortion is effected by the NF amplifier and betterment of channel separation is devised by eliminating crosstalk component through the feedback resistor inserted in the emitters of Q_{15}, Q_{16}.
Gain of the input amplifier is determined by a feedback resistor R_3 and an input resistor Ri out fitted to No. 3 terminal and expressed by following equation:

$$A_1 \fallingdotseq \frac{R_3}{Ri}$$

C_1 is a capacitor inserted to stop oscillation and R_{11}, R_{12} are resistor inserted for offset voltage compensation. Of the composite signal input from No. 2 terminal only the pilot signal is passed through LPF out fitted to No. 3 terminal and lead to the phase detector of PLL circuit. Further, the main signal and subsignal of the composite signal are lead to the demodulator through the emitter-follower of transistor Q_{10}.

(2) Demodulator

Fig. 6 shows configuration of the double balance type demodulator. Transistors Q_{60} to Q_{63} are those which perform switching by 38 kHz which is a subcarrier injected from the frequency divider. The composite signal is input from the bases of Q_{64}, Q_{65} and divided into L, R-Ch signals. The resistors R_{76}, R_{77}, R_{78} inserted in the emitters of Q_{64}, Q_{65} are, similar to NF amplifier, inserted as feedback resistor to eliminate crosstalk component. The switching signal, i.e. a subcarrier of 38 kHz, is 38 kHz that is 50 % of duty cycle obtained by injecting the oscillation frequency, 76 kHz, of VCO into one stage bistable multivibrator (flip flop).

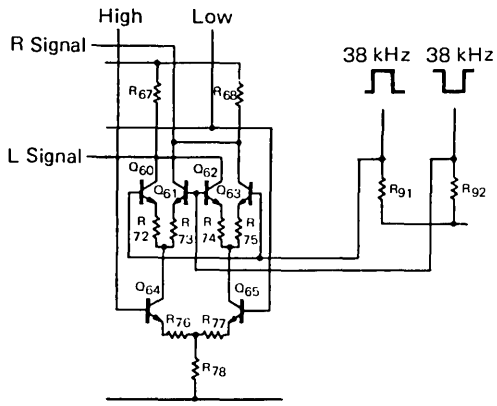


Fig. 6 Demodulator

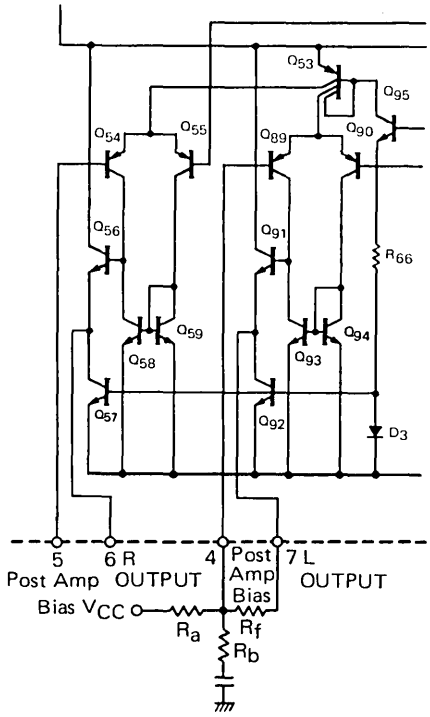


Fig. 7 Output Stage Post Amplifier

(3) Output stage post amplifier

The structure of the output stage post amplifier is shown in Fig. 7.
The L, R signals separated by the demodulator are injected respectively into the bases of Q_{55}, Q_{90} of the differential amplifier composed of transistors Q_{54}, Q_{55} and Q_{89}, Q_{90}.
Further, bias is given to the base voltage of Q_{54}, Q_{89} to the same voltage (when no signal) as the base voltage of Q_{55}, Q_{90} by external components through No. 5, No. 4 terminals. The transistor Q_{53} is a

transistor of multicollector and constant current circuit of the differential amplifier, and the transistors Q_{58}, Q_{59} and Q_{93}, Q_{94} are active load.
The L, R signals amplified by the differential amplifier are output from No. 6 (R signal), No. 7 (L signal) terminal respectively through the emitter-follower of transistors Q_{56}, Q_{91} and feedback to No. 5, No. 4 terminals by external resistors R_6, R_8.
Accordingly, gain of the output stage post amplifier can be expressed equivalently from external resistor ratio by following equation:

$$A_2 \fallingdotseq \frac{R_a // R_b + R_f}{R_a // R_b}$$

(4) Phase detector and DC amplifier

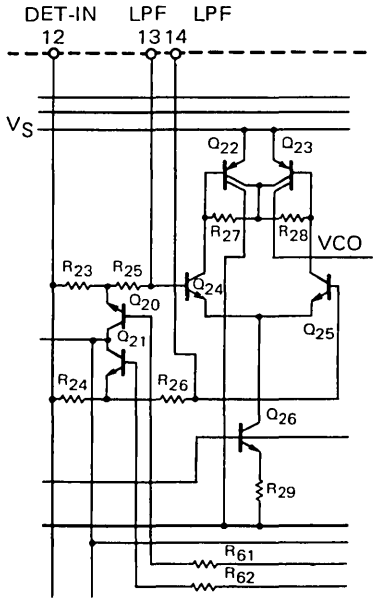


Fig. 8 Phase Detector and DC Amplifier

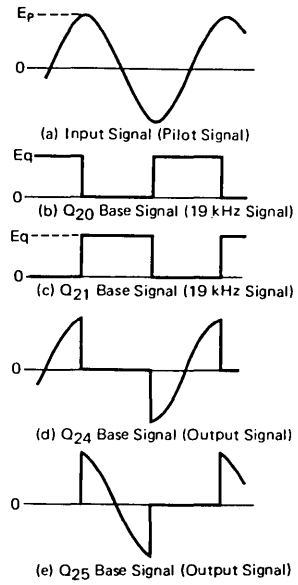


Fig. 9 Phase Detector Input Output Waveform

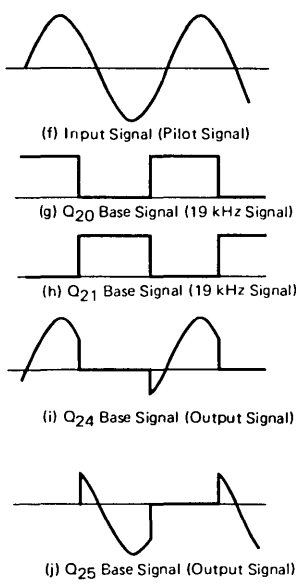


Fig. 10 Phase Detector Input Output Waveform

Fig. 8 shows structure of the phase detector and DC amplifier. The phase detector is composed of transistors Q_{20}, Q_{21}. The 19 kHz pilot signal amplified by the input amplifier is input from No. 3 terminal to No. 12 terminal through LPF being an input signal of the phase detector. The input signal (19 kHz pilot signal) is compared with the phase of 19 kHz that is the oscillation frequency of VCO, 76 kHz, divided into 1/4, and an output voltage corresponding to the phase difference is generated. When the phase difference between the two signals is 90°, the output voltage becomes zero in DC (Fig. 9).
Fig. 10 shows the waveform when 19 kHz signal advances. That is, (i) becomes high level in DC and (j) becomes low level and becomes input of the differential amplifier that constitutes the DC amplifier. However, the output waveform is a waveform when LPF out fitted to No. 13, No. 14 terminals are removed. When LPF is passed through, the above can be expressed by following equations:

$$\text{19 kHz pilot signal} \quad e_p(t) = E_p \cos \frac{\omega_S}{2} t$$

$$\text{19 kHz signal} \quad e_q(t) = \frac{4}{\pi} E_q \left\{ \cos \left(\frac{\omega_S}{2} t + \phi \right) - \frac{1}{3} \cos 3 \left(\frac{\omega_S}{2} t + \phi \right) + \frac{1}{5} \cos 5 \left(\frac{\omega_S}{2} t + \phi \right) \ldots \right\}$$

Here, if the output voltage of the phase detector is assumed to be $e_0(t)$, all but fundamental wave are attenuated by LPF, hence the following equation:

$$e_o(t) = e_p(t) \cdot e_q(t)$$
$$= \frac{2}{\pi} E_p E_q \cos\phi$$

Accordingly, an output voltage proportional to cosine of the phase difference of the two signals is generated and when the phase difference is 90°, above equation becomes zero and the oscillation frequency of the VCO is taken to have locked to the input signal.

(5) VCO

VCO (Voltage Controlled Oscillator) is shown in Fig. 11.

VCO determines high level and low level dividing the reference voltage V_S by resistor, actuates the comparator (astable multivibrator) making the level the reference voltage and produces blocking oscillation by charging and discharging the capacitor out fitted to No. 15 terminal.

Now, if transistor Q_{30} is in ON-state, transistors Q_{32}, Q_{33} will come to ON state, and the reference voltage of the comparator which is the base voltage of Q_{30} becomes a high level.

This relation is expressed by following equation:

$$V_H = (V_S - V_{CE(sat)}(Q_{33})) \times \frac{R_{35}}{R_{33} + R_{35}}$$

Then, current flows from another emitter of Q_{33} and the current charges the external capacitor C to high level through the resistor R_{32}.

When charging is completed, transistor Q_{29} becomes ON state and discharged by external resistor R.

Then, since Q_{30} is in OFF state, Q_{32}, Q_{33} become OFF state and the reference voltage of the comparator becomes low level voltage given by the following equation:

$$V_L = V_S \frac{R_{35}}{R_{34} + R_{35}}$$

The state is manifested in waveform in Fig. 12.

In the figure, t_1, t_2 represent time required for charging and discharging respectively and given by following equations:

$$t_1 = R_{32} \cdot C \cdot \ln \frac{V_S - V_L}{V_S - V_H}$$

$$t_2 = R \cdot C \cdot \ln \frac{V_H}{V_L}$$

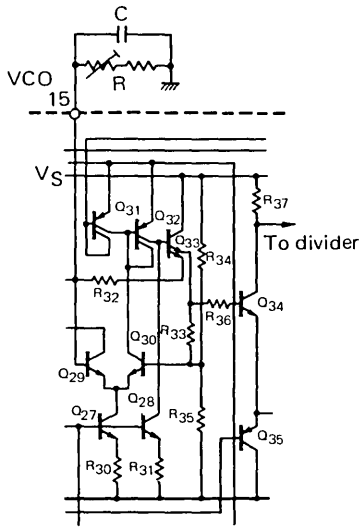


Fig. 11 VCO

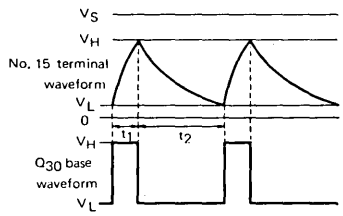


Fig. 12 VCO Waveform

(6) Divider

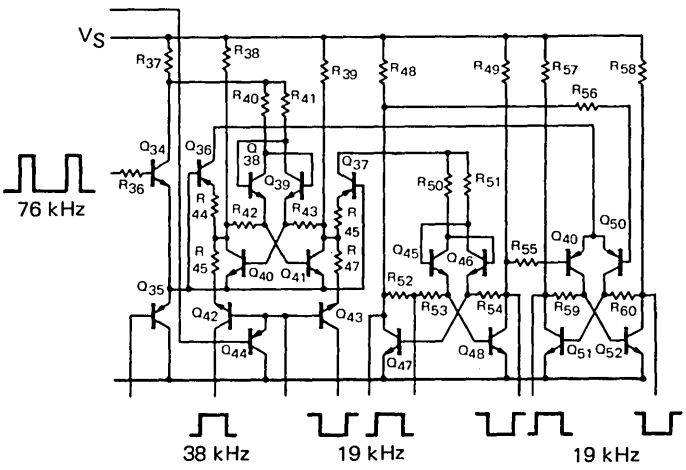


Fig. 13 Divider

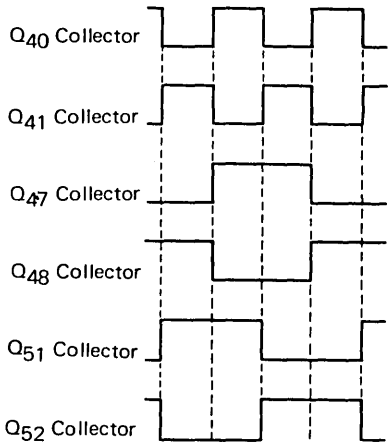


Fig. 14 Divider Output Waveform

Fig. 13 shows the frequency divider.
These are bistable multivibrator (flip flop), and composed of a frequency divider that produces from 76 kHz, oscillation frequency of VCO, switching signal 38 kHz of duty cycle 50 % required for stereo demodulation, and a frequency divider that produces 19 kHz injected into the phase detector from 38 kHz to control the VCO, and a frequency divider that produces 19 kHz required for driving the stereo indicator lamp synchronized with the pilot signal as well as for controlling the stereo switch.
Fig. 14 gives phase relation of the above.
The collector waveform of transistor Q_{48} and that of transistor Q_{52} appear at a 90° phase shift. Therefore, the collector waveforms of Q_{51}, Q_{52} are synchronized with the pilot signal.

(7) Lamp driver and stereo switch

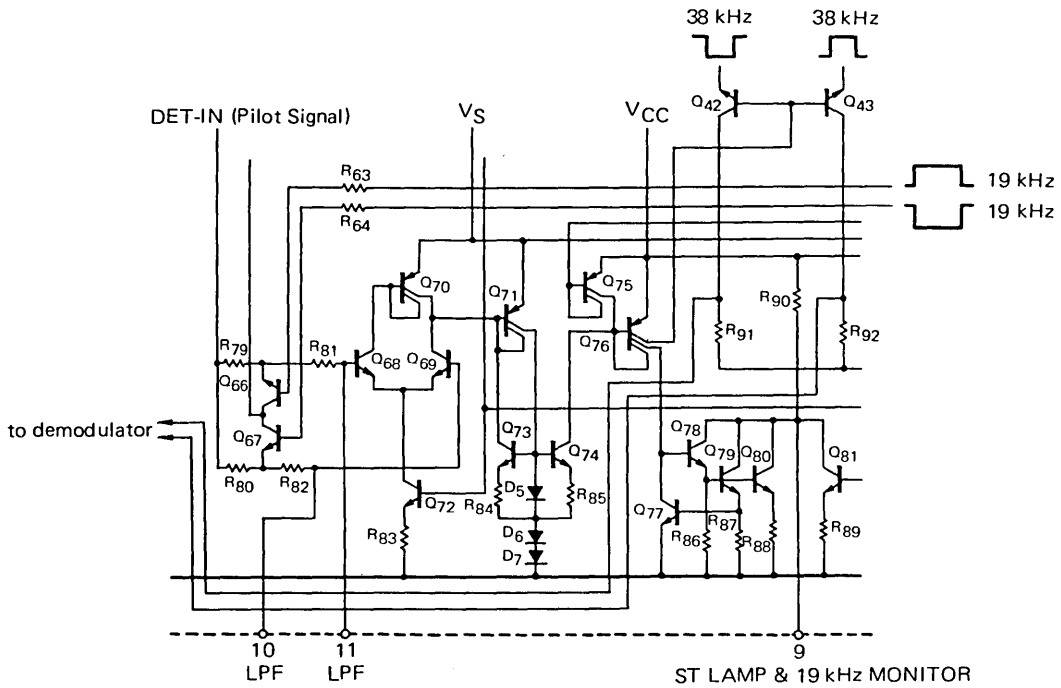


Fig. 15 Lamp Driver and Stereo Switch Circuit

The lamp driver is shown in Fig. 15.

The phase detector composed of transistors Q_{66}, Q_{67} and resistors R_{63}, R_{64}, R_{79}, R_{80}, R_{81}, R_{82} performs phase detection by the input signal (pilot signal) and 19 kHz divider output signal synchronized with the above. The state is expressed in equations as below:

Pilot signal
$$e_p(t) = E_p \cos\frac{\omega S}{2} t$$

19 kHz divider output signal
$$e_r(t) = \frac{4}{\pi} E_r \left(\cos\frac{\omega S}{2} t - \frac{1}{3}\cos 3\frac{\omega S}{2} t + \frac{1}{5}\cos 5\frac{\omega S}{2} t \ldots\right)$$

Here, if the output voltage of the phase detector is assumed as $e_{0(t)}$, since all but the standard wave are removed by LPF out fitted to No. 10, No. 11 terminals, equation becomes as below:

$$e_0(t) = \frac{2}{\pi} E_p E_r$$

Accordingly, output proportional to the pilot signal is obtained for $e_0(t)$ after LPF.

When the pilot signal is input to the phase detector, difference in voltage level is brought about at No. 10, No. 11 terminals, and the collector current $I_C(Q_{69})$ of Q_{69}, flows more than the collector current $I_C(Q_{68})$ of Q_{68}.

Consequently, the current difference $\Delta I_C = I_C(Q_{69}) - I_C(Q_{68})$ becomes unable to be let flow by the multi-collector transistor i.e. active load, thus reducing the base current of Q_{71} by ΔI_C.

When Q_{71} is turned ON, the collector current flows to the diode D_5, and Q_{74} is biased, and, consequently, Q_{76} is turned ON. Since Q_{76} is a multicollector, flow is effected on the one hand to the divider to turn Q_{42}, Q_{43} of the divider ON, and the switching signal of 38 kHz is supplied to the demodulator. Thus, stereo demodulation is effectuated.

On the other hand, the current flows to the lamp driver made up of transistors Q_{78} to Q_{80} and light the lamp. When the pilot signal is not input, the input level of No. 10, No. 11 terminals become zero and the collector current of Q_{64}, Q_{65} constituting the differential is supplied only from Q_{70}. Thus, Q_{71} becomes OFF, and as no current flows to D_5, Q_{76} also becomes OFF. Consequently, Q_{42}, Q_{43} become OFF and the switching signal of 38 kHz is not supplied to the demodulator and monaural function is effected. At the same time, the lamp driver becomes OFF so that the lamp is not lit.

(8) VCO stop, ST.-MONO switching circuit

Fig. 16 shows VCO stop and ST.-MONO switching circuit.

When voltage is supplied to No. 16 terminal, the constant-voltage circuit constituting with transistors Q_{86}, Q_{87}, diodes D_9, D_{10} and resistors R_{94}, R_{96} operates to give bias voltage to the transistor Q_{84} and turns Q_{31} of VCO ON and Q_{32}, Q_{33} OFF. Consequently, charge and discharge by the external capacitor at No.15 terminal are not effected and VCO stops.

At the same time, as bias is provided to Q_{83} and Q_{75} of the lamp driver is turned ON, Q_{76} becomes OFF and the switching signal of 38 kHz is not supplied to the demodulator. Thus charge is made to monaural function and lighting is not effected.

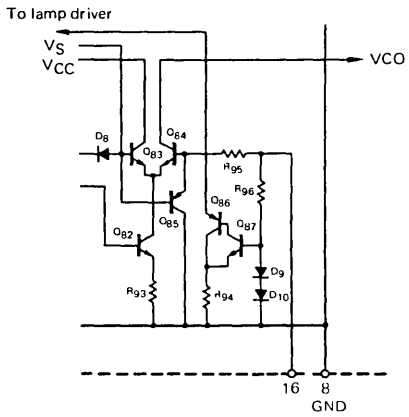


Fig. 16 VCO Stop, ST.-MONO Switching Circuit

4. APPLICATION EXAMPLES OF THE μPC1235C

4–1. Stereo-Monaural Manual Switching Circuit

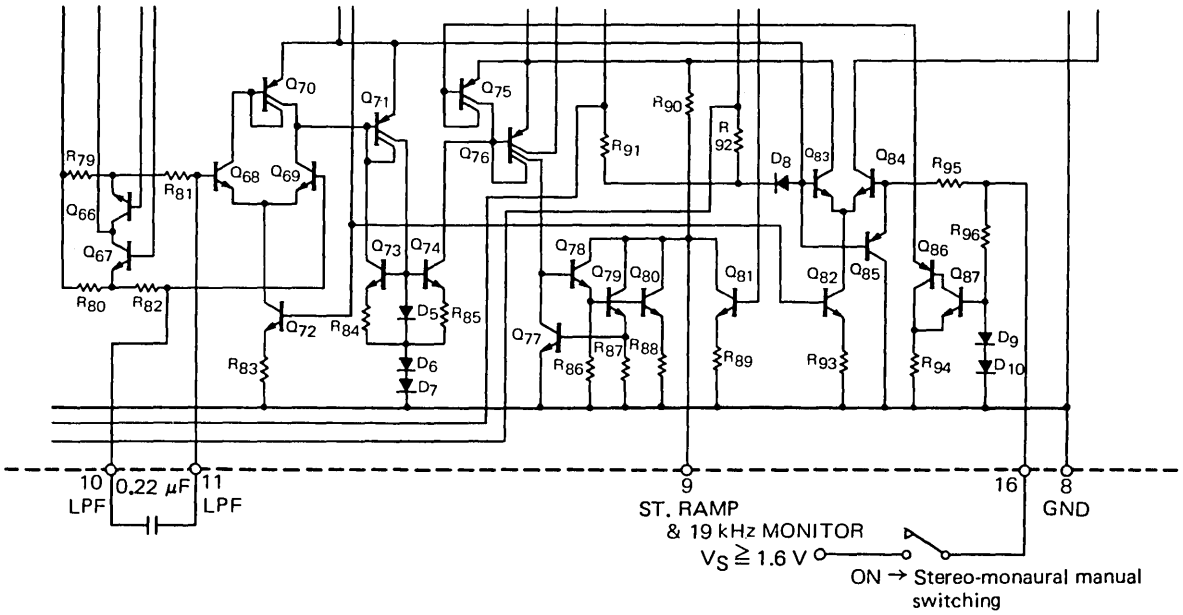


Fig. 17 Stereo-Monaural Manual Switching Circuit

The μPC1235C, by virtue of synchronization with 19 kHz pilot signal normally input with 19 kHz generated within IC, injects the subcarrier of 38 kHz into the demodulator by driving the lamp driver as well as turning ON of the gate circuit. In consequence, stereo multiplex demodulator function is made possible. However, the necessity of monaural function at a set point irrelevant to condition of input circuit is considered. Fig. 17 shows the operation circuit for such case.

As mentioned in previous section, when the constant- voltage circuit is operated by applying voltage to No. 16 terminal, transistor Q_{75} is turned ON and the gate circuit is turned OFF. Therefore, the subcarrier of 38 kHz is not injected to the demodulator and monaural function can be effected forcibly.

The voltage level then applied to No. 16 terminal is $V_{16} \geqq 1.6$ V.

Therefore, stereo-monaural switching becomes possible by virtue of muting voltage from IF stage etc.

4–2. On Beat Interference When Receiving AM.

As the μPC1235C adopts PLL (Phase Locked Loop) system, it has an internal oscillator. While AM receiving, the internal oscillation voltage can give interference so that VCO becomes necessary to be stopped.

As stated in foregoing section, when transistor Q_{31} is turned ON and, in consequence, transistors Q_{32}, Q_{33} are turned OFF, charge and discharge at external capacitor are not effected and the oscillation of VCO stops.

Accordingly, if voltage is applied to No. 16 terminal, transistor Q_{84} becomes ON and Q_{31} becomes OFF. Thus, by simply applying voltage to No. 16 terminal, oscillation of VCO can be stopped and at the same time, forced monaural function becomes possible. Further, as the voltage level at the time of stereo-monaural manual switching is $5 \geqq V_{16} \geqq 1.6$ V, and that when VCO stop is $V_{CC} \geqq V_{16} \geqq 7$ V, individual function is possible according to the level of voltage applied.

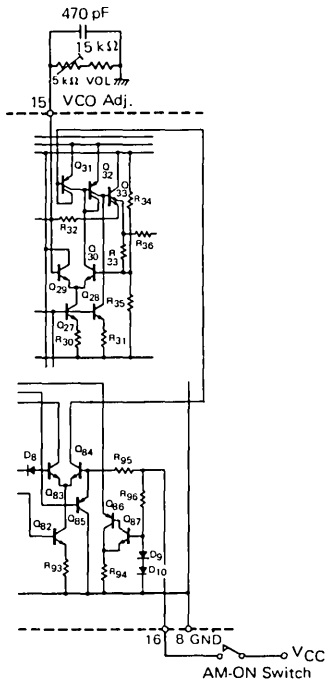


Fig. 18 VCO Stop Circuit

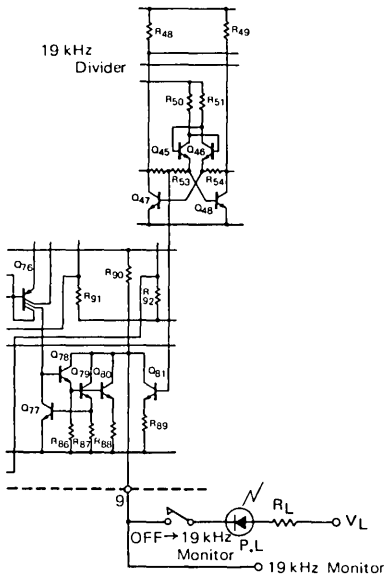


Fig. 19 VCO Monitor Circuit

4–3. On VCO Monitor

VCO monitor circuit is shown in Fig. 19.

This is to monitor from No. 9 terminal dividing the oscillation frequency 76 kHz of VCO into 1/4 (19 kHz) by the divider.

At this time, monitoring can be performed by making input signal to monaural signal and directly connecting the frequency counter to No. 9 terminal by cutting off the stereo indicator lamp. VCO oscillation frequency is adjusted by means of a semi-fixed potentiometer connected to No. 15 terminal.

4–4. On Stereo Lamp Lighting Level

The stereo lamp lighting level can be adjusted, as is clear from the circuit shown in Fig. 15, by changing the input ON level of the differential amplifier circuit made up of transistors Q_{68}, Q_{69}, Q_{70}, Q_{72}.

Generally, when 19 kHz pilot signal increases, the base potential rises, and if it becomes above a certain potential, more collector current i_2 of Q_{69} flows than the current i_1 of Q_{68}. Further, in case the 19 kHz pilot signal is not input, as active load Q_{70} is set so that collector current of Q_{68} and Q_{69} becomes $i_1 > i_2$, if it becomes $i_2 \geqq i_1$, the collector current of Q_{69} cannot be supplied by Q_{70} only.

Accordingly, deficiency $i_2 - i_1$ of the collector current of Q_{69} is reduced from Q_{71} and light the lamp.

From the above, it will be understood that to charge the lamp lighting level can be performed by charging the offset voltage of above mentioned differential amplifier circuit.

Examples of change are shown in Fig. 20 and Fig. 21.

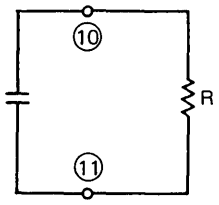


Fig. 20

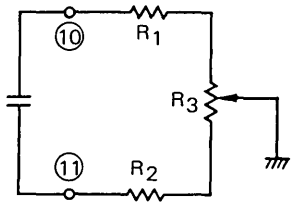


Fig. 21

4–5. Explanation of External Componentes

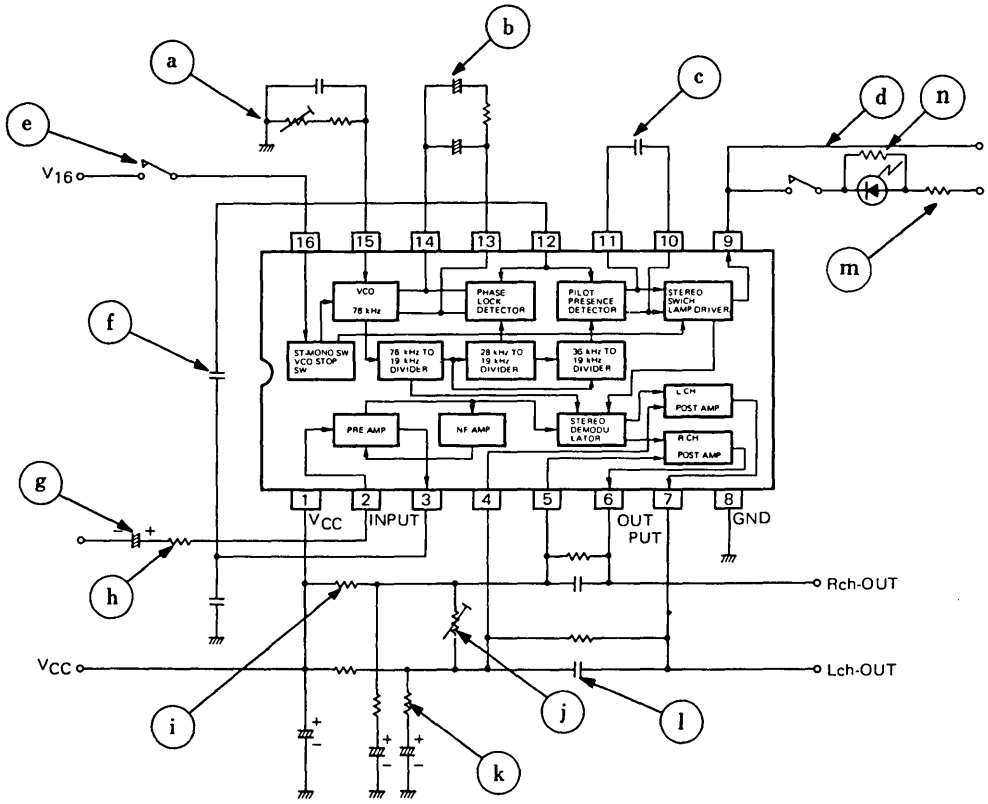


Fig. 22 Explanation of External Components

a. Semi-fixed potentiometer for determination of VCO oscillation frequency.

b. PLL loop LPF. Determines lock range together with PLL loop gain.

c. Lamp operation LPF. Determines low pass cutoff frequency by internal impedance and time constant. When the value of C is large, cutoff frequency becomes low.

d. 19 kHz VCO monitor terminal and stereo indicator lamp. To monitor 19 kHz switch is turned OFF and to light the lamp switch is turned ON.

e. Manual monaural switching switch and VCO stop. Then, monaural level $5\ V \geqq V_{16} \geqq 1.6\ V$, VCO stop level $V_{CC} \geqq V_{16} \geqq 7\ V$.

f. PLL input coupling capacitor. Divides audio frequency from pilot frequency.

g. Input coupling capacitor. Effects low pass Fre-characteristics and low pass Sep-characteristics.

h. Input resistor. Determines gain of the input amplifier.

i. Input registor of output stage post amplifier. Effects gain of amplifier.

j. Semi-fixed potentiometer for adjusting Sep.

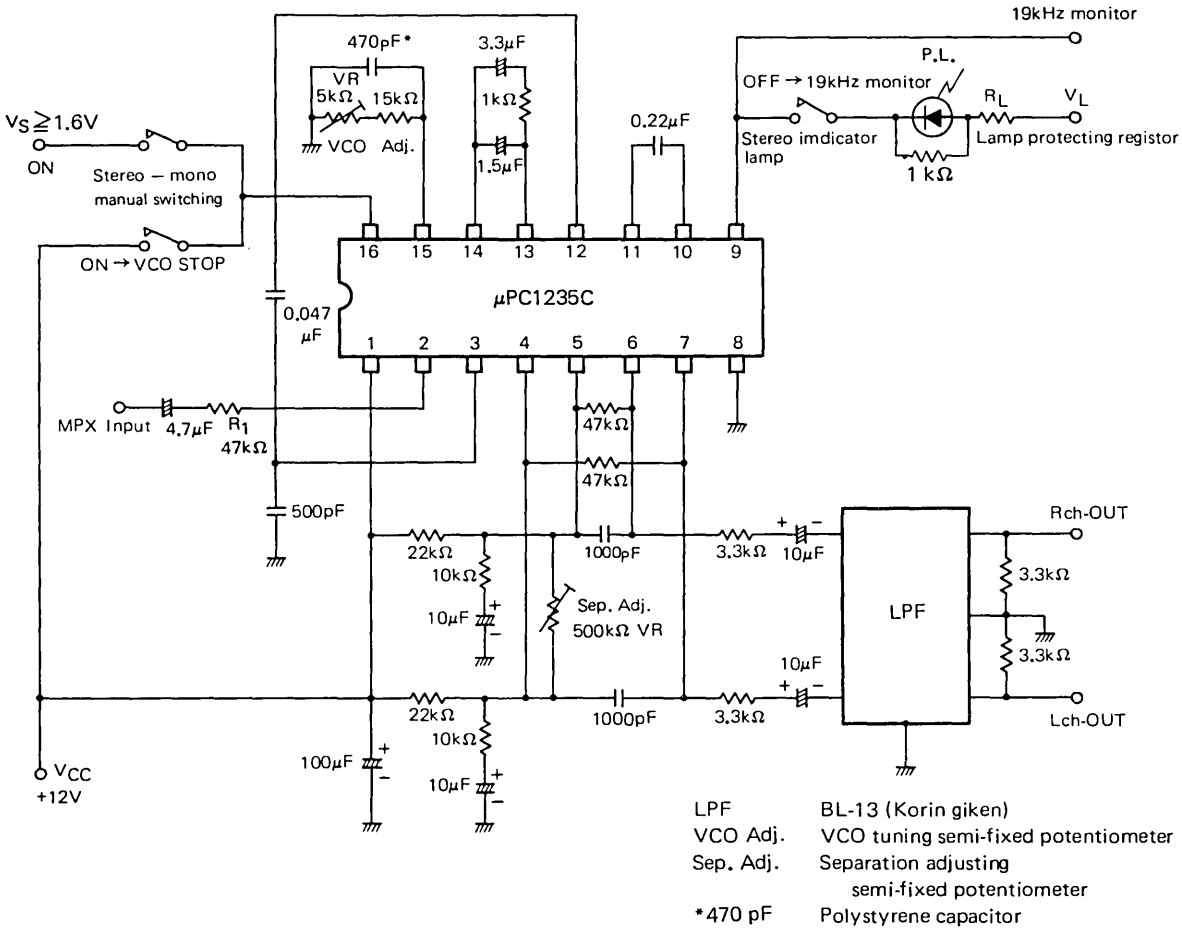
k. Resistor to determine gain of the output post amplifier.

l. Output capacitor and resistor. Determines output de-emphasis characteristics. Effects gain being feedback resistor of the output post amplifier.

m. Lamp protecting resistor.

n. Lamp by-pass resistor

4–6. Typical Application (Top View)



LPF	BL-13 (Korin giken)
VCO Adj.	VCO tuning semi-fixed potentiometer
Sep. Adj.	Separation adjusting semi-fixed potentiometer
*470 pF	Polystyrene capacitor

Fig. 23 Typical Application

NOTES:
When the unit is used with power supply voltage of less than 12 V, the mid-point electric potential of the output terminals 6, 7 in the above typical application may change and Total Harmonic Distortion at output terminal will increase.
In this case change the bias resistor 47 kΩ between terminals 5, 6 and terminals 4, 7 and keep at mid-point electric potential.

Example of printed-circuit board (unit: mm)

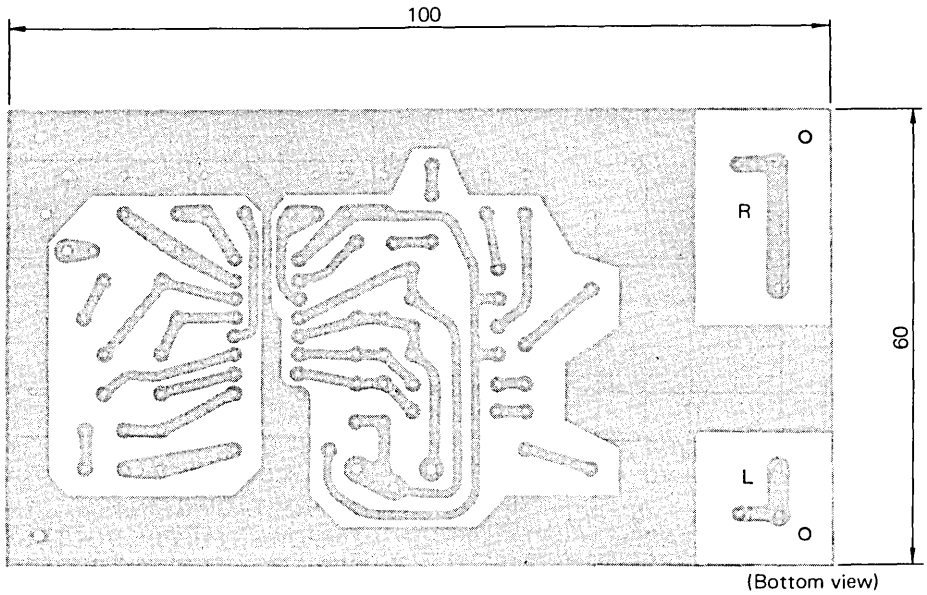
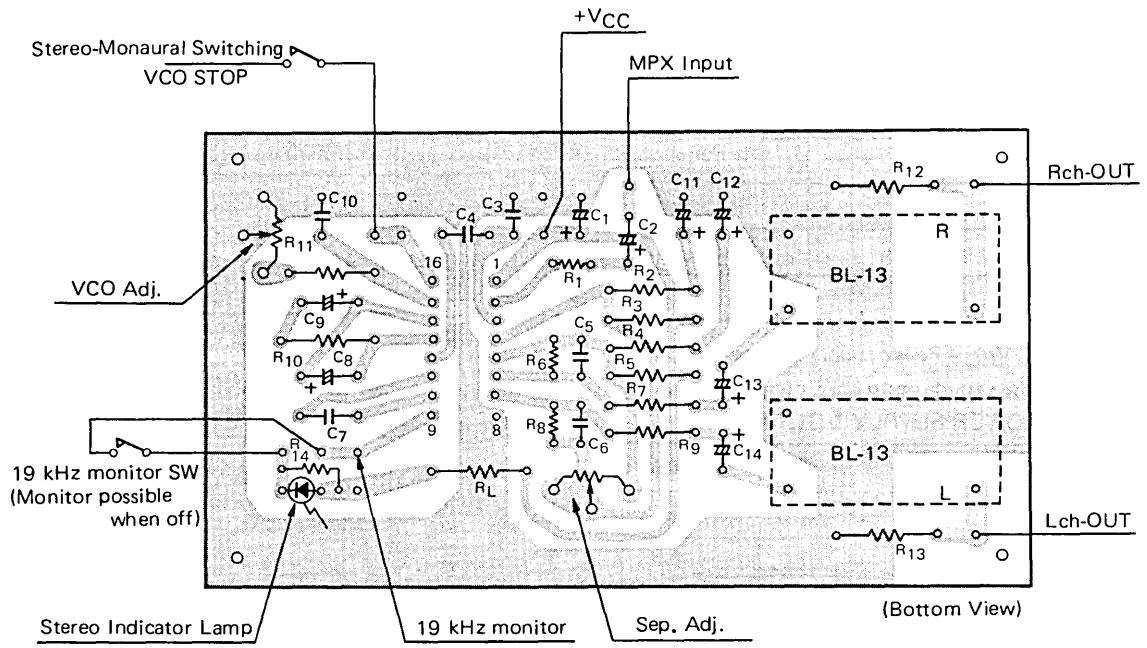


Fig. 24 Example of Printed-Circuit Board

Outboard components mounted on a printed-circuit board



R_1=47 kΩ	R_6 =47 kΩ	R_{11}=15 kΩ	C_1=100 μF	C_6=1 000 pF	C_{11}=10 μF	Sep. Adj.=500 kΩ VR
R_2=10 kΩ	R_7 =3.3 kΩ	R_{12}=3.3 kΩ	C_2=4.7 μF	C_7 =0.22 μF	C_{12}=10 μF	VCO Adj=5 kΩ VR
R_3=22 kΩ	R_8 =47 kΩ	R_{13}=3.3 kΩ	C_3=500 pF	C_8 =1.5 μF	C_{13}=10 μF	BL-13=19 kHz
R_4=10 kΩ	R_9 =3.3 kΩ	R_{14}=1.0 kΩ	C_4=0.047 μF	C_9 =3.3 μF	C_{14}=10 μF	LPF (Korin giken)
R_5=22 kΩ	R_{10}=1.0 kΩ	R_L =Lamp protecting resistor	C_5=1 000 pF	C_{10}=470 pF Polystyrene capacitor		

Fig. 25 Outboard Components Mounted on a Printed-Circuit Board

4–7. Typical Performance Characteristics

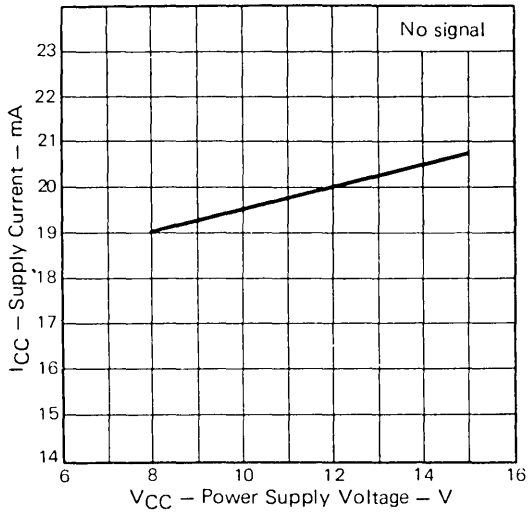


Fig. 26 SUPPLY CURRENT vs. POWER SUPPLY VOLTAGE

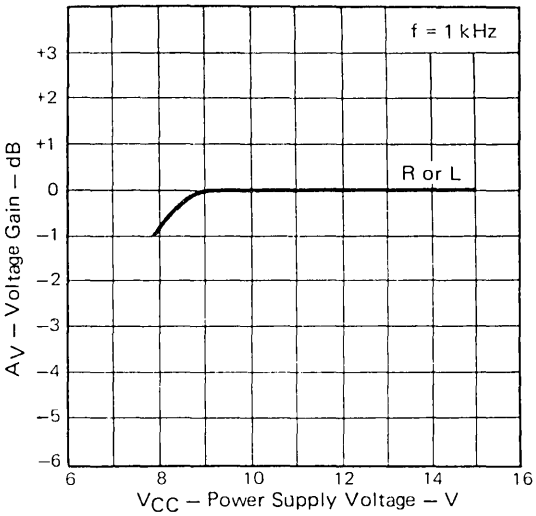


Fig. 27 VOLTAGE GAIN vs. POWER SUPPLY VOLTAGE (Monaural)

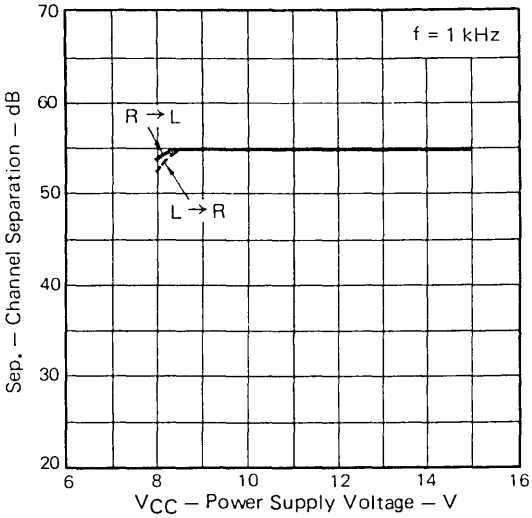


Fig. 28 CHANNEL SEPARATION vs. POWER SUPPLY VOLTAGE

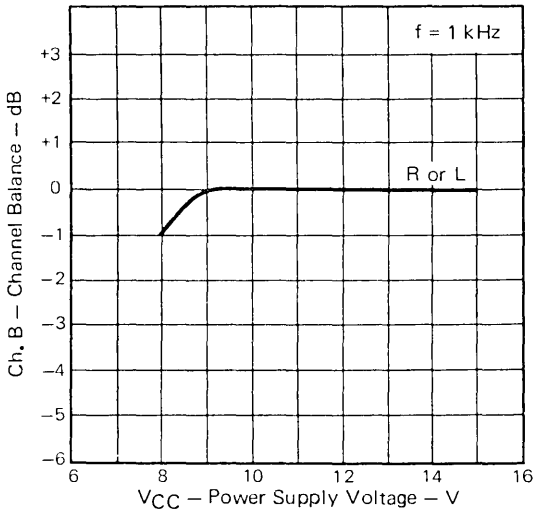


Fig. 29 CHANNEL BALANCE vs. POWER SUPPLY VOLTAGE (Monaural)

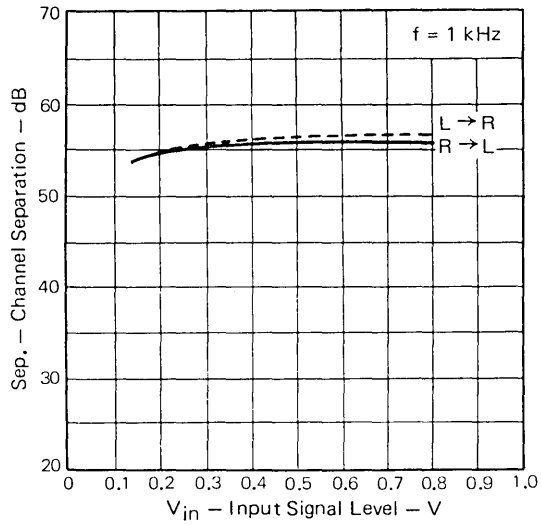


Fig. 30 CHANNEL SEPARATION vs. INPUT SIGNAL LEVEL

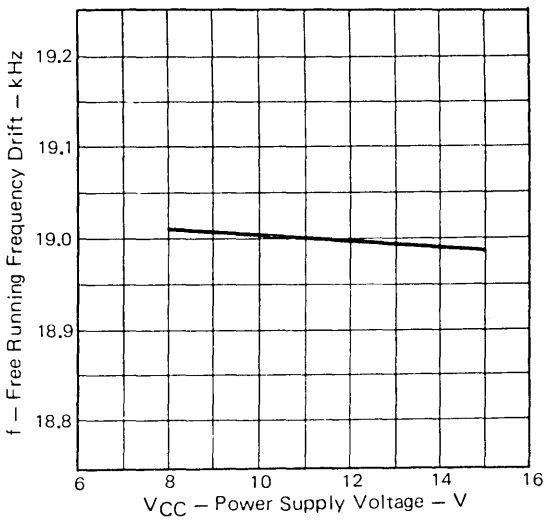


Fig. 31 FREE RUNNING FREQUENCY DRIFT vs. POWER SUPPLY VOLTAGE

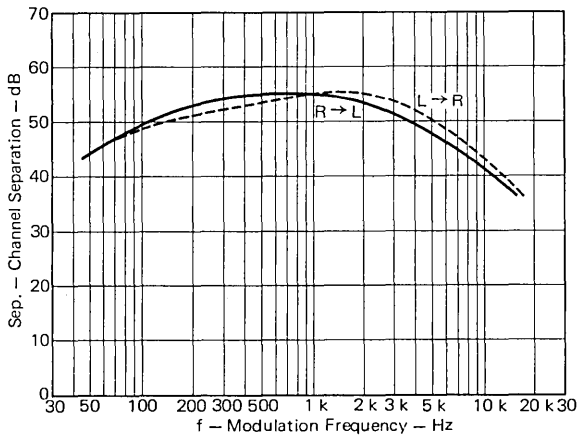


Fig. 32 CHANNEL SEPARATION vs. MODULATION FREQUENCY

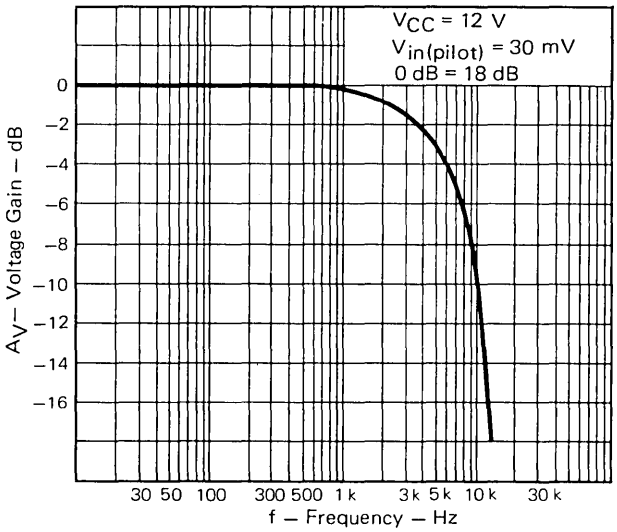


Fig. 33 VOLTAGE GAIN vs. FREQUENCY

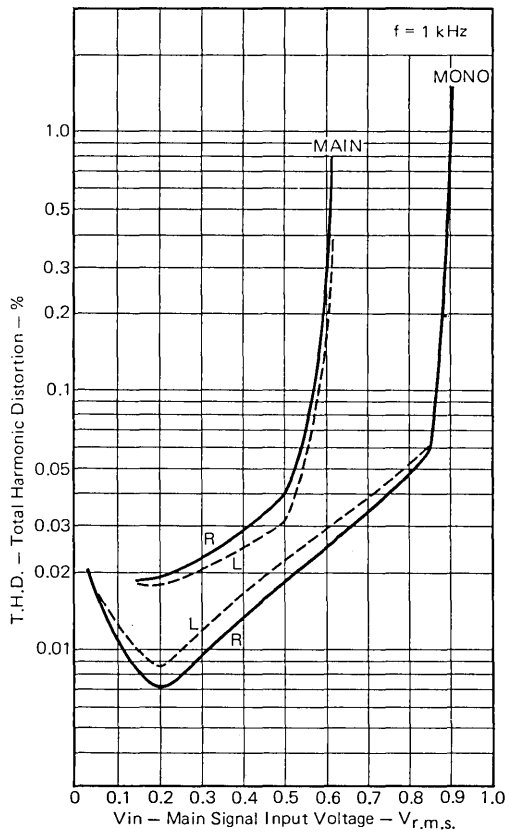


Fig. 34 TOTAL HARMONIC DISTORTION vs. MAIN SIGNAL INPUT VOLTAGE

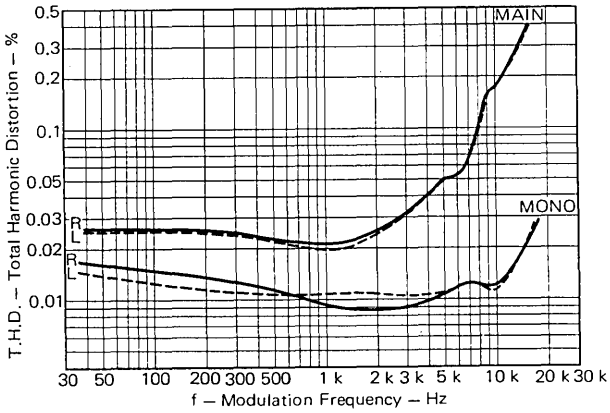


Fig. 35 TOTAL HARMONIC DISTORTION vs. MODULATION FREQUENCY

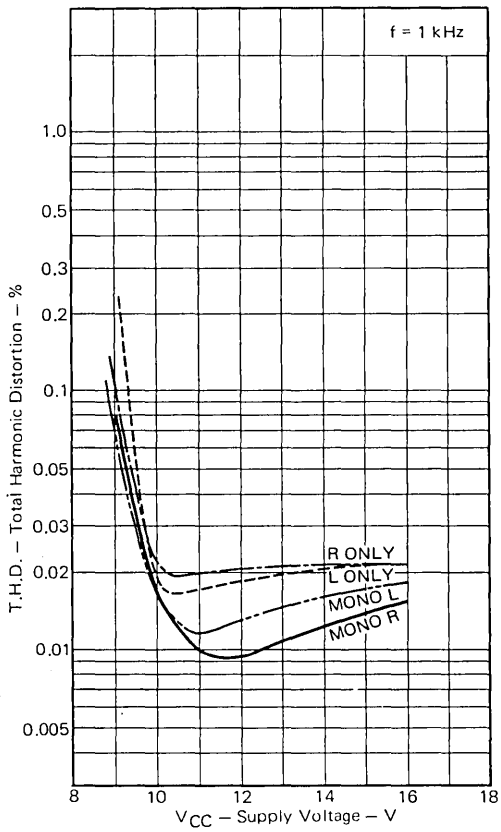


Fig. 36 TOTAL HARMONIC DISTORTION vs. SUPPLY VOLTAGE

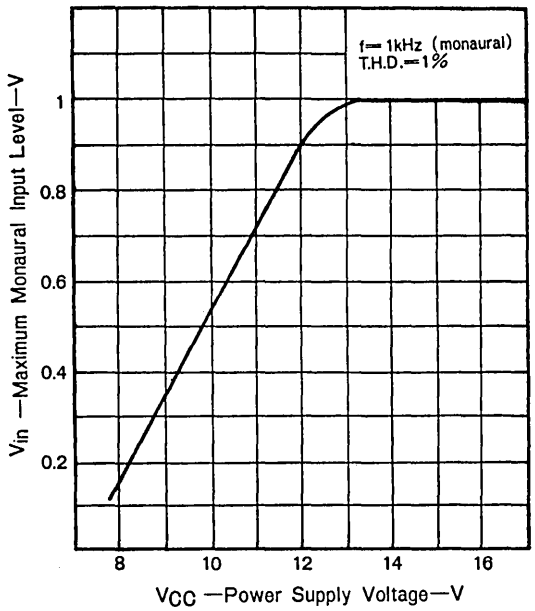


Fig.37 MAXIMUM MONAURAL INPUT LEVEL vs.POWER SUPPLY VOLTAGE

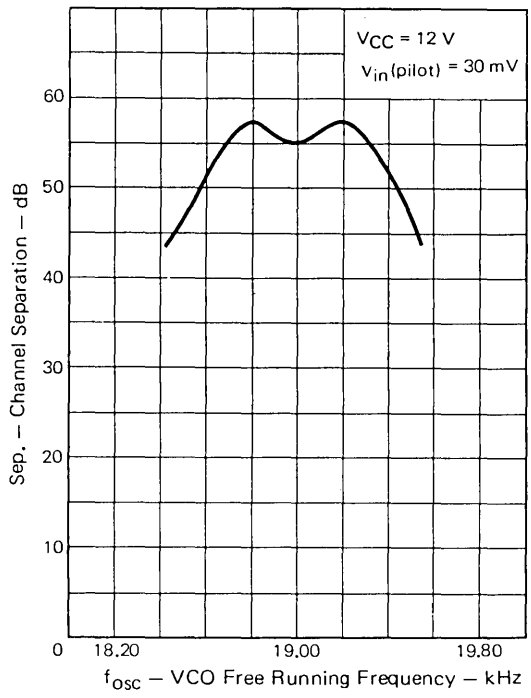


Fig. 38 CHANNEL SEPARATION vs. VCO FREE RUNNING FREQUENCY

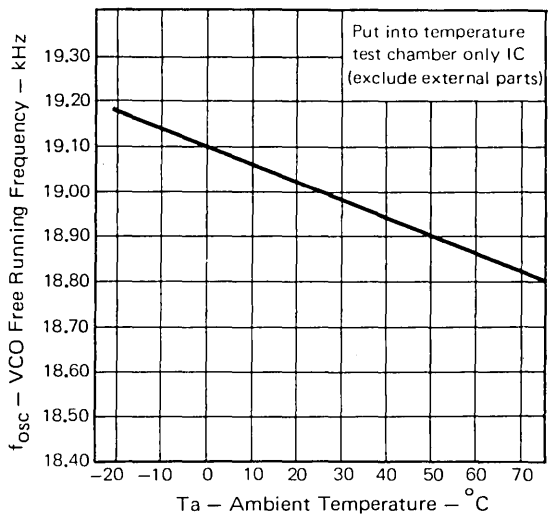


Fig. 39 VCO FREE RUNNING FREQUENCY vs. AMBIENT TEMPERATURE

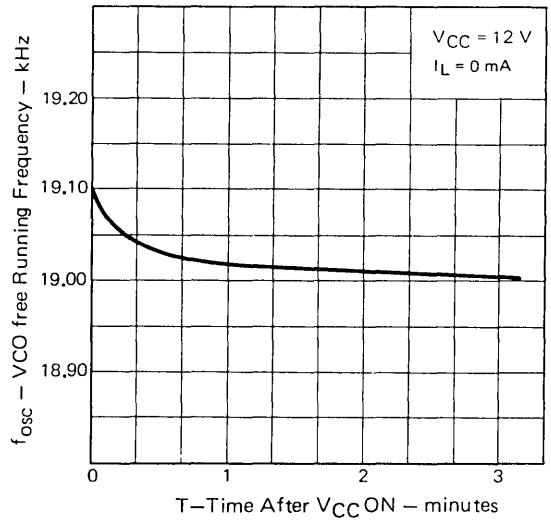


Fig. 40 TIME DRIFT OF VCO FREE RUNNING FREQUENCY

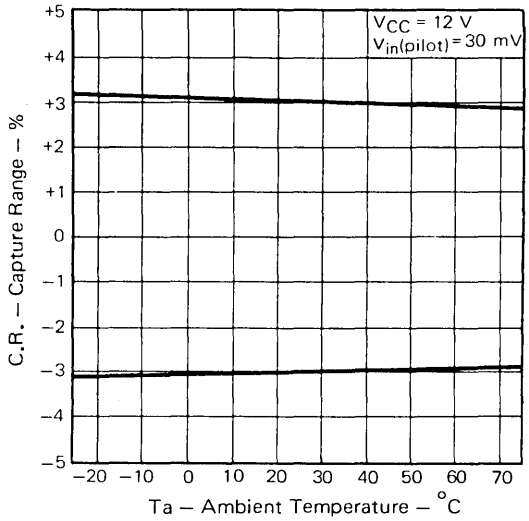


Fig. 41 CAPTURE RANGE vs. AMBIENT TEMPERATURE

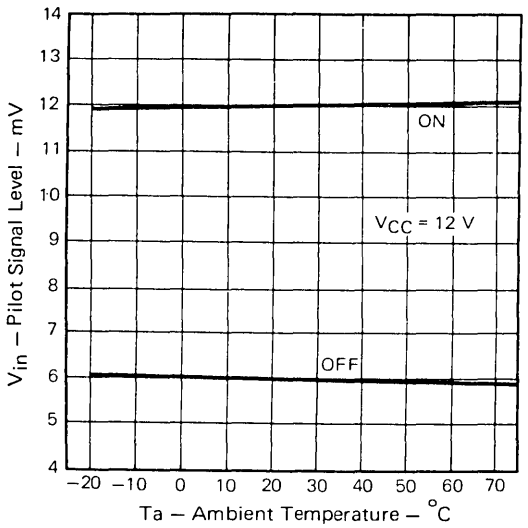


Fig. 42 PILOT LAMP INPUT LEVEL FOR LAMP ON-OFF vs. AMBIENT TEMPERATURE

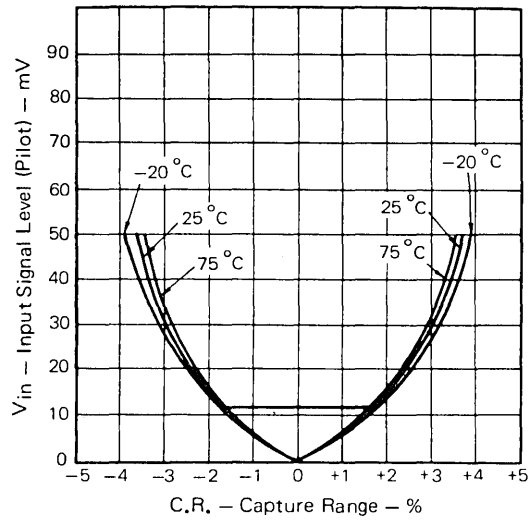


Fig. 43 PILOT LEVEL AND AMBIENT TEMPERATURE vs. CAPTURE RANGE

μPC1222C AND μPC1222C(R) : THEIR OPTIMUM USAGE

1 OUTLINE OF μPC1222

The μPC1222 is a silicon monolithic integrated circuit operating on a low supply voltage. It includes an FM-IF amplifier, FM detecter, AM-MIX, OSC, AM/IF-Amp., AM-detecter, and AGC circuit.

Its optimum usage is for radio sets and radio cassette sets with 4.5 V power supply, however, its characteristics allow it to be used for medium class stereo radio cassette sets.

2 DIFFERENCE BETWEEN μPC1222C AND μPC1222C(R)

μPC1222C(R) (hereinafter called (R) type) has suffix (R) which stands for "reverse" to indicate that the detection characteristic curve of the FM detecter, or so-called S curve, is in reverse to that of μPC1222C (called C type).

Since their electrical characteristics are, except S curves, utterly same, they can be used without any difference for sets using no AFC.

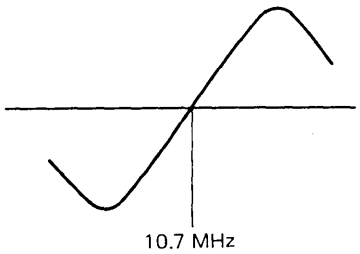


Fig. 1-a S curve of C type

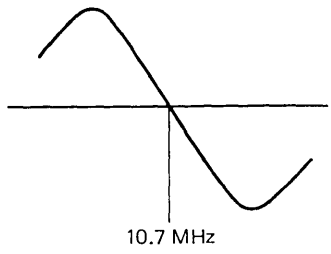


Fig. 1-b S curve of (R) type

3 THE PROPER USE OF C TYPE AND (R) TYPE

On designing an FM radio set, its AFC circuit is configured as shown in Fig. 2-a when the set is for domestic (Japanese) use, and as shown in Fig. 2-b when for overseas use.

The circuit shown in Fig. 2-b has one more external resistor than that shown in Fig. 2-a and setting of the bias is more complicated in the former circuit (Fig. 2-b).

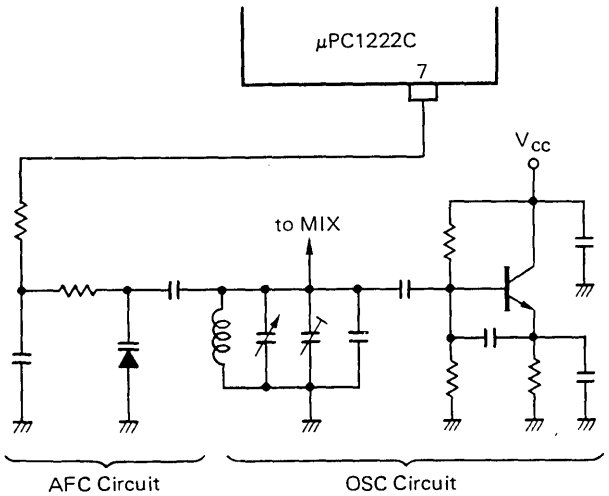


Fig. 2-a AFC circuit in the Japanese system

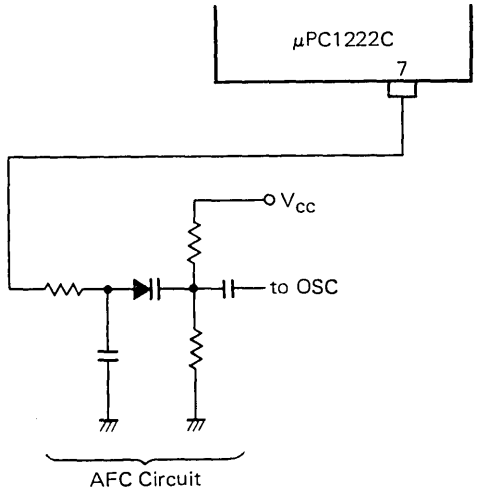


Fig. 2-b AFC circuit in the American and European systems

In these cases, if an (R) type is used for an American or European system, its AFC circuit can be as that shown in Fig. 2-a.

Therefore, same printed circuit boards can be used for domestic and overseas sets whose reception wave bands are designed as so-called wide band (76 to 180 MHz).

Thus, the proper use of μPC1222 is configuring the AFC circuit as shown in Fig. 2-a, and;

using μPC1222C for domestic sets, and

using μPC1222C(R) for overseas sets.

4 DIFFERENCE IN INTERNAL STRUCTURE

The internal structure of the (R) type is completely same as that of the C type except connections of R_{48} and R_{49}. In the (R) type they are connected in reverse to those in the C type.

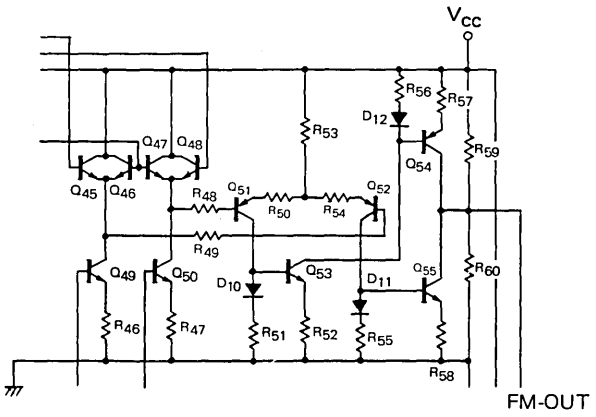


Fig. 3-a μPC1222C

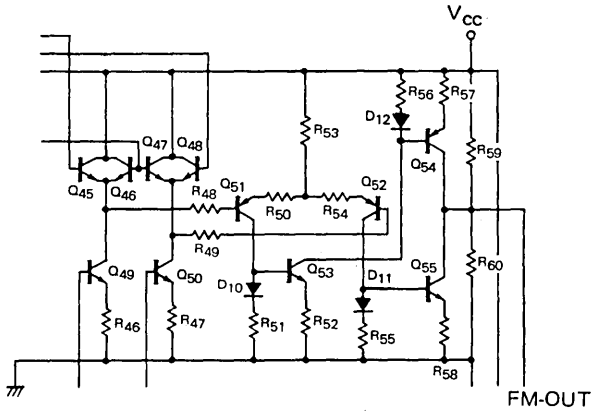


Fig. 3-b μPC1222C (R)

μPC1222C(R), μPC1222C; APPLICATION TO SHORT WAVE BAND

1 OUTLINE OF μPC1222C(R), μPC1222C

μPC1222C(R) and μPC1222C are FM-IF/AM Tuner System ICs operating at low voltages (V_{CC}=2 V min.) and it includes detection circuits. μPC1222C(R) is same as μPC1222C in their characteristics except that their FM detection S curves are in reverse to each other. Hereinafter, they are represented by μPC1222.

2 APPLICATION OF μPC1222 TO SHORT WAVES

1) Notices on Designing Oscillation Coils

1 Making coupling between primary and secondary of oscillation coils as tight as possible:
When the secondary coil is tightly coupled to the primary, the oscillation frequency is determined by L and C of the primary side. On the contrary, if this coupling is loose, oscillation whose frequency is determined by secondary coil and capacity of inside IC occurs to affect the waveform of oscillation to be introduced into #1 pin and sometimes to stop oscillation.

2 Making the turn ration of primary and secondary coils large:
The larger number of turns of the secondary coil enables what is described above (1). Be careful, however, that, by so doing, capacity within the IC affects the primary side to make it sometimes impossible to acquire the cover range desinged using the value of L in the primary side.

In order to satisfy what are mentioned in 1 and 2 simultaneously, it is a good method to wind the secondary coil over the primary as shown in Fig. 1. Split winding, shown in Fig. 2, generally used for short waves is not suitable for μPC1222, an oscillation circuit.

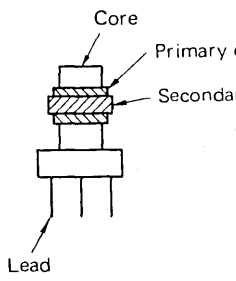


Fig. 1

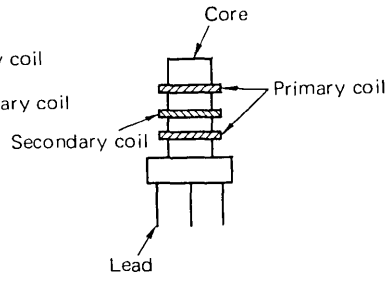
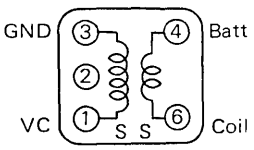


Fig. 2

2) Example of Oscillation Coil for Short Wave

An oscillation coil for short waves made as an example is explained below:



- Bobbin : ϕ 7.5 mm
- Core: 10 MHz
- Wire material: polyurethane covered copper wire
  diameter: 0.15 mm

Fig. 3 Coil terminal connection

Table 1 Coil data and Oscillation Frequencies

Coil No.	Inductance	No load Q	Number of turns	Way of winding	Oscillation frequency (VC : 80 pF)
No. 1	①–③ 29 μH	①–③ 71 (2.52 MHz)	①–③: $44\frac{3}{4}$T ④–⑥: $8\frac{3}{4}$T	Overlap	2.6 ~ 6.4 MHz
No. 2	①–③ 4.85 μH	①–③ 74 (7.96 MHz)	①–③: $14\frac{3}{4}$T ④–⑥: $3\frac{3}{4}$T	Overlap	7.6 ~ 23 MHz
No. 3	①–③ 1.24 μH	①–③ 68 (7.96 MHz)	①–③: $7\frac{3}{4}$T ④–⑥: $3\frac{3}{4}$T	Parallel	19.6 ~ 42 MHz
No. 4	①–③ 0.44 μH	①–③ 66 (25.2 MHz)	①–③: $3\frac{3}{4}$T ④–⑥: $3\frac{3}{4}$T	Parallel	25 ~ 70 MHz

Note 1: Coils are designed so that they match the trackingless variable capacitor (C_{OSC} Max.=80 pF) used for MW.

2: "Overlap" and "Parallel" in the item of "Way of winding" represent those shown in Figs. 4 and 5 respectively. Winding Coils No. 3 and 4 in parallel offers no problem. It is because coupling between primary and secondary coils is tight enough due to high frequency.

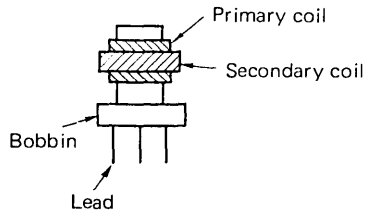


Fig. 4 Overlap winding

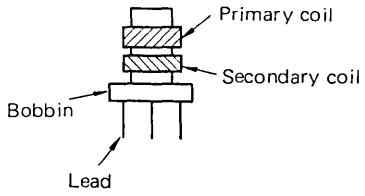


Fig. 5 Parallel winding

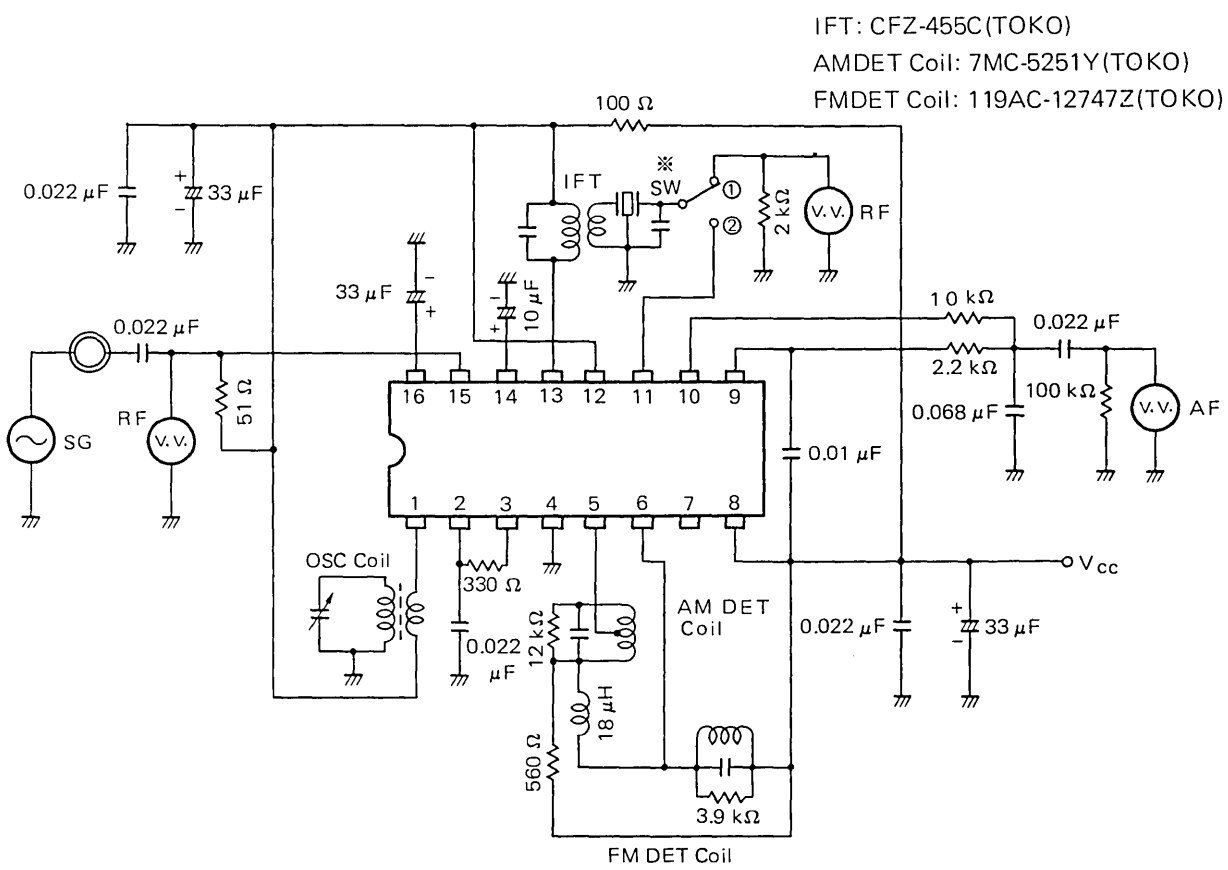
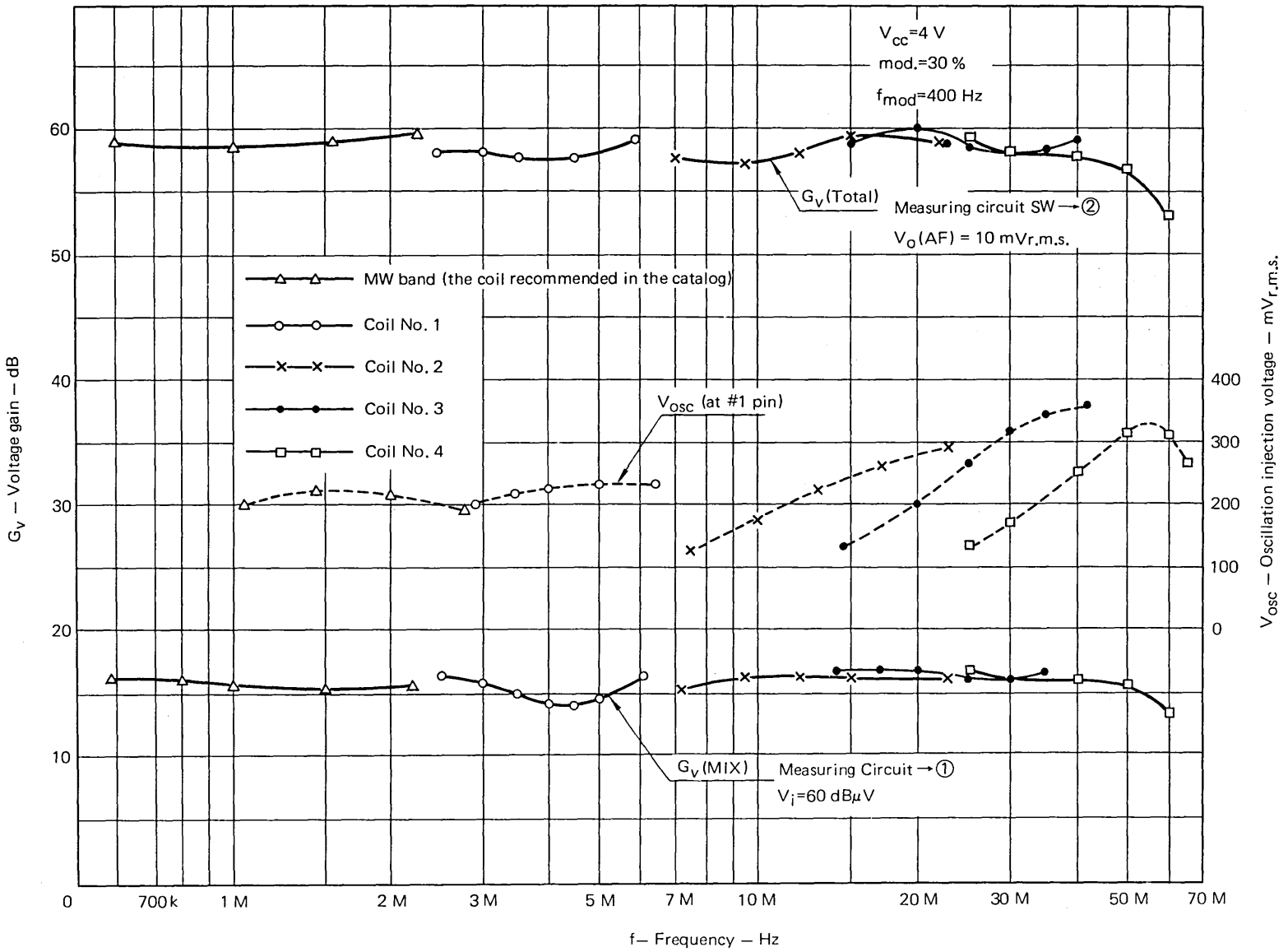


Fig. 6 Short wave measuring circuit

※ Turn the switch (SW) to ① when MIX gain measuring, and to ② when total gain measuring.

Fig. 7 VOLTAGE GAIN AND OSCILLATION VOLTAGE vs. FREQUENCY



APPLICATION OF THE μPC1197C INTEGRATED CIRCUIT PLL MULTIPLEX STEREO DEMODULATOR

1. DESCRIPTION

The μPC1197C is a silicon monolithic integrated circuit designed for PLL (Phase Locked Loop) FM multiplex stereo demodulator applications in FM stereo radio receivers. The device contains VCO (Voltage Controlled Oscillator), phase detectors, LPF (Low Pass Filter), frequency dividers and DC amplifiers for a stereo composit signal. It also contains an automatic stereo-monaural switching circuit, a VCO mute circuit for FM/AM radio application, a forced monaural switch-over circuit, and an automatic change-over circuit from stereo to monaural at low supply voltage.

2. FEATURES

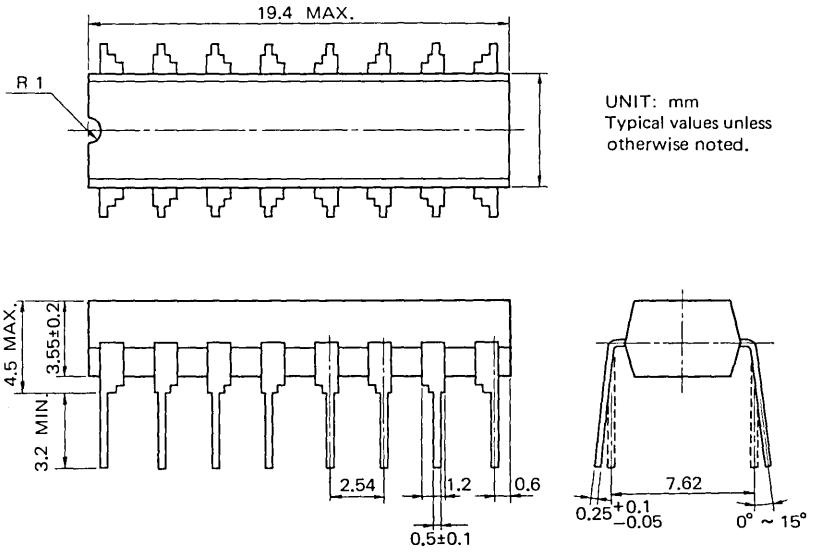
(1) Wide operating voltage range. V_{CC} = 4 to 16 V
(2) Low noise stereo-monaural switch-over.
(3) Built in switch-over circuit for forced monaural and VCO mute circuits for FM/AM radio application.

$V(\#9) \geq 3$ V for VCO mute

$0.7\ V \leq V\ (\#9) < 3$ V for forced monaural

(4) Automatic switch-over from stereo to monaural at low supply voltage. ($V_{CC} \leq 3.5$ V)
(5) No coil is necessary, all tuning is performed with only two potentiometers.
(6) The terminal (8) is for separation adjust.

3. PACKAGE DEMENSIONS



UNIT: mm
Typical values unless otherwise noted.

4. BLOCK DIAGRAM

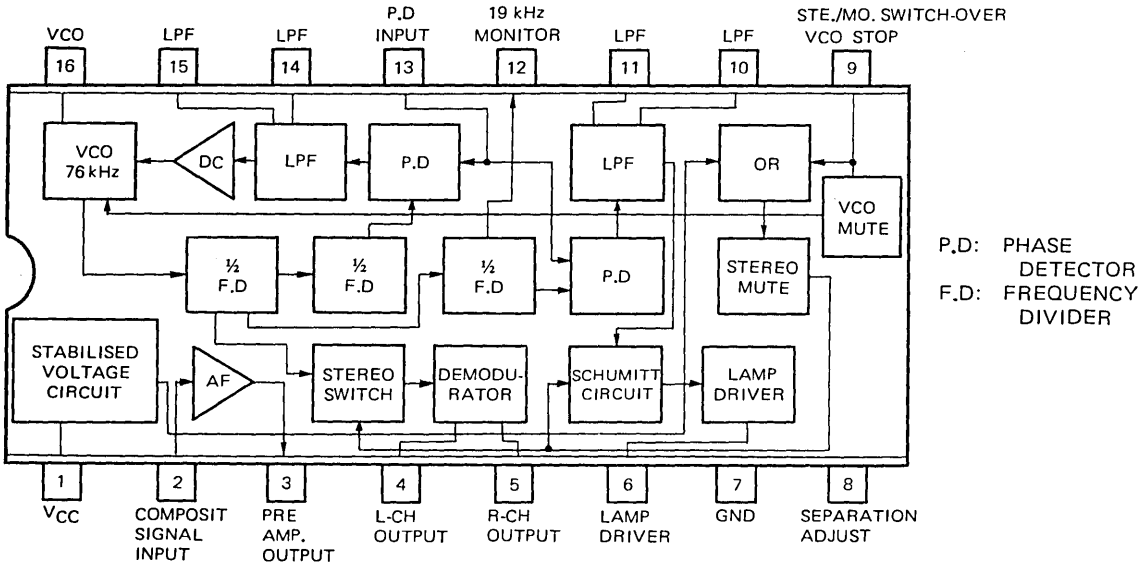


Fig.1 Block Diagram

5. ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	16	V
Package Dissipation	PD	350*	mW
Operating Temperature	Topt	−20~+75	°C
Storage Temperature	Tstg	−40~+125	°C

* Ta = 75 °C

6. RECOMMENDED CONDITION (Ta = 25 °C)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	4	9	16	V

7. ELECTRICAL CHARACTERISTICS

(Ta=25 °C, V_{CC}=9 V, υi=200 mVr.m.s., L=45 %, R=45 %, PILOT=10 %)

CHARACTERISTIC	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Circuit Current	I_{CC}	No Signal	7	12	16	mA
Separation	Sep.	f=100 Hz	30	45		dB
		f=1 kHz	40	55		dB
		f=10 kHz	30	45		dB
Total Harmonic Distortion	T.H.D.	υi=200 mVr.m.s. Monaural		0.3	0.5	%
Total Harmonic Distortion	T.H.D.	υi=200 mVr.m.s. Stereo		0.2	0.5	%
Output Voltage	υ_o	υi=200 mVr.m.s. Monaural		170		mVr.m.s.
Channel Balance	ch.B	υi=200 mVr.m.s. Monaural	−2	0	2	dB
Input Pilot Level for Lamp ON	LAMP-ON	υi=Pilot	4	8	12	mVr.m.s.
Lamp Hysteresis	Hys. (LAMP)	υi=Pilot		4		dB
Caputure Range	C.R.	υi(pilot)=20 mVr.m.s.	±1.5	±4		%
Ultrasonic Frequency Rejection	Rej. (19)	υi(pilot)=20 mVr.m.s.		35		dB
	Rej. (38)	υi(pilot)=20 mVr.m.s.		45		dB
SCA Rejection	Rej. (SCA)	$\frac{\upsilon i(pilot)}{\upsilon i(compsit)} = \frac{1}{10}$, $\frac{\upsilon i(SCA)}{\upsilon i(composit)} = \frac{1}{10}$		70		dB
Maximum Input Level	υi(MAX.)	T.H.D.≦2 %		500		mVr.m.s.
Signal To Noise Ratio	S/N	υi=200 mVr.m.s.		86		dB
Forced Monaural	V(Monaural)	Terminal No. 9		0.7		V
VCO Stop	V(Stop)	Terminal No. 9	2.7	3.0	3.7	V
Stereo-Monaural Switch-over Voltage	V_{CC}(Monaural)	Supply Voltage		3.5		V

8. TEST CIRCUIT

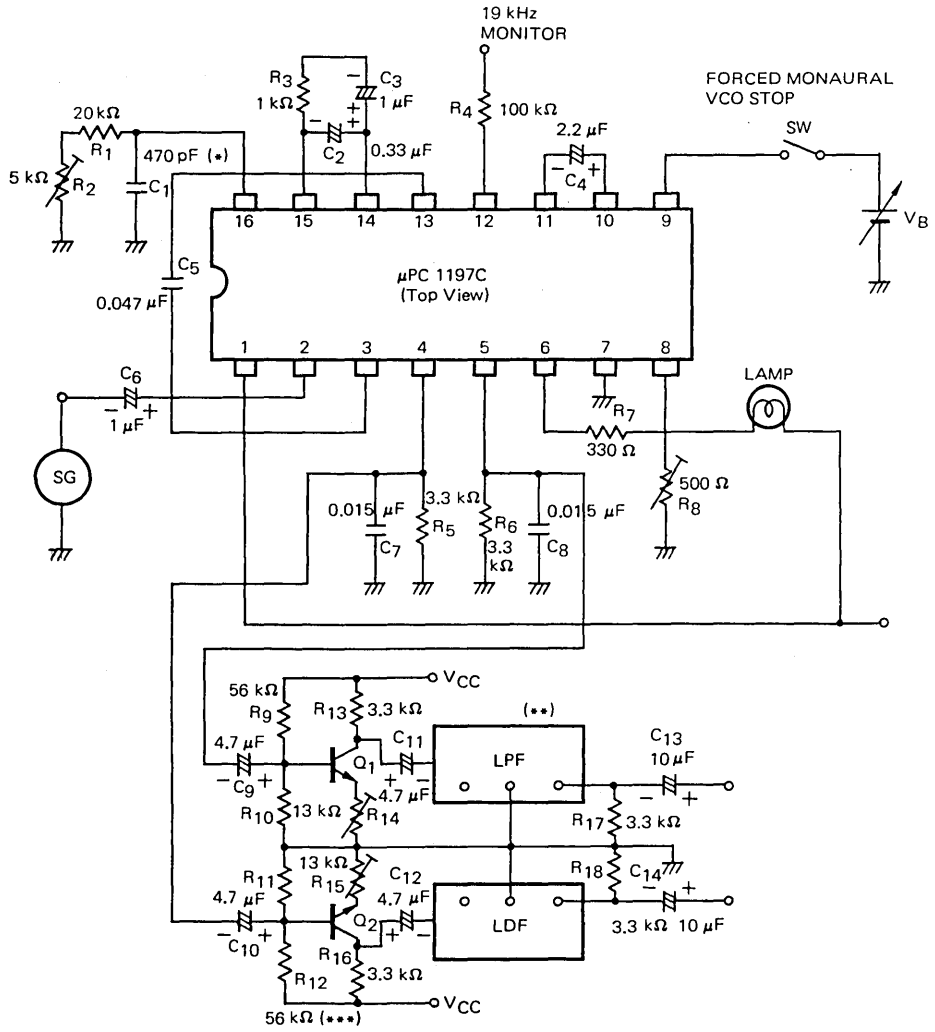


Fig.2 Test Circuit

* POLYSTYLENE CAPACITOR
** LOW PASS FILTER: BL – 13 (KORIN LAB.)
*** Transistors Q_1 and Q_2 should be set so that, the voltage gain between the output terminal of the IC and the output terminal of the LPF is 0 dB.

9. EQUIVALENT CIRCUIT

Fig.3 shows the equivalent circuit of the μPC 1197C

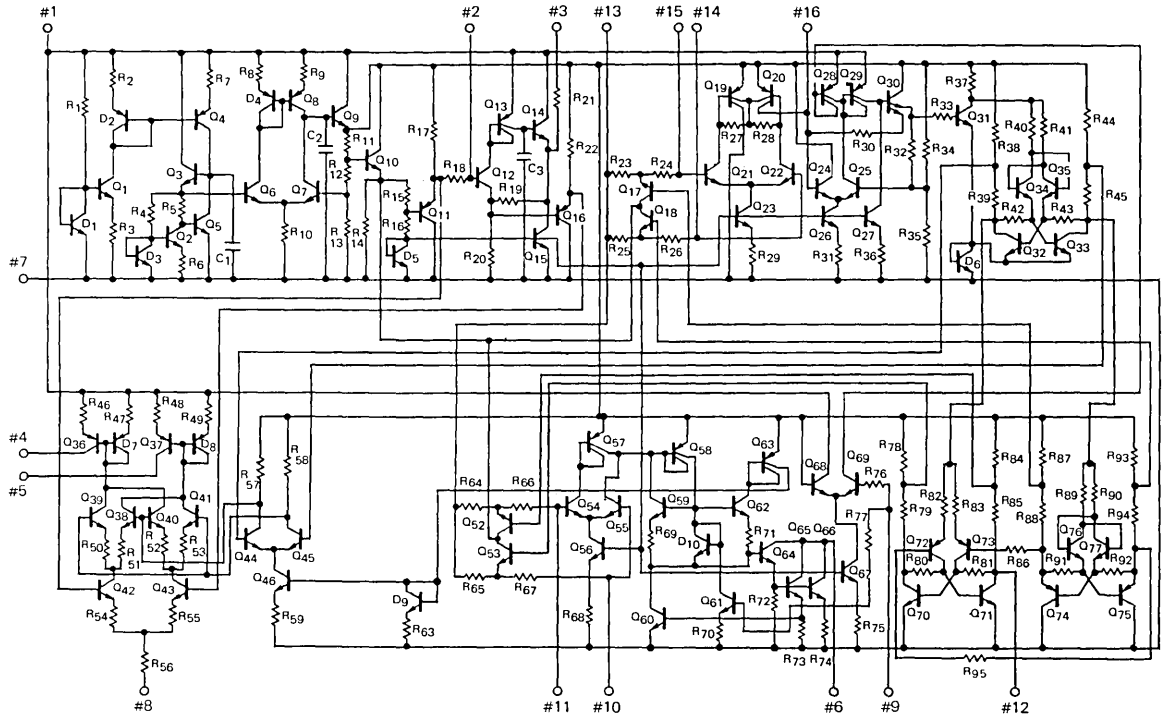


Fig.3 Equivalent Circuit

10. DESCRIPTION OF EXTERNAL DISCRITE COMPONENTS

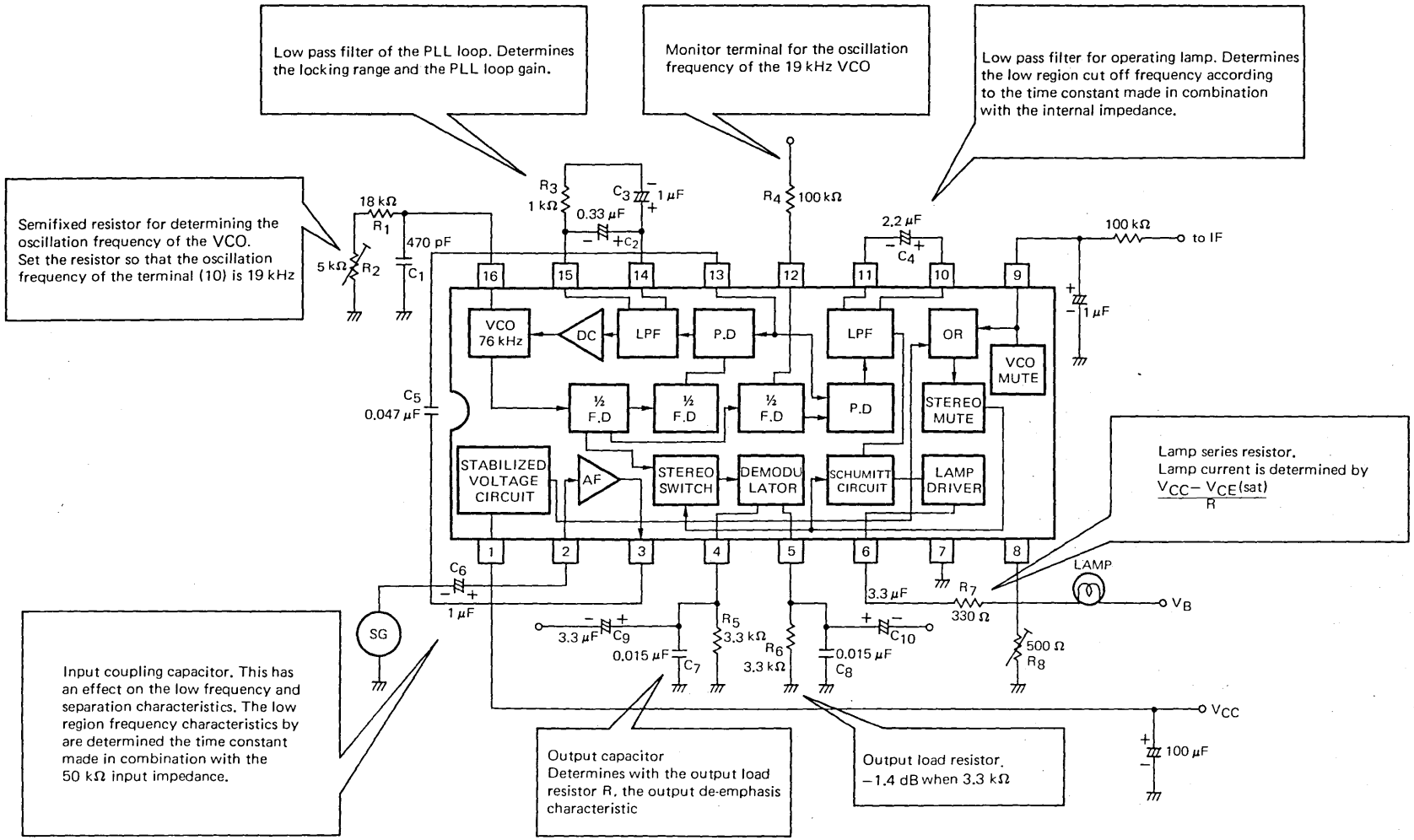


Fig.4 Description of External Discrete Components

11. TYPICAL APPLICATION

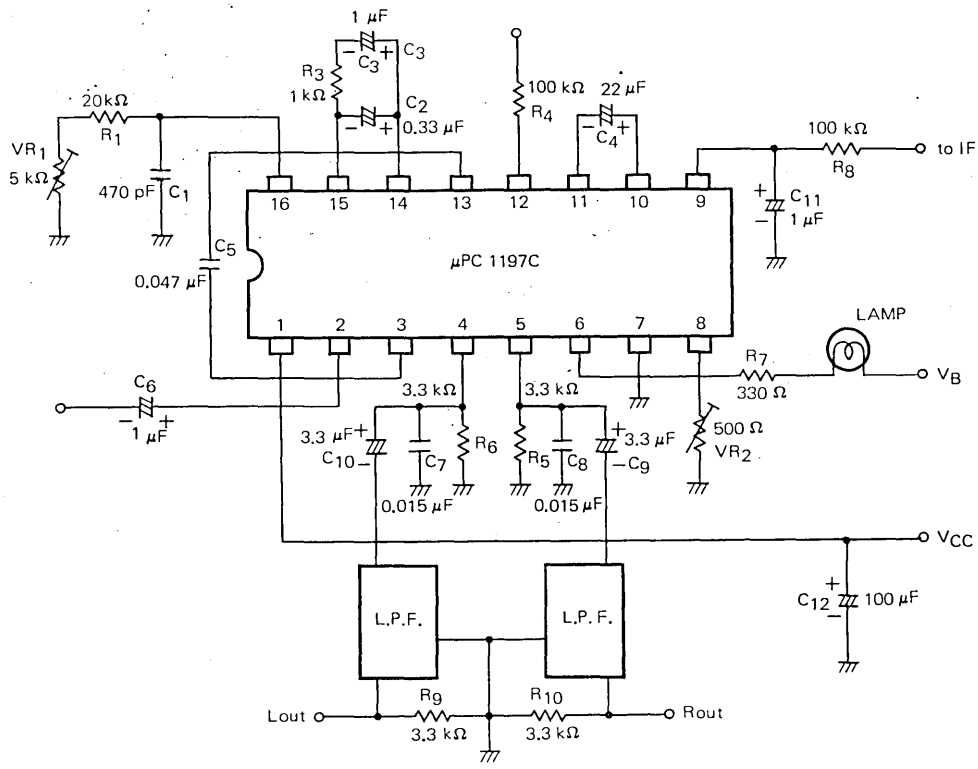


Fig. 5 Typical Application

11-1. Notes for Use

(1) The μPC1197C is designed to have a equivalent thermal constant to a polystylene capacitor.

(2) In the application which the terminal (9) is connected to the terminal (1) to force monaural or to stop VCO, when the supply voltage is over 10 voltages, insurt a resistor which have a value shown by the next equation.

$$1.1\left\{V_{CC}\ (MAX.) - 10\right\} \leq R \leq 2\left\{V_{CC}\ (MAX.) - 4\right\}$$

V_{CC} (MAX.) : Maximum voltage of a power supply
V_{CC} (MIN.) : Minimum voltage of a power Supply

11-2. Printed wiring board (Copper side)

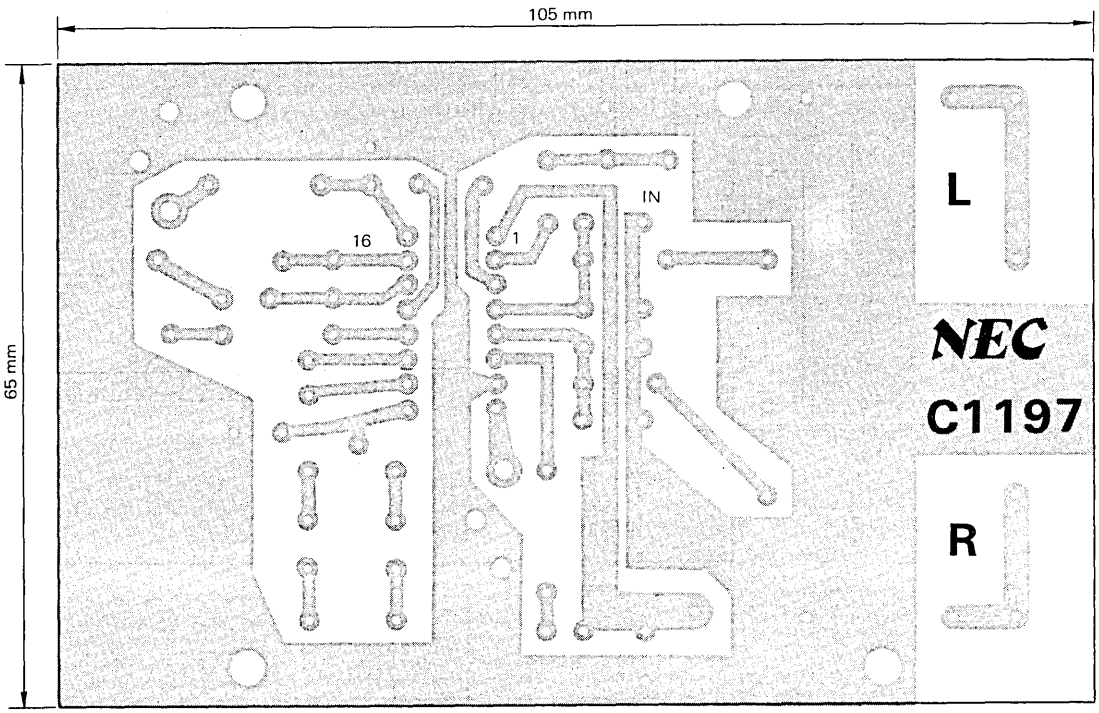
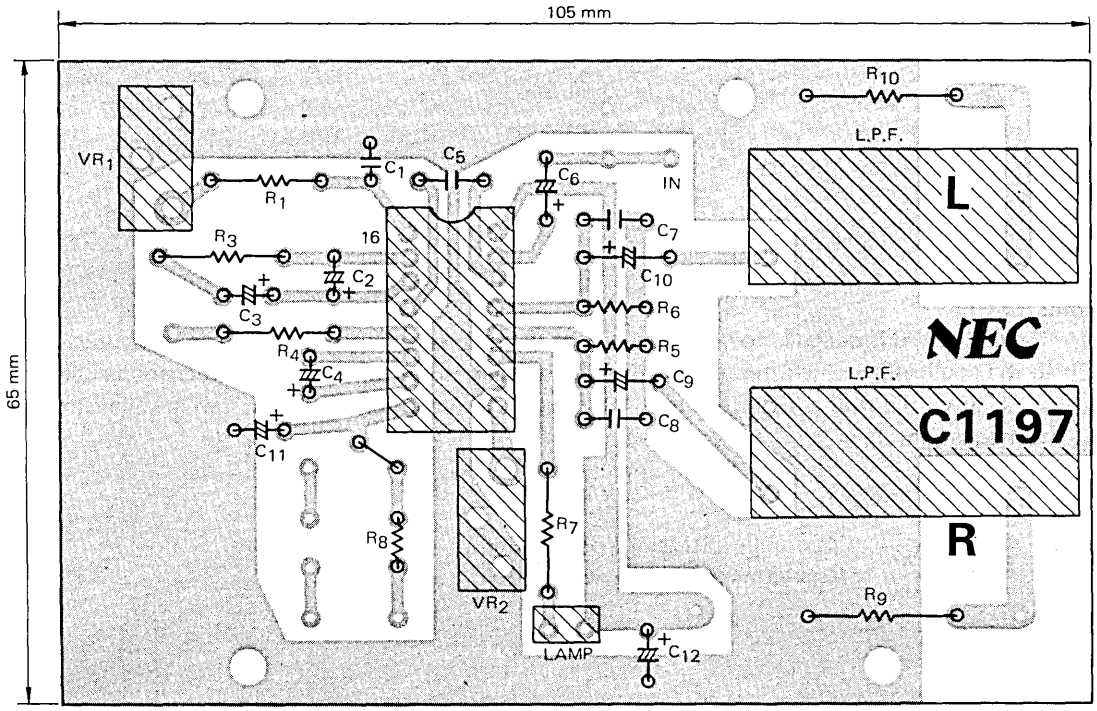


Fig. 6 Printed Wiring Board

11-3. Components layout for P.W. assembly (Copper side)



R_1 = 18 kΩ
VR_1 = 5 kΩ
R_3 = 1 kΩ
R_4 = 100 kΩ
R_5 = 3.3 kΩ
R_6 = 3.3 kΩ
R_7 = 330 Ω
R_8 = 100 kΩ
R_9 = 3.3 kΩ
R_{10} = 3.3 kΩ
C_1 = 470 pF
C_2 = 0.33 μF
C_3 = 1 μF
C_4 = 2.2 μF
C_5 = 0.047 μF
C_6 = 1 μF
* POLYSTYLENE CAPACITOR
C_7 = 0.015 μF
C_8 = 0.015 μF
C_9 = 3.3 μF
C_{10} = 3.3 μF
C_{11} = 1 μF
C_{12} = 100 μF

Fig. 7 Components Layout for P.W. Assembly

12. DESCRIPTION OF CIRCUIT

12-1. Stabilized Voltage Circuit

The equivalent circuit of the stabilized voltage Circuit is shown in Fig. 8. In Fig. 8 the stabilized voltage Vs is expressed by the equation (1), the reference voltage Vr is expressed by the equation (2). Both are constant against variations of the power supply.

$$Vs = \frac{R_{11} + R_{12} + R_{13}}{R_{13}} \times Vr \quad \cdots\cdots\cdots\cdots \quad (1)$$

$$Vr = \frac{R_5}{R_6} \left\{ V_{BE}(D_3) - V_{BE}(Q_2) \right\} + V_{BE}(Q_5) \quad \cdots\cdots \quad (2)$$

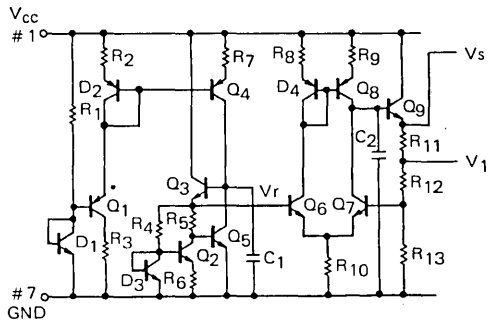


Fig. 8 Stabilized Voltage Circuit

The biases of other circuits are designed with the stabilized voltage Vs. The circuit composed of a diode D3, transistors Q_2, Q_5 and resistors R_4, R_5, R_6 is the thermal compensation circuit of the reference voltage Vr.

$$Vr = V_{BE(Q5)} + Ic_{(Q2)} \cdot R_5 + I_{B(Q5)} \cdot R_5$$

$$= V_{BE(Q5)} + \frac{R_5}{R_6} \Delta V_{BE} + I_{B(Q5)} \cdot R_5 \quad (\Delta V_{BE} = V_{BE(D3)} - V_{BE(Q2)})$$

$$= V_{BE(Q5)} + \frac{R_5}{R_6} \left(\frac{KT}{q} \ln \frac{JD3}{JQ2} \right) + I_{B(Q5)} \cdot R_5$$

$$\fallingdotseq V_{BE(Q5)} + \frac{R_5}{R_6} \left(\frac{KT}{q} \ln \frac{R_5}{R_4} \right) \cdots\cdots\cdots\cdots (3)$$

$$(I_{B(Q5)} \cdot R_5 \ll 1)$$

$$\frac{\partial Vr}{\partial T} = \frac{\partial V_{BE(Q5)}}{\partial T} + \frac{K}{q} \cdot \frac{R_5}{R_6} \ln \left(\frac{R_5}{R_4} \right) \cdots\cdots\cdots (4)$$

The equation (4) expresses the reference voltage compensated against thermal vaviations is given by to choose the values of resistors R_4, R_5 and R_6 fitly.

12-2. Input Signal Amplifier

The equivalent circuit of the input buffer amplifier is shown in Fig. 9. The input signal amplifier is composed of transistors Q_{12}, Q_{13}, Q_{14}, resistors R_{19}, R_{20}, R_{21} and a capacitor C_3. Since transistor Q_{13} is a multi-collector transistor, its collector current is nearly the same as the collecter current of transistor Q_{12}. And its current gain is close to unity. Capacitor C_3 is for frequency stability, and its value is 5 to 20 pF.

The voltage gain of the input signal amplifier is determined by the feedback circuit R_{19}, R_{20}, and expressed by the following equation (5).

$$A_{V(AF)} = \frac{R_{19} + R_{20}}{R_{20}} \quad \cdots\cdots\cdots\cdots\cdots \quad (5)$$

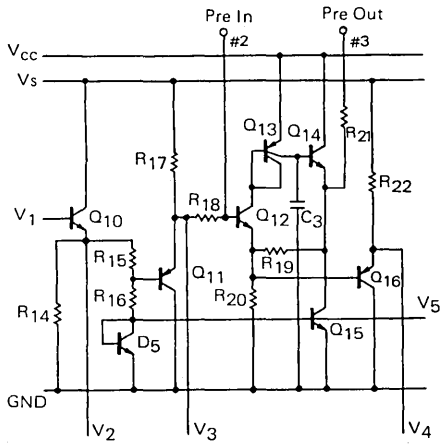


Fig. 9 Input Signal Amplifier

Stereo signals entering terminal (2) are amplified by an amount indicated the above equation, and then introduced to the phase detector of the PLL circuit through terminal (3). Besides the above, stereo signals pass through emitter follower Q_{16} and are injected into the stereo demodulator circuit.

12-3. Demodulator Circuit

The equivalent circuit of the stereo demodulator is shown in Fig. 10. The circuit consists of a common double-balanced type detector circuit, the stereo signals are injected into the lower transistors Q_{42} and Q_{43} while the 38 kHz subcarrier is injected into the upper transistors Q_{38}, Q_{39}, Q_{40} and Q_{41}. Stereo demodulation is accomplished by the subcarrier switching the above transistors.

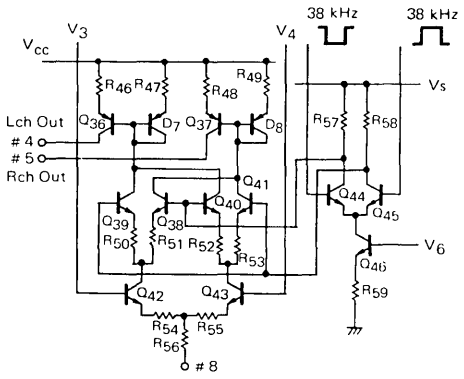


Fig. 10 Demodulator Circuit

The resistors R_{54}, R_{55}, R_{50} and external resistor R_8 (Fig. 2) are feedback resistors inserted for the parpose of cancelling the cross talk components produced during the switching. To adjust the external resistor R_8 give the best separation.

The subcarrier is a 50 % duty cycle 38 kHz wave obtained from bistable multivibrator (flip-flop) circuit, into which a 76 kHz signal produced by the VCO is injected. In the μPC1197C the stereo lamp and stereo demodulation are synchronized and accomplished by transistor Q_{46}. The base of Q_{46} is controlled by the stereo lamp circuit, and when the stereo lamp is turned on Q_{46} will also be turned on and a 38 kHz subcarrier of reverse phase will be injected into the demodulation circuit, Q_{38}, Q_{39}, Q_{40} and Q_{41}. On other hand, when the stereo lamp is turned off Q_{46} is also turned off, and an in-phase 38 kHz subcarrier is injected into Q_{38}, Q_{39}, Q_{40} and Q_{41} so that a monaural wave is obtained from the output terminal (4) and (5).

12-4. Lamp Driver

Fig. 11 shows a lamp driver circuit with its auxiliary circuits.

The phase detector circuit and low pass filter are composed of transistors Q_{52}, Q_{53}, resistors R_{64}, R_{65}, R_{66}, R_{67} and the external capacitor C_4 (Fig. 2)

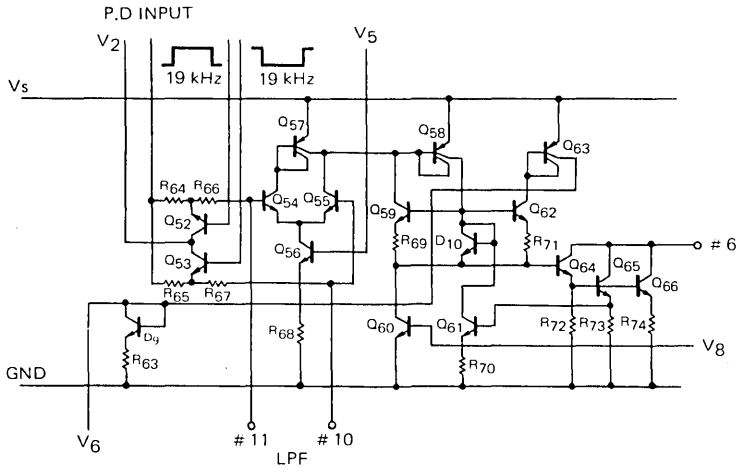


Fig. 11 Lamp Driver

The lamp driver circuit is composed of transistors Q_{54} to Q_{66} with ist auxiliary resistors. Transistor Q_{54} and Q_{55} amplify the DC voltage obtained through LPF. Transistor Q_{57} is a active load of the differential amplifier. Now, if the collector current Ic (Q54) of Q_{54} and $I_{C\ (Q55)}$ of Q_{55} change by $\triangle Ic$ ($\triangle Ic = I_{C(Q55)} - Ic\ (Q54)$), due to the control current passed through the phase detector, $\triangle Ic$ will flow intact into the base of Q_{58}.

Q_{58} is a multicollector transistor, and its collector current will amplify the change $\triangle Ic$ of the base current and D_{10} will become biased by this current. And, when this diode is biased transistor Q_{62} will operate causing lamp driving transistor Q_{64} to be turned on, thus the lamp will light. On the other hand, when Q_{62} turns on it will draw the base current of Q_{63}, and as a result Q_{63} and Q_{46} will be turned on and stereo operation will start.

Since transistors Q_{58}, Q_{59} diode D_{10} and resistor R_{69} form a positive feedback loop, when the lamp is turned on, this rise of current will be abrupt. In addition transistors Q_{61}, Q_{64}, Q_{65} and resistor R_{73} form a negative feedback loop, which composes a current limiting circuit for performing current limiting action.

12-5. Phase Detector and DC Amplifier

Fig. 12 shows the phase detector and the DC amplifier.

The 19 kHz signal obtained through the divider will switch the pilot signal of the stereo signals coming into terminal 13, and will supply a DC voltage proportional to the phase difference of these to the DC amplifier composed of Q_{19} to Q_{23}. When the phase difference of the 19 kHz signal and pilot signal, entering the phase detector, is 90° the control voltage of the PLL circuit will be O. When the phase of the 19 kHz signal advances from the above, a positive control voltage will be produced, and when the 19 kHz phase lags a negative control voltage will be produced.

When this state is expressed as an equation, it becomes as follows.

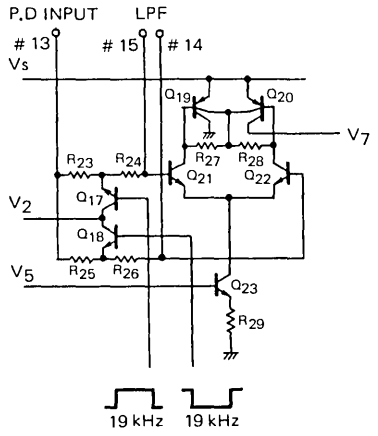


Fig. 12 Phase Detector and DC Amplifier

Pilot Signal $e_{p\,(t)} = Ep \cos \omega pt$

19 kHz Signal $e_{19\,(t)} = E_{19} \sin (\omega p + \phi)\, t$

(Note) (To be precise, 19 kHz is a square wave.)

$$e_p(t) \times e_{19}(t) = \frac{Ep \cdot E19}{2} \{ \sin\phi t + \sin (2\omega p + \phi)\, t \}$$

$$= \frac{Ep \cdot E19}{2} \sin\phi t \quad \ldots\ldots\ldots (6)$$ E liminated by LPF

The DC amplifier converts the change of the control voltage to current to be sent to the VCO.

12-6. VCO (Voltage Controlled Oscillator)

Fig. 13 shows the VCO.

This circuit is basically a comparator, which produces oscillations through variations of the reference voltage.

Now, when transistor Q_{25} is operating, both Q_{29} and Q_{30} will become conducting and the instantaneous reference voltage of the comparator applied to the bace of Q_{25} is expressed as follows.

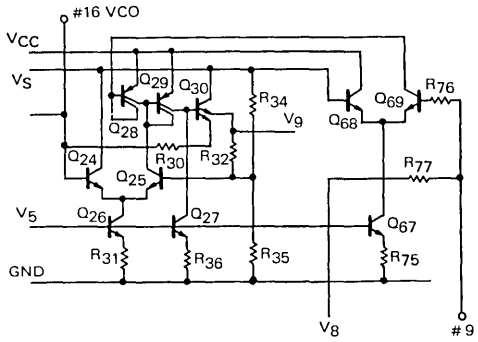


Fig. 13 VCO

$$VH = (VS - VCE(sat.)\ (Q_{30})) \times \frac{R_{35}}{R_{32} + R_{35}} \quad \ldots\ldots (7)$$

On one hand, current will flow from the emitter of Q_{30}, and this current will charge the external capacitor C_1 (Fig. 2) through R_{30}. The charging time t_1 of this capacitor is expressed as follows:

$$t_1 = R_{30} C_1 \ln \frac{VS - VL}{VS - VH} \quad \ldots\ldots\ldots\ldots\ldots (8)$$

When the above charging is completed the comparator will be switched-over and Q_{24} will be turned on. At this point, the reference voltage VL of the comparator will become as follows.

$$VL = VS \times \frac{R_{35}}{R_{34} + R_{35}} \quad \ldots\ldots\ldots\ldots\ldots\ldots (9)$$

The charge accumulated in the external capacitor of terminal 16 will discharge at a rate determined by the external resistor R_1, R_2 and capacitor C_1 (Fig. 2).

The forced monaural circuit and VCO stopper are composed of transistors Q_{67}, Q_{68}, Q_{28}, Q_{60} and resistors R_{76}, R_{77}. Q_{60} is turned on by the external voltage on terminal 9, and as a result Q_{64} turns off and the lamp turns off. ($0.7 \leq V_9 \leq 3$ V)

When higher voltage is added on terminal 9 Q_{69} will turn on, as a result Q_{29} will turn off and VCO will be stopped.

12-7. Divider Circuit

Fig. 14 shows the divider circuit.

This circuit is a bistable multivibrator (flip-flop). This multivibrator serves to produce 38 kHz and 19 kHz, 50 % duty cycle, signals from the 76 kHz signal generated by the VCO. The 38 kHz signal is the subcarrier required for FM stereo demodulation, the 19 kHz having a 90° phase difference with the pilot signal is required as the control voltage of the PLL, and the 19 kHz synchronized with the pilot signal is required for driving the stereo lamp and controlling the stereo switch.

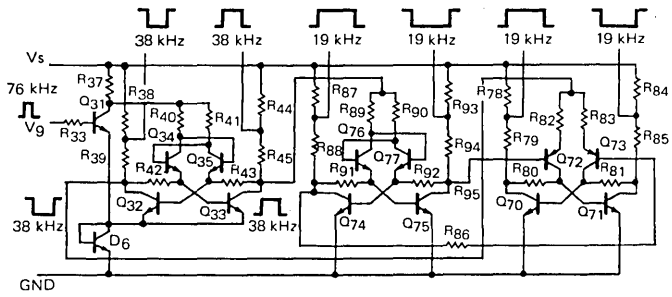


Fig. 14 Divider Circuit

13. CHARACTERISTIC CURVES

Fig.15 CIRCUIT CURRENT vs. SUPPLY VOLTAGE

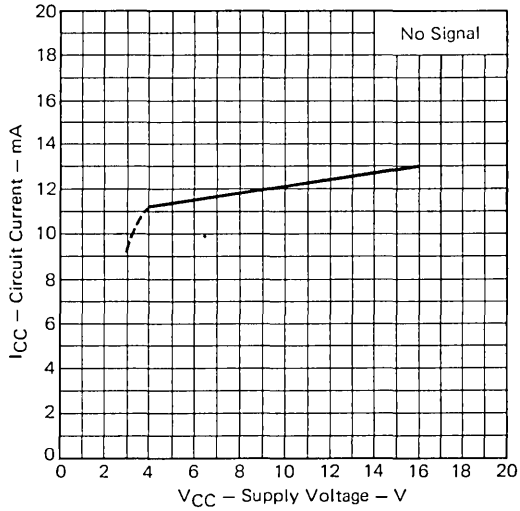


Fig.16 VOLTAGE GAIN vs. SUPPLY VOLTAGE
(Monaural)

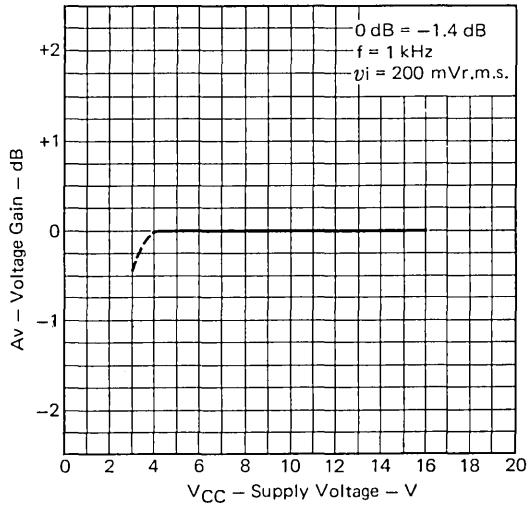


Fig.17 SEPARATION vs. SUPPLY VOLTAGE
(Stereo)

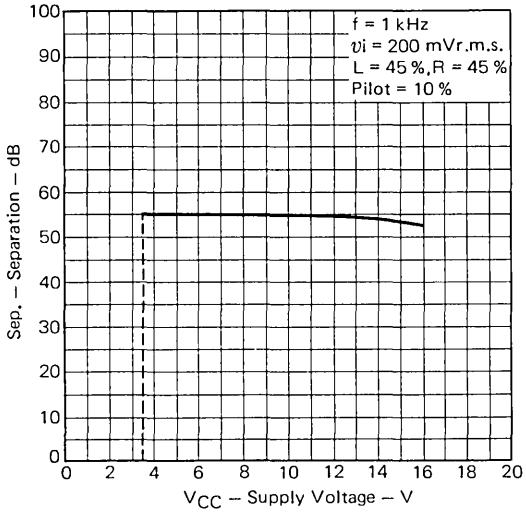


Fig.18 CHANNEL BALANCE vs. SUPPLY VOLTAGE
(Monaural)

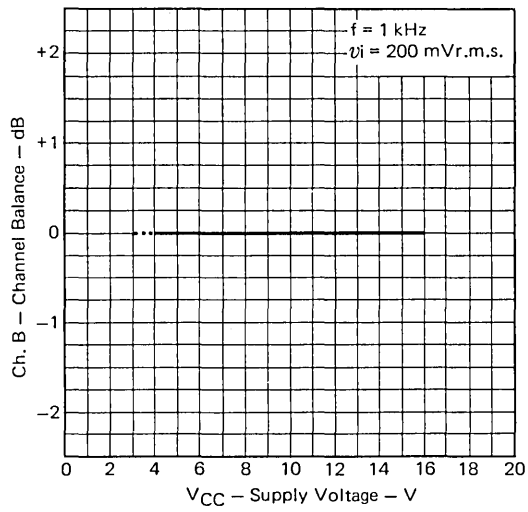


Fig.19 VOLTAGE GAIN vs. FREQUENCY
(Monaurai)

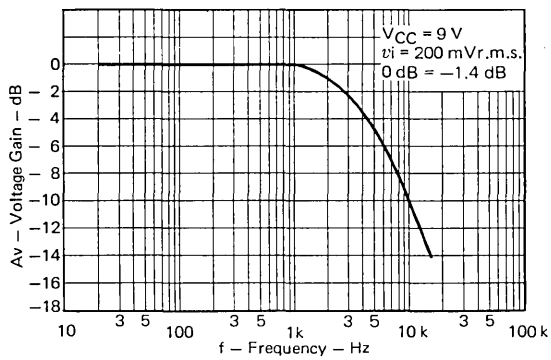


Fig.20 SEPARATION vs. FREQUENCY
(Stereo)

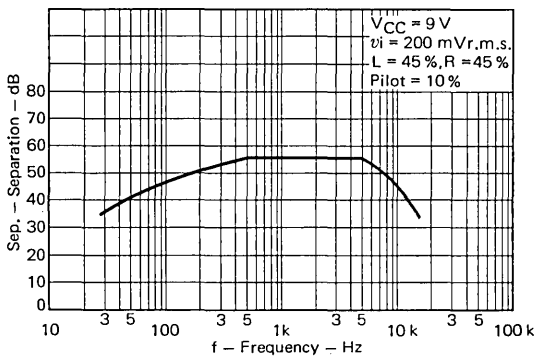


Fig.21 VCO FREE RUNNING FREQUENCY vs. SUPPLY VOLTAGE

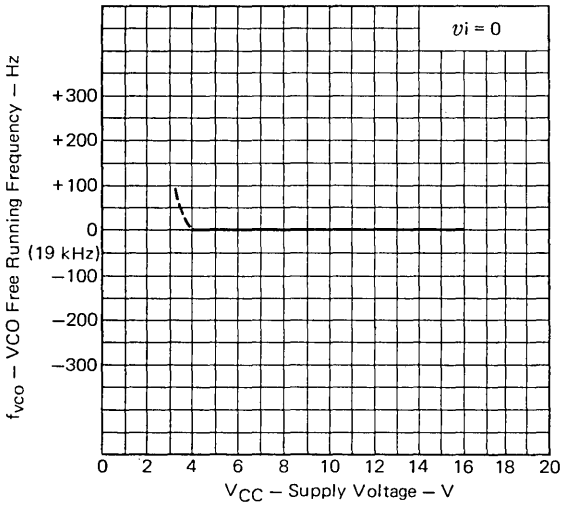


Fig.22 SEPARATION vs. PILOT INPUT LEVEL (Stereo)

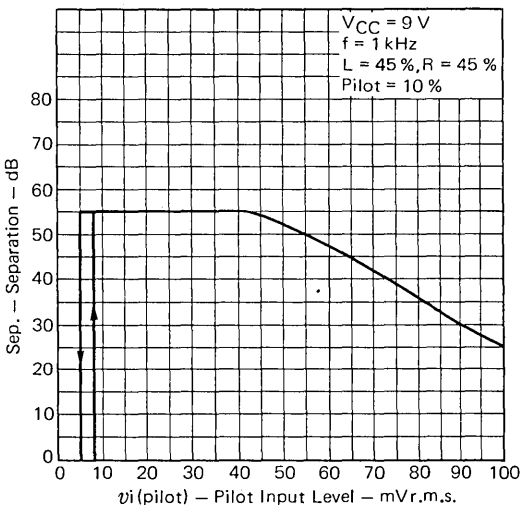


Fig.23 TOTAL HARMONIC DISTORTION vs. SIGNAL INPUT LEVEL (Monaural)

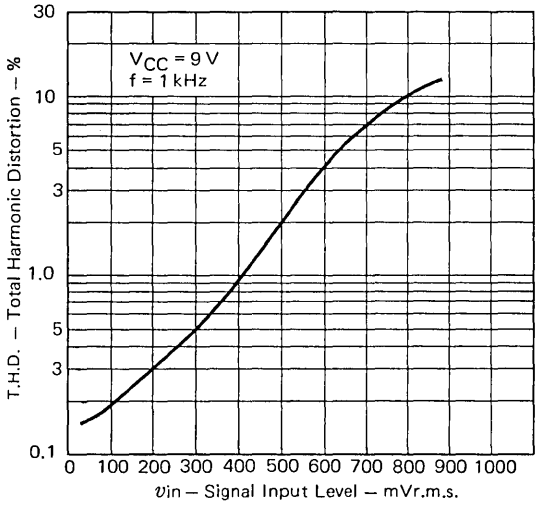


Fig.24 TOTAL HARMONIC DISTORTION vs. SUPPLY VOLTAGE (Monaural)

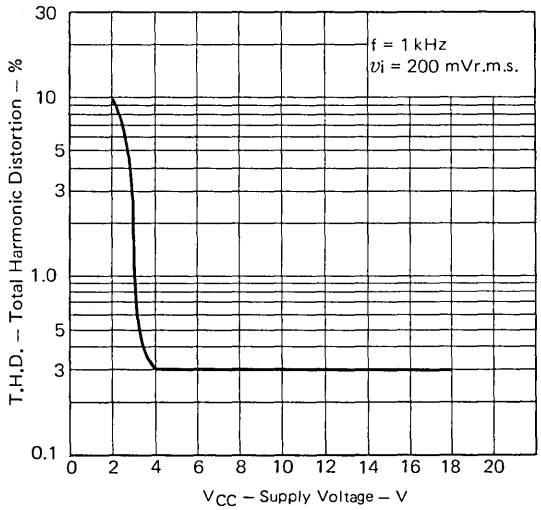


Fig.25 TOTAL HARMONIC DISTORTION vs. FREQUENCY (Monaural)

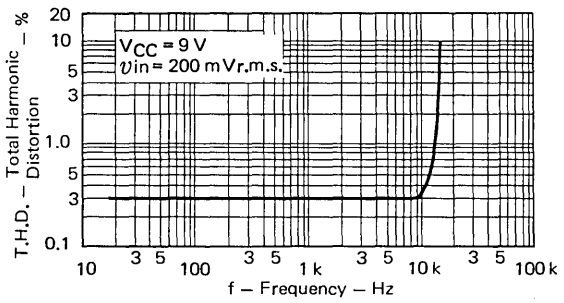


Fig.26 TOTAL HARMONIC DISTORTION vs. FREQUENCY (Stereo)

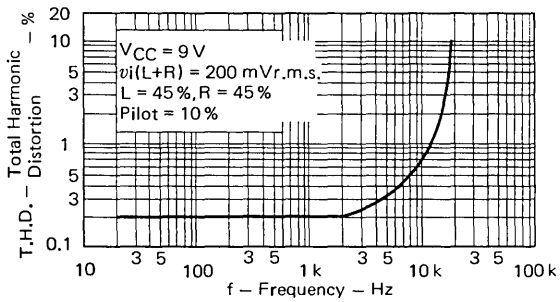


Fig.27 TOTAL HARMONIC DISTORTION vs. PILOT INPUT LEVEL (Stereo)

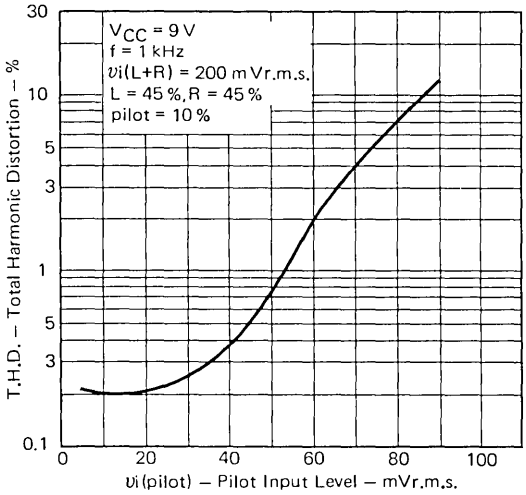


Fig.28 MAXIMUM INPUT LEVEL vs. SUPPLY VOLTAGE (Monaural)

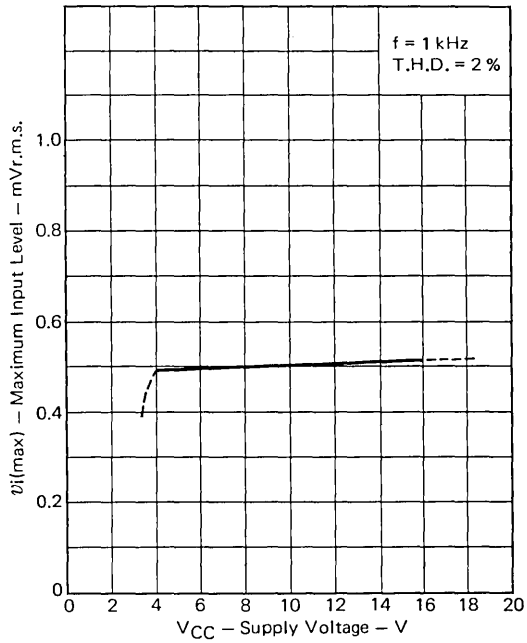


Fig.29 CAPTURE RANGE

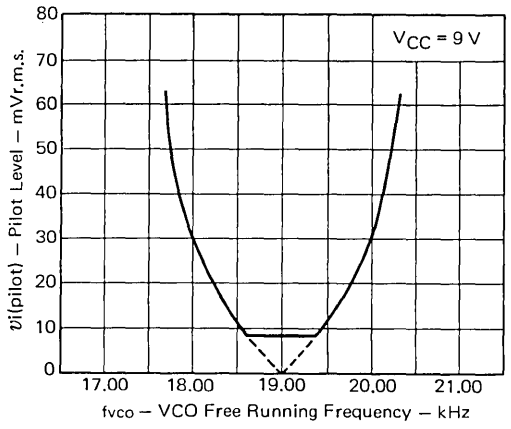


Fig.30 POWER DISSIPATION AND SATURATION VOLTAGE OF LAMP DRIVER vs. LAMP CURRENT

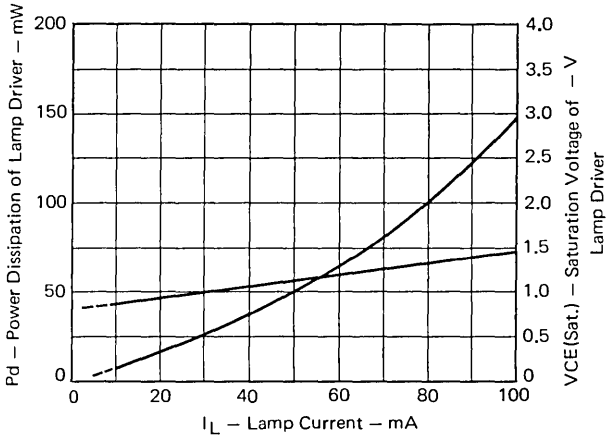


Fig.31 VCO FREE RUNNING FREQUENCY vs. AMBIENT TEMPERATURE

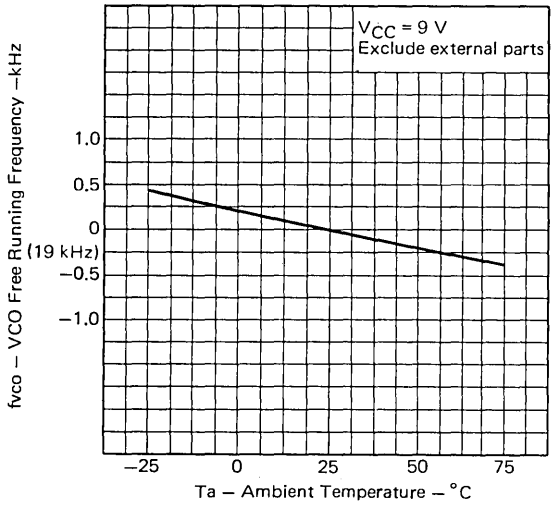


Fig.32 VCO FREE RUNNING FREQUENCY vs. AMBIENT TEMPERATURE

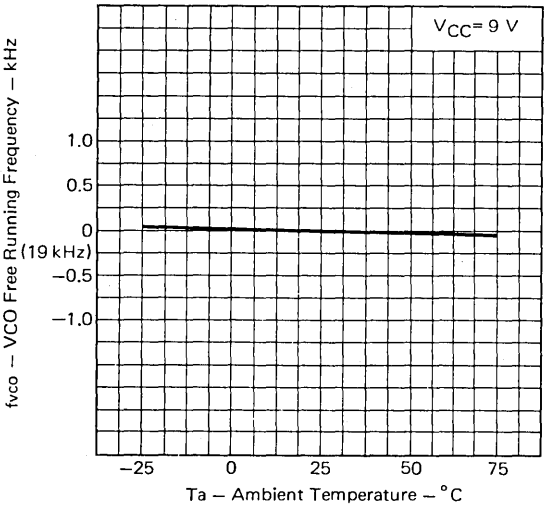


Fig.33 INPUT PILOT LEVEL (LAMP ON – OFF) vs. AMBIENT TEMPERATURE

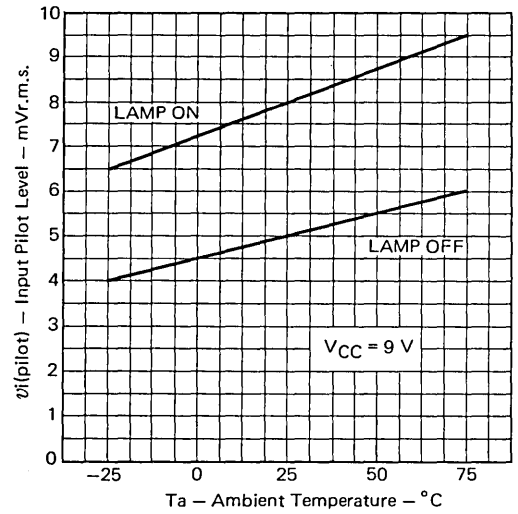
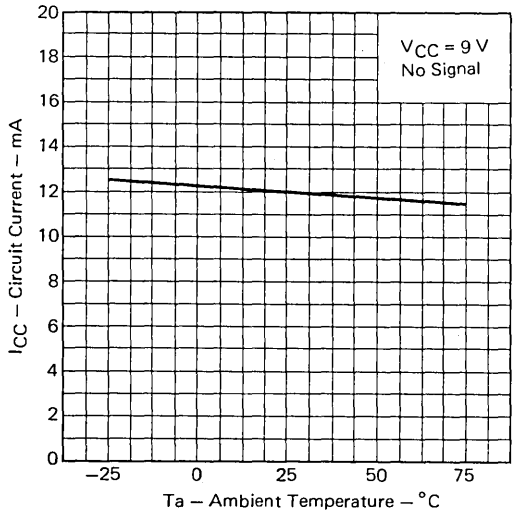


Fig.34 CIRCUIT CURRENT vs. AMBIENT TEMPERATURE



APPLICATION NOTE FOR μPC1277H
EXTERNAL PARTS AND CHARACTERISTICS

1 INTRODUCTION

μPC1277H is a dual channel audio power amplifier circuit designed for radio cassette tape recorders. It operates in the power supply voltage range of 5 to 16 V and can be used for a variety of stereo radio cassette sets.

This document explains how μPC1277H's external parts change its characteristics.

2 BLOCK DIAGRAM

Figure 1 briefly shows external parts and their effect upon characteristics using a block diagram.

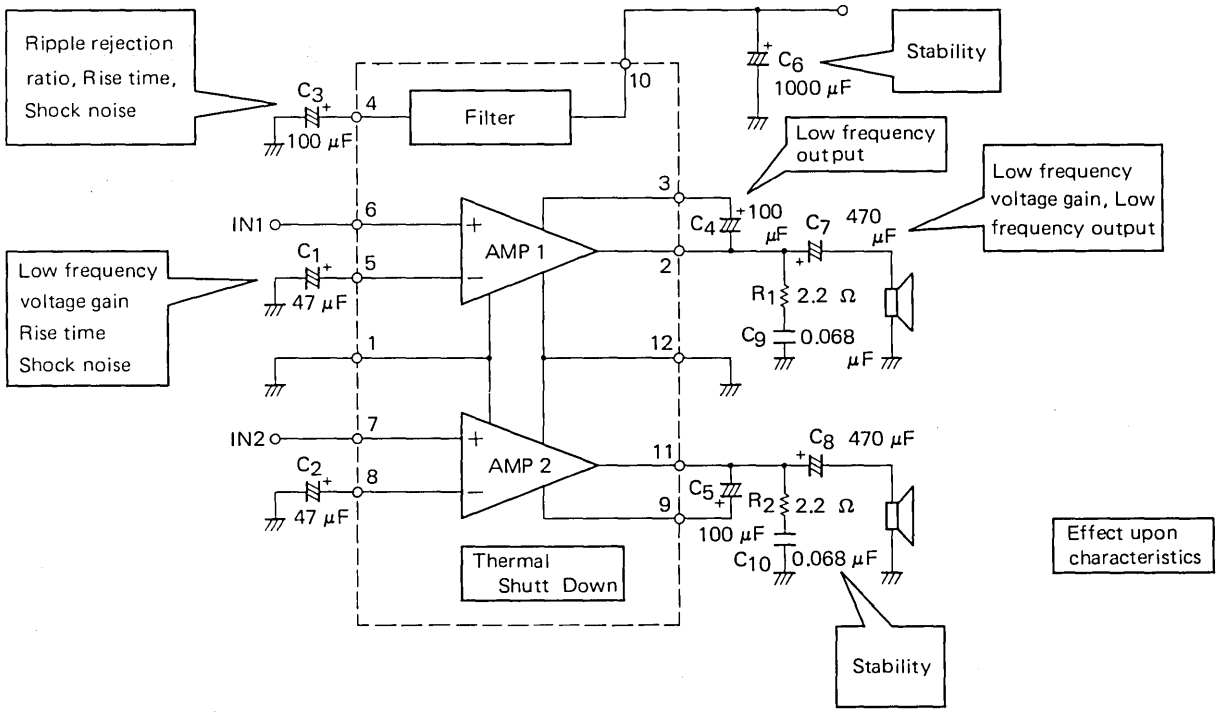


Fig. 1 Block diagram

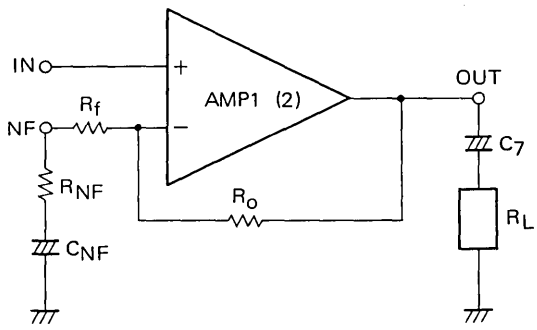
3 VOLTAGE GAIN

μPC1277H has a built-in resistor for setting the closed loop voltage gain as shown in the figure right. Add a resistor between the feed back terminal and ground when it is used with a lower voltage gain. Then, the voltage gain is obtained by the following equation:

$$G_V = \frac{G_{VO}}{1 + A_{VO}(R_f + R_{NF})/R_O}$$

A_{VO} ; Open loop voltage gain 65 dB (TYP.)

R_O=22 kΩ (TYP.) R_f=100 Ω (TYP.)



In a low frequency, impedance of C_{NF} (C_1 and C_2 in the block diagram) and that of the output coupling capacitor, C_7 (C_8) become not negligible. Figures 2 and 3 show voltage gain vs. frequency characteristics when C_1 (C_2) and C_7 (C_8) are changed.

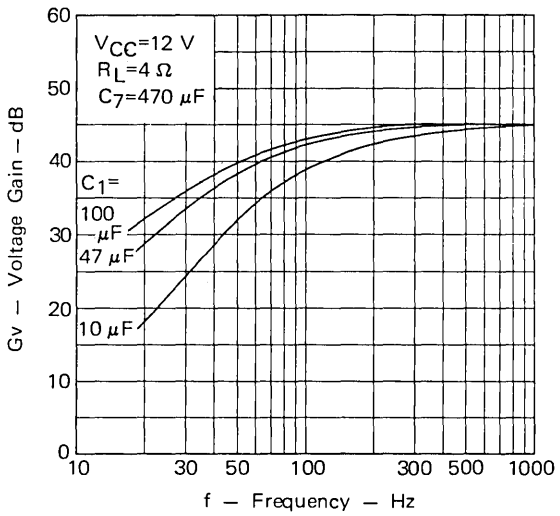


Fig. 2 VOLTAGE GAIN vs. FREQUENCY

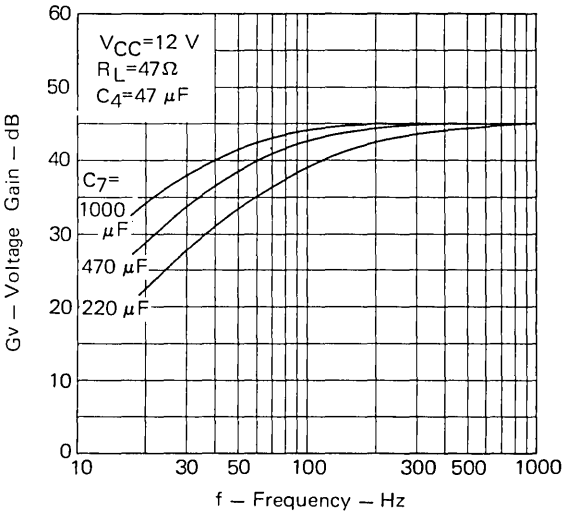


Fig. 3 VOLTAGE GAIN vs. FREQUENCY

4 OUTPUT POWER

Output power is effected by bootstrap capacitor C4 (C5) and output coupling capacitor C7(C8).

By the bootstrap circuit, whose configuration is shown in the figure right, the output voltage is feed back to the driver stage resulting that:

v_o (MAX.)=$V_{CC} - V_{CE(Q2)}$

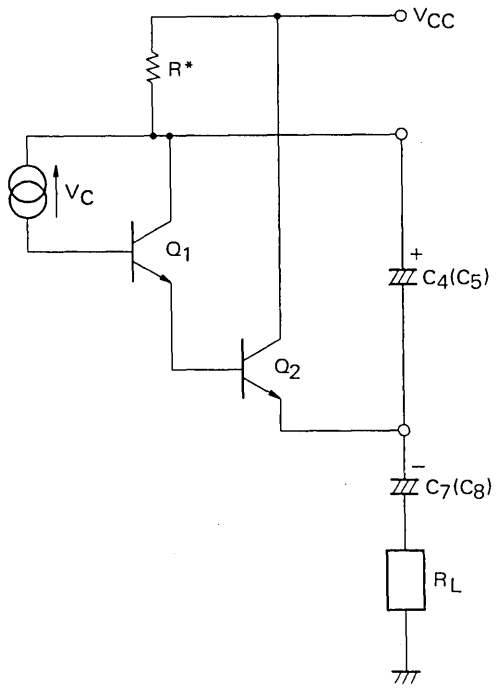
Removing C_4 (C_5) results in:

v_o(MAX.)=$V_{CC} - V_{BE(Q2)}+V_{BEQ1}+V_C+V_{(R*)}$

to limit the output amplitude and high output cannot be obtained.

When impedance of output capacitor C_7 (C_8) becomes not negligible, the load current becomes smaller by an amount corresponding to that impedance and small output is resulted.

Figure 4 shows output power vs. frequency characteristics when C_4 and C_7 are changed.



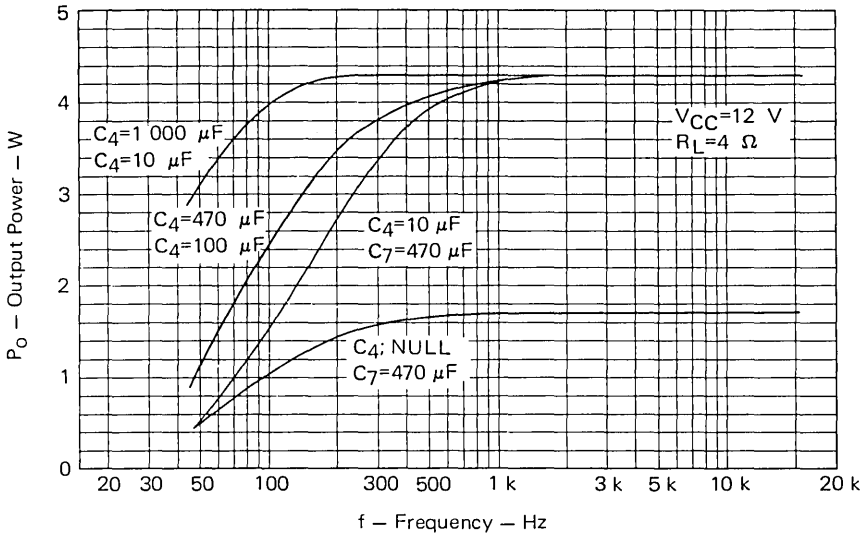
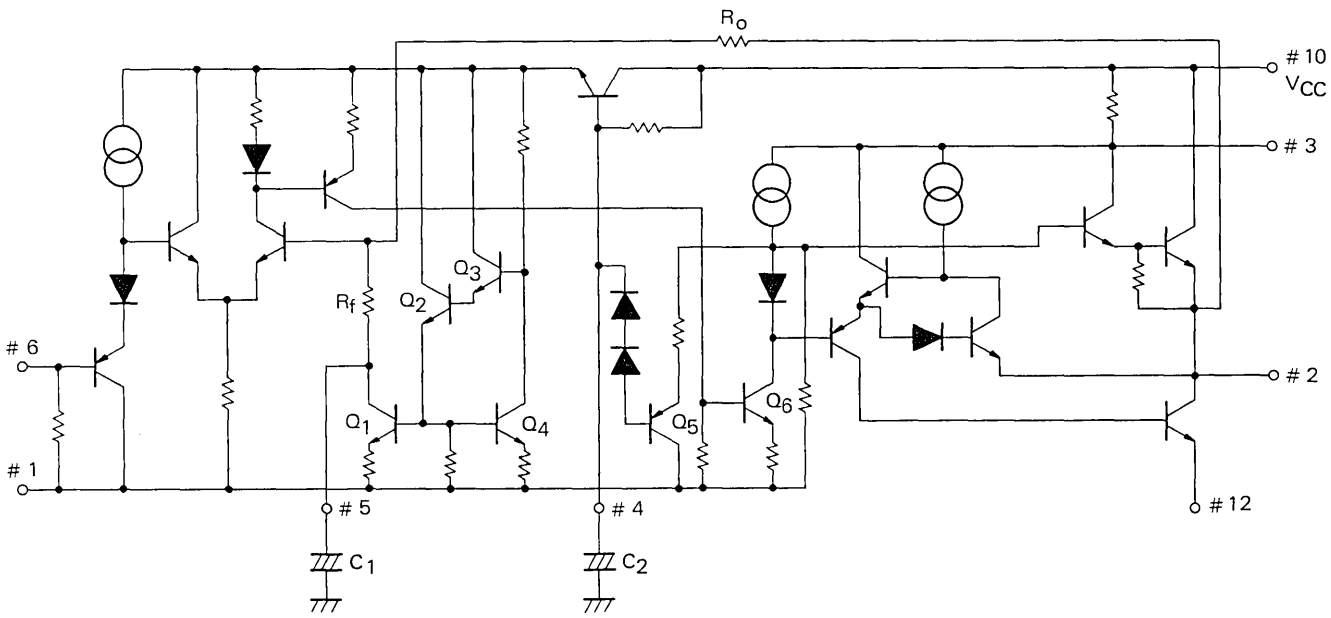


Fig. 4 OUTPUT POWER vs. FREQUENCY

5 SHOCK NOISE AND RISE UP TIME



The figure shown above is a part of the equivalent circuit of μPC1277H. The transient phenomenon occuring when power on is explained using this figure.

When the power supply voltage is applied, the input side of the differential amplifier circuit is biased to result driving the upper output transistor and to boost the output voltage. On the other hand, the voltage of C_3 is low because its charging time constant is large and transistor Q_5 is turned on. At this time, output voltage V_O becomes nearly $V_{(C3)} + V_{BE}$ to follow gentle rise up of C_3.

In the meantime, capacitor C_1 is charged by the output voltage via resistors R_f and R_O. When both base voltages of the differential amplifier circuit become equal, driving of the upper output transistor is weakened by function of predriver Q_6 and the ouput voltage is set to about $\frac{1}{2}V_{(C3)}$ by the bias circuit (transistor Q_1 to Q_4).

Because C_3 is not yet charged fully with the value of C_3 recommended for μPC1277H, the output voltage keeps going up for a while. When C_3 is fully charged and it becomes nearly V_{CC}. the output voltage is settled to $\frac{1}{2}V_{CC}$.

Therefore, the shock noise is small enough in comparison with conventional Cs.

Figures 5 and 6 show changes of the output voltage with changes of C_1 and C_3.

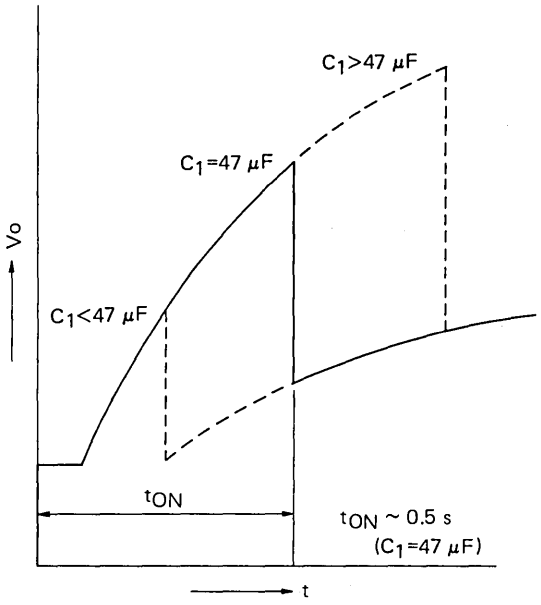


Fig. 5 C_1 AND RISE UP TIME

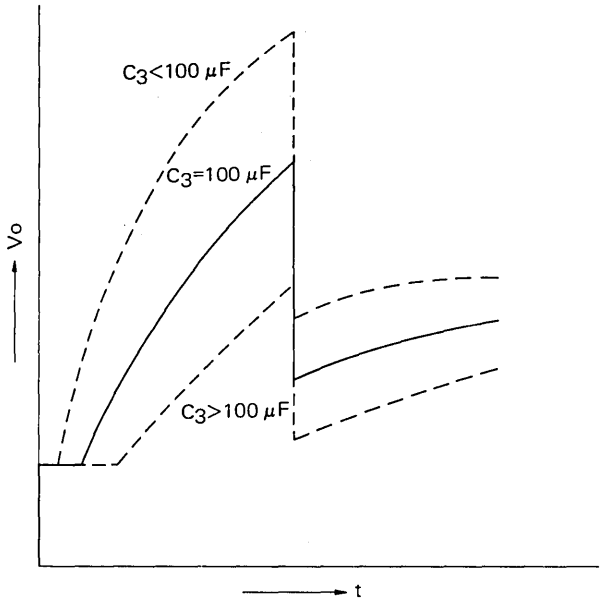


Fig. 6 C_3 AND RISE UP TIME

6 OTHERS

- Power decoupling capacitor C_6, oscillation preventing capacitor and resistor are provided so that μPC1277H has stable operations in wide ranges of voltage, 5 to 16 V temperature, −20 to +75 °C, and load, 3 to 8 Ω.
- Filter capacitor C_3 is provided to reduce the ripple voltage occuring in AC power supply . Also, gentle rise up of this capacitor is, as set forth earlier, utilized to minimize the shock noise.

μPC1350C EXAMPLE OF APPLICATION CIRCUIT WITH 4 Ω LOAD AND 0.7 W OUTPUT

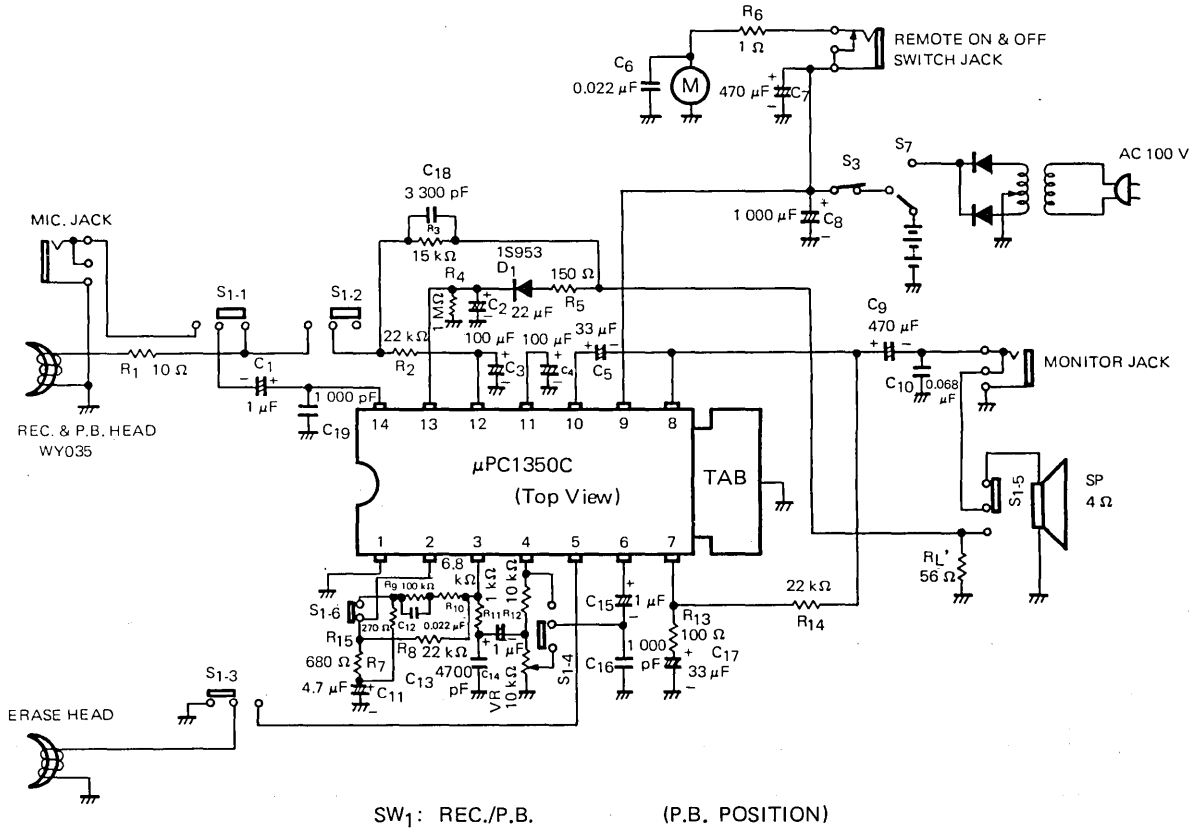
DESCRIPTION

μPC1350C is a silicon monolithic integrated circuit developed for uses in cassette tape recorders. The standard operating condition is 6 V power supply and 8 Ω load. This IC includes functions of a preamplifier, automatic level control (ALC) circuit, and ITL and OTL power amplifiers. One piece of this IC enables to construct the amplifier unit of a tape recorder.

This document shows one example of an application circuit with 4 Ω load.

1. EXAMPLE OF APPLICATION CIRCUIT

Figure 1 shows an application circuit example when used for 4 Ω load.



SW1: REC./P.B. (P.B. POSITION)
SW2: AC/DC OPERATION (DC OPERATION)
SW3: Power Switch (ON POSITION)

Fig. 1 EXAMPLE OF APPLICATION CIRCUIT

2. ELECTRICAL CHARACTERISTICS

2-1. ABSOLUTE MAXIMUM RATINGS AND RECOMMENDED OPERATING CONDITIONS

Absolute Maximum Ratings (T_a=25 °C)

Item	Symbol	Rating	Unit
Supply Voltage (D.C.)	V_{CC1}	12	V
Supply Voltage (A.C.)	V_{CC2}	10	V
Circuit Current	$I_{CC(peak)}$	500	mW
Power Dissipation	P_D	2.4 *	W
Operating Temperature	T_{opt}	−20 ~ +75	°C
Storage Temperature	T_{stg}	−40 ~ +150	°C

*Copper heat sink of 50 mm x 50 mm x 1.5 mm

Recommended Operating Condition (T_a=25 °C)

Item	MIN.	TYP.	MAX.	Unit
Supply Voltage	3.5	6	7.5	V

2-2. OUTPUT POWER

μPC1350C is designed for a tape recorder and it gives standard output of 0.7 W when its load is 4 Ω (V_{CC}=6 V, T.H.D.=10 %). Fig. 2 shows output power vs. supply voltage characteristic.

2-3. POWER DISSIPATION

Fig. 3 shows power dissipation vs. output power characteristics. Refer to this characteristic for thermal designing.

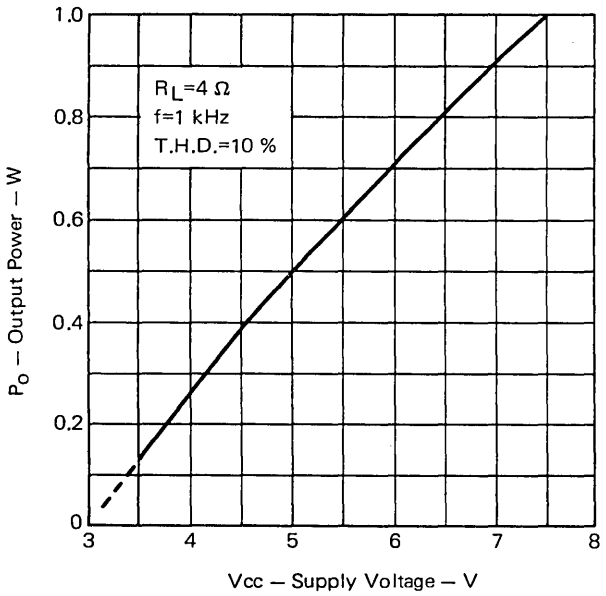


Fig. 2 OUTPUT POWER vs. SUPPLY VOLTAGE

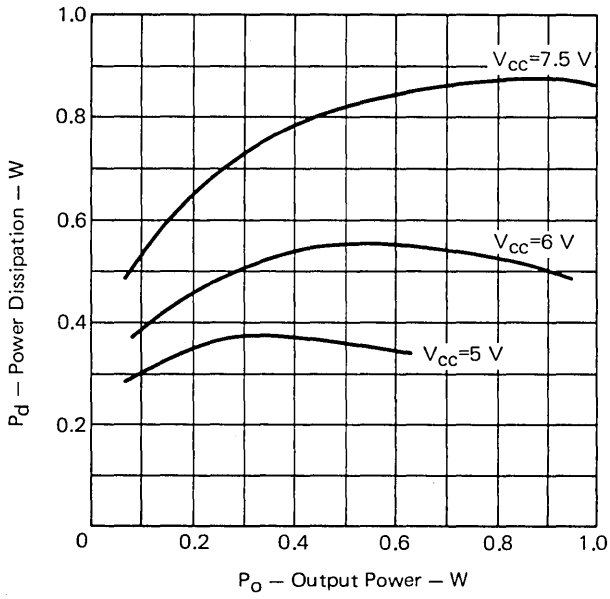


Fig. 3 POWER DISSIPATION vs. OUTPUT POWER

2-4. VOLTAGE GAIN

In μPC1350C, its pre-amp. stage gain and power amp. stage gain approximate following equations:

(A) Pre-amp. stage

$$G_{v1} \simeq \frac{R_8}{R_7} \quad \text{(Used as a FLAT Amp.)}$$

$$G_{v1} \simeq \frac{1}{R_{15}} \sqrt{R_{10}^2 + \left(\frac{R_9 + R_{10}}{\omega C_{12} R_9} \right)^2}_{\omega = 2\pi f}$$

(Used as an NAB EQ. Amp.)

(B) Power amp. stage

$$G_{v2} \simeq \frac{R_{14}}{R_{13}}$$

Using the constants of the application circuit example shown in Fig. 1, the voltage gains are 30.8 dB (FLAT), 30.2 dB (NAB EQ. at 1 kHz), and 46.8 dB (power amp. stage) respectively. The low frequency characteristics are determined by time constants of R_7, C_{11}, R_{13}, and C_{17} in the feed back circuit and C_9 and R_L in the output circuit. Namely, low cut-off frequencies f_{L1}, f_{L2}, and f_{L3} are represented by following equations:

$$f_{L1} = \frac{1}{2\pi C_{11} \cdot R_7}$$

$$f_{L2} = \frac{1}{2\pi C_{17} \cdot R_{13}}$$

and

$$f_{L3} = \frac{1}{2\pi C_9 \cdot R_L}$$

In the example of the application circuit shown in Fig. 1, $f_{L1} \simeq 50$ Hz, $f_{L2} \simeq 48$ Hz, and $f_{L3} \simeq 85$ Hz. Overall voltage again versus frequency characteristics are shown in Fig. 4 when used as an NAB. EQ. Amp., and in Fig. 5 when as a FLAT Amp.

2-5. TOTAL HARMONIC DISTORTION

Fig. 6 shows the total harmonic distortion vs. output power characteristic and Fig. 7, the total harmonic distortion vs. frequency characteristic. This IC is designed to have a low total harmonic distortion factor and it is most appropriate for use in tape recorders.

2-6. ALC CHARACTERISTICS

Fig. 8 shows ALC output change vs. input level characteristics and Fig. 9, ALC output distortion factor vs. input level characteristics. It gives ALC range (wherein distortion factor is 3 % or below) of 60 dB

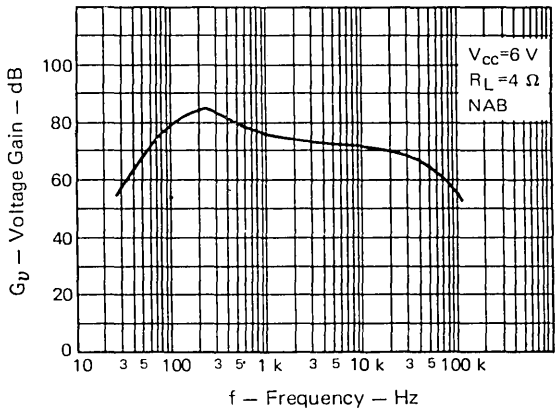


Fig. 4 VOLTAGE GAIN vs. FREQUENCY

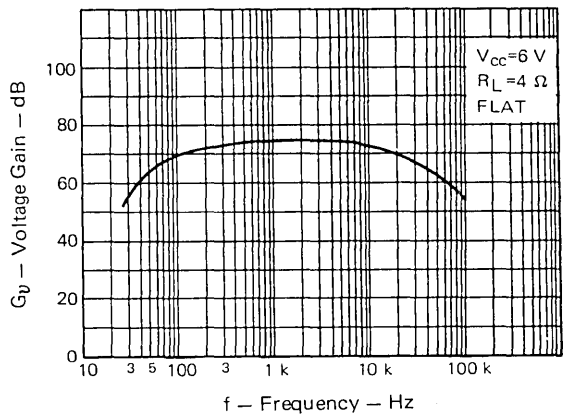


Fig. 5 VOLTAGE GAIN vs. FREQUENCY

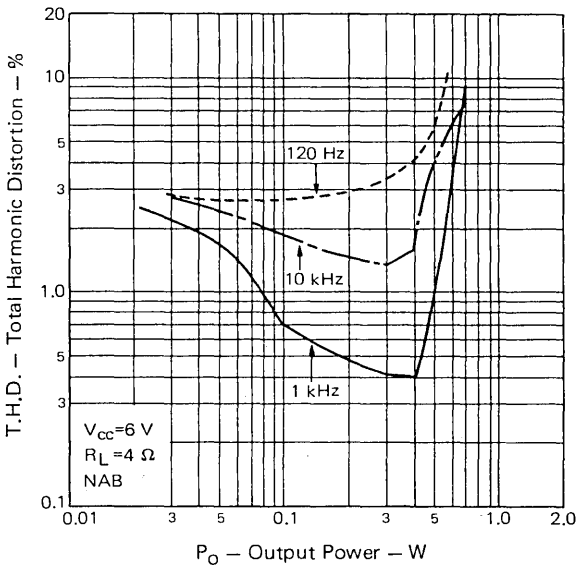


Fig. 6 TOTAL HARMONIC DISTORTION vs. OUTPUT POWER

(TYP.) and output change (difference of outputs between input levels of −70 and −40 dBm) of 1.8 dB (TYP.) when V_{CC}=6 V and R_L=56 Ω.

2-7. TEMPERATURE CHARACTERISTICS

Fig. 10 shows the overall voltage gain, power output, and circuit current vs. ambient temperature characteristics and Fig. 11 shows the total harmonic distortion vs. ambient temperature characteristics. All these characteristics show stable operations.

3. HEAT SINK DESIGN

In heat sink design, refer to Fig. 3, power dissipation vs. output power characteristics, and Fig. 12, power dissipation vs. ambient temperature characteristics. The relationship between junction temperature T_j and power dissipation P_d is represented by the following equation:

$$T_j = R_{th\ (j-a)} \cdot P_d + T_a$$

where: $R_{th(j-a)}$: thermal resistance between junction and ambience

T_a: ambient temperature

T_j: junction temperature

An example: when mounted on a printed circuit board with copper heat sink (50x50x0.035 mm) and used under V_{CC}=7.5 V, R_L=4 Ω, and ambient temperature 25 °C, P_d max.=0.88 W, as shown in Fig. 3, and $R_{th(j-a)}$=55 °C/W, in Fig. 12. Substituting these values in the equation to obtain the junction temperature, $T_j \simeq 72$ °C is given. If a lower junction temperature is desired, make the area of the printed circuit board with copper heat sink on TAB part wider, or make the area of the print board itself larger to reduce $R_{th(j-a)}$. Thus the junction temperature can be lowered.

Note

$R_{th(j-a)}$ = 90 °C/W : Free Air

$R_{th(j-a)}$ = 65 °C/W : 30x30x1.5 mm with copper heat sink

$R_{th(j-a)}$ = 55 °C/W : 50x50x1.5 mm with copper heat sink

$R_{th(j-a)}$ = 50 °C/W : infinitely large heat sink

Unit : mm

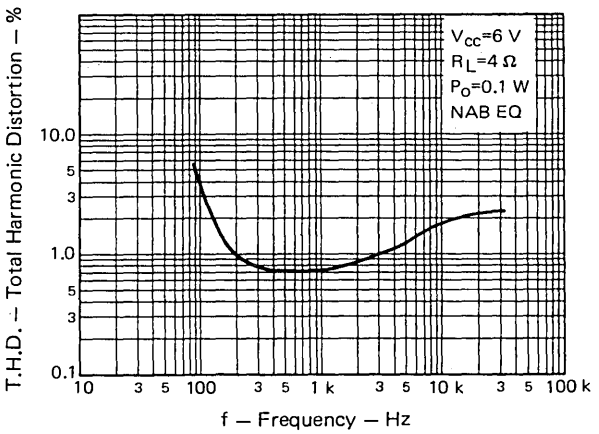


Fig. 7 TOTAL HARMONIC DISTORTION vs. FREQUENCY

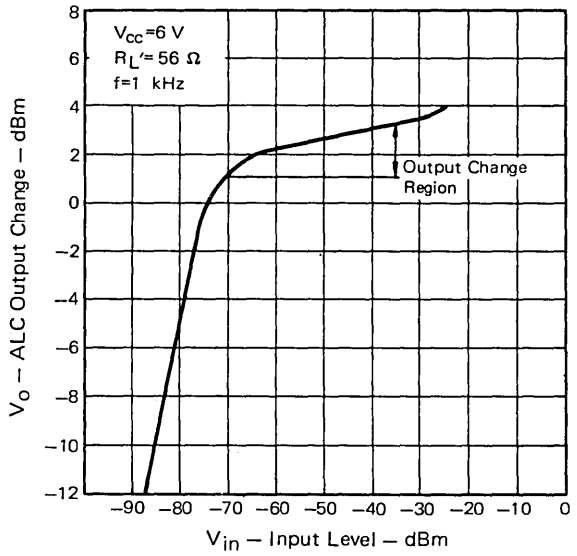


Fig. 8 ALC OUTPUT CHANGE vs. INPUT LEVEL

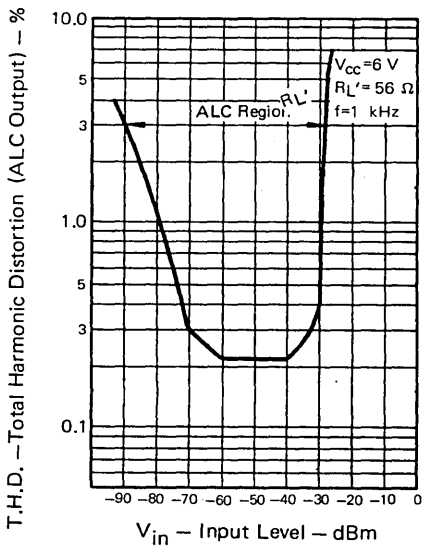


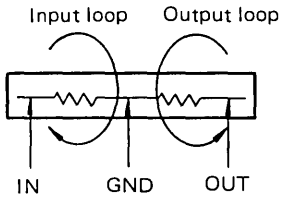
Fig. 9 TOTAL HARMONIC DISTORTION (ALC OUTPUT) vs. INPUT LEVEL

4. NOTICES ON DESIGNING PRINTED CIRCUIT BOARD

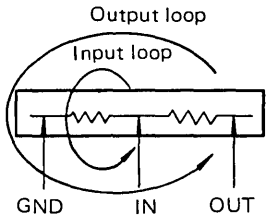
(1) Since μPC1350 is a high gain amplifier, design power supply and grounding wires thick to highten circuit stability.

(2) Although one point grounding is ideal, when it is impossible to realize, take care that the input loop does not come into the output loop. Mingled input and output loops may cause deterioration of the distortion factor and oscillation.

(Good example)



(Bad example)



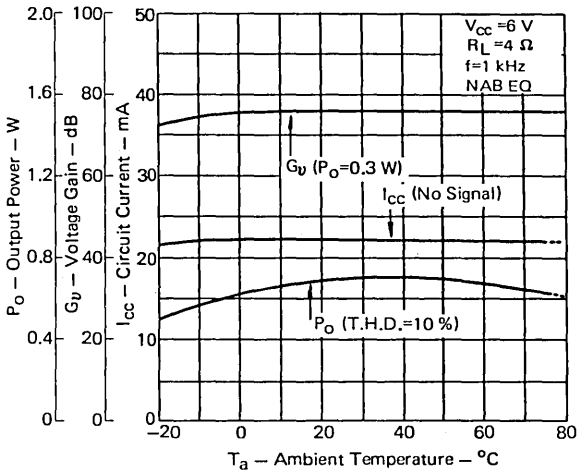


Fig. 10 OUTPUT POWER, VOLTAGE GAIN AND CIRCUIT CURRENT vs. AMBIENT TEMPERATURE

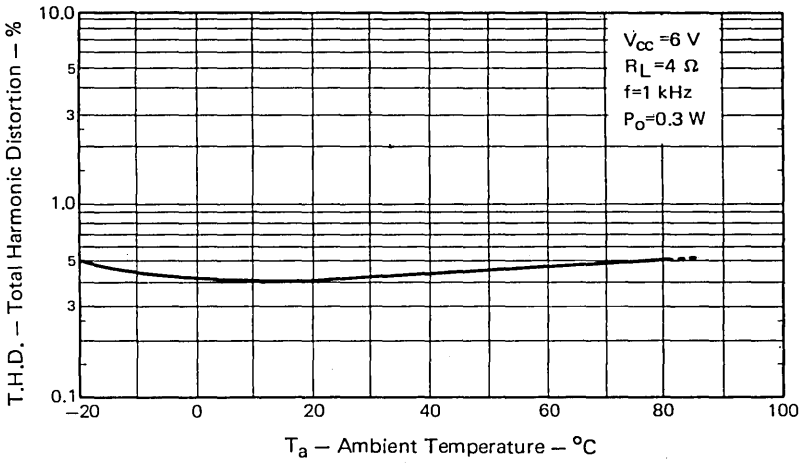


Fig. 11 TOTAL HARMONIC DISTORTION vs. AMBIENT TEMPERATURE

(3) Mount C_8: 1 000 μF (for bypass), C_{10}: 0.06 μF (output oscillation preventing capacitor), and the speaker terminal close to TABpin (GND).

(4) Fig. 13 shows the example of a printed circuit board.

5. CAUTIONS ON HANDLING

(1) Output oscillation preventing capacitor C_{10}:0.068 μF

This capacitor is for preventing oscillation on the power amp. stage. Select the type of this capacitor according to the set in which μPC1350C is used.

(A) When used for a cassette tape recorder:

Use a ceramic capacitor or Mylar capacitor for C_{10}.

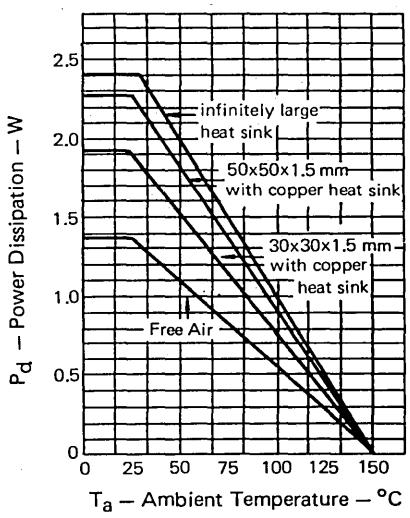


Fig. 12 POWER DISSIPATION vs. AMBIENT TEMPERATURE

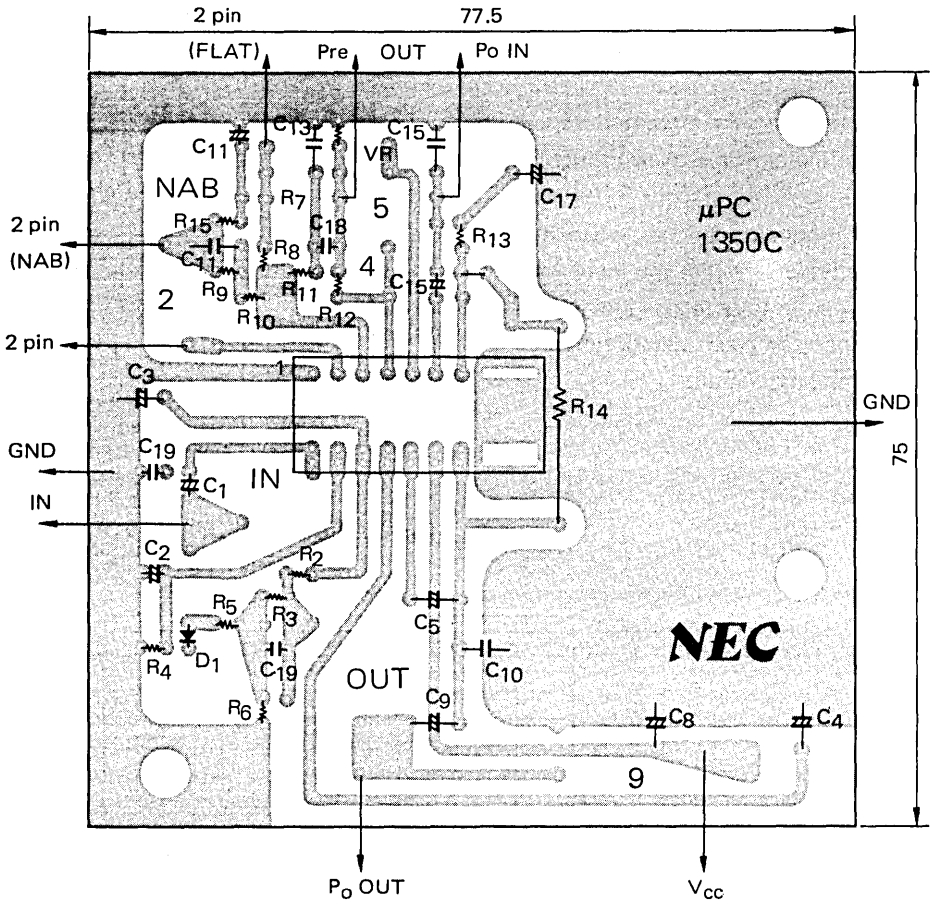


Fig. 13 PRINTED CIRCUIT BOARD

(B) When used for radio cassette tape recorders: Use a Mylar capacitor for C_{10}. If a ceramic capacitor is used, unnecessary radiation emitted from the capacitor may return to the RF stage of the radio.

(2) Recovery time during recording

Recovery time is determined by the time constant of the circuit in which capacitor C_2, input resistor to IC's 13th terminal, and R_4 are connected in parallel and is changed by varying R_4: 1 MΩ.

(3) TAB

Since TAB of μPC1350C is GND within the IC, be sure to solder it to GND of the printed circuit board.

(4) Bias terminals

The 5th terminal of μPC1350C is the DC bias terminal for the erasing head and the 12th terminal is the DC bias terminal for the recording head.

(5) When the power amp. stage only is used.

In that case, connect the input terminal (13th terminal) of the pre-amp. stage to GND through a capacitor. If the input terminal of the pre-amp. stage is left open, oscillation may occur to worsen the power amp. stage characteristics.

The 4 Ω load application circuit of μPC1350C is explained in the preceding sections. Besides what are set forth there, this IC is designed so that it has low output shock noise at power on/off and it is durable against electrostatic breakdown. Therefore, this IC can fully be used as an amplifier for a cassette tape recorder.

APPLICATION CIRCUIT OF μPD1701C-013

DESCRIPTION

The μPD1701C-013 is a CMOS LSI designed for use in Phase Locked Loop Frequency Synthesizer Digital Tuning System, which consists of PLL, swallow counter and system controller.
The μPD1701C-013 provides full electronic control of varactor tuned FM/AM radio receiver with clock function. NEC's original pulse swallowing method is applied to FM band in conjunction with μPB553AC, so that high reference frequency results in good signal-to-noise ratio. The μPB553AC is a VHF two-modulus prescaler which provides 1/16 and 1/17 division ratio. Advanced bipolar process technology is utilized to realize high frequency operation with extremely low power consumptions.

FEATURES

- PLL, swallow counter and system controller are realized in a single chip.
- Occupation of minimum mounting area in P.C. Board due to 28 pin slim DIP.
- High speed and low power consumptions due to CMOS.
- Very low stand-by current . . . . . I_{DD}=0.5 mA (TYP.)
- Single power supply voltage . . . . . V_{DD}=5.0 V ± 10 %
- FM and AM bands . . . . . Japan and U.S. bands
- External programmable IF offset for FM band.
  - Japan band . . . . . 10.675, 10.700, 10.725, 10.750 MHz
  - U.S. band . . . . . 10.650, 10.675, 10.700, 10.725 MHz
- External programmable IF offset for AM band.
  - Japan band . . . . . 450/261 kHz
  - U. S. band . . . . . 450/260 kHz or 450/261 kHz
- High reference frequency. It results in good signal-to-noise ratio.
  - FM band . . . . . 25 kHz
  - AM band . . . . . 10 kHz or 9 kHz
- Four station selection modes are available.
  - (1) SCAN (Automatic audition) of available program.
  - (2) SEEK (Automatic search and stop) for FM and AM.
  - (3) UP or DOWN manual tuning to any station by single stepping or sequencing with momentary switches or endless-rotary switch.
  - (4) Favorite station programming of 6 FM and 6 AM stations for pushbuttons selection.
- Ample time correction modes are available.
  - (1) Hour fast shift (HA key only or ME key and MD key)
  - (2) Minute fast shift (MA key only or ME key and MU key)
  - (3) One touch setting to correct time (0AD key: ±30 minutes zero reset)
- Two stage switching of display brightness (duty cycle : 25 %)
- Two independent frequency input terminals are provided for both FM and AM bands.
- Two independent error-out terminals are provided for both FM and AM bands.
- Direct interface to the FM two-modulus prescaler μPB553AC.
- Automatic power-on clear without any external components.
- Internal display decoder for 3.5 digit multiplexed display.

1. SYSTEM DESCRIPTION

NEC's Digital Tuning System provides full electronic control of a varactor tuned FM/AM radio receiver and stereo. The block diagram of the system is shown in Fig. 1. This is a Phase Locked Loop Digital Tuning System which consists of two integrated circuits; controller plus PLL in a single chip, and two-modulus prescaler.

The controller chip (μPD1701C-013) provides Phase Locked Loop capability with on-chip frequency division, a reference oscillator whose frequency is controlled by an external crystal of 4.5 MHz, and phase comparator circuitry. It accepts directly an AM local oscillator signal and an FM signal from two-modulus prescaler (μPB553AC), and outputs control signals for closed loop operation of these oscillators. The outputs drives filters for supplying analog voltages to the vari-cap tuners. The controller also provides the signals to drive the display. The frequency of the tuned station is displayed on a 3.5 digit multiplexed display. Six favorite stations on each band can be stored as well as "last stations tuned" information.

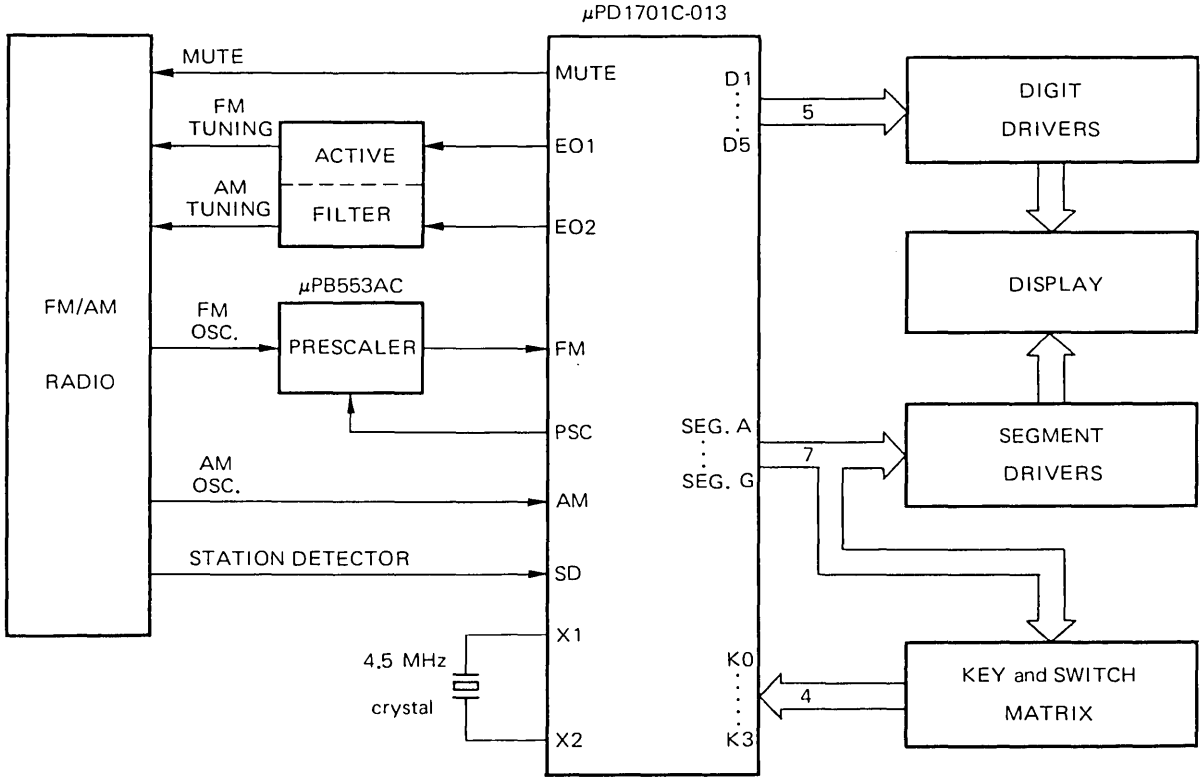


Fig. 1 Block Diagram

2. PIN CONNECTION (Top View)

The pin connection of the μPD1701C-013 is shown in Fig. 2.

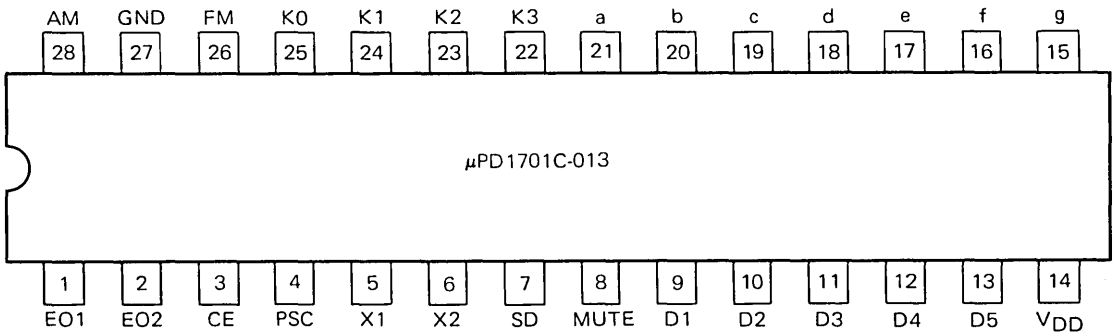


Fig. 2

3. CONTROL KEY AND MODE SWITCH MATRIX

The operation of the system is controlled by a 4 x 7 key and switch matrix (15 momentary switches, 5 alternate switches and 7 initial switches). Various functions are entered through the matrix. The configuration of the matrix is shown in Fig. 3.

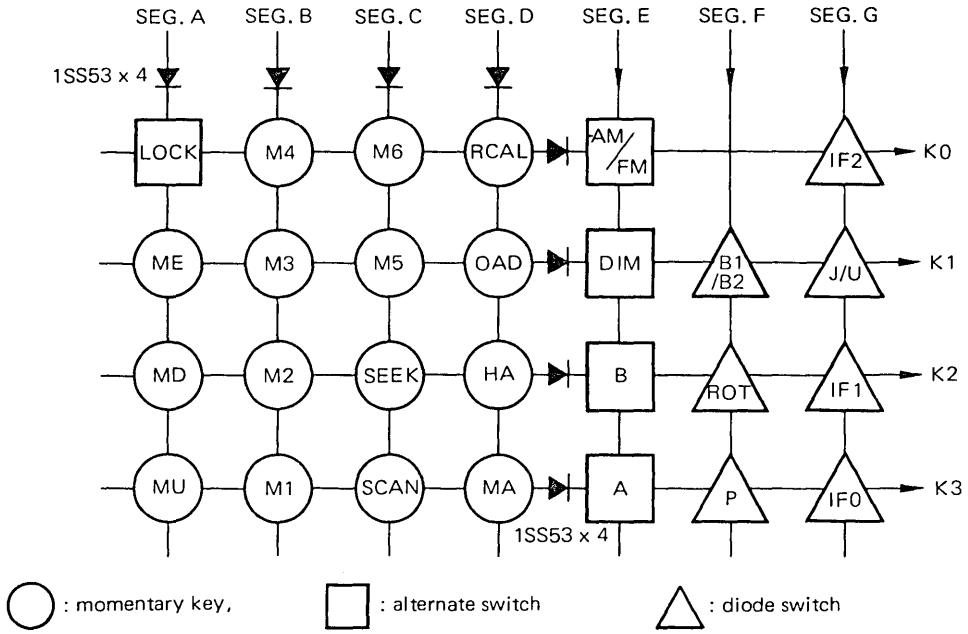


Fig. 3 Control Key and Mode Switch Matrix

4. SWITCHING-OVER THE DISPLAY BETWEEN RADIO AND CLOCK

Display mode control switches A, B, initial switch P and control key RCAL control the display mode as follows.

MODE	A	B	Display	Priority	Enable keys and switches
0	ON	ON	Frequency or time	None *1	All keys and switches
1	ON	OFF	Frequency or time	Frequency *2 or time	All keys and switches
2	OFF	OFF	Time only	–	HA, MA, and 0AD keys A, B, and DIM switches
3	OFF	ON	Disabled	–	A and B switches

*1 : A momentary depression of RCAL key causes alternate display change between frequency and time whenever it is performed. Whenever frequency is handled, frequency is displayed.

*2 : P=ON

Frequency is prior to time. A momentary depression of RCAL key causes alternative display change. When frequency is displayed, a momentary depression of RCAL key recalls time on the display and it remains there for 5 seconds. If any other key is handled when time is displayed, handling of one of the time setting keys (HA, MA and 0AD) keeps the time display, the display turns back to frequency automatically 5 seconds after the time setting is completed. Whenever frequency is handled, frequency is displayed.

P=OFF

Time is prior to frequency. A momentary depression of RCAL key causes alternative display change. When time is displayed, a depression of RCAL key or one of the frequency handling keys recalls frequency on the display for 5 seconds. After that, the display turns back to time automatically.

5. APPLICATION EXAMPLE OF A SWITCH AND B SWITCH

This section describes connection diagram of power supply source of radio unit, display drivers and control unit, and application example of A switch and B switch, and state diagram of each application example.

There are two kinds of applications. One kind of applications use DPDT (Dual Pole Dual Transfer) switches. The other one use DPTT (Dual Pole Triple Transfer) switches. One of two poles is used to control power supply source, and the other one is used to control A switch and B switch.

Each state of the state diagram is shown as follows.

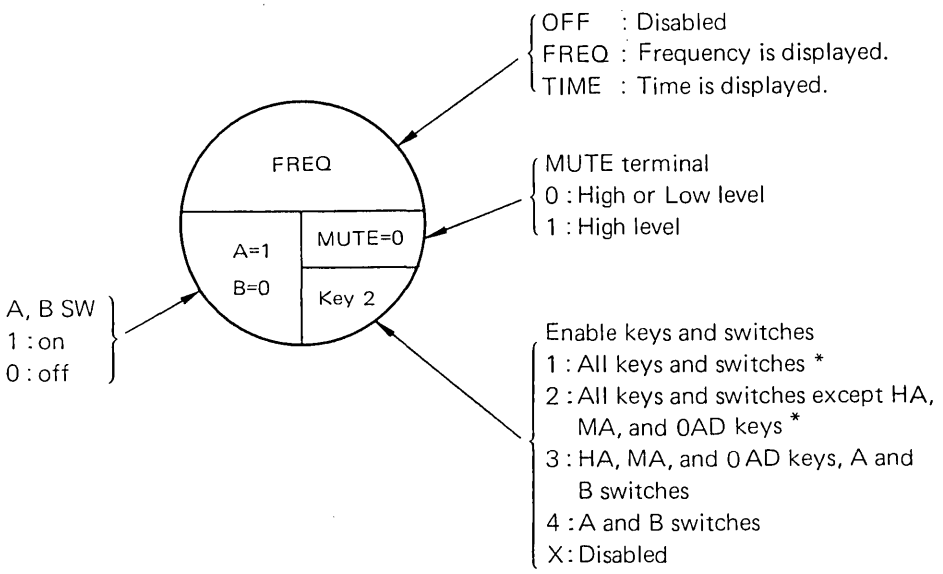


Fig. 4

* Except initial switches

Time display priority method–1 (Using DPDT SW)
Condition : B SW=off (OPEN)
P SW=off (OPEN)

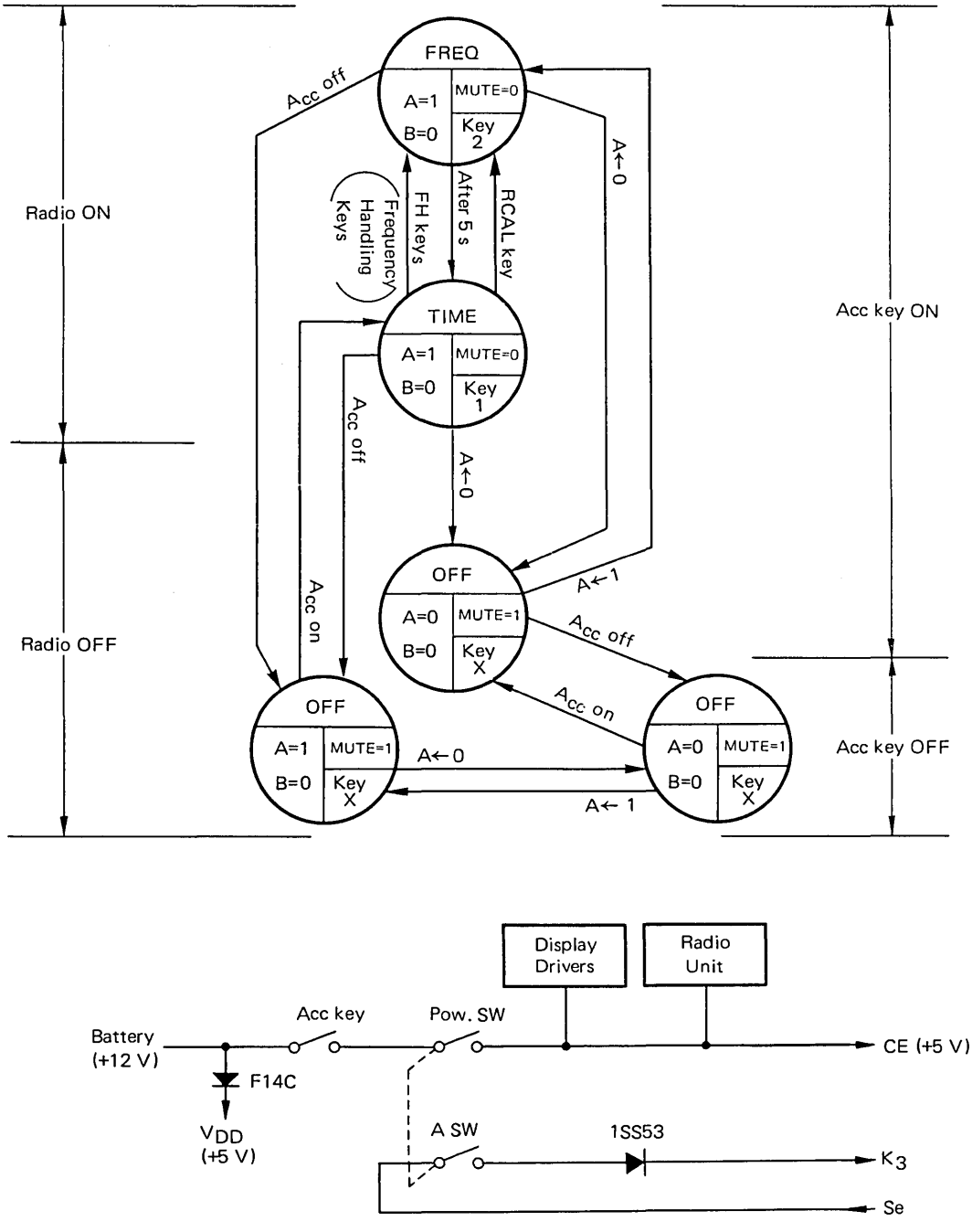


Fig. 5

Time display priority method–2 (Using DPDT SW)

Condition : B SW=off (OPEN)

P SW=off (OPEN)

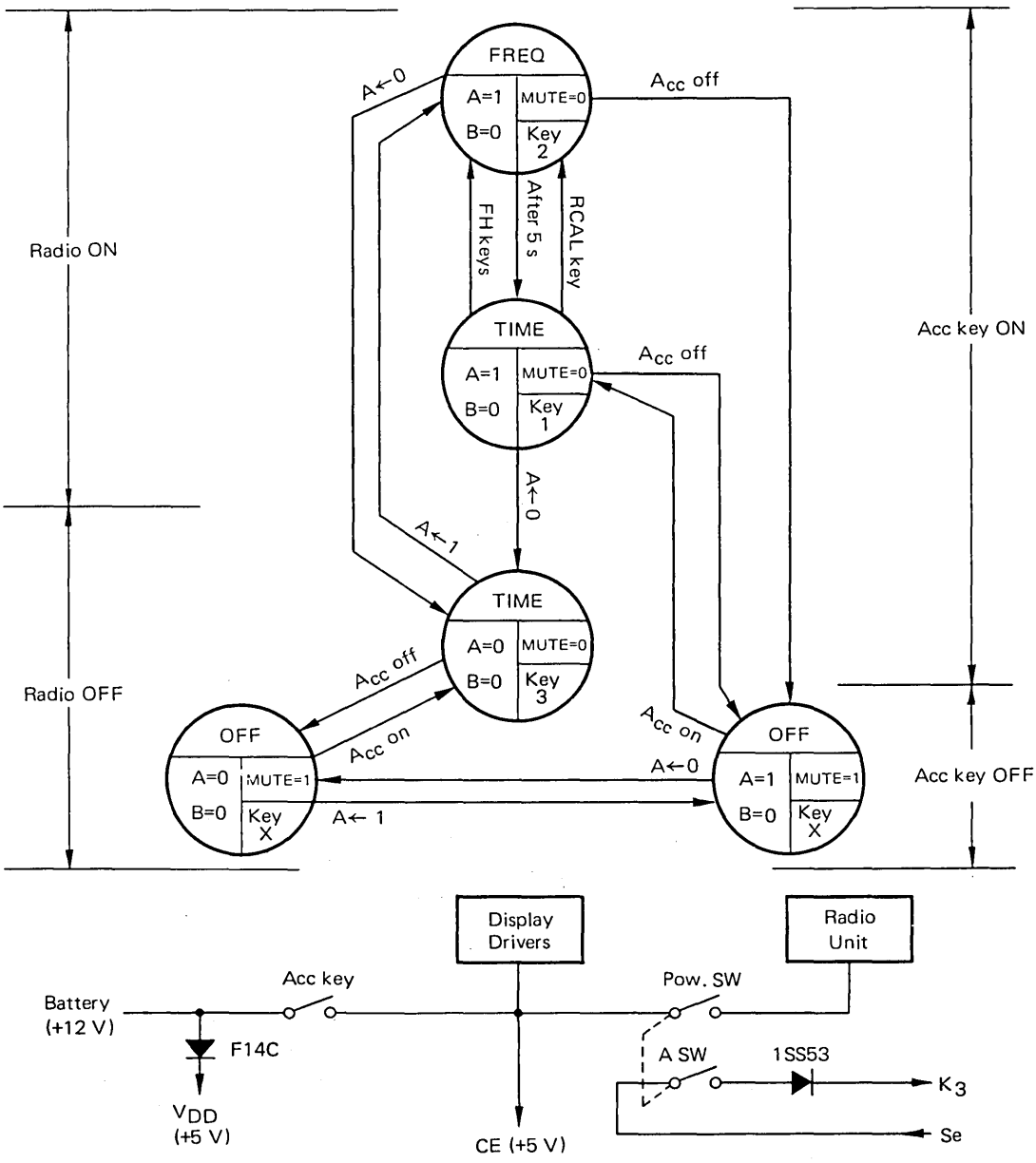


Fig. 6

Time display priority method–3 (Using DPTT SW)
Condition : P SW=off (OPEN)

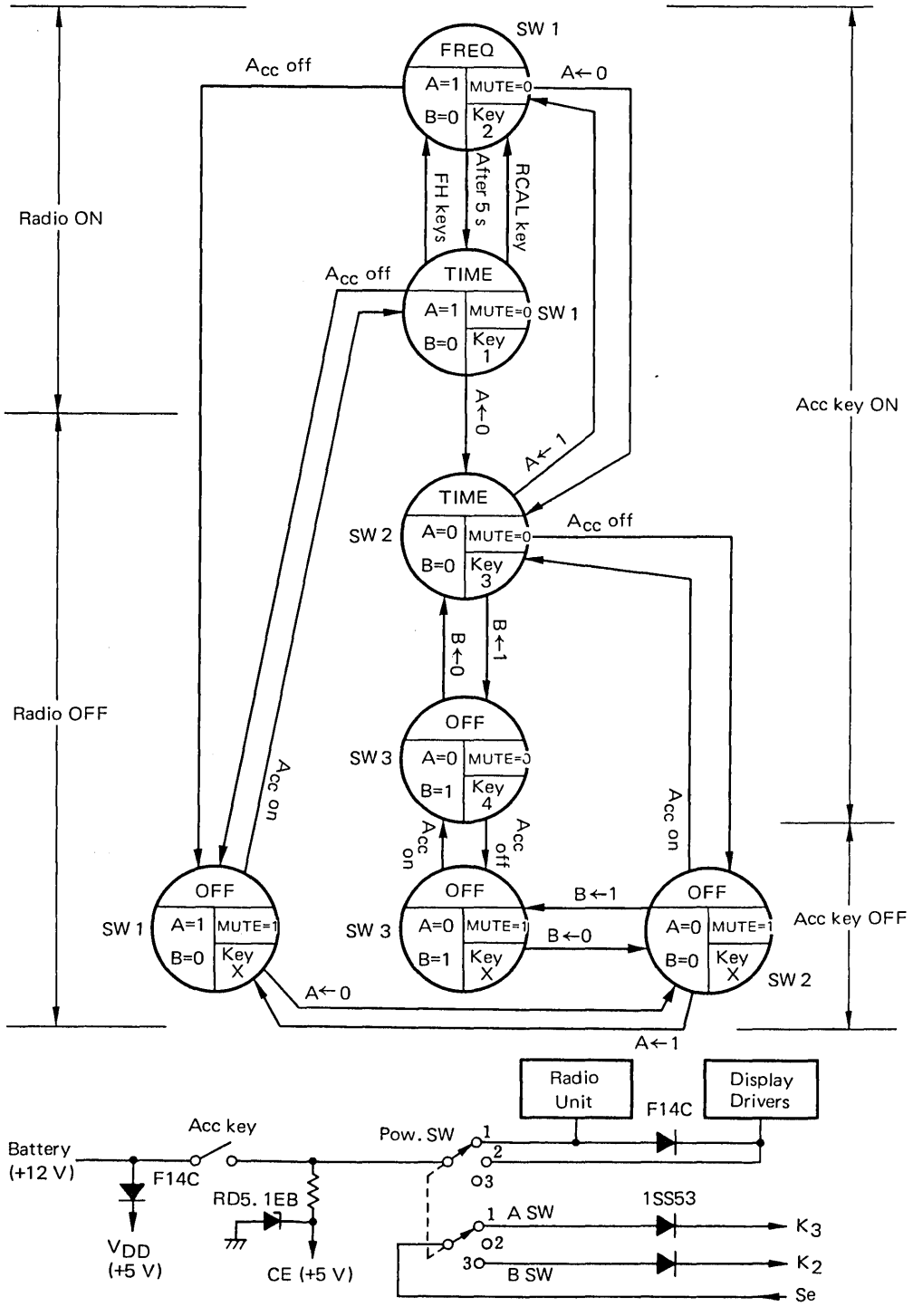


Fig. 7

Frequency display priority method—1 (Using DPDT SW)
Condition : B SW=off (OPEN)
P SW=on (CLOSE)

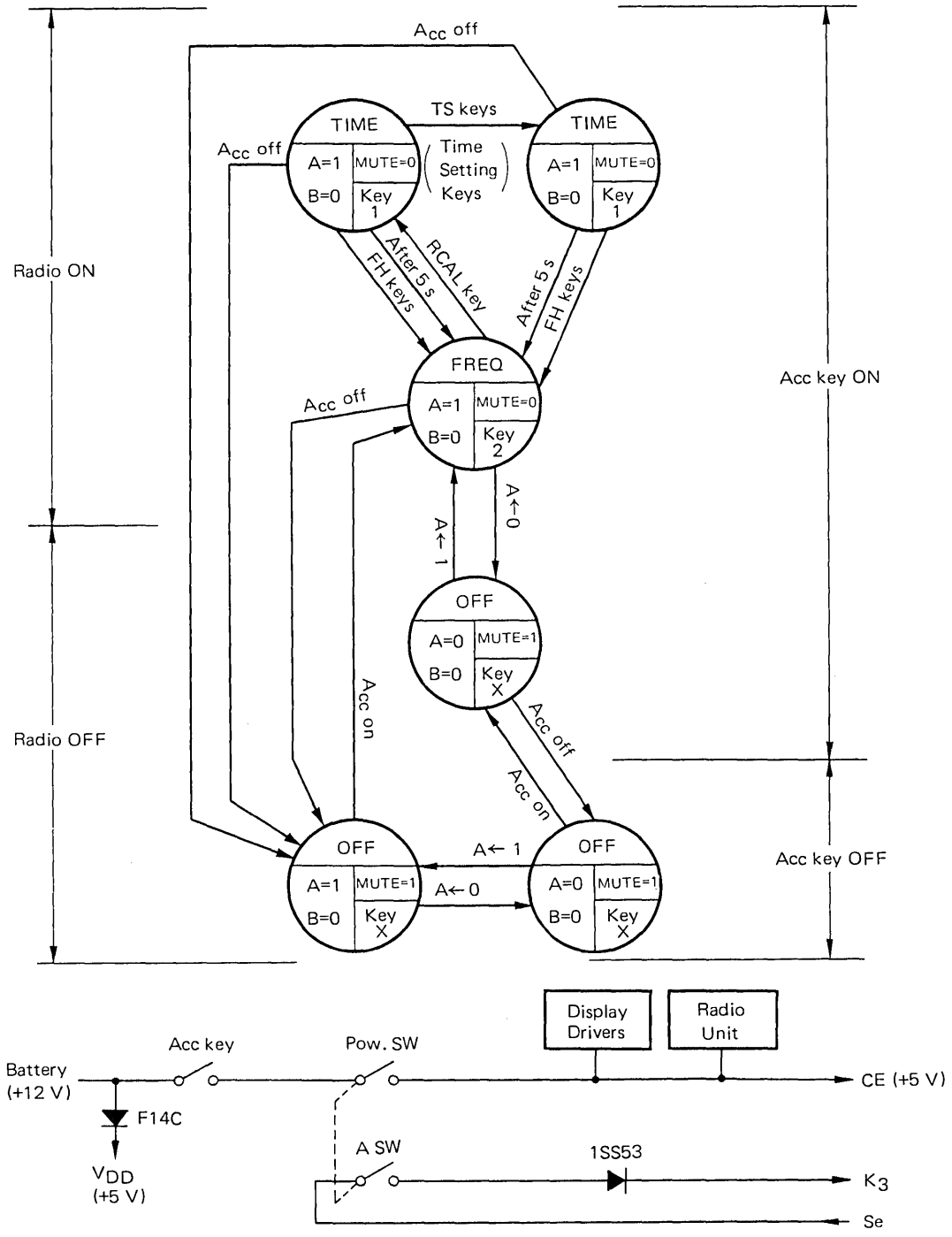


Fig. 8

Frequency display priority method–2 (Using DPDT SW)
Condition : B SW=off (OPEN)
P SW=on (CLOSE)

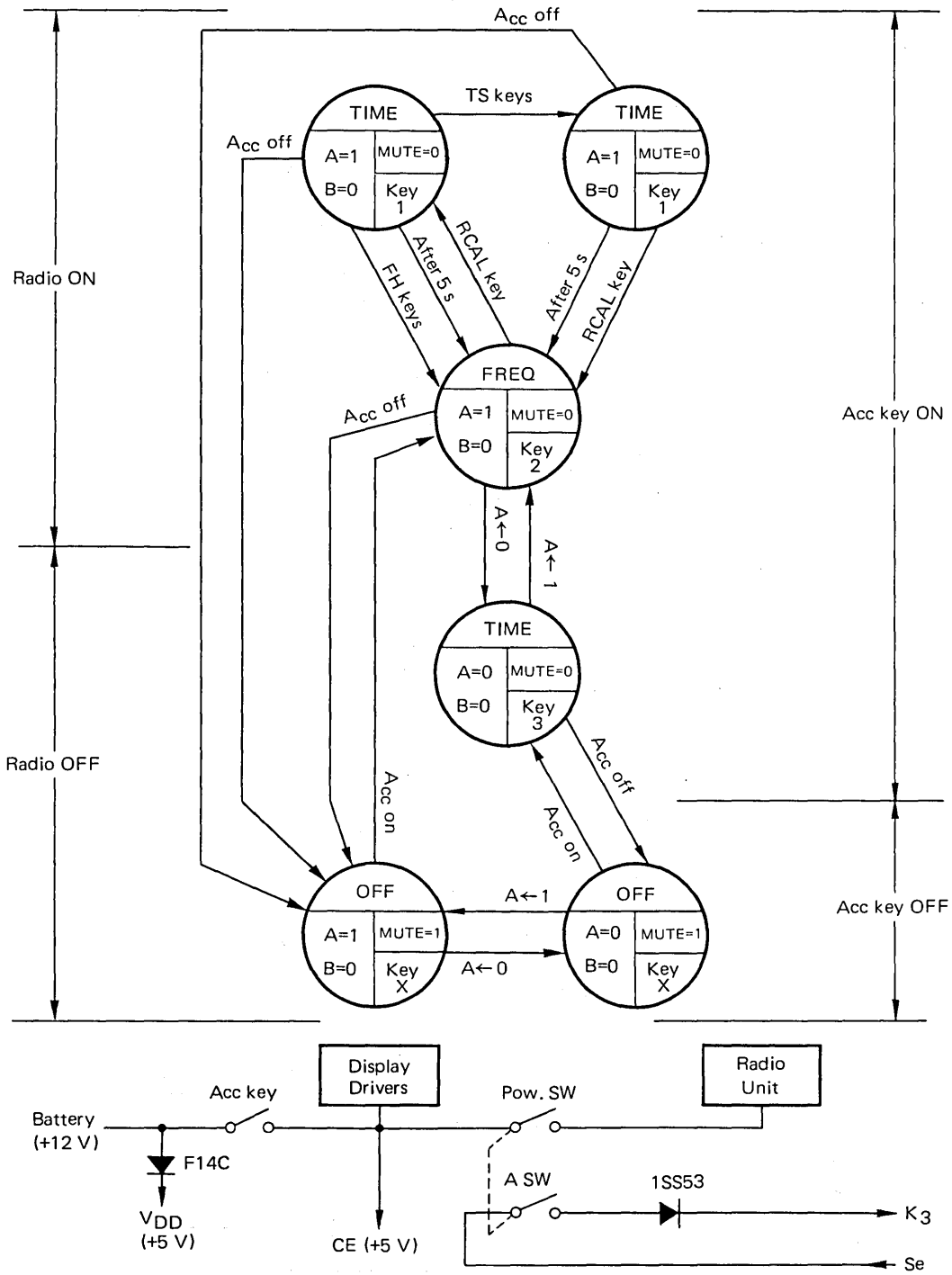


Fig. 9

Frequency display priority method–3 (Using DPTT SW)
Condition : P SW=on (CLOSE)

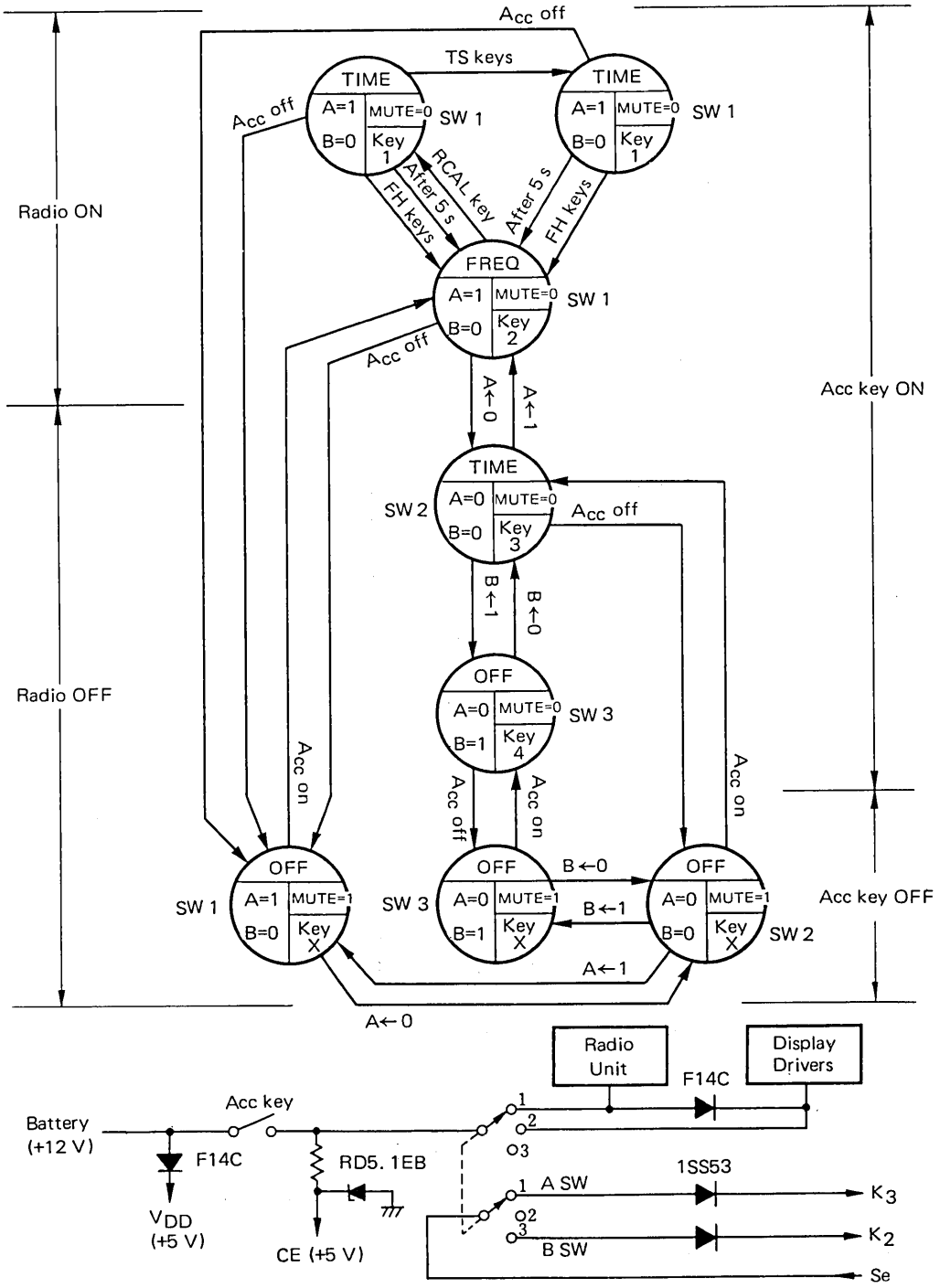
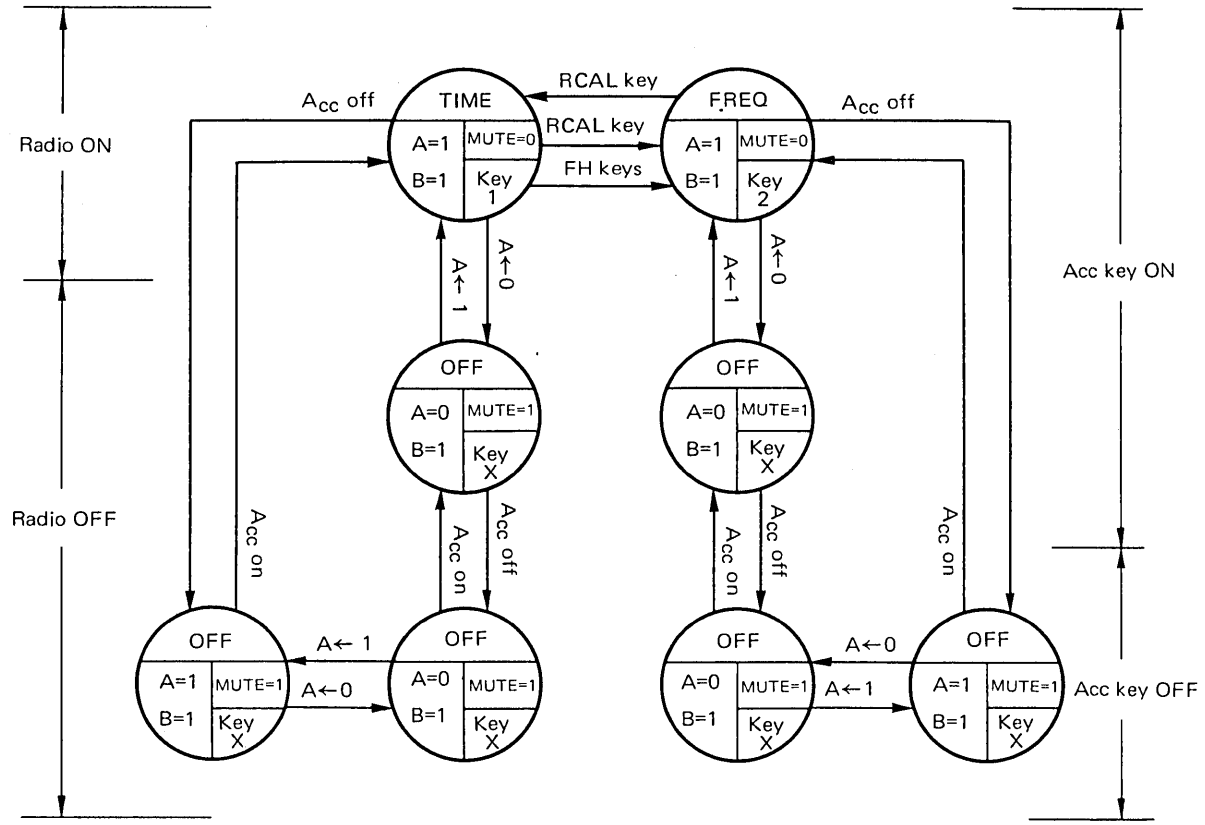


Fig. 10

Display priority switching–over method (Using DPDT SW)
Condition : B SW=on (CLOSE)
P SW= Don't Care.



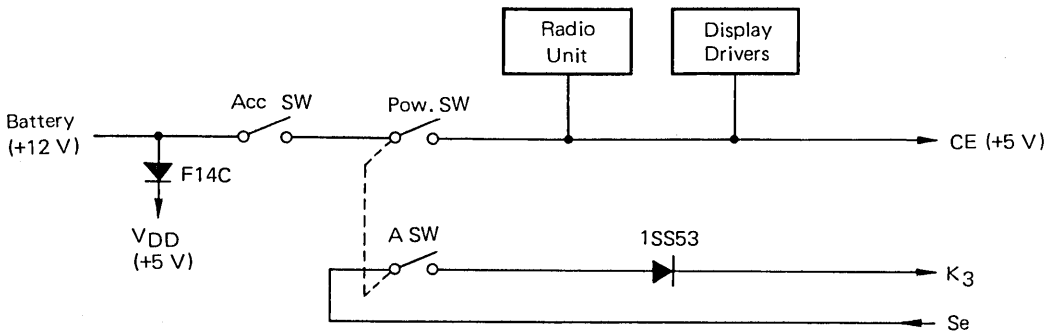


Fig. 11

6. DISPLAY INTERFACE

The μPD1701C-013 provides 5 digit outputs (D1 to D5) and 7 segment outputs (Seg a to Seg g) for display of frequency or time. Mode informations are provided from segment outputs at the timing of D1, and frequency or time (numerical) informations at the timing of D2 to D5. Incorporated display decoder allows the display to be driven by simple current buffers.

The outputs for display are active high for both segment outputs and digit outputs.

Segment Outputs / Digit Outputs	a	b	c	d	e	f	g	Note
D_1	AM	PM	FM DP	COLON 1	COLON 2	–	–	Mode Digit
D_2	A	B	C	D	E	F	G	LSD
D_3	A	B	C	D	E	F	G	2nd Digit
D_4	A	B	C	D	E	F	G	3rd Digit
D_5	–	B	C	–	–	ME	–	MSD.

6-1. DISPLAY FOUNT

When the segment outputs and digit outputs are connected as Fig. 13, a display fount as shown in Fig. 12 will be obtained.

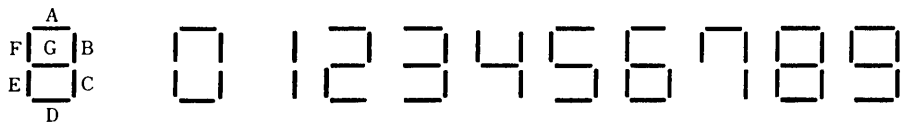


Fig. 12

6-2. MODE INFORMATIONS

The mode informations are used to indicate AM, PM, FM/DP, COLON 1, COLON 2 and ME.

Mode	Description
AM	The morning (When time is displayed) or AM band (When frequency is displayed)
PM	The afternoon
FM/DP	FM band and Decimal Point
COLON 1	Not blinking colon
COLON 2	Blinking colon
ME	Memory enable (It is able to preset station to memory when frequency is displayed)

6-3. AN APPLICATION CIRCUIT OF DISPLAY

Fig. 13 shows an application circuit of display using 7 segment LED (cathode common type).

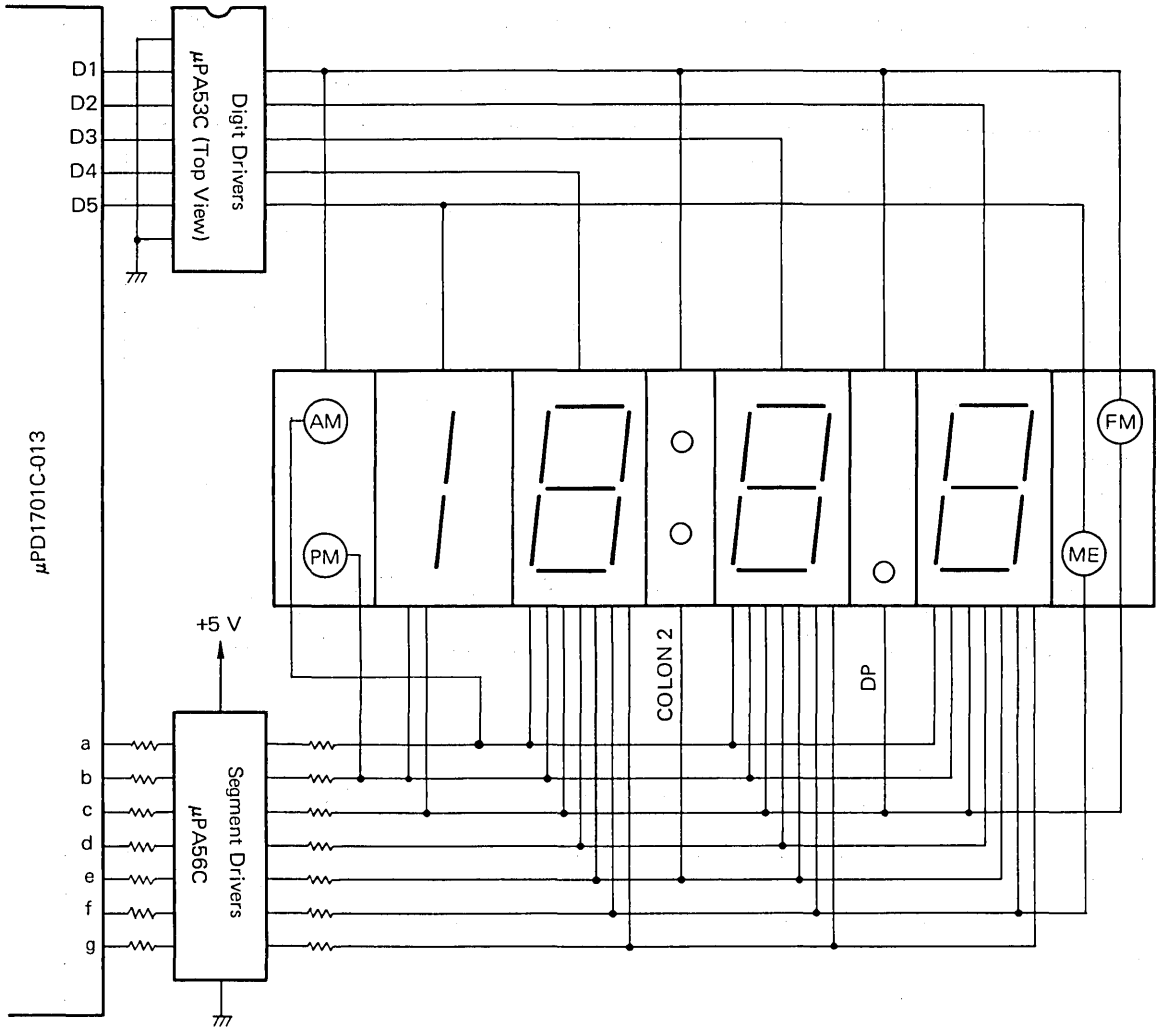


Fig. 13 An Application Circuit of Display

7. CRYSTAL RESONATOR

The oscillation circuit of the μPD1701C-013 is of the single stage CMOS inverter type, and a crystal resonator of 4.500 000 MHz nominal frequency is connected between the input (X1 ⑤ pin) and output (X2 ⑥ pin) of the oscillator stage. As properties required of a crystal clock oscillator circuit, low current consumption, low oscillation starting voltage, small frequency variation, etc. can be mentioned. In general, the current consumption will become less, the smaller the equivalent series resistance (R_1) of the crystal resonator, and the smaller and equal are the gate and drain capacitors, C_G and C_D. However, in practice it is necessary to make either C_G or C_D a variable capacitor, since the oscillation frequency will deviate from the desired value due to deviations in the capacitor of C_G and C_D, the frequency of the crystal resonator, and the stray capacity of the oscillator stage of the μPD1701C-013. As a condition to reduce the oscillation starting voltage, C_G and C_D should both be less than 30 pF, the oscillation starting voltage becoming minimum when C_G and C_D are within a range of 10 to 25 pF. The oscillation frequency will be stable against variations of voltage and temperature, when stable components are used for the series resistor (R_1) and C_G and C_D. An optimum crystal should be selected by giving consideration to the above matters. An example is given following.

Nominal frequency	:	4.500 000 MHz
Type	:	HC–18/U
Frequency deviation	:	± 20 ppm
Equivalent series resistance	:	Less than 70 Ω
Load capacitor (C_L)	:	12 pF

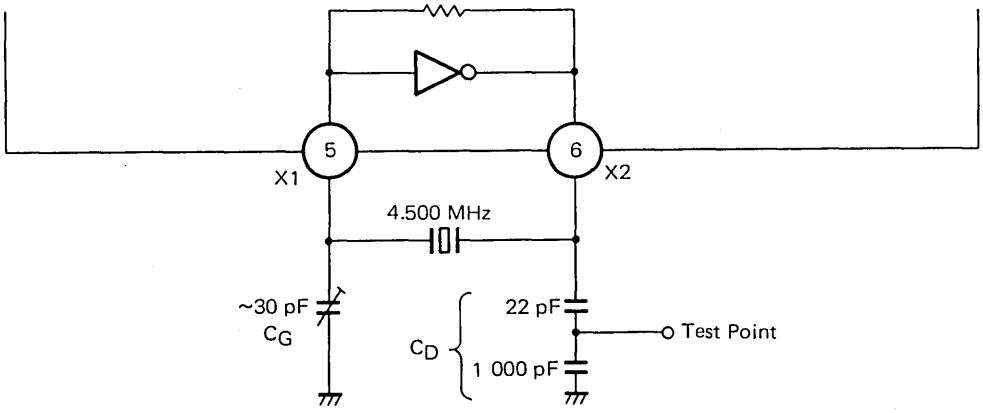


Fig. 14

8. POWER SUPPLY VOLTAGE

The operating voltage range of the μPD1701C-013 is 4.5 to 5.5 V, and is lower than the 12 volt battery systems of most automobiles. Therefore, it is necessary to connect a voltage regulator (μPC78M05, etc.) between the V_{DD} terminal (⑭ pin) and GND terminal (㉗ pin), in order to prevent a voltage of over (–0.3 to +6.0 V) being applied.

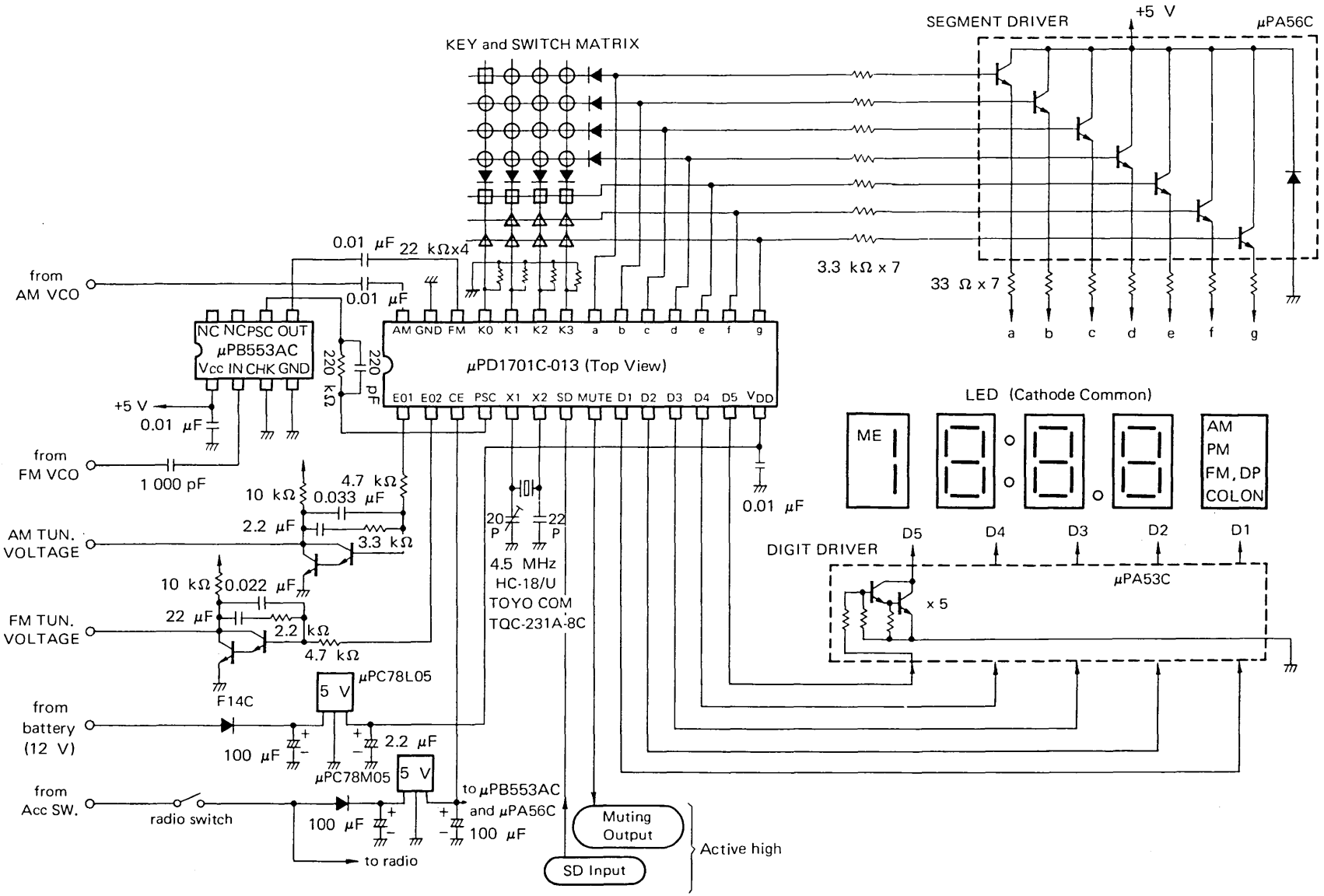


Fig. 15 Application Circuit

PROGRAMMABLE PORTABLE CLOCK LSI: μPD832G SERIES

1. DESCRIPTION OF μPD832G SERIES

The μPD832G series (μPD832G, μPD833G) are CMOS LSI's for Multiple Function Electronic Clock, which are designed to be mounted in a clock/timer altogether with either 4.194 304 MHz or 32.768 kHz quartz crystal, or the like and 4-digit liquid crystal display.

Concerning to display, not only "AM/PM", "hour" and "minute" but also "second" by a demand switch can be shown. The "24-hour" display format is of course able to be employed in stead of the "AM/PM" without essential changes.

The μPD832G series are the LSI's for programmable multi-function clock whose features are carried by internally stored 3 memories of A, B and C as follows:

Memory A is fixedly assigned to the

(1) basic clock function.

Memory B can be utilized for any one of the following applications.

(2) alarm timer
(3) control timer
(4) dual time
(5) chronograph

And Memory C can be used for

(6) snooze timer
(7) or sleep timer

Futhermore, Memory B can make a

(8) counter function

available by associating with special outside circuitry.

A single battery cell (such as UM-1,2,3,4,5 or silver oxide battery) can drive the memories of A, B and C, memory controllers and crystal oscillation circuit sections generating clock in the LSI altogether, due to the required supply voltage ($V_{DD}-V_{SS}$) of 1.5 V. Therefore, these LSI's ar especially suitable to portable clocks.

The LCD (Liquid Crystal Display) driving circuitry, however, needs differently a higher voltage (V_{SH}).

The LSI associated with outside 2 capacitors can double the voltage of the battery, in other words generate 3volts so that V_{SH} is available easily through the pin C_{2N} of the LSI.

$V_{DD}-V_{SH}$ may be supplied externally raging from 2.2 to 6.5 V,however,a safety proof such that DC voltage must not be applied to the LCD should be required as a precaution for this application.

All the outputs from the control circuits (Alarm, Control and Sleep) are available in open drain configuration of the p-channel transistor and this causes system design to be flexible.

The maximum operating voltage of that p-channel transistor is 6.5 V which corresponds to that of V_{SH}.

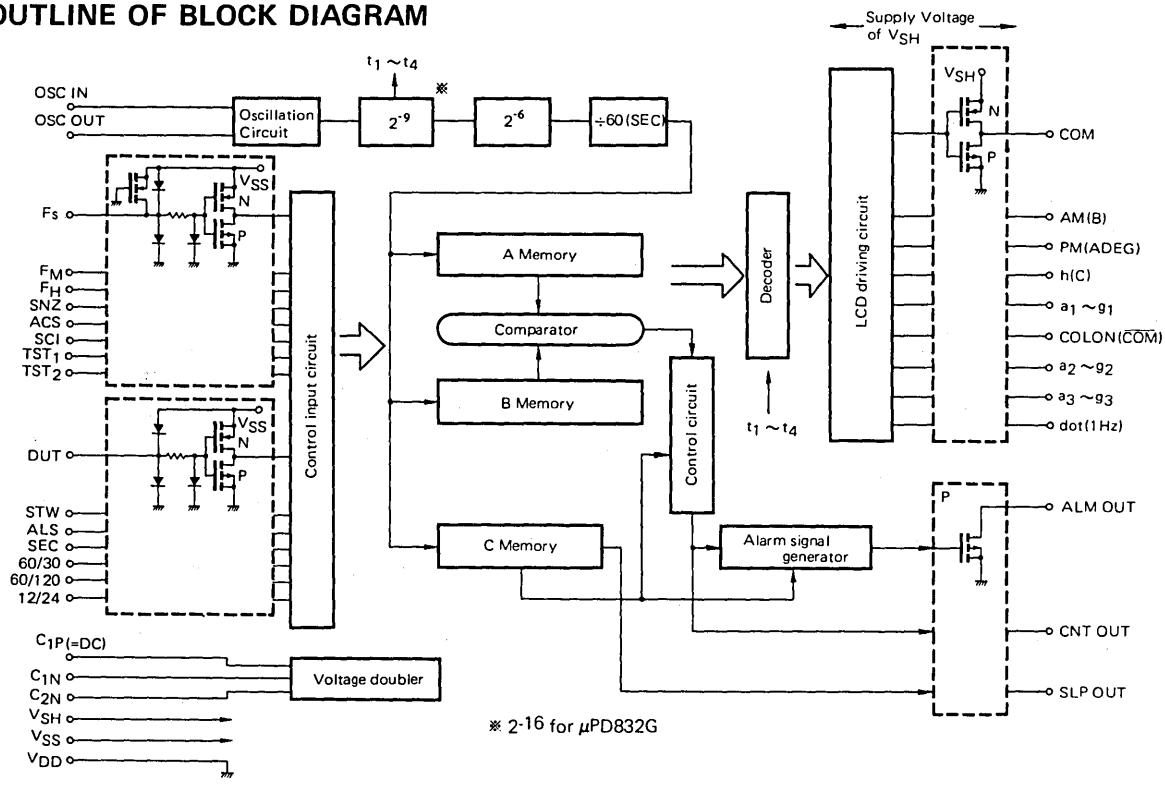
2. APPLICATIONS OF μPD832G SERIES

Digital Alarm Clock
Clock with Sleep Timer
Alarm Clock with Snooze Timer
Traverer's Clock
Dual-Time Clock
Clock with Chronograph
Control Clock for Electric Equipment
Timer for Trip Duration
Timer for Elapsed Duration
Desk-Top Clock
Portable Timer for General Control

3. TYPES IN μPD832G SERIES

Type No.	Principal Oscilator (e.g. quartz)	Flat Plastic Molded Package
μPD832G μPD833G	4.194304 MHz 32.768 kHz	9mm square 54-pin

OUTLINE OF BLOCK DIAGRAM



4. HANDLING PRECAUTIONS OF μPD832G SERIES

4-1 Soldering

Reflow soldering by such equipment as Browne's Model LR-6 or AR-7 is recommended for soldering of μPD832G series.

In the case of soldering iron, there should be no leak current from iron tip. The temperature of iron tip should not be higher than 260 °C and soldering duration should not be longer than 15 sec.

4-2 After treatment

After any one of the μPD832G series is mounted on a piece of printed circuit board, it should be cleaned with such solvent as ethanol or trichlorotrifluoroethan and then dried perfectly.

Recommended cleaning and drying conditions are as follows:

Cleaning Duration	1 min. Max per run
Cleaning Cycle	Twice
Cleaning Method	Rinsing, steam cleaning or ultrasonic cleaning
Drying Temperature	70 to 80 °C
Drying Duration	5 to 10 min.

Thereafter its package body as well as entire leads should be coated uniformly with protective silicone plastic resin featuring sufficiently small leakage. Dau Corning's XR-2622 or Pelnox's CE-22A is applicable for this purpose.

The reason for after treatment is as follows.

The clock use LSI needs quite a small current raging from hundred nano amperes to micro amperes, therefore even if very small, no additional leak current is allowable for the LSI to keep its accurate operation.

Such counter measure should be required that the LSI is not affected so as to cause extra leak current by dust, humidity and dew in the worst case because of its narrow lead arranging pitch.

4-3 Lead forming

In lead forming of the μPD832G and μPD833G, bend the leads where away from their joints by 0.5 to 1 mm. And during the lead forming, it is important that the leads are fixed straightly as far as 0.5 to 1 mm from their joints and free from bending force at the joints.

4-4 Adjustment on oscillation frequency

A particular consideration on measuring instrument is payable in fine adjustment of the oscillation frequency to assure an ultimately high accuracy. (An accuracy of 1 ppm corresponds approximately to 0.1 sec in daily defference.)

The pace regulator for clock typed as UT-200(of NipponDempa Kogyo Co., Ltd.) for example can be used for frequency adjustment of crystal oscillator.

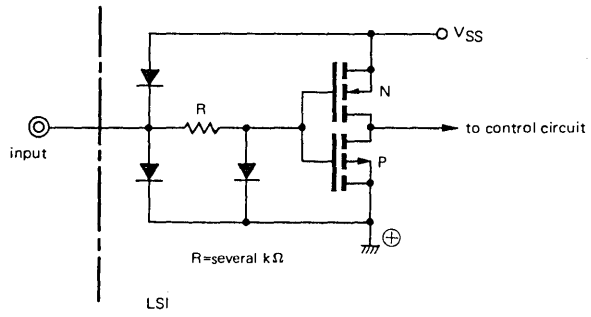
A frequency counter can also be employed to measure directly the frequency or interval, however, a 9 to 10-digit counter is desirable against such an accuracy as 0.1 sec/day.

In this case, the DC output (from pin 51 for μPD832G and μPD833G) or the COM output (from pin 40 for μPD832G and μPD833G) where the frequency of DC output is 512 Hz(=1.953125 ms) and COM output is 64 Hz (=15.625 ms) are ready to be utilized.

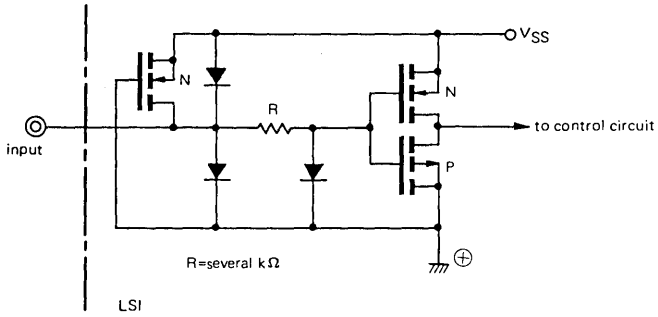
5. INPUT AND OUTPUT CIRCUITS FOR μPD832G SERIES

5-1 Input circuits

(i) Input terminals without pull-down resistor

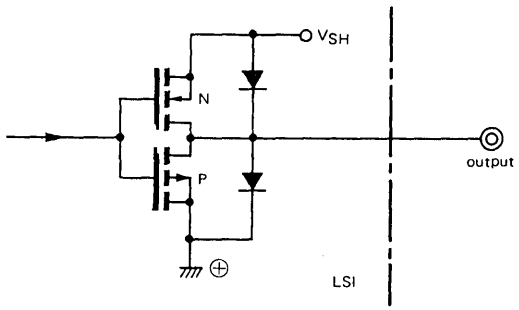


(ii) Input terminals with pull-down resistor

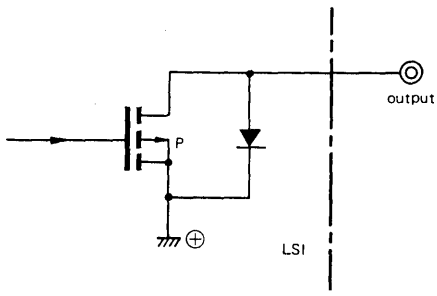


5-2 Output circuits

(i) Output terminals driving LCD segment

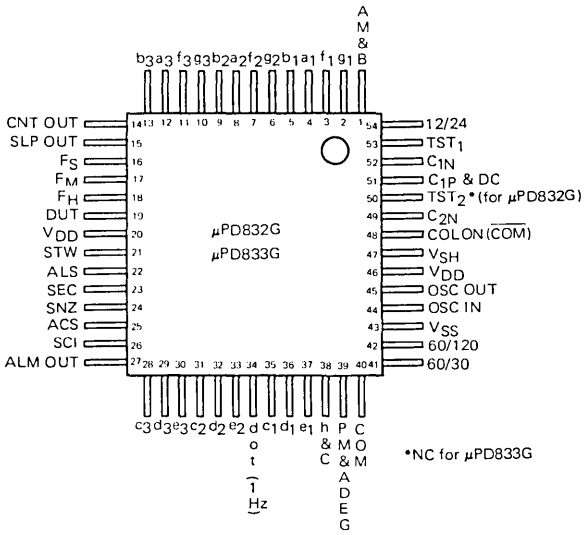


(ii) Output terminals for control



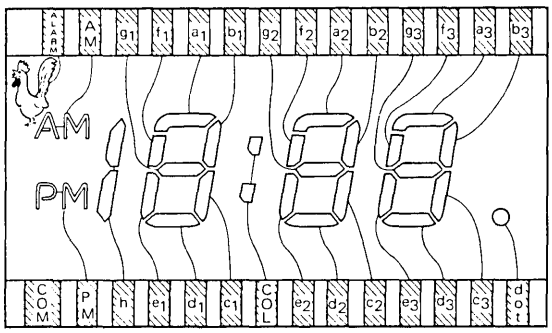
6. PIN LAYOUT

μPD832G and μPD833G

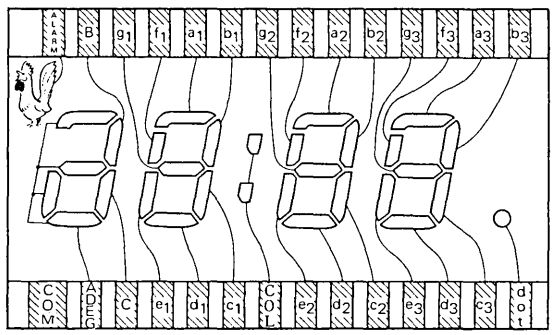


7. TYPICAL FEM-TYPE LIQUID CRYSTAL DISPLAYS FOR μPD832G SERIES

12-hour display panel



24-hour display panel



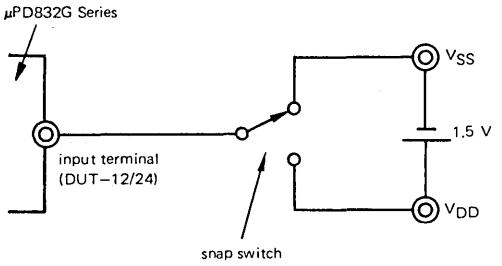
8. INTERNAL PULL-DOWN RESISTORS TO INPUT TERMINALS

Input Terminal	$V_{DD} - V_{SS}$	Resistance	Unit
F_S	1.5V	0.01 ~ 1.0	MΩ
F_M	1.5V	0.01 ~ 1.0	MΩ
F_H	1.5V	0.01 ~ 1.0	MΩ
SNZ	1.5V	0.01 ~ 1.0	MΩ
ACS	1.5V	0.01 ~ 1.0	MΩ
SCI	1.5V	0.01 ~ 1.0	MΩ
TST	1.5V	0.01 ~ 1.0	MΩ
DUT	1.5V	OPEN	
STW	1.5V	OPEN	
ALS	1.5V	OPEN	
SEC	1.5V	OPEN	
60/30	1.5V	OPEN	
60/120	1.5V	OPEN	
12/24	1.5V	OPEN	

9. TERMINATION METHODS FOR INPUT TERMINALS

9-1 Unused input terminals should be connected to V_{SS}(−).

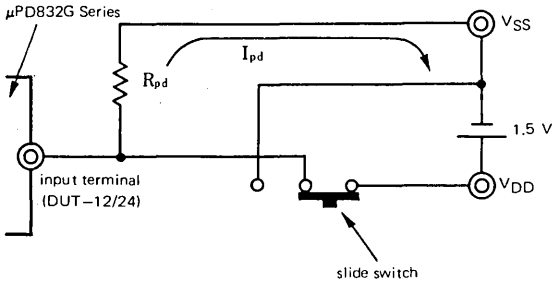
9-2 As the DUT − 12/24 input terminals tabulated in paragraph 8 are open terminals, they should be always connected to either V_{SS} or V_{DD}.It is easy for this purpose to employ a single-pole double-throw toggle switch (snap switch) as shown in the right diagram.



9-3 Terminating the DUT − 12/24 input terminals by use of a single-pole single-contact push or slide switch, etc. instead of a snap switch, a pull-down resistor should be added to each input terminal for prevention of floating as illustrated in the right.

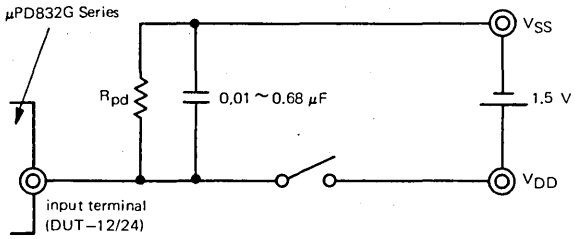
It may be noted, however, that extra current flows through the pull-down resistor R_{pd}, which is calculated with both $V_{DD}-V_{SS}$(=1.5 V) and R_{pd} according to Ohm's law.

The pull-down resistor may be determined while considering carefully the grounding capability of the clock set itself, the environmental condition (such as humidity, etc.) where it is exposed and the power capability of the battery engaged.



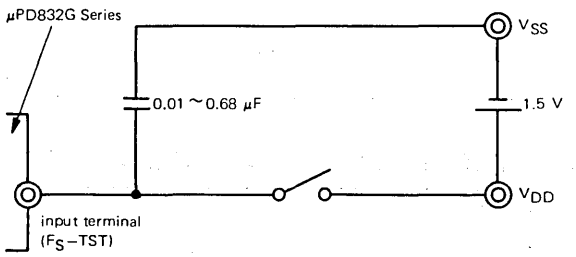
$$I_{pd}[\mu A] = \frac{1.5[V]}{R_{pd}[M\Omega]}$$

9-4 In case of the pull-down resistor R_{pd} raging from several 100 kΩ to several MΩ, it is recommended to insert a capacitor of 0.01 to 0.68 μF range in parallel to the R_{pd} for an improved pulsive noise immunity. (See the right diagram.)



The fact stated above is also applicable to each of the input terminals F_S − TST of the LSI tabulated in paragraph 8, which has an internal pull-down resistor originally.

Accordingly, if there might be pulsive noise around the LSI, a capacitor of 0.01 to 0.68 μF range should be connected between V_{SS} and each of the input terminals F_S − TST.



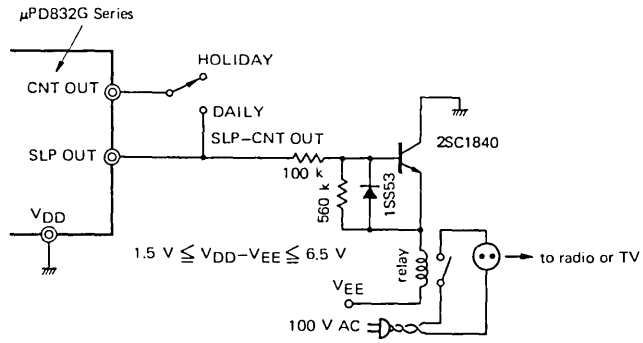
This shunt capacitor is unnecessary when a snap switch is applied to an input terminal (DUT − 12/24) or when an unused terminal is connected directly to V_{SS} or V_{DD}.

10. EXAMPLE CIRCUITRY EMPLOYING μPD832G SERIES

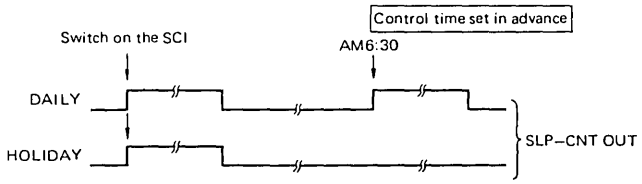
10-1 Sleep timer (Switch on SLP) at night

Dual mode time switch for a radio or TV receiver in weekday mornings (Select DAILY) and cease time switch in holiday mornings (Select HOLIDAY) (Provided that alarm timer is not engaged.)

Circuit



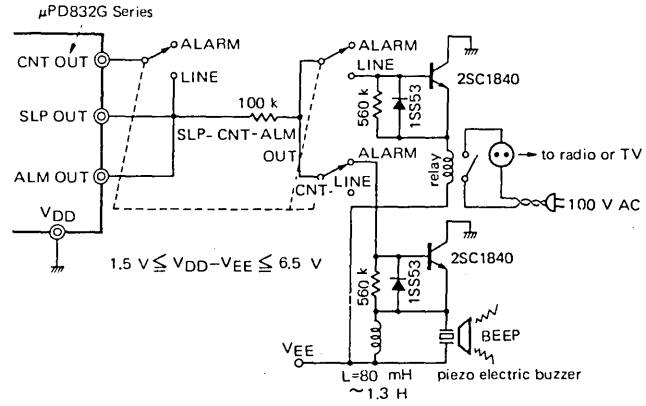
Output timing chart



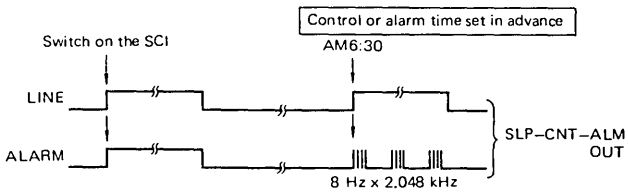
10-2 Sleep timer (Switch on SLP) at night

Eather alarm (Select ALARM) or dual mode time switch (Select LINE) for a radio or TV receiver in the morning

Circuit



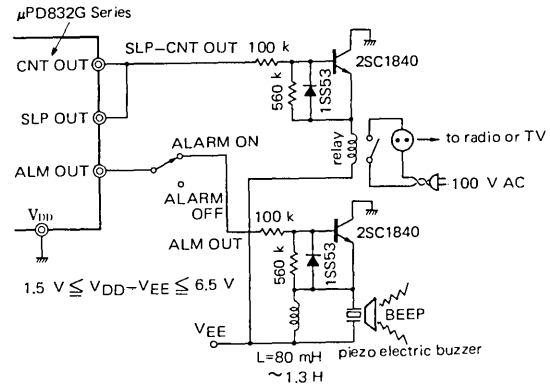
Output timing chart



10-3 Sleep timer (Switch on SLP) at night

Eather both alarm and dual mode time switch for a radio or TV receiver (Select ALARM ON) or time switch alone (Select ALARM OFF) in the morning

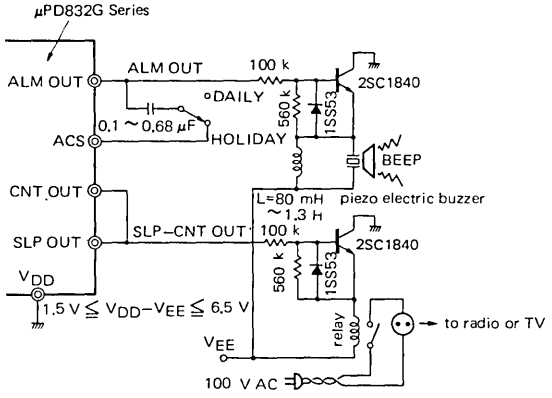
Circuit



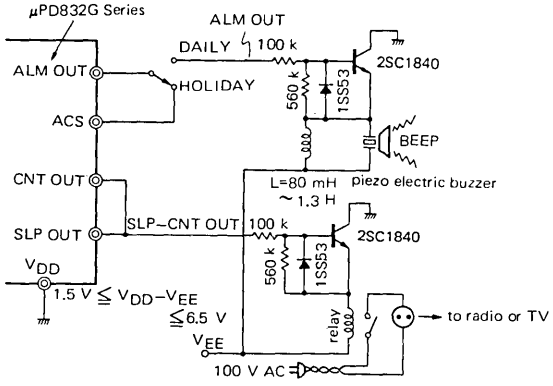
10-4 Sleep timer (Switch on SLP) at night

Both alarm and dual mode time switch for a radio or TV receiver in the weekday morning (Select DAILY) and silent in the holiday morning (Select HOLIDAY)

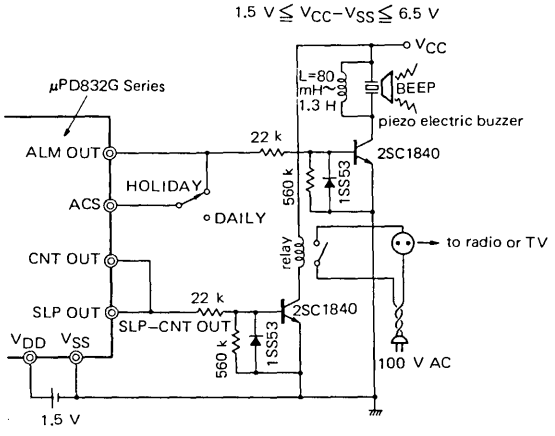
Circuit (i)

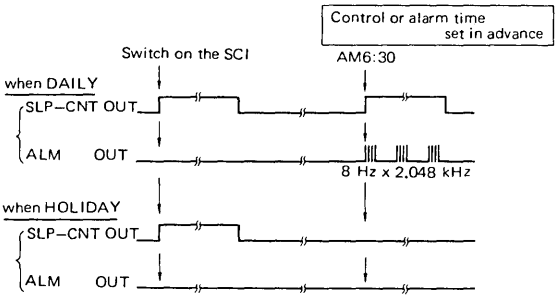


Circuit (ii)



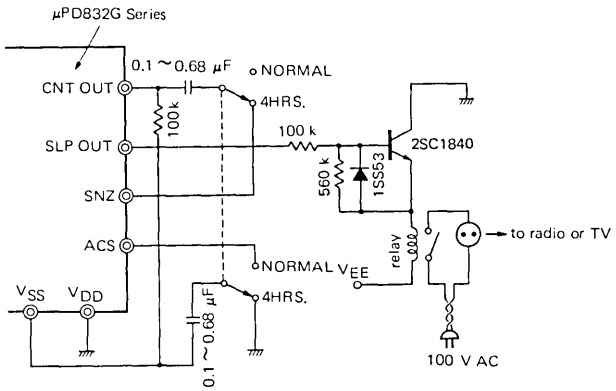
Circuit (iii)





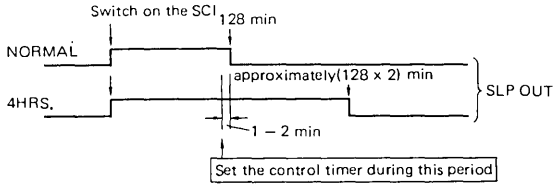
10-5 Double the duration of sleep timer at a particular night

Circuit



Set the Control Time to the time of one to two minute(s) prior the ending time to be set for sleep timer firstly and then switch on the sleep timer immedeately.

Thus, if the original duration of the sleep timer is 128min(=2hrs), the resulted duration can be approximately 128min x 2 = 256min (=4hrs).

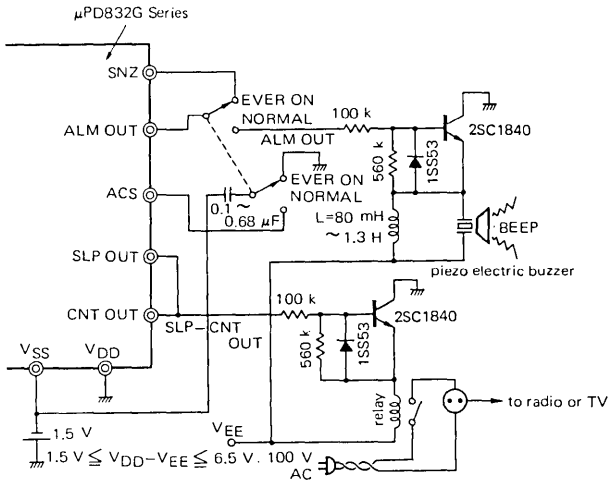


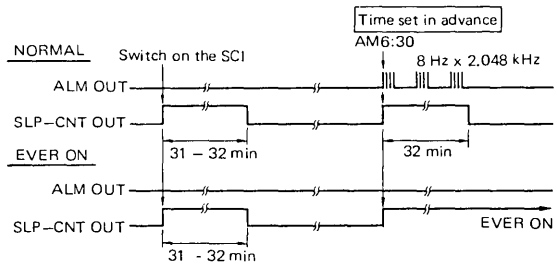
10-6 Sleep timer (Switch on SLP) at night

Eather alarm (Select NORMAL) or single mode time switch (Select EVER ON) for a radio or TV receiver in the morning

When EVER ON, alarm is not available.

Circuit

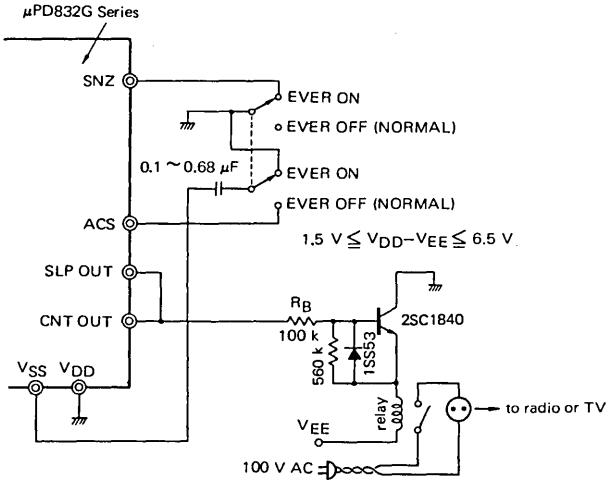




10-7 Ever-on (Select EVER ON) by eather sleep or control timer when ever-on, no alarm available.

Circuit

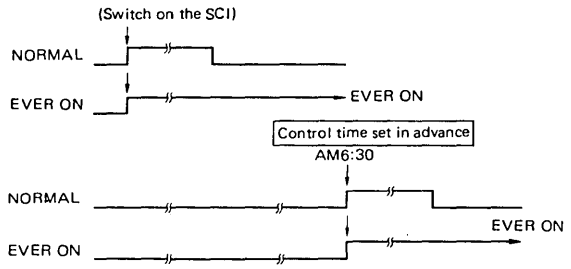
(i) Switch to EVER OFF from EVER ON and instantly the output of the SLP OUT or CNT OUT turns off.



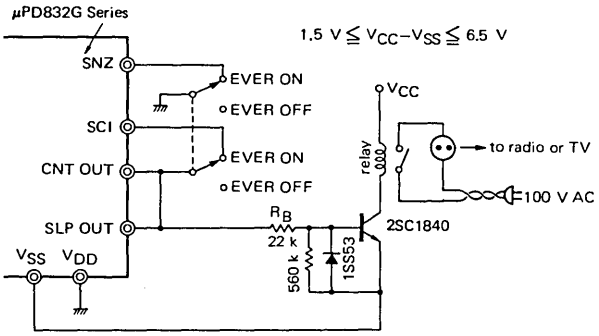
Determination on R_B $R_B \geqq \frac{V_{DD}-V_{EE}}{100\ \mu A}$

$R_B \geqq \frac{6.0\ V}{0.1\ mA} = 60\ k\Omega \rightarrow 100\ k\Omega$

Output timing chart



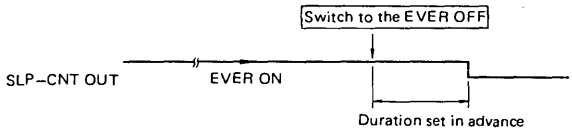
(ii) Switch to EVER OFF from EVER ON and after the pre-set duration, the output of the SLP OUT or CNT OUT turns off.



Determination on R_B $R_B \geqq \frac{V_{DD}-V_{SS}}{100\ \mu A}$

$R_B \geqq \frac{1.5\ V}{0.1\ mA} = 15\ k\Omega \rightarrow 22\ k\Omega$

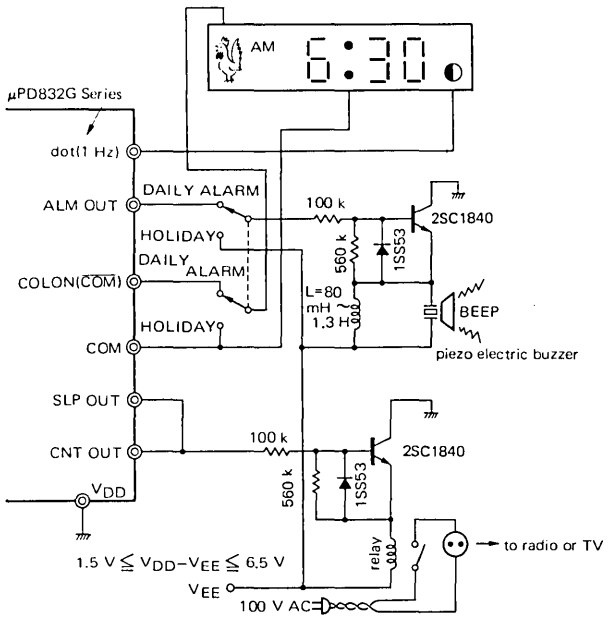
Output timing chart



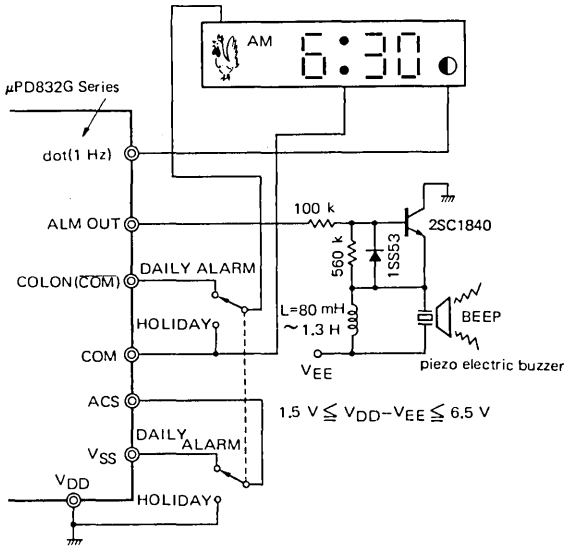
10-8 Display on alarm sign

(The "cock" mark in the LCD stands for the sign of "DAILY ALARM". When this mark is visible, alarm is available everyday at the pre-set time.)

(i) Turn off alarm output solely When the "cock" mark is invisible.
In this case, the sleep output and control output can be utilized even if HOLIDAY.



(ii) Turn off not only alarm but also sleep and control output

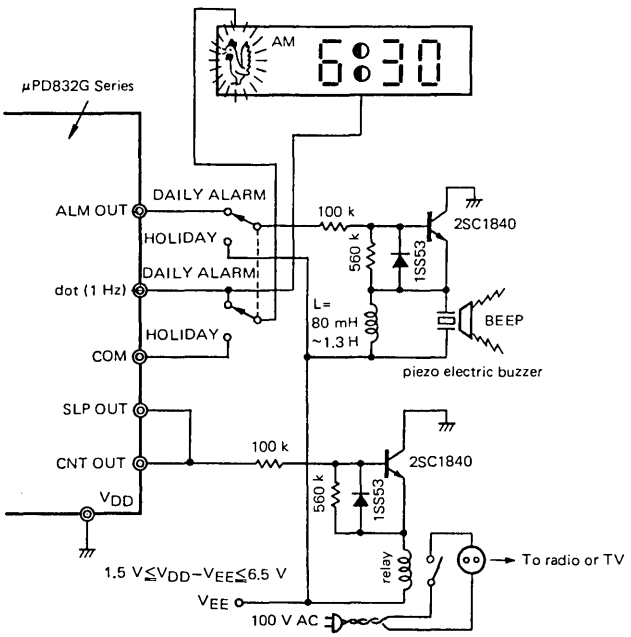


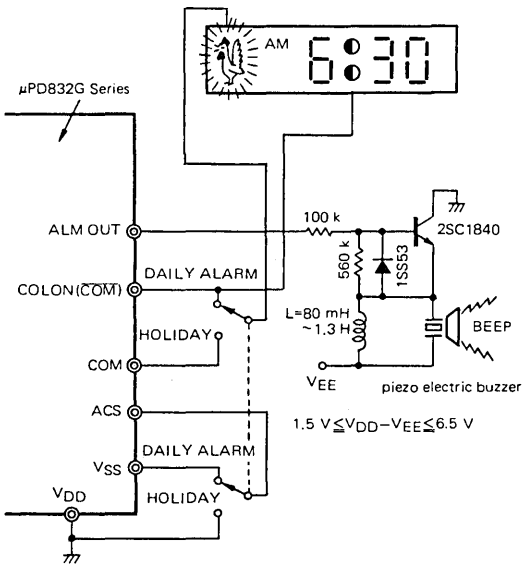
10-9 Display on alarm sign (How to be unused $\overline{COM}$ terminal)

The "cock" mark in the LCD stands for the sign of "DAILY ALARM." When this mark to be flashed at a 1Hz rate is visible, alarm is available everyday at the pre-set time.

(i) Turn off alarm output solely when the "cock" mark is invisible.
In this case, the sleep output and control output can be utilized even if HOLIDAY.

(ii) Turn off not only alarm but also sleep and control output.





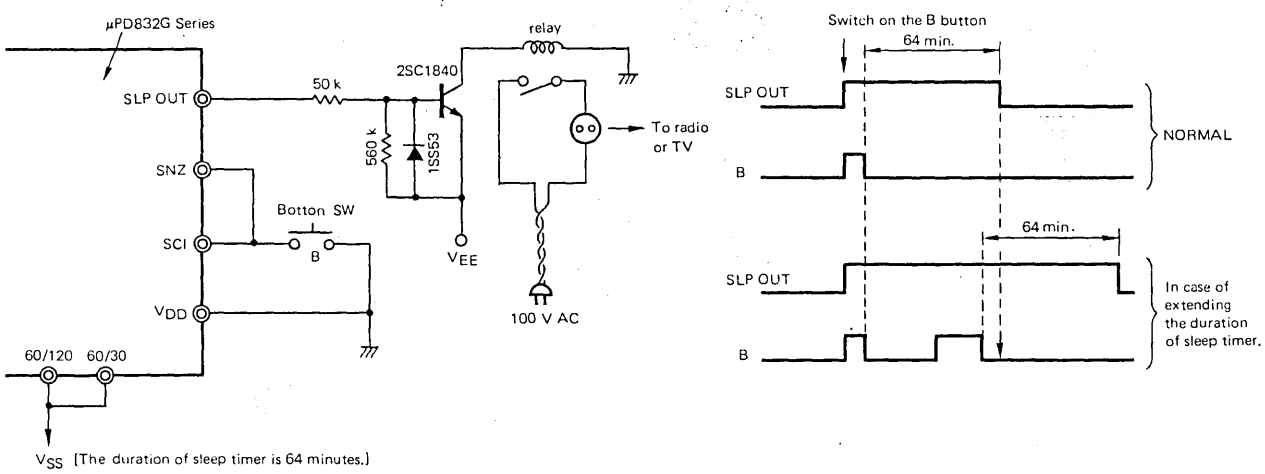
: This is the sign of "DAILY ALARM" armed with alarm and is flashing at a 1Hz rate.

: The COLON is flashing at a 1 Hz rate.

[NOTICE] 1. When is displayed the ALARM mode, the sign of "DAILY ALARM" is frozen. That condition is ( ).
2. This circuit is suitable for the "M" product of μPD833G that has not $\overline{COM}$ signal terminal.
(But is provided the integrated Voltage Tripler.)

10-10 How to be extended the duration of sleep timer output.

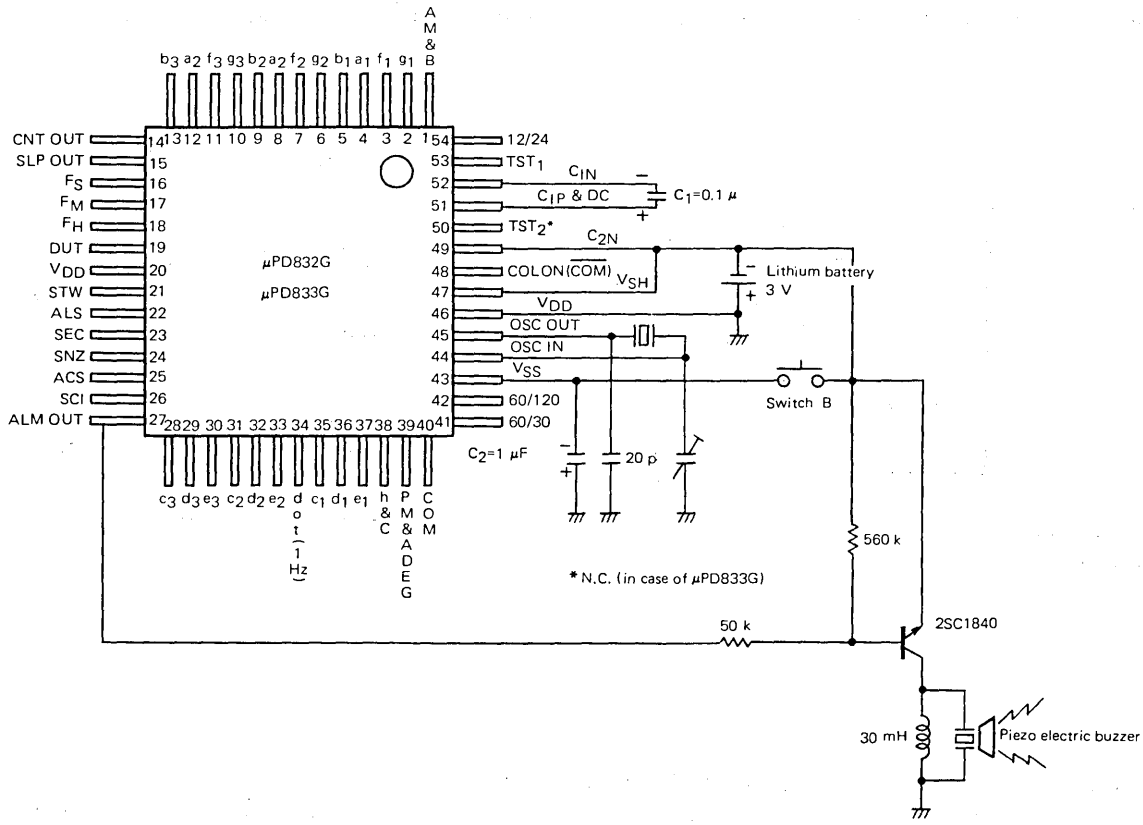
When the B button is pushed momentarily, the sleep output is activated. But in case of extending the duration of Sleep timer output while the sleep output, has to be pushed the B button in the following circuit.



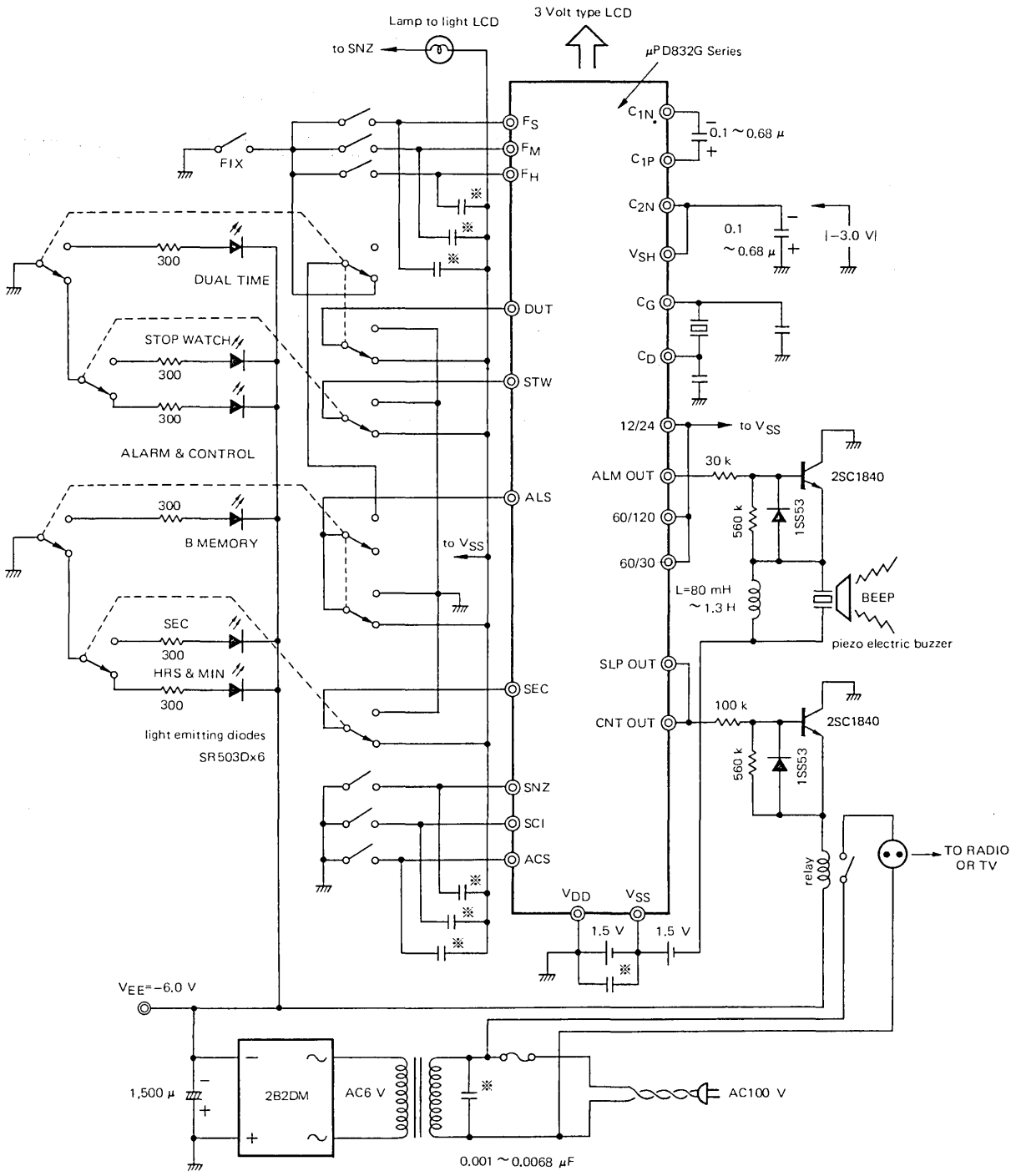
[The duration of sleep timer is 64 minutes.]

[NOTICE] 1. In case of this, it is not used the Snooze function.
2. When the CNT OUTPUT is activated, it is available to be extended the duration of the control timer by pushing the B button.
3. Whenever is pushed the B button, it can be renewed the duration of the sleep timer. It will be started the Sleep timer when is switched off the B button.

10-11 How to apply Lithium battery to μPD832G Series



[NOTICE] After lithium battery (+3 V) is connected to $V_{AA} - V_{SH}$, it should be pushed momentarily on by switch B.



※ Capacitor for absorption of surge cased by power transformer when AC-line is turned on or off necessary 0.01 to 0.68 μF.

HOW TO USE μPD1990AC
TIME KEEPING LSI FOR MICROCOMPUTER SYSTEM

INTRODUCTION

The conventional time keeper for ECR or microcomputer system is a one-board clock built with various counters, logic gates and flip-flops for TTLs, and MOS MSIs. Because this one-board clock is required a wide space for mounting and a large amount of power in the system, it has difficulty in functioning as a battery-operated clock stably for a long time when the system power supply is turned off.

Recently, a one-board time keeper using the LSI, named μPD1990AC, has attracted notice.

This time keeper μPD1990AC is a one chip LSI and consumes a very small amount of power. It is suitable for a long battery operation when the system power supply is turned off. The μPD1990AC is an easy to use IC controlled with 3 bit commands.

Since the μPD1990AC has N-channel open-drain outputs, the interface between the μPD1990AC and the system can easily be formed.

This manual describes the μPD1990AC CMOS LSI best suited for the establishment of clock functions in microcomputer systems.

TABLE OF CONTENTS

1. OUTLINE OF μPD1990AC

The μPD1990AC is an IC that supplies time data serially to a system using microcomputers and the like. Time data consists of 40 bits of month, date, day of the week, hour (24-hour system), minute, and second. Month data is expressed in hexadecimal (1 through C) and other data, in BCD (Binary Coded Decimal).

Time data is serially input and output in synchronized with the external clock applied to the CLK terminal.

The operation of the μPD1990AC is controlled with commands of 3 bits (C_0, C_1, and C_2) each. These commands are divided into two groups: 0-group commands to control the input and output of time data and 1-group commands to select timing pulses and test mode.

The supply voltage is $V_{DD}-V_{SS}$=2.0~5.5 V. When using two commercially available batteries (UM-1, UM-2, UM-3, UM-4, UM-5, or silver oxide), a supply voltage of 3.0 V is obtainable. The use of two Ni-Cd batteries (possible to charge) gives a supply voltage of 2.4 V and that of three Ni-Cd batteries gives 3.6 V. Using these Ni-Cd batteries, the μPD1990AC will be worked semipermanently. This means system power-failure never affects the time keeping and in addition, there is no need for battery replacement. Thus, it can be said that the μPD1990AC is the most suitable time keeper for system.

The μPD1990AC is in the form of 14-pin DIP (Dual In-line Package).

1-1. Features

○ Time data:	Month, date, day of the week, hour, minute and second
○ Data format:	BCD (only month is expressed in hexadecimal using 1 through C.)
○ Data input and output system:	Serial transmission system synchronized with external clocks applied through CLK input
○ Timing pulse output:	Either 64 Hz, 256 Hz, or 2 048 Hz can be selected according to programs.
○ Multi-chip structure:	Multi-chip structure is possible by chip selection (CS)
○ Crystal oscillator:	A crystal oscillator with a standard oscillation frequency of 32.768 kHz

1-2. Package dimensions and connection diagram

PACKAGE DIMENSIONS
in millimeters (inches)

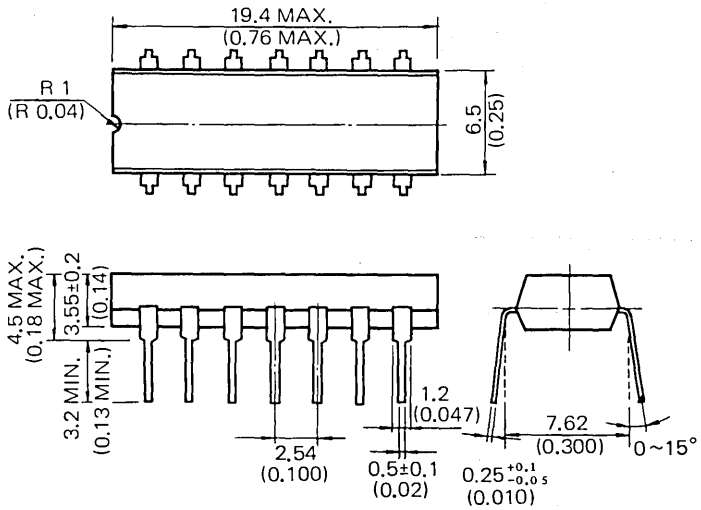


Fig. 1

CONNECTION DIAGRAM (Top View)

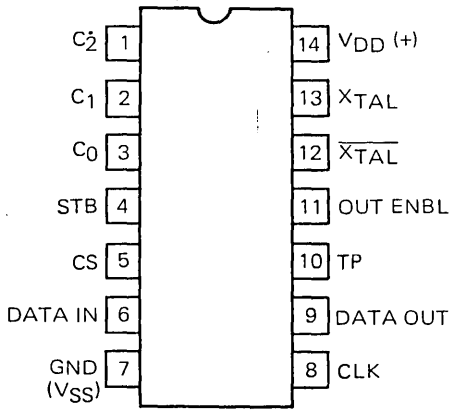
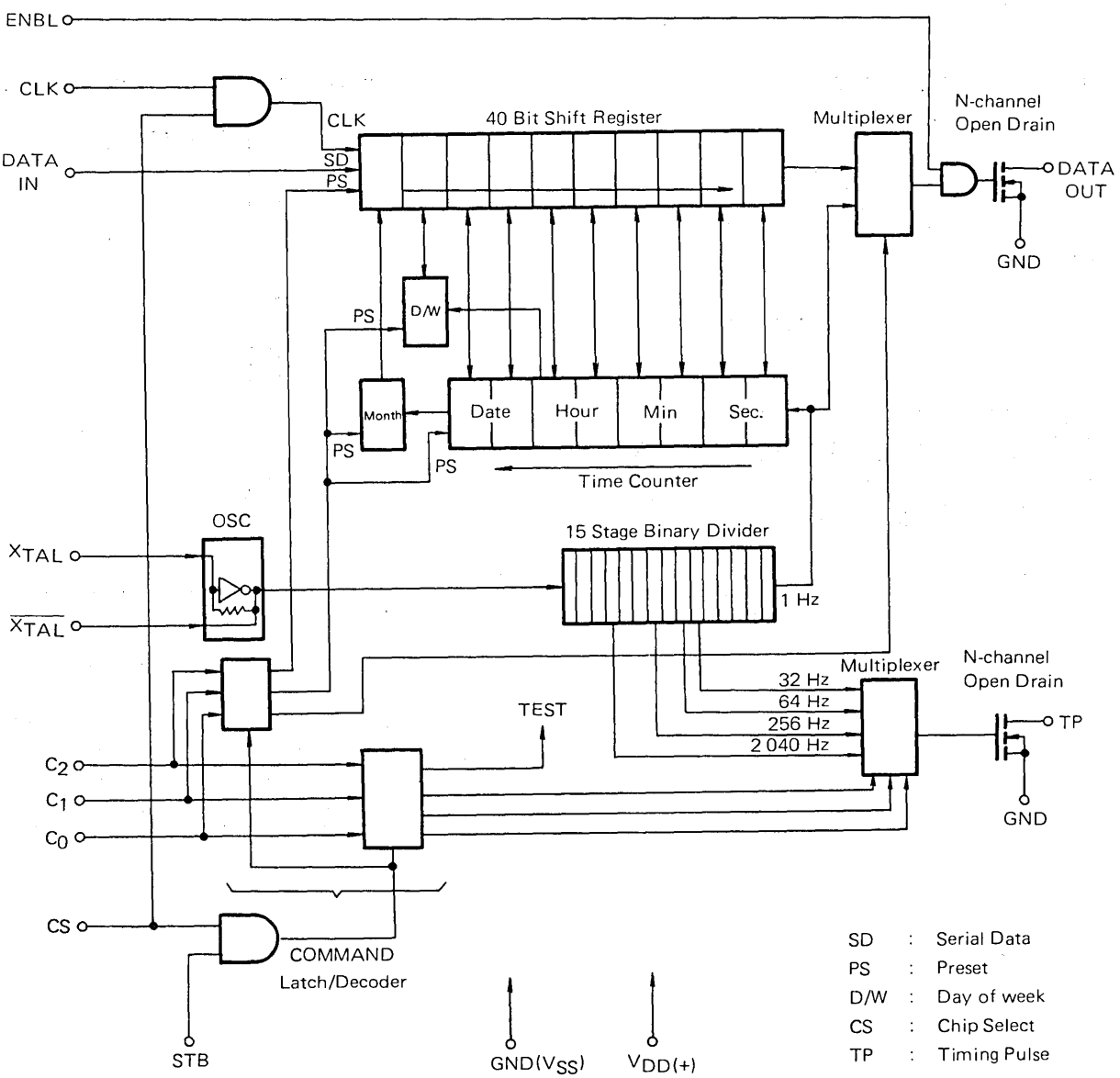


Fig. 2

NO.	Terminology	NO.	Terminology
1	C_2	8	CLK
2	C_1	9	DATA OUT
3	C_0	10	TP
4	STB	11	OUT ENBL
5	CS	12	$\overline{X_{TAL}}$
6	DATA IN	13	X_{TAL}
7	GND (V_{SS})	14	V_{DD} (+)

1-3. Block diagram



f_{osc} = 32.768 kHz
V_{DD} = 2.0 to 5.5 V

Fig. 3

1-4. ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$V_{DD}-V_{SS}$	6.0	V
Input Voltage	V_{IN}	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Operating Temperature Range	Topt	−40 to +85	°C
Storage Temperature Range	Tstg	−55 to +125	°C
Output Terminal Voltage	V_{OUT}	6.0	V

1-5. Electrical and AC characteristics

ELECTRICAL CHARACTERISTICS 1.

(f = 32.768 kHz, $C_G = C_D$ = 20 pF, Xtal R_S = 20 kΩ, Ta = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITONS
Operating Voltage	$V_{DD}-V_{SS}$	2.00		5.50	V	
Current Consumption	I_{SS}		20	50	μA	$V_{DD}-V_{SS}$=3.60 V
Low Level Output Current	I_{OL}	*500			μA	$V_{DD}-V_{SS}$=2.0 V V_{OL}=0.4 V
CLK Input Frequency	f_{CLK}	DC		100	kHz	$V_{DD}-V_{SS}$=2.0 V, Duty 50 %
Input Leakage Current	I_{IN}			1	μA	$V_{DD}-V_{SS}$=3.60 V
High Level Input Voltage	V_{IH}	0.8 V_{DD}		V_{DD}	V	
Low Level Input Voltage	V_{IL}	V_{SS}		0.2 V_{DD}	V	
Oscillation Starting Voltage	V_{STA}	2.0			V	T_{STA}= 10 s

* TP and DATA OUT are N-channel open drain output.

A.C. ELECTRICAL CHARACTERISTICS (FOR REFERENCE - - - NOT SPECIFIED)

(f = 32.768 kHz, $V_{DD}-V_{SS}$ = 2.0 V, Ta = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_0~2, CS – STB Set-up Time	t_{SU}	2			μs	
STB Pulse Width	T_{STB}	2			μs	
C_0~2, CS–STB Hold Time	T_{HLD}	2			μs	
STB LATCH Delay Time	t_{d1}			*4	μs	except Time Read mode
CLK–DATA OUT Delay Time	t_{dc-o}			2	μs	R_L=33 kΩ, C_L=15 pF
DATA IN Set-up Time	t_{DSU}	2			μs	
DATA IN Hold Time	t_{DHLD}	2			μs	

* Note: When group 0 is Time Read mode, STB LATCH delay time is 40 μs MAX. (t_{d2}).

1-6. Command

REGISTER CONTROL MODE GROUP [Group 0]

C2 = 0

MODE & COMMAND	CODE C2 C1 C0	FUNCTION	DATA OUT
REGISTER HOLD	0 0 0	Data of 40 Bit S/R are not shifted, and data is held. The TEST MODE is released by this command.	1 Hz
REGISTER SHIFT	0 0 1	Data of the 40 Bit S/R can be shifted to Data OUT terminal and the external data can be shifted to the 40 Bit S/R, each synchronizing with a clock input at the CLK terminal.	LSB = 0 or 1
TIME SET	0 1 0	Data of the 40 Bit S/R are not shifted. The T/C is kept to transfer data from the 40 Bit S/R and the 11 – 15 stage remains reset. Set a command (ie. 000, 001, 011) besides this command to start T/C.	LSB = 0 or 1
TIME READ	0 1 1	Data of 40 Bit S/R are not shifted. Data of the T/C keep to transfer to the 40 Bit S/R.	0.5 Hz

note S/R: Shift Register
T/C: Time Counter

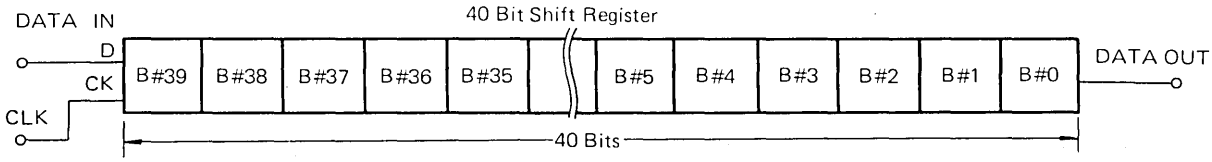
Only to change TIME READ mode to another mode, the time to be changed another mode has to need 40 μs MAX. ($=t_{d2}$) from the rising edge of STB pulse for setting a new command.

TP CONTROL MODE AND TEST MODE GROUP [Group 1]

C2 = 1

MODE & COMMAND	CODE C2 C1 C0	FUNCTION
TP = 64 Hz	1 0 0	TP terminal is the 64 Hz output.
TP = 256 Hz	1 0 1	TP terminal is the 256 Hz output.
TP = 2 048 Hz	1 1 0	TP terminal is the 2 048 Hz output.
TEST MODE	1 1 1	In this mode, TP terminal is the 32 Hz output. The TEST MODE is released by TP MODE (100, 101, 110) or REGISTER HOLD MODE (000). When is released by MODE (000), TP terminal is 64 Hz output.

1-7. The correspondence of the data between the 40 Bit Shift Register and the Time Counter.

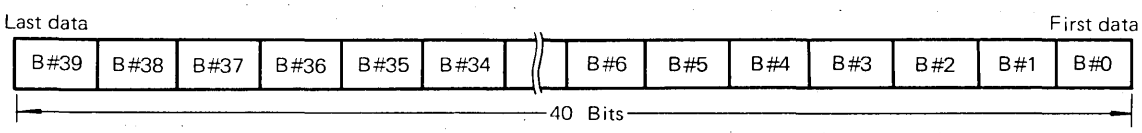


40 Bit Shift Register	Time Counter	Data of Time Counter
B#0	B#0 (LSB) of Seconds/Units	0 through 9
B#1	B#1 "	(BCD)
B#2	B#2 "	
B#3	B#3 (MSB) "	
B#4	B#0 (LSB) of Seconds/Tens	0 through 5
B#5	B#1 "	(BCD)
B#6	B#2 (MSB) "	
B#7	0	
B#8	B#0 (LSB) of Minutes/Units	0 through 9
B#9	B#1 "	(BCD)
B#10	B#2 "	
B#11	B#3 (MSB) "	
B#12	B#0 (LSB) of Minutes/Tens	0 through 5
B#13	B#1 "	(BCD)
B#14	B#2 (MSB) "	
B#15	0	
B#16	B#0 (LSB) of Hours/Units	0 through 9
B#17	B#1 "	(BCD)
B#18	B#2 "	
B#19	B#3 (MSB) "	
B#20	B#0 (LSB) of Hours/Tens	0 through 2
B#21	B#1 (MSB) "	(BCD)
B#22	0	
B#23	0	
B#24	B#0 (LSB) of Date/Units	0 through 9
B#25	B#1 "	(BCD)
B#26	B#2 "	
B#27	B#3 (MSB) "	
B#28	B#0 (LSB) of Date/Tens	0 through 3
B#29	B#1 (MSB) "	(BCD)
B#30	0	
B#31	0	
B#32	B#0 (LSB) of Day of Week	0 through 6
B#33	B#1 "	(BCD)
B#34	B#2 (MSB) "	
B#35	0	
B#36	B#0 (LSB) of Month	1 through 0CH
B#37	B#1 "	(Hexa Decimal)
B#38	B#2 "	
B#39	B#3 (MSB) "	

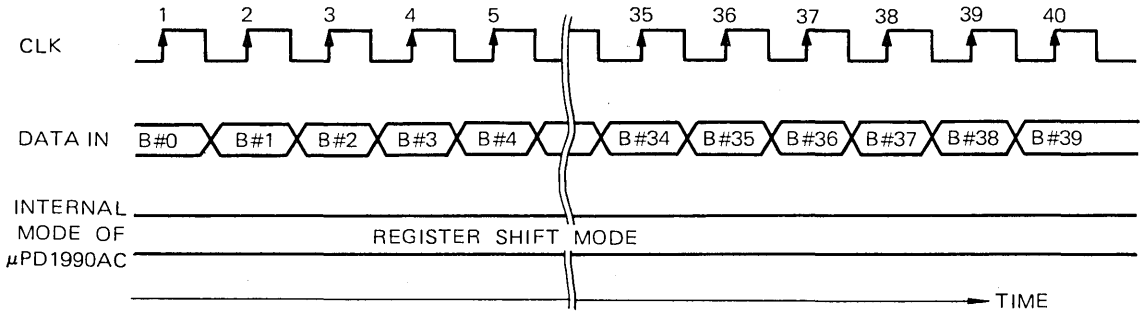
1-8. The form of loading and reading the data

● Loading of data to 40 Bit Shift Register in μPD1990AC.

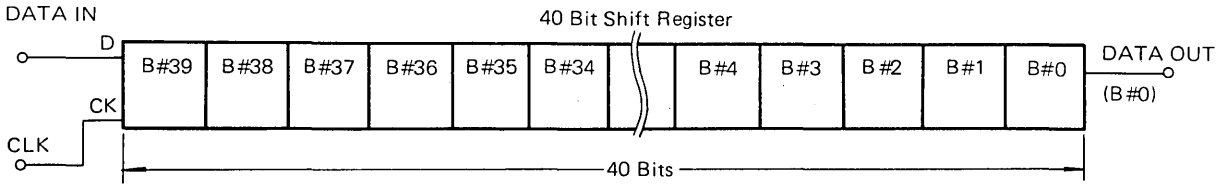
1. It is defined the external serial data loading to 40 Bit Shift Register of the μPD1990AC as follows,



2. Loading operation. (The μPD1990AC is in the Register Shift mode.)

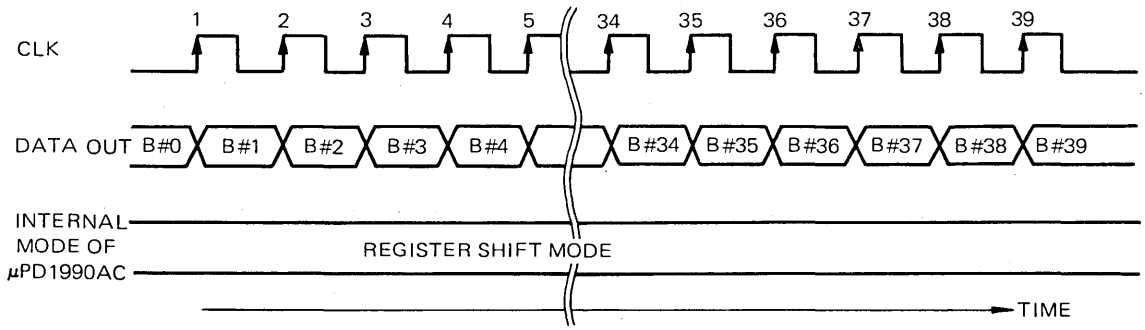


3. Data of 40 Bit Shift Register in the μPD1990AC, after loading operation



● Reading the data of 40 Bit Shift Register in the μPD1990AC.

1. Reading operation. (In the Register Shift mode.)



1-9. INPUT AND OUTPUT CIRCUITS FOR μPD1990AC

Input circuits
(for C2, C1, C0, STB, DATA IN, CLK, OUT ENBL, CS terminals)

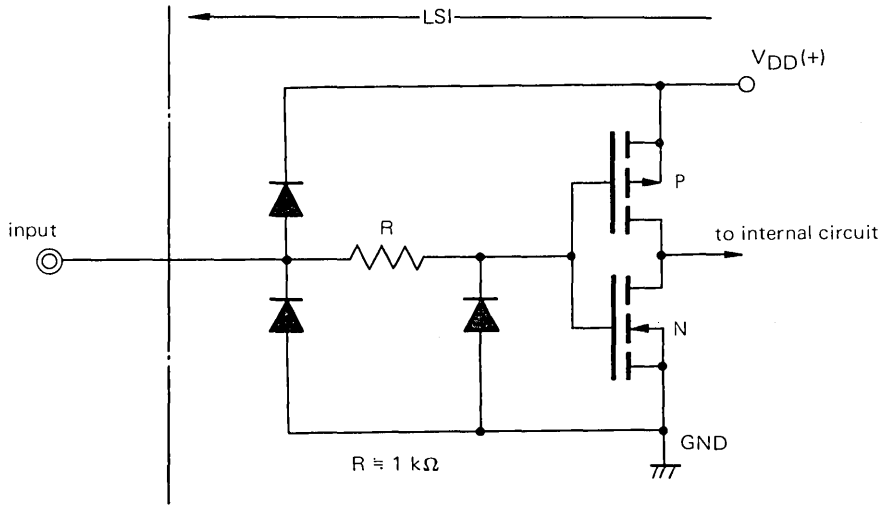


Fig. 11

Output circuits
(for DATA OUT, TP terminals)

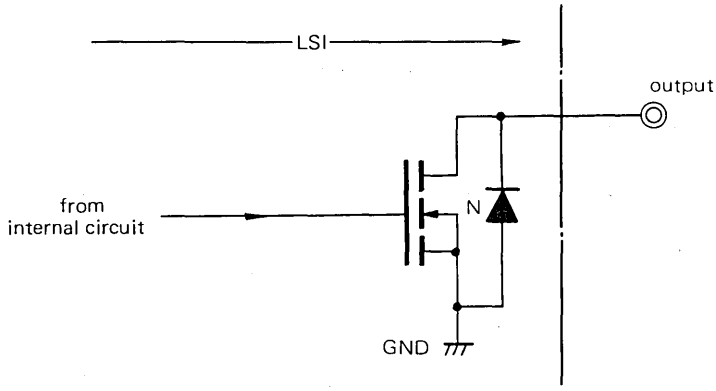


Fig. 12

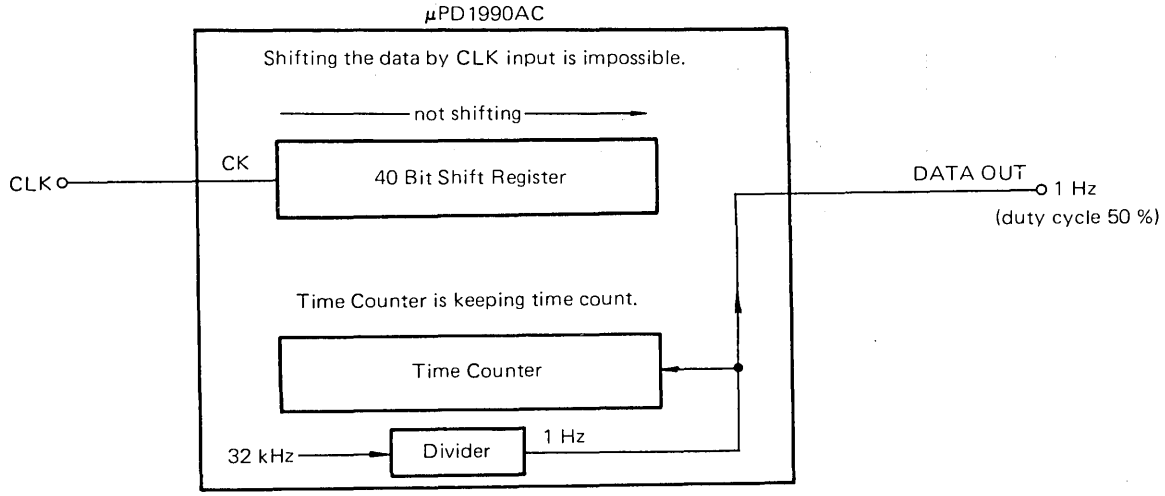
2. COMMAND DESCRIPTION

2-1. Register control modes. [Group "0"]

These mode are set by Register Control command which does not affect with TP (Timing Pulse) control mode. [Group "1"].

★ **Register Hold Mode (Set by Register Hold Command (000))**

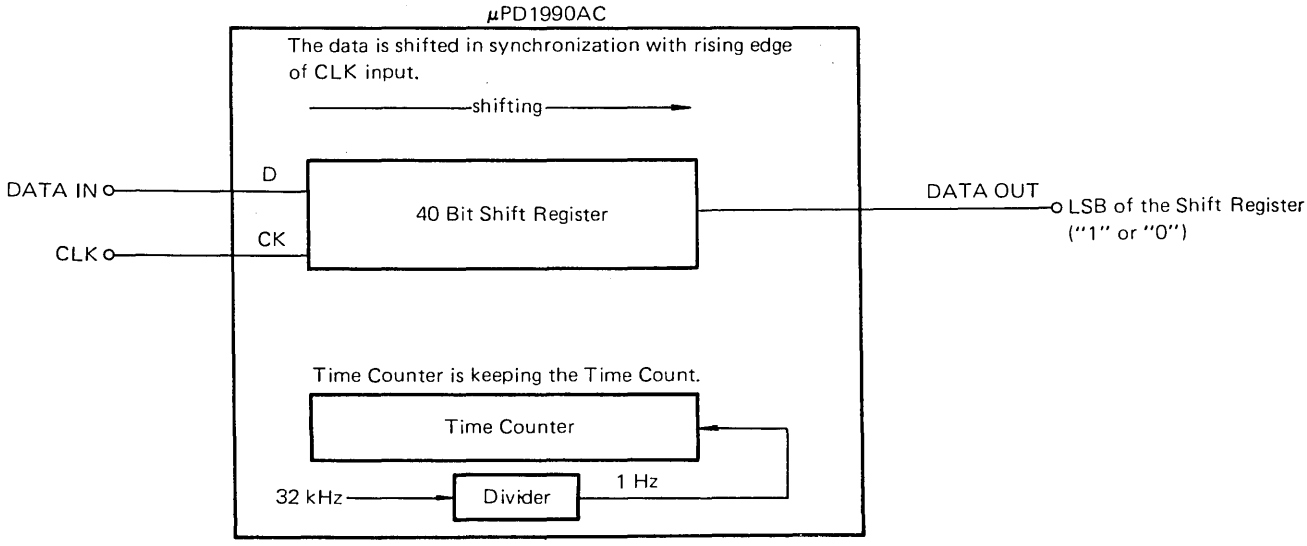
It is impossible for the data of the 40 Bit Shift Register to shift during in this mode. And the 1 Hz signal is provided at DATA OUT terminal.



note When μPD1990AC is in TEST MODE (Group "1") by setting this mode the μPD1990AC is released from TEST MODE and set TP = 64 Hz mode.

★ **Register Shift Mode (Set by Register Shift Command (001))**

Only in this mode, it is possible for the data of 40 Bit Shift Register to shift in synchronization with rising edge of CLK clock input.



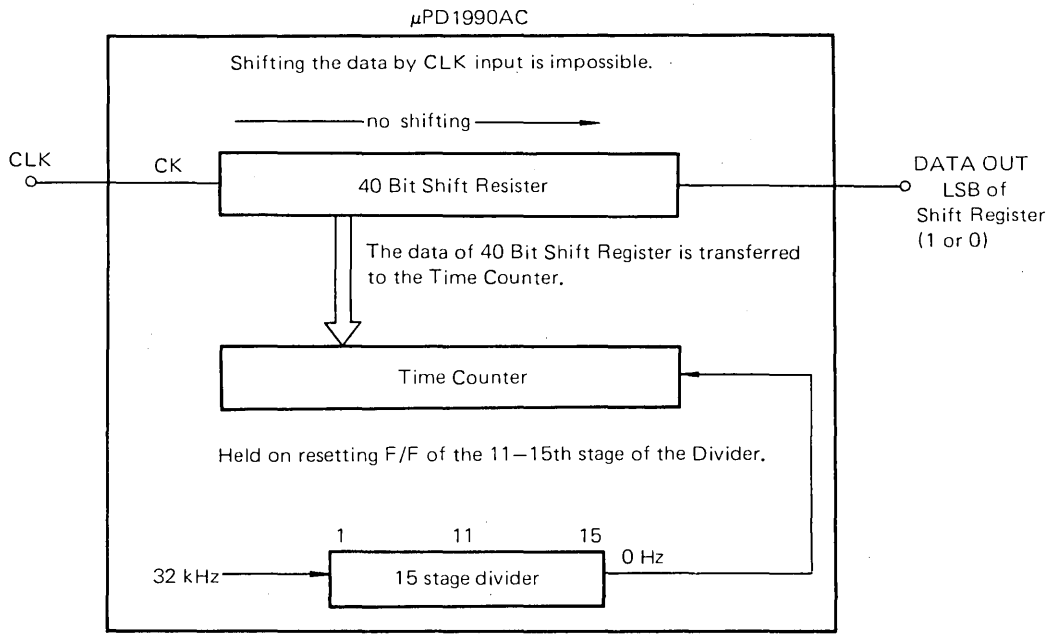
note When is set the Register Shift command "001", input level of the CLK terminal has to be low level.

The logic level present at the DATA IN input is transferred into the first register stage and shifted over one stage at each positive-going clock transition of CLK terminal. And data of the last register stage (=LSB) is provided at DATA OUT terminal.

★ **Time Set mode. (Set by Time Set command (010))**

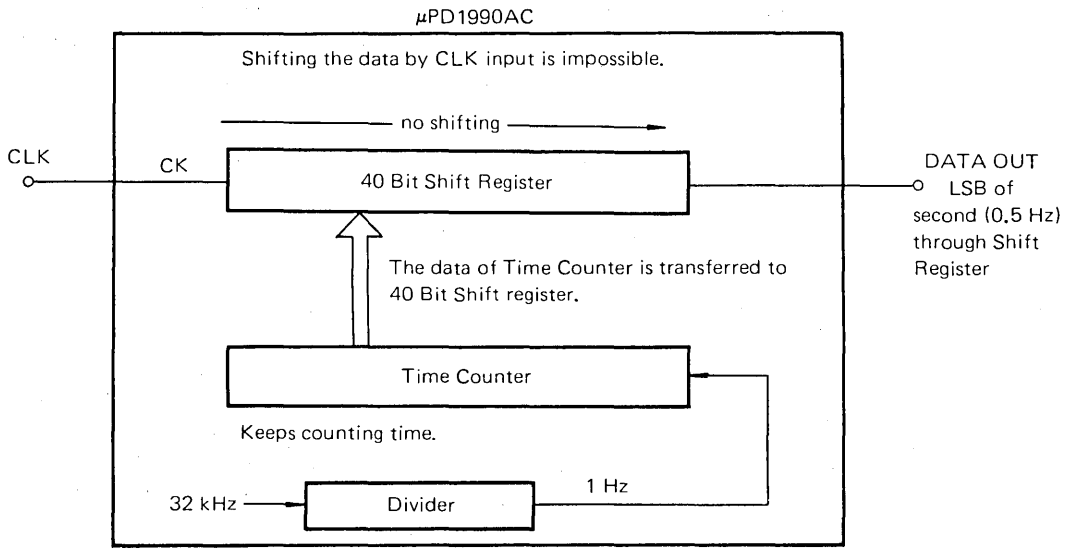
The data of 40 Bit Shift Register is transferred to Time Counter, and is reset the flip-flop of the 11th – 15th stage in the 15 Stage Binary Divider and held the Time Counter.

As soon as the μPD1990AC is released from the Time Set mode, by setting another Register Control command, such as Register Hold, Register Shift or Time Read commands, the Time Counter will be started to keep time.



★ **Time Read mode. (Set by Time Read command (011))**

The data of the Time Counter is transferred to the 40 Bit Shift Register. LSB of the units of seconds (0.5 Hz) output is provided at DATA OUT terminal through the 40 Bit Shift Register.



note: When μPD1990AC is in the Time Read mode, another new mode becomes to enable after 40 μs (MAX.) from the rising edge of STB pulse for setting the new command, because the new mode is delayed to synchronize with the highest frequency (ie. 32.768 kHz) in the μPD1990AC.

2-2. TP (Timing Pulse) Control mode and TEST mode

These modes are controlled only by TP control commands and TEST MODE set command, which does not affect Register Control modes. [Group "0"]

★ **TP=64 Hz mode. (Set by TP=64 Hz command (100))**
The TP terminal is the output of 64 Hz.

★ **TP=256 Hz mode. (Set by TP=256 Hz command (101))**
The TP terminal is the output of 256 Hz.

★ **TP=2 048 Hz mode. (Set by TP=2 048 Hz command (110))**
The TP terminals is the output of 2 048 Hz.

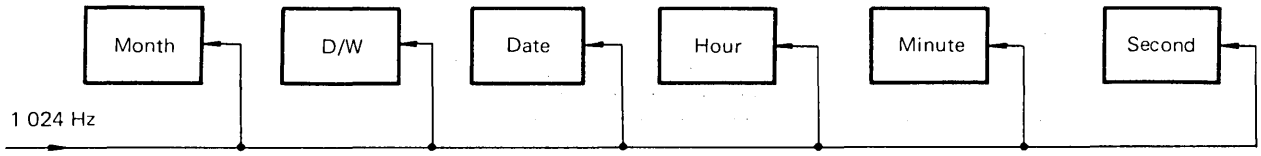
★ **TEST MODE. (Set by TEST mode of command (111))**
This mode set the μPD1990AC to LSI TEST mode. (not to be used for ordinary operation)

TEST MODE (Set by command of TEST mode (111))

In this mode, DATA OUT terminal is enabled regardless of OUT ENBL input.
There are 2 type TEST MODE to be selected by OUT ENBL terminal.
While μPD1990AC is in Register Hold mode, impossible to chage Test mode by setting TEST MODE COMMAND(111)

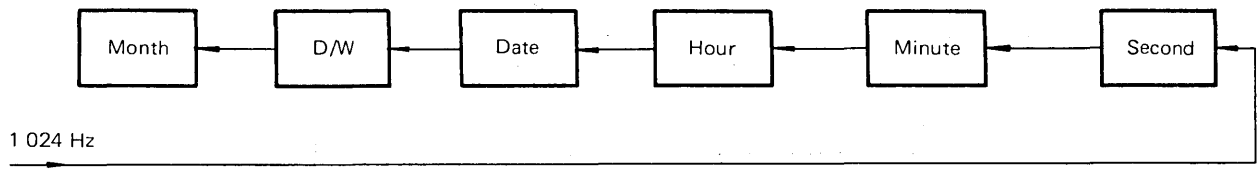
TEST MODE 1 ; OUT ENBL=0

In this mode, every Counter ("Month", "Day of Week", "Date", "Hour", "Minute", "Second") is advanced at a 1 024 Hz rate in parallel. In this case the overflow carry of each counter is not affect to the next counter.



TEST MODE 2 ; OUT ENBL = 1

In this mode TIME COUNTER is advanced at a 1 024 Hz rate in stead of 1 Hz for Second counter input.



The following table shows the signals to be provided at DATA OUT and TP terminals during the μPD1990AC is in the TEST MODE.

MODE	CODE C2 C1 C0	DATA OUT	TP		
REGISTER HOLD	0 0 0	1 Hz	64 Hz	By this command, TEST MODE is released.	
REGISTER SHIFT	0 0 1	LSB of 40 Bit S/R "0" or "1"	32 Hz	TEST MODE is re-mained.	T/C is advanced at 1 024 Hz in parallel or serial.
TIME SET	0 1 0	LSB of 40 Bit S/R "0" or "1"	32 Hz		
TIME READ	0 1 1	512 Hz	32 Hz		T/C is advanced at 1 024 Hz in parallel or serial.

note. While μPD1990AC is TEST mode, by setting the Register Hold mode (Group "0" mode), Test Mode changes TP=64 Hz mode in group "1" and as a result Register Hold mode is set. There is a 1 Hz output at DATA OUT terminal and a 64 Hz output at TP terminal.

3. SOFTWARE FOR μPD1990AC

The commands for μPD1990AC are formed with 3 bits of C_0, C_1, and C_2, and composed of 8 commands: 4 register control commands (time data read and write), 3 timing pulse (64 Hz, 256 Hz, 2,048 Hz) select commands and 1 IC test mode command. The command specifications are shown below.

Each command latches groups 0 and 1 separately with a strobe input (STB).

- Command input.
  - 3 bit, binary code input. C_0, C_1, C_2
- Number of commands.
  - Register control 4
  - TP control 3
  - TEST MODE set 1

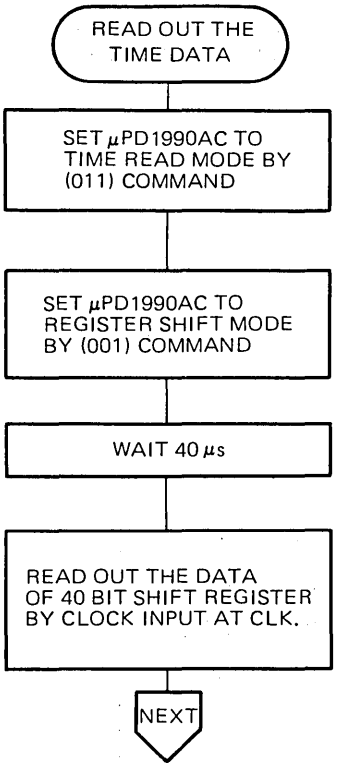
  ] 8

COMMAND SPECIFICATIONS

Group	C_2	C_1	C_0	FUNCTION	
0	0	0	0	Register Hold	DATA OUT = 1 Hz
	0	0	1	Register Shift	DATA OUT = [LSB]
	0	1	0	Time Set & Counter Hold	DATA OUT = [LSB]
	0	1	1	Time Read	DATA OUT = 0.5 Hz
1	1	0	0	TP = 64 Hz Set	
	1	0	1	TP = 256 Hz Set	
	1	1	0	TP = 2 048 Set	
	1	1	1	TEST MODE Set	

* Groups "0" and "1" hold their functions independently, in other word, the command of the group "0" ("1") can change the group "0" ("1") function mode only. Then you must release the μPD1990AC from TEST MODE by setting commands of TP selection (group "1") or Register Hold Mode.

3-1. How to read out the Time Data from the μPD1990AC.

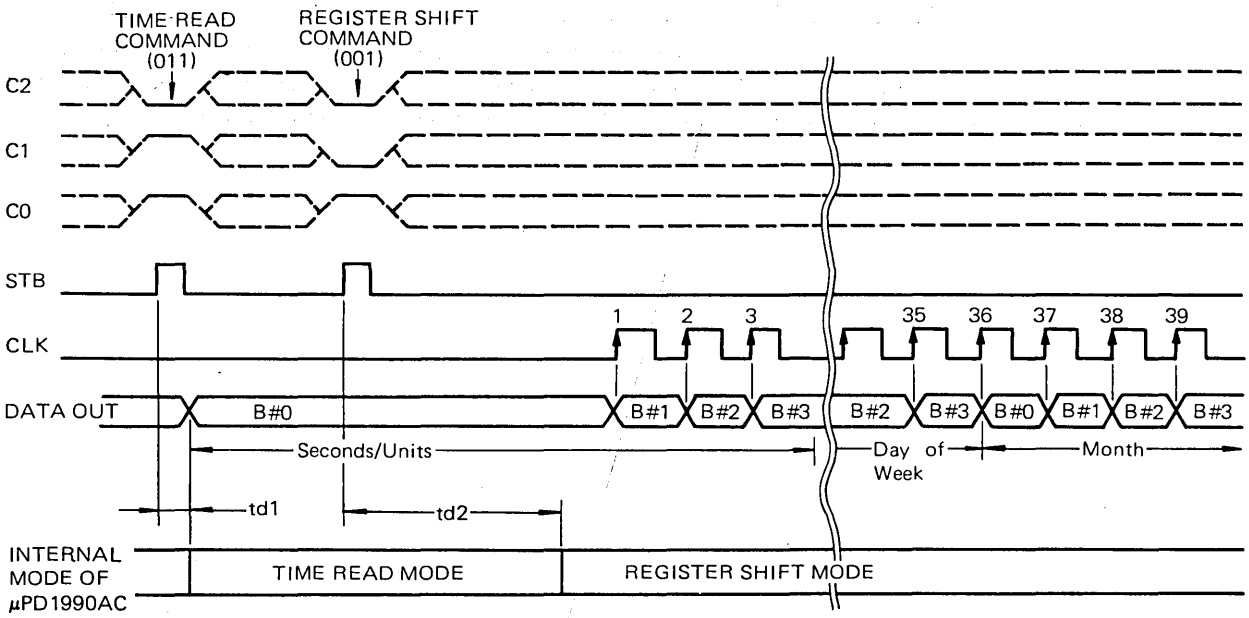


The data of the Time Counter (=Time Data) is transferred to the 40 Bit Shift Register.
But the data of 40 Bit Shift Register cannot be shifted by the clock input at CLK terminal.

The data of 40 Bit Shift Register (=Time Data) can be shifted by the clock input at CLK terminal.

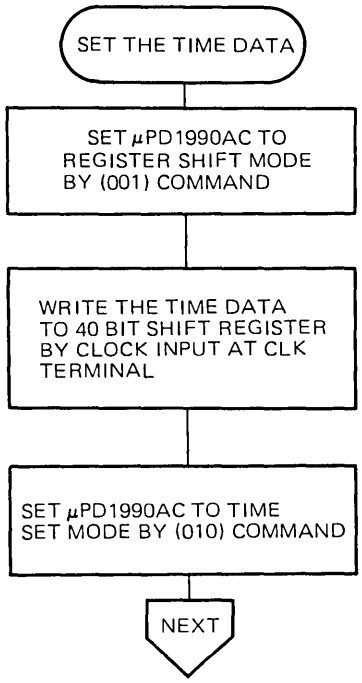
Wait 40 μs until the Register Shift mode becomes valid.

The data of the 40 Bit Shift Register (=Time Data) is shifted to DATA OUT terminal in synchronization with the rising edge of the clock input at CLK terminal.



Note: td1=4 μs (Delay time of μPD1990AC being in the ordinaly mode)
td2=40 μs (Delay time of μPD1990AC being in the Time Read mode)

3-2. How to set the Time Data to the μPD1990AC (Time Data Time Counter of the μPD1990AC)



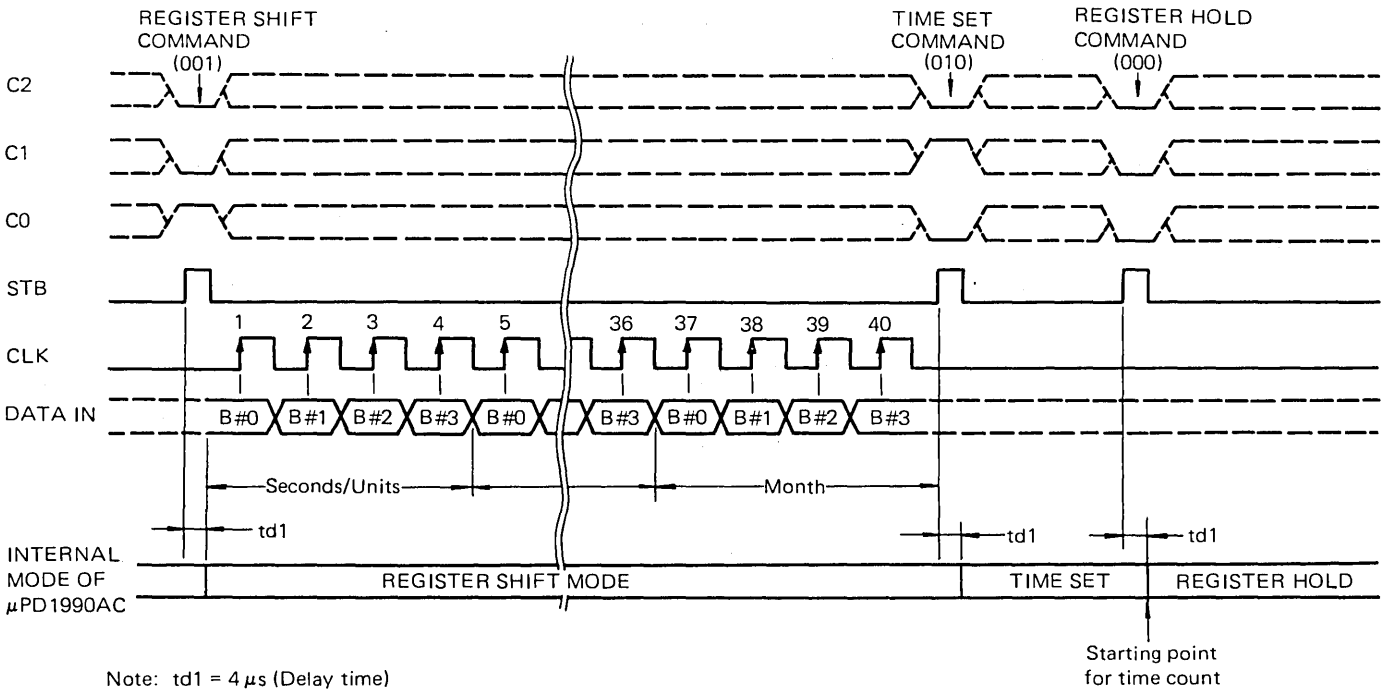
The data of 40 Bit Shift Register can be shifted by the clock input at CLK terminal.

Note: When is set Register Shift mode command (001), input level of CLK has to be low level.

Time Data is loaded to 40 Bit Shift Register by setting serial data at DATA IN terminal in synchronization with rising edge of clock input at CLK terminal.

The data of 40 Bit Shift Register (Time Data) is transferred to Time Counter. And Time Counter is kept on being held, during Time Set mode.

Note: As soon as Time Set mode is released by setting Register Hold (000), Register Shift (001) or Time Read (011) command, the Time Counter will start to count time.



Note: td1 = 4 μs (Delay time)

4. INTERFACES FOR μPD1990AC

The following is the Block diagram interface between μPD1990AC and CPU SYSTEM.

(1) Crystal oscillator circuit
(2) Power supply circuit
(3) Output interface
(4) Input interface
(5) CS interface

APPLICATION CIRCUIT

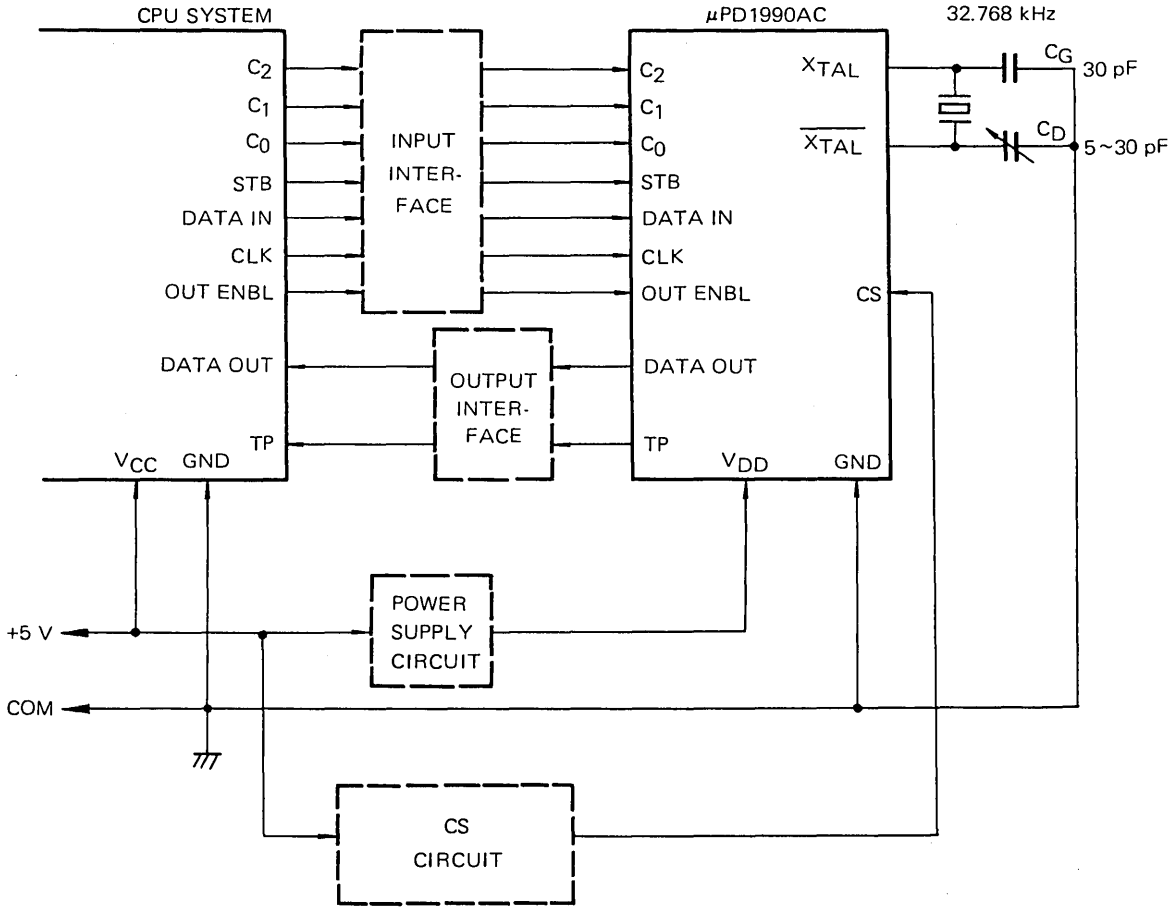


Fig. 4

4-1. Crystal oscillator circuit

The oscillator circuit of the μPD1190AC is of one-stage CMOS inverter system, incorporating a feedback resistor for bias. A crystal oscillator of nominal 32.768 kHz is connected between Xtal (13th pin) and $\overline{\text{Xtal}}$ (12th pin).

A C_G=about 30 pF capacitor is connected between Xtal (13th pin) and V_{SS} (GND) and a C_D=5~30 pF trimmer capacitor, between $\overline{\text{Xtal}}$ (12th pin) and V_{SS} (GND). Crystal oscillator frequency deviation and variation in capacitor C_G and floating capacity at the oscillating stage cause a discrepancy between the actual and nominal oscillation frequencies. To adjust this, the $\overline{\text{Xtal}}$ (12th pin) capacitor uses a variable capacitor.

Crystal Oscillator Circuit

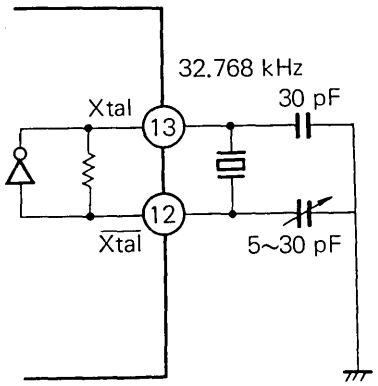


Fig. 5

4-2. Power supply circuit

Originally, the time keeper ought to continue to count the time accurately even though power fails or its AC cord is misremoved from the socket outlet or the system power is turned off. From this point of view, the power supply circuit of the μPD1990AC must be of battery-backed up type.

The μPD1990AC can use a battery of any type as a power source if its voltage is in a 2.0 through 5.5 V operating voltage range.

For reference, the following shows a example of circuit using Ni-Cd batteries (easy to charge).

POWER SUPPLY CIRCUIT

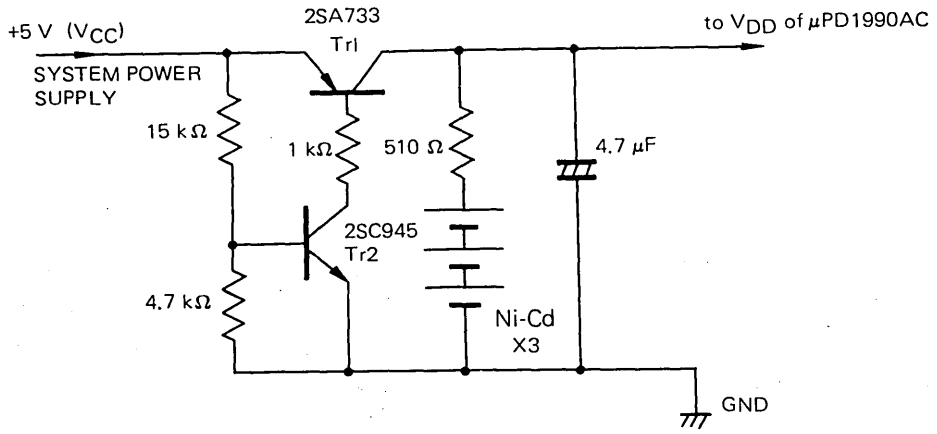


Fig. 6

SYSTEM POWER SUPPLY = "ON"
μPD1990AC is operated by System Power Supply (about 5 V).

SYSTEM POWER SUPPLY = "OFF"
μPD1990AC is operated by about Ni-Cd batteries (about 3.6 V).

4-3. Interface for output circuit

The output circuit (DATA OUT and TP) of the μPD1990AC has N-channel open-drain outputs as shown.

To form an interface with the system, insert a pull-up resistor, R_{pu}, between the system power supply V_{CC}, and the output terminal.

Notice that a low-level output current of $I_{OL}=(V_{CC}-V_{DS})/R_{pu}/\!/R_S$ (μA) flows in accordance with Ohm's law.

Decide the pull-up resistor value R_{pu} so as to balance it against the low level output current and other conditions.

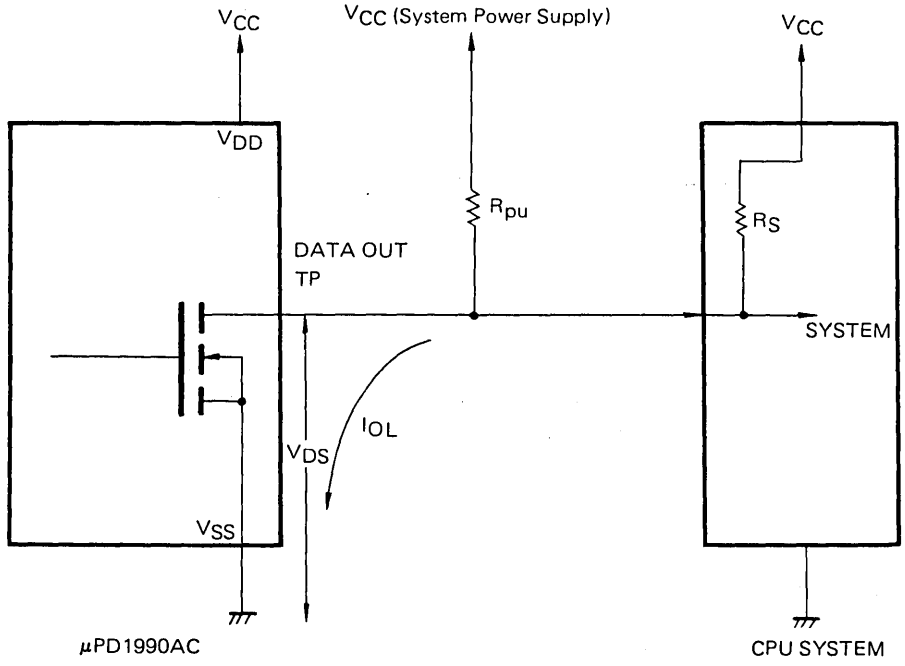


Fig. 7

4-4. Interface for input circuit

(a) Terminals of C_2, C_1, C_0, CLK, DATA IN, and OUT ENBL

To form an interface with the system, insert a pull-up resistor R_{pu} between the system power supply V_{CC} and the input terminal.

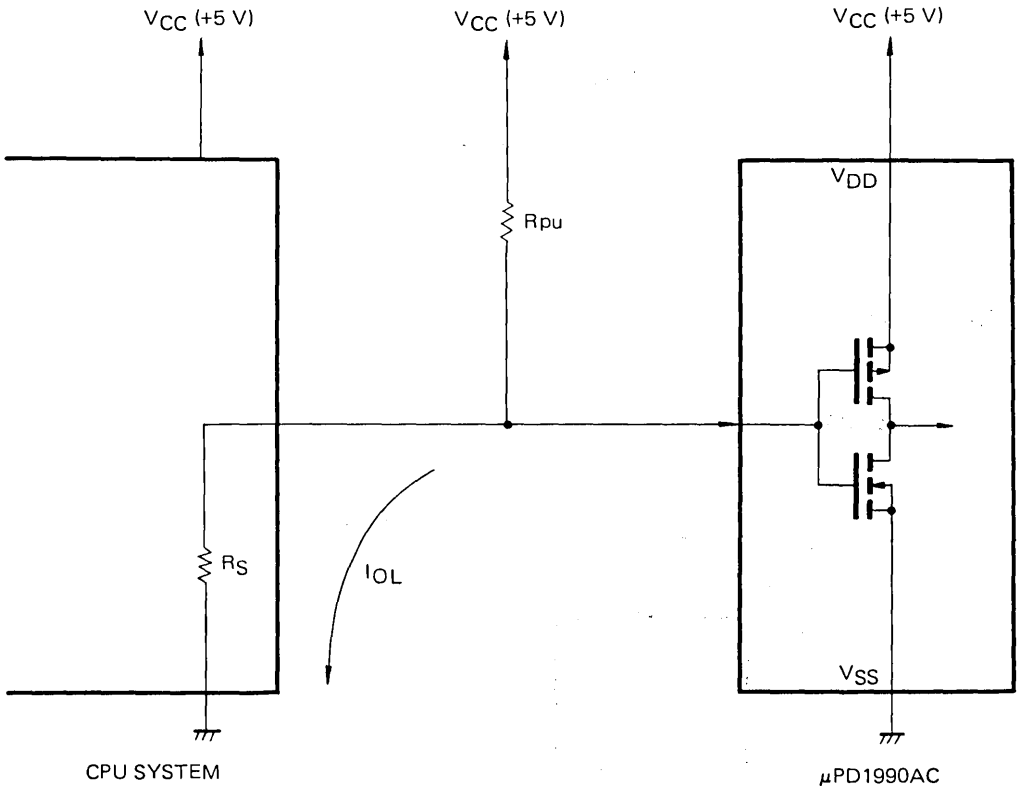


Fig. 8

Notice that a leakage current (CPU SYSTEM) of I_{OL} flows in accordance with Ohm's law.
Decide the pull-up resistor value Rpu as following.

$$Rpu \leqq \frac{5 - 3.5}{I_{OL}}$$

5 V: Power-supply (V_{CC})
3.5 V: Minimum of high level input voltage in μPD1990AC

(b) Terminal of STB

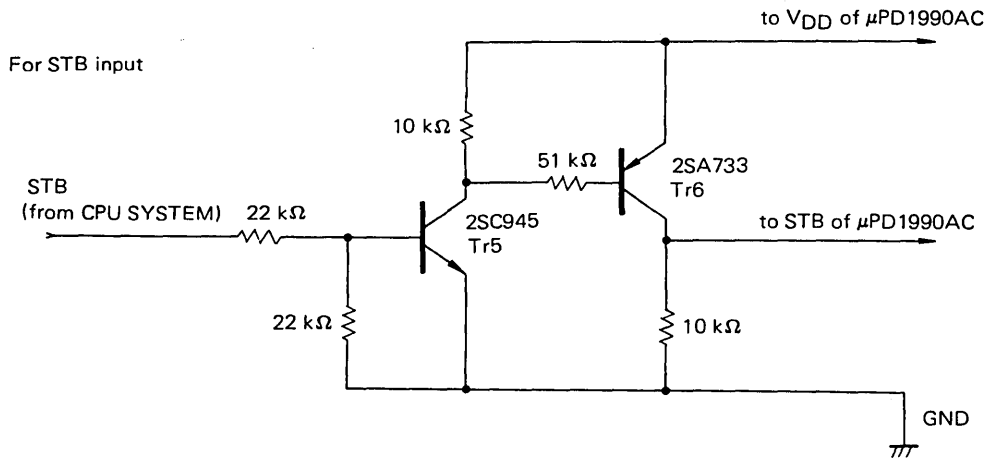


Fig. 9

The STB input is low when the CPU system output is floating and when the CPU system is off.

4-5. Interface for CS terminal

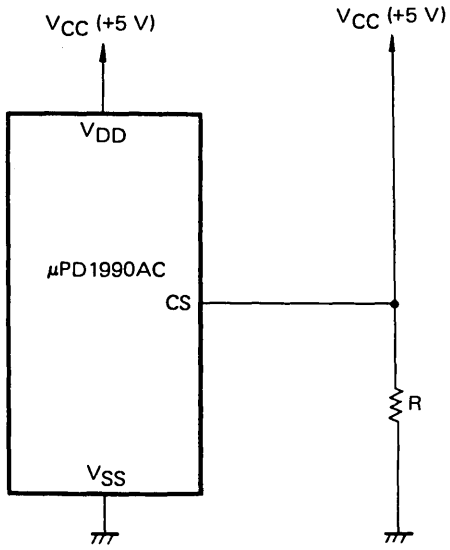


Fig. 10

A pull-down resistor R is inserted so that the CS input is low when the power supply (V_{CC}) is off. And the CLK and STB input prohibited by connecting CS input to GND level.

4-6. Example of application circuit

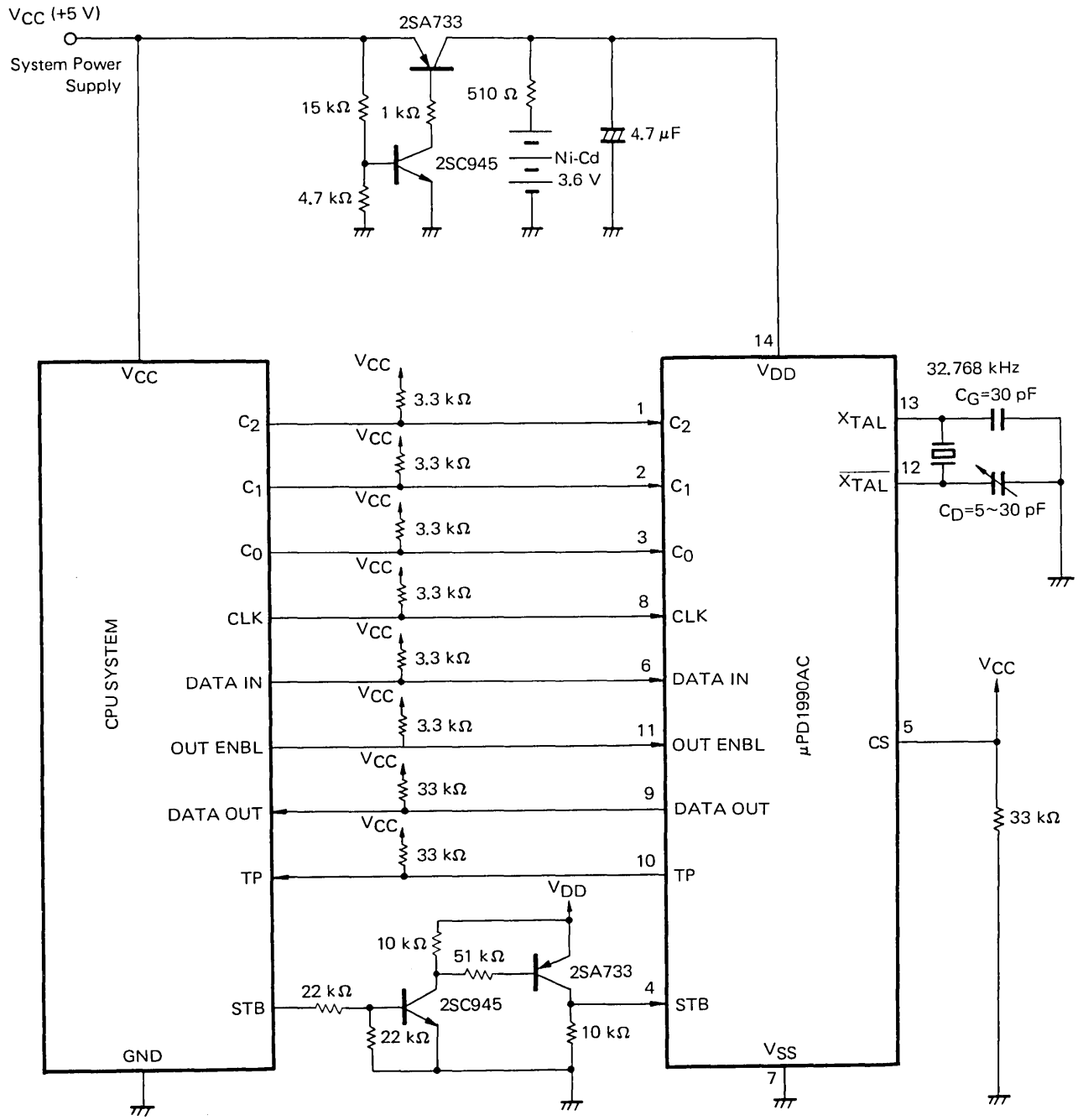


Fig. 13

APPLICATION CIRCUIT OF μPC7800H SERIES 3-TERMINAL REGULATORS

1. INTRODUCTION

The manufacturing and circuit design techniques of integrated circuits have made rapid and remarkable progress in recent years. NEC has released 3-terminal regulators (μPC7800H series) featuring an output current capability of 1 A, low noise and excellent stability. The regulators are available in fixed output voltages options 5 V, 8 V, 12 V, 15 V, 18 V and 24 V with standard TO-220 plastic package. As they have built-in current limiting circuit, thermal shut-down circuit and safe area compensation circuit, these monolithic circuits are very easy to use in various applications.

2. ABSOLUTE MAXIMUM RATINGS

Although μPC7800H series include various protective circuits, it is necessary to examine the design of the application circuits so that they can operate within the absolute maximum ratings shown in Table 1.

Table 1 Absolute Maximum Ratings
(Ta=25 °C, unless otherwise noted.)

ITEM	SYMBOL	RATINGS	UNIT
Input Voltage	V_{IN}	(μPC7805H through μPC7818H) 35	V
		(μPC7824H) 40	V
Internal Power Dissipation	P_T(Tc=25 °C)	20 *	W
Operating Temperature Range	Topt	−20 to +80	°C
Storage Temperature Range	Tstg	−55 to +150	°C
Lead Temperature (Soldering 10 sec.)	T_L	230	°C
Operating Junction Temperature Range		0 to +125	°C

* Internally Limited

3. EQUIVALENT CIRCUIT AND THE OPERATION OF THE CIRCUIT

3-1 Equivalent Circuit

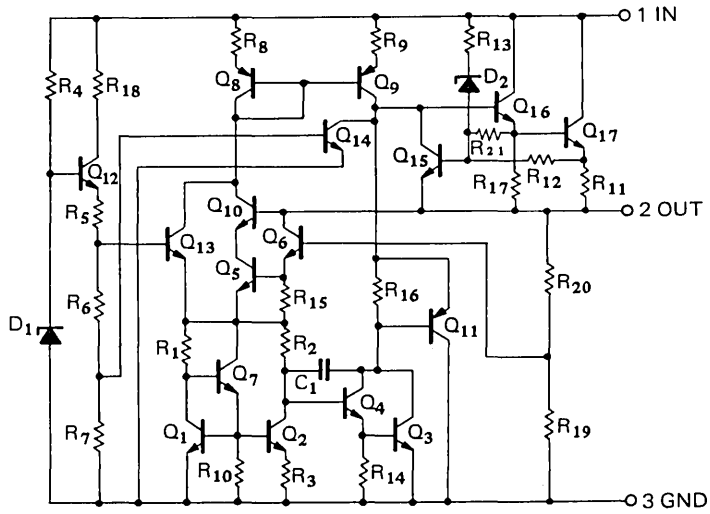


Fig. 1 Equivalent circuit

3-2 Fundamental Block Diagram

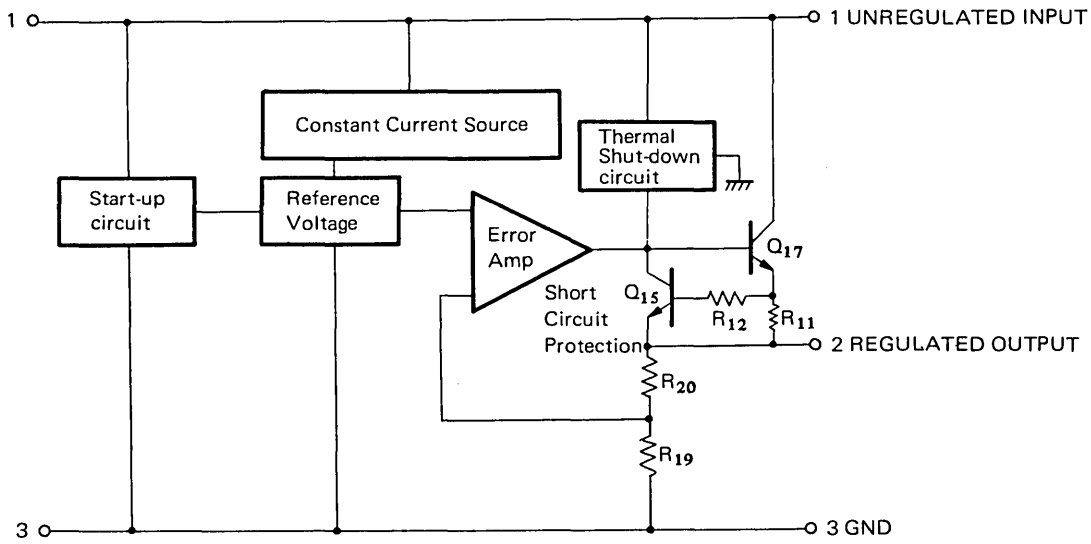


Fig. 2 Fundamental Block diagram of the 3-terminal regulator

3-3 Pin Connection

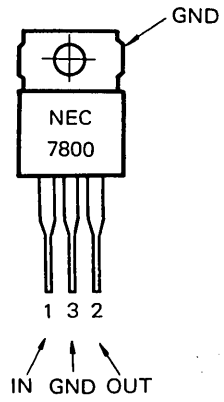


Fig. 3 Pin connection

3-4 Reference Voltage Circuit

The reverse breakdown voltage between the base and the emitter of a transistor has continuously been utilized as the reference voltage inside the monolithic IC. It is, however, difficult for this method to obtain a voltage of less than 6 V, and thus, the temperature compensation is required by adding another circuit. Instead of that conventional technique, the μPC7800H series adopt a circuit utilizing the forward voltage drop between base and emitter of a transistor as shown in Fig.4 "Basic circuit" to get a reference voltage of lower than 6 V which remains relatively stable against temperature change.

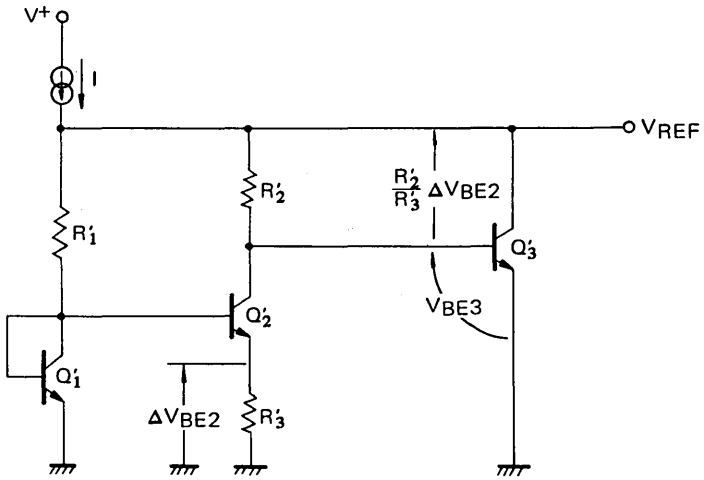


Fig. 4 Basic voltage reference diagram utilizing the forward voltage drop between base and emitter of a transistor

In the circuit shown in Fig.4, the reference voltage V_{REF} can be obtained as follows;

$$V_{REF} = V_{BE_3} + I_{CQ'_2} \cdot R'_2 + I_{BQ'_3} \cdot R'_2$$

$$= V_{BE_3} + \frac{R'_2}{R'_3}(\Delta V_{BE_2}) + I_{BQ'_3} \cdot R'_2$$

$$= V_{BE_3} + \frac{R'_2}{R'_3}\left(\frac{kT}{q} \ln \frac{J_1}{J_2}\right) + I_{BQ'_3} \cdot R'_2$$

$$\fallingdotseq V_{BE_3} + \frac{R'_2}{R'_3}\left(\frac{kT}{q} \ln \frac{R'_2}{R'_1}\right) \quad \cdots\cdots (1)$$

$(V_{BE_1} = V_{BE_2},\ I_{BQ'_3} \cdot R'_2 \ll 1$

Differentiating equation (1) by temperature T, equation (2) is obtained;

$$\frac{\partial V_{REF}}{\partial T} = \frac{\partial V_{BE_3}}{\partial T} + \frac{k}{q} \cdot \frac{R'_2}{R'_3} \ln\left(\frac{R'_2}{R'_1}\right) \quad \cdots\cdots (2)$$

It may be understood that the temperature compensated reference voltage can be obtained by selecting suitable resistance ratios R2'/R3' and R2'/R1'.

Fig. 5 shows the reference voltage circuit of μPC7800H series obtaining.

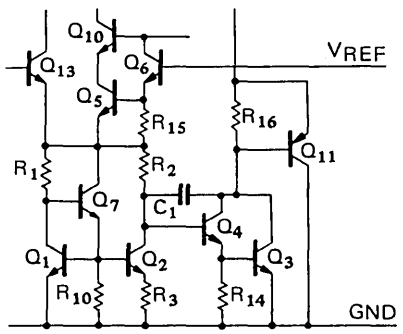


Fig. 5 V_{REF} circuit of μPC7800H series

3-5 Error Amplifier

The error amplifier consists of Q_3, Q_4, Q_9 and Q_{11}. Of these transistors, Q_3 and Q_4 compose the reference voltage circuit. Buffer circuit Q_{11} is added to eliminate an excessive current change of Q_9 which may be caused by considerable voltage change of unregulated input or load condition and to get better stability of the operating current finally. The constant current source consisting of Q_9 works as an active load of the error amplifier. A negative feedback path is provided through feedback resistors R_{19} and R_{20}, and the output voltage is given by the following equation;

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R_{20}}{R_{19}}\right) \quad \cdots\cdots (3)$$

Various output Voltage are obtained by varying the ratio of R_{20}/R_{19}.

3-6 Start-up Circuit and Thermal Overload Protection Circuit

Fig. 6 shows start-up circuit and thermal overload protection circuit.

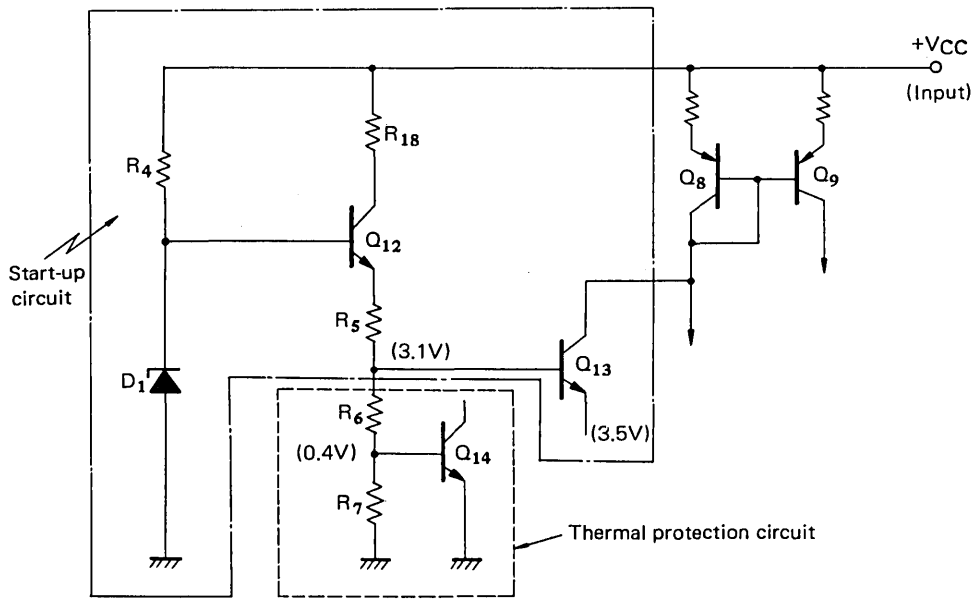


Fig. 6 Start-up Circuit and Thermal Overload Protection Circuit

When a voltage is applied to the input terminal, Q_{12} and Q_{13} are biased through R_4 causing diode-connected transistor Q_8 to be driven, and the constant current transistor Q_9 biased by Q_8 starts to supply the current to the reference voltage circuit enabling entire circuit to start operation. The Q_{13} base potential is determined according to the voltage of zener diode D_1 and the voltage split ratio of R_5, R_6, R_7 and is approximately 3.1V. On the other hand, the emitter potential of the transistor becomes about 3.5V due to the operation of the reference voltage circuit resulting 0.4V of reverse bias between the base and the emitter. Q_{13} operates at starting-up time only and then it stops operation.

And current is supplied to the reference voltage circuit through Q_8, Q_9. Also the base potential of Q_{14} is fixed to about 0.4V by the resistance split of R_5, R_6, R_7. If the junction temperature exceeds 150°C, Q_{14} is fully turned on causing the base current of the output transistors Q_{16}, Q_{17} to decrease and also cutting the output current.

3-7 Output Short-circuit Protection, Output Transistor Safe Area Compensation

The thermal overload protection circuit is effective for persistent overloads which would cause excessive chip temperature. It is not effective against instantaneous overloads which could result in secondary breakdown of the pass transistor or damage to metal interconnection due to high current density. Transistor Q_{15} and resistor R_{11} protect against instantaneous overloads by limiting output current. If the output current rises to a high level, the current through R_{11} will turn on Q_{15} shunting base current away from the driver transistor and preventing further increase in output current. In order to operate the power transistor in the output stage within its forward safe area, a power limiting circuit is built in as shown in Fig. 7.

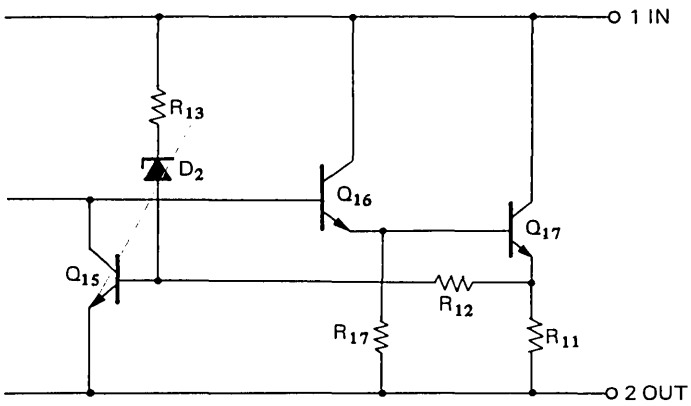


Fig. 7 Circuit of Output Stage

When the voltage between collector and emitter of Q_{17} exceeds 8V, zener diode D_2 conducts and biases the output current limiting transistor Q_{15}, cutting the base current of Q_{16}, Q_{17} and also cutting the output current.

Accordingly, the output capacity decreases correspondingly as the input/output voltage differential becomes larger, causing Q_{17} to be operated within the safe operating area as shown in Fig. 8.

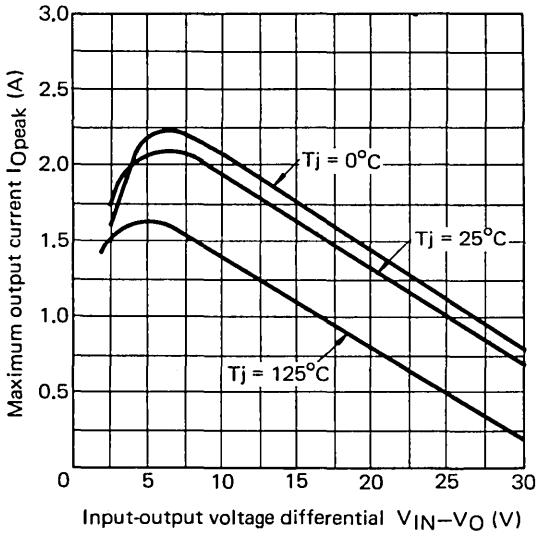


Fig. 8 Maximum output current vs input-output voltage differential

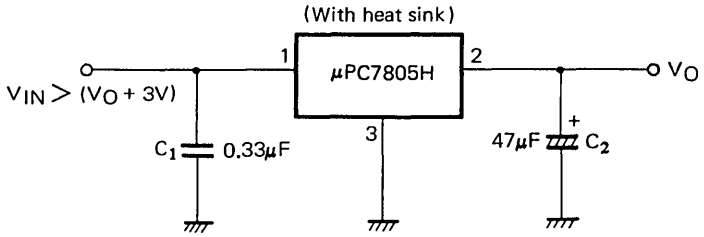
4. TYPICAL APPLICATIONS

The μPC7800H series has an output current capacity of 1A within a range of $T_j<100$ °C, and stable output voltage is obtained by connecting a capacitor of more than 0.22 μF to the input terminal for preventing oscillation. The output terminal capacitor is necessary to improve the transient response. It is effective at 10 μF or more. A suitable value ranges from 50 μF to 100 μF.

In order to operate these regulators under the best condition, it is desirable to operate them at a junction temperature of lower than 125 °C. Accordingly, it is necessary to use them with a suitable heat sink. If no heat sink is used, the load current should be under 200 mA. In this case, a resistor of more than 50 Ω should be connected to the input terminal to reduce a power loss at the time of output short-circuit.

Although the application circuits in this section are based on only μPC7805H, they can also be applied to 8 V, 12 V, 15 V regulators.

4-1 Typical Circuit



C_1: Mount closely to the input terminal for preventing oscillation (recommend mylarfilm type capacitors)
C_2: Improves transient response (electrolythic capacitor)

Fig. 9 Typical circuit of 3-terminal regulator

Fig. 9 is an example of typical application circuits of 3-terminal regulators. This circuit operates as a regulated power supply having an output voltage of 5 V and an output current capacity of 1 A.

4-2 High output current circuit

Fig. 10 shows a circuit example of increasing the output current capacity to higher than 2 A by adding a PNP power transistor. The maximum output current is limited by the power dissipation of the external transistor, and it is about 3 A taking the maximum ratings of 2SB616 into consideration.

Determine the R_1 value from equation (6)

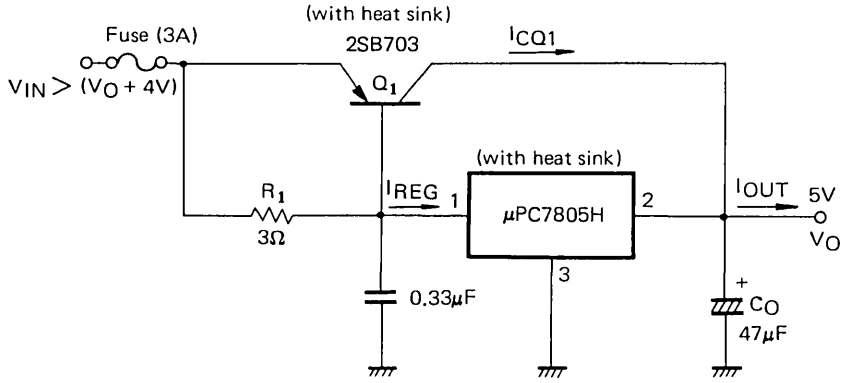
$$I_{OUT} = I_{REG} + I_{CQ_1} \quad \cdots\cdots (4)$$

$$I_{REG} = \frac{V_{BEQ_1}}{R_1} + \frac{I_{CQ_1}}{h_{FE}} \quad \cdots\cdots (5)$$

Rearraging equations (4) and (5) with reference to R_1;

$$R_1 = \frac{h_{FE} \cdot V_{BEQ_1}}{(1 + h_{FE}) \cdot I_{REG} - I_{OUT}} \quad \cdots\cdots (6)$$

Assuming $I_{out(max)} = 3$ A, $I_{reg(max)} = 0.4$ A, $h_{FE} = 20$ and R_1 is about 2.6 Ω.
A suitable value of R_1 is about 1~3 Ω.



NOTE: Q_1 may be broken by output short circuit. If there is possibility of shortening the load, refer to examples of application circuits in Figs. 12 and 13, and also please note to use a heat sink with enough margin.

Fig. 10 Circuit example of increasing the output current

When the output current is less than 0.2 A, Q_1 is OFF, and the output current is supplied through R_1 and the IC. When it exceeds 0.2 A, it is supplied through not only the IC but also Q_1. Fig.11 shows a current buffer circuit obtained by adding a current limiting protective circuit to the one shown in Fig.10.

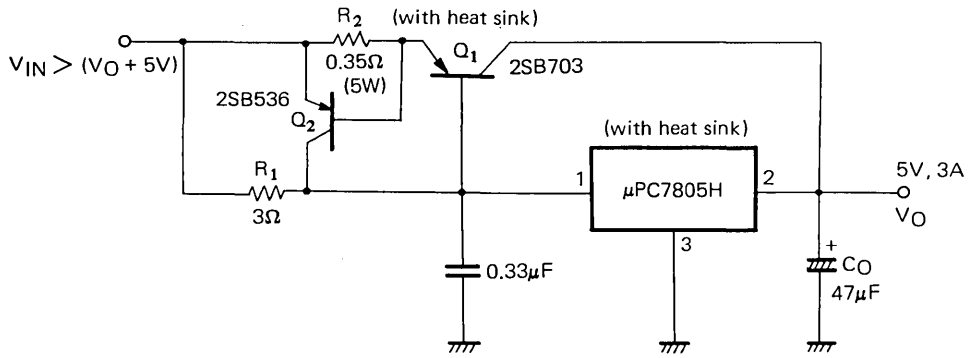


Fig. 11 Current Buffer (with short-circuit protection)

Fig. 12 shows an application circuit when the output current is limited by utilizing the built-in output current protective functions in μPC 7800H series.

Diode D_1 cancels the voltage between base and emitter of Q_1, and the current ratio of the regulator and external transistor is determined by R_1. The maximum output current is three times the maximum output current of μPC7805H. Considering a voltage loss by R_1 and D_1, the minimum input voltage to the regulator should be more than (V_O + 5 V).

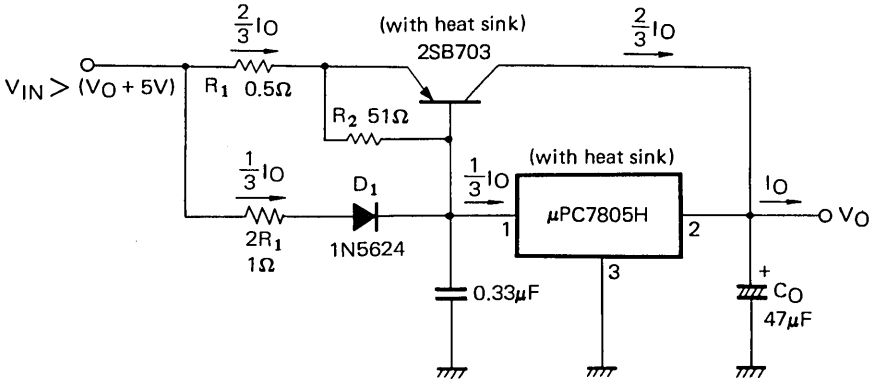


Fig. 12 Example of an application circuit with built-in current limitting circuit

4-3 Method of getting an optional output voltage (Simplified method)

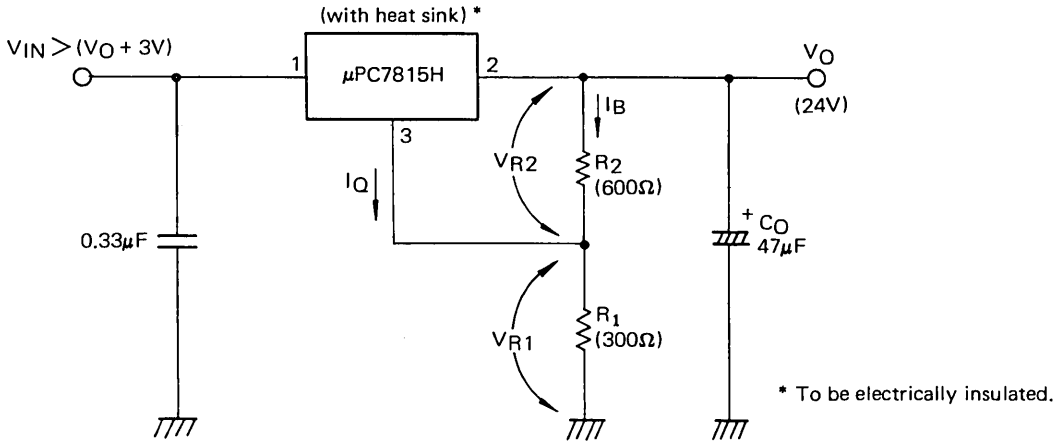


Fig. 13 Method of getting an optional output voltage

Two resistors are externally connected to the 3-terminal regulator having a fixed output so as to get an optional output voltage as shown in Fig.13. Assuming regulator current be I_Q and idling current of the external resistor R_2 be I_B, the following equation is obtained.

$$\begin{aligned} V_O &= V_{R_1} + V_{R_2} \\ &= R_1 \cdot (I_Q + I_B) + R_2 \cdot I_B \\ &= (R_1 + R_2) \cdot I_B + R_1 \cdot I_Q \end{aligned} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (7)$$

Since V_{R2} is equal to the fixed output voltage of the 3-terminal regulator;

$$I_B = \frac{V_{R_2}}{R_2} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (8)$$

Substituting equation (8) into equation (7);

$$V_O = \left(1 + \frac{R_2}{R_1}\right) \cdot V_{R_2} + R_1 \cdot I_Q \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (9)$$

From equation (9), it may be understood that the output voltage is determined by the fixed output voltage V_{R2}, circuit current I_Q and the external resistors R_1, R_2 of the 3-terminal regulator.

I_Q changes by about 0.05 mA against the input voltage variation of about 1V. Fig.14 shows the characteristic curve of the circuit current variation (ΔI_Q) vs input ripple voltage (ΔV_{IN}). By re-writing the equation (9) with this variation, equation (10) is obtained.

$$V_O = (1 + \frac{R_2}{R_1}) \cdot V_{R_2} + R_1 \cdot (I_Q + \Delta I_Q) \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (10)$$

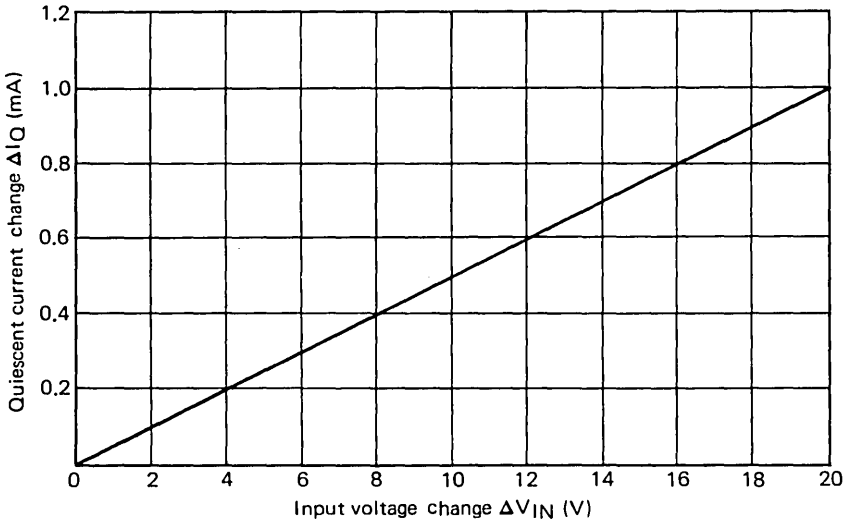


Fig. 14 ΔV_{IN}—ΔI_Q characteristic

[24 V regulator by utilizing μPC7815H]

(1) Design conditions

ΔV_{IN} = 5Vp-p (V_{IN} = 27V ~ 32V)

V_O = 24V

(2) Determination of R_1 and R_2

(2-1) From Fig. 14, I_Q = 0.25mA when V_{IN} = 5Vp-p

(2-2) I_B value should be more than 100 times the I_Q value (I_B = 25mA)

(2-3) Thus, $R_2 = V_{R2}/I_B$ = 15V/25mA = 600 (Ω)

(2-4) $V_{R1} = V_O - V_{R2}$ = 24 − 15 = 9 (V)

(2-5) Thus, $R_1 = V_{R1}/(I_B + I_Q)$ = 9V/(25 + 5) mA = 300 (Ω)

By adding R_1 = 300Ω and R_2 = 600Ω resistors, a V_O = 24V power supply is obtained.

4-4 Variable Output Circuit (1) (7 V~30 V)

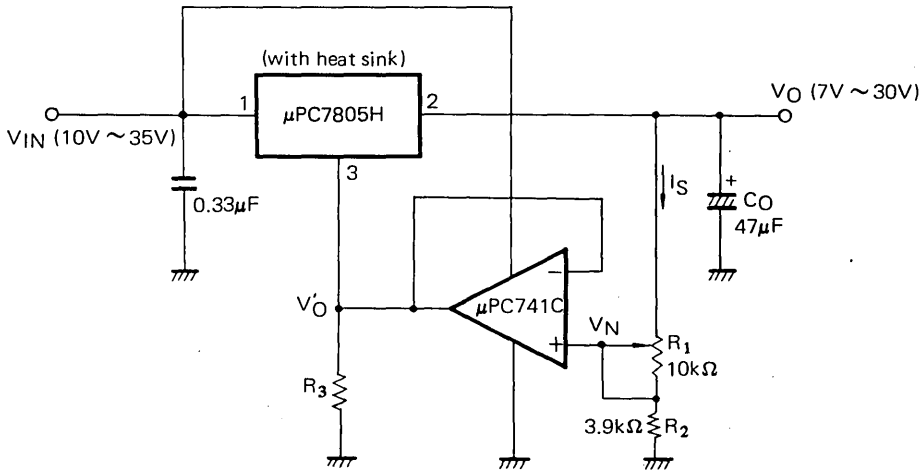


Fig. 15 Variable output power supply (I)

Assuming the output voltage of the operational amplifier be $V_{,O}$ and the current flowing into the output split resistor of the regulator be I_S in Fig. 15, the non-inverting input terminal voltage is shown by equation (11).

$$V_N = V'_O = I_S \cdot R_2 = \frac{V_O}{R_1 + R_2} \cdot R_2 \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (11)$$

Since the difference between V_O and $V_{,O}$ is always equal to the output voltage of μPC7805H, equation (12) is obtained and the output voltage V_O can be shown by equation (13).

$$V_O - V'_O = V_O \left(1 - \frac{R_2}{R_1 + R_2}\right) = V_O \cdot \frac{R_1}{R_1 + R_2} = 5\ (V) \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (12)$$

$$V_O = \left(1 + \frac{R_2}{R_1}\right) \cdot 5\ (V) \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (13)$$

4-5 Variable Output Circuit (II) (0.5~7V)

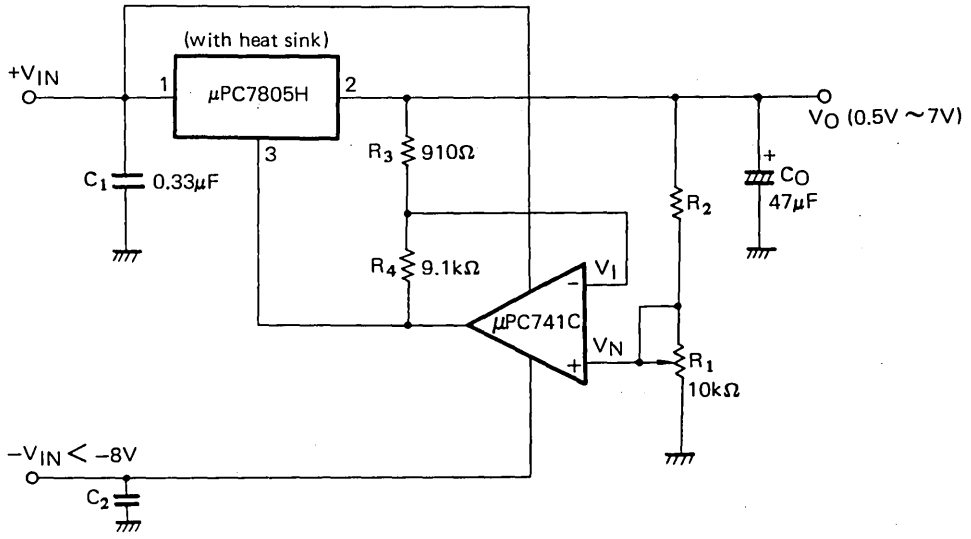


Fig. 16 Variable output power supply (II)

Fig. 16 is an example of the application circuits for obtaining an output voltage of less than 5V. It requires a low current negative power supply of −8~−10V (about −10 mA). Assuming the inverting input terminal voltage be V_I and non-inverting input terminal voltage be V_N in μPC741C.

$$V_N = \frac{R_1}{R_1 + R_2} \cdot V_O \quad \cdots\cdots (14)$$

$$V_I = V_O - \frac{R_4}{R_3 + R_4} \cdot 5\ (V) \quad \cdots\cdots (15)$$

Since $V_I \fallingdotseq V_N$ due to a negative feedback effect of the operational amplifier, the following equation is obtained.

$$\frac{R_1}{R_1 + R_2} V_O \fallingdotseq V_O - \frac{R_4}{R_3 + R_4} \cdot 5\ (V) \quad \cdots\cdots (16)$$

Solving equation (16) with reference to V_O, equation (17) is obtained.

$$V_O \fallingdotseq (1 + \frac{R_2}{R_1}) \cdot (\frac{R_4}{R_3 + R_4}) \cdot 5\ (V) \quad \cdots\cdots (17)$$

By setting $R_4 = 10\ R_3$, equation (17) can be re-written as;

$$V_O \fallingdotseq 0.45\ (1 + \frac{R_2}{R_1}) \quad \cdots\cdots (18)$$

4-6 Example of Tracking Power Supply Circuit

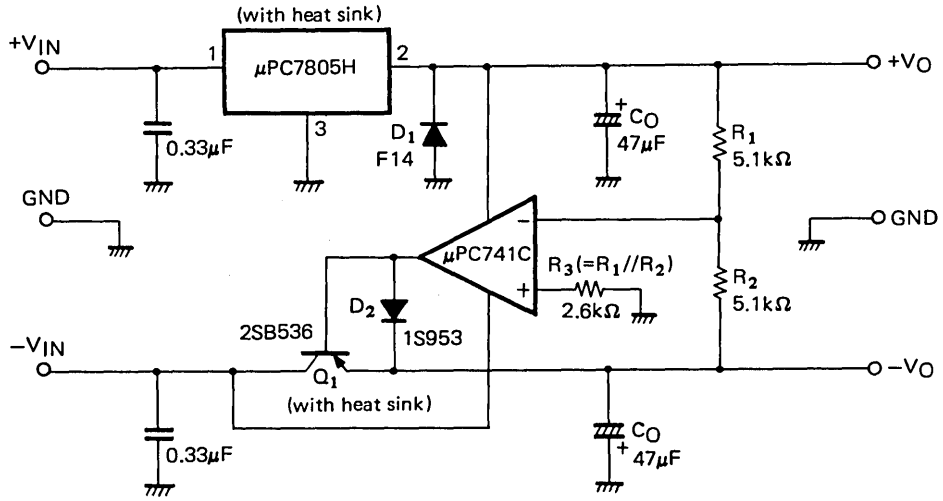


Fig. 17 Tracking Regulator

The 3-terminal regulator makes a positive power supply and a negative output power supply is obtained with a polarity-inverting circuit of gain R_2/R_1 by μPC741C.

When $R_1 = R_2$ as shown in Fig.17, the absolute values of the two output voltages are equal and the polarity is opposite to each other.

4-7 Example of Dual Power supply Circuit

A positive/negative power supply can be made by using two μPC7805H as shown in Fig. 18. In this case, two independent outputs are required on the secondary of the transformer, and the heat sink of IC_2 must be insulated using a mica sheet etc.

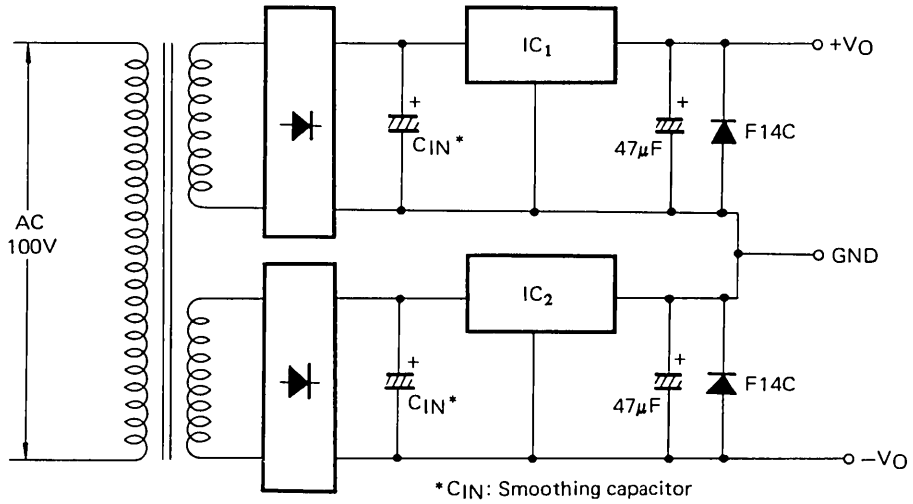


Fig. 18 Positive/Negative power supply

5. HEAT SINK DESIGN (REFERENCES)

The thermal resistance of the TO-220 type package $\theta_{J\text{-}C} \fallingdotseq 4\ ^\circ C/W$ between junction and case and $\theta_{J\text{-}A} = 83\ ^\circ C/W$ between junction and air. Accordingly, without heat sink, the package should be operated at less than 1.2 W of power dissipation. When the dissipation exceeds 1.2 W, a heat sink is necessary to operate the regulator within the maximum ratings. Fig. 19 is a graph showing the relation of area S (cm^2) and thickness d (mm) of the aluminum plate used as a heat sink vs its thermal resistance value.

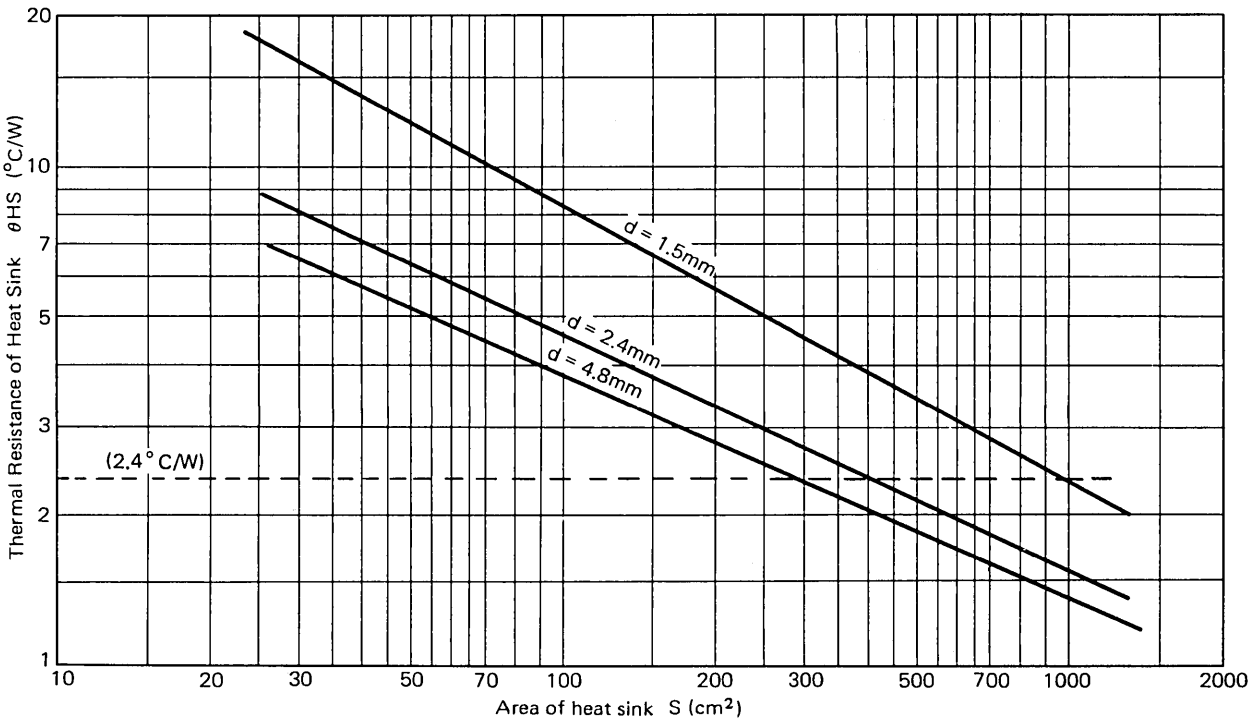


Fig. 19 Thermal resistance value of heat sink (Aluminum plate)

[Example of heat sink design]

(1) Design parameters

a. Maximum output current	$I_{Omax.} = 0.7$ (A)
b. Maximum input/output voltage differential	$V_{IN} - V_O$ max. = 10 (V)
c. Maximum ambient temperature	$T_{a\ max.} = 60$ (°C)
d. Maximum junction temperature	$T_{jmax.} = 105$ (°C)

(2) Calculation of thermal resistance

Junction temperature T_j under the actual operating condition can be calculated by equation (19).

$$T_j = (\theta_{J-C} + \theta_{C-HS} + \theta_{HS}) \cdot P_D + T_a \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (19)$$

where;

θ_{J-C} : Junction to Case thermal resistance value between junction and case (2.5 °C/W)
θ_{C-HS} : Case to Heat Sink thermal resistance value between case and heat sink
θ_{HS} : Heat Sink thermal resistance value of heat sink
P_D : Power Dissipation

Since $T_{jmax.} = 105$ °C, $T_{amax.} = 60$ °C, $\theta_{C-HS} \ll 1$ °C/W and $P_{Dmax} = 7$ W,

$$\theta_{HS} = \frac{T_{jmax.} - T_{amax.}}{P_{Dmax.}} - (\theta_{J-C} + \theta_{C-HS}) \fallingdotseq 2.4\ (°C/W) \quad \cdots\cdots\cdots\cdots\cdots \quad (20)$$

(3) Method of determining the heat sink size

From equation (20), the designed parameters can be satisfied by using a heat sink of 2.4 °C/W. If no suitable heat sink is available on the market, its size can be determined referring to Fig. 19. The dotted line of 2.4 °C/W thermal resistance intersects the solid line of d = 4.8 mm at S = 280 cm² in Fig. 19. Thus, an aluminum plate of d(thickness) = 4.8 mm, S(area) = 145 cm² has the required thermal resistance value. When d = 2.4 mm, S = 430 cm² and when d = 1.5 mm, S = 970 cm² in the same way as above. It is necessary to design an optimum heat sink to use the 3-terminal regulator normally, referring to the above examples. As design references, the recommended operating conditions of μPC7800H series are shown in Table 7.

6. RECOMMENDED OPERATING CONDITION

	V_{IN}	I_O	Tjmax.	Tamax.	θHS
μPC7805H	8 ~ 12 V	0.5 ~ 1 A	105 °C	60 °C	5 °C/W
μPC7808H	11 ~ 17 V	"	"	"	3.5 °C/W
μPC7812H	16 ~ 22 V	"	"	"	2.4 °C/W
μPC7815H	18 ~ 26 V	"	"	"	2.4 °C/W
μPC7818H	22 ~ 30 V	"	"	"	1.63 °C/W
μPC7824H	27 ~ 37 V	"	"	"	1.63 °C/W

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