NEC ELECTRONICS (EUROPE) GMBH

μPD7759

ADPCM SPEECH SYNTHESIS LSI

PRODUCT DESCRIPTION

12/85 V1.0

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OUTLINE

The uPD7759 is the external ROM version the uPD7755 family ADPCM speech synthesis LSI which provides high quality voice , psudo-sound and melody synthesis. The repeating-phoneme method is adopted to reduce the data size.

The addressing area of the uPD7759 is up to 1 Mbits , So that it may be utilized for the long term synthesis and the evaluation of the other on-chip ROM type synthesis LSI which belongs to the uPD7755 family.

The short turn around time of speech data processing is due to the adoption of the ADPCM method.

FEATURES

* method of synthesis ;

  ADPCM with repeating phoneme

  (rp-ADPCM)

* sampling frequency ;

  4 kHz, 5 kHZ, 6 kHz, 8 kHz,

* bit rate ;

  8 - 32 kbps

* speech data ;

  [1] read out from external ROMs

  (1 Mbit max.)

  [2] transferred by CPU

* duration of synthesis ;

  128 seconds max.

  (with 1 Mbits external ROMs)

* the number of message ;

  256 max.

* control signal interface ;

  general purpose 4/8-bit CPU

* output speech signal ;

  analog current output type

  (open drain - 9bits D/A converter

  is equipped.)

* process technology ;

  CMOS

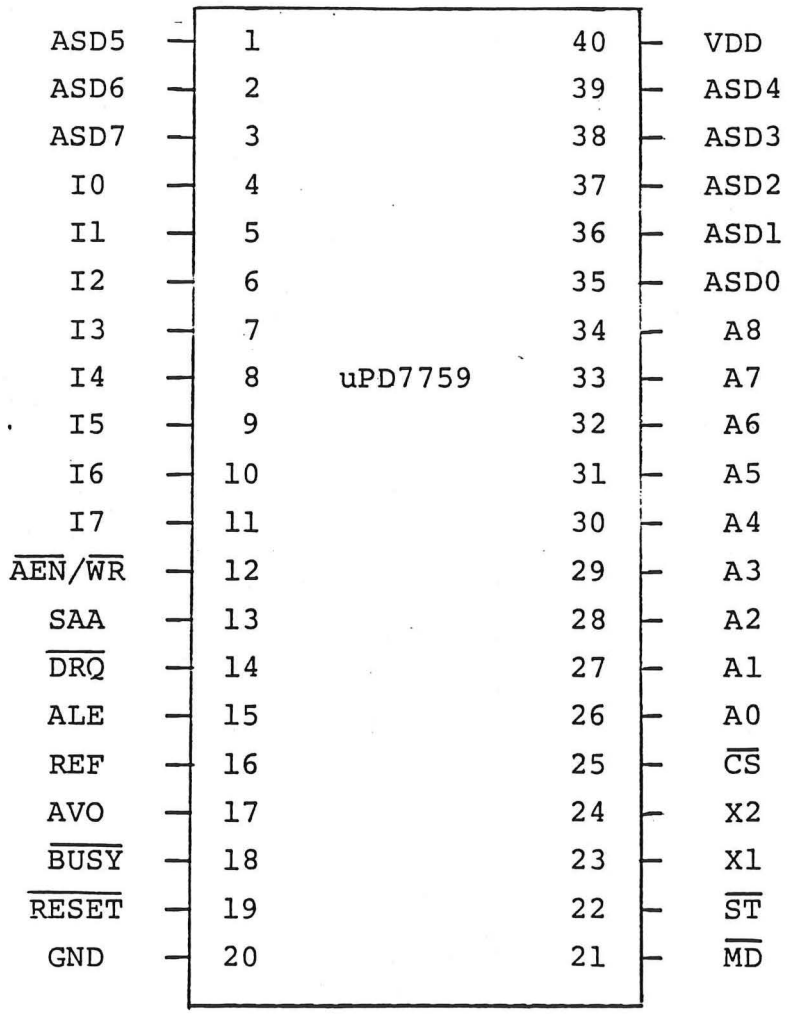
* power supply ;

  2.7 V - 5.5 V single

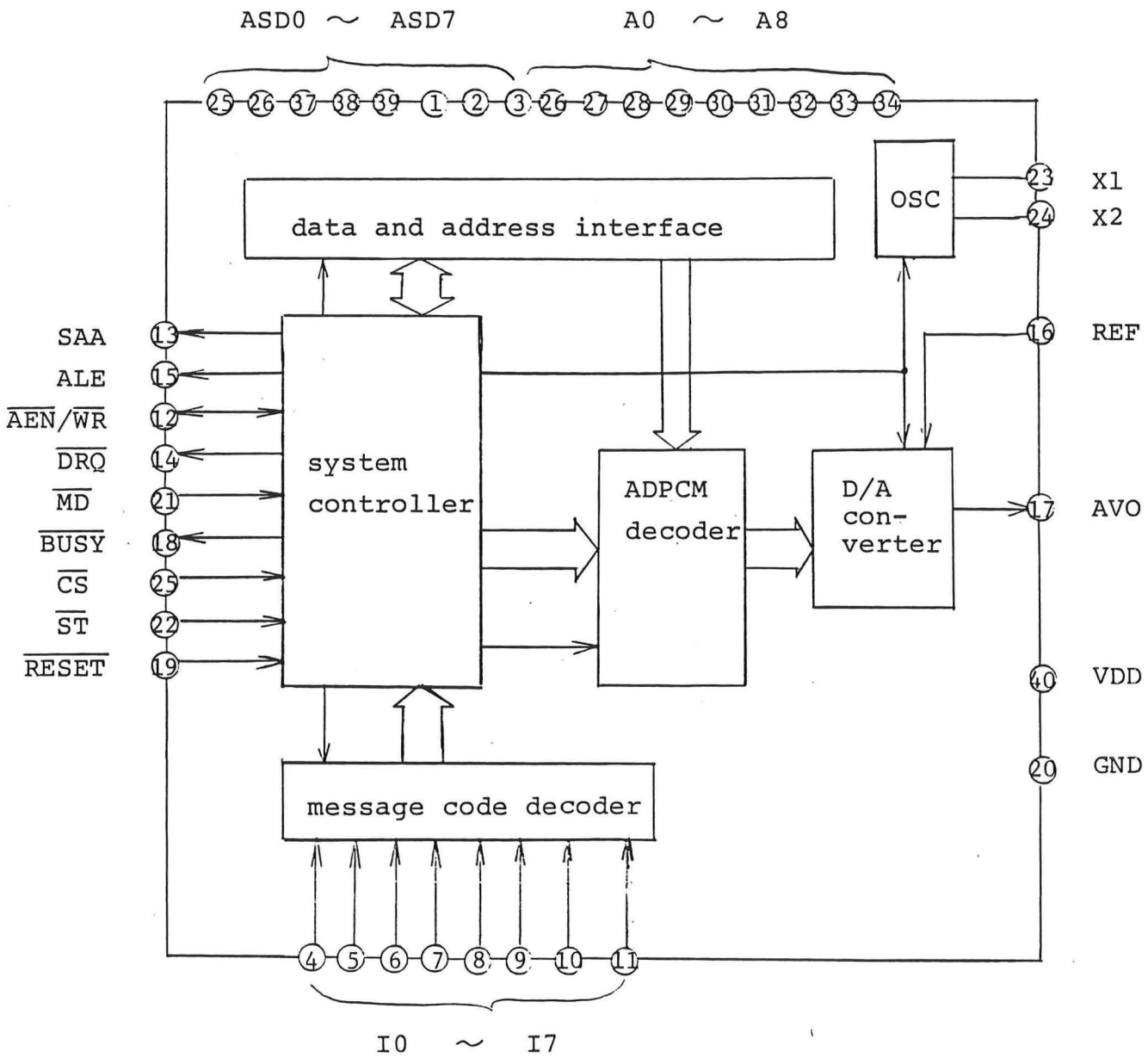
* packege ;

  40 pin plastics DIP

uPD7759 Pin configuration



uPD7759 functional block diagram



uPD7759 Pin description

signature	Pin No.	I/O	function
I0 I1 I2 I3 I4 I5 I6 I7	4 5 6 7 8 9 10 11	I	(stand alone mode) A message to be synthesized is specified by the positive logic signal on these lines. The signal is latched at the rising edge of $\overline{ST}$. (slave mode) These lines are ineffective. To be fixed at GND level.
A0 A1 A2 A3 A4 A5 A6 A7 A8	26 27 28 29 30 31 32 33 34	O	(stand alone mode) output lines for lower 9 bit of address bus. (slave mode) Ineffective
ASD0 ASD1 ASD2 ASD3 ASD4 ASD5 ASD6 ASD7	35 36 37 38 39 1 2 3	I/O	(stand alone mode) : I/O 1. Output lines for higher 8 bit of address signal. 2. Input lines for speech data. (slave mode) : I Input lines for speech data.
ALE	15	O	(stand alone mode) This signal is used to define the timing that higher address is latched by an external latch. (slave mode) Ineffective.

signature	Pin No.	I/O	function
$\overline{AEN}/\overline{WR}$	12	O/I	(stand alone mode) : AEN This signal is at high level while address signal is valid. (slave mode) : WR Write strobe signal for a speech data.
SAA	13	O	(stand alone mode) Indicates the start address of a message which is stored in the directory area of data memory, is being read out. (slave mode) ineffective.
$\overline{DRQ}$	14	O	Data request signal.
$\overline{MD}$	21	I	To specify the slave mode operation, keep this line low level. Transition between two operation modes is not accepted during synthesis or in the stand alone mode.
$\overline{CS}$	25	I	(stand alone mode) Chip select signal. Only when this line is low level, $\overline{ST}$ signal is accepted. (slave mode) Only when this line is low level, $\overline{WR}$ signal is accepted.
$\overline{ST}$	22	I	(stand alone mode) synthesis start signal. (slave mode) Ineffective. to be pulled up.

signature	Pin No.	I/O	function
$\overline{\text{BUSY}}$	18	O	This signal indicate the chip is synthesizing. In the stand-by mode line becomes high impedance state.
$\overline{\text{RESET}}$	19	I	Reset signal used to initialize the device.
REF	16	I	Refference current terminal for D/A converter. In the stand-by mode this line is high impedance state.
AVO	17	O	An output line for speech signal. In the stand-by mode, current does not flow.
X1 X2	23 24	- -	A ceramic resonator for clock generator is connected to this pin. In the stand-by mode, pin 23 is low level and pin 24 is high level.
V_{DD}	40	-	Line for power supply V_{DD}.
GND	20	-	Ground line.

Absolute maximum ratings

item	symbol	conditions	MIN.	MAX.	unit
supply voltage	V_{DD}		-0.3	+7.0	V
input voltage	V_I		-0.3	V_{DD}+0.3	V
output voltage	V_O		-0.3	V_{DD}+0.3	V
storage temperature range	T_{STG}		-4.0	+125	°C
temperature range above operating device	T_{OPT}		-10	+70	°C

Recommended operating conditions

item	symbol	conditions	MIN.	TYP.	MAX.	unit
supply voltage	V_{DD}		2.7		5.5	V
high level input voltage	V_{IH1}	applied to I0-I7, $\overline{ST}$, $\overline{CS}$, $\overline{RESET}$, $\overline{MD}$, $\overline{WR}$	$0.7V_{DD}$		V_{DD}	V
	V_{IH2}	applied to ASD0-ASD7, V_{DD}=5V± 10%	2.2		V_{DD}	V
low level input voltage	V_{IL1}	applied to I0-I7, $\overline{ST}$, $\overline{CS}$, $\overline{RESET}$, $\overline{MD}$, $\overline{WR}$	0		$0.3V_{DD}$	V
	V_{IL2}	applied to ASD0-ASD7 V_{DD}=5V± 10%	0		0.8	V
clock frequency	f_{OSC}		630	640	650	kHz

Electrical characteristics

(Ta=-10 — +70°C, V_{DD}=2.7 — 5.5V, f_{OSC}=640kHz)

item	symbol	conditions	MIN.	TYP.	MAX.	unit
high level output voltage	V_{OH}	I_{OH}=-100uA		V_{DD}-0.5		V
low level output voltage	V_{OL}	V_{DD}=5V± 10%, I_{OL}=1.6mA			0.4	V
leakage current of input lines	I_{LI}	I_0 — I_7, $\overline{ST}$, $\overline{CS}$, $\overline{WR}$, ASD0 ASD7, $\overline{MD}$			3	uA
leakage current of output lines	I_{LO}	$\overline{BUSY}$, A0 — A8			3	uA
supply current	I_{DD}	(stand alone, slave mode) V_{DD}=5V			10	mA
		(stand-by mode) V_{DD}=5V			20	uA
		(stand alone, slave mode) 2.7V ≤ V_{DD} ≤ 3.5V			1	mA
		(stand-by mode) 2.7V ≤ V_{DD} ≤ 3.5V			10	uA

item	symbol	conditions	MIN.	TYP.	MAX.	unit
input current of REF	I_{REF}	V_{DD}=2.7V, R_{REF}=0Ω	140	250	440	uA
		V_{DD}=5.5V, R_{REF}=0Ω	500	760	1200	
		V_{DD}=2.7V, R_{REF}=50kΩ	21	30	39	
		V_{DD}=5.5V, R_{REF}=50kΩ	68	78	88	
output current of AVO	I_{AVO}	2.7V≤ V_{DD}≤ 5.5V V_{AVO}=2.0, D/A input: 1FFH	32	34	36	I_{REF}
leakage current of AVO	I_{LA}	0V≤ V_{AVO}≤ V_{DD} in the stand-by mode			5	uA

Timing requirements (common to all modes)

item	symbol	conditions	MIN.	TYP.	MAX.	unit
set up time of $\overline{CS}$	t_{CS}	to $\overline{ST}\downarrow$	0			ns
hold time of $\overline{CS}$	t_{SC}	after $\overline{ST}\uparrow$	0			ns
$\overline{ST}$ pulse duration	t_{CC}	V_{DD}=5V± 10% V_{DD}=2.7—5.5V	350 5			ns uS
set up time of message code	t_{DW}	V_{DD}=5V± 10% V_{DD}=2.7—5.5V	350 5			ns us
hold time of message code	t_{WD}	after $\overline{ST}\uparrow$	0			us

Switching charateristics (common to all modes)

item	symbol	conditions	MIN.	TYP.	MAX.	unit
$\overline{BUSY}$ rise time	t_{r1}	C_L=150PF, V_{DD}=5V± 10%			800	ns
	t_{r2}	C_L=150PF, V_{DD}=2.7—5.5V			2	us
$\overline{BUSY}$ fall time	t_{f1}	C_L=150PF, V_{DD}=5V± 10%			800	ns
	t_{f2}	C_L=150PF, V_{DD}=2.7—5.5V			2	us

a. stand alone mode

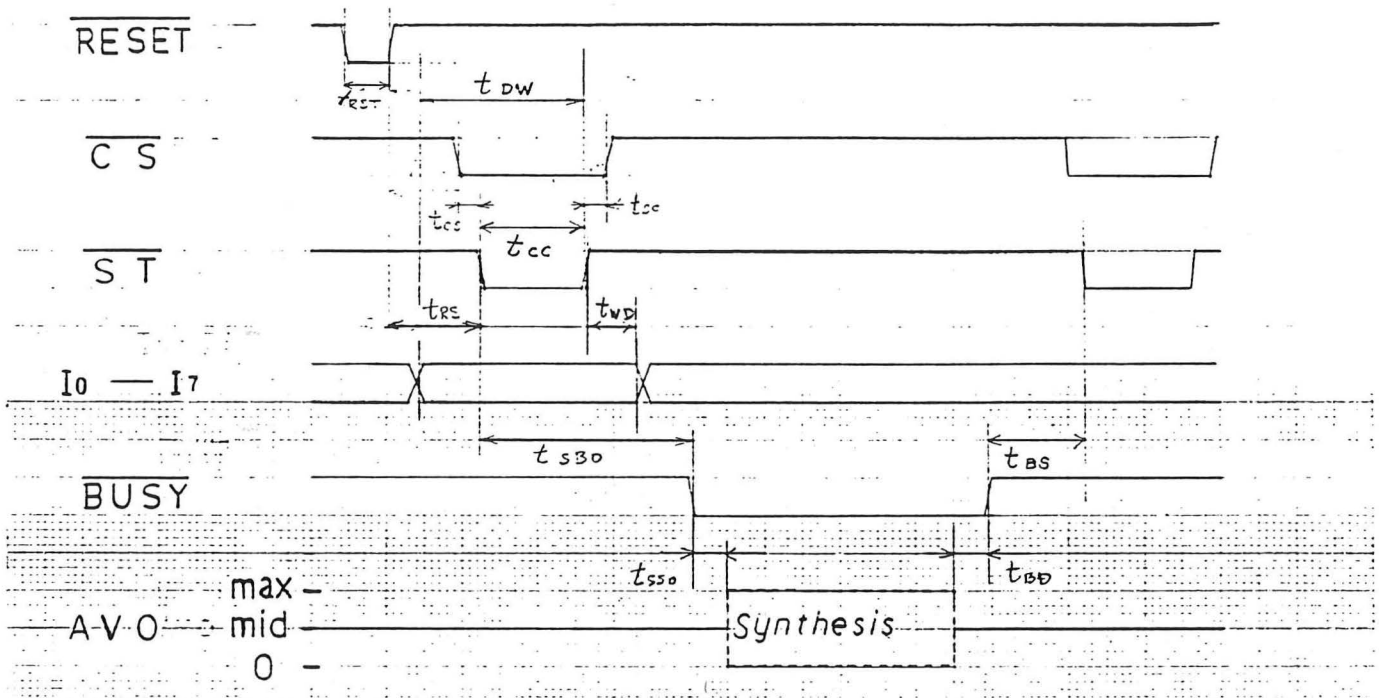
(1) timing requirements

item	symbol	conditions	MIN.	TYP.	MAX.	unit
$\overline{\text{RESET}}$ pulse duration	t_{RST}		18.5			uS
$\overline{\text{CS}}$ set up time	t_{CS}	to $\overline{\text{ST}}\downarrow$	0			ns
$\overline{\text{CS}}$ hold time	t_{SC}	after $\overline{\text{ST}}\uparrow$	0			ns
$\overline{\text{ST}}$ pulse duration	t_{CC}	$2.7V \leq V_{DD} \leq 5.5V$ $4.5V \leq V_{DD} \leq 5.5V$	2 350			us ns
message code set up time	t_{DW}	$2.7V \leq V_{DD} \leq 5.5V$ $4.5V \leq V_{DD} \leq 5.5V$	2 350			us ns
message code hold time	t_{WD}	after $\overline{\text{ST}}\uparrow$	0			ns
speech data set up time	t_{RD}	to $\overline{\text{DRQ}}\downarrow$	8			us
speech data hold time	t_{RDH}	after $\overline{\text{DRQ}}\uparrow$	1.25			us

Switching characteristics

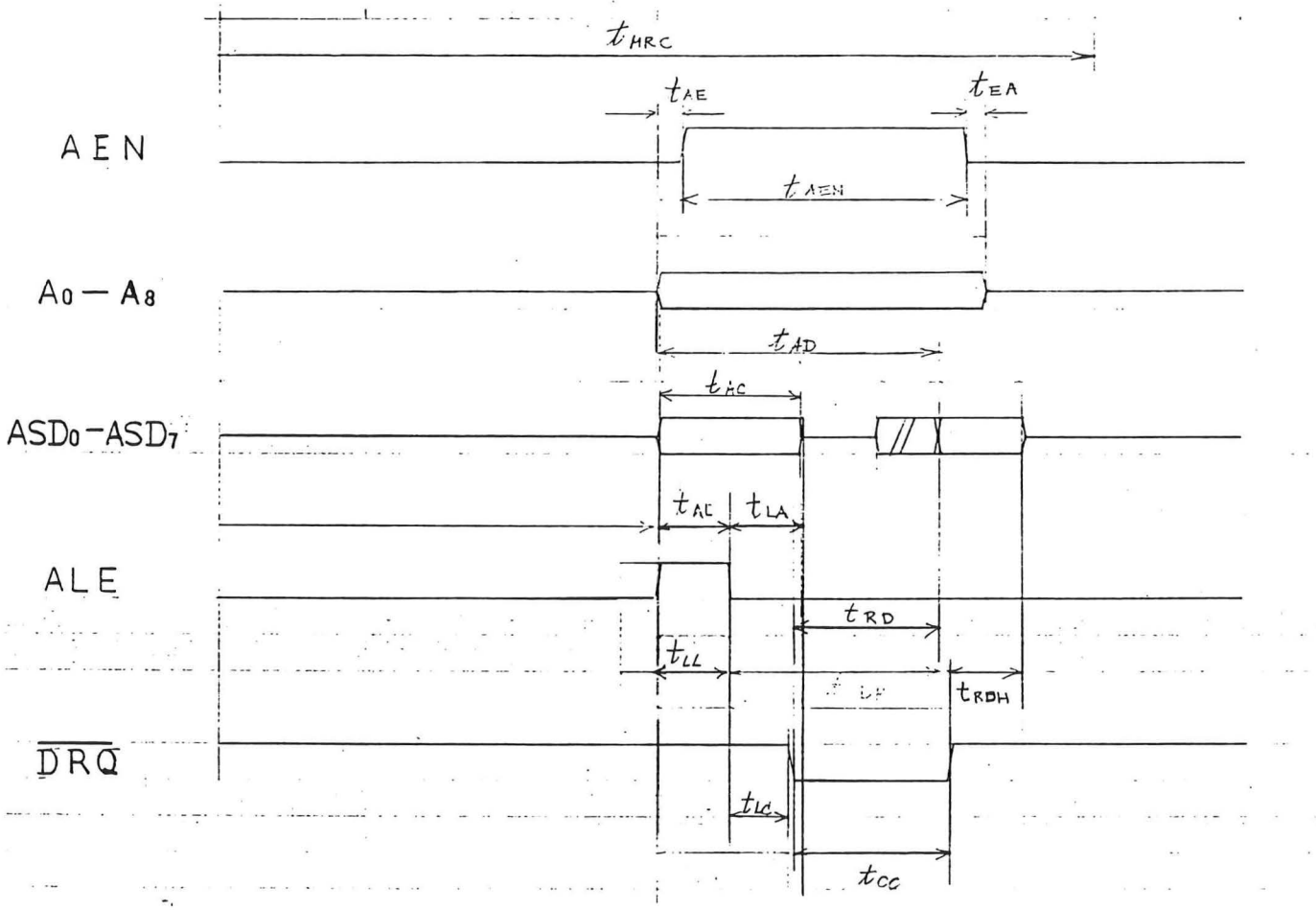
item	symbol	condition	MIN.	TYP.	MAX.	unit
$\overline{\text{BUSY}}$ output delay	t_{SBO}	operation mode (after $\overline{\text{ST}}\downarrow$)		6.25	10	uS
Speech output delay	t_{SSO}	operation mode (after $\overline{\text{BUSY}}\downarrow$)		2.1	2.2	ms
$\overline{\text{BUSY}}$ hold time	t_{BD}	after synthesis			15	uS
ALE pulse duration	t_{LL}			3.13		uS
higher address set up time	t_{AL}	to ALE$\downarrow$ to AEN$\uparrow$		3.13 0		uS uS
higher address set up time	t_{LA}	after ALE after AEN		3.13 0		uS uS
AEN pulse duration	t_{AEN}			14.1		uS
$\overline{\text{DRQ}}$ output timing	t_{LC}	after ALE$\downarrow$		3.13		uS
pulse duration timing	t_{AC}			6.25		uS
$\overline{\text{DRQ}}$ pulse duration	t_{CC}			7.81		uS
$\overline{\text{ROM}}$ read cycle time	t_{MRO}			37.5		uS

Stand alone mode



Stand alone mode

memory access



b. slave mode

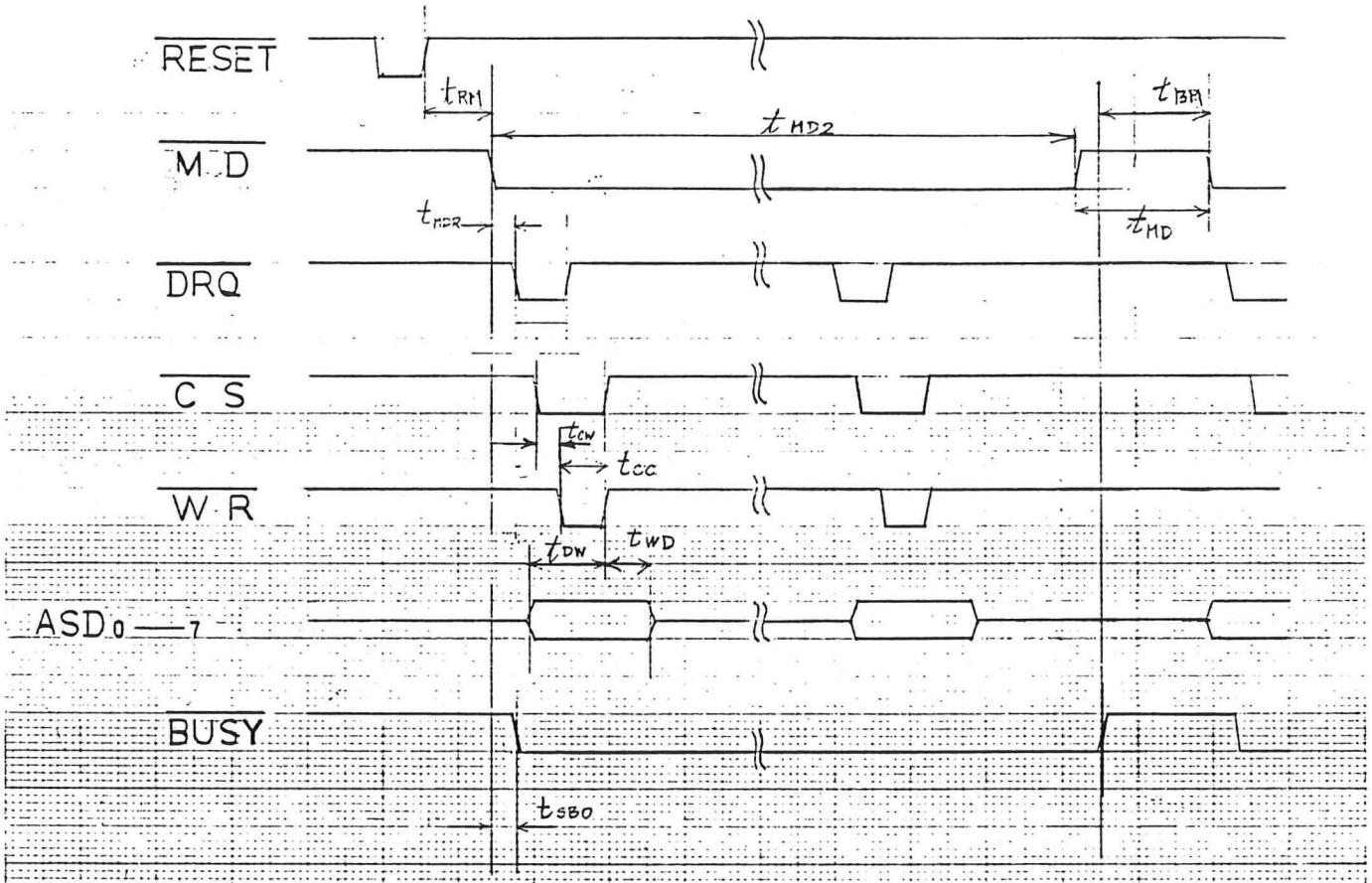
(1) timing requirements

item	symbol	condition	MIN.	TYP.	MAX.	unit
$\overline{MD}$ input timing	t_{RM}	after $\overline{RESET}\uparrow$	6.2			us
	t_{BM}	after $\overline{BUSY}\uparrow$	0			ns
	t_{MD}	after $\overline{MD}\uparrow$	6.2			us
set up time of speech data	t_{DW}	to $\overline{WR}\uparrow$ 5V$\pm$ 10%	350			ns
hold time of speech data	t_{WD}	after $\overline{WR}\uparrow$ 5V$\pm$ 10%	0			ns
data write timing	t_{WR}	after $\overline{DRQ}\downarrow$			31.7	us
$\overline{WR}$ pulse duration	t_{CC}	5V $\pm$ 10%	350			ns
$\overline{CS}$ set up time	t_{CW}	to $\overline{WR}\downarrow$	0			ns
$\overline{CS}$ hold time	t_{WC}	after $\overline{WR}\uparrow$	0			ns
$\overline{MD}$ pulse duration	t_{MD2}		6.2			ns

(2) switching characteristics

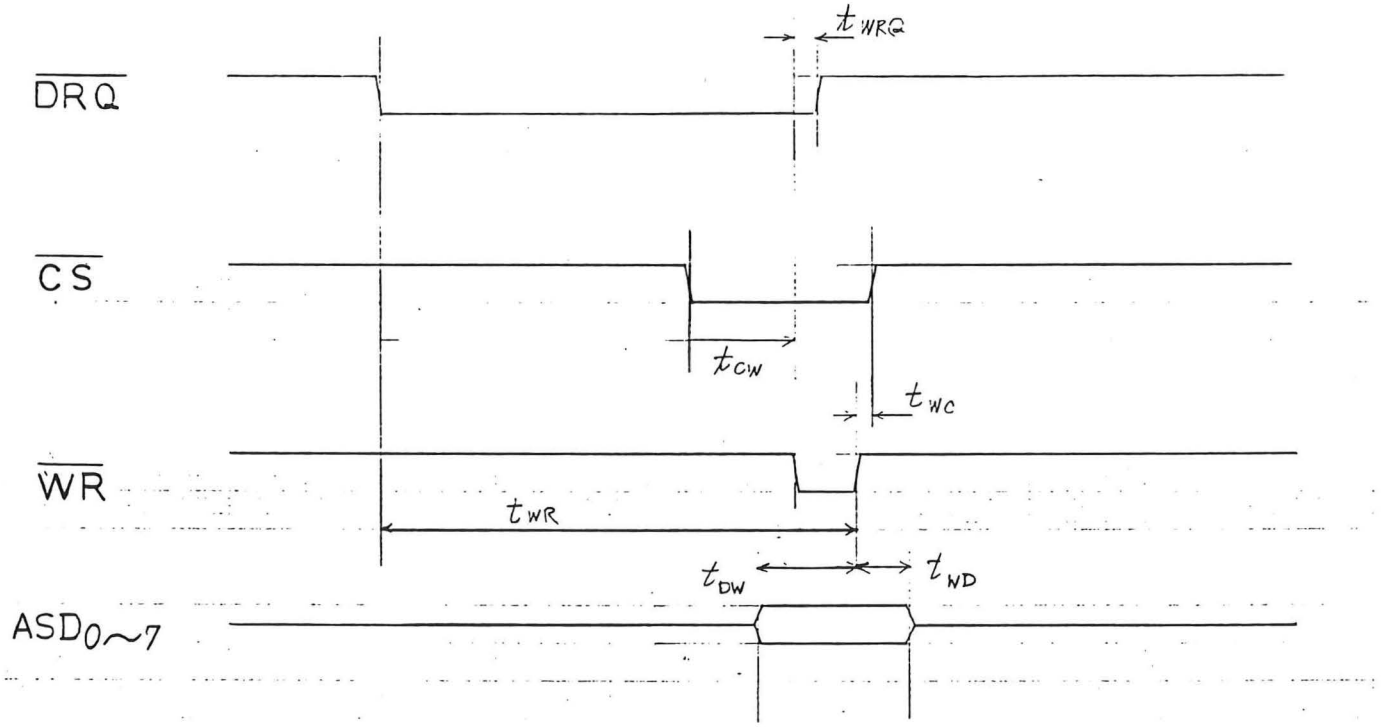
item	symbol	condition	MIN.	TYP.	MAX.	unit
BUSY output delay	t_{SBO}	after $\overline{MD}\downarrow$			9.5	us

Slave mode


RESET
M/D
DRQ
C S
W R
ASD0—7
BUSY
tRM
tMD2
tBH
tMDR
tMD
tCW
tCC
tDW
tWD
tSBO

Slave mode

data transfer



c. stand-by mode

(1) timing requirements

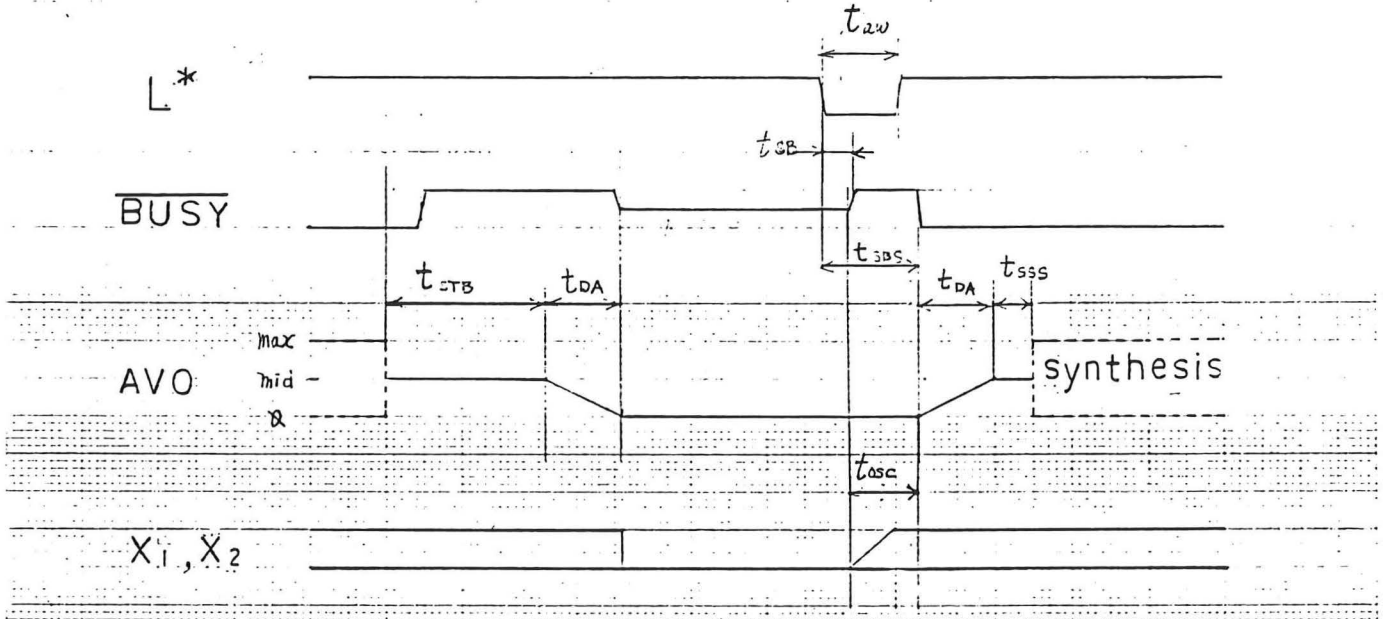
item	symbol	condition	MIN.	TYP.	MAX.	unit
pulse duration of stand-by escape signal L*	t_{AW}	V_{DD}	350			ns

(2) switching characteristics

item	symbol	condition	MIN.	TYP.	MAX.	unit
operation mode hold time	t_{STB}	after synthesis		2.9	3	s
duration to activate or inactivate D/A converter	t_{DA}			46.5	47	ms
time to $\overline{\text{BUSY}}\downarrow$	t_{SB}	after L*↓(note 1)		6.25	10	us
time to start synthesis	t_{SSS}			2.1	2.2	ms

* Note 1 see next page

Stand-by mode



(n o t e)

L* : Signal to escape stand by mode.

$$= \begin{cases} \overline{CS} \wedge \overline{ST} & \text{:When operation mode is stand alone mode} \\ \overline{CS} \wedge \overline{WR} & \text{:When operation mode is slave mode} \end{cases}$$

Mechanical data

40-pin . plastic dual-in-line package (unit: mm)