1982
Product
Catalog

Linear Integrated Circuits

Precision Monolithics Incorporated

PMI

1982 Linear Integrated Circuits

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Although every effort has been made to insure accuracy of the information contained in this data book, PMI assumes no responsibility for inadvertent errors.

PMI assumes no responsibility for the use of any circuits described herein and makes no representation that they are free of patent infringement.

The products in this catalog are manufactured under one or more of the following patents: 4,055,773; 4,056,740; 4,092,639; 4,088,905; 4,118,699; 4,131,884; 4,138,671; 4,168,528; 4,109,215; 4,142,117; 4,068,254; 4,228,367; 4,210,830; 4,260,911; 4,272,656; 4,285,051.

PRECISION MONOLITHICS, INC. LIFE SUPPORT APPLICATION POLICY

As a general policy, Precision Monolithics Inc. does not recommend the use of its components of any type in "Life Support Applications" wherein failure or malfunction of the PMI component threatens life or makes injury probable. Any manufacturer which incorporates PMI's components within a life support system must obtain PMI's prior consent based upon assurance to PMI that a malfunction of PMI's component does not pose direct or indirect threat of injury or death, and (even if such consent is given) shall indemnify PMI from any claim, loss, liability, and related expenses arising from any injury or death resulting from use of PMI components in a life support application. PMI's warranty is limited to replacement of defective components and does not cover injury to persons or property or other consequential damages.

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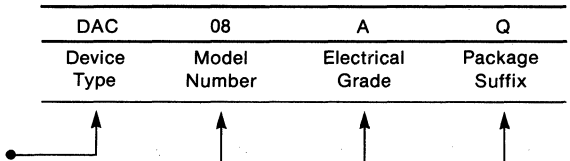
ORDERING INFORMATION



How to order standard product.

1. Select device type from catalog:

   BUF ..... Buffer
   CMP..... Comparator
   DAC..... Digital-to-Analog Converter
   DMX..... DeMultiplexer
   GAP..... General Purpose Analog Processor
   MAT..... Matched Transistor
   MUX..... Multiplexer
   OP ..... Proprietary Operational Amplifier
   PKD ..... Peak Detector
   PM ..... Second-Source Industry Specs
   REF ..... Voltage Reference
   RPT ..... PCM Line Repeater
   SMP..... Sample and Hold
   SW ..... Analog Switch

2. Select Model Number from Catalog (see Device Section and Selection Guides)

3. Select Electrical Grade from Catalog. See Data Sheet for specific suffix, DAC-02, DAC-03, DAC-04, DAC-05, DAC-06 and DAC-100 have multi-letter electrical grades.

4. Select package from appropriate data sheet in catalog.

   H..... 6 lead TO-78
   J ..... 8 lead TO-99
   K..... 10 lead TO-100
   L ..... 10 lead Hermetic Flatpack } SPECIAL ORDER Only
   M..... 14 lead Hermetic Flatpack } SPECIAL ORDER Only
   N..... 24 lead Hermetic Flatpack } SPECIAL ORDER Only
   P..... Epoxy B DIP (ALL)
   Q..... 16 lead Hermetic DIP
   R..... 20 lead Hermetic DIP
   T..... 28 lead Hermetic DIP
   V..... 24 lead Hermetic DIP
   X..... 18 lead Hermetic DIP
   Y..... 14 lead Hermetic DIP
   Z..... 8 lead Hermetic DIP

All PMI −55°C to +125°C devices are available with Class B, MIL-STD-883 screening as standard products. To order an 883B part, simply include the designation "/833" in the part number after the package suffix. For example, the DAC-08AQ screened to 883B requirements would be ordered as a DAC-08AQ/883. The DAC-100 data sheet is an exception to this procedure. Consult the DAC-100 data sheet for MIL-STD-883 ordering information.

PMI's factory is certified to produce JAN parts per MIL-M-38510. Consult the factory for availability of specific slash sheet parts not listed in this catalog.

DICE ORDERING INFORMATION

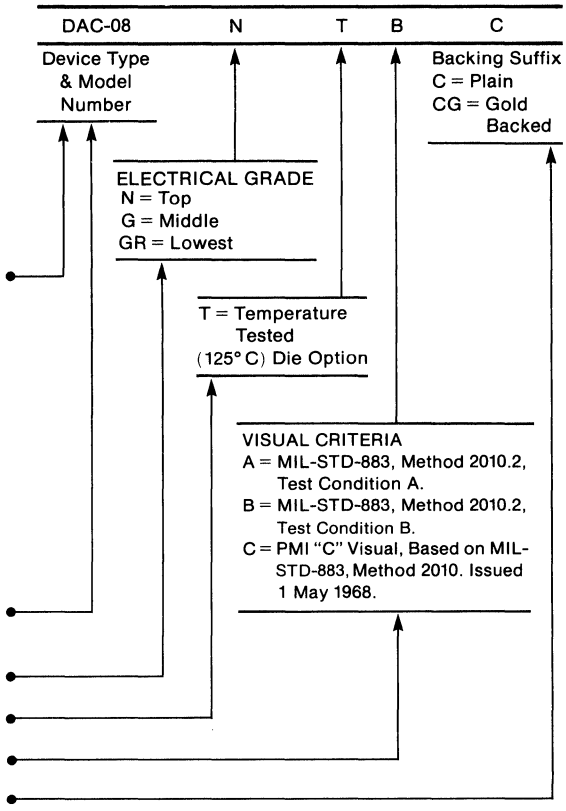
All PMI chips are available with either plain backing or, at extra cost, 1-micron thick eutectic-bonded gold backing. Electrical performance is specified at 25° C for all products in the data sheet section of this catalog. Visual inspection criteria is as listed below.

For price and delivery information or quotations for gold backed dice or special devices, contact the nearest PMI sales office or representative listed in the back of this Catalog.

1. Select device type from catalog:

   BUF..... Buffer
   CMP ..... Comparator
   DAC ..... Digital-to-Analog Converter
   DMX ..... DeMultiplexer
   GAP ..... General Purpose Analog Processor
   MAT ..... Matched Transistor
   MUX ..... Multiplexer
   OP ..... Proprietary Operational Amplifier
   PKD ..... Peak Detector
   PM ..... Second-Source Industry Specs
   REF..... Voltage Reference
   RPT..... PCM Line Repeater
   SMP ..... Sample and Hold
   SW ..... Analog Switch

2. Select Model Number from Catalog (see Device Section and Selection Guides).
3. Select electrical grade from data sheet.
4. Add 125° C Testing Option ("T") if desired.
5. Select visual screening level.
6. Select backing suffix.



BURNED-IN DEVICES

PMI now offers all commercial and industrial grade parts with 160 hour or equivalent (at our option) burn-in. Parts with this option are specified with the letters BI added between the model number and the electrical grade. For example, to order a DAC-08AQ with burn-in, the part number will be: DAC-08BIAQ. This service provides customers with the extra margin of safety required in various programs where early life failures must be reduced as much as possible.

SPECIAL DEVICES

Precision Monolithics, Inc. will be pleased to furnish quotations on requirements for devices with special electrical testing, extra reliability processing and/or qualification data per MIL-STD-883, condition A or MIL-M-38510. Please refer these requests to the authorized representatives or PMI sales office listed in Section 17 of this Catalog.

FEATURES

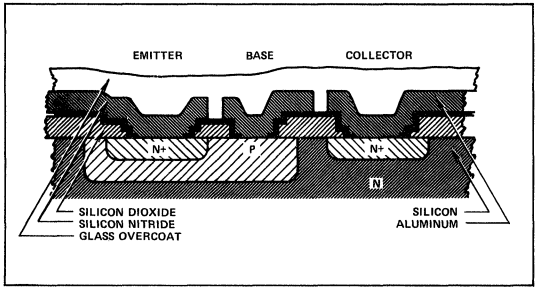
- **Highest yields ..... 25° C Parameters Guaranteed**
- **Highest Performance ..... Tight Specifications**
- **Highest Reliability-Exclusive "Triple Passivation "Process**
- **Wide Temperature Range Operations**
- **Excellent Die Attach .....Thick Gold or Standard Backing**
- **100% Visually Inspected to MIL-STD-883 Criteria**
- **Tight Distributions ..... Precision Process Control**
- **Carefully Packaged ..... No Loss During Shipment**
- **Guaranteed Dimensions ..... ±3mils**
- **Guaranteed Pad Size ..... 4 mils**

GENERAL DESCRIPTION

The superior performance of most Precision Monolithics products is available to the hybrid microcircuit designer. All chips are 100% electrically tested for all guaranteed DC parameters at 25° C and are 100% visually inspected to MIL-STD-883 visual criteria. Each die is protected with our "Triple Passivation" Process incorporating an advanced Silicon Nitride ion barrier plus a thick glass coating over the metallization. Dice are packaged in waffle-pack carriers with an anti-static shield and cushioning strip placed over the active surface to assure extra protection during shipment. Precision Monolithics dice provide the highest performance available coupled with lowest overall finished costs.

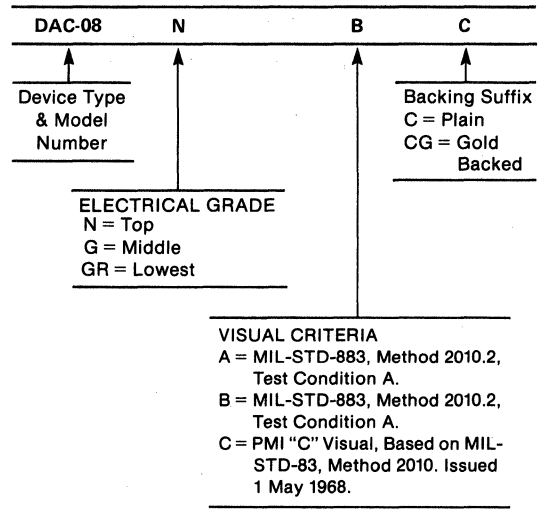
TRIPLE PASSIVATION

Triple Passivation is a three-step process which provides superior reliability and protection for all Precision Monolithics integrated circuits. First, a specially treated thermal silicon dioxide layer is grown. This protects the junctions and also attracts any residual ionic impurities to the top surface of the oxide, where they are held fixed. Next, a layer of silicon nitride is applied to prevent the entry of any potential contamination or impurities. The third step is the thick glass overcoat layer which leaves only the bonding pads exposed. This "glassivation" protects the die from damage during assembly and is especially important in minimizing yield loss during shipment and assembly of dice for hybrid circuits.



ORDERING INFORMATION

All PMI dice are available with either plain backing, or at extra cost, 3000 Å minimum alloyed gold backing. Electrical performance is specified at 25°C for all products in the data sheet section of this catalog. Visual inspection criteria is as listed below:



For price and delivery information or quotations for special devices, contact the nearest PMI sales office or representative listed in the back of this catalog.

MECHANICAL INFORMATION

DIMENSIONS

All dimensions are nominal and in mils (10^{-3} inches). Die thickness is 8 mils min. to 22 mils max.

METALLIZATION

Aluminum metallization with a nominal thickness of 10,000 angstroms is standard for all devices.

BONDING PADS

Minimum bonding pad size is 4.0 mils × 4.0 mils for all devices.

TESTING

VISUAL INSPECTION

All dice are 100% visually inspected to the applicable visual criteria per MIL-STD-883, Method 2010, Test Condition B.

Devices with visual inspection to MIL-STD-883 Method 2010 Test Condition A are available on special order only.

ELECTRICAL TESTING

All dice are 100% tested to the +25°C DC specifications listed in the data sheet section of this catalog. Sample assembly and testing in standard packages to specified LTPD of units from customer's dice lot are available at extra cost.

ASSEMBLY PROCEDURES

Proper shipping and storage, die attachment, and bonding are required to take advantage of the full performance built into PMI devices, PMI provides this information but cannot assume responsibility for technology and interface problems in applying dice, nor guarantee results in using the suggested processing methods; this information is for user assistance only and is to be used at the user's own discretion.

STORAGE

Assembly begins with storage, because dice which are metallized with aluminum will slowly oxidize if exposed to air. This action is very slow, but eventually a thin layer of aluminum oxide will form on the bonding pads. To keep oxidation to a minimum, PMI dice are stored in a temperature and humidity controlled nitrogen atmosphere at the factory until shipment.

Oxidation is a more serious problem with thermal compression gold ball bonding than it is with ultrasonic aluminum wire bonding. Ultrasonic aluminum wire bonding can penetrate a thicker layer of aluminum oxide than gold ball bonding. If thermal compression gold ball bonding is used, the devices should be bonded within a few weeks after shipment. Storage under dry nitrogen conditions is highly recommended for dice to be used with either type of bonding.

SHIPPING

Protection during shipment is provided by the waffle-pack carrier and its antistatic shield and cushioning strip. In addition the waffle pack is vacuum-sealed in a polyethylene bag.

EUTECTIC DIE ATTACHMENT CONDITIONS

The die-attach area of the package should be gold plated. While preforms are not generally required, they may be necessary in some cases depending on die size and the thickness of the package's gold plating. If required, preforms of approximately 0.65 or 0.90 mm diameter with a composition of gold-silicon 98/2 are recommended.

The heater-block used should have a sufficiently large thermal mass plus adequate control to assure a constant package temperature of 420°C ±10°C during the die-attach operation. Inert gas protection, nitrogen with a flow of approximately 30 liters/hour, is also recommended.

EUTECTIC DIE ATTACHMENT PROCEDURE

For ease of handling in die attachment, dice should first be transferred from their waffle packs to flat glass or metal plates. Allow the package to soak a sufficient time to acquire a uniform temperature. (Where necessary place a preform on the mounting surface.)

Using suitable tweezers, carefully pick up the die from the supply plate, orient properly and gently scrub in a circular or back-and-forth motion until eutectic melt is visible completely around the die. Eutectic melt should be visible completely around the periphery of the die. There should be no evidence of balling or flaking of die-attach material. After completing the die-attach operation remove the package from the heater block.

The die should be level and flat with respect to the package surface. Die attach material should not touch the top surface of the die or stand vertically above the edge of the die.

CONDUCTIVE EPOXY DIE ATTACHMENT

A solvent and other contaminant-free conductive epoxy should be used, specifically designed for die-attach use. Manufacturer's instructions should be carefully followed. While PMI uses eutectic die-attach exclusively, conductive epoxy die-attach can be used, although this technique is not as well-established.

ULTRASONIC ALUMINUM WIRE BONDING

PMI uses ultrasonic aluminum wire bonding and recommends its use for best performance. It is also more economical than gold-ball bonding. For specific procedures with either method, the detailed operation instructions of the manufacturer of the specific bonding equipment used should be carefully followed. A suitable wire for ultrasonic bonding is Aluminum-Silicon alloy 99/1, Diameter 0.001", elongation 0.5 – 2% tensile strength 14 – 16g; but again, specific instructions/recommendations related to the bonding equipment used should be observed. An average bond pull strength of 4 – 6g, and a minimum limit of 2g should be maintained to assure mechanical bond quality.

UNUSED PADS

All pads marked with (+) are not to be bonded to by user. These pads are used by the factory for testing or adjusting (zener zap) electrical parameters.

QUALITY ASSURANCE

Precision Monolithics believes that quality and reliability must be built into the product; no amount of testing can replace these inherent properties. For this reason, devices are fabricated and processed to MIL-STD-883 requirements as standard practice with many exclusive processes and controls added to improve quality and reliability. The integrity of aluminum metallization is confirmed by sampling wafer lots using a Scanning Electron Microscope (SEM) examination per Method 2018 specifications. QA testing of dice is provided by normal production testing of packaged devices.

SECTION 3

QUALITY ASSURANCE PROGRAM

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Q.A. PROGRAM

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QUALITY ASSURANCE PROGRAM DOCUMENTATION

By Howard Autry, VP/QA

INTRODUCTION

Precision Monolithics, Inc., in establishing standard procedures for Manufacturing, Screening, Qualification, and Conformance, has incorporated the requirements of both MIL-STD-883, and MIL-Q-9858. Devices meeting Class B screening requirements of MIL-STD-883, are available off-the-shelf as standard catalog items. Requests for devices with Class S or other special requirements are invited. The internal procedures designed to control and guarantee production of these devices are described herein.

PMI standard "883" parts designate devices which have been subjected to 100% screening in accordance with Method 5004 of MIL-STD-883, Class B, and have been subjected to Group A Quality Conformance Testing per Method 5005.

Complete Quality Conformance Testing (Groups A, B, C, D) in accordance with Method 5005 of MIL-STD-883 is available on special order.

1) Generic Group C & D Quality Conformance Data is available on special order. Generic Test Data is defined in accordance with D.E.S.C. selected item drawings as data from devices in the same microcircuit group (3.1.3(h) of MIL-M-38510) and package type, produced within 180 days of the deliverable devices.

- **CLASS B** — Devices inteded for use where maintenance and replacement can be performed, but are difficult and expensive, and where reliability is vital.
- **CLASS C** — Devices intended for use where maintenance and replacement can be readily accomplished and down time is not a critical factor.

Screening procedures for all 3 classes and for Precision Monolithics standard devices are shown on the following page.

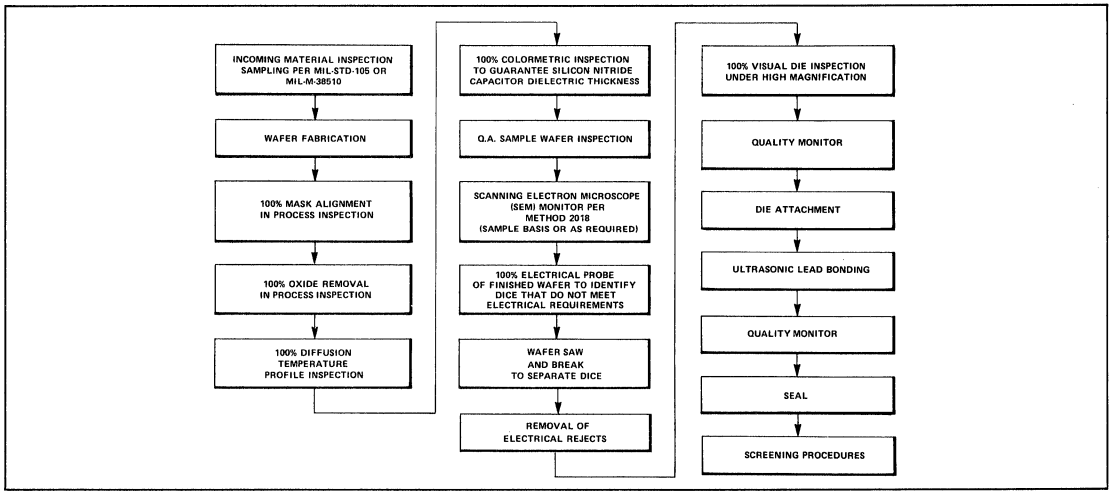
All PMI standard products (except PM series and plastics) are screened in accordance with Method 5004 of MIL-STD-883, class C or better.*

QUALIFICATION AND QUALITY CONFORMANCE PROCEDURES

MIL-STD-883 Method 5005 establishes Qualification and Quality Conformance Procedures for the 3 classes of devices and divides these procedures into group A, B, C and D tests: "The full requirements of group A, B, C and D tests and inspections are intended for use in initial device qualification, requalification in the event of product or process change and periodic testing for retention of qualification. Group A and B tests and inspections are intended for quality conformance inspection of individual inspection lots as a condition for acceptance for delivery."

Group A, B, C and D quality conformance tests are performed using a sample size determined from the LTPD table below. An initial sample size corresponding to zero rejects (an acceptance number of 0) is normally used; if necessary the sample size will be increased once to a higher number to meet the LTPD requirement for the class of device under test.

STANDARD MANUFACTURING PROCEDURE FOR ALL DEVICES



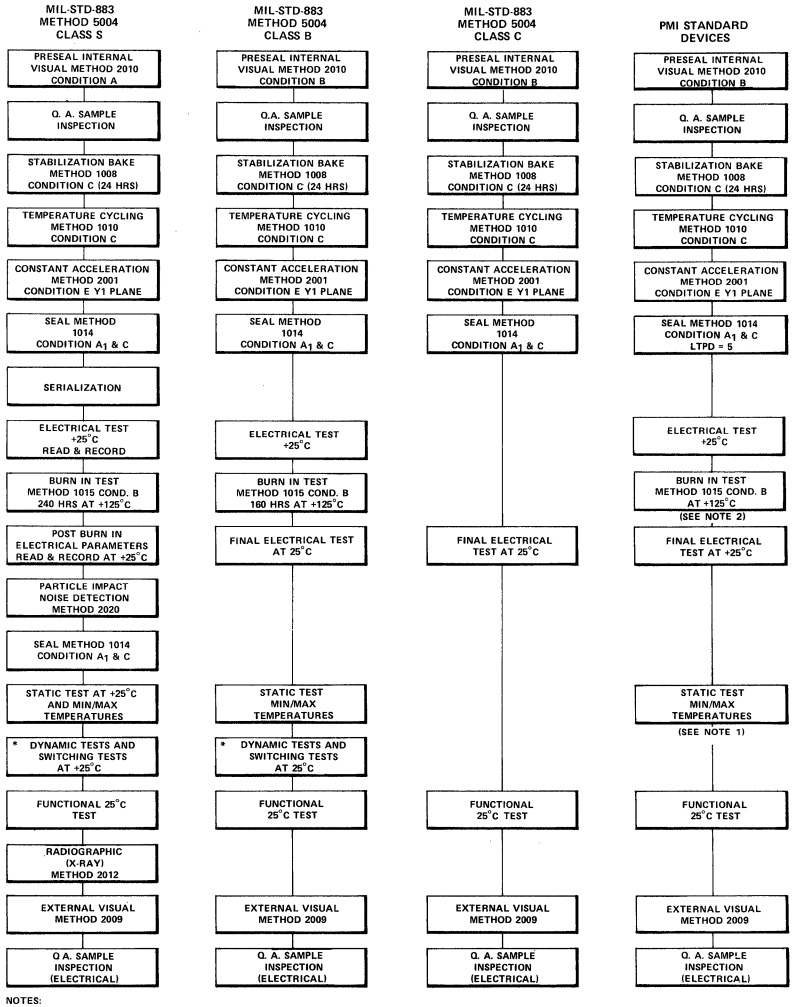
SCREENING LEVELS

MIL-STD-883 DEFINES 3 LEVELS OF MICROELECTRONIC SCREENING:

- **CLASS S** — Devices intended for use where maintenance and replacement are extremely difficult or impossible, and reliability is imperative.

*EFFECTIVE DATE CODE 8101.

SCREENING PROCEDURES



NOTES:

1. TEMP TESTING PERFORMED AS REQUIRED TO GUARANTEE DATA SHEET SPECIFICATIONS.
2. BURN-IN PERFORMED AS REQUIRED TO STABILIZE DEVICES WITH INTERNAL REFERENCES.

*AS REQUIRED BY DETAIL SPEC.

LOT TOLERANCE PERCENT DEFECTIVE (LTPD) TABLE (per MIL-M-38510)

ACCEPTANCE NUMBER*	LTPD 20	LTPD 15	LTPD 10	LTPD 7	LTPD 5	LTPD 3
			Minimum Sample Size			
0	11	15	22	32	45	76
1	18	25	38	55	77	129
2	25	34	52	75	105	176
3	32	43	65	94	132	221
4	38	52	78	113	158	265

*Maximum allowable number of failures.

GROUP A ELECTRICAL TESTS: Reference MIL-STD-883 Method 5005
(ELECTRICAL TESTS PER APPLICABLE DATA SHEET SPECIFICATIONS)

SUBGROUP	TEST DESCRIPTION	CLASS S & B LTPD	CLASS C LTPD
1	Static tests at 25°C	5	5
2	Static tests at maximum rated operating temperature	7	10
3	Static tests at minimum rated operating temperature	7	10
4	Dynamic tests at 25°C	5	5
7	Functional tests at 25°C	5	5
9	Switching tests at 25°C	7	10

GROUP B TESTS FOR CLASS S DEVICES 1/

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	CLASS S QUANTITY/(ACCEPT NO.) OR LTPD
Subgroup 1			
(a) Physical dimensions	2016		2(0)
(b) Internal water vapor content	4/ 5/		3(0) or 5(1)
Subgroup 2	2/		
(a) Resistance to solvents	2015		4(0)
(b) Internal visual for DPA	2013 & 2014	Failure criteria from design and construction requirements of applicable procurement document.	2(0)
(c) Bond Strength	2011		
(1) Ultrasonic		(1) Test Condition D	LTPD=10 6/
(d) Die shear test	2019	Per Table 1 of Method 2019 for the applicable die size	3(0)
Subgroup 3			
Solderability 3/	2003	Soldering temperature of 260°C ±10°C	LTPD=15
Subgroup 4			
Lead integrity	2004	Test Conditions B_2, lead fatigue	2(0)
Seal	1014	A_1 and C	
(a) Fine			
(b) Gross			
Lid torque	2024	5/	
Subgroup 5			
(1) Electrical parameters		Group A, Subgroups 1, 2, 3: Read and record, subgroups 4, 7, 9 attributes.	
(2) Steady state life test	1005	Condition B, 125°C, 1000 HR or 150°C, 184 HR.	
(3) Seal	1014	A_1 and C	
(a) Fine			
(b) Gross			
(4) Electrical parameters		Group A, Subgroups 1, 2, 3: Read and record, subgroups 4, 7, 9 attributes.	LTPD=5

NOTES:
1. Electrical reject devices from the same inspection lot may be used for all subgroups when end point measurements are not required.
2. For Class S lot quality conformance testing, all samples for Subgroup B2 must have been through the complete sequence of Subgroup B6 tests.
3. All devices must have been through the temperature/time exposure in burn-in. The LTPD applies to the number of leads inspected except in no case shall less than three devices be used to provide the number of leads required.
4. Not required if Group D performed on same lot.
5. Glass frit sealed devices only.
6. LTPD refers to the number of wires to be pulled from a minimum of four devices.
7. Required for initial qualification or redesign only.

GROUP B TESTS FOR CLASS S DEVICES (Continued)

TEST	METHOD	MIL-STD-883 CONDITION	CLASS S QUANTITY/(ACCEPT NO.) OR LTPD
Subgroup 6 2/			
(a) Electrical parameters		Group A, Subgroups 1, 2, 3: Read and record	
(b) Temperature cycling	1010	Condition C 100 cycles/min.	LTPD=15
(c) Constant acceleration	2001	Test Condition E: Y_1 axes	
(d) Seal	1014	Test Condition A_1 and C	
(1) Fine			
(2) Gross			
(e) Electrical parameters		Group A, Subgroups 1, 2, 3: Read and record	
Subgroup 7 7/			
(a) Electrical parameters		Group A, Subgroup 1	
(b) Electrostatic discharge sensitivity	3015	Test Condition A or B	15(0)
(c) Electrical parameters		Group A, Subgroup 1	

NOTES:
1. Electrical reject devices from the same inspection lot may be used for all subgroups when end point measurements are not required.
2. For Class S lot quality conformance testing, all samples for Subgroup B2 must have been through the complete sequence of Subgroup B6 tests.
3. All devices must have been through the temperature/time exposure in burn-in. The LTPD applies to the number of leads inspected except in no case shall less than three devices be used to provide the number of leads required.
4. Not required if Group D performed on same lot.
5. Glass frit sealed devices only.
6. LTPD refers to the number of wires to be pulled from a minimum of four devices.
7. Required for initial qualification or redesign only.

GROUP B TEST FOR CLASSES B AND C 1/

TEST	METHOD	MIL-STD-883 CONDITION	CLASSES B & C LTPD QUANTITY/(ACCEPT NO.)
Subgroup 1			
Physical dimensions	2016		2 devices (No failures)
Subgroup 2			
Resistance to solvents	2015		4 devices (No failures)
Subgroup 3			
Solderability 3/	2003	Soldering temperature of 260° C ±10° C	15
Subgroup 4			
Internal visual and mechanical	2014	Failure criteria from design and construction requirements of applicable procurement document.	1 device (No failures)
Subgroup 5			
Bond strength 2/ Ultrasonic or wedge	2011	Test Condition D	15
Subgroup 7			
Seal			
(a) Fine	1014		5
(b) Gross			
Subgroup 8 4/			
(a) Electrical parameters		Group A, Subgroup 1	
(b) Electrostatic discharge sensitivity	3015	Test Condition A or B	15(0)
(c) Electrical parameters		Group A, Subgroup 1	

NOTES:
1. Electrical reject devices from the same inspection lot may be used for all subgroups when end point measurements are not required.
2. LTPD refers to number of wires to be pulled from a minimum of 4 devices.
3. All devices must have been through the temperature/time exposure in burn-in. The LTPD applies to the number of leads inspected except in no case shall less than three devices be used to provide the number of leads required.
4. Required for initial qualification or redesign only.

GROUP C (DIE-RELATED TESTS) FOR CLASSES B AND C ONLY

TEST	METHOD (MIL-STD-883)	CONDITION	LTPD
Subgroup 1			
Steady state life test 1/	1005	Test Condition B (1000 hours, +125°C) or (184 hours, +150°C)	5
End point electrical parameters		As specified in the applicable device specification	
Subgroup 2			
Temperature cycling	1010	Test Condition C	15
Constant acceleration	2001	Test Condition E min. Y_1 axis	
Seal	1014	Test Condition A_1 and C	
(a) Fine			
(b) Gross			
Visual examination	2/		
End point electrical parameters		As specified in the applicable device specification	

NOTES:
1. See 40.4 of Appendix B of MIL-M-38510 and 3.1 of Method 1005.
2. Visual examination shall be in accordance with method 1010 or 1011.

GROUP D (PACKAGE RELATED TESTS) FOR ALL CLASSES

TEST	METHOD (MIL-STD-883)	CONDITION	LTPD
Subgroup 1			
Physical dimensions	2016		15
Subgroup 2			
Lead integrity	2004	Test Condition B2 (lead fatigue)	
Seal	1014	Conditions A_1 and C	
(a) Fine			
(b) Gross			
Lid torque 4/	2024		
Subgroup 3 1/			
Thermal shock	1011	Test Condition B as a minimum, 15 cycles minimum	15
Temperature cycling	1010	Test condition C, 100 cycles minimum	
Moisture resistance	1004		
Seal	1014	Condition A_1 and C	
(a) Fine			
(b) Gross			
Visual examination		Per visual criteria of method 1004 and 1010	
End point electrical parameters		As specified in the applicable device specification	

NOTES:
1. Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical".
2. Visual examination shall be in accordance with method 1010 at a magnification of 5X to 10X.
3. Visual examination shall be performed in accordance with method 2007 for evidence of defects or damage to case, leads, or seals resulting from testing (not fixturing). Such damages shall constitute a failure.
4. Glass frit sealed devices only.

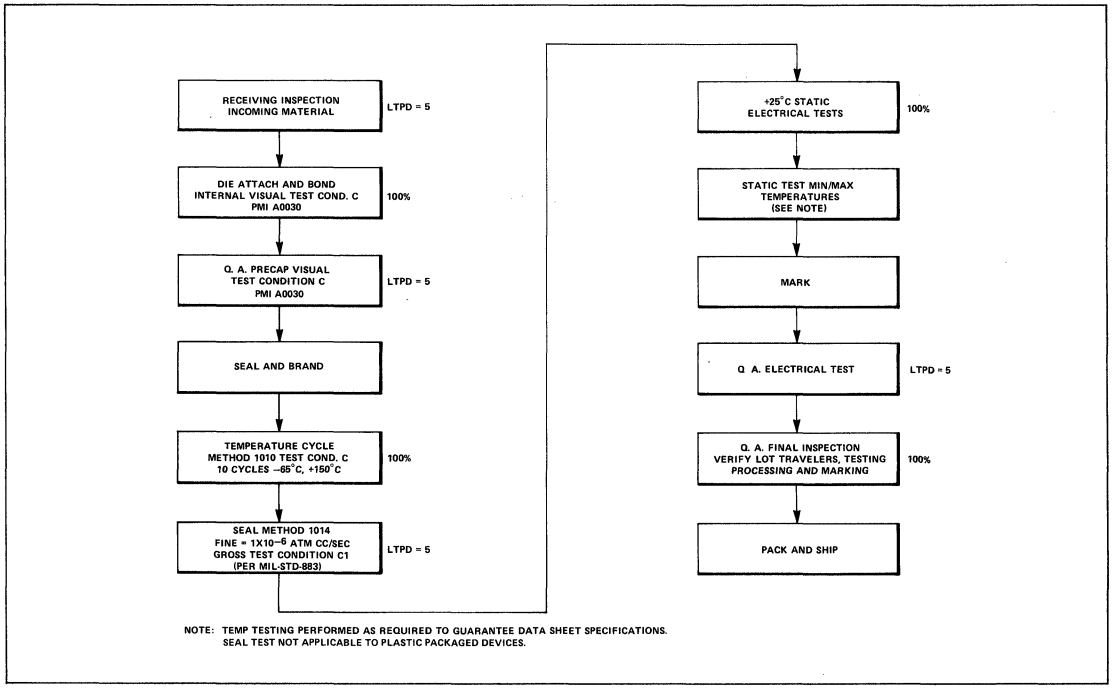
GROUP D (PACKAGE RELATED TESTS) FOR ALL CLASSES (Continued)

TEST	MIL-STD-883 METHOD	CONDITION	LTPD
Subgroup 4 1/			
Mechanical shock	2002	Test Condition B	15
Vibration variable frequency	2007	Test Condition A	
Constant acceleration	2001	Test Condition E, Y_1 axis	
Seal	1014	Condition A_1 and C	
(a) Fine			
(b) Gross			
Visual examination	3/		
End point electrical parameters		As specified in the applicable device specification	
Subgroup 5			
Salt atmosphere	1009	Test Condition A	15
Seal			
(a) Fine			
(b) Gross	1014	Condition A_1 and C	
Visual examination		Per visual criteria of method 1009	
Subgroup 6			
Internal water — vapor content	1018	5,000ppm max water content at 100° C	3 Devices (0) Failure 5 Devices (1) Failure
Subgroup 7			
Adhesion of lead finish	2025	1010 or 1011	15

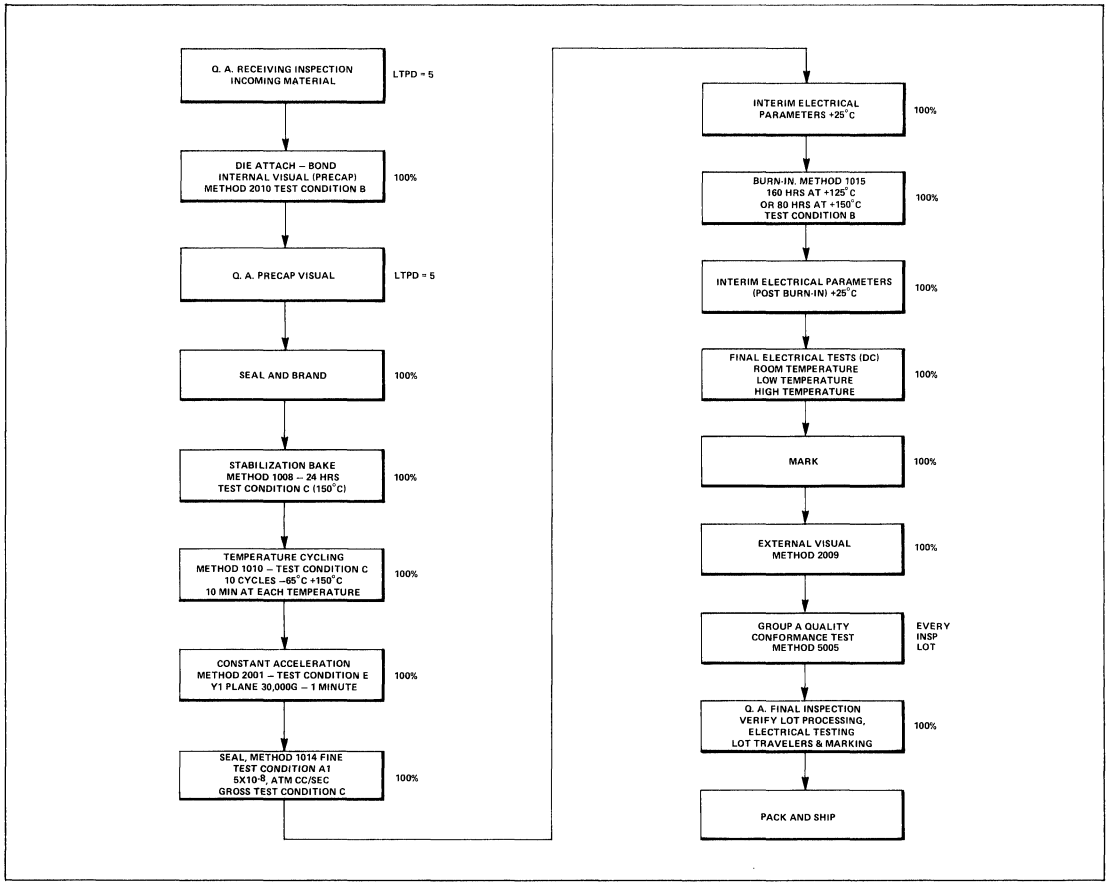
NOTES:
1. Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical".
2. Visual examination shall be in accordance with method 1010 at a magnification of 5X to 10X.
3. Visual examination shall be performed in accordance with method 2007 for evidence of defects or damage to case, leads, or seals resulting from testing (not fixturing). Such damages shall constitute a failure.

PMI STANDARD PRODUCT FLOW FOR:

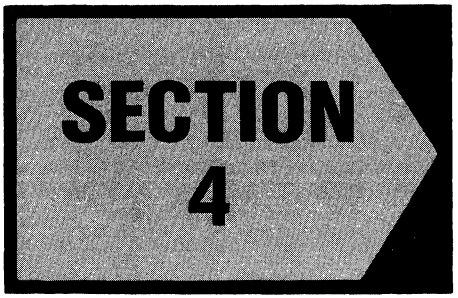
PM SERIES AND PLASTIC PACKAGED DEVICES.



PMI MIL-STD-883 CLASS B SCREENING AND QUALITY CONFORMANCE TESTING*



*Applicable to all standard "883" grade devices.



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IC CROSS REFERENCE

The following tables show both direct and functional equivalents to other manufacturers' devices. Performance and functionality are similar for functional replacements although electrical and mechanical specifications differ. Pin-for-pin equivalents are similar in electrical performance and are direct, plug-in replacements.

ANALOG DEVICES	PIN-FOR-PIN EQUIVALENT	PMI NEAREST FUNCTIONAL EQUIVALENT	PMI DIFFERENCES
AD DAC08	DAC-08		
AD07	OP-07		
AD101	OP-18		No DC balance capability. Prime grade has 0.5mV V_{OS} and 8μV/°C TCV_{OS}.
ADG200	SW-05		Bipolar, immune to static electricity.
ADG201	SW-201/SW-01		Use SW-01 for temperature compensated R_{ON}.
AD381	OP-15		
AD503		OP-15	TCV_{OS} of 5μV/°C offset null to V+.
AD504		OP-05	Nulled.
AD507	OP-16/OP-17		TCV_{OS} = 5μV/°C.
AD509		OP-16	Fast settling.
AD510		OP-05/OP-07	Unnulled. 0.6μV/°C TCV_{OS}. Pin compatible.
AD517		OP-21/OP-07	350μA power consumption. Pin compatible. 0.6μV/°C TCV_{OS}. Pin compatible
AD518		OP-01	Inverting configuration only. 2mV, V_{OS}, 8μV/°C TCV_{OS}.
AD540		OP-15	0.5mV, V_{OS}, 5μV/°C, TCV_{OS}. Offset null to V+.
AD542		OP-15	0.5mV/V_{OS} offset null to V+.
AD544		OP-15	Offset null to V+.
AD545		OP-15	10V/μs slew rate.
AD558		DAC-888	Multiplying, faster.
AD559		DAC-08	Multiplying.
AD561		DAC-100/DAC-101	Not pin-for-pin.
AD580		REF-02	+5V reference.
AD581		REF-01	
AD582		SMP-10	Faster acquisition time.
AD583		SMP-10/SMP-11	Very low droop rate. Pin compatible in unity gain configuration.
AD590		REF-02	Has pin providing output voltage proportional to temperature.

ANALOG DEVICES	PIN-FOR-PIN EQUIVALENT	PMI NEAREST FUNCTIONAL EQUIVALENT	PMI DIFFERENCES
AD741	OP-02		
AD810	MAT-01		See MAT-01 Selection Guide.
AD818		MAT-01	Log amplitude.
AD1408/1508	DAC-1408/1508		
AD2700		REF-01	IC and low power.
AD7110		DAC-78	DAC-78 has higher resolution.
AD7501		MUX-08	Immune to static electricity.
AD7502		MUX-08	Immune to static electricity.
AD7503		MUX-08	Immune to static electricity. Inverted enable logic.
AD7506	MUX-16		Immune to static electricity.
AD7507	MUX-28		Immune to static electricity.
AD7510	SW-7510		Immune to static electricity.
AD7511	SW-7511		Immune to static electricity.
AD7516		SW-7510	Wider analog signal range.
AD7520/7530/7533		DAC-10	Bipolar, high compliance.
AD7524		DAC-808/DAC-888	Bipolar.
HDH 0802		DAC-208	Monolithic, low cost, slower.
HDH 1003		DAC-210	Monolithic, low cost, slower.
HDH 1025		DAC-10	Monolithic, low cost, slower.
FET Op-Amps		OP-15/OP-16/OP-17	Select according to application.

ADVANCED MICRO DEVICES	PIN-FOR-PIN EQUIVALENT	PMI NEAREST FUNCTIONAL EQUIVALENT	PMI DIFFERENCES
AM1408	DAC-1408		
AM1508	DAC-1508		
AM6012	DAC-312		
AM6070	DAC-76		
DAC-08	DAC-08		
SSS725	OP-06		
SSS741	OP-02		

ADVANCED MICRO DEVICES	PIN-FOR-PIN EQUIVALENT	PMI NEAREST FUNCTIONAL EQUIVALENT	PMI DIFFERENCES
SSS747	OP-03/OP-04		
SSS1508	DAC-1508		
AM685		CMP-05	Lower Error.
AM686		CMP-05	Lower Error.
AM687		CMP-05	Lower Error.
AM6071		DAC-89	Improved Specs.
AM6072		DAC-88	Improved Specs.
AM6080		DAC-888	Faster.

BURR-BROWN	PIN-FOR-PIN EQUIVALENT	PMI NEAREST FUNCTIONAL EQUIVALENT	PMI DIFFERENCES
BB3500		OP-15	V_{OS} 0.5mV, TCV_{OS} 5μV/° C.
BB3501		OP-15	Null to V+, f_t = 4MHz
BB3505		OP-16	Highest speed applications.
BB3506		OP-15/OP-16/OP-17	Medium speed application. Depends on configuration.
BB3510		OP-07	Pin compatible, 25μV, V_{OS}.
BB3521		OP-15	Null to V+, 10V/μs slew rate.
BB3522		OP-15	Null to V+, 10V/μs slew rate.
BB3542		OP-15	Null to V+, 10V/μs slew rate.
BB3550		OP-15	Null to V+, 10V/μs slew rate.
DAC-82		DAC-208	Different REF, faster response.
MPC4D	MUX-24		High immunity to static electricity.
MPC8D	MUX-28		High immunity to static electricity.
MPC8S	MUX-08		High immunity to static electricity.
MPC16S	MUX-16		High immunity to static electricity.
SHC298		SMP-10/SMP-11	Specified zero-scale error.

DATEL	PIN-FOR-PIN EQUIVALENT	PMI NEAREST FUNCTIONAL EQUIVALENT	PMI DIFFERENCES
MV-808	MUX-08		High immunity to static electricity.
MV-1606	MUX-16		High immunity to static electricity.
MVD-409	MUX-24		High immunity to static electricity.
MVD-807	MUX-28		High immunity to static electricity.
MX-808	MUX-08		High immunity to static electricity.
MX-1606	MUX-16		High immunity to static electricity.
MXD-409	MUX-24		High immunity to static electricity.
MXD-807	MUX-28		High immunity to static electricity.
SHM-IC-1		SMP-10/11	Pin-for-pin replacement in unity gain configuration.
SHM-LM-2		SMP-10/11	Improved input specifications.
DAC-198B		DAC-208	Monolithic, faster.
DAC-98BIR		DAC-100	Monolithic, faster.
DAC-98BI		DAC-10	Monolithic, faster.
DAC-198BI		DAC-08	Monolithic, faster.
DAC-298B		DAC-208	Monolithic, faster.
DAC-4910B		DAC-210	Monolithic, faster.
DAC-4910BI		DAC-10	Monolithic, faster.
DAC-I8B		DAC-08	Monolithic, faster.
DAC-I10B		DAC-10	Monolithic, faster.
DAC-IC8BC/BM	DAC-1508/1408		
DAC-08BC/BM	DAC-08		
DAC-UP8B		DAC-888	Multiplying, faster.
DAC-IC10B		DAC-10	Faster.
DAC-V8B		DAC-208	Faster, monolithic.
DAC-V10B		DAC-210	Faster, monolithic.

FAIRCHILD	PIN-FOR-PIN EQUIVALENT	PMI NEAREST FUNCTIONAL EQUIVALENT	PMI DIFFERENCES
LM108	PM-108/OP-08		
LM208	PM-208/OP-08		
LM308	PM-308/OP-08		
725	OP-06		
741	PM-741/OP-02		
747	PM-747/OP-04		
801	DAC-08		
802	DAC-1508		
714	OP-07		
μA155/6/7	PM-155/6/7 OP-15/16/17		
μA255/6/7	PM-255/6/7 OP-15/16/17		
μA355/6/7	PM-355/6/7 OP-15/16/17		

HARRIS SEMICONDUCTOR	PIN-FOR-PIN EQUIVALENT	PMI NEAREST FUNCTIONAL EQUIVALENT	PMI DIFFERENCES
HA-2420		SMP-10/SMP-11	Pin compatible in unity gain configurations.
HA-2425		SMP-10/SMP-11	Pin compatible in unity gain configurations.
HA-2510		OP-16	PMI's OP-15/16/17 replaces several Harris types in some applications.
HA-2720		OP-20	Improved DC specs.
HA-2900		OP-07	See also AN-13.
HA-4950		CMP-05	Superior input specifications.
HA-4900		CMP-04	Single supply operation
HA-4905		CMP-04	Single supply operation
HI-201	SW-201		Use SW-01 for temperature compensated R_{ON}.
HI-200	SW-05		Over voltage protected.
HI-506	MUX-16		Over voltage protected.
HI-506A	MUX-16		Lower R_{ON}.

HARRIS SEMICONDUCTOR	PIN-FOR-PIN EQUIVALENT	PMI NEAREST FUNCTIONAL EQUIVALENT	PMI DIFFERENCES
HI-507	MUX-28		Over voltage protected.
HI-507A	MUX-28		Lower R_{ON}.
HI-508	MUX-08		Over voltage protected.
HI-508A	MUX-08		Lower R_{ON}.
HI-509	MUX-24		Over voltage protected.
HI-509A	MUX-24		Lower R_{ON}.
HI-1828A		MUX-24	Lower leakage currents.
HI-5610		DAC-10	18-Pin package, similar specs/speed.
HI-1818A		MUX-08	Lower leakage currents.
HI-5618		DAC-08	16-Pin package, similar specs/speed.

HYBRID SYSTEMS	PIN-FOR-PIN EQUIVALENT	PMI NEAREST FUNCTIONAL EQUIVALENT	PMI DIFFERENCES
DAC221M-10		DAC-10	Monolithic, faster.
DAC337C		DAC-03	Monolithic, faster, flexible supplies.
DAC331-8		DAC-08	Faster, better specs.
DAC337		DAC-208	Faster, better specs.
DAC371		DAC-100	Faster, better specs, monolithic.
DAC371V		DAC-208	Faster, better specs, monolithic.
DAC372		DAC-208	Faster, better specs, monolithic.
DAC3851		DAC-100	Faster, better specs, monolithic.
DAC331-10		DAC-10	Faster, better specs, monolithic.
DAC3721-10		DAC-100	Faster, better specs, monolithic.
DAC371-10		DAC-210	Faster, better specs, monolithic.

INTERSIL	PIN-FOR-PIN EQUIVALENT	PMI NEAREST FUNCTIONAL EQUIVALENT	PMI DIFFERENCES
AD7520/30/33		DAC-10	Bipolar, high compliance/speed.
IH200	SW-05		Break-before—make switching.
IH201	SW-201		Use SW-01 for temperature compensated R_{ON}.

INTERSIL	PIN-FOR-PIN EQUIVALENT	PMI NEAREST FUNCTIONAL EQUIVALENT	PMI DIFFERENCES
IH202	SW-202		Use SW-02 for temperature compensated R_{ON}.
IH6006	MUX-16		Full TTL/CMOS logic compatibility.
IH6108	MUX-08		Full TTL/CMOS logic compatibility.
IH6208	MUX-08/MUX-24		Full TTL/CMOS logic compatibility.
IH6216	MUX-28		Full TTL/CMOS logic compatibility.

MICRO NETWORKS	PIN-FOR-PIN EQUIVALENT	PMI NEAREST FUNCTIONAL EQUIVALENT	PMI DIFFERENCES
MN3013/3014		DAC-208	Monolithic, better specs.
MN3008/9		DAC-208	Monolithic.
MN3000/1/2/6		DAC-208	Monolithic, faster.
MN3003/4/5/7		DAC-210	Monolithic, faster.
MN3015		DAC-10/DAC-101	Monolithic, faster.
MN3020		DAC-808	Current output.
MN3005		DAC-03	Monolithic, faster, flexible supplies.
MN3010		DAC-20	Monolithic, faster, more accurate.
MN3100		DAC-10	Monolithic, faster, flexible supplies.

MOTOROLA	PIN-FOR-PIN EQUIVALENT	PMI NEAREST FUNCTIONAL EQUIVALENT	PMI DIFFERENCES
MC1504U5	REF-02		
MC1404U5	REF-02		
MC1404U10	REF-01		
MC1408	DAC-1408		
MC1504U10	REF-01		
MC1458	OP-14		
MC1508	DAC-1508		
MC1500U5	REF-02		
MC1500U10	REF-01		
MC1558	OP-14		

MOTOROLA	PIN-FOR-PIN EQUIVALENT	PMI NEAREST FUNCTIONAL EQUIVALENT	PMI DIFFERENCES
MC1400U5	REF-02		
MC1400U10	REF-01		
MC3502		OP-15/OP-16	
MC3510		DAC-100/DAC-10	Faster, higher compliance.
MC34022		OP-15/OP-16	
MC3302	CMP-04		Improved specs.

NATIONAL SEMICONDUCTOR	PIN-FOR-PIN EQUIVALENT	PMI NEAREST FUNCTIONAL EQUIVALENT	PMI DIFFERENCES
AD7520		DAC-10	Bipolar, high speed/compliance.
DAC0800/0801/0802	DAC-08		
DAC0808/0807/0806	DAC-1408/1508		
DAC1020		DAC-10	Bipolar, high speed.
DAC1220		DAC-312	Bipolar, high speed.
DAC1201		DAC-312	Current output, ext. ref.
LF155	PM-155		
LF156	PM-156		
LM139	PM-139/CMP-04		Improved specs.
LM161		CMP-05	Improved input specs.
LF157	PM-157		
LF198/298/398		SMP-10/11	Low zero scale error.
LM199		REF-01/02	Lower power consumption.
LF255	PM-255		
LF256	PM-256		
LF257	PM-257		
LF356	PM-356		
LF357	PM-375		
LF11202/12201/13201	SW-01		Use SW-02 for temperature compensated R_{ON}.
LF11202/12202/13202	SW-02		Use SW-02 for temperature compensated R_{ON}.
LF11331/12331/13331		SW-04	Temperature compensated R_{ON}.

NATIONAL SEMICONDUCTOR	PIN-FOR-PIN EQUIVALENT	PMI NEAREST FUNCTIONAL EQUIVALENT	PMI DIFFERENCES
LF11332/12332/13332		SW-03	Temperature compensated R_{ON}.
LF11508/12508/13508	MUX-08		Lower R_{ON}
LF11509/12509/13509	MUX-24		Lower R_{ON}
LH002		BUF-03	Improved DC accuracy.
LH0001		OP-20	Improved DC specs.
LH0023		SMP-10/11	Low zero scale error.
LH0033		BUF-03	Improved DC accuracy.
LH0043		SMP-10/11	Improved speed and DC accuracy.
LH0044		OP-07	Applications where less than 1mA supply current is required.
LH0053		SMP-10/SMP-11	Improved speed and DC accuracy.
LH0070		REF-01	Low power dissipation.
LH0071		REF-01	Low power dissipation.
LH2108	PM-2108/PM-2108A		
LH2208	PM-2208/PM-2208A		
LH2308	PM-2308/PM-2308A		
LMDAC08	DAC-08		
LM108/208/308	PM-108/208/308		Improved V_{OS}.
LM110/210/310		BUF-01/BUF-02	Total D.C. error lower.
LM114/115		MAT-01	See MAT-01 Selection Guide.

RAYTHEON	PIN-FOR-PIN EQUIVALENT	PMI NEAREST FUNCTIONAL EQUIVALENT	PMI DIFFERENCES
LM108	PM-108/OP-08		
LM208	PM-208/OP-08		
LM308	PM-308/OP-08		
RC725	PM-725/OP-06		
RC741	PM-741/OP-02		
RC747	OP-03/OP-04		
RC1458	PM-1458/OP-14		
RC4132	OP-20		

RAYTHEON	PIN-FOR-PIN EQUIVALENT	PMI NEAREST FUNCTIONAL EQUIVALENT	PMI DIFFERENCES
RC4136	PM-4136/OP-09		
RM725	PM-725/OP-06		
RM741	PM-741/OP-02		
RM747	PM-747/OP-03/OP-04		
RM1558	PM-1558/OP-14		
RM4136	PM-4136/OP-09		
RM4132	OP-20		
DAC08	DAC-08		

RCA	PIN-FOR-PIN EQUIVALENT	PMI NEAREST FUNCTIONAL EQUIVALENT	PMI DIFFERENCES
CA108	PM-108		
CA208	PM-208		
CA308	PM-308		
CA741	PM-741/OP-02		
CA747	PM-747/OP-03/OP-04		
CA1458	OP-14		
CA1558	PM-1558/OP-14		

SIGNETICS	PIN-FOR-PIN EQUIVALENT	PMI NEAREST FUNCTIONAL EQUIVALENT	PMI DIFFERENCES
MC1408/1508	DAC-1408/1508/ DAC-08		Improved replacement.
NE5537		SMP-11	Improved performance.
NE/SE5007/5008	DAC-08		
NE/SE5009	DAC-08		
NE/SE5534		OP-27/37	Lower noise, current out.
NE5118/5119		DAC-888	
5018		DAC-808	18-Pin package, current out.

SILICONIX	PIN-FOR-PIN EQUIVALENT	PMI NEAREST FUNCTIONAL EQUIVALENT	PMI DIFFERENCES
DG200	SW-05		Over voltage protected.
DG201	SW-201		Lower R_{ON}.
DG211	SW-01		Temperature compensated R_{ON}.
DG300		SW-05	BIFET.
DG506	MUX-16		Over voltage protected.
DG507	MUX-28		Over voltage protected.
DG508	MUX-08		Over voltage protected.
DG509	MUX-24		Over voltage protected.

TEXAS INSTRUMENTS	PIN-FOR-PIN EQUIVALENT	PMI NEAREST FUNCTIONAL EQUIVALENT	PMI DIFFERENCES
SN52558	PM-1558/OP-14		
SN52741	PM-741/OP-02		
SN72747	PM-747/OP-03/OP-04		
SN72558	DAC-1458/OP-14		
SN72741	PM-741/OP-02		
SN72747	OP-03/OP-04		
TL081	OP-16		
TL085	OP-215		

SECTION 5

OPERATIONAL AMPLIFIERS

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INTRODUCTION

At Precision Monolithics we introduced our first Op Amp in 1970 and since then we have constantly strived to meet the needs of the electronic industry. PMI has done this by offering a complete and versatile series of operational amplifiers.

The Op Amp product line at PMI includes a variety of widely accepted proprietary and second-source products. These products are designed and manufactured from a diverse technology base that includes linear bipolar, super-beta, and BIFET processing techniques along with Zener Zap trimming. This technology base combined with superior design, layout, and processing techniques provides products with outstanding performance and reliability. Single, Dual, and Quad amplifiers are offered in plastic, metal and ceramic packages in military, industrial, and commercial temperature ranges.

Over the past several years, the sophistication and diversity required of op amps has increased dramatically. High speed, high input impedance, low noise, and ultra low power have been just a few of the many areas in which monolithic op amps have made significant inroads. This has often made the selection of appropriate operational amplifiers as difficult as the design of a system using them. As with most designs, over-specification can be costly and under-specification can seriously affect system performance.

To overcome this problem, we've developed the selection guides on the following pages. The simplified guide below lists the basic application requirements for Op Amps and the PMI amplifier family that is most likely to fill that requirement. Consult the following pages for selection guides listing the key performance parameters of the products in these families.

REQUIREMENTS	PRODUCT FAMILY
High Speed	JFET Input, Audio/ Commercial
Low Power Consumption	Super β, μPower
Low Input Offset Voltage	Instrumentation
High Input Impedance	JFET Input, Super β
Stability with Time and Temp	Instrumentation, Super β
Single Supply	μPower
Ultra High Gain	Instrumentation
Matched Performance Duals	Instrumentation Duals, General Purpose Duals
Matched Performance Quad	General Purpose Quads

DEFINITIONS

AVERAGE BIAS CURRENT DRIFT (TCI_B)

The ratio of the change in the input bias current to the change in temperature producing it.

AVERAGE OFFSET CURRENT DRIFT (TCI_{OS})

The ratio of the change in the input offset current to the change in temperature producing it.

AVERAGE OFFSET VOLTAGE DRIFT (TCV_{OS})

The ratio of the change in the input offset voltage to the change in temperature producing it.

AVERAGE OFFSET VOLTAGE DRIFT WITH EXTERNAL TRIMMING (TCV_{OSN})

The ratio of the change in the input offset voltage to the change in temperature producing it, with the input offset voltage trimmed to zero at room temperature.

COMMON-MODE INPUT RESISTANCE (R_{inCM})

The ratio of the input voltage range to the change in input bias current over this range.

COMMON-MODE REJECTION RATIO (CMRR)

The ratio of the common-mode voltage range (CMVR) to the peak-to-peak change in equivalent input offset voltage (CME) over this range. CMRR is specified for a specific CMVR. CMRR = 20 $\log_{10}$ (CMVR/CME)

GAIN-BANDWIDTH PRODUCT (GBW)

The frequency at which the open-loop gain equals unity.

INPUT BIAS CURRENT (I_B)

The average of the currents into the two input terminals when the output is at zero volts with no load.

INPUT NOISE CURRENT (i_{np-p})

The peak-to-peak noise current within a specified frequency band.

INPUT NOISE CURRENT DENSITY (i_n)

The rms noise current in a 1Hz band centered on a specified frequency.

INPUT NOISE VOLTAGE (e_{np-p})

The peak-to-peak noise voltage within a specified frequency band.

INPUT NOISE VOLTAGE DENSITY (e_n)

The rms noise voltage in a 1Hz band centered on a specified frequency.

INPUT OFFSET CURRENT (I_{OS})

The difference between the currents into the two input terminals when the output is at zero volts with no load.

INPUT OFFSET VOLTAGE (V_{OS})

The voltage which must be applied between the input terminals to obtain zero output voltage with no load.

INPUT RESISTANCE-DIFFERENTIAL MODE (R_{IN})

The ratio of the small-signal change in input voltage to the change in input current at either input terminal with the other grounded.

INPUT VOLTAGE RANGE (IVR)

The range of input voltage for which the device will operate linearly.

LARGE-SIGNAL VOLTAGE GAIN (A_{VO})

The ratio of the change in output voltage (over a specified range) to the change in input voltage producing it.

OPEN-LOOP OUTPUT RESISTANCE (R_O)

The small-signal driving point resistance of the output terminal with respect to ground at a specified quiescent dc output voltage and current.

OUTPUT VOLTAGE SWING (V_O)

The peak output voltage that can be obtained without clipping.

POWER DISSIPATION (P_d)

The total power dissipated in the amplifier with the output at zero volts with no load.

POWER-SUPPLY REJECTION RATIO (PSRR)

The inverse ratio of the change in input offset voltage to the change in power supply voltage producing it. PSRR can be specified in dB or μV/V.

SLEW RATE (SR)

The ratio of a change in output voltage to the minimum time required to effect this change under large-signal drive conditions. Slew rate may be specified separately for positive and negative-going changes.

SUPPLY CURRENT (I_{SY})

The current required from the power supply to operate the amplifier with no load and the output at zero volts.

UNITY-GAIN CLOSED-LOOP BANDWIDTH (BW)

The frequency at which the magnitude of the small signal voltage gain of the amplifier, operated closed-loop as a unity-gain follower, is 3dB below unity.

MATCHING PARAMETER DEFINITIONS

INPUT OFFSET VOLTAGE MATCH (ΔV_{OS})

The difference between the offset voltages of side A and side B ($V_{OSA} - V_{OSB}$). If $V_{OSA} = V_{OSB}$, the net differential offset voltage at the output of the amplifier pair equals zero.

INPUT OFFSET VOLTAGE TRACKING ($TC\Delta V_{OS}$)

The ratio of the change in ΔV_{OS} to the change in temperature producing it.

AVERAGE NON-INVERTING BIAS CURRENT (I_B+)

The average of the side A and side B non-inverting input bias currents:

$$\frac{I_{BA}+ + I_{BB}+}{2}$$

NON-INVERTING INPUT OFFSET CURRENT ($I_{OS}+$)

The difference between the non-inverting input bias currents of side A and side B; ($I_{BA}+ - I_{BB}+$).

INVERTING INPUT OFFSET CURRENT ($I_{OS}-$)

The difference between the inverting input bias currents of side A and side B; ($I_{BA}- - I_{BB}-$).

AVERAGE DRIFT OF NON-INVERTING BIAS CURRENT (TCI_B+)

The ratio of the change in non-inverting bias current to the change in temperature producing it.

AVERAGE DRIFT OF NON-INVERTING OFFSET CURRENT ($TCI_{OS}+$)

The ratio of the change in non-inverting offset current to the change in temperature producing it.

COMMON-MODE REJECTION RATIO MATCH (ΔCMRR)

The difference between the common-mode rejection ratios (expressed in volt/volt) of side A and side B. ΔCMRR in dB = 20 $\log_{10}$ (ΔCMRR in volt/volt).

SUPPLY-VOLTAGE REJECTION-RATIO MATCH (ΔPSRR)

The difference between the power-supply rejection-ratios (expressed in volt/volt) of side A and side B. ΔPSRR in dB = 20 $\log_{10}$ (ΔPSRR in volt/volt).

CHANNEL SEPARATION

The ratio of the change in offset voltage of one channel to the change in output voltage in the second channel producing it.

PRODUCT SELECTOR - OPERATIONAL AMPLIFIERS

Product	Offset Voltage (mV)	Bias Current (nA)	Offset Current (nA)	Drift (μV/° C)	Bandwidth (MHz)	SR (V/μs)	Supply Current (mA)
SINGLE OP AMPS							
GENERAL PURPOSE							
OP-01	0.7	30	2	8.0	2.5	18	3.0
OP-02	0.5	30	2	8.0	0.8	0.25	2.4
OP-18	0.5	50	5	8.0	6	0.25	3.0
OP-19	0.5	50	5	8.0	0.8	0.8	3.0
PM-741	5	500	200	30	0.8	0.25	2.8
JFET INPUT							
OP-15	0.5	0.11	.022	5	4	10	4
OP-16	0.5	0.13	.025	5	6	18	7
OP-17	0.5	0.13	.025	5	20	45	7
PM-155	2	0.15	.040	5	2.5	3	4
PM-156	2	0.19	.050	5	4	10	7
PM-157	2	0.19	.050	5	15	40	7
INSTRUMENTATION							
OP-05	0.15	±2	2	0.5	0.4	0.1	4
OP-06	0.2	70	2	0.6	1000	100	4
OP-07	0.025	±2	2	0.6	0.4	0.1	4
OP-27	0.025	±40	35	0.6	5.0	1.7	4.7
OP-37	0.025	±40	35	0.6	45	11	4.7

PRODUCT SELECTOR - OPERATIONAL AMPLIFIERS

Product	Offset Voltage (mV)	Bias Current (nA)	Offset Current (nA)	Drift (μV/° C)	Bandwidth (MHz)	SR (V/μs)	Supply Current (mA)
SINGLE OP AMPS							
SUPER BETA							
OP-08	0.15	2	0.2	2.5	0.8	0.12	0.6
OP-12	0.15	2	0.2	2.5	0.8	0.12	0.6
PM-108	0.5	2	0.2	5	0.8	0.12	0.6
MICRO POWER							
OP-20	0.25	25	1.5	1.5	0.1	0.05	0.08
OP-21	0.1	100	4.0	1.0	0.6	0.25	0.30
AUDIO/COMMERCIAL							
OP-24	0.17	±85	90	2.0	5.0	1.7	4.7
OP-34	0.17	±85	90	2.0	45	11	4.7
DUAL OP AMPS							
GENERAL PURPOSE							
OP-03	0.75	50	5	8	0.8	0.25	6.0 (Total)
OP-04	0.75	50	5	8	0.8	0.25	6.0 (Total)
OP-14	0.75	50	5	8	0.8	0.25	6.0 (Total)
PM-747	5.0	500	200	30	0.8	0.25	5.7 (Total)
PM-1458/1558	6.0	500	200	30	0.8	0.25	5.0 (Total)
JFET INPUT							
OP-215	1.0	0.3	0.1	10	3.5	10.0	8.5 (Total)
INSTRUMENTATION							
OP-10	0.5	± 3	2.8	1.0	0.6	0.17	8.0 (Total)
OP-207	0.1	± 3	2.8	1.3	1.2	0.25	8.0 (Total)
OP-227	0.08	±40	30	1.0	5.0	1.7	8.0 (Total)

PRODUCT SELECTOR - OPERATIONAL AMPLIFIERS

Product	Offset Voltage (mV)	Bias Current (nA)	Offset Current (nA)	Drift (μV/° C)	Bandwidth (MHz)	SR (V/μs)	Supply Current (mA)
DUAL							
SUPER BETA							
PM-2108	0.5	2	0.2	5	0.8	0.12	1.2 (Total)
MICRO POWER							
OP-220	0.1	20	1.5	1.0	0.15	0.05	0.17 (Total)
QUAD OP AMPS							
GENERAL PURPOSE							
OP-09	0.5	300	20.0	10	1.5	0.7	6.0 (Total)
OP-11	0.5	300	20.0	10	1.5	0.7	6.0 (Total)
PM-4136	5.0	500	200.0	30	1.5	0.5	11.4 (Total)
MICRO POWER							
OP-420	2.5	20	1.5	10	0.15	0.05	0.3 (Total)
OP-421	2.5	50	5.0	10	1.0	0.25	1.8 (Total)

OP-01

INVERTING HIGH-SPEED OPERATIONAL AMPLIFIER

FEATURES

- **Fast Settling Time** ..... **1μs to 0.1%**
- **High Slew Rate** **18V/μs**
- **Power Bandwidth** **250kHz**
- **Low Power Consumption** ..... **90mW Maximum**
- **Excellent DC Specifications**
- **Internally Compensated**
- **Ideal DAC Output Amplifier**
- **MIL-STD-883 Processing Available**
- **Fits Standard 741 Sockets**
- **Low Cost**

GENERAL DESCRIPTION

The OP-01 Series of monolithic Inverting High-Speed Operational Amplifiers combines high slew rate, fast settling time and excellent DC input characteristics. An internal feed-forward frequency compensation network provides simplicity of application — no external capacitors are required for stable, high-speed performance. The fast output response is achieved without sacrifice of input bias current or power consumption. A 250kHz power bandwidth is attained with a small signal bandwidth of 2.5MHz, allowing non-critical board layout. The OP-01 is completely protected at both input and output, fits standard 741 sockets, and is offset nulled with a 10kΩ potentiometer.

The low offset voltage, input bias current, and offset voltage drift vs. temperature provide accurate DC performance in applications such as channel preamplifiers, fast integrators and precision summing amplifiers. The fast output response and excellent settling time makes the OP-01 ideal for use in D/A converter output amplifiers.

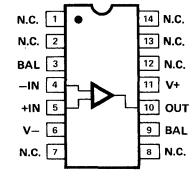
ORDERING INFORMATION †

T_A=25°C	PACKAGE				
	HERMETIC			PLASTIC	
V_{OS} Max.	TO-99	DIP		DIP	OPERATING TEMPERATURE
(mV)	8 Pin	8 Pin	14 Pin	8 Pin	RANGE
0.7	OP01J *	OP01Z *	OP01Y *		MIL.
0.7	OP01HJ	OP01HZ	OP01HY	OP01HP	COM.
2.0	OP01FJ *	OP01FZ *	OP01FY *		MIL.
2.0	OP01EJ	OP01EZ	OP01EY	OP01EP	COM.
5.0	OP01GJ *	OP01GZ *	OP01GY *		MIL.
5.0	OP01CJ	OP01CZ	OP01CY	OP01CP	COM.

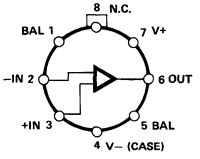
* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

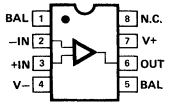
PIN CONNECTIONS



14-PIN HERMETIC DIP (Y-Suffix)*



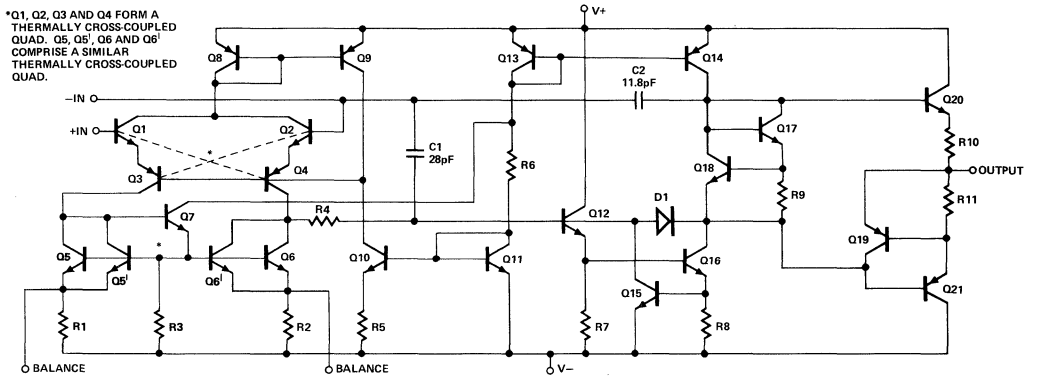
TO-99 (J-Suffix)



EPOXY B MINI-DIP (P-Suffix) & 8-PIN HERMETIC DIP (Z-Suffix)

*Not recommended for new designs.

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 2)

Total Supply Voltage, OP-01, OP-01F, OP-01E, OP-01H, OP-01N, OP-01NT, OP-01G, OP-01GT ..... ±22V
OP-01G, OP-01C, OP-01GR ..... ±20V
Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ± 30V
Input Voltage (Note 3) ..... ± 15V
Short Circuit Duration ..... Indefinite
Operating Temperature Range
OP-01, OP-01F, OP-01G ..... −55°C to +125°C
OP-01H, OP-01E, OP-01C ..... 0°C to +70°C
DICE Junction Temperature (T_j) ..... −65°C to +150°C
Storage Temperature Range
J, Y, and Z Packages ..... −65°C to + 150°C
P Package ..... −65°C to + 125°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

NOTES:
1. See table for maximum ambient temperature rating and derating factor.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
14-Pin Hermetic DIP (Y)	100°C	10.0mW/°C
8-Pin Hermetic Dip (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	35°C	5.6mW/°C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.
3. For supply voltages less than ± 15V, the maximum input voltage is the supply voltage.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

			OP-01 OP-01H			OP-01F OP-01E			OP-01G OP-01C			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.3	0.7	—	1.0	2.0	—	2.0	5.0	mV
Input Offset Current	I_{OS}		—	0.5	2.0	—	1.0	5.0	—	2.0	20	nA
Input Bias Current	I_B		—	18	30	—	20	50	—	25	100	nA
Input Voltage Range	IVR		± 12.0	±13.0	—	± 12.0	±13.0	—	± 12.0	±13.0	—	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±10V $R_S \leq 20k\Omega$	85	110	—	80	100	—	80	100	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ± 5V to ± 20V $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	μV/V
Output Voltage Swing	V_O	$R_L \geq 5k\Omega$ $R_L \geq 2k\Omega$	±12.5 ±12.0	±13.5 ±13.0	— —	±12.5 ±12.0	±13.5 ±13.0	— —	±12.5 ±12.0	±13.5 ±13.0	— —	V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ V_O = ±10V	50	100	—	50	100	—	25	75	—	V/mV
Power Consumption	P_d	V_{OUT} = 0	—	50	90	—	50	90	—	50	90	mW
Settling Time to 0.1% (Summing Node Error)	t_S	A_V = −1 (Note 1 & 2) V_{IN} = 5V	—	0.7	1.0	—	0.7	1.0	—	0.7	1.0	μs
Slew Rate (Notes 2 & 3)	SR	A_V = −1, R_S = 3K to 5KΩ	12	18	—	12	18	—	12	18	—	V/μs
Large Signal Bandwidth (Notes 3 & 4)			150	250	—	150	250	—	150	250	—	kHz
Small Signal Bandwidth (Notes 3 & 4)			1.5	2.5	—	1.5	2.5	—	1.5	2.5	—	MHz
Risetime	t_r	A_V = −1 V_{IN} = 50mV	—	150	—	—	150	—	—	150	—	ns
Overshoot	O_S		—	2	—	—	2	—	—	2	—	%

NOTES:
1. R_L = 2kΩ; C_L = 50pF. See Settling Time Test Circuit.
2. Sample tested.
3. See application information.
4. Guaranteed by design.

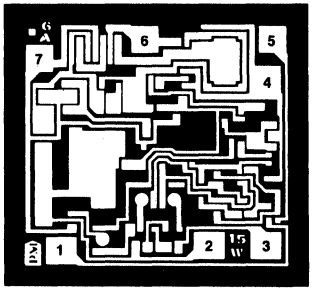
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ for OP-01, OP-01F, OP-01G and $0°C \leq T_A \leq +70°C$ for OP-01H, OP-01E, OP-01C, unless otherwise noted.

			OP-01 OP-01H			OP-01F OP-01E			OP-01G OP-01C			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.4	1.0	—	1.5	3.0	—	3.0	6.0	mV
Input Offset Current	I_{OS}		—	1.0	4.0	—	2.0	10	—	4.0	40	nA
Input Bias Current	I_B		—	30	50	—	40	100	—	50	200	nA
Input Voltage Range	IVR		±10.0	±13.0	—	±10.0	±13.0	—	±10.0	±13.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	110	—	80	100	—	80	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	30	60	—	25	60	—	15	50	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 5k\Omega$ $R_L \geq 2k\Omega$	±12.5 ±12.0	±13.5 ±13.0	— —	±12.5 ±12.0	±13.5 ±13.0	— —	±12.5 ±12.0	±13.5 ±13.0	— —	V
Offset Voltage Drift (Note 2)	TCV_{OS}	$R_S \leq 5k\Omega$	—	2.0	8.0	—	3.0	10.0	—	5.0	20.0	μV/°C

NOTE:

2. Sample tested.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



DIE SIZE 0.046 X 0.042 inch

1. NULL
2. INVERTING INPUT
3. NON-INVERTING INPUT
4. V–
5. NULL
6. OUTPUT
7. V+

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$ for OP-01N, OP-01G and OP-01GR devices, $T_A = +125°C$ for OP-01NT and OP-01GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-01NT LIMIT	OP-01N LIMIT	OP-01GT LIMIT	OP-01G LIMIT	OP-01GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	1.0	0.7	3.0	2.0	5.0	mV MAX
Input Offset Current	I_{OS}		4.0	2.0	10.0	5.0	20.0	nA MAX
Input Bias Current	I_B		50	30	100	50	100	nA MAX
Input Voltage Range	IVR		±10.0	±12.0	±10.0	±12.0	±12.0	V MIN
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	85	80	80	80	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	60	60	100	100	150	µV/V MAX
Output Voltage Swing	V_{OM}	$R_L \geq 5k\Omega$ $R_L \geq 2k\Omega$	±12.5 ±12.0	±12.5 ±12.0	±12.5 ±12.0	±12.5 ±12.0	±12.5 ±12.0	V MIN
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	30	50	25	50	25	V/mV MIN
Power Consumption	P_d	$V_{OUT} = 0$	—	90	—	90	90	mW MAX

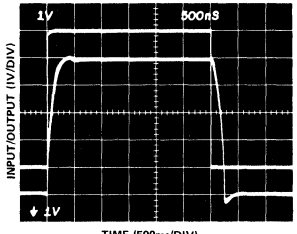
NOTE: For 25° C characteristics of NT & GT devices, see N & G characteristics respectively.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	ALL GRADES TYPICAL	UNITS
Slew Rate	SR	$A_{VCL} = -1$ $R_S = 3k\Omega$ to $5k\Omega$	18	V/µs
Settling Time to 0.1% (Summing Node Error)	t_s	$V_{IN} = 5V$ $A_V = -1$ $R_L = 2k\Omega$ (See Settling Time Test Circuit) $C_L = 50pF$	1.0	µs
Large Signal Bandwidth			250	kHz
Small Signal Bandwidth			2.5	MHz
Risetime	t_r	$V_{IN} = 50mV$ $A_V = -1$	150	ns

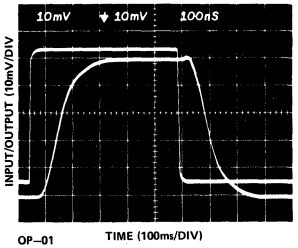
TYPICAL PERFORMANCE CURVES

LARGE-SIGNAL PULSE RESPONSE



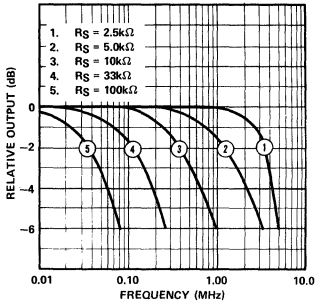
OP–01
V_S = ±15V, A_V = –1, R_L = 2kΩ, C_L = 50pF

SMALL-SIGNAL PULSE RESPONSE

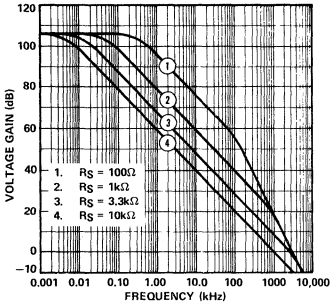


OP–01
V_S = ±15V, A_V = –1, R_L = 2kΩ, C_L = 50pF

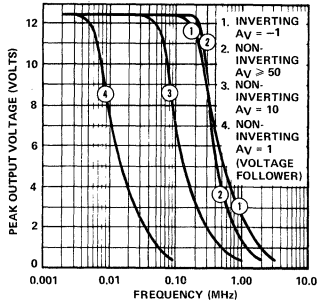
UNITY GAIN BANDWIDTH vs SOURCE RESISTANCE



OPEN LOOP GAIN vs FREQUENCY



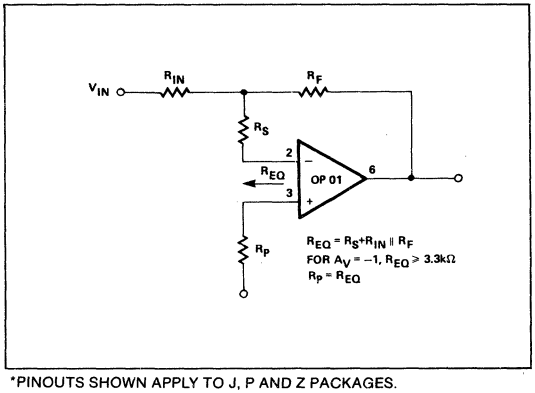
LARGE SIGNAL OUTPUT SWING vs FREQUENCY



APPLICATIONS INFORMATION

The OP-01 incorporates an internal feed-forward compensation network to provide fast slewing and settling times in all inverting and moderate-to-high gain non-inverting applications. Unity gain bandwidth is a function of the total equivalent source resistance seen by the inverting terminal, and proper choice of this resistance will allow the user to maximize bandwidth while assuring proper stability. The equivalent inverting terminal resistance is defined as $R_{IN} \| R_F$. A total equivalent input terminal resistance $\geq 3.3k\Omega$ will assure stability in all closed loop gain configurations including unity gain. Should $R_{IN} \| R_F \leq 3.3k\Omega$, a resistor ($R_S$) may be placed between the inverting input and the sum node to provide the required resistance. (See Fast Inverting Amplifier Diagram.) Lower values of total equivalent resistance may be used to improve bandwidth in higher closed loop gain configurations, as indicated by the Open Loop Gain vs. Frequency plot.

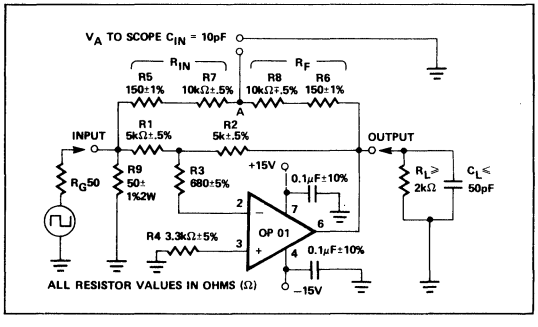
FAST INVERTING AMPLIFIER*



*PINOUTS SHOWN APPLY TO J, P AND Z PACKAGES.

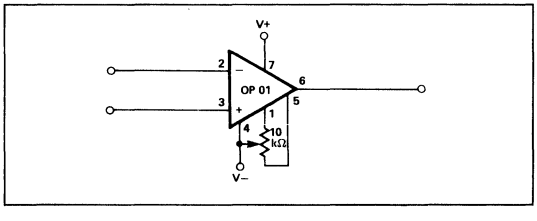
SETTLING TIME TEST CIRCUIT *

Settling time may be measured using the circuit shown; this circuit incorporates the "false sum node" technique to produce more accurate, repeatable results. For a 5 volt input step, 0.1% settling will be achieved when the false sum node settles to within ±2.5mV of its final value. The oscilloscope used for observation of the false sum node should have wide bandwidth, fast overload recovery time, and be used with a low capacity probe (≤10pF, including strays). A Tektronix 7504 scope with a 7A11 probe or equivalent is suggested. The pulse generator should have a 50Ω output impedance and be capable of a 5V rise time in ≤20ns with ringing less than 2.5mV after 0.5μs. 0.1% measurements require R_{IN} to equal R_F within 0.01%; R_5 and R_6 are used as trimming resistors to achieve this matching.

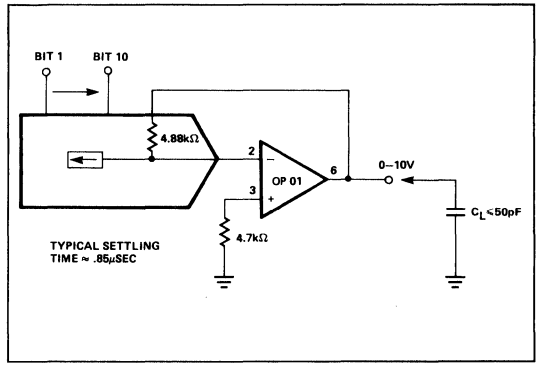


TYPICAL APPLICATIONS

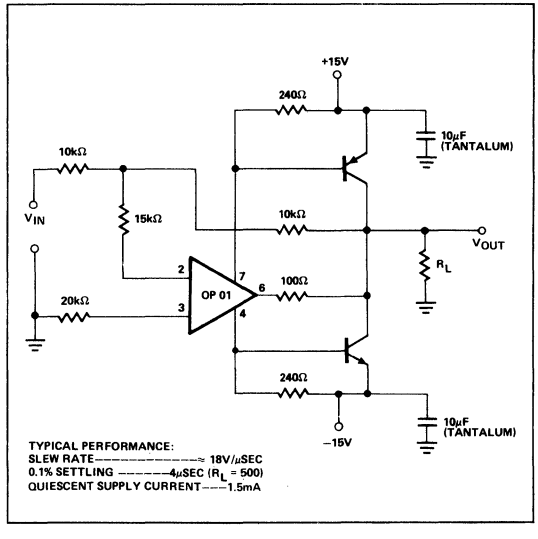
OFFSET NULLING CIRCUIT *



FAST VOLTAGE OUTPUT D/A CONVERTER *



PRECISION POWER BOOSTER CIRCUIT *



*PINOUTS SHOWN APPLY TO J, P AND Z PACKAGES

OP-02/OP-19

HIGH-PERFORMANCE GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

FEATURES

All Devices:

- **Excellent DC Input Specifications**
- **Low Noise** ..... **0.65μV_{p-p}**
- **Low Drift (TCV_{OS}) Max** ..... **8$\mu V/°C$**
- **0°C/+70°C and −55°C/+125°C Models**
- **Silicon-Nitride Passivation**
- **Guaranteed Rise Time and Overshoot**
- **125°C Tested Dice**
- **"Premium" 741 and 107 Replacement**
- **High Speed (OP-19)** ..... **1.0V/μs Slew Rate**

GENERAL DESCRIPTION

The PMI Series of High-Performance General-Purpose Operational Amplifiers provides significant improvements over industry-standard and "premium" 741 and 741HS types while maintaining pin-for-pin compatibility, ease of application, and low cost. Key specifications such as V_{OS}, I_{OS}, I_B, CMRR, PSRR and A_{VO}, are guaranteed over the full operating temperature range. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process reduces "popcorn noise." A thermally-symmetrical input stage design provides low TCV_{OS}, TCI_{OS}, and insensitivity to output load conditions.

The OP-02 is a direct replacement for the 741. It is ideal for upgrading existing designs where accuracy improvements are required and for eliminating special low-drift or low-noise selected types.

The OP-19 is a high-speed replacement for the 741. It's high slew rate increases the maximum undistorted output frequency from 5kHz to 10kHz making it ideal for telecommunications applications.

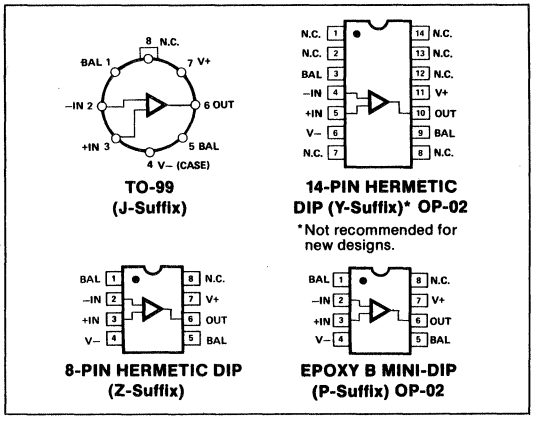
ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (mV)	PACKAGE: HERMETIC TO-99 8-PIN	HERMETIC DIP 8-PIN	HERMETIC DIP 14-PIN	PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
0.5	OP02AJ* OP19AJ*	OP02AZ* OP19AZ*	OP02AY*		MIL
0.5	OP02EJ OP19EJ	OP02EZ OP19EZ	OP02EY	OP02EP	COM
2.0	OP02J* OP19BJ*	OP02Z* OP19BZ*	OP02Y*		MIL
2.0	OP02CJ OP19FJ	OP02CZ OP19FZ	OP02CY	OP02CP	COM
5.0	OP02BJ* OP19CJ*	OP02BZ* OP19CZ*	OP02BY*		MIL
5.0	OP02DJ OP19GJ	OP02DZ OP19GZ	OP02DY	OP02DP	COM

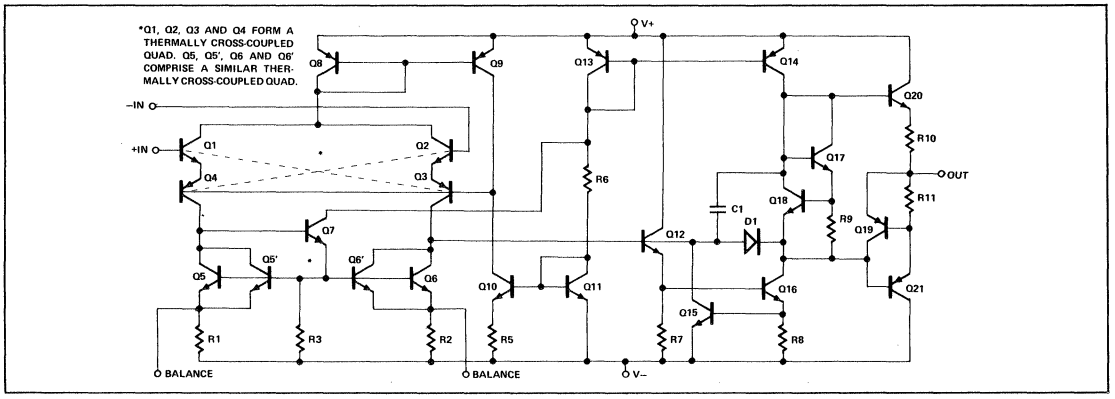
* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±22V
Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply Voltage
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range
OP-02A, OP-02, OP-02B ..... −55 to +125°C
OP-02E, OP-02C, OP-02D ..... 0°C to +70°C
OP-19A, OP-19B, OP-19C ..... −55°C to +125°C
OP-19E, OP-19F, OP-19G ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 60 sec.) ..... 300°C
DICE Junction Temperature (T_j) ..... −65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
14-Pin Hermetic DIP (Y)	100°C	10.0mW/°C
8-Pin Plastic DIP (P)	36°C	5.6mW/°C
8-Pin Hermetic Dip (Z)	75°C	6.7mW/°C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		OP-02A/OP-19A OP-02E/OP-19E MIN	TYP	MAX	OP-02/OP-19B OP-02C/OP-19F MIN	TYP	MAX	OP-02B/OP-19C OP-02D/OP-19G MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$		—	0.3	0.5	—	1.0	2.0	—	3.0	5.0	mV
Input Offset Current	I_{OS}		OP-02	—	0.5	2.0	—	1.0	5.0	—	5.0	25	nA
			OP-19	—	0.5	5.0	—	1.0	6.0	—	5.0	25	
Input Bias Current	I_B		OP-02	—	18	30	—	20	50	—	30	100	nA
			OP-19	—	18	50	—	20	60	—	30	100	
Input Resistance-Differential Mode	R_{IN}	(Note 2)		3.8	7.5	—	2.3	7.0	—	1.0	5.0	—	MΩ
Input Voltage Range	IVR			±10.0	±13.0	—	±10.0	±13.0	—	±10.0	±13.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$		85	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 20V$ $R_S \leq 20k\Omega$		—	10	60	—	30	100	—	100	150	μV/V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$		±12.0	±13.0	—	±12.0	±13.0	—	±12.0	±13.0	—	V
Large Signal Voltage Gain	A_{VO}	$R_L > 2k\Omega$ $V_O = \pm 10V$		100	250	—	50	200	—	25	150	—	V/mV
Power Consumption	P_d	$V_O = 0V$	OP-02	—	40	70	—	50	90	—	50	90	mW
			OP-19	—	50	90	—	50	90	—	50	90	
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz		—	0.65	—	—	0.65	—	—	0.65	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_o = 10Hz$		—	25	—	—	25	—	—	25	—	$nV/\sqrt{Hz}$
		$f_o = 100Hz$		—	22	—	—	22	—	—	22	—	
		$f_o = 1000Hz$		—	21	—	—	21	—	—	21	—	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz		—	12.8	—	—	12.8	—	—	12.8	—	pA_{p-p}
Input Noise Current Density	i_n	$f_o = 10Hz$		—	1.4	—	—	1.4	—	—	1.4	—	$pA/\sqrt{Hz}$
		$f_o = 100Hz$		—	0.7	—	—	0.7	—	—	0.7	—	
		$f_o = 1000Hz$		—	0.4	—	—	0.4	—	—	0.4	—	
Slew Rate	SR	(Note 1)	OP-02	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	V/μS
			OP-19	0.8	1.0	—	0.8	1.0	—	—	1.0	—	
Large Signal Bandwidth		$V_O = 20V_{p-p}$ (Note 1)	OP-02	4.0	8.0	—	4.0	8.0	—	4.0	8.0	—	kHz
			OP-19	11.0	20.0	—	11.0	20.0	—	—	20	—	
Closed Loop Bandwidth	BW	$A_{VCL} = +1.0$ (Note 1)		0.8	1.3	—	0.8	1.3	—	0.8	1.3	—	MHz
Risetime	t_r	$A_V = +1$ $V_{IN} = 50mV$ (Note 1)		—	200	300	—	200	300	—	200	300	ns
Overshoot	O_S	(Note 1)	OP-02	—	5	10	—	5	10	—	5	10	%
			OP-19	—	15	—	—	15	—	—	15	—	

NOTE:

1. Sample tested.
2. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		OP-02A/OP-19A MIN	OP-02A/OP-19A TYP	OP-02A/OP-19A MAX	OP-02/OP-19B MIN	OP-02/OP-19B TYP	OP-02/OP-19B MAX	OP-02B/OP-19C MIN	OP-02B/OP-19C TYP	OP-02B/OP-19C MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \le 20k\Omega$		—	0.5	1.0	—	1.4	3.0	—	3.0	6.0	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S = 50\Omega$		—	2.0	8.0	—	4.0	10.0	—	8.0	20	µV/°C
Input Offset Current	I_{OS}		OP-02	—	1.0	5.0	—	2.0	10.0	—	5.0	50.0	nA
			OP-19	—	1.0	10.0	—	2.0	12.0	—	5.0	50.0	
Average Input Offset Current Drift (Note 1)	TCI_{OS}			—	7.5	75	—	15	150	—	30	300	pA/°C
Input Bias Current	I_B		OP-02	—	30	60	—	40	100	—	50	200	nA
			OP-19	—	30	100	—	40	120	—	50	200	
Input Voltage Range	IVR			±10.0	±13.0	—	±10.0	±13.0	—	±10.0	±13.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \le 20k\Omega$		80	95	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 20V$ $R_S \le 20k\Omega$		—	10	60	—	30	100	—	100	150	µV/V
Large Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$ $V_O = \pm 10V$		50	100	—	25	60	—	25	60	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$		±12.0	±13.0	—	±12.0	±13.0	—	±10.0	±13.0	—	V

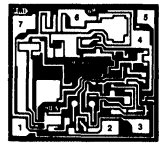
ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $0°C \le T_A \le +70°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		OP-02E/OP-19E MIN	OP-02E/OP-19E TYP	OP-02E/OP-19E MAX	OP-02C/OP-19F MIN	OP-02C/OP-19F TYP	OP-02C/OP-19F MAX	OP-02D/OP-19G MIN	OP-02D/OP-19G TYP	OP-02D/OP-19G MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \le 20k\Omega$		—	0.4	1.0	—	1.2	3.0	—	3.0	6.0	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S = 50\Omega$		—	2.0	8.0	—	4.0	10.0	—	8.0	20	µV/°C
Input Offset Current	I_{OS}		OP-02	—	0.7	4.0	—	1.4	10.0	—	5.0	50	nA
			OP-19	—	0.7	10.0	—	1.4	10.0	—	5.0	50	
Average Input Offset Current Drift (Note 1)	TCI_{OS}			—	7.5	120	—	15	250	—	70	500	pA/°C
Input Bias Current	I_B		OP-02	—	22	50	—	25	100	—	50	200	nA
			OP-19	—	22	100	—	25	100	—	50	200	
Input Voltage Range	IVR			±10.0	±13.0	—	±10.0	±13.0	—	±10.0	±13.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \le 20k\Omega$		80	100	—	80	90	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 20V$ $R_S \le 20k\Omega$		—	10	60	—	30	100	—	100	150	µV/V
Large Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$ $V_O = \pm 10V$		50	100	—	25	60	—	15	25	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$		±12.0	±13.0	—	±12.0	±13.0	—	±10.0	±13.0	—	V

NOTE:

1. Sample tested.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



DIE SIZE 0.046 × 0.042 inch

1. NULL
2. INVERTING INPUT
3. NON-INVERTING INPUT
4. V−
5. NULL
6. OUTPUT
7. V+

Refer to Section 2 for additional DICE information

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$ for N, G and GR, $T_A = +125°C$ for NT and GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-02NT LIMIT	OP-02N OP-19N LIMIT	OP-02GT LIMIT	OP-02G OP-19G LIMIT	OP-02GR OP-19GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	1.0	0.5	3.0	2.0	5.0	mV MAX
Input Offset Current	I_{OS}		5	5	6	6	25	nA MAX
Input Bias Current	I_B		50	50	60	60	200	nA MAX
Input Voltage Range	IVR		±13	±13	±13	±13	±13	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	80	85	80	80	70	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	60	60	100	100	150	μV/V MAX
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±12	±12	±12	±12	V MIN
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	25	50	25	V/mV MIN
Power Consumption	P_d	$V_O = 0V$		90		90	90	mW MAX

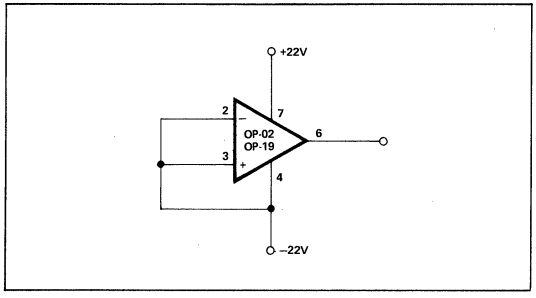
NOTE: For 25° C characteristics of NT and GT devices, see N and G characteristisc, respectively.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

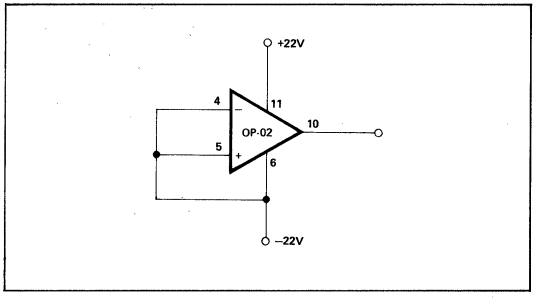
PARAMETER	SYMBOL	CONDITIONS	OP-02NT OP-02N OP-19N TYPICAL	OP-02GT OP-02G OP-19G TYPICAL	OP-02GR OP-19GR TYPICAL	UNITS
Input Resistance Differential Mode	R_{IN}		7.5	7.0	5.0	MΩ
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	0.65	0.65	0.65	μV_{p-p}
Input Noise Voltage Density	e_n	$f_o = 10Hz$ $f_o = 100Hz$ $f_o = 1000Hz$	25 22 21	25 22 21	25 22 21	$nV/\sqrt{Hz}$
Input Noise Current	I_{np-p}	0.1 Hz to 10Hz	12.8	12.8	12.8	pAp-p
Input Noise Current Density	i_n	$f_o = 10Hz$ $f_o = 100Hz$ $f_o = 1000Hz$	1.4 0.7 0.4	1.4 0.7 0.4	1.4 0.7 0.4	$pA/\sqrt{Hz}$
Slew Rate	SR		1.0	1.0	1.0	V/μs
Large Signal Bandwidth		$V_O = 20V_{p-p}$	20	20	20	kHz
Closed Loop Bandwidth	BW	$A_{VCL} = +1.0$	1.3	1.3	1.3	MHz
Risetime		$A_V = +1$ $V_{IN} = 50mV$	200	200	200	ns
Overshoot			15	15	15	%
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 500\Omega$	2.0	4.0	8	μV/°C
Average Input Offset Current Drift	TCI_{OS}		7.5	15	30	pA/°C

BURN-IN CIRCUITS

TO-99 (J) PACKAGE/8-PIN HERMETIC DIP (Z) PACKAGE

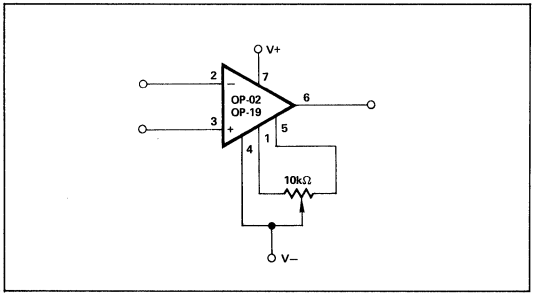


14-PIN HERMETIC DIP (Y) PACKAGE (OP-02 ONLY)

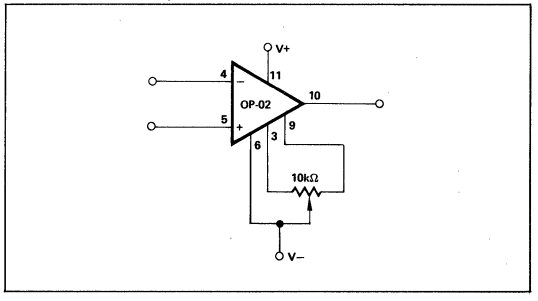


OFFSET NULLING CIRCUITS

TO-99 (J) PACKAGE/8-PIN HERMETIC DIP (Z) PACKAGE

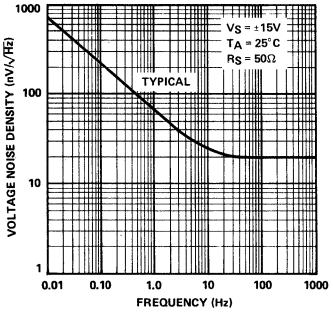


14-PIN HERMETIC DIP (Y) PACKAGE (OP-02 ONLY)

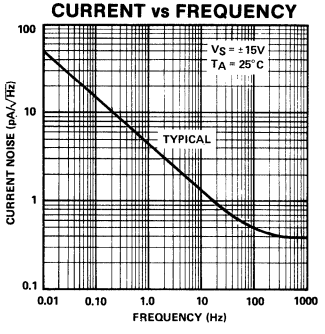


TYPICAL PERFORMANCE CURVES

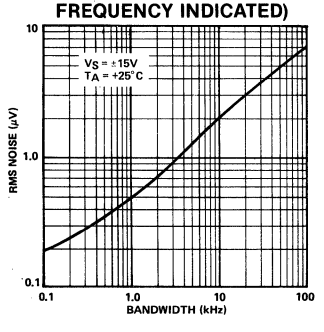
INPUT SPOT NOISE VOLTAGE vs FREQUENCY



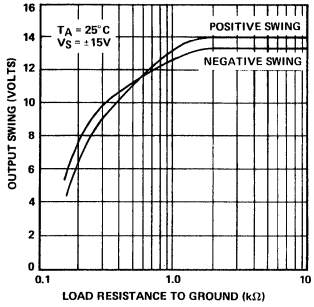
INPUT SPOT NOISE CURRENT vs FREQUENCY



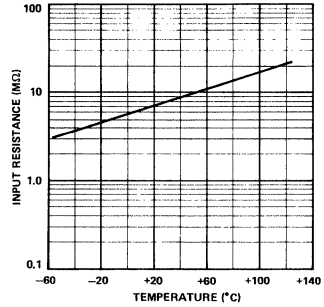
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



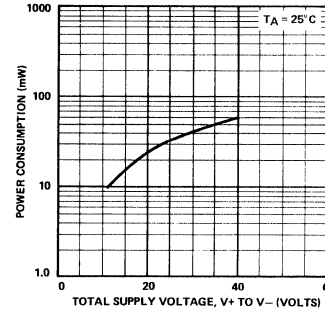
OUTPUT VOLTAGE vs LOAD RESISTANCE



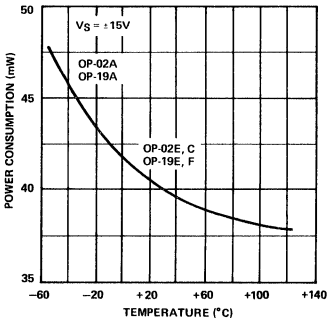
INPUT RESISTANCE vs TEMPERATURE



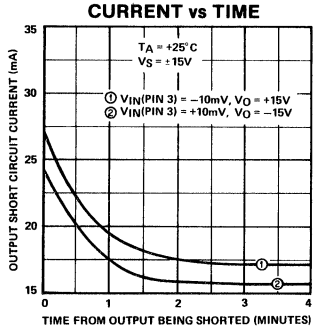
POWER CONSUMPTION vs POWER SUPPLY



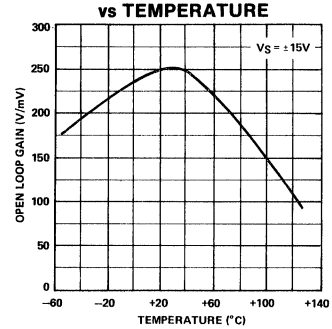
POWER CONSUMPTION vs TEMPERATURE



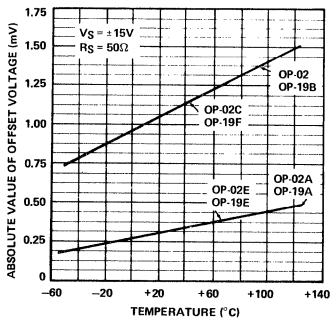
OUTPUT SHORT-CIRCUIT CURRENT vs TIME



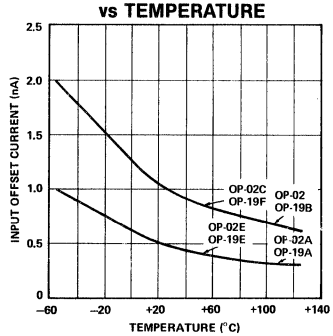
OPEN LOOP GAIN vs TEMPERATURE



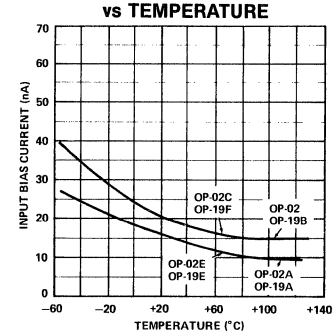
UNTRIMMED OFFSET VOLTAGE vs TEMPERATURE



INPUT OFFSET CURRENT vs TEMPERATURE

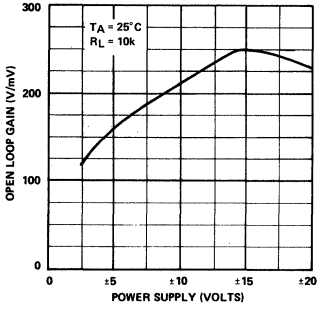


INPUT BIAS CURRENT vs TEMPERATURE

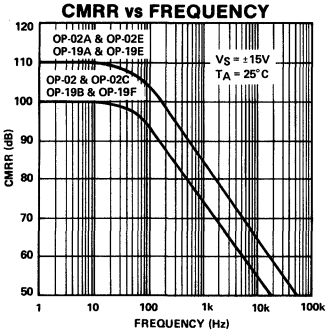


TYPICAL PERFORMANCE CURVES

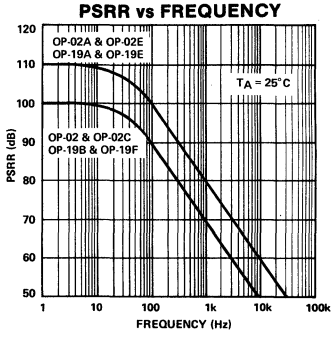
OPEN LOOP GAIN vs POWER SUPPLY VOLTAGE



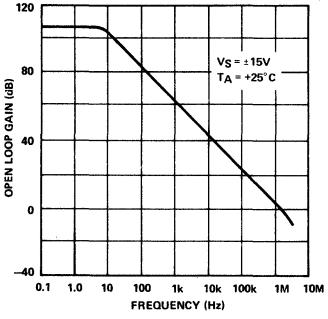
CMRR vs FREQUENCY



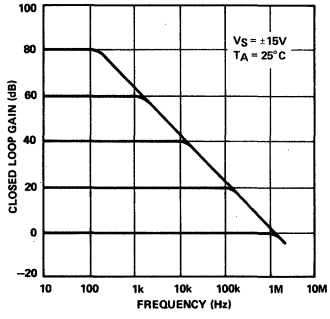
PSRR vs FREQUENCY



OPEN LOOP FREQUENCY RESPONSE

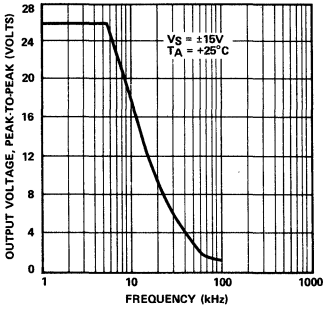


CLOSED LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



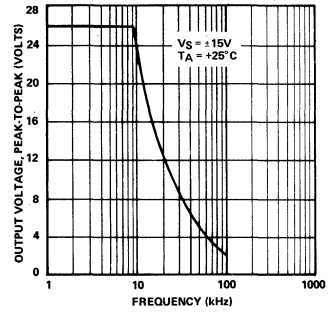
(OP-02 ONLY)

MAXIMUM UNDISTORTED OUTPUT vs FREQUENCY



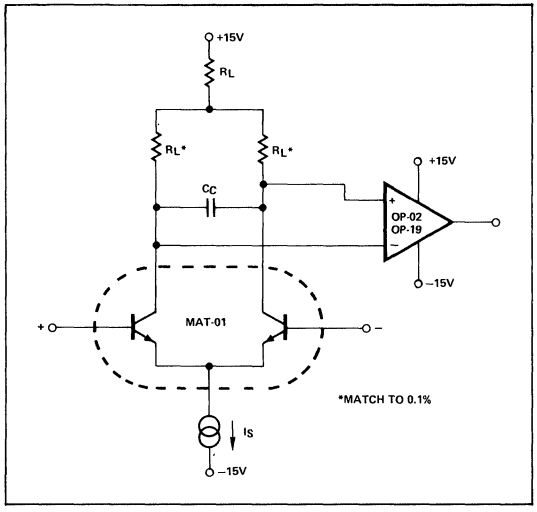
(OP-19 ONLY)

MAXIMUM UNDISTORTED OUTPUT vs FREQUENCY

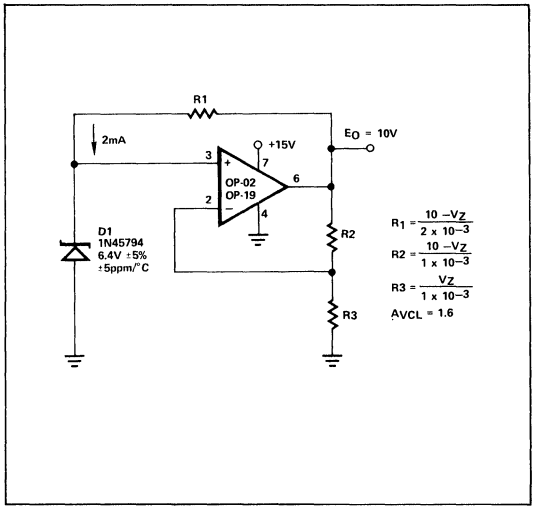


TYPICAL APPLICATIONS

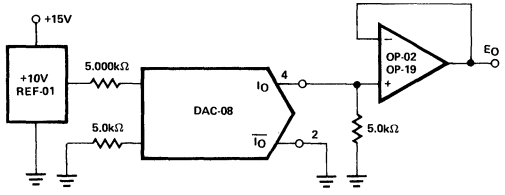
PRECISION OPERATIONAL AMPLIFIER



HIGH STABILITY VOLTAGE REFERENCE



DAC-08 OUTPUT AMPLIFIER NEGATIVE LOW IMPEDANCE OUTPUT OPERATION

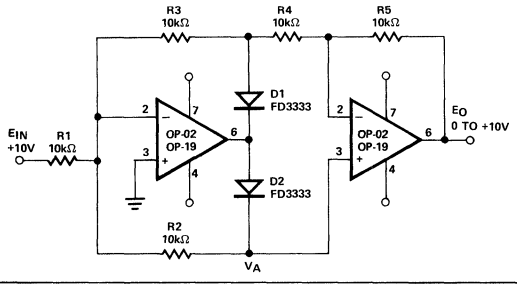


FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC) CONNECT NON-INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2), CONNECT I_O (PIN 4) TO GROUND.

INPUT/OUTPUT TABLE

	B1	B2	B3	B4	B5	B6	B7	B8	I_OmA	E_O
FULL SCALE –1LSB	1	1	1	1	1	1	1	1	1.992	–9.960
FULL SCALE –2LSB	1	1	1	1	1	1	1	0	1.984	–9.920
HALF SCALE +LSB	1	0	0	0	0	0	0	1	1.008	–5.040
HALF SCALE	1	0	0	0	0	0	0	0	1.000	–5.000
HALF SCALE –LSB	0	1	1	1	1	1	1	1	0.992	–4.960
ZERO SCALE +LSB	0	0	0	0	0	0	0	1	0.008	–0.040
ZERO SCALE	0	0	0	0	0	0	0	0	0.000	0.000

ABSOLUTE VALUE CIRCUIT



SCHEMATIC EQUATIONS
POSITIVE INPUT

1. $V_A = 0$, D2 OFF, D1 ON
2. $E_O = \left(\frac{-E_{IN}R3}{R1}\right) \cdot \left(\frac{-R5}{R4}\right) = E_{IN}\frac{R3\ R5}{R1\ R4}$
3. With R1 = R3 = R4 = R5: $E_O = E_{IN}$
4. V_{OS} error included: $E_O = E_{IN} + 2V_{OS2}$

NEGATIVE INPUT

1. D1 OFF, D2 ON
2. $\frac{-E_{IN}}{R1} = \frac{V_A}{R2} + \frac{V_A}{R3 + R4}$
3. $E_O = V_A\left(1 + \frac{R5}{R3 + R4}\right)$
4. With R3 = R4 = R5: $E_O = 1.5V_A$
5. $E_O = \frac{-(R2)\ (R3 + R4)\ (1.5)\ E_{IN}}{R1\ (R2 + R3 + R4)}$
6. With R1 = R2 = R3 = R4: $E_O = -E_{IN}$
7. V_{OS} error included: $E_O = -E_{IN} + 1.5V_{OS2} - 0.5V_{OS1}$
8. For both inputs: $E_O = +|E_{IN}|$

OP-03/OP-04/OP-14

DUAL-MATCHED HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

FEATURES

- **Excellent DC Input Specifications**
- **Matched V_{OS} and CMRR**
- **Fits Standard 747 (03/04), 1458/1558 (14) Sockets**
- **Internally Compensated**
- **Low Noise**
- **Low Drift**
- **Low Cost**
- **0°C/+70° and −55°C/+125°C Models**
- **Silicon-Nitride Passivation**
- **Models with MIL-STD-883 Class B Processing Available From Stock**

GENERAL DESCRIPTION

The OP-03/OP-04/OP-14 Series of Dual-Matched High-Performance General-Purpose Operational Amplifiers provides significant improvements over industry-standard 747 and 1458/1558 (OP-14) types while maintaining pin-for-pin compatibility, ease of application, and low cost. Key specifications, such as V_{OS}, I_{OS}, I_B, CMRR, PSRR and A_{VO}, are guaranteed over the full operating temperature range. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process reduces "popcorn noises". A thermally-symmetrical input stage design provides low TCV_{OS}, TCI_{OS} and insensitivity to output load conditions. This series is ideal for upgrading existing designs where accuracy improvements are desired and for eliminating special low-drift or low-noise selected types. For more stringent requirements, refer to the OP-207 or OP-220 Dual-Matched Instrumentation Operational Amplifier data sheets. The OP-03 provides OP-04 parameters with internally connected V+ (A) and V+ (B) positive supply pins.

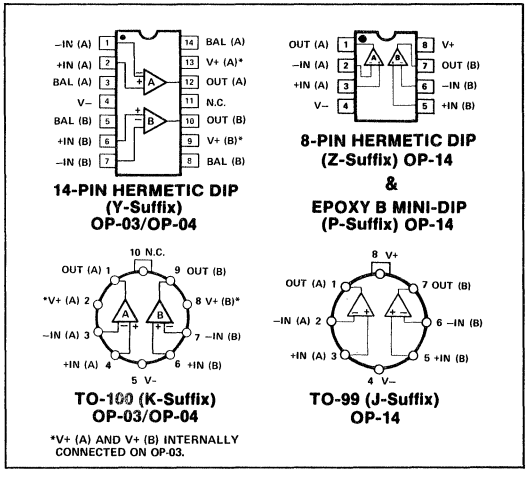
ORDERING INFORMATION†

T_A = 25°C	PACKAGE					
	HERMETIC				PLASTIC	OPERATING
V_{OS}	TO-99	TO-100	DIP		DIP	TEMP.
(mV)	8-PIN	10-PIN	8-PIN	14-PIN	8-PIN	RANGE
0.75	OP14AJ*		OP14AZ*	OP03AY* OP04AY*		MIL
0.75	OP14EJ	OP03EK OP04EK	OP14EZ	OP03EY OP04EY	OP14EP	COM
2.0	OP14J*	OP03K* OP04K*	OP14Z*	OP03Y* OP04Y*		MIL
2.0	OP14CJ	OP03CK OP04CK	OP14CZ	OP03CY OP04CY	OP14CP	COM
5.0	OP14BJ*	OP03BK* OP04BK*	OP14BZ*	OP03BY* OP04BY*		MIL
5.0	OP14DJ	OP03DK OP04DK	OP14DZ	OP03DY OP04DY	OP14DP	COM

*Also available with MIL-STD-883B processing. To order add /883 as a suffix to the part number.

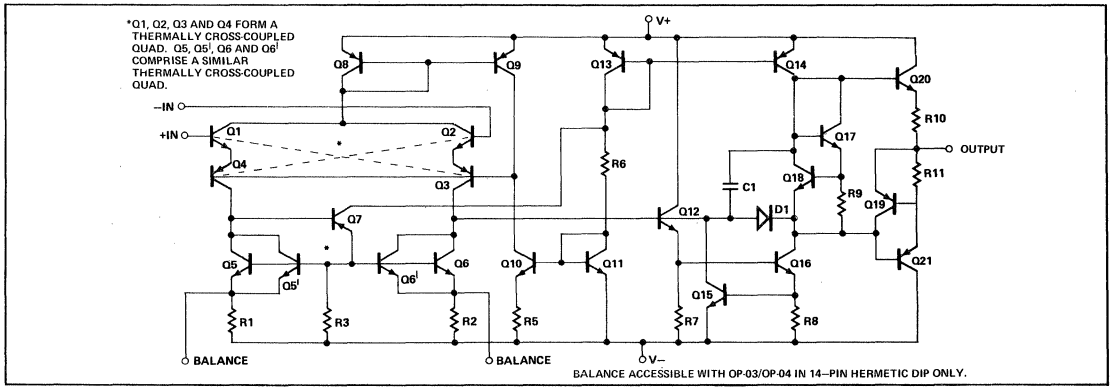
†All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



*V+ (A) AND V+ (B) INTERNALLY CONNECTED ON OP-03.

SIMPLIFIED SCHEMATIC (EACH AMPLIFIER)



ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±22V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply Voltage
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range
J, K, Y, and Z Packages ..... −65°C to +150°C
P Package ..... −65°C to +125°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Operating Temperature Range
A, Plain, B-Suffix ..... −55°C to +125°C
E, C, D-Suffix ..... 0°C to +70°C
DICE Junction Temperature (T_j) ..... −65°C to +150°C

NOTES:
1. See table for maximum ambient temperature rating and derating factor.

	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14 Pin Hermetic DIP(Y)OP-03/OP-04	100°C	10.0mW/°C
TO-100 (K) OP-03/OP-04	80°C	7.1mW/°C
TO-99 (J) OP-14	80°C	7.1mW/°C
8 Pin Hermetic DIP (Z) OP-14	75°C	6.7mW/°C
8 Pin Plastic DIP (P) OP-14	36°C	5.6mW/°C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, $R_S \leq 100\Omega$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-03A OP-03E OP-04A OP-04E OP-14A OP-14E MIN	TYP	MAX	OP-03 OP-03C OP-04 OP-04C OP-14 OP-14C MIN	TYP	MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}	$R_S \leq 20k\Omega$	—	0.3	1.0	—	1.0	2.0	mV
Common Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 10V$, $R_S \leq 100\Omega$	94	106	—	94	106	—	dB

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ for OP-03A, OP-04A, OP-14A, OP-03, OP-04 and OP-14, $0°C \leq T_A \leq 70°C$ for OP-03E, OP-04E, OP-14E, OP-03C, OP-04C and OP-14C, $R_S \leq 100\Omega$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-03A OP-03E OP-04A OP-04E OP-14A OP-14E MIN	TYP	MAX	OP-03 OP-03C OP-04 OP-04C OP-14 OP-14C MIN	TYP	MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}	$R_S \leq 20k\Omega$	—	0.5	1.5	—	1.5	3.0	mV
Common Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 10V$, $R_S \leq 100\Omega$	90	100	—	90	100	—	dB

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-03A/OP-04A OP-14A MIN	TYP	MAX	OP-03/OP-04 OP-14 MIN	TYP	MAX	OP-03B/OP-04B OP-14B MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.3	0.75	—	1.0	2.0	—	3.0	5.0	mV
Input Offset Current	I_{OS}		—	0.5	5.0	—	1.0	5.0	—	5.0	25.0	nA
Input Bias Current	I_B		—	18.0	50.0	—	20.0	75.0	—	30.0	100.0	nA
Input Resistance — Differential Mode	R_{IN}	(Note 3)	3.8	7.5	—	2.3	7.0	—	1.0	5.0	—	MΩ
Input Voltage Range	IVR		±10.0	±13.0	—	±10.0	±13.0	—	±10.0	±13.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$, $R_S \leq 20k\Omega$	85	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$, $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	μV/V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±13.0	—	±12.0	±13.0	—	±12.0	±13.0	—	V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	100	250	—	50	200	—	50	200	—	V/mV

NOTES:
1. Sample tested.
2. Power dissipation per amplifier.
3. Guaranteed by design.

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted. (Continued)

			OP-03A/OP-04A OP-14A			OP-03/OP-04 OP-14			OP-03B/OP-04B OP-14B			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Power Consumption (Note 2)	P_d	$V_O = 0V$	—	50	90	—	50	90	—	50	90	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.65	—	—	0.65	—	—	0.65	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	25.0	—	—	25.0	—	—	25.0	—	$nV/\sqrt{Hz}$
		$f_O = 100Hz$	—	22.0	—	—	22.0	—	—	22.0	—	
		$f_O = 1000Hz$	—	21.0	—	—	21.0	—	—	21.0	—	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	12.8	—	—	12.8	—	—	12.8	—	pA_{p-p}
Channel Separation	CS		100	—	—	100	—	—	80	—	—	dB
Input Noise Current Density	i_n	$f_O = 10Hz$	—	1.4	—	—	1.4	—	—	1.4	—	$pA/\sqrt{Hz}$
		$f_O = 100Hz$	—	0.7	—	—	0.7	—	—	0.7	—	
		$f_O = 1000Hz$	—	0.4	—	—	0.4	—	—	0.4	—	
Slew Rate (Note 1)	SR	$R_L = 2k\Omega$, $C_L = 100pF$	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	$V/\mu s$
Large Signal Bandwidth (Note 1)		$V_O = 20V_{p-p}$	4.0	8.0	—	4.0	8.0	—	4.0	8.0	—	kHz
Closed Loop Bandwidth (Note 1)	BW	$A_{VCL} = +1.0$	0.8	1.3	—	0.8	1.3	—	0.8	1.3	—	MHz
Risetime (Note 1)	t_r	$A_V = +1$ $V_{IN} = 50mV$ $R_L = 2k\Omega$, $C_L = 50pF$	—	200	300	—	200	300	—	200	300	ns
Overshoot (Note 1)	OS	$A_V = +1$, $V_{IN} = 50mV$ $R_L = 2k\Omega$, $C_L = 50pF$	—	5.0	10.0	—	5.0	10.0	—	5.0	10.0	%

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

			OP-03A/OP-04A OP-14A			OP-03/OP-04 OP-14			OP-03B/OP-04B OP-14B			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.4	1.5	—	1.2	3.0	—	3.0	6.0	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S = 50\Omega$	—	2.0	8.0	—	4.0	10.0	—	8.0	20.0	$\mu V/°C$
Input Offset Current	I_{OS}		—	1.0	10.0	—	2.0	10.0	—	10.0	50.0	nA
Average Input Offset Current Drift (Note 1)	TCI_{OS}		—	7.5	120.0	—	15.0	250.0	—	70.0	500.0	$pA/°C$
Input Bias Current	I_B		—	30.0	60.0	—	40.0	100.0	—	50.0	200.0	nA
Input Voltage Range	IVR		±10.0	±13.0	—	±10.0	±13.0	—	±10.0	±13.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	80	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	$\mu V/V$
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50.0	100.0	-	25.0	60.0	—	25.0	60.0	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±13.0	—	±12.0	±13.0	—	±10.0	±13.0	—	V

NOTES:
1. Sample tested.
2. Power dissipation per amplifier.

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-03E/OP-04E OP-14E			OP-03C/OP-04C OP-14C			OP-03D/OP-04D OP-14D			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.3	0.75	—	1.0	2.0	—	3.0	5.0	mV
Input Offset Current	I_{OS}		—	0.5	5.0	—	1.0	5.0	—	5.0	25.0	nA
Input Bias Current	I_B		—	18.0	50.0	—	20.0	75.0	—	30.0	100.0	nA
Input Resistance — Differential Mode	R_{IN}	(Note 3)	3.8	7.5	—	2.3	7.0	—	1.0	5.0	—	MΩ
Input Voltage Range	IVR		±10.0	±13.0	—	±10.0	±13.0	—	±10.0	±13.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	μV/V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±13.0	—	±12.0	±13.0	—	±12.0	±13.0	—	V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	100	250	—	50	200	—	25	150	—	V/mV
Power Consumption (Note 2)	P_d	$V_O = 0V$	—	50	90	—	50	90	—	50	90	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.65	—	—	0.65	—	—	0.65	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	25.0	—	—	25.0	—	—	25.0	—	$nV/\sqrt{Hz}$
		$f_O = 100Hz$	—	22.0	—	—	22.0	—	—	22.0	—	
		$f_O = 1000Hz$	—	21.0	—	—	21.0	—	—	21.0	—	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	12.8	—	—	12.8	—	—	12.8	—	pA_{p-p}
Channel Separation	CS		100	—	—	100	—	—	80	—	—	dB
Input Noise Current Density	i_n	$f_O = 10Hz$	—	1.4	—	—	1.4	—	—	1.4	—	$pA/\sqrt{Hz}$
		$f_O = 100Hz$	—	0.7	—	—	0.7	—	—	0.7	—	
		$f_O = 1000Hz$	—	0.4	—	—	0.4	—	—	0.4	—	
Slew Rate (Note 1)	SR	$R_L = 2k\Omega$, $C_L = 100pF$	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	V/μs
Large Signal Bandwidth (Note 1)		$V_O = 20V_{p-p}$	4.0	8.0	—	4.0	8.0	—	4.0	8.0	—	kHz
Closed Loop Bandwidth (Note 1)	BW	$A_{VCL} = +1.0$	0.8	1.3	—	0.8	1.3	—	0.8	1.3	—	MHz
Risetime (Note 1)	t_r	$A_V = +1$ $V_{IN} = 50mV$ $R_L = 2k\Omega$, $C_L = 50pF$	—	200	300	—	200	300	—	200	300	ns
Overshoot (Note 1)	OS	$A_V = +1$, $V_{IN} = 50mV$ $R_L = 2k\Omega$, $C_L = 50pF$	—	5.0	10.0	—	5.0	10.0	—	5.0	10.0	%

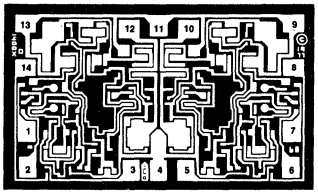
ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $0°C \leq T_A \leq +70°C$, unless otherwise noted.

			OP-03E/OP-04E OP-14E			OP-03C/OP-04C OP-14C			OP-03D/OP-04D OP-14D			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.4	1.5	—	1.2	3.0	—	3.0	6.0	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S = 50\Omega$	—	2.0	8.0	—	4.0	10.0	—	8.0	20.0	μV/°C
Input Offset Current	I_{OS}		—	1.0	10.0	—	2.0	10.0	—	10.0	50.0	nA
Average Input Offset Current Drift (Note 1)	TCI_{OS}		—	7.5	120.0	—	15.0	250.0	—	70.0	500.0	pA/°C
Input Bias Current	I_B		—	30.0	60.0	—	40.0	100.0	—	50.0	200.0	nA
Input Voltage Range	IVR		±10.0	±13.0	—	±10.0	±13.0	—	±10.0	±13.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	80	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50.0	100.0	—	25.0	60.0	—	15.0	25.0	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±13.0	—	±12.0	±13.0	—	±10.0	±13.0	—	V

NOTES:
1. Sample tested.
2. Power dissipation per amplifier.
3. Guaranteed by design.

DICE CHARACTERISTICS

OP-03 and OP-14

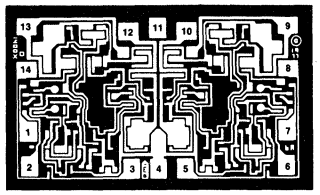


1. INVERTING INPUT (A)
2. NON-INVERTING INPUT (A)
3. BALANCE (A)
4. V−
5. BALANCE (B)
6. NON-INVERTING INPUT (B)
7. INVERTING INPUT (B)
8. BALANCE (B)
9. V+
10. OUTPUT (B)
11. V+
12. OUTPUT (A)
13. V+
14. BALANCE (A)

NOTE: 9, 11 and 13 Internally connected.

DIE SIZE
0.076 × 0.046 inch

OP-04



1. INVERTING INPUT (A)
2. NON-INVERTING INPUT (A)
3. BALANCE (A)
4. V−
5. BALANCE (B)
6. NON-INVERTING INPUT (B)
7. INVERTING INPUT (B)
8. BALANCE (B)
9. V+ (B)
10. OUTPUT (B)
11. NO CONNECTION
12. OUTPUT (A)
13. V+ (A)
14. BALANCE (A)

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

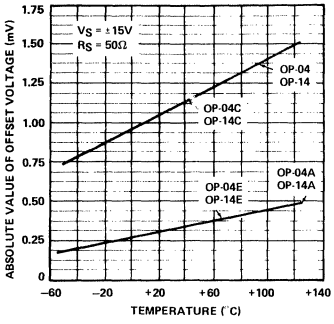
PARAMETER	SYMBOL	CONDITIONS	OP-03N/OP-04N OP-14N LIMIT	OP-03G/OP-04G OP-14G LIMIT	OP-03GR/OP-04GR OP-14GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	0.75	2.0	6.0	mV MAX
Input Offset Voltage Match	ΔV_{OS}	$R_S \leq 20k\Omega$	1.0	2.0	—	mV MAX
Input Offset Current	I_{OS}		5.0	5.0	200	nA MAX
Input Bias Current	I_B		50	75	500	nA MAX
Input Voltage Range	IVR		±10.0	±10.0	±10.0	V MIN
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	80	70	dB MIN
Common Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 10V$ $R_S \leq 100\Omega$	94	94	—	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	60	100	150	μV/V MAX
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12.0 ±12.0	±12.0 ±12.0	±12.0 ±10.0	V MIN
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	100	50	25	V/mV MIN
Power Consumption (Both Amplifiers)	P_d	$V_{OUT} = 0$	170	170	180	mW MAX
Slew Rate	SR	$R_L = 2k\Omega$ $C_L = 100pF$	0.25	0.25	—	V/μs MIN
Channel Separation	CS		100	100	—	dB MIN

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

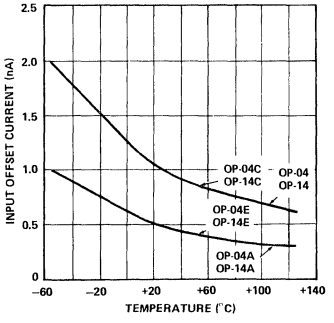
PARAMETER	SYMBOL	CONDITIONS	OP-03N/OP-04N OP-14N TYPICAL	OP-03G/OP-04G OP-14G TYPICAL	OP-03GR/OP-04GR OP-14GR TYPICAL	UNITS
Risetime		$A_V = +1$ $V_{IN} = 50mV$ $R_L = 2k\Omega$ $C_L = 50pF$	200	200	200	ns
Overshoot		$A_V = +1$ $V_{IN} = 50mV$ $R_L = 2k\Omega$ $C_L = 50pF$	5.0	5.0	5.0	%

TYPICAL PERFORMANCE CURVES (Each Amplifier)

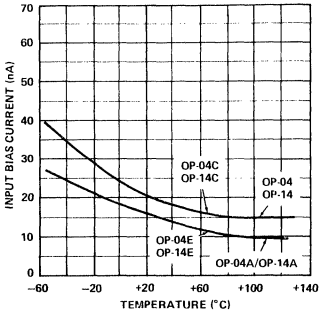
UNTRIMMED OFFSET VOLTAGE vs TEMPERATURE



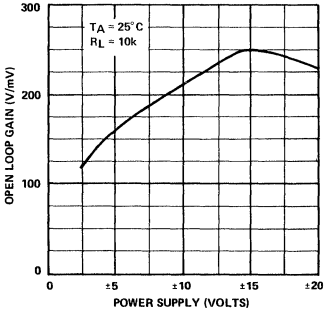
INPUT OFFSET CURRENT vs TEMPERATURE



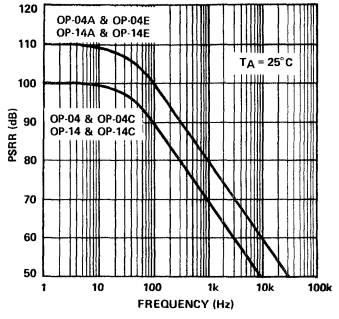
INPUT BIAS CURRENT vs TEMPERATURE



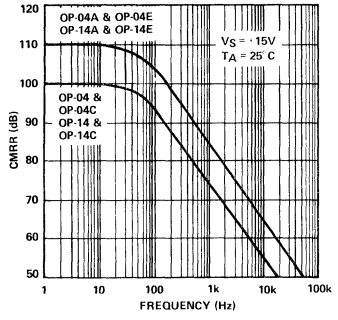
OPEN LOOP GAIN vs POWER SUPPLY VOLTAGE



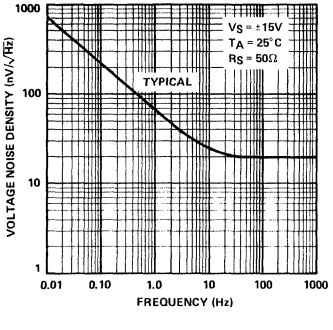
PSRR vs FREQUENCY



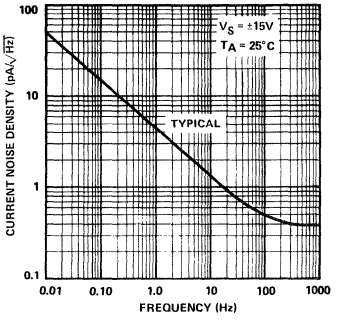
CMRR vs FREQUENCY



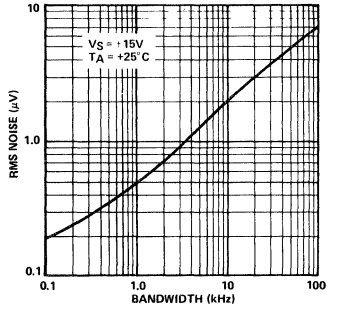
INPUT SPOT NOISE VOLTAGE vs FREQUENCY



INPUT SPOT NOISE CURRENT vs FREQUENCY

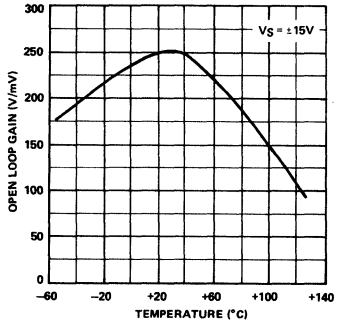


INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)

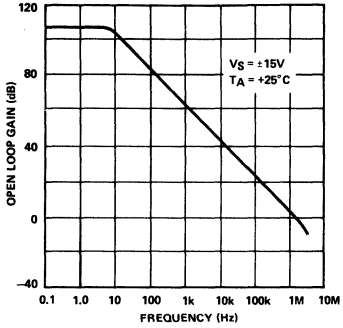


TYPICAL PERFORMANCE CURVES (Each Amplifier)

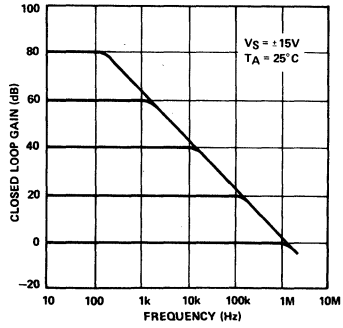
OPEN LOOP GAIN vs TEMPERATURE



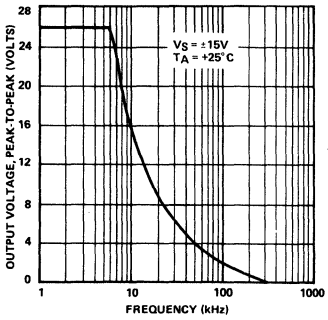
OPEN LOOP FREQUENCY RESPONSE



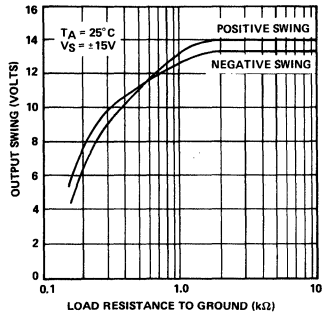
CLOSED LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



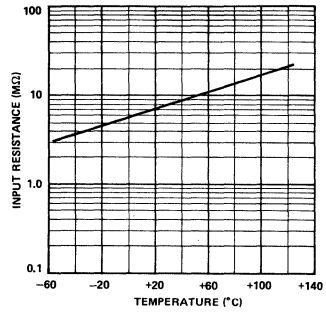
MAXIMUM UNDISTORTED OUTPUT vs FREQUENCY



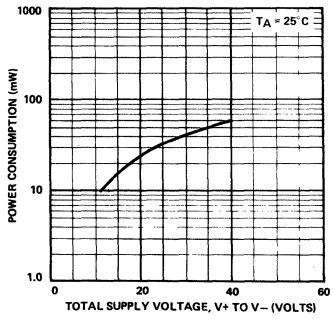
OUTPUT VOLTAGE vs LOAD RESISTANCE



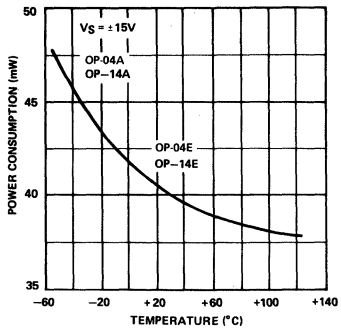
INPUT RESISTANCE vs TEMPERATURE



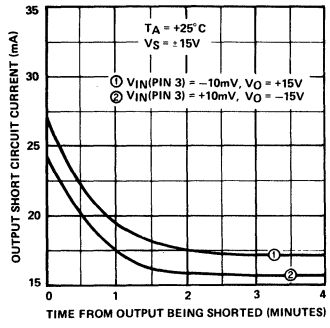
POWER CONSUMPTION vs POWER SUPPLY



POWER CONSUMPTION vs TEMPERATURE

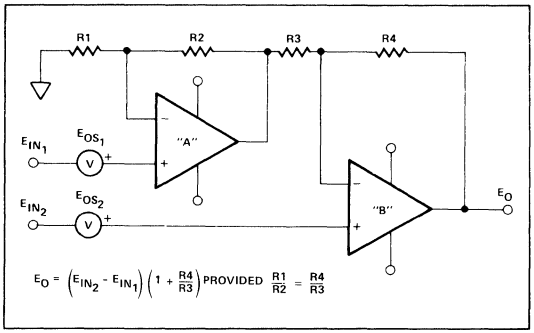


OUTPUT SHORT-CIRCUIT CURRENT vs TIME



TYPICAL APPLICATIONS

INSTRUMENTATION AMPLIFIER 2 OP-AMP DESIGN



GENERAL DESIGN CONSIDERATIONS

Assuming ideal amplifiers, the expression for output voltage is:

$$E_O = E_{in_1}\left[1+\frac{R_2}{R_1}\right]\left[-\frac{R_4}{R_3}\right] + E_{in_2}\left[1+\frac{R_4}{R_3}\right]$$

With ideal resistors this simplifies to:

$$E_O = \left[E_{in_2} - E_{in_1}\right]\left[1+\frac{R_4}{R_3}\right] \text{ provided} \frac{R_1}{R_2} = \frac{R_4}{R_3}$$

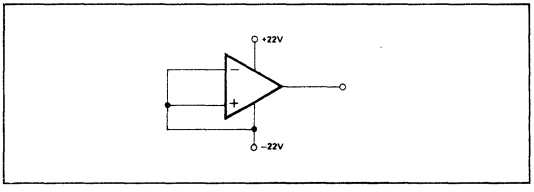
COMMON MODE REJECTION

Because the dual op amp has a high common mode rejection ratio match, the ability to reject common mode inputs becomes primarily a function of resistor ratio matching. This device eliminates the need for special op amp selections in many instrumentation amplifier applications.

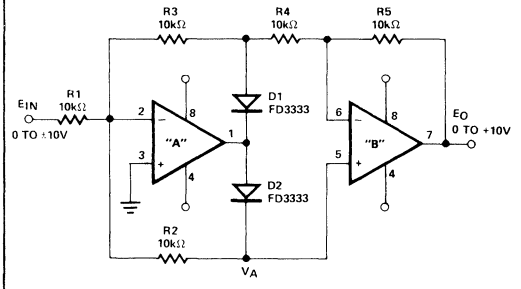
DIFFERENTIAL OFFSET VOLTAGE

The amplifier's differential input offset voltage ($E_{OS1} - E_{OS2}$) will be the major error factor. If the individual input offset voltages are of equal magnitude and polarity they appear as a common mode input and are rejected.

BURN-IN CIRCUIT (1/2 of OP-03, OP-04, OP-14)



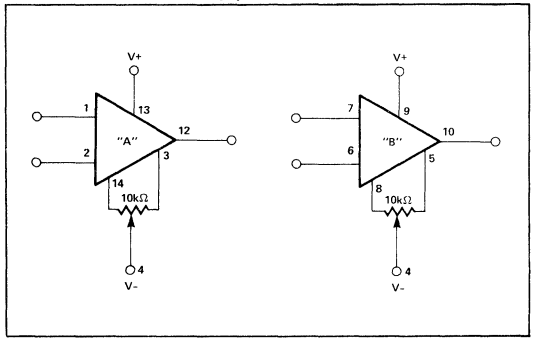
ABSOLUTE VALUE CIRCUIT *



Positive Input	Negative Input
1) V_A = 0, D2 off, D1 on	1) D1 off, D2 on
2) $E_O = E_{IN}\left(-\frac{R3}{R1}\right)\left(-\frac{R5}{R4}\right)$ $= E_{in}\frac{R3\,R5}{R1\,R4}$	2) $\frac{-E_{in}}{R1} = \frac{V_A}{R2} + \frac{V_A}{R3+R4}$
	3) $E_o = V_A\left(1+\frac{R5}{R3+R4}\right)$
3) With R1 = R3 = R4 = R5: $E_o = E_{in}$	4) With R3 = R4 = R5: $E_o = 1.5V_A$
4) V_{os} error included: $E_O = E_{IN} + 2V_{OS_B}$	5) $E_o = -\frac{(R2)\,(R3+R4)\,(1.5)\,E_{in}}{R1\,(R2+R3+R4)}$
	6) With R1 = R2 = R3 = R4: $E_o = -E_{in}$
	7) V_{OS} error included: $E_O = -E_{IN} + 1.5\,V_{OS_B} - 0.5\,V_{OS_A}$
*PIN-OUTS SHOWN FOR J, P, AND Z PACKAGES ONLY.	8) For Both Inputs: $E_o = +\lvert E_{in}\rvert$

OFFSET NULLING CIRCUITS (OP-03/OP-04)

14-PIN HERMETIC DIP (Y) PACKAGE ONLY



OP-05

INSTRUMENTATION OPERATIONAL AMPLIFIER

FEATURES

- **Low Noise** ..... **0.6μV_{p-p} Maximum, 0.1 to 10Hz**
- **Low Drift vs. Temperature** ..... **0.5μV/°C Maximum**
- **Low Drift vs. Time** ..... **0.2μV/Month Typical**
- **Low Bias Current** ..... **2.0nA Maximum**
- **High CMRR** ..... **114dB Minimum**
- **High PSRR** ..... **100dB Minimum**
- **High Gain** ..... **300,000 Minimum**
- **High R_{IN} Differential** ..... **30MΩ Minimum**
- **High R_{IN} CM** ..... **200GΩ Typical**
- **Internally Compensated** ..... **Stable to 500pF Load**
- **Easy to Use** ..... **Fully Protected**
- **Fits 725, 108A and 741 Sockets**
- **125° C Temperature Tested Dice**

GENERAL DESCRIPTION

The OP-05 Series of monolithic Instrumentation Operational Amplifiers combines superlative performance in low signal level applications with the flexibility and ease of application of a fully protected, internally compensated op amp. The OP-05 has low input offset voltage and bias current combined with very high levels of gain, input impedance, CMRR, and PSRR.

The OP-05 is a direct replacement in 725, 108A and unnulled 741 sockets allowing instant system performance improvement without redesign. The OP-05 is an excellent choice for a wide variety of applications including strain gauge and thermocouple bridges, high-gain active filters, buffers, integrators, and sample-and-hold amplifiers. For dual-matched versions refer to the OP-207 and OP-10 data sheets.

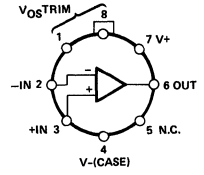
ORDERING INFORMATION†

	PACKAGE				
	HERMETIC				
T_A = 25° C V_{OS} MAX (mV)	TO-99 8-PIN	DIP 8-PIN	DIP 14-PIN	PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
0.15	OP05AJ*	OP05AZ*	OP05AY*		MIL
0.5	OP05J*	OP05Z*	OP05Y*		MIL
0.5	OP05EJ	OP05EZ	OP05EY	OP05EP	COM
1.3	OP05CJ	OP05CZ	OP05CY	OP05CP	COM

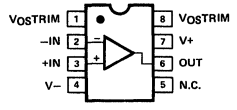
* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

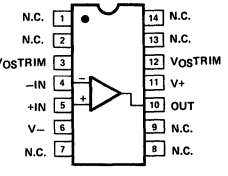
PIN CONNECTIONS



TO-99
(J-Suffix)



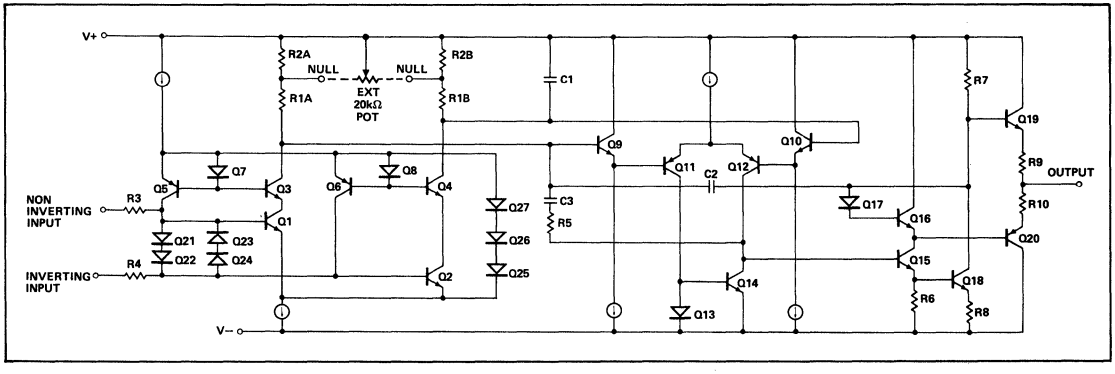
EPOXY B MINI-DIP
(P-Suffix)
&
8-PIN HERMETIC DIP
(Z-Suffix)



14-PIN HERMETIC DIP
(Y-Suffix)*

*Not recommended for new designs.

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 3)

Supply Voltage ..... ±22V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
J, Y, and Z Packages ..... −65°C to + 150°C
P Package ..... −65°C to + 125°C
Operating Temperature Range
OP-05A, OP-05 ..... −55°C to +125°C
OP-05E, OP-05C ..... 0°C to +70°C
Lead Temperature Range (Soldering, 60 sec.) ..... 300°C
DICE Junction Temperature ..... −65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
14-Pin Hermetic DIP (Y)	100°C	10.0mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	36°C	5.6mW/°C

2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
3. Absolute maximum ratings apply to both packaged parts and DICE unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05A MIN	OP-05A TYP	OP-05A MAX	OP-05 MIN	OP-05 TYP	OP-05 MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.07	0.15	—	0.2	0.5	mV
Long Term Input Offset Voltage Stability	ΔV_{OS}/Time	(Notes 1 & 2)	—	0.2	1.0	—	0.2	1.0	μV/Mo
Input Offset Current	I_{OS}		—	0.7	2.0	—	1.0	2.8	nA
Input Bias Current	I_B		—	±0.7	±2.0	—	±1.0	±3.0	nA
Input Noise Voltage (Note 2)	e_{np-p}	0.1Hz to 10Hz	—	0.35	0.6	—	0.35	0.6	μV_{p-p}
Input Noise Voltage Density (Note 2)	e_n	$f_o = 10Hz$ $f_o = 100Hz$ $f_o = 1000Hz$	— — —	10.3 10.0 9.6	18.0 13.0 11.0	— — —	10.3 10.0 9.6	18.0 13.0 11.0	$nV/\sqrt{Hz}$
Input Noise Current (Note 2)	i_{np-p}	0.1Hz to 10Hz	—	14	30	—	14	30	pA_{p-p}
Input Noise Current Density (Note 2)	i_n	$f_o = 10Hz$ $f_o = 100Hz$ $f_o = 1000Hz$	— — —	0.32 0.14 0.12	0.80 0.23 0.17	— — —	0.32 0.14 0.12	0.80 0.23 0.17	$pA/\sqrt{Hz}$
Input Resistance — Differential Mode	R_{IN}	(Note 3)	30	80	—	20	60	—	MΩ
Input Resistance — Common Mode	R_{INCM}		—	200	—	—	200	—	GΩ
Input Voltge Range	IVR		±13.5	±14.0	—	±13.5	±14.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$	114	126	—	114	126	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	4	10	—	4	10	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $R_L \geq 500\Omega$, $V_O = \pm .5V$ $V_S = \pm 3V$ (Note 2)	300 150	500 500	— —	200 150	500 500	— —	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0	— — —	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0	— — —	V
Slewing Rate (Note 2)	SR	$R_L \geq 2k\Omega$	0.1	0.3	—	0.1	0.3	—	V/μs
Closed Loop Bandwidth (Note 2)	BW	$A_{VCL} = +1.0$	0.4	0.6	—	0.4	0.6	—	MHz
Open Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	No load $V_S = \pm 3V$, No load	— —	90 4	120 6	— —	90 4	120 6	mW
Offset Adjustment Range		$R_p = 20k\Omega$	—	4	—	—	4	—	mV

NOTES:

1. Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV. Refer to typical performance curve.
2. Sample tested.
3. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05A MIN	OP-05A TYP	OP-05A MAX	OP-05 MIN	OP-05 TYP	OP-05 MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.10	0.24	—	0.3	0.7	mV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}		—	0.3	0.9	—	0.7	2.0	µV/°C
With External Trim	TCV_{OSn}	$R_p = 20k\Omega$ (Note 3)	—	0.2	0.5	—	0.3	1.0	
Input Offset Current	I_{OS}		—	1.0	4.0	—	1.8	5.6	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	5	25	—	8	50	pA/°C
Input Bias Current	I_B		—	±1.0	±4.0	—	±2.0	±6.0	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	8	25	—	13	50	pA/°C
Input Voltage Range	IVR		±13.0	±13.5	—	±13.0	±13.5	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.0V$	110	123	—	110	123	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	5	20	µV/V
Large Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	200	400	—	150	400	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12.0	±12.6	—	±12.0	±12.6	—	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05E MIN	OP-05E TYP	OP-05E MAX	OP-05C MIN	OP-05C TYP	OP-05C MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.2	0.5	—	0.3	1.3	mV
Long Term Input Offset Voltage Stability	$\Delta V_{OS}/Time$	(Notes 1 & 2)	—	0.3	1.5	—	0.4	2.0	µV/Mo
Input Offset Current	I_{OS}		—	1.2	3.8	—	1.8	6.0	nA
Input Bias Current	I_B		—	±1.2	±4.0	—	±1.8	±7.0	nA
Input Noise Voltage (Note 2)	e_{np-p}	0.1Hz to 10Hz	—	0.35	0.6	—	0.38	0.65	μV_{p-p}
Input Noise Voltage Density (Note 2)	e_n	$f_o = 10Hz$	—	10.3	18.0	—	10.5	20.0	$nV/\sqrt{Hz}$
		$f_o = 100Hz$	—	10.0	13.0	—	10.2	13.5	
		$f_o = 1000Hz$	—	9.6	11.0	—	9.8	11.5	
Input Noise Current (Note 2)	i_{np-p}	0.1Hz to 10Hz	—	14	30	—	15	35	pA_{p-p}
Input Noise Current Density (Note 2)	i_n	$f_o = 10Hz$	—	0.32	0.80	—	0.35	0.90	$pA/\sqrt{Hz}$
		$f_o = 100Hz$	—	0.14	0.23	—	0.15	0.27	
		$f_o = 1000Hz$	—	0.12	0.17	—	0.13	0.18	
Input Resistance — Differential Mode	R_{IN}	(Note 3)	15	50	—	8	33	—	MΩ
Input Resistance — Common Mode	R_{INCM}		—	160	—	—	120	—	GΩ
Input Voltge Range	IVR		±13.5	±14.0	—	±13.0	±14.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$	110	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	7	32	µV/V
Large Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	200	500	—	120	400	—	V/mV
		$R_L \ge 500\Omega$, $V_O = \pm 0.5V$	150	500	—	100	400	—	
		$V_S = \pm 3V$ (Note 2)							
Output Voltage Swing	V_O	$R_L \ge 10k\Omega$	±12.5	±13.0	—	±12.0	±13.0	—	V
		$R_L \ge 2k\Omega$	±12.0	±12.8	—	±11.5	±12.8	—	
		$R_L \ge 1k\Omega$	±10.5	±12.0	—	—	± 12.0	—	
Slewing Rate (Note 2)	SR	$R_L = \ge 2k\Omega$	0.1	0.3	—	0.1	0.3	—	V/µs
Closed Loop Bandwidth (Note 2)	BW	$A_{VCL} = +1.0$	0.4	0.6	—	0.4	0.6	—	MHz
Open Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	No load	—	90	120	—	95	150	mW
		$V_S = \pm 3V$, No load	—	4	6	—	4	8	
Offset Adjustment Range		$R_p = 20k\Omega$	—	4	—	—	4	—	mV

NOTE: See notes on previous page.

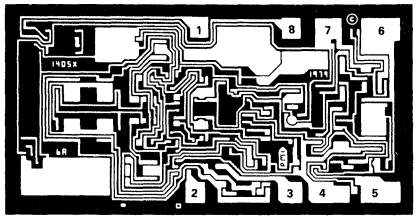
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \leq T_A \leq +70°C$, unless otherwise noted.

			OP-05E			OP-05C			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}		—	0.25	0.6	—	0.35	1.6	mV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 2)	—	0.7	2.0	—	1.3	4.5	μV/°C
With External Trim	TCV_{OSn}	$R_p = 20k\Omega$ (Note 3)	—	0.2	0.6	—	0.4	1.5	
Input Offset Current	I_{OS}		—	1.4	5.3	—	2.0	8.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	8	35	—	12	50	pA/°C
Input Bias Current	I_B		—	±1.5	±5.5	—	±2.2	±9.0	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	13	35	—	18	50	pA/°C
Input Voltage Range	IVR		±13.0	±13.5	—	±13.0	±13.5	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.0V$	107	123	—	97	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	180	450	—	100	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±12.6	—	±11.0	±12.6	—	V

NOTES:

1. Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV. Refer to typical performance curve.
2. Sample tested.
3. Guaranteed by design.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



DIE SIZE 0.100 × 0.051 inch

1. BALANCE
2. INVERTING INPUT
3. NON-INVERTING INPUT
4. V–
5. NO CONNECTION
6. OUTPUT
7. V+
8. BALANCE

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$ for OP-05N, OP-05G and OP-05GR devices, $T_A = +125°C$ for OP-05NT and OP-05GT, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05NT LIMIT	OP-05N LIMIT	OP-05GT LIMIT	OP-05G LIMIT	OP-05GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		0.25	0.15	0.7	0.5	1.3	mV MAX
Input Offset Current	I_{OS}		4.0	2.0	5.7	3.8	6.0	nA MAX
Input Bias Current	I_B		±4.0	±2.0	±6.0	±4.0	±7.0	nA MAX
Input Resistance Differential Mode	R_{IN}	(Note 2)	—	20	—	15	8	MΩ MIN
Input Voltage Range	IVR		±13.0	±13.5	±13.0	±13.5	±13.0	V MIN
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$ at + 25°C $V_{CM} = \pm 13.0V$ at + 125°C	110	114	110	110	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	20	10	20	20	30	µV/V MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$ $R_L = 1k\Omega$	— ±12.0 —	±12.5 ±12.0 ±10.5	— ±12.0 —	±12.5 ±12.0 ±10.5	±12.0 ±11.5 —	V MIN
Large Signal Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	200	200	150	200	120	V/mV MIN
Differential Input Voltage			±30	±30	±30	±30	±30	V MAX
Power Consumption	P_d	$V_{OUT} = 0V$	—	120	—	120	150	mW MAX

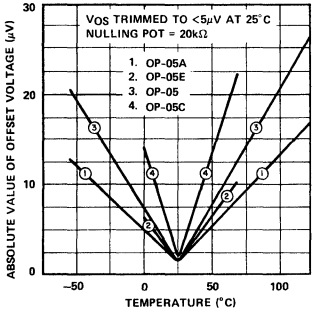
NOTES:
1. For 25°C characteristics of NT & GT devices see N & G characteristics respectively.
2. Guaranteed by design.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

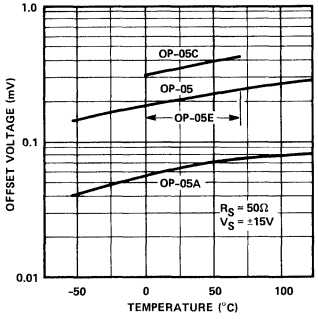
PARAMETER	SYMBOL	CONDITIONS	OP-05NT TYP	OP-05N TYP	OP-05GT TYP	OP-05G TYP	OP-05GR TYP	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \leq 50\Omega$	0.3	0.3	0.7	0.7	1.2	µV/°C
Nulled Input Offset Voltage Drift	TCV_{OSn}	$R_S \leq 50\Omega$, $R_p = 20k\Omega$	0.2	0.2	0.3	0.3	0.4	µV/°C
Average Input Offset Current Drift	TCI_{OS}		5.0	5.0	8.0	8.0	12	pA/°C
Slewing Rate	SR	$R_L \geq 2k\Omega$	0.3	0.3	0.3	0.3	0.3	V/µs
Closed Loop Bandwidth	BW	$A_{VCL} = +1$	0.6	0.6	0.6	0.6	0.6	MHz

TYPICAL PERFORMANCE CURVES

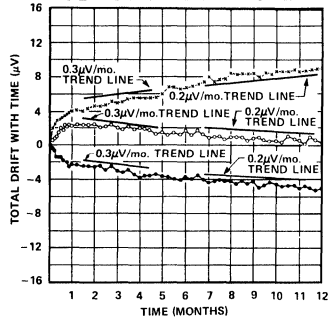
TRIMMED OFFSET VOLTAGE vs TEMPERATURE



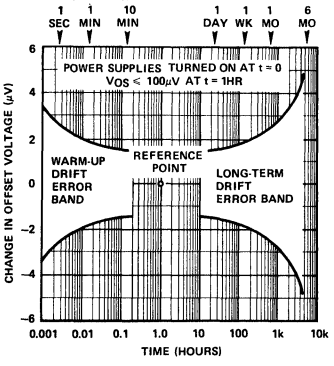
UNTRIMMED OFFSET VOLTAGE vs TEMPERATURE



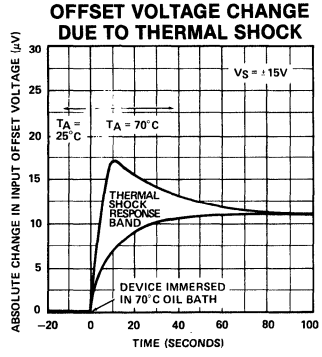
TYPICAL OFFSET VOLTAGE STABILITY vs TIME



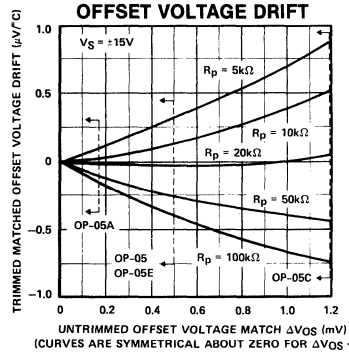
OFFSET VOLTAGE DRIFT WITH TIME



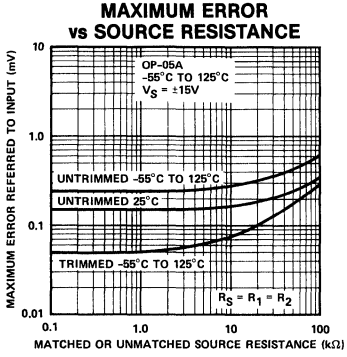
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



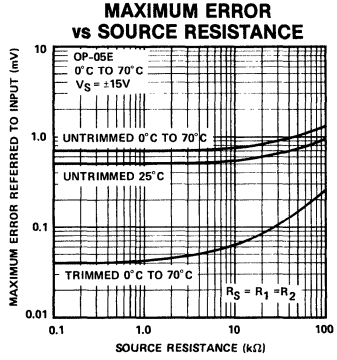
TRIMMED OFFSET VOLTAGE DRIFT



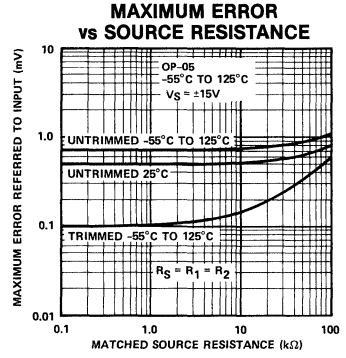
MAXIMUM ERROR vs SOURCE RESISTANCE



MAXIMUM ERROR vs SOURCE RESISTANCE

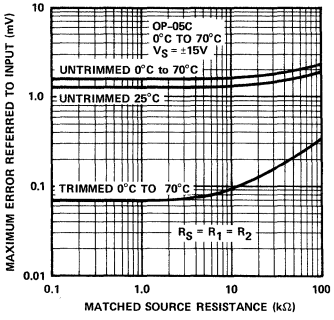


MAXIMUM ERROR vs SOURCE RESISTANCE

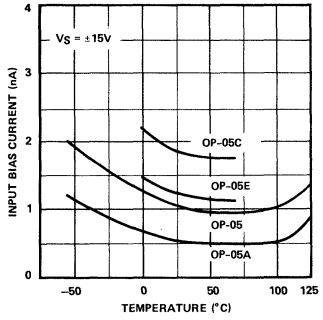


TYPICAL PERFORMANCE CURVES

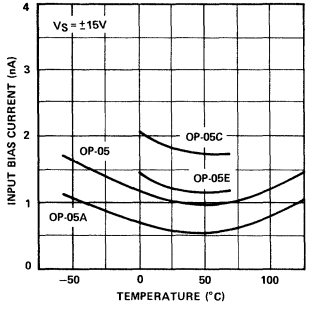
MAXIMUM ERROR vs SOURCE RESISTANCE



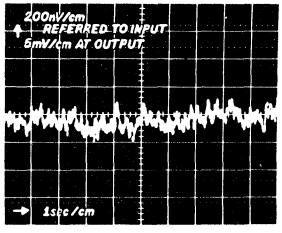
INPUT BIAS CURRENT vs TEMPERATURE



INPUT OFFSET CURRENT vs TEMPERATURE

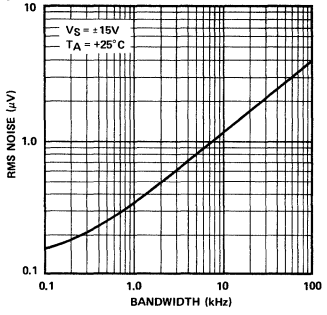


OP-05 LOW FREQUENCY NOISE

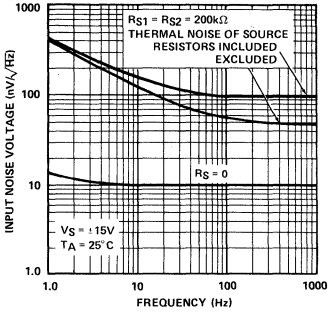


(SEE NOISE TEST CIRCUIT)

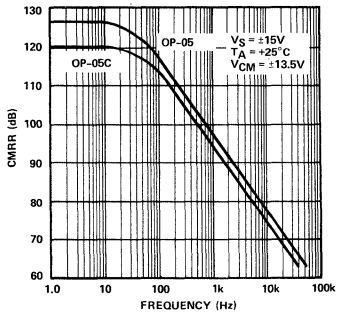
INPUT WIDEBAND NOISE vs. BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



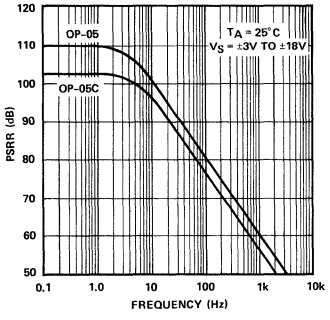
INPUT SPOT NOISE VOLTAGE vs FREQUENCY



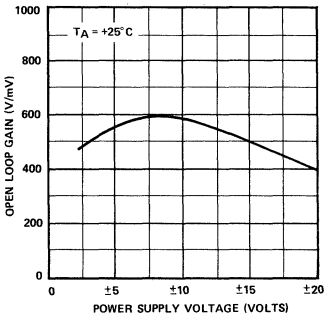
CMRR vs FREQUENCY



PSRR vs FREQUENCY

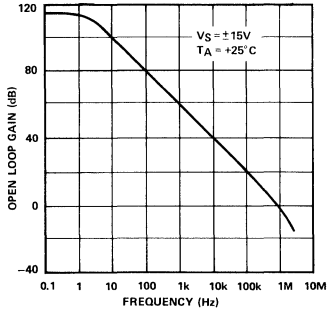


OPEN LOOP GAIN vs POWER SUPPLY VOLTAGE

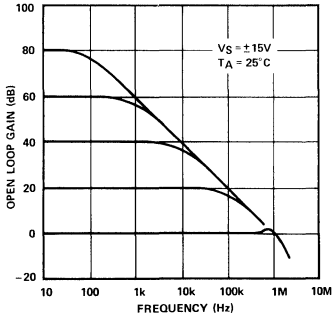


TYPICAL PERFORMANCE CURVES

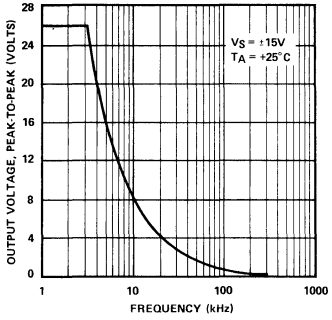
OPEN-LOOP FREQUENCY REPONSE



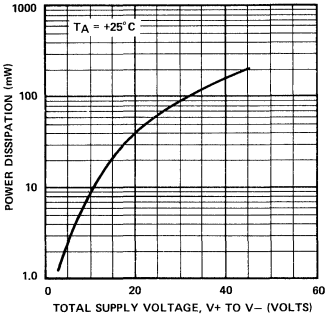
CLOSED-LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



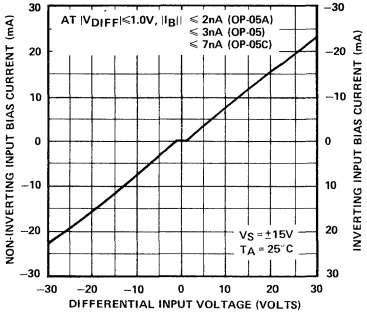
MAXIMUM UNDISTORTED OUTPUT vs FREQUENCY



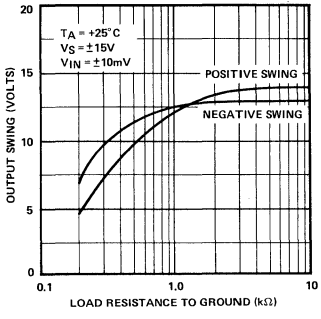
POWER CONSUMPTION vs POWER SUPPLY



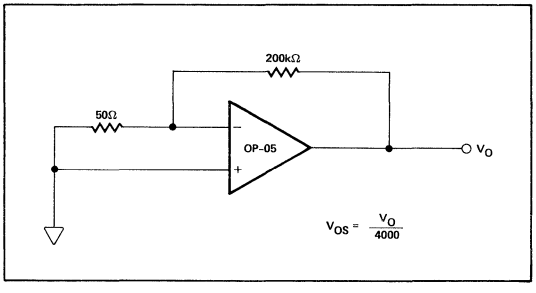
INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



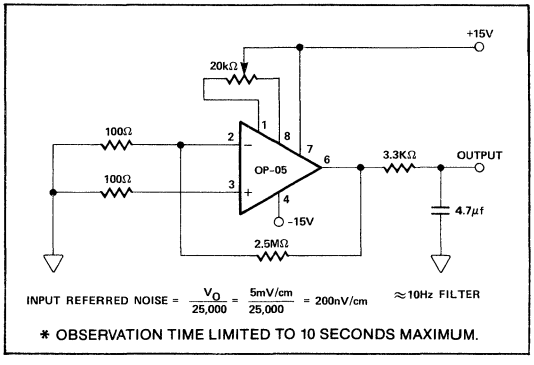
OUTPUT SWING vs LOAD



TYPICAL OFFSET VOLTAGE TEST CIRCUIT

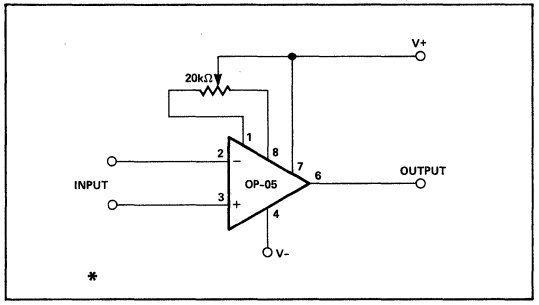


TYPICAL LOW FREQUENCY NOISE TEST CIRCUIT *

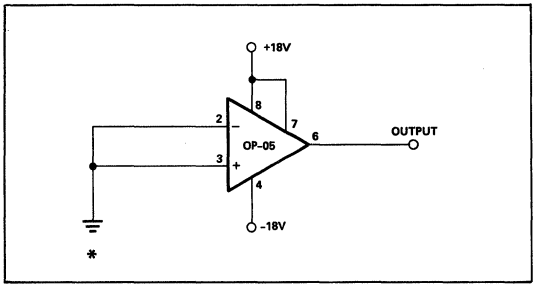


* OBSERVATION TIME LIMITED TO 10 SECONDS MAXIMUM.

OFFSET NULLING CIRCUIT



BURN-IN CIRCUIT



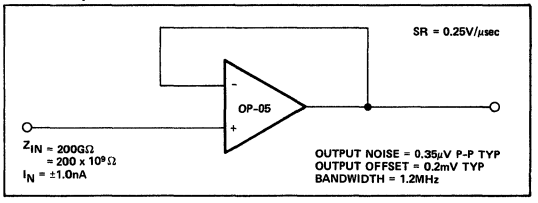
*PIN OUTS SHOWN FOR J, P, AND Z PACKAGES.

APPLICATIONS INFORMATION

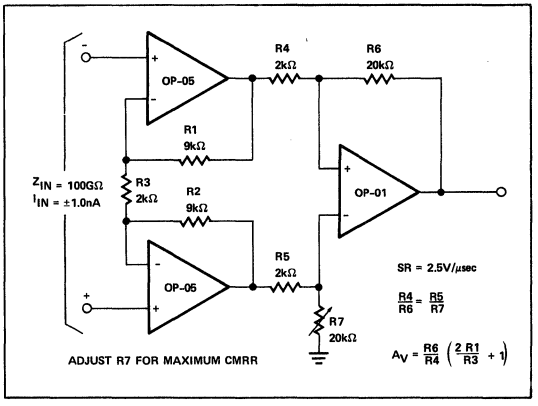
OP-05 Series devices may be fitted directly to 725 and 108/108A Series sockets with or without removal of external compensation components. Additionally, OP-05 may be fitted to unnulled 741 Series sockets; however if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP-05 operation. The OP-05 provides stable operation with load capacitances up to 500pF and ±10V swings; larger capacitances should be decoupled with 50Ω decoupling resistor. The designer is cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

TYPICAL APPLICATIONS

STABLE, HIGH IMPEDANCE BUFFER



HIGH IMPEDANCE, HIGH COMMON MODE REJECTION INSTRUMENTATION AMPLIFIER



* TO-99 package only.

OP-06

HIGH-GAIN INSTRUMENTATION OPERATIONAL AMPLIFIER

FEATURES

- **Very High Voltage Gain ..... 1,000V/mV Minimum**
- **Low Offset Voltage and Offset Current**
- **Low Drift vs. Temperature**
  (TCV_{OS}) ..... 0.8μV/ °C Maximum
- **Low Input Voltage and Current Noise**
- **Low Offset Voltage Drift with Time**
- **High Common Mode Rejection ..... 120dB Typical**
- **High Power Supply Rejection ..... 2μV/V Maximum**
- **Wide Supply Range ..... ±3.0V to ±22V**
- **±30V Input Overvoltage Protection**
- **MIL-STD-883 Processing Available**
- **Slew Rate to 100V/μs**

GENERAL DESCRIPTION

The OP-06 monolithic Instrumentation Operational Amplifier is specifically designed for accurate high-gain amplification of low level input signals in the presence of large common-mode voltages. Superior DC input characteristics include very low offset voltage and current, extremely high open-loop gain, low 1/f and wideband noise, and a minimum of "popcorn"noise. The extremely low offset voltage drift is further improved by an advanced nulling technique that provides optimum TCV_{OS} performance when V_{OS} has been nulled to zero. Very high common mode and power supply rejection enable accurate performance in the presence of large spurious signals.

Flexible external compensation provides wide bandwidth and high slew rate operation in high closed-loop gain applications. The superior long term stability, and compatibility with MIL-STD-883 processing, make the OP-06 an excellent choice for high reliability process control and aerospace applications; including strain gauge and thermocouple amplifiers, low noise audio amplifiers, and instrumentation amplifiers. The OP-06 is a direct replacement for all 725 types providing superior DC and noise performance plus the unique feature of **complete input differential voltage and output short circuit protection.**
See AN-25 for additional information.

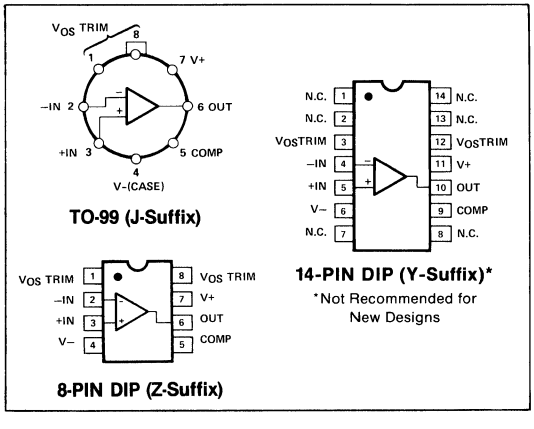
ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	PACKAGE HERMETIC DIP 8-PIN	PACKAGE HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
0.2	OP06EJ	OP06EZ	OP06EY	COM
0.2	OP06AJ*	OP06AZ*	OP06AY*	MIL
0.5	OP06FJ	OP06FZ	OP06FY	COM
0.5	OP06BJ*	OP06BZ*	OP06BY*	MIL
1.3	OP06GJ	OP06GZ	OP06GY	COM
1.3	OP06CJ*	OP06CZ*	OP06CY*	MIL

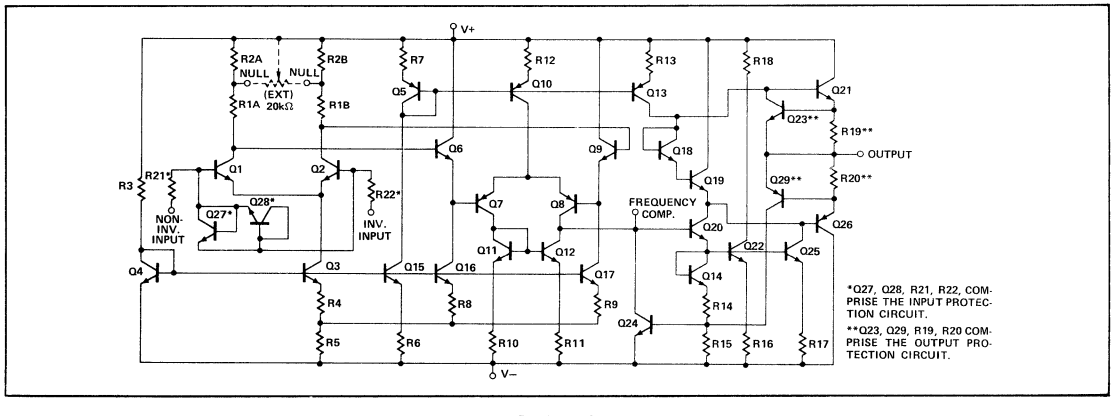
*Also available with MII-STD-883B processing. To order add /883 as a suffix to the part number.

†All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 3)

Supply Voltage ..... ±22V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±22V
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range
OP-06A, OP-06B, OP-06C ..... −55°C to +125°C
OP-06E, OP-06F, OP-06G ..... 0°C to +70°C
Lead Temperature Range (Soldering, 60 sec.) ..... 300°C
DICE Junction Temperature ..... −65°C to +150°C

NOTES:
1. See table for maximum ambient temperature rating and derating factor.

Package Type	Maximum Ambient Temperature for Rating	Derated Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
14-PIN HERMETIC DIP (Y)	100°C	10.0mW/°C
8-PIN HERMETIC DIP (Z)	75°C	6.7mV/°C

2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
3. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-06A/E			OP-6B/F			OP-6C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \le 20k\Omega$ (Note 2)	—	0.06	0.2	—	0.2	0.5	—	0.4	1.3	mV
Input Offset Current	I_{OS}		—	0.3	2.0	—	0.75	5.0	—	2	13	nA
Input Bias Current	I_B		—	30	70	—	30	80	—	40	110	nA
Input Noise Voltage Density	e_n	$f_o = 10Hz$	—	9.0	15.0	—	9.0	15.0	—	9.0	15.0	$nV/\sqrt{Hz}$
		(Note 1) $f_o = 100Hz$	—	8.0	9.0	—	8.0	9.0	—	8.0	9.0	
		$f_o = 1000Hz$	—	7.0	7.5	—	7.0	7.5	—	7.0	7.5	
Input Noise Current Density	i_n	$f_o = 10Hz$	—	0.5	1.2	—	0.5	1.2	—	0.6	1.4	$pA/\sqrt{Hz}$
		(Note 1) $f_o = 100Hz$	—	0.25	0.6	—	0.25	0.6	—	0.3	0.7	
		$f_o = 1000Hz$	—	0.15	0.25	—	0.15	0.25	—	0.2	0.3	
Input Resistance	R_{IN}	(Note 3)	0.8	1.8	—	0.7	1.8	—	0.5	1.5	—	MΩ
Large Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	1,000,000	3,000,000	—	1,000,000	3,000,000	—	500,000	3,000,000	—	V/V
Output Voltage Swing	V_O	$R_L \ge 10k\Omega$	±12.5	±13.0	—	±12.5	±13.0	—	±12.0	±13.0	—	V
		$R_L \ge 2k\Omega$	±12.0	±12.8	—	±12.0	±12.8	—	±11.5	±12.8	—	
		$R_L \ge 1k\Omega$	±11.0	±12.5	—	±11.0	±12.5	—	—	±12.0	—	
Input Voltage Range	IVR		±13.5	±14.0	—	±13.5	±14.0	—	±13.5	±14.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$, $R_S \le 20k\Omega$	114	120	—	114	120	—	110	115	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$, $R_S \le 20k\Omega$	—	0.5	2.0	—	1.0	5.0	—	2.0	10	μV/V
Power Consumption	P_d		—	90	120	—	90	120	—	110	150	mW
Large Signal Voltage Gain	A_{VO}	$R_L \ge 500\Omega$ (Note 3), $V_O = \pm 0.5V$, $V_S = \pm 3V$	100,000	600,000	—	100,000	600,000	—	60,000	600,000	—	V/V
Power Consumption	P_d	$V_S = \pm 3V$	—	4	6	—	4	6	—	4	8	mW

NOTES:
1. Sample tested.
2. Thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent the realization of the performance indicated if both sides of the contacts are not kept at approximately the same temperature. Temperature gradients should therefore be minimized.
3. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-06A MIN	OP-06A TYP	OP-06A MAX	OP-06B MIN	OP-06B TYP	OP-06B MAX	OP-06C MIN	OP-06C TYP	OP-06C MAX	UNITS
Input Offset Voltage (Without external trim)	V_{OS}	$R_S \le 20k\Omega$ (Note 2)	—	0.08	0.28	—	0.3	0.7	—	0.5	1.6	mV
Average Input Offset Voltage Drift (Without external trim)	TCV_{OS}	$R_S = 50\Omega$ (Notes 1,2)	—	0.3	0.8	—	0.7	2.0	—	1.4	4.5	µV/°C
Average Input Offset Voltage Drift (With external trim)	TCV_{OSn}	$R_S = 50\Omega$ (Notes 1,2) $R_P = 20k\Omega$	—	0.2	0.6	—	0.28	1.0	—	0.5	1.5	µV/°C
Input Offset Current	I_{OS}	T_AMAX T_AMIN	— —	0.25 0.8	1.0 4.0	— —	0.6 2.0	4.0 18.0	— —	2.0 3.0	15 25	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	3	20	—	8	90	—	14	150	pA/°C
Input Bias Current	I_B	T_AMAX T_AMIN	— —	22 40	60 120	— —	25 45	70 180	— —	35 45	110 180	nA
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$ $R_S \le 20k\Omega$	109	112	—	109	112	—	95	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$ $R_S \le 20k\Omega$	—	1.0	5.0	—	2.0	8.0	—	3.0	15	µV/V
Large Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$; $R_L \ge 2k\Omega$ T_AMAX T_AMIN	1,000,000 700,000	3,500,000 2,000,000	— —	1,000,000 700,000	3,500,000 1,800,000	— —	400,000 300,000	3,200,000 1,700,000	— —	V/V
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12.0	±12.6	—	±12.0	±12.6	—	±11.0	±12.6	—	V

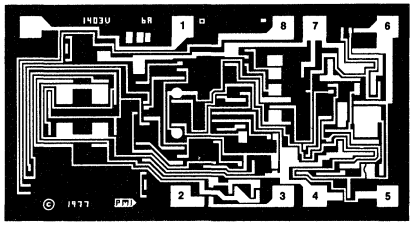
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-06E MIN	OP-06E TYP	OP-06E MAX	OP-06F MIN	OP-06F TYP	OP-06F MAX	OP-06G MIN	OP-06G TYP	OP-06G MAX	UNITS
Input Offset Voltage (Without external trim)	V_{OS}	$R_S \le 20k\Omega$ (Note 2)	—	0.08	0.28	—	0.25	0.6	—	0.5	1.6	mV
Average Input Offset Voltage Drift (Without external trim)	TCV_{OS}	$R_S = 50\Omega$ (Notes 1,2)	—	0.3	0.8	—	0.7	2.0	—	1.4	4.5	µV/°C
Average Input Offset Voltage Drift (With external trim)	TCV_{OSn}	$R_S = 50\Omega$ (Notes 1,2) $R_P = 20k\Omega$	—	0.2	0.6	—	0.28	1.0	—	0.5	1.5	µV/°C
Input Offset Current	I_{OS}	T_AMAX T_AMIN	— —	0.25 0.8	1.0 4.0	— —	0.65 2.0	5.0 18.0	— —	2.0 3.0	15 25	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	3	20	—	8	90	—	14	150	pA/°C
Input Bias Current	I_B	T_AMAX T_AMIN	— —	22 40	60 120	— —	30 45	80 180	— —	35 45	110 180	nA
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$ $R_S \le 20k\Omega$	109	112	—	109	112	—	95	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$ $R_S \le 20k\Omega$	—	1.0	5.0	—	1.5	7.0	—	3.0	15	µV/V
Large Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$; $R_L \ge 2k\Omega$ T_AMAX T_AMIN	1,000,000 800,000	3,500,000 2,000,000	— —	1,000,000 800,000	3,500,000 1,800,000	— —	400,000 300,000	3,200,000 1,700,000	— —	V/V
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12.0	±12.6	—	±12.0	±12.6	—	±11.0	±12.6	—	V

NOTES:

1. Sample tested.
2. Thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent the realization of the performance indicated if both sides of the contacts are not kept at approximately the same temperature. Temperature gradients should therefore be minimized.

DICE CHARACTERISTICS



DIE SIZE 0.094 x 0.050 inch

1. NULL
2. INVERTING INPUT
3. NON-INVERTING INPUT
4. V –
5. COMPENSATION
6. OUTPUT
7. V+
8. NULL

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-06N LIMIT	OP-06G LIMIT	OP-06GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	0.2	0.5	1.3	mV MAX
Input Offset Current	I_{OS}		2	5	13	nA MAX
Input Bias Current	I_B		70	80	110	nA MAX
Input Resistance Differential Mode	R_{IN}	(Note 1)	0.8	0.7	0.5	MΩ MIN
Input Voltage Range	IVR		±13.5	±13.5	±13.5	V MIN
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$ $R_S \leq 20k\Omega$	114	114	110	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$ $R_S \leq 20k\Omega$	2	5	10	μV/V MAX
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±11.0	± 12.5 ± 12.0 ±11.0	±12.0 ± 11.5 —	V MIN
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	1000	1000	500	V/mV MIN
Differential Input Voltage			±30	±30	±30	V MAX
Power Consumption ($V_{OUT} = 0V$)	P_d		120	120	150	mW MAX

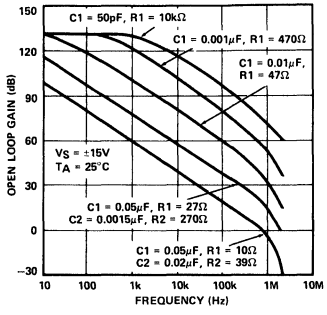
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-06N TYPICAL	OP-06G TYPICAL	OP-06GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \leq 50\Omega$	0.3	0.7	1.4	μV/°C
Nulled Input Offset Voltage Drift	TCV_{OSn}	$R_S \leq 50k\Omega$ $R_P = 20k\Omega$	0.2	0.28	0.5	μV/°C
Average Input Offset Current Drift	TCI_{OS}		3	8	14	pA/°C

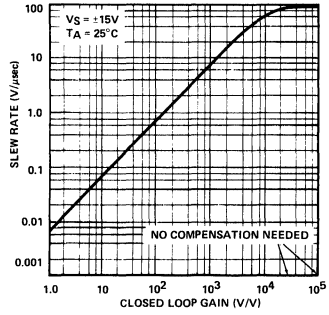
NOTE:
1. Guaranteed by design.

TYPICAL DYNAMIC PERFORMANCE CURVES

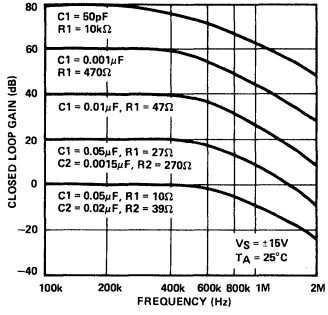
OPEN LOOP RESPONSE FOR VALUES OF COMPENSATION



SLEW RATE USING RECOMMENDED COMPENSATION NETWORKS



CLOSED LOOP FREQUENCY RESPONSE FOR VALUES OF COMPENSATION

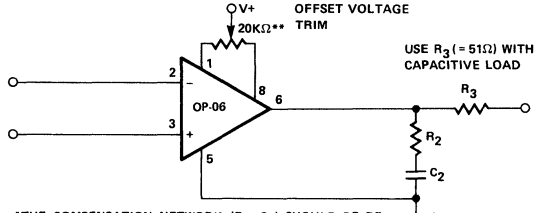


FREQUENCY COMPENSATION

COMPENSATION VALUES

Avcl	R_1 (Ω)	C_1 (μF)	R_2 (Ω)	C_2 (μF)
10000	10k	50pF	—	—
1000	470	0.001	—	—
100	47	0.01	—	—
10	27	0.05	270	0.0015
1	10	0.05	39	0.02

COMPENSATION CIRCUIT (J or Z PACKAGE)

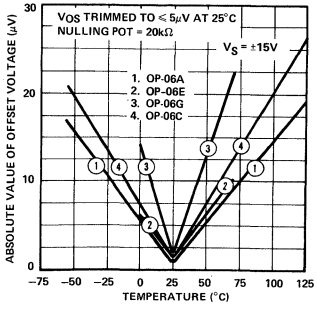


*THE COMPENSATION NETWORK (R_1, C_1) SHOULD BE RETURNED TO THE V–TERMINAL. IF THE NETWORK IS RETURNED TO GROUND, SERIOUS DEGRADATION OF POWER SUPPLY REJECTION PERFORMANCE WITH FREQUENCY WILL OCCUR. SEE TYPICAL CURVES (PSRR vs FREQUENCY).

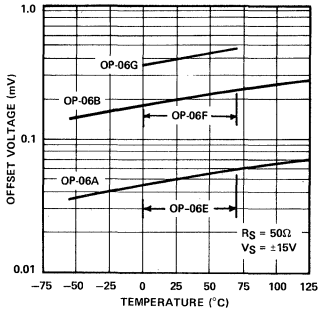
**THE TRIMMING POTENTIOMETER SHOULD BE 20kΩ FOR OPTIMUM NULLED OFFSET VOLTAGE DRIFT. SEE TYPICAL CURVES (TRIMMED OFFSET VOLTAGE DRIFT AS A FUNCTION OF TRIMMING POTENTIOMETER).

TYPICAL PERFORMANCE CURVES

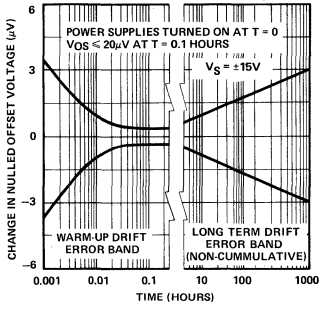
TRIMMED OFFSET VOLTAGE vs TEMPERATURE



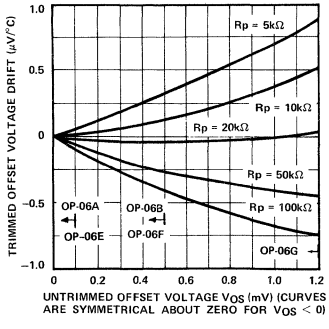
OFFSET VOLTAGE vs TEMPERATURE



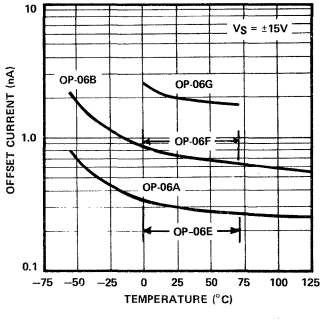
OFFSET VOLTAGE DRIFT WITH TIME



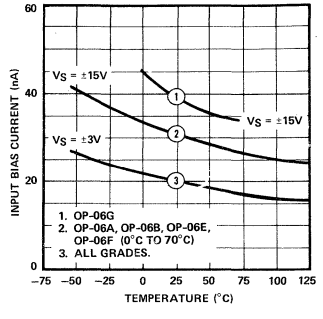
TRIMMED OFFSET VOLTAGE DRIFT AS A FUNCTION OF TRIMMING POTENTIOMETER (R_P) SIZE AND V_{OS}



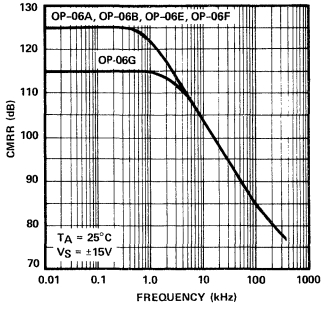
OFFSET CURRENT vs TEMPERATURE



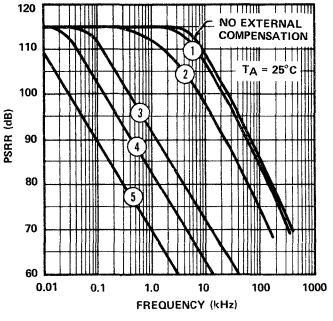
INPUT BIAS CURRENT vs TEMPERATURE



CMRR vs FREQUENCY

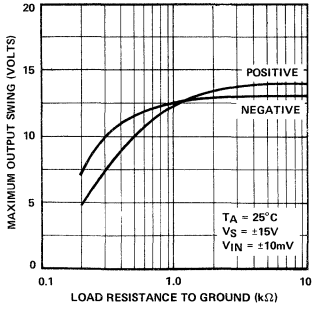


PSRR vs FREQUENCY (OP-06B, OP-06E)



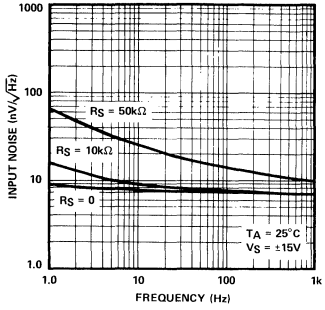
1. C1 = 0.001μF, R1 = 470Ω FROM PIN 5 TO V−
2. C1 = 0.1μF, R1 = 5Ω TO V−
3. C1 = 0.001μF; R1 = 470Ω FROM PIN 5 TO GND
4. C1 = 0.05μF, R1 = 10Ω, C2 = 0.02μF, R2 = 39Ω TO V−
5. C1 = 0.05μF, R1 = 10Ω, C2 = 0.02μF, R2 = 39Ω TO GND

OUTPUT SWING vs LOAD RESISTANCE

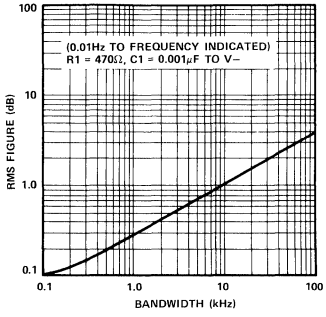


TYPICAL PERFORMANCE CURVES

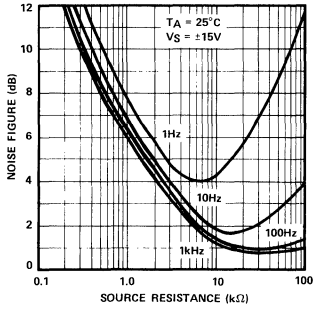
TYPICAL INPUT NOISE VOLTAGE



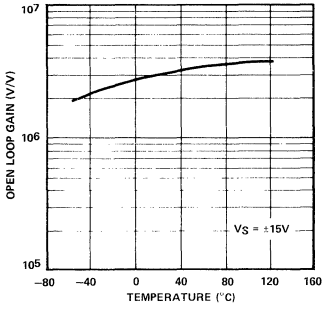
INPUT WIDEBAND NOISE vs BANDWIDTH



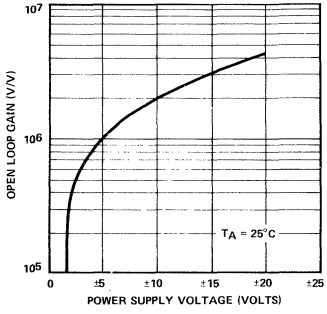
NOISE FIGURE vs SOURCE RESISTANCE



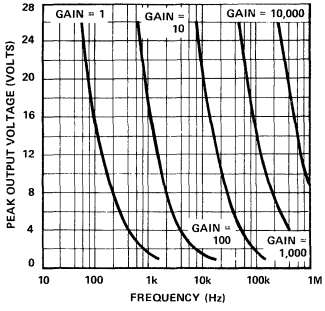
OPEN LOOP GAIN vs TEMPERATURE



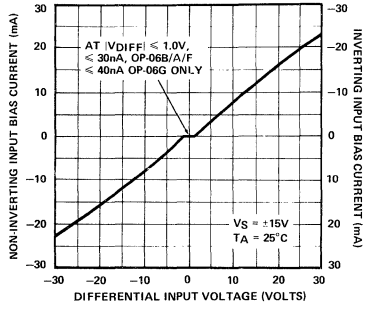
OPEN LOOP GAIN vs POWER SUPPLY VOLTAGE



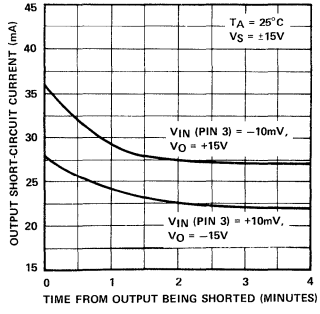
MAXIMUM UNDISTORTED OUTPUT vs FREQUENCY



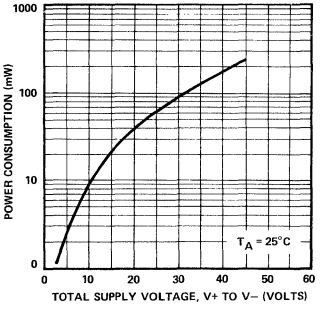
INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



OUTPUT SHORT-CIRCUIT CURRENT

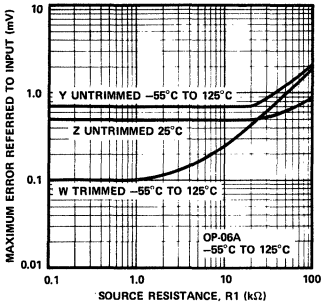


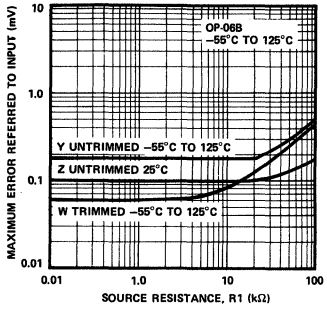
POWER CONSUMPTION vs SUPPLY VOLTAGE

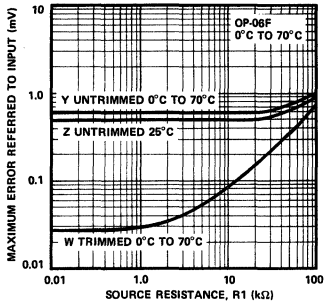


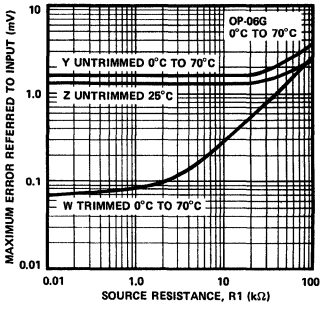
Note: For further information refer to AN-15, "Minimization of Noise in Operational Amplifier Applications".

GUARANTEED PERFORMANCE CURVES









These graphs depict maximum error referred to the input as a function of source resistance (R_1). Curves W are shown with V_{OS} trimmed at +25°C and include errors due to V_{OS} and I_{OS} over the indicated temperature range. Curves Y and Z plot maximum errors with V_{OS} not trimmed.

OP-07

ULTRA-LOW OFFSET VOLTAGE OPERATIONAL AMPLIFIER

FEATURES

- **Ultra-Low V_{OS}** **10μV**
- **Ultra-Low V_{OS} Drift** ..... **0.2μV/°C**
- **Ultra-Stable vs Time** **0.2μV/Month**
- **Ultra-Low Noise** ..... **0.35μV_{p-p}**
- **No External Components Required**
- **Large Input Voltage Range** ..... **±14.0V**
- **Wide Supply Voltage Range** ..... **±3V to ±18V**
- **Fits 725, 108A/308A, 741, AD510 Sockets**
- **125° C Temperature Tested Dice**

GENERAL DESCRIPTION

The OP-07 Series represents a breakthrough in monolithic operational amplifier performance — V_{OS} of 10μV, TCV_{OS} of 0.2μV/° C, and long-term stability of 0.2μV/month are achieved by a low-noise, bipolar input transistor amplifier circuit. Elimination of external components for offset nulling, frequency compensation, and device protection improves the system MTBF and reduces cost. Excellent device interchangeability provides reduced system assembly time and eliminates field recalibrations.

True differential inputs with wide input voltage range and outstanding common-mode rejection provide excellent performance in high-noise environments and non-inverting applications. Low bias currents and extremely-high input impedances are maintained over the entire temperature range.

The OP-07 provides unparalleled performance for low noise, high-accuracy amplification of very low-level signals in transducer applications. Devices are available in chip form for use in hybrid circuitry. The OP-07 is a direct replacement for 725, 108A/308A*, and OP-05 amplifiers; 741-types may be directly replaced by removing the 741's nulling potentiometer.

*TO-99 package only. For Matched Dual see OP-207.

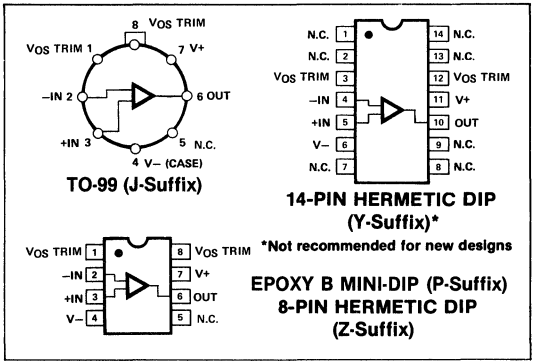
ORDERING INFORMATION†

T_A = 25° C V_{OS} MAX (μV)	PACKAGE: HERMETIC TO-99 8-PIN	HERMETIC DIP 8-PIN	HERMETIC DIP 14-PIN	PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
25	OP07AJ*	OP07AZ*	OP07AY*		MIL
75	OP07EJ	OP07EZ	OP07EY	OP07EP	COM
75	OP07J*	OP07Z*	OP07Y*		MIL
150	OP07CJ	OP07CZ	OP07CY	OP07CP	COM
150	OP07DJ			OP07DP	COM

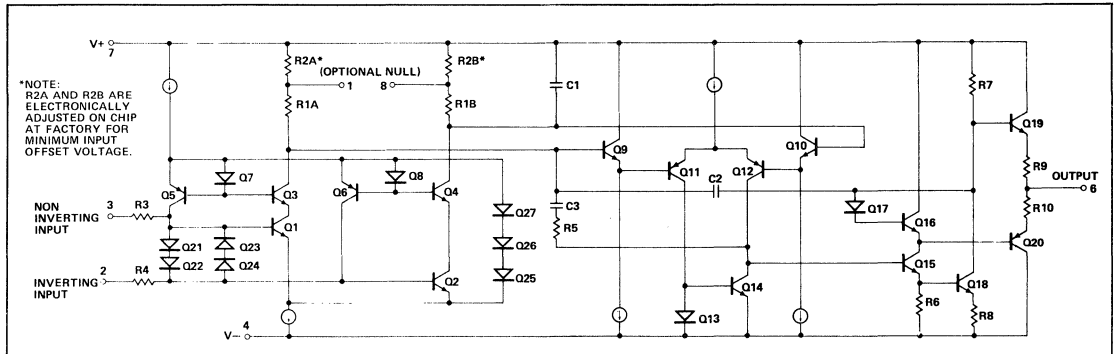
* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



PINOUTS FOR J, Z AND P PACKAGES.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±22V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage (Note 3) ..... ±22V
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range
J, Y, and Z Packages ..... -65°C to + 150°C
P Package ..... -65°C to + 125°C
Operating Temperature Range
OP-07A, OP-07 ..... −55 to +125°C
OP-07E, OP-07C, OP-07D ..... 0°C to +70°C
Lead Temperature Range (Soldering, 60 sec.) ..... 300°C
DICE Junction Temperature (T_j) ..... −65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.
2. Absolute maximum ratings apply to both packaged parts and dice, unless otherwise noted.
3. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
14-Pin Hermetic DIP (Y)	100°C	10.0mW/°C
8-Pin Hermetic Dip (Z)	75°C	6.7mW/°C
8-Pin Plastic Dip (P)	36°C	5.6mW/°C

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

			OP-07A			OP-07			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	10	25	—	30	75	μV
Long Term Input Offset Voltage Stability	ΔV_{OS}/Time	(Note 2)	—	0.2	1.0	—	0.2	1.0	μV/Mo
Input Offset Current	I_{OS}		—	0.3	2.0	—	0.4	2.8	nA
Input Bias Current	I_B		—	±0.7	±2.0	—	±1.0	±3.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	—	0.35	0.6	—	0.35	0.6	μV_{p-p}
Input Noise Voltage Density	e_n	f_o = 10Hz f_o = 100Hz (Note 3) f_o = 1000Hz	— — —	10.3 10.0 9.6	18.0 13.0 11.0	— — —	10.3 10.0 9.6	18.0 13.0 11.0	$nV/\sqrt{Hz}$
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 3)	—	14	30	—	14	30	pA_{p-p}
Input Noise Current Density	i_n	f_o = 10Hz f_o = 100Hz (Note 3) f_o = 1000Hz	— — —	0.32 0.14 0.12	0.80 0.23 0.17	— — —	0.32 0.14 0.12	0.80 0.23 0.17	$pA/\sqrt{Hz}$
Input Resistance — Differential Mode	R_{IN}	(Note 4)	30	80	—	20	60	—	MΩ
Input Resistance — Common Mode	R_{INCM}		—	200	—	—	200	—	GΩ
Input Voltage Range	IVR		±13.0	±14.0	—	±13.0	±14.0	—	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±13V	110	126	—	110	126	—	dB
Power Supply Rejection Ratio	PSRR	V_S ±3V to ±18V	—	4	10	—	4	10	μV/V
Large Signal Voltage Gain	A_{VO}	R_L ≥2kΩ, V_O = ±10V R_L ≥500Ω, V_O = ±0.5V V_S = ±3V (Note 3)	300 150	500 400	—	200 150	500 400	—	V/mV
Output Voltage Swing	V_O	R_L ≥10kΩ R_L ≥2kΩ R_L ≥1kΩ	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0	— — —	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0	— — —	V
Slewing Rate	SR	R_L ≥2kΩ (Note 3)	0.1	0.3	—	0.1	0.3	—	V/μs
Closed Loop Bandwidth	BW	A_{VCL} = +1.0 (Note 3)	0.4	0.6	—	0.4	0.6	—	MHz
Open Loop Output Resistance	R_O	V_O = 0, I_O = 0	—	60	—	—	60	—	Ω
Power Consumption	P_d	V_S = ±15V, No load V_S = ±3V, No load	— —	75 4	120 6	— —	75 4	120 6	mW
Offset Adjustment Range		R_p = 20kΩ	—	±4	—	—	±4	—	mV

NOTES:

1. OP-07A grade V_{OS} is measured one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 seconds after application of power.
2. Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV — refer to typical performance curves. Parameter is sample tested.
3. Sample tested.
4. Guaranteed by design.

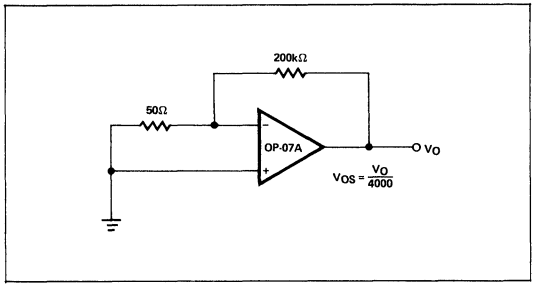
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07A MIN	OP-07A TYP	OP-07A MAX	OP-07 MIN	OP-07 TYP	OP-07 MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	25	60	—	60	200	μV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 2)	—	0.2	0.6	—	0.3	1.3	μV/°C
With External Trim	TCV_{OSn}	$R_p = 20k\Omega$ (Note 2)	—	0.2	0.6	—	0.3	1.3	
Input Offset Current	I_{OS}		—	0.8	4.0	—	1.2	5.6	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	5	25	—	8	50	pA/°C
Input Bias Current	I_B		—	±1.0	±4.0	—	±2.0	±6.0	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	8	25	—	13	50	pA/°C
Input Voltage Range	IVR		±13.0	±13.5	—	±13.0	±13.5	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	106	123	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	5	20	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	200	400	—	150	400	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12.0	±12.6	—	±12.0	±12.6	—	V

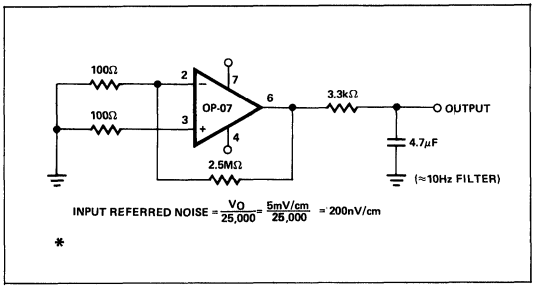
NOTES:

1. OP-07A grade V_{OS} is measured one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 seconds after application of power.
2. Sample tested.

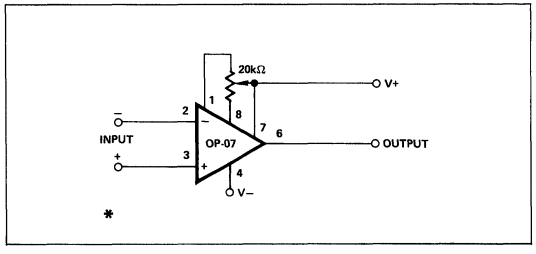
TYPICAL OFFSET VOLTAGE TEST CIRCUIT



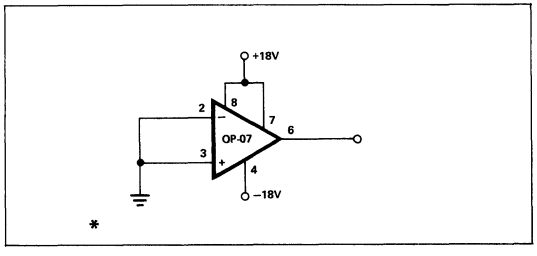
TYPICAL LOW FREQUENCY NOISE TEST CIRCUIT



OPTIONAL OFFSET NULLING CIRCUIT



BURN-IN CIRCUIT



*PINOUTS FOR P, J AND Z PACKAGES.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-07E			OP-07C			OP-07D			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	30	75	—	60	150	—	60	150	μV
Long Term V_{OS} Stability	V_{OS}/Time	(Note 2)	—	0.3	1.5	—	0.4	2.0	—	0.5	3.0	μV/Mo
Input Offset Current	I_{OS}		—	0.5	3.8	—	0.8	6.0	—	0.8	6.0	nA
Input Bias Current	I_B		—	±1.2	±4.0	—	±1.8	±7.0	—	±2.0	±12	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	—	0.35	0.6	—	0.38	0.65	—	0.38	0.65	μV_{p-p}
Input Noise Voltage Density	e_n	$f_o = 10Hz$	—	10.3	18.0	—	10.5	20.0	—	10.5	20.0	$nV/\sqrt{Hz}$
		$f_o = 100Hz$ (Note 3)	—	10.0	13.0	—	10.2	13.5	—	10.3	13.5	
		$f_o = 1000Hz$	—	9.6	11.0	—	9.8	11.5	—	9.8	11.5	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 3)	—	14	30	—	15	35	—	15	35	pA_{p-p}
Input Noise Current Density	i_n	$f_o = 10Hz$	—	0.32	0.80	—	0.35	0.90	—	0.35	0.90	$pA/\sqrt{Hz}$
		$f_o = 100Hz$ (Note 3)	—	0.14	0.23	—	0.15	0.27	—	0.15	0.27	
		$f_o = 1000Hz$	—	0.12	0.17	—	0.13	0.18	—	0.13	0.18	
Input Resistance — Differential Mode	R_{IN}	(Note 4)	15	50	—	8	33	—	7	31	—	MΩ
Input Resistance — Common Mode	R_{INCM}		—	160	—	—	120	—	—	120	—	GΩ
Input Voltage Range	IVR		±13.0	±14.0	—	±13.0	±14.0	—	±13.0	±14.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	100	120	—	94	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	7	32	—	7	32	$\mu V/V$
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	500	—	120	400	—	120	400	—	V/mV
		$R_L \geq 500\Omega$, $V_O = \pm 0.5V$, $V_S = \pm 3V$ (Note 3)	150	400	—	100	400	—	—	400	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.0	±13.0	—	±12.0	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±11.5	±12.8	—	±11.5	±12.8	—	
		$R_L \geq 1k\Omega$	±10.5	±12.0	—	—	±12.0	—	—	±12.0	—	
Slewing Rate	SR	$R_L \geq 2k\Omega$ (Note 3)	0.1	0.3	—	0.1	0.3	—	0.1	0.3	—	$V/\mu s$
Closed Loop Bandwidth	BW	$A_{VCL} = +1.0$ (Note 3)	0.4	0.6	—	0.4	0.6	—	0.4	0.6	—	MHz
Open Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	—	60	—	Ω
Power Consumption	P_d	$V_S = \pm 15V$, No load	—	75	120	—	80	150	—	80	150	mW
		$V_S = \pm 3V$, No load	—	4	6	—	4	8	—	4	8	
Offset Adjustment Range		$R_p = 20k\Omega$	—	±4	—	—	±4	—	—	±4	—	mV

NOTES:

1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically $2.5\mu V$ — refer to typical performance curves. Parameter is sample tested.
3. Sample tested.
4. Guaranteed by design.

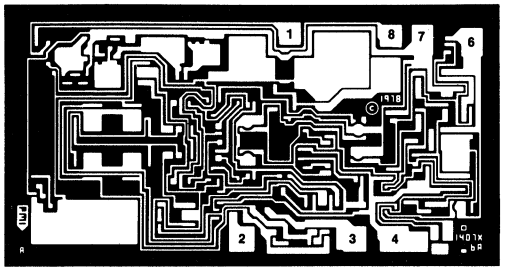
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \leq T_A \leq +70°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07E MIN	OP-07E TYP	OP-07E MAX	OP-07C MIN	OP-07C TYP	OP-07C MAX	OP-07D MIN	OP-07D TYP	OP-07D MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	45	130	—	85	250	—	85	250	μV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 2)	—	0.3	1.3	—	0.5	1.8	—	0.7	2.5	μV/°C
With External Trim	TCV_{OSn}	$R_p = 20k\Omega$ (Note 2)	—	0.3	1.3	—	0.4	1.6	—	0.7	2.5	μV/°C
Input Offset Current	I_{OS}		—	0.9	5.3	—	1.6	8.0	—	1.6	8.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	8	35	—	12	50	—	12	50	pA/°C
Input Bias Current	I_B		—	±1.5	±5.5	—	±2.2	±9.0	—	±3.0	±14	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	13	35	—	18	50	—	18	50	pA/°C
Input Voltage Range	IVR		±13.0	±13.5	—	±13.0	±13.5	—	±13.0	±13.5	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	123	—	97	120	—	94	106	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	—	10	51	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	180	450	—	100	400	—	100	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±12.6	—	±11.0	±12.6	—	±11.0	±12.6	—	V

NOTES:

1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. Sample tested.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



DIE SIZE 0.100 × 0.053 inch

1. BALANCE
2. INVERTING INPUT
3. NON-INVERTING INPUT
4. V−
6. OUTPUT
7. V+
8. BALANCE

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$ for OP-07N, OP-07G and OP-07GR devices, $T_A = +125°C$ for OP-07NT and OP-07GT, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07NT LIMIT	OP-07N LIMIT	OP-07GT LIMIT	OP-07G LIMIT	OP-07GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		140	40	210	80	150	μV MAX
Input Offset Current	I_{OS}		4.0	2.0	5.6	2.8	6.0	nA MAX
Input Bias Current	I_B		±4.0	±2.0	±6.0	±3.0	±7.0	nA MAX
Input Resistance Differential Mode	R_{IN}	(Note 2)	—	20.0	—	20.0	8.0	MΩ MIN
Input Voltage Range	IVR		±13.0	±13.0	±13.0	±13.0	±13.0	V MIN
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.0V$	100	110	100	110	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	20	10	20	10	30	μV/V MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$	—	±12.5	—	±12.0	±12.0	V MIN
		$R_L = 2k\Omega$	±12.0	±12.0	±12.0	±11.5	±11.5	
		$R_L = 1k\Omega$	—	±10.5	—	±10.5	—	
Large Signal Voltage Gain	A_{VO}	$R_L = 2k\Omega$, $V_O = \pm 10V$	200	200	150	120	120	V/mV MIN
Differential Input Voltage			±30	±30	±30	±30	±30	V MAX
Power Consumption	P_D	$V_{OUT} = 0V$	—	120	—	120	150	mW MAX

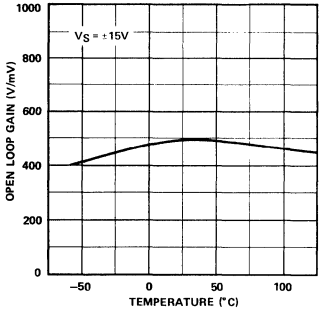
NOTE:
1. For 25°C characteristics of OP-07NT and OP-07GT, see OP-07N and OP-07G characteristics, respectively.
2. Guaranteed by design.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

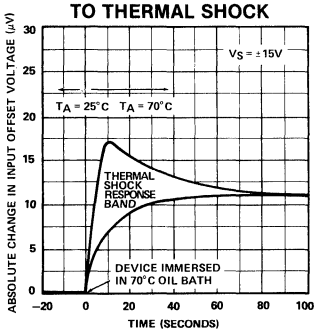
PARAMETER	SYMBOL	CONDITIONS	OP-07NT TYP	OP-07N TYP	OP-07GT TYP	OP-07G TYP	OP-07GR TYP	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	0.2	0.2	0.3	0.3	0.7	μV/°C
Nulled Input Offset Voltage Drift	TCV_{OSn}	$R_S = 50\Omega$, $R_P = 20k\Omega$	0.2	0.2	0.3	0.3	0.7	μV/°C
Average Input Offset Current Drift	TCI_{OS}		5.0	5.0	8.0	8.0	12.0	pA/°C
Slewing Rate	SR	$R_L \geq 2k\Omega$	0.3	0.3	0.3	0.3	0.3	V/μs
Closed Loop Bandwidth	BW	$A_{VCL} = +1.0$	0.6	0.6	0.6	0.6	0.6	MHz

TYPICAL PERFORMANCE CURVES

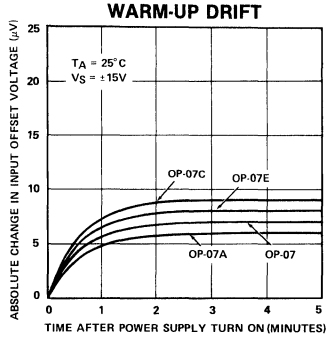
OPEN-LOOP GAIN vs TEMPERATURE



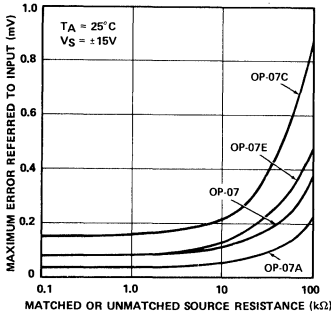
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



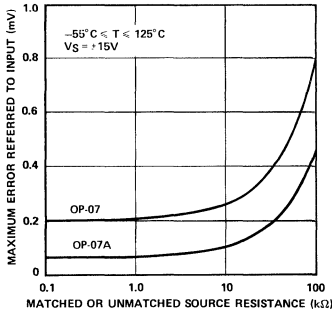
WARM-UP DRIFT



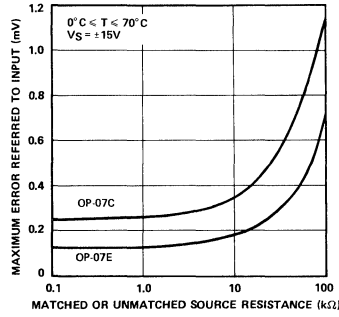
MAXIMUM ERROR vs SOURCE RESISTANCE



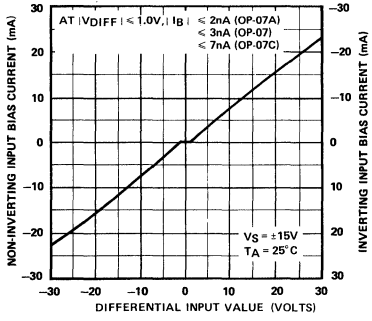
MAXIMUM ERROR vs SOURCE RESISTANCE



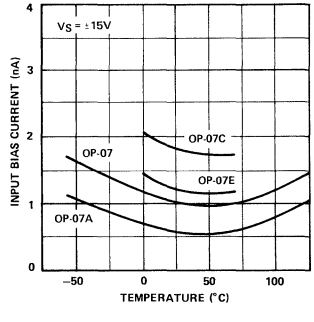
MAXIMUM ERROR vs SOURCE RESISTANCE



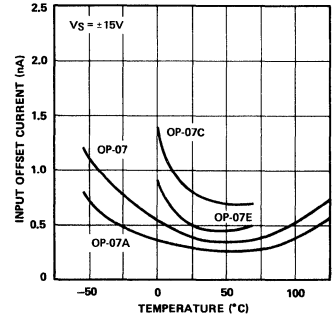
INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



INPUT BIAS CURRENT vs TEMPERATURE

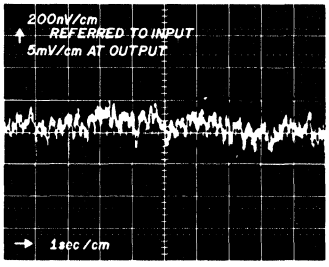


INPUT OFFSET CURRENT vs TEMPERATURE



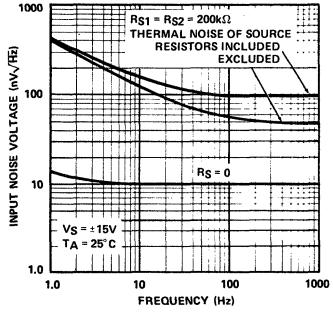
TYPICAL PERFORMANCE CURVES

OP-07 LOW FREQUENCY NOISE

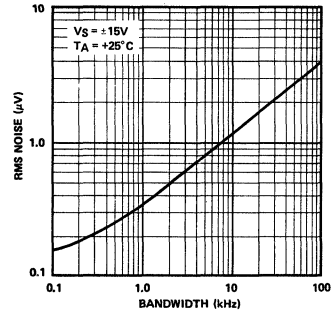


(SEE NOISE TEST CIRCUIT)

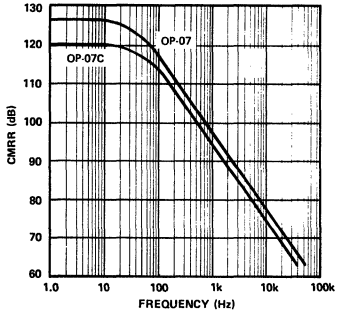
TOTAL INPUT NOISE VOLTAGE vs FREQUENCY



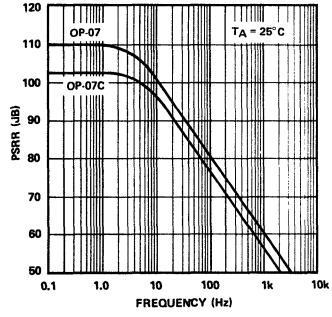
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



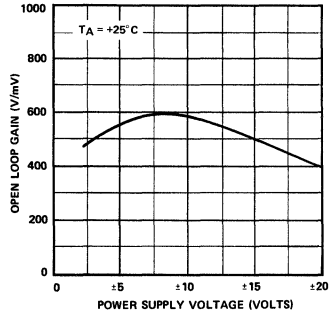
CMRR vs FREQUENCY



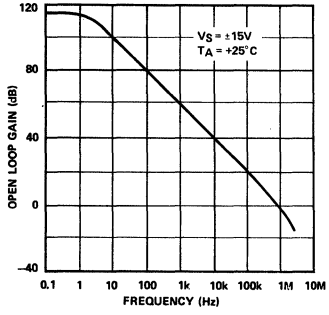
PSRR vs FREQUENCY



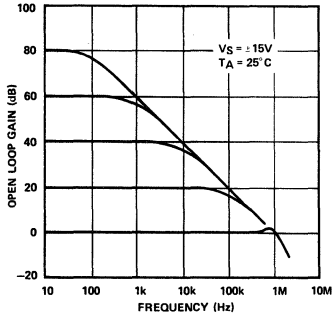
OPEN LOOP GAIN vs POWER SUPPLY VOLTAGE



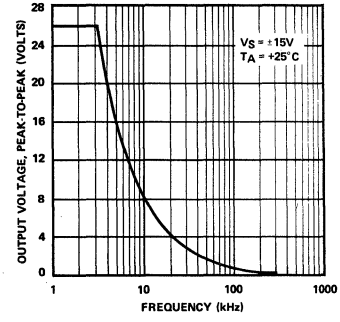
OPEN LOOP FREQUENCY RESPONSE



CLOSED LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS

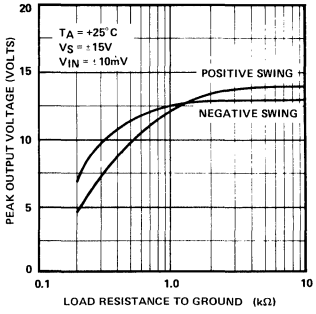


MAXIMUM UNDISTORTED OUTPUT vs FREQUENCY

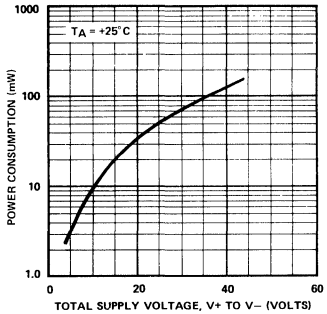


TYPICAL PERFORMANCE CURVES

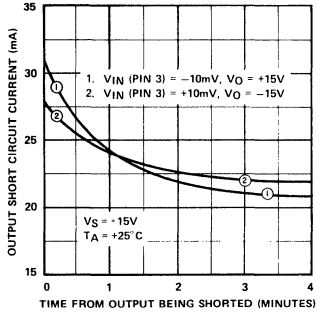
OUTPUT VOLTAGE vs LOAD RESISTANCE



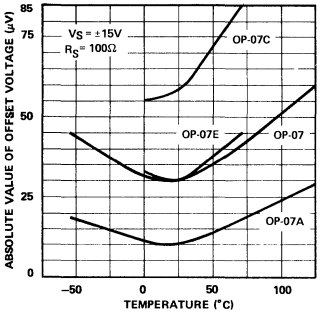
POWER CONSUMPTION vs POWER SUPPLY



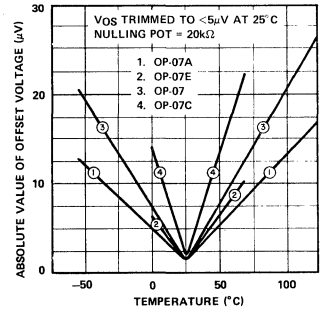
OUTPUT SHORT-CIRCUIT CURRENT vs TIME



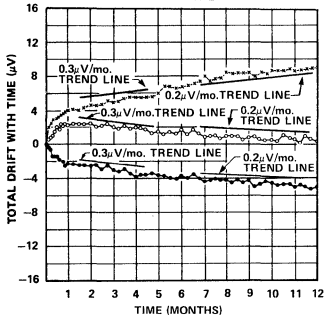
UNTRIMMED OFFSET VOLTAGE vs TEMPERATURE



TRIMMED OFFSET VOLTAGE vs TEMPERATURE

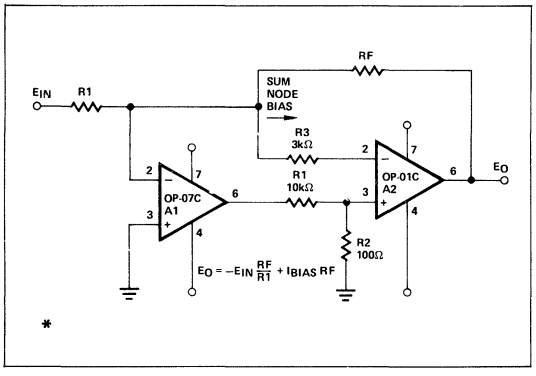


OFFSET VOLTAGE STABILITY vs TIME

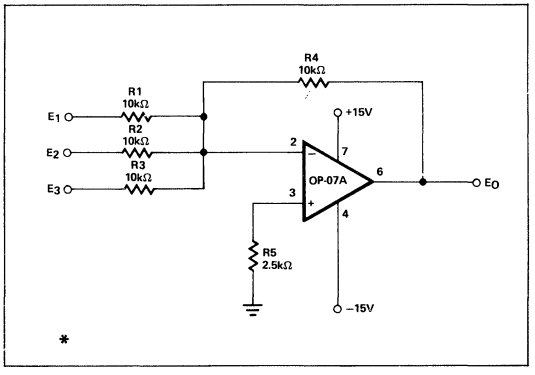


TYPICAL APPLICATIONS

HIGH SPEED, LOW V_{OS} COMPOSITE AMPLIFIER



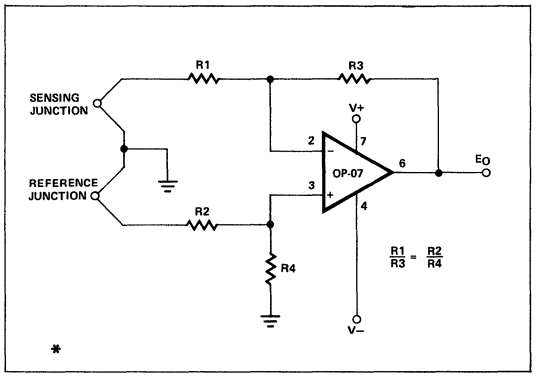
ADJUSTMENT-FREE PRECISION SUMMING AMPLIFIER



*PINOUTS SHOWN FOR J, P AND Z PACKAGES.

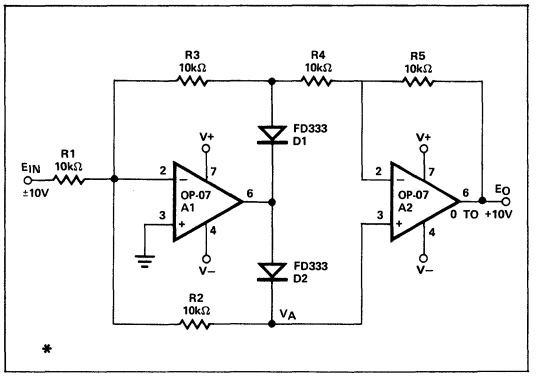
TYPICAL APPLICATIONS

HIGH STABILITY THERMOCOUPLE AMPLIFIER



*PINOUTS SHOWN FOR J, P AND Z PACKAGES.

PRECISION ABSOLUTE VALUE CIRCUIT



APPLICATIONS INFORMATION

OP-07 Series units may be fitted directly to 725, 108A/308A* and OP-05 sockets with or without removal of external compensation or nulling components. Additionally, OP-07 may be fitted to unnulled 741-type sockets; however if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP-07 operation. OP-07 offset voltage may be nulled to zero (or other desired setting) through use of a potentiometer (see offset nulling circuit diagram).

*TO-99 Package only

The OP-07 provides stable operation with load capacitance up to 500pF and ±10V swings; larger capacitances should be decoupled with 50Ω decoupling resistor. The designer is cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

OP-08

PRECISION LOW INPUT CURRENT OPERATIONAL AMPLIFIER

FEATURES

- **Low Offset Voltage ..... 150μV Maximum**
- **Low Offset Voltage Drift ..... 2.5μV/°C Maximum**
- **Five Times PM108A Load Current ..... 5mA Minimum**
- **Low Offset Current ..... 200pA Maximum**
- **Low Bias Current ..... 2.0nA Maximum**
- **Low Power Consumption .... 18mW Maximum @ ±15V**
- **High Common Mode Input Range ... ±13.5V Minimum**
- **MIL-STD-883 Class B Processing Available**
- **Silicon-Nitride Passivation**
- **125° C Temperature Tested Dice**

GENERAL DESCRIPTION

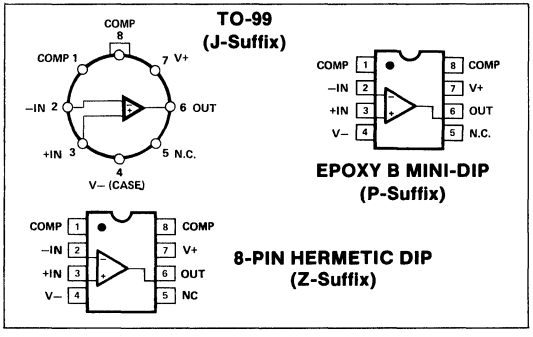
The PMI OP-08 is an improved version of the popular LM108A low power op amp. The OP-08 has a three times lower offset voltage and a two times lower offset voltage drift. The total worst case input offset voltage over −55 °C to +125 °C for the OP-08 is only 350μV, while the 108A has 900μV to 1000μV for these conditions. In addition the OP-08 drives a 2kΩ load. This is five times the output current capability of the 108A. This excellent performance is achieved by applying PMI's ion-implanted super beta process and on-chip-zener-zap trimming capabilities. For devices with identical specifications plus internal frequency compensation, see the OP-12 data sheet.

ORDERING INFORMATION†

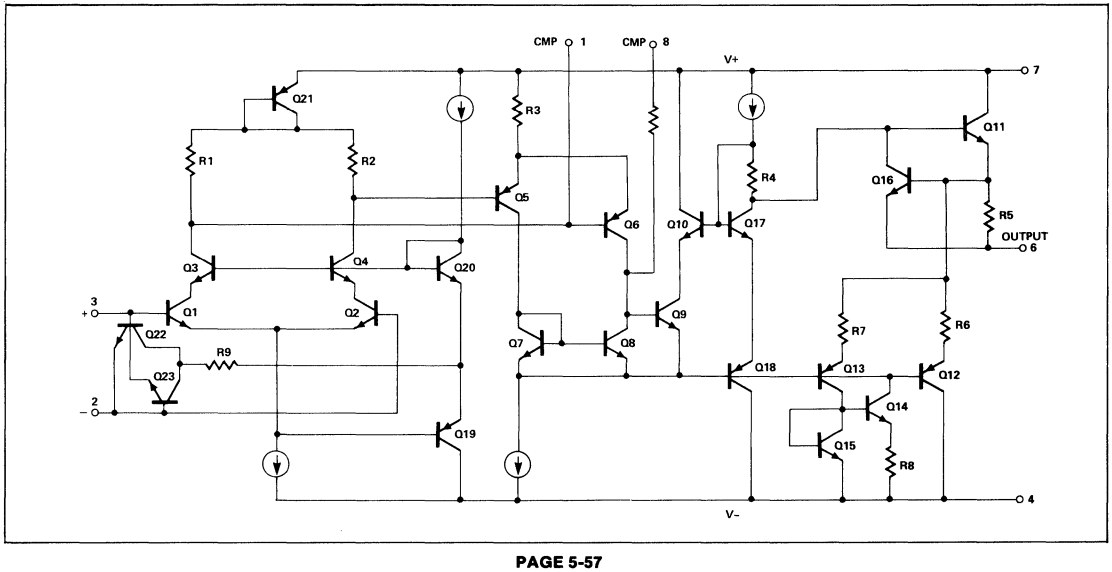
	PACKAGE			
$T_A = 25°C$	HERMETIC		PLASTIC	OPERATING
V_{OS} MAX (mV)	TO-99 8-PIN	DIP 8-PIN	DIP 8-PIN	TEMPERATURE RANGE
0.15	OP08AJ*	OP08AZ*		MIL
0.15	OP08EJ	OP08EZ	OP08EP	COM
0.30	OP08BJ*	OP08BZ*		MIL
0.30	OP08FJ	OP08FZ	OP08FJ	COM
1.0	OP08CJ*	OP08CZ*		MIL
1.0	OP08GJ	OP08GZ	OP08GP	COM

*Also available with MIL-STD-883B processing. To order add /883 as a suffix to the part number.
†All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage
- OP-08A, OP-08B, OP-08E, OP-08F (All DICE except GR) ..... ±20V
- OP-08C, OP-08G (GR DICE Only) ..... ±18V

Internal Power Dissipation (Note 1) 500mW
Differential Input Current (Note 2) ..... ±10mA
Input Voltage (Note 3) ..... ±15V
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range
- OP-08A, OP-08B, OP-08C ..... −55°C to +125°C
- OP-08E, OP-08F, OP-08G ..... 0°C to +70°C

Storage Temperature Range ..... −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec.) ..... 300°C
DICE Junction Temperature (T_j) ..... −65°C to +150°C

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Plastic DIP (P)	36°C	5.6mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C

NOTES:
1. See table for maximum ambient temperature rating and derating factor.
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless, some limiting resistance is provided.
3. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
4. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_S = \pm 20V$ for A, B, E, and F Grades, $V_S = \pm 15V$ for C and G Grades, unless otherwise noted. Compensation capacitor = 30pF.

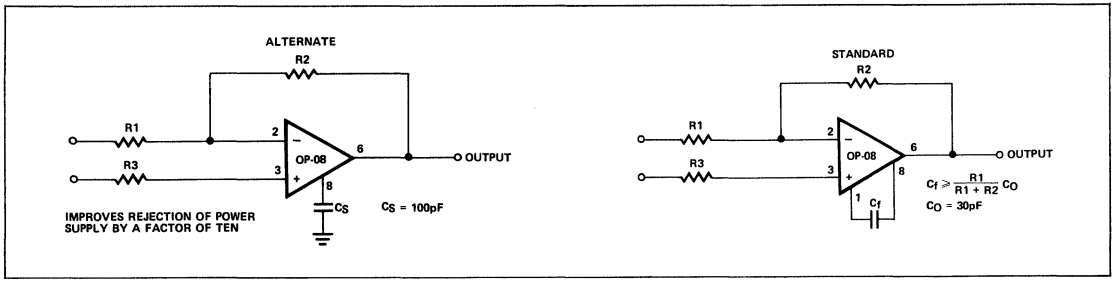
			OP-08A/E			OP-08B/F			OP-08C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.07	0.15	—	0.18	0.30	—	0.25	1.0	mV
Input Offset Current	I_{OS}		—	0.05	0.20	—	0.05	0.20	—	0.08	0.50	nA
Input Bias Current	I_B		—	0.80	2.0	—	0.80	2.0	—	1.0	5.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.9	—	—	0.9	—	—	0.9	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_o = 10Hz$ $f_o = 100Hz$ $f_o = 1000Hz$	— — —	22 21 20	— — —	— — —	22 21 20	— — —	— — —	22 21 20	— — —	$nV/\sqrt{Hz}$
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	3	—	—	3	—	—	3	—	pA_{p-p}
Input Noise Current Density	i_n	$f_o = 10Hz$ $f_o = 100Hz$ $f_o = 1000Hz$	— — —	0.15 0.14 0.13	— — —	— — —	0.15 0.14 0.13	— — —	— — —	0.15 0.14 0.13	— — —	$pA/\sqrt{Hz}$
Input Resistance — Differential Mode	R_{IN}	(Note 1)	26	70	—	26	70	—	10	50	—	MΩ
Input Voltage Range	IVR	$V_S = \pm 15V$	±13.5	±14.0	—	±13.5	±14.0	—	±13.5	±14.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$	104	120	—	104	120	—	84	116	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	—	1	7	—	1	7	—	2	63	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 10k\Omega$, $V_O = \pm 10V$ $R_L \geq 2k\Omega$, $V_O = \pm 10V$, $V_S = \pm 15V$	80 50	300 150	— —	80 50	300 150	— —	40 —	250 100	— —	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$, $V_S = \pm 15V$ $R_L \geq 2k\Omega$, $V_S = \pm 15V$	±13.0 ±10.0	±14.0 ±12.0	— —	±13.0 ±10.0	±14.0 ±12.0	— —	±13.0 ±10.0	±14.0 ±12.0	— —	V
Slewing Rate	SR	$R_L \geq 2k\Omega$	—	0.12	—	—	0.12	—	—	0.12	—	V/μs
Closed Loop Bandwidth	BW	$A_{VCL} = +1.0$	—	0.80	—	—	0.80	—	—	0.80	—	MHz
Open Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	200	—	—	200	—	—	200	—	Ω
Power Consumption	P_d	$V_S = \pm 15V$ $V_S = \pm 5V$	— —	9 3	18 6	— —	9 3	18 6	— —	12 4	24 8	mW

NOTE:
1. Guaranteed by design.

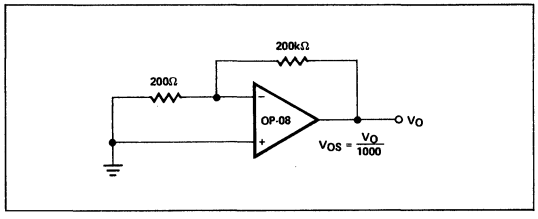
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ for C Grade and $V_S = \pm 20V$ for A or B Grades, $-55°C \le T_A \le +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-08A MIN	OP-08A TYP	OP-08A MAX	OP-08B MIN	OP-08B TYP	OP-08B MAX	OP-08C MIN	OP-08C TYP	OP-08C MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.12	0.35	—	0.28	0.60	—	0.40	2.0	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.50	2.5	—	1.0	3.5	—	1.5	10	μV/°C
Input Offset Current	I_{OS}		—	0.12	0.40	—	0.12	0.40	—	0.18	1.0	nA
Average Input Offset Current Drift	TCI_{OS}		—	0.50	2.5	—	0.50	2.5	—	1.0	5.0	pA/°C
Input Bias Current	I_B		—	1.2	3.0	—	1.2	3.0	—	1.8	10	nA
Input Voltage Range	IVR	$V_S = \pm 15V$	±13.5	±14.0	—	±13.5	±14.0	—	±13.5	±14.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$	100	110	—	100	110	—	80	106	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	—	4	10	—	4	10	—	5	100	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \ge 5k\Omega$, $V_O = \pm 10V$, $V_S = \pm 15V$	40	120	—	40	120	—	15	80	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 10k\Omega$, $V_S = \pm 15V$	±13.0	±14.0	—	±13.0	±14.0	—	±13.0	±14.0	—	V
		$R_L \ge 5k\Omega$, $V_S = \pm 15V$	±10.0	±12.0	—	±10.0	±12.0	—	±10.0	±12.0	—	
Power Consumption	P_d	$V_S = \pm 15V$	—	9	18	—	9	18	—	15	24	mW

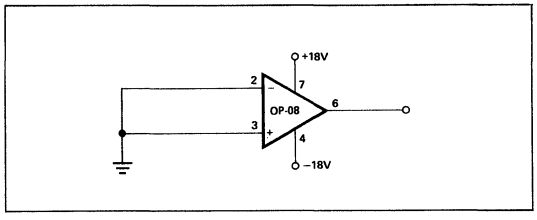
COMPENSATION CIRCUITS



OFFSET VOLTAGE TEST CIRCUIT



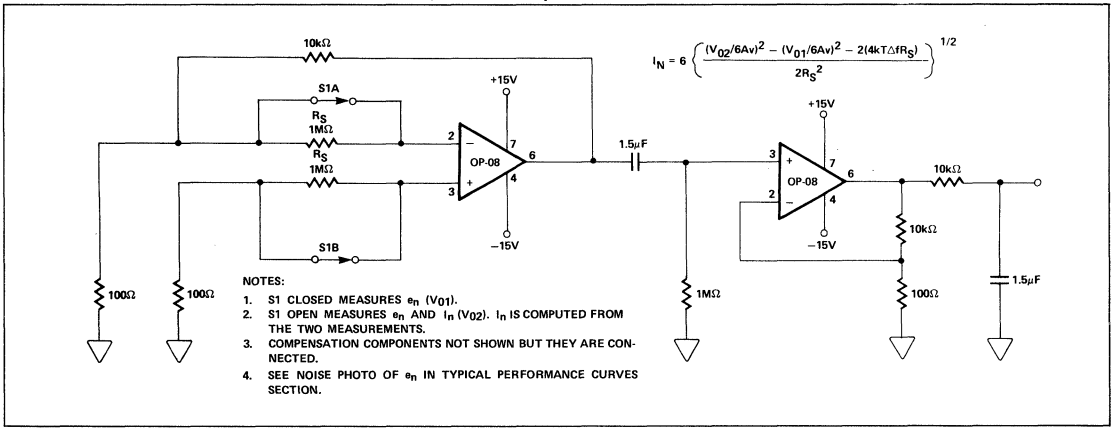
BURN-IN CIRCUIT



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ for G Grade and $V_S = \pm 20V$ for E or F Grades, $0° C \leq T_A \leq +70° C$, unless otherwise noted.

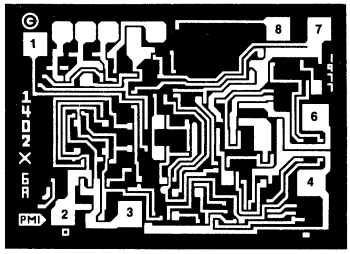
PARAMETER	SYMBOL	CONDITIONS	OP-08E MIN	OP-08E TYP	OP-08E MAX	OP-08F MIN	OP-08F TYP	OP-08F MAX	OP-08G MIN	OP-08G TYP	OP-08G MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.10	0.26	—	0.23	0.45	—	0.32	1.4	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.50	2.5	—	1.0	3.5	—	1.5	10	μV/°C
Input Offset Current	I_{OS}		—	0.08	0.30	—	0.11	0.60	—	0.12	6.5	nA
Average Input Offset Current Drift	TCI_{OS}		—	0.50	2.5	—	1.0	5.0	—	2.0	50.0	pA/°C
Input Bias Current	I_B		—	1.0	2.6	—	1.2	5.2	—	1.4	6.5	nA
Input Voltage Range	IVR	$V_S = \pm 15V$	±13.5	±14.0	—	±13.5	±14.0	—	±13.5	±14.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$	100	116	—	100	116	—	80	112	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	—	2	10	—	2	10	—	3	100	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	25	100	—	25	100	—	—	80	—	V/mV
		$R_L \geq 10k\Omega$ $V_O = \pm 10V$ $V_S = \pm 15V$	60	200	—	60	200	—	25	150	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $V_S = \pm 15V$	±13.0	±14.0	—	±13.0	±14.0	—	±13.0	±14.0	—	V
		$R_L \geq 2k\Omega$, $V_S = \pm 15V$	±10.0	±12.0	—	±10.0	±12.0	—	±10.0	±12.0	—	
Power Consumption	P_d	$V_S = \pm 15V$	—	9	18	—	9	18	—	15	24	mW

LOW FREQUENCY NOISE TEST CIRCUIT (0.1 to 10Hz)



NOTES:
1. S1 CLOSED MEASURES e_n (V_{01}).
2. S1 OPEN MEASURES e_n AND I_n (V_{02}). I_n IS COMPUTED FROM THE TWO MEASUREMENTS.
3. COMPENSATION COMPONENTS NOT SHOWN BUT THEY ARE CONNECTED.
4. SEE NOISE PHOTO OF e_n IN TYPICAL PERFORMANCE CURVES SECTION.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



DIE SIZE 0.058 × 0.042 inch

1. COMPENSATION
2. INVERTING INPUT
3. NON-INVERTING INPUT
4. V−
6. OUTPUT
7. V+
8. COMPENSATION

Refer to Section 2 for additional DICE information

ELECTRICAL CHARACTERISTICS at $V_S = \pm 20V$ and $T_A = +25°C$ for OP-08N and OP-08G, $V_S = \pm 20V$ and $T_A = +125°C$ for OP-08NT and OP-08GT, $V_S = \pm 15V$ and $T_A = +25°C$ for OP-08GR, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-08NT LIMIT	OP-08N LIMIT	OP-08GT LIMIT	OP-08G LIMIT	OP-08GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		0.35	0.3	0.60	0.5	1.0	mV MAX
Input Offset Current	I_{OS}		0.2	0.2	0.4	0.4	0.5	nA MAX
Input Bias Current	I_B		2.0	2.0	4.0	4.0	5.0	nA MAX
Input Voltage Range	IVR	$V_S = \pm 15V$	±13.5	±13.5	±13.5	±13.5	±13.5	V MIN
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$ $V_S = \pm 15V$	100	104	100	104	84	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	10	7	10	7	63	μV/V MAX
Output Voltage Swing	V_O	$V_S = \pm 15V$ $R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 5k\Omega$	±13 — ±10	±13 ±10 —	±13 — ±10	±13 ±10 —	±13 ±10 —	V MIN
Large Signal Voltage Gain ($V_O = \pm 10V$)	A_{VO}	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$, $V_S = \pm 15V$ $R_L \geq 5k\Omega$, $V_S = \pm 15V$	— — 40	80 50 —	— — 40	80 50 —	40 — —	V/mV MIN
Input Resistance	R_{IN}	(Note 2)	—	25	—	25	10	mΩ MIN
Supply Current	I_{SY}	$I_{OUT} = 0$, $V_S = \pm 15V$ $V_{OUT} = 0$	0.6	0.6	0.6	0.6	0.8	mA MAX

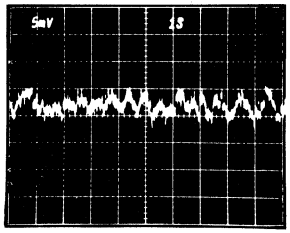
NOTES:
1. For 25° C characteristics of NT & GT devices, see N & G characteristics, respectively.
2. Guaranteed by design.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-08NT TYPICAL	OP-08N TYPICAL	OP-08GT TYPICAL	OP-08G TYPICAL	OP-08GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}		0.5	0.5	1.0	1.0	1.5	μV/° C
Average Input Offset Current Drift	TCI_{OS}		0.5	0.5	0.5	0.5	1.0	pA/° C

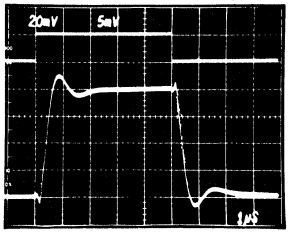
TYPICAL PERFORMANCE CURVES

LOW FREQUENCY NOISE

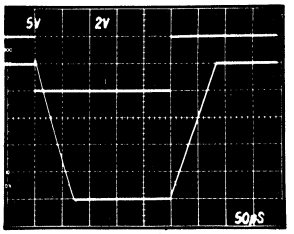


R_S = 0, BW = 0.1Hz to 10Hz
5mV/div AT READOUT
0.5μV/div REFERRED TO INPUT

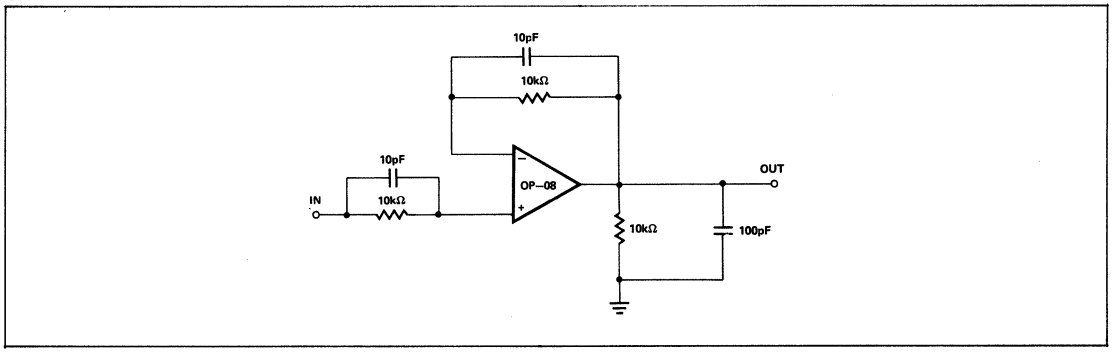
SMALL SIGNAL TRANSIENT RESPONSE



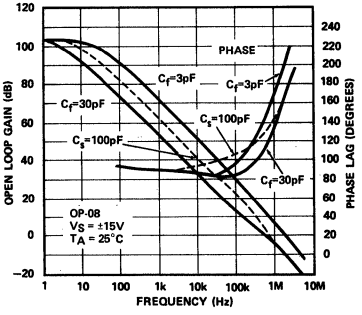
LARGE SIGNAL TRANSIENT RESPONSE



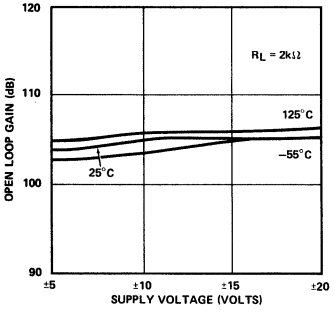
TRANSIENT RESPONSE TEST CIRCUIT



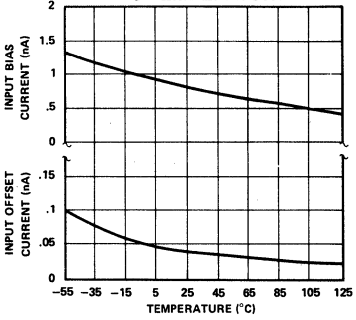
OPEN LOOP GAIN AND PHASE vs FREQUENCY



OPEN LOOP GAIN vs SUPPLY VOLTAGE

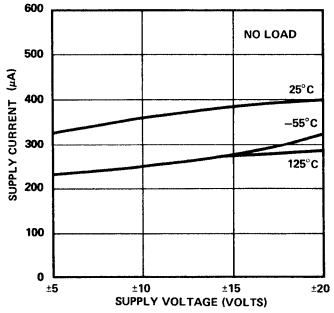


INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs TEMPERATURE

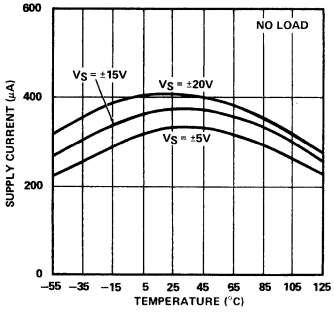


TYPICAL PERFORMANCE CURVES

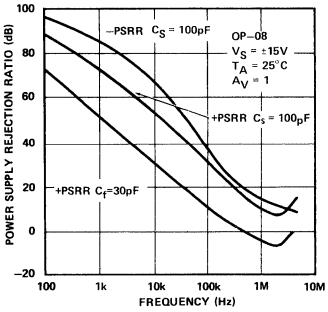
SUPPLY CURRENT vs SUPPLY VOLTAGE



SUPPLY CURRENT vs TEMPERATURE



POWER SUPPLY REJECTION RATIO (PSRR) vs FREQUENCY

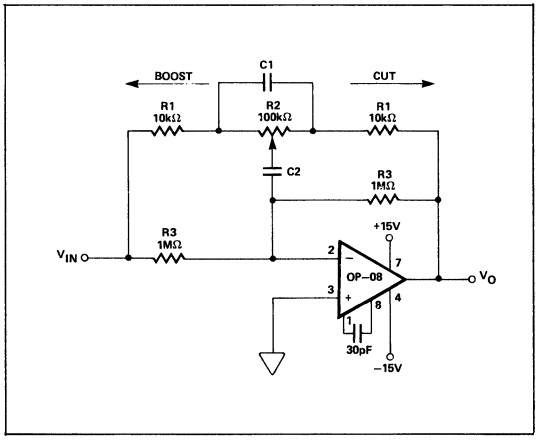


APPLICATIONS INFORMATION

The OP-08 series has extremely low input offset and bias currents; the user is cautioned that stray printed circuit board leakages can produce significant errors, especially at high board temperatures. Careful attention to board layout and cleaning procedure is required to fully realize the OP-08 performance. It is suggested that effects of board leakage be minimized by encircling the input pins with a conductive guard ring operated at a potential close to that of the inputs. This guard ring should be driven by a low impedance source, such as the amplifier's output for non-inverting circuits or ground for inverting circuits.

TYPICAL APPLICATIONS

OCTAVE EQUALIZER

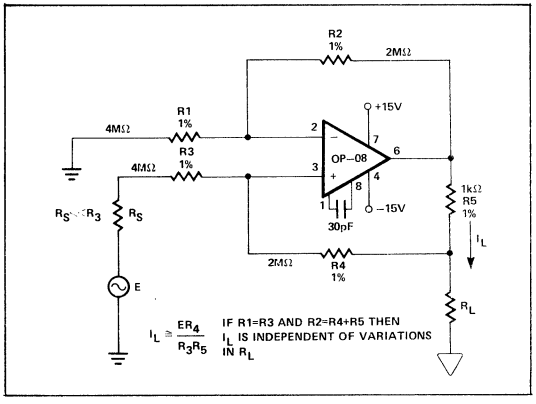


The above circuit is one section of an octave equalizer used in audio systems. The table shows the values of C_1 and C_2 needed to achieve the given center frequencies. This circuit is capable of 12dB boost or cut as determined by the position of R2.

f_o (Hz)	C_1	C_2
32	0.18μF	0.018μF
64	0.1μF	0.01μF
125	0.047μF	0.0047μF
250	0.022μF	0.0022μF
500	0.012μF	0.0012μF
1k	0.0056μF	560pF
2k	0.0027μF	270pF
4k	0.0015μF	150pF
8k	680pF	68pF
16k	360pF	36pF

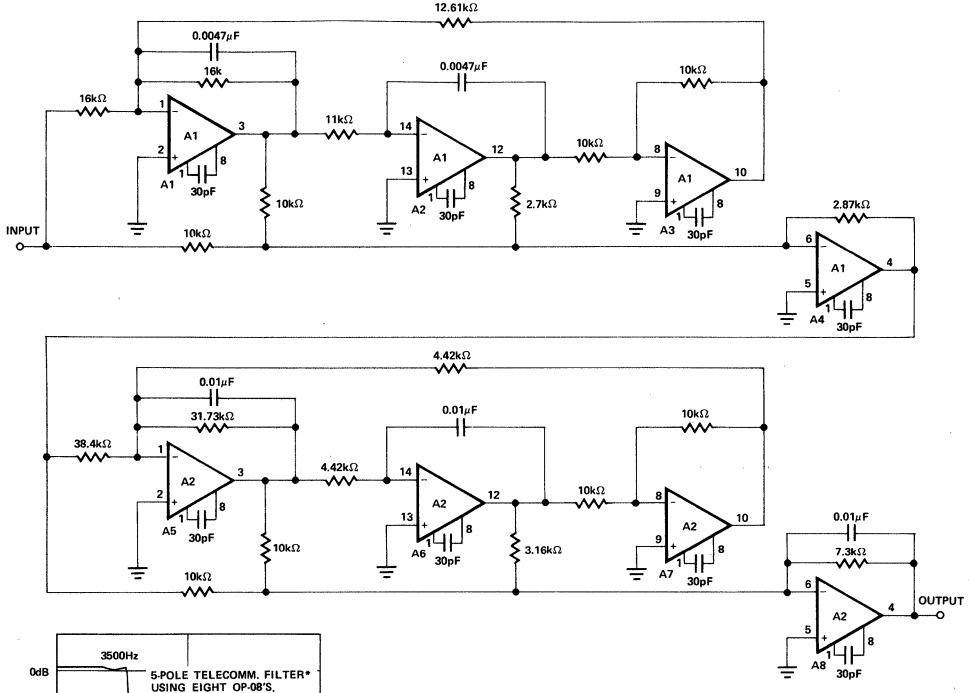
Because of the low input bias current of the OP-08 the resistors could be scaled up by a factor of ten, and thereby reduce the values of C_1 and C_2 at the low frequency end. In addition ten sections as shown above will only draw a combined supply current of 6mA maximum.

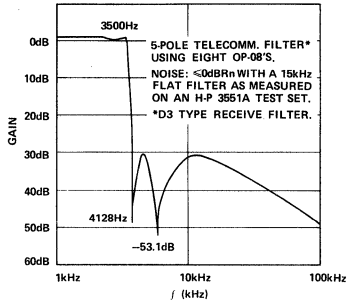
BILATERAL CURRENT SOURCE



The bilateral current source circuit shown on the previous page will produce the indicated current relationship to within 2% using 1% values for R1 through R5. This includes variations in R_L from 100Ω to 2000Ω. The use of large resistors for R1 through R4 minimizes the error due to R_L variations. The large resistors are possible because of the excellent input bias current performance of the OP-08.

5-POLE ACTIVE FILTER





The above realization of a type D3 receive filter is accomplished using eight OP-08's. As can be seen from the response curve, the >30dB attenuation in the stop band requirement has been met. In addition, the noise performance of <0dBRn has been measured. One of the unique features of the OP-08 is its low supply current of 600μA maximum. Thus the total supply drain for all eight op amps is only 4.8mA.

OP-09/OP-11

QUAD MATCHED 741-TYPE OPERATIONAL AMPLIFIER

FEATURES

- **Guaranteed V_{OS} ..... 500μV Maximum**
- **Guaranteed Matched CMRR ..... 94dB Minimum**
- **Guaranteed Matched V_{OS} ..... 750μV Maximum**
- **RC/RM4136 Direct Replacement (OP-09)**
- **LM148/LM348 and RC/RM4156 Direct Replacement (OP-11)**
- **Low Noise**
- **Silicon-Nitride Passivation**
- **Internal Frequency Compensation**
- **Low Crossover Distortion**
- **Continuous Short Circuit Protection**
- **Low Input Bias Current**

GENERAL DESCRIPTION

The OP-09 and OP-11 provide four matched 741-type operational amplifiers in a single 14-pin DIP package. The OP-11 is pin compatible with the LM148, LM348, RM4156, and HA4741 amplifiers. The OP-09 is pin compatible with the RM4136 and RC4136. The amplifiers are matched for common mode rejection ratio and offset voltage. These parameters are very important in the design of instrumentation amplifiers. In addition the amplifier is designed to have equal positive-going and negative-going slew rates. This is a very important consideration for good audio system performance.

Each of the four amplifiers has the proven OP-02 advantages of low noise, low drift and excellent long-term stability. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process reduces "popcorn noise" and provides maximum reliability and long-term stability of parameters for lowest overall system operating cost.

The OP-09 and OP-11 are ideal for use in designs requiring minimum space and cost while maintaining OP-02-type performance.

OP-09's and OP-11's with processing per the requirements of MIL-STD-883 are available. For dual-741-type versions, see the OP-03, OP-04 and OP-14 data sheets.

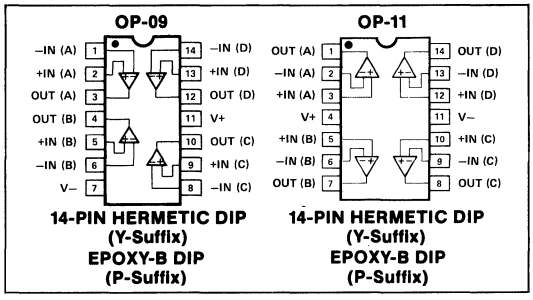
ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (mV)	HERMETIC DIP 14-PIN	EPOXY-B DIP 14-PIN	OPERATING TEMPERATURE RANGE
0.5	OP-09AY* OP-11AY*		MIL
0.5	OP-09EY OP-11EY		COM
2.5	OP-09BY* OP-11BY*		MIL
2.5	OP-09FY OP-11FY	OP-09FP OP-11FP	COM
5.0	OP-09CY* OP-11CY*		MIL
5.0	OP-09GY OP-11GY	OP-09GP OP-11GP	COM

* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

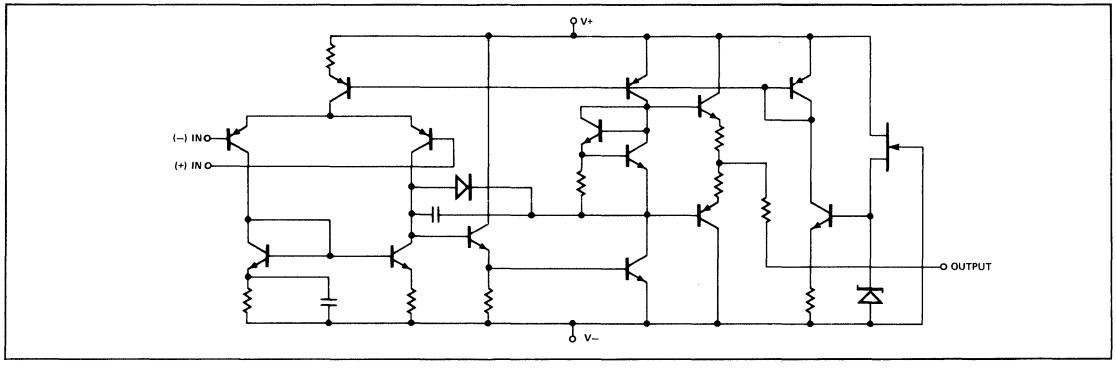
PIN CONNECTIONS



14-PIN HERMETIC DIP (Y-Suffix) EPOXY-B DIP (P-Suffix)

14-PIN HERMETIC DIP (Y-Suffix) EPOXY-B DIP (P-Suffix)

SIMPLIFIED SCHEMATIC (One of Four Amplifiers is Shown)



ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±22V
OP-09GR and OP-11GR (Only) ..... ±18V
Internal Power Dissipation (Note 1)
Y-Package 800mW
P-Package 500mW
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply Voltage
Output Short Circuit Duration ..... Continuous
(One Amplifier Only)
Storage Temperature Range
Y-Package ..... −65°C to +150°C
P-Package ..... −65°C to +125°C
Lead Temperature Range (Soldering, 60 sec.) ..... 300°C
DICE Junction Temperature (T_j) ..... −65°C to +150°C

Operating Temperature Range
OP-09A, OP-09B, OP-09C ..... −55°C to +125°C
OP-09E, OP-09F, OP-09G ..... 0°C to +70°C
OP-11A, OP-11B, OP-11C ..... −55°C to +125°C
OP-11E, OP-11F, OP-11G ..... 0°C to +70°C

NOTES:
1. See table for maximum ambient temperature and derating factor.

	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	70°C	10.0mW/°C
14-Pin Plastic DIP (P)	42°C	6mW/°C

2. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, $R_S \leq 100\Omega$, unless otherwise noted.

			OP-09A, OP-09E OP-11A, OP-11E			OP-09B, OP-09F OP-11B, OP-11F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	0.5	0.75	—	0.8	2.0	mV
Common Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 12V$ $V_{CM} = \pm 12V$	— 94	1.0 120	20 —	— 94	1.0 120	20 —	μV/V dB

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ for OP-09A, OP-09B, OP-11A and OP-11B, $0°C \leq T_A \leq +70°C$ for OP-09E, OP-09F, OP-11E and OP-11F, $R_S \leq 100\Omega$, unless otherwise noted.

			OP-09A, OP-09E OP-11A, OP-11E			OP-09B, OP-09F OP-11B, OP-11F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	0.6	1.0	—	1.0	2.5	mV
Common Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 12V$ $V_{CM} = \pm 12V$	— 94	3.2 110	20 —	— 94	3.2 110	20 —	μV/V dB

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09A/E OP-11A/E MIN	TYP	MAX	OP-09B/F OP-11B/F MIN	TYP	MAX	OP-09C/G OP-11C/G MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	0.30	0.50	—	0.60	2.5	—	1.2	5.0	mV
Input Offset Current	I_{OS}		—	5.5	20	—	25	50	—	75	200	nA
Input Bias Current	I_B		—	180	300	—	300	500	—	300	500	nA
Input Resistance Differential Mode	R_{IN}	(Note 3)	0.20	0.40	—	0.20	0.40	—	0.20	0.40	—	MΩ
Input Voltage Range	IVR		±12	±13	—	±12	±13	—	±12	±13	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V$, $R_S \leq 10k\Omega$	100	120	—	100	120	—	70	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 15V$, $R_S \leq 10k\Omega$	—	4	32	—	4	32	—	10	100	μV/V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±11	±13	—	±11	±13	—	±11	±13	—	V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	100	650	—	100	650	—	50	500	—	V/mV
Power Consumption (Note 1)	P_d	$V_O = 0V$	—	105	180	—	123	180	—	210	340	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.7	—	—	0.7	—	—	0.7	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_o = 10Hz$ $f_o = 100Hz$ $f_o = 1000Hz$	— — —	18 14 12	— — —	— — —	18 14 12	— — —	— — —	18 14 12	— — —	$nV/\sqrt{Hz}$
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	17	—	—	17	—	—	17	—	pA_{p-p}
Channel Separation	CS		100	130	—	100	130	—	—	130	—	dB
Input Noise Current Density	i_n	$f_o = 10Hz$ $f_o = 100Hz$ $f_o = 1000Hz$	— — —	1.8 1.5 1.2	— — —	— — —	1.8 1.5 1.2	— — —	— — —	1.8 1.5 1.2	— — —	$pA/\sqrt{Hz}$
Slew Rate (Note 3)	SR		0.70	1.0	—	0.70	1.0	—	0.70	1.0	—	V/μs
Large Signal Bandwidth (Note 3)		$V_O = 20V_{p-p}$	11	16	—	11	16	—	11	16	—	kHz
Closed Loop Bandwidth (Note 3)	BW	$A_{VCL} = +1.0$	1.5	2.0	—	1.5	2.0	—	1.5	2.0	—	MHz
Risetime (Note 2)	t_r	$A_V = +1$, $V_{IN} = 50mV$	—	80	120	—	80	120	—	80	120	ns
Overshoot (Note 2)	O_S		—	15	25	—	15	25	—	15	25	%

NOTES:

1. Total dissipation for all four amplifiers in package.
2. Sample tested.
3. Guaranteed by design.

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

			OP-09A OP-11A			OP-09B OP-11B			OP-09C OP-11C			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	0.40	1.0	—	1.0	3.5	—	1.5	6.0	mV
Average Input Offset Voltage Drift (Note 2)	TCV_{OS}	$R_S \leq 10k\Omega$	—	2.0	10	—	4.0	15	—	4.0	—	µV/°C
Input Offset Current	I_{OS}		—	20	40	—	40	80	—	250	300	nA
Average Input Offset Current Drift (Note 2)	TCI_{OS}		—	0.10	0.30	—	0.30	0.60	—	0.30	0.60	nA/°C
Input Bias Current	I_B		—	200	375	—	400	650	—	400	800	nA
Input Voltage Range	IVR		±12	±13	—	±12	±13	—	±12	±13	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V$, $R_S \leq 10k\Omega$	100	120	—	100	120	—	70	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 15V$, $R_S \leq 10k\Omega$	—	4	32	—	4	32	—	10	100	µV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	50	250	—	50	250	—	25	100	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±11	±13	—	±11	±13	—	±11	±13	—	V
Power Consumption (Note 1)	P_d	$V_O = 0V$	—	115	200	—	115	200	—	250	400	mW

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $0° C \leq T_A \leq +70° C$, unless otherwise noted.

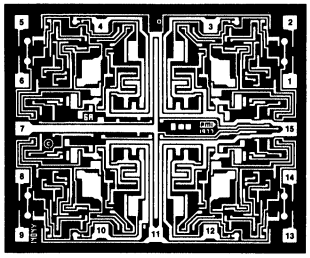
			OP-09E OP-11E			OP-09F OP-11F			OP-09G OP-11G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	0.40	0.8	—	0.8	3.0	—	1.5	6.0	mV
Average Input Offset Voltage Drift (Note 2)	TCV_{OS}	$R_S \leq 10k\Omega$	—	2.0	10	—	4.0	15	—	4.0	—	µV/°C
Input Offset Current	I_{OS}		—	14	30	—	40	60	—	250	300	nA
Average Input Offset Current Drift (Note 2)	TCI_{OS}		—	0.10	0.30	—	0.30	0.60	—	0.30	0.60	nA/°C
Input Bias Current	I_B		—	200	350	—	400	550	—	400	800	nA
Input Voltage Range	IVR		±12	±13	—	±12	±13	—	±12	±13	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V$, $R_S \leq 10k\Omega$	100	120	—	100	120	—	70	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 15V$, $R_S \leq 10k\Omega$	—	4	32	—	4	32	—	10	100	µV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	50	250	—	50	250	—	25	100	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±11	±13	—	±11	±13	—	±11	±13	—	V
Power Consumption (Note 1)	P_d	$V_O = 0V$	—	115	200	—	115	200	—	250	400	mW

NOTES:

1. Total dissipation for all four amplifiers in package.
2. Sample tested.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)

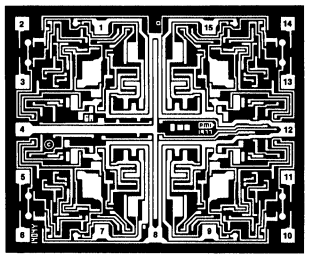
OP-09



DIE SIZE 0.085 × 0.070 inch

1. INVERTING INPUT (A)
2. NON-INVERTING INPUT (A)
3. OUTPUT (A)
4. OUTPUT (B)
5. NON-INVERTING INPUT (B)
6. INVERTING INPUT (B)
7. V−
8. INVERTING INPUT (C)
9. NON-INVERTING INPUT (C)
10. OUTPUT (C)
11. V+
12. OUTPUT (D)
13. NON-INVERTING INPUT (D)
14. INVERTING INPUT (D)
15. V+

OP-11



DIE SIZE 0.085 × 0.070 inch

1. OUTPUT (A)
2. INVERTING INPUT (A)
3. NON-INVERTING INPUT (A)
4. V−
5. NON-INVERTING INPUT (B)
6. INVERTING INPUT (B)
7. OUTPUT (B)
8. V+
9. OUTPUT (C)
10. INVERTING INPUT (C)
11. NON-INVERTING INPUT (C)
12. V+
13. NON-INVERTING INPUT (D)
14. INVERTING INPUT (D)
15. OUTPUT (D)

NOTE:
Either or both V+ pads may be used without any change in performance.

See Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$ for OP-09/11N, OP-09/11G and OP-09/11GR devices, $T_A = +125°C$ for OP-09/11NT and OP-09/11GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09NT OP-11NT LIMIT	OP-09N OP-11N LIMIT	OP-09GT OP-11GT LIMIT	OP-09G OP-11G LIMIT	OP-09GR OP-11GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	1.0	0.5	3.5	2.5	5.0	mV MAX
Input Offset Current	I_{OS}		20	20	50	50	200	nA MAX
Input Bias Current	I_B		300	300	500	500	500	nA MAX
Input Voltage Range	IVR		±12	±12	±12	±12	±12	V MIN
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V$ $R_S \leq 10k\Omega$	100	100	100	100	70	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$ $R_S \leq 10k\Omega$	32	32	32	32	100	µV/V MAX
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L = 2k\Omega$	±11 ±11	±12 ±11	±11 ±11	±12 ±11	±11 ±11	V MIN
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	50	100	50	V/mV MIN
Power Consumption (Four Amplifiers)	P_D	$V_{OUT} = 0$ No Load	200	180	200	180	340	mW MAX

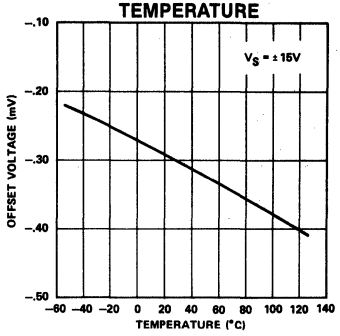
NOTE: For 25° C characteristics of NT & GT devices, see N & G characteristics, respectively.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

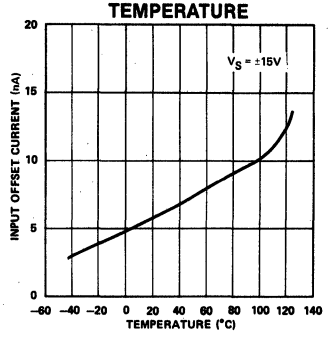
PARAMETER	SYMBOL	CONDITIONS	OP-09NT OP-11NT TYP	OP-09N OP-11N TYP	OP-09GT OP-11GT TYP	OP-09G OP-11G TYP	OP-09GR OP-11GR TYP	UNITS
Slew Rate	SR	$A_V = 1$ $R_L \geq 2k\Omega$	1.0	1.0	1.0	1.0	1.0	V/µs
Unity Gain Bandwidth	GBW		2.0	2.0	2.0	2.0	2.0	MHz
Channel Separation	CS	$A_V = 100$ $f = 10kHz$ $R_S = 1k\Omega$	130	130	130	130	130	dB

TYPICAL PERFORMANCE CURVES

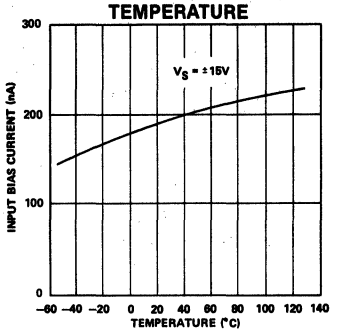
OFFSET VOLTAGE vs TEMPERATURE



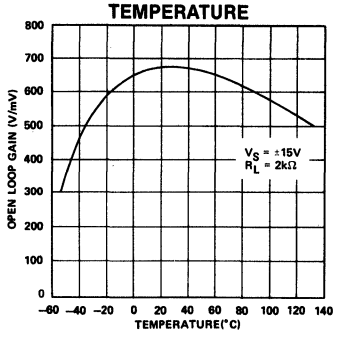
OFFSET CURRENT vs TEMPERATURE



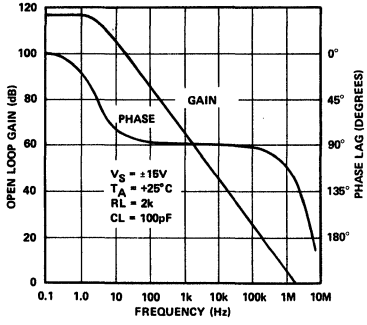
BIAS CURRENT vs TEMPERATURE



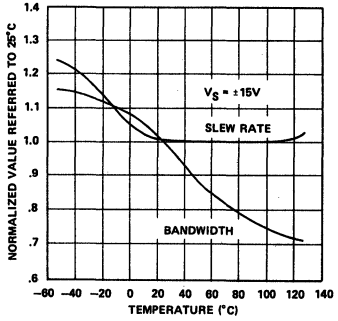
OPEN LOOP GAIN vs TEMPERATURE



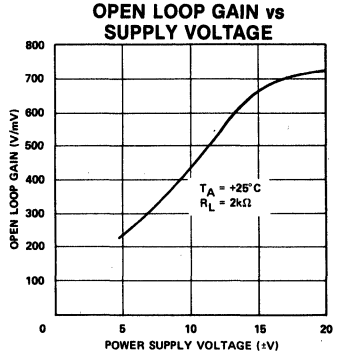
OPEN LOOP FREQUENCY AND PHASE RESPONSE



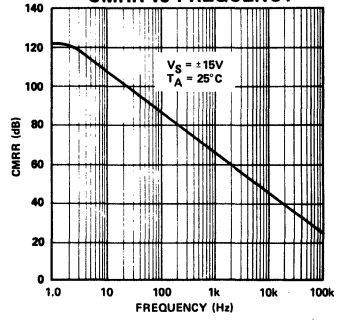
NORMALIZED A/C PARAMETERS vs TEMPERATURE



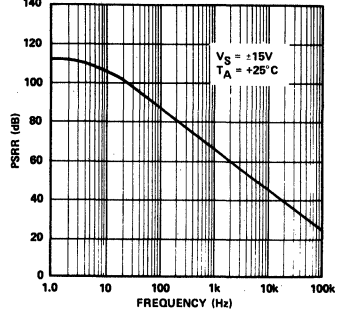
OPEN LOOP GAIN vs SUPPLY VOLTAGE



CMRR vs FREQUENCY

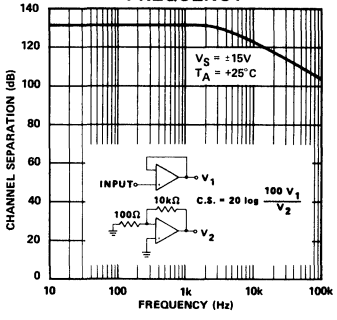


PSRR vs FREQUENCY

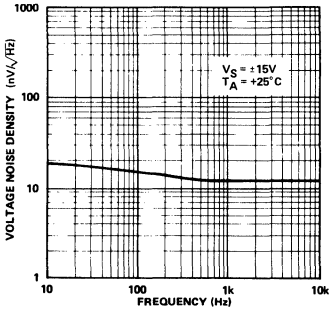


TYPICAL PERFORMANCE CURVES

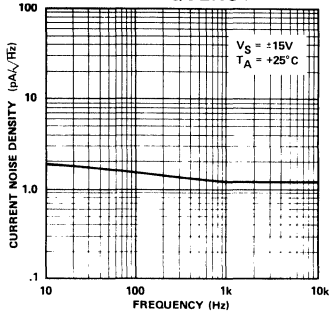
CHANNEL SEPARATION vs FREQUENCY



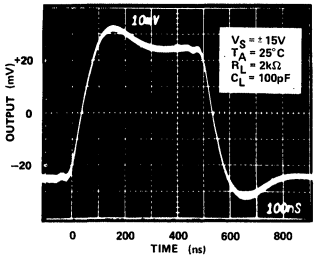
NOISE VOLTAGE DENSITY vs FREQUENCY



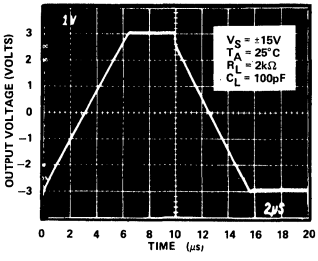
NOISE CURRENT DENSITY vs FREQUENCY



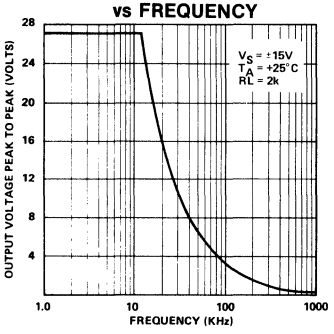
TRANSIENT RESPONSE



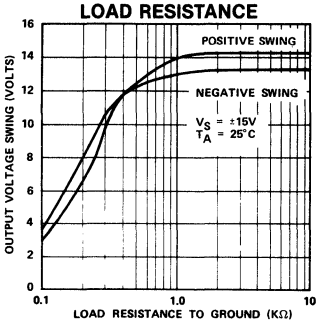
VOLTAGE FOLLOWER PULSE RESPONSE



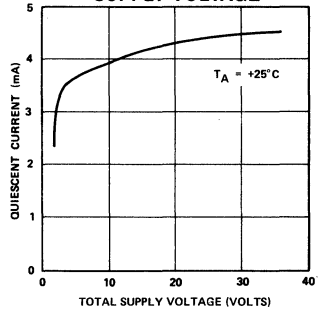
MAX UNDISTORTED OUTPUT vs FREQUENCY



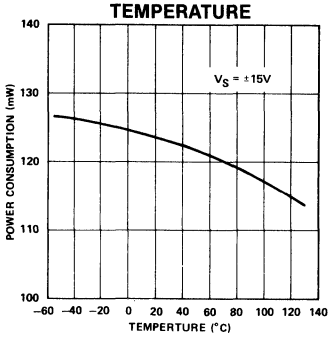
OUTPUT VOLTAGE vs LOAD RESISTANCE



QUIESCENT CURRENT vs SUPPLY VOLTAGE

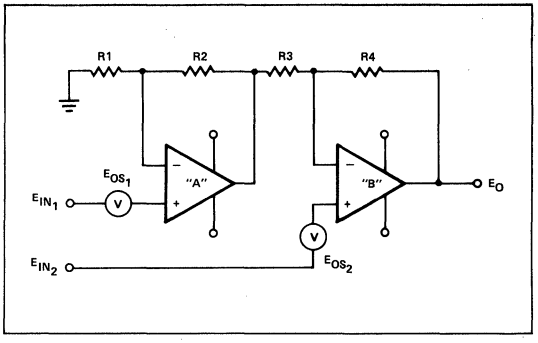


POWER CONSUMPTION vs TEMPERATURE



APPLICATION INFORMATION

INSTRUMENTATION AMPLIFIER TWO OP-AMP DESIGN



This device eliminates the need for special op amp selections in many instrumentation amplifier applications.

GENERAL DESIGN CONSIDERATIONS

Assuming ideal amplifiers, the expression for output voltage is:

$$1)\ E_o = E_{in1}\left(1 + \frac{R_2}{R_1}\right)\left(-\frac{R_4}{R_3}\right) + E_{in2}\left(1 + \frac{R_4}{R_3}\right)$$

With ideal resistors this simplifies to:

$$2)\ E_o = \left(E_{in2} - E_{in1}\right)\left(1 + \frac{R_4}{R_3}\right) \quad \text{provided } \frac{R_1}{R_2} = \frac{R_4}{R_3}$$

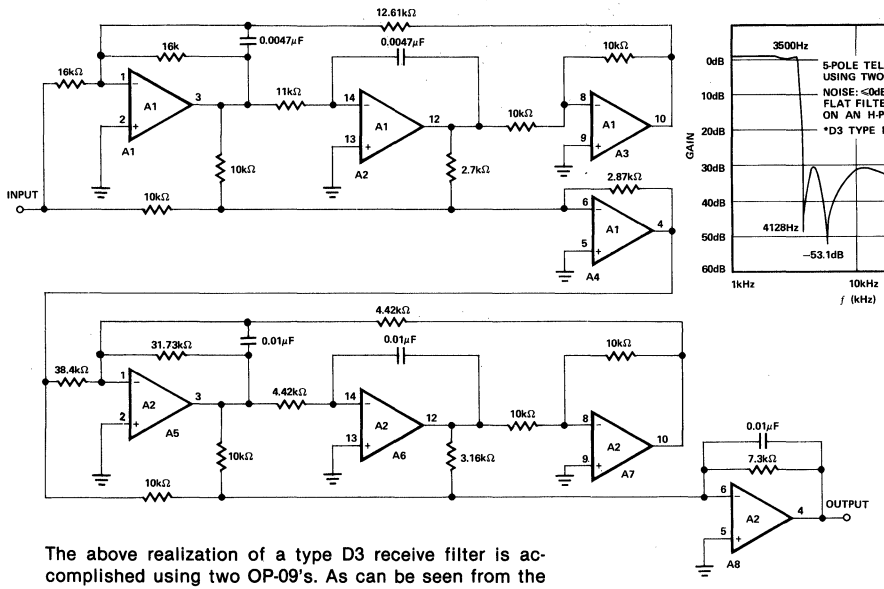
COMMON MODE REJECTION

Because the dual op amp has a high common mode rejection ratio match, the ability to reject common mode inputs becomes primarily a function of resistor ratio matching.

DIFFERENTIAL OFFSET VOLTAGE

The amplifier's differential input offset voltage ($E_{os2} - E_{os1}$) will be the major error factor. If the individual input offset voltages are of equal magnitude and polarity they appear as a common mode input and are rejected.

FIVE POLE ACTIVE FILTER

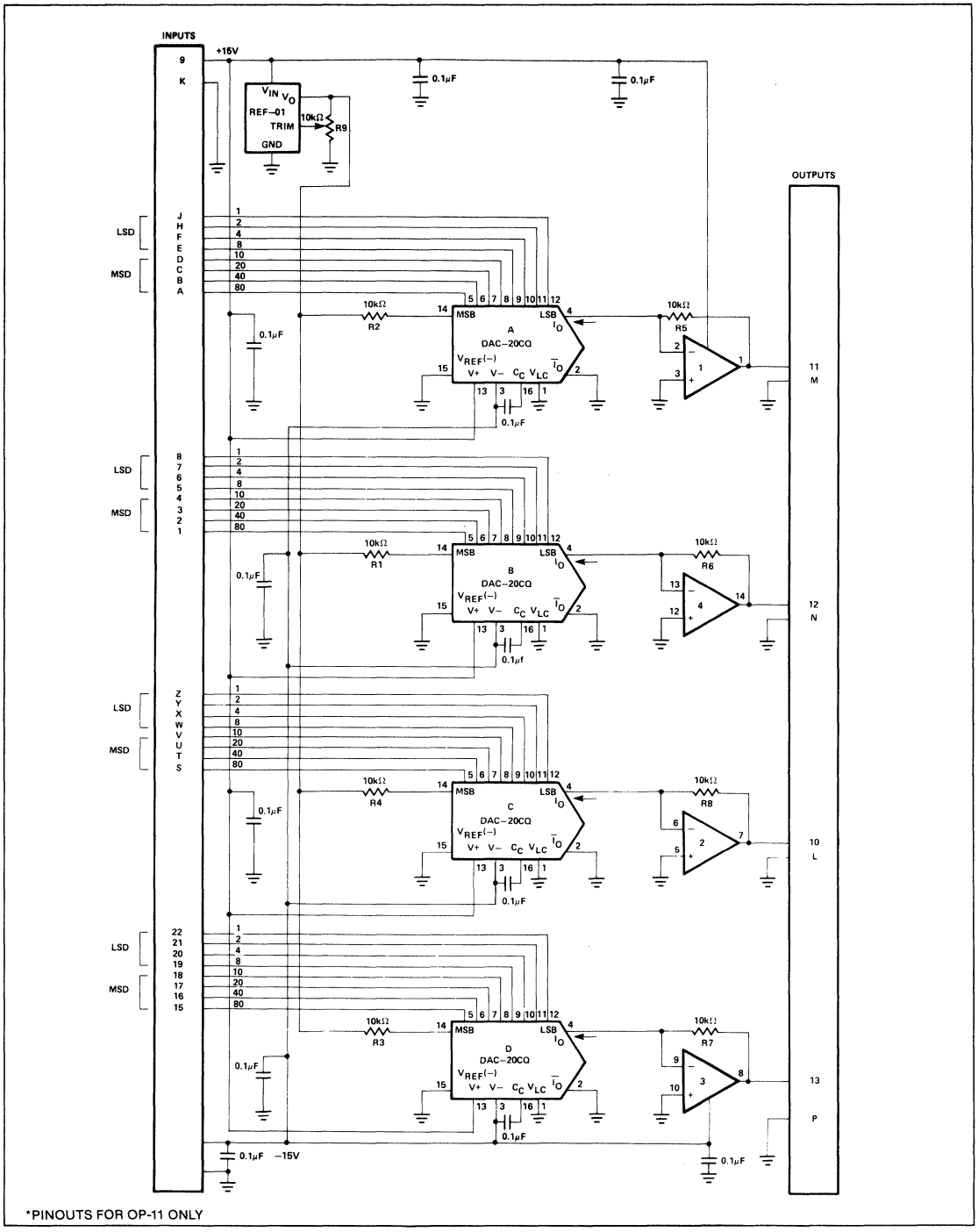


The above realization of a type D3 receive filter is accomplished using two OP-09's. As can be seen from the response curve, the >30dB attenuation in the stop band requirement has been met. In addition, the noise performance of <0dBRn has been measured. The maximum supply drain for the entire filter is only 12mA.

*PINOUTS FOR OP-09 ONLY

TYPICAL APPLICATION

FOUR-CHANNEL D/A OUTPUT AMPLIFIER



OP-10

DUAL-MATCHED INSTRUMENTATION OPERATIONAL AMPLIFIER

FEATURES

- **Extremely Tight Matching**
- **Excellent Individual Amplifier Parameters**
- **Tight Offset Voltage Match** ..... **0.18mV Max**
- **Tight Offset Voltage Match vs Temp.** ..... **0.8μV/°C Max**
- **Tight Common Mode Rejection Match** ..... **114dB Min**
- **Tight Power Supply Rejection Match** ..... **100 dB Min**
- **Tight Bias Current Match** ..... **3.0nA Max**
- **Low Noise** ..... **0.6μV_{p-p} Max**
- **Low Bias Current** ..... **3.0nA Max**
- **High Common Mode Input Impedance** ..... **200GΩ Typ**
- **High Channel Separation** ..... **126dB Min**
- **Internally Compensated** ..... **Easy to Use**
- **Compact** ..... **14-Pin Dip Package**

GENERAL DESCRIPTION

The OP-10 Series of Dual-Matched Instrumentation Operational Amplifiers consists of two independent monolithic high-performance operational amplifiers in a single 14-pin Dual-in-Line package. For the first time, extremely tight matching of critical parameters is provided between channels of a dual operational amplifier, whereas previous dual op amp designs have made no attempt towards matching.

The excellent specifications of the individual amplifiers combined with the tight matching and temperature tracking between channels enables realization of extremely high-performance instrumentation amplifier and matching of discrete amplifiers. The designer is assured of achieving the full performance guaranteed by the specification as the common package eliminates the unavoidable temperature differentials incurred by all designs utilizing separately housed amplifiers.

Matching between channels is provided on all critical parameters including offset voltage, tracking of offset voltage vs. temperature, non-inverting bias currents, and common mode and power supply rejection ratios. The individual amplifiers feature extremely low offset voltage, offset voltage drift, low noise voltage, low bias current and are completely compensated and protected.

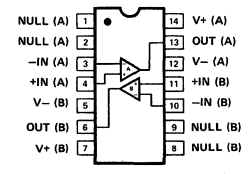
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (mV)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
0.5	OP10AY*	MIL
0.5	OP10EY	COM
0.5	OP10Y*	MIL
0.5	OP10CY	COM

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number.

†All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS

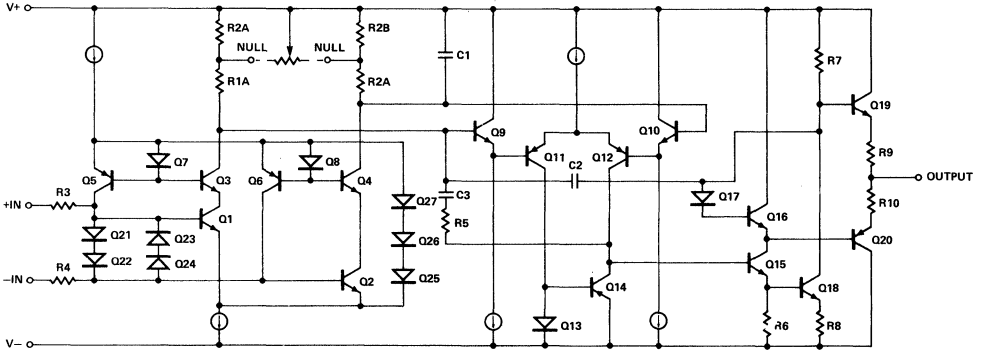


14-PIN CERAMIC DIP (Y-SUFFIX)

NOTE:

Device may be operated even if insertion is reversed; this is due to inherent symmetry of pin locations of amplifiers A and B.

SIMPLIFIED SCHEMATIC (½ OP-10)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V ..... ±22V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±22V
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range
OP-10A, OP-10 ..... −55°C to +125°C
OP-10E, OP-10C ..... 0°C to +70°C
DICE Junction Temperature (T_j) ..... −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
Dual-in-Line (Y)	106°C	11.3mW/°C

NOTES:
1. See table for maximum ambient temperature rating and derating factor.
2. For supply voltages less than +22V, the absolute maximum input voltage is equal to the supply voltage.

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-10A			OP-10			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.2	0.5	—	0.2	0.5	mV
Input Offset Voltage Stability	ΔV_{OS}/Time	(Notes 1, 2)	—	0.25	1.0	—	0.25	1.0	μV/Mo
Input Offset Current	I_{OS}		—	1.0	2.8	—	1.0	2.8	nA
Input Bias Current	I_B		—	±1.0	±3.0	—	±1.0	±3.0	nA
Input Noise Voltage	e_{np-p}	(Note 2) 0.1Hz to 10Hz	—	0.35	0.6	—	0.35	0.6	μV_{p-p}
Input Noise Voltage Density	e_n	f_o = 10Hz (Note 2) f_o = 100Hz f_o = 1000Hz	— — —	10.3 10.0 9.6	18.0 13.0 11.0	— — —	10.3 10.0 9.6	18.0 13.0 11.0	$nV/\sqrt{Hz}$
Input Noise Current	i_{np-p}	(Note 2) 0.1Hz to 10Hz	—	14	30	—	14	30	pA_{p-p}
Input Noise Current Density	i_n	f_o = 10Hz (Note 2) f_o = 100Hz f_o = 1000Hz	— — —	0.32 0.14 0.12	0.80 0.23 0.17	— — —	0.32 0.14 0.12	0.80 0.23 0.17	$pA/\sqrt{Hz}$
Input Resistance — Differential Mode	R_{IN}	(Note 3)	20	60	—	20	60	—	MΩ
Input Resistance — Common Mode	R_{INCM}		—	200	—	—	200	—	GΩ
Input Voltage Range	IVR		±13.0	±14.0	—	±13.0	±14.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.0V$	110	126	—	110	126	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	4	10	—	4	10	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $R_L \geq 500\Omega$, $V_O = \pm .5V$ $V_S = \pm 3V$ (Note 3)	200 150	500 500	— —	200 150	500 500	— —	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0	— — —	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0	— — —	V
Slewing Rate	SR	$R_L \geq 2k\Omega$	—	0.17	—	—	0.17	—	V/μs
Closed Loop Bandwidth	BW	$A_{VCL} = +1.0$	—	0.6	—	—	0.6	—	MHz
Open Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	Each Amplifier $V_S = \pm 3V$	— —	90 4	120 6	— —	90 4	120 6	mW
Offset Adjustment Range		$R_p = 20k\Omega$	—	±4	—	—	±4	—	mV
Input Capacitance	C_{IN}		—	8	—	—	8	—	pF

NOTES:
1. Long term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV — refer to typical performance curves.
2. Sample tested.
3. Guaranteed by design.

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10A MIN	OP-10A TYP	OP-10A MAX	OP-10 MIN	OP-10 TYP	OP-10 MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.3	0.7	—	0.3	0.7	mV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}		—	0.7	2.0	—	0.7	2.0 (Note 2)	μV/°C
With External Trim	TCV_{OSn}	$R_p = 20k\Omega$	—	0.3	1.0	—	0.3	1.0 (Note 2)	μV/°C
Input Offset Current	I_{OS}		—	1.8	5.6	—	1.8	5.6	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	8	50	—	8	50	pA/°C
Input Bias Current	I_B		—	±2.0	±6.0	—	±2.0	±6.0	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	13	50	—	13	50	pA/°C
Input Voltage Range	IVR		±13.0	±13.5	—	±13.0	±13.5	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.0V$	106	123	—	106	123	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	5	20	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	150	400	—	150	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±12.6	—	±12.0	±12.6	—	V

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	OP-10A MIN	OP-10A TYP	OP-10A MAX	OP-10 MIN	OP-10 TYP	OP-10 MAX	UNITS
Input Offset Voltage	ΔV_{OS}		—	0.07	0.18	—	0.12	0.5	mV
Average Non-Inverting Bias Current	I_B+		—	±1.0	±3.0	—	±1.3	±4.5	nA
Non-Inverting Offset Current	$I_{OS}+$		—	0.8	2.8	—	1.1	4.5	nA
Inverting Offset Current	$I_{OS}-$		—	0.8	2.8	—	1.1	4.5	nA
Common Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 13.0V$	114	123	—	106	120	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 3V$ to $\pm 18V$	—	3	10	—	4	20	μV/V
Channel Separation	CS	(Note 2)	126	140	—	126	140	—	dB

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10A MIN	OP-10A TYP	OP-10A MAX	OP-10 MIN	OP-10 TYP	OP-10 MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	0.10	0.30	—	0.20	0.90	mV
Input Offset Voltage Tracking Without External Trim	$TC\Delta V_{OS}$	(Note 2)	—	0.45	1.3	—	0.9	2.5	μV/°C
With External Trim	$TC\Delta V_{OSn}$	Rp = 20kΩ (Note 3) Channel A only	—	0.3	0.8	—	0.4	1.2	μV/°C
Average Non-Inverting Bias Current	I_B+		—	±2.0	±6.0	—	±2.4	±8.0	nA
Average Drift of Non-Inverting Bias Current	TCI_B+	(Note 2)	—	10	40	—	15	—	pA/°C
Non-Inverting Offset Current	$I_{OS}+$		—	2.0	6.5	—	2.4	9.0	nA
Average Drift of Non-Inverting Offset Current	$TCI_{OS}+$	(Note 2)	—	12	50	—	18	—	pA/°C
Inverting Offset Current	$I_{OS}-$		—	2.0	6.5	—	2.4	9.0	nA
Common Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 13.0V$	108	120	—	103	117	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 3V$ to $\pm 18V$	—	6	20	—	7	32	μV/V

NOTES:

1. Long term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV — refer to typical performance curves.
2. Sample tested.
3. Guaranteed by design.

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10E MIN	OP-10E TYP	OP-10E MAX	OP-10C MIN	OP-10C TYP	OP-10C MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.2	0.5	—	0.2	0.5	mV
Input Offset Voltage Stability	ΔV_{OS}/Time	(Notes 1, 2)	—	0.3	1.5	—	0.5	—	μV/Mo
Input Offset Current	I_{OS}		—	1.2	3.8	—	1.8	6.0	nA
Input Bias Current	I_B		—	±1.2	±4.0	—	±1.8	±7.0	nA
Input Noise Voltage	e_{np-p}	(Note 2) 0.1Hz to 10Hz	—	0.35	0.6	—	0.38	0.65	μV_{p-p}
Input Noise Voltage Density	e_n	$f_o = 10Hz$ (Note 2) $f_o = 100Hz$ $f_o = 1000Hz$	— — —	10.3 10.0 9.6	18.0 13.0 11.0	— — —	10.5 10.2 9.8	20.0 13.5 11.5	$nV/\sqrt{Hz}$
Input Noise Current	i_{np-p}	(Note 2) 0.1Hz to 10Hz	—	14	30	—	15	35	pA_{p-p}
Input Noise Current Density	i_n	$f_o = 10Hz$ (Note 2) $f_o = 100Hz$ $f_o = 1000Hz$	— — —	0.32 0.14 0.12	0.80 0.23 0.17	— — —	0.35 0.15 0.13	0.90 0.27 0.18	$pA/\sqrt{Hz}$
Input Resistance — Differential Mode	R_{IN}	(Note 3)	15	50	—	8	33	—	MΩ
Input Resistance — Common Mode	R_{INCM}		—	160	—	—	120	—	GΩ
Input Voltage Range	IVR		±13.0	±14.0	—	±13.0	±14.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.0V$	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	4	20	—	10	32	μV/V
Large Signal Voltage Gain	A_{VO}	$R_{L \geq 2k\Omega}$, $V_O = \pm 10V$ $R_L \geq 500\Omega$, $V_O = \pm 0.5V$ $V_S = \pm 3V$ (Note 3)	200 150	500 500	— —	120 100	400 400	— —	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0	— — —	±12.0 ±11.5 —	±13.0 ±12.8 ±12.0	— — —	V
Slewing Rate	SR	$R_L \geq 2k\Omega$	—	0.17	—	—	0.17	—	V/μs
Closed Loop Bandwidth	BW	$A_{VCL} = +1.0$	—	0.6	—	—	0.6	—	MHz
Open Loop Output Resistance	R_O	$V_O \pm 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	Each Amplifier $V_S = \pm 3V$	— —	90 4	120 6	— —	95 4	150 8	mW
Offset Adjustment Range		$R_p = 20k\Omega$	—	±4	—	—	±4	—	mV
Input Capacitance	C_{IN}		—	8	—	—	8	—	pF

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $0° C \leq T_A \leq +70° C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		OP-10E MIN	OP-10E TYP	OP-10E MAX	OP-10C MIN	OP-10C TYP	OP-10C MAX	UNITS
Input Offset Voltage	V_{OS}			—	0.25	0.6	—	0.35	1.6	mV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}		(Note 2)	—	0.7	2.0	—	1.2	4.5	μV/°C
With External Trim	TCV_{OSn}	$R_p = 20k\Omega$	(Note 2)	—	0.3	1.0	—	0.4	1.5	μV/°C
Input Offset Current	I_{OS}			—	1.4	5.3	—	2.0	8.0	nA
Average Input Offset Current Drift	TCI_{OS}		(Note 2)	—	8	50	—	12	50	pA/°C
Input Bias Current	I_B			—	±1.5	±5.5	—	±2.2	±9.0	nA
Average Input Bias Current Drift	TCI_B		(Note 2)	—	13	50	—	18	50	pA/°C
Input Voltage Range	IVR			±13.0	±13.5	—	±13.0	±13.5	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.0V$		103	123	—	97	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$		—	7	32	—	10	51	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$		100	400	—	100	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$		±12.0	±12.6	—	±11.0	±12.6	—	V

NOTES:

1. Long term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV — refer to typical performance curves.
2. Sample tested.
3. Guaranteed by design.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-10E			OP-10C			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	0.12	0.5	—	0.3	—	mV
Average Non-Inverting Bias Current	I_B+		—	±1.3	±4.5	—	±2.0	—	nA
Non-Inverting Offset Current	$I_{OS}+$		—	1.1	4.5	—	1.8	—	nA
Inverting Offset Current	$I_{OS}-$		—	1.1	4.5	—	1.8	—	nA
Common Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 13.0V$	106	120	—	—	117	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 3V$ to $\pm 18V$	—	4	20	—	5	—	μV/V
Channel Separation	CS	(Note 1)	126	140	—	120	137	—	dB

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $0°C \leq T_A \leq +70°C$, unless otherwise noted.

			OP-10E			OP-10C			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	0.18	0.7	—	0.4	—	mV
Input Offset Voltage Tracking Without External Trim	$TC\Delta V_{OS}$	(Note 1)	—	0.9	2.3 (Note 1)	—	1.3	—	μV/°C
With External Trim	$TC\Delta V_{OSn}$	$R_L = 20k\Omega$ Channel A Only (Note 2)	—	0.3	0.9	—	0.6	—	μV/°C
Average Non-Inverting Bias Current	I_B+		—	±2.0	±6.0	—	±2.8	—	nA
Average Drift of Non-Inverting Bias Current	TCI_B+	(Note 1)	—	12	40 (Note 1)	—	18	—	pA/°C
Non-Inverting Offset Current	$I_{OS}+$		—	2.0	6.0	—	2.8	—	nA
Average Drift of Non-Inverting Offset Current	$TCI_{OS}+$	(Note 1)	—	15	50 (Note 1)	—	20	—	pA/°C
Inverting Offset Current	$I_{OS}-$		—	2.0	6.0	—	2.8	—	nA
Common Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 13V$	103	117	—	—	114	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 3V$ to $\pm 18V$	—	6	32	—	8	—	μV/V

NOTES:
1. Sample tested.
2. Guaranteed by design.

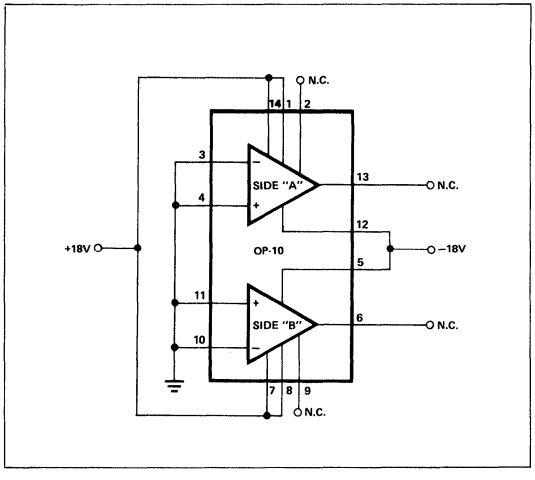
SUPPLY VOLTAGE REJECTION RATIO MATCH (ΔPSRR)

The difference between the power supply rejection ratios (expressed in volt/volt) of side A and side B. ΔPSRR in dB = 20 $\log_{10}$ (ΔPSRR in volt/volt).

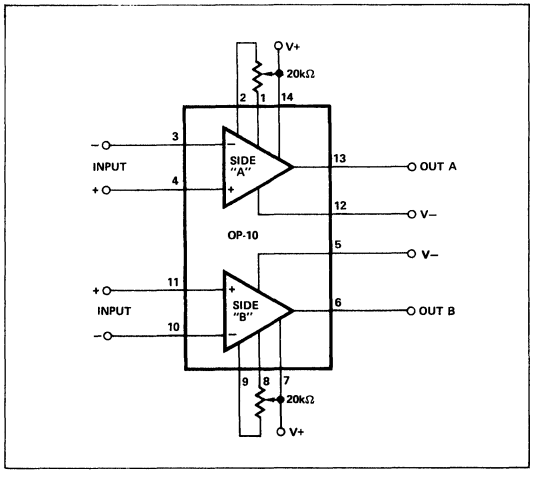
CHANNEL SEPARATION

The ratio of the change in input offset voltage of one channel to the change in output voltage in the second channel producing it.

BURN-IN CIRCUIT

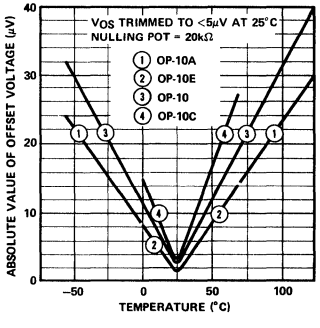


OFFSET NULLING CIRCUIT

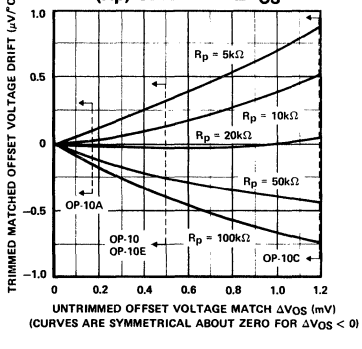


TYPICAL PERFORMANCE CURVES

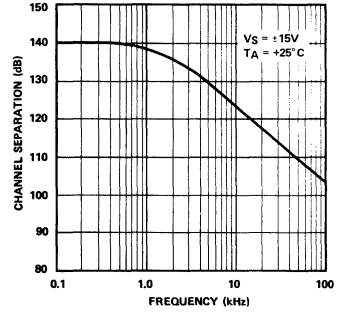
MATCHING CHARACTERISTICS TRIMMED OFFSET VOLTAGE MATCH vs TEMPERATURE



MATCHING CHARACTERISTICS TRIMMED MATCHED OFFSET VOLTAGE DRIFT AS A FUNCTION OF TRIMMING POT (Rp) SIZE AND ΔV_{OS}

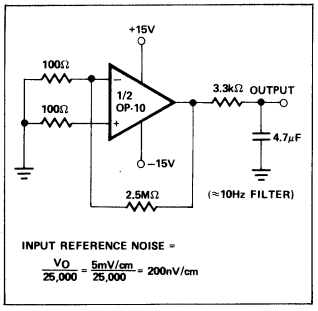


MATCHING CHARACTERISTICS CHANNEL SEPARATION vs FREQUENCY

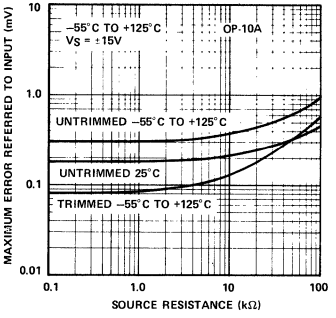


TYPICAL PERFORMANCE CURVES

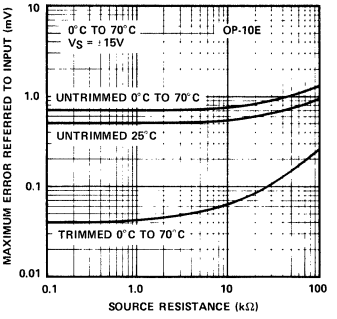
TYPICAL LOW FREQUENCY NOISE TEST CIRCUIT



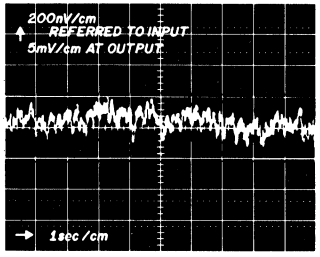
MATCHING CHARACTERISTIC MAXIMUM INPUT ERROR vs SOURCE RESISTANCE



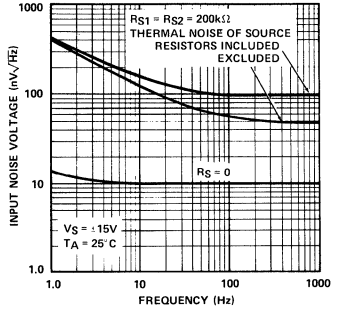
MATCHING CHARACTERISTIC MAXIMUM INPUT ERROR vs SOURCE RESISTANCE



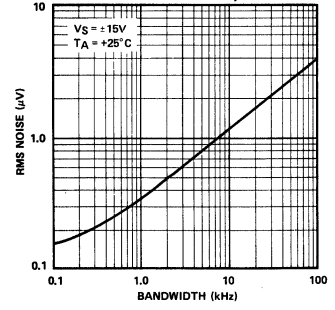
OP-10 LOW FREQUENCY NOISE



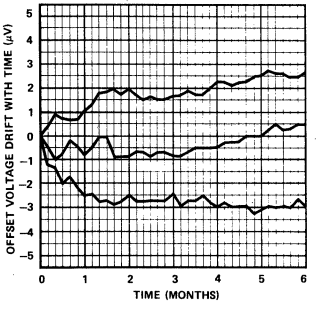
TOTAL INPUT NOISE VOLTAGE vs FREQUENCY



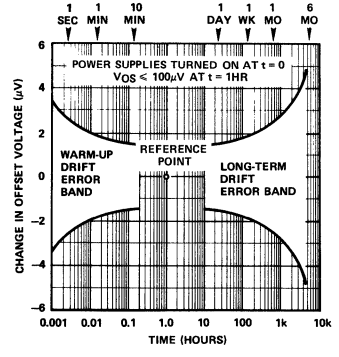
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1 Hz TO FREQUENCY INDICATED)



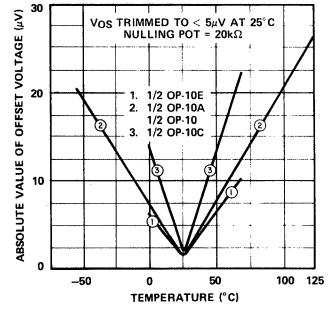
TYPICAL OFFSET VOLTAGE STABILITY vs TIME



OFFSET VOLTAGE DRIFT WITH TIME

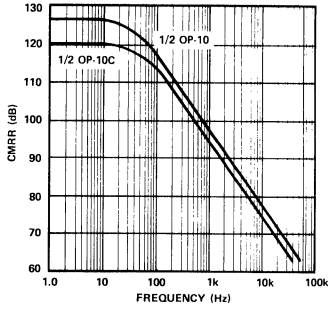


TRIMMED OFFSET VOLTAGE vs TEMPERATURE

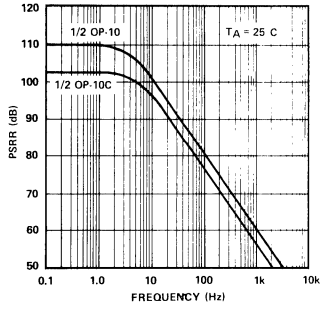


TYPICAL PERFORMANCE CURVES EACH AMPLIFIER

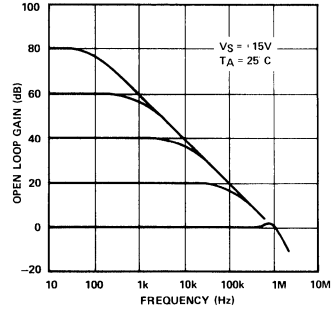
CMRR vs FREQUENCY



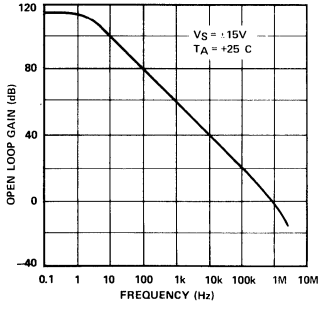
PSRR vs FREQUENCY



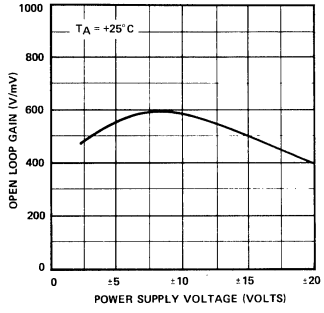
CLOSED LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



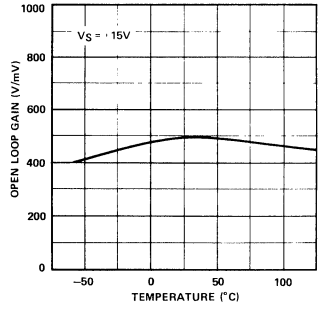
OPEN LOOP FREQUENCY RESPONSE



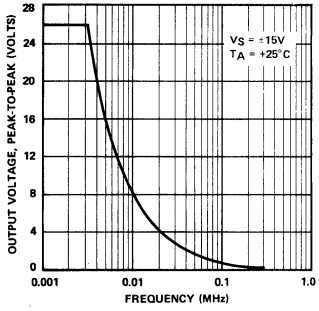
OPEN LOOP GAIN vs POWER SUPPLY VOLTAGE



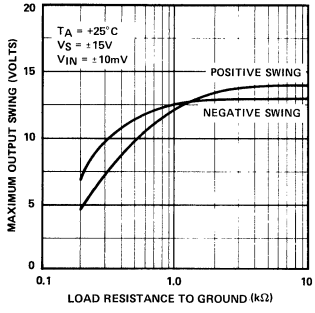
OPEN LOOP GAIN vs TEMPERATURE



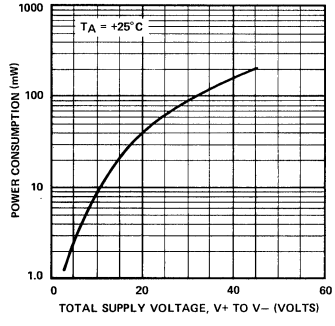
MAXIMUM UNDISTORTED OUTPUT vs FREQUENCY



OUTPUT SWING vs LOAD

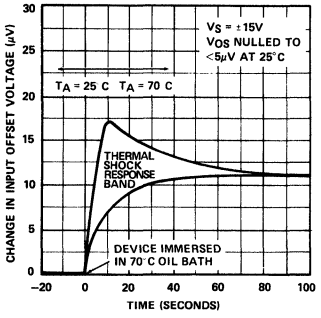


POWER CONSUMPTION vs POWER SUPPLY

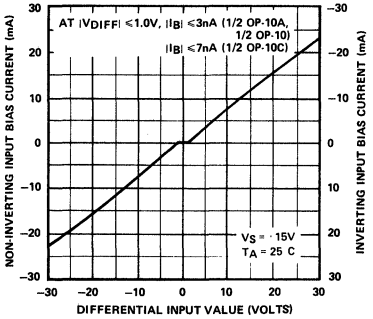


TYPICAL PERFORMANCE CURVES

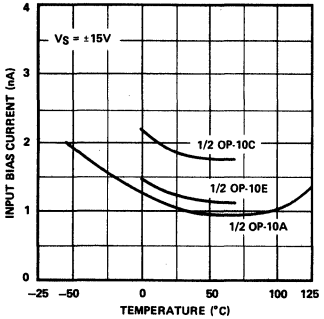
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



INPUT BIAS CURRENT vs TEMPERATURE

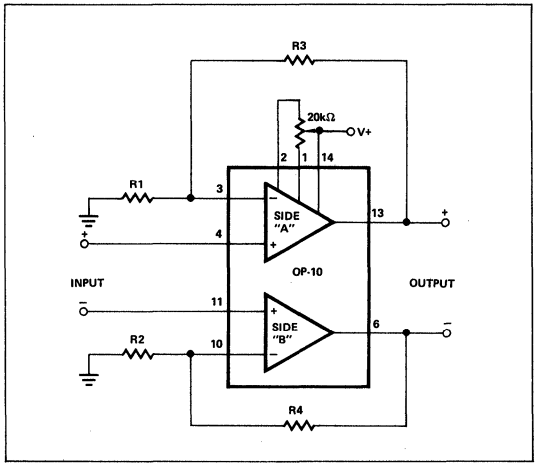


APPLICATIONS INFORMATION

SPECIAL NOTES ON THE APPLICATION OF DUAL-MATCHED OPERATIONAL AMPLIFIERS

ADVANTAGES OF DUAL MATCHED OPERATIONAL AMPLIFIERS

Dual Matched Operational Amplifiers provide the engineer a powerful tool for the solution of a number of difficult circuit design problems including true instrumentation amplifiers, extremely low drift, high common-mode rejection DC amplifiers, low DC drift active filters, dual tracking voltage references and many other demanding applications. These designs are based on the principle that careful matching between two operational amplifiers can, to a large extent, eliminate the effect of DC errors inherent in the individual amplifiers.



Reference to the circuit shown, a differential-in, differential-out amplifier, shows how the reductions in error can be accomplished. Assuming the resistors used are ideally matched, the gain of each side will be identical; if the offset voltages of each amplifier are perfectly matched, then the net differential voltage at the amplifiers output will be zero. Note that the output offset error of this amplifier is not a function of the offset voltage of the individual amplifiers, but only a function of the **difference** (degree of matching) between the amplifiers' offset voltages. This error-cancellation principle holds for a considerable number of input referred error parameters — offset voltage, offset voltage drift, inverting and non-inverting bias currents, common mode and power supply rejection ratios. Note also that the impedances of each input, both common mode and differential mode, are extremely high and can also be tightly matched, an important feature not possible with single operational amplifier circuits. Common-mode rejection can be made exceptionally high; this is especially important in instrumentation amplifiers where errors due to large common mode voltages can be far greater than those due to noise or drift with temperature.

(For example, consider the case of two op amps, each with 80dB (100μV/V) CMRR. However, if the CMRR of one device is +100μV/V while CMRR of the the other is −100μV/V for a net 200μV/V CMRR match, the resultant input referred error over a 10V common mode input signal will be 2mV.)

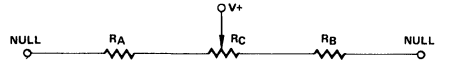
POWER SUPPLIES

The V+ supply terminals are completely independent and may be powered by separate supplies if desired (this approach, however, would sacrifice the advantages of the power supply rejection ratio matching). The V− supply terminals are both connected to the common substrate and must be tied to the same voltage.

OFFSET TRIMMING

Offset trimming terminals are provided for each amplifier of the OP-10 — however, guaranteed performance over temperature can be obtained by trimming only one side (side A) to match the offset of the other for a net differential offset of zero. This is due to the specific procedure used during factory testing of the devices; however, results which are essentially the same may be obtained by trimming side B to match side A, or by nulling each side individually.

The OP-10 is designed to provide lowest drift performance when trimmed with a 20kΩ potentiometer; this value provides about ±4mV of adjustment range which should be considerably more than adequate for most applications. Where finer resolution of trimming is desired, or where unwanted changes in potentiometer position with time and temperature could create unacceptable offsets, the sensitivity to offset vs. potentiometer position may be reduc by using the circuit shown below.



Model	Null Range	Fixed Resistors R_A, R_B	Potentiometer R_C
OP-10AY, OP-10Y, OP-10EY	±1.2mV	5.1kΩ	10.0kΩ

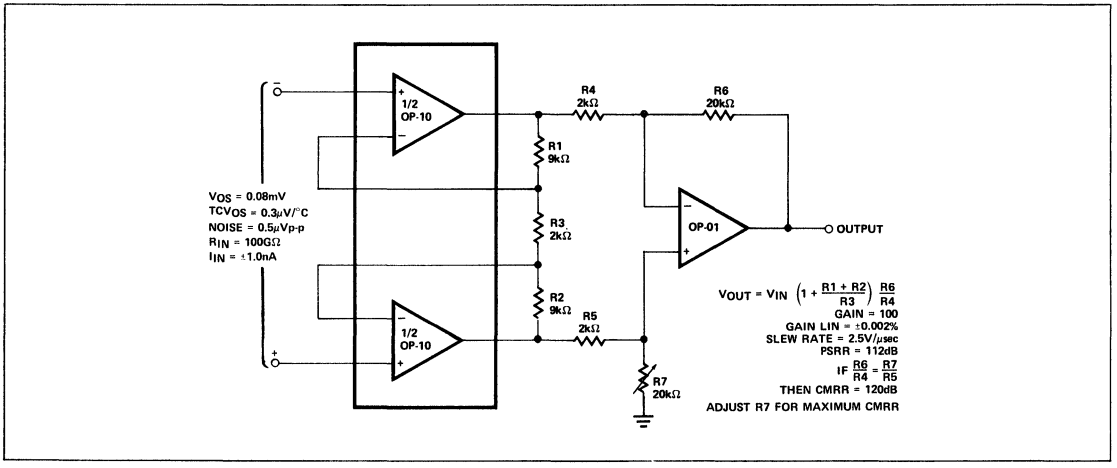
TYPICAL PERFORMANCE OF INSTRUMENTATION AMPLIFIERS GAIN = 100

PARAMETER	2 OP AMP DESIGN	3 OP AMP DESIGN
Gain Nonlinearity	.004%	.001% (OP-05)
		.002% (OP-01)
Initial Input Offset Voltage	70μV	75μV
vs. Temperature (amplifier A nulled with 20k pot)	03μV/°C	0.3μV/°C
vs. Time	3.5μV/month	3.5μV/month
Input Bias Current	±1.0nA	±1.0nA
vs. Temperature	10pA/°C	10pA/°C
Input Offset Current	0.8nA	0.8nA
vs. Temperature	12pA/°C	12pA/°C
Input Impedance Differential	80GΩ	100GΩ
Common Mode	100GΩ	100GΩ
Input Noise Voltage (0.1 to 10Hz)	$0.5\mu V_{p-p}$	$0.5\mu V_{p-p}$
Input Noise Current (0.1 to 10Hz)	14pAp-p	14pAp-p
Common Mode Rejection	120dB	120dB
Power Supply Rejection	112dB	112dB
Frequency Response		
Small Signal (−3dB)	6.0Hz	26kHz (OP-05) 85kHz (OP-01)
Full Power	2.5Hz	4.3kHz (OP-05) 43kHz (OP-01)
Slew Rate	0.17V/μs	0.17V/μsec (OP-05) 4.0V/μsec (OP-01)

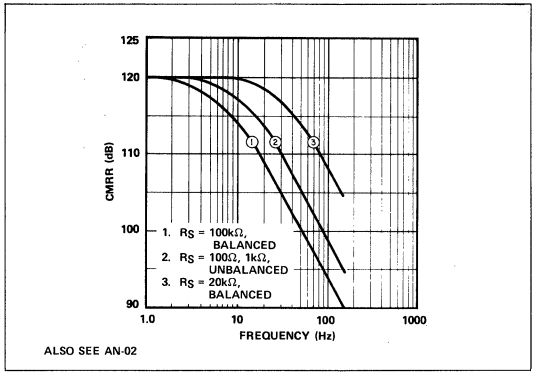
INSTRUMENTATION AMPLIFIERS USING OP-10

Instrumentation Amplifiers with excellent performance can be easily and compactly built using the OP-10. Typical performance for a two and three-amplifier design are given in the table. The three-amplifier design, while more complex, has the advantages of convenient overall gain adjustment by trimming a single resistor (R_3) and of wide common mode voltage handling capability at any overall gain, plus improved gain linearity. Slew rate, small-signal bandwidth, and full power bandwidth are also superior. Speed may be further improved by use of an OP-01 series op amp for the output stage.

TRIPLE OP-AMP INSTRUMENTATION AMPLIFIER

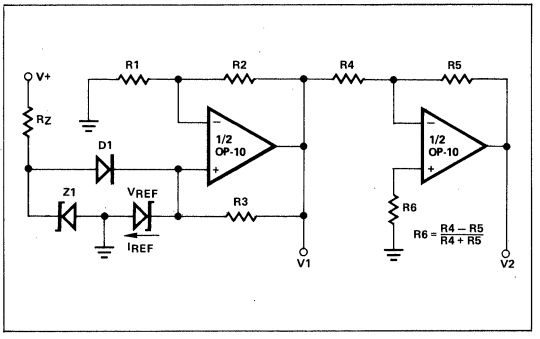


CMRR vs FREQUENCY INSTRUMENTATION AMPLIFIER (3 OP-AMP DESIGN)



ALSO SEE AN-02

PRECISION DUAL TRACKING VOLTAGE REFERENCES USING OP-10



PRECISION DUAL TRACKING VOLTAGE REFERENCES USING OP-10

Precision dual tracking voltage references using a single reference source are easily constructed using OP-10. These references exhibit low noise, excellent stability vs. temperature and time, and have excellent power supply rejection.

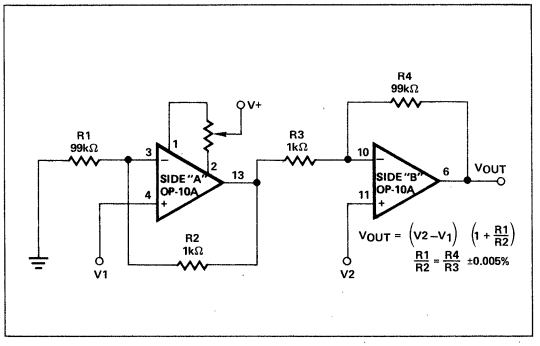
In the circuit shown, R_3 should be adjusted to set I_{REF} to operate V_{REF} at its minimum temperature coefficient current. Proper circuit start-up is assured by R_Z, Z_1, and D_1.

$$V_{Z1} \leq V_{REF} + 2.0V \qquad V1 = V_{REF}\left(1 + \frac{R2}{R1}\right)$$

$$I_{REF} = (V1 - V_{REF})/R3 \qquad V2 = V1\left(\frac{-R5}{R4}\right)$$

Output Impedance (ΔI_L:1.0mA-5.0mA) . . . $0.25 \cdot 10^3\Omega$

INSTRUMENTATION AMPLIFIER (2 OP-AMP DESIGN)



OP-12

PRECISION LOW INPUT CURRENT OPERATIONAL AMPLIFIER
INTERNALLY COMPENSATED

FEATURES

- **Low Offset Voltage** ..... **150μV Maximum**
- **Low Offset Voltage Drift** ..... **2.5μV/°C Maximum**
- **Load Current Capability** ..... **5 mA Minimum**
- **Internal Frequency Compensation**
- **125° C Temperature Tested Die**
- **Low Offset Current** ..... **200pA Maximum**
- **Low Bias Current** ..... **2.0nA Maximum**
- **Low Power Consumption** .... **18mW Maximum @ ±15V**
- **High Common Mode Input Range** .....**±13V Minimum**
- **MIL-STD-883 Class B Processing Available**
- **Silicon-Nitride Passivation**

ORDERING INFORMATION†

T_A = 25° C V_{OS} MAX (mV)	PACKAGE HERMETIC TO-99 8-PIN	PACKAGE HERMETIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
0.15	OP12AJ*	OP12AZ*	MIL
0.15	OP12EJ	OP12EZ	COM
0.30	OP12BJ*	OP12BZ*	MIL
0.30	OP12FJ	OP12FZ	COM
1.0	OP12CJ*	OP12CZ*	MIL
1.0	OP12GJ	OP12GZ	COM

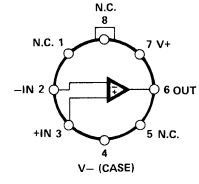
* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

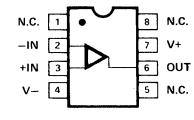
GENERAL DESCRIPTION

The PMI OP-12 is an improved version of the popular LM108A low-power op amp. The OP-12 is internally compensated and its chip dimensions are only 42 x 58 mils. Additionally, the OP-12 has a three times lower offset voltage and a two times lower offset voltage drift. The total worst case input offset voltage over −55°C to +125°C for the OP-12Ais only 350μV while the 108A has 900μV to 1000μV for these conditions. In addition, the OP-12 drives a 2kΩ load. This is five times the output current capability of the 108A. This excellent performance is achieved by applying PMI's ion-implanted super beta process and on-chip zener-zap trimming capabilities. The internal compensation makes this op amp ideal for hybrid assembly applications.

PIN CONNECTIONS

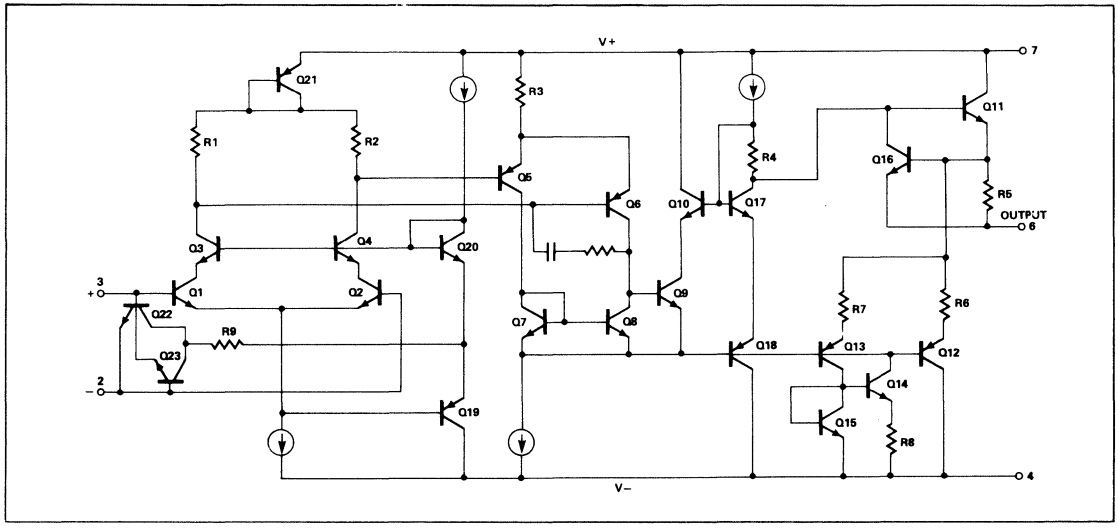


TO-99 (J-Suffix)



8-PIN HERMETIC MINI-DIP (Z-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage
- OP-12A, OP-12B,
- OP-12E, OP-12F, All DICE except GR ..... ±20V
- OP-12C, OP-12G, GR DICE Only ..... ±18V

Operating Temperature Range
- OP-12A, OP-12B, OP-12C ..... −55°C to +125°C
- OP-12E, OP-12F, OP-12G ..... 0°C to +70°C

Storage Temperature Range ..... −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec.) ..... 300°C
Internal Power Dissipation (Note 1) 500mW
Differential Input Current (Note 2) ..... ±10mA
Input Voltage (Note 3) ..... ±15V
Output Short Circuit Duration ..... Indefinite
DICE Junction Temperature (T_j) ..... −65°C to +150°C

NOTES:
1. See table for maximum ambient temperature rating and derating factor.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
Hermetic 8-Pin DIP (Z)	75°C	6.7mW/°C

2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is provided.
3. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
4. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 20V$ and $T_A = 25°C$ for A, B, E and F grades, $V_S = \pm 15V$, and $T_A = 25°C$ for C and G grades, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-12A/E MIN	OP-12A/E TYP	OP-12A/E MAX	OP-12B/F MIN	OP-12B/F TYP	OP-12B/F MAX	OP-12C/G MIN	OP-12C/G TYP	OP-12C/G MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.07	0.15	—	0.18	0.30	—	0.25	1.0	mV
Input Offset Current	I_{OS}		—	0.05	0.20	—	0.05	0.20	—	0.08	0.50	nA
Input Bias Current	I_B		—	0.80	2.0	—	0.80	2.0	—	1.0	5.0	nA
Input Resistance-Differential Mode	R_{IN}	(Note 1)	26	70	—	26	70	—	10	50	—	MΩ
Input Voltage Range	IVR	$V_S = \pm 15V$	±13.0	±14.0	—	±13.0	±14.0	—	±13.0	±14.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.0V$	104	120	—	104	120	—	84	116	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	—	1	7	—	1	7	—	4	63	μV/V
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$, $V_S = \pm 15V$ $R_L \geq 2k\Omega$, $V_S = \pm 15V$	±13.0 ±10.0	±14.0 ±12.0	— —	±13.0 ±10.0	±14.0 ±12.0	— —	±13.0 ±10.0	±14.0 ±12.0	—	V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 10k\Omega$ $V_O = \pm 10V$ $R_L \geq 2k\Omega$ $V_O = \pm 10V$	80 50	300 150	— —	80 50	300 150	— —	40 —	250 100	— —	V/mV
Power Consumption	P_d	$V_S = \pm 15V$, No Load $V_S = \pm 5V$, No Load	— —	9 3	18 6	— —	9 3	18 6	— —	12 4	24 8	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.9	—	—	0.9	—	—	0.9	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_o = 10Hz$ $f_o = 100Hz$ $f_o = 1000Hz$	— — —	22 21 20	— — —	— — —	22 21 20	— — —	— — —	22 21 20	— — —	$nV/\sqrt{Hz}$
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	3	—	—	3	—	—	3	—	pA_{p-p}
Input Noise Current Density	i_n	$f_o = 10Hz$ $f_o = 100Hz$ $f_o = 1000Hz$	— — —	0.15 0.14 0.13	— — —	— — —	0.15 0.14 0.13	— — —	— — —	0.15 0.14 0.13	— — —	$pA/\sqrt{Hz}$
Slewing Rate	SR	$R_L \geq 2k\Omega$	—	0.12	—	—	0.12	—	—	0.12	—	V/μs
Closed Loop Bandwidth	BW	$A_{VCL} = +1.0$	—	0.80	—	—	0.80	—	—	0.80	—	MHz
Open Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	200	—	—	200	—	—	200	—	Ω

NOTE:
1. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, for C grade, $V_S = \pm 20V$ for A and B grades, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

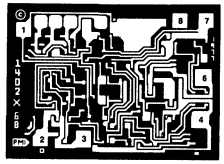
PARAMETER	SYMBOL	CONDITIONS	OP-12A MIN	OP-12A TYP	OP-12A MAX	OP-12B MIN	OP-12B TYP	OP-12B MAX	OP-12C MIN	OP-12C TYP	OP-12C MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.12	0.35	—	0.28	0.60	—	0.40	2.0	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.50	2.5	—	1.0	3.5	—	1.5	10	µV/°C
Input Offset Current	I_{OS}		—	0.12	0.40	—	0.12	0.40	—	0.18	1.0	nA
Average Input Offset Current Drift	TCI_{OS}		—	0.50	2.5	—	0.50	2.5	—	1.0	5.0	pA/°C
Input Bias Current	I_B		—	1.2	3.0	—	1.2	3.0	—	1.8	10	nA
Input Voltage Range	IVR	$V_S = \pm 15V$	±13.0	±14.0	—	±13.0	±14.0	—	±13.0	±14.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.0V$	100	116	—	100	116	—	80	112	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 15V$	—	4	10	—	4	10	—	6	100	µV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 5k\Omega$, $V_O = \pm 10V$	40	120	—	40	120	—	15	80	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$, $V_S = \pm 15V$ $R_L \geq 5k\Omega$, $V_S = \pm 15V$	±13.0 ±10.0	±14.0 ±13.0	— —	±13.0 ±10.0	±14.0 ±13.0	— —	±13.0 ±10.0	±14.0 ±12.0	— —	V
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	9	18	—	9	18	—	15	24	mW

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, for G grade, $V_S = \pm 20V$ for E and F grades, $0°C \leq T_A \leq 70°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-12E MIN	OP-12E TYP	OP-12E MAX	OP-12F MIN	OP-12F TYP	OP-12F MAX	OP-12G MIN	OP-12G TYP	OP-12G MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.10	0.26	—	0.23	0.45	—	0.32	1.4	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.50	2.5	—	1.0	3.5	—	1.5	10	µV/°C
Input Offset Current	I_{OS}		—	0.08	0.30	—	0.11	0.60	—	0.12	0.70	nA
Average Input Offset Current Drift	TCI_{OS}		—	0.50	2.5	—	1.0	5.0	—	1.0	5.0	pA/°C
Input Bias Current	I_B		—	1.0	2.6	—	1.2	5.2	—	1.4	6.5	nA
Input Voltage Range	IVR	$V_S = \pm 15V$	±13.0	±14.0	—	±13.0	±14.0	—	±13.0	±14.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.0V$	100	116	—	100	116	—	80	112	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 15V$	—	4	10	—	4	10	—	6	100	µV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 10k\Omega$, $V_O = \pm 10V$ $R_L \geq 2k\Omega$, $V_O = \pm 10V$	60 25	200 100	— —	60 25	200 100	— —	25 —	150 80	— —	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$, $V_S = \pm 15V$ $R_L \geq 5k\Omega$, $V_S = \pm 15V$	±13.0 ±10.0	±14.0 ±12.0	— —	±13.0 ±10.0	±14.0 ±12.0	— —	±13.0 ±10.0	±14.0 ±12.0	— —	V
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	9	18	—	9	18	—	15	24	mW

For typical performance curves, see Op-08 data sheet. Assume $C_C = 30pF$.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



DIE SIZE 0.058 × 0.042 inch

1. NO CONNECTION
2. INVERTING INPUT
3. NON-INVERTING INPUT
4. V–
6. OUTPUT
7. V+
8. NO CONNECTION

Refer to Section 2 for additional DICE informaiton

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +125°C$ for OP-12NT and OP-12GT, $T_A = +25°C$ for OP-12N, OP-12G and OP-12GR, unless otherwise noted. (Note 2)

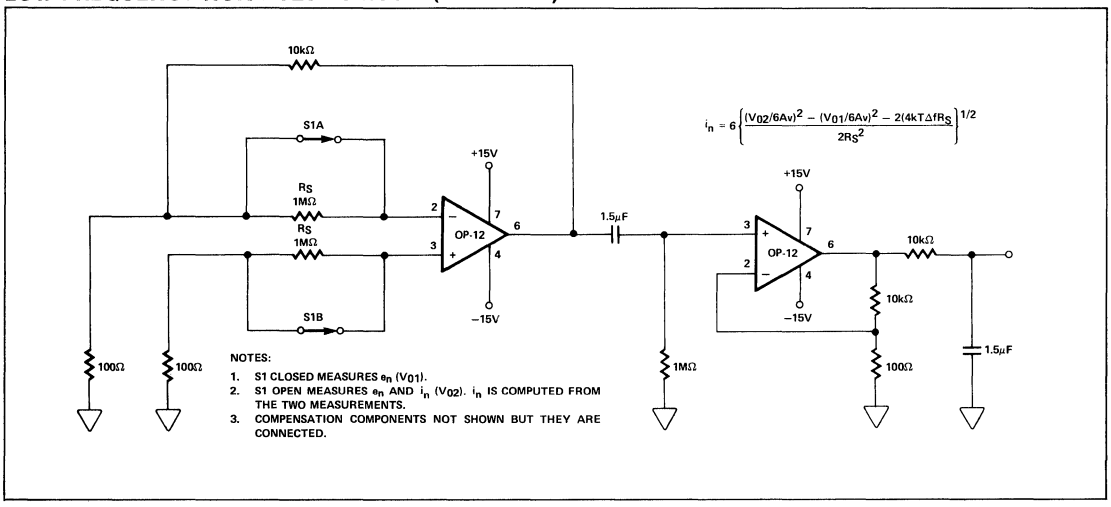
PARAMETER	SYMBOL	CONDITIONS	OP-12NT LIMIT	OP-12N LIMIT	OP-12GT LIMIT	OP-12G LIMIT	OP-12GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		0.35	0.3	0.6	0.5	1.0	mV MAX
Input Offset Current	I_{OS}		0.2	0.2	0.2	0.2	0.5	nA MAX
Input Bias Current	I_B		2.0	2.0	2.0	2.0	5.0	nA MAX
Input Voltage Range	IVR		±13	±13	±13	±13	±13	V MIN
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	100	104	100	104	84	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	10	7	10	7	63	μV/V MAX
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±13	±13	±13	±13	±13	V MIN
		$R_L \geq 2k\Omega$	—	±10	—	±10	±10	
		$R_L \geq 5k\Omega$	±10	—	±10	—	—	
Large Signal Voltage Gain	A_{VO}	$R_L \geq 10k\Omega$, $V_O = \pm 10V$	80	80	80	80	40	V/mV MIN
		$R_L \geq 2k\Omega$, $V_O = \pm 10V$	—	50	—	50	—	
		$R_L \geq 5k\Omega$, $V_O = \pm 10V$	40	—	40	—	—	
Input Resistance	R_{IN}	(Note 1)	25	25	13	13	10	MΩ MIN
Supply Current	I_{SY}	$I_{OUT} = 0$, $V_{OUT} = 0$	0.6	0.6	0.6	0.6	0.8	mA MAX

NOTES:
1. Guaranteed by design.
2. For 25°C specifications of OP-12NT and OP-12GT, see OP-12N and OP-12G, respectively.

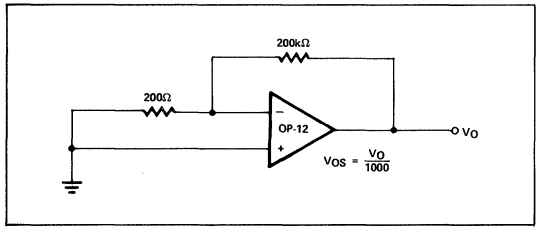
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-12NT TYPICAL	OP-12N TYPICAL	OP-12GT TYPICAL	OP-12G TYPICAL	OP-12GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}		1.0	1.0	1.0	1.0	1.5	μV/°C
Average Input Offset Current Drift	TCI_{OS}		0.5	0.5	1.0	1.0	1.0	pA/°C

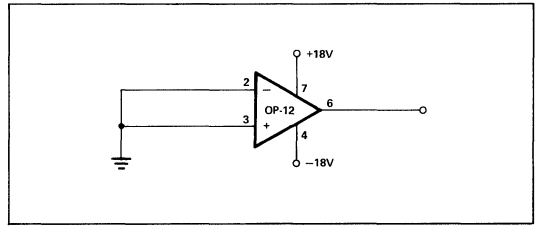
LOW FREQUENCY NOISE TEST CIRCUIT (0.1 to 10Hz)



OFFSET VOLTAGE TEST CIRCUIT



BURN-IN CIRCUIT



OP-15/OP-16/OP-17

PRECISION JFET-INPUT OPERATIONAL AMPLIFIERS

FEATURES (All Devices)

- **Significant Performance Advantages over LF155, 156 and 157 Devices.**
- **Low Input Offset Voltage ..... 500μV Maximum**
- **Low Input Offset Voltage Drift ..... 2.0μV/° C**
- **Minimum Slew Rate Guaranteed on All Models**
- **Temperature-Compensated Input Bias Currents**
- **Guaranteed Input Bias Current @ 125° C**
- **Bias Current Specified WARMED UP Over Temperature**
- **Internal Compensation**
- **Low Input Noise Current ..... 0.01pA/$\sqrt{Hz}$**
- **High Common-Mode Rejection Ratio 100dB**
- **Models With MIL-STD-883 Class B Processing Available From Stock**
- **125° C Temperature Tested DICE**

OP-15

- **156 Speed With 155 Dissipation..... (80mW Typical)**
- **Wide Bandwidth..... 6MHz**
- **High Slew Rate..... 17V/μs**
- **Fast Settling to ±0.1% 900ns**

OP-16

- **Higher Slew Rate 25V/μs**
- **Faster Settling To ±0.1%..... 700ns**
- **Wider Bandwidth 8MHz**

OP-17

- **Highest Slew Rate 70V/μs**
- **Fastest Settling to ±0.1% 400ns**
- **Highest Gain Bandwidth Product 30MHz**

GENERAL DESCRIPTION

The PMI BIFET Series of devices offers clear advantages over industry-generic BIFET's and is superior in both cost and performance to many dielectrically-isolated and hybrid op-amps. All devices offer offset voltages as low as 0.5mV with T_cV_{OS} guaranteed to 5μV/° C. A unique input bias cancellation circuit reduces the I_B by a factor of 10 over conventional designs. In addition, PMI specifies I_B and I_{OS} with the devices warmed up and operating at 25° C ambient.

These devices were designed to provide real precision performance along with high speed. Although they can be nulled, the design objective was to provide low offset-voltage without nulling. Systems generally become more cost effective as the number of error correcting "knobs" is decreased. PMI achieves this performance by use of an improved BIFET process coupled with on-chip, zener-zap offset trimming.

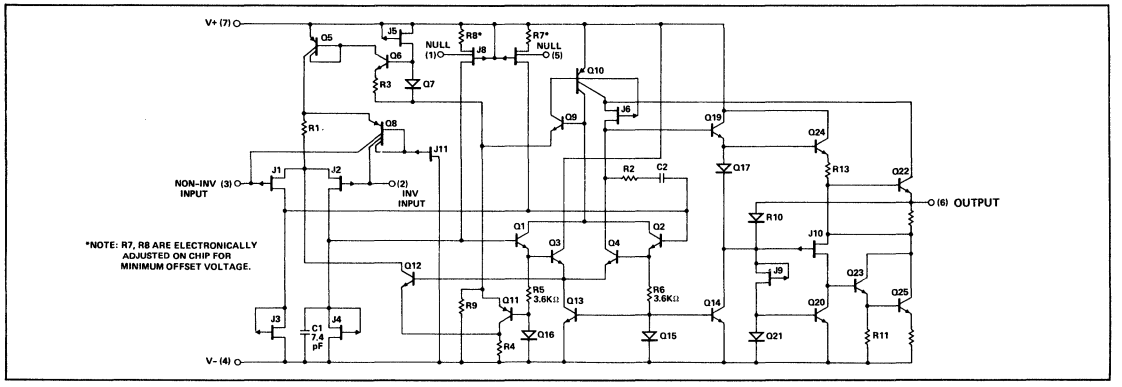
The OP-15 provides an excellent combination of high speed and low input offset voltage. In addition, the OP-15 offers the speed of the 156A op amp with the power dissipation of a 155A. The combination of a low input offset voltage of 500μV, slew rate of 17V/μs, and settling time of 900 ns to 0.1% makes the OP-15 an op amp of both precision and speed. The additional features of low supply current coupled with an input bias current of 9nA at 125° C ambient (not junction) temperature makes the OP-15 ideal for a wide range of applications.

The OP-16 features a slew rate of 25V/μs and a settling time of 700 ns to 0.1% which represents a 100% improvement in speed over the 156. Also the OP-16 has all the D.C. features of the OP-15.

The OP-17 has a slew rate of 70V/μs and is the best choice for applications requiring high closed-loop gain with high speed. Applications include high-speed amplifiers for current output DACs, active filters, sample-and-hold buffers, and photocell amplifiers.

See the OP-215 data sheet for a dual configuration of the OP-15.

SIMPLIFIED SCHEMATIC DIAGRAM



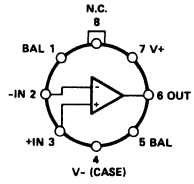
ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	PACKAGE 8-PIN HERMETIC DIP	OPERATING TEMPERATURE RANGE
0.5	OP15AJ* OP16AJ* OP17AJ*	OP15AZ* OP16AZ* OP17AZ*	MIL
0.5	OP15EJ OP16EJ OP17EJ	OP15EZ OP16EZ OP17EZ	COM
1.0	OP15BJ* OP16BJ* OP17BJ*	OP15BZ* OP16BZ* OP17BZ*	MIL
1.0	OP15FJ OP16FJ OP17FJ	OP15FZ OP16FZ OP17FZ	COM
3.0	OP15CJ* OP16CJ* OP17CJ*	OP15CZ* OP16CZ* OP17CZ*	MIL
3.0	OP15GJ OP16GJ OP17GJ	OP15GZ OP16GZ OP17GZ	COM

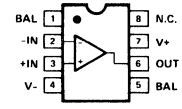
* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



TO-99
(J-Suffix)



8-PIN HERMETIC DIP
(Z-Suffix)

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage
- All Devices Except C, G (Packaged) & GR Grades . . ±22V
- C, G (Packaged) & GR Grades . . . . . ±18V

Internal Power Dissipation (Note 1) 500mW

Operating Temperature
- A, B, & C Grades . . . . . −55°C to +125°C
- E, F & G Grades . . . . . 0°C to +70°C

Maximum Junction Temperature . . . . . +150°C

DICE Junction Temperature (T_j) . . . . . −65°C to +150°C

Differential Input Voltage
- All Devices Except C, G (Packaged) & GR Grades . . ±40V
- C, G (Packaged) & GR Grades . . . . . ±30V

Input Voltage (Note 3)
- All Devices Except C, G (Packaged) & GR Grades . . ±20V
- C, G (Packaged) & GR Grades . . . . . ±16V

Input Voltage
- OP-15A, OP-15B, OP-15E, OP-15F . . . . . ±20V
- OP-15C, OP-15G . . . . . ±16V
- OP-16A, OP-16B, OP-16E, OP-16F . . . . . ±20V
- OP-16C, OP-16G . . . . . ±16V
- OP-17A, OP-17B, OP-17E, OP-17F . . . . . ±20V
- OP-17C, OP-17G . . . . . ±16V

Output Short Circuit Duration . . . . . Indefinite

Storage Temperature Range . . . . . −65°C to +150°C

Lead Temperature Range (Soldering, 60 sec.) . . . +300°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.
3. Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		OP-15A/E OP-16A/E OP-17A/E MIN	TYP	MAX	OP-15B/F OP-16B/F OP-17B/F MIN	TYP	MAX	OP-15C/G OP-16C/G OP-17C/G MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$		—	0.2	0.5	—	0.4	1.0	—	0.5	3.0	mV
Input Offset Current	I_{OS}	$T_J = 25°C$ (Note 1)	OP-15	—	3.0	10	—	6.0	20	—	12	50	pA
		Device Operating		—	5.0	22	—	10.0	40	—	20	100	
		$T_J = 25°C$ (Note 1)	OP-16/OP-17	—	3.0	10	—	6.0	20	—	12	50	
		Device Operating		—	5.0	25	—	10.0	50	—	20	125	
Input Bias Current	I_B	$T_J = 25°C$ (Note 1)	OP-15	—	15	50	—	30	100	—	60	200	pA
		Device Operating		—	18	110	—	40	200	—	80	400	
		$T_J = 25°C$ (Note 1)	OP-16/OP-17	—	15	50	—	30	100	—	60	200	
		Device Operating		—	20	130	—	40	250	—	80	500	
Input Resistance	R_{IN}			—	10^{12}	—	—	10^{12}	—	—	10^{12}	—	Ω
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$		100	240	—	75	220	—	50	200	—	V/mV
Output Voltage Swing	V_O	$R_L = 10k\Omega$		±12	±13	—	±12	±13	—	±12	±13	—	V
		$R_L = 2k\Omega$		±11	±12.7	—	±11	±12.7	—	±11	±12.7	—	
Supply Current	I_{SY}		OP-15	—	2.7	4.0	—	2.7	4.0	—	2.8	5.0	mA
			OP-16/OP-17	—	4.6	7.0	—	4.6	7.0	—	4.8	8.0	
Slew Rate	SR	$A_{VCL} = +1.0$ (Note 3)	OP-15	10	17	—	7.5	16	—	5.0	15	—	V/μs
			OP-16	18	25	—	12	24	—	9.0	23	—	
		$A_{VCL} = +5.0$ (Note 3)	OP-17	45	70	—	35	66	—	25	62	—	
Gain Bandwidth Product	GBW	(Note 3)	OP-15	4.0	6.0	—	3.5	5.7	—	3.0	5.4	—	MHz
			OP-16	6.0	8.0	—	5.5	7.6	—	5.0	7.2	—	
			OP-17	20	30	—	15	28	—	11	26	—	
Closed Loop Bandwidth	CLBW	$A_{VCL} = +1.0$	OP-15	—	14	—	—	13	—	—	12	—	MHz
			OP-16	—	19	—	—	18	—	—	17	—	
		$A_{VCL} = +5.0$	OP-17	—	11	—	—	10	—	—	9	—	
Settling Time	t_s	to 0.01%		—	2.2	—	—	2.3	—	—	2.4	—	μs
		to 0.05% (Note 2)	OP-15	—	1.1	—	—	1.1	—	—	1.2	—	
		to 0.10%		—	0.9	—	—	0.9	—	—	1.0	—	
		to 0.01%		—	1.7	—	—	1.7	—	—	1.8	—	
		to 0.05% (Note 2)	OP-16	—	0.9	—	—	0.9	—	—	1.0	—	
		to 0.10%		—	0.7	—	—	0.7	—	—	0.8	—	
		to 0.01%		—	1.5	—	—	1.5	—	—	1.6	—	
		to 0.05% (Note 4)	OP-17	—	0.5	—	—	0.5	—	—	0.6	—	
		to 0.10%		—	0.4	—	—	0.4	—	—	0.5	—	
Input Voltage Range	IVR			±10.5	—	—	±10.5	—	—	±10.3	—	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10.5V$		86	100	—	86	100	—	—	—	—	dB
		$V_{CM} = \pm 10.3V$		—	—	—	—	—	—	82	96	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$		—	10	51	—	10	51	—	—	—	μV/V
		$V_S = \pm 10V$ to $\pm 15V$		—	—	—	—	—	—	—	16	80	
Input Noise Voltage Density	e_n	$f_o = 100Hz$		—	20	—	—	20	—	—	20	—	$nV/\sqrt{Hz}$
		$f_o = 1000Hz$		—	15	—	—	15	—	—	15	—	
Input Noise Current Density	i_n	$f_o = 100Hz$		—	0.01	—	—	0.01	—	—	0.01	—	$pA/\sqrt{Hz}$
		$f_o = 1000Hz$											
Input Capacitance	C_{IN}			—	3.0	—	—	3.0	—	—	3.0	—	pF

NOTES:

1. Input bias current is specified for two different conditions. The $T_j = 25°C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at 25° C ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs T_j and I_B vs T_A. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Settling time is defined here for a unity gain inverter connection using 2kΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within a specified percent of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.
3. Sample tested.
4. Settling time is defined here for a $A_V = -5$ connection with $R_F = 2k\Omega$. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 2V step input is applied to the inverter. See settling time test circuit.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-55°C \le T_A \le 125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		OP-15A/16A/17A MIN	OP-15A/16A/17A TYP	OP-15A/16A/17A MAX	OP-15B/16B/17B MIN	OP-15B/16B/17B TYP	OP-15B/16B/17B MAX	OP-15C/16C/17C MIN	OP-15C/16C/17C TYP	OP-15C/16C/17C MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$		—	0.4	0.9	—	0.7	2.0	—	0.9	4.5	mV
Average Input Offset Voltage Drift											(Note 2)		
Without External Trim	TCV_{OS}			—	2.0	5.0	—	3.0	10	—	4.0	15	µV/°C
With External Trim	TCV_{OSn}	$R_p = 100k\Omega$		—	2.0	—	—	3.0	—	—	4.0	—	
Input Offset Current (Note 1)	I_{OS}	$T_J = 125°C$		—	0.6	4.0	—	0.8	6.0	—	1.0	9.0	nA
		$T_A = 125°C$ Device Operating	OP-15	—	0.8	7.0	—	1.2	11	—	1.5	17	
		$T_J = 125°C$		—	0.6	4.0	—	0.8	6.0	—	1.0	9.0	
		$T_A = 125°C$ Device Operating	OP-16/OP-17	—	1.0	8.5	—	1.3	14.5	—	1.7	22	
Input Bias Current (Note 1)	I_B	$T_J = 125°C$		—	1.2	5.0	—	1.5	7.5	—	1.8	10	nA
		$T_A = 125°C$ Device Operating	OP-15	—	1.7	9.0	—	2.2	14	—	2.7	19	
		$T_J = 125°C$		—	1.2	5.0	—	1.5	7.5	—	1.8	10	
		$T_A = 125°C$ Device Operating	OP-16/OP-17	—	2.0	11	—	2.5	18	—	3.0	25	
Input Voltage Range	IVR			±10.4	—	—	±10.4	—	—	±10.25	—	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10.4V$		85	97	—	85	97	—	—	—	—	dB
		$V_{CM} = \pm 10.25V$		—	—	—	—	—	—	80	93	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$		—	15	57	—	15	57	—	—	—	µV/V
		$V_S = \pm 10V$ to $\pm 15V$		—	—	—	—	—	—	—	23	100	
Large Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$		35	120	—	30	110	—	25	100	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 10k\Omega$		±12	±13	—	±12	±13	—	±12	±13	—	V

NOTES:

1. Input bias current is specified for two different conditions. The $T_j = 25°C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at 25° C ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs T_j and I_B vs T_A. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Sample tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \leq T_A \leq 70°C$, unless otherwise noted.

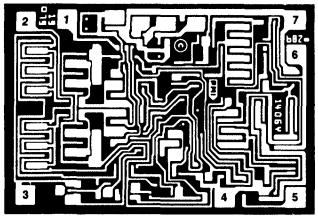
PARAMETER	SYMBOL	CONDITIONS		OP-15E OP-16E OP-17E MIN	TYP	MAX	OP-15F OP-16F OP-17F MIN	TYP	MAX	OP-15G OP-16G OP-17G MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$		—	0.3	0.75	—	0.55	1.5	—	0.7	3.8	mV
Average Input Offset Voltage Drift											(Note 2)		
Without External Trim	TCV_{OS}			—	2.0	5.0	—	3.0	10	—	4.0	15	µV/°C
With External Trim	TCV_{OSn}	$R_p = 100k\Omega$		—	2.0	—	—	3.0	—	—	4.0	—	
Input Offset Current (Note 1)	I_{OS}	$T_J = 70°C$		—	0.04	0.30	—	0.06	0.45	—	0.08	0.65	nA
		$T_A = 70°C$ Device Operating	OP-15	—	0.06	0.55	—	0.08	0.80	—	0.10	1.2	
		$T_J = 70°C$		—	0.04	0.30	—	0.06	0.45	—	0.08	0.65	
		$T_A = 70°C$ Device Operating	OP-16/OP-17	—	0.07	0.70	—	0.10	1.1	—	0.15	1.7	
Input Bias Current (Note 1)	I_B	$T_J = 70°C$		—	0.10	0.40	—	0.12	0.60	—	0.14	0.80	nA
		$T_A = 70°C$ Device Operating	OP-15	—	0.13	0.75	—	0.16	1.1	—	0.19	1.5	
		$T_J = 70°C$		—	0.10	0.40	—	0.12	0.60	—	0.14	0.80	
		$T_A = 70°C$ Device Operating	OP-16/OP-17	—	0.15	0.90	—	0.20	1.4	—	0.25	2.0	
Input Voltage Range	IVR			±10.4	—	—	±10.4	—	—	±10.25	—	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10.4V$		85	98	—	85	98	—	—	—	—	dB
		$V_{CM} = \pm 10.25V$		—	—	—	—	—	—	80	94	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$		—	13	57	—	13	57	—	—	—	µV/V
		$V_S = \pm 10V$ to $\pm 15V$		—	—	—	—	—	—	—	20	100	
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$		65	200	—	50	180	—	35	160	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$		±12	±13	—	±12	±13	—	±12	±13	—	V

NOTES:

1. Input bias current is specified for two different conditions. The $T_J = 25°C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at 25°C ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of 1_B vs T_J and 1_B vs T_A. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. 1_B and 1_{OS} are measured at $V_{CM} = 0$.
2. Sample tested.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)

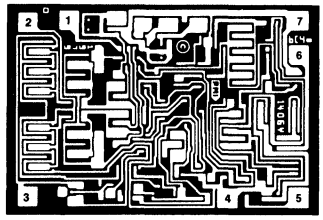
OP-15



DIE SIZE 0.064 × 0.045 inch

1. BALANCE
2. INVERTING INPUT
3. NON-INVERTING INPUT
4. V –
5. BALANCE
6. OUTPUT
7. V +

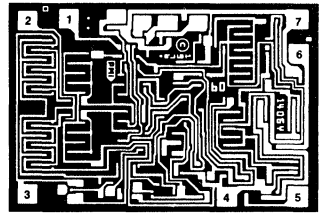
OP-16



DIE SIZE 0.064 × 0.045 inch

1. BALANCE
2. INVERTING INPUT
3. NON-INVERTING INPUT
4. V –
5. BALANCE
6. OUTPUT
7. V +

OP-17



DIE SIZE 0.064 × 0.045 inch

1. BALANCE
2. INVERTING INPUT
3. NON-INVERTING INPUT
4. V –
5. BALANCE
6. OUTPUT
7. V+

See Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$ for OP-15/16/17N, OP-15/16/17G and OP-15/16/17GR devices, $T_A = +125°C$ for OP-15/16/17NT and OP-15/16/17GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-15NT OP-16NT OP-17NT LIMIT	OP-15N OP-16N OP-17N LIMIT	OP-15GT OP-16GT OP-17GT LIMIT	OP-15G OP-16G OP-17G LIMIT	OP-15GR OP-16GR OP-17GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	0.9	0.5	2.0	1.0	3.0	mV MAX
Large Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$, $R_L = 2k\Omega$	35	100	30	75	50	V/mV MIN
Input Voltage Range	IVR		±10.4	±10.5	±10.4	±10.5	±10.3	V MIN
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	85	86	85	86	82	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$	57	51	57	51	—	µV/V MAX
		$V_S = \pm 10V$ to $\pm 15V$	—	—	—	—	80	
Output Voltage Swing	V_O	$R_L = 10k\Omega$	±12	±12	±12	±12	±12	V MIN
		$R_L = 2k\Omega$	—	±11	—	±11	±11	
Supply Current	I_{SY}	OP-15	—	4.0	—	4.0	5.0	mA MAX
		OP-16, OP-17	—	7.0	—	7.0	8.0	
Input Bias Current	I_B	OP-15	9.0	—	14.0	—	—	nA MAX
		OP-16, OP-17	11.0	—	18.0	—	—	
Input Offset Current	I_{OS}	OP-15	7.0	—	11.0	—	—	nA MAX
		OP-16, OP-17	8.5	—	14.5	—	—	

NOTE: For 25° C characteristics of OP-15/16/17NT and OP-15/16/17GT, see OP-15/16/17N and OP-15/16/17G characteristics, respectively.

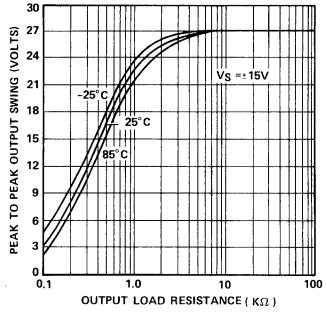
DICE CHARACTERISTICS (continued)

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

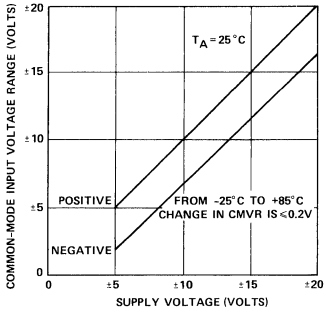
PARAMETER	SYMBOL	CONDITIONS		OP-15NT OP-16NT OP-17NT TYP	OP-15N OP-16N OP-17N TYP	OP-15GT OP-16GT OP-17GT TYP	OP-15G OP-16G OP-17G TYP	OP-15GR OP-16GR OP-17GR TYP	UNITS
Average Input Offset Drift Unnulled	TCV_{OS}			2.0	2.0	3.0	3.0	4.0	µV/°C
Average Input Offset Drift Nulled	TCV_{OSn}	$R_p = 100k\Omega$		2.0	2.0	3.0	3.0	4.0	µV/°C
Input Offset Current	I_{OS}			3.0	3.0	3.0	3.0	3.0	pA
Input Bias Current	I_B			15	15	15	15	15	pA
Slew Rate	SR	$A_{VCL} = +1$	OP-15	17	17	16	16	15	V/µs
			OP-16	25	25	24	24	23	
		$A_{VCL} = +5$	OP-17	70	70	66	66	62	
Settling Time (see settling time test circuits)	t_s	to 0.01%		2.2	2.2	2.3	2.3	2.4	µs
		to 0.05%	OP-15	1.1	1.1	1.1	1.1	1.2	
		to 0.10%		0.9	0.9	0.9	0.9	1.0	
		to 0.01%		1.7	1.7	1.7	1.7	1.8	
		to 0.05%	OP-16	0.9	0.9	0.9	0.9	1.0	
		to 0.10%		0.7	0.7	0.7	0.7	0.8	
		to 0.01%		1.5	1.5	1.5	1.5	1.6	
		to 0.05%	OP-17	0.5	0.5	0.5	0.5	0.6	
		to 0.10%		0.4	0.4	0.4	0.4	0.5	
Gain Bandwidth Product	GBW		OP-15	6.0	6.0	5.7	5.7	5.4	MHz
			OP-16	8.0	8.0	7.6	7.6	7.2	
			OP-17	30	30	28	28	26	
Closed Loop Bandwidth	CLBW	$A_{VCL} = +1$	OP-15	14	14	13	13	12	MHz
			OP-16	19	19	18	18	17	
		$A_{VCL} = +5$	OP-17	11	11	10	10	9	
Input Noise Voltage Density	e_n	f = 100Hz		20	20	20	20	20	$nV/\sqrt{Hz}$
		f = 1000Hz		15	15	15	15	15	
Input Noise Current Density	i_n	f = 100Hz		0.01	0.01	0.01	0.01	0.01	$pA/\sqrt{Hz}$
		f = 1000Hz		0.01	0.01	0.01	0.01	0.01	
Input Capacitance	C_{IN}			3	3	3	3	3	pF

TYPICAL PERFORMANCE CURVES (OP-15/OP-16/OP-17)

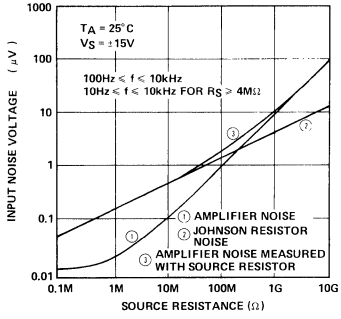
OUTPUT VOLTAGE SWING vs LOAD RESISTANCE



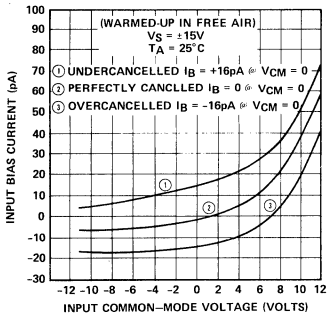
COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE



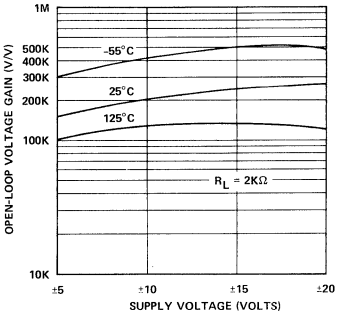
VOLTAGE NOISE vs SOURCE RESISTANCE



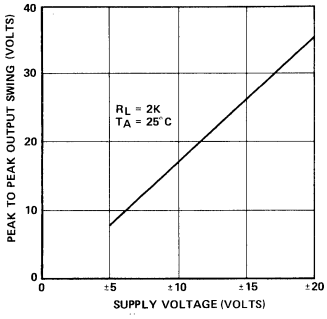
INPUT BIAS CURRENT vs COMMON MODE VOLTAGE



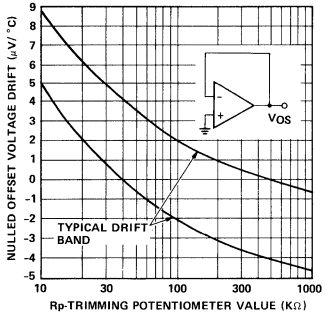
OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE



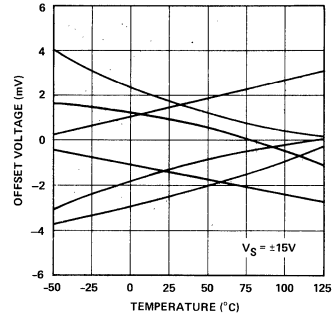
OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE



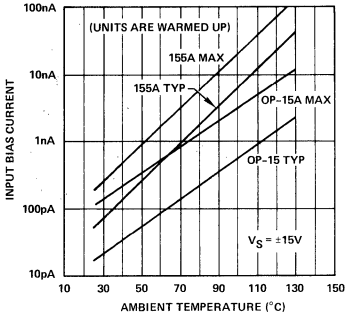
NULLED OFFSET VOLTAGE DRIFT vs POTENTIOMETER SIZE



OFFSET VOLTAGE DRIFT vs TEMPERATURE OF REPRESENTATIVE UNITS

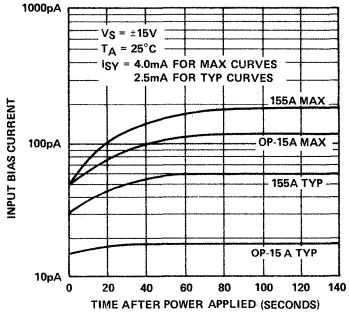


INPUT BIAS CURRENT vs AMBIENT TEMPERATURE (UNITS ARE WARMED-UP IN FREE AIR)

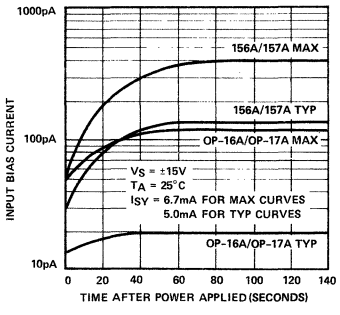


TYPICAL PERFORMANCE CURVES (OP-15/OP-16/OP-17)

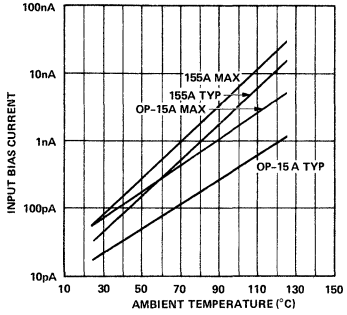
BIAS CURRENT VS. TIME IN FREE AIR (OP-15)



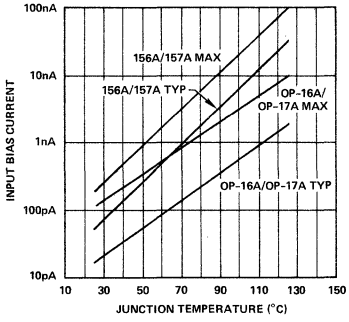
BIAS CURRENT VS. TIME IN FREE AIR (OP-16/OP-17)



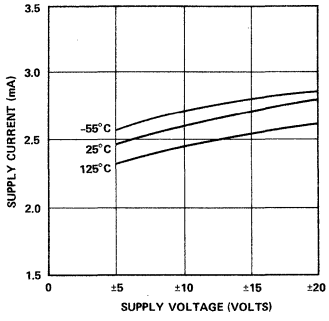
INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE (UNITS ARE WARMED-UP IN FREE AIR) (OP-15)



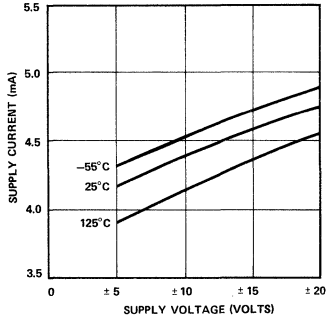
INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE (UNITS ARE WARMED-UP IN FREE AIR) (OP-16/OP-17)



SUPPLY CURRENT VS. SUPPLY VOLTAGE (OP-15)

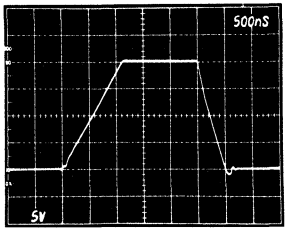


SUPPLY CURRENT VS. SUPPLY VOLTAGE (OP-16/OP-17)

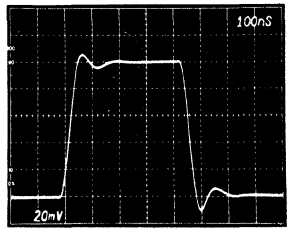


TYPICAL PERFORMANCE CURVES (OP-15)

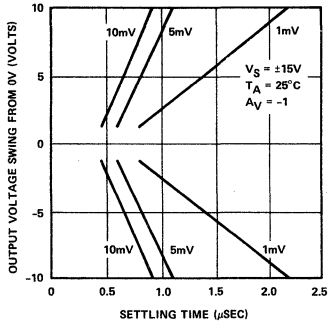
LARGE-SIGNAL TRANSIENT RESPONSE



SMALL-SIGNAL TRANSIENT RESPONSE

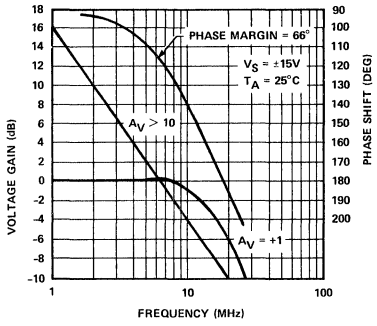


SETTLING TIME

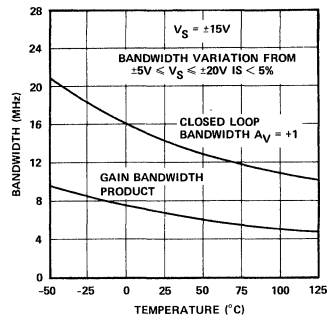


TYPICAL PERFORMANCE CURVES (OP-15)

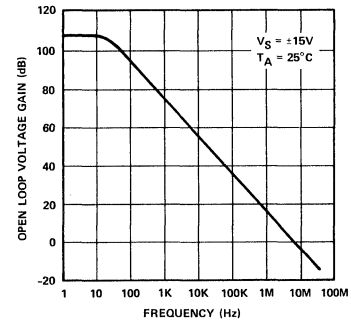
CLOSED-LOOP BANDWIDTH AND PHASE SHIFT vs FREQUENCY



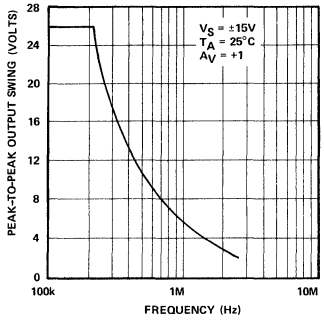
BANDWIDTH vs TEMPERATURE



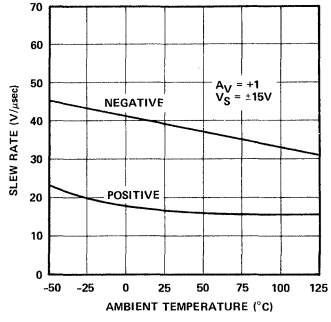
OPEN-LOOP FREQUENCY RESPONSE



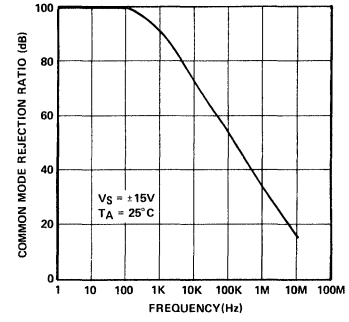
UNDISTORTED OUTPUT SWING vs FREQUENCY



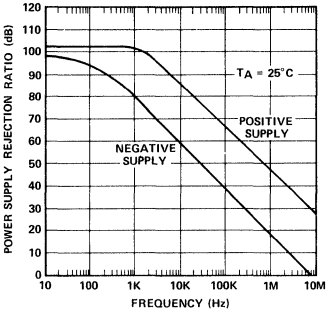
SLEW RATE vs TEMPERATURE



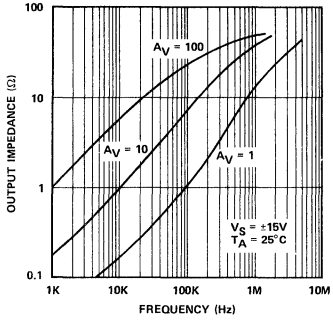
COMMON-MODE REJECTION RATIO vs FREQUENCY



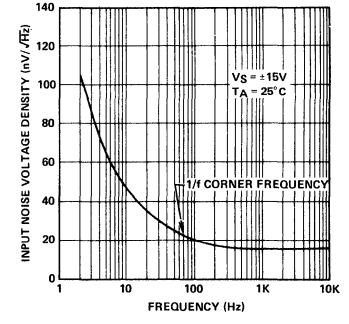
POWER SUPPLY REJECTION vs FREQUENCY



OUTPUT IMPEDANCE vs FREQUENCY

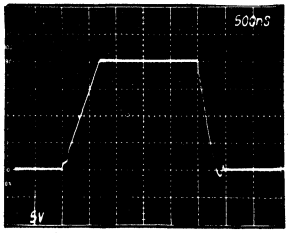


VOLTAGE NOISE vs FREQUENCY

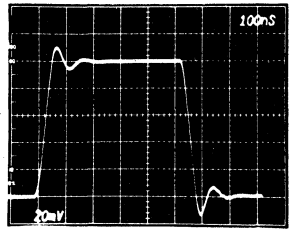


TYPICAL PERFORMANCE CURVES (OP-16)

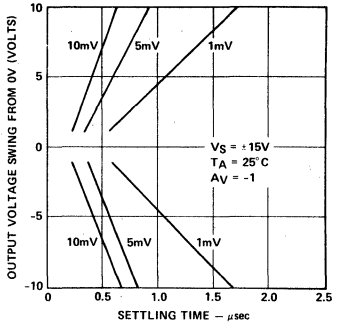
LARGE-SIGNAL TRANSIENT RESPONSE



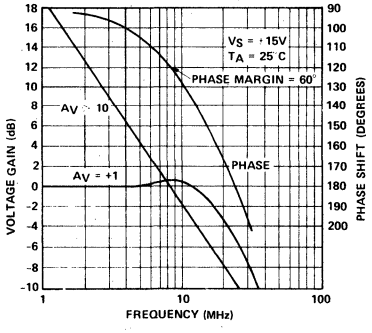
SMALL-SIGNAL TRANSIENT RESPONSE



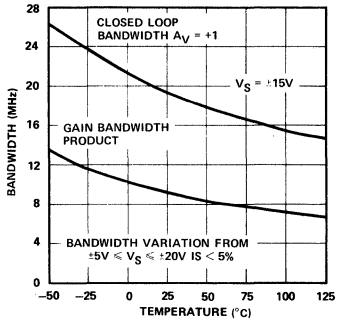
SETTLING TIME



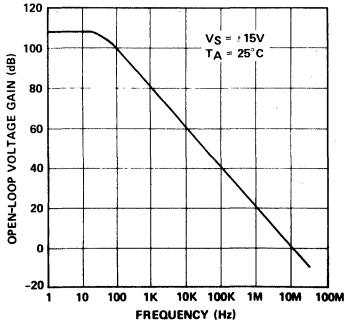
CLOSED-LOOP BANDWIDTH AND PHASE SHIFT vs FREQUENCY



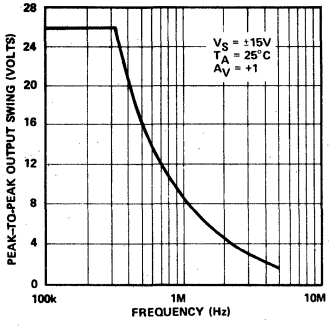
BANDWIDTH vs TEMPERATURE



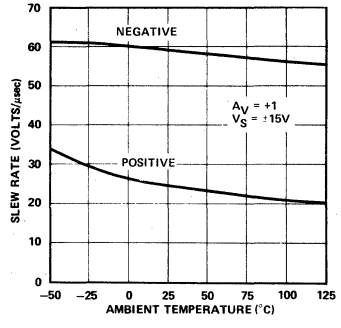
OPEN-LOOP FREQUENCY RESPONSE



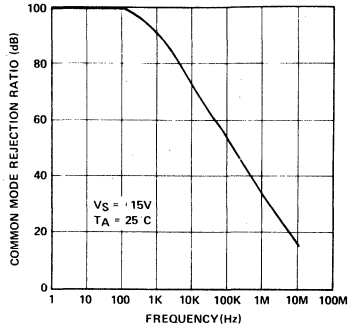
UNDISTORTED OUTPUT SWING vs FREQUENCY



SLEW RATE vs TEMPERATURE

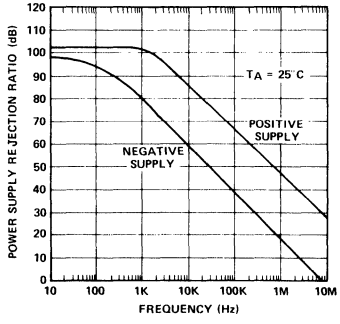


COMMON MODE REJECTION RATIO vs FREQUENCY

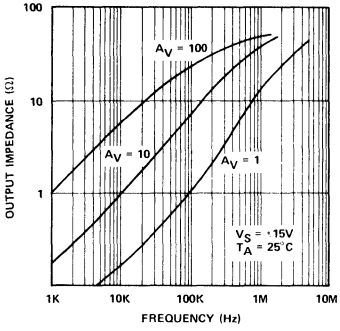


TYPICAL PERFORMANCE CURVES (OP-16)

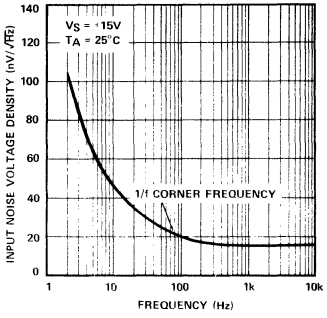
POWER SUPPLY REJECTION vs FREQUENCY



OUTPUT IMPEDANCE vs FREQUENCY

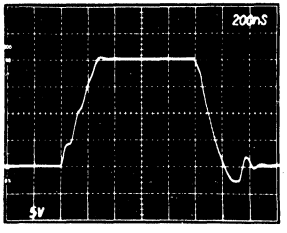


VOLTAGE NOISE vs FREQUENCY

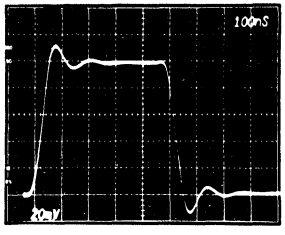


TYPICAL PERFORMANCE CURVES (OP-17)

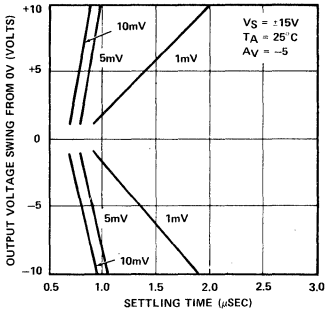
LARGE-SIGNAL TRANSIENT RESPONSE



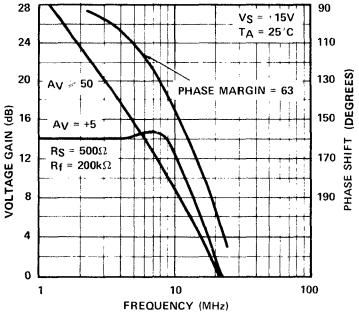
SMALL-SIGNAL TRANSIENT RESPONSE



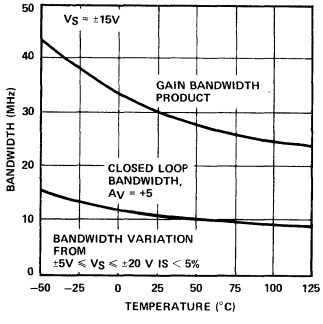
SETTLING TIME



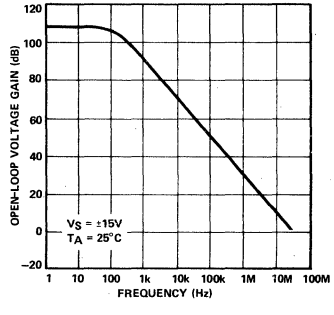
CLOSED-LOOP BANDWIDTH AND PHASE SHIFT vs FREQUENCY



BANDWIDTH vs TEMPERATURE

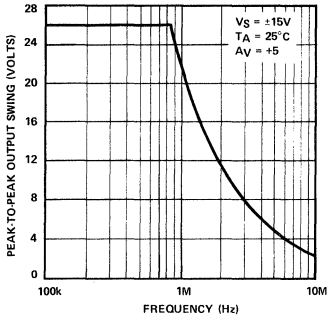


OPEN-LOOP FREQUENCY RESPONSE

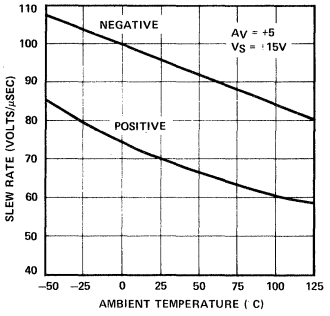


TYPICAL PERFORMANCE CURVES (OP-17)

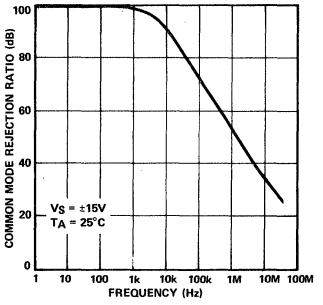
UNDISTORTED OUTPUT SWING vs FREQUENCY



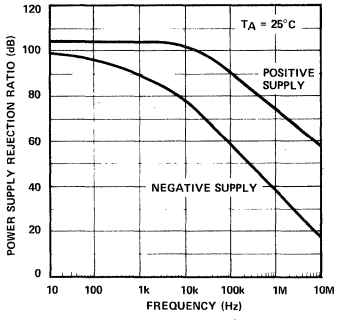
SLEW RATE vs TEMPERATURE



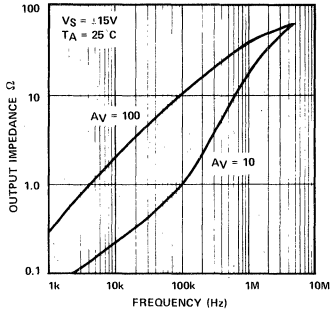
COMMON MODE REJECTION RATIO vs FREQUENCY



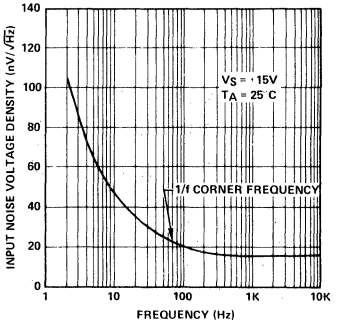
POWER SUPPLY REJECTION vs FREQUENCY



OUTPUT IMPEDANCE vs FREQUENCY

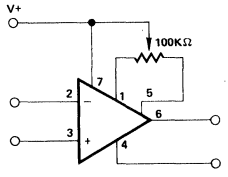


VOLTAGE NOISE vs FREQUENCY



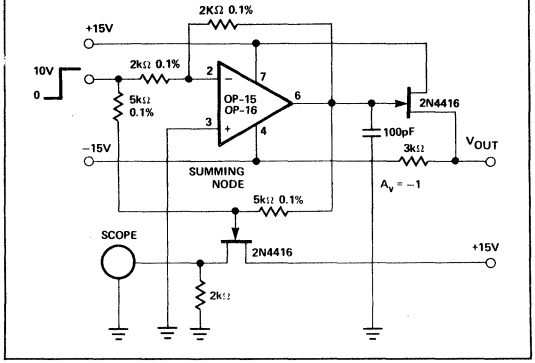
BASIC CONNECTIONS

INPUT OFFSET VOLTAGE NULLING

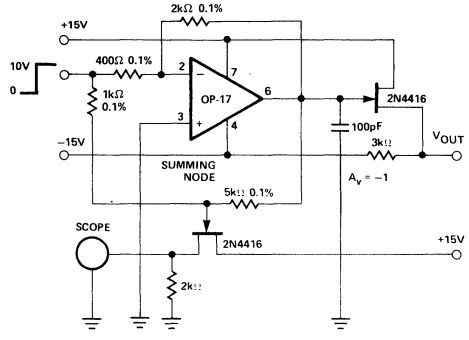


NOTE: V_{OS} CAN BE TRIMMED WITH POTENTIOMETERS RANGING FROM 10kΩ TO 1MΩ. FOR MOST UNITS TCV_{OS} WILL BE MINIMUM WHEN V_{OS} IS ADJUSTED WITH A 100kΩ POTENTIOMETER.

SETTLING TIME TEST CIRCUIT — OP-15/OP-16

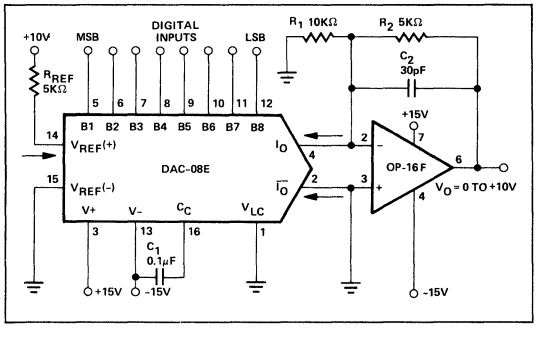


SETTLING TIME TEST CIRCUIT — OP-17



TYPICAL APPLICATIONS

CURRENT-TO-VOLTAGE AMPLIFIER OUTPUT



APPLICATION INFORMATION

DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement, and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency a lead capacitor should be placed from the output to the negative input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than,or equal,to the original feedback pole time constant.

OP-18

HIGH PERFORMANCE GENERAL PURPOSE EXTERNALLY COMPENSATED OPERATIONAL AMPLIFIER

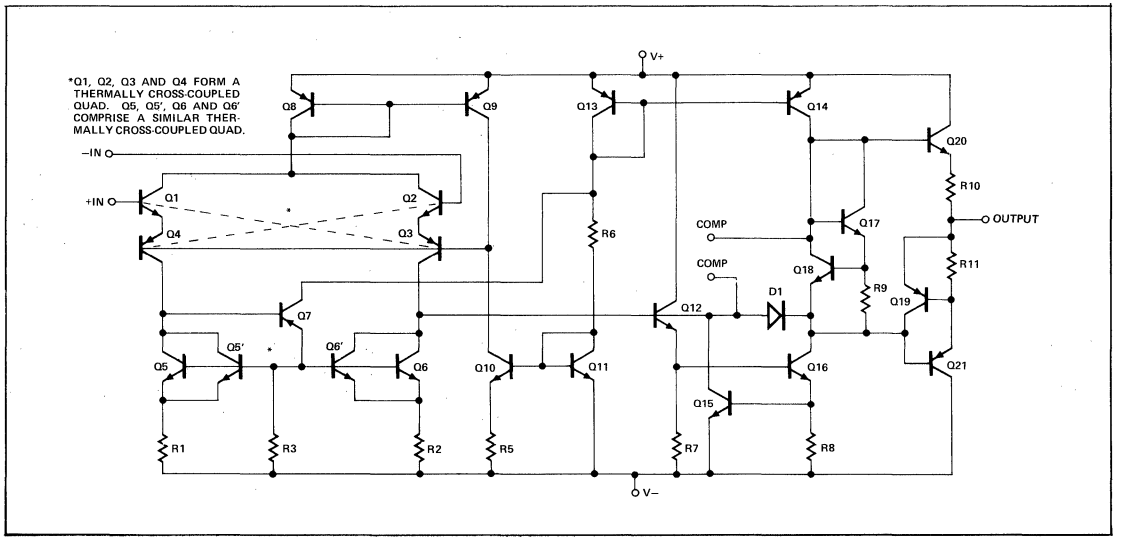
FEATURES

- **Excellent D.C. Input Specifications**
- **Fits Standard 748, 101 and 777 Sockets**
- **Low Noise** ..... **0.65 μV_{p-p}**
- **Low Drift (TCV_{OS})** ..... **8 $\mu V/°C$**
- **"Premium" 748 and 101 Replacement**
- **−25°C/ + 85°C and − 55°C/ + 125°C Models**
- **MIL-STD-883 Processing Available**
- **Silicon-Nitride Passivation**
- **Low Cost**

GENERAL DESCRIPTION

The OP-18 Series of High Performance General Purpose Operational Amplifiers provides significant improvements over industry-standard and "premium" 748, 101 and 777 types while maintaining pin-for-pin compatibility, ease of application, and low cost. Key specifications, such as V_{OS}, I_{OS}, I_B, CMRR, PSRR and A_{VO}, are guaranteed over the full operating temperature range. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process reduces "popcorn noise." A thermally-symmetrical input stage design provides low TCV_{OS}, TCI_{OS} and insensitivity to output load conditions. The OP-18 Series is ideal for upgrading existing designs where accuracy improvements are required and for eliminating special low drift or low noise selected types. OP-18's with MIL-STD-883 processing are available. The choice of the compensating capacitor allows the user to tailor slew rate, open loop bandwidth and maximum undistorted output swing for the application.

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±22V
Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply Voltage
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range
OP-18A, OP-18B, OP-18C ..... −55°C to +125°C
OP-18E, OP-18F, OP-18G ..... −25°C to +85°C
DICE Junction Temperature (T_j) ..... −65°C to +150°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 60 Sec.) ..... 300°C

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C

NOTES:
1. See table for maximum ambient temperature rating and derating factor.
2. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, $C_C = 30pF$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-18A MIN	OP-18A TYP	OP-18A MAX	OP-18B MIN	OP-18B TYP	OP-18B MAX	OP-18C MIN	OP-18C TYP	OP-18C MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.3	0.5	—	1.0	2.0	—	3.0	5.0	mV
Input Offset Current	I_{OS}		—	0.5	5.0	—	1.0	6.0	—	5.0	25	nA
Input Bias Current	I_B		—	18	50	—	20	60	—	30	100	nA
Input Resistance-Differential Mode	R_{in}	(Note 2)	3.8	7.5	—	2.3	7.0	—	1.0	5.0	—	MΩ
Input Voltage Range	IVR		—	±13.0	—	—	±13.0	—	—	±13.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$, $R_S \leq 20k\Omega$	85	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 20V$, $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	μV/V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±13.0	—	±12.0	±13.0	—	±12.0	±13.0	—	V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	100	250	—	50	200	—	25	150	—	V/mV
Power Consumption	P_d	$V_O = 0V$	—	50	90	—	50	90	—	50	90	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.65	—	—	0.65	—	—	0.65	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_o = 10Hz$	—	25	—	—	25	—	—	25	—	$nV/\sqrt{Hz}$
		$f_o = 100Hz$	—	22	—	—	22	—	—	22	—	
		$f_o = 1000Hz$	—	21	—	—	21	—	—	21	—	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	12.8	—	—	12.8	—	—	12.8	—	pA_{p-p}
Input Noise Current Density	i_n	$f_o = 10Hz$	—	1.4	—	—	1.4	—	—	1.4	—	$pA/\sqrt{Hz}$
		$f_o = 100Hz$	—	0.7	—	—	0.7	—	—	0.7	—	
		$f_o = 1000Hz$	—	0.4	—	—	0.4	—	—	0.4	—	
Slew Rate	SR	(Note 1)	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	V/μs
Slew Rate	SR	$C_C = 3pF$ (Note 1)	2.0	4	—	2.0	4	—	2.0	4	—	V/μs
Large Signal Bandwidth		$V_O = 20V_{p-p}$ (Note 1)	4.0	8.0	—	4.0	8.0	—	4.0	8.0	—	kHz
Closed Loop Bandwidth	BW	$A_{VCL} = +1.0$ (Note 1)	0.8	1.3	—	0.8	1.3	—	0.8	1.3	—	MHz
Risetime	t_r	$A_V = +1$, $V_{IN} = 50mV$ (Note 1)	—	200	300	—	200	300	—	200	300	ns
Overshoot	Os	(Note 1)	—	5	15	—	5	15	—	5	15	%

NOTE:
1. Sample tested.
2. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

				OP-18A			OP-18B			OP-18C			
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$		—	0.5	1.0	—	1.4	3.0	—	3	6.0	mV
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	(Note 1)	—	2.0	8.0	—	4.0	10.0	—	8	20	µV/°C
Input Offset Current	I_{OS}			—	1.0	10.0	—	2.0	12.0	—	5	50	nA
Average Input Offset Current Drift	TCI_{OS}		(Note 1)	—	7.5	75	—	15	150	—	30	300	pA/°C
Input Bias Current	I_B			—	30	100	—	40	120	—	50	200	nA
Input Voltage Range	IVR			—	±13.0	—	—	±13.0	—	—	13.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$		80	95	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 20V$ $R_S \leq 20k\Omega$		—	10	60	—	30	100	—	100	150	µV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$		50	100	—	25	60	—	25	60	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$		±12.0	±13.0	—	±12.0	±13.0	—	±10.0	±13.0	—	V

NOTE:
1. Sample tested.

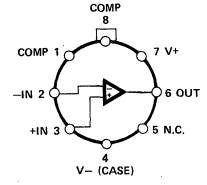
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	PACKAGE HERMETIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
0.5	OP18AJ*	OP18AZ*	MIL
0.5	OP18EJ	OP18EZ	IND
2.0	OP18BJ*	OP18BZ*	MIL
2.0	OP18FJ	OP18FZ	IND
5.0	OP18CJ*	OP18CZ*	MIL
5.0	OP18GJ	OP18GZ	IND

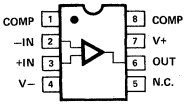
* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



TO-99 (J-Suffix)



8 PIN HERMETIC DIP (Z-Suffix)

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, $C_C = 30pF$, unless otherwise noted.

			OP-18E			OP-18F			OP-18G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.3	0.5	—	1.0	2.0	—	3.0	5.0	mV
Input Offset Current	I_{OS}		—	0.5	5.0	—	1.0	6.0	—	5.0	25	nA
Input Bias Current	I_B		—	18	50	—	20	60	—	30	100	nA
Input Resistance-Differential Mode	R_{in}	(Note 2)	3.8	7.5	—	2.3	7.0	—	1.0	5.0	—	MΩ
Input Voltage Range	IVR		—	±13.0	—	—	±13.0	—	—	±13	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	μV/V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±13.0	—	±12.0	±13.0	—	±12.0	±13.0	—	V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	100	250	—	50	200	—	25	150	—	V/mV
Power Consumption	P_d	$V_O = 0V$	—	50	90	—	50	90	—	50	90	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.65	—	—	0.65	—	—	0.65	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_o = 10Hz$ $f_o = 100Hz$ $f_o = 1000Hz$	— — —	25 22 21	— — —	— — —	25 22 21	— — —	— — —	25 22 21	— — —	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	12.8	—	—	12.8	—	—	12.8	—	pA_{p-p}
Input Noise Current Density	i_n	$f_o = 10Hz$ $f_o = 100Hz$ $f_o = 1000Hz$	— — —	1.4 0.7 0.4	— — —	— — —	1.4 0.7 0.4	— — —	— — —	1.4 0.7 0.4	— — —	pA/√Hz
Slew Rate	SR	(Note 1)	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	V/μs
Slew Rate	SR	$C_C = 3pF$ (Note 1)	2.0	4	—	2.0	4	—	2.0	4	—	V/μs
Large Signal Bandwidth		$V_O = 20V_{p-p}$ (Note 1)	4.0	8.0	—	4.0	8.0	—	4.0	8.0	—	kHz
Closed Loop Bandwidth	BW	$A_{VCL} = +1.0$ (Note 1)	0.8	1.3	—	0.8	1.3	—	0.8	1.3	—	MHz
Risetime	t_r	$A_V = +1$ $V_{IN} = 50mV$ (Note 1)	—	200	300	—	200	300	—	200	300	ns
Overshoot	Os	(Note 1)	—	5	15	—	5	15	—	5	15	%

NOTE:

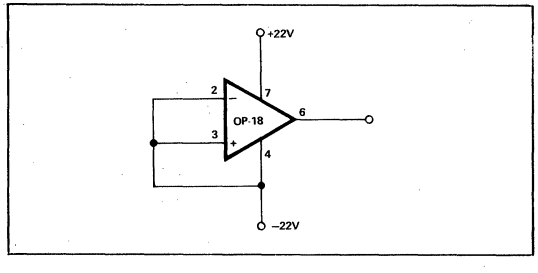
1. Sample tested.
2. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25°C \leq T_A \leq +85°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-18E MIN	OP-18E TYP	OP-18E MAX	OP-18F MIN	OP-18F TYP	OP-18F MAX	OP-18G MIN	OP-18G TYP	OP-18G MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.4	1.0	—	1.2	3.0	—	3	6.0	mV
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$ (Note 1)	—	2.0	8.0	—	4.0	10.0	—	8	20	µV/°C
Input Offset Current	I_{OS}		—	0.7	10	—	1.4	12	—	5	50	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	7.5	120	—	15	250	—	70	500	pA/°C
Input Bias Current	I_B		—	22	100	—	25	120	—	50	200	nA
Input Voltage Range	IVR		—	±13.0	—	—	±13.0	—	—	13.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	80	100	—	80	90	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	µV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	—	25	60	—	15	25	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±13.0	—	±12.0	±13.0	—	±10.0	±13.0	—	V

NOTE:
1. Sample tested.

BURN-IN CIRCUIT

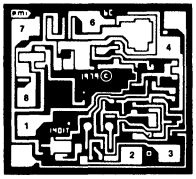


RECOMMENDED COMPENSATION VALUES

CLOSED LOOP GAIN	COMPENSATION CAPACITOR (C_C)
1000	1pF
100	2pF
10	5pF
1	30pF

NOTE:
C_C is connected between pins 1 and 8.

DICE CHARACTERISTICS



DIE SIZE 0.044 × 0.041 inch

1. COMPENSATION
2. INVERTING INPUT
3. NON-INVERTING INPUT
4. V −
6. OUTPUT
7. V +
8. COMPENSATION

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$ for N, G and GR, unless otherwise noted.

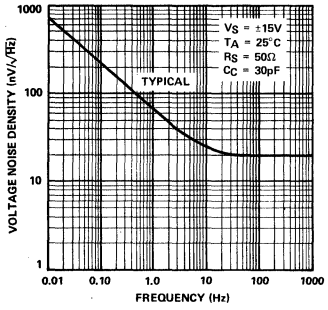
PARAMETER	SYMBOL	CONDITIONS	OP-18N LIMITS	OP-18G LIMITS	OP-18GR LIMITS	UNITS
Input Offset Voltage Range	V_{OS}	$R_S \leq 20k\Omega$	0.5	2.0	5.0	mV MAX
Input Offset Current	I_{OS}		5.0	6.0	25	nA MAX
Input Bias Current	I_B		50	60	100	nA MAX
Input Voltage Range	IVR		±13	±13	±13	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	80	70	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	60	100	150	μV/V MAX
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±12	±12	V MIN
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	100	50	25	V/mV MIN
Power Consumption	P_d	$V_O = 0V$	90	90	90	mW MAX

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

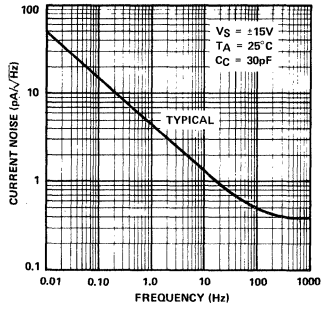
PARAMETER	SYMBOL	CONDITIONS	OP-18N TYP	OP-18G TYP	OP-18GR TYP	UNITS
Input Resistance Differential Mode	R_{in}		7.5	7.0	5.0	MΩ
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	0.65	0.65	0.65	μV_{p-p}
Input Noise Voltage Density	e_n	$f_o = 10Hz$ $f_o = 100Hz$ $f_o = 1000Hz$	25 22 21	25 22 21	25 22 21	$nV/\sqrt{Hz}$
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	12.8	12.8	12.8	pA_{p-p}
Input Noise Current Density	i_n	$f_o = 10Hz$ $f_o = 100Hz$ $f_o = 1000Hz$	1.4 0.7 0.4	1.4 0.7 0.4	1.4 0.7 0.4	$pA/\sqrt{Hz}$
Slew Rate	SR		0.5	0.5	0.5	V/μS
Slew Rate	SR	$C_C = 3pF$	4	4	4	V/μS
Large Signal Bandwidth		$V_O = 20V_{p-p}$	8.0	8.0	8.0	kHz
Closed Loop Bandwidth	BW	$A_{VCL} = +1.0$	1.3	1.3	1.3	MHz
Risetime	t_r	$A_V = +1$ $V_{IN} = 50mV$	200	200	200	nS
Overshoot	Os		5	5	5	%
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	2.0	4.0	8.0	μV/°C
Average Input Offset Current Drift	TCI_{OS}		7.5	15	70	pA/°C

TYPICAL PERFORMANCE CURVES

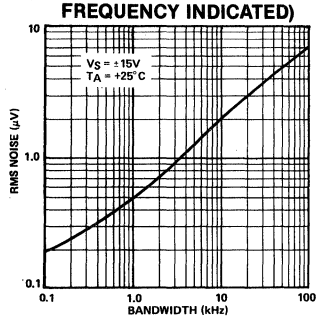
INPUT SPOT NOISE VOLTAGE vs FREQUENCY



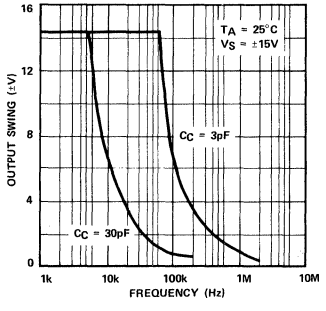
INPUT SPOT NOISE CURRENT vs FREQUENCY



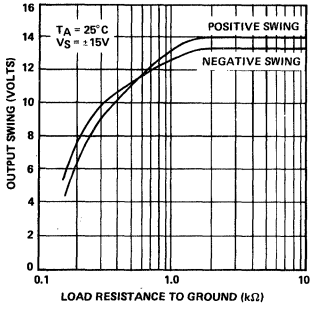
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1 Hz TO FREQUENCY INDICATED)



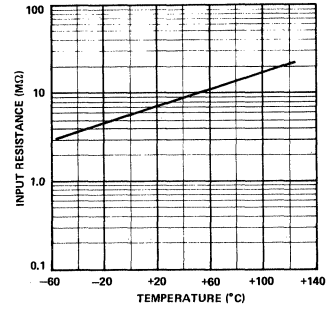
MAXIMUM UNDISTORTED OUTPUT vs FREQUENCY



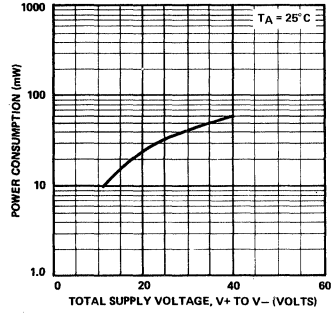
OUTPUT VOLTAGE vs LOAD RESISTANCE



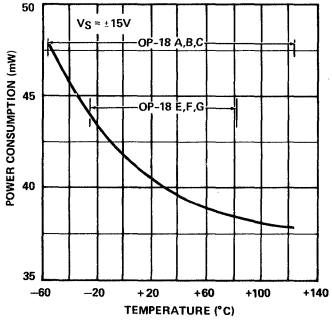
INPUT RESISTANCE vs TEMPERATURE



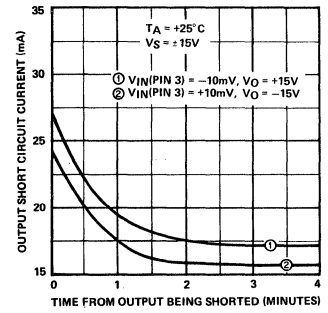
POWER CONSUMPTION vs POWER SUPPLY



POWER CONSUMPTION vs TEMPERATURE

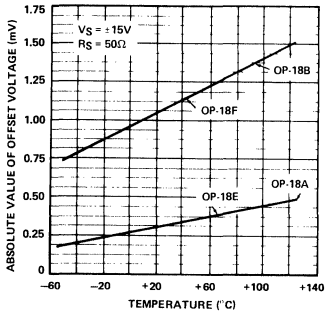


OUTPUT SHORT-CIRCUIT CURRENT vs TIME

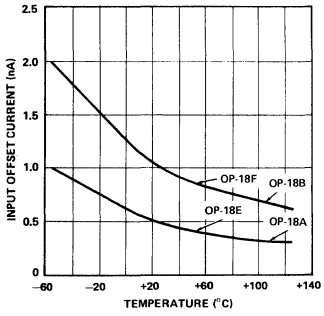


TYPICAL PERFORMANCE CURVES

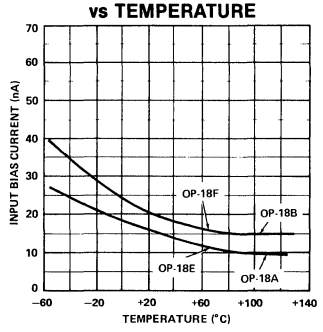
UNTRIMMED OFFSET VOLTAGE vs TEMPERATURE



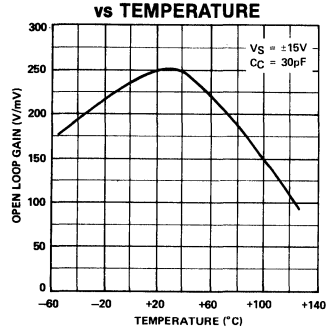
INPUT OFFSET CURRENT vs TEMPERATURE



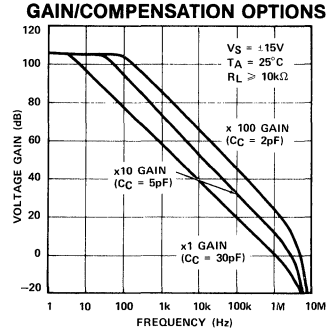
INPUT BIAS CURRENT vs TEMPERATURE



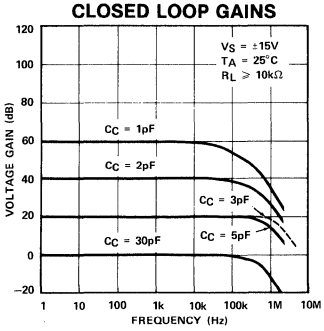
OPEN LOOP GAIN vs TEMPERATURE



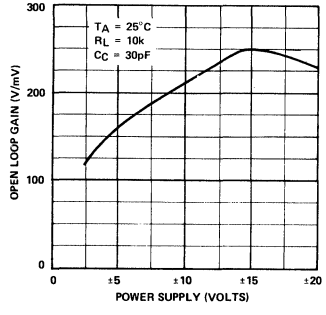
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY FOR VARIOUS GAIN/COMPENSATION OPTIONS



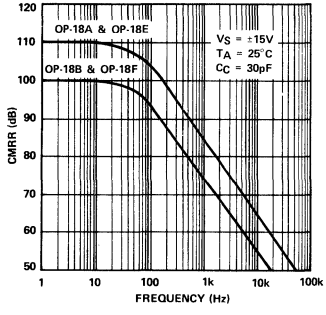
FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS



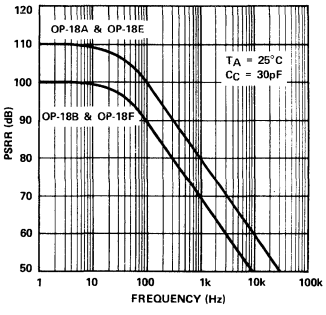
OPEN LOOP GAIN vs POWER SUPPLY VOLTAGE



CMRR vs FREQUENCY



PSRR vs FREQUENCY



OP-20

MICROPOWER PRECISION OPERATIONAL AMPLIFIER

SINGLE OR DUAL SUPPLY

FEATURES

- **Low Supply Current** **40μA**
- **Single Supply Operation** ..... **+3V to +30V**
- **Dual Supply Operation** ..... **±1.5V to ±15V**
- **Low Input Offset Voltage** **55μV**
- **Low Input Offset Voltage Drift** ..... **0.75μV/°C**
- **High Common Mode Input Range** ... **V− to V+ (−1.5V)**
- **High CMRR and PSRR** **110dB**
- **High Open Loop Gain** **126dB**
- **±30V Input Overvoltage Protection**
- **No External Components Required** ..... **Easy to Use**
- **Single Chip Monolithic Construction**
- **741 Pinout and Nulling**

GENERAL DESCRIPTION

The OP-20 is a monolithic precision micropower operational amplifier that can be used either in single or dual supply operation. Offset voltages as low as 250μV maximum and offset voltage drifts as low as 1.5μV/° C maximum are available with supply currents ranging between 45μA and 95μA maximum. Common-mode input voltage range includes ground to accommodate low, ground-referenced inputs from strain gauges or thermocouples. The OP-20 pinout and offset nulling technique is identical to the industry standard 741 device, offering an instant system upgrade in many applications. The monolithic construction makes the OP-20 ideal for use in hybrid designs, replacing devices such as the LM108, LM112, LM4250, ICL8021 and others.

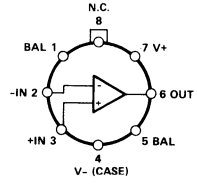
ORDERING INFORMATION †

T_A = 25°C V_{OS} MAX (μV)	PACKAGE TO-99 8-PIN	PACKAGE HERMETIC DIP 8-PIN	PACKAGE PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
250	OP20BJ*	OP20BZ*		MIL
250	OP20FJ	OP20FZ		IND
250			OP20FP	COM
500	OP20CJ*	OP20CZ*		MIL
500	OP20GJ	OP20GZ		IND
500			OP20GP	COM
1000	OP20HJ	OP20HZ	OP20HP	COM

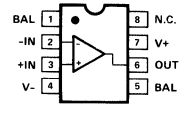
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number.

†All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS

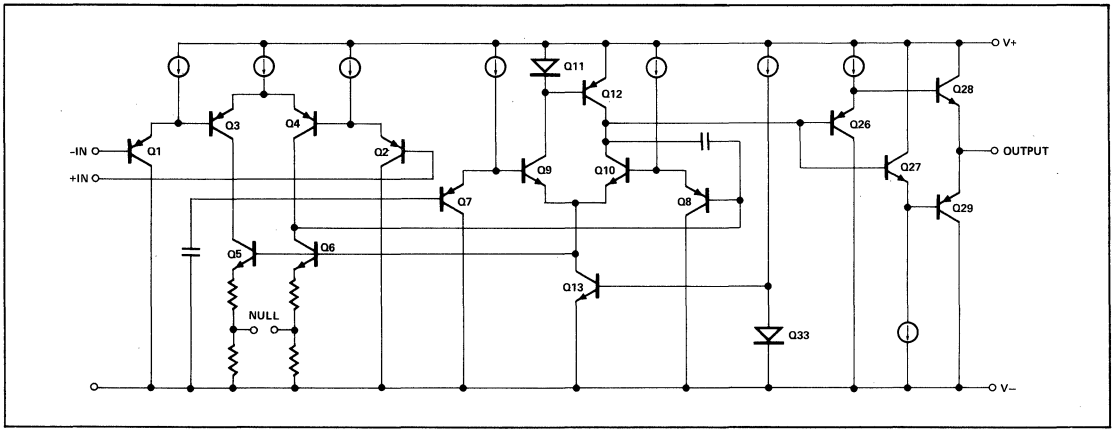


TO-99
(J-Suffix)



EPOXY B MINI-DIP
(P-Suffix)
AND
8-PIN HERMETIC DIP
(Z-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±18V
Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply Voltage
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range
J and Z Packages ..... -65°C to + 150°C
P Package ..... -65°C to + 125°C
Operating Temperature Range
OP-20B, OP-20C (J or Z package) .... −55°C to +125°C
OP-20F, OP-20G (J or Z package) ..... −25°C to +85°C
OP-20FP, OP-20GP, OP-20HP
OP-20HJ, OP-20HZ ..... 0°C to +70°C
Lead Temperature (Soldering, 60 Sec.) ..... 300°C
DICE Junction Temperature ..... −65°C to +150°C

NOTES:
1. See table for maximum ambient temperature rating and derating factor.
2. Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Plastic DIP	36°C	5.6mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C

ELECTRICAL CHARACTERISTICS at V_S = ± 2.5V to ± 15V, T_A = + 25°C, unless otherwise noted.

			OP-20B/F			OP-20C/G			OP-20H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	V_S = ± 15V	—	55	250	—	150	500	—	300	1000	μV
Input Offset Current	I_{OS}		—	0.15	1.5	—	0.2	2.5	—	0.3	4.0	nA
Input Bias Current	I_B		—	12	25	—	14	30	—	16	40	nA
Input Voltage Range	IVR	V+ = +5V, V− = 0V	+4.0/−0.2	—	—	+4.0/−0.2	—	—	+3.8/−0.2	—	—	V
		V_S = ±15V	+14.0/−15.2	—	—	+14.0/−15.2	—	—	+13.8/−15.2	—	—	
Common Mode Rejection Ratio	CMRR	V+ = +5V, V− = 0V, 0V ≤ V_{CM} ≤ + 3.5V, V_S = ±15V	95	105	—	90	95	—	85	90	—	dB
		−15V ≤ V_{CM} ≤ + 13.5V	100	110	—	94	105	—	90	100	—	
Power Supply Rejection Ratio	PSRR	V_S = ±2.5V to ±15V; and V− = 0V, V+ = 5V to 30V	—	4	6	—	6	10	—	10	32	μV/V
Large Signal Voltage Gain	A_{VO}	V+ = +5V, V− = 0V (Note 1), V_S = ±15V, R_L = 25kΩ	500	1000	—	300	800	—	—	500	—	V/mV
			1000	2000	—	800	2000	—	500	1000	—	
Output Voltage Swing	V_O	V+ = 5V, V− = 0V, R_L = 100kΩ	0.6	—	4.1	0.7	—	4.1	0.8	—	4.0	V
		V_S = ±15V, R_L = 25kΩ	±14.1	—	—	±14.1	—	—	±14.0	—	—	
Closed Loop Bandwidth	BW	A_{VCL} = +1.0, R_L = 10kΩ	—	100	—	—	100	—	—	100	—	kHz
Slew Rate	SR	V_S = ±15V, R_L = 25kΩ	—	0.05	—	—	0.05	—	—	0.05	—	V/μs
Supply Current	I_{SY}	V_S = ±2.5V, no load	—	40	55	—	44	63	—	45	70	μA
		V_S = ±15V, no load	—	55	80	—	57	85	—	60	95	

NOTES:
1. Sample tested.

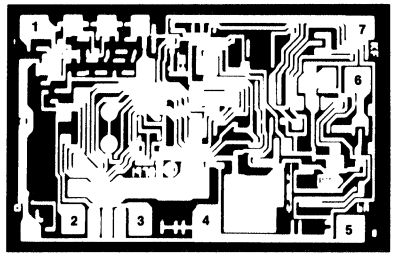
ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55°C \le T_A \le +125°C$ for OP-20BJ/BZ and OP-20CJ/CZ, $-25°C \le T_A \le +85°C$ for OP-20FJ/FZ and OP-20GJ/GZ, and $0°C \le T_A \le +70°C$ for OP-20FP, OP-20GP, OP-20HP, OP-20HZ and OP-20HJ, unless otherwise noted.

			OP-20B/F			OP-20C/G			OP-20H			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Average Input Offset Voltage Drift (Note 1)	TCV_{OS} TCV_{OSn}	Unnulled Nulled, $R_p = 10k\Omega$	—	0.75	1.5	—	1.0	3.0	—	1.5	7.0	μV/°C
Input Offset Voltage	V_{OS}	$V_S = \pm 15V$	—	155	400	—	250	800	—	500	1700	μV
Input Offset Current	I_{OS}		—	0.5	2.5	—	1.0	3.5	—	1.5	5.0	nA
Input Bias Current	I_B		—	12	27	—	14	33	—	16	45	nA
Input Voltage Range	IVR	V+ = +5V, V− = 0V	+3.9/−0.1	—	—	+3.9/−0.1	—	—	+3.7/−0.1	—	—	V
		$V_S = \pm 15V$	+13.9/−15.0	—	—	+13.9/−15.0	—	—	+13.7	—	—	
Common Mode Rejection Ratio (Note 3)	CMRR	V+ = +5V, V− = 0V $0V \le V_{CM} \le 3.3V$	90	100	—	85	90	—	80	85	—	dB
		$V_S = \pm 15V$ $-15V \le V_{CM} \le 13.3V$	96	110	—	90	105	—	85	100	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	4	10	—	6	18	—	10	32	μV/V
		V− = 0V, V+ = 5V to 30V	—	4	10	—	6	18	—	10	57	
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 25k\Omega$	500	700	—	400	600	—	250	400	—	V/mV
Output Voltage Swing (Note 2)	V_O	V+ = 5V, V− = 0V, $R_L = 10k\Omega$	+0.8	—	+4.0	+0.9	—	+3.9	+1.0	—	+3.8	V
		$V_S = \pm 15V$, $R_L = 25k\Omega$	±14.0	—	—	±13.9	—	—	±13.9	—	—	
Supply Current	I_{SY}	$V_S = \pm 2.5V$, no load or +5V, 0V	—	50	65	—	53	75	—	55	85	μA
		$V_S = \pm 15V$, no load	—	64	95	—	68	100	—	72	115	

NOTES:

1. Sample tested
2. $R_L = 50k$ for $-55°C \le T_A \le +125°C$, $V_S = \pm 15V$.
3. BJ and CJ grades tested to $V_{CM} \ge 150mV$ above negative supply voltage.

DICE CHARACTERISTICS



DIE SIZE 0.068 × 0.045 inch

1. BALANCE
2. INVERTING INPUT
3. NON-INVERTING INPUT
4. V−
5. BALANCE
6. OUTPUT
7. V+

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$ unless otherwise noted.

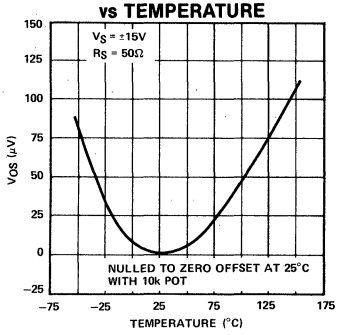
PARAMETER	SYMBOL	CONDITIONS	OP-20N LIMIT	OP-20G LIMIT	OP-20GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		300	600	1000	µV MAX
Input Offset Current	I_{OS}		1.5	2.5	4.0	nA MAX
Input Bias Current	I_B		20	25	30	nA MAX
Input Voltage Range	IVR	V+ = +5V, V− = 0V	4.0/−0.2	4.0/−0.2	3.8/−0.2	V MIN
		$V_S = \pm 15V$	+14.0/−15.2	+14.0/−15.2	+13.8/−15.2	
Common Mode Rejection Ratio	CMRR	V+ = +5V, V− = 0V, $0V \le V_{CM} \le +3.5V$	95	90	85	dB MIN
		$V_S = \pm 15V$, $-15V \le V_{CM} \le \pm 13.5V$	100	94	90	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ V− = 0V, V+ = +5V to +30V	6	10	32	µV/V MAX
Large Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$	1000	800	500	V/mV MIN
Output Voltage Swing	V_O	$R_L = 100k\Omega$, V+ = +5V, V− = 0V	0.7/4.2	0.8/4.1	0.9/4.0	V MIN
		$R_L = 25k\Omega$, $V_S = \pm 15V$	±14.1	± 14.1	± 14.0	
Supply Current No Load	I_{SY}	$V_S = \pm 2.5V$	45	50	60	µA MAX
		$V_S = \pm 15V$	65	70	80	

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

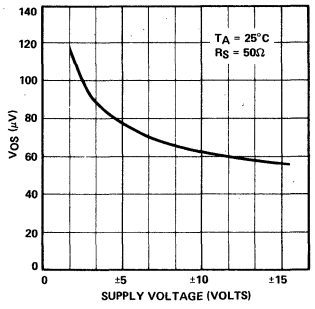
PARAMETER	SYMBOL	CONDITIONS	OP-20N TYPICAL	OP-20G TYPICAL	OP-20GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	Unnulled	1.0	1.5	2.5	µV/°C
	TCV_{OSn}	Nulled, $R_P = 10k\Omega$	1.0	1.5	2.5	
Large Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$	2000	2000	1000	V/mV

TYPICAL PERFORMANCE CURVES

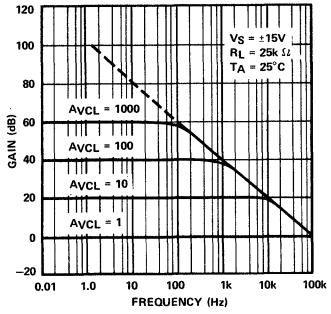
TRIMMED OFFSET VOLTAGE vs TEMPERATURE



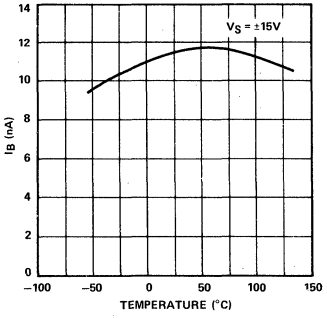
INPUT OFFSET VOLTAGE vs POWER SUPPLY VOLTAGE



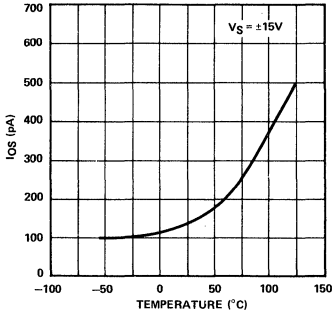
CLOSED LOOP GAIN vs FREQUENCY



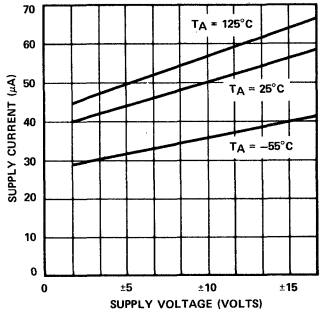
INPUT BIAS CURRENT vs TEMPERATURE



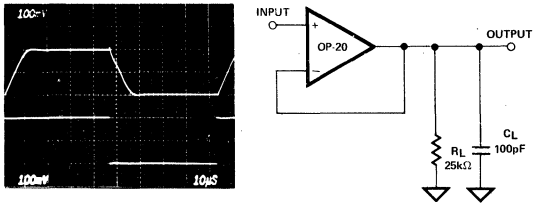
INPUT OFFSET CURRENT vs TEMPERATURE



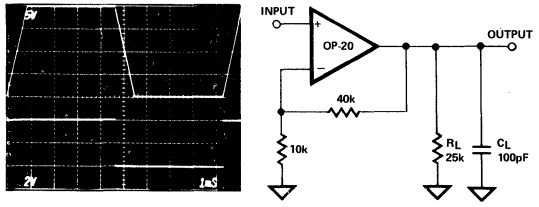
SUPPLY CURRENT vs SUPPLY VOLTAGE



SMALL-SIGNAL TRANSIENT RESPONSE

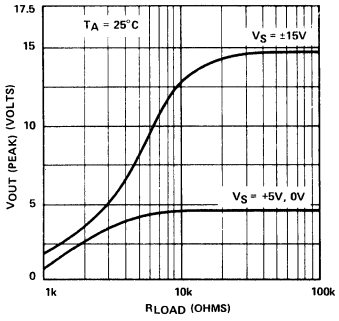


LARGE-SIGNAL TRANSIENT RESPONSE

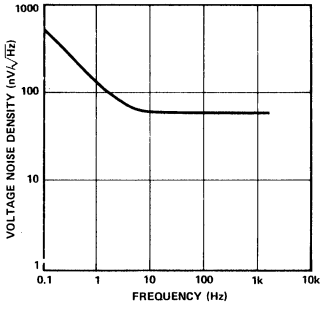


TYPICAL PERFORMANCE CURVES

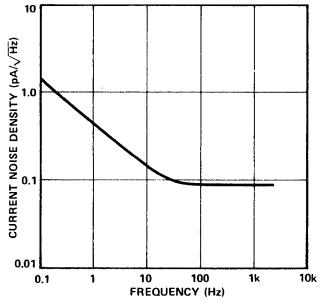
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISISTANCE



INPUT VOLTAGE NOISE DENSITY vs FREQUENCY

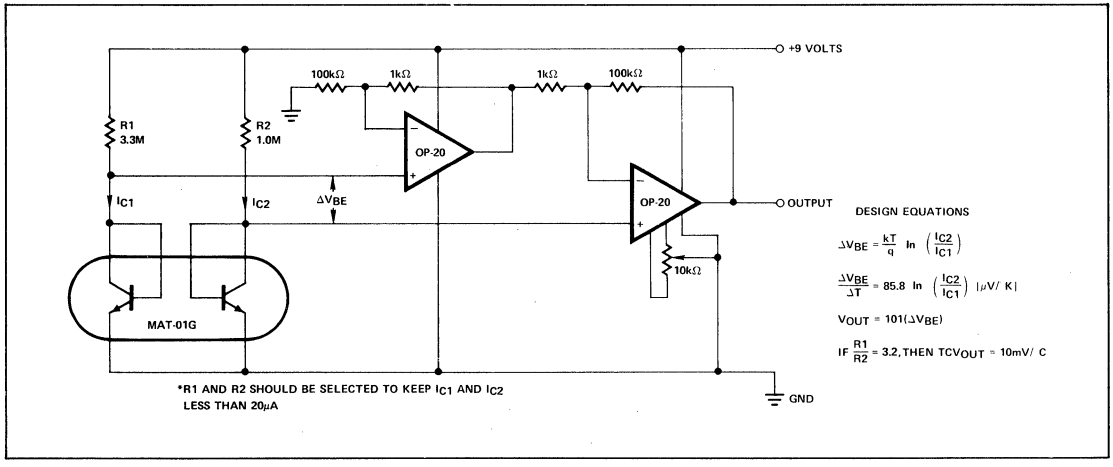


INPUT CURRENT NOISE DENSITY vs FREQUENCY



TYPICAL APPLICATIONS

TEMPERATURE SENSOR



OP-21

HIGH-SPEED LOW POWER PRECISION OPERATIONAL AMPLIFIER

FEATURES

- Low Supply Current 170μA
- High Slew Rate 0.25V/μs
- Dual Supply Operation ..... ±1.5V to ±15V
- Low Input Offset Voltage 40μV
- Low Input Offset Voltage Drift ..... 0.5μV/°C
- High Common Mode Input Range ..... V− (+0.5V) to V+ (−1.5V)
- High CMRR and PSRR 110dB
- High Open Loop Gain 2000V/mV
- ±30V Input Overvoltage Protection
- No External Components Required ..... Easy to Use
- Single Chip Monolithic Construction
- 741 Pinout and Nulling
- 125° C Temperature Tested DICE

ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (μV)	PACKAGE TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
100	OP21AJ*	OP21AZ*		MIL
100	OP21EJ	OP21EZ	OP21EP	IND
200	OP21BJ*	OP21BZ*		MIL
200	OP21FJ	OP21FZ	OP21FP	IND
500	OP21GJ	OP21GZ	OP21GP	IND

* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

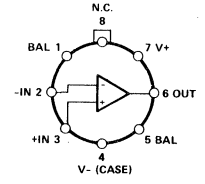
† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

GENERAL DESCRIPTION

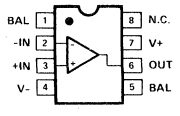
The OP-21 is a precision low-power operational amplifier offering the benefits of low offset voltage and high slew rate with the advantages of low power. Supply ranges of ±1.5V to ±15V allow a wide range of applications.

Two military temperature range models and three industrial temperature range models are available in TO-99 CANs and 8-Pin Hermetic DIPs. Industrial temperature range models are also available in 8-Pin Plastic DIPs. For quads see OP-421.

PIN CONNECTIONS

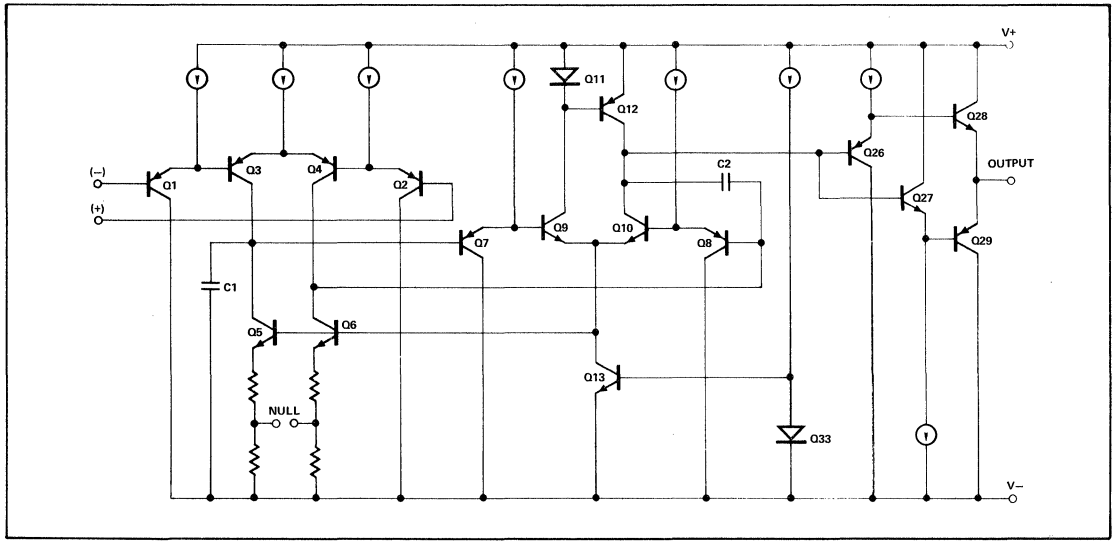


TO-99 (J-Suffix)



EPOXY B MINI-DIP (P-Suffix) & 8-PIN HERMETIC DIP (Z-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±18V
Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply Voltage
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range
J and Z Packages ..... −65°C to +125°C
P Package ..... −65°C to +125°C
Operating Temperature Range
OP-21A, OP-21B ..... −55°C to +125°C
OP-21E, OP-21F, OP-21G ..... −25°C to +85°C
DICE Junction Temperature ..... −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec.) ..... 300°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.
2. Absolute maximum ratings apply to both packaged parts and dice, unless otherwise noted.

	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Plastic Dip (P)	36°C	5.6mW/°C
8-Pin Hermetic Dip (Z)	75°C	6.7mW/°C

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$ and $T_A = +25°C$, unless otherwise noted.

			OP-21A/E			OP-21B/F			OP-21G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$V_S = \pm 15V$	—	40	100	—	150	200	—	300	500	μV
Input Offset Current	I_{OS}		—	0.6	4	—	0.8	5	—	1.2	6	nA
Input Bias Current	I_B		—	50	100	—	60	120	—	70	150	nA
Input Voltage Range	IVR	$V_S = \pm 15V$	−14.5 +14.0	— —	— —	−14.5 +14.0	— —	— —	−14.5 +13.8	— —	— —	V
Common Mode Rejection Ratio	CMRR	$V_S = \pm 15V$, no load $-14.5V \le V_{CM} \le 13.5V$	100	110	—	90	105	—	84	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$, no load	—	2	6	—	4	10	—	10	32	μV/V
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 10k\Omega$	1000	2000	—	500	1500	—	500	1000	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 15V$, $R_L = 10k\Omega$	−13.7 +14.0	— —	— —	−13.7 +13.9	— —	— —	−13.6 +13.8	— —	— —	V
Slew Rate	SR	$C_L = 100pF$, $R_L = 25k\Omega$	—	0.25	—	—	0.25	—	—	0.25	—	V/μs
Closed Loop Bandwidth	BW	$A_{VCL} = +1$, $R_L = 10k\Omega$	—	600	—	—	600	—	—	600	—	kHz
Supply Current	I_{SY}	$V_S = \pm 2.5V$, No load $V_S = \pm 15V$, No load	— —	170 230	230 300	— —	180 235	275 360	— —	190 250	300 420	μA

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55°C \leq T_A \leq +125°C$ for OP-21A and OP-21B, $-25°C \leq T_A \leq +85°C$ for Op-21E, OP-21F and OP-21G, unless otherwise noted.

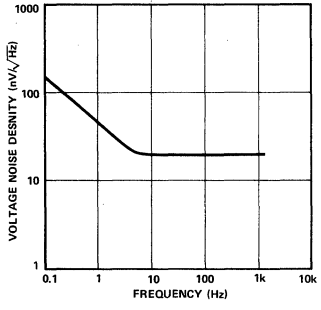
			OP-21A/E			OP-21B/F			OP-21G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Average Input Offset Voltage Drift (Note 1)	TCV_{OS} TCV_{OSn}	Unnulled Nulled	—	0.5	1.0	—	1.0	2.0	—	2.5	5.0	μV/°C
Input Offset Voltage	V_{OS}		—	75	200	—	200	500	—	500	1000	μV
Input Offset Current	I_{OS}		—	1.5	5	—	2.0	6	—	2.0	8	nA
Input Bias Current	I_B		—	50	110	—	60	130	—	70	165	nA
Input Voltage Range	IVR		−14.3 +13.5	— —	— —	−14.3 +13.5	— —	— —	−14.3 +13.5	— —	— —	V
Common Mode Rejection Ratio	CMRR	No load, $V_S = \pm 15V$, $-14.5V \leq V_{CM} \leq 13.5V$	96	105	—	86	100	—	80	95	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$, no load	—	4	10	—	6	18	—	18	57	μV/V
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 20k\Omega$	500	1500	—	250	1300	—	250	1000	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 15V$, $R_L = 20k\Omega$	−13.5 +13.8	— —	— —	−13.5 +13.7	— —	— —	−13.5 +13.6	— —	— —	V
Supply Current	I_{SY}	$V_S = \pm 2.5V$, No load $V_S = \pm 15V$, No load	— —	205 275	275 360	— —	215 285	330 430	— —	230 300	360 500	μA

NOTE:

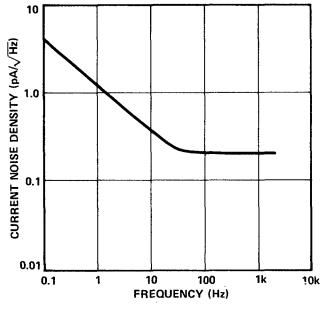
1. Sample tested.

NOISE CHARACTERISTICS

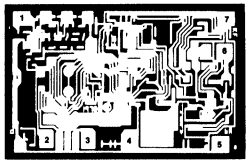
INPUT SPOT NOISE VOLTAGE vs FREQUENCY



INPUT SPOT NOISE CURRENT vs FREQUENCY



DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



DIE SIZE 0.068 × 0.045 inch

1. BALANCE
2. INVERTING INPUT
3. NON-INVERTING INPUT
4. V–
5. BALANCE
6. OUTPUT
7. V+

See Section 2 for additional Dice information.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$ for OP-21N, OP-21G and OP-21GR devices; $T_A = +125°C$ for OP-21NT and OP-21GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-21NT LIMIT	OP-21N LIMIT	OP-21GT LIMIT	OP-21G LIMIT	OP-21GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		200	100	500	200	500	μV MAX
Input Offset Current	I_{OS}		4	4	5	5	6	nA MAX
Input Bias Current	I_B		100	100	120	120	150	nA MAX
Input Voltage Range	IVR		−14.3 +13.5	−14.5 +14.0	−14.3 +13.5	−14.5 +14.0	−14.5 +13.8	V MIN
Common Mode Rejection Ratio	CMRR	No Load CMVR = IVR	96	100	86	90	84	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ No Load	10	6	18	10	32	μV/V MAX
Large Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$	500	1000	250	500	500	V/mV MIN
Output Voltage Swing	V_O	$R_L = 10k\Omega$	−13.5 +13.8	−13.7 +14.0	−13.5 +13.7	−13.7 +13.9	−13.6 +13.8	V MIN
Supply Current	I_{SY}		300	300	360	360	420	μA MAX

NOTE: For 25° C characteristics of NT & GT devices, see N & G characteristics respectively.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-21NT TYP	OP-21N TYP	OP-21GT TYP	OP-21G TYP	OP-21GR TYP	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	Unnulled	0.5	0.5	1	1	2.5	μV/°C
Nulled Input Offset Voltage Drift	TCV_{OSn}	Nulled, $R_p = 10k\Omega$	0.5	0.5	1	1	2.5	μV/°C
Large Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$	2000	2000	1500	1500	1000	V/mV
Slew Rate	SR	$R_L = 25k\Omega$ $C_L = 100pF$	.25	.25	.25	.25	.25	V/μs
Closed Loop Bandwidth	BW	$A_{VCL} = +1$ $R_L = 10k\Omega$	600	600	600	600	600	kHz

OP-24/OP-34
ULTRA-LOW NOISE OPERATIONAL AMPLIFIERS

FEATURES

- **Ultra Low Noise ..... 5nV/$\sqrt{Hz}$ at 30Hz Maximum**
- **High Speed ..... Slew Rates to 17V/μs**
- **Low V_{OS} ..... 170μV Maximum**
- **Low I_b and I_{OS} ..... 90nA Maximum**
- **Double Buffer Output ..... $\pm$11.5 Volts into 600Ω**
- **Socket Compatible with 5534**

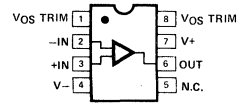
GENERAL DESCRIPTION

The OP-24 and OP-34 op amps offer a unique combination of low noise, wide bandwidth, and high gain without sacrifice of input offset performance. Input bias current is under 85nA and maximum input offset voltage is only 170μV. In addition, a double-buffered output stage can deliver $\pm$11.5V into a 600Ω load.

This excellent performance in a low cost, plastic minidip package makes the OP-24 and OP-34 an ideal choice for use in professional and consumer audio equipment; such as phono, tape, and microphone pre-amplifiers. The guarantees in maximum noise and minimum slew rates assure high performance on a production basis. In many AC amplifier applications, the low DC offsets allow *direct coupling* between gain stages. The usual coupling capacitors can often be eliminated when using the PMI OP-24/OP-34.

The OP-24 is pin compatible with the 5534 and can often be used to upgrade designs through direct replacement of the 5534. For high gain applications (A_V>5),the decompensated OP-34 is recommended. AC performance can be improved substantially through use of the OP-34 for high-gain applications. These two amplifiers, the OP-24 and OP-34, offer excellent AC performance for audio, active filter, and data conversion applications, while retaining the low DC offsets which are characteristic of PMI products.

ORDERING INFORMATION & PIN CONNECTIONS

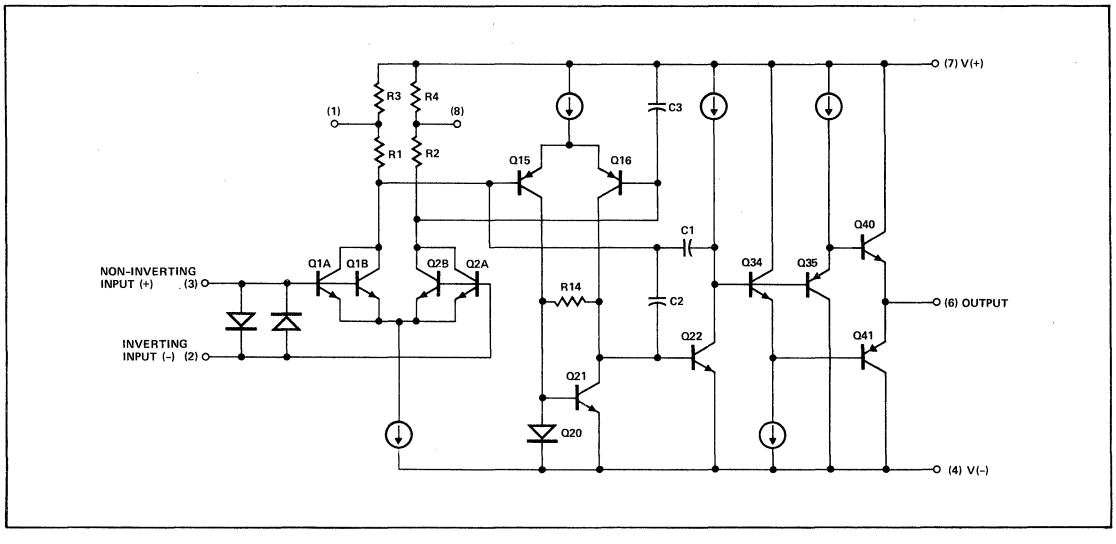


EPOXY B MINI-DIP
(P SUFFIX)

OP-24GP
OP-34GP*

*Available May 1982

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Internal Power Dissipation (Note 1) 500mW
Input Voltage (Note 3) ..... ±22V
Output Short Circuit Duration ..... Indefinite
Differential Input Voltage (Note 2) ..... ±0.7V
Differential Input Current (Note 2) ..... ±25mA
Storage Temperature Range ..... −65°C to +125°C
Operating Temperature Range ..... 0°C to +70°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
DICE Junction Temperature ..... - 65° C to + 150° C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
8-Pin Epoxy Mini-Dip (P)	36°C	5.6mW/°C

2. The OP-24/34's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
3. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-24 MIN	OP-24 TYP	OP-24 MAX	OP-34 MIN	OP-34 TYP	OP-34 MAX	UNITS
Input Offset Voltage	V_{OS}		—	50	170	—	50	170	μV
Input Offset Current	I_{OS}		—	12	90	—	12	90	nA
Input Bias Current	I_B		—	±15	±85	—	±15	±85	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.1	—	—	0.1	—	μVp-p
Input Noise Voltage Density	e_n	f_o = 10Hz (Note 1)	—	3.7	9.5	—	3.7	9.5	nV/√Hz
		f_o = 30Hz (Note 1)	—	3.3	5.0	—	3.3	5.0	
		f_o = 1000Hz (Note 1)	—	3.2	4.5	—	3.2	4.5	
Input Noise Current Density	i_n	f_o = 10Hz	—	1.9	—	—	1.9	—	pA/√Hz
		f_o = 30Hz	—	1.1	—	—	1.1	—	
		f_o = 1000Hz	—	0.45	—	—	0.45	—	
Input Resistance-Differential Mode	R_{IN}	(Note 2)	0.8	4	—	0.8	4	—	MΩ
Input Resistance-Common Mode	R_{INCM}		—	2	—	—	2	—	GΩ
Input Voltage Range	IVR		±11.0	±12.3	—	±11.0	±12.3	—	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±11V	100	120	—	100	120	—	dB
Power Supply Rejection Ratio	PSSR	V_S = ±4V to ±18V	—	2	20	—	2	20	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	50	500	—	50	500	—	V/mV
		$R_L \geq 1k\Omega$, V_O = ±10V	—	500	—	—	500	—	
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±11.5	±13.5	—	±11.5	±13.5	—	V
		$R_L \geq 600\Omega$	±10.0	±11.5	—	±10.0	±11.5	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 2)	1.7	2.8	—	11	17	—	V/μs
Gain Bandwidth Product OP-24	GBW	(Note 2)	5.0	8.0	—	—	—	—	MHz
Gain Bandwidth Product OP-34	GBW	f_o = 10kHz (Note 2)	—	—	—	45	63	—	MHz
		f_o = 1MHz	—	—	—	—	40	—	
Open Loop Output Resistance	R_O	V_O = 0, I_O = 0	—	70	—	—	70	—	Ω
Power Consumption	P_d	No Load	—	100	170	—	100	170	mW
Offset Adjustment Range		R_p = 10kΩ	—	±4.0	—	—	±4.0	—	mV

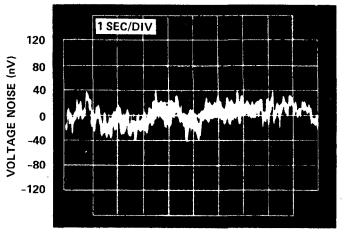
NOTES:
1. Sample Tested. 2. Guaranteed by Design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15$ V, $0° C \leq T_A \leq +70° C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-24 MIN	OP-24 TYP	OP-24 MAX	OP-34 MIN	OP-34 TYP	OP-34 MAX	UNITS
Input Offset Voltage	V_{OS}		—	55	250	—	55	250	μV
Input Offset Current	I_{OS}		—	20	135	—	20	135	nA
Input Bias Current	I_B		—	±25	±150	—	±25	±150	nA
Input Voltage Range	IVR		±10.5	±11.8	—	±10.5	±11.8	—	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±10V	96	118	—	96	118	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	—	20	32	—	20	32	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	30	400	—	30	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±11.0	±13.3	—	±11.0	±13.3	—	V

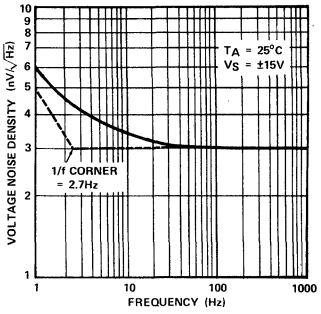
TYPICAL PERFORMANCE CURVES

LOW FREQUENCY NOISE

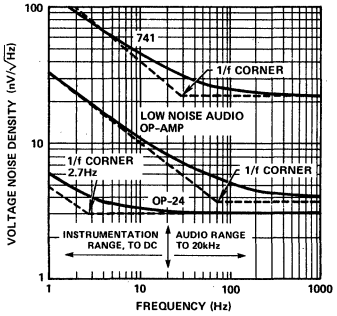


0.1Hz TO 10Hz PEAK-TO-PEAK NOISE

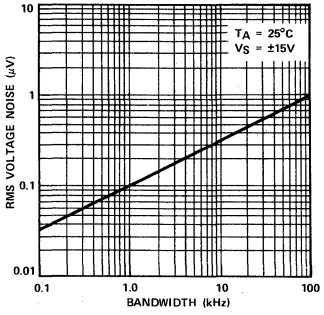
VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE



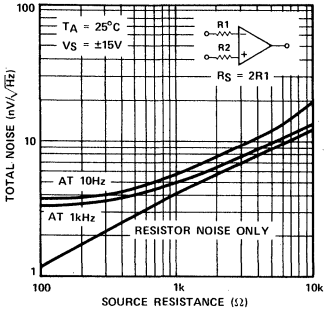
A COMPARISON OF OP AMP VOLTAGE NOISE SPECTRUMS



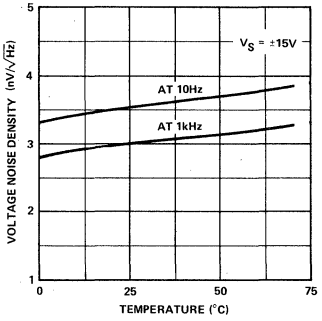
INPUT WIDEBAND VOLTAGE NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



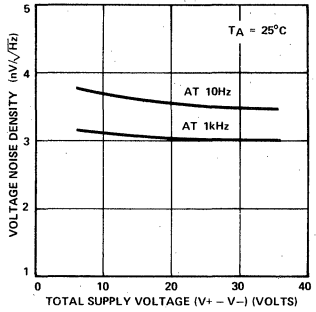
TOTAL NOISE vs SOURCE RESISTANCE



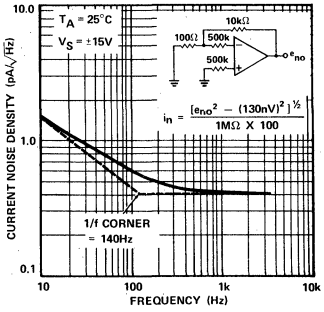
VOLTAGE NOISE DENSITY vs TEMPERATURE



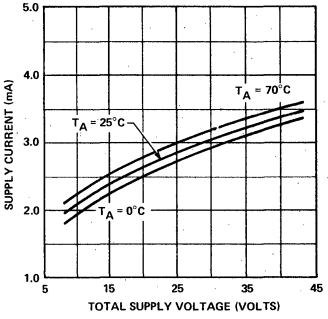
VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE



CURRENT NOISE DENSITY vs FREQUENCY

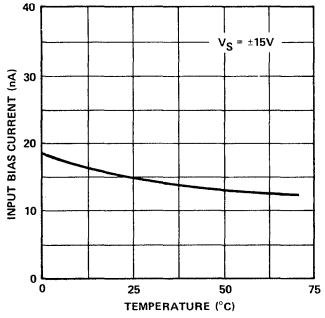


SUPPLY CURRENT vs SUPPLY VOLTAGE

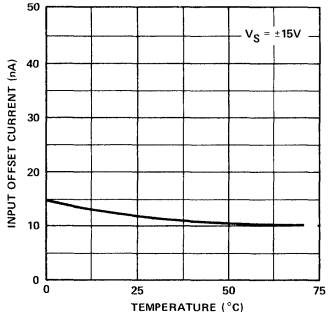


TYPICAL PERFORMANCE CURVES

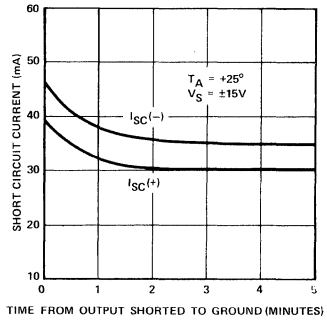
INPUT BIAS CURRENT vs TEMPERATURE



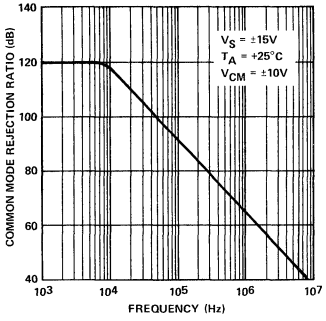
INPUT OFFSET CURRENT vs TEMPERATURE



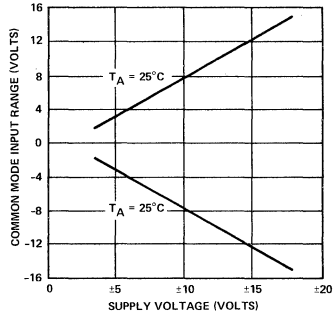
SHORT CIRCUIT CURRENT vs TIME



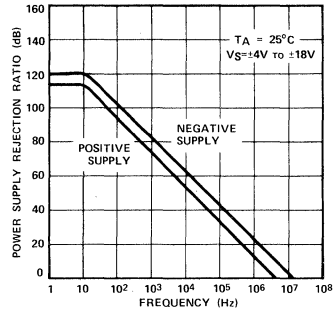
CMRR vs FREQUENCY



COMMON MODE INPUT RANGE vs SUPPLY VOLTAGE

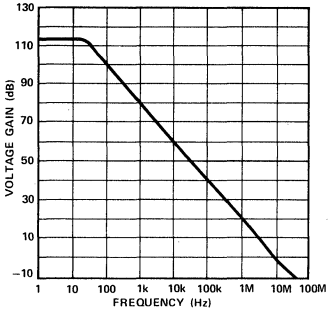


PSRR vs FREQUENCY

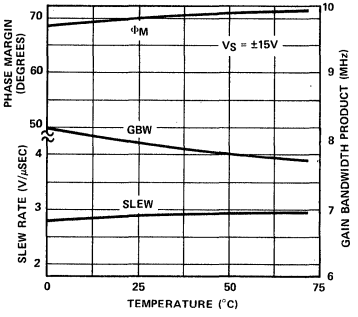


OP-24 ONLY, TYPICAL PERFORMANCE CURVES

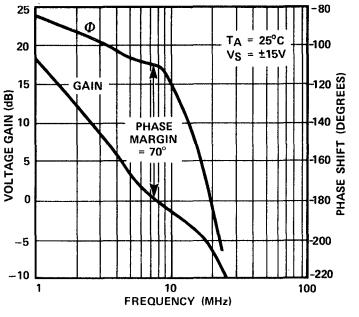
OPEN-LOOP GAIN vs FREQUENCY



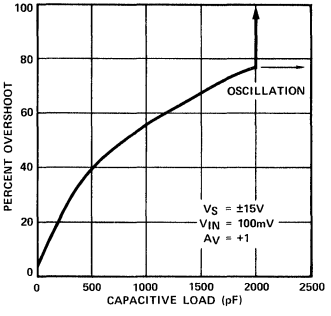
SLEW RATE, GAIN BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE



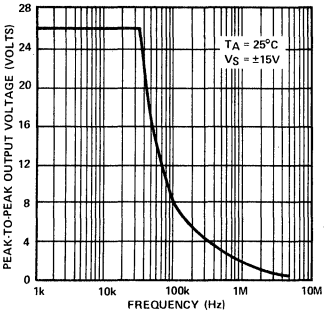
GAIN, PHASE SHIFT vs FREQUENCY



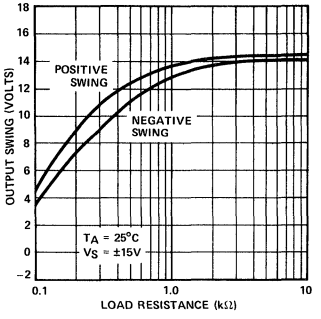
SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD



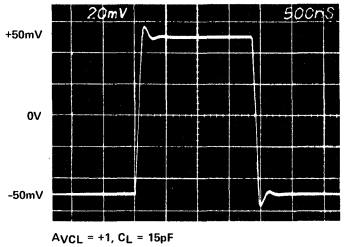
MAXIMUM UNDISTORTED OUTPUT vs FREQUENCY



MAXIMUM OUTPUT SWING vs RESISTIVE LOAD

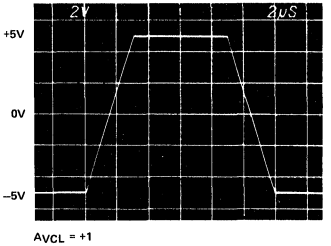


SMALL-SIGNAL TRANSIENT RESPONSE



AVCL = +1, CL = 15pF
VS = ±15V
TA = 25°C

LARGE-SIGNAL TRANSIENT RESPONSE

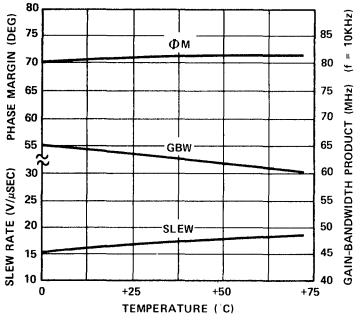


AVCL = +1
VS = ±15V
TA = 25°C

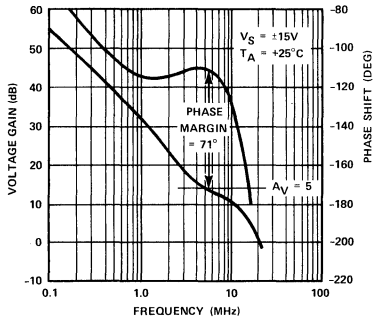
OP-34 ONLY, TYPICAL PERFORMANCE CURVES

$A_{VCL} \geq 5$ MINIMUM

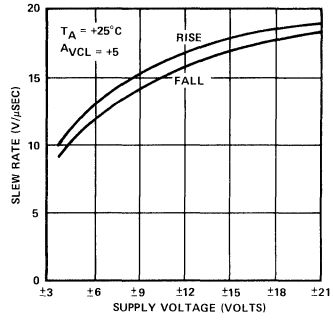
SLEW RATE, GAIN BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE



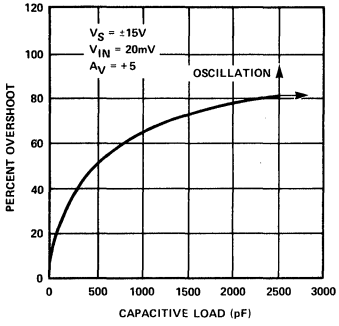
GAIN, PHASESHIFT vs FREQUENCY



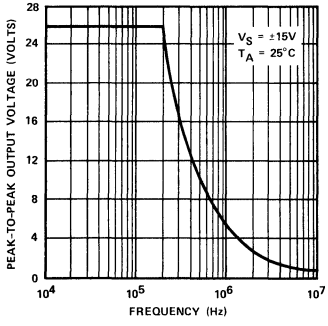
SLEW RATE vs SUPPLY VOLTAGE



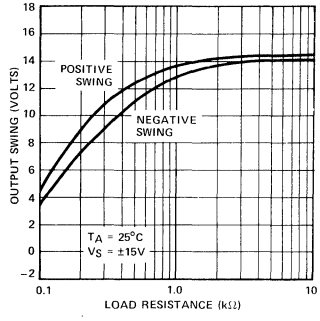
SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD



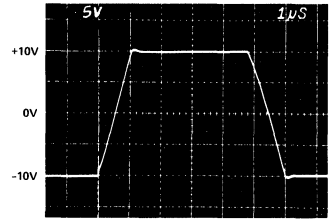
MAXIMUM UNDISTORTED OUTPUT vs FREQUENCY



MAXIMUM OUTPUT SWING vs RESISTIVE LOAD

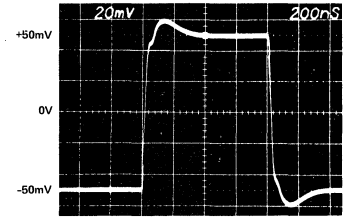


LARGE-SIGNAL TRANSIENT RESPONSE



$V_S = \pm 15V$
$A_V = +5V$
$T_A = +25°C$

SMALL-SIGNAL TRANSIENT RESPONSE



$V_S = \pm 15V$
$A_V = +5V$
$T_A = +25°C$
$C_L = 25pF$

APPLICATIONS INFORMATION

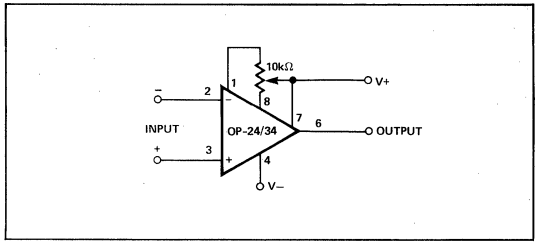
The OP-24/34 series of devices may be inserted directly in 5534 sockets without the removal of external compensating or nulling components. While the nulling circuit which is typically used for the 5534 differs from the preferred OP-24/34 nulling circuit, both will allow the user to null out the initial V_{OS} of the OP-24/34.

The OP-24/34 may also be used directly in unnulled 741 applications. In nulled 741 applications the OP-24/34 may be used after the nulling circuitry is removed or properly modified as shown in offset nulling circuit diagram.

The OP-24 should be used in circuits where the closed-loop gain is less than five. For maximum bandwidth and slew rate in circuits with gains greater than five, the OP-34 is the recommended device.

The OP-24/34 provides stable operation with large load capacitance and ± 10 Volt output swings. The OP-24 may be directly coupled into loads of up to 2000 pf and the OP-34 into loads of up to 2500 pf. For capacitive loads exceeding these values, a 50Ω decoupling resistor is recommended.

OFFSET NULLING CIRCUIT



OPTIMIZING LINEARITY

Best linearity can be obtained by designing for the minimum output current required for the application. High gain and excellent linearity can be achieved by operating the op amp within an output current range of ±10mA.

COMMENTS ON NOISE MEASUREMENTS

The extremely low noise of the OP-24 and OP-34 implies that its precise measurement is a difficult task. In order to realize the 80nV peak-to-peak noise specification of the op amp in the 0.1 Hz to 10 Hz frequency range, the following constraints have to be observed:

(1) The device has to be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically 4μV due to its chip temperature increasing 14 to 20° C from the moment the power supplies are turned on. In the 10sec measurement interval these temperature-induced effects can easily exceed tens of nanovolts.

(2) For similar reasons, the device has to be well shielded from air currents to eliminate the possibility of thermoelectric effects in excess of a few nanovolts invalidating the measurements.

(3) Sudden motion in the vicinity of the device can also "feedthrough" to increase the observed noise.

(4) The test time to measure 0.1 Hz to 10 Hz noise should not exceed 10 sec. As shown in the noise tester frequency response curve the 0.1 Hz corner is defined by only one zero. The test time of 10 sec acts an additional zero to eliminate noise contributions from the frequency band below 0.1 Hz.

A noise-voltage density test is recommended when measuring noise on a large number of units. A 10 Hz noise-voltage density measurement will correlate well with a 0.1 Hz-to-10 Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

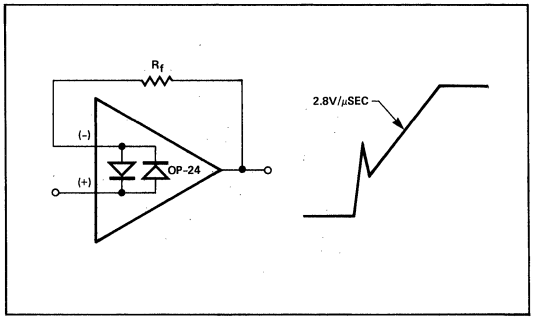
UNITY GAIN BUFFER APPLICATIONS (OP-24 ONLY)

When $R_f \leq 100\Omega$ and the input is driven with a fast, large signal pulse (>1V), the output waveform will look as shown in the pulsed operation diagram.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short circuit protection, will be drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20$mA at 10V) and the amplifier stays in its active mode and a smooth transition will occur.

As with all operational amplifiers, when $R_f > 2k\Omega$ a pole will be created with R_f and the amplifier's input capacitance (8pF), creating additional phase shift and reducing the phase margin. A small capacitor (20 to 50pF) in parallel with R_f will eliminate this problem.

PULSED OPERATION



AUDIO APPLICATIONS

The following applications information has been abstracted from Electronic Design magazine and updated. The authors are G. Erdi, T. J. Schwartz, S. Bernardi of Precision Monolithics, Inc. and Walter Jung, an independent audio consultant.

FIGURE 1

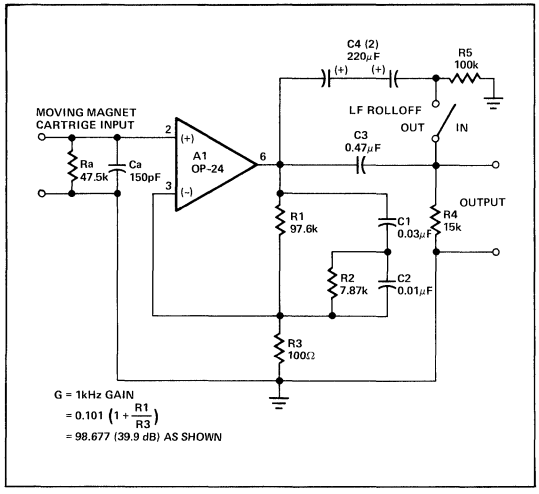


Figure 1 is an example of a phono pre-amplifier circuit using the OP-24 for A_1; R_1-R_2-C_1-C_2 form a very accurate RIAA network with standard component values. The popular method to accomplish RIAA phono equalization is to employ frequency-dependent feedback around a high-quality gain block. Properly chosen, an RC network can provide the three necessary time constants of 3180, 318 and 75 μs.[1]

For initial equalization accuracy and stability, precision metal-film resistors and film capacitors of polystyrene or polypropylene are recommended, since they have low voltage coefficients, dissipation factors, and dielectric absorption.[4] (High-K ceramic capacitors should be avoided here, though low-K ceramics—such as NPO types, which have excellent dissipation factors, and somewhat lower dielectric absorption—can be considered for small values or where space is at a premium.)

NOISE AND GAIN CONSIDERATIONS

The OP-24 brings a 3.2-nV/$\sqrt{Hz}$ voltage noise and 0.45-pA/$\sqrt{Hz}$ current noise to this circuit. To minimize noise from other sources, R_3 is set to a value of 100-Ω, which generates a voltage noise of 1.3 nV/$\sqrt{Hz}$. The noise increases the 3.2-nV/$\sqrt{Hz}$ of the amplifier by only 0.7 dB. With a 1-kΩ source, the circuit noise measures 63 dB below a 1-mV reference level, unweighted, in a 20-kHz noise bandwidth.

Gain (G) of the circuit at 1-kHz can be calculated by the expression:

$$G = 0.101\ (1 + \frac{R_1}{R_3}).$$

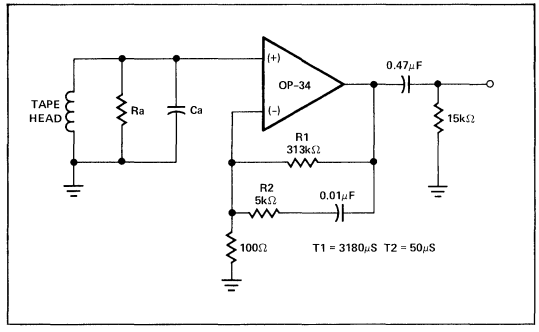
For the values shown, the gain is just under 100 (or 40 dB). Lower gains can be accommodated by increasing R_3, but gains higher than 40 dB will show more equalization errors, because of the 8-MHz gain-bandwidth of the OP-24.

This circuit is capable of very low distortion over its entire range, generally below 0.01% at levels up to 7-V rms. At 3-V output levels, it will produce less than 0.03% total harmonic distortion at frequencies up to 20 kHz.

Capacitor C_3 and resistor R_4 form a simple –6-dB-per-octave rumble filter, with a corner at 22 Hz. As an option, the switch-selected shunt capacitor C_4, a nonpolarized electrolytic, bypasses the low-frequency rolloff. Placing the rumble filter's high-pass action after the preamp has the desirable result of discriminating against the RIAA-amplified low-frequency noise components and pickup-produced low-frequency disturbances.

A preamplifier for NAB tape playback is similar to an RIAA phono preamp, though more gain is typically demanded, along with equalization requiring a heavy low—frequency boost. The circuit in Fig. 1 can be readily modified for tape use, as shown by Fig. 2.

FIGURE 2



While the tape-equalization requirement has a flat high-frequency gain above 3 kHz (T_2=50 μs), the amplifier need not be stabilized for unity gain. The decompensated OP-34 provides a greater bandwidth and slew rate. For many applications, the idealized time constants shown may require trimming of R_1 and R_2 to optimize frequency response for nonideal tape-head performance and other factors.[5]

The network values of the configuration yield a 50-dB gain at 1 kHz, and the dc gain is greater than 70 dB. Thus, the worst-case output offset is just over 500 mV. A single 0.47-μF output capacitor can block this level, without affecting the dynamic range.

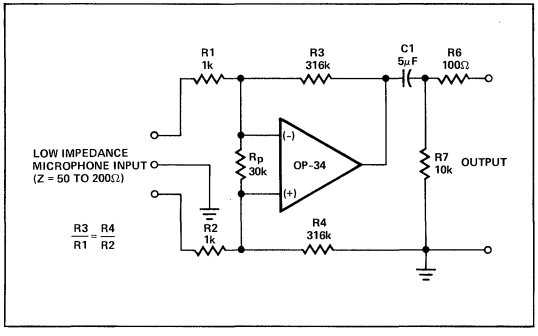
The tape head can be coupled directly to the amplifier input, since the worst-case bias current of 85 nA with a 400-mH, 100-μin. head (such as the PRB2H7K) will not be troublesome.

One potential tape-head problem is presented by amplifier bias-current transients which can magnetize a head. The OP-24 and OP-34 are free of bias-current transients, upon power up or power down. However, it is always advantageous to control the speed of power-supply rise and fall, to eliminate transients.[7]

In addition, the dc resistance of the head should be carefully controlled, and preferably below 1-kΩ. For this configuration, the bias-current-induced offset voltage can be greater than the 170-μV maximum offset, if the head resistance is not sufficiently controlled.

A simple but effective fixed-gain transformerless microphone preamp (Fig. 3) amplifies differential signals from low-impedance microphones by 50 dB, and has an input impedance of 2 kΩ. Because of the high working gain of the circuit, an OP-34 helps to preserve bandwidth, which will be 110 kHz. As the OP-34 is a decompensated device (minimum stable gain of 5), a dummy resistor, R_p, may be necessary, if the microphone is to be unplugged. Otherwise the 100% feedback from the open input may cause the amplifier to oscillate.

FIGURE 3

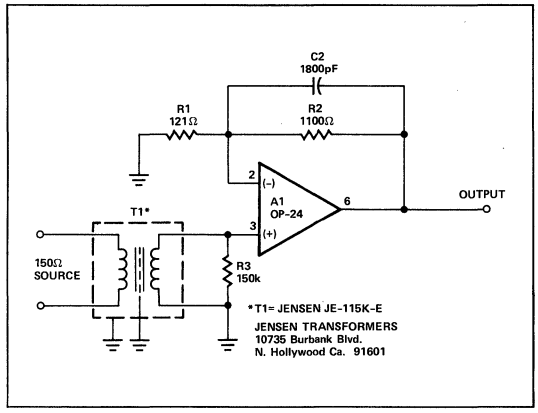


Common-mode input-noise rejection will depend upon the match of the bridge-resistor ratios. Either close-tolerance (0.1%) types should be used, or R_4 should be trimmed for best CMRR. All resistors should be metal-film types, for best stability and low noise.

Noise performance of this circuit is limited more by the input resistors R_1 and R_2 than by the op amp, as R_1 and R_2 each generate a 4-nV/$\sqrt{Hz}$ noise, while the op amp generates a 3.2-nV/$\sqrt{Hz}$ noise. The rms sum of these predominant noise sources will be about 6 nV/$\sqrt{Hz}$, equivalent to 0.9 μV in a 20-kHz noise bandwidth, or nearly 61 dB below a 1-mV input signal. Measurements confirm this predicted performance.

For applications demanding appreciably lower noise, a high-quality microphone-transformer-coupled preamp (Fig. 4) incorporates the internally compensated OP-24. T_1 is a JE-115K-E 150Ω/15-kΩ transformer which provides an optimum source resistance for the OP-24 device. The circuit has an overall gain of 40 dB, the product of the transformer's voltage setup and the op amp's voltage gain.

FIGURE 4



Gain may be trimmed to other levels if desired, by adjusting R_2 or R_1. Because of the low offset voltage of the OP-24, the output offset of this circuit will be very low, 1.7 mV or less, for a 40-dB gain. The typical output blocking capacitor can be eliminated in such cases, but is desirable for higher gains to eliminate switching transients.

Capacitor C_2 and resistor R_2 form a 2-μs time constant in this circuit, as recommended for optimum transient response by the transformer manufacturer. With C_2 in use, A_1 must have unity-gain stability. For situations where the 2-μs time constant is not necessary, C_2 can be deleted, allowing the faster OP-34 to be employed.

Some comment on noise is appropriate to understand the capability of this circuit. A 150-Ω resistor and R_1 and R_2 gain resistors connected to a noiseless amplifier will generate 220 nV of noise in a 20-kHz bandwidth, or 73 dB below a 1-mV reference level. Any practical amplifier can only approach this noise level; it can never exceed it. With the OP-24 and T_1 specified, the additional noise degradation will be close to 3.6 dB (or −69.5 dB referenced to 1 mV).

References

1. Lipshitz, S.P., "On RIAA Equalization Networks," *JAES*, Vol. 27, June 1979, p. 458-481.
2. Jung, W.G., *IC Op Amp Cookbook*, 2nd Ed., H.W. Sams and Company, 1980.
3. Jung, W.G., *Audio IC Op Amp Applications*, 2nd Ed., H.W. Sams and Company, 1978.
4. Jung, W.G., and Marsh, R.M., "Picking Capacitors," *Audio*, February & March, 1980.
5. Otala, M., "Feedback-Generated Phase Nonlinearity in Audio Amplifiers," London AES Convention, March 1980, preprint 1576.
6. Stout, D.F., and Kaufman, M., *Handbook of Operational Amplifier Circuit Design*, New York, McGraw Hill, 1976.

OP-27

ULTRA-LOW NOISE, PRECISION OPERATIONAL AMPLIFIER

FEATURES

- **Unprecedented Low Noise** ... 80nV p-p,0.1Hz to 10Hz; 3nV/$\sqrt{Hz}$ at 1kHz
- **Ultra Stable** ..... 0.2μV/° C; 0.2μV/Month
- **Fast** ..... 2.8V/μS Slew Rate; 8MHz Gain Bandwidth
- **Low V_{OS}** 10μV
- **Excellent CMRR** .... 126dB Over Input Voltage of ±11V
- **High Gain** ..... 1.8 Million
- **Fits 725, OP-07, OP-05, AD510, AD517 sockets**

GENERAL DESCRIPTION

The world's first triple threat Op Amp, the OP-27, offers the ideal features of precision, low noise and high speed in one monolithic device. This low-noise instrumentation Op Amp combines the exceptional DC performance of the OP-07 (V_{OS} of 10μV, TCV_{OS} of 2μV/° C) with a truly awesome noise performance (e_n = 3.5nV/$\sqrt{Hz}$ at 10Hz) and a remarkably low 1/f noise corner frequency (2.7Hz). The high-speed performance is assured by a gain-bandwidth product of 8MHz and a slew rate of 2.8Vμsec.

In addition, this device has a gain of 1.5M with 1kΩ load while consuming 3mA. The OP-27 also features an I_B of ±10nA and an I_{OS} of 7nA. These surprisingly low currents are realized through the use of a unique input bias current cancellation circuit which typically holds I_B and I_{OS} of ±20nA and 15nA resepectively, over the full military temperature range.

Other sources of input referred errors, such as PSRR and CMRR, are reduced by factors in excess of 120dB. These characteristics, coupled with long term drift of 0.2μV/month, allow the circuit designer to achieve performance levels previously attained by only the most complex and expensive hybrid or discrete designs.

Low cost, high volume production of OP-27 is achieved by electronic adjustment of an on-chip zener-zap offset trimming network during initial factory testing. This reliable and stable zener-zap trimming scheme has demonstrated its effectiveness over seven years of production history.

The OP-27 provides unparalleled performance for low noise, high accuracy amplification of very low level signals in transducer applications. Other applications include stable integrators, precision summing amplifiers for analog computation and test equipment, ultra-precise voltage threshold detectors, comparators, and audio circuits such as tape head and microphone preamplifiers.

The OP-27 is a direct replacement for 725, OP-06, OP-07 and OP-05 amplifiers; 741 types may be directly replaced by removing the 741's nulling potentiometer.

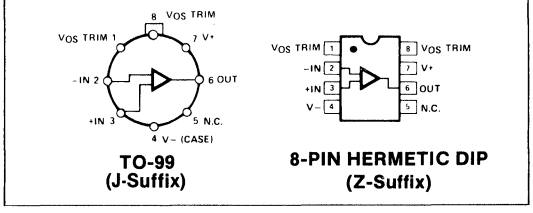
ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (μV)	PACKAGE TO-99 8-PIN	PACKAGE HERMETIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
25	OP27AJ*	OP27AZ*	MIL
25	OP27EJ	OP27EZ	IND
60	OP27BJ*	OP27BZ*	MIL
60	OP27FJ	OP27FZ	IND
100	OP27CJ*	OP27CZ*	MIL
100	OP27GJ	OP27GZ	IND

*Also available with MIL-STD-883B processing. To order add /883 as a suffix to the part number.

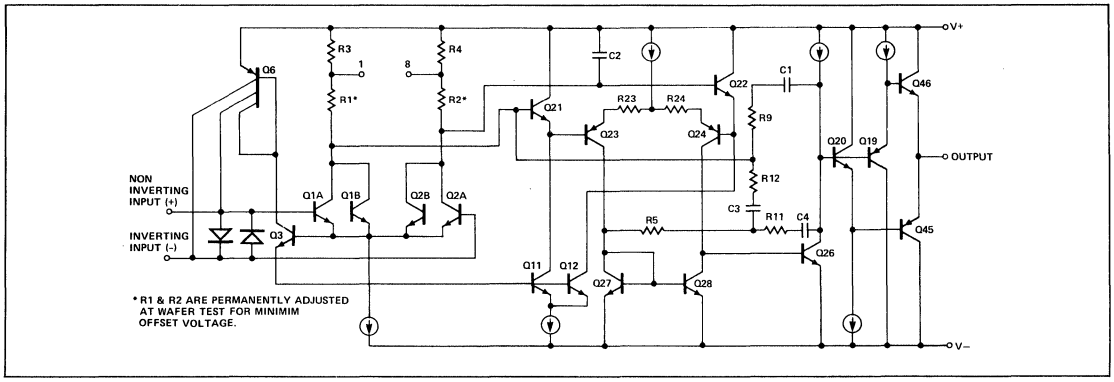
† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



TO-99 (J-Suffix) **8-PIN HERMETIC DIP (Z-Suffix)**

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage ..... ±22V
Internal Power Dissipation (Note 1) 500mW
Input Voltage (Note 3) ..... ±22V
Output Short Circuit Duration ..... Indefinite
Differential Input Voltage (Note 2) ..... ±0.7V
Differential Input Current (Note 2) ..... ±25mA
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range
OP-27A, OP-27B, OP-27C ..... −55°C to +125°C
OP-27E, OP-27F, OP-27G ..... −25°C to +85°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
DICE Junction Temperature ..... −65°C to +150°C

NOTES:
1. See table for maximum ambient temperature rating and derating factor.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic Dip (Z)	75°C	6.7mW/°C

2. The OP-27's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
3. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
4. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

			OP-27A/E			OP-27B/F			OP-27C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	–	10	25	–	20	60	–	30	100	μV
Long Term V_{OS} Stability	V_{OS}/Time	(Note 2)	–	0.2	1.0	–	0.3	1.5	–	0.4	2.0	μV/Mo
Input Offset Current	I_{OS}		–	7	35	–	9	50	–	12	75	nA
Input Bias Current	I_B		–	±10	±40	–	±12	±55	–	±15	±80	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3, 5)	–	0.08	0.18	–	0.08	0.18	–	0.09	0.25	μVp-p
Input Noise Voltage Density	e_n	f_o = 10Hz (Note 3)	–	3.5	5.5	–	3.5	5.5	–	3.8	8.0	nV/√Hz
		f_o = 30Hz (Note 3)	–	3.1	4.5	–	3.1	4.5	–	3.3	5.6	
		f_o = 1000Hz (Note 3)	–	3.0	3.8	–	3.0	3.8	–	3.2	4.5	
Input Noise Current Density	i_n	f_o = 10Hz (Note 3, 6)	–	1.7	4.0	–	1.7	4.0	–	1.7	–	pA/√Hz
		f_o = 30Hz (Note 3, 6)	–	1.0	2.3	–	1.0	2.3	–	1.0	–	
		f_o = 1000Hz (Note 3, 6)	–	0.4	0.6	–	0.4	0.6	–	0.4	0.6	
Input Resistance — Differential Mode	R_{IN}	(Note 4)	1.5	6	–	1.2	5	–	0.8	4	–	MΩ
Input Resistance — Common Mode	R_{INCM}		–	3	–	–	2.5	–	–	2	–	GΩ
Input Voltage Range	IVR		±11.0	±12.3	–	±11.0	±12.3	–	±11.0	±12.3	–	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 11V$	114	126	–	106	123	–	100	120	–	dB
Power Supply Rejection Ratio	PSSR	$V_S = \pm 4V$ to ±18V	—	1	10	—	1	10	—	2	20	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	1000	1800	–	1000	1800	–	700	1500	–	V/mV
		$R_L \geq 1k\Omega$, $V_O = \pm 10V$	800	1500	–	800	1500	–	–	1500	–	
(Note 4)	$R_L = 600\Omega$,	$V_O = \pm 1V$, $V_S = \pm 4V$	250	700	–	250	700	–	200	500	–	
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±13.8	–	±12.0	±13.8	–	±11.5	±13.5	–	V
		$R_L \geq 600\Omega$	±10.0	±11.5	–	±10.0	±11.5	–	±10.0	±11.5	–	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 4)	1.7	2.8	–	1.7	2.8	–	1.7	2.8	–	V/μs
Gain Bandwidth Prod.	GBW	(Note 4)	5.0	8.0	–	5.0	8.0	–	5.0	8.0	–	MHz
Open Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	–	70	–	–	70	–	–	70	–	Ω
Power Consumption	P_d	$V_O = 0$	–	90	140	–	90	140	–	100	170	mW
Offset Adjustment Range		$R_P = 10k\Omega$	–	±4.0	–	–	±4.0	–	–	±4.0	–	mV

NOTES:
1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed up.
2. Long Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5μV — refer to typical performance curve.
3. Sample tested.
4. Guaranteed by design.
5. See test circuit and frequency response curve for 0.1Hz to 10Hz tester.
6. See test circuit for current noise measurement.

ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

			OP-27A			OP-27B			OP-27C			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	(Note 1)	–	30	60	–	50	200	–	70	300	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSN}	(Note 2)	–	0.2	0.6	–	0.3	1.3	–	0.4	1.8	μV/°C
Input Offset Current	I_{OS}		–	15	50	–	22	85	–	30	135	nA
Input Bias Current	I_B		–	±20	±60	–	±28	±95	–	±35	±150	nA
Input Voltage Range	IVR		±10.3	±11.5	–	±10.3	±11.5	–	±10.2	±11.5	–	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	108	122	–	100	119	–	94	116	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	16	—	2	20	—	4	51	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	600	1200	–	500	1000	–	300	800	–	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±11.5	±13.5	–	±11.0	±13.2	–	±10.5	±13.0	–	V

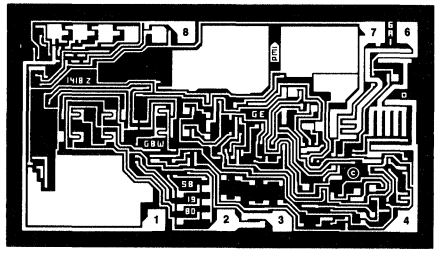
ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$, $-25°C \leq T_A \leq +85°C$, unless otherwise noted.

			OP-27E			OP-27F			OP-27G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}		–	20	50	–	40	140	–	55	220	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSN}	(Note 2)	–	0.2	0.6	–	0.3	1.3	–	0.4	1.8	μV/°C
Input Offset Current	I_{OS}		–	10	50	–	14	85	–	20	135	nA
Input Bias Current	I_B		–	±14	±60	–	±18	±95	–	±25	±150	nA
Input Voltage Range	IVR		±10.5	±11.8	–	±10.5	±11.8	–	±10.5	±11.8	–	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	110	124	–	102	121	–	96	118	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	15	—	2	16	—	2	32	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	750	1500	–	700	1300	–	450	1000	–	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±11.7	±13.6	–	±11.4	±13.5	–	±11.0	±13.3	–	V

NOTES:

1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E Grades Guaranteed Fully Warmed up.
2. The TCV_{OS} performance is within the specifications unnulled or when nulled with $R_P = 8k\Omega$ to $20k\Omega$.

DICE CHARACTERISTICS



DIE SIZE 0.054 X 0.096 inch

1. NULL
2. (–) INPUT
3. (+) INPUT
4. V–
6. OUTPUT
7. V+
8. NULL

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27N LIMIT	OP-27G LIMIT	OP-27GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	35	60	100	μV MAX
Input Offset Current	I_{OS}		35	50	75	nA MAX
Input Bias Current	I_B		±40	±55	±80	nA MAX
Input Voltage Range	IVR		±11.0	±11.0	±11.0	V MIN
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 11V$	114	106	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4V$ to $\pm 18V$	10	10	20	μV/V MAX
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $R_L \geq 1k\Omega$, $V_O = \pm 10V$	1000 800	1000 800	700 —	V/mV MIN
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	±12.0 ±10.0	±12.0 ±10.0	±11.5 ±10.0	V MIN
Power Consumption	P_d	$V_O = 0$	140	140	170	mW MAX

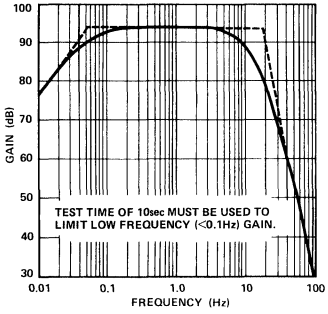
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27N TYPICAL	OP-27G TYPICAL	OP-27GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS} or TCV_{OSn}	Nulled or Unnulled $R_P = 8k\Omega$ to $20k\Omega$	0.2	0.3	0.4	μV/°C
Average Input Offset Current Drift	TCI_{OS}		80	130	180	pA/°C
Average Input Bias Current Drift	TCI_B		100	160	200	pA/°C
Input Noise Voltage Density	e_n	$f_O = 10Hz$ $f_O = 30Hz$ $f_O = 1000Hz$	3.5 3.1 3.0	3.5 3.1 3.0	3.8 3.3 3.2	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	$f_O = 10Hz$ $f_O = 30Hz$ $f_O = 1000Hz$	1.7 1.0 0.4	1.7 1.0 0.4	1.7 1.0 0.4	$pA/\sqrt{Hz}$
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	0.08	0.08	0.09	μVp-p
Slew Rate	SR	$R_L \geq 2k\Omega$	2.8	2.8	2.8	V/μs
Gain Bandwidth Product	GBW		8.0	8.0	8.0	MHz

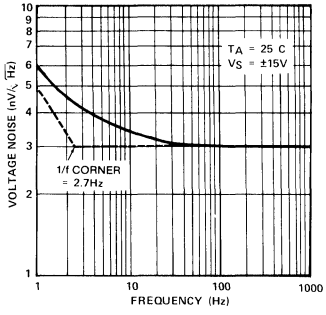
NOTE:
1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

TYPICAL PERFORMANCE CURVES

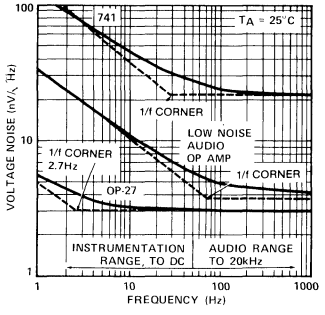
0.1Hz TO 10Hz p-p NOISE TESTER FREQUENCY RESPONSE



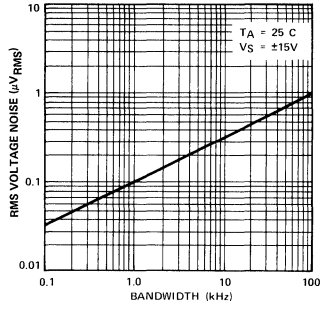
OP-27 VOLTAGE NOISE vs FREQUENCY



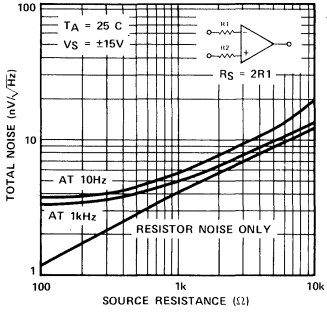
A COMPARISON OF OP AMP VOLTAGE NOISE SPECTRUMS



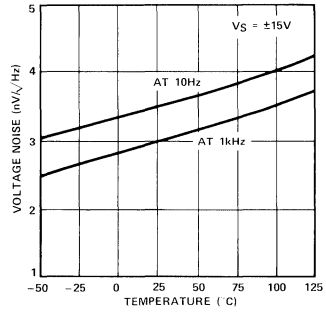
INPUT WIDEBAND VOLTAGE NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



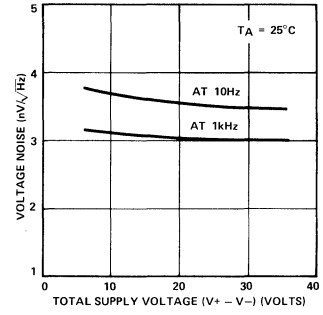
TOTAL NOISE vs SOURCE RESISTANCE



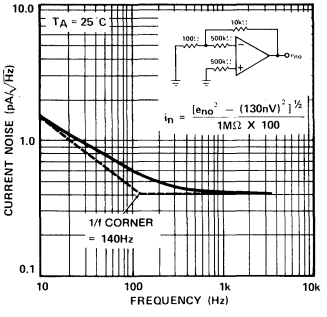
VOLTAGE NOISE vs TEMPERATURE



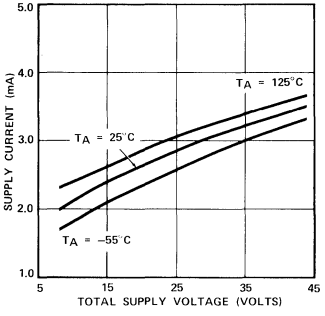
VOLTAGE NOISE vs SUPPLY VOLTAGE



CURRENT NOISE vs FREQUENCY

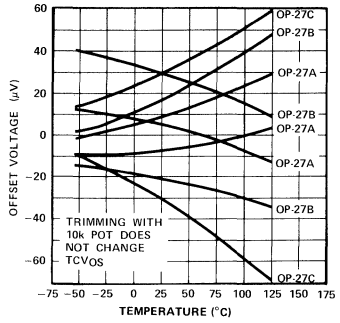


SUPPLY CURRENT vs SUPPLY VOLTAGE

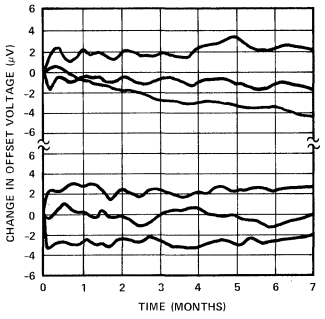


TYPICAL PERFORMANCE CURVES

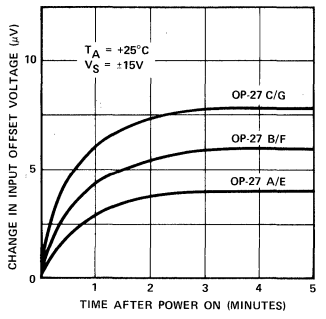
OFFSET VOLTAGE DRIFT OF REPRESENTATIVE UNITS vs TEMPERATURE



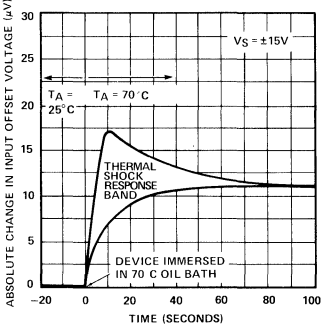
LONG TERM OFFSET VOLTAGE DRIFT OF REPRESENTATIVE UNITS



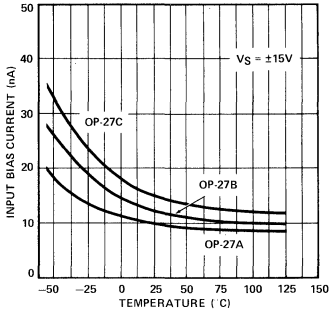
WARM-UP OFFSET VOLTAGE DRIFT



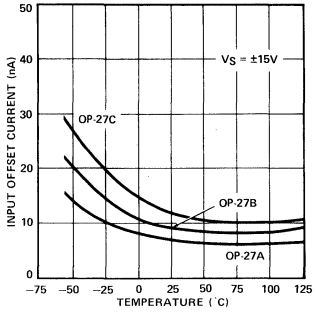
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



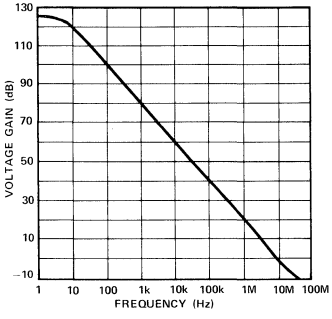
INPUT BIAS CURRENT vs TEMPERATURE



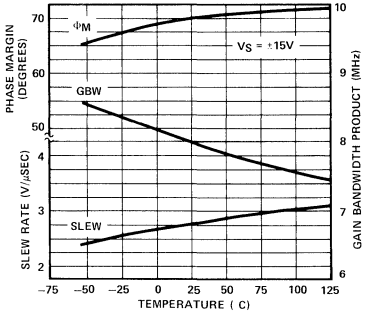
INPUT OFFSET CURRENT vs TEMPERATURE



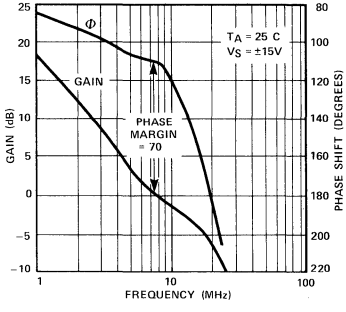
OPEN LOOP GAIN vs FREQUENCY



SLEW RATE, GAIN BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE

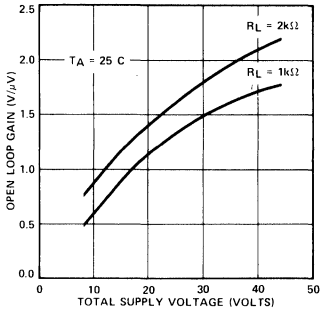


GAIN, PHASE SHIFT vs FREQUENCY

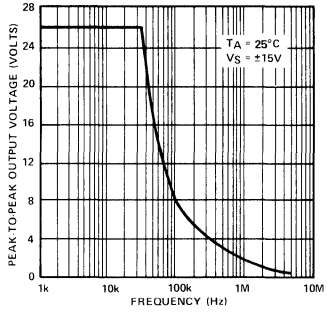


TYPICAL PERFORMANCE CURVES

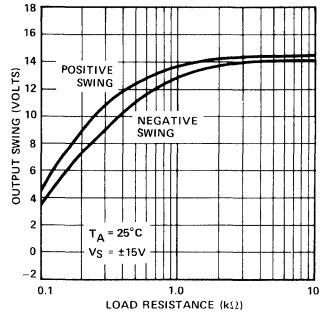
OPEN LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE



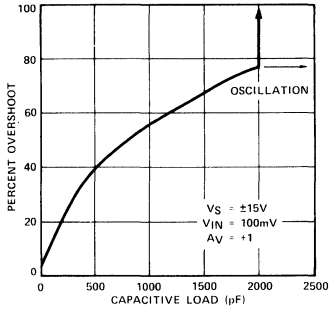
MAXIMUM UNDISTORTED OUTPUT vs FREQUENCY



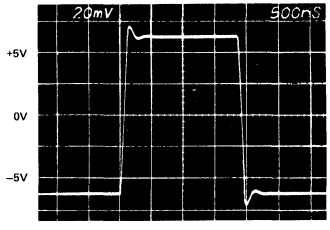
MAXIMUM OUTPUT SWING vs RESISTIVE LOAD



SMALL SIGNAL OVERSHOOT vs CAPACITIVE LOAD

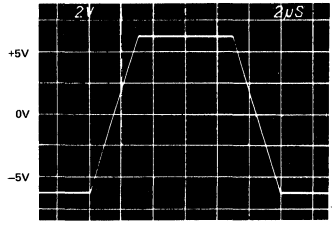


SMALL SIGNAL TRANSIENT RESPONSE



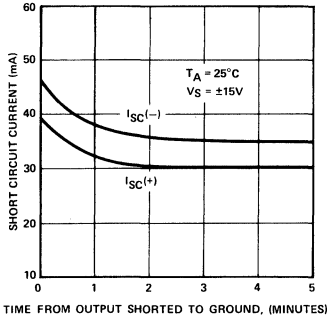
A_{VCL} = +1, C_L = 15pF
T_A = 25°C
V_S = ±15V

LARGE SIGNAL TRANSIENT RESPONSE

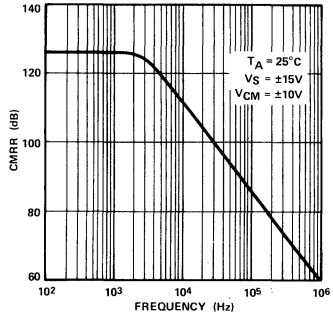


A_{VCL} = +1
T_A = +25°C
V_S = ±15V

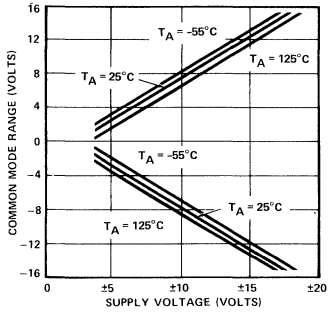
SHORT CIRCUIT CURRENT vs TIME



CMRR vs FREQUENCY

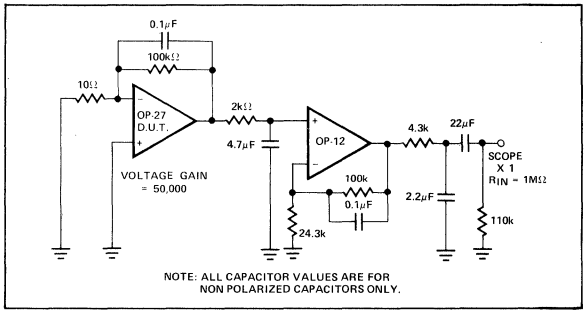


COMMON MODE INPUT RANGE vs SUPPLY VOLTAGE

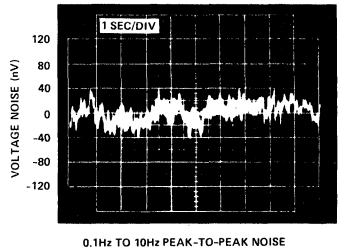


TYPICAL PERFORMANCE CURVES

0.1Hz TO 10Hz NOISE TEST CIRCUIT

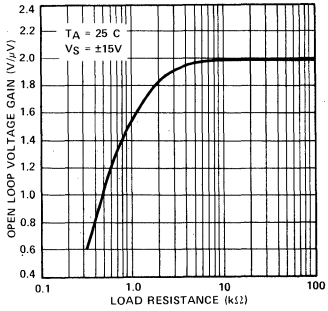


LOW FREQUENCY NOISE

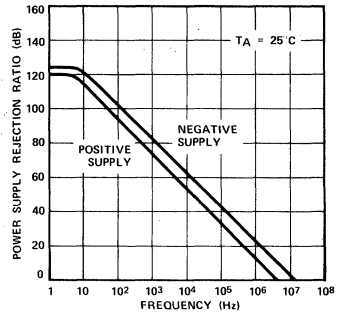


0.1Hz TO 10Hz PEAK-TO-PEAK NOISE

OPEN LOOP VOLTAGE GAIN vs LOAD RESISTANCE



PSRR vs FREQUENCY



APPLICATION INFORMATION

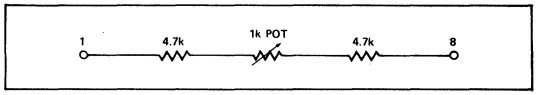
OP-27 Series units may be inserted directly into 725, OP-06, OP-07 and OP-05 sockets with or without removal of external compensation or nulling components. Additionally, OP-27 may be fitted to unnulled 741-type sockets; however, if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP-27 operation. OP-27 offset voltage may be nulled to zero (or other desired setting) through use of a potentiometer (see offset nulling circuit).

The OP-27 provides stable operation with load capacitances up to 2000pF and ±10V swings; larger capacitances should be decoupled with a 50Ω decoupling resistor.

The designer is cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

OFFSET VOLTAGE ADJUSTMENT

The input offset voltage of the OP-27, and its drift with temperature, are permanently trimmed at wafer testing to a very low level. However, if further adjustment of V_{OS} is necessary, nulling with a 10kΩ potentiometer will not degrade TCV_{OS} (see offset nulling circuit). Other potentiometer values from 1kΩ to 1MΩ can be used with a slight degradation (0.1 to 0.2μV/° C) of TCV_{OS}. Trimming to a value other than zero creates a drift of $(V_{OS}/300)\mu V/°C$, e.g. if V_{OS} is adjusted to 100μV, the change in TCV_{OS} will be 0.33μV/° C. The offset voltage adjustment range with a 10kΩ potentiometer is ±4mV. If smaller adjustment range is required, the sensitivity and/or resolution of the nulling can be increased by using a smaller pot in conjunction with fixed resistors. For example,



this network will have a ±280μV adjustment range.

OPTIMIZING LINEARITY

Best linearity can be obtained by designing for the minimum output current required for the application. High gain and excellent linearity can be achieved by operating the op amp within an output current range of ±10mA.

UNITY GAIN BUFFER APPLICATIONS

When $R_f \leq 100\Omega$ and the input is driven with a fast, large signal pulse (> 1V), the output waveform will look as shown in the pulsed operation diagram.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short circuit protection, will be drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20$mA at 10V) and the amplifier stays in its active mode and a smooth transition will occur.

As with all operational amplifiers when $R_f > 2k\Omega$, a pole will be created with R_f and the amplifier's input capacitance (8pF), creating additional phase shift and reducing the phase margin. A small capacitor (20 to 50pf) in parallel with R_f will eliminate this problem.

COMMENTS ON NOISE MEASUREMENTS

The extremely low noise of the OP-27 implies that its precise measurement is a difficult task. In order to realize the 80nV peak-to-peak noise specification of the op amp in the 0.1 Hz to 10 Hz frequency range, the following constraints have to be observed:

(1) The device has to be warmed up for at least five minutes. As shown in the warm-up drift curve, as the op amp warms up, its offset voltage changes typically 4μV due to its chip temperature increasing 14 to 20° C from the moment the power supplies are turned on. In the 10 sec measurement interval these temperature-induced effects can easily exceed tens of nanovolts.

(2) For similar reasons, the device has to be well shielded from air currents to eliminate the possibility of thermoelectric effects in excess of a few nanovolts invalidating the measurements.

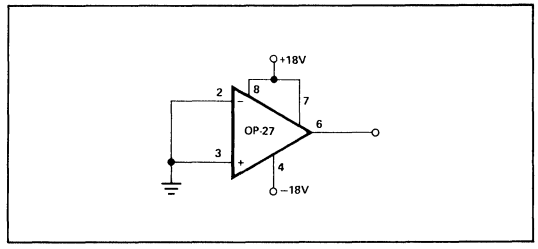
(3) Sudden motion in the vicinity of the device can also "feedthrough" to increase the observed noise.

(4) The test time to measure 0.1 Hz to 10 Hz noise should not exceed 10 sec. As shown in the noise tester frequency response curve the 0.1 Hz corner is defined by only one zero. The test time of 10 sec acts as an additional zero to eliminate noise contributions from the frequency band below 0.1 Hz.

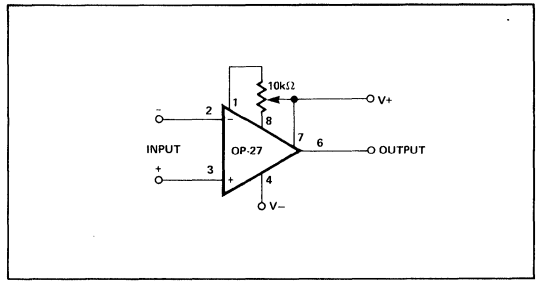
A noise-voltage density test is recommended when measuring noise on a large number of units. A 10 Hz noise-voltage density measurement will correlate well with a 0.1 Hz-to-10 Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

TYPICAL APPLICATIONS

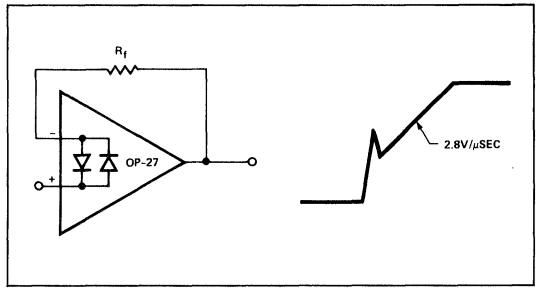
BURN-IN CIRCUIT



OFFSET NULLING CIRCUIT



PULSED OPERATION



OP-37

ULTRA-LOW NOISE PRECISION HIGH-SPEED OPERATIONAL AMPLIFIER ($A_{VCL} \geq 5$)

FEATURES

- **Unprecedented Low Noise** ... {**80nV p-p 0.1Hz to 10Hz**; **3nV/$\sqrt{Hz}$ at 1kHz**}
- **Ultra Stable** ..... {**0.2μV/°C**; **0.2μV/Month**}
- **Fast** ..... {**17V/μs Slew Rate**; **63MHz Gain Bandwidth**}
- **Low V_{OS}** **10μV**
- **Excellent CMRR** .... **126dB Over Input Voltage of ±11V**
- **High Gain** ..... **1.8 Million**
- **Replaces 725, OP-05, OP-06, OP-07, AD510, AD517, SE5534 in gains > 5**

GENERAL DESCRIPTION

A matchless combination of precision D.C. performance, low noise and wide bandwidth is featured in the OP-37 - an Operational Amplifier designed to maximize speed in applications requiring gains greater than five.

This low-noise instrumentation Op Amp combines the exceptional DC performance of the OP-07 (V_{OS} of 10μV, TCV_{OS} of 0.2μV/°C) with a truly awesome noise performance (e_n = 3.5nV/$\sqrt{Hz}$ at 10Hz) and a remarkably low 1/f noise corner frequency (2.7Hz). The high speed performance is assured by a gain-bandwidth product of 63MHz, and a slew rate of 17V/μsec.

In addition, this device has a gain of 1.5 million with a 1kΩ load while consuming 3mA. The OP-37 also features an I_B of ±10nA and an I_{OS} of 7nA. These surprisingly low currents are realized through the use of a unique input bias current cancellation circuit which typically holds I_B and I_{OS} of ±20nA and 15nA, respectively, over the full military temperature range.

Other sources of input referred errors, such as PSRR and CMRR, are reduced by factors in excess of 120dB. These characteristics, coupled with long term drift of 0.2μV/month allow the circuit designer to achieve performance levels previously attained by only the most complex and expensive hybrid or discrete designs.

The OP-37 brings low noise instrumentation type performance to such diverse applications as microphone, NAB tape head, and RIAA phone preamplifiers, high speed signal conditioning for data acquisition systems, wide bandwidth instrumentation and high speed analog controllers. The OP-37 also can be used as a comparator to discriminate extremely low voltages.

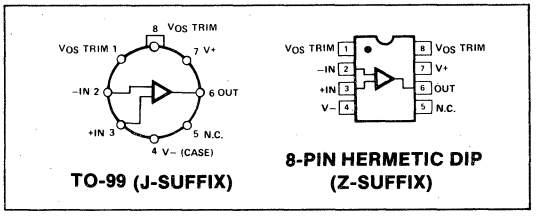
ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (μV)	PACKAGE TO-99 8-PIN	PACKAGE HERMETIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
25	OP37AJ*	OP37AZ*	MIL
25	OP37EJ	OP37EZ	IND
60	OP37BJ*	OP37BZ*	MIL
60	OP37FJ	OP37FZ	IND
100	OP37CJ*	OP37CZ*	MIL
100	OP37GJ	OP37GZ	IND

* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

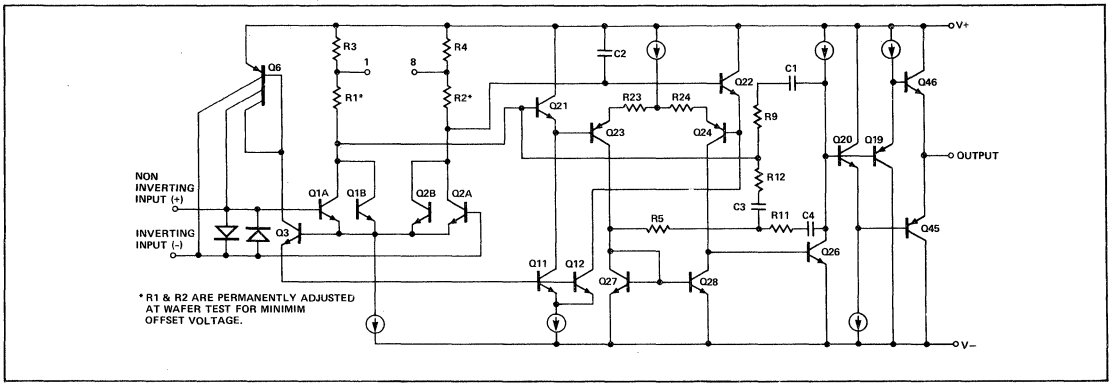
PIN CONNECTIONS



TO-99 (J-SUFFIX)

8-PIN HERMETIC DIP (Z-SUFFIX)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage ..... ±22V
Internal Power Dissipation (Note 1) 500mW
Input Voltage (Note 3) ..... ±22V
Output Short Circuit Duration ..... Indefinite
Differential Input Voltage (Note 2) ..... ±0.7V
Differential Input Current (Note 2) ..... ±25mA
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range
OP-37A, OP-37B, OP-37C ..... −55°C to +125°C
OP-37E, OP-37F, OP-37G ..... −25°C to +85°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
DICE Junction Temperature ..... −65°C to +150°C

NOTES:
1. See table for maximum ambient temperature rating and derating factor.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C

2. The OP-37's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
3. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
4. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V_S = ± 15V, T_A = + 25°C, unless otherwise noted.

			OP-37A/E			OP-37B/F			OP-37C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	–	10	25	–	20	60	–	30	100	µV
Long Term V_{OS} Stability	V_{OS}/Time	(Note 2)	–	0.2	1.0	–	0.3	1.5	–	0.4	2.0	µV/Mo
Input Offset Current	I_{OS}		–	7	35	–	9	50	–	12	75	nA
Input Bias Current	I_B		–	±10	±40	–	±12	±55	–	±15	±80	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3, 5)	–	0.08	0.18	–	0.08	0.18	–	0.09	0.25	µVp-p
Input Noise Voltage Density	e_n	f_o = 10Hz (Note 3)	–	3.5	5.5	–	3.5	5.5	–	3.8	8.0	nV/√Hz
		f_o = 30Hz (Note 3)	–	3.1	4.5	–	3.1	4.5	–	3.3	5.6	
		f_o = 1000Hz (Note 3)	–	3.0	3.8	–	3.0	3.8	–	3.2	4.5	
Input Noise Current Density	i_n	f_o = 10Hz (Note 3, 6)	–	1.7	4.0	–	1.7	4.0	–	1.7	–	pA/√Hz
		f_o = 30Hz (Note 3, 6)	–	1.0	2.3	–	1.0	2.3	–	1.0	–	
		f_o = 1000Hz (Note 3, 6)	–	0.4	0.6	–	0.4	0.6	–	0.4	0.6	
Input Resistance — Differential Mode	R_{IN}	(Note 4)	1.5	6	–	1.2	5	–	0.8	4	–	MΩ
Input Resistance — Common Mode	R_{INCM}		–	3	–	–	2.5	–	–	2	–	GΩ
Input Voltage Range	IVR		±11.0	±12.3	–	±11.0	±12.3	–	±11.0	±12.3	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±11V	114	126	–	106	123	–	100	120	–	dB
Power Supply Rejection Ratio	PSSR	V_S = ±4V to ±18V	—	1	10	—	1	10	—	2	20	µV/V
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V	1000	1800	–	1000	1800	–	700	1500	–	V/mV
		R_L ≥ 1kΩ, V_O = ±10V	800	1500	–	800	1500	–	400	1500	–	
(Note 4)	R_L = 600Ω,	V_O = ±1V, V_S = ±4V	250	700	–	250	700	–	200	500	–	
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±12.0	±13.8	–	±12.0	±13.8	–	±11.5	±13.5	–	V
		R_L ≥ 600Ω	±10.0	±11.5	–	±10.0	±11.5	–	±10.0	±11.5	–	
Slew Rate	SR	R_L ≥ 2kΩ (Note 4)	11	17	–	11	17	–	11	17	–	V/µs
Gain Bandwidth Prod.	GBW	f_o = 10kHz (Note 4)	45	63	–	45	63	–	45	63	–	MHz
		f_o = 1MHz	–	40	–	–	40	–	–	40	–	
Open Loop Output Resistance	R_O	V_O = 0, I_O = 0	–	70	–	–	70	–	–	70	–	Ω
Power Consumption	P_d	V_O = 0	–	90	140	–	90	140	–	100	170	mW
Offset Adjustment Range		R_P = 10kΩ	–	±4.0	–	–	±4.0	–	–	±4.0	–	mV

NOTES:
1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed up.
2. Long Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5µV — refer to typical performance curve.
3. Sample tested.
4. Guaranteed by design.
5. See test circuit and frequency response curve for 0.1Hz to 10Hz tester.
6. See test circuit for current noise measurement.

ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

			OP-37A			OP-37B			OP-37C			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	(Note 1)	–	30	60	–	50	200	–	70	300	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSN}	(Note 2)	–	0.2	0.6	–	0.3	1.3	–	0.4	1.8	μV/°C
Input Offset Current	I_{OS}		–	15	50	–	22	85	–	30	135	nA
Input Bias Current	I_B		–	±20	±60	–	±28	±95	–	±35	±150	nA
Input Voltage Range	IVR		±10.3	±11.5	–	±10.3	±11.5	–	±10.2	±11.5	–	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	108	122	–	100	119	–	94	116	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	16	—	2	20	—	4	51	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	600	1200	–	500	1000	–	300	800	–	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±11.5	±13.5	–	±11.0	±13.2	–	±10.5	±13.0	–	V

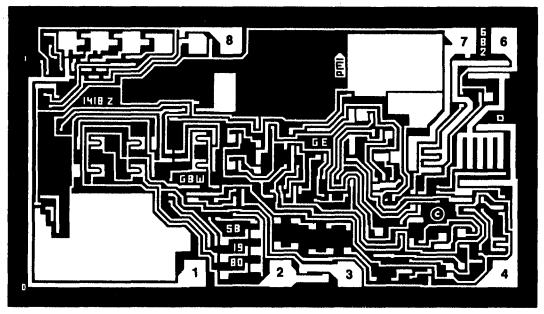
ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$, $-25°C \leq T_A \leq +85°C$, unless otherwise noted.

			OP-37E			OP-37F			OP-37G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}		–	20	50	–	40	140	–	55	220	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSN}	(Note 2)	–	0.2	0.6	–	0.3	1.3	–	0.4	1.8	μV/°C
Input Offset Current	I_{OS}		–	10	50	–	14	85	–	20	135	nA
Input Bias Current	I_B		–	±14	±60	–	±18	±95	–	±25	±150	nA
Input Voltage Range	IVR		±10.5	±11.8	–	±10.5	±11.8	–	±10.5	±11.8	–	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	110	124	–	102	121	–	96	118	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	15	—	2	16	—	2	32	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	750	1500	–	700	1300	–	450	1000	–	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±11.7	±13.6	–	±11.4	±13.5	–	±11.0	±13.3	–	V

NOTES:

1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed up.
2. The TCV_{OS} performance is within the specifications unnulled or when nulled with $R_P = 8k\Omega$ to $20k\Omega$.

DICE CHARACTERISTICS



DIE SIZE 0.054 X 0.096 inch

1. NULL
2. (–) INPUT
3. (+) INPUT
4. V–
6. OUTPUT
7. V+
8. NULL

For additional DICE information see Section 2.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-37N LIMIT	OP-37G LIMIT	OP-37GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	35	60	100	μV MAX
Input Offset Current	I_{OS}		35	50	75	nA MAX
Input Bias Current	I_B		±40	±55	±80	nA MAX
Input Voltage Range	IVR		±11.0	±11.0	±11.0	V MIN
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 11V$	114	106	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4V$ to $\pm 18V$	10	10	20	μV/V MAX
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$ $R_L \geq 1k\Omega$ $V_O = \pm 10V$	1000 800	1000 800	700 –	V/mV MIN
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	±12.0 ±10.0	±12.0 ±10.0	±11.5 ±10.0	V MIN
Power Consumption	P_d	$V_O = 0$	140	140	170	mW MAX

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

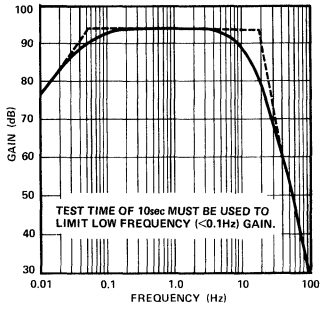
PARAMETER	SYMBOL	CONDITIONS	OP-37N TYP	OP-37G TYP	OP-37GR TYP	UNITS
Average Input Offset Voltage Drift	TCV_{OS} or TCV_{OSN}	Nulled or Unnulled $R_P = 8k\Omega$ to $20k\Omega$	0.2	0.3	0.4	μV/°C
Average Input Offset Current Drift	TCI_{OS}		80	130	180	pA/°C
Average Input Bias Current Drift	TCI_B		100	160	200	pA/°C
Input Noise Voltage Density	e_n	$f_o = 10Hz$ $f_o = 30Hz$ $f_o = 1000Hz$	3.5 3.1 3.0	3.5 3.1 3.0	3.8 3.3 3.2	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	$f_o = 10Hz$ $f_o = 30Hz$ $f_o = 1000Hz$	1.7 1.0 0.4	1.7 1.0 0.4	1.7 1.0 0.4	$pA/\sqrt{Hz}$
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	0.08	0.08	0.09	μVp-p
Slew Rate	SR	$R_L \geq 2k\Omega$	17	17	17	V/μs
Gain Bandwidth Product	GBW	$f_o = 10kHz$	63	63	63	MHz

NOTE:

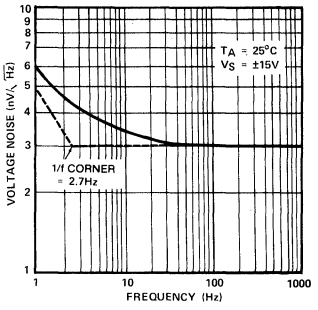
1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

TYPICAL PERFORMANCE CURVES

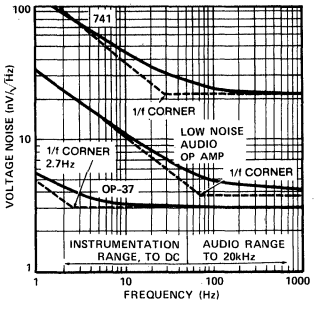
0.1Hz TO 10Hzp-p NOISE TESTER FREQUENCY RESPONSE



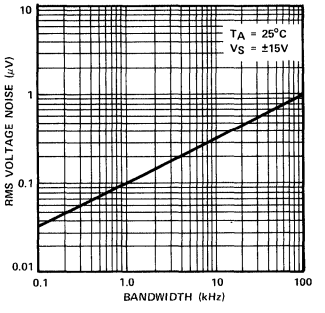
OP-37 VOLTAGE NOISE vs FREQUENCY



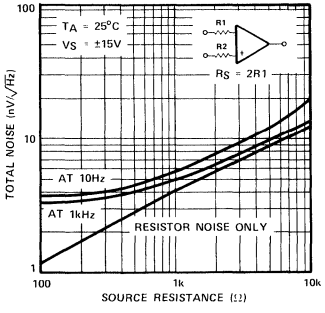
A COMPARISON OF OP AMP VOLTAGE NOISE SPECTRUMS



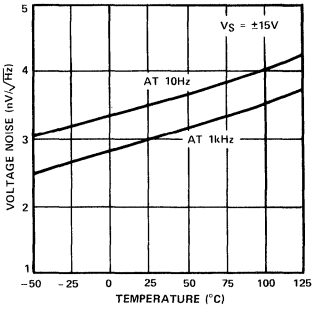
INPUT WIDEBAND VOLTAGE NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



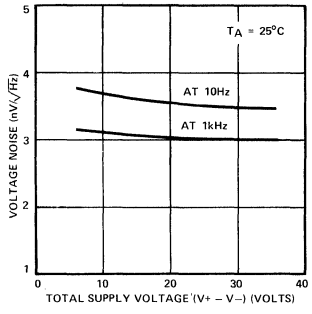
TOTAL NOISE vs SOURCE RESISTANCE



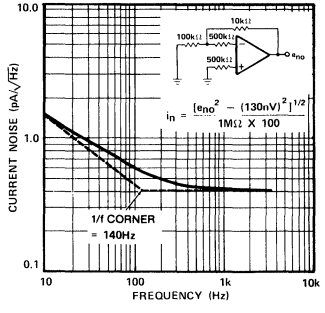
VOLTAGE NOISE vs TEMPERATURE



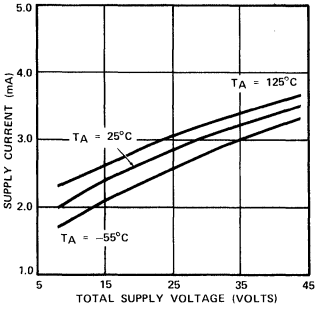
VOLTAGE NOISE vs SUPPLY VOLTAGE



CURRENT NOISE vs FREQUENCY

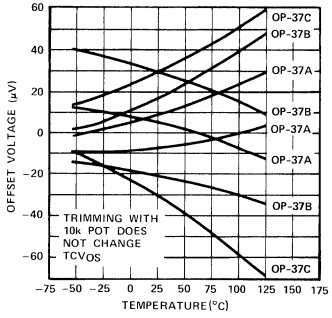


SUPPLY CURRENT vs SUPPLY VOLTAGE

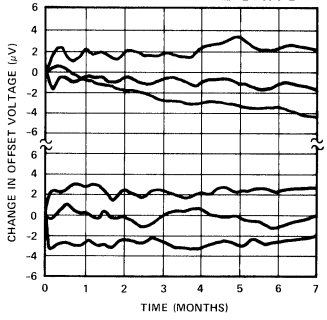


TYPICAL PERFORMANCE CURVES

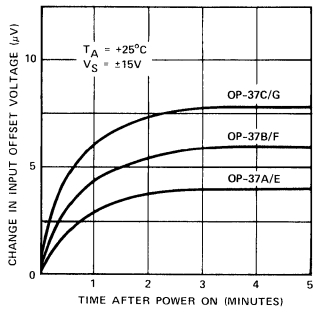
OFFSET VOLTAGE DRIFT OF REPRESENTATIVE UNITS vs TEMPERATURE



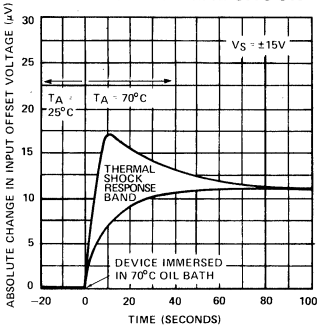
LONG TERM OFFSET VOLTAGE DRIFT OF REPRESENTATIVE UNITS



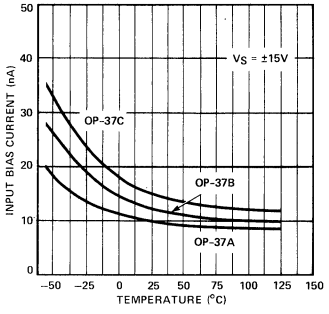
WARM-UP OFFSET VOLTAGE DRIFT



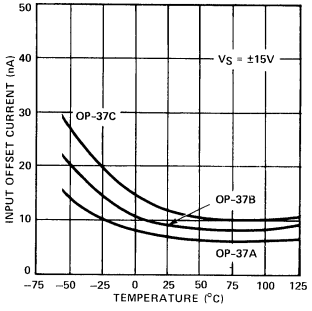
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



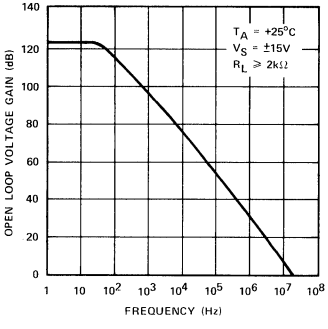
INPUT BIAS CURRENT vs TEMPERATURE



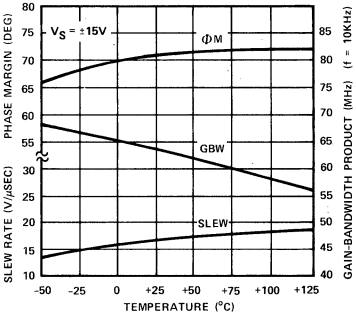
INPUT OFFSET CURRENT vs TEMPERATURE



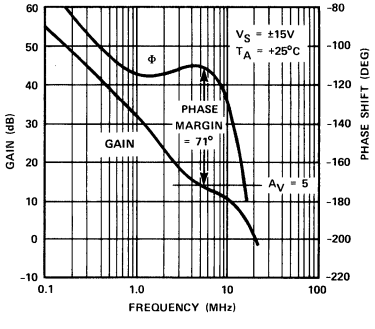
OPEN LOOP GAIN vs FREQUENCY



SLEW RATE, GAIN BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE

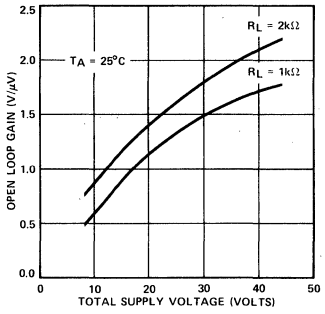


GAIN, PHASE SHIFT vs FREQUENCY

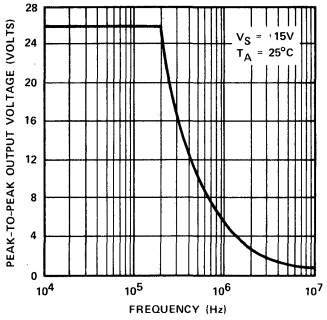


TYPICAL PERFORMANCE CURVES

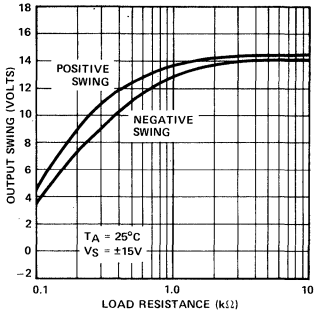
OPEN LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE



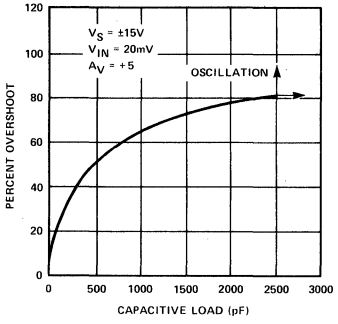
MAXIMUM UNDISTORTED OUTPUT vs FREQUENCY



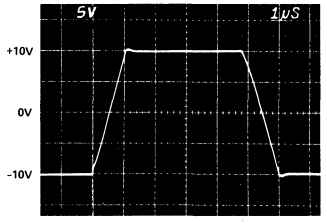
MAXIMUM OUTPUT SWING vs RESISTIVE LOAD



SMALL SIGNAL OVERSHOOT vs CAPACITIVE LOAD

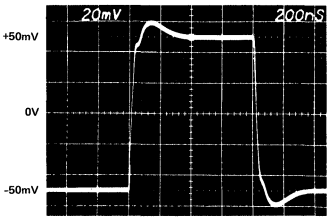


LARGE SIGNAL TRANSIENT RESPONSE



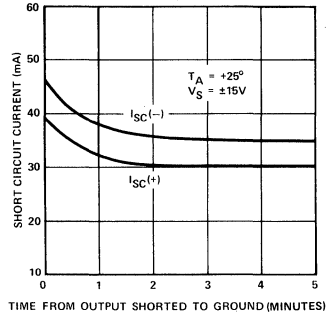
V_S = ±15V
A_V = +5
T_A = +25°C

SMALL SIGNAL TRANSIENT RESPONSE

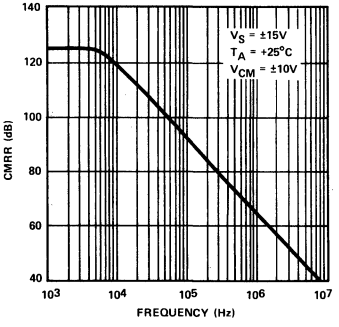


V_S = ±15V
A_V = +5
T_A = +25°C
C_L =25pF

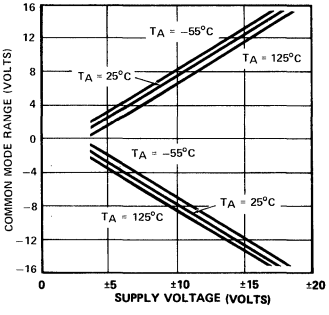
SHORT CIRCUIT CURRENT vs TIME



CMRR vs FREQUENCY

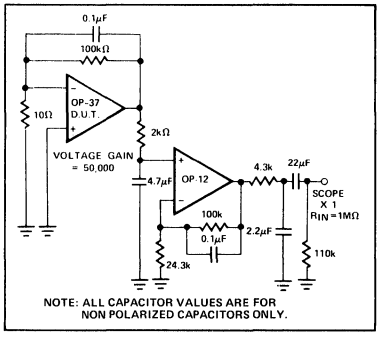


COMMON MODE INPUT RANGE vs SUPPLY VOLTAGE



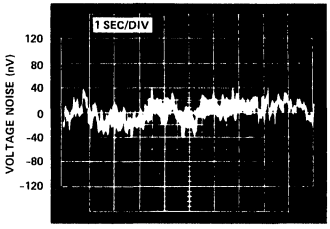
TYPICAL PERFORMANCE CURVES

0.1Hz TO 10Hz NOISE TEST CIRCUIT



NOTE: ALL CAPACITOR VALUES ARE FOR NON POLARIZED CAPACITORS ONLY.

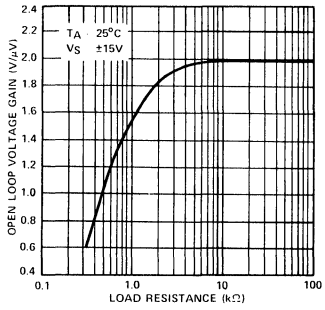
LOW FREQUENCY NOISE



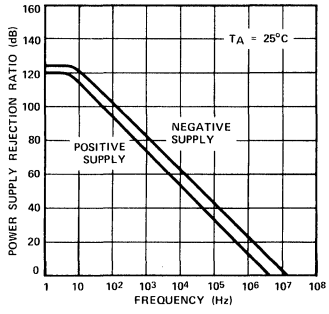
0.1Hz TO 10Hz PEAK-TO-PEAK NOISE

NOTE:
Observation time limited to 10 seconds to insure 0.1 Hz cutoff.

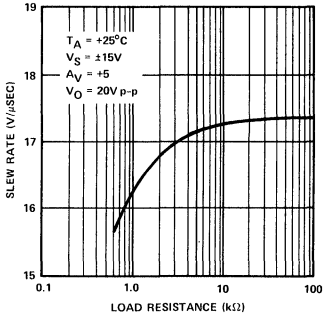
OPEN LOOP VOLTAGE GAIN vs LOAD RESISTANCE



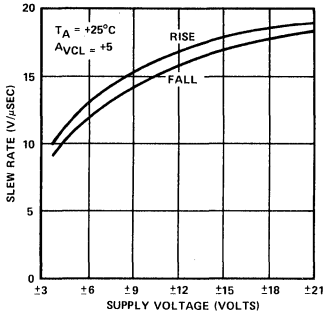
PSRR vs FREQUENCY



SLEW RATE vs LOAD



SLEW RATE vs SUPPLY VOLTAGE



APPLICATION INFORMATION

OP-37 Series units may be inserted directly into 725, OP-06, OP-07 and OP-05 sockets with or without removal of external compensation or nulling components. In addition, the OP-37 may be fitted to unnulled 741-type sockets; however, if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP-37 operation. OP-37 offset voltage may be nulled to zero (or other desired setting) through use of a potentiometer (see offset nulling circuit).

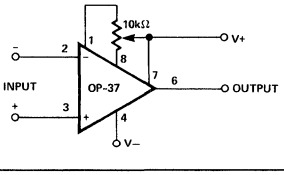
The OP-37 provides stable operation with load capacitances up to 2500pF and ±10V swings; larger capacitances should be decoupled with a 50Ω decoupling resistor.

The designer is cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

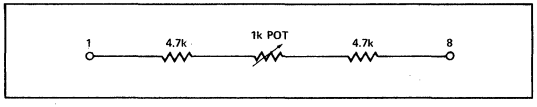
Offset Voltage Adjustment

The input offset voltage of the OP-37 and its drift with temperature are permanently trimmed at wafer testing to a very low level. However, if further adjustment of V_{OS} is necessary, nulling with a 10kΩ potentiometer will not degrade TCV_{OS} (see offset nulling circuit). Other potentiometer values from 1kΩ to 1MΩ can be used with a slight degradation (0.1 to 0.2μV/°C) of TCV_{OS}. Trimming to a value other than

OFFSET NULLING CIRCUIT



zero creates a drift of $(V_{OS}/300)\mu V/°C$, e.g. if V_{OS} is adjusted to 100μV, the change in TCV_{OS} will be 0.33μV/° C. The offset voltage adjustment range with a 10kΩ potentiometer is ±4mV. If smaller adjustment range is required, the sensitivity and/or resolution of the nulling can be increased by using a smaller pot in conjunction with fixed resistors. For example,



this network will have a ±280μV adjustment range.

COMMENTS ON NOISE MEASUREMENTS

The extremely low noise of the OP-37 implies that its precise measurement is a difficult task. In order to realize the 80nV peak-to-peak noise specification of the op amp in the 0.1 Hz to 10 Hz frequency range, the following constraints have to be observed:

(1) The device has to be warmed up for at least five minutes. As shown in the warm-up drift curve, as the op amp warms up, its offset voltage changes typically 4μV due to its chip temperature increasing 14 to 20° C from the moment the power supplies are turned on. In the 10 sec measurement interval these temperature-induced effects can easily exceed tens of nanovolts.

(2) For similar reasons, the device has to be well shielded from air currents to eliminate the possibility of thermoelectric effects in excess of a few nanovolts invalidating the measurements.

(3) Sudden motion in the vicinity of the device can also "feedthrough" to increase the observed noise.

(4) The test time to measure 0.1 Hz to 10 Hz noise should not exceed 10 sec. As shown in the noise tester frequency response curve the 0.1 Hz corner is defined by only one zero. The test time of 10 sec acts as an additional zero to eliminate noise contributions from the frequency band below 0.1 Hz.

A noise-voltage density test is recommended when measuring noise on a large number of units. A 10 Hz noise-voltage density measurement will correlate well with a 0.1 Hz-to-10 Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

OPTIMIZING LINEARITY

Best linearity can be obtained by designing for the minimum output current required for the application. High gain and excellent linearity can be achieved by operating the op amp within an output current range of ±10mA.

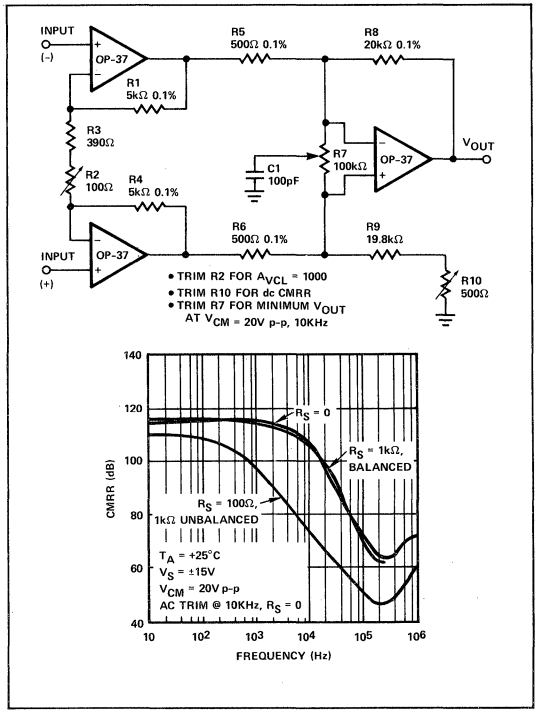
INSTRUMENTATION AMPLIFIER

A traditional 3 Op Amp instrumentation amplifier provides high gain and wide bandwidth.

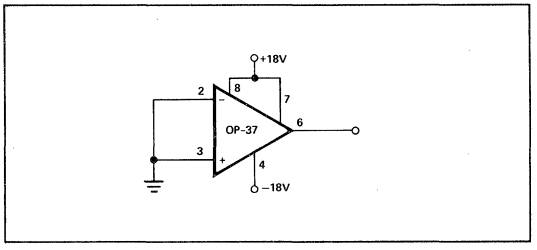
The input noise of this configuration is $4.9nV/\sqrt{Hz}$. In the circuit shown, the gain of the input stage is set at 25, and the gain of the second stage is 40. The overall gain of the circuit, then, is 1000.

The bandwidth of this amplifier is 800kHz - extraordinarily wide for a precision instrumentation amp. When the gain of 1000 is factored in, the gain-bandwidth of the circuit, is 800MHz. The full power bandwidth of the circuit, for a 20Vp-p output, is 250kHz.

Resistor R_7 in the circuit is trimmed to optimize the instrumentation amplifier's common-mode rejection throughout its operating frequencies.



BURN-IN CIRCUIT



OP-207

DUAL, ULTRA-LOW V_{OS}, MATCHED OPERATIONAL AMPLIFIER (EXTREMELY TIGHT MATCHING)

FEATURES

- **Low V_{OS} ..... 100μV Max.**
- **Tight Offset Voltage Match ..... 90μV Max.**
- **Tight Offset Voltage Match vs Temp. .... 1.0μV/°C Max.**
- **Tight Common Mode Rejection Match .... 103dB Min.**
- **Tight Bias Current Match ..... 3.5nA Max.**
- **Low Noise ..... 0.6μV_{p-p} Max.**
- **Low Bias Current ..... 3.0nA Max.**
- **High Channel Separation ..... 126dB Min.**

GENERAL DESCRIPTION

The OP-207 Series of Dual Ultra-low V_{OS} Matched Operational Amplifiers consists of two independent OP-07 high performance operational amplifiers in a single 14-pin Dual-in-Line package. Exceptionally low offset voltage and extremely tight matching of critical parameters is provided between the channels of this dual operational amplifier.

The excellent specifications of the individual amplifiers combined with the tight matching and temperature tracking between channels enables realization of extremely high performance instrumentation amplifier designs without resorting to laborious and expensive selection and matching of discrete amplifiers. The designer is assured of achieving the full performance guaranteed by the specification as the common package eliminates the unavoidable temperature differentials incurred by all designs utilizing separately packaged amplifiers.

Matching between channels is provided on all critical parameters including offset voltage, tracking of offset voltage vs. temperature, non-inverting bias currents, and common mode and power supply rejection ratios. The dual, factory-trimmed, compensated amplifiers allow the complete elimination of external components for offset nulling, frequency compensation and device protection. In addition the individual amplifiers feature extremely low offset voltage, low offset voltage drift, low noise voltage and low bias current.

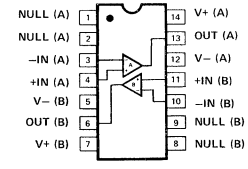
ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (μV)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
100	OP207AY*	MIL
100	OP207EY	COM
200	OP207BY*	MIL
200	OP207FY	COM

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number.

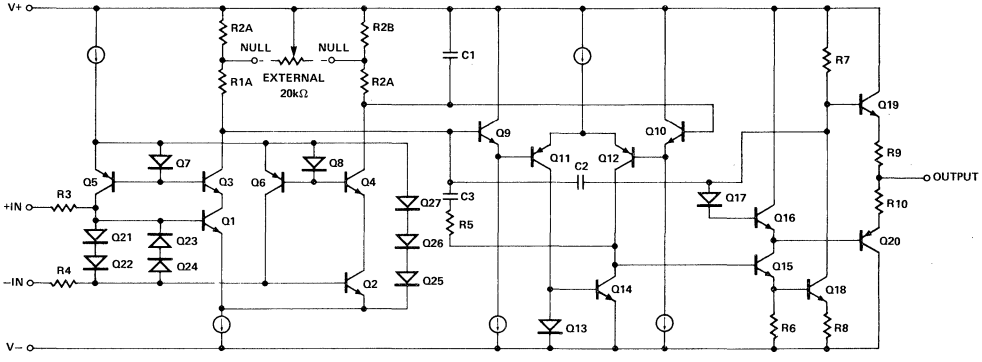
†All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



14 PIN HERMETIC DIP (Y-Suffix)

SIMPLIFIED SCHEMATIC (1/2 OP-207)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±22V
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range
OP-207A, OP-207B ..... -55°C to +125°C
OP-207E, OP-207F ..... 0°C to + 70°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14 PIN HERMETIC DIP	106°C	11.3mW/°C

NOTES:
1. See table for maximum ambient temperature rating and derating factor.
2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

MATCHING CHARACTERISTICS at V_S = ± 15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-207A/E MIN	OP-207A/E TYP	OP-207A/E MAX	OP-207B/F MIN	OP-207B/F TYP	OP-207B/F MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}	R_S = 100Ω	—	30	90	—	50	280	µV
Average Non-Inverting Bias Current	I_B^+		—	±1.5	±3.5	—	±1.5	±6.0	nA
Non-Inverting Offset Current	I_{OS}^+		—	±0.7	±3.5	—	±1.0	±6.0	nA
Inverting Offset Current	I_{OS}^-		—	±0.7	±3.5	—	±1.0	±6.0	nA
Common Mode Rejection Ratio Match	ΔCMRR	V_{CM} = ± 13V	103	120	—	96	114	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	V_S = ±3V to ±18V	—	7	32	—	10	51	µV/V
Channel Separation			126	140	—	126	140	—	dB

MATCHING CHARACTERISTICS at V_S = ±15V, -55 ≤ T_A ≤ 125°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-207A MIN	OP-207A TYP	OP-207A MAX	OP-207B MIN	OP-207B TYP	OP-207B MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}	R_S = 100Ω	—	70	180	—	180	450	µV
Input Offset Voltage Tracking									
Without External Trim	$TC\Delta V_{OS}$	(Note 1)	—	0.5	1.0	—	0.9	1.5	µV/°C
With External Trim	$TC\Delta V_{OSn}$	R_p = 20kΩ (Note 1)	—	0.3	1.0	—	0.4	1.3	—
Average Non-Inverting Bias Current	I_B^+		—	2.0	6.0	—	3.0	12.0	nA
Average Drift of Non-Inverting Bias Current	TCI_B^+		—	10	—	—	12	—	pA/°C
Non-Inverting Offset Current	I_{OS}^+		—	2.0	6.5	—	3.0	12.0	nA
Average Drift of Non-Inverting Offset Current	TCI_{OS}^+		—	12	—	—	15	—	pA/°C
Inverting Offset Current	I_{OS}^-		—	2.0	6.5	—	3.0	12.0	nA
Common Mode Rejection Ratio Match	ΔCMRR	V_{CM} = ± 13V	100	117	—	94	114	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	V_S = ±3V to ±18V	—	10	51	—	16	100	µV/V

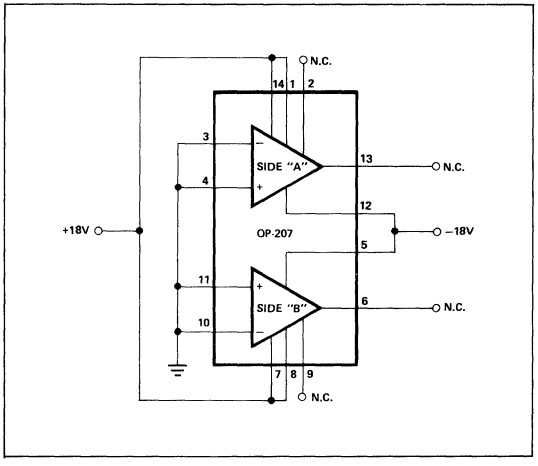
NOTE:
1. Sample tested.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $0°C \leq T_A \leq 70°C$, unless otherwise noted.

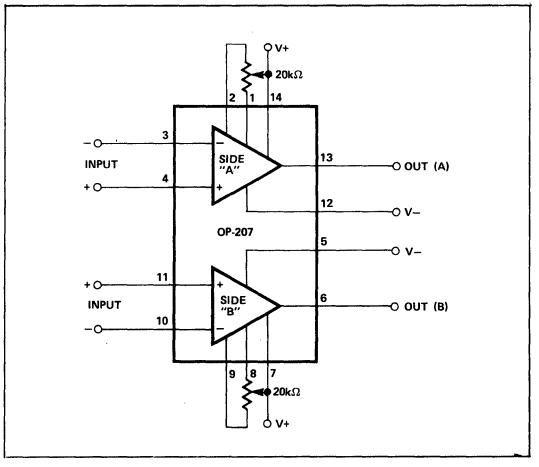
PARAMETER	SYMBOL	CONDITIONS	OP-207E MIN	OP-207E TYP	OP-207E MAX	OP-207F MIN	OP-207F TYP	OP-207F MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}	$R_S = 100\Omega$	—	60	150	—	120	350	μV
Input Offset Voltage Tracking									
Without External Trim	$TC\Delta V_{OS}$	(Note 1)	—	0.5	1.0	—	0.9	1.5	μV/°C
With External Trim	$TC\Delta V_{OSn}$	$R_p = 20k\Omega$ (Note 1)	—	0.3	1.0	—	0.4	1.3	
Average Non-Inverting Bias Current	I_{B^+}		—	2.0	5.0	—	3.0	10.0	nA
Average Drift of Non-Inverting Bias Current	TCI_{B^+}		—	10	—	—	12	—	pA/°C
Non-Inverting Offset Current	I_{OS^+}		—	2.0	5.0	—	3.0	10.0	nA
Average Drift of Non-Inverting Offset Current	TCI_{OS^+}		—	12	—	—	15	—	pA/°C
Inverting Offset Current	I_{OS^-}		—	2.0	5.0	—	3.0	10.0	nA
Common Mode Rejection Ratio	ΔCMRR	$V_{CM} = \pm 13V$	100	117	—	94	114	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 3V$ to $\pm 18V$	—	10	51	—	16	100	μV/V

NOTE:
1. Sample tested.

BURN-IN CIRCUIT



OFFSET NULLING CIRCUIT



INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-207A/E			OP-207B/F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S = 100\Omega$	—	35	100	—	60	200	μV
Input Offset Voltage Stability	ΔV_{OS}/Time	(Note 1)	—	0.3	1.5	—	0.4	2.0	μV/Mo
Input Offset Current	I_{OS}		—	0.9	2.8	—	1.5	6.0	nA
Input Bias Current	I_B		—	1.0	3.0	—	2.0	7.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)	—	0.35	0.6	—	0.35	0.6	μV_{p-p}
Input Noise Voltage Density	e_n	$f_o = 10Hz$	—	10.3	18.0	—	10.3	18.0	$nV/\sqrt{Hz}$
		(Note 2) $f_o = 100Hz$	—	10.0	13.0	—	10.0	13.0	
		$f_o = 1000Hz$	—	9.6	—	—	9.6	—	
Input Noise Current	i_{np-p}	(Note 2) 0.1Hz to 10Hz	—	14	30	—	14	30	pA_{p-p}
Input Noise Current Density	i_n	$f_o = 10Hz$	—	0.32	0.80	—	0.32	0.80	$pA/\sqrt{Hz}$
		(Note 2) $f_o = 100Hz$	—	0.14	0.23	—	0.14	0.23	
		$f_o = 1000Hz$	—	0.12	—	—	0.12	—	
Input Resistance — Differential Mode	R_{IN}	(Note 3)	20	60	—	8	30	—	MΩ
Input Resistance — Common Mode	$R_{IN\ CM}$		—	200	—	—	120	—	GΩ
Input Voltage Range	IVR		±13.0	±14.0	—	±13.0	±14.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	7	32	$\mu V/V$
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	500	—	150	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.5	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±12.0	±12.8	—	
		$R_L \geq 1k\Omega$	±10.0	±12.0	—	±10.0	±12.0	—	
Slewing Rate	SR	$R_L \geq 2k\Omega$	—	0.2	—	—	0.2	—	$V/\mu s$
Closed Loop Bandwidth	BW	$A_{VCL} = +1.0$	—	0.6	—	—	0.6	—	MHz
Open Loop Output Resistance	R_o	$V_O = 0$, $I_o = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	No load	—	90	120	—	100	150	mW
Offset Adjustment Range		$R_p = 20k\Omega$	—	±4	—	—	±4	—	mV
Input Capacitance	C_{IN}		—	8	—	—	8	—	pF

NOTES:

1. Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically $2.5\mu V$. Paremeter is sample tested.
2. Sample tested.
3. Guaranteed by design.

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le 125°C$, unless otherwise noted.

			OP-207A			OP-207B			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S = 100\Omega$	—	75	230	—	100	400	μV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}		—	0.4	1.3	—	0.7	1.8	μV/°C
With External Trim	TCV_{OSn}	$R_p = 20k\Omega$ (Note 1)	—	0.4	—	—	0.7	—	
Input Offset Current	I_{OS}			1.8	5.6		3.0	12.0	nA
Average Input Offset Current Drift	TCI_{OS}		—	10	—	—	12	—	pA/°C
Input Bias Current	I_B		—	3.0	5.6	—	4.0	14.0	nA
Average Input Bias Current Drift	TCI_B		—	12	—	—	18	—	pA/°C
Input Voltage Range	IVR		±13.0	±13.5	—	±13.0	±13.5	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	120	—	97	117	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	150	400	—	120	350	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	12.0	12.8	—	12.0	12.8	—	V

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

			OP-207E			OP-207F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S = 100\Omega$	—	60	200	—	90	350	μV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}		—	0.4	1.3	—	0.7	1.8 (Note 2)	μV/°C
With External Trim	TCV_{OSn}	$R_p = 20k\Omega$ (Note 1)	—	0.4	—	—	0.7	—	
Input Offset Current	I_{OS}		—	1.4	5.0	—	2.5	10.0	nA
Average Input Offset Current Drift	TCI_{OS}		—	10	—	—	12	—	pA/°C
Input Bias Current	I_B		—	2.0	5.0	—	3.0	11.0	nA
Average Input Bias Current Drift	TCI_B		—	12	—	—	18	—	pA/°C
Input Voltage Range	IVR		±13.0	±13.5	—	±13.0	±13.5	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	120	—	97	117	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	150	400	—	120	350	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	12.0	12.8	—	12.0	12.8	—	V

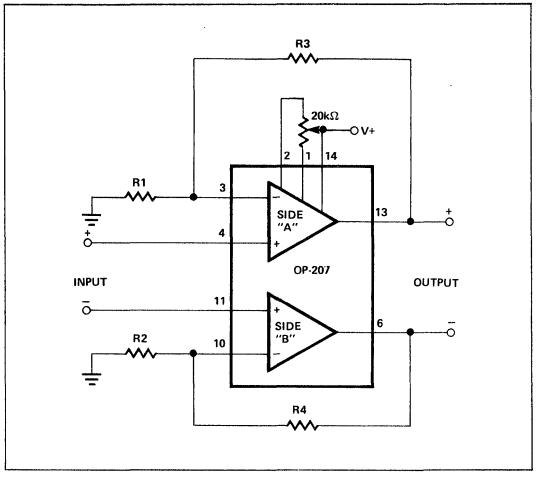
NOTES:
1. Exclude first hour of operation to allow for stabilization of external circuitry.
2. Sample tested.

APPLICATION OF DUAL MATCHED OPERATIONAL AMPLIFIERS

ADVANTAGES OF DUAL MATCHED OPERATIONAL AMPLIFIERS

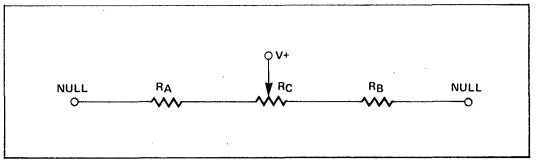
Dual Matched Operational Amplifiers provide the engineer a powerful tool for the solution of a number of difficult circuit design problems including true instrumentation amplifiers, extremely low drift, high common mode rejection DC amplifiers, low DC drift active filters, dual tracking voltage references and many other demanding applications. These designs are based on the principle that careful matching between two operational amplifiers can, to a large extent, eliminate the effect of DC errors inherent in the individual amplifiers.

Reference to the circuit, a differential-in, differential-out amplifier, shows how the reductions in error can be accomplished. Assuming the resistors used are ideally matched, the gain of each side will be identical; if the offset voltages of each amplifier are perfectly matched, then the net differential voltage at the amplifiers output will be zero. Note that the output offset error of this amplifier is not a function of the offset voltage of the individual amplifiers, but only a function of the *difference* (degree of matching) between the amplifiers' offset voltages. This error-cancellation principle holds for a considerable number of input referred error parameters — offset voltage, offset voltage drift, inverting and noninverting bias currents, common-mode and power supply rejection ratios. Note also that the impedances of each input, both common-mode and differential mode, are extremely high and can also be tightly matched, an important feature not possible with single operational amplifier circuits. Common mode rejection can be made exceptionally high; this is especially important in instrumentation amplifiers where errors due to large common-mode voltages can be far greater than those due to noise or drift with temperature. (For example, consider the case of two op amps, each with 80dB (100μV/V) CMRR. However, if the CMRR of one device is +100μV/V while CMRR of the other is -100μV/V for a net 200μV/V CMRR match, the resultant input reference error over a 10V common-mode input signal will be 2mV.



POWER SUPPLIES

The V+ supply terminals are completely independent and may be powered by separate supplies if desired (this approach, however, would sacrifice the advantages of the power supply rejection ratio matching). The V- supply terminals are both connected to the common substrate and must be tied to the same voltage.



OFFSET TRIMMING

Offset trimming terminals are provided for each amplifer of the OP-207 — however, guaranteed performance over temperature can be obtained by trimming only one side (side A) to match the offset of the other for a net differential offset of zero. This is due to the specific procedure used during factory testing of the devices; however, results which are essentially the same may be obtained to trimming side B to match side A, or by nulling each side individually.

The OP-207 is designed to provide lowest drift performance when trimmed with a 20kΩ potentiometer; this value provides about ±4mV of adjustment range which should be considerably more than adequate for most applications. When finer resolution of trimming is desired, or where unwanted changes in potentiometer position with time and temperature could create unacceptable offsets, the sensitivity to offset potentiometer position may be reduced by using the circuit.

OP-215

DUAL PRECISION JFET INPUT OPERATIONAL AMPLIFIER

FEATURES

- **High Slew Rate** **18V/μs**
- **Fast Settling Time** **900ns**
- **Low Input Offset Voltage Drift** ..... **3.0μV/°C**
- **Wide Bandwidth** **6MHz**
- **Temperature Compensated Input Bias Currents**
- **Guaranteed Input Bias Current** ..... **18nA Max (125° C)**
- **Bias Current Specified WARMED UP Over Temperature**
- **Low Input Noise Current** ..... **0.01pA/√Hz**
- **High Common Mode Rejection Ratio** **100dB**
- **PIN compatible with Standard Dual Pinouts**
- **125°C Temperature Test DICE**
- **Models with MIL-STD-883 Class B Processing Available from Stock**

GENERAL DESCRIPTION

The OP-215 offers the proven BIFET performance advantages of high speed and low input bias current with the tracking and convenience advantages of a Dual Op-Amp configuration.

Low input offset voltages, low input currents and minimal drift parameters are featured in these high speed amplifiers. On-chip Zener Zap trimming is used to achieve low V_{OS} while a bias current compensation scheme gives a low input bias current at elevated temperatures. Thus the OP-215 features an input bias current of 18nA at 125° C ambient (not junction) temperature which greatly extends the application usefulness of this device.

Applications include high speed amplifiers for current output DACs, active filters, sample-and-hold buffers, and photocell amplifiers. For additional precision JFET op amps, see the OP-15, OP-16 and OP-17 data sheets.

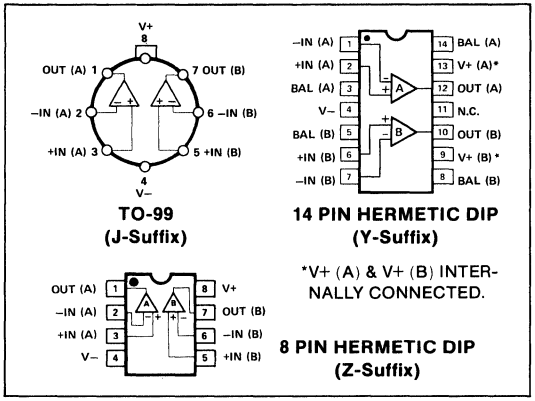
ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	HERMETIC DIP 8-PIN	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
1.0	OP215AJ*	OP215AZ*	OP215AY*	MIL
1.0	OP215EJ	OP215EZ	OP215EY	COM
2.0	OP215BJ*	OP215BZ*	OP215BY*	MIL
2.0	OP215FJ	OP215FZ	OP215FY	COM
4.0	OP215CJ*	OP215CZ*	OP215CY*	MIL
6.0	OP215GJ	OP215GZ	OP215GY	COM

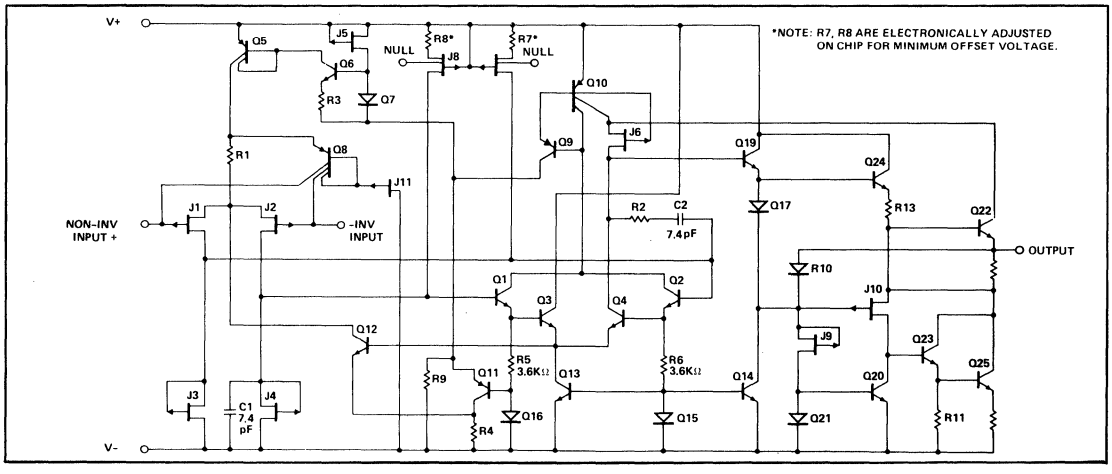
* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC DIAGRAM (1/2 OP-215)



ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage
- OP-215A, OP-215B, OP-215E, OP-215F (All DICE except GR) ..... ±22V
- OP-215C, OP-215G (GR DICE only)..... ±18V

Internal Power Dissipation (Note 1) 500mW

Operating Temperature Range
- OP-215A, OP-215B, OP-215C ..... −55°C to +125°C
- OP-215E, OP-215F, OP-215G ..... 0°C to +70°C

Maximum Junction Temperature (T_J) ..... +150°C

Differential Input Voltage
- OP-215A, OP-215B, OP-215E, OP-215F (All DICE except GR) ... ± 40V
- OP-215C, OP-215G (GR DICE only) ..... ± 30V

Input Voltage
- OP-215A, OP-215B, OP-215E, OP-215F (All DICE except GR) ... ± 20V
- OP-215C, OP-215G (GR DICE only) ..... ± 16V

(Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.)

Output Short Circuit Duration ..... Indefinite

Storage Temperature Range ..... −65°C to +150°C

Lead Temperature (Soldering, 60 sec) ..... 300°C

DICE Junction Temperature (T_j) ..... −65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	100°C	10.0mW/°C
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C

2. Absolute maximum ratings apply to both packaged parts and dice, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	OP-215A/E MIN	OP-215A/E TYP	OP-215A/E MAX	OP-215B/F MIN	OP-215B/F TYP	OP-215B/F MAX	OP-215C/G MIN	OP-215C/G TYP	OP-215C/G MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	–	0.2	1.0	–	0.8	2.0	–	2.0	4.0	mV
		'G' Grade	–	–	–	–	–	–	–	2.5	6.0	
Input Offset Current	I_{OS}	$T_J = 25°C$ (Note 1)	–	3.0	50	–	3.0	50	–	3.0	100	pA
		Device Operating	–	5.0	100	–	5.0	100	–	5.0	200	
Input Bias Current	I_B	$T_J = 25°C$ (Note 1)	–	15	100	–	15	200	–	15	300	pA
		Device Operating	–	18	300	–	18	400	–	18	600	
Input Resistance	R_{IN}		–	10^{12}	–	–	10^{12}	–	–	10^{12}	–	Ω
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	150	500	–	75	220	–	50	200	–	V/mV
Output Voltage Swing	V_O	$R_L = 10k\Omega$	±12	±13	–	±12	±13	–	±12	±13	–	V
		$R_L = 2k\Omega$	±11	±12.7	–	±11	±12.7	–	±11	±12.7	–	
Supply Current	I_{SY}		–	6.0	8.5	–	6.0	8.5	–	7.0	10.0	mA
		'G' Grade	–	–	–	–	–	–	–	7.0	12.0	
Slew Rate	SR	$A_{VCL} = +1.0$ (Note 3)	10.0	18	–	7.5	18	–	5.0	15	–	V/μs
Gain Bandwidth Product	GBW	(Note 3)	3.5	5.7	–	3.5	5.7	–	3.0	5.4	–	MHz
Closed Loop Bandwidth	CLBW	$A_{VCL} = +1.0$	–	13	–	–	13	–	–	12	–	MHz
Settling Time	t_s	to 0.01%	–	2.3	–	–	2.3	–	–	2.4	–	μs
		to 0.05% (Note 2)	–	1.1	–	–	1.1	–	–	1.2	–	
		to 0.10%	–	0.9	–	–	0.9	–	–	1.0	–	
Input Voltage Range	IVR		+10.2	+14.8	–	+10.2	+14.8	–	+10.1	+14.8	–	V
			-10.2	-11.5	–	-10.2	-11.5	–	-10.1	-11.5	–	
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$ A, B, C Grades	86	100	–	86	100	–	82	96	–	dB
		$V_{CM} = \pm IVR$ E, F, G Grades	82	100	–	82	100	–	80	96	–	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 16V$	–	10	51	–	10	80	–	–	–	μV/V
		$V_S = \pm 10V$ to $\pm 15V$	–	–	–	–	–	–	–	16	100	
Input Noise Voltage Density	e_n	$f_o = 100Hz$	–	20	–	–	20	–	–	20	–	nV/√Hz
		$f_o = 1000Hz$	–	15	–	–	15	–	–	15	–	
Input Noise Current Density	i_n	$f_o = 100Hz$	–	0.01	–	–	0.01	–	–	0.01	–	pA/√Hz
		$f_o = 1000Hz$	–	0.01	–	–	0.01	–	–	0.01	–	
Input Capacitance	C_{IN}		–	3.0	–	–	3.0	–	–	3.0	–	pF

NOTES:

1. Input bias current is specified for two different conditions. The $T_j = 25°C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at 25°C ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs T_j and I_B vs T_A. PMI has a bias current compensation circuit which gives improved bias current and bias current over temperature vs standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Settling time is defined here for a unity gain inverter connection using 2kΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within a specified percent of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.
3. Sample tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	OP-215A MIN	OP-215A TYP	OP-215A MAX	OP-215B MIN	OP-215B TYP	OP-215B MAX	OP-215C MIN	OP-215C TYP	OP-215C MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	–	0.5	2.0	–	1.5	3.0	–	3.0	6.0	mV
Average Input Offset Voltage Drift												
Without External Trim	TCV_{OS}	(Note 3)	–	3.0	10	–	3.0	10	–	6.0	–	µV/°C
With External Trim	TCV_{OSn}	$R_P = 100k\Omega$	–	3.0	–	–	3.0	–	–	4.0	–	
Input Offset Current (Note 1)	I_{OS}	$T_J = +125°C$	–	0.8	8	–	0.8	8	–	1.0	12	nA
		$T_A = +125°C$ Device Operating	–	1.2	14	–	1.2	14	–	1.5	22	
Input Bias Current (Note 1)	I_B	$T_J = +125°C$	–	1.5	10	–	1.5	10	–	1.8	15	nA
		$T_A = +125°C$, Device Operating	–	2.2	18	–	2.2	18	–	2.7	28	
Input Voltage Range	IVR		+10.2	+14.6	–	+10.2	+14.6	–	+10.1	+14.6	–	V
			-10.2	-11.3	–	-10.2	-11.3	–	-10.1	-11.3	–	
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	82	97	–	82	97	–	80	93	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 16V$	–	10	100	–	15	100	–	–	–	µV/V
		$V_S = \pm 10V$ to $\pm 15V$	–	–	–	–	–	–	–	23	126	
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	30	110	–	30	110	–	25	100	–	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12	±13	–	±12	±13	–	±12	±13	–	V

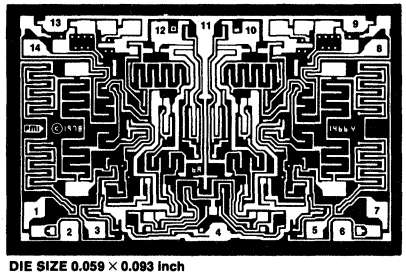
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \leq T_A \leq +70°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	OP-215E MIN	OP-215E TYP	OP-215E MAX	OP-215F MIN	OP-215F TYP	OP-215F MAX	OP-215G MIN	OP-215G TYP	OP-215G MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	–	0.4	1.65	–	1.4	2.65	–	3.5	8.0	mV
Average Input Offset Voltage Drift												
Without External Trim	TCV_{OS}	(Note 3)	–	3.0	15	–	3.0	15	–	6.0	–	µV/°C
With External Trim	TCV_{OSn}	$R_P = 100k\Omega$	–	3.0	–	–	3.0	–	–	4.0	–	
Input Offset Current (Note 1)	I_{OS}	$T_J = +70°C$	–	0.06	0.45	–	0.06	0.45	–	0.08	0.65	nA
		$T_A = +70°C$, Device Operating	–	0.08	0.80	–	0.08	0.80	–	0.10	1.2	
Input Bias Current (Note 1)	I_B	$T_J = +70°C$	–	0.12	0.70	–	0.12	0.70	–	0.14	0.9	nA
		$T_A = +70°C$, Device Operating	–	0.16	1.40	–	0.16	1.40	–	0.19	1.8	
Input Voltage Range	IVR		+10.2	+14.7	–	+10.2	+14.7	–	+10.1	+14.7	–	V
			-10.2	-11.4	–	-10.2	-11.4	–	-10.1	-11.3	–	
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	80	98	–	80	98	–	76	94	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 16V$	–	13	100	–	13	100	–	–	–	µV/V
		$V_S = \pm 10V$ to $\pm 15V$	–	–	–	–	–	–	–	20	159	
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	50	180	–	50	180	–	35	130	–	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12	±13	–	±12	±13	–	±12	±13	–	V

NOTES:

1. Input bias current is specified for two different conditions. The $T_j = 25°C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at 25° C ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs T_j and I_B vs T_A. PMI has a bias current compensation circuit which gives improved bias current and bias current over temperature vs standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Settling time is defined here for a unity gain inverter connection using 2kΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within a specified percent of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.
3. Sample tested.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



DIE SIZE 0.059 × 0.093 inch
All V+ PADS ARE INTERNALLY CONNECTED

1. INVERTING INPUT (A)
2. NON-INVERTING INPUT (A)
3. NULL (A)
4. V–
5. NULL (B)
6. NON-INVERTING INPUT (B)
7. INVERTING INPUT (B)
8. NULL (B)
9. V+
10. V_O(B)
11. V+
12. V_O(A)
13. V+
14. NULL (A)

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$ for OP-215N, OP-215G and OP-215GR devices, $T_A = +125°C$ for OP-215NT and OP-215GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-215NT LIMIT	OP-215N LIMIT	OP-215GT LIMIT	OP-215G LIMIT	OP-215GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	2.0	1.0	3.0	2.0	6.0	mV MAX
Input Bias Current	I_B		18	—	18	—	—	nA MAX
Input Offset Current	I_{OS}		14	—	14	—	—	nA MAX
Large Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$, $R_L = 2k\Omega$	30	150	30	75	50	V/mV MIN
Input Voltage Range	IVR		±10.2	±10.2	±10.2	±10.2	±10.1	V MIN
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	82	86	82	86	82	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10$ to $\pm 16V$ $V_S = \pm 10$ to $\pm 15V$	100 —	51 —	100 —	80 —	— 100	μV/V MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 —	± 12 ± 11	±12	± 12 ± 11	± 12 ± 11	V MIN
Supply Current	I_{SY}		—	8.5	—	8.5	12.0	mA MAX

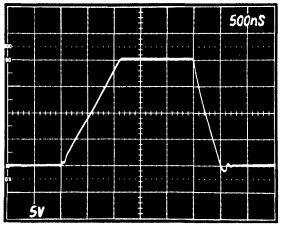
NOTE: For 25°C characteristics of NT & GT devices, see N&G characteristics respectively.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

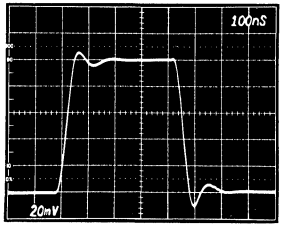
PARAMETER	SYMBOL	CONDITIONS	OP-215NT TYP	OP-215N TYP	OP-215GT TYP	OP-215G TYP	OP-215GR TYP	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	Unnulled $R_p = 100k\Omega$	2.0	2.0	3.0	3.0	4.0	μV/°C
Average Input Offset Voltage Drift	TCV_{OSn}	Nulled $R_p = 100k\Omega$	0.5	0.5	1	1	2	μV/°C
Input Offset Current	I_{OS}		3.0	3.0	3.0	3.0	3.0	pA
Input Bias Current	I_B		15	15	15	15	15	pA
Slew Rate	SR	$A_{VCL} = +1$	17	17	16	16	15	V/μs
Settling Time	t_s	to 0.01% to 0.05% to 0.10%	2.2 1.1 0.9	2.2 1.1 0.9	2.3 1.1 0.9	2.3 1.1 0.9	2.4 1.2 1.0	μs
Gain Bandwidth Product	GBW		6.0	6.0	5.7	5.7	5.4	MHz
Closed Loop Bandwidth	CLBW	$A_{VCL} = +1$	14	14	13	13	12	MHz
Input Noise Voltage Density	e_n	$f_o = 100Hz$ $f_o = 1000Hz$	20 15	20 15	20 15	20 15	20 15	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	$f_o = 100Hz$ $f_o = 1000Hz$	0.01	0.01	0.01	0.01	0.01	$pA/\sqrt{Hz}$
Input Capacitance	C_{IN}		3	3	3	3	3	pF

TYPICAL PERFORMANCE CURVES

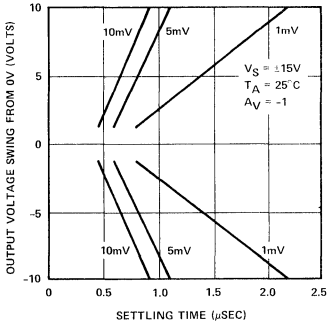
LARGE SIGNAL TRANSIENT RESPONSE



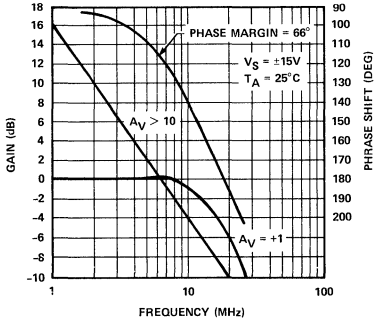
SMALL SIGNAL TRANSIENT RESPONSE



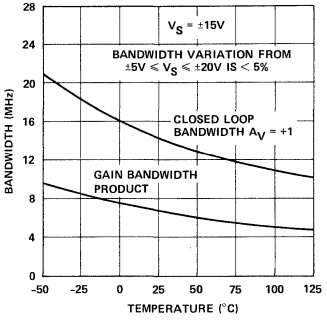
SETTLING TIME



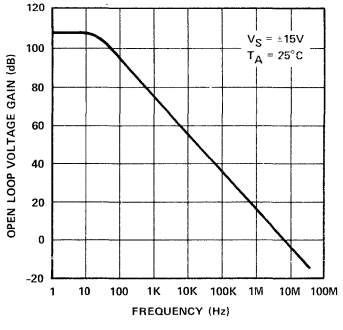
CLOSED LOOP BANDWIDTH AND PHASE SHIFT vs FREQUENCY



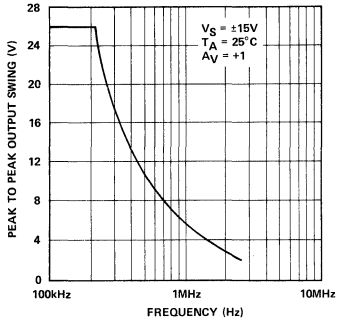
BANDWIDTH vs TEMPERATURE



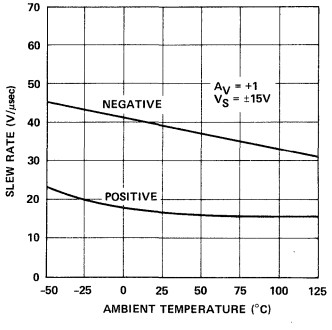
OPEN LOOP FREQUENCY RESPONSE



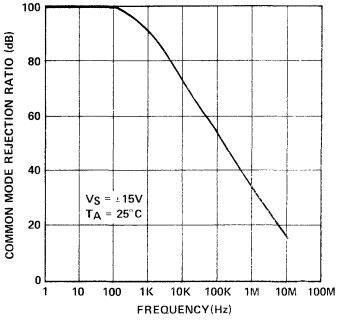
UNDISTORTED OUTPUT SWING



SLEW RATE vs TEMPERATURE

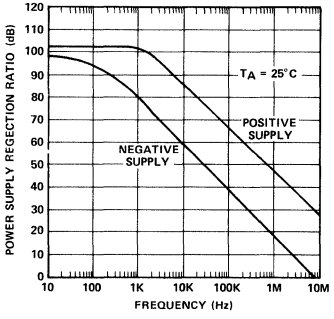


COMMON MODE REJECTION RATIO vs FREQUENCY

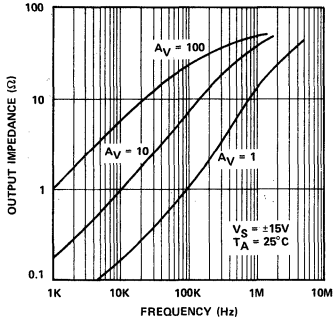


TYPICAL PERFORMANCE CURVES

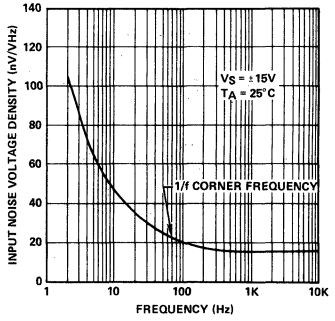
POWER SUPPLY REJECTION vs FREQUENCY



OUTPUT IMPEDANCE vs FREQUENCY

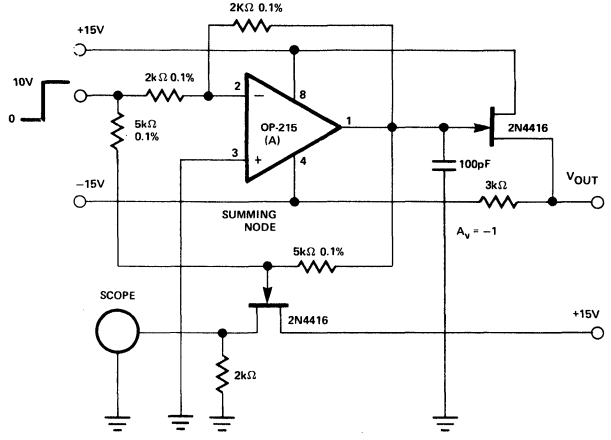


VOLTAGE NOISE vs FREQUENCY



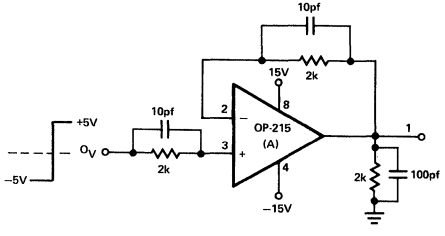
BASIC CONNECTIONS

SETTLING TIME TEST CIRCUIT



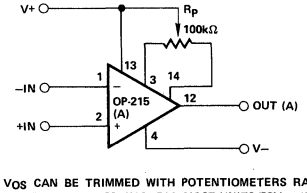
(PINOUT FOR "J" AND "Z" PACKAGES ONLY)

SLEW RATE TEST CIRCUIT



(PINOUT FOR "J" AND "Z" PACKAGES ONLY)

INPUT OFFSET VOLTAGE NULLING

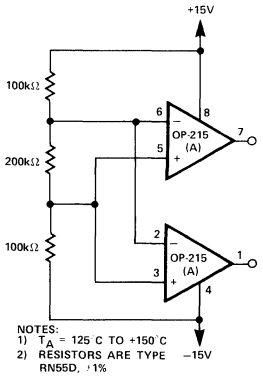


NOTE: V_{OS} CAN BE TRIMMED WITH POTENTIOMETERS RANGING FROM 10kΩ TO 1MΩ. FOR MOST UNITS TCV_{OS} WILL BE MINIMUM WHEN V_{OS} IS ADJUSTED WITH A 100kΩ POTENTIOMETER.

("Y" PACKAGE ONLY)

BASIC CONNECTIONS

TYPICAL BURN-IN CIRCUIT



("J" AND "Z" PACKAGES ONLY)

APPLICATION INFORMATION

DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground sets the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency, a lead capacitor should be placed from the output to the negative input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

OP-220

MICROPOWER PRECISION DUAL OPERATIONAL AMPLIFIER

SINGLE OR DUAL SUPPLY

FEATURES

- **Tight TCV_{OS} Match ..... 1μV/° C Max**
- **Low Input Offset Voltage ..... 100μV Max**
- **Low Supply Current 100μA**
- **Single Supply Operation ..... +3V to +30V**
- **Low Input Offset Voltage Drift ..... 0.75μV/° C**
- **High Open Loop Gain 1000V/mV**
- **High PSRR 114dB**
- **Single Chip Construction**
- **Low Input Bias Current 12nA**
- **Wide Common Mode Voltage Range from V– to Within 1.5V of V+**
- **Pin Compatible with 1458, LM158, LM2902, 747**

GENERAL DESCRIPTION

The OP-220 is a monolithic dual operational amplifier that can be used either in single or dual supply operation. Offset voltages as low as 80μV and input offset voltage tracking as low as 0.75μV/° C make this the first micropower precision dual operational amplifier.

The excellent specifications of the individual amplifiers combined with the tight matching and temperature tracking between channels enables realization of extremely high performance instrumentation amplifier designs without resorting to laborious and expensive selection and matching of discrete amplifiers. The individual amplifiers feature extremely low input offset voltage, low offset voltage drift, low noise voltage, low bias current and are completely compensated and protected.

Matching between channels is provided on all critical parameters including input offset voltage, tracking of offset voltage vs. temperature, non-inverting bias currents, and common mode and power supply rejection ratios.

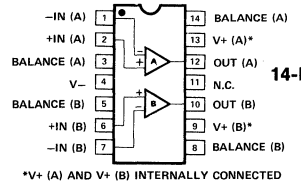
ORDERING INFORMATION †

T_A = 25° C V_{OS} MAX (μV)	PACKAGE TO-99 8-PIN	HERMETIC DIP 8-PIN	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
150	OP220AJ*	OP220AZ*	OP220AY*	MIL
150	OP220EJ	OP220EZ	OP220EY	IND
300	OP220BJ*	OP220BZ*	OP220BY*	MIL
300	OP220FJ	OP220FZ	OP220FY	IND
750	OP220CJ*	OP220CZ*	OP220CY*	MIL
750	OP220GJ	OP220GZ	OP220GY	IND
1000	OP220HJ	OP220HZ	OP220HY	COM

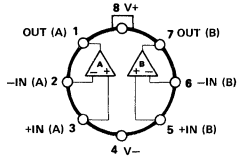
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number.

†All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

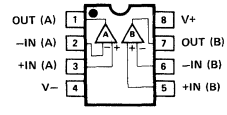
PIN CONNECTIONS



14-PIN HERMETIC DIP (Y-Suffix)

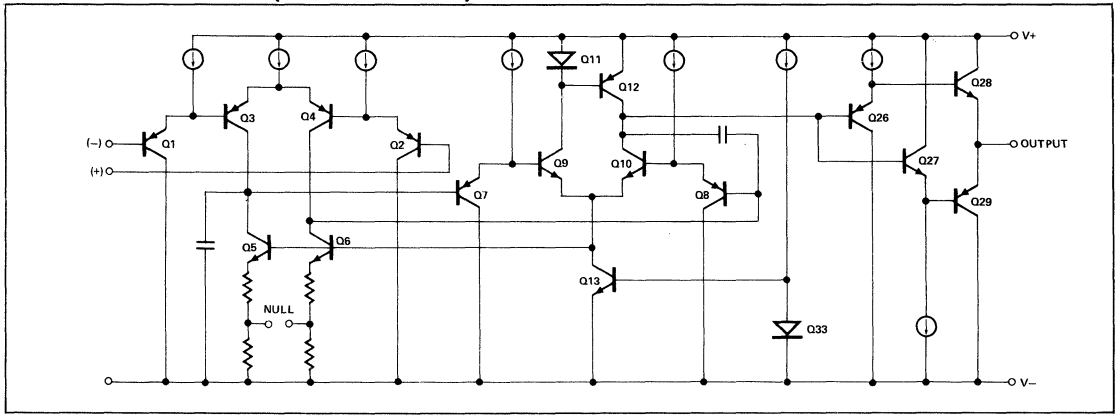


TO-99 (J-Suffix)



8-PIN HERMETIC DIP (Z-Suffix)

SIMPLIFIED SCHEMATIC (EACH AMPLIFIER)



ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±18V
Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... 30V or Supply Voltage
Input Voltage ..... Supply Voltage
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range —

OP-220 A, B, C ..... −55°C to +125°C
OP-220 E, F, G ..... −25°C to +85°C
OP-220 H ..... 0°C to +70°C

Lead Temperature (Soldering, 60 sec) ..... 300°C
DICE Junction Temperature ..... −65°C to +150°C

NOTES:
1. See table for maximum ambient temperature rating and derating factor.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
14-Pin Hermetic DIP (Y)	100°C	10.0mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C

2. Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

5

OPERATIONAL AMPLIFIERS OP-220

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-220A/E MIN	OP-220A/E TYP	OP-220A/E MAX	OP-220B/F MIN	OP-220B/F TYP	OP-220B/F MAX	UNITS
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$ $V_S = \pm 7.5V$	— —	120 80	150 100	— —	250 150	300 200	µV
Input Offset Current	I_{OS}		—	0.15	1.5	—	0.2	2.0	nA
Input Bias Current	I_B		—	12	20	—	13	20	nA
Input Voltage Range	IVR	V+ = +5V, V− = 0V $V_S = \pm 15V$	0 +13.8/-15.0	— —	3.8 —	0 +13.8/-15.0	— —	3.8 —	V
Common Mode Rejection Ratio	CMRR	V+ = +5V, V− = 0V $0V \le V_{CM} \le 3.5V$ $V_S = \pm 15V$ $-15V \le V_{CM} \le 13.5V$	97 100	102 104	— —	94 98	98 102	— —	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ V− = 0V, V+ = 5V to 30V	— —	2 4	4 7	— —	4 7	7 10	µV/V
Large Signal Voltage Gain	A_{VO}	V+ = + 5V, V− = 0V, R_L = 100KΩ (Note 1) $V_S = \pm 15V$, R_L = 25kΩ	500 1000	1000 2000	— —	500 1000	800 2000	— —	V/mV
Output Voltage Swing	V_O	V+ = +5V, V− = 0V, R_L = 10kΩ $V_S = \pm 15V$, R_L = 25kΩ	0.7 ±14.0	— —	4.0 —	0.7 ±14.0	— —	4.0 —	V
Closed Loop Bandwidth	BW	A_{VCL} = +1.0, R_L = 25kΩ	—	150	—	—	150	—	kHz
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load $V_S = \pm 15V$, No Load	— —	100 140	115 170	— —	115 150	125 170	µA

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55°C \le T_A \le +125°C$ for OP-220A and B, $-25°C \le T_A \le +85°C$ for OP-220E and F, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-220A/E MIN	OP-220A/E TYP	OP-220A/E MAX	OP-220B/F MIN	OP-220B/F TYP	OP-220B/F MAX	UNITS
Average Input Offset Voltage Drift (Note 1)	TCV_{OS} TCV_{OSn}	Unnulled, $V_S = \pm 7.5V$ Nulled, R_p = 10kΩ, $V_S = \pm 7.5V$	— —	0.75 0.75	1.0 1.0	— —	1.0 1.0	1.5 1.5	µV/°C
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$ $V_S = \pm 7.5V$	— —	200 150	300 200	— —	400 300	500 350	µV
Input Offset Current	I_{OS}		—	0.5	2	—	0.6	2.5	nA
Input Bias Current	I_B		—	12	25	—	13	25	nA
Input Voltage Range	IVR	V+ = +5V, V− = 0V $V_S = \pm 15V$	0 +13.5/−15.0	— —	3.5 —	0 +13.5/−15.0	— —	3.5 —	V
Common Mode Rejection Ratio	CMRR	V+ = +5V, V− = 0V $0V \le V_{CM} \le 3.0$ $V_S = \pm 15V$ $-15V \le V_{CM} \le 13.0$	93 96	98 100	— —	90 94	94 98	— —	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ V− = 0V, V+ = 5V to 30V	— —	4 8	7 13	— —	8 13	13 20	µV/V
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, R_L = 50KΩ	500	1000	—	500	800	—	V/mV
Output Voltage Swing	V_O	V+ = 5V, V− = 0V, R_L = 20kΩ $V_S = \pm 15V$, R_L = 50KΩ	0.9 ±13.8	— —	3.8 —	0.9 ±13.8	— —	3.8 —	V
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, or +5V, 0V, No Load $V_S = \pm 15V$, No Load	— —	135 190	170 250	— —	155 200	185 250	µA

NOTES:
1. Sample tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$ and $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-220C/G MIN	OP-220C/G TYP	OP-220C/G MAX	OP-220H MIN	OP-220H TYP	OP-220H MAX	UNITS
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	500	750	—	750	1000	µV
		$V_S = \pm 7.5V$	—	300	500	—	500	1000	
Input Offset Current	I_{OS}		—	0.2	3.5	—	0.2	5.0	nA
Input Bias Current	I_B		—	14	30	—	14	40	nA
Input Voltage Range	IVR	V+ = +5V, V- = 0V	0	—	3.8	0	—	3.6	V
		$V_S = \pm 15V$	+13.8/–15.0	—	—	+13.6/–15.0	—	—	
Common Mode Rejection Ratio	CMRR	V+ = +5V, V- = 0V $0V \le V_{CM} \le 3.5V$	90	94	—	80	86	—	dB
		$V_S = \pm 15V$ $-15V \le V_{CM} \le 13.5V$	92	96	—	80	86	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	10	16	—	16	51	µV/V
		V- = 0V, V+ = 5V to 30V	—	16	26	—	20	51	
Large Signal Voltage Gain	A_{VO}	V+ = + 5V, V- = 0V, $R_L = 100K\Omega$ (Note 1)	300	500	—	200	300	—	V/mV
		$V_S = \pm 15V$, $R_L = 25k\Omega$	800	1600	—	500	800	—	
Output Voltage Swing	V_O	V+ = +5V, V- = 0V, $R_L = 10k\Omega$	0.8	—	4.0	0.8	—	3.8	V
		$V_S = \pm 15V$, $R_L = 25k\Omega$	±14.0	—	—	±13.8	—	—	
Closed Loop Bandwidth	BW	$A_{VCL} = +1.0$, $R_L = 25k\Omega$	—	150	—	—	150	—	kHz
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load	—	125	135	—	135	170	µA
		$V_S = \pm 15V$, No Load	—	205	220	—	220	300	

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55°C \le T_A \le +125°C$ for OP-220C, $-25°C \le T_A \le +85°C$ for OP-220G, and $0°C \le T_A \le 70°C$ for OP-220H, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-220C/G MIN	OP-220C/G TYP	OP-220C/G MAX	OP-220H MIN	OP-220H TYP	OP-220H MAX	UNITS
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnulled, $V_S = \pm 7.5V$	—	2.0	3.0	—	4.0	7.0	µV/°C
	TCV_{OSn}	Nulled, $R_p = 10k\Omega$, $V_S = \pm 7.5V$	—	2.0	3.0	—	4.0	7.0	
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	1000	1300	—	1600	3200	µV
		$V_S = \pm 7.5V$	—	750	800	—	850	1700	
Input Offset Current	I_{OS}		—	0.8	5	—	1.0	10	nA
Input Bias Current	I_B		—	14	40	—	14	60	nA
Input Voltage Range	IVR	V+ = +5V, V- = 0V	0	—	3.5	0	—	3.3	V
		$V_S = \pm 15V$	–15.0/+13.5	—	—	–15.0/+13.3	—	—	
Common Mode Rejection Ratio	CMRR	V+ = +5V, V- = 0V $0V \le V_{CM} \le 3.0$	86	90	—	76	80	—	dB
		$V_S = \pm 15V$ $-15V \le V_{CM} \le 13.0$	88	92	—	76	80	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	20	32	—	51	100	µV/V
		V- = 0V, V+ = 5V to 30V	—	32	51	—	51	100	
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 50K\Omega$	400	500	—	250	400	—	V/mV
Output Voltage Swing	V_O	V + = 5V, V- = 0V, $R_L = 20K\Omega$	1.0	—	3.8	1.1	—	3.5	V
		$V_S = \pm 15V$, $R_L = 50K\Omega$	±13.8	—	—	±13.5	—	—	
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, or +5V, 0V, No Load	—	170	210	—	180	260	µA
		$V_S = \pm 15V$, No Load	—	275	330	—	300	450	

NOTES:
1. Sample tested.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-220A/E MIN	OP-220A/E TYP	OP-220A/E MAX	OP-220B/F MIN	OP-220B/F TYP	OP-220B/F MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	150	300	—	250	500	µV
Average Non-Inverting Bias Current	I_{B^+}		—	10	20	—	15	20	nA
Non-Inverting Offset Current	I_{OS^+}		—	0.7	1.5	—	1.0	2.0	nA
Inverting Offset Current	I_{OS^-}		—	0.7	1.5	—	1.0	2.0	nA
Common Mode Rejection Ratio Match	ΔCMRR	V_{CM} = −15V to +13.5V	98	106	—	92	98	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	4	7	—	7	13	µV/V
Channel Separation		J Package Y and Z Packages	98 108	100 111	— —	98 108	100 111	— —	dB

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ for OP-220A and B, $-25°C \leq T_A \leq +85°C$ for OP-220E and F, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-220A/E MIN	OP-220A/E TYP	OP-220A/E MAX	OP-220B/F MIN	OP-220B/F TYP	OP-220B/F MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	250	500	—	400	800	µV
Input Offset Voltage Tracking									
Without External Trim	$TC\Delta V_{OS}$		—	0.4	0.9	—	1.0	2.5	µV°C
With External Trim	$TC\Delta V_{OSn}$	$R_p = 20k\Omega$	—	0.5	1.0	—	1.0	2.5	
Average Non-Inverting Bias Current	I_{B^+}		—	10	25	—	15	25	nA
Average Drift of Non-Inverting Bias Current	TCI_{B^+}		—	15	25	—	15	25	pA/°C
Non-Inverting Offset Current	I_{OS^+}		—	0.7	2.0	—	1.0	2.5	nA
Average Drift of Non-Inverting Offset Current	TCI_{OS^+}		—	7	15	—	12	22.5	pA/°C
Inverting Offset Current	I_{OS^-}		—	0.7	2.0	—	1.0	2.5	nA
Common Mode Rejection Ratio Match	ΔCMRR	V_{CM} = −15V to +13.0V	94	104	—	90	96	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	5	10	—	10	20	µV/V

NOTE:
The above characteristics are sample tested.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

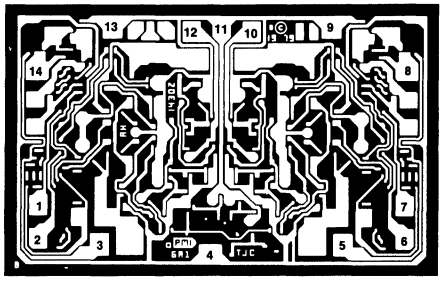
PARAMETER	SYMBOL	CONDITIONS	OP-220C/G MIN	OP-220C/G TYP	OP-220C/G MAX	OP-220H MIN	OP-220H TYP	OP-220H MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	300	600	—	600	1000	µV
Average Non-Inverting Bias Current	I_B^+		—	20	30	—	30	40	nA
Non-Inverting Offset Current	I_{OS}^+		—	1.4	2.5	—	2.5	4.0	nA
Inverting Offset Current	I_{OS}^-		—	1.4	2.5	—	2.5	4.0	nA
Common Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = -15V$ to $+13.5V$	86	92	—	74	80	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	16	32	—	51	100	µV/V
Channel Separation		J Package Y and Z Packages	98 108	100 111	— —	98 108	108 111	— —	dB

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ for OP-220C, $-25°C \leq T_A \leq +85°C$ for OP-220G, and $0°C \leq T_A \leq +70°C$ for OP-220H, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-220C/G MIN	OP-220C/G TYP	OP-220C/G MAX	OP-220H MIN	OP-220H TYP	OP-220H MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	800	1800	—	1000	2500	µV
Input Offset Voltage Tracking									
Without External Trim	$TC\Delta V_{OS}$		—	1.5	5.0	—	7	10	µV°C
With External Trim	$TC\Delta V_{OSn}$	$R_p = 20k\Omega$	—	1.5	5.0	—	7	10	
Average Non-Inverting Bias Current	I_B^+		—	22	40	—	40	60	nA
Average Drift of Non-Inverting Bias Current	TCI_B^+		—	30	50	—	50	70	pA/°C
Non-Inverting Offset Current	I_{OS}^+		—	2.5	5.0	—	5	10	nA
Average Drift of Non-Inverting Offset Current	TCI_{OS}^+		—	15	30	—	30	50	pA/°C
Inverting Offset Current	I_{OS}^-		—	3.0	5.0	—	7	10	nA
Common Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = -15V$ to $+13.0V$	82	90	—	72	76	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	20	51	—	100	159	µV/V

NOTE:
The above characteristics are sample tested.

DICE CHARACTERISTICS



1. INVERTING INPUT (A)
2. NON-INVERTING INPUT (A)
3. BALANCE (A)
4. V–
5. BALANCE (B)
6. NON-INVERTING INPUT (B)
7. INVERTING INPUT (B)
8. BALANCE (B)
9. V+
10. OUT (B)
11. V+
12. OUT (A)
13. V+
14. BALANCE (A)

DIE SIZE 0.095 × 0.061 inch
NOTE: ALL V+ PADS ARE INTERNALLY CONNECTED.

See Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

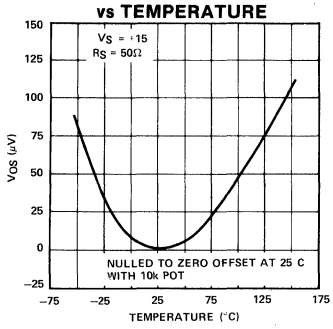
PARAMETER	SYMBOL	CONDITIONS	OP-220N LIMIT	OP-220G LIMIT	OP-220GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	V+ = +7.5V V– = –7.5V	200	500	1000	μV MAX
Input Offset Current	I_{OS}		2.0	3.5	5.0	nA MAX
Input Bias Current	I_B		20	30	40	nA MAX
Input Voltage Range	IVR		+13.8/–15.0	+13.8/–15.0	+13.6/–15.0	V MIN
Common Mode Rejection Ratio	CMRR	V – = 0V, V+ = + 5V, $0V \le V_{CM} \le 3.5V$ $V_S = \pm 15V$, $-15V \le V_{CM} \le 13.5V$	94 98	90 92	80 80	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ V– = 0V, V+ = +5V to +30V	10 10	16 26	51 51	μV/V MAX
Large Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$	1000	800	500	V/mV MIN
Output Voltage Swing	V_O	V+ = +5V, V– = 0V, $R_L = 100k\Omega$ $V_S = \pm 15V$, $R_L = 25k\Omega$	0.7/4.0 ±14.0	0.8/4.0 ±14.0	0.8/3.8 ±13.8	V MIN
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No load $V_S = \pm 15V$, No load	125 170	135 220	170 300	μA MAX

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

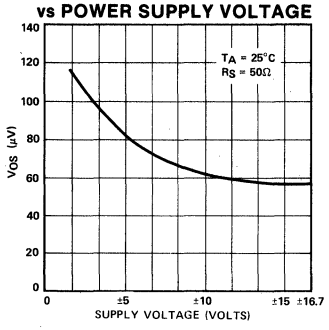
PARAMETER	SYMBOL	CONDITIONS	OP-220N TYPICAL	OP-220G TYPICAL	OP-220GR TYPICAL	UNITS
Average Input Offset	TCV_{OS}	Unnulled	1.0	1.5	3.0	μV/°C
Voltage Drift	TCV_{OSn}	Nulled, $R_P = 10k\Omega$	1.0	1.5	3.0	
Large Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$	2000	1600	800	V/mV

TYPICAL PERFORMANCE CURVES

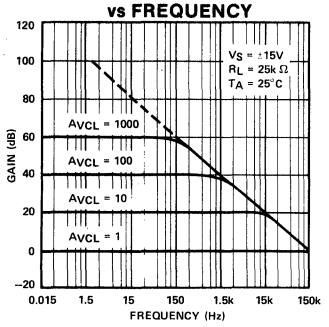
TRIMMED OFFSET VOLTAGE vs TEMPERATURE



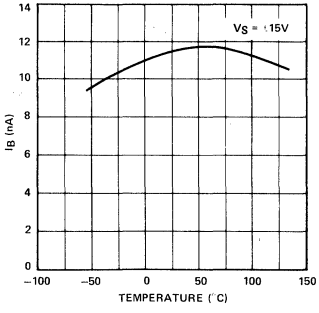
INPUT OFFSET VOLTAGE vs POWER SUPPLY VOLTAGE



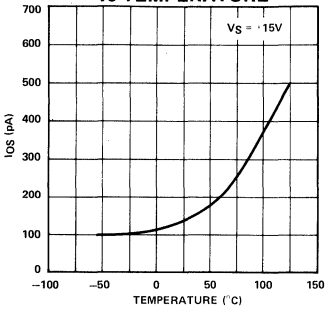
CLOSED LOOP GAIN vs FREQUENCY



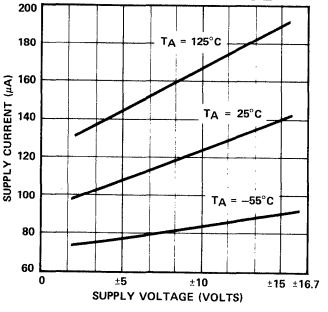
INPUT BIAS CURRENT vs TEMPERATURE



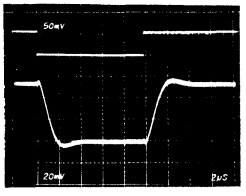
INPUT OFFSET CURRENT vs TEMPERATURE

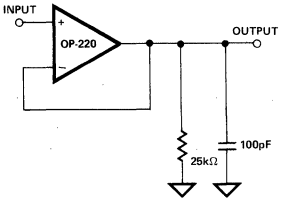


SUPPLY CURRENT vs SUPPLY VOLTAGE

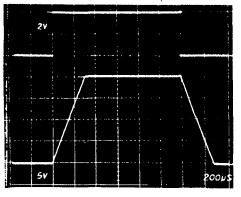


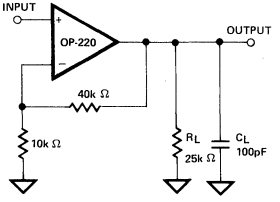
SMALL SIGNAL TRANSIENT RESPONSE





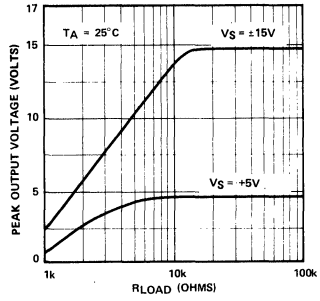
LARGE SIGNAL TRANSIENT RESPONSE



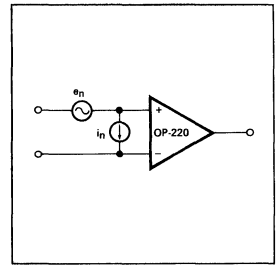


TYPICAL PERFORMANCE CURVES

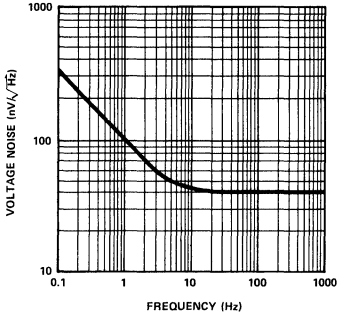
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



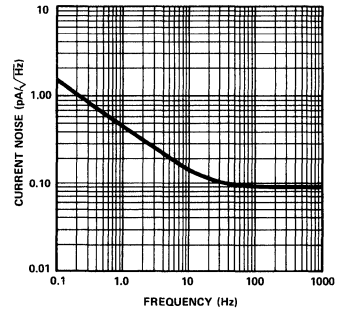
NOISE CIRCUIT MODEL



VOLTAGE NOISE DENSITY (e_n) vs FREQUENCY



CURRENT NOISE DENSITY (i_n) vs FREQUENCY



SPECIAL NOTES ON THE APPLICATION OF DUAL MATCHED OPERATIONAL AMPLIFIERS

ADVANTAGES OF DUAL MONOLITHIC OPERATIONAL AMPLIFIERS

Dual Matched Operational Amplifiers provide the engineer with a powerful tool for the solution of a number of difficult circuit design problems, including true instrumentation amplifiers, extremely low drift, high common mode rejection DC amplifiers, low DC drift active filters, dual tracking voltage references, and many other demanding applications. These designs are based on the principle that careful matching between two operationsal amplifiers can, to a large extent, eliminate the effect of DC errors inherent in the individual amplifiers.

Reference to the circuit shown in Figure 1, a differential-in, differential-out amplifier, shows how the reductions in error can be accomplished. Assuming the resistors used are ideally matched, the gain of each side will be identical. If the offset voltages of each amplifier are perfectly matched, then the net differential voltage at the amplifier's output will be

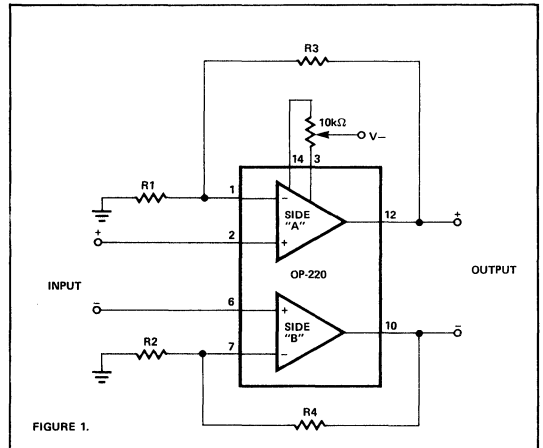


FIGURE 1.

Y PACKAGE ONLY

zero. Note that the output offset error of this amplifier is not a function of the offset voltage of the individual amplifiers, but only a function of the *difference* (degree of matching) between the amplifiers' offset voltages. This error-cancellation principle holds for a considerable number of input referred error parameters — offset voltage, offset voltage drift, inverting and non-inverting bias currents, common-mode and power supply rejection ratios. Note also that the impedances of each input, both common-mode and differential mode, are extremely high and can also be tightly matched, an important feature not possible with single operational amplifier circuits. Common mode rejection can be made exceptionally high; this is especially important in instrumentation amplifiers where errors due to large common-mode voltages can be far greater than those due to noise or drift with temperature. For example, consider the case of two op amps, each with 80dB (100μV/V) CMRR. However, if the CMRR of one device is +100μV/V while CMRR of the other is -100μV/V for a net 200μV/V CMRR match, the resultant input referred error over a 10V common-mode input signal will be 2mV.

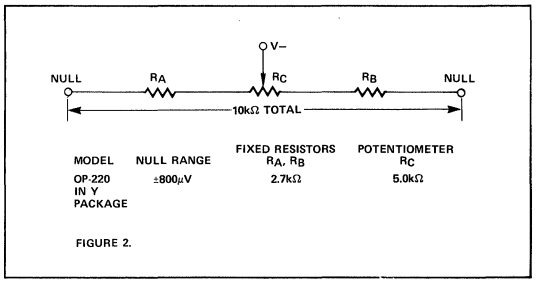


FIGURE 2.

OFFSET TRIMMING — Y PACKAGE ONLY

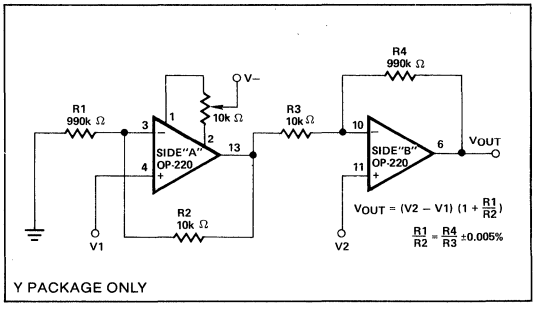
Offset trimming terminals are provided for each amplifier of the OP-220.

The OP-220 is designed to provide lowest drift performance when trimmed with a 10kΩ potentiometer; this value provides about ±4mV of adjustment range which should be considerably more than adequate for most applications. Where finer resolution of trimming is desired, or where unwanted changes in potentiometer position with time and temperature could create unacceptable offsets, the sensitivity to offset vs. potentiometer position may be reduced by using the circuit of Figure 2.

INSTRUMENTATION AMPLIFIERS USING OP-220

Instrumentation Amplifiers with performance surpassing those costing many hundreds of dollars can be easily and compactly built using the OP-220. The 3-amplifier design, while more complex, has the advantages of convenient overall gain adjustment by trimming a single resistor (R_3) and of wide common-mode voltage handling capability at any overall gain, plus improved gain linearity. Slew rate, small signal bandwidth, and full power bandwidthare also superior and may be further improved by choosing a high-speed op-amp such as the OP-21 series for the output op-amp.

INSTRUMENTATION AMPLIFIER 2 OP-AMP DESIGN



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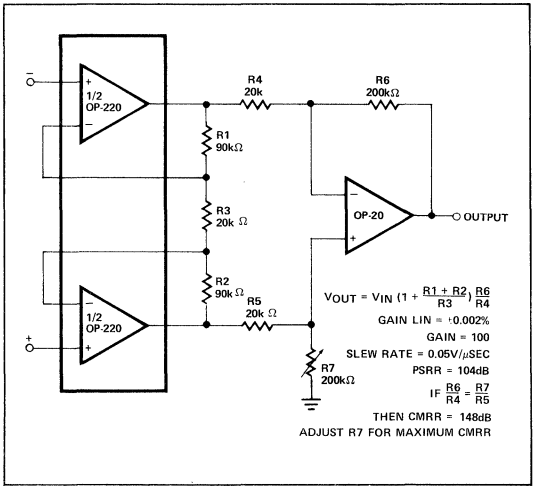
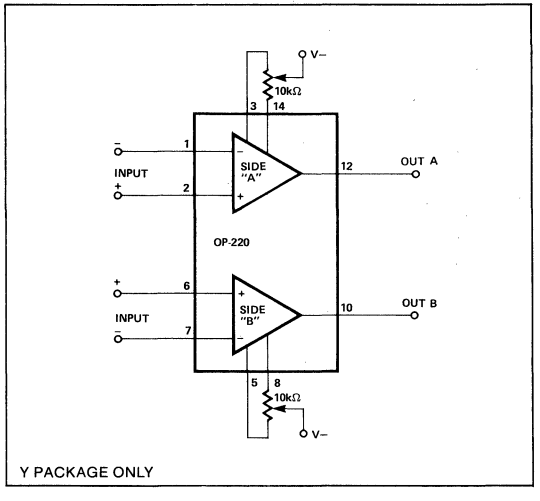
INSTRUMENTATION AMPLIFIER — 3 OP-AMP DESIGN



OFFSET NULLING CIRCUIT



Y PACKAGE ONLY

OP-227

ULTRA-LOW NOISE, LOW OFFSET DUAL INSTRUMENTATION OPERATIONAL AMPLIFIER

FEATURES

- **Excellent Individual Amplifier Parameters**
- **Low V_{OS}** ..... **20 μV**
- **Tight Offset Voltage Match** ..... **25 μV**
- **Tight Offset Voltage Match vs. Temperature** ... **0.3 μV/° C**
- **Unprecedented Low Noise** { ..... **3nV/√Hz** ; ..... **0.2 μVp-p**
- **Fast** ..... **2.8 V/μsec**
  ..... **8 MHz**
- **Stable** ..... **0.3 μV/° C**
  ..... **0.2 μV/Mo**
- **High Gain** ..... **1.8 million**
- **Excellent Gain Match** **1.5%**
- **High Channel Separation** ..... **154 db**

GENERAL DESCRIPTION

The OP-227 is the first dual amplifier to offer a combination of low offset, low noise, high speed and guaranteed amplifier matching characteristics in one device. The OP-227 with a V_{OS} match of 25μV, a TCV_{OS} match of 0.3μV/° C, and a 1/f corner of only 2.7 Hz is the best choice for precision low noise design. These D.C. characteristics coupled with a slew rate of 2.8 V/μs and a small-signal bandwidth of 8 MHz allow the designer to achieve AC performance previously unattainable with op-amp based instrumentation designs.

When utilized in a three op-amp instrumentation amplifier configuration, the OP-227 can easily achieve a CMRR in excess of 100 db at 10 KHz. In addition, this device has an open-loop gain of 1.5 M with a 1KΩ load and a gain match of 1.5% between amplifiers. The OP-227 also features an I_B of ±10nA, an I_{OS} of 7nA, and guaranteed matching of input currents between amplifiers. These outstanding input current specifications are realized through the use of a unique input-current cancellation circuit which typically holds I_B and I_{OS} to ±20 nA and 15 nA respectively over the full military temperature range.

Other sources of input-referred errors, such as PSRR and CMRR, are reduced by factors in excess of 120dB for the individual amplifiers. D.C. stability is assured by a long-term drift specification of 0.2 μV/month.

Matching between channels is provided on all critical parameters including offset voltage, tracking of offset voltage vs. temperature, non-inverting bias current, CMRR, and power supply rejection ratio. This unique dual amplifier allows the complete elimination of external components for offset nulling and frequency compensation.

The OP-227 is pin compatible with the OP-10 and OP-207.

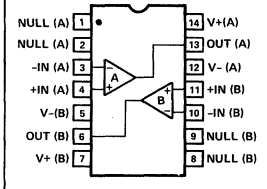
ORDERING INFORMATION†

T_A - 25° C V_{OS} MAX (μV)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
80	OP227AY*	MIL
80	OP227EY	IND
120	OP227BY*	MIL
120	OP227FY	IND
180	OP227CY*	MIL
180	OP227GY	IND

* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

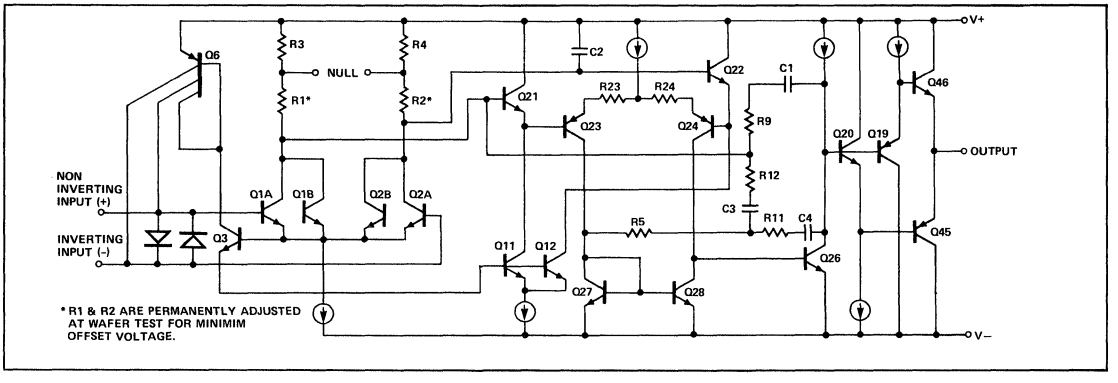
PIN CONNECTIONS



14-PIN CERAMIC DIP (Y-SUFFIX)

NOTE:
Device may be operated even if insertion is reversed; this is due to inherent symmetry of pin locations of amplifiers A and B.

SIMPLIFIED SCHEMATIC (½ OP-227)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Internal Power Dissipation (Note 1) 500mW
Input Voltage (Note 3) ..... ±22V
Output Short Circuit Duration ..... Indefinite
Differential Input Voltage (Note 2) ..... ±0.7V
Differential Input Current (Note 2) ..... ±25mA
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range
OP-227A, OP-227B, OP-227C ..... -55°C to +125°C
OP-227E, OP-227F, OP-227G ..... -25°C to +85°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

Package	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
14-Pin (Y)	106°C	11.3mW/°C

2. The OP-227's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
3. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-227A/E			OP-227B/F			OP-227C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	–	20	80	–	40	120	–	60	180	μV
Long Term V_{OS} Stability	V_{OS}/Time	(Note 2)	–	0.2	1.0	–	0.3	1.5	–	0.4	2.0	μV/Mo
Input Offset Current	I_{OS}		–	7	35	–	9	50	–	12	75	nA
Input Bias Current	I_B		–	±10	±40	–	±12	±55	–	±15	±80	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3, 5)	–	0.08	0.20	–	0.08	0.20	–	0.09	0.28	μVp-p
Input Noise Voltage Density	e_n	f_o = 10Hz (Note 3)	–	3.5	6.0	–	3.5	6.0	–	3.8	9.0	nV/√Hz
		f_o = 30Hz (Note 3)	–	3.1	4.7	–	3.1	4.7	–	3.3	5.9	
		f_o = 1000Hz (Note 3)	–	3.0	3.9	–	3.0	3.9	–	3.2	4.6	
Input Noise Current Density	i_n	f_o = 10Hz (Note 3, 6)	–	1.7	4.5	–	1.7	4.5	–	1.7	–	pA/√Hz
		f_o = 30Hz (Note 3, 6)	–	1.0	2.5	–	1.0	2.5	–	1.0	–	
		f_o = 1000Hz (Note 3, 6)	–	0.4	0.7	–	0.4	0.7	–	0.4	0.7	
Input Resistance — Differential Mode	R_{IN}	(Note 4)	1.5	6	–	1.2	5	–	0.8	4	–	MΩ
Input Resistance — Common Mode	R_{INCM}		–	3	–	–	2.5	–	–	2	–	GΩ
Input Voltage Range	IVR		±11.0	±12.3	–	±11.0	±12.3	–	±11.0	±12.3	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±11V	114	126	–	106	123	–	100	120	–	dB
Power Supply Rejection Ratio	PSSR	V_S = ±4V to ±18V	—	1	10	—	1	10	—	2	20	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	1000	1800	–	1000	1800	–	700	1500	–	V/mV
		$R_L \geq 1k\Omega$, V_O = ±10V	800	1500	–	800	1500	–	–	1500	–	
		$R_L \geq 600\Omega$, V_O = ±1V, V_S = ±4V (Note 4)	250	700	–	250	700	–	200	500	–	
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±13.8	–	±12.0	±13.8	–	±11.5	±13.5	–	V
		$R_L \geq 600\Omega$	±10.0	±11.5	–	±10.0	±11.5	–	±10.0	±11.5	–	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 4)	1.7	2.8	–	1.7	2.8	–	1.7	2.8	–	V/μs
Gain Bandwidth Prod.	GBW	(Note 4)	5.0	8.0	–	5.0	8.0	–	5.0	8.0	–	MHz
Open Loop Output Resistance	R_O	V_O = 0, I_O = 0	–	70	–	–	70	–	–	70	–	Ω
Power Consumption	P_d	Each Amplifier	–	90	140	–	90	140	–	100	170	mW
Offset Adjustment Range		R_P = 10kΩ	–	±4.0	–	–	±4.0	–	–	±4.0	–	mV

NOTES:

1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E Grades Guaranteed Fully Warmed up.
2. Long Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5μV — refer to typical performance curve.
3. Sample tested.
4. Parameter is guaranteed by design.
5. See test circuit and frequency response curve for 0.1Hz to 10Hz tester.
6. See test circuit for current noise measurement.

INDIVIDUAL AMPLIFIER CHARACTERISTICS for $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

			OP-227A			OP-227B			OP-227C			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	(Note 1)	–	60	180	–	80	270	–	110	350	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSN}	(Note 2)	–	0.3	1.0	–	0.4	1.5	–	0.5	1.8	μV/°C
Input Offset Current	I_{OS}		–	15	50	–	22	85	–	30	135	nA
Input Bias Current	I_B		–	±20	±60	–	±28	±95	–	±35	±150	nA
Input Voltage Range	IVR		±10.3	±11.5	–	±10.3	±11.5	–	±10.2	±11.5	–	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	108	122	–	100	119	–	94	116	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	16	—	2	20	—	4	51	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	600	1200	–	500	1000	–	300	800	–	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±11.5	±13.5	–	±11.0	±13.2	–	±10.5	±13.0	–	V

INDIVIDUAL AMPLIFIER CHARACTERISTICS for $V_S = \pm 15V$, $-25°C \leq T_A \leq 85°C$, unless otherwise noted.

			OP-227E			OP-227F			OP-227G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	(Note 1)	–	40	140	–	60	200	–	85	280	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSN}	(Note 2)	–	0.5	1.0	–	0.4	1.5	–	0.5	1.8	μV/°C
Input Offset Current	I_{OS}		–	10	50	–	14	85	–	20	135	nA
Input Bias Current	I_B		–	±14	±60	–	±18	±95	–	±25	±150	nA
Input Voltage Range	IVR		±10.5	±11.8	–	±10.5	±11.8	–	±10.5	±11.8	–	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	110	124	–	102	121	–	96	118	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	15	—	2	16	—	2	32	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	750	1500	–	700	1300	–	450	1000	–	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±11.7	±13.6	–	±11.4	±13.5	–	±11.0	±13.3	–	V

NOTES:

1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. The TCV_{OS} performance is within the specifications unnulled or when nulled with $R_P = 8k\Omega$ to $20k\Omega$, optimum performance is obtained with $R_P = 8k\Omega$.

MATCHING CHARACTERISTICS for $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-227A/E			OP-227B/F			OP-227C/G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage Match	ΔV_{OS}		–	25	80	–	35	150	–	55	300	μV
Average Non-Inverting Bias Current	I_B^+	$I_B^+ = \frac{I_{B^+A} + I_{B^+B}}{2}$	–	±10	±40	–	±12	±55	–	±15	±90	nA
Non-Inverting Offset Current	I_{OS}^+	$I_{OS}+ = I_{B^+A} - I_{B^+B}$	–	±12	±60	–	±15	±80	–	±20	±130	nA
Inverting Offset Current	I_{OS}^-	$I_{OS}^- = I_{B^-A} - I_{B^-B}$	–	±12	±60	–	±15	±80	–	±20	±130	nA
Common Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 11V$	110	123	–	103	120	–	97	117	–	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 4$ V to ±18V	—	2	10	—	2	10	—	2	20	μV/V
Channel Separation	CS	(Note 1)	126	154	–	126	154	–	126	154	–	dB
Gain Match	ΔA_{VO}	$f_o = 100$ KHz (Note 1) $R_L \geq 2k\Omega$, $V_O = \pm 10V$	–	1.5	6.0	–	1.5	6.0	–	2.0	9.0	%

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = -55°C$ to $+125°C$, unless otherwise noted.

			OP-227A			OP-227B			OP-227C			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage Match	ΔV_{OS}		–	55	180	–	75	300	–	100	480	μV
Input Offset Voltage Tracking	$TC\Delta V_{OS}$	Nulled or Unnulled (Note 2)	–	0.3	1.0	–	0.4	1.5	–	0.5	1.8	μV/°C
Average Non-Inverting Bias Current	I_B^+	$I_B^+ = \frac{I_{B^+A} + I_{B^+B}}{2}$	–	±20	±60	–	±28	±95	–	±35	±170	nA
Average Drift of Non-Inverting Bias Current	TCI_B^+		–	100	–	–	160	–	–	200	–	pA/°C
Non-Inverting Offset Current	I_{OS}^+	$I_{OS}+ = I_{B^+A} - I_{B^+B}$	–	±25	±90	–	±35	±140	–	±45	±250	nA
Average Drift of Non-Inverting Offset Current	TCI_{OS}^+		–	130	–	–	200	–	–	250	–	pA/°C
Inverting Offset Current	I_{OS}^-	$I_{OS}^- = I_{B^-A} - I_{B^-B}$	–	±25	±90	–	±35	±140	–	±45	±250	nA
Common Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 10V$	105	118	–	97	114	–	90	110	–	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 4.5$V to ±18V	—	2	16	—	3	20	—	4	51	μV/V

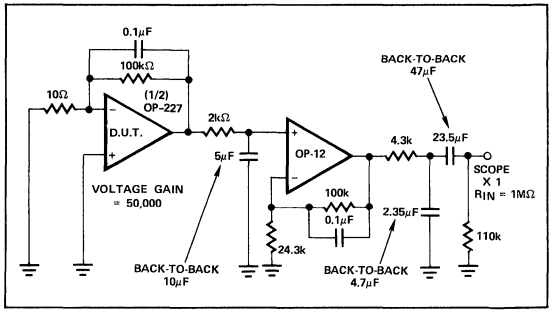
MATCHING CHARACTERISTICS for $V_S = \pm 15V$, $T_A = -25°C$ to $+85°C$, unless otherwise noted.

			OP-227E			OP-227F			OP-227G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage Match	ΔV_{OS}		–	40	140	–	65	210	–	90	400	μV
Input Offset Voltage Tracking	$TC\Delta V_{OS}$	Nulled or Unnulled (Note 1)	–	0.3	1.0	–	0.4	1.5	–	0.5	1.8	μV/°C
Average Non-Inverting Bias Current	I_B^+	$I_B^+ = \frac{I_{B^+A} + I_{B^+B}}{2}$	–	±14	±60	–	±18	±95	–	±25	±170	nA
Average Drift of Non-Inverting Bias Current	TCI_B^+		–	80	–	–	140	–	–	180	–	pA/°C
Non-Inverting Offset Current	I_{OS}^+	$I_{OS}+ = I_{B^+A} - I_{B^+B}$	–	±20	±90	–	±25	±140	–	±35	±250	nA
Average Drift of Non-Inverting Offset Current	TCI_{OS}^+		–	130	–	–	200	–	–	250	–	pA/°C
Inverting Offset Current	I_{OS}^-	$I_{OS}^- = I_{B^-A} - I_{B^-B}$	–	±20	±90	–	±25	±140	–	±35	±250	nA
Common Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 10V$	106	120	–	98	117	–	90	112	–	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 4.5$V to ±18V	—	2	15	—	2	16	—	3	32	μV/V

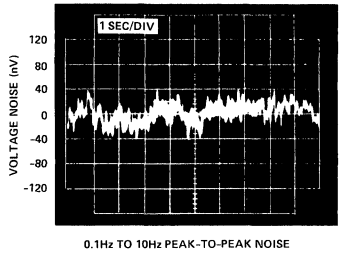
NOTES:
1. Sample tested.
2. Guaranteed by design.

TYPICAL PERFORMANCE CURVES

0.1 HZ TO 10 HZ P-P NOISE CIRCUIT SCHEMATIC



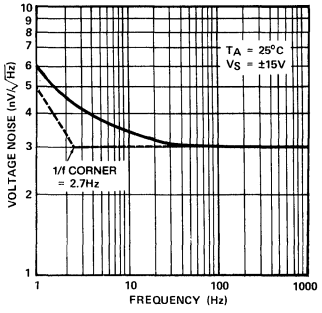
0.1 Hz TO 10 Hz NOISE TEST CIRCUIT



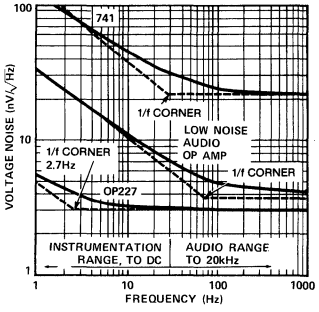
0.1Hz TO 10Hz PEAK-TO-PEAK NOISE

NOTE: OBSERVATION TIME MUST BE LIMITED TO 10 SECONDS TO INSURE 0.1Hz CUTOFF.

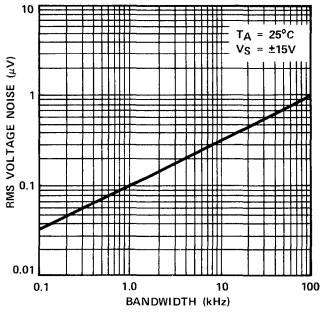
VOLTAGE NOISE vs FREQUENCY



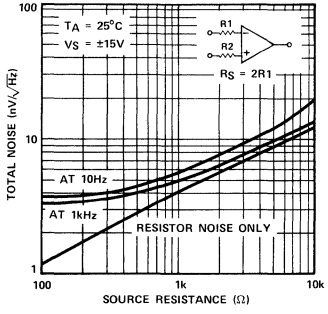
COMPARISON OF OP-AMP VOLTAGE NOISE SPECTRUMS



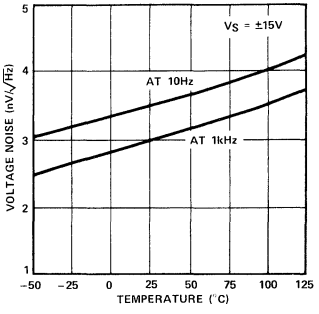
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



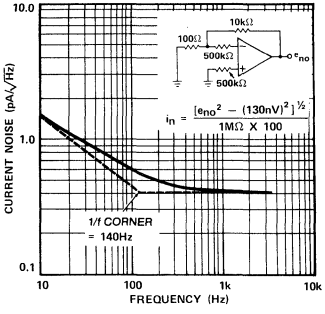
TOTAL NOISE vs SOURCE RESISTANCE



VOLTAGE NOISE vs TEMPERATURE

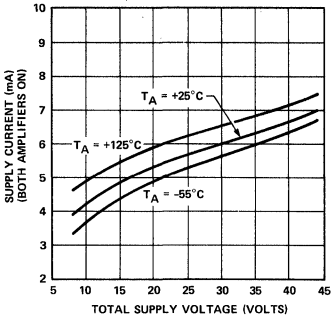


CURRENT NOISE vs FREQUENCY

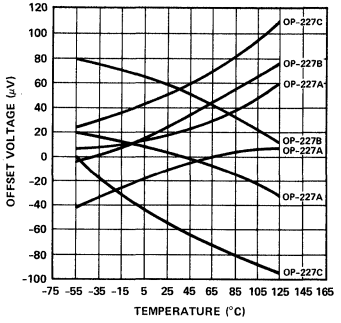


TYPICAL PERFORMANCE CURVES

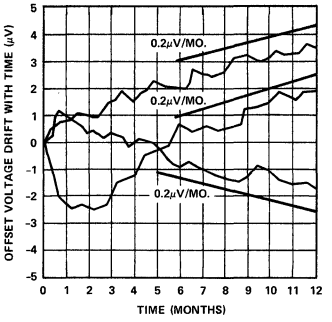
SUPPLY CURRENT vs SUPPLY VOLTAGE



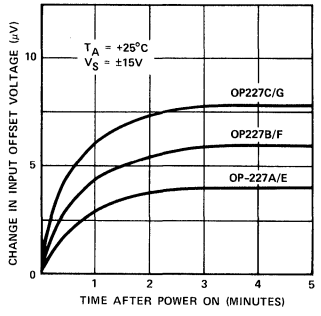
OFFSET VOLTAGE DRIFT OF REPRESENTATIVE UNITS



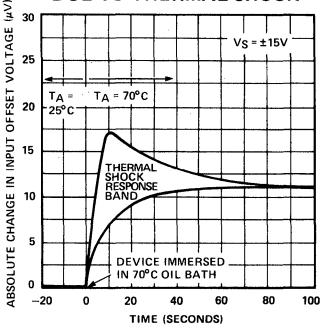
OFFSET VOLTAGE STABILITY WITH TIME



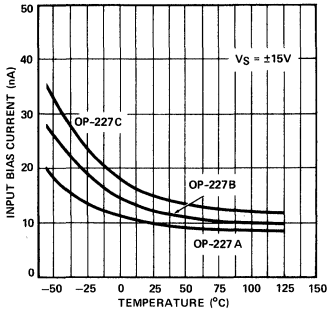
WARM-UP DRIFT



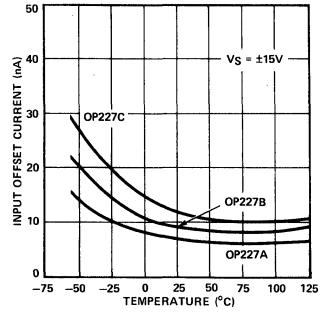
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



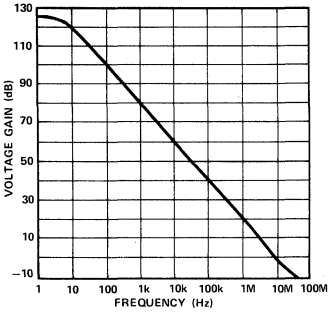
INPUT BIAS CURRENT vs TEMPERATURE



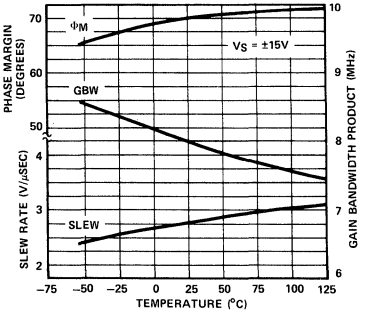
INPUT OFFSET CURRENT vs TEMPERATURE



VOLTAGE GAIN vs FREQUENCY

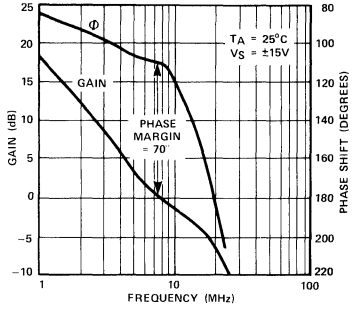


SLEW RATE, GAIN- BANDWIDTH PRODUCT, PHASE MARGIN vs TEMP.

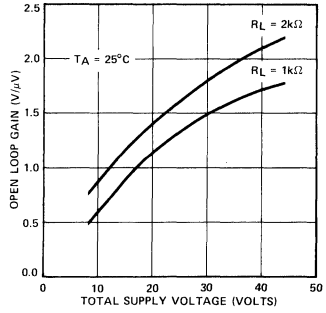


TYPICAL PERFORMANCE CURVES

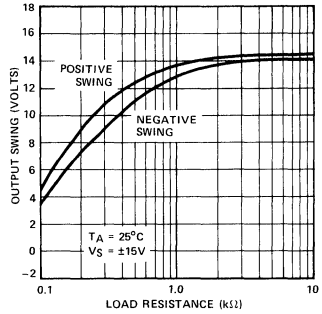
GAIN, PHASE SHIFT vs FREQUENCY



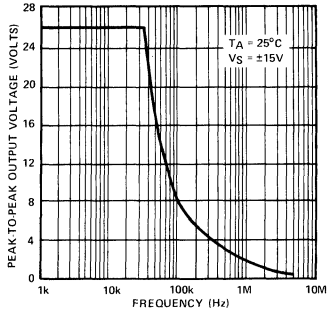
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



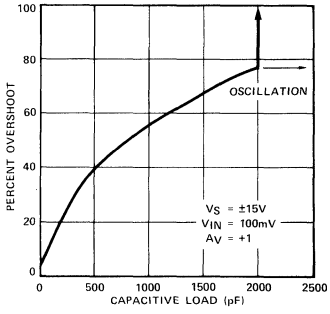
OUTPUT SWING vs RESISTIVE LOAD



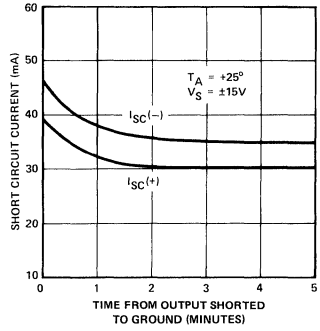
MAXIMUM UNDISTORTED OUTPUT vs FREQUENCY



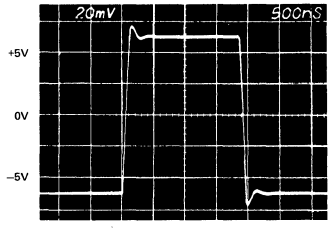
SMALL SIGNAL OVERSHOOT vs CAPACITIVE LOAD



SHORT CIRCUIT CURRENT vs TIME

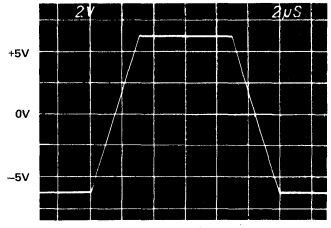


SMALL SIGNAL TRANSIENT RESPONSE



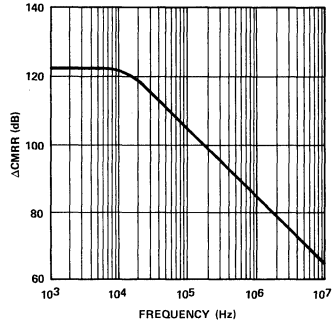
A_{VCL} = +1, C_L = 15pF
V_S = ±15V
T_A = 25°C

LARGE SIGNAL TRANSIENT RESPONSE



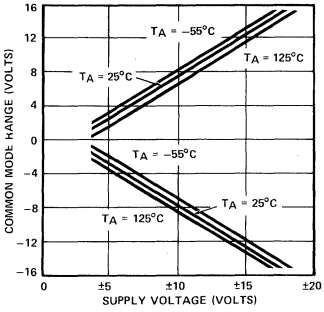
A_{VCL} = +1
V_S = ±15V
T_A = 25°C

MATCHING CHARACTERISTIC CMRR MATCH vs FREQUENCY

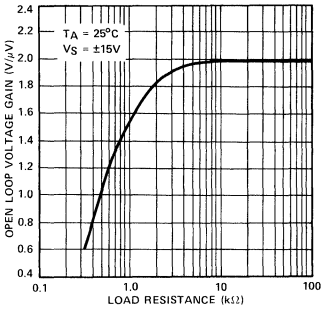


TYPICAL PERFORMANCE CURVES

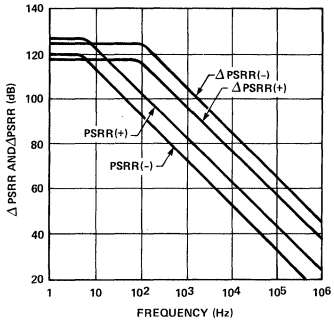
COMMON-MODE INPUT RANGE vs SUPPLY VOLTAGE



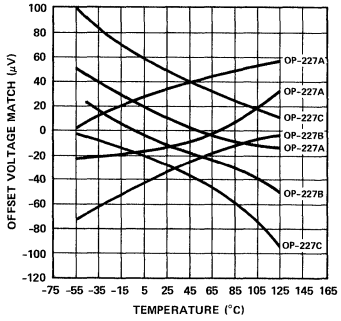
OPEN-LOOP VOLTAGE GAIN vs LOAD RESISTANCE



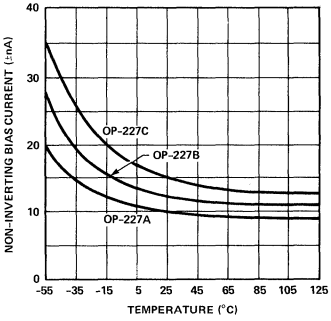
PSRR AND ΔPSRR vs FREQUENCY



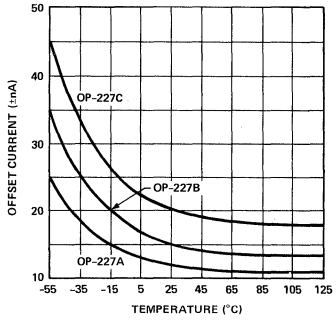
MATCHING CHARACTERISTIC; DRIFT OF OFFSET VOLTAGE MATCH OF REPRESENTITIVE UNITS



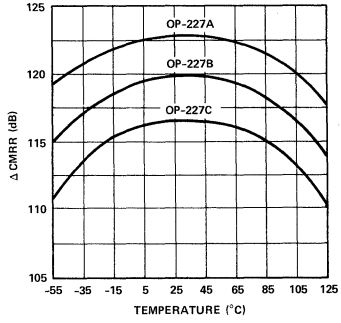
MATCHING CHARACTERISTIC; AVERAGE NON-INVERTING BIAS CURRENT vs TEMPERATURE



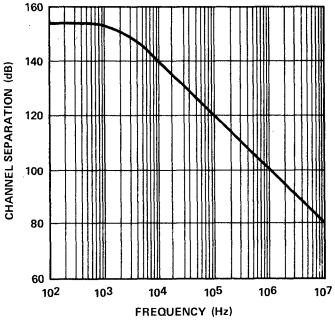
MATCHING CHARACTERISTIC; AVERAGE OFFSET CURRENT vs TEMPERATURE (INVERTING OR NON-INVERTING)



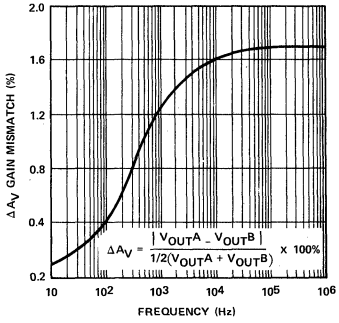
MATCHING CHARACTERISTIC; CMRR MATCH vs TEMPERATURE



CHANNEL SEPARATION vs FREQUENCY

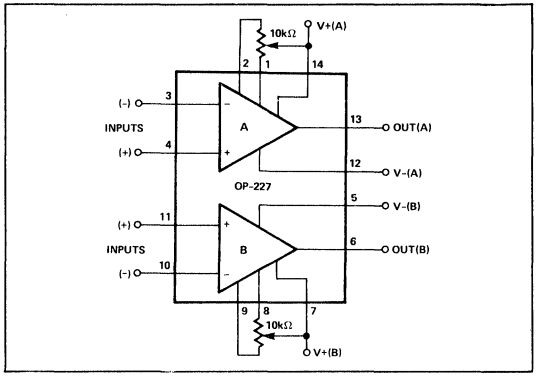


GAIN MISMATCH vs FREQUENCY



BASIC CONNECTIONS

OFFSET NULLING CIRCUIT



APPLICATION INFORMATION

COMMENTS ON NOISE MEASUREMENTS

The extremely low noise of the OP-227 (27, 37, 237) implies that its precise measurement is a difficult task. In order to realize the 80nV peak-to-peak noise specification of the op amp in the 0.1 Hz to 10 Hz frequency range, the following constraints have to be observed:

(1) The device has to be warmed up for at least five minutes. As shown in the warm-up drift curve, as the op amp warms up, its offset voltage changes typically 4μV due to its chip temperature increasing 14 to 20°C from the moment the power supplies are turned on. In the 10 sec measurement interval these temperature-induced effects can easily exceed tens of nanovolts.

(2) For similar reasons, the device has to be well shielded from air currents to eliminate the possibility of thermoelectric effects in excess of a few nanovolts invalidating the measurements.

(3) Sudden motion in the vicinity of the device can also "feedthrough" to increase the observed noise.

(4) The test time to measure 0.1 Hz to 10 Hz noise should not exceed 10 sec. As shown in the noise tester frequency response curve the 0.1 Hz corner is defined by only one zero. The test time of 10 sec acts an additional zero to eliminate noise contributions from the frequency band below 0.1 Hz.

A noise-voltage density test is recommended when measuring noise on a large number of units. A 10 Hz noise-voltage density measurement will correlate well with a 0.1 Hz-to-10 Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

OPTIMIZING LINEARITY

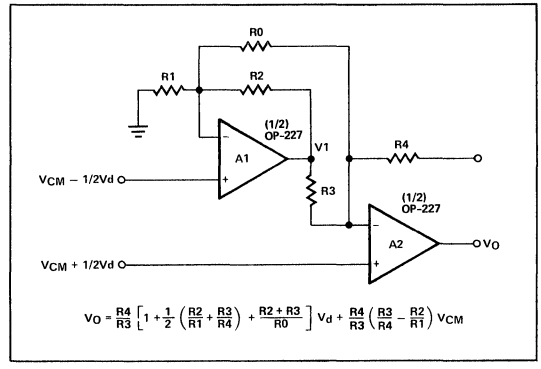
Best linearity can be obtained by designing for the minimum output current required for the application. High gain and excellent linearity can be achieved by operating the op amp within an output current range of ±10mA.

INSTRUMENTATION AMPLIFIER APPLICATIONS OF THE OP-227 AND OP-237

The excellent input characteristics of the OP-227/237 make them ideal for use in *instrumentation amplifier* configurations where low-level differential signals are to be amplified. The low-noise, low input offsets, low drift, and high gain combined with excellent CMRR provides the characteristics needed for high-performance instrumentation amplifiers. In addition, CMRR vs. frequency is very good due to the wide gain bandwidth of these op amps.

The circuit of Fig. 1 is recommended for applications where the common-mode input range is relatively low and differential gain will be in the range of 10 to 1000. This two-op-amp instrumentation amplifier features *independent* adjustment of common-mode rejection and differential gain. Input impedance is very high since both inputs are applied to noninverting op amp inputs.

FIG. 1. TWO-OP-AMP INSTRUMENTATION AMPLIFIER CONFIGURATION



The output voltage V_o, assuming ideal op amps, is given in Fig. 1. The input voltages are represented as a common-mode input V_{cm} plus a differential input V_d. The ratio R_3/R_4 is made equal to the ratio R_2/R_1 to reject the common-mode input V_{cm}. The differential signal V_d is then amplified according to:

$$V_o = \frac{R_4}{R_3}\left(1+\frac{R_3}{R_4}+\frac{R_2+R_3}{R_o}\right)V_d, \text{ where } \frac{R_3}{R_4}=\frac{R_2}{R_1}$$

Note that gain can be independently varied by adjusting R_o. From considerations of dynamic range, resistor tempco matching, and matching of amplifier response, it is generally best to make R_1, R_2, R_3, and R_4 approximately equal. Designating R_1, R_2, R_3, and R_4 as R_N allows the output equation to be further simplified:

$$V_o = 2\left(1+\frac{R_N}{R_o}\right)V_d, \text{ where } R_N = R_1 = R_2 = R_3 = R_4$$

Dynamic range is limited by A1 as well as A2; the output of A1 is:

$$V_1 = -\left(1+\frac{R_N}{R_o}\right)V_d + 2\,V_{cm}$$

If the instrumentation amplifier were designed for a gain of 10 and maximum V_d of ±1V, then R_N/R_o would need to be four and V_o would be a maximum of ±10V. Amplifier A1 would have a maximum output of ±5V plus $2V_{cm}$, thus a limit of ±10V on the output of A1 would imply a limit of ±2.5V on V_{cm}. A nominal value of 10KΩ for R_N is suitable for most applications. A range of 20Ω to 2.5KΩ for R_o will then provide a gain range of 10 to 1000. The current through R_o is V_d/R_o, so the amplifiers must supply ±10mV/20Ω (or ±0.5mA) when the gain is at the maximum value of 1000 and V_d is at ±10mV.

Rejecting common-mode inputs is most important in accurately amplifying low-level differential signals. Two factors determine the CMR in this instrumentation amplifier configuration (assuming infinite gain):

(1) CMRR of the op amps
(2) Matching of the resistor network ($R_4/R_3 = R_2/R_1$)

In this instrumentation amplifier configuration, error due to CMRR effect is directly proportional to the *differential* CMRR of the op amps. For the OP-227 and OP-237, this ΔCMRR is a minimum of 97dB for the "G" and 110 dB for the "E" grade. A ΔCMRR value of 100 dB and common-mode input range of ±2.5V indicates a peak input-referred error of only ±25μV. Resistor matching is the other factor affecting CMRR. Defining A_d as the differential gain of the instrumentation amplifier and assuming that R_1, R_2, R_3 and R_4 are approximately equal (R_N will be the nominal value), then CMRR for this instrumentation amplifier configuration will be approximately A_d divided by $4\Delta R/R_N$. CMRR at differential gain of 100 would be 88dB with resistor matching of 0.1%. Trimming R_1 to make the ratio R_3/R_4 equal to R_2/R_1 will directly raise the CMRR until limited by linearity and resistor stability considerations.

The high open-loop gain of the OP-227 and OP-237 is very important to achieving high accuracy in the two op-amp instrumentation amplifier configuration. Gain error can be approximated by

$$\text{Gain Error} \sim \frac{1}{1+\frac{A_d}{A_{02}}}, \qquad \frac{A_d}{2\,A_{01}\,A_{02}} \ll 1$$

where A_d is the instrumentation amplifier differential gain and A_{02} is the open-loop gain of op amp A2. this analysis assumes equal values of R_1, R_2, R_3, and R_4. For example, consider an OP-227 with A_{02} of 700V/mV. If the differential gain A_d were set to 700, then the gain error would be 1/1.001 which is approximately 0.1%.

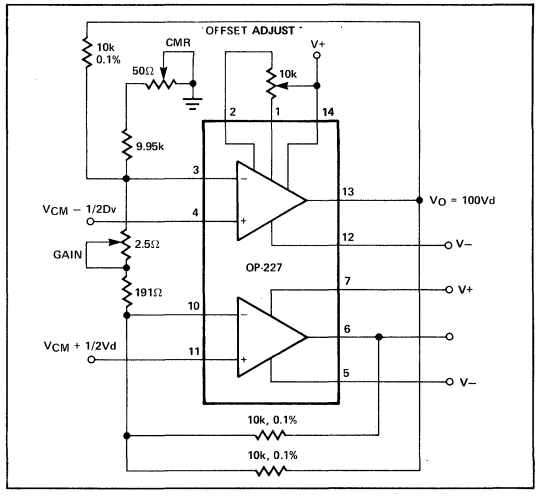
Another effect of finite op amp gain is undesired feedthrough of common-mode input. Defining A_{01} as the open-loop gain of op amp A1, then the common-mode error (CME) at the output due to this effect will be approximately

$$\text{CME} \sim \frac{2\,A_d}{1+\frac{A_d}{A_{01}}}\,\frac{1}{A_{01}}\,V_{cm}$$

For $A_d/A_{01} \ll 1$, this simplifies to $(2\,A_d/A_{01}) \times V_{cm}$. If the op amp gain is 700 V/mV, V_{cm} is 2.5V, and A_d is set to 700, then the error at the output due to this effect will be approximately 5mV.

A complete instrumentation amplifier designed for a gain of 100 is shown in Figure 2. It has provision for trimming of input offset voltage, CMR, and gain. Performance is excellent due to the high gain, high CMRR, and low noise of the individual amplifiers combined with the tight matching characteristics of the OP-227 dual.

FIG. 2. TWO-OP-AMP INSTRUMENTATION AMPLIFIER USING OP-227 DUAL



A three-op-amp instrumentation amplifier configuration using the OP-227 and OP-27 is recommended for applications requiring high accuracy over a wide gain range. This circuit provides excellent CMR over a wide frequency range. As with the two-op-amp instrumentation amplifier circuits, the tight matching of the two op-amps within the OP-227 package provides a real boost in performance. Also, the low-noise, low offset, and high gain of the individual op-amps serves to minimize errors.

A simplified schematic is shown in Figure 3. The input stage (A1 and A2) serves to amplify the differential input V_d without amplifying the common-mode voltage V_{CM}. The output stage then rejects the common-mode input. With ideal op-amps and no resistor matching errors, then the outputs of each amplifier will be:

$$V_1 = -\left(1+\frac{2R_1}{R_o}\right)\frac{V_d}{2} + V_{cm}$$

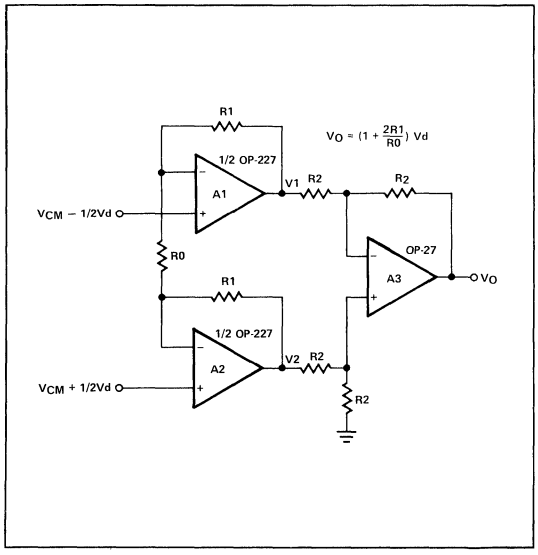
$$V_2 = \left(1+\frac{2R_1}{R_o}\right)\frac{V_d}{2} + V_{cm}$$

$$V_o = V_2 - V_1 = \left(1+\frac{2R_1}{R_o}\right)V_d$$

$$V_o = A_d\,V_d$$

The differential gain A_d is $1+2R_1/R_o$ and the common-mode input V_{cm} is rejected.

FIG. 3. THREE-OP AMP INSTRUMENTATION AMPLIFIER USING OP-227 AND OP-27



While output error due to input offsets and noise are easily determined the effects of finite gain and common-mode rejection are more subtle. CMR of the complete instrumentation amplifier is directly proportioned to the *match* in CMR of the input op-amps. This match varies from 97dB to 110dB minimum for the OP-227. Using 100dB, then the ouput response to a common-mode input V_{CM} would be:

$$[V_0]_{cm} = A_d\, V_{cm} \times 10^{-5}$$

CMRR of the instrumentation amplifier, which is defined as $20 \log_{10} A_d/A_{cm}$, is simply equal to the ΔCMRR of the OP-227 While this ΔCMRR is already high, overall CMRR of the complete amplifier can be raised even further by trimming of the output stage resistor network.

Finite gain of the input op-amps causes a scale factor error and a small degradation in CMR. Designating the open-loop gain of op-amp A_1 as A_{01} and op-amp A_2 as A_{02}, then the following equation is an excellent approximation.

$$V_o \sim \frac{1}{1 + \frac{R_1}{R_o}\left(\frac{1}{A_{01}} + \frac{1}{A_{02}}\right)} \left[A_d\, V_d + \frac{2R_1}{R_o}\left(\frac{1}{A_{01}} - \frac{1}{A_{02}}\right) V_{cm}\right]$$

This can be further simplified by defining A_o as the nominal open-loop gain and ΔA_o as the differential open-loop gain. Then

$$V_o \sim \frac{1}{1 + \frac{2R_1}{R_o}\frac{1}{A_o}} \left[A_d\, V_d + \frac{2R_1}{R_o}\frac{\Delta A_o}{A_o{}^2}\, V_{cm}\right]$$

The high open-loop gain of the individual amplifiers within the OP-227 (7000,000 minimum at 25° C into $R_L \geq 2K$) assures good gain accuracy even at high values of A_d. The effect of finite open-loop gain on CMRR can be approximated by:

$$CMRR \sim \frac{A_o{}^2}{\Delta A_o}$$

If $\Delta A_o/A_o$ were 6% and A_o were 600,000, then the CMRR due to finite gain of the input op-amps would be approximately 140dB.

The unity-gain output stage using an OP-27 contributes negligible error to the overall amplifier configuration, but matching of the four-resistor R_2-network is critical to achieving high CMR. Consider a worst-case situation where each R_2 resistor has an error of $\pm\Delta R_2$. If the resistor ratio is high on one side and low on the other, then the common-mode gain will be $2\Delta R_2/R_2$. Since the output stage gain is unity, CMRR will then be $R_2/2\Delta R_2$. It is common practice to trim the R_2 resistor connected to ground to maximize overall CMRR for the total instrumentation amplifier circuit.

This three-op-amp instrumentation amplifier configuration using the OP-227 dual at the input and the OP-27 single at the output can provide excellent performance over a wide gain range. A range of 1 to 2000 is practical and CMR of over 120 dB is readily achievable.

OP-420

QUAD MICROPOWER OPERATIONAL AMPLIFIER

FEATURES

- **Low Supply Current ..... 220μA Typical @ V_S = ±15V**
- **Single Supply Operation ..... +5V to +30V**
- **Dual Supply Operation ..... ±1.5V to ±15V**
- **Low Input Offset Voltage ..... 500μV Typical**
- **Low Input Offset Voltage Drift ..... 5μV/°C Typical**
- **High Common Mode Input Range ..... V− to (V+ − 1.5V)**
- **High CMRR ..... 100dB Typical**
- **High Open Loop Gain ..... 1100V/mV Typical**
- **±30V Input Overvoltage Protection**
- **No External Components Required ..... Easy to Use**
- **Single Chip Monolithic Construction**
- **LM 148 Pinout**

GENERAL DESCRIPTION

The OP-420 Quad Micropower Operational Amplifier is a single-chip quad op amp patterned after the OP-20 Precision Micropower Single Operational Amplifier. The Darlington PNP input stage allows the input common mode voltage to include V−. Combined with a low power supply drain (~40μA/section at 5V), the OP-420 offers a unique solution for designs requiring high function density and portable operation. Examples of applications ideally suited to use of the OP-420 would include two-wire transmitter for process control loops, battery-operated remote line filters, signal preconditioning amplifiers, and a variety of multiple gain block arrays.

As with all PMI products, the OP-420 is fabricated using a triple passivation process which results in maximum long term reliability and stability at the lowest overall system cost.

For single and dual micropower operational amplifier requirements that allow convenient offset nulling see the OP-20 and OP-220 data sheets.

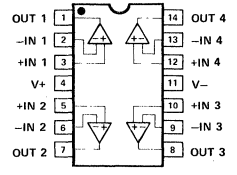
ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (mV)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
2.5	OP420BY*	MIL
2.5	OP420FY	IND
4.0	OP420CY*	MIL
4.0	OP420GY	IND
6.0	OP420HY	COM

* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

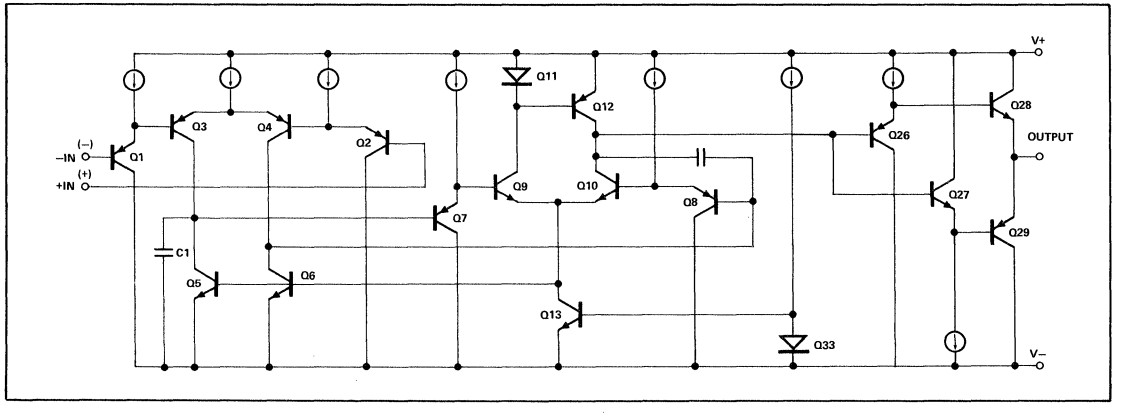
† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



14-PIN HERMETIC DIP (Y SUFFIX)

SIMPLIFIED SCHEMATIC (1/4 Shown)



ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±18V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply voltage
Output Short Circuit Duration ..... Continuous
(One Amplifier Only)
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C

Operating Temperature Range
OP-420BY, OP-420CY ..... −55°C to +125°C
OP-420FY, OP-420GY ..... −25°C to +85°C
OP-420HY ..... 0°C to +70°C
DICE Junction Temperature ..... −65°C to +150°C

NOTES:
1. See table for maximum ambient temperature rating and derating factor.

	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	100°C	10mW/°C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-420B OP-420F			OP-420C OP-420G			OP-420H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	0.5	2.5	—	1	4	—	2	6	mV
Input Offset Current	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	0.5	1.5	—	0.8	2.5	—	1.2	6	nA
Input Bias Current	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	—	9	20	—	12	30	—	18	40	nA
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	80	—	—	80	—	—	80	—	$nV/\sqrt{Hz}$
		$f_O = 100Hz$	—	60	—	—	60	—	—	60	—	
Input Noise Current Density	i_n	$f_O = 10Hz$	—	1	—	—	1	—	—	1	—	$pA/\sqrt{Hz}$
		$f_O = 100Hz$	—	0.8	—	—	0.8	—	—	0.8	—	
Input Voltage Range	IVR	V+ = +5V, V− = 0V	0	—	3.8	0	—	3.8	0	—	3.6	V
		$V_S = \pm 15V$	+13.8/-15.0	—	—	+13.8/15.0	—	—	+13.8/15.0	—	—	
Common Mode Rejection Ratio (V_{CM} = CMVR)	CMRR	$V_S = \pm 2.5V$ to $\pm 15V$ and V− = 0V, V+ = 5 to 30V	83	100	—	80	96	—	76	90	—	dB
			96	100	—	80	96	—	76	90	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ V− = 0V, V+ = 5V to 30V	—	10	30	—	20	50	—	30	80	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$	600	1100	—	400	900	—	200	800	—	V/mV
Slew Rate	SR		—	.05	—	—	.05	—	—	.05	—	V/μs
Closed Loop Bandwidth	BW	$A_{VCL} = +1.0$ $R_L = 10k\Omega$	—	150	—	—	150	—	—	150	—	kHz
Output Voltage Swing	V_O	V+ = 5V, V− = 0V, $R_L = 10k\Omega$	0.7	—	4.1	0.8	—	4.0	0.9	—	3.8	V
		$V_S = \pm 15V$, $R_L = 25k\Omega$	± 14.0	—	—	± 14.0	—	—	±13.8	—	—	
Supply Current (All 4 Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, no load	—	140	200	—	170	300	—	200	400	μA
		$V_S = \pm 15V$, no load	—	220	300	—	240	450	—	260	600	

NOTE:
1. Sample tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ for OP-420B and OP-420C, $-25°C \leq T_A \leq +85°C$ for OP-420F and OP-420G, and $0°C \leq T_A \leq +70°C$ for OP-420H, unless otherwise noted.

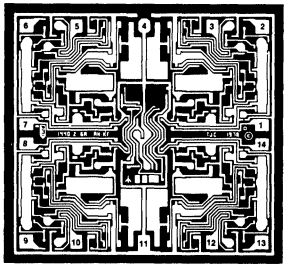
			OP-420B OP-420F			OP-420C OP-420G			OP-420H			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnulled	—	5	10	—	8	15	—	15	25	µV/°C
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	—	3.5	—	—	5.5	—	—	7.5	mV
Input Offset Current	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	—	3	—	—	4	—	—	8	nA
Input Bias Current	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	—	—	30	—	—	40	—	—	60	nA
Input Voltage Range	IVR	V+ = +5V, V− = 0V	0	—	3.5	0	—	3.5	0	—	3.5	
		$V_S = \pm 15V$	+13.5/−15.0	—		+13.5/−15.0	—		+13.5/−15.0	—		V
Common Mode Rejection Ratio (V_{CM} = CMVR)	CMRR	V+ = +5V, V− = 0V 0V ≤ VCM ≤ 3V	76	96	—	73	92	—	73	86	—	
		$V_S = \pm 15V$ −15V ≤ VCM ≤ 13V	80	96	—	76	92	—	73	86	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ and V− = 0V, V+ = 5V to 30V	—	15	50	—	25	80	—	40	100	µV/V
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 50k\Omega$	300	800	—	200	650	—	100	400	—	V/mV
Output Voltage Swing	V_O	V+ = 5V, V− = 0V, $R_L = 20k\Omega$	0.9	—	3.9	1.0	—	3.8	1.1	—	3.6	
		$V_S = \pm 15V$, $R_L = 50k\Omega$	±13.8	—	—	±13.8	—	—	±13.6	—	—	V
Supply Current (All 4 Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, no load	—	170	300	—	210	400	—	250	500	µA
		$V_S = \pm 15V$, no load	—	260	400	—	290	550	—	320	700	

NOTE:

1. Sample tested.

For typical performance curves, see OP-220 data sheet. Note that supply current will be approximately twice as much as shown in graph.

DICE CHARACTERISTICS



1. OUTPUT 1
2. INVERTING INPUT 1
3. NON-INVERTING INPUT 1
4. V+
5. NON-INVERTING INPUT 2
6. INVERTING INPUT 2
7. OUTPUT 2
8. OUTPUT 3
9. INVERTING INPUT 3
10. NON-INVERTING INPUT 3
11. V–
12. NON-INVERTING INPUT 4
13. INVERTING INPUT 4
14. OUTPUT 4

DIE SIZE 0.086 × 0.092 inch

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

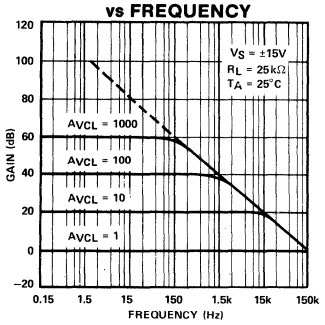
PARAMETER	SYMBOL	CONDITIONS	OP-420N LIMIT	OP-420G LIMIT	OP-420GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5$ to $\pm 15V$	2.5	4	6	mV MAX
Input Offset Current	I_{OS}	$V_S = \pm 2.5$ to $\pm 15V$	1.5	2.5	6	nA MAX
Input Bias Current	I_B	$V_S = \pm 2.5$ to $\pm 15V$	20	30	40	nA MAX
Input Voltage Range	IVR		+13.8/–15.0	+13.8/–15.0	+13.8/–15.0	V MIN
Common Mode Rejection Ratio	CMRR	V+ = +5V, V– = 0V $0V \le V_{CM} \le 3.5V$ $V_S = \pm 15V$, $-15V \le V_{CM} \le 13.5V$	83 86	80 80	76 76	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5$ to $\pm 15V$ V– = 0V, V+ = +5V to +30V	30	50	80	μV/V MAX
Large Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$	600	400	200	V/mV MIN
Output Voltage Swing	V_O	V+ = +5V, V– = 0V $R_L = 10k\Omega$ $V_S = \pm 15V$ $R_L = 25k\Omega$	4.1 ± 14.0	4.0 ± 14.0	3.8 ±13.8	V MIN V MIN
Supply Current	I_{SY}	No Load, (All 4 amplifiers)	300	450	600	μA MAX

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

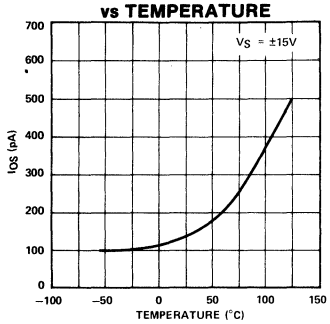
PARAMETER	SYMBOL	CONDITIONS	OP-420N TYP	OP-420G TYP	OP-420GR TYP	UNITS
Input Noise Voltage Density	e_n	$f_o = 10Hz$ $f_o = 100Hz$	80 60	80 60	80 60	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	$f_o = 10Hz$ $f_o = 100Hz$	1 0.8	1 0.8	1 0.8	$pA/\sqrt{Hz}$
Closed Loop Bandwidth	BW	$A_{VCL} = +1.0$ $R_L = 10k\Omega$	150	150	150	kHz

TYPICAL PERFORMANCE CURVES

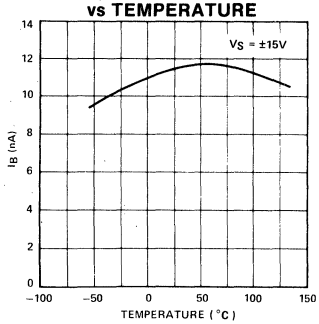
CLOSED LOOP GAIN vs FREQUENCY



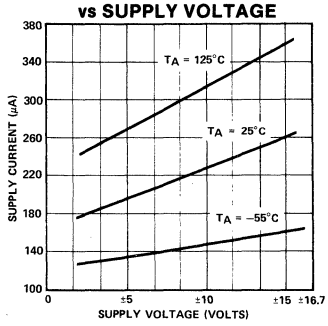
INPUT OFFSET CURRENT vs TEMPERATURE



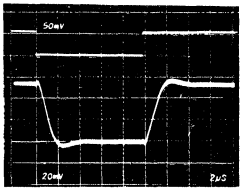
INPUT BIAS CURRENT vs TEMPERATURE

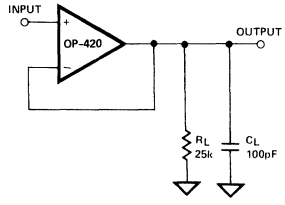


SUPPLY CURRENT vs SUPPLY VOLTAGE

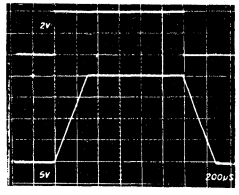


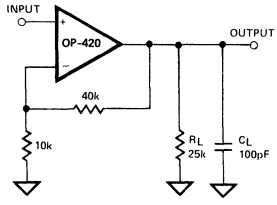
SMALL-SIGNAL TRANSIENT RESPONSE





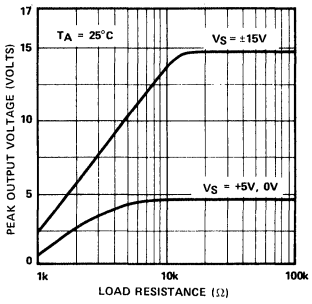
LARGE-SIGNAL TRANSIENT RESPONSE



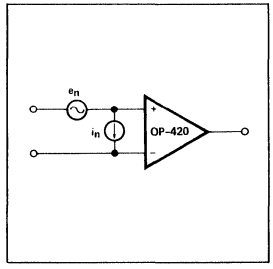


TYPICAL PERFORMANCE CURVES

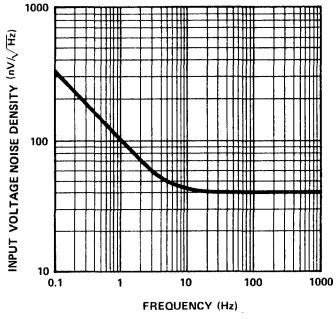
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



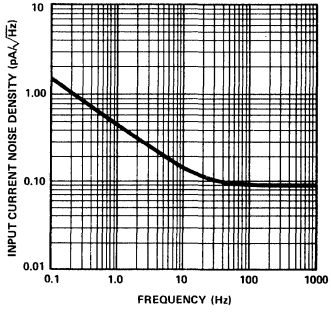
NOISE CIRCUIT MODEL



INPUT VOLTAGE NOISE DENSITY (e_n) vs FREQUENCY



INPUT CURRENT NOISE DENSITY (i_n) vs FREQUENCY



OP-421

HIGH SPEED QUAD LOW POWER OPERATIONAL AMPLIFIER

FEATURES

- **Wide Bandwidth** **1MHz**
- **Low Supply Current** **600μA**
- **Slew Rate** **0.5V/μs**
- **Single Supply Operation** ..... **+3V to +30V**
- **Low Input Offset Voltage** **500μV**
- **Low Input Offset Voltage Drift** ..... **5μV/°C**
- **High Common Mode Input Range** .... **V− to V+ (−1.5V)**
- **High CMRR** **100dB**
- **High Open Loop Gain** **400V/mV**
- **±30V Input Overvoltage Protection**
- **No External Components Required** ..... **Easy to Use**
- **Single Chip Monolithic Construction**
- **Pin Compatible With LM124, LM148 and OP-11**

ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (mV)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
2.5	OP421BY*	MIL
2.5	OP421FY	IND
4	OP421CY*	MIL
4	OP421GY	IND
6	OP421HY	COM

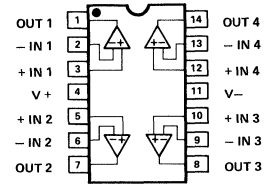
*Also available with MIL-STD-883B processing. To order add /883 as a suffix to the part number.

†All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

GENERAL DESCRIPTION

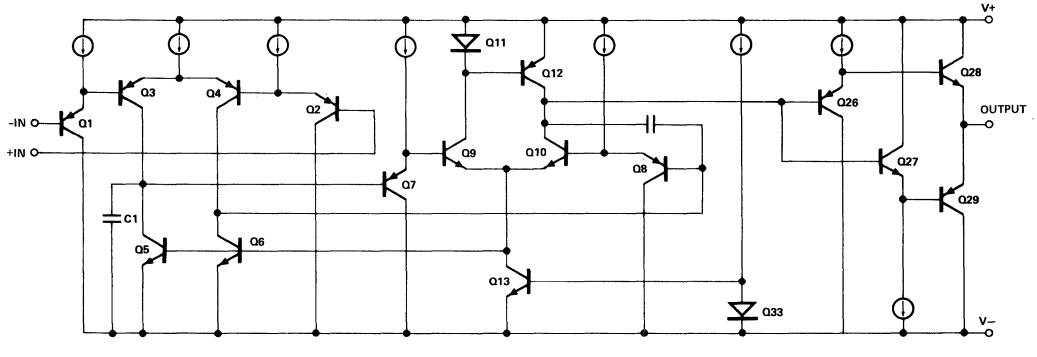
The OP-421 Quad Low-Power Operational Amplifier is a single-chip quad op amp patterned after the OP-21 High-Speed Precision Low-Power single Operational Amplifier. The PNP input stage allows the input common mode voltage to include V-. Combined with a low-power supply current (150μA/section at 5V), the OP-421 offers a unique solution for designs requiring high function density, wide bandwidth and low-power operation. Examples of applications ideally suited to use of the OP-421 would include low-power active filters, battery-operated remote line filters, signal preconditioning amplifiers, and a variety of multiple gain block arrays. In addition, the ever present problem of crossover distortion in low-power devices is eliminated by a unique double buffered output section.

PIN CONNECTIONS



14-PIN HERMETIC DIP (Y-SUFFIX)

SIMPLIFIED SCHEMATIC (1/4 Shown)



ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±18V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply voltage
Output Short Circuit Duration ..... Continuous
(One Amplifier Only)
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Operating Temperature Range
OP-421BY, OP-421CY ..... −55°C to +125°C
OP-421FY, OP-421GY ..... −25°C to +85°C
OP-421HY ..... 0°C to +70°C

DICE Junction Temperature ..... −65°C to +150°C

NOTES:
1. See table for maximum ambient temperature rating and derating factor.

	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	100°C	10mW/°C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A + 25°C$, unless otherwise noted.

			OP-421B OP-421F			OP-421C OP-421G			OP-421H			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	–	0.5	2.5	–	1	4	–	2	6	mV
Input Offset Current	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	–	0.6	5.0	–	2.0	10	–	5.0	20	nA
Input Bias Current	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	–	20	50	–	50	80	–	100	150	nA
Input Noise Voltage Density	e_n	$f_o = 10Hz$ (Note 1)	–	20	40	–	20	40	–	20	40	$nV/\sqrt{Hz}$
		$f_o = 100Hz$ (Note 1)	–	15	30	–	15	30	–	15	30	
Input Noise Current Density	i_n	$f_o = 10Hz$ (Note 1)	–	0.3	0.6	–	0.3	0.6	–	0.3	0.6	$pA/\sqrt{Hz}$
		$f_o = 100Hz$ (Note 1)	–	0.2	0.4	–	0.2	0.4	–	0.2	0.4	
Input Voltage Range	IVR	V+ = +5V, V− = 0V	0	–	3.5	0	–	3.5	0	–	3.5	V
		$V_S = \pm 15V$	−15	–	13.5	−15	–	13.5	−15	–	13.5	
Common Mode Rejection Ratio	CMRR	V + = + 5V, V− = 0V, $0V \le V_{CM} \le +3.5V$	83	100	–	80	96	–	76	90	–	dB
		$V_S = \pm 15V$, $-15V \le V_{CM} \le +13.5V$	83	100	–	80	96	–	76	90	–	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$; and V− = 0V, V + = 5V to 30V	–	10	30	–	20	50	–	30	80	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$	200	400	–	100	200	–	100	200	–	V/mV
Output Voltage Swing	V_O	V+ = 5V, V− = 0V $R_L = 5k\Omega$	0.7	–	4.0	0.8	–	3.9	0.9	–	3.8	V
		$V_S = \pm 15V$, $R_L = 10k\Omega$	−14	–	+14	−13.9	–	+13.9	−13.8	–	+13.8	
Closed Loop Bandwidth (Note 2)	BW	$A_{VCL} = +1.0$, $R_L = 10k\Omega$	1.0	1.9	–	1.0	1.9	–	1.0	1.9	–	MHz
Supply Current	I_{SY}	$V_S = \pm 2.5V$, no load	–	0.6	1.0	–	0.7	1.5	–	0.9	2.0	mA
		$V_S = \pm 15V$, no load	–	1.2	1.8	–	1.4	2.3	–	1.8	3.0	
Slew Rate	SR	(Note 1)	0.25	0.5	–	0.25	0.5	–	0.25	0.5	–	V/μs
Channel Separation	CS	(Note 1)	100	120	–	100	120	–	100	120	–	dB

NOTE:
1. Sample tested.
2. Guaranteed by design.

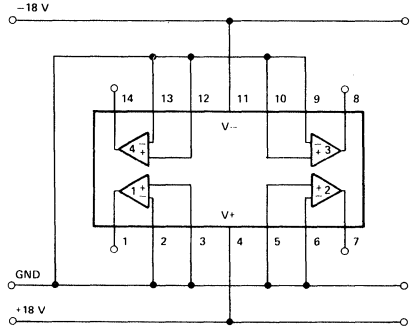
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ for OP-421B and OP-421C, $-25°C \leq T_A \leq +85°C$ for OP-421F and OP-421G, and $0°C \leq T_A \leq +70°C$ for OP-421H, unless otherwise noted.

			OP-421B OP-421F			OP-421C OP-421G			OP-421H			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}		–	5	10	–	8	15	–	10	15	µV/°C
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	–	1	3.5	–	1.8	5.5	–	3	7.5	mV
Input Offset Current	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	–	1.6	8	–	3.0	15	–	6.0	30	nA
Input Bias Current	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	–	25	70	–	60	125	–	140	230	nA
Input Voltage Range	IVR	V+ = +5V, V– = 0V	0	–	3.5	0	–	3.5	0	–	3.5	V
		$V_S = \pm 15V$	–15	–	13.5	–15	–	13.5	–15	–	13.5	
Common Mode Rejection Ratio	CMRR	V + = + 5V, V– = 0V, $0V \leq V_{CM} \leq +3.5V$	78	96	–	74	94	–	73	86	–	dB
		$V_S = \pm 15V$, $-15V \leq V_{CM} \leq +13.5V$	78	96	–	74	94	–	73	86	–	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$; and	–	15	50	–	25	80	–	40	100	µV/V
		V– = 0V, V + = 5V to 30V	–	15	50	–	25	80	–	40	100	
Large Signal Voltage Gain	A_{VO}	$R_L = 20k\Omega$	100	200	–	50	100	–	50	100	–	V/mV
Output Voltage Swing	V_O	V+ = 5V, V– = 0V, $R_L = 10k\Omega$	0.8	–	3.9	0.9	–	3.8	1.0	–	3.7	V
		$V_S = \pm 15V$, $R_L = 20k\Omega$	–13.8	–	+13.8	–13.7	–	+13.7	–13.7	–	+13.7	
Supply Current	I_{SY}	$V_S = \pm 2.5V$, no load	–	1.2	1.5	–	1.5	2.0	–	2.0	3.0	mA
		$V_S = \pm 15V$, no load	0.68	2.0	2.5	0.68	2.5	3.2	0.68	3.2	4.0	

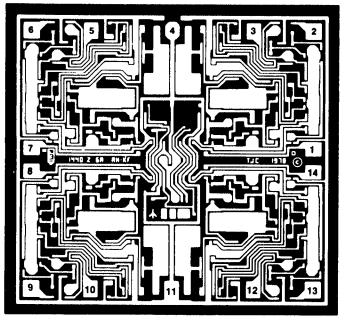
NOTE:

1. Sample tested.

BURN-IN CIRCUIT



DICE CHARACTERISITICS



DIE SIZE 0.086 × 0.092 inch

1. OUTPUT 1
2. INVERTING INPUT 1
3. NON-INVERTING INPUT 1
4. V+
5. NON-INVERTING INPUT 2
6. INVERTING INPUT 2
7. OUTPUT 2
8. OUTPUT 3
9. INVERTING INPUT 3
10. NON-INVERTING INPUT 3
11. V–
12. NON-INVERTING INPUT 4
13. INVERTING INPUT 4
14. OUTPUT 4

Refer to Section 2 for additional DICE informaiton.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

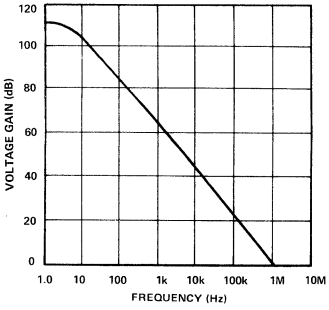
PARAMETER	SYMBOL	CONDITIONS	OP-421N LIMIT	OP-421G LIMIT	OP-421GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$V_S = +2.5V$ to $\pm 15V$	2.5	4	20	mV MAX
Input Offset Current	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	5.0	10	150	nA MAX
Input Bias Current	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	50	80	150	nA MAX
Input Voltage Range	IVR		−15 / +13.5	−15 / +13.5	−15 / +13.5	V MIN
Common Mode Rejection Ratio	CMRR	V + = + 5V, V− = 0V, 0V ≤ V_{CM} ≤ + 3.5V $V_S = \pm 15V$, − 15V ≤ V_{CM} ≤ + 13.5V	83	80	76	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$; and V− = 0V, V + = 5V to 30V	30	50	80	μV/V MAX
Output Voltage Swing	V_O	V+ = +5V, V− = 0V, $R_L = 5k\Omega$ $V_S = \pm 15V$, $R_L = 10k\Omega$	0.7/4.0 ± 14	0.8/3.9 ± 13.9	0.9/3.8 ±13.8	V MIN
Supply Current	I_{SY}	$V_S = \pm 2.5V$, No Load $V_S = \pm 15V$, No Load	1.0 1.8	1.5 2.3	2.0 3.0	mA MAX

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A + 25°C$, unless otherwise noted.

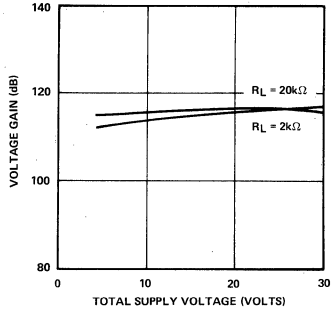
PARAMETER	SYMBOL	CONDITIONS	OP-421N TYPICAL	OP-421G TYPICAL	OP-421GR TYPICAL	UNITS
Input Noise Voltage Density	e_n	$f_O = 10Hz$ $f_O = 100Hz$	20 15	20 15	20 15	$nV/\sqrt{Hz}$
Closed Loop Bandwidth	BW	$A_{VCL} = +1.0$ $R_L = 10k\Omega$	1.9	1.9	1.9	MHz
Slew Rate	SR		0.5	0.5	0.5	V/μs
Channel Separation	CS		120	120	120	dB

TYPICAL PERFORMANCE CURVES

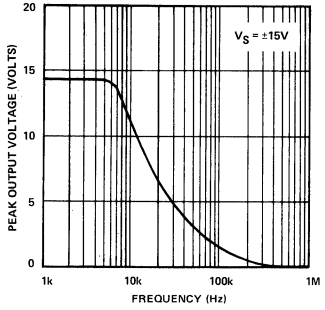
OPEN LOOP FREQUENCY RESPONSE



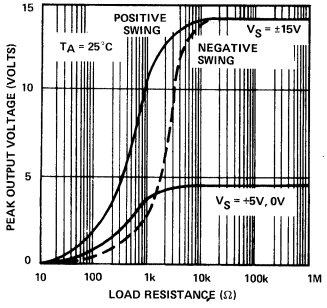
OPEN LOOP GAIN vs POWER SUPPLY VOLTAGE



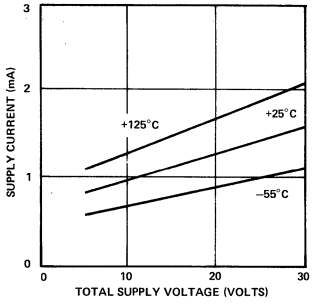
OUTPUT SWING vs FREQUENCY



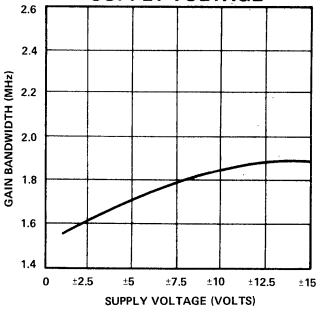
OUTPUT SWING vs OUTPUT LOAD



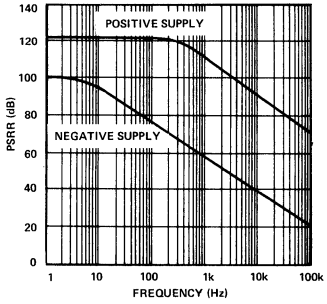
SUPPLY CURRENT vs SUPPLY VOLTAGE



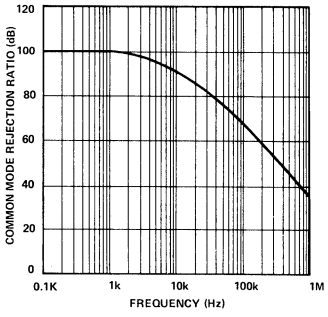
GAIN BANDWIDTH vs SUPPLY VOLTAGE



POWER SUPPLY REJECTION RATIO vs FREQUENCY

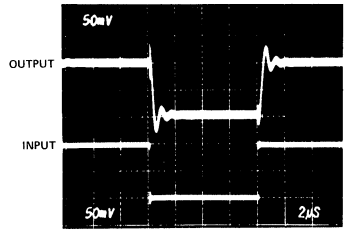


COMMON MODE REJECTION RATIO vs FREQUENCY



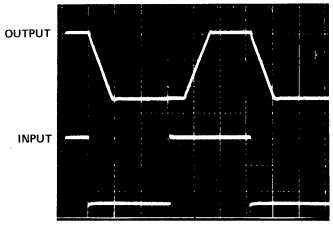
TYPICAL PERFORMANCE CURVES

VOLTAGE FOLLOWER SMALL-SIGNAL RESPONSE



V_S = 0V, +15V
R_L = 10kΩ
T_A = 25°C
C_L = 50pf

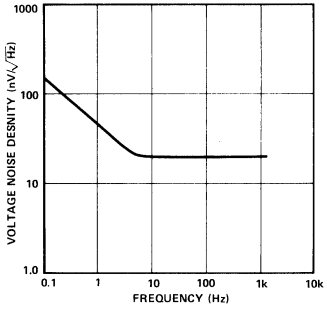
VOLTAGE FOLLOWER LARGE-SIGNAL RESPONSE



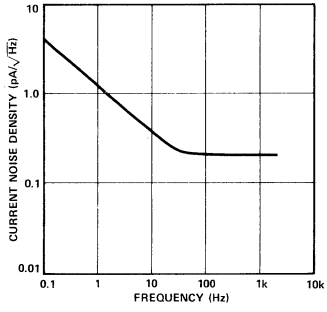
V_S = 0V, +15V
R_L = 10kΩ
T_A = 25°C
C_L = 50pf

NOISE CHARACTERISTICS

INPUT NOISE VOLTAGE DENSITY vs FREQUENCY



INPUT NOISE CURRENT DENSITY vs FREQUENCY



PM108A/PM2108A

LOW INPUT CURRENT OPERATIONAL AMPLIFIERS

PM108A/PM208A/PM308A/PM108/PM208/PM308
PM2108A/PM2108/PM2208A/PM2208/PM2308A/PM2308

FEATURES

- **Low Offset Current ..... 200pA Max**
- **Low Bias Current ..... 2.0nA Maximum**
- **Low Power Consumption ..... 18mW Maximum @ ±15V**
- **Wide Supply Range ..... ±3V to ±20V**
- **High Power Supply Rejection Ratio ..... 96dB Minimum**
- **Low Offset Voltage Drift ..... 5.0μV/°C Maximum**
- **High Common Mode Input Range .... ±13.5V Minimum**
- **High Common Mode Rejection Ratio ... 96dB Minimum**
- **MIL-STD-883 Class B Processing Models Available**
- **Silicon-Nitride Passivation**

GENERAL DESCRIPTION

The PM108A Series of precision monolithic operational amplifiers features extremely low input offset and bias currents. Although directly interchangeable with industry-standard types, Precision Monolithics' advanced processing technique provides a significant improvement in input noise voltage. Low supply current drain over a wide power supply range makes the PM108A attractive in battery operated and other low power applications. Low offset current and low bias current provide excellent performance with piezoelectric and capacitive transducers and in high impedance circuits such as long period integrators and sample-and-holds. For improved performance see OP-08, OP-12, OP-20 and OP-21.

The PM2108A series contains two superbeta, PM108A op amps in a single 16-pin DIP. Models are provided for -55°/+125°C, -25°C/+85°C and 0°C/+70°C operation in low power applications. Compared to the single PM108A types, these models offer higher packaging density, closer thermal tracking between the two amplifiers, and reduced insertion cost. For improved performance see OP-220.

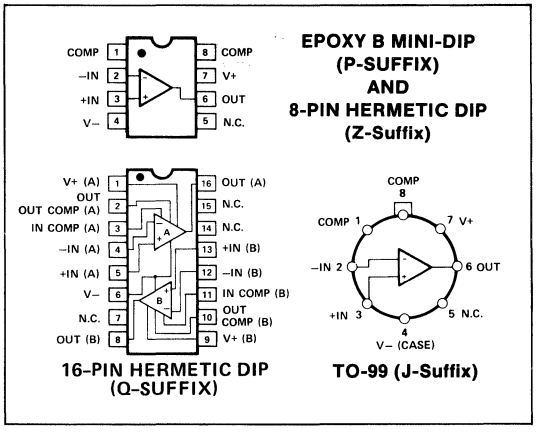
ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (mV)	PACKAGE: HERMETIC TO-99 8-PIN	HERMETIC DIP 8-PIN	HERMETIC DIP 16-PIN	PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
0.5	PM108AJ*	PM108AZ*	PM2108AQ*		MIL
0.5	PM208AJ	PM208AZ	PM2208AQ		IND
0.5	PM308AJ	PM308AZ	PM2308AQ	PM308AP	COM
2.0	PM108J*	PM108Z*	PM2108Q*		MIL
2.0	PM208J	PM208Z	PM2208Q		IND
7.5	PM308J	PM308Z	PM2308Q	PM308P	COM

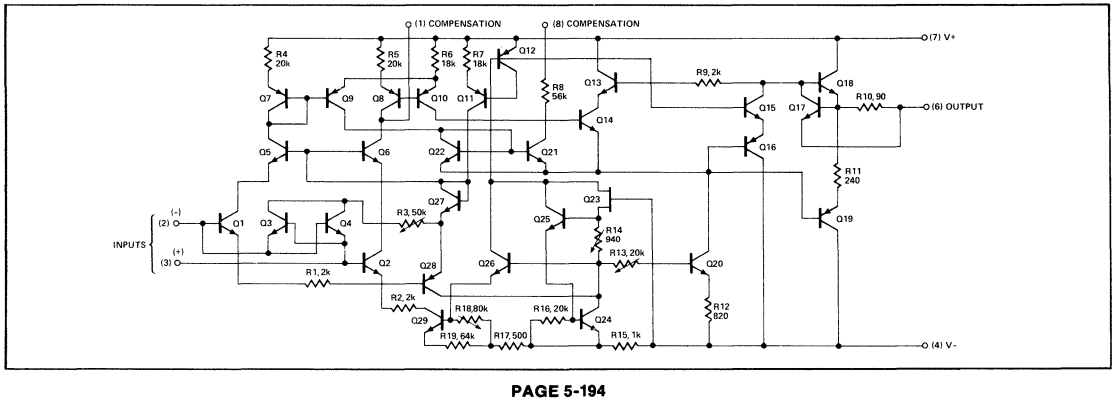
* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

† All listed parts are available with 160 hour burn-in. See ordering information, Section 2.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (Pin numbers for PM108 only. Circuit is 1/2 2108.)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage
PM108A, PM108, PM208A, PM208,
PM2108A, PM2108, PM2208A, PM2208 ..... ± 20V
PM308A, PM308, PM2308A, PM2308 ..... ± 18V
Internal Power Dissipation (Note 1) 500mW
Differential Input Current (Note 2).....±10mA
Input Voltage (Note 3) .....±15V
Output Short Circuit Duration.....Indefinite
Operating Temperature Range
PM108A, PM108, PM2108,
PM2108A .....−55°C to +125°C
PM208A, PM208, PM2208,
PM2208A .....−25°C to +85°C
PM308A, PM308, PM2308,
PM2308A ..... 0°C to +70°C
Storage Temperature Range
(Q-, J-, or Z-Package) ..... -65°C to + 150°C
(P-Package) ..... -65°C to + 125°C

Lead Temperature Range
(Soldering, 60 sec.) .....300°C

NOTE 1. Maximum package power dissipation vs ambient temperature:

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
Plastic 8-Pin Dip (P)	36°C	5.6mW/°C
Hermetic 8-Pin Dip (Z)	75°C	6.7mW/°C
Hermetic 16-Pin Dip (Q)	100°C	10.0 mW/°C

Note 2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, if a differential input voltage in excess of 1V is applied between the inputs, excessive current will flow, unless some limiting resistance is provided.
NOTE 3. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS at $\pm 5V \le V_S \le \pm 20V$ and $T_A = 25°C$, unless otherwise noted.

			PM108A/PM2108A PM208A/PM2208A			PM108/PM2108 PM208/PM2208			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.3	0.5	—	0.7	2.0	mV
Input Offset Current	I_{OS}		—	0.05	0.2	—	0.05	0.2	nA
Input Bias Current	I_B		—	0.8	2.0	—	0.8	2.0	nA
Input Resistance	R_{IN}	(Note 1)	30	70	—	30	70	—	MΩ
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \ge 10k\Omega$	80	300	—	50	300	—	V/mV
Supply Current	I_{SY}	$I_{OUT} = 0$, $V_{OUT} = 0$, Each amplifer	—	0.3	0.6	—	0.3	0.6	mA

ELECTRICAL CHARACTERISTICS at $\pm 5V \le V_S \le \pm 20V$, $-55°C \le T_A \le +125°C$ for PM108A, PM108, PM2108A and PM2108, $-25°C \le T_A \le +85°C$ for PM208A, PM208, PM2208A and PM2208, unless otherwise noted.

			PM108A/PM2108A PM208A/PM2208A			PM108/PM2108 PM208/PM2208			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.4	1.0	—	1.0	3.0	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	1.0	5.0	—	3.0	15	µV/°C
Input Offset Current	I_{OS}		—	0.1	0.4	—	0.1	0.4	nA
Average Input Offset Current Drift	TCI_{OS}		—	0.5	2.5	—	0.5	2.5	pA/°C
Input Bias Current	I_B		—	1.0	3.0	—	1.0	3.0	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \ge 10k\Omega$	40	200	—	25	200	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 15V$, $R_L = 10k\Omega$	±13	±14	—	±13	±14	—	V
Input Voltage Range	IVR	$V_S = \pm 15V$	±13.5	—	—	±13.5	—	—	V
Common Mode Rejection Ratio	CMRR	$V_S = \pm 15V$, $V_{CM} = \pm 13.5V$	96	110	—	85	100	—	dB
Supply Voltage Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$	—	3	15	—	15	100	µV/V
Supply Current	I_{SY}	$V_{OUT} = 0$, T_A = MAX, Each amplifier	—	0.15	0.4	—	0.15	0.4	mA

NOTE:
1. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $\pm 5V \leq V_S \leq \pm 15V$ and $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM308A/PM2308A MIN	PM308A/PM2308A TYP	PM308A/PM2308A MAX	PM308/PM2308 MIN	PM308/PM2308 TYP	PM308/PM2308 MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.3	0.5	—	2.0	7.5	mV
Input Offset Current	I_{OS}		—	0.2	1.0	—	0.2	1.0	nA
Input Bias Current	I_B		—	1.5	7.0	—	1.5	7.0	nA
Input Resistance	R_{IN}	(Note 1)	10	40	—	10	40	—	MΩ
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 10k\Omega$	80	300	—	25	300	—	V/mV
Supply Current	I_{SY}	$I_{OUT} = 0$, $V_{OUT} = 0$, Each amplifer	—	0.3	0.8	—	0.3	0.8	mA

ELECTRICAL CHARACTERISTICS at $\pm 5V \leq V_S \leq \pm 15V$ and $0°C \leq T_A \leq +70°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM308A/PM2308A MIN	PM308A/PM2308A TYP	PM308A/PM2308A MAX	PM308/PM2308 MIN	PM308/PM2308 TYP	PM308/PM2308 MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.4	0.73	—	3.0	10.0	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	1.0	5.0	—	6.0	30	μV/°C
Input Offset Current	I_{OS}		—	0.3	1.5	—	0.3	1.5	nA
Average Input Offset Current Drift	TCI_{OS}		—	2.0	10	—	2.0	10	pA/°C
Input Bias Current	I_B		—	2.0	10	—	2.0	10	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 10k\Omega$	60	200	—	15	100	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 15V$, $R_L = 10k\Omega$	±13	±14	—	±13	±14	—	V
Input Voltage Range	IVR	$V_S = \pm 15V$	±14	—	—	±13	—	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$	96	110	—	80	100	—	dB
Supply Voltage Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	—	3	15	—	15	100	μV/V
Supply Current	I_{SY}	$V_{OUT} = 0$, T_A = MAX, Each amplifier	—	0.23	—	—	0.23	—	mA

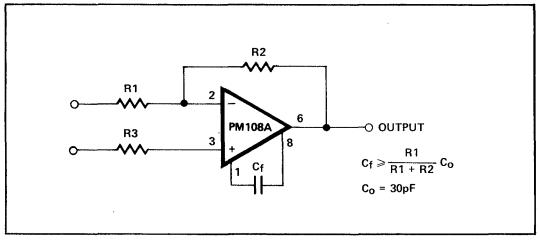
NOTE:
1. Guaranteed by design.

APPLICATION INFORMATION

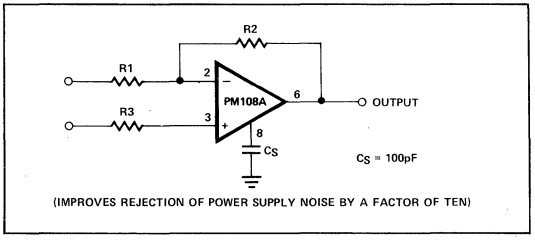
The PM108A series has extremely low input offset and bias currents; the user is cautioned that stray printed circuit board leakages can produce significant errors, especially at high board temperatures. Careful attention to board layout and cleaning procedure is required to fully realize the PM108A's performance. It is suggested that effects of board leakage be minimized by encircling the input pins with a conductive guard ring operated at a potential close to that of the inputs. This guard ring should be driven by a low impedance source such as the amplifier's output for non-inverting circuits, or be tied to ground for inverting circuits.

COMPENSATION CIRCUITS

STANDARD



ALTERNATE



PM155A, PM156A, PM157A

MONOLITHIC JFET INPUT OPERATIONAL AMPLIFIERS

PM155A/PM355A/PM155/PM255/PM355 LOW SUPPLY CURRENT
PM156A/PM356A/PM156/PM256/PM356
PM157A/PM357A/PM157/PM257/PM357
WIDE BANDWIDTH DECOMPENSATED ($A_{V_{MIN}} = 5$)

FEATURES

All Devices

- **Internal Compensation**
- **Low Input Bias and Offset Currents**
- **Low Input Offset Voltage 1.0mV**
- **Low Input Offset Voltage Drift ..... 3.0μV/°C**
- **Low Input Noise Current ..... 0.01pA/√Hz**
- **High Common-Mode Rejection Ratio 100dB**
- **Models With MIL-STD-883 Class B Processing Available From Stock**
- **125° C Temperature Tested Dice (See OP-15,16,17 Data Sheet)**

PM155 (Only) ..... LF155 Replacement

- **Low Supply Current 2mA**

PM156 (Only) ..... LF156 Replacement

- **High Slew Rate 12V/μsec**
- **Fast Settling to ±0.01% 1.5μsec**

PM157 (Only) ..... LF157 Replacement

- **Wide Bandwidth (A_{VCL} = 5 Min) 20MHz**
- **Higher Slew Rate 50V/μsec**
- **Fast Settling to ±0.01% 1.5μsec**

GENERAL DESCRIPTION

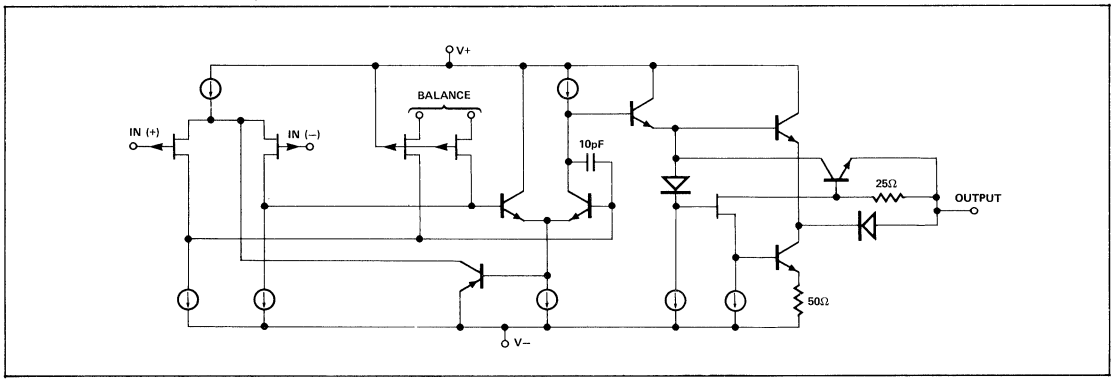
The PM BIFET Series provides low input current, high slew rate, and direct interchangeability with LF155, 156, and 157 types. These operational amplifiers use a new process which allows fabrication of matched JFET transistors and standard bipolar transistors on the same chip. High accuracy and low cost make the PM BIFET Series useful in new designs and as replacements for modular and hybrid types. Unlike many designs, nulling the input offset voltage does not degrade common-mode rejection ratio or input offset voltage drift. Low input voltage noise and current noise plus a low 1/f noise corner frequency allow these amplifiers to be used in a variety of low noise, wide bandwidth applications.

Dynamic specifications for the PM155 include a slew rate of 5V/μs, a 2.5MHz gain bandwidth product, and settling time to within ±0.01% of final value in 4.0μs. The PM156 has a slew rate of 12V/μs and a settling time of 1.5μs to ±0.01% of final value.

The PM157 is a very fast decompensated device. This results in a 50V/μs slew rate, a 20MHz gain bandwidth product, and a settling time of 1.5μs. Decompensation requires a minimum closed loop gain of five because of stability considerations.

For improved performance see the OP-15/OP-16/OP-17 data sheet. For duals see the OP-215 data sheet.

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- PM155A, PM156A, PM157A, PM155, PM156, PM157, PM255, PM256, PM257, PM355A, PM356A, PM357A ..... ±22V
- PM355, PM356, PM357 ..... ±18V

Internal Power Dissipation
- PM155A, PM156A, PM157A, PM155, PM156, PM157 ..... 670mW
- PM255, PM256, PM257 ..... 570mW
- PM355A, PM356A, PM357A, PM355, PM356, PM357 ..... 500mW
  (Derate based on a thermal resistance of 150° C/W junction to ambient or 45° C/W junction to case.)

Operating Temperature Range
- PM155A, PM156A, PM157A, PM155, PM156, PM157 ..... −55° C to +125° C
- PM255, PM256, PM257 ..... −25° C to +85° C
- PM355A, PM356A, PM357A, PM355, PM356, PM357 ..... 0° C to +70° C

Maximum Junction Temperature (T_j)
- PM155A, PM156A, PM157A, PM155, PM156, PM157 ..... +150° C
- PM255, PM256, PM257 ..... +115° C
- PM355A, PM356A, PM357A, PM355, PM356, PM357 ..... +100° C

Differential Input Voltage
- PM155A, PM156A, PM157A, PM155, PM156, PM157, PM255, PM256, PM257, PM355A, PM356A, PM357A ..... ±40V
- PM355, PM356, PM357 ..... ±30V

Input Voltage
- PM155A, PM156A, PM157A, PM155, PM156, PM157, PM255, PM256, PM257, PM355A, PM356A, PM357A ..... ±20V
- PM355, PM356, PM357 ..... ±16V
  (unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.)

Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... −65° C to +150° C
Lead Temperature Range (Soldering, 60 sec.) ... +300° C

ELECTRICAL CHARACTERISTICS at $\pm 15V \le V_S \le \pm 20V$, $-55° C \le T_A \le +125° C$ and $T_{HIGH} = +125° C$ for PM155A, PM156A and PM157A, $0° C \le T_A \le +70° C$ and $T_{HIGH} = +70° C$ for PM355A, PM356A and PM357A, unless otherwise noted.

			PM155A/ PM156A/ PM157A			PM355A/ PM356A/ PM357A			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	1.4	2.5	—	1.2	2.3	mV
Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	—	3.0	5.0	—	3.0	5.0	µV/° C
Change in Input Offset Drift with V_{OS} Adjust	$\left(\frac{\Delta TCV_{OS}}{\Delta V_{OS}}\right)$	$R_S = 50\Omega$	—	0.5	—	—	0.5	—	µV/° C per mV
Input Offset Current	I_{OS}	$T_j \le T_{HIGH}$ (Note 1)	—	4.0	10	—	0.4	1.0	nA
Input Bias Current	I_B	$T_j \le T_{HIGH}$ (Note 1)	—	10	25	—	2.0	5.0	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 2k\Omega$	25	75	—	25	75	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 15V$, $R_L = 10k\Omega$ $V_S = \pm 15V$, $R_L = 2k\Omega$	±12 ±10	±13 ±12	— —	±12 ±10	±13 ±12	— —	V
Input Voltage Range	IVR	$V_S = \pm 15V$	±10.4	+15.1 −12.0	—	±10.4	+15.1 −12.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	85	100	—	85	100	—	dB
Power Supply Rejection Ratio	PSRR	(Note 2)	—	10	57	—	10	57	µV/V

NOTES:

1. Input bias current is specified for two different conditions. The $T_j = 25° C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at 25° C ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs T_j and I_B vs T_A. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Power supply rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

ELECTRICAL CHARACTERISTICS at $\pm 15V \leq V_S \leq \pm 20V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		PM155A/ PM156A/ PM157A MIN	TYP	MAX	PM355A/ PM356A/ PM357A MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$		—	1.0	2.0	—	1.0	2.0	mV
Input Offset Current	I_{OS}	$T_j = 25°C$ (Note 1)		—	3.0	10	—	3.0	10	pA
Input Bias Current	I_B	$T_j = 25°C$ (Note 1)		—	30	50	—	30	50	pA
Input Resistance	R_{IN}			—	10^{12}	—	—	10^{12}	—	Ω
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 2k\Omega$		50	200	—	50	200	—	V/mV
Supply Current	I_{SY}	$V_S = \pm 15V$	PM155	—	2.0	4.0	—	2.0	4.0	mA
			PM156/PM157	—	5.0	7.0	—	5.0	7.0	
Slew Rate	SR	$A_{VCL} = +1$, $V_S = \pm 15V$	PM155	3.0	5.0	—	3.0	5.0	—	V/μs
			PM156	10	12	—	10	12	—	
		$A_{VCL} = +5$, $V_S = \pm 15V$	PM157	40	50	—	40	50	—	
Gain Bandwidth Product	GBW	$A_{VCL} = +1$, $V_S = \pm 15V$	PM155	—	2.5	—	—	2.5	—	MHz
			PM156	4.0	4.5	—	4.0	4.5	—	
		$A_{VCL} = +5$, $V_S = \pm 15V$	PM157	15	20	—	15	20	—	
Settling Time (to ±0.01%)	t_S	$V_S = \pm 15V$ (Note 2)	PM155	—	4.0	—	—	4.0	—	μs
			PM156	—	1.5	—	—	1.5	—	
		$V_S = \pm 15V$ (Note 3)	PM157	—	1.5	—	—	1.5	—	
Input Noise Voltage	e_n	$R_S = 100\Omega$, f = 100Hz	PM155	—	25	—	—	25	—	nV/√Hz
		$R_S = 100\Omega$, f = 1000Hz		—	20	—	—	20	—	
		$R_S = 100\Omega$, f = 100Hz	PM156/PM157	—	15	—	—	15	—	
		$R_S = 100\Omega$, f = 1000Hz		—	12	—	—	12	—	
Input Noise Current	i_n	f = 100Hz, $V_S = \pm 15V$		—	0.01	—	—	0.01	—	pA/√Hz
		f = 1000Hz, $V_S = \pm 15V$		—	0.01	—	—	0.01	—	
Input Capacitance	C_{IN}			—	3.0	—	—	3.0	—	pF

NOTES:

1. Input bias current is specified for two different conditions. The $T_j = 25°C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at 25°C ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs T_j and I_B vs T_A. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Settling time is defined here for a unity gain inverter connection using 2kΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.
3. Settling time is defined here for a $A_V = -5$ connection with $R_F = 2k\Omega$. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 2V step input is applied to the inverter. See settling time test circuit.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $\pm 15V \leq V_S \leq \pm 20V$ for PM155, PM156, PM157, PM255, PM256 and PM257, $V_S = \pm 15V$ for PM355, PM356 and PM357, unless otherwise noted.

				PM155/156/157 PM255/256/257			PM355/ 356/357			
PARAMETER	**SYMBOL**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$		—	3.0	5.0	—	3.0	10	mV
Input Offset Current	I_{OS}	$T_j = 25°C$ (Note 1)		—	3.0	20	—	3.0	50	pA
Input Bias Current	I_B	$T_j = 25°C$ (Note 1)		—	30	100	—	30	200	pA
Input Resistance	R_{IN}			—	10^{12}	—	—	10^{12}	—	Ω
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 2k\Omega$		50	200	—	25	200	—	V/mV
Supply Current	I_{SY}	$V_S = \pm 15V$	PM155	—	2.0	4.0	—	2.0	4.0	mA
			PM156/PM157	—	5.0	7.0	—	5.0	10	
Slew Rate	SR	$A_{VCL} = +1$, $V_S = \pm 15V$	PM155	—	5.0	—	—	5.0	—	V/μs
			PM156	7.5	12	—	—	12	—	
		$A_{VCL} = +5$, $V_S = \pm 15V$	PM157	30	50	—	—	50	—	
Gain Bandwidth Product	GBW	$A_{VCL} = +1$, $V_S = \pm 15V$	PM155	—	2.5	—	—	2.5	—	MHz
			PM156	—	5.0	—	—	5.0	—	
		$A_{VCL} = +5$, $V_S = \pm 15V$	PM157	—	20	—	—	20	—	
Settling Time (to ±0.01%)	t_S	$V_S = \pm 15V$ (Note 2)	PM155	—	4.0	—	—	4.0	—	μs
			PM156	—	1.5	—	—	1.5	—	
		$V_S = \pm 15V$ (Note 3)	PM157	—	1.5	—	—	1.5	—	
Input Noise Voltage	e_n	$R_S = 100\Omega$, f = 100Hz	PM155	—	25	—	—	25	—	nV/√Hz
		$R_S = 100\Omega$, f = 1000Hz		—	20	—	—	20	—	
		$R_S = 100\Omega$, f = 100Hz	PM156/PM157	—	15	—	—	15	—	
		$R_S = 100\Omega$, f = 1000Hz		—	12	—	—	12	—	
Input Noise Current	i_n	f = 100Hz, $V_S = \pm 15V$		—	0.01	—	—	0.01	—	pA/√Hz
		f = 1000Hz, $V_S = \pm 15V$								
Input Capacitance	C_{IN}			—	3.0	—	—	3.0	—	pF

NOTES:

1. Input bias current is specified for two different conditions. The $T_j = 25°C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at 25° C ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs T_j and I_B vs T_A. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Settling time is defined here for a unity gain inverter connection using 2kΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.
3. Settling time is defined here for a $A_V = -5$ connection with $R_F = 2k\Omega$. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 2V step input is applied to the inverter. See settling time test circuit.

ELECTRICAL CHARACTERISTICS at $\pm 15V, \leq V_S \leq \pm 20V$, $-55°C \leq T_A \leq +125°C$ and $T_{HIGH} = +125°C$ for PM155, PM156 and PM157, $\pm 15V \leq V_S \leq \pm 20V$, $-25°C \leq T_A \leq +85°C$ and $T_{HIGH} = +85°C$ for PM255, PM256 and PM257, $V_S = \pm 15V$, $0°C \leq T_A \leq +70°C$ and $T_{HIGH} = +70°C$ for PM355, PM356 and PM357, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM155/156/157 MIN	PM155/156/157 TYP	PM155/156/157 MAX	PM255/256/257 MIN	PM255/256/257 TYP	PM255/256/257 MAX	PM355/356/357 MIN	PM355/356/357 TYP	PM355/356/357 MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	4.0	7.0	—	3.5	6.5	—	5.0	13	mV
Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	—	5.0	—	—	5.0	—	—	5.0	—	$\mu V/°C$
Change In Input Offset Drift With V_{OS} Adjust.	$\left(\frac{\Delta TCV_{OS}}{\Delta V_{OS}}\right)$	$R_S = 50\Omega$	—	0.5	—	—	0.5	—	—	0.5	—	$\mu V/°C$ per mV
Input Offset Current	I_{OS}	$T_j \leq T_{HIGH}$ (Note 1)	—	8.0	20	—	0.5	1.0	—	1.0	2.0	nA
Input Bias Current	I_B	$T_j \leq T_{HIGH}$ (Note 1)	—	20	50	—	2.0	5.0	—	3.0	8.0	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 2k\Omega$	25	75	—	25	75	—	15	50	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 15V$, $R_L = 10k\Omega$ $V_S = \pm 15V$, $R_L = 2k\Omega$	± 12 ± 10	± 13 ± 12	— —	± 12 ± 10	± 13 ± 12	— —	± 12 ± 10	± 13 ± 12	— —	V
Input Voltage Range	IVR	$V_S = \pm 15V$	± 10.4	$+15.1$ -12.0	—	± 10.4	$+15.1$ -12.0	—	± 10.0	$+15.1$ -12.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	85	100	—	85	100	—	80	100	—	dB
Power Supply Rejection Ratio	PSRR	(Note 2)	—	10	57	—	10	57	—	10	100	$\mu V/V$

NOTES:

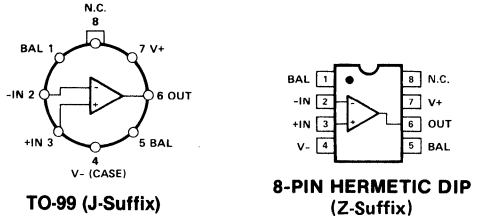
1. Input bias current is specified for two different conditions. The $T_j = 25°C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at 25° C ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs T_j and I_B vs T_A. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$. For PM155: $T_j = +125°C$. For PM255: $T_j = +85°C$. For PM355: $T_j = +70°C$.
2. Power supply rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	PACKAGE 8-PIN HERMETIC DIP	OPERATING TEMPERATURE RANGE
2.0	PM155AJ* PM156AJ* PM157AJ*	PM155AZ* PM156AZ* PM157AZ*	MIL
2.0	PM355AJ PM356AJ PM357AJ	PM355AZ PM356AZ PM357AZ	COM
5.0	PM155J* PM156J* PM157J*	PM155Z* PM156Z* PM157Z*	MIL
5.0	PM255J PM256J PM257J	PM255Z PM256Z PM257Z	IND
10	PM355J PM356J PM357J	PM355Z PM356Z PM357Z	COM

*Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.
†All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS

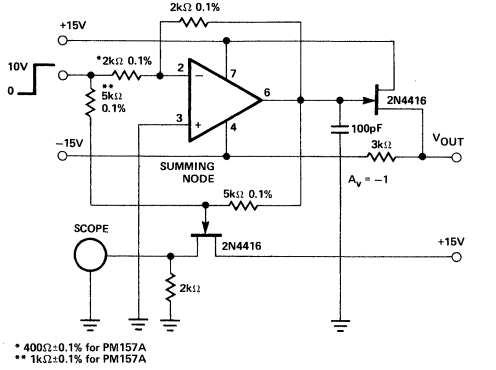


TO-99 (J-Suffix)

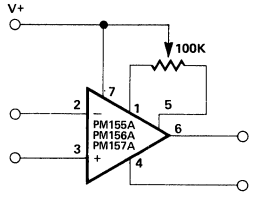
8-PIN HERMETIC DIP (Z-Suffix)

BASIC CONNECTIONS

SETTLING TIME TEST CIRCUIT



INPUT OFFSET VOLTAGE NULLING



NOTE: FOR POTENTIOMETERS WITH A TEMPERATURE COEFFICIENT ≤ 100ppm/°C THE ADDED TCV_{OS} WITH NULLING IS ≈ 0.5μV/°C/mV OF ADJUSTMENT.

APPLICATION INFORMATION

INPUT VOLTAGE CONSIDERATIONS

The PM Series JFET input stages can accommodate large input differential voltages without external clamping as long as neither input exceeds the negative power supply. An input voltage which is more negative than V− can result in a destroyed unit.

If both inputs exceed the negative common mode voltage limit, the amplifier will be forced to a high positive output. If only one input exceeds the negative common mode voltage limit, a phase reversal takes place forcing the output to the corresponding high or low state. In either of the above conditions, normal operation will return when both inputs are returned to within the specified common mode voltage range.

Exceeding the positive common-mode limit on a single input will not change the phase of the output. However, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

POWER SUPPLY CONSIDERATIONS

Power supply polarity reversal can result in a destroyed unit.

DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency a lead capacitor should be placed from the output to the inverting input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

PM725

INSTRUMENTATION OPERATIONAL AMPLIFIER

FEATURES

- **Extremely High Voltage Gain ..... 3M Typical**
- **Low Offset Voltage and Offset Current**
- **Low Drift with Temperature**
- **Low Input Voltage and Current Noise**
- **High Common Mode Rejection ..... 110dB Minimum**
- **High Power Supply Rejection ..... 10μV/V Maximum**
- **Silicon-Nitride Passivation**
- **Differential Input Overvoltage Protection**

GENERAL INFORMATION

The PM725 Series of monolithic Instrumentation Operational Amplifiers provides industry-standard 725 specifications. In addition, Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process minimizes "popcorn noise" and provides maximum reliability and long-term stability of parameters for lowest overall system operating cost. For improved specifications, see the OP-06 Series data sheet. For devices with internal frequency compensation see the OP-05 instrumentation and Op-07 Ultra-low Offset Voltage Operational Amplifier data sheets.

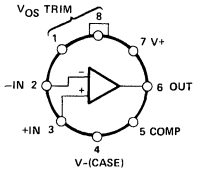
ORDERING INFORMATION†

	PACKAGE				
	HERMETIC				
T_A = 25°C V_{OS} MAX (mV)	TO-99 8-PIN	DIP 8-PIN	DIP 14-PIN	PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
1.0	PM725J*	PM725Z*	PM725Y*		MIL
2.5	PM725CJ	PM725CZ	PM725CY	PM725CP	COM

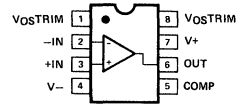
* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

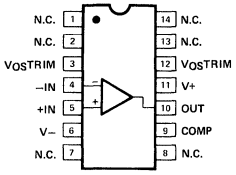
PIN CONNECTIONS



TO-99
(J-Suffix)



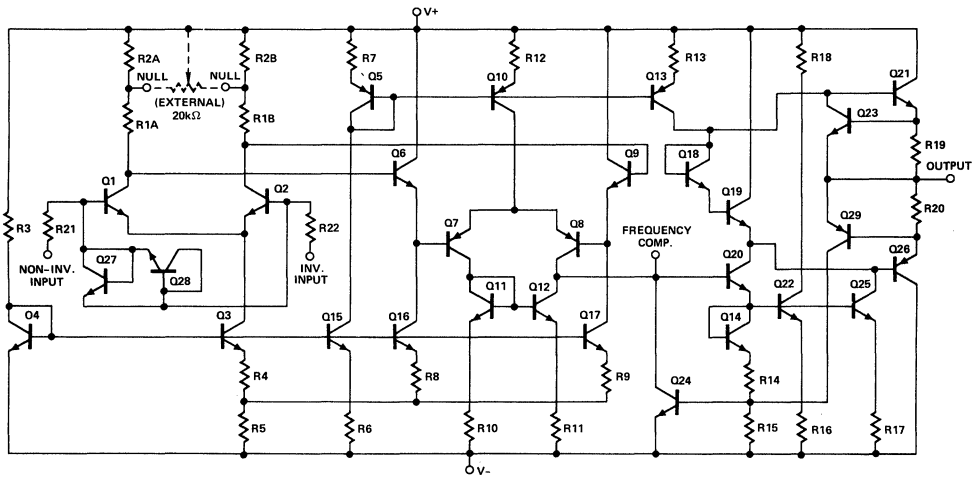
8-PIN HERMETIC DIP
(Z-Suffix)
&
EPOXY B MINI-DIP
(P-Suffix)



14-PIN DIP*
(Y-Suffix)

*Not recommended for new design.

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Internal Power Dissipation (see note) 500mW
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply Voltage
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range
J, Y, and Z Packages ..... -65°C to + 150°C
P Package ..... -65°C to + 125°C
Operating Temperature Range
PM725 ..... -55°C to +125°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
PM725C ..... 0°C to +70°C

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
8-Pin Plastic DIP (P)	36°C	5.6mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
14-Pin Hermetic DIP(Y)	100°C	10.0mW/°C

NOTE:
1. See table for maximum ambient temperature rating and derating factor.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

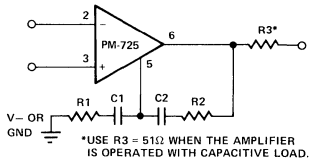
PARAMETER	SYMBOL	CONDITIONS	PM725 MIN	PM725 TYP	PM725 MAX	PM725C MIN	PM725C TYP	PM725C MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	0.5	1.0	—	0.5	2.5	mV
Input Offset Current	I_{OS}		—	2.0	20	—	2.0	35	nA
Input Bias Current	I_B		—	42	100	—	42	125	nA
Input Noise Voltage	e_n	f_o = 10Hz	—	15	—	—	15	—	nV/√Hz
		f_o = 100Hz	—	9.0	—	—	9.0	—	
		f_o = 1kHz	—	8.0	—	—	8.0	—	
Input Resistance	R_{IN}		—	1.5	—	—	1.5	—	MΩ
Input Voltage Range	IVR		±13.5	±14	—	±13.5	±14	—	V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	1,000,000	3,000,000	—	250,000	3,000,000	—	V/V
Common Mode Rejection Ratio	CMRR	$R_S \leq 10k\Omega$, $V_{CM} = \pm 13.5V$	110	120	—	94	120	—	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 10k\Omega$, $V_S = \pm 5V$ to $\pm 15V$	—	2.0	10	—	2.0	35	μV/V
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12.0	±13.5	—	±12.0	±13.5	—	V
		$R_L \geq 2k\Omega$	±10.0	±13.5	—	±10.0	±13.5	—	
Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	150	—	—	150	—	Ω
Power Consumption	P_d	No load	—	80	105	—	80	150	mW

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ for PM725, $0°C \leq T_A \leq +70°C$ for PM725C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM725 MIN	PM725 TYP	PM725 MAX	PM725C MIN	PM725C TYP	PM725C MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	—	1.5	—	—	3.5	mV
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$, Unnulled (Note 1)	—	2.0	5.0	—	2.0	—	μV/°C
Average Input Offset Voltage Drift	TCV_{OSn}	$R_S = 50\Omega$, Nulled	—	0.6	—	—	0.6	—	μV/°C
Input Offset Current	I_{OS}	T_A = MAX	—	1.2	20	—	1.2	35	nA
		T_A = MIN	—	7.5	40	—	4.0	50	
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	35	150	—	10	—	pA/°C
Input Bias Current	I_B	T_A = MAX	—	20	100	—	30	125	nA
		T_A = MIN	—	80	200	—	100	250	
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, T_A = MAX	1,000,000	—	—	125,000	—	—	V/V
		$R_L \geq 2k\Omega$, T_A = MIN	250,000	—	—	125,000	—	—	
Common Mode Rejection Ratio	CMRR	$R_S \leq 10k\Omega$, $V_{CM} = \pm 13.5V$	100	—	—	—	115	—	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 10k\Omega$, $V_S = \pm 5V$ to $\pm 15V$	—	—	20	—	20	—	μV/V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±10	—	—	±10	—	—	V

NOTE:
1. Sample tested.

COMPENSATION CIRCUIT



*USE R3 = 51Ω WHEN THE AMPLIFIER IS OPERATED WITH CAPACITIVE LOAD.

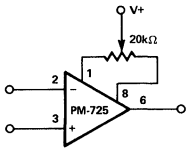
COMPENSATION COMPONENT VALUES

A_V	R_1 (Ω)	C_1 (μF)	R_2 (Ω)	C_2 (μF)
10,000	10k	50pF		
1,000	470	0.001		
100	47	0.01		
10	27	0.05	270	0.0015
1	10	0.05	39	0.02

*FOR MAXIMUM PSRR VS FREQUENCY COMPENSATION NETWORK SHOULD BE RETURNED TO V–

*

VOLTAGE OFFSET NULL CIRCUIT



*

*PINOUTS FOR J, Z AND P PACKAGES.

PM741

COMPENSATED OPERATIONAL AMPLIFIER

FEATURES

- **Industry Standard 741 Specifications**
- **Internal Frequency Compensation**
- **Continuous Short Circuit Protection**
- **MIL-STD-883 Processing Available**
- **Silicon-Nitride Passivation**
- **Low Noise**

GENERAL DESCRIPTION

The PM741 Series of Internally Compensated Operational Amplifiers provides industry-standard 741 specifications. In addition, Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process provides maximum reliability and long term stability of parameters for lowest overall system operating cost. For very high performance general purpose op amps, refer to the OP-02 Series data sheet. For duals see OP-03, OP-04 and OP-14.

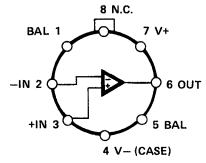
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (mV)	HERMETIC PACKAGE TO-99 8-PIN	HERMETIC PACKAGE DIP 8-PIN	HERMETIC PACKAGE DIP 14-PIN	OPERATING TEMPERATURE RANGE
5.0	PM741J*	PM741Z*	PM741Y*	MIL
6.0	PM741CJ	PM741CZ	PM741CY	COM

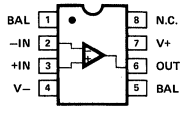
*Also available with MIL-STD-883B processing. To order add /883 as a suffix to the part number.

†All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

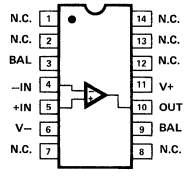
PIN CONNECTIONS



TO-99
(J-Suffix)



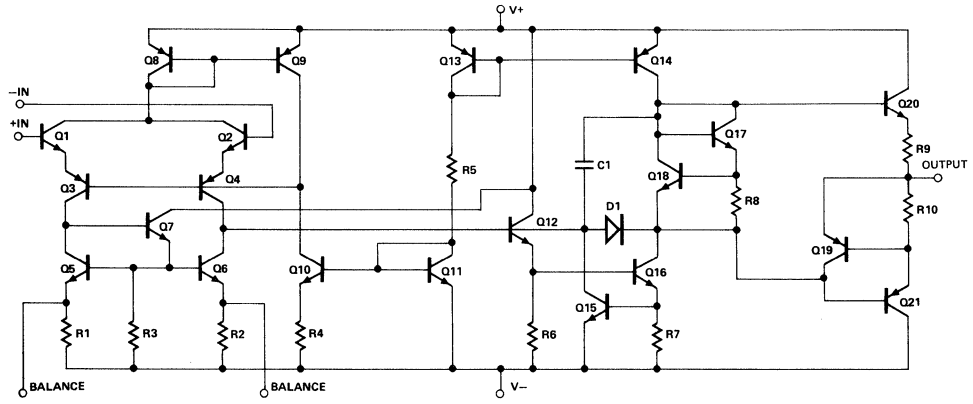
8-PIN HERMETIC DIP
(Z-Suffix)



14-PIN HERMETIC DIP*
(Y-Suffix)

*Not Recommended for new designs.

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- PM741 ..... ±22V
- PM741C ..... ±18V

Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply Voltage
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec.) ..... 300°C
Operating Temperature Range
- PM741 ..... −55°C to +125°C
- PM741C ..... 0°C to + 70°C

NOTE:
1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATUARE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
14-PIN HERMETIC DIP (Y)	100°C	10.0mW/°C
8-PIN HERMETIC DIP (Z)	75°C	6.7mW/°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_S = ±15V, unless otherwise noted.

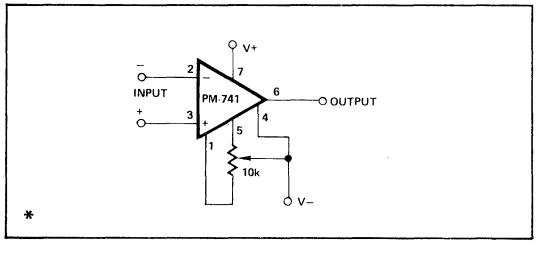
PARAMETER	SYMBOL	CONDITIONS	PM741 MIN	PM741 TYP	PM741 MAX	PM741C MIN	PM741C TYP	PM741C MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	—	5.0	—	—	6.0	mV
Input Offset Current	I_{OS}		—	—	200	—	—	200	nA
Input Bias Current	I_B		—	—	500	—	—	500	nA
Input Resistance	R_{IN}	(Note 1)	0.3	—	—	0.3	—	—	MΩ
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	50,000	—	—	25,000	—	—	V/V
Supply Current	I_{SY}	$V_{OUT} = 0$	—	—	2.8	—	—	2.8	mA

ELECTRICAL CHARACTERISTICS at −55°C ≤ T_A ≤ +125°C for PM741, 0°C ≤ T_A ≤ +70°C for PM741C, V_S = ±15V, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM741 MIN	PM741 TYP	PM741 MAX	PM741C MIN	PM741C TYP	PM741C MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	—	6.0	—	—	7.5	mV
Input Offset Current	I_{OS}		—	—	500	—	—	300	nA
Input Bias Current	I_B		—	—	1.5	—	—	0.8	μA
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	25,000	—	—	15,000	—	—	V/V
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 1k\Omega$	±12 ±10	— —	— —	±12 ±10	— —	— —	V
Input Voltage Range	IVR		±12	—	—	±12	—	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	70	—	—	70	—	—	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 10k\Omega$	—	—	142	—	—	142	μV/V

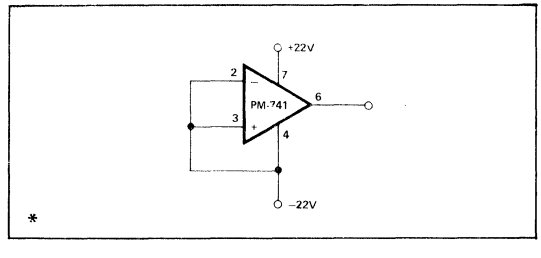
NOTE:
1. Guaranteed by design.

TYPICAL OFFSET NULLING CIRCUIT*



*

TYPICAL BURN-IN CIRCUIT*



*

*PINOUTS FOR J AND Z PACKAGES.

PM747/PM1458/1558

DUAL COMPENSATED OPERATIONAL AMPLIFIERS

FEATURES

- **Industry Standard 741 Specifications**
- **Dual PM741 Internally Compensated Operational Amplifier ..... PM747 and PM1458**
- **Internal Frequency Compensation**
- **Low Power Consumption**
- **Continuous Short Circuit Protection**
- **MIL-STD-883 Processing Available**
- **Silicon-Nitride Passivation**

GENERAL DESCRIPTION

The PMI Series of Internally Compensated Operational Amplifiers provides industry-standard 747 and 1458 specifications. In addition, Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process provides maximum reliability and long term stability of parameters for lowest overall system operating cost. For very high performance dual general-purpose op amps, refer to the OP-03/OP-04/OP-14 data sheet.

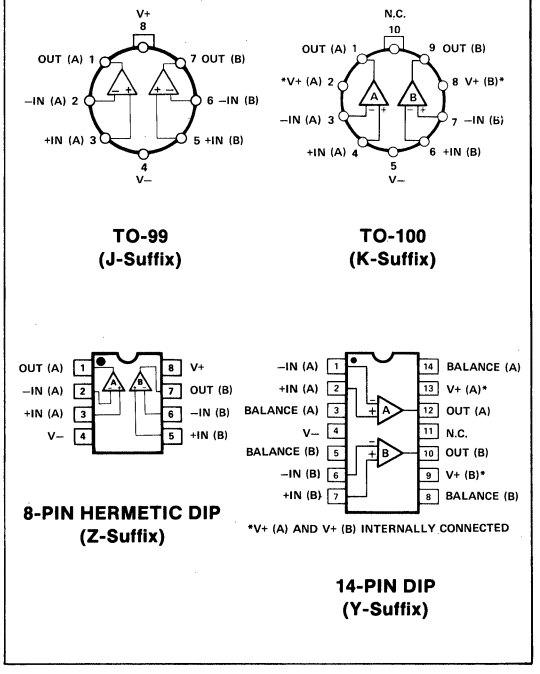
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	TO-100 10-PIN	HERMETIC DIP 8-PIN	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
5.0	PM1558J*	PM747K*	PM1558Z*	PM747Y*	MIL
6.0	PM1458J	PM747CK	PM1458Z	PM747CY	COM

*Also available with MIL-STD-883B processing. To order add /883 as a suffix to the part number.

†All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



TO-99 (J-Suffix)

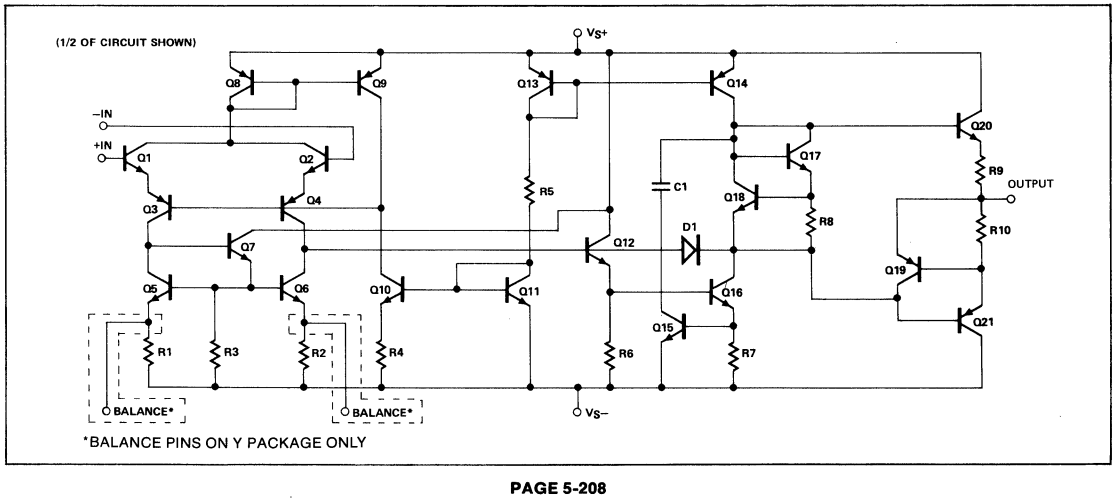
TO-100 (K-Suffix)

8-PIN HERMETIC DIP (Z-Suffix)

*V+ (A) AND V+ (B) INTERNALLY CONNECTED

14-PIN DIP (Y-Suffix)

SIMPLIFIED SCHEMATIC



*BALANCE PINS ON Y PACKAGE ONLY

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- PM747, PM1558 ..... ±22V
- PM747C, PM1458 ..... ±18V

Internal Power Dissipation (Note 1)
- J, K, and Z Packages 500mW
- Y Package 670mW

Differential Input Voltage ..... ±30V
Input Voltage ..... Supply Voltage
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Operating Temperature Range
- PM747, PM1558 ..... −55°C to +125°C
- PM747C, PM1458 ..... 0°C to +70°C

NOTE:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)/ TO-100 (K)	80°C	7.1mW/°C
14-Pin Hermetic DIP (Y)	83°C	10.0mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C

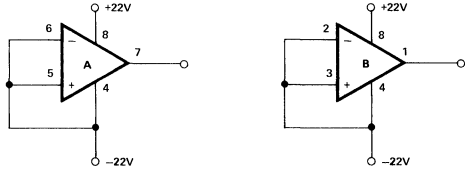
ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM747/PM1558 MIN	PM747/PM1558 TYP	PM747/PM1558 MAX	PM747C/PM1458 MIN	PM747C/PM1458 TYP	PM747C/PM1458 MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	1.0	5.0	—	1.0	6.0	mV
Input Offset Current	I_{OS}		—	20	200	—	20	200	nA
Input Bias Current	I_B		—	80	500	—	80	500	nA
Input Resistance	R_{IN}		0.3	2.0	—	0.3	2.0	—	MΩ
Input Capacitance	C_{IN}		—	1.4	—	—	1.4	—	pF
Offset Voltage Adjustment Range			—	±15	—	—	±15	—	mV
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	50	200	—	25	200	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10	±14 ±13	— —	±12 ±10	±14 ±13	— —	V
Output Resistance	R_O		—	75	—	—	75	—	Ω
Output Short Circuit Current	I_{SC}		—	25	—	—	25	—	mA
Supply Current	I_{SY}	Per Amplifier, No Load	—	1.7	2.8	—	1.7	2.8	mA
Input Voltage Range	IVR		±12	±13	—	±12	±13	—	V
Common Mode Rejection Ratio	CMRR	$R_S \leq 10k\Omega$, $V_{CM} = \pm 10V$	70	90	—	70	90	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $V_S = \pm 5V$ to $\pm 18V$	— —	30 —	150 —	— —	— 30	— 150	μV/V
Power Consumption	P_d	Per Amplifier, No Load	—	50	85	—	50	85	mW
Transient Response (Unity Gain)	Risetime Overshoot	$V_{IN} = 20mV$, $R_L = 2k\Omega$ $C_L \leq 100pF$	— —	0.3 5.0	— —	— —	0.3 5.0	— —	μs %
Slew Rate	SR	$R_L \leq 2k\Omega$	—	0.7	—	—	0.7	—	V/μs
Channel Separation	CS		—	120	—	—	120	—	dB

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ for PM747/PM1558, $0°C \leq T_A \leq +70°C$ for PM747C/PM1458, unless otherwise noted.

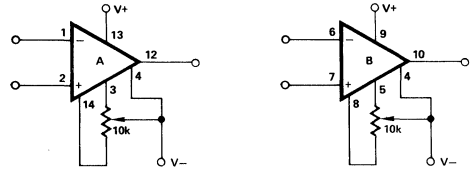
			PM747/PM1558			PM747C/PM1458			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	1.0	6.0	—	1.0	7.5	mV
Input Offset Current	I_{OS}	T_A = MAX T_A = MIN	— —	7.0 85	200 500	— —	7.0 30	200 300	nA
Input Bias Current	I_B	T_A = MAX T_A = MIN	— —	0.03 0.3	0.5 1.5	— —	0.03 0.10	0.5 0.8	μA
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10	±14 ±13	— —	±12 ±10	±14 ±13	— —	V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	25	50	—	15	25	—	V/mV
Input Voltage Range	IVR		±12	±13	—	±12	±13	—	V
Common Mode Rejection Ratio	CMRR	$R_S \leq 10k\Omega$, $V_{CM} = \pm 10V$	70	90	—	70	90	—	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 10k\Omega$ $V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 10k\Omega$ $V_S = \pm 5V$ to $\pm 18V$	— —	30 —	150 —	— —	— 30	— 150	μV/V
Supply Current	I_{SY}	T_A = MAX Per Amplifier T_A = MIN No Load	— —	1.5 2.0	2.5 3.3	— —	1.5 2.0	2.5 3.3	mA
Power Consumption	P_d	T_A = MAX Per Amplifier, T_A = MIN No Load	— —	45 60	75 100	— —	45 60	75 100	mW
Channel Separation	CS		—	120	—	—	120	—	dB

TYPICAL BURN-IN CIRCUIT *



*PINOUTS FOR J AND Z PACKAGES ONLY

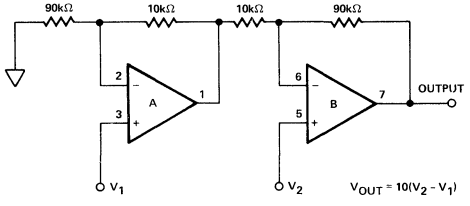
TYPICAL OFFSET NULLING CIRCUIT*



*PINOUTS FOR Y PACKAGE ONLY

TYPICAL APPLICATION

HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER*



*PINOUTS FOR J AND Z PACKAGES ONLY

PM4136

QUAD 741-TYPE OPERATIONAL AMPLIFIER

FEATURES

- RM4136/RC4136 Direct Replacements
- Low Noise
- Silicon-Nitride Passivation
- Internal Frequency Compensation
- Low Crossover Distortion
- Continuous Short-Circuit Protection
- Low Input Bias Current
- Low Input Offset Voltage

GENERAL DESCRIPTION

The PM4136 Series provides four 741-type operational amplifiers in a single 14-pin DIP package, pin compatible with the RM4136 and RC4136. Each of the four amplifiers has the proven OP-02 family advantages of low noise, low drift, and excellent long term stability. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process reduces "popcorn noise" and provides maximum reliability and long term stability of parameters for lowest overall system operating cost.

The PM4136 Series is ideal for use in designs requiring minimum space and cost while maintaining OP-02-type performance. PM4136's with processing per the requirements of MIL-STD-883B and MIL-M-38510 are available. For dual-741-type versions, see the OP-03/OP-04/OP-14 data sheet. For improved performance see the OP-09 data sheet.

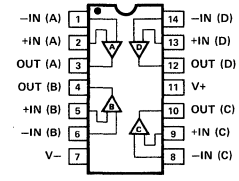
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (mV)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
5.0	PM4136Y*	MIL
6.0	PM4136CY	COM

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number.

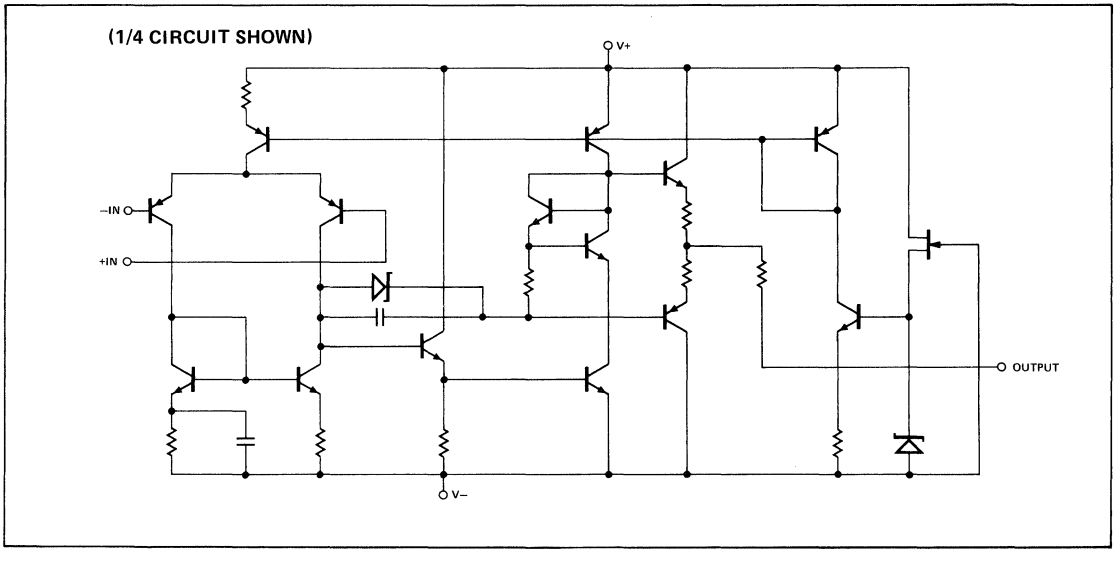
†All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



14-PIN HERMETIC DIP
(Y-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage, PM4136 ..... ±22V
Supply Voltage, PM4136C, PM4136GR ..... ±18V
Internal Power Dissipation (Note 1) 800mW
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±15V
Output Short Circuit Duration (Note 3) ..... Indefinite
Storage Temperature Range ..... −65°C to +150°C
DICE Junction Temperature (T_j) ..... −65°C to +150°C

Operating Temperature Range
PM4136 ..... −55°C to + 125°C
PM4136C ..... 0°C to +70°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C

NOTES:
1. Rating applies for ambient temperature of +25°C; derate linearly at 6.4mW/°C for ambient temperatures above +25°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be ground, one amplifier only. I_{SC} = 45mA (typical).
4. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS At T_A = +25°C and V_S = ±15V unless otherwise specified.

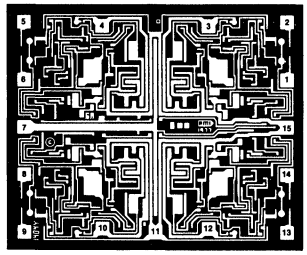
			PM4136			PM4136C			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	0.5	5.0	—	0.5	6.0	mV
Input Offset Current	I_{OS}		—	5.0	200	—	5.0	200	nA
Input Bias Current	I_B		—	40	500	—	40	500	nA
Input Resistance	R_{IN}	(Note 1)	0.3	5.0	—	0.3	5.0	—	MΩ
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	50,000	300,000	—	20,000	300,000	—	V/V
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12	±14	—	±12	±14	—	V
	V_O	$R_L \geq 2k\Omega$	±10	±13	—	±10	±13	—	V
Input Voltage Range	IVR		±12	±14	—	±12	±14	—	V
Common Mode Rejection Ratio	CMRR	$R_S \leq 10k\Omega$, V_{CM} = ± 12V	70	100	—	70	100	—	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 10k\Omega$, V_S = ±5V to ±15V	—	10	150	—	10	150	μV/V
Power Consumption (Four Amplifiers)	P_d	No load, V_{OUT} = 0	—	210	340	—	210	340	mW
Transient Response Risetime	t_r	V_{IN} = 20mV, R_L = 2kΩ, $C_L \leq 100pF$, A_{VCL} = + 1.0	—	0.13	—	—	0.13	—	μs
Transient Response Overshoot	OS	V_{IN} = 20mV, R_L = 2kΩ, $C_L \leq 100pF$, A_{VCL} = +1.0	—	5.0	—	—	5.0	—	%
Closed Loop Bandwidth	BW	A_{VCL} = + 1.0	—	3.0	—	—	3.0	—	MHz
Slew Rate	SR	$R_L \geq 2k\Omega$, A_{VCL} = + 1.0	—	1.5	—	—	1.0	—	V/μs
Channel Separation	CS	f = 10kHz, R_S = 1kΩ open loop	—	105	—	—	105	—	dB
Channel Separation (Gain-100)	CS	f = 10kHz, R_S = 1kΩ, A_{VCL} = 100	—	105	—	—	105	—	dB

ELECTRICAL CHARACTERISTICS At −55°C ≤ T_A ≤ +125°C for PM4136, 0°C ≤ T_A ≤ +70°C for PM4136C, and V_S = ±15V unless otherwise specified.

			PM4136			PM4136C			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	—	6.0	—	—	7.5	mV
Input Offset Current	I_{OS}		—	—	500	—	—	300	nA
Input Bias Current	I_B		—	—	1500	—	—	800	nA
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	25,000	—	—	15,000	—	—	V/V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±10	—	—	±10	—	—	V
Power Consumption	P_d	T_A = High, No load	—	180	300	—	180	300	mW
	P_d	T_A = Low, No load	—	240	400	—	240	400	mW

NOTE:
1. Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.085 × 0.070 inch

1. INVERTING INPUT (A)
2. NON-INVERTING INPUT (A)
3. OUTPUT (A)
4. OUTPUT (B)
5. NON-INVERTING INPUT (B)
6. INVERTING INPUT (B)
7. V-
8. INVERTING INPUT (C)
9. NON-INVERTING INPUT (C)
10. OUTPUT (C)
11. V + (CONNECTED INTERNALLY TO PAD 15)
12. OUTPUT (D)
13. NON-INVERTING INPUT (D)
14. INVERTING INPUT (D)
15. V + (CONNECTED INTERNALLY TO PIN 11)

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM4136GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	6.0	mV MAX
Input Offset Current	I_{OS}		200.0	nA MAX
Input Bias Current	I_B		500.0	nA MAX
Input Voltage Range	IVR		±12.0	V MIN
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V$, $R_S \leq 10k\Omega$	70.0	dB MIN
Power Supply Rejection Ratio	PSRR	$R_S \leq 10k\Omega$, $V_S = \pm 5V$ to $\pm 15V$	150.0	μV/V MAX
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12.0 ± 10.0	V MIN
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	20,000	V/V MIN
Power Consumption (Four Amplifiers)	P_d	$V_{OUT} = 0$ No Load	340	mW MAX

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM4136GR TYPICAL	UNITS
Slew Rate	SR	$A_{VCL} = +1.0$ $R_L \geq 2k\Omega$	1.5	V/μs
Closed Loop Bandwidth	BW	$A_{VCL} = +1.0$	3.0	MHz
Channel Separation	CS	$A_{VCL} = 100$ f = 10kHz $R_S = 1k\Omega$	105	dB

NOTE:
Either or both V+ pads may be used without any change in performance.

JM38510/10104

JAN SINGLE LOW INPUT CURRENT OPERATIONAL AMPLIFIER — EXTERNALLY COMPENSATED

GENERAL DESCRIPTION

This data sheet covers the electrical requirements for a monolithic, low input current externally compensated operational amplifier as specified in MIL-M-38510/101 for device type 04. Devices supplied to this data sheet are manufactured and tested at PMI's MIL-M-38510 certified facility and are listed in QPL-38510.

Complete device requirements will be found in MIL-M-38510 and MIL-M-38510/101 for Class B processed devices.

GENERIC CROSS-REFERENCE INFORMATION

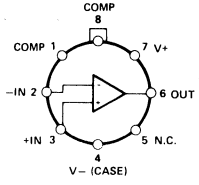
This cross-reference information is presented for the convenience of the user. The generic-industry types listed may not have identical operational performance characteristics across the military temperature range or reliability factors equivalent to the MIL-M-38510 device.

Military Device Type	Generic-Industry Type
04	LM108A

CASE OUTLINE

Per MIL-M-38510, Appendix C, Case Outline A-1 (8 Lead Can). Package Type Designator "G".

PIN CONNECTIONS AND ORDERING INFORMATION



TO-99 (J-Suffix)

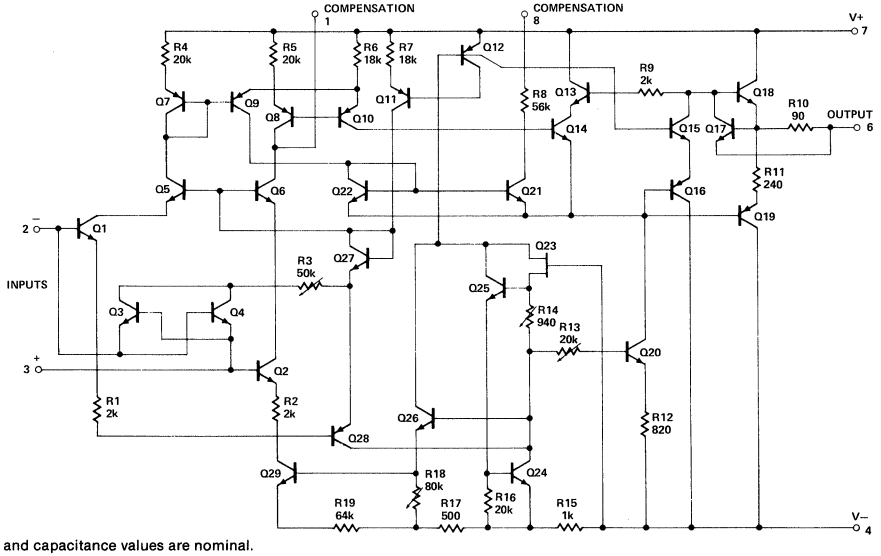
Jan Device	PMI Device Type
JM38510/10104BGC	PM108AJ1/38510

NOTE: Lead Finish: Gold Plate.
Check with factory for other qualified lead finishes.

POWER AND THERMAL CHARACTERISTICS

Package	Case outline	Maximum allowable power dissipation	Maximum θJ—C	Maximum θJ—A
8 Lead Can (TO-99)	G	330mW at $T_A = 125°C$	40° C/W	150° C/W

SIMPLIFIED SCHEMATIC



NOTE:
1. All resistance and capacitance values are nominal.

ELECTRICAL CHARACTERISTICS at $5V \leq \pm V_{CC} \leq 20V$ and $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input Offset Voltage	V_{IO}	(Note 2) $T_A = 25°C$ $R_S = 50\Omega$ $-55°C \leq T_A \leq 125°C$	−0.5 −1.0	+0.5 +1.0	mV
Input Offset Voltage Temperature Sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	ΔT_A from −55°C to +25°C ΔT_A from +25°C to +125°C	−5.0 −5.0	+5.0 +5.0	µV/°C
Input Offset Current	I_{IO}	(Note 2) $T_A = 25°C$ $-55°C \leq T_A \leq 125°C$	−0.2 −0.4	+0.2 +0.4	nA
Input Offset Current Temperature Sensitivity	$\frac{\Delta I_{IO}}{\Delta T}$	ΔT_A from −55°C to +25°C ΔT_A from +25°C to +125°C	−2.5 −2.5	+2.5 +2.5	pA/°C
Input Bias Current	$+I_{IB}$	(Note 2) $25°C \leq T_A \leq 125°C$ $-55°C \leq T_A \leq +25°C$	−0.1 −0.1	+2.0 +3.0	nA
	$-I_{IB}$	(Note 2) $25°C \leq T_A \leq 125°C$ $-55°C \leq T_A \leq +25°C$	−0.1 −0.1	+2.0 +3.0	nA
Power Supply Rejection Ratio	+PSRR	$+V_{CC} = 10V$ $R_S = 50\Omega$ $T_A = 25°C$ $-V_{CC} = 20V$ $-55°C \leq T_A 125°C$	−16 −16	+16 +16	µV/V
Power Supply Rejection Ratio	−PSRR	$+V_{CC} = 20V$ $R_S = 50\Omega$ $T_A = 25°C$ $-V_{CC} = -10V$ $-55°C \leq T_A \leq 125°C$	−16 −16	+16 +16	µV/V
Input Voltage Common Mode Rejection	CMR	$\pm V_{CC} = 20V$ $V_{IN} = \pm 15V$ $R_S = 50\Omega$	96	—	dB
Adjustment For Input Offset Voltage	V_{IO} ADJ (+)	$\pm V_{CC} = 20V$	No External Adjustment		mV
Adjustment For Input Offset Voltage	V_{IO} ADJ (−)	$\pm V_{CC} = 20V$	No External ADJ.		mV
Output Short Circuit Current (For Positive Output)	$I_{OS(+)}$	$\pm V_{CC} = 15V$ $t \leq 25mS$ (Note 3)	15	—	mA
Output Short Circuit Current (For Negative Output)	$I_{OS(-)}$	$\pm V_{CC} = 15V$ $t \leq 25mS$ (Note 3)	—	15	mA
Supply Current	I_{CC}	$\pm V_{CC} = 15V$ $T_A = -55°C$ $T_A = +25°C$ $T_A = +125°C$	— — —	0.8 0.6 0.6	mA
Output Voltage Swing (Maximum)	V_{OP}	$\pm V_{CC} = 20V$, $R_L = 10k\Omega$ $\pm V_{CC} = 20V$, $R_L = 2k\Omega$	±16 —	— —	V
Open Loop Voltage Gain (Single Ended) (Note 1)	$A_{VS(\pm)}$	$\pm V_{CC} = 20V$ $R_L = 10k\Omega$ $T_A = 25°C$ $V_{OUT} = \pm 15V$ $-55°C \leq T_A \leq 125°C$	80 40	— —	V/mV
Open Loop Voltage Gain (Single Ended) (Note 1)	A_{VS}	$\pm V_{CC} = 5V$ $R_L = 10k\Omega$ $V_{OUT} = \pm 2V$	20	—	V/mV
Transient Response Rise Time	$TR_{(tr)}$	$C_F = 10pF$	—	1000	nsec
Transient Response Overshoot	$TR_{(OS)}$	$C_F = 10pF$	—	50	%
Noise (Referred to Input) Broadband	N_I (BB)	$\pm V_{CC} = 20V$ Bandwidth = 5kHz $T_A = 25°C$	—	15	µV rms
Noise (Referred to Input) Popcorn	N_I (PC)	$\pm V_{CC} = 20V$ Bandwidth = 5kHz $T_A = 25°C$	—	40	µV peak

NOTES:

1. Note that gain is not specified at $V_{IO(ADJ)}$ extremes. Some gain reduction is usually seen at $V_{IO(ADJ)}$ extremes. For closed loop applications (closed loop gain less than 1,000), the open loop tests (A_{VS}) prescribed herein should guarantee a positive, reasonably linear, transfer characteristic. They do not, however, guarantee that the open loop gain is linear, or even positive, over the operating range. If either of these requirements exist (positive open loop gain or open loop gain linearity). they should be specified in the individual procurement document as additional requirements.
2. Tests at common mode $V_{CM} = 0$, $V_{CM} = -15V$, and $V_{CM} = +15V$.
3. Continuous short circuit limits will be considerably less than the indicated test limits. Continuous I_{OS} at $T_A \leq 75°C$ will cause T_j to exceed the maximum of 175°C. For dual devices, I_{OS} is measured one channel at a time.

ELECTRICAL CHARACTERISTICS at $5V \leq \pm V_{CC} \leq 20V$ and $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Slew Rate	SR (+)	$A_V = 1$ $-55°C \leq T_A \leq 25°C$ $V_{IN} = +5V$ $T_A = 125°C$	0.05 0.05	— —	V/μsec
Slew Rate	SR (−)	$A_V = 1$ $-55°C \leq T_A \leq 25°C$ $V_{IN} = \pm 5V$ $T_A = 125°C$	0.05 0.05	— —	V/μsec
Settling Time	t_S (+)	$T_A = 25°C$ $-55°C \leq T_A \leq 125°C$	— —	— —	ns
	t_S (−)	$T_A = 25°C$ $-55°C \leq T_A \leq 125°C$	— —	— —	ns

NOTES:

1. Note that gain is not specified at $V_{IO\ (ADJ)}$ extremes. Some gain reduction is usually seen at $V_{IO\ (ADJ)}$ extremes. For closed loop applications (closed loop gain less than 1,000), the open loop tests (A_{VS}) prescribed herein should guarantee a positive, reasonably linear, transfer characteristic. They do not, however, guarantee that the open loop gain is linear, or even positive, over the operating range. If either of these requirements exist (positive open loop gain or open loop gain linearity). they should be specified in the individual procurement document as additional requirements.
2. Tests at common mode $V_{CM} = 0$, $V_{CM} = -15V$, and $V_{CM} = +15V$.
3. Continuous short circuit limits will be considerably less than the indicated test limits. Continuous I_{OS} at $T_A \leq 75°C$ will cause T_j to exceed the maximum of 175° C. For dual devices, I_{OS} is measured one channel at a time.

For Test Circuit Diagrams See MIL-M-38510/101

JM38510/10106

JAN DUAL LOW INPUT CURRENT OPERATIONAL AMPLIFIER — EXTERNALLY COMPENSATED

GENERAL DESCRIPTION

This data sheet covers the electrical requirements for a dual low input current externally compensated operational amplifier as specified in MIL-M-38510/101 for device type 06.

Devices supplied to this data sheet are manufactured and tested at PMI's MIL-M-38510 certified facility and are listed in QPL-38510.

Complete device requirements will be found in MIL-M-38510 and MIL-M-38510/101 for Class B processed devices.

GENERIC CROSS-REFERENCE INFORMATION

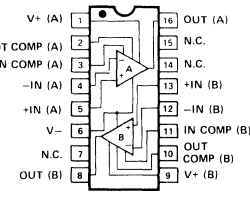
This cross-reference information is presented for the convenience of the user. The generic-industry types listed may not have identical operational performance characteristics across the military temperature range or reliability factors equivalent to the MIL-M-38510 device.

Military Device Type	Generic-Industry Type
06	LM2108A

CASE OUTLINE

Per MIL-M-38510, Appendix C, Case Outline D-2 (16-pin DIP). Package Type Designator "E".

PIN CONNECTIONS AND ORDERING INFORMATION



16 PIN HERMETIC DIP
(Q-Suffix)

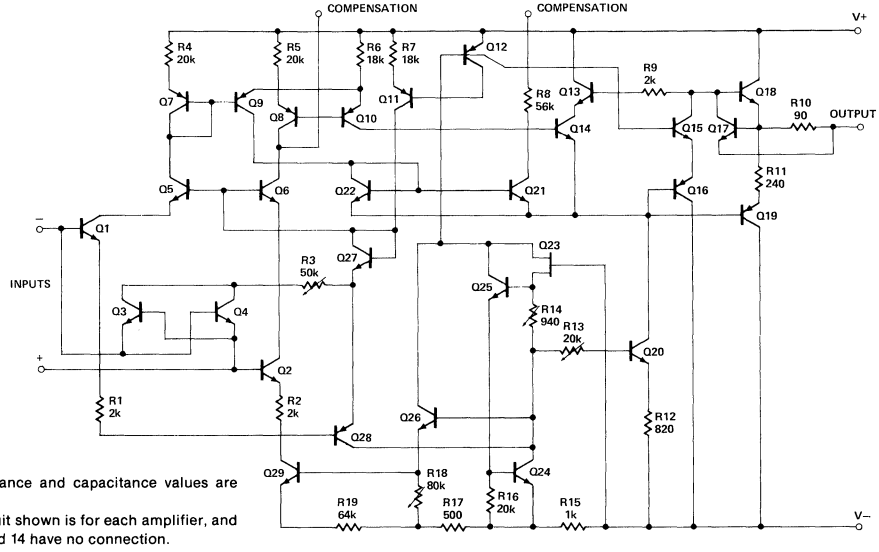
Jan Device	PMI Device Type
JM38510/10106BEB	PM2108AQ2/38510

Note: Lead Finishe: Acid Tin Plate
Check with factory for other qualified lead finishes.

POWER AND THERMAL CHARACTERISTICS

Package	Case outline	Maximum allowable power dissipation	Maximum θJ—C	Maximum θJ—A
Dual-in-line	E	400mW at T_A = 125° C	35° C/W	120° C/W

SIMPLIFIED SCHEMATIC



NOTES:
1. All resistance and capacitance values are nominal.
2. The circuit shown is for each amplifier, and pins 7 and 14 have no connection.

ELECTRICAL CHARACTERISTICS at $5V \leq \pm V_{CC} \leq 20V$ and $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input Offset Voltage	V_{IO}	(Note 2) $T_A = 25°C$ $R_S = 50\Omega$ $-55°C \leq T_A \leq 125°C$	−0.5 −1.0	+0.5 +1.0	mV
Input Offset Voltage Temperature Sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	ΔT_A from −55°C to +25°C ΔT_A from +25°C to +125°C	−5.0 −5.0	+5.0 +5.0	µV/°C
Input Offset Current	I_{IO}	(Note 2) $T_A = 25°C$ $-55°C \leq T_A \leq 125°C$	−0.2 −0.4	+0.2 +0.4	nA
Input Offset Current Temperature Sensitivity	$\frac{\Delta I_{IO}}{\Delta T}$	ΔT_A from −55°C to +25°C ΔT_A from +25°C to +125°C	−2.5 −2.5	+2.5 +2.5	pA/°C
Input Bias Current	$+I_{IB}$	(Note 2) $25°C \leq T_A \leq 125°C$ $-55°C \leq T_A \leq +25°C$	−0.1 −0.1	+2.0 +3.0	nA
	$-I_{IB}$	(Note 2) $25°C \leq T_A \leq 125°C$ $-55°C \leq T_A \leq +25°C$	−0.1 −0.1	+2.0 +3.0	nA
Power Supply Rejection Ratio	+PSRR	$+V_{CC} = 10V$ $R_S = 50\Omega$ $T_A = 25°C$ $-V_{CC} = 20V$ $-55°C \leq T_A 125°C$	−16 −16	+16 +16	µV/V
Power Supply Rejection Ratio	−PSRR	$+V_{CC} = 20V$ $R_S = 50\Omega$ $T_A = 25°C$ $-V_{CC} = -10V$ $-55°C \leq T_A \leq 125°C$	−16 −16	+16 +16	µV/V
Input Voltage Common Mode Rejection	CMR	$\pm V_{CC} = 20V$ $V_{IN} = \pm 15V$ $R_S = 50\Omega$	96	—	dB
Adjustment For Input Offset Voltage	V_{IO} ADJ (+)	$\pm V_{CC} = 20V$	No External Adjustment		mV
Adjustment For Input Offset Voltage	V_{IO} ADJ (−)	$\pm V_{CC} = 20V$	No External Adjustment		mV
Output Short Circuit Current (For Positive Output)	$I_{OS(+)}$	$\pm V_{CC} = 15V$ $t \leq 25mS$ (Note 3)	15	—	mA
Output Short Circuit Current (For Negative Output)	$I_{OS(-)}$	$\pm V_{CC} = 15V$ $t \leq 25mS$ (Note 3)	—	15	mA
Supply Current	I_{CC}	$\pm V_{CC} = 15V$ $T_A = -55°C$ $T_A = +25°C$ $T_A = +125°C$	— — —	0.8 0.6 0.6	mA
Output Voltage Swing (Maximum)	V_{OP}	$\pm V_{CC} = 20V$, $R_L = 10k\Omega$ $\pm V_{CC} = 20V$, $R_L = 2k\Omega$	±16 —	— —	V
Open Loop Voltage Gain (Single Ended) (Note 1)	$A_{VS(\pm)}$	$\pm V_{CC} = 20V$ $R_L = 10k\Omega$ $T_A = 25°C$ $V_{OUT} = \pm 15V$ $-55°C \leq T_A \leq 125°C$	80 40	— —	V/mV
Open Loop Voltage Gain (Single Ended) (Note 1)	A_{VS}	$\pm V_{CC} = 5V$ $R_L = 10k\Omega$ $V_{OUT} = \pm 2V$	20	—	V/mV
Transient Response Rise Time	$TR_{(tr)}$	$C_F = 10pF$	—	1000	nsec
Transient Response Overshoot	$TR_{(OS)}$	$C_F = 10pF$	—	50	%
Noise (Referred to Input) Broadband	N_I (BB)	$\pm V_{CC} = 20V$ Bandwidth = 5kHz $T_A = 25°C$	—	15	µV rms
Noise (Referred to Input) Popcorn	N_I (PC)	$\pm V_{CC} = 20V$ Bandwidth = 5kHz $T_A = 25°C$	—	40	µV peak

NOTES:

1. Note that gain is not specified at $V_{IO(ADJ)}$ extremes. Some gain reduction is usually seen at $V_{IO(ADJ)}$ extremes. For closed loop applications (closed loop gain less than 1,000), the open loop tests (A_{VS}) prescribed herein should guarantee a positive, reasonably linear, transfer characteristic. They do not, however, guarantee that the open loop gain is linear, or even positive, over the operating range. If either of these requirements exist (positive open loop gain or open loop gain linearity). they should be specified in the individual procurement document as additional requirements.
2. Tests at common mode $V_{CM} = 0$, $V_{CM} = -15V$, and $V_{CM} = +15V$.
3. Continuous short circuit limits will be considerably less than the indicated test limits. Continuous I_{OS} at $T_A \leq 75°C$ will cause T_j to exceed the maximum of 175°C. For dual devices, I_{OS} is measured one channel at a time.

ELECTRICAL CHARACTERISTICS at $5V \leq \pm V_{CC} \leq 20V$ and $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Slew Rate	SR (+)	$A_V = 1$ $-55°C \leq T_A \leq 25°C$ $V_{IN} = +5V$ $T_A = 125°C$	0.05 0.05	— —	V/μsec
Slew Rate	SR (−)	$A_V = 1$ $-55°C \leq T_A \leq 25°C$ $V_{IN} = \pm 5V$ $T_A = 125°C$	0.05 0.05	— —	V/μsec
Settling Time	t_S (+)	$T_A = 25°C$ $-55°C \leq T_A \leq 125°C$	— —	— —	ns
	t_S (−)	$T_A = 25°C$ $-55°C \leq T_A \leq 125°C$	— —	— —	ns
Channel Separation	CS	$\pm V_{CC} = 20V$ $T_A = 25°C$	80	—	dB

NOTES:

1. Note that gain is not specified at $V_{IO\,(ADJ)}$ extremes. Some gain reduction is usually seen at $V_{IO\,(ADJ)}$ extremes. For closed loop applications (closed loop gain less than 1,000), the open loop tests (A_{VS}) prescribed herein should guarantee a positive, reasonably linear, transfer characteristic. They do not, however, guarantee that the open loop gain is linear, or even positive, over the operating range. If either of these requirements exist (positive open loop gain or open loop gain linearity). they should be specified in the individual procurement document as additional requirements.
2. Tests at common mode $V_{CM} = 0$, $V_{CM} = -15V$, and $V_{CM} = +15V$.
3. Continuous short circuit limits will be considerably less than the indicated test limits. Continuous I_{OS} at $T_A \leq 75°C$ will cause T_j to exceed the maximum of 175° C. For dual devices, I_{OS} is measured one channel at a time.

For Test Circuit Diagrams See MIL-M-38510/101

JM38510/11401/11402/ 11403/11404/11405/11406

JAN JFET INPUT OPERATIONAL AMPLIFIERS

GENERAL DESCRIPTION

This data sheet covers the electrical requirements for a monolithic, low-power, internally compensated BIFET operational amplifier as specified in MIL-M-38510/114 for device types 01 to 06. Devices supplied to this data sheet are manufactured and tested at PMI's MIL-M-38510 certified facility and are listed in QPL-38510.

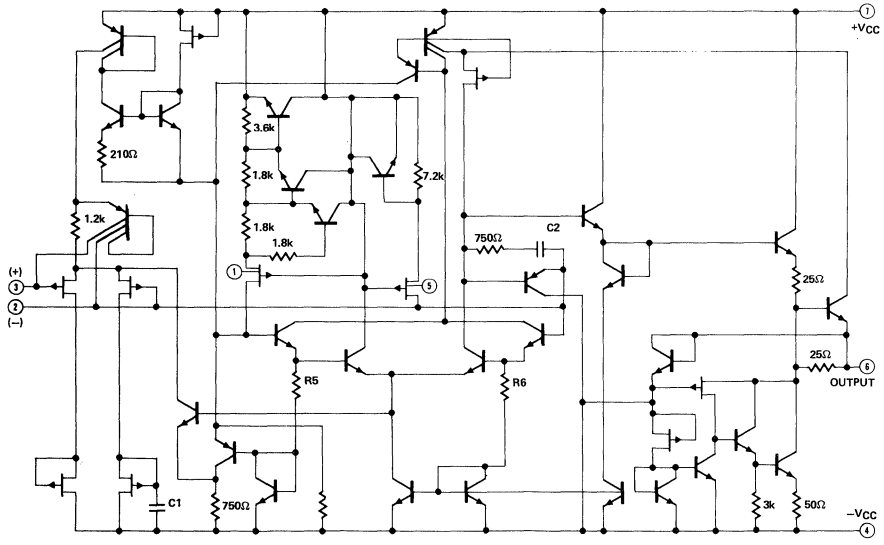
Complete device requirements will be found in MIL-M-38510 and MIL-M-38510/114 for Class B processed devices.

GENERIC CROSS-REFERENCE INFORMATION

This cross-reference information is presented for the convenience of the user. The generic-industry types listed may not have identical operational performance characteristics across the military temperature range or reliability factors equivalent to the MIL-M-38510 device.

Military Device Type	Generic-Industry Type
01	LF-155
04	LF-155A
02	LF-156
05	LF-156A
03	LF-157
06	LF-157A

SIMPLIFIED SCHEMATIC



NOTE: For values of C1, C2, R5, R6 see the following table:

	01/04	02/05	03/06
C1	7pF	5pF	1.7pF
C2	7pF	5pF	1.7pF
R5	7.2kΩ	3.6kΩ	3.6kΩ
R6	7.2kΩ	3.6kΩ	3.6kΩ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range ..... ±22V
Input Voltage Range (Note 1) ..... ±20V
Differential Input Voltage Range ..... ±40V

Lead Temperature (Soldering, 60 sec.) ..... 300°C
Junction Temperature ..... T_J = 175°C (Note 3)
Storage Temperature Range ..... −65°C to +150°C
Output Short-Circuit Duration ..... Unlimited (Note 2)

NOTES:
1. The absolute maximum negative input voltage is equal to the negative power supply voltage.
2. Short circuit may be to ground to either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
3. For short-term test (in the specific burn-in and life test configuration when required and up to 168 hours maximum), T_J = 275°C.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... ±5 to ±20 VDC

Ambient Temperature Range ..... −55°C to +125°C

ELECTRICAL CHARACTERISTICS at V_{CC} from ±5V to ±20V; source resistance = 50 ohm; ambient temperature range = −55°C to +125°C and figure 1, unless otherwise noted.

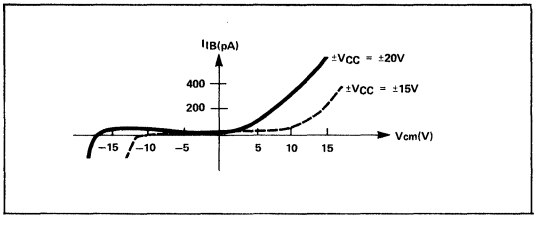
PARAMETER	SYMBOL	CONDITIONS	01 LIMITS MIN	01 LIMITS MAX	04 LIMITS MIN	04 LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	$\pm V_{CC}$ = ±5V, V_{CM} = 0V, T_A = 25°C	−5	5	−2	2	mV
		$\pm V_{CC}$ = ±20V, V_{CM} = ±15V, 0V, −55°C ≤ T_A ≤ +125°C	−7	7	−2.5	2.5	
Input Offset Voltage Temperature Sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	$\pm V_{CC}$ = ±20V, V_{CM} = 0V	−30	30	−10	10	µV/°C
Input Offset Current	I_{IO}	$\pm V_{CC}$ = ±20V, V_{CM} = 0V, T_J = 25°C	−20	20	−20	20	pA
		T_J = 125°C	−20	20	−20	20	nA
Input Bias Current (Note 1) (Note 2) (Note 3)	$+I_{IB}$	$\pm V_{CC}$ = ±20V, V_{CM} = +15V, T_j = 25°C	−100	3500	−100	3500	pA
		t ≤ 25ms T_j = 125°C	−10	60	−10	60	nA
	$-I_{IB}$	$\pm V_{CC}$ = ±15V, V_{CM} = +10V, T_j = 25°C	−100	300	−100	300	pA
		t ≤ 25ms T_j = 125°C	−10	50	−10	50	nA
		$\pm V_{CC}$ = ±20V, −15V ≤ V_{CM} ≤ 0V, T_j = 25°C	−100	100	−100	100	pA
		t ≤ 25ms T_j = 125°C	−10	50	−10	50	nA
Power Supply Rejection Ratio	+PSRR	$+V_{CC}$ = 10V, $-V_{CC}$ = −20V	85	—	85	—	dB
	−PSRR	$+V_{CC}$ = 20V, $-V_{CC}$ = −10V					
Input Voltage Common Mode Rejection (Note 4)	CMR	$\pm V_{CC}$ = ±20V, V_{IN} = ±15V	85	—	85	—	dB
Adjustment for Input Offset Voltage	V_{IO} ADJ(+)	$\pm V_{CC}$ = ±20V	+8	—	+8	—	mV
	V_{IO} ADJ(−)	$\pm V_{CC}$ = ±20V	—	−8	—	−8	
Output Short Circuit Current (for Positive Output) (Note 5)	$I_{OS(+)}$	$\pm V_{CC}$ = ±15V, t ≤ 25ms (Short Circuit to Ground)	−50	—	−50	—	mA
Output Short Circuit Current (for Negative Output) (Note 5)	$I_{OS(-)}$	$\pm V_{CC}$ = ±15V, t ≤ 25ms (Short Circuit to Ground)	—	50	—	50	mA
Supply Current	I_{CC}	T_A = −55°C	—	6	—	6	mA
		$\pm V_{CC}$ = ±15V, T_A = +25°C	—	4	—	4	
		T_A = +125°C	—	4	—	4	
Output Voltage Swing (Maximum)	V_{OP}	$\pm V_{CC}$ = ±20V, R_L = 10kΩ	±16	—	±16	—	V
		$\pm V_{CC}$ = ±20V, R_L = 2kΩ	±15	—	±15	—	
Open Loop Voltage Gain (Single Ended) (Note 6)	$A_{VS(+)}$	$\pm V_{CC}$ = ±20V, V_{OUT} = ±15V, R_L = 2kΩ, T_A = 25°C	50	—	50	—	V/mV
	$A_{VS(-)}$	−55°C ≤ T_A ≤ +125°C	25	—	25	—	
Open Loop Voltage Gain (Single Ended) (Note 6)	A_{VS}	$\pm V_{CC}$ = ±5V, R_L = 2kΩ, V_{OUT} = ±2V	10	—	10	—	V/mV

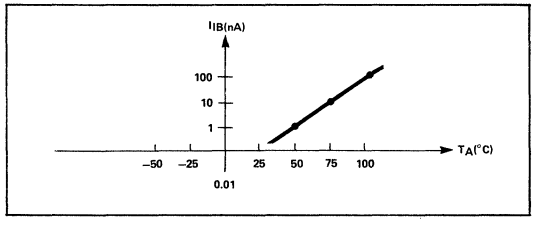
ELECTRICAL CHARACTERISTICS at V_{CC} from ±5V to ±20V; source resistance = 50 ohm; ambient temperature range = −55°C to +125°C and figure 1, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	01 LIMITS MIN	01 LIMITS MAX	04 LIMITS MIN	04 LIMITS MAX	UNITS
Transient Response Rise Time	$TR_{(tr)}$	$\pm V_{CC}$ = ±15V, R_L = 2kΩ, AV = 1 C_L = 100pF, See Figure 2 V_{IN} = 50mV	—	150	—	150	ns
Transient Response Overshoot	$TR_{(os)}$	$\pm V_{CC}$ = ±15V, R_L = 2kΩ, AV = 1 C_L = 100pF, See Figure 2 V_{IN} = 50mV	—	40	—	40	%
Slew Rate	SR(+) and SR(−)	V_{IN} = ±5V, $\pm V_{CC}$ = ±15V AV = 1, See Figure 2 T_A = 25°C T_A = −55°C, +125°C	2 1	— —	3 1.5	— —	V/μs
Settling Time	ts(+) and ts(−)	$\pm V_{CC}$ = ±15V (0.1% error) T_A = 25°C AV = −1 See Figure 3	—	1500	—	1500	ns
Noise (Referred to Input) Broadband	$N_{I(BB)}$	$\pm V_{CC}$ = 20V, T_A = 25°C Bandwidth = 5kHz	—	10	—	10	μV_{rms}
Noise (Referred to Input) Popcorn	$N_{I(PC)}$	IV_{CC} = 20V, T_A = 25°C Bandwidth = 5kHz	—	80	—	80	μV_{pk}

NOTES:

1. Bias currents are actually junction leakage currents which double (approximately) for each 10°C increase in junction temperature T_J. Measurement of bias current is specified at T_J rather than T_A, since normal warmup thermal transients will affect the bias currents. The measurements for bias currents must be made within 25ms after power is first applied to the device for test. Measurement at T_A = −55°C is not necessary since expected values are too small for typical test systems.
2. Bias current is sensitive to power supply voltage, common mode voltage and temperature as shown by the following typical curves:





3. Negative I_{IB} minimum limits reflect the characteristics of devices with bias current compensation.
4. CMR is calculated from V_{IO} measurements at V_{CM} = +15V and −15V.
5. Continuous limits shall be considerably lower. Protection for shorts to either supply exists providing that $T_J(max) \leq 175°C$.
6. Because of thermal feedback effects from output to input, open loop gain is not guaranteed to be linear or positive over the operating range. These requirements, if needed, should be specified by the user in additional procurement documents.

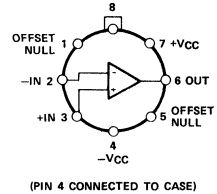
CASE OUTLINE

Per MIL-M-38510, Appendix C, Case Outline A-1 (8 Lead Can). Package Type Designator "G".

POWER AND THERMAL CHARACTERISTICS

Package	Case outline	Maximum allowable power dissipation	Maximum ΘJ — C	Maximum ΘJ — A
8 Lead Can (TO-99)	G	330mW at T_A = 125°C	40°C/W	150°C/W

PIN CONNECTIONS & ORDERING INFORMATION



(PIN 4 CONNECTED TO CASE)

Jan Device	PMI Device Type
JM38510/11401BGC	PM155J1/38510
JM38510/11404BGC	PM155AJ1/38510
JM38510/11402BGC	PM156J1/38510
JM38510/11405BGC	PM156AJ1/38510
JM38510/11403BGC	PM157J1/38510
JM38510/11406BGC	PM157AJ1/38510

Note: Lead Finish-Gold Plate.
Check with factory for other qualified lead finishes.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range ..... ±22V
Input Voltage Range (Note 1) ..... ±20V
Differential Input Voltage Range ..... ±40V

Lead Temperature (Soldering, 60 sec.) ..... 300°C
Junction Temperature ..... T_J = 175°C (Note 3)
Storage Temperature Range ..... −65°C to +150°C
Output Short-Circuit Duration ..... Unlimited (Note 2)

NOTES:
1. The absolute maximum negative input voltage is equal to the negative power supply voltage.
2. Short circuit may be to ground to either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
3. For short-term test (in the specific burn-in and life test configuration when required and up to 168 hours maximum), T_J = 275°C.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... ±5 to ±20 VDC

Ambient Temperature Range ..... −55°C to +125°C

ELECTRICAL CHARACTERISTICS at V_{CC} from ±5V to ±20V; source resistance = 50 ohm; ambient temperature range = −55°C to +125°C and figure 1, unless otherwise noted.

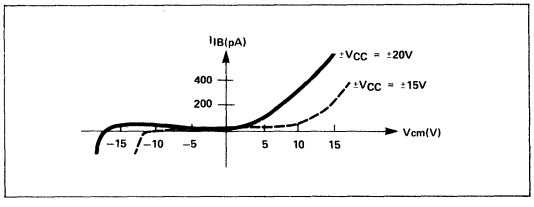
PARAMETER	SYMBOL	CONDITIONS	02 LIMITS MIN	02 LIMITS MAX	05 LIMITS MIN	05 LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	$\pm V_{CC}$ = ±5V, V_{CM} = 0V, T_A = 25°C	−5	5	−2	2	mV
		$\pm V_{CC}$ = ±20V, V_{CM} = ±15V, 0V, −55°C ≤ T_A ≤ +125°C	−7	7	−2.5	2.5	
Input Offset Voltage Temperature Sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	$\pm V_{CC}$ = ±20V, V_{CM} = 0V	−30	30	−10	10	µV/°C
Input Offset Current	I_{IO}	$\pm V_{CC}$ = ±20V, V_{CM} = 0V, T_J = 25°C	−20	20	−20	20	pA
		T_J = 125°C	−20	20	−20	20	nA
Input Bias Current (Note 1)	$+I_{IB}$	$\pm V_{CC}$ = ±20V, V_{CM} = +15V, T_j = 25°C	−100	3500	−100	3500	pA
		t ≤ 25ms T_j = 125°C	−10	60	−10	60	nA
	$-I_{IB}$	$\pm V_{CC}$ = ±15V, V_{CM} = +10V, T_j = 25°C	−100	300	−100	300	pA
		t ≤ 25ms T_j = 125°C	−10	50	−10	50	nA
(Note 2)		$\pm V_{CC}$ = ±20V, −15V ≤ V_{CM} ≤ 0V, T_j = 25°C	−100	100	−100	100	pA
(Note 3)		t ≤ 25ms T_j = 125°C	−10	50	−10	50	nA
Power Supply Rejection Ratio	+PSRR	+V_{CC} = 10V, −V_{CC} = −20V	85	—	85	—	dB
	−PSRR	+V_{CC} = 20V, −V_{CC} = −10V					
Input Voltage Common Mode Rejection (Note 4)	CMR	$\pm V_{CC}$ = ±20V, V_{IN} = ±15V	85	—	85	—	dB
Adjustment for Input Offset Voltage	V_{IO} ADJ(+)	$\pm V_{CC}$ = ±20V	+8	—	+8	—	mV
	V_{IO} ADJ(−)	$\pm V_{CC}$ = ±20V	—	−8	—	−8	
Output Short Circuit Current (for Positive Output) (Note 5)	$I_{OS(+)}$	$\pm V_{CC}$ = ±15V, t ≤ 25ms (Short Circuit to Ground)	−50	—	−50	—	mA
Output Short Circuit Current (for Negative Output) (Note 5)	$I_{OS(-)}$	$\pm V_{CC}$ = ±15V, t ≤ 25ms (Short Circuit to Ground)	—	50	—	50	mA
Supply Current	I_{CC}	T_A = −55°C	—	11	—	11	mA
		$\pm V_{CC}$ = ±15V, T_A = +25°C	—	7	—	7	
		T_A = +125°C	—	7	—	7	
Output Voltage Swing (Maximum)	V_{OP}	$\pm V_{CC}$ = ±20V, R_L = 10kΩ	±16	—	±16	—	V
		$\pm V_{CC}$ = ±20V, R_L = 2kΩ	±15	—	±15	—	
Open Loop Voltage Gain (Single Ended) (Note 6)	$A_{VS(+)}$	$\pm V_{CC}$ = ±20V, V_{OUT} = ±15V, R_L = 2kΩ, T_A = 25°C	50	—	50	—	V/mV
	$A_{VS(-)}$	−55°C ≤ T_A ≤ +125°C	25	—	25	—	
Open Loop Voltage Gain (Single Ended) (Note 6)	A_{VS}	$\pm V_{CC}$ = ±5V, R_L = 2kΩ, V_{OUT} = ±2V	10	—	10	—	V/mV

ELECTRICAL CHARACTERISTICS at V_{CC} from ±5V to ±20V; source resistance = 50 ohm; ambient temperature range = −55°C to +125°C and figure 1, unless otherwise noted.

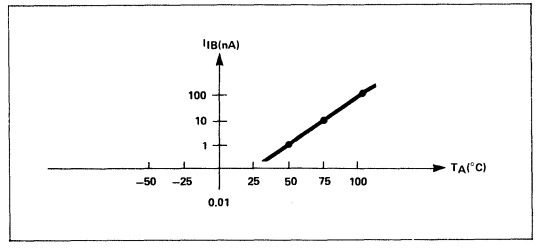
PARAMETER	SYMBOL	CONDITIONS	02 LIMITS MIN	02 LIMITS MAX	05 LIMITS MIN	05 LIMITS MAX	UNITS
Transient Response Rise Time	$TR_{(tr)}$	$\pm V_{CC} = \pm 15V$, $R_L = 2k\Omega$, AV = 1 $C_L = 100pF$, See Figure 2 $V_{IN} = 50mV$	—	100	—	100	ns
Transient Response Overshoot	$TR_{(os)}$	$\pm V_{CC} = \pm 15V$, $R_L = 2k\Omega$, AV = 1 $C_L = 100pF$, See Figure 2 $V_{IN} = 50mV$	—	40	—	40	%
Slew Rate	SR(+) and SR(−)	$V_{IN} = \pm 5V$, $\pm V_{CC} = \pm 15V$ AV = 1, See Figure 2 $T_A = 25°C$ $T_A = -55°C, +125°C$	7.5 5	— —	10 7	— —	V/μs
Settling Time	ts(+) and ts(−)	$\pm V_{CC} = \pm 15V$ (0.1% error) $T_A = 25°C$ AV = −1 See Figure 3	—	1500	—	1500	ns
Noise (Referred to Input) Broadband	$N_I(BB)$	$\pm V_{CC} = 20V$, $T_A = 25°C$ Bandwidth = 5kHz	—	10	—	10	μV_{rms}
Noise (Referred to Input) Popcorn	$N_I(PC)$	$IV_{CC} = 20V$, $T_A = 25°C$ Bandwidth = 5kHz	—	80	—	80	μV_{pk}

NOTES:

1. Bias currents are actually junction leakage currents which double (approximately) for each 10°C increase in junction temperature T_J. Measurement of bias current is specified at T_J rather than T_A, since normal warmup thermal transients will affect the bias currents. The measurements for bias currents must be made within 25ms after power is first applied to the device for test. Measurement at $T_A = -55°C$ is not necessary since expected values are too small for typical test systems.
2. Bias current is sensitive to power supply voltage, common mode voltage and temperature as shown by the following typical curves:



3. Negative I_{IB} minimum limits reflect the characteristics of devices with bias current compensation.



4. CMR is calculated from V_{IO} measurements at $V_{CM} = +15V$ and $-15V$.
5. Continuous limits shall be considerably lower. Protection for shorts to either supply exists providing that $T_J(max) \leq 175°C$.
6. Because of thermal feedback effects from output to input, open loop gain is not guaranteed to be linear or positive over the operating range. These requirements, if needed, should be specified by the user in additional procurement documents.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range ..... ±22V
Input Voltage Range (Note 1) ..... ±20V
Differential Input Voltage Range ..... ±40V

Lead Temperature (Soldering, 60 sec.) ..... 300°C
Junction Temperature ..... T_J = 175°C (Note 3)
Storage Temperature Range ..... −65°C to +150°C
Output Short-Circuit Duration ..... Unlimited (Note 2)

NOTES:
1. The absolute maximum negative input voltage is equal to the negative power supply voltage.
2. Short circuit may be to ground to either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
3. For short-term test (in the specific burn-in and life test configuration when required and up to 168 hours maximum), T_J = 275°C.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... ±5 to ±20 VDC

Ambient Temperature Range ..... −55°C to +125°C

ELECTRICAL CHARACTERISTICS at V_{CC} from ±5V to ±20V; source resistance = 50 ohm; ambient temperature range = −55°C to +125°C and figure 1, unless otherwise noted.

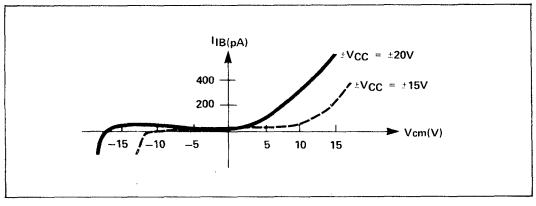
PARAMETER	SYMBOL	CONDITIONS	03 LIMITS MIN	03 LIMITS MAX	06 LIMITS MIN	06 LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	$\pm V_{CC}$ = ±5V, V_{CM} = 0V, T_A = 25°C	−5	5	−2	2	mV
		$\pm V_{CC}$ = ±20V, V_{CM} = ±15V, 0V, −55°C ≤ T_A ≤ +125°C	−7	7	−2.5	2.5	
Input Offset Voltage Temperature Sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	$\pm V_{CC}$ = ±20V, V_{CM} = 0V	−30	30	−10	10	µV/°C
Input Offset Current	I_{IO}	$\pm V_{CC}$ = ±20V, V_{CM} = 0V, T_J = 25°C	−20	20	−20	20	pA
		T_J = 125°C	−20	20	−20	20	nA
Input Bias Current (Note 1) (Note 2) (Note 3)	$+I_{IB}$	$\pm V_{CC}$ = ±20V, V_{CM} = +15V, T_j = 25°C	−100	3500	−100	3500	pA
		t ≤ 25ms T_j = 125°C	−10	60	−10	60	nA
	$-I_{IB}$	$\pm V_{CC}$ = ±15V, V_{CM} = +10V, T_j = 25°C	−100	300	−100	300	pA
		t ≤ 25ms T_j = 125°C	−10	50	−10	50	nA
		$\pm V_{CC}$ = ±20V, −15V ≤ V_{CM} ≤ 0V, T_j = 25°C	−100	100	−100	100	pA
		t ≤ 25ms T_j = 125°C	−10	50	−10	50	nA
Power Supply Rejection Ratio	+PSRR	$+V_{CC}$ = 10V, $-V_{CC}$ = −20V	85	—	85	—	dB
	−PSRR	$+V_{CC}$ = 20V, $-V_{CC}$ = −10V					
Input Voltage Common Mode Rejection (Note 4)	CMR	$\pm V_{CC}$ = ±20V, V_{IN} = ±15V	85	—	85	—	dB
Adjustment for Input Offset Voltage	V_{IO} ADJ(+)	$\pm V_{CC}$ = ±20V	+8	—	+8	—	mV
	V_{IO} ADJ(−)	$\pm V_{CC}$ = ±20V	—	−8	—	−8	
Output Short Circuit Current (for Positive Output) (Note 5)	$I_{OS(+)}$	$\pm V_{CC}$ = ±15V, t ≤ 25ms (Short Circuit to Ground)	−50	—	−50	—	mA
Output Short Circuit Current (for Negative Output) (Note 5)	$I_{OS(-)}$	$\pm V_{CC}$ = ±15V, t ≤ 25ms (Short Circuit to Ground)	—	50	—	50	mA
Supply Current	I_{CC}	T_A = −55°C	—	11	—	11	mA
		$\pm V_{CC}$ = ±15V, T_A = +25°C	—	7	—	7	
		T_A = +125°C	—	7	—	7	
Output Voltage Swing (Maximum)	V_{OP}	$\pm V_{CC}$ = ±20V, R_L = 10kΩ	±16	—	±16	—	V
		$\pm V_{CC}$ = ±20V, R_L = 2kΩ	±15	—	±15	—	
Open Loop Voltage Gain (Single Ended) (Note 6)	$A_{VS(+)}$	$\pm V_{CC}$ = ±20V, V_{OUT} = ±15V, R_L = 2kΩ, T_A = 25°C	50	—	50	—	V/mV
	$A_{VS(-)}$	−55°C ≤ T_A ≤ +125°C	25	—	25	—	
Open Loop Voltage Gain (Single Ended) (Note 6)	A_{VS}	$\pm V_{CC}$ = ±5V, R_L = 2kΩ, V_{OUT} = ±2V	10	—	10	—	V/mV

ELECTRICAL CHARACTERISTICS at V_{CC} from ±5V to ±20V; source resistance = 50 ohm; ambient temperature range = −55°C to +125°C and figure 1, unless otherwise noted.

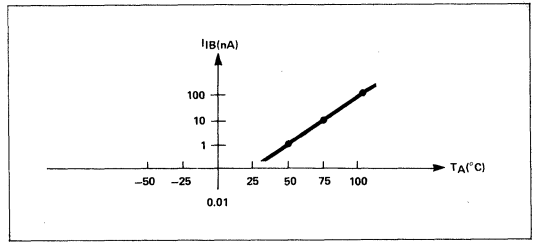
PARAMETER	SYMBOL	CONDITIONS	03 LIMITS MIN	03 LIMITS MAX	06 LIMITS MIN	06 LIMITS MAX	UNITS
Transient Response Rise Time	$TR_{(tr)}$	$\pm V_{CC} = \pm 15V$, $R_L = 2k\Omega$, AV = 1 $C_L = 100pF$, See Figure 2 $V_{IN} = 50mV$	—	450	—	450	ns
Transient Response Overshoot	$TR_{(os)}$	$\pm V_{CC} = \pm 15V$, $R_L = 2k\Omega$, AV = 1 $C_L = 100pF$, See Figure 2 $V_{IN} = 50mV$	—	25	—	25	%
Slew Rate	SR(+) and SR(−)	$V_{IN} = \pm 5V$, $\pm V_{CC} = \pm 15V$ AV = 1, See Figure 2 $T_A = 25°C$ $T_A = -55°C$, $+125°C$	30 20	— —	40 25	— —	V/μs
Settling Time	ts(+) and ts(−)	$\pm V_{CC} = \pm 15V$ (0.1% error) $T_A = 25°C$ AV = −1 See Figure 3	—	800	—	800	ns
Noise (Referred to Input) Broadband	$N_I(BB)$	$\pm V_{CC} = 20V$, $T_A = 25°C$ Bandwidth = 5kHz	—	10	—	10	μV_{rms}
Noise (Referred to Input) Popcorn	$N_I(PC)$	$IV_{CC} = 20V$, $T_A = 25°C$ Bandwidth = 5kHz	—	80	—	80	μV_{pk}

NOTES:

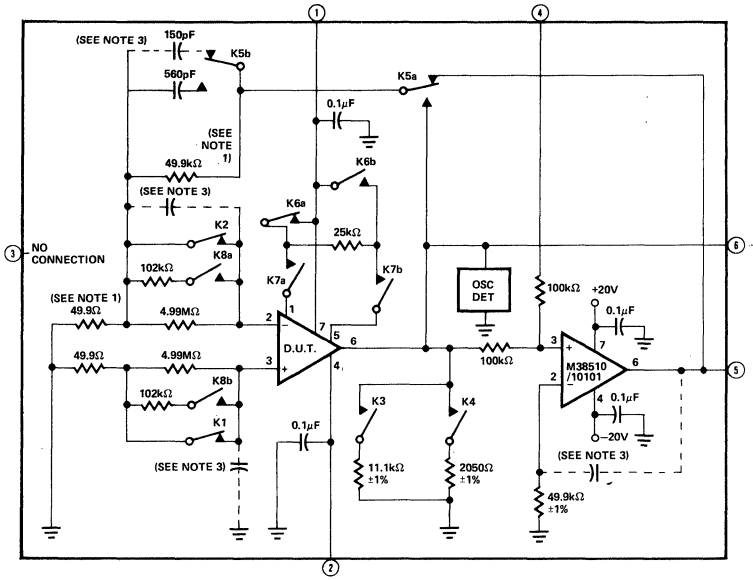
1. Bias currents are actually junction leakage currents which double (approximately) for each 10°C increase in junction temperature T_J. Measurement of bias current is specified at T_J rather than T_A, since normal warmup thermal transients will affect the bias currents. The measurements for bias currents must be made within 25ms after power is first applied to the device for test. Measurement at $T_A = -55°C$ is not necessary since expected values are too small for typical test systems.
2. Bias current is sensitive to power supply voltage, common mode voltage and temperature as shown by the following typical curves:



3. Negative I_{IB} minimum limits reflect the characteristics of devices with bias current compensation.



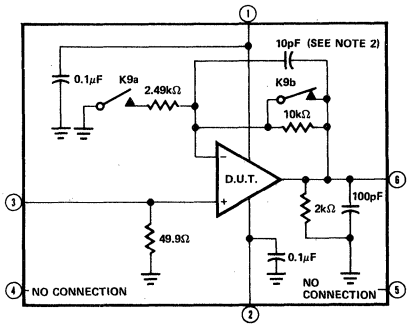
4. CMR is calculated from V_{IO} measurements at $V_{CM} = +15V$ and $-15V$.
5. Continuous limits shall be considerably lower. Protection for shorts to either supply exists providing that $T_J(max) \leq 175°C$.
6. Because of thermal feedback effects from output to input, open loop gain is not guaranteed to be linear or positive over the operating range. These requirements, if needed, should be specified by the user in additional procurement documents.



NOTES:

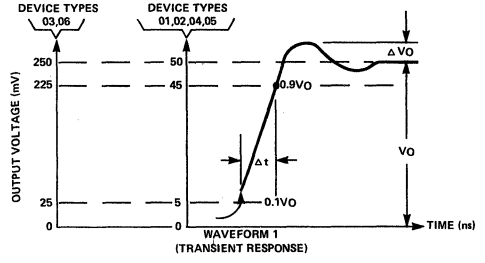
1. ALL RESISTORS ARE ±0.1% TOLERANCE AND ALL CAPACITORS ARE ±10% TOLERANCE UNLESS OTHERWISE SPECIFIED.
2. PRECAUTIONS SHALL BE TAKEN TO PREVENT DAMAGE TO THE D.U.T. DURING INSERTION INTO SOCKET AND CHANGE OF STATE OF RELAYS (i.e. DISABLE VOLTAGE SUPPLIES, CURRENT LIMIT $\pm V_{CC}$, ETC.).
3. COMPENSATION CAPACITORS SHOULD BE ADDED AS REQUIRED FOR TEST CIRCUIT STABILITY.TWO GENERAL METHODS FOR STABILITY COMPENSATION EXIST, ONE METHOD IS WITH A CAPACITOR FOR NULLING AMP FEEDBACK. THE OTHER METHOD IS WITH A CAPACITOR IN PARALLEL WITH THE 49.9kΩ CLOSED LOOP FEEDBACK RESISTOR. BOTH METHODS SHOULD NOT BE USED SIMULTANEOUSLY. PROPER WIRING PROCEDURES SHALL BE FOLLOWED TO PREVENT UNWANTED COUPLING AND OSCILLATIONS, ETC. LOOP RESPONSE AND SETTLING TIME SHALL BE CONSISTENT WITH THE TEST RATE SUCH THAT ANY VALUE HAS SETTLED FOR AT LEAST FIVE LOOP TIME CONSTANTS BEFORE THE VALUE IS MEASURED.
4. ADEQUATE SETTLING TIME SHOULD BE ALLOWED SUCH THAT EACH PARAMETER HAS SETTLED TO WITHIN 5% OF ITS FINAL VALUE.
5. ALL RELAYS ARE SHOWN IN THE NORMAL DE-ENERGIZED STATE.
6. THE NULLING AMPLIFIER SHALL BE A M38510/10101XXX. SATURATION OF THE NULLING AMPLIFIER IS NOT ALLOWED ON TESTS WHERE THE E (PIN 5) VALUE IS MEASURED.
7. THE LOAD RESISTORS 2050Ω AND 11.1kΩ YIELD EFFECTIVE LOAD RESISTANCES OF 2kΩ AND 10kΩ RESPECTIVELY.
8. ANY OSCILLATION GREATER THAN 300mV IN AMPLITUDE (PEAK-TO-PEAK) SHALL BE CAUSE FOR DEVICE FAILURE.

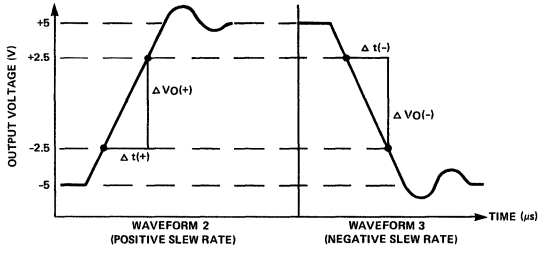
Figure 1. Test Circuit for Static Tests



NOTES:

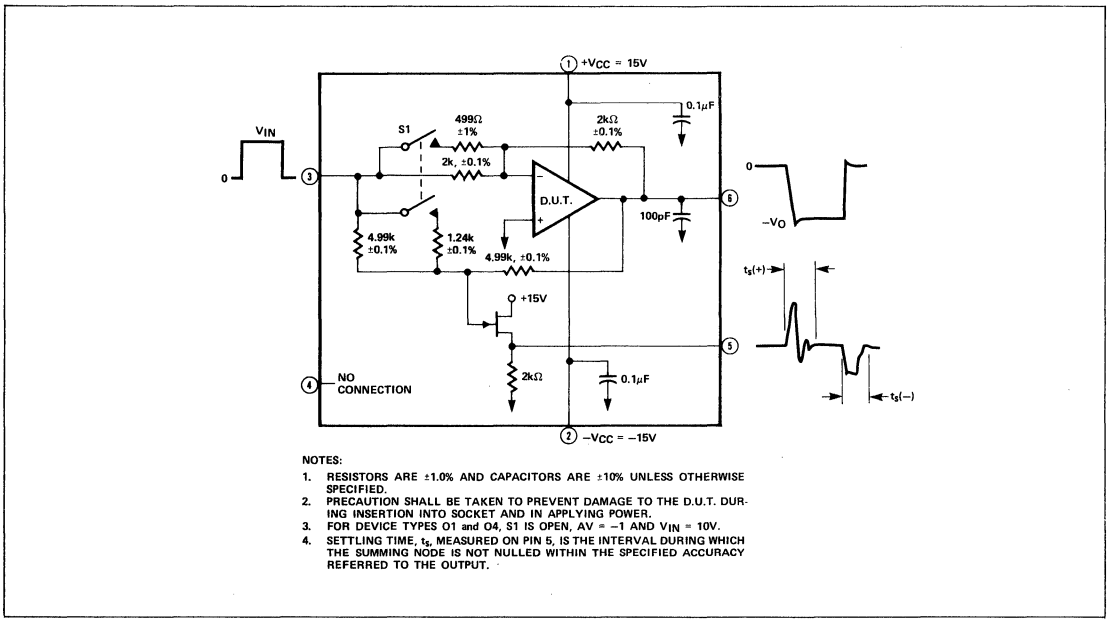
1. RESISTORS ARE ±1.0% TOLERANCE AND CAPACITORS ARE ±10% TOLERANCE.
2. THIS CAPACITANCE INCLUDES THE ACTUAL MEASURED VALUE WITH STRAY AND WIRE CAPACITANCE.
3. PRECAUTIONS SHALL BE TAKEN TO PREVENT DAMAGE TO THE D.U.T. DURING INSERTION INTO SOCKET AND IN APPLYING POWER.





PARAMETER SYMBOL	DEVICE TYPE	INPUT PULSE SIGNAL AT $t_r \leq 50ns$	OUTPUT PULSE SIGNAL	EQUATION
TR (t_r)	ALL	+50mV	WAVEFORM 1	TR (t_r) = Δt
TR (O_S)	ALL	+50mV	WAVEFORM 1	TR (O_S) = 100 ($\Delta V_O/V_O$) %
SR (+)	01, 02, 04, 05	−5V to +5V STEP	WAVEFORM 2	SR (+) = $\Delta V_O(+)/\Delta t(+)$
	03, 06	−1V to +1V STEP	WAVEFORM 2	
SR (−)	01, 02, 04, 05	+5V to −5V STEP	WAVEFORM 3	SR (−) = $\Delta V_O(-)/\Delta t(-)$
	03, 06	−1V to +1V STEP	WAVEFORM 3	

Figure 2. Test Circuit for Transient Response and Slew Rate



NOTES:
1. RESISTORS ARE ±1.0% AND CAPACITORS ARE ±10% UNLESS OTHERWISE SPECIFIED.
2. PRECAUTION SHALL BE TAKEN TO PREVENT DAMAGE TO THE D.U.T. DURING INSERTION INTO SOCKET AND IN APPLYING POWER.
3. FOR DEVICE TYPES 01 and 04, S1 IS OPEN, AV = −1 AND V_{IN} = 10V.
4. SETTLING TIME, t_s, MEASURED ON PIN 5, IS THE INTERVAL DURING WHICH THE SUMMING NODE IS NOT NULLED WITHIN THE SPECIFIED ACCURACY REFERRED TO THE OUTPUT.

Figure 3. Test Circuit for Settling Time

BURN-IN

Devices supplied by PMI have been subjected to burn-in per method 1015 of MIL-STD-883 using test condition C with circuit shown on Figure 4 or test condition F using circuit shown on Figure 5.

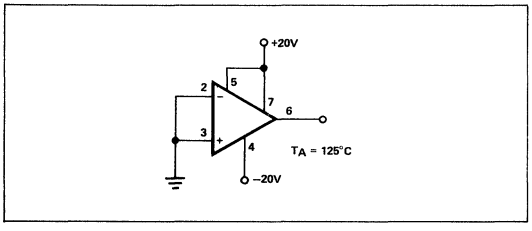


Figure 4. Test Circuit, Burn-In (Steady-State Power and Reverse Bias) and Operating Life Test

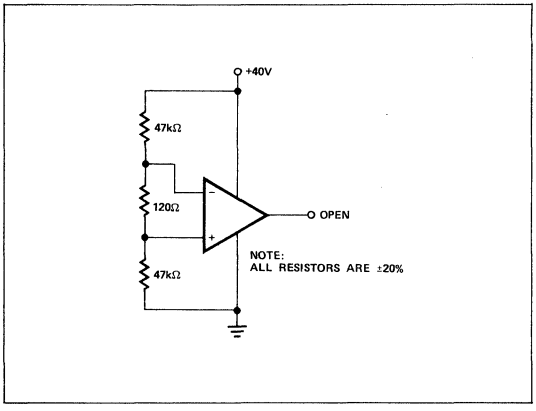


Figure 5. Accelerated Burn-In and Life Test Circuit

SECTION 6

BUFFERS (VOLTAGE FOLLOWERS)

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BUFFERS (VOLTAGE FOLLOWERS)

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PRODUCT	TITLE	PAGE
BUF-01	Precision Buffer/Voltage-Follower	6-3
BUF-02	High-Speed BIFET Buffer/Voltage-Follower	6-8
BUF-03	Very High-Speed Buffer/Voltage-Follower	6-12

INTRODUCTION

Analog buffers, as the name implies, are used to buffer a high-impedance source from a low-impedance load while accurately reproducing the input signal. Consequently, the most important criterion for a buffer is that it introduces minimal error between input signal and output signal. Inaccuracies such as those due to offsets, bandwidth limitations, or non-unity gain must be considered when specifying an analog buffer. The buffer is like an op amp operating in the voltage follower mode. Many manufacturers specify buffers as if they were operational amplifiers making the error analysis of a buffer a tedious chore.

PMI's buffers are unique in specifying maximum DC output error for a wide range of input signals, source resistances, and load impedances. Output error includes errors introduced by offset voltage (V_{OS}), input bias current (I_B), voltage gain (A_V), common-mode rejection ratio (CSMRR) and output loading ($R_O/(R_L + r_O)$).

PMI tests, specifies and guarantees the maximum output error. For people using op amps as buffers, a worst-case analysis must be performed to determine what the maximum DC output error could be.

The important specs for a buffer are output error, slew rate, bandwidth, input bias current, and output drive capability. A brief scan of the PMI buffer specifications will show the premium performance that has been achieved through PMI's high-technology processing which includes triple passivation, Zener Zap trimming and superior design. Common applications of buffers include Sample/Hold circuits, ADCs, analog commutators,and impedance converters.

Three PMI voltage buffers (also known as unity-gain amplifiers or voltage followers) satisfy most buffer applications. The BUF-01 stresses accuracy and is suitable in low-speed applications. The BUF-02 provides high speed along with accuracy. The BUF-03 delivers very high speed and bandwidth while surpassing the accuracy specifications of comparable devices. The BUF-03 is especially well-suited to drive large capacitive loads.

BUF-01

PRECISION BUFFER/VOLTAGE FOLLOWER WITH OVERVOLTAGE PROTECTION

FEATURES

- **Output Error Fully Specified ..... 250μV Maximum**
- **Low Input Offset Voltage ..... 60μV Typical**
- **Pin Compatible with LM110**
- **Drives 10kΩ Load to ±10V**
- **Low Voltage Gain Error 0.001%**
- **Excellent Power Supply Rejection Ratio ..... 106dB Typical**
- **Low Output Impedance ..... 0.03Ω Typical**
- **Low Input Noise Voltage ..... $0.8\mu V_{p-p}$ Maximum**

GENERAL DESCRIPTION

The BUF-01 is the first precision voltage follower tested and guaranteed with a **Maximum Output Error** specification. **Maximum Output Error** includes errors introduced by offset voltage, input bias current, gain, CMRR and output loading. This ensures that the TOTAL output error will not exceed the maximum under any combination of input or output.

Pin compatible with the LM110, the BUF-01 features low output impedance (0.03Ω typical), high gain and excellent power supply rejection (106dB typical) with extremely low input voltage noise.

Fabricated with Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation™ Process," the BUF-01 utilizes on-chip zener-zap trimming to achieve very low offset voltage with excellent long-term stability. This eliminates the need for offset nulling in all but the most stringent applications.

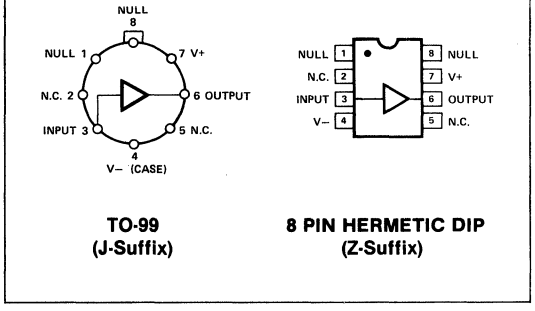
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (μV)	HERMETIC PACKAGE TO-99 8-PIN	HERMETIC PACKAGE DIP 8-PIN	OPERATING TEMPERATURE RANGE
100	BUF01AJ*	BUF01AZ*	MIL
100	BUF01EJ	BUF01EZ	COM
150	BUF01BJ*	BUF01BZ*	MIL
150	BUF01FJ	BUF01FZ	COM

* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

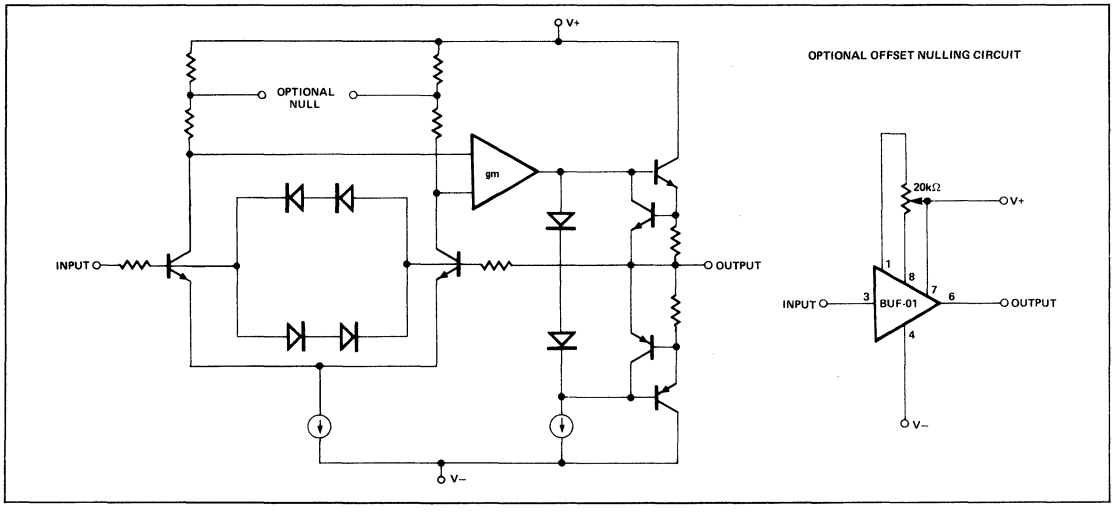
PIN CONNECTIONS



TO-99 (J-Suffix)

8 PIN HERMETIC DIP (Z-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 3)

Supply Voltage ..... ±22V
Internal Power Dissipation (Note 1) 500mW
Input Voltage (Note 2) ..... ±22V
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range
BUF-01A, BUF-01B ..... −55°C to +125°C
BUF-01E, BUF-01F ..... 0°C to +70°C
DICE Junction Temperature (T_j) ..... −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.
2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
3. Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

Package Type	Maximum Ambient Temperature Rating	Derate Above Maximum Ambient Temperature
TO-99(J)	80°C	7.1mW/°C
8 PIN HERMETIC DIP (Z)	75°C	6.7mW°C

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	BUF-01A BUF-01E MIN	BUF-01A BUF-01E TYP	BUF-01A BUF-01E MAX	BUF-01B BUF-01F MIN	BUF-01B BUF-01F TYP	BUF-01B BUF-01F MAX	UNITS
Maximum Output Error	OUT_{error}	$V_{IN} = +10V, 0V, -10V$ $R_S = 0$ to 20kΩ $R_L \geq 10K\Omega$ (in all combinations.)	—	0.1	0.25	—	0.2	0.5	mV
Input Offset Voltage	V_{OS}	$V_{IN} = 0V$, $R_S = 50\Omega$	—	60	100	—	80	150	μV
Input Current	I_{IN}		—	±2.0	±7.0	—	±2.0	±7.0	nA
Input Resistance	R_{IN}		—	10^{11}	—	—	10^{11}	—	Ω
Large-Signal Voltage Gain Error	A_{VE}	$R_L \geq 10k\Omega$, $V_O = \pm 10V$	—	0.001	0.0025	—	0.001	0.005	%
Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	0.03	—	—	0.03	—	Ω
Input Voltage Range	V_{IN}		±12.0	±13.0	—	±12.0	±13.0	—	V
Output Current	I_O	$-5V \leq V_O \leq +5V$	—	±13	—	—	±13	—	mA
Power Supply Rejection Ratio	PSRR	$\pm 3V \leq V_S \leq \pm 18V$	—	5	20	—	7	32	μV/V
Small Signal Bandwidth	BW	(Note 1)	0.4	0.7	—	0.4	0.7	—	MHz
Input Noise Voltage	$e_{n\ p\text{-}p}$	0.1Hz to 10Hz (Note 2)	—	0.5	0.8	—	0.5	0.8	$\mu V_{p\text{-}p}$
Input Noise Current	$i_{n\ p\text{-}p}$	0.1Hz to 10Hz (Note 2)	—	15	40	—	15	40	$pA_{p\text{-}p}$
Slew Rate	SR	$R_L \geq 10k\Omega$ (Note 1)	0.1	0.2	—	0.1	0.2	—	V/μs
Power Consumption	Pd	$V_S = \pm 15V$, $V_O = 0$ $V_S = \pm 3V$, $V_O = 0$	— —	75 6	120 —	— —	80 8	150 —	mW

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ for BUF-01A and FUB-01B, $0°C \leq T_A \leq +70°C$ for BUF-01E and BUF-01F, unless otherwise noted.

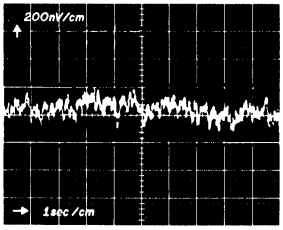
PARAMETER	SYMBOL	CONDITIONS	BUF-01A BUF-01E MIN	BUF-01A BUF-01E TYP	BUF-01A BUF-01E MAX	BUF-01B BUF-01F MIN	BUF-01B BUF-01F TYP	BUF-01B BUF-01F MAX	UNITS
Maximum Output Error	OUT_{error}	$V_{IN} = +10V, 0V, -10V$; $R_S = 0$ to 20kΩ $R_L \geq 10k\Omega$ (in all combinations)	—	0.2	0.35	—	0.4	0.8	mV
Input Offset Voltage	V_{OS}	$V_{IN} = 0V$, $R_S = 50\Omega$	—	80	280	—	120	400	μV
Large-Signal Voltage Gain Error	A_{VE}	$R_L \geq 10k\Omega$, $V_O = \pm 10V$	—	0.002	0.0035	—	0.002	0.008	%
Average Input Offset Voltage Drift	TCV_{OS}	(Note 2)	—	0.2	1.8	—	0.3	2.5	μV/°C
Input Current	I_{IN}		—	—	±12	—	—	±12	nA
Average Input Current Drift	TCI_{IN}	(Note 2)	—	10	120	—	12	120	pA/°C
Input Voltage Range	V_{IN}		±11.5	±12.6	—	±11.0	±12.6	—	V
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	μV/V
Power Consumption	Pd	$V_O = 0$	—	80	150	—	90	180	mW

NOTES:

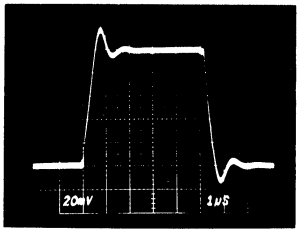
1. Guaranteed by design.
2. Sample tested.

TYPICAL PERFORMANCE CURVES

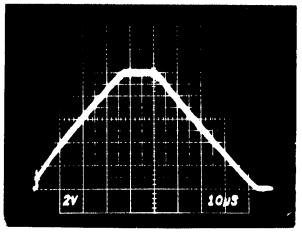
BUF-01 LOW FREQUENCY NOISE



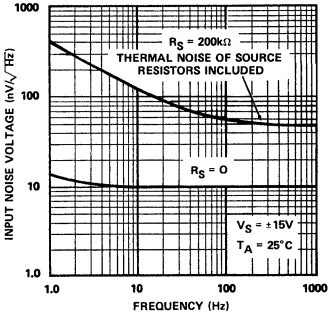
SMALL-SIGNAL TRANSIENT RESPONSE



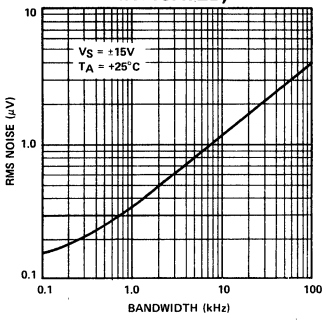
LARGE-SIGNAL TRANSIENT RESPONSE



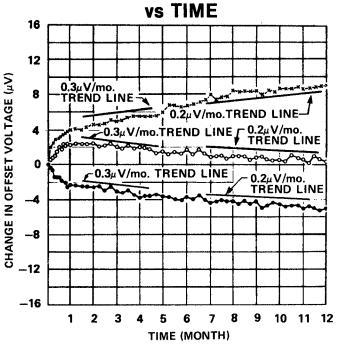
TOTAL INPUT NOISE VOLTAGE vs FREQUENCY



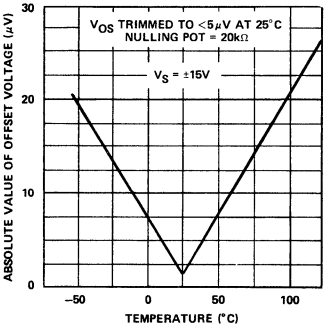
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



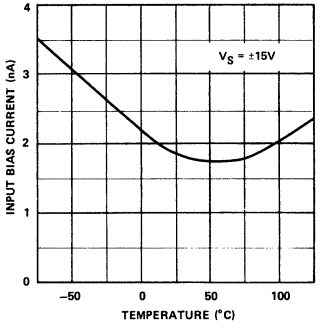
OFFSET VOLTAGE STABILITY vs TIME



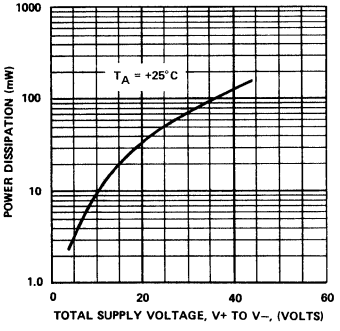
TRIMMED OFFSET VOLTAGE vs TEMPERATURE



INPUT BIAS CURRENT vs TEMPERATURE

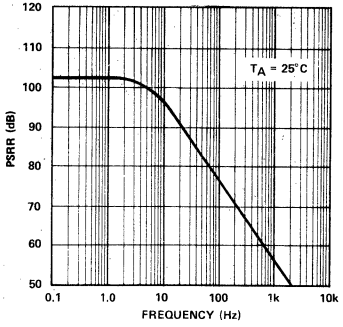


POWER CONSUMPTION vs POWER SUPPLY

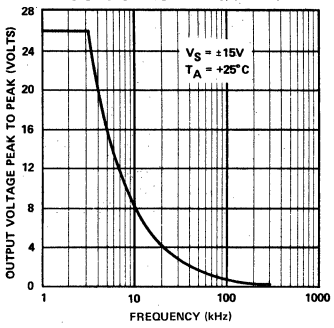


TYPICAL PERFORMANCE CURVES

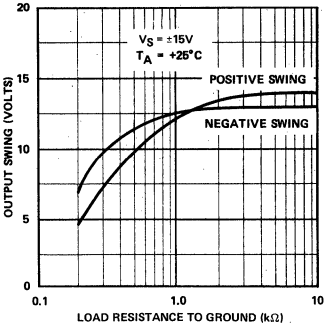
PSRR vs FREQUENCY



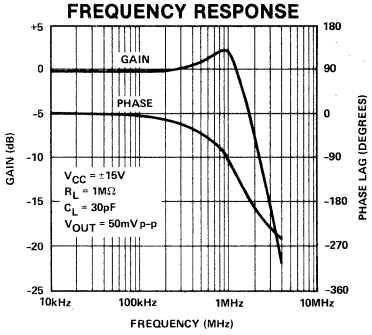
MAXIMUM UNDISTORTED OUTPUT vs FREQUENCY



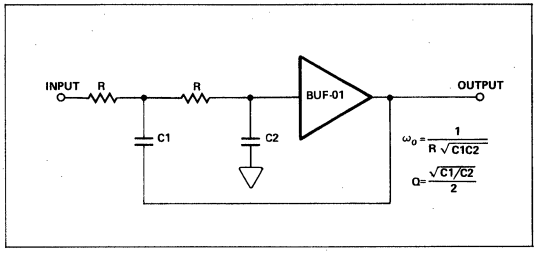
OUTPUT VOLTAGE vs LOAD RESISTANCE



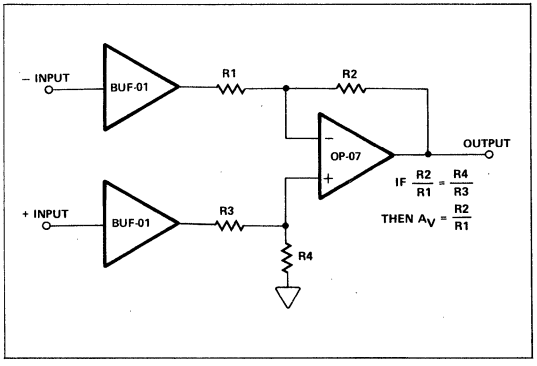
GAIN AND PHASE vs FREQUENCY RESPONSE



SECOND-ORDER LOWPASS FILTER

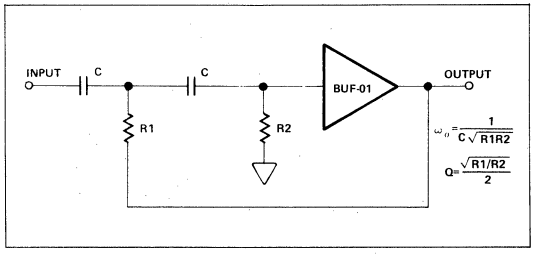


HIGH-IMPEDANCE DIFFERENTIAL AMPLIFIER

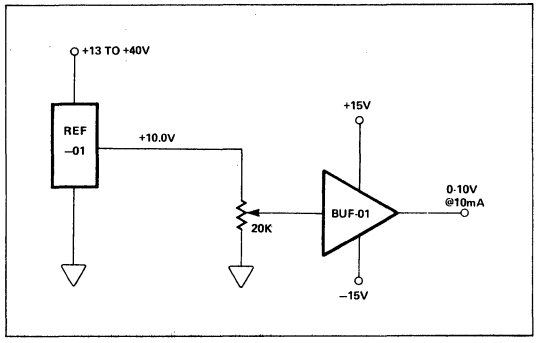


TYPICAL APPLICATIONS

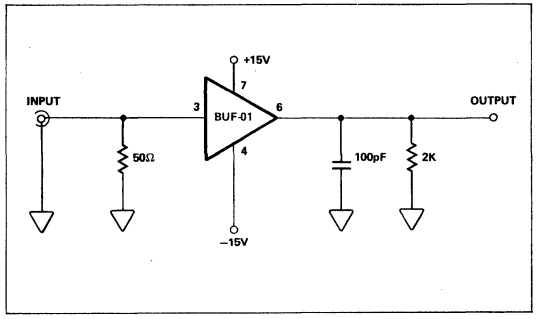
SECOND-ORDER HIGHPASS FILTER



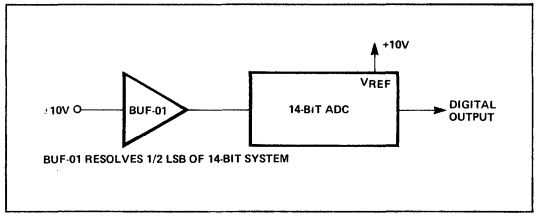
BUFFERED REFERENCE



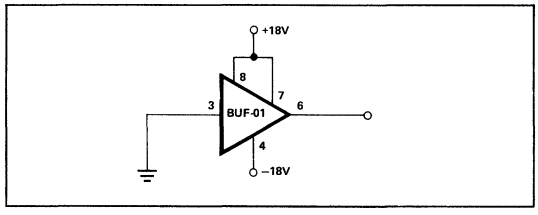
TRANSIENT RESPONSE TEST CIRCUIT



HIGH RESOLUTION ADC INPUT BUFFER



BURN-IN CIRCUIT



MAXIMUM OUTPUT ERROR

The **Maximum Output Error** specification combines errors introduced by offset voltage, input bias current, gain, CMRR, and device output impedance. The specification is 100% tested for a given combination of source resistance, load resistance, and input voltages. The tedious chore of performing a worst case summation of component error terms is not necessary.

To assist the designer who has a specific application, the individual parameters of offset voltage, input current, voltage gain and PSRR are also given.

It should be noted that an error analysis may yield a figure higher than the Maximum Output Error specification. This is due to the potential cancellation of the effects of one error source by another. In situations such as this, the Maximum Output Error specification supersedes results from any error analysis.

BUF-02

HIGH-SPEED BIFET BUFFER/VOLTAGE FOLLOWER

FEATURES

- **Output Error Fully Specified ..... 1.5mV Maximum**
- **Low Input Offset Voltage ..... 1.0mV Maximum**
- **Pin Compatible with LM110 in Unnulled Applications**
- **Low Gain Error 0.001%**
- **High Gain ..... 0.9999 V/V Minimum**
- **Excellent Power Supply Rejection Ratio ..... 100dB Typical**
- **Low Output Impedance ..... 0.03Ω Typical**
- **High Slew Rate ..... 24V/μs Typical**
- **Very Low Input Current ..... 0.3nA Maximum**

GENERAL DESCRIPTION

The BUF-02 is the first high-speed voltage follower tested and guaranteed with a Maximum Output Error specification. Comprised of a wide array of input and output loads and input voltage test conditions, this specification assures that the BUF-02 will drive a 10kΩ load over a ±10V output voltage range with less than 1.5mV error referred to the input. Pin compatible with the LM110 in unnulled applications, the BUF-02 features low output impedance (0.03Ω typical), high gain, and excellent power supply rejection (100dB typical) with very low input bias current.

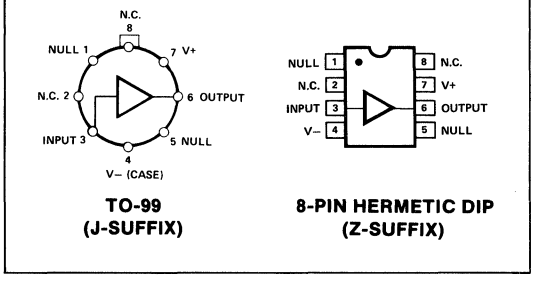
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	PACKAGE HERMETIC DIP 8-PIN	OPERATING TEMP. RANGE
1.5	BUF02AJ*	BUF02AZ*	MIL
1.5	BUF02EJ	BUF02EZ	COM
4.0	BUF02BJ*	BUF02BZ*	MIL
4.0	BUF02FJ	BUF02FZ	COM

* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

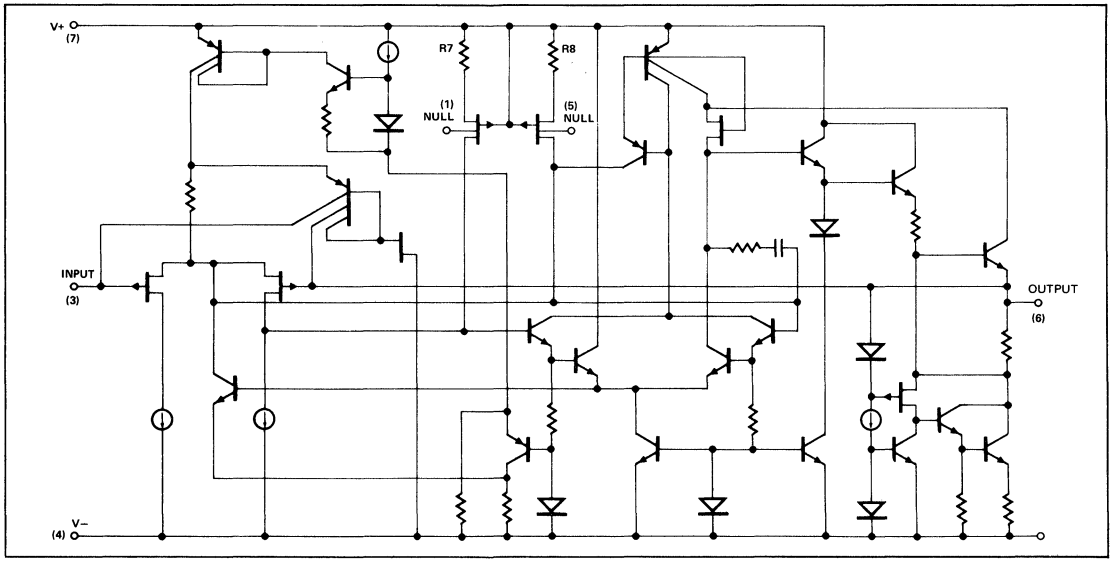
PIN CONNECTIONS



TO-99 (J-SUFFIX)

8-PIN HERMETIC DIP (Z-SUFFIX)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Internal Power Dissipation (Note 1) 500mW
Input Voltage (Note 2) ..... ±15V
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range
BUF-02A, BUF-02B ..... −25°C to +125°C
BUF-02E, BUF-02F ..... 0°C to +70°C
Lead Temperature Range (Soldering 60 sec.) ..... 300°C

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic Dip (Z)	75°C	6.7mW/°C

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	BUF-02A BUF-02E MIN	BUF-02A BUF-02E TYP	BUF-02A BUF-02E MAX	BUF-02B BUF-02F MIN	BUF-02B BUF-02F TYP	BUF-02B BUF-02F MAX	UNITS
Maximum Output Error	OUT_{error}	$V_{IN} = +10V, 0V, -10V$ $R_S = 0$ to $20k\Omega$ $R_L \geq 10k\Omega$, in all combinations.	—	0.8	1.5	—	1.5	4.0	mV
Input Offset Voltage	V_{OS}	$V_{IN} = 0V$, $R_S \leq 50\Omega$	—	0.5	1.0	—	1.0	3.0	mV
Input Current	I_{IN}	(Note 4)	—	0.1	0.2	—	0.2	0.5	nA
Input Resistance	R_{IN}		—	10^{12}	—	—	10^{12}	—	Ω
Large Signal Voltage Gain Error	A_{VE}	$R_L \geq 10k\Omega$, $\Delta V_{IN} = \pm 10V$	—	0.001	0.015	—	0.001	0.04	%
Output Resistance	R_O		—	0.03	—	—	0.03	—	Ω
Input Voltage Range	V_{IN}		±10.5	±11.5	—	±10.5	±11.5	—	V
Input Noise Voltage Density	e_n	$R_S = 100\Omega$, f = 100Hz	—	15	—	—	15	—	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	f = 100Hz	—	0.01	—	—	0.01	—	$pA/\sqrt{Hz}$
Slew Rate	SR	$R_L \geq 10k\Omega$ (Note 3)	12	24	—	9.0	18	—	V/μs
Power Consumption	P_d	$V_O = 0V$	—	150	210	—	160	240	mW
Output Current		$-5V \leq V_O \leq +5V$	—	10	—	—	10	—	mA
Power Supply Rejection	PSRR	$\pm 10V \leq V_S \leq \pm 15V$	—	10	57	—	20	63	μV/V
Settling Time	t_s	$\Delta V_{IN} = 10V$, to 0.1% $\Delta V_{IN} = 10V$, to 0.02%	— —	0.7 1.5	— —	— —	0.7 1.5	— —	μs

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25°C \leq T_A \leq +125°C$ for BUF-02A and BUF-02B, and for $0°C \leq T_A \leq +70°C$ for BUF-02E and BUF-02F, unless otherwise noted. (Note 5)

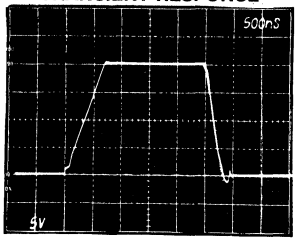
PARAMETER	SYMBOL	CONDITIONS	BUF-02A BUF-02E MIN	BUF-02A BUF-02E TYP	BUF-02A BUF-02E MAX	BUF-02B BUF-02F MIN	BUF-02B BUF-02F TYP	BUF-02B BUF-02F MAX	UNITS
Maximum Output Error	OUT_{error}	$V_{IN} = +10V, 0V, -10V$; $R_S = 0$ to $20k\Omega$ $R_L \geq 10k\Omega$ in all combinations.	—	1.0	2.5	—	2.0	6.0	mV
Input Offset Voltage	V_{OS}	$V_{IN} = 0V$, $R_S = 50\Omega$	—	0.7	1.5	—	1.5	5.0	mV
Large Signal Voltage Gain Error	A_{VE}	$R_L \geq 10k\Omega$, $\Delta V_{IN} = \pm 10V$	—	0.01	0.025	—	0.01	0.06	%
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	—	2.0	—	—	5.0	—	μV/°C
Change in Input Offset Drift with V_{OS} Adjust	$\frac{\Delta TCV_{OS}}{\Delta V_{OS}}$	$R_S = 50\Omega$	—	0.5	—	—	0.5	—	$\frac{\mu V/°C}{mV}$
Input Current	I_{IN}	$T_A \leq 125°C$ (Note 4) $T_A \leq 70°C$ (Note 4)	— —	3 0.4	10 1.0	— —	8 0.8	25 2.0	nA
Input Voltage Range	V_{IN}		±10.4	±11.3	—	±10.4	±11.3	—	V
Power Supply Rejection Ratio	PSRR	$\pm 10V \leq V_S \leq \pm 15V$	—	16	100	—	32	200	μV/V
Power Consumption	Pd	$V_O = 0V$	—	180	240	—	190	270	mW

NOTES:

1. See table for maximum ambient temperature rating and derating factor.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Parameter is guaranteed by design.
4. The input bias currents are junction leakage currents which approximately double for every 18°C increase in the junction temperature. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_d
5. Military grade devices are tested at 0°C ambient temperature. This is equivalent to a −25°C ambient temperature test with the device warmed up.

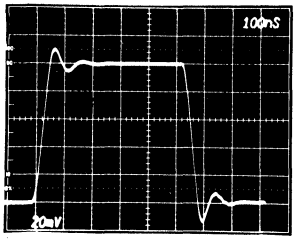
TYPICAL PERFORMANCE CURVES

LARGE-SIGNAL TRANSIENT RESPONSE



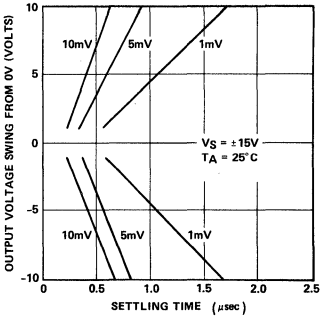
$V_S = \pm 15V, T_A = 25°C$

SMALL-SIGNAL TRANSIENT RESPONSE

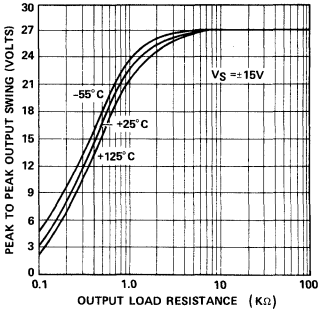


$V_S = \pm 15V, T_A = 25°C$

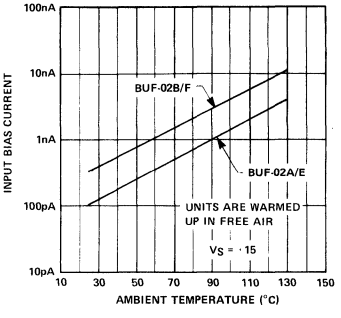
SETTLING TIME vs STEP SIZE



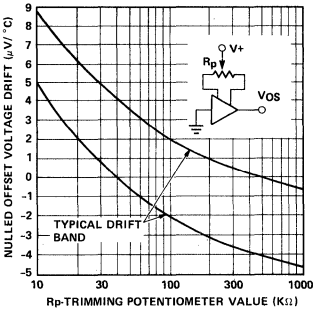
OUTPUT VOLTAGE vs LOAD RESISTANCE



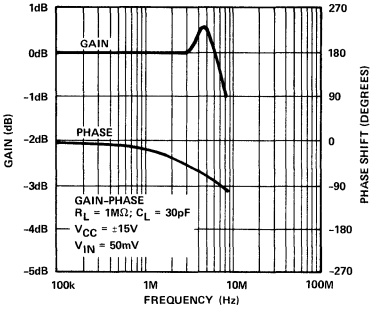
INPUT CURRENT vs AMBIENT TEMPERATURE



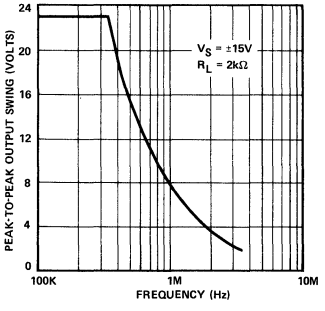
OFFSET VOLTAGE vs TEMPERATURE OF REPRESENTATIVE UNITS



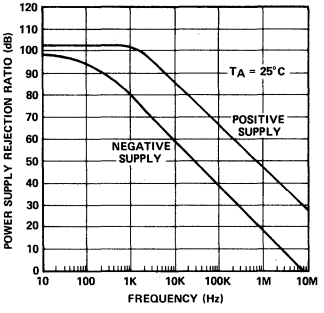
SMALL SIGNAL FREQUENCY RESPONSE



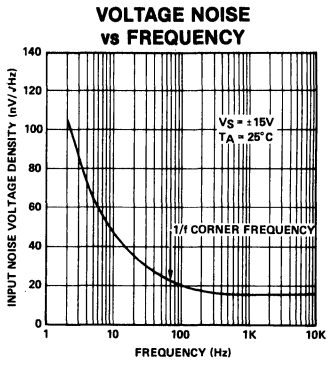
LARGE SIGNAL FREQUENCY RESPONSE



POWER SUPPLY REJECTION vs FREQUENCY

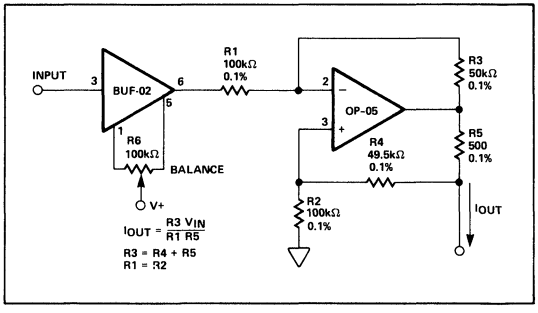


TYPICAL PERFORMANCE CURVES

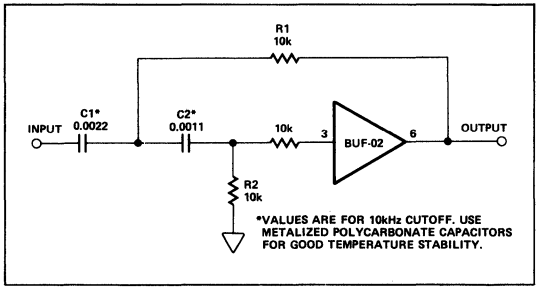


TYPICAL APPLICATIONS

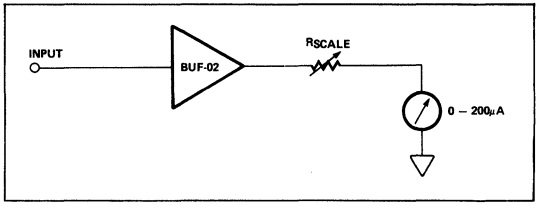
BILATERAL CURRENT SOURCE



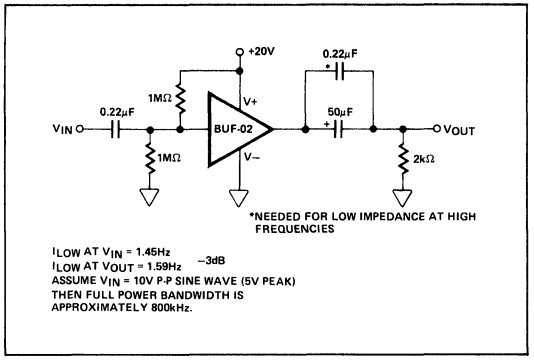
SECOND-ORDER HIGH-PASS ACTIVE FILTER



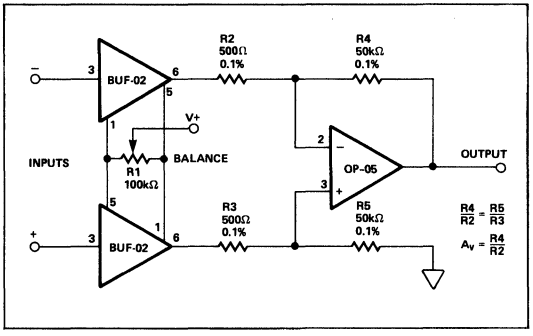
HIGH IMPEDANCE METER DRIVER



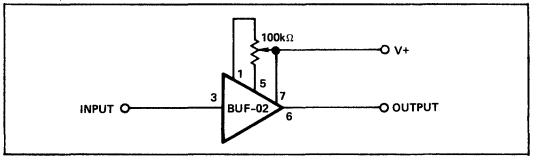
HIGH-SPEED SINGLE-SUPPLY AC BUFFER



DIFFERENTIAL INPUT INSTRUMENTATION AMPLIFIER



OPTIONAL OFFSET NULLING CIRCUIT



MAXIMUM OUTPUT ERROR

The **Maximum Output Error** specification combines errors introduced by offset voltage, input bias current, gain, CMRR and device output impedance. The specification is 100% tested for a given combination of source resistance, load resistance and input voltages. The tedious chore of performing a worst case summation of component error terms is not necessary.

The individual parameters of offset voltage, input current, voltage gain and PSRR are also given.

It should be noted that an error analysis may yield a figure higher than the Maximum Output Error specification. This is due to the potential cancellation of the effects of one error source by another. In situations such as this, the Maximum Output Error specification supersedes results from any error analysis.

BUF-03

VERY HIGH-SPEED BUFFER/VOLTAGE FOLLOWER

FEATURES

- **Very High Slew Rate** **300V/μsec**
- **Wide Bandwidth** **63MHz**
- **Load Drive Current** ..... **70mA Peak**
- **Easily Drives any Capacitive Load without Oscillation**
- **High Input Resistance** ..... $5 \times 10^{11}\Omega$
- **Low Output Resistance** **2Ω**
- **Very Low Bias Current (Warmed Up)** **150pA**
- **Low Offset Voltage** **2mV**
- **Unity Gain** **0.997V/V**
- **Excellent Gain Linearity** **0.015%**

GENERAL DESCRIPTION

The BUF-03 is the first very high-speed monolithic voltage follower. Featuring performance previously unobtainable in a monolithic unit, it offers a combination of both exceptional speed and excellent input/output specifications. Implemented in an open-loop circuit employing source followers and emitter followers, the BUF-03 utilizes a quasi-quad FET input structure to optimize both speed and D.C. input characteristics. On-chip zener-zap trimming is used to achieve low offset voltage while careful biasing throughout results in excellent gain linearity over the full input voltage range.

Applications for which the BUF-03 is well suited include high-speed line drivers, isolation amplifiers for driving reactive loads and high-speed data conversion and sample-hold circuits.

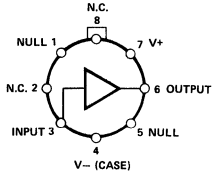
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	OPERATING TEMPERATURE RANGE
6	BUF03AJ*	MIL
6	BUF03EJ	COM
15	BUF03BJ*	MIL
15	BUF03FJ	COM

*Also available with MIL-STD-883B processing. To order add /883 as a suffix to the part number.

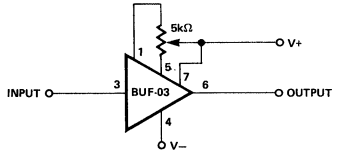
†All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS

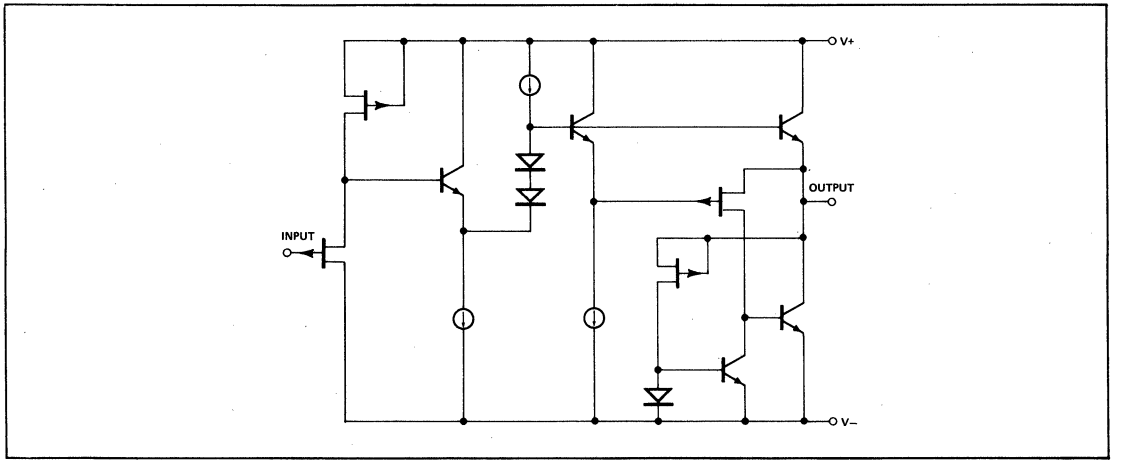


TO-99 (J-Suffix)

OPTIONAL OFFSET NULLING CIRCUIT



SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note)

Supply Voltage (V+ to V−) 36V
Internal Power Dissipation (P_d) (see curves)
in still air, no heat sink 1.05W
with heat sink, θ_{JA} = 90 °C/W 1.40W
Input Voltage (for V_S < ±18V, maximum input voltage is equal to supply) ..... ±18V
Continuous Output Current 70mA
Peak Output Current 100mA
Short Circuit Protection (Maximum P_d or T_j not to be exceeded) ..... Indefinite at 80mA

Maximum Junction Temperature (T_j) ..... 175 °C
Storage Temperature Range ..... −65 °C to +175 °C
Operating Temperature Range
BUF-03A, BUF-03B ..... −55 °C to +125 °C
BUF-03E, BUF-03F ..... 0 °C to +70 °C
Lead Temperature (soldering, 60 sec) ..... 300 °C
DICE Junction Temperature (T_j) ..... −65° C to +175° C

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25 °C, T_{CHIP} = 75 °C, device fully warmed up, unless otherwise noted. (Note 1)

			BUF-03A/E			BUF-03B/F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
AC SPECIFICATIONS									
Slew Rate	SR	$R_L \geq 2k\Omega$, C_L = 50pF (Note 2)	220	300	—	180	250	—	V/μsec
Power Bandwidth	PBW	$V_{IN} = 10V_{p-p}$, $R_L \geq 2k\Omega$	—	9	—	—	8	—	MHz
Bandwidth	BW	$\Delta V_{IN} = \leq 2Vp\text{-}p$	—	63	—	—	50	—	MHz
Settling Time	t_s	to 0.1%, ±10V step	—	90	—	—	100	—	nsec
Capacitive Load Capability	C_{LOAD}	No Oscillations	—	1	—	—	1	—	μF
Propagation Delay	t_d		—	7	—	—	7	—	nsec
Rise Time	t_r	ΔV = 0.5V	—	7	—	—	7	—	nsec
Wide Band Input Noise Voltage	V_n	DC to 50MHz	—	350	—	—	400	—	μV_{RMS}
Input Noise Voltage Density	e_n	f = 10kHz	—	50	—	—	60	—	nV/√Hz
DC SPECIFICATIONS									
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	2	6	—	4	15	mV
Input Bias Current	I_B		—	150	400	—	180	700	pA
Input Resistance	R_{IN}		—	$5x10^{11}$	—	—	$4x10^{11}$	—	Ω
Voltage Gain (V_{IN} = ±10V)	A_{VO}	$R_L \geq 10k\Omega$	0.9960	0.9975	—	0.9940	0.9970	—	V/V
		$R_L \geq 2k\Omega$	0.9945	0.9960	—	0.9930	0.9950	—	
		$R_L \geq 1k\Omega$	0.9925	0.9945	—	0.9905	0.9930	—	
Nonlinearity (Note 3)	NL	V_{IN} = ±10V, $R_L \geq 2k\Omega$	—	0.015	0.023	—	0.017	0.03	%F.S.
		V_{IN} = ±7V, $R_L \geq 1k\Omega$	—	0.013	0.023	—	0.015	0.03	
Maximum Output Error	OUT_{error}	V_{IN} = +10V, 0V, −10V R_S = 0 to 20kΩ $R_L \geq 2k\Omega$ in all combinations	—	40	60	—	50	85	mV
Power Supply Rejection Ratio	PSRR	V_S = ±6V to ±18V	—	0.10	0.71	—	0.15	1.42	mV/V
Supply Current	I_{SY}	No Load	—	18	22	—	19	25	mA
Peak Load Current	$I_{L(PK)}$		—	70	—	—	70	—	mA
Output Resistance	R_O		—	2	—	—	2	—	Ω
Offset Voltage Nulling Range	ΔV_{OS}	$R_P \geq 1k\Omega$	—	±80	—	—	±80	—	mV
Input Voltage Range (Reduced Accuracy)	IVR		—	±11.5	—	—	±11.5	—	V

NOTES:

1. The BUF-03 package thermal resistance, in still air, is 145 °C/W (45 °C/W junction to case, 100 °C/W case to ambient). The chip temperature of 75 °C is achieved by reducing the case to ambient thermal resistance to 45 °C/W. An inexpensive heat sink, such as the Thermalloy 2271 or 6203, is recommended for use in this application. In addition, if the device is operated in a forced-air environment, or is attached to a PC board which has good thermal conductivity, the chip temperature may be further reduced. If no heat sinking is used, the chip temperature (in still air) may exceed 105 °C. The effect of this elevated temperature will be to increase the input bias current by a factor of eight, increase the V_{OS} specification by TCV_{OS} x 30 °C, and reduce device speed by 10%.
2. Guaranteed by design.
3. Nonlinearity is computed using linear regression techniques with data from five points (e.g., −10V, −5V, 0V, +5V, and +10V for ±10V full-scale linearity).

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$, T_{CHIP} (MAX) = +165° C, device fully warmed-up, unless otherwise noted. (Note 1)

			BUF-03A			BUF-03B			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Slew Rate	SR	$R_L \geq 2k\Omega$, $C_L = 50pF$	—	260	—	—	220	—	V/μsec
Input Offset Voltage	V_{OS}	$R_S \leq 2k\Omega$	—	6	20	—	10	35	mV
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \leq 2k\Omega$ (Note 2)	—	50	100	—	90	170	μV/°C
Input Bias Current	I_B	$T_A = +125°C$	—	25	75	—	30	90	nA
Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_{IN} = \pm 10V$	0.9920	0.9955	—	0.9902	0.9942	—	V/V
Gain Drift with Temperature			—	5	—	—	8	—	ppm/°C
Power Supply Rejection Ratio	PSRR	$V_S = \pm 7V$ to $\pm 15V$	—	0.15	1.26	—	0.20	0.24	mV/V
Supply Current	I_{SY}	$T_A = +125°C$	—	17	21	—	18	24	mA

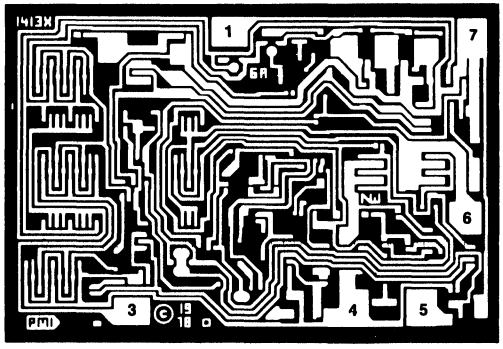
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \leq T_A \leq +70°C$, T_{CHIP} (MAX) = +120° C, device fully warmed-up, unless otherwise noted.

			BUF-03E			BUF-03F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Slew Rate	SR	$R_L \geq 2k\Omega$	—	280	—	—	240	—	V/μsec
Input Offset Voltage	V_{OS}	$R_S \leq 2k\Omega$, $C_L = 50pF$	—	4	14	—	7	28	mV
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \leq 2k\Omega$ (Note 2)	—	40	90	—	80	150	μV/°C
Input Bias Current	I_B	$T_A = +70°C$	—	1.5	5.0	—	1.8	8.0	nA
Voltage Gain ($V_{IN} = \pm 10V$)	A_{VO}	$R_L \geq 2k\Omega$	0.9935	0.9958	—	0.9918	0.9946	—	V/V
Gain Drift with Temperature			—	5	—	—	8	—	ppm/°C
Power Supply Rejection Ratio	PSRR	$V_S = \pm 7V$ to $\pm 15V$	—	0.12	1.0	—	0.16	1.78	mV/V
Supply Current	I_{SY}	$T_A = +70°C$	—	18	22	—	19	25	mA

NOTES:

1. In order to operate the device at an ambient temperature of +125° C, more extensive heat sinking must be used to ensure that the chip temperature never exceeds the absolute maximum of +175° C. The chip temperature of +165° C is achieved by reducing the case to ambient thermal resistance to 30° C/W (e.g., Thermalloy 2227).
2. Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.070 × 0.048 inch

1. NULL
3. INPUT
4. NEGATIVE SUPPLY
5. NULL
6. OUTPUT
7. POSITIVE SUPPLY

Refer to Section 2 for additional DICE informaiton

ELECTRICAL CHARACTERISTICS at $T_j = 25°C$, $V_S = \pm 15V$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	BUF-03N LIMIT	BUF-03G LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	6	15	mV MAX
Slew Rate (Note 1)	SR	$R_L \geq 2k\Omega$, $C_L = 50pF$	250	180	V/μsec MIN
Voltage Gain	A_{VO}	$R_L \geq 10k\Omega$, $V_{IN} = \pm 10V$	0.9960	0.9940	V/V MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 6V$ to $\pm 18V$	0.71	1.42	mV/V MAX
Supply Current	I_{SY}	No Load	22	25	mA MAX

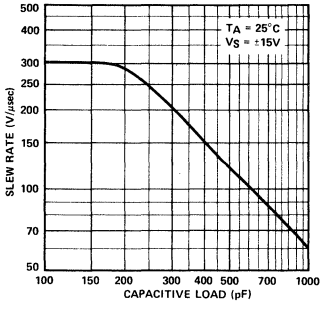
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_j = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	BUF-03N TYPICAL	BUF-03G TYPICAL	UNITS
Peak Load Current	I_L (PK)		70	70	mA
Input Bias Current	I_B		40	60	pA
Input Resistance	R_{IN}		5×10^{11}	5×10^{11}	Ω
Output Resistance	R_O		2	2	Ω
Offset Voltage Nulling Range	ΔV_{OS}	$R_P \geq 1k\Omega$	±80	±80	mV
Input Voltage Range (Reduced Accuracy)	IVR		±11.5	±11.5	V
Power Bandwidth	PBW	$V_{IN} = 10V$ p-p, $R_L \geq 2k\Omega$	9	8	MHz
Bandwidth	BW	$\Delta V_{IN} \leq 2V$ p-p	63	55	MHz
Settling Time	t_S	To 0.1%, ±10V step	90	100	ns
Capacitive Load Capacity	C_{LOAD}	No Oscillations	1	1	μF
Propagation Delay	t_d		7	7	ns
Rise Time	t_r	$\Delta V_{IN} = 0.5V$	7	7	ns
Wide Band Input Noise Voltage	V_n	DC to 50MHz	350	400	μV_{RMS}
Input Noise Voltage Density	e_n	f = 10kHz	50	60	$nV/\sqrt{Hz}$

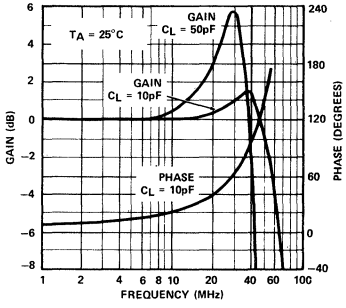
NOTE:
1. Sample tested.

TYPICAL PERFORMANCE CURVES

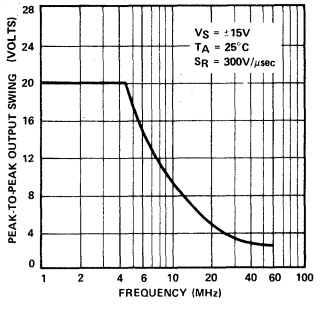
SLEW RATE vs CAPACITIVE LOAD



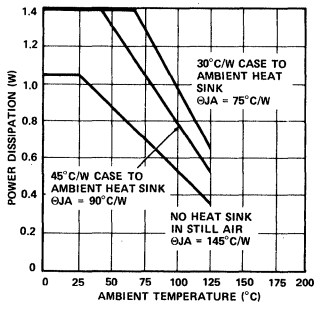
GAIN AND PHASE RESPONSE vs FREQUENCY



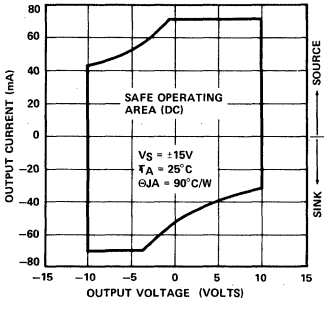
LARGE SIGNAL FREQUENCY RESPONSE



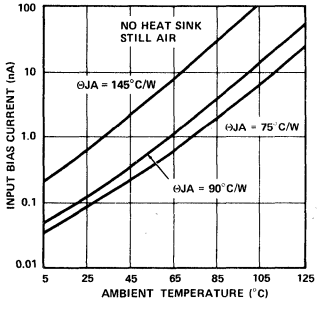
MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



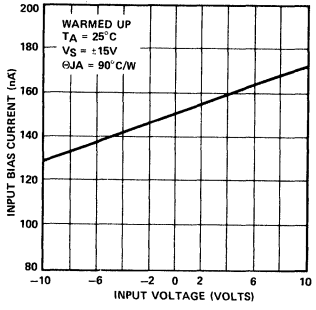
OUTPUT CURRENT vs OUTPUT VOLTAGE



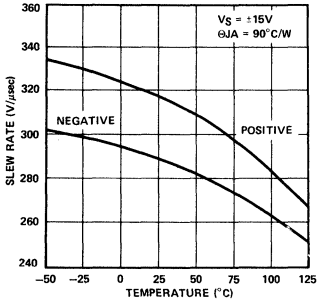
INPUT BIAS CURRENT vs TEMPERATURE (WARMED-UP)



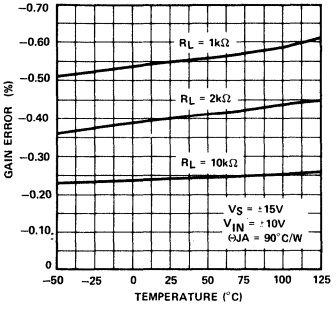
INPUT BIAS CURRENT vs INPUT VOLTAGE



SLEW RATE vs TEMPERATURE

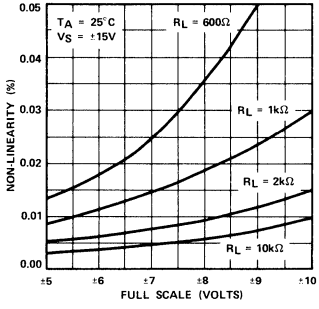


GAIN ERROR vs TEMPERATURE

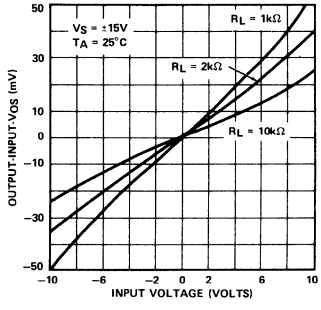


TYPICAL PERFORMANCE CURVES

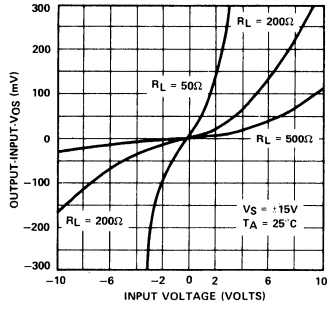
NON-LINEARITY vs FULL-SCALE VOLTAGE



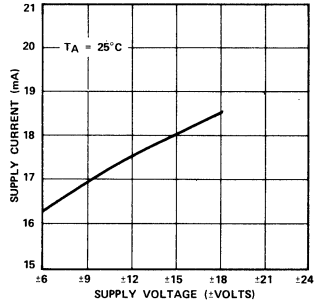
GAIN ERROR vs INPUT VOLTAGE



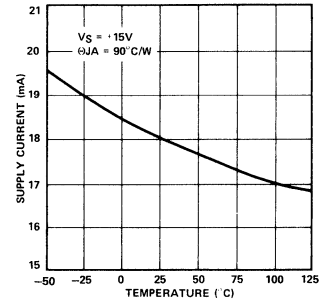
GAIN ERROR vs INPUT VOLTAGE



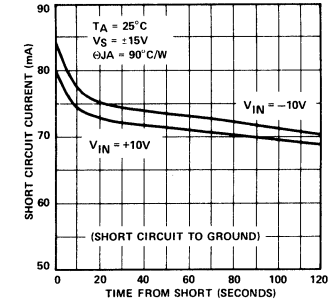
SUPPLY CURRENT vs SUPPLY VOLTAGE



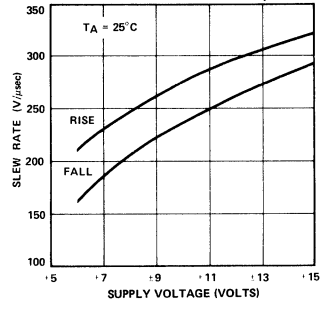
SUPPLY CURRENT vs TEMPERATURE



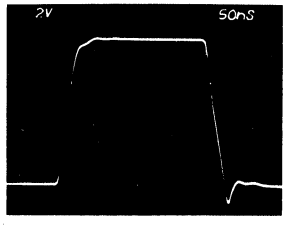
OUTPUT SHORT CIRCUIT CURRENT vs TIME



SLEW RATE vs SUPPLY VOLTAGE



SLEW RATE

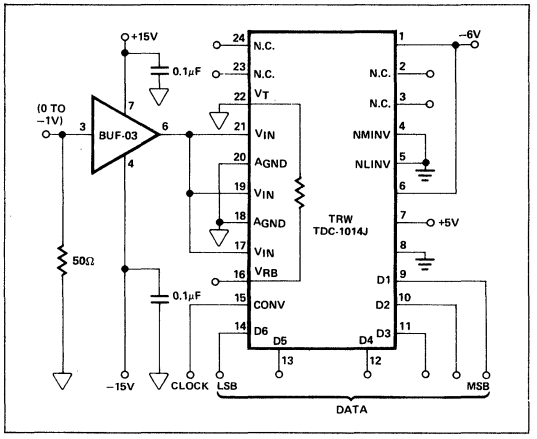


APPLICATIONS INFORMATION

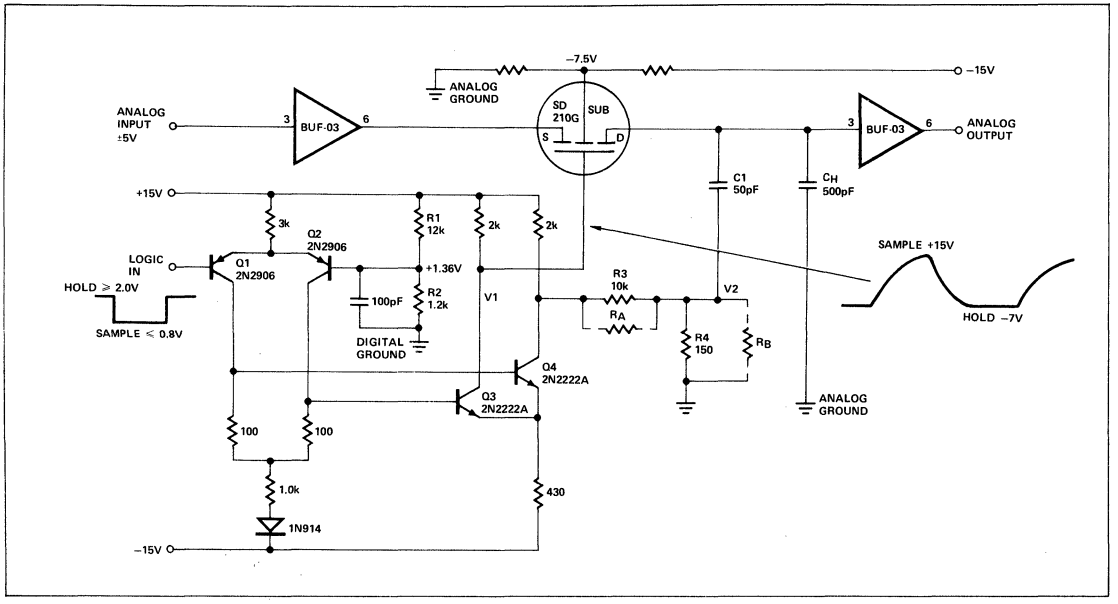
OPERATING THE BUF-03 AT REDUCED POWER SUPPLIES

In most video applications the signal levels are significantly lower than the 20V peak-to-peak capability of the BUF-03. This suggests operating the BUF-03 at reduced power supplies; for example, at ±6V supplies ±2V signals can be handled. The obvious advantage of reduced supplies is the accompanying decrease in power dissipation: from a typical 540 mW (=30V x 18 mA) to 195 mW (=12V x 16.2 mA) at ±6V. At lower supply voltages heat sinking is no longer necessary. However, as shown on the slew rate vs supply voltage curve, slew rate does degrade at lower supplies. This occurs because of higher internal node capacitances at lower voltages and because of the slightly decreased operating current.

HIGH SPEED 6-BIT A/D BUFFER



HIGH-SPEED SAMPLE/HOLD AMPLIFIER



SECTION 7

COMPARATORS

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COMPARATORS

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INTRODUCTION

A comparator provides a logic output indicating the amplitude relationship between two analog signal inputs.

When selecting a comparator, certain device parameters must be considered for proper design and application. These parameters are:

- V_{OS} (Input Offset Voltage)
- Response Time
- Slew Rate and Response Time
- PSRR (Power Supply Rejection)
- I_B (Input Bias Current)
- CMVR (Common-Mode Voltage Range)
- Output Configuration
- Voltage Gain

The input offset voltage (V_{OS}) for a comparator should be as small as possible because in a high gain circuit it is the dominating factor that determines the exact threshold level. For this reason, comparators should be nulled or a Precision Comparator used so that the input differential voltage is as close to zero as practical when the output is at the logic switching threshold.

The voltage gain (A_V) determines the sensitivity and threshold accuracy of a comparator. For the ideal comparator, the gain could be considered infinite; and an extremely small voltage applied between the two inputs will cause a change in the output. In practice, some minimum voltage variation will be required at the input to effect a change in the output state. This minimum sensitivity will be determined from the voltage gain of the comparator. The relationship is as follows:

$$\Delta V_{IN(MIN)} = \frac{\Delta V_O}{A_V}$$

The quantity ΔV_O which is the difference between the high and low state of the output is generally chosen to be 2.5V to insure the matching of the comparator with the TTL load.

Precision Monolithic's comparator product line has expanded to five devices.

The CMP01 is a fast precision comparator with low offset voltage. The CMP02 offers the CMP01's offset voltage performance along with lower input bias currents.

The quad CMP04 offers both low power and low offset voltages. Existing "139" type applications can be upgraded by the pin compatible CMP04. The PM139/239/339 devices provide equal performance to "139/239/339" type comparators.

The CMP05 brings together superior input specifications with very fast response times. This combination makes the CMP05 the ideal choice in high-accuracy 10 and 12-bit data systems.

COMPARATOR DEFINITIONS

COMMON MODE REJECTION RATIO (CMRR)

The ratio, expressed in dB, of the change in the arithmetic mean of voltage present at the device inputs with respect to the device reference ground (Δ common mode voltage) to the change in input offset voltage (ΔV_{OS}).

$$CMRR\ (dB) = 20\log\ (\Delta CMV/\Delta V_{OS})$$

COMMON-MODE VOLTAGE RANGE (CMVR)

The range of common mode voltage on the input terminals for which operation within specifications is assured.

DIFFERENTIAL INPUT RESISTANCE (R_{IN})

The resistance looking into either input terminal with the other grounded.

DIFFERENTIAL INPUT VOLTAGE

The range of voltage between the input terminals for which operation within specifications is assured.

INPUT BIAS CURRENT (I_B)

The average of the two input currents, with the inputs tied together.

INPUT OFFSET CURRENT (I_{OS})

The difference in the currents into the two input terminals when the output is within a specified voltage range.

INPUT OFFSET VOLTAGE (V_{OS})

The voltage between the input terminals when the output is within a specified voltage range.

INPUT SLEW RATE

The maximum rate of change in differential and/or common-mode input voltage which the input stage can follow. The comparator's total response time for any input voltage step with arbitrary overdrive is equal to the sum of the response time for the small signal (100mV) step with the same overdrive, plus the slewing time (=initial differential input voltage divided by input slew rate).

INPUT TO OUTPUT HIGH PROPAGATION DELAY (tpd+)

The time measured between the input signal's V_{OS} crossing and the output voltage's 50% low-to-high transition point. Specified for given input voltage step size and overdrive.

INPUT TO OUTPUT LOW PROPAGATION DELAY (tpd−)

The time measured between the input signal's V_{OS} crossing and the output voltage's 50% high-to-low transition point. Specified for a given input voltage step size and overdrive.

LATCH DISABLE PROPAGATION DELAY (t_{LPD})

The time measured between the 50% transition points of the latch enable signal's high-to-low transition and the output signal's low-to-high or high-to-low transition point.

LATCH SET-UP TIME (t_S)

The minimum time required before the low-to-high latch enable signal transition that an input signal change can occur and still be recognized and held at the output. Specified for a given input voltage step size and overdrive.

OFFSET VOLTAGE ADJUSTMENT RANGE

The change in offset voltage that can be obtained by adjusting a specified external nulling potentiometer.

OUTPUT LEAKAGE CURRENT (I_{LEAK})

The current into the output terminal with a given output voltage and input drive equal to or greater than a specified value.

OUTPUT SINK CURRENT (I_{SINK})

The maximum negative current that can be delivered by the comparator.

OVERDRIVE

The input step voltage of specified size drives the comparator from some initial input voltage to an input level just barely in excess of that required to bring the output from its high or low state to the logic threshold voltage. This excess is defined as the voltage overdrive.

POSITIVE OUTPUT VOLTAGE (V_{OH})

The high output voltage level with a given load and input drive equal to or greater than a specified value.

POWER SUPPLY REJECTION RATIO (PSRR)

The ratio of the maximum change in input offset voltage to the specified change in power supply voltage.

RESPONSE TIME (t_r)

The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. Logic threshold is defined as the voltage at the output of the comparator at which the loading logic circuitry changes its digital state, or, as 1.4V when the loading logic circuitry is not used.

SATURATION VOLTAGE (V_{SAT})

The low output voltage level with a given sink current and drive less than or equal to a specified value.

STROBE CURRENT (I_{STB})

The current out of the strobe terminal when it is active.

STROBED OUTPUT VOLTAGE ($V_{O(STB)}$)

The DC output voltage — independent of input conditions — with the strobe function active.

SUPPLY CURRENTS

The currents required from the positive or negative supplies to operate the comparator with no output load. The currents will vary with input voltage, but are maximum when the output is low, and, therefore, are specified with the input drive less than or equal to a given value.

VOLTAGE GAIN (A_V)

The ratio of the change in output voltage (over a specified range) to the change in input voltage producing it.

CMP-01

FAST PRECISION COMPARATOR

FEATURES

- **Fast Response Time .. 110ns Typical, 180ns Maximum**
- **High Input Slew Rate 92V/μs**
- **Low Offset Voltage ... 0.3mV Typical, 0.8mV Maximum**
- **Low Offset Current ..... 4nA Typical, 25nA Maximum**
- **Low Offset Drift ..... 1.0μV/°C, 30pA/°C**
- **Standard Power Supplies ..... ±5V to ±18V**
- **Guaranteed Operation from Single +5V Supply**
- **No Pull-Up Resistor Required for TTL Drive**
- **Wired OR Capability**
- **Fits 111, 106, 710 Sockets**
- **Easy Offset Nulling ..... Single 2kΩ Potentiometer**
- **Easy to Use ..... Free from Oscillations**

GENERAL DESCRIPTION

The CMP-01 is a monolithic fast precision voltage comparator using an advanced compatible NPN-Schottky Barrier Diode process. It features fast response time to both large and small input signals, while maintaining excellent input characteristics. The CMP-01 is capable of operating over a wide range of supply voltages including single ended 5 volt supply. The large output current sinking and high output voltage capability assure good application flexibility, while the combination of fast response, high accuracy, and freedom from oscillation assure performance in precision level detectors and 12 and 13-bit A/D converters. The CMP-01 is pin-compatible to earlier 111, 106, and 710 types. For applications requiring lower input offset and bias currents, refer to the CMP-02 data sheet.

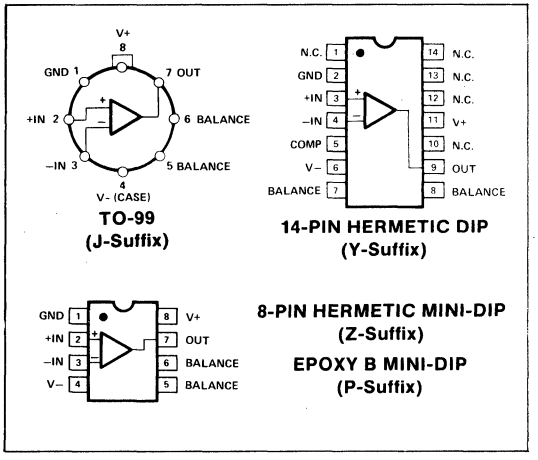
ORDERING INFORMATION†

	PACKAGE				
	HERMETIC			PLASTIC	
+25°C		DIP		DIP	OPERATING
V_{OS} (mV)	TO-99 8 Pin	8 Pin	14 Pin	8 Pin	TEMPERATURE RANGE
0.8	CMP01J*	CMP01Z*	CMP01Y*	——	MIL
	CMP01EJ	CMP01EZ	CMP01EY	CMP01EP	COM
2.8	CMP01BJ*	CMP01BZ*	CMP01BY*	——	MIL
	CMP01CJ	CMP01CZ	CMP01CY	CMP01CP	COM

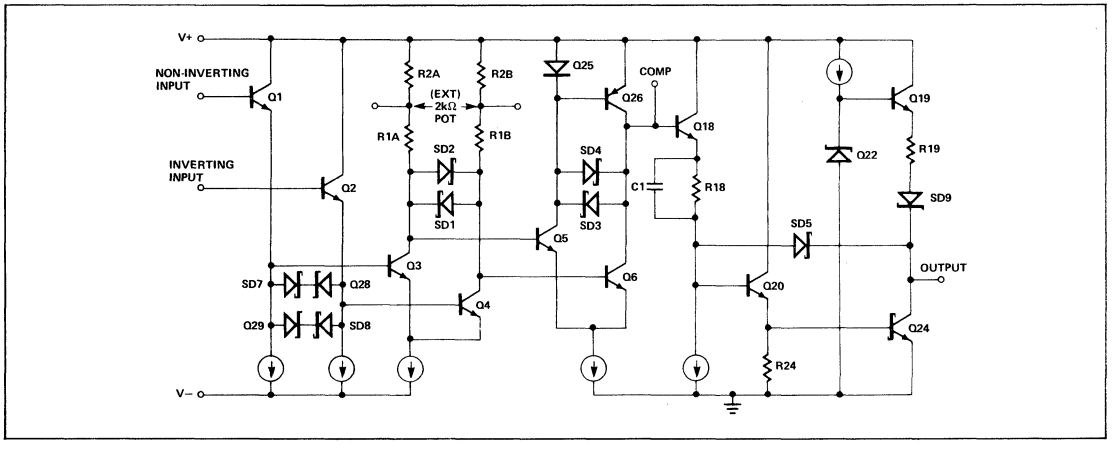
*Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

†All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 2)

Total Supply Voltage, V+ to V− 36V
Output to Ground ..... -5V to +32V
Output to Negative Supply Voltage 50V
Ground to Negative Supply Voltage 30V
Positive Supply Voltage to Ground ..... + 30V
Positive Supply Voltage to Offset Null ..... 0 to 2V
Power Dissipation (See Note) 500mW
Differential Input Voltage ..... ±11V
Input Voltage (V_S = ±15V) ..... ±15V
Output Sink Current (Continuous Operation) 75mA
Operating Temperature Range —
CMP-01, CMP-01B ..... -55°C to +125°C
CMP-01E, CMP-01C ..... 0°C to +70°C
DICE Junction Temperature (T_j) ..... −65°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Output Short Circuit Duration — to ground .... Indefinite
to V+ ..... 1 Minute

NOTES:
1. Maximum package power dissipation vs. ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J) — 8-Pin	80°C	7.1mW/°C
Dual-in-Line (Y) — 14-Pin	100°C	10.0mW/°C
Epoxy Mini-Dip (P) — 8-Pin	36°C	5.6mW/°C
Hermetic Mini-Dip (Z) — 8-Pin	75°C	6.7mW/°C

2. Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V_S = ± 15V, T_A = 25°C, unless otherwise noted.

			CMP-01 CMP-01E			CMP01B CMP01C			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	—	0.3	0.8	—	0.4	2.8	mV
Input Offset Current	I_{OS}	(Note 1)	—	4	25	—	5	80	nA
Input Bias Current	I_B		—	350	600	—	400	900	nA
Differential Input Resistance	R_{IN}	(Note 2)	3.0	14	—	1.0	10	—	mΩ
Voltage Gain	A_V	V_O = 0.4V to 2.4V (Notes 1 and 2)	200	500	—	100	500	—	V/mV
Response Time	t_r	100mV step, 5mV overdrive							ns
		No Load (No Pull-Up) (Note 3)	—	110	180	—	110	180	
		5kΩ to 5V (Pull-Up)	—	110	—	—	110	—	
		TTL Fan-Out = 4, No Pull-Up	—	110	—	—	110	—	
		5V Step 5mV Overdrive							
		No Load (No Pull-Up)	—	160	—	—	160	—	
		5kΩ to 5V (Pull-Up)	—	160	—	—	160	—	
		TTL Fan-Out = 4, No Pull-Up	—	160	—	—	160	—	
Input Slew Rate			—	92	—	—	92	—	V/μs
Input Voltage Range	CMVR		±12.5	±13.0	—	±12.5	±13.0	—	V
Common Mode Rejection Ratio	CMRR		94	110	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 18V$, $-18V \leq V_{S-} \leq 0V$	80	100	—	74	98	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \geq 3mV$, I_O = 320μA	2.4	3.2	—	—	—	—	V
		$V_{IN} \geq 3mV$, I_O = 240μA	—	—	—	2.4	3.4	—	
		$V_{IN} \geq 3mV$, I_O = 0mA	2.4	4.8	—	2.4	4.8	—	
Saturation Voltage	V_{OL}	$V_{IN} \leq -10mV$, I_{sink} = 0A	—	0.16	0.4	—	0.16	0.4	V
		$V_{IN} \leq -10mV$, $I_{sink} \leq 6.4mA$	—	0.3	0.45	—	0.31	0.45	
		$V_{IN} \leq -10mV$, $I_{sink} \leq 12mA$ (CMP-01 only)	—	0.36	0.5	—	—	—	
Output Leakage Current	I_{LEAK}	$V_{IN} \geq 10mV$, V_O = + 30V	—	0.03	2.0	—	0.05	8.0	μA
Positive Supply Current	I+	$V_{IN} \leq -10mV$	—	5.6	8.0	—	5.6	8.5	mA
Negative Supply Current	I−	$V_{IN} \leq -10mV$	—	1.3	2.2	—	1.3	2.2	mA
Power Dissipation	P_d	$V_{IN} \leq -10mV$	—	103	153	—	103	161	mW
Offset Voltage Adjustment Range		Nulling Pot ≥ 2kΩ	—	±5	—	—	±5	—	mV

NOTES:
1. These Parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
2. Guaranteed by design.
3. Sample tested.

ELECTRICAL CHARACTERISTICS at $V_S+ = 5V$, $V_S- = 0V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-01 CMP-01E MIN	CMP-01 CMP-01E TYP	CMP-01 CMP-01E MAX	CMP01B CMP01C MIN	CMP01B CMP01C TYP	CMP01B CMP01C MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	—	0.4	1.5	—	0.5	3.5	mV
Input Offset Current	I_{OS}	(Note 1)	—	3	21	—	4	65	nA
Input Bias Current	I_B		—	250	500	—	300	720	nA
Voltage Gain	A_V	V_O = 0.4V to 2.4V (Notes 1 and 2)	—	50	—	—	50	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive 5kΩ to 5V (Pull-Up) TTL Fan-Out = 4, 5kΩ to 5V (Pull-Up)	— —	150 150	— —	— —	150 150	— —	ns
Input Voltage Range	CMVR		1.8	1.7-3.8	3.5	1.8	1.7-3.8	3.5	V
Saturation Voltage	V_{OL}	$V_{IN} \leq -10mV$, $I_{sink} \leq 6.4mA$	—	0.3	0.45	—	0.3	0.45	V
Positive Supply Current	I+	$V_{IN} \leq -10mV$	—	2.3	3.2	—	2.4	3.8	mA
Power Dissipation	P_d	$V_{IN} \leq -10mV$	—	11.5	16.0	—	12.0	19.0	mW

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-01 MIN	CMP-01 TYP	CMP-01 MAX	CMP-01B MIN	CMP-01B TYP	CMP-01B MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1) $V_{S-} = 5V$, $V_{S-} = 0V$ (Note 1)	— —	0.5 0.6	1.6 2.8	— —	0.5 0.6	3.5 4.3	mV
Average Input Offset Voltage Drift Without External Trim With External Trim	 TCV_{OS} TCV_{OSn}	 $R_S = 50\Omega$	 — —	 1.5 1.0	 — —	 — —	 1.8 1.2	 — —	μV/°C
Input Offset Current	I_{OS}	T_A = +125°C (Note 1) T_A = −55°C (Note 1)	— —	4 5	25 45	— —	5 6	80 120	nA
Average Input Offset Current Drift	TCI_{OS}	+25°C ≤ T_A ≤ +125°C −55°C ≤ T_A ≤ +25°C	— —	12 35	— —	— —	12 40	— —	pA/°C
Input Bias Current	I_B	T_A = +125°C T_A = −55°C	— —	330 550	600 1400	— —	340 450	900 1200	nA
Voltage Gain	A_V	V_O = 0.4V to 2.4V (Notes 1 and 2)	100	500	—	70	500	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive T_A = +125°C No Load T_A = −55°C, No Load	— —	220 100	— —	— —	220 100	— —	ns
Input Voltage Range	CMVR		±12.0	±13.0	—	±12.0	±13.3	—	V
Common Mode Rejection Ratio	CMRR		88	106	—	86	108	—	dB
Power Supply Rejection Ratio	PSRR	5V ≤ V_{S+} ≤ 15V, −15V ≤ V_{S-} ≤ 0V	75	96	—	70	88	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \geq 4mV$, $I_O = 200\mu A$	2.4	3.0	—	2.4	3.2	—	V
Saturation Voltage	V_{OL}	$V_{IN} \leq -10mV$, I_{sink} = 0 $V_{IN} \leq -10mV$, I_{sink} = 6.4mA	— —	0.20 0.32	0.4 0.5	— —	0.17 0.31	0.4 0.5	V

NOTES:

1. These Parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
2. Guaranteed by design.

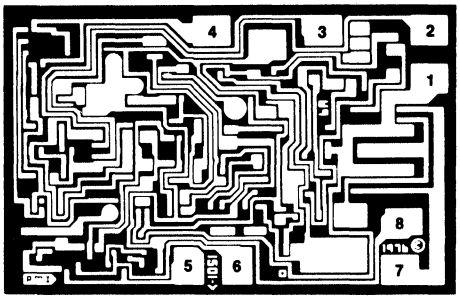
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \leq T_A \leq 70°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-01E MIN	CMP-01E TYP	CMP-01E MAX	CMP-01C MIN	CMP-01C TYP	CMP-01C MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1) $V_{S+} = 5V$, $V_{S+} = 0V$ (Note 1)	— —	0.4 0.5	1.4 2.4	— —	0.5 0.6	3.5 4.3	mV
Average Input Offset Voltage Drift Without External Trim With External Trim	 TCV_{OS} TCV_{OSn}	 $R_S = 50\Omega$	 — —	 1.5 1.0	 — —	 — —	 1.8 1.2	 — —	μV/°C
Input Offset Current	I_{OS}	$T_A = +70°C$ (Note 1) $T_A = 0°C$ (Note 1)	— —	4 5	25 45	— —	5 6	80 120	nA
Average Input Offset Current Drift	TCI_{OS}	$+25°C \leq T_A \leq +70°C$ $0°C \leq T_A \leq +25°C$	— —	12 35	— —	— —	12 40	— —	pA/°C
Input Bias Current	I_B	$T_A = +70°C$ $T_A = 0°C$	— —	330 400	600 950	— —	340 450	900 1200	nA
Voltage Gain	A_V	$V_O = 0.4V$ to $2.4V$ (Notes 1 and 2)	100	500	—	70	500	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive $T_A = +70°C$, No Load $T_A = 0°C$, No Load	 — —	 220 100	 — —	 — —	 220 100	 — —	ns
Input Voltage Range	CMVR		±12.0	±13.3	—	±12.0	±13.3	—	V
Common Mode Rejection Ratio	CMRR		90	108	—	86	108	—	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 15V$, $-15V \leq V_{S-} \leq 0V$	77	98	—	70	88	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \geq 4mV$, $I_O = 200\mu A$	2.4	3.2	—	2.4	3.2	—	V
Saturation Voltage	V_{SAT}	$V_{IN} \leq -10mV$, $I_{sink} = 0$ $V_{IN} \leq -10mV$, $I_{sink} = 6.4mA$	— —	0.17 0.3	0.4 0.5	— —	0.17 0.31	0.4 0.5	V

NOTES:

1. These Parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
2. Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.065 × 0.042 inch

1. GROUND
2. NON-INVERTING INPUT
3. INVERTING INPUT
4. NEGATIVE SUPPLY
5. BALANCE
6. BALANCE
7. OUTPUT
8. POSITIVE SUPPLY

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$ at 25° C.

PARAMETER	SYMBOL	CONDITIONS	CMP-01N LIMIT	CMP-01GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	0.8	2.8	mV MAX
Input Offset Current	I_{OS}		25	80	nA MAX
Input Bias Current	I_B		600	900	nA MAX
Differential Input Resistance	R_{IN}	(Note 2)	3.0	1.0	MΩ MIN
Input Voltage Range	IVR		±12.5	±12.5	V MIN
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm$CMVR	94	90	dB MIN
Power Supply Rejection Ratio	PSRR	$5V \leq V_S+ \leq 18V$ $-18V \leq V_S- \leq 0V$	80	74	dB MIN
Positive Output Voltage	V_{OH}	$V_{IN} \geq 3mV$, $I_O = 320\mu A$ $V_{IN} \geq 3mV$, $I_O = 240\mu A$	2.4 —	— 2.4	V MIN
Saturation Voltage	V_{OL}	$I_{sink} = 6.4mA$	0.45	0.45	V MAX
Output Leakage Current	I_{LEAK}	$V_{IN} \geq 10mV$, $V_O = 30V$	4.0	8.0	μA MAX
Positive Supply Current	I+	$V_{IN} \leq -10mV$	8.0	8.5	mA MAX
Negative Supply Current	I–	$V_{IN} \leq -10mV$	2.2	2.2	mA MAX
Power Consumption	P_d	$V_{IN} \leq -10mV$	153	161	mW MAX

NOTES:
1. These Parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
2. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S+ = 5V$ and $V_S- = 0V$ at 25° C.

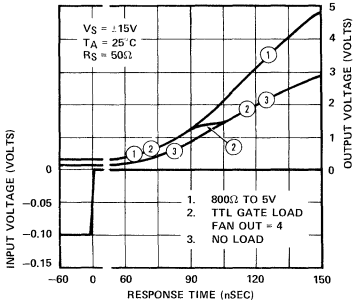
PARAMETER	SYMBOL	CONDITIONS	CMP-01N LIMIT	CMP-01GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$	1.5	3.5	mV MAX
Input Offset Current	I_{OS}		21	65	nA MAX

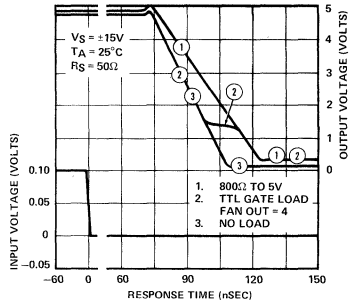
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm$ 15V, and 25° C.

PARAMETER	SYMBOL	CONDITIONS	CMP-01N TYPICAL	CMP-01GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$ (Note 1)	1.5	1.8	μV/° C
Average Input Offset Current Drift	TCI_{OS}		35	40	pA/° C
Response Time	t_r	100mV Step, 5mV Overdrive No Load (No Pull-Up)	100	100	ns

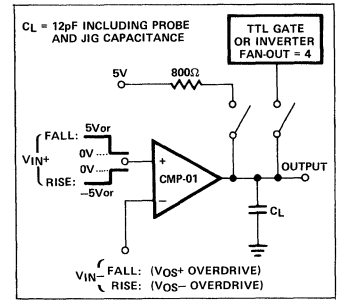
TYPICAL PERFORMANCE CURVES

RESPONSE TIME, 100mV STEP, 5mV OVERDRIVE, VARIOUS LOADS

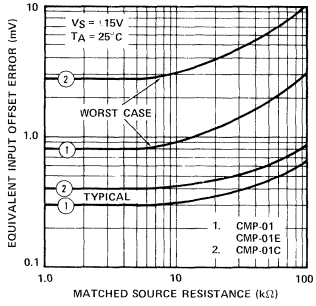




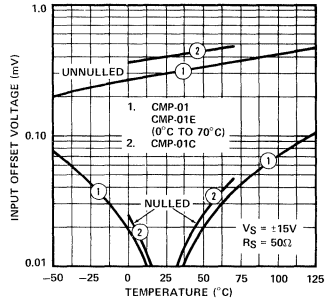
RESPONSE TIME TEST CIRCUIT



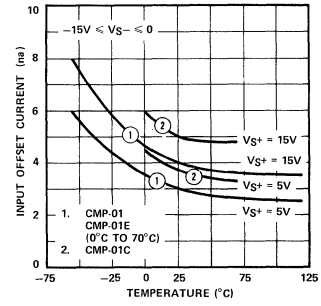
INPUT OFFSET ERROR vs SOURCE RESISTANCE



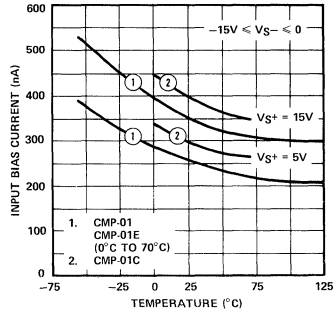
OFFSET VOLTAGE vs TEMPERATURE



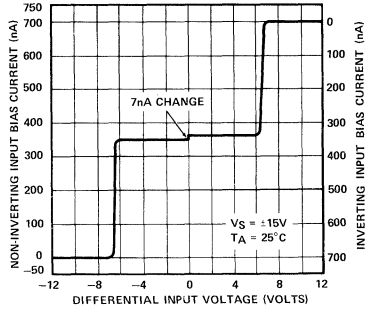
INPUT OFFSET CURRENT vs TEMPERATURE



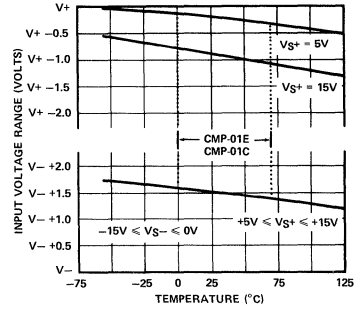
INPUT BIAS CURRENT vs TEMPERATURE



INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE

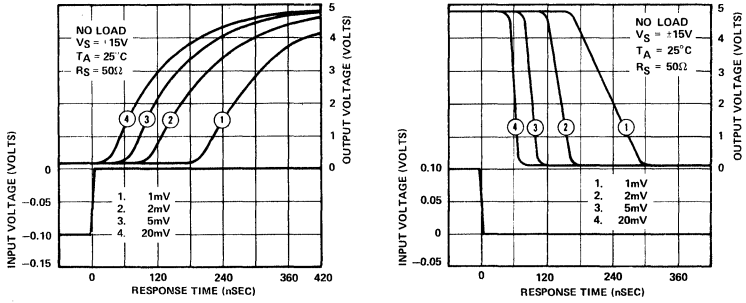


INPUT VOLTAGE RANGE vs TEMPERATURE

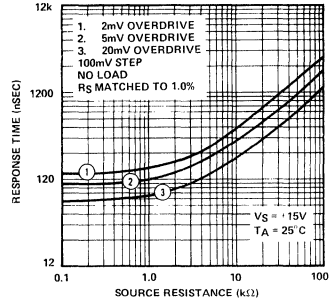


TYPICAL PERFORMANCE CURVES

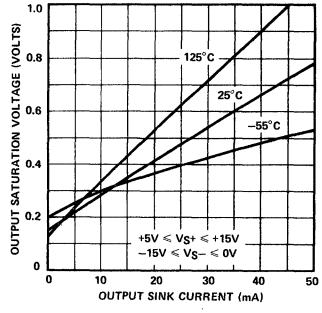
RESPONSE TIME FOR 100mV STEP AND VARIOUS INPUT OVERDRIVES



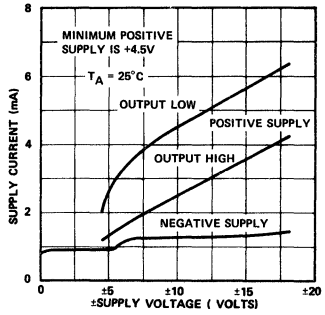
RESPONSE TIME vs SOURCE RESISTANCE



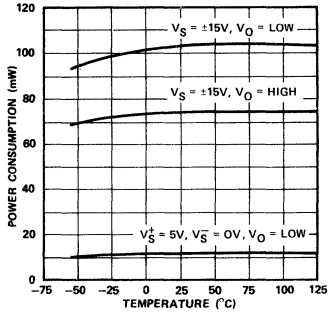
SATURATION VOLTAGE vs SINK CURRENT



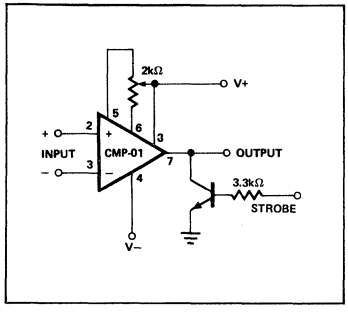
SUPPLY CURRENT vs SUPPLY VOLTAGE



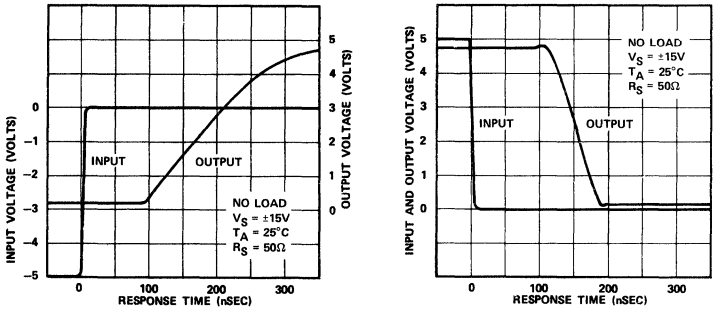
POWER CONSUMPTION vs TEMPERATURE



OFFSET TRIMMING AND STROBE CIRCUIT

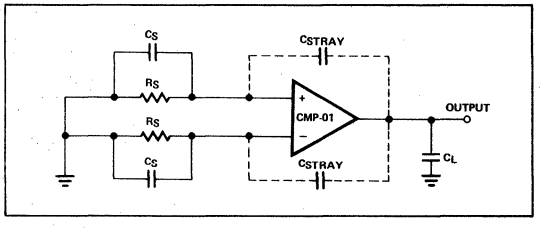


RESPONSE TIME FOR 5V STEP AND 5mV OVERDRIVE



APPLICATION NOTES

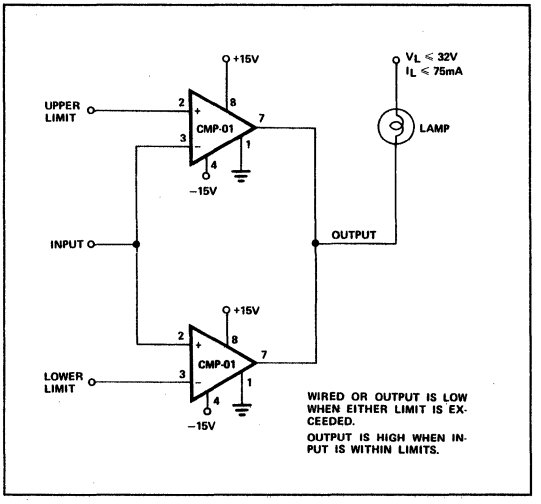
The CMP-01 provides fast response times even with small input overdrives; to achieve this performance requires very high gain at high frequencies. The CMP-01 is completely free of oscillations; however, small values of stray capacitance from output to input when combined with high-source resistances can cause an unstable condition. DC characteristics are not affected, but when the input is within a few microvolts of the transition level, certain conditions can create an oscillation region. The width of this oscillatory region and the size of source resistance where oscillations begin is a strong function of the stray coupling present. The following suggestions are offered as a guide towards minimizing the conditions for oscillation: matched source resistors, minimized stray capacitances (e.g., a ground plane between output and input), capacitive output loading (C_L), or a capacitor from the compensation terminal to AC ground (DIP only). The capacitive loading techniques will eliminate the oscillations, but result in slower response time. Positive resistive feedback creating a hysteresis condition can be very effective — see level detector below. Matched bypass capacitors across the input resistors also can eliminate the instability,



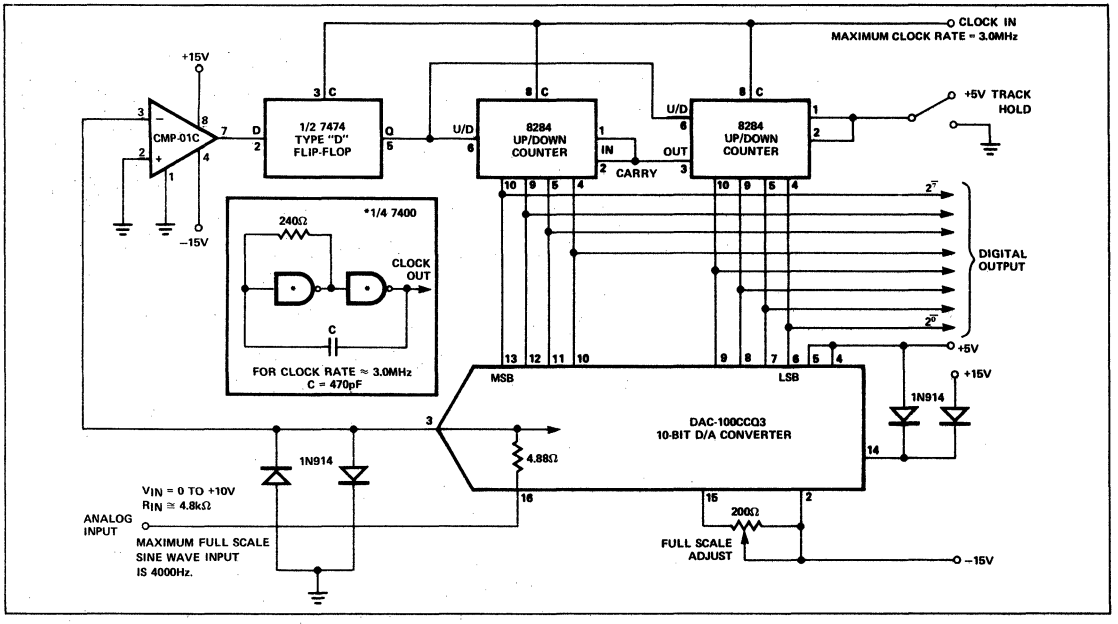
and if $C_S \geq 20pF$ $\frac{\text{maximum step size}}{\text{minimum overdrive}}$

the response time will approximate the response time for low values of R_S. It should be noted that the offset nulling terminals do not require bypassing for stability. As with all wideband circuits, it is recommended that the supplies be bypassed near the socket of the device.

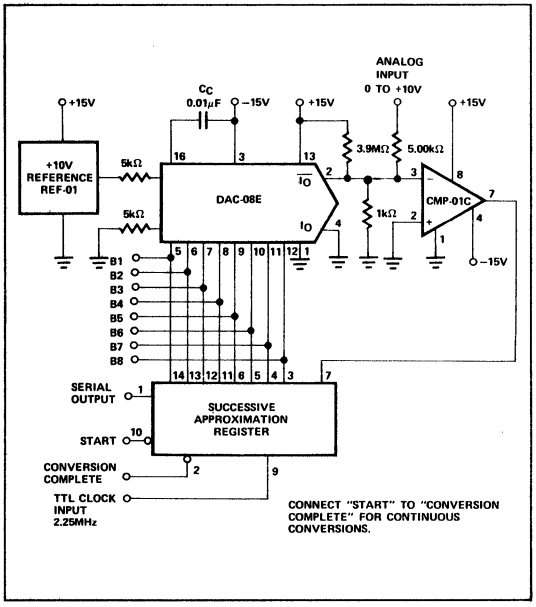
PRECISION, DUAL LIMIT, GO/NO GO TESTER



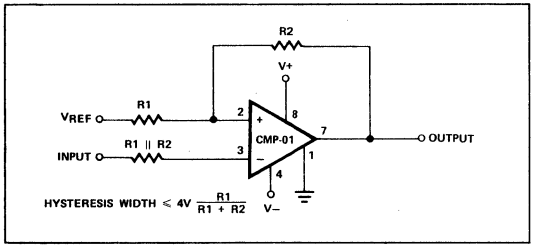
8-BIT TRACKING A/D CONVERTER



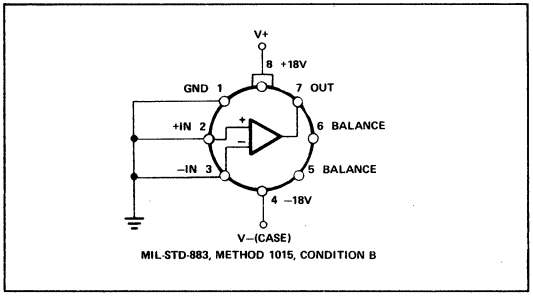
3 IC LOW COST A/D CONVERTER



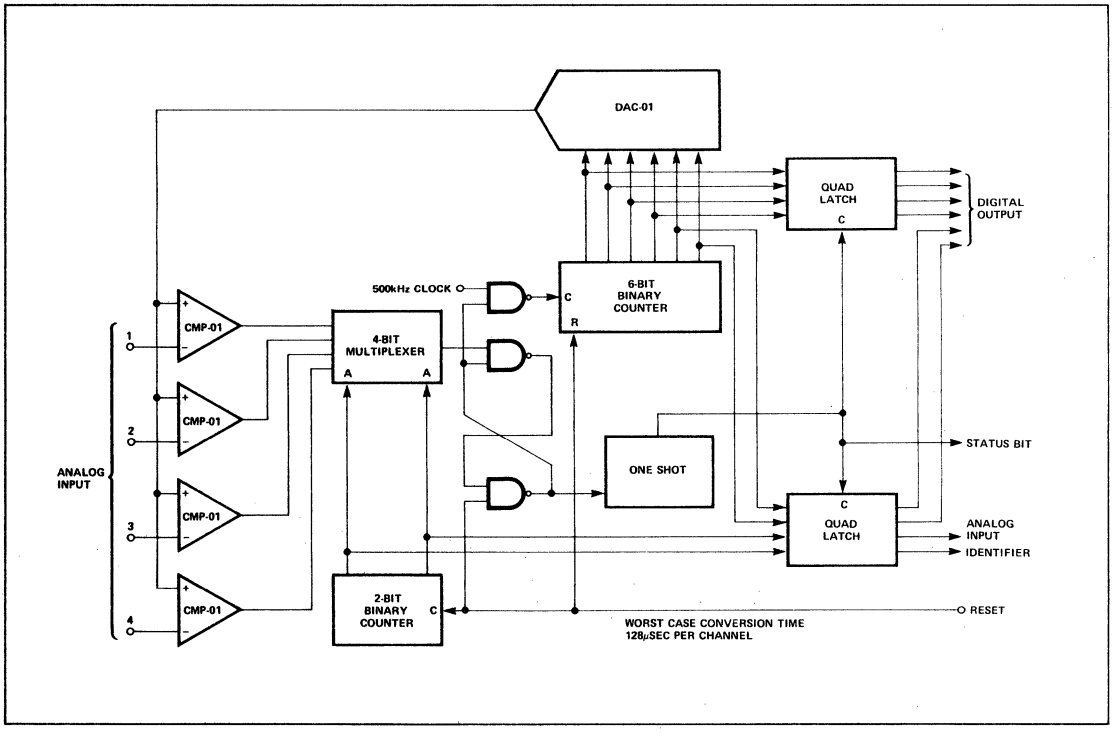
LEVEL DETECTOR WITH HYSTERESIS(Positive Feedback)



BURN-IN CIRCUIT



4-CHANNEL DIGITALLY MULTIPLEXED RAMPED A/D CONVERTER



CMP-02

LOW INPUT CURRENT PRECISION COMPARATOR

FEATURES

- **Low Offset Voltage ... 0.3mV Typical, 0.8mV Maximum**
- **Low Offset Current .... 0.3nA Typical, 3.0nA Maximum**
- **Low Bias Current ..... 28nA Typical, 50nA Maximum**
- **Low Offset Drift ..... 1.0μV/°C, 4pA/°C**
- **High Gain ..... 200,000 Minimum**
- **High CMRR ..... 110dB Typical, 94dB Minimum**
- **High Input Impedance 16MΩ**
- **Fast Response Time .. 190ns Typical, 270ns Maximum**
- **Standard Power Supplies ..... ±5V to ±18V**
- **Guaranteed Operation from Single +5V to ±18V**
- **No Pull-Up Resistor Required for TTL Drive**
- **Wired-OR Capability**
- **Fits 111, 106, 710 Sockets**
- **Easy Offset Nulling ..... Single 2kΩ Potentiometer**
- **Easy to Use ..... Free from Oscillations**

GENERAL DESCRIPTION

The CMP-02 is a monolithic low input current comparator using an advanced compatible NPN-Schottky Barrier Diode process. It features superior input characteristics with extremely low offset voltage, offset current, bias current and temperature drift. High common mode and power supply rejection plus good response time contribute to excellent performance in the most demanding applications. The balanced offset nulling, large output drive, and wired-OR capability combined with internal pull-up maximize application convenience. The CMP-02 is capable of operating over a wide range of supply voltages, including single plus 5 volt supply operation, and is pin-compatible to earlier 111, 106, and 710 types. For applications requiring faster response time, please refer to the CMP-01 Fast Precision Comparator data sheet.

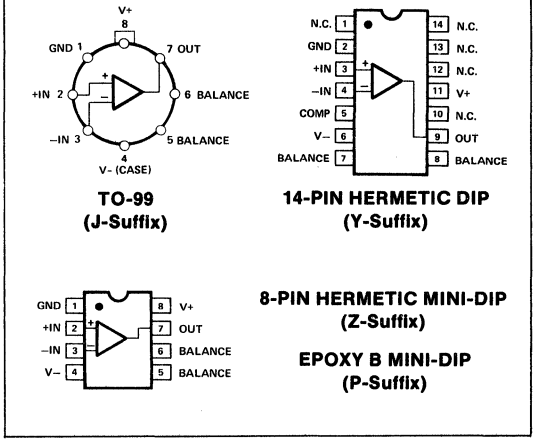
ORDERING INFORMATION†

+25°C V_{OS} (mV)	PACKAGE: HERMETIC TO-99 8 Pin	HERMETIC DIP 8 Pin	HERMETIC DIP 14 Pin	PLASTIC DIP 8 Pin	OPERATING TEMPERATURE RANGE
0.8	CMP02J*	CMP02Z*	CMP02Y*	——	MIL
	CMP02EJ	CMP02EZ	CMP02EY	CMP02EP	COM
2.8	CMP02BJ*	CMP02BZ*	CMP02BY*	——	MIL
	CMP02CJ	CMP02CZ	CMP02CY	CMP02CP	COM

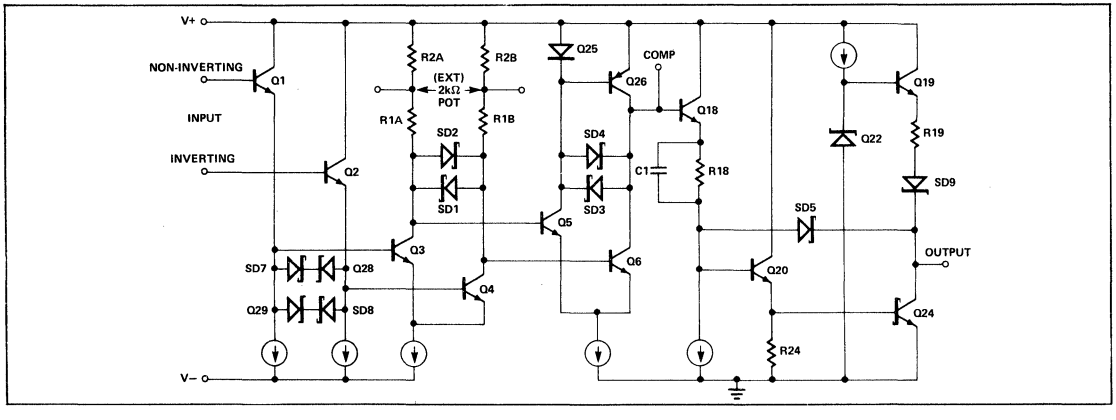
*Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

†All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 2)

Total Supply Voltage, V+ to V- 36V
Output to Ground ..... -5V to +32V
Output to Negative Supply Voltage 50V
Ground to Negative Supply Voltage 30V
Positive Supply Voltage to Ground 30V
Positive Supply Voltage to Offset Null ..... 0 to 2V
Power Dissipation (See Note) 500mW
Differential Input Voltage ..... ±11V
Input Voltage (V_S = ±15V) ..... ±15V
Output Sink Current (Continuous Operation) 75mA
Operating Temperature Range —
CMP-01, CMP-01B ..... -55°C to +125°C
CMP-01E, CMP-01C ..... 0°C to +70°C
DICE Junction Temperature (T_j) ..... -65°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Output Short Circuit Duration — to ground .... Indefinite
to V+ ..... 1 Minute

NOTES:
1. Maximum package power dissipation vs. ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J) — 8-Pin	80°C	7.1mW/°C
Dual-in-Line (Y) — 14-Pin	100°C	10.0mW/°C
Mini-Dip (P) — 8-Pin	36°C	5.6mW/°C
Hermetic Mini-DIP (Z) — 8-Pin	75°C	6.7mW/°C

2. Ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V_S = ± 15V, T_A = 25°C, unless otherwise noted.

			CMP-02 CMP-02E			CMP-02B CMP-02C			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	—	0.3	0.8	—	0.4	2.8	mV
Input Offset Voltage	V_{OS}	$R_S \leq 50k\Omega$ (Note 1)	—	0.3	0.9	—	0.4	3.0	mV
Input Offset Current	I_{OS}	(Note 1)	—	0.3	3.0	—	0.4	15	nA
Input Bias Current	I_B		—	28	50	—	3.5	100	nA
Differential Input Resistance	R_{IN}	(Note 2)	5.0	16	—	1.5	12	—	MΩ
Voltage Gain	A_{VO}	V_O = 0.4V to 2.4V (Notes 1 and 2)	200	500	—	100	500	—	V/mV
Response Time (Note 3)	t_r	100mV Step 5mV Overdrive							ns
		No Load (No Pull-Up)	—	190	270	—	190	270	
		5kΩ to 5V (Pull-Up)	—	190	—	—	190	—	
		TTL Fan-Out = 4, No Pull-Up	—	190	—	—	190	—	
Input Slew Rate			—	15	—	—	15	—	V/μs
Input Voltage Range	CMVR		±12.5	±13.0	—	±12.5	±13.0	—	V
Common Mode Rejection Ratio	CMRR		94	110	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 18V, -18V \leq V_{S-} \leq 0V$	80	100	—	74	98	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \geq 3mV, I_O = 320\mu A$	2.4	3.2	—	—	—	—	V
		$V_{IN} \geq 3mV, I_O = 240\mu A$	—	—	—	2.4	3.4	—	
		$V_{IN} \geq 3mV, I_O = 0\mu A$	2.4	4.8	—	2.4	4.8	—	
Saturation Voltage	V_{SAT}	$V_{IN} \leq -10mV, I_{sink} = 0A$	—	0.16	0.40	—	0.16	0.4	V
		$V_{IN} \leq -10mV, I_{sink} \leq 6.4mA$	—	0.3	0.45	—	0.31	0.45	
		$V_{IN} \leq -10mV, I_{sink} \leq 12mA$ (CMP-02 only)	—	0.36	0.5	—	—	—	
Output Leakage Current	I_{LEAK}	$V_{IN} \geq 10mV, V_O = 30V$	—	0.03	2.0	—	0.05	8.0	μA
Positive Supply Current	I+	$V_{IN} \leq -10mV$	—	5.5	8.0	—	5.6	8.5	mA
Negative Supply Current	I-	$V_{IN} \leq -10mV$	—	1.1	2.2	—	1.2	2.2	mA
Power Dissipation	P_d	$V_{IN} \leq -10mV$	—	99	153	—	102	161	mW
Offset Voltage Adjustment Range		Nulling Pot ≥ 2kΩ	—	±5	—	—	±5	—	mV

NOTES:
1. These Parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
2. Guaranteed by design.
3. Sample tested.

ELECTRICAL CHARACTERISTICS at V_S = 5V, V_{S-} = 0V, T_A = 25°C, unless otherwise noted.

			CMP-02 CMP-02E			CMP-02B CMP-02C			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	—	0.4	1.5	—	0.5	3.5	mV
Input Offset Current	I_{OS}		—	0.25	3.0	—	0.35	14	nA
Input Bias Current	I_B		—	24	45	—	30	90	nA
Voltage Gain	A_V	V_O = 0.4V to 2.4V (Notes 1 and 2)	—	50	—	—	50	—	v/mV
Response Time	t_r	100mV Step, 5mV Overdrive 5kΩ to 5V (Pull-Up)	—	250	—	—	250	—	ns
		TTL Fan-Out = 4, 5kΩ to 5V	—	250	—	—	250	—	
Input Voltage Range	CMVR		1.8-3.5	1.7-3.8	—	1.8-3.5	1.7-3.8	—	V
Saturation Voltage	V_{SAT}	$V_{IN} \leq -3.5mV$, $I_{sink} \leq 6.4mA$	—	0.3	0.45	—	0.3	0.45	V
Positive Supply Current	I+	$V_{IN} \leq -10mV$	—	2.2	3.0	—	2.3	3.6	mA
Power Dissipation	P_d	$V_{IN} \leq -10mV$	—	11.0	15.0	—	11.5	18.0	mW

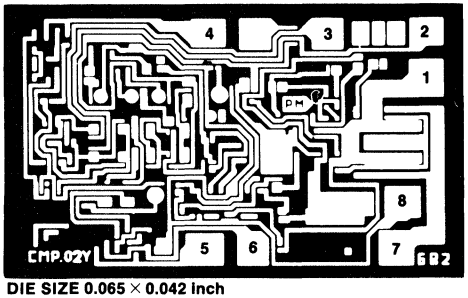
ELECTRICAL CHARACTERISTICS at V_S = ±15V, -55°C ≤ T_A ≤ 125°C, unless otherwise noted.

			CMP-02			CMP-02B			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	—	0.4	1.6	—	0.5	3.5	mV
		V_{S+} = 5V, V_{S-} = 0V (Note 1)	—	0.5	2.8	—	0.6	4.3	
Average Input Offset Voltage Drift									
Without External Trim	TCV_{OS}	$R_S = 50\Omega$	—	1.5	—	—	1.8	—	μV/°C
With External Trim	TCV_{OSn}	$R_S = 50\Omega$	—	1.0	—	—	1.2	—	
Input Offset Current	I_{OS}	T_A = +125°C (Note 1)	—	0.3	4.0	—	0.4	15	nA
		T_A = -55°C (Note 1)	—	0.4	12.0	—	0.5	25	
Average Input Offset Current Drift	TCI_{OS}	+25°C ≤ T_A ≤ +125°C	—	2.0	—	—	3.0	—	pA/°C
		-55°C ≤ T_A ≤ +25°C	—	4.0	—	—	5.0	—	
Input Bias Current	I_B	T_A = +125°C	—	25	50	—	33	100	nA
		T_A = -55°C	—	45	120	—	42	160	
Voltage Gain	A_{VO}	V_O = 0.4V to 2.4V (Notes 1 and 2)	100	500	—	70	500	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive T_A = +125°C, No Load	—	310	—	—	225	—	ns
		T_A = -55°C, No Load	—	155	—	—	180	—	
Input Voltage Range	CMVR		±12.0	±13.0	—	±12.0	±13.0	—	V
Common Mode Rejection Ratio	CMRR		88	106	—	86	106	—	dB
Power Supply Rejection Ratio	PSRR	5V ≤ V_{S+} ≤ 15V, -15V ≤ V_{S-} ≤ 0V	75	96	—	70	88	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \geq 4mV$, $I_O = 200\mu A$	2.4	3.0	—	2.4	3.2	—	V
Saturation Voltage	V_{SAT}	$V_{IN} \leq -10mV$, I_{sink} = 0	—	0.20	0.4	—	0.17	0.4	V
		$V_{IN} \leq -10mV$, I_{sink} = 6.4mA	—	0.32	0.5	—	0.31	0.5	

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \leq T_A \leq 70°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-02E MIN	CMP-02E TYP	CMP-02E MAX	CMP-02C MIN	CMP-02C TYP	CMP-02C MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	—	0.4	1.4	—	0.5	3.5	mV
		$V_{S+} = 5V$, $V_{S-} = 0V$ (Note 1)	—	0.5	2.4	—	0.6	4.3	
Average Input Offset Voltage Drift									
Without External Trim	TCV_{OS}	$R_S = 50\Omega$	—	1.5	—	—	1.8	—	μV/°C
With External Trim	TCV_{OSn}	$R_S = 50\Omega$	—	1.0	—	—	1.2	—	
Input Offset Current	I_{OS}	$T_A = +70°C$ (Note 1)	—	0.3	3.0	—	0.4	15	nA
		$T_A = 0°C$ (Note 1)	—	0.4	6.0	—	0.5	25	
Average Input Offset Current Drift	TCI_{OS}	$+25°C \leq T_A \leq +70°C$	—	2.0	—	—	3.0	—	pA/°C
		$0°C \leq T_A \leq +25°C$	—	4.0	—	—	5.0	—	
Input Bias Current	I_B	$T_A = +70°C$	—	26	50	—	33	100	nA
		$T_A = 0°C$	—	34	80	—	42	160	
Voltage Gain	A_V	$V_O = 0.4V$ to 2.4V (Notes 1 and 2)	100	500	—	70	500	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive							
		$T_A = +70°C$, No Load	—	225	—	—	225	—	ns
		$T_A = 0°C$, No Load	—	180	—	—	180	—	
Input Voltage Range	CMVR		±12.0	±13.0	—	±12.0	±13.0	—	V
Common Mode Rejection Ratio	CMRR		90	108	—	86	108	—	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 15V$, $-15V \leq V_{S-} \leq 0V$	77	98	—	70	88	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \geq 4mV$, $I_O = 200\mu A$	2.4	3.2	—	2.4	3.2	—	V
Saturation Voltage	V_{SAT}	$V_{IN} \leq -10mV$, $I_{sink} = 0$	—	0.17	0.4	—	0.17	0.4	V
		$V_{IN} \leq -10mV$, $I_{sink} = 6.4mA$	—	0.30	0.5	—	0.31	0.5	

DICE CHARACTERISTICS



DIE SIZE 0.065 × 0.042 inch

1. GROUND
2. NON-INVERTING INPUT
3. INVERTING INPUT
4. NEGATIVE SUPPLY
5. BALANCE
6. BALANCE
7. OUTPUT
8. POSITIVE SUPPLY

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$ at 25°C.

PARAMETER	SYMBOL	CONDITIONS	CMP-02N LIMIT	CMP-02GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ $R_S \leq 50k\Omega$	0.8 0.9	2.8 3.0	mV MAX
Input Offset Current	I_{OS}		3.0	15	nA MAX
Input Bias Current	I_B		50	100	nA MAX
Differential Input Resistance	R_{IN}		5.0	1.5	MΩ MIN
Input Voltage Range	IVR		±12.5	±12.5	V MIN
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm CMVR$	94	90	dB MIN
Power Supply Rejection Ratio	PSRR	$5V \leq V_S+ \leq 18V$ $-18V \leq V_S- \leq 0V$	80	74	dB MIN
Positive Output Voltage	V_{OH}	$V_{IN} \geq 3mV$, $I_O = 320\mu A$ $V_{IN} \geq 3mV$, $I_O = 240\mu A$	2.4 —	— 2.4	V MIN
Saturation Voltage	V_{SAT}	$I_{sink} = 6.4mA$	0.45	0.45	V MAX
Output Leakage Current	I_{LEAK}	$V_{IN} \geq 10mV$, $V_O = 30V$	4.0	8.0	μA MAX
Positive Supply Current	I+	$V_{IN} \leq -10mV$	8.0	8.5	mA MAX
Negative Supply Current	I–	$V_{IN} \leq -10mV$	2.2	2.2	mA MAX
Power Consumption	P_d	$V_{IN} \leq -10mV$	153	161	mW MAX

ELECTRICAL CHARACTERISTICS at $V_S+ = 5V$ and $V_S- = 0V$ at 25°C.

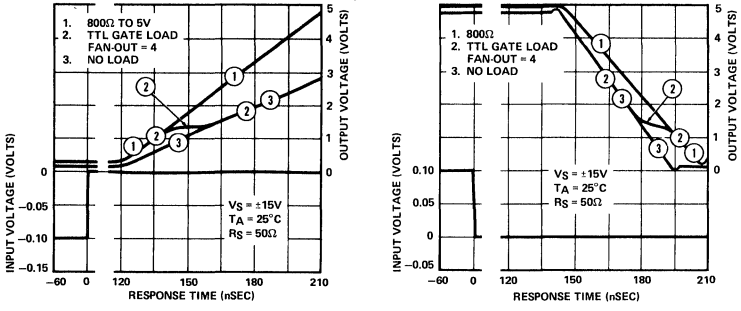
PARAMETER	SYMBOL	CONDITIONS	CMP-02N LIMIT	CMP-02GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$	1.5	3.5	mV MAX
Input Offset Current	I_{OS}		3.0	14	nA MAX

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm$ 15V, and 25°C.

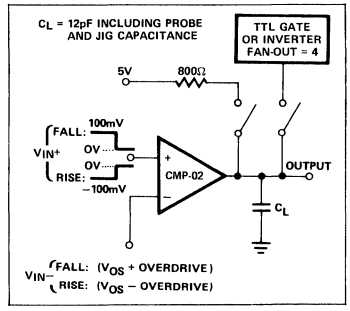
PARAMETER	SYMBOL	CONDITIONS	CMP-02N TYPICAL	CMP-02GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	1.5	1.8	μV/°C
Average Input Offset Current Drift	TCI_{OS}		4.0	5.0	pA/°C
Response Time	t_r	100mV Step, 5mV Overdrive No Load (No Pull-Up)	180	180	ns

TYPICAL PERFORMANCE CURVES

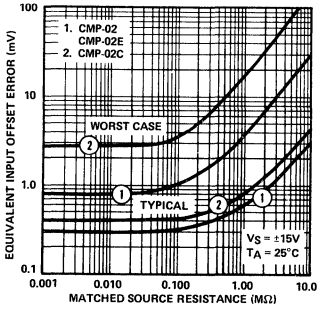
RESPONSE TIME, 100mV STEP, 5mV OVERDRIVE, VARIOUS LOADS



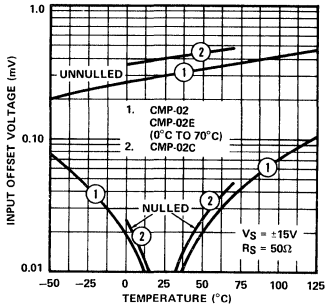
RESPONSE TIME TEST CIRCUIT



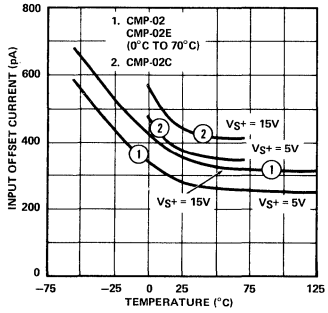
INPUT OFFSET ERROR vs SOURCE RESISTANCE



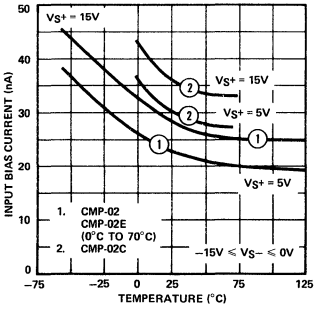
OFFSET VOLTAGE vs TEMPERATURE



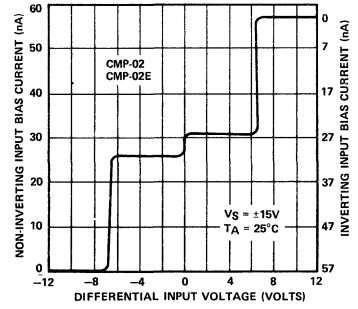
INPUT OFFSET CURRENT vs TEMPERATURE



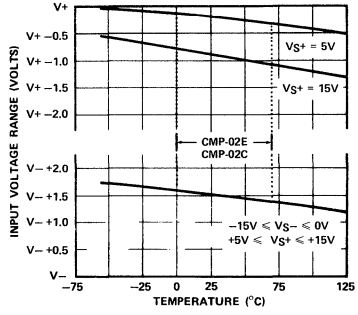
INPUT BIAS CURRENT vs TEMPERATURE



INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE

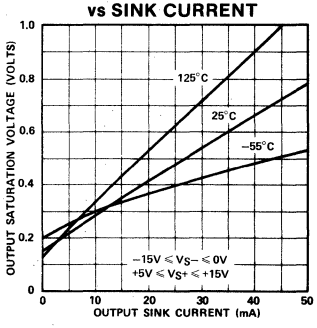


INPUT VOLTAGE RANGE vs TEMPERATURE

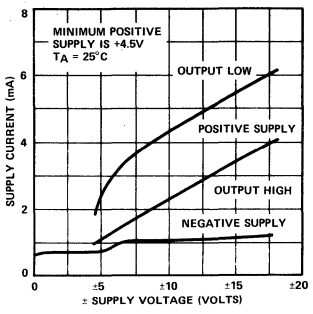


TYPICAL PERFORMANCE CURVES

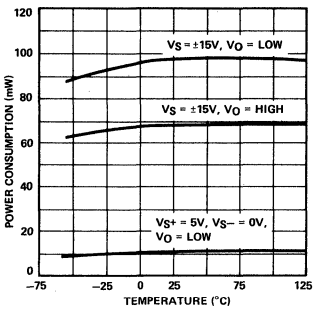
SATURATION VOLTAGE vs SINK CURRENT



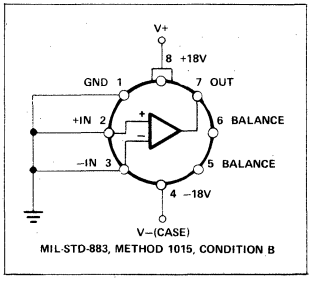
SUPPLY CURRENT vs SUPPLY VOLTAGE



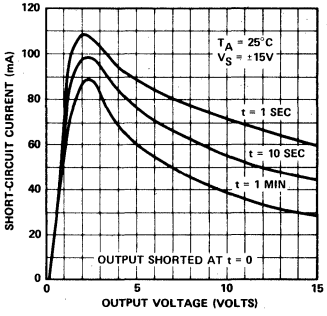
POWER CONSUMPTION vs TEMPERATURE



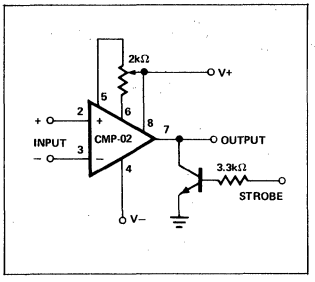
STANDARD BURN-IN CIRCUIT



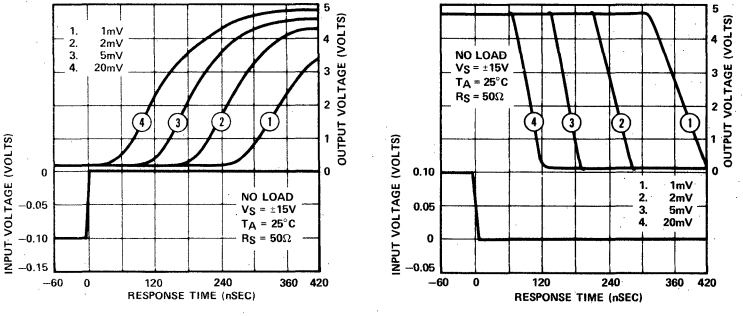
OUTPUT SHORT-CIRCUIT CURRENT vs OUTPUT VOLTAGE



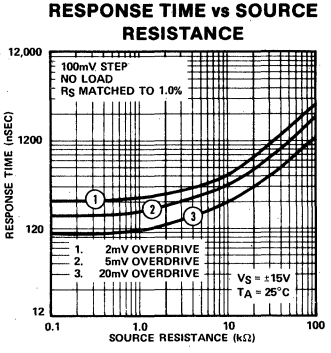
OFFSET TRIMMING AND STROBE CIRCUITS



RESPONSE TIME FOR 100mV STEP AND VARIOUS INPUT OVERDRIVES



RESPONSE TIME vs SOURCE RESISTANCE

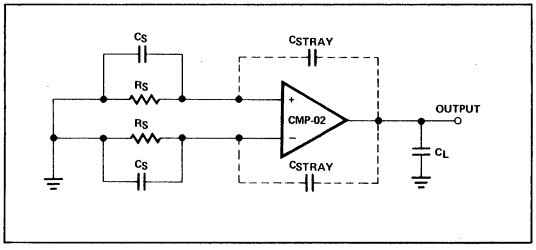


APPLICATION NOTES

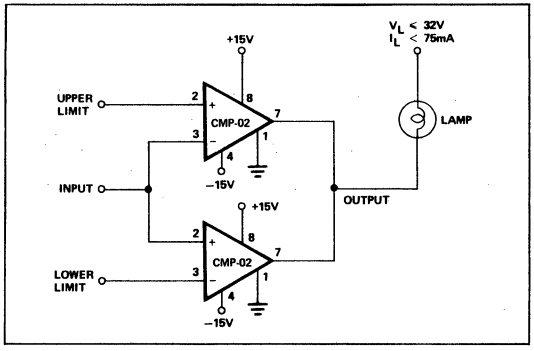
The CMP-02 provides fast response times even with small input overdrives; to achieve this performance requires very high gain at high frequencies. The CMP-02 is completely free of oscillations; however, small values of stray capacitance from output to input when combined with high-source resistances can cause an unstable condition. DC characteristics are not affected, but when the input is within a few microvolts of the transition level, certain conditions can create an oscillation region. The width of this oscillatory region and the size of source resistance where oscillations begin is a strong function of the stray coupling present. The following suggestions are offered as a guide towards minimizing the conditions for oscillation: matched source resistors, minimized stray capacitances (e.g., a ground plane between output and input), capacitive output loading (C_L), or a capacitor from the compensation terminal to AC ground (DIP only). The capacitive loading techniques will eliminate the oscillations, but result in slower response time. Positive resistive feedback creating a hysteresis condition can be very effective — see level detector below. Matched bypass capacitors across the input resistors also can eliminate the instability,

and if $C_S \geq 20pF \left(\frac{\text{maximum step size}}{\text{minimum overdrive}}\right)$

the response time will approximate the response time for low values of R_S. It should be noted that the offset nulling terminals do not require bypassing for stability. As with all wideband circuits, it is recommended that the supplies be bypassed near the socket of the device.



PRECISION DUAL LIMIT GO/NO GO TESTER



CMP-04

LOW POWER PRECISION QUAD COMPARATOR

FEATURES

- **High Gain** ..... **200V/mV Typical**
- **Single or Dual Supply Operation**
- **Input Voltage Range Includes Ground**
- **Low Power Consumption (1.5mW/Comparator)**
- **Low Input Bias Current** **25nA**
- **Low Input Offset Current** ..... **±2.0nA**
- **Low Offset Voltage** ..... **±0.4mV Typical**
- **Low Output Saturation Voltage** ..... **250mV @ 4mA**
- **Logic Output Compatible with TTL, DTL, ECL, MOS and CMOS**
- **Directly Replaces LM139/239/339 Comparators**

GENERAL DESCRIPTION

Four precision independent comparators comprise the CMP-04. Performance highlights include a very low offset voltage, low output saturation voltage and high gain in a single supply design. The input voltage range includes ground for single supply operation and V– for split supplies. A low power supply current of 2mA, which is independent of supply voltage, makes this the preferred comparator for precision applications requiring minimal power consumption. Maximum logic interface flexibility is offered by the open-collector TTL output.

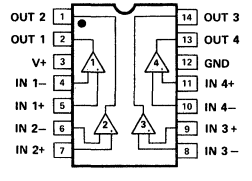
ORDERING INFORMATION†

25°C V_{OS} (mV)	DIP PACKAGE HERMETIC 14 PIN	DIP PACKAGE PLASTIC 14 PIN	OPERATING TEMPERATURE RANGE
1	CMP04BY *	——	MIL
1	CMP04FY		IND
1	——	CMP04FP	COM

* Also available with MIL-STD-883B processing. To order add /883 as a suffix to the part number.

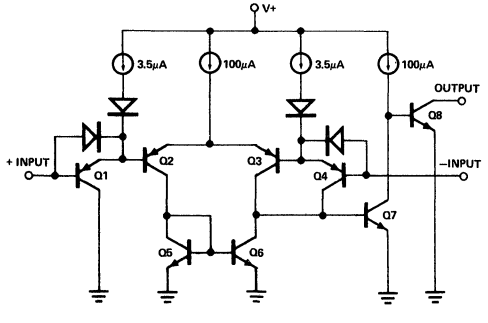
† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS

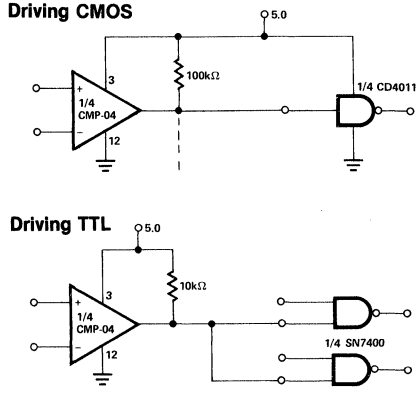


14 PIN HERMETIC DIP (Y SUFFIX) **14 PIN EPOXY DIP (P SUFFIX)**

SIMPLIFIED SCHEMATIC (1/4 CMP-04)



TYPICAL INTERFACE



ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... 36V or ±18V
Differential Input Voltage ..... $36V_{DC}$
Input Voltage ..... −0.3V to +36V
Power Dissipation (Note 1) 500mW
Operating Temperature Range
CMP-04 FY ..... −25°C to +85°C
CMP-04 BY ..... −55°C to +125°C
CMP-04 FP ..... 0°C to +70°C
DICE Junction Temperature (T_j) ..... −65°C to +150°C
Storage Temperature Range ..... −65°C to +150°C
Input Current (V_{IN} < −3.0V) 50mA
Output Short Circuit to GND ..... Continuous
Lead Temperature (soldering, 10 sec) ..... 300°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.
2. Absolute maximum ratings apply to both packaged parts and dice, unless otherwise noted.

Package	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
Hermetic DIP (Y)	100°C	10 mW/°C
Plastic DIP (P)	50°C	6 mW/°C

ELECTRICAL CHARACTERISTICS at V+ = +5V, T_A = 25°C, unless otherwise noted.

			CMP-04B/F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	R_S = 0Ω, R_L = 5.1kΩ V_O = 1.4V (Note 1)	—	0.40	1.0	mV
Input Offset Current	I_{OS}	$I_{IN}(+) - I_{IN}(-)$ R_L = 5.1kΩ V_O = 1.4V	—	2.0	10	nA
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$ (Note 1)	—	25	100	nA
Voltage Gain	A_V	$R_L \geq$ 15k, V_+ = 15V (Note 6)	80	200	—	V/mV
Large Signal Response Time	t_r	V_{IN} = TTL Logic Swing V_{REF} = 1.4V (Note 5) V_{RL} = 5V, R_L = 5.1kΩ	—	300	—	ns
Small Signal Response Time	t_r	V_{IN} = 100mV Step (Note 5) 5mV Overdrive V_{RL} = 5V, R_L = 5.1kΩ	—	1.3	—	μs
Input Voltage Range	IVR	(Note 2)	0	—	V+ −1.5	V
Common Mode Rejection Ratio	CMRR	(Note 4, Note 6)	80	100	—	dB
Power Supply Rejection Ratio	PSRR	V+ = +5V to 18V (Note 6)	80	100	—	dB
Saturation Voltage	V_{SAT}	$V_{IN}(-) \geq$ 1V $V_{IN}(-)$ = 0 $I_{SINK} \leq$ 4mA	—	250	400	mV
Output Sink Current	I_{SINK}	$V_{IN}(-) \geq$ 1V $V_{IN}(+)$ = 0, $V_O \leq$ 1.5V	6.0	16	—	mA
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq$ 1V $V_{IN}(-)$ = 0, V_O = 5V	—	0.1	100	nA
Supply Current	I+	R_L = ∞, All Comps V+ = 30V	—	0.8	2.0	mA

NOTES:

1. At output switch point, V_O = 1.4V, R_S on 0Ω with V+ from 5V; and over the full input common-mode range (0V to V+ − 1.5V).
2. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ − 1.5V, but either or both inputs can go to +30V without damage.
3. Operating temperature ranges are:
   BY ..... −55°C to +125°C
   FY ..... −25°C to +85°C
   FP ..... 0°C to +70°C
4. $R_L \geq$ 15kΩ V+ = 15V, V_{CM} = 1.5V to 13.5V.
5. Sample tested.
6. Guaranteed by design.

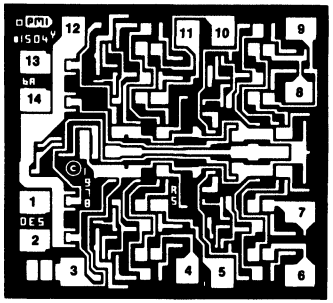
ELECTRICAL CHARACTERISTICS at $V_S+ = 5V$. For CMP-04BY, $-55°C \leq T_A \leq 125°C$. For CMP-04FY, $-25°C \leq T_A \leq 85°C$. For CMP-04FP, $0°C \leq T_A \leq 70°C$, unless otherwise noted.

			CMP-04B/F (Note 3)			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S = 0\Omega$, $R_L = 5.1k\Omega$ $V_O = 1.4V$ (Note 1)	—	1.0	2.0	mV
Input Offset Current	I_{OS}	$I_{IN}(+) - I_{IN}(-)$ $R_L = 5.1k\Omega$ $V_O = 1.4V$	—	4.0	20	nA
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$ (Note 1)	—	40	200	nA
Voltage Gain	A_V	$R_L \geq 15k$, $V_+ = 15V$ (Note 6)	70	125	—	V/mV
Large Signal Response Time	t_r	V_{IN} = TTL Logic Swing $V_{REF} = 1.4V$ (Note 5) $V_{RL} = 5V$, $R_L = 5.1k\Omega$	—	300	—	ns
Small Signal Response Time	t_r	V_{IN} = 100mV Step (Note 5) 5mV Overdrive $V_{RL} = 5V$, $R_L = 5.1k\Omega$	—	1.3	—	μs
Input Voltage Range	IVR	(Note 2)	0	—	V+ −1.5	V
Common Mode Rejection Ratio	CMRR	(Note 4, Note 6)	60	100	—	dB
Power Supply Rejection Ratio	PSRR	V+ = +5V to +18V	80	100	—	dB
Saturation Voltage	V_{SAT}	$V_{IN}(-) \geq 1V$ $V_{IN}(+) = 0$ $I_{SINK} \leq 4mA$	—	250	700	mV
Output Sink Current	I_{SINK}	$V_{IN}(-) \geq 1V$ $V_{IN}(+) = 0$, $V_O \leq 1.5V$	5.0	16	—	mA
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq 1V$ $V_{IN}(-) = 0$, $V_O = 5V$	—	0.1	200	nA
Supply Current	I+	$R_L = \infty$, All Comps V+ = 30V	—	1.2	3.0	mA

NOTES:

1. At output switch point, $V_O = 1.4V$, R_S on 0Ω with V+ from 5V; and over the full input common-mode range (0V to V+ − 1.5V).
2. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ − 1.5V, but either or both inputs can go to +30V without damage.
3. Operating temperature ranges are:
   BY ..... −55°C to +125°C
   FY ..... −25°C to +85°C
   FP ..... 0°C to +70°C
4. $R_L \geq 15k\Omega$ V+ = 15V, $V_{CM} = 1.5V$ to 13.5V.
5. Sample tested.
6. Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.052 × 0.056 inch

1. OUTPUT (2)
2. OUTPUT (1)
3. POSITIVE SUPPLY
4. INVERTING INPUT (1)
5. NON-INVERTING INPUT (1)
6. INVERTING INPUT (2)
7. NON-INVERTING INPUT (2)
8. INVERTING INPUT (3)
9. NON-INVERTING INPUT (3)
10. INVERTING INPUT (4)
11. NON-INVERTING INPUT (4)
12. GROUND
13. OUTPUT (4)
14. OUTPUT (3)

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at V+ = +5V, T_A = 25° C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	CMP-04N LIMIT	CMP-04G LIMIT	CMP-04GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S = 0\Omega$, $R_L = 5.1k\Omega$ $V_O = 1.4V$ (Note 1)	1.0	2.0	5	mV MAX
Input Offset Current	I_{OS}	$I_{IN}(+) - I_{IN}(-)$ $R_L = 5.1k\Omega$ $V_O = 1.4V$	10	25	50	nA MAX
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$ (Note 1)	100	100	250	nA MAX
Voltage Gain	A_V	$R_L \geq 15k$, $V_+ = 15V$ (Note 3)	80	50	50	V/mV MIN
Input Voltage Range	IVR	(Notes 2, 3)	V+ – 1.5	V+ – 1.5	V+ – 2.0	V MAX
Common Mode Rejection Ratio	CMRR	(Note 4)	80	80	80	dB MIN
Power Supply Rejection Ratio	PSRR	V + +5 to +18V	80	80	80	dB MIN
Saturation Voltage	V_{SAT}	$V_{IN}(-) \geq 1V$ $V_{IN}(-) = 0$ $I_{SINK} \leq 4mA$	400	400	400	mV MAX
Output Sink Current	I_{SINK}	$V_{IN}(-) \geq 1V$ $V_{IN}(+) = 0$, $V_O \leq 1.5V$	6.0	6	6	mA MIN
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq 1V$ $V_{IN}(-) = 0$, $V_O = 5V$	100	100	100	nA MAX
Supply Current	I+	$R_L = \infty$, All Comps V+ = 30V	2.0	2.0	2.0	mA MAX

ELECTRICAL CHARACTERISTICS at V+ = +5V, unless otherwise specified.

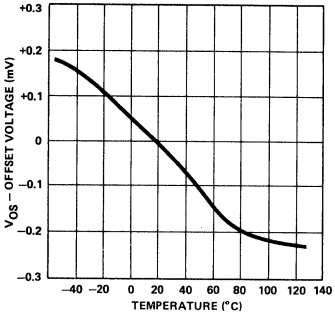
PARAMETER	SYMBOL	CONDITIONS	CMP-04N TYP	CMP-04G TYP	CMP-04GR TYP	UNITS
Large Signal Response Time	t_r	V_{IN} = TTL Logic (Note 5) Swing V_{REF} = 1.4V V_{RL} = 5V, $R_L = 5.1k\Omega$	300	300	300	ns
Small Signal Response Time	t_r	V_{IN} = 100mV Step (Note 5) 5mV Overdrive V_{RL} = 5V, $R_L = 5.1k\Omega$	1.3	1.3	1.3	μs

NOTES:

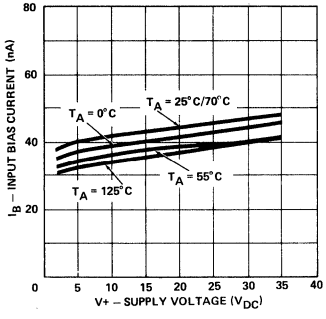
1. At output switch point, V_O = 1.4V, R_S on 0Ω with V+ from 5V; and over the full input common-mode range (0V to V+ – 1.5V).
2. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ – 1.5V, but either or both inputs can go to +30V without damage.
3. Guaranteed by design.
4. $R_L \geq 15k\Omega$. V+ = 15V. V_{CM} = 1.5V to 13.5V.
5. Sample tested.

TYPICAL PERFORMANCE CURVES

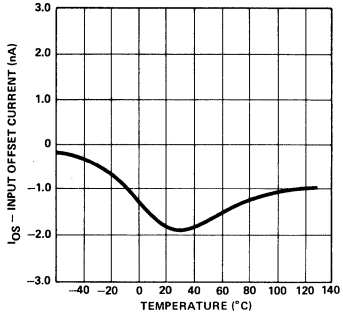
OFFSET VOLTAGE vs TEMPERATURE



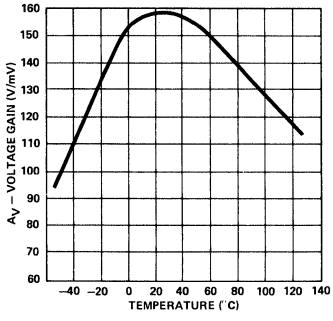
INPUT BIAS CURRENT vs V+ TEMPERATURE



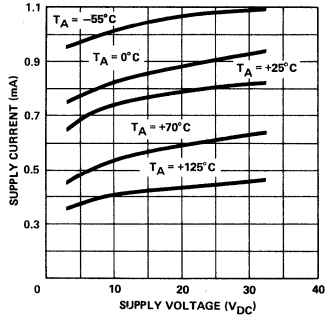
INPUT OFFSET CURRENT vs TEMPERATURE



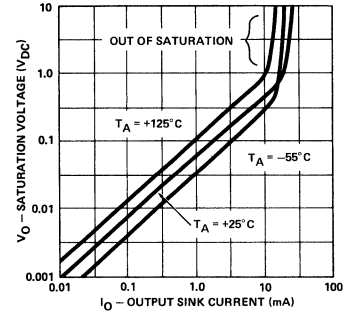
VOLTAGE GAIN vs TEMPERATURE



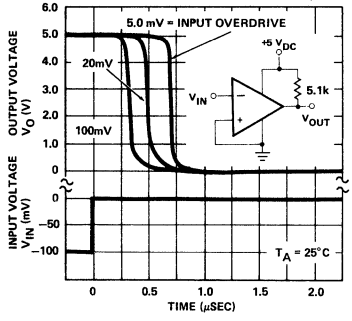
SUPPLY CURRENT vs SUPPLY VOLTAGE



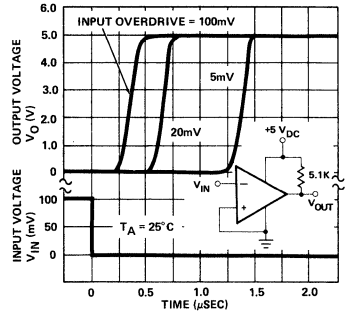
OUTPUT VOLTAGE vs OUTPUT CURRENT AND TEMPERATURE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES — NEGATIVE TRANSITION

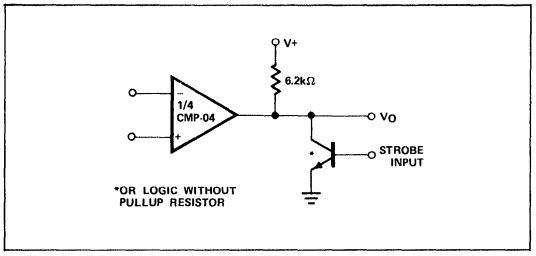


RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES — POSITIVE TRANSITION

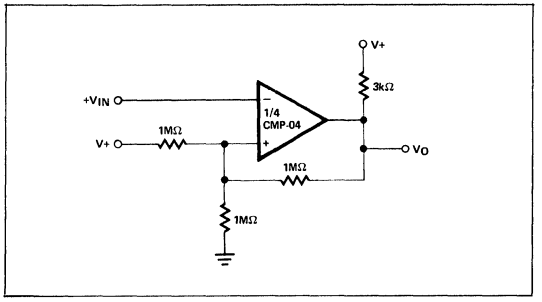


TYPICAL APPLICATIONS

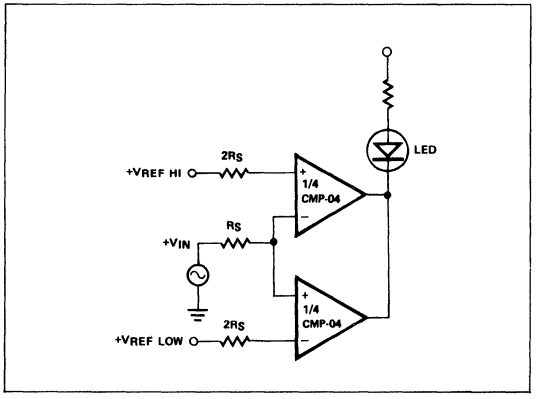
OUTPUT STROBING



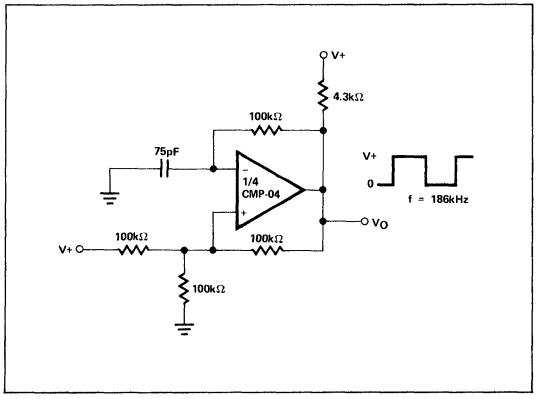
INVERTING COMPARATOR WITH HYSTERESIS



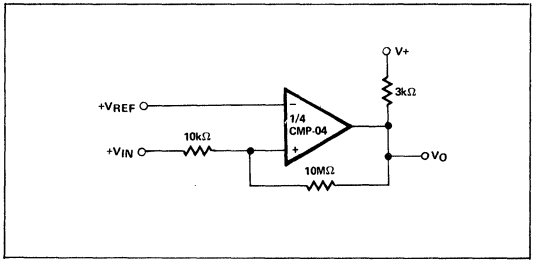
LIMIT COMPARATOR



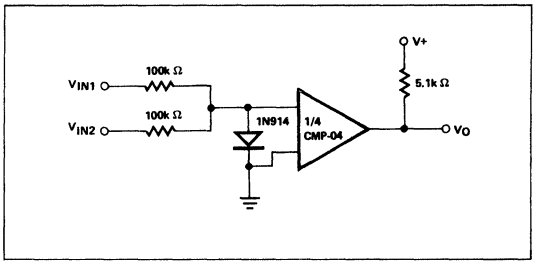
SQUAREWAVE OSCILLATOR



NON-INVERTING COMPARATOR WITH HYSTERESIS



COMPARING INPUT VOLTAGES OF OPPOSITE POLARITY

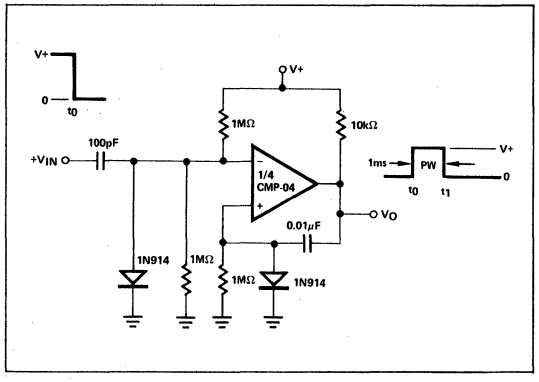


7

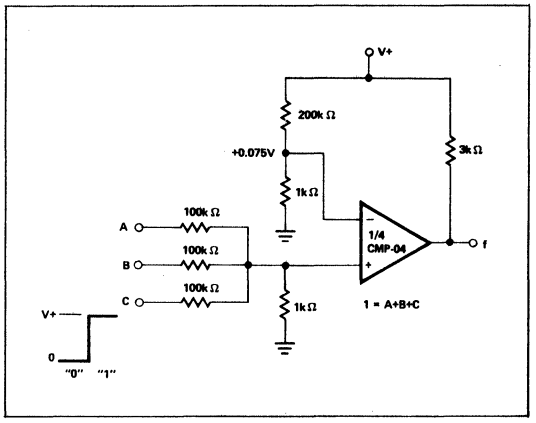
COMPARATORS CMP-04

TYPICAL APPLICATIONS

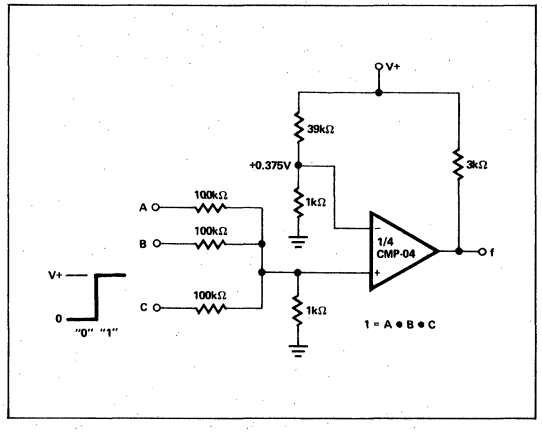
ONE-SHOT MULTIVIBRATOR



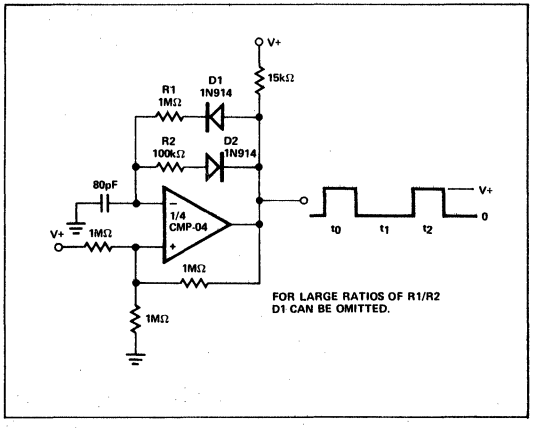
OR GATE



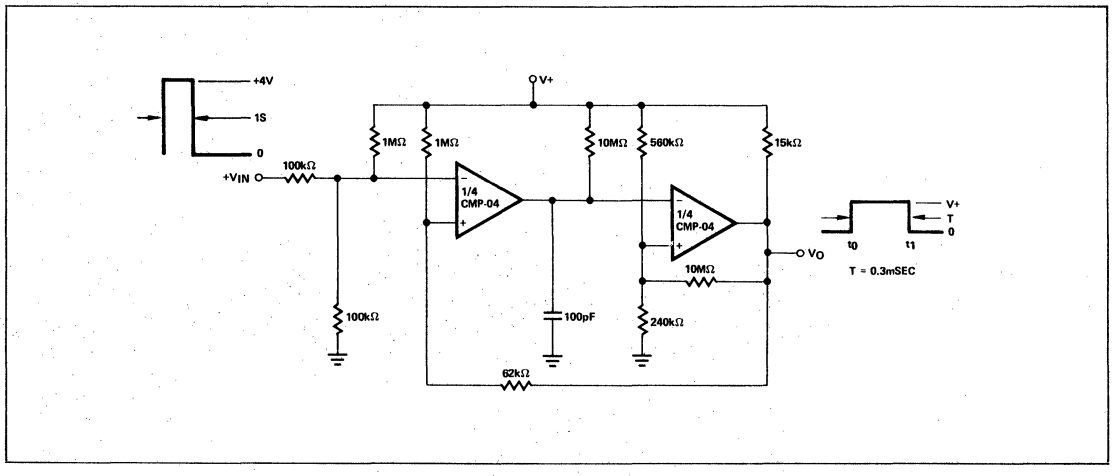
AND GATE



PULSE GENERATOR

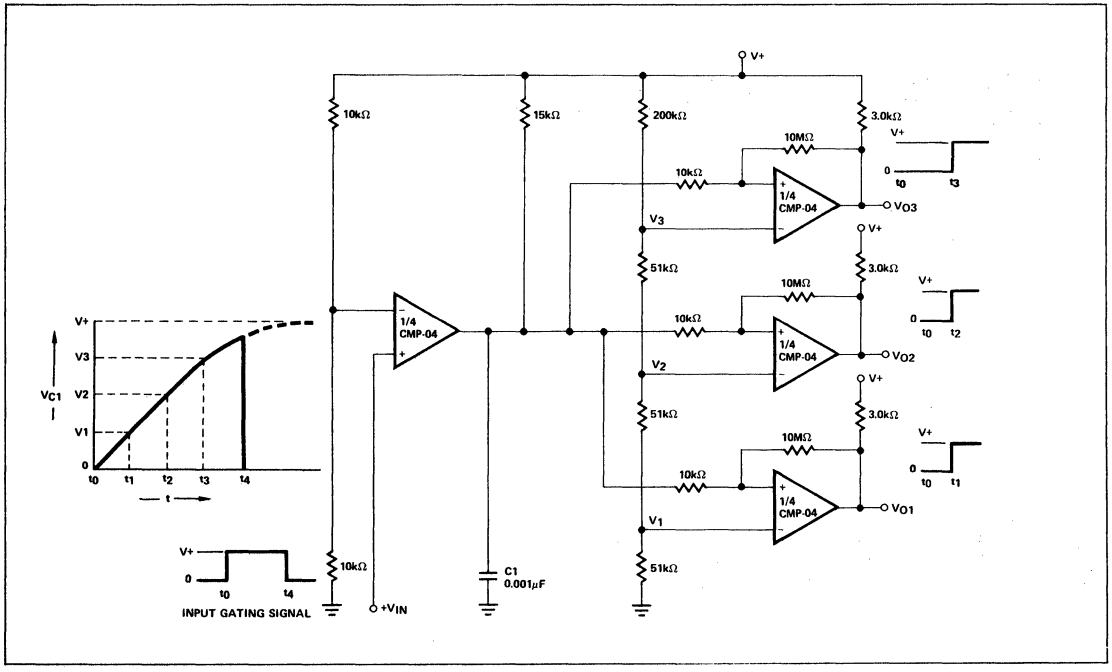


ONE-SHOT MULTIVIBRATOR WITH INPUT LOCK OUT

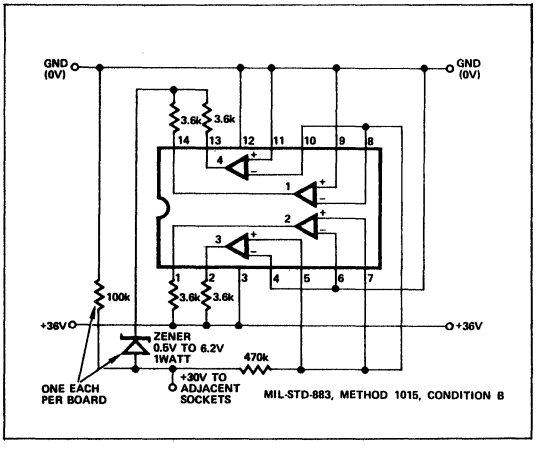


TYPICAL APPLICATIONS

TIME DELAY GENERATOR



BURN-IN CIRCUIT



CMP-05

HIGH-SPEED PRECISION COMPARATOR WITH LATCH CIRCUIT

FEATURES

- **Precision Input Stage**
  - **Input Offset Voltage** **100μV**
  - **Input Offset Current** **15nA**
- **Fast Response Time (5mV OD)** **35nsec**
- **High Voltage Gain** **16,000V/V**
- **Latch Function with TTL Compatible Input**
- **TTL Compatible Output**
- **Available in Hermetic Mini-DIP Package**

ORDERING INFORMATION†

25°C V_{OS} (μV)	PACKAGE HERMETIC TO-99 8 PIN	PACKAGE HERMETIC DIP 8 PIN	PACKAGE PLASTIC DIP 8 PIN	OPERATING TEMPERATURE RANGE
250*	CMP05AJ	CMP05AZ	——	MIL
600*	CMP05BJ	CMP05BZ	——	MIL
250	CMP05EJ	CMP05EZ	——	IND
600	CMP05FJ	CMP05FZ	——	IND
250	——	——	CMP05EP	COM
600	——	——	CMP05FP	COM

* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

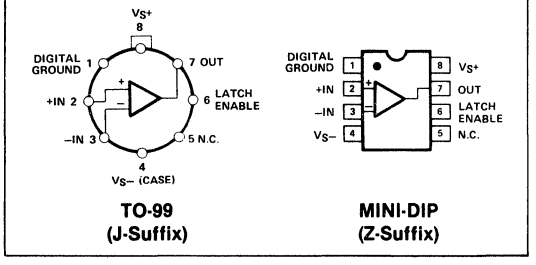
† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

GENERAL DESCRIPTION

The CMP05's very high speed and precision input specifications make it the ideal comparator in systems needing 12-bit accuracy along with high speed. By using "Zener Zap" trimming input offset voltage is less than 1/10 LSB (12-bit, 10-volt system). An exceptionally fast response time of 50 nsec is possible with only 1/2 LSB overdrive (12-bit, 10-volt system).

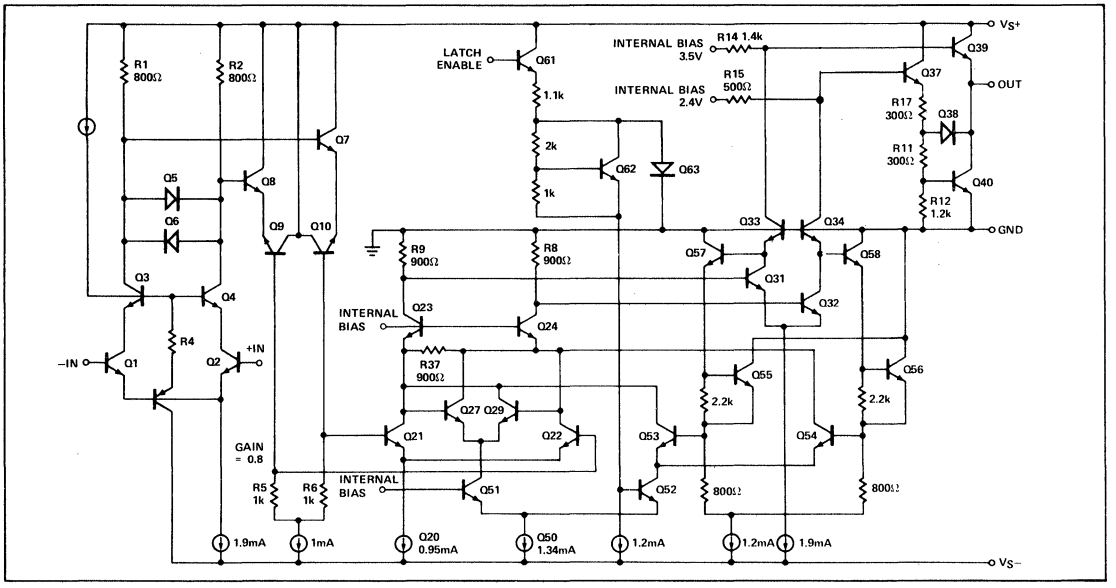
The CMP05 design makes it the ideal component in systems requiring high speed with excellent low-level analog signal resolution. High-speed 12-bit successive approximation A/D converters, zero crossing detectors and logic threshold detectors are typical system applications.

PIN CONNECTIONS



TO-99 (J-Suffix) **MINI-DIP (Z-Suffix)**

SIMPLIFIED SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 2)

Positive Supply Voltage ..... +6V
Negative Supply Voltage ..... -18V
Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±5V
Latch Enable Input Voltage ..... -0.5V to V+ Supply
Operating Temperature Range
CMP-05A/B (J or Z Package)
(Note 3) ..... -55°C to +125°C
CMP-05E/F (J or Z Package) ..... -25°C to +85°C
CMP-05E/F (P Package) ..... 0°C to +70°C
DICE Junction Temperature (T_j) ..... -65°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 60 Sec) ..... 300°C

Output Short Circuit Duration — to ground ..... Indefinite
— to V+ = 5.0V .... 1 Minute

Package	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1 mW/°C
Epoxy Mini-DIP (P)	36°C	5.6 mW/°C
Hermetic Mini-DIP (Z)	75°C	6.7mW/°C

NOTES:
1. See table for maximum ambient temperature rating and derating factor.
2. Absolute maximum ratings apply to both packaged parts and dice, unless otherwise noted.
3. Latch is functional for $-55°C \leq T_A \leq +85°C$.

ELECTRICAL CHARACTERISTICS $V_S+ = 5.0V$, $V_S- = -5.0V$, $T_A = 25°C$ and Latch Enable grounded, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-05A/E MIN	CMP-05A/E TYP	CMP-05A/E MAX	CMP-05B/F MIN	CMP-05B/F TYP	CMP-05B/F MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	100	250	—	200	600	µV
Input Offset Current	I_{OS}		—	15	80	—	30	150	nA
Input Bias Current	I_B		—	0.6	1.2	—	0.8	1.8	µA
Voltage Gain	AVO	Note 1	8	16	—	7	14	—	V/mV
Common Mode Rejection Ratio	CMRR	$V_{cm} = \pm3.0V$, Note 1	86	91	—	84	89	—	dB
Input Voltage Range	IVR	Note 1	±3.0	±3.3	—	±3.0	±3.3	—	V
Power Supply Rejection Ratio	PSRR	$V_S = \pm4.75V$ to $V_S = \pm5.25V$	51	126	—	64	126	—	µV/V
		$V_S^+ = 5V$, $V_S^- = -5V$ to $-15V$	15	51	—	18	63	—	
Output High Voltage	V_{OH}	$V_{IN} \geq 10mV$, $I_O = 0\mu A$	2.4	2.9	—	2.4	2.9	—	V
		$V_{IN} \geq 10mV$, $I_O = 320\mu A$	2.4	2.9	—	—	—	—	
		$V_{IN} \geq 10mV$, $I_O = 200\mu A$	—	—	—	2.4	2.9	—	
Saturation Voltage	V_{SAT}	$V_{IN} \leq -10mV$, $I_{sink} = 0mA$	—	0.13	0.40	—	0.13	0.40	V
		$V_{IN} \leq -10mV$, $I_{sink} = 8mA$	—	—	—	—	0.28	0.40	
		$V_{IN} \leq -10mV$, $I_{sink} = 12.8mA$	—	0.32	0.40	—	—	—	
Positive Supply Current	I_S+	$V_O \geq 2.4V$, Note 1	—	7.5	11	—	8.0	12	mA
		$V_O \leq 0.4V$	—	10	15	—	11	16	
Negative Supply Current	I_S-	$V_O \leq 0.4V$	—	11	16	—	12	18	mA
Power Dissipation	P_d	$V_O \leq 0.4V$	—	105	155	—	115	170	mW
Latch Input Voltage									
Logic 1	V_{LH}	Over Operating Temp. Range Note 1	2.0	—	—	2.0	—	—	V
Logic 0	V_{LL}	Over Operating Temp. Range Note 1	—	—	0.80	—	—	0.80	
Latch Input Current									
Logic 1	I_{LH}	$V_{LH} = 3.0V$, Note 1	—	10	45	—	10	45	µA
Logic 0	I_{LL}	$V_{LL} = 0.8V$, Note 1	—	6	25	—	6	25	
Input to Output High Response Time	t_{pd+}	$V_{OD} = 1.2mV$, Notes 1, 2	—	50	—	—	50	—	ns
		$V_{OD} = 5.0mV$, Notes 1, 2	—	37	55	—	37	60	
Input to Output Low Response Time	t_{pd-}	$V_{OD} = 1.2mV$, Notes 1, 2	—	47	—	—	47	—	ns
		$V_{OD} = 5.0mV$, Notes 1, 2	—	35	55	—	35	60	
Latch Disable	$t_{ipd}+$, $t_{ipd}-$	Notes 1, 3	—	16	—	—	18	—	ns
Latch Set-Up Time	t_s	$V_{OD} = 100mV$, Notes 1, 4	6	3	—	6	3	—	ns

NOTES:
1. Guaranteed by design.
2. Times are for 100mV step inputs. See switching time waveforms.
3. See switching time waveforms.
4. With overdrive signals less than 100mV set-up time decreases and may become negative. Large overdrive signals represent worst case conditions for set-up time.

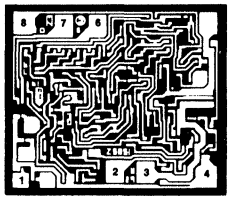
ELECTRICAL CHARACTERISTICS at $V_S+=5.0V$, $V_S-=-5.0V$, and Latch Enable grounded. For CMP-05A/B, $-55°C \leq T_A \leq 125°C$. For CMP-05E/F; $-25°C \leq T_A \leq 85°C$ (J,Z Packages) and $0°C \leq T_A \leq 70°C$ (P Package), unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-05A/E MIN	CMP-05A/E TYP	CMP-05A/E MAX	CMP-05B/F MIN	CMP-05B/F TYP	CMP-05B/F MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	0.25	0.80	—	0.40	1.5	mV
Input Offset Voltage Drift	TC_{VOS}		—	1.5	—	—	2.5	—	µV/°C
Input Offset Current	I_{OS}		—	40	250	—	70	400	nA
Input Bias Current	I_B		—	1.1	2.5	—	1.5	3.8	µA
Voltage Gain	A_{VO}	Note 1	6	11	—	5	10	—	V/mV
Common Mode Rejection Ratio	CMRR	$V_{cm} = \pm 2.9V$, Note 1	83	90	—	80	88	—	dB
Input Voltage Range	IVR	Note 1	±2.9	±3.2	—	±2.9	±3.2	—	V
Power Supply Rejection Ratio	PSRR	$\pm 4.75V \leq V_S \leq \pm 5.25V$	63	178	—	80	252	—	µV/V
Output High Voltage	V_{OH}	$V_{IN} \geq 10mV$, $I_O = 0\mu A$	2.4	—	—	2.4	—	—	V
		$V_{IN} \geq 10mV$, $I_O = 240\mu A$	2.4	—	—	—	—	—	
		$V_{IN} \geq 10mV$, $I_O = 160\mu A$	—	—	—	2.4	—	—	
Saturation Voltage	V_{SAT}	$V_{IN} \leq -10mV$, $I_{sink} = 0mA$	—	0.18	0.40	—	0.20	0.40	V
		$V_{IN} \leq -10mV$, $I_{sink} = 9.6mA$	—	0.2	0.40	—	—	—	
		$V_{IN} \leq -10mV$, $I_{sink} = 6.4mA$	—	—	—	—	0.30	0.40	
Positive Supply Current	I_S^+	$V_O \leq 0.4V$	—	11	16	—	12	17	mA
Negative Supply Current	I_S^-	$V_O \leq 0.4V$	—	12	17	—	13	19	mA
Power Dissipation	P_d	$V_O \leq 0.4V$	—	115	165	—	125	180	mW
Latch Input Current									
Logic 1	I_{LH}	$V_{LH} = 3V$, Note 1	—	18	90	—	18	90	µA
Logic 0	I_{LL}	$V_{LL} = 0.8V$, Note 1	—	10	50	—	10	50	
Input to Output High Response Time	t_{pd+}	$V_{OD} = 1.2mV$, Notes 1, 2	—	125	—	—	125	—	ns
		$V_{OD} = 5.0mV$, Notes 1, 2	—	92	—	—	92	—	
Input to Output Low Response Time	t_{pd-}	$V_{OD} = 1.2mV$, Notes 1, 2	—	115	—	—	115	—	ns
		$V_{OD} = 5.0mV$, Notes 1, 2	—	88	—	—	88	—	
Latch Disable	t_{pd}	Notes 1, 2, 5	—	38	—	—	38	—	ns
Latch Set-Up Time	t_s	Notes 2, 4, 5	—	6	—	—	6	—	ns

NOTES:

1. Guaranteed by design.
2. Times are for 100mV step inputs. See switching time waveforms.
3. A high on the latch enable input will cause the latch to assume the state of the comparator and not follow subsequent inputs.
4. With overdrive signals less than 100mV set-up time decreases and may become negative. Large overdrive signals represent worst case conditions for set-up time.
5. Latch is functional for $-55°C \leq T_A \leq +85°C$.

DICE CHARACTERISTICS



DIE SIZE 0.051 × 0.045 inch

1. DIGITAL GROUND
2. NON-INVERTING INPUT
3. INVERTING INPUT
4. NEGATIVE SUPPLY
6. LATCH ENABLE
7. OUTPUT
8. POSITIVE SUPPLY

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS $V_S = \pm 5V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-05N LIMIT	CMP-05G LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	250	600	μV MAX
Input Offset Current	I_{OS}		80	150	nA MAX
Input Bias Current	I_B		1.2	1.8	μA MAX
Voltage Gain	A_{VO}	Note 1	8	7	V/mV MIN
Input Voltage Range	IVR	Note 1	±3.0	±3.0	V MIN
Power Supply Rejection Ratio	PSRR	$\pm 4.75 \le V_S \le \pm 5.25$ $V_S+ = 5V$, $V_S- = -5V$ to $-15V$	78 86	75 84	dB MIN
Positive Output Voltage	V_{OH}	$V_{IN} \ge 10mV$, $I_O = 0\mu A$	2.4	2.4	V MIN
Saturation Voltage	V_{SAT}	$V_{IN} \le 10mV$, $I_O = 0\mu A$	0.4	0.4	V MAX
Positive Supply Current	I+	$V_O \le 0.4V$	15	16	mA MAX
Negative Supply Current	I−	$V_O \le 0.4V$	16	18	mA MAX
Negative Supply Current	I−	$V- = -15V$, $V_O \le 0.4V$	18	20	mA MAX
Latch Input Voltage Logic 1 Logic 0	 V_{LH} V_{LL}	 Latch Enabled Latch Disabled	 2.0 0.8	 2.0 0.8	 V MIN V MAX
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 2.9V$ Note 1	83	80	dB MIN
Latch Input Current Logic 1 Logic 0	 I_{LH} I_{LL}	 $V_{LH} = 3.0V$, Note 1 $V_{LL} = 0.8V$, Note 1	 45 25	 45 25	 μA MAX
Input-to-Output High Response Time	t_{pd+}	$V_{OD} = 5.0mV$, Notes 1, 2	55	60	ns MAX
Input-to-Output Low Response Time	t_{pd-}	$V_{OD} = 5.0mV$, Notes 1, 2	55	60	ns MAX

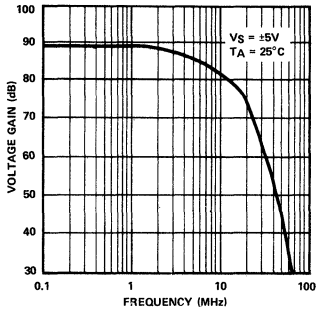
ELECTRICAL CHARACTERISTICS $V_S = \pm 5V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-05N TYPICAL	CMP-05G TYPICAL	UNITS
Input-to-Output High Response Time	t_{pd+}	$V_{OD} = 1.2mV$, Note 2	50	50	ns
Input-to-Output Low Response Time	t_{pd-}	$V_{OD} = 1.2mV$, Note 2	47	47	ns
Latch Disable Time	t_{ipd+}, t_{ipd-}	Note 3	16	18	ns
Latch Set-Up Time	t_S	$V_{OD} = 100mV$	3	3	ns

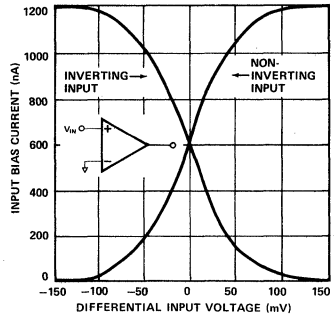
NOTES:
1. Guaranteed by design.
2. Times are for 100mv step inputs.
3. With overdrive signals less than 100mV set-up time decreases and may become negative. Large overdrive signals represent worst case conditions for set-up time.

TYPICAL PERFORMANCE CURVES

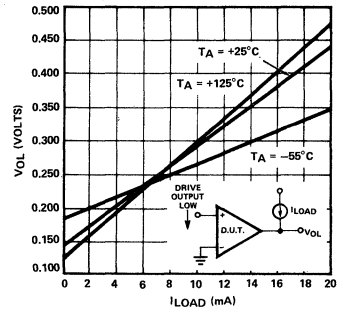
VOLTAGE GAIN vs FREQUENCY



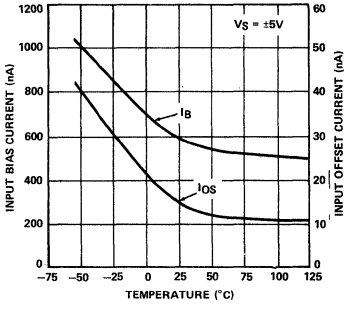
INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



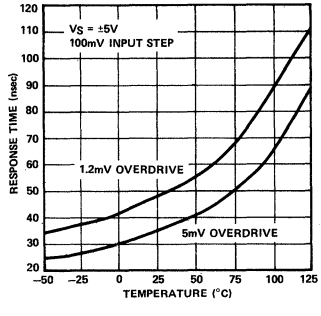
V_{SAT} vs LOAD CURRENT



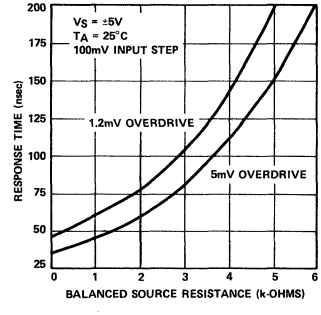
INPUT CURRENTS vs TEMPERATURE



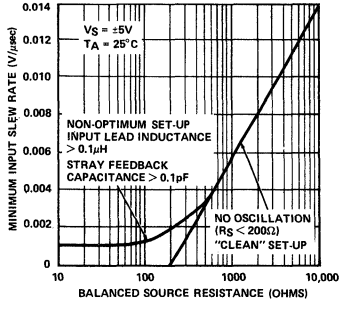
RESPONSE TIME vs TEMPERATURE



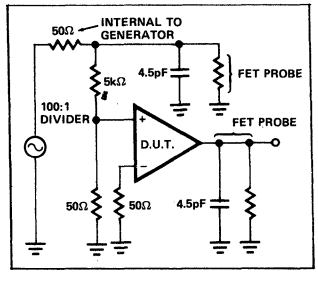
RESPONSE TIME vs BALANCED SOURCE RESISTANCE



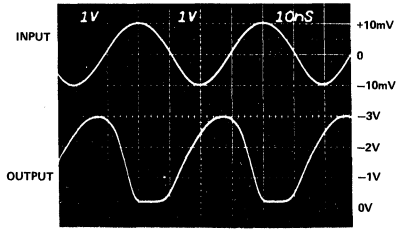
MINIMUM INPUT SIGNAL SLEW RATE vs BALANCED SOURCE RESISTANCE



RESPONSE PHOTOGRAPH TEST SETUP

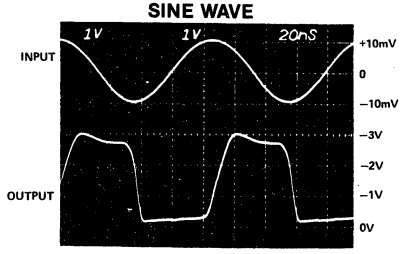


RESPONSE TO 25MHz SINE WAVE

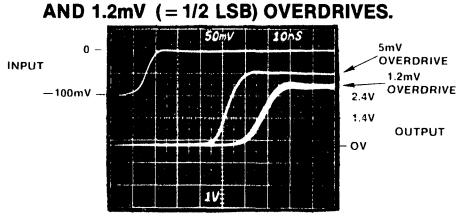


TYPICAL PERFORMANCE CURVES

RESPONSE TO 10MHz SINE WAVE



RESPONSE TIME TO 5mV AND 1.2mV (= 1/2 LSB) OVERDRIVES.



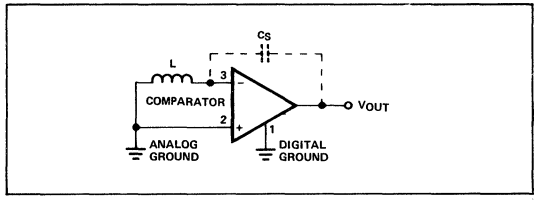
APPLICATION INFORMATION

The CMP-05 is a very accurate device providing fast response time even with small—Microvolt level—overdrives. To achieve this performance requires high gain at high frequencies. As shown in the voltage gain versus frequency curve, the gain—bandwidth product of the CMP-05 is 1.5×10^{11} Hz. It maintains its full gain to approximately 8MHz and rolls off at a very fast rate beyond that frequency due to the fact that five poles occur in the 30 to 60MHz range. At 30MHz the gain of the comparator is still 2000. Therefore, in the transition region small values of source lead inductance and stray feedback capacitance can cause an oscillatory condition.

For example (in the figure below) with $L = 0.1\mu H$, $C_S = 0.15pF$, the closed loop gain of the circuit at 30MHz is:

$$A_V = \frac{1}{LC_S\omega^2} = \frac{1}{10^{-7} \times 0.15 \times 10^{-12} \times (2\pi \times 30 \times 10^6)^2} = 1880$$

POTENTIAL FEEDBACK SOURCES



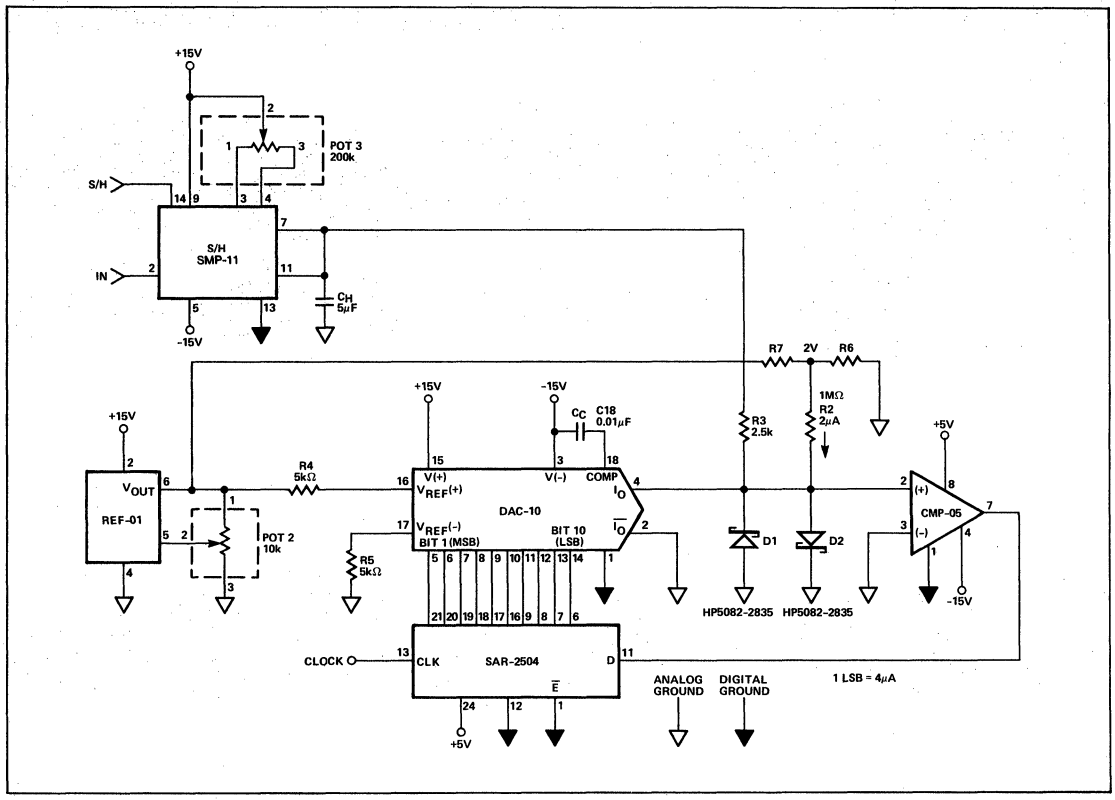
With the open loop gain at 2000 oscillation will occur since the phase shift exceeds 180°. To minimize these problems power supplies should be decoupled, lead lengths should be kept as short as possible, and a ground plane should be used to reduce the stray feedback capacitance. In addition, a ground plane substantially diminishes the possibility of the output current spike coupling back to the inputs through the ground lead. Keeping a separate digital ground (pin 1) and analog ground (to which the inputs are referenced) also reduces the magnitude of the problem.

Fortunately, in high-speed circuitry the comparator inputs will be driven at a fast rate, in which case no transition region oscillations will occur. As the minimum slew rate versus source resistance curve indicates, if the input is driven at a rate exceeding 6mV/μsec, no oscillations will occur with source resistors of less than 1kΩ. Examples of "clean" transitions can be observed in the photographs of the response time with 5mV and 1.2mV overdrives, and the response to the 10 and 25MHz input signals.

In order to not degrade its speed the CMP-05's inputs are not internally clamped. If large differential voltages are present it is recommended that the inputs be clamped with high speed, low capacitance diodes such as the H.P. 5082-2835, which is a Schottky Diode.

As in all high-speed devices, it is to the user's advantage to keep the source impedances low and matched.

10-BIT A TO D CONVERTER



PM139/PM239/PM339/ PM139A/PM239A/PM339A

LOW POWER QUAD VOLTAGE COMPARATOR

FEATURES

- **Single or Dual Supply Operation**
- **Input Voltage Range Includes Ground**
- **Low Power Consumption (2mW/Comparator)**
- **Low Input Bias Current 25nA**
- **Low Input Offset Current ..... ±5nA**
- **Low Offset Voltage ..... ±2mV**
- **Low Output Saturation Voltage (250mV @ 4mA)**
- **Logic Outputs Compatible with TTL, DTL, ECL, MOS and CMOS**
- **Directly replaces LM139/239/339 and LM139A/239A/339A Comparators**

GENERAL DESCRIPTION

The PM139 has four independent voltage comparators, each with precision DC specifications. Low offset voltage, bias current, power consumption and output saturation voltage are offered in a design that features single power supply operation. The input voltage range includes ground for convenient single supply operation. The 2mA power supply current, independent of supply voltage — coupled with the single supply operation, makes this comparator ideal for low power applications. Open collector outputs allow maximum applications flexibility.

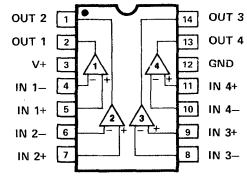
ORDERING INFORMATION†

+25°C V_{OS} (mV)	PACKAGE is 14 PIN HERMETIC DIP	OPERATING TEMPERATURE RANGE
±2*	PM139AY*	MIL
±5*	PM139Y*	MIL
±2	PM239AY	IND
±5	PM239Y	IND
±2	PM339AY	COM
±5	PM339Y	COM

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number.

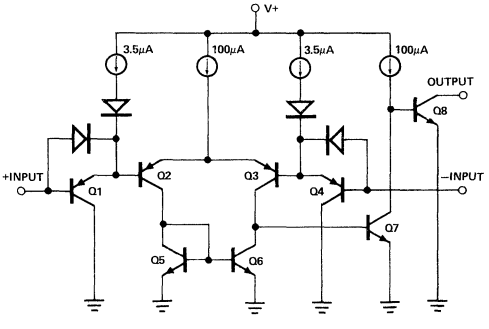
†All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS

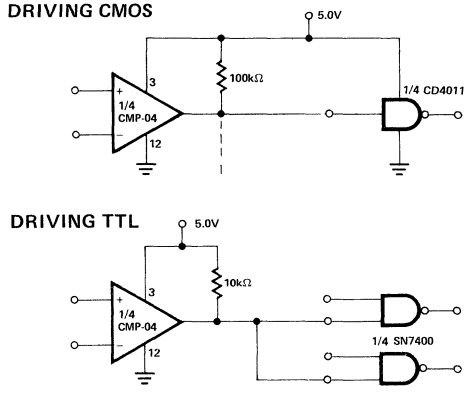


14-PIN HERMETIC DIP (Y SUFFIX)

SIMPLIFIED SCHEMATIC (ONE COMPARATOR)



TYPICAL INTERFACE



ELECTRICAL CHARACTERISTICS at V_S = + 5V, T_A = 25°C, unless otherwise noted.

			PM139A			PM239A PM339A			PM139			PM239 PM339			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	±1.0	±2.0	—	±1.0	±2.0	—	±2.0	±5.0	—	±2.0	±5.0	mV
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$ with Output in Linear Range	—	25	100	—	25	250	—	25	100	—	25	250	nA
Input Offset Current	I_{OS}	$I_{IN}(+)$ or $I_{IN}(-)$	—	±3.0	±25	—	±5.0	±50	—	±3.0	±25	—	±5.0	±50	nA
Input Common Mode Vol. Range	CMVR	(Note 2, Note 5)	0	—	V+ - 1.5	0	—	V+ - 1.5	0	—	V+ - 1.5	0	—	V+ - 1.5	V
Supply Current	I_S	R_L = ∞ on all Compar. V+ = 30V	—	0.8	2.0	—	0.8	2.0	—	0.8	2.0	—	0.8	2.0	mA
Voltage Gain	A_{V0}	$R_L \geq 15k\Omega$, V+ = 15V (to support large V_O swing) (Note 5)	50	200	—	50	200	—	50	200	—	50	200	—	V/mV
Large Signal Response Time		V_{IN} = TTL Logic Swing, V_{REF} = 1.4V, V_{RL} = 5V, R_L = 5.1kΩ Note 4	—	300	—	—	300	—	—	300	—	—	300	—	ns
Response Time		V_{RL} = 5V, R_L = 5.1kΩ (Note 3, Note 4)	—	1.3	—	—	1.3	—	—	1.3	—	—	1.3	—	μs
Output Sink Current	I_O	$V_{IN}(-) \geq 1V$, $V_{IN}(+) = 0$, $V_O \leq 1.5V$	6.0	16	—	6.0	16	—	6.0	16	—	6.0	16	—	mA
Saturation Voltage	V_{SAT}	$V_{IN}(-) \geq 1V$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4mA$	—	250	400	—	250	400	—	250	400	—	250	400	mV
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq 1V$, $V_{IN}(-) = 0$, V_O = 30V	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	—	nA

ELECTRICAL CHARACTERISTICS at V_S = + 5V, -55°C ≤ T_A ≤ + 125°C for PM-139/139A, -25°C ≤ T_A ≤ + 85°C for PM-239/239A, and 0°C ≤ T_A ≤ + 70°C for PM-339/339A.

			PM139A			PM239A PM339A			PM139			PM239 PM339			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	Note 1	—	—	4.0	—	—	4.0	—	—	9.0	—	—	9.0	mV
Input Offset Current	I_{OS}	$I_{IN}(+)$ or $I_{IN}(-)$	—	—	±100	—	—	±150	—	—	±100	—	—	±150	nA
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$ with Output in Linear Range	—	—	300	—	—	400	—	—	300	—	—	400	nA
Input Common Mode Vol. Range	CMVR	(Notes 3, 5)	0	—	V+ - 2.0	0	—	V+ - 2.0	0	—	V+ - 2.0	0	—	V+ - 2.0	V
Saturation Voltage	V_{SAT}	$V_{IN}(-) \geq 1V$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4mA$	—	—	700	—	—	700	—	—	700	—	—	700	mV
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq 1V$, $V_{IN}(-) = 0$, V_O = 30V	—	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	μA
Differential Input Voltage		Keep All $V_{IN's} \geq V-$	—	—	V+	—	—	V+	—	—	36 V+	—	—	36 V+	V

NOTES:

1. At output switch point, V_O = 1.4V, R_S = 0Ω with V+ from 5V, and over the full input common mode range (0V to V+ -1.5V).
2. The input common mode voltage or either input voltage signal should not be allowed to go negative by more than 0.3V. The upper end of the common mode voltage range is V+ -1.5V, but either or both inputs can go to +30V without damage.
3. The response time specified is for a 100mV input step with 5mV overdrive. For larger overdrive signals 300ns can be obtained. See characteristics section. Guaranteed by design.
4. Sample tested.
5. Guaranteed by design.

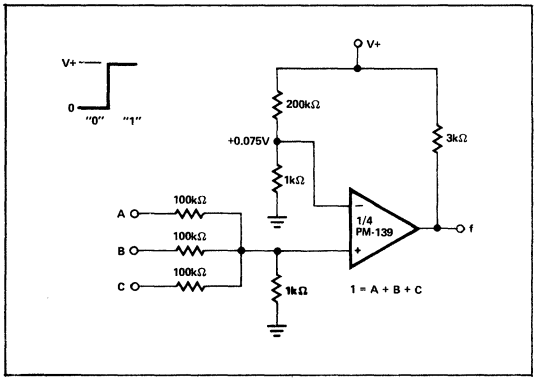
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+ ..... 36V or ±18V
Differential Input Voltage 36V
Input Voltage ..... -0.3V to +36V
Power Dissipation Hermetic Dip 500mW
Output Short-Circuit to Ground ..... Continuous
Input Current (V_{IN} > - 0.3V) 50mA

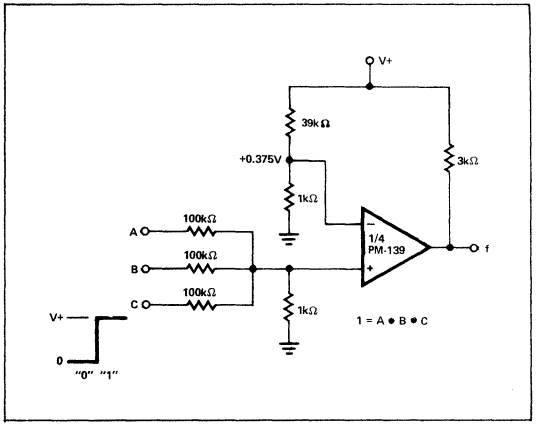
Operating Temperature Range
PM339A/339 ..... 0°C to +70°C
PM239A/239 ..... -25°C to +85°C
PM139A/139 ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

TYPICAL APPLICATIONS

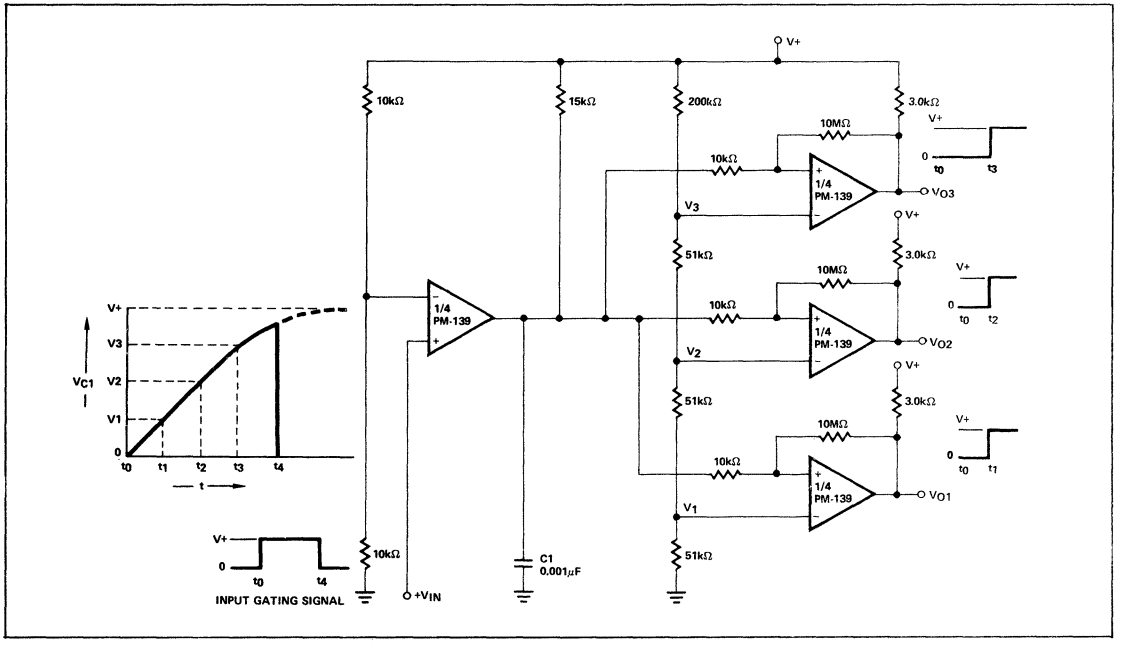
OR GATE



AND GATE

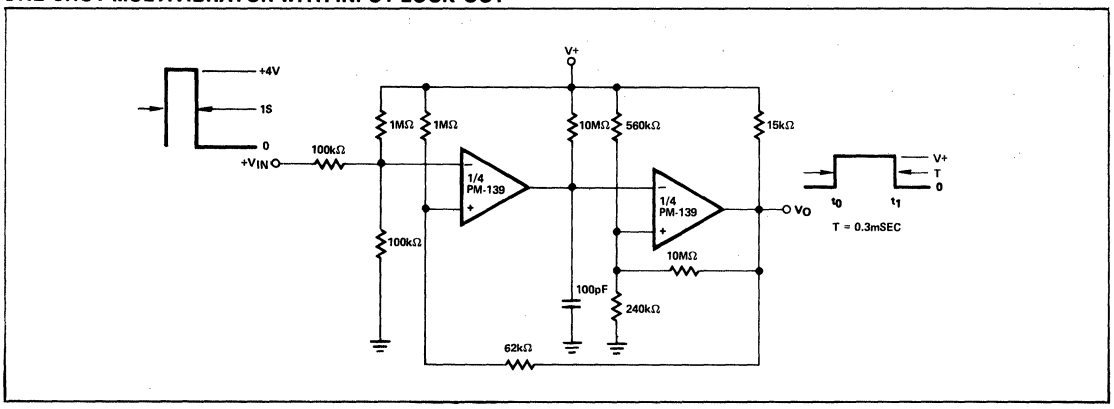


TIME DELAY GENERATOR

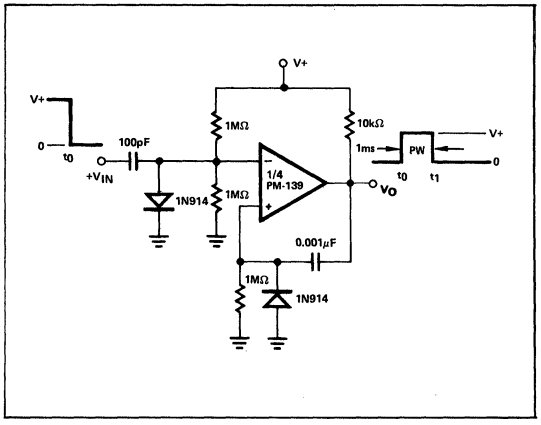


TYPICAL APPLICATIONS

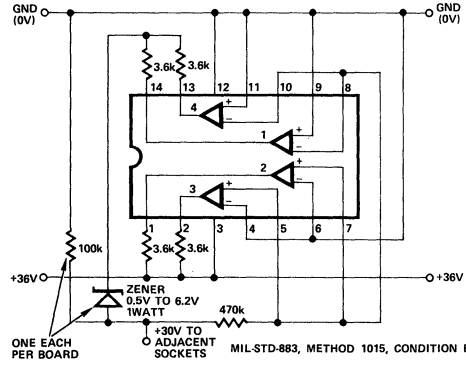
ONE-SHOT MULTIVIBRATOR WITH INPUT LOCK-OUT



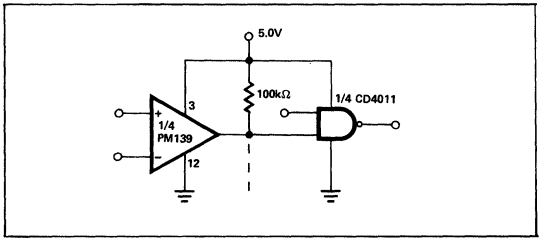
ONE-SHOT MULTIVIBRATOR



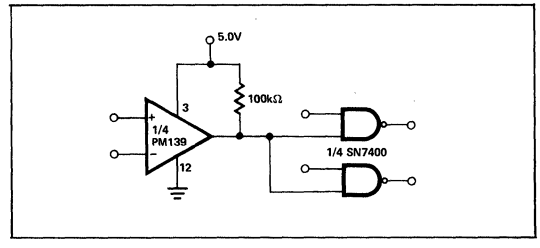
BURN-IN CIRCUIT



DRIVING CMOS



DRIVING TTL



SECTION 8

MATCHED TRANSISTORS

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MATCHED TRANSISTORS

INDEX

PRODUCT	TITLE	PAGE
MAT-01	Ultra-Matched Monolithic Dual Transistor	8-4

INTRODUCTION

Matched transistors such as the MAT-01 have applications in a variety of systems from temperature sensors to analog multipliers. The inherent close thermal proximity resulting from single-chip construction minimizes the errors introduced by temperature excursions.

Other useful characteristics of matched transistors include log conformity for use in analog multiplier applications, emitter-base voltage matching for amplifier front-end circuits, and a large matched h_{FE} for current mirrors.

The MAT-01 consists of four high-gain transistors connected in cross-coupled pairs for excellent thermal tracking.

The experience PMI has gained in the manufacture of Precision op amps has been applied to the MAT-01. The result is a matched transistor pair that exhibits low noise, low leakage, and low drift.

DEFINITIONS

AVERAGE OFFSET CURRENT DRIFT (TCI_{OS})

The ratio of the change in I_{OS} to the change in temperature producing it.

AVERAGE OFFSET VOLTAGE DRIFT (TCV_{OS})

The ratio of the change in V_{OS} to the change in temperature producing it.

BIAS CURRENT (I_B)

The average of the base currents at a specified collector voltage and current.

BROADBAND NOISE VOLTAGE (e_{nRMS})

The root-mean-square noise voltage referred to the input in a specified bandwidth at a specified collector voltage and current.

CURRENT GAIN MATCH (Δh_{FE})

The difference in h_{FE} between the transistors at a specified voltage and current, expressed as a percentage of the lower of the two h_{FE}'s.

$$1 - \frac{h_{FE1}}{h_{FE2}} \times 100$$

NOISE VOLTAGE ($e_{np\text{-}p}$)

The peak-to-peak noise voltage referred to the input in a specified bandwidth at a specified collector voltage and current.

NOISE VOLTAGE DENSITY (e_n)

The rms noise voltage referred to the input within a 1Hz band centered on a specified frequency. It is measured at a specified collector voltage and current.

OFFSET CURRENT (I_{OS})

The difference between the base currents at a specified collector voltage and current.

OFFSET CURRENT CHANGE ($\Delta I_{OS}/\Delta V_{CB}$)

The ratio of the change in offset current to the change in collector-base voltage producing it.

OFFSET VOLTAGE (V_{OS})

The difference between the base-emitter voltages (V_{BE_1}-V_{BE_2}) at a specified collector voltage and current.

CROSS REFERENCE — MAT-01 TO MONOLITHIC DUAL TRANSISTORS ($I_C = 10\mu A$)

DEVICE	BV_{CEO} MIN (V)	V_{OS} MAX (mV)	TCV_{OS} MAX ($\mu V/°C$)	h_{FE} MIN	I_{OS} MAX (nA)	TCI_{OS} MAX (pA/°C)
MAT-01AH	**45**	**0.1**	**0.5**	**500**	**0.6**	**90**
MAT-01H	**60**	**0.1**	**0.5**	**330**	**0.8**	**110**
MAT-01FH	**60**	**0.5**	**1.8**	**250**	**3.2**	**150**
MAT-01GH	**45**	**0.5**	**1.8**	**250**	**3.2**	**150**
LM114A	45	0.5	2.0	500	2.0	—
LM114	45	2.0	10	250	10	—
LM115A	60	0.5	2.0	250	2.0	—
LM115	60	2.0	10	250	10	—
AD810	35	3.0	15	100	2.0	600
AD811	45	1.5	7.5	200	10	300
AD812 DISCONTINUED	35	1.0	5.0	400	2.5	300
AD813	45	0.5	2.5	200	5	300
AD818	20	1.0	5.0	200	10	300

CROSS REFERENCE — MAT-01 TO 2N TYPES ($I_C = 10\mu A$)

DEVICE	BV_{CEO} MIN (V)	V_{OS} MAX (mV)	TCV_{OS} MAX ($\mu V/°C$)	h_{FE} MIN	$\%h_{FE}$ MATCH MAX	I_{OS} MAX (nA)	TCI_{OS} MAX (pA/°C)
MAT-01GH	**45**	**0.5**	**1.8**	**250**	**8**	**3.2**	**150**
2N2639	45	5.0	10	50	10	20	1000
2N2640	45	10	20	50	20	40	2000
2N2642	45	5.0	10	100	10	10	500
2N2643	45	10	20	100	20	20	375
2N2915	45	3.0	10	60	10	17	600
2N2915A	45	2.0	5.0	60	15	26	900
2N2916	45	5.0	10	150	10	7	N.C.
2N2916A	45	2.0	5.0	150	15	10	300
2N2917	45	10	20	60	20	17	1450
2N2918	45	5.0	20	150	20	7	750
MAT-01FH	**60**	**0.5**	**1.8**	**250**	**8**	**3.2**	**150**
2N2919	60	3.0	10	60	10	17	600
2N2919A	60	1.5	5.0	60	10	17	600
2N2920	60	3.0	10	150	10	7	N.C.
2N2920A	60	1.5	5.0	150	10	7	300
2N2060	60	5.0	10	25	10	40	N.C.
2N2060A	60	3.0	5.0	25	10	40	N.C.
2N2060B	60	1.5	5.0	25	10	40	N.C.

NOTES:
1. TCI_{OS} Max and I_{OS} Max calculated from published data.
2. N.C. = Insufficient published data to calculate.
3. All of the above are physically interchangeable pin-for-pin with MAT-01 series.

MAT-01

ULTRA-MATCHED MONOLITHIC DUAL TRANSISTOR

EXCELLENT LOG CONFORMANCE

FEATURES

- **Tight V_{OS} (V_{BE} Match) ..... 40μV Typical, 100μV Maximum**
- **Low TCV_{OS} ... 0.15μV/°C Typical, 0.5μV/°C Maximum**
- **Tight h_{FE} Match ..... 0.7% Typical, 3.0% Maximum**
- **High h_{FE} ..... 77- Typical, 500 Minimum**
- **Excellent h_{FE} Linearity from 10nA to 10mA**
- **High h_{FE} at Low I_C ..... 590 Typical @ I_C = 10nA**
- **Low Noise Voltage ..... 0.23μV_{p-p} — 0.1Hz to 10Hz**
- **Excellent Long-Term Stability ... 0.2μV/Month, Typical**
- **High Breakdown ..... 45V and 60V Minimum**
- **Precision Logarithmic Conformance**
- **Direct Replacement for Most Dual Transistors**

ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (mV)	PACKAGE	OPERATING TEMPERATURE RANGE
0.1	MAT01AH*	MIL
0.1	MAT01H*	MIL
0.5	MAT01GH*	MIL
0.5	MAT01FH*	MIL

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number.

†All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

ABSOLUTE MAXIMUM RATINGS (Note 4)

Collector-Base Voltage (BV_{CBO})
- MAT-01AH, GH, N 45V
- MAT-01H, FH 60V

Collector-Emitter Voltage (BV_{CEO})
- MAT-01AH, GH, N 45V
- MAT-01H, FH 60V

Collector-Collector Voltage (BV_{CC})
- MAT-01AH, GH, N 45V
- MAT-01H, FH 60V

Emitter-Emitter Voltage (BV_{EE})
- MAT-01AH, GH, N 45V
- MAT-01H, FH 60V

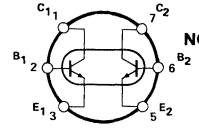
NOTES:

1. Application of reverse bias voltages in excess of rating shown can result in degradation of h_{FE} and h_{FE} matching characteristics. Do not attempt to measure BV_{EBO} greater than the 5V rating shown.

GENERAL DESCRIPTION

The MAT-01 series are monolithic ultra-tightly matched dual NPN transistors, fabricated using an exclusive Silicon Nitride "Triple-Passivation" process which provides extreme stability of critical parameters versus both temperature and time. Outstanding matching characteristics include offset voltage of 40μV, temperature drift of V_{OS} of 0.15μV/°C and h_{FE} matching of 0.7%. Very high h_{FE} is provided over a six decade range of collector current, including an exceptional h_{FE} of 590 at I_C = 10nA! Excellent logarithmic conformance over a seven decade collector current span suggests application in log/antilog and multiplier/divider circuitry. The very low values of noise voltage and current make the MAT-01 ideal for usage in critical low-level input stages while the 6-pin TO-99 package allows direct replacement of most previous dual transistors for immediate performance improvements. The very high h_{FE} at low collector currents also makes the MAT-01 attractive in all high impedance and micropower circuit designs.

PIN CONNECTIONS



NOTE: Substrate is connected to case

Emitter-Base Voltage (BV_{EBO}) (Note 1) 5V
Collector Current (I_C) 25mA
Emitter Current (I_E) 25mA
Total Power Dissipation
- Case Temperature ≤ 40°C (Note 2) 1.8W
- Ambient Temperaure ≤ 70°C (Note 3) 500mW

Operating Ambient Temperature ..... -55°C to +125°C
Operating Junction Temperature .....-55°C to +150°C
Storage Temperature .....-65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
DICE Junction Temperature ..... -65°C to +150°C

2. Rating applies to applications using heat sinking to control case temperature. Derate linearly at 16.4mW/°C for case temperatures above 40°C.
3. Rating applies to applications not using heat sinking; device in free air only. Derate linearly at 6.3mW/°C for ambient temperatures above 70°C.
4. Absolute maximum ratings apply to both DICE and packaged devices.

ELECTRICAL CHARACTERISTICS at V_{CB} = 15V, I_C = 10μA, T_A = 25°C, unless otherwise noted.

			MAT-01AH			MAT-01GH			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Breakdown Voltage	BV_{CEO}		45	—	—	45	—	—	V
Offset Voltage	V_{OS}		—	0.04	0.1	—	0.10	0.5	mV
Offset Voltage Stability									
First Month	V_{OS}/Time	(Note 1)	—	2.0	—	—	2.0	—	μV/Mo
Long-Term		(Note 2)	—	0.2	—	—	0.2	—	
Offset Current	I_{OS}		—	0.1	0.6	—	0.2	3.2	nA
Bias Current	I_B		—	13	20	—	18	40	nA
Current Gain	h_{FE}	I_C = 10nA	—	590	—	—	430	—	
		I_C = 10μA	500	770	—	250	560	—	
		I_C = 10mA	—	840	—	—	610	—	
Current Gain Match	Δh_{FE}		—	0.7	3.0	—	1.0	8.0	%
		100nA ≤ I_C ≤ 10mA	—	0.8	—	—	1.2	—	
Low Frequency Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	—	0.23	0.4	—	0.23	0.4	μV_{p-p}
Broadband Noise Voltage	e_{nRMS}	1Hz to 10kHz	—	0.60	—	—	0.60	—	μV_{RMS}
Noise		f_o = 10Hz	—	7.0	9.0	—	7.0	9.0	
Voltage Density	e_n	f_o = 100Hz (Note 3)	—	6.1	7.6	—	6.1	7.6	nV/√Hz
		f_o = 1000Hz	—	6.0	7.5	—	6.0	7.5	
Offset Voltage Change	$\Delta V_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ 30V	—	0.5	3.0	—	0.8	8.0	μV/V
Offset Current Change	$\Delta I_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ 30V	—	2.0	15	—	3.0	70	pA/V
Collector-Base Leakage Current	I_{CBO}	V_{CB} = 30V, I_E = 0 (Note 4)	—	15	50	—	25	200	pA
Collector-Emitter Leakage Current	I_{CES}	V_{CE} = 30V, V_{BE} = 0 (Note 4)	—	50	200	—	90	400	pA
Collector-Collector Leakage Current	I_{CC}	V_{CC} = 30V	—	20	200	—	30	400	pA
Collector Saturation Voltage	$V_{CE(SAT)}$	I_B = 0.1mA, I_C = 1mA	—	0.12	0.20	—	0.12	0.25	V
		I_B = 1mA, I_C = 10mA	—	0.8	—	—	0.8	—	
Gain-Bandwidth Product	f_T	V_{CE} = 10V, I_C = 10mA	—	450	—	—	450	—	MHz
Output Capacitance	C_{ob}	V_{CE} = 15V, I_E = 0	—	2.8	—	—	2.8	—	pF
Collector-Collector Capacitance	C_{CC}	V_{CC} = 0	—	8.5	—	—	8.5	—	pF

ELECTRICAL CHARACTERISTICS at V_{CB} = 15V, I_C = 10μA, -55°C ≤ T_A ≤ +125°C, unless otherwise noted

			MAT-01AH			MAT-01GH			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Offset Voltage	V_{OS}		—	0.06	0.15	—	0.14	0.70	mV
Average Offset Voltage Drift	TCV_{OS}	(Note 5)	—	0.15	0.50	—	0.35	1.8	μV/°C
Offset Current	I_{OS}		—	0.9	8.0	—	1.5	15.0	nA
Average Offset Current Drift	TCI_{OS}	(Note 5)	—	10	90	—	15	150	pA/°C
Bias Current	I_B		—	28	60	—	36	130	nA
Current Gain	h_{FE}		167	400	—	77	300	—	
Collector-Base Leakage Current	I_{CBO}	T_A = 125°C, V_{CB} = 30V, I_E = 0 (Note 4)	—	15	80	—	25	200	nA
Collector-Emitter Leakage Current	I_{CES}	T_A = 125°C, V_{CE} = 30V, V_{BE} = 0 (Note 4)	—	50	300	—	90	400	nA
Collector-Collector Leakage Current	I_{CC}	T_A = 125°C, V_{CC} = 30V	—	30	200	—	50	400	nA

NOTES:

1. Exclude first hour of operation to allow for stabilization of external circuitry.
2. Parameter describes long-term average drift trend after first month of operation.
3. Sample tested.
4. The collector-base (I_{CBO}) and collector-emitter (I_{CEO}) leakage currents may be reduced by a factor of two to ten times by connecting the substrate (package) to a potential which is lower than either collector voltage.
5. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at V_{CB} = 15V, I_C = 10μA, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-01H MIN	MAT-01H TYP	MAT-01H MAX	MAT-01FH MIN	MAT-01FH TYP	MAT-01FH MAX	UNITS
Breakdown Voltage	BV_{CEO}		60	—	—	60	—	—	V
Offset Voltage	V_{OS}		—	0.04	0.1	—	0.10	0.5	mV
Offset Voltage Stability									
First Month	V_{OS}/Time	(Note 1)	—	2.0	—	—	2.0	—	μV/Mo
Long-Term		(Note 2)	—	0.2	—	—	0.2	—	
Offset Current	I_{OS}		—	0.1	0.8	—	0.2	3.2	nA
Bias Current	I_B		—	15	30	—	18	40	nA
Current Gain	h_{FE}	I_C = 10nA	—	520	—	—	430	—	
		I_C = 10μA	330	680	—	250	560	—	
		I_C = 10mA	—	740	—	—	610	—	
Current Gain Match	Δh_{FE}		—	0.7	2.7	—	1.0	8.0	%
		100nA ≤ I_C ≤ 10mA	—	0.8	—	—	1.2	—	
Low Frequency Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	—	0.23	0.4	—	0.23	0.4	μV_{p-p}
Broadband Noise Voltage	e_{nRMS}	1Hz to 10kHz	—	0.60	—	—	0.60	—	μV_{RMS}
Noise		f_o = 10Hz	—	7.0	9.0	—	7.0	9.0	
Voltage Density	e_n	f_o = 100Hz (Note 3)	—	6.1	7.6	—	6.1	7.6	$nV/\sqrt{Hz}$
		f_o = 1000Hz	—	6.0	7.5	—	6.0	7.5	
Offset Voltage Change	$\Delta V_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ 45V	—	0.5	3.0	—	0.8	8.0	μV/V
Offset Current Change	$\Delta I_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ 45V	—	2.0	15	—	3.0	70	pA/V
Collector-Base Leakage Current	I_{CBO}	V_{CB} = 45V, I_E = 0 (Note 4)	—	15	50	—	25	200	pA
Collector-Emitter Leakage Current	I_{CES}	V_{CE} = 45V, V_{BE} = 0 (Note 4)	—	50	200	—	90	400	pA
Collector-Collector Leakage Current	I_{CC}	V_{CC} = 45V	—	20	200	—	30	400	pA
Collector Saturation Voltage	$V_{CE(SAT)}$	I_B = 0.1mA, I_C = 1mA	—	0.12	0.20	—	0.12	0.25	V
		I_B = 1mA, I_C = 10mA	—	0.8	—	—	0.8	—	
Gain-Bandwidth Product	f_T	V_{CE} = 10V, I_C = 10mA	—	450	—	—	450	—	MHz
Output Capacitance	C_{ob}	V_{CE} = 15V, I_E = 0	—	2.8	—	—	2.8	—	pF
Collector-Collector Capacitance	C_{CC}	V_{CC} = 0	—	8.5	—	—	8.5	—	pF

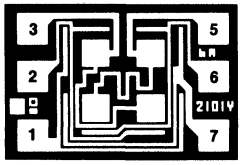
ELECTRICAL CHARACTERISTICS at V_{CB} = 15V, I_C = 10μA, -55°C ≤ T_A ≤ +125°C, unless otherwise noted

PARAMETER	SYMBOL	CONDITIONS	MAT-01H MIN	MAT-01H TYP	MAT-01H MAX	MAT-01FH MIN	MAT-01FH TYP	MAT-01FH MAX	UNITS
Offset Voltage	V_{OS}		—	0.06	0.15	—	0.14	0.70	mV
Average Offset Voltage Drift	TCV_{OS}	(Note 5)	—	0.15	0.50	—	0.35	1.8	μV/°C
Offset Current	I_{OS}		—	0.9	9.0	—	1.5	15.0	nA
Average Offset Current Drift	TCI_{OS}	(Note 5)	—	11	110	—	15	150	pA/°C
Bias Current	I_B		—	30	95	—	36	130	nA
Current Gain	h_{FE}		105	350	—	77	300	—	
Collector-Base Leakage Current	I_{CBO}	T_A = 125°C, V_{CB} = 45V, I_E = 0 (Note 4)	—	15	80	—	25	200	nA
Collector-Emitter Leakage Current	I_{CES}	T_A = 125°C, V_{CE} = 45V, V_{BE} = 0 (Note 4)	—	50	300	—	90	400	nA
Collector-Collector Leakage Current	I_{CC}	T_A = 125°C, V_{CC} = 45V	—	30	200	—	50	400	nA

NOTES:

1. Exclude first hour of operation to allow for stabilization of external circuitry.
2. Parameter describes long-term average drift trend after first month of operation.
3. Sample tested.
4. The collector-base (I_{CBO}) and collector-emitter (I_{CEO}) leakage currents may be reduced by a factor of two to ten times by connecting the substrate (package) to a potential which is lower than either collector voltage.
5. Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.035 × 0.025 inch

1. COLLECTOR (1)
2. BASE (1)
3. EMITTER (1)
5. EMITTER (2)
6. BASE (2)
7. COLLECTOR (2)

Refer to Section 2 for additional DICE information

ELECTRICAL CHARACTERISTICS at 25° C for V_{CB} = 15V and I_C = 10μA, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-01N LIMITS	UNITS
Breakdown Voltage	BV_{CEO}		45	V MIN
Offset Voltage	V_{OS}		0.5	mV MAX
Offset Current	I_{OS}		3.2	nA MAX
Bias Current	I_B		40	nA MAX
Current Gain	h_{FE}		250	MIN
Current Gain Match	Δh_{FE}		8.0	% MAX
Offset Voltage Change	$\Delta V_{OS}/\Delta V_{CB}$	$0 \le V_{CB} \le 30V$	8.0	μV/V MAX
Offset Voltage Change	$\Delta I_{OS}/\Delta V_{CB}$	$0 \le V_{CB} \le 30V$	70	pA/V MAX
Collector-Base-Leakage Current	I_{CBO}	V_{CB} = 30V, I_E = 0	200	pA MAX
Collector-Emitter-Leakage Current	I_{CES}	V_{CE} = 30V, V_{BE} = 0	400	pA MAX
Collector Saturation Voltage	$V_{CE(SAT)}$	I_B = 0.1mA, I_C = 1mA	0.25	V MAX

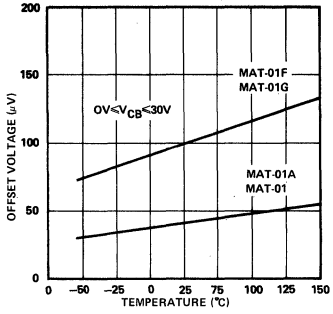
TYPICAL ELECTRICAL CHARACTERISTICS at V_{CB} = 15V and I_C = 10μA, T_A = 25° C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-01N TYPICAL	UNITS
Average Offset Voltage Drift	TCV_{OS}		0.35	μV/° C
Average Offset Current Drift	TCI_{OS}		15	pA/° C
Gain Bandwidth Product	f_T	V_{CE} = 10V, I_C = 10mA	450	MHz
Offset Voltage Stability	$\Delta V_{OS}/T$	First Month (Note 1) Long-Term (Note 2)	2.0 0.2	μV/Mo

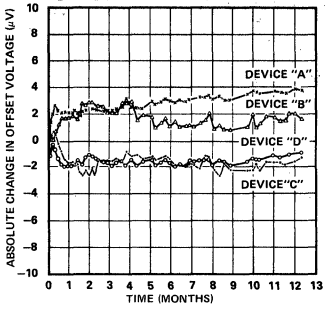
NOTES:
1. Exclude first hour of operation to allow for stabilization of external circuitry.
2. Parameter describes long-term average drift after first month of operation.

TYPICAL PERFORMANCE CURVES

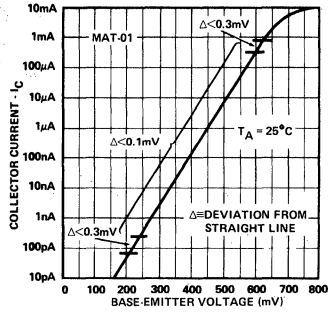
OFFSET VOLTAGE vs TEMPERATURE



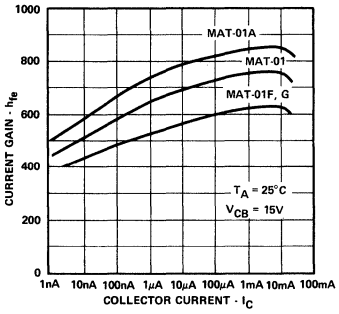
OFFSET VOLTAGE vs TIME



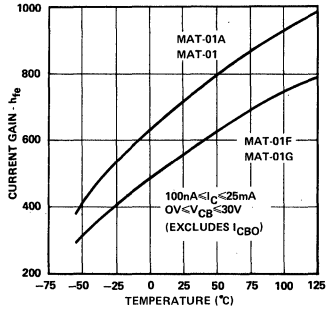
BASE-EMITTER VOLTAGE vs COLLECTOR CURRENT



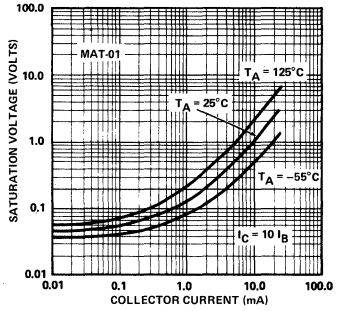
CURRENT GAIN vs COLLECTOR CURRENT



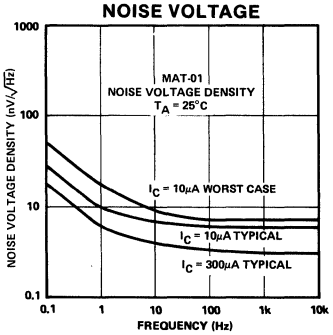
CURRENT GAIN vs TEMPERATURE



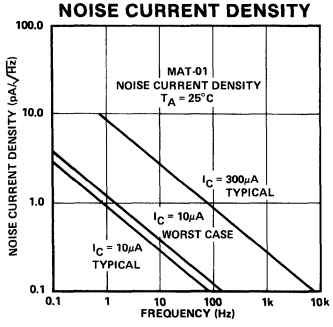
SATURATION VOLTAGE vs COLLECTOR CURRENT



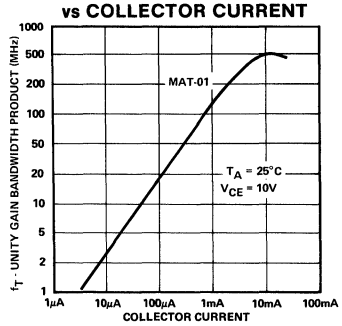
NOISE VOLTAGE



NOISE CURRENT DENSITY

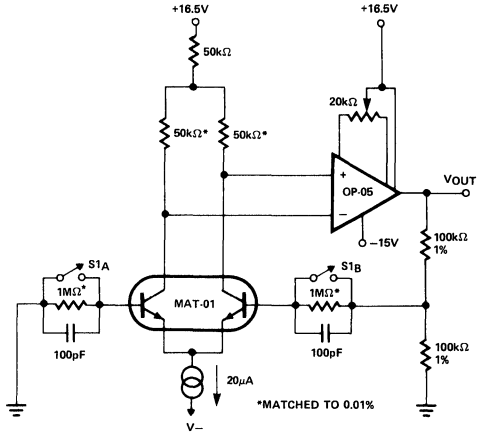


GAIN-BANDWIDTH vs COLLECTOR CURRENT



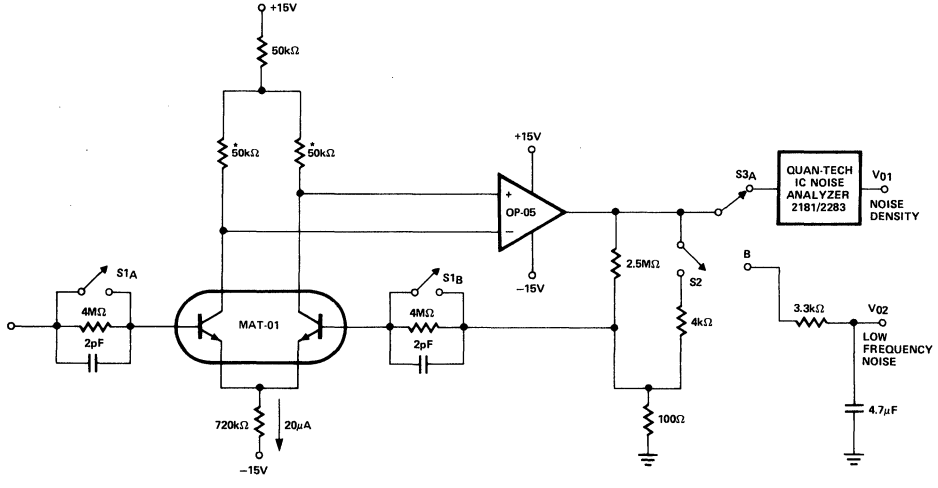
MAT-01 TEST CIRCUITS

MAT-01 MATCHING MEASUREMENT CIRCUIT



TEST	SI_A	SI_B	UNITS	
V_{OS}	X	X	V_{OUT_1}	1mV per volt
I_{OS}	O	O	$V_{OUT_2} - V_{OUT_1}$	1nA per volt

MAT-01 NOISE MEASUREMENT CIRCUIT



* Matched to 0.01%

TEST	SI_A	SI_B	S_2	S_3	READING
Noise Voltage Density (Per Transistor)	X	X	X	A	$V_{01}/\sqrt{2}$
Noise Current Density (Per Transistor)	O	O	X	A	$V_{01}/\sqrt{2.M\Omega}$
Low Frequency Noise (Referred to Input)	X	X	O	B	$\frac{V_{02}\ \text{PEAK-TO-PEAK}}{25{,}000}$

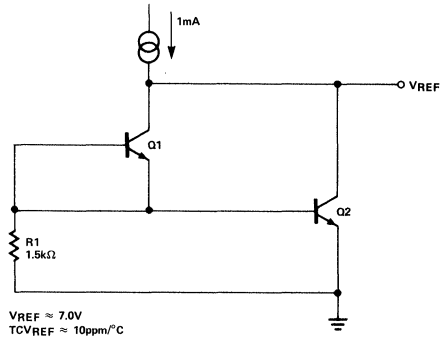
APPLICATION NOTES

Application of reverse bias voltages to the emitter-base junctions in excess of ratings (5V) may result in degradation of h_{FE} and h_{FE} matching characteristics; circuit designs should be checked to insure that such reverse bias voltages cannot be applied during transient conditions, such as at circuit turn-on and turn-off.

The designer is cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input terminals are maintained at the same temperature, preferably close to the temperature of the device's package.

TYPICAL APPLICATIONS

PRECISION REFERENCE

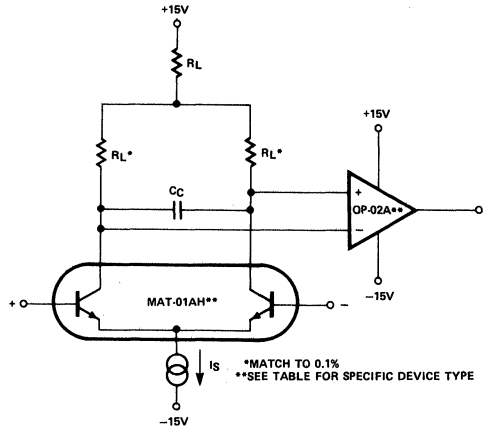


$V_{REF} \approx 7.0V$
$TCV_{REF} \approx 10ppm/°C$
$R_O \approx 40\Omega$

R_1 MAY BE ADJUSTED TO MINIMIZE TCV_{REF}. INCREASING R_1 WILL CAUSE A POSITIVE CHANGE IN TCV_{REF}.

NOTE: h_{FE} OF Q1 WILL BE REDUCED BY OPERATION OF BREAKDOWN MODE.

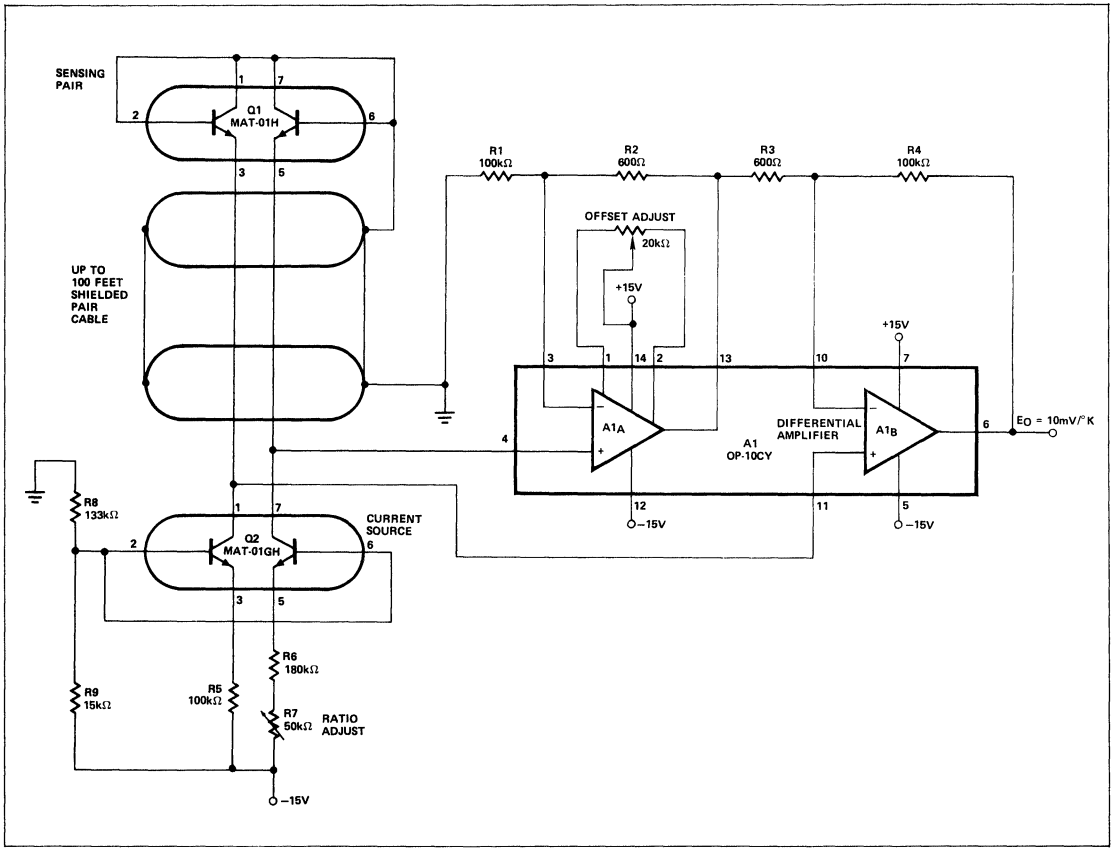
PRECISION OPERATIONAL AMPLIFIERS



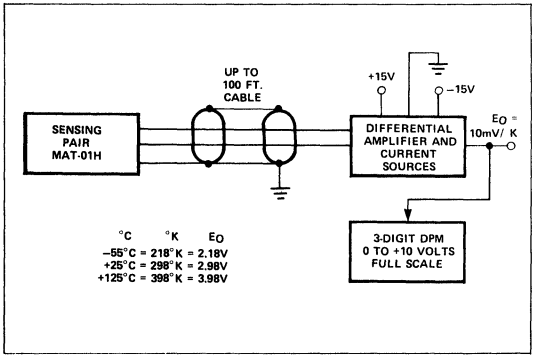
THIS CONFIGURATION CAN ALSO BE USED WITH THE LOW POWER OP-21 OR MICROPOWER OP-20 TO ACHIEVE A LOW NOISE AND LOW POWER PRECISION OP-AMP.

	MAT-01AH OP-02A	MAT-01AH OP-02A	MAT-01GH OP-02	MAT-01GH OP-02
V_{OS} Maximum	0.15mV	0.27mV	0.65mV	1.2mV
TCV_{OS} Maximum	0.6μV/°C	1μV/°C	2μV/°C	4μV/°C
I_{OS} Maximum	0.8nA	0.1nA	3.2nA	0.32nA
I_B Maximum	20nA	2nA	40nA	4nA
Gain Minimum	2,000,000	2,000,000	800,000	800,000
I_S	20μA	2μA	20μA	2μA
R_L	100kΩ	1MΩ	100kΩ	1MΩ

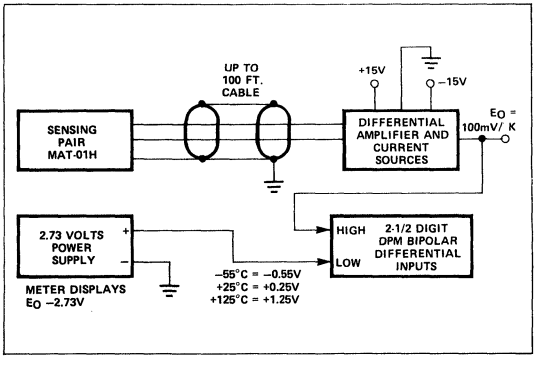
COMPLETE SCHEMATIC – TEMPERATURE MEASUREMENT SYSTEM



BASIC DIGITAL THERMOMETER READOUT IN DEGREES KELVIN (°K)



DIGITAL THERMOMETER WITH READOUT IN °C



NOTE:

For a complete discussion of the circuits above, see Application Note 12, "Temperature Measurement Method Based on Matched Transistor Pair Requires No Reference".

SECTION 9

VOLTAGE REFERENCES

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INTRODUCTION

Voltage references must provide a constant output voltage irrespective of changes in input voltage, output current or temperature. References find applications in many design situations: D to A's, power supplies, cold junction thermistor compensation circuits, A to D's, panel meters, calibration standards, precision current sources, and control set-point circuits.

Line regulation, load regulation (output impedance) and temperature coefficient specifications indicate how close a reference resembles an ideal voltage source. Line regulation specifies reference output voltage vs. input voltage changes. Output voltage changes due to load current variations are reflected by load regulation specifications. Temperature coefficient specifications indicate output voltage variation over temperature.

Present-day references are based on zener diodes or bandgap generated voltages. Zeners characteristically exhibit high power dissipation and poor noise specifications. Bandgap voltage reference designs sum voltages with negative and positive temperature coefficients to yield stable output voltages over temperature. A transistor base emitter junction voltage (V_{BE}) exhibits a negative temperature coefficient. Two transistors operating with unequal current densities will have different V_{BE}s and the difference, ΔV_{BE}, exhibits a positive temperature coefficient. When ΔV_{BE} is amplified and added to V_{BE}, a voltage level of near zero temperature coefficient results if the sum equals 1.23V. (See AN-18 for bandgap reference theory.) The 1.23V level then is amplified to provide stable output voltages of +5.00 and +10.00V.

PMI's exclusive "Zener Zapping" technique allows for trimming of the ΔV_{BE} amplification factor to insure low output voltage temperature coefficients. Additional zapping trims the output's absolute value within specified limits.

The REF-01 and REF-02 are stable +10.00V and +5.00V monolithic bandgap voltage references. Output voltages are adjustable for precision applications with small effect on output voltage temperature coefficients. The REF-02 provides an additional output voltage that has a linear temperature dependence. (See AN-18).

The REF-05 and REF-10 are premium versions of the REF-01 and REF-02 that have guaranteed long-term stability. Extensive testing over a long period of time, combined with tight control of processing has enabled PMI to specify limits on output change with time.

DEFINITIONS

LINE REGULATION

The ratio of the change in output voltage to the change in input (line) voltage producing it. It includes the effects of self-heating.

LOAD REGULATION

The ratio of the change in output voltage to the change in load current. It includes the effects of self-heating.

OUTPUT CHANGE WITH TEMPERATURE (ΔV_{OT})

The absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of the typical output voltage.

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{V_O \text{ (Typical)}} \times 100$$

OUTPUT TEMPERATURE COEFFICIENT (TCV_O)

The ratio of the output change with temperature to the specified temperature range expressed in ppm/°C. For example, TCV_O is defined as ΔV_{OT} divided by the temperature range; i.e.,

$$TCV_O(0° \text{ to } +70°C) = \frac{\Delta V_{OT}(0° \text{ to } +70°C}{70°C}$$

$$\text{and } TCV_O(-55° \text{ to } +125°C) = \frac{\Delta V_{OT}(-55° \text{ to } +125°C)}{180°C}$$

OUTPUT TURN-ON SETTLING TIME (t_{ON})

The time required for the output voltage to reach its final value within a specified error band after application of V_{IN}.

OUTPUT VOLTAGE NOISE (e_{np-p})

The peak-to-peak output noise voltage within a specified frequency band.

QUIESCENT SUPPLY CURRENT (I_{SY})

The current required from the supply to operate the device with no load.

REF-01

+10V PRECISION VOLTAGE REFERENCE

FEATURES

- **10 Volt Output** ..... **±0.3%**
- **Adjustment Range** ..... **±3%**
- **Excellent Temperature Stability** ..... **3ppm/°C**
- **Low Noise** **20μVp-p**
- **Low Power** **15mW**
- **Wide Input Voltage Range** ..... **12V to 40V**
- **High Load Driving Capability** **20mA**
- **No External Components**
- **Short Circuit Proof**
- **MIL-STD-883 Screening Available**

ORDERING INFORMATION†

$T_A = 25°C$ ΔV_O MAX (mV)	PACKAGE TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	OPERATING TEMP. RANGE
± 30	REF01AJ*	REF01AZ*		MIL
± 30	REF01EJ	REF01EZ		COM
± 50	REF01J*	REF01Z*		MIL
± 50	REF01HJ	REF01HZ	REF01HP	COM
± 100	REF01CJ	REF01CZ	REF01CP	COM
± 150	REF01DJ	REF01DZ	REF01DP	COM

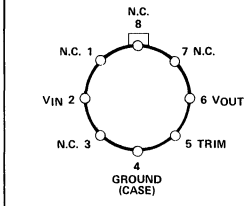
* Also available with Mil-STD-883B processing. To order add /883 as a suffix to the part number.

† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

GENERAL DESCRIPTION

The REF-01 Precision Voltage Reference provides a stable +10V output which can be adjusted over a ±3% range with minimal effect on temperature stability. Single supply operation over an input voltage range of 12V to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise and low power make the REF-01 an excellent choice whenever a stable voltage reference is required. Applications include D/A and A/D converters, portable instrumentation, and digital voltmeters. Full miltary temperature range devices with screening to MIL-STD-883 are available. For guaranteed long term drift see REF-10 data sheet.

PIN CONNECTIONS

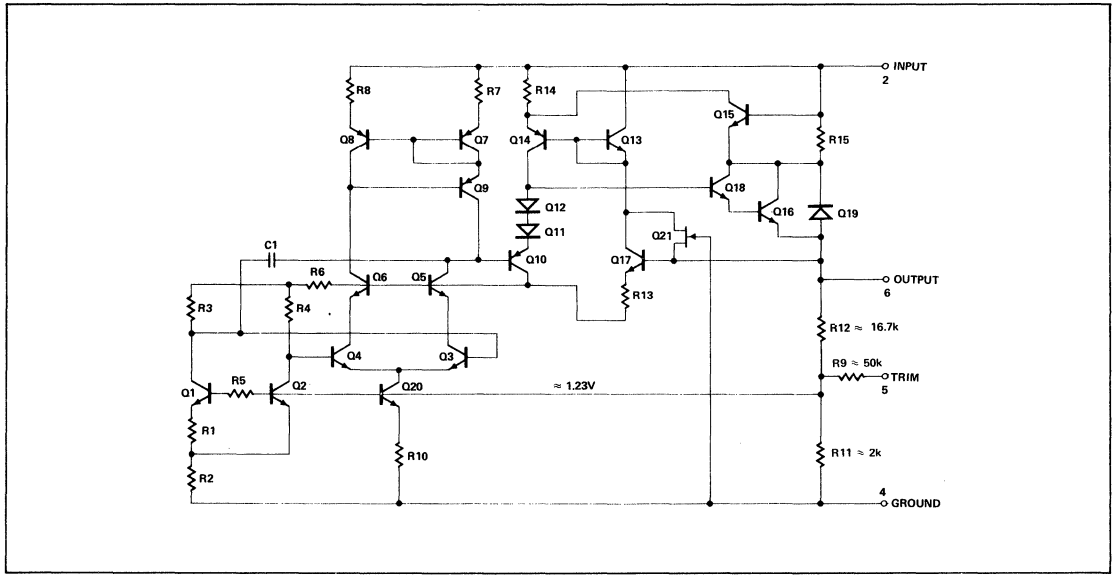


TO-99 (J-Suffix)

EPOXY B MINI-DIP (P-Suffix)

8-PIN HERMETIC DIP (Z-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 2)

Input Voltage
- REF-01, A, E, H, All DICE except GR 40V
- REF-01C, D, GR DICE only 30V

Power Dissipation (Note 1) 500mW
Output Short Circuit Duration ..... indefinite (to ground or V_{IN})
Storage Temperature Range
- J and Z Packages ..... −65°C to +150°C
- P Package ..... −65°C to +125°C

Operating Temperature Range
- REF-01A, REF-01 ..... −55°C to + 125°C
- REF-01E, REF-01H
- REF-01D, REF-01C ..... 0°C to +70°C

DICE Junction Temperature (T_j) ..... −65°C to +150°C
Lead Temperature (Soldering, 60 sec.) ..... 300°C

NOTES:
1. See table for maximum ambient temperature rating and derating factor.

	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8 Pin Hermetic Dip (Z)	75°C	6.7mW/°C
8 Pin Plastic Dip (P)	36°C	5.6mW/°C

2. Absolute maximum ratings apply to both packaged parts and dice, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V_{IN} = +15V, T_A = 25°C, unless otherwise noted.

			REF-01A/E			REF-01/H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Output Voltage	V_O	I_L = 0mA	9.97	10.00	10.03	9.95	10.00	10.05	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±3.0	±3.3	—	±3.0	±3.3	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 5)	—	20	30	—	20	30	μVp-p
Input Voltage Range	V_{IN}		12	—	40	12	—	40	V
Line Regulation (Note 4)		V_{IN} = 13 to 33V	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 4)		I_L = 0 to 10mA	—	0.005	0.008	—	0.006	0.010	%/mA
Turn-on Settling Time	t_{on}	To ±0.1% of final value	—	5.0	—	—	5.0	—	μsec.
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S		−0.3	−0.5	—	−0.3	−0.5	—	mA
Short Circuit Current	I_{SC}	V_O = 0	—	30	—	—	30	—	mA

ELECTRICAL CHARACTERISTICS at V_{IN} = +15V, −55°C ≤ T_A ≤ +125°C and I_L = 0mA, unless otherwise noted.

			REF-01A/E			REF-01/H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Output Voltage Change with Temperature (Notes 1 and 2)	ΔV_{OT}	0° ≤ T_A ≤ +70°C −55° ≤ T_A ≤ +125°C	— —	0.02 0.06	0.06 0.15	— —	0.07 0.18	0.17 0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	—	3.0	8.5	-	10.0	25.0	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10kΩ	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (V_{IN} = 13 to 33V) (Note 4)		0° ≤ T_A ≤ +70°C −55° ≤ T_A ≤ +125°C	— —	0.007 0.009	0.012 0.015	— —	0.007 0.009	0.012 0.015	%/V
Load Regulation (I_L = 0 to 8mA) (Note 4)		0° ≤ T_A ≤ +70°C −55° ≤ T_A ≤ +125°C	— —	0.006 0.007	0.010 0.012	— —	0.007 0.009	0.012 0.015	%/mA

NOTES:

1. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{10V} \times 100$$

2. ΔV_{OT} specification applies trimmed to +10.000V or untrimmed.
3. TCV_O is defined as ΔV_{OT} divided by the temperature range; i.e.,

$$TCV_O(0° \text{ to } +70°C) = \frac{\Delta V_{OT}\ 0° \text{ to } +70°C}{70°C}$$

$$\text{and } TCV_O\ (-55° \text{ to } +125°C) = \frac{\Delta V_{OT}\ -55 \text{ to } +125°C}{180°C}$$

4. Line and Load Regulation specifications include the effects of self heating.
5. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at V_{IN} = +15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-01C MIN	REF-01C TYP	REF-01C MAX	REF-01D MIN	REF-01D TYP	REF-01D MAX	UNITS
Output Voltage	V_O	I_L = 0mA	9.90	10.00	10.10	9.850	10.00	10.150	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±2.7	±3.3	—	±2.0	±3.3	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 5)	—	25	35	—	25	—	μVp-p
Input Voltage Range	V_{IN}		12	—	30	12	—	30	V
Line Regulation (Note 4)		V_{IN} = 13 to 30V	—	0.009	0.015	—	0.012	0.04	%/V
Load Regulation (Note 4)		I_L = 0 to 8mA I_L = 0 to 4mA	— —	0.006 0.006	0.015 0.015	— —	— 0.009	— 0.04	%/mA
Turn-on Settling Time	t_{on}	To ±0.1% of final value	—	5.0	—	—	5.0	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.6	—	1.0	2.0	mA
Load Current	I_L		8	21	—	8	21	—	mA
Sink Current	I_S		−0.2	−0.5	—	−0.2	−0.5	—	mA
Short Circuit Current	I_{SC}	V_O = 0	—	30	—	—	30	—	mA

ELECTRICAL CHARACTERISTICS at V_{IN} = +15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-01C MIN	REF-01C TYP	REF-01C MAX	REF-01D MIN	REF-01D TYP	REF-01D MAX	UNITS
Output Voltage Change with Temperature	ΔV_{OT}	(Notes 1 and 2)	—	0.14	0.45	—	0.49	1.7	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	—	20	65	—	70	250	ppm/°C
Change in V_O Temperature Coefficient With Output Adjustment		R_p = 10kΩ	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (Note 4)		V_{IN} = 13 to 30V	—	0.011	0.018	—	0.020	0.025	%/V
Load Regulation (Note 4)		I_L = 0 to 5 mA	—	0.008	0.018	—	0.020	0.025	%/mA

NOTES:

1. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V:

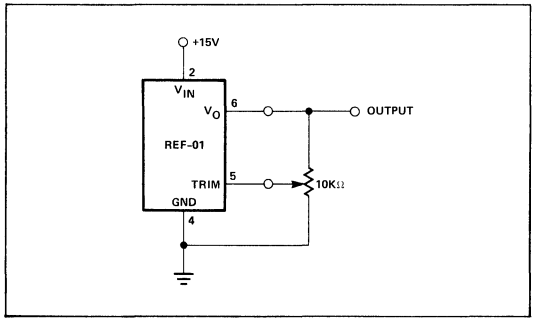
$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{10V} \times 100$$

2. ΔV_{OT} specification applies trimmed to +10.000V or untrimmed.
3. TCV_O is defined as ΔV_{OT} divided by the temperature range; i.e.,

$$TCV_O = \frac{\Delta V_{OT}}{70°C}$$

4. Line and Load Regulation specifications include the effects of self heating.
5. Guaranteed by design.

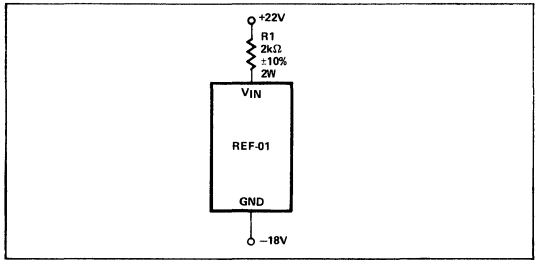
OUTPUT ADJUSTMENT



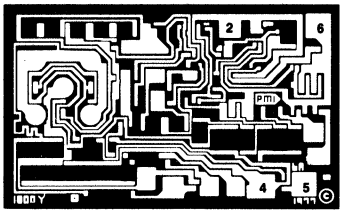
The REF-01 trim terminal can be used to adjust the output voltage over a 10V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 10V. Of course, the output can also be set to exactly 10.000V, or to 10.240V for binary applications.

Adjustment of the output does not significantly affect the temperature performance of the device. Typically the temperature coefficient change is 0.7 ppm/°C for 100mV of output adjustment.

BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.063 X 0.040 inch

2. INPUT VOLTAGE (V_{IN})
4. GROUND
5. TRIM
6. OUTPUT VOLTAGE (V_{OUT})

Refer to Section 2 for additional DICE information

ELECTRICAL CHARACTERISTICS at V_S = + 15V, T_A = + 25°C, unless otherwise noted.

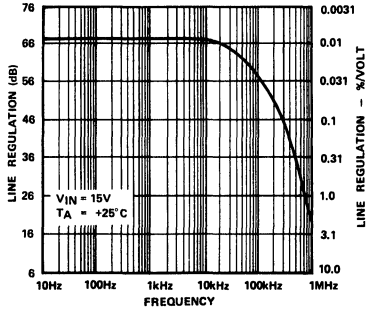
PARAMETER	SYMBOL	CONDITIONS	REF-01N LIMIT	REF-01G LIMIT	REF-01GR LIMIT	UNITS
Output Voltage	V_O	I_L = 0	10.05 9.95	10.05 9.85	10.20 9.80	V MAX V MIN
Output Adjustment Range	V_{trim}	R_P = 10kΩ	± 3.0	± 2.7	—	% MIN
Input Voltage Range	V_{IN}		40 12	40 12	30 12	V MAX V MIN
Line Regulation		V_{IN} = 13V to 33V V_{IN} = 13V to 30V	0.01 —	0.01 —	— 0.015	%/V MAX

TYPICAL ELECTRICAL CHARACTERISTICS at V_S = ± 15V, T_A = 25°C, unless otherwise noted.

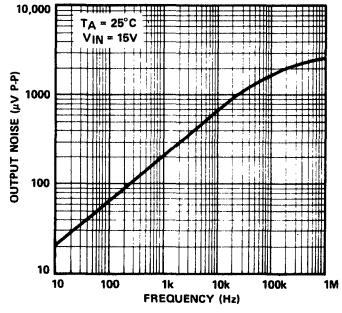
PARAMETER	SYMBOL	CONDITIONS	REF-01N TYPICAL	REF-01G TYPICAL	REF-01GR TYPICAL	UNITS
Load Regulation		I_L = 0 to 10mA I_L = 0 to 8mA	0.006 —	0.006 —	— 0.006	%/mA
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz	20	20	25	μV_{p-p}
Turn-On Settling Time	t_{ON}	To ± 0.01% of Final Value	5.0	5.0	5.0	μs
Quiescent Current	I_{SY}	No Load	1.0	1.0	1.0	mA
Load Current	I_L		21	21	21	mA
Sink Current	I_S		0.5	0.5	0.5	mA
Short Circuit Current	I_{SC}	V_O = 0	30	30	30	mA
Output Voltage Temperature Coefficient	TCV_O		10	10	20	ppm/°C

TYPICAL PERFORMANCE CURVES

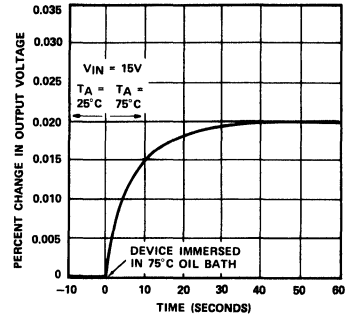
LINE REGULATION vs FREQUENCY



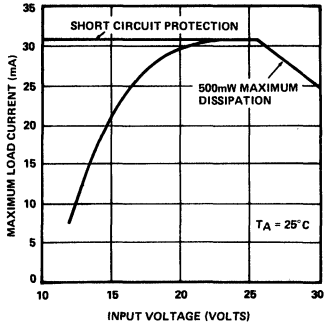
OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



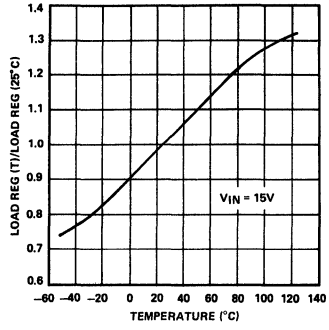
OUTPUT CHANGE DUE TO THERMAL SHOCK



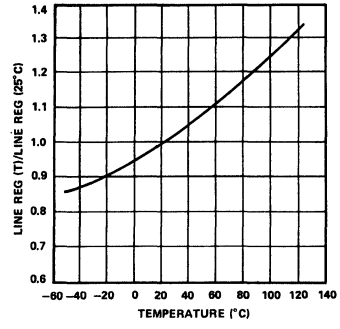
MAXIMUM LOAD CURRENT vs INPUT VOLTAGE



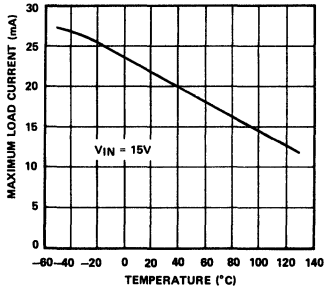
NORMALIZED LOAD REGULATION (ΔI_L = 10mA) vs TEMPERATURE



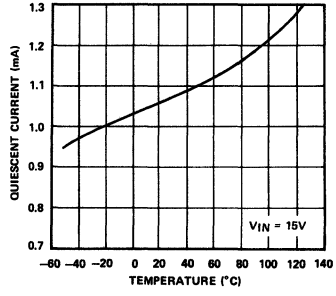
NORMALIZED LINE REGULATION vs TEMPERATURE



MAXIMUM LOAD CURRENT vs TEMPERATURE

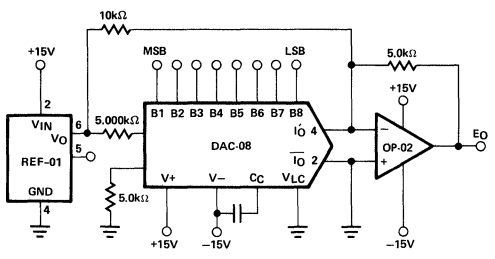


QUIESCENT CURRENT vs TEMPERATURE



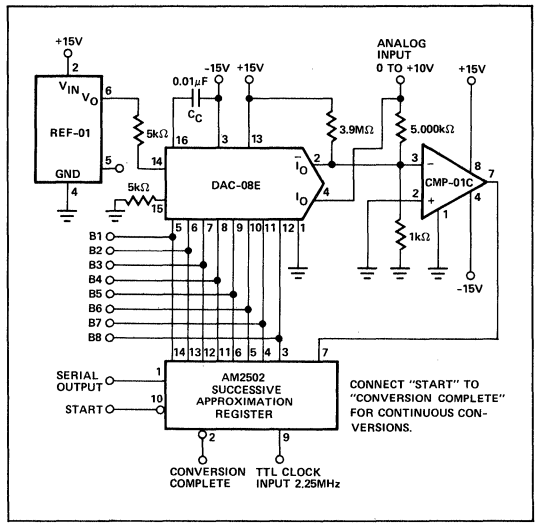
TYPICAL APPLICATIONS

D/A CONVERTER REFERENCE

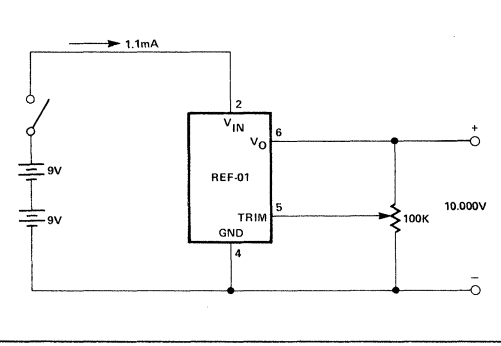


	B1	B2	B3	B4	B5	B6	B7	B8	E
POS FULL SCALE −1 LSB	1	1	1	1	1	1	1	1	+4.960
ZERO SCALE	1	0	0	0	0	0	0	0	0.000
NEG FULL SCALE +1 LSB	0	0	0	0	0	0	0	1	−4.960
NEG FULL SCALE	0	0	0	0	0	0	0	0	−5.000

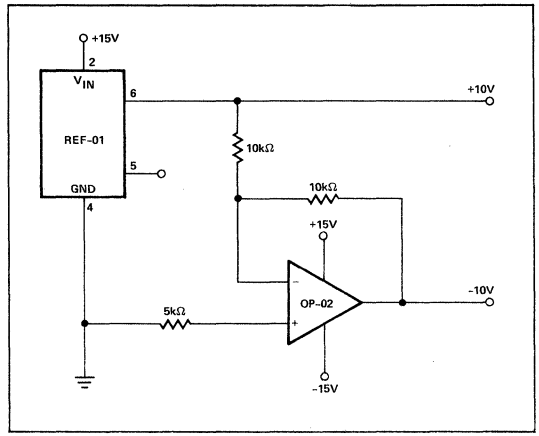
A/D CONVERTER REFERENCE



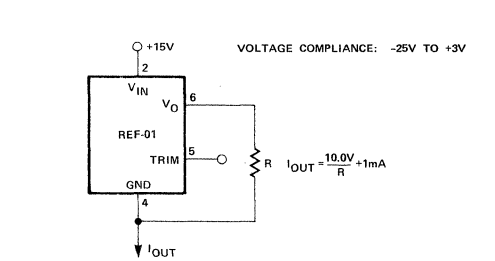
PRECISION CALIBRATION STANDARD



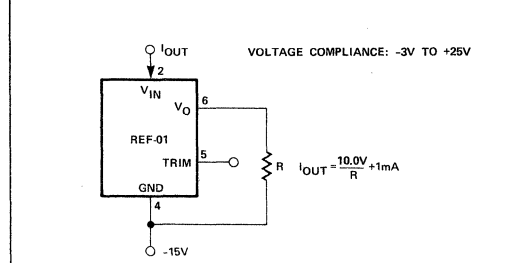
±10V REFERENCE



CURRENT SOURCE



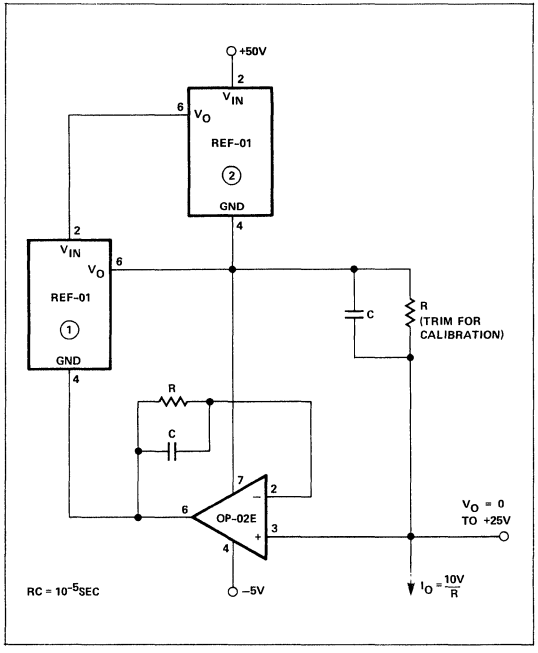
CURRENT SINK



PRECISION CURRENT SOURCE

A current source with 25V output compliance and excellent output impedance can be obtained using this circuit. REF-01 ② keeps the line voltage and power dissipation constant in device ①; the only important error consideration at room temperature is the negative supply rejection of the op amp. The typical 3μV/V PSRR of the OP-02E will create an 8ppm change (3μV/V × 25V/10V) in output current over a 25V range; for example, a 10mA current source can be built (R = 1kΩ) with 300MΩ output impedance.

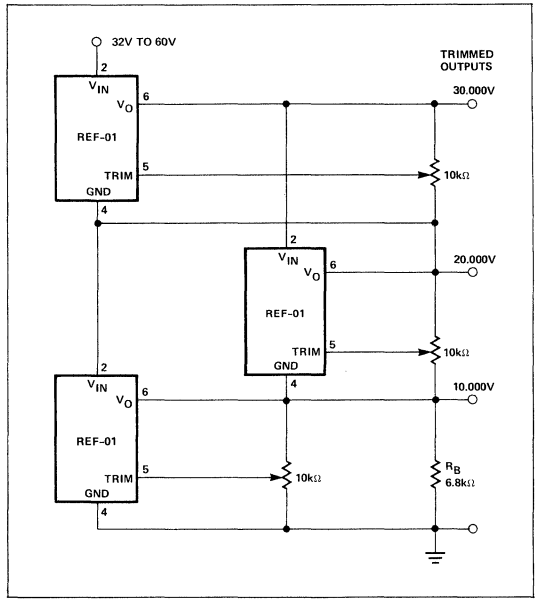
$$R_O = \frac{25V}{8x10^{-6}x10mA}$$



REFERENCE STACK WITH EXCELLENT LINE REGULATION

Three REF-01's can be stacked to yield 10.000, 20.000 and 30.000V outputs. An additional advantage is near-perfect line regulation of the 10.000 and 20.000 output voltages. A 32V to 60V input change produces an output change which is less than the noise voltage of the devices. A load bypass resistor (R_B) provides a path for the supply current (I_{SY}) of the 20.000V regulator.

In general, any number of REF-01's can be stacked this way. For example, ten devices will yield outputs of 10, 20, 30 . .. 100V. The line voltage can range from 105V to 130V. However, care must be taken to ensure that the total load currents do not exceed the maximum usable current (typically 21mA).



REF-02

+5V PRECISION VOLTAGE REFERENCE/TEMPERATURE TRANSDUCER

FEATURES

- 5 Volt Output ..... ±0.3%
- Temperature Voltage Output ..... 2.1mV/°C
- Adjustment Range ..... ±6%
- Excellent Temperature Stability ..... 3ppm/°C
- Low Noise ..... $10\mu V_{p-p}$
- Low Power 15mW
- Wide Input Voltage Range ..... 7V to 40V
- High Load Driving Capability 20mA
- No External Components
- Short Circuit Proof
- MIL-STD-883 Screening Available

ORDERING INFORMATION†

T_A = 25°C ΔV_O MAX (mV)	PACKAGE TO-99 8-PIN	PACKAGE HERMETIC DIP 8-PIN	PACKAGE PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
±15	REF02AJ*	REF02AZ*		MIL
±15	REF02EJ	REF02EZ		COM
±25	REF02J*	REF02Z*		MIL
±25	REF02HJ	REF92HZ	REF02HP	COM
±50	REF02CJ	REF02CZ	REF02CP	COM
±100	REF02DJ	REF02DZ	REF02DP	COM

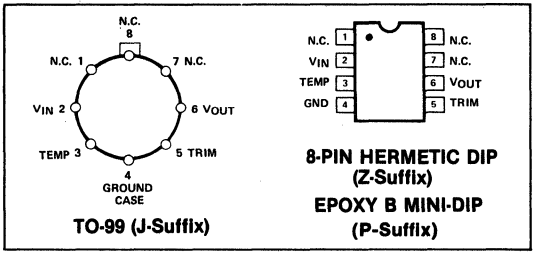
*Also available with MIL-STD-883 processing. To order add /883 as a suffix to the part number.

†All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

GENERAL DESCRIPTION

The REF-02 Precision Voltage Reference provides a stable +5V output which can be adjusted over a ±6% range with minimal effect on temperature stability. Single supply operation over an input voltage range of 7V to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise and low power make the REF-02 an excellent choice whenever a stable voltage reference is required. Applications include D/A and A/D converters, portable instrumentation, and digital voltmeters. The versatility of the REF-02 is enhanced by its use as a monolithic temperature transducer. (See AN-18 "Thermometer Applications of the REF-02.") For +10V Precision Voltage References see the REF-01 and REF-10 data sheets. For guaranteed long term drift see the REF-05 data sheet.

PIN CONNECTIONS

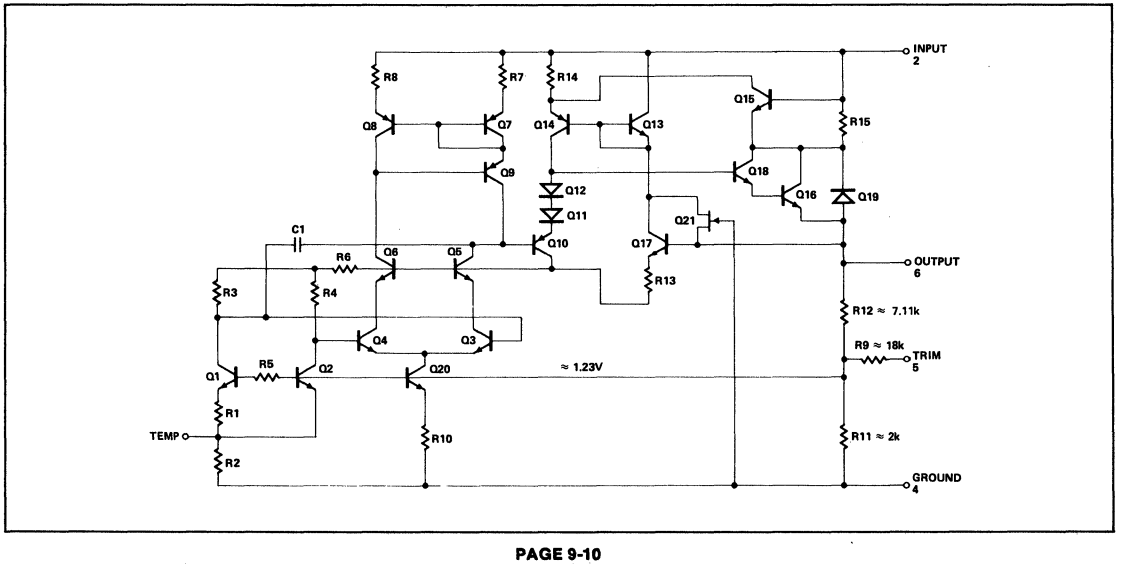


TO-99 (J-Suffix)

8-PIN HERMETIC DIP (Z-Suffix)

EPOXY B MINI-DIP (P-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 2)

Input Voltage
- REF-02, A, E, H 40V
- REF-02C, D 30V

Power Dissipation (Note 1) 500mW

Output Short Circuit Duration
- (to Ground or V_{IN}) ..... Indefinite

Storage Temperature Range
- J and Z Packages ..... −65°C to +150°C
- P Package ..... −65°C to +125°C

Operating Temperature Range
- REF-02A, REF-02 ..... −55°C to +125°C
- REF-02E, REF-02H ..... 0°C to +70°C
- REF-02C, REF-02D ..... 0°C to +70°C

Lead Temperature (Soldering, 60 sec) ..... 300°C

DICE Junction Temperature (T_j) ..... −65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERTURE
TO-99 (J)	80°C	7.1mW/°C
8 Pin Hermetic Dip (Z)	75°C	6.7mW/°C
8 Pin Plastic Dip (P)	36°C	5.6mW/°C

2. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V_{IN} = +15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-02A/E MIN	REF-02A/E TYP	REF-02A/E MAX	REF-02/H MIN	REF-02/H TYP	REF-02/H MAX	UNITS
Output Voltage	V_O	I_L = 0mA	4.985	5.000	5.015	4.975	5.000	5.025	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±3.0	±6.0	—	±3.0	±6.0	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 1)	—	10	15	—	10	15	μV_{p-p}
Input Voltage Range	V_{IN}		7	—	40	7	—	40	V
Line Regulation (Note 2)		V_{IN} = 8 to 33V	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 2)		I_L = 0 to 10mA	—	0.005	0.010	—	0.006	0.010	%/mA
Turn-on Settling Time	t_{on}	To ±0.1% of final value	—	5.0	—	—	5.0	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S		−0.3	−0.5	—	−0.3	−0.5	—	mA
Short Circuit Current	I_{SC}	V_O = 0	—	30	—	—	30	—	mA
Temperature Voltage Output	V_T	(Note 3)	—	630	—	—	630	—	mV

ELECTRICAL CHARACTERISTICS at V_{IN} = +15V, −55°C ≤ T_A ≤ +125°C for REF-02A and REF-02, 0°C ≤ T_A ≤ +70°C for REF-02E and REF-02H, I_L = 0mA, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-02A/E MIN	REF-02A/E TYP	REF-02A/E MAX	REF-02/H MIN	REF-02/H TYP	REF-02/H MAX	UNITS
Output Voltage Change with Temperature (Notes 4 and 5)	ΔV_{OT}	0°C ≤ T_A ≤ +70°C	—	0.02	0.06	—	0.07	0.17	%
	ΔV_{OT}	−55°C ≤ T_A ≤ +125°C	—	0.06	0.15	—	0.18	0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 6)	—	3	8.5	—	10	25	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10kΩ	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (V_{IN} = 8 to 33V) (Note 2)		0°C ≤ T_A ≤ +70°C	—	0.007	0.012	—	0.007	0.012	%/V
		−55°C ≤ T_A ≤ +125°C	—	0.009	0.015	—	0.009	0.015	%/V
Load Regulation (I_L = 0 to 8mA) (Note 2)		0°C ≤ T_A ≤ +70°C	—	0.006	0.010	—	0.007	0.012	%/mA
		−55°C ≤ T_A ≤ +125°C	—	0.007	0.012	—	0.009	0.015	%/mA
Temperature Voltage Output Temperature Coefficient	TCV_T	(Note 3)	—	2.1	—	—	2.1	—	mV/°C

NOTES:

1. Guaranteed by design.
2. Line and Load Regulation specifications include the effect of self heating.
3. Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
4. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V.

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{5V} \times 100$$

5. ΔV_{OT} specification applied trimmed to +5.000V or untrimmed.
6. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O = \frac{\Delta V_{OT}}{70°C}$$

ELECTRICAL CHARACTERISTICS at V_{IN} = +15V, T_A = 25°C, unless otherwise noted.

			REF-02C			REF-02D			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Output Voltage	V_O	I_L = 0mA	4.950	5.000	5.050	4.900	5.000	5.100	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±2.7	±6.0	—	±2.0	±6.0	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 1)	—	12	18	—	12	—	μV_{p-p}
Input Voltage Range	V_{IN}		7	—	30	7	—	30	V
Line Regulation (Note 2)		V_{IN} = 8 to 30V	—	0.009	0.015	—	0.010	0.04	%/V
Load Regulation (Note 2)		I_L = 0 to 8mA	—	0.006	0.015	—	—	—	%/mA
		I_L = 0 to 4mA	—	—	—	—	0.015	0.04	%/mA
Turn-on Settling Time	t_{on}	To ±0.1% of final value	—	5.0	—	—	5.0	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.6	—	1.0	2.0	mA
Load Current	I_L		8	21	—	8	21	—	mA
Sink Current	I_S		−0.2	−0.5	—	−0.2	−0.5	—	mA
Short Circuit Current	I_{SC}	V_O = 0	—	30	—	—	30	—	mA
Temperature Voltage Output	V_T	(Note 3)	—	630	—	—	630	—	mV

ELECTRICAL CHARACTERISTICS at V_{IN} = +15V, 0°C ≤ T_A ≤ +70°C and I_L = 0mA, unless otherwise noted.

			REF-02C			REF-02D			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Output Voltage Change with Temperature	ΔV_{OT}	(Notes 4 and 5)	—	0.14	0.45	—	0.49	1.7	%
Output Voltage Temperature Coefficient	TCV_O	(Note 6)	—	20	65	—	70	250	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10kΩ	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (Note 2)		V_{IN} = 8 to 30V	—	0.011	0.018	—	0.012	0.025	%/V
Load Regulation (Note 2)		I_L = 0 to 5mA	—	0.008	0.018	—	0.016	0.025	%/mA
Temperature Voltage Output Temperature Coefficient	TCV_T	(Note 3)	—	2.1	—	—	2.1	—	mV/°C

NOTES:

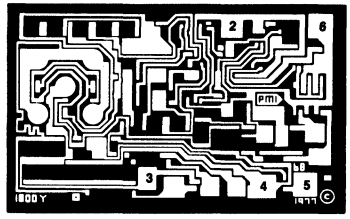
1. Guaranteed by design.
2. Line and Load Regulation specifications include the effect of self heating.
3. Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
4. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V.

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{5V} \times 100$$

5. ΔV_{OT} specification applied trimmed to +5.000V or untrimmed.
6. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O = \frac{\Delta V_{OT}}{70°C}$$

DICE CHARACTERISTICS



DIE SIZE 0.063 × 0.040 inch

2. INPUT VOLTAGE (V_{IN})
3. TEMPERATURE TRANSDUCER OUTPUT VOLTAGE (TEMP)
4. GROUND
5. TRIM
6. OUTPUT VOLTAGE (V_{OUT})

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at $V_S = +15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-02N LIMIT	REF-02G LIMIT	REF-02GR LIMIT	UNITS
Output Voltage	V_O	$I_L = 0$	4.975 5.025	4.925 5.075	4.90 5.10	V MIN V MAX
Output Adjustment Range	ΔV_{trim}	$R_P = 10K\Omega$	±3.0	±3.0	—	% MIN
Input Voltage Range	V_{IN}		7 40	7 40	7 30	V MIN V MAX
Line Regulation		$V_{IN} = 8V$ to $33V$ $V_{IN} = 8V$ to $30V$	0.01 —	0.01 —	— 0.015	%/V

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = +15V$, $T_A = +25°C$, unless otherwise noted.

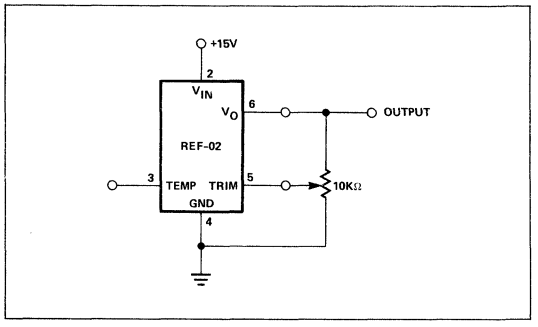
PARAMETER	SYMBOL	CONDITIONS	REF-02N TYPICAL	REF-02G TYPICAL	REF-02GR TYPICAL	UNITS
Temp. Voltage Output	V_T	(Note)	630	630	630	mV
Temp. Voltage Output Temp. Coefficient	TCV_T	(Note)	2.1	2.1	2.1	mV/°C
Output Voltage Temp. Coefficient	TCV_O		10	10	20	ppm/°C
Load Regulation		$I_L = 0mA$ to $10mA$ $I_L = 0mA$ to $8mA$	0.006 —	0.006 —	— 0.006	%/mA
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz	20	25	25	μVp-p
Turn-On Settling Time	t_{ON}	To ±0.1% of Final Value	5.0	5.0	5.0	μs
Quiescent Supply Current	I_{SY}	No Load	1.0	1.0	1.0	mA
Load Current	I_L		21	21	21	mA
Sink Current	I_S		−0.5	−0.5	−0.5	mA
Short Circuit Current	I_{SC}	$V_O = 0$	30	30	30	mA

NOTES:
1. See AN-18 for detailed REF-02 thermometer applications information.
2. Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.

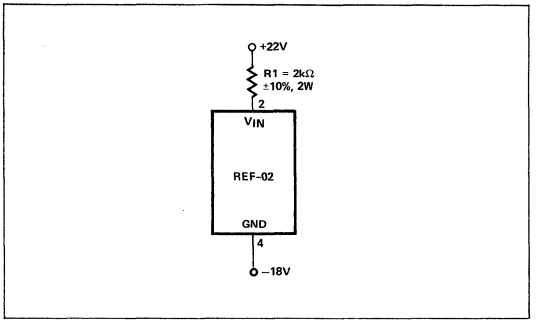
OUTPUT ADJUSTMENT

The REF-02 trim terminal can be used to adjust the output voltage over a 5V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 5V. Of course, the output can also be set to exactly 5.000V or to 5.12V for binary applications.

Adjustment of the output does not significantly affect the temperature performance of the device. Typically the temperature coefficient change is 0.7ppm/°C for 100mV of output adjustment.

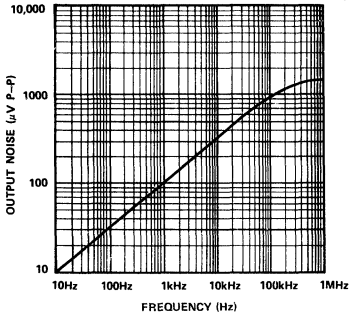


BURN-IN CIRCUIT

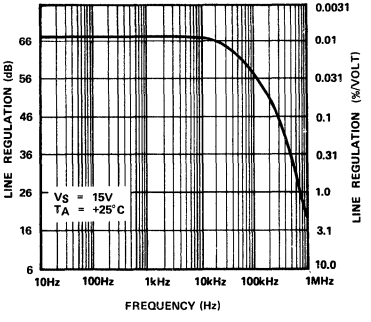


TYPICAL PERFORMANCE CURVES

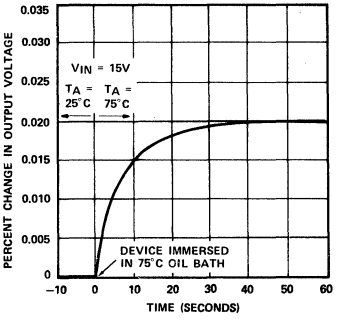
OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



LINE REGULATION vs FREQUENCY

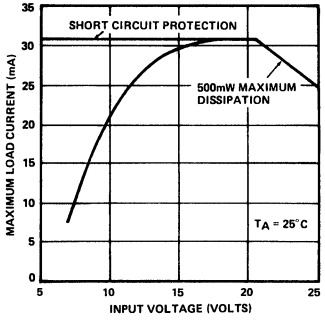


OUTPUT CHANGE DUE TO THERMAL SHOCK

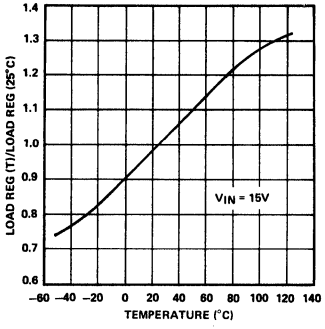


TYPICAL PERFORMANCE CURVES

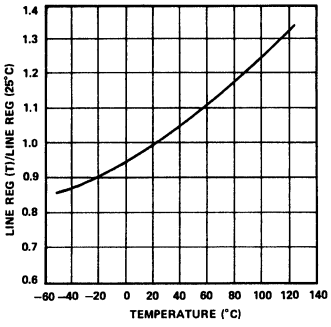
MAXIMUM LOAD CURRENT vs INPUT VOLTAGE



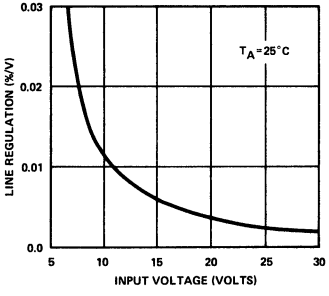
NORMALIZED LOAD REGULATION (ΔI_L = 10mA) vs TEMPERATURE



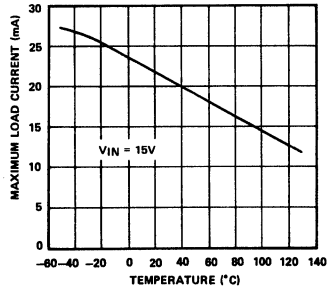
NORMALIZED LINE REGULATION vs TEMPERATURE



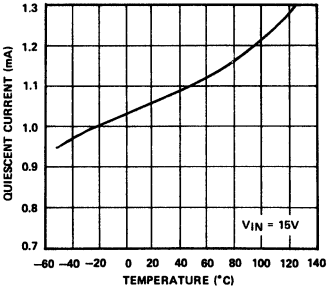
LINE REGULATION vs SUPPLY VOLTAGE



MAXIMUM LOAD CURRENT vs TEMPERATURE

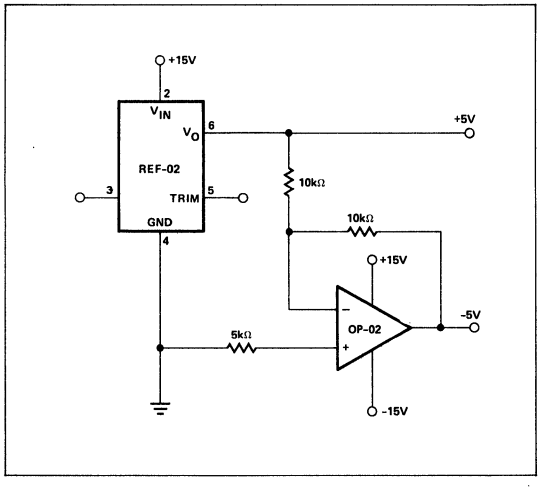


QUIESCENT CURRENT vs TEMPERATURE

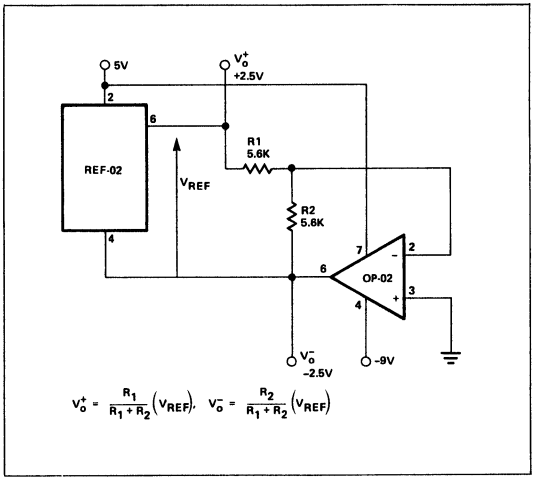


TYPICAL APLICATIONS

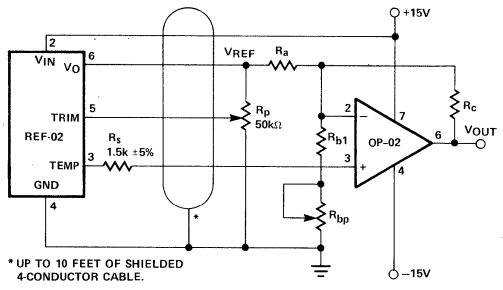
±5V REFERENCE



±2.5V REFERENCE



PRECISION TEMPERATURE TRANSDUCER WITH REMOTE SENSOR



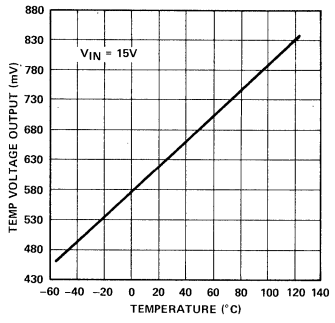
FOR THEORY OF OPERATION AND CALIBRATION PROCEDURE CONSULT APPLICATION NOTE 18, "THERMOMETER APPLICATIONS OF THE REF-02".

RESISTOR VALUES

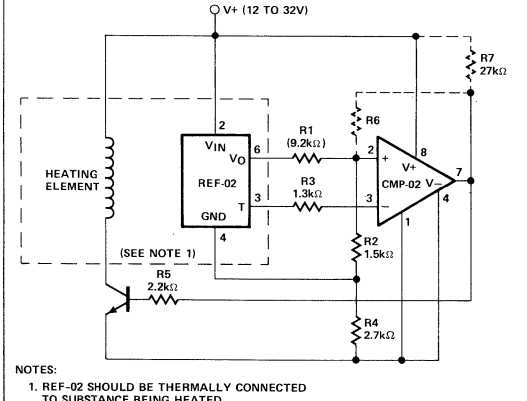
TCV_{OUT} SLOPE (S)	10mV/°C	100mV/°C	10mV/°F
TEMPERATURE RANGE	−55°C to +125°C	−55°C to +125°C	−67°F to +257°C
OUTPUT VOLTAGE RANGE	−0.55V to +1.25V	−5.5V to +12.5V*	−0.67V to +2.57V
ZERO SCALE	0V@0°C	0V@0°C	0V@0°F
R_a (±1% resistor)	9.09kΩ	15kΩ	7.5kΩ
R_{b1} (±1% resistor)	1.5kΩ	1.82kΩ	1.21kΩ
R_{bp} (Potentiometer)	200Ω	500Ω	200Ω
R_c (±1% resistor)	5.11kΩ	84.5kΩ	8.25kΩ

* For 125°C operation, the op amp output must be able to swing to +12.5V, increase V_{IN} to +18V from +15V if this is a problem.

TYPICAL TEMPERATURE VOLTAGE OUTPUT vs TEMPERATURE (REF-02A)



TEMPERATURE CONTROLLER

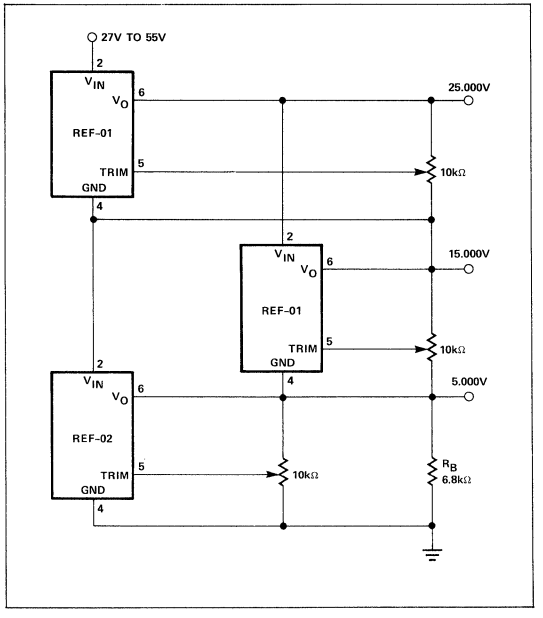


NOTES:
1. REF-02 SHOULD BE THERMALLY CONNECTED TO SUBSTANCE BEING HEATED.
2. NUMBERS IN PARENTHESES ARE FOR A SETPOINT TEMPERATURE OF 60°C.
3. R3 = R1||R2||R6

REFERENCE STACK WITH EXCELLENT LINE REGULATION

Two REF-01's and one REF-02 can be stacked to yield 5.000, 15.000 and 25.000V outputs. An additional advantage is near-perfect line regulation of the 5.000 and 15.000 output voltages. A 27V to 55V input change produces an output change which is less than the noise voltage of the devices. A load bypass resistor (R_B) provides a path for the supply current (I_{SY}) of the 15.000V regulator.

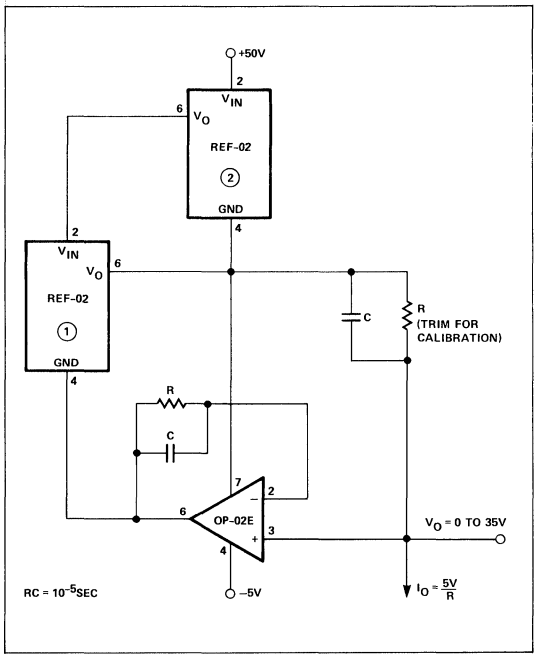
In general any number of REF-01's and REF-02's can be stacked this way. For example, ten devices will yield ten outputs in 5 or 10V steps. The line voltage can range from 100 to 130V. However, care must be taken to ensure that the total load currents do not exceed the maximum usable current (typically 21mA).



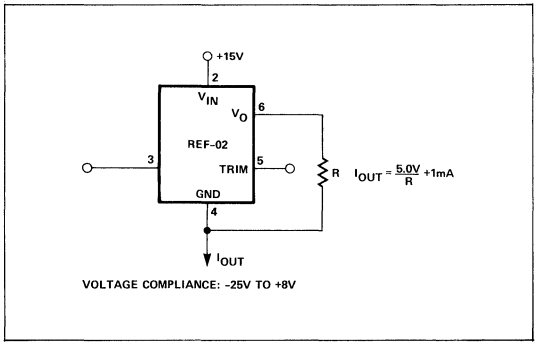
PRECISION CURRENT SOURCE

A current source with 35V output compliance and excellent output impedance can be obtained using this circuit. REF-02 (2) keeps the line voltage and power dissipation constant in device (1) ; the only important error consideration at room temperature is the negative supply rejection of the op amp. The typical 3μV/V PSRR of the OP-02E will create a 20ppm change (3μV/V x 35V/5V) in output current over a 35V range; for example, a 5mA current source can be built (R = 1kΩ) with 350MΩ output impedance.

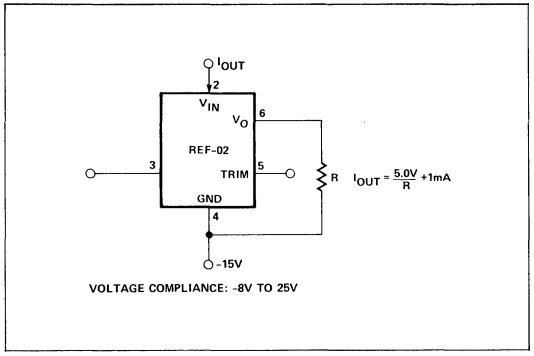
$$R_O = \frac{35V}{20 \times 10^{-6} \times 5mA}$$



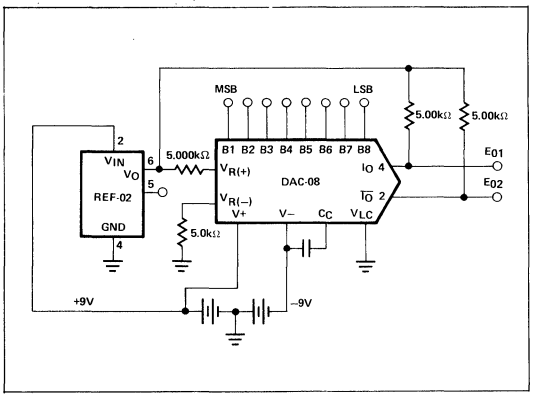
CURRENT SOURCE



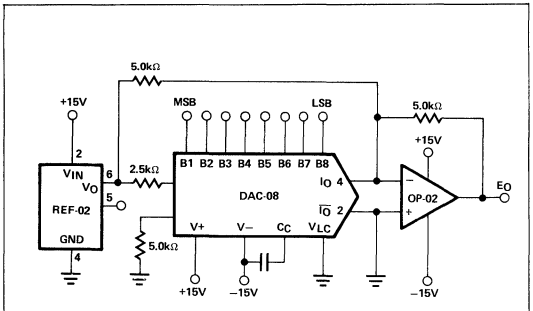
CURRENT SINK



BATTERY OPERATED D/A CONVERTER REFERENCE

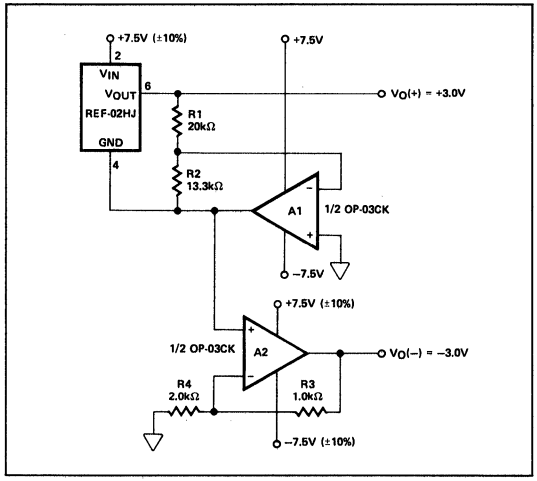


D/A CONVERTER REFERENCE

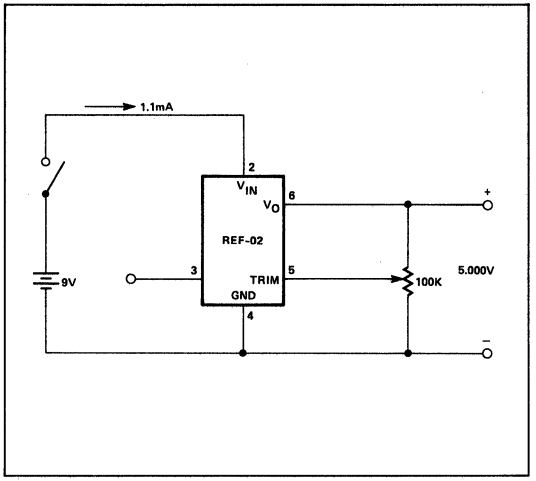


POS FULL SCALE −1 LSB	B1	B2	B3	B4	B5	B6	B7	B8	E
ZERO SCALE	1	1	1	1	1	1	1	1	+4.960
NEG FULL SCALE +1 LSB	1	0	0	0	0	0	0	0	0.000
NEG FULL SCALE	0	0	0	0	0	0	0	1	−4.960
	0	0	0	0	0	0	0	0	−5.000

±3V REFERENCE



PRECISION CALIBRATION STANDARD



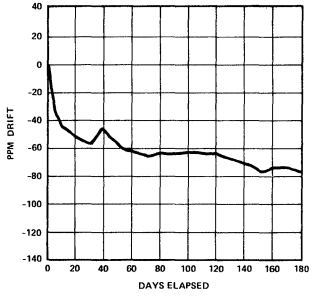
REF-05

+5V PRECISION VOLTAGE REFERENCE WITH GUARANTEED LONG-TERM STABILITY

FEATURES

- 5 Volt Output
- Guaranteed Long-Term Stability ..... 100ppm/1000 Hrs Max
- Excellent Temperature Stability ..... 3ppm/°C
- Low Noise ..... 10μV p-p
- Low Power Drain 15mW
- Wide Input Voltage Range ..... 7V to 40V
- High Load Driving Capability 20mA
- Short Circuit Proof
- Processed Per MIL-STD-883

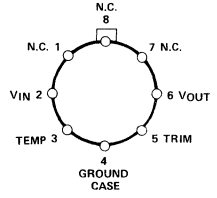
LONG TERM DRIFT PLOT (Average of 20 Devices)



GENERAL DESCRIPTION

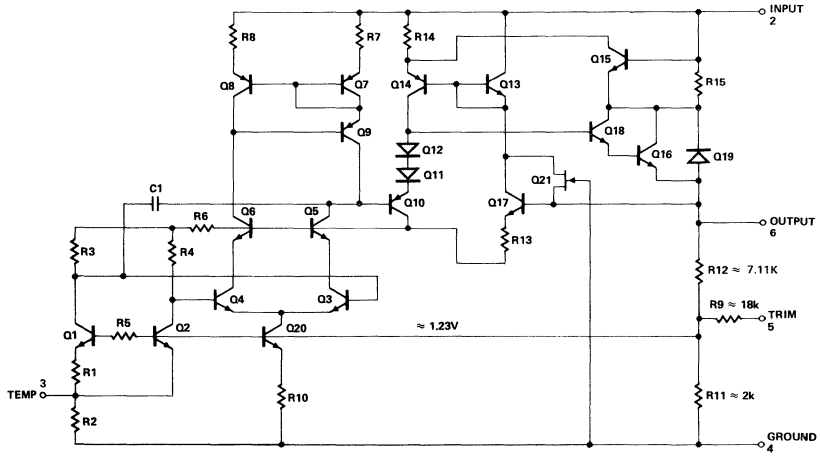
The REF-05 Precision Voltage Reference provides a stable +5V output which can be adjusted over a ±6% range with minimal effect on temperature stability. Single supply operation over an input voltage range of 7V to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise, and low power make the REF-05 an excellent choice whenever a stable voltage reference is required. Applications include D/A and A/D converters, portable instrumentation, and digital voltmeters. The versatility of the REF-05 is enhanced by its use as a monolithic temperature transducer. (See AN-18 "Thermometer Applications of the REF-02.") For +10V Precision Voltage References see the REF-10 data sheet.

PIN CONNECTIONS



TO-99 (J-Suffix)
REF05AJ
REF05BJ

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Input Voltage
REF-05A, B 40V
Power Dissipation (see note) 500mW
Output Short Circuit Duration
(to Ground or V_{IN}) ..... Indefinite

Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Operating Temperature Range
REF-05A, REF-05B ..... −55°C to +125°C

NOTE: Derate at 7.1mW/°C above 80°C ambient temperature for TO-99 (J) package.

ELECTRICAL CHARACTERISTICS at V_{IN} = +15V, T_A = 25°C unless otherwise noted.

			REF-05A			REF-05B			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage	V_O	I_L = 0mA	4.985	5.000	5.015	4.975	5.000	5.025	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±3.0	±6.0	—	±3.0	±6.0	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 1)	—	10	15	—	10	15	μV_{p-p}
Long Term Stability		(Note 1)	—	65	100	—	65	100	ppm/1kHrs
Input Voltage Range	V_{IN}		7	—	40	7	—	40	V
Line Regulation (Note 2)		V_{IN} = 8 to 33V	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 2)		I_L = 0 to 10mA	—	0.005	0.010	—	0.006	0.010	%/mA
Turn-on Settling Time	t_{on}	To ±0.1% of final value	—	5.0	—	—	5.0	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S		−0.3	−0.5	—	−0.3	−0.5	—	mA
Short Circuit Current	I_{SC}	V_O = 0	—	30	—	—	30	—	mA
Temperature Voltage Output	V_T	(Note 3)	—	630	—	—	630	—	mV

ELECTRICAL CHARACTERISTICS at V_{IN} = +15V, −55°C ≤ T_A ≤ +125°C and I_L = 0mA unless otherwise noted.

			REF-05A			REF-05B			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage Change with Temperature (Notes 4 and 5)	ΔV_{OT}	0°C ≤ T_A ≤ +70°C	—	0.02	0.06	—	0.07	0.17	%
	ΔV_{OT}	−55°C ≤ T_A ≤ +125°C	—	0.06	0.15	—	0.18	0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 6)	—	3	8.5	—	10	25	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10kΩ	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (V_{IN} = 8 to 33V) (Note 2)		0°C ≤ T_A ≤ +70°C	—	0.007	0.012	—	0.007	0.012	%/V
		−55°C ≤ T_A ≤ +125°C	—	0.009	0.015	—	0.009	0.015	%/V
Load Regulation (I_L = 0 to 8mA) (Note 2)		0°C ≤ T_A ≤ +70°C	—	0.006	0.010	—	0.007	0.012	%/mA
		−55°C ≤ T_A ≤ +125°C	—	0.007	0.012	—	0.009	0.015	%/mA
Temperature Voltage Output Temperature Coefficient	TCV_T	(Note 3)	—	2.1	—	—	2.1	—	mV/°C

NOTES:

1. Sample tested.
2. Line and Load Regulation specifications include the effect of self heating.
3. Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
4. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V.

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{5V} \times 100$$

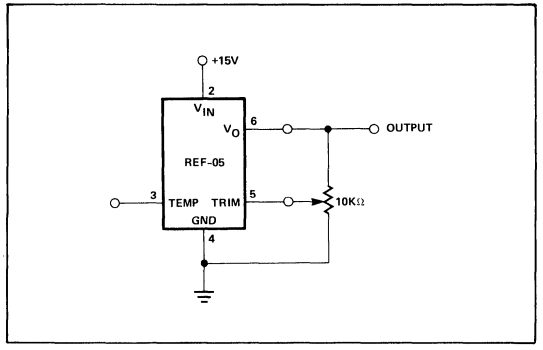
5. ΔV_{OT} specification applied trimmed to +5.000V or untrimmed.
6. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O = \frac{\Delta V_{OT}}{180°C}$$

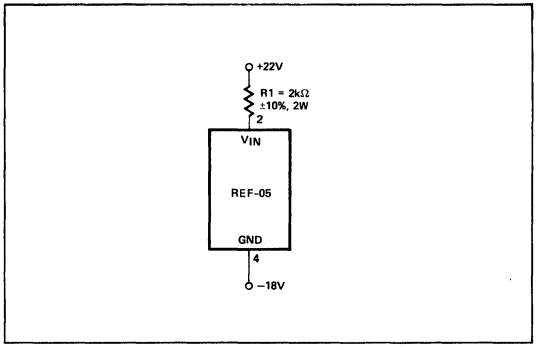
OUTPUT ADJUSTMENT

The REF-05 trim terminal can be used to adjust the output voltage over a 5V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 5V. Of course, the output can also be set to exactly 5.000V or to 5.12V for binary applications.

Adjustment of the output does not significantly affect the temperature performance of the device. Typically the temperature coefficient change is 0.7ppm/°C for 100mV of output adjustment.

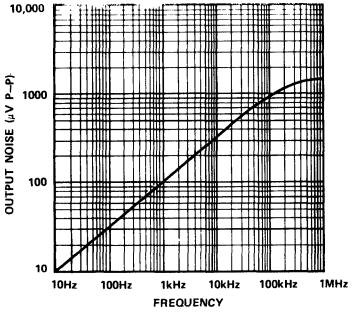


BURN-IN CIRCUIT

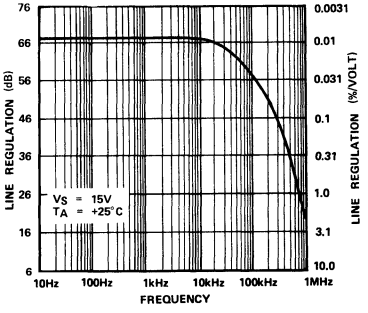


TYPICAL PERFORMANCE CURVES

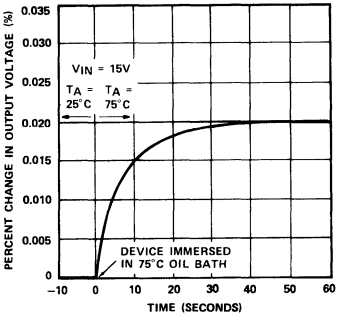
OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



LINE REGULATION vs FREQUENCY

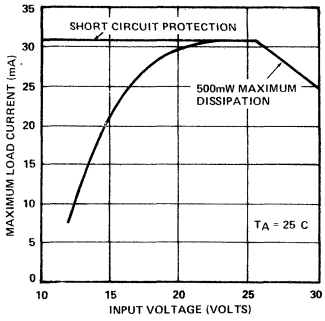


OUTPUT CHANGE DUE TO THERMAL SHOCK

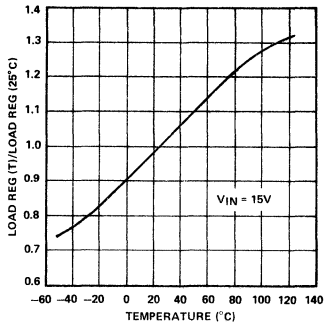


TYPICAL PERFORMANCE CURVES

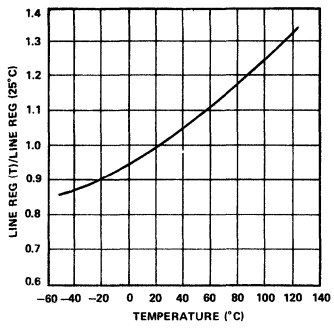
MAXIMUM LOAD CURRENT vs INPUT VOLTAGE



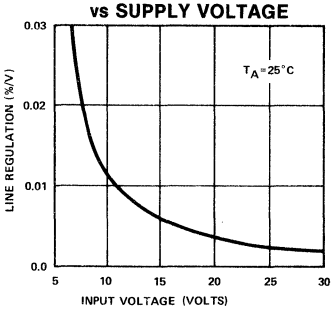
NORMALIZED LOAD REGULATION (ΔI_L = 10mA) vs TEMPERATURE



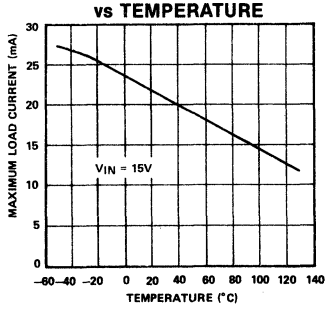
NORMALIZED LINE REGULATION vs TEMPERATURE



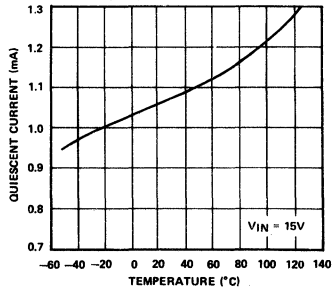
LINE REGULATION vs SUPPLY VOLTAGE



MAXIMUM LOAD CURRENT vs TEMPERATURE

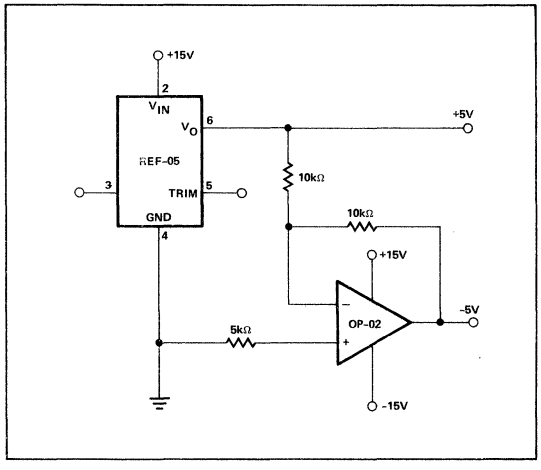


QUIESCENT CURRENT vs TEMPERATURE

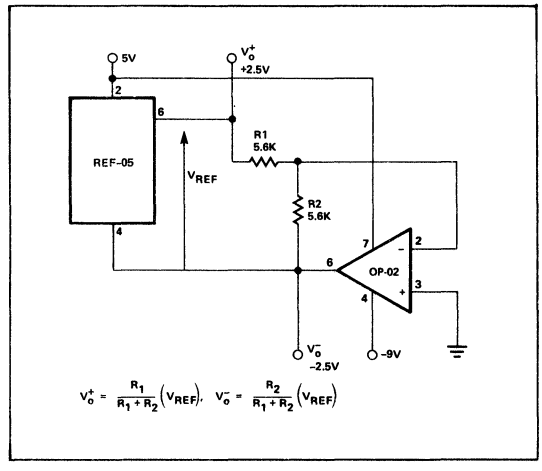


TYPICAL APLICATIONS

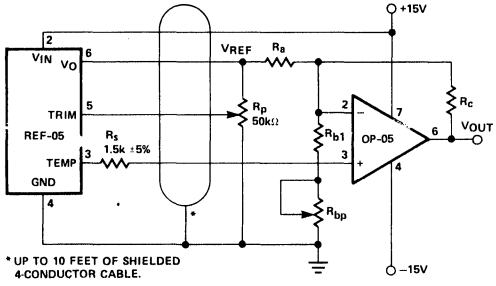
±5V REFERENCE



±2.5V REFERENCE



PRECISION TEMPERATURE TRANSDUCER WITH REMOTE SENSOR



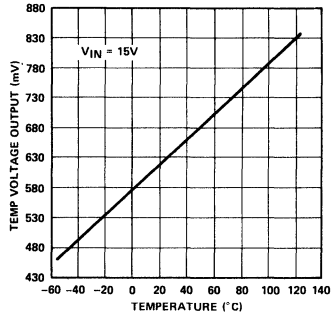
FOR THEORY OF OPERATION AND CALIBRATION PROCEDURE CONSULT APPLICATION NOTE 18, "THERMOMETER APPLICATIONS OF THE REF-02".

RESISTOR VALUES

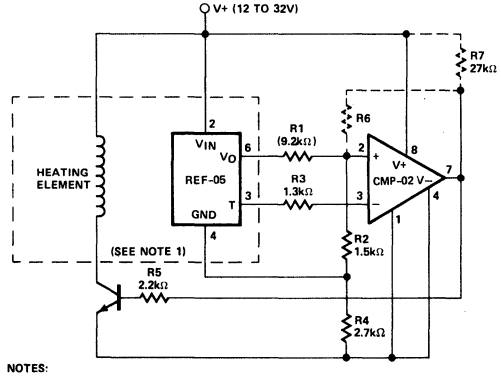
TCV_{OUT} SLOPE (S)	10mV/°C	100mV/°C	10mV/°F
TEMPERATURE RANGE	−55°C to +125°C	−55°C to +125°C	−67°F to +257°C
OUTPUT VOLTAGE RANGE	−0.55V to +1.25V	−5.5V to +12.5V	−0.67V to +2.57V
ZERO SCALE	0V@0°C	0V@0°C	0V@0°F
R_a (±1% resistor)	9.09kΩ	15kΩ	7.5kΩ
R_{b1} (±1% resistor)	1.5kΩ	1.82kΩ	1.21kΩ
R_{bp} (Potentiometer)	200Ω	500Ω	200Ω
R_c (±1% resistor)	5.11kΩ	84.5kΩ	8.25kΩ

* For 125°C operation, the op amp output must be able to swing to +12.5V, increase V_{IN} to +18V from +15V if this is a problem.

TYPICAL TEMPERATURE VOLTAGE OUTPUT vs TEMPERATURE (REF-05A)



TEMPERATURE CONTROLLER

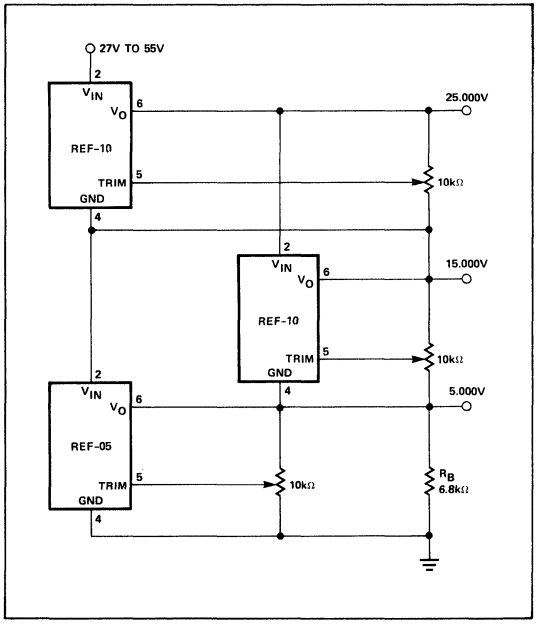


NOTES:
1. ▯ SHOULD BE THERMALLY CONNECTED TO SUBSTANCE BEING HEATED.
2. NUMBERS IN PARENTHESES ARE FOR A SETPOINT TEMPERATURE OF 60°C.
3. R3 = R1‖R2‖R6

REFERENCE STACK WITH EXCELLENT LINE REGULATION

Two Ref-10's and one REF-05 can be stacked to yield 5.000, 15.000 and 25.000V outputs. An additional advantage is near-perfect line regulation of the 5.000 and 15.000 output voltages. A 27V to 55V input change produces an output change which is less than the noise voltage of the devices. A load bypass resistor (R_g) provides a path for the supply current (I_{SY}) of the 15.000V regulator.

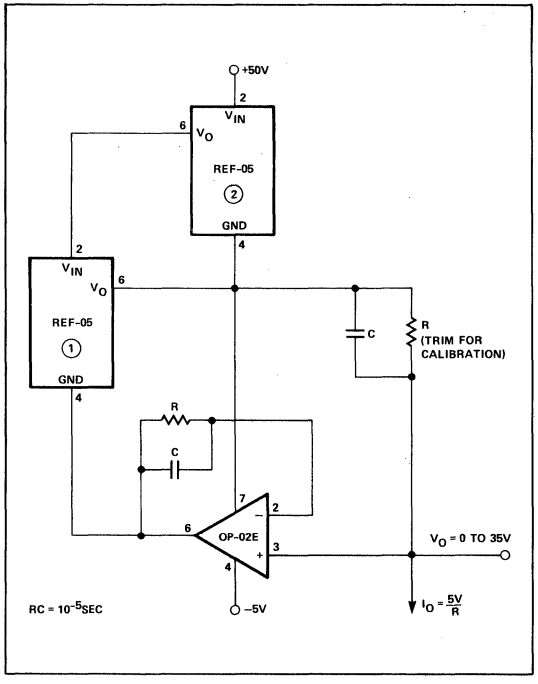
In general any number of REF-10's and REF-05's can be stacked this way. For example, ten devices will yield ten outputs in 5 or 10V steps. The line voltage can range from 100 to 130V. However, care must be taken to ensure that the total load currents do not exceed the maximum usable current (typically 21mA).



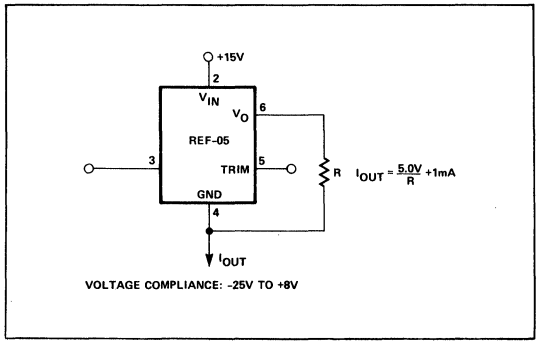
PRECISION CURRENT SOURCE

A current source with 35V output compliance and excellent output impedance can be obtained using this circuit. REF-05 2 keeps the line voltage and power dissipation constant in device 1 ; the only important error consideration at room temperature is the negative supply rejection of the op amp. The typical 3μV/V PSRR of the OP-02E will create a 20ppm change (3μV/V × 35V/5V) in output current over a 35v range. For example, a 5mA current source can be built (R = 1kΩ) with 350MΩ output impedance.

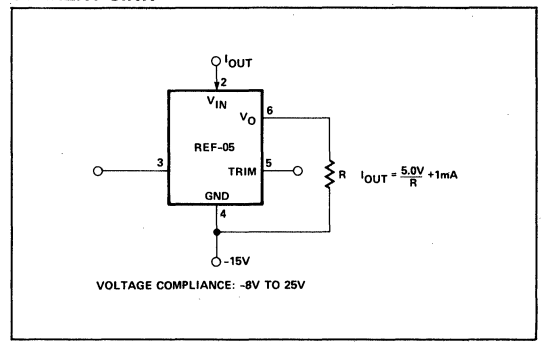
$$R_O = \frac{35V}{20 \times 10^{-6} \times 5mA}$$



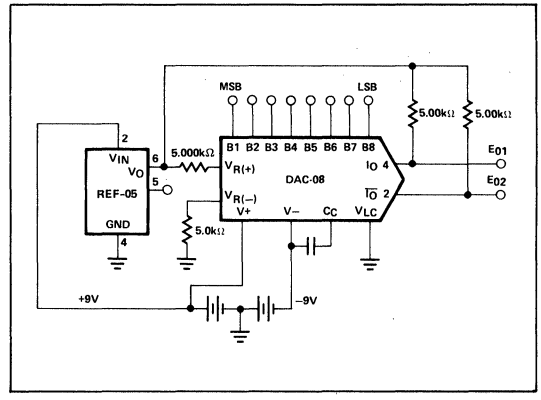
CURRENT SOURCE



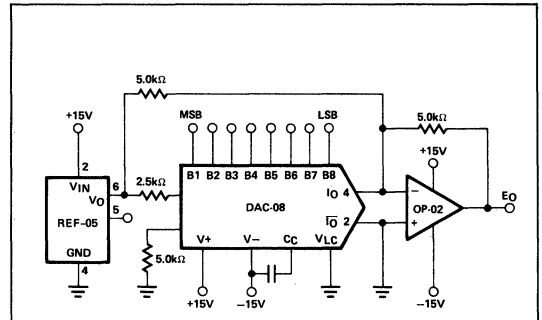
CURRENT SINK



BATTERY-OPERATED D/A CONVERTER REFERENCE

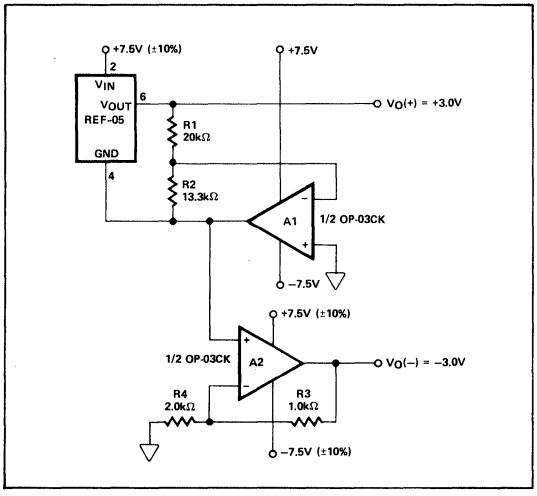


D/A CONVERTER REFERENCE

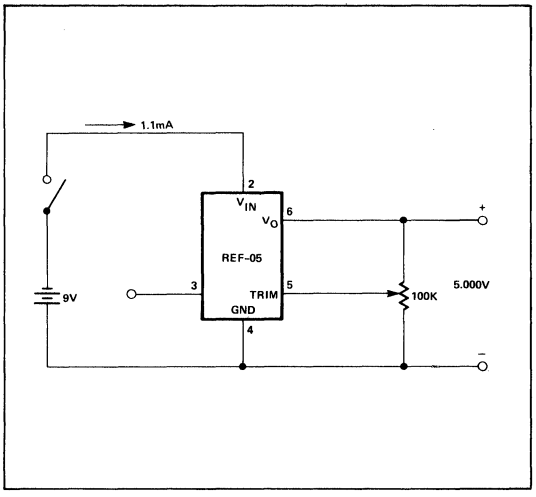


POS FULL SCALE −1 LSB	B1	B2	B3	B4	B5	B6	B7	B8	E
ZERO SCALE	1	1	1	1	1	1	1	1	+4.960
NEG FULL SCALE +1 LSB	1	0	0	0	0	0	0	0	0.000
NEG FULL SCALE	0	0	0	0	0	0	0	1	−4.960
	0	0	0	0	0	0	0	0	−5.000

±3V REFERENCE



PRECISION CALIBRATION STANDARD



REF-10

+10V PRECISION VOLTAGE REFERENCE WITH GUARANTEED LONG TERM STABILITY

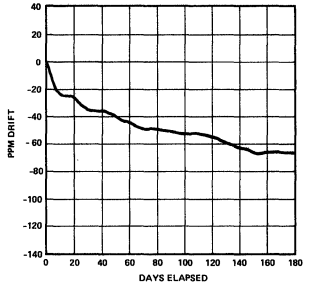
FEATURES

- **10 Volt Output**
- **Guaranteed Long-Term Stability ..... 50ppm/1000 Hrs Max**
- **Excellent Temperature Stability ..... 3ppm/°C**
- **Low Noise ..... 20μV p-p**
- **Low Power Drain 15mW**
- **Wide Input Voltage Range ..... 12V to 40V**
- **High Load Driving Capability 20mA**
- **Short Circuit Proof**
- **Processed Per MIL-STD-883**

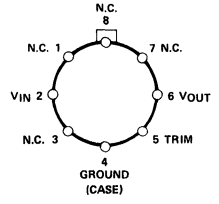
GENERAL DESCRIPTION

The REF-10 Precision Voltage Reference provides a stable +10V output which can be adjusted over a ±3% range with minimal effect on temperature stability. Single supply operation over an input voltage range of 12V to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise, and low power make the REF-10 an excellent choice whenever a stable voltage reference is required. Applications include D/A and A/D converters, portable instrumentation, and digital voltmeters. For +5V Precision Voltage References see the REF-05 data sheet.

LONG TERM DRIFT PLOT (Average of 20 Devices)

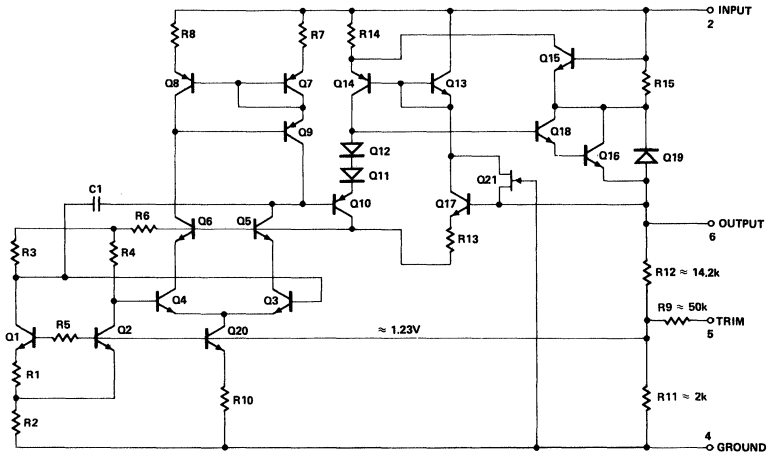


PIN CONNECTIONS



TO-99 (J-Suffix)
REF10AJ
REF10BJ

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Input Voltage
REF-10A, B 40V
Power Dissipation (see note) 500mW
Output Short Circuit Duration
(to Ground or V_{IN}) ..... Indefinite

Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Operating Temperature Range
REF-10A, REF-10B ..... −55°C to +125°C

NOTE: Derate at 7.1mW/°C above 80°C ambient temperature for TO-99 (J) package.

ELECTRICAL CHARACTERISTICS at V_{IN} = +15V, T_A = 25°C, unless otherwise noted.

			REF-10A			REF-10B			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage	V_O	I_L = 0mA	9.97	10.00	10.03	9.95	10.00	10.05	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±3.0	±3.3	—	±3.0	±3.3	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 5)	—	20	30	—	20	30	μVp-p
Long Term Stability		(Note 5)	—	—	50	—	—	50	ppm/1000 Hrs
Input Voltage Range	V_{IN}		12	—	40	12	—	40	V
Line Regulation (Note 4)		V_{IN} = 13 to 33V	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 4)		I_L = 0 to 10mA	—	0.005	0.008	—	0.006	0.010	%/mA
Turn-on Settling Time	t_{on}	To ±0.1% of final value	—	5.0	—	—	5.0	—	μsec.
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S		−0.3	−0.5	—	−0.3	−0.5	—	mA
Short Circuit Current	I_{SC}	V_O = 0	—	30	—	—	30	—	mA

ELECTRICAL CHARACTERISTICS at V_{IN} = +15V, −55°C ≤ T_A ≤ +125°C and I_L = 0mA, unless otherwise noted.

			REF-10A			REF-10B			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage Change with Temperature (Notes 1 and 2)	ΔV_{OT}	0° ≤ T_A ≤ +70°C −55° ≤ T_A ≤ +125°C	— —	0.02 0.06	0.06 0.15	— —	0.07 0.18	0.17 0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	—	3.0	8.5	—	10.0	25.0	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10kΩ	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (V_{IN} = 13 to 33V) (Note 4)		0° ≤ T_A ≤ +70°C −55° ≤ T_A ≤ +125°C	— —	0.007 0.009	0.012 0.015	— —	0.007 0.009	0.012 0.015	%/V
Load Regulation (I_L = 0 to 8mA) (Note 4)		0° ≤ T_A ≤ +70°C −55° ≤ T_A ≤ +125°C	— —	0.006 0.007	0.010 0.012	— —	0.007 0.009	0.012 0.015	%/mA

NOTES:

1. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{10V} \times 100$$

2. ΔV_{OT} specification applies trimmed to +10.000V or untrimmed.
3. TCV_O is defined as ΔV_{OT} divided by the temperature range; i.e.,

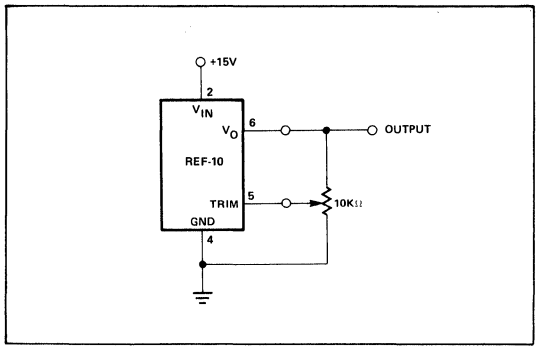
$$TCV_O\,(-55° \text{ to } +125°C) = \frac{\Delta V_{OT}\,(-55 \text{ to } +125°C)}{180°C}$$

4. Line and Load Regulation specifications include the effects of self heating.
5. Sample tested.

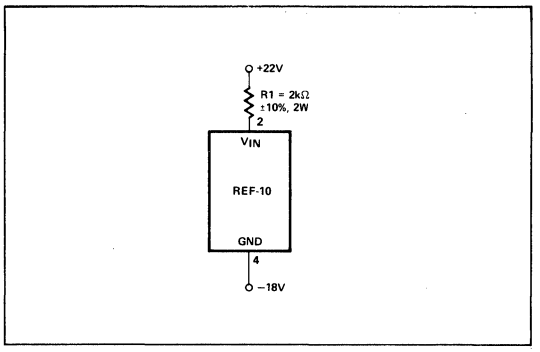
OUTPUT ADJUSTMENT

The REF-10 trim terminal can be used to adjust the output voltage over a 10V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 10V. Of course, the output can also be set to exactly 10.000V or to 10.240V for binary applications.

Adjustment of the output does not significantly affect the temperature performance of the device. Typically the temperature coefficient change is 0.7ppm/°C for 100mV of output adjustment.

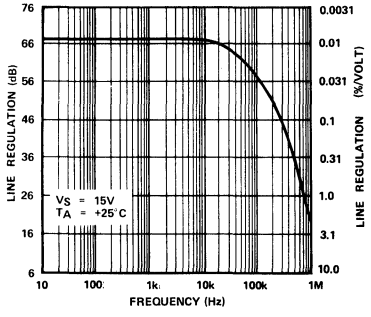


BURN-IN CIRCUIT

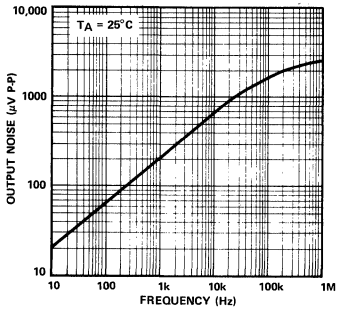


TYPICAL PERFORMANCE CURVES

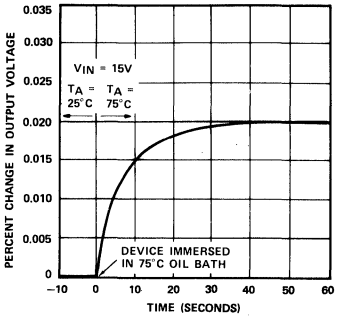
LINE REGULATION vs FREQUENCY



OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)

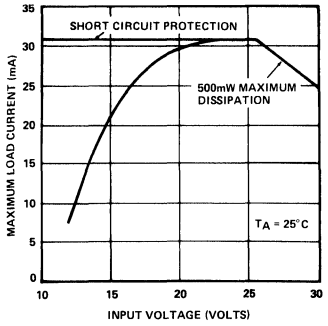


OUTPUT CHANGE DUE TO THERMAL SHOCK

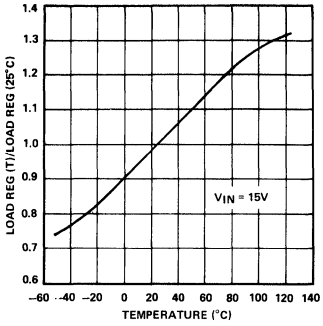


TYPICAL PERFORMANCE CURVES

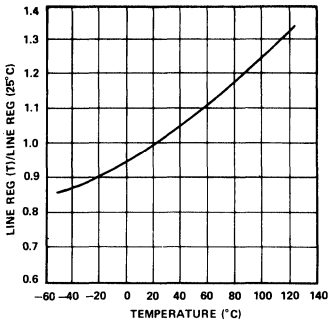
MAXIMUM LOAD CURRENT vs INPUT VOLTAGE



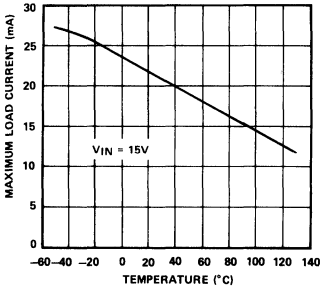
NORMALIZED LOAD REGULATION (ΔI_L = 10mA) vs TEMPERATURE



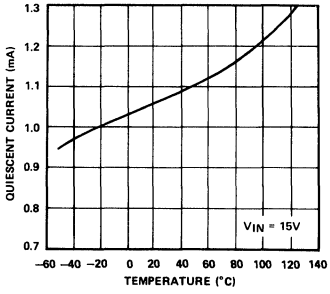
NORMALIZED LINE REGULATION vs TEMPERATURE



MAXIMUM LOAD CURRENT vs TEMPERATURE

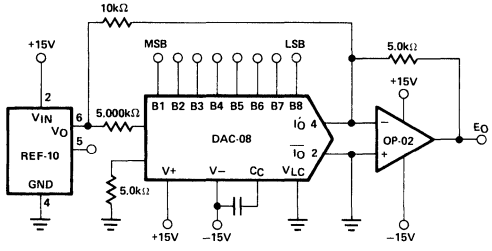


QUIESCENT CURRENT vs TEMPERATURE



TYPICAL APPLICATIONS

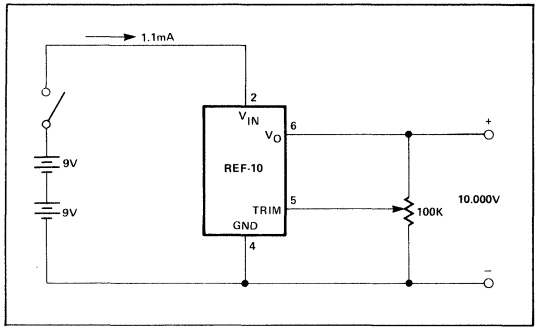
D/A CONVERTER REFERENCE



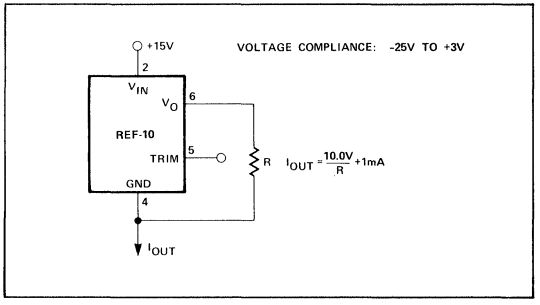
	B1	B2	B3	B4	B5	B6	B7	B8	E
POS FULL SCALE −1 LSB	1	1	1	1	1	1	1	1	+4.960
ZERO SCALE	1	0	0	0	0	0	0	0	0.000
NEG FULL SCALE +1 LSB	0	0	0	0	0	0	0	1	−4.960
NEG FULL SCALE	0	0	0	0	0	0	0	0	−5.000

TYPICAL APPLICATIONS

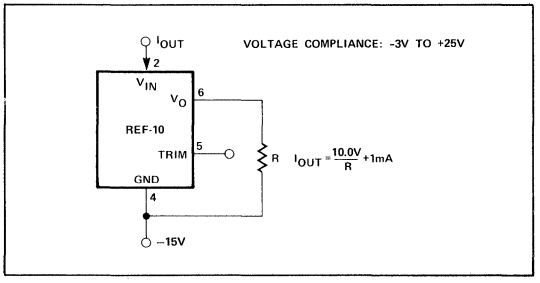
PRECISION CALIBRATION STANDARD



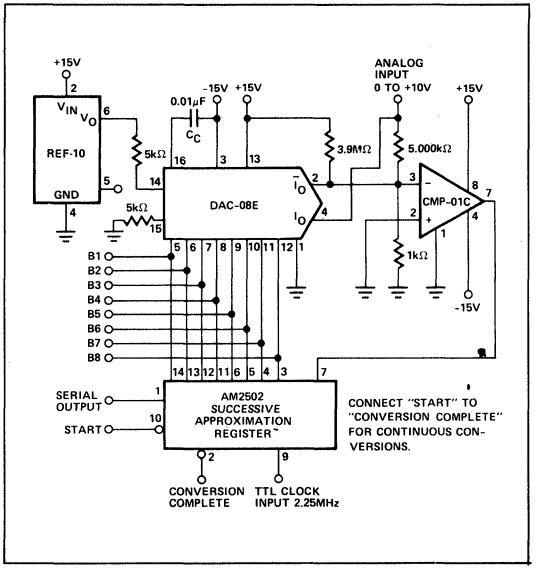
CURRENT SOURCE



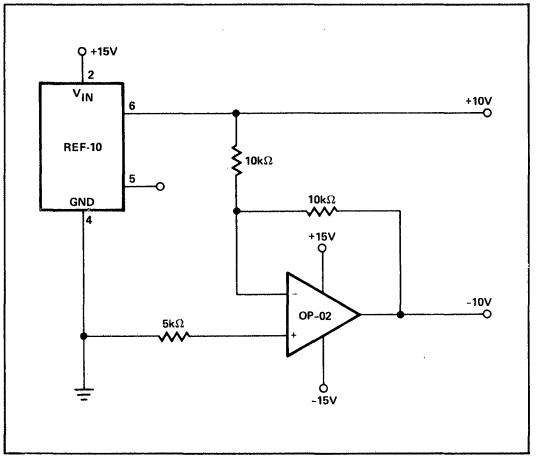
CURRENT SINK



A/D CONVERTER REFERENCE



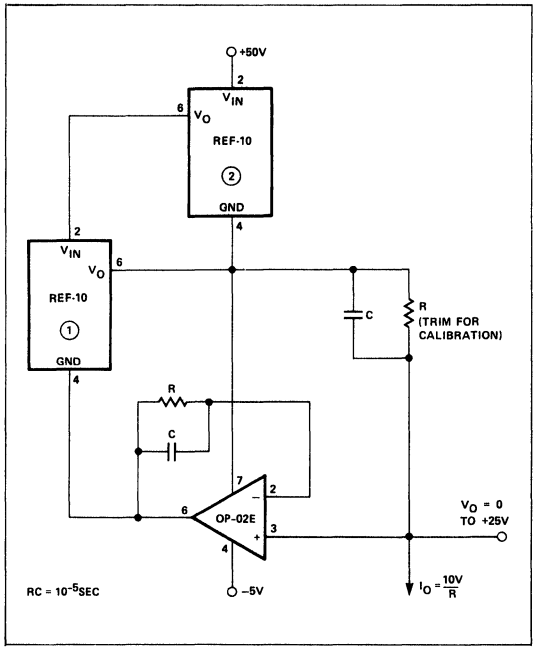
±10V REFERENCE



PRECISION CURRENT SOURCE

A current source with 25V output compliance and excellent output impedance can be obtained using this circuit. REF-10 ②keeps the line voltage and power dissipation constant in device ①; the only important error consideration at room temperature is the negative supply rejection of the op amp. The typical 3μV/V PSRR of the OP-02E will create an 8ppm change (3μV/V × 25V/10V) in output current over a 25V range. For Example, a 10mA current source can be built (R = 1kΩ) with 300MΩ output impedance.

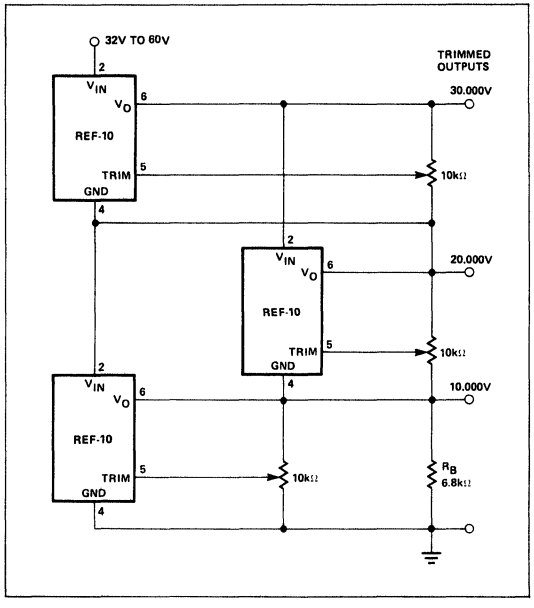
$$R_O = \frac{25V}{8x10^{-6}x10mA}$$



REFERENCE STACK WITH EXCELLENT LINE REGULATION

Three REF-10's can be stacked to yield 10.000, 20.000 and 30.000V outputs. An additional advantage is near-perfect line regulation of the 10.000 and 20.000 output voltages. A 32V to 60V input change produces an output change which is less than the noise voltage of the devices. A load bypass resistor (R_B) provides a path for the supply current (I_{SY}) of the 20.000V regulator.

In general, any number of REF-10's can be stacked this way. For example, ten devices will yield outputs of 10, 20, 30 . .. 100V. The line voltage can range from 105V to 130V. However, care must be taken to ensure that the total load currents do not exceed the maximum usable current (typically 21mA).



SECTION 10

D/A CONVERTERS

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INTRODUCTION

A D/A converter accepts a digital input and produces an analog output. The basic DAC consists of a voltage or current reference, binary weighted precision resistors, a set of electronic switches and a means of summing the weighted currents.

Three important criteria for selecting a good DAC are accuracy, speed and resolution. Other essential requirements to be considered are temperature stability, input coding, output format, reference requirements and power consumption.

PMI DACs use bipolar transistor technology. Some of the advantages these DACs offer over CMOS-FET types are:

1. Bipolar technology allows a stable internal zener reference to be fabricated monolithically. Adequate references are not available in CMOS devices.
2. Reference servoed NPN current source transistors give high compliance, temperature stable outputs.
3. Stable low-offset op amps are also difficult to fabricate with CMOS devices.
4. The bipolar transistor switches provided on PMI DACs have faster settling times than their FET counterparts.

DACs can be categorized by the type of analog output — a current or a voltage. "Complete" DACs have an on-board reference source, R-2R ladder network and current-to-voltage converting op amp on one monolithic IC. "Multiplying" DACs have access to the reference input pin allowing the user to multiply an analog quantity by a digital number.

Since introducing the first monolithic D/A converter in 1970, PMI has continually improved and updated its DAC series. PMI offers an extensive choice of DAC resolutions, coding formats, output configurations and temperature ranges. All of these products are characterized by high speed and temperature stable performance. Wide dynamic range and good zero resolution are offered by PMI's "companding" (compressing/expanding) D/A converter, the COMDAC® , in applications where a high-resolution linear DAC is not needed.

The selection guides following the definition pages will aid you in quickly locating the appropriate DAC.

COMPANDING DAC DEFINITIONS

CHORDS
Groups of linearly-related steps in the transfer function. Also known as segments.

CHORD ENDPOINTS
The maximum code in each chord. Used to specify accuracy.

DYNAMIC RANGE
Ratio of the largest output ($I_{7,15}$) to the smallest output excluding zero ($I_{0,0}$) expressed in dB. This can be measured peak or peak-to-peak with the same result.

ENCODE CURRENT
The difference between $I_{OE}(+)$ and $I_{OD}(+)$ or the difference between $I_{OE}(-)$ and $I_{OD}(-)$ at any code.

FULL SCALE SYMMETRY ERROR
The difference between $I_{OD}(-)$ and I $(+)$ or the difference between $I_{OE}(+)$ and $I_{OE}(-)$ at full-scale output.

OUTPUT LEVEL NOTATION
Each output current level may be designated by the code $I_{C,S}$ where C = chord number and S = step number. For example, $I_{0,0}$ = zero scale current; $I_{0,1}$ = first step from zero; $I_{0,15}$ = endpoint of first chord (C_0); $I_{7,15}$ = full scale current.

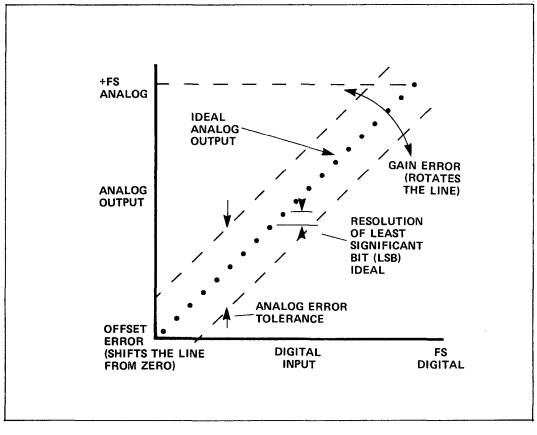
STEPS
Increments in each chord which divide it into 16 equal levels.

STEP NONLINEARITY
Step size deviation from ideal within a chord.

LINEAR DIGITAL-TO-ANALOG CONVERTER TERMS AND DEFINITIONS

D/A Converters accept a digital input code and convert this input into an equivalent analog voltage or current output. PMI's D/A Converters utilize the current-switched ladder network design principle which provides fast settling and reduced switching transients. D/A Converters are classified according to the type of analog output, the input code and multiplying capability.

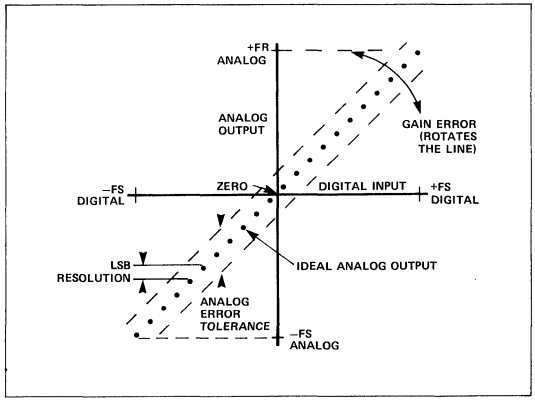
UNIPOLAR D/A CONVERTERS



DISCUSSION OF ERRORS

Transfer accuracy in a D/A Converter is generally determined by measuring deviation of the actual analog output from the ideal expected output. In general, the adjustable analog output errors of a D/A Converter are full-scale or gain error and offset or zero-scale error. Nonadjustable D/A Converter errors include nonlinearity, differential nonlinearity, zero-scale symmetry, zero and full-scale temperature drift coefficients and power-supply sensitivity. The most meaningful nonadjustable error term in a D/A Converter is NONLINEARITY. The next most important nonadjustable error terms are full-scale drift and differential-nonlinearity. A D/A Converter that has a specified maximum nonlinearity of ± 1/2 LSB over temperature will also be guaranteed to be monotonic. PMI specifies maximum nonlinearity over temperature for every D/A converter (except the DAC-03 and DAC-101) to assure the designer of precision performance for the most demanding applications.

BIPOLAR D/A CONVERTERS



DIGITAL-TO-ANALOG CONVERTER
A circuit for converting a digital code word into discrete analog quantities according to a prescribed relationship.

FULL SCALE
Essentially a digitally controlled attenuator, a DAC can only provide fractional multiples of the analog input. The maximum analog output is $\frac{2^n - 1}{2^n}$ times the "scaled" (a possible gain factor) analog input. An output that equals the "scaled" analog input would be considered Full-Scale. Note that a D/A converter can only achieve a full-range output that is less than Full-Scale (by an LSB).

Offsetting the DAC output with a value equal to minus one-half of full-scale will give an analog output range that goes from an offset zero scale which is renamed "negative Full-Scale" to a positive full-range output that is 1 LSB less than "positive Full-Scale". Sign magnitude DAC's have symmetrical output ranges that are one LSB less than Full-Scale. For both positive and negative outputs.

FULL OUTPUT RANGE (FR)
The output analog signal span expressed in units of voltage or current.

BIT

A binary unit (0 or 1) that provides the weighting for each power of 2 in a digital word. For an n-Bit DAC, the Mose Significant Bit (MSB) gives an output equal to 2^{-1} (FS) and the Least Significant Bit (LSB) gives an output equal to 2^{-n} (FS).

DIGIT

A numeric unit in a decimal system that identifies the weight of each power of ten in a digital word. A digit can have any value from 0 to 9. For an n-Digit DAC, the Most Significant Digit (MSD) gives an output equal to (0 to 9) (10^{-1}) and the Least Significant Digit (LSD) gives an output equal to (0 to 9) (10^{-n}). A digit in a Binary-Coded-Decimal (BCD) DAC is represented by four bit binary word that can take on values from 0000 to 1001 (0 to 9).

LEAST SIGNIFICANT BIT (LSB)

The smallest incremental analog output change obtainable and equal to the full scale output range divided by 2^n where n = number of bits.

$$LSB = \frac{FS}{2^n}$$

MOST SIGNIFICANT BIT (MSB)

The largest incremental analog output change obtainable by switching a single logic bit input. It is ideally equal to:

$$MSB = \frac{FS}{2}$$

ZERO SCALE OFFSET ERROR (ZS)

The measured analog output when the digital input code corresponds to an analog value of zero. Usually expressed as a percentage of nominal Full-Scale Range but also expressed in ppm, LSBs, or given in units of current or voltage.

ZERO SCALE SYMMETRY ERROR

For a Sign-Magnitude D/A Converter, zero scale symmetry is the change in the analog output produced by switching the sign bit with a zero code input to the magnitude bits. This quantity is expressed in units of current, voltage, or in fractions of an LSB.

RESOLUTION

The number of states (2^n) that the Full-Scale range may be divided or resolved into, where n = number of bits. Generally this is expressed in number of bits.

NONLINEARITY (NL) (INTEGRAL NON-LINEARITY)

The maximum deviation from an ideal straight line drawn between the end points, expressed as a percent of Full-Scale Range (FSR) or given in terms of LSB value. The end points are zero scale output to full analog output for unipolar operation and minus full scale to positive full output for bipolar operation. Note that the zero scale output may be offset without effecting the nonlinearity specification.

DIFFERENTIAL NONLINEARITY (DNL)

The maximum deviation of the analog output between any two adjacent output states from the ideal value.

Differential nonlinearity error is expressed as percent of full-scale or in terms of LSB value. For example, a differential linearity error specification of ± 1/2 LSB implies that the output step size for adjacent digital input codes is 1 ± 1/2 LSB or 1/2 to 3/2 LSB.

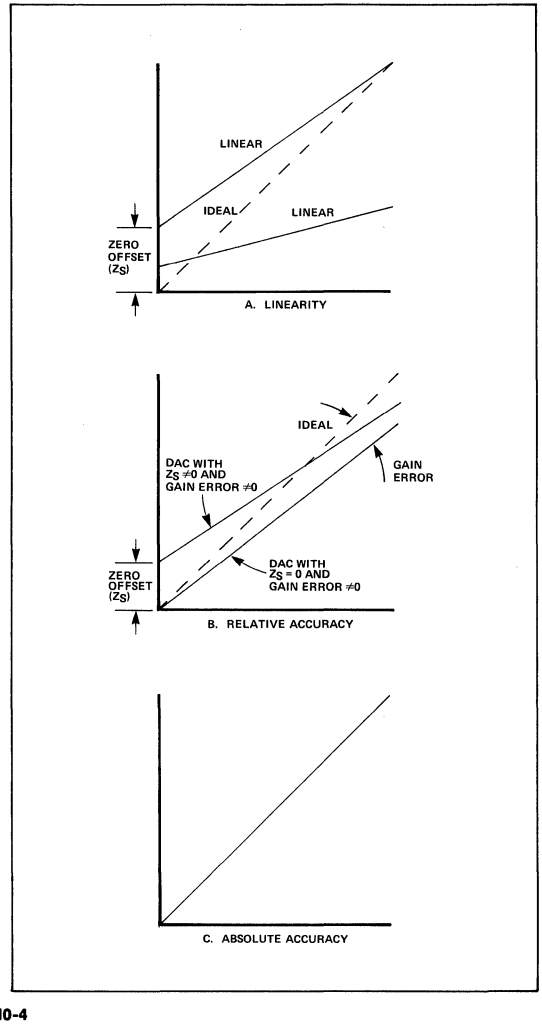
RELATIVE ACCURACY

Relative accuracy defines the deviation in % of full-scale or LSBs, from an ideal straight line drawn between the ideal zero output and the full range output. Thus the relative accuracy specification includes the zero scale offset error as well as non-linearity, and gain error. Relative accuracy defines how well "relative" proportions will be maintained over the full analog output range.

ABSOLUTE ACCURACY

Absolute accuracy defines how closely the output of a DAC approximates the ideal straight line drawn from the ideal zero output to the full-scale output. Absolute accuracy is inclusive of all error terms. The relative accuracy specification will be the absolute accuracy spec *at the moment* of gain error correction. Time, temperature and supply voltage changes will degrade the absolute accuracy specification.

ACCURACY DEFINED



MONOTONICITY

A Digital-to-Analog transfer relationship in which each increment in the digital code is accompanied by an analog output greater than or equal to that of the preceding code. The digital increment for which this definition holds may not be the LSB defined by the DAC resolution but rather the "LSB" defined by the monotonicity specifications.

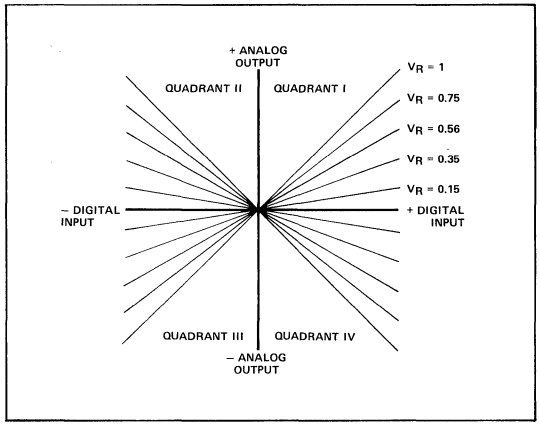
FUNCTIONAL COMPLIANCE

The voltage range over which the current output of a DAC can be moved and for which the DAC will maintain the same relative accuracy (the output can change absolutely).

TRUE COMPLIANCE

The voltage range over which the current output of a DAC can vary while the DAC will maintain an absolute accuracy of ± 1/2 LSB. True compliance requires an extremely high DAC output impedance.

MULTIPLYING DAC TRANSFER CURVES



MULTIPLYING DAC's

The D/A function involves multiplying an analog reference by a digital word ($V_O = V_{REF} \bullet X$). Depending on design, some DAC's can multiply only positive digital words. This is known as single Quadrant (Quadrant 1) operation, Two Quadrant operation, involving Quadrants I and III, is achieved by offsetting a single Quadrant DAC by a negative MSB (1/2 of full-scale) so that a bipolar digital code, in which the MSB becomes the sign bit, can multiply a unipolar reference (positive slope), for example, Quadrants I and III. Full four Quadrant multiplication requires a DAC that can accept a reference of either polarity, and positive and negative values of digital input.

GAIN ERROR

The difference between the actual analog output range and the ideal analog output range expressed as a percent of Full-Scale or in terms of LSB value.

SETTLING TIME

The elapsed time for the analog output to reach its final value within a specified error band after the corresponding digital input code has been changed. Usually specified for a Full-Scale Range change and measured from the 50% point of the logic input change to the time the output reaches final value within the specified error band.

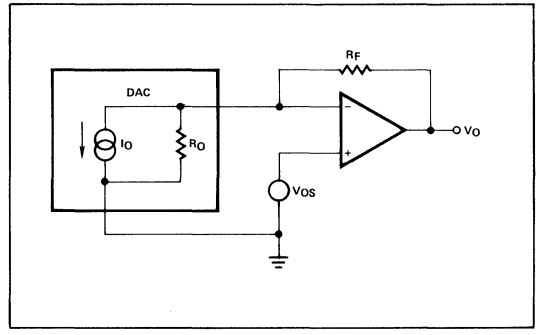
GLITCH

A switching transient appearing in the output during a code transition. Its value is expressed in volts or current and time duration or in charge transferred (in Pico coulombs).

OUTPUT RESISTANCE

The equivalent internal resistance for a current output D/A Converter as seen at its output. It is measured as the change in output current ΔI with the change in output voltage ΔV and, as such, is a direct measure of the true output compliance.

Besides the compliance consideration, low output resistance can lead to V_{OS} drift problems when used with a current-to-voltage converting amplifier. In this case, the DAC output resistance forms a gain setting resistive divider with the feedback resistor which effectively amplifies V_{OS} drift by the factor $\frac{R_F}{R_O} + 1$.



FEED THROUGH

An AC specification on a multiplying DAC which defines the frequency at which a 1/2 LSB (pk-pk) AC signal is seen at the DAC output with all bits in the "OFF" state (zero output code).

POWER SUPPLY SENSITIVITY

The change in the output of the converter due to a change in the power supply value. This may be expressed as a percent of Full-Scale Range per one percent change in the power supply or as a percent of Full Scale per volt of power supply change. Normally this is specified at DC, but is sometimes specified over a given frequency range.

FULL SCALE TEMPERATURE COEFFICIENT OR GAIN DRIFT

This is the change in the Full Analog Range from the 25 °C value and either temperature extreme divided by the corresponding change in temperature and is expressed in ppm/°C.

MISCELLANEOUS TEMPERATURE COEFFICIENTS

Although nonlinearity and differential nonlinearity should be specified as a worst case error over temperature, some manufacturers do specify a drift component on these terms. As in gain drift, they are specified as the change from the 25°C values to either temperature extreme divided by the corresponding change in temperature and expressed in ppm of FSR/°C.

D/A CONVERTERS BY OUTPUT TYPE

CURRENT OUTPUT D/A CONVERTERS

The output of the converter is a true digitally controlled current source or sink which has a high output impedance and a voltage compliance within which the converter meets the specified error limits.

RESISTIVE OUTPUT D/A CONVERTER

The output of the converter is a current, but has a low output resistance (typically 1-20k ohm) and nearly zero output voltage compliance.

VOLTAGE OUTPUT D/A CONVERTER

The output of the converter is a voltage source, and is characterized by low output impedance and a specified load driving capability.

DAC SELECTION GUIDE • Voltage Output • Commercial Temperature Range (0° to 70°C)

Resolution	PMI Part Number	Nonlinearity (% F.S.)		Zero Scale Offset (% F.S.)		Monotonicity (Bits)		Gain T.C. (PPM/°C)		Settling Time (μs)	Output Voltage Range	Power Dissipation (mW)	Codes
		25°C	0° to 70°C	25°C	70°C	25°C	0° to 70°C	Int. Ref.	Ext. Ref				
6-Bit Linear	DAC-01CY	±0.40	±0.45	±0.25 typ.	±0.25 typ.	6	6	±160 max.	—	3.0 max.	±10V to ±11.89V	250	Complement Binary
	DAC-01HY	±0.40	±0.45	±0.40 typ.	±0.40	6	6	±160 max.	—	3.0 max.	±10V to ±11.89V	250	Complement Binary
	DAC-01DY	±0.78	±0.78	±0.50 typ.	±0.50	6	6	±160 max.	—	3.0 max.	±10V to ±11.89V	250	Complement Binary
	DAC-206EY	±0.4	±0.78	±0.25	±0.25	6	6	±120 max.	—	3.0 max.	±5V, +10V or ±10V	270	Complement Binary
	DAC-206FY	±0.80	±1.2	±0.5	±0.5	6	6	±160 max.	—	3.0 max.	±5V, +10V or ±10V	270	Complement Binary
8-Bit +Sign Linear	DAC-208EX	±0.1	±0.1	±0.1	±0.15	8	8	±40 max.	±15 typ.	0.75 typ.	±5V or ±10V	290	Sign Magnitude
	DAC-208FX	±0.2	±0.2	±0.1	±0.1	8	8	±60 max.	±30 typ.	0.75 typ.	±5V or ±10V	290	Sign Magnitude
10-Bit Linear	DAC-02ACX1	±0.10	±0.10	±0.10	±0.10	10	10	±60 max.	±30 typ.	2.0 typ.	±10V to ±11.5V	300	Sign Magnitude
	DAC-02BCX1	±0.10	±0.10	±0.10	±0.10	9	9	±60 max.	±30 typ.	2.0 typ.	±10V to ±11.5V	300	Sign Magnitude
	DAC-02CCX1	±0.20	±0.20	±0.10	±0.10	8	8	±60 max.	±30 typ.	2.0 typ.	±10V to ±11.5V	300	Sign Magnitude
	DAC-02DDX1	±0.40	±0.40	±0.10	±0.10	7	7	±150 max.	±30 typ.	2.0 typ.	±10V	350	Sign Magnitude
	*DAC-03ADX1	±0.10	—	±0.10	—	10	—	±60 typ.	±40 typ.	2.0 typ.	+10V to +11.5V	350	Natural Binary
	*DAC-03BDX1	±0.10	—	±0.10	—	9	—	±60 typ.	±40 typ.	2.0 typ.	+10V to +11.5V	350	Natural Binary
	*DAC-03CDX1	±0.20	—	±0.10	—	8	—	±60 typ.	±40 typ.	2.0 typ.	+10V to +11.5V	350	Natural Binary
	*DAC-03DDX1	±0.4	—	±0.1	—	7	—	±60 typ.	±40 typ.	2.0 typ.	+10V +11.5V	350	Natural Binary

* DAC-03 available all grades with +5V output — use X2 suffix.

DAC SELECTION GUIDE • Voltage Output • Commercial Temperature Range (0° to 70°C)

Resolution	PMI Part Number	Nonlinearity (% F.S.) 25°C	Nonlinearity (% F.S.) 0° to 70°C	Zero Scale Offset (% F.S.) 25°C	Zero Scale Offset (% F.S.) 70°C	Monotonicity (Bits) 25°C	Monotonicity (Bits) 0° to 70°C	Gain T.C. (PPM/°C) Int. Ref.	Gain T.C. (PPM/°C) Ext. Ref	Settling Time (μs)	Output Voltage Range	Power Dissipation (mW)	Codes
10-Bit Linear	DAC-04BCX1	±0.10	±0.10	—	±0.1 typ.	9	9	±60 typ.	±30 typ.	1.5 typ.	±5V typ.	300	Two's Complement
	DAC-04CCX1	±0.20	±0.20	—	±0.1 typ.	8	8	±90 max.	±30 typ.	1.5 typ.	±5V typ.	300	Two's Complement
	DAC-04DDX1	±0.40	±0.40	—	±0.1 typ.	7	7	±150 max.	±50 typ.	2.5 typ.	±5V typ.	350	Two's Complement
	**DAC-05EX	±0.10	±0.20	±0.05	±0.10	10	10	±100	±30 typ.	2.0 typ.	±10V to ±11.5V	300	Sign Magnitude
	**DAC-05FX	±0.20	±0.30	±0.05	±0.10	9	9	±100	±30 typ.	2.0 typ.	±10V to ±11.5V	300	Sign Magnitude
	**DAC-05GX	±0.40	±0.50	±0.05	±0.10	8	8	±100	±30 typ.	2.0 typ.	±10V to ±11.5V	300	Sign Magnitude
	DAC-06EX	±0.10	±0.20	±0.05	±0.10	10	10	±100	±30 typ.	1.5 typ.	±10V to ±11.5V	300	Two's Complement
	DAC-06FX	±0.20	±0.30	±0.05	±0.10	9	9	±100	±30 typ.	1.5 typ.	±10V to ±11.5V	300	Two's Complement
	DAC-06GX	±0.40	±0.40	±0.05	±0.10	8	8	±100	±30 typ.	1.5 typ.	±10V to ±11.5V	300	Two's Complement
	**DAC-210EX	±0.05	±0.05	±0.05	±0.06	10	10	±40 max.	±15 typ.	1.5 typ.	±10V to ±11.5V	290	Sign Magnitude
	**DAC-210FX	±0.05	±0.1	±0.1	±0.1	10	10	±60 max.	±30 typ.	1.5 typ.	±10V to ±11.5V	290	Sign Magnitude
	**DAC-210GX	±0.1	—	—	—	9	9	±30 typ.	±30 typ.	1.5 typ.	±10V to ±11.5V	290	Sign Magnitude

** Sign and magnitude coding (11-Bit).

DAC SELECTION GUIDE • Voltage Output • Military Temperature Range (−55°C to +125°C) THESE PRODUCTS AVAILABLE IN 883B

Resolution	PMI Part Number	Nonlinearity (% F.S.) 25°C	Nonlinearity (% F.S.) −55°C to +125°C	Zero Scale Offset (% F.S.) 25°C	Zero Scale Offset (% F.S.) −55°C to +125°C	Monotonicity (Bits) 25°C	Monotonicity (Bits) −55°C to +125°C	Gain T.C. (PPM/°C) Int. Ref.	Gain T.C. (PPM/°C) Ext. Ref	Settling Time (μs)	Output Voltage Range	Power Dissipation (Pd)	Codes
6-Bit Linear	DAC-01AY	±0.20	±0.30	±0.25	±0.25	6	6	±80		3.0 max.	±10V to ±11.75V	250mW	Complement Binary
	DAC-01Y	±0.40	±0.45	±0.25	±0.25	6	6	±80		3.0 max.	±10V to ±11.75V	250mW	Complement Binary
	DAC-01BY	±0.40	±0.45	±0.25	±0.25	6	6	±120		3.0 max.	±10V to ±11.75V	250mW	Complement Binary
	DAC-01FY	±0.40	±0.45	±0.40	±0.40	6	6	±80		3.0 max.	±10V to ±11.75V	250mW	Complement Binary
	DAC-206AY	±0.40	±0.80	0.25	0.25	6	6	±80		3.0 max.	±10V	270mW	Bipolar
	DAC-206BY	±0.80	±1.2	0.5	0.5	6	6	±160		3.0 max.	±11.75V	270mW	Bipolar
8-Bit Linear	DAC-208AX	±0.1	±0.1		±0.1	8	8	±40	±15 typ.	0.75 max.	±10V	290mW	Sign Magnitude
	DAC-208BX	±0.2	±0.2		±0.15	8	8	±60	±30 typ.	0.75 max.	±11.75V	290mW	Sign Magnitude
10-Bit Linear	DAC-05AX1	±0.10	±0.20	±0.05	±0.10	10	10	±60	±30 typ.	2.0 typ.	±10V to ±11.75V	300mW	Sign Magnitude
	DAC-05BX1	±0.20	±0.30	±0.05	±0.10	9	9	±90	±30 typ.	2.0 typ.	±10V to ±11.75V	300mW	Sign Magnitude
	DAC-05CX1	±0.40	±0.50	±0.05	±0.10	8	8	±120	±30 typ.	2.0 typ.	±10V to ±11.75V	300mW	Sign Magnitude
	DAC-06BX	±0.20	±0.30	±0.05	±0.10	9	9	±90	±30 typ.	1.5 typ.	±10V to ±11.5V	300mW	Two's Complement
	DAC-06CX	±0.40	±0.50	±0.05	±0.10	8	8	±120	±30 typ.	1.5 typ.	±10V to ±11.5V	300mW	Two's Complement
	DAC-210AX	±0.05	±0.075	±0.05	±0.06	10	10	±40	±15 typ.	1.5 typ.	±10V to ±11.5V	325mW	Sign Magnitude
	DAC-210BX	±0.05	±0.10	±0.1	±0.1	10	10	±60	±30 typ.	1.5 typ.	±10V to ±11.5V	325mW	Sign Magnitude

DAC SELECTION GUIDE • Current Output • Commercial Temperature Range (0° to 70°C)

Resolution	PMI Part Number	Nonlinearity (% F.S.) 25°C	Nonlinearity (% F.S.) 0° to 70°C	Zero Scale Offset (% F.S.) 25°C	Zero Scale Offset (% F.S.) 0°C 70°C	Monotonicity (Bits) 25°C	Monotonicity (Bits) 0° to 70°C	Gain T.C. (PPM/°C) Int. Ref.	Gain T.C. (PPM/°C) Ext. Ref	Settling Time (μs)	Output Compliance (Volts)	Power Dissipation (mW)	Output Impedance (MΩ)
8-Bit Linear	DAC-08HQ(HP)	±0.10	±0.10	0.05	0.05	8	8	—	±50 max.	0.135	−10V to +18V	174	>20
	DAC-08EQ(EP)	±0.19	±0.19	0.10	0.10	8	8	—	±50 max.	0.150	−10V to +18V	174	>20
	DAC-08CQ(CP)	±0.39	±0.39	0.20	0.20	8	8	—	±80 max.	0.150	−10V to +18V	174	>20
	DAC-1408A-8Q(7P)	±0.19	±0.19	—	—	8	8	—	±20 typ.	0.250	−5V to +0.5V	265	—
	DAC-1408A-7Q(7P)	±0.39	±0.39	—	—	7	7	—	±20 typ.	0.250	−0.5V to +0.5V	265	—
	DAC-1408A-6Q	±0.78	±0.78	—	—	6	6	—	±20 typ.	0.250	−0.5V to +0.5V	265	—
	DAC-20CQ(CP)	±0.50	±0.50	0.250	0.250	2 Digits	2 Digits	—	±80 max	0.150	−10V to +18V	200	>20
8-Bit Latched	DAC-808EX	±0.1	±0.1	0.1	0.1	9	8	—	±50	0.5	−5V to +8V	170	>20
	DAC-808FX	±0.19	±0.19	0.1	0.1	8	8	—	±80	0.5	−5V to +8V	170	>20
	DAC-808GX	±0.39	±0.39	0.1	0.1	8	8	—	±80	0.5	−5V to +8V	170	>20
	DAC-888EX	±0.1	±0.1	±0.1	±0.1	8	8	—	±50	0.25	−5V to +8V	190	—
	DAC-888FX	±0.19	±0.19	±0.1	±0.1	8	8	—	±80	0.25	−5V to +8V	190	—
10-Bit Linear	DAC-10FX	±0.05	±0.05	0.01	0.01	10	10	—	±25 max.	0.135	−5.5V to +10V	460	—
	DAC-10GX	±0.1	±0.1	±0.01	±0.1	10	10	—	±50 max.	150	−5.5V to +10V	460	—
	DAC-100ACQ3/Q4	±0.05	±0.05	0.013	0.013	10	10	±60	—	0.375	—	300	—
	DAC-100BCQ3/Q4	±0.10	±0.10	0.013	0.013	9	9	±60	—	0.300	—	300	—
	DAC-100CCQ3/Q4	±0.20	±0.20	0.013	0.013	8	8	±60	—	0.225	—	300	—
	DAC-100DDQ3/Q4	±0.30	±0.30	0.013	0.013	8	8	±120	—	0.150	—	300	—
	DAC-101EQ	±0.1	—	0.013	—	10	—	±120	—	0.2	—	—	360
	DAC-101FQ	±0.2	—	0.013	—	9	—	±120	—	0.2	—	—	360
	DAC-101GQ	±0.3	—	0.02	—	8	—	±120	—	0.2	—	—	360
8/12 Companding	DAC-76EX	±½ Step	—	¼ Step	—	128 Steps	—	—	—	0.500 typ.	−5V to +18V	207	—
	DAC-76CX	±1 Step	—	½ Step	—	128 Steps	—	—	—	0.500 typ.	−5V to +18V	207	—
	DAC-76DX	±1½ Step	—	½ Step	—	128 Steps	—	—	—	0.500 typ.	−5V to +18V	207	—
	DAC-312FR	±0.025*	±0.025	±0.003	±0.003	12	12	—	±40	0.25	−5V to +10V	375	>10

*Differential Non-Linearity

DAC SELECTION GUIDE • Current Output • Industrial Temperature Range (25° to +85°C)

Resolution	PMI Part Number	Nonlinearity (% F.S.) 25°C	Nonlinearity (% F.S.) 0° to +85°C	Zero Scale Offset (% F.S.) 25°C	Zero Scale Offset (% F.S.) 70°C +85°C	Monotonicity (Bits) 25°C	Monotonicity (Bits) 0° to +85°C	Gain T.C. (PPM/°C) Int. Ref.	Gain T.C. (PPM/°C) Ext. Ref	Settling Time (μs)	Output Compliance (Volts)	Output Impedance (KΩ)	Power Dissipation (Pd)
10-Bit Linear	DAC-100AAQ7/Q8	±0.05	±0.05	0.013	0.013	10	10	±15	—	0.375	—	500 typ.	250mW
	DAC-100ABQ7/Q8	±0.05	±0.05	0.013	0.013	10	10	±30	—	0.375	—	500 typ.	250mW
	DAC-100ACQ7/Q8	±0.05	±0.05	0.013	0.013	10	10	±60	—	0.375	—	500 typ.	250mW
	DAC-100BBQ7/Q8	±0.10	±0.10	0.013	0.013	9	9	±30	—	0.300	—	500 typ.	250mW
	DAC-100BCQ7/Q8	±0.10	0.10	0.013	0.013	9	9	±60	—	0.300	—	500 typ.	250mW
	DAC-100CCQ7/Q8	±0.20	±0.20	0.013	0.013	8	8	±60	—	0.225	—	500 typ.	250mW
	DAC-100DDQ7/Q8	±0.30	±0.30	0.013	0.013	8	8	±120	—	0.150	—	500 typ.	250mW
8/10-Bit Companding	DAC-78E	—	±1/2 Step		1/8 Step	128 Steps	—	—		0.5	−5V to +18V	262	>10
	DAC-78F		±1 Step	—	1/4 Step	128 Steps	—	—		0.5	−5V to +18V	262	>10
	DAC-78G		±1 1/2 Step	—	1/2 Step	128 Steps	—	—		0.5	−5V to +18V	262	>10

DAC SELECTION GUIDE • Current Output • Military Temperature Range (−55° to +125°C)

Resolution	PMI Part Number	Nonlinearity (% F.S.) 25°C	Nonlinearity (% F.S.) −55°C to +125°C	Zero Scale Offset (% F.S.) 25°C	Zero Scale Offset (% F.S.) −55°C to +125°C	Monotonicity (Bits) 25°C	Monotonicity (Bits) −55°C to +125°C	Gain T.C. (PPM/°C) Int. Ref.	Gain T.C. (PPM/°C) Ext. Ref	Settling Time (μs)	Output Compliance (Volts)	Output Impedance (MΩ)	Power Dissipation (Pd)
8-Bit Linear	DAC-08AQ	±0.10	±0.10	0.05	0.05	8	8	—	±50	0.135	−10V to +18V	>20MΩ typ.	174mW
	DAC-08Q	±0.19	±0.19	0.10	0.10	8	8	—	±80	0.150	−10V to +18V	>20MΩ typ.	174mW
	SSS-1508A-08Q	±0.19	±0.19	0.2	0.2	8	8	—	—	0.250 typ.	−5V to +0.05V	—	265mW
8-Bit Latched	DAC-808AX	—	±0.1	0.1	0.1	8	8	—	±50	0.500	−5V to +8V	>20	170mW
	DAC-808BX	—	±0.19	0.1	0.1	8	8	—	±80	0.500	−5V to +8V	>20	170mW
	DAC-888AX		0.1	0.1	0.1	8	8		±50	0.250	−5V to +8V	>20	190mW
	DAC-888BX		0.19	0.1	0.1	8	8		±80	0.250	−5V to +8V	>20	190mW
10-Bit Linear	DAC-100ACQ5/Q6	±0.05	±0.05	0.013	0.013	10	10	±15	—	0.375	—	500kΩ typ.	300mW
	DAC-100BBQ5/Q6	±0.10	±0.12	0.013	0.013	9	9	±30	—	0.300	—	500kΩ typ.	300mW
	DAC-100BCQ5/Q6	±0.10	±0.10	0.013	0.013	9	9	±30	—	0.300	—	500kΩ typ.	300mW
	DAC-100CCQ5/Q6	±0.20	±0.20	0.013	0.013	8	8	±60	—	0.225	—	500kΩ typ.	300mW
	DAC-10BX	0.05	0.05	0.013	0.013	10	10	±25	—	0.135	−5.5V to +10V	—	460mW
	DAC-10CX	0.1	0.1	0.013	0.013	10	10	±50	—	0.150	−5V to +10V	—	460mW

DAC SELECTION GUIDE • Current Output • Military Temperature Range (−55° to +125°C)

Reso-lution	PMI Part Number	Nonlinearity (% F.S.)		Zero Scale Offset (% F.S.)		Monotonicity (Bits)		Gain T.C. (PPM/°C)		Settling Time (μs)	Output Compli-ance (Volts)	Output Imped-ance (MΩ)	Power Dissipa-tion (Pd)
		25°C	−55°C to +125°C	25°C	−55°C to +125°C	25°C	−55°C to +125°C	Int. Ref.	Ext. Ref				
	DAC-312BR	±0.025	±0.25	±0.003	±0.003	12	12	—	±40	0.25	−10V to +8V	375	>10
	DAC-76BX	½ Step	—	¼ Step	—	128 Steps	—	—	—	0.500 typ.	−5V to +18V	—	192mW
	DAC-76X	1 Step	—	½ Step	—	128 Steps	—	—	—	0.500 typ.	−5V to +18V	—	192mW

DAC-01

6-BIT VOLTAGE OUTPUT D/A CONVERTER

FEATURES

- **Fast** ..... **3μs Settling Time (Maximum)**
- **Complete** ..... **Includes Reference, Ladder, Op Amp**
- **Low Power Consumption** ..... **250mW (Maximum)**
- **6-Bit Resolution** ..... **7-Bit Accuracy**
- **3 Output Options** ..... **+10V, ±5V, ±10V**
- **Standard Power Supplies** ..... **±12V to ±18V**
  −55°/+125°C or 0°/70°C Ranges Available
- **TTL, Compatible Logic Levels**
- **Models with MIL-STD-883 Class B Processing Available From Stock**

GENERAL DESCRIPTION

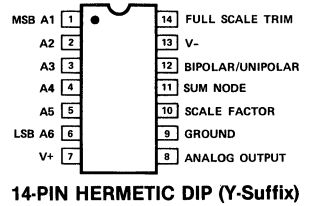
The DAC-01 is a complete monolithic 6-bit digital-to-analog converter, incorporating current steering logic, current sources, diffused resistor ladder network, precision voltage reference and fast summing op amp on one chip. Monolithic construction provides small size, light weight, low power consumption and very high reliability. Wide power supply range, three output voltage options, and three input code options assure flexibility for a wide variety of applications. A seventh bit may also be added for greater resolution. The DAC-01 is ideal for CRT deflection circuits, servo positioning controls, digitally programmed power supplies and pulse generators, modem and telephone system digitizing and demodulation circuits, digital filters, and 6-bit A/D converters. Introduced in 1970, the DAC-01 is still the fastest, lowest power, most accurate 6-bit complete monolithic DAC ever made.

ORDERING INFORMATION††

	14 PIN DIP-HERMETIC	
FULL TEMP. N.L. LSB	**MILITARY TEMP.**	**COMMERCIAL TEMP.**
±1/8	DAC01AY*	——
±1/4	DAC01Y* DAC01BY* DAC01FY*†	DAC01CY DAC01HY†
±1/2	——	DAC01DY

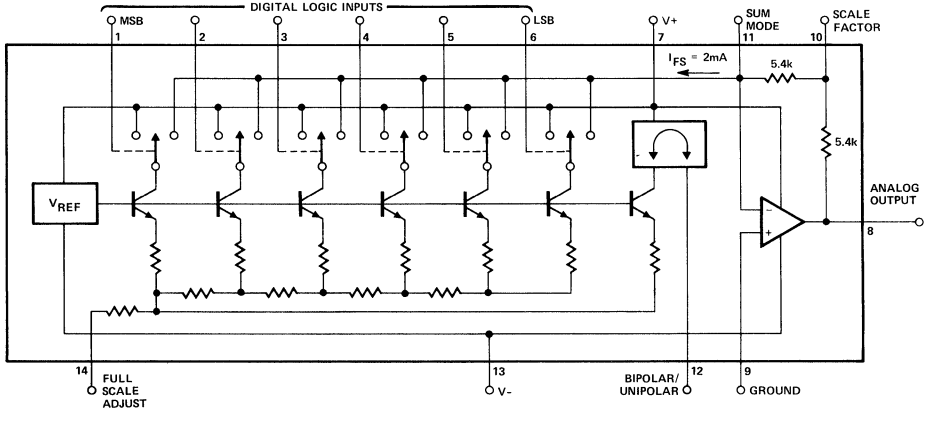
*Available with MIL-STD-883B processing. To order add suffix/883.
†Unipolar only — all others unipolar or bipolar.
††All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



14-PIN HERMETIC DIP (Y-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (See Note 3)

Operating Temperature
- DAC-01A, DAC-01, DAC-01B, DAC-01F ..... −55°C to +125°C
- DAC-01C, DAC-01H, DAC-01D ..... 0°C to +70°C

DICE Junction Temperature (T_j) ..... −65°C to +150°C
V+ Supply Voltage to Ground ..... 0 to +18V
V− Supply Voltage to Ground ..... 0 to −18V
Logic Input to Ground ..... −0.7 to +6V
Internal Power Dissipation (Note 1) 500mW
Storage Temperature ..... −65°C to +150°C
Lead Soldering Temperature (60 sec.) ..... 300°C
Output Short Circuit Duration (Note 2) ..... Indefinite

NOTES:
1. Rating applies to ambient temperatures of 100°C. For temperatures above 100°C, derate linearly at 10mW/°C.
2. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
3. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and over the rated operating temperature range unless otherwise noted.

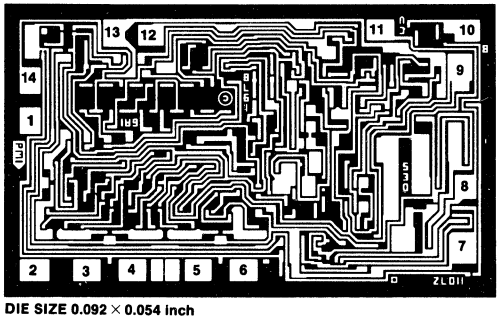
PARAMETER	SYMBOL	DAC-01A	DAC-01	DAC-01B	DAC-01F	DAC-01C	DAC-01H	DAC-01D	UNITS
Output Options		Unipolar Bipolar	Unipolar Bipolar	Unipolar Bipolar	Unipolar	Unipolar Bipolar	Unipolar	Unipolar Bipolar	
Temperature Range	T_A	−55/+125	−55/+125	−55/+125	−55/+125	0/+70	0/+70	0/+70	°C
Nonlinearity 25°C/Maximum	N_L	±0.20	±0.40	±0.40	±0.40	±0.40	±0.40	±0.78	%FS
Nonlinearity Over Temperature — Maximum	N_L	±0.30	±0.45	±0.45	±0.45	±0.45	±0.45	±0.78	%FS
Full Scale Tempco — Maximum	T_C	±80	±80	±120	±80	±160	±160	±160	ppm/°C
Unipolar Zero Scale Output Voltage — Maximum (Note 1, 2)	V_{ZS}	25	25	25	40	25	40	50	mV

ELECTRICAL CHARACTERISTICS for all DAC-01 grades, $V_S = \pm 15V$ and over the rated operating temperature range unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-01 MIN	DAC-01 TYP	DAC-01 MAX	UNITS
Unipolar Full Range Output Voltage (Note 3)	V_{FR}	2kΩ load, logic≤0.8V, short pin 13 to pin 14. Short pin 12 to Ground and pin 10 to pin 11.	+10.0	—	+11.75	V
Bipolar Output Voltage (Note 3) ±5 Volt Range		2kΩ load, short pin 11 to pin 12. Short pin 13 to pin 14, short pin 10 to pin 11.				
	V_{FR+}	Logic Inputs ≤ 0.8V	+4.93	—	+5.94	V
	V_{FR-}	Logic Inputs ≥2.0V	−5.94	—	−4.93	
±10 Volt Range		Open pin 10				
	V_{FR+}	Logic Inputs≤0.8V	+9.86	—	+11.89	V
	V_{FR-}	Logic Inputs≥2.0V	−11.89	—	−9.86	
Bipolar Offset Voltage (Note 1) ±1/2 (| V_{FR+} | − | V_{FS-} |)		±5 Volt Range	—	±40	±70	mV
		±10 Volt Range	—	±80	±140	
Resolution			—	—	6	Bits
Logic Input "0"	V_{INL}		—	—	0.8	V
Logic Input "1"	V_{INH}		2.0	—	—	V
Logic Input Current, Each Input	I_{IN}		—	±2.0	±8	μA
Power Supply Sensitivity	P_{SS}	$\pm 12V \le V_S \le \pm 18V$ $V_{FS} \approx 10.0V$	—	±0.01	±0.15	$\%V_{FS}/V$
Power Consumption	P_d	No Load	—	200	250	mW
Supply Current	I+	V+ = +15V	—	—	7.3	mA
	I−	V− = −15V	—	—	9.3	
Settling Time to ±1/2 LSB (Note 4)	t_s	2.0V≤logic level≤0.8V $T_A = 25°C$	—	1.5	3	μs

NOTES:
1. Zero scale or bipolar offset voltage can be trimmed to zero volts or to the exact one's or two's complement condition with an external resistor network to pin 11.
2. Logic input voltage≥2.0 volts.
3. Full scale is adjustable to precisely 10 volts for unipolar operation and 10 volt or 20 volt peak-to-peak bipolar operation with an external 500 ohm potentiometer from pin 14 to V−.
4. Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.092 × 0.054 inch

1. B1 (MSB)
2. B2
3. B3
4. B4
5. B5
6. B6 (LSB)
7. V+
8. ANALOG OUTPUT (VOLTAGE)
9. GROUND
10. SCALE FACTOR
11. SUM NODE
12. BIPOLAR/UNIPOLAR
13. V−
14. FULL SCALE TRIM

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at 25° C.

PARAMETER	SYMBOL	CONDITIONS	DAC-01N BIPOLAR AND UNIPOLAR LIMIT	DAC-01G BIPOLAR AND UNIPOLAR LIMIT	UNITS
Nonlinearity	NL	$V_S = \pm 15V$	1/4	1/2	% MAX
Zero Scale Voltage	V_{ZS}	$V_S = \pm 15V$	25	35	V MAX

ELECTRICAL CHARACTERISTICS at 25° C for all grades; $V_S = \pm 15V$, unless otherwise noted.

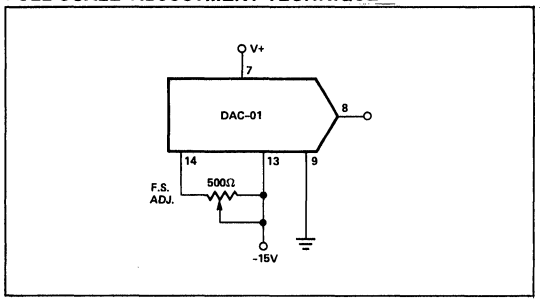
PARAMETER	SYMBOL	CONDITIONS	DAC-01 LIMIT	UNITS
Unipolar Full Scale Output Voltage (All Models)	V_{FR}	2kΩ Load, Logic ≤ 0.8V, Short V− to Full Scale Trim, Unipolar/ Bipolar to Ground, and Scale Factor to Sum Node	10.00 11.75	V MIN V MAX
Bipolar Output Voltage ±5 Volt Range ±10 Volt Range	V_{FR+} V_{FR-}	2kΩ Load, Short Sum Node to Unipolar/Bipolar. Short V− to Full Scale Trim and Scale Factor to Sum Node. Logic Inputs ≤ 0.8V Logic Inputs ≥ 2.0V Open Scale Factor	+4.93 −5.94	V MIN V MAX
	V_{FR+} V_{FR-}	Logic Inputs ≤ 0.8V Logic Inputs ≥ 2.0V	+9.78 −11.89	V MIN V MAX
Bipolar Offset Voltage $\pm 1/2 (\lvert V_{FR+} \rvert - \lvert V_{FR-} \rvert)$		±5 Volt Range ±10 Volt Range	±1/2	LSB MAX
Resolution			6	Bits MAX
Logic Input "0"	V_{INL}		0.8	V MAX
Logic Input "1"	V_{INH}		2.0	V MIN
Logic Input Current, Each Input	V_{OV}		±8.0	μA MAX
Power Supply Rejection	PSR	$\pm 12V \le V_S \le \pm 18V$, $V_S = 10.0V$	0.15	%FS/V MAX
Power Consumption	P_d	No Load	250	mW MAX

TYPICAL ELECTRICAL CHARACTERISTICS at 25° C.

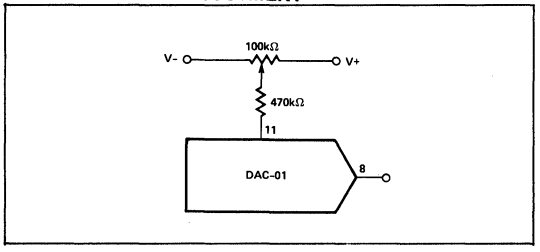
PARAMETER	SYMBOL	CONDITIONS	DAC-01N TYP	DAC-01G TYP	UNITS
Settling Time	t_S	To ±1/2 LSB	1.5	1.5	μs
Full Scale Tempco	TCV_{FS}	$V_S = \pm 15V$	60	90	ppm/° C

BASIC CIRCUIT CONNECTIONS

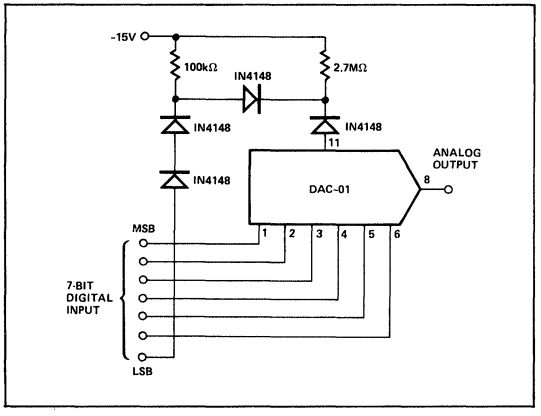
FULL SCALE ADJUSTMENT TECHNIQUE



OPTIONAL ZERO SCALE OR BIPOLAR OFFSET ADJUSTMENT



ADDITION OF 7TH BIT



APPLICATIONS INFORMATION

INPUT CODES

The DAC-01 utilizes standard complementary binary coding for unipolar mode operation (all inputs high produces zero output voltage). One's complement coding may be implemented by shorting pin 11 to pin 12 and inverting the MSB before entering pin 1 (all other bits are not inverted). Complementary offset binary coding may be implemented by shorting pin 11 to pin 12, and injecting approximately 5μA into pin 11 (which is at ground potential) by using the "zero scale or bipolar offset adjustment" circuit. Two's complement code is achieved when the MSB for complementary offset binary is complemented.

FULL SCALE ADJUST

A 500Ω pot from pin 14 to V – can be used to adjust the full range output voltage to exactly 10 volts in unipolar mode or 10 to 20 volts peak-to-peak in bipolar mode. If no pot is used, tie pin 14 to V –.

SCALE FACTOR

For +10 volts or ±5 volt outputs, short pin 10 to pin 11 (adjusts the feedback resistor around the output amplifier). For ±10 volt output, leave pin 10 open. Intermediate output voltages may be obtained by placing a pot between pin 10 and pin 11, but this will seriously degrade the full scale temperature coefficient due to the mismatch between the +1150ppm/°C tempco of the diffused resistors and the pot tempco.

CAPACITIVE LOADS

When driving capacitive loads greater than 50pF in Unipolar mode or 30pF in Bipolar mode a 100pF capacitor may be placed from pin 11 to ground for added stability.

LOWER RESOLUTION APPLICATIONS

When less than 6 bits of resolution is required, tie off unused bits to a voltage level greater than +2.0 volts. The +5 volt logic supply is usually convenient.

DAC-02/DAC-03/DAC-05

10-BIT PLUS SIGN VOLTAGE OUTPUT D/A CONVERTERS

FEATURES

- **Complete** ..... **Includes Reference and Op Amp**
- **Compact** ..... **Single 18-Pin DIP Package**
- **Bioplar Output** ..... **Sign/Magnitude Coding (DAC-03 — Unipolar Only)**
- **Monotonicity Guaranteed**
- **Nonlinearity** ..... **±1 LSB**
- **Fast** ..... **2.0μs Settling Time**
- **Stable** ..... **Full Scale Tempco 60ppm/°C**
- **Low Power Consumption** ..... **300mW Maximum**
- **TTL, CMOS Compatible Inputs**
- **MIL-STD-883 Class B Processing Available on DAC-05**

GENERAL DESCRIPTION

The DAC-02 and DAC-05 are complete 10-bit plus sign D/A converters on a single 90 x 163 mil monolithic chip. All elements of a complete sign/magnitude DAC are included — precision voltage reference, current steering logic, current sources, R-2R resistor network, logic-controlled polarity switch, and high speed internally-compensated output op amp. Monotonicity guaranteed over the entire temperature range is achieved using an untrimmed diffused R-2R resistor network. The buffered reference input is capable of tracking over a wide range of voltages, increasing application flexibility. The wide power supply range, low power consumption, wide logic input compatibility and sign/magnitude coding assures utility in a wide range of applications including CRT displays, data acquisition systems, A/D converters, servo positioning controls, and audio digitizing/reconstruction systems.

The DAC-03 is similar in construction to the DAC-02/DAC-05 except for a unipolar only output. This device is intended for low cost, limited temperature range applications, with the same general specifications as its premium counterparts.

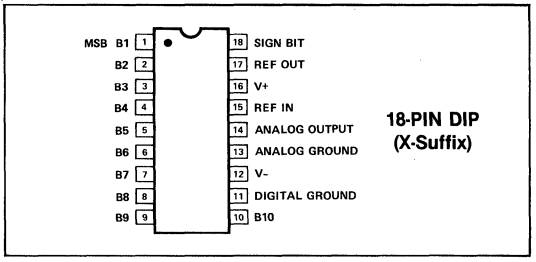
ORDERING INFORMATION†

	PACKAGE: 18 PIN HERMETIC DIP			
MONO-TONICITY	MILITARY TEMP.*	COMMERCIAL TEMP		
10	DAC05AX	DAC02ACX	DAC03ADX	DAC05EX
9	DAC05BX	DAC02BCX	DAC03BDX	DAC05FX
8	DAC05CX	DAC02CCX	DAC03CDX	DAC05GX
7	——	DAC02DDX	DAC03DDX	——

* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

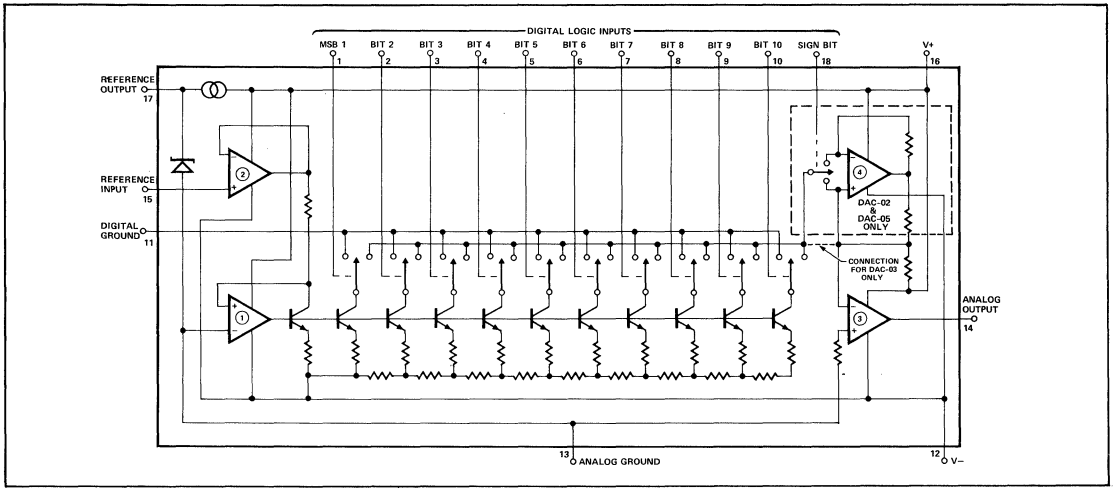
† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



18-PIN DIP (X-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note)

Operating Temperature Range
DAC-05A,B,C ..... −55°C to +125°C
DAC-02 and DAC-03, All
DAC-05E,F,G ..... 0°C to +70°C
DICE Junction Temperature (T_j) ..... −65°C to +150°C
Storage Temperature Range ..... −65°C to +150°C
V+ Supply to Analog Ground ..... 0 to +18V
V− Supply to Analog Ground ..... 0 to −18V
Analog Ground to Digital Ground ..... 0 to ±0.5V
Logic Inputs to Digital Ground .....−5V to (V + −0.7V)
Internal Reference Output Current 300μA
Reference Input Voltage ..... 0 to +10V
Internal Power Dissipation 500mW
Lead Soldering Temperature (60 sec) .....300°C
Output Short Circuit Duration .....Indefinite
(Short circuit may be to ground or either supply.)

NOTE: Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0 \le T_A \le +70°C$ for DAC-02, and DAC-05E, F & G, $T_A = 25°C$ for DAC-03 and $-55°C \le T_A \le +125°C$ for DAC-05A, B & C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-02	DAC-03	DAC-05	MIN	TYP	MAX	UNITS
Monotonicity			AC	AD	A/E	10	—	—	Bits
			BC	BD	B/F	9	—	—	Bits
			CC	CD	C/G	8	—	—	Bits
			DD	DD		7	—	—	Bits
Non-Linearity	INL		AC/BC	AD/BD		—	—	±0.1	% FS
			CC	CD	A/E	—	—	±0.2	% FS
					B/F	—	—	±0.3	% FS
			DD	DD		—	—	±0.4	% FS
					C/G	—	—	±0.5	% FS
Full Scale Tempco	T_C	INT REF	AC/BC/CC		A	—	—	±60	ppm/°C
				ALL		—	±60	—	ppm/°C
					B	—	±45	±90	ppm/°C
					E/F/G	—	±45	±100	ppm/°C
					C	—	±60	±120	ppm/°C
			DD			—	—	±150	ppm/°C
		EXT REF	ALL		ALL	—	±30	—	ppm/°C
				ALL		—	±40	—	ppm/°C
Settling Time	T_S	To 1/2 LSB, 10V Step (Note 4)	ALL	ALL	ALL	—	2	—	μs
Full Range Output Voltage (Note 1)	V_{FR}	V_{FR+} (SB High)	ALL		ALL	+10	—	+11.5	Volts
		V_{FR-} (SB Low)	ALL		ALL	−11.5	—	−10	Volts
		DAC-03 +10V		ALL		+10	—	+11.5	Volts
		+5V		ALL		+5.00	—	+5.75	Volts
Zero Scale Offset	V_{ZS}	SB High. All other logic			ALL	—	±1	±5	mV
		inputs low. $T_A = 25°C$		ALL		—	±1	±10	mV
			ALL			—	±5	±10	mV
		T_A = Min or Max	ALL		ALL	—	±2	±10	mV
Zero Scale Symmetry		(Note 2)	AC/BC/CC	N/A		—	±1	±5	mV
			DD	N/A		—	±1	±10	mV
				N/A	ALL	—	±4	±10	mV
Full Range Bipolar Symmetry		$V_{FR+} - \lvert V_{FR-} \rvert$	AC/BC/CC			—	±30	±60	mV
		(Note 3)	DD	N/A		—	±30	±80	mV
		T_A = Min − Max			ALL	—	±20	±70	mV
		$T_A = 25°C$			ALL	—	±10	±50	mV
Reference Input Bias Current	I_B		ALL	ALL	ALL	—	100	—	nA
Reference Input Impedance	Z_{IN}		ALL	ALL	ALL	—	200	—	MΩ
Reference Input Slew Rate	SR		ALL	ALL	E/F/G	—	1.5	—	V/μs
					A/B/C	—	2.0	—	
Reference Output Voltage	V_{REF}		ALL	ALL	ALL	—	6.7	—	Volts

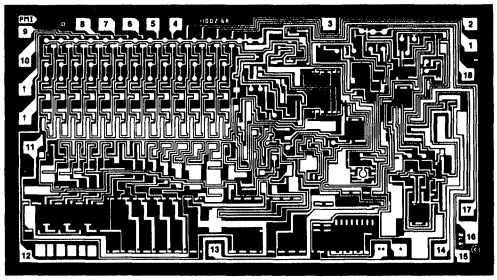
NOTES:

1. Reference Output terminal connected directly to Reference Input terminal, $R_L = 2k\Omega$, all logic inputs ≥ 2.0V.
2. Zero Scale Symmetry is the change in the output voltage produced by switching the Sign Bit with all logic bits low ($V_{ZS+} - V_{ZS-}$).
3. Full Scale Bipolar Symmetry is the magnitude of the difference between V_{FR+} and $|V_{FR-}|$.
4. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0 \leq T_A \leq +70°C$ for DAC-02, and DAC-05E, F & G, $T_A = 25°C$ for DAC-03 and $-55°C \leq T_A \leq +125°C$ for DAC-05A, B & C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-02	DAC-03	DAC-05	MIN	TYP	MAX	UNITS
Logic Input Current	I_{IN}	Each input	ALL	ALL		—	±1.0	—	μA
		−5V to $(V_+ - 0.7)V$			ALL	—	±1.0	±10.0	
Logic Input 0	V_{INL}		ALL	ALL	ALL	—	—	0.8	Volts
Logic Input 1	V_{INH}		ALL	ALL	ALL	2.0	—	—	Volts
Positive Supply Current	I+		AC/BC/CC		ALL	—	+7	+10	mA
			DD	ALL		—	+7	+11.6	mA
Negative Supply Current	I−		AC/BC/CC		ALL	—	−9	−10	mA
			DD			—	−9	−11.6	mA
				ALL		—	−10	−11.6	mA
Power Supply Sensitivity	P_{SS}	$V_S = \pm 12$ to $\pm 18V$	AC/BC/CC			—	±0.015	±0.05	% V_{FS}/V
			DD	ALL		—	±0.015	±0.1	% V_{FS}/V
		T_A = Min to Max			ALL	—	±0.05	±0.1	% V_{FS}/V
		$T_A = 25°C$			ALL	—	±.02	±.05	% V_{FS}/V
Power Dissipation	P_d	$I_{OUT} = 0$	AC/BC/CC			—	225	300	mW
			DD	ALL		—	225	350	mW
		$T_A = 25°C$			ALL	—	200	300	mW
		T_A = Min to Max			ALL	—	250	350	mW
Output Drive Current	I_O		N/A	ALL	N/A	—	—	5	mA

DICE CHARACTERISTICS



DIE SIZE 0.163 X 0.090 inch

1. BIT 1-MSB
2. BIT 2
3. BIT 3
4. BIT 4
5. BIT 5
6. BIT 6
7. BIT 7
8. BIT 8
9. BIT 9
10. BIT 10
11. DIGITAL GROUND
12. V–
13. ANALOG GROUND
14. ANALOG OUTPUT
15. REF IN
16. V+
17. REF OUT
18. SIGN BIT

Refer to Section 2 for additional DICE information.

†Bits 11 & 12 (not normally used)

NOTE: Voltage output range programmable by connecting *(10V) to analog output for 10 volt range. Jumps from **(5V) to analog output for 5 volt range.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, 25° C, and +10V Full Scale Output unless otherwise noted.

PARAMETER	CONDITIONS	DAC-02-N LIMIT	DAC-02-G LIMIT	DAC-02-GR LIMIT	UNITS
Resolution (Bits 11 and 12 Not Normally Used)	Bipolar Output Unipolar Output	13 12	13 12	13 12	Bits MAX
Monotonicity		9	8	7	Bits MIN
Nonlinearity		±0.1	±0.2	±0.4	% FS MAX
Zero Scale Offset	Sign Bit High, All Other Inputs Low	±10	±10	±10	mV MAX
Zero Scale Symmetry	±10V Full Scale	±5.0	±5.0	±10	mV MAX
Full Scale Bipolar Symmetry	±10V Full Scale	±60	±60	±80	mV MAX
Power Supply Rejection	$V_S = \pm 12V$ to $\pm 18V$	0.05	0.05	0.1	$\%V_{FS}/V$ MAX
Power Dissipation	$I_{OUT} = 0$	300	300	350	mW MAX
Logic Input "0"		0.8	0.8	0.8	V MAX
Logic Input "1"		2.0	2.0	2.0	V MIN
Output Voltage Analog (All Bits High)	V_{FR} + (Sign Bit High) V_{FR} - (Sign Bit Low)	±11.5 ±10	±11.5 ±10	±11.5 ±10	V MAX V MIN

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and +10V Full Scale Output, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-02-N TYP	DAC-02-G TYP	DAC-02-GR TYP	UNITS
Full Scale Tempco	TCV_{FS}	Internal Reference	60	60	90	ppm/° C
Settling Time ($T_A = 25°C$)	t_s	To ±1/2 LSB 10 Volt Step	2.0	2.0	2.0	μS
Logic Input Current		$T_A = 25°C$	1.0	1.0	1.0	μA

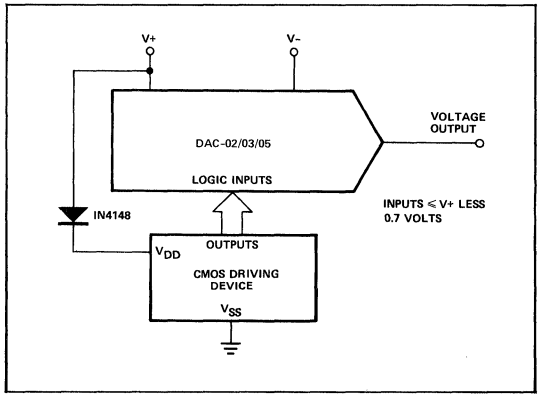
NOTE: When ordering DICE in this series, use DAC-02 numbers and grades above.

TYPICAL APPLICATIONS

The DAC-02's, DAC-03's and DAC-05's logic input stages require about 1μA and are capable of operation with inputs between −5 volts and V+ less 0.7 volt. This wide input voltage range allows direct CMOS interfacing in most applications, the exception being where the CMOS logic and D/A converter must use the same positive power supply.

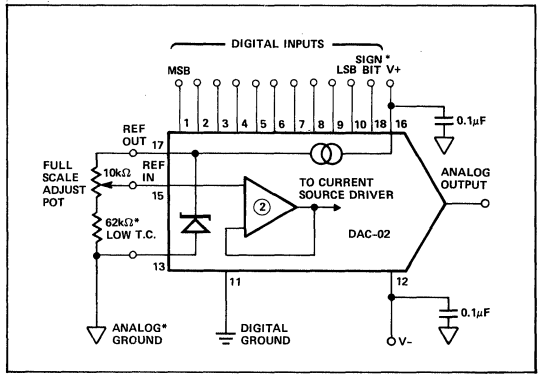
In this special case, a diode should be placed in series with the CMOS driving device's V_{DD} lead as shown in Figure 1. The diode limits V_D to V+ less 0.7 volt — since the output from the CMOS device cannot exceed this value, the DAC's maximum input voltage rule is satisfied. Summarizing: in all applications, the DAC-02, DAC-03 and DAC-05 require either no interfacing components, or at most a single inexpensive diode for full CMOS compatibility.

CMOS LOGIC INTERFACE CIRCUIT



CONNECTION INFORMATION

FULL SCALE ADJUSTMENT CIRCUIT



FULL SCALE ADJUSTMENT

Full Range output voltage may be trimmed by use of a potentiometer and series resistor as shown; however, best results will be obtained if a low tempco resistor is used or if pot and resistor tempcos match. Alternatively, a single pot of ≤72kΩ may be used.

REFERENCE INPUT BYPASS

Lowest noise and fastest settling operation will be obtained by bypassing the Reference Input to Analog Ground with a 0.01μF disk capacitor.

GROUNDING

For optimum noise rejection, separate digital and analog grounds have been brought out. Best results will be obtained if these grounds are connected together at one point only, preferably near the DAC-02, DAC-03 and DAC-05 package, so that the large digital currents do not flow through the analog ground path.

APPLICATIONS INFORMATION

LOWER RESOLUTION APPLICATIONS

For applications not requiring full 10-bit resolution, unused logic inputs should be tied to ground.

UNIPOLAR OPERATION

Operation as a 10-bit straight binary converter may be implemented by permanently tying the Sign Bit to +5V (for positive Full Scale output) or to ground (for negative Full Scale output). In the DAC-03 only, Pin 18 unipolar enable is tied to Pin 17.

POWER SUPPLIES

The DAC-02, DAC-03 and DAC-05 will operate within specifications for power supplies ranging from ±12V to ±18V. Power supplies should be bypassed near the package with a 0.1μF disk capacitor.

CAPACITIVE LOADING

The output operational amplifier provides stable operation with capacitive loads up to 100pF.

REFERENCE OUTPUT

For best results, Reference Output current should not exceed 100μA.

USE WITH EXTERNAL REFERENCES

Positive-polarity external reference voltages referred to Analog Ground may be applied to the Reference Input terminal to improve Full Scale Tempco, to provide tracking to other system elements, or to slave a number of DAC-02s, DAC-03s and DAC-05s to the Reference Output of any one of them. This reference voltage should be between +5V to +7V for optimum performance.

SIGN PLUS MAGNITUDE CODING TABLE (DAC-02 and DAC-05)

	SIGN BIT	MSB								LSB
+ FULL RANGE	1	1	1	1	1	1	1	1	1	1
+ HALF SCALE	1	1	0	0	0	0	0	0	0	0
ZERO SCALE (+)	1	0	0	0	0	0	0	0	0	0
ZERO SCALE (−)	0	0	0	0	0	0	0	0	0	0
− HALF SCALE	0	1	0	0	0	0	0	0	0	0
− FULL SCALE	0	1	1	1	1	1	1	1	1	1

DAC-04/DAC-06

TWO'S COMPLEMENT 10-BIT D/A CONVERTER

FEATURES

- **Complete** ..... **Includes Reference and Op Amp**
- **Compact** ..... **Single 18-Pin DIP Package**
- **Bipolar Output** ..... **Two's Complement Coding**
- **Monotonicity Guaranteed**
- **Nonlinearity** ..... **±1 LSB**
- **Fast** ..... **1.5μs Settling Time**
- **Low Power Consumption** ..... **300mW Maximum**
- **TTL, CMOS Compatible Inputs**
- **125°C Tested Dice Available**

GENERAL DESCRIPTION

The DAC-04 and DAC-06 are complete 10-Bit Two's Complement D/A Converters on a single 90 x 163 mil monolithic chip. All elements of a complete bipolar output Two's Complement DAC are included — precision voltage reference, current steering logic, current sources, R-2R resistor network, bipolar offset circuit and high speed internally compensated output op amp. Monotonicity guaranteed over the entire 0° C to +70° C temperature range is achieved using an untrimmed diffused R-2R resistor network. The buffered reference input is capable of tracking over a wide range of voltages, increasing application flexibility. The user may also easily implement One's Complement, Straight Offset Binary, or unipolar operation. The ±12V to ±18V power supply range, low power consumption, TTL and CMOS compatibility, wide logic input compatibility, and adaptable logic coding capability assure utility in a wide range of applications.

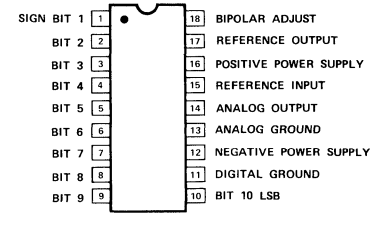
ORDERING INFORMATION†

PACKAGE 18 PIN HERMETIC DIP			
MONO-TONICITY	MILITARY TEMP*	COMMERCIAL TEMP	
10		DAC-06EX	
9	DAC-06BX	DAC-04BCX	DAC-06FX
8	DAC-06CX	DAC-04CCX	DAC-06GX
7		DAC-04DDX	

* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

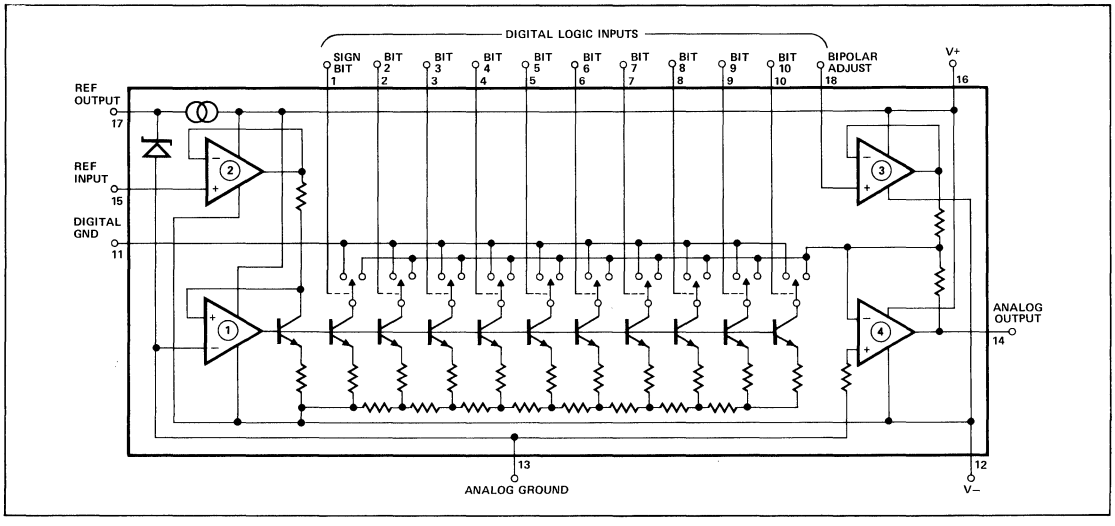
† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



18-PIN DIP (X-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note)

Operating Temperature Range
DAC-06B,C ..... −55°C to +125°C
DAC-04B,C,D, DAC-06E,F,G ..... 0°C to +70°C
DICE Junction Temperature (T_j) ..... −65°C to +150°C
Storage Temperature Range ..... −65°C to +150°C
V+ Supply to Analog Ground ..... 0 to +18V
V− Supply to Analog Ground ..... 0 to −18V
Analog Ground to Digital Ground ..... 0 to ±0.5V
Logic Inputs to Digital Ground ..... −5V to (V+ −0.7)V
Internal Reference Output Current 300μA
Reference Input Voltage ..... 0 to +10V
Bipolar Offset Input Voltage ..... 0 to +10V
Internal Power Dissipation 500mW
Lead Soldering Temperature (60 sec) ..... 300°C
Output Short Circuit Duration ..... Indefinite
(Short circuit may be to ground or either supply)

NOTE: Ratings apply to both DICE and packaged devices unless otherwise noted.

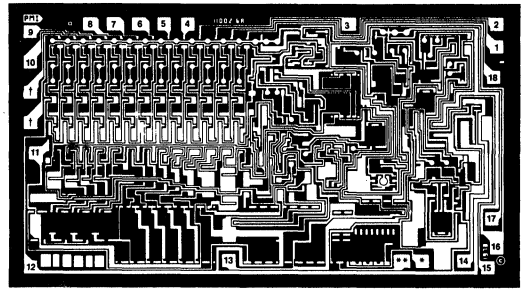
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$; $-55°C \le T_A \le +125°C$ for DAC-06B & C; and $0°C \le T_A \le +70°C$ for DAC-04B, C & D and DAC-06E, F & G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-04	DAC-06	MIN	TYP	MAX	UNITS
Resolution			All	All	10	—	10	Bits
Monotonicity				E	10	—	—	Bits
			BC	B/F	9	—	—	Bits
			CC	C/G	8	—	—	Bits
			DD		7	—	—	Bits
Nonlinearity	NL	$T_A = 25°C$		E	±0.1	—	—	% FS
				B/F	±0.2	—	—	% FS
				C/G	±0.4	—	—	% FS
		T_A = Full Temp	BC		±0.1	—	—	% FS
			CC	E	±0.2	—	—	% FS
				B/F	±0.3	—	—	% FS
			DD		±0.4	—	—	% FS
				C/G	±0.5	—	—	% FS
Full Scale Tempco	$TC_{V_{FS}}$	Total Internal Ref Connected	BC/CC	B	—	±45	±90	ppm/°C
				E/F/G	—	±45	±100	ppm/°C
				C	—	±60	±120	ppm/°C
			DD		—	±60	±150	ppm/°C
		Zero Drift Ext Ref Applied	BC/CC	All	—	±30	—	ppm/°C
			DD		—	±50	—	ppm/°C
Settling Time	T_S	To ±1/2 LSB, 10V Step	BC/CC	All	—	1.5	—	μs
			DD		—	2.5	—	μs
Unipolar Zero Scale Output	V_{ZS}	Short Pin 18 to Ground (Note 1) $T_A = 25°C$		All	—	±1	±5	mV
		T_A = Full Temp		All	—	±2	±10	mV
			All		—	±5	—	mV
Bipolar Offset Voltage	BP Off	Connect Pins 15, 17 & 18 (Note 2)	All	All	−5.0	—	+2.5	% Range
Full Range Output Voltage	V_{FR}	Connect Pin 15 to 17 (Note 2) $R_L = 2k\Omega$	All	All	10	—	11.5	V
Reference Input Bias Current	I_B		All	All	—	100	—	nA
Reference Input Impedance	Z_{IN}		All	All	—	200	—	MΩ
Reference Input Slew Rate	SR		All	All	—	1.5	—	V/μs
Reference Output Voltage	V_{REF}		All	All	—	6.7	—	V
Logic Input Current	I_{IN}	Each Input	All		—	1.0	—	μA
		−5V to (V+ −0.7)V		All	—	1	10	μA
Logic Input "0"	V_{INL}		All	All	—	—	0.8	V
Logic Input "1"	V_{INH}		All	All	2.0	—	—	V
Power Supply Sensitivity	P_{SS}	$V_S = \pm 12$ to $\pm 18V$ $T_A = 25°C$		All	—	±0.02	±0.05	% FS/V
		T_A = Full Temp	BC/CC		—	±0.015	±0.1	% FS/V
				All	—	±0.02	±0.1	% FS/V
			DD		—	±0.015	—	% FS/V
Supply Current	I+	$T_A = 25°C$	BC/CC	All	—	7	10	mA
			DD		—	7	11.6	mA
	I−	$T_A = 25°C$	BC,CC	All	—	−9	−10	mA
			DD		—	−9	−11.6	mA
Power Dissipation	P_D	$T_A = 25°C$	BC,CC	All	—	250	300	mW
			DD		—	250	350	mW
		T_A = Full Temp		All	—	—	350	mW

NOTES:

1. May be operated in the 0 to +10V unipolar mode by shorting Pin 18 to Ground.
2. $V_{FR} = |V_{FR}+| + |V_{FR}-|$ and is trimmable to exactly 10V range with the circuit shown in typical applications.
3. Bipolar offset voltage is trimmable to exact two's or one's complement condition with the circuit shown in typical applications.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



DIE SIZE 0.163 × 0.090 inch

Refer to Section 2 for additional DICE information.

1. BIT 1 MSB (SIGN BIT)
2. BIT 2
3. BIT 3
4. BIT 4
5. BIT 5
6. BIT 6
7. BIT 7
8. BIT 8
9. BIT 9
10. BIT 10 LSB
11. DIGITAL GROUND
12. V–
13. ANALOG GROUND
14. ANALOG OUTPUT
15. REF IN
16. V+
17. REF OUT
18. BIPOLAR ADJUST

NOTE:
Voltage Output Range programmable by connecting *(10V) to Analog Output for 10 volt range. Jumper from **(5V) to Analog Output sets device to 5 volt range.
† Two additional least significant bits are provided.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 125°C$ for DAC-04NT, GT and $T_A = 25°C$ for DAC-04N, G, GR, unless otherwise noted.

PARAMETER	CONDITIONS	DAC-04NT LIMIT	DAC-04N LIMIT	DAC-04GT LIMIT	DAC-04G LIMIT	DAC-04GR LIMIT	UNITS
Resolution	Bipolar Output	12	12	12	12	12	Bits Min
Monotonicity		10	9	9	8	7	Bits Min
Nonlinearity		±0.2	±0.2	±0.4	±0.2	±0.4	% FS Min
Bipolar Offset Voltage	Short Ref Input to Reference	+2.5	+2.5	+2.5	+2.5	+2.5	V MAX
	Output and Bipolar Adjust	−5.0	−5.0	−5.0	−5.0	−5.0	V Min
Power Supply Rejection	$V_S = \pm 12V$ to $\pm 18V$	0.1	0.1	0.1	0.1	0.15	$\%V_{FS}$ Max
Power Dissipation	$I_{OUT} = 0$	350	300	350	300	350	mW Max
Logic Input "0"		0.8	0.8	0.8	0.8	0.8	V Max
Logic Input "1"		2.0	2.0	2.0	2.0	2.0	V Min
Analog Output Voltage	Short Reference Input	11.5	11.5	11.5	11.5	11.5	V Max
	to Reference Output	10.0	10.0	10.0	10.0	10.0	V Min

NOTE: For 25°C characteristics of DAC-04NT & GT, see DAC-04N & G characteristics respectively.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and ±5V Full Scale Output, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-04NT TYP	DAC-04N TYP	DAC-04GT TYP	DAC-04G TYP	DAC-04GR TYP	UNITS
Full Scale Tempco	TCV_{FS}	Internal Reference	±60	±60	±60	±60	±90	ppm/°C
Settling Time ($T_A = 25°C$)	t_S	To ±1/2 LSB 10 Volt Step	1.5	1.5	1.5	1.5	1.5	μs
Logic Input Current		$T_A = 25°C$	1.0	1.0	1.0	1.0	1.0	nA

TYPICAL APPLICATIONS

ADJUSTNG FOR TWO'S COMPLEMENT CODING

1. Connect Full Scale Adjust and Bipolar Adjust Circuitry as shown in figure.
2. Turn all bits OFF (V_{FS-}) = 1000000000
3. Adjust Bipolar Pot for V_{FS} at output ..... −5.000V
4. Turn all bits ON (V_{FR+}) − 0111111111
5. Adjust Full Scale Pot for desired V_{FR+} value ..... +4.990V
6. Check Zero Scale Reading (V_{ZS}) − 0000000000
   If this reading is outside desired V_{ZS} range, readjust Bipolar Pot until the output reads 0.0000V.

TWO'S COMPLEMENT CODING TABLE

	INPUT MSB									LSB	IDEAL OUTPUT
V_{FS+} −1LSB	0	1	1	1	1	1	1	1	1	1	+4.990V
V_{FS+} −2LSB	0	1	1	1	1	1	1	1	1	0	+4.980V
+1LSB	0	0	0	0	0	0	0	0	0	1	+0.010V
Zero	0	0	0	0	0	0	0	0	0	0	0.000V
−1LSB	1	1	1	1	1	1	1	1	1	1	−0.010V
V_{FS-} +LSB	1	0	0	0	0	0	0	0	0	1	−4.990V
V_{FS-}	1	0	0	0	0	0	0	0	0	0	−5.000V

ADJUSTING FOR ONE'S COMPLEMENT CODING

1. Connect Full Scale Adjust and Bipolar Adjust Circuitry as shown in above figure.
2. Turn all bits OFF (V_{FR-}) − 1000000000
3. Adjust Bipolar Pot for V_{FR-} at output ..... −5.0000V
4. Turn all bits ON (V_{FR+}) − 0111111111
5. Adjust Full Scale Pot for desired V_{FR+} value ..... +5.0000V

ONE'S COMPLEMENT CODING TABLE

	INPUT MSB									LSB	IDEAL OUTPUT
V_{FS+} −1LSB	0	1	1	1	1	1	1	1	1	1	+5.000V
V_{FS+} −2LSB	0	1	1	1	1	1	1	1	1	0	+4.990V
+0	0	0	0	0	0	0	0	0	0	0	+0.005V
−0	1	1	1	1	1	1	1	1	1	1	−0.005V
V_{FS-} +2LSB	1	0	0	0	0	0	0	0	0	1	−4.990V
V_{FS-} +1LSB	1	0	0	0	0	0	0	0	0	0	−5.000V

Note that two zero states will straddle (±1/2 LSB) the true zero. Therefore the DAC will give symmetrical outputs for both positive and negative full scale.

REFERENCE OUTPUT

For best results, Reference Output current should not exceed 100μA.

POWER SUPPLIES

The DAC-04 and DAC-06 will operate within specifications for power supplies ranging from ±12V to ±18V. Power supplies should be bypassed near the package with a 0.1μF disk capacitor. Chip users should connect the substrate to V−.

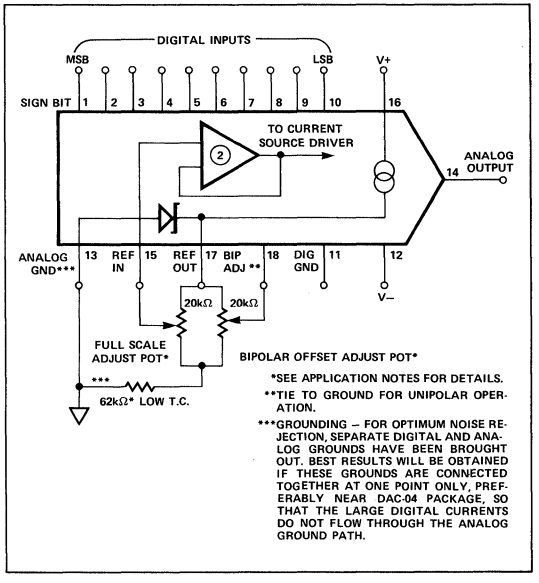
GROUNDING

For optimum noise rejection, separate digital and analog grounds have been brought out. Best results will be obtained if these grounds are connected together at one point only, preferably at the DAC-04 and DAC-06 package, so that large degital currents do not flow through the analog ground path.

CAPACITIVE LOADING

The output operational amplifier provides stable operation with capacitive loads up to 100pF.

FULL SCALE OUTPUT RANGE AND BIPOLAR OFFSET ADJUSTMENT CIRCUIT



EXTERNAL ADJUSTMENT NETWORK

Full Scale Output Range and Bipolar Offset may be adjusted by using the circuit shown in the figure above. Best results will be obtained when low tempco pots and resistors are used, or if pot and resistor tempcos match.

TYPICAL APPLICATIONS

IMPLEMENTING

Offset Binary coding is exactly the same as Two's Complement coding except that the most significant bit occurs in true, rather than inverted form and the output states are relabeled. To convert the DAC-04 and DAC-06 to Offset Binary code operation, simply place a logic inverter in series with the MSB input (Pin 1) and invert the MSB value shown in steps 2, 4 and 6 of the Two's Complement adjustment procedure shown above.

OFFSET BINARY CODING TABLE

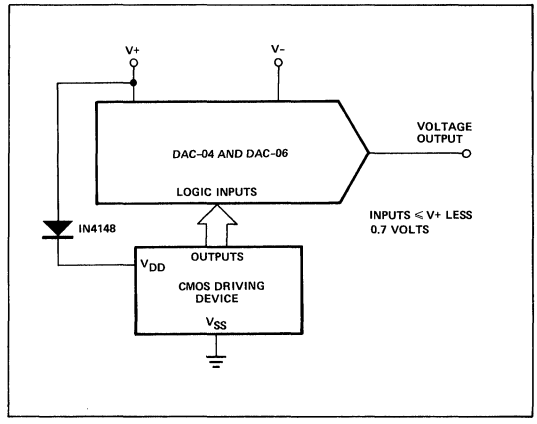
	INPUT										IDEAL
	MSB									LSB	OUTPUT
V_{FS+} −1LSB	1	1	1	1	1	1	1	1	1	1	+4.990V
V_{FS+} −2LSB	1	1	1	1	1	1	1	1	1	0	+4.980V
ZERO	1	0	0	0	0	0	0	0	0	0	0.00
ZERO 1LSB	0	1	1	1	1	1	1	1	1	1	−0.005V
V_{FS-} +1LSB	0	0	0	0	0	0	0	0	0	1	−4.990V
V_{FS-}	0	0	0	0	0	0	0	0	0	0	−5.000V

INTERFACING WITH CMOS LOGIC

The DAC-04 and DAC-06 logic input stages require about 1μA and are capable of operation with inputs between −5 volts and V+ less 0.7 volt. This wide input voltage range allows direct CMOS interfacing in most applications, the exception being where the CMOS logic and D/A converter must use the same positive power supply.

In this special case, a diode should be placed in series with the CMOS driving device's V_{DD} lead as shown in Figure 1. The diode limits V_D to V+ less 0.7 volt — since the output from the CMOS device cannot exceed this value, the DAC's maximum input voltage rule is satisfied. Summarizing: in all applications, the DAC-06 requires either no interfacing components, or at most a single inexpensive diode for full CMOS compatibility.

CMOS LOGIC INTERFACE CIRCUIT



DAC-08

8-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER

UNIVERSAL DIGITAL LOGIC INTERFACE

FEATURES

- **Fast Settling Output Current** **85ns**
- **Full Scale Current Prematched to ±1 LSB**
- **Direct Interface to TTL, CMOS, ECL, HTL, PMOS**
- **Nonlinearity to ±0.1% Maximum Over Temperature Range**
- **High Output Impedance and Compliance** ..... **−10V to +18V**
- **Differential Current Outputs**
- **Wide Range Multiplying Capability** ... **1MHz Bandwidth**
- **Low FS Current Drift** ..... **±10ppm/°C**
- **Wide Power Supply Range** ..... **±4.5V to ±18V**
- **Low Power Consumption** ..... **33mW @ ±5V**
- **Low Cost**

GENERAL DESCRIPTION

The DAC-08 series of 8-bit monolithic Digital-to-Analog Converters provide very high-speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85nS settling times with very low "glitch" and at low power consumption. Monotonic multiplying performance is attained over a wide 40 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

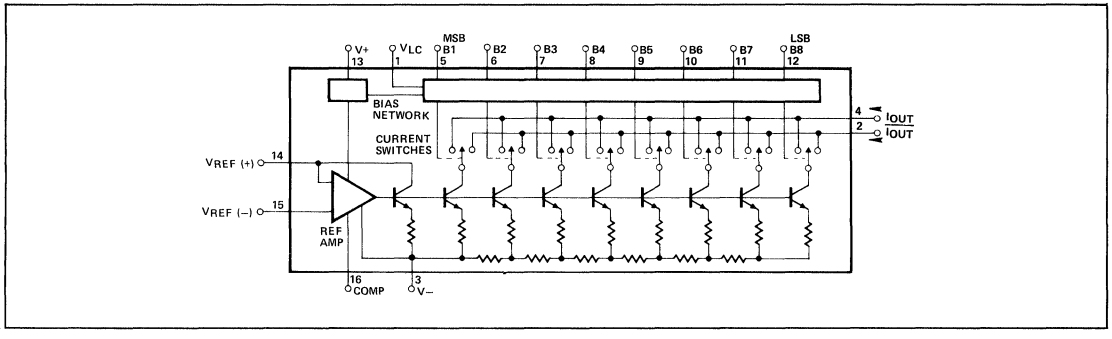
High-voltage compliance dual-complementary current outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. In many applications, the outputs can be directly converted to voltage without the need for an external op amp.

All DAC-08 series models guarantee full 8-bit monotonicity, and nonlinearities as tight as ±0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5 to ±18V power supply range, with 33mW power consumption attainable at ±5V supplies.

The compact size and low power consumption make the DAC-08 attractive for portable and military/aerospace applications; devices processed to MIL-STD-883, Level B are available.

DAC-08 applications include 8-bit, 1μS A/D converters, servo motor and pen drivers, waveform generators, audio encoders and attenuators, analog meter drivers, programmable power supplies, CRT display drivers, high-speed modems and other applications where low cost, high speed and complete input/output versatility are required.

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Operating Temperature
- DAC-08AQ, Q ..... −55°C to +125°C
- DAC-08HQ, EQ, CQ ..... 0°C to +70°

DICE Junction Temperature (T_j) ..... −65°C to +150°C
Storage Temperature ..... −65°C to 150°C
Power Dissipation* 500mW
- Derate above 100°C ..... 10mW/°C

Lead Soldering Temperature (60 sec.) ..... 300°C

*Over full operating range

V+ Supply to V− Supply 36V
Logic Inputs ..... V− to V− plus 36V
V_{LC} ..... V− to V+
Analog Current Outputs (at V_S^- = 15V) 4.25mA
Reference Inputs (V_{14} to V_{15}) ..... V− to V+
Reference Input Differential Voltage (V_{14} to V_{15}) ..... ±18V
Reference Input Current (I_{14}) 5.0mA

NOTE: Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

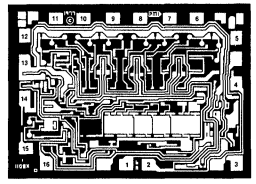
ELECTRICAL CHARACTERISTICS

at V_S = ±15V, I_{REF} = 2.0mA, T_A = 0°C to +70°C unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-08A/H MIN	DAC-08A/H TYP	DAC-08A/H MAX	DAC-08/E MIN	DAC-08/E TYP	DAC-08/E MAX	DAC-08C MIN	DAC-08C TYP	DAC-08C MAX	UNITS
Resolution			8	8	8	8	8	8	8	8	8	Bits
Monotonicity			8	8	8	8	8	8	8	8	8	Bits
Nonlinearity		T_A = 0°C to 70°C	—	—	±0.1	—	—	±0.19	—	—	±0.39	%FS
Settling Time	t_s	To ±½ LSB, all bits switched ON or OFF, T_A = 25°C (See Note)	—	85	135	—	85	150	—	85	150	ns
Propagation Delay												
Each bit	t_{PLH}	T_A = 25°C	—	35	60	—	35	60	—	35	60	ns
All bits switched	t_{PHL}	(See Note)	—	35	60	—	35	60	—	35	60	
Full Scale Tempco	TCI_{FS}		—	±10	±50	—	±10	±80	—	±10	±80	ppm/°C
		DAC-08E	—	—	—	—	—	±50	—	—	—	
Output Voltage Compliance (True Compliance)	V_{OC}	Full scale current change < ½ LSB, R_{OUT} > 20MΩ typical	−10	—	+18	−10	—	+18	−10	—	−18	Volts
Full Range Current	I_{FR4}	V_{REF} = 10.000V R_{14}, R_{15} = 5.000kΩ T_A = +25°C	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Range Symmetry	I_{FRS}	$I_{FR4} - I_{FR2}$	—	±0.5	±4.0	—	±1.0	±8.0	—	±2.0	±16.0	μA
Zero Scale Current	I_{ZS}		—	0.1	1.0	—	0.2	2.0	—	0.2	4.0	μA
Output Current Range	I_{OR1} I_{OR2}	R_{14}, R_{15} = 5.000kΩ V_{REF} = +15.0V, V− = −10V V_{REF} = +25.0V, V− = −12V	2.1 4.2	— —	— —	2.1 4.2	— —	— —	2.1 4.2	— —	— —	mA
Logic Input Levels												
Logic "0"	V_{IL}	V_{LC} = 0V	—	—	0.8	—	—	0.8	—	—	0.8	Volts
Logic Input "1"	V_{IH}		2.0	—	—	2.0	—	—	2.0	—	—	
Logic Input Current		V_{LC} = 0V										
Logic "0"	I_{IL}	V_{IN} = −10V to +0.8V	—	−2.0	−10	—	−2.0	−10	—	−2.0	−10	μA
Logic Input "1"	I_{IH}	V_{IN} = 2.0V to 18V	—	0.002	10	—	0.002	10	—	0.002	10	
Logic Input Swing	V_{IS}	V− = −15V	−10	—	+18	−10	—	+18	−10	—	+18	Volts
Logic Threshold Range	V_{THR}	V_S = ±15V	−10	—	+13.5	−10	—	+13.5	−10	—	+13.5	Volts
Reference Bias Current	I_{15}		—	−1.0	−3.0	—	−1.0	−3.0	—	−1.0	−3.0	μA
Reference Input Slew Rate	dI/dt	R_{EQ} ≈ 200Ω See fast pulsed R_L = 100Ω ref. info. C_C = 0pF following.	4.0	8.0	—	4.0	8.0	—	4.0	8.0	—	mA/μs
Power Supply Sensitivity	$PSSI_{FS+}$	V+ = 4.5V to 18V	—	±0.0003	±0.01	—	±0.0003	±0.01	—	±0.0003	±0.01	$\%\Delta I_O/\%\Delta V+$
	$PSSI_{FS-}$	V− = −4.5V to −18V I_{REF} = 1.0mA	—	±0.002	±0.01	—	±0.002	±0.01	—	±0.002	±0.01	$\%\Delta I_O/\%\Delta V-$
Power Supply Current	I+	V_S = ±5V, I_{REF} = 1.0mA	—	2.3	3.8	—	2.3	3.8	—	2.3	3.8	mA
	I−		—	−4.3	−5.8	—	−4.3	−5.8	—	−4.3	−5.8	
	I+	V_S = +5V, −15V, I_{REF} = 2.0mA	—	2.4	3.8	—	2.4	3.8	—	2.4	3.8	
	I−		—	−6.4	−7.8	—	−6.4	−7.8	—	−6.4	−7.8	
	I+	V_S = ±15V, I_{REF} = 2.0mA	—	2.5	3.8	—	2.5	3.8	—	2.5	3.8	
	I−		—	−6.5	−7.8	—	−6.5	−7.8	—	6.5	7.8	
Power Dissipation	P_d	±5V, I_{REF} = 1.0mA	—	33	48	—	33	48	—	33	48	mW
		+5V, −5V, I_{REF} = 2.0mA	—	108	136	—	103	136	—	108	136	
		±15V, I_{REF} = 2.0mA	—	135	174	—	135	174	—	135	174	

NOTE: Guaranteed by design.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



DIE SIZE 0.085 × 0.062 inch

1. V_{LC}
2. $I_{\overline{OUT}}$
3. V−
4. I_{OUT}
5. BIT 1 (MSB)
6. BIT 2
7. BIT 3
8. BIT 4
9. BIT 5
10. BIT 6
11. BIT 7
12. BIT 8 (LSB)
13. V+
14. V_{REF} (+)
15. V_{REF} (−)
16. COMP

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 125°C$ for DAC-08NT, GT and $T_A = 25°C$ for DAC-08N, G, GR, $I_{REF} = 2.0mA$, unless otherwise noted. Output characteristics apply to both I_{OUT} and $I_{\overline{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-08NT LIMIT	DAC-08N LIMIT	DAC-08GT LIMIT	DAC-08G LIMIT	DAC-08GR LIMIT	UNITS
Resolution			8	8	8	8	8	Bits MIN
Monotonicity			8	8	8	8	8	Bits MIN
Nonlinearity			±0.1	±0.1	±0.19	±0.19	±0.39	Bits MIN
Output Voltage Compliance	V_{OC}	Full Scale Current Change < 1/2 LSB	+18 −10	+18 −10	+18 −10	+18 −10	+18 −10	Volts MAX Volts MIN
Full Scale Current	I_{FS4} or I_{FS2}	$V_{REF} = 10.000V$ $R_{14}, R_{15} = 5.000k\Omega$	2.04 1.94	2.04 1.94	2.04 1.94	2.04 1.94	2.04 1.94	mA MAX mA MIN
Full Scale Symmetry	I_{FSS}		±8.0	±8.0	±8.0	±8.0	±16	nA MAX
Zero Scale Current	I_{ZS}		2.0	2.0	4.0	4.0	4.0	nA MAX
Output Current Range	I_{FS1} or	V− = −5.0V, V_{REF} = +15V V− = −7.0V,	2.1	2.1	2.1	2.1	2.1	mA MAX
	I_{FS2}	V_{REF} = +25V $R_{14}, R_{15} = 5.000k\Omega$	4.2	4.2	4.2	4.2	4.2	mA MAX
Logic Input "0"	V_{IL}		0.8	0.8	0.8	0.8	0.8	V MAX
Logic Input "1"	V_{IH}		2.0	2.0	2.0	2.0	2.0	V MIN
Logic Input Current Logic "0" Logic "1"	 V_{IL} I_{IH}	V_{LC} = 0V V_{IN} = −10V to +0.8V V_{IN} = 2.0V to 18V	 ±10 ±10	 ±10 ±10	 ±10 ±10	 ±10 ±10	 ±10 ±10	 μA MAX
Logic Input Swing	V_{IS}	V− = −15V	+18 −10	+18 −10	+18 −10	+18 −10	+18 −10	V MAX V MIN
Reference Bias Current	I_{15}		3.0	3.0	3.0	3.0	3.0	μA MAX
Power Supply Sensitivity	$PSSI_{FS+}$ $PSSI_{FS-}$	V+ = 4.5V to 18V V− = −4.5V to −18V I_{REF} = 1.0mA	0.01	0.01	0.01	0.01	0.01	%FS/%V MAX
Power Supply Current	I+	$V_S = \pm 15V$ $I_{REF} \leq 2.0mA$	3.8 −7.8	3.8 −7.8	3.8 −7.8	3.8 −7.8	3.8 −7.8	mA MAX
Power Dissipation	P_d	$V_S = \pm 15V$ $I_{REF} \leq 2.0mA$	174	174	174	174	174	mW MAX

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and $I_{REF} = 2.0mA$, unless otherwise noted. Output characteristics apply to both I_{OUT} and $I_{\overline{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	ALL GRADES TYPICAL	UNITS
Reference Input Slew Rate	dI/dt		8.0	mA/ns
Propagation Delay	t_{PLH}, t_{PHL}	$T_A = 25°C$, Any Bit	35	ns
Settling Time	t_S	To ±1/2 LSB, All Bits Switched ON or OFF, $T_A = 25°C$	85	ns

NOTE:
For DAC08NT & GT 25°C characteristics, see DAC08N & G characteristics respectively.

ORDERING INFORMATION† **

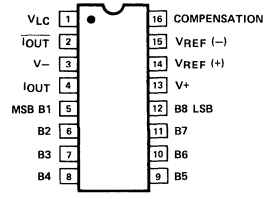
NL	DUAL INLINE PACKAGE HERMETIC 16 PIN	DUAL INLINE PACKAGE PLASTIC 16 PIN	OPERATING TEMPERATURE RANGE
0.1%	DAC08AQ*	DAC08HP	MIL
	DAC08HQ		COM
0.1%	DAC08Q*	DAC08EP	MIL
	DAC08EY		COM
0.39%	DAC08CQ	DAC08CP	COM

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number.

†All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

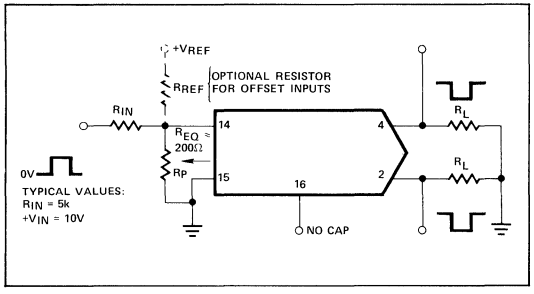
**See JM38510/11301/11302, this section, for JAN qualified DAC-08.

PIN CONNECTION

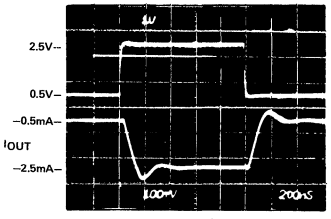


16-PIN DUAL-IN-LINE

PULSED REFERENCE OPERATION

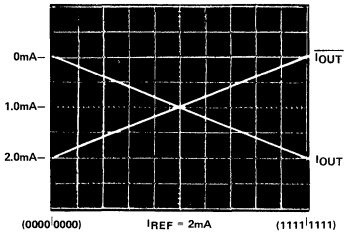


FAST PULSED REFERENCE OPERATION

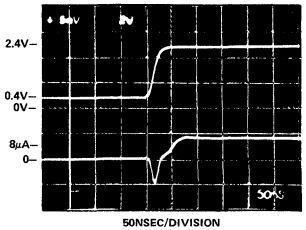


REQ ≈ 200Ω 200NSEC/DIVISION
RL = 100Ω
CC = 0

TRUE AND COMPLEMENTARY OUTPUT OPERATION



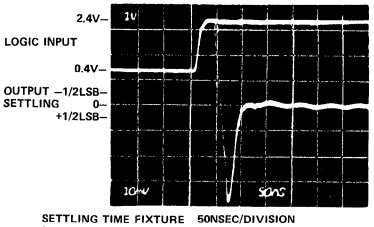
LSB SWITCHING



50NSEC/DIVISION

FULL SCALE SETTLING TIME

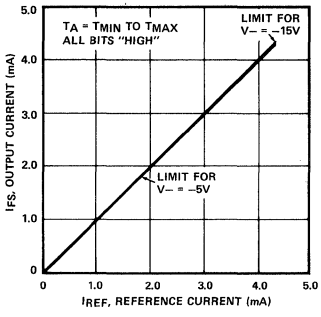
ALL BITS SWITCHED ON



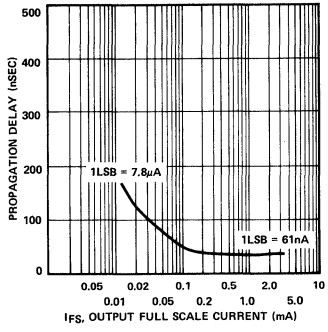
SETTLING TIME FIXTURE 50NSEC/DIVISION
IFS = 2mA, RL = 1kΩ
1/2LSB = 4μA

TYPICAL PERFORMANCE CURVES

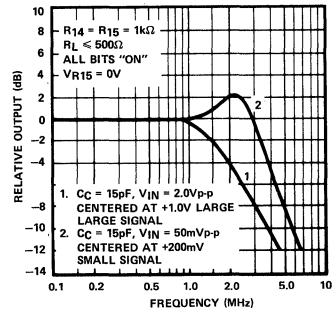
FULL SCALE CURRENT vs REFERENCE CURRENT



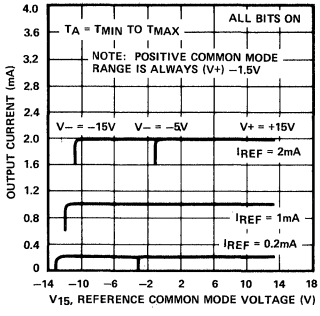
LSB PROPAGATION DELAY vs I_{FS}



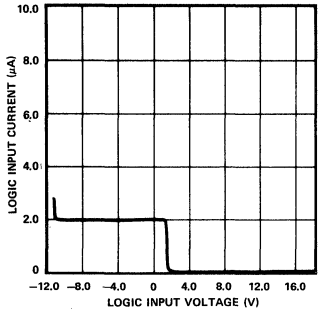
REFERENCE INPUT FREQUENCY RESPONSE



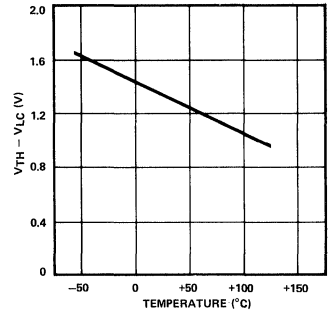
REFERENCE AMP COMMON MODE RANGE



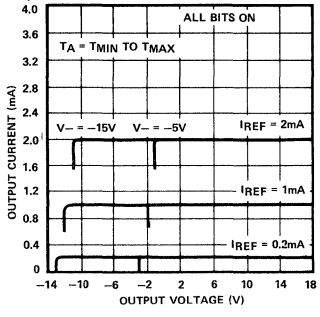
LOGIC INPUT CURRENT vs INPUT VOLTAGE



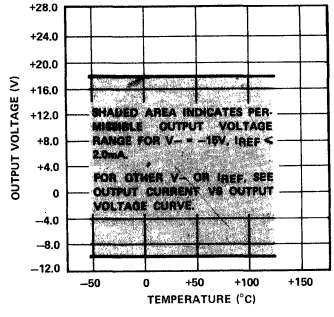
V_{TH} — V_{LC} vs TEMPERATURE



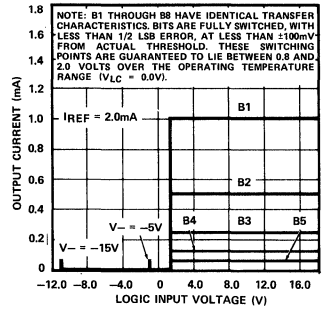
OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)



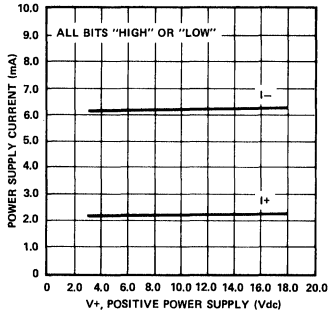
OUTPUT VOLTAGE COMPLIANCE vs TEMPERATURE

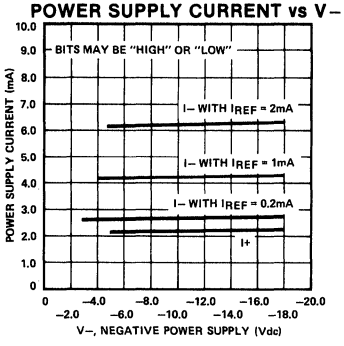


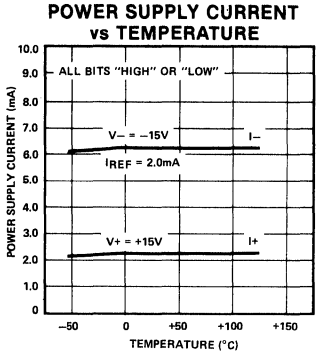
BIT TRANSFER CHARACTERISTICS



TYPICAL PERFORMANCE CURVES

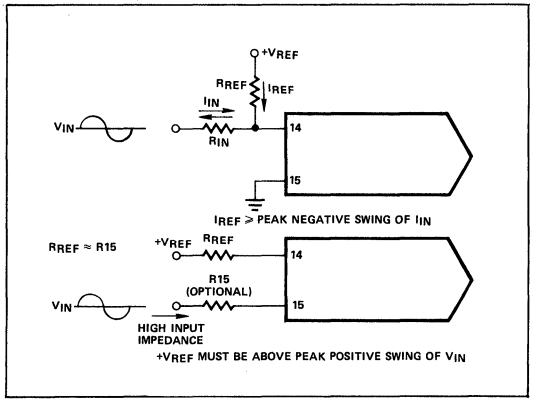




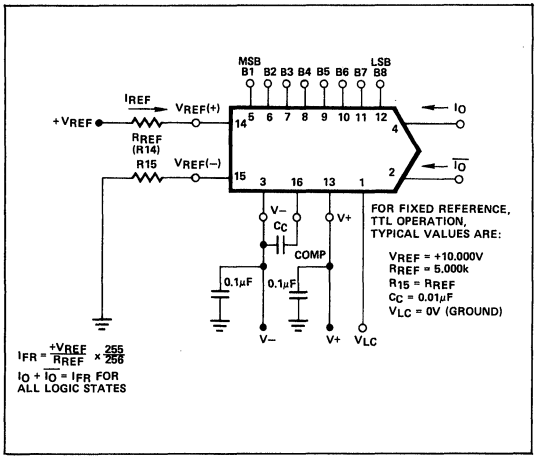


BASIC CONNECTIONS

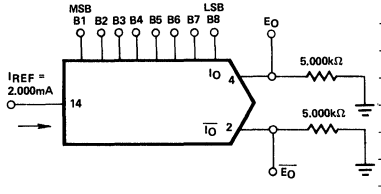
ACCOMODATING BIPOLAR REFERENCES



BASIC POSITIVE REFERENCE OPERATION



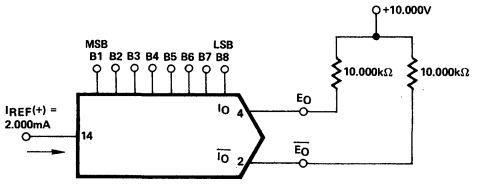
BASIC UNIPOLAR NEGATIVE OPERATION



	B1	B2	B3	B4	B5	B6	B7	B8	I_OmA	$I_{\overline{O}}$mA	E_O	$\overline{E_O}$
FULL RANGE	1	1	1	1	1	1	1	1	1.992	.000	–9.960	– .000
HALF SCALE +LSB	1	0	0	0	0	0	0	1	1.008	.984	–5.040	–4.920
HALF SCALE	1	0	0	0	0	0	0	0	1.000	.992	–5.000	–4.960
HALF SCALE –LSB	0	1	1	1	1	1	1	1	.992	1.000	–4.960	–5.000
ZERO SCALE +LSB	0	0	0	0	0	0	0	1	.008	1.984	– .040	–9.920
ZERO SCALE	0	0	0	0	0	0	0	0	.000	1.992	.000	–9.960

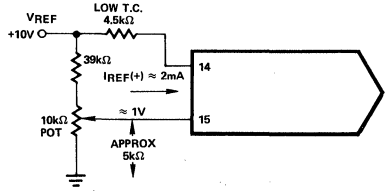
BASIC CONNECTIONS

BASIC BIPOLAR OUTPUT OPERATION

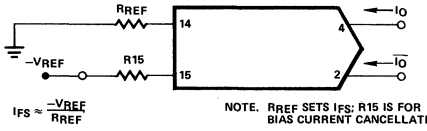


	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
POS FULL RANGE	1	1	1	1	1	1	1	1	−9.920	+10.000
POS FULL RANGE −LSB	1	1	1	1	1	1	1	0	−9.840	+ 9.920
ZERO SCALE +LSB	1	0	0	0	0	0	0	1	−0.080	+ 0.160
ZERO SCALE	1	0	0	0	0	0	0	0	0.000	+ 0.080
ZERO SCALE −LSB	0	1	1	1	1	1	1	1	+0.080	0.000
NEG FULL SCALE +LSB	0	0	0	0	0	0	0	1	+9.920	− 9.840
NEG FULL SCALE	0	0	0	0	0	0	0	0	+10.000	− 9.920

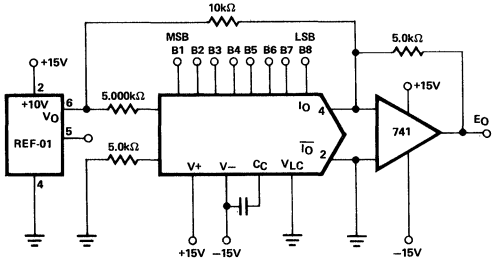
RECOMMENDED FULL SCALE ADJUSTMENT CIRCUIT



BASIC NEGATIVE REFERENCE OPERATION



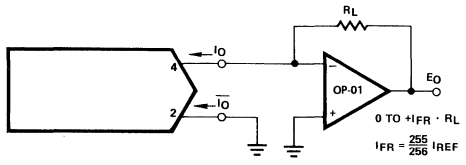
OFFSET BINARY OPERATION



	B1	B2	B3	B4	B5	B6	B7	B8	E_O
POS FULL RANGE	1	1	1	1	1	1	1	1	+4.960
ZERO SCALE	1	0	0	0	0	0	0	0	0.00
NEG FULL SCALE +1 LSB	0	0	0	0	0	0	0	1	−4.960
NEG FULL SCALE	0	0	0	0	0	0	0	0	−5.000

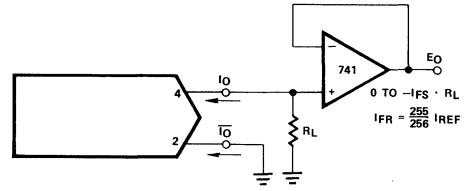
BASIC CONNECTIONS

POSITIVE LOW IMPEDANCE OUTPUT OPERATION



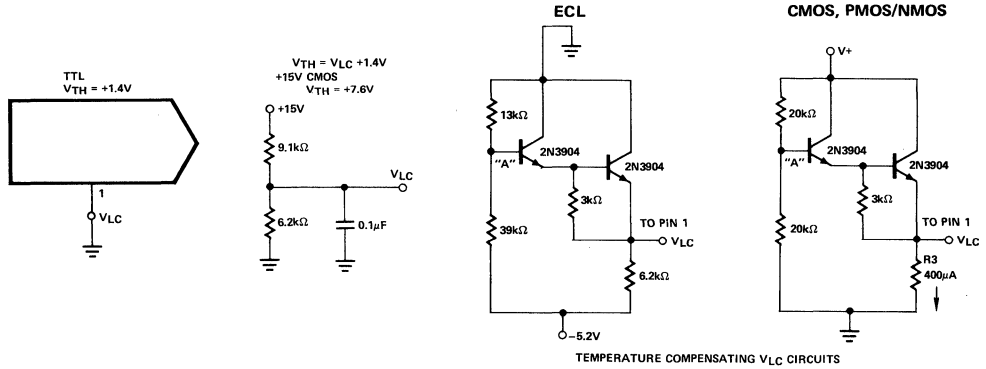
FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2); CONNECT I_O (PIN 4) TO GROUND.

NEGATIVE LOW IMPEDANCE OUTPUT OPERATION



FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT NON-INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2); CONNECT I_O (PIN 4) TO GROUND.

INTERFACING WITH VARIOUS LOGIC FAMILIES



TEMPERATURE COMPENSATING V_{LC} CIRCUITS

APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SETUP

The DAC-08 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full scale output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{255}{256} X\ I_{REF} \text{ where } I_{REF} = I_{14}.$$

In positive reference applications, an external positive reference voltage forces current through R_{14} into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15; reference current flows from ground through R_{14} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R_{15} (nominally equal to R_{14}) is used to cancel bias current errors; R_{15} may be eliminated with only a minor increase in error.

Bipolar references may be accomodated by offsetting V_{REF} or pin 15. The negative common mode range of the reference amplifier is given by: $V_{CM}- = V-$ plus (I_{REF} x 1kΩ) plus 2.5V. The positive common mode range is V+ less 1.5V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R_{14}, or by using a potentiometer for R_{14}. An improved method of full scale trimming which

eliminates potentiometer T.C. effects is shown in the recommended full scale adjustment circuit.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common mode range. The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifer to be compensated using a capacitor from pin 16 to V−. The value of this capacitor depends on the the impedance presented to pin 14: for R_{14} values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 15, 37, and 75pF. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R_{14} enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For $R_{14} = 1k\Omega$ and $C_C = 15pF$, the reference amplifier slews at 4mA/μs enabling a transition from $I_{REF} = 0$ to $I_{REF} = 2mA$ in 500ns.

Operation with pulse inputs to the reference amplifier may be accomodated by an alternate compensation scheme. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff ($I_{REF} = 0$) condition. Full scale transition (0 to 2mA) occurs in 120ns when the equivalent impedance at pin 14 is 200Ω and $C_C = 0$. This yields a reference slew rate of 16mA/μs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The DAC-08 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2μA logic input current and completely adjustable logic threshold voltage. For V− = −15V, the logic inputs may swing between −10V and +18V. This enables direct interface with +15V CMOS logic, even when the DAC-08 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V− plus (I_{REF} x 1kΩ) plus 2.5V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 1, V_{LC}). The appropriate graph shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC}. For TTL and DTL interface, simply ground pin 1. When interfacing ECL, an $I_{REF} = 1mA$ is recommended. For interfacing other logic families, see previous page. For general setup of the logic control circuit, it should be noted that pin 1 will source 100μA typical; external circuitry should be designed to accomodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1kΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \overline{I_O} = I_{FS}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases I_O as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V− and is independent of the positive supply. Negative compliance is given by V− plus (I_{REF} x 1kΩ) plus 2.5V.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC-08 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5V or less, $I_{REF} \leq 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifer negative common mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at −4.5V with $I_{REF} = 2mA$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be aplied to insure turn-on of the internal bias network.

Symetrical supplies are not required, as the DAC-08 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required: however, an artificial ground may be used to insure logic swings, etc. remain between acceptable limits.

Power consumption may be calculated as follows:

$P_d = (I+)(V+) + (I-)(V-) + (2\ I_{REF})(V-)$. A useful feature of the DAC-08 design is that supply current is constant and independent of input logic states; this is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-08 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is tight, typically ±10ppm/°C, with zero scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for minimum overall full scale drift. Settling times of the DAC-08 decrease approximately 10% at −55°C; at +125°C an increase of about 15% is typical.

The reference amplifier must be compensated by using a capacitor from pin 16 to V−. For fixed reference operation, a 0.01μF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifer Compensation for Multiplying Applications".

MULTIPLYING OPERATION

The DAC-08 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4mA to 4μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 4.0mA

SETTLING TIME

The DAC-08 is capable of extremely fast settling times, typically 85ns at I_{REF} = 2.0mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35ns for each of the 8 bits. Settling time to within 1/2 LSB of the LSB is therefore 35ns, with each progressively larger bit taking successively longer. The MSB settles in 85ns, thus determining the overall settling time of 85ns. Settling to 6-bit accuracy requires about 65 to 70ns. The output capacitance of the DAC-08 including the package is approximately 15pF, therefore the output RC time constant dominates settling time if $R_L > 500\Omega$.

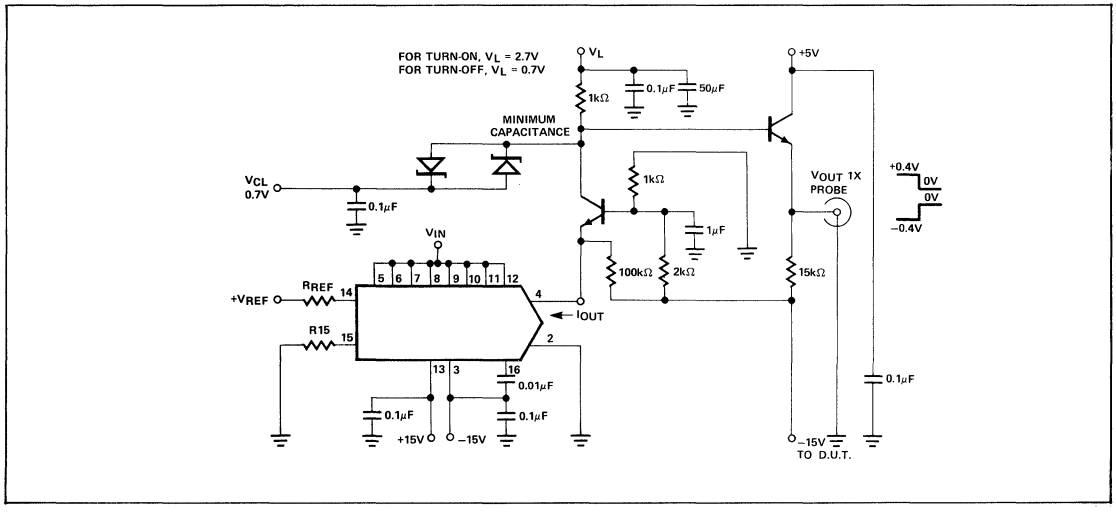
Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 1.0mA, with gradual increases for lower I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±4μA, therefore a 1kΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture shown in schematic labelled "Settling Time Measurement" uses a cascode design to permit driving a 1kΩ load with less than 5pF of parasitic capacitance at the measurement node. At I_{REF} values of less than 1.0mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value, and thus settling times may be observed at lower values of I_{REF}.

DAC-08 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1μF capacitors at the supply pins provide full transient protection.

SETTLING TIME MEASUREMENT



DAC-10

10-BIT HIGH SPEED MULTIPLYING D/A CONVERTER

UNIVERSAL DIGITAL LOGIC INTERFACE

FEATURES

- **Fast Settling 85ns**
- **Low Full Scale Drift ..... 10ppm/°C**
- **Nonlinearity to 0.05% Max Over Temp Range**
- **Differential Current Outputs ..... 0 to 4mA**
- **Wide Range Multiplying Capability ... 1MHz Bandwidth**
- **Wide Power Supply Range ... +5, −7.5 Min to ±18V Max**
- **Direct Interface to TTL, CMOS, ECL, PMOS, NMOS**

GENERAL DESCRIPTION

The DAC-10 series of 10-bit monolithic multiplying Digital-to-Analog Converters provide high-speed performance and full-scale accuracy.

Advanced circuit design achieves 85ns settling times with very low 'glitch' and low power consumption. Direct interface to all-popular logic families with full noise immunity is provided by the high-swing, adjustable threshold logic inputs.

All DAC-10 series models guarantee full 10-bit monotonicity, and nonlinearities as tight as ±0.05% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±18V power supply range, with 85mW power consumption attainable at lower supplies.

A highly stable, unique trim method is used, which selectively shorts zener diodes, to provide ½ LSB full scale accuracy without the need for laser trimming.

Single-chip reliability coupled with low cost and outstanding flexibility make the DAC-10 device an ideal building block for A/D converters, Data Acquisition systems, CRT display, programmable test equipment, and other applications where low power consumption, input/output versatility, and long-term stability are required.

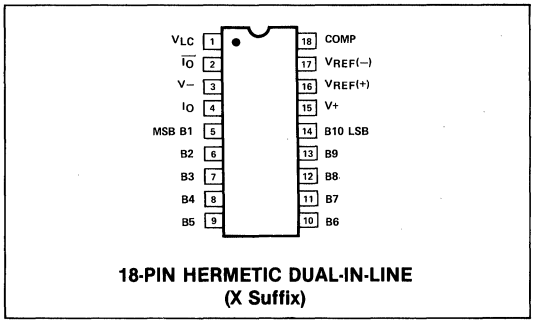
ORDERING INFORMATION†

I.N.L. L.S.B.	DUAL-IN-LINE PACKAGE 18 PIN HERMETIC	
	MILITARY TEMP.*	COMMERCIAL TEMP.
±1/2	DAC10BX*	DAC10FX
±1	DAC10CX*	DAC10GX

* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

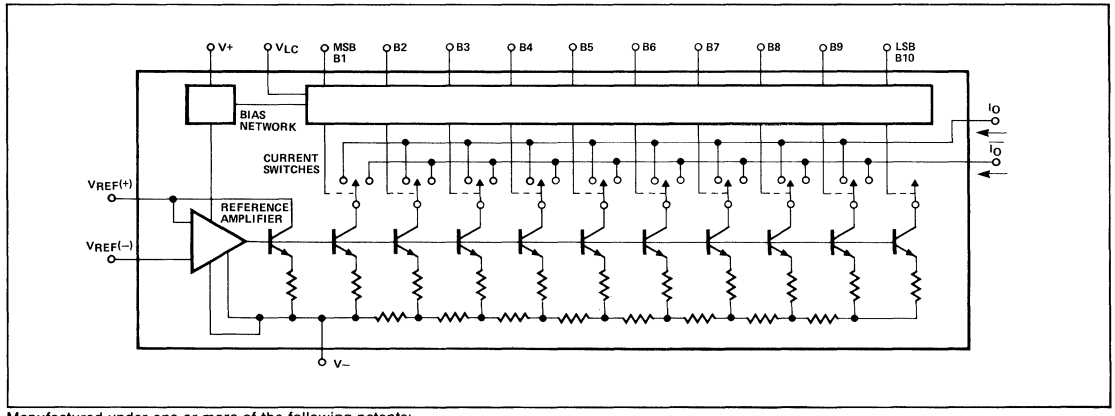
† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



18-PIN HERMETIC DUAL-IN-LINE (X Suffix)

SIMPLIFIED SCHEMATIC



Manufactured under one or more of the following patents:
4,055,770; 4,056,740; 4,092,639

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
- DAC-10BX, CX ..... −55°C to +125°C
- DAC-10FX, GX ..... 0°C to +70°C

DICE Junction Temperature (T_j) ..... −65°C to +150°C
Storage Temperature ..... −65°C to +150°C
Power Dissipation* 500mW
Derate above 100°C ..... 10mW/°C
Lead Soldering Temperature (60 sec.) ..... 300°C
V+ Supply to V− Supply 36V
Logic Inputs ..... V− to V− plus 36V
V_{LC} ..... V− to V+
Analog Current Outputs ..... +18 to −18V
Reference Inputs (V_{14} to V_{15}) ..... V− to V+
Reference Input Differential Voltage (V_{14} to V_{15}) ..... ±18V
Reference Input Current (I_{14}) 2.5mA

NOTE: Ratings apply to both packaged parts and DICE unless otherwise noted.
*Over full operating range

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$; $I_{REF} = 2.0mA$; $-55°C \le T_A \le 125°C$ for DAC-10B and DAC-10C, $0°C \le T_A \le 70°C$ for DAC-10F and G, unless otherwise noted. Output characteristics apply to both I_{OUT} and $\overline{I_{OUT}}$.

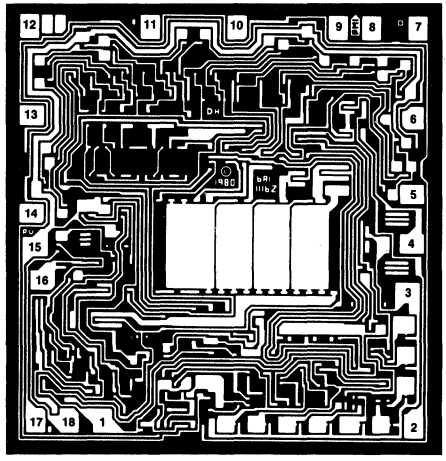
PARAMETER	SYMBOL	CONDITIONS	DAC-10B/F MIN	DAC-10B/F TYP	DAC-10B/F MAX	DAC-10C/G MIN	DAC-10C/G TYP	DAC-10C/G MAX	UNITS
Monotonicity			10	—	—	10	—	—	Bits
Nonlinearity	NL		—	0.3	0.5	—	0.6	1	LSB
Differential Nonlinearity	DNL		—	0.3	1.0	—	0.7	—	LSB
Settling Time	t_s	All Bits Switched ON or OFF Settle to 0.05% of FS (See Note)	—	85	135	—	85	150	ns
Output Capacitance	C_O		—	18	—	—	18	—	pF
Propagation Delay	t_{pLH} t_{pHL}	All Bits Switched $R_L = 5k\Omega$ $R_L = 0$	— —	50 50	— —	— —	50 50	— —	ns
Output Voltage Compliance	V_{OC}	Full Scale Current Change <1 LSB	— —	−5.5 +10	— —	— —	−5.5 +10	— —	V
Gain Tempco	TCI_{FS}	(See Note)	—	±10	±25	—	±10	±50	ppm/°C
Full Scale Symmetry	I_{FSS}	I_{FR}-$\overline{I_{FR}}$	—	0.1	4.0	—	0.1	4.0	μA
Zero Scale Current	I_{ZS}		—	0.01	0.5	—	0.01	0.5	μA
Full Scale Current	I_{FR}	(See Note)	3.968	3.996	4.024	3.936	3.996	4.056	mA
Reference Input Slew Rate	dI/dt		—	6	—	—	6	—	mA/μs
Reference Bias Current	I_B		—	−1	−3	—	−1	−3	nA
Power Supply Sensitivity	$FSSI_{FS}+$ $PSSI_{FS}-$	$4.5V \le V+ \le 18V$ $-18V \le V- \le -10V$	— —	0.001 0.0012	0.01 0.01	— —	0.001 0.0012	0.01 0.01	$\%\Delta I_{FS}/\%\Delta V$
Power Supply Current	I+ I− I+ I−	$V_S = +5V/-7.5V$; $I_{REF} = 1.0mA$	— — — —	2.3 9.0 1.8 5.9	4.0 15 4.0 9	— — — —	2.3 9.0 1.8 5.9	4.0 15 4.0 9	mA
Power Dissipation	P_d	$V_S = +5V/-7.5V$; $I_{REF} = 1.0mA$	— —	231 85	276 107	— —	231 85	276 107	mW
Logic Input Levels	V_{IL} V_{IH}	$V_{LC} = 0$	— 2.0	— —	0.8 —	— 2.0	— —	0.8 —	V
Logic Input Currents	I_{IL} I_{IH}	$V_{LC} = 0$; $-5V \le V_{IN} \le 0.8V$ $2.0V \le V_{IN} \le 18V$	−10 —	−5 0.001	— 10	−10 —	−5 0.001	— 10	μA

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$; $I_{REF} = 2.0mA$; $T_A = 25°C$, unless otherwise noted. Output characteristics apply to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-10B/C/F MIN	DAC-10B/C/F TYP	DAC-10B/C/F MAX	DAC-10G MIN	DAC-10G TYP	DAC-10G MAX	UNITS
Monotonicity			10	—	—	10	—	—	Bits
Nonlinearity	NL		—	0.3	0.5	—	0.6	1	LSB
Differential Nonlinearity	DNL		—	0.3	1.0	—	0.7	—	LSB
Output Voltage Compliance	V_{OC}	Full Scale Current Change <1 LSB	−5	−6/+18	+10	−5	−6/+15	+10	V
Full Scale Current	I_{FS}	$V_{REF} = 10.000V$, $R_{14} = R_{15} = 5.000k\Omega$	3.978	3.996	4.014	3.956	3.996	4.036	mA
Full Scale Symmetry	I_{FSS}	I_{FR}-$\overline{I_{FR}}$	—	0.1	4.0	—	0.1	4.0	μA
Zero Scale Current	I_{ZS}		—	0.01	0.5	—	0.01	0.5	μA

NOTE: Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.086 × 0.090 inch

1. V_{LC} (LOGIC) THRESHOLD CONTROL
2. $\overline{I_O}$
3. V−
4. I_O
5. B1 (MSB)
6. B2
7. B3
8. B4
9. B5
10. B6
11. B7
12. B8
13. B9
14. B10 (LSB)
15. V+
16. V_{REF} (+)
17. V_{REF} (−)
18. COMPENSATION

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 0.5mA$, and $T_A = 25°C$, unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

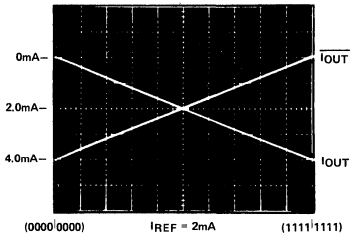
PARAMETER	SYMBOL	CONDITIONS	DAC-10-N LIMIT	DAC-10-G LIMIT	UNITS
Resolution			10	10	Bits MIN
Monotonicity			10	10	Bits MIN
Nonlinearity	NL		±0.5	±1.0	LSB MAX
Output Voltage Compliance	V_{OC}	True 1/2 LSB	+10.0 −5.0	+10.0 −5.0	V MAX V MIN
Output Current Range		I_{FS} ± 3.996 MA	± 18	± 40	μA MAX
Zero Scale Current	I_{ZS}	All Bits OFF	0.5	0.5	μA MAX
Logic Input "1"	V_{IH}	$I_{IN} = 100nA$	2.0	2.0	V MIN
Logic Input "0"	V_{IL}	V_{LC} @ Ground $I_{IN} = -100\mu A$	0.8	0.8	V MAX
Positive Supply Current	I+	V+ = 15V	14.0	14.0	mA MAX
Negative Supply Current	I−	V− = −15V	15.0	15.0	mA MAX

TYPICAL ELECTRICAL CHARACTERISTICS at V_S ± 15V and $I_{REF} = 0.5mA$, unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

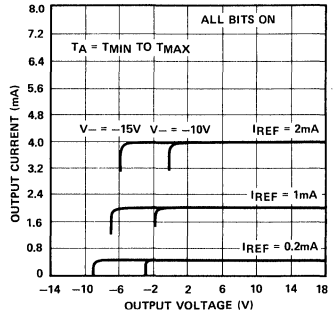
PARAMETER	SYMBOL	CONDITIONS	DAC-10-N TYP	DAC-10-G TYP	UNITS
Settling Time	t_S	To ±1/2 LSB When Output is Switched from 0 to FS	85	85	ns
Gain Temperature Coefficient (TC)		V_{REF} Tempco Excluded	±10	±10	ppm FS/°C
Output Capacitance			18	18	pF
Output Resistance			10	10	MΩ

TYPICAL PERFORMANCE CURVES

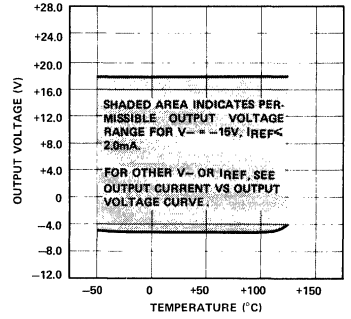
TRUE AND COMPLEMENTARY OUTPUT OPERATIONS



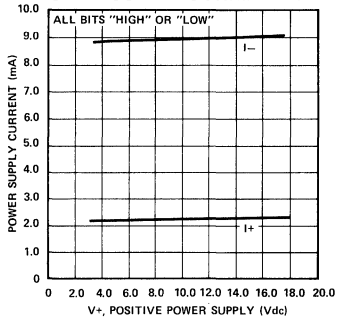
OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)



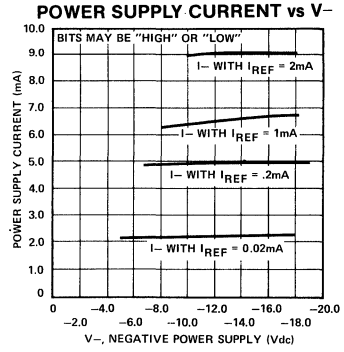
OUTPUT VOLTAGE COMPLIANCE vs TEMPERATURE



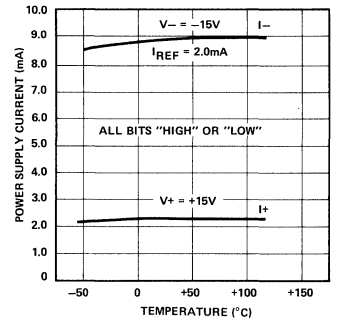
POWER SUPPLY CURRENT vs V+



POWER SUPPLY CURRENT vs V–

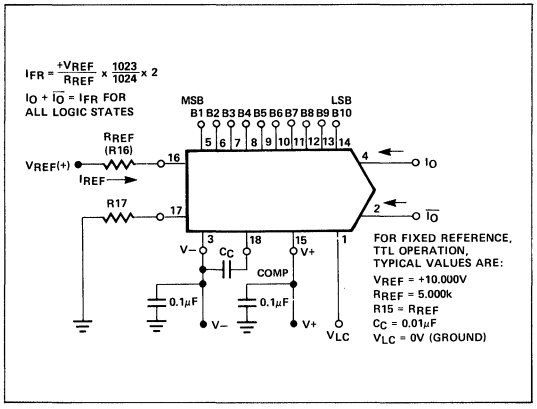


POWER SUPPLY CURRENT vs TEMPERATURE

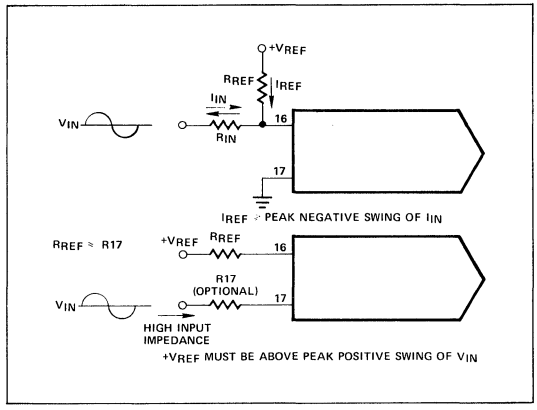


BASIC CONNECTIONS

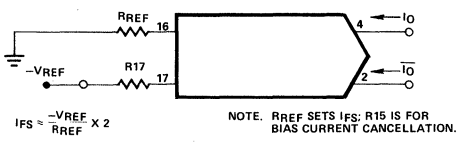
BASIC POSITIVE REFERENCE OPERATION



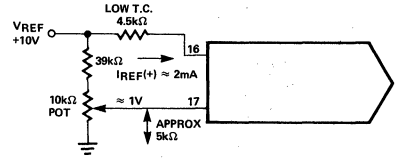
ACCOMMODATING BIPOLAR REFERENCES



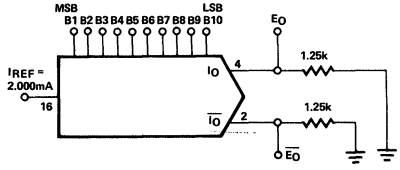
BASIC NEGATIVE REFERENCE OPERATION



RECOMMENDED FULL SCALE ADJUSTMENT CIRCUIT

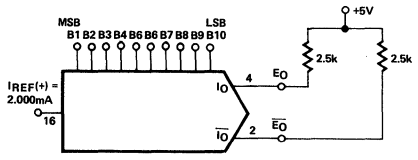


BASIC UNIPOLAR NEGATIVE OPERATION



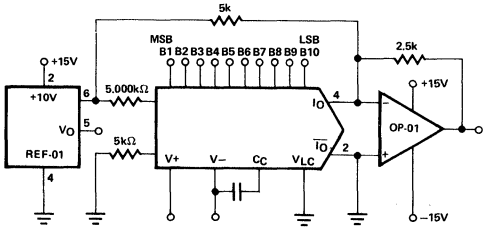
	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	I_OmA	$\overline{I_O}$mA	E_O	$\overline{E_O}$
FULL RANGE	1	1	1	1	1	1	1	1	1	1	3.996	0.000	−4.995	−0.000
HALF SCALE + LSB	1	0	0	0	0	0	0	0	0	1	2.004	1.992	−2.505	−2.490
HALF SCALE	1	0	0	0	0	0	0	0	0	0	2.000	1.996	−2.500	−2.495
HALF SCALE −LSB	0	1	1	1	1	1	1	1	1	1	1.996	2.000	−2.495	−2.500
ZERO SCALE +LSB	0	0	0	0	0	0	0	0	0	1	0.004	3.992	−0.005	−4.990
ZERO SCALE	0	0	0	0	0	0	0	0	0	0	0.000	3.996	−0.000	−4.995

BASIC BIPOLAR OUTPUT OPERATION



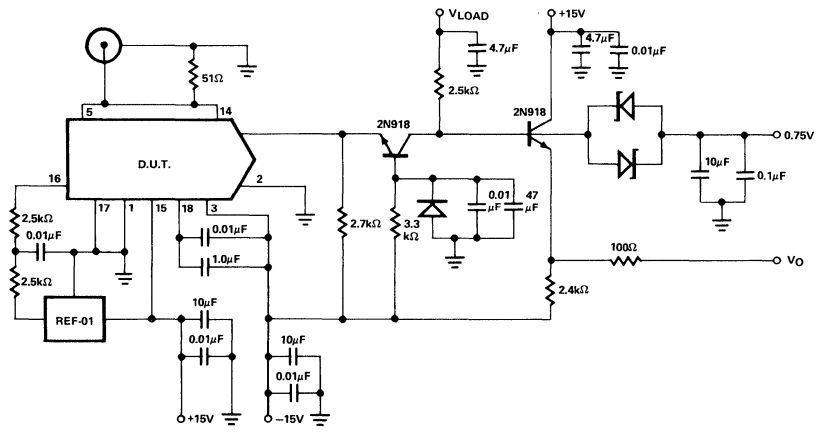
	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	E_O	$\overline{E_O}$
POS FULL RANGE	1	1	1	1	1	1	1	1	1	1	−4.990	+5.000
POS FULL RANGE −LSB	1	1	1	1	1	1	1	1	1	0	−4.980	+4.990
ZERO SCALE +LSB	1	0	0	0	0	0	0	0	0	1	−0.010	+0.020
ZERO SCALE	1	0	0	0	0	0	0	0	0	0	0.000	+0.010
ZERO SCALE −LSB	0	1	1	1	1	1	1	1	1	1	+0.010	0.000
NEG FULL SCALE +LSB	0	0	0	0	0	0	0	0	0	1	+4.990	−4.980
NEG FULL SCALE	0	0	0	0	0	0	0	0	0	0	+5.000	−4.990

OFFSET BINARY OPERATION

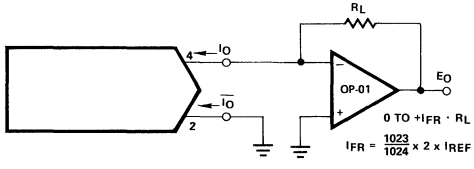


	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	E_O
POS FULL RANGE	1	1	1	1	1	1	1	1	1	1	+4.990
ZERO SCALE	1	0	0	0	0	0	0	0	0	0	0.00
NEG FULL SCALE +1 LSB	0	0	0	0	0	0	0	0	0	1	−4.990
NEG FULL SCALE	0	0	0	0	0	0	0	0	0	0	−5.000

SETTLING TIME MEASUREMENT

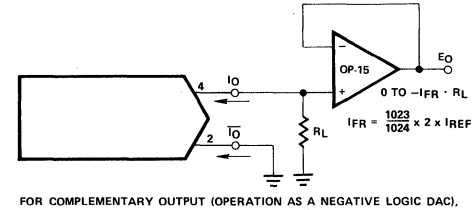


POSITIVE LOW IMPEDANCE OUTPUT OPERATION



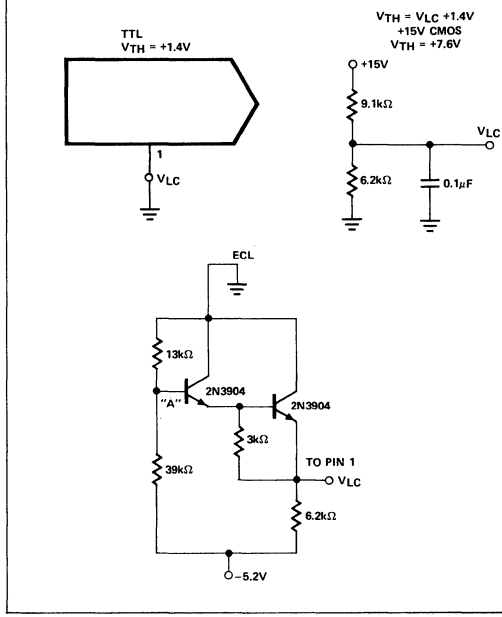
FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT INVERTING INPUT OF OP-AMP TO $\overline{IO}$ (PIN 2); CONNECT I_O (PIN 4) TO GROUND.

NEGATIVE LOW IMPEDANCE OUTPUT OPERATION

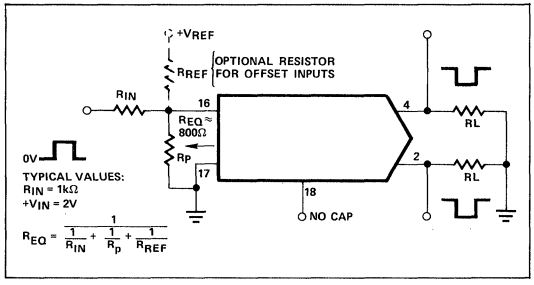


FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT NON-INVERTING INPUT OF OP-AMP TO $\overline{IO}$ (PIN 2); CONNECT I_O (PIN 4) TO GROUND.

INTERFACING WITH VARIOUS LOGIC FAMILIES



PULSED REFERENCE OPERATION



APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SETUP

The DAC-10 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full scale output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{1023}{1024} \times 2 \times (I_{REF}) \text{ where } I_{REF} = I_{16}$$

In positive reference applications, an external positive reference voltage forces current through R16 into the $V_{REF(+)}$ terminal (pin 16) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 17; reference current flows from ground through R16 into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 17. The voltage at pin 18 is equal to and tracks the voltage at pin 17 due to the high gain of the internal reference amplifier. R17 (nominally equal to R16) is used to cancel bias current errors; R17 may be eliminated with only a minor increase in error.

Bipolar references may be accomodated by offsetting V_{REF} or pin 17. The negative common mode range of the reference amplifier is given by: V_{CM^-} = V- plus (I_{REF} x 2kΩ) plus 2.V. The positive common mode range is V+ less 1.8V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R16 should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R16, or by using a potentiometer for R16. An improved method of full scale trimming which eliminates potentiometer T.C. effects is shown in the Recommended Full Scale Adjustment circuit.

The reference amplifier must be compensated by using a capacitor from pin 18 to V-. For fixed reference operation, a 0.01μF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications."

MULTIPLYING OPERATION

The DAC-10 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4mA to 4μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 4.0mA.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 18 to V-. The value of this capacitor depends on the impedance presented to pin 16 for R16 values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 15, 37, and 75pF. Larger values of R16 require proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R16 enabling small C_C values should be used. If pin 16 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R16 = 1 kΩ and C_C = 15pF, the reference amplifier slews at 4mA/μs enabling a transition from I_{REF} = 0 to I_{REF} = 2mA in 500ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full scale transition (0 to 2mA) occurs in 120ns when the equivalent impedance at pin 16 is 200Ω and C_C=0. This yields a reference slew rate of 16mA/μs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The DAC-10 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2μA logic input current and completely adjustable logic threshold voltage. For V- = −15V, the logic inputs may swing between −5 and +18V. This enables direct interface with +15V CMOS logic, even when the DAC-10 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V- plus (I_{REF}x2kΩ) plus 3V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 1, V_{LC}). The appropriate graph shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC}. For TTL interface, simply ground pin 1. When interfacing ECL, an I_{REF} = 1mA is recommended. For interfacing other logic families, see previous page. For general setup of the logic control circuit, it should be noted that pin 1 will sink 1. 1mA typical; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1kΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \overline{I_O} = I_{FS}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}; DO NOT LEAVE AN UNUSED OUTPUT PIN OPEN.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V– and is independent of the positive supply. Negative compliance is +10V above V–.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC-10 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating with V– supplies of –10V or less, $I_{REF} \leq 1$mA is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at –9V with $I_{REF} = 2$mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-10 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc. remain in between acceptable limits.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-10 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is tight, typically ±10ppm/°C, with zero scale output current and drift essentially negligible compared to ½ LSB.

The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full scale drift. Settling times of the DAC-10 decrease approximately 10% at –55°C; at +125°C an increase of about 15% is typical.

SETTLING TIME

The DAC-10 is capable of extremely fast settling times; typically 85ns at $I_{REF} = 2.0$mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35ns for each of the 10 bits. Settling time to within ½ LSB of the LSB is therefore 35ns, with each progressively larger bit taking successively longer. The MSB settles in 130ns, thus determining the overall settling time of 85ns. Settling to 8-bit accuracy requires about 60 to 78ns. The output capacitance of the DAC-10 including the package is approximately 18pF; therefore the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 1.0mA, with gradual increases for lower I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±2μA, therefore a 2.5KΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture of schematic titled "Settling Time Measurement" uses a cascode design to permit driving a 2.5kΩ load with less than 5pF of parasitic capacitance at the measurement node. At I_{REF} values of less than 1.0mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 0111111111 to 1000000000 provides an accurate indicator of settling time. This code changes does not require the normal 6.2 time constants to settle to within ±0.2% of the final value, and thus settling times may be observed at lower values of I_{REF}.

DAC-10 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1μF capacitors at the supply pins provide full transient protection.

DAC-20

2-DIGIT BCD HIGH-SPEED MULTIPLYING D/A CONVERTER

UNIVERSAL DIGITAL LOGIC INTERFACE

FEATURES

- **Fast Settling Output Current** **85ns**
- **Full Scale Current Prematched to ±1 LSB**
- **Direct Interface to TTL, CMOS, ECL, PMOS, NMOS**
- **Nonlinearity to ±1/4 LSB Maximum Over Temperature Range**
- **High Output Impedance and Compliance −10V to +18V**
- **Complementary Current Outputs**
- **Wide Range Multiplying Capability ... 1MHz Bandwidth**
- **Low FS Current Drift** ..... **±10ppm/°C**
- **Wide Power Supply Range** ..... **±4.5V to ±18V**
- **Low Power Consumption** ..... **37mW @ ±5V**
- **Low Cost**

GENERAL DESCRIPTION

The DAC-20 series of 2-digit BCD monolithic multiplying digital-to-analog converters provide very high-speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85ns settling times with very low "glitch" and at low power consumption. Monotonic multiplying performance is attained over a wide 40 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

Dual complementary current outputs with −10V to +18V voltage compliance enable resistive termination, a voltage output without an external op amp.

All DAC-20 series models guarantee full 2-digit monotonicity, and nonlinearities as tight as ±1/2 LSB over the entire operating temperature range are available. Nonlinearity is unchanged over the ±4.5V to ±18V power supply range, with 37mW power consumption attainable at ±5V supplies.

The compact size and low power consumption make the DAC-20 attractive for portable applications.

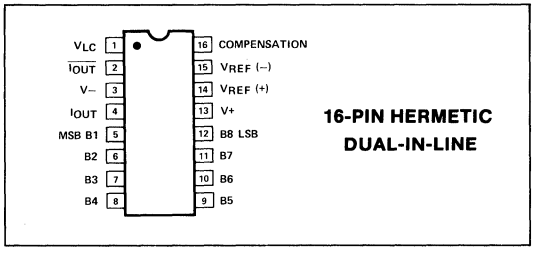
DAC-20 applications include A/D converters, audio attenuators, analog meter drivers, programmable power supplies, high-speed modems and other applications where low cost, high speed and complete input/output versatility are required.

ORDERING INFORMATION †

INL LSB	16 PIN DUAL INLINE PACKAGE COMMERCIAL TEMPERATURE RANGE	
	HERMETIC	PLASTIC
1/2	DAC20CQ	DAC20CP

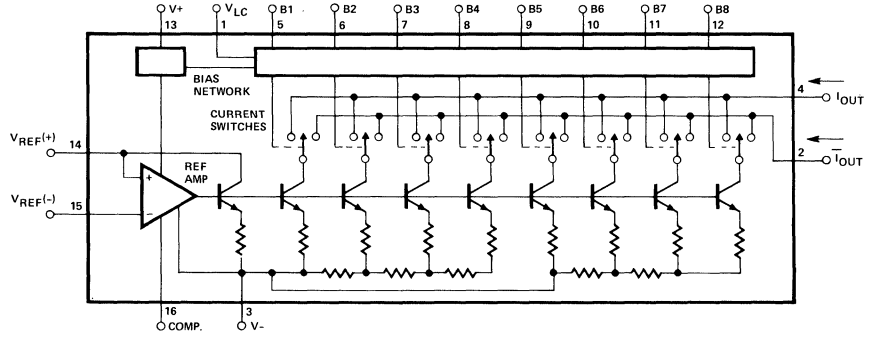
† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



16-PIN HERMETIC DUAL-IN-LINE

EQUIVALENT CIRCUIT



Manufactured under one or more of the following patents:
4,055,773; 4,056,740; 4,092,639

ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Operating Temperature Range
DAC-20 CQ, CP ..... 0°C to +70°C
DICE Junction Temperature (T_j) ..... −65°C to +150°C
Storage Temperature Range ..... −65°C to +150°C
Power Dissipation 500mW
Derate above 100°C ..... 10mW/°C
Lead Soldering Temperature (60 sec) ..... 300°C

V+ Supply to V− Supply 36V
Logic Inputs ..... V− to V− plus 36V
V_{LC} ..... V− to V+
Reference Inputs (V_{14}, V_{15}) ..... V− to V+
Reference Input Differential Voltage (V_{14} to V_{15}) .... ±18V
Reference Input Current (I_{14}) 5.0mA

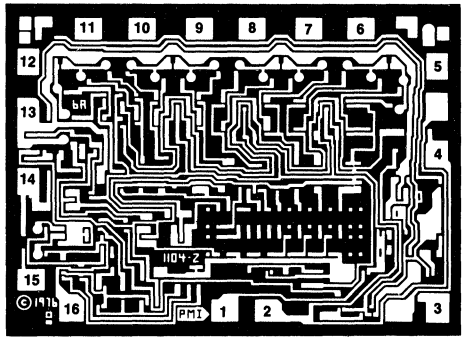
NOTE: Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $I_{REF} = 2.0mA$, $0°C \le T_A \le 70°C$, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-20C MIN	DAC-20C TYP	DAC-20C MAX	UNITS
Resolution		BCD 0 to 99 steps	2	2	2	Digits
Monotonicity		BCD 99 steps	2	2	2	Digits
Nonlinearity	NL	0000 0000 to 1001 1001	—	—	±1/2	LSB
Settling Time (Note 1)	t_S	To ±1/2 LSB (±0.5% FS) all bits switched ON or OFF, $T_A = 25°C$	—	85	150	ns
Propagation Delay Each Bit All bits switched (Note 1)	t_{PLH}, t_{PHL}	$T_A = 25°C$	—	35	60	ns
Full Tempco	TCI_{FS}	(Note 1)	—	±10	±80	ppm/°C
Output Voltage Compliance (True Compliance)	V_{OC}	Full scale current change < 1/2 LSB (< 0.5% FS) $R_{OUT} > 20M\Omega$ typical $I_{REF} = 1.0mA$	−10	—	+18	V
Full Range Output (Digital Input 1001 1001)	I_{FR4}	$T_A = 25°C$, $I_{REF} = 2mA$	1.92	1.98	2.04	mA
Zero Scale Current	I_{ZS}		—	0.2	5.0	μA
Output Current Range	I_{OR}	V− = −5.0V V− = −7.0V to −18V	2.2 4.2	2.0 2.0	— —	mA
Logic Input Levels Logic "0" Logic "1"	 V_{IL} V_{IH}	$V_{LC} = 0V$	 — 2.0	 — —	 0.8 —	V
Logic Input Current Logic "0" Logic "1"	 I_{IL} I_{IH}	$V_{LC} = 0V$ $V_{IN} = -10V$ to +0.8V $V_{IN} = 2.0V$ to 18V	 — —	 −2.0 0.002	 ±10 ±10	μA
Logic Input Swing	V_{IS}	V− = −15V	−10	—	+18	V
Logic Threshold Range	V_{THR}	$V_S = \pm15V$	−10	—	+13.5	V
Reference Bias Current	I_{15}		—	−1.0	−3.0	μA
Reference Input Slew Rate (Note 1)	dI/dt		4.0	8.0	—	mA/μs
Power Supply Sensitivity	$PSSI_{FS+}$ $PSSI_{FS-}$	V+ = 4.5V to 18V V− = −4.5V to −18V $I_{REF} = 1.0mA$	— —	±0.0003 ±0.002	±0.03 ±0.03	$\frac{\%\Delta I_{FS}}{\%\Delta V}$
Power Supply Current	I+ I− I+ I−	$V_S = \pm5V$, $I_{REF} = 1.0mA$ $V_S = \pm15V$, $I_{REF} = 2.0mA$ 	— — — —	2.3 −5.0 2.5 −7.8	3.8 −6.5 3.8 −9.1	mA
Power Dissipation	P_d	$V_S = \pm5V$, $I_{REF} = 1.0mA$ $V_S = \pm15V$, $I_{REF} = 2.0mA$	— —	37 152	52 194	mW

NOTE:
1. Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.085 × 0.065 inch

1. V_{LC}
2. I_{OUT}
3. V−
4. $\overline{I_{OUT}}$
5. BIT 1 (MSB)
6. BIT 2
7. BIT 3
8. BIT 4
9. BIT 5
10. BIT 6
11. BIT 7
12. BIT 8 (LSB)
13. V+
14. V_{REF} (+)
15. V_{REF} (−)
16. COMP

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 2.0mA$, and $T_A = 25°C$, unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

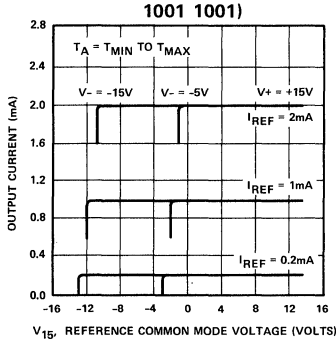
PARAMETER	SYMBOL	CONDITIONS	DAC-20-G LIMIT	UNITS
Resolution		BCD 0 to 99 Steps	2	Digits MIN
Monotonicity		BCD 99 Steps	2	Digits MIN
Nonlinearity	NL	FS = 1001 1001	±1/2	LSB MAX
Output Voltage Compliance	V_{OC}	Full Scale Current Change < 1/2 LSB	+18 −10	V MAX V MIN
Full Scale Current	I_{FS4}	$V_{REF} = 10.000V$ $R_{14}, R_{15} = 5.000k\Omega$	2.04 1.92	mA MAX mA MIN
Zero Scale Current	I_{ZS}		5.0	μA MAX
Output Current Range	I_{OR}	V− = −5.0V V− = −7.0V to −18V	2.1 4.2	mA MIN mA MIN
Logic "0" Input Level	V_{IL}		0.8	V MAX
Logic "1" Input Level	V_{IH}		2.0	V MIN
Logic Input Current Logic "0" Logic "1"	 I_{IL} I_{IH}	 $V_{IN} = -10V$ to +0.8V $V_{IN} = 2.0V$ to 18V	 ±10 ±10	 μA MAX
Logic Input Swing	V_{IS}	V− = −15V	+18 −10	V MAX V MIN
Power Supply Sensitivity	$PSSI_{FS+}$ $PSSI_{FS-}$	V+ = 4.5V to 18V V− = −4.5V to −18V $I_{REF} = 1.0mA$	±0.03 ±0.03	$\frac{\%\Delta I_{FS}}{\%\Delta V}$ MAX
Power Supply Current	I+ I−	$V_S = \pm 18V$ $I_{REF} \leq 2.0mA$	3.8 −7.8	mA MAX
Power Dissipation	P_d	$V_S = \pm 18V$ $I_{REF} \leq 2.0mA$	194	mW MAX

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and $I_{REF} = 2.0mA$, unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-20-G TYPICAL	UNITS
Reference Input Slew Rate	dI/dt		8.0	mA/μs
Propagation Delay	t_{PLH}, t_{PHL}	$T_A = 25°C$, Any Bit	35	ns
Settling Time	t_S	To ±1/2 LSB, All Bits Switched ON or OFF, $T_A = 25°C$	85	ns

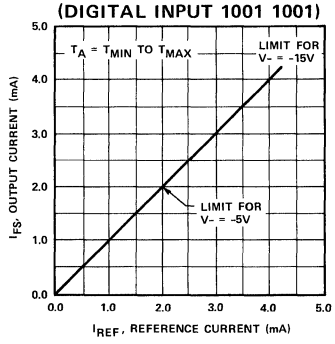
TYPICAL REFERENCE PERFORMANCE CURVES

REFERENCE AMP COMMON MODE RANGE (DIGITAL INPUT 1001 1001)



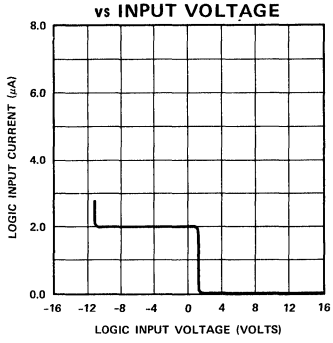
NOTE: POSITIVE COMMON MODE IS ALWAYS (V+) -1.5V; NEGATIVE COMMON MODE RANGE IS V- PLUS (I_{REF} x 800Ω) PLUS 2.5V.

FULL SCALE CURRENT vs REFERENCE CURRENT (DIGITAL INPUT 1001 1001)

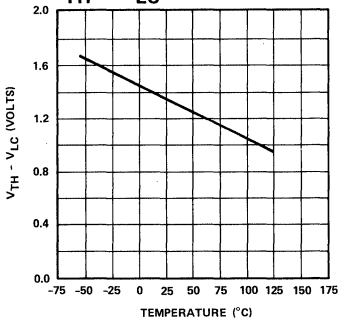


NOTE: THE RECOMMENDED RANGE FOR OPERATION WITH WITH A DC REFERENCE CURRENT IS +0.2mA TO +4.0mA.

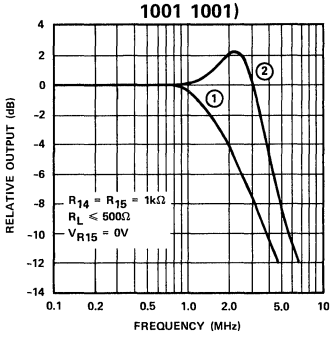
LOGIC INPUT CURRENT vs INPUT VOLTAGE



$V_{TH} - V_{LC}$ vs TEMPERATURE

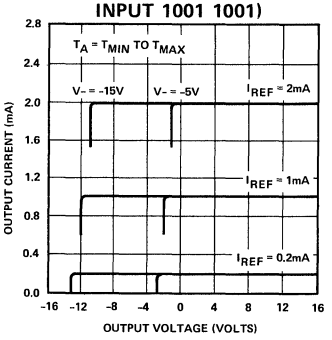


REFERENCE INPUT FREQUENCY RESPONSE (DIGITAL INPUT 1001 1001)

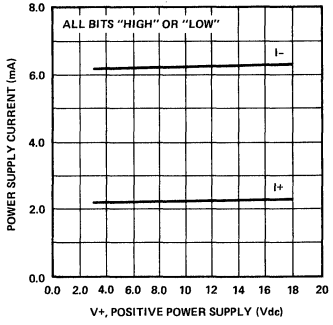


CURVE 1: C_C = 15pF, V_{IN} = $2.0V_{P-P}$ CENTERED AT +1.0V, LARGE SIGNAL.
CURVE 2: C_C = 15pF, V_{IN} = $50mV_{P-P}$ CENTERED AT +200mV, SMALL SIGNAL.

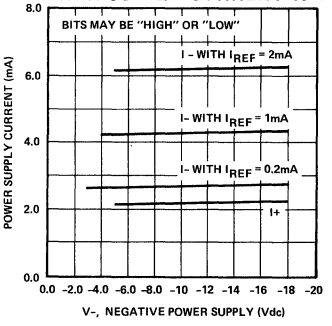
OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE) (DIGITAL INPUT 1001 1001)



POWER SUPPLY CURRENT vs V+

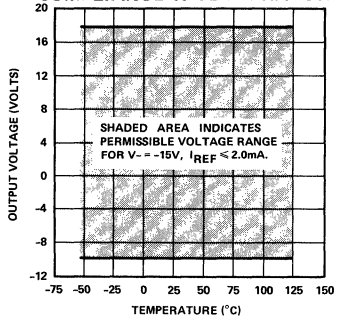


POWER SUPPLY CURRENT vs V–

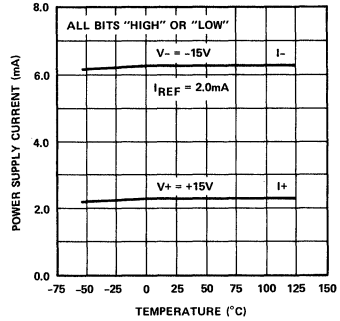


TYPICAL REFERENCE PERFORMANCE CURVES

OUTPUT VOLTAGE COMPLIANCE vs TEMPERATURE



POWER SUPPLY CURRENT vs TEMPERATURE



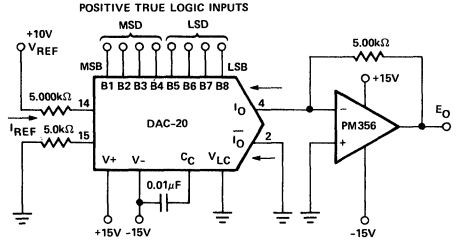
BASIC OUTPUT CONNECTIONS

With complementary current outputs, the DAC-20 may be used with either positive true or negative true (complementary) logic. Current appears at the "true" output (I_O) when a "1" is applied to a logic input. As the BCD-coded input increases, the sink current at Pin 4 increases proportionately, in the fashion of a "positive logic" D/A converter. When a "0" is applied to a logic input, that current is turned OFF at Pin 4 and ON at Pin 2 ($\overline{I_O}$) which is used for negative true or "negative logic" D/A converters.

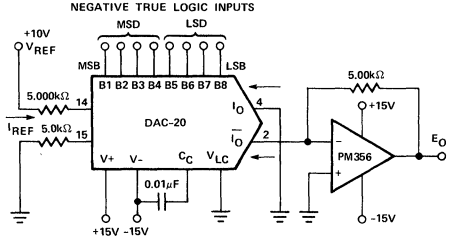
The unused output must be connected to ground or some voltage source capable of sourcing 1.65 times I_{REF}. A detailed discussion of reference input operation begins on the next page.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V− and is independent of the positive supply. Negative compliance is given by V− plus (I_{REF}X800Ω) plus 2.5V.

POSITIVE VOLTAGE OUTPUT

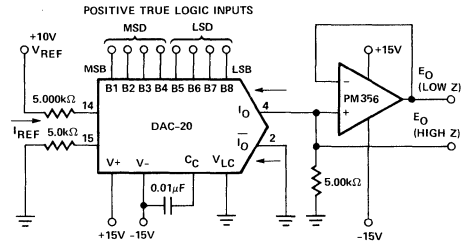


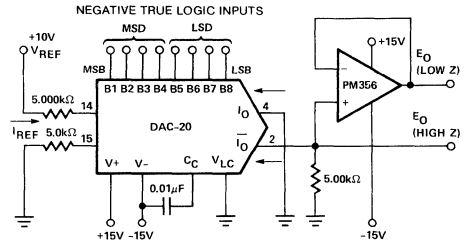
DECIMAL INPUT	BCD INPUT MSD	BCD INPUT LSD	I_O	E_O
0	0000	0000	0	0
10	0001	0000	0.20mA	+1.0V
20	0010	0000	0.40mA	+2.0V
30	0011	0000	0.60mA	+3.0V
40	0100	0000	0.80mA	+4.0V
80	1000	0000	1.60mA	+8.0V
99	1001	1001	1.98mA	+9.9V



DECIMAL INPUT	BCD INPUT MSD	BCD INPUT LSD	$\overline{I_O}$	E_O
0	1111	1111	0	0
10	1110	1111	0.20mA	+1.0V
20	1101	1111	0.40mA	+2.0V
30	1100	1111	0.60mA	+3.0V
40	1011	1111	0.80mA	+4.0V
80	0111	1111	1.60mA	+8.0V
99	0110	0110	1.98mA	+9.9V

NEGATIVE VOLTAGE OUTPUT



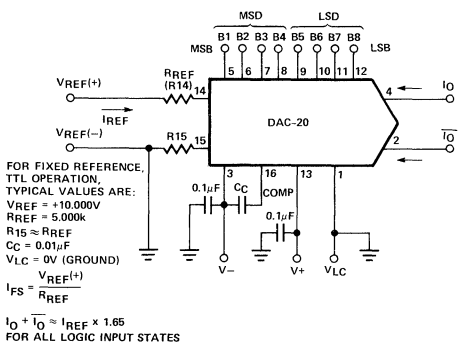


DECIMAL INPUT	BCD INPUT MSD	BCD INPUT LSD	I_O	E_O
0	0000	0000	0	0
10	0001	0000	0.20mA	−1.0V
20	0010	0000	0.40mA	−2.0V
30	0011	0000	0.60mA	−3.0V
40	0100	0000	0.80mA	−4.0V
80	1000	0000	1.60mA	−8.0V
99	1001	1001	1.98mA	−9.9V

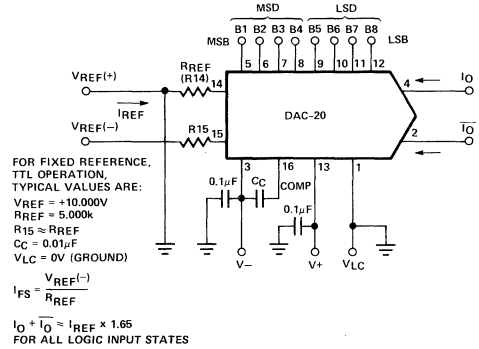
DECIMAL INPUT	BCD INPUT MSD	BCD INPUT LSD	$\overline{I_O}$	E_O
0	1111	1111	0	0
10	1110	1111	0.20mA	−1.0V
20	1101	1111	0.40mA	−2.0V
30	1100	1111	0.60mA	−3.0V
40	1011	1111	0.80mA	−4.0V
80	0111	1111	1.60mA	−8.0V
99	0110	0110	1.98mA	−9.9V

REFERENCE OPERATION

POSITIVE



NEGATIVE



REFERENCE AMPLIFIER SETUP

The DAC-20 is a multiplying converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full range output current is a linear function of the reference current and is given by:

$I_{FR} = 99/100 \times I_{REF}$, where $I_{REF} = I_{14}$.

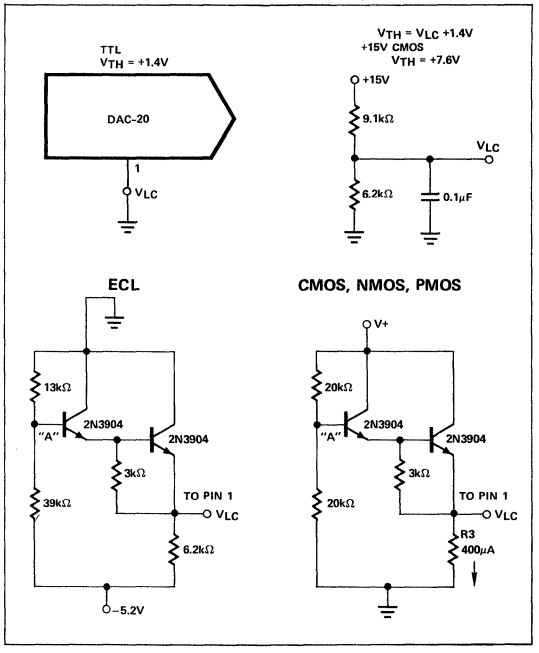
In positive reference applications an external positive reference voltage forces current through R_{14} into the $V_{REF}(+)$ terminal (Pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF}(-)$ at Pin 15; reference current flows from ground through R_{14} into $V_{REF}(+)$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at Pin 15. The voltage at Pin 14 is equal to and tracks the voltage at Pin 15 due to the high gain of the internal reference amplifier. R_{15} (nominally equal to R_{14}) is used to cancel bias current errors and may be eliminated with only a minor increase in error.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications the tight relationship between I_{REF} and I_{FR} will eliminate the need for trimming I_{REF}. If required, full-scale trimming may be accomplished by adjusting the value of R_{14}.

The reference amplifier must be compensated by using a capacitor from Pin 16 to V−. For fixed reference operation, a 0.01μF capacitor is recommended. For variable reference applications, see section entitled "Multiplying Operation."

LOGIC INPUT OPERATION AND INTERFACING



LOGIC THRESHOLD CONTROL

The DAC-20 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2μA logic input current and completely adjustable logic threshold voltage. For V− = −15V, the logic inputs may swing between −10V and +18V. This enables direct interface with a +15V CMOS logic, even when the DAC-20 is powered from a +5V supply. Minimum logic threshold voltage are given by: V− plus (I_{REF} X 800Ω) plus 2.5V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (Pin 1, V_{LC}).

The logic input threshold is 1.4V above V_{LC}. For TTL and DTL interface, simply ground Pin 1. When interfacing ECL, an I_{REF} = 1mA is recommended. For interfacing other logic families, see the figure above. Pin 1 will source 100μA typically, so the external circuitry must be designed to accommodate this current. Note that the threshold voltage has the temperature dependence of two forward biased diodes. The two V_{LC} setting circuits shown above include temperature compensation.

Fastest settling times are obtained when Pin 1 sees a low impedance. If Pin 1 is connected to a 1kΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

MULTIPLYING OPERATION

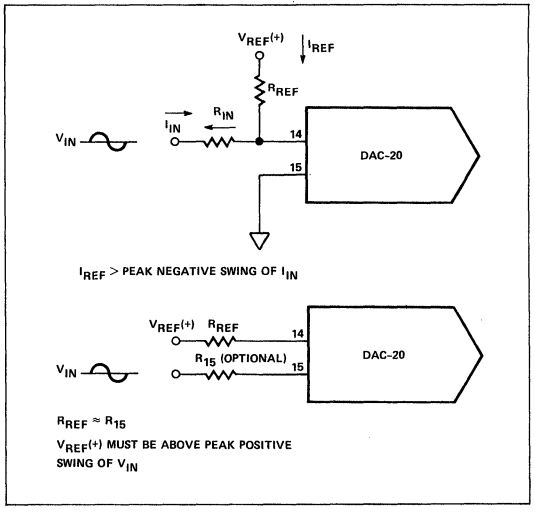
The DAC-20 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4mA to 4μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 4.0mA.

Bipolar references may be accommodated by offsetting V_{REF} or Pin 15. The negative common mode range of the reference amplifier is given by: V_{CM-} = V− plus (I_{REF} X 800Ω) plus 2.5V. The positive common mode range is V+ less 1.5V.

AC reference applications will require the reference amplifier to be compensated using a capacitor from Pin 16 to V−. The value of this capacitor depends on the impedance presented to Pin 14: for R_{14} values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 15, 37, and 75pF. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R_{14} enabling small C_C values should be used. If Pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{14} = 1kΩ and C_C = 15pF, the reference

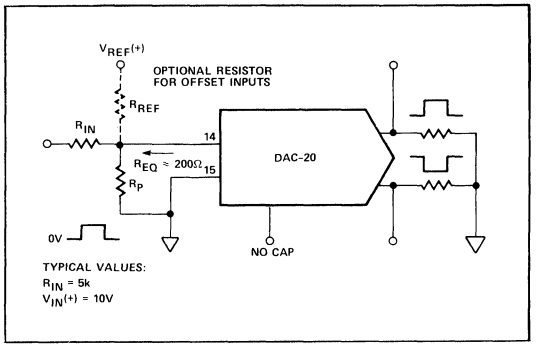
ACCOMMODATING BIPOLAR REFERENCES



amplifier slews at 4mA/μs enabling a transition from $I_{REF} = 0$ to $I_{REF} = 2mA$ in 500ns.

Operation with pulse inputs to the reference amplifier may be accommodated by the alternate compensation scheme shown above. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff ($I_{REF} = 0$) condition. Full-scale transition (0 to 2mA) occurs in 120ns when the equivalent impedance at Pin 14 is 200Ω and $C_C = 0$. This yields a reference slew rate of 16mA/μs which is relatively independent of R_{IN} and V_{IN} values.

PULSED REFERENCE OPERATION



POWER SUPPLY CONSIDERATIONS

The DAC-20 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5V or less, $I_{REF} \leq 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at −4.5V with $I_{REF} = 2mA$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible. However, at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-20 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required: however, an artificial ground may be useful to insure logic swings, etc., remain between acceptable limits.

Power consumption may be calculated as follows:
$P_d = (I+)(V+) + (I-)(V-) + (2\ I_{REF})(V-)$. A useful feature of the DAC-20 design is that supply current is constant and independent of input logic states; this reduces the size of the power supply bypass capacitors.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-20 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is tight, typically ±10ppm/°C, with zero-scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for minimum overall full-scale drift.

SETTLING TIME OPTIMIZATION

The DAC-20 is capable of extremely fast settling times, typically 85ns at $I_{REF} = 2.0mA$. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The output capacitance of the DAC-20 including the package is approximately 15pF, therefore the output RC time constant dominates settling time if $R_L > 500\Omega$.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1μF capacitors at the supply pins provide full transient protection.

DAC-76

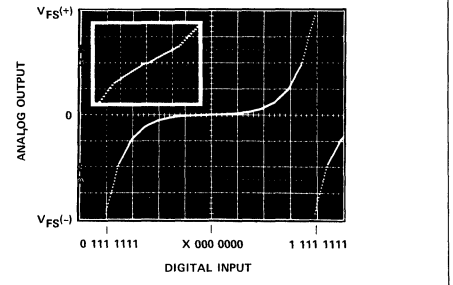
COMDAC® COMPANDING D/A CONVERTER

MONOLITHIC LOGARITHMIC DAC

FEATURES

- Sign Plus 12-Bit Range with Sign Plus 7-Bit Coding
- 12-Bit Accuracy and Resolution Around Zero
- Sign Plus 72dB Dynamic Range
- True Current Outputs: −5V to +18V Compliance
- Tight Full Scale Tolerance Eliminates Calibration
- Low Full Scale Drift Over Temperature
- Conforms with Bell System μ-255 Companding Law
- Multiplying Reference Inputs
- Low Power Consumption and Low Cost
- Ideal for PCM, Audio, and 8-Bit μP Applications
- Outputs Multiplexed for Time Shared Applications

COMDAC® TRANSFER CHARACTERISTIC



GENERAL DESCRIPTION

The DAC-76 monolithic COMDAC® D/A Converter provides the dynamic range of a sign + 12-bit DAC in a sign + 7-bit format. A companding (compression/expansion) transfer function is implemented by using three bits to select one of eight binarily-related chords (or segments) and four bits to select one of sixteen linearly-related steps within each chord. Accuracy is assured by specifying chord end point values, chord nonlinearity, and monotonicity over the full operating temperature range.

The 8-bit format with a sign + 72dB dynamic range is especially useful in control systems using 8-bit microprocessors, RAMs and ROMs. Low distortion multiplying capability and conformance with the Bell System μ-255 logarithmic law for PCM transmission make the DAC-76 ideal for use in audio applications. Other applications include servo controls, stress and vibration analysis, digital recording and speech synthesis. Additional applications are listed on the last page.

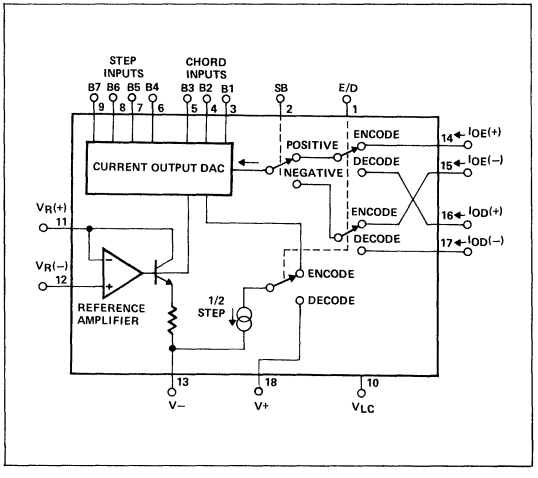
ORDERING INFORMATION†

	18 PIN DUAL IN LINE PACKAGE HERMETIC	
ACCURACY	MILITARY TEMPERATURE	COMMERCIAL TEMPERATURE
1/2 STEP	DAC76BX*	DAC76EX
1 STEP	DAC76X*	DAC76CX
1 1/2 STEP		DAC76DX

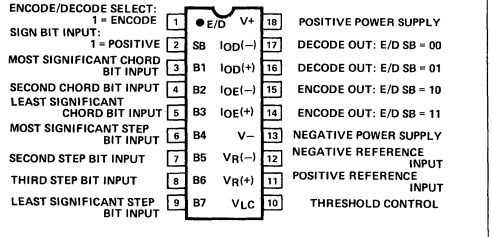
*Also available with MIL-STD-883B processing. To order add /883 as a suffix to the part number.

†All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

EQUIVALENT CIRCUIT



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

V+ Supply to V− Supply 36V
V_{LC} Swing ..... V− plus 8V to V+
Analog Current Outputs ..... V− plus 8V to V− plus 36V
Reference Inputs ..... V− to V+
Reference Input Differential Voltage ..... ±18V
Reference Input Current 1.25mA
Logic Inputs ..... V− plus 8V to V− plus 36V
Operating Temperature
DAC-76B, DAC-76 ..... −55°C to +125°C
DAC-76E, DAC-76C, DAC-76D ..... 0°C to +70°C

DICE Junction Temperature (T_j) ..... −65°C to +150°C
Storage Temperature ..... −65°C to +150°C
Power Dissipation 500mW
Derate above 100°C ..... 10mW/°C
Lead Soldering Temperature (60 sec.) ..... 300°C

NOTE: Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 528\mu A$ $-55°C \leq T_A \leq +125°C$ for DAC-76B and DAC-76, $0°C \leq T_A \leq +70°C$ for DAC-76E, C, D and for all 4 outputs, unless otherwise noted.

			DAC-76B/E			DAC-76/C			DAC-76D			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Resolution		8 chords with 16 steps each	±128	±128	±128	±128	±128	±128	±128	±128	±128	Steps
Dynamic Range		20 log ($I_{7,15}/I_{0,1}$)	72	72	72	72	72	72	72	72	72	dB
Monotonicity		Sign Bit + or −	128	—	—	128	—	—	128	—	—	Steps
Chord Endpoint Accuracy		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	—	—	±1/2	—	—	±1	—	—	±1-1/2	Step
Differential Step Nonlinearity		Step error within chord	—	—	±1/2	—	—	±1	—	—	±1-1/2	Step
Encode Current		Additional Output Encode/Decode = 1	3/8	1/2	5/8	1/4	1/2	3/4	1/4	1/2	3/4	Step
Settling Time	t_s	To within ±1/2 step	—	500	—	—	500	—	—	500	—	ns
Full Scale Drift	ΔI_{FS}	Full Temperature Range	—	±1/20	±1/4	—	±1/10	±1/2	—	±1/10	±1/2	Step
Output Voltage Compliance	V_{OC}	Full scale current change ≤1/2 step	−5	—	+18	−5	—	+18	−5	—	+18	V
Full Scale Current Deviation from Ideal (See Tables)	$I_{FS}(D)$ $I_{FS}(E)$	$V_{REF} = 10.000V$ $T_A = 25°C$ R11 = 18.94kΩ, R12 = 20kΩ	—	—	±1/2	—	—	±1	—	—	±1	Step
Full Scale Symmetry Error	$I_O(+)$ $-I_O(-)$	Decode or Encode Pair	—	±1/40	±1/8	—	±1/20	±1/4	—	±1/20	±1/2	Step
Zero Scale Current	I_{ZS}	Measured at $I_{OD}(+)$ or $I_{OD}(-)$ with 000 0000 Input	—	1/40	1/4	—	1/20	1/2	—	1/20	1/2	Step
Disable Current	I_{DIS}	Leakage of output disabled by E/D or SB	—	5.0	50	—	5.0	50	—	5.0	100	nA
Output Current Range	I_{OR}		0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	mA
Logic Input Levels Logic "0" Logic "1"	 V_{IL} V_{IH}	$V_{LC} = 0V$	 — 2.0	 — —	 0.8 —	 — 2.0	 — —	 0.8 —	 — 2.0	 — —	 0.8 —	V
Logic Input Current	I_{IN}	$V_{IN} = -5V$ to +18V	—	—	40	—	—	40	—	—	40	μA
Logic Input Swing	V_{IS}	V− = −15V	−5	—	+18	−5	—	+18	−5	—	+18	V

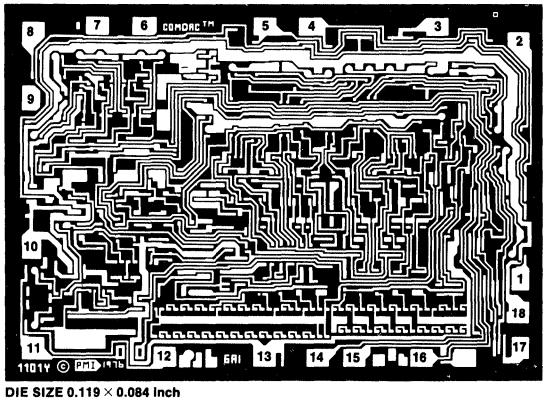
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 528\mu A$ $-55°C \leq T_A \leq +125°C$ for DAC76B and DAC76, $0°C \leq T_A \leq +70°C$ for DAC76E, C, D and for all 4 outputs, unless otherwise noted. **(CONTINUED)**

PARAMETER	SYMBOL	CONDITIONS	DAC-76B/E MIN	DAC-76B/E TYP	DAC-76B/E MAX	DAC-76/C MIN	DAC-76/C TYP	DAC-76/C MAX	DAC-76D MIN	DAC-76D TYP	DAC-76D MAX	UNITS
Reference Bias Current	I_{12}		—	−1.0	−4.0	—	−1.0	−4.0	—	−1.0	−6.0	μA
Reference Input Slew Rate	dI/dt		—	0.25	—	—	0.25	—	—	0.25	—	mA/μs
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	$PSSI_{FS+}$	V+ = 4.5 to 18V, V− = −15V	—	±1/20	±1/2	—	±1/20	±1/2	—	±1/20	±3/4	Step
	$PSSI_{FS-}$	V− = −10.8V to −18V, V+ = 15V	—	±1/10	±1/2	—	±1/10	±1/2	—	±1/0	±3/4	Step
Power Supply Current	I+	$V_S = +5V, -15V$, $I_{FS} = 2.0mA$	—	2.7	4.0	—	2.7	4.0	—	2.7	4.5	mA
	I−		—	−6.7	−8.8	—	−6.7	−8.8	—	−6.7	−9.3	mA
	I+	$V_S = \pm 15V$, $I_{FS} = 2.0mA$	—	2.7	4.0	—	2.7	4.0	—	2.7	4.5	mA
	I−		—	−6.7	−8.8	—	−6.7	−8.8	—	−6.7	−9.3	mA
Power Dissipation	P_d	$V_S = +5V, -15V$, $I_{FS} = 2.0mA$	—	114	152	—	114	152	—	114	167	mW
		$V_S = \pm 15V$, $I_{FS} = 2.0mA$	—	141	192	—	141	192	—	141	207	mW

NOTE:

1. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) step size is 0.5μA, while in the last chord near full scale (C_7) step size is 64μA.

DICE CHARACTERISTICS



DIE SIZE 0.119 × 0.084 inch

1. E/D
2. S.B.
3. BIT 1 (MSB)
4. BIT 2
5. BIT 3
6. BIT 4
7. BIT 5
8. BIT 6
9. BIT 7 (LSB)
10. V_{LC}
11. V_R (+)
12. V_R (−)
13. V−
14. I_{OE} (+)
15. I_{OE} (−)
16. I_{OD} (+)
17. I_{OD} (−)
18. V+

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$, $I_{REF} = 528\mu A$, $T_A = 25°C$, and all 4 outputs, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-76N (Note 1) LIMIT	DAC-76G (Note 2) LIMIT	UNITS
Resolution		8 chords with 16 steps each	±128	±128	Steps MIN
Dynamic Range		20 log ($I_{u,15}/I_{0,1}$)	72	72	dB MIN
Monotonicity		Sign Bit + or −	128	128	Steps MIN
Chord Endpoint Accuracy		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	±1	±1 1/2	Step MAX
Step Nonlinearity		Step error within chord	±	±1 1/2	Step MAX
Encode Current		Additional Output Encode/Decode = 1	1/4 3/4	1/4 3/4	Step MIN Step MAX
Output Voltage Compliance	V_{OC}	Full scale current change < 1/2 step	−5 +18	−5 +18	Volts MIN Volts MAX
Full Scale Current Deviation from Ideal (See Tables)	$I_{FS}(D)$ $I_{FS}(E)$	$V_{REF} = 10.000V$ $T_A = 25°C$ $R_{11} = 18.94k\Omega$ $R_{12} = 20k\Omega$	±1 ±1	±1 ±1	Step MAX Step MAX
Full Scale Symmetry Error	$I_O(+) - I_O(-)$	Decode or Encode Pair	±1/4	±1/2	Step MAX
Zero Scale Current	I_{ZS}	Measured at Selected Output with 000 0000 Input	1/2	1/2	Step MAX
Disable Current	I_{DIS}	Leakage of output disabled by E/D and SB	50	100	nA MAX
Output Current Range	I_{FSR}		0 42	0 42	mA MIN mA MAX
Logic Input Levels Logic "0" Logic "1"	 V_{IL} V_{IH}	 $V_{LC} = 0V$	 0.8 2.0	 0.8 2.0	 Volts MAX Volts MIN
Logic Input current	I_{IN}	$V_{IN} = -5V$ to $+18V$	40	40	μA MAX
Logic Input Swing	V_{IS}	V− = −15V	−5 +18	−5 +18	Volts MIN Volts MAX
Reference Bias Current	I_{12}		4.0	6.0	μA MAX
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	$PSSI_{FS+}$ $PSSI_{FS-}$	V+ = 4.5V to 18V, V− = −15V V− = −10.8V to −18V, V+ = 15V	±1/2 ±1/2	±3/4 ±3/4	Step MAX Step MAX
Power Supply Current	I+ I−	$V_S = +5V, -15V$, $I_{FS} = 2.0mA$	4.0 −8.8	4.5 −9.3	mA MAX mA MAX
Power Supply Current	I+ I−	$V_S = \pm 15V$, $I_{FS} = 2.0mA$	4.0 −8.8	4.5 −9.3	mA MAX mA MAX

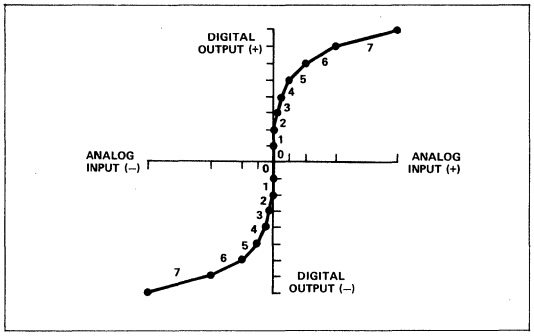
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-76N TYPICAL	DAC-76G TYPICAL	UNITS
Settling Time	t_S	To within ±1/2 Step	500	500	ns
Full Scale Drift	ΔI_{FS}	Full Temperature Range	±1/10	±1/10	Step
Reference Input Slew Rate	dI/dt		0.25	0.25	A/μs
Power Dissipation	P_D	$V_S = +5V, -15V$, $I_{FS} = 2.0mA$ $V_S = \pm 15V$, $I_{FS} = 2.0mA$	114 141	114 141	mW mW

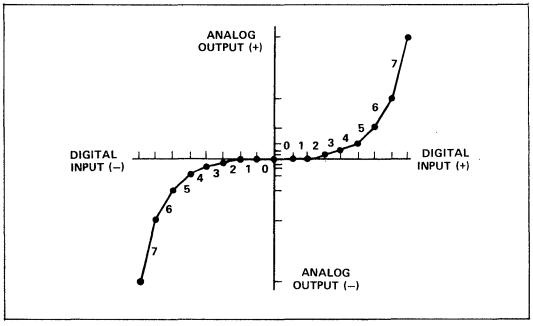
NOTES:
1. See DAC-76C for typical values.
2. See DAC-76D for typical values.

TRANSFER CHARACTERISTICS

ENCODE TRANSFER CHARACTERISTIC (A/D CONVERSION)



DECODE TRANSFER CHARACTERISTIC (D/A CONVERSION)



The system transfer characteristics above result when the DAC-76 is used for signal compression (A/D conversion) and for signal expansion (D/A conversion). As one would expect, when the curves are superimposed their average is a straight line because compression and expansion must be equal and opposite.

Both transfer characteristics show outputs divided into 8 chords in both polarities with 16 equal steps in each chord.

Note that each chord endpoint is approximately 6dB down from the next higher chord's endpoint and that the chord slopes are binarily-related.

The table below relates step size in each chord to other commonly-encountered measurements and to the equivalent, conventional, binary-coded DAC. Step size (except in Chord 0) is about 0.3dB and is an almost constant percentage of reading. In addition, there is a 1-1/2 step change between the maximum code in each chord and the minimum code in the next chord to smooth the chord transitions and to conform with existing telecommunication specifications.

The following three pages contain electrical specifications, the DC test circuit, tables of ideal chord endpoint currents for both encode and decode modes, and parameter definitions.

COMPANDING PRINCIPLES

BACKGROUND

Companding or signal compression and signal expansion is widely used. In FM broadcasting companding is performed by de-emphasis and pre-emphasis. In analog systems companding is performed by log and antilog amplifiers. But in data conversion and transmission, companding has been limited to the telecommunications industry. They recognized the need to efficiently represent analog signals with the fewest possible number of digital bits. With just 8 bits, the standard format of microprocessors, RAMs, ROMs and registers, telecommunications companding systems achieve very low signal-to-quantizing distortion over a 40dB range of speech amplitudes by using the Bell System μ-255 logarithmic companding law.

BELL μ-255 LOGARITHMIC CHARACTERISTIC

The output of the DAC-76 is an approximation to the μ-255 law which can be expressed as:

$$Y = 0.18 \ln (1 + \mu x)$$ where:

X = Normalized input signal level of the compressor (encoder), V_{IN}/V_{FS} with values from -1 to $+1$.

Y = Output signal level of the encoder

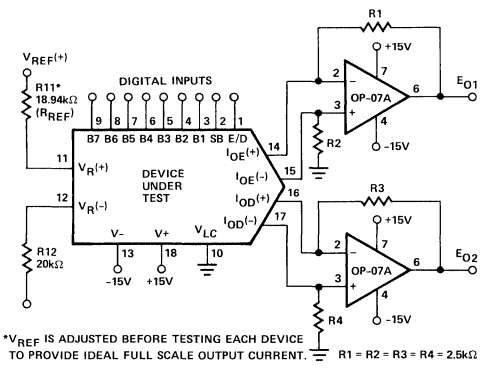
$\mu = 255$

This law is implemented by the DAC-76 with an eight chord (or segment) piecewise linear approximation for each polarity with sixteen linear steps in each chord. A dynamic range of 72dB in both polarities is achieved with 8-bit coding.

STEP SIZE SUMMARY TABLE DECODE OUTPUT (SIGN BIT EXCLUDED)

CHORD	STEP SIZE NORMALIZED TO FULL SCALE	STEP SIZE IN μA WITH 2007.75 μA F.S.	STEP SIZE AS A % OF FULL SCALE	STEP SIZE IN dB AT CHORD ENDPOINTS	STEP SIZE AS A % OF READING AT CHORD ENDPOINTS	RESOLUTION & ACCURACY OF EQUIVALENT BINARY DAC
0	2	0.5	0.025%	0.60	6.67%	SIGN + 12 BITS
1	4	1.0	0.05%	0.38	4.30%	SIGN + 11 BITS
2	8	2.0	0.1%	0.32	3.65%	SIGN + 10 BITS
3	16	4.0	0.2%	0.31	3.40%	SIGN + 9 BITS
4	32	8.0	0.4%	0.29	3.28%	SIGN + 8 BITS
5	64	16	0.8%	0.28	3.23%	SIGN + 7 BITS
6	128	32	1.6%	0.28	3.20%	SIGN + 6 BITS
7	256	64	3.2%	0.28	3.19%	SIGN + 5 BITS

OUTPUT CURRENT DC TEST CIRCUIT



LINE SELECTION TABLE

TEST GROUP	ENCODE/ DECODE	SIGN BIT	OUTPUT MEASUREMENT	
1	1	1	$I_{OE}(+)$	(E_{01}/R1)
2	1	0	$I_{OE}(-)$	(E_{01}/R2)
3	0	1	$I_{OD}(+)$	(E_{02}/R3)
4	0	0	$I_{OD}(-)$	(E_{02}/R4)

NOTE: Accuracy is specified in the test circuit using the tables below to be within the specified proportion of a step at the maximum value in each chord. Monotonic operation is guaranteed for all input codes.

CONDENSED CURRENT OUTPUT TABLES

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

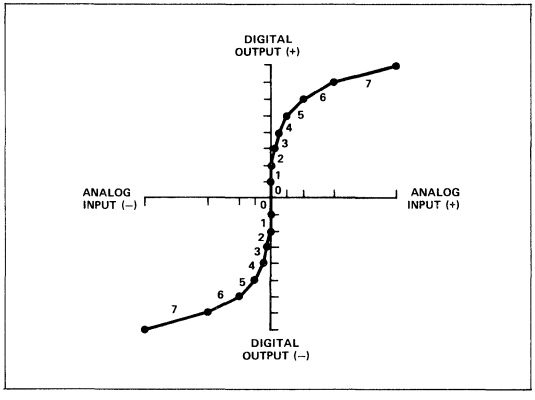
	CHORD	0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0	8.25	24.75	57.75	123.75	255.75	519.75	1047.75
15	1111	7.5	23.25	54.75	117.75	243.75	495.75	999.75	2007.75
STEP SIZE		0.50	1	2	4	8	16	32	64

IDEAL ENCODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

	CHORD	0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0.25	8.75	25.75	59.75	127.75	263.75	535.75	1079.75
15	1111	7.75	23.75	55.75	119.75	247.75	503.75	1015.75	2039.75
STEP SIZE		0.50	1	2	4	8	16	32	64

BASIC ENCODE OPERATION (COMPRESSING A/D CONVERSION)

ENCODE TRANSFER CHARACTERISTIC (A/D CONVERSION)



ENCODE DECISION LEVELS

Compressing A/D conversion with the DAC-76 requires a comparator, an exclusive-OR gate, and a successive approximation register — the usual elements in any sign-plus-magnitude A/D converter. However, a compressing ADC has one signficant difference from regular A/D converters.

In a conventional (linear) converter, the step size is a constant percentage of full scale, but in a compressing A/D converter, the step size increases as the output changes from zero scale to full scale. The standard 1/2 sfep bias used in conventional ADCs to keep quantizing error below ±1/2 step cannot be easily furnished by the user of a compressing ADC. For this reason, the DAC has a 1/2 step greater output in the encode mode that it has in the decode mode. This may be seen clearly by comparing the normalized encode and decode output tables at any code point.

ENCODING SEQUENCE

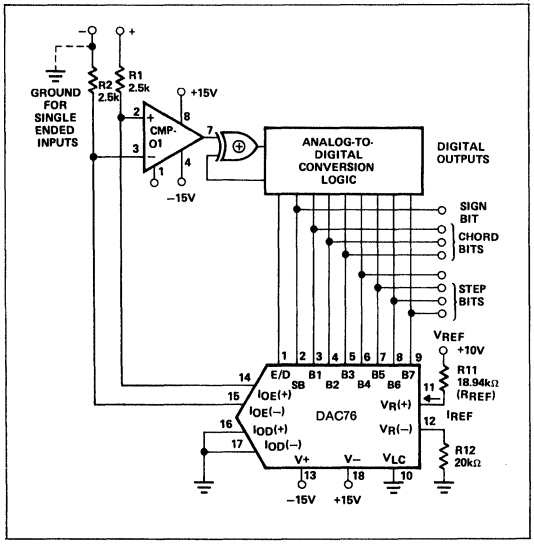
An encoding sequence begins with the Sign Bit comparison and decision. During this time the comparator is a polarity

NORMALIZED ENCODE LEVEL (SIGN BIT EXCLUDED) $I_{C,S} = 2[2^C (S + 17) - 16.5]$

C = chord no. (0 through 7)
S = step no. (0 through 15)

STEP	CHORD	0 000	1 001	2 010	3 011	4 100	5 101	6 110	7 111
0	0000	1	35	103	239	511	1055	2143	4319
1	0001	3	39	111	255	543	1119	2271	4575
2	0010	5	43	119	271	575	1183	2399	4831
3	0011	7	47	127	287	607	1247	2527	5087
4	0100	9	51	135	303	639	1311	2655	5343
5	0101	11	55	143	319	671	1375	2783	5599
6	0110	13	59	151	335	703	1439	2911	5855
7	0111	15	63	159	351	735	1503	3039	6111
8	1000	17	67	167	367	767	1567	3167	6367
9	1001	19	71	175	383	799	1631	3295	6623
10	1010	21	75	183	399	831	1695	3423	6879
11	1011	23	79	191	415	863	1759	3551	7135
12	1100	25	83	199	431	895	1823	3679	7391
13	1101	27	87	207	447	927	1887	3807	7647
14	1110	29	91	215	463	959	1951	3935	7903
15	1111	31	95	223	479	991	2015	4063	8159
STEP SIZE		2	4	8	16	32	64	128	256

BASIC ENCODE CONNECTIONS



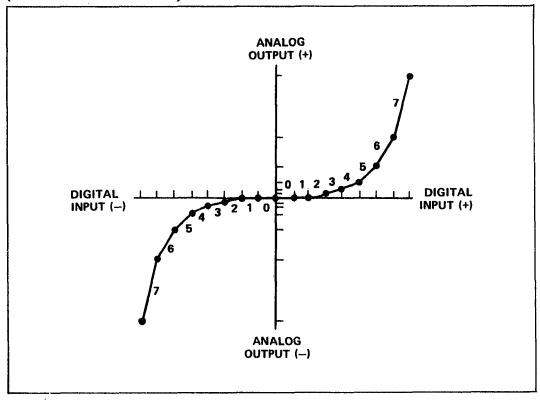
detector only. The Encode/Decode (E/D) input is held at a logic "0". Therefore, no current flows into the encode outputs, and the comparator is effectively disconnected from the DAC. Once the input polarity has been determined, the E/D input is changed to a logic "1" allowing current to flow into $I_{OE}(+)$ or $I_{OE}(-)$ depending upon the Sign Bit Answer.

For positive inputs, current flows into $I_{OE}(+)$ through R1, and the comparator's output will be entered as the answer for each successive decision. For negative inputs, current flows into $I_{OE}(-)$ through R2 developing a negative voltage which is compared with the analog input. An exclusive-OR gate inverts the comparator's output during negative trials to maintain the proper logic coding, all ones for full scale and all zeros for zero scale. (A more complete schematic is shown in the applications section).

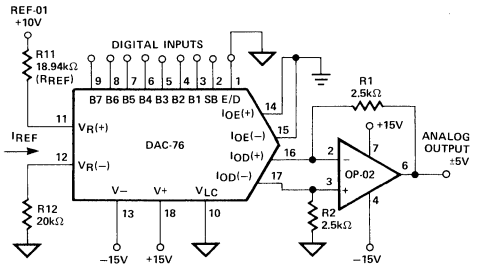
The bits are converted with a successive removal technique, starting with a decision at the code 011 1111 and turning off bits sequentially until all decisions have been made. Successive removal is necessary because the 1/2 step encode decision level current is drawn from the sum node, rather than sourced into it.

BASIC DECODE OPERATION (EXPANDING D/A CONVERSION)

DECODE TRANSFER CHARACTERISTIC (D/A CONVERSION)



BASIC DECODE CONNECTIONS



	E/D	SB	B1	B2	B3	B4	B5	B6	B7	E_0
POS FULL SCALE	0	1	1	1	1	1	1	1	1	5.019V
(+) ZERO SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.0012
(+) ZERO SCALE	0	1	0	0	0	0	0	0	0	0V
(−) ZERO SCALE	0	0	0	0	0	0	0	0	0	0V
(−) ZERO SCALE +1 STEP	0	0	0	0	0	0	0	0	1	−0.0012
NEG FULL SCALE	0	0	1	1	1	1	1	1	1	−5.019V

DECODE OPERATION

D/A conversion with the DAC-76 may be illustrated by using an operational amplifier connected to the decode outputs as a balanced load. The decode mode of operation is selected by applying a logic "0" to the Encode/Decode input. This enables the I_{OD} outputs, disables the I_{OE} outputs, and allows $I_{OD}(+)$ or $I_{OD}(-)$ to be selected by the Sign Bit input. When the Sign Bit input is high, a logic "1", all of the output current flows into $I_{OD}(+)$ forcing a positive voltage at the operational amplifier's output. When the Sign Bit input is low, a logic "0", all of the output current flows into $I_{OD}(-)$ through R2 forcing a negative voltage output. Since the Sign Bit only steers current into $I_{OD}(+)$ or $I_{OD}(-)$, the output will always be symmetrical, limited only by the matching of R1 and R2.

NORMALIZED TABLES

The encode and decode tables may be used to calculate ideal output current at any code point. For example, in decode mode at $I_{3,7}$ (011 0111) find 343. 343/8031 times I_{FS} of 2007.75μA equals 85.75μA. Alternatively, use the condensed current tables and add up the number of steps.

BASIC REFERENCE CONSIDERATIONS

Full scale output current is ideally 2007.75μA when the reference current is 528μA in the decode mode. In the encode mode it is 2039.75μA because the additional 1/2 step adds 32μA to the output. A percentage change in I_{REF} caused by changes in V_{REF} or R_{REF} will produce the same percentage change in output current.

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D/A CONVERTERS DAC-76

NORMALIZED DECODE OUTPUT (SIGN BIT EXCLUDED) $I_{C,S} = 2[2^C (S + 16.5) - 16.5]$

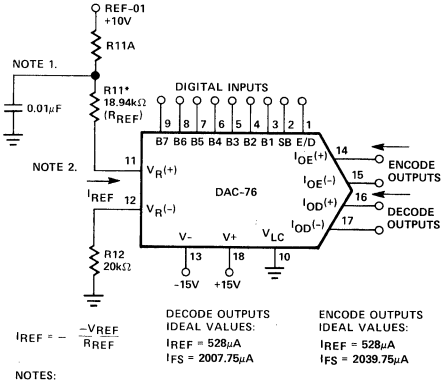
C = chord no. (0 through 7)
S = step no. (0 through 15)

STEP	CHORD	0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	33	99	231	495	1023	2079	4191
1	0001	2	37	107	247	527	1087	2207	4447
2	0010	4	41	115	263	559	1151	2335	4703
3	0011	6	45	123	279	591	1215	2463	4959
4	0100	8	49	131	295	623	1279	2591	5215
5	0101	10	53	139	311	655	1343	2719	5471
6	0110	12	57	147	327	687	1407	2847	5727
7	0111	14	61	155	343	719	1471	2975	5983
8	1000	16	65	163	359	751	1535	3103	6239
9	1001	18	69	171	375	783	1599	3231	6495
10	1010	20	73	179	391	815	1663	3359	6751
11	1011	22	77	187	407	847	1727	3487	7007
12	1100	24	81	195	423	879	1791	3615	7263
13	1101	26	85	203	439	911	1855	3743	7519
14	1110	28	89	211	455	943	1919	3871	7775
15	1111	30	93	219	471	975	1983	3999	8031
STEP SIZE		2	4	8	16	32	64	128	256

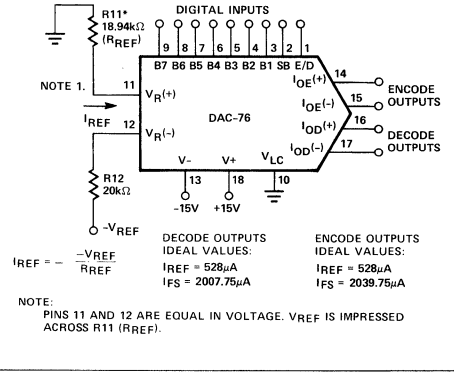
The large step size at full scale allows the use of inexpensive references in many applications. In some situations V_{REF} may even be the positive power supply. For example, with V+ = 15V, R_{REF} = 15V/528μA or 28.4kΩ. When using a power supply as a reference, R11 should be two resistors, R11A and R11B, and the junction should be bypassed to ground to provide decoupling.

REFERENCE AMPLIFIER OPERATION

POSITIVE REFERENCE OPERATION



NEGATIVE REFERENCE OPERATION



REFERENCE AMPLIFIER SETUP

The DAC-76 is a multiplying D/A converter in which the output current is the product of the normalized digital input and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full scale output current is a linear function of the reference current and is given for all four outputs in the figures above.

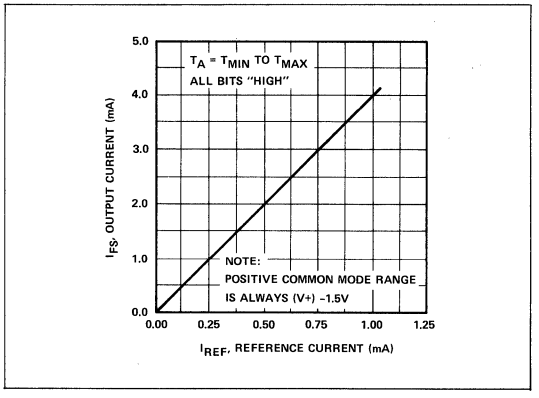
In positive reference applications an external positive reference voltage forces current through R11 into the $V_R(+)$ terminal (Pin 11) of the reference amplifier. Alternatively, a negative reference may be applied to $V_R(-)$ at Pin 12; reference current flows from ground through R11 into $V_R(+)$, as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at Pin 12. The voltage at Pin 11 is equal to and tracks the voltage at Pin 12 due to the high gain of the internal reference amplifier. R12 (nominally equal to R11) is used to cancel bias current errors and may be eliminated with only a minor increase in error.

REFERENCE RECOMMENDATIONS

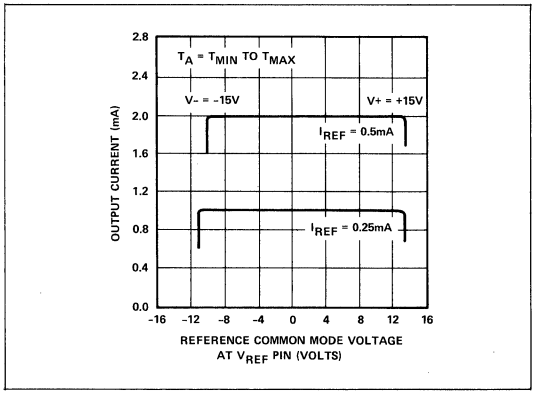
For most applications a +10.0V reference, such as the PMI REF-01, is recommended for optimum full scale temperature coefficient performance. (This also minimizes the contributions of reference amplifier V_{OS} and TCV_{OS}.) For most

TYPICAL PERFORMANCE CURVES

OUTPUT FULL SCALE CURRENT vs REFERENCE INPUT CURRENT



REFERENCE AMPLIFIER INPUT COMMON MODE RANGE

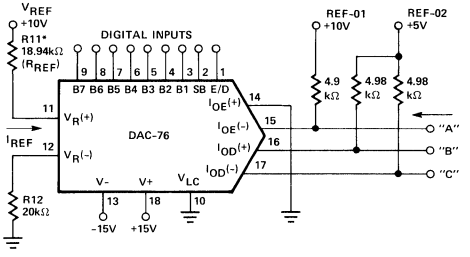


applications the tight relationship between I_{REF} and I_{FS} eliminates the need for trimming I_{REF}; but if desired, full scale trimming may be accomplished by selecting R11 or by using a potentiometer for R11.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common mode range. While the recommended operating range of DC reference currents is 0.1mA to 1.0mA, monotonic operation is maintained over an even wider range allowing the DAC-76 to be used in many multiplying applications. For variable reference applications, see section entitled "Multiplying Operation."

TRUE CURRENT OUTPUT OPERATION

RESISTIVE OUTPUT CONNECTIONS



OUTPUT VOLTAGE (V)

INPUT CODE	"A"	"B"	"C"	DIFF
11 111 1111	0			
11 110 1111	+ 5.02	N/A	N/A	N/A
11 000 0000	+10.00			
01 111 1111		−5.00	+5.00	−10
01 110 1111		+0.02	+5.00	− 4.98
01 000 0000	N/A	+5.00	+5.00	0
00 000 0000		+5.00	+5.00	0
00 110 1111		+5.00	+0.02	+ 4.98
00 111 1111		+5.00	−5.00	+10

NEGATIVE OUTPUT VOLTAGE COMPLIANCE $V_{OC}(-)$

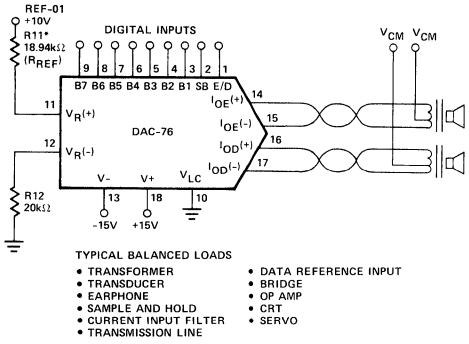
V− \ I_{FS}	1.0mA	2.0mA	4.0mA
−12V	−2.8V	−2.0V	−0.4V
−15V	−5.8V	−5.0V	−3.4V
−18V	−8.8V	−8.0V	−6.4V

MINIMUM NEGATIVE COMPLIANCE

$V_{OC}(-)$ MIN = (V−) + ($2I_{REF}$ • 1.6kΩ) + 8.4V

The DAC-76 has true current outputs with wide voltage compliance enabling fast drive of a variety of single-ended and balanced loads. Positive voltage compliance is +18V, and negative voltage compliance is −5.0V with I_{REF} = 528μA and V− = −15V. Negative voltage compliance for other values of I_{REF} and V− may be calculated using the table above. Typical connections, both single-ended and differential, are shown in the figure above with output voltage tables. Note the differential sign-plus-magnitude relationship between

BALANCED LOAD CONNECTIONS

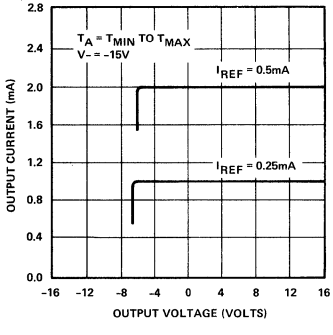


"B" and "C". The differential output voltage is independent of the +5.00 nominal voltage source as long as the $V_{OC}(-)$ minimum values are observed.

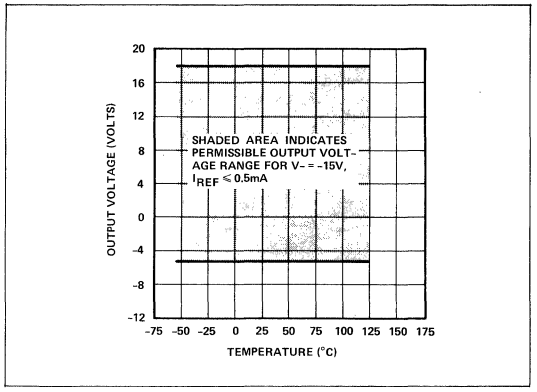
High common mode output range is possible due to the wide output voltage compliance and allows use with transformers or other balanced loads. The terminating impedances may be located a distance away from the DAC-76 allowing transmission of analog quantities as currents rather than voltages and elimination of ground loop errors. Capacitive termination is also possible, performing an "integrate-and-hold" process which is a function of V_{REF}, R_{REF}, the digital input code, and the selection time for a given current output. Resetting of the integrating capacitor may be accomplished with a CMOS switch in parallel with the capacitor. Thus, many applications traditionally requiring op amps may be performed with a high voltage compliance, current output DAC.

TYPICAL PERFORMANCE CURVES

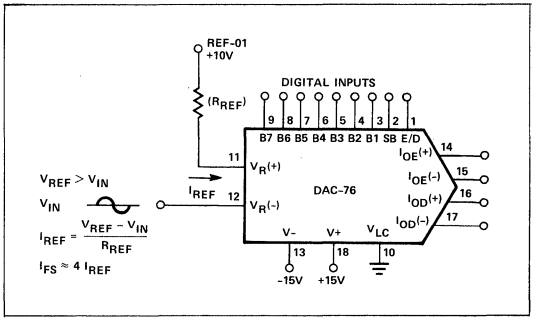
OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)



OUTPUT VOLTAGE COMPLIANCE vs TEMPERATURE

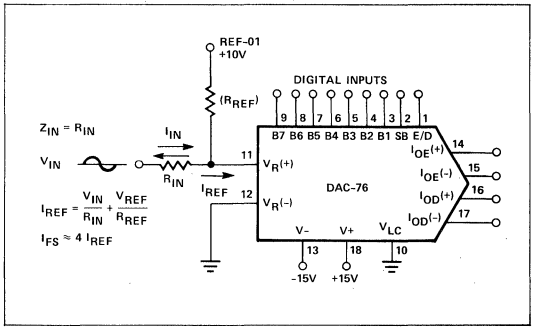


HIGH INPUT IMPEDANCE CONNECTION

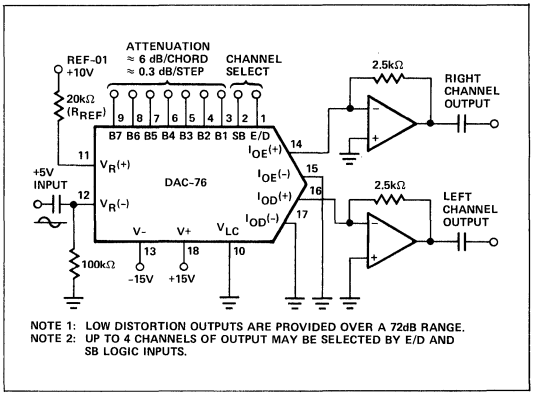


MULTIPLYING OPERATION

LOW INPUT IMPEDANCE CONNECTION

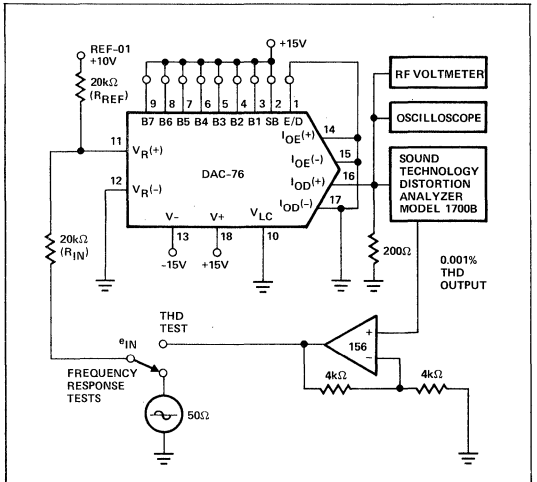


LOGARITHMIC DIGITAL GAIN CONTROL



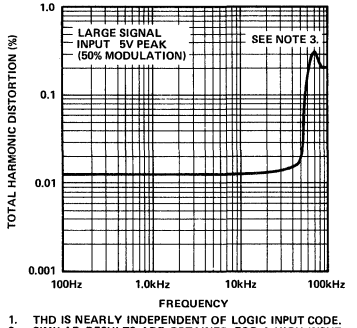
NOTE 1: LOW DISTORTION OUTPUTS ARE PROVIDED OVER A 72dB RANGE.
NOTE 2: UP TO 4 CHANNELS OF OUTPUT MAY BE SELECTED BY E/D AND SB LOGIC INPUTS.

REFERENCE AMPLIFIER DYNAMIC TEST CIRCUIT



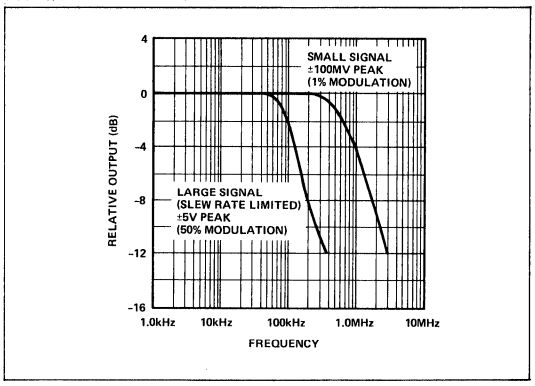
TYPICAL PERFORMANCE CURVES

REFERENCE AMPLIFIER TOTAL HARMONIC DISTORTION vs FREQUENCY (80kHz FILTER)



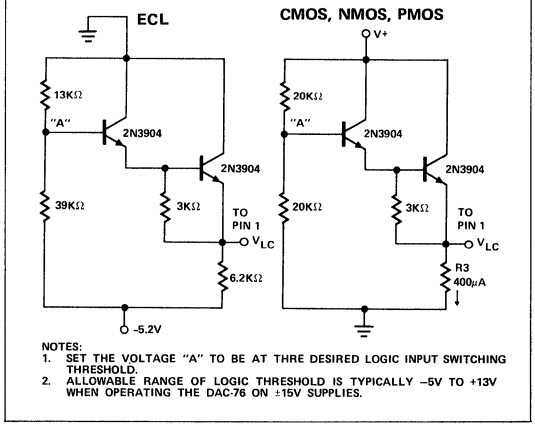
1. THD IS NEARLY INDEPENDENT OF LOGIC INPUT CODE.
2. SIMILAR RESULTS ARE OBTAINED FOR A HIGH INPUT IMPEDANCE CONNECTION USING PIN 12 AS AN INPUT.
3. INCREASED DISTORTION ABOVE 50kHz IS DUE TO SLEW RATE LIMITING WHICH DETERMINED LARGE SIGNAL BANDWIDTH. FOR AN INPUT OF ±2.5V PEAK (25% MODULATION), BANDWIDTH IS 100kHz.

REFERENCE AMPLIFIER INPUT FREQUENCY RESPONSE



LOGIC INPUT & POWER SUPPLY CONSIDERATIONS

INTERFACING CIRCUIT FOR ECL, CMOS, & NMOS LOGIC INPUTS



NOTES:
1. SET THE VOLTAGE "A" TO BE AT THRE DESIRED LOGIC INPUT SWITCHING THRESHOLD.
2. ALLOWABLE RANGE OF LOGIC THRESHOLD IS TYPICALLY -5V TO +13V WHEN OPERATING THE DAC-76 ON ±15V SUPPLIES.

LOGIC INPUTS

The DAC-76 may be interfaced with other-than-TTL logic by placing V_{LC} (Pin 10) at a potential which is 1.4V below the desired logic input switching threshold. However, this voltage source must be capable of sourcing and sinking a changing current at Pin 10.

The negative voltage at the logic inputs must be limited to +10V with respect to V− (Pin 13).

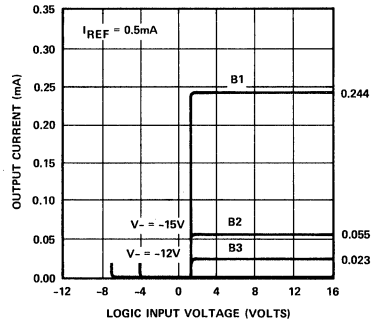
POWER SUPPLIES

As shown in the curves on the next page, power supply current drain is relatively independent of voltage and temperature and completely independent of the logic input states.

When operating with V− between −15V and −11V, output negative voltage compliance, $V_{OC}(-)$, reference input amplifier common mode voltage range, and logic input negative voltage range are reduced by an amount equivalent to the difference between −15V and the V− supply in use. Operation with V+ between +5V and +15V affects V_{LC} and the reference amplifier common mode positive voltage range in the same manner.

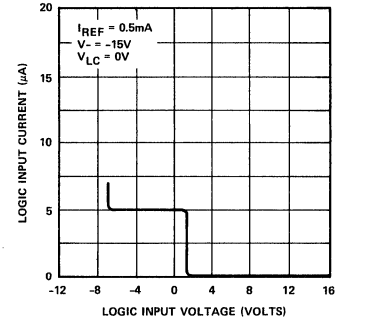
TYPICAL PERFORMANCE CURVES

BIT TRANSFER CHARACTERISTICS



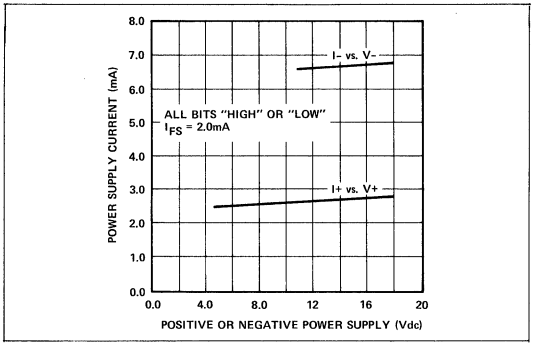
NOTE: ALL BITS ARE FULLY SWITCHED WITH LESS THAN 1/2 STEP ERROR AT SWITCHING POINTS WHICH ARE GUARANTEED TO LIE BETWEEN 0.8V AND 2.0V OVER THE OPERATING TEMPERATURE RANGE.

LOGIC INPUT CURRENT vs INPUT VOLTAGE AND LOGIC INPUT RANGE

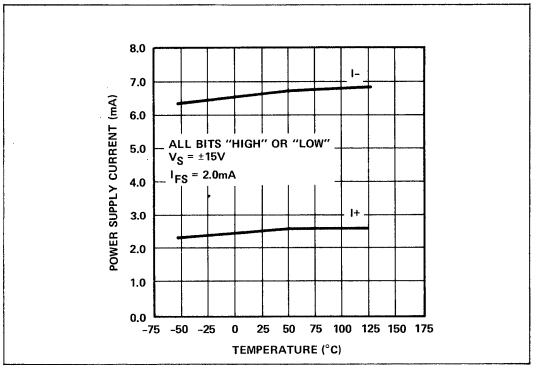


NOTE: LOGIC INPUT VOLTAGE RANGE IS INDEPENDENT OF THE POSITIVE POWER SUPPLY, AND LOGIC INPUTS MAY SWING ABOVE THE SUPPLY.

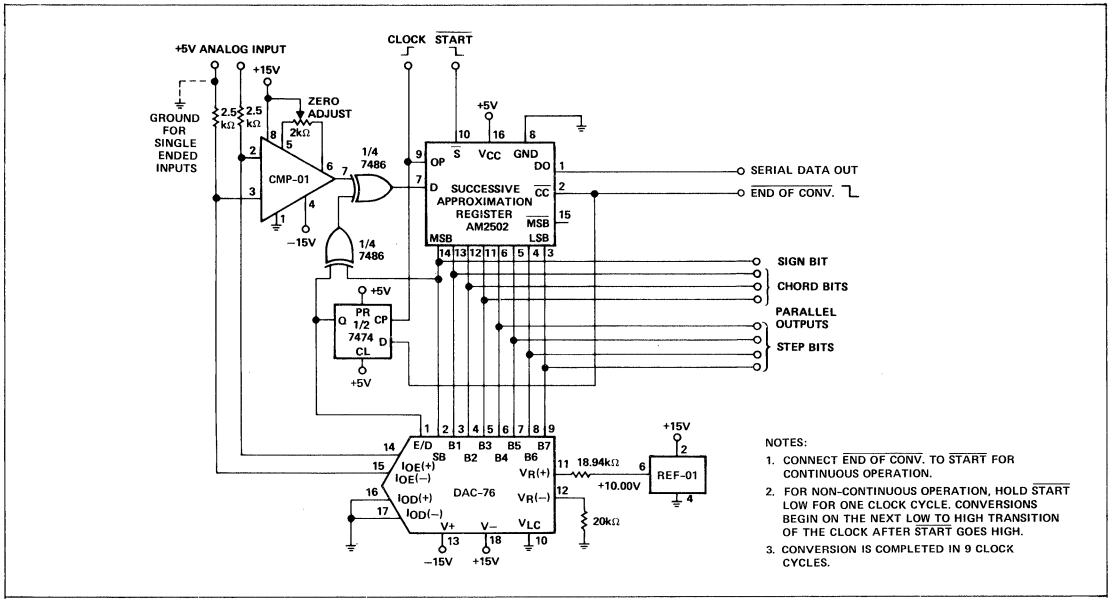
POWER SUPPLY CURRENTS vs POWER SUPPLY VOLTAGES



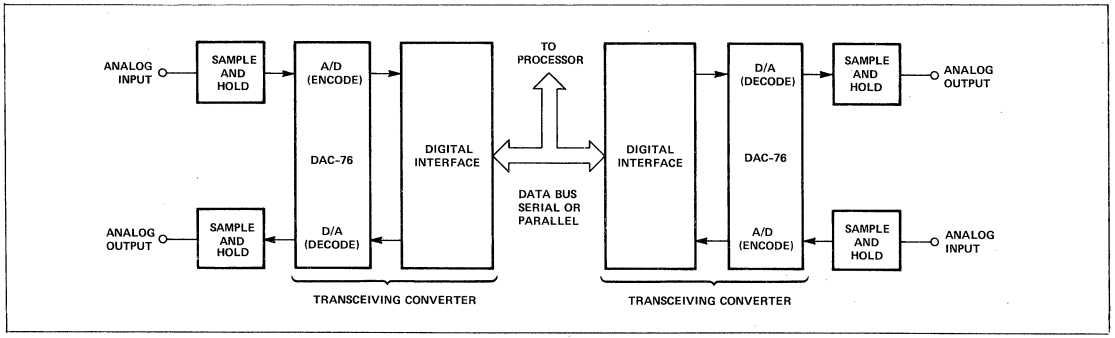
POWER SUPPLY CURRENTS vs TEMPERATURE



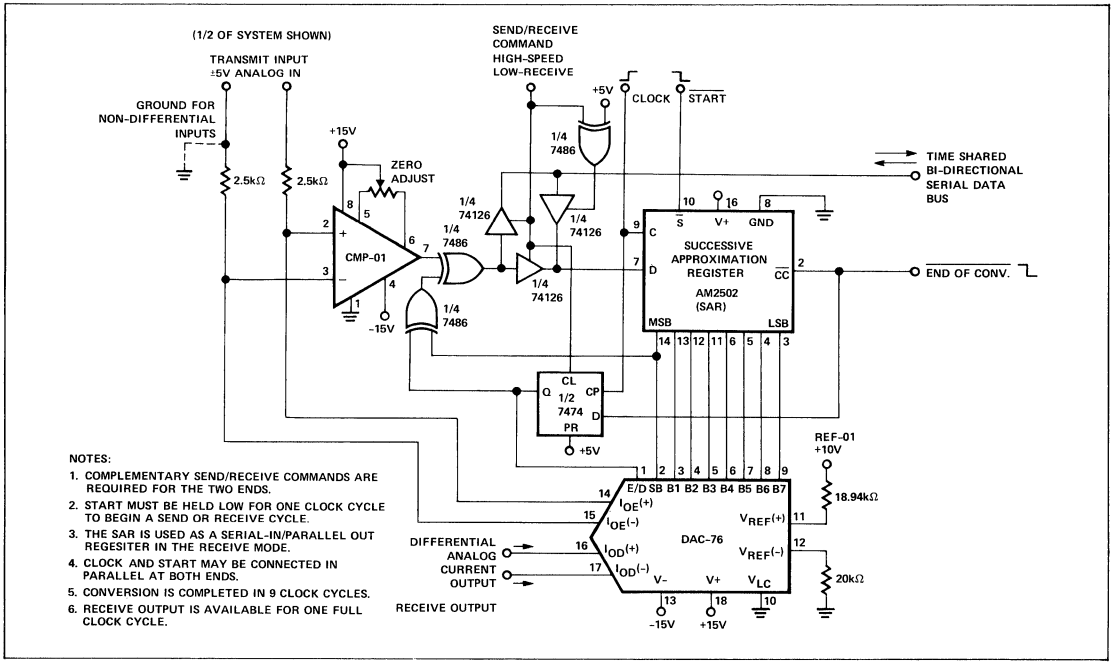
DETAILED ENCODE CONNECTIONS



TRANSCEIVING CONVERTER – TWO WAY DATA TRANSMISSION



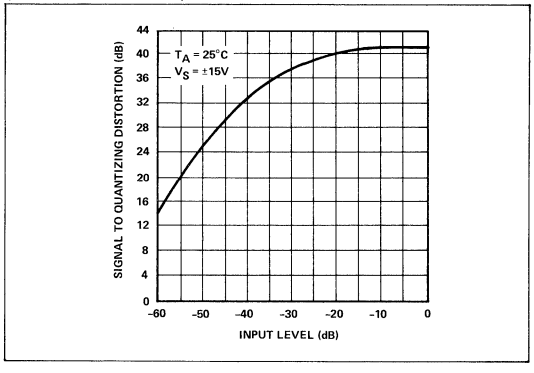
SERIAL DATA TRANSCEIVING CONVERTER



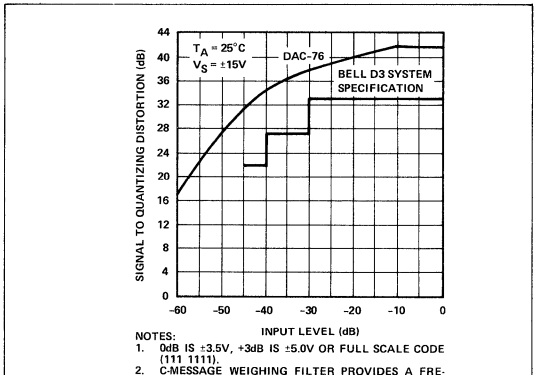
NOTES:
1. COMPLEMENTARY SEND/RECEIVE COMMANDS ARE REQUIRED FOR THE TWO ENDS.
2. START MUST BE HELD LOW FOR ONE CLOCK CYCLE TO BEGIN A SEND OR RECEIVE CYCLE.
3. THE SAR IS USED AS A SERIAL-IN/PARALLEL OUT REGESITER IN THE RECEIVE MODE.
4. CLOCK AND START MAY BE CONNECTED IN PARALLEL AT BOTH ENDS.
5. CONVERSION IS COMPLETED IN 9 CLOCK CYCLES.
6. RECEIVE OUTPUT IS AVAILABLE FOR ONE FULL CLOCK CYCLE.

TYPICAL SIGNAL TO QUANTIZING DISTORTION CURVES

SIGNAL TO QUANTIZING DISTORTION vs INPUT LEVEL (3kHz FLAT FILTER)

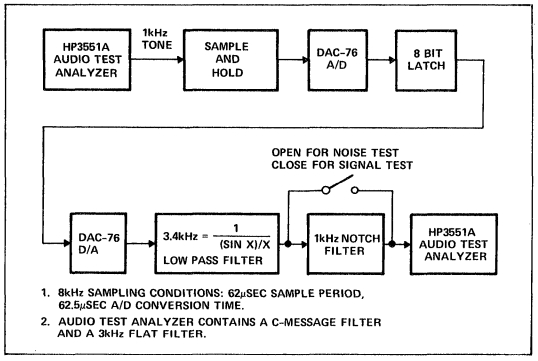


SIGNAL TO QUANTIZING DISTORTION vs INPUT LEVEL (C-MESSAGE WEIGHTING FILTER & BELL SPEC)



NOTES:
1. 0dB IS ±3.5V, +3dB IS ±5.0V OR FULL SCALE CODE (111 1111).
2. C-MESSAGE WEIGHING FILTER PROVIDES A FREQUENCY RESPONSE CHARACTERISTIC WHICH SIMULATES THE PRECEIVED RESPONSE OF THE HUMAN EAR TO TELEPHONE NOISE.

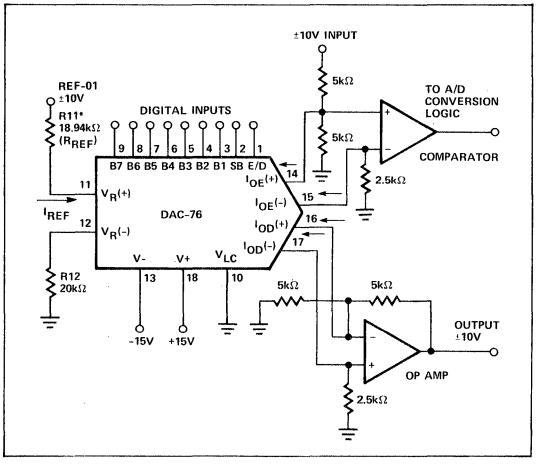
SIGNAL TO QUANTIZING DISTORTION TEST CIRCUIT



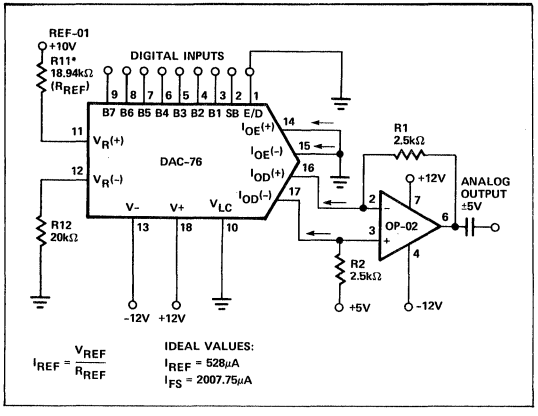
1. 8kHz SAMPLING CONDITIONS: 62μSEC SAMPLE PERIOD, 62.5μSEC A/D CONVERSION TIME.
2. AUDIO TEST ANALYZER CONTAINS A C-MESSAGE FILTER AND A 3kHz FLAT FILTER.

OUTPUT COMPLIANCE EXTENSION CONNECTIONS

±10V RANGE ENCODE/DECODE CONNECTIONS



COMPLIANCE EXTENSION USING AC COUPLED OUTPUT

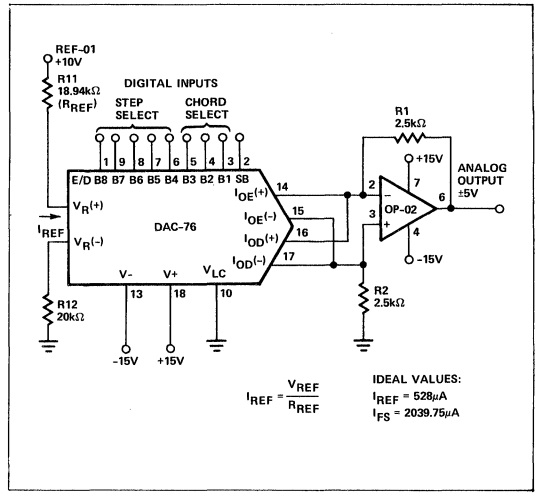


EXTENSION TO SIGN PLUS 78dB DYNAMIC RANGE

EXTENDED RANGE OPERATION

When used as a D/A converter only, the DAC-76 range may be extended from sign + 72dB to sign + 78dB by using the encode output current to insert additional levels halfway between each step. By connecting $I_{OD}(+)$ to $I_{OE}(+)$ and $I_{OD}(-)$ to $I_{OE}(-)$, the E/D logic input functions as a fifth step bit input. Full scale positive now becomes 1 111 11111; full scale negative is 0 111 11111. Each chord is divided into 32 steps instead of the former 16 steps, effectively increasing dynamic range by 6dB.

EXTENDED RANGE CONNECTIONS



SUMMARY TABLE FOR 3-CHORD BITS AND 5-STEP BITS

CHORD	STEP (μA)	RANGE (μA)	STEP (mV)	RANGE (V)
0	0.25	0 to 7.75	0.625	0 to 0.019
1	0.5	8.25 to 23.75	1.25	0.021 to 0.059
2	1.0	24.75 to 55.75	2.5	0.062 to 0.139
3	2.0	57.75 to 119.75	5.0	0.144 to 0.299
4	4.0	123.75 to 247.75	10	0.309 to 0.619
5	8.0	255.75 to 503.75	20	0.639 to 1.259
6	16	519.75 to 1015.75	40	1.299 to 2.539
7	32	1047.75 to 2039.75	80	2.619 to 5.099

The accompanying table summarizes the new chord and step characteristics obtained in the extended connection shown above.

ADDITIONAL DECODE OUTPUT TABLES

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS (SIGN BIT EXCLUDED)

STEP	CHORD	0 000	1 001	2 010	3 011	4 100	5 101	6 110	7 111
0	0000	0	8.25	24.75	57.75	123.75	255.75	519.75	1047.75
1	0001	0.5	9.25	26.75	61.75	131.75	271.75	551.75	1111.75
2	0010	1	10.25	28.75	65.75	139.75	287.75	583.75	1175.75
3	0011	1.5	11.25	30.75	69.75	147.75	303.75	615.75	1239.75
4	0100	2	12.25	32.75	73.75	155.75	319.75	647.75	1303.75
5	0101	2.5	13.25	34.75	77.75	163.75	335.75	679.75	1367.75
6	0110	3	14.25	36.75	81.75	171.75	351.75	711.75	1431.75
7	0111	3.5	15.25	38.75	85.75	179.75	367.75	743.75	1495.75
8	1000	4	16.25	40.75	89.75	187.75	383.75	775.75	1559.75
9	1001	4.5	17.25	42.75	93.75	195.75	399.75	807.75	1623.75
10	1010	5	18.25	44.75	97.75	203.75	415.75	839.75	1687.75
11	1011	5.5	19.25	46.75	101.75	211.75	431.75	871.75	1751.75
12	1100	6	20.25	48.75	105.75	219.75	447.75	903.75	1815.75
13	1101	6.5	21.25	50.75	109.75	227.75	463.75	935.75	1879.75
14	1110	7	22.25	52.75	113.75	235.75	479.75	967.75	1943.75
15	1111	7.5	23.25	54.75	117.75	243.75	495.75	999.75	2007.75
STEP SIZE		.50	1	2	4	8	16	32	64

CHORD SIZE SUMMARY TABLE DECODE OUTPUT (SIGN BIT EXCLUDED)

CHORD	CHORD ENDPOINTS NORMALIZED TO FULL SCALE	CHORD ENPOINTS IN μA WITH 2007.75μA F.S.	CHORD ENDPOINTS AS A PERCENTAGE OF FULL SCALE	CORD ENDPOINTS IN dB DOWN FROM FULL SCALE
0	30	7.5	0.37%	−48.55
1	93	23.25	1.16%	−38.73
2	219	54.75	2.73%	−31.29
3	471	117.75	5.86%	−24.63
4	975	243.75	12.1%	−18.32
5	1983	495.75	24.7%	−12.15
6	3999	999.75	49.8%	− 6.06
7	8031	2007.75	100%	0

DECODE OUTPUT EXPRESSED IN dB DOWN FROM FULL SCALE (SIGN BIT EXCLUDED)

STEP	CHORD	0 000	1 001	2 010	3 011	4 100	5 101	6 110	7 111
0	0000	—	−47.73	−38.18	−30.82	−24.20	−17.90	−11.74	−5.65
1	0001	−72.07	−46.73	−37.51	−30.24	−23.66	−17.37	−11.22	−5.13
2	0010	−66.05	−45.84	−36.88	−29.70	−23.15	−16.87	−10.73	−4.65
3	0011	−62.53	−45.03	−36.30	−29.18	−22.66	−16.40	−10.27	−4.19
4	0100	−60.03	−44.29	−35.75	−28.70	−22.21	−15.96	− 9.83	−3.75
5	0101	−58.10	−43.61	−35.24	−28.24	−21.77	−15.53	− 9.41	−3.33
6	0110	−56.51	−42.98	−34.75	−27.80	−21.36	−15.13	− 9.01	−2.94
7	0111	−55.17	−42.39	−34.29	−27.39	−20.96	−14.74	− 8.63	−2.56
8	1000	−54.01	−41.84	−33.85	−26.99	−20.58	−14.37	− 8.26	−2.19
9	1001	−52.99	−41.32	−33.44	−26.61	−20.22	−14.02	− 7.91	−1.84
10	1010	−52.07	−40.83	−33.04	−26.25	−19.87	−13.68	− 7.57	−1.51
11	1011	−51.25	−40.37	−32.66	−25.90	−19.54	−13.35	− 7.25	−1.18
12	1100	−50.49	−39.93	−32.29	−25.57	−19.22	−13.03	− 6.93	−0.87
13	1101	−49.80	−39.51	−31.95	−25.25	−18.91	−12.73	− 6.63	−0.57
14	1110	−49.15	−39.11	−31.61	−24.94	−18.61	−12.43	− 6.34	−0.28
15	1111	−48.55	−38.73	−31.29	−24.63	−18.32	−12.15	− 6.06	0

DECODE OUTPUT EXPRESSED IN PERCENT OF FULL SCALE (SIGN BIT EXCLUDED)

	CHORD	0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0	0.411	1.23	2.88	6.16	12.7	25.9	52.2
1	0001	0.025	0.461	1.33	3.08	6.56	13.5	27.5	55.4
2	0010	0.050	0.511	1.43	3.27	6.96	14.3	29.1	58.6
3	0011	0.075	0.560	1.53	3.47	7.36	15.1	30.7	61.7
4	0100	0.100	0.610	1.63	3.67	7.76	15.9	32.3	64.9
5	0101	0.125	0.660	1.73	3.87	8.16	16.7	33.9	68.1
6	0110	0.149	0.710	1.83	4.07	8.55	17.5	35.5	71.3
7	0111	0.174	0.760	1.93	4.27	8.95	18.3	37.0	74.5
8	1000	0.199	0.809	2.03	4.47	9.35	19.1	38.6	77.7
9	1001	0.224	0.859	2.13	4.67	9.75	19.9	40.2	80.9
10	1010	0.249	0.909	2.23	4.87	10.1	20.7	41.8	84.1
11	1011	0.274	0.959	2.33	5.07	10.5	21.5	43.4	87.2
12	1100	0.299	1.01	2.43	5.27	10.9	22.3	45.0	90.4
13	1101	0.324	1.06	2.53	5.47	11.3	23.1	46.6	93.6
14	1110	0.349	1.11	2.63	5.67	11.7	23.9	48.2	96.8
15	1111	0.374	1.16	2.73	5.86	12.1	24.7	49.9	100
STEP SIZE		0.025	0.050	0.100	0.199	0.398	0.797	1.59	3.19

DAC-78

COMDAC® COMPANDING D/A CONVERTER

FEATURES

- **Log Response Gives 12 Bit Accuracy Near Zero**
- **Sign Magnitude Coding**
- **Multiple Outputs Allow Shared A/D - D/A Conversion**
- **Tight Full Scale Tolerance Eliminates Calibration**
- **Low Full Scale Drift**
- **Multiplying Reference Inputs**
- **High Reliability**
- **Low Power Consumption**
- **Low Cost**

GENERAL DESCRIPTION

The DAC-78 monolithic D/A converter provides a linear approximation to logarithmic response curve of the form: K ($e^{my} - 1$) where K and m are scale factors and y is the normalized digital input. The curve is implemented by using 3 bits to select one of 8 straight line segments (chords) and 4 bits to select one of 16 binary steps within each chord. A sign bit is provided to select output signal polarity and an encode/decode operation. Accuracy is assured by specifying chord endpoint values, step nonlinearity and monotonicity over the full operating temperature range. Typical applications include: data compression, transducer linearization (e.g., photo and pin diodes), light and audio attenuators, and servo positioning systems. For telecommunications applications please refer to the DAC-88 data sheet.

DAC-78 TRANSFER FUNCTION

The DAC-78 was originally designed for use in companding telecommunications applications. It was noted that the transfer function thus generated could also be used in a large number of industrial control, attenuator or data compression applications. The transfer function is in the form $X = k(e^{my}-1)$ where:

X = analog output
k, m = scale factors
y = normalized digital input

This was derived from a Bell system specification which has the following function:

$$Y = \frac{\ln(1+\mu X)}{\ln(1+\mu)} \quad \text{where } \mu = 255$$

Solving for D/A converter operations gives:

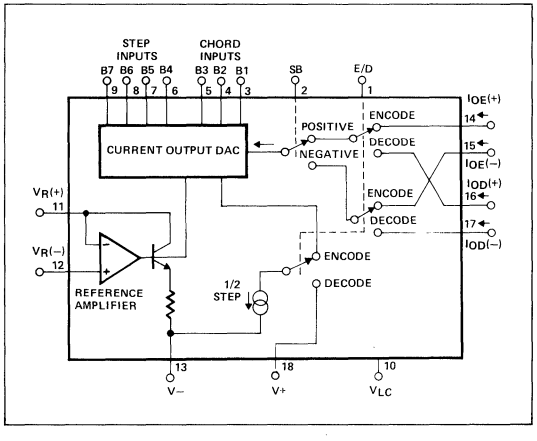
$$X = \frac{\epsilon^{\frac{5.55 \ldots Y}{128}} - 1}{256}$$

which after adjustment for the linear approximation effects yields

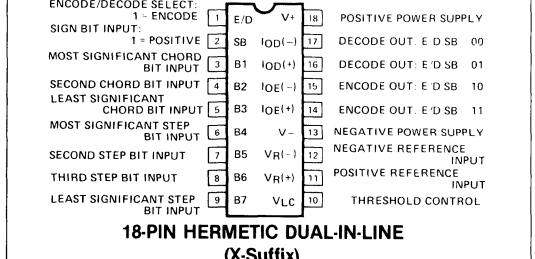
$$X = 0.00365(\epsilon^{0.0425Y} - 1)(\text{Sign } Y)$$

This equation gives a normalized number which when multiplied by the smallest step current (.25μA for 528μA I_{REF}) will give a good approximation of the input. Tables are given in the data sheet with which the exact output may be calculated.

EQUIVALENT CIRCUIT AND PIN CONNECTION DIAGRAM



PIN CONNECTIONS & ORDERING INFORMATION



18-PIN HERMETIC DUAL-IN-LINE
(X-Suffix)

CHORD ACCURACY (STEP)		TEMP
±1/4	DAC-78EX	IND
±1/2	DAC-78FX	IND
±1	DAC-78GX	IND

†All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

ABSOLUTE MAXIMUM RATINGS

V+ Supply to V– Supply 36V
V_{LC} Swing ..... V– plus 8V to V+
Analog Current Outputs ..... V– plus 8V to V– plus 36V
Reference Inputs ..... V– to V+
Reference Input Differential Voltage ..... ±18V
Reference Input Current 1.25mA
Logic Inputs ..... V– plus 8V to V– plus 36V

Operating Temperature ..... –25°C to +85°C
Storage Temperature ..... –65°C to +150°C
Dice Junction Temperature ..... –65°C to +150°C
Power Dissipation 500mW
Derate above 100°C ..... 10mW/°C
Lead Soldering Temperature ..... 300°C (60 nS)

NOTE: Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 528\mu A$, $-25°C \le T_A \le T_A \le +85°C$, and all 4 outputs, unless otherwise noted.

			DAC-78-E			DAC-78-F			DAC-78-G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Resolution		8 chords with 16 steps each	±128	±128	±128	±128	±128	±128	±128	±128	±128	Steps
Dynamic Range		20 log ($I_{7,15}/I_{0,1}$)	72	72	72	72	72	72	72	72	72	dB
Monotonicity		Sign Bit + or –	128	—	—	128	—	—	128	—	—	Steps
Chord Endpoint Accuracy Chord Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	—	—	±1/4	—	—	±1/2	—	—	±1	Step
Chord Endpoint Accuracy All Chords Other Than Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	—	—	±1/2	—	—	±1	—	—	±1½	Step
Encode Offset Current		Additional output encode/decode = 1	3/8	1/2	5/8	1/4	1/2	3/4	1/4	1/2	3/4	Step
Settling Time (Note 1)	t_s	To within ±1/2 step	—	500	see note 1	—	500	see note 1	—	500	see note 1	ns
Settling Time in Chord Zero	T_{SCO}	To within ±1/2 step	—	500	—	—	500	—	—	500	—	ns
Full Scale Drift (C_7)	ΔI_{FS}	Full temperature range	—	±1/16	±1/10	—	±1/10	±1/4	—	±1/10	±1/2	Step
Output Voltage Compliance	V_{OC}	Full scale current change ≤1/2 step	-5	—	+18	-5	—	+18	-5	—	+18	Volts
Full Scale Symmetry Error (Note 2)	$I_O(+) - I_O(-)$	Decode or encode pair Input Code 111 1111	—	±1/40	±1/8	—	±1/40	±1/4	—	±1/20	±1/2	Step
Zero Scale Current (Note 2)	I_{ZS}	Measured at selected output 000 0000 input	—	1/40	1/8	—	1/40	1/4	—	1/20	1/2	Step
Disable Current (All bits high) (Note 2)	I_{DIS}	Leakage of output disabled by E/D and SB	—	5.0	100	—	5.0	100	—	5.0	100	nA
Step Accuracy Chord Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	—	—	±1/4	—	—	±1/2	—	—	±1	Step
Step Accuracy All Chords Other Than Zero		Error relative to ideal values at $I_{FS} = 2016\mu A$	—	—	±1/2	—	—	±1	—	—	±1½	Step
Output Current Range	I_{FSR}		0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	mA
Logic Input Levels, Logic "0"	V_{IL}	$V_{LC} = 0V$	—	—	0.8	—	—	0.8	—	—	0.8	Volts
Logic Input Levels, Logic "1"	V_{IH}	$V_{LC} = 0V$	2.0	—	—	2.0	—	—	2.0	—	—	Volts
Logic Input Current	I_{IN}	$V_{IN} = -5V$ to +18V	—	—	120	—	—	120	—	—	120	μA
Logic Input Swing	V_{IS}	V– = –15V	-5	—	+18	-5	—	+18	-5	—	+18	Volts
Reference Bias Current	I_{12}		—	-3.0	-12.0	—	-3.0	-12.0	—	-3.0	-12.0	μA
Reference Input Slew Rate	dI/dt		—	0.25	—	—	0.25	—	—	0.25	—	mA/μs
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	$PSSI_{FS+}$	V+ = 4.5 to 18V	—	±1/20	±1/2	—	±1/20	±1/2	—	±1/20	±1/2	Step
	$PSSI_{FS-}$	V– = –10.8V to –18V	—	±1/10	±1/2	—	±1/10	±1/2	—	±1/10	±1/2	Step
Power Supply Current	I+	$V_S = +5V, -15V, I_{FS} = 2.0mA$	—	2.7	5.5	—	2.7	5.5	—	2.7	5.5	mA
	I–		—	-6.7	-12	—	-6.7	-12	—	-6.7	-12	
	I+	$V_S = \pm 15V, I_{FS} = 2.0mA$	—	2.7	5.75	—	2.7	5.75	—	2.7	5.75	mA
	I–		—	-6.7	-12	—	-6.7	-12	—	-6.7	-12	

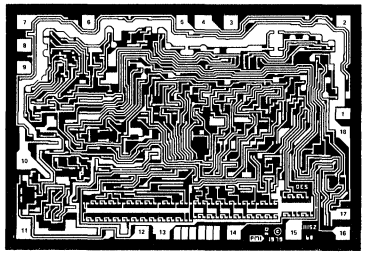
NOTES:
1. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) step size is 0.5μA, while in the last chord near full scale (C_7) step size is 64μA. Settling time varies for each of the chord bits and step bits and a maximum specification in misleading.
2. Current specifications relate to differential currents between (+) and (–) output leads. At the selected outputs, equal idle currents are present simultaneously on both current output leads.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 528\mu A$, $-25°C \leq T_A \leq +85°C$, and for all 4 outputs, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-78-E MIN	DAC-78-E TYP	DAC-78-E MAX	DAC-78-F MIN	DAC-78-F TYP	DAC-78-F MAX	DAC-78-G MIN	DAC-78-G TYP	DAC-78-G MAX	UNITS
Power Dissipation	P_D	V_S +5V, −15V	—	114	207	—	114	207	—	114	207	mW
	P_D	$V_S = \pm 15V$	—	141	262	—	141	262	—	141	262	mW
Full Scale Current Deviation From Ideal Deviation (See Tables)(Note 2)	$I_{FS}(D)$	V_{REF} 10.000V, $T_A = 25°C$	—	—	±1/2	—	—	±1	—	—	±1½	Step
	$I_{FS}(E)$	R11 = 19.53kΩ R12 = 20kΩ	—	—	±1/2	—	—	±1	—	—	±1½	Step
Idle Current (Note 2)	I_I		—	10	—	—	10	—	—	10	—	μA

NOTES:
1. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) step size is 0.5μA, while in the last chord near full scale (C_7) step size is 64μA. Settling time varies for each of the chord bits and step bits and a maximum specification in misleading.
2. Current specifications relate to differential currents between (+) and (−) output leads. At the selected outputs, equal idle currents are present simultaneously on both current output leads.

DICE CHARACTERISTICS



DIE SIZE 0.123 X 0.085 inch

1. E/D
2. S.B.
3. BIT 1 (MSB)
4. BIT 2
5. BIT 3
6. BIT 4
7. BIT 5
8. BIT 6
9. BIT 7 (LSB)
10. V_{LC}
11. V_R (+)
12. V_R (−)
13. V −
14. I_{OE} (+)
15. I_{OE} (−)
16. I_{OD} (+)
17. I_{OD} (−)
18. V +

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 528\mu A$, $T_A = 25°C$ and all 4 outputs, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-78-N (NOTE 3) LIMIT	DAC-78-G (NOTE 4) LIMIT	UNITS
Resolution		8 chords with 16 steps each	±128	±128	Steps MIN
Dynamic Range		20 log ($I_{7,15}/I_{0,1}$)	72	72	dB MIN
Monotonicity		Sign Bit + or −	128	128	Steps MIN
Chord Endpoint Accuracy Chord Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	±1/2	±1	Step MAX
Chord Endpoint Accuracy All Chords Other Than Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	±1	±1½	Step MAX
Encode Current		Additional output encode/decode = 1	1/4 3/4	1/4 3/4	Step MIN Step MAX
Output Voltage Compliance	V_{OC}	Full scale current change ≤1/2 step	−5 +18	−5 +18	Volts MIN Volts MAX
Full Scale Symmetry Error (Note 2)	$I_{O+} - I_{O-}$	Decode or encode pair Input Code 111 1111	±1/4	±1/2	Step MAX
Zero Scale Current (Note 2)	I_{ZS}	Measured at selected output 000 0000 input	1/4	1/2	Step MAX
Disable Current (All bits high) (Note 2)	I_{DIS}	Leakage of output disabled by E/D and SB	100	100	nA MAX
Step Accuracy Chord Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	±1/2	±1	Step MAX
Step Accuracy All Chords Other Than Zero		Error relative to ideal values at $I_{FS} = 2016\mu A$	±1	±1½	Step MAX
Output Current Range	I_{FSR}		4.2	4.2	mA MAX
Logic Input Levels, Logic "0"	V_{IL}	$V_{LC} = 0V$	0.8	0.8	Volts MAX
Logic Input Levels, Logic "1"	V_{IH}	$V_{LC} = 0V$	2.0	2.0	Volts MIN
Logic Input Current	I_{IN}	$V_{IN} = -5V$ to $+18V$	120	120	μA MAX
Logic Input Swing	V_{IS}	V− = −15V	−5 +18	−5 +18	Volts MIN Volts MAX
Reference Bias Current	I_{12}		−12.0	−12.0	μA
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	$PSSI_{FS-}$	V+ = 4.5 to 18V	±1/2	±1/2	Step MAX
	$PSSI_{FS-}$	V− = −10.8V to −18V	±1/2	±1/2	Step MAX
Power Supply Current	I+ I−	$V_S = +5V, -15V$, $I_{FS} = 2.0mA$	5.5 −12	5.5 −12	mA MAX
	I+ I−	$V_S = \pm 15V$, $I_{FS} = 2.0mA$	5.75 −12	5.75 −12	mA MAX
Full Scale Current Deviation From Ideal Deviation (See Tables) (Note 2)	I_{FS} D	V_{REF} 10.000V, $T_A = 25°C$	±1	±1½	Step MAX
	I_{FS} E	R11 = 19.53kΩ R12 = 20kΩ	±1	±1½	Step MAX

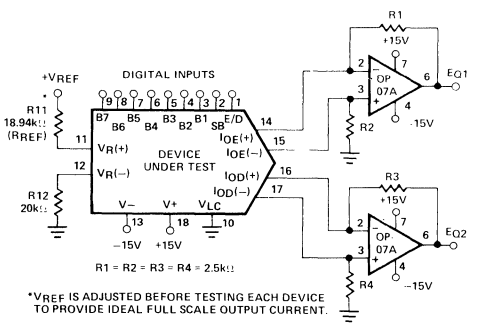
TYPICAL CHARACTERISTICS at $V_S = \pm 15V$, and $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-78-N TYP	DAC-78-G TYP	UNITS
Settling Time (Note 1)	t_S	To within ±1/2 step	500	500	nS
Settling Time in Chord Zero	T_{SCO}	To within ±1/2 step	500	500	nS
Full Scale Drift (C_7)	ΔI_{FS}	Full temperature range	±1/10	±1/10	Step
Reference Input Slew Rate	dI/dt		0.25	0.25	mA/μS
Power Dissipation	P_D	V_S +5V, −15V	114	114	mW
	P_D	$V_S = \pm 15V$	141	141	mW
Idle Current (Note 2)	I_I		10	10	μA

NOTES:

1. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) step size is 0.5μA, while in the last chord near full scale (C_7) step size is 64μA. Setting time varies for each of the chord bits and step bits and a maximum specification is misleading.
2. Current specifications relate to differential currents between (+) and (−) output leads. At the selected outputs, equal idle currents are present simultaneously on both current output leads.
3. See DAC-78F for typical values.
4. See DAC-78G for typical values.

OUTPUT CURRENT DC TEST CIRCUIT



*VREF IS ADJUSTED BEFORE TESTING EACH DEVICE TO PROVIDE IDEAL FULL SCALE OUTPUT CURRENT.

LINE SELECTION TABLE

TEST GROUP	ENCODE/ DECODE	SIGN BIT	OUTPUT MEASUREMENT	
1	1	1	$I_{OE}(+)$	(E_{O1}/R1)
2	1	0	$I_{OE}(-)$	(E_{O1}/R2)
3	0	1	$I_{OD}(+)$	(E_{O2}/R3)
4	0	0	$I_{OD}(-)$	(E_{O2}/R4)

NOTE: Accuracy is specified in the test circuit using the tables below to be within the specified proportion of a step at the maximum value in each chord. Monotonic operation is guaranteed for all input codes.

CONDENSED CURRENT OUTPUT TABLES ($I_{REF} = 528\mu A$)

IDEAL DECODE (DAC) OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

	CHORD	0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0	8.25	24.75	57.75	123.75	255.75	519.75	1047.75
15	1111	7.5	23.25	54.75	117.75	243.75	495.75	999.75	2007.75
STEP SIZE		0.50	1	2	4	8	16	32	64

IDEAL DECODE (ADC) OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

	CHORD	0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0.25	8.75	25.75	59.75	127.75	263.75	535.75	1079.75
15	1111	7.75	23.75	55.75	119.75	247.75	503.75	1015.75	2039.75
STEP SIZE		0.50	1	2	4	8	16	32	64

These tables may be extended to include all of the encode/decode currents (ideal with $I_{REF} = 528\mu A$) by multiplying any of the numbers in the normalized tables by $0.25\mu A$.

SPECIFICATION PARAMETER DEFINITIONS

FULL SCALE DRIFT

The change in output current over the full operating temperature with $V_{REF} = 10.000V$, R11 = 18.94kΩ, and R12 = 20kΩ.

ENCODE OFFSET CURRENT (A/D CONVERSION)

An offset current added to the DAC output to move the encode decision point to mid-value (i.e., the 0 → 1 transition should occur at the 1/2 I step point).

FULL SCALE SYMMETRY ERROR

The difference between $I_{OD}(-)$ and $I_{OD}(+)$ or the difference between $I_{OE}(-)$ and $I_{OE}(+)$ at full scale output.

OUTPUT VOLTAGE COMPLIANCE

The maximum output voltage swing at any current level which causes < ½ step change in output current.

IDEAL OUTPUT CURRENT

The difference between the (+) and (−) currents (encode or decode) at any code.

CHORDS

Groups of linearly-related steps in the transfer function. Also known as segments.

CHORD ENDPOINTS

The maximum code in each chord. Used to specify accuracy.

STEPS

Increments in each chord which divides it into 16 equal levels.

OUTPUT LEVEL NOTATION

Each output current level may be designated by the code $I_{C,S}$ where C = chord number and S = step number. For example, $I_{0,0}$ = zero scale current; $I_{0,1}$ = first step from zero; $I_{0,15}$ = endpoint of first chord (C_0); $I_{7,15}$ = full scale current. For encode operation $I_{C,S} = 0.5\,[2^C\,(S + 17) - 16.5]$. For decode operation $I_{C,S} = 0.5\,[S + 16.5) - 16.5]$ based on $I_{REF} = 528\mu A$.

DYNAMIC RANGE

Ratio of full scale current to step size in chord zero expressed in dB.

BASIC ENCODE OPERATION (COMPRESSING A/D CONVERSION)

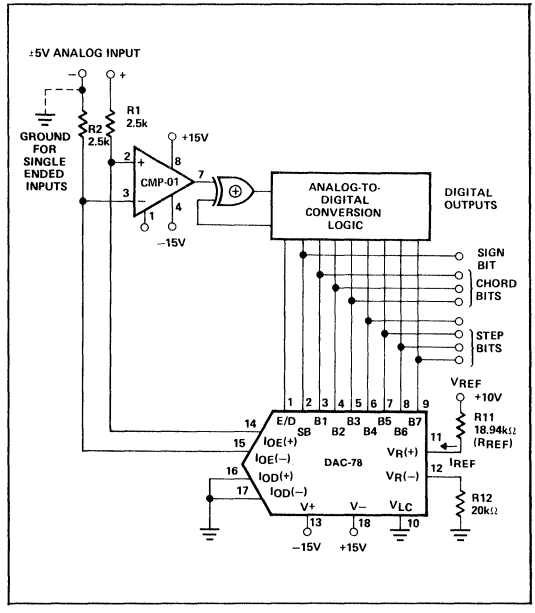
ENCODE DECISION LEVELS

Compressing A/D conversion with the DAC-78 requires a comparator, an exclusive-or gate, and a successive approximation register — the usual elements in any sign-plus-magnitude A/D converter. However, a compressing ADC has one signficant difference from regular A/D converters.

In a conventional (linear converter), the step size is a constant percentage of full scale, but in a compressing A/D converter, the step size increases as the output changes from zero scale to full scale.

When the DAC is used in the feedback loop of a successive approximation ADC the DAC outputs are used as decision levels to determine the edges of the quantizing bands. When the DAC is used in the decode mode it follows that the outputs must correspond to the center of the quantizing bands. Thus the encode mode output must exceed the decode mode output by one-half step. See AN 39 for further explanation.

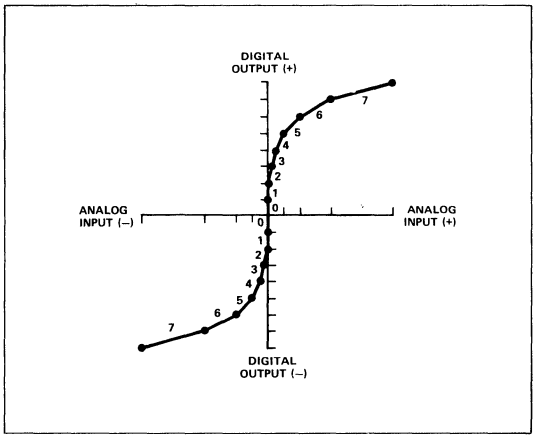
BASIC ENCODE (ADC) CONNECTIONS



IDEAL ENCODE (A/D) LEVEL (SIGN BIT EXCLUDED) IN MICROAMPS (I_{REF} = 528μA)

	CHORD	0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0.25	8.75	25.75	59.75	127.75	263.75	535.75	1079.75
1	0001	0.75	9.75	27.75	63.75	135.75	279.75	567.75	1143.75
2	0010	1.25	10.75	29.75	67.75	143.75	295.75	599.75	1207.75
3	0011	1.75	11.75	31.75	71.75	151.75	311.75	631.75	1271.75
4	0100	2.25	12.75	33.75	75.75	159.75	327.75	663.75	1335.75
5	0101	2.75	13.75	35.75	79.75	167.75	343.75	695.75	1399.75
6	0110	3.25	14.75	37.75	83.75	175.75	359.75	727.75	1463.75
7	0111	3.75	15.75	39.75	87.75	183.75	377.75	759.75	1527.75
8	1000	4.25	16.75	41.75	91.75	191.75	391.75	791.75	1591.75
9	1001	4.75	17.75	43.75	95.75	199.75	407.75	823.75	1655.75
10	1010	5.25	18.75	45.75	99.75	207.75	423.75	855.75	1719.75
11	1011	5.75	19.75	47.75	103.75	215.75	439.75	887.75	1783.75
12	1100	6.25	20.75	49.75	107.75	223.75	455.75	929.75	1847.75
13	1101	6.75	21.75	51.75	111.75	231.75	471.75	951.75	1911.75
14	1110	7.25	22.75	53.75	115.75	239.75	487.75	983.75	1975.75
15	1111	7.75	23.75	55.75	119.75	247.75	503.75	1015.75	2039.75
STEP SIZE		0.50	1	2	4	8	16	32	64

ENCODE TRANSFER CHARACTERISTICS (A/D CONVERSION)



ENCODING SEQUENCE

An encoding sequence begins with the sign bit decision. During this time the comparator is a polarity detector only. The Encode/Decode (E/D) input is held at a logic "0", so that no current flows into the encode outputs, and the comparator is effectively disconnected from the DAC. Once the input polarity has been determined, the E/D input is changed to a logic "1" allowing current to flow into $I_{OE}(+)$ or $I_{OE}(-)$ depending upon the Sign Bit Answer.

For positive inputs, current flows into $I_{OE}(+)$ through R1, and the comparator's output will be entered as the answer for each successive decision. For negative inputs, current flows into $I_{OE}(-)$ through R2 developing a negative voltage which is compared with the analog input. An exclusive-OR gate inverts the comparator's output during negative trials to maintain the proper logic coding, all ones for full scale and all zeros for zero scale.

The bits are converted with a successive removal technique, starting with a decision at the code 011 1111 and turning off bits sequentially until all decisions have been made. This ensures the accuracy of the result.

BASIC DECODE OPERATION (EXPANDING D/A CONVERSION)

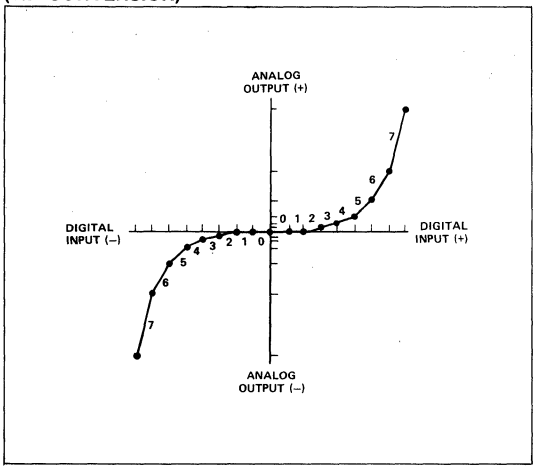
DECODE OPERATION

D/A conversion with the DAC-78 may be illustrated by using an operational amplifier connected to the decode outputs. The decode mode of operation is selected by applying a logic "0" to the Encode/Decode input. This enables the I_{OD} outputs, disables the I_{OE} outputs and, allows $I_{OD}(+)$ or $I_{OD}(-)$ to be selected by the Sign Bit input. When the Sign Bit input is high, a logic "1", all of the output current flows into $I_{OD}(+)$ forcing a positive voltage at the operational amplifier's output. When the Sign Bit input is low, a logic "0", all of the output current flows into $I_{OD}(-)$ through R2 forcing a negative voltage output. Since the Sign Bit only steers current into $I_{OD}(+)$ or $I_{OD}(-)$, the output will always be symmetrical, limited only by the matching of R1 and R2.

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS (SIGN BIT EXCLUDED) (I_{REF} = 528μA)

STEP	CHORD	0 000	1 001	2 010	3 011	4 100	5 101	6 110	7 111
0	0000	0	8.25	24.75	57.75	123.75	255.75	519.75	1047.75
1	0001	0.5	9.25	26.75	61.75	131.75	271.75	551.75	1111.75
2	0010	1	10.25	28.75	65.75	139.75	287.75	583.75	1175.75
3	0011	1.5	11.25	30.75	69.75	147.75	303.75	615.75	1239.75
4	0100	2	12.25	32.75	73.75	155.75	319.75	647.75	1303.75
5	0101	2.5	13.25	34.75	77.75	163.75	335.75	679.75	1367.75
6	0110	3	14.25	36.75	81.75	171.75	351.75	711.75	1431.75
7	0111	3.5	15.25	38.75	85.75	179.75	367.75	743.75	1495.75
8	1000	4	16.25	40.75	89.75	187.75	383.75	775.75	1559.75
9	1001	4.5	17.25	42.75	93.75	195.75	399.75	807.75	1623.75
10	1010	5	18.25	44.75	97.75	203.75	415.75	839.75	1687.75
11	1011	5.5	19.25	46.75	101.75	211.75	431.75	871.75	1751.75
12	1100	6	20.25	48.75	105.75	219.75	447.75	903.75	1815.75
13	1101	6.5	21.25	50.75	109.75	227.75	463.75	935.75	1879.75
14	1110	7	22.25	52.75	113.75	235.75	479.75	967.75	1943.75
15	1111	7.5	23.25	54.75	117.75	243.75	495.75	999.75	2007.75
STEP SIZE		.50	1	2	4	8	16	32	64

DECODE TRANSFER CHARACTERISTIC (D/A CONVERSION)



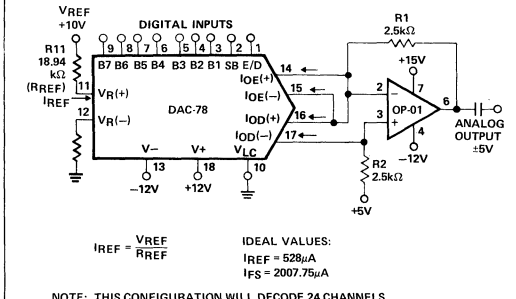
BASIC REFERENCE CONSIDERATIONS

Full scale output current is ideally 2007.75μA when the reference current is 528μA in the decode mode, due to a multiplier of 3.803. In the encode mode it is 2039.75μA because the additional 1/2 step adds 32μA to the output. A percentage change in I_{REF} caused by changes in V_{REF} or R_{REF} will produce the same percentage change in output current.

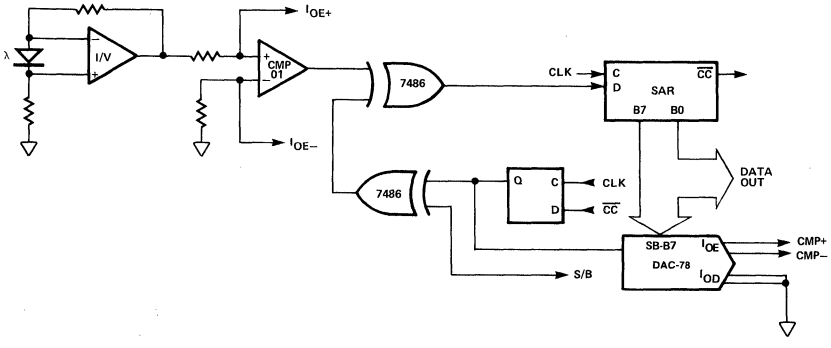
The large step size at full scale allows the use of inexpensive references in many applications. In some situations V_{REF} may even be the positive power supply. For example, with V+ = 15V, R_{REF} = 15V/528μA, or 28.4kΩ. When using a power supply as a reference, R11 should be two resistors, R11A and R11B, and the junction should be bypassed to ground to provide decoupling.

	E/D	SB	B1	B2	B3	B4	B5	B6	B7	E_0
POS FULL SCALE	0	1	1	1	1	1	1	1	1	5.019V
(+) ZERO SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.0012
(+) ZERO SCALE	0	1	0	0	0	0	0	0	0	0V
(–) ZERO SCALE	0	0	0	0	0	0	0	0	0	0V
(–) ZERO SCALE +1 STEP	0	0	0	0	0	0	0	0	1	–0.0012
NEG FULL SCALE	0	0	1	1	1	1	1	1	1	–5.019V

BASIC DECODE CONNECTIONS



PHOTODIODE LINEARIZING CIRCUIT



REFERENCE AMPLIFIER OPERATION

REFERENCE AMPLIFIER SETUP

The DAC-78 is a multiplying D/A converter in which the output current is the product of the normalized digital input and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full scale output current is a linear function of the reference current and is given for all four outputs in the figures above.

REFERENCE RECOMMENDATIONS

For most applications a +10.0V reference, such as the PMI REF-01, is recommended for optimum full scale temperature coefficient performance.

POWER SUPPLY CONSIDERATIONS

POWER SUPPLIES

Power supply current drain is relatively independent of voltage and temperature and completely independent of the logic input states.

When operating with V− between −15V and −11V, output negative voltage compliance, $V_{OC}(-)$, reference input amplifier common mode voltage range, and logic input negative voltage range are reduced by an amount equivalent to the difference between −15V and the V− supply in use. Operation with V+ between +5V and +15V affects V_{LC} and the reference amplifier common mode positive voltage range in the same manner.

OUTPUT VOLTAGE COMPLIANCE

The DAC-78 has true current outputs with wide voltage compliance enabling fast drive of a variety of single ended and balanced loads. Positive voltage compliance is +18V and negative voltage compliance is −5.0V with $I_{REF} = 528\mu A$ and V = −15V. Negative voltage compliance $V_{OC}(-)$ for other values of I_{REF} and V− may be obtained from the table, or calculated as follows:

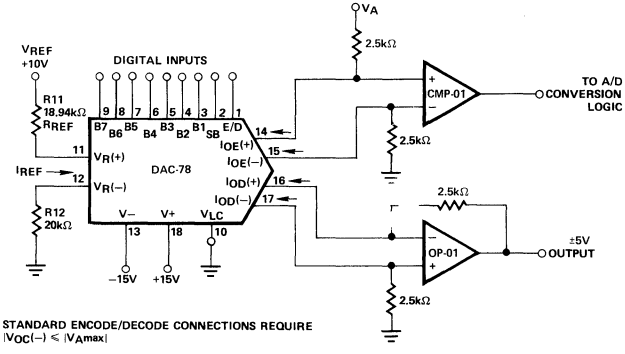
$$V_{OC}(-)\ \text{min} = (V-) + (2\ I_{REF} \times 1.6k\Omega) + 8.4V$$

Output voltage compliance can be extended in both encode and decode modes using the connections shown below.

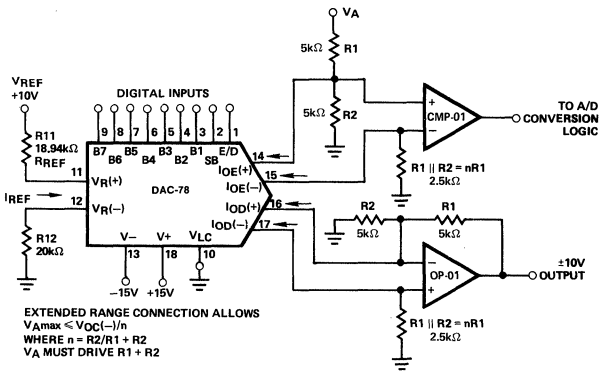
NEGATIVE OUTPUT VOLTAGE COMPLIANCE $V_{OC}(-)$

V− \ I_{FS}	1.0mA	2.0mA	4.0mA
−12V	−2.8V	−2.0V	−0.4V
−15V	−5.8V	−5.0V	−3.4V
−18V	−8.8V	−8.0V	−6.4V

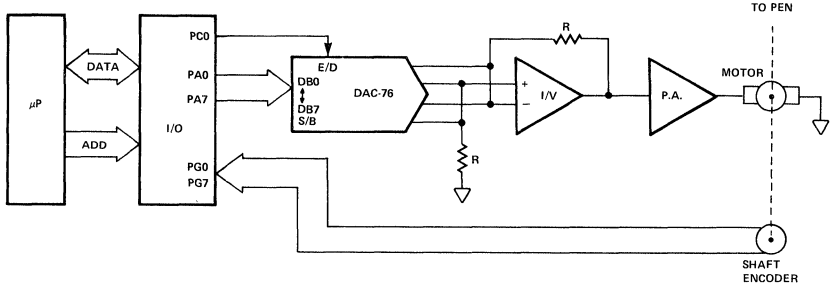
STANDARD OUTPUT CONNECTIONS



COMPLIANCE EXTENSION CONNECTIONS



SERVO POSITIONING SYSTEM



DAC-100/DAC-101

10-BIT D/A CONVERTERS

FEATURES

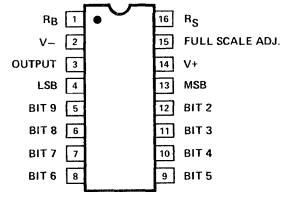
- **Complete** ..... **Internal Reference**
- **Flexible** ..... **0 to 2mA Output**
- **Fast Settling** ..... **225nsec (8 Bits), 375nsec (10 Bits)**
- **Stable** ..... **Tempcos to ±15ppm/° C Maximum**
- **0° C/ +70° C, −25° C/ +85° C, −55° C/ +125° C Models Available**
- **TTL Compatible Logic Inputs**
- **Wide Supply Range** ..... **±6V to ±18V**
- **8 and 10 Bit Versions Available**
- **MIL-STD-883 Class B Processing Models Available**
- **Low Cost Q3, Q4 Series**

GENERAL DESCRIPTION

The DAC-100/DAC-101 are complete 10-bit resolution digital-to-analog converters constructed on two monolithic chips in a single 16-pin DIP. Featuring excellent linearity vs. temperature performance, the DAC-100/DAC-101 include a low tempco voltage reference, ten current source/switches and a high stability thin-film R-2R ladder network. Maximum application flexibility is provided by the fast current output and by matched bipolar offset and feedback resistors which are included for use with an external op amp for voltage output applications. Although all units have 10-bit resolution, a wide choice of linearity and tempco options is provided to allow price/performance optimization.

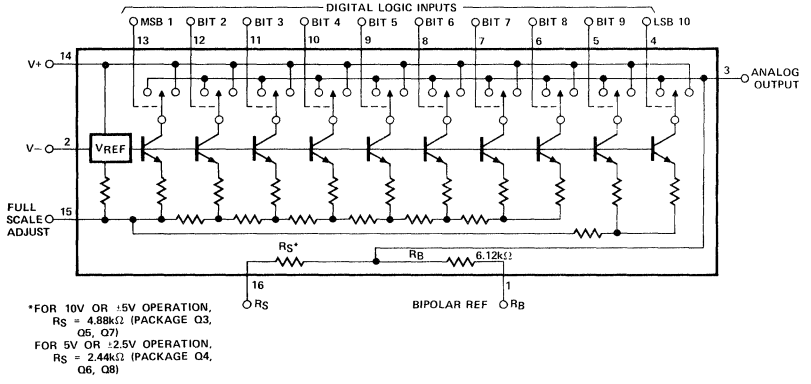
The small size, wide operating temperature range, low power consumption and high reliability construction make the DAC-100 ideal for aerospace applications. Other applications include use in servo-positioning systems, X-Y plotters, CRT displays, programmable power supplies, analog meter movement drivers, waveform generators and high speed analog-to-digital converters. The DAC-101 is used in similar applications with limited temperature range requirements.

PIN CONNECTIONS



16 PIN HERMETIC DUAL-IN-LINE (Q-Suffix)

SIMPLIFIED SCHEMATIC



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25°C \leq T_A \leq +85°C$ for Q7, Q8 devices; $0°C \leq T_A \leq +70°C$; for Q3 and Q4, $-55°C \leq T_A \leq +125°C$ for Q5 and Q6 devices and $T_A = 25°C$ for DAC-100 (All), unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-100	DAC-101	MIN	TYP	MAX	UNITS
Resolution					10	10	10	Bits
Nonlinearity	N_L	(±1/2LSB — 10 bits)	A—		—	—	±0.05	%FS
(For nonlinearity/tempco	N_L	(±1/2LSB — 9 bits)	B—	EQ	—	—	±0.1	%FS
combinations, see Ordering	N_L	(±1/2LSB — 8 bits)	C—	FQ	—	—	±0.2	%FS
Information.)	N_L	(±3/4LSB — 8 bits)	D—	GQ	—	—	±0.3	%FS
Full Scale Tempco (See Full Scale Test Circuit)	T_C		—A		—	—	±15	ppm/°C
	T_C		—B		—	—	±30	ppm/°C
	T_C		—C		—	—	±60	ppm/°C
	T_C		—D		—	—	±120	ppm/°C
				ALL	—	±120	—	ppm/°C
Settling Time $T_A = 25°C$	t_S	to ±0.05% FS	ALL		—	—	375	ns
	t_S	to ±0.1% FS	ALL		—	—	300	ns
	t_S	to ±0.2% FS	ALL		—	—	225	ns
	t_S	to ±0.4% FS	ALL		—	—	150	ns
	t_S	to ±0.8% FS	ALL		—	—	100	ns
				ALL	—	200	—	ns
Full Range Output Voltage (Limits guarangee adjustability to exact 10.0 (5.0)V with a 200Ω Trimpot® between Adjust and V−	F_{FR}	Connect FS Adjust to V− 10V Models (Q3, Q5, Q7) (See Full Scale Test Circuit)		ALL	10	—	11.1	V
		5V Models (Q4, Q6, Q8) $V_{IN} = 0.0V$ (See Full Scale Test Circuit)			5	—	5.55	V
Zero Scale Output Voltage	V_{ZS}	$V_{IN} = 2.1V$	ALL	EQ/FQ	—	—	0.013	%FS
				GQ	—	—	0.02	
Logic Inputs: High	V_{INH}	Measured with respect to output pin	ALL	ALL	2.1	—	—	V
Logic Inputs: Low	V_{INL}	Measured with respect to output pin	ALL	ALL	—	—	0.7	V
Logic Input Current, Each Input	I_{IN}	$V_{IN} = 0$ to $+6V$	ALL	ALL	—	—	5	μA
Logic Input Resistance	R_{IN}	$V_{IN} = 0$ to $+6V$	ALL	ALL	—	3	—	mΩ
Logic Input Capacitance	C_{IN}		ALL	ALL	—	2	—	pF
Output Resistance	R_O		ALL	ALL	—	500	—	kΩ
Output Capacitance	C_O		ALL	ALL	—	13	—	pF
Applied Power Supplies: V+		Linearity within specification	ALL	ALL	+6	—	+18	V
Applied Power Supplies: V−		Linearity within specification	ALL	ALL	−6	—	−18	V
Power Supply Sensitivity	P_{SS}	$V_S = \pm 6V$ to $\pm 18V$	ALL	ALL	—	—	±0.10	% per Volt
Power Consumption	P_D	$V_S = \pm 15V$	Q3, Q4	EQ	—	200	300	mW
	P_D	$V_S = \pm 6V$	Q3, Q4		—	80	100	mW
	P_D	$V_S = \pm 15V$	Q5, Q6, Q7, Q8		—	200	250	mW
	P_D	$V_S = \pm 15V$		FQ/GQ	—	250	350	mW
Positive Supply Current	I+	$V_S = +15V$	Q3, Q4	EQ	—	—	10.0	mA
	I+	$V_S = +15V$		FQ/GQ	—	—	12	mA
	I+	$V_S = +15V$	Q5, Q6, Q7, Q8		—	—	8.33	mA
Negative Supply Current	I−	$V_S = -15V$	Q3, Q4	EQ	—	—	−10.0	mA
	I−	$V_S = -15V$	Q5, Q6, Q7, Q8		—	—	−8.33	mA
	I−	$V_S = -15V$		FQ/GQ	—	—	−12	mA

ABSOLUTE MAXIMUM RATINGS (Note 2)

V+ Supply to V− Supply ..... 0 to +36V
V+ Supply to Output ..... 0 to +18V
V− Supply to Output ..... 0 to −18V
Logic Inputs to Output ..... −1V to +6V
Power Dissipation (Note 1) 500mW
Operating Temperature Range
Q3, Q4 & All DAC-101 ..... 0° C to +70° C
All others ..... −55° C to +125° C

DICE Junction Temperature ..... −25° C to +150° C
Storage Temperature Range ..... −65° C to +150° C
Lead Temperature (Soldering) ..... +300° C (60 sec)

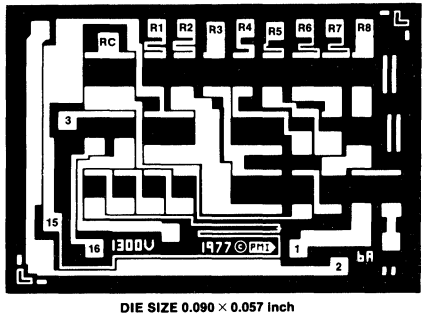
NOTES:
1. Rating applies to ambient temperature of 100° C. Above 100° C, derate at 10mW/° C.
2. Ratings apply to DICE and packaged parts, unless otherwise noted.

ORDERING INFORMATION†

N.L.** %FS MAX.	TEMPCO** ppm/° C MAX.	MILITARY TEMPERATURE $V_O = \pm5V/10V$	MILITARY TEMPERATURE $V_O = \pm2.5V/5V$	INDUSTRIAL TEMPERATURE $V_O = \pm5V/10V$	INDUSTRIAL TEMPERATURE $V_O = \pm2.5V/5V$	COMMERCIAL TEMPERATURE $V_O = \pm5V/10V$	COMMERCIAL TEMPERATURE $V_O = \pm2.5V/5V$
±0.05	±15	——	——	DAC100AAQ7*	DAC100AAQ8*	——	——
±0.05	±30	——	——	DAC100ABQ7*	DAC100ABQ8*	——	——
±0.05	±60	DAC100ACQ5*	DAC100ACQ6*	DAC100ACQ7*	DAC100ACQ8*	DAC100ACQ3	DAC100ACQ4
±0.10	±30	DAC100BBQ5*	DAC100BBQ6*	DAC100BBQ7*	DAC100BBQ8*	——	——
±0.10	±60	DAC100BCQ5*	DAC100BCQ6*	DAC100BCQ7*	DAC100BCQ8*	DAC100BCQ3	DAC100BCQ4
±0.10	±120	——	——	——	——	DAC101EQ	——
±0.20	±60	DAC100CCQ5*	DAC100CCQ6*	DAC100CCQ7*	DAC100CCQ8*	DAC100CCQ3	DAC100CCQ4
±0.20	±120	——	——	——	——	DAC101EQ	——
±0.30	±120	——	——	DAC100DDQ7*	DAC100DDQ8*	DAC100DDQ3 DAC101FQ	DAC100DDQ4

*These devices supplied with MIL-STD-883 Class B Processing as standard — No suffix necessary.
†All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.
** Part number construction: The 1st letter following DAC-100 (A-D) refers to the non-linearity specification; the 2nd letter (A-D) refers to the full-scale tempco; the letter Q refers to the package; and the end numeral indicates the output voltage and temperature.

DICE CHARACTERISTICS

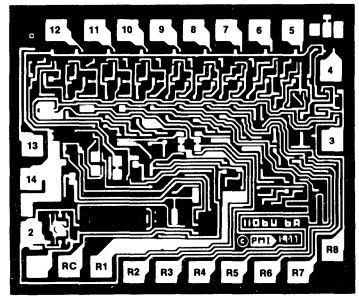


DIE SIZE 0.090 × 0.057 inch

1. R_B
2. V−
3. OUTPUT
15. FULL SCALE ADJ
16. R_S

R — Pads are connected to similarly marked pads on DAI-01

NOTE: Pads 4 — 14, See DAI-01



DIE SIZE 0.080 × 0.067 inch

2. V−
3. OUTPUT
4. BIT 10 (LSB)
5. BIT 9
6. BIT 8
7. BIT 7
8. BIT 6
9. BIT 5
10. BIT 4
11. BIT 3
12. BIT 2
13. BIT 1 (MSB)
14. V+

R — Pads are connected to similarly marked pads on DAR-01

NOTE:
Pads 1, 2, 15, 16, See DAR-01

Refer to Section 2 for additional DICE information

ELECTRICAL CHARACTERISTICS at 25° C; for the R2R Ladder Network comprised of R1-R8, R12, R34, R23, R45 and R56 when connected to an ideal DAI-01.

		DAR-01-N			DAR-01-G			DAR-01-GR			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Nonlinearity	VR1 = 3.2V	—	—	±0.035	—	—	±0.05	—	—	±0.1	%

ELECTRICAL CHARACTERISTICS at 25 °C in common to all grades; VR1 = 3.2V, unless otherwise noted.

		DAR-01			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resistance R1	Absolute Measurement	2.56	—	3.84	kΩ
Ratio RC1 to R1	Ideal = 1 to 1	−1.0	—	+1.0	%
Ratio R1 to RS1	Ideal = 1.31147 to 1	−1.0	—	+1.0	%
Ratio R1 to RS2	Ideal = 1.31147 to 1	−1.0	—	+1.0	%
Ratio RB to R1	Ideal = 1.9125 to 1	−1.0	—	+1.0	%

TYPICAL ELECTRICAL CHARACTERISTICS in common to all grades.

		DAR-01			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Absolute Temperature Coefficient	All Resistors	—	±120	—	ppm/°C
Tracking Temperature Coefficient	All Resistors with Respect to R1	—	3.0	—	ppm/°C

ELECTRICAL CHARACTERISTICS at 25 °C when connected to an ideal DAR-01.

			DAI-01-N			DAI-01-G			DAI-01-GR			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Nonlinearity		V_S = ±15V	—	—	±0.05	—	—	±0.10	—	—	±0.2	%
Internal Reference Voltage	V_{MCR}	V_S = ±15V	6.600	—	6.825	6.6	—	6.825	6.45	—	6.90	V

ELECTRICAL CHARACTERISTICS at 25 °C in common to all grades; V_S = +15V and when connected to an ideal DAR-01, unless otherwise noted.

		DAI-01			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		10	—	10	Bits
Analog Output Current	All Bits Low, V− Connected to FS Adjust	1840	—	2274	μA
Zero Scale Output Current	All Bits High, V− Connected to FS Adjust	—	—	±0.25	μA
Logic Input "0"	Measured with Respect to Output	—	—	0.7	V
Logic Input "1"	Measured with Respect to Output	2.1	—	—	V
Supply Current	All Bits High, V− Connected to FS Adjust	—	—	8.33	mA
Power Supply Rejection	V_S = ±6V to ±18V	—	—	0.1	%IFS/V

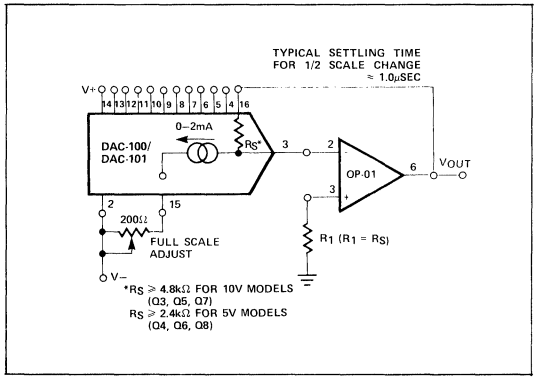
TYPICAL ELECTRICAL CHARACTERISTICS at V_S = ±15V, and when connected to an ideal DAR-01, unless otherwise noted.

		DAI-01-N			DAI-01-G			DAI-01-GR			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Full Scale Tempco	(Note)	—	±60	—	—	±60	—	—	±120	—	ppm/°C

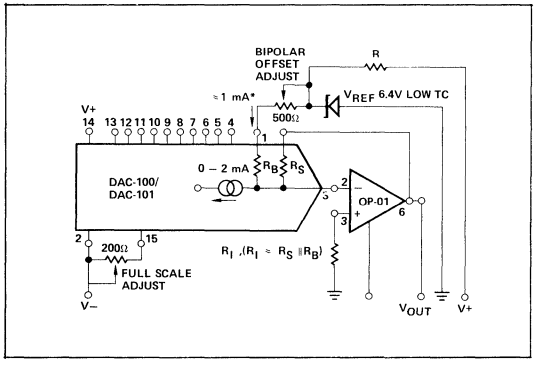
NOTE:
Full Scale Tempco is defined as the change in output voltage measured in the test circuit shown on the DAC-100 data sheet and is expressed in ppm between 25°C and either temperature extreme divided by the corresponding temperature change.

BASIC CONNECTIONS

BASIC UNIPOLAR VOLTAGE OUTPUT CIRCUIT



BASIC BIPOLAR VOLTAGE OUTPUT CIRCUIT

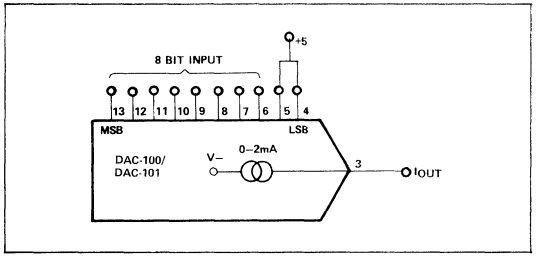


APPLICATIONS INFORMATION

FULL RANGE OUTPUT ADJUSTMENT — The output current of the DAC-100/DAC-101 may be reduced to produce an exact 10.000 (5.000) volt output by connecting a 200Ω adjustable resistance between the Full Scale Adjust pin and V– Adjustment should be made with an input of all "zeroes."

LOWER RESOLUTION APPLICATIONS — The DAC-100/DAC-101 may be used in applications requiring less than 10 bits of resolution. All unused logic inputs **must** be tied to the high logic for proper operation. "Floating" logic inputs can cause improper operation.

REDUCED RESOLUTION APPLICATION



LOGIC CODING — The DAC-100/DAC-101 uses complementary or inverted binary logic coding, i.e., an all "zeroes" input produces a full range output, while an all "ones" input produces a zero scale output. Each lesser significant bit's weight is one-half the previous more significant bit's value. High logic input turns the bit "OFF," low logic input level turns the bit "ON."

LOGIC COMPATIBILITY — The input logic levels are directly compatible with TTL logic and may also be used with CMOS logic powered from a single +5 volt supply.

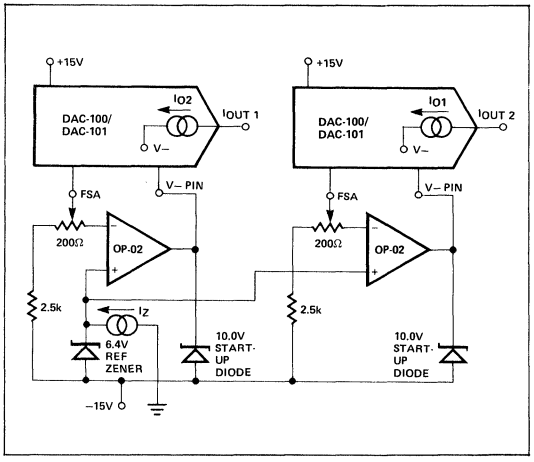
NONLINEARITY (NL) — The maximum deviation from an ideal straight line drawn between the end points, expressed as a percent of Full Scale Range (FSR) or given in terms of LSB value. The end points are zero scale output to full range output for unipolar operation and minus full scale to positive full range for bipolar operation.

BIPOLAR OPERATION — The DAC-100/DAC-101 may be converted to bipolar operation by injecting a half-scale current into the output; this is accomplished by connecting the internal bipolar resistor to a +6.4 volt reference. Trimming of the zero output may be facilitated by placing a 500Ω adjustable resistance in series with the +6.4 volts.

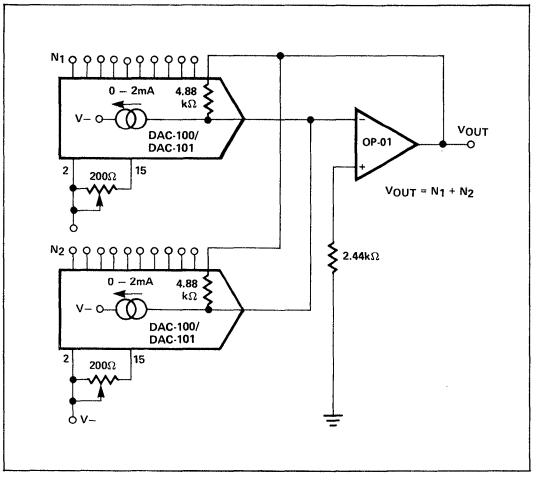
VOLTAGE AT OUTPUT PIN — The DAC-100/DAC-101 is designed to be operated with the voltage at the output pin held very close to zero volts. Input logic threshold levels are directly affected by output pin voltage changes; voltage swings at the output may cause loss of linearity due to improper switching of bits. Large voltage swings may cause permanent damage and should be avoided. Proper operation can be obtained with output voltages held within ±0.7 volts; a pair of back-to-back silicon diodes tied from the output ground is a convenient way of clamping the output to this limit.

TYPICAL APPLICATIONS

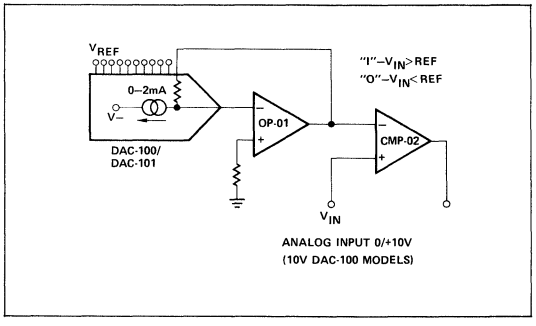
EXTERNAL REFERENCE CONNECTION



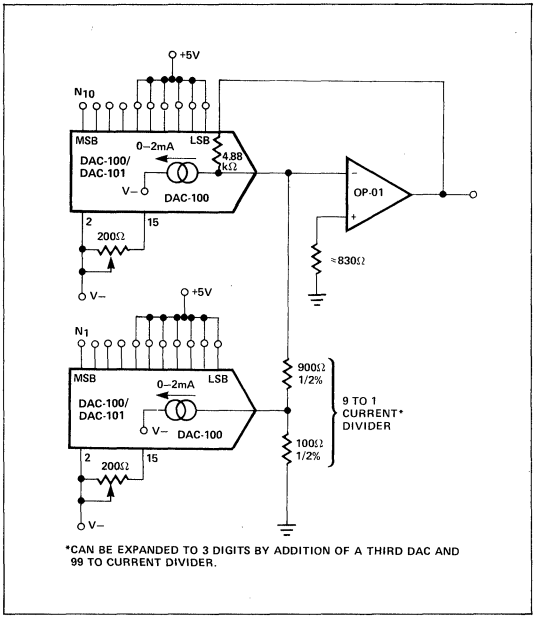
ANALOG SUM OF TWO DIGITAL NUMBERS



DIGITALLY PROGRAMMED LEVEL DETECTOR



BINARY-CODED-DECIMAL D/A CONVERSION



*CAN BE EXPANDED TO 3 DIGITS BY ADDITION OF A THIRD DAC AND 99 TO CURRENT DIVIDER.

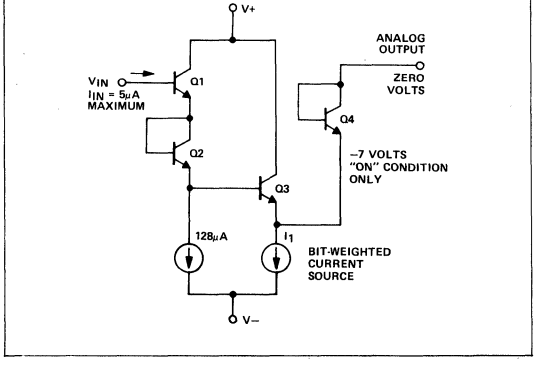
INTERFACING WITH CMOS LOGIC

The DAC-100/DAC-101 requires only about 1μA of input current into each logic stage. This enables use with CMOS inputs as long as one rule is observed; logic input voltages should not exceed 6.5 volts or V+, whichever is smaller. To provide an understanding of this rule, it is necessary to discuss the logic input stage design.

LOGIC INPUT STAGE DESIGN

For simplicity, only one of the ten identical input circuits is shown below. The DAC-100/DAC-101 uses a fast current-steering technique that switches a bit-weighted current

DAC-100 — LOGIC INPUT STAGE



between the positive supply (V+) and the analog output, which is usually constrained to be at zero volts (virtual ground) by an external summing amplifier.

Switching is accomplished by forward biasing Q4, a diode-connected transistor, for the bit "ON" condition and back biasing Q4 in the "OFF" condition. For the "ON" condition ($V_{IN} \leq 0.7$ volts), Q3 is "OFF" — all of the bit-weighted current, I_1, flows from the analog output through Q4 and ultimately to V−. In the "OFF" condition ($V_{IN} \geq 2.1$ volts), Q3 is "ON", Q4 is back biased, and the bit-weighted current is sourced from the positive power supply instead of the analog output.

If V_{IN} is too high, Q4's emitter-base junction will experience reverse breakdown and a fault condition will occur. Equation 1 describes this condition:

$$1)\ BV_{IH} = V_{BE1} + V_{BE2} + V_{BE3} + BV_{EB4} \cong 7.7 \text{ volts}$$

Using this relationship, it can be seen that a conservative input voltage limit would be around 6.5 volts. When the 6.5V input limit is observed, DAC-100/DAC-101 operation with CMOS inputs is easily achieved.

±6 VOLT POWER SUPPLY OPERATION

This is the most convenient method of interfacing the DAC-100 and DAC-101 with CMOS logic. At ±6 volts, DAC-100 and DAC-101 power dissipation is only 80mW, which is very small considering the inclusion of a complete internal reference. No interfacing components are required with ±5% power supplies, and the CMOS logic and DAC-100 or DAC-101 can use the same +6 volt power supply. In this application the device is directly CMOS compatible.

HIGH LEVEL CMOS INTERFACING

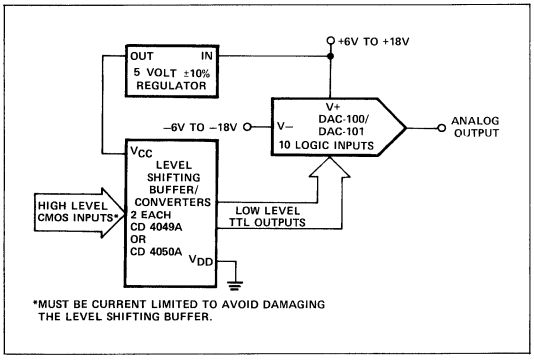
The block diagram below illustrates a convenient method for interfacing CMOS input levels between 6.5 volts and 15 volts with DAC-100 or DAC-101. Inexpensive and readily available CMOS hex buffer/converters step down the high-level inputs to TTL levels that cannot exceed 5 volts — clearly satisfying the input stage voltage rule.

In addition to level shifting, vuffer/converters provide input coding flexibility since they are available as inverting (CD4049A) or non-inverting (CD4050A) devices. This gives the user a choice between negative-true and positive-true binary coding and allows the same basic DAC-100 or DAC-101-to-CMOS interfacing method to be used in either type of application.

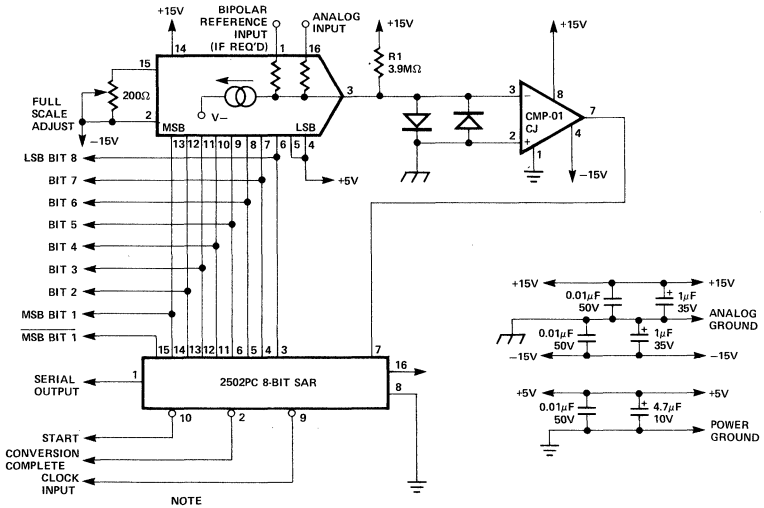
Since buffer/converter power consumption is very low, the required +5 volts can be provided by a simple regulator or even a resistive divider in some applications. In a multi-DAC system, one central, inexpensive three-terminal IC regulator can supply several level shifting devices.

NOTE: For a more complete explanation and detailed circuit connections, refer to AN-14, "Interfacing PMI D/As with CMOS Logic."

BLOCK DIAGRAM — CMOS TO DAC-100 INTERFACE

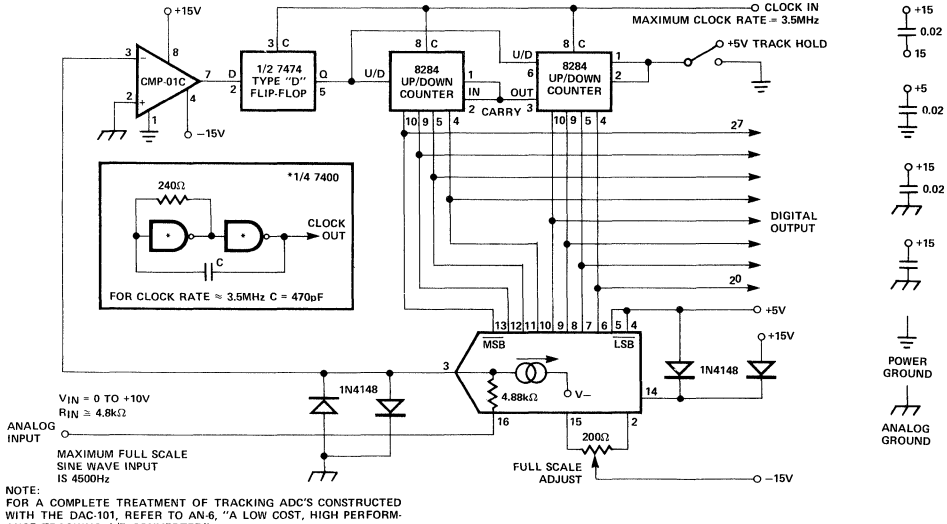


SUCCESSIVE APPROXIMATION A/D CONVERTER



NOTE
FOR A COMPLETE TREATMENT OF SA ADC'S CONSTRUCTED WITH THE DAC-100, REFER TO AN-11, "A LOW COST, EASY-TO-BUILD SUCCESSIVE APPROXIMATION A/D CONVERTER".

TRACKING (SERVO-TYPE) A/D CONVERTER



NOTE:
FOR A COMPLETE TREATMENT OF TRACKING ADC'S CONSTRUCTED WITH THE DAC-101, REFER TO AN-6, "A LOW COST, HIGH PERFORMANCE TRACKING A/D CONVERTER".

DAC-206

6-BIT VOLTAGE OUTPUT D/A CONVERTER

FEATURES

- **Complete** ..... **Includes Internal Reference**
- **6-Bit Resolution** ..... **7-Bit Accuracy**
- **3 Output Options** ..... **+10V, ±5V, ±10V**
- **Fast** ..... **3μs Settling Time**
- **Low Power Consumption** ..... **250mW Maximum**
- **Standard Power Supplies** ..... **±12V to ±18V**
- **TTL Compatible Logic Levels**

GENERAL DESCRIPTION

The DAC-206 is a monolithic 6-bit digital-to-analog converter that can be considered a complete D/A system. It features an internal reference and output amplifier that complement a fast 6-bit DAC. Wide applications flexibility is offered by the jumper selectable unipolar and bipolar binary coding format and output voltage range options. The addition of a seventh bit allows the resolution of this DAC to be brought in line with its accuracy. The DAC-206 offers high-speed operation in a highly accurate "complete" converter.

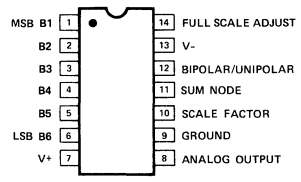
ORDERING INFORMATION†

	14 PIN DIP-HERMETIC	
FULL TEMP. N.L. LSB	**MILITARY TEMP.**	**COMMERCIAL TEMP.**
±1/2	DAC206AY*	DAC206EY
±3/4	DAC206BY*	DAC206FY

* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

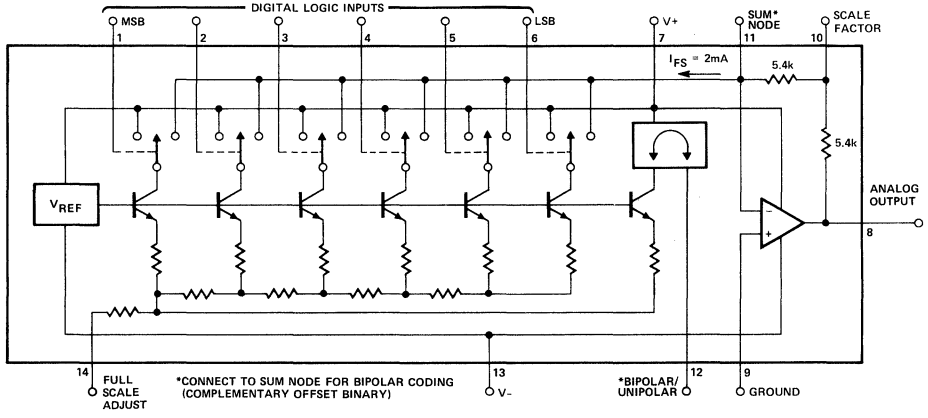
† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



14-PIN HERMETIC DIP (Y-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (See Note 3)

Operating Temperature
- DAC-206A, DAC-206B ..... −55°C to +125°C
- DAC-206E, DAC-206F ..... 0°C to +70°C

DICE Junction Temperature (T_j) ..... −65°C to +150°C
V+ Supply Voltage to Ground ..... 0 to +18V
V− Supply Voltage to Ground ..... 0 to −18V
Logic Input to Ground ..... −0.7 to +6V
Internal Power Dissipation (Note 1) 500mW
Storage Temperature ..... −65°C to +150°C
Lead Soldering Temperature (60 sec.) ..... 300°C
Output Short Circuit Duration (Note 2) ..... Indefinite

NOTES:
1. Rating applies up to ambient temperatures of 100°C. For temperatures above 100°C, derate linearly at 10mW/°C.
2. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
3. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

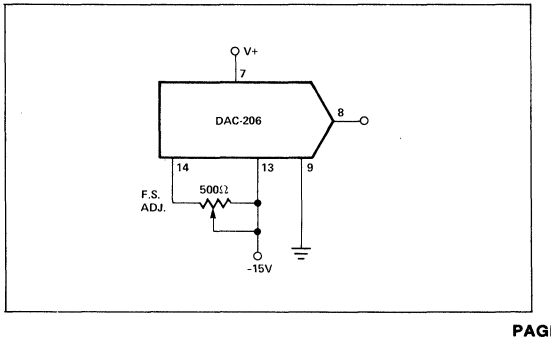
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, T_A = full operating range, unless otherwise noted.

			DAC206A/E			DAC206B/F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Nonlinearity	NL	$T_A = 25°C$ T_A = Full Operating Range	—	—	±1/4 ±1/2	—	—	±1/2 ±3/4	LSB
Full-Scale Tempco A-Suffix E-Suffix B- and F-Suffix	TC_{VFS}		—	—	80 120 —	—	—	— — 160	ppm/°C
Unipolar Zero Scale Output (Notes 1, 2)	V_{ZS}		—	±5.5	25	—	—	50	mV
Unipolar Full Range Output (Note 3)	V_{FR}	$R_L = 2k\Omega$, Pin 13 to 14 10 to 11, 12 to Ground	+10.00	—	+11.75	+10.00	—	+11.75	V
Bipolar Output Voltage (Note 3)	V_{FR} V_{FR}	±5V Range ±10V Range	— —	±10% ±11 ±10%	— —	— —	±5.5 ±10% ±11 ±10%	— —	V
Settling Time (Note 4)	t_s	To ±1/2 LSB	—	1.5	3	—	1.5	3	μs
Bipolar Offset Voltage (Note 1) $\pm 1/2 (\lvert V_{FR+} \rvert - \lvert V_{FS-} \rvert)$		Bit 1 = "0", Pin 11 shorted to 12 Pin 13 shorted to 14	—	—	±1	—	—	±1.5	LSB
Logic "0" Input Voltage	V_{INL}		—	—	0.8	—	—	0.8	V
Logic "1" Input Voltage	V_{INH}		2.0	—	—	2.0	—	—	V
Logic Input Current	I_{IN}	V_{IN} = 0V, each input	—	—	10	—	—	10	μA
Power Supply Sensitivity	P_{SS}	$\pm 12V \le V_S \le \pm 18V$, $V_{FR} \approx 10V$	—	—	0.15	—	—	0.2	%/%
Power Supply Current	I+ I−	V+ = +15V V− = −15V	— —	—	8 10	—	—	8 10	mA

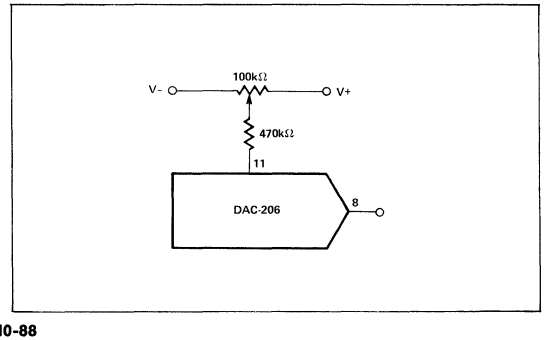
NOTES:
1. Zero scale or bipolar offset voltage can be trimmed to zero volts or to the exact one's or two's complement condition with an external resistor network to Pin 11.
2. Logic input voltage ≥ 2.0 volts.
3. Full scale is adjustable to precisely 10 volts for unipolar operation and 10 volt or 20 volt peak-to-peak bipolar operation with an external 500Ω potentiometer from Pin 14 to V−.
4. Guaranteed by design.

BASIC CIRCUIT CONNECTIONS

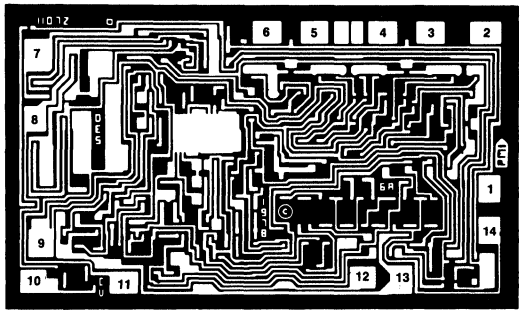
FULL SCALE ADJUSTMENT TECHNIQUE



OPTIONAL ZERO SCALE OR BIPOLAR OFFSET ADJUSTMENT



DICE CHARACTERISTICS



DIE SIZE 0.092 × 0.054 inch

1. B1 (MSB)
2. B2
3. B3
4. B4
5. B5
6. B6 (LSB)
7. V+
8. ANALOG OUTPUT
9. GROUND
10. SCALE FACTOR
11. SUM NODE
12. BIPOLAR/UNIPOLAR
13. V−
14. FULL SCALE ADJUST

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at 25° C.

PARAMETER	SYMBOL	CONDITIONS	DAC-206N BIPOLAR AND UNIPOLAR LIMIT	DAC-206G BIPOLAR AND UNIPOLAR LIMIT	UNITS
Nonlinearity	NL	$V_S = \pm 15V$	1/4	1/2	LSB MAX
Zero Scale Voltage	V_{ZS}	$V_S = \pm 15V$	25	50	mV MAX

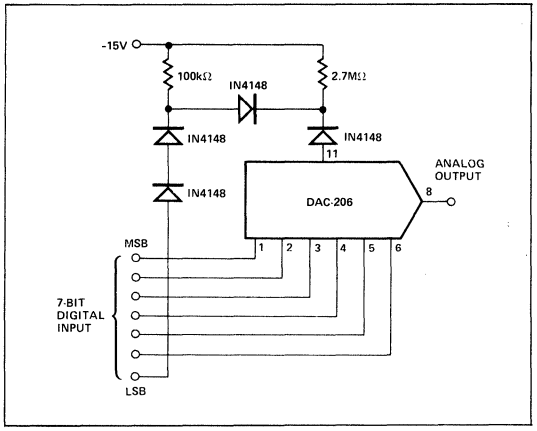
ELECTRICAL CHARACTERISTICS at 25° C for all grades; $V_S = \pm 15V$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-206 LIMIT	UNITS
Unipolar Full Scale Output Voltage (All Models)	V_{FR}	2kΩ Load, Logic ≤ 0.8V, Short V− to Full Scale Trim, Unipolar/ Bipolar to Ground, and Scale Factor to Sum Node	10.00 11.75	V MIN V MAX
Bipolar Output Voltage ±5 Volt Range ±10 Volt Range	V_{FR+} V_{FR-} V_{FR+} V_{FR-}	2kΩ Load, Short Sum Node to Unipolar/Bipolar. Short V− to Full Scale Trim and Scale Factor to Sum Node. Logic Inputs ≤ 0.8V Logic Inputs ≥ 2.0V Open Scale Factor Logic Inputs ≤ 0.8V Logic Inputs ≥ 2.0V	 +4.93 −5.94 +9.78 −11.89	 V MIN V MAX V MIN V MAX
Bipolar Offset Voltage $\pm 1/2\ (\lvert V_{FR+} \rvert - \lvert V_{FR-} \rvert)$		±5 Volt Range ±10 Volt Range	±1.5	LSB MAX
Resolution			6	Bits MAX
Logic Input "0"	V_{INL}		0.8	V MAX
Logic Input "1"	V_{INH}		2.0	V MIN
Logic Input Current, Each Input	V_{IN} = 0V		±8.0	μA MAX
Power Supply Rejection	PSR	$\pm 12V \le V_S \le \pm 18V$, $V_{FR} \cong 10.0V$	0.15	%FS/V MAX
Power Consumption	P_d	No Load	250	mW MAX

TYPICAL ELECTRICAL CHARACTERISTICS at 25° C.

PARAMETER	SYMBOL	CONDITIONS	DAC-206N TYPICAL	DAC-206G TYPICAL	UNITS
Settling Time	t_S	To ±1/2 LSB	1.5	1.5	μs
Full Scale Tempco	TCV_{FS}	$V_S = \pm 15V$	60	90	ppm/° C

ADDITION OF 7TH BIT



APPLICATIONS INFORMATION

INPUT CODES

The DAC-206 utilizes standard complementary binary coding for unipolar mode operation (all inputs high produces zero output voltage). Complementary offset binary coding may be implemented by shorting Pin 11 to Pin 12.

FULL SCALE ADJUST

A 500Ω pot from Pin 14 to V− can be used to adjust the full range output voltage to exactly 10 volts in unipolar mode or 10 to 20 volts peak-to-peak in bipolar mode. If no pot is used, tie Pin 14 to V−.

SCALE FACTOR

For +10 volt or ±5 volt outputs, short Pin 10 to Pin 11 (adjusts the feedback resistor around the output amplifier). For ±10 volt output, leave Pin 10 open. Intermediate output voltages may be obtained by placing a pot between Pin 10 and Pin 11, but this will seriously degrade the full-scale temperature coefficient due to the mismatch between the +1150ppm/°C tempco of the difussed resistors and the pot tempco.

CAPACITIVE LOADS

When driving capacitive loads greater than 50pF in unipolar mode or 30pF in bipolar mode a 100pF capacitor may be placed from Pin 11 to ground for added stability.

LOWER RESOLUTION APPLICATIONS

When less than 6 bits of resolution is required, tie off unused bits to a voltage level greater than +2.0 volts. The +5 volt logic supply is usually convenient.

DAC-208

9-BIT DIGITAL-TO-ANALOG CONVERTER (8 BITS PLUS SIGN)

FEATURES

- **Complete** . . . . . **Includes Reference and Op Amp**
- **Bipolar Output** . . . . . **Sign/Magnitude Coding**
- **User Selected +5V or ±10V Output**
- **No Bipolar Offset Adjustment Required**
- **8-Bit Non-Linearity Maintained over Full Temperature (0.1%)**
- **Multiplying Operation**
- **Fast** . . . . . **750ns Settling Time**
- **Monotonicity Guaranteed**
- **Models with MIL-STD-883 Class B Processing Available**

GENERAL DESCRIPTION

The DAC-208 is a complete, monolithic, 8-Bit Plus Sign DAC with a voltage output. A precision voltage reference, a logic-controlled polarity switch, and a high-speed (750ns settling time) output op amp are included. Non-linearity, monotonicity, and full-scale temperature coefficient are guaranteed over the full operating temperature range. Reliability is enhanced by a monolithic design and a hermetic DIP package. Two low-cost 0°/70°C and two −55°/+125°C models are available plus two models with MIL-STD-883 Class B processing. All bits are guaranteed monotonic.

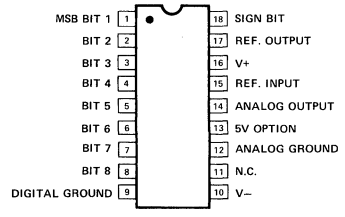
ORDERING INFORMATION†

	18 PIN HERMETIC DUAL-IN-LINE	
INL % FS	MILITARY TEMP	COMMERCIAL TEMP
0.1	DAC208AX*	DAC208EX
0.2	DAC208BX*	DAC208FX

* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

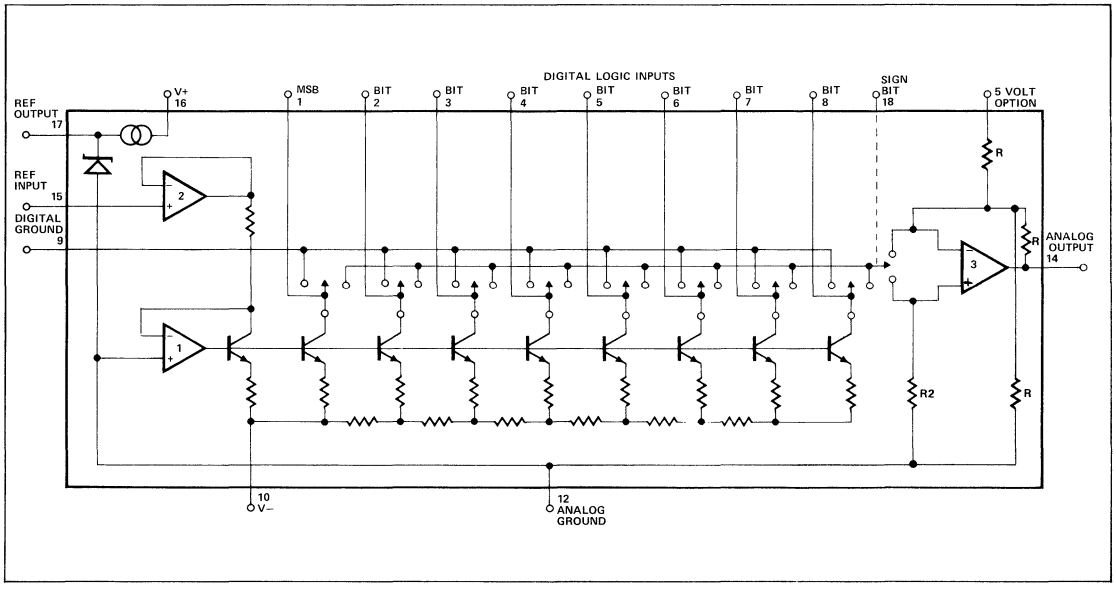
† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



18-PIN DIP (X-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range
DAC-208A,B ..... −55°C to +125°C
DAC-208E, F ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C
V+ Supply to Analog Ground ..... 0 to +18V
V− Supply to Analog Ground ..... 0 to −18V
Analog Ground to Digital Ground ..... 0 to ±0.5V
Logic Inputs to Digital Ground ..... −5V to (V_+ −0.7V)
Internal Reference Output Current 300μA
Reference Input Voltage ..... 0 to +10V
Internal Power Dissipation 500mW
Lead Soldering Temperature ..... 300°C (60 sec)
Output Short Circuit Duration ..... Indefinite
(Short circuit may be to ground or either supply.)

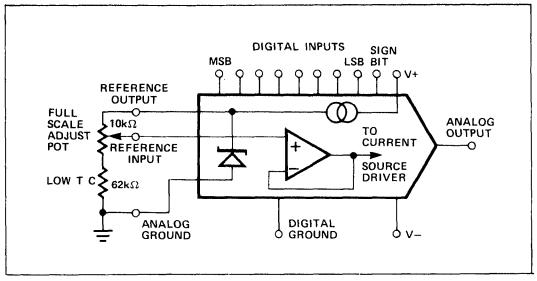
ELECTRICAL CHARACTERISTICS — MILITARY AND COMMERCIAL GRADES

at $V_S = \pm 15V$, $T_A = -55°C$ to $+125°C$ for A and B grades, $T_A = 0°C$ to $+70°C$ for E and F grades.

			DAC-208A, E			DAC-208B, F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Resolution		Including Sign	9	9	9	9	9	9	Bits
Monotonicity			8	—	—	8	—	—	Bits
Non-Linearity	NL	$T_A = 25°C$	—	—	±0.1	—	—	±0.2	%FS
		$T_A = 0°C$ - 70°C (E and F only)	—	—	±0.1	—	—	±0.2	
		$-55°C \le T_A \le +125°C$ (A + B Suffix Only)	—	—	±0.1	—	—	±0.2	
Zero Scale Offset Voltage	V_{ZS}	T_A = Full Range	—	—	—	—	—	—	%FS
			—	—	±0.1	—	—	±0.15	
Bipolar Full Range Voltage Symmetry	V_{FRS}	$T_A = 25°C$ ($V_{FR+} - V_{FR-}$)	—	—	60	—	—	70	mV
		T_A = Full Range	—	—	70	—	—	70	
Zero Scale Voltage Symmetry	V_{ZSS}	($V_{ZS+} - V_{ZS-}$) T_A = Full Range	—	—	1	—	—	2	mV
Gain Tempco	T_C	Internal Reference	—	—	40	—	—	60	ppm/°C
		External Reference	—	15	—	—	30	—	
Output Voltage Range	V_{OR+}		+10.0	—	+11.5	+10.0	—	+11.5	V
			+5.0	—	+5.75	+5.0	—	+5.75	
	V_{OR-}		−11.5	—	−10.0	−11.5	—	−10.0	
Differential Non-Linearity	DNL	$T_A = 25°C$	—	—	±1/2	—	—	1	LSB
Settling Time	t_s		—	750	—	—	750	—	ns
Reference Input Slew Rate	SR_{REF}		—	1.5	—	—	1.5	—	V/μs
Reference Input Impedance	Z_{IN}		—	200	—	—	200	—	MΩ
Reference Input Multiplying Range	IVR_m	For 0.1% Typical Non-Linearity	3	—	10	3	—	10	V
Reference Amplifier Bandwidth	BW		—	1	—	—	1	—	MHz
Reference Output Voltage	V_{REF}		—	7.6	—	—	7.6	—	V
DAC Output Current	I_O	For Stated Non-Linearity	0	—	10	0	—	10	mA
Reference Output Current	I_{REF}		—	100	—	—	100	—	μA
Output Slew Rate	SR_O		—	10	—	—	10	—	V/μs
Logic Input Current	I_{IN}	$-5V \le V_I \le V+ -0.7V$	—	±2.0	±10.0	—	±2.0	±10.0	μA
Logic "0" Voltage	V_{INL}		—	—	0.8	—	—	0.8	V
Logic "1" Voltage	V_{INH}		2.0	—	—	2.0	—	—	V
Power Supply Sensitivity	P_{SS}	T_A = Full Range	0.03	—	0.15	0.03	—	0.15	$\%V_{FS}/V$
Positive Supply Current	I+		—	7	9	—	7	9	mA
Negative Supply Current	I−		—	10	12	—	10	12	mA

CONNECTION INFORMATION

FULL SCALE ADJUSTMENT CIRCUIT



FULL SCALE ADJUSTMENT

Full Scale output voltage may be trimmed by use of a potentiometer and series resistor as shown; however, best results will be obtained if a low tempco resistor is used or if pot and resistor tempcos match. Alternatively, a single pot of $\geq 75k\Omega$ may be used.

REFERENCE INPUT BYPASS

Lowest noise and fastest settling operation will be obtained by bypassing the Reference Input to Analog Ground with a $0.01\mu F$ disk capacitor.

GROUNDING

For optimum noise rejection, separate digital and analog grounds have been brought out. Best results will be obtained if these grounds are connected together at one point only, preferably at the power supply, so that the large digital currents do not flow through the analog ground path.

APPLICATIONS INFORMATION

LOWER RESOLUTION APPLICATIONS

For applications not requiring full 8-bit resolution, unused logic inputs should be tied to ground.

UNIPOLAR OPERATION

Operation as a 8-bit straight binary converter may be implemented by permanently tying the Sign Bit to +5V (for positive Full Scale output).

+5 VOLT OUTPUT

The output voltage range can be changed to +5V by connecting the 5V option pin (pin 13) to the analog output (pin 14). The 5V option is unipolar only and will not function for negative outputs.

POWER SUPPLIES

The DAC-208 will operate within specifications for power supplies ranging from ±12V to ±18V for unipolar positive operation; and from ±13V to ±18V for bipolar. Power supplies should be bypassed near the package with a $0.1\mu F$ disk capacitor.

CAPACITIVE LOADING

The output operational amplifier provides stable operation with capacitive loads up to 100pF.

REFERENCE OUTPUT

For best results, Reference Output current should not exceed $100\mu A$.

INTERFACING WITH CMOS LOGIC

The DAC-208's logic input stages require about $1\mu A$ and are capable of operation with inputs between −5 volts and $V_+ - .7V$. This wide input voltage range allows direct CMOS interface with no additional components.

USE WITH EXTERNAL REFERENCES

Positive-polarity external reference voltages referred to Analog Ground may be applied to the Reference Input terminal to improve full scale tempco, to provide tracking to other system elements, or to slave a number of DAC-208's to the Reference Output of any one of them.

VARIABLE REFERENCES

Operation as a two-quadrant multiplying DAC is achieved by applying an analog input varying between 0 and +10V to the Reference Input terminal. The DAC output is then the scaled product of this voltage and the digital input.

SIGN PLUS MAGNITUDE CODING TABLE

	SIGN BIT	MSB							LSB
+FULL SCALE −1LSB	1	1	1	1	1	1	1	1	1
+HALF SCALE	1	1	0	0	0	0	0	0	0
ZERO SCALE (+)	1	0	0	0	0	0	0	0	0
ZERO SCALE (−)	0	0	0	0	0	0	0	0	0
−HALF SCALE	0	1	0	0	0	0	0	0	0
−FULL SCALE +1LSB	0	1	1	1	1	1	1	1	1

DAC-210

11-BIT DIGITAL-TO-ANALOG CONVERTER (10 BITS PLUS SIGN)

FEATURES

- **Complete ..... Includes Reference and Op Amp**
- **Bipolar Output ..... ±10V**
- **Sign-Magnitude Coding**
- **No Bipolar Offset Adjustment Required**
- **10-Bit Non-Linearity Maintained over Full Temperature (0.075%)**
- **Multiplying Operation**
- **Fast ..... 1.5μs Settling Time**
- **Monotonicity Guaranteed**
- **Reliable ..... 100% Burned-in 72 hrs. at +125°C**
- **Models with MIL-STD-883 Class B Processing Available**
- **Models with Guaranteed ±1 LSB Full Range Symmetry Available**

ORDERING INFORMATION †

		18 PIN HERMETIC DUAL INLINE PACKAGE	
TEMPCO	**INL**	**MILITARY***	**COMMERCIAL**
±40	±0.05	DAC210AX **DAC210ASX	DAC210EX *DAC210ESX
±60	±0.05	DAC210BX **DAC210BSX	DAC210FX *DAC210FSX
±30 Typ	±0.10		DAC210GX

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number.

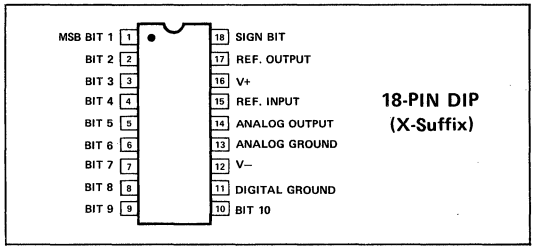
† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

**These parts are selected for ±10mV Full Range Voltage Symmetry error max.

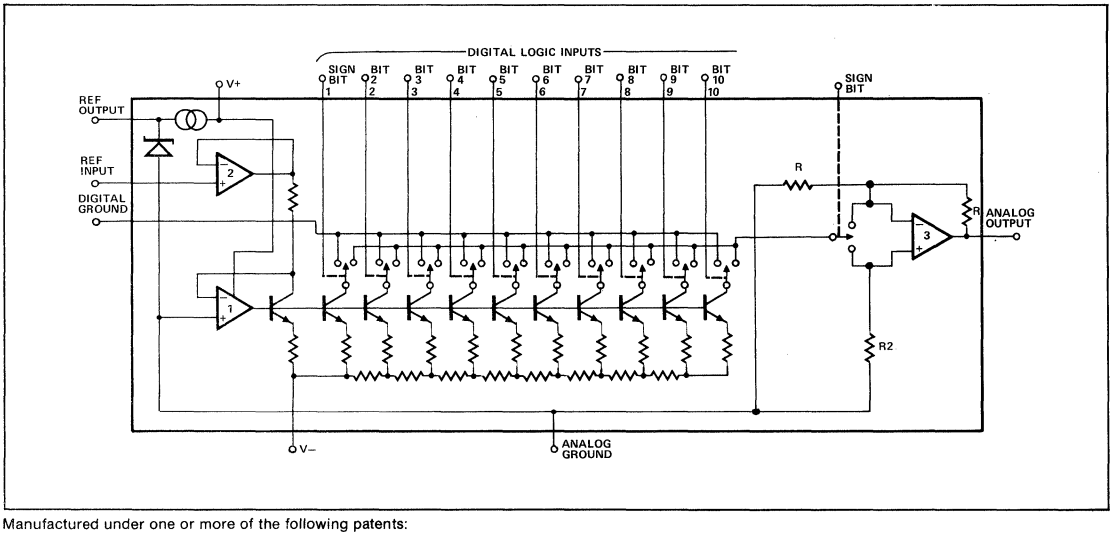
GENERAL DESCRIPTION

The DAC-210 is a complete, monolithic 10 Bit plus sign DAC with a ±10V Voltage output. A precision voltage reference, a logic controlled polarity switch and output amplifier are included. Non-linearity, monotonicity, and full-scale temperature coefficient are guaranteed over the full operating temperature range. Ease of application is achieved by the **total** D/A system specs given for non-linearity and zero-scale offset. System specs eliminate the complex error budget analysis required by less "complete" DACs. Sign Magnitude Coding minimizes the "Major-Carry" zero code errors inherent in offset coding schemes. Reliability is enhanced by a monolithic design, 100% burn-in, and a hermetic DIP package. MIL-STD-883 Class B processing is available on −55°C to +125°C grades. Also offered are models with a ±1 LSB Maximum Full Range Symmetry error.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



Manufactured under one or more of the following patents:
4,055,753; 4,056,740; 4,092,639

ELECTRICAL CHARACTERISTICS — MILITARY AND COMMERCIAL GRADES at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$, for A and B grades. $0°C \leq T_A \leq +70°C$ for E, F and G grades, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-210A,E MIN	DAC-210A,E TYP	DAC-210A,E MAX	DAC-210B,F MIN	DAC-210B,F TYP	DAC-210B,F MAX	DAC-210G MIN	DAC-210G TYP	DAC-210G MAX	UNITS
Resolution		Including Sign	11	11	11	11	11	11	11	11	11	Bits
Monotonicity			10	—	—	10	—	—	9	—	—	Bits
Non-Linearity	NL	$T_A = 25°C$	—	—	±0.05	—	—	±0.05	—	—	±0.10	%FS
		T_A = Full Range	—	—	±0.05	—	—	±0.10	—	—	—	
		T_A = Full Range (A or B only)	—	—	±0.075	—	—	±0.10	—	—	—	
Zero Scale Offset Voltage	V_{ZS}	$T_A = 25°C$	—	—	±0.05	—	—	±0.1	—	—	—	%FS
		T_A = Full Range	—	—	±0.06	—	—	±0.1	—	—	—	
Bipolar Full Range Voltage Symmetry ($V_{FR+} - \lvert V_{FR-} \rvert$)	V_{FRS}	$T_A = 25°C$ (Note 2)	—	—	40	—	—	60	—	—	80	mV
		T_A = Full Range	—	—	50	—	—	70	—	50	—	
Zero Scale Voltage Symmetry ($V_{ZS+} - V_{ZS-}$)	V_{ZSS}	T_A = Full Range	—	—	1	—	—	1	—	—	2	mV
Gain Tempco	T_C	Internal Reference	—	—	±40	—	—	±60	—	±30	—	ppm/°C
		External Reference	—	±15	—	—	±30	—	—	±30	—	
Output Voltage Range	$+V_{OR}$		+10.0	—	+11.5	+10.0	—	+11.5	+10.0	—	+11.5	V
	$-V_{OR}$		−11.5	—	−10.0	−11.5	—	−10.0	−11.5	—	−10.0	
Differential Non-Linearity	DNL	$T_A = 25°C$	—	—	±1	—	—	±1	—	±1	—	LSB
Settling Time	T_S		—	1.5	—	—	1.5	—	—	1.5	—	µs
Reference Input Slew Rate	SR_{REF}		—	1.5	—	—	1.5	—	—	1.5	—	V/µs
Reference Input Impedance	Z_{IN}		—	200	—	—	200	—	—	200	—	MΩ
Reference Input Multiplying Range	IVR_m	For 0.1% Typical Non-Linearity (Note 1)	3	—	10	3	—	10	3	—	10	V
Reference Amplifier Bandwidth	BW		—	1	—	—	1	—	—	1	—	MHz
Reference Output Voltage	V_{REF}		—	7.6	—	—	7.6	—	—	7.6	—	V
DAC Output Current	I_O	For Stated Non-Linearity (Note 1)	0	—	10	0	—	10	0	—	10	mA
Reference Output Current	I_{REF}	(Note 1)	—	—	100	—	—	100	—	—	100	µA
Output Slew Rate	SR_O		—	10	—	—	10	—	—	10	—	V/µs
Logic Input Current	I_{IN}	$-5V \leq V_I \leq V+$	—	±2.0	±10.0	—	±2.0	±10.0	—	±2.0	±10.0	µA
Logic "0" Input Voltage	V_{INL}		—	—	0.8	—	—	0.8	—	—	0.8	V
Logic "1" Input Voltage	V_{INH}		2.0	—	—	2.0	—	—	2.0	—	—	V
Power Supply Sensitivity	P_{SS}	$T_A = 25°C$	—	0.015	0.05	—	0.015	0.05	—	0.015	0.1	$\%V_{FS}/V$
		T_A = Full Range	—	0.015	0.1	—	0.015	0.1	—	0.015	0.1	$\%V_{FS}/V$
Positive Supply Current	I+		—	7	9	—	7	9	—	7	9	mA
Negative Supply Current	I−		—	−10	−12	—	−10	−12	—	−10	−12	mA

NOTES:

1. Guaranteed by design.
2. The DAC-210A, B, E, & F grades are available with ±10mV (±1 LSB or ±0.10%FS) Bipolar Full Range Voltage Symmetry. Part numbers for this option are DAC-210ASX, DAC-210BSX, DAC-210ESX and DAC-210FSX, respectively.

ABSOLUTE MAXIMUM RATINGS

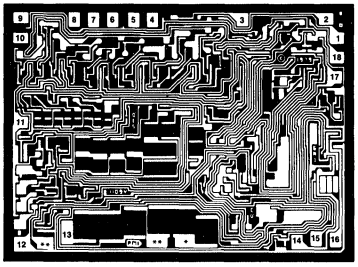
Operating Temperature Range
- DAC-210A,B ..... −55°C to +125°C
- DAC-210E,F,G ..... 0°C to +70°C

DICE Junction Temperature (T_j) ..... −65°C to +150°C
Storage Temperature Range ..... −65°C to +150°C
V+ Supply to Analog Ground ..... 0 to +18V
V− Supply to Analog Ground ..... 0 to −18V
Analog Ground to Digital Ground ..... 0 to ±0.5V
Logic Inputs to Digital Ground ..... −5V to (V_+ −0.7V)
Internal Reference Output Current 300μA
Reference Input Voltage ..... 0 to +10V
Internal Power Dissipation 500mW
Lead Soldering Temperature ..... 300°C (60 sec)
Output Short Circuit Duration ..... Indefinite
(Short circuit may be to ground or either supply.)

NOTE: Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

DICE CHARACTERISTICS

DIE SIZE 0.117 × 0.086 inch



Refer to Section 2 for additional DICE information.

1. B1 (MSB)
2. B2
3. B3
4. B4
5. B5
6. B6
7. B7
8. B8
9. B9
10. B10 (LSB)
11. DIGITAL GROUND
12. V−
13. ANALOG GROUND
14. ANALOG OUPUT
15. REFERENCE INPUT
16. V+
17. REFERENCE OUTPUT
18. SIGN BIT

NOTE:
For 5 volt output option (+5V only) * is connected to analog output. ** is connected to analog ground.

ELECTRICAL CHARACTERISTICS at 25°C; V_S = ±15V +10V Full Scale Output, unless otherwise noted.

PARAMETER	CONDITIONS	DAC-210N LIMIT	DAC-210G LIMIT	DAC-210GR LIMIT	UNITS
Resolution	Bipolar Output Unipolar Output	11 10	11 10	11 110	Bits MAX
Monotonicity		10	9	8	Bits MIN
Nonlinearity		±0.05	±0.1	±0.2	%FS MAX
Zero Scale Offset	Sign Bit High, All Other Inputs Low	±5	±10	±10	mV MAX
Zero Scale Symmetry	±10V Full Scale	±1.0	±2.0	±2.0	mV MAX
Full Scale Bipolar Symmetry	±10V Full Scale	±40	±80	±80	mV MAX
Power Supply Rejection	V_S = ±12V to ±18V	0.05	0.05	0.1	%V_{FS}/V MAX
Power Consumption	I_{OUT} = 0	300	300	300	mW MAX
Logic Input "0"		0.8	0.8	0.8	V MAX
Logic Input "1"		2.0	2.0	2.0	V MIN
Output Voltage Analog (All Bits High)	V+ (Sign Bit High) V− (Sign Bit Low)	11.5 10 −10 −11.5	11.5 10 −10 −11.5	11.5 10 −10 −11.5	V MAX V MIN V MAX V MIN
Differential Nonlinearity		±1	±1	±1	LSB MAX

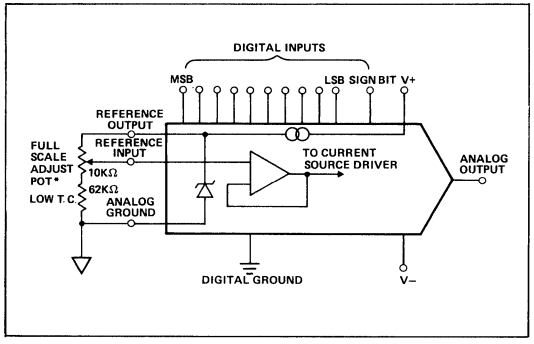
TYPICAL ELECTRICAL CHARACTERISTICS at V_S = ±15V and +10V Full Scale Output, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-210N TYPICAL	DAC-210G TYPICAL	DAC-210GR TYPICAL	UNITS
Full Scale Tempco	TCV_{FS}	Internal Reference	15	30	30	ppm/°C
Settling Time (T_A = 25°C)	t_S	To ±1/2 LSB 10 Volt Step	1.5	1.5	1.5	μs
Logic Input Current	T_A = 25°C	1.0	1.0	1.0	1.0	μA

CONNECTION INFORMATION

FULL SCALE ADJUSTMENT — Full Scale output voltage may be trimmed by use of a potentiometer and series resistor as shown; however, best results will be obtained if a low tempco resistor is used or if pot and resistor tempcos match. Alternatively, a single pot of ≥75kΩ may be used.

FULL SCALE ADJUSTMENT CIRCUIT

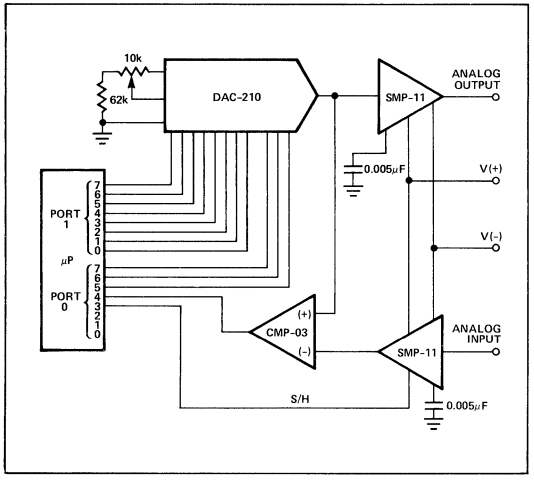


REFERENCE INPUT BYPASS — Lowest noise and fastest settling operation will be obtained by bypassing the Reference Input to Analog Ground with a 0.01μF disk capacitor.

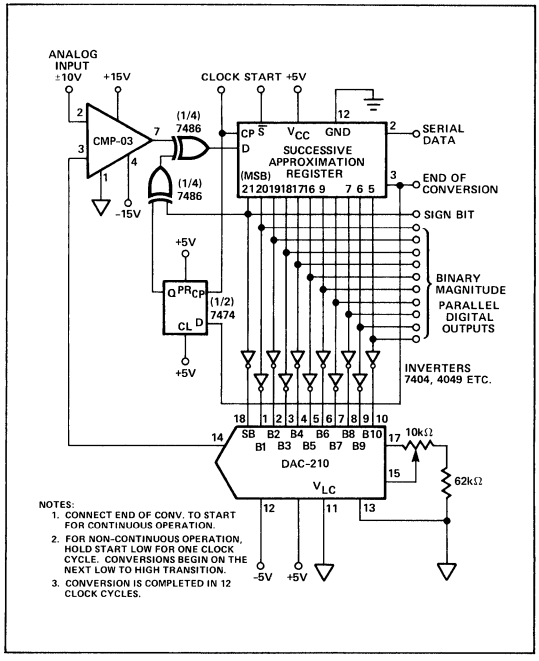
GROUNDING — For optimum noise rejection, separate digital and analog grounds have been brought out. Best results will be obtained if these grounds are connected together at one point only, preferably at the power supply, so that the large digital currents do not flow through the analog ground path.

TYPICAL APPLICATIONS

TIME MULTIPLEXED A/D CONVERTER



10-BIT SIGN-MAGNITUDE ADC



APPLICATIONS INFORMATION

LOWER RESOLUTION APPLICATIONS — For applications not requiring full 10-bit resolution, unused logic inputs should be tied to ground.

UNIPOLAR OPERATION — Operation as a 10-bit straight binary converter may be implemented by permanently tying the Sign Bit to +5V (for positive Full Scale output) or to ground (for negative Full Scale output).

POWER SUPPLIES — The DAC-210 will operate within specifications for power supplies ranging from ±12V to ±18V. Power supplies should be bypassed near the package with a 0.1μF disk capacitor.

CAPACITIVE LOADING — The output operational amplifier provides stable operation with capacitive loads up to 100pF.

REFERENCE OUTPUT — For best results, Reference Output current should not exceed 100μA.

INTERFACING WITH CMOS LOGIC — The DAC-210's logic input stages require about 1μA and are capable of operation with inputs between −5 volts and V+. This wide input voltage range allows direct CMOS interface with no additional components.

USE WITH EXTERNAL REFERENCES — Positive-polarity external reference voltages referred to Analog Ground may be applied to the Reference Input terminal to improve full

scale tempco, to provide tracking to other system elements, or to slave a number of DAC-210's to the Reference Output of any one of them.

VARIABLE REFERENCES — Operation as a two-quadrant multiplying DAC is achieved by applying an analog input varying between 0 and +10V to the Reference Input terminal. The DAC output is then the scaled product of this voltage and the digital input.

SIGN-MAGNITUDE CODING TABLE

	SIGN BIT	MSB									LSB
+ FULL SCALE −1LSB	1	1	1	1	1	1	1	1	1	1	1
+HALF SCALE	1	1	0	0	0	0	0	0	0	0	0
ZERO SCALE (+)	1	0	0	0	0	0	0	0	0	0	0
ZERO SCALE (−)	0	0	0	0	0	0	0	0	0	0	0
−HALF SCALE	0	1	0	0	0	0	0	0	0	0	0
− FULL SCALE +1LSB	0	1	1	1	1	1	1	1	1	1	1

DAC-312

12-BIT HIGH SPEED MULTIPLYING D/A CONVERTER

FEATURES

- **Guaranteed Differential Nonlinearity 0.025%**
- **Fast Settling Time 250ns**
- **High Compliance ..... −5V to +10V**
- **Differential Outputs ..... 0 to 4mA**
- **Guaranteed Monotonicity 12-Bits**
- **Low Full Scale Tempco ..... 10ppm/°C**
- **Circuit Interface to TTL, CMOS, ECL, PMOS/NMOS**
- **Low Power Consumption 225mW**

GENERAL DESCRIPTION

The DAC-312 series of 12 bit Multiplying Digital-to-Analog Converters provide high speed with guaranteed performance to 0.025% differential nonlinearity over the full operating temperature range.

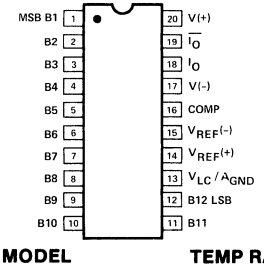
Based on the segmented design approach pioneered by PMI with the COMDAC™ line of Data Converters, the DAC-312 combines a 9 bit master D/A Converter with a three bit (MSB's) segment generator to form an accurate 12 bit D/A Converter at low cost. This technique guarantees a very uniform step size (up to ±1/2 LSB from the ideal), monotonicity to 12 bits and integral nonlinearity to 0.05% at its differential current outputs. In order to provide the same performance with a 12 bit R-2R ladder design, an integral nonlinearity over temperature of 1/2 LSB (0.012%) would be required.

The 250 ns settling time with low glitch energy and low power consumption are achieved by careful attention to the circuit design and stringent process controls. Direct interface with all popular logic families is achieved through the logic threshold terminal.

High compliance and low drift characteristics (as low as 10ppm/°C) are also features of the DAC-312 along with an excellent power supply rejection ratio of ±.001% FS/%ΔV. Operating over a power supply range of +5/−11V to ±18V the device consumes 225mW at the lower supply voltages with an absolute maximum dissipation of 375mW at the higher supply levels.

With their guaranteed specifications, single chip reliability and low cost, the DAC-312 device makes excellent building blocks for A/D Converters, Data Acquisition systems, video display drivers, programmable test equipment and other applications where low power consumption and complete input/output versatility are required.

PIN CONNECTIONS & ORDERING INFORMATION †



20 PIN HERMETIC DUAL IN LINE (R-SUFFIX)

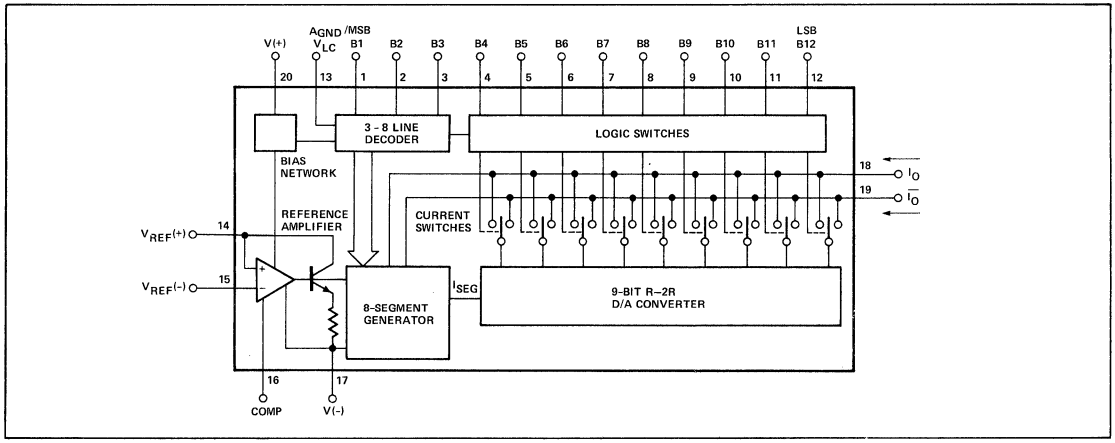
MODEL	TEMP RANGE	DNL
DAC312BR	−55°C/ +125°C	± 1 LSB
DAC312FR	0°C/+70°C	± 1 LSB

Military Temperature Range Devices
With MIL-STD-883 Class B Processing

MODEL	TEMP RANGE	DNL
DAC312BR/883	−55°C/+125°C	±1 LSB

† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

FUNCTIONAL DIAGRAM



Manufactured under one or more of the following patents:
4,055,773; 4,056,740; 4,092,639

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
- DAC-312B ..... −55°C to +125°C
- DAC312F ..... 0°C to +70°C

DICE Junction Temperature (T_j) ..... −65°C to +150°C
Storage Temperature ..... −65°C to +125°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Power Supply Voltage ..... ±18V
Logic Inputs ..... −5V to +18V
Analog Current Outputs ..... −8V to +12V
Reference Inputs V_{14}, V_{15} ..... V− to V+
Reference Input Differential Voltage (V_{14} to V_{15}) .... ±18V
Reference Input Current (I_{14}) 1.25mA

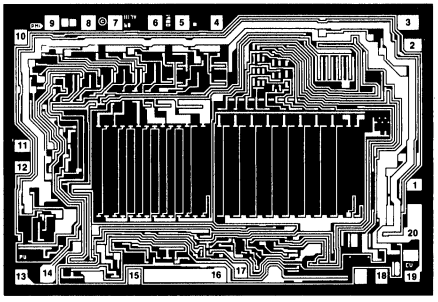
NOTE: Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 1.0mA$, $-55°C \le T_A \le 125°C$ for DAC-312B, $0°C \le T_A \le 70°C$ for DAC-312F, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-312B/F MIN	TYP	MAX	UNITS
Resolution			12	–	–	Bits
Monotonicity			12	–	–	Bits
Differential Nonlinearity	D.N.L.	Deviation from ideal step size	–	–	±.025	%FS
			–	–	±1.0	LSB
Nonlinearity	N.L.	Deviation from ideal straight line	–	–	±.05	%FS
Full Scale Current	I_{FS}	$V_{REF} = 10.000V$ $R_{14} = R_{15} = 10.000k\Omega$	3.935	3.999	4.063	mA
Full Scale Tempco	TCI_{FS}	(See Note)	–	±10	±40	ppm/°C
			–	±.001	±.004	%FS/°C
Output Voltage Compliance	V_{OC}	D.N.L. Specification guaranteed over compliance range	−5	–	+10	Volts
Full Scale Symmetry	I_{FSS}	$\lvert I_{FS} \rvert - \lvert \overline{I_{FS}} \rvert$	–	±0.4	±2.0	µA
Zero Scale Current	I_{ZS}		–	–	0.10	µA
Settling Time	t_S	To ±1/2 LSB, all bits switched ON or OFF (See Note)	–	250	500	ns
Propagation Delay — all bits	t_{PLH} t_{PHL}	All bits switched 50% point logic swing to 50% point output (See Note)	–	25	50	ns
Output Resistance	R_O		–	>10	–	MΩ
Output Capacitance	C_{OUT}		–	20	–	pF
Logic Input Levels "0"	V_{IL}	$V_{LC} = GND$	–	–	0.8	Volts
Logic Input Levels "1"	V_{IH}	$V_{LC} = GND$	2.0	–	–	Volts
Logic Input Current	I_{IN}	$V_{IN} = -5$ to +18V	–	–	40	µA
Logic Input Swing	V_{IS}		−5	–	+18	Volts
Reference Current Range	I_{REF}		0.2	1.0	1.1	mA
Reference Bias Current	I_{15}		0	−0.5	−2.0	µA
Reference Input Slew Rate	dI/dt	$R_{14(eq)} = 800\Omega$ $C_C = 0pF$ (See Note)	4.0	8.0	–	mA/µs
Power Supply Sensitivity	$PSSI_{FS+}$	V+ = +13.5V to +16.5V, V− = −15V	–	±0.0005	±.001	%FS/%ΔV
	$PSSI_{FS-}$	V− = −13.5V to −16.5V, V+ = +15V	–	±.00025	±.001	
Power Supply Range	V+	$V_{OUT} = 0V$	4.5	–	18	Volts
	V−		−18	–	−10.8	
Power Supply Current	I+	V+ = +5V, V− = −15V	–	3.3	7.0	mA
	I−		–	−13.9	−18.0	
	I+	V+ = +15V, V− = −15V	–	3.9	7.0	
	I−		–	−13.9	−18.0	
Power Dissipation	P_D	V+ = +5V, V− = −15V	–	225	305	mW
		V+ = +15V, V− = −15V	–	267	375	

NOTE: Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.140 × 0.095

1. B1 (MSB)
2. B2
3. B3
4. B4
5. B5
6. B6
7. B7
8. B8
9. B9
10. B10
11. B11
12. (LSB) B12
13. V_{LC}/A_{GND}
14. V_{REF} (+)
15. V_{REF} (−)
16. COMP
17. V −
18. I_O
19. $\overline{I_O}$
20. V +

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at 25° C; $V_S = \pm 15V$, and $I_{REF} = 1.0mA$, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

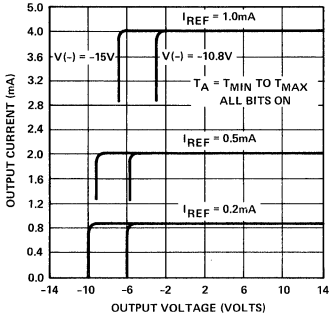
PARAMETER	SYMBOL	CONDITIONS	DAC-312N LIMIT	DAC-312G LIMIT	UNITS
Resolution			12	12	Bits MIN
Monotonicity			12	12	Bits MIN
Nonlinearity			±0.05	±0.05	%FS MAX
Output Voltage Compliance	V_{OC}	Full Scale Current Change <1/2 LSB	+10 −5	+10 −5	V MAX V MIN
Full Scale Current		$V_{REF} = 10.000V$ $R_{14}, R_{15} = 10.000k\Omega$	4.031 3.967	4.063 3.935	mA MAX mA MIN
Full Scale Symmetry	I_{FSS}		±1.0	±2.0	μA MAX
Zero Scale Current	I_{ZS}		0.1	0.1	μA MAX
Differential Nonlinearity	DNL	Deviation from ideal step size	±0.012 ±1/2	±0.025 ±1	%FS MAX Bits (LSB) MAX
Logic Input Levels "0"	V_{IL}	$V_{LC} = GND$	0.8	0.8	V MAX
Logic Input Levels "1"	V_{IH}	$V_{LC} = GND$	2.0	2.0	V MIN
Logic Input Swing	V_{IS}		+18 −5	+18 −5	V MAX V MIN
Reference Bias Current	I_{15}		−2.0	−2.0	μA MAX
Power Supply Sensitivity	$PSSI_{FS+}$ $PSSI_{FS-}$	V+ = +13.5V to +16.5V, V− = −15V V− = −13.5V to −16.5V, V+ = +15V	±.001 ±.001	±.001 ±.001	%/% MAX %/% MAX
Power Supply Current	I+ I−	$V_S = \pm 15V$ $I_{REF} \leq 1.0mA$	7 −18.0	7 −18.0	mA MAX mA MAX
Power Dissipation	P_D	$V_S = +15V$ $I_{REF} \leq 1.0mA$	375	375	mW MAX

ELECTRICAL CHARACTERISTICS at 25° C; $V_S = \pm 15V$, and $I_{REF} = 1.0mA$, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

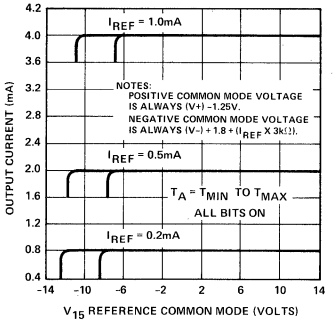
PARAMETER	SYMBOL	CONDITIONS	DAC-312N TYP	DAC-312G TYP	UNITS
Reference Input Slew Rate	dI/dt		8.0	8.0	mA/μs
Propagation Delay	t_{PLH}, t_{PHL}	Any Bit	25	25	ns
Settling Time	t_S	To ±1/2 LSB, All Bits Switched ON or OFF.	250	250	ns
Full Scale	TC_{IFS}		±10	±10	ppm/° C

TYPICAL PERFORMANCE CURVES

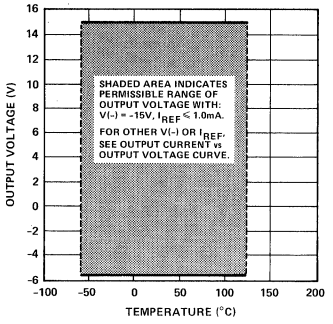
OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)



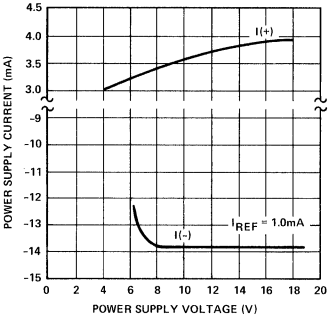
REFERENCE AMPLIFIER COMMON MODE RANGE



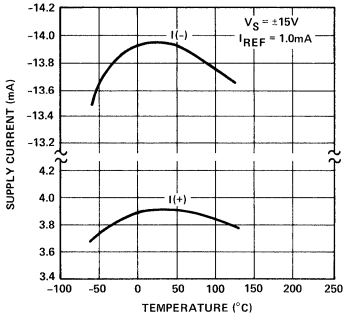
OUTPUT COMPLIANCE vs TEMPERATURE



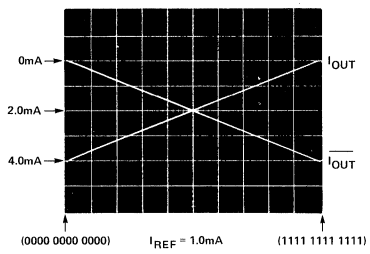
POWER SUPPLY CURRENT vs POWER SUPPLY VOLTAGE



POWER SUPPLY CURRENT vs TEMPERATURE

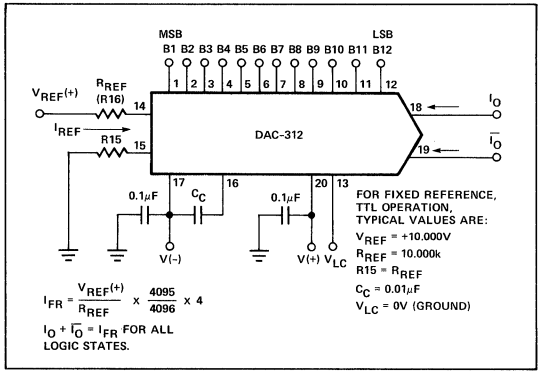


TRUE AND COMPLEMENTARY OUTPUT OPERATION

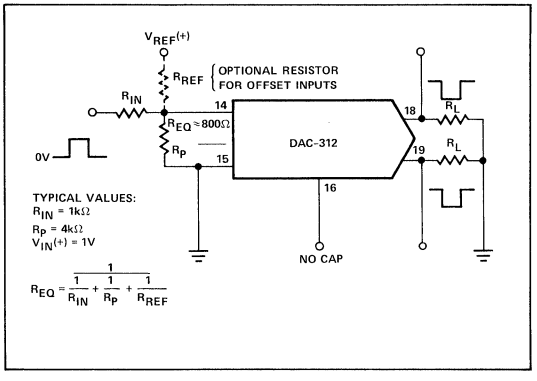


BASIC CONNECTIONS

BASIC POSITIVE REFERENCE OPERATION

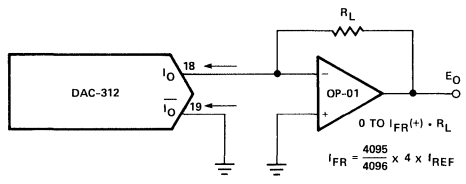


PULSED REFERENCE OPERATION



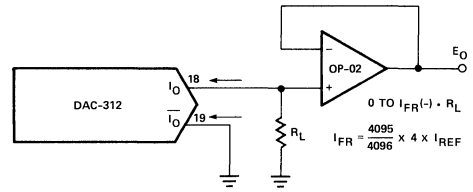
BASIC CONNECTIONS

NEGATIVE LOW IMPEDANCE OUTPUT OPERATION



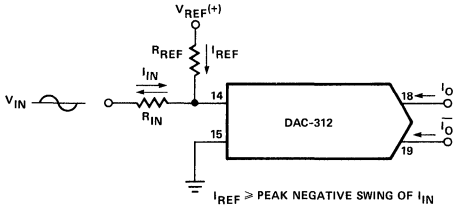
FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 19); CONNECT I_O (PIN 18) TO GROUND.

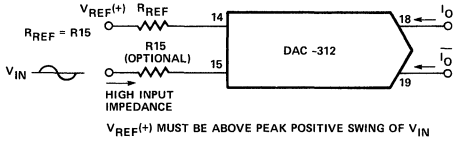
POSITIVE LOW IMPEDANCE OUTPUT OPERATION



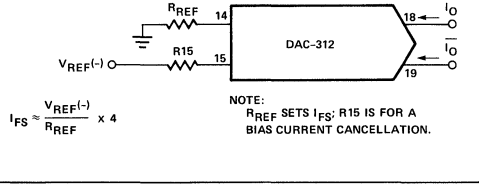
FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT NON-INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 19); CONNECT I_O (PIN 18) TO GROUND.

ACCOMODATING BIPOLAR REFERENCES

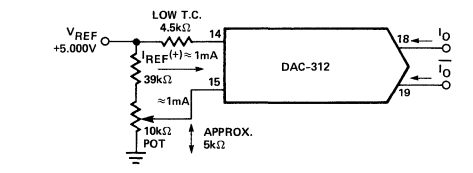




BASIC NEGATIVE REFERENCE OPERATION

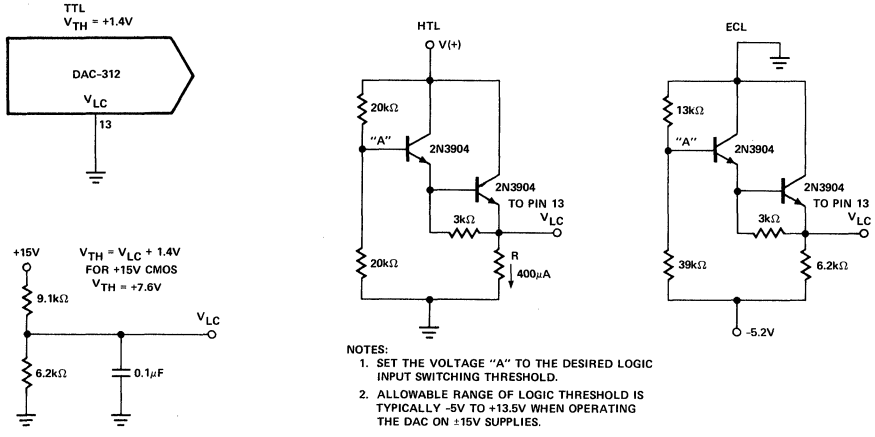


RECOMMENDED FULL SCALE ADJUSTMENT CIRCUIT



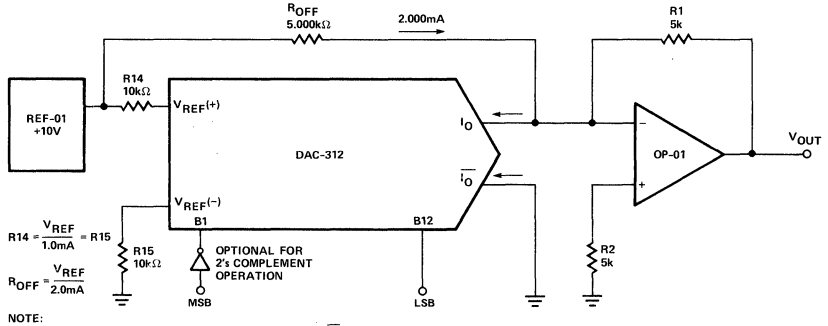
BASIC CONNECTIONS

INTERFACING WITH VARIOUS LOGIC FAMILIES



NOTES:
1. SET THE VOLTAGE "A" TO THE DESIRED LOGIC INPUT SWITCHING THRESHOLD.
2. ALLOWABLE RANGE OF LOGIC THRESHOLD IS TYPICALLY -5V TO +13.5V WHEN OPERATING THE DAC ON ±15V SUPPLIES.

BIPOLAR OFFSET (TRUE ZERO)

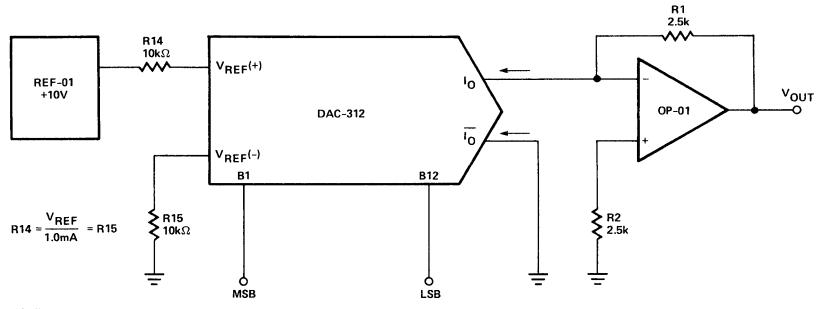


NOTE:
CODE MAY BE COMPLEMENTED BY REVERSING I_O & $\overline{I_O}$

CODE FORMAT	OUTPUT SCALE	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O (mA)	$\overline{I_O}$ (mA)	V_{OUT}
Offset binary;	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951
true zero output.	Positive full scale — LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
	+ LSB	1	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
	Zero scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.000
	- LSB	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-0.0049
	Negative full scale + LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	-9.9951
	Negative full scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	-10.000
2's complement;	Positive full scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951
true zero output	Positive full scale — LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
MSB complemented	+ 1 LSB	0	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
(need inverter at B1).	Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.000
	- 1 LSB	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-0.0049
	Negative full scale + LSB	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	-9.9951
	Negative full scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	-10.000

BASIC CONNECTIONS

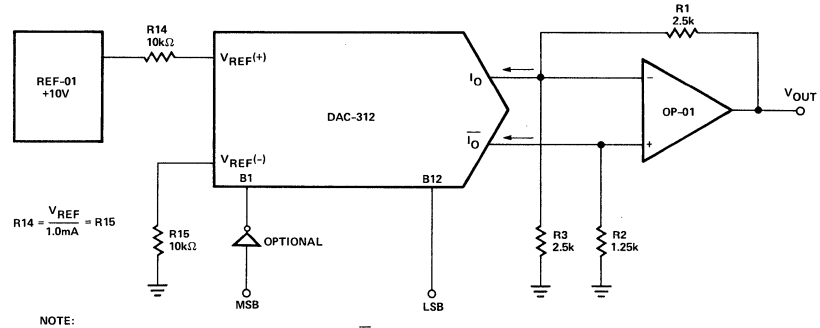
BASIC UNIPOLAR OPERATION



NOTE:
CODE MAY BE COMPLEMENTED BY REVERSING I_O & $\overline{I_O}$

CODE FORMAT	OUTPUT SCALE	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O (mA)	$\overline{I_O}$ (mA)	V_{OUT}
Straight binary;	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
unipolar with true input	Positive full scale — LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9951
code, true zero output.	LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	0.0024
	Zero Scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	0.0000
Complementary binary;	Positive full scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	9.9976
unipolar with	Positive full scale — LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	9.9951
complementary input	LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	0.0024
code, true zero output.	Zero scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	0.0000

SYMMETRICAL OFFSET OPERATION



NOTE:
CODE MAY BE COMPLEMENTED BY REVERSING I_O & $\overline{I_O}$

CODE FORMAT	OUTPUT SCALE	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O (mA)	$\overline{I_O}$ (mA)	V_{OUT}
Straight offset binary;	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
symmetrical about zero,	Positive full scale — LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
no true zero output.	(+) Zero scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
	(−) Zero scale	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−0.0024
	Negative full scale — LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	−9.9927
	Negative full scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	−9.9976
1's complement;	Positive full scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
symmetrical about zero,	Positive full scale — LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
no true zero output	(+) Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
MSB complemented	(−) Zero scale	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−0.0024
(need inverter at B1).	Negative full scale — LSB	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	−9.9927
	Negative full scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	−9.9976

APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SETUP

The DAC-312 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{4095}{4096} \text{ X } 4 \text{ X } (I_{REF}) = 3.999\, I_{REF},$$

where $I_{REF} = I_{14}$

In positive reference applications, an external positive reference voltage forces current through R14 into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15. Reference current flows from ground through R14 into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R15 (nominally equal to R14) is used to cancel bias current errors.

Bipolar references may be accomodated by offsetting V_{REF} or pin 15. The negative common-mode range of the reference amplifier is given by: V_{CM}–=V-plus (I_{REF}X 3kΩ) plus 1.8V. The positive common-mode range is V+ less 1.23V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R14 should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R14, or by using a potentiometer for R14. An improved method of full scale trimming which eliminates potentiometer T.C. effects is shown in the Recommended Full Scale Adjustment circuit.

The reference amplifier must be compensated by using a capacitor from pin 16 to V–. For fixed reference operation, a 0.01μF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications."

MULTIPLYING OPERATION

The DAC-312 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 1mA to 1μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 1.0mA.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V–. The value of this capacitor depends on the impedance presented to pin 14. For R14 values of 1.0, 2.5 and 5.0kΩ; minimum values of C_C are 5, 10, and 25pF. Larger values of R14 require proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R14 enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R14 = 1kΩ and C_C = 5pF, the reference amplifier slews at 4mA/ms enabling a transition from I_{REF} = 0 to I_{REF} = 1mA in 250ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full scale transition (0 to 1mA) occurs in 62.5ns when the equivalent impedance at pin 14 is 800Ω and C_C = 0. This yields a reference slew rate of 8mA/μs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The DAC-312 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 40μA logic input current, and completely adjustable logic threshold voltage. For V– = –15V, the logic inputs may swing between –5 and +10V. This enables direct interface with +15V CMOS logic, even when the DAC-312 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V– plus (I_{REF} X 3kΩ) plus 1.8V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 13, V_{LC}). The appropriate graph shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC}. For TTL interface, simply ground pin 13. When interfacing ECL, an $I_{REF} \leq$ 1mA is recommended. For interfacing other logic families, see block titled "Interfacing With Various Logic Families". For general setup of the logic control circuit, it should be noted that pin 13 will sink 1. 1mA typical; external circuitry should be designed to accommodate this current.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \overline{I_O} = I_{FR}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 18 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 18 and turned on at pin 19. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FR}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 25V above V– and is independent of the positive supply. Negative compliance is +10V above V–.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC-312 operates over a wide range of power supply voltages from a total supply of 20V to 36V. When operating with V– supplies of –10V or less, $I_{REF} \leq 1$mA is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at –9V with $I_{REF} =$ 1mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-312 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc. remain between acceptable limits.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-312 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is tight, typically ±10ppm/° C, with zero scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full scale drift. Settling times of the DAC-312 decrease approximately 10% at –55° C; at +125° C an increase of about 15% is typical.

SETTLING TIME

The DAC-312 is capable of extremely fast settling times, typically 250ns at $I_{REF} = 1.0$mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 25ns for each of the 12 bits. Settling time to within 1/2 LSB of the LSB is therefore 25ns, with each progressively larger bit taking successively longer. The MSB settles in 250ns, thus determining the overall settling time of 250ns. Settling to 10-bit accuracy requires about 90 to 130ns. The output capacitance of the DAC-312 including the package is approximately 20pF; therefore, the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 0.5mA, with gradual increases for lower I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±2μA, therefore a 2.5kΩ load is needed to provide adequate drive for most oscilloscopes. At I_{REF} values of less than 0.5mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 011111111111 to 100000000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.1% of the final value, and thus settling times may be observed at lower values of I_{REF}.

DAC-312 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference, and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1μF capacitors at the supply pins provide full transient protection.

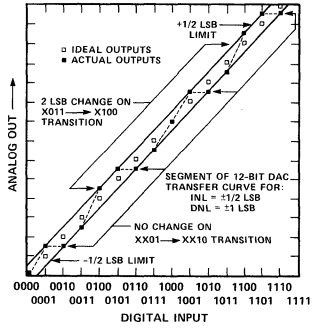
DIFFERENTIAL vs INTEGRAL NONLINEARITY

Integral nonlinearity, for the purposes of the discussion, refers to the "straightness" of the line drawn through the individual response points of a data converter. Differential nonlinearity, on the other hand, refers to the deviation of the spacing of the adjacent points from a 1 LSB ideal spacing. Both may be expressed as either a percentage of full scale output or as fractional LSBs or both. The following figures define the manner in which these parameters are specified. The left figure shows a portion of the transfer curve of a DAC with 1/2 LSB INL and the (implied) DNL spec of 1LSB. Below this is a graphic representation of the way this would appear on a CRT, for example, if the D/A Converter output were to be applied to the Y input of a CRT as shown in the application schematic titled "CRT Display Driver". On the right is a portion of the transfer curve of a DAC specified for 2LSB INL with 1/2 LSB DNL specified and the graphic display below it.

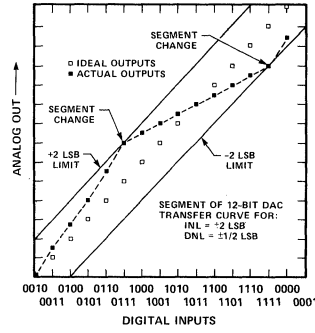
One of the characteristics of an R-2R DAC in standard form is that any transition which causes a zero LSB change (i.e. the same output for two different codes) will exhibit the same output each time that transition occurs. The same holds true for transitions causing a 2LSB change. These two problem transitions are allowable for the standard definition of monotonicity and also allow the device to be specified very tightly for INL. The major problem arising from this error type is in A/D converter implementations. Inputs producing the same output are now represented by ambiguous output codes for an identical input. Also, 2LSB gaps can cause large errors at those input levels (assuming 1/2 LSB quantizing levels). It can be seen from the two figures that the DNL specified D/A converter will yield much finer grained data than the INL specified part, thus improving the ability of the A/D to resolve changes in the analog input.

DIFFERENTIAL LINEARITY COMPARISON

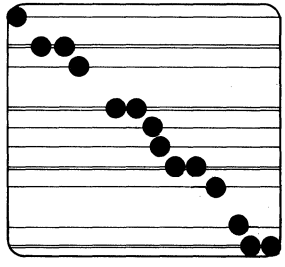
D/A CONVERTER WITH ±1/2 LSB INL, ±1 LSB DNL



D/A CONVERTER WITH ±2 LSB INL, ±1/2 LSB DNL

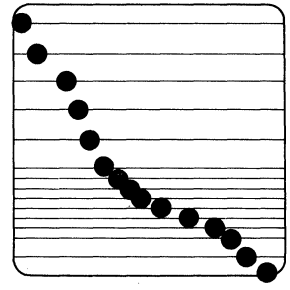


VIDEO DEFLECTION BY DAC's



ENLARGED "POSITIONAL" OUTPUTS

VIDEO DEFLECTION BY DAC's



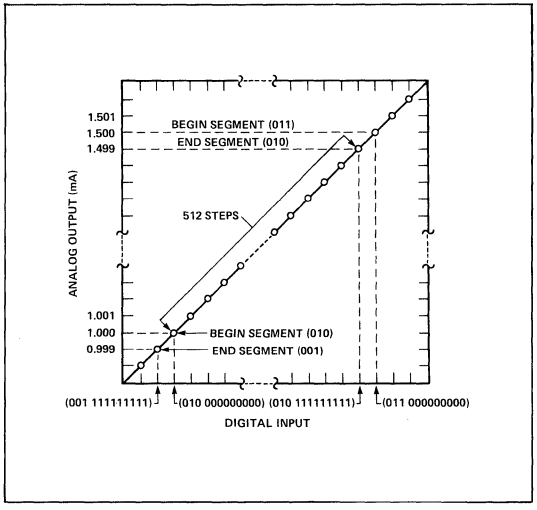
ENLARGED "POSITIONAL" OUTPUTS

DESCRIPTION OF OPERATION

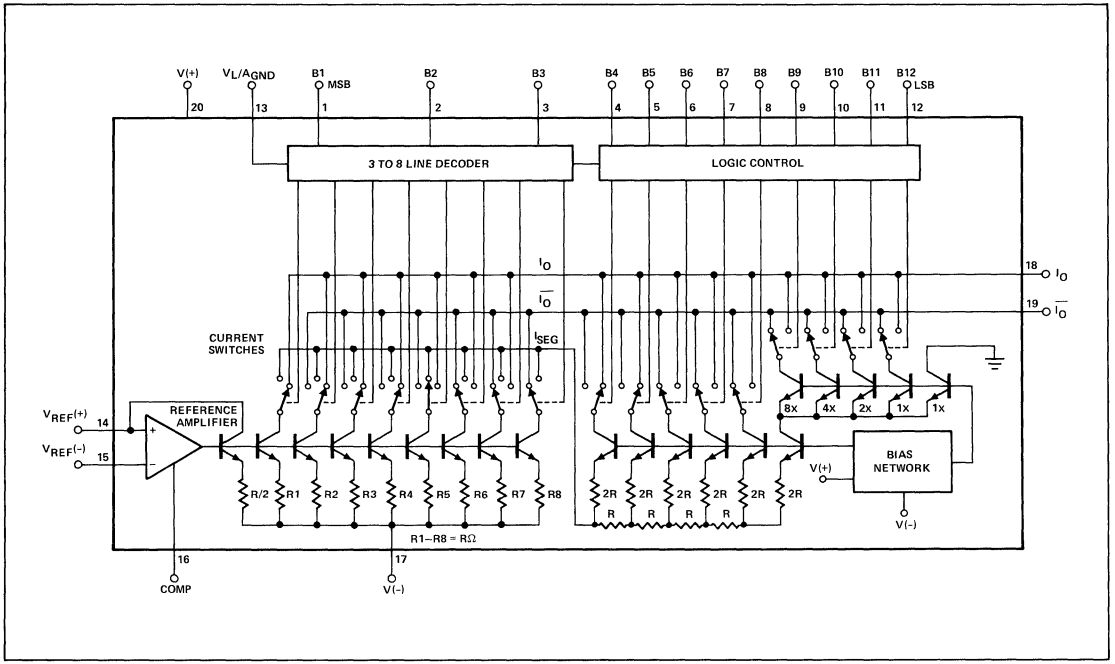
The DAC-312 is divided into two major sections, an 8-segment generator and a 9-Bit master/slave D/A Converter. In operation the device performs as follows (See Simplified Schematic):

The three most significant bits (MSB's) are inputs to a 3-to-8 line decoder. The selected resistor (R5 in the figure) is connected to the master/slave 9-Bit D/A Converter. All lower order resistors (R1 through R4) are summed into the I_O line, while all higher order resistors (R6 through R8) are summed into the $\overline{I_O}$ line. The R5 current supplies 512 steps of current (0 to 0.499mA for a 1mA reference current) which are also summed into the I_O or $\overline{I_O}$ lines depending on the bits selected. In the figure,the code selected is: 100 110000000. Therefore, 2mA (4 X 0.5mA/segment) +0.375mA (from master/slave D/A Converter) are summed into I_O giving an I_O of 2.375mA. $\overline{I_O}$ has a current of 1.625mA with this code. As the three MSB's are incremented, each successively higher code adds 0.5mA to I_O and subtracts 0.5mA from $\overline{I_O}$, with the selected resistor feeding its current to the master/slave D/A Converter; thus each increment of the 3 MSB's allows the current in the 9-Bit D/A Converter to be added to a pedestal consisting of the sum of all lower order currents from the segment generator. This configuration guarantees monotonicity.

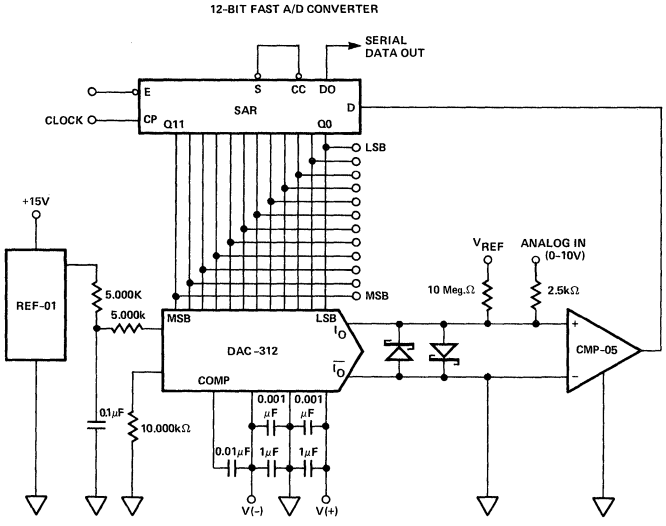
EXPANDED TRANSFER CHARACTERISTIC SEGMENT (001 010 011)



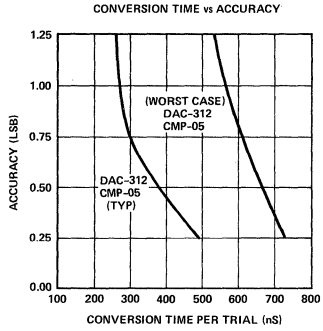
SIMPLIFIED SCHEMATIC



12-BIT FAST A/D CONVERTER



NOTE:
DEVICE(S) CONNECTED TO ANALOG INPUT MUST BE CAPABLE OF SOURCING 4.0mA. A BUFFER (eg. BUF-02) MAY BE REQUIRED.



CONVERSION TIME (nS)	TYP	WORST CASE
SAR	33	55
CMP-05	92	125
TOTAL	375nS	680nS
× 13	4.9μS	8.8μS

DAC-808

8-BIT HIGH-SPEED "MICROPROCESSOR COMPATIBLE" MULTIPLYING D/A CONVERTER

FEATURES

- **Dual 4-Bit Input Latch Coupled to 8-Bit Latched DAC**
- **8 and 4-Bit μP Compatible**
- **Easily Interfaced to 8080, and Z-80 Processors**
- **TTL Logic Compatible**
- **Programmable Mode Control**
- **High Output Impedance and Compliance**
- **Proven DAC-08 Analog Flexibility**
- **Nonlinearity to ±0.1% Maximum**
- **Low Power Dissipation 150mW**

GENERAL DESCRIPTION

The BYTEDAC™ DAC-808 is a Double-Buffered Latch Input Digital-to-Analog Converter designed specifically for 8- and 4-bit microprocessors. The double latch concept allows the processor to load data in the master latch without disturbing existing data in the slave latch which controls the analog output. The DAC-808 operates in five modes which are selected by the user under processor control. Data transfer is accomplished in two 4-bit nibbles, one 4-bit nibble, or one 8-bit byte.

The Analog section consists of a "Field-Proven" DAC-08 D/A Converter. Monotonic multiplying performance is attained over a wide 40 to 1 reference current range. Matching to within 1 LSB between reference and full-scale currents eliminates full-scale adjustments in most applications.

DAC-808 applications include graphic display drivers, high-speed modems, A/D converters, programmable waveform generators and power supplies, analog meter drivers, audio encoders and programmable attenuators, and other applications where low cost, high speed and double-buffering flexibility are required.

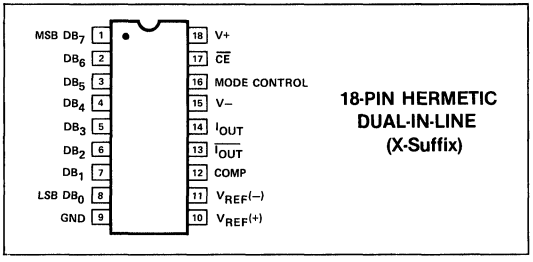
ORDERING INFORMATION†

INL	18 PIN HERMETIC DUAL INLINE PACKAGE		
% FS	MILITARY	INDUSTRIAL	COMMERCIAL
± 0.1	DAC-808A*	DAC-808EX	———
± 0.19	DAC-808BX*	DAC-808FX	———
± 0.39	———	———	DAC-808GX

* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

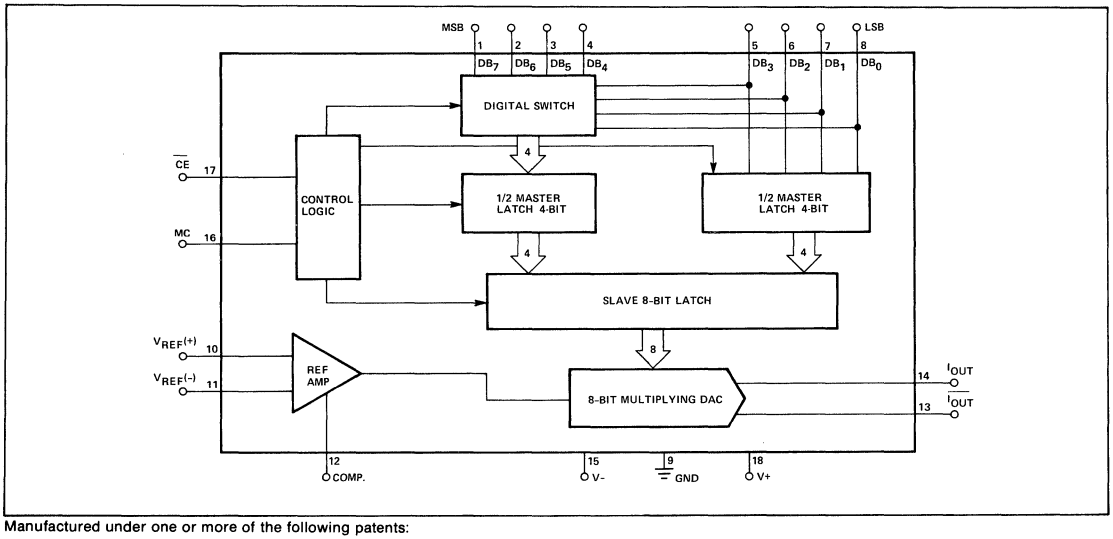
† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



18-PIN HERMETIC DUAL-IN-LINE (X-Suffix)

EQUIVALENT CIRCUIT



Manufactured under one or more of the following patents:
4,055,773; 4,056,740; 4,092,639

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
- DAC-808A/B ..... −55°C to +125°C
- DAC-808E/F ..... −25°C to +85°C
- DAC-808G ..... 0°C to +70°C

Dice Junction Temperature ..... −65°C to +150°C
Storage Temperature ..... −65°C to +150°C
Power Dissipation 300mW
Derate above 100°C ..... 10mW/°C
Lead Soldering Temperature ..... 300°C (60 sec)

V+ Supply to V− Supply 18.1V
Logic Inputs ..... 0V to 5.5V
Analog Current Outputs ..... −5mA
Reference Inputs (V_{14}, V_{15}) ..... V− to V+
Reference Input Differential Voltage (V_{14} to V_{15}) ..... ±15V
Reference Input Current 5.0mA

NOTE: Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V+ = +5V, V− = −12V, I_{REF} = 2.0mA, T_A = −55°C to +125°C for DAC-808A/B, unless otherwise noted. T_A = −25°C to +85°C apply for DAC-808E/F; T = 0°C to +70°C apply for DAC-808G. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

			DAC-808A/E			DAC-808B/F			DAC-808G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Resolution			8	8	8	8	8	8	8	8	8	Bits
Monotonicity			8	8	8	8	8	8	8	8	8	Bits
Nonlinearity			—	—	±0.1	—	—	±0.19	—	—	±0.39	%FS
Full Scale Tempco	TCI_{FS}	See Note	—	±10	±50	—	±10	±80	—	±10	±80	ppm/°C
Output Voltage Compliance	V_{OC}	Full Scale Current Change < ½ LSB	−5	—	+8	−5	—	+8	−5	—	+8	V
Output Impedance	R_{OUT}		—	>20	—	—	>20	—	—	>20	—	MΩ
Full Range Current	I_{FR14}	V_{REF} = 5.00V R_{11},R_{10} = 2.500kΩ T_A = 25°C	1.94	1.99	2.04	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Range Symmetry	I_{FRS}	I_{FR14}-I_{FR13}	—	±1.0	±8.0	—	±1.0	±8.0	—	±1.0	±8.0	μA
Zero Scale Current	I_{ZS}		—	0.2	2.0	—	0.2	2.0	—	0.2	2.0	μA
Output Current Range	I_{FSR}	V− = −12V	0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	mA
Reference Bias Current	I_B		—	−1.0	−3.0	—	−1.0	−3.0	—	−1.0	−3.0	μA
Reference Input Slew Rate	dI/dt	See Note	4.0	8.0	—	4.0	8.0	—	4.0	8.0	—	mA/μs
Power Supply Sensitivity	$PSSI_{FR+}$	V+ = 4.5V to 5.5V	—	±0.0003	±0.01	—	0.0003	±0.01	—	±0.0003	±0.01	$\%\Delta I_{FS}$ / $\%\Delta V+$
	$PSSI_{FR-}$	V− = −4.5V to −12V I_{REF} = 1mA	—	±0.002	±0.01	—	±0.002	±0.01	—	±0.002	±0.01	$\%\Delta I_{FS}$ / $\%\Delta V-$
Power Supply Current	I+	V_S = +5V, −12V	—	12	16	—	12	16	—	12	16	mA
	I−	I_{REF} = 2.0mA	—	6	9	—	6	9	—	6	9	
Power Dissipation	P_d	+5V, −12V, I_{REF} = 2.0mA	—	120	170	—	120	170	—	120	170	mW
Logic Input Levels												
Logic Input "0"	V_{IL}		—	—	0.8	—	—	0.8	—	—	0.8	V
Logic Input "1"	V_{IH}		2.0	—	—	2.0	—	—	2.0	—	—	

NOTE: Not 100% tested, guaranteed by design.

ELECTRICAL CHARACTERISTICS — A.C. PARAMETERS $V_S = +5V, -10V$, $I_{REF} = 2.0mA$, $T_A = 25°C$, unless otherwise noted.

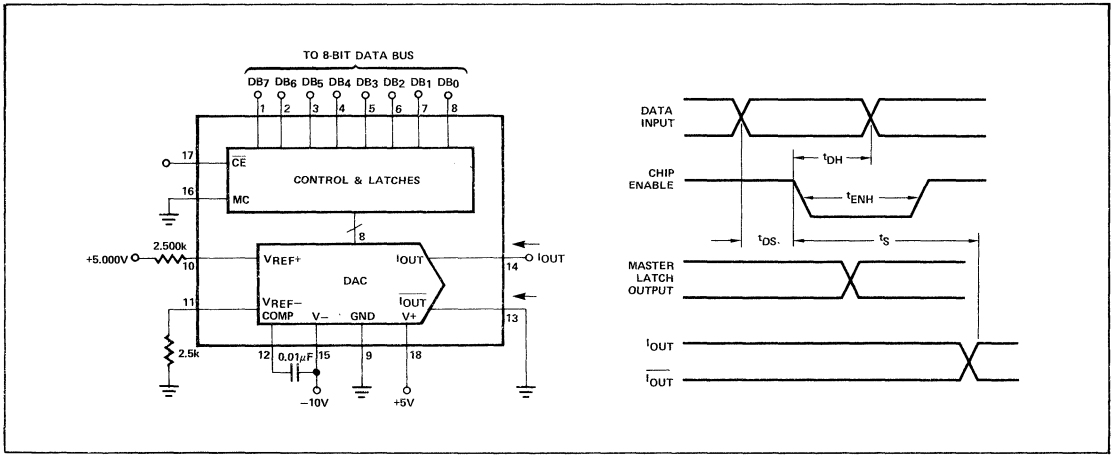
PARAMETER	SYMBOL	CONDITIONS	DAC-808A/E MIN	DAC-808A/E TYP	DAC-808A/E MAX	DAC-808B/F MIN	DAC-808B/F TYP	DAC-808B/F MAX	UNITS
Settling Time	t_s	From CE Negative Edge to ± ½ LSB, All Bits Switched ON or OFF, See Note	—	300	500	—	300	500	ns
Data Input Setup Time	t_{DS}	See Note	50	30	—	50	30	—	ns
Data Input Hold Time	t_{DH}	See Note	—	30	100	—	30	100	ns
Address Input Setup Time (Bits 7 and 6)	t_{AS}	4-Bit Mode, See Note	150	100	—	150	100	—	ns
Address Hold Time	t_{AH}	4-Bit Mode, See Note	—	0	10	—	0	10	ns
Chip Enable Negative Hold Time	t_{ENH}	See Note	250	100	—	250	100	—	ns
Chip Enable Positive Hold Time	t_{EPH}	See Note	350	200	—	350	200	—	ns

NOTE:
Guaranteed by design.

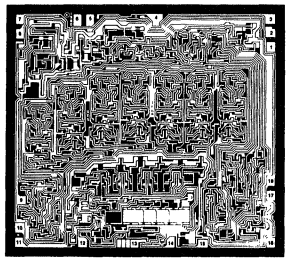
DAC-808 PIN DESCRIPTION

SYMBOL	DESCRIPTION
DB_0-DB_7	DATA BIT — Bits 0-7 are digital, active-high inputs that have DB_7 assigned the MSB.
CE	CHIP ENABLE — An active-low input control serving a dual purpose in that it's both the device enable and chip write input terminal.
MC	MODE CONTROL — A control that places the DAC in 8-bit operation when low and 4-bit operation when high.
I_{OUT}-$\overline{I_{OUT}}$	CURRENT OUTPUT — Complementary current outputs when added equal I_{FS}.
V_{REF-}, V_{REF+}	VOLTAGE REFERENCE — Differential inputs that accept a negative, positive, or bipolar input and are used to adjust I_{FS}.
COMP	COMPENSATION — The reference amplifier frequency compensating terminal.

FUNCTIONAL DIAGRAM AND TIMING DIAGRAM FOR 8-BIT OPERATION



DICE CHARACTERISTICS



1. DB7 (MSB)
2. DB6
3. DB5
4. DB4
5. DB3
6. DB2
7. DB1
8. DB0 (LSB)
9. GROUND
10. $V_{REF}(+)$
11. $V_{REF}(-)$
12. COMP
13. $\overline{I_{OUT}}$
14. I_{OUT}
15. V
16. MODE CONTROL
17. $\overline{CE}$
18. V+

DIE SIZE 0.138 × 0.125 inch

Refer to Section 2 for additional DICE information.

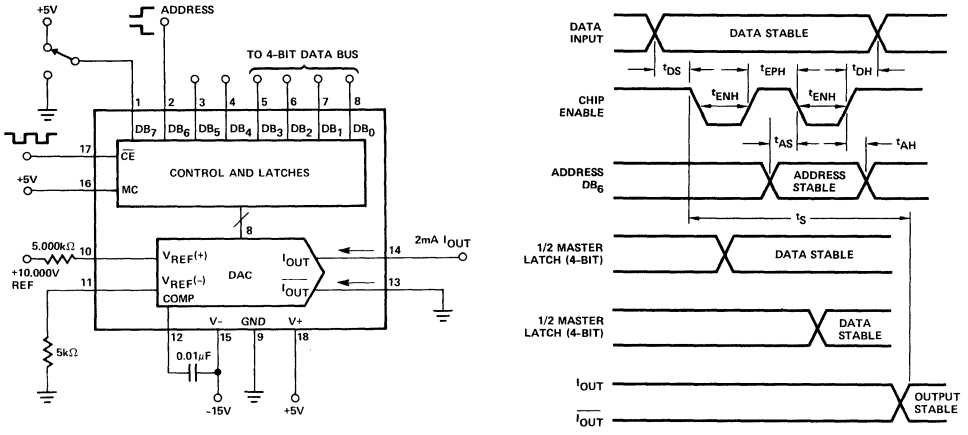
ELECTRICAL CHARACTERISTICS at 25°C; V_S = +5V, −12V and I_{REF} = 2.0mA, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-808N LIMIT	DAC-808G LIMIT	DAC-808GR LIMIT	UNITS
Resolution			8	8	8	Bits MIN
Monotonicity			8	8	8	Bits MIN
Nonlinearity			±0.1	±0.19	±0.39	%FS MAX
Output Voltage Compliance	V_{OC}	Full Scale Current Change < 1/2 LSB R_{OUT} > 20 MΩ Typ.	+8 −5	+8 −5	+8 −5	V MAX V MIN
Full Range Current	I_{FR14}	V_{REF} = 5.00V R_{11}, R_{10} = 2.500kΩ T_A = 25°C	2.04 1.94	2.04 1.94	2.04 1.94	mA MAX mA MIN
Full Range Symmetry	I_{FRS}	I_{FR14}-I_{FR13}	±8.0	±8.0	±8.0	μA MAX
Zero Scale Current	I_{ZS}		2.0	2.0	2.0	μA MAX
Output Current Range	I_{FSR}	V− = −12V	2.1 0	2.1 0	2.1 0	mA MAX mA MIN
Reference Bias Current	I_B		−3.0	−3.0	−3.0	μA MAX
Power Supply Sensitivity	$PSSI_{FR+}$ $PSSI_{FR-}$	V+ = 4.5V to 5.5V V− = −4.5V to −12V I_{REF} = 1mA	±0.01 ±0.01	±0.01 ±0.01	±0.01 ±0.01	$\%\Delta I_{FS}/\%\Delta V+$ MAX $\%\Delta I_{FS}/\%\Delta V-$ MAX
Power Supply Current	I+ I−	V_S = +5V, −12V I_{REF} = 2.0mA	16 9	16 9	16 9	mA MAX mA MAX
Power Dissipation	P_d	+5V, −12V, I_{REF} = 2.0mA	170	170	170	mW MAX
Logic Input Levels Logic Input "0" Logic Input "1"	 V_{IL} V_{IH}		 0.8 2.0	 0.8 2.0	 0.8 2.0	 V MAX V MIN

TYPICAL ELECTRICAL CHARACTERISTICS at 25° C; V_S = +5V, −12V, I_{REF} = 2.0mA, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-808 TYP	UNITS
Reference Input Slew Rate	dI/dt		8.0	mA/μs
Settling Time	t_S	From CE Negative Edge to ±1/2 LSB, All Bits Switched ON or OFF	300	ns
Data Input Setup Time	t_{DS}		30	ns
Data Input Hold Time	t_{DH}		30	ns
Address Input Setup Time (Bits 7 and 6)	t_{AS}	4-Bit Mode	100	ns
Address Hold Time	t_{AH}	4-Bit Mode	0	ns
Chip Enable Negative Hold Time	t_{ENH}		100	ns
Chip Enable Positive Hold Time	t_{EPH}		200	ns

FUNCTIONAL DIAGRAM AND TIMING DIAGRAM FOR 4-BIT OPERATION



DAC-808 FUNCTION TABLE

NO.	MODE	FUNCTION	DESCRIPTION	$\overline{CE}$	MC	PIN 1 DB7	PIN 2 DB6
1	8-Bit	8-bit byte transfer (1 cycle)	1. Data transfer to master	↓	0	X	X
			2. Data to slave match	↑	0	X	X
2	4-Bit (2 nibbles)	Two 4-bit transfers using 2 cycles. DB0-DB3 LSB first.	1. 4 bits to LSB's master	↓	1	0	0
			2. No change in latch	↑	1	0	0
			3. 4 bits to MSB's master	↓	1	0	1
			4. 8 bits in master to slave and output	↑	1	0	1
3	4-Bit (2 nibbles)	Two 4-bit transfers using 2 cycles. DB0-DB3 MSB first.	1. 4 bits to MSB's master	↓	1	1	1
			2. No change	↑	1	1	1
			3. 4 bits to LSB's master	↓	1	1	0
			4. 8 bits in master to slave and output	↑	1	1	0
4	4-Bit	4-bit transfer using 1 cycle.	1. 4 bits to LSB's master	↓	1	1	0
			2. 4 bits in master to LSB slave and output	↑	1	1 OR	0
		Input DB0-DB3.			0	X	X
		Ground DB4-DB7.			0	X	X
5	4-Bit	4-bit transfer using 1 cycle.	1. 4 bits to MSB's master	↓	1	0	1
			2. 4 bits in master to MSB slave and output	↑	1	0 OR	1
		Input DB4-DB7.			0	X	X
		Ground DB0-DB3.			0	X	X
6	None	No operation	Chip disabled — Previous output still present	1	X	X	X

LSB — Least Significant Bit
MSB — Most Significant Bit
X — Insignificant (Don't Care)

↑ — Positive Transition
↓ — Negative Transition
DB — Data Bit

DIGITAL INFORMATION

The DAC-808 is a monolithic microprocessor compatible device consisting of a quad digital switch, two 4-bit master latches, one 8-bit slave latch, control circuitry, and one 8-bit multiplying DAC; all housed in an 18-pin Dual In-line Package.

The DAC-808 can be thought of, in the 4-bit mode, as a quad 1 to 2-line digital demultiplexer which selects a 4-bit input and transfers this data to one of two 4-bit master latches.

The BYTEDAC™ accepts a straight binary digital byte at the master latch which is a fast edge-triggered device. Two 4-bit independent latches make up the master latch and are clocked separately depending on the state of the Mode Control (MC). The second latch, or slave latch, is 8 bits and connects directly with the DAC. The Chip Enable (CE) is used to clock data to and from both latches. When CE is high, the DAC will output a current equal to the last digital value entered (refer to the Equivalent Circuit).

8-BIT TRANSFER MODE #1

To load 8-bit parallel data, a low must be present at MC which sets both master latches in a condition for simultaneous clocking. The negative transition on CE will now transfer data to the master latch while the positive transaction clocks data to the slave latch and input to the DAC (see the Timing Diagram). The CE line can be held low for an indefinite period to prevent data transfer.

INTERFACE TO 4-BIT BUS

The DAC-808 is able to handle 4-bit data in four ways, which will be discussed here. Modes 2 and 3 transfer two 4-bit nibbles which are assembled at the slave latch into an 8-bit byte (refer to Function Table). Modes 4 and 5 transfer a single 4-bit nibble only.

LOADING LSB NIBBLE FIRST, MODE #2

For all 4-bit operations the MC pin must be high. A low must be applied to Data Bit 6 (DB6) which now acts as an address pin. Data is brought in at DB0 through DB3 and clocked into the LSB master latch on the negative transition of CE. Nothing occurs on the positive transition of the CE's first cycle. DB6 must now go high to enable the second master latch which is loaded through the digital switch on the next negative transition at CE. Both the MSB and LSB nibbles are then loaded in the slave latch on the positive transition at CE. Data Bit 7 (DB7) must remain low in this mode.

LOADING MSB NIBBLE FIRST, MODE #3

This mode is identical to Mode 2 except DB7 remains high and DB6 is high during the first cycle and low during the second cycle. The MSB nibble is loaded into the master latch through the digital switch during the first CE cycle. The second CE cycle loads LSB nibble and transfers all 8 bits to slave latch and DAC.

LOADING 4 BITS (DB0 THROUGH DB3), MODE #4

By applying a low at MC and entering data at DB0 through DB3, 4 bits of data can be loaded. Again, the nibble is latched into the LSB master latch on negative CE and clocked to the lower slave inputs at CE positive. DB7 must be high and DB6 must be low. The MSB nibble will contain and hold the last data entered into it. If four LSBs of resolution are all that will be required, the data may be entered in the 8-bit mode with MC low and DB4 through DB7 tied high or low.

DAC-808 EQUIVALENT CIRCUIT

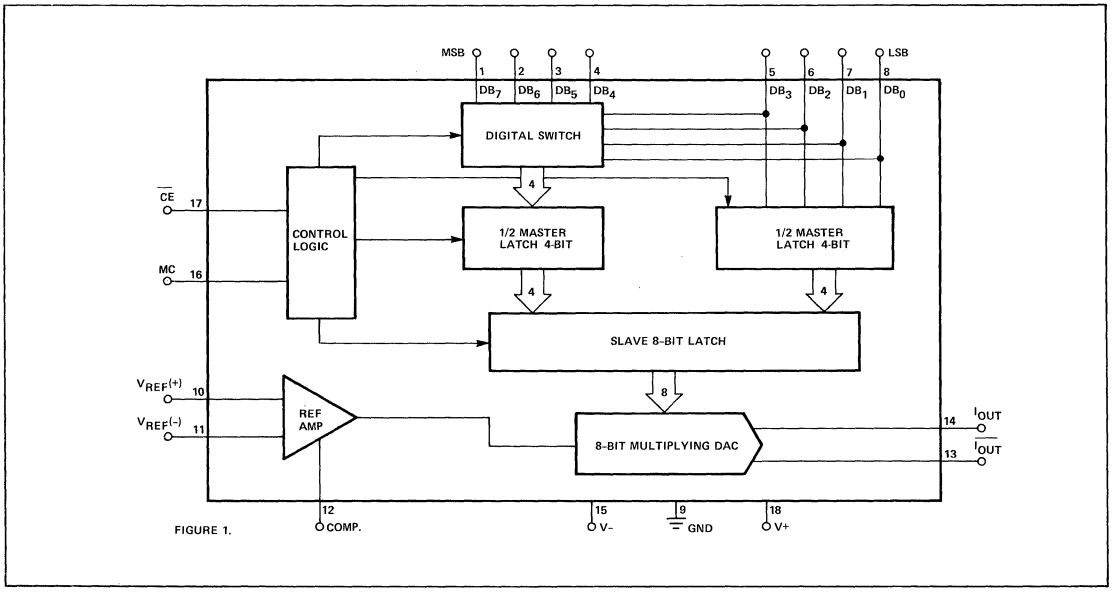


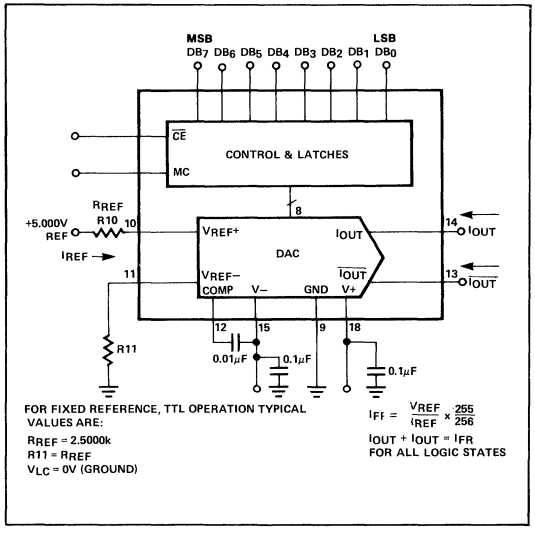
FIGURE 1.

LOADING 4 BITS (DB4 THROUGH DB7), MODE #5

This is the same as Mode 4 except that DB7 is now low and DB6 is now high. The data is still entered into DB0 through DB3, but the data is now loaded into the MSB nibble. The LSB nibble will contain and hold the last data entered into it. If 4 MSBs of resolution are all that will be required, the data may be entered in the 8-bit mode with MC low and DB0 through DB3 tied high or low.

ANALOG INFORMATION

BASIC POSITIVE REFERENCE OPERATION



REFERENCE AMPLIFIER SETUP

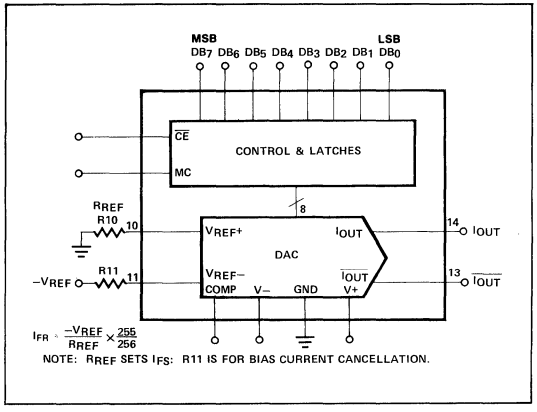
The DAC-808 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly 0 to +4.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{255}{256} \times I_{REF} \text{ where } I_{REF} = I_{10}$$

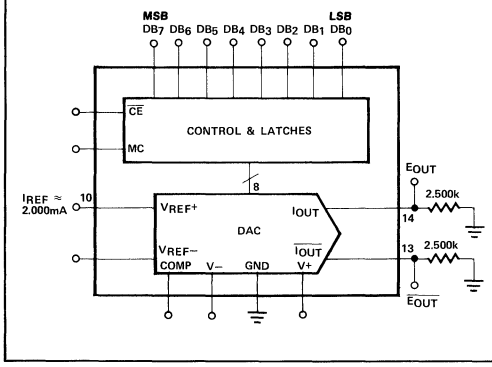
In positive reference applications, an external positive reference voltage current flows through R_{10} into the $V_{REF(+)}$ terminal of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$; reference current flows from ground through R_{10} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 11. The voltage at pin 10 is equal to and tracks the voltage at pin 11 due to the high gain of the internal reference amplifier. R_{11} (nominally equal to R_{10}) is used to cancel bias current errors; R_{11} may be eliminated with only a minor increase in error.

For most applications the tight relationship between I_{REF} and I_{FR} will eliminate the need for trimming I_{REF}. If required, full-scale trimming may be accomplished by adjusting the value of R_{10} or by using a potentiometer for R_{10}. An improved method of full-scale trimming which eliminates poten-

BASIC NEGATIVE REFERENCE OPERATION

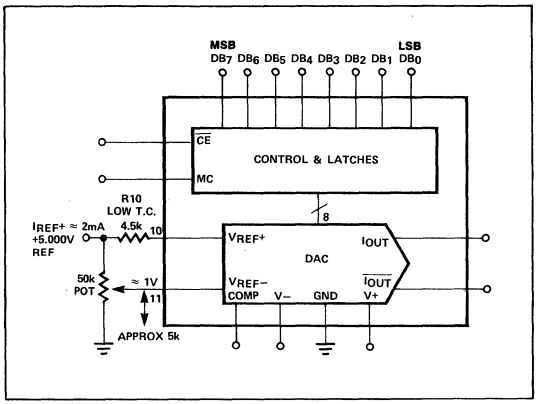


BASIC UNIPOLAR NEGATIVE OPERATION



	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	I_OmA	$\overline{I_O}$mA	E_O	$\overline{E_O}$
FULL SCALE – 1 LSB	1	1	1	1	1	1	1	1	1.992	0.000	– 4.980	0.000
FULL SCALE – 2 LSB	1	1	1	1	1	1	1	0	1.984	0.008	– 4.960	– 0.020
HALF SCALE + LSB	1	0	0	0	0	0	0	1	1.008	0.984	– 2.520	– 2.460
HALF SCALE	1	0	0	0	0	0	0	0	1.000	0.992	– 2.500	– 2.480
HALF SCALE – LSB	0	1	1	1	1	1	1	1	0.992	1.000	– 2.480	– 2.500
ZERO SCALE + LSB	0	0	0	0	0	0	0	1	0.008	1.984	– 0.020	– 4.960
ZERO SCALE	0	0	0	0	0	0	0	0	0.000	1.992	– 0.000	– 4.980

RECOMMENDED FULL SCALE ADJUSTMENT CIRCUIT



tiometer TC effects is shown in the Recommended Full Scale Adjustment Circuit.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common mode range. The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

The reference amplifier must be compensated by using a capacitor from pin 12 to V−. For fixed reference operation, a 0.01μF capacitor is recommended. For variable reference applications, see "Reference Amplifier Compensation for Multiplying Applications" section.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 12 to V−. The value of this capacitor depends on the impedance presented to pin 10 (see Table 1).

TABLE 1. REFERENCE AMPLIFIER COMPENSATION

REF. INPUT RESISTANCE	SUGGESTED C_C
1kΩ	15pF
2.5kΩ	37pF
5kΩ	75pF

NOTE: A 0.01μF capacitor is suggested for fixed references.

For fastest response to a pulse, low values of R_{10}, enabling small C_C values, should be used. If pin 10 is driven by a high current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For $R_{10} = 1k\Omega$ and $C_C = 15pF$, the reference amplifier slews at 4mA/μs, enabling a transition from $I_{REF} = 0$ to $I_{REF} = 2mA$ in 500ns (see Figure 6).

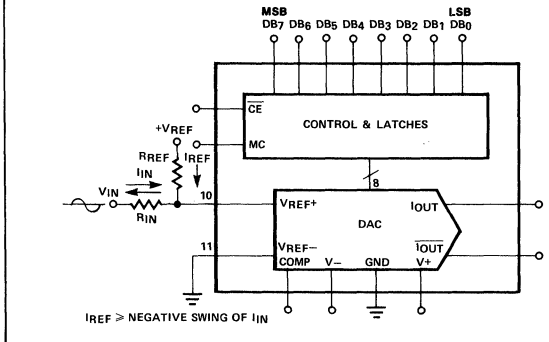
Bipolar references may be accommodated by offsetting V_{REF} or pin 11, as shown in Figure 5. The negative common mode range of the reference amplifier is given by $V_{CM} = V-$ plus ($I_{REF} \times 1k\Omega$) plus 2.5V. The positive common mode range is V+ less 1.5V.

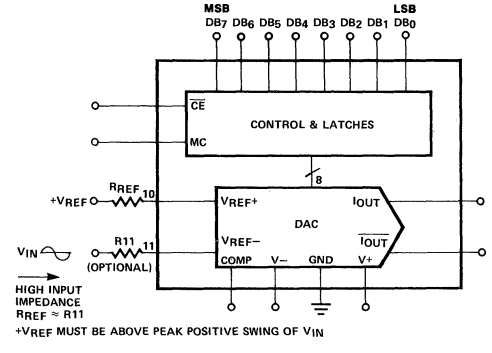
When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL Logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{10} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

ANALOG OUTPUT CURRENTS

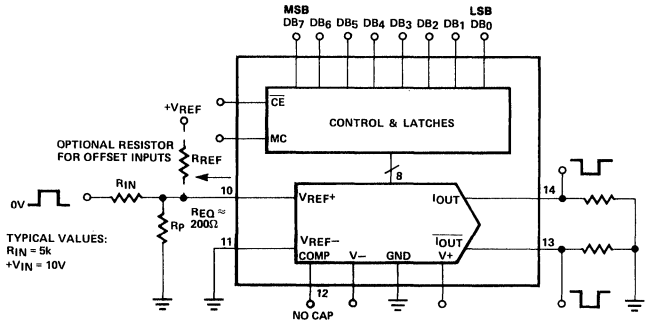
Both true and complemented output sink currents are provided, where $I_O + \overline{I_O} = I_{FR}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 14 increases proportionally in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 14 and turned on at pin 13. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}; do not leave an unused output pin open.

ACCOMMODATING BIPOLAR REFERENCES

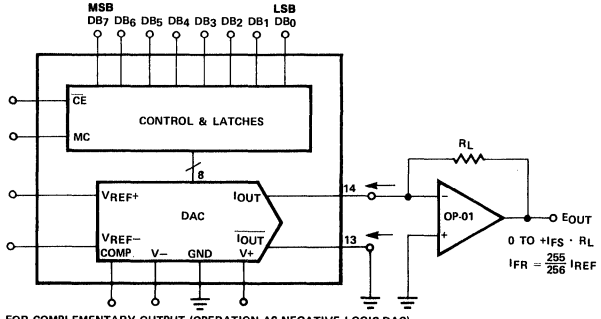




ALTERNATE PULSED REFERENCE OPERATION

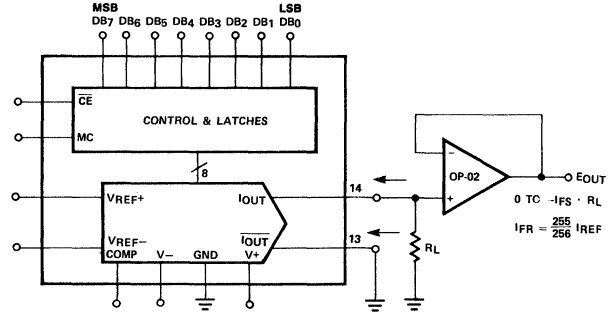


POSITIVE LOW IMPEDANCE OUTPUT OPERATION



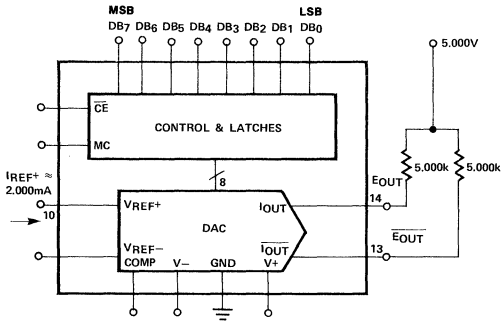
FOR COMPLEMENTARY OUTPUT (OPERATION AS NEGATIVE LOGIC DAC), CONNECT INVERTING INPUT OF OP-AMP TO $\overline{I_{OUT}}$. CONNECT I_{OUT} TO GROUND.

NEGATIVE LOW IMPEDANCE OUTPUT OPERATION



FOR COMPLEMENTARY OUTPUT (OPERATION AS NEGATIVE LOGIC DAC), CONNECT INVERTING INPUT OF OP-AMP TO $\overline{I_{OUT}}$. CONNECT I_{OUT} TO GROUND.

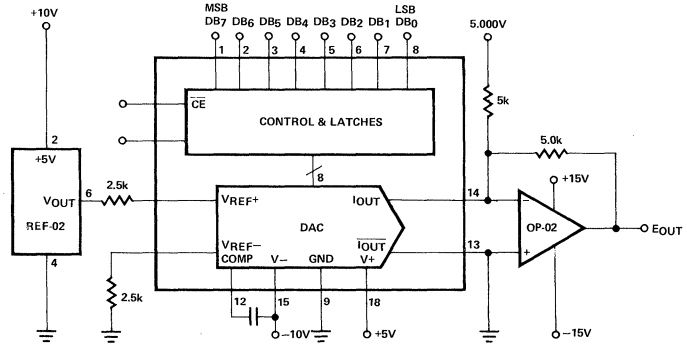
BASIC BIPOLAR OUTPUT OPERATION



	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	E_O	E_O
POSITIVE FULL SCALE	1	1	1	1	1	1	1	1	−4.960	5.000
POSITIVE FULL SCALE − LSB	1	1	1	1	1	1	1	0	−4.920	4.960
ZERO SCALE + LSB	1	0	0	0	0	0	0	1	−0.040	0.080
ZERO SCALE	1	0	0	0	0	0	0	0	0.000	0.040
ZERO SCALE − LSB	0	1	1	1	1	1	1	1	0.040	0.000
NEGATIVE FULL SCALE + LSB	0	0	0	0	0	0	0	1	4.900	−4.920
NEGATIVE FULL SCALE	0	0	0	0	0	0	0	0	5.000	−4.960

Both outputs have an extremely wide voltage compliance, enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 18V above V− and is independent of the positive supply. Negative compliance is given by V− plus ($I_{REF} \times 1k\Omega$) plus 2.5V.

OFFSET BINARY OPERATION



	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	E_O
POSITIVE FULL SCALE −1 LSB	1	1	1	1	1	1	1	1	4.960
POSITIVE FULL SCALE −2 LSB	1	1	1	1	1	1	1	0	4.920
ZERO SCALE	1	0	0	0	0	0	0	0	0.000
NEGATIVE ZERO SCALE +2 LSB	0	0	0	0	0	0	0	1	−4.960
NEGATIVE FULL SCALE +1 LSB	0	0	0	0	0	0	0	0	−5.00

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC-808 operates over a wide range of power supply voltages from a total supply of 9V to 15V. When operating at supplies of ±5V or less, $I_{REF} \leq 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at −4.5V with $I_{REF} = 2mA$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible. However, at least 8V must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-808 is quite insensitive to variations in supply voltage.

Power consumption may be calculated as follows:

$$P_d = (I+)(V+) + (I-)(V-) + (2\ I_{REF})(V-).$$

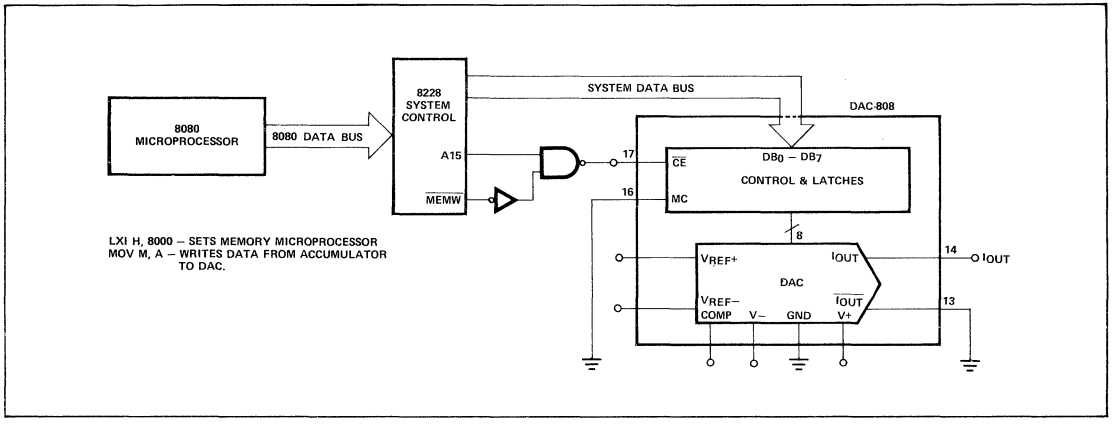
TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-808 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is tight, typically ±10ppm/°C, with zero scale output current and drift essentially negligible compared to 1/2 LSB.

Full-scale output drive performance will be best with +5.0V reference, as V_{OS} and TCV_{OS} of the reference amplifier will be very small compared to 10.0V. The temperature coefficient of the reference resistor R_{10} should match and track that of the output resistor for minimum overall full-scale drift. Settling times of the DAC-808 decrease approximately 10% at −55°C; at +125°C an increase of about 15% is typical.

APPLICATIONS

8080 MICROPROCESSOR INTERFACE — 8-BIT TRANSFER



DAC-888

8-BIT HIGH-SPEED "MICROPROCESSOR COMPATIBLE" MULTIPLYING D/A CONVERTER

FEATURES

- **8-Bit Level Triggered Latch**
- **8-Bit μP Compatible**
- **Easily Interfaced to All 8-Bit Processors**
- **TTL Logic Compatible**
- **$\overline{CE}$ and $\overline{WR}$ Inputs**
- **High Output Impedance and Compliance**
- **Proven DAC-08 Analog Flexibility**
- **Nonlinearity to $\pm$0.1% Maximum**
- **Low Power Dissipation 134mW**

GENERAL DESCRIPTION

The BYTEDAC™ DAC-888 is a buffered 8-bit digital-to-analog converter designed specifically for 8-bit bus oriented systems. The data inputs are connected to level-triggered latches. Two active-low control pins are provided for ease of interface to virtually all available microprocessors. The latches may also be operated in a transparent mode by holding both control pins low. Additionally, the DAC-888 has a data hold time requirement of zero nanoseconds.

The Analog section consists of a "Field-Proven" DAC-08 D/A Converter. Monotonic multiplying performance is attained over a wide 40 to 1 reference current range. Matching to within 1 LSB between reference and full-scale currents eliminates full-scale adjustment in most applications.

DAC-888 applications include graphic display drivers, high-speed modems, A/D converters, programmable waveform generators and power supplies, analog meter drivers, audio encoders and programmable attenuators; and other applications where low cost, high speed and buffered flexibility are required.

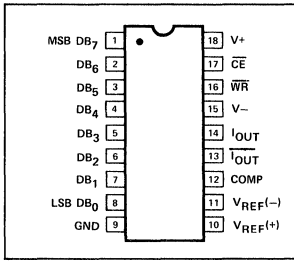
ORDERING INFORMATION†

	18-PIN HERMETIC DUAL INLINE	
INL %FS	**MILITARY TEMP.**	**COMMERCIAL TEMP.**
0.1	DAC888AX*	DAC888EX
0.19	DAC888BX*	DAC888FX

* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

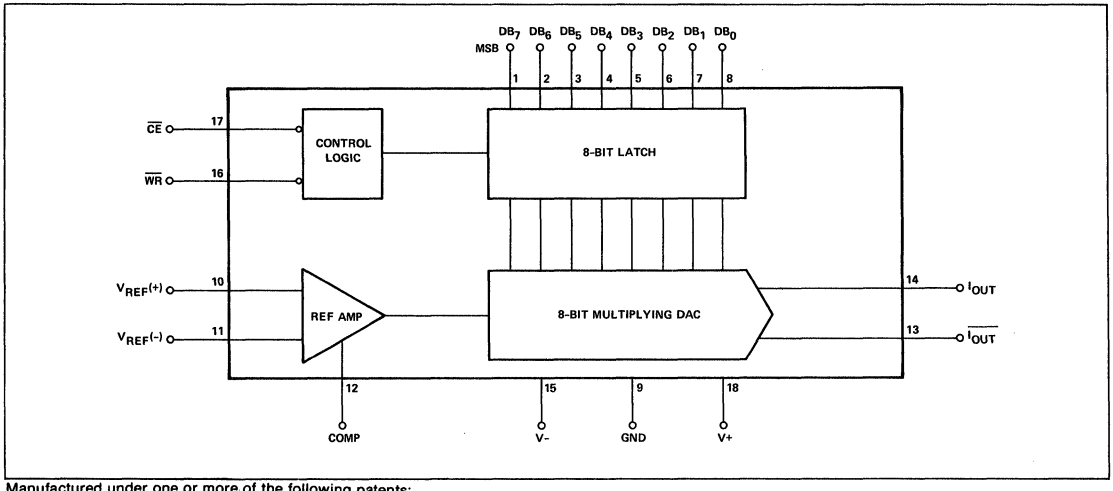
† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



18-PIN HERMETIC DUAL-IN-LINE (X Suffix)

FUNCTIONAL DIAGRAM



Manufactured under one or more of the following patents: 4,055,773; 4,056,740; 4,092,639

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
DAC-888 A/B ..... −55°C to +125°C
DAC-888 E/F ..... −25°C to +85°C
DICE Junction Temperature (T_j) ..... −65°C to +150°C
Storage Temperature ..... −65°C to +150°C
Power Dissipation 300mW
Derate above 100°C ..... 10mW/°C
Lead Soldering Temperature ..... 300°C (60 sec)

V+ Supply to V− Supply 18.1V
Logic Inputs ..... 0V to 5.5V
Analog Current Outputs ..... −5mA
Reference Inputs (V_{14} to V_{15}) ..... V− to V+
Reference Input Differential Voltage
(V_{14} to V_{15}) ..... ±15V
Reference Input Current 5.0mA

NOTE: Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V+ = +5V, V− = −12V, I_{REF} = 2.0mA, T_A = −55°C to +125°C for DAC-888A/B, unless otherwise noted. T_A = −25°C to +85°C apply for DAC-888E/F; Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-888A/E MIN	DAC-888A/E TYP	DAC-888A/E MAX	DAC-888B/F MIN	DAC-888B/F TYP	DAC-888B/F MAX	UNITS
Resolution			8	8	8	8	8	8	Bits
Monotonicity			8	8	8	8	8	8	Bits
Nonlinearity			–	–	±0.1	–	–	±0.19	%FS
Full Scale Tempco	TCI_{FS}	(See note)	–	±10	±50	–	±10	±80	ppm/°C
Output Voltage Compliance	V_{OC}	Full Scale Current Change < 1/2 LSB	−5	–	+8	−5	–	+8	V
Output Impedance	R_{OUT}		–	>20	–	–	>20	–	MΩ
Full Range Current	I_{FR}	V_{REF} = 5.00V, R_{11}, R_{10} = 2.500kΩ, T_A = 25°C	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Range Symmetry	I_{FRS}	$I_{FR14} - I_{FR13}$	–	±1.0	±8.0	–	±1.0	±8.0	μA
Zero Scale Current	I_{ZS}		–	0.2	2.0	–	0.2	2.0	μA
Output Current Range	I_{FSR}		0	2.0	2.1	0	2.0	2.1	mA
Reference Bias Current	I_B		–	−1.0	−3.0	–	−1.0	−3.0	μA
Power Supply Sensitivity	$PSSI_{FR+}$ $PSSI_{FR-}$	V+ = 4.5V to 5.5V V− = −4.5V to −12V I_{REF} = 1mA		−±0.0003 −±0.0002	±0.01 0.01		−±0.0003 −±0.0002	±0.01 0.01	$\%\Delta I_{FS}/\%\Delta V+$ $\%\Delta I_{FS}/\%\Delta V-$
Power Supply Current	$I+$ $I-$	V_S = +5V, −12V I_{REF} = 2.0mA	–	12 6	16 9	–	12 6	16 9	mA
Power Dissipation	P_d	+5V, −12V I_{REF} = 2.0mA	–	134	190	–	134	190	mW
Logic Input Levels									
Logic Input "0"	V_{IL}		–	–	0.8	–	–	0.8	V
Logic Input "1"	V_{IH}		2.0	–	–	2.0	–	–	
Logic Input Current									
Logic Input "0"	I_{IL}		–	–	−5	–	–	−5	μA
Logic Input "1"	I_{IH}		–	–	+0.1	–	–	+0.1	

NOTE: Guaranteed by design

ELECTRICAL CHARACTERISTICS— A.C. PARAMETERS V_S = + 5V, - 12V, I_{REF} = 2.0mA, T_A = 25° C

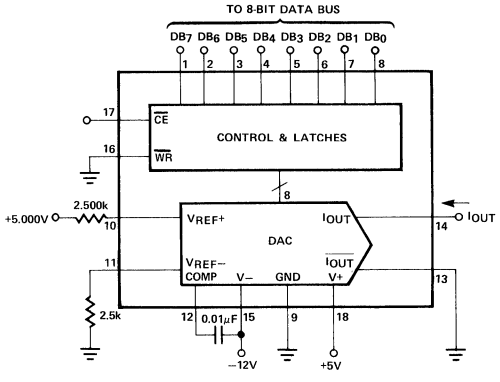
PARAMETER	SYMBOL	CONDITIONS	DAC-888A/E MIN	DAC-888A/E TYP	DAC-888A/E MAX	DAC-888B/F MIN	DAC-888B/F TYP	DAC-888B/F MAX	UNITS
Settling Time	t_S	From $\overline{CE}$ & $\overline{WR}$ Negative Level to ±1/2LSB, All Bits Switched ON or OFF, (See note)		100	250	–	100	250	ns
Reference Input Slew Rate	dI/dt	(See Note)	4.0	8.0	–	4.0	8.0	–	mA/μs
Data Input Setup Time	t_{DS}	(See note)	150	–	–	150	–	–	ns
Data Input Hold Time	t_{DH}	(See note)	10	–	–	10	–	–	ns
Chip Enable/Write Pulse Width	t_{ENW}	(See note)	250	–	–	250	–	–	ns

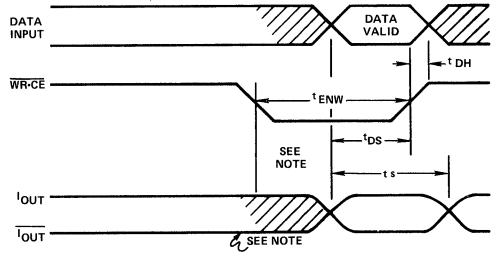
NOTE: Guaranteed by design

DAC-888 PIN DESCRIPTION

SYMBOL	DESCRIPTION	
DB_0-DB_7	DATA BIT — Bits 0-7 are digital, active-high inputs. DB_7 is assigned as the MSB.	PINS 1-8
$\overline{CE}$	CHIP ENABLE — An active-low input control which is the device enable input terminal.	PIN 17
$\overline{WR}$	WRITE CONTROL — An active low control which enables the microprocessor to write data to the DAC.	PIN 16
I_{OUT} • $I_{\overline{OUT}}$	CURRENT OUTPUT — Complementary current outputs when added equal I_{FS}.	PINS 13-14
V_{REF+}, V_{REF-}	VOLTAGE REFERENCE — Differential inputs that accept a negative, positive, or bipolar input and are used to adjust I_{FS}.	PINS 10-11
COMP	COMPENSATION — The reference amplifier frequency compensating terminal.	PIN 12

FUNCTIONAL DIAGRAM AND TIMING DIAGRAM FOR 8-BIT OPERATION



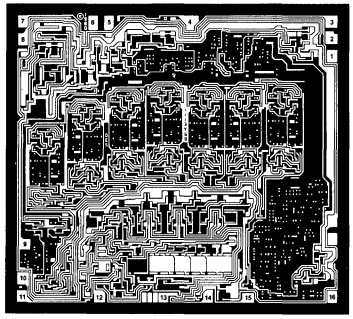


NOTE: If input data changes after $\overline{WR}$ • $\overline{CE}$ low, I_{OUT}/$I_{\overline{OUT}}$ will change. The last data input before $\overline{WR}$ + $\overline{CE}$ high will be latched. It is suggested, but not mandatory, that data be valid from $\overline{WR}$ • $\overline{CE}$ low to $\overline{WR}$ + $\overline{CE}$ high.

OPERATION TABLE

$\overline{CE}$	$\overline{WR}$	OUTPUT
I	X	NO CHANGE
O	I	NO CHANGE
O	O	UPDATE LATCHES (TRANSPARENT)

DICE CHARACTERISTICS



1. DB7 (MSB)
2. DB6
3. DB5
4. DB4
5. DB3
6. DB2
7. DB1
8. DB0 (LSB)
9. GROUND
10. V_{REF} (+)
11. V_{REF} (−)
12. COMP
13. I_{OUT}
14. I_{OUT}
15. V −
16. $\overline{WR}$
17. $\overline{CE}$
18. V +

DIE SIZE 0.138 × 0.125 inch

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at 25°C; V_S = +5V, -12V and I_{REF} = 2.0 mA, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-888N LIMIT	DAC-888G LIMIT	UNITS
Resolution			8	8	Bits MIN
Monotonicity			8	8	Bits MIN
Nonlinearity			±0.1	±0.19	%FS MAX
Output Voltage Compliance	V_{OC}	Full Scale Current Change < 1/2 LSB R_{OUT} > 20 MΩ Typ.	+8 −5	+8 −5	V MAX V MIN
Full Range Current	I_{FR14}	V_{REF} = 5.00V R_{11}, R_{10} = 2.500kΩ T_A = 25°C	2.04 1.94	2.04 1.94	mA MAX mA MIN
Full Range Symmetry	I_{FRS}	I_{FR14}-I_{FR13}	±8.0	±8.0	μA MAX
Zero Scale Current	I_{ZS}		2.0	2.0	μA MAX
Output Current Range	I_{FSR}	V− = −12V	2.1 0	2.1 0	mA MAX mA MIN
Reference Bias Current	I_B		−3.0	−3.0	μA MAX
Power Supply Sensitivity	$PSSI_{FR+}$ $PSSI_{FR-}$	V+ = 4.5V to 5.5V V− = −4.5V to −12V I_{REF} = 1mA	±0.01 ±0.01	±0.01 ±0.01	$\%\Delta I_{FS}/\%\Delta V+$ MAX $\%\Delta I_{FS}/\%\Delta V-$ MAX
Power Supply Current	I+ I−	V_S = +5V, −12V I_{REF} = 2.0mA	16 9	16 9	mA MAX mA MAX
Power Dissipation	P_d	+5V, −12V, I_{REF} = 2.0mA	170	170	mW MAX
Logic Input Levels Logic Input "0" Logic Input "1"	 V_{IL} V_{IH}		 0.8 2.0	 0.8 2.0	 V MAX V MIN

TYPICAL ELECTRICAL CHARACTERISTICS V_S = + 5V, - 12V, I_{REF} = 2.0mA, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-888 TYPICAL	UNITS
Reference Input Slew Rate	dI/dt		8.0	mA/μs
Settling Time	t_S	From CE Negative Edge to ±1/2 LSB, All bits Switched ON or OFF	100	ns
Data Input Setup Time	t_{DS}		100	ns
Data Input Hold Time	t_{DH}		0	ns
Chip Enable/ Write Pulse Width	t_{ENW}		200	ns

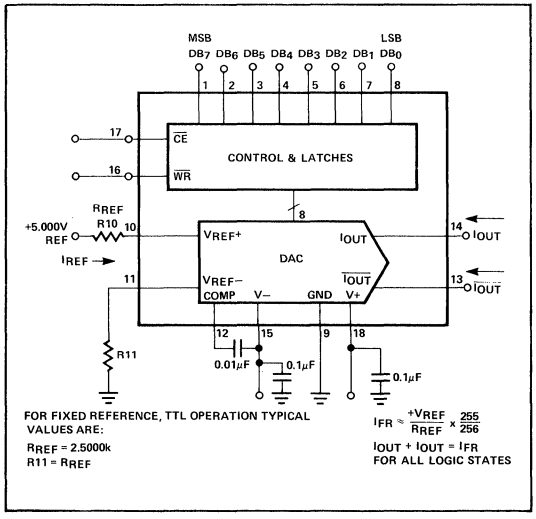
DIGITAL INFORMATION

The DAC-888 (BYTEDAC™) is a monolithic microprocessor compatible D/A converter consisting of an 8-bit level triggered latch, control circuitry and one 8-bit multiplying D/A converter housed in an 18 pin dual in line package (DIP).

The DAC-888 accepts 8-bit binary bytes at the data inputs. Data access is accomplished when $\overline{WR}$ and $\overline{CE}$ are low. During the low state of $\overline{CE}$ and $\overline{WR}$, the latches are transparent, therefore, data should be valid from 100ns prior to $\overline{WR}$ and $\overline{CE}$ low until $\overline{CE}$ or $\overline{WR}$ high. When $\overline{CE}$ or $\overline{WR}$ goes high, the data stored in the latches will hold the selected output indefinitely.

ANALOG INFORMATION

BASIC POSITIVE REFERENCE OPERATION



REFERENCE AMPLIFIER SETUP

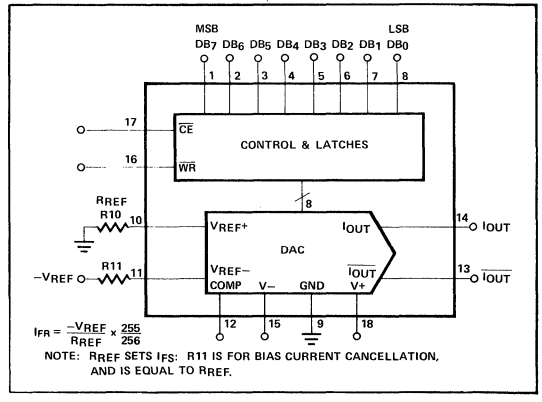
The DAC-888 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly 0 to +4.0mA. The full range output currrent is a linear function of the reference current and is given by:

$$I_{FR} = \frac{255}{256} \times I_{REF} \text{ where } I_{REF} = I_{10}$$

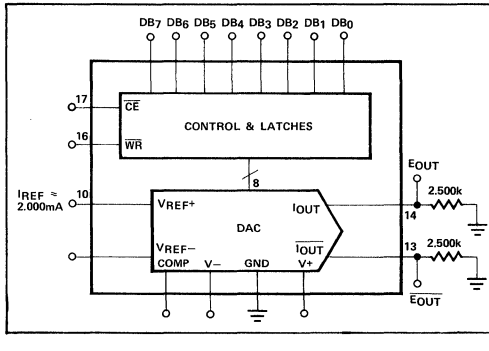
In positive reference applications, an external positive reference voltage current flows through R_{10} into the $V_{REF(+)}$ terminal of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$; reference current flows from ground through R_{10} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 11. The voltage at pin 10 is equal to and tracks the voltage at pin 11 due to the high gain of the internal reference amplifier. R_{11} (nominally equal to R_{10}) is used to cancel bias current errors; R_{11} may be eliminated with only a minor increase in error.

For most applications the tight relationship between I_{REF} and I_{FR} will eliminate the need for trimming I_{REF}. If required, full-scale trimming may be accomplished by adjusting the value of R_{10} or by using a potentiometer for R_{10}. An improved method of full-scale trimming which eliminates potentio-

BASIC NEGATIVE REFERENCE OPERATION

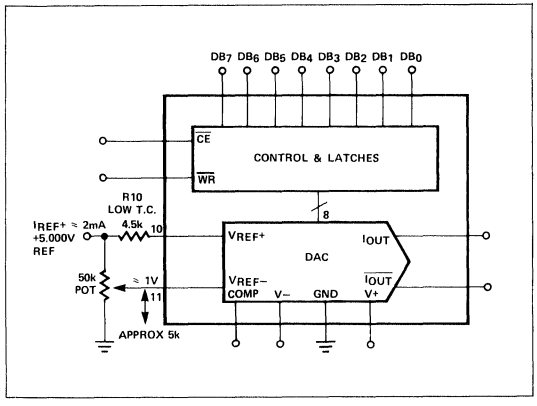


BASIC UNIPOLAR NEGATIVE OPERATION



	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	I_{OmA}	$I_{\overline{OmA}}$	E_O	$E_{\overline{O}}$
FULL SCALE – 1 LSB	1	1	1	1	1	1	1	1	1.992	0.000	– 4.980	0.000
FULL SCALE – 2 LSB	1	1	1	1	1	1	1	0	1.984	0.008	– 4.960	– 0.020
HALF SCALE + LSB	1	0	0	0	0	0	0	1	1.008	0.984	– 2.520	– 2.460
HALF SCALE	1	0	0	0	0	0	0	0	1.000	0.992	– 2.500	– 2.480
HALF SCALE – LSB	0	1	1	1	1	1	1	1	0.992	1.000	– 2.480	– 2.500
ZERO SCALE + LSB	0	0	0	0	0	0	0	1	0.008	1.984	– 0.020	– 4.960
ZERO SCALE	0	0	0	0	0	0	0	0	0.000	1.992	– 0.000	– 4.980

RECOMMENDED FULL SCALE ADJUSTMENT CIRCUIT



meter TC effects is shown in the Recommended Full Scale Adjustment Circuit.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common mode range. The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

The reference amplifier must be compensated by using a capacitor from pin 12 to V–. For fixed reference operation a 0.01μF capacitor is recommended. For variable reference applications, see "Reference Amplifier Compensation for Multiplying Applications" section.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 12 to V–. The value of this capacitor depends on the impedance presented to pin 10 (see Table 1).

TABLE 1. REFERENCE AMPLIFIER COMPENSATION

REF. INPUT RESISTANCE	SUGGESTED C_C
1kΩ	15pF
2.5kΩ	37pF
5kΩ	75pF

NOTE: A 0.01μF capacitor is suggested for fixed references.

For fastest response to a pulse, low values of R_{10}, enabling small C_C values, should be used. If pin 10 is driven by a high current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{10} = 1kΩ and C_C = 15pF, the reference amplifier slews at 4mA/μs, enabling a transition from I_{REF} = 0 to I_{REF} = 2mA in 500ns (see Figure, pulsed reference operation).

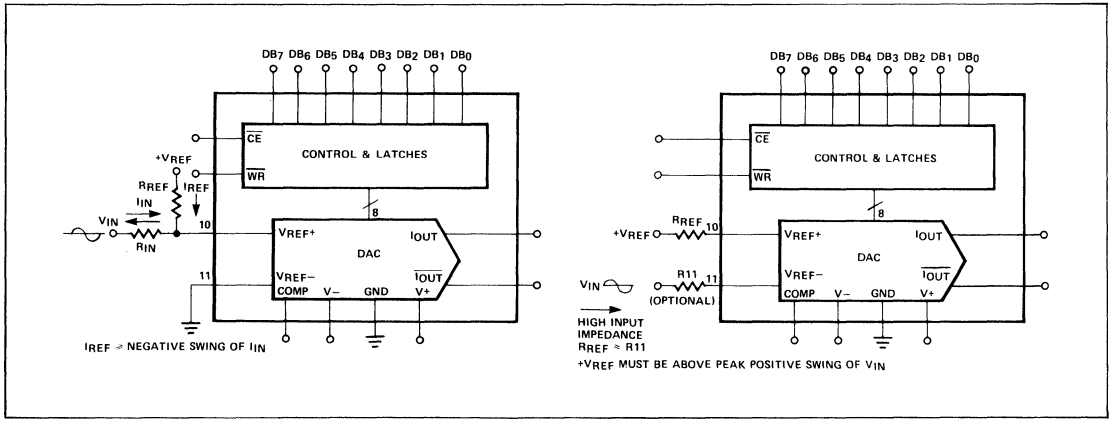
Bipolar references may be accommodated by offsetting V_{REF} or pin 11, as shown in Figure below. The negative common mode range of the reference amplifier is given by V_{CM} = V– plus (I_{REF} X 1kΩ) plus 2.5V. The positive common mode range is V+ less 1.5V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL Logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{10} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

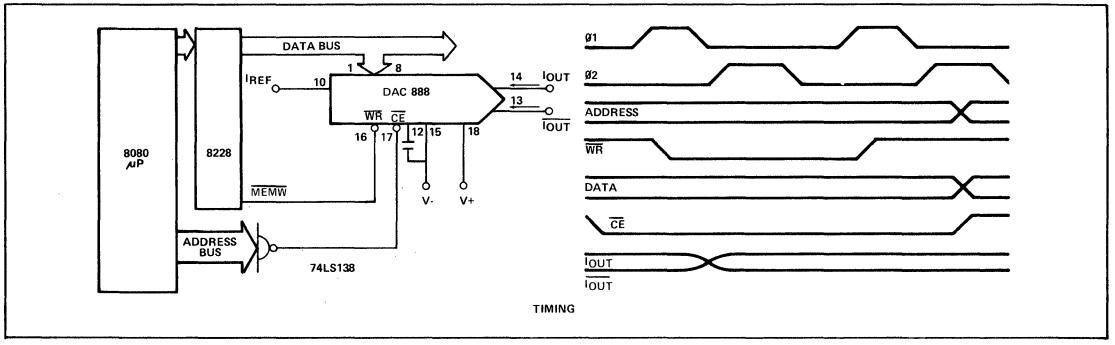
ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided, where $I_O + \overline{I_O} = I_{FR}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 14 increases proportionally in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 14 and turned on at pin 13. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}; do not leave an unused output pin open.

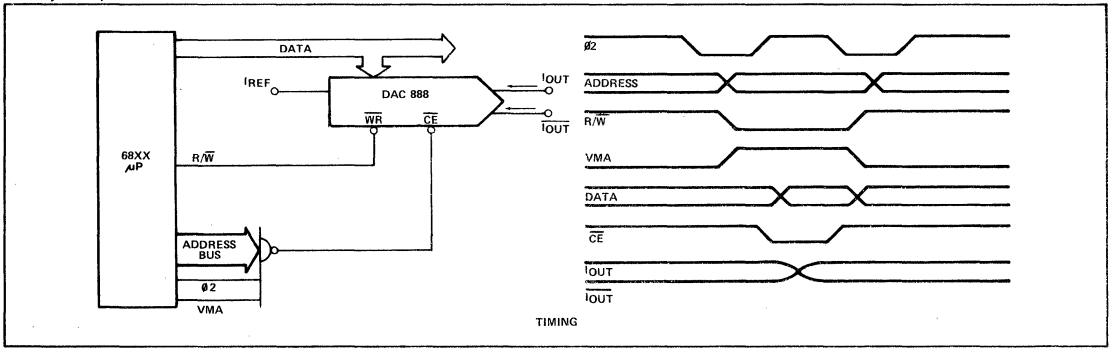
ACCOMMODATING BIPOLAR REFERENCES



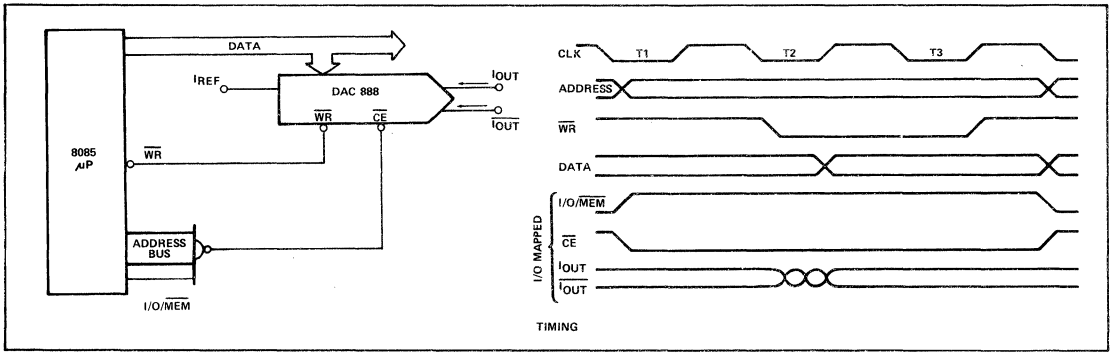
8080 INTERFACE



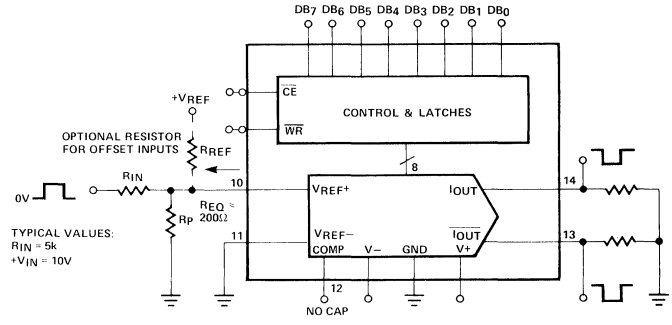
6800,6801,6809 INTERFACE



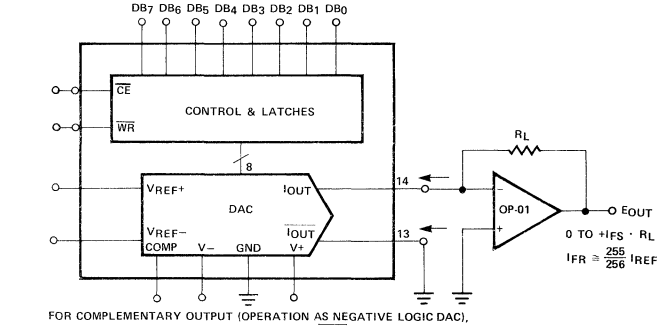
8085 INTERFACE



PULSED REFERENCE OPERATION

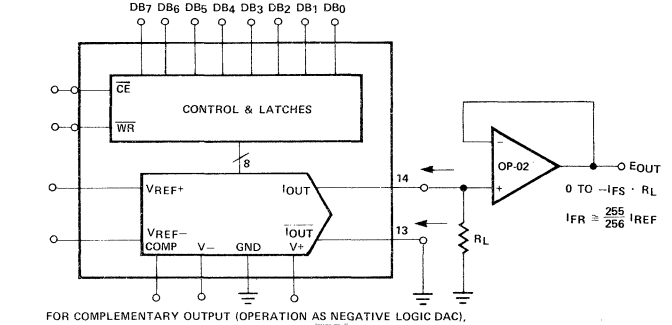


POSITIVE LOW IMPEDANCE OUTPUT OPERATION



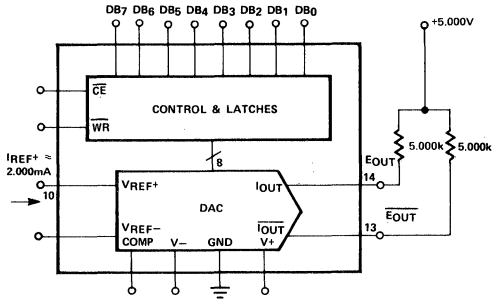
FOR COMPLEMENTARY OUTPUT (OPERATION AS NEGATIVE LOGIC DAC), CONNECT INVERTING INPUT OF OP-AMP TO $I_{\overline{OUT}}$. CONNECT I_{OUT} TO GROUND.

NEGATIVE LOW IMPEDANCE OUTPUT OPERATION



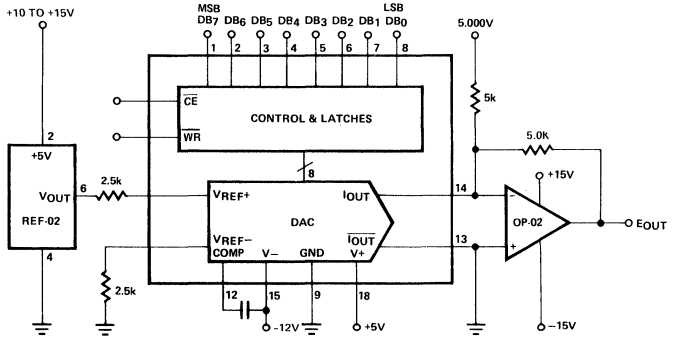
FOR COMPLEMENTARY OUTPUT (OPERATION AS NEGATIVE LOGIC DAC), CONNECT INVERTING INPUT OF OP-AMP TO $I_{\overline{OUT}}$. CONNECT I_{OUT} TO GROUND.

BASIC BIPOLAR OUTPUT OPERATION



	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	E_O	E_O
POSITIVE FULL SCALE	1	1	1	1	1	1	1	1	−4.960	5.000
POSITIVE FULL SCALE − 1 LSB	1	1	1	1	1	1	1	0	−4.920	4.960
ZERO SCALE + LSB	1	0	0	0	0	0	0	1	−0.040	0.080
ZERO SCALE	1	0	0	0	0	0	0	0	0.000	0.040
ZERO SCALE − LSB	0	1	1	1	1	1	1	1	0.040	0.000
NEGATIVE FULL SCALE + 1 LSB	0	0	0	0	0	0	0	1	4.900	−4.920
NEGATIVE FULL SCALE	0	0	0	0	0	0	0	0	5.000	−4.960

OFFSET BINARY OPERATION



	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	E_O
POSITIVE FULL SCALE − 1 LSB	1	1	1	1	1	1	1	1	4.960
POSITIVE FULL SCALE − 2 LSB	1	1	1	1	1	1	1	0	4.920
ZERO SCALE	1	0	0	0	0	0	0	0	0.000
NEGATIVE ZERO SCALE + 1 LSB	0	0	0	0	0	0	0	1	− 4.960
NEGATIVE FULL SCALE	0	0	0	0	0	0	0	0	− 5.000

BASIC BIPOLAR OUTPUT OPERATION

Both outputs have an extremely wide voltage compliance, enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 18V above V– and is independent of the positive supply. Negative compliance is given by V– plus (I_{REF} X 1kΩ) plus 2.5V.

POWER SUPPLIES

The DAC-888 operates over a wide range of power supply voltages from a total supply of 9V to 17V. When operating at supplies of ±5V or less, $I_{REF} \leq 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at –4.5V with I_{REF} = 2mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible. However, at least 8V must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-888 is quite insensitive to variations in supply voltage.

Power consumption may be calculated as follows:

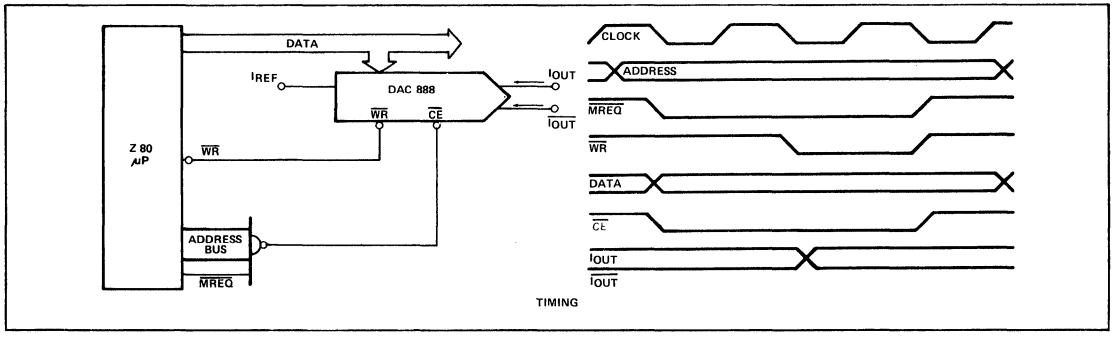
$P_d = (1 +) (V +) + (I -) (V -) + (2\ I_{REF}) (V -)$.

TEMPERATURE PERFORMANCE

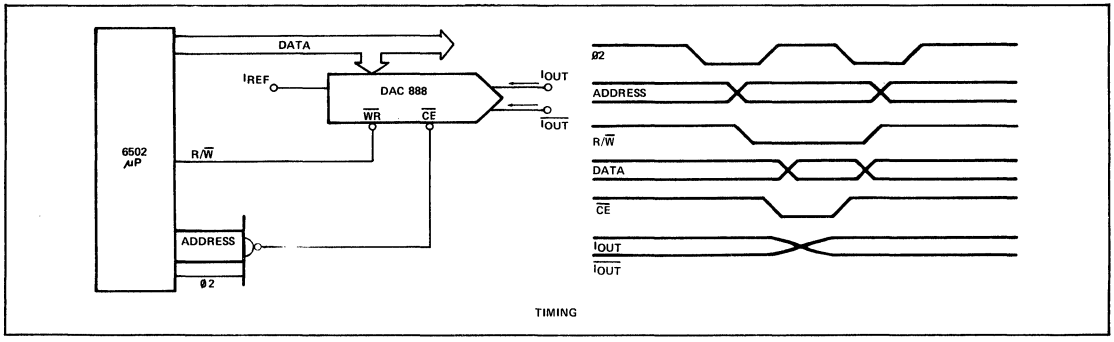
The nonlinearity and monotonicity specifications of the DAC-888 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is tight, typically ±10ppm/° C, with zero scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R_{10} should match and track that of the output resistor for minimum overall full-scale drift. Settling times of the DAC-888 decrease approximately 10% at –55° C; at +125° C an increase of about 15% is typical.

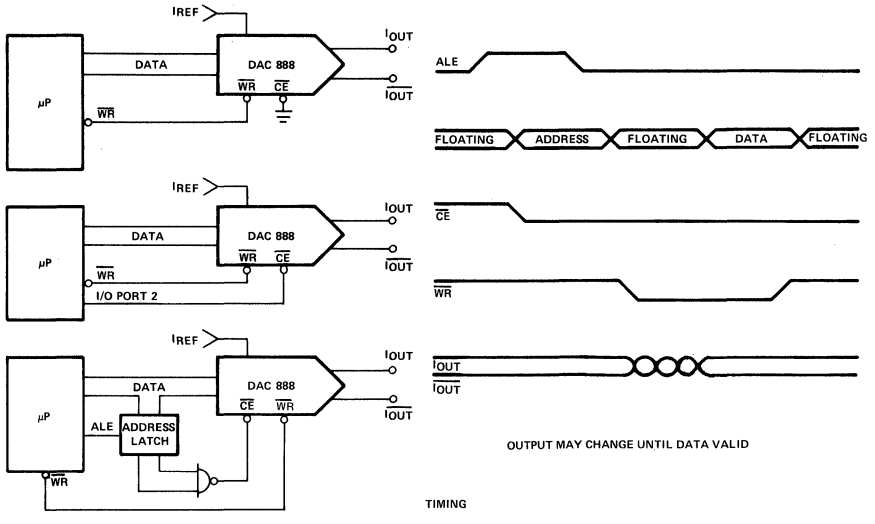
Z-80 INTERFACE



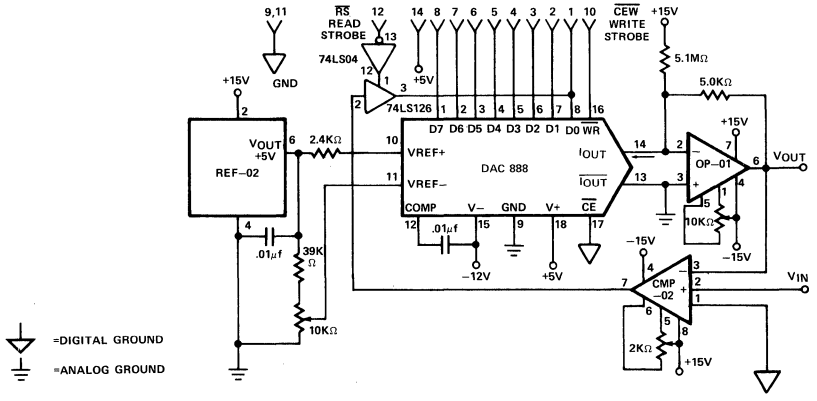
6502 INTERFACE



8048 INTERFACE



'SOFTWARE SAR'A/D CONVERTER (WITH 6502 MICRO PROCESSOR)

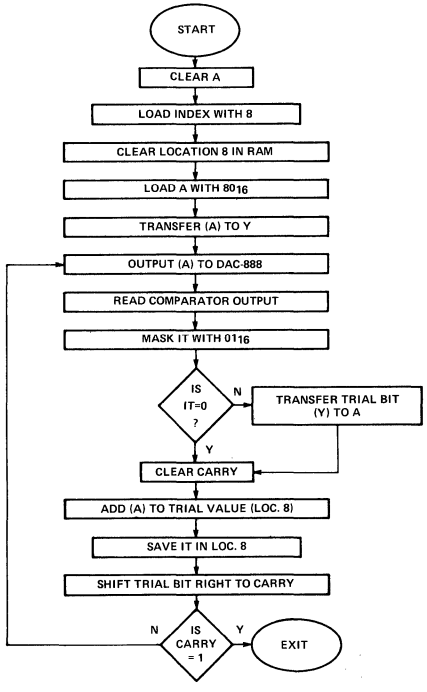


SUCCESSIVE APPROXIMATION ANALOG-TO-DIGITAL CONVERSION PROGRAM LISTING USING DAC-888 AND SYM1 PCB WITH 6502μP

LOCATION	DATA	MNEMONIC	COMMENTS
500	A9 00	LDA #00	CLEAR
502	A2 08	LDX #08	SET INDEX REGISTER
504	95 00	STA ,X	CLEAR MEMORY AT 08_H
506	A9 80	LDA #80	TRIAL BIT
508	A8	TAY	TO Y
509	*D 00 10	STA 1000 (CONT.)	OUTPUT
50C	AD 00 1C	LDA 1C00	READ COMP.
50F	29 01	AND A, #01	MASK IT
511	F0 01	BEQ * +1	BRANCH IF CMP = 0
513	98	TYA	GET TRIAL BIT
514	18	CLC	CLEAR CARRY
515	75 00	ADC ,X	RESULT SUMMED WITH PREVIOUS TEST
517	95 00	STA ,X	SAVE IT
519	98	TYA	GET TRIAL VALUE
51A	4A	LSR	NEXT BIT
51B	A8	TAY	SAVE IT
51C	15 00	ORA ,X	NEXT DATA
51E	90 E9	BCC * −23	CONTINUE FOR 8 TRIALS
520	4C 00 05	JMP 500	DO OVER

NOTE:
32 BYTES
260μs

FLOW CHART 'SOFTWARE SAR' A/D CONVERTER



DAC-1508A/1408A

8-BIT MULTIPLYING D/A CONVERTER

FEATURES

- **Improved Direct Replacement for MC1508/MC1408**
- **0.19% Nonlinearity Maximum Over Temperature Range**
- **Improved Settling Time ..... 250ns, Typical**
- **Improved Power Consumption ..... 157mW, Typical**
- **Compatible with TTL, CMOS Logic**
- **Standard Supply Voltages ..... +5.0V and −5.0V to −15V**
- **Output Voltage Swing .....+0.5V to −5.0V**
- **High-Speed Multiplying Input 4.0mA/μs**

GENERAL DESCRIPTION

The DAC-1508A/1408A are 8-bit monolithic multiplying digital-to-analog converters consisting of a reference current-2R ladder, and eight high-speed current switches. For many applications, only a reference resistor and reference voltage need be added. Improvements in design and processing techniques provide faster settling times combined with lower power consumption while retaining direct interchangeability with MC1508/1408 devices.

The R-2R ladder divides the reference current into eight binarily-related components which are fed to the switches. A remainder current equal to the least significant bit is always shunted to ground, therefore the maximum output current is 255/256 of the reference amplifier input current. For example, a full-scale output current of 1.992mA would result from a reference input current of 2.0mA.

The DAC-1508A/1408A is useful in a wide variety of applications, including waveform synthesizers, digitally programmable gain and attenuation blocks, CRT character generation, audio digitizing and decoding, stepping motor drives, programmable power supplies and in building tracking and successive approximation analog-to-digital converters.

For significantly improved speed and applications flexibility the user's attention is directed to the DAC-08 8-bit high-speed multiplying D/A converter data sheet. For D/A converters which include precision voltage references on the chip please refer to the DAC-02, DAC-04 and DAC-100 data sheets.

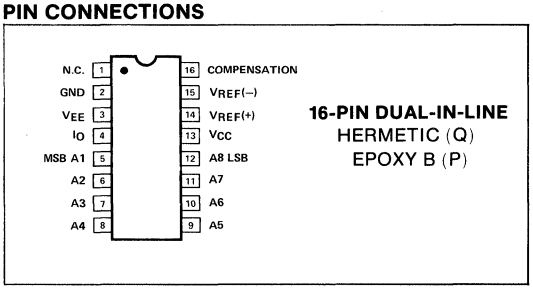
ORDERING INFORMATION†

	16-PIN DUAL-IN-LINE PACKAGE		
RELATIVE ACCURACY % FS	HERMETIC MILITARY	COMMERCIAL	PLASTIC COMMERCIAL
±0.19%	DAC1508A-8Q*	DAC1408A-8Q	DAC1408A-8P
±0.39%	——	DAC1408A-7Q	DAC1408A-7P
±0.78%	——	DAC1408A-6Q	DAC1408A-6P

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number.

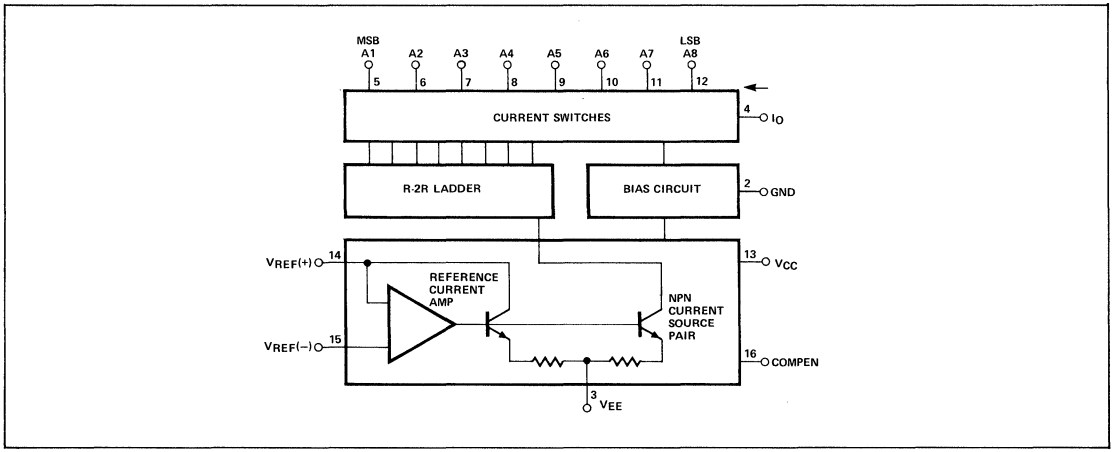
†All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



16-PIN DUAL-IN-LINE
HERMETIC (Q)
EPOXY B (P)

SIMPLIFIED SCHEMATIC



Manufactured under one or more of the following patents: 4,055,773; 4,056,740; 4,092,639.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage
- V_{CC} ..... +5.5Vdc
- V_{EE} ..... −16.5Vdc

Digital Input Voltage, V_5 through V_{12} ..... +5.5,0Vdc
Applied Input Voltage ..... +0.5, −5.2Vdc
Reference Current, I_{14} 5.0mA
Power Dissipation (Package Limitation), P_d
- Ceramic Package (or Expoxy B Package) 100mW
- Derate above $T_A = +25°C$ ..... 6.7mW/°C
- Derate above $T_A = +100°C$ for Epoxy B Package ..... 5.3mW/°C

Operating Temperature Range, T_A
- DAC-1508A ..... −55°C to +125°C
- DAC-1408A ..... 0°C to +75°C

DICE Junction Temperature (T_j) ..... −65°C to 150°C
Storage Temperature Range, T_{stg} ..... −65°C to +150°C
- Plastic Package Only ..... −65°C to +125°C

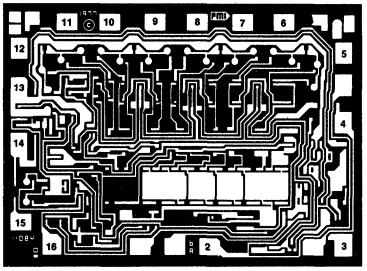
NOTE: Ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_{CC} = +5.0$Vdc, $V_{EE} = -15$Vdc, $V_{REF}/R14 = 2.0$mA, $-55°C \le T_A \le +125°C$ for DAC-1508A-8, $0°C \le T_A \le +75°C$ for DAC-1408A, unless otherwise noted. All digital inputs at high logic level.

PARAMETER	SYMBOL	CONDITIONS	DAC-1508A/1408A MIN	TYP	MAX	UNITS
Relative Accuracy (error relative to full-scale I_O)	E_r					
DAC-1508A-8, DAC-1408A-8			—	—	±0.19	
DAC-1408A-7			—	—	±0.39	%IFS
DAC-1408A-6			—	—	±0.78	
Settling Time to within 1/2 LSB (includes t_{PLH})	t_S	$T_A = +25°C$, Note 1	—	250	—	ns
Propagation Delay Time	t_{PLH}, t_{PHL}	$T_A = +25°C$, Note 1	—	30	100	ns
Output Full-Scale Current Drift	TCI_O		—	±20	—	ppm/°C
Digital Input Logic Levels (MSB)						
High Level, Logic "1"	V_{IH}		2.0	—	—	Vdc
Low Level, Logic "1"	V_{IL}		—	—	0.8	
Digital Input Current (MSB)	I_{IH}	High Level, $V_{IH} = 5.0V$	—	0	0.04	mA
	I_{IL}	Low Level, $V_{IL} = 0.8V$				
Reference Input Bias Current (Pin 15)	I_{15}		—	−1.0	−3.0	μA
Output Current Range	I_{OR}	$V_{EE} = -5.0V$	0	2.0	2.1	mA
		$V_{EE} = -6.0V$ to $-15V$	0	2.0	4.2	
Output Current	I_O	$V_{REF} = 2.000V$, R14 = 1000Ω	1.9	1.99	2.1	mA
Output Current	$I_{O(min)}$	All bits low	—	0	4.0	μA
Output Voltage Compliance ($E_r \le 0.19\%$ at $T_A = +25°C$)	V_O	$I_{REF} = 1mA$				
		$V_{EE} = -5$	—	—	−0.6, +0.5	Vdc
		V_{EE} below −10V	—	—	−5.0, +0.5	
Reference Current Slew Rate	SRI_{REF}		—	4.0	—	mA/μs
Output Current Power Supply Sensitivity	$PSSI_{O-}$		—	0.5	2.7	μA/V
Power Supply Current	I_{CC}	All bits low	—	+9	+14	mA
	I_{EE}		—	−7.5	−13	
Power Supply Voltage	V_{CCR}	$T_A = +25°C$	+4.5	+5.0	+5.5	Vdc
	V_{EER}		−4.5	−15	−16.5	
Power Dissipation	P_d	All bits low				mW
		$V_{EE} = -5.0$Vdc	—	82	135	
		$V_{EE} = -15$Vdc	—	157	265	
		All bits high				
		$V_{EE} = -5.0$Vdc	—	70	—	
		$V_{EE} = -15$Vdc	—	132	—	

NOTE: Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.085 × 0.062 inch

2. GROUND
3. V_{EE}
4. I_O
5. A1 (MSB)
6. A2
7. A3
8. A4
9. A5
10. A6
11. A7
12. A8 (LSB)
13. V_{CC}
14. V_{REF} (+)
15. V_{REF} (−)
16. COMP

Refer to Section 2 for additional DICE informaiton

ELECTRICAL CHARACTERISTICS at 25° C; V+ = 5V, V− = 15V, I_{REF} = 2.0mA, unless otherwise noted.

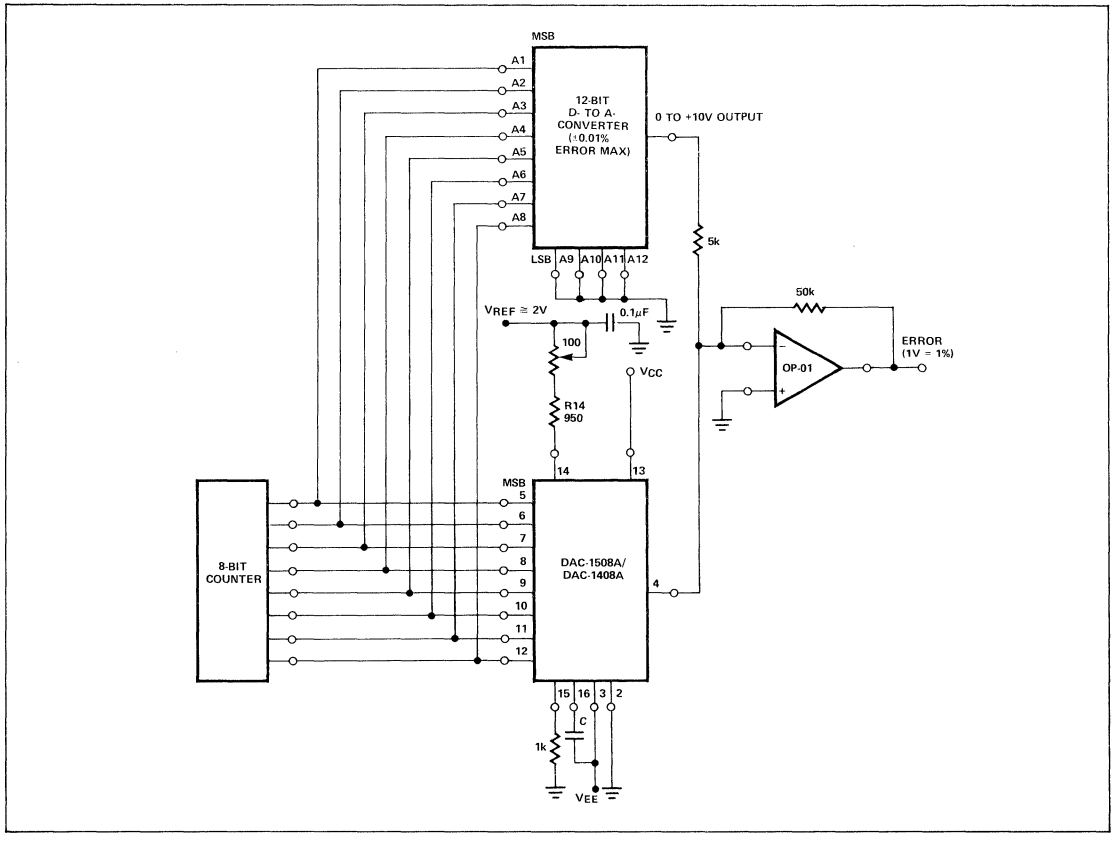
PARAMETER	SYMBOL	CONDITIONS	DAC-1408A-G LIMIT	UNITS
Resolution			8	Bits MIN
Monotonicity			8	Bits MIN
Nonlinearity			±0.9	%FS MAX
Output Voltage Compliance	V_{OS}	Full Scale Current Change < 1/2 LSB V− = −5V	+0.5	V MAX
			+0.6	V MIN
		V− below +10V	0.5	V MIN
Full Scale Current	I_{FS}	V_{REF} = 2.000V, R_{14}, R_{15} = 1.000kΩ	2.0, ±0.1	mA MAX
Zero Scale Current	I_{ZS}	(All Bits Low)	4.0	μA MAX
Output Current Range	I_{OR}	V− = −5.0V	2.1	mA MIN
		V− = −7.0V to −15V	4.2	
Logic "0" Input Level	V_{IL}		0.8	V MAX
Logic "1" Input Level	V_{IH}		2.0	V MIN
Logic Input Current				
Logic "0"	I_{IL}	Low Level, V_{IL} = −0.8V	±10	μA MAX
Logic "1"	I_{IH}	High Level, V_{IH} = 5.0V	±10	
Reference Bias Current	I_{15}		−3.0	μA MAX
Output Current Power Supply Sensitivity	$PSSI_{O-}$		2.7	μA/V MAX
Power Supply Current (All Bits Low)	I+		+14	mA MAX
	I−	−13		
Power Supply Voltage Range	V_{CCR}	−16.5	+5.0, ±0.5	mA MAX
	V_{EER}		−4.5	mA MIN
Power Dissipation (All Bits Low)	P_d	V− = −5.0V	135	mW MAX
		V− = −15V	265	

TYPICAL ELECTRICAL CHARACTERISTICS at V+ = +5V, V− = −15V, T_A = 25° C, V_{LC} and I_{OUT} connected to ground, and I_{REF} = 2.0mA, unless otherwise noted. Output characteristics refer to I_{OUT} only.

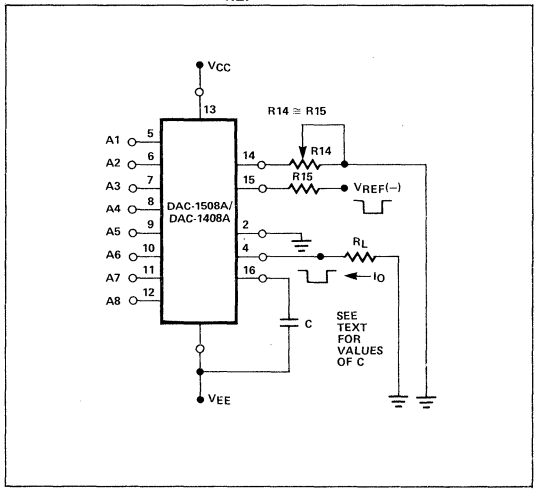
PARAMETER	SYMBOL	CONDITIONS	DAC-1408G TYPICAL	UNITS
Reference Input Slew Rate	dI/dt		4.0	mA/μs
Propagation Delay	t_{PLH}, t_{PHL}	Any Bit	30	ns
Settling Time	t_S	To ±1/2 LSB, All Bits Switched ON or OFF	250	ns

APPLICATIONS

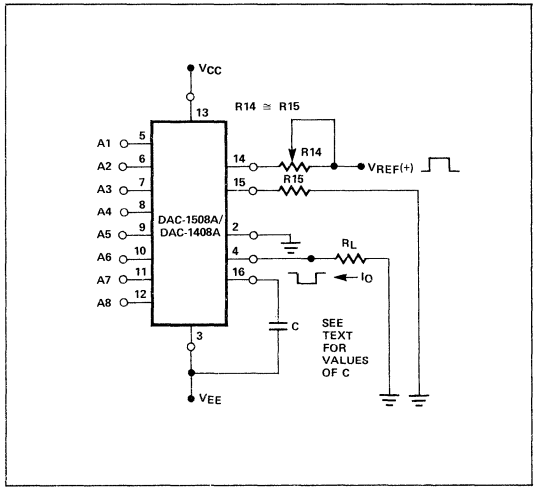
RELATIVE ACCURACY TEST CIRCUIT



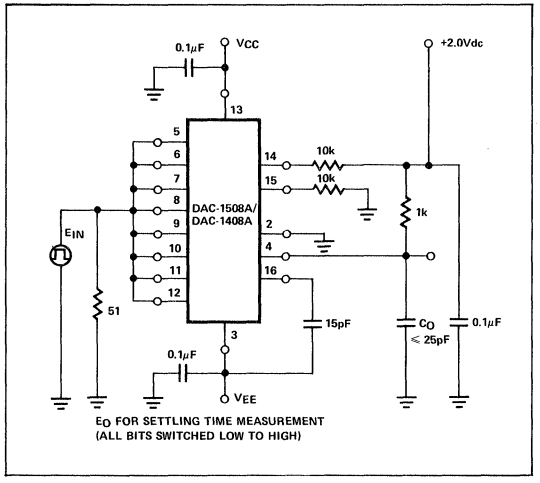
USE WITH NEGATIVE V_{REF}



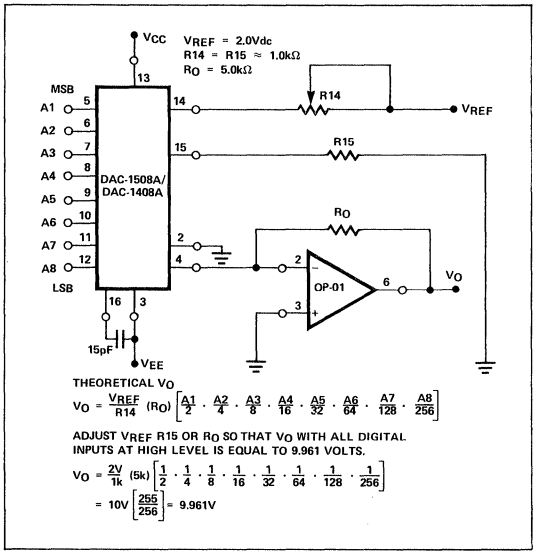
USE WITH POSITIVE V_{REF}



TRANSIENT RESPONSE AND SETTLING TIME TEST CIRCUIT



USE WITH CURRENT-TO-VOLTAGE CONVERTING OP AMP



GENERAL INFORMATION AND APPLICATION NOTES

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at Pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I_{14}, must always flow into Pin 14 regardless of the setup method or reference voltage polarity. Connections for a positive voltage are shown on the preceeding page. The reference voltage source supplies the full current I_{14}. The Preceeding bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1.0, 2.5 and 5.0kΩ, minimum capacitor values are 15, 37, and 75pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on Pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 4.0V above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at Pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5.0V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to +5.0V through another resistor and bypassing the junction of the two resistors with 0.1μF to ground. For reference voltages greater than 5.0V, a clamp diode is recommended between Pin 14 and ground.

If Pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

The voltage on Pin 4 is restricted to a range of −0.6V to +0.5V when V_{EE} = −5V due to the current switching methods employed in the DAC-1508A-8.

The negative output voltage compliance of the DAC-1508A-8 is extended to −5.0V where the negative supply voltage is more negative than −10V. Using a full-scale current of 1.992mA and load resistor of 2.5kΩ between Pin 4 and ground will yield a voltage output of 256 levels between 0 and −4.980V. The value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500Ω do not significantly affect performance but a 2.5kΩ load increases "worst case" settling time to 1.2μs (when all bits are switched on). Refer to the subsequent text section of Settling Time for more details on output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2mA may be used only for negative supply voltages more negative than −0.7V, due to the increased voltage drop across the resistors in the reference current amplifier.

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current. The relative accuracy of the DAC-1508A-8 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC-1508A-8 has a very low full-scale current drift with temperature.

The DAC-1508A-8/DAC-1408A Series is guaranteed accurate to within ±1/2 LSB at a full-scale output current of 1.992mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0mA, with the loss of one LSB (8.0μA) which is the ladder remainder shunted to ground. The input current to Pin 14 has a guaranteed value of between 1.9 and 2.1mA, allowing some mismatch in the NPN current source pair. Testing relative accuracy is accomplished by the circuit labelled "Relative Accuracy Test Circuit". The 12-bit converter is calibrated for a full-scale output current of 1.992mA. This is an optional step since the DAC-1508A-8 accuracy is essentially the same between 1.5 and 2.5mA. Then the DAC-1508A-8 circuit's full-scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D/A converters may not be used to construct a 16-bit accuracy D/A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65, 536, or ±0.00076% which is much more accurate than the ±0.19% specification provided by the DAC-1508A-8.

MULTIPLYING ACCURACY

The DAC-1508A-8 may be used in the multiplying mode with eight-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16μA to 4.0mA, the additional error contributions are less than 1.6μA. This is well within eight-bit accuracy when referred to full scale.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the DAC-1508A-8 is monotonic for all values of reference current above 0.5mA. The recommended range for operation with a DC reference current is 0.5 to 4.0mA.

SETTLING TIME

The "worst case" switching condition occurs when all bits are switched "ON", which corresponds to a low-to-high transition for all bits. This time is typically 250ns for settling to within ±1/2 LSB, for 8-bit accuracy, and 200ns to 1/2 LSB for 7 and 6-bit accuracy. The turn off is typically under 100ns. These times apply when $R_L \leq 500\Omega$ and $C_O \leq 25pF$.

The slowest single switch is the least significant bit. In applications where the D/A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 250ns may be realized.

Extra care must be taken in board layout since this is usually the cominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

JM38510/11301/11302

JAN 8-BIT DIGITAL-TO-ANALOG CONVERTER

GENERAL DESCRIPTION

This data sheet covers the electrical requirements of the monolithic 8-bit Digital-to-Analog Converters found in MIL-M-38510/113. Devices supplied to this data sheet are manufactured and tested at PMI's MIL-M-38510 certified facility and are listed in QPL-38510.

Complete device requirements will be found in MIL-M-38510 and MIL-M-38510/113 for Class B processed devices.

Device types shall be as follows:

01 D/A Converter, 8 bit, 0.19% linearity
02 D/A Converter, 8 bit, 0.10% linearity

GENERIC CROSS-REFERENCE INFORMATION

This cross-reference information is presented for the convenience of the user. The Generic-Industry types listed may not have identical operational performance characteristics across the military temperature range or the reliability factor equivalent to the MIL-M-38510/113 devices.

Military Device Type	Generic Industry Type
01	DAC-08
02	DAC-08A

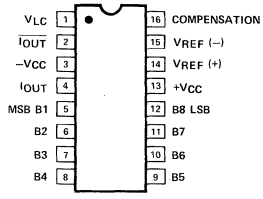
CASE OUTLINE

Per MIL-M-38510, Appendix C, Case Outline D-2 (16 Lead 1/4″ x 7/8″, dual-in-line). Package type designator "E".

POWER AND THERMAL CHARACTERISTICS

Package	Case outline	Maximum allowable power dissipation	Maximum θJ — C	Maximum θJ — A
Dual-in-line	E	400mW at $T_A = 125°C$	35°C/W	120°C/W

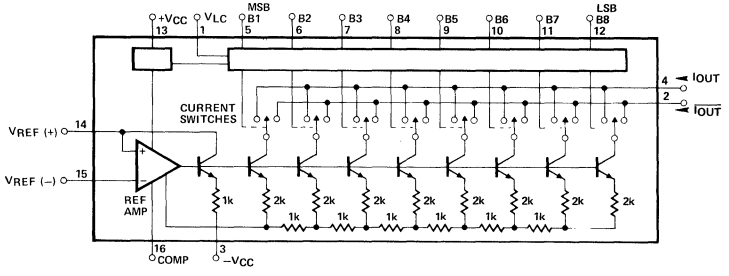
PIN CONNECTIONS & ORDERING INFORMATION



Jan Device	PMI Device Type	Linearity
JM38510/11301BEC	DAC08Q1/38510	0.19%
JM38510/11302BEC	DAC08AQ1/38510	0.10%
JM38510/11301BEB	DAC08Q2/38510	0.19%
JM38510/11302BEB	DAC08AQ2/38510	0.10%

NOTE: Lead finish as follows
BEC: Gold Plate, side braze package
BEB: Tin Plate, CERDIP package

SIMPLIFIED SCHEMATIC



Manufactured under one or more of the following patents:
4,055,773; 4,056,740; 4,092,639

ABSOLUTE MAXIMUM RATING

Supply Voltage [$+V_{CC} - (-V_{CC})$] 36Vdc
Voltage, Digital Input to Negative Supply
[$V_{logic} - (-V_{CC})$] ..... 0 to 36Vdc
Voltage, Logic Control (V_{LC}) ..... $-V_{CC}$ to $+V_{CC}$
Reference Voltage Input [(V_{14}, V_{15})] ..... $-V_{CC}$ to $+V_{CC}$

Reference Input Current (I_{14}) 5.0mA
Reference Input Differential Voltage [($V_{14} - V_{15}$)] .. ±18Vdc
Lead Temperature (Soldering, 60 sec.) ..... 300°C
Junction Temperature ..... 175°C
Storage Temperature ..... −65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... ±5Vdc to ±15Vdc*

Ambient Temperature Range ..... −55°C to +125°C

***NOTE:**
A slight degradation in linearity can occur when the supply voltage is near the ±5V end of the recommended operating range.

ELECTRICAL CHARACTERISTICS at $\pm V_{CC}$ = ±15Vdc; Source resistance = 50 ohms; I_{REF} = 2.0mA; Figure 1; Ambient temperature range = −55°C to +125°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	01 limits MIN	01 limits MAX	02 limits MIN	02 limits MAX	UNITS
Monotonicity	$\Delta(i)$	Measure I_O, $(I_{ON} - I_{ON-1}) \geq 0$ at each major carry point	0	16.0	0	16.0	µA
	$\Delta(\overline{i})$	Measure $\overline{I_O}$, $(\overline{I_{ON}} - \overline{I_{ON-1}}) \geq 0$ at each major carry point	0	16.0	0	16.0	
Output Symmetry	ΔI_{FS}	$I_{FS} - \overline{I_{FS}}$	−8.0	8.0	−4.0	4.0	µA
Full Scale Current Temperature Coefficient	$T_C(I_{FS})$	All input bits high, Measure I_O	−50.0	50.0	−50.0	50.0	ppm/°C
	$T_C(\overline{I_{FS}})$	All input bits low, Measure $\overline{I_O}$					
Full Scale Current	I_{FS}	All input bits high, T_A = 25°C Measure I_O	1.94	2.04	1.984	2.000	mA
	$\overline{I_{FS}}$	All input bits low, T_A = 25°C Measure $\overline{I_O}$					
Zero Scale Current	I_{ZS}	All input bits low, Measure I_O	−2.0	2.0	−1.0	1.0	µA
	$\overline{I_{ZS}}$	All input bits high, Measure $\overline{I_O}$					
Positive Bit Errors	ΣNL^+	Measure I_O (ΣPositive bit errors)/IFS	0	0.19	0	0.10	%
	$\Sigma\overline{NL}^+$	Measure $\overline{I_O}$ (ΣPositive bit errors)/$\overline{IFS}$					
Negative Bit Errors	ΣNL^-	Measure I_O (ΣNegative bit errors)/IFS	−0.19	0	−0.10	0	%
	$\Sigma\overline{NL}^-$	Measure $\overline{I_O}$ (ΣNegative bit errors)/$\overline{IFS}$					
Positive and Negative Bit Error Difference	$\Delta\Sigma NL$	Measure I_O $\lvert\Sigma NL^+\rvert - \lvert\Sigma NL^-\rvert$	−0.05	0.05	−0.03	0.03	%
	$\Delta\Sigma\overline{NL}$	Measure $\overline{I_O}$ $\lvert\Sigma\overline{NL}^+\rvert - \lvert\Sigma\overline{NL}^-\rvert$					
Positive Relative Accuracy	NL^+	Measure I_O $\lvert\Sigma NL^+\rvert + \lvert\Delta\Sigma NL\rvert$	0	0.19	0	0.10	%
	$\overline{NL}^+$	Measure $\overline{I_O}$ $\lvert\Sigma\overline{NL}^+\rvert + \lvert\Delta\Sigma\overline{NL}\rvert$					
Negative Relative Accuracy	NL^-	Measure I_O $\lvert\Sigma NL^-\rvert + \lvert\Sigma NL\rvert$	0	0.19	0	0.10	%
	$\overline{NL}^-$	Measure $\overline{I_O}$ $\lvert\Sigma\overline{NL}^-\rvert + \lvert\Delta\Sigma\overline{NL}\rvert$					

ELECTRICAL CHARACTERISTICS at $\pm V_{CC} = \pm 15$Vdc; Source resistance = 50 ohms; $I_{REF} = 2.0$mA; Figure 1; Ambient temperature range = −55°C to +125°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	01 limits MIN	01 limits MAX	02 limits MIN	02 limits MAX	UNITS
Output Current Range	$I_{FS}R_1$	All input bits high, Measure I_O, $-V_{CC} = -10V$, $V_{REF} = 15V$	2.1	—	2.1	—	mA
	$\overline{I_{FS}R_1}$	All input bits low, Measure $\overline{I_O}$, $-V_{CC} = -10V$, $V_{REF} = 15V$					
	$I_{FS}R_2$	All input bits high, Measure I_O $-V_{CC} = -12V$, $V_{REF} = 25V$	4.2	—	4.2	—	
	$\overline{I_{FS}R_2}$	All input bits low, Measure $\overline{I_O}$, $-V_{CC} = -12V$, $V_{REF} = 25V$					
Reference Bias Current	$I_{REF}-$	All input bits low	−3.0	0	−3.0	0	μA
High Level Input Current	I_{IH}	All input bits $V_{IN} = 18V$, each input measured separately	−0.05	10.0	−0.05	10.0	μA
Low Level Input Current	I_{IL}	All input bits $V_{IN} = -10V$, each input measured separately	−10.0	—	−10.0	—	μA
Full Scale Current At +18V Compliance	$I_{FS}+$	All input bits high, Measure I_O, $V_{IO} = 18V$	1.90	2.08	1.94	2.04	mA
	$\overline{I_{FS}+}$	All input bits low, Measure $\overline{I_O}$, $V_{\overline{IO}} = 18V$					
Full Scale Current At −10V Compliance	$I_{FS}-$	All input bits high, Measure I_O, $V_{IO} = -10V$	1.90	2.08	1.94	2.04	mA
	$\overline{I_{FS}-}$	All input bits low, Measure $\overline{I_O}$, $V_{\overline{IO}} = -10V$					
Change In Full Scale Current Due to Voltage Compliance	ΔI_{FSC}	All input bits high, Measure I_O, $25°C \le T_A \le 125°C$ $T_A = -55°C$ $V_{IO} = 18V$ to $-10V$	−4.0 −8.0	4.0 8.0	−4.0 −8.0	4.0 8.0	μA
	$\Delta\overline{I_{FSC}}$	All input bits low, Measure $\overline{I_O}$, $25°C \le T_A \le 125°C$ $T_A = -55°C$ $V_{\overline{IO}} = 18V$ to $-10V$	−4.0 −8.0	4.0 8.0	−4.0 −8.0	4.0 8.0	
Power Supply Sensitivity From $+V_{CC}$	$P_{SS}I_{FS}+1$	All input bits high, Measure I_O, $+V_{CC} = 4.5V$ to $+5.5V$, $-V_{CC} = -18V$	−4.0	4.0	−4.0	4.0	μA
	$\overline{P_{SS}I_{FS}+1}$	All input bits low, Measure $\overline{I_O}$, $+V_{CC} = 4.5V$ to $+5.5V$, $-V_{CC} = -18V$					
	$P_{SS}I_{FS}+2$	All input bits high, Measure I_O, $+V_{CC} = 12V$ to $18V$, $-V_{CC} = -18V$	−8.0	8.0	−8.0	8.0	
	$\overline{P_{SS}I_{FS}+2}$	All input bits low, Measure $\overline{I_O}$, $+V_{CC} = 12V$ to $18V$, $-V_{CC} = -18V$					
Power Supply Sensitivity From $-V_{CC}$	$P_{SS}I_{FS}-1$	All input bits high, Measure I_O, $+V_{CC} = 18V$, $-V_{CC} = -12V$ to $-18V$	−8.0	8.0	−8.0	8.0	μA
	$\overline{P_{SS}I_{FS}-1}$	All input bits low, Measure $\overline{I_O}$, $+V_{CC} = 18V$, $-V_{CC} = -12V$ to $-18V$					
	$P_{SS}I_{FS}-2$	All input bits high, Measure I_O, $+V_{CC} = 18V$, $-V_{CC} = -4.5V$ to $-5.5V$ $I_{REF} = 1mA$	−2.0	2.0	−2.0	2.0	
	$\overline{P_{SS}I_{FS}-2}$	All input bits low, Measure $\overline{I_O}$, $+V_{CC} = 18V$, $-V_{CC} = -4.5V$ to $-5.5V$ $I_{REF} = 1mA$					

ELECTRICAL CHARACTERISTICS at $\pm V_{CC} = \pm 15$Vdc; Source resistance = 50 ohms; $I_{REF} = 2.0$mA; Figure 1; Ambient temperature range = −55°C to +125°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	01 limits MIN	01 limits MAX	02 limits MIN	02 limits MAX	UNITS
Supply Current From $+V_{CC}$	I_{CC}^+	All input bits high	0.4	3.8	0.4	3.8	mA
Supply Current from $-V_{CC}$	I_{CC}^-	All input bits high	−7.8	−0.8	−7.8	−0.8	mA
Propagation Delay Time, High-to-Low Level	t_{PHL}	Figure 2, Measure V_O	6.0	60.0	6.0	60.0	ns
Propagation Delay Time, Low-to-High Level	t_{PLH}	Figure 2, Measure V_O	6.0	60.0	6.0	60.0	ns
Reference Amplifer Input Slew Rate	dI_O/dt $T_A = 25°C$	Figure 3, Measure V_O	1.5	—	1.5	—	mA/μs
Settling Time High-to-Low Level	t_{SHL} $T_A = 25°C$	Figure 2, Output within ½ LSB of final value of I_O	10	135	10	135	ns
Settling Time Low-to-High Level	t_{SLH} $T_A = 25°C$	Figure 2, Output within ½ LSB of final value of I_O	10	135	10	135	ns

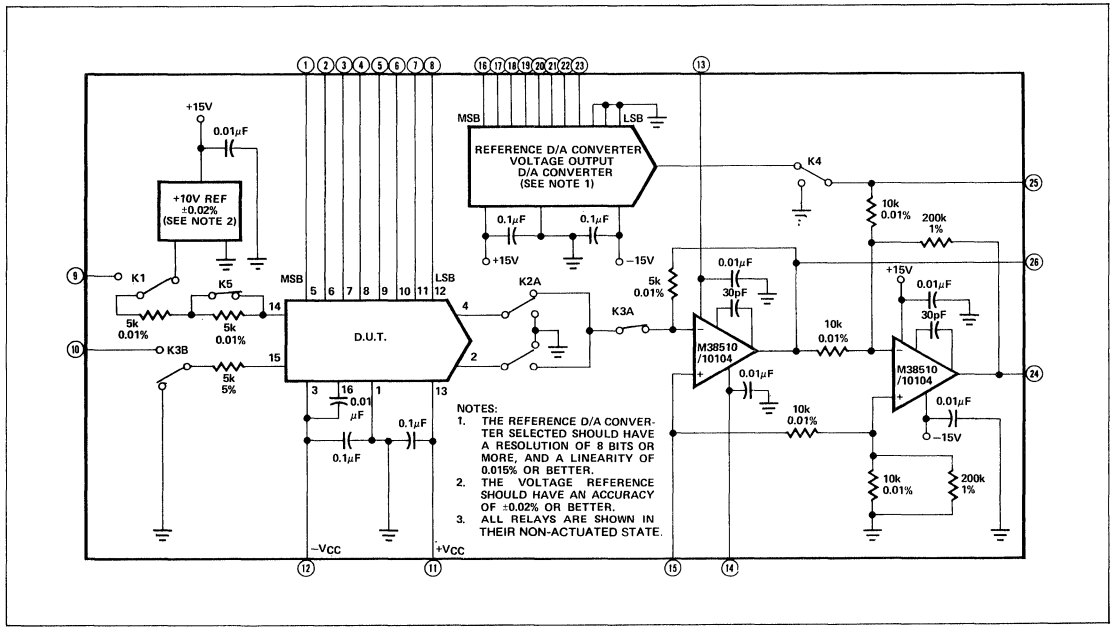


Figure 1. Test Circuit For Static Tests

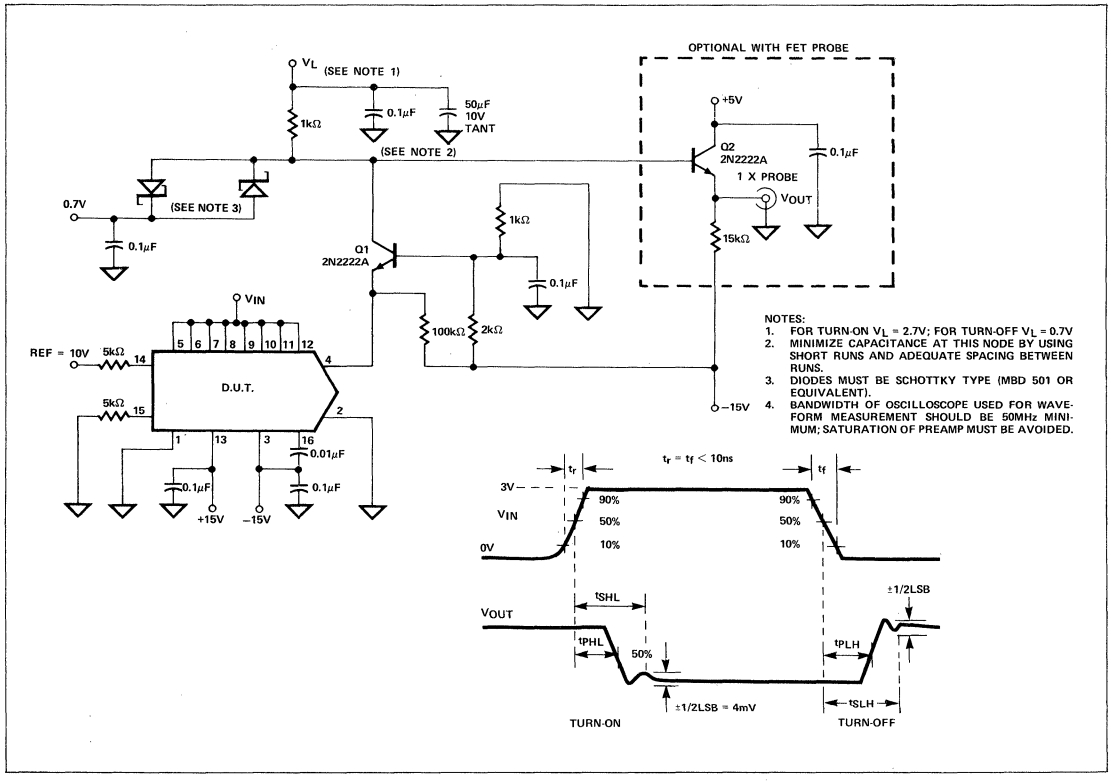


Figure 2. Test Circuit For Propagation Delay and Settling Time, Device Types 01 and 02.

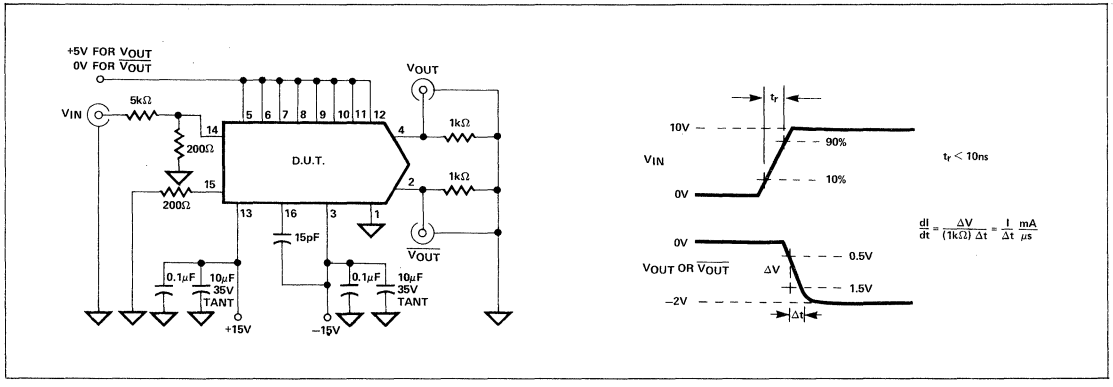


Figure 3. Test Circuit For Slew Rate, Device Types 01, 02.

BURN-IN

Devices supplied by PMI have been subjected to burn-in per method 1015 of MIL-STD-883 using test condition C or test condition F with the circuit shown in Figure 4.

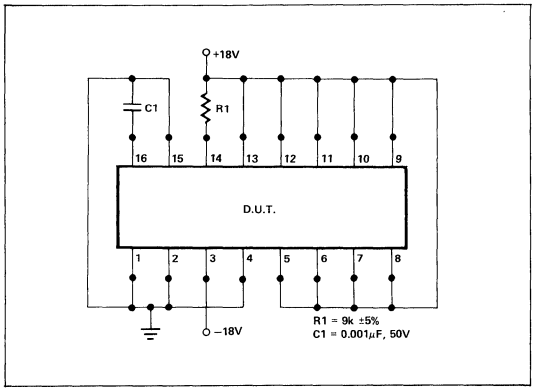


Figure 4. Test Circuit, Burn-In and Operating Life Test.

SECTION 11

MULTIPLEXERS ANALOG SWITCHES

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MULTIPLEXERS/ANALOG SWITCHES

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INTRODUCTION

Analog multiplexers and switches find applications in data acquisition, metrology, telemetry, process control and telephony systems. Multiplexers are multiple analog switches which share a common output. An on-chip address decoder selects the appropriate input by means of a binary code. All channels may be deactivated by an enable/disable control pin.

In the past multiplexers/switches have been manufactured with hybrid, monolithic CMOS or dielectrically isolated CMOS technologies. The merging of ion implant techniques with the standard bipolar process creates a fourth technological alternative — The BIFET process. High-quality ion implanted p-channel FET's can now be compatibly processed with bipolar devices.

The cost of hybrid devices limits their use to applications which require the extremely low "R_{ON}" resistance made possible by discrete FET's. MOS technologies are inherently plagued by SCR "latch up" problems and analog signal overvoltage destruction. The use of buried layers and expensive dielectric isolation processing can eliminate the SCR failure mode, but the overvoltage blowout problems can be solved only by adding large series input resistance with each switch. This increases system errors since the equivalent "R_{ON}" may typically be over 1000 ohms.

BIFET switches have no SCR "latch up" tendency and can withstand analog input overvoltages while maintaining low "R_{ON}" resistance. In addition, the special handling required with CMOS devices is not necessary with BIFET switches.

In selecting analog multiplexers attention must be paid to several key specs. Break-before-make switching insures no two-channel inputs are simultaneously connected. This prevents input sensor damage and misoperation. Acquiring analog input signals within a specified time and error band are primary concerns affected by "R_{ON}" resistance and "C_{OUT}" capacitance specifications. A low "R_{ON}" insures minimum signal attenuation and maximum accuracy. The "C_{OUT}" capacitance forms on R-C time constant with "R_{ON}" placing fundamental limits on signal acquisition time. Low "R_{ON}" and "C_{OUT}" insures minimum elapsed time between the channel select command and the acquisition of data to within a specified error band. High cross talk and off isolation specifications prevent unselected input signals from affecting the signal path.

PMI offers a wide selection of single-ended and differential multiplexers and switches. Sixteen and eight-channel multiplexers as well as differential eight and four-channel devices are available. Dual and Quad SPST switches in normally closed and open configurations are also available. All devices are pin-for-pin replacements for many industry standard CMOS devices.

ANALOG MULTIPLEXER AND SWITCH DEFINITIONS

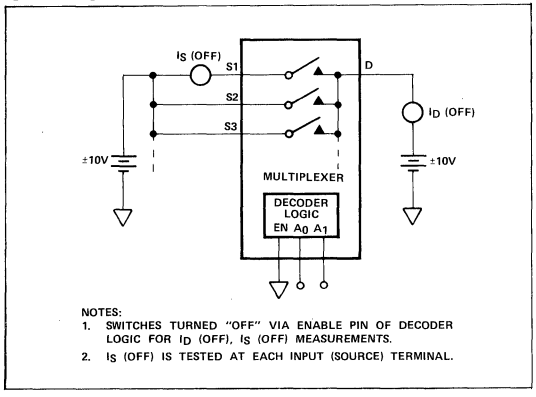
ANALOG INPUT LEAKAGE CURRENT ($I_{S(OFF)}$)

The algebraic sum of diode current losses from an "OFF"-channel source input to the power supplies, ground and through the channel. Specified as an absolute value, as the direction of current flow is not predictable.

ANALOG OUTPUT LEAKAGE CURRENT ($I_{D(OFF)}$)

The algebraic sum of diode current losses from an "OFF"-channel "D" output to the power supplies, ground and through the channel. Specified as an absolute value, as the direction of current flow is not predictable.

I_D(OFF), I_S(OFF) TEST CONDITION DEFINITIONS



NOTES:
1. SWITCHES TURNED "OFF" VIA ENABLE PIN OF DECODER LOGIC FOR I_D (OFF), I_S (OFF) MEASUREMENTS.
2. I_S (OFF) IS TESTED AT EACH INPUT (SOURCE) TERMINAL.

ANALOG INPUT-TO-INPUT CAPACITANCE ($C_{DS(OFF)}$)

The equivalent capacitance which shunts as open switch effectively between "S" and "D" output.

ANALOG INPUT CAPACITANCE ($C_{S(ON)}$)

The capacitance between an analog "S" input and ground with the channel "ON".

ANALOG INPUT CAPACITANCE ($C_{S(OFF)}$)

The capacitance between an analog (S) input and ground with the channel "OFF."

ANALOG OUTPUT CAPACITANCE ($C_{D(OFF)}$)

The capacitance between the analog (DRAIN) output and ground with the channel "OFF." High-frequency transmission and output settling time characteristics are highly influenced by this parameter in conjunction with R_{ON}.

ANALOG OUTPUT CAPACITANCE ($C_{D(ON)}$)

The capacitance between the analog "D" output and ground with the channel "ON".

BREAK-BEFORE-MAKE DELAY (t_{DLY})

The elapsed time between the turn-off of one analog input and the subsequent turn-on of another input as determined by the appropriate instantaneous change in the digital input code for both inputs measured between the outputs' 50% transition points.

CHANNEL CAPACITANCE ($C_{SS(OFF)}$, $C_{DD(OFF)}$)

The capacitance between the D(S) teminals of any two channels.

CROSSTALK (CT)

The proportionate amount of cross-coupling from an "OFF" analog input channel to the output of another "ON" output channel, expressed in dB.

DIGITAL INPUT CAPACITANCE (C_{DIG})

The capacitance between a digital input and ground.

LOGIC "0" INPUT CURRENT (I_{INL})

The current flowing into a digital input when a specified low-level voltage is applied to that input.

LOGIC "0" INPUT VOLTAGE LEVEL (V_{INL})

The maximum (or most-positive) digital low-level input voltage for which proper operation of the device is guaranteed.

LOGIC "1" INPUT VOLTAGE LEVEL (V_{INH})

The minimum (or least-positive) digital high-level input voltage for which proper operation of the device is guaranteed.

NEGATIVE VOLTAGE SUPPLY (V−)

The most negative voltage supply with respect to ground.

POSITIVE VOLTAGE SUPPLY (V+)

The most positive voltage supply with respect to ground.

"OFF" ISOLATION (ISO_{OFF})

The proportionate amount of a high-frequency analog input signal which is coupled through the channel of an "OFF" device. This feedthrough is transmitted through $C_{DS(OFF)}$ to a load comprised of $C_{D(OFF)}$ in parallel with an external load. Isolation generally decreases by 6dB/octave with increasing frequency.

"ON" RESISTANCE (R_{ON})

The series "ON" — channel resistance measured between addressed "S" input and "D" output terminals under specified conditions.

"ON" RESISTANCE MATCH (R_{ON} MATCH)

The channel-to-channel matching of "ON" resistance when channels are operated under identical conditions.

$$R_{ON}\ \text{MATCH} = \frac{R_i - R_{AVG}}{R_{AVG}} \times 100\%$$

where

N = # of channels in package (i.e., for MUX-08 N = 8, for MUX-16 N = 16, etc.)

R_i = Each channel's "ON" resistance

$$R_{AVG} = \frac{\sum_{i=1}^{N} R_i}{N}$$

"ON" RESISTANCE VARIATION (ΔR_{ON})

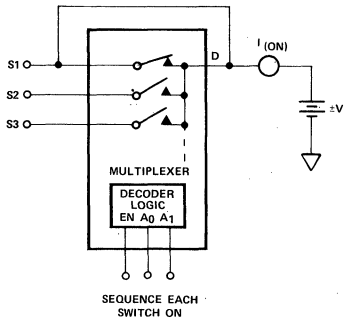
The variation of "ON" resistance produced by the specified analog input voltage change with a constant load current.

$$\Delta R_{ON}\,(\%) = \frac{R_{ON}|V_A = -10V - R_{ON}|V_A = +10V}{R_{ON}|V_A = 0V} \times 100\%$$

"ON" CHANNEL ANALOG LEAKAGE CURRENT ($I_{D(ON)} + I_{S(ON)}$)

Current loss (or gain) through an "ON"-channel creating a voltage offset across the device. As the direction of current flow is not predictable, only the magnitude is specified at various temperature ranges.

I(ON) TEST CONDITION DEFINITIONS



NOTES:
1. TEST IS REPEATED FOR EACH SWITCH WITH SOURCE CONNECTED TO DRAIN.
2. V_D = +10V AND −10V.

OUTPUT ENABLE DELAY TIME "OFF" ($t_{OFF(EN)}$) — MULTIPLEXERS

The time required to disconnect the analog output from the analog input determined by the digital address input code. It is measured from the 50% point of ENABLE input logic change to the time the input output reaches 10% of the initial value.

OUTPUT ENABLE DELAY TIME "ON" ($t_{ON(EN)}$) — MULTIPLEXERS

The time required to connect the analog output to the analog input determined by the digital address input code. It is measured from the 50% point of the ENABLE input logic change to the time the output is within 90% of final value.

OUTPUT "ON" SWITCHING TIME (t_{ON})

The time required to connect the analog output to the analog input. The time is measured from the 50% point of the logic input change to the time the output reaches 90% of the final value.

OUTPUT "OFF" SWITCHING TIME (t_{OFF})

The time required to disconnect the analog output from the analog input. The time is measured from the 50% point of the logic input change to the time the output reaches 10% of the initial value.

OUTPUT SETTLING TIME (t_s)

The elapsed time for the analog output to reach its final value within a specified error band after the corresponding digital input code has been changed. It is measured from the 50% point of the logic input change to the time the output reaches final value within the specified error band.

SWITCHING TIME (t_{TRAN}) — MULTIPLEXERS

The time required to switch and slew from one analog input channel to another analog input with a full-scale differential between inputs with a high impedance output load. The time is measured from the 50% point of the logic input change to the time the output reaches 90% of the final value.

MUX-08/MUX-24

8-CHANNEL/DUAL 4-CHANNEL BI-FET ANALOG MULTIPLEXERS

OVERVOLTAGE AND POWER SUPPLY LOSS PROTECTED

FEATURES

- **MUX-08 Pin Compatible with DG508, HI-508A, LF11508/12508/13508, AD7506**
- **MUX-24 Pin Compatible with DG509, HI-509A, LF11509/12509/13509, AD7507**
- **JFET Switches Rather Than CMOS**
- **Highly Resistant to Static Discharge Damage**
- **No SCR Latch-up Problems**
- **Low "ON" Resistance ..... 220Ω Typical**
- **Low Output Leakage Current ..... 100nA Maximum**
- **Digital Inputs Compatible with TTL and CMOS**
- **No Pullup Resistors Required**
- **Break-Before-Make Action**
- **Overvoltage and Power Supply Loss Protected**
- **Single Supply Operation**
- **125°C Temperature Tested Dice Available**

GENERAL DESCRIPTION

The MUX-08 is a monolithic eight-channel analog multiplexer which connects a single output to one of the eight analog inputs depending upon the state of a 3-bit binary address. Disconnection of the output is provided by a logical "0" at the ENABLE input, thereby providing a package select function.

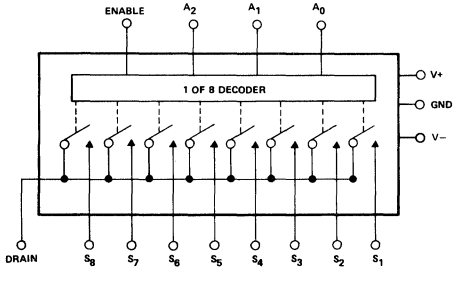
The MUX-24 is a monolithic four-channel differential analog multiplexer configured in a double pole, four—position (plus OFF) electronic switch array. A two-bit binary input address connects a pair of independent analog inputs from each four-channel input section to the corresponding pair of independent analog outputs. Disconnection of both inputs is provided by a logical "0" at the ENABLE input, thereby offering a package select function.

Fabricated with Precision Monolithics' high performance BIFET technology, these devices offer low, constant "ON" resistance. Performance advantages include low leakage currents and fast settling time with low crosstalk to satisfy a wide variety of applications. These multiplexers do not suffer from latch-up or static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pull-up resistors over the full operating temperature range.

For single sixteen-channel and dual eight channel models, refer to the MUX-16/MUX-28 data sheet.

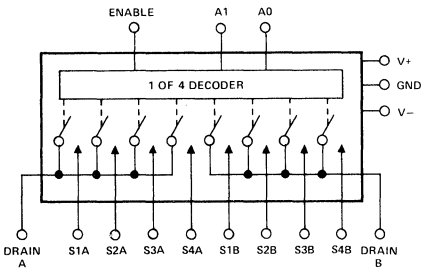
FUNCTIONAL DIAGRAM AND TRUTH TABLE

MUX-08



LOGIC STATE				CHANNEL STATE
A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

MUX-24



A_1	A_0	EN	"ON" CHANNEL
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

ABSOLUTE MAXIMUM RATINGS (Note)

Operating Temperature Range,
- MUX-08/24-AQ, BQ ..... −55°C to +125°C
- MUX-08/24-EQ, FQ ..... −25°C to +85°C
- MUX-08/24-EP, FP ..... 0°C to +70°C

DICE Junction Temperature (T_j) ..... −65°C to +150°C
Storage Temperature Range ..... −65°C to +150°C
Power Dissipation 500mW
Derate above 100°C (Q Package) ..... 10mW/°C
Lead Soldering Temperature ..... 300°C (60 SEC)
Maximum Junction Temperature ..... 150°C
V+ Supply to V− Supply 36V
Logic Input Voltage (Note 5) ..... −4V to V+ Supply
Analog Input Voltage .... V− Supply −20V to V+ Supply +20V
Maximum Current Through Any Pin 25mA

NOTE: Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V+ = 15V, V− = −15V and T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		MUX-08A/E MUX-24A/E MIN	TYP	MAX	MUX-08B/F MUX-24B/F MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	$V_D \le 10V$, $I_D \le 200\mu A$		–	220	300	–	300	400	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \le V_D \le 10V$, $I_S = 200\mu A$		–	1.0	5	–	3.0	7	%
R_{ON} Match Between Switches	R_{ON} Match	$V_D \le 10V$, $I_S = 200\mu A$		–	7	15	–	9	20	%
Analog Voltage Range	V_A	$I_S = 100\mu A$		+10 −10	+10.4 −15	– –	+10 −10	+10.4 −15	– –	Volts
Source Current (Switch "OFF")	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Note 1)		–	0.01	1.0	–	0.01	2.0	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Note 1)	MUX-08	–	0.1	1.0	–	0.1	2.0	nA
			MUX-24	–	0.05	1.0	–	0.05	2.0	nA
Leakage Current (Switch "ON")	$I_{D(ON)}$ $+I_{S(ON)}$	$V_D = 10V$ (Note 1)	MUX-08	–	0.1	1.0	–	0.1	2.0	nA
			MUX-24	–	0.05	1.0	–	0.05	2.0	
Digital "1" Input Voltage	V_{INH}			2.0	–	–	2.0	–	–	Volts
Digital "0" Input Voltage	V_{INL}			–	–	0.8	–	–	0.8	Volts
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V		–	1.0	10	–	1.0	10	μA
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.4V$		–	4.0	10	–	4.0	10	μA
Digital Input Capacitance	C_{DIG}			–	3.0	–	–	3.0	–	pF
Switching Time	t_{TRAN}	Figure 1 (Note 2)		–	1.0	1.3	–	1.5	2.1	μS
Output Settling Time	t_S	10V Step to 0.10%		–	1.3	–	–	1.7	–	μS
		10V Step to 0.05%		–	1.5	–	–	1.7	–	
		10V Step to 0.02%		–	2.3	–	–	1.7	–	
Break-Before-Make Delay	t_{DLY}			–	0.8	–	–	1.0	–	μS
Enable Delay "ON"	$t_{ON(EN)}$	(Note 6)	MUX-08	–	1.0	2.0	–	1.0	2.0	μS
			MUX-24	–	1.0	2.0	–	1.2	2.0	
Enable Delay "OFF"	$t_{OFF(EN)}$	(Note 6)	MUX-08	–	0.1	0.4	–	0.2	0.4	μS
			MUX-24	–	0.2	0.4	–	0.2	0.4	
"OFF" Isolation	$ISO_{(OFF)}$	(Note 4)	MUX-08	–	60	–	–	60	–	dB
			MUX-24	–	66	–	–	66	–	
Crosstalk	CT	(Note 3)	MUX-08	–	70	–	–	70	–	dB
			MUX-24	–	76	–	–	76	–	
Source Capacitance	$C_{S(OFF)}$	Switch "OFF", $V_S = 0V$, $V_D = 0V$	MUX-08	–	2.5	–	–	2.5	–	pF
			MUX-24	–	2	–	–	2	–	
Drain Capacitance	$C_{D(OFF)}$	Switch "OFF", $V_S = 0V$, $V_D = 0V$	MUX-08	–	7	–	–	7	–	pF
			MUX-24	–	4	–	–	4	–	
Input to Output Capacitance	$C_{DS(OFF)}$	(Note 4)	MUX-08	–	0.3	–	–	0.3	–	pF
			MUX-24	–	0.15	–	–	0.15	–	
Positive Supply Current (All Digital Inputs Logic "0" or "1")	I+	V+ = 15V		–	10	12.0	–	6.0	12.0	mA
		V+ = 5V		–	8.0	–	–	5.0	–	
Negative Supply Current (All Digital Inputs Logic "0" or "1")	I−	V− = −15V		–	3.0	3.8	–	2.0	3.8	mA
		V− = −5V		–	2.5	–	–	1.8	–	

NOTES:

1. Conditions applied to leakage tests insure worst case leakages. Exceeding 11V on the analog input may cause an "OFF" channel to turn "ON."
2. $R_L = 10M\Omega$, $C_L = 10pF$
3. Crosstalk is measured by driving channel 8 (3A)* with channel 4 (4A)* "ON".
   $R_L = 1M\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, f = 500kHz.
4. OFF isolation is measured by driving channel 8 (3A)* with ALL channels "OFF".
   $R_L = 1k\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, f = 500kHz. C_{CS} is computed from the OFF isolation measurement.
5. The ground (GND) pin must be ≥ 4V above the V− pin to include −4V logic levels.
6. Sample Tested

ELECTRICAL CHARACTERISTICS at V+ = 15V, V− = −15V and −55°C ≤ T_A ≤ 125°C for MUX-08AQ,BQ and MUX-24AQ,BQ, −25°C ≤ T_A ≤ +85°C for MUX-08EQ,FQ and MUX-24EQ,FQ, 0°C ≤ T_A ≤ +70°C for MUX-08EP,FP and MUX-24EP,FP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		MUX-08A/24A MIN	TYP	MAX	MUX-08B/24B MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	$V_D \leq 10V$, $I_D \leq 200\mu A$		–	–	400	–	–	500	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_D \leq 10V$, $I_S = 200\mu A$		–	1.5	–	–	4.5	–	%
R_{ON} Match Between Switches	R_{ON} Match	$V_D \leq 10V$, $I_S = 200\mu A$		–	10	–	–	15	–	%
Analog Voltage Range	V_A	$I_S = 100\mu A$		+10 −10	+10.4 −15	– –	+10 −10	+10.4 −15	– –	Volts
Source Current (Switch "OFF")	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Note 1)		–	–	10	–	–	10	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Note 1)	MUX-08	–	–	100	–	–	100	nA
			MUX-24	–	–	50	–	–	50	nA
Leakage Current (Switch "ON")	$I_{D(ON)}$ $+I_{S(ON)}$	$V_D = 10V$ (Note 1)	MUX-08	–	–	100	–	–	100	nA
			MUX-24	–	–	50	–	–	50	
Digital "1" Input Voltage	V_{INH}			2.0	–	–	2.0	–	–	Volts
Digital "0" Input Voltage	V_{INL}			–	–	0.8	–	–	0.8	Volts
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V		–	–	20	–	–	20	μA
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.4V$		–	–	20	–	–	20	μA
Positive Supply Current	I+	All Digital Inputs Logic "0" or "1"		–	–	15.0	–	–	15.0	mA
Negative Supply Current	I−	All Digital Inputs Logic "0" or "1"		–	–	5.0	–	–	5.0	mA

NOTES:
1. Conditions applied to leakage tests insure worst case leakages. Exceeding 11V on the analog input may cause an "OFF" channel to turn "ON."
2. $R_L = 10M\Omega$, $C_L = 10pF$
3. Crosstalk is measured by driving channel 8 with channel 4 "ON". $R_L = 1M\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, f = 500kHz.
4. OFF isolation is measured by driving channel 8 with ALL channels "OFF". $R_L = 1k\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, f = 500kHz. C_{CS} is computed from the OFF isolation measurement.
5. The ground (GND) pin must be ≥ 4V above the V− pin to include −4V logic levels.
6. Sample Tested

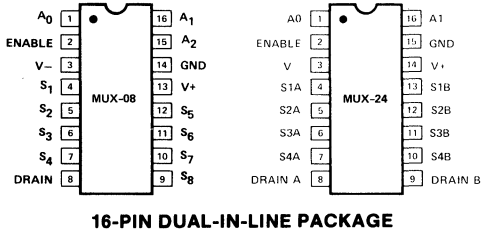
ORDERING INFORMATION†

25°C ON RESISTANCE	PACKAGE HERMETIC DIP	PACKAGE PLASTIC DIP	TEMPERATURE RANGE
220Ω	MUX08AQ*	——	MIL
	MUX08EQ	——	IND
	——	MUX08EP	COM
300Ω	MUX08BQ*	——	MIL
	MUX08FQ	——	IND
	——	MUX08FP	COM
220Ω	MUX24AQ*	——	MIL
	MUX24EQ	——	IND
	——	MUX24EP	COM
300Ω	MUX24BQ*	——	MIL
	MUX24FQ	——	IND
	——	MUX24FP	COM

* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

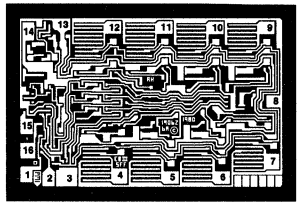
PIN CONNECTIONS



16-PIN DUAL-IN-LINE PACKAGE
(Q or P Package)

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)

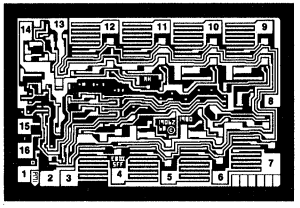
MUX-08



DIE SIZE 0.090 × 0.061 inch

1. ADDRESS BIT ZERO (A_0)
2. ENABLE
3. NEGATIVE SUPPLY V–
4. SOURCE ONE (S1)
5. SOURCE TWO (S2)
6. SOURCE THREE (S3)
7. SOURCE FOUR (S4)
8. DRAIN
9. SOURCE EIGHT (S8)
10. SOURCE SEVEN (S7)
11. SOURCE SIX (S6)
12. SOURCE FIVE (S5)
13. POSITIVE SUPPLY V+
14. GROUND (GND)
15. ADDRESS BIT TWO (A_2)
16. ADDRESS BIT ONE (A_1)

MUX-24



DIE SIZE 0.090 × 0.061 inch

1. ADDRESS BIT ZERO (A0)
2. ENABLE
3. NEGATIVE SUPPLY
4. SOURCE 1A (S1A)
5. SOURCE 2A (S2A)
6. SOURCE 3A (S3A)
7. SOURCE 4A (S4A)
8. DRAIN A
9. DRAIN B
10. SOURCE 4B (S4B)
11. SOURCE 3B (S3B)
12. SOURCE 2B (S2B)
13. SOURCE 1B (S1B)
14. POSITIVE SUPPLY
15. GROUND
16. ADDRESS BIT 1 (A1)

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at 25° C for V+ = 15V, V– = –15V and T_A = 25° C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		MUX-08/ 24-NT LIMIT	MUX-08/ 24N LIMIT	MUX-08/ 24GT LIMIT	MUX-08/ 24G LIMIT	UNITS
"ON" Resistance	R_{ON}	V_D = 0V, I_S = 200μA		300	300	400	400	Ω MAX
			T_A = 125° C	400			520	Ω MAX
Digital "1" Input Voltage	V_{INH}		2.0	2.0	2.0	2.0	V MIN	
Digital "0" Input Voltage	V_{INL}		0.8	0.8	0.8	0.8	V MAX	
Digital "0" Input Current	I_{INL}	V_{IN} = 0.4V		10	10	10	10	μA MAX
			T_A = 125° C	20		20		μA MAX
Digital "0" Enable Current	$I_{INL(EN)}$	V_{EN} = 0.4V		10	10	10	10	μA MAX
			T_A = 125° C	20		20		μA MAX
Positive Supply Current (All Digital Inputs Logic "0")	I+			12	12	12	12	mA MAX
			T_A = 125° C	15		15		mA MAX
Negative Supply Current (All Digital Inputs Logic "0")	I–			3.8	3.8	3.8	3.8	mA MAX
			T_A = 125° C	5		5		mA MAX
Analog Input Range	V_A			±10	±10	±10	±10	V MIN

TYPICAL ELECTRICAL CHARACTERISTICS at V+ = 15V, V– = –15V and T_A = 25° C for MUX-08/24N & G, T_A = 125° C for MUX-08/24NT & GT, unless otherwise noted.

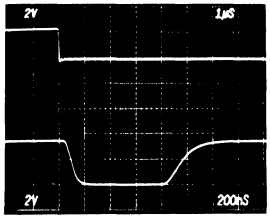
PARAMETER	SYMBOL	CONDITIONS	MUX-08N MUX-08NT TYP	MUX-24N MUX-24NT TYP	MUX-08G MUX-08GT TYP	MUX-24G MUX-24GT TYP	UNITS
Switching Time	t_{TRAN}	(Note 1)	1.3	1.3	2.1	2.1	μs
Output Settling Time	t_s	10V Step to 0.1% (Note 1)	1.5	1.5	1.9	1.9	μs
Break-Before-Make Delay	t_{DLY}	(Note 1)	0.8	0.8	1.0	1.0	μs
Crosstalk	CT	(Note 1)	70	70	70	70	dB
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \le V_D \le 10V$, I_S = 200μA	2.0	2.0	6.0	6.0	%
Leakage Current (Switch "ON")	$I_{D(ON)}$	V_D = 10V (Note 1)	1.0	0.5	1.0	0.5	nA
Analog Input Range	V_A		+11/ –15	+11/ –15	+11/ –15	+11/ –15	V

NOTES:

1. The data shown is extrapolated from measurements made on the packaged devices.
2. The ground (GND) pin must be ≥4V above the V– pin to include –4V logic levels.

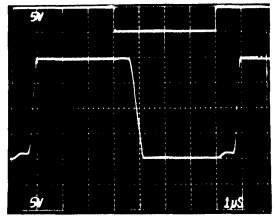
TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades unless otherwise noted.)

MUX-08 BREAK-BEFORE-MAKE SWITCHING



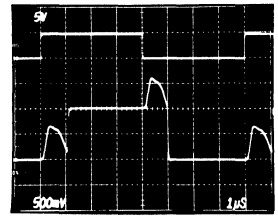
*R_L = 1kΩ, C_L = 10pF, $V_{1,8}$ = 10V
VOLTAGE = 2V/DIV
TIME = 500nS/DIV

MUX-08 LARGE SIGNAL SWITCHING



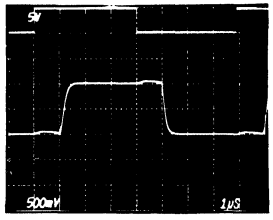
*R_L = 1MΩ, C_L = 10pF, V_1 = −10V, V_8 = +10V
VOLTAGE = 5V/DIV
TIME = 1μS/DIV

MUX-08 SMALL SIGNAL SWITCHING



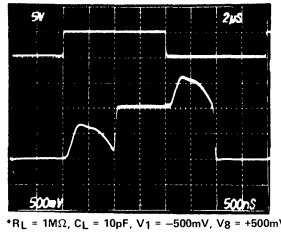
*R_L = 1MΩ, C_L = 10pF, V_1 = −500mV, V_8 = +500mV
VOLTAGE = 500mV/DIV
TIME = 1μS/DIV

MUX-08 SMALL SIGNAL SWITCHING WITH FILTERING



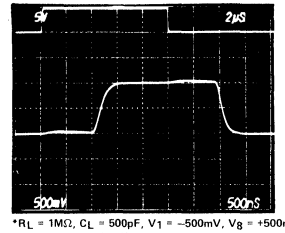
*R_L = 1MΩ, C_L = 500pF, V_1 = 500mV, V_8 = +500mV
VOLTAGE = 500mV/DIV
TIME = 1μS/DIV

MUX-08 SMALL SIGNAL SWITCHING WITH 2μs SAMPLE TIME



*R_L = 1MΩ, C_L = 10pF, V_1 = −500mV, V_8 = +500mV
VOLTAGE = 500mV/DIV
TIME = 500nS/DIV

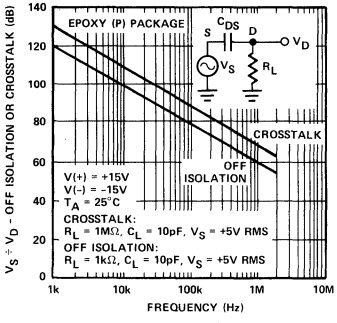
MUX-08 SMALL SIGNAL SWITCHING WITH FILTERING AND 2.5μs SAMPLE TIME



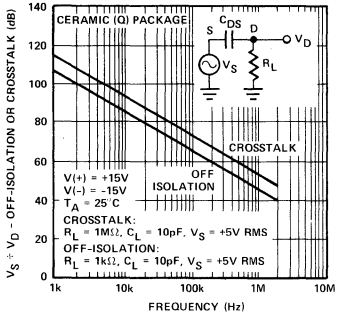
*R_L = 1MΩ, C_L = 500pF, V_1 = −500mV, V_8 = +500mV
VOLTAGE = 500mV/DIV
TIME = 500nS/DIV

*Top Waveforms: Digital Input −5V/DIV
Bottom Waveforms: Multiplexer Output

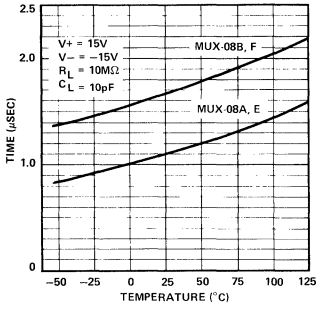
MUX-08 CROSSTALK AND OFF ISOLATION PERFORMANCE OF CHANNEL 8



MUX-08 CROSSTALK AND OFF ISOLATION PERFORMANCE OF CHANNEL 8

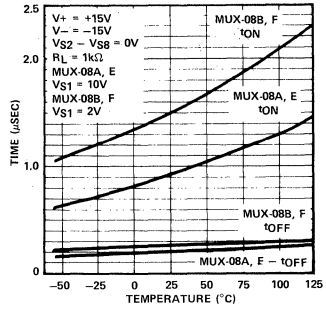


TRANSITION TIMES vs TEMPERATURE

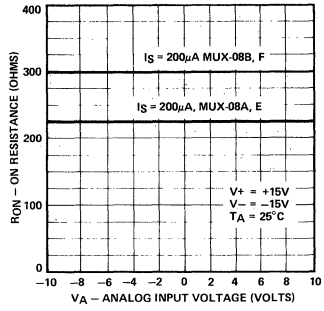


TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades unless otherwise noted.)

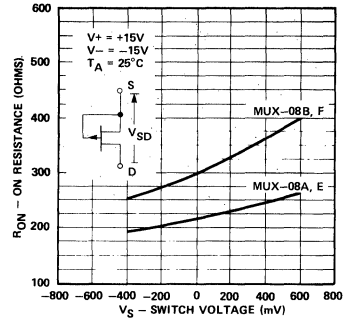
ENABLE DELAY TIMES vs TEMPERATURE



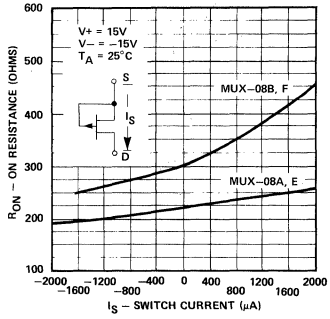
"ON" RESISTANCE (R_{ON}) vs ANALOG VOLTAGE (V_A)



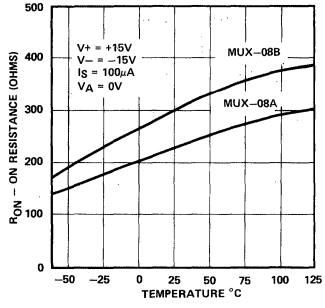
R_{ON} vs SWITCH VOLTAGE (V_{SD})



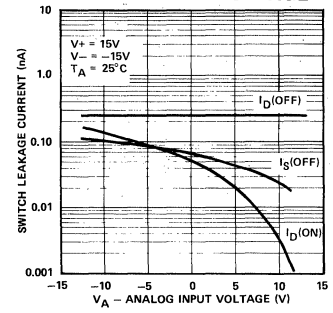
R_{ON} vs SWITCH CURRENT (I_S)



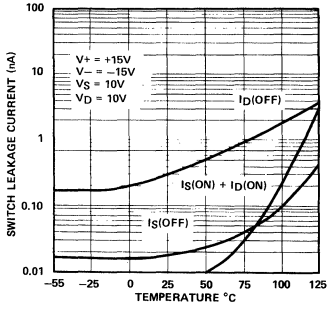
R_{ON} vs TEMPERATURE



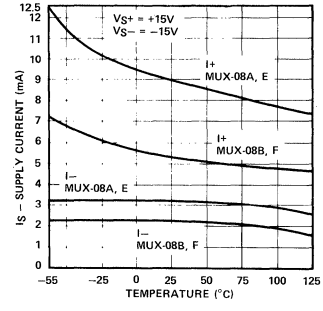
SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE



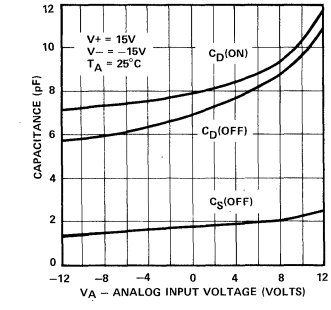
SWITCH LEAKAGE CURRENTS vs TEMPERATURE



SUPPLY CURRENTS vs TEMPERATURE

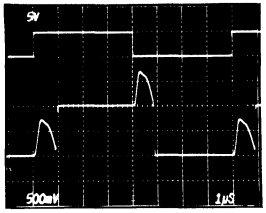


MUX-08 SWITCH CAPACITANCES vs ANALOG INPUT VOLTAGE



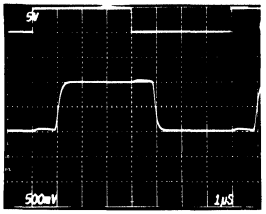
TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades unless otherwise noted.)

MUX-24 SMALL SIGNAL SWITCHING



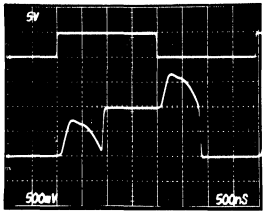
*R_L = 1MΩ, C_L = 10pF, V_1 = –500mV,
V_4 = +500mV
VOLTAGE = 500mV/DIV, TIME = 1μS/DIV

MUX-24 SMALL SIGNAL SWITCHING WITH FILTERING



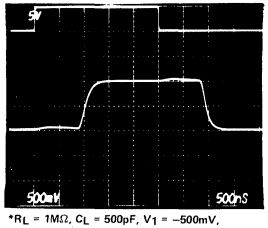
*R_L = 1MΩ, C_L = 500pF, V_1 = –500mV,
V_4 = +500mV
VOLTAGE = 500mV/DIV, TIME = 1μS/DIV

MUX-24 SMALL SIGNAL SWITCHING WITH 2μs SAMPLE TIME



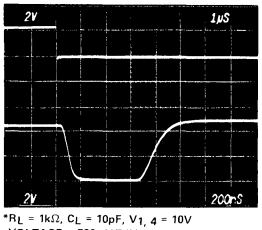
*R_L = 1MΩ, C_L = 10pF, V_1 = –500mV,
V_4 = +900mV
VOLTAGE = 500mV/DIV, TIME = 500nS/DIV

MUX-24 SMALL SIGNAL SWITCHING WITH FILTERING AND 2.5μs SAMPLE TIME



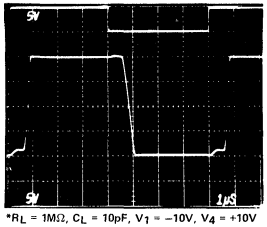
*R_L = 1MΩ, C_L = 500pF, V_1 = –500mV,
V_4 = +900mV
VOLTAGE = 500μV/DIV, TIME = 500nS/DIV

MUX-24 BREAK-BEFORE-MAKE SWITCHING



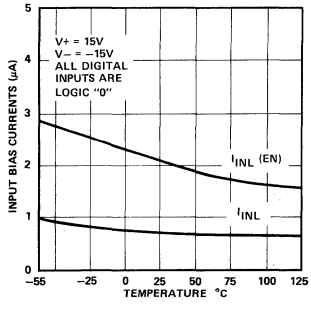
*R_L = 1kΩ, C_L = 10pF, $V_{1,4}$ = 10V
VOLTAGE = 500mV/DIV

MUX-24 LARGE SIGNAL SWITCHING

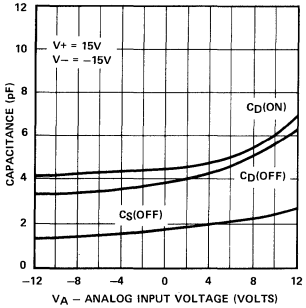


*R_L = 1MΩ, C_L = 10pF, V_1 = –10V, V_4 = +10V
VOLTAGE = 500V/DIV, TIME = 1μS/DIV

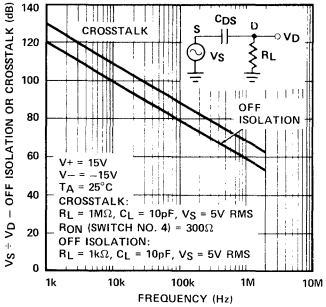
DIGITAL INPUT BIAS CURRENTS vs TEMPERATURE



MUX-24 SWITCH CAPACITANCES vs ANALOG INPUT VOLTAGE

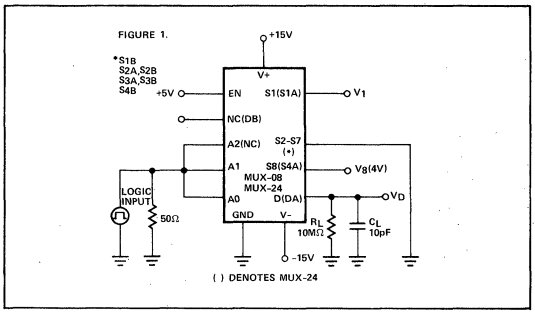


MUX-24 CROSSTALK AND OFF ISOLATION PERFORMANCE OF CHANNEL 3A

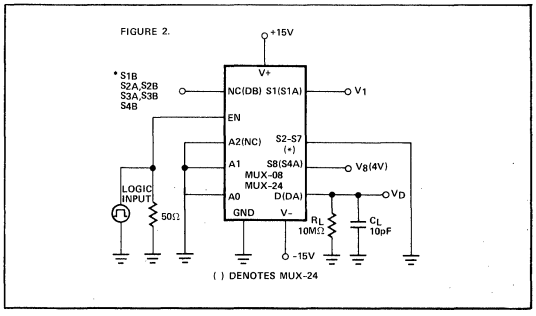


A.C. TEST CIRCUITS

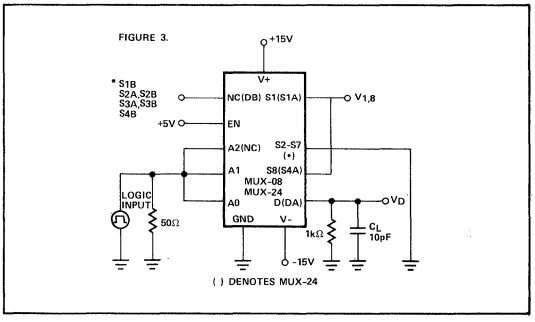
TRANSITION TIME TEST CIRCUIT



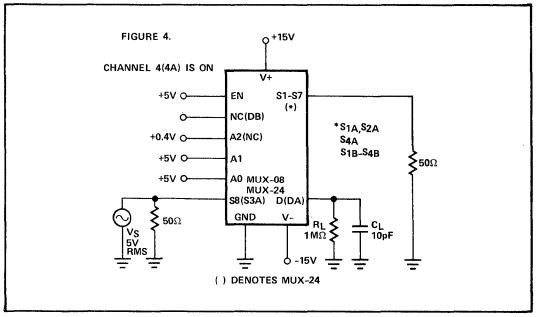
ENABLE DELAY TIME TEST CIRCUIT



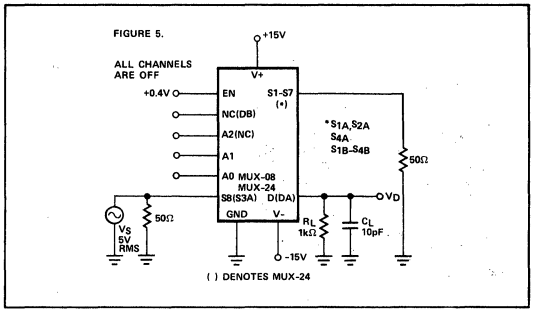
BREAK-BEFORE-MAKE TEST CIRCUIT



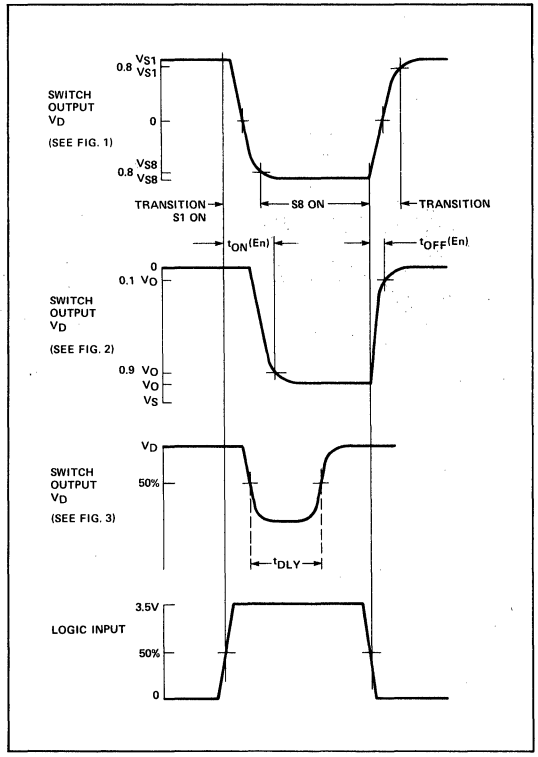
CROSSTALK MEASUREMENT CIRCUIT



OFF-ISOLATION MEASUREMENT CIRCUIT



SWITCHING TIME WAVEFORMS



APPLICATIONS INFORMATION

These analog multiplexers employ ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with BI-FET processing, **special handling as required with CMOS devices, is not necessary to prevent damage to this multiplexer.** Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pullup resistors are not

required for TTL compatibility to insure break-make switching as is most often the case with CMOS multiplexers. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above ≃ 1.4V.

The "ON" resistance, R_{ON}, of the analog switches is constant over the wide input voltage range of −15V to +11V with $V_{SUPPLY} = \pm 15V$. Higher input voltage is tolerable provided that some form of current limiting is employed (such as that of an op-amp output stage) to avoid exceeding junction temperature and power dissipation requirements. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an "OFF" switch remains greater than its V_p, and prevents that channel from being falsely turned "ON". When operating with negative input voltages, the gate-to-channel diode will be turned on if the voltage drop across an "ON" switch exceeds −0.6V. While this condition will cause an error in the output, it will not damage the switch. In lab tests, the multiplexer output has been loaded with a 0.01μF capacitor in the circuit of Figure 1. With $V_1 = -10V$ and $V_8 = +10V$, the logic input was driven at a 1kHz rate. The positive-going slew rate was 0.3V/μs which is equivalent to a normal I_{DSS} of 3mA. The negative-going slew rate was 0.7V/μs which is equivalent to a "reverse" I_{DSS} of 7mA. Note that when switch 1 is first turned "ON" it has a drop of −20V across its terminals. In spite of that fact, the current is limited to approximately twice its normal I_{DSS}.

CROSSTALK AND OFF-ISOLATION

Crosstalk and off-isolation performance is influenced by the type of package selected. Epoxy (P) packaged devices typically exhibit a 12dB improvement in off-isolation (f = 500kHz) performance when compared to ceramic (Q) packaged devices. Epoxy packaged devices typically exhibit a 15dB improvement in crosstalk (f = 500kHz) performance when compared to ceramic (Q) packaged devices.

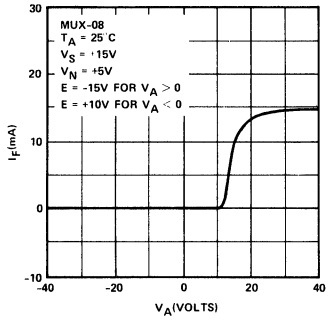
SINGLE SUPPLY OPERATION OF BIFET MULTIPLEXERS

PMI's BIFET multiplexers will operate from a single positive supply voltage with the negative supply pin at ground potential. The analog signal range will include ground.

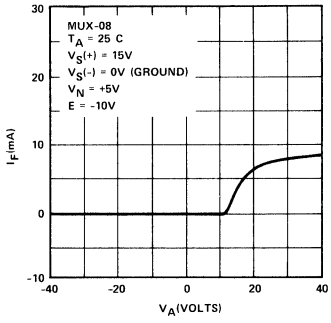
For complete information refer to application note, AN-32.

TYPICAL PERFORMANCE CHARACTERISTICS

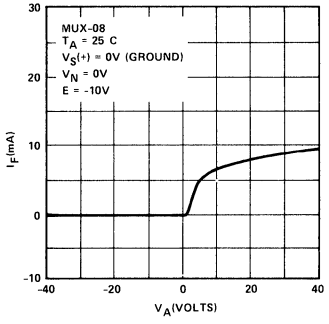
OVERVOLTAGE V-I CHARACTERISTIC



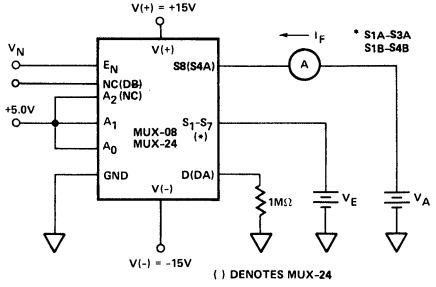
OVERVOLTAGE V-I CHARACTERISTIC



POWER-LOSS V-I CHARACTERISTIC



OVERVOLTAGE/POWER-LOSS MEASUREMENT TEST CIRCUIT



MUX-16/MUX-28

16 CHANNEL/DUAL 8 CHANNEL BI-FET ANALOG MULTIPLEXERS

OVERVOLTAGE PROTECTED

FEATURES

- **MUX-16 Pin Compatible With DG506, HI-506A, AD7506**
- **MUX-28 Compatible With DG507, HI-507A, AD7507**
- **JFET Switches Rather Than CMOS**
- **No SCR Latch-up Problems**
- **Low "ON" Resistance — 290ΩTypical**
- **Digital Inputs Compatible With TTL and CMOS**
- **Low Leakage Current**
- **Break-Before-Make Action**
- **Overvoltage Protected**
- **Supply Loss Protection**
- **125° C Temperature-Tested Die Available**
- **Highly Resistant To Static Discharge Damage**

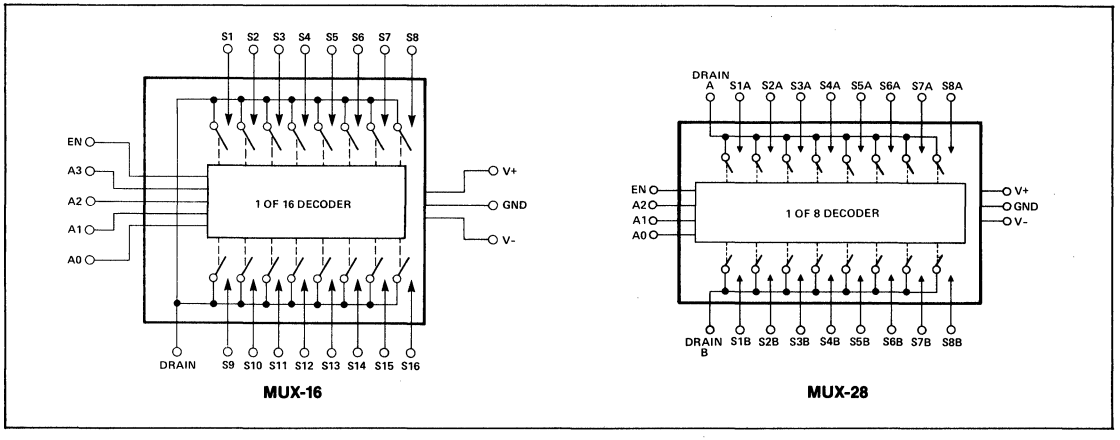
GENERAL DESCRIPTION

The MUX-16 is a monolithic 16-channel analog multiplexer which connects a single output to 1 of the 16 analog inputs depending upon the state of a 4-bit binary address. Disconnection of the output is provided by a logical "0" at the ENABLE input, thereby providing a package selection function.

The MUX-28 is a monolithic 8-channel differential analog multiplexer configured in a double pole, 8-position (plus OFF) electronic switch array. For single 8-channel and dual 4 channel models, refer to the MUX-08/MUX-24 data sheet. A 3-bit binary input address connects a pair of independent analog inputs from each 8-channel input section to the corresponding pair of independent analog outputs. Disconnection of both inputs is provided by a logical "0" at the ENABLE input, thereby offering a package select funciton.

Fabricated with Precision Monolithics' high performance BI-FET technology, these devices offer low, constant "ON" resistance. Performance advantages include low leakage currents and fast settling time with low crosstalk to satisfy a wide variety of applications. These multiplexers do not suffer from latch-up or static discharge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pull-up resistors.

FUNCTIONAL DIAGRAM



MUX-16 MUX-28

ABSOLUTE MAXIMUM RATINGS (Ratings apply to both DICE and packaged parts, unless otherwise noted.)

Operating Temperature Range,
- MUX-16/28-AT, BT ..... −55°C to +125°C
- MUX-16/28-ET, FT ..... −25°C to +85°C
- Dice Junction Temperature (T_j) ..... −65°C to +150°C

Storage Temperature Range ..... −65°C to +150°C
Power Dissipation 1000mW
Lead Soldering Temperature ..... 300°C (60 SEC)
Maximum Junction Temperature ..... 150°C
V+ Supply to V− Supply 36V
Logic Input Voltage (Note 5) ..... −4V to V+ Supply
Analog Input Voltage .... V− Supply −20V to V+ Supply +20V
Maximum Current Through Any Pin 25mA

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and $T_A = 25°C$, unless otherwise noted.

				MUX-16A/E MUX-28A/E			MUX-16B/F MUX-28B/F			
PARAMETER	**SYMBOL**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
"ON" Resistance	R_{ON}	$V_D \le 10V$, $I_D \le 200\mu A$		—	290	380	—	400	580	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \le V_D \le 10V$, $I_S = 200\mu A$		—	1.5	7.5	—	4.0	4.5	%
R_{ON} Match Between Switches	R_{ON} Match	$V_D = 0V$, $I_S = 200\mu A$		—	7	15	—	9	20	%
Analog Voltage Range	V_A	$I_S = 100\mu A$ $I_S = 100\mu A$		+10 −10	+11 −15	— —	+10 −10	+11 −15	— —	Volts
Source Current (Switch "OFF")	I_S (OFF)	$V_S = 10V$, $V_D = -10V$ (Note 1)		—	0.01	1.0	—	0.01	2.0	nA
Drain Current (Switch "OFF")	I_D (OFF)	$V_S = 10V$, $V_D = -10V$ (Note 1)	MUX-16 MUX-28	— —	0.2 0.1	1.0 1.0	— —	0.2 0.1	2.0 2.0	nA nA
Leakage Current (Switch "ON")	I_D (ON) $+I_S$ (ON)	$V_D = 10V$ (Note 1)	MUX-16 MUX-28	— —	0.2 0.1	1.0 0.5	— —	0.2 0.1	1.0 0.5	nA nA
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V		—	1.0	10	—	1.0	10	μA
Digital "0" Enable Current	I_{INL} (EN)	$V_{EN} = 0.4V$		—	4.0	10	—	4.0	10	μA
Digital Input Capacitance	C_{DIG}			—	3.0	—	—	3.0	—	pF
Switching Time	t_{TRAN}	(Note 2)		—	1.0	1.5	—	1.5	2.1	μSec
Output Settling Time	t_S	10V Step to 0.10% Accuracy 10V Step to 0.05% Accuracy 10V Step to 0.02% Accuracy		— — —	1.5 1.7 2.5	— — —	— — —	1.9 1.9 1.9	— — —	μSec
Break-Before-Make Delay	t_{DLY}			—	0.7	—	—	1.0	—	μSec
Enable Delay "ON"	$t_{ON\,(EN)}$	(Note 6)		—	1.0	2.0	—	1.2	2.5	μSec
Enable Delay "OFF"	$t_{OFF\,(EN)}$	(Note 6)		—	0.25	0.5	—	0.25	0.5	μSec
"OFF" Isolation	ISO_{OFF}	(Note 4)		—	66	—	—	66	—	dB
Crosstalk	CT	(Note 3)		—	75	—	—	75	—	dB
Source Capacitance	$C_{S\,(OFF)}$	Switch "OFF", $V_S = 0V$, $V_D = 0V$		—	2.5	—	—	2.5	—	pF
Drain Capacitance	C_D (OFF)	Switch "OFF", $V_S + 0V$, $V_D = 0V$	MUX-16 MUX-28	— —	13 8.0	— —	— —	13 8.0	— —	pF pF
Positive Supply Current (All Digital Inputs Logic "0" or "1")	I+	V+ = 15V V+ = 5V	MUX-16 MUX-28 MUX-16 MUX-28	— — — —	15 15 12 12	19 19 — —	— — — —	9.0 8.0 8.0 7.0	19 19 — —	mA mA mA mA
Negative Supply Current (All Digital Inputs Logic "0" or "1")	I−	V− = −15V V− = −5V	MUX-16 MUX-28 MUX-16 MUX-28	— — — —	5.0 5.0 4.0 4.0	7.0 7.0 — —	— — — —	3.5 3.0 3.0 2.5	7.0 7.0 — —	mA mA mA mA

NOTES:
1. Conditions applied to leakage tests insure worst case leakages. Exceeding 11V on the analog input may cause an "OFF" channel to turn "ON."
2. $R_L = 10M\Omega$, $C_L = 10pF$.
3. Crosstalk is measured by driving channel 8 (8B*) with channel 7 (7B*) ON. $R_L = 1M\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, f = 500kHz.
4. OFF isolation is measured by driving channel 8 (8B*) with ALL channels OFF. $R_L = 1k\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, F = 500kHz. C_{DS} is computed from the OFF isolation measurement.
5. The ground (GND) pin must be ≥4V above the V− pin to include −4V logic levels.
6. Sample tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$; for MUX-16AT/BT and MUX-28AT/BT and $-25°C \le T_A \le +85°C$ for MUX-16ET/FT and MUX-28ET/FT, unless otherwise noted.

			MUX-16A/E MUX-28A/E			MUX-16B/F MUX-28B/F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
"ON" Resistance	R_{ON}	$V_D \le 10$, $I_D \le 200\mu A$	—	—	500	—	—	800	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \le V_D \le 10V$, $I_S = 200\mu A$	—	2.0	—	—	5.5	—	%
R_{ON} Match Between Switches	R_{ON} Match	$V_D = 0V$, $I_S = 200\mu A$	—	10	—	—	15	—	%
Analog Voltage Range	V_A	$I_S = 200\mu A$	+10 −10	+11 −15	— —	+10 −10	+11 −15	— —	Volts
Source Current (Switch "OFF")	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Note 1)	—	—	10	—	—	10	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Note 1)	—	—	75	—	—	75	nA
Leakage Current (Switch "ON")	$I_{D(ON)}$ $+I_{S(ON)}$	$V_D = 10V$ (Note 1)	—	—	75	—	—	75	nA
Digital "1" Input Voltage	V_{INH}		2.0	—	—	2.0	—	—	Volts
Digital "0" Input Voltage	V_{INL}		—	—	0.8	—	—	0.8	Volts
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to $15.0V$	—	—	20	—	—	20	μA
Digital "0" Enable Current	I_{INL} (EN)	$V_{EN} = 0.4V$	—	—	20	—	—	20	μA
Positive Supply Current	I+	All Digital Inputs Logic "0" or "1"	—	—	24	—	—	24	mA
Negative Supply Current	I−	All Digital Inputs Logic "0" or "1"	—	—	8.2	—	—	8.2	mA

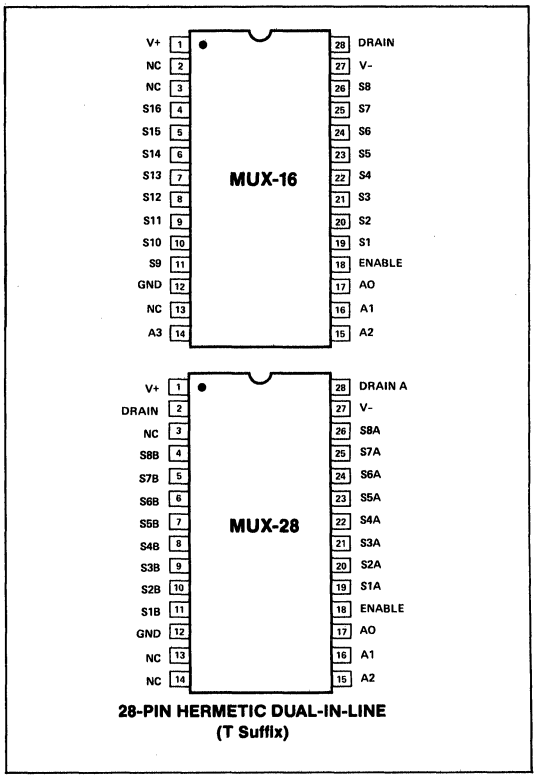
ORDERING INFORMATION†

25°C RESISTANCE	PACKAGE HERMETIC DIP	TEMPERATURE RANGE
290Ω*	MUX16AT	MIL
290Ω	MUX16ET	IND
400Ω*	MUX16BT	MIL
400Ω	MUX16FT	IND
290Ω*	MUX28AT	MIL
290Ω	MUX28ET	IND
400Ω*	MUX28BT	MIL
400Ω	MUX28FT	IND

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number.

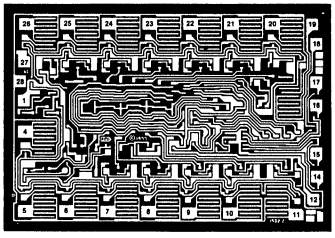
†All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



28-PIN HERMETIC DUAL-IN-LINE (T Suffix)

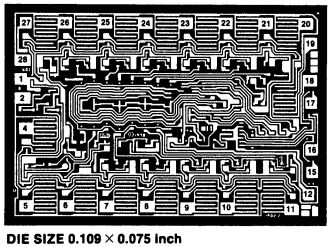
DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



MUX-16

DIE SIZE 0.109 × 0.075

1. POSITIVE SUPPLY
4. SOURCE 16 (S16)
5. SOURCE 15 (S15)
6. SOURCE 14 (S14)
7. SOURCE 13 (S13)
8. SOURCE 12 (S12)
9. SOURCE 11 (S11)
10. SOURCE 10 (S10)
11. SOURCE 9 (S9)
12. GROUND
14. ADDRESS BIT 3 (A3)
15. ADDRESS BIT 2 (A2)
16. ADDRESS BIT 1 (A1)
17. ADDRESS BIT 0 (A0)
18. ENABLE
19. SOURCE 1 (S1)
20. SOURCE 2 (S2)
21. SOURCE 3 (S3)
22. SOURCE 4 (S4)
23. SOURCE 5 (S5)
24. SOURCE 6 (S6)
25. SOURCE 7 (S7)
26. SOURCE 8 (S8)
27. NEGATIVE SUPPLY
28. DRAIN



MUX-28

DIE SIZE 0.109 × 0.075 inch

1. POSITIVE SUPPLY
2. DRAIN B
4. SOURCE 8 (S8B)
5. SOURCE 7 (S7B)
6. SOURCE 6 (S6B)
7. SOURCE 5 (S5B)
8. SOURCE 4 (S4B)
9. SOURCE 3 (S3B)
10. SOURCE 2 (S2B)
11. SOURCE 1 (S1B)
12. GROUND
15. ADDRESS BIT 2 (A2)
16. ADDRESS BIT 1 (A1)
17. ADDRESS BIT 0 (A0)
18. ENABLE
19. SOURCE 1 (S1A)
20. SOURCE 2 (S2A)
21. SOURCE 3 (S3A)
22. SOURCE 4 (S4A)
23. SOURCE 5 (S5A)
24. SOURCE 6 (S6A)
25. SOURCE 7 (S7A)
26. SOURCE 8 (S8A)
27. NEGATIVE SUPPLY
28. DRAIN A

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at 25° C for V+ = 15V, V− = −15V and T_A = 25° C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		MUX-16/ 28NT LIMIT	MUX-16/ 28N LIMIT	MUX-16/ 28GT LIMIT	MUX-16/ 28G LIMIT	UNITS
"ON" Resistance	R_{ON}	V_D = 0V	T_A = 25° C	380	380	580	580	Ω MAX
		I_S = 100μA	T_A = 125° C	540		800		Ω MAX
Digital "1" Input Voltage	V_{INH}			2.0	2.0	2.0	2.0	V MIN
Digital "0" Input Voltage	V_{INL}			0.8	0.8	0.8	0.8	V MAX
Digital "0" Input Current	I_{INL}	V_{IN} = 0.4V		10	10	10	10	μA MAX
Digital "0" Enable Current	$I_{INL(EN)}$	V_{EN} = 0.4V		10	10	10	10	μA MAX
Positive Supply Current (All Digital Inputs Logic "0")	I+			19	19	19	19	mA MAX
Negative Supply Current (All Digital Inputs Logic "0")	I−			7	7	7	7	mA MAX
Analog Input Range	V_A			±10	±10	±10	±10	V MIN

TYPICAL ELECTRICAL CHARACTERISTICS for V+ = 15V, V− = −15V and T_A = 25° C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-16/ 28NT TYP	MUX-16/ 28N TYP	MUX-16/ 28GT TYP	MUX-16/ 28G TYP	UNITS
Switching Time	t_{TRAN}	(Note 2)	1.5	1.5	2.1	2.1	μs
Output Settling Time	t_S	10V Step to 0.1% (Note 2)	1.5	1.5	1.9	1.9	μs
Break-Before-Make Delay	t_{DLY}	(Note 2)	0.8	0.8	1.0	1.0	μs
Crosstalk	CT	(Note 2)	70	70	70	70	dB
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \le V_D \le 10V$, I_S = 200μA	2.0	2.0	6.0	6.0	%
Leakage Current (Switch "ON")	$I_{D(ON)}$	V_D = 10V (Note 2)	1.0	1.0	1.0	1.0	nA
Analog Input Range	V_A		+11/ −15	+11/ −15	+11/ −15	+11/ −15	V

NOTES:

1. For MUX-16/28NT and MUX-16/28GT electrical characteristics apply at 25° C and 125° C, unless otherwise noted.
2. The data shown is extrapolated from measurements made on the packaged devices.

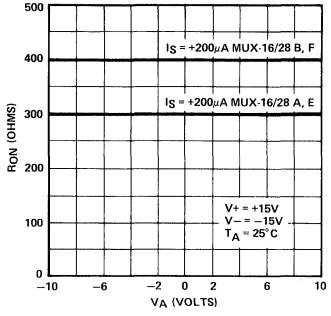
TRUTH TABLE

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

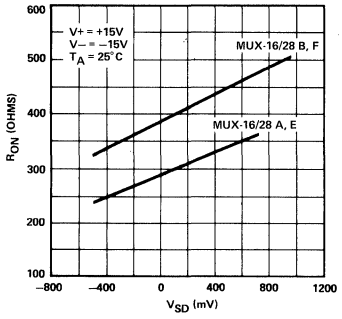
A_3	A_2	A_1	A_0	EN	"ON" CHANNEL	A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE	H	L	L	L	H	9
L	L	L	L	H	1	H	L	L	H	H	10
L	L	L	H	H	2	H	L	H	L	H	11
L	L	H	L	H	3	H	L	H	H	H	12
L	L	H	H	H	4	H	H	L	L	H	13
L	H	L	L	H	5	H	H	L	H	H	14
L	H	L	H	H	6	H	H	H	L	H	15
L	H	H	L	H	7	H	H	H	H	H	16
L	H	H	H	H	8						

STATIC CHARACTERISTIC CURVES (apply to all grades unless otherwise noted.)

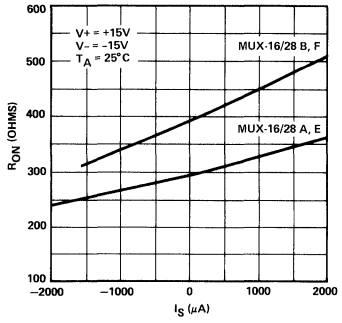
"ON" RESISTANCE (R_{ON}) vs ANALOG VOLTAGE (V_A)



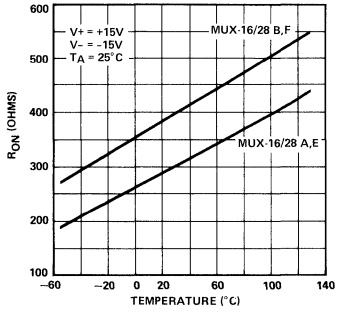
R_{ON} vs SWITCH VOLTAGE (V_{SD})



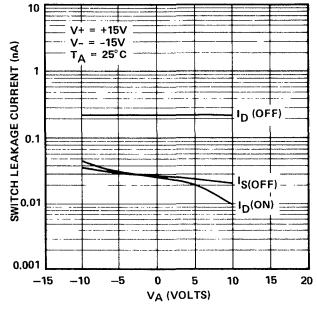
R_{ON} vs SWITCH CURRENT (I_S)



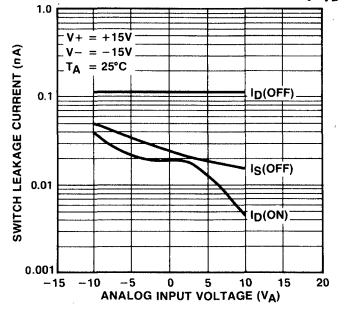
R_{ON} vs TEMPERATURE (T)



MUX-16 SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE (V_A)

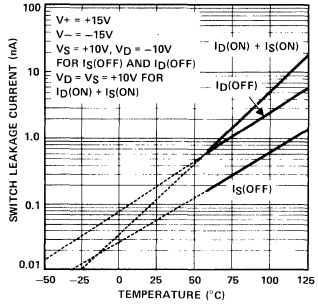


MUX-28 SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE (V_A)

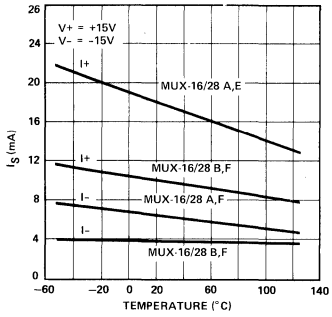


STATIC CHARACTERISTIC CURVES (apply to all grades unless otherwise noted)

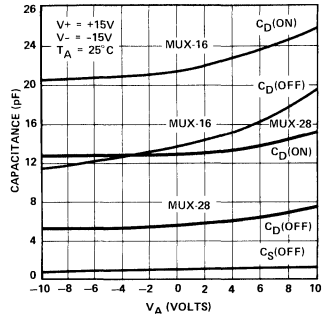
SWITCH LEAKAGE CURRENTS vs TEMPERATURE



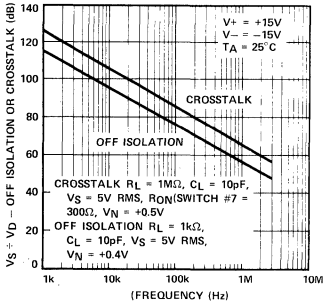
SUPPLY CURRENTS vs TEMPERATURE (T)



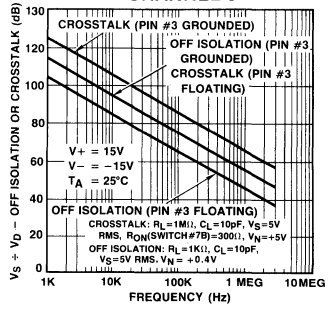
SWITCH CAPACITANCES vs ANALOG INPUT VOLTAGE (V_A)



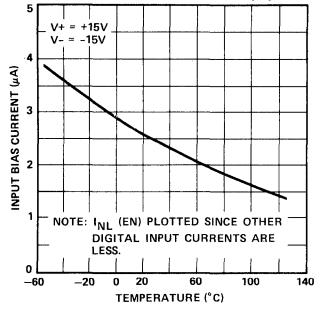
MUX-16 OFF PERFORMANCE OF CHANNEL 8



MUX-28 OFF PERFORMANCE OF CHANNEL 8

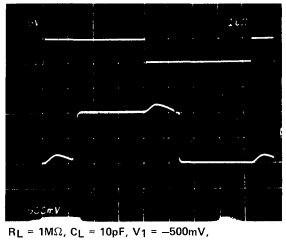


DIGITAL INPUT BIAS CURRENTS vs TEMPERATURE (T)



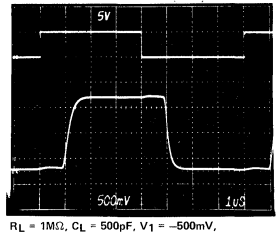
DYNAMIC CHARACTERISTIC CURVES (MUX-16)

SMALL SIGNAL SWITCHING



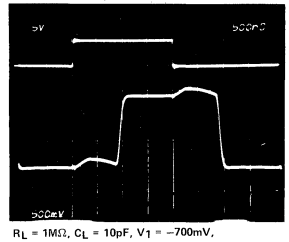
R_L = 1MΩ, C_L = 10pF, V_1 = –500mV,
V_{16} = +500mV

SMALL SIGNAL SWITCHING WITH FILTERING



R_L = 1MΩ, C_L = 500pF, V_1 = –500mV,
V_{16} = +500mV

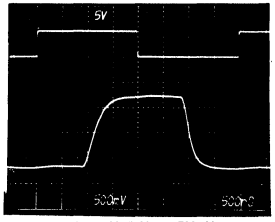
SMALL SIGNAL SWITCHING WITH 2µS SAMPLE TIME



R_L = 1MΩ, C_L = 10pF, V_1 = –700mV,
V_{16} = +700mV

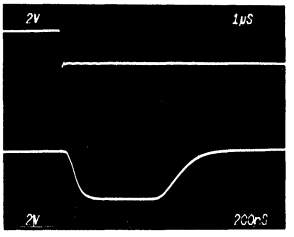
DYNAMIC CHARACTERISTIC CURVES (MUX-16)

SMALL SIGNAL SWITCHING WITH FILTERING AND 2.0μS SAMPLE TIME



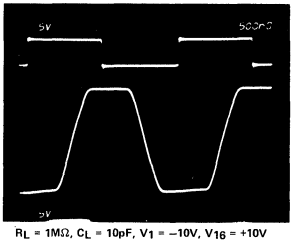
R_L = 1MΩ, C_L = 500pF, V_1 = −700mV, V_{16} = +700mV

BREAK-BEFORE-MAKE SWITCHING



R_L = 1kΩ, C_L = 10pF, $V_{1,\ 16}$ = 10V

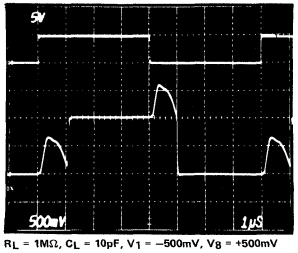
LARGE SIGNAL SWITCHING



R_L = 1MΩ, C_L = 10pF, V_1 = −10V, V_{16} = +10V

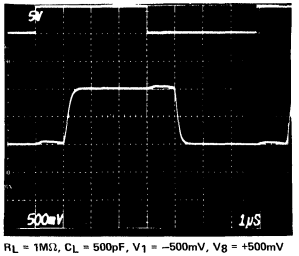
DYNAMIC CHARACTERISTIC CURVES (MUX-28)

SMALL SIGNAL SWITCHING



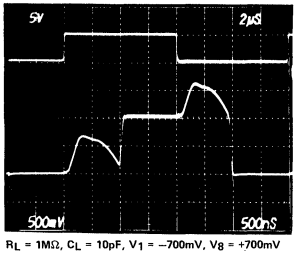
R_L = 1MΩ, C_L = 10pF, V_1 = −500mV, V_8 = +500mV

SMALL SIGNAL SWITCHING WITH FILTERING



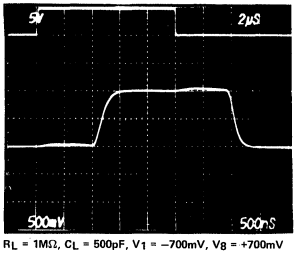
R_L = 1MΩ, C_L = 500pF, V_1 = −500mV, V_8 = +500mV

SMALL SIGNAL SWITCHING WITH 2μS SAMPLE TIME



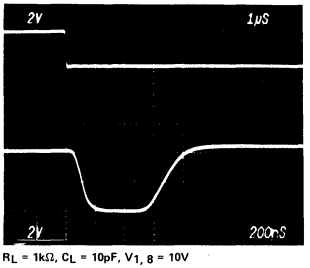
R_L = 1MΩ, C_L = 10pF, V_1 = −700mV, V_8 = +700mV

SMALL SIGNAL SWITCHING WITH FILTERING AND 2.5μS SAMPLE TIME



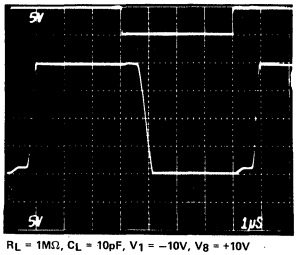
R_L = 1MΩ, C_L = 500pF, V_1 = −700mV, V_8 = +700mV

BREAK-BEFORE-MAKE SWITCHING



R_L = 1kΩ, C_L = 10pF, $V_{1,\ 8}$ = 10V

LARGE SIGNAL SWITCHING

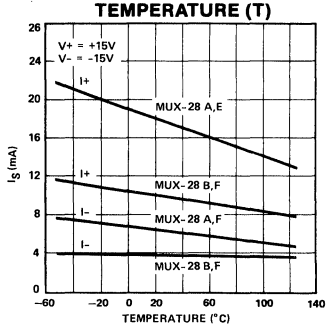


R_L = 1MΩ, C_L = 10pF, V_1 = −10V, V_8 = +10V

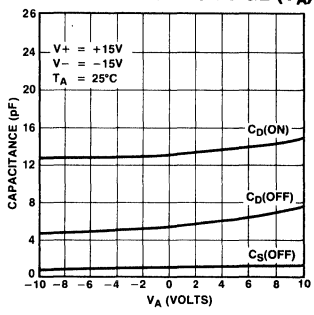
*Top Waveforms: Digital Input −5V/DIV
Bottom Waveforms: Multiplexer Output

DYNAMIC CHARACTERISTIC CURVES (MUX-28) (apply to all grades unless otherwise noted)

SUPPLY CURRENTS vs TEMPERATURE (T)

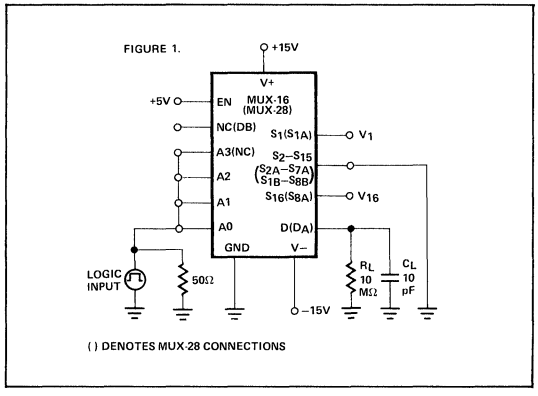


SWITCH CAPACITANCES vs ANALOG INPUT VOLTAGE (V_A)

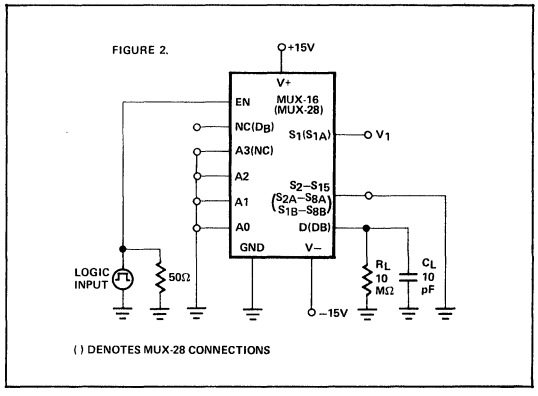


A.C. TEST CIRCUITS

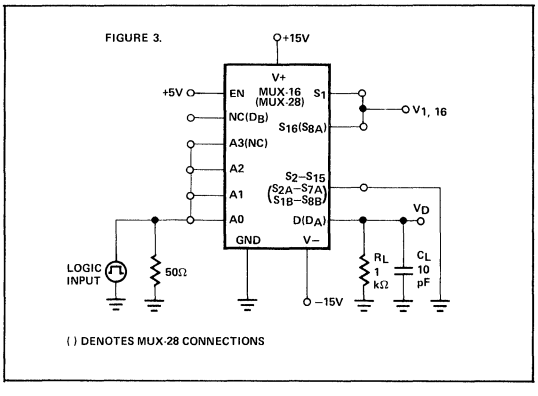
TRANSITION TIME TEST CIRCUIT



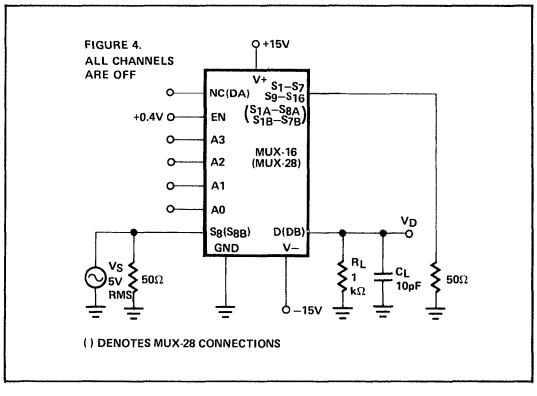
ENABLE DELAY TIME TEST CIRCUIT



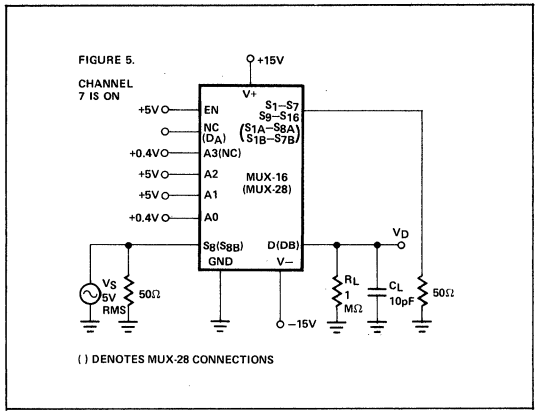
BREAK-BEFORE-MAKE TEST CIRCUIT



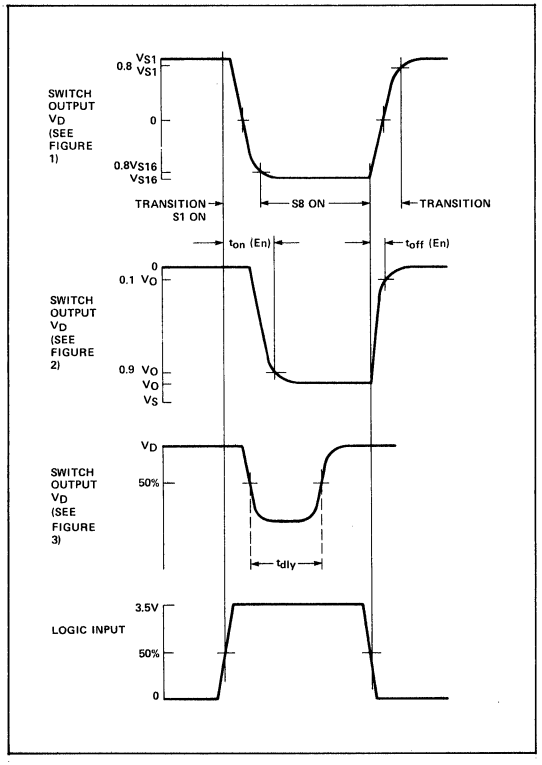
OFF ISOLATION TEST CIRCUIT



CROSSTALK MEASUREMENT CIRCUIT



SWITCHING TIME WAVEFORMS

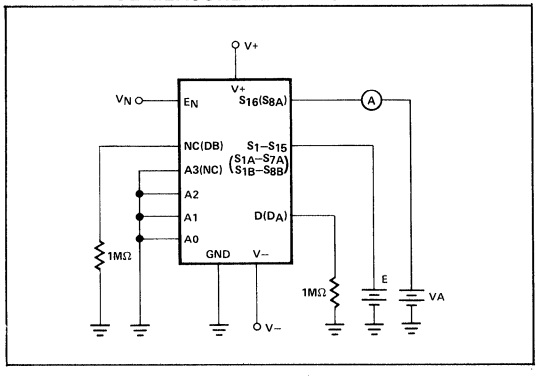


APPLICATIONS INFORMATION

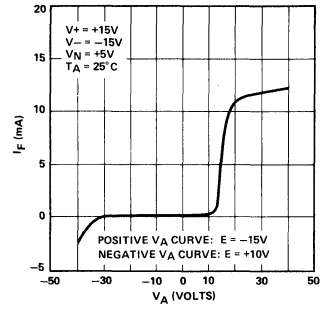
These analog multiplexers employ ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with BI-FET processing rather than CMOS, special handling is not necessary to prevent damage to this multiplexer. Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pullup resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS multiplexers. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised about ≈ 1.4V.

The "ON" resistance, R_{ON} of the analog switches is constant over the wide input voltage range of −15V to +11V with $V_{SUPPLY} = \pm 15V$. The overvoltage and supply-loss V-I characteristics shown above indicate typical performance when the multiplexer is subjected to abnormal signals. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF switch remains greater than its V_P, and prevents that channel from being falsely turned ON. When operating with negative input voltages, the gate-to-channel diode will be turned on if the voltage drop acrross an ON switch exceeds −0.6V. While this condition will cause an error in the output, it will not damage the switch. In lab tests, the multiplexer output has been loaded with a 0.01μF capacitor in the circuit of Figure 1. With $V_1 = -10V$ and $V_{16} = +10V$, the logic input was driven as a 1kHz rate. The positive-going slew rate was 0.3V/μSec which is equivalent to a normal I_{DSS} of 3mA. The negative-going slew rate was 0.7V/μSec which is equivalent to a "reverse" I_{DSS} of 7mA. Note that when switch one (1) if first turned ON it has a drop of −20V across its terminals. In spite of that fact, the current is limited to approximately twice its normal I_{DSS}.

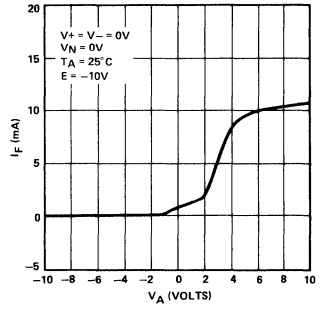
OVERVOLTAGE MEASUREMENT TEST CIRCUIT



OVERVOLTAGE V-I CHARACTERISTIC



SUPPLY-LOSS V-I CHARACTERISTIC



SW-01/02, SW-03/04

QUAD SPST BIFET ANALOG SWITCHES WITH TEMPERATURE COMPENSATED R_{ON} AND DISABLE FUNCTION

FEATURES

- **Low R_{ON} vs Temperature ..... 0.03%/°C**
- **Low Absolute R_{ON} 85Ω**
- **Low R_{ON} Variation vs Analog Signal 4%**
- **High Speed 300nS**
- **Low Leakage Current 0.2nA**
- **Over Voltage and Supply Loss Protected**
- **SW-01 is Improved Pin Compatible Device for DG201, ADG201, LF11201**
- **SW-02 is Improved Pin Compatible Device for LF11202, IH202**
- **SW-03 — Normally Closed, WithDisable. Functional Equivalent to LF11332.**
- **SW-04 — Normally Open, With Disable. Functional Equivalent to LF11331.**

GENERAL DESCRIPTION

The SW-01 through SW-04 are four-channel single-pole, single-throw analog switches which offer operating characteristics unavailable in other JFET or CMOS devices. A unique circuit design provides a nearly constant R_{ON} over the full operating temperature span. R_{ON} drift typically runs under 300ppm/°C.

The SW-01/02 are pin compatible with the DG201/202, while the SW-03/04 incorporate a chip disable pin which allows switch ganging for multiple switch systems. An Ion Implanted FET switch inherently exhibits low R_{ON} variations vs analog input signals. The junction FET construction also eliminates static discharge destruction prevalent in CMOS devices.

Low R_{ON} sensitivity to temperature and voltage is complemented by guaranteed high-speed operation and low-leakage currents. Address inputs may operate directly from either CMOS or TTL logic levels and are supply voltage independent. The SW-01 through SW-04 are protected during supply voltage power loss and against input signal overvoltages.

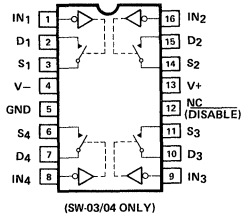
ORDERING INFORMATION†

	16 PIN HERMETIC DUAL INLINE PACKAGE	
FUNCTION	**MILITARY***	**INDUSTRIAL**
N.C.	SW01BQ	SW01FQ
N.C. (Disable)	SW03BQ	SW03FQ
N.O.	SW02BQ	SW02FQ
N.O. (Disable)	SW04BQ	SW04FQ

* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



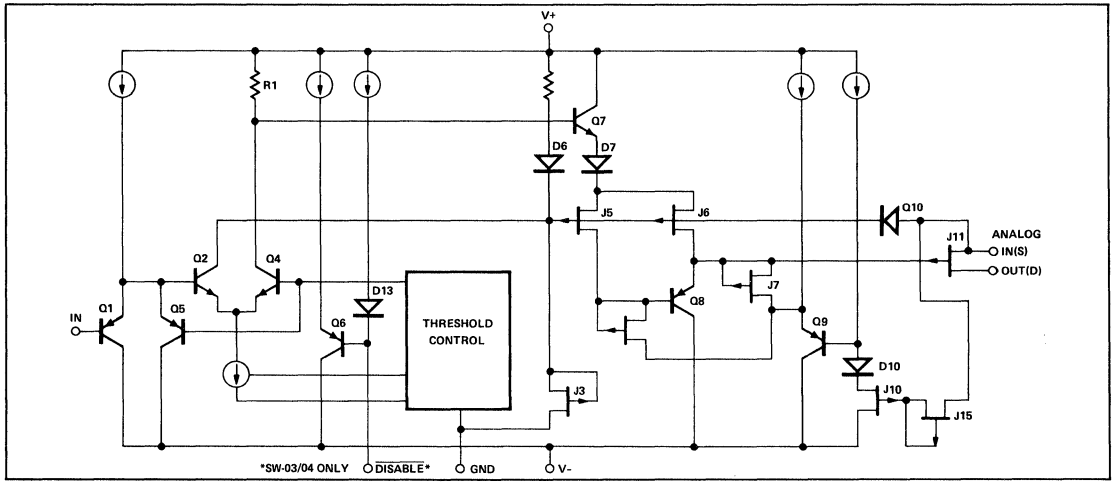
(SW-03/04 ONLY)

CONTROL LOGIC

LOGIC		SWITCH STATE			
		SW	SW	SW	SW
Dy	INy	01	02	03	04
0	X	NA	NA	OFF	OFF
1	0	ON	OFF	ON	OFF
1	1	OFF	ON	OFF	ON

NOTES: Dy = DISABLE 1-4
INy = INPUT 1-4
X = DON'T CARE
NA = NOT APPLICABLE

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-01-04B MIN	SW-01-04B TYP	SW-01-04B MAX	SW-01-04F MIN	SW-01-04F TYP	SW-01-04F MAX	UNITS
"ON" Resistance	R_{ON}	$-10V \le V_A \le 10V$, $I_D \le 1mA$	—	85	100	—	85	120	Ω
R_{ON} Match		Note 1	—	4	10	—	4	10	%
Analog Voltage Range	V_A	$R_L \ge 2k\Omega$ Full Temperature Range	+10 −10	+11 −15	— —	+10 −10	+11 −15	— —	V
ΔR_{ON} vs V_A		$V_A \le 10V$, $I_D \le 1mA$	—	7	10	—	7	10	%
Analog Current Range	I_A	$V_A \le 10V$	—	5	—	—	5	—	mA
Source Current in "OFF" Condition	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$	—	0.2	1.0	—	0.2	2.0	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$	—	0.2	1.0	—	0.2	2.0	nA
Leakage Current in "ON" Condition	$I_{D(ON)} + I_{S(ON)}$	$V_S = \pm 10V$, Note 2	—	—	1.0	—	—	1.0	nA
"OFF" Isolation	$I_{SO(OFF)}$	Test Figure 2	—	58	—	—	58	—	dB
Crosstalk	C_T	Test Figure 3	—	70	—	—	70	—	dB
Turn-On-Time	T_{ON}	Test Figure 1; Note 3	—	300	400	—	300	400	ns
Turn-Off-Time	T_{OFF}	Test Figure 1; Note 3	—	200	300	—	200	300	ns
Break-Before-Make Time		Test Figure 1; Notes 3, 7	—	100	—	—	100	—	ns
Source Capacitance	$C_{S(OFF)}$	$V_A \le 10V$	—	7.0	—	—	7.0	—	pF
Drain Capacitance	$C_{D(OFF)}$	$V_A \le 10V$	—	5.5	—	—	5.5	—	pF
Logical "1" Input Voltage	V_{INH}	Full Temperature Range	2.0	—	—	2.0	—	—	V
Logical "0" Input Voltage	V_{INL}	Full Temperature Range	—	—	0.8	—	—	0.8	V
Logical "1" Input Current	I_{INH}	$2.0 \le V_{IN} \le 15.0V$, Note 3	—	1.0	3.0	—	1.0	3.0	mA
Logical "0" Input Current	I_{INL}	$0 \le V_{IN} \le 0.8V$	—	1.0	3.0	—	1.0	3.0	μA
Positive Supply Current	I+	Note 5	—	6.3	8.0	—	6.3	9.0	mA
Negative Supply Current	I−	Note 5	—	3.2	4.5	—	3.2	5.5	mA
Ground Current	I_G	Note 5	—	3.0	4.0	—	3.0	4.5	mA

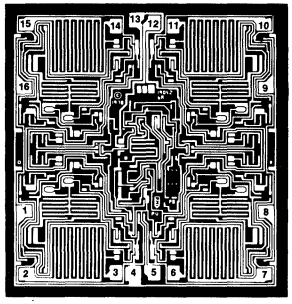
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and $-55°C \le T_A \le +125°C$ for SW-01-04B and $-25°C \le T_A \le +85°C$ for SW-01-04F.

PARAMETER	SYMBOL	CONDITIONS	SW-01-04B MIN	SW-01-04B TYP	SW-01-04B MAX	SW-01-04F MIN	SW-01-04F TYP	SW-01-04F MAX	UNITS
"ON" Resistance	R_{ON}	$-10V \le V_A \le 10V$, $I_D \le 1mA$	—	—	120	—	—	140	Ω
R_{ON} Match		Note 1	—	10	15	—	10	15	%
R_{ON} Temperature Coefficient — Average	TC_R	$V_A = 0V$, $I_D = 100\mu A$; Notes 3, 6	—	0.03	0.20	—	0.03	0.15	%/°C
Source Current in "OFF" Condition	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$; Note 4	—	—	10	—	—	10	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$; Note 4	—	—	10	—	—	10	nA
Leakage Current in "ON" Condition	$I_{D(ON)} + I_{S(ON)}$	$V_S = \pm 10V$; Note 2, 4	—	—	10	—	—	10	nA
Turn-On-Time	T_{ON}	Test Figure 1; Note 3	—	500	600	—	500	600	ns
Turn-Off-Time	T_{OFF}	Test Figure 1; Note 3	—	400	500	—	400	500	ns
Break-Before-Make Time		Test Figure 1; Notes 3, 7	—	100	—	—	100	—	ns
Logical "1" Input Current	I_{INH}	$2.0 \le V_{IN} \le 15.0V$; Note 3	—	1.0	5	—	1.0	5	mA
Logical "0" Input Current	I_{INL}	$0 \le V_{IN} \le 0.8V$	—	—	5.0	—	—	5.0	μA
Positive Supply Current	I+	Note 5	—	—	11	—	—	12.0	mA
Negative Supply Current	I−	Note 5	—	—	6.0	—	—	7.0	mA
Ground Current	I_G	Note 5	—	—	5.0	—	—	6.0	mA

NOTES:

1. $V_A = 0V$. $I_D = 100\mu A$. Specified as a percentage of $R_{AVERAGE}$ where:
$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3} + R_{ON4}}{4}$$
2. The conditions listed specify the worst case leakage current. The leakage currents apply equally to source or drain.
3. Guaranteed by design.
4. Parameter tested at $T_A = 125°C$ for military temperature range device.
5. Power supply and ground currents specified for switch "ON" or "OFF" The "OFF" state gives highest power consumption.
6. $TC_R = \frac{R_{ON}@T_1 - R_{ON}@25°C}{R_{ON}@25°C\ [T_1 - 25]} \times 100$
7. Switching is guaranteed to be break-before-make.

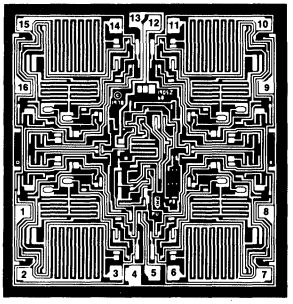
DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



SW01/03

DIE SIZE 0.100 × 0.096 inch

1. SWITCH (1) ADDRESS (IN1)
2. SWITCH (1) DRAIN (D1)
3. SWITCH (1) SOURCE (S1)
4. NEGATIVE SUPPLY
5. GROUND
6. SWITCH (4) SOURCE (S4)
7. SWITCH (4) DRAIN (D4)
8. SWITCH (4) ADDRESS (IN4)
9. SWITCH (3) ADDRESS (IN3)
10. SWITCH (3) DRAIN (D3)
11. SWITCH (3) SOURCE (S3)
12. DISABLE (NO CONNECTION SW01)
13. POSITIVE SUPPLY
14. SWITCH (2) SOURCE (S2)
15. SWITCH (2) DRAIN (D2)
16. SWITCH (2) ADDRESS (IN2)



SW02/04

DIE SIZE 0.100 × 0.096 inch

1. SWITCH (1) ADDRESS (IN1)
2. SWITCH (1) DRAIN (D1)
3. SWITCH (1) SOURCE (S1)
4. NEGATIVE SUPPLY
5. GROUND
6. SWITCH (4) SOURCE (S4)
7. SWITCH (4) DRAIN (D4)
8. SWITCH (4) ADDRESS (IN4)
9. SWITCH (3) ADDRESS (IN3)
10. SWITCH (3) DRAIN (D3)
11. SWITCH (3) SOURCE (S3)
12. DISABLE (NO CONNECTION SW02)
13. POSITIVE SUPPLY
14. SWITCH (2) SOURCE (S2)
15. SWITCH (2) DRAIN (D2)
16. SWITCH (2) ADDRESS (IN2)

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-01-04N LIMIT	SW-01-04G LIMIT	UNITS
"ON" Resistance	R_{ON}	$-10V \le V_A \le 10V$, $I_D \le 1mA$	100	120	Ω MAX
R_{ON} Match		$V_A = 0V$, $I_D \le 100\mu A$	10	10	% MAX
ΔR_{ON} vs V_A		$V_A \le 10V$, $I_D \le 1mA$	10	10	% MAX
Positive Supply Current	I+	Note 1	8.0	9.0	mA MAX
Negative Supply Current	I–	Note 1	4.5	5.5	mA MAX
Ground Current	I_G		4.0	4.5	mA MAX
Analog Voltage Range	V_A	$R_L \ge 2k\Omega$	±10	±10	V MIN
Logical "1" Input Voltage	V_{INH}		2.0	2.0	V MIN
Logical "0" Input Voltage	V_{INL}		0.8	0.8	V MAX
Logical "0" Input Current	I_{INL}	$0 \le V_{IN} \le 0.8V$	3.0	3.0	μA MAX
Logical "1" Input Current	I_{INH}	$2.0 \le V_{IN} \le 15V$	1.0	1.0	μA MAX

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-01-04N TYPICAL	SW-01-04G TYPICAL	UNITS
"ON" Resistance	R_{ON}	$-55°C \le T_A \le 125°C$	90	90	Ω
R_{ON} Temperature Coefficient	TC_R	$V_A = 0$, $I_D = 100\mu A$	0.03	0.03	%/° C
Turn-On-Time	T_{ON}	$R_L = 1k$, $C_L = 13pF$	300	300	nS
Turn-Off-Time	T_{OFF}	$R_L = 1k$, $C_L = 13pF$	200	200	nS
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$	0.2	0.2	nA
"OFF" Isolation	$I_{SO(OFF)}$	$f = 500kHz$, $R_L = 680\Omega$	58	58	dB
Crosstalk	C_T	$f = 500kHz$, $R_L = 680\Omega$	70	70	dB

NOTE:
1. Power Supply and ground current specified for switch "ON" or "OFF".

ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise stated).

Operating Temperature Range
- SW-01-04BQ ..... −55°C to +125°C
- SW-01-04FQ ..... −25°C to +85°C

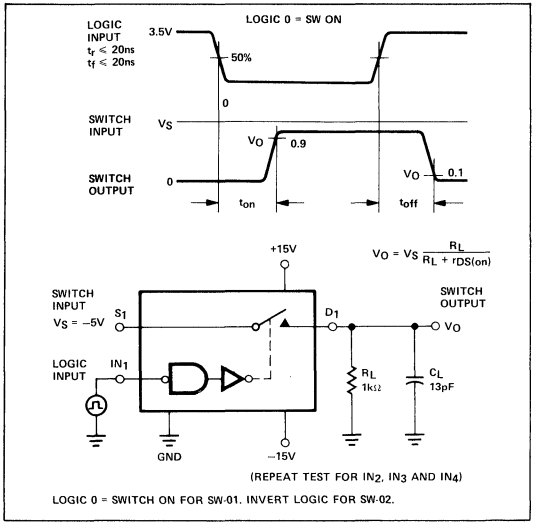
DICE Junction Temperature (T_j) ..... −65°C to +150°C
Storage Temperature Range ..... −65°C to +150°C
Power Dissipation (Q Package) 900mW
Lead Soldering Temperature ..... 300°C (60 sec)
Maximum Junction Temperature ..... 150°C
V+ Supply to V− Supply 36V
V+ Supply to Ground 36V
Logic Input Voltage ..... −4V to V+ Supply
Analog Input Voltage
- Continuous .... V − Supply − 25V to V + Supply + 25V
- For V+ = V− = 0 ..... ±15V

Maximum Current Through Any Pin 30mA
Peak Current,
- (Pulsed at 1ms, 10% Duty Cycle) 70mA

NOTE: Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

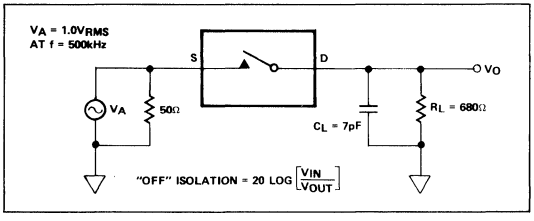
TEST CIRCUITS

TEST FIGURE 1

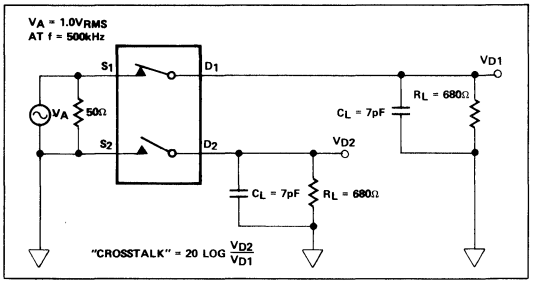


LOGIC 0 = SWITCH ON FOR SW-01. INVERT LOGIC FOR SW-02.

TEST FIGURE 2



TEST FIGURE 3



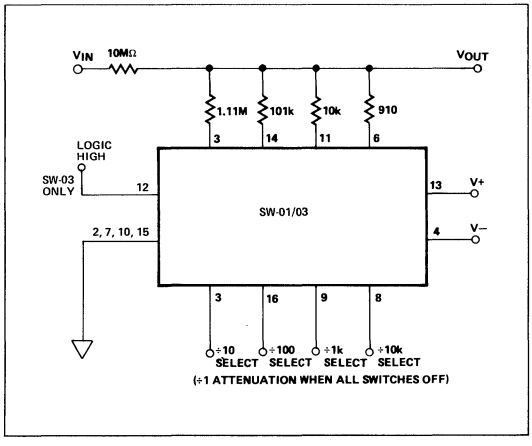
APPLICATIONS INFORMATION

This analog switch employs ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with BI-FET processing rather than CMOS, special handling is not necessary to prevent damage to these switches. Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pullup resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS switches. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above ≈1.4V.

The "ON" resistance, R_{ON}, of the analog switches is constant over the wide input voltage range of −15V to +11V with $V_{SUPPLY} = \pm 15V$. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF switch remains greater than its V_p, and prevents that channel from being falsely turned ON. Individual switches are "ON" without power applied.

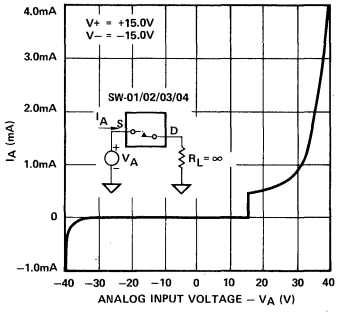
Proper switching requires the "Source" terminal to be connected to the input driving signal. If the DISABLE pin switches are controlled by the logic select pins.

PROGRAMMABLE ATTENUATOR (1 to 0.0001)

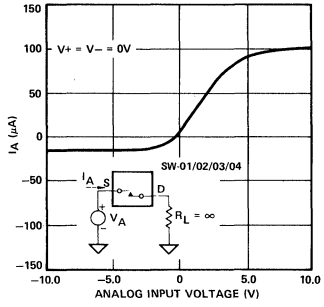


TYPICAL PERFORMANCE CHARACTERISTICS (SW-01/02/03/04)

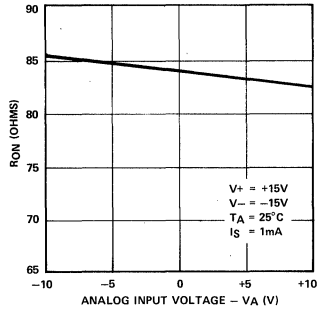
OVERVOLTAGE CHARACTERISTIC



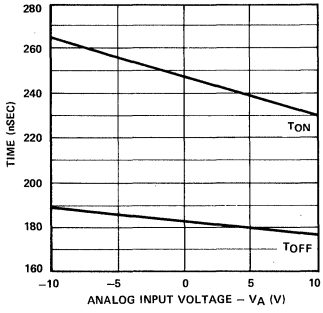
POWER SUPPLY LOSS CHARACTERISTIC



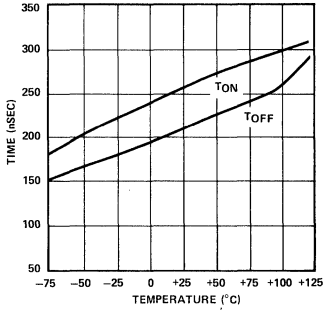
"ON" RESISTANCE vs. ANALOG VOLTAGE (V_A)



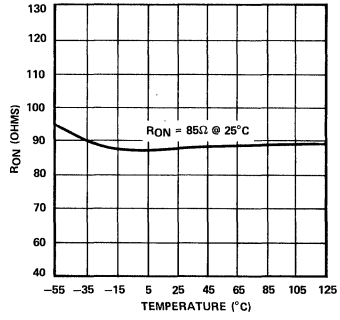
SWITCHING TIMES vs. ANALOG VOLTAGE



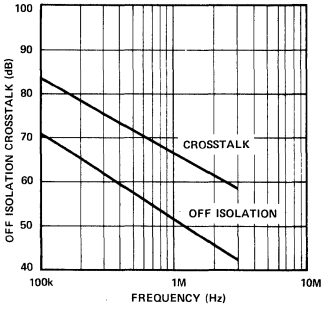
SWITCHING TIMES vs. TEMPERATURE



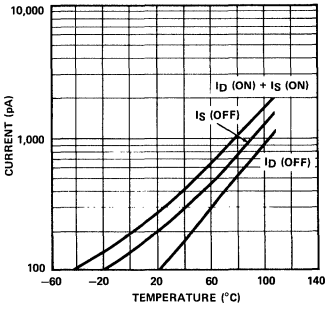
R_{ON} vs. TEMPERATURE



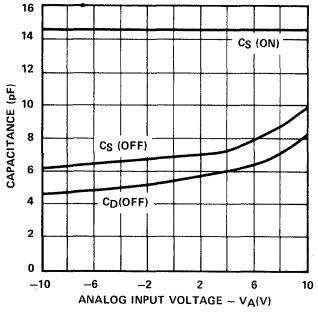
CROSSTALK AND "OFF" ISOLATION vs. FREQUENCY



LEAKAGE CURRENT vs. TEMPERATURE



SWITCH CAPACITANCE vs. ANALOG VOLTAGE



The SW-01–SW-04 designs have been optimized for low "ON" resistance variation with temperature, signal voltage, and supply voltage changes. Fast switching response and low leakage currents at high temperature are also key performance improvements over older circuit designs.

The static-electricity immune BIFET switches and additional overvoltage protection circuitry make the precision switches extremely durable in most application environments.

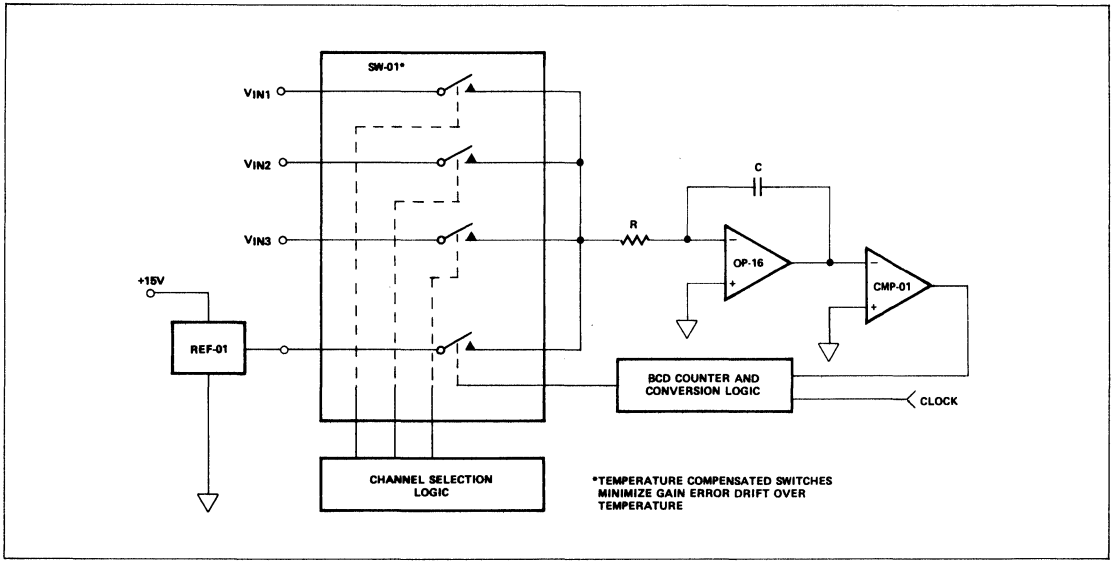
The SW-01–SW-04 are well suited to applications requiring analog currents <5mA with driving source impedances <100Ω. Applications using op amps, buffers or voltage sources as input drive sources are typical of those fulfilling these conditions. Within the given range of source impedance and analog current near ideal signal transfer accuracy is obtainable.

Applications needing very high analog current capability (>5mA) or where the switch is driven from high source impedances (>100Ω) should use the SW-201 (Pin Compatible to SW-01) or the SW-202 (Pin Compatible to SW-02) high-current Quad Switches.

Although the SW-201/SW-202 do not offer the same "ON" resistance temperature coefficient, many other premium characteristics are similar. In addition, the SW-201/SW-202 offer exceptionally low signal distortion over a wide signal voltage and frequency range.

TYPICAL APPLICATIONS

DUAL SLOPE A/D CONVERSION



SW06

QUAD SPST BI-FET ANALOG SWITCH

FEATURES

- **Highly Resistant to Static Discharge Destruction**
- **Guaranteed R_{ON} Matching ..... 15% Max.**
- **Guaranteed Switching Speeds ..... T_{ON} = 500ns Max.**
  T_{OFF} = 400ns Max.
- **Guaranteed Break-Before-Make Switching**
- **Low "ON" Resistance ..... 80Ω Max.**
- **Low R_{ON} Variation from Analog Input Voltage 5%**
- **High Analog Current Operation ..... 10mA Min.**
- **Low Leakage Currents at High Temperature:**
  T_A = 125° C ..... 60nA Max.
  T_A = 85° C ..... 30nA Max.
- **Digital Inputs TTL/CMOS Compatible**
- **Improved Specifications and Pin Compatible to LF-11333/13333**
- **Dual or Single Power Supply Operation**

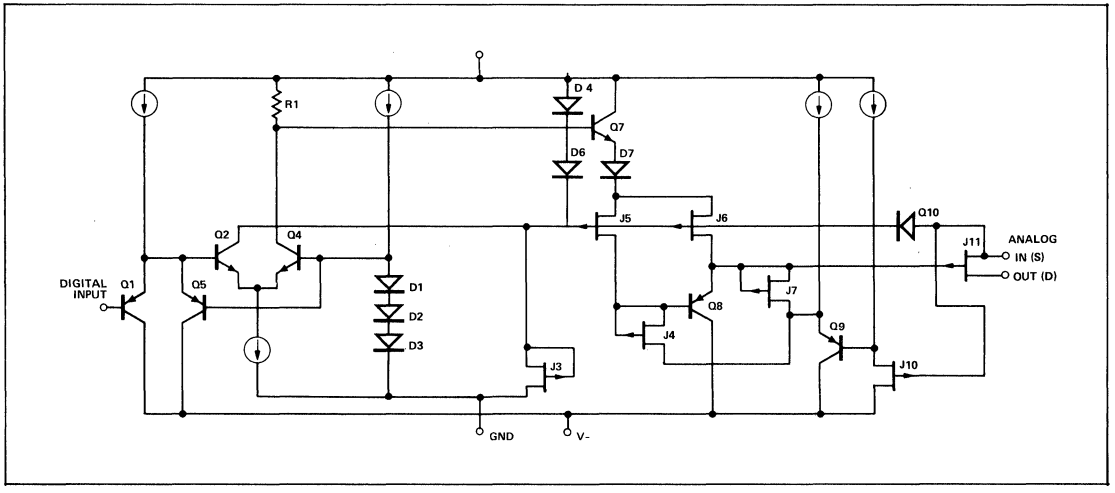
GENERAL DESCRIPTION

The SW06 is a four channel single-pole, single throw analog switch that employs both bipolar and ion-implanted FET devices. The SW06 FET switches are bipolar digital logic inputs are immune to static electricity that can catastrophically destroy devices based on CMOS technology. OEM manufacturers using CMOS devices must often establish costly special handling procedures in production to prevent static electric switch destruction. Ruggedness and reliability are inherent in the SW06 design and construction technology. *No special handling, as required with CMOS devices, is necessary to maintain the SW06 reliability.*

Increased reliability is complemented by excellent electrical specifications. Potential error sources are reduced by minimizing "ON" resistance and controlling leakage currents at high temperatures. The switching FET exhibits minimal R_{ON} variation over a 20V analog signal range and with power supply voltage changes. Operation from a single positive power supply voltage is possible. With V+ = 36V, V− = 0V, the analog signal range will extend from ground to +32V.

PNP logic inputs are TTL and CMOS compatible to allow the SW06 to upgrade existing designs. The logic "0" and logic "1" input currents are at micro-ampere levels for logic levels between 0 and 15V.

SIMPLIFIED SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS at V+ = 15V, V− = −15V and T_A = 25°C, unless otherwise specified.

			SW06B			SW06F			SW06G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
"ON" Resistance	R_{ON}	V_S = 0V, I_S = 1mA V_S = ±10V, I_S = 1mA	– –	60 65	80 80	– –	60 65	100 100	– –	100 100	150 150	Ω
R_{ON} Match Between Switches	R_{ON} Match	V_S = 0V, I_S = 100μA; Note 1	–	5	15	–	5	20	–	–	20	%
Analog Voltage Range	V_A	1mA = I_S 1mA = I_S	+11 −11	– −15	– –	+11 −11	– −15	– –	+10 −10	+11 −15	– –	V
Analog Current Range	I_A	V_S = ±10V	10	15	–	7	12	–	5	10	–	mA
ΔR_{ON} vs Applied Voltage	ΔR_{ON}	−10V ≤ V_S ≤ 10V, I_S = 1.0mA	–	5	15	–	10	20	–	10	20	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	V_S = 10V, V_D = −10V, V_{IN} = 0.8V	–	0.3	2.0	–	0.3	2.0	–	0.3	10	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	V_S = 10V, V_D = −10V, V_{IN} = 0.8V	–	0.3	2.0	–	0.3	2.0	–	0.3	10	nA
Source Current in "ON" Condition	$I_{S(ON)}$+ $I_{D(ON)}$	V_S = 10V, V_D = −10V, V_{IN} = 2.0V	–	0.3	2.0	–	0.3	2.0	–	0.3	10	nA
Logical "1" Input Voltage	V_{INH}	Full Temperature Range	2.0	–	–	2.0	–	–	2.0	–	–	V
Logical "0" Input Voltage	V_{INL}	Full Temperature Range	–	–	0.8	–	–	0.8	–	–	0.8	V
Logical "1" Input Current	I_{INH}	V_{IN} = 2.0V to 15.0V, Note 4	–	–	0.1	–	–	0.1	–	–	0.1	μA
Logical "0" Input Current	I_{INL}	V_{IN} = 0.8V	–	1.5	5.0	–	1.5	5.0	–	1.5	10.0	μA
Turn-On-Time	t_{ON}	See Switching Time Test Circuit; Note 2	–	340	500	–	340	600	–	340	700	ns
Turn-Off-Time	t_{OFF}	See Switching Time Test Circuit; Note 2	–	200	400	–	200	400	–	200	500	ns
Break-Before-Make Time	t_{ON}-t_{OFF}	Note 2, 3	50	140	–	50	140	–	50	140	–	ns
Source Capacitance	$C_{S(OFF)}$	V_S = 0V, V_{IN} = 0.8V	–	7.0	–	–	7.0	–	–	7.0	–	pF
Drain Capacitance	$C_{D(OFF)}$	V_S = 0V, V_{IN} = 0.8V	–	5.5	–	–	5.5	–	–	5.5	–	pF
Channel "ON" Capacitance		V_S = V_D = 0V	–	15	–	–	15	–	–	15	–	pF
"OFF" Isolation	$I_{SO(OFF)}$	V_S = 1V_{RMS}, R_L = 680Ω, C_L = 7pF, f = 500kHz	–	58	–	–	58	–	–	58	–	dB
Crosstalk	C_T	V_S = 1V_{RMS}, R_L = 680Ω, C_L = 7pF, f = 500kHz	–	70	–	–	70	–	–	70	–	dB
Positive Supply Current	I+	Two Channels "ON" Two Channels "OFF"	–	4.0	9.0	–	4.0	10.5	–	4.0	12.0	mA
Negative Supply Current	I−	Two Channels "ON" Two Channels "OFF"	–	1.0	5.0	–	1.0	6.0	–	1.0	6.5	mA
Positive Supply Current	I+	All Channels "OFF", V_{IN} = 0.8V	–	5.0	9.0	–	5.0	10.5	–	6.0	12.0	mA
Negative Supply Current	I−	All Channels "OFF", V_{IN} = 0.8V	–	4.0	6.0	–	4.0	7.0	–	4.0	8.0	mA
Ground Current	I_G	All Channels "ON" or "OFF"	–	3.0	4.0	–	3.0	4.0	–	3.0	6.0	mA

NOTES:

1. V_S = 0V, I_S = 100μA. Specified as a percentage of $R_{AVERAGE}$ where:

$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3} + R_{ON4}}{4}$$

2. Guaranteed by design.
3. Switch is guaranteed to provide break-before-make operation.
4. Current tested at V_{IN} = 2.0V. This is worst case condition.
5. The ground pin (GND) must be ≥4V above the V− pin to include −4V logic levels.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Operating Temperature Range
- SW06BQ ..... −55°C to +125°C
- SW06FQ ..... −25°C to +85°C
- SW06GP ..... 0°C to +70°C

Storage Temperature Range ..... −65°C to +150°C
Power Dissipation (Note 1) 900mW
Lead Soldering Temperature (60 sec) ..... 300°C
Maximum Junction Temperature ..... 150°C
V+ Supply to V− Supply 36V
V+ Supply to Ground 36V
Logic Input Voltage (Note 5) ..... −4V to V+ Supply
Analog Input Voltage Range
Continuous ..... V− Supply to V+ Supply +20V
1% Duty Cycle and Driving
all 4 Inputs with
500μsec pulse ..... V− Supply −15V to V+ Supply +20V
Maximum Current Through Any Pin 30mA

NOTES:
1. Derated 12mW/°C above 75°C.
2. Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V+ = 15V, V− = −15V, −55°C ≤ T_A ≤ +125°C for SW06BQ, −25°C ≤ T_A ≤ +85°C for SW06FQ and 0°C ≤ T_A ≤ 70°C for SW06GP.

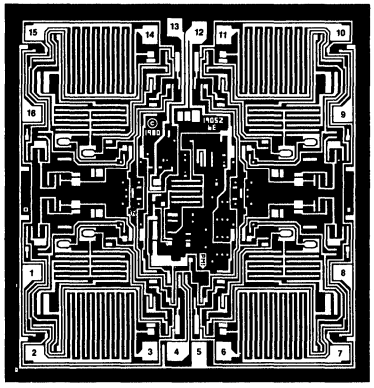
			SW06B			SW06F			SW06G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
"ON" Resistance	R_{ON}	V_S = 0V, I_D = 1.0mA V_S = ±10V, I_D = 1.0mA	–	75 80	110 110	–	75 80	125 125	–	75 80	175 175	Ω
R_{ON} Match Between Switches	R_{ON} Match	V_S = 0V, I_S = 100μA; Note 1	–	6	20	–	6	25	–	10	–	%
Analog Voltage Range	V_A	I_S = 1.0mA I_S = 1.0mA	+11 −11	– −15	– –	+11 −11	– −15	– –	+10 −10	+11 −15	– –	V
Analog Current Range	I_A	V_S = ±10.0V	7	12	–	5	11	–	–	11	–	mA
ΔR_{ON} With Applied Voltage	ΔR_{ON}	−10V ≤ V_S ≤ +10V, I_S = 100μA	–	30	–	–	30	–	–	30	–	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	V_S = 10V, V_D = −10V, V_{IN} = 0.8V T_A = Max. Operating Temp.	–	–	60	–	–	30	–	–	60	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	V_S = 10V, V_D = −10V, V_{IN} = 0.8V T_A = Max. Operating Temp.	–	–	60	–	–	30	–	–	60	nA
Leakage Current in "ON" Condition	$I_{S(ON)}$+ $I_{D(ON)}$	V_S = V_D = ±10V, V_{IN} = 2.0V T_A = Max. Operating Temp.	–	–	60	–	–	30	–	–	60	nA
Logical "1" Input Current	I_{INH}	V_{IN} = 2.0V to 15.0V, Note 4	–	–	5	–	–	5	–	–	5	μA
Logical "0" Input Current	I_{INL}	V_{IN} = 0.8V	–	4	10	–	4	10	–	5	15	μA
Turn-On-Time	t_{ON}	See Switching Time Test Circuit; Note 2	–	440	900	–	500	900	–	–	1000	ns
Turn-Off-Time	t_{OFF}	See Switching Time Test Circuit; Note 2	–	300	500	–	330	500	–	–	500	ns
Break-Before-Make Time	t_{ON}-t_{OFF}		–	70	–	–	70	–	–	50	–	ns
Positive Supply Current	I+	Two Channels "ON" Two Channels "OFF"	–	–	13.5	–	–	14.0	–	–	15.8	mA
Negative Supply Current	I−	Two Channels "ON" Two Channels "OFF"	–	–	8.5	–	–	11.0	–	–	14.5	mA
Positive Supply Current	I+	All Channels "OFF", V_{IN} = 0.8V	–	–	13.5	–	–	14.0	–	–	18.0	mA
Negative Supply Current	I−	All Channels "OFF", V_{IN} = 0.8V	–	–	8.5	–	–	11.0	–	–	14.5	mA
Ground Current	I_G	All Channels "ON" or "OFF"	–	–	6.0	–	–	7.8	–	–	10.0	mA

NOTES:
1. V_S = 0V, I_S = 100μA. Specified as a percentage of $R_{AVERAGE}$ where:

$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3} + R_{ON4}}{4}$$

2. Guaranteed by design.
3. Switch is guaranteed to provide break-before-make operation.
4. Current tested at V_{IN} = 2.0V. This is worst case condition.
5. The ground (GND) pin must be ≥ 4V above the V− pin to include −4V logic levels.

DICE CHARACTERISTICS



DIE SIZE 0.100 × 0.096 inch

1. IN (1)
2. D (1)
3. S (1)
4. GND
5. V−
6. S (2)
7. D (2)
8. IN (2)
9. IN (3)
10. D (3)
11. S (3)
12. V+
13. DISABLE
14. S (4)
15. D (4)
16. IN (4)

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS V+ = 15V, V− = −15V and T_A = 25°C, unless otherwise noted.

			SW06N			SW06G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	$-10V \le V_A \le 10V$, $I_S \le 1mA$	–	–	80	–	–	100	Ω
R_{ON} Mismatch	R_{ON} Match	V_A = 0V, $I_S \le 100\mu A$	–	5	15	–	–	20	%
ΔR_{ON} vs V_A	ΔR_{ON}	$-10V \le V_A \le 10V$, $I_S \le 1mA$	–	5	15	–	5	20	%
Positive Supply Current	I+	Note 1	–	–	9.0	–	–	10.5	mA
Negative Supply Current	I−	Note 1	–	–	6.0	–	–	7.0	mA
Ground Current	I_G		–	–	4.0	–	–	4.0	mA
Analog Voltage Range	V_A	$R_L \ge 2k\Omega$	±10.0	–	–	±10.0	–	–	V
Logic "1" Input Voltage	V_{INH}		2.0	–	–	2.0	–	–	V
Logic "0" Input Voltage	V_{INL}		–	–	0.8	–	–	0.8	V
Logic "0" Input Current	I_{INL}	$0V \le V_{IN} \le 0.8V$	–	–	5.0	–	–	5.0	μA
Logic "1" Input Current	I_{INH}	$2.0V \le V_{IN} \le 15V$, Note 2	–	–	0.1	–	–	0.1	μA
Analog Current Range	I_A	V_S = ±10V	10	–	–	7	–	–	mA

TYPICAL ELECTRICAL CHARACTERISTICS V+ = 15V, V− = −15V, and T_A = 25°C, unless otherwise noted.

			SW06N			SW06G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	$-10V \le V_A \le 10V$, $I_S \le 1mA$	–	60	–	–	60	–	Ω
Turn-On-Time	T_{ON}		–	340	–	–	340	–	ns
Turn-Off-Time	T_{OFF}		–	200	–	–	200	–	ns
Drain Current in "OFF" Condition	$I_{D(OFF)}$	V_S = 10V, V_D = −10V	–	0.3	–	–	0.3	–	nA
"OFF" Isolation	$I_{SO(OFF)}$	f = 500kHz, $R_L = 680\Omega$	–	58	–	–	58	–	dB
Crosstalk	C_T	f = 500kHz, $R_L = 680\Omega$	–	70	–	–	70	–	dB

NOTES:
1. Power supply and ground current specified for switch "ON" or "OFF".
2. Current tested at V_{IN} = 2.0V This is worst case condition.
3. The ground pin (GND) must be ≥4V above the V− pin to include −4V logic levels.

ORDERING INFORMATION†

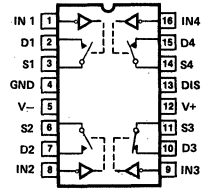
PACKAGE IS 16 PIN DIP	ORDER PART NUMBER	OPERATING TEMPERATURE RANGE
HERMETIC	SW06BQ*	MIL
HERMETIC	SW06FQ	IND
EPOXY	SW06GP	COM

* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

DISABLE INPUT	LOGIC INPUT	SWITCH STATE CHANNELS 1 & 2	SWITCH STATE CHANNELS 3 & 4
0	X	OFF	OFF
1	0	OFF	ON
1	1	ON	OFF

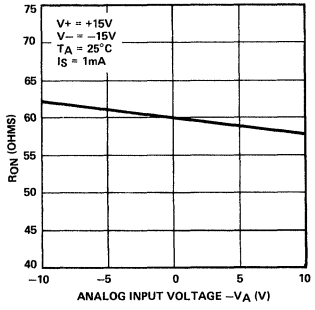
PIN CONNECTIONS



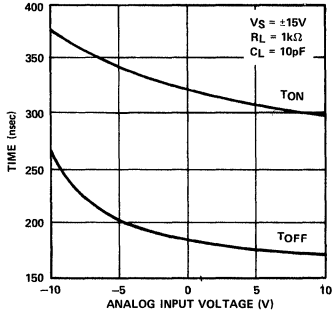
16-PIN DUAL-IN-LINE PACKAGE (Q or P Package)

TYPICAL PERFORMANCE CHARACTERISTICS

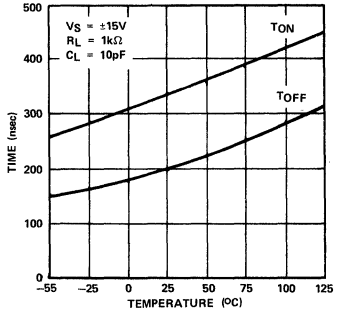
"ON" RESISTANCE vs. ANALOG VOLTAGE (V_S)



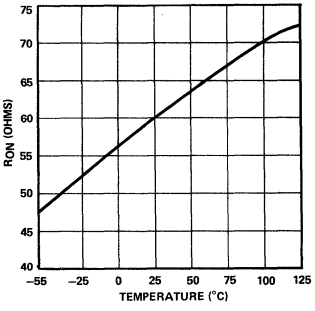
SWITCHING TIME vs. ANALOG VOLTAGE



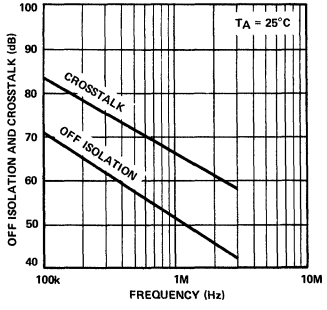
SWITCHING TIME vs. TEMPERATURE



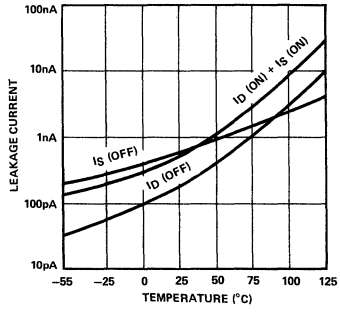
R_{ON} vs. TEMPERATURE



CROSSTALK AND "OFF" ISOLATION vs. FREQUENCY

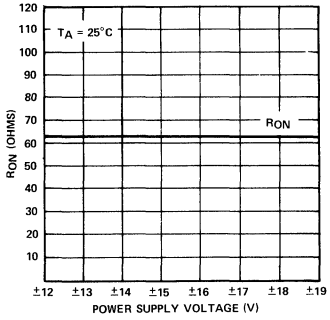


LEAKAGE CURRENT vs. TEMPERATURE

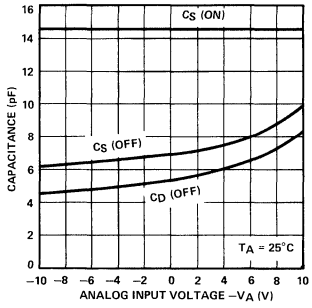


TYPICAL PERFRMANCE CHARACTERISTICS

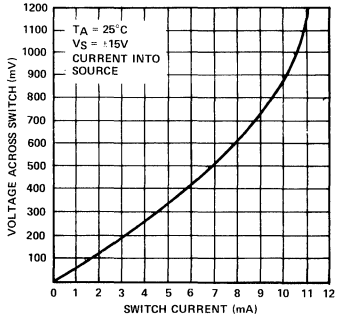
"ON" RESISTANCE vs POWER SUPPLY VOLTAGE



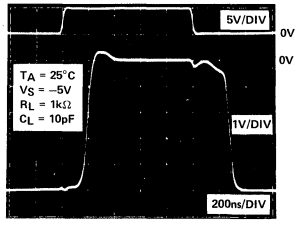
SWITCH CAPACITANCE vs. ANALOG VOLTAGE



SWITCH CURRENT vs. VOLTAGE

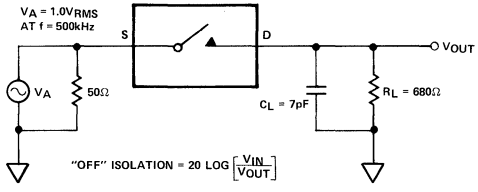


T_{ON}/T_{OFF} SWITCHING RESPONSE

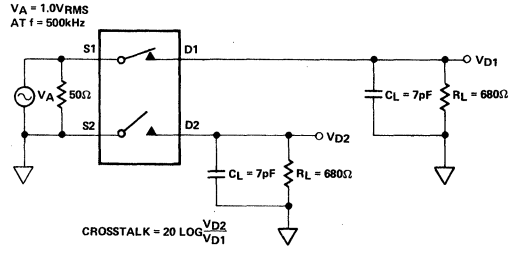


TOP TRACE: LOGIC INPUT (5V/DIV)
BOTTOM TRACE: SWITCH OUTPUT (1V/DIV)

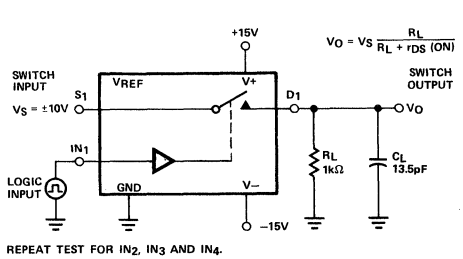
OFF ISOLATION TEST CIRCUIT

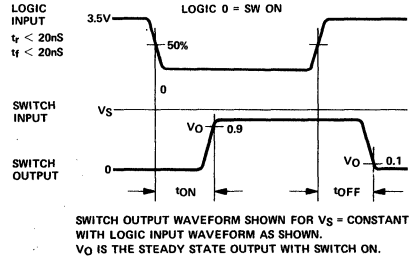


CROSSTALK TEST CIRCUIT



SWITCHING TIME TEST CIRCUIT





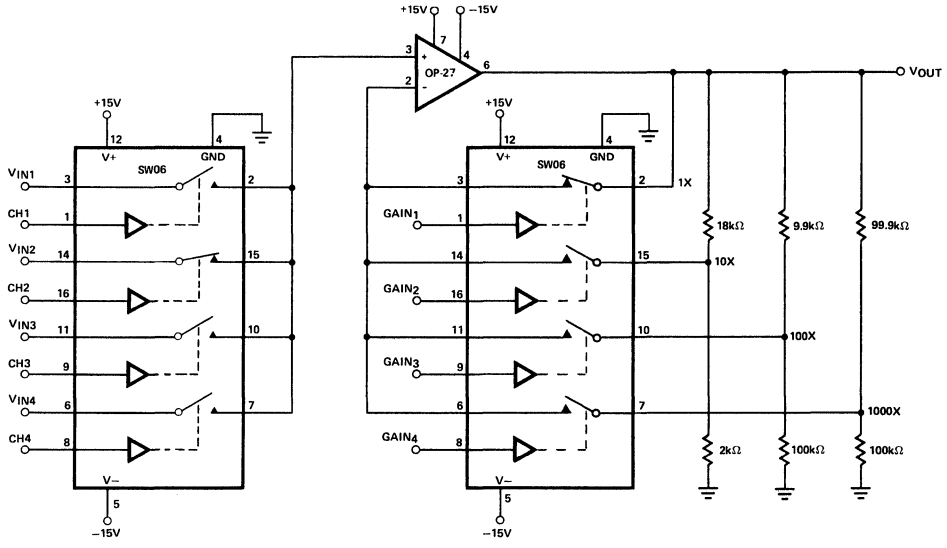
APPLICATIONS INFORMATION

This analog switch employs ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with BI-FET processing rather than CMOS, special handling is not necessary to prevent damage to these switches. Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pullup resistors are not required to TTL compatibility to insure break-before-make switching as is often the case with the CMOS switches. The digital inputs utilize PNP input transistors whereinput current is maximum at the logic "0" level and drops to that of a reverse-biased diode as the input voltage is raised above +1.4V.

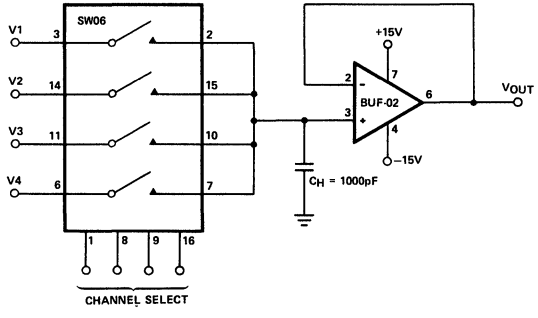
The "ON" resistance, R_{ON}, of the analog switches is constant over the wide input voltage range of −15V to +11V with $V_{SUPPLY} = \pm 15V$. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF switch remains greater than its V_p, and prevents that channel from being falsely turned ON.

TYPICAL APPLICATIONS

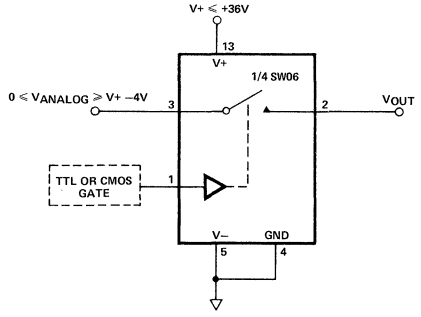
PROGRAMMABLE GAIN NON-INVERTING AMPLIFIER WITH SELECTABLE INPUTS



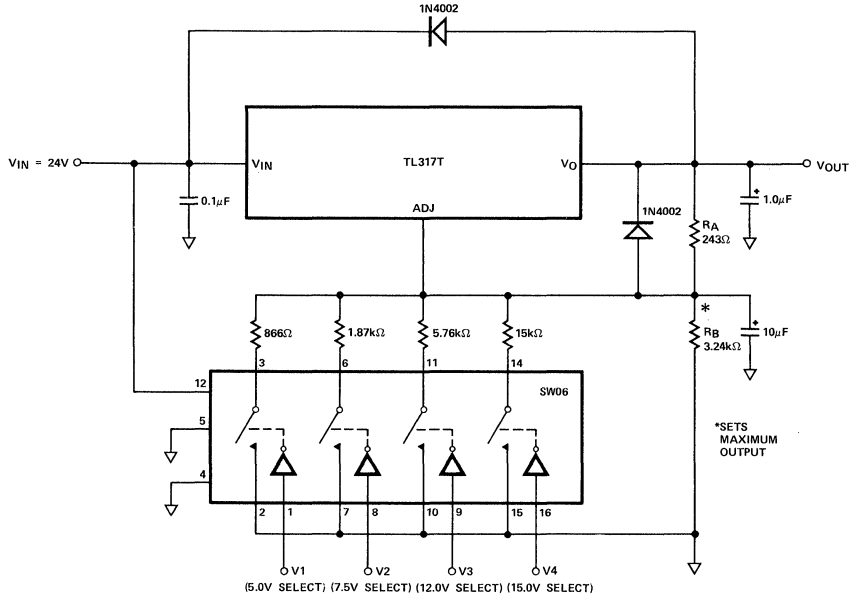
4-CHANNEL SAMPLE HOLD AMPLIFIER



OPERATION FROM SINGLE POSITIVE POWER SUPPLY



PROGRAMMABLE VOLTAGE SUPPLY



V_O	R_i	NOTE
5.0	866Ω	$V_O \approx 1.25\left(1 + \frac{R_B \mid\mid R_i}{R_A}\right)$
7.5	1.87 kΩ	
12.0	5.76 kΩ	
15.0	15.0 kΩ	
SWITCH $R_{ON} \approx 60\Omega$ R_B = 3.24 kΩ		

SW-201/SW-202

QUAD SPST BI-FET ANALOG SWITCHES

FEATURES

SW-201
- **Normally "ON" for Logic 0 Input**
- **Improved Performance and Pin Compatible With DG-201, LF11201/13201, HI201, and IH201.**

SW-202
- **Normally "OFF" For Logic 0 Input**
- **Improved Performance and Pin Compatible With LF11202/12202/13202 and IH202**

Both SW-201 and SW-202
- **Highly Resistant to Static Discharge Destruction**
- **Guaranteed Break-Before-Make Switching ($t_{OFF} < t_{ON}$)**
- **Low "ON" Resistance ..... 80Ω Max.**
- **Guaranteed R_{ON} Matching ..... 15% Max.**
- **Low R_{ON} Variation from Analog Input Voltage 5%**
- **High Analog Current Operation ..... 10mA Min.**
- **Low Leakage Currents at High Temperatures:**
  T_A = 125°C ..... 60nA Max.
  T_A = 85°C ..... 30nA Max.
- **Guaranteed Switching Speeds:**
  t_{ON} = 500ns Max. t_{OFF} = 400ns Max.
- **Digital Inputs are TTL/CMOS Compatible and are Low Current PNP Transistors.**

GENERAL DESCRIPTION

The SW-201 and SW-202 each consist of four independent, single-pole, single-throw (SPST) analog switches, which may be independently digitally controlled. Each SW-201 switch is normally closed (NC), whereas each SW-202 is normally open (NO) when the corresponding digital control input is a zero. The SW-201 and SW-202 are otherwise identical.

The judicious combination of bipolar and FET devices in a single monolithic IC results in a product with performance characteristics and ruggedness that are superior to those of a similar circuit fabricated using CMOS technology. No special handling requirements are necessary to maintain the SW-201/SW-202 reliability.

Increased reliability is complemented by excellent electrical specifications. Potential error sources are reduced by minimizing "ON" resistance and controlling leakage currents at high temperatures. The switching FET exhibits minimal R_{ON} variation over a 20V analog signal range and with power supply voltage changes. Operation from a single positive power supply voltage is possible. With V+ = 36V, V− = 0V, the analog signal range will extend from ground to +32V.

The PNP logic inputs are TTL and CMOS compatible and require input currents at the micro-ampre level for logic levels between 0V and 15V.

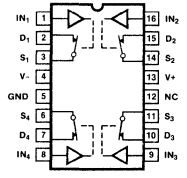
ORDERING INFORMATION†

DIP PACKAGE	SWITCH CONFIGURATION NC	SWITCH CONFIGURATION NO	OPERATING TEMPERATURE RANGE
16 PIN HERMETIC	SW201BQ*	SW202BQ*	MIL
16 PIN HERMETIC	SW201FQ	SW202FQ	IND
16 PIN EPOXY	SW201GP	SW202GP	COM

*Also available with MIL-STD-883B processing. To order add /883 as a suffix to the part number.
† All listed parts are available with 160 hour burn-in. See Ordering Information.

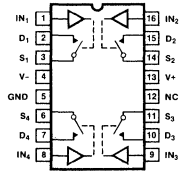
PIN CONNECTIONS

16-PIN DUAL-IN-LINE PACKAGE
(Q or P Package)



SW-201
CONTROL LOGIC

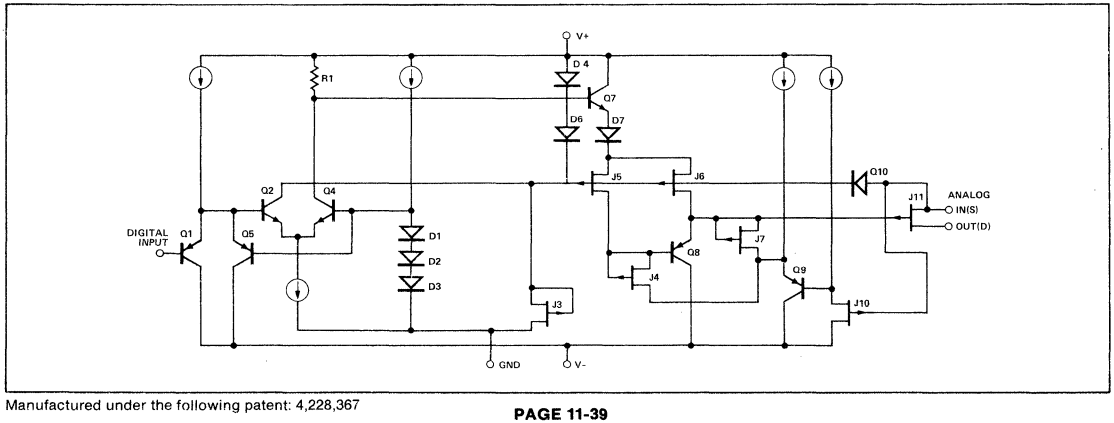
LOGIC	SWITCH
0	ON
1	OFF



SW-202
CONTROL LOGIC

LOGIC	SWITCH
0	OFF
1	ON

SIMPLIFIED SCHEMATIC DIAGRAM (ONE SWITCH)



Manufactured under the following patent: 4,228,367

ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating Temperature Range
- SW-201BQ, SW-202BQ ..... −55°C to +125°C
- SW-201FQ, SW-202FQ ..... −25°C to +85°C
- SW-201GP, SW-202GP ..... 0°C to +70°C

DICE Junction Temperature (T_j) ..... −65°C to +150°C
Storage Temperature Range ..... −65°C to +150°C
Power Dissipation (Note 2) 900mW
Lead Soldering Temperature (60 sec) ..... 300°C
Maximum Junction Temperature ..... 150°C
V+ Supply to V− Supply 36V
V+ Supply to Ground 36V
Logic Input Voltage ..... −4V to V+ Supply
Analog Input Voltage Range
- Continuous ..... V− Supply to V+ Supply +20V

1% Duty Cycle and Driving all 4 Inputs with 500μsec pulse ..... V− Supply −15V to V+ Supply +20V

Maximum Current Through Any Pin 30mA

NOTES:
1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Derated 12mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS at V± = ±15V and T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-201B SW-202B MIN	SW-201B SW-202B TYP	SW-201B SW-202B MAX	SW-201F SW-202F MIN	SW-201F SW-202F TYP	SW-201F SW-202F MAX	SW-201G SW-202G MIN	SW-201G SW-202G TYP	SW-201G SW-202G MAX	UNITS
"ON" Resistance	R_{ON}	V_A = 0V, I_S = 1mA	—	60	80	—	60	100	—	100	150	Ω
		V_A = ±10V, I_S = 1mA	—	65	80	—	65	100	—	100	150	
R_{ON} Match Between Switches	R_{ON} Match	V_A = 0V, I_D = 100μA; Note 1	—	5	15	—	5	20	—	—	20	%
Analog Voltage Range	V_A	I_S = 1.0mA	+10	+11	—	+10	+11	—	+10	+11	—	V
		I_S = 1.0mA	−10	−15	—	−10	−15	—	−10	−15	—	
Analog Current Range	I_A	V_S = ±10V	10	15	—	7	12	—	5	10	—	mA
ΔR_{ON} vs Applied Voltage	ΔR_{ON}	−10V ≤ V_S ≤ 10, I_S = 1.0mA	—	5	15	—	10	20	—	10	20	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	V_S = 10V, V_D = −10V, V_{IN} = 2.0V	—	0.3	2.0	—	0.3	2.0	—	—	10	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	V_S = 10V, V_D = −10V, V_{IN} = 2.0V	—	0.3	2.0	—	0.3	2.0	—	—	10	nA
Leakage Current in "ON" Condition	$I_{S(ON)}$ + $I_{D(ON)}$	V_S = V_D = ±10V, V_{IN} = 0.8	—	0.3	2.0	—	0.3	2.0	—	—	10	nA
Logical "1" Input Voltage	V_{INH}	Full Temperature Range	2.0	—	—	2.0	—	—	2.0	—	—	V
Logical "0" Input Voltage	V_{INL}	Full Temperature Range	—	—	0.8	—	—	0.8	—	—	0.8	V
Logical "1" Input Current	I_{INH}	V_{IN} = 2V to 15V; Note 4	—	—	0.1	—	—	0.1	—	—	0.1	μA
Logical "0" Input Current	I_{INL}	V_{IN} = 0.8	—	1.5	5.0	—	1.5	5.0	—	1.5	10.0	μA
Turn-On-Time	t_{ON}	See Switching Time Test Circuit; Note 2	—	340	500	—	340	600	—	340	700	ns
Turn-Off-Time	t_{OFF}	See Switching Time Test Circuit; Note 2	—	200	400	—	200	400	—	200	500	ns
Break-Before-Make Time	t_{ON}-t_{OFF}	Notes 2, 3	50	140	—	50	140	—	50	140	—	ns
Source Capacitance	$C_{S(OFF)}$	V_A = 0V, V_{IN} = 2.0V	—	7.0	—	—	7.0	—	—	7.0	—	pF
Drain Capacitance	$C_{D(OFF)}$	V_A = 0V, V_{IN} = 2.0V	—	5.5	—	—	5.5	—	—	5.5	—	pF
Channel "ON" Capacitance		V_S = V_D = 0V	—	15.0	—	—	15.0	—	—	15.0	—	pF
"OFF" Isolation	$I_{SO(OFF)}$	V_S = 1VRMS, R_L = 680Ω, C_L = 7pF, f = 500kHz	—	58	—	—	58	—	—	58	—	dB
Crosstalk	C_T	V_S = 1VRMS, R_L = 680Ω, C_L = 7pF, f = 500kHz	—	70	—	—	70	—	—	70	—	dB
Positive Supply Current	I=	All Channels "ON", V_{IN} = 0	—	4.0	9.0	—	4.0	10.5	—	4.0	12.0	mA
Negative Supply Current	I−	All Channels "ON", V_{IN} = 0	—	1.0	5.0	—	1.0	6.0	—	1.0	6.5	mA
Positive Supply Current	I+	All Channels "OFF", V_{IN} = 2.0	—	5.0	9.0	—	5.0	10.5	—	6.0	12.0	mA
Negative Supply Current	I−	All Channels "OFF", V_{IN} = 2.0	—	4.0	6.0	—	4.0	7.0	—	4.0	8.0	mA
Ground Current	I_G	All Channelse "ON" or "OFF"	—	3.0	4.0	—	3.0	4.0	—	3.0	6.0	mA

NOTES:
1. V_A = 0V, I_D = 100μA. Specified as a percentage of $R_{AVERAGE}$ where:
$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3} + R_{ON4}}{4}$$
2. Guaranteed by design.
3. Switch is guaranteed to provide break-before-make operation.
4. Current tested at V_{IN} = 2.0V. This is worst case condition.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$; $-55°C \le T_A \le +125°C$ for SW-201/202-BQ; $-25°C \le T_A \le +85°C$ for SW-201/202-BQ; $0°C \le T_A \le 70°C$ for SW-201/202-GP.

			SW-201B SW-202B			SW-201F SW-202F			SW-201G SW-202G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
"ON" Resistance	R_{ON}	$V_A = 0V$, $I_D = 1mA$ $V_A = \pm 10V$, $I_D = 1mA$	— —	75 80	110 110	— —	75 80	125 125	— —	— —	175 175	Ω
R_{ON} Match Between Switches	R_{ON} Match	$V_A = 0V$, $I_D = 100\mu A$; Note 1	—	6	20	—	6	25	—	10	—	%
Analog Voltage Range	V_A	$I_S = 1.0mA$ $I_S = 1.0mA$	+10 −10	+11 −15	— —	+10 −10	+11 −15	— —	+10 −10	+11 −15	— —	V
Analog Current Range	I_A	$V_S = \pm 10.0V$	7	12	—	5	11	—	—	11	—	mA
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \le V_S \le +10$, $I_S = 100mA$	—	30	—	—	30	—	—	30	—	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$, $V_{IN} = 2.0V$ T_A = Max. Operating Temp.	—	—	60	—	—	30	—	—	60	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$, $V_{IN} = 2.0V$ T_A = Max. Operating Temp.	—	—	60	—	—	30	—	—	60	nA
Leakage Current in "ON" Condition	$I_{S(ON)} + I_{D(ON)}$	$V_S = V_D = \pm 10V$, $V_{IN} = 0.8$ T_A = Max. Operating Temp.	—	0.3	2.0	—	0.3	2.0	—	—	10	nA
Logical "1" Input Current	I_{INH}	$V_{IN} = 2.0V$ to 15.0V, Note 4	—	—	5.0	—	—	5.0	—	—	5.0	μA
Logical "0" Input Current	I_{INL}	$V_{IN} = 0.8$	—	4.0	10	—	4.0	10	—	5.0	15	μA
Turn-On-Time	t_{ON}	See Test Circuit, Note 2	—	440	900	—	500	900	—	—	1000	ns
Turn-Off-Time	t_{OFF}	See Test Circuit, Note 2 Test Circuit; Note 2	—	300	500	—	330	500	—	—	500	ns
Break-Before-Make Time	t_{ON}-t_{OFF}	Notes 2, 3	—	70	—	—	70	—	—	50	—	ns
Positive Supply Current	I=	All Channels "ON", $V_{IN} = 0$	—	—	13.5	—	—	14.0	—	—	15.8	mA
Negative Supply Current	I−	All Channels "ON", $V_{IN} = 0$	—	—	8.5	—	—	11.0	—	—	14.5	mA
Positive Supply Current	I+	All Channels "OFF", $V_{IN} = 2.0$	—	—	13.5	—	—	14.0	—	—	18	mA
Negative Supply Current	I−	All Channels "OFF", $V_{IN} = 2.0$	—	—	8.5	—	—	11.0	—	—	14.5	mA
Ground Current	I_G	All Channelse "ON" or "OFF"	—	—	6.0	—	—	7.8	—	—	10.0	mA

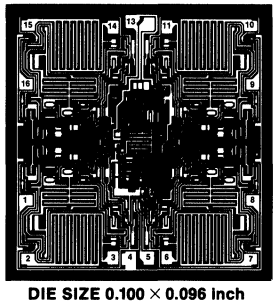
NOTES:

1. $V_A = 0V$, $I_D = 100\mu A$. Specified as a percentage of $R_{AVERAGE}$ where:

$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3} + R_{ON4}}{4}$$

2. Guaranteed by design.
3. Switch is guaranteed to provide break-before-make operation.
4. Current tested at $V_{IN} = 2.0V$. This is worst case condition.

DICE CHARACTERISTICS



DIE SIZE 0.100 × 0.096 inch

1. SWITCH 1 ADDRESS (IN1)
2. SWITCH 1 DRAIN (D1)
3. SWITCH 1 SOURCE (S1)
4. NEGATIVE SUPPLY V−
5. GROUND (GND)
6. SWITCH 4 SOURCE (S4)
7. SWITCH 4 DRAIN (D4)
8. SWITCH 4 ADDRESS (IN4)
9. SWITCH 3 ADDRESS (IN3)
10. SWITCH 3 DRAIN (D3)
11. SWITCH 3 SOURCE (S3)
13. POSITIVE SUPPLY V+
14. SWITCH 2 SOURCE (S2)
15. SWITCH 2 DRAIN (D2)
16. SWITCH 2 ADDRESS (IN2)

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS V+ = 15V, V− = −15V and T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-201N SW-202N LIMIT	SW-201G SW-202G LIMIT	UNITS
"ON" Resistance	R_{ON}	$-10V \le V_A \le 10V$, $I_S \le 1mA$	80	100	Ω MAX
R_{ON} Mismatch	R_{ON} Match	V_A = 0V, $I_S \le 100\mu A$	15	20	% MAX
ΔR_{ON} vs V_A	ΔR_{ON}	$-10V \le V_A \le 10V$, $I_S \le 1mA$	15	20	% MAX
Positive Supply	I+	Note 1	9.0	10.5	mA MAX
Negative Supply Current	I−	Note 1	6.0	7.0	mA MAX
Ground Current	I_G		4.0	4.0	mA MAX
Analog Voltage Range	V_A	$R_L \ge 2k\Omega$	±10.0	±10.0	V MIN
Logic "1" Input Voltage	V_{INH}		2.0	2.0	V MIN
Logic "0" Input Voltage	V_{INL}		0.8	0.8	V MAX
Logic "0" Input Current	I_{INL}	$0V \le V_{IN} \le 0.8V$	5.0	5.0	μA MAX
Logic "1" Input Current	I_{INH}	$2.0V \le V_{IN} \le 15V$, Note 2	0.1	0.1	μA MAX
Analog Current Range	I_A	$V_S = \pm 10V$	10	7	mA MIN

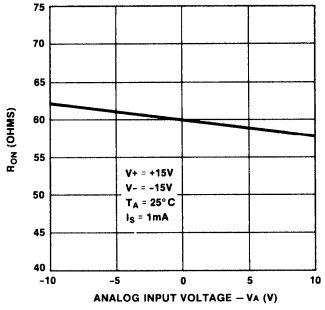
TYPICAL ELECTRICAL CHARACTERISTICS V+ = 15V, V− = −15V and T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-201N SW-202N TYP	SW-201G SW-202G TYP	UNITS
"ON" Resistance	R_{ON}	$-10V \le V_A \le 10V$, $I_S \le 1mA$	60	60	Ω
Turn-On-Time	t_{ON}		340	340	ns
Turn-Off-Time	t_{OFF}		200	200	ns
Drain Current in "OFF" Condition	$I_{D(OFF)}$	V_S = 10V, V_D = −10V	0.3	0.3	nA
"OFF" Isolation	$I_{SO(OFF)}$	f = 500kHz, $R_L = 680\Omega$	58	58	dB
Crosstalk	C_T	f = 500kHz, $R_L = 680\Omega$	70	70	dB

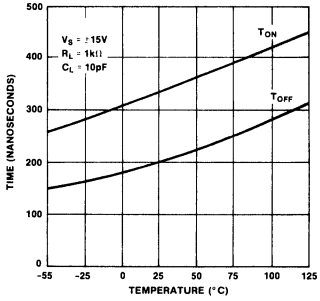
NOTES:
1. Power supply and ground current specified for switch "ON" or "OFF".
2. Current tested at V_{IN} = 2.0V. This is worst case condition.
3. The ground (GND) pin must be ≥ 4V above V− pin to include −4V logic levels.

TYPICAL PERFORMANCE CURVES

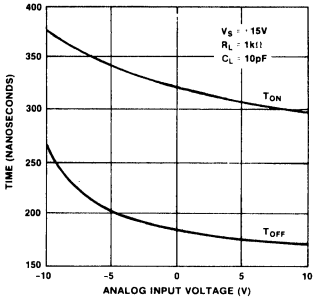
"ON" RESISTANCE VS. ANALOG VOLTAGE (VA)



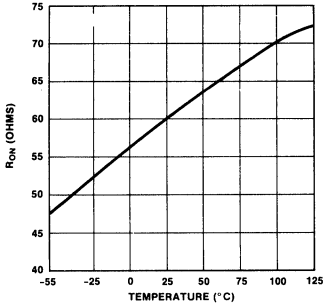
SWITCHING TIME VS. TEMPERATURE



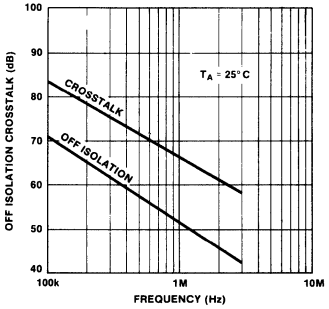
SWITCHING TIME VS. ANALOG VOLTAGE



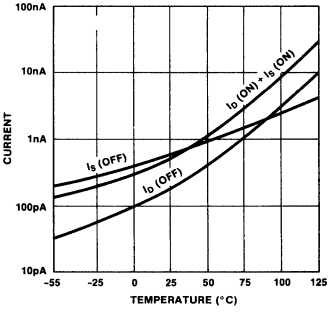
R_{ON} VS. TEMPERATURE



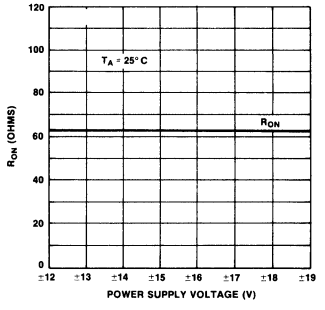
CROSSTALK AND "OFF" ISOLATION VS. FREQUENCY



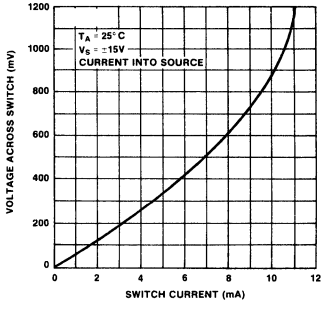
LEAKAGE CURRENT VS. TEMPERATURE



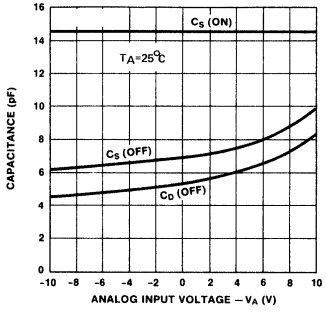
"ON" RESISTANCE VS. POWER SUPPLY VOLTAGE



SWITCH CURRENT VS. VOLTAGE

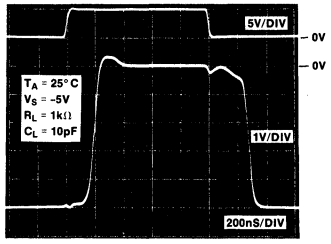


SWITCH CAPACITANCE VS. ANALOG VOLTAGE



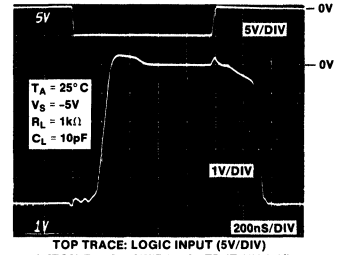
TYPICAL PERFORMANCE CURVES

SW-201
t_{ON}/t_{OFF} SWITCHING RESPONSE



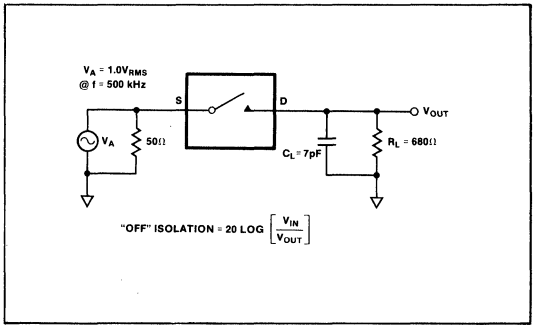
TOP TRACE: LOGIC INPUT (5V/DIV)
BOTTOM TRACE: SWITCH OUTPUT (1V/DIV)

SW-202
t_{ON}/t_{OFF} SWITCHING RESPONSE

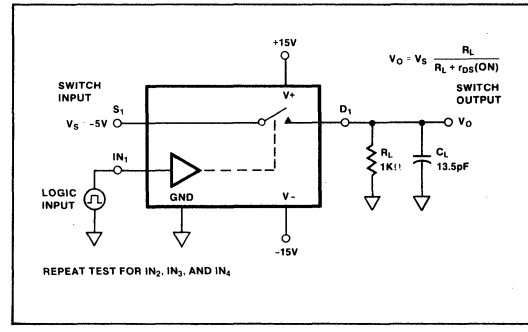


TOP TRACE: LOGIC INPUT (5V/DIV)
BOTTOM TRACE: SWITCH OUTPUT (1V/DIV)

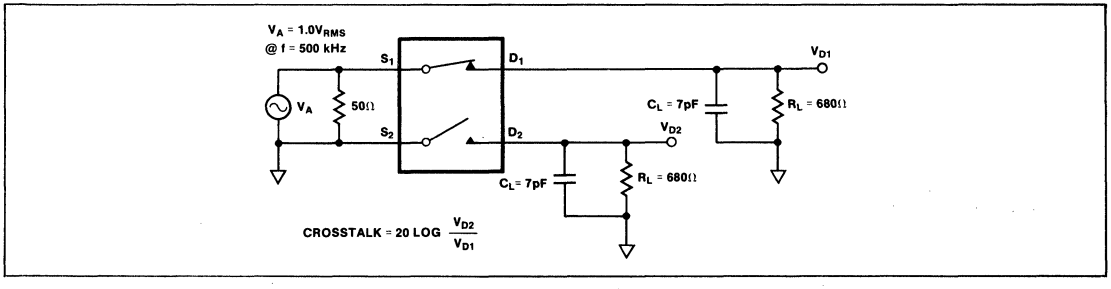
OFF ISOLATION TEST CIRCUIT



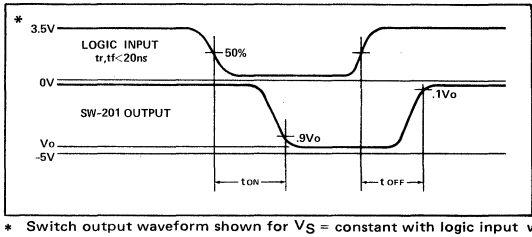
SWITCHING TIME TEST CIRCUIT



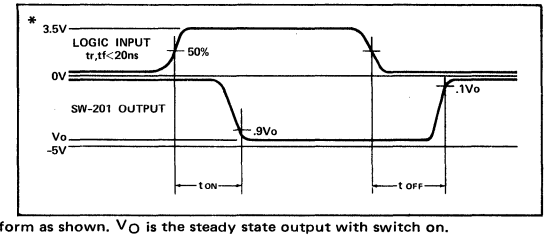
CROSSTALK TEST CIRCUIT



SW-201 WAVEFORMS



SW-202 WAVEFORMS



* Switch output waveform shown for V_S = constant with logic input waveform as shown. V_O is the steady state output with switch on.

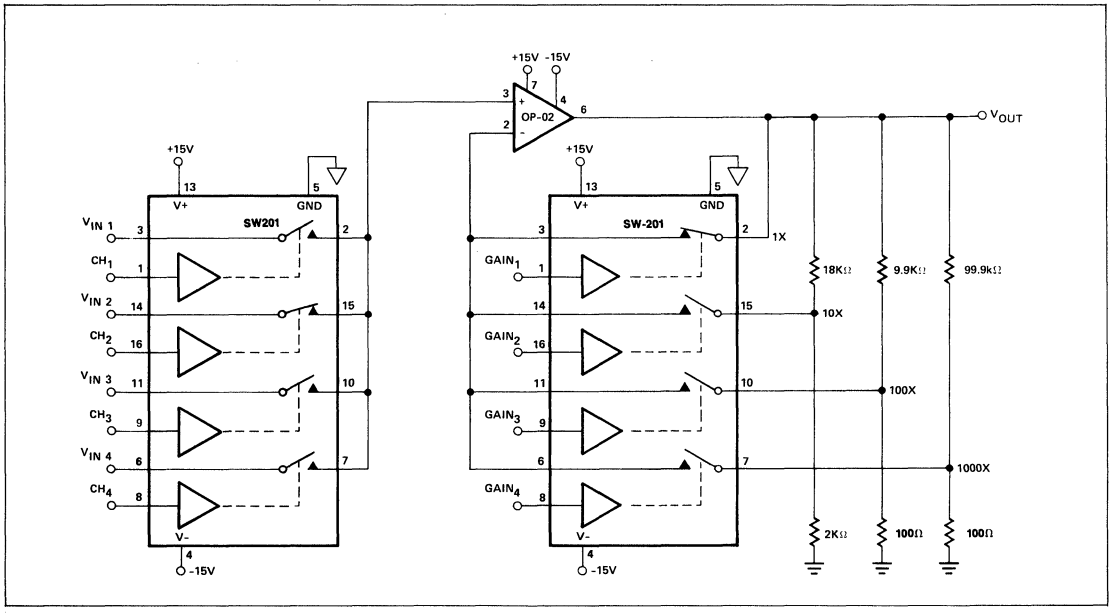
APPLICATIONS INFORMATION

This analog switch employs ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with BI-FET processing rather than CMOS, special handling is not necessary to prevent damage to these switches. Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pullup resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS switches. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode as the input voltage is raised above ≈1.4V.

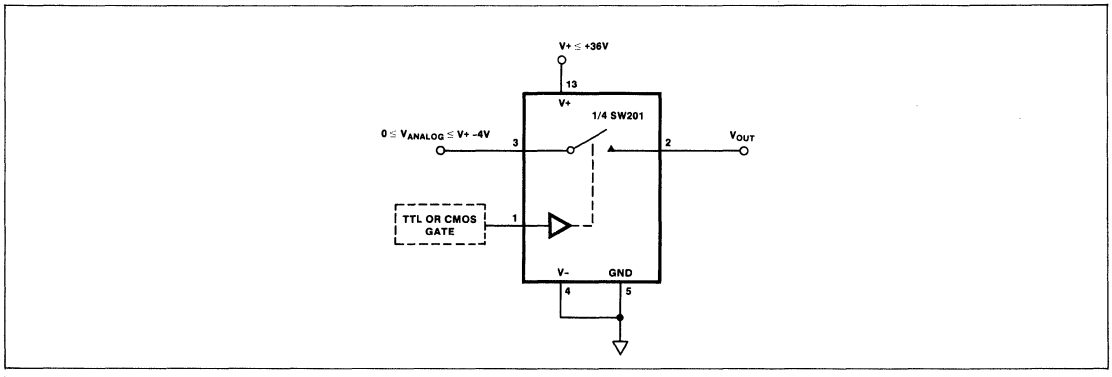
The "ON" resistance, R_{ON}, of the analog switches is constant over the wide input voltage range of −15V to +11V with $V_{SUPPLY} = \pm 15V$. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF switch remains greater than its V_p, and prevents that channel from being falsely turned ON. Individual switches are "ON" without power applied.

TYPICAL APPLICATIONS

PROGRAMMABLE GAIN NON-INVERTING AMPLIFIER WITH SELECTABLE INPUTS



OPERATION FROM SINGLE POSITIVE POWER SUPPLY



SW7510/7511

QUAD SPST BI-FET ANALOG SWITCHES

FEATURES

- **Pin Compatible with AD7510 DI, AD7511 DI**
- **JFET Switches Rather than CMOS**
- **Highly Resistant to Static Discharge Damage**
- **No SCR Latch-up Problems**
- **Low "ON" Resistance — 75Ω Maximum**
- **Superior "OFF" Isolation and Crosstalk**
- **Digital Inputs Compatible with TTL and CMOS**
- **No Pull-up Resistors Required to Insure Break-Before-Make Action With TTL Inputs**

ORDERING INFORMATION†

25°C RESISTANCE	PACKAGE HERMETIC DIP	TEMPERATURE RANGE
60Ω	SW7510AQ*	MIL
	SW7510EQ	IND
75Ω	SW7510BQ*	MIL
	SW7510FQ	IND
60Ω	SW7511AQ*	MIL
	SW7511EQ	IND
75Ω	SW7511BQ*	MIL
	SW7511FQ	IND

* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

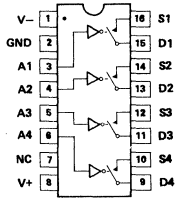
† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

GENERAL DESCRIPTION

The SW7510/7511 are monolithic linear devices, each containing four independently selectable SPST analog switches. Offering both normally open (SW7510), and normally closed operation (SW7511), these units are fabricated with Precision Monolithic's high-performance BI-FET technology. Because JFET switches are used, **special handling, as required with CMOS, is not necessary to avoid damaging these units.**

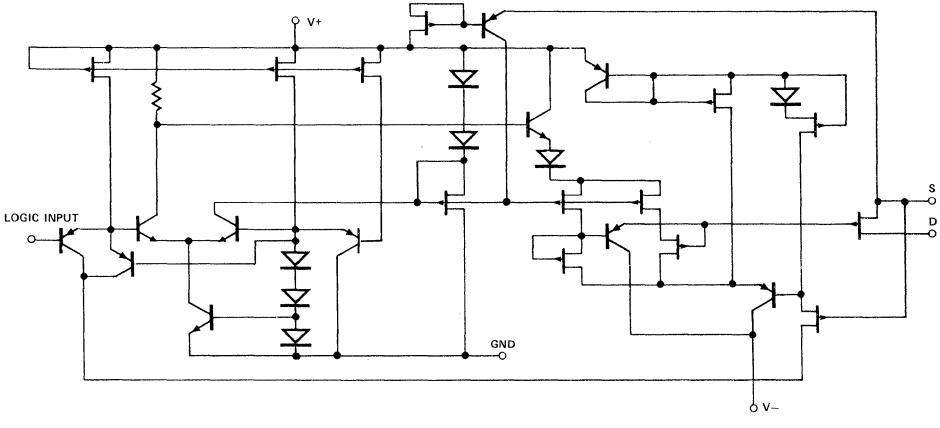
Performance advantages include exceptionally high "OFF" isolation and low crosstalk. Low leakage currents enable high transfer accuracy applications which include programmable gain amplifiers and active filters. Data conversion, position controllers, choppers, demodulators, and general purpose switching and multiplexing are among other applications for which these devices are well suited.

PIN CONNECTIONS



16-PIN HERMETIC DUAL-IN-LINE (Q-Suffix)
CONTROL LOGIC:
SW7510: Switch "ON" for Address "HIGH"
SW7511: Switch "ON" for Address "LOW"

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Operating Temperature Range,
SW7510/7511 AQ, BQ ..... −55°C to +125°C
SW7510/7511 EQ, FQ ..... −25°C to +85°C
DICE Junction Temperature (T_j) ..... −65°C to +150°C
Storage Temperature Range ..... −65°C to +150°C
Power Dissipation 500mW
Derate above 100°C ..... 10mW/°C
Lead Soldering Temperature (60 sec) ..... 300°C
Maximum Junction Temperature ..... 150°C
V+ Supply to V− Supply 36V
V+ Supply to Ground 36V
Logic Input Voltage ..... Note 3
Analog Input Voltage
Continuous ..... V− Supply to V+ Supply +20V
1% Duty Cycle and Driving
all 4 Inputs with
500 μs pulse .... V− Supply −15V to V+ Supply +20V
Maximum Current through Any Pin 25mA

NOTE: Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and $T_A = +25°C$, unless otherwise noted.

			SW7510A/E SW7511A/E			SW7510B/F SW7511B/F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
"ON" Resistance	R_{ON}	$V_D = 0V$, $I_{DS} = 1mA$	—	60	75	—	80	100	Ω
ΔR_{ON} vs. V_D (V_S)	ΔR_{ON}	$-10V \le V_D \le +10V$, $I_{DS} = 1mA$	—	6	10	—	10	10	%
R_{ON} Match of Switches	R_{ON} Match	$V_D = 0V$, $I_{DS} = 1mA$	—	1.5	10	—	1.5	10	%
Analog Voltage Range	V_A	$I_S = 1mA$	+10 −10	+11 −15	— —	+10 −10	+11 −15	— —	Volts
"OFF" Leakage Current	$I_{S(OFF)}$, $I_{D(OFF)}$	$V_S = +10V$, $V_D = -10V$ (Note 1)	—	—	1.0	—	—	3.0	nA
"ON" Leakage Current	$I_{S(ON)} + I_{D(ON)}$	$V_S = V_D = +10V$ (Note 1)	—	—	1.0	—	—	3.0	nA
Logic "1" Voltage	V_{INH}		2.0	—	—	2.0	—	—	Volts
Logic "0" Voltage	V_{INL}		—	—	0.8	—	—	0.8	Volts
Logic "0" Current	I_{INL}	$V_{IN} = +0.4V$	—	1.5	3.5	—	1.5	3.5	μA
Logic Input Capacitance	C_{DIG}	$V_{IN} = +0.4V$	—	1.5	—	—	1.5	—	pF
"ON" Switching Time	t_{ON}	$V_S = -5V$, $R_L = 1k\Omega$, $C_L = 7pF$ (Note 5)	—	350	450	—	450	550	ns
"OFF" Switching Time	t_{OFF}	$V_S = -5V$, $R_L = 1k\Omega$, $C_L = 7pF$ (Note 5)	—	260	300	—	350	450	ns
"OFF" Isolation	ISO_{OFF}	(Note 2)	—	66	—	—	66	—	dB
Crosstalk	C_T	(Note 4)	—	70	—	—	70	—	dB
Analog "OFF" Capacitance	$C_{S(OFF)}$, $C_{D(OFF)}$	$V_S = 0V$, $V_D = 0$	—	6.5	—	—	6.5	—	pF
Analog "ON" Capacitance	$C_{S(ON)}$, $C_{D(ON)}$	$V_S = 0V$, $V_D = 0$	—	14	—	—	14	—	pF
Feedthrough Capacitance	$C_{DS(OFF)}$	$V_S = 0V$	—	0.8	—	—	0.8	—	pF
Channel Capacitance	$C_{SS(OFF)}$,	$V_S = 0V$	—	0.4	—	—	0.4	—	pF
	$C_{DD(OFF)}$	$V_S = 0V$		0.4	—	—	0.4	—	pF
Positive Supply Current	I+	Logic Inputs at "0" or "1"	—	5.0	9.0	—	3.0	9.0	mA
Negative Supply Current	I−	Logic Inputs at "0" or "1"	—	2.8	5.0	—	1.7	5.0	mA

NOTES:

1. The conditions listed specifty the worst case leakage currents. The leakage currents apply equally to source (S) or drain (D).
2. OFF isolation is measured by driving the source of any OFF switch, and observing the voltage which appears on the drain. The conditions are: $R_L = 680\Omega$, $C_L = 7pF$, $V_S = 1V$, RMS, f = 100kHz.
3. The minimum logic input voltage may be as much as 2V below the GND (pin 2) terminal; however it may not be lower than the V− terminal (pin 1). The maximum logic input voltage may be as much as 36V above the V− terminal.
4. Crosstalk is measured by driving source of any OFF switch and observing voltage which appears on any other "ON" output drain. The conditions are: $R_L = 680\Omega$, $C_L = 7pF$, $V_S = 1V$, f = 100kHz.
5. Sample tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$ for SW7510AQ, BQ and SW7511AQ, BQ and $-25°C \le T_A \le +85°C$ for SW7510EQ, FQ and SW7511EQ, FQ, unless otherwise noted.

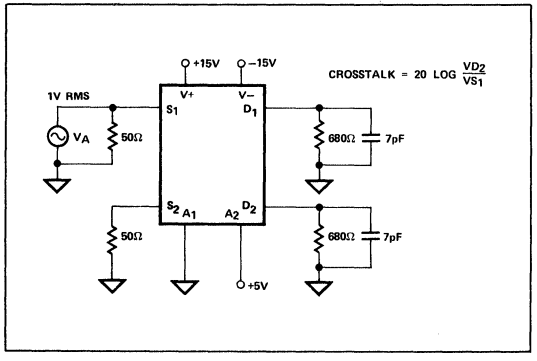
			SW7510A/E SW7511A/E			SW7510B/F SW7511B/F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
"ON" Resistance	R_{ON}	$V_D = 0V$, $I_{DS} = 1mA$	—	—	100	—	—	150	Ω
R_{ON} vs. Temperature	R_{ON} Drift	$V_D = 0V$, $I_{DS} = 1mA$	—	0.4	—	—	0.5	—	%/°C
Analog Voltage Range	V_A	$I_S = 1mA$	+10 −10	+11 −15	— —	+10 −10	+11 −15	— —	Volts
"OFF" Leakage Current	$I_{S(OFF)}$, $I_{D(OFF)}$	$V_S = +10V$, $V_D = -10V$ (Note 1)	—	—	90	—	—	100	nA
"ON" Leakage Current	$I_{S(ON)} + I_{D(ON)}$	$V_S = V_D = +10V$ (Note 1)	—	—	90	—	—	100	nA
Logic "1" Voltage	V_{INH}		2.0	—	—	2.0	—	—	Volts
Logic "0" Voltage	V_{INL}		—	—	0.8	—	—	0.8	Volts
Logic "0" Current	I_{INL}	$V_{IN} = +0.4V$	—	—	5.0	—	—	7.0	μA
"ON" Switching Time	t_{ON}	$V_S = -5V$, $R_L = 1k\Omega$, $C_L = 7pF$	—	—	600	—	—	1000	ns
"OFF" Switching Time	t_{OFF}	$V_S = -5V$, $R_L = 1k\Omega$, $C_L = 7pF$	—	—	500	—	—	750	ns
Positive Supply Current	I+	Logic Inputs at "0" or "1"	—	—	13	—	—	13	mA
Negative Supply Current	I−	Logic Inputs at "0" or "1"	—	—	7.5	—	—	7.5	mA

NOTE:

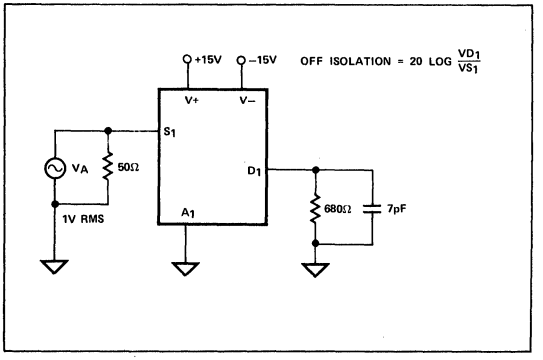
1. The conditions listed specify the worst case leakage currents. The leakage currents apply equally to source (S) or drain (D).

AC TEST CIRCUITS

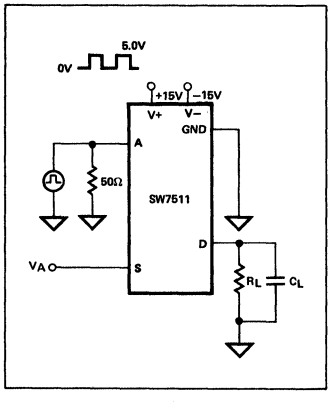
CROSSTALK MEASUREMENT CIRCUIT



ISOLATION MEASUREMENT CIRCUIT

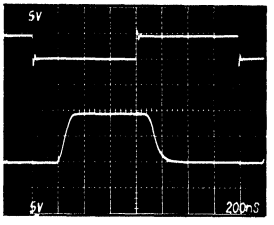


SWITCHING TIME TEST CIRCUIT



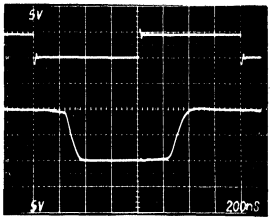
TYPICAL PERFORMANCE CHARACTERISTICS

LARGE SIGNAL SWITCHING



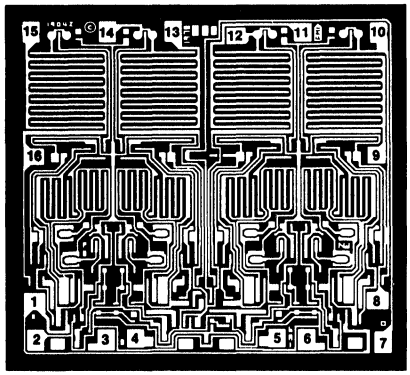
$V_A = +10V$, $R_L = 1k\Omega$, $C_L = 13pF$

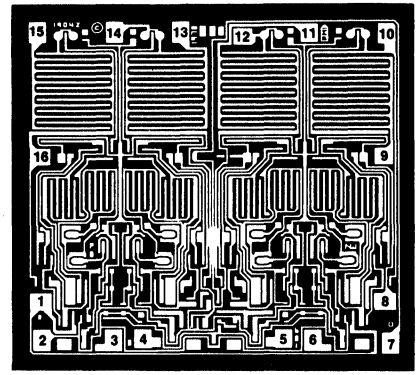
LARGE SIGNAL SWITCHING



$V_A = -10V$, $R_L = 1k\Omega$, $C_L = 100pF$

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)





DIE SIZE 0.091 x 0.083 inch

SW-7510 (SWITCH ON FOR ADDRESS HIGH)

1. NEGATIVE SUPPLY
2. GROUND
3. SWITCH (1) ADDRESS (A1)
4. SWITCH (2) ADDRESS (A2)
5. SWITCH (3) ADDRESS (A3)
6. SWITCH (4) ADDRESS (A4)
7. DISABLE
8. POSITIVE SUPPLY
9. SWITCH (4) DRAIN (D4)
10. SWITCH (4) SOURCE (S4)
11. SWITCH (3) DRAIN (D3)
12. SWITCH (3) SOURCE (S3)
13. SWITCH (2) DRAIN (D2)
14. SWITCH (2) SOURCE (S2)
15. SWITCH (1) DRAIN (D1)
16. SWITCH (1) SOURCE (S1)

SW-7511 (SWITCH ON FOR ADDRESS LOW)

1. NEGATIVE SUPPLY
2. GROUND
3. SWITCH (1) ADDRESS (A1)
4. SWITCH (2) ADDRESS (A2)
5. SWITCH (3) ADDRESS (A3)
6. SWITCH (4) ADDRESS (A4)
7. DISABLE
8. POSITIVE SUPPLY
9. SWITCH (4) DRAIN (D4)
10. SWITCH (4) SOURCE (S4)
11. SWITCH (3) DRAIN (D3)
12. SWITCH (3) SOURCE (S3)
13. SWITCH (2) DRAIN (D2)
14. SWITCH (2) SOURCE (S2)
15. SWITCH (1) DRAIN (D1)
16. SWITCH (1) SOURCE (S1)

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at 25° C for V+ = +15V, V− = −15V and T_A = 25° C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW7510/7511N LIMIT	SW7510/7511G LIMIT	UNITS
"ON" Resistance	R_{ON}	V_D = 0V, I_{DS} = 1mA	75	100	Ω MAX
Logic "1" Voltage	V_{INH}		2.0	2.0	V MIN
Logic "0" Voltage	V_{INL}		0.8	0.8	V MAX
Logic "0" Current	I_{INL}	V_{IN} = +0.4V	3.5	3.5	μA MAX
Positive Supply Current	I+	Logic Inputs at "0"	7.5	7.5	mA MAX
Negative Supply Current	I−	Logic Inputs at "0"	4.0	4.0	mA MAX

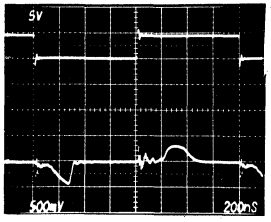
TYPICAL ELECTRICAL CHARACTERISTICS at V+ = +15V, V− = −15V and T_A = 25° C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW7510/7511N TYP	SW7510/7511G TYP	UNITS
"ON" Resistance	R_{ON}	V_D = 0V, I_{DS} = 1mA, −55° C ≤ T_A ≤ +125° C	100	150	Ω
R_{ON} vs. Temperature	R_{ON} Drift	V_D = 0V, I_{DS} = 1mA	0.4	0.5	%/° C
"ON" Switching Time	t_{ON}	V_S = −5V, R_L = 1kΩ, C_L = 7pF	600	1000	ns
"OFF" Switching Time	t_{OFF}		500	750	ns

NOTE:
The minimum logic input voltage may be as much as 2V below the GND pad; however, it may not be lower than the V- pad. The maximum logic input voltage may be as much as 36V above V- pad.

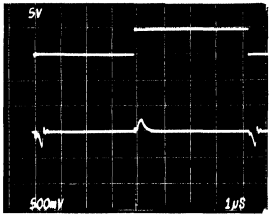
TYPICAL PERFORMANCE CHARACTERISTICS (Apply to all models, unless otherwise noted)

SMALL SIGNAL SWITCHING



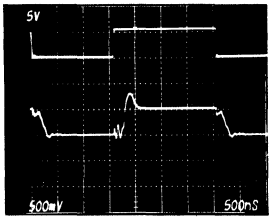
V_A = OV, R_L = 1kΩ, C_L = 13pF

SMALL SIGNAL SWITCHING WITH FILTERING



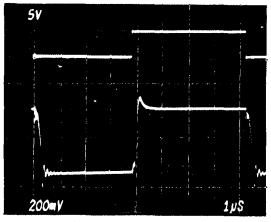
V_A = OV, R_L = 1kΩ, C_L = 13pF

SMALL SIGNAL SWITCHING



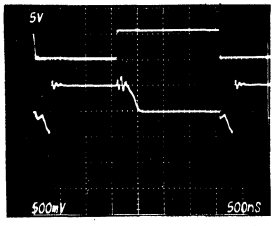
V_A = −500mV, R_L = 1kΩ, C_L = 13pF

SMALL SIGNAL SWITCHING WITH FILTERING



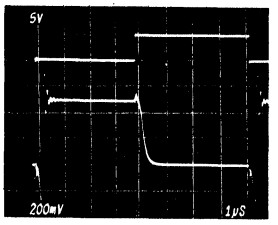
V_A = −500mV, R_L = 1kΩ, C_L = 100pF

SMALL SIGNAL SWITCHING



V_A = 500mV, R_L = 1kΩ, C_L = 13pF

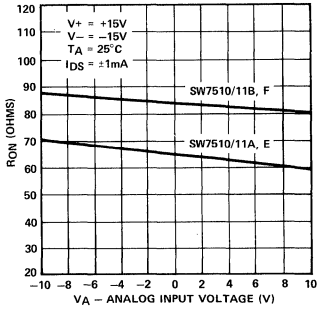
SMALL SIGNAL SWITCHING WITH FILTERING



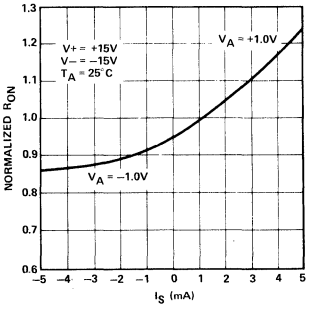
V_A = 500mV, R_L = 1kΩ, C_L = 100pF

CHARACTERISTIC CURVES

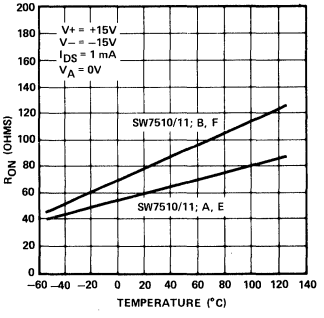
"ON" RESISTANCE (R_{ON}) vs ANALOG VOLTAGE (V_A)



NORMALIZED R_{ON} vs SWITCH CURRENT (I_S)

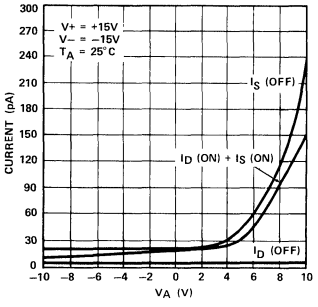


R_{ON} vs TEMPERATURE

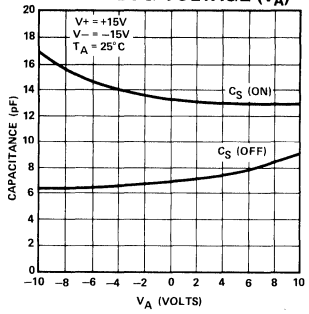


CHARACTERISTICS CURVES (Apply to all models, unless otherwise noted)

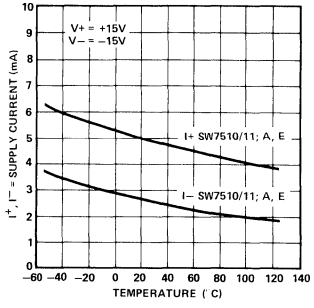
SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE



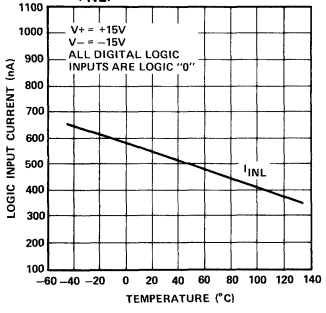
SWITCH CAPACITANCES vs ANALOG VOLTAGE (V_A)



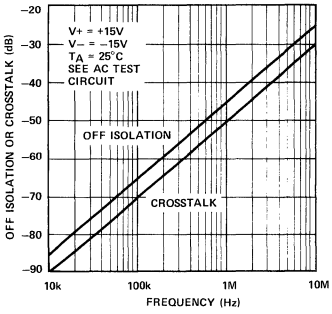
SUPPLY CURRENTS vs TEMPERATURE



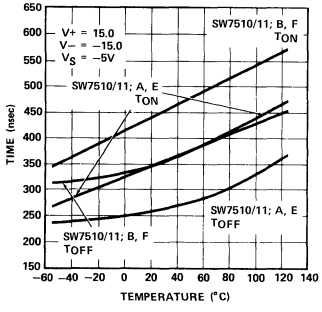
DIGITAL INPUT BIAS CURRENT (I_{NL}) vs TEMPERATURE



CROSSTALK AND "OFF" ISOLATION vs FREQUENCY



SWITCHING TIMES vs TEMPERATURE



APPLICATIONS INFORMATION

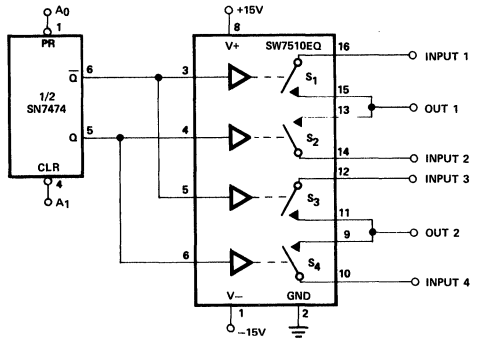
This analog switch employs ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with BIFET processing, special handling, as required with CMOS, is not necessary to prevent damage to these switches. Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pullup resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS switches. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above ≈ 1.4V.

The "ON" resistance, R_{ON}, of the analog switches is constant over the wide input voltage range of −15V to +11V with $V_{SUPPLY} = \pm 15V$. Higher input voltage is tolerable provided that some form of current limiting is employed (such as that of an op-amp output stage) to avoid exceeding junction temperature and power dissipation requirements. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF switch remains greater than its V_p, and prevents that channel from being falsely turned ON. Individual switches are "ON" without power applied.

Proper switching requires the "Source" terminal be connected to the input driving signal.

TYPICAL APPLICATIONS

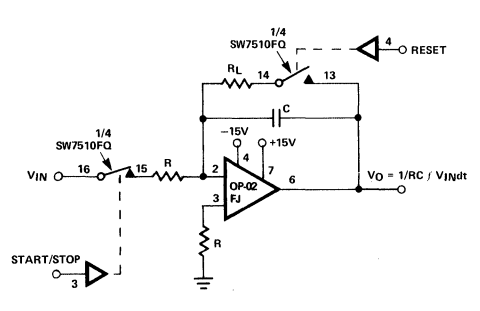
LATCHING DPDT SWITCH



Truth Table

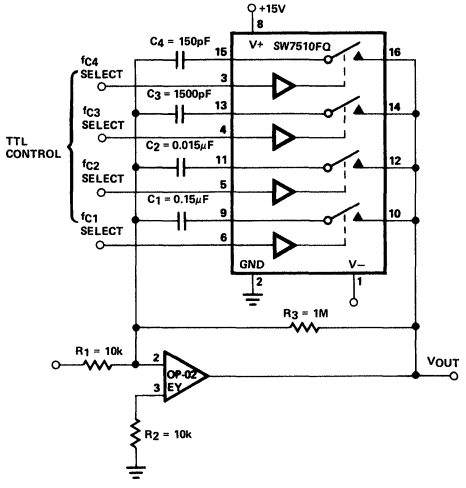
Command		State of Switches After Command	
A_0	A_1	S2 and S3	S1 and S3
1	1	same	same
0	1	on	off
1	0	off	on
0	0	INDETERMINATE	

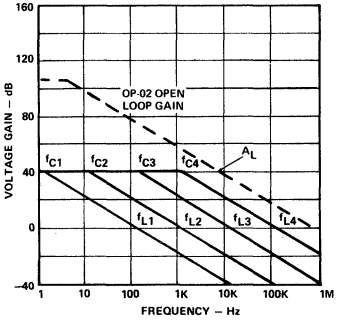
INTEGRATOR WITH ANALOG RESET AND START/STOP CAPABILITY



NOTE: Applications show SW7510. For SW7511 applications the logic is inverted.

ACTIVE LOW-PASS FILTER WITH DIGITALLY SELECTED BREAK FREQUENCY





A_L (VOLTAGE GAIN BELOW BREAK FREQUENCY) =

$$\frac{R_3}{R_1} = 100\ (40dB)$$

f_c (BREAK FREQUENCY) = $\dfrac{1}{2\pi R_3 C_X}$

f_L (UNITY GAIN FREQUENCY) = $\dfrac{1}{2\pi R_1 C_X}$

SECTION 12

SAMPLE AND HOLD AMPLIFIERS

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SAMPLE AND HOLD AMPLIFIERS

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INTRODUCTION

Sample-and-hold amplifiers "Sample" an analog input signal and then "Hold" the instantaneous input value upon the command of a logic control signal. Basically the sample-and-hold is an "analog memory" where an external capacitor serves as the storage element. Applications in which a time varying input cannot be tolerated require sample-and-hold circuits. A fast successive-approximation analog-to-digital converter is one application. Data acquisition, data distribution, analog delay and telephony requirements dictate the use of sample-hold circuits to "freeze" the analog signal for further signal processing.

A sample-and-hold circuit is conceptually an amplifier, switch, and capacitor. Many specifications are similar to those of switches and operational amplifiers — bias currents, voltage gain, and charge injection are examples. These and other specifications pertaining uniquely to sample-and-hold circuits are defined below.

The SMP-10 and SMP-11 are precision sample-and-hold amplifiers with high accuracy, low droop rate, and fast signal acquisition time. These circuits contain a high input impedance input buffer amplifier, a diode bridge sample hold switch, a transconductance or "Super-Charger" circuit to enhance slewing and a high speed output amplifier. The "Super-Charger" is capable of supplementing the diode bridge capacitor charging current whenever the difference between input and output levels exceeds a given threshold. Settling to final value is under control of currents from the diode bridge, thus minimizing the chances of overshoot and instability. The low zero scale error is achieved by precision current matching techniques employed in the biasing of both input and output amplifiers and the diode bridge. The inherent low offset voltage errors and low charge injection made possible by precise circuit design and layout allows the residual zero scale errors to be actively trimmed using PMI's "Zener Zapping" technology without degrading temperature performance. "Super Beta" transistors made possible by ion implant processing create the high input impedance amplifiers needed for low droop rate and minimal signal loading.

The SMP-10 and SMP-11 differ from each other in droop rate and settling time in the hold mode.

In addition to Precision Sample and Hold Amplifiers, two products with related capabilities are also available. The GAP-01 General Purpose Analog Processor provides the user with two independent switched transconductance amplifiers, a unity gain buffer and an uncommitted voltage comparator. This is a non-dedicated functional block which has a wide variety of applications. The second device is the PKD-01 Monolithic Peak Detector. This device performs the peak detector function with accuracies approaching those obtainable with high cost hybrid modules at a cost approaching the low cost, low performance discrete designs.

DEFINITIONS OF TERMS

ACQUISITION TIME

The minimum time for the output voltage to begin tracking the input voltage, to within a specified error band, after the inception of the sample command. By convention, acquisition time is defined for sampling of a DC level. For instance a circuit which is "holding" a 10V output signal, and operating with zero input volts, is switched to the sample mode. The acquisition time is then the time required for the output to decrease to within a ±10mV band about ground potential.

APERTURE TIME

The time between the inception of the hold command and the time the circuit output ceases tracking the input signal. When the holding capacitor charging current is less than 0.3mA the aperture time is nominally 50ns. The aperture time is a function of the holding capacitor charging current I_{CH}. The changing current is in turn a function of the rate of change of the input signal voltage. This relationship holds true up to a maximum of 50mA which is the maximum current available from the SMP-11 to charge holding capacitor C_H. Charging current can be calculated from the rate of change of the input analog signal and the size of C_H by the equation:

$$I_{CH} = C_H \frac{dv}{dt} \quad (I_{CH} = 50mA \text{ Max.})$$

CHANGE IN HOLD STEP

Actual hold step less the hold step measured after sampling V = 0. A change in hold step has two components: the first is a function of input voltage, the second is a function of the rise time of the S/H voltage. Note that rise time of S/H voltage also effects ZERO-SCALE-ERROR.

CHARGE TRANSFER

The amount of charge transferred to the holding capacitor due to the action of the switch. Charge is transferred to C_H when the circuit is switched to the hold mode. Charge transfer causes a change in output voltage ΔV_{ZS} as defined by the equation:

$$\Delta V_{ZS}(V) = \frac{Q_t(pC)}{C_H\,(pF)}$$

Note that for $Q_t = 5pC$ and $C_H = 5000pF$ offset error = 1mV. The SMP-11 has been factory nulled for $C_H = 5000pF$. For other values of C_H the zero scale shift can be calculated from the equation:

$$\Delta V_{ZS}(V) = \frac{Q_t}{C_H} - 1mV$$

DROOP RATE

Droop rate dVd/dt is the rate of change of output voltage while the circuit is operated in the hold mode. dVd/dt is a direct function of droop current I_{DR} and related by the equation:

$$\frac{dV_d}{dt} = \frac{I_{DR}}{C_H} \times 10^6$$

where dVd/dt is expressed in μV/ms with I_{DR} in nanoamperes and C_H in picofarads.

FEEDTHROUGH ATTENUATION RATIO

The change of voltage applied to the input as a ratio of the change of voltage observed at the output, caused by the input disturbance, while the circuit is in the hold mode.

FULL POWER BANDWIDTH

The maximum frequency at which rated output voltage E_{or} can be supplied without significant distortion. Full power bandwidth F_p is related to slew rate SR by the following equation:

$$F_p = \frac{SR}{2\pi E_{or}}$$

Using this equation F_p of 160kHz can be computed. This is applicable only for pulsed conditions. Power dissipation limits F_p to 100kHz for C.W. operation.

GAIN ERROR

Voltage difference between input and output voltage minus the output voltage measured over specified range.

HOLD CAPACITOR CHARGING CURRENT

The current I_{CH} which charges, or discharges, the capacitor while the circuit is in the sample mode.

HOLD MODE SETTLING TIME

The time for all transients to settle within a specified error band. Measured from the inception of the hold command.

HOLD STEP

Magnitude of step caused in the output voltage by switching the circuit from sample mode to hold mode.

INPUT BIAS CURRENT

The current into the input terminal with input voltage held at zero volts.

INPUT RESISTANCE

The ratio of the AC change in the input current as a result of the change in the input voltage.

LEAKAGE (DROOP) CURRENT

The current which flows out of holding capacitor C_H while the circuit is operating in the hold mode. In general droop current I_{DR} is defined positive when its direction is *into* the C_H pin.

OUTPUT RESISTANCE

An AC change in output voltage as a result of an AC change in load current.

POWER SUPPLY REJECTION RATIO

The change in output voltage for a change in power supply voltage when the circuit is maintained in the sample mode. The best power supply rejection ratio PSRR is obtained with the power supply voltage changing at a very low rate (DC). For essentially DC conditions PSRR for the hold mode of operation is essentially the same as the PSRR for the

sample mode. PSRR is degraded as the frequency of the disturbance increases. PSRR for both sample and hold modes is shown graphically as a function of frequency.

SAMPLE/HOLD CURRENT RATIO

The ratio of the peak charging current available to the droop current.

SIGNAL TRANSFER NONLINEARITY

The total input to output, nonadjustable, hold mode error caused by gain nonlinearity, feedthrough, thermal transient, charge transfer and droop rate. These error terms cannot be corrected by offset and gain adjustments. Signal transfer nonlinearity is tested for a specified holding capacitor, input voltage change and hold period.

SLEW RATE

The maximum possible rate of change of the output voltage when supplying the rated output. For a sample and hold circuit, slew rate must be defined with a specified value of holding capacitor C_H. For the SMP-11, slew rate can either be measured by operating the circuit in the sample mode and applying a step function to the input, or by applying an input voltage which differs from the output voltage, with the circuit in the hold mode, then switching to the sample mode and observing the rate of change of the output voltage.

TOTAL ERROR

The algebraic sum of the following factors:

i. ZERO-SCALE ERROR

ii. Gain Error

iii. Hold Step Change versus $\frac{dV_{(S/H)}}{dt}$

iv. Hold Step Change versus V_{IN}

VOLTAGE GAIN

The ratio of the output voltage to the input voltage with the circuit operating in the sample mode.

ZERO SCALE ERROR

The magnitude of the output voltage when the circuit is switched from sample to hold mode while holding the input at zero volts. ZERO SCALE ERROR V_{ZS} is the algebraic sum of the offset voltage and the charge transfer step voltage. V_{ZS} can be adjusted to zero (see ZERO SCALE ERROR pull adjustment).

SMP-10/SMP-11

LOW DROOP RATE/ACCURATE SAMPLE AND HOLD AMPLIFIERS

FEATURES

SMP-10

- **Low Droop Rate 5.0μV/mS**
- **Low Signal Transfer Non-Linearity 0.005%**
- **High Sample Current/Hold Ratio ..... $2x10^9$**

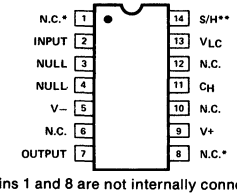
SMP-11

- **Low Droop Rate over Temperature 120μV/mS**
- **High Sample Current/Hold Ratio ..... $1.7x10^8$**

BOTH SMP-10 AND SMP-11

- **Fast Acquisition Time, 10V Step to 0.1% 3.5μS**
- **High Slew Rate 10V/μS**
- **Low Aperture Time 50nS**
- **Trimmed for Minimum Zero Scale Error 0.45mV**
- **Feedtrhough Attenuation Ratio 96dB**
- **Low Power Dissipation 160mW**
- **DTL, TTL & CMOS Compatible Logic Input**
- **HA-2420, HA-2425, DATEL, SHM-IC-1, and AD583 Socket Compatible***

PIN CONNECTIONS

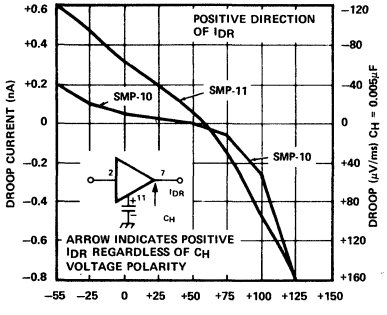


14-PIN DIP (Y-SUFFIX)

*Pins 1 and 8 are not internally connected, in unity gain applications, SMP-10 and SMP-11 can replace HA-2425, HA-2420, SHM-IC-1 and AD-583 directly.

**Sample/Hold Control (High = Hold Low = Track)

LOW DROOP RATE OVER TEMPERATURE



Manufactured under one or more of the following patents: 4,109,215; 4,142, 117.

GENERAL DESCRIPTION

The SMP-10/11 are precision sample and hold amplifiers that provide the high accuracy , the low droop rate and the fast acquisition time required in data acquisition and signal processing systems. Both devices are essentially non-inverting unity gain circuits consisting of two very high input impedance buffer amplifiers connected together by a diode bridge switch.

HIGH ACCURACY AND LOW DROOP RATE

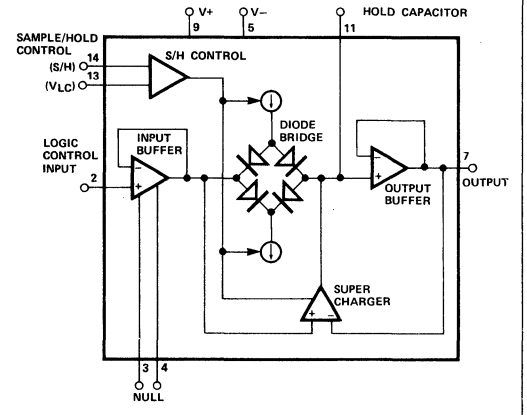
The high input impedance and the low droop rates of the SMP-10 and the SMP-11 are achieved by using bipolar darlington circuits and an ion implant process that creates "super beta" transistors.

The output buffer's input stage converts to a super beta darlington configuration during the hold mode, which results in a very low droop rate with no penalty in acquisition time. The use of bipolar transistors achieves a low change in droop rate over the operating temperature range.

FAST ACQUISITION

A unique super charger provides up to 50mA of charging current to the hold capacitor, which results in smooth, fast charging with minimum noise. As the hold capacitor voltage nears its final value, the low current diode bridge controls the final settling time. This unique combination of linear functions in a monolithic circuit enables the system designer to achieve superior performance.

FUNCTIONAL DIAGRAM



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $T_A = 25°C$, device fully warmed up, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		SMP-10A/E SMP-11A/E MIN	TYP	MAX	SMP-10B/F SMP-11B/F MIN	TYP	MAX	SMP-11G MIN	TYP	MAX	UNITS
Zero Scale Error (Hold Mode)	V_{ZS}	$V_{IN} = 0$, $V_{LOG} = 3.5V$		—	0.45	1.5	—	0.60	3.0	—	1.5	7.0	mV
Input Bias Current	I_B	$V_{IN} = 0$		—	25	50	—	30	90	—	40	160	nA
Leakage (Droop) Current	I_{DR}	Device Warmed Up	SMP-10	—	—	0.10	—	—	0.25	—	—	—	nA
			SMP-11	—	—	1.00	—	—	2.50	—	—	4.5	
Droop Rate	dV_{CH}/dt	Device Warmed Up	SMP-10	—	5	20	—	5	50	—	—	—	μV/ms
			SMP-11	—	60	200	—	70	500	—	80	900	
Input Resistance	R_{IN}	See Note 1		3×10^{10}	6×10^{10}	—	1.5×10^{10}	5×10^{10}	—	—	4×10^{10}	—	Ω
Voltage Gain	A_V	Sample Mode $V_{IN} = \pm 10V$, $R_L = 5k\Omega$ or $V_{IN} = \pm 5V$, $R_L = 2.5k\Omega$		0.99963	0.99983	—	0.99953	0.99978	—	0.99940	0.99975	—	V/V
Acquisition Time		10V step to within 10mV of final value (0.1%)		—	3.5	—	—	3.5	—	—	3.5	—	μs
		10V step to within 1.0mV of final value (0.01%)		—	5.0	—	—	5.0	—	—	5.0	—	μs
Aperture Time	t_a			—	50	—	—	50	—	—	50	—	ns
Hold Mode Settling Time	t_{Hm}	Settling to 1mV of final value.	SMP-10	—	7	—	—	7	—	—	—	—	μs
			SMP-11	—	1.5	—	—	1.5	—	—	1.5	—	
Charge Transfer	Qt	$V_{IN} = 0$, $V_{LOG} = 3.5V$		—	5	—	—	5	—	—	5	—	pC
Slew Rate	SR	$V_{IN} = \pm 10V$, $R_L = 2.5k\Omega$		—	10	—	—	10	—	—	10	—	V/μs
Hold Capacitor Charging Current	I_{CH}	$V_{IN} - V_{OUT} \geq \pm 3V$		30	50	—	20	50	—	—	50	—	mA
Sample/Hold Current Ratio	I_{CH}/I_{DR}		SMP-10	3×10^8	2×10^9	—	8×10^7	8×10^8	—	—	—	—	mA/mA
			SMP-11	—	1.7×10^8	—	—	1.5×10^8	—	—	1.5×10^8	—	
Feedthrough Attenuation Ratio		Input = $20V_{p-p}$ 1kHz Note 1		86	96	—	80	90	—	—	90	—	dB
Full Power Bandwidth	F_p	$\pm 10V_{p-p}$ (Dissipation Limited)		—	100	—	—	100	—	—	100	—	kHz
Input Voltage Range and/or Output Voltage Swing		$R_L = 2.5k\Omega$		±11	±11.5	—	±10.5	±11.5	—	±10.5	±11.5	—	—
Output Resistance	R_O			—	0.15	—	—	0.15	—	—	0.15	—	Ω
Power Supply Rejection Ratio	PSRR	Sample Mode $V_S = \pm 9V$ to $\pm 18V$		82	92	—	77	92	—	72	92	—	dB
Power Consumption (DC)	P_D	Sample Mode $V_{IN} = 0$		—	160	180	—	170	210	—	180	240	mW

SMP-10 ONLY

PARAMETER	SYMBOL	CONDITIONS	SMP-10A/E MIN	TYP	MAX	SMP-10B/F MIN	TYP	MAX	UNITS
Hold Step		$V_{IN} = 0$, Sample Time = 10μs	−1.0	+1.5	+4.0	−3.0	+1.5	+6.0	mV
Signal Transfer Nonlinearity		±10V Input, $R_L = 5K$, Sample Time = 10μs, Hold Time = 1ms (See Note)	—	0.005	0.010	—	0.007	0.015	% of 20V
Output Noise		Wideband Noise 100Hz to 100kHz Sample Mode	—	40	—	—	50	—	μV RMS
Hold Mode Settling Time		Settling to 1.0mV of Final Value, $V_{IN} = 0V$	—	7.0	—	—	7.0	—	μs

NOTES:

1. Guaranteed by design.
2. These measurements are made with the devices warmed up. It can be seen that there is a selection trade off between Droop Rate and Hold Mode settling time.

ABSOLUTE MAXIMUM RATINGS (Note)

Supply Voltage (V+ minus V−) 36V
Power Dissipation 500mW
Input Voltage ..... Equal to Supply Voltage
Logic and Logic Reference
Voltage ..... Equal to Supply Voltage
Output Short Circuit Duration ..... Indefinite
Hold Capacitor Short Circuit Duration ..... 60 sec
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering 60 sec) ..... 300°C

Operating Temperature Range
SMP-10AY, BY ..... −55°C to +125°C
SMP-10EY, FY ..... 0°C to +70°C
SMP-11AY, BY ..... −55°C to 125°C
SMP-11EY, FY, GY ..... 0°C to 70°C
DICE Junction Temperature (T_j) ..... −65°C to +150°C

NOTE: Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground. $0°C \leq T_A \leq +70°C$, device fully warmed up, unless otherwise noted.

			SMP-10E SMP-11E			SMP-10F SMP-11F			SMP-11G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Zero Scale Error	V_{ZS}	$V_{IN} = 0$, $V_{LOG} = 3.5V$	—	0.75	2.0	—	1.0	4.0	—	2.7	10	mV
Input Bias Current	I_B	$V_{IN} = 0V$	—	35	75	—	40	140	—	50	250	nA
Leakage (Droop) Current	I_{DR}	Device Warmed Up SMP-10	—	0.05	0.25	—	0.080	0.65	—	—	—	nA
		See Note 2 SMP-11	—	0.5	1.8	—	0.6	2.8	—	0.7	5	
Droop Rate	dV_{CH}/dt	Device Warmed Up SMP-10	—	10	50	—	16	130	—	—	—	μV/ms
		See Note 2 SMP-11	—	100	360	—	120	560	—	140	1000	
Voltage Gain	A_V	Sample Mode $V_{IN} = \pm 10V$, $R_L = 5k\Omega$ or $V_{IN} = \pm 5V$, $R_L = 2.5k\Omega$	0.99955	0.99976	—	0.99950	0.99972	—	0.99930	0.99970	—	V/V
Power Supply Rejection Ratio	PSRR	Sample Mode $V_S = \pm 9V$ to $\pm 18V$	80	90	—	75	80	—	70	90	—	dB
Logic Control Input Current	I_{LC}	$V_{LC} = 0V$	—	−1	−2	—	−1	−3	—	−1	−4	μA
Logic Input	$I_{S/H}$	Sample Mode $V_{S/H} = 0.5V$	—	−5	−15	—	−5	−15	—	−5	−15	μA
		Hold Mode $V_{S/H} = 5.0V$	—	0.2	—	—	0.2	—	—	0.2	—	nA
Differential Logic Threshold			0.8	1.3	2.0	0.8	1.3	2.0	0.8	1.3	2.0	V

ORDERING INFORMATION†

$T_A = +25°C$

VZS (mV)	DROOP RATE IN μV/mS	PACKAGE IS 14 PIN DIP HERMETIC	PACKAGE IS 14 PIN DIP PLASTIC	OPERATING TEMPERATURE RANGE
1.5*	20	SMP10AY	——	MIL
3.0*	50	SMP10BY	——	MIL
1.5	20	——	SMP10EP	COM
3.0	50	——	SMP10FP	COM
1.5*	200	SMP11Y	——	MIL
3.0*	500	SMP11Y	——	MIL
1.5	200	——	SMP11EP	COM
3.0	500	——	SMP11FP	COM
7.0	900	——	SMP11GP	COM

* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.
† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

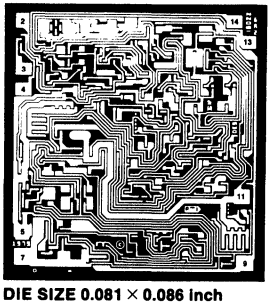
ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $-55°C \leq T_A \leq +125°C$, device fully warmed up, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		SMP-10A SMP-11A MIN	SMP-10A SMP-11A TYP	SMP-10A SMP-11A MAX	SMP-10B SMP-11B MIN	SMP-10B SMP-11B TYP	SMP-10B SMP-11B MAX	UNITS
Zero Scale Error	V_{ZS}	$V_{IN} = 0$, $V_{LOG} = 3.5V$		—	1.25	3.0	—	1.60	5.5	mV
Input Bias Current	I_B	$V_{IN} = 0V$		—	60	150	—	70	280	nA
Leakage (Droop) Current	I_{DR}	$T_A = -55°C$	SMP-10	—	0.050	0.50	—	0.080	1.22	nA
		$T_A = +125°C$	SMP-10	—	0.60	1.50	—	0.90	4.00	
		T_A = Full Range See Note 2	SMP-11	—	0.60	4.0	—	0.90	10.0	
Droop Rate	dV_{CH}/dt	$T_A = -55°C$	SMP-10	—	10	100	—	16	250	μV/ms
		$T_A = +125°C$	SMP-10	—	120	300	—	180	800	
		T_A = Full Range See Note 2	SMP-11	—	120	800	—	180	2000	
Voltage Gain	A_V	Sample Mode $V_{IN} = \pm 10V$, $R_L = 5k\Omega$ or $V_{IN} = \pm 5V$, $R_L = 2.5k\Omega$		0.99950	0.99972	—	0.99940	0.99968	—	V/V
Power Supply Rejection Ratio	PSRR	Sample Mode $V_S = \pm 9V$ to $\pm 18V$		78	88	—	72	90	—	dB
Logic Control Input Current	I_{LC}	$V_{LC} = 0V$		—	−1	−3	—	−1	−5	μA
Logic Input	$I_{S/H}$	Sample Mode $V_{S/H} = 0.6V$		—	−5	−15	—	−5	−15	μA
		Hold Mode $V_{S/H} = 5.0V$		—	0.2	—	—	0.2	—	nA
Differential Logic Threshold				0.8	1.3	2.0	0.8	1.3	2.0	V

NOTES:

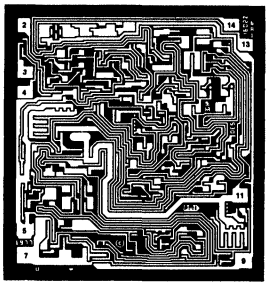
1. Guaranteed by design.
2. These measurements are made with the devices warmed up. It can be seen that there is a selection trade off between Droop Rate and Hold Mode settling time.

DICE CHARACTERISTICS



DIE SIZE 0.081 × 0.086 inch

2. INPUT
3. NULL
4. NULL
5. NEGATIVE SUPPLY
7. OUTPUT
9. POSITIVE SUPPLY
11. HOLD CAPACITOR (C_H)
13. LOGIC THRESHOLD CONTROL (V_{LC})
14. SAMPLE/HOLD COMMAND



DIE SIZE 0.081 × 0.086 inch

2. INPUT
3. NULL
4. NULL
5. NEGATIVE SUPPLY
7. OUTPUT
9. POSITIVE SUPPLY
11. HOLD CAPACITOR (C_H)
13. LOGIC THRESHOLD CONTROL (V_{LC})
14. SAMPLE/HOLD COMMAND

Refer to Section 2 for additional DICE information

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $T_A = 25°C$, device fully warmed up, unless otherwise noted.

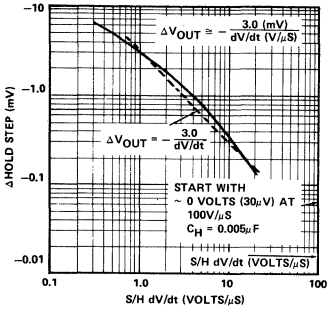
PARAMETER	SYMBOL	CONDITIONS	SMP-10N SMP-11N LIMIT	SMP-10G SMP-11G LIMIT	UNITS
Zero Scale Error	V_{ZS}	$V_{IN} = 0$, $V_{LOG} = 3.5V$ Hold Mode	1.5	3.0	mV MAX
Input Bias Current	I_B	$V_{IN} = 0V$	50	90	nA MAX
Leakage (Droop) Current	I_{DR}	Device Warmed Up SMP-10	0.10	0.25	nA MAX
		Device Warmed Up SMP-11	1	2.5	
Droop Rate	I_{DR}	Device Warmed Up SMP-10	20	50	μV/ms MAX
		Device Warmed Up SMP-11	200	500	
Voltage Gain	A_V	Sample Mode $V_{IN} = \pm 10V$ or $V_{IN} = \pm 5V$	0.99963	0.99953	V/V MIN
Hold Capacitor Charging Current	I_{CH}	$V_{IN} - V_{OUT} \geq \pm 3V$	30	20	mA MIN
Input Voltage Range and/or Output Voltage Swing		$R_L = 2.5k\Omega$	±11	±10.5	V MIN
Power Supply Rejection Ratio	PSRR	Sample Mode $V_S = \pm 9V$ to $\pm 18V$	82	77	dB MIN
Power Consumption	P_D	Sample Mode $V_{IN} = 0$	180	210	mW MAX
Logic Reference Input Current			−2	−3	μA MAX
Logic Input	$I_{S/H}$	Sample Mode $V_{S/H} = 0.6V$	−15	−15	μA MAX
		Hold Mode $V_{S/H} = 5V$	0	0	nA MAX
Differential Logic Threshold		$V_{LC} = 0$	2.0	2.0	V MAX
			0.8	0.8	V MIN

TYPICAL ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $T_A = 25°C$, device fully warmed up, unless otherwise noted.

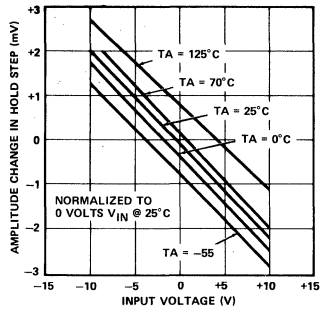
PARAMETER	SYMBOL	CONDITIONS	SMP-10N SMP-11N TYP	SMP-10G SMP-11G TYP	UNITS
Acquisition Time		10V step to 0.1% of final value	3.5	3.5	μs
Aperture Time	t_a		50	50	ns
Charge Transfer	Q_t	$V_{IN} = 0$, $V_{LOG} = 3.5V$	5	5	pC
Slew Rate	SR	$V_{IN} = \pm 10V$, $R_L = 2k\Omega$	10	10	V/μs

TYPICAL PERFORMANCE CURVES

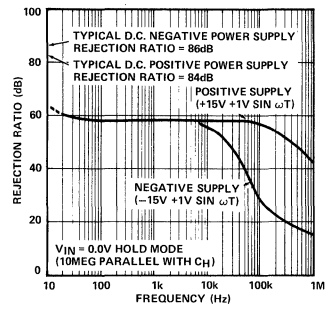
CHANGE IN HOLD STEP vs S/H $\frac{dV}{dt}$



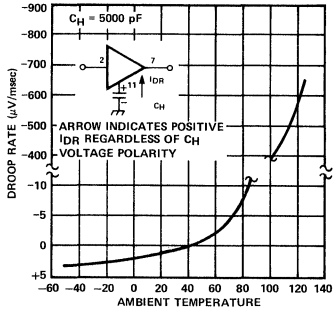
AMPLITUDE CHANGE IN HOLD STEP vs INPUT VOLTAGE



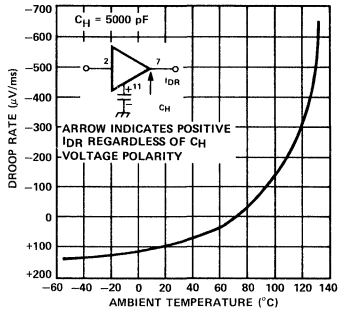
HOLD MODE POWER SUPPLY REJECTION



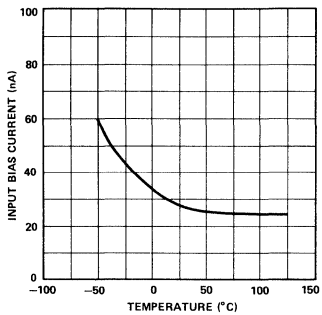
SMP-10 DROOP RATE vs TEMPERATURE



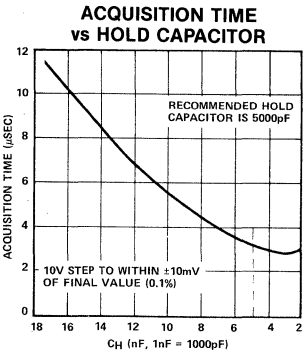
SMP-11 DROOP RATE vs TEMPERATURE



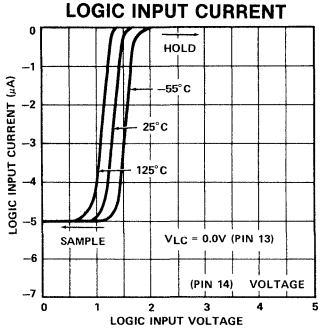
INPUT BIAS CURRENT vs TEMPERATURE



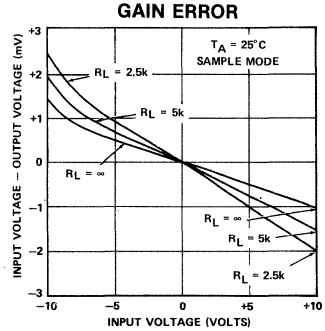
ACQUISITION TIME vs HOLD CAPACITOR



LOGIC INPUT CURRENT

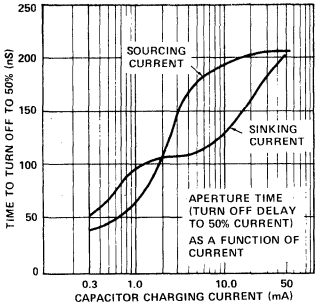


GAIN ERROR

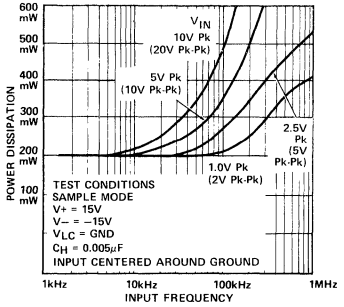


TYPICAL PERFORMANCE CURVES

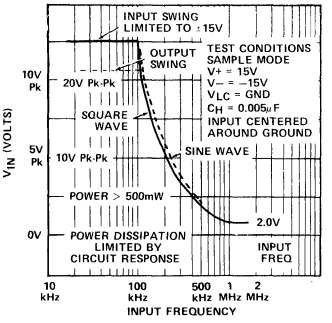
APERTURE TIME vs CAPACITOR CHARGING CURRENT DURING SAMPLING



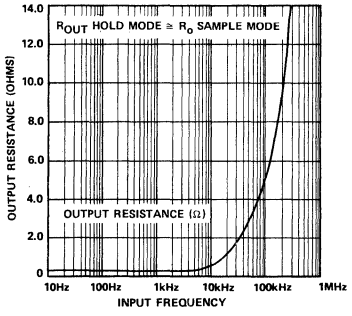
POWER DISSIPATION vs FREQUENCY INPUT = V_{pk} Sin ωt



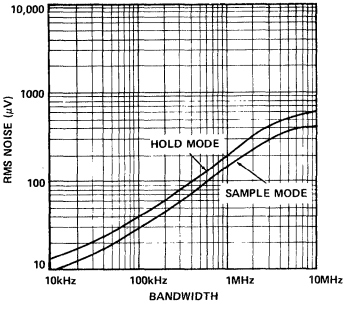
MAXIMUM INPUT SIGNAL AMPLITUDE vs FREQUENCY



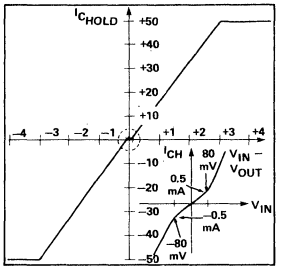
OUTPUT RESISTANCE vs FREQUENCY



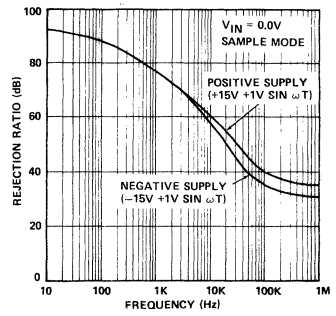
OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



HOLD CAPACITOR CHARGING CURRENT vs INPUT OUTPUT VOLTAGE

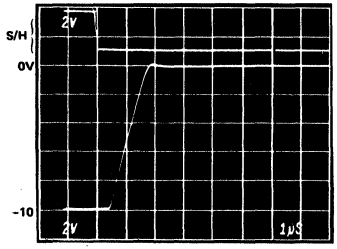


SAMPLE MODE POWER SUPPLY REJECTION

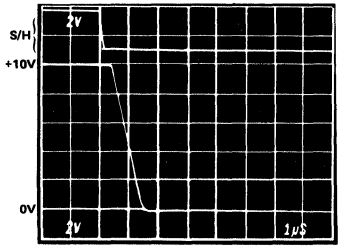


SMP-10/SMP-11 ACQUISITION TIMES

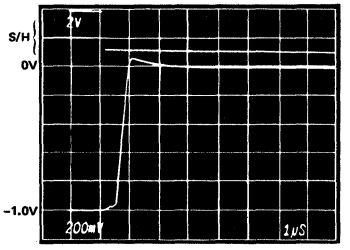
ACQUISITION TIME
−10V to 0V



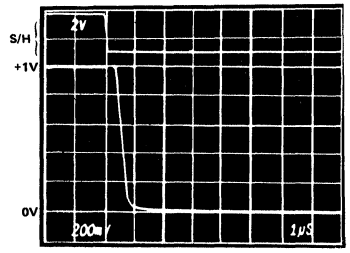
ACQUISITION TIME
+10V to 0V



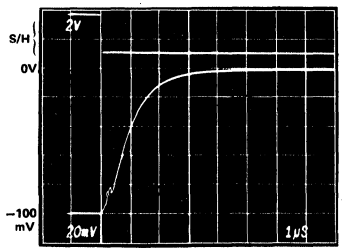
ACQUISITION TIME
−1.0V to 0V



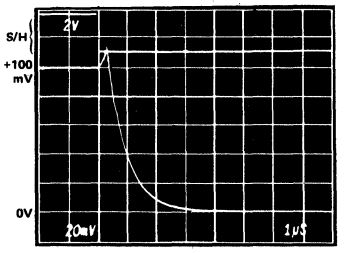
ACQUISITION TIME
+1.0V to 0V

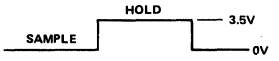


ACQUISITION TIME
−100mV to 0V



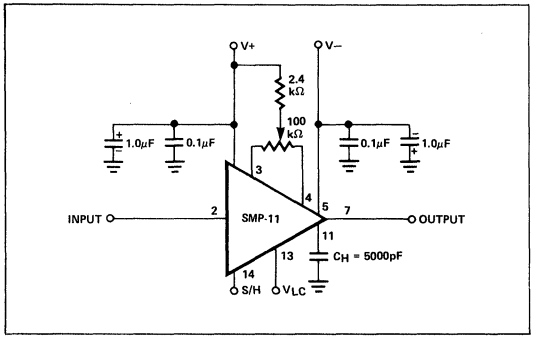
ACQUISITION TIME
+100mV to 0V





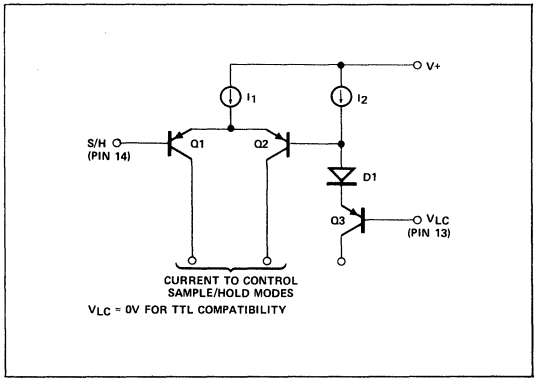
APPLICATIONS INFORMATION

ZERO SCALE NULL ADJUSTMENT



During the null adjustment, the amplifier should be switched continuously between the "sample" and "hold" mode. The error should be adjusted to read zero when the unit is in the "hold" mode. In this way, both offset voltage errors and charge transfer errors are adjusted to zero.

LOGIC CONTROL



As shown in the Figure, the sample/hold mode control is accomplished by steering the current (I_1) through Q1 or Q2, thus providing high-speed switching and a predictable logic

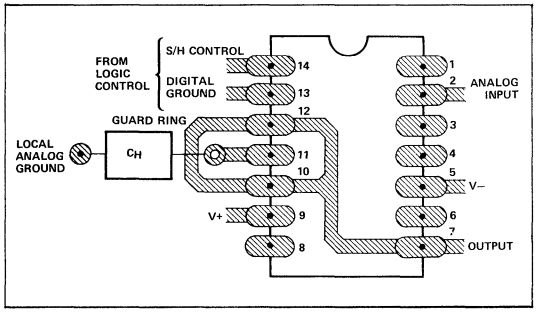
threshold. For TTL and DTL interface, simply ground V_{LC} (Pin 13). For CMOS, HTL and HNIL interface, the appropriate threshold voltage, allowing for 2 diode drops for D1 and V_{BE} of Q3, should be applied to V_{LC}.

For proper operation, the V_{LC} (logic control) must always be at least 3.5V below the positive supply and 2.0V above the negative supply.

Sample and hold control voltage (S/H) must always be at least 2.8V above the negative supply.

GUARDING AND GROUNDING LAYOUT

The use of a ground plane is strongly recommended to minimize ground path resistances. Separate analog and digital grounds should be used, and it is advisable to keep these two ground systems isolated until they are tied back to the common system ground. Digital currents should not flow back to the system ground through the analog ground path.



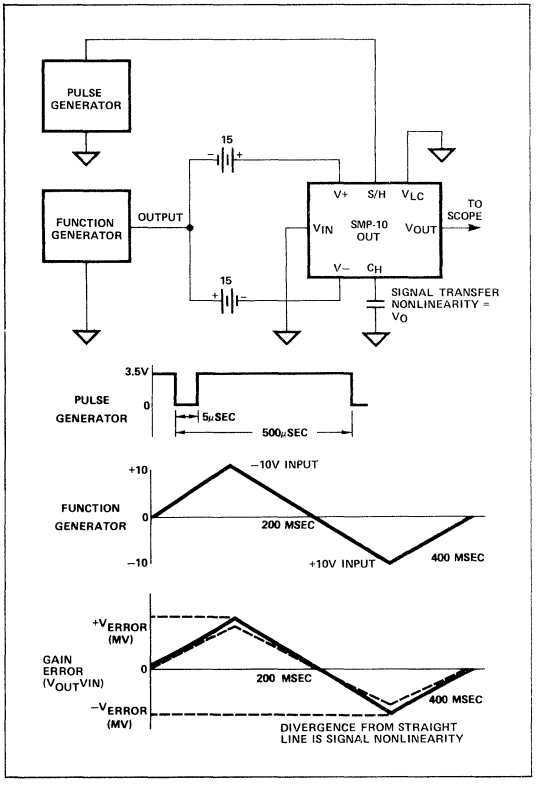
HOLD CAPACITOR RECOMMENDATIONS

The hold capacitor (C_H) acts as a memory element and also as a compensating capacitor for the sample and hold amplifier. For stable operation, a minimum value of 2000pF is recommended, with no limit set for the maximum value. The devices have been internally trimmed for $C_H = 5000$ pF. Other values of C_H will cause a zero scale shift, which can be calculated from the following equation:

$$\Delta V_{ZS}(mV) = \frac{5\ (pC) \times 10^3}{C_H\ (pF)} - 1$$

The hold capacitor should have very high insulation resistance and low dielectric absorption. For temperatures below 85°C, polystyrene capacitors are recommended, while teflon capacitors are recomended for higher temperature applications.

SIGNAL TRANSFER NONLINEARITY TEST CIRCUIT



GAP-01

ANALOG SIGNAL PROCESSING SUBSYSTEM

FEATURES

- **Low Zero Scale Error** **3.0mV**
- **Low Droop Rate** **0.1mV/ms**
- **Wide Bandwidth** **400kHz**
- **Digitally Selected Signal Path**
- **Uncommitted Comparator On Chip**
- **Wide Application Versatility**
  - **Synchronous Demodulator**
  - **Absolute Value Amplifier**
  - **Two-Channel S/H Amplifier**
  - **Two-Channel Multiplexer with Gain**

GENERAL DESCRIPTION

Designed as a general-purpose analog processing subsystem, the GAP-01 combines many commonly used system building blocks within a single integrated circuit. Being a monolithic design, the GAP-01 offers significant performance and package density advantages over discrete designs without sacrificing system versatility.

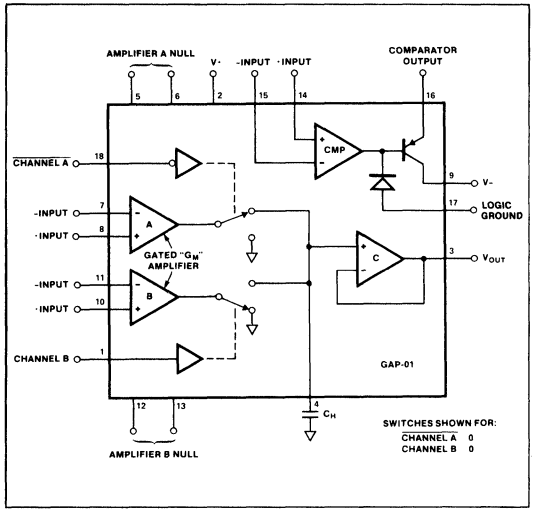
The basic circuit versatility stems from the GAP-01's architecture. The circuit features two differential input transconductance amplifiers, two low-glitch current mode switches, an output voltage buffer amplifier and a precision comparator.

Both transconductance input amplifier outputs are switched by current mode switches into the voltage follower output stage, thus providing two digitally selectable signal paths through the device. Gain through the two channels may be different in both sign and magnitude with proper feedback selection. An external capacitor provides loop compensation and doubles as a hold or "memory" capacitor when the GAP-01 functions as a dual-channel sample/hold amplifier. Offset voltage and charge transfer errors are actively trimmed by using the "Zener Zap" trim technique. The output buffer features an FET input stage to reduce droop rate error in S/H applications. A bias current cancellation circuit minimizes droop error at high ambient temperature.

The inclusion of a precision comparator on chip increases the GAP-01's versatility and cost effectiveness in non-linear or data conversion applications. The output high voltage level is set by external resistors. This scheme maximizes noise immunity and permits interface to all standard logic families — TTL, DTL, and CMOS.

Several applications exploit the ability to select the signal path through the GAP-01. As a two-channel multiplexer or analog switch, the GAP-01 high input impedance offers advantages when switching high impedance signals. Gain through the "MUX" is also possible. The GAP-01 operates as a sample/hold amplifier in the hold mode when both input amplifiers are unselected. With the on-board comparator, a two-channel successive approximation analog-to-digital conversion (ADC) system may be constructed. Combining a sign-magnitude, digital-to-analog (DAC) converter with the GAP-01 results in a four-quadrant multiplying DAC. The GAP-01 contains all the functional devices needed to perform synchronous demodulation or implement the absolute value function.

FUNCTIONAL DIAGRAM



CONTROL LOGIC

Ch A	Ch B	OUTPUT to C
0	0	Channel A
0	1	Indeterminate*
1	0	Hold Last Input
1	1	Channel B

*This condition will not damage the GAP-01. It will merely cause an unpredictable output.

Manufactured under the following patent: 4,285,051

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	GAP01A/E MIN	GAP01A/E TYP	GAP01A/E MAX	GAP01B/F MIN	GAP01B/F TYP	GAP01B/F MAX	UNITS
"g_m" AMPLIFIERS A, B									
Zero Scale Error	V_{ZS}		—	2.0	3.0	—	3.0	6.0	mV
Input Offset Voltage	V_{OS}		—	2.0	4.0	—	3.0	7.0	mV
Input Bias Current	I_B		—	80	150	—	80	250	nA
Input Offset Current	I_{OS}		—	20	40	—	50	100	nA
Voltage Gain	A_V		18	25	—	10	25	—	V/mV
Common Mode Rejection Ratio	CMRR	$10V \le V_{CM} \le +10V$	80	90	—	74	90	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \le \pm 18V$	86	96	—	76	96	—	dB
Input Voltage Range	V_{CM}	(Note 2)	±11.5	±12.0	—	±11.5	±12.0	—	V
Slew Rate	SR		—	0.5	—	—	0.5	—	V/μs
Feedthrough Error		$\Delta V_{IN} = 20V$, DET = 1, RST = 0	66	80	—	76	80	—	dB
Acquisition Time to 0.1% Accuracy	t_a	20V Step, $A_{VCL} = +1$	—	41	70	—	41	70	μs
Acquisition Time to 0.01% Accuracy	t_a	20V Step, $A_{VCL} = +1$	—	45	—	—	45	—	μs
COMPARATOR									
Input Offset Voltage	V_{OS}		—	0.5	1.5	—	1.0	3.0	mV
Input Bias Current	I_B		—	700	1000	—	700	1000	nA
Input Offset Current	I_{OS}		—	75	300	—	75	300	nA
Voltage Gain	A_V	2.0kΩ Pull-up Resistor to 5.0V (Note 2)	5	7.5	—	3.5	7.0	—	V/mV
Common Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	82	106	—	82	106	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \le \pm 18V$	76	90	—	76	90	—	dB
Input Voltage Range	V_{CM}	(Note 2)	±11.5	±12.5	—	±11.5	±12.5	—	V
Low Output Voltage	V_{OL}	$I_{sink} \le 5.0mA$, Logic GND = 0V	-0.2	0.15	0.4	-0.2	0.15	0.4	V
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	—	25	80	—	25	80	μA
Output Short Circuit Current	I_{SC}	$V_{OUT} = 5V$	7.0	12	45	7.0	12	45	mA
Response Time	t_s	5mV Overdrive, (Note 3) 2.0kΩ Pull-up Resistor to 5.0V	—	150	—	—	150	—	ns
DIGITAL INPUTS-RST, DET (See Note 3)									
Logic "1" Input Voltage	V_H		2.0	—	—	2.0	—	—	V
Logic "0" Input Voltage	V_L		—	—	0.8	—	—	0.8	V
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	—	0.02	1.0	—	0.02	1.0	μA
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	—	1.6	10	—	2.0	10	μA
MISCELLANEOUS									
Droop Rate	V_{DR}	$T_J = +25°C$ (Note 1)	—	0.02	0.07	—	—	0.1	mV/ms
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	±11.5	±12.5	—	±11.0	±12.0	—	V
Short Circuit Current: Amplifier C	I_{SC}		7.0	15	40	7.0	15	40	mA
Switch Aperture Time	t_{ap}		—	75	—	—	75—	nS	
Switch Switching Time	ts		—	50	—	—	50	—	ns
Slew Rate: Amplifier C	S_R	$R_L = 2.5k$	—	2.5	—	—	2.5	—	V/μs
Power Supply Current	I_{SY}	No Load	—	5.0	7.0	—	5.5	8.0	mA

NOTES:

1. Due to limited production test times the droop current corresponds to junction temperature (T_j). The droop current vs. time (after power-on) curve clarifies this point. Since most peak detectors (in use) are on for more than 1 second. PMI specifies droop rate for ambient temperature.
2. Guaranteed by design.
3. $\overline{\text{Channel A}}$ = "1", Channel B = "0".

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$, $C_H = 1000pF$, $-55°C \leq T_A \leq 125°C$ for GAP01A & B, GAP01EX & FX, and $0°C \leq T_A \leq 70°C$ for GAP01EP & FP.

PARAMETER	SYMBOL	CONDITIONS	GAP01A/E MIN	GAP01A/E TYP	GAP01A/E MAX	GAP01B/F MIN	GAP01B/F TYP	GAP01B/F MAX	UNITS
"g_m" AMPLIFIERS A, B									
Zero Scale Error	V_{ZS}		—	3.0	6.0	—	5.0	10	mV
Input Offset Voltage	V_{OS}		—	4.0	7.0	—	6.0	12	mV
Input Bias Current	I_B		—	160	250	—	160	550	nA
Input Offset Current	I_{OS}		—	30	100	—	30	150	nA
Voltage Gain	A_V		7.5	9.0	—	5.0	9.0	—	V/mV
Common Mode Rejection Ratio	CMRR	$10V \leq V_{CM} \leq +10V$	74	82	—	72	80	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \leq V_S \leq \pm 18V$	80	90	—	70	90	—	dB
Input Voltage Range	V_{CM}	(Note 2)	±11.0	±12.0	—	±10.5	±12.0	—	V
Slew Rate	SR		—	0.4	—	—	0.4	—	V/μs
Acquisition Time to 0.1% Accuracy	t_a	20V Step, $A_{VCL} = +1.0$	—	60	—	—	60	—	μs
COMPARATOR									
Input Offset Voltage	V_{OS}		—	2.0	2.5	—	2.0	5.0	mV
Input Bias Current	I_B		—	1000	2000	—	1100	2000	nA
Input Offset Current	I_{OS}		—	100	600	—	100	600	nA
Voltage Gain	A_V	2.0kΩ Pull-up Resistor to 5.0V (Note 2)	4.0	6.5	—	2.5	6.5	—	V/mV
Common Mode Rejection Ratio	CMRR	$-10V \leq V_{CM} \leq +10V$	80	100	—	80	92	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \leq V_S \leq \pm 18V$	72	82	—	72	86	—	dB
Input Voltage Range	V_{CM}	(Note 2)	±11.0	—	—	±11.0	—	—	V
Low Output Voltage	V_{OL}	$I_{sink} \leq 5.0mA$, Logic GND = 5.0V	-0.2	0.15	0.4	-0.2	0.15	0.4	V
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	—	25	100	—	100	160	μA
Output Short Circuit Current	I_{SC}	$V_{OUT} = 5V$	6.0	10	45	6.0	10	45	mA
Response Time	t_s	5mV Overdrive. (Note 3) 2.0kΩ Pull-up Resistor to 5.0V	—	200	—	—	200	—	ns
DIGITAL INPUTS-RST, DET (See Note 3)									
Logic "1" Input Voltage	V_H		2.0	—	—	2.0	—	—	V
Logic "0" Input Voltage	V_L		—	—	0.8	—	—	0.8	V
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	—	0.02	1.0	—	0.02	1.0	μA
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	—	2.5	15	—	2.5	15	μA
MISCELLANEOUS									
Droop Rate	V_{DR}	T_J = Max. Operating Temp. (Note 1)	—	1.0	10	—	1.0	10	
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	±11.0	±12.0	—	±10.5	±12.0	—	V
Short Circuit Current: Amplifier C	I_{SC}		6.0	12	40	6.0	12	40	mA
Switch Aperture Time	t_{ap}		—	75	—	—	75	—	ns
Slew Rate: Amplifier C	S_R	$R_L = 2.5k$	—	2.0	—	—	2.0	—	V/μs
Power Supply Current	I_{SY}	No Load	—	5.5	8.0	—	6.5	10.0	mA

NOTES:

1. Due to limited production test times the droop current corresponds to junction temperature (T_j). The droop current vs. time (after power-on) curve clarifies this point. Since most peak detectors (in use) are on for more than 1 second. PMI specifies droop rate for ambient temperature.
2. Guaranteed by design.
3. $\overline{\text{Channel A}}$ = "1", Channel B = "0".

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±18V
Power Dissipation 500mW
Input Voltage ..... Equal to Supply Voltage
Logic and Logic Ground
Voltage ..... Equal to Supply Voltage
Output Short Circuit Duration ..... Indefinite
Amplifier A or B Differential Input Voltage ..... ±24V
Cmparator Differential Input Voltage
Input Voltage ..... ±6.0V Indefinite
Input Voltage ..... ±24.0V Pulsed
(Input Bias Current may degrade from large continuous differential voltages)
Comparator Output Voltage... Equal to Positive Supply Voltage
Hold Capacitor Short Circuit Duration ..... Indefinite
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering 60 sec) ..... 300°C
Operating Temperature Range
GAP01BX ..... −55°C to +125°C
GAP01FX ..... −25°C to +85°C
GAP01EP ..... 0°C to +70°C
DICE Junction Temperature (T_j) ..... −65°C to +150°C

	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
18-Pin DIP (X)	100°C	10mW/°C
18-Pin DIP (P)	50°C	10mW/°C

NOTES:
1. Maximum package power dissipation vs. ambient temperature.
2. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

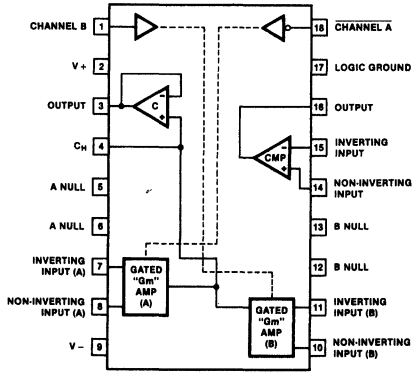
ORDERING INFORMATION†

V_{ZS} (mV)	HERMETIC MILITARY	HERMETIC INDUSTRIAL	PLASTIC COMMERCIAL
3.0	GAP01AX*	GAP01EX	GAP01EP
6.0	GAP01BX*	GAP01FX	GAP01FP

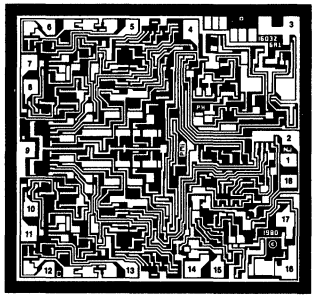
*Also available with MIL-STD-883B processing. To order add /883 as a suffix to the part number.

† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



DICE CHARACTERISTICS



1. CHANNEL (B)
2. V+
3. OUTPUT
4. C_H
5. (A) NULL
6. (A) NULL
7. INVERTING INPUT (A)
8. NON-INVERTING INPUT (A)
9. V−
10. NON-INVERTING INPUT (B)
11. INVERTING INPUT (B)
12. (B) NULL
13. (B) NULL
14. COMPARATOR NON-INVERTING INPUT
15. COMPARATOR INVERTING INPUT
16. COMPARATOR OUT
17. LOGIC GND
18. CHANNEL (A)

DIE SIZE 0.090 × 0.095 inch

Refer to Section 2 for additional DICE informaiton

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	GAP-01N LIMIT	UNITS
"g_m" AMPLIFIERS A, B				
Zero Scale Error	V_{ZS}		6.0	mV MAX
Input Offset Voltage	V_{OS}		7.0	mV MAX
Input Bias Current	I_B		250	nA MAX
Input Offset Current	I_{OS}		75	nA MAX
Voltage Gain	A_V		10	V/mV MIN
Common Mode Rejection Ratio	CMRR	$10V \le V_{CM} \le +10V$	74	dB MIN
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \pm 18V$	76	dB MIN
Input Voltage Range	V_{CM}	(Note 1)	± 11.5	V MIN
Feedthrough Error		$\Delta V_{IN} = 20V$, DET = 1, RST = 0	66	dB MIN
COMPARATOR				
Input Offset Voltage	V_{OS}		3.0	mV MAX
Input Bias Current	I_B		1000	nA MAX
Input Offset Current	I_{OS}		300	nA MAX
Voltage Gain	A_V	2.0kΩ Pull-up Resistor to 5.0V (Note 1)	3.5	V/mV MIN
Common Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	82	dB MIN
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \le \pm 18V$	76	dB MIN
Input Voltage Range	V_{CM}	(Note 1)	± 11.5	V MIN
Low Output Voltage	V_{OL}	$I_{SINK} \le 5.0mA$, Logic GND = 5.0V	0.4 −0.2	V MAX V MIN
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	80	μA MAX
Output Short Circuit Current	I_{SC}	$V_{OUT} = 5V$	45 7.0	mA MAX mA MIN
DIGITAL INPUTS-RST, DET (See Note 3)				
Logic "1" Input Voltage	V_H		2.0	V MIN
Logic "0" Input Voltage	V_L		0.8	V MAX
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	1.0	μA MAX
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	10	μA MAX
MISCELLANEOUS				
Droop Rate	V_{DR}	$F_J = 25°C$ $T_A = 25°C$ (See Note 2)	0.1 0.20	mV/ms MAX mV/ms MAX
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	± 11.0	V MIN
Short Circuit Current: Amplifier C	I_{SC}		40 7.0	mA MAX mA MIN
Power Supply Current	I_{SY}	No Load	9.0	mA MAX

NOTES:

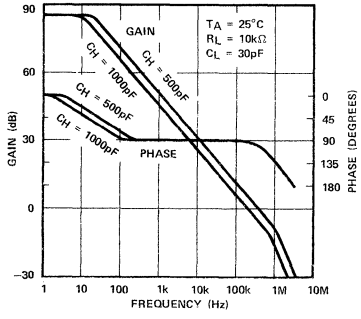
1. Guaranteed by design.
2. Due to limited production test times the droop current corresponds to junction temperature (T_J). The droop current vs. time (after power-on) curve clarifies this point. Since most peak detectors (in use) are on for more than 1 second. PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_J) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperatures.
3. DET = 1, RST = 0.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, and $T_A = 25°C$, unless otherwise noted.

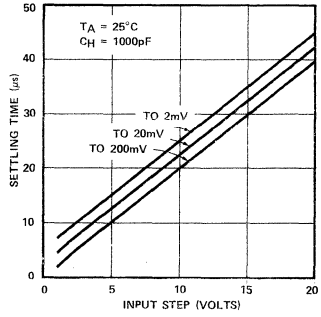
PARAMETER	SYMBOL	CONDITIONS	GAP-01N TYPICAL	UNITS
"g_m AMPLIFIERS A, B				
Slew Rate	SR		0.5	V/μs
Acquisition Time	t_a	0.1% Accuracy, 20V step, $A_{VCL} = 1$	41	μs
Acquisition Time	t_a	0.01% Accuracy, 20V step, $A_{VCL} = 1$	45	μs
COMPARATOR				
Response Time		5mV Overdrive 2kΩ Pull-up Resistor to +5.0V	150	ns
MISCELLANEOUS				
Switch Aperture Time	t_{ap}		75	ns
Switching Time	t_s		50	ns
Buffer Slew Rate	SR_C	$R_L = 2.5k\Omega$	2.5	V/μs

TYPICAL CHARACTERISTIC

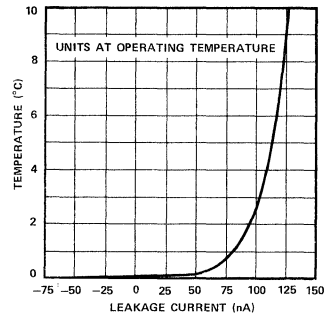
SMALL SIGNAL OPEN LOOP GAIN/PHASE vs FREQUENCY



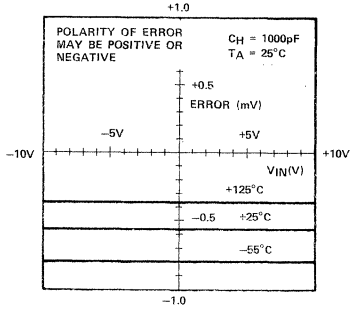
ACQUISITION TIME vs INPUT VOLTAGE STEP SIZE



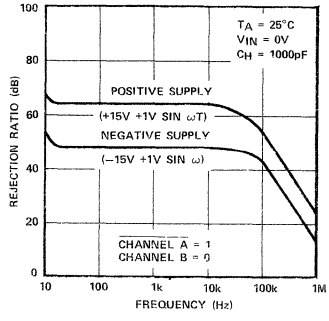
DROOP CURRENT vs TEMPERATURE



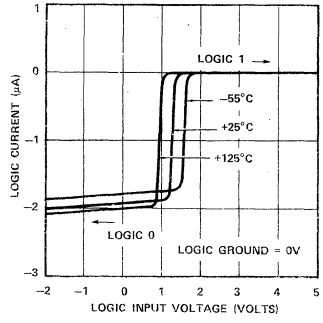
AMPLIFIER CHARGE INJECTION ERROR vs INPUT VOLTAGE AND TEMPERATURE



HOLD MODE POWER SUPPLY REJECTION vs FREQUENCY

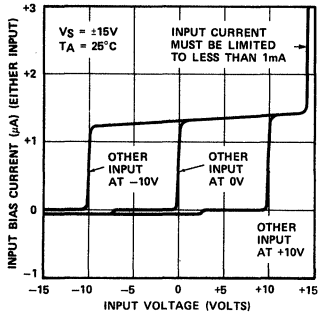


LOGIC INPUT CURRENT vs LOGIC INPUT VOLTAGE

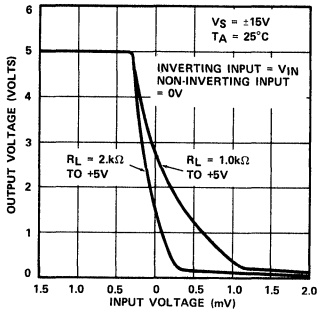


TYPICAL CHARACTERISTICS

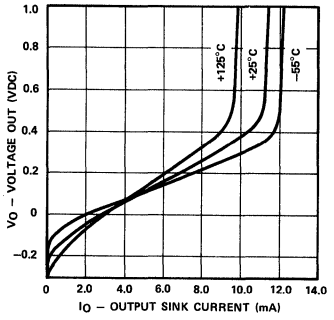
COMPARATOR INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



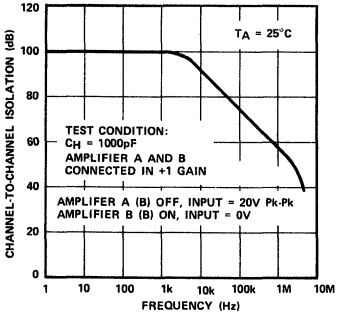
COMPARATOR TRANSFER CHARACTERISTIC



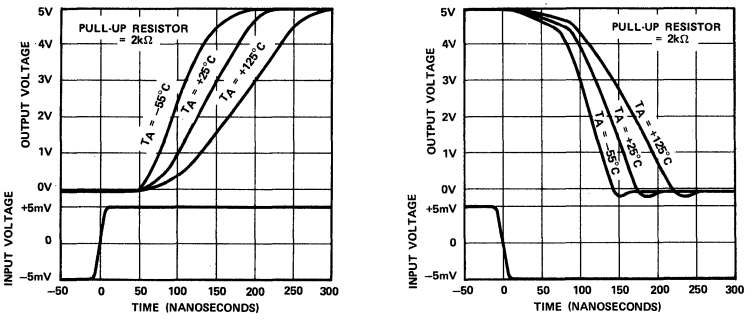
COMPARATOR OUTPUT VOLTAGE vs OUTPUT CURRENT AND TEMPERATURE



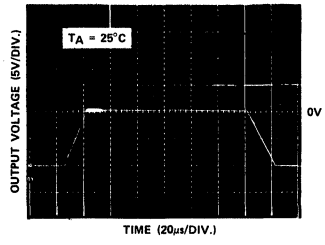
CHANNEL TO CHANNEL ISOLATION vs FREQUENCY



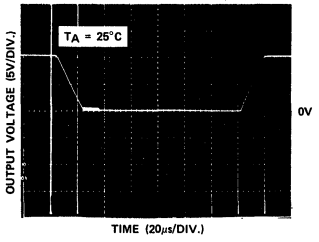
COMPARATOR RESPONSE TIME vs TEMPERATURE



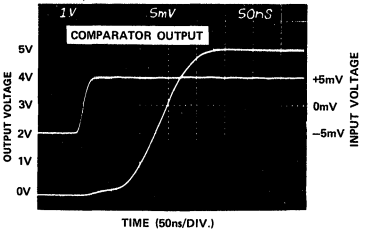
LARGE SIGNAL NON-INVERTING RESPONSE



LARGE SIGNAL NON-INVERTING RESPONSE

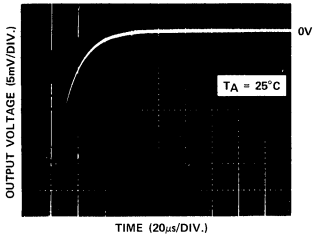


COMPARATOR OUTPUT RESPONSE TIME (2KΩ PULL-UP RESISTOR, $T_A = 25°C$)

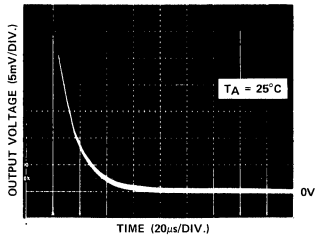


TYPICAL CHARACTERISTICS

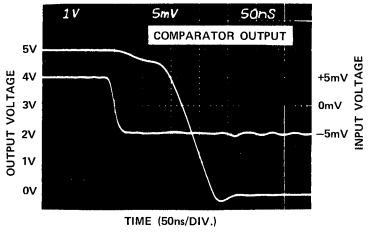
SETTLING TIME FOR −10V TO 0V STEP INPUT



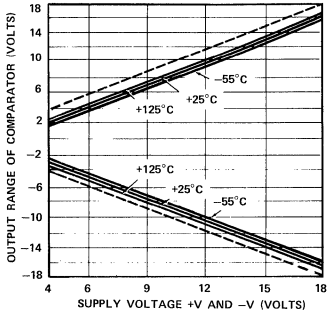
SETTLING TIME FOR +10V TO 0V STEP INPUT



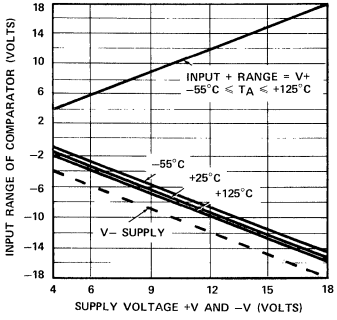
COMPARATOR OUTPUT RESPONSE TIME (2KΩ PULL-UP RESISTOR, $T_A = 25°C$



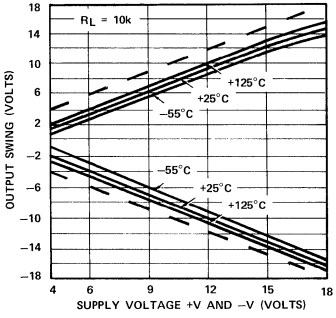
OUTPUT SWING OF COMPARATOR vs SUPPLY VOLTAGE



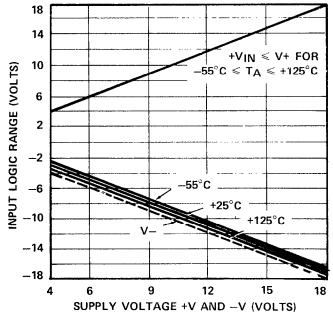
A AND B INPUT RANGE vs SUPPLY VOLTAGE



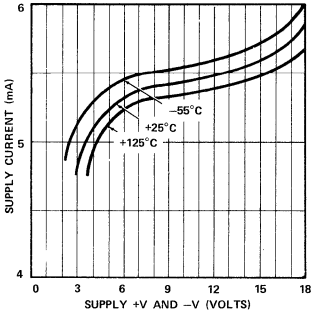
OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE (DUAL SUPPLY OPERATION)



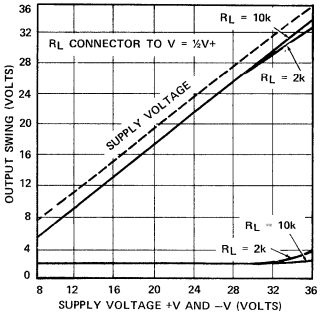
INPUT LOGIC RANGE vs SUPPLY VOLTAGE



SUPPLY CURRENT vs SUPPLY VOLTAGE

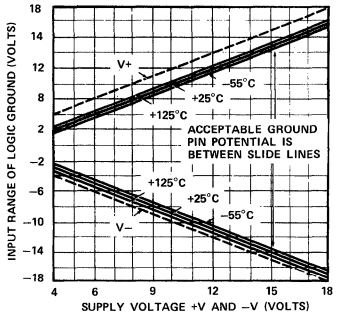


OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE (SINGLE SUPPLY OPERATION)

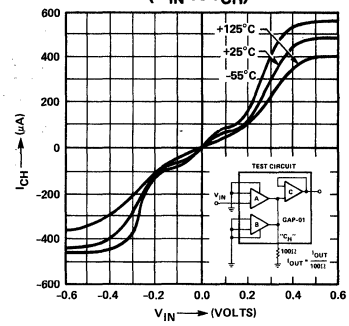


TYPICAL CHARACTERISTICS

INPUT RANGE OF LOGIC GROUND vs SUPPLY VOLTAGE

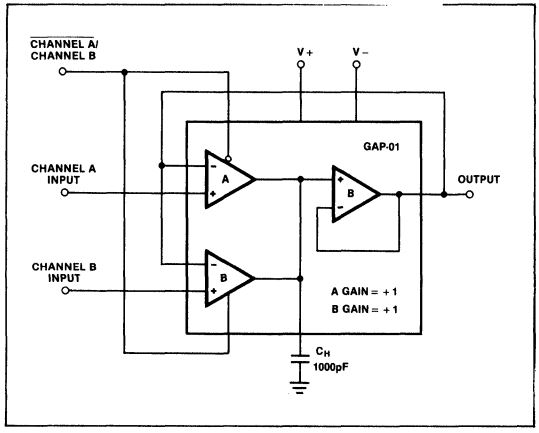


AMPLIFIER "A" OR "B" VOLTAGE TO CURRENT TRANSFER FUNCTION (V_{IN} vs I_{CH})

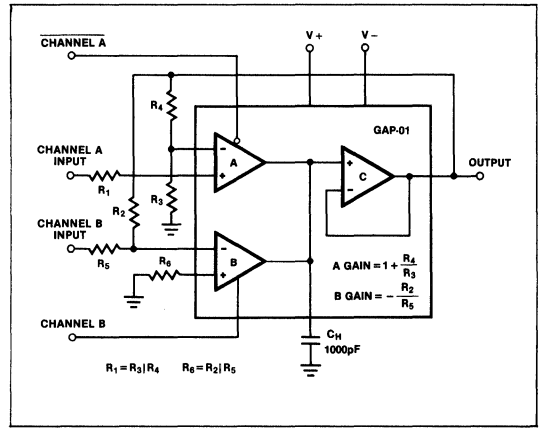


APPLICATION CIRCUITS

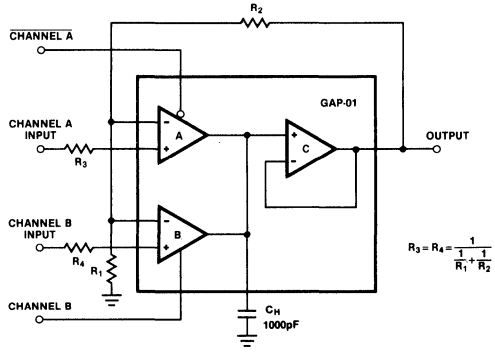
GAP-01 IN UNITY GAIN (+1) CONFIGURATION



GAP-01 WITH POSITIVE AND NEGATIVE GAINS

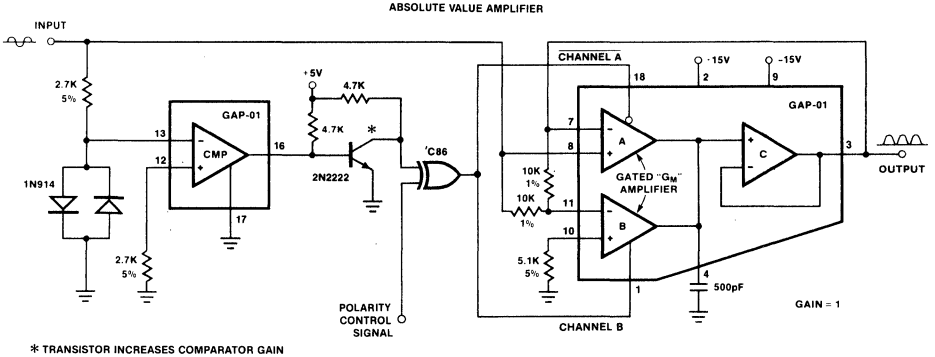


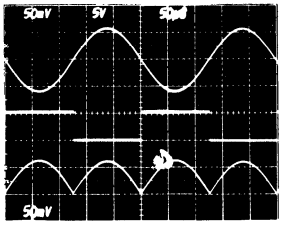
ALTERNATE GAIN CONFIGURATION



IF BOTH CHANNEL A AND CHANNEL B HAVE THE SAME POSITIVE VOLTAGE GAIN, A SINGLE VOLTAGE DIVIDER SETS THE GAIN FOR BOTH CHANNELS.

ABSOLUTE VALUE CIRCUIT WITH POLARITY PROGRAMMABLE OUTPUT

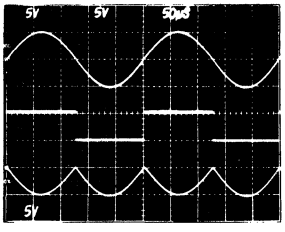




TRACE 1: INPUT SIGNAL

TRACE 2: $\overline{\text{CHANNEL A}}$/CHANNEL B CONTROL SIGNAL

TRACE 3: OUTPUT. POLARITY CONTROL SIGNAL = 1



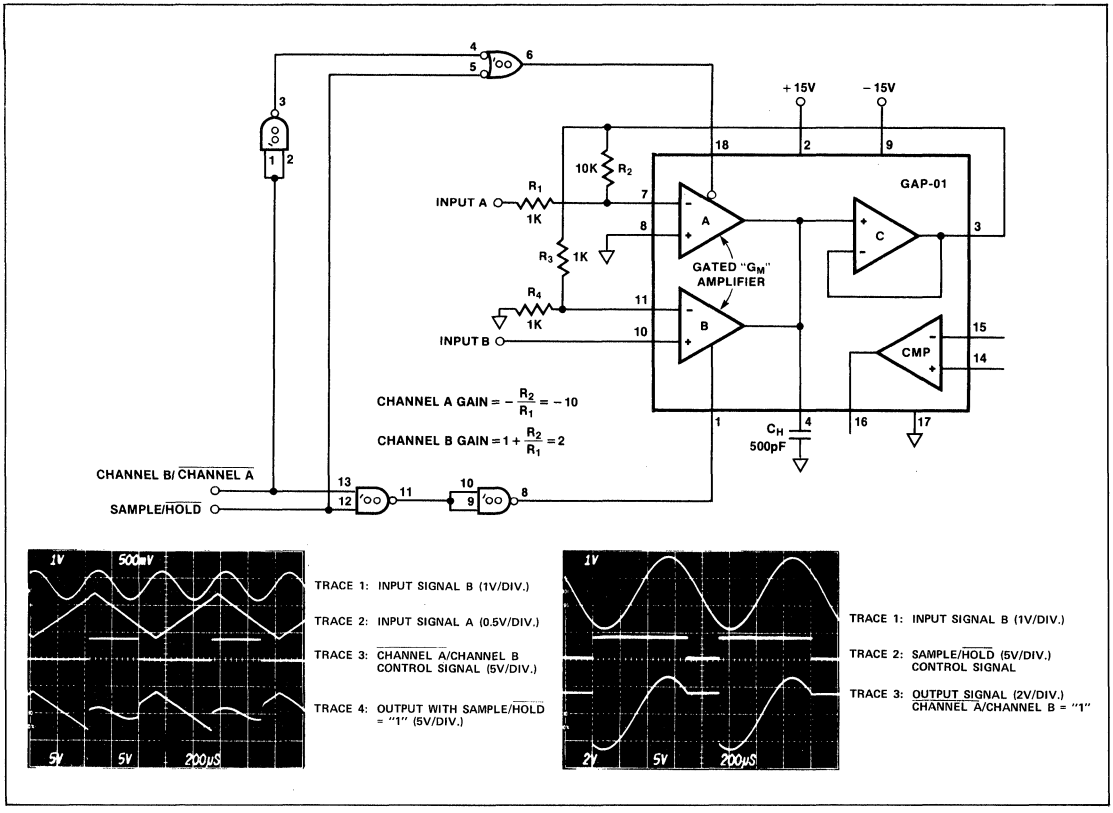
TRACE 1: INPUT SIGNAL

TRACE 2: $\overline{\text{CHANNEL A}}$/CHANNEL B CONTROL SIGNAL

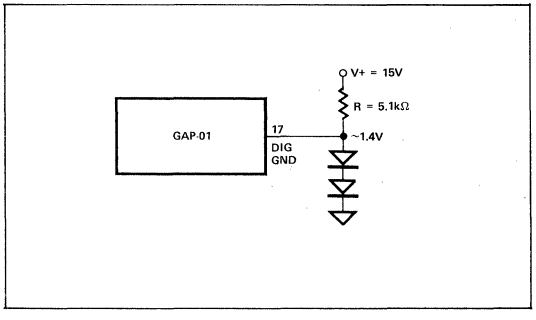
TRACE 3: OUTPUT. POLARITY CONTROL SIGNAL = 0

APPLICATION CIRCUITS

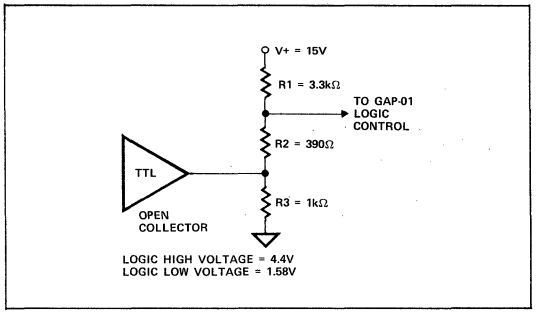
TWO-CHANNEL SAMPLE/HOLD AMPLIFIER



DIGITAL GROUND CONNECTION FOR SINGLE SUPPLY OPERATION

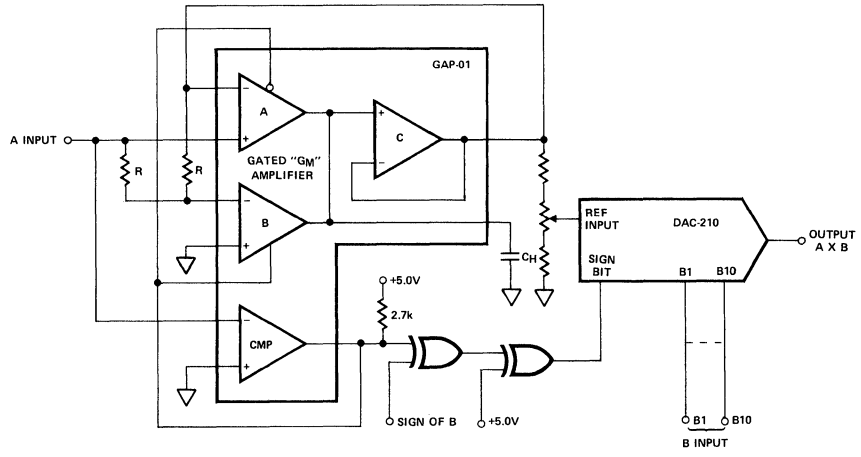


LOGIC LEVEL TRANSLATION FOR GAP-01 SINGLE SUPPLY OPERATION



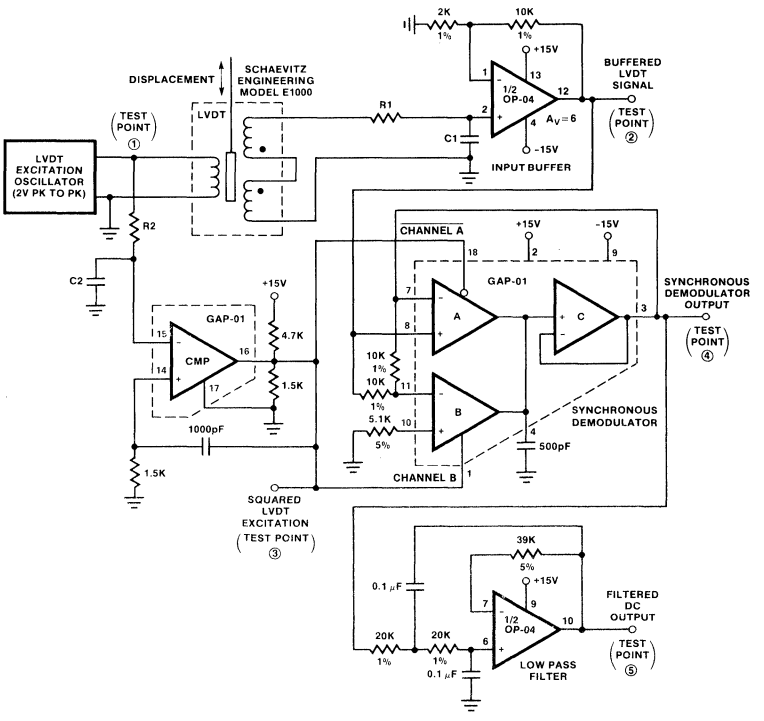
APPLICATION CIRCUITS

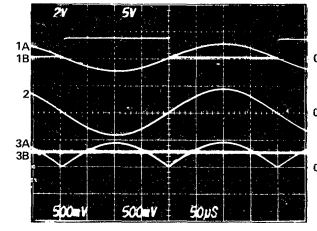
FOUR QUADRANT MULTIPLYING DAC



APPLICATION CIRCUITS

SYNCHRONOUS DEMODULATION OF LVDT SIGNAL





TRACE 1A: LVDT SINEWAVE EXCITATION (TEST POINT 1) –2V/DIV.
TRACE 1B: GAP-01 COMPARATOR OUTPUT (TEST POINT 3) –5V/DIV.

TRACE 2: BUFFERED LVDT OUTPUT AT GAP-01 INPUT (TEST POINT 2) 0.5V/DIV.

TRACE 3A: LVDT SIGNAL AFTER GAP-01 SYNCHRONOUS DEMODULATION (TEST POINT 4) –0.5V/DIV.

TRACE 3B: DC OUTPUT LEVEL INDICATING LVDT CORE POSITION (TEST POINT 5) 0.5V/DIV.

APPLICATION INFORMATION

CAPACITOR RECOMMENDATIONS

The external capacitor (C_H) serves as the compensation capacitor and hold capacitor in sample/hold applications. Stable operation requires a minimum value of 500pF. Larger capacitors may be used to lower droop rate errors, but acquisition time will increase and bandwidth decrease.

The capacitor should have very high insulation resistance and low dielectric absorption. For temperatures below 85°C, a polystyrene capacitor is recommended, while a Teflon capacitor is recommended for high temperature environments.

COMPARATOR

The comparator output high level (V_{OH}) is set by external resistors. It's possible to optimize noise immunity while interfacing to all standard logic families — TTL, DTL, and CMOS. Figure 1 shows the comparator output with external level setting resistors. Table I gives typical R_1 and R_2 values for common circuit conditions.

With the comparator in the low state (V_{OL}), the output stage will be required to sink a current approximately equal to V_C/R_1.

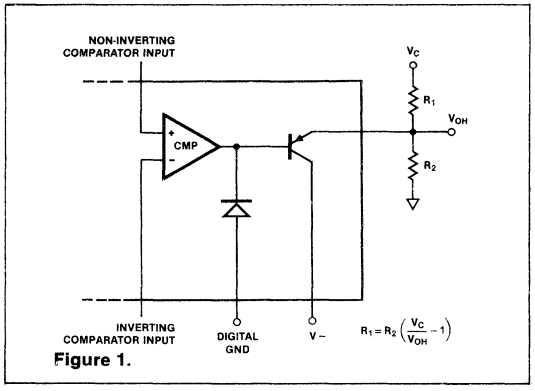


Figure 1.

Table I.

V_C	V_{OH}	R_1	R_2
5	3.5	2.7K	6.2K
5	5.0	2.7K	∞
15	3.5	4.7K	1.5K
15	5.0	4.7K	2.4K
15	7.5	7.5K	7.5K
15	10.0	7.5K	15K

$$R_1 \approx \frac{V_C}{I_{sink}}$$

$$R_2 \approx R_1\left(\frac{1}{\frac{V_C}{V_{OH}} - 1}\right)$$

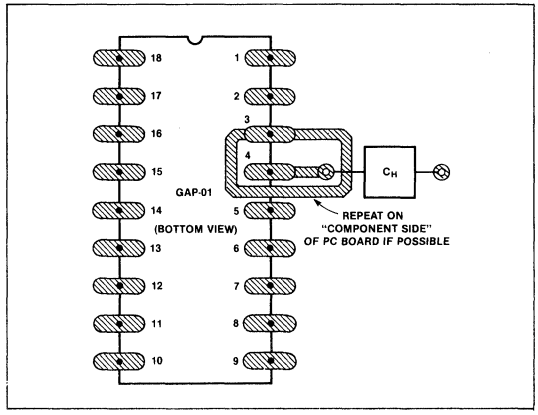
The maximum comparator high output voltage (V_{OH}) should be constrained to:

$$V_{OH}(max) < V+ - 2V$$

CAPACITOR GUARDING AND GROUND LAYOUT

Ground planes are recommended to minimize ground path resistance. Separate analog and digital grounds should be used. The two ground systems are tied together only at the common system ground. Avoid digital currents returning to the system ground through the analog ground path.

The C_H terminal (Pin 4) is a high-impedance point since a transconductance amplifier is used as the input amplifier. To minimize gain errors and maintain the GAP-01's inherently low droop rate, guarding Pin 4 is recommended.



LOGIC CONTROL

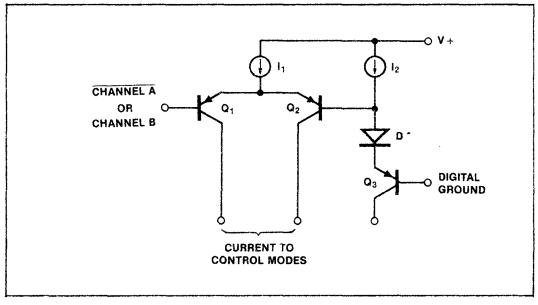
The input transconductance amplifier outputs are switched by the digital logic signals channel A and channel B. Two signal paths through the GAP-01 are possible.

The logic threshold voltage is 1.4 volts when digital ground is at zero volts. Other threshold voltages (V_{TH}) may be selected by applying the formula:

$$V_{TH} \approx 1.4V + \text{Digital Ground Potential.}$$

For proper operation, digital ground must always be at least 3.5V below the positive supply and 2.5V above the negative supply. The logic signals must always be at least 2.8V above the negative supply.

Operating the digital ground at other than zero volts does influence the comparator output low voltage. The V_{OL} level is



APPLICATION INFORMATION

reference to digital ground and will follow any changes in digital ground potential:

$V_{OL} \approx 0.2V$ + Digital Ground Potential.

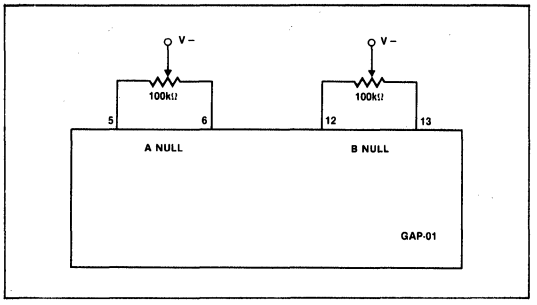
ZERO SCALE ERROR ADJUSTMENT

For sample/hold applications the zero scale error (V_{OS} plus charge injection error) can be adjusted to zero. With the input to each channel equal to zero, the GAP-01 is switched between the sample mode (either channel $\overline{A}$ or channel B active) and the hold mode (channel $\overline{A} = 1$, channel $B = 0$). The output is adjusted to read zero when the unit is in the hold mode.

The V_{ZS} trim circuit is identical to the V_{OS} trim circuit.

OFFSET VOLTAGE ERROR ADJUSTMENT

Offset voltage through either channel $\overline{A}$ or channel B may be nulled with an external 100kΩ potentiometer.



PKD-01

MONOLITHIC PEAK DETECTOR
WITH RESET AND HOLD MODE

FEATURES

- **Monolithic Design for Reliability and Low Cost**
- **Settling Time**
  20V Step to 0.1% ..... 41 μS
- **High Slew Rate 0.5v/μS**
- **Low Droop Rate**
  T_A = 25°C 0.1mV/mS
  T_A = 125°C 10mV/mS
- **Low Zero Scale Error 3.0mV**
- **Digitally Selected Hold and Reset Modes**
- **Reset Voltage Buffer Amplifier**
- **Reset to Positive or Negative Voltage Levels**
- **Logic Signals TTL and CMOS Compatible**
- **Uncommitted Comparator on Chip**
- **Wide Differential Input Voltage Range ..... ±24V**
- **Convenient 2 Supply Operation ..... ±15V**

Innovative design techniques were developed to maximize the advantages monolithic technology presented. Transconductance (g_m) amplifiers were chosen over conventional voltage amplifier circuit building blocks. The "g_m amplifiers simplify internal frequency compensation, minimize acquisition time and maximize circuit accuracy. The g_m amplifier outputs are easily switched by low glitch current steering circuits. The steered outputs are clamped to reduce charge injection errors upon entering the peak hold mode or exiting the reset mode. The inherently low zero scale error, is reduced further by active "Zener-Zap" trimming to optimize overall accuracy.

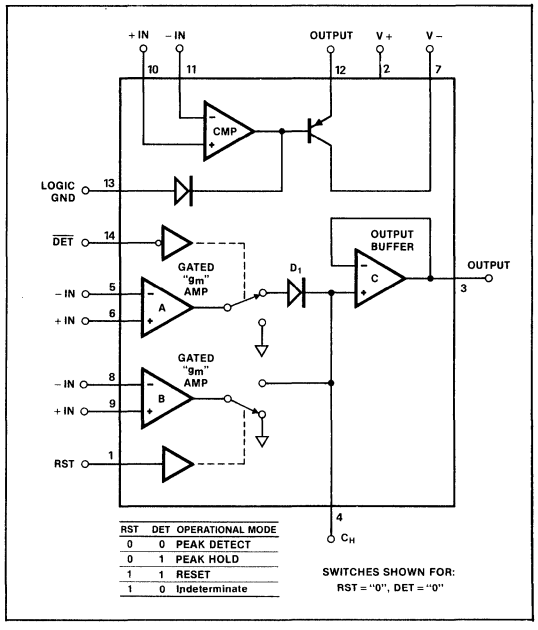
The output buffer amplifier features an FET input stage to reduce droop rate error during lengthy peak hold periods. A bias current cancellation circuit minimizes droop error at high ambient temperatures.

Many system functions are included in the PKD-01. The external hold capacitor is resettable to any voltage within the output buffer input voltage range. The analog reset voltage is applied through a high impedance, switched "g_m" amplifier. The reset buffer amplifier, B, may operate as a inverting or non-inverting gain stage.

Through the $\overline{DET}$ control pin, new peaks may either be detected or ignored. Detected peaks are presented as positive output levels. Positive or negative peaks may be detected without additional active circuits since amplifier A can operate as an inverting or non-inverting gain stage.

An uncommitted comparator provides many application options. Status indication and logic shaping/shifting are typical examples.

FUNCTIONAL DIAGRAM



Manufactured under the following patent: 4,285,051

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±18V
Power Dissipation 500mW
Input Voltage ..... Equal to Supply Voltage
Logic and Logic Ground
Voltage ..... Equal to Supply Voltage
Output Short Circuit Duration ..... Indefinite
Amplifier A or B Differential Input Voltage ..... ±24V
Comparator Differential Input Voltage
Input Voltage ..... ±6.0V Indefinite
Input Voltage ..... ±24.0V Pulsed
(Input Bias Current may degrade from large continuous differential voltages)
Comparator Output Voltage.. Equal to Positive Supply Votage
Hold Capacitor Short Circuit Duration ..... Indefinite
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering 60 sec) ..... 300°C
Operating Temperature Range
PKD01AY, PKD01BY ..... −55°C to +125°C
PKD01EY, PKD01FY ..... −25°C to +85°C
PKD01EP, PKD01FP ..... 0°C to +70°C
Dice Junction Temperature ..... −65°C to +150°C

	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin DIP (Y)	80°C	10mW/°C
14-Pin DIP (P)	50°C	6mW/°C

NOTES:

1. Maximum package power dissipation vs. ambient temperature.
2. Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $C_H = 1000pF$, $T_A = 25°C$.

			PKD01A/E			PKD01B/F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
"g_m" AMPLIFIERS A, B									
Zero Scale Error	V_{ZS}		–	2.0	3.0	–	3.0	6.0	mV
Input Offset Voltage	V_{OS}		–	2.0	4.0	–	3.0	7.0	mV
Input Bias Current	I_B		–	80	150	–	80	250	nA
Input Offset Current	I_{OS}		–	20	40	–	20	75	nA
Voltage Gain	A_V		18	25	–	10	25	–	V/mV
Common Mode Rejection Ratio	CMRR	$10V \le V_{CM} \le +10V$	80	90	–	74	90	–	dB
Power Supply Rejection Ratio	PSRR	$\pm9V \le V_S \le \pm18V$	86	96	–	76	96	–	dB
Input Voltage Range	V_{CM}	(Note 1)	±11.5	±12.0	–	±11.5	±12.0	–	V
Slew Rate	SR		–	0.5	–	–	0.5	–	V/μs
Feedthrough Error		$\Delta V_{IN} = 20V$, DET = 1, RST = 0	66	80	–	66	80	–	dB
Acquisition Time to 0.1% Accuracy	t_a	20V Step, $A_{VCL} = +1$	–	41	70	–	41	70	μs
Acquisition Time to 0.01% Accuracy	t_a	20V Step, $A_{VCL} = +1$	–	45	–	–	45	–	μs
COMPARATOR									
Input Offset Voltage	V_{OS}		–	0.5	1.5	–	1.0	3.0	mV
Input Bias Current	I_B		–	700	1000	–	700	1000	nA
Input Offset Current	I_{OS}		–	75	300	–	75	300	nA
Voltage Gain	A_V	2.0kΩ Pull-up Resistor to 5.0V (Note 1)	5	7.5	–	3.5	7.5	–	V/mV
Common Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	82	106	–	82	106	–	dB
Power Supply Rejection Ratio	PSRR	$\pm9V \le V_S \le \pm18V$	76	90	–	76	90	–	dB
Input Voltage Range	V_{CM}	(Note 1)	±11.5	±12.5	–	±11.5	±12.5	–	V
Low Output Voltage	V_{OL}	$I_{sink} \le 5.0mA$, Logic GND = 5.0V	−0.2	0.15	0.4	−0.2	0.15	0.4	V

NOTES:

1. Notes guaranteed by design.
2. Due to limited production test times the droop current corresponds to junction temperature (T_J). The droop current vs. time (after power-on) curve clarifies this point. Since most peak detectors (in use) are on for more than 1 second. PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_J) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperature. Ambient (T_A) temperature specifications are not subject to production testing.
3. DET = 1, RST = 0.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25°C$. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PKD01A/E MIN	PKD01A/E TYP	PKD01A/E MAX	PKD01B/F MIN	PKD01B/F TYP	PKD01B/F MAX	UNITS
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	–	25	80	–	25	80	μA
Output Short Circuit Current	I_{SC}	$V_{OUT} = 5V$	7.0	12	45	7.0	12	45	mA
Response Time	t_s	5mV Overdrive, (Note 3) 2.0kΩ Pull-up Resistor to 5.0V	–	150	–	–	150	–	ns
DIGITAL INPUTS-RST. DET (See Note 3)									
Logic "1" Input Voltage	V_H		2.0	–	–	2.0	–	–	V
Logic "0" Input Voltage	V_L		–	–	0.8	–	–	0.8	V
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	–	0.02	1.0	–	0.02	1.0	μA
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	–	1.6	10	–	1.6	10	μA
MISCELLANEOUS									
Droop Rate	V_{DR}	$T_J = 25°C$ $T_A = 25°C$ (See Note 2)	– –	0.01 0.02	0.07 0.15	– –	0.01 0.03	0.1 0.20	mV/ms
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	±11.5	±12.5	–	±11.0	±12.0	–	V
Short Circuit Current: Amplifier C	I_{SC}		7.0	15	40	7.0	15	40	mA
Switch Aperture Time	t_{ap}		–	75	–	–	75	–	μs
Switch Switching Time	ts		–	50	–	–	50	–	ns
Slew Rate: Amplifier C	S_R	$R_L = 2.5k$	–	2.5	–	–	2.5	–	V/μs
Power Supply Current	I_{SY}	No Load	–	5.0	7.0	–	6.0	9.0	mA

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$, $C_H = 1000pF$, $-55°C \le T_A \le 125°C$ for PKD01AY, PKD01BY, $-25°C \le T_A \le 85°C$ for PKD01EY, PKD01FY and $0°C \le T_A \le 70°C$ for PKD01EP, PKD01FP).

PARAMETER	SYMBOL	CONDITIONS	PKD01A/E MIN	PKD01A/E TYP	PKD01A/E MAX	PKD01B/F MIN	PKD01B/F TYP	PKD01B/F MAX	UNITS
"g_m" AMPLIFIERS A, B									
Zero Scale Error	V_{ZS}		–	3.0	6.0	–	5.0	10	mV
Input Offset Voltage	V_{OS}		–	4.0	7.0	–	6.0	12	mV
Input Bias Current	I_B		–	160	250	–	160	550	nA
Input Offset Current	I_{OS}		–	30	100	–	30	150	nA
Voltage Gain	A_V		7.5	9.0	–	5.0	9.0	–	V/mV
Common Mode Rejection Ratio	CMRR	$10V \le V_{CM} \le +10V$	74	82	–	72	80	–	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \le \pm 18V$	80	90	–	70	90	–	dB
Input Voltage Range	V_{CM}	(Note 1)	±11.0	±12.0	–	±10.5	±12.0	–	V
Slew Rate	SR		–	0.4	–	–	0.4	–	V/μs
Acquisition Time to 0.1% Accuracy	t_a	20V Step, $A_{VCL} = +1$	–	60	–	–	60	–	μs
COMPARATOR									
Input Offset Voltage	V_{OS}		–	2.0	2.5	–	2.0	5.0	mV
Input Bias Current	I_B		–	1000	2000	–	1100	2000	nA
Input Offset Current	I_{OS}		–	100	600	–	100	600	nA
Voltage Gain	A_V	2.0kΩ Pull-up Resistor to 5.0V	4.0	6.5	–	2.5	6.5	–	V/mV
Common Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	80	100	–	80	92	–	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \le \pm 18V$	72	82	–	72	86	–	dB
Input Voltage Range	V_{CM}	(Note 1)	±11.0	–	–	±11.0	–	–	V
Low Output Voltage	V_{OL}	$I_{sink} \le 5.0mA$, Logic GND = 5.0V	-0.2	0.15	0.4	-0.2	0.15	0.4	V

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$, $C_H = 1000pF$, $-55°C \leq T_A \leq 125°C$ for PKD01AY, PKD01BY, $-25°C \leq T_A \leq 85°C$ for PKD01EY, PKD01FY and $0°C \leq T_A \leq 70°C$ for PKD01EP, PKD01FP). (Continued)

PARAMETER	SYMBOL	CONDITIONS	PKD01A/E MIN	PKD01A/E TYP	PKD01A/E MAX	PKD01B/F MIN	PKD01B/F TYP	PKD01B/F MAX	UNITS
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	–	25	100	–	100	180	μA
Output Short Circuit Current	I_{SC}	$V_{OUT} = 5V$	6.0	10	45	6.0	10	45	mA
Response Time	t_s	5mV Overdrive. 2.0kΩ Pull-up Resistor to 5.0V	–	200	–	–	200	–	ns
DIGITAL INPUTS-RST. DET *(See Note 3)*									
Logic "1" Input Voltage	V_H		2.0	–	–	2.0	–	–	V
Logic "0" Input Voltage	V_L		–	–	0.8	–	–	0.8	V
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	–	0.02	1.0	–	0.02	1.0	μA
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	–	2.5	15	–	2.5	15	μA
MISCELLANEOUS									
Droop Rate	V_{DR}	T_J = Max. Operating Temp T_A = Max. Operating Temp. DET = 1, Note 2	– –	1.2 2.4	10 20	– –	3.0 6.0	15 20	mV/ms
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	±11.0	±12.0	–	±10.5	±12.0	–	V
Short Circuit Current: Amplifier C	I_{SC}		6.0	12	40	6.0	12	40	mA
Switch Aperture Time	t_{ap}		–	75	–	–	75	–	ns
Slew Rate: Amplifier C	S_R	$R_L = 2.5k$	–	2.0	–	–	2.0	–	V/μs
Power Supply Current	I_{SY}	No Load	–	5.5	8.0	–	6.5	10.0	mA

NOTES:

1. Guaranteed by design.
2. Due to limited production test times the droop current corresponds to junction temperature (T_J). The droop current vs. time (after power-on) curve clarifies this point. Since most peak detectors (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_J) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperature. Ambient (T_A) temperature specifications are not subject to production testing.
3. DET = 1, RST = 0.

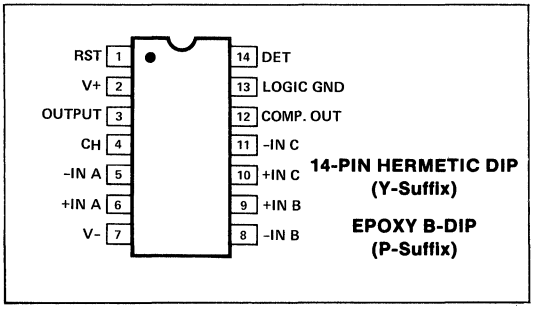
ORDERING INFORMATION†

25°C Vzs (mV)	PACKAGE 14 PIN DIP HERMETIC	PACKAGE 14 PIN DIP PLASTIC	OPERATING TEMPERATURE RANGE
3	PKD01AY*	—	MIL
6	PKD01BY*	—	MIL
3	PKD01EY	—	IND
6	PKD01FY	—	IND
3	—	PKD01EP	COM
6	—	PKD01FP	COM

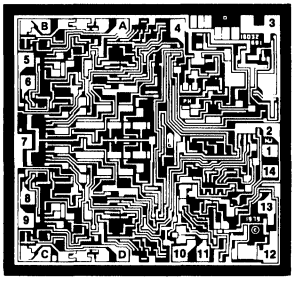
*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number.

†All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS



DICE CHARACTERISTICS



1. RST (RESET CONTROL)
2. V+
3. OUTPUT
4. C_H (HOLD CAPACITOR)
5. INVERTING INPUT (A)
6. NON-INVERTING INPUT (B)
7. V−
8. NON-INVERTING INPUT (B)
9. INVERTING INPUT (B)
10. COMPARATOR NON-INVERTING INPUT
11. COMPARATOR INVERTING INPUT
12. COMPARATOR OUTPUT
13. LOGIC GROUND
14. DET (PEAK DETECT CONTROL)
    A,B (A) NULL
    C,D (B) NULL

0.090 inch × 0.095 inch

Refer to Section 2 for additional DICE information.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	PKD-01N LIMIT	UNITS
"g_m" AMPLIFIERS A, B				
Zero Scale Error	V_{ZS}		6.0	mV MAX
Input Offset Voltage	V_{OS}		7.0	mV MAX
Input Bias Current	I_B		250	nA MAX
Input Offset Current	I_{OS}		75	nA MAX
Voltage Gain	A_V		10	V/mV MIN
Common Mode Rejection Ratio	CMRR	$10V \le V_{CM} \le +10V$	74	dB MIN
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \pm 18V$	76	dB MIN
Input Voltage Range	V_{CM}	(Note 1)	±11.5	V MIN
Feedthrough Error		$\Delta V_{IN} = 20V$, DET = 1, RST = 0	66	dB MIN
COMPARATOR				
Input Offset Voltage	V_{OS}		3.0	mV MAX
Input Bias Current	I_B		1000	nA MAX
Input Offset Current	I_{OS}		300	nA MAX
Voltage Gain	A_V	2.0kΩ Pull-up Resistor to 5.0V (Note 1)	3.5	V/mV MIN
Common Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	82	dB MIN
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \le \pm 18V$	76	dB MIN
Input Voltage Range	V_{CM}	(Note 1)	±11.5	V MIN
Low Output Voltage	V_{OL}	$I_{SINK} \le 5.0mA$, Logic GND = 5.0V	0.4 −0.2	V MAX V MIN
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	80	µA MAX
Output Short Circuit Current	I_{SC}	$V_{OUT} = 5V$	45 7.0	mA MAX mA MIN

NOTES:
1. Guaranteed by design.
2. Due to limited production test times the droop current corresponds to junction temperature (T_J). The droop current vs. time (after power-on) curve clarifies this point. Since most peak detectors (in use) are on for more than 1 second. PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_J) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperature. Ambient (T_A) temperature specifications are not subject to production testing.
3. DET = 1, RST = 0.

DICE CHARACTERISTICS

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25°C$. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PKD-01N LIMIT	UNITS
DIGITAL INPUTS-RST, DET (See Note 3)				
Logic "1" Input Voltage	V_H		2.0	V MIN
Logic "0" Input Voltage	V_L		0.8	V MAX
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	1.0	µA MAX
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	10	µA MAX
MISCELLANEOUS				
Droop Rate	V_{DR}	$F_J = 25°C$ (See Note 2) $T_A = 25°C$	0.1 0.20	mV/ms MAX mV/ms MAX
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	±11.0	V MIN
Short Circuit Current: Amplifier C	I_{SC}		40 7.0	mA MAX mA MIN
Power Supply Current	I_{SY}	No Load	9.0	mA MAX

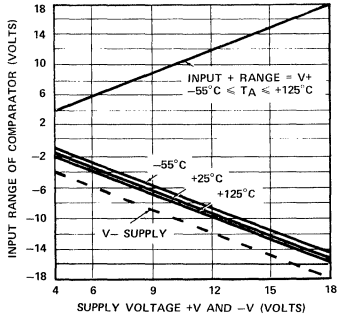
NOTES:
1. Guaranteed by design.
2. Due to limited production test times the droop current corresponds to junction temperature (T_J). The droop current vs. time (after power-on) curve clarifies this point. Since most peak detectors (in use) are on for more than 1 second. PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_J) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperatures.
3. DET = 1, RST = 0.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, and $T_A = 25°C$, unless otherwise noted.

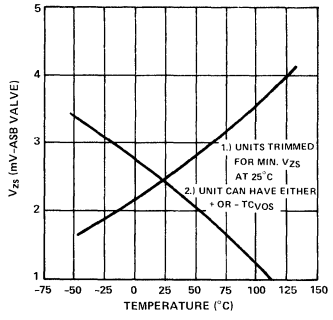
PARAMETER	SYMBOL	CONDITIONS	PKD-01N TYPICAL	UNITS
"g_m AMPLIFIERS A, B				
Slew Rate	SR		0.5	V/µs
Acquisition Time	t_a	0.1% Accuracy, 20V step, $A_{VCL} = 1$	41	µs
Acquisition Time	t_a	0.01% Accuracy, 20V step, $A_{VCL} = 1$	45	µs
COMPARATOR				
Response Time		5mV Overdrive 2kΩ Pull-up Resistor to +5.0V	150	ns
MISCELLANEOUS				
Switch Aperture Time	t_{ap}		75	ns
Switching Time	t_s		50	ns
Buffer Slew Rate	SR_C	$R_L = 2.5k\Omega$	2.5	V/µs

TYPICAL PERFORMANCE CHARACTERISTICS

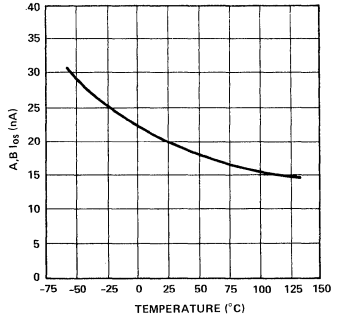
A AND B INPUT RANGE vs SUPPLY VOLTAGE



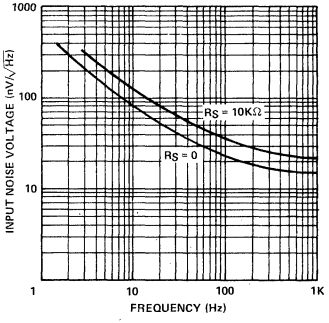
V_{ZS} vs TEMPERATURE A AND B AMPLIFIERS



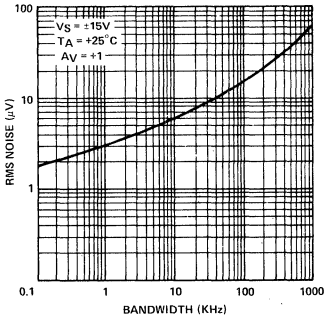
A, B I_{OS} vs TEMPERATURE



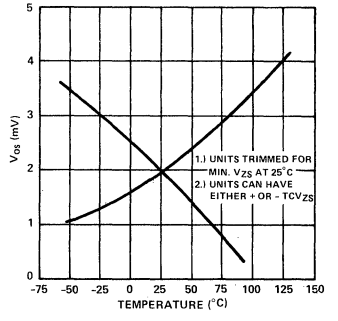
INPUT SPOT NOISE vs FREQUENCY



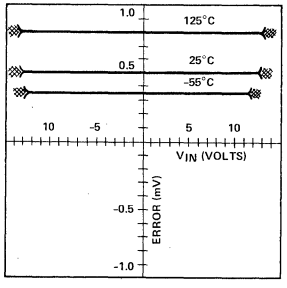
WIDEBAND NOISE vs BANDWIDTH



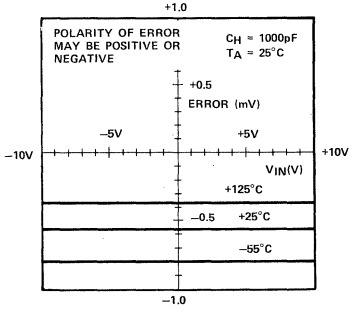
A AND B V_{OS} vs TEMPERATURE



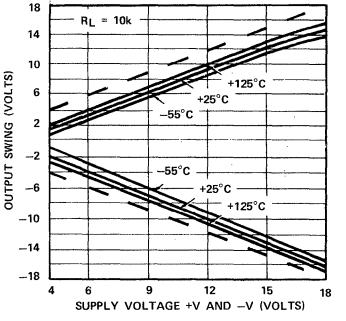
AMPLIFIER B CHARGE INJECTION ERROR vs INPUT VOLTAGE AND TEMPERATURE



AMPLIFIER CHARGE INJECTION ERROR vs INPUT VOLTAGE AND TEMPERATURE

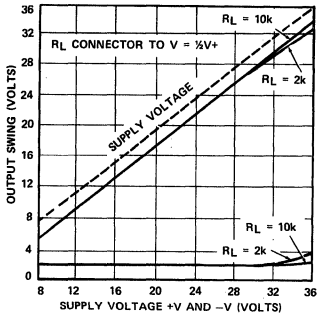


OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE (DUAL SUPPLY OPERATION)

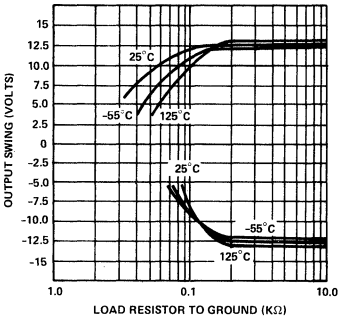


TYPICAL PERFORMANCE CHARACTERISTICS

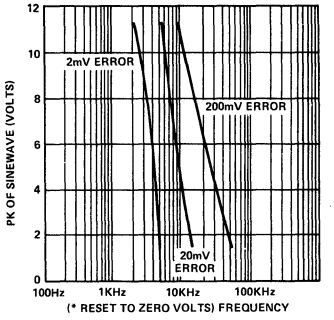
OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE (SINGLE SUPPLY OPERATION)



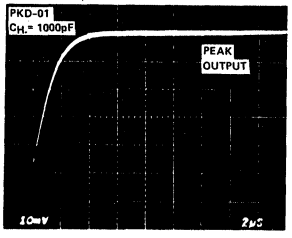
OUTPUT VOLTAGE vs LOAD RESISTANCE



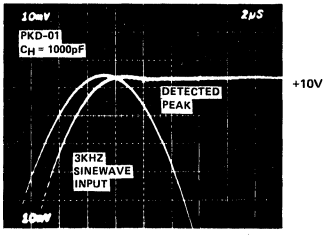
OUTPUT ERROR FOR FREQUENCY vs INPUT VOLTAGE



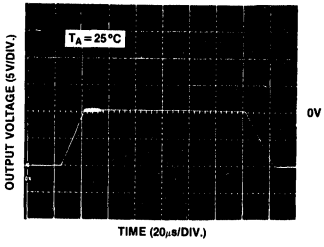
PKD-01 SETTLING RESPONSE



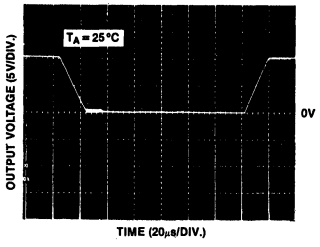
PKD-01 SETTLING RESPONSE



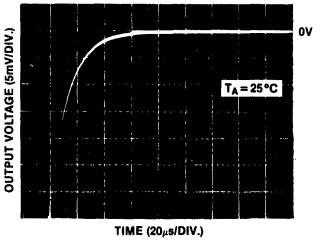
LARGE SIGNAL NON-INVERTING RESPONSE



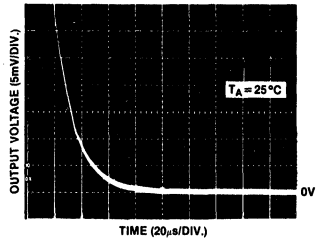
LARGE SIGNAL NON-INVERTING RESPONSE



SETTLING TIME FOR –10V TO 0V STEP INPUT

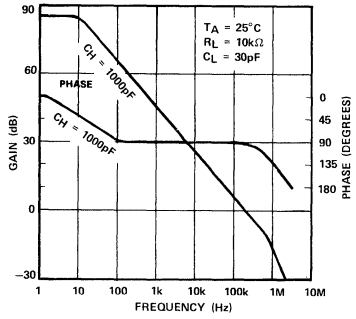


SETTLING TIME FOR +10V TO 0V STEP INPUT

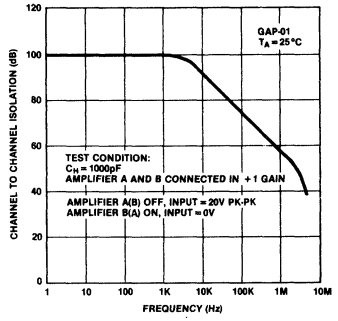


TYPICAL PERFORMANCE CHARACTERISTICS

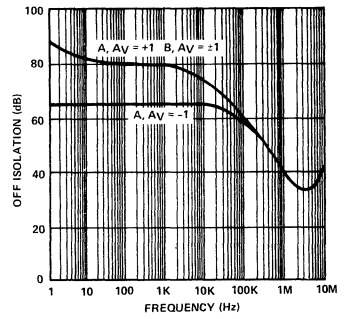
SMALL SIGNAL OPEN LOOP GAIN/PHASE vs FREQUENCY



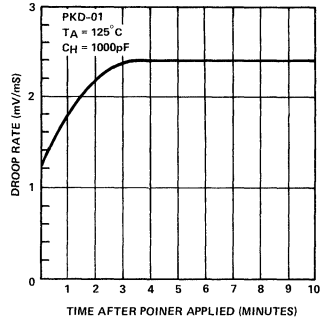
CHANNEL TO CHANNEL ISOLATION vs FREQUENCY



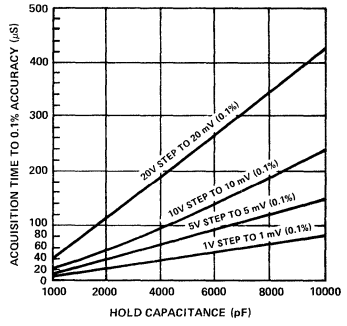
OFF ISOLATION vs FREQUENCY



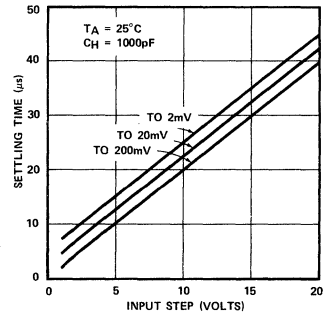
DROOP RATE vs TIME AFTER POWER ON



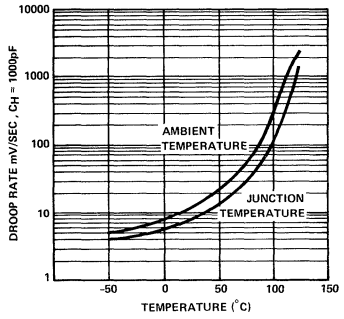
AQUISITION TIME vs EXTERNAL HOLD CAPACITOR AND AQUISITION STEP



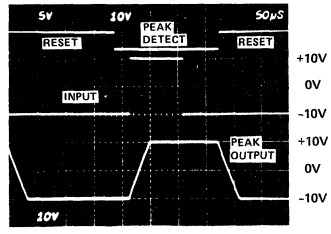
AQUISITION TIME vs INPUT VOLTAGE STEP SIZE



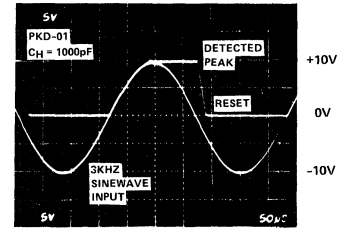
DROOP RATE vs TEMPERATURE



AQUISITION OF STEP INPUT

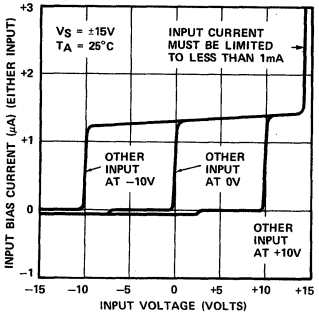


AQUISITION OF SINEWAVE PEAK

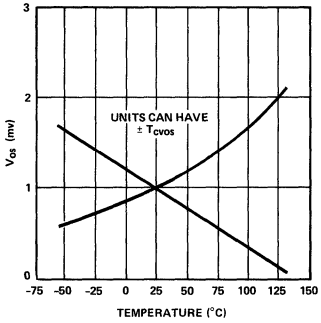


TYPICAL PERFORMANCE CHARACTERISTICS

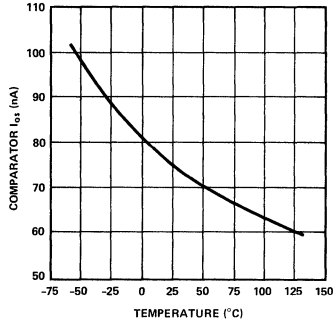
COMPARATOR INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



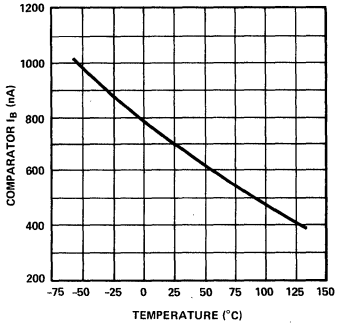
COMPARATOR V_{OS} vs TEMPERATURE



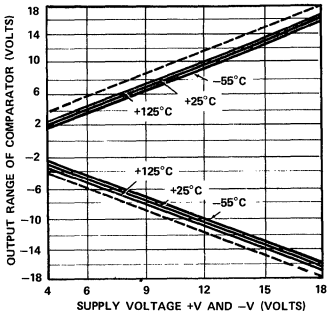
COMPARATOR I_{OS} vs TEMPERATURE



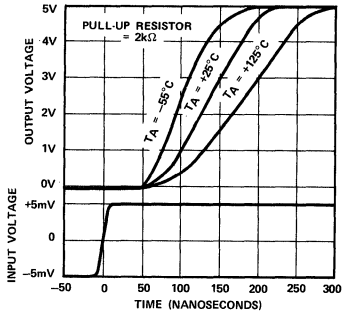
COMPARATOR I_B vs TEMPERATURE



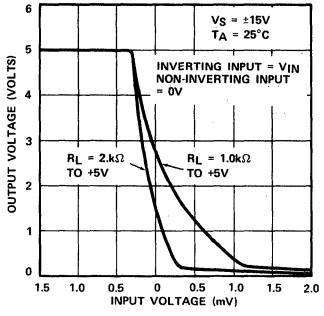
OUTPUT SWING OF COMPARATOR vs SUPPLY VOLTAGE



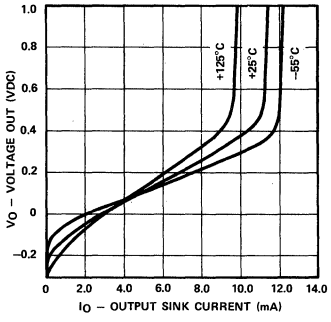
COMPARATOR RESPONSE TIME vs TEMPERATURE



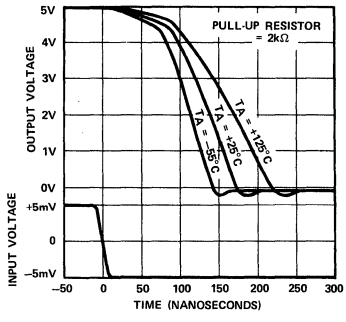
COMPARATOR TRANSFER CHARACTERISTIC



COMPARATOR OUTPUT VOLTAGE vs OUTPUT CURRENT AND TEMPERATURE

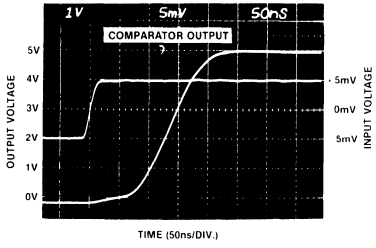


COMPARATOR RESPONSE TIME vs TEMPERATURE

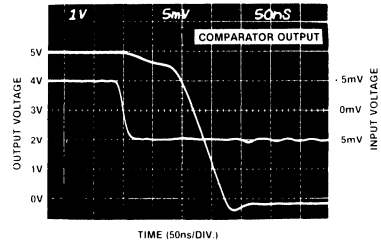


TYPICAL PERFORMANCE CHARACTERISTICS

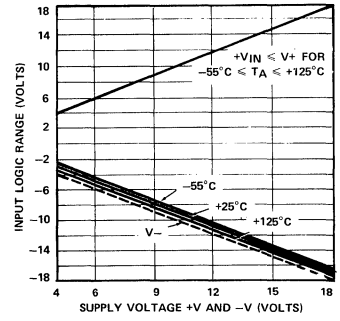
COMPARATOR OUTPUT RESPONSE TIME
(2kΩ PULL-UP RESISTOR, $T_A = 25°C$)



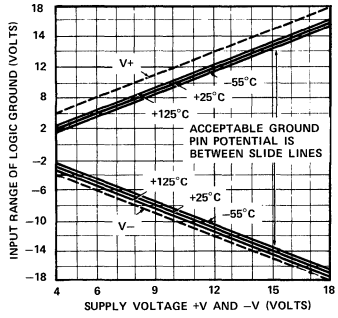
COMPARATOR OUTPUT RESPONSE TIME
(2kΩ PULL-UP RESISTOR, $T_A = 25°C$)



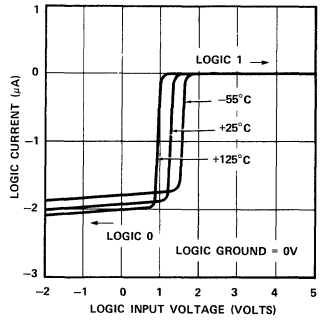
INPUT LOGIC RANGE vs SUPPLY VOLTAGE



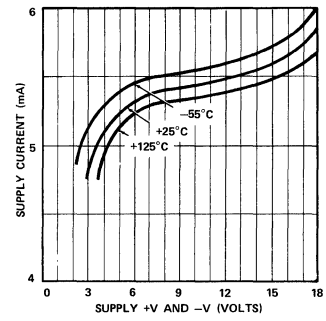
INPUT RANGE OF LOGIC GROUND vs SUPPLY VOLTAGE



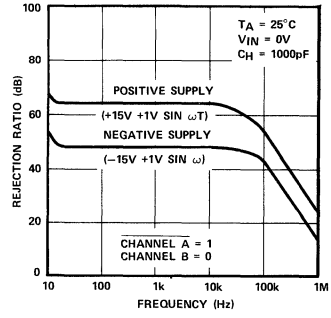
LOGIC INPUT CURRENT vs LOGIC INPUT VOLTAGE



SUPPLY CURRENT vs SUPPLY VOLTAGE



HOLD MODE POWER SUPPLY REJECTION vs FREQUENCY



THEORY OF OPERATION

The typical peak detector uses voltage amplifiers and a diode or an emitter follower to charge the hold capacitor, C_H, unidirectionally (Figure 1). The output impedance of A plus D_1's dynamic impedance, r_d, make up the resistance which determines the feedback loop pole. The dynamic impedance is $r_d = \frac{kT}{q\, I_d}$. I_d is the capacitor charging current.

The pole moves toward the origin of the S plane as I_d goes to zero. The pole movement in itself will not significantly lengthen the acquisition time since the pole is enclosed in the system feedback loop.

When the moving pole is considered with the typical frequency compensation of voltage amplifiers there is, however, a loop stability problem. The necessary compensation can increase the required acquisition time. PMI's approach replaces the input voltage amplifier with a transconductance amplifier; Figure 2.

The PKD-01 transfer function can be reduced to:

$$\frac{V_{out}}{V_{IN}} = \frac{1}{1 + \frac{sC_H}{g_m} + \frac{1}{g_m R_{out}}} \approx \frac{1}{1 + \frac{sC_H}{g_m}}$$

Where: $g_m \approx 1\mu A/mV$, $R_{out} \approx 20M\Omega$.

The diode in series with A's output (Figure 2) has no effect because it is a resistance in series with a current source. In addition to simplifying the system compensation, the input transconductance amplifier output current is switched by current steering. The steered output is clamped to reduce and match any charge injection.

Fig. 3 shows a simplified schematic of the reset "g_m" amplifier, B. In the track mode, Q_1 & Q_4 are ON and Q_2 & Q_3 are OFF. A current of 2I passes through D_1, I is summed at "B" and passes through Q_1, and is summed with $g_m V_{IN}$. The current sink can absorb only 3I, thus, the current passing through D_2 can only be: $2I - g_m V_{IN}$. The net current into the hold capacitor node then, is $g_m V_{IN}$ ($IC_H = 2I - (2I - g_m V_{IN})$. The hold mode, Q_2 & Q_3 are ON while Q_1 & Q_4 are OFF. The net current into the top of D_1 is $-I$ until D_3 turns ON. With Q_1 OFF, the bottom of D_2 is pulled up with a current I until D_4 turns ON, thus D_1 & D_2 are reverse biased by $\approx 0.6V$ and charge injection is independent of input level.

The monolithic layout results in points A and B having equal nodal capacitance. In addition, matched diodes D_1 and D_2 have equal diffusion capacitance. When the transconductance amplifier outputs are switched open, points A and B are ramped equally but in opposite phase. Diode clamps D_3 and D_4 cause the swings to have equal amplitudes. The net charge injection (voltage change) at node C is therefore zero.

The peak transconductance amplifier, A, is shown in Figure 4. Unidirectional hold capacitor charging requires diode D_1 to be connected in series with the output. Upon entering the peak hold mode D_1 is reverse biased. The voltage clamp limits charge injection to approximately 1pC and the hold step to 0.6mV.

Minimizing acquisition time dictated a small C_H capacitance. A 1000pF value was selected. Droop rate was also minimized by providing the output buffer with an FET input stage. A current cancellation circuit further reduces droop current and minimizes the gate current's tendency to double for every 10°C temperature change.

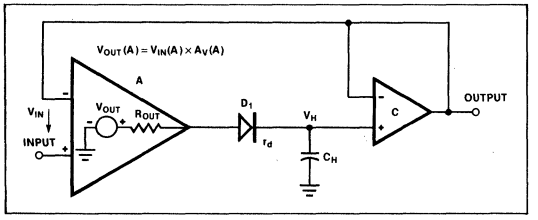


Figure 1. Conventional Voltage Amplifier Peak Detector.

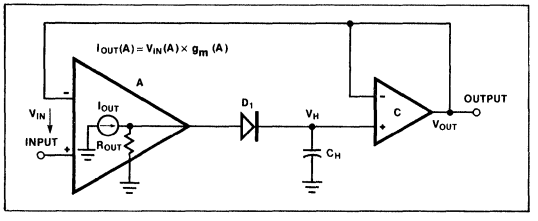


Figure 2. Transconductance Amplifier Peak Detector.

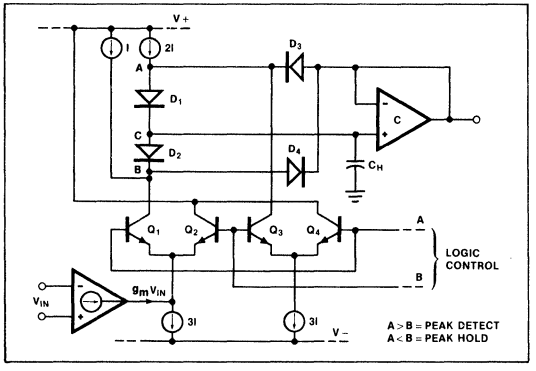


Figure 3. Transconductance Amplifier With Low Glitch Current Switch

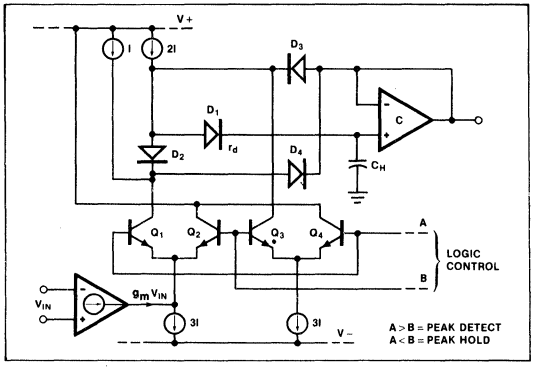


Figure 4. Peak Detecting Transconductance Amplifier With Switched Output.

APPLICATION INFORMATION

OPTIONAL OFFSET VOLTAGE ADJUSTMENT

Offset voltage is the primary zero scale error component since a variable voltage clamp limits voltage excursions at D_1's anode and reduces charge injection. The PKD-01 circuit gain and operational mode (positive or negative peak detection) determine the applicable null circuit. Figures A through D are suggested circuits. Each circuit corrects amplifier C offset voltage error also.

A. NULLING GATED OUTPUT g_m AMPLIFIER A. Diode D_1 must be conducting to close the feedback circuit during amplifier A V_{OS} adjustment. Resistor network R_A-R_C cause D_1 to conduct slightly. With $\overline{DET} = 0$ and $V_{IN} = 0V$ monitor the PKD-01 output. Adjust the null potentiometer until $V_{OUT} = 0V$. After adjustment, disconnect R_C from C_H.

B. NULLING GATED g_m AMPLIFIER B. Set amplifier B signal input to $V_{IN} = 0V$ and monitor the PKD-01 output. Set $\overline{DET} = 1$, $RST = 1$ and adjust the null potentiometer for $V_{OUT} = 0V$. The circuit gain — inverting or noninverting — will determine which null circuit illustrated in Figures A through D is applicable.

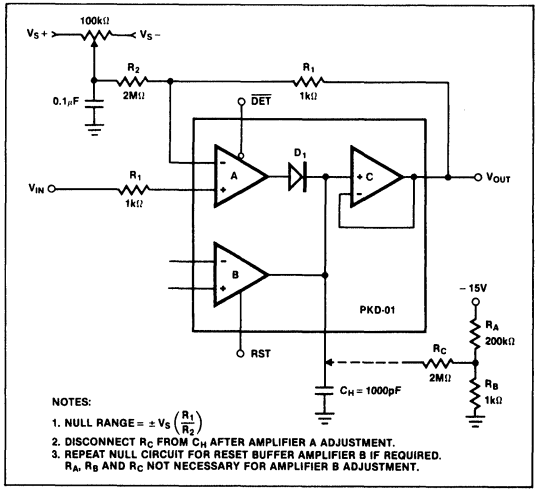


Figure A. V_{OS} Null Circuit for Unity Gain Positive Peak Detector.

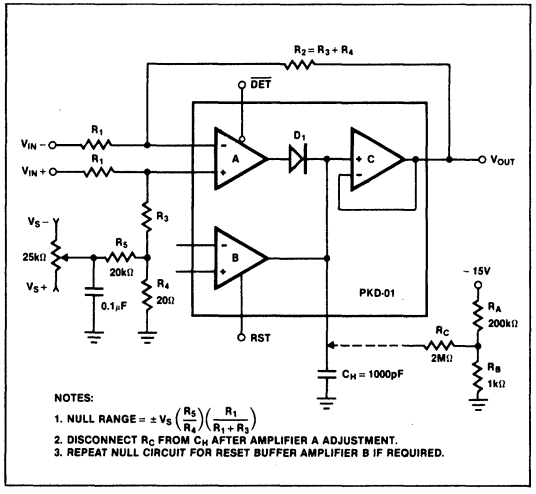


Figure B. V_{OS} Null Circuit for Differential Peak Detector.

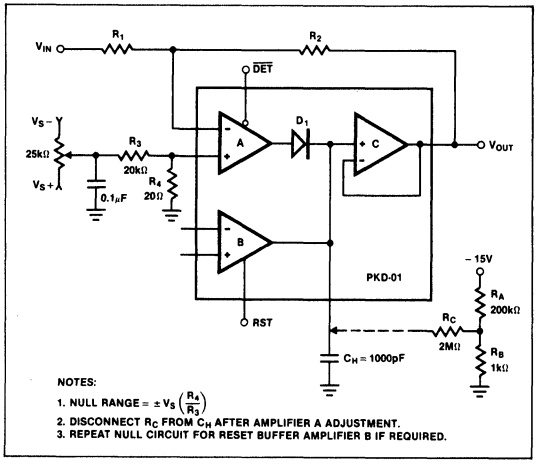


Figure C. V_{OS} Null Circuit for Negative Peak Detector.

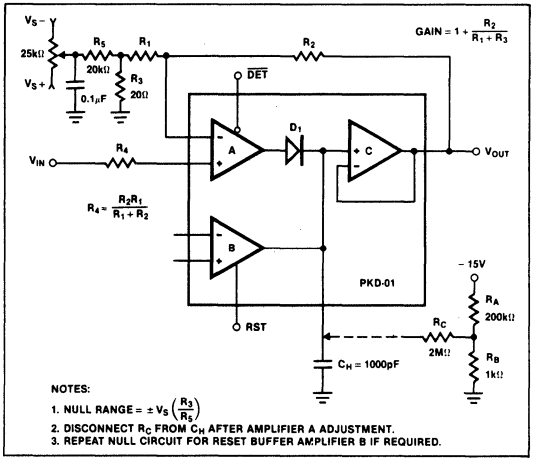


Figure D. V_{OS} Null Circuit for Positive Peak Detector With Gain.

PEAK HOLD CAPACITOR RECOMMENDATIONS

The hold capacitor (C_H) serves as the peak memory element and compensating capacitor. Stable operation requires a minimum value of 1000pF. Larger capacitors may be used to lower droop rate errors, but acquisition time will increase.

Zero scale error is internally trimmed for C_H = 1000pF. Other C_H values will cause a zero scale shift which can be approximated with the following equation.

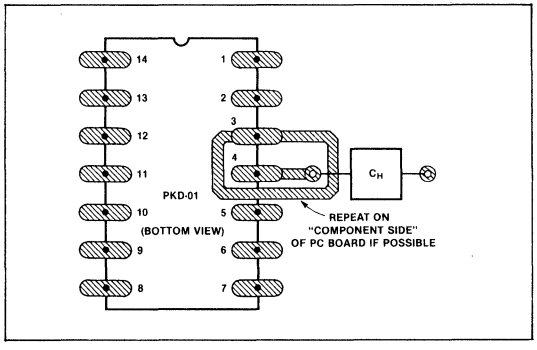
$$\Delta V_{ZS}(mV) = \frac{1 \times 10^3(pC)}{C_H(nF)} - 0.6mV$$

The peak hold capacitor should have very high insulation resistance and low dielectric absorption. For temperatures below 85 °C, a polystyrene capacitor is recommended, while a Teflon capacitor is recommended for high temperature environments.

CAPACITOR GUARDING AND GROUND LAYOUT

Ground planes are recommended to minimize ground path resistance. Separate analog and digital grounds should be used. The two ground systems are tied together only at the common system ground. Avoid digital currents returning to the system ground through the analog ground path.

The C_H terminal (Pin 4) is a high-impedance point since a transconductance amplifier is used as the input amplifier. To minimize gain errors and maintain the PKD-01's inherently low droop rate, guarding Pin 4 is recommended.



COMPARATOR OUTPUT

The comparator output high level (V_{OH}) is set by external resistors. It's possible to optimize noise immunity while interfacing to all standard logic families — TTL, DTL, and CMOS. Figure 1 shows the comparator output with external level setting resistors. Table I gives typical R_1 and R_2 values for common circuit conditions.

The maximum comparator high output voltage (V_{OH}) should be limited to:

$V_{OH}(maximum) < V^+ - 2.0V$

With the comparator in the low state (V_{OL}), the output stage will be required to sink a current approximately equal to V_C/R_1.

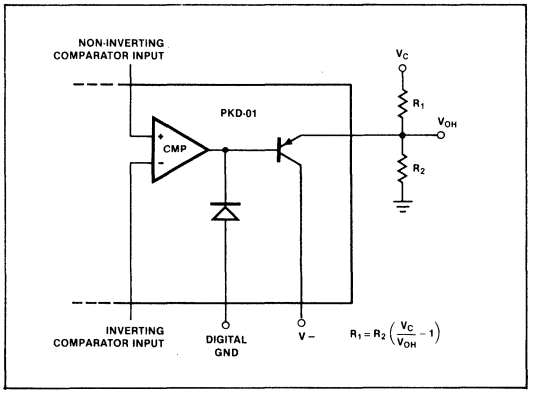


Figure 1.

Table 1.

V_C	V_{OH}	R_1	R_2
5	3.5	2.7K	6.2K
5	5.0	2.7K	∞
15	3.5	4.7K	1.5K
15	5.0	4.7K	2.4K
15	7.5	7.5K	7.5K
15	10.0	7.5K	15K

$$R_1 \approx \frac{V_C}{I_{sink}}$$

$$R_2 \approx R_1\left(\frac{1}{\frac{V_C}{V_{OH}} - 1}\right)$$

PEAK DETECTOR LOGIC CONTROL (RST, $\overline{DET}$)

The transconductance amplifier outputs are controlled by the digital logic signals RST and $\overline{DET}$. The PKD-01 operational mode is selected by steering the current (I_1) through Q_1 and Q_2, thus providing high-speed switching and a predictable logic threshold. The logic threshold voltage is 1.4 volts when digital ground is at zero volts.

Other threshold voltages (V_{TH}) may be selected by applying the formula:

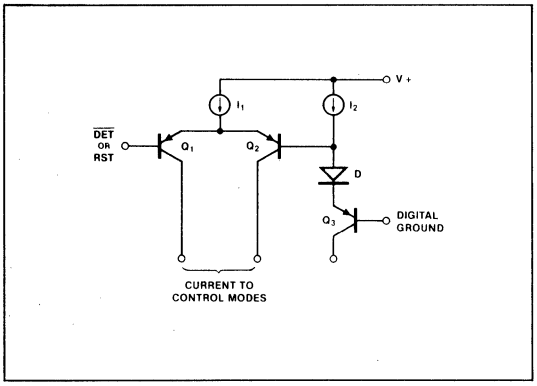
$V_{TH} \approx 1.4V$ + Digital Ground Potential.

For proper operation, digital ground must always be at least 3.5V below the positive supply and 2.5V above the negative supply. The RST or $\overline{DET}$ signal must always be at least 2.8V above the negative supply.

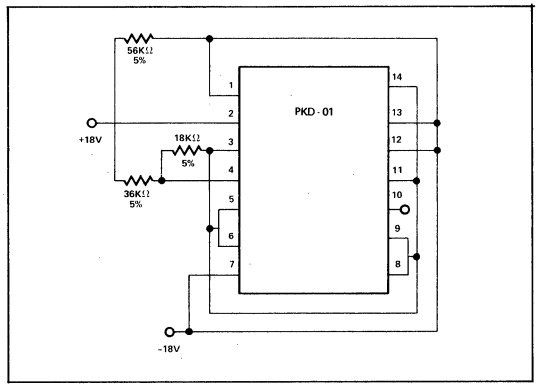
Operating the digital ground at other than zero volts does influence the comparator output low voltage. The V_{OL} level is reference to digital ground and will follow any changes in digital ground potential:

$V_{OL} \approx 0.2V$ + Digital Ground Potential.

PKD-01 LOGIC CONTROL

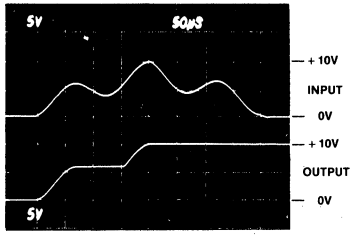


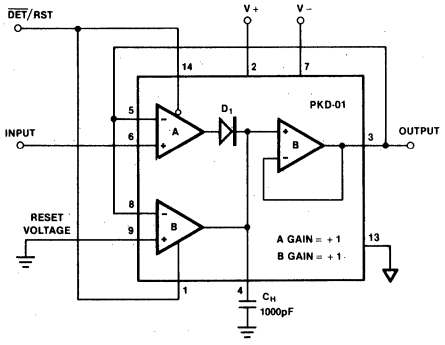
BURN-IN CIRCUIT



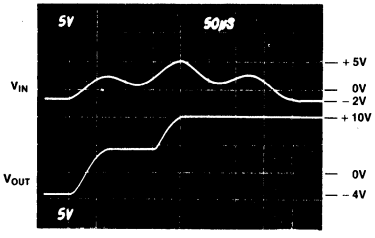
TYPICAL CIRCUIT CONFIGURATIONS

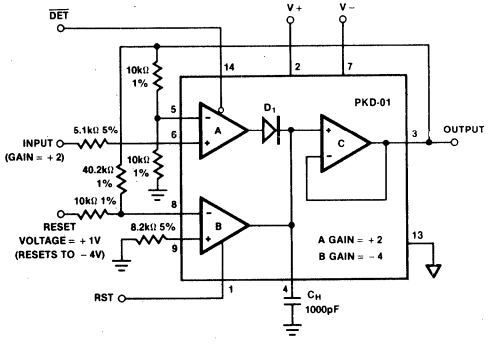
UNITY GAIN POSITIVE PEAK DETECTOR



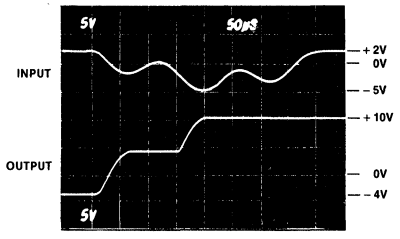


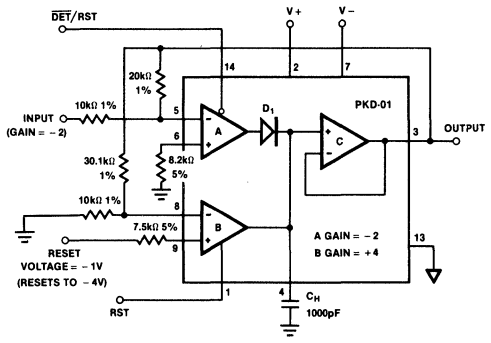
POSITIVE PEAK DETECTOR WITH GAIN



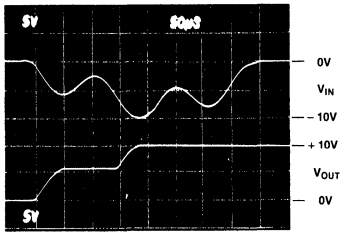


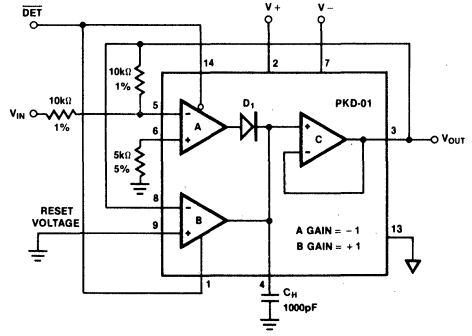
NEGATIVE PEAK DETECTOR WITH GAIN



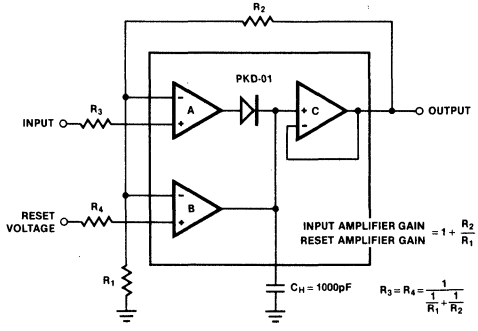


UNITY GAIN NEGATIVE PEAK DETECTOR



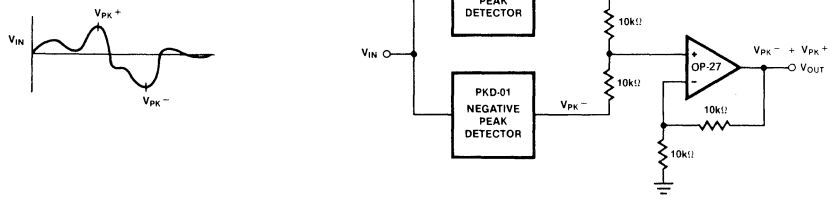


ALTERNATE GAIN CONFIGURATION

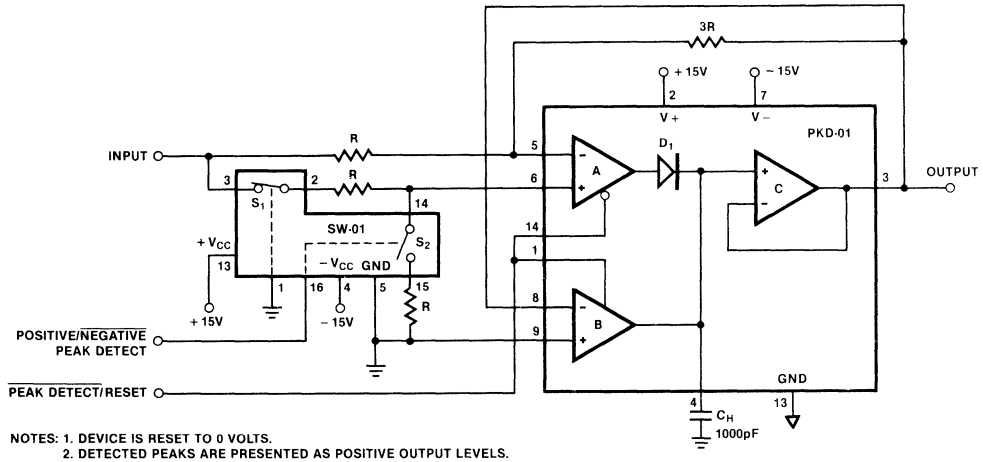


IF BOTH INPUT SIGNAL (AMPLIFIER A INPUT) AND THE RESET VOLTAGE (AMPLIFIER B INPUT) HAVE THE SAME POSITIVE VOLTAGE GAIN THE GAIN CAN BE SET BY A SINGLE VOLTAGE DIVIDER FOR BOTH INPUT AMPLIFIERS.

PEAK-TO-PEAK DETECTOR

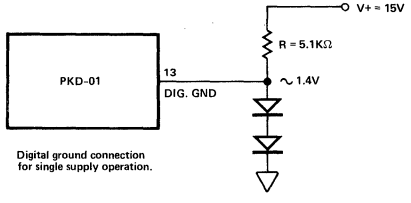


LOGIC SELECTABLE POSITIVE OR NEGATIVE PEAK DETECTOR



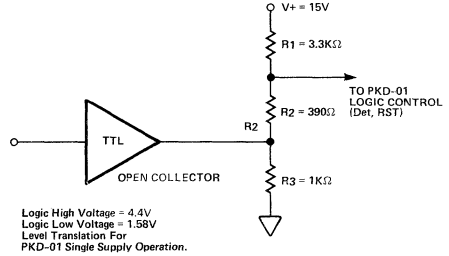
NOTES: 1. DEVICE IS RESET TO 0 VOLTS.
2. DETECTED PEAKS ARE PRESENTED AS POSITIVE OUTPUT LEVELS.
3. R = 10kΩ.
4. S_1 IS ALWAYS CLOSED TO COMPENSATE FOR VOLTAGE DIVIDER ERROR WHEN S_2 IS CLOSED.

DIGITAL GROUND CONNECTION FOR SINGLE SUPPLY OPERATION



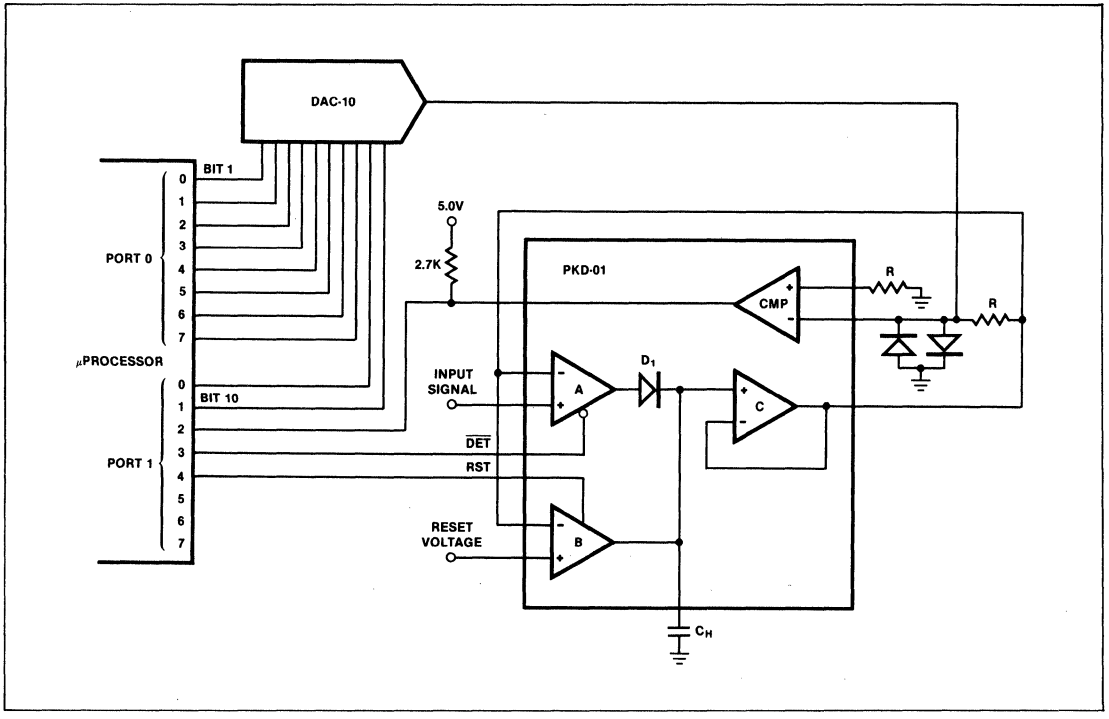
Digital ground connection for single supply operation.

LOGIC LEVEL TRANSLATION FOR PKD-01 SINGLE SUPPLY OPERATION

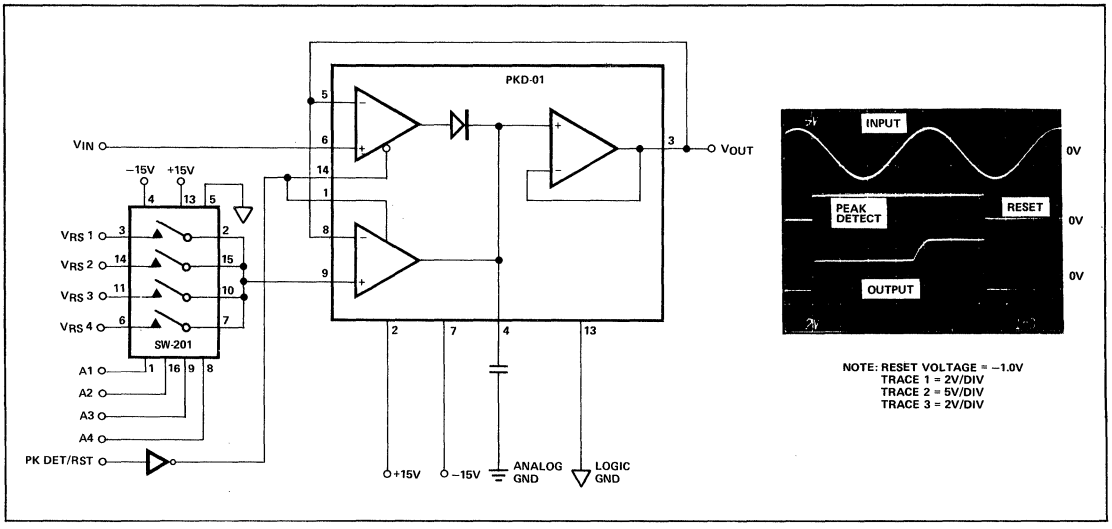


Logic High Voltage = 4.4V
Logic Low Voltage = 1.58V
Level Translation For
PKD-01 Single Supply Operation.

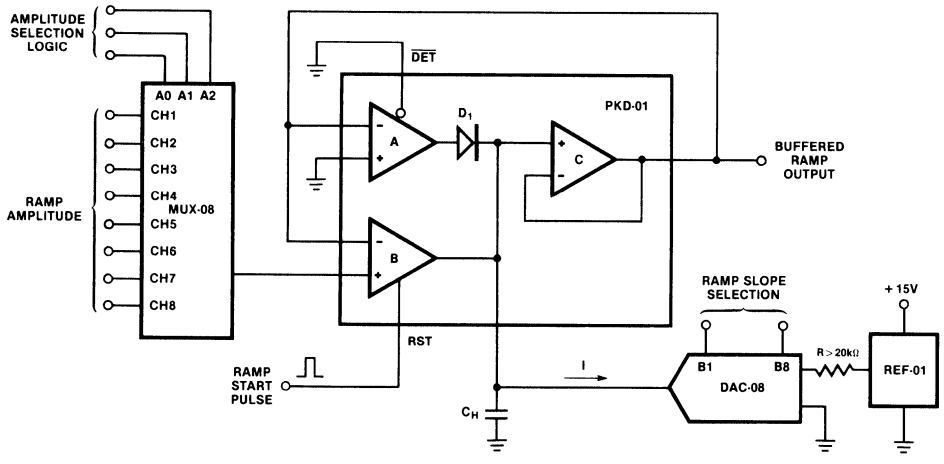
PEAK READING A/D CONVERTER

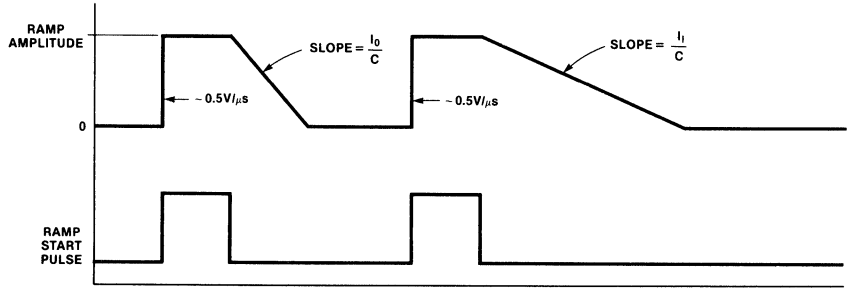


POSITIVE PEAK DETECTOR WITH SELECTABLE RESET VOLTAGE



PROGRAMMABLE LOW FREQUENCY RAMP GENERATOR





NOTES: 1. NEGATIVE SLOPE OF RAMP IS SET BY DAC-08 OUTPUT CURRENT.
2. DAC-08 IS DIGITALLY CONTROLLED CURRENT GENERATOR. THE MAXIMUM FULL SCALE CURRENT MUST BE LESS THAN 0.5mA.

SECTION 13

TELE-COMMUNICATIONS

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INTRODUCTION

The circuits described in this section are intended for, but not limited to, Telecommunication Applications. These circuits fill such applications as PCM CODECs, Repeaters, switching systems, etc. The components include: D/A Converters, Sample-and-Hold Amplifiers, Multiplexers/Demultiplexers and Repeaters. When used with references, comparators, operational amplifiers and other components in this catalog, they comprise the analog portion of many Telecommunications systems.Some components will bear a great resemblance to Devices listed elsewhere; e.g., the DAC-88 resembles the DAC-78. In fact, they are the same device with the exception that Telecommunications devices are selected and tested to parameters of interest to Telecommunications users and the industrial counterparts are specified for those parameters of interest to users in other industries.

Included in this section are a series of D/A converters: the DAC-86, DAC-87, DAC-88 and DAC-89. These devices are intended for use in Bell "255" companding law (DAC-86/88) Codec systems (U.S.) or "A" companding law (DAC-87/89) response for use in European systems. In conjunction with these systems, other devices available for use in codecs are: the SMP81 Sample-and-Hold Amplifier, the MUX88 8-channel Analog Multiplexer, and the DMX-88 8-channel Demultiplexer. Standard industrial devices which may be used with these specialized devices are: CMP01/CMP05 Comparators, REF01/REF02 Voltage Reference, and OP01, OP15, OP 37 operational amplifiers (to name a few).

Also included in this section are the RPT81 and RPT82 PCM Carrier Repeater. These devices can also be used as clock regeneration circuits in non-telephony applications.

Complete data, as well as applications ideas are given for all devices.

FOR EXISTING DESIGNS ONLY
FOR NEW DESIGNS SEE DAC-88

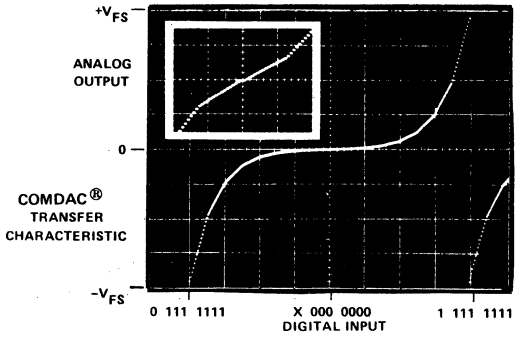
DAC-86

COMDAC® COMPANDING D/A CONVERTER

μ - 255 LAW DAC

FEATURES

- Conforms With Bell System μ-255 Companding Law
- Meets D3 Compandor Tracking Specifications
- Both Encode and Decode Capability
- Tight Full Scale Tolerance Eliminates Calibration
- Low Full Scale Drift Over Temperature
- Extremely Low Noise Contribution
- Multiplying Reference Inputs
- Simplifies PCM System Design
- High Reliability
- Low Power Consumption and Low Cost



GENERAL DESCRIPTION

The DAC-86 monolithic COMDAC® D/A Converter provides a 15 segment linear approximation to the Bell System μ-255 companding law. The law is implemented by using three bits to select one of eight binarily-related chords (or segments) and four bits to select one of sixteen linearly-related steps within each chord. A sign bit determines signal polarity, and an encode/decode select bit determines encode or decode operation.

Accuracy is assured by specifying chord end point values, step nonlinearity, and monotonicity over the full operating temperature range. Typical applications include PCM carrier systems, digital PBX's, intercom systems, and PCM recording. For CCITT "A" Law models, refer to the DAC-87/89 data sheet.

BELL μ-255 LAW TRANSFER CHARACTERISTIC

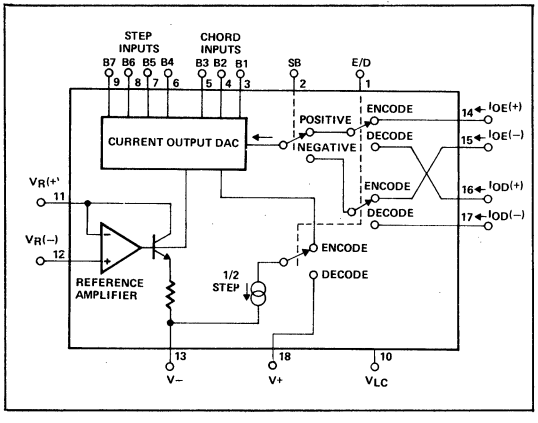
The transfer characteristic of the DAC-86 is a piecewise linear approximation to the Bell System μ-25 law expressed by:

$$Y(\chi) = \mathrm{sgn}(\chi)\,\frac{\ln(1+\mu|\chi|)}{\ln(1+\mu)} \quad -1 \le \chi \le 1$$

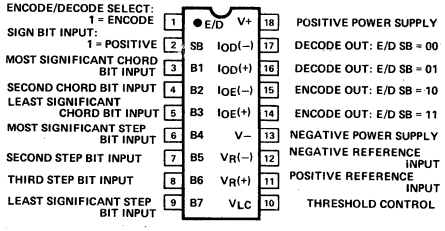
for a normalized coding range of ±1
where: χ = input signal level
Y = output compressed signal level
μ = 255

This law is implemented by the DAC-86 with an eight chord (or segment) piecewise linear approximation with 16 linear steps in each chord for both polarities. Dynamic range of 72dB in both polarities is achieved with eight-bit coding.

EQUIVALENT CIRCUIT AND PIN CONNECTION DIAGRAM



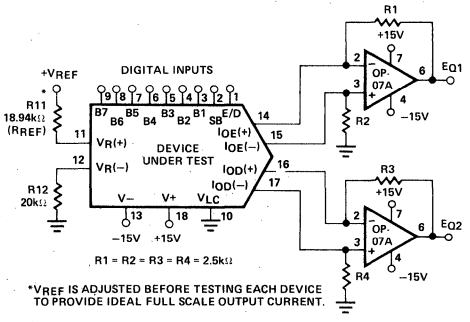
PIN CONNECTIONS & ORDERING INFORMATION



18 PIN HERMETIC DUAL-IN-LINE
(X-Suffix)

ACCURACY	
±1/2 STEP	DAC-86EX
±1 STEP	DAC-86CX

OUTPUT CURRENT DC TEST CIRCUIT



*VREF IS ADJUSTED BEFORE TESTING EACH DEVICE TO PROVIDE IDEAL FULL SCALE OUTPUT CURRENT.

LINE SELECTION TABLE

TEST GROUP	ENCODE/ DECODE	SIGN BIT	OUTPUT MEASUREMENT	
1	1	1	$I_{OE}(+)$	(E_{01}/R1)
2	1	0	$I_{OE}(-)$	(E_{01}/R2)
3	0	1	$I_{OD}(+)$	(E_{02}/R3)
4	0	0	$I_{OD}(-)$	(E_{02}/R4)

NOTE: Accuracy is specified in the test circuit using the tables below to be within the specified proportion of a step at the maximum value in each chord. Monotonic operation is guaranteed for all input codes.

CONDENSED CURRENT OUTPUT TABLES (I_{REF} = 528μA)

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

STEP \ CHORD		0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0	8.25	24.75	57.75	123.75	255.75	519.75	1047.75
15	1111	7.5	23.25	54.75	117.75	243.75	495.75	999.75	2007.75
STEP SIZE		0.50	1	2	4	8	16	32	64

IDEAL ENCODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

STEP \ CHORD		0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0.25	8.75	25.75	59.75	127.75	263.75	535.75	1079.75
15	1111	7.75	23.75	55.75	119.75	247.75	503.75	1015.75	2039.75
STEP SIZE		0.50	1	2	4	8	16	32	64

These tables may be extended to include all of the encode/decode currents (ideal with SI_{REF} = 528μA) by multiplying any of the numbers in the normalized tables by 0.5μA.

SPECIFICATION PARAMETER DEFINITIONS

FULL SCALE DRIFT

The change in output current over the full operating temperature with V_{REF} = 10.000V, R11 = 18.94kΩ, and R12 = 20kΩ.

FULL SCALE SYMMETRY ERROR

The difference between $I_{OD}(-)$ and $I_{OD}(+)$ or the difference between $I_{OE}(-)$ and $I_{OE}(+)$ at full scale output.

OUTPUT VOLTAGE COMPLIANCE

The maximum output voltage swing at any current level which causes < ½ step change in output current.

CHORDS

Groups of linearly-related steps in the transfer function. Also known as segments.

CHORD ENDPOINTS

The maximum code in each chord. Used to specify accuracy.

STEPS

Increments in each chord which divides it into 16 equal levels.

OUTPUT LEVEL NOTATION

Each output current level may be designated by the code $I_{C,S}$ where C = chord number and S = step number. For example, $I_{0,0}$ = zero scale current; $I_{0,1}$ = first step from zero; $I_{0,15}$ = endpoint of first chord (C_0); $I_{7,15}$ = full scale current.

DYNAMIC RANGE

Ratio of the largest output ($I_{7,15}$) to the smallest output excluding zero ($I_{0,1}$) expressed in dB. This can be measured peak or peak-to-peak with the same result.

ABSOLUTE MAXIMUM RATINGS

V+ Supply to V− Supply 36V
V_{LC} Swing ..... V− plus 8V to V+
Analog Current Outputs ..... V− plus 8V to V− plus 36V
Reference Inputs ..... V− to V+
Reference Input Differential Voltage ..... ±18V
Reference Input Current 1.25mA
Logic Inputs ..... V− plus 8V to V− plus 36V
Operating Temperature ..... −25°C to +85°C
Storage Temperature ..... −65°C to +150°C
Power Dissipation 500mW
Derate above 100°C ..... 10mW/°C
Lead Soldering Temperature ..... 300°C (60 sec)

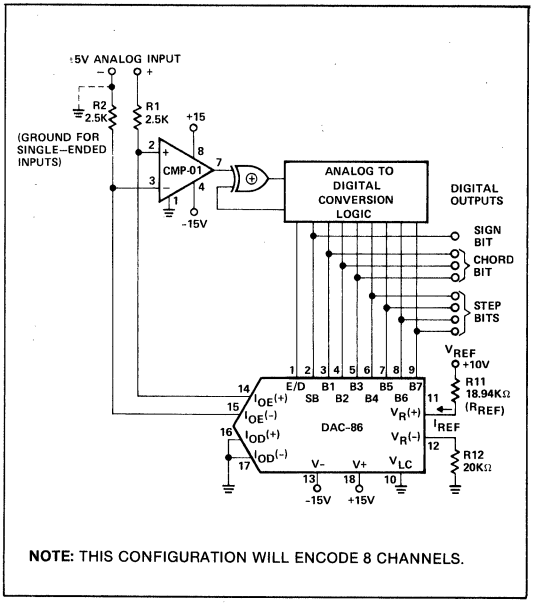
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 528\mu A$, $-25°C \leq T_A \leq +85°C$, and for all 4 outputs, unless otherwise noted.

			DAC-86-E			DAC-86-C			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Resolution		8 chords with 16 steps each	±128	±128	±128	±128	±128	±128	Steps
Dynamic Range		20 log ($I_{7,15}/I_{0,1}$)	72	72	72	72	72	72	dB
Monotonicity		Sign Bit + or −	128	—	—	128	—	—	Steps
Chord Endpoint Accuracy All Chords		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	—	—	±1/2	—	—	±1	Step
Encode Decision Level Current		Additional output encode/decode = 1	3/8	1/2	5/8	1/4	1/2	3/4	Step
Settling Time	t_s	To within ±1/2 step	—	1.0	see note	—	1.0	see note	μsec
Full Scale Drift (C_7)	ΔI_{FS}	Full temperature range	—	±1/16	±1/10	—	±1/10	±1/4	Step
Output Voltage Compliance	V_{OC}	Full scale current change ≤1/2 step	−5	—	+18	−5	—	+18	Volts
Full Scale Symmetry Error	$I_O(+) - I_O(-)$	Decode or encode pair Input Code 111 1111	—	±1/40	±1/8	—	±1/40	±1/4	Step
Zero Scale Current (C_0)	I_{ZS}	Measured at selected output with 000 0000 input	—	1/40	1/8	—	1/40	1/4	Step
Disable Current (All bits high)	I_{DIS}	Leakage of output disabled by E/D and SB	—	5.0	75	—	5.0	75	nA
Step Accuracy All Chords		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	—	—	±1/2	—	—	±1	Step
Output Current Range	I_{FSR}		0	2.0	4.2	0	2.0	4.2	mA
Logic Input Levels, Logic "0"	V_{IL}	$V_{LC} = 0V$	—	—	0.8	—	—	0.8	Volts
Logic Input Levels, Logic "1"	V_{IH}	$V_{LC} = 0V$	2.0	—	—	2.0	—	—	Volts
Logic Input Current	I_{IN}	$V_{IN} = -5V$ to +18V	—	—	120	—	—	120	μA
Logic Input Swing	V_{IS}	V− = −15V	−5	—	+18	−5	—	+18	Volts
Reference Bias Current	I_{12}		—	−3.0	−12.0	—	−3.0	−12.0	μA
Reference Input Slew Rate	dI/dt		—	0.25	—	—	0.25	—	mA/μs
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	$PSSI_{FS+}$	V+ = 4.5 to 18V, V− = −15V	—	±1/20	±1/2	—	±1/20	±1/2	Step
	$PSSI_{FS-}$	V− = −10.8V to −18V, V+ = 15V	—	±1/10	±1/2	—	±1/10	±1/2	Step
Power Supply Current	I+	$V_S = +5V, -15V, I_{FS} = 2.0mA$	—	2.7	4.5	—	2.7	4.5	mA
	I−	$V_S = +5V, -15V, I_{FS} = 2.0mA$	—	−6.7	−9.3	—	−6.7	−9.3	mA
	I+	$V_S = \pm 15V, I_{FS} = 2.0mA$	—	2.7	4.5	—	2.7	4.5	mA
	I−	$V_S = \pm 15V, I_{FS} = 2.0mA$	—	−6.7	−9.3	—	−6.7	−9.3	mA
Power Dissipation	P_D	$V_S = +5V, -15V, I_{FS} = 2.0mA$	—	114	167	—	114	167	mW
	P_D	$V_S = \pm 15V, I_{FS} = 2.0mA$	—	141	207	—	141	207	mW

NOTE:
In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) step size is 0.5μA, while in the last chord near full scale (C_7) step size is 64μA. Settling time varies for each of the chord bits and step bits and a maximum specification is misleading. In decode operation, the DAC-86 and OP-16 combination will decode eight channels. In the encode mode, the DAC-86 and CMP-01 combination will encode eight channels. Both encode and decode statements assume a 5.2μsec channel time.

BASIC ENCODE OPERATION (COMPRESSING A/D CONVERSION)

BASIC ENCODE CONNECTIONS



NOTE: THIS CONFIGURATION WILL ENCODE 8 CHANNELS.

ENCODE DECISION LEVELS

Compressing A/D conversion with the DAC-86 requires a comparator, an exclusive-or gate, and a successive approximation register — the usual elements in any sign-plus-magnitude A/D converter. However, a compressing ADC has one signficant difference from regular A/D converters.

In a conventional (linear converter), the step size is a constant percentage of full scale, but in a compressing A/D converter, the step size increases as the output changes from zero scale to full scale.

When the DAC is used in the feedback loop of a successive approximation ADC the DAC outputs are used as decision levels to determine the edges of the quantizing bands. When the DAC is used in the decode mode it follows that the outputs must correspond to the center of the quantizing bands. Thus the encode mode output must exceed the decode mode output by one-half step. See AN 39 for further explanation.

ENCODING SEQUENCE

An encoding sequence begins with the sign bit decision. During this time the comparator is a polarity detector only. The Encode/Decode (E/D) input is held at a logic "0", so that no current flows into the encode outputs, and the comparator is effectively disconnected from the DAC. Once the input polarity has been determined, the E/D input is changed to a logic "1" allowing current to flow into $I_{OE}(+)$ or $I_{OE}(-)$ depending upon the Sign Bit Answer.

For positive inputs, current flows into $I_{OE}(+)$ through R1, and the comparator's output will be entered as the answer for each successive decision. For negative inputs, current flows into $I_{OE}(-)$ through R2 developing a negative voltage which is compared with the analog input. An exclusive-OR gate inverts the comparator's output during negative trials

NORMALIZED ENCODE LEVEL (SIGN BIT EXCLUDED) $I_{C,S} = 2[2^C (S + 17) - 16.5]$

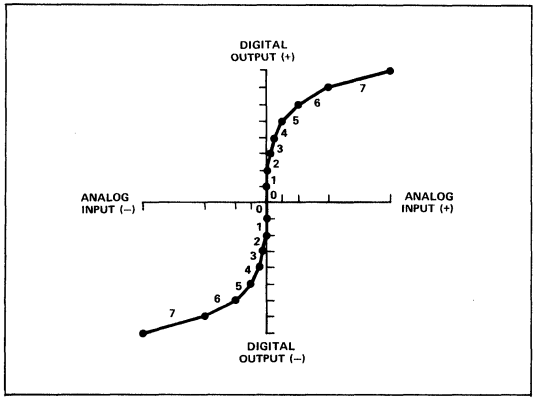
C = chord no. (0 through 7)
S = step no. (0 through 15)

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	1	35	103	239	511	1055	2143	4319
1	0001	3	39	111	255	543	1119	2271	4575
2	0010	5	43	119	271	575	1183	2399	4831
3	0011	7	47	127	287	607	1247	2527	5087
4	0100	9	51	135	303	639	1311	2655	5343
5	0101	11	55	143	319	671	1375	2783	5599
6	0110	13	59	151	335	703	1439	2911	5855
7	0111	15	63	159	351	735	1503	3039	6111
8	1000	17	67	167	367	767	1567	3167	6367
9	1001	19	71	175	383	799	1631	3295	6623
10	1010	21	75	183	399	831	1695	3423	6879
11	1011	23	79	191	415	863	1759	3551	7135
12	1100	25	83	199	431	895	1823	3679	7391
13	1101	27	87	207	447	927	1887	3807	7647
14	1110	29	91	215	463	959	1951	3935	7903
15	1111	31	95	223	479	991	2015	4063	8159
STEP SIZE		2	4	8	16	32	64	128	256

to maintain the proper logic coding, all ones for full scale and all zeros for zero scale. (A more complete schematic is shown in the applications section).

The bits are converted with a successive removal technique, starting with a decision at the code 011 1111 and turning off bits sequentially until all decisions have been made.

ENCODE TRANSFER CHARACTERISTICS (A/D CONVERSION)



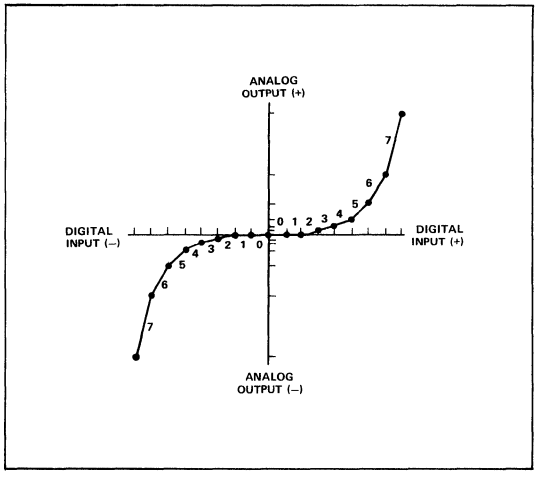
BASIC DECODE OPERATION (EXPANDING D/A CONVERSION)

DECODE OPERATION

D/A conversion with the DAC-86 may be illustrated by using an operational amplifier connected to the decode outputs.

The decode mode of operation is selected by applying a logic "0" to the Encode/Decode input. This enables the I_{OD} outputs, disables the I_{OE} outputs and, allows $I_{OD}(+)$ or $I_{OD}(-)$ to be selected by the Sign Bit input. When the Sign Bit input is high, a logic "1", all of the output current flows into $I_{OD}(+)$ forcing a positive voltage at the operational amplifier's output. When the Sign Bit input is low, a logic "0", all of the output current flows into $I_{OD}(-)$ through R2 forcing a negative voltage output. Since the Sign Bit only steers current into $I_{OD}(+)$ or $I_{OD}(-)$, the output will always be symmetrical, limited only by the matching of R1 and R2.

DECODE TRANSFER CHARACTERISTIC (D/A CONVERSION)



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TELECOMMUNICATIONS DAC-86

NORMALIZED DECODE OUTPUT (SIGN BIT EXCLUDED) $I_{C,S} = 2[2^C (S + 16.5) - 16.5]$

C = chord no. (0 through 7)
S = step no. (0 through 15)

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	33	99	231	495	1023	2079	4191
1	0001	2	37	107	247	527	1087	2207	4447
2	0010	4	41	115	263	559	1151	2335	4703
3	0011	6	45	123	279	591	1215	2463	4959
4	0100	8	49	131	295	623	1279	2591	5215
5	0101	10	53	139	311	655	1343	2719	5471
6	0110	12	57	147	327	687	1407	2847	5727
7	0111	14	61	155	343	719	1471	2975	5983
8	1000	16	65	163	359	751	1535	3103	6239
9	1001	18	69	171	375	783	1599	3231	6495
10	1010	20	73	179	391	815	1663	3359	6751
11	1011	22	77	187	407	847	1727	3487	7007
12	1100	24	81	195	423	879	1791	3615	7263
13	1101	26	85	203	439	911	1855	3743	7519
14	1110	28	89	211	455	943	1919	3871	7775
15	1111	30	93	219	471	975	1983	3999	8031
STEP SIZE		2	4	8	16	32	64	128	256

NORMALIZED TABLES

The encode and decode tables may be used to calculate ideal output current at any point. For example, in decode mode at $I_{3,7}$ (011 0111) find 343. 343/8031 times I_{FS} of 2007.75μA equals 85.75μA. Alternatively, use the condensed current tables and add up the number of steps.

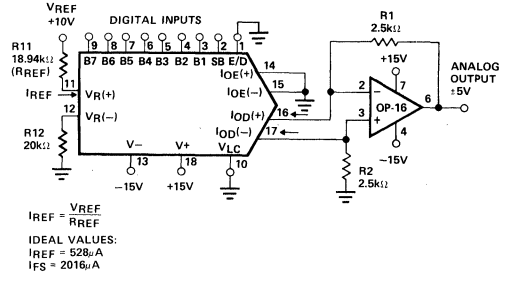
BASIC REFERENCE CONSIDERATIONS

Full scale output current is ideally 2007.75μA when the reference current is 528μA in the decode mode. In the encode mode it is 2039.75μA because the additional 1/2 step adds 32μA to the output. A percentage change in I_{REF} caused by changes in V_{REF} or R_{REF} will produce the same percentage change in output current.

The large step size at full scale allows the use of inexpensive references in many applications. In some situations V_{REF} may even be the positive power supply. For example, with V+ = 15V, R_{REF} = 15V/528μA or 28.4kΩ. When using a power supply as a reference, R11 should be two resistors, R11A and R11B, and the junction should be bypassed to ground to provide decoupling.

	E/D	SB	B1	B2	B3	B4	B5	B6	B7	E_0
POS FULL SCALE	0	1	1	1	1	1	1	1	1	5.019V
(+) ZERO SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.0012
(+) ZERO SCALE	0	1	0	0	0	0	0	0	0	0V
(−) ZERO SCALE	0	0	0	0	0	0	0	0	0	0V
(−) ZERO SCALE +1 STEP	0	0	0	0	0	0	0	0	1	−0.0012
NEG FULL SCALE	0	0	1	1	1	1	1	1	1	−5.019V

BASIC DECODE CONNECTIONS



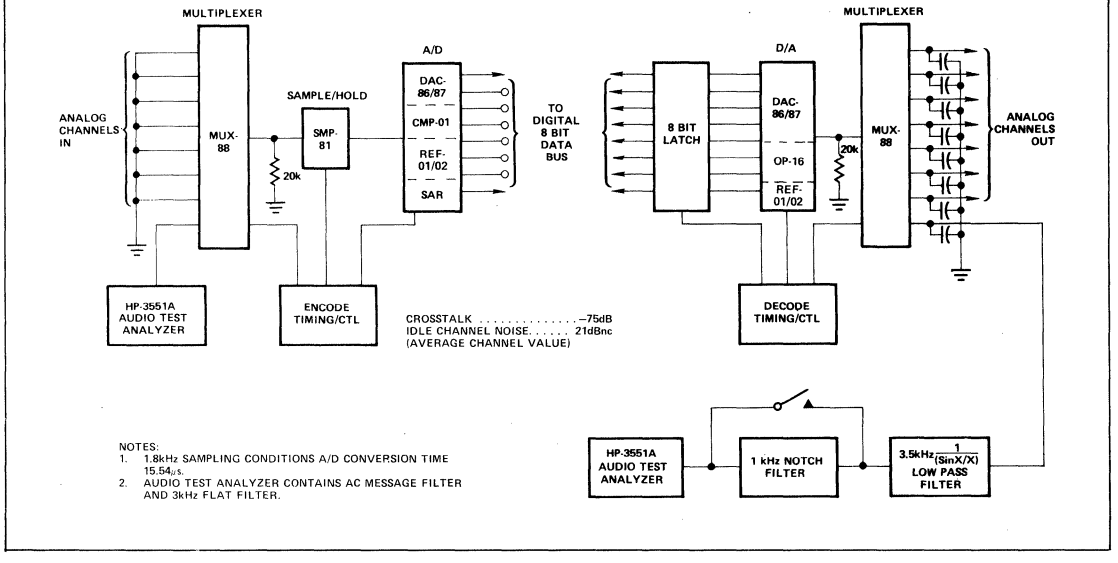
NOTE: THIS CONFIGURATION WILL DECODE 24 CHANNELS.

REFERENCE AMPLIFIER SETUP

The DAC-86 is a multiplying D/A converter in which the output current is the product of the normalized digital input and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full scale output current is a linear function of the reference current and is given for all four outputs in the figures above.

In positive reference applications an external positive reference voltage forces current through R11 into the $V_R(+)$ terminal (pin 11) of the reference amplifier. Alternatively, a negative reference may be applied to $V_R(-)$ at pin 12; reference current flows from ground through R11 into $V_R(+)$, as in the positive reference case. This negative reference connection has the advantage of a very high impedance

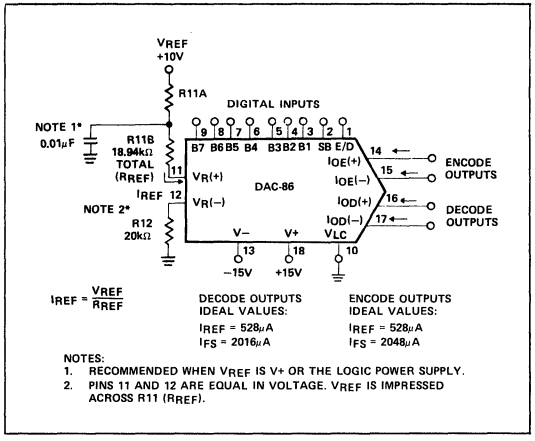
SYSTEM TEST CIRCUIT



NOTES:
1. 1.8kHz SAMPLING CONDITIONS A/D CONVERSION TIME 15.54μs.
2. AUDIO TEST ANALYZER CONTAINS AC MESSAGE FILTER AND 3kHz FLAT FILTER.

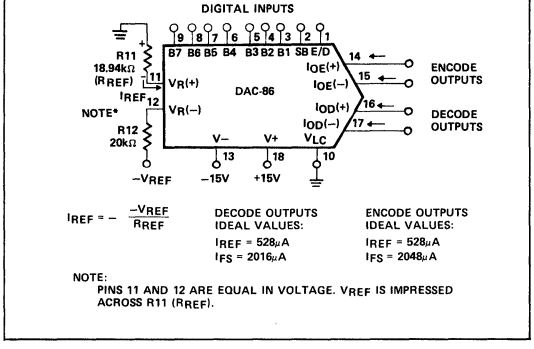
presented at pin 12. The voltage at pin 11 is equal to and tracks the voltage at pin 12 due to the high gain of the internal reference amplifier. R12 (nominally equal to R11) is used to cancel bias current errors and may be eliminated with only a minor increase in error.

POSITIVE REFERENCE OPERATION



NOTES:
1. RECOMMENDED WHEN V_{REF} IS V+ OR THE LOGIC POWER SUPPLY.
2. PINS 11 AND 12 ARE EQUAL IN VOLTAGE. V_{REF} IS IMPRESSED ACROSS R11 (R_{REF}).

NEGATIVE REFERENCE OPERATION



NOTE:
PINS 11 AND 12 ARE EQUAL IN VOLTAGE. V_{REF} IS IMPRESSED ACROSS R11 (R_{REF}).

REFERENCE AMPLIFIER OPERATION

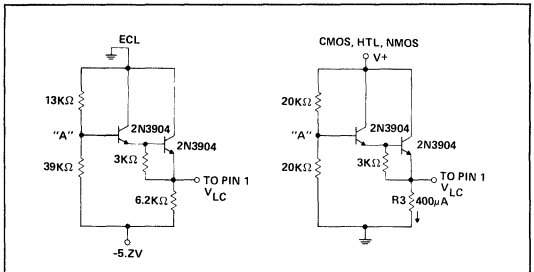
REFERENCE RECOMMENDATIONS

For most applications a +10.0V reference, such as the PMI REF-81, is recommended for optimum full scale temperature coefficient performance. (This also minimizes the contributions of reference amplifier V_{OS} and TCV_{OS}.) For most applications the tight relationship between I_{REF} and I_{FS} eliminates the need for trimming I_{REF}; but if desired full scale trimming may be accomplished by selecting R11 or by using a potentiometer for R11.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common mode range. While the recommended operating range of DC reference currrent is 0.1mA to 1.0mA, monotonic operation is maintained over an even wider range.

LOGIC INPUT AND POWER SUPPLY CONSIDERATIONS

INTERFACING CIRCUIT FOR ECL, CMOS, HTL, AND NMOS LOGIC INPUTS



NOTES:
1. SET THE VOLTAGE "A" TO BE AT THE DESIRED LOGIC INPUT SWITCHING THRESHOLD.
2. ALLOWABLE RANGE OF LOGIC THRESHOLD IS TYPICALLY −5V TO +13V WHEN OPERATING THE DAC-86 ON ±15V SUPPLIES.

LOGIC INPUTS

The DAC-86 may be interfaced with other-than-TTL logic by placing V_{LC} (pin 10) at a potential which is 1.4V below the desired logic input switching threshold. However, this voltage source must be capable of sourcing and sinking a changing current at pin 10.

The negative voltage at the logic inputs must be limited to +10V with respect to V− (pin 13).

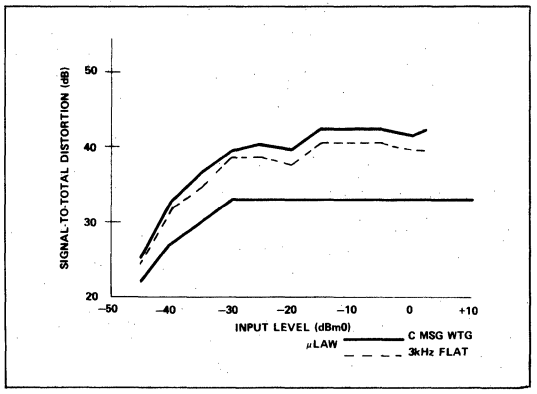
POWER SUPPLIES

Power supply current drain is relatively independent of voltage and temperature and completely independent of the logic input states.

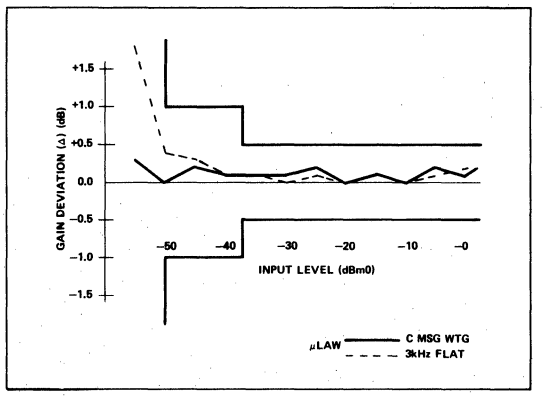
When operating with V− between −15V and −11V, output negative voltage compliance, $V_{OC}(-)$, reference input amplifier common mode voltage range, and logic input negative voltage range are reduced by an amount equivalent to the difference between −15V and the V− supply in use. Operation with V+ between +5V and +15V affects V_{LC} and the reference amplifier common mode positive voltage range in the same manner.

SYSTEM PERFORMANCE CURVES

SIGNAL TO QUANTIZING DISTORTION vs INPUT LEVEL



GAIN TRACKING



OUTPUT VOLTAGE COMPLIANCE

The DAC-86 has true current outputs with wide voltage compliance enabling fast drive of a variety of single ended and balanced loads. Positive voltage compliance is +18V and negative voltage compliance is −5.0V with $I_{REF} = 528\mu A$ and V = −15V. Negative voltage compliance $V_{OC}(-)$ for other values of I_{REF} and V− may be obtained from the table, or calculated as follows:

$$V_{OC}(-)\ \text{min} = (V-) + (2\ I_{REF}\ X\ 1.6k\Omega) + 8.4V$$

Output voltage compliance can be extended in both encode and decode modes using the connections shown below.

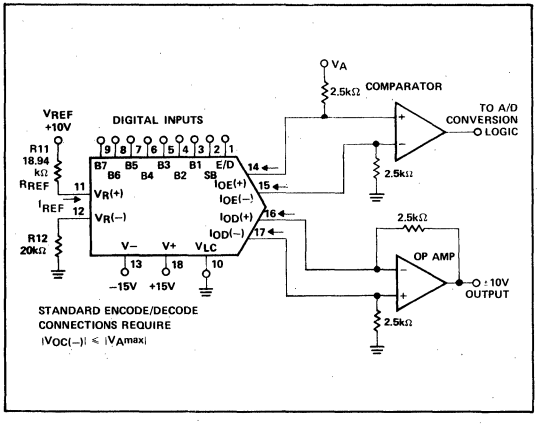
NEGATIVE OUTPUT VOLTAGE COMPLIANCE $V_{OC}(-)$

V− \ I_{FS}	1.0mA	2.0mA	4.0mA
−12V	−2.8V	−2.0V	−0.4V
−15V	−5.8V	−5.0V	−3.4V
−18V	−8.8V	−8.0V	−6.4V

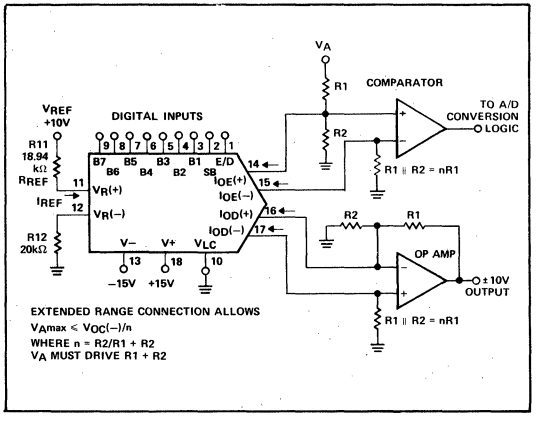
MINIMUM NEGATIVE COMPLIANCE

$V_{OC}(-)\ MIN = (V-) + (2\ I_{REF}\ 1.6k\Omega) + 8.4V$

STANDARD OUTPUT CONNECTIONS



OUTPUT COMPLIANCE EXTENSION CONNECTIONS



DICE

For applicable DICE information see DAC-76 Data Sheet.

FOR EXISTING DESIGNS ONLY

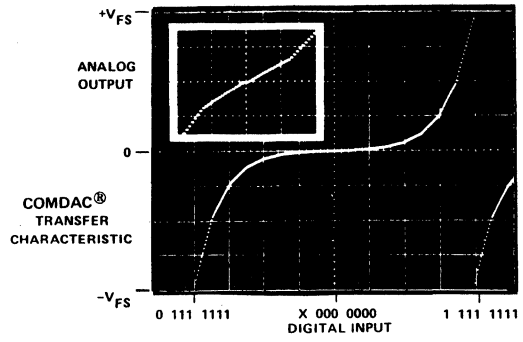
FOR NEW DESIGNS SEE DAC-89

DAC-87

COMDAC® COMPANDING D/A CONVERTER

FEATURES

- Conforms with CCITT "A" Companding Law
- Sign Plus 11-Bit Range with Sign Plus 7-Bit Coding
- 11-Bit Accuracy and Resolution Around Zero
- Sign Plus 66dB Dynamic Range
- True Current Outputs: −5V to +18V Compliance
- Tight Full Scale Tolerance Eliminates Calibration
- Low Full Scale Drift Over Temperature
- Low Power Consumption and Low Cost
- Ideal for PCM and 8-Bit μP Applications
- Outputs Multiplexed for Time Shared Applications



GENERAL DESCRIPTION

The DAC-87 monolithic COMDAC® D/A Converter provides the complete decode function for "A" Law PCM CODECs. The DAC-87 may be configured in an encoder, as a decoder, or may be timeshared between encoding and decoding.

Accuracy is assured by specifying chord end point values, chord nonlinearity, and monotonicity over the full operating temperature range. For companding D/A converters with Bell μ-255 law conformance, refer to the DAC-86/88 data sheets. For non-telecommunications applications, see the DAC-78 data sheet.

CCITT "A" LAW CHARACTERISTIC

The output of the DAC-87 is an approximation to the CCITT "A" law which can be expresed as:

$$Y = \frac{1 + \ln AX}{1 + \ln A} \quad 1/A \leq X \leq 1$$

$$Y = \frac{AX}{1 + \ln A} \quad 0 \leq X \leq 1/A \text{ where:}$$

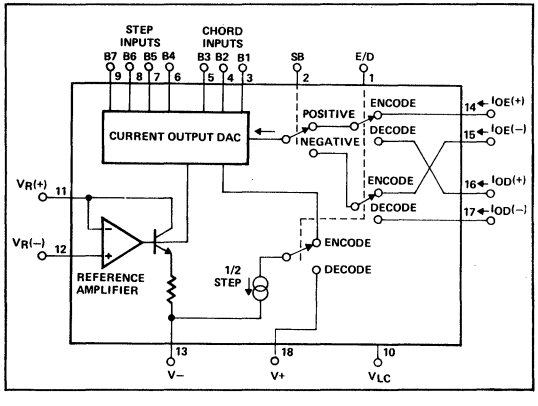
X = Normalized input signal level of the compressor (encoder), V_{IN}/V_{FS}.

Y = Output signal level of the compressor (encoder).

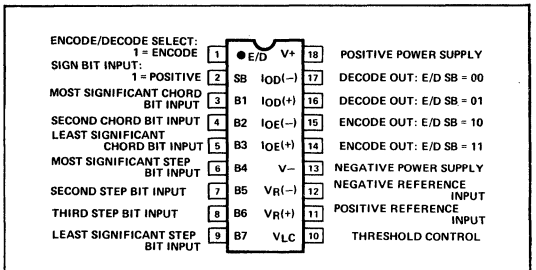
A = 87.6

This law is implemented by the DAC-87 with an eight chord (or segment) piecewise linear approximation for each polarity with sixteen linear steps in each chord. The first two chords are co-linear and of equal step size, and may be considered as one chord of 32 steps. Step sizes of the remaining six chords are binarily related to the first chord.

EQUIVALENT CIRCUIT



PIN CONNECTIONS & ORDERING INFORMATION



TOP VIEW

18-PIN HERMETIC DUAL-IN-LINE (X-Suffix)

ACCURACY

±1/2 STEP	DAC-87EX
±1 STEP	DAC-87CX

ABSOLUTE MAXIMUM RATINGS

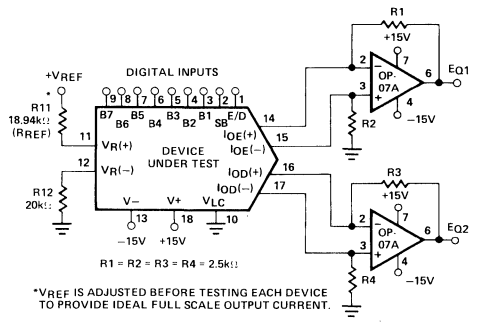
V+ Supply to V− Supply 36V
V_{CL} Swing ..... V− plus 8V to V+
Analog Current Outputs ..... V− plus 8V to V− plus 36V
Reference Inputs ..... V− to V+
Reference Input Differential Voltage ..... ±18V
Reference Input Current 1.25mA
Logic Inputs ..... V− plus 8V to V− plus 36V
Operating Temperature Range ..... −25°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Power Dissipation 500mW
Derate about 100°C ..... 10mW/°C
Lead Soldering Temperature (60 sec.) ..... 300°C

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 528\mu A$, $-25°C \leq T_A \leq +85°C$, and for all 4 outputs unless otherwise noted. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) step size is 1.0μA, while in the last chord near full scale (C_7) step size is 64μA.

			DAC-87-E			DAC-87-C			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Resolution		8 chords with 16 steps each	±128	—	±128	±128	—	±128	Steps
Dynamic Range		20 log ($I_{7,15}/I_{0,0}$)	66	—	66	66	66	66	dB
Monotonicity		Sign Bit + or −	128	—	—	128	—	—	Steps
Chord Endpoint Accuracy All Chords		Error relative to ideal values at $I_{FS} = 2016\mu A$	—	—	±1/2	—	—	±1	Step
Step Accuracy All Chords		Error relative to ideal values at $I_{FS} = 2016\mu A$	—	—	±1/2	—	—	±1	Step
Encode Current		Additional output Encode/Decode = 1	1/4	1/2	3/4	1/4	1/2	3/4	Step
Settling Time (Note)	t_s	To within ±1/2 step	—	1.0	—	—	—	—	μsec
Full Scale Drift	ΔI_{FS}	Full temperature range	—	±1/20	±1/4	—	±1/10	±1/2	Step
Output Voltage Compliance	V_{OS}	Full scale current change ≤1/2 step	−5	—	+18	−5	—	+18	Volts
Full Scale Current Deviation from Ideal (See Tables)	$I_{FS}(D)$	V_{REF}10.000V $T_A = 25°C$	—	—	±1/2	—	—	±1	Step
	$I_{FS}(E)$	RII = 18.94kΩ, R12 = 20kΩ	—	—	±1/2	—	—	±1	Step
Full Scale Symmetry Error	$I_O(+)$-$I_O(-)$	Decode or Encode pair	—	±1/40	±1/8	—	±1/20	±1/4	Step
Zero Scale Current	I_{ZS}	Measured at selected output with 000 0000 input	1/4	1/2	3/4	1/4	1/2	3/4	Step
Disable Current	I_{DIS}	Leakage of output disabled by E/D and SB	—	5.0	75	—	5.0	75	nA
Output Current Range	I_{FSR}		0	2.0	4.2	0	2.0	4.2	mA
Logic Input Levels, Logic "0"	V_{IL}	$V_{LC} = 0V$	—	—	0.8	—	—	0.8	Volts
Logic Input Levels, Logic "1"	V_{IH}	$V_{LC} = 0V$	2.0	—	—	2.0	—	—	Volts
Logic Input Current	I_{IN}	$V_{IN} = -5V$ to +18V	—	—	120	—	—	120	μA
Logic Input Swing	V_{IS}	V− = −15V	−5	—	+18	−5	—	+18	Volts
Reference Bias Current	I_{12}		—	−3.0	−12.0	—	−3.0	−12.0	μA
Reference Input Slew Rate	dI/dt		—	0.25	—	—	0.25	—	mA/μs
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	$PSSI_{FS+}$	V+ = 4.5 to 18V, V− = −15V	—	±1/20	±1/2	—	±1/20	±1/2	Step
	$PSSI_{FS-}$	V− = −10.8V to −18V, V+ = 15V	—	±1/10	±1/2	—	±1/10	±1/2	Step
Power Supply Current	I+	$V_S = +5V$, −15V, $I_{FS} = 2.0mA$	—	2.7	4.5	—	2.7	4.5	mA
	I−	$V_S = +5V$, −15V, $I_{FS} = 2.0mA$	—	−6.7	−9.3	—	−6.7	−9.3	mA
	I+	$V_S = \pm 15V$, $I_{FS} = 2.0mA$	—	2.7	4.5	—	2.7	4.5	mA
	I−	$V_S = \pm 15V$, $I_{FS} = 2.0mA$	—	−6.7	−9.3	—	−6.7	−9.3	mA
Power Dissipation	P_D	$V_S = +5V$, −15V, $I_{FS} = 2.0mA$	—	114	167	—	114	167	mW
	P_D	$V_S = \pm 15V$, $I_{FS} = 2.0mA$	—	141	207	—	141	207	mW

NOTE: Settling time varies for each of the chord bits and step bits and a maximum specification may be misleading. In decode operation, the DAC-87 and OP-16 combination will decode 8 channels. In the encode mode, the DAC-87 and CMP-01 combination will encode 8 channels. Both encode and decode statements assume a 3.9μs channel time.

OUTPUT CURRENT DC TEST CIRCUIT



*V_{REF} IS ADJUSTED BEFORE TESTING EACH DEVICE TO PROVIDE IDEAL FULL SCALE OUTPUT CURRENT.

LINE SELECTION TABLE

TEST GROUP	ENCODE/ DECODE	SIGN BIT	OUTPUT MEASUREMENT	
1	1	1	$I_{OE}(+)$	(E_{01}/R1)
2	1	0	$I_{OE}(-)$	(E_{01}/R2)
3	0	1	$I_{OD}(+)$	(E_{02}/R3)
4	0	0	$I_{OD}(-)$	(E_{02}/R4)

NOTE: — Accuracy is specified in the test circuit using the tables below to be within the specified proportion of a step at the maximum value in each chord. Monotonic operation is guaranteed for all input codes.

CONDENSED CURRENT OUTPUT TABLES

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0.5	16.5	33	66	132	264	528	1056
15	1111	15.5	31.5	63	126	252	504	1008	2016
STEP SIZE		1	1	2	4	8	16	32	64

IDEAL ENCODE OUTPUT CURRRENT IN MICROAMPS AT CHORD ENPOINTS

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	1	17	34	68	136	272	544	1088
15	1111	16	32	64	128	256	512	1024	2048
STEP SIZE		1	1	2	4	8	16	32	64

These tables may be extended to include all of the encode/decode currents (ideal with $I_{REF} = 528\mu A$) by multiplying any of the numbers in the normalized tables by 0.5μA.

SPECIFICATION PARAMETER DEFINITIONS

STEP NONLINEARITY
Step size deviation from ideal within a chord.

ENCODE CURRENT
The difference between $I_{OE}(+)$ and $I_{OD}(+)$ or the difference between $I_{OE}(-)$ and $I_{OD}(-)$ at any code.

FULL SCALE DRIFT
The change in output current over the full operating temperature with $V_{REF} = 10.000V$, R11 = 18.94kΩ, and R12 = 20kΩ.

FULL SCALE SYMMETRY ERROR
The difference between $I_{OD}(-)$ and $I_{OD}(+)$ or the difference between $I_{OE}(-)$ and $I_{OE}(+)$ at full scale output.

OUTPUT VOLTAGE COMPLIANCE
The maximum output voltage swing at any current level which causes <½ step change in output current.

CHORDS
Groups of linearly-related steps in the transfer function. Also known as segments.

CHORD ENDPOINTS
The maximum code in each chord. Used to specify accuracy.

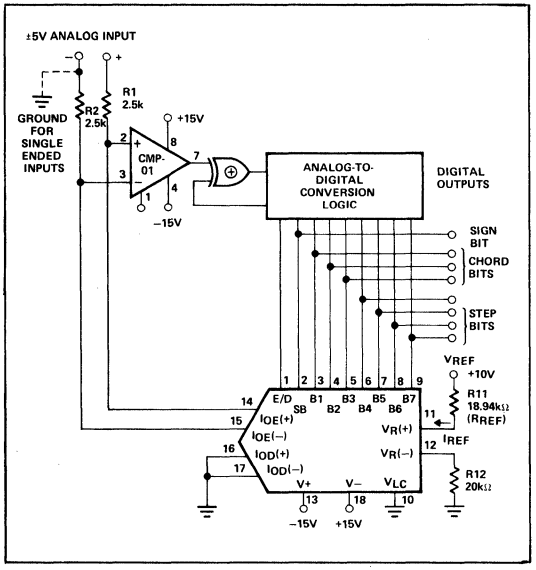
STEPS
Increments in each chord which divide it into 16 equal levels.

OUTPUT LEVEL NOTATION
Each output current level may be designated by the code $I_{C,S}$ where C = chord number and S = step number. For example, $I_{0,0}$ = zero scale current; $I_{0,1}$ = first step from zero; $I_{0,15}$ = endpoint of first chord (C_0); $I_{7,15}$ = full scale current.

DYNAMIC RANGE
Ratio of full scale current to step size in chord zero expressed in dB.

BASIC ENCODE OPERATION (COMPRESSING A/D CONVERSION)

BASIC ENCODE CONNECTIONS



ENCODE DECISION LEVELS

Compressing A/D conversion with the DAC-87 requires a comparator, an exclusive-OR gate, and a successive approximation register — the usual elements in any sign-plus-magnitude A/D converter. However, a compressing ADC has one significant difference from regular A/D converters.

In a conventional (linear) converter, the step size is a constant percentage of full scale, but in a compressing A/D converter, the step size increases as the output changes from zero scale to full scale.

When the DAC is used in the feedback loop of a successive approximation ADC the DAC outputs are used as decision levels to determine the edges of the quantizing bands. When the DAC is used in the decode mode it follows that the outputs must correspond to the center of the quantizing bands. Thus the encode mode output must exceed the decode mode output by one-half step. See AN 39 for further explanation.

ENCODING SEQUENCE

An encoding sequence begins with the Sign Bit comparison and decision. During this time the comparator is a polarity detector only. The Encode/Decode (E/D) input is held at a logic "0" so that no current flows into the encode outputs, and the comparator is effectively disconnected from the DAC. Once the input polarity has been determined, the E/D input is changed to a logic "1" allowing current to flow into $I_{OE}(+)$ or $I_{OE}(-)$ depending upon the Sign Bit Answer.

For positive inputs, current flows into $I_{OE}(+)$ through R1, and the comparator's output will be entered as the answer for each successive decision. For negative inputs, current flows into $I_{OE}(-)$ through R2 developing a negative voltage which is compared with the analog input. An exclusive-OR gate inverts the comparator's output during negative trials to maintain the proper logic coding, all ones for full scale and all zeros for zero scale. (A more complete schematic is shown in the applications section.)

NORMALIZED ENCODE DECISION LEVELS (SIGN BIT EXCLUDED)

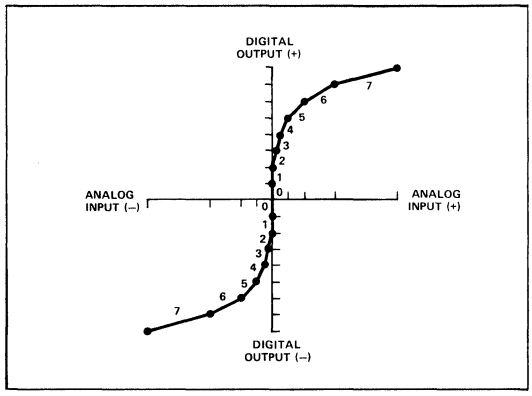
NORMALIZED ENCODE DECISION

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	2	34	68	136	272	544	1088	2176
1	0001	4	36	72	144	288	576	1152	2304
2	0010	6	38	76	152	304	608	1216	2432
3	0011	8	40	80	160	320	640	1280	2560
4	0100	10	42	84	168	336	672	1344	2688
5	0101	12	44	88	176	352	704	1408	2816
6	0110	14	46	92	184	368	736	1472	2944
7	0111	16	48	96	192	384	768	1536	3072
8	1000	18	50	100	200	400	800	1600	3200
9	1001	20	52	104	208	416	832	1664	3328
10	1010	22	54	108	216	432	864	1728	3456
11	1011	24	56	112	224	448	896	1792	3584
12	1100	26	58	116	232	464	928	1856	3712
13	1101	28	60	120	240	480	960	1920	3840
14	1110	30	62	124	248	496	992	1984	3968
15	1111	32	64	128	256	512	1024	2048	*4096
STEP SIZE		2	2	4	8	16	32	64	128

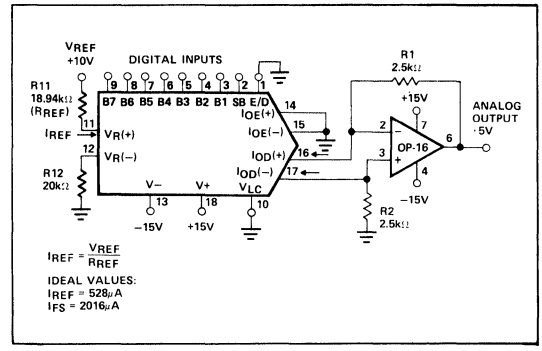
*Virtual Decision Level

The successive removal technique requires the first magnitude decision to be made at the code 011 1111 and sequentially turning off bits until all decisions have been made.

ENCODE TRANSFER CHARACTERISTIC (A/D CONVERSION)



BASIC DECODE CONNECTIONS



BASIC DECODE OPERATION (EXPANDING D/A CONVERSION)

DECODE OPERATION

D/A conversion with the DAC-87 may be illustrated by using an operational amplifier connected to the decode outputs as a balanced load. The decode mode of operation is selected by applying a logic "0" to the Encode/Decode input. This enables the I_{OD} outputs, disables the I_{OE} outputs, and allows $I_{OD}(+)$ or $I_{OD}(-)$ to be selected by the Sign Bit input. When the Sign Bit input is high, a logic "1", all of the output current flows into $I_{OD}(+)$ forcing a positive voltage at the operational amplifier's output. When the Sign Bit input is low, a logic "0", all of the output current flows into $I_{OD}(-)$ through R2 forcing a negative voltage output. Since the Sign

	E/D	SB	B1	B2	B3	B4	B5	B6	B7	E_0
POS FULL SCALE	0	1	1	1	1	1	1	1	1	5.040V
(+) ZERO SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.0012V
(+) ZERO SCALE	0	1	0	0	0	0	0	0	0	0.004V
(–) ZERO SCALE	0	0	0	0	0	0	0	0	0	0.004V
(–) ZERO SCALE +1 STEP	0	0	0	0	0	0	0	0	1	–0.0012V
NEG FULL SCALE	0	0	1	1	1	1	1	1	1	–5.040V

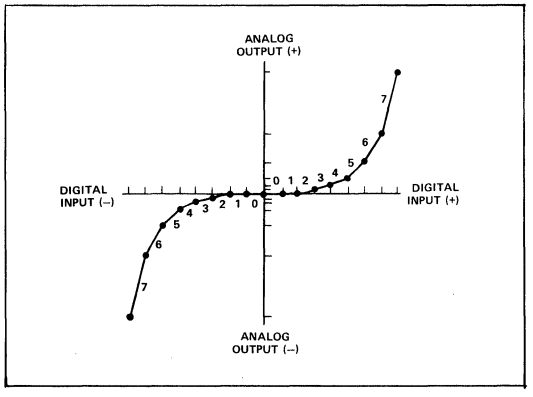
NORMALIZED DECODE OUTPUT (SIGN BIT EXCLUDED)

NORMALIZED DECODE OUTPUT

STEP \ CHORD	0	1	2	3	4	5	6	7
	000	001	010	011	100	101	110	111
0	0000	1	33	66	132	264	528	1056	2112
1	0001	3	35	70	140	280	560	1120	2240
2	0010	5	37	74	148	296	592	1184	2368
3	0011	7	39	78	156	312	624	1248	2496
4	0100	9	41	82	164	328	656	1312	2624
5	0101	11	43	86	172	344	688	1376	2752
6	0110	13	45	90	180	360	720	1440	2880
7	0111	15	47	94	188	376	752	1504	3008
8	1000	17	49	98	196	392	784	1568	3136
9	1001	19	51	102	204	408	816	1632	3264
10	1010	21	53	106	212	424	848	1696	3392
11	1011	23	55	110	220	440	880	1760	3520
12	1100	25	57	114	228	456	912	1824	3648
13	1101	27	59	118	236	472	944	1888	3776
14	1110	29	61	122	244	488	976	1952	3904
15	1111	31	63	126	252	504	1008	2016	4032
STEP SIZE		2	2	4	8	16	32	64	128

Bit only steers current into $I_{OD}(+)$ or $I_{OD}(-)$, the output will always be symmetrical, limited only by the matching of R1 and R2.

DECODE TRANSFER CHARACTERISTIC (D/A CONVERSION)



NORMALIZED TABLES

The encode and decode tables may be used to calculate ideal output current at any code point. For example, in decode mode at $I_{3,7}$ (011 0111) find 188. 188/4032 times I_{FS} of 2016μA equals 94μA.

BASIC REFERENCE CONSIDERATIONS

Full scale output current is ideally 2016μA when the reference current is 528μA in the decode mode. In the encode mode it is 2048μA because the additional one-half step adds 32μA to the output. A percentage change in I_{REF} caused by changes in V_{REF} or R_{REF} will produce the same percentage change in output current.

The large step size at full scale allows the use of inexpensive references in many applications. In some situations V_{REF} may even be the positive power supply. For example, with V+ = 15V, $R_{REF} = 15V/528\mu A$ or 28.4kΩ. When using a power supply as a reference, R11 should be two resistors, R11A and R11B, and the junction should be bypassed to ground to provide decoupling.

OUTPUT VOLTAGE COMPLIANCE

The DAC-87 has true current outputs with wide voltage compliance enabling fast drive of a variety of single ended and balanced loads. Positive voltage compliance is +18V and negative voltage compliance is −5.0V with $I_{REF} = 528\mu A$ and V = −15V. Negative voltage compliance $V_{OC}(-)$ for other values of I_{REF} and V− may be obtained from the table, or calculated as follows:

$$V_{OC}(-)\ \text{min} = (V-) + (2\ I_{REF} \times 1.6k\Omega) + 8.4V$$

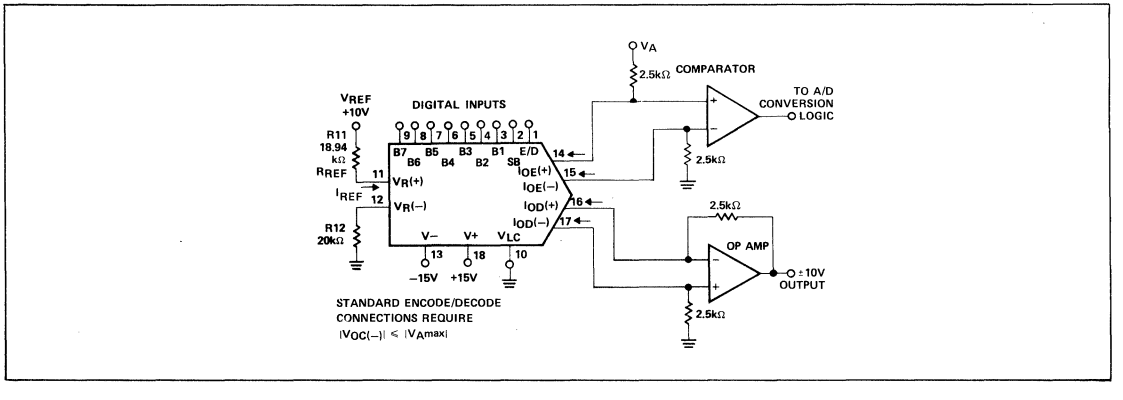
Output voltage compliance can be extended in both encode and decode modes using the connections shown below.

NEGATIVE OUTPUT VOLTAGE COMPLIANCE $V_{OC}(-)$

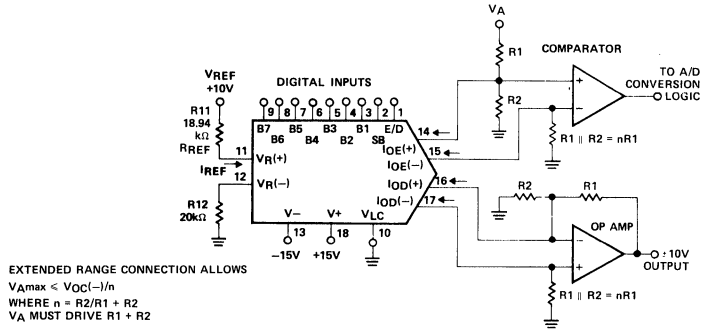
V−	I_{FS} 1.0mA	2.0mA	4.0mA
−12V	−2.8V	−2.0V	−0.4V
−15V	−5.8V	−5.0V	−3.4V
−18V	−8.8V	−8.0V	−6.4V

MINIMUM NEGATIVE COMPLIANCE
$V_{OC}(-)\ \text{MIN} = (V-) + (2I_{REF}\ 1.6k\Omega) + 8.4V$

STANDARD OUTPUT CONNECTIONS



OUTPUT COMPLIANCE EXTENSION CONNECTIONS



IDEAL DECODE OUTPUT CURRENT IN MICROAMPS (SIGN BIT EXCLUDED)

IDEAL DECODE OUTPUT

	CHORD	0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0.5	16.5	33	66	132	264	528	1056
1	0001	1.5	17.5	35	70	140	280	560	1120
2	0010	2.5	18.5	37	74	148	286	592	1184
3	0011	3.5	19.5	39	78	156	312	624	1248
4	0100	4.5	20.5	41	82	164	328	656	1312
5	0101	5.5	21.5	43	86	172	344	688	1376
6	0110	6.5	22.5	45	90	180	360	720	1440
7	0111	7.5	23.5	47	94	188	376	752	1504
8	1000	8.5	24.5	49	98	196	392	784	1568
9	1001	9.5	25.5	51	102	204	408	816	1632
10	1010	10.5	26.5	53	106	212	424	848	1696
11	1011	11.5	27.5	55	110	220	440	880	1760
12	1100	12.5	28.5	57	114	228	456	912	1824
13	1101	13.5	29.5	59	118	236	472	944	1888
14	1110	14.5	30.5	61	122	244	488	976	1952
15	1111	15.5	31.5	63	126	252	504	1008	2016
STEP SIZE		1	1	2	4	8	16	32	64

DAC-88

COMDAC® COMPANDING D/A CONVERTER

μ - 255 LAW DAC

FEATURES

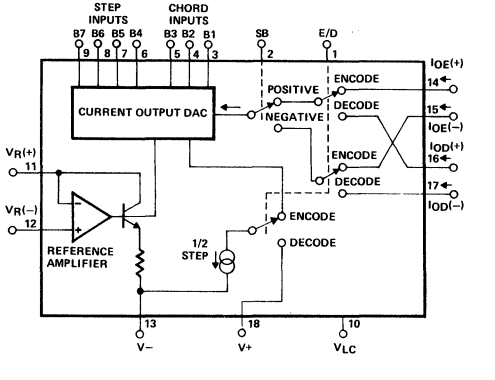
- **IMPROVED ACCURACY over DAC-86**
- **IMPROVED SPEED over DAC-86**
- **Conforms With Bell System μ-255 Companding Law**
- **Meets D3 Compandor Tracking Specifications**
- **Both Encode and Decode Capability**
- **Tight Full Scale Tolerance Eliminates Calibration**
- **Low Full Scale Drift Over Temperature**
- **Extremely Low Noise Contribution**
- **Multiplying Reference Inputs**
- **Simplifies PCM System Design**
- **High Reliability**
- **Low Power Consumption and Low Cost**

GENERAL DESCRIPTION

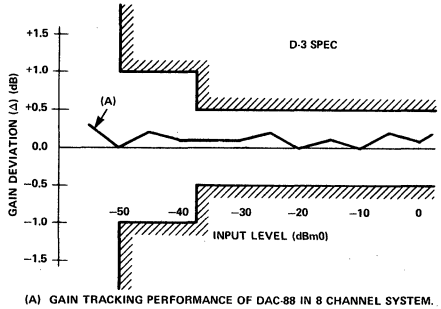
The DAC-88 monolithic COMDAC® D/A Converter provides a 15 segment linear approximation to the Bell System μ-255 companding law. The law is implemented by using three bits to select one of eight binarily-related chords (or segments) and four bits to select one of sixteen linearly-related steps within each chord. A sign bit determines signal polarity, and an encode/decode select bit determines encode or decode operation.

Accuracy is assured by specifying chord end point values, step nonlinearity, and monotonicity over the full operating temperature range. Typical applications include PCM carrier systems, digital PBX's, intercom systems, and PCM recording. For CCITT "A" Law models, refer to the DAC-89 data sheet.

EQUIVALENT CIRCUIT AND PIN CONNECTION DIAGRAM



GAIN TRACKING



(A) GAIN TRACKING PERFORMANCE OF DAC-88 IN 8 CHANNEL SYSTEM.

BELL μ-255 LAW TRANSFER CHARACTERISTIC

The transfer characteristic of the DAC-88 is a piecewise linear approximation to the Bell System μ255 law expressed by:

$$Y(\chi) = \mathrm{sgn}(\chi)\,\frac{\ln(1+\mu|\chi|)}{\ln(1+\mu)} \quad -1 \le \chi \le 1$$

for a normalized coding range of ±1

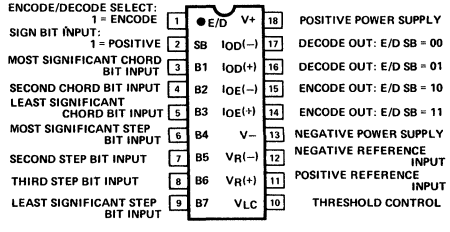
where: χ = input signal level

Y = output compressed signal level

$\mu = 255$

This law is implemented by the DAC-88 with an eight chord (or segment) piecewise linear approximation with 16 linear steps in each chord for both polarities. Dynamic range of 72dB in both polarities is achieved with eight-bit coding.

PIN CONNECTIONS & ORDERING INFORMATION



18-PIN HERMETIC DUAL-IN-LINE
(X-Suffix)

ACCURACY

±1/4 STEP	DAC-88EX
±1/2 STEP	DAC-88CX

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 528\mu A$, $-25°C \le T_A \le +85°C$, and for all 4 outputs, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-88-E MIN	DAC-88-E TYP	DAC-88-E MAX	DAC-88-C MIN	DAC-88-C TYP	DAC-88-C MAX	UNITS
Resolution		8 chords with 16 steps each	±128	±128	±128	±128	±128	±128	Steps
Dynamic Range		20 log ($I_{7,15}/I_{0,1}$)	72	72	72	72	72	72	dB
Monotonicity		Sign Bit + or −	128	—	—	128	—	—	Steps
Chord Endpoint Accuracy Chord Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	—	—	±1/4	—	—	±1/2	Step
Chord Endpoint Accuracy All Chords Other Than Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	—	—	±1/2	—	—	±1	Step
Encode Decision Level Current		Additional output encode/decode = 1	3/8	1/2	5/8	1/4	1/2	3/4	Step
Settling Time (Note 1)	t_s	To within ±1/2 step	—	500	see note	—	500	see note	ns
Settling Time in Chord Zero	T_{SCO}	To within ±1/2 step	—	500	—	—	500	—	ns
Full Scale Drift (C_7)	ΔI_{FS}	Full temperature range	—	±1/16	±1/10	—	±1/10	±1/4	Step
Output Voltage Compliance	V_{OC}	Full scale current change ≤1/2 step	−5	—	+18	−5	—	+18	Volts
Full Scale Symmetry Error (Note 2)	$I_O(+) - I_O(-)$	Decode or encode pair Input Code 111 1111	—	±1/40	±1/8	—	±1/40	±1/4	Step
Zero Scale Current (C_0) (Note 2)	I_{ZS}	Measured at selected output with 000 0000 input	—	1/40	1/8	—	1/40	1/4	Step
Disable Current (All bits high) (Note 2)	I_{DIS}	Leakage of output disabled by E/D and SB	—	5.0	100	—	5.0	100	nA
Step Accuracy Chord Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	—	—	±1/4	—	—	±1/2	Step
Step Accuracy All Chords Other Than Zero		Error relative to ideal values at $I_{FS} = 2016\mu A$	—	—	±1/2	—	—	±1	Step
Output Current Range	I_{FSR}		0	2.0	4.2	0	2.0	4.2	mA
Logic Input Levels, Logic "0"	V_{IL}	$V_{LC} = 0V$	—	—	0.8	—	—	0.8	Volts
Logic Input Levels, Logic "1"	V_{IH}	$V_{LC} = 0V$	2.0	—	—	2.0	—	—	Volts
Logic Input Current	I_{IN}	$V_{IN} = -5V$ to +18V	—	—	120	—	—	120	μA
Logic Input Swing	V_{IS}	V− = −15V	−5	—	+18	−5	—	+18	Volts
Reference Bias Current	I_{12}		—	−3.0	−12.0	—	−3.0	−12.0	μA
Reference Input Slew Rate	dI/dt		—	0.25	—	—	0.25	—	mA/μs
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	$PSSI_{FS+}$	V+ = 4.5 to 18V, V− = −15V	—	±1/20	±1/2	—	±1/20	±1/2	Step
	$PSSI_{FS-}$	V− = −10.8V to −18V, V+ = 15V	—	±1/10	±1/2	—	±1/10	±1/2	Step
Power Supply Current	I+	$V_S = +5V, -15V$, $I_{FS} = 2.0mA$	—	2.7	5.5	—	2.7	5.5	mA
	I−	$V_S = +5V, -15V$, $I_{FS} = 2.0mA$	—	−6.7	−12	—	−6.7	−12	mA
	I+	$V_S = \pm 15V$, $I_{FS} = 2.0mA$	—	2.7	5.5	—	2.7	5.5	mA
	I−	$V_S = \pm 15V$, $I_{FS} = 2.0mA$	—	−6.7	−12	—	−6.7	−12	mA
Power Dissipation	P_D	$V_S = +5V, -15V$, $I_{FS} = 2.0mA$	—	114	207	—	114	207	mW
	P_D	$V_S = \pm 15V$, $I_{FS} = 2.0mA$	—	141	262	—	141	262	mW
Full Scale Current Deviation From Ideal Deviation (See Tables) (Note 2)	$I_{FS}(D)$	V_{REF} 10.000V, $T_A = 25°C$	—	—	±1/2	—	—	±1	Step
	$I_{FS}(E)$	R11 = 19.53kΩ, R12 = 20kΩ	—	—	±1/2	—	—	±1	Step
Idle Current (Note 2)	I_I		—	10	—	—	10	—	μA

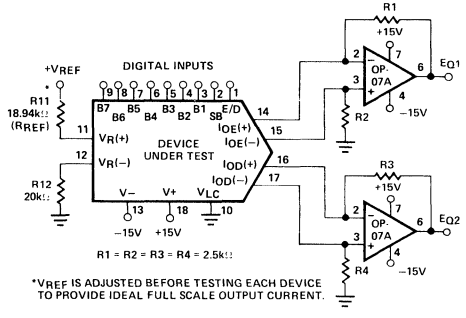
NOTES:

1. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) step size is 0.5μA, while in the last chord near full scale (C_7) step size is 64μA. Settling time varies for each of the chord bits and step bits and a maximum specification is misleading. In decode operation, the DAC-88 and OP-16 combination will decode 24 channels. In the encode mode, the DAC-88 and CMP-01 combination will encode 8 channels. Both encode and decode statements assume a 5.2μs channel time.
2. Current specifications relate to differential currents between (+) and (−) output leads. At the selected outputs, equal idle currents are present simultaneously on both current output leads.

ABSOLUTE MAXIMUM RATINGS

V+ Supply to V− Supply 36V
V_{LC} Swing ..... V− plus 8V to V+
Analog Current Outputs ..... V− plus 8V to V− plus 36V
Reference Inputs ..... V− to V+
Reference Input Differential Voltage ..... ± 18V
Reference Input Current 1.25mA
Logic Inputs ..... V− plus 8V to V− plus 36V
Operating Temperature ..... −25°C to +85°C
Storage Temperature ..... −65°C to +150°C
Power Dissipation 500mW
Derate above 100°C ..... 10mW/°C
Lead Soldering Temperature ..... 300°C (60 sec)

OUTPUT CURRENT DC TEST CIRCUIT



LINE SELECTION TABLE

TEST GROUP	ENCODE/ DECODE	SIGN BIT	OUTPUT MEASUREMENT	
1	1	1	$I_{OE}(+)$	(E_{01}/R1)
2	1	0	($I_{OE}(-)$	(E_{01}/R2)
3	0	0	($I_{OD}(+)$	(E_{02}/R3)
4	0	0	($I_{OD}(-)$	(E_{02}/R4)

NOTE: Accuracy is specified in the test circuit using the tables below to be within the specified proportion of a step at the maximum value in each chord. Monotonic operation is guaranteed for all input codes.

CONDENSED CURRENT OUTPUT TABLES ($I_{REF} = 528\mu A$)

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

	CHORD	0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0	8.25	24.75	57.75	123.75	255.75	519.75	1047.75
15	1111	7.5	23.25	54.75	117.75	243.75	495.75	999.75	2007.75
STEP SIZE		0.50	1	2	4	8	16	32	64

IDEAL ENCODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

	CHORD	0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0.25	8.75	25.75	59.75	127.75	263.75	535.75	1079.75
15	1111	7.75	23.75	55.75	119.75	247.75	503.75	1015.75	2039.75
STEP SIZE		0.50	1	2	4	8	16	32	64

These tables may be extended to include all of the encode/decode currents (ideal with $I_{REF} = 528\mu A$) by multiplying any of the numbers in the normalized tables by 0.25μA.

SPECIFICATION PARAMETER DEFINITIONS

FULL SCALE DRIFT

The change in output current over the full operating temperature with $V_{REF} = 10.000V$, R11 = 18.94kΩ, and R12 = 20kΩ.

ENCODE CURRENT

The difference between $I_{OE}(+)$ and $I_{OD}(+)$ or the difference between $I_{OE}(-)$ and $I_{OD}(-)$ at any code.

FULL SCALE SYMMETRY ERROR

The difference between $I_{OD}(-)$ and $I_{OD}(+)$ or the difference between $I_{OE}(-)$ and $I_{OE}(+)$ at full scale output.

OUTPUT VOLTAGE COMPLIANCE

The maximum output voltage swing at any current level which causes < ½ step change in output current.

IDEAL OUTPUT CURRENT

The difference between the (+) and (−) currents (encode or decode) at any code.

CHORDS

Groups of linearly-related steps in the transfer function. Also known as segments.

CHORD ENDPOINTS

The maximum code in each chord. Used to specify accuracy.

STEPS

Increments in each chord which divides it into 16 equal levels.

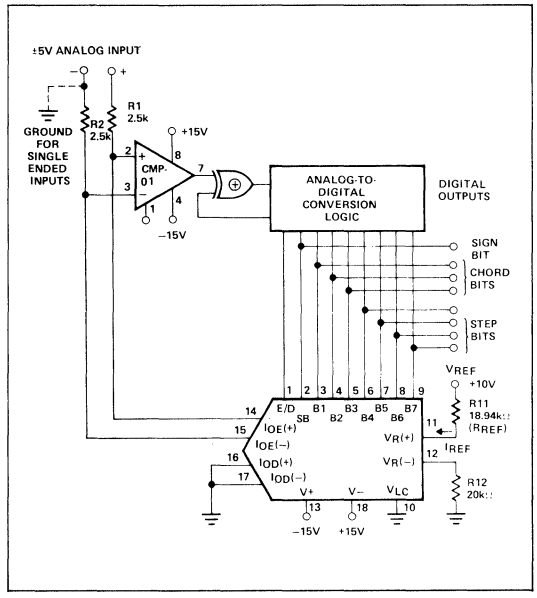
OUTPUT LEVEL NOTATION

Each output current level may be designated by the code $I_{C,S}$ where C = chord number and S = step number. For example, $I_{0,0}$ = zero scale current; $I_{0,1}$ = first step from zero; $I_{0,15}$ = endpoint of first chord (C_0); $I_{7,15}$ = full scale current.

DYNAMIC RANGE

Ratio of full scale current to step size in chord zero expressed in dB.

BASIC ENCODE CONNECTIONS



BASIC ENCODE OPERATION (COMPRESSING A/D CONVERSION)

ENCODE DECISION LEVELS

Compressing A/D conversion with the DAC-88 requires a comparator, an exclusive-or gate, and a successive approximation register — the usual elements in any sign-plus-magnitude A/D converter. However, a compressing ADC has one signficant difference from regular A/D converters.

In a conventional (linear converter), the step size is a constant percentage of full scale, but in a compressing A/D converter, the step size increases as the output changes from zero scale to full scale.

When the DAC is used in the feedback loop of a successive approximation ADC the DAC outputs are used as decision levels to determine the edges of the quantizing bands. When the DAC is used in the decode mode it follows that the outputs must correspond to the center of

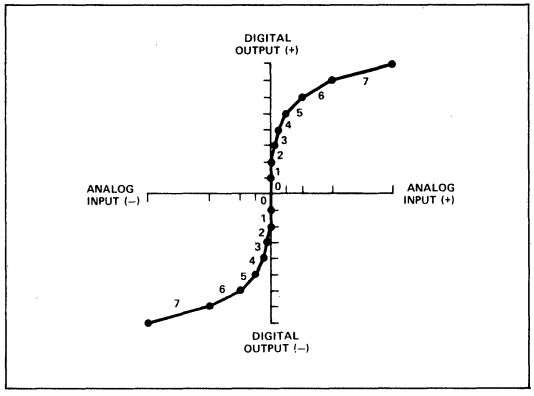
NORMALIZED ENCODE LEVEL (SIGN BIT EXCLUDED) $I_{C,S} = 2[2^C (S + 17) - 16.5]$

C = chord no. (0 through 7)
S = step no. (0 through 15)

	CHORD	0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	1	35	103	239	511	1055	2143	4319
1	0001	3	39	111	255	543	1119	2271	4575
2	0010	5	43	119	271	575	1183	2399	4831
3	0011	7	47	127	287	607	1247	2527	5087
4	0100	9	51	135	303	639	1311	2655	5343
5	0101	11	55	143	319	671	1375	2783	5599
6	0110	13	59	151	335	703	1439	2911	5855
7	0111	15	63	159	351	735	1503	3039	6111
8	1000	17	67	167	367	767	1567	3167	6367
9	1001	19	71	175	383	799	1631	3295	6623
10	1010	21	75	183	399	831	1695	3423	6879
11	1011	23	79	191	415	863	1759	3551	7135
12	1100	25	83	199	431	895	1823	3679	7391
13	1101	27	87	207	447	927	1887	3807	7647
14	1110	29	91	215	463	959	1951	3935	7903
15	1111	31	95	223	479	991	2015	4063	8159
STEP SIZE		2	4	8	16	32	64	128	256

the quantizing bands. Thus the encode mode output must exceed the decode mode output by one-half step. See AN 39 for further explanation.

ENCODE TRANSFER CHARACTERISTICS (A/D CONVERSION)



ENCODING SEQUENCE

An encoding sequence begins with the sign bit decision. During this time the comparator is a polarity detector only. The Encode/Decode (E/D) input is held at a logic "0", so that no current flows into the encode outputs, and the comparator is effectively disconnected from the DAC. Once the input polarity has been determined, the E/D input is changed to a logic "1" allowing current to flow into $I_{OE}(+)$ or $I_{OE}(-)$ depending upon the Sign Bit Answer.

For positive inputs, current flows into $I_{OE}(+)$ through R1, and the comparator's output will be entered as the answer for each successive decision. For negative inputs, current flows into $I_{OE}(-)$ through R2 developing a negative voltage which is compared with the analog input. An exclusive-OR gate inverts the comparator's output during negative trials to maintain the proper logic coding, all ones for full scale and all zeros for zero scale.

The bits are converted with a successive removal technique, starting with a decision at the code 011 1111 and turning off bits sequentially until all decisions have been made.

BASIC DECODE OPERATION (EXPANDING D/A CONVERSION)

DECODE OPERATION

D/A conversion with the DAC-88 may be illustrated by using an operational amplifier connected to the decode outputs. The decode mode of operation is selected by applying a logic "0" to the Encode/Decode input. This enables the I_{OD} outputs, disables the I_{OE} outputs and, allows $I_{OD}(+)$ or $I_{OD}(-)$ to be selected by the Sign Bit input. When the Sign Bit input is high, a logic "1", all of the output current flows into $I_{OD}(+)$ forcing a positive voltage at the operational amplifier's output. When the Sign Bit input is low, a logic "0", all of the output current flows into $I_{OD}(-)$ through R2 forcing a negative voltage output. Since the Sign Bit only steers current into $I_{OD}(+)$ or $I_{OD}(-)$, the output will always be symmetrical, limited only by the matching of R1 and R2.

NORMALIZED TABLES

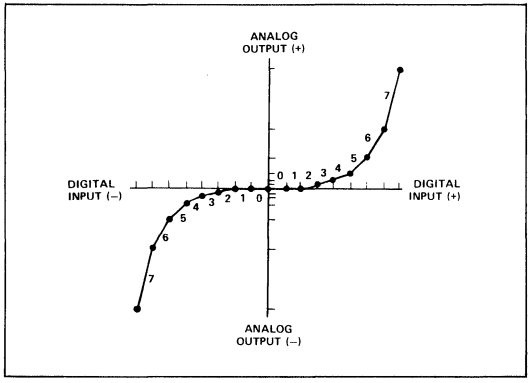
The encode and decode tables may be used to calculate ideal output current at any point. For example, in decode mode at $I_{3,7}$ (011 0111) find 343. 343/8031 times I_{FS} of

NORMALIZED DECODE OUTPUT (SIGN BIT EXCLUDED) $I_{C,S} = 2[2^C (S + 16.5) - 16.5]$

C = chord no. (0 through 7)
S = step no. (0 through 15)

STEP	CHORD	0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	33	99	231	495	1023	2079	4191
1	0001	2	37	107	247	527	1087	2207	4447
2	0010	4	41	115	263	559	1151	2335	4703
3	0011	6	45	123	279	591	1215	2463	4959
4	0100	8	49	131	295	623	1279	2591	5215
5	0101	10	53	139	311	655	1343	2719	5471
6	0110	12	57	147	327	687	1407	2847	5727
7	0111	14	61	155	343	719	1471	2975	5983
8	1000	16	65	163	359	751	1535	3103	6239
9	1001	18	69	171	375	783	1599	3231	6495
10	1010	20	73	179	391	815	1663	3359	6751
11	1011	22	77	187	407	847	1727	3487	7007
12	1100	24	81	195	423	879	1791	3615	7263
13	1101	26	85	203	439	911	1855	3743	7519
14	1110	28	89	211	455	943	1919	3871	7775
15	1111	30	93	219	471	975	1983	3999	8031
STEP SIZE		2	4	8	16	32	64	128	256

DECODE TRANSFER CHARACTERISTIC (D/A CONVERSION)



2007.75μA equals 85.75μA. Alternatively, use the condensed current tables and add up the number of steps.

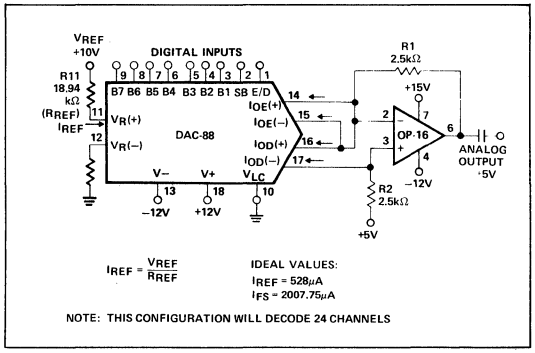
BASIC REFERENCE CONSIDERATIONS

Full scale output current is ideally 2007.75μA when the reference current is 528μA in the decode mode. In the encode mode it is 2039.75μA because the additional 1/2 step adds 32μA to the output. A percentage change in I_{REF} caused by changes in V_{REF} or R_{REF} will produce the same percentage change in output current.

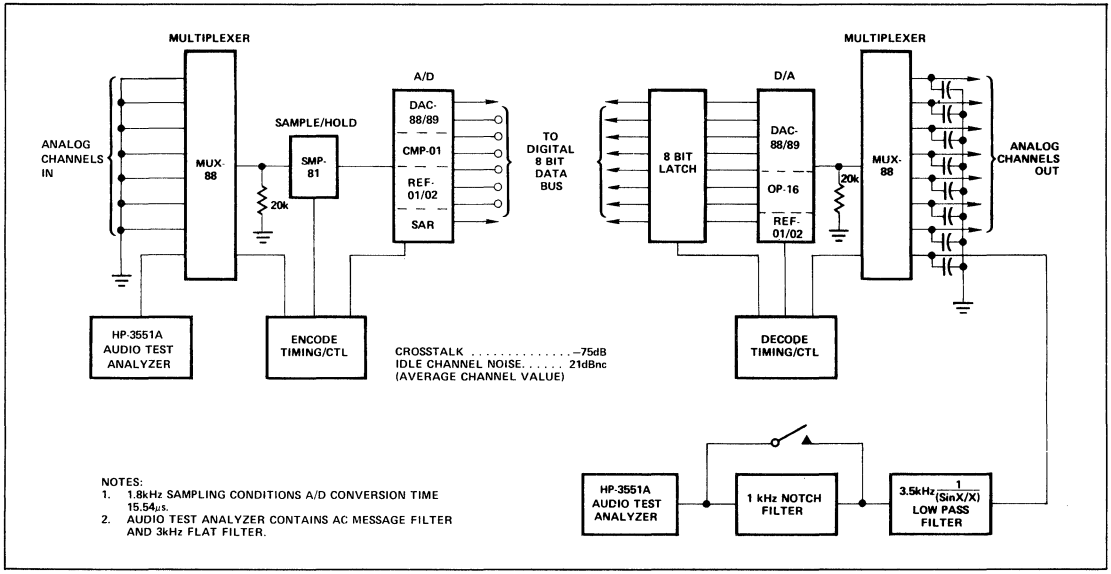
The large step size at full scale allows the use of inexpensive references in many applications. In some situations V_{REF} may even be the positive power supply. For example, with V+ = 15V, R_{REF} = 15V/528μA or 28.4kΩ. When using a power supply as a reference, R11 should be two resistors, R11A and R11B, and the junction should be bypassed to ground to provide decoupling.

	E/D	SB	B1	B2	B3	B4	B5	B6	B7	E_0
POS FULL SCALE	0	1	1	1	1	1	1	1	1	5.019V
(+) ZERO SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.0012
(+) ZERO SCALE	0	1	0	0	0	0	0	0	0	0V
(–) ZERO SCALE	0	0	0	0	0	0	0	0	0	0V
(–) ZERO SCALE +1 STEP	0	0	0	0	0	0	0	0	1	–0.0012
NEG FULL SCALE	0	0	1	1	1	1	1	1	1	–5.019V

BASIC DECODE CONNECTIONS



SYSTEM TEST CIRCUIT



REFERENCE AMPLIFIER OPERATION

REFERENCE AMPLIFIER SETUP

The DAC-88 is a multiplying D/A converter in which the output current is the product of the normalized digital input and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full scale output current is a linear function of the reference current and is given for all four outputs in the figures above.

REFERENCE RECOMMENDATIONS

For most applications a +10.0V reference, such as the PMI REF-01, is recommended for optimum full scale temperature coefficient performance.

POWER SUPPLY CONSIDERATIONS

POWER SUPPLIES

Power supply current drain is relatively independent of voltage and temperature and completely independent of the logic input states.

When operating with V− between −15V and −11V, output negative voltage compliance, $V_{OC}(-)$, reference input amplifier common mode voltage range, and logic input negative voltage range are reduced by an amount equivalent to the difference between −15V and the V− supply in use. Operation with V+ between +5V and +15V affects V_{LC} and the reference amplifier common mode positive voltage range in the same manner.

OUTPUT VOLTAGE COMPLIANCE

The DAC-88 has true current outputs with wide voltage compliance enabling fast drive of a variety of single ended and balanced loads. Positive voltage compliance is +18V and negative voltage compliance is −5.0V with $I_{REF} = 528\mu A$ and V = −15V. Negative voltage compliance $V_{OC}(-)$ for other values of I_{REF} and V− may be obtained from the table, or calculated as follows:

$$V_{OC}(-)\ \text{min} = (V-) + (2\ I_{REF} \times 1.6k\Omega) + 8.4V$$

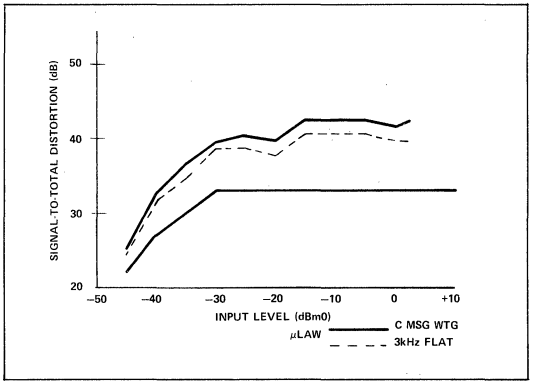
Output voltage compliance can be extended in both encode and decode modes using the connections shown below.

NEGATIVE OUTPUT VOLTAGE COMPLIANCE $V_{OC}(-)$

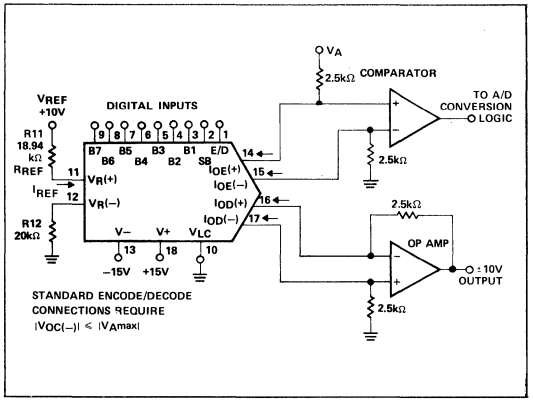
V−	I_{FS} 1.0mA	2.0mA	4.0mA
−12V	−2.8V	−2.0V	−0.4V
−15V	−5.8V	−5.0V	−3.4V
−18V	−8.8V	−8.0V	−6.4V

MINIMUM NEGATIVE COMPLIANCE
$V_{OC}(-)\ \text{MIN} = (V-) + (2\ I_{REF}\ 1.6k\Omega) + 8.4V$

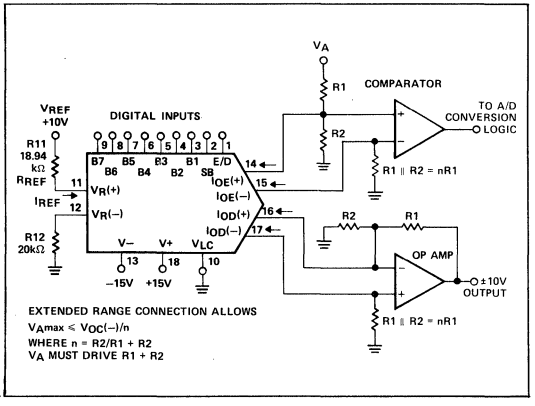
SIGNAL TO QUANTIZING DISTORTION vs INPUT LEVEL



STANDARD OUTPUT CONNECTIONS



COMPLIANCE EXTENSION CONNECTIONS



DICE

For applicable DICE information see DAC-78 Data Sheet.

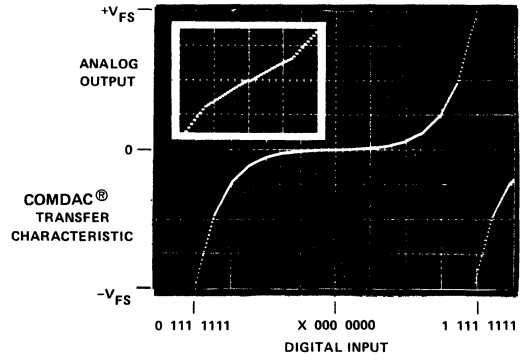
DAC-89

COMDAC® COMPANDING D/A CONVERTER

'A'- LAW DAC

FEATURES

- **Improved Accuracy Over DAC-87**
- **Improved Speed Over DAC-87**
- **11-Bit Accuracy and Resolution Around Zero**
- **Sign Plus 66dB Dynamic Range**
- **True Current Outputs: −5V to +18V Compliance**
- **Tight Full Scale Tolerance Eliminates Calibration**
- **Low Full Scale Drift Over Temperature**
- **Low Power Consumption and Low Cost**
- **Ideal for PCM and 8-Bit μP Applications**
- **Outputs Multiplexed for Time Shared Applications**



GENERAL DESCRIPTION

The DAC-89 monolithic COMDAC® D/A Converter provides the complete decode function for "A" Law PCM CODECs. The DAC-89 may be configured in an encoder, as a decoder, or may be timeshared between encoding and decoding.

Accuracy is assured by specifying chord end point values, chord nonlinearity, and monotonicity over the full operating temperature range. For companding D/A converters with Bell μ-255 law conformance refer to the DAC-88 data sheet. For non-telecommunications applications, see the DAC-78 data sheet.

CCITT "A" LAW CHARACTERISTIC

The output of the DAC-89 is an approximation to the CCITT "A" law which can be expresed as:

$$Y = \frac{1 + \ln AX}{1 + \ln A} \quad 1/A \leq X \leq 1$$

$$Y = \frac{AX}{1 + \ln A} \quad 0 \leq X \leq 1/A \text{ where:}$$

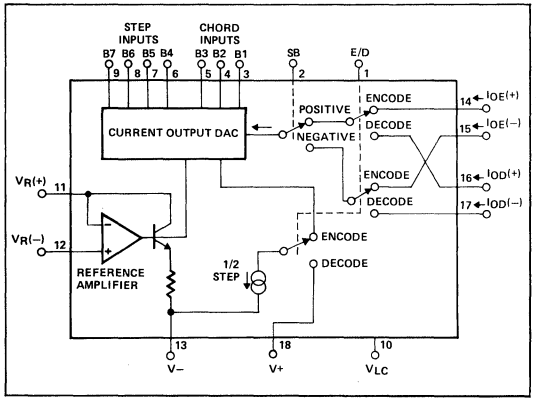
X = Normalized input signal level of the compressor (encoder), V_{IN}/V_{FS}.

Y = Output signal level of the compressor (encoder).

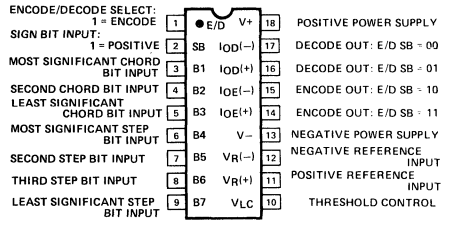
A = 87.6

This law is implemented by the DAC-89 with an eight chord (or segment) piecewise linear approximation for each polarity with sixteen linear steps in each chord. The first two chords are co-linear and of equal step size, and may be considered as one chord of 32 steps. Step sizes of the remaining six chords are binarily related to the first chord.

EQUIVALENT CIRCUIT



PIN CONNECTIONS & ORDERING INFORMATION



TOP VIEW

18-PIN HERMETIC DUAL-IN-LINE (X-Suffix)

ACCURACY	
±1/4 STEP	DAC-89EX
±1/2 STEP	DAC-89CX

ABSOLUTE MAXIMUM RATINGS

V+ Supply to V− Supply 36V
V_{CL} Swing ..... V− plus 8V to V+
Analog Current Outputs ..... V− plus 8V to V− plus 36V
Reference Inputs ..... V− to V+
Reference Input Differential Voltage ..... ±18V
Reference Input Current 1.25mA

Logic Inputs ..... V− plus 8V to V− plus 36V
Operating Temperature Range ..... −25°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Power Dissipation 500mW
Derate above 100° C ..... 10mW/° C
Lead Soldering Temperature (60 sec.) ..... 300°C

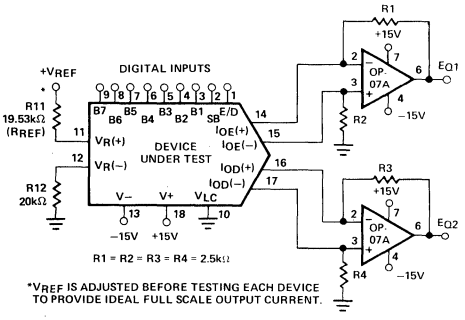
ELECTRICAL CHARACTERISTICS at $V_s = \pm 15V$, $I_{REF} = 512\mu A$, $-25°C \leq T_A \leq +85°C$, and for all 4 outputs unless otherwise specified. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) step size is 1.0μA, while in the last chord near full scale (C_7) step size is 64μA.

			DAC-89-E			DAC-89-C			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Resolution		8 chords with 16 steps each	±128	—	±128	±128	—	±128	Steps
Dynamic Range		20 log ($I_{7,15}/I_{0,0}$)	66	—	66	66	66	66	dB
Monotonicity		Sign Bit + or −	128	—	—	128	—	—	Steps
Chord Endpoint Accuracy Chord Zero		Error relative to ideal values at $I_{FS} = 2016\mu A$	—	—	±1/4	—	—	±1/2	Step
Chord Endpoint Accuracy All Chords Other Than Zero		Error relative to ideal values at $I_{FS} = 2016\mu A$	—	—	±1/2	—	—	±1	Step
Step Accuracy Chord Zero		Error relative to ideal values at $I_{FS} = 2016\mu A$	—	—	±1/4	—	—	±1/2	Step
Step Accuracy All Chords Other Than Zero		Error relative to ideal values at $I_{FS} = 2016\mu A$	—	—	±1/2	—	—	±1	Step
Encode Current		Additional output Encode/Decode = 1	1/4	1/2	3/4	1/4	1/2	3/4	Step
Settling Time (Note 1)	t_s	To within ±1/2 step	—	500	—	—	—	—	ns
Full Scale Drift	ΔI_{FS}	Full temperature range	—	±1/20	±1/4	—	±1/10	±1/2	Step
Output Voltage Compliance	V_{OS}	Full scale current change ≤1/2 step	−5	—	+18	−5	—	+18	Volts
Full Scale Current Deviation from Ideal (See Tables) (Note 2)	$I_{FS}(D)$	V_{REF}10.000V $T_A = 25°C$	—	—	±1/2	—	—	±1	Step
	$I_{FS}(E)$	RII = 19.53kΩ, R12 = 20kΩ	—	—	±1/2	—	—	±1	Step
Full Scale Symmetry Error (Note 2)	$I_O(+)$-$I_O(-)$	Decode or Encode pair	—	±1/40	±1/8	—	±1/20	±1/4	Step
Zero Scale Current (Note 2)	I_{ZS}	Measured at selected output with 000 0000 input	1/4	1/2	3/4	1/4	1/2	3/4	Step
Disable Current (Note 2)	I_{DIS}	Disabled by E/D and SB	—	5.0	100	—	5.0	100	nA
Idle Current (Note 2)	I_I		—	10	—	—	10	—	μA
Output Current Range	I_{FSR}		0	2.0	4.2	0	2.0	4.2	mA
Logic Input Levels, Logic "0"	V_{IL}	$V_{LC} = 0V$	—	—	0.8	—	—	0.8	Volts
Logic Input Levels, Logic "1"	V_{IH}	$V_{LC} = 0V$	2.0	—	—	2.0	—	—	Volts
Logic Input Current	I_{IN}	$V_{IN} = -5V$ to +18V	—	—	120	—	—	120	μA
Logic Input Swing	V_{IS}	V− = −15V	−5	—	+18	−5	—	+18	Volts
Reference Bias Current	I_{12}		—	−3.0	−12.0	—	−3.0	−12.0	μA
Reference Input Slew Rate	dI/dt		—	0.25	—	—	0.25	—	mA/μs
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	$PSSI_{FS+}$	V+ = 4.5 to 18V, V− = −15V	—	±1/20	±1/2	—	±1/20	±1/2	Step
	$PSSI_{FS-}$	V− = −10.8V to −18V, V+ = 15V	—	±1/10	±1/2	—	±1/10	±1/2	Step
Power Supply Current	I+	$V_S = +5V, -15V$, $I_{FS} = 2.0mA$	—	2.7	5.5	—	2.7	5.5	mA
	I−	$V_S = +5V, -15V$, $I_{FS} = 2.0mA$	—	−6.7	−12	—	−6.7	−12	mA
	I+	$V_S = \pm 15V$, $I_{FS} = 2.0mA$	—	2.7	5.5	—	2.7	5.5	mA
	I−	$V_S = \pm 15V$, $I_{FS} = 2.0mA$	—	−6.7	−12	—	−6.7	−12	mA
Power Dissipation	P_d	$V_S = +5V, -15V$, $I_{FS} = 2.0mA$	—	114	207	—	114	207	mW
	P_d	$V_S = \pm 15V$, $I_{FS} = 2.0mA$	—	141	262	—	141	262	mW

NOTES

1. Settling time varies for each of the chord bits and step bits and a maximum specification may be misleading. In decode operation, the DAC-89 and OP-16 combination will decode 8 channels. In the encode mode, the DAC-89 and CMP-01 combination will encode 8 channels. Both encode and decode statements assume a 3.9μs channel time.
2. Current specifications relate to differential currents between (+) and (−) output leads. At selected outputs, equal idle currents are present simultaneously on both current output leads.

OUTPUT CURRENT DC TEST CIRCUIT



*VREF IS ADJUSTED BEFORE TESTING EACH DEVICE TO PROVIDE IDEAL FULL SCALE OUTPUT CURRENT.

LINE SELECTION TABLE

TEST GROUP	ENCODE/ DECODE	SIGN BIT	OUTPUT MEASUREMENT	
1	1	1	$I_{OE}(+)$	(E_{01}/R1)
2	1	0	$I_{OE}(-)$	(E_{01}/R2)
3	0	1	$I_{OD}(+)$	(E_{02}/R3)
4	0	0	$I_{OD}(-)$	(E_{02}/R4)

NOTE: — Accuracy is specified in the test circuit using the tables below to be within the specified proportion of a step at the maximum value in each chord. Monotonic operation is guaranteed for all input codes.

CONDENSED CURRENT OUTPUT TABLES

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

	CHORD	0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0.5	16.5	33	66	132	264	528	1056
15	1111	15.5	31.5	63	126	252	504	1008	2016
STEP SIZE		1	1	2	4	8	16	32	64

IDEAL ENCODE OUTPUT CURRRENT IN MICROAMPS AT CHORD ENPOINTS

	CHORD	0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	1	17	34	68	136	272	544	1088
15	1111	16	32	64	128	256	512	1024	2048
STEP SIZE		1	1	2	4	8	16	32	64

These tables may be extended to include all of the encode/decode currents (ideal with $I_{REF} = 512\mu A$) by multiplying any of the numbers in the normalized tables by $0.5\mu A$.

SPECIFICATION PARAMETER DEFINITIONS

STEP NONLINEARITY
Step size deviation from ideal within a chord.

ENCODE CURRENT
The difference between $I_{OE}(+)$ and $I_{OD}(+)$ or the difference between $I_{OE}(-)$ and $I_{OD}(-)$ at any code.

FULL SCALE DRIFT
The change in output current over the full operating temperature with $V_{REF} = 10.000V$, R11 = 19.53kΩ, and R12 = 20kΩ.

FULL SCALE SYMMETRY ERROR
The difference between $I_{OD}(-)$ and $I_{OD}(+)$ or the difference between $I_{OE}(-)$ and $I_{OE}(+)$ at full scale output.

IDEAL OUTPUT CURRENT
The difference between the (+) and (−) currents (encode or decode) at any code.

OUTPUT VOLTAGE COMPLIANCE
The maximum output voltage swing at any current level which causes <½ step change in output current.

CHORDS
Groups of linearly-related steps in the transfer function. Also known as segments.

CHORD ENDPOINTS

The maximum code in each chord. Used to specify accuracy.

STEPS

Increments in each chord which divide it into 16 equal levels.

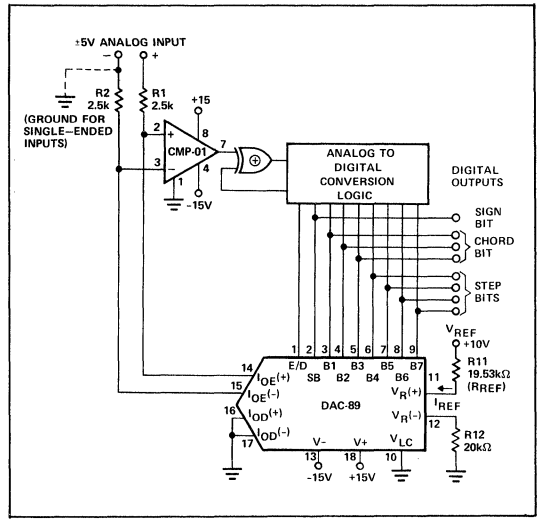
OUTPUT LEVEL NOTATION

Each output current level may be designated by the code $I_{C,S}$ where C = chord number and S = step number. For example, $I_{0,0}$ = zero scale current; $I_{0,1}$ = first step from zero; $I_{0,15}$ = endpoint of first chord (C_0); $I_{7,15}$ = full scale current.

DYNAMIC RANGE

Ratio of full scale current to step size in chord zero expressed in dB.

BASIC ENCODE CONNECTIONS



BASIC ENCODE OPERATION (COMPRESSING A/D CONVERSION)

ENCODING SEQUENCE

An encoding sequence begins with the Sign Bit comparison and decision. During this time the comparator is a polarity detector only. The Encode/Decode (E/D) input is held at a logic "0" so that no current flows into the encode outputs, and the comparator is effectively disconnected from the DAC. Once the input polarity has been determined, the E/D input is changed to a logic "1" allowing current to flow into $I_{OE}(+)$ or $I_{OE}(-)$ depending upon the Sign Bit Answer.

For positive inputs, additional current flows into $I_{OE}(+)$ through R1, and the comparator's output will be entered as the answer for each successive decision. For negative inputs, current flows into $I_{OE}(-)$ through R2 developing a negative voltage which is compared with the analog input. An exclusive-OR gate inverts the comparator's output during negative trials to maintain the proper logic coding, all ones for full scale and all zeros for zero scale.

NORMALIZED ENCODE DECISION LEVELS (SIGN BIT EXCLUDED)

NORMALIZED ENCODE DECISION

	CHORD	0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	2	34	68	136	272	544	1088	2176
1	0001	4	36	72	144	288	576	1152	2304
2	0010	6	38	76	152	304	608	1216	2432
3	0011	8	40	80	160	320	640	1280	2560
4	0100	10	42	84	168	336	672	1344	2688
5	0101	12	44	88	176	352	704	1408	2816
6	0110	14	46	92	184	368	736	1472	2944
7	0111	16	48	96	192	384	768	1536	3072
8	1000	18	50	100	200	400	800	1600	3200
9	1001	20	52	104	208	416	832	1664	3328
10	1010	22	54	108	216	432	864	1728	3456
11	1011	24	56	112	224	448	896	1792	3584
12	1100	26	58	116	232	464	928	1856	3712
13	1101	28	60	120	240	480	960	1920	3840
14	1110	30	62	124	248	496	992	1984	3968
15	1111	32	64	128	256	512	1024	2048	*4096
STEP SIZE		2	2	4	8	16	32	64	128

*Virtual Decision Level

The successive removal technique requires the first magnitude decision to be made at the code 011 1111 and sequentially turning off bits until all decisions have been made.

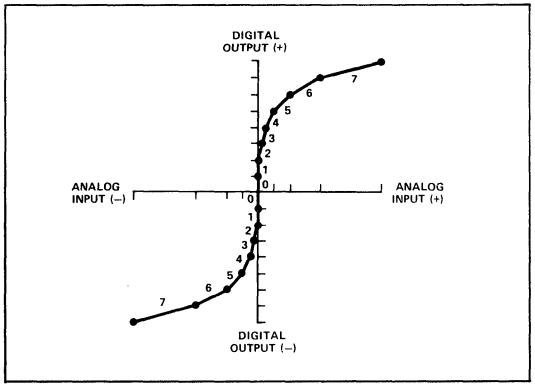
ENCODE DECISION LEVELS

Compressing A/D conversion with the DAC-89 requires a comparator, an exclusive-OR gate, and a successive approximation register — the usual elements in any sign-plus-magnitude A/D converter. However, a compressing ADC has one significant difference from regular A/D converters.

In a conventional (linear) converter, the step size is a constant percentage of full scale, but in a compressing A/D converter, the step size increases as the output changes from zero scale to full scale.

When the DAC is used in the feedback loop of a successive approximation ADC the DAC outputs are used as decision levels to determine the edges of the quantizing bands. When the DAC is used in the decode mode it follows that the outputs must correspond to the center of the quantizing bands. Thus the encode mode output must exceed the decode mode output by one-half step. See AN 39 for further explanation.

ENCODE TRANSFER CHARACTERISTIC (A/D CONVERSION)

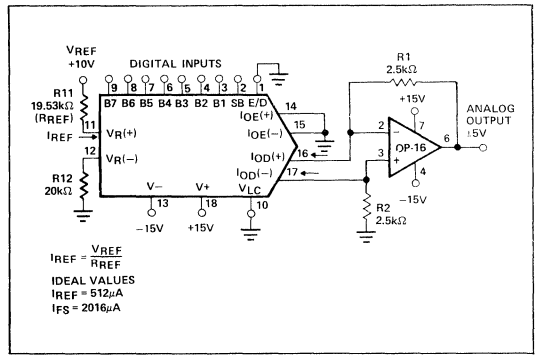


BASIC DECODE OPERATION (EXPANDING D/A CONVERSION)

DECODE OPERATION

D/A conversion with the DAC-89 may be illustrated by using an operational amplifier connected to the decode outputs as a balanced load. The decode mode of operation is selected by applying a logic "0" to the Encode/Decode input. This enables the I_{OD} outputs, disables the I_{OE} outputs, and allows $I_{OD}(+)$ or $I_{OD}(-)$ to be selected by the Sign Bit input. When the Sign Bit input is high, a logic "1", the output current flows into $I_{OD}(+)$ forcing a positive voltage at the operational amplifier's output. When the Sign Bit input is low, a logic "0", the output current flows into $I_{OD}(-)$ through R2 forcing a negative voltage output. Since the Sign Bit only steers current into $I_{OD}(+)$ or $I_{OD}(-)$, the output will always be symmetrical, limited only by the matching of R1 and R2.

BASIC DECODE CONNECTIONS

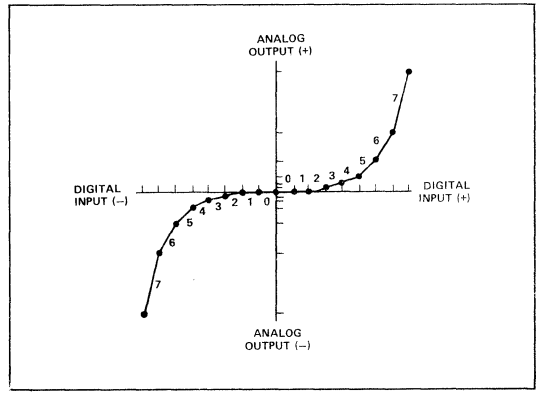


	E/D	SB	B1	B2	B3	B4	B5	B6	B7	E_0
POS FULL SCALE	0	1	1	1	1	1	1	1	1	5.040V
(+) ZERO SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.0012V
(+) ZERO SCALE	0	1	0	0	0	0	0	0	0	0.004V
(–) ZERO SCALE	0	0	0	0	0	0	0	0	0	0.004V
(–) ZERO SCALE +1 STEP	0	0	0	0	0	0	0	0	1	–0.0012V
NEG FULL SCALE	0	0	1	1	1	1	1	1	1	–5.040V

NORMALIZED TABLES

The encode and decode tables may be used to calculate ideal output current at any code point. For example, in decode mode at $I_{3,7}$ (011 0111) find 188. 188/4032 times I_{FS} of 2016μA equals 94μA.

DECODE TRANSFER CHARACTERISTIC (D/A CONVERSION)



NORMALIZED DECODE OUTPUT (SIGN BIT EXCLUDED)

NORMALIZED DECODE OUTPUT

	CHORD	0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	1	33	66	132	264	528	1056	2112
1	0001	3	35	70	140	280	560	1120	2240
2	0010	5	37	74	148	296	592	1184	2368
3	0011	7	39	78	156	312	624	1248	2496
4	0100	9	41	82	164	328	656	1312	2624
5	0101	11	43	86	172	344	688	1376	2752
6	0110	13	45	90	180	360	720	1440	2880
7	0111	15	47	94	188	376	752	1504	3008
8	1000	17	49	98	196	392	784	1568	3136
9	1001	19	51	102	204	408	816	1632	3264
10	1010	21	53	106	212	424	848	1696	3392
11	1011	23	55	110	220	440	880	1760	3520
12	1100	25	57	114	228	456	912	1824	3648
13	1101	27	59	118	236	472	944	1888	3776
14	1110	29	61	122	244	488	976	1952	3904
15	1111	31	63	126	252	504	1008	2016	4032
STEP SIZE		2	2	4	8	16	32	64	128

BASIC REFERENCE CONSIDERATIONS

Full scale output current is ideally 2016μA when the reference current is 512μA in the decode mode. In the encode mode it is 2048μA because the additional one-half step adds 32μA to the output. A percentage change in I_{REF} caused by changes in V_{REF} or R_{REF} will produce the same percentage change in output current.

The large step size at full scale allows the use of inexpensive references in many applications. In some situations V_{REF} may even be the positive power supply. For example, with V+ = 15V, R_{REF} = 15V/512μA or 29.3kΩ. When using a power supply as a reference, R11 should be two resistors, R11A and R11B, and the junction should be bypassed to ground to provide decoupling.

OUTPUT VOLTAGE COMPLIANCE

The DAC-89 has true current outputs with wide voltage compliance enabling fast drive of a variety of single ended and balanced loads. Positive voltage compliance is +18V and negative voltage compliance is −5.0V with I_{REF} = 512μA and V = −15V. Negative voltage compliance $V_{OC}(-)$ for other values of I_{REF} and V− may be obtained from the table, or calculated as follows:

$$V_{OC}(-)\ \text{min} = (V-) + (2\ I_{REF} \times 1.6k\Omega) + 8.4V$$

Output voltage compliance can be extended in both encode and decode modes using the output compliance extension connections.

NEGATIVE OUTPUT VOLTAGE COMPLIANCE $V_{OC}(-)$

V− \ I_{FS}	1.0mA	2.0mA	4.0mA
−12V	−2.8V	−2.0V	−0.4V
−15V	−5.8V	−5.0V	−3.4V
−18V	−8.8V	−8.0V	−6.4V

MINIMUM NEGATIVE COMPLIANCE

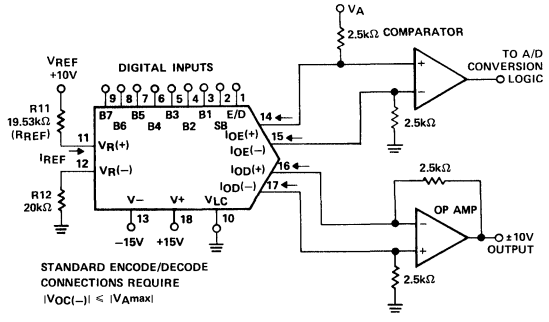
$$V_{OC}(-)\ \text{MIN} = (V-) + (2I_{REF}\ 1.6k\Omega) + 8.4V$$

IDLE OUTPUT CURRENT

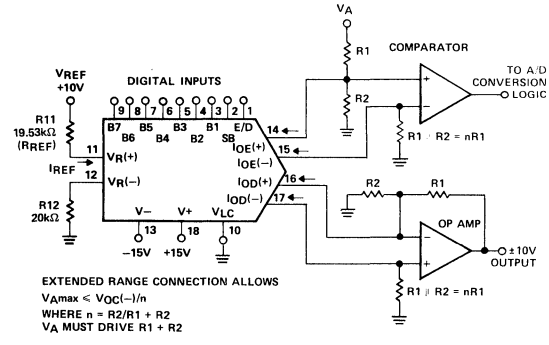
In the selected output state (encode or decode), equivalent idle currents are present on the (+) and (−) output leads. The output will be symmetrical with the external resistor matching determining the overall system accuracy.

OUTPUT COMPLIANCE EXTENSION CONNECTIONS

STANDARD ENCODE DECODE CONNECTIONS



EXTENDED RANGE CONNECTIONS



IDEAL DECODE OUTPUT CURRENT IN MICROAMPS (SIGN BIT EXCLUDED)

IDEAL DECODE OUTPUT

	CHORD	0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0.5	16.5	33	66	132	264	528	1056
1	0001	1.5	17.5	35	70	140	280	560	1120
2	0010	2.5	18.5	37	74	148	286	592	1184
3	0011	3.5	19.5	39	78	156	312	624	1248
4	0100	4.5	20.5	41	82	164	328	656	1312
5	0101	5.5	21.5	43	86	172	344	688	1376
6	0110	6.5	22.5	45	90	180	360	720	1440
7	0111	7.5	23.5	47	94	188	376	752	1504
8	1000	8.5	24.5	49	98	196	392	784	1568
9	1001	9.5	25.5	51	102	204	408	816	1632
10	1010	10.5	26.5	53	106	212	424	848	1696
11	1011	11.5	27.5	55	110	220	440	880	1760
12	1100	12.5	28.5	57	114	228	456	912	1824
13	1101	13.5	29.5	59	118	236	472	944	1888
14	1110	14.5	30.5	61	122	244	488	976	1952
15	1111	15.5	31.5	63	126	252	504	1008	2016
STEP SIZE		1	1	2	4	8	16	32	64

DMX-88

8-CHANNEL ANALOG DE-MULTIPLEXER FOR PCM CODECs

LOW CHARGE TRANSFER

FEATURES

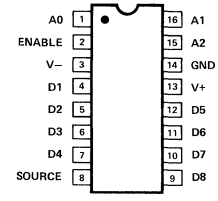
- **Low Charge Transfer — 18pC Typical**
- **Compatible with Standards for Noise and Crosstalk in Telephony Systems**
- **Pin Compatible with DG508, HI-508A, LF12508/13508**
- **JFET Switches Rather Than CMOS**
- **Low "ON" Resistance — 220Ω Typical**
- **Low Output Leakage Current — 100nA Maximum**
- **Digital Inputs Compatible with TTL and CMOS**
- **No Pullup Resistors Required to Ensure Break-Before-Make Action with TTL Inputs**

GENERAL DESCRIPTION

The DMX-88 is a 8-channel analog de-multiplexer which is ideally suited for use in shared-channel PCM decoder systems. Typical crosstalk at 20kHz is 98dB. Monolithic construction makes possible this kind of performance while keeping the price reasonable. The DMX-88 makes use of digital logic to select the one-of-eight channels to be presented to the output. In addition, there is an ENABLE input which permits turning OFF all channels. Using this function permits selection of any given circuit in a system employing multiple devices.

Fabricated with Precision Monolithics' high performance Bi-FET technology, this device offers low, constant "ON" resistance. In addition the multiplexer has fast settling times and low leakage currents necessary to satisfy the requirements of an 8-channel PCM DECODER. This de-multiplexer does not suffer from latch-up and is highly resistant to static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pull-up resistors.

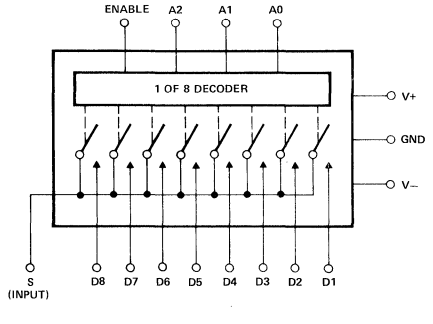
PIN CONNECTIONS & ORDERING INFORMATION



16-PIN HERMETIC DUAL-IN-LINE (Q-Suffix)

R_{ON}	MODEL	TEMP RANGE
400Ω	DMX88EQ	IND
520Ω	DMX88FQ	IND

FUNCTIONAL DIAGRAM & TRUTH TABLE



A_2	A_1	A_0	E_N	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

"X" = DON'T CARE

ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Operating Temperature Range,
DMX-88EQ, FQ ..... −25°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Power Dissipation 500mW
Derate about 100°C ..... 10mW/°C
Lead Soldering Temperature ..... 300°C (60 sec)

V+ Supply to V− Supply 36V
V+ Supply to Ground 18V
Logic Input Voltage ..... −4V to V+ Supply
Analog Input Voltage ..... V− Supply −20V to V+ Supply
Maximum Current Through Any Pin 25mA

ELECTRICAL CHARACTERISTICS These specifications apply for V+ = 15V, V− = −15V and $-25°C \le T_A \le 85°C$ unless otherwise specified.

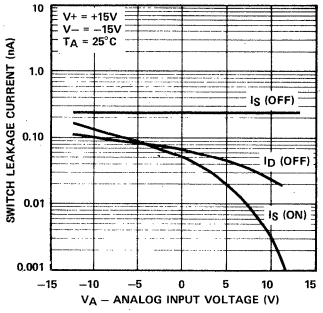
PARAMETER	SYMBOL	CONDITIONS	DMX-88E MIN	DMX-88E TYP	DMX-88E MAX	DMX-88F MIN	DMX-88F TYP	DMX-88F MAX	UNITS
ON Resistance	R_{ON}	$V_D = 0V$, $I_S = 100\mu A$	—	—	400	—	—	520	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \le V_D \le 10V$, $I_S = 100\mu A$	—	1.5	—	—	4.5	—	%
R_{ON} Match Between Switches	R_{ON} Match	$V_D = 0V$, $I_S = 100\mu A$	—	25	—	—	30	—	Ω
Analog Voltage Range	V_A	$I_S = 100\mu A$	+10 −10	+11 −15	— —	+10 −10	+11 −15	— —	V
Drain Current (Switch OFF)	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Note 1)	—	—	10	—	—	10	nA
Source Current (Switch OFF)	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Note 1)	—	—	100	—	—	100	nA
Charge Transfer		$R_S = 0$, $C_L = 200pF$ $V_{IN} = 0$ (Note 4)	—	18	25	—	18	25	pC
Leakage Current (Switch ON)	$I_{S(ON)}$	$V_D = 10V$ (Note 1)	—	—	100	—	—	100	nA
Digital "1" Input Voltage	V_{INH}		2.0	—	—	2.0	—	—	V
Digital "0" Input Voltage	V_{INL}		—	—	0.8	—	—	0.8	V
Digital "0" Input Current	I_{INL}	$V_{IN} = 0.7V$	—	—	20	—	—	20	μA
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.7V$	—	—	20	—	—	20	μA
Positive Supply Current	I+	All Digital Inputs Logic "0"	—	—	15	—	—	15	mA
Negative Supply Current	I−	All Digital Inputs Logic "0"	—	—	5.0	—	—	5.0	mA
Switching Time	t_{ON}	Figure 1 $C_L = 10pF$	—	0.8	—	—	1.5	—	μs
Output Settling Time	t_s	10V Step 0.10% 10V Step 0.05% 10V Step 0.02%	— — —	1.3 1.5 2.3	— — —	— — —	1.7 1.7 1.7	— — —	μs
Break-Before-Make Delay	t_{DLY}	Figure 3	—	0.8	—	—	1.0	—	μs
Enable Delay ON	$t_{ON(EN)}$	$C_L = 10pF$	—	1.0	—	—	1.2	—	μs
Enable Delay OFF	$t_{OFF(EN)}$	$C_L = 10pF$	—	0.2	—	—	0.2	—	μs
OFF Isolation	ISO_{OFF}	(Note 3)	—	88	—	—	88	—	dB
Crosstalk	CT	(Note 2)	—	98	—	—	98	—	dB
Drain Capacitance	$C_{D(OFF)}$	Switch OFF, $V_S = 0V$, $V_D = 0V$	—	2.5	—	—	2.5	—	pF
Source Capacitance	$C_{S(OFF)}$	Switch OFF, $V_S = 0V$, $V_D = 0V$	—	7	—	—	7	—	pF
Input to Output Capacitance	$C_{DS(OFF)}$	(Note 3)	—	0.3	—	—	0.3	—	pF

NOTES:

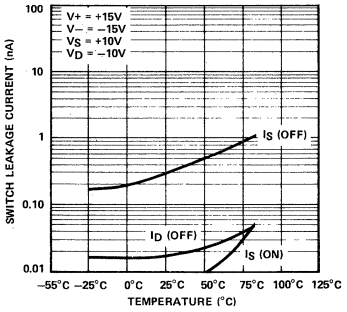
1. Conditions applied to leakage tests insure worst case leakages. Exceeding 11V on the analog input may cause an OFF channel to turn ON.
2. Crosstalk is measured by driving channel 8 with channel 4 ON. $R_L = 1M\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, f = 20kHz.
3. OFF isolation is measured by monitoring channel 8 with ALL channels OFF. $R_L = 1k\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, f = 20kHz. C_{DS} is computed from the OFF isolation measurement.
4. Guaranteed by design.

TYPICAL PERFORMANCE CURVES

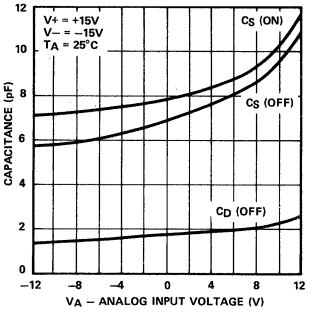
SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE



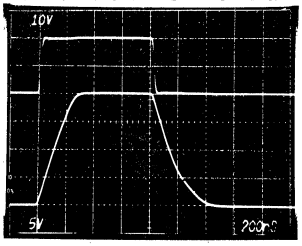
SWITCH LEAKAGE CURRENTS vs TEMPERATURE



SWITCH CAPACITANCE vs ANALOG INPUT VOLTAGE

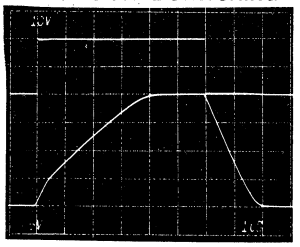


LARGE SIGNAL SWITCHING



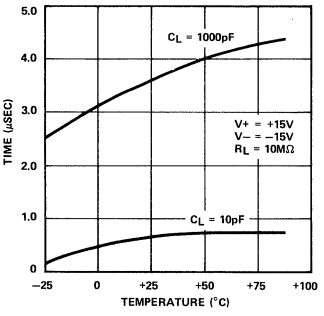
RL = 1MΩ, CL = 100pF, VIN = ±10V

LARGE SIGNAL SWITCHING

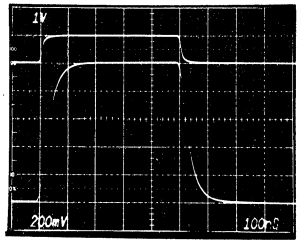


RL = 1MΩ, CL = 1000pF, VIN = ±10V

SWITCHING TIME vs TEMPERATURE

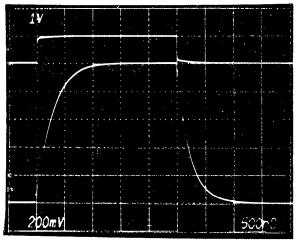


SMALL SIGNAL SWITCHING



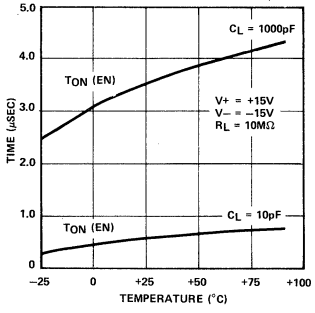
RL = 1MΩ, CL = 100pF, VIN = ±0.5V

SMALL SIGNAL SWITCHING



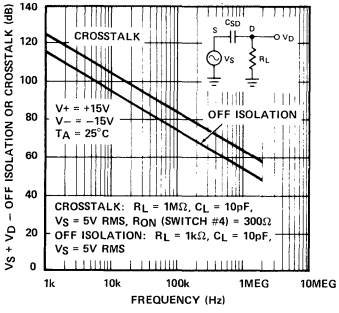
RL = 1MΩ, CL = 1000pF, VIN = ±0.5V

ENABLE DELAY TIME vs TEMPERATURE

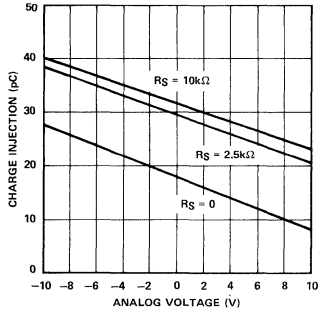


TYPICAL PERFORMANCE CURVES

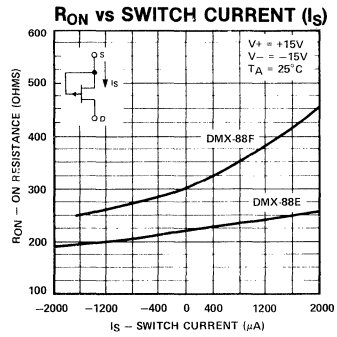
OFF PERFORMANCE OF CHANNEL 8



CHARGE INJECTION vs ANALOG VOLTAGE

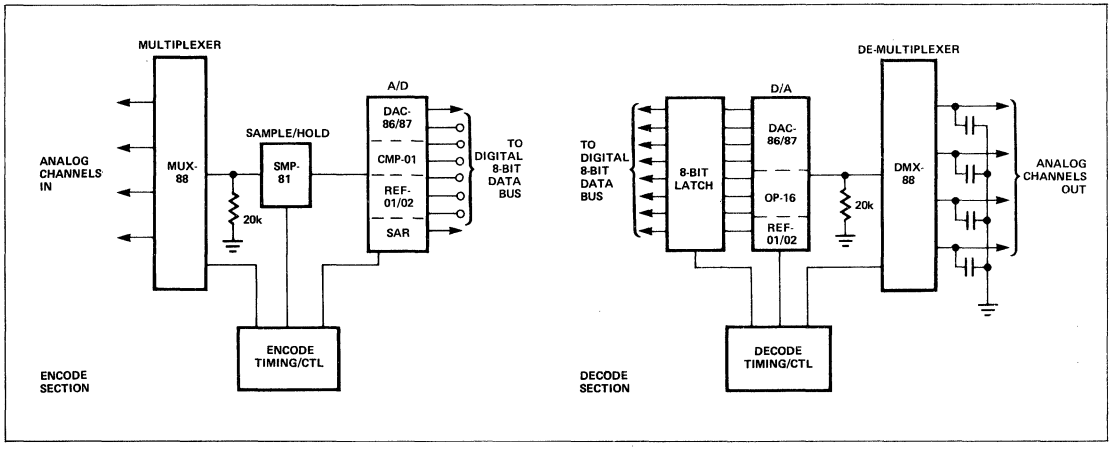


R_{ON} vs SWITCH CURRENT (I_S)



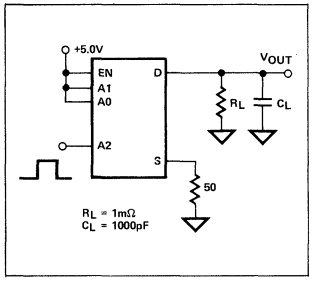
TYPICAL APPLICATION

FOUR-CHANNEL SHARED CHANNEL PCM CODEC

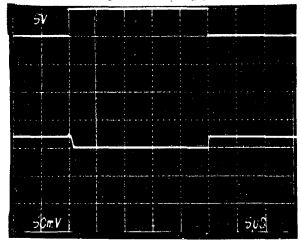


CHARGE TRANSFER

TEST CIRCUIT

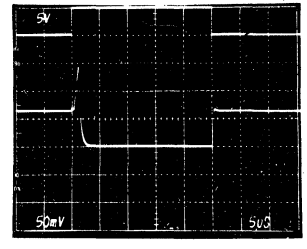


TYPICAL CHARGE TRANSFER OF DMX-88



TOP TRACE: ADDRESS INPUT
BOTTOM TRACE: DRAIN OUTPUT

TYPICAL CHARGE TRANSFER OF CONVENTIONAL BI-FET SWITCH



TOP TRACE: ADDRESS INPUT
BOTTOM TRACE: DRAIN OUTPUT

A.C. TEST CIRCUITS

SWITCHING TIME — T_{ON} AND T_{ENABLE}

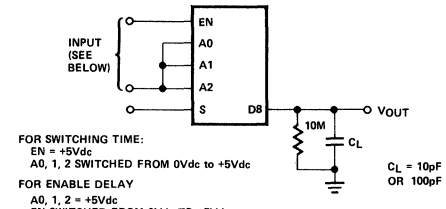


FIGURE 1.

BREAK-BEFORE-MAKE DELAY

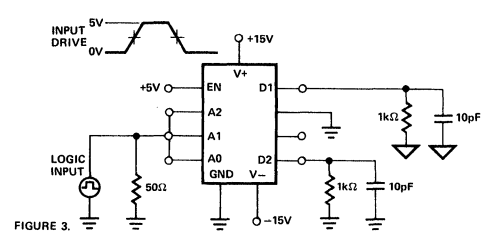


FIGURE 3.

CROSSTALK MEASUREMENT CIRCUIT

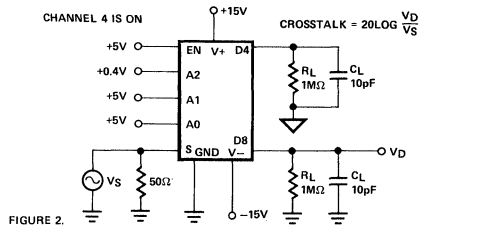


FIGURE 2.

OFF ISOLATION MEASUREMENT CIRCUIT

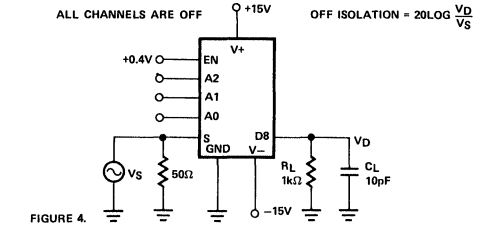


FIGURE 4.

APPLICATIONS INFORMATION

These de-multiplexers employ ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with BI-FET processing rather than CMOS, **special handling is not necessary to prevent damage to this multiplexer**. Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pullup resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS devices. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised about $\approx$1.4V.

The ON resistance, R_{ON}, of the analog switches is constant over the wide input voltage range of $-15V$ to $+11V$ with $V_{SUPPLY} = \pm 15V$. Higher input voltage is tolerable provided that some form of current limiting is employed (such as that of an op-amp output stage) to avoid exceeding junction temperature and power dissipation requirements. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF switch remains greater than its V_p, and prevents that channel from being falsely turned ON. When operating with negative input voltages, the gate-to-channel diode will be turned on if the voltage drop across an ON switch exceeds $-0.6V$. While this condition will cause an error in the output, it will not damage the switch.

CROSSTALK IN PCM SYSTEMS

In PAM or PCM systems crosstalk specifications for components, such as multiplexers or de-multiplexers, are related to overall system crosstalk specifications in a complex manner. Component specification must, of necessity, refer to the operation of the multiplexer in a non-sampling mode of operation. When rapid sequential sampling takes place, such as would be the case with a typical shared-channel CODEC, crosstalk will be caused by the off isolation properties of the multiplexer as well as by storage elements on chip and PC card stray capacitance. For example, the capacitance has the effect of conferencing the channels and increasing crosstalk. Thus, system crosstalk in a shared-channel PCM CODEC is influenced by multiplexed characteristics as well as PC card layout and the timing relationship between the multiplexer and the sample-hold circuit.

MUX-88
8-CHANNEL ANALOG MULTIPLEXER FOR PCM CODECs
OVERVOLTAGE PROTECTED

FEATURES

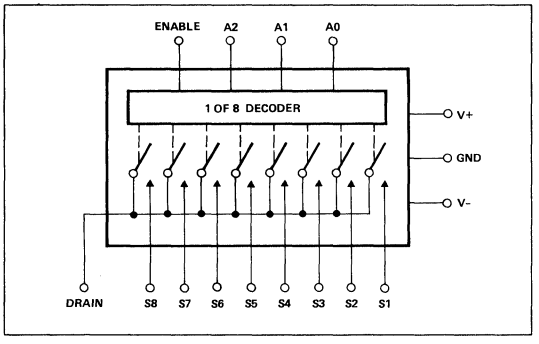
- **Compatible with Standards for Noise and Crosstalk in Telephony Systems**
- **Pin Compatible with DG508, HI-508A, LF11508**
- **JFET Switches Rather Than CMOS**
- **Low "ON" Resistance — 220Ω Typical**
- **Low Output Leakage Current — 100nA Maximum**
- **Digital Inputs Compatible with TTL and CMOS**
- **No Pullup Resistors Required to Ensure Break-Before-Make Action with TTL Inputs**

GENERAL DESCRIPTION

The MUX-88 is a 8-channel analog multiplexer which is ideally suited for use in shared-channel PCM CODEC systems. Typical crosstalk at 20kHz is 98dB. Monolithic construction makes possible this kind of performance while keeping the price reasonable. The MUX-88 makes use of digital logic to select the one-of-eight channels to be presented to the multiplexer output. In addition, there is an ENABLE input which permits turning OFF all channels. Using this function permits selection of any given multiplexer in a system employing multiple devices.

Fabricated with Precision Monolithics' high performance BI/FET technology, this device offers low, constant "ON" resistance. In addition the multiplexer has fast settling times and low leakage currents necessary to satisfy the requirements of a 8-channel PCM CODEC. This multiplexer does not suffer from latch-up and is highly resistant to static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pull-up resistors.

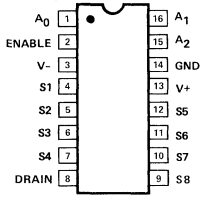
FUNCTIONAL DIAGRAM



TRUTH TABLE

A_2	A_1	A_0	E_N	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

PIN CONNECTIONS & ORDERING INFORMATION



TOP VIEW
16-PIN HERMETIC DUAL-IN-LINE
(Q-Suffix)

R_{ON}	MODEL	TEMP RANGE
400Ω	MUX-88EQ	IND
520Ω	MUX-88FQ	IND

ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Operating Temperature Range,
MUX-88EQ, FQ ..... −25°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Power Dissipation 500mW
Derate about 100°C ..... 10mW/°C
Lead Soldering Temperature ..... 300°C (60 sec)

V+ Supply to V− Supply 36V
V+ Supply to Ground 18V
Logic Input Voltage ..... −4V to V+
Analog Input Voltage ..... V− Supply −20V to V+
Maximum Current Through Any Pin 25mA

ELECTRICAL CHARACTERISTICS

These specifications apply for V+ = 15V, V− = −15V and $-25°C \le T_A \le 85°C$ unless otherwise specified.

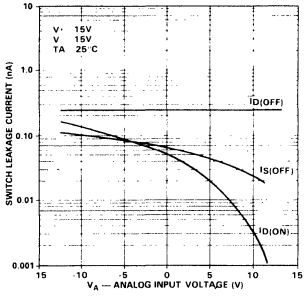
PARAMETER	SYMBOL	CONDITIONS	MUX-88E MIN	MUX-88E TYP	MUX-88E MAX	MUX-88F MIN	MUX-88F TYP	MUX-88F MAX	UNITS
"ON" Resistance	R_{ON}	$V_D = 0V$, $I_S = 100\mu A$	—	—	400	—	—	520	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \le V_D \le 10V$, $I_S = 100\mu A$	—	1.5	—	—	4.5	—	%
R_{ON} Match Between Switches	R_{ON} Match	$V_D = 0V$, $I_S = 100\mu A$	—	25	—	—	30	—	Ω
Source Current (Switch "OFF")	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Note 1)	—	—	10	—	—	10	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Note 1)	—	—	100	—	—	100	nA
Leakage Current (Switch "ON")	$I_{D(ON)}$	$V_D = 10V$ (Note 1)	—	—	100	—	—	100	nA
Digital "1" Input Voltage	V_{INH}		2.0	—	—	2.0	—	—	Volts
Digital "0" Input Voltage	V_{INL}		—	—	0.8	—	—	0.8	Volts
Digital Input Current	I_{IN}	$V_{IN} = 0.7V$ to $+5V$	—	—	20	—	—	20	μA
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.7V$	—	—	20	—	—	20	μA
Positive Supply Current	I+	All Digital Inputs Logic "0"	—	—	15	—	—	15	mA
Negative Supply Current	I−	All Digital Inputs Logic "0"	—	—	5.0	—	—	5.0	mA
Switching Time	t_{TRAN}	Figure 1 (Note 2)	—	1.0	1.3	—	1.5	2.1	μsec
Output Settling Time	t_s	10V Step 0.10%	—	1.3	—	—	1.7	—	μsec
	t_s	10V Step 0.05%	—	1.5	—	—	1.7	—	μsec
	t_s	10V Step 0.02%	—	2.3	—	—	1.7	—	μsec
Break-Before-Make Delay	t_{DLY}	Figure 3	—	0.8	—	—	1.0	—	μsec
Enable Delay "ON"	$t_{ON(EN)}$		—	1.0	—	—	1.2	—	μsec
Enable Delay "OFF"	$t_{OFF(EN)}$		—	0.2	—	—	0.2	—	μsec
"OFF" Isolation	ISO_{OFF}	(Note 4)	—	88	—	—	88	—	dB
Crosstalk	CT	(Note 3)	—	98	—	—	98	—	dB
Source Capacitance	$C_{S(OFF)}$	Switch "OFF", $V_S = 0V$, $V_D = 0V$	—	2.5	—	—	2.5	—	pF
Drain Capacitance	$C_{D(OFF)}$	Switch "OFF", $V_S = 0V$, $V_D = 0V$	—	7	—	—	7	—	pF
Input to Output Capacitance	$C_{DS(OFF)}$	(Note 4)	—	0.3	—	—	0.3	—	pF

NOTES:

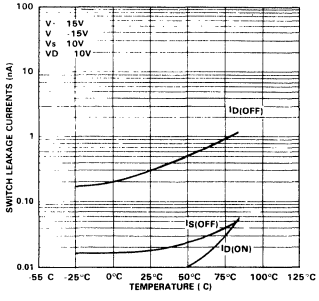
1. Conditions applied to leakage tests insure worst case leakages. Exceeding 11V on the analog input may cause an "OFF" channel to turn "ON."
2. Sample tested. The measurement conditions of FIGURE 1 insure worst case transition time.
3. Crosstalk is measured by driving channel 8 with channel 4 ON. $R_L = 1M\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, f = 20kHz.
4. OFF isolation is measured by driving channel 8 with ALL channels OFF. $R_L = 1k\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, f = 20kHz. C_{DS} is computed from the OFF isolation measurement.

TYPICAL PERFORMANCE CURVES

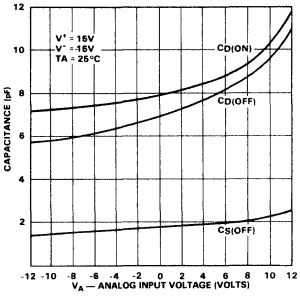
SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE



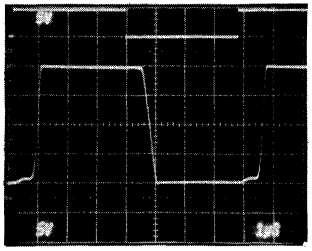
SWITCH LEAKAGE CURRENTS vs TEMPERATURE



SWITCH CAPACITANCE vs ANALOG INPUT VOLTAGE

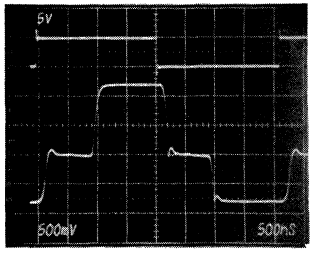


LARGE SIGNAL SWITCHING



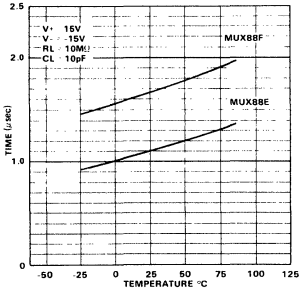
*R_L = 1MΩ, C_L = 10pF, V_1 = –500mV
VOLTAGE = 500mV/DIV, TIME = 1μS/DIV
SEE TRANSISTION TIME CIRCUIT

BREAK-BEFORE-MAKE SWITCHING



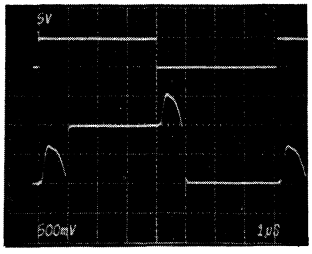
*VOLTAGE = 500mV/DIV, TIME = 500nS/DIV
SEE BREAK-BEFORE-MAKE CIRCUIT

TRANSITION TIMES vs TEMPERATURE



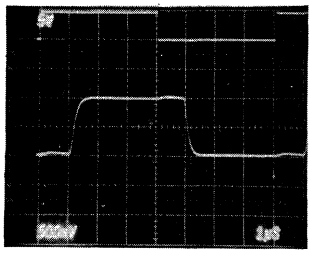
*TOP WAVEFORMS: DIGITAL INPUT –5V/DIV
BOTTOM WAVEFORMS: MULTIPLEX OUTPUT – SEE PHOTO

SMALL SIGNAL SWITCHING



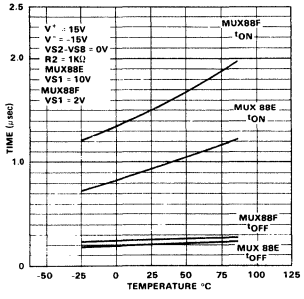
*R_L = 1MΩ, C_L = 500pF, V_1 = –500mV,
V_8 = +500mV VOLTAGE = 500mV/DIV,
TIME = 1μS/DIV
SEE TRANSITION CIRCUIT

SMALL SIGNAL SWITCHING WITH FILTERING



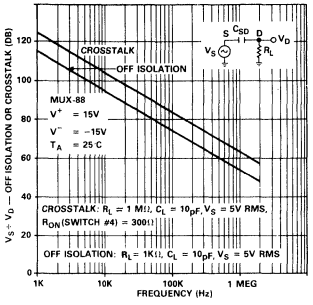
*R_L = 1MΩ, C_L = 10pF, V_S = +10V
VOLTAGE = 5V/DIV, TIME = 1μS/DIV
SEE TRANSISTION TIME CIRCUIT

ENABLE DELAY TIME vs TEMPERATURE

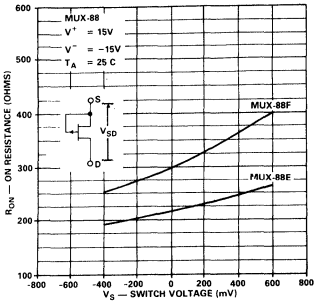


TYPICAL PERFORMANCE CURVES (continued)

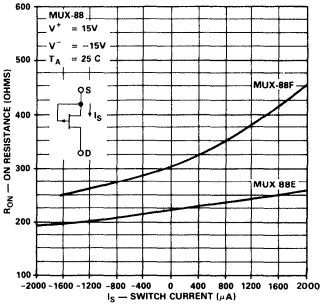
OFF PERFORMANCE OF CHANNEL 8



R_{ON} vs SWITCH VOLTAGE (V_{SD})

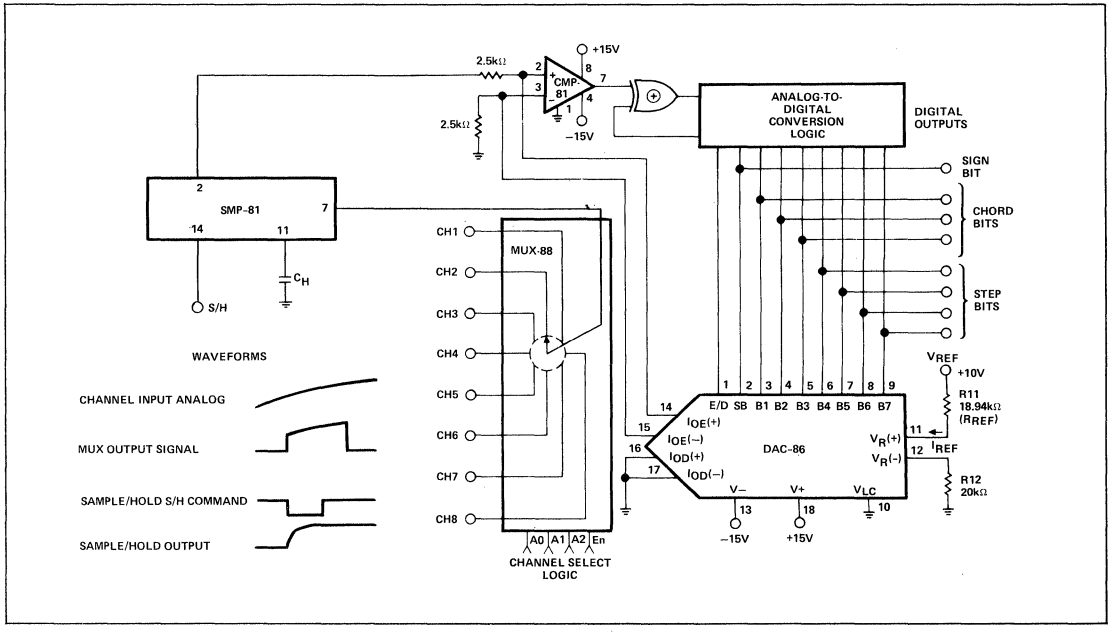


R_{ON} vs SWITCH CURRENT (I_S)



TYPICAL APPLICATION

EIGHT-CHANNEL SHARED CODEC PCM ENCODER



CROSSTALK IN PCM SYSTEMS

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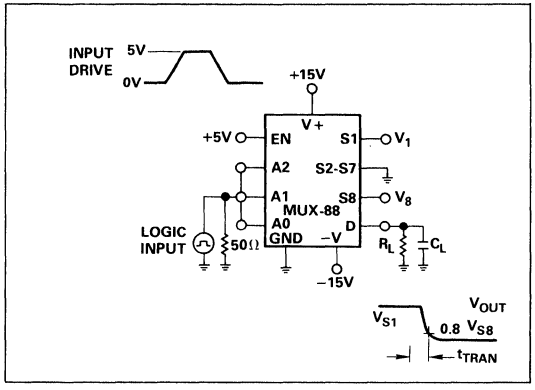
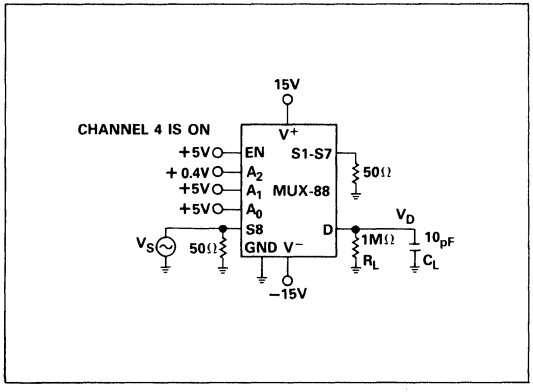
A.C. TEST CIRCUITS

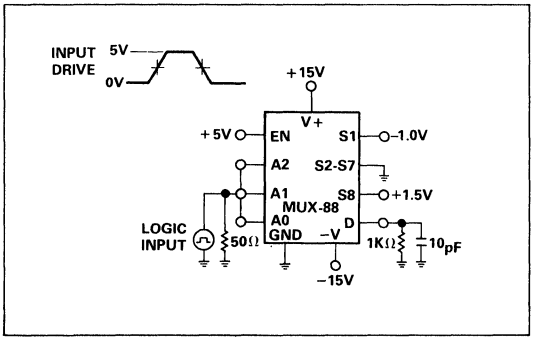
TRANSITION TIME



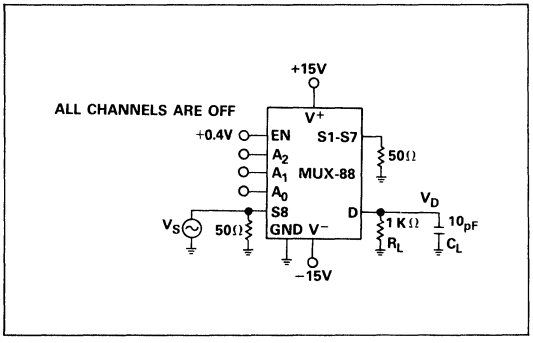
CROSSTALK MEASUREMENT CIRCUIT



BREAK-BEFORE-MAKE DELAY



OFF ISOLATION MEASUREMENT CIRCUIT



APPLICATIONS INFORMATION

These analog multiplexers employ ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with BI-FET processing rather than CMOS, **special handling is not necessary to prevent damage to this multiplexer**. Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pullup resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS multiplexers. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised about ≈1.4V.

The "ON" resistance, R_{ON}, of the analog switches is constant over the wide input voltage range of −15V to +11V with V_{SUPPLY} = ±15V. Higher input voltage is tolerable provided that some form of current limiting is employed (such as that of an op-amp output stage) to avoid exceeding junction temperature and power dissipation requirements. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF switch remains greater than its V_p, and prevents that channel from being falsely turned ON. When operating with negative input voltages, the gate-to-channel diode will be turned on if the voltage drop across an ON switch exceeds −0.6V. While this condition will cause an error in the output, it will not damage the switch. In lab tests, the multiplexer output has been loaded with a 0.01μF capacitor in the Transition Time circuit. With V_1 = −10V and V_8 = +10V, the logic input was driven as a 1kHz rate. The positive-going slew rate was 0.3V/μsec which is equivalent to a normal I_{DSS} of 3mA. The negative-going slew rate was 0.7V/μsec which is equivalent to a "reverse" I_{DSS} of 7mA. Note that when switch 1 is first turned ON it has a drop of −20V across its terminals. In spite of that fact, the current is limited to approximately twice its normal I_{DSS}.

DICE

For applicable DICE information see MUX-08 Data Sheet.

RPT-81/RPT-82
PCM CARRIER REPEATERS

FEATURES

- **On-Chip ALBO Diode**
- **Clock Shutdown Circuit (RPT-81)**
- **On-Chip Voltage Regulator (RPT-81)**
- **Low Power Operation (100mW)**
- **Pin-Compatible with XR-C277**
- **Improved Pre-Amplifier Response (RPT-82)**

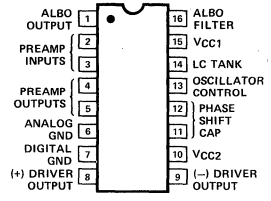
GENERAL DESCRIPTION

The PMI PCM Repeater Circuits are monolithic integrated circuits which perform all the active functions required for a regenerative repeater operating at 1.544-2.048 Mega-bits per second (Mbps) data rates on PCM lines.

In a PCM carrier system, coded information is transmitted over paired cables by the presence or absence of pulses in specified time slots. The RPT-81/RPT-82 regenerate all pulses that meet threshold requirements without inserting pulses incorrectly during empty time slots.

Additional system functions have been incorporated on-chip. These include an Automatic Line Build Out (ALBO) circuit that compensates for 36dB of line loss and an oscillator control pin that permits injectioned-locked (free-running) or pulsed-tank operation. The RPT-81 also incorporates an automatic clock shutdown circuit. The clock shutdown inhibits the clock amplifier when no signal is applied, greatly reducing system noise.

PIN CONNECTIONS AND ORDERING INFORMATION

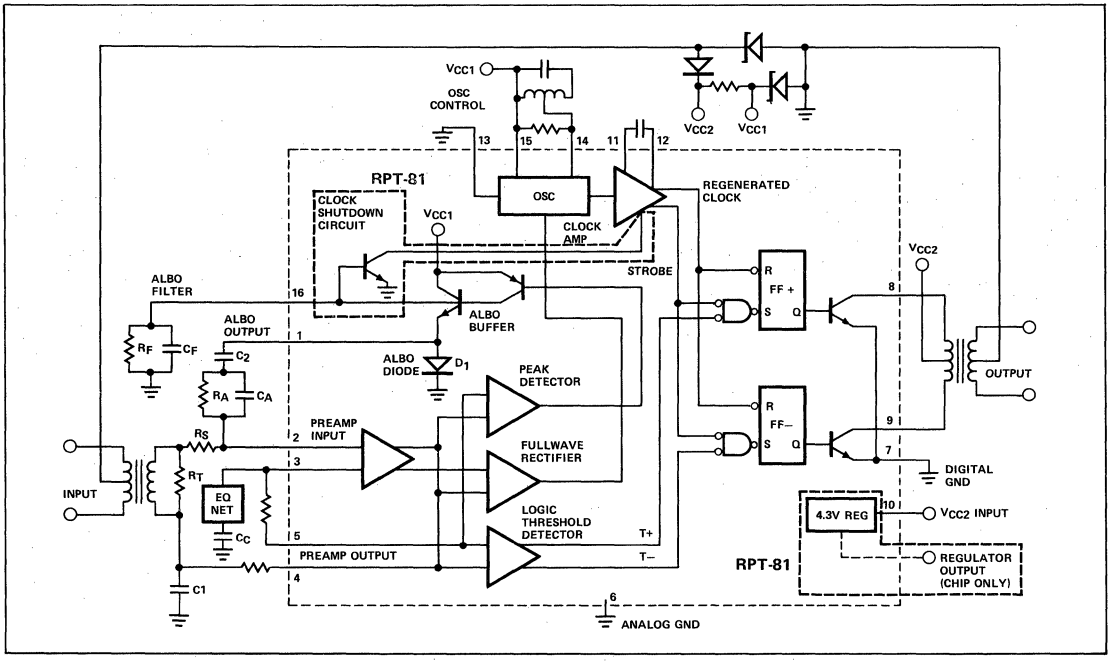


16-PIN HERMETIC DUAL-IN-LINE
(Q-Suffix)

RPT-81-FQ
RPT-82-FQ

*The on-chip (RPT-81) 4.3V regulated output voltage is not available for external use in 16-Pin package.

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Biopolar pulse transmission, the transmission of alternately positive and negative pulses, is used on repeatered lines to remove the DC component from the unipolar PCM pulse train. This also places the principle energy components in the 0-1.544MHz band, as opposed to the 0-3.088MHz band for the unipolar pulse train. The absence of a DC component in the bipolar pulse train permits the repeater to be transformer coupled to the line and helps to prevent time shifting of the regenerator firing level with variation in input pulse density.

The bipolar PCM pulse train is transformer coupled into the preamplifier as shown in the RPT-81/RPT-82 functional block diagram. The secondary of the input transformer is loaded with the proper terminating resistor R_T to match the line impedance. One side of the transformer secondary is AC coupled to ground by capacitor C1, the other side of the secondary winding is in series with resistance R_S. Resistor R_S and RC network R_AC_A are AC coupled to the ALBO output by capacitor C2. The impedance from the ALBO output to ground is governed by the amount of current through the ALBO diode. R_S in series with R_AC_A provides maximum signal attenuation when maximum current flows through the ALBO diode. When minimum current flows through the ALBO, diode C2 is effectively isolated from ground and the input signal attenuation is minimal. The RPT-81/RPT-82 ALBO circuits can compensate for 36dB of line loss.

The preamplifier amplifies the signal and applies it to the three comparators labeled *logic threshold detector, fullwave rectifier,* and *peak detector,* respectively. Each comparator is set to trigger on both positive and negative pulses. Each comparator trips at a different threshold. The logic threshold is set to trip at the 50% point, the fullwave rectifier trips at the 65% point, and the peak detector trips at peak amplitude. Thresholds and waveforms are drawn on the RPT-81/RPT-82 waveforms and thresholds diagram.

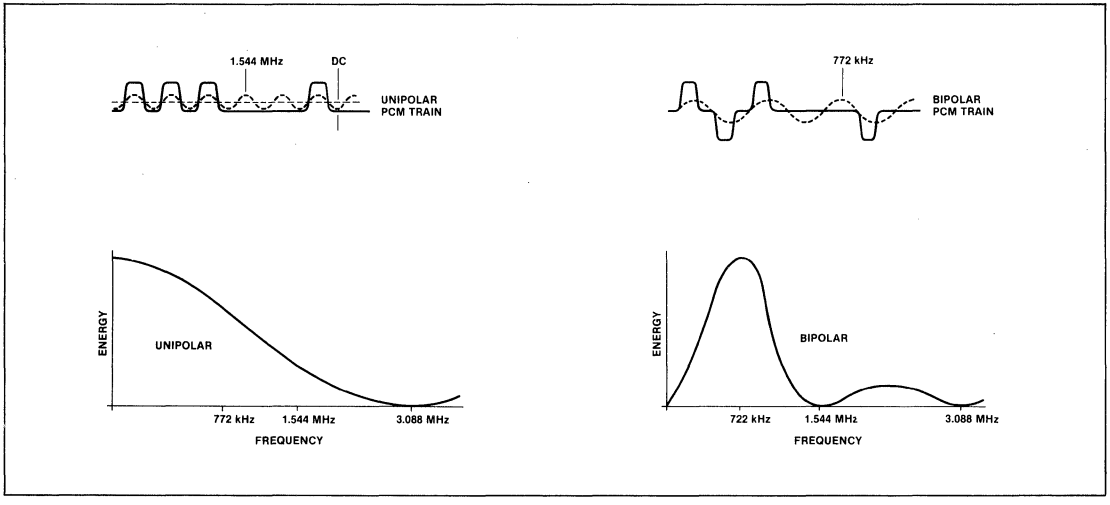
The peak detector output charges the capacitor of the ALBO filter. The voltage on this capacitor causes a relatively constant current to flow through D1 by means of the emitter follower ALBO buffer. A decaying voltage on the ALBO filter enables the clock shutdown circuit when there is no input signal. The clock shutdown circuit turns off the clock amplifier so that neither the regenerated clock nor the strobe outputs are sent to FF+ or FF– flip flops.

The fullwave detector output injection locks the oscillator to the input frequency. The clock amplifier shapes the oscillator output and shifts it in time. The phase shift capacitor of the clock amplifier is selected such that the strobe pulse will occur as close as possible to the center of an incoming pulse. When the regenerated clock waveform goes low, it resets both FF+ and FF–. A 0 to 30pF capacitor (10pF is typical) selection is made to optimize noise performance for a complete repeater.

The logic threshold detector has an output on the T+ line for a positive pulse and an output on the T– line for a negative pulse. The T+ line enables the NAND gate of FF+ and the T– line enables the NAND gate of FF–. A T+ output pulse from the logic threshold detector is ANDed with the strobe pulse to set the FF+ flip flop which turns on its corresponding output transistor, causing current to flow through one half of the output transformer primary. A positive output pulse results. Similarly, A T– output pulse and a strobe pulse are ANDed to set the FF– flip flop, thus causing a negative output pulse. The flip flops are turned off (and the output pulse terminated) by the regenerated clock pulse. In this way the output pulse is controlled by the oscillator tank circuit and not the incoming pulse.

When pin 13 is grounded the full wave detector injection locks the oscillator to the input frequency with pin 13 ungrounded the system operates in the "pulsed tank" mode.

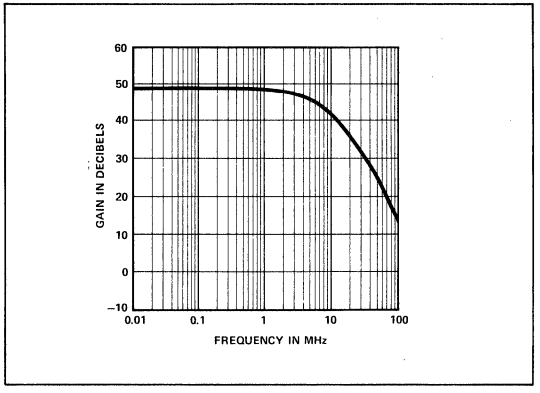
ENERGY SPECTRA OF BIPOLAR AND UNIPOLAR PULSE TRAINS



PREAMPLIFIER

The preamplifier must have wideband frequency response in order to amplify the 1.544Mb/sec pulse train. In addition it must have well behaved roll-off characteristics for the purpose of applying feedback.

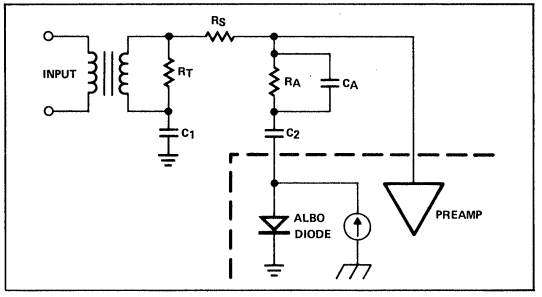
PREAMPLIFIER FREQUENCY RESPONSE



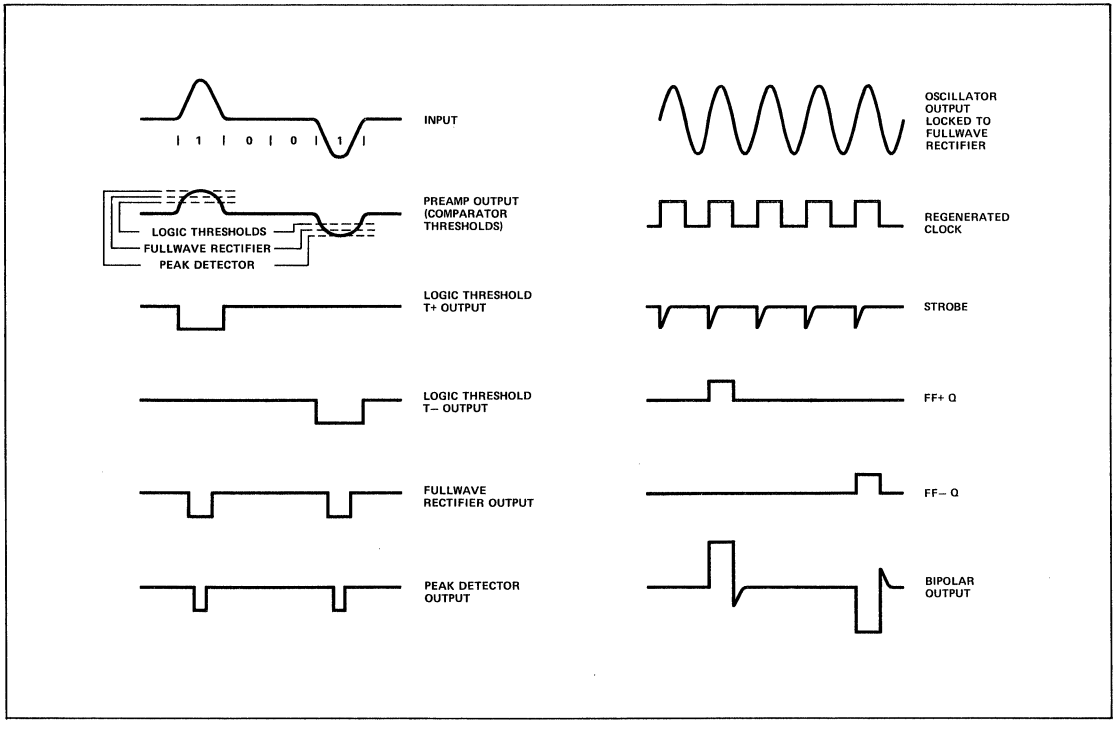
AUTOMATIC LINE BUILDOUT EXTERNAL CIRCUIT

The external circuitry required to achieve automatic line buildout must attenuate the signal while simultaneously matching the transformer to the line. Capacitors C1 and C2 are blocking capacitors. R_A and C_A in parallel shape the frequency response of the attenuator network to compensate for the reactive source impedance of the line. Resistor R_T provides an input match to this line. R_S is the series branch of the attenuator.

AUTOMATIC LINE BUILDOUT EXTERNAL CIRCUITRY



WAVEFORMS AND THRESHOLDS



ABSOLUTE MAXIMUM RATINGS

Pin 10 to Pin 7 or 6 ..... 16.0V, −0.2V
Pin 15 to Pin 7 or 6 ..... 8.0V, −0.2V
Maximum Voltage at Pins 8 or 9 ..... 30V, −0.2V
Maximum Voltage at Pins 2, 3, 4, 5, 11, 12, 14 ..... V_{CC2}
Maximum Sinking Current at Pin 8 or 9 ..... 300mA

Operating Temperature Range ..... −40°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Power Dissipation 500mW
Lead Soldering Temperature ..... 300°C

REPEATER DEFINITIONS

ALBO THRESHOLD

The differential voltage measured between pins 4 and 5, required to activate the internal peak detector.

AUTOMATIC LINE BUILD OUT

An automatic gain control circuit which operates by simulating a line "build-out" or extension.

BIPOLAR VIOLATION

The transmission of two consecutive pulses of the same polarity.

CLOCK THRESHOLD

The differential voltage measured between pins 4 and 5, required to drive the internal fullwave rectifier.

DATA THRESHOLD

The differential voltage measured between pins 4 and 5, required to trip logic threshold detector.

DIFFERENTIAL OUTPUT VOLTAGE

The difference in voltage of the two outputs with a binary one output of either polarity.

ALBO DIODE RESISTANCE

Small signal resistance of ALBO diode measured between pins 1 and 6. The ALBO diode is a diode connected transistor whose current-resistance relationship is $R_D = 26/I_O$ where R_D = ALBO diode resistance and I_O = ALBO diode current in mA.

DELAY CIRCUIT RESISTANCE

Resistance seen at pins 11 and 12.

LINE BUILD OUT

The attenuation that must be added to the output of a short line to increase the line attenuation to 31dB.

MAXIMUM DENSITY

An input signal pattern consisting of all ones.

MINIMUM DENSITY

An input signal pattern consisting of two ones followed by 14 zeros.

OUTPUT PULSE RISE (FALL) TIME

Rise (Fall) time of regenerated pulse. Measured from the 10-90% points.

OUTPUT PULSE WIDTH DIFFERENTIAL

In a T1 carrier system a typical pulse width is 324nsec. The pulse width differential is the difference in pulse width of the two outputs.

PREAMPLIFIER BANDWIDTH

3dB bandwidth of preamplifier circuit.

EQUALIZING NETWORK

A network which compensates for the amplitude and phase response of the cable over the operating bandwidth.

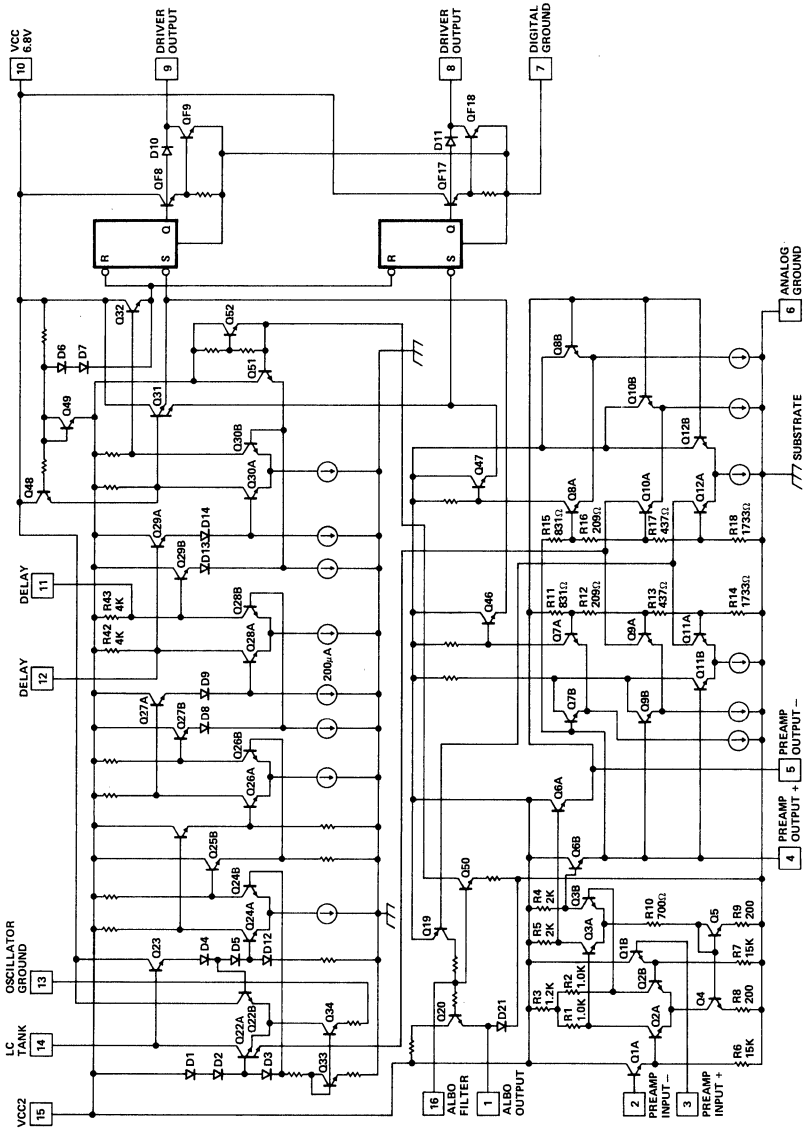
ELECTRICAL CHARACTERISTICS at V_{CC1} = 4.4V, V_{CC2} = 6.8V, −40° C ≤ T_A ≤ +85° C unless otherwise noted. $V_{pin\ 6}$ = $V_{pin\ 7}$ = $V_{pin\ 13}$ = GND.

		PARAMETER	SYMBOL	CONDITIONS	RPT-81 MIN	RPT-81 TYP	RPT-81 MAX	RPT-82 MIN	RPT-82 TYP	RPT-82 MAX	UNITS
SUPPLY	1.	Power Supply Voltage	V_{CC1}	Power Supply Range over which device will function	4.3	4.4	4.7	4.1	4.4	4.7	V
	2.	Power Supply Voltage	V_{CC2}	Power Supply Range over wich device will function	5.0	6.8	7.25	5.0	6.8	7.5	V
	3.	Supply Current	I_{CC1}	T_A = 25° C, Note 1	—	8.5	—	—	8.5	—	mA
	4.	Supply Current	I_{CC2}	T_A = 25° C, Note 1	—	2.5	—	—	2.5	—	mA
	5.	Total Supply Current	$I_{CC1} + I_{CC2}$	T_A = 25° C, Note 1	6.0	11.0	13	6.0	11.0	13	mA
PREAMPLIFIER	6.	Preamplifier Open Loop Gain $\frac{\Delta V_{pin\ 5}}{\Delta V_{pin\ 2}}$	A_0	Measure $\Delta V_{pin\ 2}$ necessary to change pins from 1.8V to 3.3V	44	48	52	44	48	52	dB
	7.	Preamplifier Bandwidth	B_w	3dB Points	—	5	—	—	7	—	MHz
	8.	Preamplifier Input Impedance	Z_{IN}	Shunted by 2pF	—	600	—	—	600	—	kΩ
	9.	Preamplifier Input Offset Voltage	V_{OS}	Note 1, $V_{pin\ 2}$-$V_{pin\ 3}$	—	1	15	—	1	15	mV
	10.	Preamplifier Output Impedance	Z_{OUT}		—	80	—	—	80	—	Ω
	11.	Preamplifier Output High Voltage	V_{OHA}	T_A = 25° C, $V_{pin\ 4}$, $V_{pin\ 2}$ = 2.5V, $V_{pin\ 3}$ = 2.7V	3.25	3.45	3.75	3.4	3.5	3.75	V
	12.	Preamplifier Output Low Voltage	V_{OHL}	T_A = 25° C, $V_{pin\ 4}$, $V_{pin\ 2}$ = 2.5V, $V_{pin\ 3}$ = 2.3V	1.25	1.4	1.55	1.2	1.4	1.5	V
	13.	Preamplifier Input Bias Current	I_B	$I_{pin\ 2}$ or $I_{pin\ 3}$, Note 1	—	1.0	4	—	1.0	4	μA
	14.	Preamplifier Input Offset Current	I_{OS}	$I_{pin\ 2}$-$I_{pin\ 3}$, Note 1	—	0.05	2	—	0.05	2	μA
OUTPUT DRIVE	15.	Output Voltage Swing	V_{OP}	$V_{pin\ 8\ High}$-$V_{pin\ 8\ Low}$, $V_{pin\ 9\ High}$-$V_{pin\ 9\ Low}$	—	6.0	—	—	6.0	—	V
	16.	Low Level Output Voltage	V_{OL}	T_A = 25° C, I_{LOAD} = 15mA, Note 2	0.65	0.8	0.95	0.65	0.8	0.95	V
	17.	Differential Output Voltage (Low Level)	V_{OLD}	T_A = 25° C, I_{LOAD} = 15mA, Note 2	—	0.02	0.15	—	0.02	0.15	V
	18.	High Level Output Leakage Current	I_{OH}	$V_{pin\ 14}$ = 4.9V, Note 1, $V_{pin\ 8}$ = $V_{pin\ 9}$ = 20V, T_A = 25° C	—	0.05	50	—	0.05	50	μA
	19.	Output Pulse Rise Time	T_{os}	AC Test Circuit	—	30	—	—	30	—	ns
	20.	Output Pulse Fall Time	T_{of}	AC Test Circuit	—	10	—	—	10	—	ns
	21.	Output Pulse Width	P_w	AC Test Circuit	—	324	—	—	324	—	ns
	22.	Pulse Width Differential	P_{wD}	AC Test Circuit	—	3	—	—	3	—	ns
	23.	Bipolar Violations at Maximum Density	BV_1 MAX	Repeater Test Circuit Line Atten. = 6-36dB	—	0	—	—	0	—	—
	24.	Bipolar Violations with Quasi-Random Input Pattern	BV_R MAX	Repeater Test Circuit Line Atten. = 6-36dB	—	0	—	—	0	—	—
CLOCK CIRCUIT	25.	Tank Emitter Follower Base Current	I_{TB}	$I_{pin\ 14}$, Note 1, $V_{pin\ 14}$ = 4.9V	—	4	15	—	4	15	μA
	26.	Tank Input Impedance	Z_{INT}	Measured from pin 14 to pin 15	—	300	—	—	300	—	kΩ
	27.	Oscillator Bias Current	I_{OSC}	Note 1, $V_{pin\ 14}$ = 3.9V (I_{OSC}-I_{TB})	10	30	50	10	30	50	μA
	28.	Oscillator Injection Current	I_{INJ}	Set $V_{pin\ 4}$-$V_{pin\ 5}$ = ±1.4V, $V_{pin\ 14}$ = 3.9V (I_{INJ}-I_{OSC})	75	120	160	75	120	160	μA
	29.	Delay Circuit Resistor	R_d	Measured from pin 11 or pin 12 to pin 15, T_A = 25° C	3.2	4.0	4.8	3.2	4.0	4.8	kΩ
MISCELLANEOUS	30.	ALBO Threshold	V_{TA}	Differential voltage, measured between pins 4 and 5, required to trip Peak Detector. T_A = 25° C	1.35	1.5	1.65	1.35	1.5	1.65	V
	31.	Clock Threshold	V_{TC}	Differential voltage, measured between pins 4 and 5, required to drive Fullwave Rectifier. T_A = 25° C	0.85	1.0	1.2	0.9	1.08	1.25	V
	32.	Logic Threshold	V_{TL}	Differential voltage, measured between pins 4 and 5, required to trip Logic Threshold. T_A = 25° C	0.65	0.75	0.85	0.65	0.75	0.85	V
	33.	Clock Threshold as % of ALBO Voltage	V_{TC}	T_A = 25° C	62	66	70	68	72	76	%
	34.	Logic Threshold as % of ALBO Voltage	V_{TL}	T_A = 25° C	47	50	53	46	49	52	%
	35.	ALBO ON Voltage	V_{O16}	Measured at pin 16, $\lvert V_{p4}$-$V_{p5}\rvert$ = ALBO Threshold	1.0	1.7	2.5	1.0	1.7	2.5	V
	36.	ALBO OFF Voltage	V_{F16}	Measured at pin 16 and pin 1 Note 1, T_A = 25° C	—	—	75	—	—	75	mV
	37.	Minimum ALBO Diode Resistance	R_D Min		—	8	—	—	8	—	Ω
	38.	Maximum ALBO Diode Resistance	R_D Max		—	30	—	—	30	—	kΩ

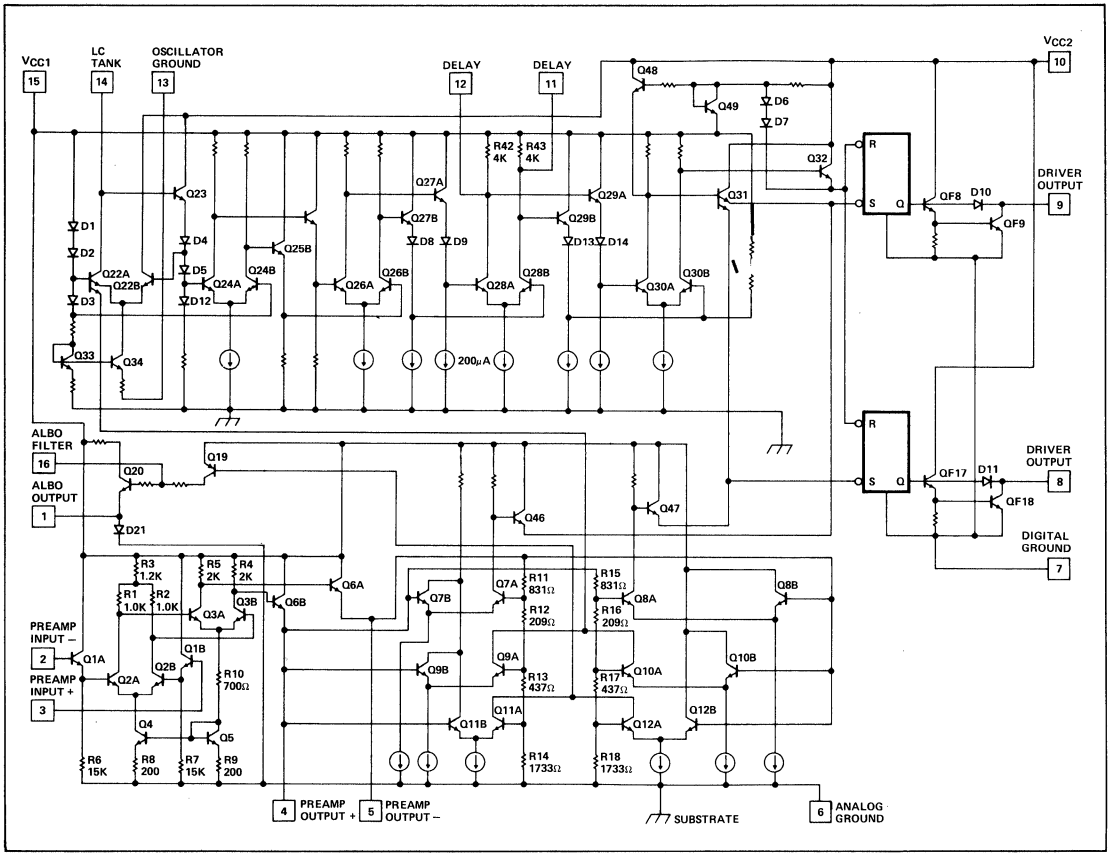
NOTES:

1. $V_{pin\ 2}$ = 2.5V, adjust $V_{pin\ 3}$ until $V_{pin\ 4}$ = $V_{pin\ 5}$.
2. A dynamic test, pin 2 = 2.5V, pin 3 pulsed at 100Hz rate, pin 14 pulsed at 200Hz rate.

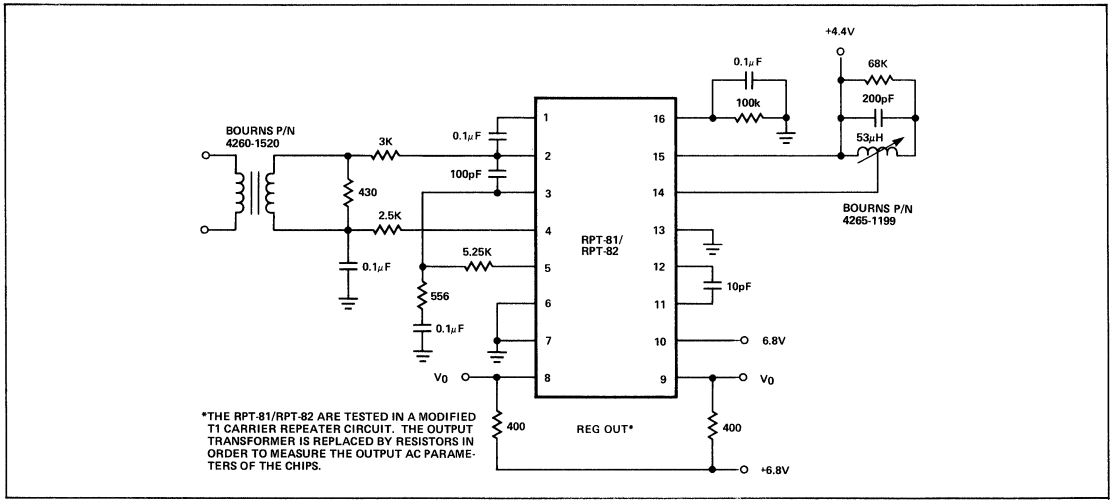
RPT-81 SIMPLIFIED SCHEMATIC



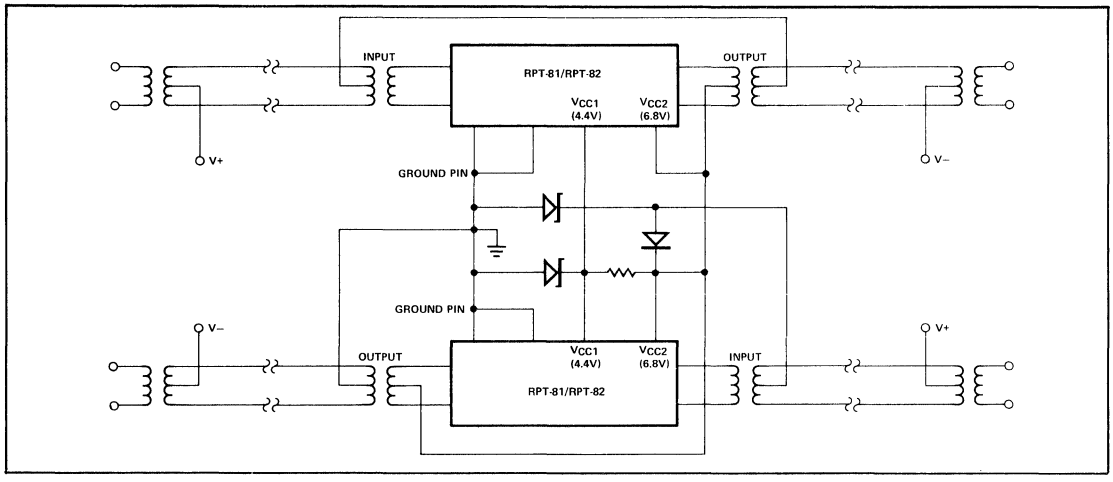
RPT-82 SIMPLIFIED SCHEMATIC



TEST CIRCUIT



TYPICAL REPEATER POWERING ARRANGEMENT



REPEATER CURRENT REQUIREMENTS

For comparison to CCIT or ATT specifications it is convenient to estimate total repeater current requirements. Repeater current is typically calculated in the following manner:

i. Each of the two zeners used as regulators have idle current requirements of approximately 1.0mA (2mA).

ii. Total no-signal supply current, from the electrical characteristics table, is 13.0mA (guaranteed maximum) for each side.

iii. To compute worst case (all ones) output current assumes a 6.0 volt pulse across a 400Ω transformer primary (50% d.f.) for the U.S. or a 6.0 volt pulse across a 480Ω transformer primary (50% d.f.) for CCITT. These currents compute to 15mA and 12.5mA respectively (for both sides).

iv. ALBO diode current is 26mV divided by the minimum required ALBO resistance (approximately 8Ω). Typically worst case is 6.5mA (for both sides).

Adding the currents calculated into the currents calculated in ii, iii, and iv gives the following typical repeater current requirements:

i. U.S. ..... 49.5mA (worst case all ones output)

ii. Europe ..... 47.0mA (worst case all ones output)

APPLICATIONS INFORMATION

In a typical repeater system extensive external circuitry is required. The regulator network, assembled from zener diodes and resistors is used to power the integrated circuit. Normally one common circuit is provided for the two ICs operating in opposite directions. Input and output transformers are used to couple the transmission lines. The input one-to-one transformer has secondary loaded with a line matching resistor to avoid reflections on the input lines. An attenuator network may be installed after this input transformer as a fixed line-build-out pad. Feedback resistors are used to set the DC bias of the circuit. Additionally the bias network is connected to a fixed resistive voltage divider to tie the biasing network to a fixed potential. The ALBO network consists of a series impedance and a shunt impedance where the shunt impedance is AC terminated to the ALBO diode.

The shunt impedance has both resistive and reactive components to assist in line equalization. The equalizing network is basically a series tuned circuit in one of the input legs of the preamplifier whose function is to give the preamplifier a frequency response which corrects for the amplitude and phase response of the input line. The design of the equalizing network is very important to the system performance. A lag capacitor across the preamplifier input stabilizes the preamplifier. The output transformer normally incorporates a fault locating winding which is used, in conjunction with appropriate filters, to detect defective repeaters. The input transformer has a center tapped primary to allow for a simplex powering system.

The RPT-81/RPT-82 oscillator allows two modes of operation controllable by pin 13 (Oscillator Control). When grounded the oscillator is in a free-running mode. With pin 13 open the oscillator works in a pulsed, ringing mode. In both cases the external L-C tank circuit determines the oscillation frequency.

The external delay capacitor (across pins 11 and 12) provides 90° of phase shift through the clock amplifier. For best performance a 10pF silver mica capacitor is suggested.

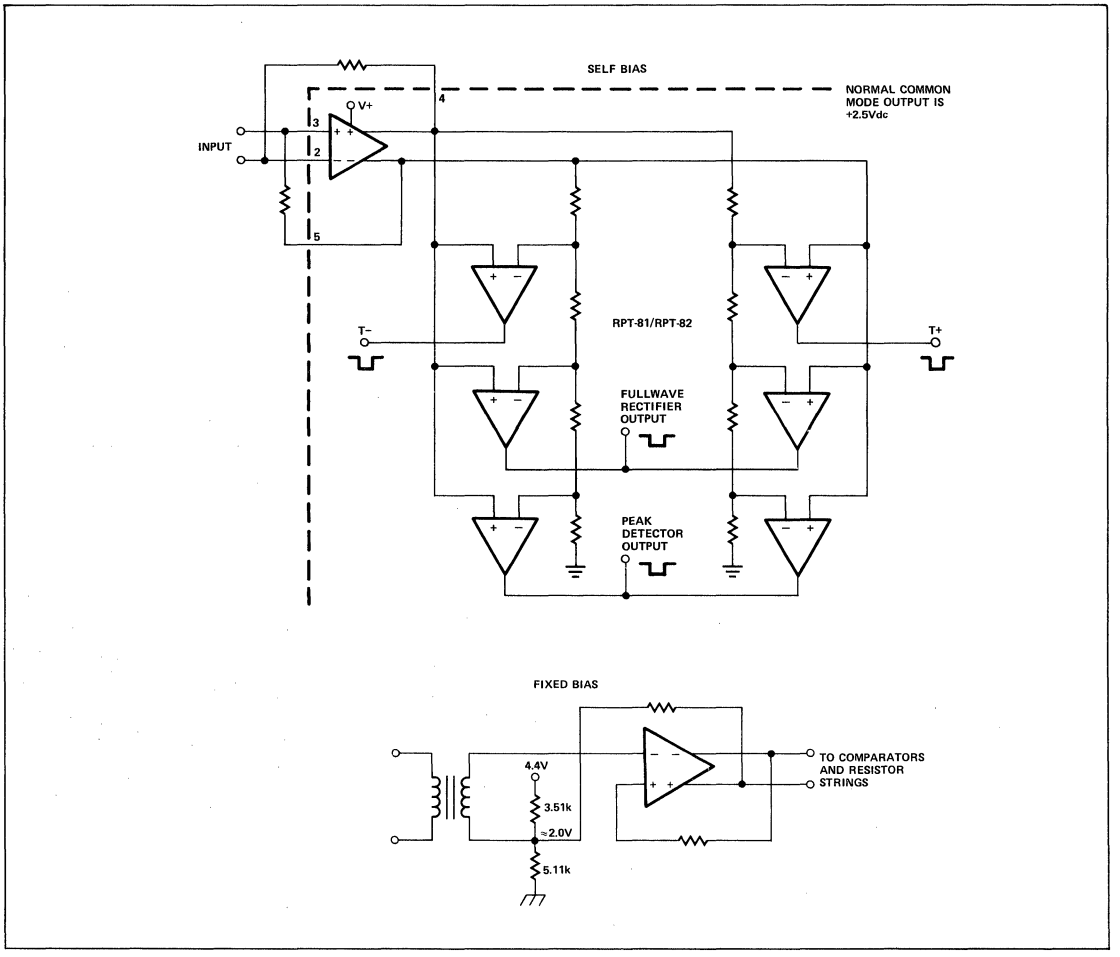
Oscillator tank circuit Q directly affects the clock regeneration circuitry. The effective Q of the L-C oscillator tank circuit must be high enough that ringing will be maintained with minimum pulse densities. The resonant Q cannot, however, be arbitrarily large, or operating temperature changes and component aging will cause resonant frequency shifts. The RPT-81/RPT-82 will operate with Q's as low as 75.

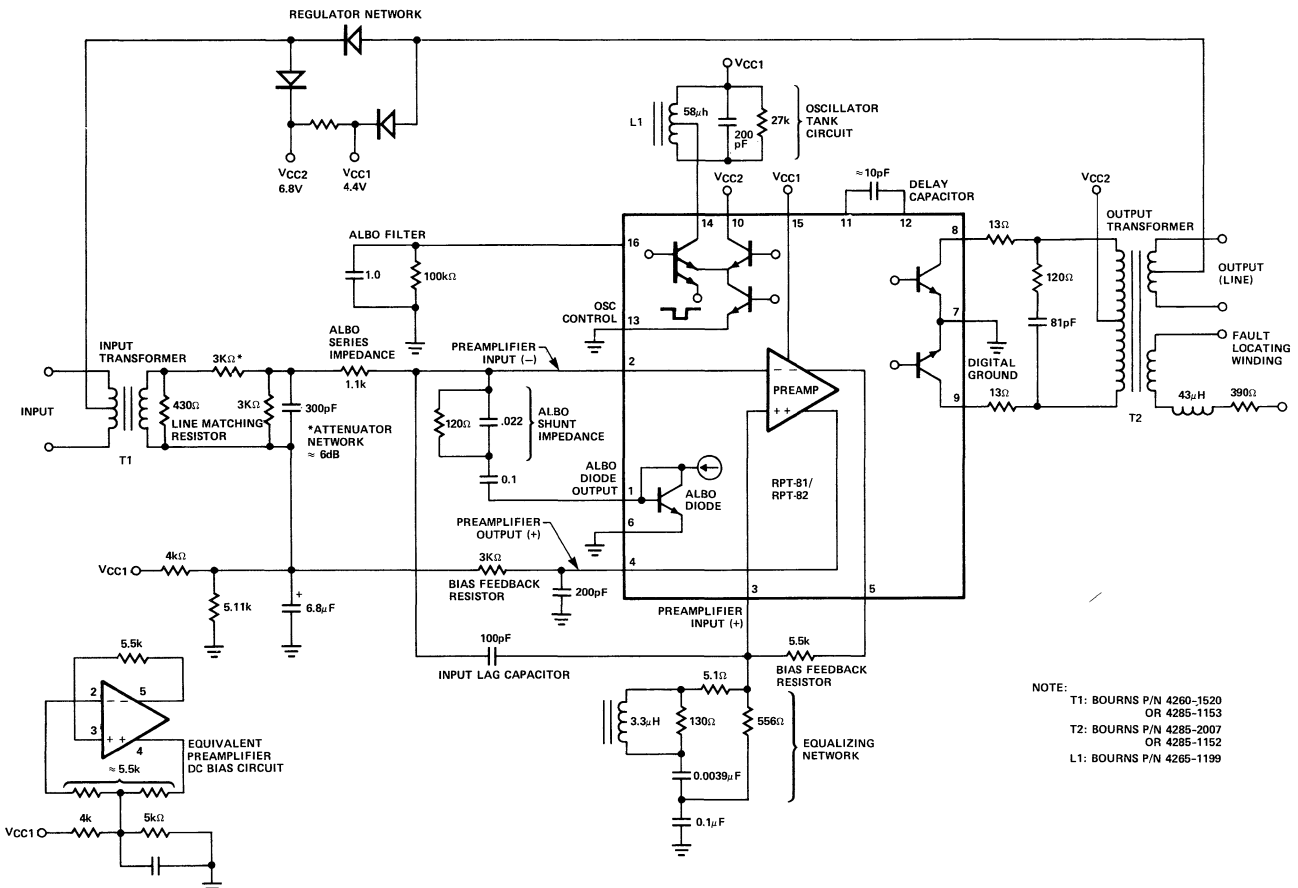
In order to provide noise rejection, the analog and digital grounds have been isolated on chip. Low noise/distortion operation can be enhanced if the high power output leads and external circuitry are physically located as far as possible from the preamplifier inputs. Supply bypassing of V_{CC1} and V_{CC2} close to device pins is encouraged.

PREAMPLIFIER BIASING SCHEMES

Both inverting and non-inverting outputs of the RPT-81/ RPT-82 preamplifier are available so that either self-biasing or fixed-biasing techniques may be employed. The effect of the DC biasing is to set the thresholds of the detectors. All the thresholds move together, the relative threshold which is defined in terms of a percentage of the peak detector threshold is determined by the resistor string. In a self-biased scheme the non-inverting output is returned to the inverting input and the inverting output is returned to the non-inverting input. In this manner the input leads are biased to the normally occurring common mode output voltage. The best noise performance is obtained with this system but some problems are encountered at low temperatures where the circuit tends to turn itself off. In a fixed biased scheme one of the inputs is biased to a fixed DC level while the other input is biased to the opposite output in the same manner as with self bias. Note that with fixed bias a differential output offset will be caused if the fixed bias is not matched to the normally occuring output level. If the fixed level is very close to the normally occuring output level then there is an improvement in performance at low temperature.

PREAMPLIFIER BIASING SCHEMES




REGULATOR NETWORK
VCC2 6.8V
VCC1 4.4V
VCC1
L1
58μh
27k
200 pF
OSCILLATOR TANK CIRCUIT
VCC2
VCC1
≈10pF
DELAY CAPACITOR
VCC2
OUTPUT TRANSFORMER
ALBO FILTER
1.0
100kΩ
OSC CONTROL
13
16
14
10
15
11
12
8
13Ω
120Ω
81pF
7
9
DIGITAL GROUND
OUTPUT (LINE)
FAULT LOCATING WINDING
43μH
390Ω
T2
INPUT TRANSFORMER
3KΩ*
ALBO SERIES IMPEDANCE
1.1k
PREAMPLIFIER INPUT (–)
2
PREAMP
INPUT
430Ω
3KΩ
LINE MATCHING RESISTOR
300pF
*ATTENUATOR NETWORK ≈ 6dB
T1
120Ω
.022
ALBO SHUNT IMPEDANCE
0.1
ALBO DIODE OUTPUT
1
ALBO DIODE
RPT-81/ RPT-82
PREAMPLIFIER OUTPUT (+)
6
4
VCC1
4kΩ
3KΩ
BIAS FEEDBACK RESISTOR
200pF
5.11k
6.8μF
3
5
PREAMPLIFIER INPUT (+)
100pF
INPUT LAG CAPACITOR
5.5k
BIAS FEEDBACK RESISTOR
5.5k
2
5
3
4
EQUIVALENT PREAMPLIFIER DC BIAS CIRCUIT
≈ 5.5k
5.1Ω
3.3μH
130Ω
556Ω
EQUALIZING NETWORK
0.0039μF
0.1μF
VCC1
4k
5kΩ
NOTE:
T1: BOURNS P/N 4260-1520 OR 4285-1153
T2: BOURNS P/N 4285-2007 OR 4285-1152
L1: BOURNS P/N 4265-1199

SMP-81

TELECOMMUNICATIONS SAMPLE AND HOLD AMPLIFIER

FEATURES

- **Meets System Performance Requirements in Multi-Channel CODECs**
- **Trimmed for Minimum Zero Scale Error 0.6mV**
- **Low Droop Rate Over Temperature 0.1μV/μs**
- **Low Aperture Time 50ns**
- **Fast Acquisition Time 10V Step to 0.1% 3.5μs**
- **High Slew Rate 10V/μs**
- **High Sample Current/Hold Current Ratio ..... 1.7×10^8**
- **DTL, TTL & CMOS Compatible Logic Input**
- **HA-2425, DATEL SHM-IC-1, and AD-583 Socket Compatible***
- **Low Dissipation**
- **Low Cost**
- **Feedthrough Attenuation Ratio 96dB**

GENERAL DESCRIPTION

The SMP-81 precision sample and hold amplifier provides the high accuracy, low droop rate and fast acquisition ideally required for PCM encoders. The SMP-81 is a non-inverting unity gain circuit consisting of two buffer amplifiers of very high input impedance connected by a diode bridge switch.

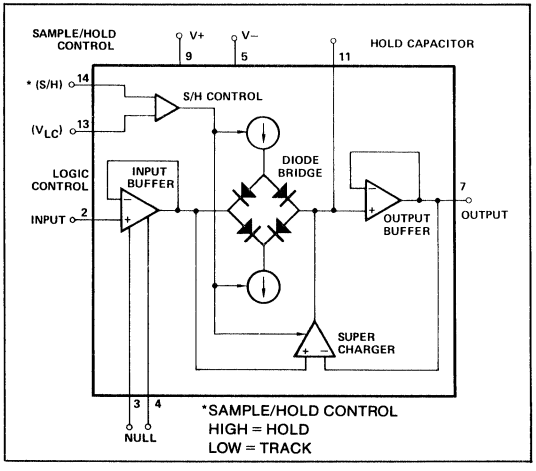
HIGH ACCURACY AND LOW DROOP RATE

The high input impedance and low droop rate of the SMP-81 are achieved by PMI's ion implant super beta process. The high input impedance permits high impedance source applications without degrading accuracy, and low droop rate. Other features of the SMP-81 include high accuracy, 0.6mV of combined offset voltage and step transfer error, and very low feedthrough. A diode bridge switch design allows minimum charge transfer step. On-chip Zener-Zap trimming eliminates nulling for most applications.

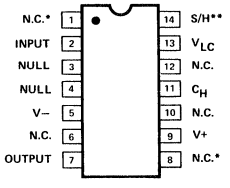
FAST ACQUISITION

A unique super charger or transconductance amplifier provides up to 50mA charging current to the hold capacitor. As a result, smooth charging of the hold capacitor is achieved with minimum noise. The super charger, in conjunction with the high slewing rate input and output buffer amplifiers, permits fast acquisition operation. The adjustable logic input threshold makes the SMP-81 compatible to all logic families.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS & ORDERING INFORMATION



14 PIN DIP - HERMETIC
(Y SUFFIX)

V_{ZS} (mV)	
1.6	SMP-81EY
3.5	SMP-81FY

*Pins 1 and 8 are not internally connected. In unity gain applications, the SMP-81 can replace HA-2425, SHM-IC-1 and AD-583 directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ minus V−) 36V
Power Dissipation 500mW
Input Voltage ..... Equal to Supply Voltage
Logic and Logic Control Voltage .. Equal to Supply Voltage
Output Short Circuit Duration ..... Indefinite
Hold Capacitor Short Circuit Duration 60sec
Operating Temperature Range ..... −25°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering 60 sec) ..... 300°C

ELECTRICAL CHARACTERISTICS at $V_S \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $-25°C \leq T_A \leq +85°C$, device fully warmed up, unless otherwise noted.

			SMP-81E			SMP-81F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Zero Scale Error (Hold Mode)	V_{ZS}	$V_{IN} = 0V_{LOG} = 3.5V$ (500μsec after Hold Command)	—	0.6	1.6	—	0.9	3.5	mV
Input Bias Current	I_B	$V_{IN} = 0$	—	105	225	—	120	450	nA
Leakage (Droop) Current	I_{DR}	Device Warmed Up	—	0.5	10	—	0.5	20	nA
Droop Rate	dVCH/dt		—	0.1	2.0	—	0.1	4.0	mV/msec
Input Resistance	R_{IN}		$3x10^{10}$	$6x10^{10}$	—	$1.5x10^{10}$	$5x10^{10}$	—	Ω
Voltage Gain	A_V	Sample Mode $V_{IN} = \pm 10V$ $R_L = 5K\Omega$	0.99960	0.99980	—	0.99955	0.99978	—	V/V
	A_V	or $V_{IN} = \pm 5V$ $R_L = 2.5K\Omega$	0.99960	0.99980	—	—	0.99978	—	V/V
Acquisition Time		10V step to within 10mV of final value (0.1%)	—	3.5	—	—	3.5	—	μs
Aperture Time	t_a		—	50	—	—	50	—	nsec
Charge Transfer	Qt	$V_{IN} = 0V_{LOG} = 3.5V$	—	5	—	—	5	—	pC
Slew Rate	SR	$V_{IN} = \pm 10V$ $R_L = 2.5K\Omega$	—	10	—	—	10	—	V/μs
Hold Capacitor Charging Current	I_{CH}	$V_{IN} - V_{OUT} \geq \pm 3$ volts	30	50	—	20	50	—	mA
Feedthrough Attenuation Ratio		Input $-20V_{p-p}$ 1kHz (See note)	86	96	—	80	90	—	dB
Full Power Bandwidth	F_p	$\pm 10V_{p-p}$ (Dissipation Limited)	—	100	—	—	100	—	kHz
Input Voltage Range and/or		$R_L = 2.5K\Omega$	±10	±11.5	—	±10	±11.5	—	V
Output Voltage Swing		$R_L = 2.5K\Omega$	±10	±11.5	—	±10	±11.5	—	V
Output Resistance	R_o		—	0.15	—	—	0.15	—	Ω
Power Supply Rejection Ratio	PSRR	Sample Mode $V_S = \pm 9V$ to $\pm 18V$	80	90	—	75	90	—	dB
Power Consumption (DC)	P_D	Sample Mode $V_{IN} = 0$	—	160	180	—	170	210	mW
Logic Control Input Current	I_{LC}		−6	−3	—	−9	−3	—	μA
Logic Input Current	$I_{S/H}$	Sample Mode $V_{S/H} = 0.6V$	—	−15	−45	—	−15	−45	μA
	$I_{S/H}$	Hold Mode $V_{S/H} = 5.0V$	—	0.6	—	—	0.6	—	nA
Differential Logic Threshold			0.8	1.3	2.0	0.8	1.3	2.0	V
Hold Mode Settling Time	t_{HM}	5V step to within 1mV of final value	—	1.5	—	—	1.5	—	μs

Note: Guaranteed by design.

DEFINITION OF TERMS

ZERO SCALE ERROR

The magnitude of the output voltage when the circuit is switched from sample to hold mode while holding the input at zero volts. Zero Scale Error V_{ZS} is the algebraic sum of the offset voltage and the charge transfer step voltage. V_{ZS} can be adjusted to zero (see Zero Scale Error null adjustment).

INPUT BIAS CURRENT

The current into the input terminal with input voltage held at zero volts.

LEAKAGE (DROOP) CURRENT

The current which flows out of holding capacitor C_H while the circuit is operating in the hold mode. In general droop current I_{DR} is defined positive when its direction is **into** the C_H pin.

DROOP RATE

Droop rate dV_{CH}/dt is the rate of change of output voltage while the circuit is operated in the hold mode dV_{CH}/dt is a direct function of droop current I_{DR} and related by the equation

$$\frac{dV_{CH}}{dt} = \frac{I_{DR}}{C_H} \times 10^3$$

where dV_{CH}/dt is expressed in μV/ms with I_{DR} in microamperes and C_H in microfarads.

INPUT RESISTANCE

The ratio of the AC change in the input current as a result of the change in the input voltage.

VOLTAGE GAIN

The ratio of the output voltage to the input voltage with the circuit operating in the sample mode.

ACQUISITION TIME

The minimum time for the output voltage to begin tracking the input voltage, to within a specified error band, after the inception of the sample command. By convention, acquisition time is defined for sampling of a DC level. For instance, a circuit which is "holding" a 10V output signal, and operating with zero input volts, is switched to the sample mode. The acquisition time is then the time required for the output to decrease to within a ±10mV band about ground potential.

APERTURE TIME

The time between the inception of the hold command and the time the circuit output ceases tracking the input signal. When the holding capacitor charging current is less than 0.3ma the aperture time is nominally 50ns. The aperture time is a function of the holding capacitor charging current I_{CH}. The charging current is in turn a function of the rate of change of the input signal voltage. This relationship holds true up to a maximum of 50mA which is the maximum current available from the SMP-81 to charge holding capacitor C_H. Charging current can be calculated from the rate of change of the input analog and the size of C_H by the equation:

$$I_{CH} = C\frac{dv}{dt} \quad (I_{CH} = 50\text{mA Max.})$$

GAIN-ERROR

Voltage difference between input and output voltage minus the output voltage measured with input at zero volts.

CIRCUIT IN SAMPLE MODE

HOLD STEP

Magnitude of step caused in the output voltage by switching the circuit from sample mode to hold mode.

CHARGE TRANSFER

The amount of charge transferred to the holding capacitor due to the action of the switch. Charge is transferred to C_H when the circuit is switched to the hold mode. Charge transfer causes a change in output voltage ΔV_{ZS} as defined by the equation:

$$\Delta V_{ZS}(V) = \frac{Q_t\,(pC)}{C_H\,(pF)}$$

Note that for $Q_t = 5pC$ and $C_H = 5000pF$ offset error = 1mV. The SMP-81 has been factory nulled for $C_H = 5000pF$. For other values of C_H, the zero scale shift can be calculated from the equation:

$$\Delta V_{ZS}(V) = \frac{Q_t}{C_H} - 1mV$$

SLEW RATE

The maximum possible rate of change of the output voltage when supplying the rated output. For a sample and hold circuit, slew rate must be defined with a specified value of holding capacitor C_H. For the SMP-81, slew rate can either be measured by operating the circuit in the sample mode and applying a step function to the input, or by applying an input voltage which differs from the output voltage, with the circuit in the hold mode, then switching to the sample mode and observing the rate of change of the output voltage.

HOLD CAPACITOR CHARGING CURRENT

The current I_{CH} which charges, or discharges, the capacitor while the circuit is in the sample mode.

SAMPLE/HOLD CURRENT RATIO

The ratio of the peak charging current available to the droop current.

FEEDTHROUGH ATTENUATION RATIO

The change of voltage applied to the input as a ratio of the change of voltage observed at the output, caused by the input disturbance, while the circuit is in the hold mode.

FULL POWER BANDWIDTH

The maximum frequency at which rated output voltage E_{or} can be supplied without significant distortion. Full power bandwidth F_p is related to slew rate SR by the following equation:

$$F_p = \frac{SR}{2\pi E_{or}}$$

Using this equation, F_p of 160kHz can be computed. This is applicable only for pulsed conditions. Power dissipation limits F_p to 100kHz for C.W. operation.

OUTPUT RESISTANCE

An AC change in output voltage as a result of an AC change in load current.

POWER SUPPLY REJECTION RATIO

The change in output voltage for a change in power supply voltage when the circuit is maintained in the sample mode. The best power supply rejection ratio PSRR is obtained with the power supply voltage changing at a very low rate (DC). For essentially DC conditions PSRR for the hold mode of operation is essentially the same as the PSRR for the sample mode. PSRR is degraded as the frequency of the disturbance increases. PSRR for both sample and hold modes is shown graphically as a function of frequency.

CHANGE IN HOLD STEP

Actual hold step less the hold step measured after sampling V = 0. A change in hold step has two components: the first is a function of input voltage; the second is a function of the rise time of the S/H voltage. Note that rise time of S/H voltage also effects ZERO-SCALE-ERROR.

TOTAL ERROR

The algebraic sum of the following factors:

i. ZERO-SCALE-ERROR

ii. Gain Error

iii. Hold Step Change versus $\frac{dV_{(S/H)}}{dt}$

vi. Hold Step Change versus V_{in}

HOLD MODE SETTLING TIME

The time for all transients to settle to within a specified error band measured from the inception of the hold command.

HOLD CAPACITOR RECOMMENDATIONS

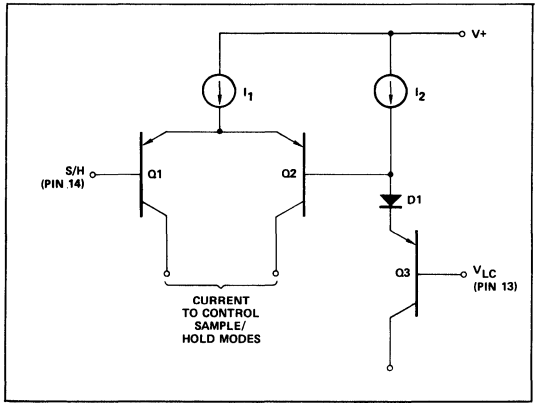
The hold capacitor (C_H) acts as a memory element and also as a compensating capacitor for the sample and hold amplifier. For stable operation, a minimum value of 2000pF is recommended, with no limit set for the maximum value. The SMP-81 is internally trimmed for $C_H = 5000pF$. Other values of C_H will cause a zero scale shift, which can be calculated from the following equation: a C_H of 5000pF has been empirically determined to be an optimum value for 8-channel shared CODEC operation.

$$\Delta V_{ZS}\,(mV) = \frac{5\,(pC) \times 10^3}{C_H\,(pF)} - 1$$

The hold capacitor should have very high insulation resistance and low dielectric absorption. For temperatures below 85°C, polystyrene capacitors are recommended, while teflon capacitors are recommended for higher temperature applications.

SMP-81 LOGIC CONTROL

The sample/hold mode control of the SMP-81 incorporates a unique logic input circuit, which enables direct interface to all popular logic families and provides maximum noise immunity. As shown in the figure, the mode control is accomplished by steering the current (I_1) through Q1 or Q2, thus providing high speed switching and a predictable logic threshold. For TTL and DTL interface, simply ground V_{LC} (pin 13). For CMOS, HTL and HNIL interface, the appropriate threshold voltage, allowing for 2 diode drops for D1 and V_{BE} of Q3, should be applied to V_{LC}.

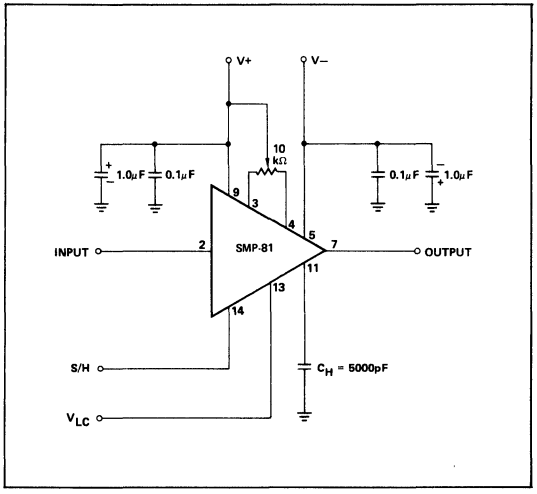


For proper operation, the V_{LC} (logic control) must always be at least 3.5V below the positive supply and 2.0V above the negative supply.

Sample and hold control voltage (S/H) must always be at least 2.8V above the negative supply.

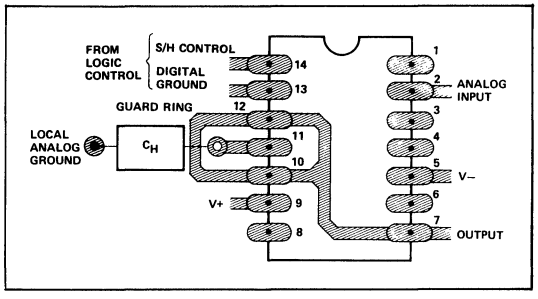
ZERO SCALE ERROR NULL ADJUSTMENT

During the null adjustment, the amplifier should be switched continuously between the "sample" and "hold" mode. The error should be adjusted to read zero when the unit is in the "hold" mode. In this way, both offset voltage errors and charge transfer errors are adjusted to zero.



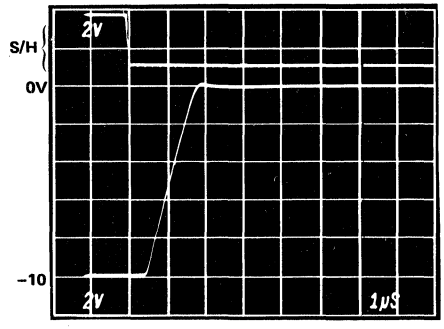
GUARDING AND GROUNDING LAYOUT

The use of a ground plane is strongly recommended to minimize ground path resistances. Separate analog and digital grounds should be used, and it is advisable to keep these two ground systems isolated until they are tied back to the common system ground. Digital currents should not flow back to the system ground through the analog ground path.

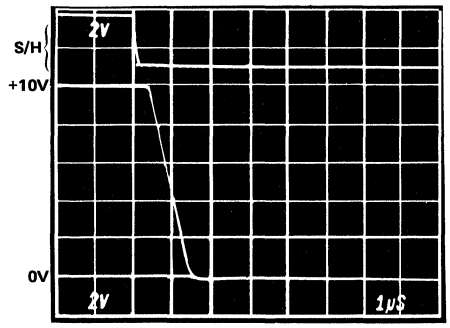


SMP-81 ACQUISITION TIMES

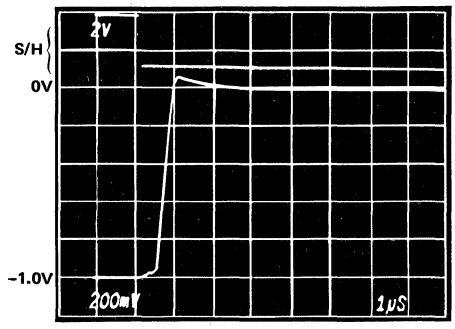
ACQUISITION TIME
– 10V TO 0V



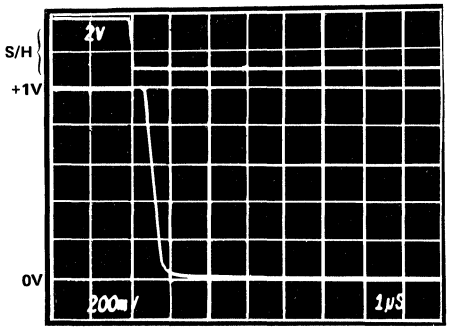
ACQUISITION TIME
+ 10V TO 0V



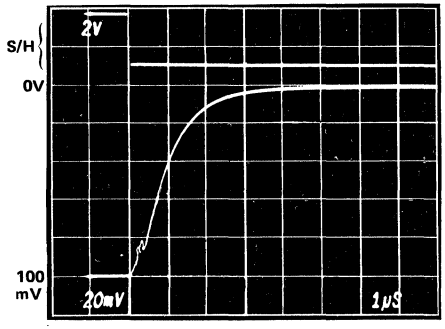
ACQUISITION TIME
– 1.0V TO 0V



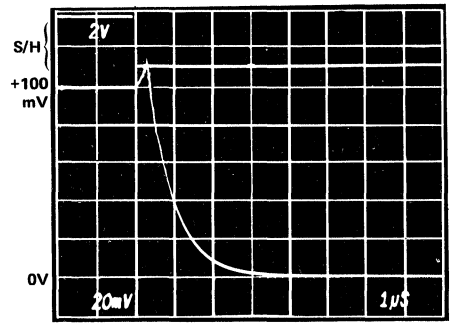
ACQUISITION TIME
+ 1.0V TO 0V

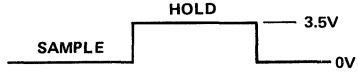


ACQUISITION TIME
– 100mV TO 0V



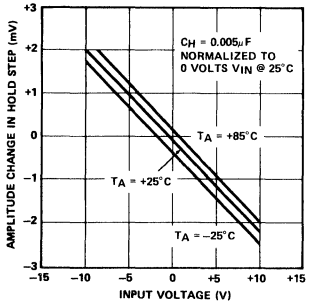
ACQUISITION TIME
+ 100mV TO 0V



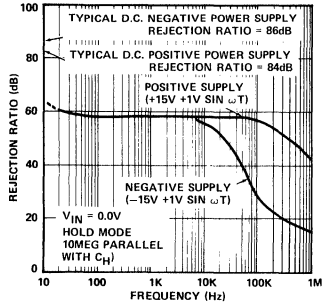


TYPICAL PERFORMANCE CURVES

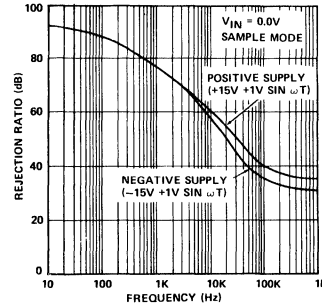
AMPLITUDE CHANGE IN HOLD STEP vs INPUT VOLTAGE



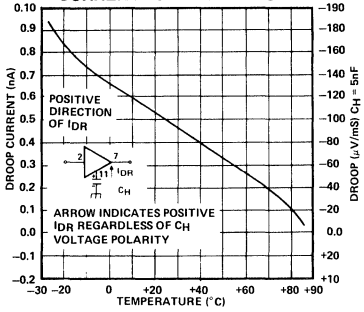
HOLD MODE POWER SUPPLY REJECTION



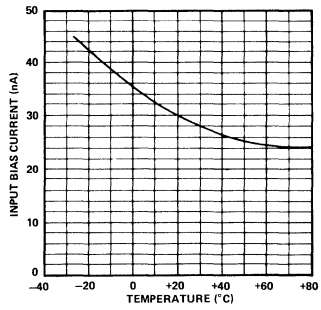
SAMPLE MODE POWER SUPPLY REJECTION



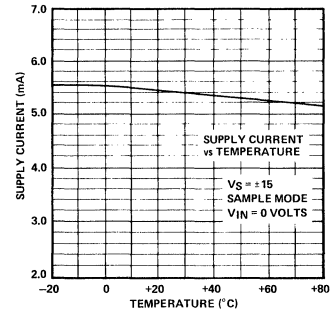
LEAKAGE (DROOP) CURRENT vs TEMPERATURE



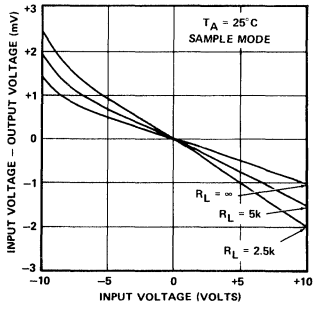
INPUT BIAS CURRENT vs TEMPERATURE



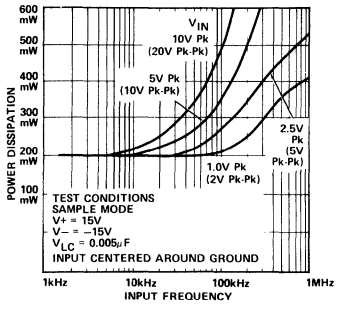
SAMPLE MODE SUPPLY CURRENT vs TEMPERATURE



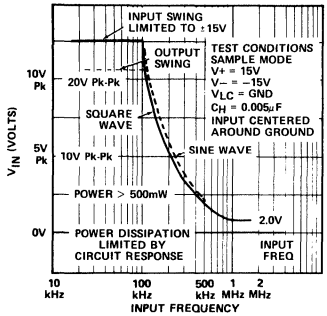
GAIN ERROR



POWER DISSIPATION vs FREQUENCY INPUT = V_p sin ωt

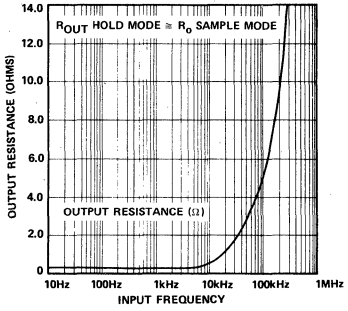


MAXIMUM INPUT SIGNAL AMPLITUDE vs FREQUENCY

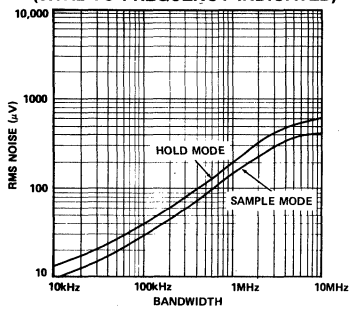


TYPICAL PERFORMANCE CURVES

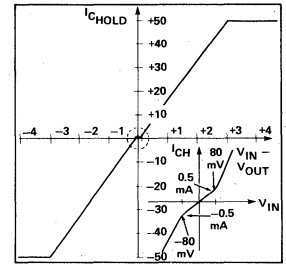
OUTPUT RESISTANCE vs FREQ



OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)

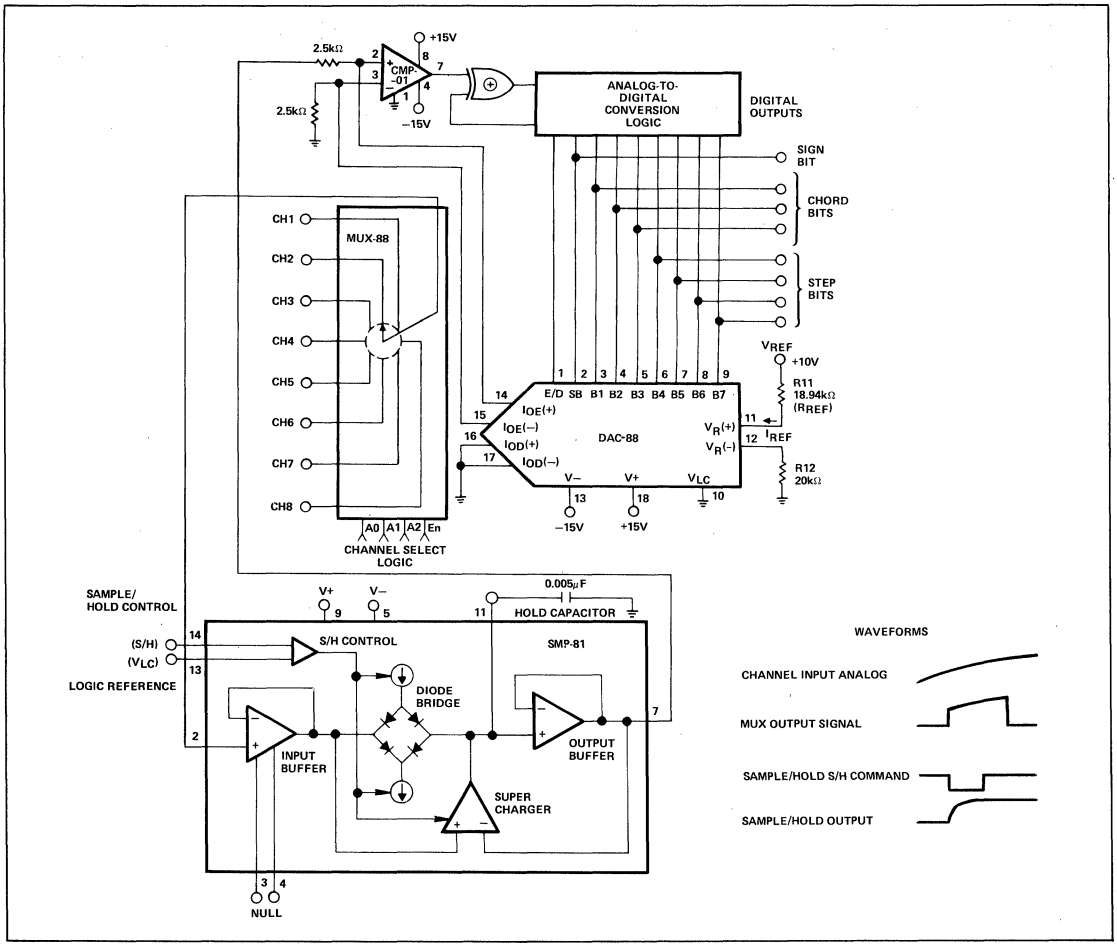


HOLD CAPACITOR CHARGING CURRENT vs INPUT OUTPUT VOLTAGE

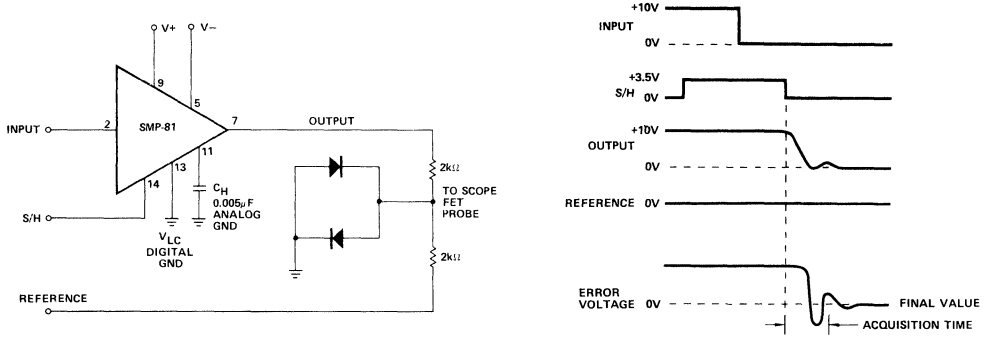


TYPICAL APPLICATION

EIGHT CHANNEL SHARED CODEC PCM ENCODER



ACQUISITION TIME TEST CIRCUIT



DICE

For applicable DICE information see SMP-11 Data Sheet.

SECTION 14

CUSTOM WAFER FAB

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Custom Wafer Fabrication

INTRODUCTION

Since its beginning, PMI has placed emphasis on precision performance and high quality. At PMI, high-reliability business is no peripheral affair; rather it is a fundamental element in the company's growth plan. As a result of PMI's stress on quality and reliability, our integrated circuits have been used in controlling, monitoring and sensing system designs in many military and aerospace programs including Viking, Trident, Cruise Missile, Minuteman, Aerosat, Sparrow Missile, Harm Missile System, Spacelab, Satcom, Voyager, Roland, Exosat, Stinger Missile, DSCS-3, TDRSS, AMRAAN, ARIANE, ISPM, SBS, METRO-2, TIROS-N, IUS, GBU-15, GPS, Intelsat-5, the Delta launch vehicle, Pathfinder Radar, Columbia Space Shuttle and many more.

Contributing to the high-reliability capabilities of PMI devices is the use of proprietary processing techniques including triple passivation. These techniques have made it possible for PMI to develop the world's lowest noise family of IC op-amps (OP-27/37), featured on the cover of the December 20, 1980 issue of Electronic Design Magazine and have improved the radiation resistance characteristics exhibited by many PMI products.

CUSTOM PRODUCTS

There is a marked trend toward increased end-user involvement in the design of integrated circuits. Frequently, an end-user will have the design accomplished by either in-house engineering or by an outside custom design facility. Manufacturing can then be done by an outside facility. The advantages to this system are:

1. The user gets precisely the required part.
2. The mask set is owned by the user.
3. Inherent protection of proprietary designs.
4. The user is not tied to one vendor.
5. Control over design and manufacturing remains with the user.

Additional advantages of dealing with PMI are:

1. Absolute commitment to quality.
2. Technical assistance with mask design.
3. Wide range of available processes.
4. Non-disclosure agreements for particularly market sensitive products.
5. MIL-M-38510 qualified fab area.
6. Nitride passivation available.

SEPARATE STAFF AND FACILITY

PMI's custom wafer fabrication group occupies a completely self-contained facility for servicing its customers. The staff of the facility provides customers with high-quality wafer processing, assurance of a long-term commitment to service-oriented dependable wafer processing, and access to high-performance processes not normally available for custom circuits.

PROCESS TECHNOLOGY

Processes offered by PMI include:

- **Linear Bipolar.** The entire range of linear processing, including FET-input op-amps, is available.
- **Transistor Transistor Logic.** Aluminum and PtSiTiW Schottky processes.
- **I^2L, ISL.** PMI has gained exceptional expertise through processing thousands of high-quality wafers.
- **Emitter Coupled Logic.** PtSiTiW washed emitter process.
- **Complementary Metal-Oxide-Semiconductors.** PMI's selective-oxide-isolated, silicon-gate CMOS process can provide gate delays under 10nsec.

All of the processes mentioned above can be enhanced with ion implanted resistors and bases, dual layer metalization, nitride passivation, and thin film resistors. PMI's processes are compatible with the design rules followed by leading independent custom IC design houses whose names can be furnished on request.

Continuous investigation and implementation of the latest wafer processing technologies has helped PMI maintain a position at the leading edge of integrated circuit development.

PROCESS CAPABILITY

PMI's masking operation uses negative resist, contact printing. Emulsion working plates are either printed from the customer's submasters or chrome working plates are obtained from mask vendors.

PMI uses low temperature techniques for its epitaxial layer deposition to minimize crystal defects. Other capabilities include Antimony buried layer, Boron diffusion (100 to 300 ohms/sq.), ion implanted resistors and bases (B_{11}), with resistor values from 1000 to 2000 ohms/sq., and ion implanted BiFET and super beta devices on PMI's Extrion DF4 200keV Ion Implanter.

Thin film capabilities include Al, AlSi, and PtSiTiW metalization; silicon and nitride passivation; and CrSi resistors (2kΩ/sq.) with positive TC's of less than 200ppm and matching to 5ppm. An in-house scanning electron microscope (S.E.M.) routinely monitors metalization and other processes.

PROCESS CONTROL

As has been previously mentioned, the PMI custom wafer fabrication facility is qualified to Military MIL-M-38510. This qualification requires that all areas be monitored for particulate levels, all diffusion and evaporation processes are CV plotted for contamination control, and all in-process parameters are recorded and retained by lot numbers. (Oxide thicknesses on actual devices are measured on NANOMETRIC's non-destructive thin-film monitor.)

Electrical evaluation on dropped-in die is recorded and retained using a LOMAC LM-80 System (engineering lots are manually probed). All incoming materials (wafers, chemicals, masks) are checked for compliance to PMI standards.

DESIGN RULES

Design rules and electrical process parameter specifications may be made available for most linear and digital processes run at PMI.

FAB PROCEDURE

PMI will evaluate a customer's mask set to ensure its compatibility with PMI's processing capabilities; a nominal fee is charged for this service. Following the acceptance of PMI's quote to manufacture the desired wafers, prototype runs are begun. Delivery is normally four to six weeks for single-layer metalization, and six to eight weeks for dual-layer metalization devices.

Wafers, both prototype and production lots, are accepted by the customer based on

parametric data obtained from drop-in test dice on the wafers.

After the customer completes evaluation of the prototype-runs, processing adjustments are made, if required, and volume production is initiated. On an ongoing basis, the customer receives consultation on the proper selection of a process for the customer's specific application, electrical parameters to be expected from the process selected, parameters for computer simulation (CAD), and assistance to maximize wafer circuit yields.

The chart shown on this page reveals the approximate number of die that a wafer will provide as a function of the die size. The actual useful number of dice may be obtained by multiplying the unyielded quantity by the expected probed dice yield percentage.

CAPACITY

Three-inch or four-inch diameter wafers are supplied depending on the desired volume. Three-inch wafers are 15 ±1mil thick; four-inch wafers are 20 ±1mil thick.

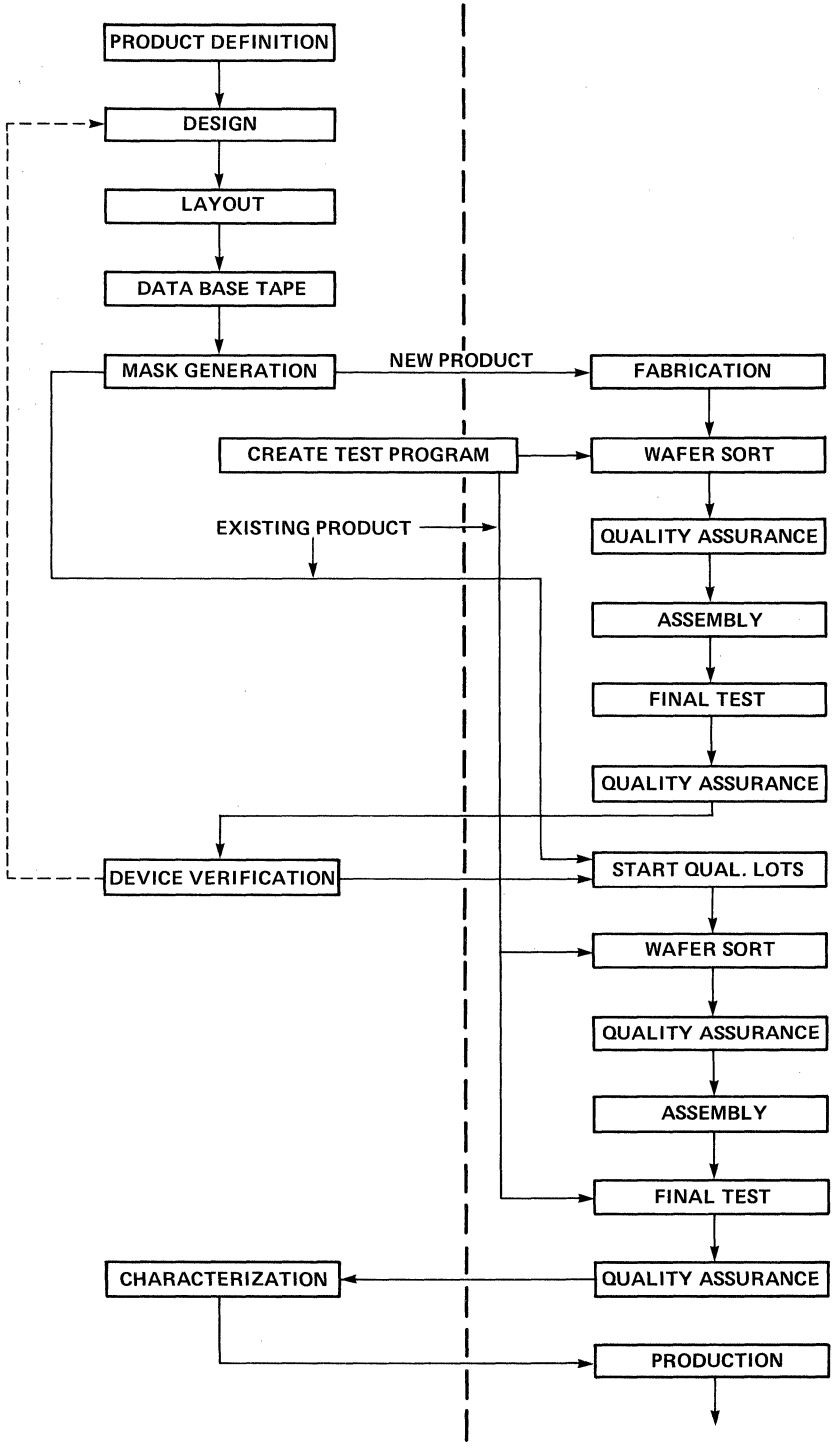
ASSEMBLED/TESTED PARTS

Custom products are available from PMI as wafers, die or assembled-and-tested parts. Assembled and tested devices can be supplied in a variety of packages including 12 to 40 pin DIPs (ceramic, Cerdip, or plastic), flatpacks, TO cans, and leadless chip carriers. The assembled parts undergo final electrical testing and screening. If die fabrication alone is desired, the processed wafers are electrically probed by PMI and bad die are marked on the wafer. Test parameters or test tapes are to be supplied by the customer.

DIE COUNT vs DIE SIZE

DIE SIZE (mils)		DIE AREA (sq. mils)	APPROXIMATE UNYIELDED* NUMBER OF WHOLE DIE PER WAFER		
X	Y	IN 1000s	2.0"	3.0"	100mm (4.0")
10	10	0.1	30116	68968	123946
20	20	0.4	7438	17106	31000
30	30	0.9	3262	7526	13618
40	40	1.6	1835	4214	7598
50	50	2.5	1148	2666	4824
60	60	3.6	790	1828	3346
70	70	4.9	570	1342	2438
80	80	6.4	424	1018	1846
90	90	8.1	330	804	1470
100	100	10.0	268	638	1164
110	110	12.1	214	532	964
120	120	14.4	184	434	804
130	130	16.9	150	370	682
140	140	19.6	130	310	580
150	150	22.5	108	276	496
160	160	25.6	94	236	434
170	170	28.9	88	208	392
180	180	32.4	72	184	338
190	190	36.1	66	164	302
200	200	40.0	60	144	276
210	210	44.1	52	130	256
220	220	48.8	48	120	222
230	230	52.9	42	108	208
240	240	57.6	38	95	184
250	250	62.5	32	88	164
260	260	67.6	32	80	156
270	270	72.9	32	76	148
280	280	78.4	24	66	130
290	290	84.1	22	66	120
300	300	90.0	22	60	112
310	310	96.1	22	52	112
320	320	102.4	16	52	94
330	330	108.9	16	52	88
340	340	115.6	16	44	88
350	350	122.5	16	42	80

*To calculate the number of good dice or parts multiply by the expected yield percentages.


PRODUCT DEFINITION
DESIGN
LAYOUT
DATA BASE TAPE
MASK GENERATION
NEW PRODUCT
FABRICATION
CREATE TEST PROGRAM
WAFER SORT
EXISTING PRODUCT
QUALITY ASSURANCE
ASSEMBLY
FINAL TEST
QUALITY ASSURANCE
DEVICE VERIFICATION
START QUAL. LOTS
WAFER SORT
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ASSEMBLY
FINAL TEST
CHARACTERIZATION
QUALITY ASSURANCE
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SECTION 15

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APPLICATION BRIEF NO. 1

STROBING THE DAC-08 UNDER LOGIC CONTROL

by Bob Blair and Donn Soderquist

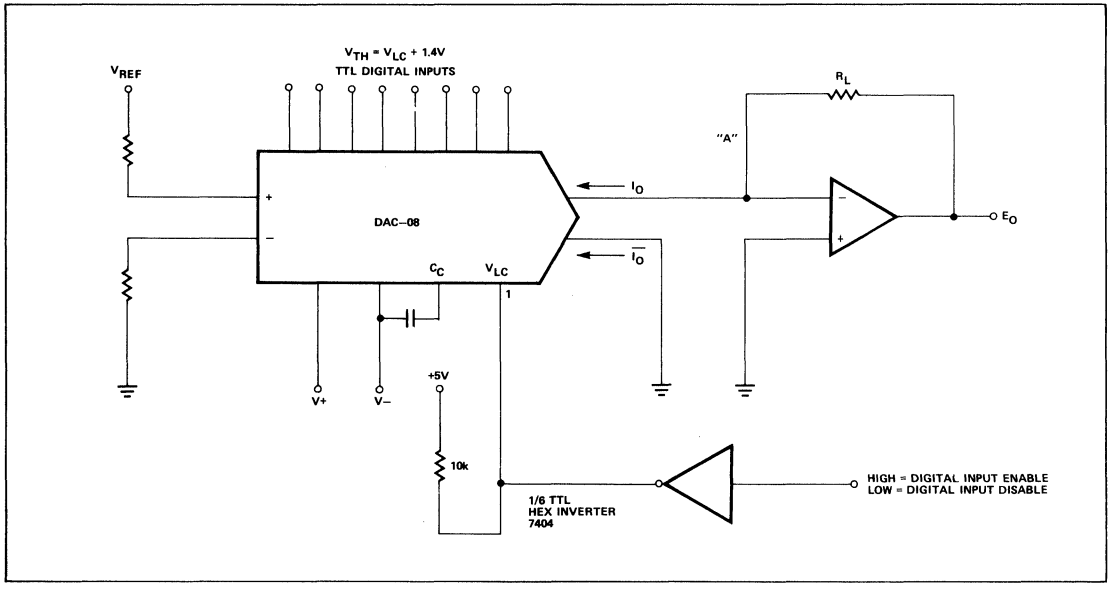
FEATURES

- Digital inputs are treated as all zeros by increasing the logic threshold to +6.4V.
- Single Line Logic Control
- Handy in Multiplying Applications
- When more than one DAC is connected to point "A" —party line connection — strobing is simple.
- Higher speed and greater simplicity when compared to the alternative method of disabling which is accomplished by reducing V_{REF} to zero.

GENERAL DESCRIPTION

Since the PMI DAC-08 has a variable logic input threshold, strobing the output is easily accomplished using the circuit below. Normally, for TTL thresholds, Pin 1 (V_{LC}) is grounded; but if it is connected instead to a hex inverter with a pullup resistor to +5V, all Digital inputs effectively become zeros. All current flows in I_O; no current flows in $\overline{I_O}$ no matter what the digital input code may be. When the hex inverter's output is low, normal TTL input logic threshold and operation is restored.

NOTE:
Recovery when logic inputs are enabled may be slower when DAC is on ±5V supply due to bias line saturation. This should be checked in the actual application.



APPLICATION BRIEF NO. 2

OP-10 INSTRUMENTATION AMPLIFIER CMRR vs FREQUENCY IMPROVEMENT

By Donn Soderquist and George Erdi

FEATURES

- Addition of one selected capacitor improves CMRR at 400Hz to >95dB.
- OP-10 Side "A" and Side "B" bandwidths are matched.
- Circuit uses existing nulling pins as frequency compensation connections.
- Added capacitor is in the range of 5pF to 100pF.

CAPACITOR SELECTION PROCEDURE

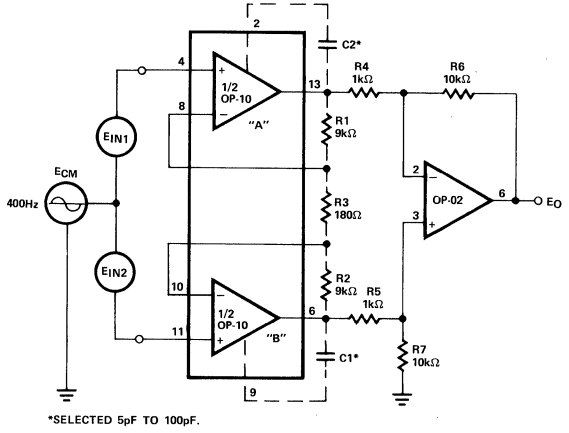
1. Connect E_{IN1} to E_{IN2} and to a 400Hz ±10V signal source.
2. While observing E_O with an oscilloscope, try different values of C1 or C2 until E_O is at a minimum.
3. Permanently install the selected capacitor.

GENERAL DESCRIPTION

Common mode rejection ratio (CMRR) versus frequency of the familiar three op-amp instrumentation amplifier can be optimized by matching the frequency responses of the input differentially-connected pair of op amps. The circuit shown uses one selected capacitor (to reduce the frequency response of the faster op amp) which is connected between an output and one of the pins usually used for nulling ΔV_{OS}.

Eight devices were tested in this connection. Improvement to greater than 95dB @ 400Hz was achieved on all devices, an improvement of 1 to 20dB over performance without the selected capacitor.

TRIPLE OP-AMP INSTRUMENTATION AMPLIFIER CIRCUIT



*SELECTED 5pF TO 100pF.

NOTES:

1. $E_O = (E_{IN1} - E_{IN2})\,A_{VCL}$
2. $A_{VCL} = \left(1 + \frac{R1 + R2}{R3}\right)\left(\frac{R6}{R4}\right) = 1000$
3. $CMRR = 20\ LOG\ \frac{E_{CM}\,(A_{VCL})}{E_O}$ @ DC
4. IF $\frac{R6}{R4} = \frac{R7}{R5}$, CMRR @ DC ≅ 120dB
5. AT 400Hz, CMRR IS A FUNCTION OF THE DIFFERENCE IN FREQUENCY RESPONSE OF SIDE "A" AND SIDE "B".
6. USE OF C1 OR C2, SELECTED USING THE PROCEDURE DESCRIBED, MATCHES THE FREQUENCY RESPONSE OF SIDE "A" AND SIDE "B", THEREBY MAXIMIZING CMRR AT 400Hz.

APPLICATION BRIEF NO. 3

DIGITAL NULLING OF OP05, OP06, AND OP07

By Charles Vinn

FEATURES

- Digitally-controlled offset nulling is achieved by imbalancing the first stage collector currents of a precision op amp.
- Greater than 1.5mV of offset voltage may be nulled to zero with 5μV resolution at 25° C.
- This application is especially useful in microprocessor-controlled systems where stringent error budgets exist.
- Circuit uses the nulling terminals with a DAC-08 substituted for the conventional nulling potentiometer.

GENERAL DESCRIPTION

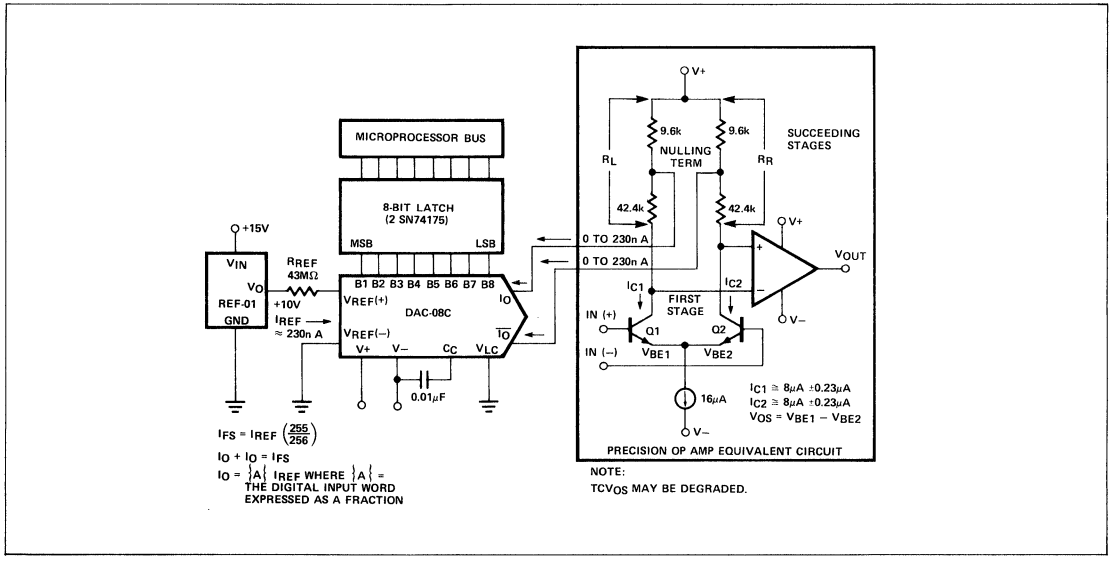
The input offset voltage of a precision op amp (OP-05 or OP-07) may be nulled to <5μV using the complementary current outputs of a DAC-08 to change the ratio of collector currents in the first stage. With V_{OS} being defined as the voltage which must be applied between the input terminals to force V_{OUT} to zero and assuming all errors to be in the first stage, V_{OS} may be expressed as:

1) $V_{OS} = \frac{kT}{q} \log_e \frac{I_{C1}}{I_{C2}} \cdot \frac{I_{S2}}{I_{S1}}$ where

k = Boltzmann's constant = 1.38×10^{-23} joules/° K
T = Absolute temperature, ° K
q = Charge of an electron = 1.6×10^{-19} coulomb
I_S = Theoretical reverse-saturation current
I_C = Collector Current

Changing the ratio I_{C1}/I_{C2} over a ±3% range results in an input offset voltage nulling range of greater than 1.5mV at 25° C.

CIRCUIT



APPLICATION BRIEF NO. 4

REF-02 TEMPERATURE CONTROLLER

By Bob Blair

FEATURES

- Variable Temperature Control
- Adjustable Hysteresis
- 12V To 32V Power Supply
- 2 IC Design
- Low Cost

SETPOINT DETERMINATION

With R2 = 1.5kΩ, the value of R1 may be found for any desired temperature using the following procedure:

$$E_1 \cong (\text{Desired Temp} - 25°C)\,(2.1mV/°C) + 630mV$$

$$R1 \cong R2\left(\frac{5 - E_1}{E_1}\right)$$

DESCRIPTION

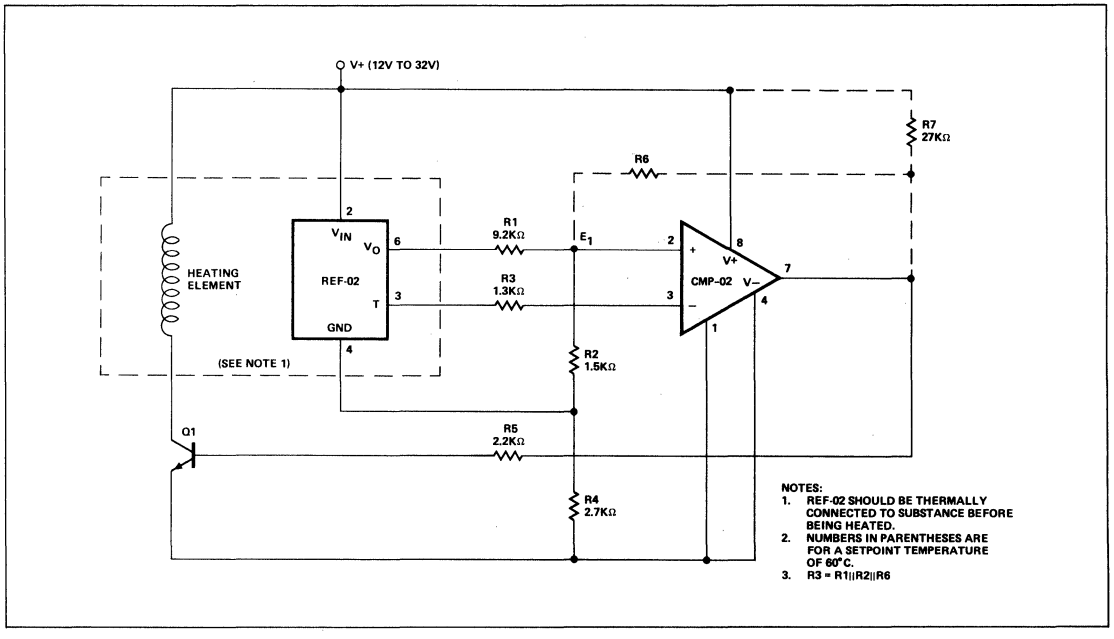
In the circuit below, temperature control is achieved using the REF-02 +5V Reference/Thermometer and a CMP-02 Precision Low Input Current Comparator. The CMP-02 turns on a heating element driver (Q1) whenever the present temperature drops below a setpoint temperature determined by the ratio of R1 to R2. The circuit also provides adjustable hysteresis and single supply operation.

HYSTERESIS DETERMINATION

R6 and R7 set hysteresis. With R7 = 27kΩ, R6 may be calculated:

$$R6 \cong \frac{[(V+) - 4V]}{(2.1mV/°C)\ (\text{Hysteresis width in } °C)}$$

CIRCUIT



APPLICATION BRIEF NO. 5

THE DAC-03 μP CONTROLLED D/A

by Mike Parsin

FEATURES

- **Software Control of Digital to Analog Converters**
- **Expandable Analog Outputs**
- **Self-Contained DACs Include Reference and Output Amps**
- **Low Cost**

GENERAL DESCRIPTION

This brief describes a μP controlled digital-to-analog conversion. By simply placing a digital word on the data bus and selecting 1 of 3 output ports on the PPI, a Ramp signal is generated at the output of DAC #1. The software can be modified to expand the number of analog outputs. Complex waveforms also can be created through software control. The following expression is used to determine a single Ramp Cycle Time when the clock is 2MHz.

1 Ramp Cycle = 20μsec + (16μsec × 256 steps) = 4.116msec

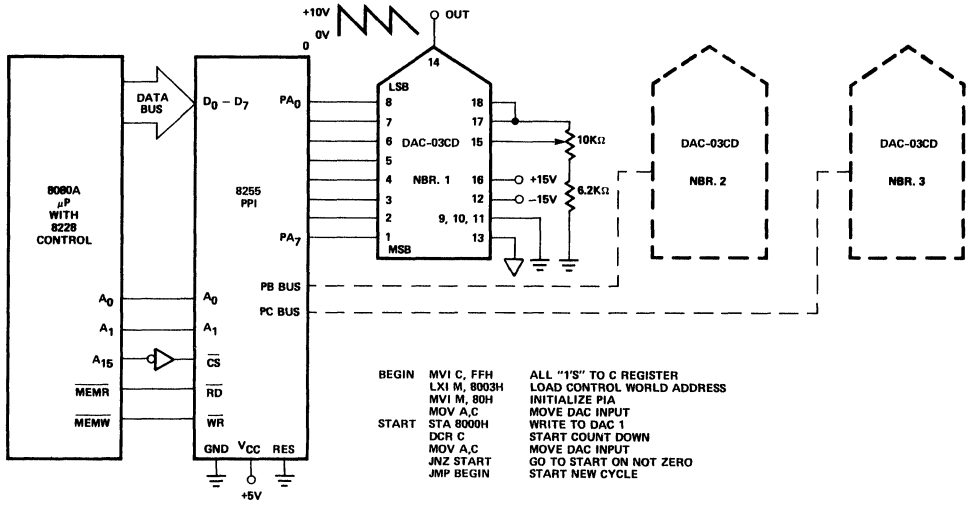
The software shown here was designed to demonstrate the ease of programming a DAC and exercising its capabilities.

For Two's Complement Coding replace the DAC-03 with the DAC-06, and a DAC-210 is ideal when Sign - Magnitude Coding is required.

APPLICATIONS

- Programmable voltage reference.
- Waveform generation:
  - A. Sawtooth
  - B. Triangular
  - C. Pulse
  - D. Complex

HARDWARE AND SOFTWARE



NOTE: DAC'S ARE WIRED FOR 8 BIT OPERATION.

APPLICATION BRIEF NO. 6

SINGLE SUPPLY OPERATION OF THE DAC-08 AND DAC-20

By Dennis Van Dalsen

FEATURES

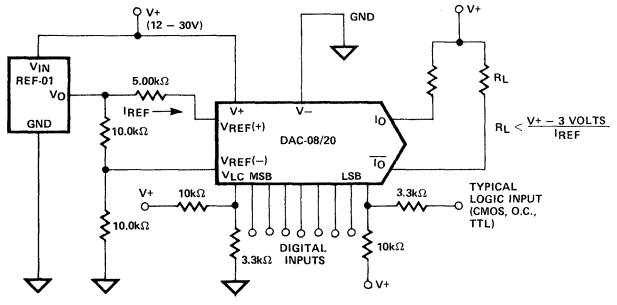
- Simple Interface
- Compatible with CMOS and Open Collector TTL
- No Degradation in Performance

GENERAL DESCRIPTION

The DAC-08 may be operated from a single supply when properly biased. This circuit will allow the use of a single power supply, or battery, and still realize the premium performance of these high speed DACs.

The resistive voltage divider inputs to V_{LC} and logic inputs provide the necessary voltage levels for operation from CMOS and Open Collector TTL logic.

CIRCUIT



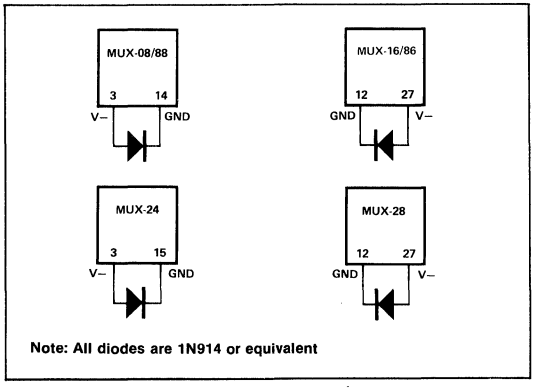
APPLICATION BRIEF NO. 7
NEGATIVE SUPPLY LOSS PROTECTION FOR PMI MULTIPLEXERS

By Shelby D. Givens

DESCRIPTION

Like most ICs, PMI BIFET multiplexers do strange things when the substrate is left floating. Removal of the −15V supply lead causes the substrate (V−) to float up past the potential on the GND terminal, and the substrate diode will turn on. If the ENABLE line is held low (the multiplexer is inoperative), nothing bad will happen. However, if the ENABLE line is high, the above condition (V− pin positive with respect to GND pin) could be catastrophic.

The solution to this potential problem is the same for all PMI multiplexers as shown in the figure: a small signal diode connected between V− and GND. The table shows data taken with and without the diode.



SOLVING MULTIPLEXER SUBSTRATE FLOTATION

MUX-08 NEGATIVE SUPPLY LOSS MEASUREMENTS

WITHOUT DIODE			WITH DIODE		
E_N	V−	I+	E_N	V−	I+
4.8V	−15V	9.8mA	4.8V	−15V	9.8mA
0V	−15V	10.6mA	0V	−15V	10.6mA
0V	OPEN	11.3mA	0V	OPEN	10.8mA
4.8V	OPEN	70mA*	4.8V	OPEN	9.7mA
(V+ = +15V)			(V+5+15V)		

*See Test Conditions

Note: If the negative power supply simply shorts out to ground, then with or without the diode, the multiplexer will continue to function with no catastrophic failure mechanisms.

TEST CONDITIONS

A power supply current limited to 70mA was used to make the measurements allowing non-destructive testing. Note that the excessive current problem is solved when the diode is attached as shown in the figure.

APPLICATION BRIEF NO. 8

3-DIGIT BCD D/A CONVERTER

by Vic Spiler

FEATURES

- Monotonic
- Linear to 2 LSBs
- Compatible with CMOS and TTL
- Excellent Voltage Compliance
- Low Cost

GENERAL DESCRIPTION

CALIBRATION PROCEDURES

With bits 1 through 4 turned off (DAC-08H), and bits 1 through 8 turned on (DAC-20E), code 099, adjust potentiometer 2 until the voltage out equals 0.990V.

With bits 1 through 8 turned off (DAC-20E), and with bits 1 through 4 turned on, code 900, adjust potentiometer 1 until the voltage out equals 9.000V.

REFERENCE CURRENTS IN BOTH DACs

$$I_{REF_1} = \frac{V_{REF}}{R_{REF_1}} = \frac{5V}{35k} = 0.1428mA$$

$I_{REF_1} = 0.1428mA$

I_{REF_2} = 16 to 1 current ratio to I_{REF_1}

$I_{REF_2} = 16\ (0.1428mA)$

$I_{REF_2} = 2.28mA$

FULL SCALE CURRENT

$$I_{FS_1} = \frac{99}{100} \cdot I_{REF_1} = \frac{99}{100}\ 0.1428mA$$

$I_{FS_1} = 0.1413mA$

$$I_{FS_2} = \frac{144}{256} \cdot I_{REF_1} = \frac{144}{256}\ (2.284mA)$$

$I_{FS_2} = 1.284mA$

$I_{FS_T} = I_{FS_1} + I_{FS_2}$

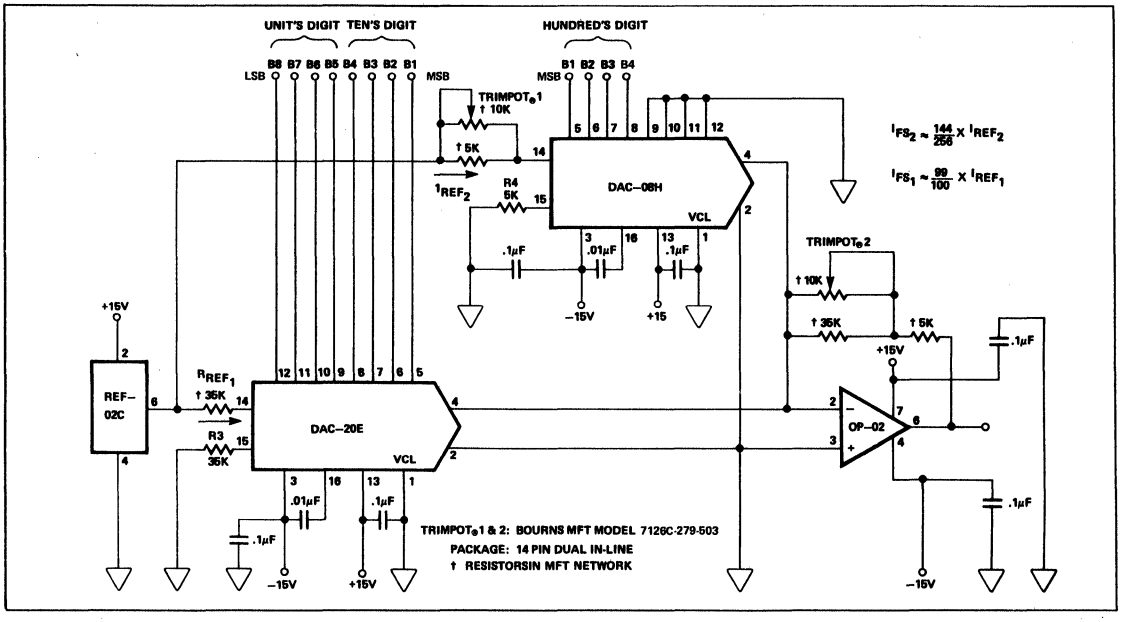
$I_{FS_T} = 1.425mA$

FULL SCALE VOLTAGE

$V_{FS} = 9.990V$

$V_{01} = 0.990V$

$V_{02} = 9.000V$



APPLICATION NOTE 6

A LOW-COST, HIGH-PERFORMANCE TRACKING A/D CONVERTER

INTRODUCTION

The availability of low-cost IC D/A converters, comparators and up/down counters makes possible construction of tracking A/D converters having high performance and reliability despite their small size and low cost. These A/D converters are suitable for a wide range of applications such as transducer and audio digitizing, infinite sample and holds, and servo-control loops. This paper describes an 8-bit tracking A/D converter that can be built using Precision Monolithics, Inc., DAC-100 CCQ3 D/A converter, CMP-01CJ Fast Precision Comparator and 4-bit MSI up/down counters.

TYPES OF A/D CONVERTERS

There are several popular styles of A/D converters (ADC) based on using a D/A converter in a feedback configuration. The three most common are: ramp or count-up, tracking or servo, and successive approximation.

Ramp types produce one conversion per each 2N clock counts for an "N" bit converter and are suitable only for very slowly changing analog data; additionally, the data can be taken out only at the end of the conversion period. Successive approximation types are quite fast, requiring only "N + 1" clock counts for conversion. They are capable of encoding fast-moving analog signals if an external sample-and-hold circuit is used to stop the analog data; again, the digital output is true only at the end of the conversion period.

For many applications, tracking ADCs can provide adequate speed while costing approximately the same as simple ramp types. Additional advantages are that no sample-and-hold circuit is required and that the digital data is continuously available at the output.

BASIC OPERATION

The tracking A/D is a relatively simple system, both in concept and in practice. The basic design requires three major elements: an up/down counter, a current output D/A converter, and a voltage comparator (see Figure 1). The voltage at the comparator's input will be the result of the analog input voltage minus the DAC output sink current times R_{IN} ($V_O = V_{IN} - I_1 \cdot R_{IN}$). Assuming a perfect comparator, if the output voltage (V_O) is above ground, the comparator's output will be low, causing the up/down counter to increase the DAC's output sink current by one LSB. (The counter actually counts down one count; this results from the DAC's utilization of complementary logic, i.e., an all-zero input produces maximum DAC output current.) The comparator continues to examine the voltage for polarity, and always drives the counter's code in the direction which causes the output voltage to approach zero. Once a balance is achieved, the loop is "locked," and tracks the analog input signal so long as the loop slew rate is not exceeded. When the loop is balanced, the converter's output is the binary-coded equivalent of the analog input.

When encoding a DC input signal, the digital output will "dither" or alternate between the two adjacent states which span the theoretically correct output value. This is of little consequence as all A/D converters have a similar error, known as the "quantizing" error.

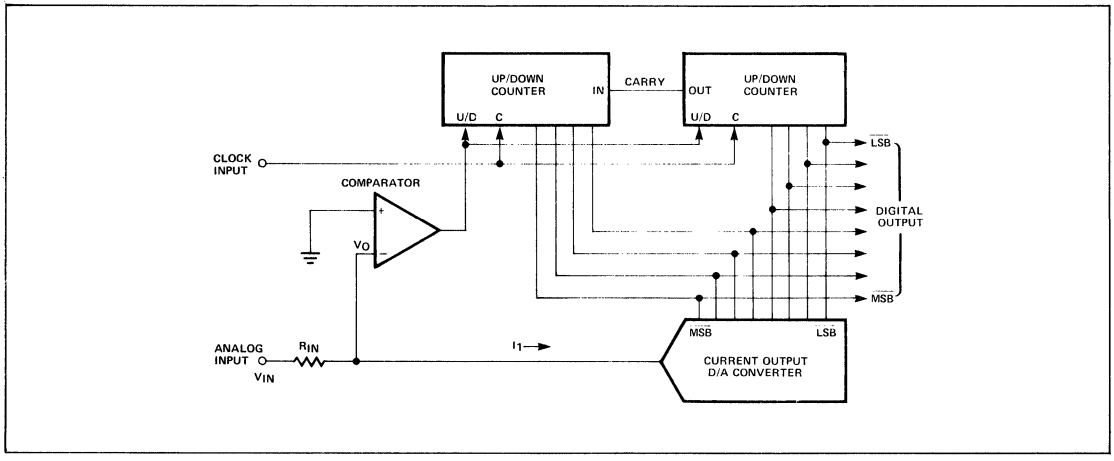


Figure 1. Basic Tracking A/D Block Diagram

In the actual circuit design, a "type-D" flip-flop is inserted between the comparator and the counter's up/down input. This is to insure adequate set-up time between the comparator's output change and the counter's next stage change.

Loop timing can be seen in Figure 2. After the positive clock transition, the counter changes to its next state and drives the DAC to its new output. After the DAC has settled and the comparator has come to its final state, the next positive clock transition loads the comparator's new state into the flip-flop and the cycle repeats.

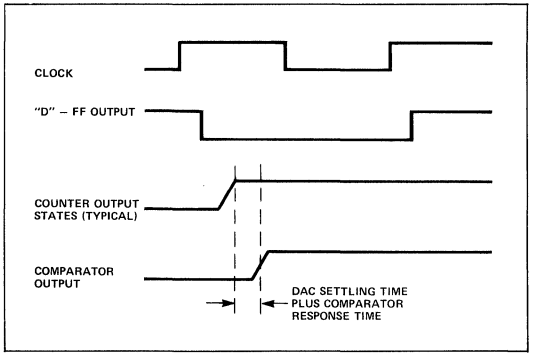


Figure 2. System Timing Diagram

FINAL CIRCUIT DESIGN

The completed 8-bit tracking A/D design is shown in Figure 3. The digital output is available in complemented form, as the DAC-100 utilizes complementary logic. Diode clamps insure the DAC output remains near zero despite input and turn-on transients. For this 8-bit design, the two least significant digital inputs of the 10-bit DAC are not required and are connected to +5V, thus turning them off. Diodes are also used to insure that a positive voltage is applied to the V+ pin (Pin 14) as soon as the +5V supply comes up. The clock, although extremely simple, is quite stable over a wide range of temperatures and supply voltages. Several layouts were tried, with no perceptible differences in performance. (See Figure 4.)

TRIMMING

The circuit requires only one trimming operation. The full-scale output current of the DAC is adjusted to produce proper encoding at full scale input. Although several schemes are possible, the simplest is to place +10.0V at the input, and trim the 200Ω Full Scale Adjust pot to produce a low output at the seven most significant bits with the LSB alternating states (dithering) at the clock frequency.

VOLTAGE OUTPUT APPLICATIONS

The basic tracking A/D uses a "current-comparison" technique; the analog voltage is not reconstructed at the comparator's input, thus eliminating the need for an op amp to convert the DAC-100's current output to a voltage. For applications such as infinite (no-droop) analog sample-and-hold circuits, the OP-01CJ, a low-cost, fast slewing, fast settling op amp with internal compensation can be added as in Figure 5. This configuration also provides very high input impedances, without requiring an extra buffer amplifier. The reconstructed analog voltage is available at the output of the op amp; gating the counter "off" stores the data in analog form.

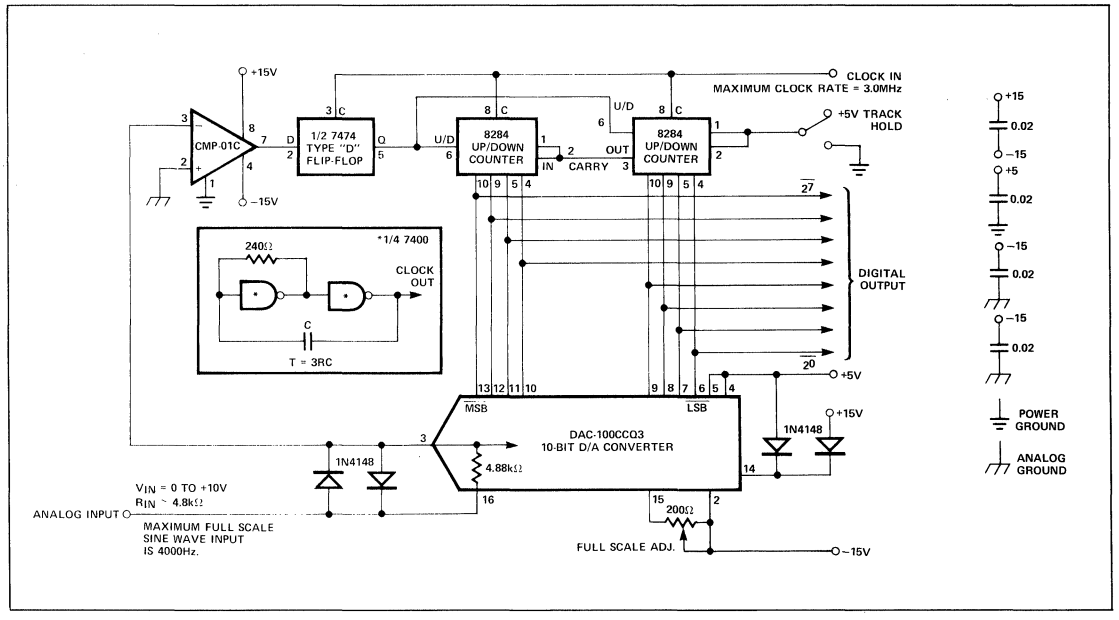
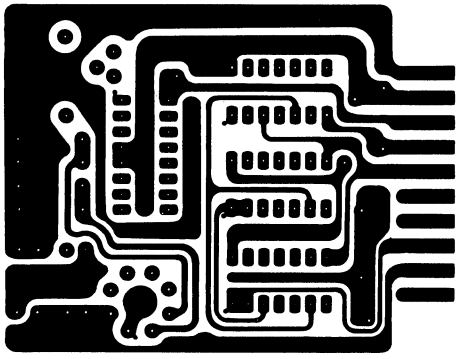
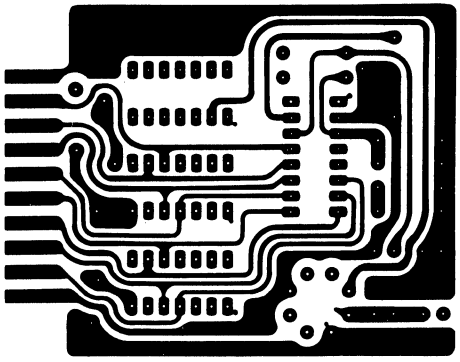


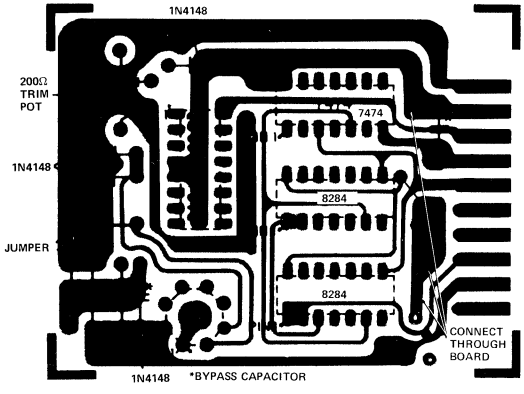
Figure 3. Complete Schematic — 8-Bit Tracking A/D Converter



FRONT



BACK



FRONT

CONNECTOR		
FRONT	BACK	
ANALOG GND	ANALOG GND	
+5V	DIGITAL OUTPUT	2^7
ANALOG IN		2^6
DIGITAL GND		2^5
CLOCK		2^4
N.C.		2^3
N.C.		2^2
TRACK & HOLD		2^1
+15V		2^0
N.C.	-15V	

8-BIT TRACKING A/D PARTS LIST

Quantity	Description	Quantity	Description
1	DAC-100CCQ3 D/A Converter	1	200Ω Trimpot, Bourns 3359P
1	CMP-01CJ Comparator	4	IN4148 Diodes
2	8284 Up/Down Counters	5	Ceramic Capacitors
1	7474 Dual D-Type Flip-Flop	1	Carbon Composition Resistor
1	7400 Quad Gate	1	PC Board

Figure 4. Actual Size Printed Circuit Layout — Circuit of Figure 3

BIPOLAR OPERATION

Bipolar operation (±5V) can be obtained by injecting a current equal to 1/2 the full scale current into the DAC-100 sum line. This can be accomplished by applying +6.4V to the internal bipolar resistor of the DAC-100 (Pin 1) — a 500Ω symmetry-trimpot to produce a high output at all bits, with the normal "dither" in the LSB only. Next, ground the input and adjust the Full Scale trimpot to produce an output which alternates between 10000000 and 01111111.

0 TO +5V OPERATION

Operation with 5 volt full scale inputs (0V to +5V or ±2.5V) can be obtained by specifying the DAC-100CCQ4.

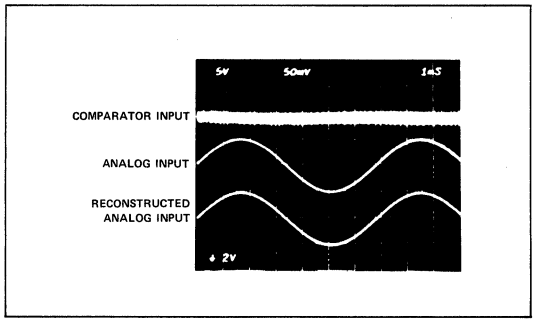
0.05% APPLICATIONS

Applications requiring 10 bits of resolution with 0.05% linearity can be implemented by adding a third up/down counter and utilizing all 10 inputs of a DAC-100ACQ3 (or Q4). See Figure 5.

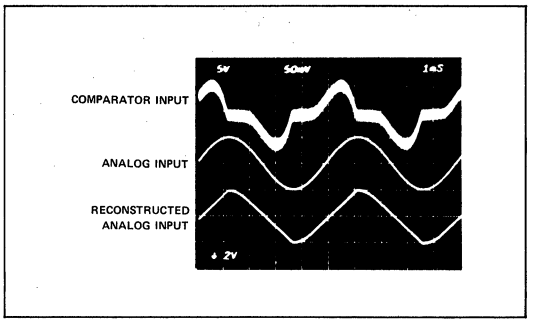
TRACKING A/D CONVERTER WAVEFORMS

These scope photos were taken to indicate the waveforms observed at the comparator input during normal and abnormal operation of the converter. The output analog voltage trace was generated by applying the encoded digital output to a second D/A converter.

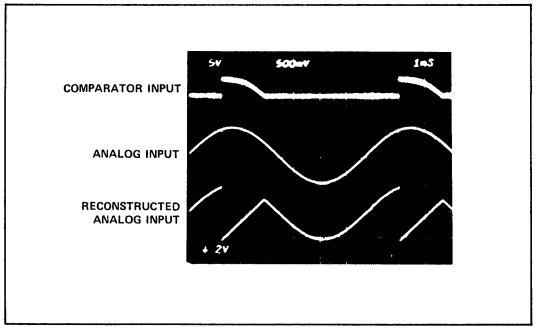
NORMAL OPERATION



SLEW RATE LIMITING



INPUT OVER-RANGE



PERFORMANCE

Performance of the completed converter is quite impressive despite the low cost and small size. Using clock rates of 3.0MHz, 10 V_{p-p} signals can be accurately tracked to frequencies of about 4.0kHz; higher frequencies can be accommodated by reducing the peak-to-peak amplitude.

Fully monotonic operation is obtained from 0° to 70° C; this is achieved because the DAC-100CQ3 is guaranteed to have ±1/2 LSB linearity to 8 bits (0.2%) over this temperature range, and the DAC-100ACQ3 has ±1/2 LSB linearity to 10 bits (0.05%).

All D.C. static errors can be attributed to the analog components only; the comparator makes no contribution to linearity errors, but its V_{OS} and V_{OS} drift with temperature are a

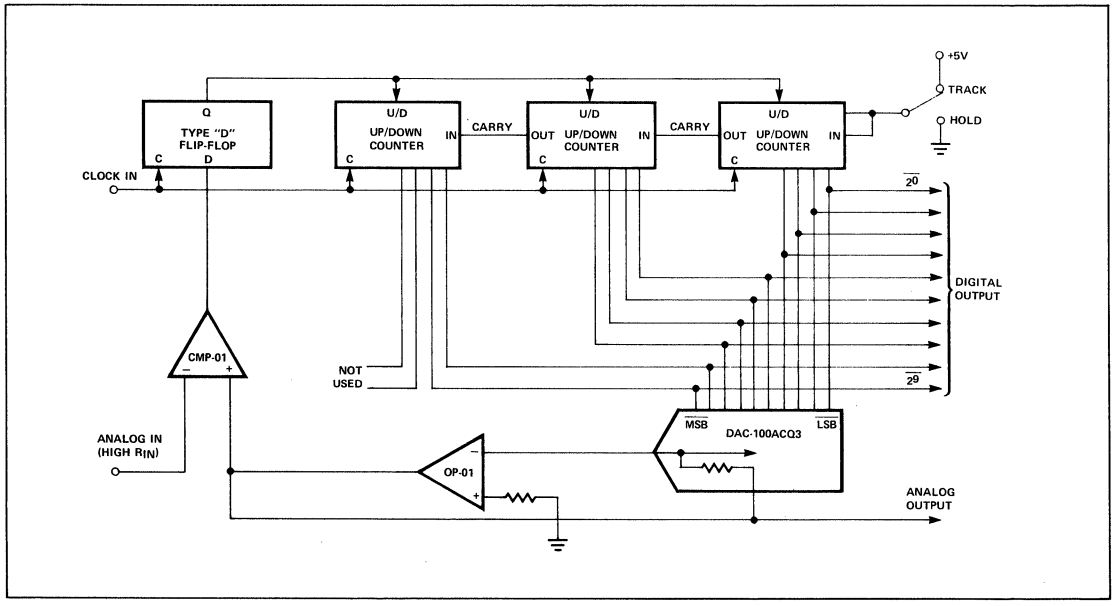


Figure 5. 10-Bit Voltage Output A/D Converter Block Diagram

consideration in the zero scale and full scale performance, and especially so in bipolar applications. The worst case DAC-100 zero error over 0° C to 70° C is 0.6mV; adding to this the 3.5mV maximum V_{OS} of the CMP-01C results in a worst case zero scale error of 4.1mV, which is acceptably small compared to the value of 1/2 LSB (19.5mV) for the 8-bit A/D.

Because the V_{OS} drift of the CMP-01C is typically only 1.8μV/° C even without offset triming, the full scale drift will be almost entirely a function of the DAC-100CC tempco —60ppm/° C maximum.

For 10-bit applications, the comparator V_{OS} becomes significant; the CMP-01C can be nulled, or the 0.8V maximum V_{OS} CMP-01E can be utilized without nulling. Nulling of the comparator is not required in bipolar applications; this is accomplished by the bipolar symmetry trimming.

Other performance characteristics of the completed converter are listed in Table 1.

TABLE 1. PERFORMANCE DATA

	8-BIT	10-BIT
Nonlinearity (0° C to +70° C)	0.2% Maximum	0.05% Maximum
Full Scale Tempco (0° C to +70° C)	60ppm Maximum	60ppm Maximum
Zero Scale Error (0° C to +70° C)	0.10 LSB Maximum	0.20 LSB Maximum*
Zero Scale Error Comparator Trimmed (0° C to +70° C)	0.02 LSB	0.08 LSB
Full Scale Voltages	0V to +10V, ±5V 0V to +5V, ±2.5V	0V to +10V, ±5V 0V to +5V, ±2.5V
Power Supply Rejection (0° C to +70° C)	0.02% per % Maximum	0.02% per % Maximum
Power Consumption (V_S = ±15V, +5V)	1.4W Maximum	1.77W Maximum

*Untrimmed CMP-01E

MILITARY TEMPERATURE RANGE OPERATION

Operation over wider temperature ranges can be obtained by simply specifying appropriate temperature range components. The simplicity of the all IC design coupled with the compatibility with MIL-M-38510 processing assures high reliability in military applications.

CONCLUSION

Extremely compact, low power consumption, all IC tracking A/D converters are made possible by combining Precision Monolithics, Inc. DAC-100 series 10-bit D/A converter, CMP-01 series comparator, and commerically available MSI up/down counters. Layout, construction and adjustment are noncritical. The simplicity and low cost of the tracking A/D converter invites usage in many new applications, including single channel digitizing at remote transducer locations.

APPENDIX — USEFUL DATA AND FORMULAE

	10V Full Scale	5V Full Scale
LSB — 8 Bits	39.1mV	19.5mV
10 Bits	9.85mV	4.92mV

Loop Slew Rate = Clock Frequency X V_{LSB} = f_c X V_{LSB}

Maximum Clock Frequency = $1/(T_A + T_B + T_C + T_D + T_E)$

WHERE: T_A = Flip-Flop Propagation Delay

T_B = Minimum Counter Set-Up Time

T_C = Counter Propagation Delay

T_D = D/A converter Settline Time (to n-bits)

T_E = Comparator Response Time

$$\text{Minimum Clock Frequency} = \frac{\pi \cdot V_{IN_{p\text{-}p}} \cdot f_{IN}\,\text{max}}{V_{LSB}}$$

APPLICATION NOTE 10

SIMPLE PRECISION MILLIVOLT REFERENCE USES NO ZENERS

by Donn Soderquist

GENERAL DESCRIPTION

A low output impedance millivolt source is frequently required in test systems, for generating small currents with moderate resistance values, and for general laboratory use. An excellent millivolt source can be built using only two parts; an instrumentation op amp and a potentiometer. The op amp is connected as a unity-gain buffer (Figure 1) and the output is adjusted to the required voltage using the offset nulling terminals. The amplifier must have suitable characteristics such as low long term drift, freedom from chopper and "popcorn" noise, good power supply rejection and low offset voltage drift with temperature. To achieve low output impedance the op amp must have high gain around zero output voltages, and should have negligible thermal-induced drift for stable performance under varying load conditions. Use of a high performance bipolar input op amp such as the Precision Monolithics OP-05CJ provides low drift without chopper noise. With a typical initial offset voltage of 0.3mV, outputs from about −3.5mV to +3.5mV can be achieved. Adjusting the offset of the OP-05CJ to a value other than zero will create a drift equal to 3.3μV/°C per millivolt of output setting. The circuit's low frequency noise will be less than 0.65μV peak-to-peak with an output impedance of less than one milliohm. Long term drift will be much less than 3.5μV per month and power supply rejection is about 10μV/Volt.

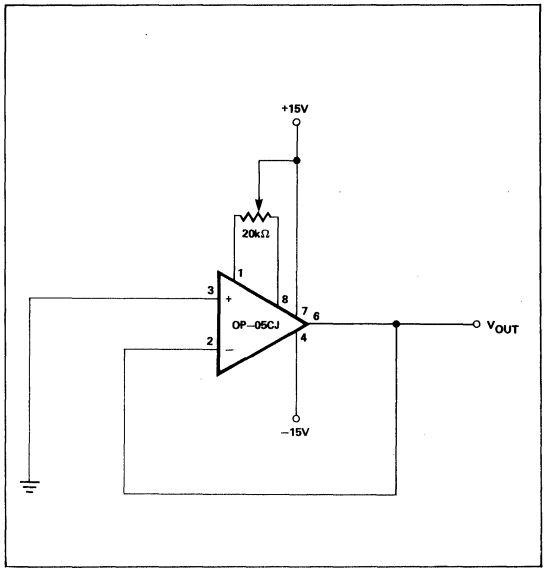


Figure 1. Zenerless Precision Millivolt Source

APPLICATION NOTE 11

A LOW-COST, EASY-TO-BUILD SUCCESSIVE APPROXIMATION ANALOG-TO-DIGITAL CONVERTER

By Donn Soderquist

Successive Approximation Analog-to-Digital Converters have often been considered to be complex, expensive and troublesome circuits to produce. This application note describes a high-speed 8-bit successive approximation A/D easily constructed using only three readily available ICs. Precision Monolithics' DAC-100 Digital-to-Analog Converter, CMP-01 Fast Precision Voltage Comparator, a Successive Approximation Register plus a handful of discrete components complete the design. Despite the simplicity, the A/D is capable of 8-bit conversions in 6μsec, and can easily be expanded to 10-bit resolution operation.

FEEDBACK A/D CONVERTERS

Most popular A/D converters built today use a digital-to-analog converter as part of a feedback or servo loop. Three of the most common types are the Ramp, Tracking, and Successive-Approximation; these differ primarily in the type of programming logic circuitry used to drive the D/A converter. All three types perform a comparison between the analog input and the output of a D/A converter; the logic changes the D/A output so that it approaches the analog input —when they are equal, the input to the DAC is the correct digitally encoded number (Figure 1).

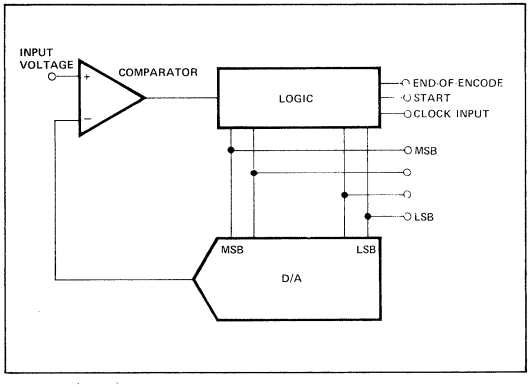


Figure 1. Basic Feedback A/D Converter

The Ramp or Count-up type ADC uses up-counters for the programming logic. A start command clears the counters which then count up until the comparator output changes. The user must allow 2^n clock periods to insure a complete conversion; therefore only very slowly varying data may be converted.

Tracking A/D converters use up/down counters for the programming logic; the comparator output forces the counters to "track" the changes in the analog input. Once initial "lock" is acquired the correct digital output is continuously available, and the converter may be capable of encoding fairly fast-moving input signals without requiring a sample and hold circuit. (Complete details on the construction of this type of converter are available in Precision Monolithics Application Note 6, "A Low-Cost, High-Performance Tracking A/D Converter.")

Tracking ADCs are at their best when used to encode a single signal with a well-behaved maximum slew rate; multiplexed or video signals have large discontinuities which cause large errors while the tracking loop moves to acquire a new "lock" on the signal.

Successive Approximation A/D Converters are attractive for their rapid conversion rates and have found wide acceptance in video and multiplexed data systems. Recently-announced ICs provide the three basic converter building blocks in integrated form, reducing the cost and complexity of this approach to a figure at or below that of the ramp and tracking types. The great advantage of the SA ADC is that complete "N"-bit conversions can be accomplished typically in N+1 clock periods — for a 10-bit converter this would be a speed improvement of about 100 times over the ramp type.

BASIC SUCCESSIVE APPROXIMATION A/D CONVERSION

An SA ADC operates by comparing the analog input to a series of "trial" conversions; the first trial compares the input to the value of the most significant bit (MSB) or half of full scale. Figure 2 shows the progression of trials for a 3-bit converter. If the input is greater than the MSB value, the MSB is retained and the converter moves on to "trying" the next most significant bit, or three-quarters full scale. If the input had been less than the MSB, the logic would have turned the MSB off before going on to the next most significant bit, or one-quarter full scale. This "branching" continues until each successively smaller bit has been tried, with the entire process taking "N+1" trials.

To implement the logic for the successive approximation algorithm, a configuration similar to Figure 3 may be employed wherein a start command places a "one" in the first bit of a shift register. This sets the first latch to "one," and turns on the DAC's MSB. If the comparator output remains slow, the "one" will remain in the latch; if not, the latch will be reset to zero before the next bit trial begins. The next clock cycle causes the shift register to place a "one" in the second bit and

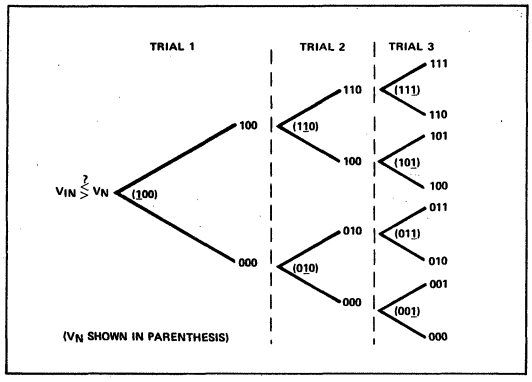


Figure 2. Flow Diagram for 3-Bit Successive Approximation A/D Conversion

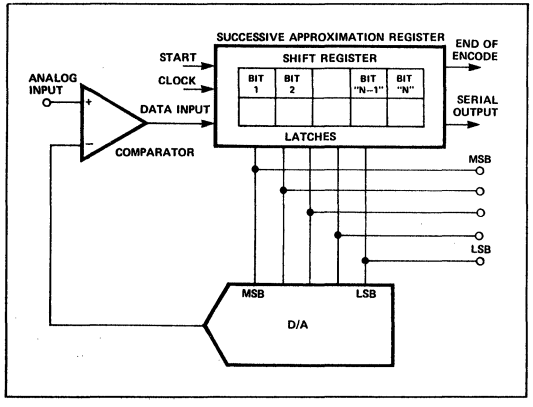


Figure 3. Successive Approximation A/D Converter

a similar process continues until all bits have been tried. After the last bit's trial, the end-of-encode output changes state indicating the parallel data is ready to be used. A useful feature of successive approximation conversion is that the correctly converted data is also available in serial form; this is handy for transmission of data on a single bus.

The complete sequence of events is demonstrated in the timing diagram of Figure 4. Note that "negative true" logic is shown; the DAC-100 employs a complementary binary code and the AM2502 produces a "low" output during each bit's trial, thus producing the standard successive approximation routine starting with the MSB trial and working towards the LSB trial. All events are initiated during positive-going clock transitions; the conversion process starts when the S input is held low, which also causes the CC (Conversion Completed) output to go high. After all bits have been tried, the last positive clock transition returns the CC to a low state, indicating the conversion has completed.

"CURRENT" COMPARISON

The previous discussion has indicated that the function of the comparator was to perform a comparison between the

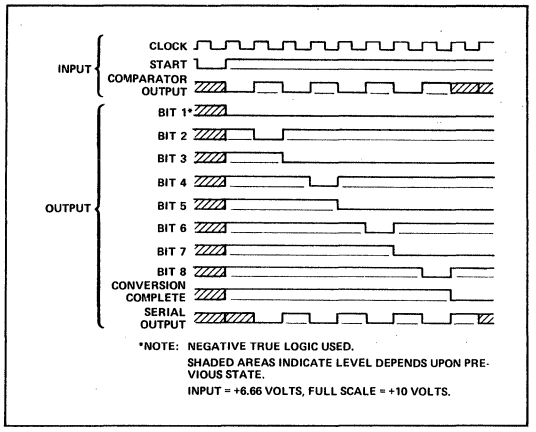


Figure 4. Timing Diagram

analog input voltage and the output voltage of the D/A converter. Higher speed conversions may be achieved by using the output of a fast current output DAC directly. This may be implemented as shown in Figure 5, where the comparator examines the polarity of ($V_{IN} - I_{IN} R_{IN}$). The "current comparison" method eliminates the need for a current-to-voltage converting op amp which is by far the slowest element in most D/A converters.

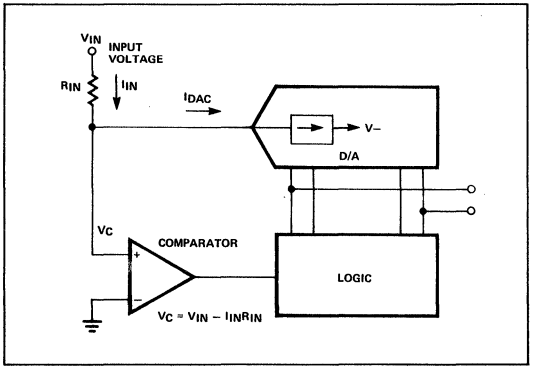


Figure 5. "Current Comparison" A/D Input

COMPLETE CIRCUIT

The schematic for the complete 8-bit A/D converter is shown in Figure 6. It is seen that the complete circuit adds very few components to the basic three ICs of the block diagram. A 200Ω potentiometer is used to adjust the full scale output and R1 is used to inject a +1/2 LSB value current into the sum node. This insures that adjacent code point transitions occur at 1/2 LSB points for minimum overall error. The clamp diodes minimize settling time and prevent large inputs from damaging the DAC output. For an 8-bit, 10 volt system the CMP-01CJ's maximum offset voltage is less than 1/10 LSB and should not require nulling.

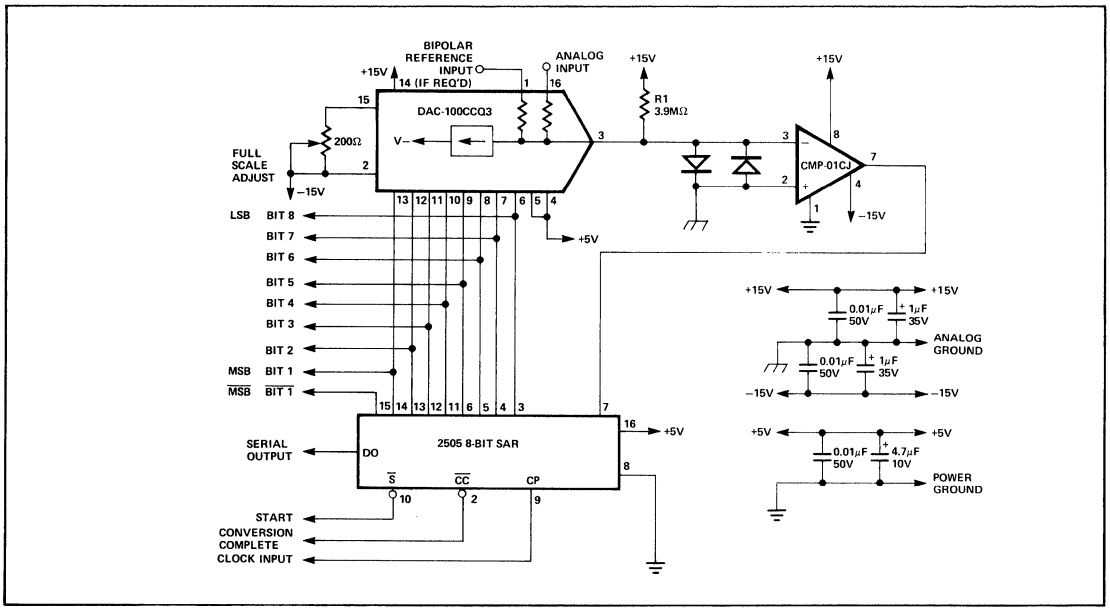


Figure 6. Complete 8-Bit A/D Schematic

GROUNDING

For optimum noise rejection, digital (power) ground currents should not flow in signal input ground return lines. Analog and power grounds should be connected as close as possible to the A/D converter input connector. Figure 7 illustrates a typical system installation showing the ground connections.

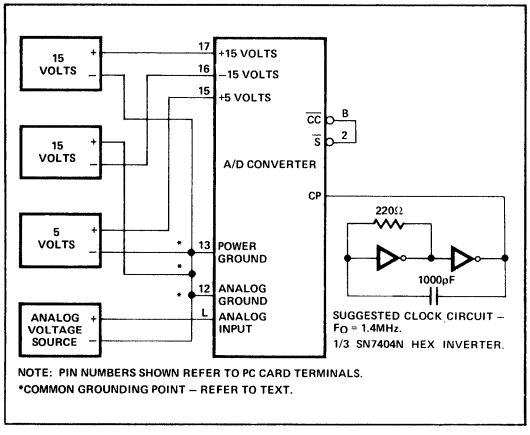


Figure 7. Grounding and Supply Hookup

LAYOUT

A suggested layout for an 8-bit converter is shown in Figure 8. This layout demonstrates some of the basic rules of good A/D converter practice: analog wiring is kept as short as possible and is separated from digital lines; the DAC output trace is especially short and directly connected to the comparator input and clamping diodes. Generous power supply bypassing has been employed using both disc and electrolytic capacitors. Other layouts can be easily designed because of the extreme simplicity of this circuit.

SERIAL OUTPUT

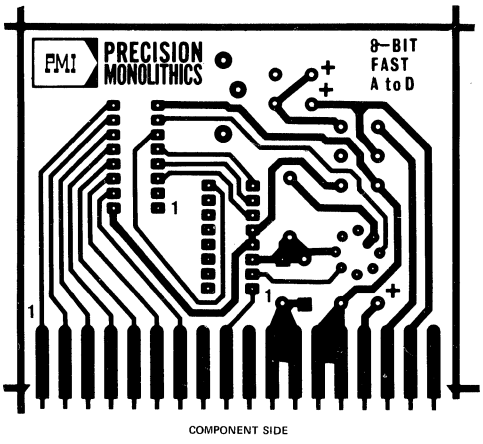
The digital output is available in serial NRZ (non-return-to-zero) format at the data output (DO) shortly after each positive-going clock transition. Serial output is especially convenient in applications where system wiring must be minimized, such as in one A/D per channel systems. Performing the A/D conversion process in close proximity to the signal source has the advantage of reducing errors associated with transmission of low level analog signals; instead, digitally encoded signals are transmitted with their inherent low error rates and ease of multiplexing.

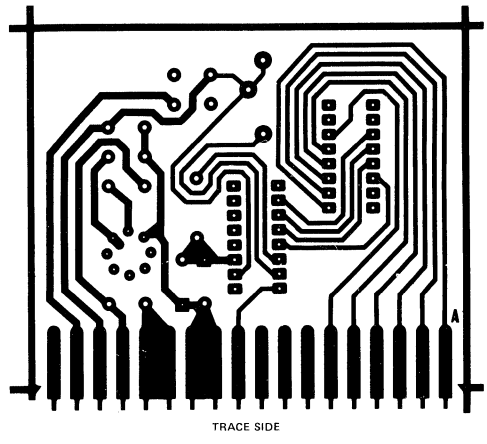
BIPOLAR OPERATION

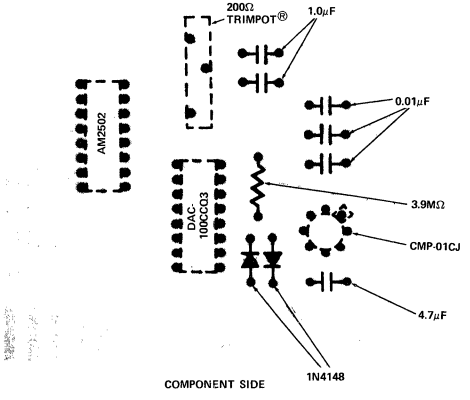
Bipolar operation can be obtained by injecting a current equal to 1/2 full scale into the sum node. This can be accomplished by applying +6.4 volts through a 500 ohm potentiometer to the internal bipolar resistor of the DAC-100. Both Bit 1 and Bit 1 are available so 2's complement or offset binary coding may be obtained as desired.

0 TO +5V, ±2.5V OPERATION

Operation with 5V full scale inputs (0 to +5V, ±2.5V) may be obtained by specifying DAC-100 models with a Q4 suffix.







CONNECTOR PIN CONNECTIONS

18	N.C.	V	N.C.
17	+15 VOLTS	U	+15 VOLTS
16	−15 VOLTS	T	−15 VOLTS
15	+5 VOLTS	S	+5 VOLTS
14	POWER GROUND ⏚	R	POWER GROUND ⏚
13	POWER GROUND ⏚	P	POWER GROUND ⏚
12	ANALOG GROUND ⏚	N	ANALOG GROUND ⏚
11	ANALOG GROUND ⏚	M	ANALOG GROUND ⏚
10	N.C.	L	ANALOG INPUT
9	BIPOLAR REFERENCE VOLTAGE INPUT	K	N.C.
8	N.C.	J	N.C.
7	BIT 1	H	N.C.
6	BIT 1	F	BIT 5
5	BIT 2	E	BIT 6
4	BIT 3	D	BIT 7
3	BIT 4	C	BIT 8
2	S START	B	CC CONVERSION COMPLETED
1	CLOCK INPUT	A	DO SERIAL OUTPUT

Figure 8. 8-Bit A/D Layout

CALIBRATION

For unipolar, 8-bit, 10 volt full scale calibration apply +9.941 volts (full scale -3/2 LSB) to the input. Adjust the gain potentiometer until the digital output is alternating between "0000 0000" and "0000 0001". This calibrates the converter at a transition point insuring correct outputs over the analog input range. No zero adjust is necessary due to the low comparator input offset voltage (V_{OS}), virtually zero output offset of the DAC and the correct +1/2 LSB bias established by R1.

For 8-bit, ±5 volt full scale offset binary operation, first perform the unipolar calibration as described above with the bipolar reference removed. Next connect the +6.4 volt bipolar reference through the 500 ohm potentiometer to the bipolar input resistor. With -5.000 volts as an analog input, adjust the 500 ohm potentiometer until the digital output is alternating between "1111 1111" and "1111 1110". For calibration at lower bit resolutions refer to Table 1.

PERFORMANCE

Performance of the completed converter for 6, 7 and 8-bit resolution applications is shown in Table 2. To assure fully monotonic operation in 8-bit applications the DAC-100CC grade with its maximum nonlinearity of 0.2% from 0° to 70° C should be specified. Applications requiring 8-bit resolution with 0.3% or less linearity may utilize the lower cost DAC-100DD types.

All D.C. static errors can be attributed to the analog components only; the comparator makes no contribution to nonlinearity, but its 25° C V_{OS} and V_{OS} drift with temperature are a consideration in the zero scale and full scale performance, and especially so in bipolar applications. The worst case DAC-100 zero error over 0° to 70° C is 0.6mV; adding to this the 3.5mV maximum V_{OS} of the CMP-01C results in a worst case zero scale error of 4.1mV, which is acceptably small compared to the value of 1/2 LSB (19.5mV) for the 8-bit A/D.

Table 1. Reduced Resolution Application Data

Resolution Desired		Offset Current Value (1/2 LSB)	Conversion Complete Indicator	Full Scale Calibration Point	LSB (10VFS)
8 Bits	3.9MΩ	3.9μA	CC	9.941V	39mV
7 Bits	2MΩ	7.8μA	Bit 8	9.883V	78mV
6 Bits	1MΩ	15.6μA	Bit 7	9.766V	156mV
5 Bits	470kΩ	31.3μA	Bit 6	9.531V	313mV
4 Bits	240kΩ	62.5μA	Bit 5	9.163V	625mV

Table 2. Performance Data

Resolution D/A	6 Bits DAC-100DDQ3	7 Bits DAC-100DDQ3	8 Bits DAC-100CCQ3
0° to 70° C Maximum Nonlinearity	±0.3%	±0.3%	±0.2%
0° to 70° C Full Scale Tempco Maximum	120ppm/° C	120ppm/° C	60ppm/° C
Zero Scale Error Maximum	±0.05 LSB	±0.1 LSB	±0.2 LSB
Conversion Time 1.5MHz Clock	4.7μs	5.3μs	6.0μs
Unipolar Reference		Internal	
Bipolar Reference		External +6.4 Volts	
Input Impedance (+10V or ±5V Scale)		5kΩ Nominal	
Input Impedance (+5V or ±2.5V Scale)		2.5kΩ Nominal	
Quantizing Error		±1/2 LSB	
Output Code Unipolar		Complementary Binary	
Output Code Bipolar		Complementary Offset Binary	
Clock		External	
Logic Output Drive Capability		6 TTL Loads	
Analog Power Supply Range		±6V to ±18V	
Digital Power Supply Range		+5V ±5%	
Power Consumption ±15V and +5V Supplies		935mW Maximum	

Because the V_{OS} drift of the CMP-01C is typically only 1.8μV/° C even without offset trimming, the full scale drift will be almost entirely a function of the DAC-100CC tempco —60ppm/° C maximum. (Tempco of DAC-100DD models is 120ppm/° C.)

REDUCED RESOLUTION APPLICATIONS

Encoding time may be reduced in applications not requiring the full 8-bit resolution. In convert-on-command applications, the negative-going transition of the (N+1) bit may be used as the Conversion Completed (CC) signal; the register will continue to step through the remaining bits so the CC level will be present for one clock period only. For continuous conversion applications, the register may be truncated by applying a low level to the S input; however, caution must be observed to prevent possible stalling on power-up: the S input should be generated by either the CC or bit (N+1) going to a low state. Figure 9 demonstrates a 6-bit, continuous-encoding application. Since reducing the resolution increases the size of the LSB, the value of R1 and the full scale calibration point should be changed accordingly, as shown in Table 1. Additional speed in reduced resolution applications may be achieved by increasing the clock frequency.

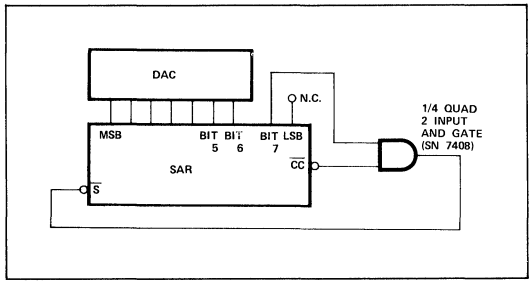


Figure 9A. Short-Cycled Continuous Coding (6 Bits Shown)

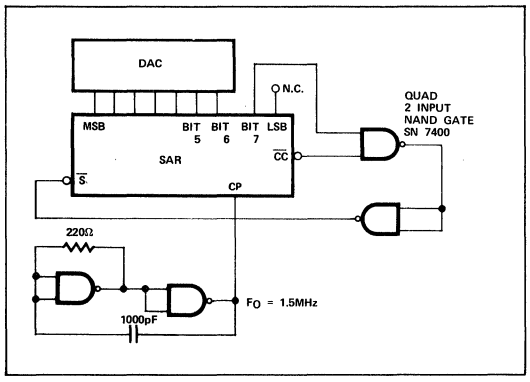


Figure 9B. Short-Cycled Continuous Encoding (Alternate Method Including Clock)

10-BIT APPLICATIONS

The basic 8-bit converter may easily be expanded to 10 bits by using a 2504 12-bit Successive Approximation Register; it may be allowed to step through all 12 bits or short-cycled as described above (Figures 9A, 9B). All DAC-100 Series devices have 10-bit resolution; for applications requiring 10-bit monotonic performance the DAC-100ACQ3 or Q4 grades with maximum nonlinearity of ±0.05% (0° to 70° C) should be specified; for less demanding applications the ±0.1% DAC-100BCQ3 (Q4) grades are recommended. Due to the 10mV LSB size, comparator V_{OS} can provide significant zero error. This can be eliminated in unipolar applications by nulling the CMP-01CJ or specifying the 0.8mV offset CMP-01EJ. No initial V_{OS} improvement is required in bipolar applications, as this error will be eliminated during the bipolar calibration procedure. The offsetting resistor (R1) should be 15MΩ for 10-bit applications, with the full scale calibration voltage of +9.985 for unipolar applications.

SYSTEM CONSIDERATIONS

When integrating the A/D Converter into a system, consideration must be given to several factors to assure best performance. First, the analog signal to be encoded should not change more than 1/2 LSB during the encoding process; a sample-and-hold circuit should be used if required to hold changes to 1/2 LSB or preferably, much less (Figure 11). Second, proper grounding of the system is essential to prevent errors due to system noise. The preferred method is to connect the analog signal ground and digital power ground together at only one point, right at the A/D's connector. This will insure that digital ground currents do not flow in the analog ground line.

LOWER POWER CONSUMPTION

Power consumption may easily be reduced from 935mW maximum to about 310mW with two minor design changes. The D/A and comparator power supplies can be reduced from ±15 volts to ±6 volts and low power TTL AM25LO2PC logic function may be specified. Digital output fanout is reduced to three standard TTL loads. The value of R1 must also be lowered accordingly to maintain the same +1/2 LSB bias current to the sum node.

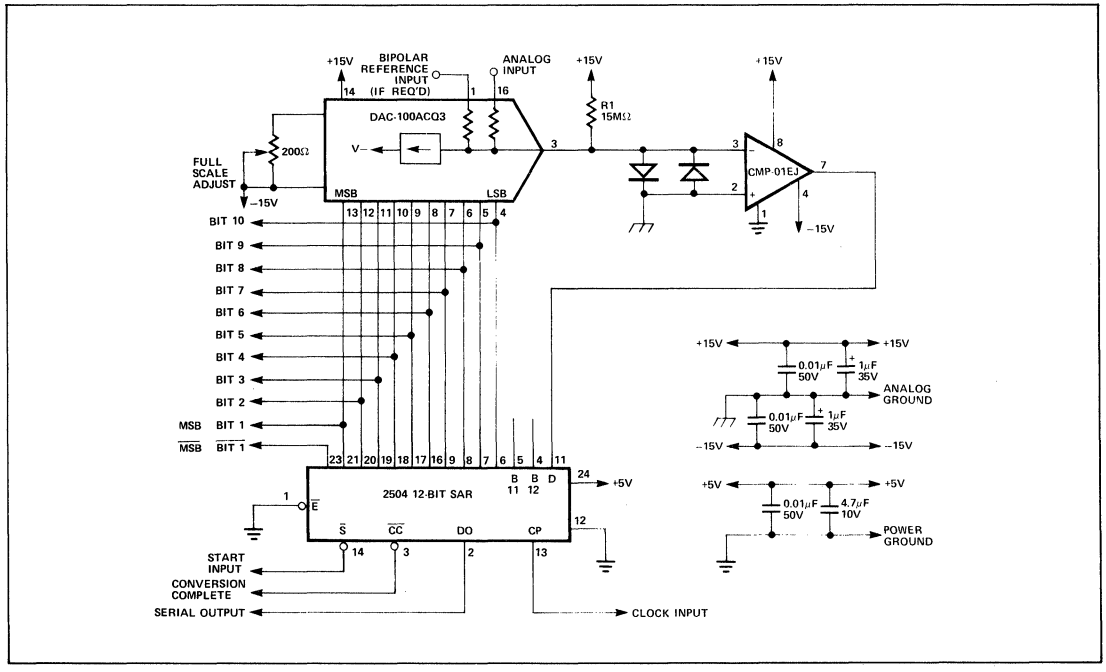


Figure 10. Complete 10-Bit A/D Schematic

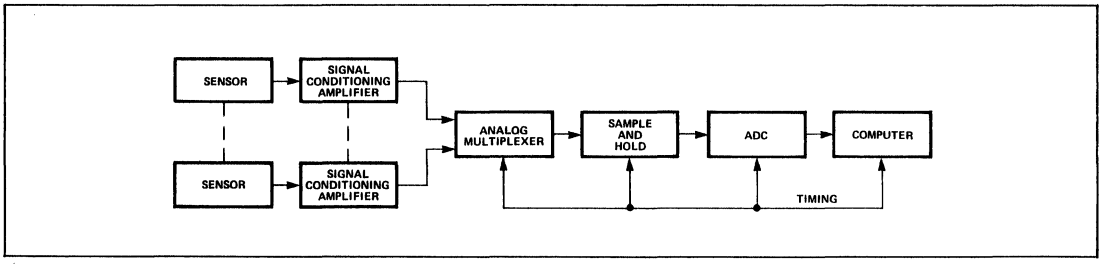


Figure 11. Typical Multiplexed Data Acquisition System

MILITARY TEMPERATURE RANGE OPERATION

Operation over wider temperature ranges can be obtained by simply specifying appropriate temperature range components. The simplicity of the three IC designs coupled with the compatibility of the devices with MIL-STD-883A processing assures high reliability in military applications.

CONCLUSION

Extremely compact, rugged, low power consumption successive approximation A/D converters are made possible by combining three ICs: PMI's DAC-100 Series 10-bit D/A, CMP-01 comparator, and a Successive Approximation Register. This simple, low cost design opens up new applications such as one A/D per channel operation in data acquisition systems.

PARTS LIST FOR 8-BIT A/D CONVERTER

±0.3% maximum nonlinearity, FS tempco 120ppm/°C	
1	DAC-100DDQ3 (or Q4)
1	CMP-01CJ
1	AMP2502PC (Advanced Micro Devices) or Equivalent
1	Pot-200Ω Bourns #3006P-1-201
1	4.7μF CAP-Mallory #TDC475M010EL
2	1.0μF CAP-Mallory #TDC105M035EL
2	Diode, 1N4148
3	.01μF CAP-Centralab #CK-103
1	PC Board
1	Resistor 3.9MΩ 5% 1/4W
For ±0.2% maximum nonlinearity, FS tempco 60ppm/°C use DAC-100CCQ3 (or Q4)	

PARTS LIST FOR 10-BIT A/D CONVERTER

±0.1% maximum nonlinearity, FS tempco 60ppm/°C	
1	DAC-100BCQ3 (or Q4)
1	CMP-01EJ
1	AM2504PC (Advanced Micro Devices) or Equivalent
1	Pot-200Ω Bourns #3006P-1-201
1	4.7μF CAP-Mallory #TDC475M010EL
2	1.0μF CAP-Mallory #TDC105M035EL
2	Diode, 1N4148
3	.01μF CAP-Centralab #CK-103
1	PC Board
1	Resistor 15MΩ 5% 1/4W
For ±0.05% maximum nonlinearity, FS tempco 60ppm/°C use DAC-100ACQ3 (or Q4)	

APPLICATION NOTE 12

TEMPERATURE MEASUREMENT METHOD BASED ON MATCHED TRANSISTOR PAIR REQUIRES NO REFERENCE

By Jim Simmons and Donn Soderquist

Most remote temperature measurements are made with thermistors or thermocouples as the sensing elements. This article shows how the function can be accomplished by using the intrinsic properties of a well-matched monolithic transistor pair. The method is attractive for its simplicity, accuracy, and long-term stability. Of particular utility is the fact the output is inherently linear and is directly useable without special linearizing circuitry.

Thermocouples can require both linearizing circuitry and reference junction making them difficult to apply. Linear outputs may be achieved with composite thermistor-resistor networks but long-term stability is diffult to predict. Ordinary silicon diodes, when operated as temperature sensors, require constant current drive and extensive calibration. The matched transistor pair method has none of these drawbacks.

BASIC THEORY

Matched transistor pairs have predictable relationships which make temperature measurements possible. To develop these relationships, let us consider the fundamental properties of a single transistor. The well known relationship between collector current and base-emitter voltage for a single transistor is:

$$1.\ V_{BE} = \frac{kT}{q} \log_e \left(\frac{I_C}{I_S}\right) \text{ provided } I_C/I_S >> 1$$

where

k = Boltzmann's constant = 1.38 x 10^{-23} joules/°K
T = absolute temperature, °K
q = charge of an electron = 1.6 x 10^{-19} coulomb
I_S = theoretical reverse-saturation current ≅ 1.87 x 10^{-14}A
I_C = collector current

Consider the difference in base-emitter voltages, ΔV_{BE}, of two transistors operated at the same temperature:

$$2.\ \Delta V_{BE} = \frac{kT}{q} \log_e \left(\frac{I_{C1}}{I_{S1}}\right) - \frac{kT}{q} \log_e \left(\frac{I_{C2}}{I_{S2}}\right)$$

This expression may be rewritten to:

$$3.\ \Delta V_{BE} = \frac{kT}{q} \log_e \left(\frac{I_{C1}}{I_{C2}}\right) - \frac{kT}{q} \log_e \left(\frac{I_{S1}}{I_{S2}}\right)$$

The values of I_{S1} and I_{S2} are a strong function of processing and geometry variables, and are very nearly identical in a well-matched monolithic transistor pair. As I_{S1} and I_{S2} approach equality ($\log_e 1 = 0$), the second term can be eliminated. For an ideal pair the expression becomes:

$$4.\ \Delta V_{BE} = \frac{kT}{q} \log_e \left(\frac{I_{C1}}{I_{C2}}\right)$$

Note that if the ratio of collector currents I_{C1} to I_{C2} is made constant, ΔV_{BE} will be proportional to absolute temperature alone. No absolute values of current are required because only a stable current ratio must be maintained. For a fixed ratio of 2 to 1 the expression is:

$$5.\ \frac{\Delta V_{BE}}{\Delta T} = 5.973 \times 10^{-5} = 59.73 \mu V/°K$$

This predictable differential base-emitter voltage relationship allows a matched transistor pair to be used as a temperature sensor. A complete temperature measuring system can be built with a matched pair, two constant current sources, and a differential amplifier as shown in Figure 1.

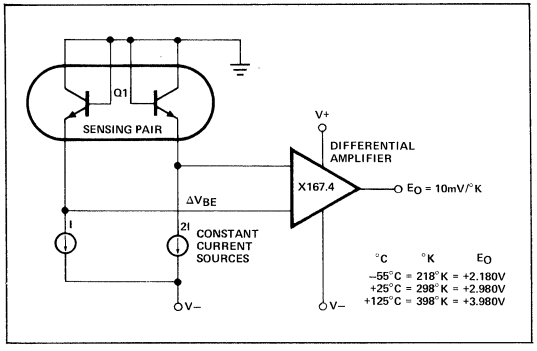


Figure 1. Basic Temperature Sensor

SYSTEM DESIGN CONSIDERATIONS

To illustrate this concept, let us design a system to provide accurate temperature mesurement over the range of −55 °C to +125 °C (218 °K to 398 °K). Other goals are: ease of calibration, long-term stability, standard resistor values, and small physical size. In addition, the system should be capable of operation with the sensing matched pair located up to 100 feet from the current sources and differential amplifier. A system achieving these goals is detailed below.

SENSING MATCHED PAIR

Any mismatch will cause performance to deviate from the ideal case shown in Equation 4, the most critical parameter

being average offset voltage drift (TCV_{OS}). This quantity, multiplied by the largest temperature excursion (100°K) and the differential amplifier gain (167.4), will be the output error and is shown in Table 1 for typical TCV_{OS} specifications.

Clearly, system accuracy is directly related to the degree of matching of the sensing pair. A Precision Monolithics MAT-01H with its typical TCV_{OS} of 0.15V/°C was specified in order to minimize this error factor.

Table 1.

TCV_{OS}	Error in °K over 100°
0.15μV/°C	0.251°K
0.5μV/°C	0.837°K
1.0μV/°C	1.67°K
2.0μV/°C	3.34°K
2.5μV/°C	4.19°K
5.0μV/°C	8.37°K
10μV/°C	16.7°K

CONSTANT CURRENT SOURCES

Two currents of a precise 2 to 1 ratio are provided by this section. Several considerations make 5μA and 10μA good choices as nominal operating currents for I_{C2} and I_{C1} respectively. Most monolithic matched transistor pairs are specified at $I_C = 10\mu A$. Input bias currents associated with the differential amplifier can be ignored because 5μA is three orders of magnitude larger. Resistor values are small enough to keep physical size and cost reasonable. Finally, the quiescent currents do not develop significant voltage drops in 100 feet of ordinary shielded-pair cable.

The two most important current source transistor matching characteristics required are h_{FE} and V_{OS} long-term stability, assuming that this part of the circuit is not subjected to wide temperature variations. If the system is to have good power supply and ripple rejection, the h_{FE} match must be maintained over a range of operating currents. These characteristics will insure a constant 2 to 1 ratio of I_{C1} to I_{C2} is maintained.

With the circuit as shown in Figure 2, the total system has measured power supply rejection of 1°K/volt. Once calibrated, long-term changes in V_{OS} will change the current ratio, and, in turn, the output. A Precision Monlithics MAT-01GH ws selected for Q2 because it has the desired combination of specified long-term stability (0.2μV/month) and close h_{FE} matching, typically 1%.

DIFFERENTIAL AMPLIFIER

The sensing pair and constant current sources provide a differential voltage (ΔV_{BE}) which is directly proportional to absolute temperature. The amplifier must acquire this voltage difference in the presence of common mode voltages, amplify it by 167.4, and change it from a differential to a single-ended signal. Excellent performance is obtained using the circuit of Figure 3.

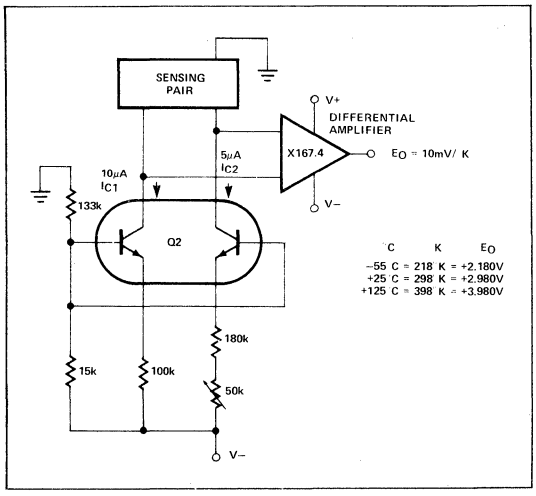


Figure 2. Basic Temperature Sensor

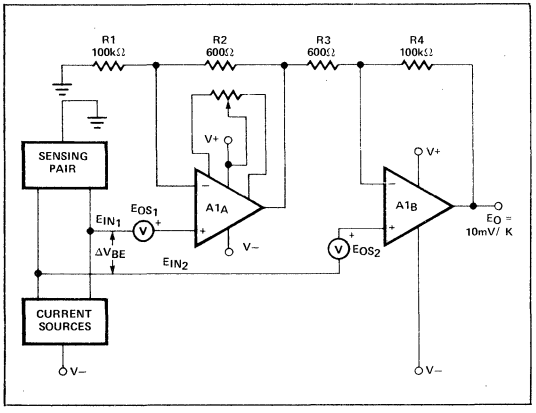


Figure 3. Differential Amplifier Design

The two op-amp differential amplifier configuration is widely used wherever high input impedance and fixed gain are required. This amplifier uses a dual matched instrumentation operational amplifier designed and specified for differential applications, the Precision Monolithics OP-01CY.

GENERAL DESIGN CONSIDERATIONS

Assuming ideal amplifiers, the expression for output voltage is:

$$6.\ E_o = \left[E_{IN_1}\left(1 + \frac{R2}{R1}\right) - \frac{R4}{R3}\right] + E_{IN_2}\left(\frac{R4}{R3} + 1\right)$$

With ideal resistors this simplifies to:

$$7.\ E_o = (E_{IN_2} - E_{IN_1})\left(\frac{R4}{R3} + 1\right) \text{ provided } \frac{R1}{R2} = \frac{R4}{R3}$$

In this system, $(E_{IN1} - E_{IN2})$ has been previously defined as ΔV_{BE}. The actual expression for E_o may be written as:

8. $E_o = \Delta V_{BE} \left(\frac{R4}{R3} + 1\right)$ but $\frac{\Delta V_{BE}}{\Delta T} = 5.973 \times 10^{-5}$ (Eq. 5)

Therefore, the ideal overall system output expression is:

9. $E_o = (5.973 \times 10^{-5}) \left(\frac{R4}{R3} + 1\right) T$

COMMON MODE REJECTION

At 25°C (298°K), ΔV_{BE} is 17.8mV while the individual sensing pair base-emitter voltages are about 520mV. There is a need to reject the 520mV common mode input voltage while accurately amplifying the differential input voltage, ΔV_{BE}. At −55°C (218°K), the situation becomes more difficult with ΔV_{Be} of 13mV and 396mV of common mode voltage. Keeping in mind that this is a best case disregarding any extraneous cable pickup, it can be observed that the requirement for high common mode rejection is very real.

Because the dual op amp has a specified 117dB common mode rejection ratio match, the ability to reject common mode inputs becomes primarily a function of resistor ratio matching. This device eliminates the need for special op amp selections in this stringent differential amplifier application.

Resistor selections can be avoided by using readily available 0.01% tolerance precision resistors, resulting in a worst-case ratio match of 0.04%. This ratio match, a combination with the dual op amp's performance, results in greater than 100dB common mode rejection at the amplifier's input.

Long term stability of the resistors must approach the initial ratio match or degradation of common mode rejection can occur over time. The resistors chosen are specified at ±50ppm/3 years and ±5ppm/°C thereby assuring stability versus time and temperature.

DIFFERENTIAL OFFSET VOLTAGE

The amplifier's differential input offset voltage (E_{OS1} — E_{OS2}) will be the major error factor. If the individual input offset voltages are of equal magnitude and polarity they appear as a common mode input and are rejected. The OP-10CY provides the additional convenience that only a single

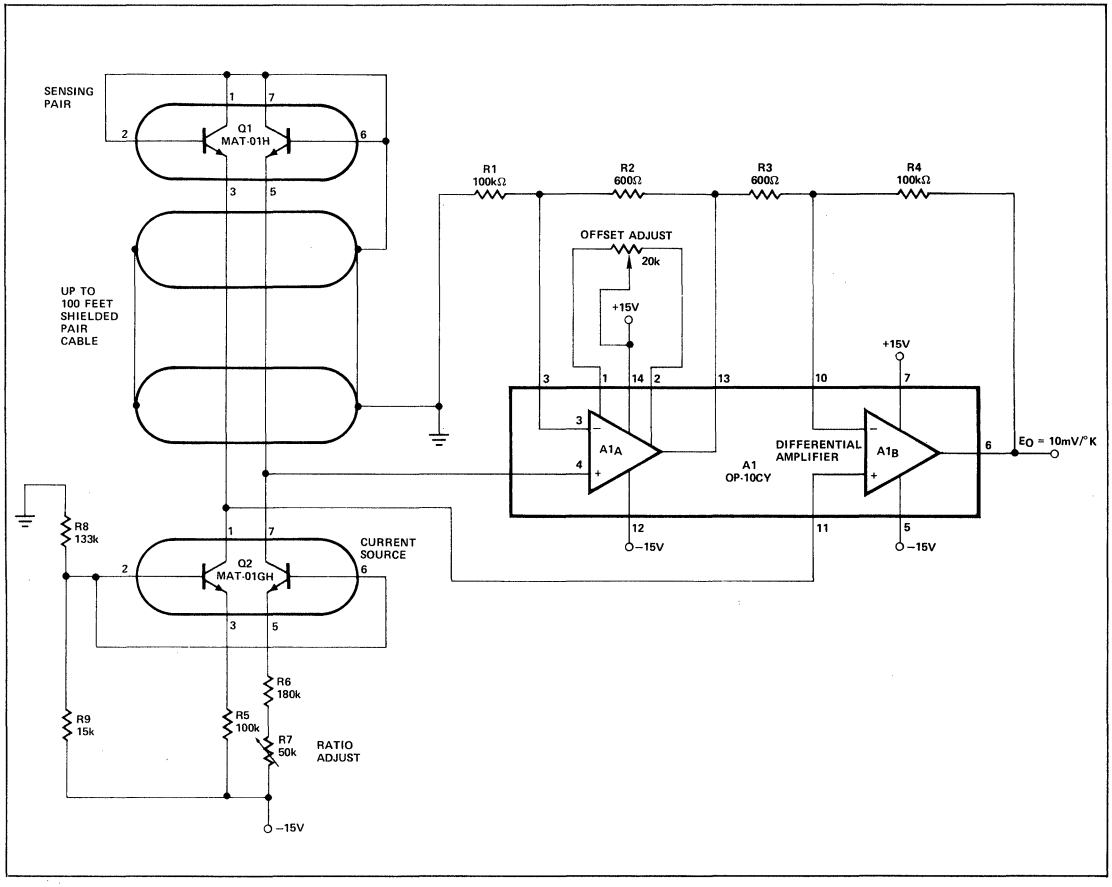


Figure 4. Complete Schematic

offset adjustment is necessary to provide the required ΔV_{OS} match; this adjustment at the same time provides a minimum $TC\Delta V_{OS}$ of the differential amplifier.

INSTALLATION

Ordinary shielded pair cable, with #22 or larger conductors, is satisfactory for most remote temperature measuring applications. Good thermal conductivity from the sensing pair's case to the environment being measured is essential to avoid incorrect readings. When this circuit is used for temperature control, thermally-conductive epoxy works especially well in attaching the sensing pair to the device being controlled.

CALIBRATION PROCEDURE

This is an easy two-step procedure. First, short the differential amplifier inputs and adjust the offset potentiometer until the output reads zero volts. Remove the input short. Second, with the sensing pair at a known temperature (room temperature is suitable), adjust the ratio potentiometer for a correct differential amplifier output reading. Having the capability of room temperature calibration makes this circuit much more convenient to calibrate than other types.

OVERALL ACCURACY

This circuit, with the components as specified, is capable of ±1°k accuracy over the full military temperature range of −55°C to +125°C (218°k to 398°k). Optimum accuracy is obtained with the differential amplifier and constant current sources in a controlled environment remote from the sensing pair. Maintenance of high accuracy over long periods of time is achieved because all components used in this design have long-term stability specified.

APPLICATIONS

The circuit's output, as measured by a 10-volt full scale digital panel meter, makes a digital thermometer. DPMs with BCD outputs may be used in applications requiring simultaneous direct readout and digital outputs for control purposes.

CONCLUSIONS

Accurate temperature measurement and control sysems are easily and economically built using the predictable characteristics of modern monolithic matched transistor pairs. This method offers long-term stability, excellent linearity, simple calibration, and high performance in severe environments.

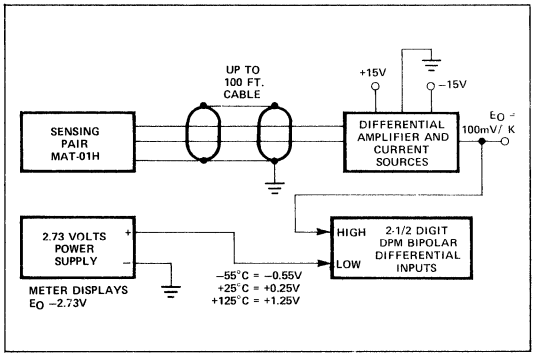


Figure 6. Digital Thermometer with Readout in °C

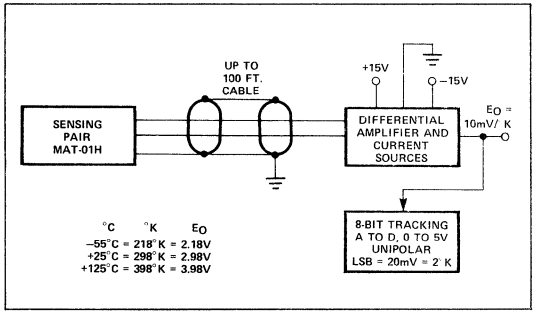


Figure 7. Binary-Coded Temperature Readings with 2° Resolution

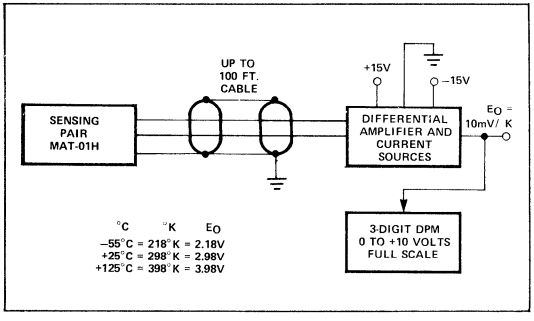


Figure 5. Basic Digital Thermometer with Readout in Degrees Kelvin (°k)

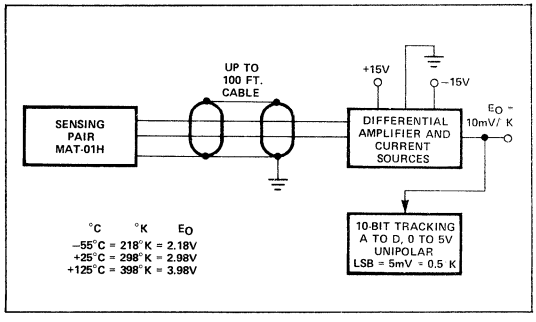


Figure 8. Binary-Coded Temperature Readings with 5° Resolution

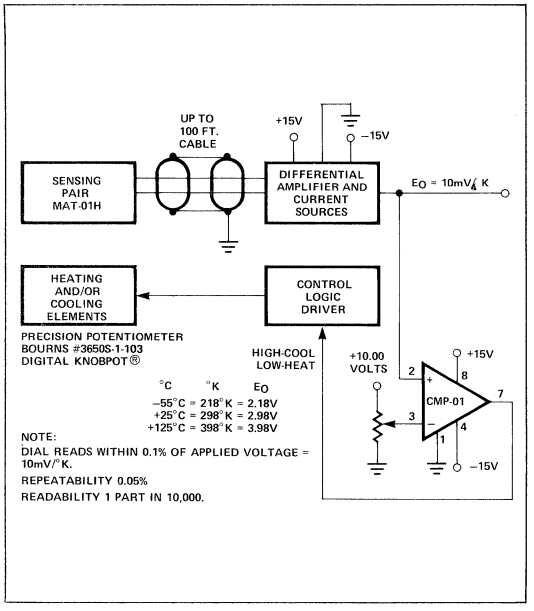


Figure 9. Temperature Controller — Digital Dial Controlled

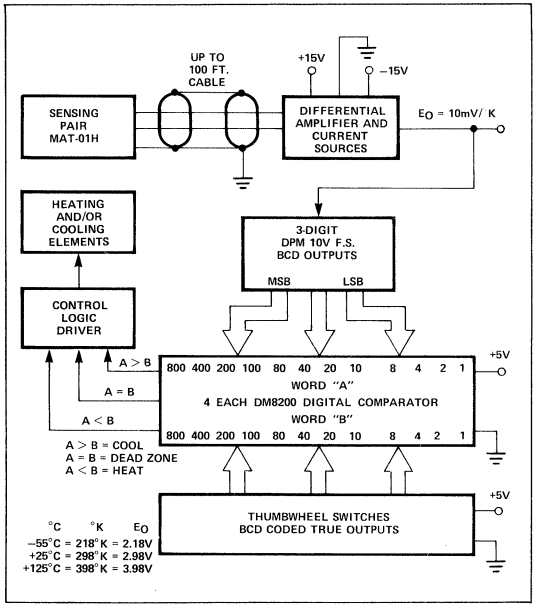


Figure 10. Temperature Controller — Digital Thermometer

PARTS LIST

1.	Q1	MAT-01H, Matched Transistor Pair Precision Monolithics, Inc.
2.	Q2	MAT-01GH, Matched Transistor Pair Precision Monolithics, Inc.
3.	A1	OP-10CY, Dual Instrumentation Op Amp Precision Monolithics, Inc.
4.	R1, R4	Resistor, 600Ω, 0.01% General Resistance Econister
5.	R2, R3	Resistor, 100kΩ, 0.01% General Resistance Econister
6.	R5	Resistor, 100kΩ, 0.1% General Resistance Econistor
7.	R6	Resistor, 180kΩ, 0.1% General Resistance Econistor
8.	R7	Potentiometer, 50kΩ, 10% Bourns #3006P-1-503
9.	R8	Resistor, 133kΩ, 1% RN55C1333F
10.	R9	Resistor, 15kΩ, 1% RN55C1502F
11.	R10	Potentiometer, 20kΩ, 10% Bourns #3006P-1-203

APPLICATION NOTE 13

THE OP-07 ULTRA-LOW OFFSET VOLTAGE OP AMP — A BIPOLAR OP AMP THAT CHALLENGES CHOPPERS, ELIMINATES NULLING

By Donn Soderquist and George Erdi

The OP-07, a new bipolar-input monolithic operational amplifier, provides chopper-stabilized amplifier performance at bipolar prices. Input offset voltage, the major error contribution in most designs, is reduced to a maximum of 25μV by a new computer-controlled on-chip trimming technique. Such low V_{OS} eliminates the nulling potentiometer requirement of most op amp circuits, greatly reducing system complexity while improving reliability. A description of this amplifier's design and performance is given, followed by an applications section showing how superior input specifications can simplify high-accuracy analog design.

IMPORTANCE OF LOW INPUT OFFSET VOLTAGE

In many applications, the initial input offset voltage of operational amplifiers causes more inaccuracy than all other error factors combined. The other significant error parameters, such as bias and offset currents, open-loop gain, and common mode rejection, have come closer to theoretically ideal performance than has V_{OS}. For this reason, most operational amplifiers, monolithic and modular, are provided with terminals to allow the user to adjust this offset voltage to zero — a costly and potentially unreliable procedure, which in many cases degrades performance of TCV_{OS}. Monolithic op amp manufacturers have constantly strived for improvement in V_{OS} from μA709 and μA741 at 5000μV, to the μA725 at 1000μV in 1969, to the OP-05A at 150μV in 1972. The OP-07A at 25μV maximum V_{OS} is a significant milestone in monolithic bipolar operational amplifier design.

Temperature stability is also important since the benefits of low initial V_{OS} are quickly lost if a small change in operating temperature causes substantial V_{OS} drift. Good long-term V_{OS} stability is required to avoid periodic re-calibrations and degradation of system performance over time. Until now, chopper-stabilized or externally-nulled monolithic op amps have been the usual choices despite the disadvantages of high noise and/or external components. The OP-07 design achieves the desired combination of low V_{OS}, low TCV_{OS}, long-term V_{OS} stability, low bias current, and low noise. It provides performance comparable to chopper-stabilized amplifiers with the further advantages of freedom from chopper-frequency noise and external component requirements.

LOW V_{OS} AMPLIFIERS

Some of the more common methods for optimizing V_{OS} performance have been chopper-stabilized amplifiers, bipolar amplifiers nulled to zero initial V_{OS}, and combinational amplifiers constructed with a matched transistor pair followed by a standard bipolar op amp. Each approach to the V_{OS} problem is a compromise between allowable error, reliability and price. The purpose of this discussion is to show how the OP-07 provides superior performance, higher reliability, and reduced size at a lower overall cost.

CHOPPER-STABILIZED AMPLIFIERS

In the past, designers have been forced to use chopper-stabilized amplifiers in applications requiring less than 100μV initial V_{OS}. The OP-07 is a cost-effective alternative, providing chopper-type performance with 741 ease-of-application. Use of a bipolar input op amp eliminates the usual chopper problems of high noise, large physical size, and limited common-mode input voltage range.

Low initial offset voltage specifications lose their significance if noise and long-term drift are of the same magnitude. Although the monolithic choppers have lower average input bias currents, the chopping action produces very large spikes in the input currents and prevents their use with large or unbalanced source resistors. For this reason, most chopper manufacturers carefully avoid specifying noise currents above 10Hz. The input bias current, remains below 4nA over the full military temperature range, and being free from chopper spikes, enables use in high impedance circuitry.

Another chopper-related problem is that input signals often interact with chopping frequency components and their harmonics. This interaction can cause errors due to intermodulation, producing slowly varying offset voltages usually below 20Hz. Chopper frequency switching transients can also cause electromagnetic interference frequently requiring special shielding and input guarding methods to protect adjacent circuitry. Modular choppers can have input overload recovery times as high as five seconds and require up to ten external components to effectively eliminate this problem. Monolithic choppers require expensive, large external components, such as two 0.1μF teflon dielectric capacitors, for wide temperature range operation. These problems are eliminated by the OP-07.

NULLED BIPOLAR AMPLIFIERS

The major disadvantage of most high performance bipolar op amps is that their high initial V_{OS} must be adjusted to zero with a nulling potentiometer or trimming resistors. In certain amplifiers, this is also a requirement in order to optimize TCV_{OS} performance. Selected or adjusted components re-

quire special test labor, take up much-needed space, decrease reliability, and add to system complexity. "Maintainability" is poor — field replacements or renulling due to long-term V_{OS} and resistance changes must be performed by a skilled technician with sophisticated test equipment. Use of an internally-nulled OP-07 avoids all of these problems since it is a complete, fully-interchangeable device, and does not require zeroing to optimize TCV_{OS}.

COMBINATIONAL AMPLIFIERS

This is one of the oldest methods, usually implemented with a heated-substrate matched transistor pair in a differential-input gain stage followed by a conventional op amp. This method requires four precision resistors, a nulling potentiometer, external frequency compensation, and up to 360mW of heater power. TCV_{OS} is only about $2\mu V/°C$ despite the temperature control for the input pair. The OP-07 provides improved performance in all parameters as well as lower cost, elimination of calibration labor, lower noise and a tremendous reduction in total power consumption.

CIRCUIT DESCRIPTION

The three-stage design concept of previous Precision Monolithics' instrumentation quality op amps was retained for the OP-07 because, using this design, nulling of V_{OS} simultaneously optimizes TCV_{OS}. (This relationship is not the case for the more commonly used two-stage "741"-type amplifier.) There are additional advantages of high gain, low noise, and predictable long-term stability. Low input bias current is achieved by bias current cancellation; i.e., currents are generated equal in magnitude but opposite in direction to the base currents of the input transistors Q1 and Q2 in the simplified schematic of Figure 1.

The symmetry of the input stage allows examination of only one side to demonstrate bias current cancellation. Base drive for the input transistor, Q1, is provided by Q5 and the external circuitry; the difference between Q5's collector current and Q1's base current being the input bias current. Q1 and Q3 are h_{FE}-matched transistors operating at similar collector currents and, therefore, the base current of Q1 is approximately equal to the base current of Q3. Q3's base current is supplied by Q7, a diode-connected PNP transistor closely matched to Q5. Together Q5 and Q7 form a current mirror (turnaround) and the collector current of Q5 will equal the base current of Q3. In this manner almost all base current for Q1 is provided by Q5 and precise bias current cancellation is achieved. Careful design has enabled this cancellation to be effective over a wide temperature range. (Figure 2.)

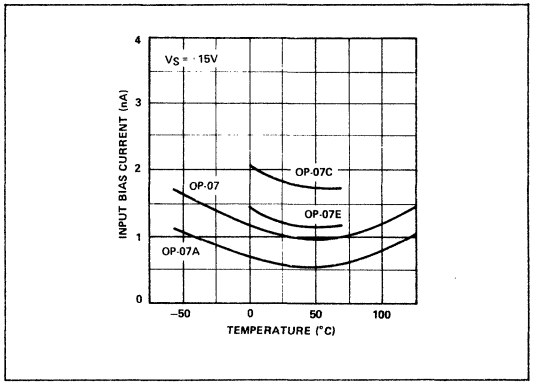


Figure 2. Input Bias Current vs Temperature

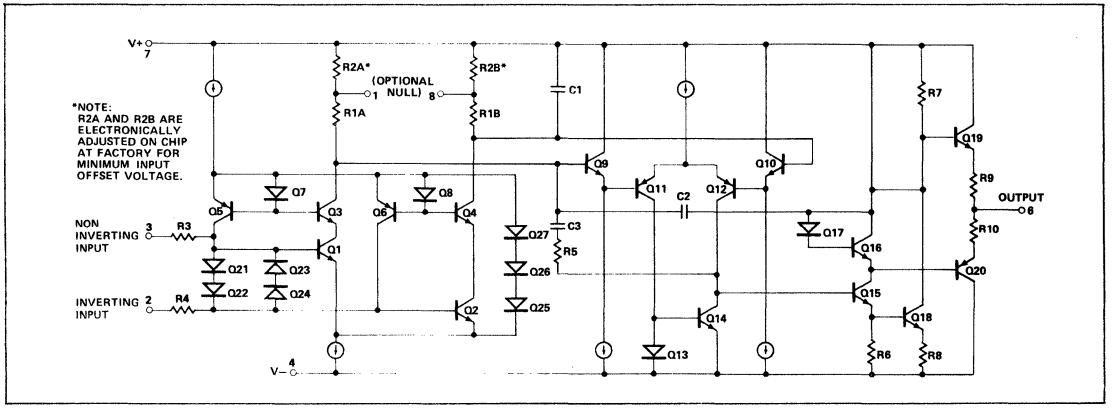


Figure 1. OP-07 Simplified Schematic

INPUT STAGE

To achieve lowest initial V_{OS}, TCV_{OS} and noise, a simple differential input pair, Q1 and Q2, was chosen. V_{OS} nulling resistors R2A and R2B are electronically adjusted and will be covered separately in the trimming discussion. R3 and R4, in conjunction with Q21-Q24, provide input differential overvoltage protection.

FOLLOWING STAGES

The first stage output is buffered by emitter followers Q9 and Q10, and applied to a high-gain differential stage, Q11 and Q12. Its output, the junction of Q12, Q14, Q15, and R5, drives a short-circuit-protected complementary emitter follower power output stage.

COMPENSATION

Frequency compensation of the OP-07 is accompished using three capacitors. Feedforward capacitor C3 bypasses the second stage lateral pnp's at high frequencies and, therefore, the excessive phase-shift normally associated with these transistors is circumvented. The dominant pole of the amplifier is set by C_2 which feed back around the second and driver stages and rolls off the open loop response at 20dB decade. The presence of C_1 ensures that the high frequency signal path is single-ended by rolling off the response of one side of the input stage. The total internal capacitance on the 100 X 53 mil chip is 210pF, a remarkable amount for a monolithic device.

LAYOUT

The circuit layout has thermal symmetry, a concept which has been used quite extensively on precision amplifier designs since its inception in 1969.[1] Variations in power dissipation in the driver and output stages, and the resultant thermal gradients affect the critical input transistors identically, thereby preventing offset voltage changes at the input.

INTERNAL NULLING TECHNIQUE

To understand the nulling technique some fundamental relationships should be examined using the equivalent circuit of Figure 3. (Errors caused by the second stage are effectively divided by the first stage gain and will be neglected in this discussion.) V_{OS} is defined as the voltage which must be applied between the input terminals to obtain zero voltage at the amplifier's output. Referring to Figure 3:

1. $V_{OS} = V_{be1} - V_{be2}$, V_{OUT} = zero

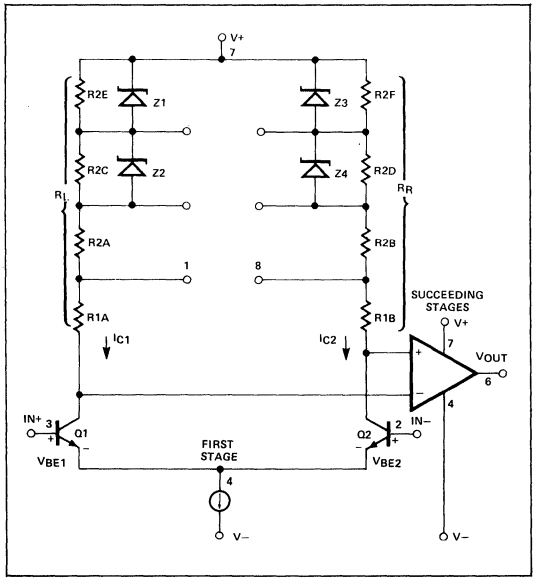


Figure 3. Offset Nulling Circuit

[1] **Editor's note:** This concept was originally introduced by George Erdi during employment at Fairchild Semiconductor Research and Development.

With an error free second stage it may be assumed that the input transistor collectors are equal in potential.

2. $I_{C1}R_L = I_{C2}R_R$ and $\frac{I_{C1}}{I_{C2}} = \frac{R_R}{R_L}$

3. $V_{be} = \frac{kT}{q} \log_e \left(\frac{I_{C1}}{I_{S1}}\right)$, $V_{be2} = \frac{kT}{q} \log_e \left(\frac{I_{C2}}{I_{S2}}\right)$,

   Provided $I_C/I_S >> 1$.

Substituting in Equation 1:

4. $V_{OS} = \frac{kT}{q} \log_e \left(\frac{I_{C1}}{I_{S1}}\right) - \frac{kT}{q} \log_e \left(\frac{I_{C2}}{I_{S2}}\right)$

Rewriting:

5. $V_{OS} = \frac{kT}{q} \log_e \left(\frac{I_{C1}}{I_{C1}} \cdot \frac{I_{S2}}{I_{S1}}\right)$

Substituting from Equation 2:

6. $V_{OS} = \frac{kT}{q} \log_e \left(\frac{R_R}{R_L} \cdot \frac{I_{S2}}{I_{S1}}\right)$

For V_{OS} = zero:

7. $\frac{R_R}{R_L} \cdot \frac{I_{S2}}{I_{S1}} = 1$

Where:

k = Boltzmann's constant = 1.38 X 10^{-23} joules/° K

T = Absolute temperature, ° K

q = Charge of an electron = 1.6 X 10^{-19} coulomb

I_S = Theoretical reverse-saturation current

I_C = Collector Current

Therefore, by adjusting the ratio of $\frac{R_R}{R_L}$ the inherent processing-related differences in I_{S1} and I_{S2} which cause V_{be} differentials may be cancelled. Earlier amplifier designs achieved the adjustment of collector resistance by an external nulling potentiometer between Pin 1 and Pin 8 with its wiper connected to Pin 7 (Figure 1).

In the OP-07, permanent nulling is accomplished by shorting out a small percentage of R_R or R_L as determined by a computer programmed with Equation 6 and a lookup table. This is done by reading V_{OS} before trimming, comparing its magnitude and polarity with a lookup table value, and shorting out one of the normally nonconducting zener diodes. The short is created by passing a high current pulse through the selected zener, fusing its metal contacts into the silicon as shown in Figure 4. High volume production is achieved through automation, with initial device testing at wafer probe including V_{OS} trimming requiring less than one second.

Through this technique, V_{OS} of the entire "raw" OP-07 distribution can be nulled to less than 150μV, with the majority being under 75μV. Prime grade yields are high, providing adequate numbers of OP-07A devices with a V_{OS} maximum of 25μV.

PERFORMANCE

The specifications in Table 1 and curves of Figure 5 show noise, initial V_{OS}, and long-term stability performance unsurpassed by any other monolithic op amp. This device is free of

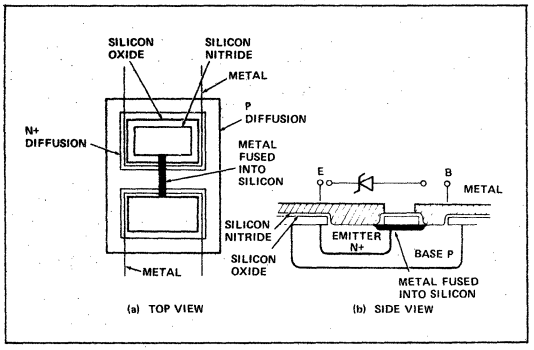


Figure 4. Short-Circuiting of Zener Diodes

Table 1. OP-07A Performance

OP-07 Performance @ V_S = ±15V, T_A = 25°C			
Parameter	**Typical**	**Min/Max**	**Units**
Offset Voltage, V_{OS}	10	25	μV
Drift with Temperature	0.2	0.6	μV/°C
Drift with Time	0.2	1.0	μV/mo
Offset Current, I_{OS}	0.3	2.0	nA
Drift with Temperature	5	25	pA/°C
Input bias current, I_B	±0.7	±2.0	nA
Noise Voltage 0.1Hz to 10Hz	0.35	0.6	μV_{p-p}
Noise Current 0.1Hz to 10Hz	14	30	pA_{p-p}
Input Resistance — Differential	80	30	MΩ
Input Resistance — Common Mode	200	—	GΩ
Common-Mode Rejection	126	110	dB
Power Supply Rejection	110	100	dB
Voltage Gain	500	300	V/mV
Slew Rate	0.25	—	V/μs
Unity Gain Bandwidth	1.2	—	MHz

the common problems of latchup, noise, compensation capacitors, and narrow power supply limitations. Power supply rejection ratio (PSRR) exceeds 100dB over the unusually wide range of ±3 to ±18 volts. Common-mode rejection is specified over a full ±13 volt input range allowing small signal amplification in high noise environments and use in inverting, non-inverting, and differential applications. The amplifier is completely self-contained — no external compensation or protection components are required. It is an excellent replacement for chopper-stabilized amplifiers where reductions in cost, noise, size, and power consumption are desired, and for monolithic op amps where elimination of the offset nulling potentiometer is desirable.

The pinout of the OP-07 allows direct replacement of 725, 108, and OP-05 types without circuit changes while 741 devices may be replaced by removal of the nulling potentiometer. HA-2900 series chopper-stabilized amplifiers may be replaced by removing the two 0.1μF capacitors and the 1500pF capacitor whenever cost or noise reductions are required. Table 2 is included to show comparative performance in wide temperature range applications.

Table 3 compares various OP-07 versions with competitive op amps and over the 0°/70°C temperature range. An absence of noise and long-term stability specifications for

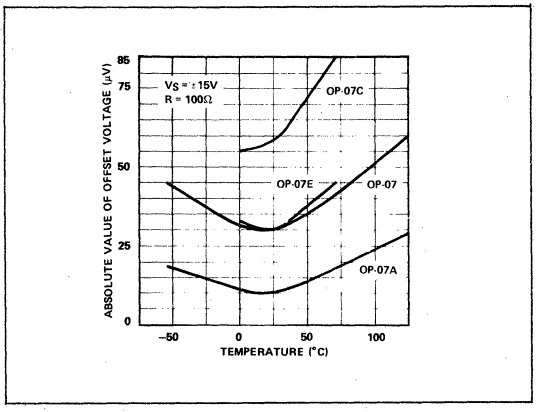


Figure 5A. Untrimmed Offset Voltage vs Temperature

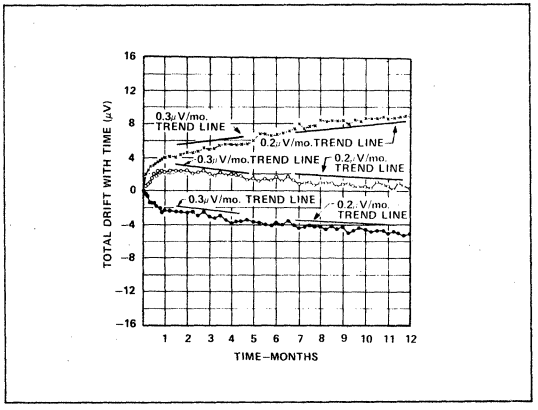


Figure 5B. Offset Voltage Stability vs Time

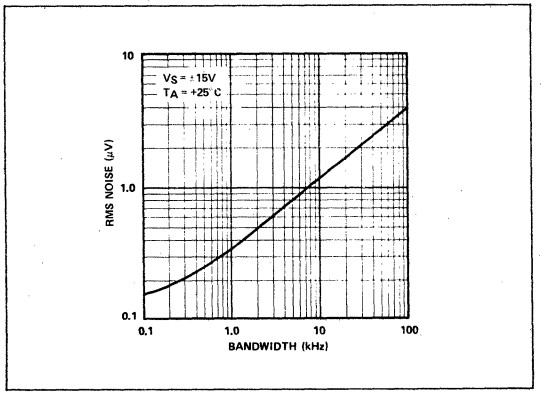


Figure 5C. Input Wideband Noise vs Bandwidth (0.1Hz to Frequency Indicated)

some amplifiers should caution potential users of possible deficiencies in those areas. This same comment would apply to "typical-only" specifications since accurate predictions of circuit performance can only be made with a fully specified device.

PERFORMANCE

The low frequency noise photograph in Figure 6A shows $0.35\mu V_{p-p}$ input voltage noise (0.1Hz to 10Hz), the best performance available in an instrumentation op amp at this writing. The wideband voltage noise comparison photograph (Figure 7A) shows relative performance of a OP-07 and a monolithic chopper in the same X100 configuration; the chopper is seen to have at least $200\mu V_{p-p}$ noise referred to the input. Clearly, low V_{OS} specifications are not very meaningful if input voltage noise is the predominant error factor.

Chopper-frequency noise is a common mode current noise occurring at the chopping frequency due to switching transients. The effect of a 500kΩ source mismatch is shown in the wideband curent noise photograph comparing a OP-07 with a monolithic chopper in the non-inverting buffer application (Figure 7B). High source impedance circuits require low

Table 2. Military Temperature Range Performance Comparison

Manufacturer's Part Number	V_{OS} Maximum −55°/+125°C	TCV_{OS} Maximum −55°/+125°C (Unnulled)	Voltage Noise Typical F = 10Hz	Current Noise Typical F = 10Hz	I_{Bias} Maximum −55°/+125°C	Long-Term Drift Typical
OP-07A	60μV	0.6μV/°C	10.3nV/√Hz	0.32pA/√Hz	4nA	0.2μV/mo
OP-07	200μV	1.3μV/°C	10.3nV/√Hz	0.32pA/√Hz	6nA	0.2μV/mo
HA-2900	60μV	0.6μV/°C	900nV/√Hz	Not Specified (Chopper)	1nA	Not Specified
OP-05A	240μV	0.9μV/°C	10.3nV/√Hz	0.32pA √Hz	4nA	0.2μV/mo
OP-05	700μV	2.0μV/°C	10.3nV/√Hz	0.32pA/√Hz	6nA	0.2μV/mo
μA725	1500μV	5.0μV/°C	15mV/√Hz	1.0pA/√Hz	200nA	Not Specified
LM108A	1000μV	5.0μV/°C	43nV/√Hz	Not Specified	3nA	Not Specified

Table 3. Commercial Temperature Range Performance Comparison

Manufacturer's Part Number		V_{OS} Maximum 0°/70°C	Long Term Drift Typical	Long Term Typical Maximum	Voltage Noise Maximum 0.1Hz to 10Hz	Voltage Noise Maximum 0.1Hz to 10Hz
OP-07A	(M)	45μV	0.2μV/mo	1.0μV/mo	$0.35\mu V_{p-p}$	$0.6\mu V_{p-p}$
OP-07	(M)	130μV	0.2μV/mo	1.0μV/mo	$0.35\mu V_{p-p}$	$0.6\mu V_{p-p}$
OP-07E	(C)	130μV	0.3μV/mo	1.5μV/mo	$0.35\mu V_{p-p}$	$0.6\mu V_{p-p}$
OP-07C	(C)	250μV	0.4μV/mo	2.0μV/mo	$0.38\mu V_{p-p}$	$0.65\mu V_{p-p}$
LM108A	(M)	725μV	Not Specified	Not Specified	Not Specified	Not Specified
HA-2900 Chopper-Stabilized	(M)	60μV	Not Specified	Not Specified	$35\mu V_{p-p}$	Not Specified
HA-2905 Chopper-Stabilized	(C)	80μV	Not Specified	Not Specified	$35\mu V_{p-p}$	Not Specified
AD504M	(C)	545μV	10μV/mo	Not Specified	Not Specified	$0.6\mu V_{p-p}$
AD508L	(C)	612μV	Not Specified	10μV/mo	$1.0\mu V_{p-p}$	Not Specified
Typical Inverting-Only Chopper Module	(C)	95μV	2.0μV/mo	Not Specified	$1.7\mu V_{p-p}$	Not Specified

M = 55°/+125°C Range Device
C = 0°/+70°C Range Device

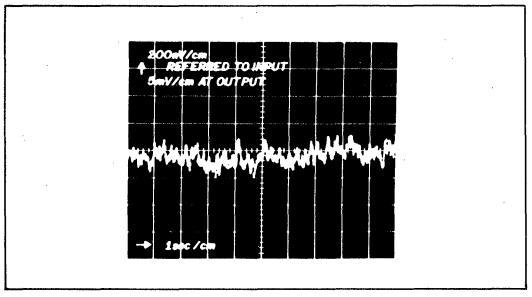


Figure 6A. Low Frequency Noise

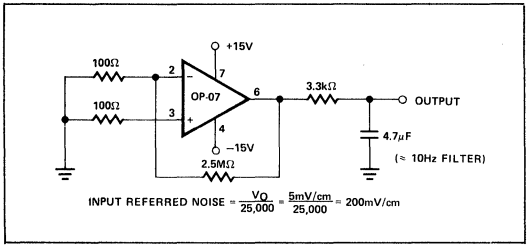


Figure 6B. Low Frequency Noise Test Circuit

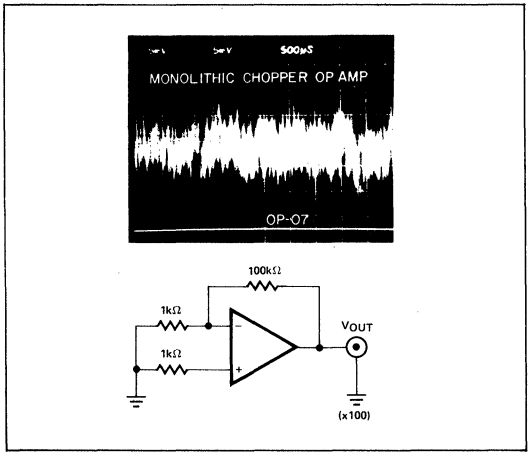


Figure 7A. Wideband Voltage Noise vs Chopper

input noise currents, which as the photograph illustrates, can be larger than input bias current with certain operational amplifiers.

LONG-TERM V_{OS} DRIFT

Input offset voltage drift over time has three components: warmup drift, first month drift, and trend line stability.

Warmup drift is a change in V_{OS} occurring in the first few minutes of operation. In order to produce high volumes of OP-07s, V_{OS} is measured 0.5 seconds after application of

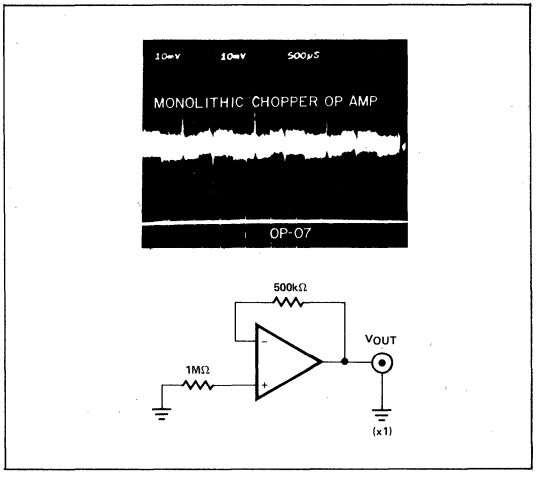


Figure 7B. Wideband Current Noise vs Chopper

power using automated test equipment. The pass limits are "guardbanded" or made small enough with respect to V_{OS} maximum specification to compensate for not having directly observed warmup drift.

The first month stability, defined as changes in V_{OS} from one hour to 30 days, is typically 2.5μV. Even with closely maintained equipment, individual measurements with time can suffer from inaccuracies on the order of a half-microvolt due to low frequency noise and slight temperature variations. Fortunately, over a large number of measurements these errors tend to integrate out, and an accurate trend line can be defined.

The trend line is defined as the drift per month averaged over the month one to month twelve period, and is generally an order of magnitude better than the first month drift (Figure 5B). Over 1.7 million device hours of testing and characterization have been logged in order to accurately specify long-term V_{OS} stability. Results indicate an average trend line drift of 0.2μV/month-outstanding stability performance for any amplifier, regardless of its technological approach.

LONG-TERM V_{OS} TESTING CONDITIONS

The deceptively simple circuit of Figure 8 is used for long-term V_{OS} stability testing. Three absolutely essential conditions must exist for accurate measurements: still air, power supply accuracy, and long-term temperature control

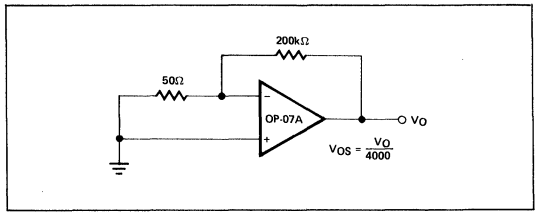


Figure 8. Long-Term Offset Voltage Test Circuit

All components, including sockets and solder joints, are enclosed in a metal box to eliminate air movement and temperature gradients. Thermoelectric error voltages may be generated if the dissimilar metal junctions formed by solder joints and socket contacts are at different temperatures. This effect is minimized by using "low thermal" solder (70% Cadmium, 30% Tin) and nonmetallic flux, such as Kester #1544, to avoid ionic contamination.

Although the power supply rejection ratio (PSRR) of the OP-07 is extremely high, nevertheless it should be considered as a potential error factor in long-term V_{OS} testing. The power supplies are verified to be at ±10mV before each set of weekly readings. This removes any possible significant errors due to the PSRR specification of 110dB (3μV/Volt).

All long-term V_{OS} testing is performed in a controlled laboratory environment of 30°C to eliminate TCV_{OS}, 0.2μV/°C, as an error possibility.

APPLICATIONS OF OP-07

HIGH STABILITY VOLTAGE REFERENCE

The simple bootstrapped voltage reference of Figure 9 provides a precise 10 volts virtually independent of changes in power supply voltage, ambient temperature, and output loading. Correct zener operating current of exactly 2mA is maintained by R1, a selected 5ppm/°C resistor, connected to the regulated output. Accuracy is primarily determined by three factors: the 5ppm/°C temperature coefficient of D1, 1ppm/°C ratio tracking of R2 and R3, and operational amplifier V_{OS} errors.

V_{OS} errors, amplified by 1.6 (A_{VCL}), appear at the output and can be significant with most monolithic amplifiers. For example: an ordinary amplifier with TCV_{OS} of 5μV/°C contributes 0.8ppm/°C of output error while the OP-07 at 0.3μV/°C (0.5ppm/°C) effectively eliminates TCV_{OS} as an error consideration.

Perhaps the most easily overlooked accuracy requirement in this and many other critical circuits is long-term V_{OS} stability. In this circuit, a 741 drifting at 100μV/mo would cause 200ppm/year of output drift — a very large amount. This type of problem is particularly troublesome in potted subassemblies where periodic recalibration is impossible. Use of the OP-07 at 1μV/mo maximum avoids this potentially troublesome condition.

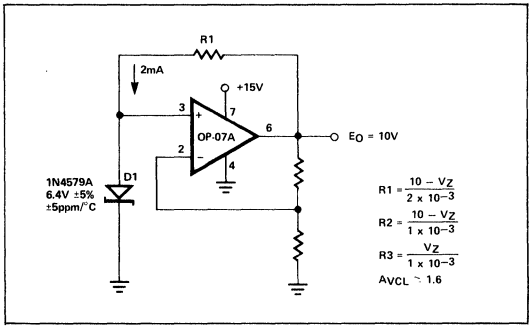


Figure 9. High Stability Voltage Reference

LARGE SIGNAL BUFFER — 0.005% WORST-CASE ACCURACY

Unity gain large-signal buffers are one of the most common applications of operational amplifiers. The low V_{OS} and high CMRR of the OP-07 provide high accuracy, and small physical size is achieved due to the complete absence of external components. Performance over the appropriate temperature range is shown for the various OP-07 selections. Note that the errors on Table 4 are absolute worst-case numbers, a combination that would be extremely unlikely in actual practice. A figure closer to expected overall performance based on the RMS sum of typical errors is also included. Typical

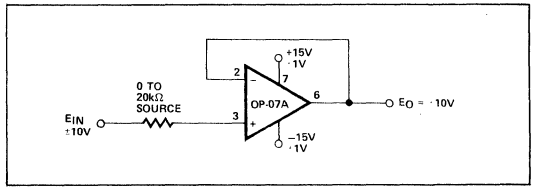


Figure 10. Large Signal Voltage Buffer

Table 4. Large Signal Voltage Buffer Error Analysis

Error Source	OP-07A −55°/+125°		OP-07 −55°/+125°		OP-07E 0°/+70°		OP-07C 0°/+70°	
	Min/Max	Typical	Min/Max	Typical	Min/Max	Typical	Min/Max	Typical
V_{OS}[1]	60μV	25μV	200μV	60μV	130μV	45μV	250μV	85μV
I_{Bias}[1]	80μV	20μV	120μV	40μV	110μV	30μV	180μV	44μV
CMRR[1]	50μV	7μV	50μV	7μV	70μV	7μV	141μV	10μV
PSRR[1]	40μV	10μV	40μV	10μV	63μV	13μV	100μV	20μV
Gain[1]	50μV	25μV	67μV	25μV	56μV	22μV	100μV	25μV
ΔV_{OS} 5 Years	60μV	12μV	60μV	12μV	90μV	18μV	120μV	24μV
Total	340μV	44μV*	537μV	78μV*	519μV	63μV*	891μV	104μV*
Percent Full Scale	0.0034%	0.0005%*	0.0054%	0.0008%*	0.0052%	0.0006%*	0.009%	0.001%*

*RMS Calculation

[1]Full operating temperature range specification.

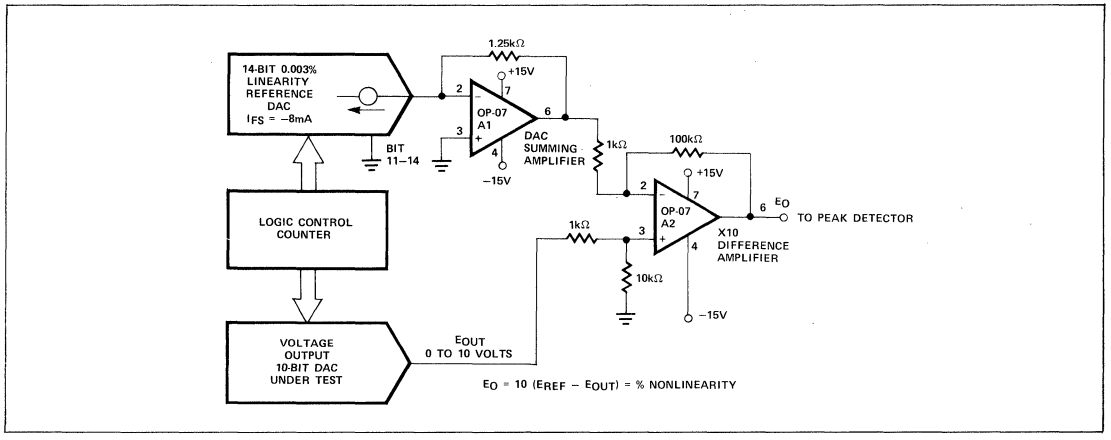


Figure 11. D/A Converter Test System

military temperature range error for the OP-07A is 44μV —far smaller than most other amplifiers' input offset voltage error alone.

CALIBRATION-FREE DAC SYSTEM

The circuit of Figure 11 is part of an automated test system used for measuring 6-bit to 10-bit DAC nonlinearity at each possible digital input code combination. It detects the largest difference between a 14-bit linear reference DAC and a unit under test, and generates an output voltage that is directly proportional to nonlinearity as a percentage of full scale.

Reference DACs are frequently supplied having current-output only, with selection of a summing amplifier left up to the user. Summing amplifier characteristics must not cause degradation of reference DAC linearity, full-scale, or zero scale performance or erroneous testing could occur. In addition, V_{OS} errors are direct zero scale output errors, so both long-term V_{OS} stability and drift over temperature are important. Using a OP-07, total E_{REF} errors due to op amp performance are estimated at less than 100μV or 0.2 LSB on a 14-bit base, permanently eliminating zero calibration while maintaining test system accuracy. Summing amplifier applications requiring higher speed should use the composite amplifier of Figure 12

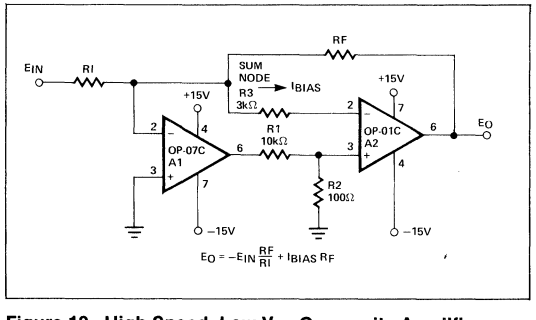


Figure 12. High Speed, Low V_{OS} Composite Amplifier

Another 0P-07 is used in the dfference amplifier for high common mode rejection and V_{OS} stability. This op amp is well-suited for critical test system circuits, providing accurate measurements, high reliability, and calibration-free operation.

COMPOSITE SUMMING AND AMPLIFIER WITH HIGH SLEW RATE AND LOW V_{OS}

The circuit configuration of Figure 12 is a method for obtaining a 18V/μs slew rate with OP-07 V_{OS} characteristics. V_{OS} of A2 (3mV) is continuously nulled by forcing the sum node to equal V_{OS} of A1 through a secondary feedback loop formed by R1, R2, A2's input stage, and R3. An error due to I_{Bias} of A2 limits practical values of feedback resistances to a maximum of 5kΩ in most applications; a fast FET input op amp could be used as A2 to reduce the circuit's bias current to approximately 2nA. The circuit is also good as a current-output DAC summing amplifier because zero scale offset adjustments are not required and high speed is preserved. Composite connections such as this are generally quite cost-effective compared to single op amps having both high slew rate and good V_{OS} specifications.

ABSOLUTE VALUE CIRCUIT WITH MINIMUM ERROR

This circuit provides precise full-wave rectification by inverting negative-polarity input voltages and operating as a unity-gain buffer for positive-polarity inputs. It is useful for conditioning inputs to unipolar A to D's, positive peak detectors, single quadrant multipliers, and magnitude-only measurement systems. A polarity indication for sign plus magnitude applications is present at the output of A1.

For a positive input, the circuit operates as two stages of inverting unity-gain amplification. As the input goes positive, the output of A1 becomes negative, turning D2 off and D1 on, placing the junction of R3 and R4 at $-E_{IN}$. V_A is at zero volts because D2 is off and only insignificant A2 bias current flows in R2. A2 operates as a second inverting unity-gain stage and E_O equals E_{IN}.

For negative inputs, the first stage gain to point V_A is -2/3 because D2 is on, D1 is off, and 1/3 of the input current, $E_{IN}/R1$, flows in R3 and R4. The second stage is operated in a

non-inverting gain of 1.5 configuration with V_A as its input, giving an over-all circuit gain of −1.

Using conventional op amps, input offset voltage is usually the predominent error factor because it is doubled and added to E_{IN}. For example, with E_{IN} of 100mV, only 0.5mV of V_{OS} will cause 1% output error. Clearly, A1 and A2 must be low V_{OS} op amps to achieve high accuracy over the full input voltage range. By using a OP-07, performance is mainly a function of resistor ratio matching and diode leakages. Gain errors due to resistor matching will typically be less than 0.3% when R2-R4 are within 0.01% of R1's value. Low leakage diodes should be used to prevent errors from reverse current flow in R2 or R3 which would appear as V_{OS} error of A2.

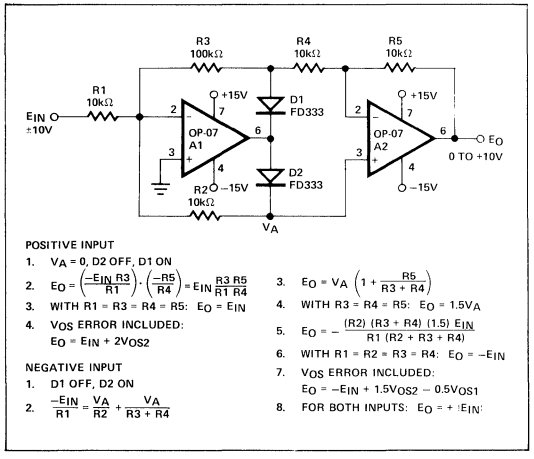


Figure 13. Precision Absolute Value Circuit

PRECISION SUMMING AMPLIFIER WITH NO ADJUSTMENTS

Figure 14 shows the basic op amp connection for analog computation, a precision summing amplifier. Analog computers use several of these stages connected in combinations to produce continuous outputs that are a function of multiple input variables. Single-stage accuracy is important because errors accumulate throughout a system and determine its over-all performance. Some analog computers require time-consuming and annoying recalibration of each stage at weekly or monthly intervals to compensate for long-term V_{OS} drift. This circuit, with 1μV to 2μV per month maximum change in V_{OS}, completely eliminates periodic calibration while insuring long-term accuracy.

Single-stage maximum full scale errors contributed by the op amp range from 0.001% for a OP-07A to 0.004% for a OP-07C. This makes resistor-related errors of ratio matching and temperature tracking the major accuracy considerations. Instrumentation quality operational amplifiers with ultra-low V_{OS} allow simple construction of high performance summing and differencing amplifiers.

INSTRUMENTATION AMPLIFIERS FOR THERMOCOUPLES

Thermocouples are very low voltage output temperature transducers requiring differential DC amplification before linearization and display. Typical full scale outputs are under 50mV with some types having as low as 5μV/°C sensitivity.

These very small input signals often have sizable common mode voltages present because the thermocouples are frequently located in high-noise industrial environments. The single op-amp instrumentation amplifier of Figure 15 has the high common mode rejection and long-term accuracy required for this stringent application.

The amplifier achieves about 100dB of common mode voltage rejection over a full ±13 volt range when the ratios of R2/R1 and R4/R3 are matched within 0.01%. R1B and R3B are usually around 1kΩ, a value large in respect to line resistance but small enough to make voltage drops from input bias currents negligible. Input voltages and V_{OS} are both amplified by 200 so V_{OS} changes, either long-term or due to temperature, can cause direct output error. For example, with a 5μV/°C thermocouple, the OP-07A holds this error factor to 0.05°C/year and 1°C for an amplifier operating temperature range of 100°C (−25°C to +75°C) — a typical industrial environment. For 0°C to 70°C applications, the low-cost OP-07C holds output error due to a change in V_{OS} below 1°C/year and 2°C over the full commercial operating temperature range.

The circuit is useful whenever small differential signals from low-impedance sources must be accurately amplified in the presence of large common mode voltages.

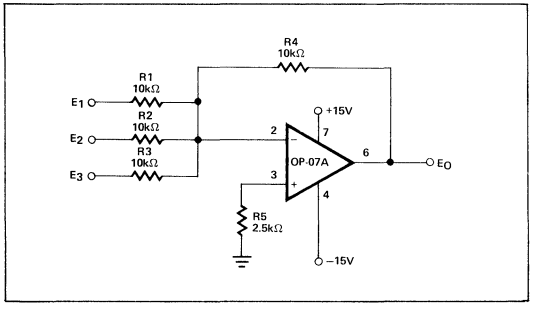


Figure 14. Adjustment-Free Precision Summing Amplifier

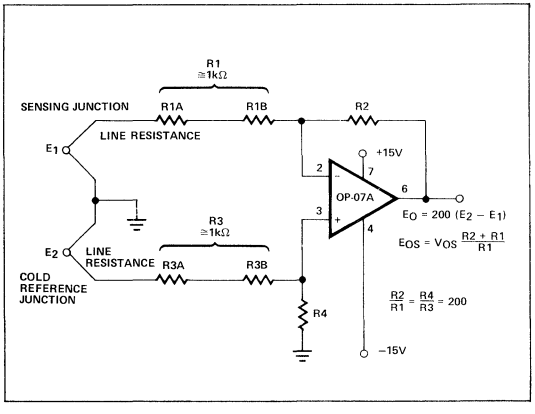


Figure 15. High Stability Thermocouple Amplifier

CONCLUSIONS

The OP-07 Ultra-Low Offset Voltage Operational Amplifier is a cost-effective monolithic alternative to the chopper-stabilized amplifier and is suitable for a wide variety of critical applications. An internal trimming procedure achieves significant improvements over previous bipolar designs in offset voltage, noise levels, and long-term stability at a moderate cost. For the first time, a complete precision IC op amp is available requiring no external components whatsoever for general application, thus increasing reliability by decreasing system complexity. The adjustment-free, fully interchangeable device allows tremendous simplification of calibration and field servicing procedures. This is a most powerful and cost-effective design tool — chopper-type performance and bipolar prices with 741 ease-of-operation.

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1. *Minimizing Offset Voltage Drift with Temperature in Monolithic Operational Amplifiers,* G. Erdi, Proceedings of the National Electronic Conference, Volume 25, 1969
2. *A Low Drift, Low Noise Monolithic Operational Amplifier for Low Level Signal Processing,* G. Erdi, Fairchild Semiconductor Application Brief #136, July 1969

APPLICATION NOTE 14

INTERFACING PRECISION MONOLITHIC'S DIGITAL-TO-ANALOG CONVERTERS WITH CMOS LOGIC

By Donn Soderquist

The rise in popularity of CMOS logic has created a demand for digital-to-analog converters with CMOS-compatible logic inputs. PMI DACs allow simple CMOS interfacing in most applications. Since interfacing is easily achieved, the proven advantages of low-cost and high speed are available to both TTL and CMOS system designers. This application note discusses interfacing methods and rules for both voltage and current output types and describes several typical CMOS system applications.

INTERFACING THE DAC-08/20

The DAC-08 design incorporates a unique logic input circuit which enables direct interface to all popular families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2μA logic input current and completely adjustable logic threshold voltage. For V– = –15V, the logic inputs may swing between –10V and +18V. This enables direct interface with +15V CMOS logic, even when the DAC-08 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V– plus (I_{REF} • 1kΩ) plus 2.5V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic control pin (Pin 1, V_{LC}). It should be noted that Pin 1 will source approximately 100μA; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when Pin 1 sees a low impedance. If Pin 1 is connected to a resistive divider, as in Figure 1, it should be bypassed to ground by a 0.1μF capacitor.

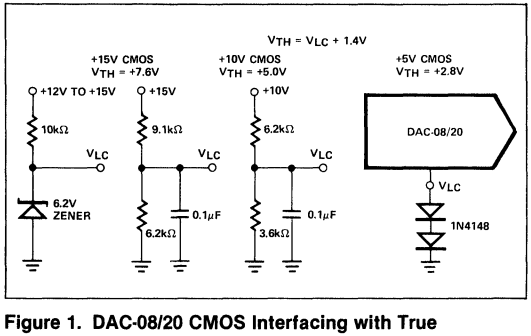


Figure 1. DAC-08/20 CMOS Interfacing with True CMOS Threshold

Revised January 1980

INTERFACING THE DAC-76/86/87/88/89

These companding D/A converters are similar to the DAC-08 in that the input logic threshold is two diode drops positive with respect to the logic control pin. However, more current flows into the logic control pin requiring active current sourcing as shown below.

V_{LC} (Pin 10) is placed as a potential which is 1.4V below the desired logic input switching threshold. However, this voltage source must be capable of sourcing and sinking a changing current at Pin 10. The negative voltage at the logic inputs must be limited to +10V with respect to V– (Pin 13).

INTERFACING THE DAC-210

Use the same circuit as in Figure 2 except connect to Digital Ground, Pin 11. Input logic threshold will be 1.4V above the potential at Pin 11.

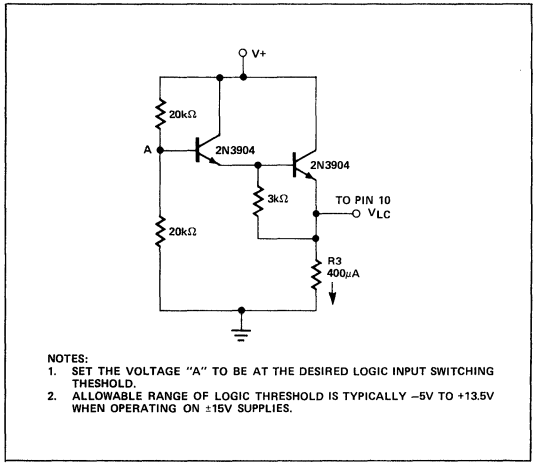


Figure 2. Interfacing Circuit For CMOS Logic Inputs

INTERFACING THE DAC-02/03/04/05/06

Five complete voltage output monolithic DACs are described in this section: the DAC-02/5 and DAC-03, 10-bit plus sign devices, and the DAC-04/06 10-bit two's complement coded converters. These DACs are well-suited to use in

CMOS systems as their complete, internal temperature-compensated references eliminate the external reference voltage requirement, a major source of power dissipation, drift, and cost in some CMOS compatible designs.

These DACs have logic input stages which require about 1μA and are capable of operation with inputs between −5 volts and V+ less 0.7 volt. This wide input voltage range allows direct CMOS interfacing in many applications, the exception being where the CMOS logic and D/A converter must use the same power supply.

In this special case, the diode should be placed in series with the CMOS driving device's V_{DD} lead as shown in Figure 3. The diode limits V_{DD} to V+ less 0.7 volt — since the output from the CMOS device cannot exceed this value, the DAC's maximum input voltage rule is satisfied. Summarizing: in all applications, these high-speed DACs require either no interfacing components, or, at most, a single inexpensive diode for full CMOS compatibility.

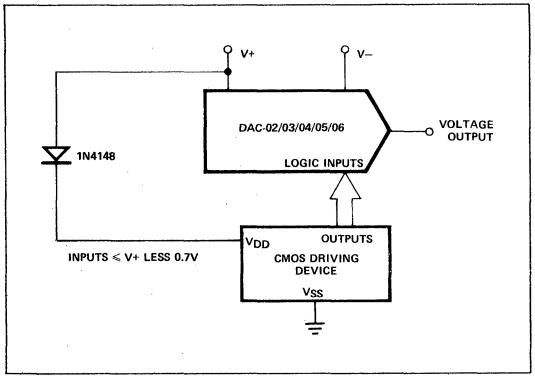


Figure 3. DAC-02/03/04/05/06 CMOS Interfacing

INTERFACING THE DAC-100 AND DAC-01

The DAC-100, a complete 10-bit monolithic fast current output DAC is available in a wide range of electrical grades and packages. This device requires only about 1μA of input current into each logic stage. Similar logic input stages are used in the DAC-01, a complete voltage output 6-bit DAC. One rule must be observed when interfacing these DACs with CMOS inputs: logic input voltages should not exceed 6.5 volts or V+, whichever is smaller. To provide an understanding of this rule, it is necessary to discuss the logic input stage design.

DAC-100 LOGIC INPUT STAGE DESIGN

For simplicity, only one of the ten identical input circuits is shown in Figure 4. The DAC-100 uses a fast current-steering technique that switches a bit-weighted current between the positive supply (V+) and the analog output, which is usually constrained to be at zero volts (virtual ground) by an external summing amplifier.

Switching is accomplished by forward biasing Q4, a diode-connected transistor, for the bit "ON" condition and back

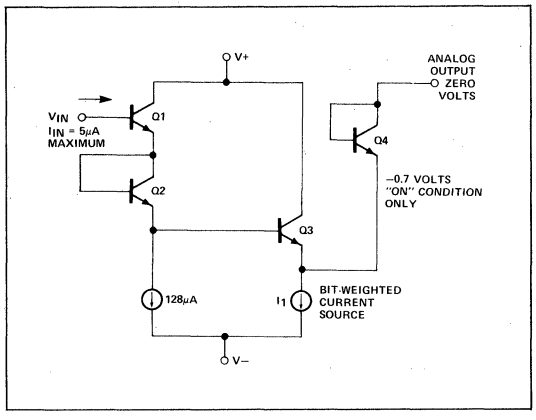


Figure 4. DAC-100 Logic Input Stage

biasing Q4 in the "OFF" condition. For the "ON" condition ($V_{IN} \leq 0.7$ volts), Q3 is "OFF" — all of the bit-weighted current, I_1, flows from the analog output through Q4 and ultimately to V−. In the "OFF" condition ($V_{IN} \leq 2.1$ volts), Q3 is "ON", Q4 is back biased, and the bit-weighted current is sourced from the positive power supply instead of the analog output.

If V_{IN} is too high, Q4's emitter-base junction will experience reverse breakdown and a fault condition will occur. Equation 1 describes this condition:

1. $BV_{IH} = V_{BE1} + V_{BE2} + V_{BE3} + BV_{EB4} \cong 7.7$ volts

Using this relationship, it can be seen that a conservative input voltage limit would be around 6.5 volts. When the 6.5V input limited is observed, DAC-100 operation with CMOS inputs is easily achieved as demonstrated in the following applications section.

CMOS COMPATIBLE OPERATION OF DAC-100 WITH ±6 VOLT POWER SUPPLIES

This is the most convenient method of interfacing a DAC-100 with CMOS logic. At ±6 volts, DAC-100 power dissipation is only 80mW, which is very small considering the inclusion of a complete internal reference. No interfacing components are required with ±5% power supplies, and the CMOS logic and DAC-100 can use the same +6 volt power supply. In this application the device is directly CMOS compatible.

HIGH LEVEL CMOS INTERFACING

The block diagram in Figure 5 illustrates a convenient method for interfacing CMOS input levels between 6.5 volts and 15 volts with a DAC-100. Inexpensive and readily available CMOS hex buffer/converters step down the high-level inputs to TTL levels that cannot exceed 5 volts — clearly satisfying the input stage voltage rule.

In addition to level shifting, buffer/converters provide input coding flexibility since they are available as inverting (CD4049A) or noninverting (CD4050A) devices. This gives the

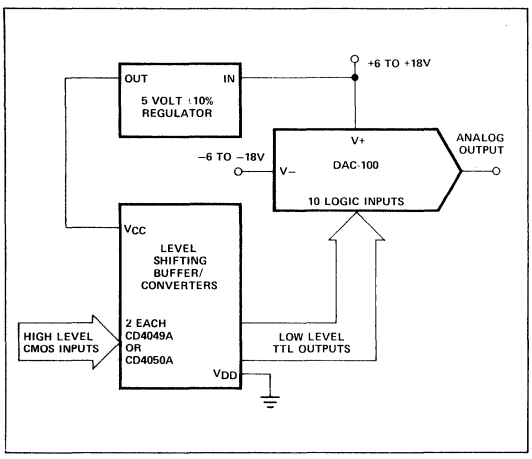


Figure 5. Block Diagram — CMOS to DAC-100 Interface

user a choice between negative-true and positive-true binary coding and allows the same basic DAC-100-to-CMOS interfacing method to be used in either type of application.

Since buffer/converter power consumption is very low, the required +5 volts can be provided by a simple regulator or even a resistive divider in some applications. In a multi-DAC system, one central, inexpensive 3-terminal IC regulator can supply several level shifting devices. Next, we will examine a complete circuit using all of these concepts in a high-speed CMOS compatible DAC.

COMPLETE CMOS COMPATIBLE DAC

The complete, 10-bit, voltage output DAC in Figure 6 has CMOS input compatibility, high speed, and low-cost. Current output from the DAC-10 is accurately converted to a voltage by the Precision Monolithics OP-01, a high speed op amp which has been specifically designed for the DAC summing amplifier application. Input offset voltage of this op amp is typically 2mV, eliminating the requirement for zero scale adjustment.

COMPLETE CMOS COMPATIBLE DAC DYNAMIC PERFORMANCE

The dynamic performance, as shown in the photograph, is quite good. Slew rate is 18V/μs while settling time to ±0.5% of full scale requires less than 1.5μs. DC performance is also

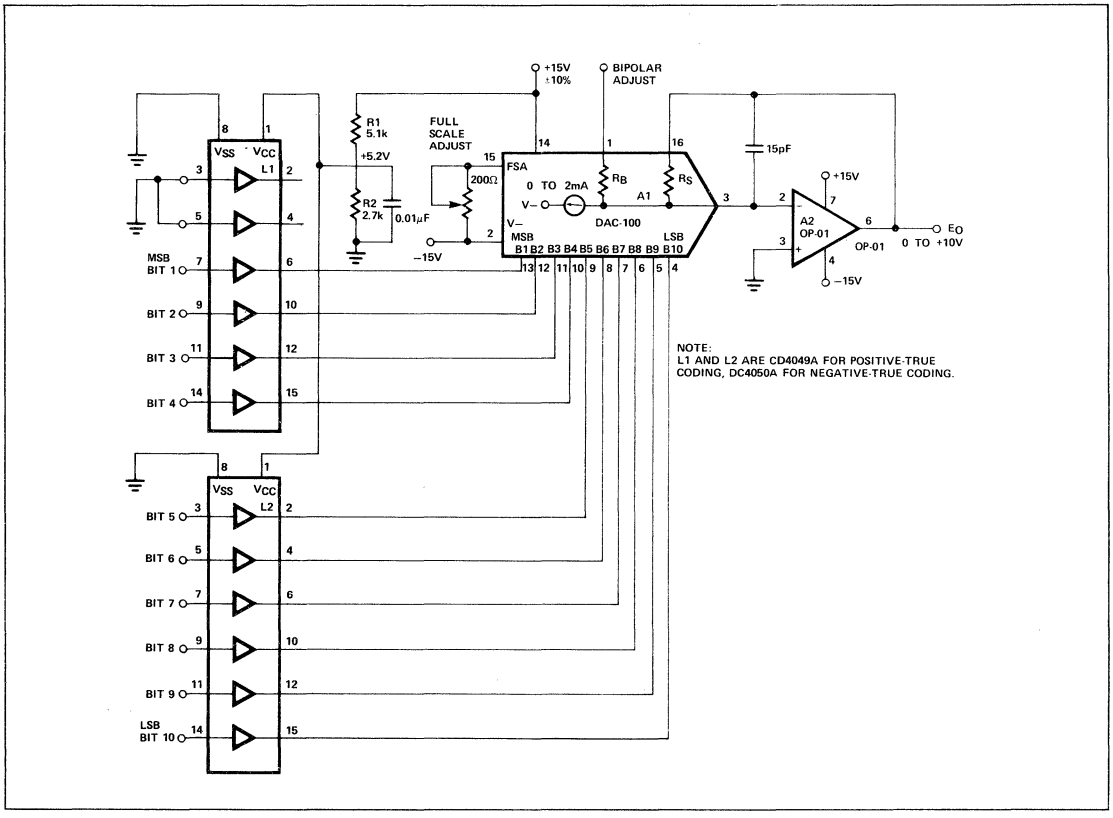
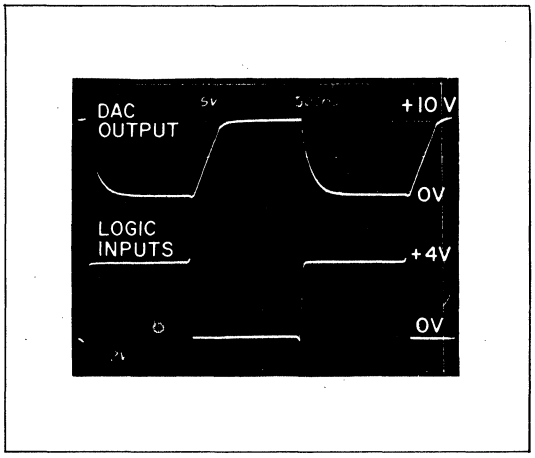


Figure 6. Interfacing DAC-100 with ±15 Volt CMOS Systems



good since DAC-100 nonlinearity is specified over the entire temperature range. In addition, the internal temperature-compensated voltage reference provides minimum full scale drift and decreases overall circuit complexity.

LOW COST THREE IC CMOS COMPATIBLE A/D CONVERTER

The diagram in Figure 7 is a modification of a previously published application note circuit substituting CMOS logic for TTL. All necessary logic for A to D conversion is contained in L1, a MC14559 CMOS successive approximation register. A conversion sequence is initiated by applying a positive pulse, with a width greater than one clock cycle, to the "Start Conversion" input. The analog input, applied to R_S and converted to a current, is compared successively to 1/2 scale, then 1/4 scale, and the remaining binarily-decreasing bit weights until it has been resolved within ±1/2LSB. At this time, "End of Conversion" changes to a logic "1" and the parallel answer is present in negative-true, binary-coded format at the register outputs.

Tracking A/D's may be similarly constructed using CD4029A up/down counters, a DAC-100, and a CMP-01 fast precision comparator.

CONCLUSION

Precision Monolithics D/A converters may be easily incorporated into CMOS systems. Low current logic input stage designs allow simple interfacing with a minimum of external components. The low power dissipation, high speed output and low cost make this line of monolithic DACs attractive in CMOS system designs.

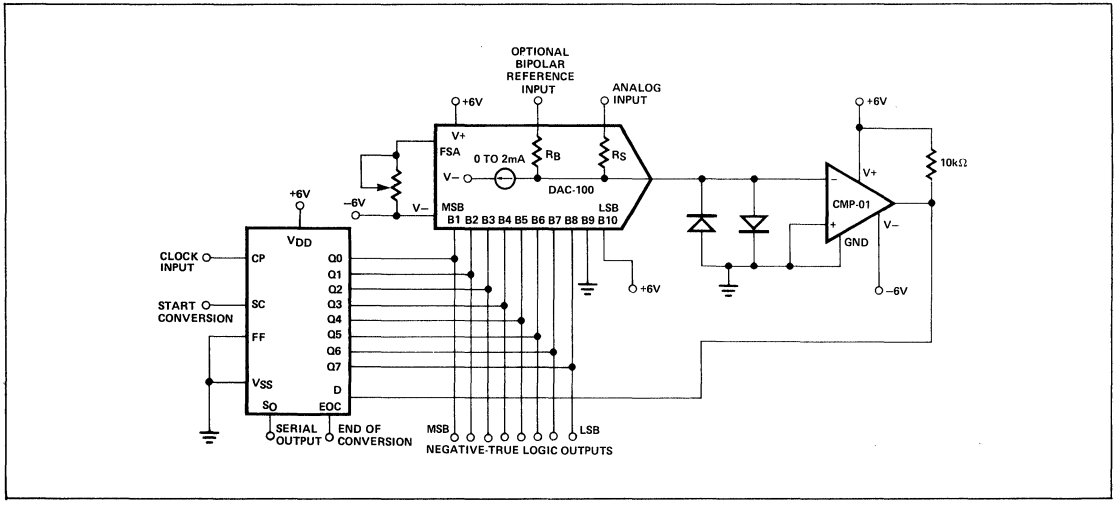


Figure 7. 8-Bit CMOS Compatible Three IC Successive Approximation A/D Converter

APPLICATION NOTE 15

MINIMIZATION OF NOISE IN OPERATIONAL AMPLIFIER APPLICATIONS

by Donn Soderquist

INTRODUCTION

Since operational amplifier specifications such as Input Offset Voltage and Input Bias Current have improved tremendously in the past few years, noise is becoming an increasingly important error consideration. To take advantage of today's high performance op amps, an understanding of the noise mechanisms affecting op amps is required. This paper examines noise contributions, both internal and external to an op amp, and provides practical methods for minimizing their effects.

BASIC NOISE PROPERTIES

Noise, for purposes of this discussion, is defined as any signal appearing in an op amp's output that could not have been predicted by DC and AC input error analysis. Noise can be random or repetitive, internally or externally generated, current or voltage type, narrowband or wideband, high frequency or low frequency; whatever its nature, it can be minimized.

The first step in minimizing noise is source identification in terms of bandwidth and location in the frequency spectrum; some of the more common soures are shown in Figure 1, an 11-decade frequency spectrum chart. Some preliminary observations can be made: noise is present from DC to VHF from sources which may be identified in terms of bandwidth and frequency. Noise source bandwidths overlap, making noise a composite quantity at any given frequency. Most externally caused noise is repetitive rather than random and can be found at a definite frequency. Noise effects from external sources must be reduced to insignificant levels to realize the full performance available from a low noise op amp.

EXTERNAL NOISE SOURCES

Since noise is a composite signal, the individual sources must be identified to minimize their effects. For example, 60Hz power line pickup is a common interference noise appearing at an op amp's output as a 16ms sine wave. In this and most other situations, the basic tool for external noise source frequency characterization is the oscilloscope sweep rate setting. Recognizing the oscilloscope's potential in this area, Tektronix® manufactures several preamplifiers with variable bandwidth and frequency which allow quick noise source frequency identification. Another basic identification tool is the simple low pass filter as shown in Figure 2, where the bandpass is calculated by:

$$1) \quad f_O \cong \frac{1}{2\pi RC}$$

With such a filter, measurement bandpass can be changed from 10Hz to 100kHz ($C = 4.7\mu F$ to 470pF), attenuating higher frequency components while passing frequencies of interest. Once identified, noise from an external source may be minimized by the methods outlined in Table 1 — the external noise source chart.

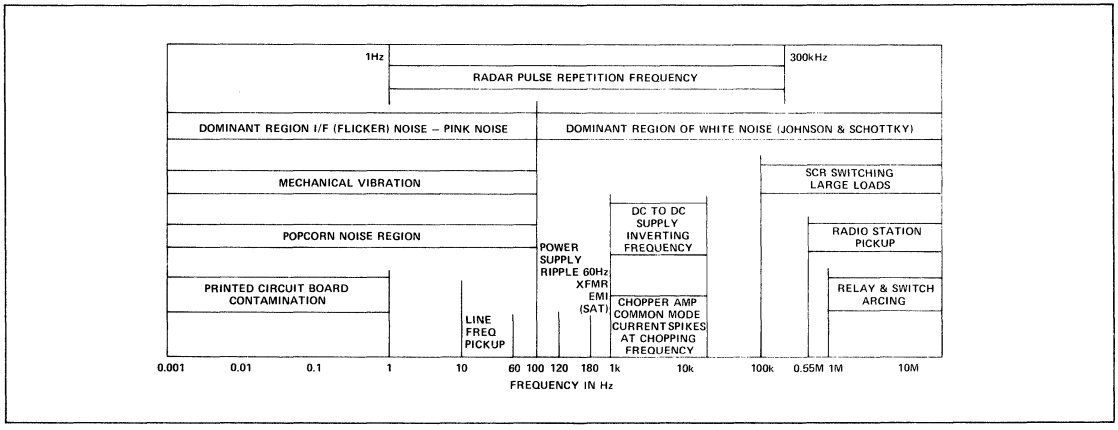


Figure 1. Frequency Spectrum of Noise Sources Affecting Operational Amplifier Performance

Table 1. External Noise Source Chart

Source	Nature	Causes	Minimization Methods
60Hz	Repetitive Interference	Powerlines physically close to op amp inputs. Poor CMRR at 60Hz. Power Transformer primary-to-secondary capacitive coupling.	Reorientation of power wiring. Shielded transformers. Single point grounding. Battery power.
120Hz Ripple	Repetitive	Full wave rectifier ripple on op amp's supply terminals. Inadequate ripple consideration. Poor PSRR at 120Hz.	Thorough design to minimize ripple. RC decoupling at the op amp. Battery power.
180Hz	Repetitive EMI	180Hz radiated from saturated 60Hz transformers.	Physical reorientation of components. Shielding. Battery power.
Radio Stations	Standard AM Broadcast Through FM	Antenna action anyplace in system.	Shielding. Output filtering. Limited circuit bandwidth.
Relay and Switch Arcing	High frequency burst at switching rate	Proximity to amplifier inputs, power lines, compensation terminals, or nulling terminals.	Filtering of HF components. Shielding. Avoidance of ground loops. Arc suppressors at switching source.
Printed Circuit Board Contamination	Random Low Frequency	Dirty boards or sockets.	Thorough cleaning at time of soldering followed by a bakeout and humidity sealant.
Radar Transmitters	High Frequency Gated At Radar Pulse Repetition Rate	Radar transmitters from long range surface search to short range navigational — especially near airports.	Shielding. Output filtering of frequencies >>PRR.
Mechanical Vibration	Random < 100Hz	Loose connections, intermittent contact in mobile equipment.	Attention to connectors and cable conditions. Shock mounting in severe environments.
Chopper Frequency Noise	Common Mode Input Current At Chopping Frequency	Abnormally high noise chopper amplifier in system.	Balanced source resistors. Use bipolar input op amps instead. Use premium low noise chopper.

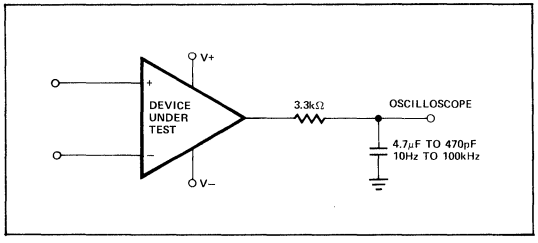


Figure 2. Noise Frequency Analysis RC Low Pass Filter

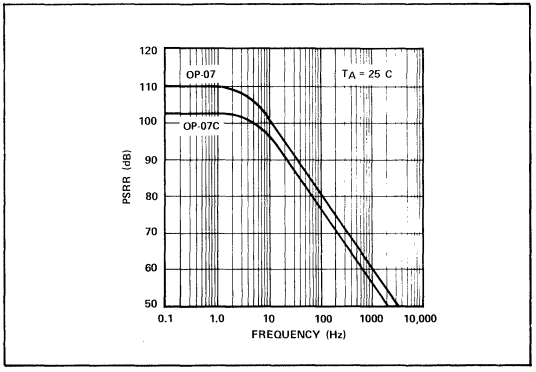


Figure 3. PSRR vs Frequency (OP-07, OP-07C)

POWER SUPPLY RIPPLE

Power supply ripple at 120Hz is not usually thought of as a noise, but it should be. In an actual op amp application, it is quite possible to have a 120Hz noise component that is equal in magnitude to all other noise sources combined, and, for this reason, it deserves a special discussion.

To be negligible, 120Hz ripple noise should be between 10nV and 100nV referred to the input of an op amp. Achieving these low levels requires consideration of three factors: the op amp's 120Hz power supply rejection ratio (PSRR), the regulator's ripple rejection ratio, and finally, the regulator's input capacitor size.

PSRR at 120Hz for a given op amp may be found in the manufacturer's data sheet curves of PSRR versus frequency as shown in Figure 3. For the amplifier shown, 120Hz PSRR is about 74dB, and to attain a goal of 100nV referred to the input, ripple at the power terminals must be less than 0.5mV. Today's IC regulators provide about 60dB of ripple rejection; in this case the regulator input capacitor must be made large enough to limit input ripple to 0.5V.

Externally-compensated low noise op amps can provide improved 120Hz PSRR in high closed-loop gain configurations. The PSRR versus frequency curves of such an op amp are shown in Figure 4. When compensated for a closed-loop gain of 1000, 120Hz PSRR is 115dB. PSRR is still excellent at much higher frequencies allowing low ripple-noise operation in exceptionally severe environments.

POWER SUPPLY DECOUPLING

Usually, 120Hz ripple is not the only power supply associated noise. Series regulator outputs typically contain at

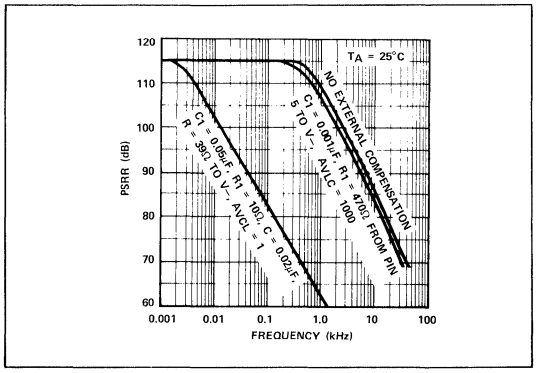


Figure 4. PSRR vs Frequency (OP-06)

least 150μV of noise in the 100Hz to 10kHz range; switching types contain even more. Unpredictable amounts of induced noise can also be present on power leads from many sources. Since high frequency PSRR decreases at 20dB/decade, these higher frequency supply noise components must not be allowed to reach the op amp's power terminals. RC decoupling, as shown in Figure 5, will adequately filter most wideband noise. Some caution must be exercised with this type of decoupling, as load current changes will modulate the voltage at the op amp's supply pins.

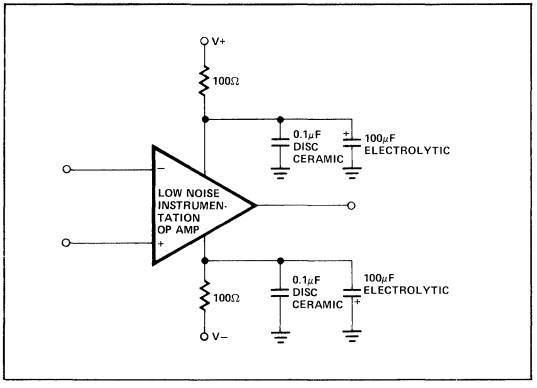


Figure 5. RC Decoupling

POWER SUPPLY REGULATION

Any change in power supply voltage will have a resultant effect referred to an op amp's inputs. For the op amp of Figure 3, PSRR at DC is 110dB (3μV/V) which may be considered as a potential low frequency noise source. Power supplies for low noise op amp applications should, therefore, be both low in ripple and well-regulated. Inadequate supply regulation is often mistaken to be low frequency op amp noise.

When noise from external sources has been effectively minimized, further improvements in low noise performance are obtained by specifying the right op amp and through careful selection and application of the associated components.

OPERATIONAL AMPLIFIER INTERNAL NOISE

OP AMP NOISE SPECIFICATIONS

Most completely specified low noise op amp data sheets specify current and voltage noises in a 1Hz bandwidth and low frequency noise over a range of 0.1Hz to 10Hz. To minimize total noise, a knowledge of the deviation of these specifications is useful. In this section, the reader is provided with an explanation of basic op amp-associated random noise mechanisms and introduced to a simplified method for calculating total input-referred noise in typical applications.

RANDOM NOISE CHARACTERISTICS

Op amp-associated noise currents and voltages are random. They are aperiodic and uncorrelated to each other and have Gaussian amplitude distributions, the highest noise amplitudes having the lowest probability. Gaussian amplitude distribution allows random noises to be expressed as rms quantities; multiplying a Gaussian rms quantity by six results in a peak-to-peak value that will not be exceeded 99.73% of the time (this is a handy rule-of-thumb for noise calculations).

The two basic types of op amp-associated noises are white noise and flicker noise (1/f). White noise contains equal amounts of power in each Hertz of bandwidth. Flicker noise is different in that it contains equal amounts of power in each *decade* of bandwidth. This is best illustrated by spectral noise density plots such as in Figures 6 and 7. Above a certain corner frequency, white noise dominates; below that frequency flicker (1/f) noise is dominant. Low noise corner frequencies distinquish low noise op amps from general purpose devices.

SPECTRAL NOISE DENSITY

To utilize Figures 6 and 7, let us consider the definition of spectral noise density: the square root of the rate of change of mean-square noise voltage (or current) with frequency (Equation 2).

2A. $e_n^2 = \frac{d}{df}(E_n)^2$ 2B. $i_n^2 = \frac{d}{df}(I_n)^2$

3A. $E_n = \sqrt{\int_{f_L}^{f_H} e_n^2\, df}$ 3B. $I_n = \sqrt{\int_{f_L}^{f_H} i_n^2\, df}$

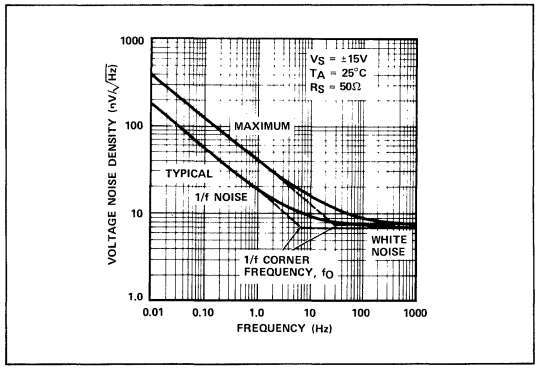


Figure 6. OP-06 Noise Voltage

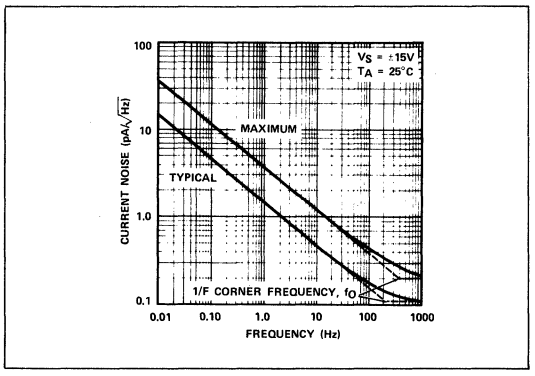


Figure 7. OP-06 Noise Current

Where: e_n, i_n = Spectral noise density
E_n, I_n = Total rms noise
f_H = Upper frequency limit
f_L = Lower frequency limit

Conversely, the rms noise value within a given frequency band is the square root of the definite integral of the spectral noise density over that frequency band (Equation 3). This means that three things must be known to evaluate total voltage noise (E_n) or current noise (I_n): f_H, f_L, and a knowledge of noise behavior over frequency.

WHITE NOISE

White noise sources are defined to have a noise content that is equal in each Hertz of bandwidth, and Equation 3 may be rewritten for white noise sources as:

4. $E_n(w) = e_n\sqrt{f_H - f_L}$ 5. $I_n(w) = i_n\sqrt{f_H - f_L}$

It is therefore convenient to express spectral noise density in $V/\sqrt{Hz}$ or $A/\sqrt{Hz}$ where $f_H - f_L = 1Hz$. When $f_H \geq 10f_L$, the white noise expressions may be further reduced to:

6. $E_n(w) = e_n\sqrt{f_H}$ 7. $I_n(w) = i_n\sqrt{f_H}$

FLICKER NOISE

Since flicker noise content is equal in each decade of bandwidth, total flicker noise may be calculated if noise in one decade is known. The 0.1Hz to 1Hz decade noise content (K) is widely used for this purpose because the white noise contribution below 10Hz is usually negligible.

8. $E_n(f) \cong K\sqrt{\frac{1}{f}}$ 9. $I_n(f) K\sqrt{\frac{1}{f}}$

When substituted in Equation 3, the expressions may be rewritten to:

10. $E_n(f) = K\sqrt{I_n \frac{f_H}{f_L}}$ 11. $I_n(f) = K\sqrt{I_n \frac{f_H}{f_L}}$

FLICKER NOISE AND WHITE NOISE

When corner frequencies are known, simplified expressions for total voltage and current noise (E_N and I_N) may be written:

12. $E_N(f_H - f_L) = e_n\sqrt{f_{ce} I_n (\frac{f_H}{f_L}) + f_H - f_L}$

13. $I_N(f_H - f_L) = i_n\sqrt{f_{ci} I_n (\frac{f_H}{f_L}) + f_H - f_L}$

Where: e_n = White noise voltage in a 1Hz bandwidth
i_n = White noise current in a 1Hz bandwidth
f_{ce} = Voltage noise corner frequency
f_{ci} = Current noise corner frequency
f_H = Upper frequency limit
f_L = Lower frequency limit

The two most important internally generated noise minimization rules are derived from Equation 12 and 13: limit the circuit bandwidth and use operational amplifiers with low corner frequencies.

NOISE SUMMATION

In the spectral density discussion, the concepts of white noise and flicker noise were introduced. In Figure 8, the complete input-referred op amp noise model, internal white and flicker noise sources are combined into three equivalent input noise generators, E_N, I_{N1} and I_{N2}. The noise current generators produce noise voltage drops across their respective source resistors, R_{S1} and R_{S2}. The source resistors themselves generate thermal noise voltages, E_{t1}, and E_{t2}. Total rms input-referred voltage noise, over a given bandwidth, is the square root of the sum of the squares of the five noise voltage sources over that bandwidth.

14. $E_{NT}(f_H - f_L) = \sqrt{E_N^2 + (I_{N1} \cdot R_{S1})^2 + (I_{N2} \cdot R_{S2})^2 + E_{t1}^2 + E_{t2}^2}$

Minimization of total noise requires an understanding of the mechanisms involved in each of the five generators. First, the white noise mechanisms, thermal and shot, are discussed, followed by the low frequency noise mechanisms, flicker and popcorn.

THERMAL NOISE

Thermal (Johnson) noise is a white noise voltage generated by random movement of thermally-charged carriers in a resistance; in op amp circuits this is the type of noise produced by the source resistances in series with each input. Its rms value over a given bandwidth is calculated by:

15. $E_t = \sqrt{4kTR(f_H - f_L)}$

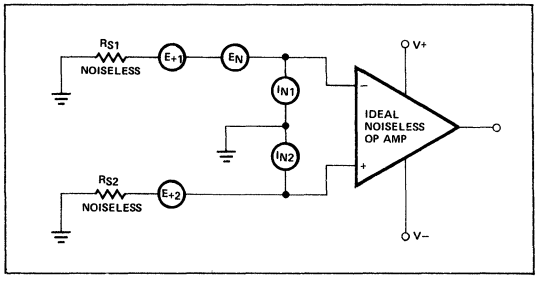


Figure 8. Op Amp Noise Model

Where: k = Boltzmann's constant = 1.38 x 10^{-23}joules/°K

T = Absolute temperature, °Kelvin

R = Resistance in ohms

f_H = Upper frequency limit in Hertz

f_L = Lower frequency limit in Hertz

At room temperature Equation 15 simplifies to:

16. $E_t = 1.28 \times 10^{-10} \sqrt{R(f_H - f_L)}$

To minimize thermal noise (E_{t1} and E_{t2}) from R_{S1} and R_{S2}, large source resistors and excessive system bandwidth should be avoided.

Thermal noise is also generated inside the op amp, principally from $r_{bb'}$, the base-spreading resistances in the input stage transistors. These noises are included in E_N, the total equivalent input voltage noise generator.

SHOT NOISE

Shot noise (Schottky noise) is a white noise current associated with the fact that current flow is actually a movement of discrete charged particles (electrons). In Figure 8, I_{N1} and I_{N2}, above the 1/f frequency, are shot noise currents which are related to the amplifier's DC input bias currents:

17. $I_{sh} = \sqrt{2qI_{BIAS}(f_H - f_L)}$

Where: I_{sh} = RMS shot noise value in amps

q = Charge of an electron = 1.59 x 10^{-19}

I_{BIAS} = Bias current in amps

f_H = Upper frequency limit in Hertz

f_L = Lower frequency limit in Hertz

At room temperature Equation 17 simplifies to:

18. $I_{sh} = 5.64 \times 10^{-10} \sqrt{I_{BIAS}(f_H - f_L)}$

Shot noise currents also flow in the input stage emitter dynamic resistances (r_e), producing input noise voltages. These voltages, along with the $r_{bb'}$ thermal noise, make up the white noise portion of E_N, the total equivalent input noise voltage generator.

FLICKER NOISE

In limited bandwidth applications, flicker (1/f) noise is the most critical noise source. An op amp designer minimizes flicker noise by keeping current noise components in the input and second stages from contributing to input voltage noise. Equation 19 illustrates this relationship:

19. $\frac{i_{n\ \text{second stage}}}{g_{m\ \text{first stage}}} = e_{n\ \text{input}}$

Another critical factor is corner frequency. For minimum noise the current and voltage noise corner frequencies must be low; this is crucial. As shown in Figure 9, low noise corner frequencies distinquish low noise op amps from ordinary industry-standard 741 types.

The photograph in Figure 10, taken using the test circuit of Figure 11, illustrates the flicker noise performance of the OP-07. This device demonstrates proper attention to low noise circuit design and wafer processing and achieves a remarkable 0.35μV peak-to-peak input voltage noise in the 0.1Hz to 10Hz bandwidth.

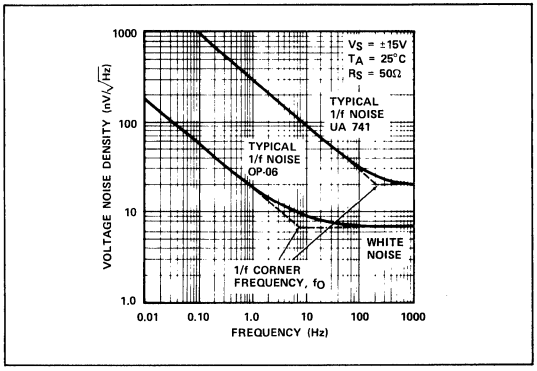


Figure 9. Noise Voltage Comparison

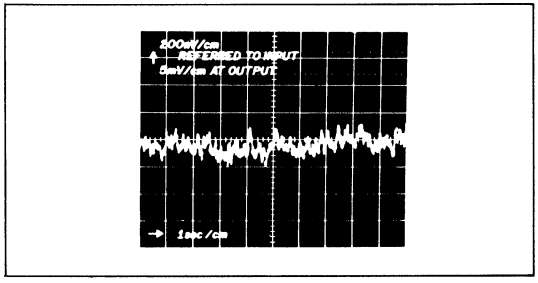


Figure 10. OP-07 Low Frequency Noise

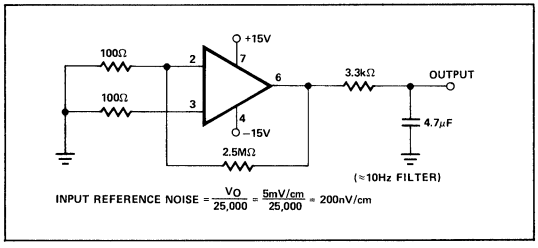


Figure 11. Low Frequency Noise Test Circuit

POPCORN NOISE

Popcorn noise (burst noise) is a momentary change in input bias current usually occurring below 100Hz, and is caused by imperfect semiconductor surface conditions incurred during wafer processing. Precision Monolithics minimizes this problem through careful surface treatment, general cleanliness, and a special three-step process known as "Triple Passivation."

To begin the process, a specially treated thermal silicon dioxide layer is grown. This protects the junctions and also attracts any residual ionic impurities to the top surface of the oxide, where they are held fixed. Next, a layer of silicon nitride is applied to prevent the entry of any potential contamination or impurities. The third step is the thick glass overcoat which leaves only the bonding pads exposed. A cutaway view of a finished device is shown in Figure 12.

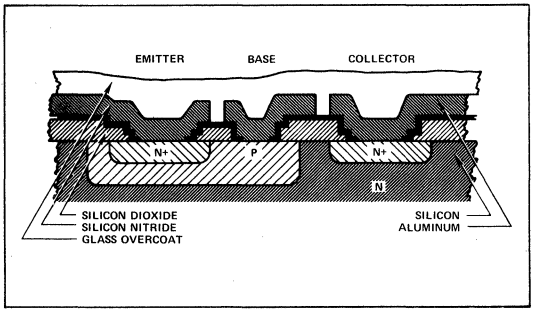


Figure 12. Triple Passivated™ Integrated Circuit Process

Op amp manufacturers face a difficult decision in dealing with popcorn noise. Through careful low noise processing, it can be eliminated from almost all devices; alternatively, the processing may be relaxed, and finished devices must be individually tested for this parameter. Special noise testing takes valuable labor time, adds significant amounts to manufacturing cost, and ultimately increases the price a customer has to pay. At Precision Monolithics the low noise process alternative is used to manufacture high volumes of cost-effective low noise op amps.

TOTAL NOISE CALCULATION

With data sheet curves and specifications, and a knowledge of source resistance values, total input-referred noise may be calculated for a given application. To illustrate the method, noise information from the Precision Monolithics OP-07 data sheet is reproduced in Figure 13. The first step is to determine the current and voltage noise corner frequencies so that the E_N and I_N terms of Equation 14 may be calculated using Equation 12 and 13.

CORNER FREQUENCY DETERMINATION

In the input spot noise versus frequency curves of Figure 13, it may be seen that voltage noise ($R_S = 0$) begins to rise at about 10Hz. Lines projected from the horizontal (white noise) portion and sloped (flicker noise) portion intersect at 6Hz, the voltage noise corner frequency (f_{ce}). In the center curve, excluding thermal noise from the source resistance,

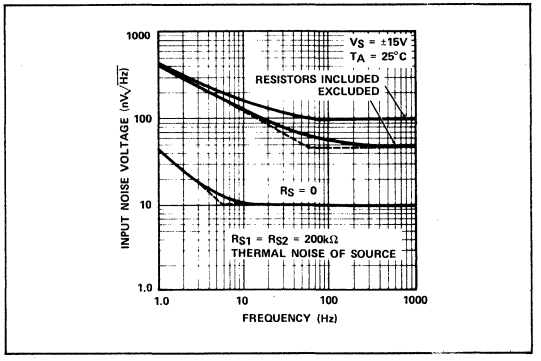


Figure 13A. Input Spot Noise Voltage vs Frequency

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and $T_A = 25°C$, unless otherwise noted.

			OP-07A			OP-07			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.35	0.6	—	0.35	0.6	μV_{p-p}
Input Noise Voltage Density	e_n	f_o = 10Hz	—	10.3	18.0	—	10.3	18.0	$nV/\sqrt{Hz}$
		f_o = 100Hz	—	10.0	13.0	—	10.0	13.0	
		f_o = 1000Hz	—	9.6	11.0	—	9.6	11.0	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	14	30	—	14	30	pA_{p-p}
Input Noise Current Density	i_n	f_o = 10Hz	—	0.32	0.80	—	0.32	0.80	$pA/\sqrt{Hz}$
		f_o = 100Hz	—	0.14	0.23	—	0.14	0.23	
		f_o = 1000Hz	—	0.12	0.17	—	0.12	0.17	
Input Offset Voltage	V_{os}		—	10	25	—	30	75	μV
Long Term Input Offset Voltage Stability	V_{os}/Time		—	0.2	1.0	—	0.2	1.0	μV/Mo
Input Offset Current	I_{os}		—	0.3	2.0	—	0.4	2.8	nA
Input Bias Current	I_B		—	±0.7	±2.0	—	±1.0	±3.0	nA

INPUT NOISE VOLTAGE (e_{np-p})

The peak-to-peak noise voltage in a specified frequency band.

INPUT NOISE VOLTAGE DENSITY (e_n)

The rms noise voltage in a 1Hz band surrounding a specified value of frequency.

INPUT NOISE CURRENT (i_{np-p})

The peak-to-peak noise current in a specified frequency band.

INPUT NOISE CURRENT DENSITY (i_n)

The rms noise current in a 1Hz band surrounding a specified value of frequency.

Figure 13B. OP-07 Ultra-Low Offset Voltage Op-Amp

current noise multiplied by 200kΩ is plotted as a voltage noise. Lines projected from the horizontal portion and sloped portions intersect at 60Hz, the current noise corner frequency (f_{ci}).

Equations 12 and 13 aiso require e_n and i_n for calculation of E_N and I_N. To find e_n and i_n, use the data sheet specification a decade or more above the respective corner frequencies; in this case e_n is 9.6nV/$\sqrt{Hz}$ (1000Hz), and i_n is 0.12pA/$\sqrt{Hz}$ (1000Hz).

BANDWIDTH OF INTEREST

To be summed correctly, each of the five noise quantities must be expressed over the same bandwidth, $f_H - f_L$. At this time, assume f_H to be the highest frequency component that must be amplified without distortion. Note that e_n, i_n, corner frequencies and bandwidth are independent of actual circuit component values. When doing noise calculations for a large number of circuits using the same op amp, these numbers only have to be calculated once.

TYPICAL APPLICATION EXAMPLE

Figure 14A shows a typical X10 gain stage with a 10kΩ source resistance. In Figure 14B, the circuit is redrawn to show five noise voltage sources. To evaluate total input-referred noise, the values of each of the five sources must be determined.

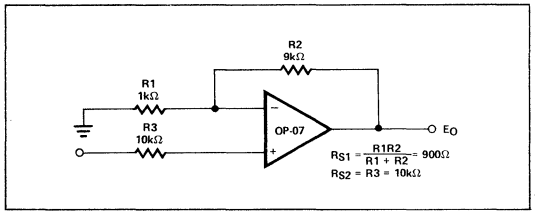


Figure 14A. Noise Analysis Circuit

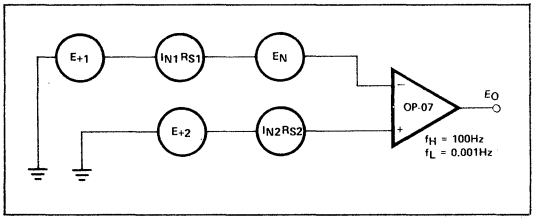


Figure 14B. Noise Analysis Equivalent Circuit

Using Equation 16: $E_t = \sqrt{R\,(f_H - f_L)}$

$E_{t1} = 1.28 \times 10^{-10} \sqrt{(900\Omega)\,(100Hz)} = 0.04\mu Vrms$

$E_{t2} = 1.28 \times 10^{-10} \sqrt{(10k\Omega)\,(100Hz)} = 0.128\mu Vrms$

Next, calculate I_N using Equation 13:

$$I_N = \sqrt{f_{ci}\, I_n \left(\frac{f_H}{f_L}\right) + f_H - f_L}$$

$$= 0.12pA \sqrt{60\, I_n \frac{100Hz}{0.0001Hz} + 100 - 0.0001}$$

$$= 3.66pArms$$

and:

$I_{N1} \cdot R_{S1} = 3.66pA\ (900\Omega) = 0.0033\mu Vrms$
$I_{N2} \cdot R_{S2} = 3.66pA\ (10k\Omega) = 0.0366\mu Vrms$

Finally, E_N from Equation 12:

$$E_N = e_n \sqrt{f_{ce}\, I_n \left(\frac{f_H}{f_L}\right) + f_H - f_L}$$

$$= 9.6nV \sqrt{6\, I_n \frac{100Hz}{0.0001Hz} + 100 - 0.0001}$$

$$= 0.130\mu Vrms$$

Substituting in Equation 14:

$$14)\ E_{NT}\,(f_H - f_L) = \sqrt{E_N^2 + I_{N1}^2\, R_{S1}^2 + I_{N2}^2\, R_{S2}^2 + E_{t1}^2 + E_{t2}^2}$$

$$= \sqrt{(.130\mu V)^2 + (.0033\mu V)^2 + (.0366\mu V)^2 + (.04\mu V)^2 + (.128\mu V)^2}$$

$$= 0.19\mu Vrms$$

Total input-referred noise = 1.14μV peak-to-peak (0.0001Hz to 100Hz).

741 CALCULATION EXAMPLE

The preceding calculation determined total noise in a given bandwidth using a low noise op amp. To place this level of performance into perspective, a calculation using the industry-standard 741 op amp in the circuit of Figure 14 is useful. Once again the starting point is corner frequency determination, using the data sheet curves of Figure 15: f_{ce} = 200Hz; f_{ci} = 2kHz; $e_n \cong 20nV/\sqrt{Hz}$; $i_n = 0.5pA/\sqrt{Hz}$.

Using these corner frequencies and noise magnitudes, E_N and I_N are calculated to be 1μVrms and 83pArms respectively. Multiplying this noise current by the source resistance gives terms 2 and 3 of Equation 14 as shown below:

$$14.\ E_{NT}\,(f_H - f_L) = \sqrt{E_N^2 + I_{N1}^2\, R_{S1}^2 + I_{N2}^2\, R_{S2}^2 + E_{+1}^2 + E_{+2}^2}$$

Substituting in Equation 14:

$$= \sqrt{(1\mu V)^2 + (0.075\mu V)^2 + (0.83\mu V)^2 + (0.04\mu V)^2 + (0.128\mu V)^2}$$

$$= 1.3\mu Vrms$$

Total input-referred noise = 7.8μV peak-to-peak (0.0001Hz to 100Hz).

This is 6.8 times that of the low noise op amp example.

The calculation examples illustrate three rules for minimizing noise in operational amplifier applications:

Rule 1. Use an op amp with low corner frequencies.

Rule 2. Keep source resistances as low as possible.

Rule 3. Limit circuit bandwidth to signal bandwidth.

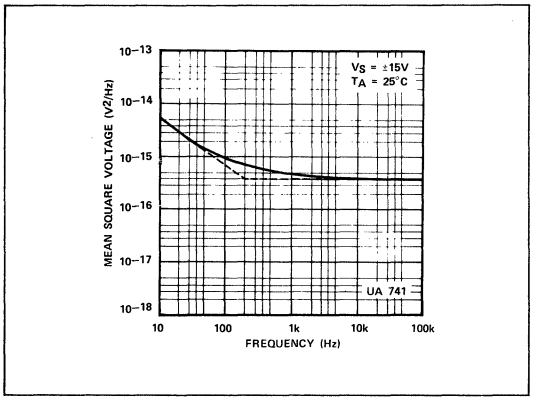


Figure 15A. Input Noise Voltage as a Function of Frequency

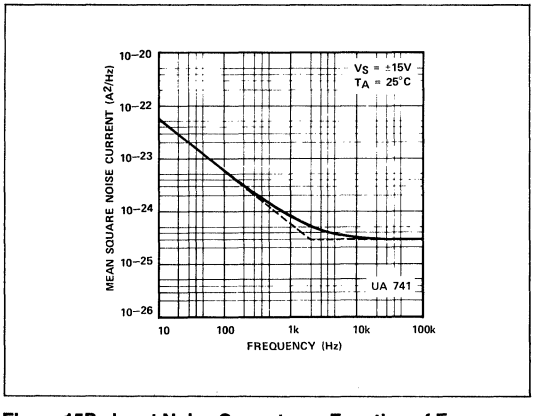


Figure 15B. Input Noise Current as a Function of Frequency

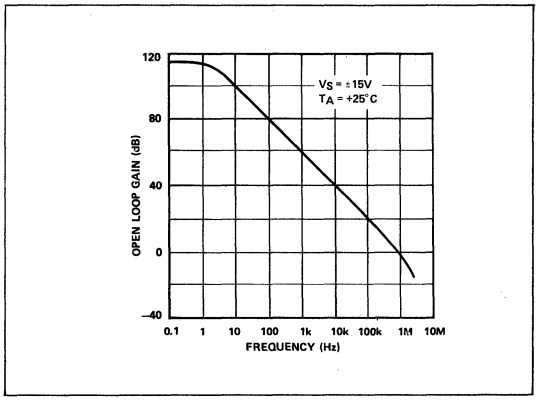


Figure 16A. Open Loop Frequency Response

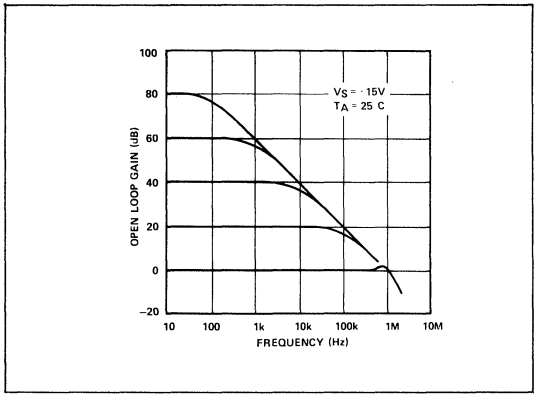


Figure 16B. Closed Loop Response for Various Gain Configurations

BANDWIDTH

Effective circuit bandwidth must not be much greater than signal bandwidth or amplification of undesirable high frequency noise components will occur. Throughout the preceding calculations, an assumption of "bandwidth-of-interest" was made, while in actual application the amplifier's bandwidth must be considered.

In Figure 16, the OP-07 frequency response curves show a rolloff of 20dB/decade; integration of the area under the curve will show the effective circuit noise bandwidth to be 1.57 times the 3dB bandwidth. In most closed-loop gain configurations, the amplifier's bandwidth may be greater than required, and output filtering, such as in Figure 17, could be used. As an alternate to output filtering, an integrating capacitor may be connected across the feedback resistor. Bandwidth may also be limited in some applications by overcompensating an externally-compensated low noise op amp, such as the SSS725.

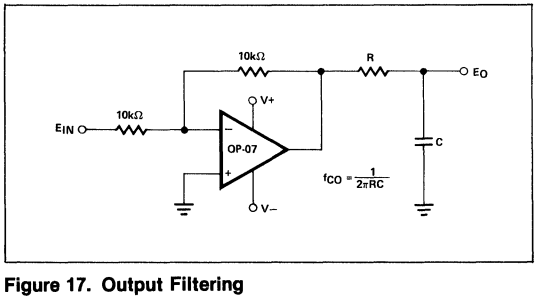


Figure 17. Output Filtering

MISCELLANEOUS NOISE MINIMIZATION METHODS

Certain other noise mechanisms merit consideration: use metal film resistors; carbon resistors exhibit "excess noise", with both 1/f and white noise content being related

to DC applied voltage. The use of balanced source resistors, while sometimes good for DC error purposes, will increase noise; the balancing resistor is not required for op amps such as the OP-07, since $I_{OS} \cong I_B$. Keep noise in its proper perspective; minimize it without introducing additional DC errors. Use low noise op amps with overall DC specifications that will satisfy the application.

SUMMARY

A summary of the major points to consider is as follows:

1. Minimize externally generated noise.
2. Choose an amplifier with low 1/f noise corner requencies.
3. Limit the circuit bandwidth to signal bandwidth.
4. Eliminate excessive resistance in the input circuit.

CONCLUSION

Recent improvements in IC op amp DC specifications have made noise an important error consideration. From data sheet information and source resistance values, total input-referred noise over a given bandwidth can be easily calculated. Total noise can be minimized by a thorough understanding of the various noise-generation mechanisms.

ACKNOWLEDGEMENTS

The author wishes to express his thanks to George Erdi, the designer of the OP-06 and OP-07, for his patient technical assistance.

NOISE BIBLIOGRAPHY

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APPLICATION NOTE 16

LOW-COST, HIGH-SPEED ANALOG-TO-DIGITAL CONVERSION WITH THE DAC-08

By Donn Soderquist and John Schoeff

Today's fast computer and microprocessor-controlled systems frequently require A/D converters which will complete a conversion in one cycle time.

Until now, these high speed A/D converters have been expensive and difficult to build. Most designers have therefore chosen to purchase modular A/D converters typically ranging in price from $100 to $400. This application note describes three less costly A/D designs, with total conversion times of 4μs, 2μs, and 1μs. These designs are implemented with the DAC-08, a recently announced high speed monolithic digital-to-analog converter. A discussion of basic successive approximation is given, followed by practical circuit designs.

SUCCESSIVE APPROXIMATION A/D ADVANTAGES

Successive approximation A/D conversion is the most popular choice in many systems today because it achieves high conversion rates at very low cost. Other methods, such as Tracking (Servo) or Staircase (Ramp), require up to "2^n" clock cycles per conversion, where "n" is the number of bits of resolution, while successive approximation requires only "n + 1" clock cycles. Finally, a designer can easily construct his A/D with readily available standard ICs.

BASIC SUCCESSIVE APPROXIMATION A/D CONVERSION

A successive approximation A/D converter operates by comparing the analog input to a series of "trial" conversions; the first trial compares the input to the value of the most significant bit (MSB) or half of full scale. Figure 1 shows the progression of trials for a 3-bit converter. If the input is greater than the MSB value, the MSB is retained and the converter moves on to "trying" the next most significant bit, or three-quarters full scale. If the input had been less than the MSB, the logic would have turned the MSB off before going on to the next most significant bit, or one-quarter full scale. This "branching" continues until each successively smaller bit has been tried, with the entire process taking "n" trials.

To implement the logic for the successive approximation algorithm, a configuration similar to Figure 2 may be employed, wherein a start command places a "one" in the first bit of a shift register. This sets the first latch to "one" and turns on the DAC's MSB. If the comparator output remains low, the "one" will remain in the latch; if not, the latch

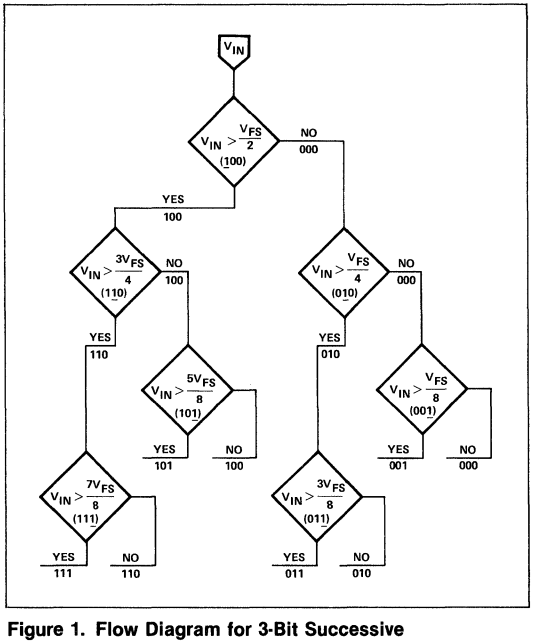


Figure 1. Flow Diagram for 3-Bit Successive Approximation A/D Conversion

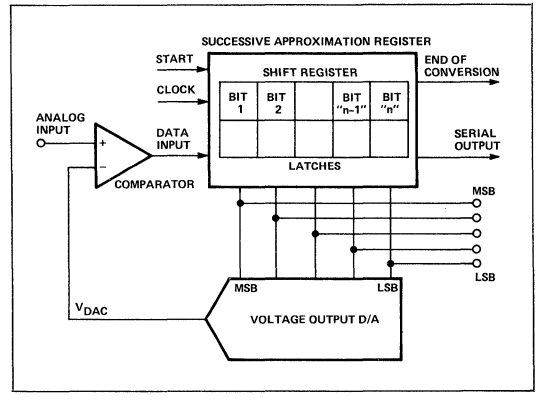


Figure 2. Successive Approximation A/D Converter

will be reset to zero before the next bit trial begins. The next clock cycle causes the shift register to place a "one" in the second bit, and a similar process continues until all bits have been tried. After the last bit's trial, the end-of-conversion output changes state indicating the parallel data is ready to be used.

CURRENT COMPARISON

The previous discussion indicated that the function of the comparator was to perform a comparison between the analog input **voltage** and the output **voltage** of the DAC. Higher speed conversions may be achieved by using the output of a fast current output DAC directly. This may be implemented as shown in Figure 3, where the comparator examines the polarity of $(V_{IN} - I_{DAC}R_{IN})$. Current comparison eliminates the need for a current-to-voltage converting op amp which is by far the slowest element in most D/A converters.

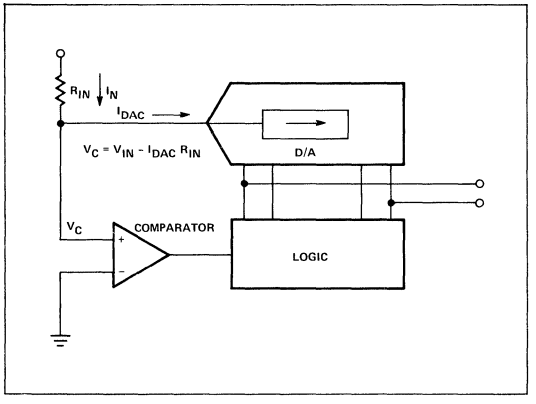


Figure 3. Current Comparison A/D Input

DYNAMIC CONSIDERATIONS

The time required to complete an 8-bit successive approximation A/D conversion is determined by the length of 8 trials and their associated comparator decisions, plus one clock cycle. To minimize these periods, three dynamic considerations must be made:

1. DAC output current settling time to ±1/2LSB.
2. Comparator propagation delay with the available overdrive.
3. Logic propagation delay and setup time requirements.

For example, with a 500ns DAC, a 500ns comparator, and 100nsec of logic delay, each of these cycles would require 1.1μs. An 8-bit conversion would take nine clock periods, or 10μs. To design a fast A/D, each of these delays must be made as short as possible. In the next few paragraphs, practical methods of minimizing these delays are discussed.

DAC CURRENT SETTLING TIME

The DAC-08 is a low cost monolithic current output DAC with 85ns full scale settling time and is ideal for use in high speed A/D converter designs. The internal logic switch design enables propagation delays of 35ns for each of the 8 bits. Settling time of the LSB to within ±1/2LSB of final value is therefore 35ns, with each successively more significant bit taking progressively longer. The MSB settles in 85ns; it is the dominant factor of full scale settling time. This performance is illustrated in the scope photo of Figure 4, taken at the output of the test circuit of Figure 5.

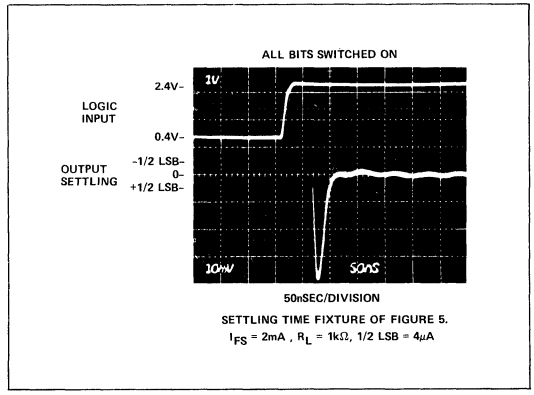


Figure 4. Output Settling Time

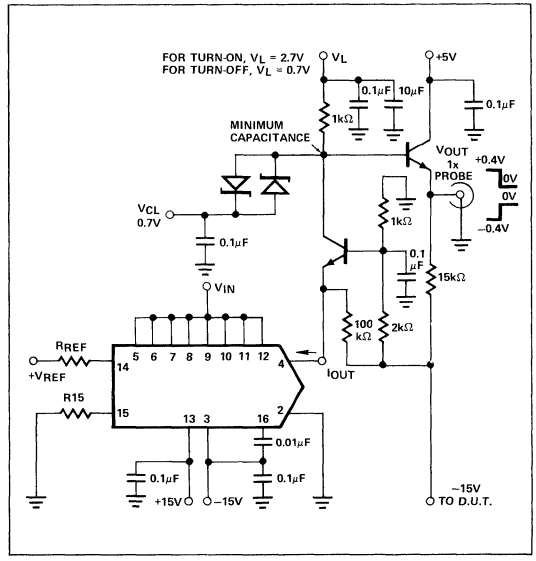


Figure 5. Settling Time Measurement

A major factor affecting settling time is the RC time constant formed by the load resistance (R_L) and the DAC output capacitance (C_O) plus any stray capacitance present at the

summing node. Settling to within ±1/2LSB at 8 bits (±0.2% full scale) requires 6.2 RC time constants. For the DAC-08, the output capacitance is 15pF; as a result the output RC time constant is a major factor influencing settling time when R_L is greater than 500Ω and dominates when R_L exceeds 900Ω.

This situation produces difficult requirements. Optimum DAC settling time occurs when $R_L \leq 500\Omega$, but for full scale currents of 2mA, 1/2LSB is only 4μA. Thus, with a 500Ω equivalent resistance, the voltage at the DAC output corresponding to 1/2LSB is only 2mV and is inadquate for high speed operation of many comparators. For this reason, R_L is usually larger than 500Ω, which is a necessary compromise between DAC settling time and comparator input overdrive requirements.

COMPARATOR CONSIDERATIONS

All comparators respond fastest to large differential input voltages (high overdrive). This phenomenon is shown in Figure 6, a graph of response time vs input voltage for the Precision Monolithics' CMP-01. This low cost comparator provides DC characteristics compatible with 10 and 12-bit A/D converters and has adequate speed for 4μs 8-bit converters.

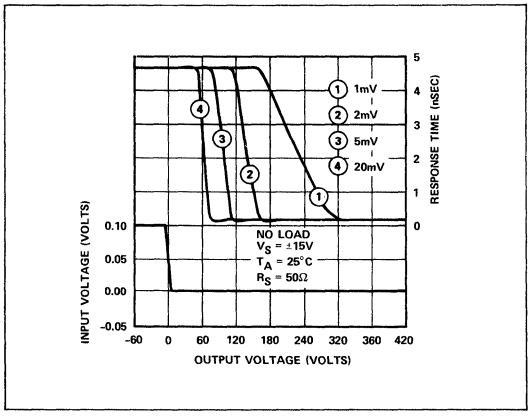


Figure 6. Response Time For 100mV Step and Various Input Overdrives

For 2μs and 1μs designs, the AM686 was selected. It povides 12ns propagation with 2.5mV overdrive, Schottky TTL outputs, and DC input specifications adequate for an 8-bit A/D. Ultra-high speed requires considerable power. Maximum supply currents are 42mA from the +5V supply and 34mA from the −5V supply.

LOGIC CONSIDERATIONS

A single DIP package, the AM2502 Successive Approximation Register, contains the logic for 8-bit A/D converters operating at 2μs or greater conversion times. (Detailed descriptions of A/Ds constructed with the AM2502 and Precision Monolithics DACs are contained in AN-11, available upon request.) A 1μs A/D requires special logic design using Schottky TTL and will be described in the detailed circuit description.

PRACTICAL 3 IC A/Ds

When the required conversion time is ≥2μs, the DAC-08's fast settling time enables very simple and low cost designs. A 4μs design is shown in Figure 7. At additional cost and increased power dissipation, changing the comparator to an AM686 results in a 2μs A/D. Every nanosecond counts in a 1μs A/D, and the circuit necessarily increases in complexity. However, with the DAC-08, Schottky TTL logic, and attention to layout, a 1μs A/D can be constructed at low cost.

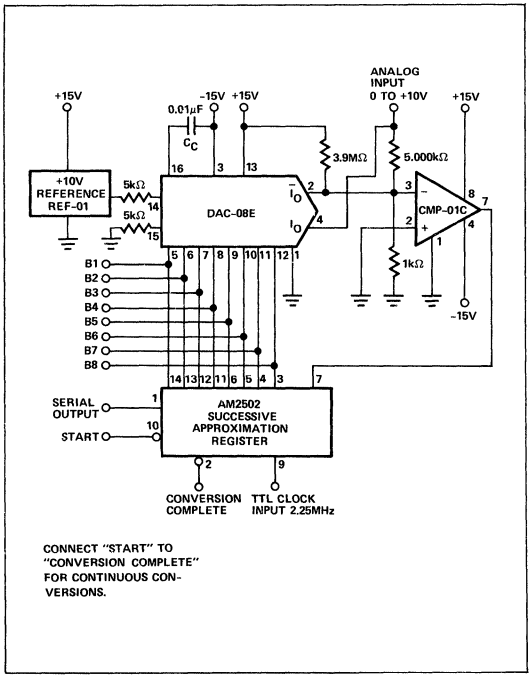
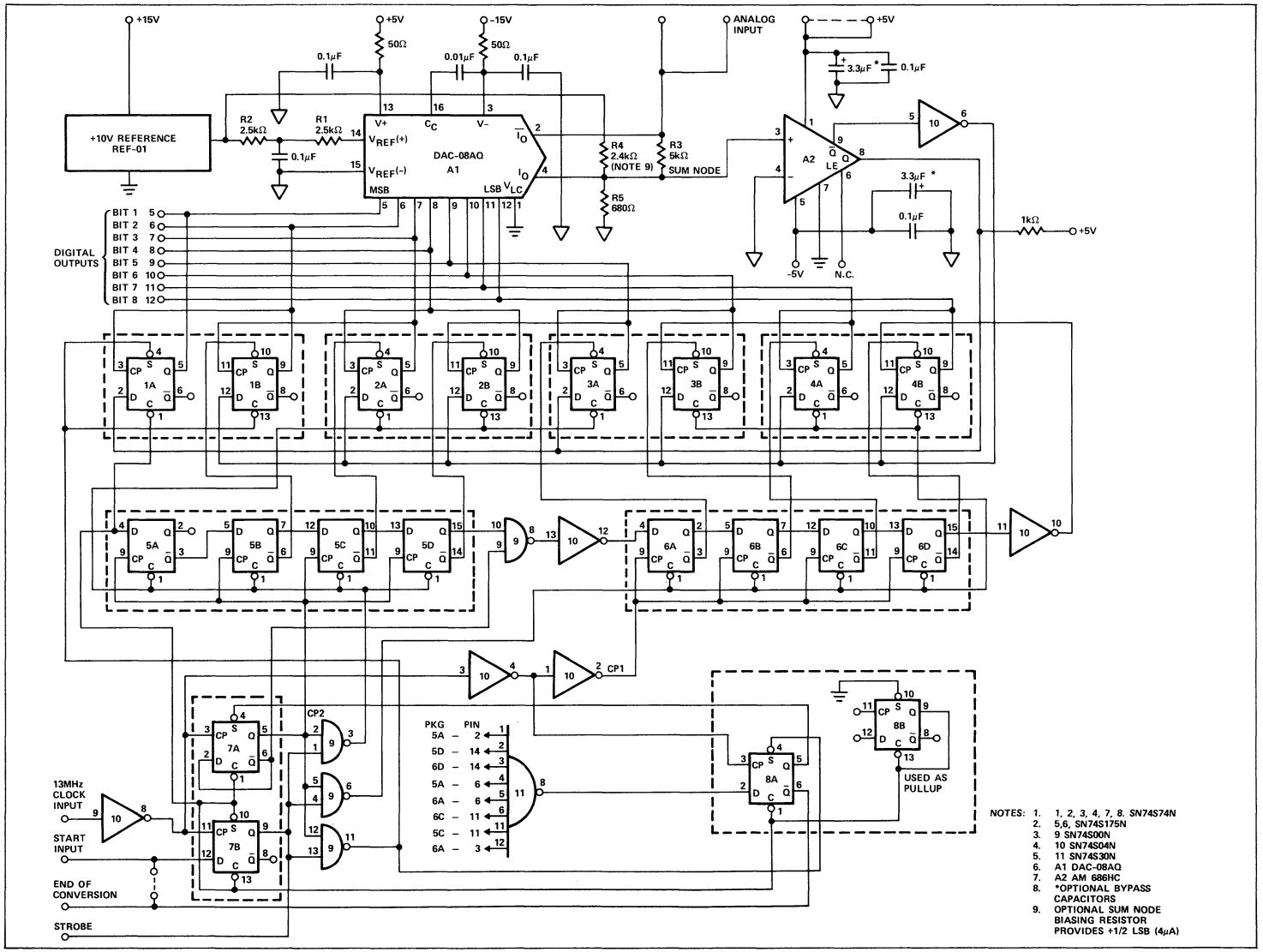


Figure 7. 3 IC Low Cost A/D Converter

ANALOG DESIGN

The DAC-08AQ is useful in this design for several reasons. Its output full scale current is guaranteed to be 1.992mA ±8μA, when a 10.000V reference is connected to a 5.000kΩ resistor in series with Pin 14. In this design, the 5kΩ is split to allow bypassing without capacitively loading the 10 volt source. For slightly higher speed, the total resistance may be reduced to 2.5kΩ, thereby increasing I_O full scale to 3.984mA, allowing a lower sum node resistance and lower RC time constant. (The DAC itself does not settle faster at 4mA full scale current.) The DAC-08A maximum nonlinearity of ±0.1% full scale enables faster settling time to within ±1/2LSB (±0.2% full scale) for each bit trial than would be the case using a DAC with ±0.2% nonlinearity. Using the



NOTES:
1. 1, 2, 3, 4, 7, 8. SN74S74N
2. 5,6, SN74S175N
3. 9 SN74S00N
4. 10 SN74S04N
5. 11 SN74S30N
6. A1 DAC-08AQ
7. A2 AM 686HC
8. *OPTIONAL BYPASS CAPACITORS
9. OPTIONAL SUM NODE BIASING RESISTOR PROVIDES +1/2 LSB (4μA)

Figure 8. Complete Schematic 8-Bit, 1μs A/D

±0.2% nonlinearity DAC-08 or DAC-08E provides cost savings at an overall increase in conversion time. Both true and complementary current outputs are provided, and their summation is always $I_{full\ scale}$. In this design, I_O is connected to the analog input. Since $I_O + I_{\overline{O}}$ is constant, and $I_{\overline{O}}$ flows in R3, the DC input current is constant. Holding the A/D input current constant reduces buffer amplifier output impedance requirements. The buffer amplifier used in this application must have sufficient bandwidth to hold V_{IN} constant during a 1μs A/D conversion.

CALIBRATION AND ACCURACY

In many applications calibration is not required. With a 10.000V reference and ±0.05% tolerance resistors, the worst case full scale error is ±0.15%. The zero scale error is totally dependent upon comparator input offset voltage and input bias current, and, in most cases, it may be tolerated. If the errors are not tolerable, then the following calibration procedure may be used.

Calibration of the A/D is done first at zero scale, then at full scale. The zero transition is set by R4, a resistor connected to the +10 volt reference. For 10V full scale, the desired transition point between a code of 0000 0000 and 0000 0001 is at +20mV (+1/2LSB). With an ideal comparator, R4 would be 2.56mΩ (10 volts/3.9μA). Since comparators are less than ideal, R4 must also cancel out the comparator's input offset errors. With +20mV applied at the analog input and using a low clock rate, select R4 to cause the output code to fluctuate between 0000 0000 and 0000 0001. (Do not install a pot for R2 or R4 since it will increase capacitance and inductance at the sum node.) Full scale is calibrated by applying +9.940V to the analog input and trimming R2 until the output code fluctuates between 1111 1110 and 1111 1111. Alternatively, the reference voltage source may be adjusted for the same effect. This will be a small adjustment due to the DAC-08A's tight output full scale current relationship with the reference voltage. Once calibrated, accuracy is a function of temperature-induced drifts only.

A TYPICAL CONVERSION CYCLE

A conversion is initiated by a high level at the Start input when the input 13mHz clock makes a low to high transition. Approximately 9ns later, the control logic generates a clear and reset pulse (Strobe) which causes several events: the 8 output flip-flops are cleared except for the MSB flip-flop 1 which is set to a "one"; both shift registers are cleared; the DAC has Bit 1 turned on, all others are off. The conditions for the first trial at half scale are now established.

As the DAC output settles, the comparator continuously examines the polarity at its noninverting input. For this case, with zero volts at the analog input, the comparator finds a negative voltage present; its output therefore is low. This low is applied to the "D" inputs of all 8 output flip-flops. Recall that 74S74 flip-flop outputs won't change until they are clocked by a positive transition at their CP inputs. At the time labeled 1 on the CP1 waveform, the reset and clear pulse, Strobe, returns high.

Shift Register Number 1 waits for a positive-going transition of CP2. At 2 time CP2 goes high, transferring a "one" from 9A-Q to 9B-Q; 9B-Q goes low, setting 2-Q high and clocking the comparator's "zero" into the Bit 1 flip-flop. The other six flip-flops do nothing, because they are not clocked. Bit 1's answer is now latched, and Bit 2, 1/4 full scale, is being tried. The process continues with the shift register causing each bit to be tried from Bit 2 to Bit 8. After the Bit 8 decision, the EOC output goes high, indicating that the answer in parallel format is available at the 8-bit outputs.

OUTPUT INTERFACING

In continuous conversion operation, the most common connection, EOC is connected to the Start input. While the answer is available whenever EOC is high, it is convenient to use the positive-going edge of the Strobe output as a clock for two 74S175 quad "D" flip-flops used as an 8-bit storage latch. Since Strobe goes high before another conversion cycle begins, there is ample setup time for the latch; the answer has been steady for over 35ns.

OVERALL DESIGN

Due to the bit settling time range of the DAC-08 from 85ns for Bit 1 to 35ns for Bit 8, progressively decreasing trial-and-decision periods would be ideal. Practically, such a timing sequence is difficult to generate at low cost, so a compromise was made: The first four bits allow 160ns for each trial-and-decision, while the last four bits allow 80ns. This may be seen in the waveforms of Figure 9. The timing sequence is generated by shifting a "one" through two shift registers with in-phase clocks, one at 6.5mHz derived from the other at 13mHz.

Standard 74 Schottky TTL logic was selected for speed, compatibility with the AM686 comparator, ready availability, and price.

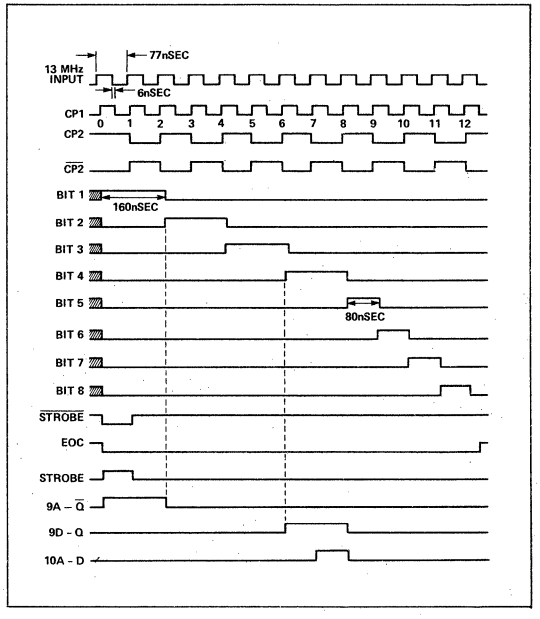


Figure 9. Timing Waveforms with Zero Volts Input

A useful characteristic of the DAC-08 is its capability to directly interface with all popular logic families including TTL, CMOS, and ECL. For this design the DAC-08's logic control pin (Pin 1) is grounded to provide the proper TTL logic threshold. A design utilizing ECL could provide slightly faster conversion time at increased power consumption.

LOGIC DESIGN

The primary logic design element is the 74S series positive-edge-triggered "D" flip-flop. This type of flip-flop is useful in A/D designs because of several properties:

1. The propagation delay from Set to Q going high is only 3ns.
2. The information on the D input is transferred to the Q output only at a positive-going edge of CP.
3. Changes at the D input (comparator settling changes) are ignored when CP is in a steady state.

74S74 dual "D" flip-flops are used for the 8 output latches and for the control logic, and 74S175 quad "D" flip-flops are used for the two shift registers.

Flip-flops 2 through 8 in the simplified schematic (Figure 10) perform two functions. Typical operation can be understood by examining the operation of Flip-Flop 2. When set by an input from Shift Register Number 1, the Q output of Flip-Flop Number 2 goes high, which starts the trial of Bit 2 and acts as a clock which is the result of Trial 1, to Q of Flip-Flop 1. This basic connection, using the beginning of a new trial to clock the previous bit trial, is used on all eight output flip-flops. The start of each bit trial is precisely coincident with clocking of the previous bit answer; so no time is wasted, and logic delays are reduced to setup times only.

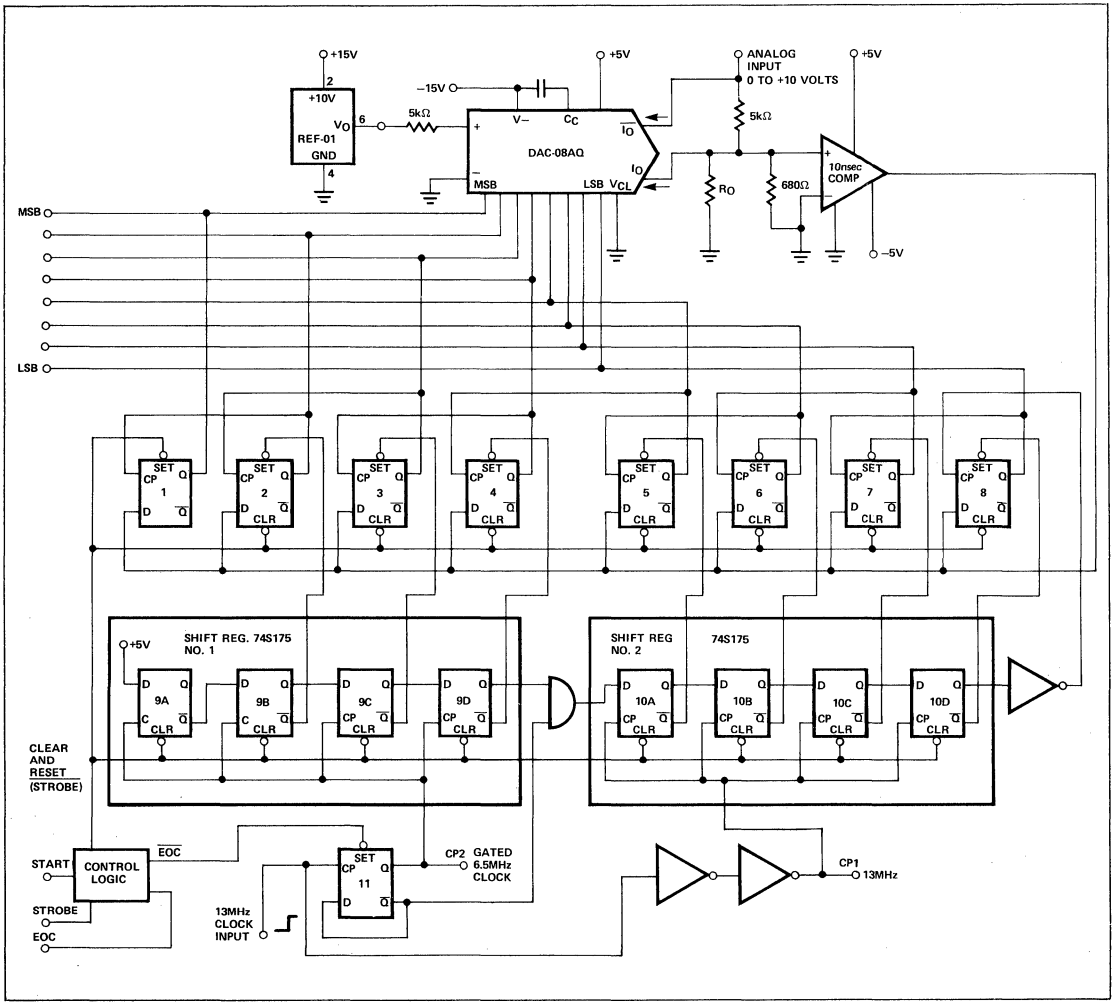


Figure 10. Simplified Schematic 1μs A/D

PRINTED CIRCUIT BOARD LAYOUT RULES

For A/D designs generally, and high speed designs in particular, layout is important. Some of the more important rules are listed below:

1. Digital ground must be separated from analog ground; they must meet at only one common point.
2. Digital traces should not cross or be routed near sensitive analog areas; this is especially important near the sum node.
3. With Schottky TTL logic, the digital ground and V_{CC} traces should be large and contain provisions for generous bypassing.
4. The trace from the DAC output to comparator input (sum node) should be short, and it should be guarded by analog ground.
5. All analog components should be located as close as possible to the edge connector so that the input analog traces will be short.
6. The comparator's outputs should be routed away from its inputs, to minimize capacitive coupling and possible oscillation.

SYSTEM CONSIDERATIONS

Typical system connections ar shown in Figure 11. Digital grounds and analog grounds meet at one point only keeping large power supply return currents away from the sensitive analog ground portion of the A/D system. Start is connected to EOC for continuous conversions, and Strobe is used to clock the parallel answer into an output register at the end of each conversion.

CONCLUSION

The DAC-08 High Speed Monolithic D/A Converter greatly simplifies construction of high speed A/D converters. Designs using only three ICs achieve 2μs conversions, and 1μs conversion can be attained with additional logic. Techniques have been presented which allow the user to construct low cost, high speed A/D converters.

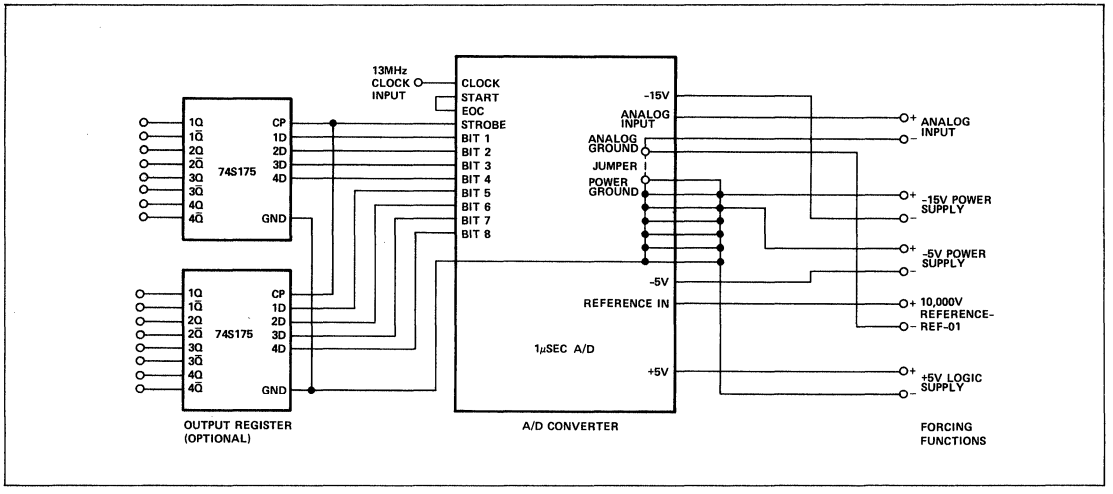


Figure 11. Typical System Connection

APPLICATION NOTE 17

DAC-08 APPLICATIONS COLLECTION

By John Schoeff and Donn Soderquist

GENERAL DESCRIPTION

There has been a trend in recent years toward providing totally dedicated digital-to-analog converters with limited applications versatility. This application note describes a new type of monolithic DAC designed for an extremely broad range of applications, the Precision Monolithics DAC-08.

Several unique design features of this low-cost DAC combine to provide total applications flexibility. Principal among them are: dual complementary, true current outputs; universal logic inputs capable of interfacing with any logic family; 85ns settling time; high-speed multiplying capability; and finally, the ability to use any standard system power supply voltages. A description of these features is given followed by specific applications using each feature.

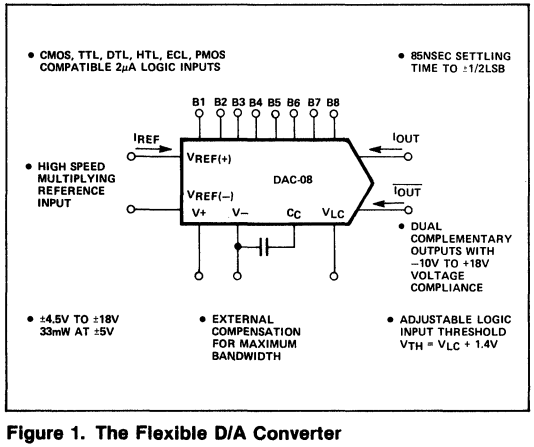


Figure 1. The Flexible D/A Converter

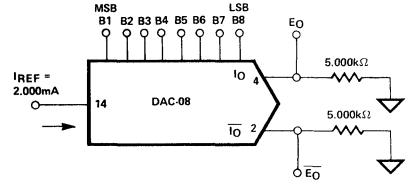
OUTPUT

HIGH VOLTAGE COMPLIANCE CURRENT OUTPUTS

Many older current-output DACs actually have resistive outputs which must be terminated in a virtual ground. The DAC-08, however, is a true digitally-controlled current source with an output impedance typically exceeding 20MΩ.

Its outputs can swing between −10V and +18V with little or no effect on full-scale current or linearity. Some of the applications that require high output voltage compliance include:

1. Precise current transmission over long distances.
2. Programmable current sources.
3. Analog meter movement driving.
4. Resistive termination for a voltage output without an op amp.
5. Capacitive termination for digitally-controlled integrators.
6. Inductive termination with balanced transformers, transducers and headsets.



	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	I_O mA	E_O	E_O
FULL SCALE −1LSB	1	1	1	1	1	1	1	1	1.992	0.000	−9.960	0.000
FULL SCALE −2LSB	1	1	1	1	1	1	1	0	1.984	0.008	−9.920	− 0.40
HALF SCALE +LSB	1	0	0	0	0	0	0	1	1.008	0.984	−5.040	−4.920
HALF SCALE	1	0	0	0	0	0	0	0	1.000	0.992	−5.000	−4.960
HALF SCALE −LSB	0	1	1	1	1	1	1	1	0.992	1.000	−4.960	−5.000
ZERO SCALE +LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.040	−9.920
ZERO SCALE	0	0	0	0	0	0	0	0	0.000	1.992	0.000	−9.960

Figure 2. Basic Unipolar Negative Operation

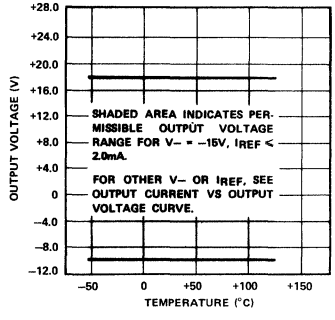


Figure 3. Output Voltage Compliance vs Temperature

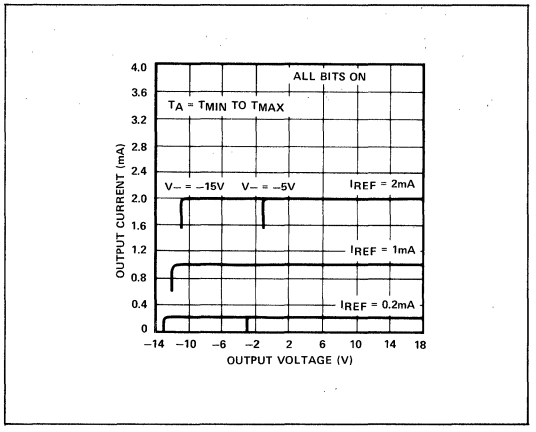
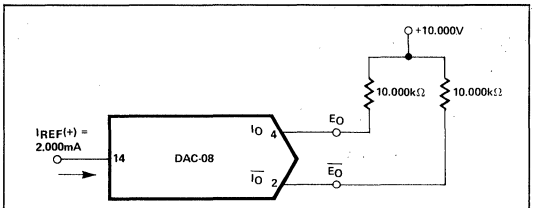
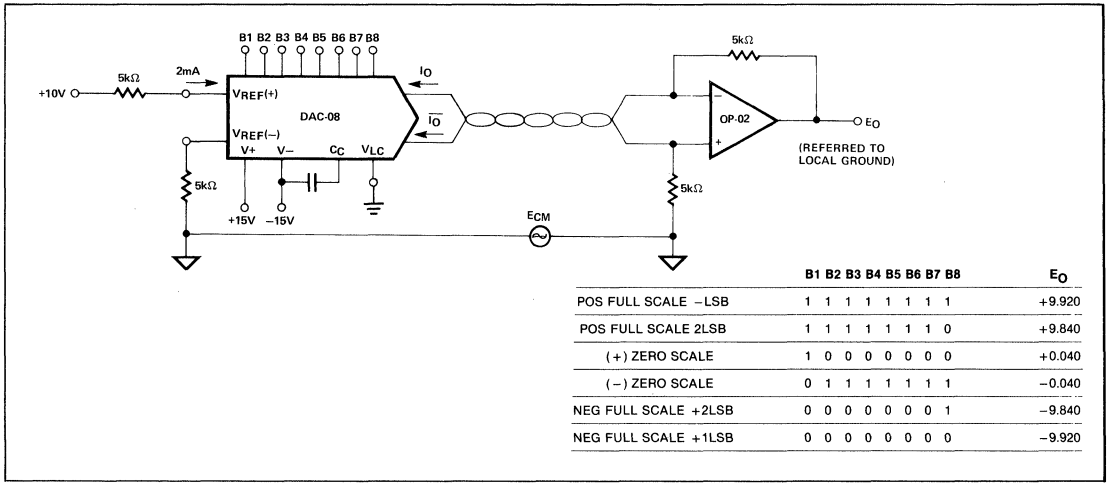


Figure 4. Output Current vs Output Voltage (Output Voltage Compliance)



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	E_O
POS FULL SCALE –LSB	1	1	1	1	1	1	1	1	– 9.920	+10.000
POS FULL SCALE 2LSB	1	1	1	1	1	1	1	0	– 9.840	+ 9.920
ZERO SCALE +LSB	1	0	0	0	0	0	0	1	– 0.080	+ 0.160
ZERO SCALE	1	0	0	0	0	0	0	0	0.000	+ 0.080
ZERO SCALE –LSB	0	1	1	1	1	1	1	1	+ 0.080	0.000
NEG FULL SCALE +LSB	0	0	0	0	0	0	0	1	+ 9.920	– 9.840
NEG FULL SCALE	0	0	0	0	0	0	0	0	+10.000	– 9.920

Figure 5. Basic Bipolar Output Operation



	B1	B2	B3	B4	B5	B6	B7	B8	E_O
POS FULL SCALE –LSB	1	1	1	1	1	1	1	1	+9.920
POS FULL SCALE 2LSB	1	1	1	1	1	1	1	0	+9.840
(+) ZERO SCALE	1	0	0	0	0	0	0	0	+0.040
(–) ZERO SCALE	0	1	1	1	1	1	1	1	–0.040
NEG FULL SCALE +2LSB	0	0	0	0	0	0	0	1	–9.840
NEG FULL SCALE +1LSB	0	0	0	0	0	0	0	0	–9.920

Figure 6. High Noise Immunity Current to Voltage Conversion

DUAL COMPLEMENTARY OUTPUTS

Convertional DACs have a single output, so they cannot drive balanced loads and are limited to a single input code polarity. The DAC-08 was designed to overcome these limitations.

Input coding of positive binary or complementary binary is obtained by a choice of outputs, I_O for positive-true or $\overline{I_O}$ for negative-true. In many applications both are used either independently or in combination. Dual comlementary outputs allow some very unusual and useful DAC applications:

1. CRT display driving without transformers.
2. Differential transducer control systems.
3. Differential line driving.
4. High-speed waveform generation.
5. Digitally controlled offset nulling of op amps.

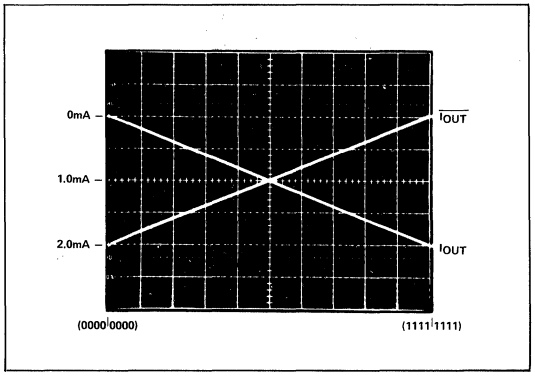


Figure 7. True and Complementary Output Operation

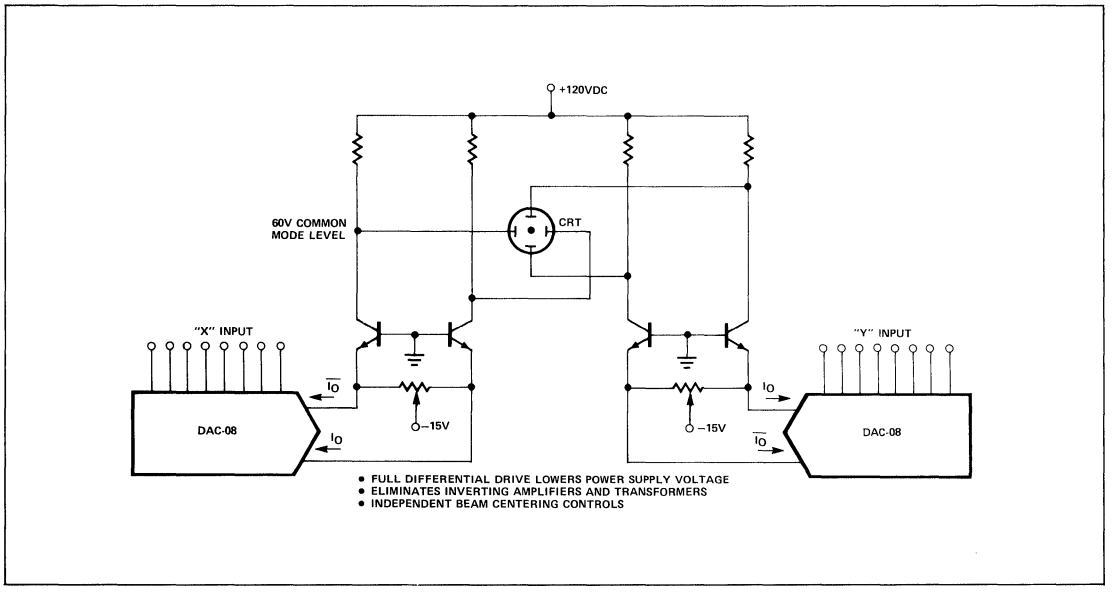


Figure 8. CRT Display Driver

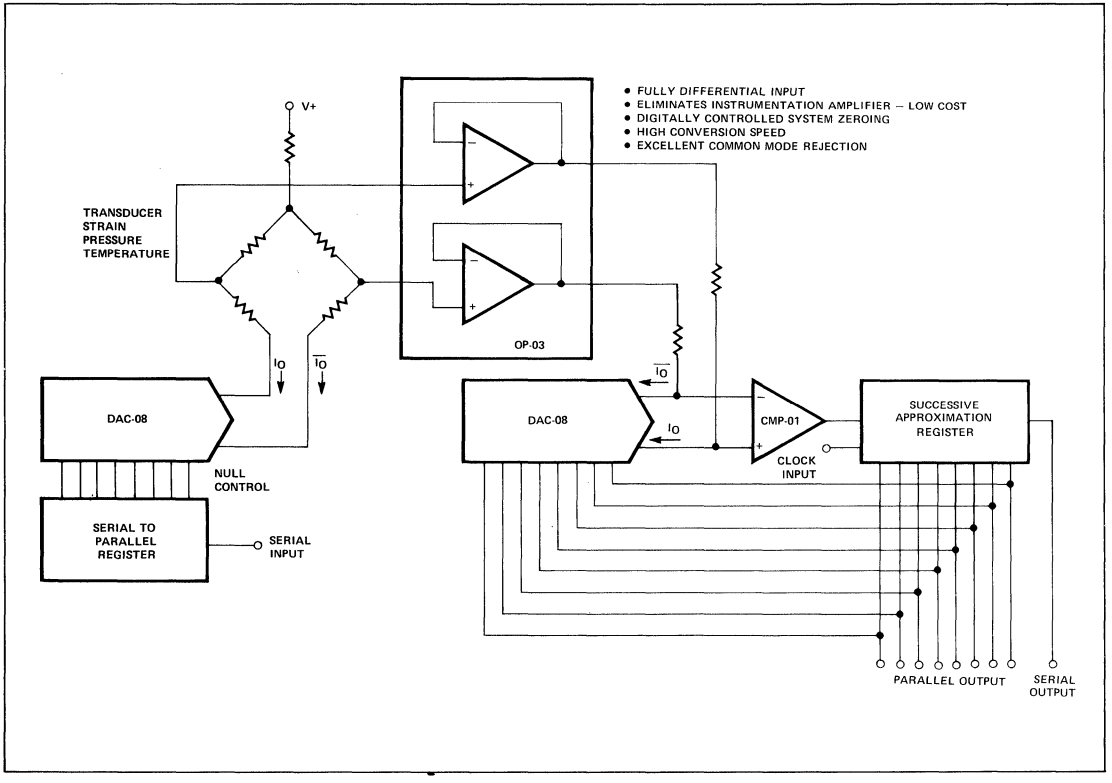


Figure 9. Bridge Transducer Control System with Full Differential Input

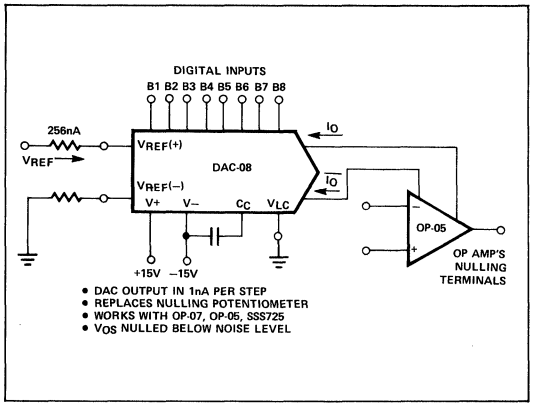


Figure 10. Digitally Controlled Offset Nulling

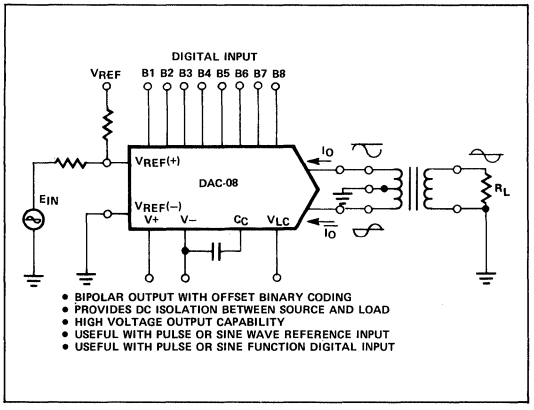


Figure 11. Balanced Transformer Drive

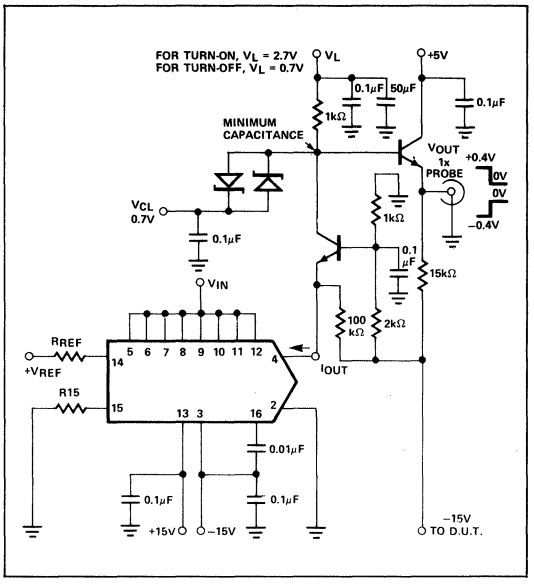


Figure 12. Settling Time Measurement Circuit

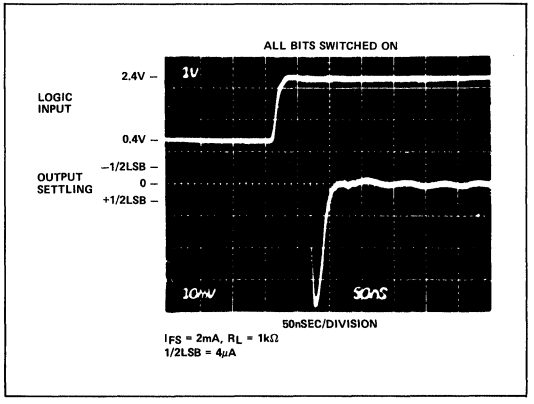


Figure 13. Full Scale Settling Time

HIGH SPEED

Sub-microsecond settling times are common in current-output DACs. Many DACs settle in 500ns; 300ns is not unusual. But 85ns settling time for a low-cost DAC is exceptional, and this characteristic allows the use of the DAC-08 in formerly difficult and expensive-to-build applications:

1. 1μs, 2μs and 4μs A/Ds. (These are completely described in AN-16, available upon request.)
2. 15MHz Tracking A/Ds.
3. ECL compatible applications.
4. Video displays requiring a low-glitch DAC.
5. Radar pulse height analysis system.

LOGIC INPUTS

ADJUSTABLE INPUT LOGIC THRESHOLD

Most DACs have TTL or CMOS compatible inputs which require complicated interfaces for use with ECL, PMOS, NMOS or HTL logic. By contrast, the DAC-08, with typical logic input current of 2μA and an adjustable input logic threshold, interfaces easily with any logic family in use today. The logic input threshold is 1.4V positive with respect to Pin 1; for TTL Pin 1 is therefore grounded; for other families Pin 1 is connected as shown in the interfacing figure. An adjustable threshold and a −10V to +18V input range greatly simplify system design especially with other-than-TTL logic. The circuits shown in c and d provide a $2V_{BE}$ V_{LC} compensation to minimize temperature drift.

1. ECL applications without level translators.
2. Direct interfaces with Hi-Z RAM outputs.
3. CMOS applications without static discharge considerations.
4. HTL or HNIL applications without level translators.
5. System size, weight, and cost reduction.

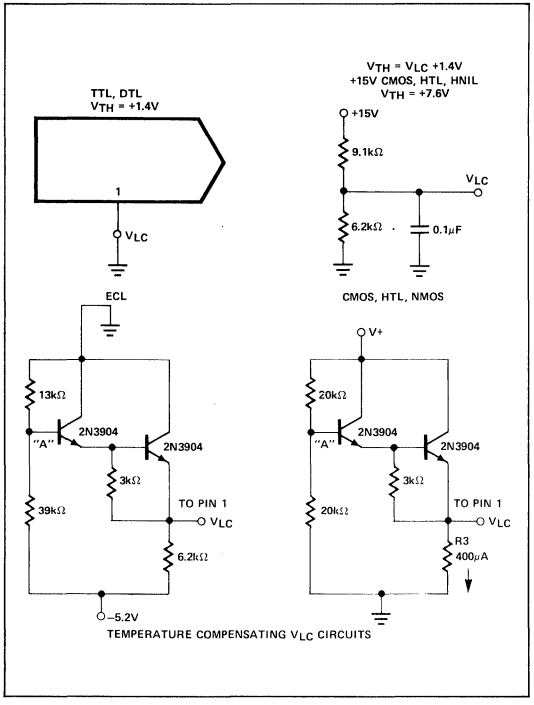


Figure 14. Interfacing with Various Logic Families ($V_{TH} = V_{LC} + 1.4V$)

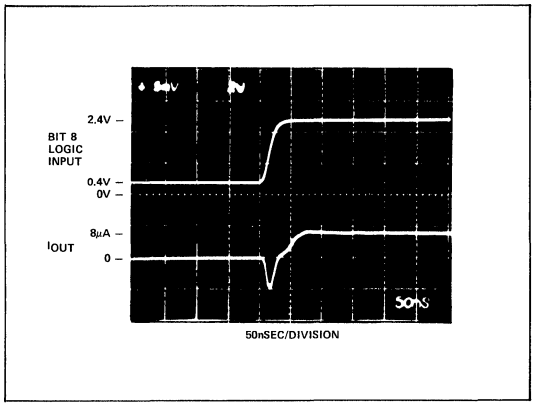


Figure 16. LSB Switching

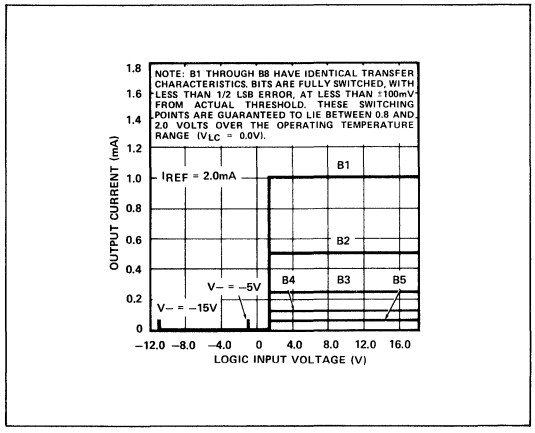


Figure 17. Bit Transfer Characteristics

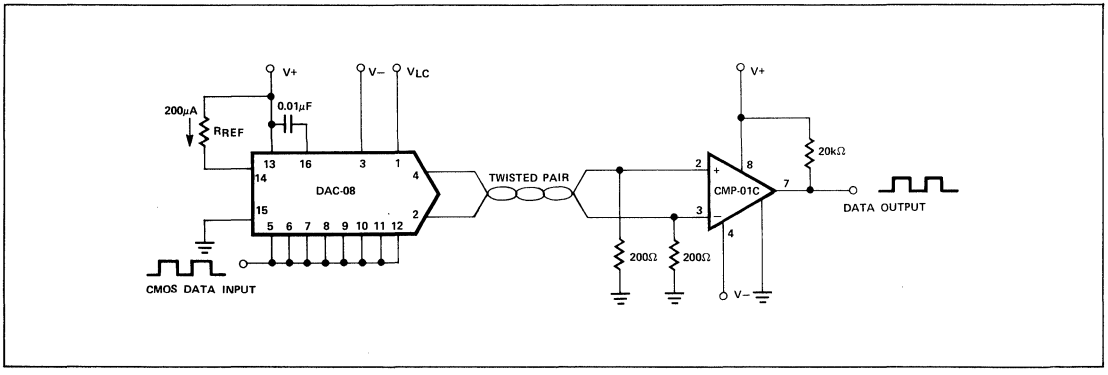


Figure 15. CMOS Differential Line Driver/Receiver

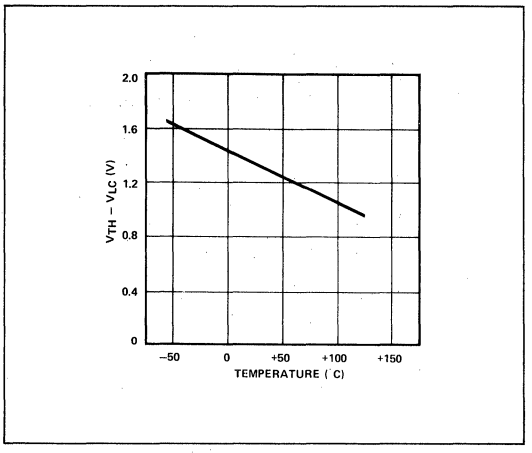


Figure 18. $V_{TH} - V_{LC}$ vs Temperature

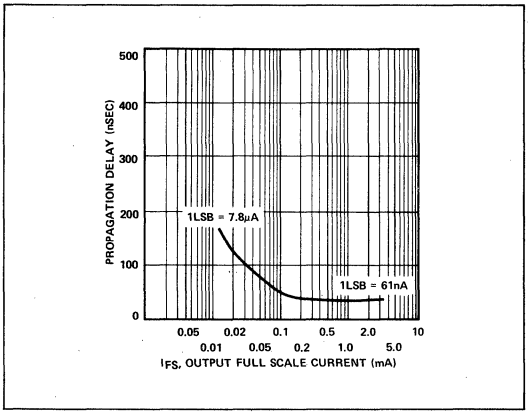


Figure 19. LSB Propogation Delay vs I_{FS}

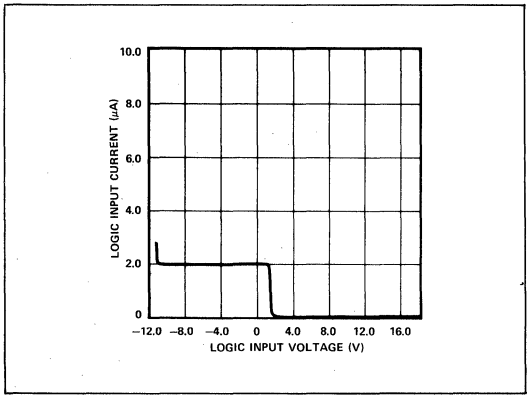


Figure 20. Logic Input Current vs Input Voltage

REFERENCE INPUTS

MULTIPLYING CAPABILITY

Fixed internal references are included in many DACs, but they limit the user to non-multiplying, single-polarity reference applications and do not allow a single-system reference. To achieve the design goals of low cost and total applications flexibility, the DAC-08 uses an external reference. Positive or negative references may be applied over a wide common-mode voltage range. In addition, the full-scale current is matched to the reference current eliminating calibration in most applications.

1. Digitally controlled full-scale calibration.
2. 8 x 8 multiplication of two digital words.
3. Digital Attenuators/Programmable gain amplifiers.
4. Modem transmitters to 1MHz.
5. Remote shutdown and party line DAC applications.

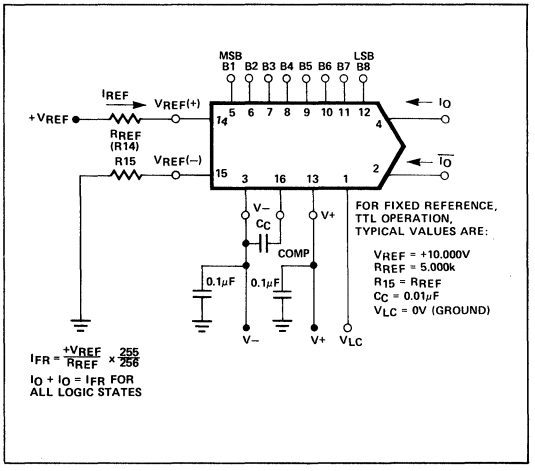


Figure 21. Basic Positive Reference Operation

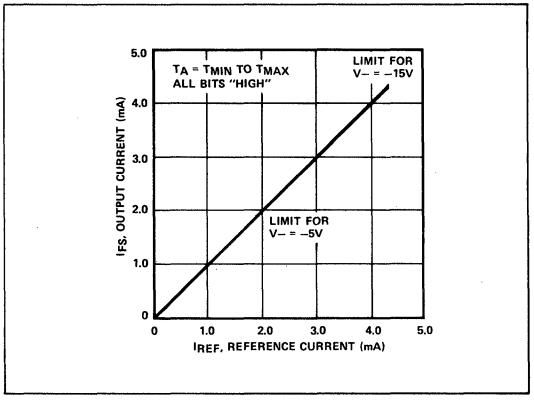


Figure 22. Full-Scale Current vs Reference Current

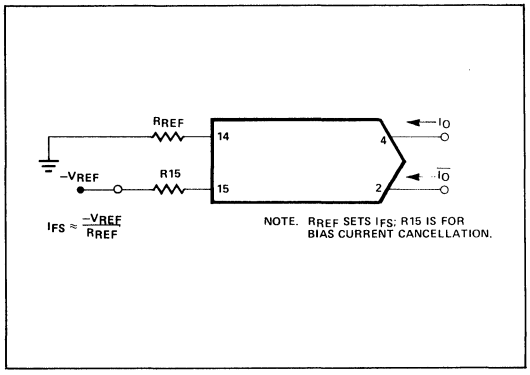


Figure 23. Basic Negative Reference Operation

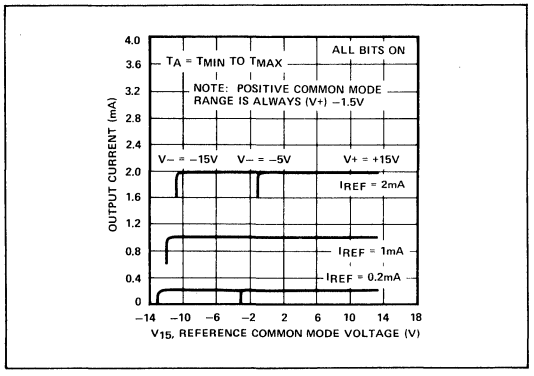


Figure 24. Reference Amp Common-Mode Range

HIGH SPEED

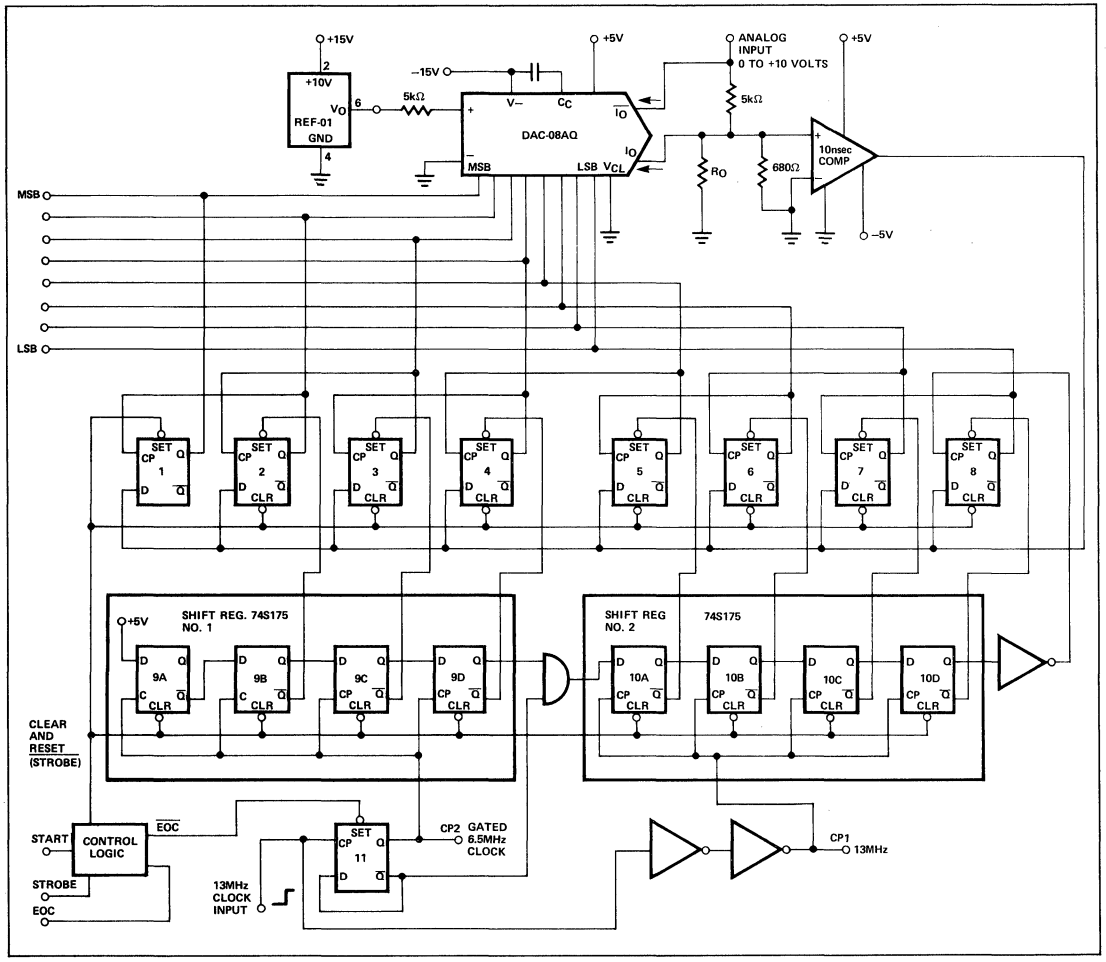
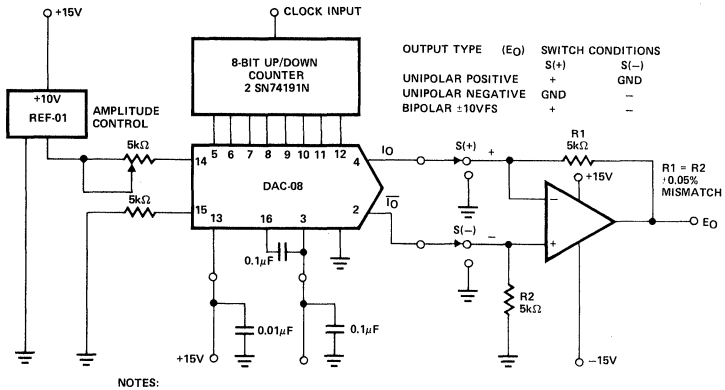


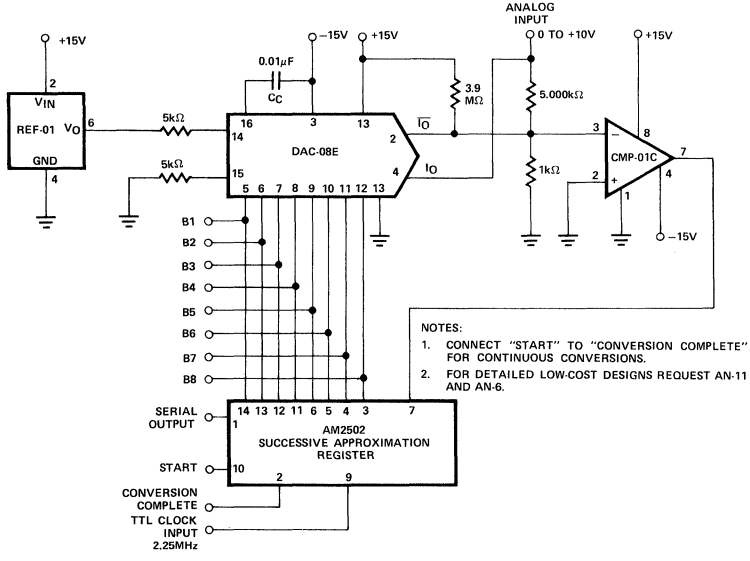
Figure 25. Simplified Schematic 1μs A/D



NOTES:

1. BIPOLAR OUTPUT IS SYMMETRICAL AROUND ZERO. ADJUSTABLE PEAK-TO-PEAK AMPLITUDE.
2. FOR TRIANGLE WAVE, COUNT UP TO FULL REVERSE AND COUNT DOWN.
3. FOR POSITIVE-GOING SAWTOOTH, COUNT UP TO FULL CLEAR, REPEAT.
4. FOR NEGATIVE-GOING SAWTOOTH, COUNT DOWN. CLEAR REPEAT.
5. FOR OTHER WAVEFORMS, USE A ROM PROGRAMMED WITH THE DESIRED FUNCTION.
6. 85nSEC SETTLING TIME PERMITS WAVEFORM PERIOD OF 25.6μSEC OR 39kHz REPETITION RATE IN THE UNIPOLAR POSITIVE MODE.

Figure 26. High-Speed Waveform Generator



NOTES:

1. CONNECT "START" TO "CONVERSION COMPLETE" FOR CONTINUOUS CONVERSIONS.
2. FOR DETAILED LOW-COST DESIGNS REQUEST AN-11 AND AN-6.

Figure 27. Four IC Low-Cost A/D Converter

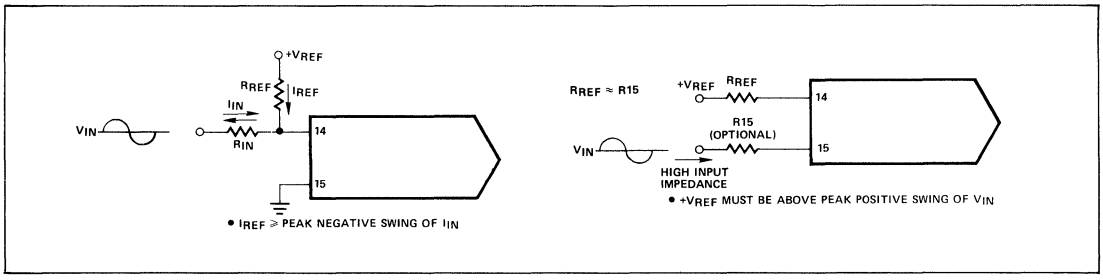


Figure 28. Accommodating Bipolar References

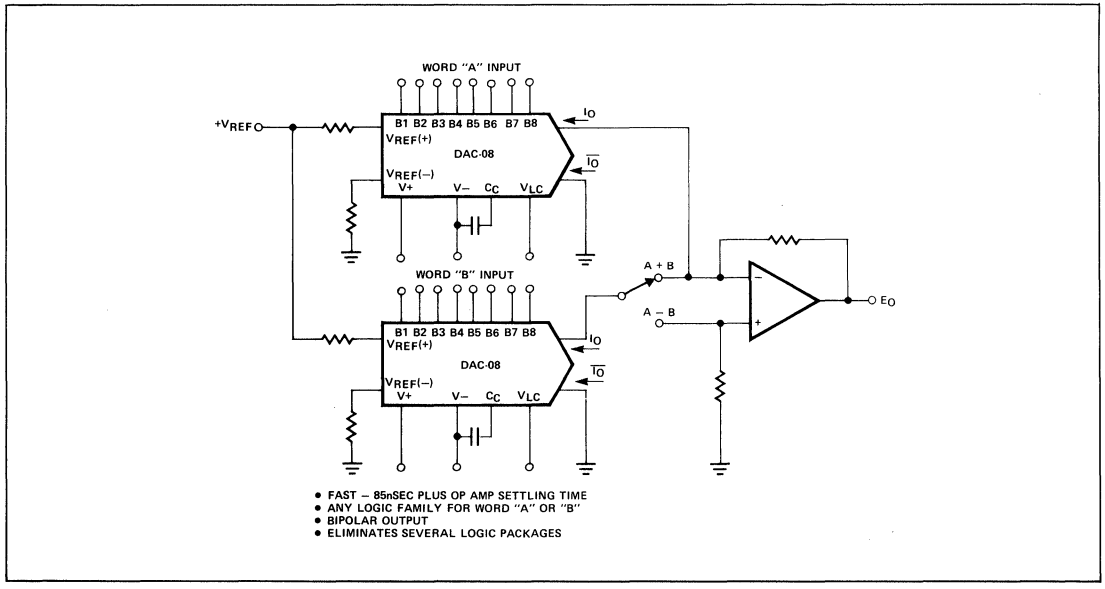


Figure 29. Digital Addition or Subtraction with Analog Output

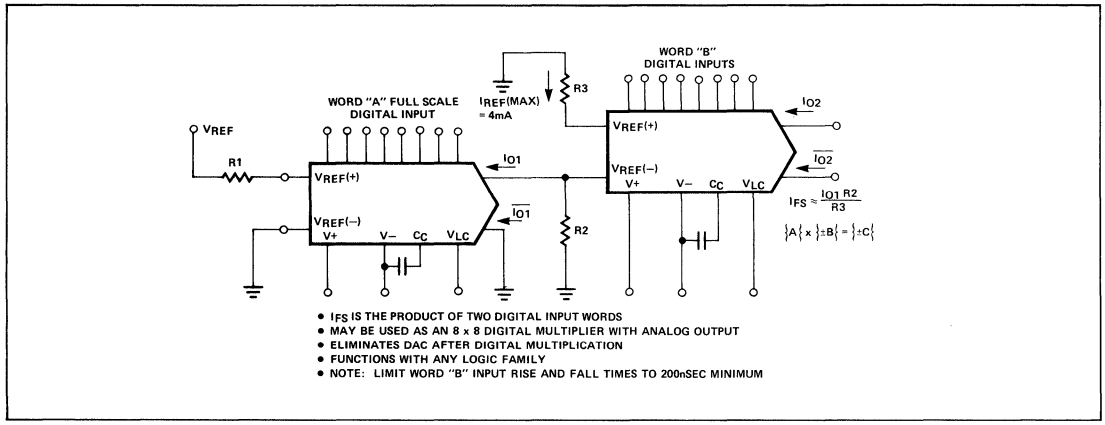


Figure 30. Digitally Controlled Full-Scale Calibration (Multiplier)

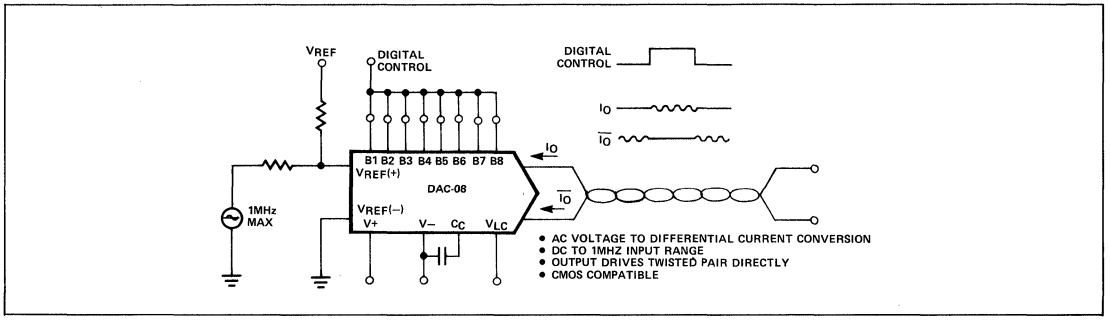


Figure 31. Modem Transmitter

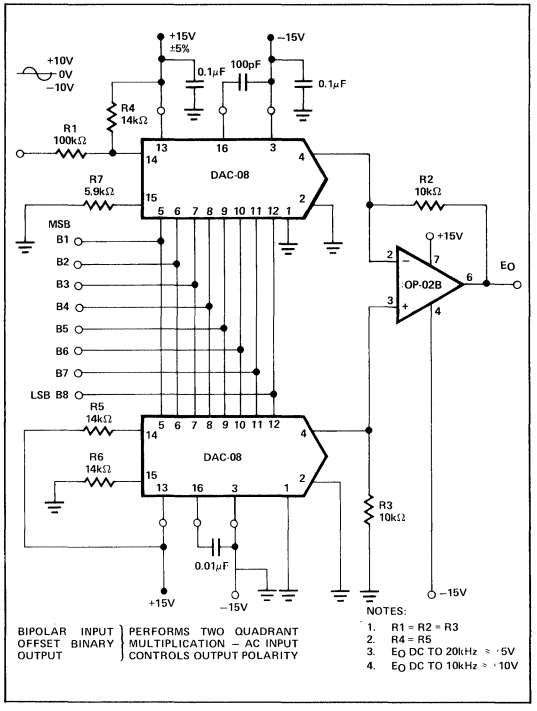


Figure 32. DC-Coupled Digital Attenuator/ Programmable Gain Amplifier

POWER SUPPLIES

POWER SUPPLY REQUIREMENTS

The DAC-08 works with ±4.5V to ±18V supplies allowing use with all standard digital and analog system supply voltages plus most battery voltages. With only 33mW of power dissipation at ±5V and 85ns settling time, it has a lower speed power product than CMOS DACs. Power dissipation is almost constant over temperature, and bypassing is accomplished with 0.01μF capacitors — no large electrolytics are required. These power supply requirements allow:

1. Battery operation.
2. Use of unregulated or poorly regulated power supplies.
3. Use in space-limited areas due to small bypass capacitors.
4. Use in constant power dissipation applications.
5. Common digital and analog power supplies.

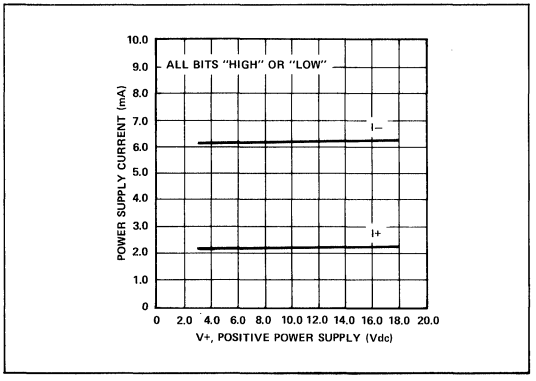


Figure 33. Power Supply Current vs V+

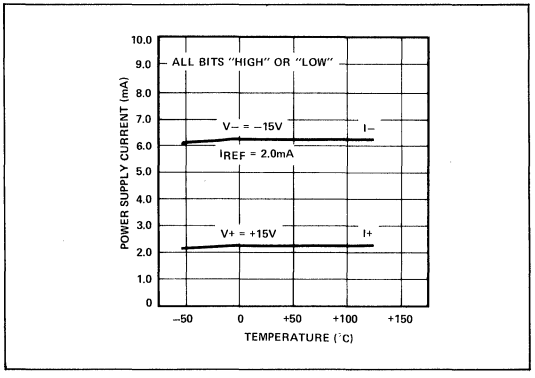


Figure 34. Power Supply Current vs Temperature

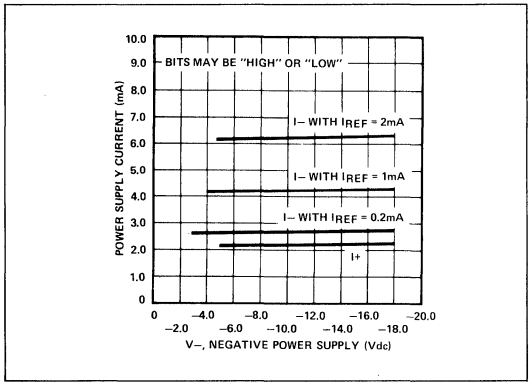


Figure 35. Power Supply Current vs V–

OTHER APPLICATIONS

MICROPROCESSOR APPLICATIONS

The ability to use μP power supply voltages and the ability to interface with any logic family make the DAC-08 especially useful in μP applications:

1. Tracking A/D converters.

2. Successive approximation A/D converters.

3. Direct drive from Hi-Z MOS RAM outputs.

By programming the ROMs with the successive approximation or the tracking A/D algorithm, all of the logic for A/D conversion is contained in the μP. This is a very inexpensive approach, since there is no need for the usual A/D conversion logic packages.

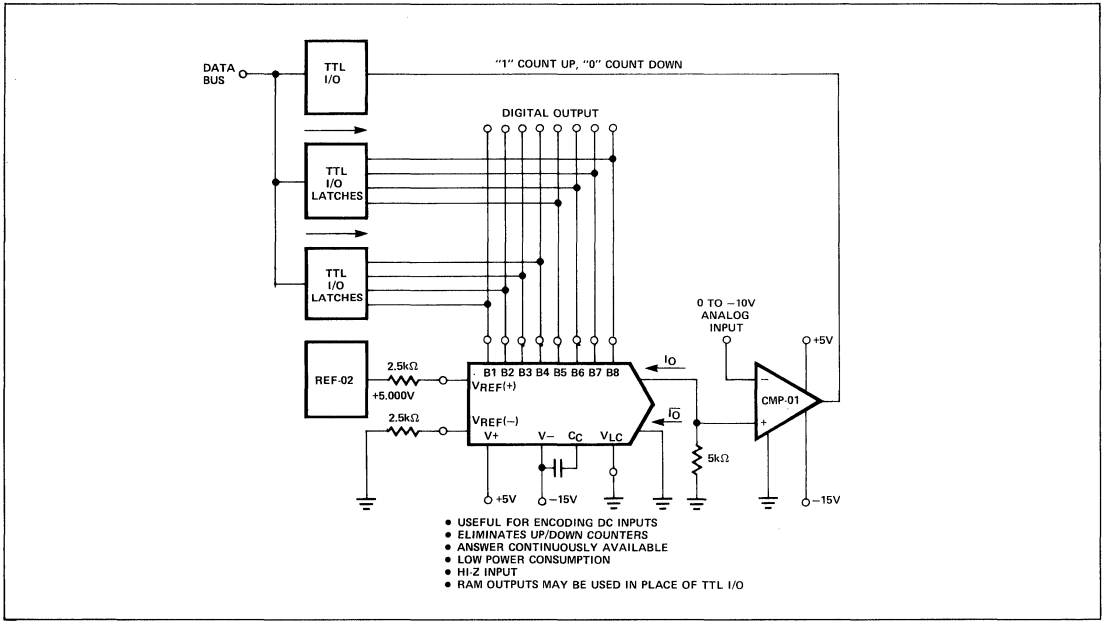


Figure 36. Microprocessor Controlled Tracking A/D Converter

CONCLUSION

High voltage compliance complementary current outputs, universal logic inputs and multiplying capability make the Precision Monolithics DAC-08 the most versatile monolithic high-speed DAC available today.

APPLICATION NOTE 18

THERMOMETER APPLICATIONS OF THE REF-02

By George Erdi

INTRODUCTION

This application note describes electronic thermometer applications of the REF-02 +5V Voltage Reference where the voltage output is a direct measurement of temperature in °C or in °F. These applications use the predictable 2.1mV/°C TEMP output voltage temperature coefficient of the REF-02, a byproduct of a bandgap voltage reference design. Thermometer applications are described first followed by a discussion of bandgap voltage reference theory.

THERMOMETER ESSENTIALS

In addition to a highly linear temperature sensitive component, electronic thermometers should have the following characteristics:

1. Convenient scaling such as 10mV/°C, 100mV/°C, or 10mV/°F.
2. Direct voltage readings such as −0.55V at −55°C, 0V at 0°C, and +1.25V at +125°C.
3. Room temperature calibration.

BASIC CIRCUIT IMPLEMENTATION

The simplified schematic in Figure 1 shows the basic thermometer connections. An operational amplifier, three resistors, and the +5.000V output of the REF-02 function together to level shift and amplify V_{TEMP} allowing V_{OUT} to read in the desired manner. The expression for V_{OUT} is:

$$1.\ V_{OUT} = \left(1 + \frac{R_c}{R_a \| R_b}\right) V_{TEMP} - \frac{R_c}{R_a} (V_{REF})$$

The first term is the gain of the circuit with V_{REF} equal to 0V; the second term is the gain of the circuit with V_{TEMP} equal to 0V. Differentiating Equation 1 with respect to temperature gives the slope, S, of the output-versus-temperature curve:

$$2.\ \frac{dV_{OUT}}{dT} = S = m\left(1 + \frac{R_c}{R_a \| R_b}\right)$$

$$= 2.1\text{mV/°C}\left(1 + \frac{R_c}{R_a \| R_b}\right)$$

where $m = TCV_{TEMP}$

Thus, the ratio of R_c to $R_a \| R_b$ sets the slope of V_{OUT}, and the ratio of R_c to R_a and V_{REF} set the initial output value at 25°C. Table 1 lists typical scaling ratios for different output scales.

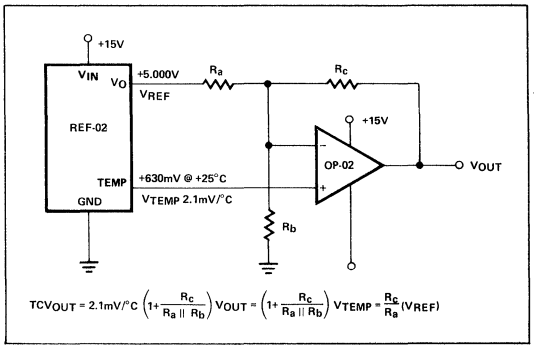


Figure 1. Simplified Schematic

Table 1. Temperature Scaling Ratios

$V_{REF} = 5.000V, V_{TEMP} = 630mV @ 25°C, TCV_{TEMP} = 2.1mV/°C$

V_{OUT}@25°C (77°F)	TCV_{OUT} (Slope)	$\frac{R_c}{R_a}$	$\frac{R_c}{R_a \| R_b}$
250mV	10mV/°C	0.55	3.76
2.5V	100mV/°C	5.50	46.6
770mV	10mV/°F	0.926	7.57

COMPLETE CIRCUIT

Two potentiometers, R_p and R_{bp}, have been added to the circuit for precise calibration and to allow for the ±1% resistor tolerances. V_{REF} is adjusted by R_p to set the V_{OUT} value at +25°C (77°F); the ratio of R_c to $R_a \| R_b$ is adjusted by R_{bp} to set the slope of V_{OUT} versus temperature. Resistor values for typical output scales are shown in Table 2.

Table 2. Resistor Values

TCV_{OUT} SLOPE(S)	10mV/°C	100mV/°C	10mV/°F
TEMPERATURE RANGE	−55° to +125°C	−55° to +125°C	−67°F to +257°F
OUTPUT VOLTAGE RANGE	−0.55V to +1.25V	−5.5V to +12.5V*	−0.67V to +2.57V
ZERO SCALE	0V@0°C	0V@0°C	0V@0°F
R_a (±1% resistor)	9.09kΩ	15kΩ	8.25kΩ
R_{b1} (±1% resistor)	1.5kΩ	1.82kΩ	1.0kΩ
R_{bp} (potentiometer)	200Ω	500Ω	200Ω
R_c (±1% resistor)	5.11kΩ	84.5kΩ	7.5kΩ

*For 125°C operation, the op amp output must be able to swing to +12.5V; increase V_{IN} to +18V from +15V if this is a problem.

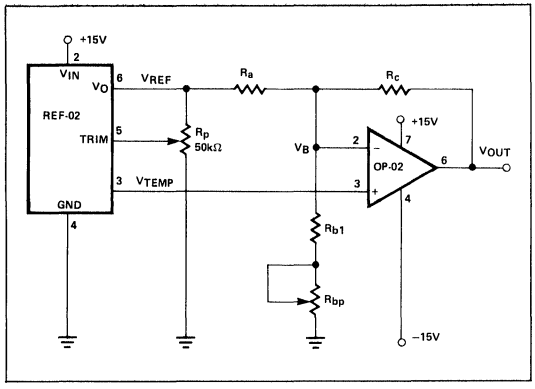


Figure 2. Complete Schematic

CALIBRATION CONDITIONS

All calibration is conducted in free air. Heatsinking of the REF-02 is unnecessary and is undesirable. The small (2°C) rise in chip temperature of the REF-02 above ambient temperature serves as an error-cancelling factor of some second order effects internal to the REF-02 design. The calibration procedure which follows assumes free air — no heatsinking — calibration.

CALIBRATION PROCEDURE

Calibration is performed at ambient temperature with two adjustments using the following procedure:

Step 1: Measure and record V_{TEMP} and T_A in °C.

Step 2: Calculate the calibration ratio "r" using Equation 3:

$$3.\ r \equiv \frac{R_a \| R_b}{R_c + R_a \| R_b} = \frac{V_{TEMP} \text{ in mV}}{S(T_A + 273)}$$

Where S = TCV_{OUT}, T_A = ambient temperature in °C

Step 3: Turn power off, short V_{REF} terminal to ground, and apply a precise 100mV to the V_{OUT} terminal.

Step 4: Adjust R_{bp} so that $V_B = r(100mV)$; remove short.

Step 5: Turn power on; adjust R_p so that V_{OUT} equals the correct value at ambient temperature.

The system is now calibrated.

CALIBRATION EXAMPLE

Here is an example at $T_A = 25°C$, $S = 10mV/°C$, and $V_{TEMP} = 632mV$:

Step 1: $V_{TEMP} = 632mV$, $T_A = 25°C$.

Step 2: Using Equation 3:

$$r = \frac{V_{TEMP}}{S(T_A + 273)} = \frac{632}{10(25 + 273)} = \frac{632}{2980} = 0.2121$$

Step 3: Apply 100.00mV to V_{OUT} with power off and V_{REF} connected to ground.

Step 4: Adjust R_{bp} so that $V_B = r(100mV) = 21.21mV$.

Step 5: Turn power on and adjust R_p so that V_{OUT} equals +0.25V.

The system is now calibrated.

TRANSDUCER ERROR FACTORS

Error terms are threefold:

1. Slope errors — Deviations from nominal slope. For example, if the slope is 10.04mV/°C instead of 10.00mV/°C, the accuracy due to the slope error is 0.4%.
2. Linearity errors — Deviations in V_{TEMP} versus temperature from straight line performance, a change in V_{TEMP} slope with temperature.
3. Offset error — V_{OUT} deviations due to changes in V_{REF} with temperature.

Since these errors are grade dependent, Table 3 is provided as an aid in specifying the correct combination of components for a given application. Offset error can be eliminated by using one REF-02 as a temperature sensor only and another REF-02 (operated at a constant temperature) as V_{REF}.

Table 3. Typical Transducer Performance vs Grade

GRADE / PARAMETER	REF-02A	REF-02	REF-02E	REF-02H	REF-02C
TEMPERATURE RANGE	−55° to +125°C	−55° to +125°C	0° to +70°C	0° to +70°C	0° to +70°C
SLOPE ERROR	±0.30%	±0.40%	±0.25%	±0.35%	±0.45%
TCV_{TEMP} ERROR	±0.10%	±0.12%	±0.08%	±0.10%	±0.15%
OFFSET ERROR	±0.15%	±0.40%	±0.10%	±0.30%	±0.60%
RMS ERROR SUM	±0.35%	±0.58%	±0.28%	±0.47%	±0.76%
TYPICAL ACCURACY	0.50%	0.75%	0.40%	0.60%	0.90%
OP-02 GRADE RECOMMENDED	OP-02A	OP-02	OP-02E	OP-02C	OP-02C

TRANSDUCER PERFORMANCE

Typical system accuracy is ±0.5% over the −55° to +125°C range of a REF-02A. For example, when calibrated at +25°C, the reading of V_{OUT} at +105°C may be 105.4°C, a deviation of 0.5% of the 80° temperature change (+25°C to +105°C).

Although the REF-02 is guaranteed to perform over the −55° to +125°C range only, operation beyond those limits is possible. A large number of devices were measured and found to be functioning satisfactorily over the −150°C to +170°C range, and there was only a slight degradation in accuracy.

REMOTE APPLICATIONS

In many applications, the sensor must be located some distance away from the measurement circuitry. One precaution must be taken with the REF-02: a 1.5kΩ resistor should be connected between Pin 3 (TEMP) and its associated cable conductor to isolate this pin from cable capacitances.

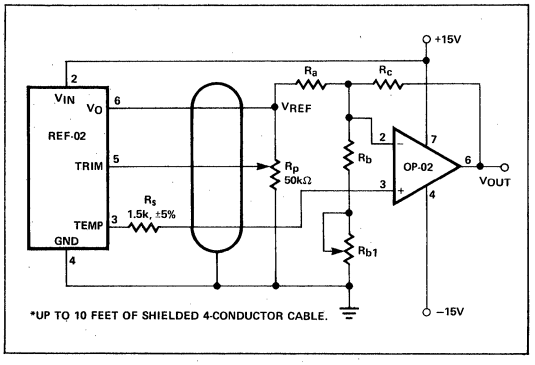


Figure 3. Precision Temperature Transducer with Remote Sensor

Remote application of the transducer is illustrated in Figure 3 with R_S, the isolation resistor.

TRANSDUCER SUMMARY

The accuracies indicated compare quite favorably to traditional temperature measurement methods such as thermocouples and thermistors. Ease-of-use, low cost, and high accuracy make this new bandgap method of temperature measurement attractive in a wide range of applications.

The following section describes the bandgap principle in theory and its use in the internal REF-02 design.

BANDGAP REFERENCE THEORY

Bandgap voltage references (1), (2), (3), use predictable relationships from semiconductor physics to generate a constant voltage. The base-emitter voltage of a transistor (V_{BE}) has a processing and current density dependent **negative** temperature coefficient of about −2.1mV/°C. Another well-known relationship with a **positive** temperature coefficient is the difference between base-emitter voltages of two transistors operated at different current densities:

4. $\Delta V_{BE} = \frac{kT}{q} \log_e \left(\frac{J2}{J1}\right)$, where

   k = Boltzmann's constant = 1.38 x 10^{-23} joules/°K

   T = absolute temperature, °K

   q = charge of an electron = 1.6 x 10^{-19} coulomb

   J = current density

When ΔV_{BE} is amplified and added to V_{BE}, a voltage reference with zero temperature coefficient results if the sum (V_Z) of these two terms equals the linearly-extrapolated bandgap voltage of silicon (V_{go}) at 0°K or −273°C, V_{go} = 1.205V. A more exact calculation, see reference 2, will show that V_Z will have zero temperature coefficient if:

5. $V_Z = V_{go} + \frac{kT}{q} = 1.230V @ +25°C$

The circuit in Figure 4 generates a ΔV_{BE} of 72mV at 25°C by making the current density of Q2 16 times greater than Q1. Q2 has four times the current of Q1, and Q1 has four times the emitter area of Q2. A ΔV_{BE} of 72mV appears across R1 and is amplified by 8.75 (becoming the TEMP output) and is added to V_{BE} (Q2) to produce a nearly constant V_Z of 1.23V. The −2.1mV/°C of TCV_{BE} is cancelled by the +2.1mV/°C of TCV_{TEMP}; and V_Z is amplified by 4.06 to produce an output of V_{REF} of 5.000V.

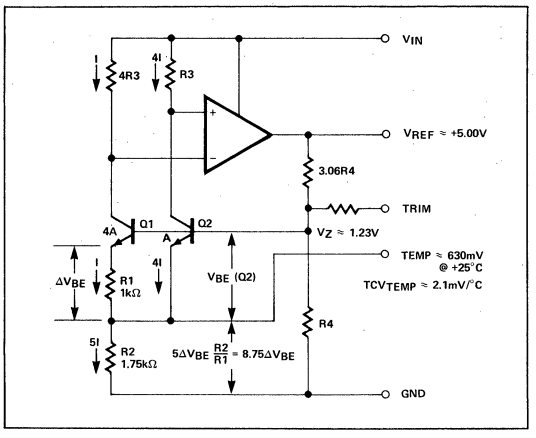


Figure 4. REF-02 Simplified Schematic

Table 4. REF-02 Typical Nodal Voltages

VOLTAGE \ TEMPERATURE	T_A = −75°C (T_J = 200°K)	T_A = +25°C (T_J = 300°K)	T_A = +125°C (T_J = 400°K)
$\Delta V_{BE} = \frac{kT}{q} \log_e 16$	48mV	72mV	96mV
$V_{TEMP} = 8.75\ \Delta V_{BE}$	420mV	630mV	840mV
V_{BE}(Q2)	810mV	600mV	390mV
$V_{REF} \approx V_{BE} + V_{TEMP}$	1.23V	1.23V	1.23V
$V_{REF} \approx 1 + \frac{3.06R4}{R4}$ $\approx 4.06V_Z$	5.00V	5.00V	5.00V

CONCLUSION

The REF-02, by using a bandgap design, provides both a stable +5V reference voltage output and an additional output voltage directly proportional to temperature. Accurate electronic thermometers reading in °C or in °F can be constructed at low cost for a wide variety of temperature monitoring and controlling applications.

REFERENCES

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   IEEE Journal of Solid-State Circuits
   Volume sc-6, Number 1, February 1971.
2. "A Precision Reference Voltage Source"
   K.E. Kuijk
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APPLICATION NOTE 19

DIFFERENTIAL AND MULTIPLYING DIGITAL-TO-ANALOG CONVERTER APPLICATIONS

By John Schoeff and Donn Soderquist

INTRODUCTION

The introduction of low-cost monolithic D/A converters has simplified data acquisition and control system design. This application note describes several new applications using the multiplying capability and dual complementary current outputs of the Precision Monolithics DAC-08.

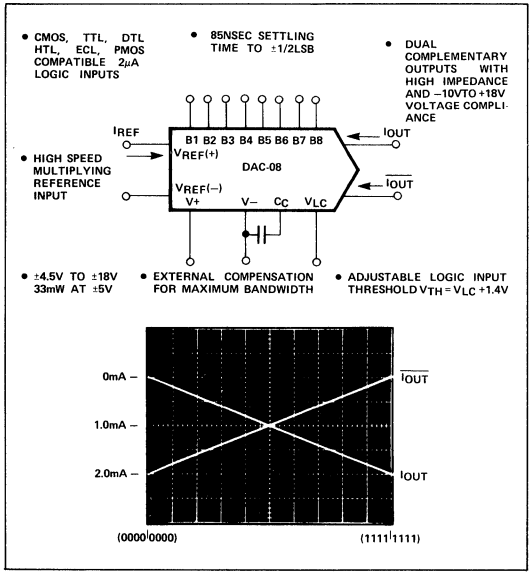


Figure 1. The Universal DAC

MULTIPLYING DAC BASICS

A multiplying DAC has an analog output which is the product of a digital input word and a reference voltage and can be expressed as:

$$1.\ 1\ E_O = E_{REF}\ \frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}$$

For a current reference, current output DAC, the expression becomes:

$$2.\ 1\ I_O = I_{REF}\ \frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}$$

The DAC-08 has complementary/differential current outputs, and I_O has a complement expressed as:

3. $I_O = I_{FS} - I_O$ for all input logic states.

The relationship of I_{REF} to I_O and $\overline{I_O}$ is illustrated in Figure 2 and in Figure 3, the basic DC reference connections. References may be either positive or negative, and a bipolar output voltage may be achieved using the high compliance current outputs alone or with an output operational amplifier. The simplest form of a multiplying DAC accepts a unipolar varying reference input.

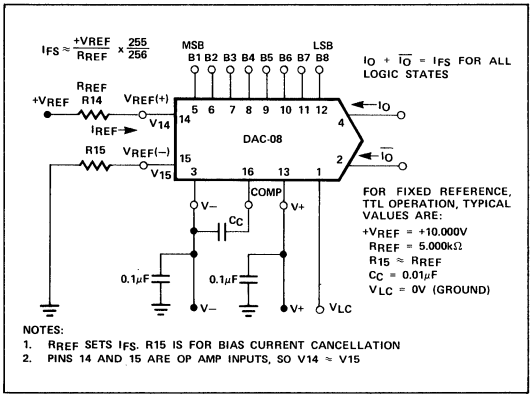


Figure 2. Positive Reference Connection

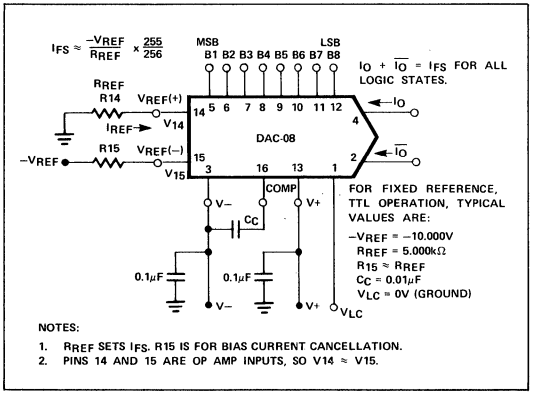


Figure 3. Negative Reference Connection

BIPOLAR REFERENCES

Operation with bipolar references is achieved by modulating I_{REF} as shown in Figure 5. To aid in understanding bipolar operation, see the equivalent circuit in Figure 4. The reference inputs of the DAC-08 are op amp inputs — $V_{REF}(+)$ being the inverting input and $V_{REF}(-)$ being the noninverting input. Excellent gain linearity of the reference amplifier allows multiplying operation over a range of I_{REF} of 4μA to 4mA with monotonic operation from less than 100μA to 4mA.

$C_C = 15pF$, the reference amplifier slews at 4mA/μs enabling a transition from $I_{REF} = 0$ to $I_{REF} = 2mA$ in 500ns. If R_{14} or the parallel equivalent resistance at Pin 14 is less than 200Ω, no compensation capacitor is necessary, and a full-scale transition requires only 16ns.

TWO-QUADRANT MULTIPLICATION

There are two forms of two-quadrant multiplication: bipolar digital, where the digital input word controls output polarity,

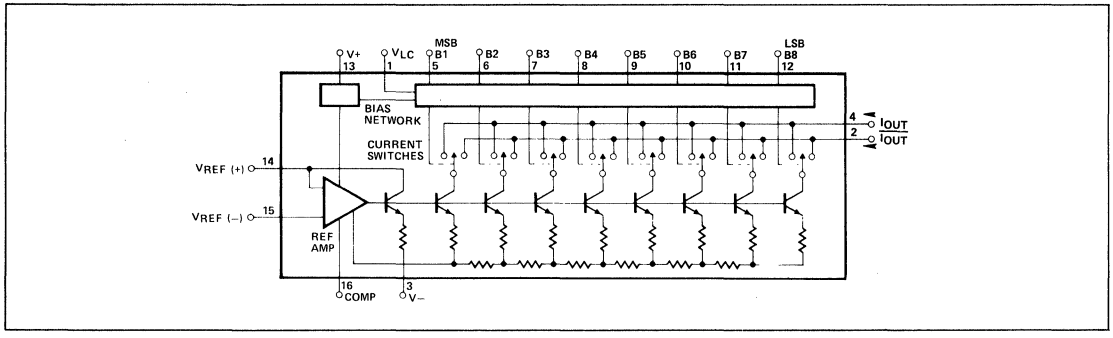


Figure 4. DAC-08 Equivalent Circuit

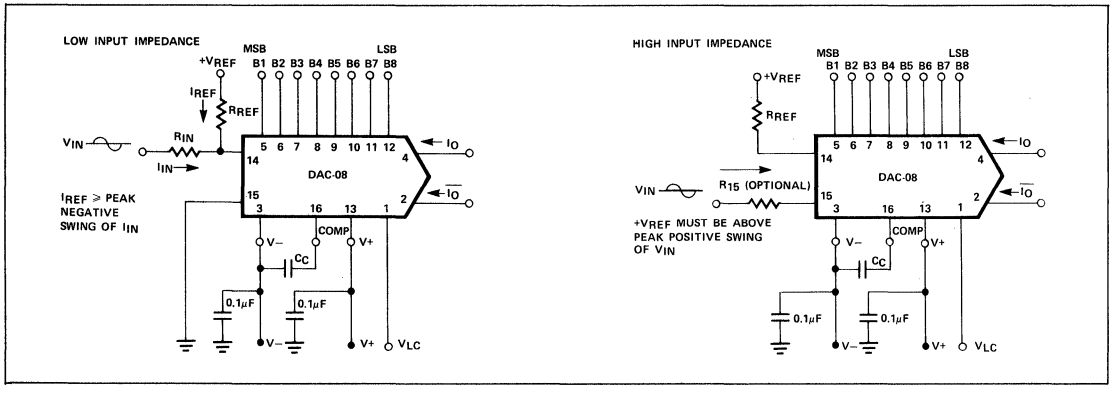


Figure 5. Bipolar Reference Connections

REFERENCE AMPLIFIER COMPENSATION

AC reference applications will require the reference amplifier to be compensated using a capacitor from Pin 16 to V–. The value of this capacitor depends on the impedance presented to Pin 14: for R_{14} values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 15, 37, and 75pF. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin.

FAST PULSED OPERATION

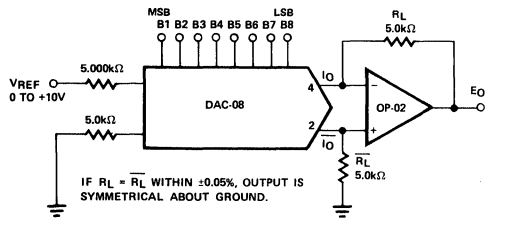
For fastest multiplying response, low values of R_{14} enabling small C_C values should be used. For $R_{14} = 1k\Omega$ and

and bipolar analog, where the analog reference input controls output polarity.

Bipolar digital two-quadrant mutliplication is shown in Figure 6 with the output polarity being controlled by an offset-binary-coded digital input word.

Bipolar analog two-quadrant multiplication is shown in Figure 7. A bipolar reference voltage is connected to the upper DAC-08 and modulates the reference current by ±1.0mA around a quiescent current of 1.1mA. The lower DAC-08 also has a reference current of 1.1mA; due to the parallel digital inputs, the lower DAC-08 effectively subtracts out the quiescent 1.1mA of the upper DAC-08's reference current at all in-

put codes, since the voltage across R3 varies between −10V and 0V. Thus, the output voltage, E_O, is a product of a digital input word and a bipolar analog reference voltage.



	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O (V)
POS. FULL SCALE	1	1	1	1	1	1	1	1	1.992	0.000	+9.96
POS. FULL SCALE −LSB	1	1	1	1	1	1	1	0	1.984	0.008	+9.88
(+) ZERO SCALE	1	0	0	0	0	0	0	0	1.000	0.992	+0.040
(−) ZERO SCALE	0	1	1	1	1	1	1	1	0.992	1.000	−0.040
NEG. FULL SCALE +LSB	0	0	0	0	0	0	0	1	0.008	1.984	−9.88
NEG. FULL SCALE	0	0	0	0	0	0	0	0	0.000	1.992	−9.96

Figure 6. Bipolar Digital Two-Quadrant Multiplication (Symmetrical Offset Binary)

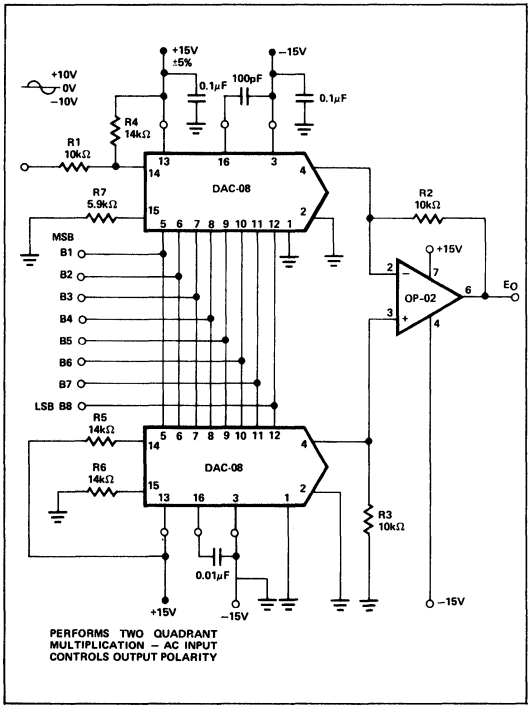


Figure 7. Bipolar Analog Two-Quadrant Multiplication (DC-Coupled Digital Attenuator)

FOUR-QUADRANT MUTLIPLICATION

Four-quadrant multiplication combines the two forms of two-quadrant multiplication. Output analog polarity is controlled by either the analog input reference or by the offset binary digital input word. One implementation of this function with the DAC-08 is shown in Figure 8 with output current values listed in Table 1.

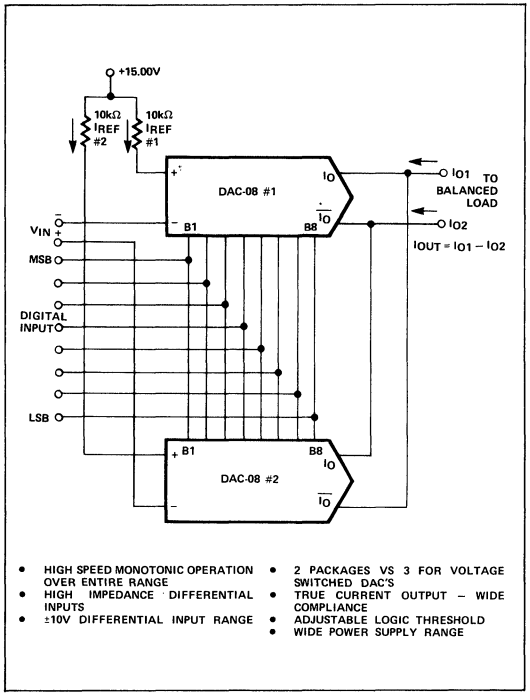


Figure 8. Four-Quadrant Multiplying DAC with with Impedance Input

The four-quadrant mutliplying DAC circuit shown accepts a differential voltage input and produces a differential current output. An output op amp is not shown because it is not always required; many applications are more suited for high output compliance (−10V to +18V) differential current outputs. Typical balanced loads include transformers, transducers, transmission lines, bridges and servos.

Operation of the four-quadrant multiplier may be more easily visualized by considering that if either $V_{IN} = 0V$ or the offset binary digital input code is at midscale (corresponding to zero), then a change in the other input will not affect the output. Zero multiplied by any number equals zero.

A common mode current will be present at the output and must be accommodated by the balanced load. A pair of matched resistors may be used at the outputs to shunt most of the common mode current to ground, thus reducing the common mode voltage swing at the output.

Table 1. Four-Quadrant Multiplying Current Values in Figure 8.

DIGITAL INPUT	$V_{IN}(+)$	$V_{IN}(-)$	V_{IN} DIFF.	I_{REF} #1 (mA)	I_{REF} #2 (mA)	I_O#1 (mA)	I_O#2 (mA)	I_{01} (mA)	I_O#2 (mA)	I_O#1 (mA)	I_{02} (mA)	I_{OUT} DIFF.
1111 1111	+5V	−5V	+10V	2.000	1.000	1.992	0	1.992	0.996	0	0.996	0.996mA
1000 0000	+5V	−5V	+10V	2.000	1.000	1.000	0.496	1.496	0.500	0.992	1.492	0.004mA
0111 1111	+5V	−5V	+10V	2.000	1.000	0.992	0.500	1.492	0.496	1.000	1.496	−0.004mA
0000 0000	+5V	−5V	+10V	2.000	1.000	0	0.996	0.996	0	1.992	1.992	−0.996mA
1111 1111	0V	0V	0V	1.500	1.500	1.494	0	1.494	1.494	0	1.494	0.000mA
1000 0000	−10V	−10V	0V	2.500	2.500	1.250	1.240	2.490	1.250	1.240	2.490	0.000mA
0111 1111	+10V	+10V	0V	0.500	0.500	0.248	0.250	0.498	0.248	0.250	0.498	0.000mA
0000 0000	0V	0V	0V	1.500	1.500	0	1.494	1.494	0	1.494	1.494	0.000mA
1111 1111	−5V	+5V	−10V	1.000	2.000	0.996	0	0.996	1.992	0	1.992	−0.996mA
1000 0000	−5V	+5V	−10V	1.000	2.000	0.500	0.992	1.492	1.000	0.496	1.496	−0.004mA
0111 1111	−5V	+5V	−10V	1.000	2.000	0.496	1.000	1.496	0.992	0.500	1.492	0.004mA
0000 0000	−5V	+5V	−10V	1.000	2.000	0	1.992	1.992	0	0.996	0.996	0.996mA

HIGHEST SPEED FOUR-QUADRANT MULTIPLYING CONSIDERATIONS

The configuration shown in Figure 10 makes use of the DAC-08's ability to operate in a fast-pulsed reference mode without compensation capacitors. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff ($I_{REF} = 0$) condition. This connection yields a reference slew rate of 16mA/μs which is relatively independent of R_{IN} and V_{IN} values.

Input resistances are not limited to 10kΩ. For example, 100kΩ resistors for R_{IN1} and R_{IN2} allow ±100V reference voltage inputs making this connection especially useful in high common mode voltage environments. Except for different reference treatment, operation and digital input coding are identical in the circuits shown in Figure 8 and in Figure 10; both have the transfer function shown in Figure 9.

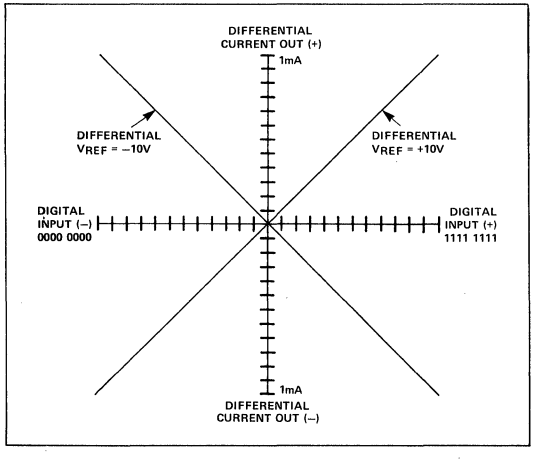


Figure 9. Four-Quadrant Multiplying DAC Transfer Function

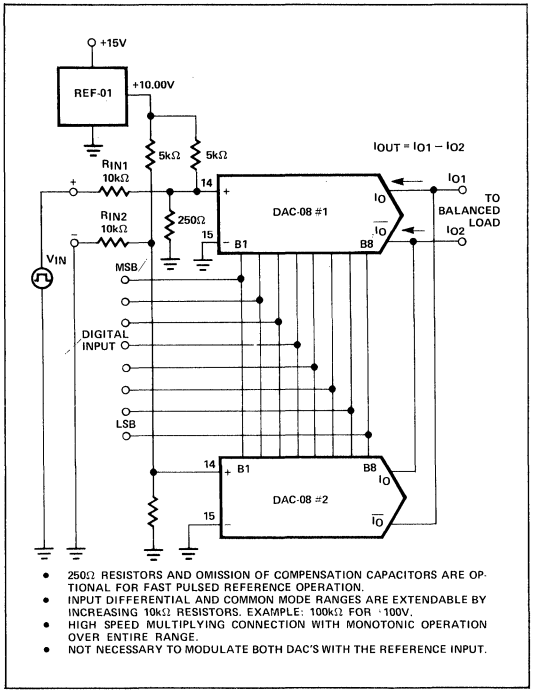


Figure 10. Four-Quadrant Multiplying DAC with Extendable Input Range and Highest Speed

AC-COUPLED MULTIPLICATION

Some multiplying DAC applications are more easily achieved with AC coupling. At the same time, a high impedance input is often required to avoid loading a relatively high source impedance. Both requirements are met by the circuits shown in Figure 11 and Figure 12 which use the compensation

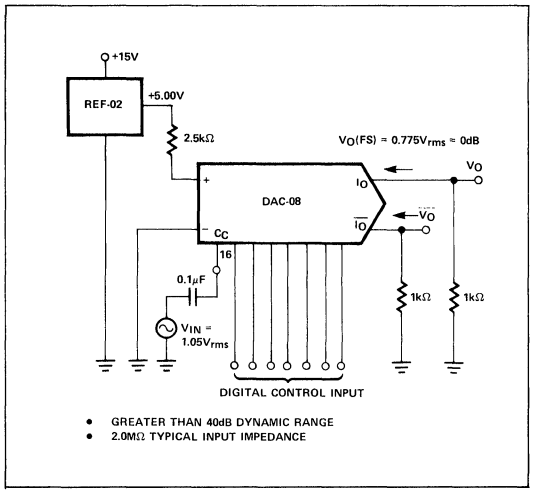


Figure 11. High Input Impedance AC-Coupled Multiplication (Audio Frequency Digital Attenutor)

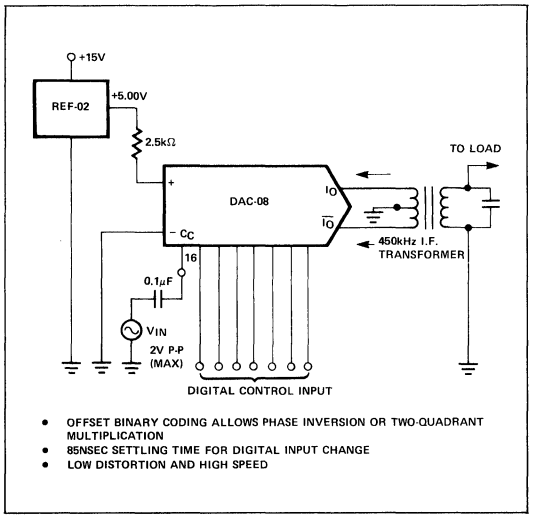


Figure 12. High Input Impedance AC-Coupled Multiplication (I.F. Amplifier/Digital Attenuator)

capacitor terminal (C_C) as an input. This is possible because C_C is the base of a transistor whose emitter is one diode drop (0.7V) away from the R-2R ladder network common baseline internal to the DAC-08.

With a full-scale input code the output, V_O, is flat to >200kHz and is 3dB down at approximately 1.0MHz making this type of multiplying connection useful even beyond the audio frequency range. Such a connection is illustrated in Figure 12 operating at 455kHz, the highest recommended operating frequency in this connection.

DIFFERENTIAL AND RATIOMETRIC A/D CONVERSION

Complementary/differential current-source outputs and multiplying capability allow the DAC-08 to be used in differential and ratiometric A/D converter designs directly without signal conditioning amplifiers. This group of applications begins with the basic differential A/D converter and ratiometric A/D conveter connections followed by more specific applications.

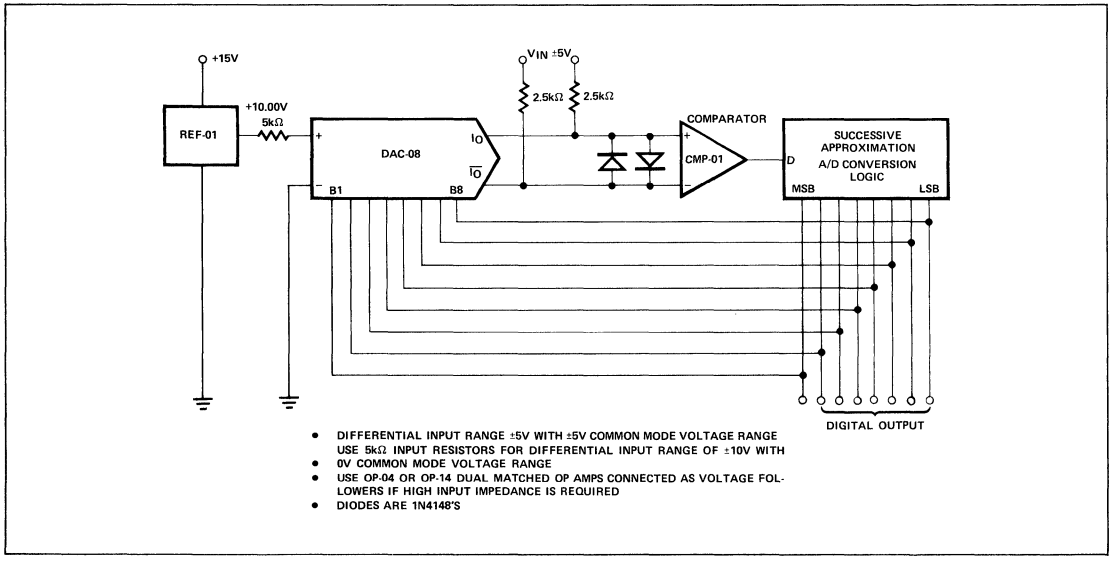


Figure 13. Differential Input A/D Conversion Basic Connections

These are extremely cost-effective designs due to their low parts count and simplicity. Alternative designs performing identical functions require instrumentation amplifiers for the differential-to-single-ended input signal conditioning and analog multipliers or dividers for the arithmetic functions.

DIFFERENTIAL A/D CONVERSION

The circuit in Figure 13 uses the high voltage compliance current output capability of the DAC-08 and the high common mode voltage rejection of the CMP-01 to construct a differential input ADC without input signal conditioning.

A successive approximation ADC is constructed with four ICs: a REF-01 +10V reference, a 2502-type successive approximation register, a CMP-01 precision voltage comparator, and a DAC-08. As shown, the circuit converts an analog input in less than 2.0μs. For lower speed requirements, the A/D conversion logic can be the tracking or servo type consisting of up/down counters.

FOUR-QUADRANT RATIOMETRIC A/D CONVERSION

Ratiometric A/D conversion with fully differential X and Y inputs is accomplished with the circuit in Figure 14. Here, one set of inputs, V_X, is connected in a manner similar to the circuit in Figure 13, and the other set of inputs V_Y, is connected in a multiplying fashion. Operation is as follows: I_{REF} for both the upper and the lower DAC-08 is modulated between 1mA and 3mA; and the resulting output currents are differentially transformed into voltages by the 5kΩ resistors at the comparator's inputs and compared with the V_X differential input. When the conversion process is complete (comparator inputs differentially nulled to less than 1/2 LSB) a digital output is available which corresponds to the quotient of V_X/V_Y. Thus, four-quadrant ratiometric A/D conversion is achieved with four ICs and without instrumentation amplifiers.

BRIDGE TRANSDUCER NULL

In many control systems, bridges must be nulled, and a digital representation of the bridge's error must be provided for computer monitoring and control. The circuit in Figure 15 accomplishes both tasks by using the DAC-08 complementary/differential current outputs to null the bridge with the DAC-08 connected in a tracking differential A/D converter configuration. The REF-02 reference voltage source provides both the bridge excitation voltage and the positive reference voltage for the DAC-08. Some of the advantages of this circuit are listed at the bottom of Figure 15.

POWER MONITOR

Another differential current-input ADC is shown in Figure 16 with a transformer-coupled input. An up/down counter, a precision high-speed comparator, and the DAC-08 form a tracking A/D converter which continuously monitors the analog input. Two precautions must be observed: the common mode voltage at the comparator's inputs must not ex-

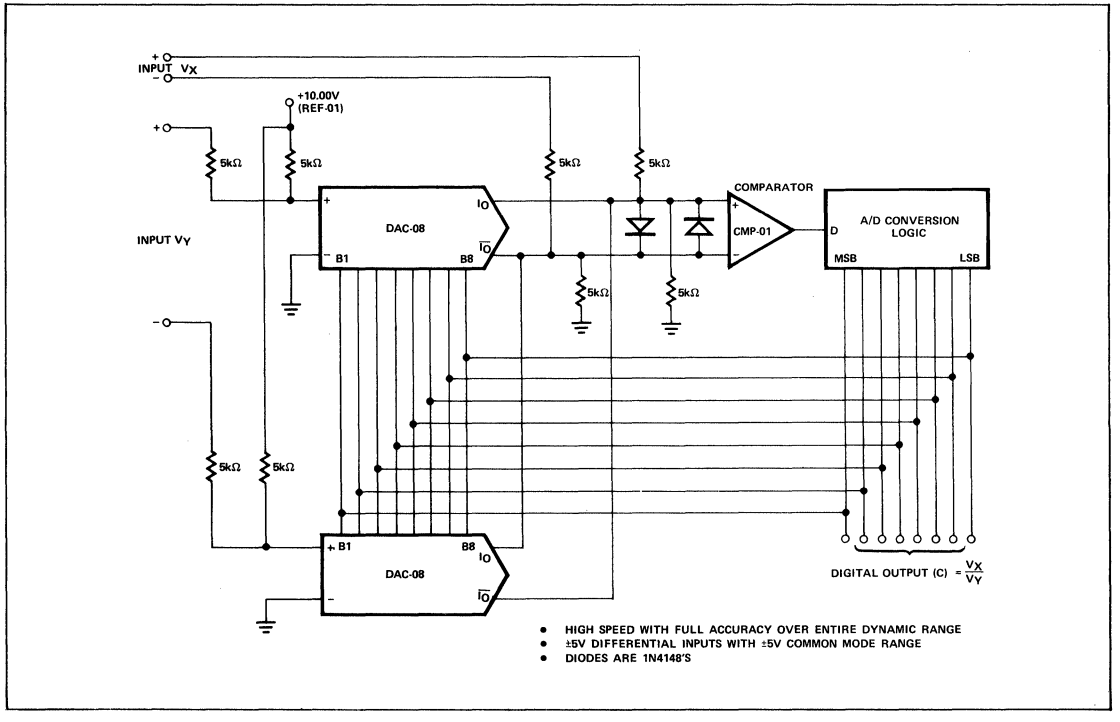


Figure 14. Four-Quadrant Ratiometric A/D Conversion Basic Connections

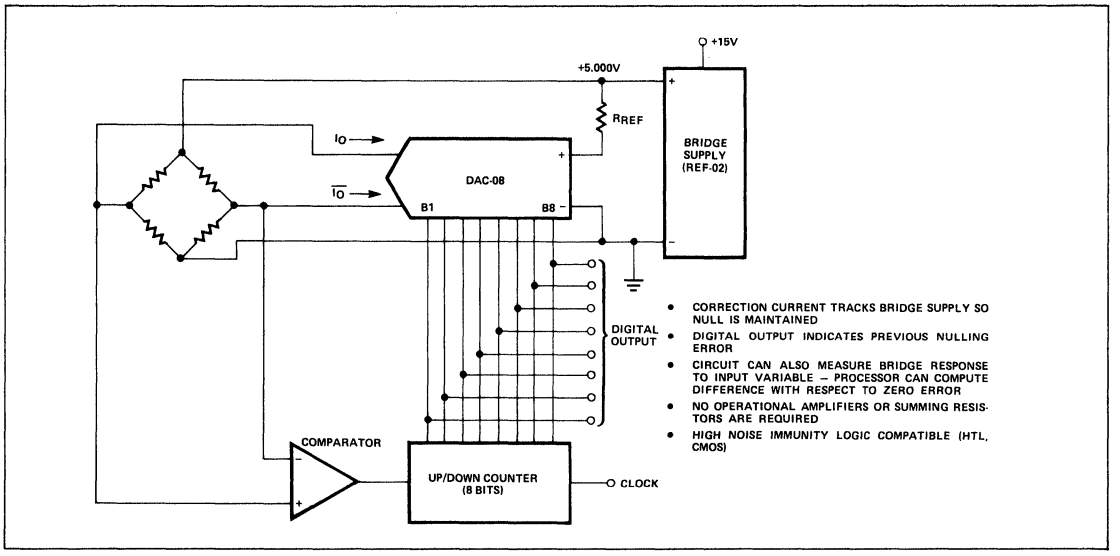


Figure 15. Bridge Transducer Null

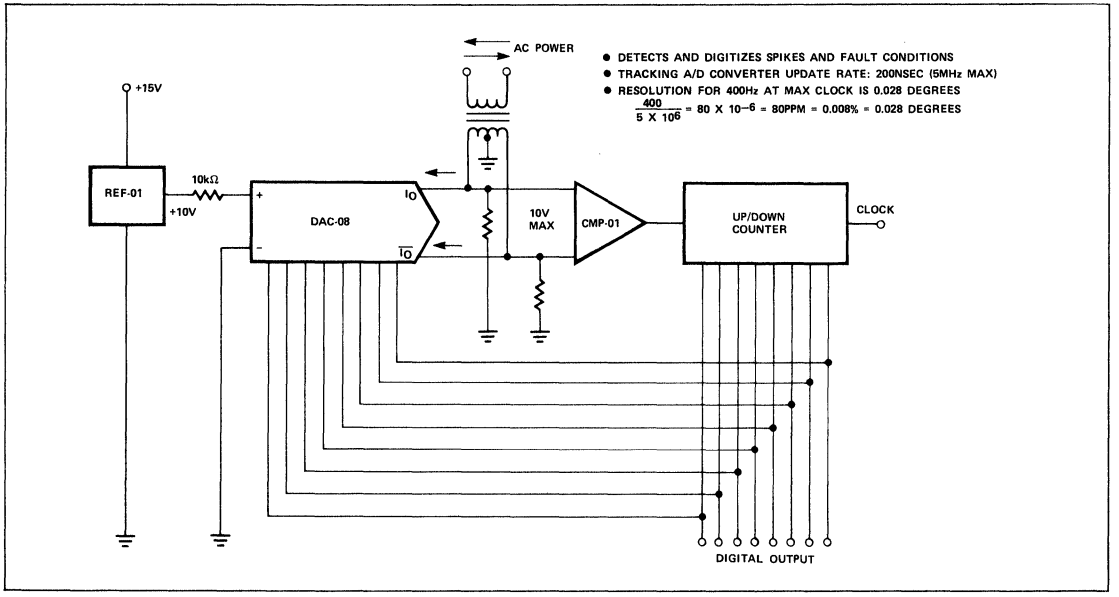


Figure 16. Power Fault Monitor and Detector

ceed ±10V; and the differential voltage must not exceed 11V. Voltage-limiting resistors at the comparator's inputs are recommended.

ALGEBRAIC DIGITAL COMPUTATION

Frequently, a digital arithmetic operation (addition, subtraction, multiplication, or division) must be performed, and an analog output must be provided. Traditionally, the arithmetic operations are performed with several ICs, and the output drives a D/A converter. This section decribes applications of the DAC-08 as an arithmetic building block, new design approaches that reduce the number of packages required in many applications. Today's low cost, versatile DACs merit a designer's consideration as arithmetic elements.

One benefit is not immediately apparent and deserves special mention. In all of these applications, the digital input words can be CMOS, TTL, DTL, NMOS, or MECL, because the DAC-08 interfaces with all of those logic families. In fact, the two input words may even be from different logic families to eliminate special level translators or interface circuitry. (See AN-17 "DAC-08 Applications Collection.")

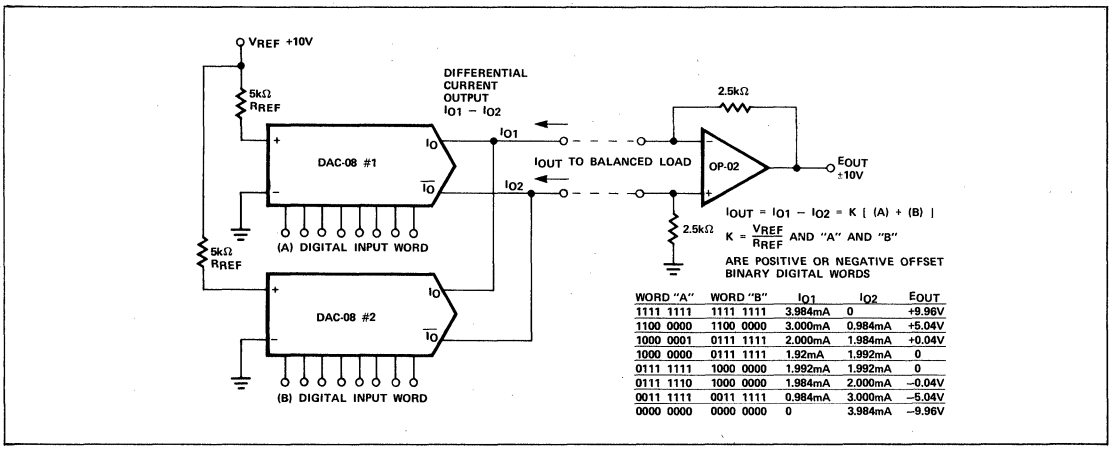
The first arithmetic application is shown in Figure 17. Two DAC-08s perform a fast algebraic summation with a direct analog output. The circuit works by paralleling the outputs of two DAC-08s and summing their currents while driving a balanced load. The output is the algebraic sum of word "A" and word "B" in all four quadrants.

FOUR-QUADRANT DIGITAL MULTIPLICATION

High-speed multiplication of two 8-bit digital words with an analog output usually requires several logic packages and a D/A converter. The circuit in Figure 18 performs this function using only three ICs.

In Figure 18 DAC-08 number 1 and number 2 are connected as previously shown, and DAC-08 number 3 provides the analog reference inputs to DAC-08 number 1 and number 2. Those reference inputs are determined by digital input word "A." The circuit's output, I_{01}-I_{02}, is a differential current output which may be used to drive a balanced load.

Four-quadrant multiplication is thus performed by adding one more DAC-08 to the basic four-quadrant multiplying connection.



WORD "A"	WORD "B"	I_{O1}	I_{O2}	E_{OUT}
1111 1111	1111 1111	3.984mA	0	+9.96V
1100 0000	1100 0000	3.000mA	0.984mA	+5.04V
1000 0001	0111 1111	2.000mA	1.984mA	+0.04V
1000 0000	0111 1111	1.92mA	1.992mA	0
0111 1111	1000 0000	1.992mA	1.992mA	0
0111 1110	1000 0000	1.984mA	2.000mA	−0.04V
0011 1111	0011 1111	0.984mA	3.000mA	−5.04V
0000 0000	0000 0000	0	3.984mA	−9.96V

Figure 17. Four-Quadrant Algebraic Digital Computation

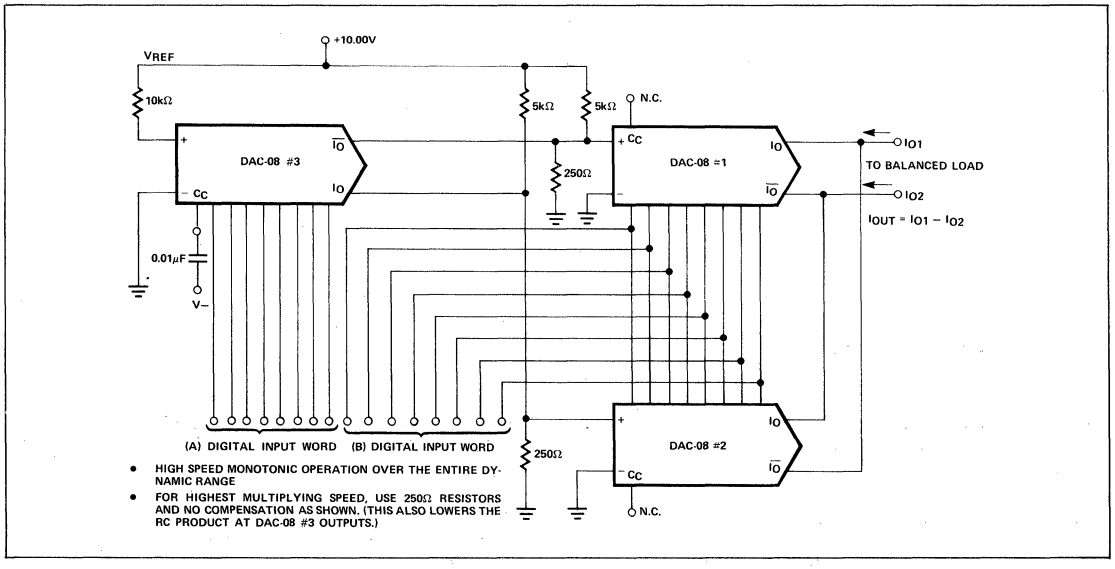


Figure 18. Four-Quadrant 8-Bit × 8-Bit Digital Multiplier

APPLICATION NOTE 20

EXPONENTIAL DIGITALLY CONTROLLED OSCILLATOR USING DAC-76

By Donn Soderquist

Here is a 4-IC, microprocessor-controlled oscillator with a 8159 to 1 frequency range covering 2.5Hz to 20kHz. An exponential, current output IC DAC functioning as a programmable current source alternately charges and discharges a capacitor between precisely-controlled upper and lower limits. This circuit features instantaneous frequency change, operates with +5V ±1V and −15V ±3V supplies, and provides monotonic frequency changes over a 78dB range — the dynamic range of a 13-bit DAC.

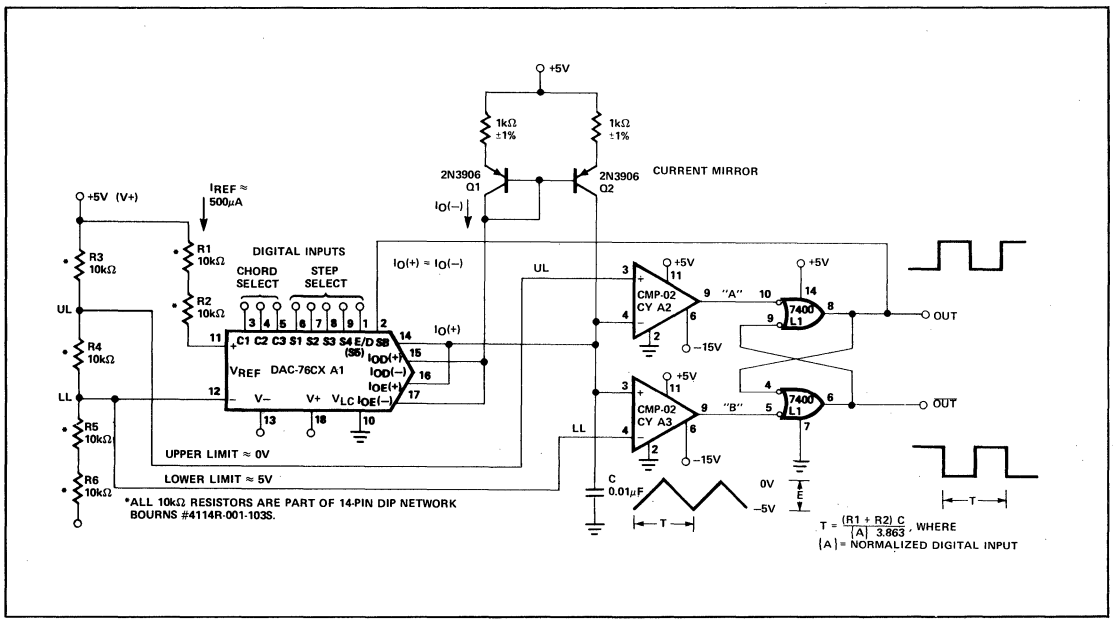
BASIC OPERATION

Connected as shown below, the output of the exponential DAC is an eight-chord (or segment) current ranging between 250nA and 2.0mA. The three most significant bits select 1 of 8 binarily-related chords; and the five least significant bits select 1 of 32 linear steps within each chord. This current is switched between the $I_O(+)$ output and the $I_O(-)$ output under the control of a pin labeled SB.

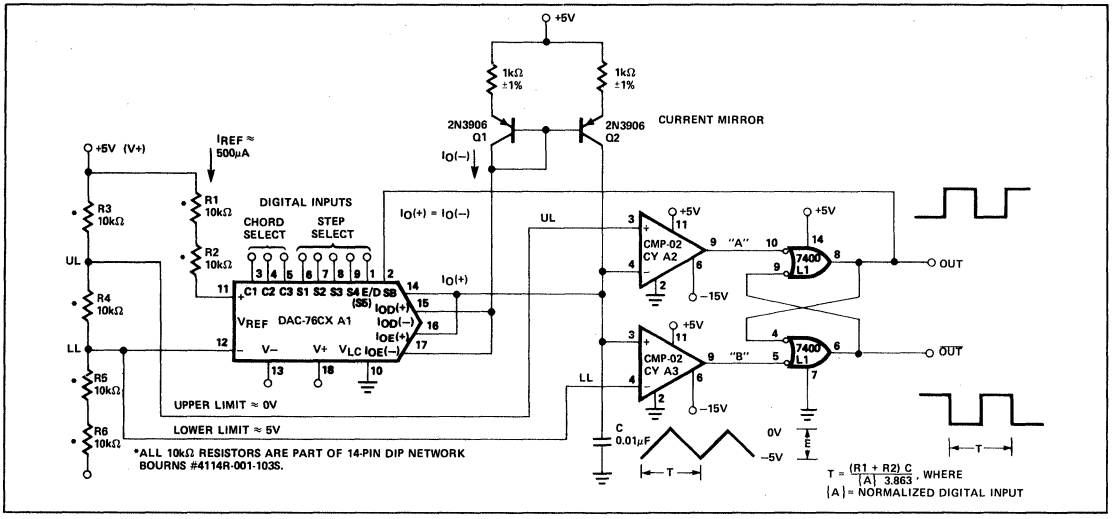
When SB is low, $I_O(-)$ is selected, and the DAC's output current drives a current mirror which ramps the timing capacitor in a positive direction until an upper limit of 0V is sensed by A2. At this time the set-resist flip-flop (L1) is set, SB becomes a "1", and the DAC's output current is switched to the $I_O(+)$ output. Now the capacitor is charged to a lower limit of −5V, the flip-flop is reset, and the cycle repeats itself.

REFERENCE SETUP

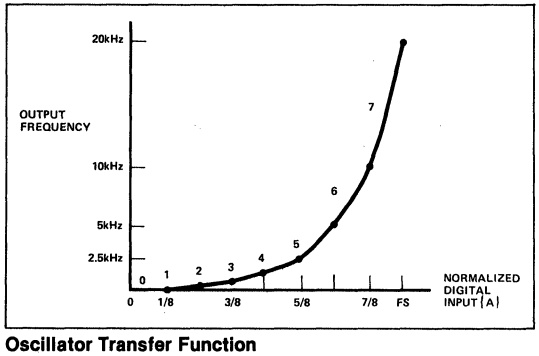
The multiplying relationship between the reference current, I_{REF}, and the full-scale output of the DAC is 3.863. I_{REF} is set by the voltage between V+ and the lower limit divided by R1 + R2. This is so because Pin 12, $V_{REF}(-)$, is a high-impedance input, namely the noninverting input of an op amp internal to the DAC. Since both I_{REF} and the upper and lower limits are derived by dividing down the power supply voltages, operation (frequency of oscillation) is independent of power supply changes. (See Appendix for a complete derivation of the timing formula.)



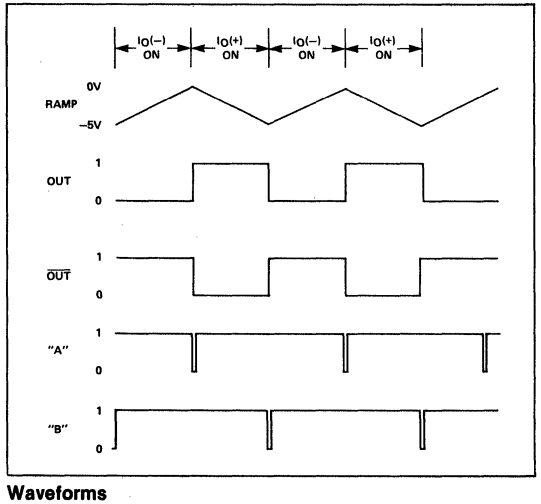
Circuit Diagram Exponential Digitally-Controlled Oscillator



Circuit Diagram Exponential Digitally-Controlled Oscillator



Oscillator Transfer Function



Waveforms

Table 1. Ideal Output Frequency

CHORD (SEGMENT)	DIGITAL INPUT CODE	NORMALIZED DIGITAL INPUT |A|	OUTPUT FREQUENCY	AVERAGE STEP SIZE
0	000 00001	$\frac{1}{8159}$	2.45Hz	2.3Hz
	000 01000	$\frac{8}{8159}$	19.6Hz	
	000 11111	$\frac{31}{8159}$	76.0Hz	
1	001 00000	$\frac{33}{8159}$	80.9Hz	4.8Hz
	001 11111	$\frac{95}{8159}$	233Hz	
2	010 00000	$\frac{99}{8159}$	243Hz	9.5Hz
	010 11111	$\frac{223}{8159}$	547Hz	
3	011 00000	$\frac{231}{8159}$	566Hz	19Hz
	011 11111	$\frac{479}{8159}$	1.17kHz	
4	100 00000	$\frac{495}{8159}$	1.21kHz	38Hz
	100 11111	$\frac{991}{8159}$	2.43kHz	
5	101 00000	$\frac{1023}{8159}$	2.51kHz	76Hz
	101 11111	$\frac{2015}{8159}$	4.94kHz	
6	110 00000	$\frac{2079}{8159}$	5.09kHz	152Hz
	110 11111	$\frac{4063}{8159}$	9.96kHz	
7	111 00000	$\frac{4191}{8159}$	10.3kHz	303Hz
	111 11111	$\frac{8159}{8159}$ = FS	20.0kHz	

FREQUENCY SELECTION

Table 1 lists ideal output frequencies at the lowest and highest codes of each chord and the average change in frequency produced by a one-step change (LSB change) within each chord. For highest accuracy in Chord 0, especially between 2.5Hz and 19.6Hz, comparators with low input current are recommended. The CMP-02CY comparators typically have 35nA of input current; at the lowest code point (000 00001) the DAC output is 250nA; so low input current comparators are essential for best operation. Above 000 01000 (4μA or 19.6Hz) the comparator input currents become less critical.

CONCLUSION

A microprocessor-controlled oscillator has been shown which achieves a 13-bit dynamic range with only 8 bits of control. Monotonic frequency steps over 2.5Hz to 20kHz are provided in a 4-IC low-cost design.

REFERENCE

"Eight-bit Frequency Source Suited for μP Control" by Albert Helfrick, **EDN**, September 20, 1976, pp. 116-118.

APPENDIX

TIMING EQUATION DERIVATIONS

One of the best features of this design is its insensitivity to power supply changes. The equation derivations are shown to explain how V+ and V− drop out as timing determinations.

With a constant current drive the charge on C changes linearly over a range (E) between an upper limit (UL) and a lower limit (LL) dependent upon the DAC's digital input code, the DAC's output current, and the value of the timing capacitor (C).

Equation 1. $T = 2\left(\frac{CE}{I}\right)$ where:

C = timing capacitor value

E = upper limit — lower limit

I = DAC output current, $I_O(+)$ or $I_O(-)$

T = period

Equation 2. E = UL − LL where: UL = upper limit
LL = lower limit

Equation 3. $UL = \frac{R4+R5+R6}{R3+R4+R5+R6}\left[(V+)-(V-)\right]+(V-)$

where: V+ = positive power supply and V− = negative power supply

but: R3 = R4 = R5 = R6

$\therefore UL = \frac{3(V+)+(V-)}{4}$

Equation 4. $LL = \frac{R5+R6}{R3+R4+R5+R6}\left[(V+)-(V-)\right]+(V-)$

$$LL = \frac{(V+)+(V-)}{2}$$

Substituting 3 and 4 into 2 and solving for E:

Equation 5. $E = \frac{(V+)-(V-)}{4}$

Rewriting Equation 1 and substituting 5:

Equation 6. $\frac{T}{2C} \quad \frac{(V+)-(V-)}{\frac{4}{I}}$

The expression for I is:

Equation 7. $I = 3.863\ \{A\}\ I_{REF}$

where: 3.863 is a constant derived from the ratio of I_{REF} to $I_{FULL\ SCALE}$ of the DAC
A = the normalized digital input code
I_{REF} = the reference current

Equation 8. $I_{REF} = \frac{(V+)-LL}{R1+R2}$

Substituting 4 into 8:

Equation 9. $I_{REF} = \frac{(V+)-\left[\frac{(V+)+(V-)}{2}\right]}{R1+R2}$

$$= \frac{(V+)-(V-)}{2(R1+R2)}$$

Substituting 9 and 7 into 6:

Equation 10. $\frac{T}{2C} = \frac{\frac{(V+)-(V-)}{4}}{3.863\ \{A\}\left[\frac{(V+)-(V-)}{2(R1+R2)}\right]}$

Multiplying by {A} 3.863:

Equation 11. $\frac{\{A\}\ 3.863T}{2C} = \frac{\frac{(V+)-(V-)}{4}}{\frac{(V+)-(V-)}{2(R1+R2)}}$

$$\frac{\{A\}\ 3.863T}{2C} = \frac{R1+R2}{2}$$

So V+ and V− have dropped out as timing considerations. Solving for T:

Equation 12. $T = \frac{C(R1+R2)}{3.863\ \{A\}}$ but: $C = 0.01\mu F$
$R1 = R2 = 10k\Omega$

Equation 13. $T = \frac{5.177 \times 10^{-5}}{\{A\}}$

Finally, the simplified expressions:

Equation 14. $T \cong \frac{50\mu s}{\{A\}}$

Equation 15. f (frequency) $\cong \frac{\{A\}}{50 \times 10^{-6}} \cong$ 20kHz full scale

OTHER DAC APPLICATIONS

The combination of high voltage compliance complementary current outputs, universal logic inputs, and multiplying capability in a low-cost DAC enables widespread application. Consider the following partial list:

A/D CONVERTERS

Tracking (Servo)
Successive Approximation
Ramp (Staircase)
Microprocessor Controlled
Ratiometric (Bridge Balancing)

TEST SYSTEMS

Transistor Tester (Force I_B and I_C)
Resistor Matching (Use both outputs)
Programmable Power Supplies
Programmable Pulse Generators
Programmable Current Source
Function Generators (ROM Drive)

ARITHMETIC OPERATIONS

Analog Division by a Digital Word
Analog Quotient of Two Digital Words
Analog Product of Two Digital Words — Squaring
Addition and Subtraction with Analog Output
Magnitude Comparison of Two Digital Words
Digital Quotient of Two Analog Variables
Arithmetic Operations with Words from Different Logic Families

GRAPHICS AND DISPLAYS

Polar to Rectangular Conversion
CRT Character Generation
Chart Recorder Driver
CRT Display Driver

DATA TRANSMISSION

Modem Transmitter
Differential Line Driver
Party Line Multiplexing of Analog Signals
Multi-Level 2-Wire Data Transmission
Secure Communications (Constant Power Dissipation)

CONTROL SYSTEMS

Reference Level Generator for Setpoint Controllers
Positive Peak Detector
Negative Peak Detector
Disc Drive Head Positioner
Microfilm Head Positioner

AUDIO SYSTEMS

Digital AVC and Reverberation
Music Distribution
Organ Tone Generator
Audio Tracking A/D

CONCLUSION

Differential and multiplying applications have been described which use the high-voltage compliance, complementary-current outputs and the high-speed multiplying inputs of the Precision Monolithics DAC-08.

BIBLIOGRAPHY

1. *"DAC-08 Applications Collection"*, John Schoeff and Donn Soderquist, Precision Monolithics Application Note 17, 1975
2. *"Low Cost, High-Speed Analog-to-Digital Conversion with the DAC-08"*, Donn Soderquist and John Schoeff, Precision Monolithics Application Note 16, 1975
3. *"Differential and Multiplying Use of Digital-to-Analog Converters"*, Donn Soderquist and John Schoeff, **E.E. Times** article, June 21, 1976, pp. 40-47

APPLICATION NOTE 21

3 IC 8-BIT BINARY DIGITAL TO PROCESS CURRENT CONVERTER WITH 4-20mA OUTPUT

By Donn Soderquist

This application note describes a 3 IC, 4-20mA process current, digital-to-analog converter that can be constructed for less than $20 at current 100+ prices. It operates from a −5V ±1V negative power supply and a +23V ±7V positive power supply, has 24V output voltage compliance, and occupies less than 4 square inches of printed circuit board space. Other significant features include TTL logic input compatibility, 8-bit binary coding, 0° to +70° C operation, and 5μs full scale settling time into a 500Ωload.

THEORY OF OPERATION

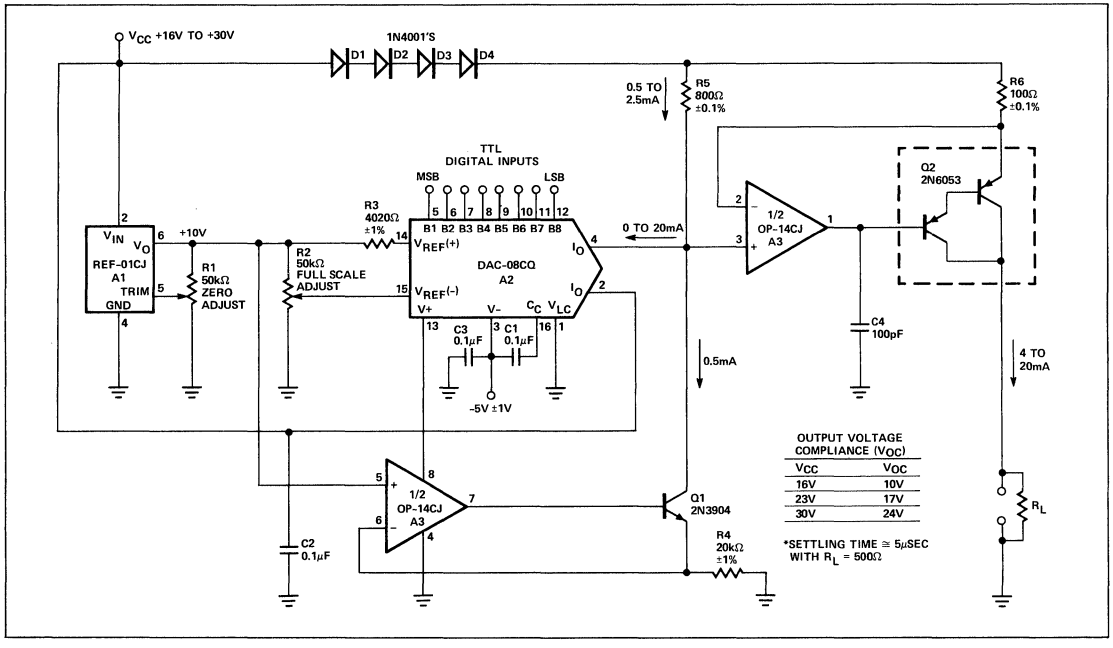
A fixed current of 0.5mA is added to a DAC's output current varying between 0 and 2.0mA and the resulting total current is multiplied by a factor of 8 to produce an output current of 4.0 to 20mA.

In the schematic, first note the REF-01CJ, a +10V adjustable reference. Its output goes to the noninverting input of one half of A3, a dual precision op amp. The inverting input is within a feedback loop forcing +10V to appear at the top of R4, a 20kΩ resistor; a 0.5mA current will flow in R4 through Q1, a high h_{FE} transistor. The same +10V is applied to R3, the reference input resistor of a multiplying IC D/A converter, the DAC-08. Full scale output current of the DAC will be the difference in voltage between the +10V reference and Pin 14 of the DAC divided by R3; Pin 15 will be at the same voltage as Pin 14 because it is a high impedance point, the noninverting input of an op amp internal to the DAC. After calibration a current of 0 to 2mA (depending on the digital input code) will flow into the DAC's output, Pin 4.

Both the DAC's output current and the fixed 0.5mA flow in R5, a 800Ω precision resistor. The voltage developed by that current is applied to the noninverting input of the other half of A3 and will also appear across R6, a 100Ω precision resistor. Thus, eight times the 0.5 to 2.5mA current in R5 flows in R6, or 4 to 20mA. Almost all of this current appears at the output because the 2N6053 is a high h_{FE} device, a power darlington transistor.

Some other components need explanation. C1 provides frequency compensation of the DAC's reference amplifier; C2

SCHEMATIC DIAGRAM



and C3 are power supply decoupling (bypass) capacitors; C4 prevents high frequency oscillations. D1 through D4 insure at least 2.5V differential between the op amp's inputs and its positive power supply under all conditions. R1 and R2 are zero scale and full scale adjustments respectively.

CALIBRATION PROCEDURE

Apply +23V ±7V and −5V ±1V to the converter with a current-measuring meter connected between the output and ground. Make the digital inputs all zeros, < +0.8V. Adjust R1 until the output current is 4.0mA. Now change the digital inputs to all ones, > +2.0V. Adjust R2 until the output current is 20mA. Calibration is now completed.

OUTPUT VOLTAGE COMPLIANCE

Output voltage compliance is V_{CC} −6V. For example, at V_{CC} = +16V, the output may go to a maximum of +10V without affecting output current. Thus, a 500Ω resistor would be the maximum load resistor at V_{CC} = +30V, V_{OC} = 24V, and R_L Maximum = 1.2kΩ.

SCALE MODIFICATION

Although the values shown are for the more common 4-20mA requirement, operation at 1-5mA or 10-50mA may be achieved by changing some components. For 10-50mA, change R6 to 40Ω; this makes the multiplying factor 20 instead of 8. For 1-5mA, replace the 2N6053 with a 2N5087, and change R6 to 400Ω.

CONCLUSION

A simple, low-cost process current converter has been shown with wide application in the controls industry. The design is tolerant of wide power supply variations, has high voltage compliance, and is easily calibrated. Reliability and cost are optimized by using only three integrated circuits, the Precision Monolithics DAC-08, REF-01, and OP-14, plus a few readily available discrete components.

REFERENCE

Crowley, B., "Circuit Converts Voltages to 4-20mA For Industrial Control Loops," **Electronic Design**, Jan. 5, 1976, page 116.

PARTS LIST

Circuit Symbol(s)	Description
A1	+10V Reference, PMI REF-01CJ
A2	8-Bit DAC, PMI DAC-08CQ
A3	Dual Op Amp, PMI OP-14CJ
C1-C3	0.1μF +80%/−20% 50V, Type CK-104
C4	100pF ±5% Mica, DM100ED101J03
D1-D4	Power Diode, 1N4001
Q1	NPN Transistor, 2N3904
Q2	PNP Power Darlington, Motorola 2N6053
R1-R2	50kΩ Potentiometer, Bourns #3006P-1-503
R3	4020Ω ±1%, RN55C4021F
R4	20kΩ ±1#, RN55C2002F
R5	800Ω ±0.1%, GR#8E16D800
R6	100Ω ±0.1%, GR#8E16D100

APPLICATION NOTE 22

SOFTWARE CONTROLLED ANALOG TO DIGITAL CONVERSION USING DAC-08 AND THE 8080A MICROPROCESSOR

by Will Ritmanich and Wes Freeman

The microprocessor is generally regarded as a flexible replacement for discrete logic devices. Yet most microprocessor-based designs still use numerous isolation and support packages for analog-to-digital (A/D) conversion, rather than using just software and the processor itself. There are many applications where the minimum system approach is both desirable and feasible. This application note describes a very simple, low-cost method of software controlled 8-bit A/D conversion using the Precision Monolithics DAC-08 and the Intel 8080A. Innovative software eliminates the need for peripheral isolation devices. Easily expandable to 10-bit or 12-bit A/D conversions, the technique may be emulated using other microprocessors having separate address and data busses.

8080A I/O INTERFACE CONSIDERATIONS

In order to communicate with any input/output peripheral device, the 8080A must be able to distinguish between its normal memory array and that particular I/O peripheral. Two techniques exist for accomplishing this, each with its own set of advantages and disadvantages.

The basic approach, used especially in large systems requiring greater than 32k memory, assigns the particular peripheral to an I/O "Port." This has the effect of isolating the I/O from the memory bus by the use of additional interface devices (generally the 8255 Programmable Peripheral Interface). Data transfers to and from the peripheral are then enabled by special instructions IN or OUT. This method has the advantage of allowing full 65k memory usage (Figure 1), but requires additional support circuits. Although conceptually simple, it restricts communications to the peripheral through the 8080A Accumulator.

For simple applications or where the full memory addressing capability of the 8080A is not needed, a powerful technique referred to as "Memory-mapped I/O" can be implemented. By utilizing unused portions of memory address space for I/O operations, the full instruction set used to control memory can also be used to operate on peripherals. This creates a powerful "new" capability for dealing with I/O. The major constraint, however, is that the peripheral must now conform to memory bus signals and timing.

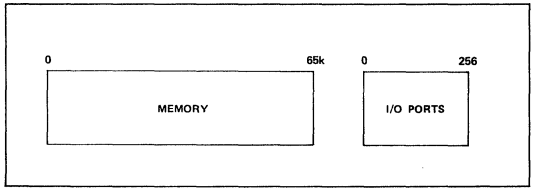


Figure 1. Isolated I/O

I/O CONTROL USING MEMORY-MAPPING

The convention used in establishing memory-mapped I/O is to assign address line A_{15} as the I/O control flag. Thus, if A_{15} is "zero," then memory is active, and if A_{15} is "one" then I/O is active. This creates a "map" of the memory as shown in Figure 2. Although other address lines could be used for the function, A_{15} is normally used because it is easier to control with software and allows full address capability for the lower 32k of memory.

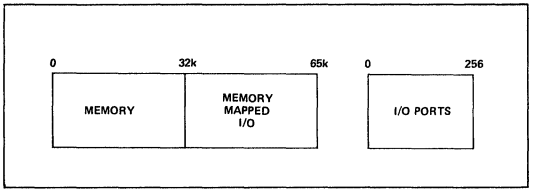


Figure 2. Memory-Mapped I/O

MEMORY-MAPPED I/O CONTROL SIGNALS

In order to manipulate memory-mapped I/O, it is necessary to generate the appropriate control signals. This is accomplished by gating MEMR and MEMW with A_{15} as shown in Figure 3. System bus characteristics are preserved and all instructions normally used to operate on memory can now be used on I/O as well.

SUCCESSIVE APPROXIMATION A/D CONVERSION

Because it provides the best tradeoff between speed and hardware/software complexity, the successive approximation method of A/D conversion has been selected. Figure 4 shows a simple analogy of this approach based on the use of a pan balance.

To measure some unknown weight, it is placed on one pan of the balance. By successively applying binarily-weighted

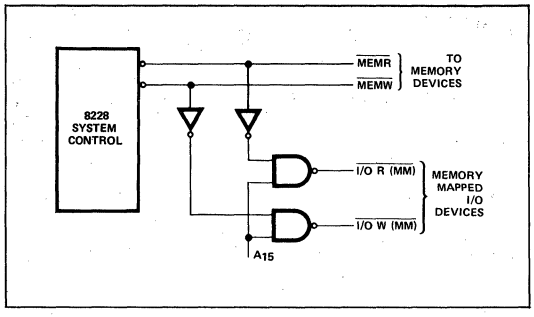


Figure 3. I/O Control Signal Generation

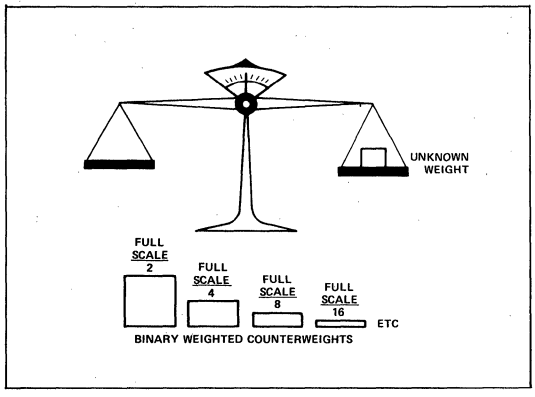


Figure 4. Successive Approximations Analogy

counterweights to the other pan until the scale is balanced, we can ascertain the portion of the unknown weight compared to that of the known full scale weight. The number of "trials" is made equal to the number of counterweights available by starting with the heaviest counterweight first, and either retaining it or rejecting it based on the comparison to the unknown. This process is repeated for the next heaviest and so on until all weights have been tried.

Electrically, this can be simulated by sequential comparisons between the output of a digital-to-analog converter and some unknown analog input. Figure 5 shows the basic circuit configuration.

At the start of a conversion, the most significant bit (MSB) of the DAC is turned on by the Successive Approximation Register (SAR) producing an output from the DAC equal to one-half full scale. The DAC's output is compared to the analog input by a comparator, and if the DAC output is greater than the unknown input voltage, the MSB is turned off. If, however, the DAC output is less than the unknown input, the MSB is allowed to remain on, and the next most significant bit is tried. Whether or not this second bit should remain on or be turned off is subject to the same criteria as before (Figure 6). This basic procedure is used to test all remaining DAC bit inputs.

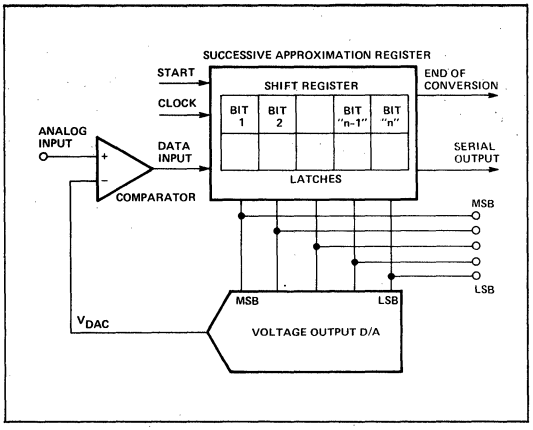


Figure 5. Basic Successive Approximation Circuit

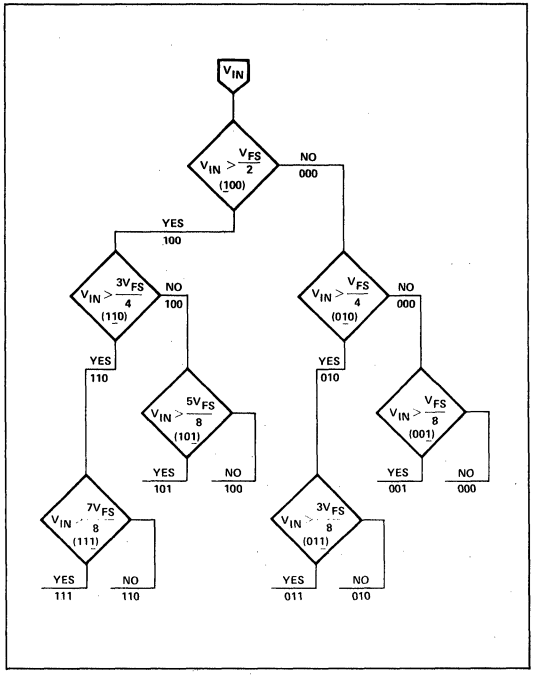


Figure 6. Flow Diagram for 3-Bit Successive Approximation A/D Conversion

LOGIC REPLACEMENT BY THE 8080A

The circuit illustrated in Figure 5 can be simplified by utilizing the logic capability of the 8080A to replace the SAR. The eight lowest order address bits control the data bit inputs to the DAC-08 (Figure 7). Table 1 contains the software used to accomplish this. Figure 8 depicts the corresponding flow diagram.

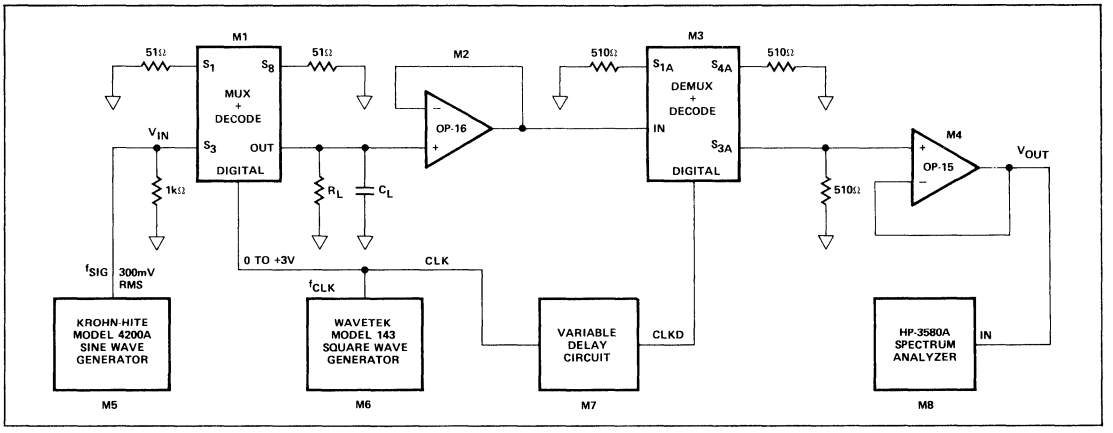
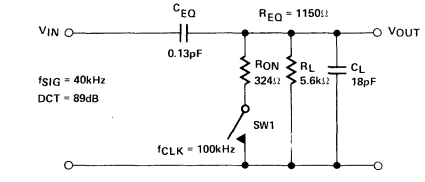


Figure 9. Dynamic Crosstalk Measuring System



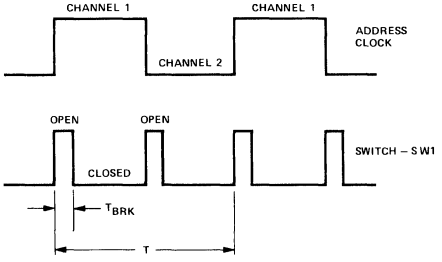
NOTE: SWI is a time dependent switch. Its characteristic is shown in Figure 10c.

a. TYPICAL DYNAMIC CROSSTALK ELEMENT VALUES

SYSTEM DYNAMIC CROSSTALK

f_{SIG}	f_{CLK}	R_L	R_{EQ}	DCT (C_{EQ} = 0.13pF)	DCT (C_{EQ} = 0.5pF)
Hz	HZ	Ω	Ω	dB	dB
10K	100K	10K	1718	97.1	85.4
10K	100K	22K	3463	91.0	79.3
10K	100K	33K	5059	87.7	76.0
10K	100K	47K	7090	84.7	73.0
10K	100K	100K	14.78K	78.4	66.7

b.



$T = 5\mu sec$

$T_{BRK} = 725nsec$

$R_{EQ} = 1089\Omega$

$T \equiv$ Period of Address Clock

$T_{BRK} \equiv$ Break-Before-Make Time

$$\text{If } R_L \gg R_{ON},\ R_{EQ} \cong \frac{R_{ON}(T - 2T_{BRK}(+ 2R_L T_{BRK})}{T}$$

c.

Figure 10. Computed Dynamic Crosstalk for Actual Multiplexer

The numbers shown in Figure 10 apply to the measurement system, but are unlikely in a real multiplexer. To satisfy sampling theory limitations, f_{SIG} must be less than one-half the sampling frequency. Assuming $f_{CLK} = 200kHz$ then each channel in a multiplexer is addressed for $5\mu sec$. This means that it takes $40\mu sec$ to sample all channels of an eight channel multiplexer. In other words, **each channel** is sampled at a 25kHz rate. Thus the maximum value of f_{SIG} would be 12.5kHz. Figure 10b gives values of dynamic crosstalk (DCT) which would be experienced if the values of R_{ON} and T_{BRK} shown in Figures 10a and 10b were used. The first DCT column lists the values for a C_{EQ} of 0.13pF (measured value of channel three). The second DCT column shows the performance for $C_{EQ} = 0.5pF$. The purpose for the second column is to point out how critical minimizing stray capacitance is to good crosstalk performance.

MEASUREMENT OF ADJACENT CHANNEL CROSSTALK

The system shown in Figure 11 was used to measure adjacent channel crosstalk (ACCT). M_1 drives the address lines of the MUX system and the gating input of M_4. By setting the period of M_4 (T_2) to $10\mu sec$, the pulse rate out of M_4 is controlled by the pulse rate of M_1 ($40\mu sec$) coming into the gate input of M_4. The output of M_4 is in the complement mode

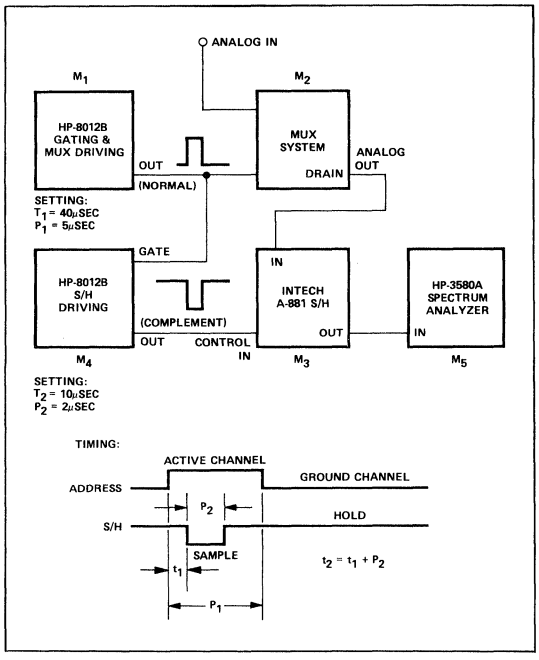
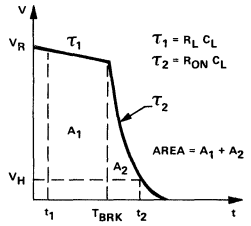


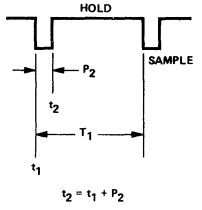
Figure 11. Adjacent Channel Crosstalk Measuring System

because the control input to M_3 causes the S/H to HOLD when the input is high (1). Thus the sample period occurs during the time P_2. M_4 also can delay its pulse relative to the pulse out of M_1, thereby allowing measurements of crosstalk versus t_1 (start of the sample time). This information is valuable because in many systems, a sample/hold is used with a successive approximation ADC to encode the analog output of the MUX. As will be shown, the ACCT can be made negligible if a sufficient time elapses before going to the HOLD mode for encoding the data. Since "time is money," the term "sufficient time" becomes important.

The nature of sample/holds and the nature of spectrum analyzers can cause some apparent discrepancies in the data observed by this measurement system. It is important to note the spectrum analyzer "sees" the average of **everything** that is presented to its input terminals. While it is true the sample/hold holds the last value it "saw," the spectrum analyzer also looks at the signal present during the sample/hold's sample time. Thus the equation which expresses the signal level present as a function of time must also account for the true averaging of the spectrum analyzer. Figure 12 shows the equations (12c) and the definitions of the terms used in the equations (12a and 12b). The term N_O is the **relative** signal level which the spectrum analyzer measures. If the model of the signal decay shown in Figure 12a is the correct one to explain the ACCT, then the computed value of N_O should correspond to the measured values. As will be shown in Figure 14, the agreement does in fact justify the model; however it was necessary to choose the measurement conditions **very carefully.**



a. VOLTAGE DECAY ON MUX OUTPUT



b. SAMPLE/HOLD

EQUATIONS:

1. $$\frac{V_O}{V_R} \equiv N_O = \frac{N_H(T_1 - P_2) + S_1 + S_2}{T_1}\text{; Where}$$

2. $$\frac{V_H}{V_R} \equiv N_H = EXP\left[\frac{-t}{\tau_1}\right],\ t \le T_{BRK}$$

$$= EXP\left[\frac{-T_{BRK}}{\tau_1}\right] EXP\left[\frac{T_{BRK} - t}{\tau_2}\right],\ t \ge T_{BRK}$$

3. $$\frac{A_1}{V_R} \equiv S_1 = \tau_1\left[EXP\left(\frac{-t_1}{\tau_1}\right) - EXP\left(\frac{-T_{BRK}}{\tau_1}\right)\right]$$

4. $$\frac{A_2}{V_R} \equiv S_2 = \tau_2\, EXP\left[\frac{-T_{BRK}}{\tau_1}\right]\left[1 - EXP\left(\frac{T_{BRK} - t_2}{\tau_2}\right)\right]$$

c.

Figure 12. Predicting the Measurement System Response

In order to get good correlation between lab data and theoretical predictions, it was necessary to use fairly long time constants ($R_L = 22k\Omega$ and $C_L = 1000pF$). With $R_L = 22k\Omega$ and $C_L = 50pF$ ($R_{ON} = 300\Omega$), the theoretical plot of ACCT (as measured on the spectrum analyzer) vs. t_1 is shown in Figure 13. Note that the data is plotted between 900nsec and 1025nsec. The curve shows that a **10nsec error in t_1 can cause a 6dB error** in reading on the spectrum analyzer. The results shown in Figure 14 confirm the necessity of using large capacitances to obtain predictable results. The theoretical curve tracks the actual data well in both cases; however the 1000pF curve is better than the 300pF curve. Notice that there is good agreement both at DC and at 4kHz.

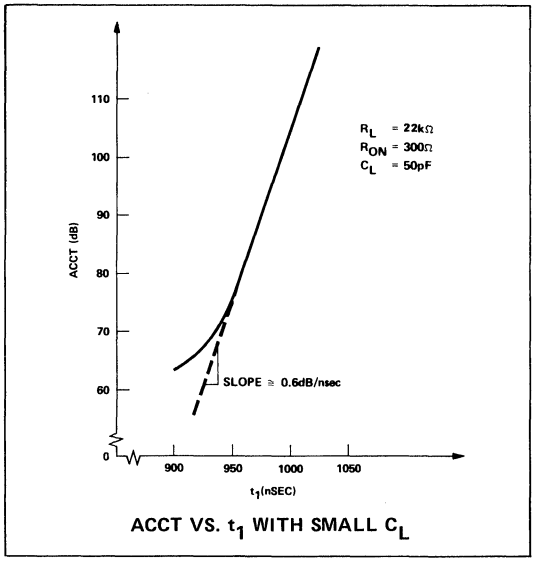


Figure 13. Measurement Errors Due To Small C_L

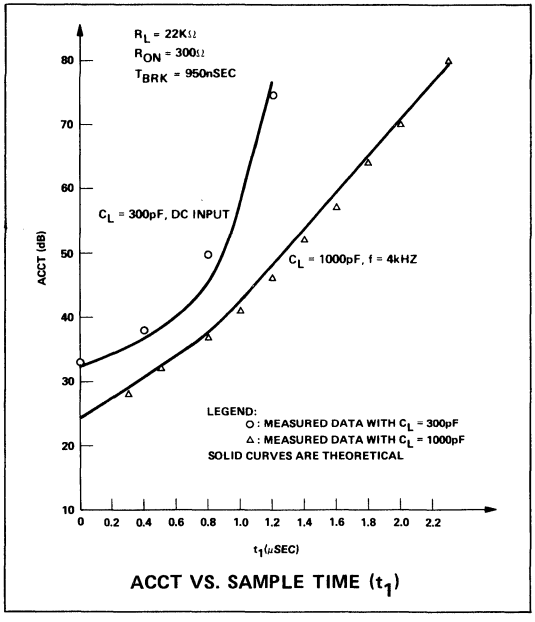


Figure 14. Agreement Between Measured and Computed ACCT

PREDICTING AND CONTROLLING ADJACENT CHANNEL CROSSTALK

The equations in Figure 12c can be used to predict how much adjacent channel crosstalk one might expect in an actual system. An all analog system will follow the MUX with a

A. Multiplexer-Demultiplexer System:

$N_H \equiv 0$ Therefore

1. $N_O = \dfrac{S_1 + S_2}{T_1}$, Where $T_1 = \dfrac{1}{f_{CLK}}$ x (No. of Channels)

2. $S_1 = \tau_1 \left[EXP\left(\dfrac{-t_1}{\tau_1}\right) - EXP\left(\dfrac{-T_{BRK}}{\tau_1}\right) \right]$

3. $S_2 = \tau_2 \; EXP\left[\dfrac{T_{BRK}}{\tau_1}\right]\left[1 - EXP\left(\dfrac{T_{BRK} - t_2}{\tau_2}\right)\right]$

Where $t_1 = T_D$ (Break-Before-Make Time of DEMUX)

$$t_2 = \frac{1}{f_{CLK}} - T_D$$

B. Multiplexer — Sample/Hold System

$S_1 = S_2 = P_2 \equiv 0$

4. $N_O = N_H = EXP\left[\dfrac{-t}{\tau_1}\right] \; t \le T_{BRK}$

$$= EXP\left[\frac{-T_{BRK}}{\tau_1}\right] EXP\left[\frac{T_{BRK} - t}{\tau_2}\right], \; t \ge T_{BRK}$$

Where: $t = t_H$ (Hold Command for Sample/Hold as measured from Address Change Time)

Figure 15. Predicting Adjacent Channel Crosstalk

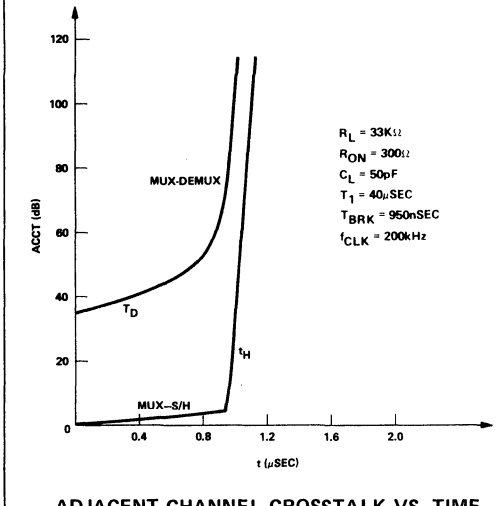


Figure 16. Computed ACCT vs Time for MUX-DEMUX and MUX-S/H Systems

demultiplexer, which will have its own break-before-make delay. An analog to digital system will have a sample/hold amplifier in front of the A/D converter. Since the equations which apply to these situations are different, they will be discussed separately. Figure 15 summarizes the conditions and the equations which apply to them.

Since there is no held voltage, then $N_H = 0$ in the multiplexer-demultiplexer system. This reduces N_O to the simple form shown in equation (1). S_1 and S_2 follow in equations (2) and (3). Since $t_1 = T_D$ (break-before-make time of the DEMUX), that time will have a significant effect on ACCT. The MUX-sample/hold system imposes the condition $S_1 = S_2 = P_2 = 0$; thus $N_O = N_H$. It will be instructive to compare the levels of ACCT in these two systems versus their appropriate times.

Figure 16 looks at a "typical" system which will give approximately one percent transmission error (33kΩ R_L and 300Ω R_{ON}), and has 50pF C_L. The value of C_L is somewhat on the high side (20pF being typical for MUX-08 connected to a buffer amp), but it does give a conservative value for analysis. What Figure 16 shows is rather startling. The adjacent channel crosstalk, while inherent in the multiplexer itself, can be eliminated in **both** systems by the proper timing. In the case of the sample/hold it is only necessary to delay the hold command for approximately 1.2μsec to have the ACCT vanish completely. This is no problem, since most sample/holds need at least 2μsec to accurately acquire the signal (this is particularly true of monolithic devices). The plot for the MUX-DEMUX system relates to T_D, which is **not adjustable** for a given DEMUX. What is possible is to add some delay to the address change for the DEMUX. In this way, the DEMUX will not "look" at the MUX output until the charge from the previous channel has had a chance to dissipate.

CONCLUSION

Table II summarizes the forms of crosstalk and lists ways of coping with them. Reduction of R_{ON} is helpful in all three cases. While T_{BRK} should be minimized as much as possible, it is important that no two channels are ON at the same time. In some cases, T_{BRK} is chosen such that even over temperature extremes, the break-before-make feature is maintained. Since all three components of crosstalk are present in a dynamic multiplexer, the "careful circuit board layout" is important even though it is not listed in the ACCT section.

Table 2. How to Handle Crosstalk

Crosstalk Component	Variation with f_{SIG}	Ways to Minimize Effects
Static	**6dB/octave**	• **Minimize R_{ON}** • **Reduce stray capacitance (C_{EQ}) by careful circuit board layout.**
Dynamic	**6dB/octave**	• **Minimize R_{ON}** • **Minimize f_{CLK}** • **Minimize T_{BRK}, but $T_{BRK} > 0$ is needed to prevent shorting channels together.** • **Minimize R_L** • **Reduce stray capacitance (C_{EQ}) by careful circuit board layout.**
Adjacent Channel	**NONE**	• **Minimize R_{ON}** • **Minimize f_{CLK}** • **Minimize T_{BRK}, but $T_{BRK} > 0$ is needed to prevent shorting channels together.** • **Minimize R_L and C_L** • **WAIT before allowing sample/hold or DEMUX to measure MUX output.**

This paper has pointed out the fact that static crosstalk (given on multiplexer data sheets) is only **one** of the **three** components of crosstalk. The models for static and dynamic crosstalk are relatively simple and were discussed to show how they are related. The most troublesome component of crosstalk (adjacent channel crosstalk) was shown not to be quite so straight-forward. For one thing, adjacent channel crosstalk (ACCT) is **not signal frequency dependent** as are CT and DCT. The mechanism which governs this form of crosstalk is stored charge on the MUX node. While CT and DCT must be minimized by careful layout and once present in the multiplexer cannot be reduced, such is not the case with ACCT. Even though ACCT is present in the multiplexer, the proper timing of demultiplexer or sample/hold commands can effectively eliminate ACCT from the total system.

APPLICATION NOTE 36

DAC-08 CONTROL OF 555 TIMERS

by Kishor Patel

INTRODUCTION

This application note describes a digitally or microprocessor controlled one-shot and an astable multivibrator using two of the industry's most widely used low cost building blocks, the PMI DAC-08 8 bit DAC and the 555 timer. Digital control ranges of 255 to 1 and 510 to 1 are shown for one-shot and astable applications allowing periods of 18μsec to 1.4 seconds and frequencies of 1 Hz to 60 KHz.

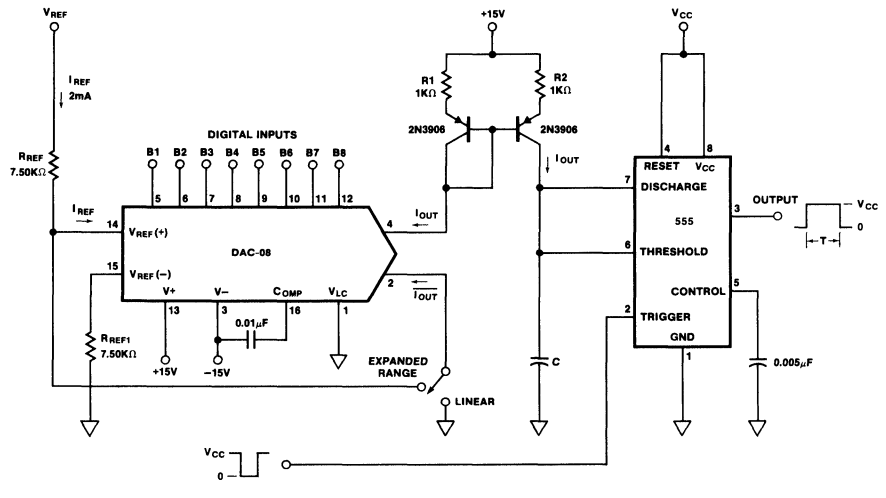
ONE-SHOT LINEAR MODE OPERATION

In the one-shot mode of operation, the time delay or the one-shot period is determined by a constant current source and a capacitor. A digitally programmable constant current source is made using the DAC-08 and two PNP transistors. The DAC-08 is a current sink; the two PNP transistors are used as a current mirror which reverses the direction of the DAC's sink current forming a current source. The current source charges the timing capacitor, causing the voltage across the capacitor to increase linearly at the rate of $\left\{\frac{I_{OUT}}{C}\right\}$ volts per second from approximately zero volts to $\frac{2}{3}V_{CC}$ of the 555 timer.

The one-shot's period, T, is basically an RC product with two other control factors. The R is fixed and represented by R_{REF} which sets up the correct I_{REF} current for the DAC. With the fixed R_{REF}, the one-shot period is directly proportional to the value of the timing capacitor C (see Table 1). The other two controlling factors are the DAC's digital inputs and the ratio of the timer's V_{CC} to the DAC's V_{REF}. The one-shot period is inversely proportional to the normalized digital input value and directly proportional to the V_{CC} to V_{REF} ratio as illustrated in Fig. 2. When operated in the linear mode, a 255 to 1 control range of the one-shot's period is achieved.

BASIC DESIGN

As shown in Fig. 1, this design involves a series of conversions from a digital input to an analog current to a threshold voltage and finally to a time delay or a frequency. A DAC-08 converts the digital input to an analog current



$$\text{ONE-SHOT PERIOD, } T = \frac{2}{3}\,\frac{R_{REF}C}{\{D\}}\,\frac{V_{CC}}{V_{REF}} \text{ FOR LINEAR MODE}$$

$$\text{ONE-SHOT PERIOD, } T = \frac{2}{3}\,R_{REF}C\,\frac{V_{CC}}{V_{REF}}\left[\frac{2-\{D\}}{\{D\}}\right] \text{FOR EXPANDED MODE}$$

Figure 1. Digitally Controlled One-Shot

Table 1. One-Shot Linear Mode Timing Table

	ONE-SHOT PERIOD (msec)					
	V_{CC} = 15V V_{REF} = 15V			V_{CC} = 5V V_{REF} = 15V		
Input Digital Code	C = 1μF	C = 0.1μF	C = 0.01μF	C = 1μF	C = 0.1μF	C = 0.01μF
11 11 11 11	5.2	0.505	0.049	1.72	0.160	0.0176
00 00 00 01	1440	134	13.8	455	43	4.8

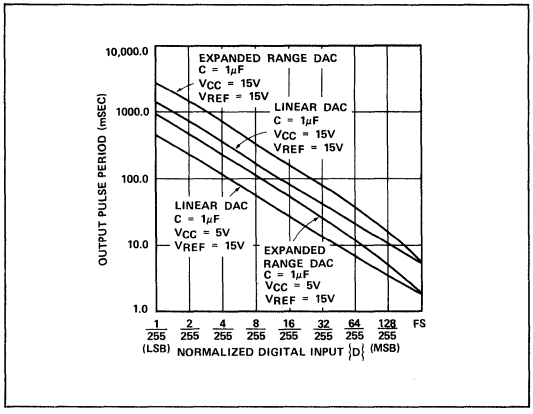


Figure 2. One-Shot Period vs Digital Input

which is then converted to a voltage by a two transistor current source and a capacitor. The voltage is then converted to a time delay or frequency by a timing capacitor and the 555 timer.

ONE-SHOT EXPANDED MODE OPERATION

Range is doubled to 510 to 1 by operating the DAC in the expanded range mode with the DAC's I_{OUT} fed forward from the reference input node of the DAC. Expanded range mode timing is shown in Table 2 and in the graph of Fig. 2.

ASTABLE MODE OPERATION

An astable multivibrator is made in a similar fashion in Fig. 3. A DAC-08 and two PNP's form a current source driving the timing capacitor (C) and a discharge resistor (R_B). The timing capacitor is charged linearly by the current source and discharged exponentially through R_B. Once again, the

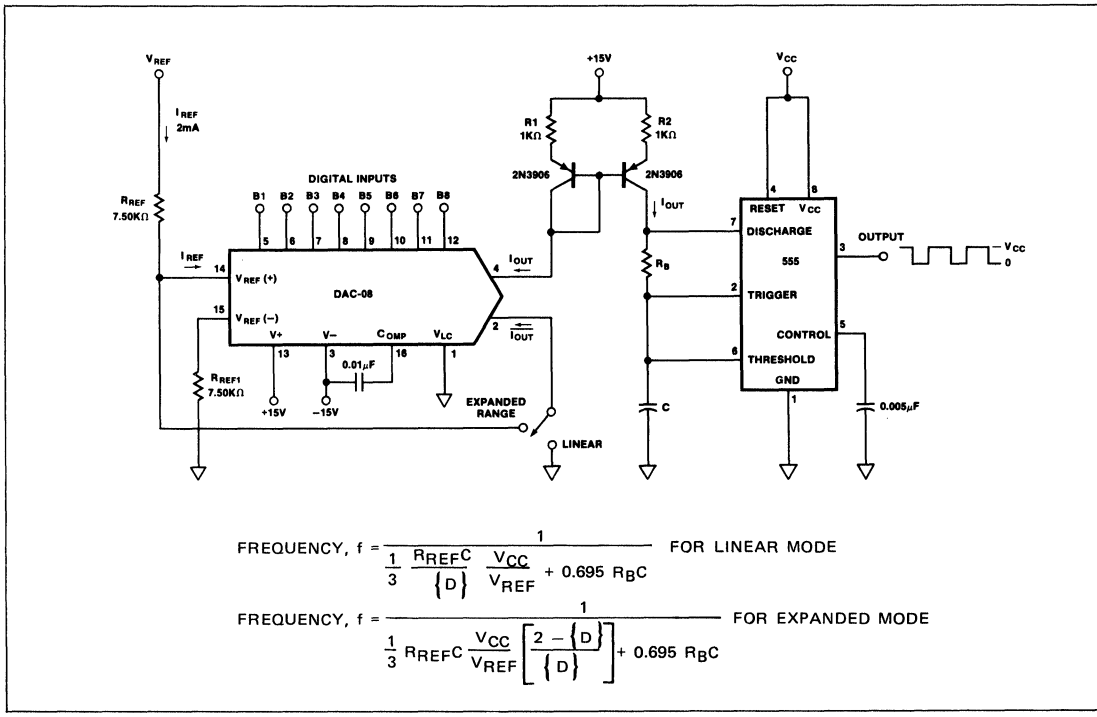


Figure 3. Digitally Controlled Astable Multivibrator

digital DAC input and the ratio of the timer V_{CC} to the DAC's V_{REF} provide additional control on the multivibrator's frequency. The digital input has directly proportional control while the V_{CC} to V_{REF} ratio has an inversely proportional control of frequency.

Frequency range is not fully 255 to 1 as expected but approximately 220 to 1, because the discharge time (output low) of a cycle is invariable for any digital input being determined by the product of R_B and C. Frequency is shown in Table 3 and in Fig. 4. Expanded range operation doubles frequency range as it did in the one-shot application. Frequency is shown in Table 4.

MICROPROCESSOR CONTROL

Both the one-shot and the astable multivibrator can be microprocessor controlled. Fig. 5 shows the implementation of a microprocessor controlled one-shot. The eight bit latch (74LS377) is used to interface between the data bus and the DAC. Stable data is latched in by a positive going edge of an address coincident pulse. After the data is latched, a buffered negative going address coincident pulse can be used to trigger the one-shot. The astable multivibrator is implimented similarily except for elimination of the buffer and the trigger pulses which are not required.

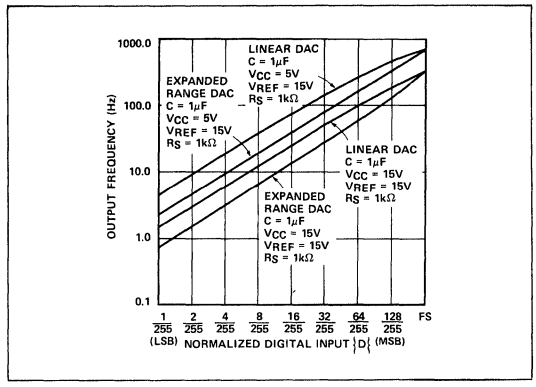


Figure 4. Multivibrator Frequency vs Digital Input

CONCLUSION

Digitally controlled one-shot and astable multivibrator with a wide range of outputs have been implemented. The one-shot has a 255 to 1 (8 Bit dynamic) time period range and the astable multivibrator a 220 to 1 frequency range. When the DAC is operated in the expanded modes, these ranges are doubled.

Table 2. One-Shot Expanded Mode Timing Table

	ONE-SHOT PERIOD (msec)					
	V_{CC} = 15V V_{REF} = 15V			V_{CC} = 5V V_{REF} = 15V		
Input Digital Code	C = 1μF	C = 0.1μF	C = 0.01μF	C = 1μF	C = 0.1μF	C = 0.01μF
11 11 11 11	5.2	0.495	0.049	1.72	0.160	0.0176
00 00 00 01	2900	280	26	970	87	8.4

Table 3. Astable Linear Mode Frequency Table

	ASTABLE MULTIVIBRATOR FREQUENCY (Hz)					
	R_B = 1kΩ; V_{CC} = 15V; V_{REF} = 15V			R_B = 1kΩ; V_{CC} = 5V; V_{REF} = 15V		
Input Digital Code	C = 1μF	C = 0.1μF	C = 0.01μF	C = 1μF	C = 0.1μF	C = 0.01μF
00 00 00 01	1.49	14.7	156	4.86	49.8	433
11 11 11 11	328	3,279	33,333	717	7,273	60,241

Table 4. Astable Expanded Mode Frequency Table

	ASTABLE MULTIVIBRATOR FREQUENCY (Hz)					
	R_B = 1kΩ; V_{CC} = 15V; V_{REF} = 15V			R_B = 1kΩ; V_{CC} = 5V; V_{REF} = 10V		
Input Digital Code	C = 1μF	C = 0.10μF	C = 0.01μF	C = 1μF	C = 0.1μF	C = 0.01μF
00 00 00 01	0.74	7.69	79.9	2.42	24.7	217
11 11 11 11	328	3,279	33,333	714	7,299	60,241

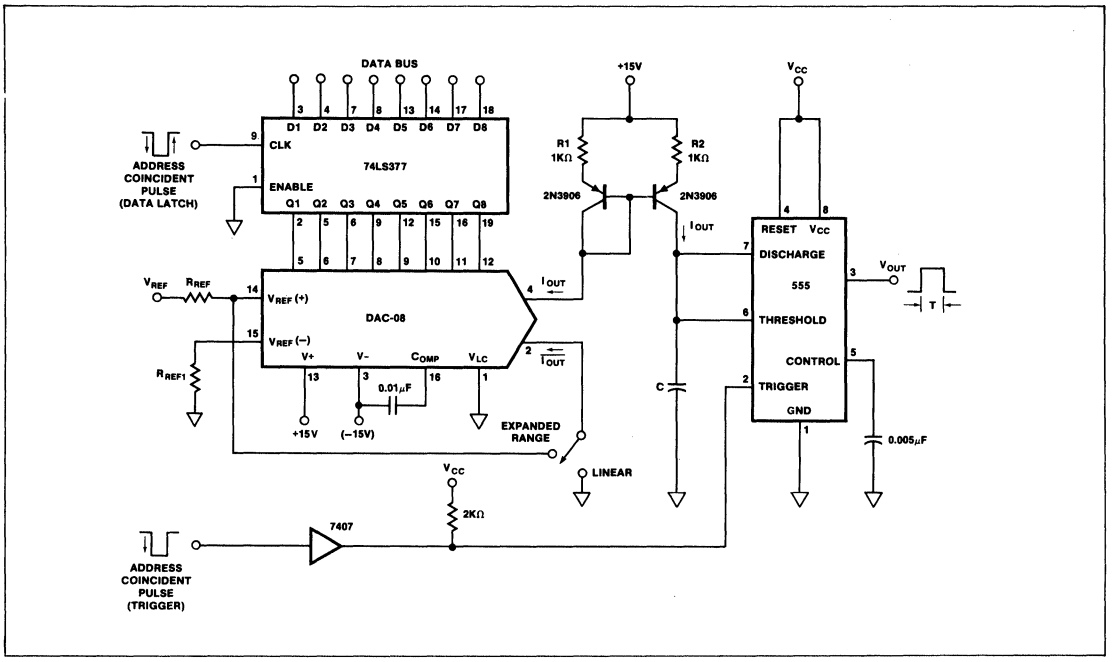


Figure 5. Microprocessor Controlled One-Shot

APPLICATION NOTE 37

EIGHT CHANNEL CODEC DEMONSTRATOR

by B. W. Berry

Precision Monolithics, Inc. has developed a CODEC demonstrator system in order to show the use of their line of telecom devices in a shared-channel system. These circuits provide a working digital transmission system incorporating eight analog input channels digitally interfacing to eight output channels. The circuit design was completed so that a single analog printed circuit board could be used either for encoding eight channels or decoding eight channels. A single digital timing and interface board is used to provide system clocks and the parallel digital data bus from transmitter to receiver. All board layouts and schematics are available from PMI. The design uses pluggable connections so that, if desired, the encoding portion or the decoding portion of the system can be tested separately. The user need only provide three voltage supplies (±15VDC, +5VDC), the appropriate filters and any applicable transmission test equipment.

HARDWARE

The entire eight-channel system consists of twenty-one integrated circuits mounted on three printed circuit boards. Two of the boards, as mentioned, are a common layout which is used for the analog functions of the system. The analog board used for the encoder (analog-to-digital conversion) requires the addition of a COMDAC® (DAC-86, 87), a MUX-88, a SMP-81, a CMP-01, and a REF-02. The other analog board is used for the decoder (digital-to-analog conversion) with the addition of a DAC-86, MUX-88, REF-02, and an OP-16. The general schematic and parts list for the analog boards is shown in Figures 1 and 2.

The control board is a T²L circuit of twelve devices designed to provide three basic functions, a) the successive approximation register with interface to the DAC-86, b) the clock for the encode portion of the demonstrator, and c) the digital

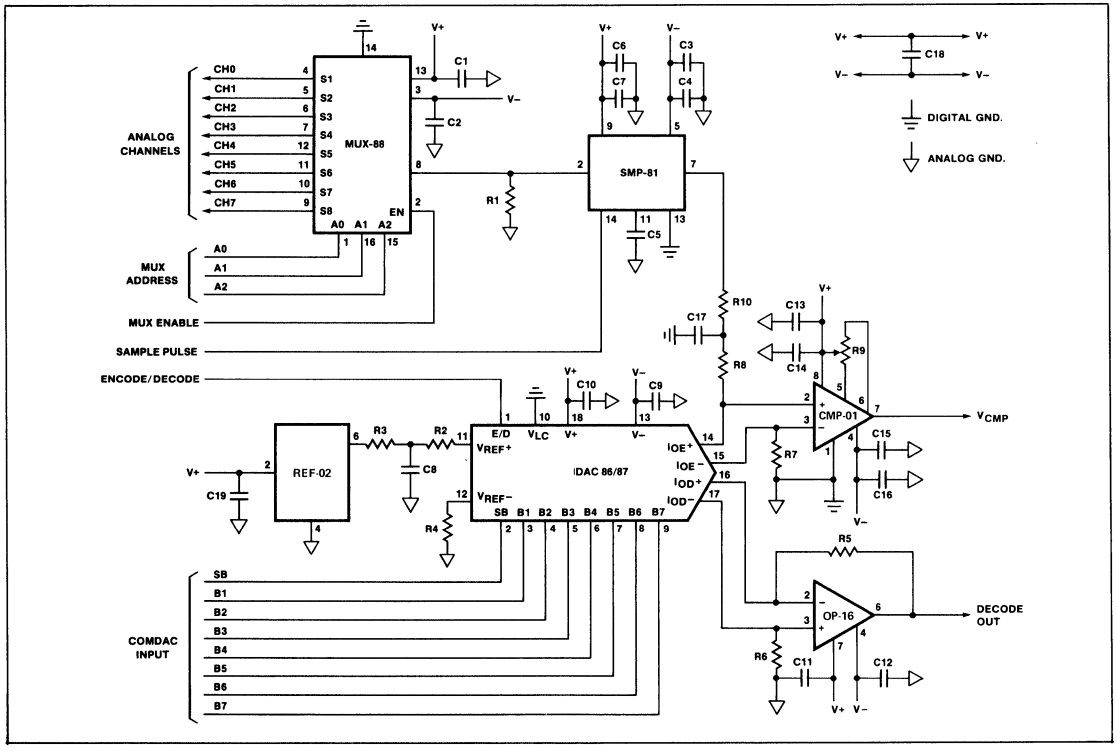


Figure 1. COMDAC* Encoder/Decoder Analog Circuit Board

*COMDAC IS A REGISTERED TRADEMARK.

TRANSMIT (Eight-Channel Encoder)	RECEIVE (Eight-Channel Decoder)
MUX-88	MUX-88
SMP-81FY	COMDAC®DAC-86EX (87)
COMDAC®DAC-86EX (87)	OP-16F
CMP-01EJ	REF-02
REF-02	

RESISTORS

R1 – 20K	R6 – 2.49K
R2 – 330	R7 – 2.49K
R3 – 9.1K	R8 – 1.5K
R4 – 10K	R9 – 2K (POT)
R5 – 2.49K	R10 – 1.0K

CAPACITORS

C1, C2, C4, C7, C8, C9, C10, C11, C12, C13, C15, C18, C19	0.1μf
C3, C6, C14, C16	10μf
C5	5000pf
C17	100pf

Figure 2. Parts List – Analog Board

interface between the encode and decode sections. The encoder clock design is a multiple frequency clock, the usefulness of which is treated in a later section, generated from a programmable read-only memory frequency divider. The PROM was used to provide flexibility in changing the clock waveforms if the user so wishes. The resultant clock waveforms are also described later; the circuit schematic is shown in Figures 3a and 3b. The PROM data is listed in Figure 4. The digital interface is provided by using a standard 8-bit, parallel-in, parallel-out latch updated as the successive approximation process is completed for each input channel. The remainder of the circuit consists of the SAR and the multiplexer address counters. A parts list for the circuit is shown in Figure 5. A complete circuit schematic for the digital board is shown in Appendix A.

The boards are interconnected by use of four mini-dip connectors and cables, a 16-pin and 14-pin from each analog board to the controller. The lead designations of the two connectors are shown in Figure 6. The input and output channels are accessible through "banana"-type plugs; this allows optional connections from the transmission line in order to try different types of filters and line interface circuits. The two analog boards require ±15VDC and "banana" plugs are provided to interface to the appropriate supplies. The control board requires +5VDC only. The entire system layout is shown in block diagram in Figure 7.

SYSTEM OPERATION AND DESIGN

To achieve a workable system configuration, the encoding and decoding operations were approached as two separate designs. The entire transmission link was then connected to complete the end-to-end tests.

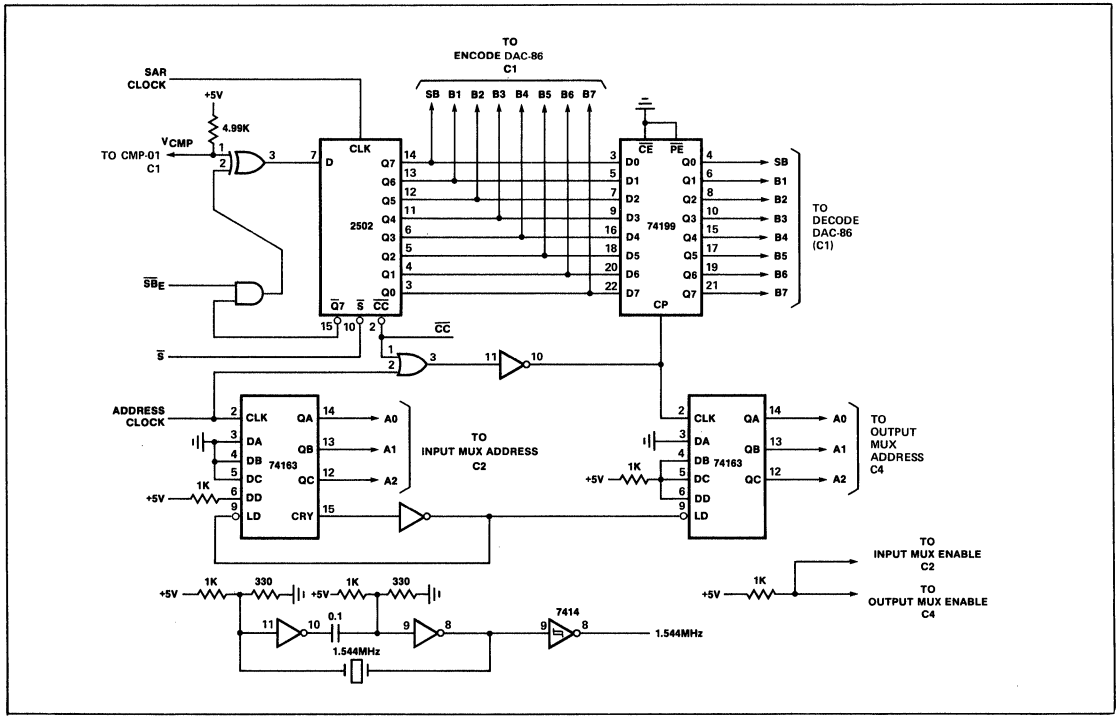


Figure 3A. Encoder/Decode Controller

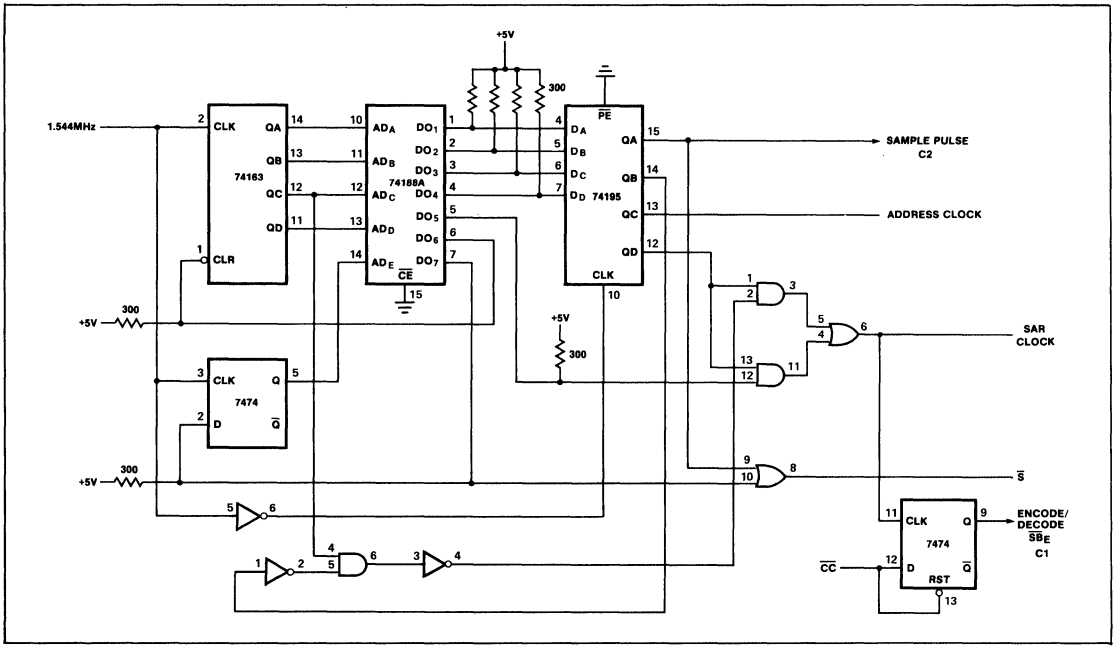


Figure 3B. Encode Clock

ADDRESS	DATA (MSB–LSB)	ADDRESS	DATA (MSB–LSB)
00	20	0C	27
01	28	0D	27
02	20	0E	2F
03	21	0F	6F
04	39	10	67
05	2B	11	67
06	23	12	6F
07	2B	13	6F
08	23	14	67
09	2B	15	67
0A	23	16	6E
0B	2F	17	0E

MSB = $D0_8$
LSB = $D0_1$
Address 18 – 1F – Unused.

Figure 4. PROM-Based Clock

PARTS		PARTS	
7404	2	74163	3
7408	1	74188A	1
7414	1	74195	1
7432	1	74199	1
7474	1	2502	1
7486	1	1.544MHz Crystal	

Figure 5. Parts List – Controller

CONNECTORS

PIN #	C1 (C3)	C2 (C4)
1	+5	+5 Gnd
2	+5	Sample Pulse
3	+5	MUX Enable
4	VC MP	A0 – Address
5	+5 Gnd	+5 Gnd
6	+5 Gnd	A2 – MUX Address
7	+5 Gnd	A1 – MUX Address
8	B7 – LSB	+5 Gnd
9	B6	+5 Gnd
10	B5	+5 Gnd
11	B4	+5 Gnd
12	B3	+5 Gnd
13	B2	+5 Gnd
14	B1	+5 Gnd
15	SB – MSB	+5 Gnd
16	Encode/Decode	+5 Gnd

*C2 is 14 Pin – C1 is 16 Pin

Figure 6. Pin Designations – System Connectors

The accuracy of the encoder, the analog-to-digital converter, is dependent upon several factors. The first, and most significant, is the speed (settling time) of the companding DAC in conjunction with the comparator. Other factors are switching time of the multiplexer, acquisition time of the sample-and-hold, hold-step settling time of the sample-and-hold, and output noise of the sample-and-hold and

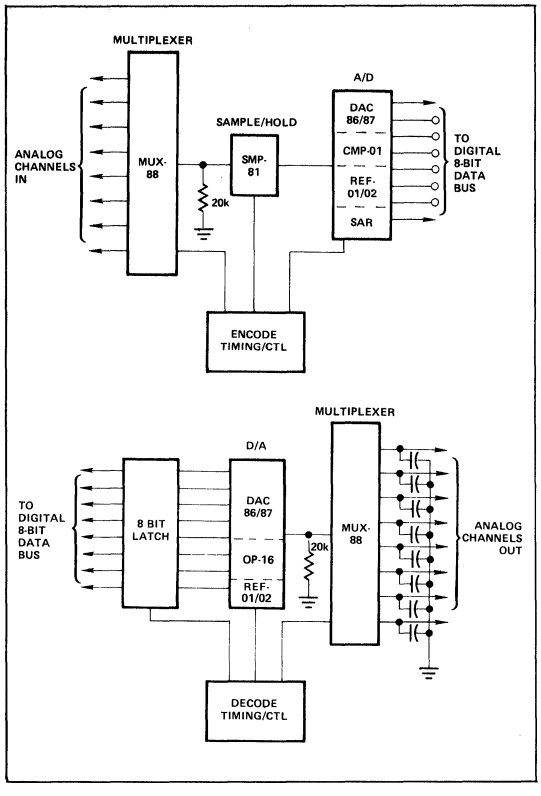


Figure 7. Eight-Channel System Layout

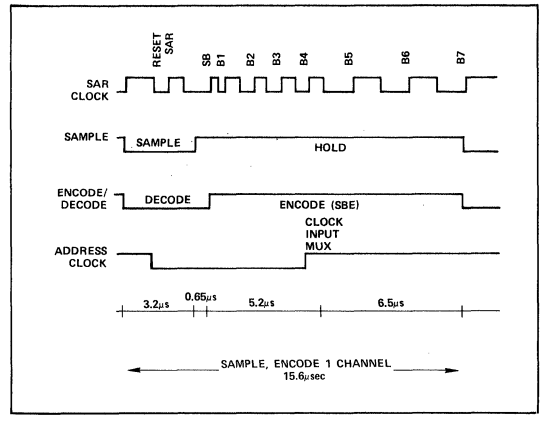


Figure 8. Encoder Timing Waveforms

multiplexer. All of these characteristics had to be considered while developing the encoder circuit.

In a companded A/D conversion, using a successive approximation method, different digital bits require different settling times. There is a constant increase in the settling time required as one goes from the sign bit to the chord bits and then to the step bits. This increase in settling time is partially caused by the scaled current sources used to design a companding D/A and is most affected by the magnitude of the voltage level being converted. So as the output currents of the DAC-86 become smaller (at smaller voltage levels), the comparator is less responsive. Also as the less significant bits are clocked in, the situation becomes more critical since progressively smaller current changes are provided to force the comparator to change output state. The encoder clock waveforms, shown in Figure 8, depict a system approach to accommodate these timing characteristics. The governing design criteria was that a limited amount of time is available to complete the successive approximation of the analog signal (for eight channels, with a sampling frequency of 8kHz, this means 15.6μs) and the optimum clock must fit within this period. All functions (including sampling, encoding, switching) must therefore be completed with an acceptable accuracy, within this time constraint. To achieve accurate data acquisition with the sample-and-hold, a sample pulse of 3.2μs was used. Once the pulse goes from sample to hold, there is a waiting time required to allow the sample-and-hold output to settle to the "held" value, 650ns is the time added. Since the sign bit is the fastest transition, the basic system clock (1.544MHz) is used for the first SAR clock period. The clock frequency is then halved to clock in the chord bits (B1, B2, B3), the next "slowest" transitions. Finally, the clock frequency is halved again to allow for the step bits (B4-B7), a frequency of 386kHz. The times required for the different bit conversions are shown in Figure 8. The SAR is reset during the sampling period and once the sample circuit has entered the hold mode, the input multiplexer's address is changed. This provides ample time for the MUX to switch to the next analog input with little effect on the adjacent waveforms. In addition, to further minimize interchannel crosstalk, a 20kΩ resistor to ground is added to the multiplexer output.

To provide sufficient noise immunity from the sample-and-hold to the comparator, a simple filtering circuit using a 100pF capacitor is added. A 4.9kΩ resistor to +5V from the comparator output aids in increasing the DAC-86 and comparator speed. In order to test the encoder without adding a decoder, a high-precision voltage source (DC levels) was used as an input to one or more channels of the A/D circuit. The data output (one byte every 15.6μs) was sampled and stored in a logic analyzer. By reviewing the samples for each channel, and comparing the data from all channels of the eight channel system, the effects of changes in the clock on the accuracy of the design could be observed. By inputting a steady-state value, the data out would not only demonstrate the "consistency" of the A/D conversion but also make obvious any adjacent channel effects that were produced.

The analyzer sampling also presents a method of initializing the system components. By grounding all inputs and digitally sampling the data bus output, the zero level can be set so as to produce an alternating series of data bytes equivalent to 0 volts (10000000 and 00000000).

A similar design approach was used in developing an eight-channel decoder. In this case, the response time of the DAC-86 and op amp offers little problem since an eight-channel decoder is relatively slow. However, the accuracy of the devices does become important. The design considerations become, therefore, the nonlinearity of the DAC-86 in

conjunction with the switching time and charge injection of the multiplexer. The DAC-86 is manufactured to strict linear specifications, which assures both excellent decoding linearity and absolute accuracy. The multiplexer is used both as a switch to demultiplex the output waveforms and as a holding circuit by adding capacitance to the output leads. One effect seen in the multiplexer is that as a channel is switched off, there is a charge injected onto the output. This charge is not normally obvious in a MUX design, however, when working into a high impedance (such as a filter) and with capacitors on the source leads (outputs), the charge can add an offset to the waveform. To minimize the effect, a large capacitor (0.1μF or greater) is added. Since the charge pulse is a short duration signal, the signal on the larger capacitor will be less affected by the charge than if a smaller component was used.

In terms of a system decoder design, this circuit could be used for more than eight channels. The op amp and DAC-86 are both capable of responding to more output channels. An eight-channel system was incorporated to remain compatible with the analog board that is used in the demonstrator. In order to decode more channels (>12), the output capacitance on the demultiplexer would need to be reduced. The other circuit components would remain the same.

The decoding circuitry can be tested separately by adding a series of data bytes and monitoring the output channels. The CCITT recommendation for testing PCM systems includes a method of testing a decoder by introducing a standard sequence of digital data words in order to produce a 1kHz sinusoid at a nominal level of 0dBm0.* This method proved useful in "debugging" the circuit design prior to attempting the end-to-end tests.

SYSTEM TESTS

Once the encoder and decoder were functioning separately, the entire system was connected with the appropriate interfacing to allow for full-system transmission tests. The measurements taken were the standard set of PCM specifications observed in the majority of data sheets for telecommunication oriented products. These tests included signal-to-total distortion, gain tracking, intelligible crosstalk, and idle channel noise.

There are two different methods of performing the tests. For the U.S. standards, a sinusoid signal is used as the channel input and the measurements are taken around the base (test) frequency. For the European tests, a pseudo-random or "white" noise source is preferred as the input signal. The test results discussed here were obtained with the U.S. testing procedures; similar test results have been achieved using European test methods.

The test set-up for signal-to-total distortion and gain tracking measurements is shown in Figure 9. The results are plotted in Figures 10 and 11. As is seen, each test was performed with both the C-Message Weighting and the 3kHz Flat response terminating configurations. The results using the μ-law parts (DAC-86) are represented. In terms of signal-to-total distortion, the system exceeds the recommended standard at all input levels by 2dB or greater. The system is also well within the recommended gain tracking limits for both terminations.

The crosstalk and idle channel noise measurements are given in Figure 12. One consideration of the system design, in terms of performance, was that the most difficult characteristic for a shared-channel system to minimize is the intelligible crosstalk specification. The design is directed

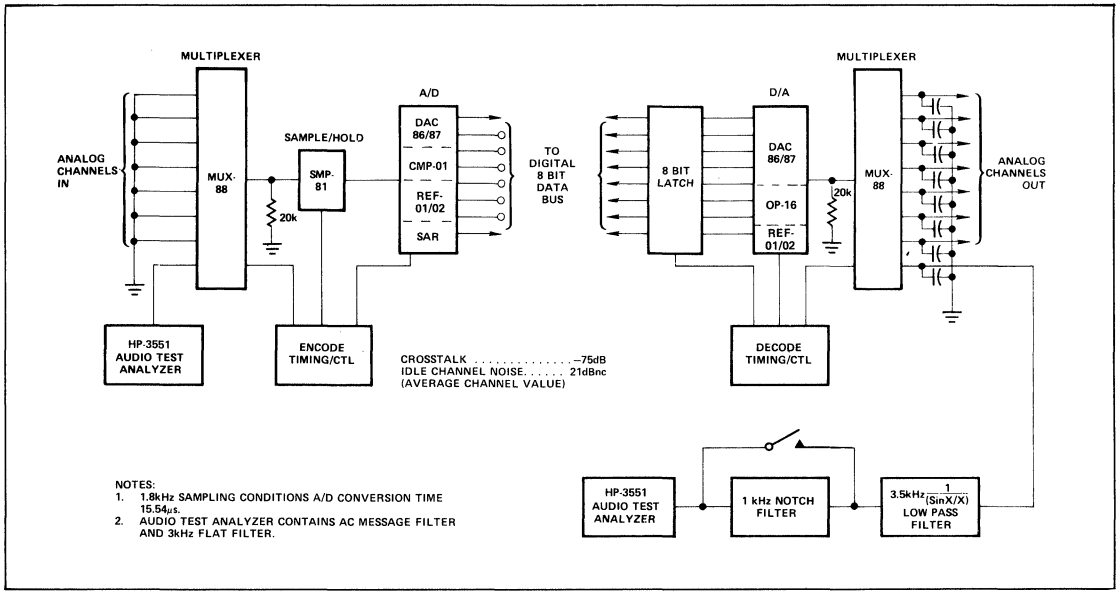


Figure 9. Eight-Channel Test Configuration

*Reference — CCITT Sixth Plenary Assembly (1976), Orange Book Vol. III-2

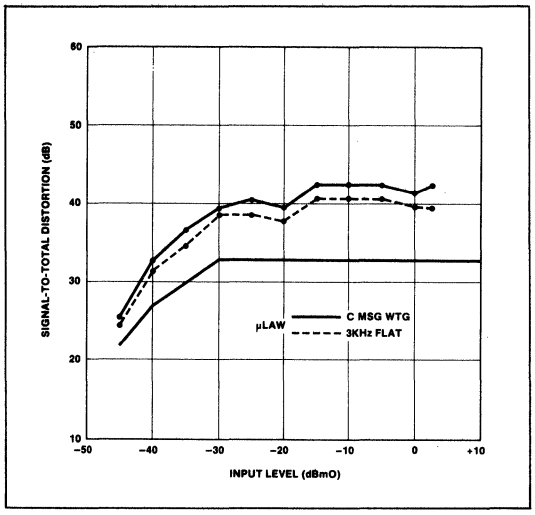


Figure 10. Signal-To-Quantizing Distortion vs. Input Level

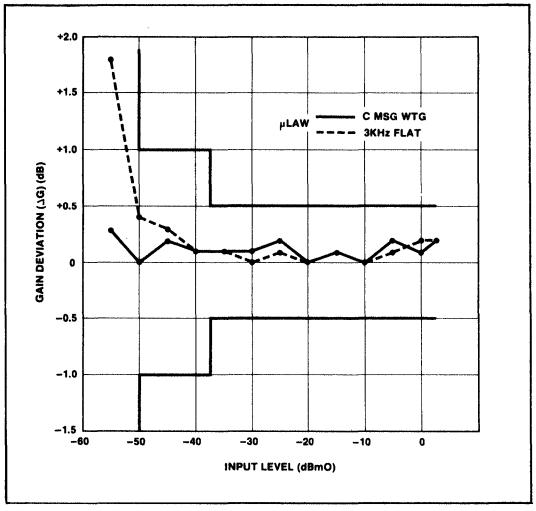


Figure 11. Gain Tracking

toward optimizing this measurement. The idle channel noise is at the system recommended level when measured without output filtering. It is further reduced by adding a PCM receive filter on the decoder multiplexer.

CONCLUSIONS

The circuitry just discussed is meant to represent one approach to designing an eight-channel, shared CODEC system. It is not meant to be the only design, but provides a working system upon which to base further engineering development. It should be noted that in terms of transmission testing, the demonstrator is an end-to-end system. The configuration presents the users with a complete circuit enabling them to observe the individual device characteristics significant in producing a shared-channel design.

The completed eight-channel CODEC demonstrator is shown in Figure 13, mounted in its carrying case.

IDLE CHANNEL NOISE

CHANNEL	NOISE (dBm0)	CHANNEL	NOISE (dBm0)
1	−66.9	5	−62.6
2	−67.6	6	−65.3
3	−67.0	7	−67.0
4	−67.2	8	−61.8

CROSSTALK

FREQUENCY	INTELLIGIBLE CROSSTALK
300 – 2900Hz	≤−78dBm0
2900 – 3400Hz	≤−70dBm0

Figure 12. Idle Channel Noise and Crosstalk

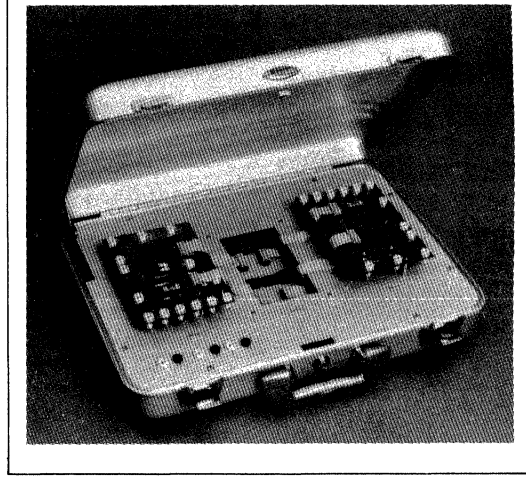


Figure 13. CODEC Eight-Channel Demonstrator

The demonstrator provides a starting point from which most characteristics important to both shared-channel and single-channel designs can be manipulated to allow for improvements in transmission quality. To be able to develop a realistic transmission design, the system engineer needs to consider more than just the coder/decoder devices. A complete multiple channel system, such as the PMI eight-channel demonstrator, allows the user to observe the complete system performance as it is affected by the individual system components.

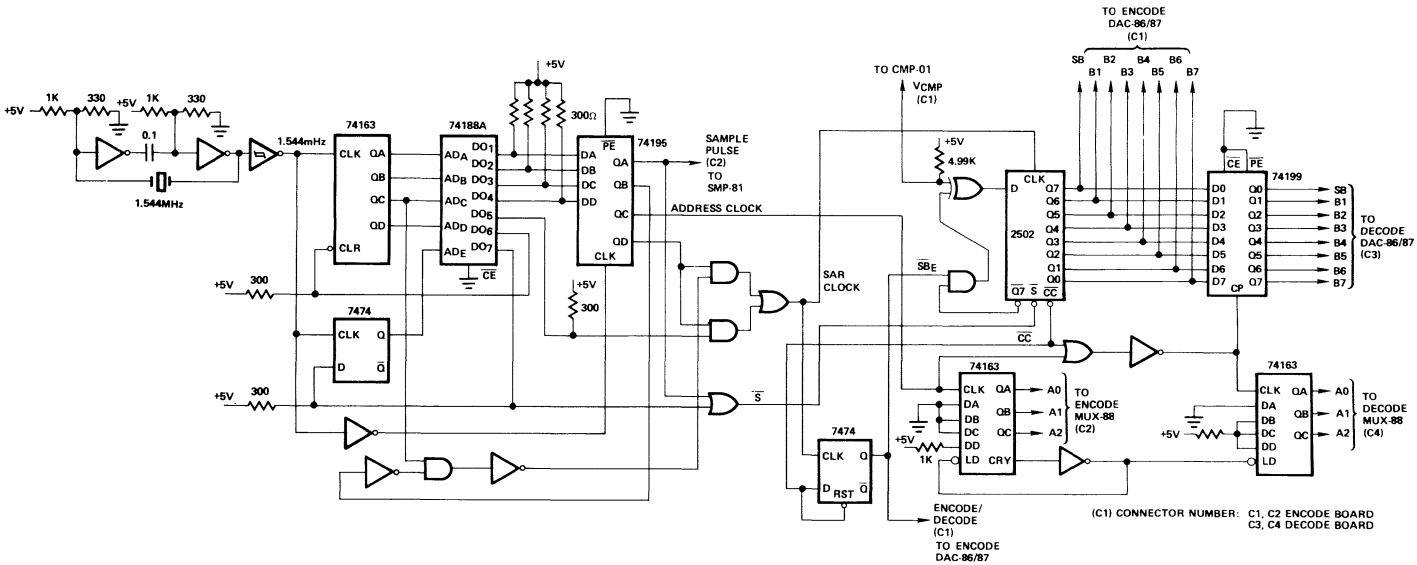


Figure A-1. Circuit Schematic

APPLICATION NOTE 38

FOUR-CHANNEL SHARED CODEC

by B.W. Berry

FOUR-CHANNEL SHARED CODEC

A four-channel CODEC assembled from LSI components is a cost-effective digital transmission system requiring a relatively small number of devices. The system makes use of a single COMDAC®* companded DAC-86 or DAC-87 digital-to-analog converter for both encoding and decoding (see Figure 1). The timing of the circuitry is compatible with ATT and CCITT system specifications.

Each channel is sampled at the standard 8kHz rate. With four channels this allows approximately 31.2μs to encode the sampled analog input and to decode the received digital signal for the same channel. To simplify the timing system requirements equal amounts of time were allowed for encoding and decoding, thus permitting 15.6μs for the more critical encode portion of the cycle. The encode/decode clocking scheme for this CODEC was incorporated directly from a successful eight-channel CODEC system which has been published as PMI Application Note 37. One original feature of the four-channel design was the use of dual eight-channel multiplexer ICs to switch the four channels. This results in a system whose interchannel crosstalk is practically negligible. Crosstalk figures of −85dB have been observed. This article describes the design procedure and reviews the transmission characteristics of the completed system.

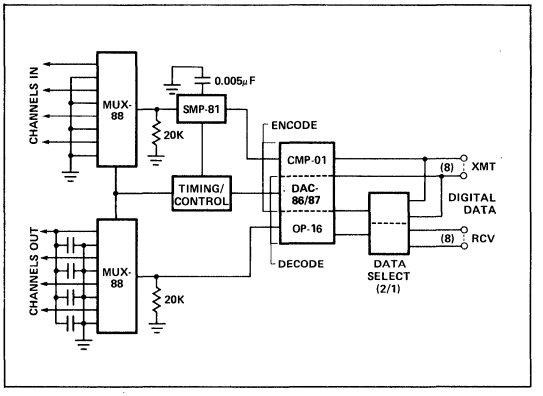


Figure 1. Four-Channel CODEC

CIRCUIT DESIGN

The analog circuitry required for a four-channel system is shown in Figure 2. The circuit uses the same printed circuit

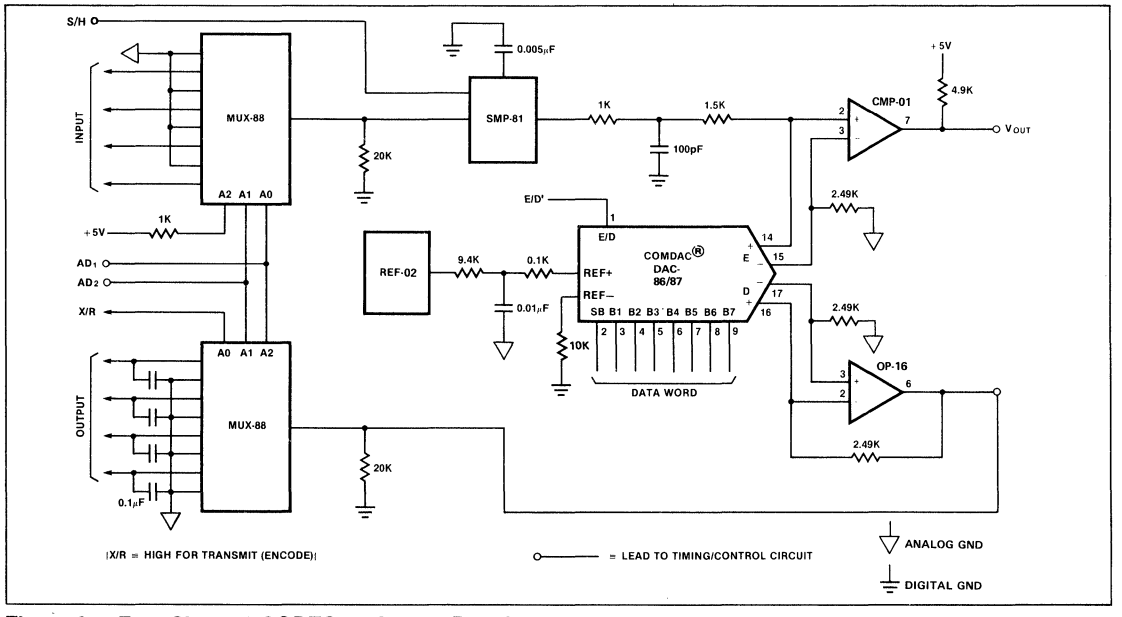


Figure 2. Four-Channel CODEC — Analog Board

*COMDAC® is a registered trademark of Precision Monolithics, Inc.

card as the transmit or receive sections of the eight-channel CODEC demonstrator (with the addition of a second multiplexer). The analog inputs all connect at the input multiplexer (MUX-88) using alternating inputs, the output (drain) of the MUX drives the SMP-81 sample-and-hold device. Once the input level is held, the COMDAC® (DAC-86 or 87), in conjunction with the comparator (CMP-01), begins the analog-to-digital conversion sequence. A successive approximation encode procedure is used; this generates, within the allotted conversion time (15.6μs), an eight-bit digital approximation of the analog level. The data byte is available at the successive approximation register output for the next 15.6μs time frame. During this time the CODEC decodes the incoming digital signals.

The decode cycle begins as soon as the encode cycle is completed. The DAC-86 is switched to the decode mode and an eight-bit data word is presented at its input leads, presumably from some distant analog-to digital converter through a switching matrix. As the DAC-86 is switched to decode, the operational amplifier (OP-16) converts the out put current of the DAC-86 into the appropriate voltage level. The output multiplexer is switched to the proper analog port as the decode procedure is initiated. On the output leads of the "de"-multiplexer, a hold capacitor is used to provide an output holding function. The "staircase" waveform is then available for filtering and the final subcriber interface.

As shown in the Figure 2, several circuit precautions were taken to reduce the internal noise levels. Foremost among these is the ample use of grounding throughout the analog circuit. All power supply inputs to the ICs are bypassed with capacitance (0.1μF) to ground. In addition, any spare land area of the board is filled with ground paths. The various voltage return paths are kept separate except for one common location on the board at the supply input leads. For further noise protection, a 20kΩ resistor to ground is connected to the drain leads (the common output or input) of both multiplexers. This reduces the multiplexer output noise and any crosstalk voltage feedthroughs. Also, in terms of the multiplexers, the output MUX is addressed to a grounded terminal (source connection) in between the active channels. This aids in minimizing the mutiplexer injection phenomena (discussed in detail in Application Note 37, describing the eight-channel CODEC design) and helps to further reduce the device crosstalk. The significance of using two multiplexers in this design is to allow unused channels of the output MUX to be connected to ground. The active channels are then alternated, in terms of addressing, with the grounded terminals. Addressing the multiplexers requires only two of the address leads to be controlled by a binary counter for data selection. The third address input is either held active (as in the input MUX), or can follow the system transmit and receive control signal (lead X/R, as in the output MUX). The address sequence for the input MUX is repeated through ports 4 to 7 (100 to 111), the most significant bit is held high and the two lower bits are counter outputs. This scheme allows maximum settling time for the MUX since the next channel to be encoded is selected more than 16μsecprior to the conversion. For the output MUX, the two **most** significant bits of the address are the counter output leads, the least significant bit is the transmit/receive lead (X/R). As is shown in Figure 3, the address sequence

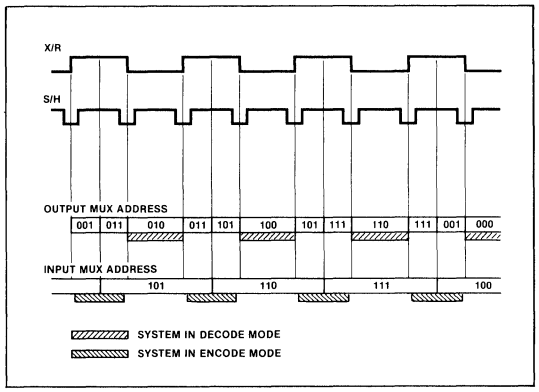


Figure 3. Four-Channel CODEC — Multiplexer Sequencing

alternates from active output port (even addresses) to grounded ports (odd addresses). The counter is changed while the MUX is selecting an unused (grounded) channel. This type of sequencing reduces the interchannel interference of the MUX and greatly adds to the system's measured performance.

To minimize sample-and-hold noise, a simple filter circuit is added to the output terminal of the device. A similar approach was used in the eight-channel design. Another feature in common with the eight-channel system is the use of a 4.9kΩ resistor pull-up from +5V to the output of the comparator; this decreases the switching time of the device for the encode procedure.

The timing waveforms generated for the four-channel system are based on the encoder clock used in the eight-channel CODEC. This clock circuit is shown in Figure 4. In a companded A/D conversion, using a successive approximation method, different digital bits require different settling times. There is a constant increase in the settling time required as one goes from the sign bit to the chord bits and then to the step bits. This increase in settling time is partially caused by the scaled current sources used to design a companding D/A and is most affected by the magnitude of the voltage level being converted. So that, as, the output currents of the DAC-86 become smaller (at smaller voltage levels), the comparator is less responsive. As the less significant bits are clocked in, the situation becomes more critical since progressively smaller current changes are provided to drive the comparator. A multi-frequency clock will take advantage of these timing variations; such a clocking scheme is shown in Figure 5. The governing design criteria is that a limited amount of time is available to complete the successive approximation of the analog signal and the optimum clock must fit within this period. All functions (including sampling, encoding, switching) must be completed, therefore, with an acceptable accuracy, within this time constraint. To achieve accurate data acquisition with the sample-and-hold, a sample pulse of 3.2μs was used. Once the pulse goes from sample to hold, there is a waiting time required to allow the sample-and-hold output to settle to the "held" value; 650ns is the time added. Since the sign bit is

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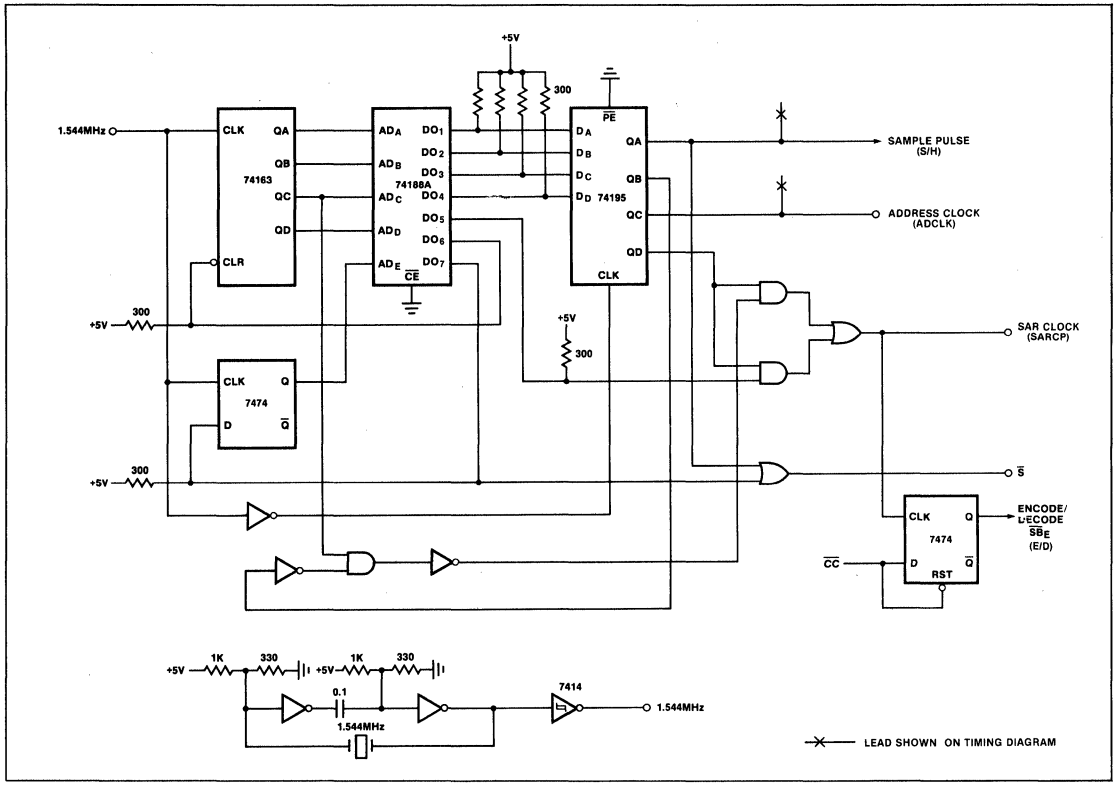


Figure 4. PROM Based System Clock

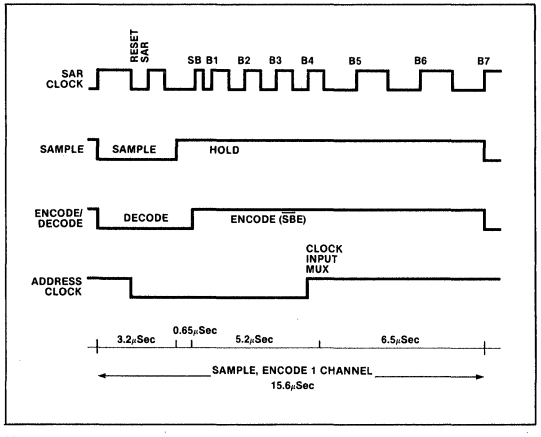


Figure 5. Four-Channel CODEC — Encoder Timing

the fastest transition, the basic system clock (1.544MHz) is used for the first SAR clock period. The clock frequency is then halved to clock in the chord bits (B1, B2, B3), the next "slowest" transitions. Finally, the clock frequency is halved again to allow for the step bits (B4-B7), a frequency of 386KHz. The SAR is reset during the sampling period and once the sample circuit has entered the hold mode, the input multiplexer's address is changed. This provides ample time for the MUX to switch to the next analog input with little effect on the adjacent waveforms.

Using this timing pattern as the starting point, the original eight-channel system was converted to a four-channel bidirectional design. The only additional control functions to be added were the timing signals needed to switch the DAC-86 between the encoding and decoding modes, to operate the output multiplexer, and to select the proper data inputs for the DAC-86. The DAC-86 mode select and the multiplexer address leads, as mentioned previously, are generated from a single system transmit/receive control (shown as X/R in Figure 6). The lead is the system monitor of the mode in which the CODEC is operating. When active (logic "1"), the DAC-86 and associated parts are in the encode mode. In the encode mode: the successive approximation register clock is enabled, the encode/decode lead to the DAC-86 (E/D) is enabled, the data input selector directs the SAR output back toward the DAC-86 for the feedback needed in successive approximation, and the output MUX connects the OP-16 to a grounded (unused) channel. The X/R lead remains at logic "1" until encoding is completed, then goes to ground (logic "0"), the decode state. To decode a

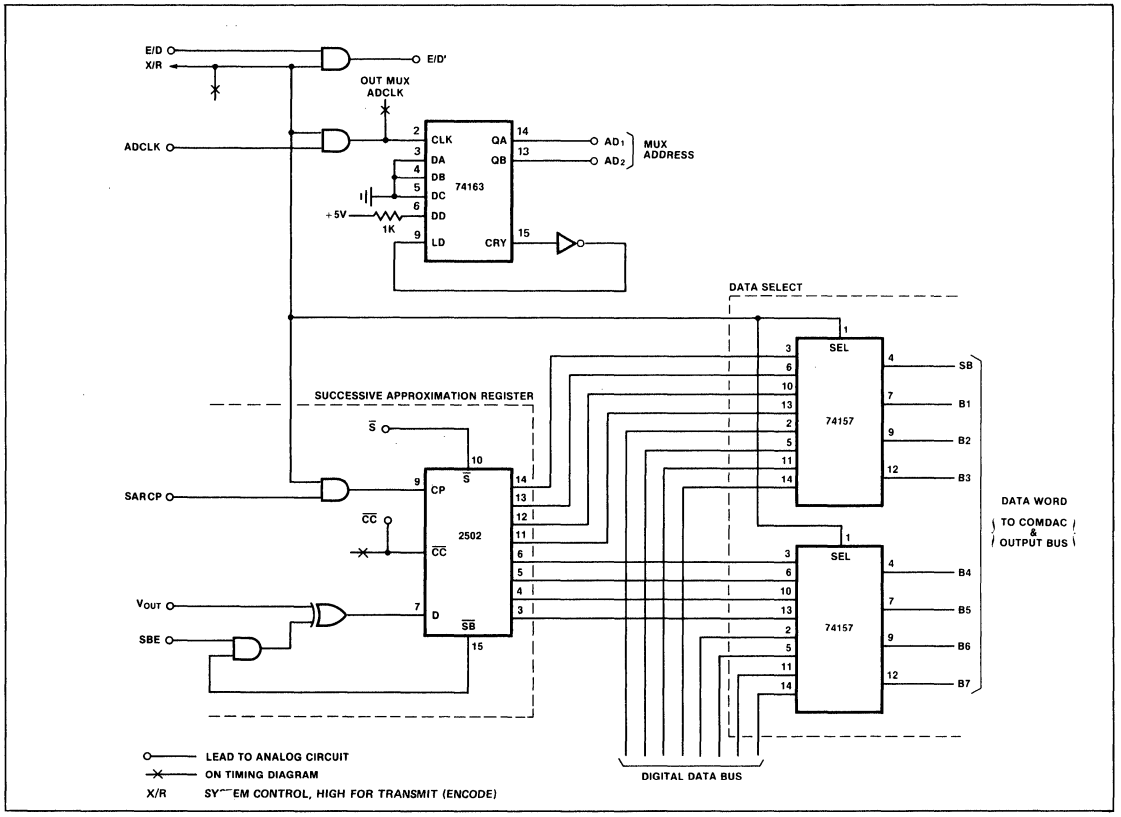


Figure 6. Four-Channel CODEC — Control Board

data byte, the DAC-86 is held in the decode mode (E/D is low), the output MUX is addressed to an active output port, and the SAR clock is disabled (this register will hold the last encoded data word throughout the decode cycle — it is not cleared until a new input signal is to be encoded). The data selector is directed to the digital system bus and the decoding of the byte on the bus begins. As described, the address leads of the multiplexers are programmed such that the input MUX will always be directed toward the next active channel, once the previous analog sample has been held. But the output MUX does not connect to an active channel until the decode cycle begins; during the encode cycle only unused (grounded) ports are addressed.

SYSTEM TESTS

The system as configured in the block diagram (Figure 7) is a complete four-channel CODEC. To perform the transmission tests, it was decided to use a single CODEC circuit and transmit data in a "loopback" configuration. As was mentioned earlier, the only signal required from an external controller is the X/R lead. This is generated for the test circuit by halving the inverted ADCLK lead from the prom-based clock. The system waveforms that result are shown in Figure 8. These clock patterns can be correlated to the encode clock waveforms in Figure 5 by comparing the ADCLK or the S/H leads. Since the successive approximation register is not cleared until after the decode cycle, an external register is not necessary to hold the data for the decoding process.

The transmission tests that were completed were the typical telephone network tests as described in the eight-

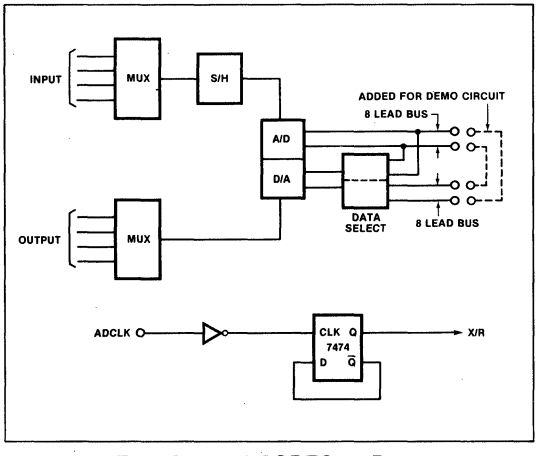


Figure 7. Four-Channel CODEC — Demonstrator Layout

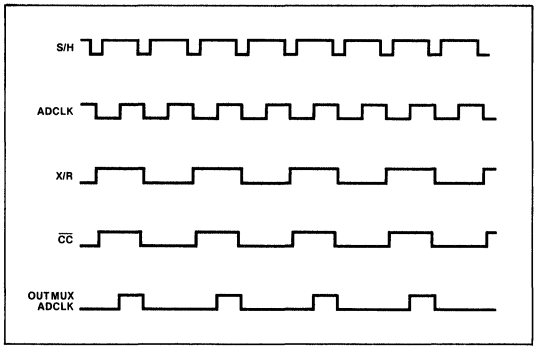


Figure 8. Four-Channel CODEC — Demonstrator Timing

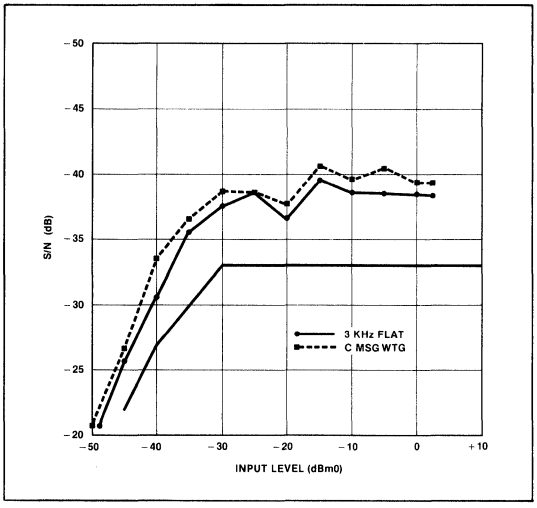


Figure 9. Signal-To-Total Distortion (Four-Channel)

channel application information. The tests include signal-to-total distortion, gain tracking, intelligible crosstalk and idle channel noise. Again the test method used for the first two tests was based on a sinusoidal input signal, as is common in the AT&T specifications, at a frequency between 400 and 3400Hz using a frequency-selective wave analyser. The results of all testing are shown in Figures 9 through 11.

It is of some interest to compare this data with the test results of the eight-channel CODEC design. In particular, the idle channel noise and the crosstalk measurements are improved. This can be partially explained by the different manipulations of the output multiplexer. This does however, tend to point to the fact that the output MUX can be a significant source of noise and cross channel interference. Further data is certainly necessary, but these results do point out an area of concentration for the system designer wanting to improve system performance.

In terms of signal-to-total distortion and gain tracking, the four-channel results compare favorably with the eight-

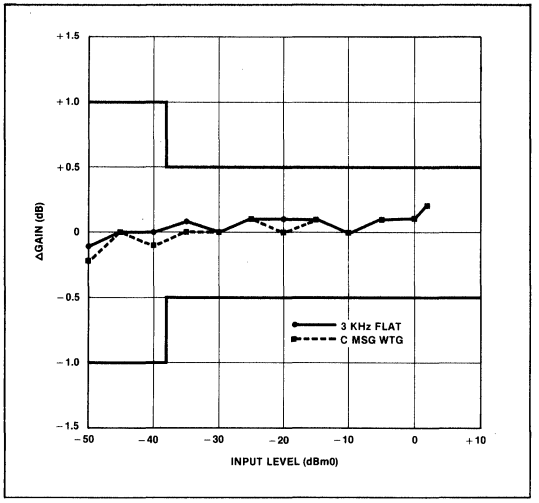


Figure 10. Gain Deviation (Four-Channel)

IDLE CHANNEL NOISE

Channel	
1	
2	no channel
3	had noise
4	level > 2dBrnc

INTELLIGIBLE CROSSTALK

f_{input}	Level
400-3400Hz	≤ −85dBmO

Figure 11. Transmission Measurements (Four-Channel)

channel data and both systems exceed the AT&T requirements. Overall, the transmission tests point out that using a single DAC-86 for four-channel transmitting and receiving is a realistic approach and can comply with all "system" standards.

CONCLUSIONS

The testing described in the preceeding pages demonstrates the feasibility of encoding and decoding four channels with a single DAC-86. The system has several advantages: 1) a smaller number of devices are required to complete the CODEC function than were necessary for the eight-channel design, 2) the clock circuitry (prom-based timing generator) is common to all encoders, so only a single such circuit is needed for multiple CODECs. Both of these factors contribute to reduced printed circuit board area for multiple transmission channels. The devices needed for a four-channel CODEC are listed in Figure 12. In terms of package sizes only one device is larger than sixteen pins (the DAC 86/87 is 18 pins) and three of the components are only eight pins. This should make system layout fairly simple and allow relatively dense component packing. If channel monitoring is incorporated, then a single supervision circuit could administer several circuit packs in a system line-

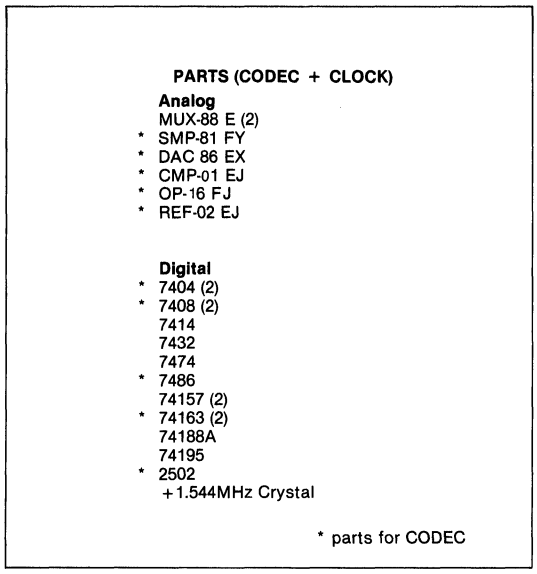


Figure 12. Four-Channel CODEC — Parts

up. The number of external leads is reduced in a four-channel CODEC and the design is easily added to a bus-structure data switching system.

The price per channel is still less than that being quoted by single-channel CODEC designers although slightly more than the eight-channel approach. (See pricing, Figure 13). The sacrifice made in price-per-channel is offset by the gains in system architecture and board layout offered by a four-channel shared CODEC. The shared channel CODEC approach is a viable solution to producing a digital transmission system. AN-37 shows designs at even lower per channel cost.

	ENCODE/DECODE	CLOCK
Digital	$ 3.82	$ 4.12
PMI	$19.90	
Total	$23.72	$ 4.12
per channel	$ 5.93	$ 1.03 ($0.17, when using clock for 24 channels)

NOTE: Pricing Based on 100,000 Parts

Figure 13. Four-Channel CODEC — Costs

APPLICATION NOTE 39

COMPANDING DIGITAL-TO-ANALOG CONVERTER

by Guido Pastorino

(FROM PMI DESIGN REVIEW NOTES – 1975)

INTRODUCTION

A companding digital-to-analog converter (DAC) is the key component in PCM CODEC systems. (CODEC is an acronym for coder-decoder.) A CODEC performs the coding functions which consist of an analog-to-digital conversion (ADC) of the input analog (voice) signal and decoding, which consists of a digital-to-analog conversion (DAC) of the received digital input.

The DAC is used for both encoding and decoding; it is in a feedback loop to generate the ADC functions. Voice signals in telephony require a system with a very large dynamic range. The dynamic range (DR) of a CODEC is defined as the ratio of the largest resolvable signal to the smallest signal which can be encoded. The dynamic range of the CODEC is the same as that of the DAC used in either the decode mode or in the feedback loop of the successive approximation type ADC. The dynamic range of a DAC is simply the ratio of its output for a linear input of one least significant bit (LSB) to that of the largest, all "1s," input. This ratio is usually expressed in decibels using the equation:

$$DR = 20 \log_{10} \frac{I_{MAX.}}{I_{LSB}}$$

where for a current output DAC I_{MAX} is the output current for all "1s" input and I_{LSB} is the output current for one LSB input. Using this equation a linear bit DAC can be shown to resolve a ratio of 2^n:1 therefore:

$$DR = 20\log_{10} \frac{2^n}{1} \approx 6^n$$

The wide dynamic range requirements of a telephone system require the equivalent dynamic range of a 12-bit system or 72dB. However, this system would not be satisfactory for telephone voice transmission because of its excessive bandwidth requirements. With present day T1 type transmission systems a 64kbits/sec data rate is required to transmit each voice channel. The use of the linear system would increase this bit rate to 96kbits/sec. This would provide more accuracy than is needed at the expense of excessive bandwidth.

For voice systems the most important criterion is the signal-to-noise ratio. In a PCM system noise is due almost entirely to quantizing distortion. Thus, a non-linear DAC has a non-linear transfer characteristic to compress the analog signal into a digital word and a complementary transfer characteristic to expand the digital words into analog signals with a wide dynamic range. For a telephone system a CODEC requires a fairly uniform signal-to-distortion ratio over its entire dynamic range. Achieving this uniform signal-to-distortion ratio over a wide dynamic range requires the use of non-uniform coding. A non-uniform CODEC is a coder-decoder pair whose input amplitude range is divided into steps of unequal widths, such that the width of the quantizing steps increase in proportion to the amplitude of the signal. To achieve uniform signal to distortion performance a logarithmic transfer function is required. The word compand, (compand is an acronym for compress — expand) was borrowed from analog systems to describe this non-uniform coding system where quantizing and coding is such that step size depends on the input amplitude.

COMPANDING PRINCIPLES

Companding requirements differ for different signal distributions. As mentioned above, voice signals require constant S/D performance over a wide dynamic range. In order to accomplish this the distortion must be proportional to the signal level. This feat is best achieved by the use of a logarithmic compression law. However, a truly logarithmic assignment of code words is not physically possible since this implies an infinite number of codes. Two methods for generating practical implementations of logarithmic transfer functions have been derived which have become industry standards. These methods are generally known by their transfer functions which are called μ-law and A-law respectively. Both of these transfer functions are normally implemented with eight-bit non-linear DACs to achieve a 72dB dynamic range. This is the equivalent dynamic range of a twelve-bit linear DAC. The μ-law and the A-law transfer functions are described by the following equations:

$$\mu\text{-law} \quad Y = \frac{1n\,(1+\mu|X|)}{1n\,(1+\mu)} \quad \text{sgn } X \quad \text{for } -1 \le X \le +1$$

$$\text{A-law} \quad Y = \frac{1+1nA|X|}{1+1nA} \quad \text{sgn } X \quad \text{for } 1/A \le X \le 1$$

$$Y = \frac{A|X|}{1+1n\,A} \quad \text{sgn } X \quad \text{for } 0 \le X \le 1/A$$

These laws have unique signal-to-distortion characteristics for each value of μ and A respectively. At present ATT has settled on a value of μ equal to 255 and CCITT specifications use a value of A equal to 87.6. Substituting these constants into the original equation above obtain:

$$\mu\text{-law} \quad Y = 0.18\ 1n\,(1+\mu|X|) \quad \text{sgn } X \text{ for } -1 \le X \le 1$$

$$\text{A-law} \quad Y = 0.18\ 1n\,(1+1n|X|) \quad \text{sgn } X \text{ for } 1/A \le |X| \le 1$$

$$Y = 0.18\ A|X| \quad \text{sgn } X \text{ for } 0 \le |X| = 1/A$$

The wideband (unfiltered) signal-to-distortion ratio over the useable dynamic range of voice transmissions is shown in Figure 1. This plot does not represent actual system performance; it is instead, a measure of the distortion which would be caused by an ideal quantizer.

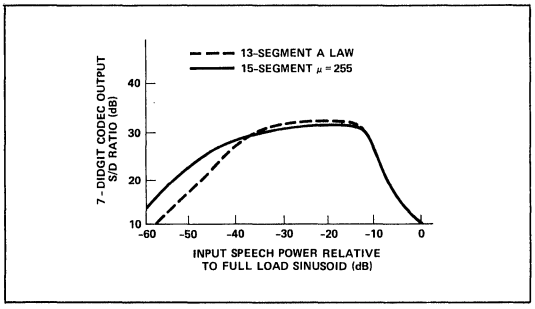


Figure 1. Input Speech Power Relative to Full Load Sinusoid (dB)

The practical implementation of the two transfer functions is accomplished by standardized piece-wise linear approximations. The transfer functions are implemented in chords or segments where the transfer function within any one chord is a linear staircase. Each chord has sixteen steps and the size of the step in each succeeding chord is double the size of the step in the preceeding chord. There are normally eight chords numbered zero through seven in both μ-law and A-law characteristics. For the A-law function the first two chords on either side of the origin have equal step sizes, whereas, for the μ-law function, the second chord after the origin has a step size which is double that of the first. For all remaining chords the steps double in size for each succeeding chord. This applies to both the μ-law and A-law functions. For the A-law function the four chords about the origin can be considered as a single segment so that the A-law characteristic is sometimes referred to as being a "13-segment" code. The A-law characteristic also differs from the μ-law characteristic in the manner in which the transfer function crosses the origin. The X-axis origin for the μ-law is at "mid-step" while the X-axis origin for the A-law is coincident with a "riser". This can be understood better from the "blow-ups" about the origin of Figures 2 and 3.

In order to obtain the best implementations of the transfer function, companded DACs are constructed such that encode and decode functions are offset by one-half step. With this technique the quantizing band for the encode DAC will be centered about the decode value. This can be seen in Figure 4, where the μ-law characteristics about the origin are shown. (The A-law characteristics would be identical except for the "mid-riser" phenomena at the origin.) As an example suppose that, for Figure 4, an analog input whose amplitude lies between levels 2 and 4 is being encoded. The best quantizing code to assign to this entire quantizing band is its mean value of 3. Thus the DAC used in the suc-

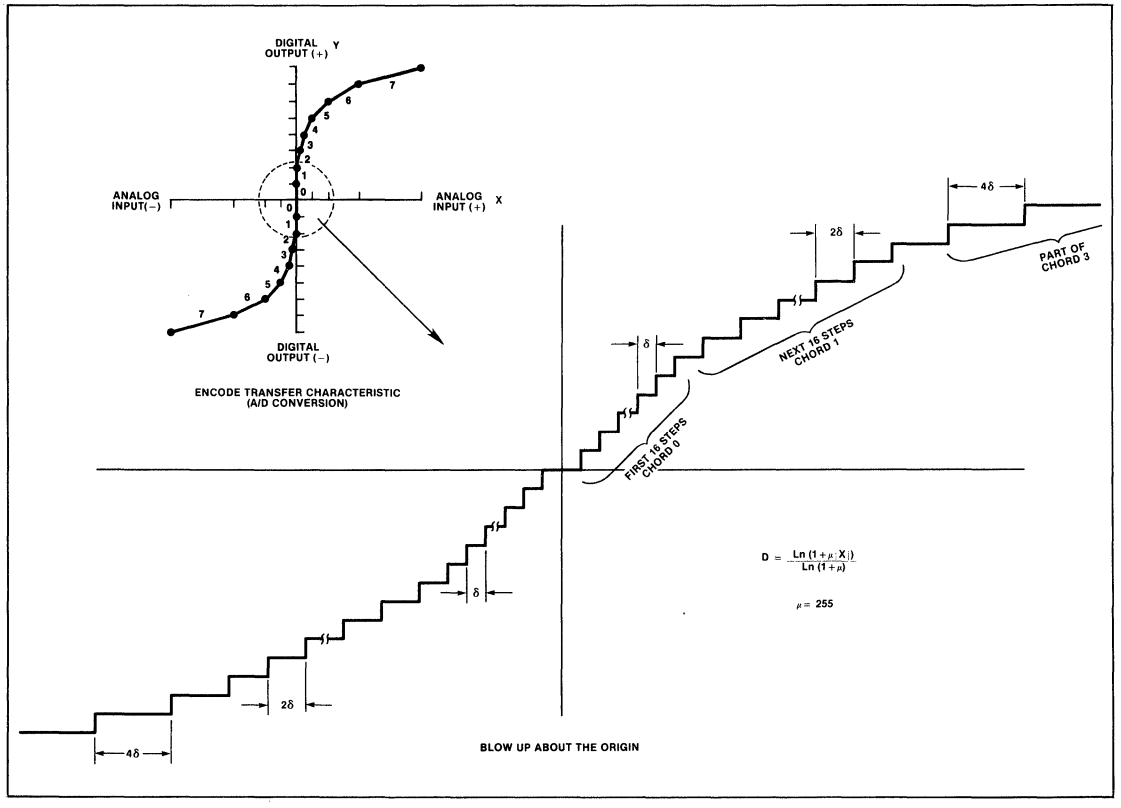


Figure 2. μ-Law Transfer Function

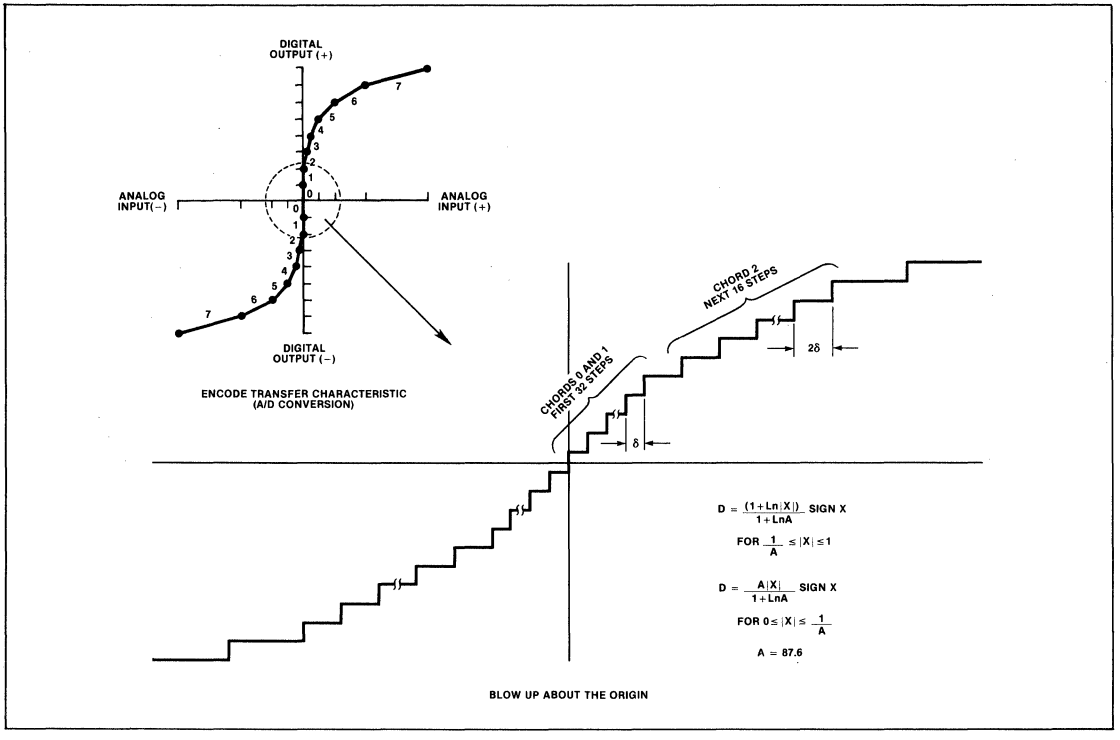


Figure 3. A-Law Transfer Function

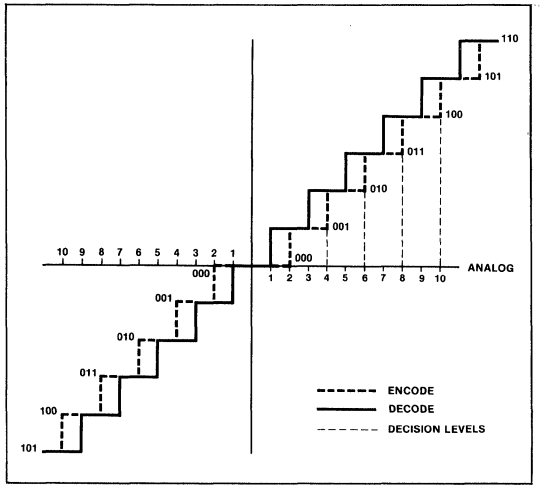


Figure 4. μ-Law Encode/Decode Characteristics About the Origin

cessive approximation feedback loop of the encode has output levels which represent the quantizing band edges. These can be referred to as decision levels. On the other hand the DAC for the decoder has output levels which represent the mean values of the quantizing bands which must, of necessity, be centered about the decoder output values. The end result is that a DAC used for decoding must be offset one-half step from the DAC used for encoding. This situation must exist over the entire range of the CODEC. A transmission system implemented with companding DACs is shown in Figure 5.

COMDAC® SYSTEM DESCRIPTION

A block diagram of PMI's companding DAC is shown in Figure 6. A single current output DAC is used to generate outputs for either the encode or decode mode of operation.

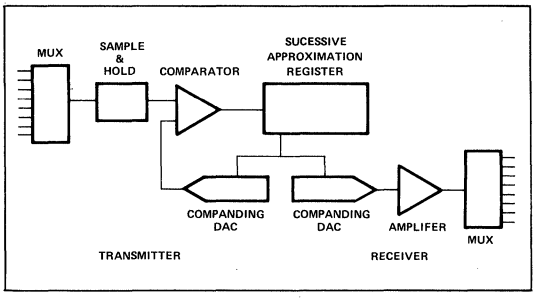


Figure 5. Transmission System Implemented with Companding DAC

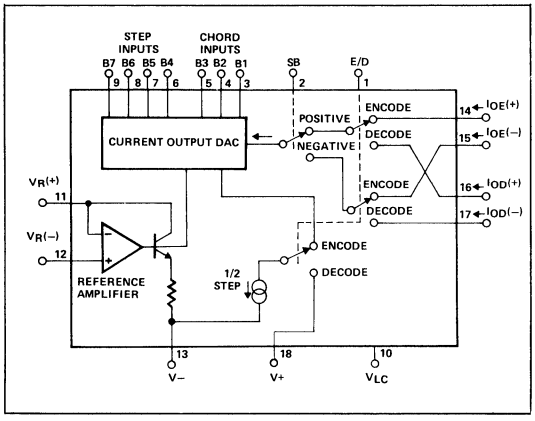


Figure 6. Equivalent Circuit and Pin Connection Diagram

Each companding DAC can be programmed to operate as either an encoder or a decoder by properly programming the E/D pin. The encode mode is offset one-half step from the decode mode by means of the current generator which is switched in during the encode mode. The reference amplifier establishes the current reference for the current output DAC. The sign bit pin (SB) controls the positive-negative switch which directs the output of the current output DAC.

This output will eventually end up at the positive (I_{OE+} or I_{OD+}) outputs or the negative (I_{OE-} or I_{OD-}) outputs depending on whether the SB pin is programmed to a binary "1" or a binary "0". The encode-decode switch E/D determines whether the DAC output shall be directed to the encode or decode terminations as shown in Figure 6. In addition, this same switch introduces the one-half step of offset current required during encode.

A better understanding of the COMDAC® circuitry is obtained by reviewing the previously discussed piece-wise linear approximation of the companding DAC transfer function to the desired μ-law or A-law transfer functions. Each chord or segment consists of 16 steps numbered from 0 to 15. The size of the steps double in size from one chord to the next as the number of the chord increases. The chords are numbered 0 to 7. In order to smooth out the characteristics during the transition from one chord to the next, the step current for step 0 of each chord is 1-1/2 times larger than the current of the highest step of the chord immediately preceding it. The succeeding 15 steps (steps 1 to 15) are then two times the size of the steps of this previous chord. These characteristics can be examined in Figure 7.

To implement the transfer function, the first chord (N = 0) uses 16 equal steps each of whose size, I_0 is 1/16 of chord current source I_{C0} for A-law, or 1/16.5 of current source I_{C0}

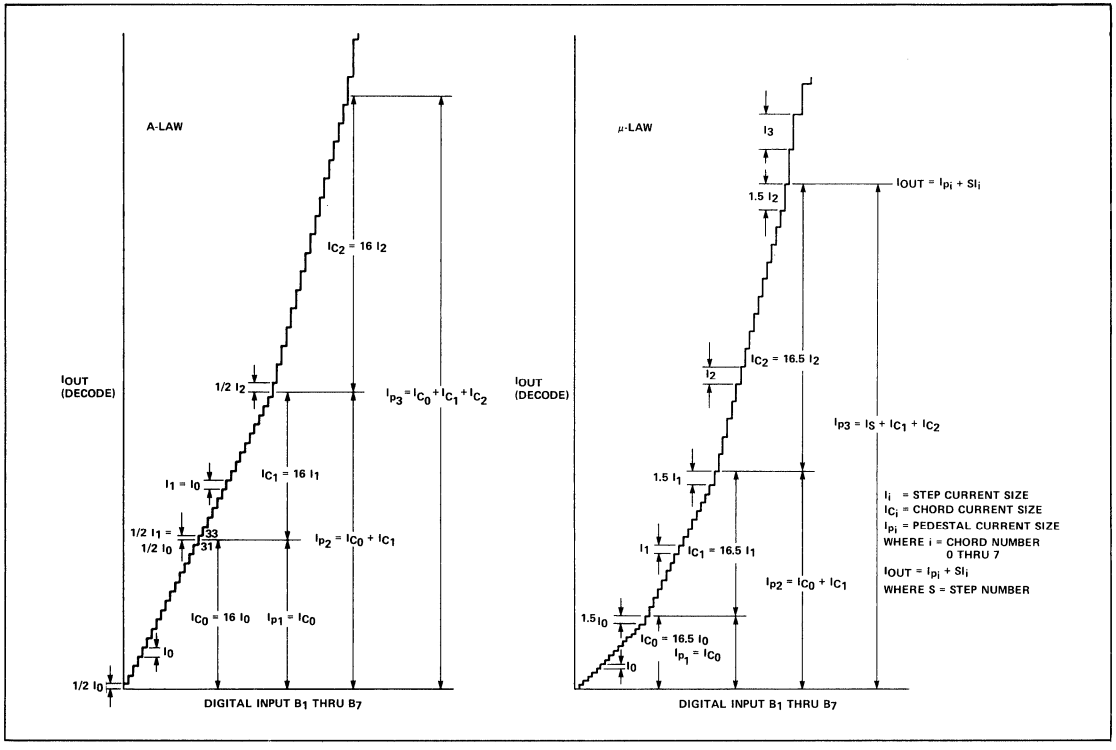


Figure 7. Construction of the Companding DAC Transfer Function

for μ-law. The next chord, N = 1, must begin at $I_{C0} + 1.5I_0$ for both A-law or μ-law. Another way of saying this is that chord N = 1 begins 16.5 steps from the origin. In order to accomplish this a pedestal current must be directed toward the output whose magnitude is equal to $I_{C0} + 1.5I_0$. Chord C2 begins at $I_{C0} + 1.5I_0 + I_{C1} + 1.5I_1$ and ends at $I_{C0} + 1.5I_0 + I_{C1} + 1.5I_1 + I_{C2} + 1.5I_2$ and so forth. This process continues with pedestal currents for each chord number N described by the equation:

$$I_{PN} = \sum_{i=0}^{N-1} (I_{Ci} + 1.5I_i) = 16.5 \sum_{i=0}^{N-1} I_i$$

note that $I_{PO} = 0$.

A functional diagram of a companding DAC which implements the proper transfer function discussed above is shown in Figure 8, which operates in the following manner: the reference amplifier sets the bias current for the chord generator by means of I_{C7} which is a current mirror whose output is equal to $2I_{REF}$. Next, due to the operation of an R–2R ladder which is described in a following paragraph, I_{C6} is made equal to one-half I_{C7} and is therefore equal to I_{REF}. I_{C5} is made equal to one-half I_{C6} and so forth. From I_{C3} down to I_{C0} a slave ladder is used rather than an R–2R ladder but the results are the same. The chord currents double in size progressing from I_{C0} to I_{C7} respectively (for A-law however $I_{C1} = I_{C0}$). The chord selector is programmed from the 1 of 8 decoder so that the chord identified by binary chord number N on leads B_1 to B_3 will switch I_{CN} to the step generator. All other chord currents are switched to the pedestal selector. The pedestal selector is programmed from the same 1 of 8 chord decoder such that chords I_0 to I_{N-1} are switched to the pedestal selector output in order to generate pedestal current I_{PN}. All other chord currents are switched to ground so that a pedestal current equal to the sum of the chord currents from I_{C0} to $I_{C(N-1)}$ will be directed to the output current switch matrix as I_{PN}. The I_{CN} flowing into the chord selector from the step generator is equal to 16.5 step currents (16.0 steps for A-law) where a step current is equal to the current step caused by changing the least significant bit in the chord of interest. Note that this satisfies the requirement of the equation for pedestal current I_{PN}. The step generator has the ability to sum current I_E into the output mode to provide the one-half step offset required when the system is operating in the encode mode. This one-half step offset current is controlled by the E/D pin. The system is in the encode mode when the E/D pin is biased to a binary "1".

DETAILED CIRCUIT DESCRIPTION

All of the single pole double throw switches in Figure 8 are constructed of bipolar emitter coupled transistors. One such switch is shown as an example in Figure 9. When the

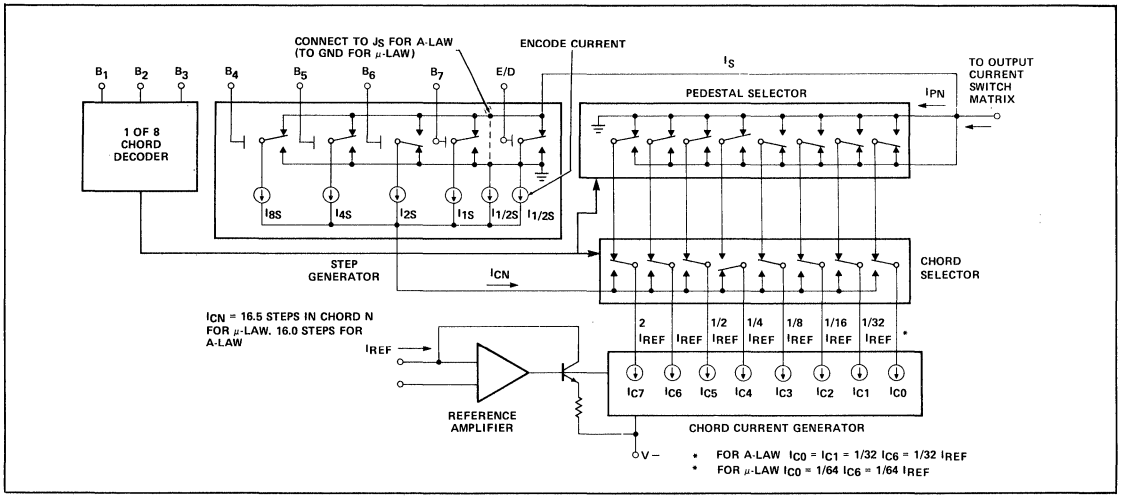


Figure 8. COMDAC® Companding DAC Functional Diagram

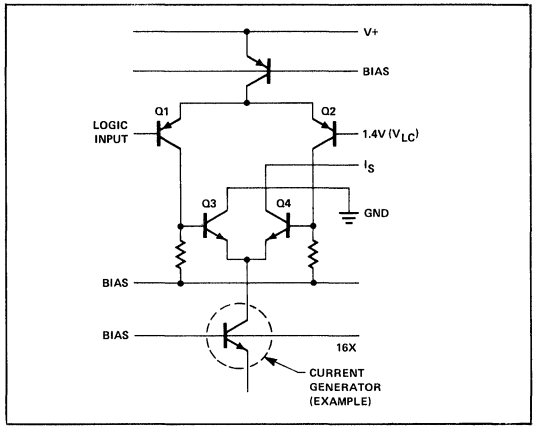


Figure 9. Double Pole Double Throw Switch Implemented with Emitter Coupled Transistors

logic input exceeds the logic level bias V_{LC} Q_1 is turned off and Q_2 is turned on. In turn Q_3 is turned off and Q_4 is turned on thus effectively switching the current generator, shown as an example, from the ground to I_S. Conversely, lowering the logic level input below V_{LC} will switch the current from I_S to ground. The V_{LC} Control permits the circuit to interface with a large range of logic levels.

The chord current generator circuit is shown in Figure 10. This circuit is the implementation of the chord current generator previously discussed. Q_0 is forced to operate at the reference input current I_{REF} and Q_1, with an emitter resistor one-half the size of the emitter resistor of Q_0, will then operate at $2I_{REF}$. Q_2 through Q_4 will operate at progressively smaller currents where each transistor operates at one-half the current of the transistor to its immediate left. To review this normal R−2R current-ladder function notice that Q_{4A} and Q_{4B} operate at equal currents and that the sum of their currents is equal to that of one transistor with an emitter resistor equal to R. When the series resistor R is added to the junction of the emitter resistors of Q_{4A} and Q_{4B} the current of Q_3 will be forced to equal the sum of the Q_{4A} and Q_{4B} currents. Thus Q_{4A} current equals one-half the Q_3 current. Now the current from Q_{4A}, Q_{4B} and Q_3 must all flow through the next series resistor R. This current is equal to twice that of Q_3; therefore it is easy to compute that the Q_2 current is twice that of the Q_3. The same reasoning may be used to proceed down the ladder to show that each transistor in the ladder sinks twice the current of the transistor on its immediate right. The slave ladder consisting of Q_5 through Q_{8A} and Q_{8B} continues to halve currents for each transistor proceeding to the right. However this part of the chord current generator uses scaled resistors instead of the R−2R ladder technique. Since Q_{4B} sinks constant current from the slave ladder, and since all the current must flow through the scaled emitter resistors, then the curent through each transistor must be inversely proportional to the size of its emitter resistor. By examination of the slave ladder it can be seen that each transistor proceeding to the right sinks one-half the current of the transistor to its immediate left. For the μ-law chord current generator Q_{8B} is simply diode connected such that the chord current for chord C_0 is roughly one-half the current of chord C_1. For the A-law chord current generator, however, the collectors of transistors Q_{8A} and Q_{8B} are tied together so that I_{C0} is exactly equal to I_{C1}. The currents flow to the chord current generator from an array of bipolar single pole double throw switches labeled "chord selector" in Figure 8. The actual switches are not shown in this paper.

The Step Current Generator is shown in Figure 11. Again the single pole double throw switches which connect the step generator to the output current matrix as shown in the companding DAC functional diagram are not represented. The step generator is connected to the chord selector which sinks I_{CN}. Ratioed emitters are used to divide the current. The largest emitter is 16 times the size of the smallest emitter and therefore sinks 16 times the current. The A-law step generator differs from the μ-law step generator in that each chord begins with a riser instead of a step. This also applies to the origin, therefore one-half step of current flows (decode mode) even when the binary input to the step generator is "0". Step switches controlled directly by the binary code connect the appropriate collectors of the step current generator transistors to the output current matrix. For both A-law and μ-law devices I_{CN} is one of the pedestal currents. The difference is that for the A-law device the pedestal current is equal to 16 steps whereas, for the μ-law, the pedestal current is equal to 16.5 steps.

NORMALIZED COMPANDING DAC OUTPUTS

It is convenient to generate tables of normalized values which correspond exactly to the CCITT (Consultive Committee for International Telephone and Telegraph) specifications. The following tables are normalized to the smallest DAC output which is equivalent to one-half step.

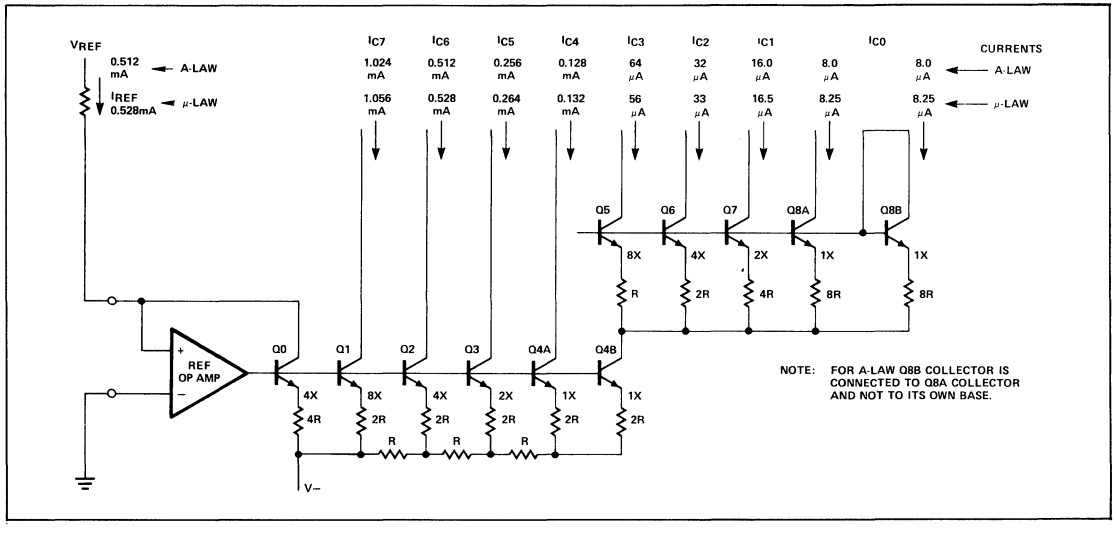


Figure 10. Chord Current Generator Diagram

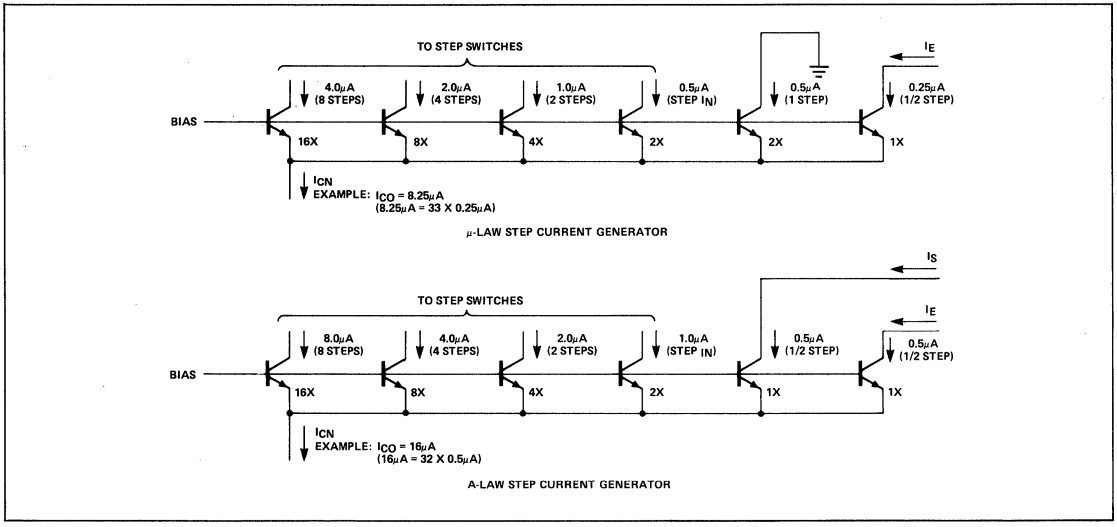


Figure 11. A-Law and μ-Law Step Current Generators

μ-Law Normalized Table

NORMALIZED DECODE OUTPUT (SIGN BIT EXCLUDED) $I_{C,S} = 2[2^C (S + 16.5) - 16.5]$

C = chord no. (0 through 7)
S = step no. (0 through 15)

STEP \ CHORD		0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0	33	99	231	495	1023	2079	4191
1	0001	2	37	107	247	527	1087	2207	4447
2	0010	4	41	115	263	559	1151	2335	4703
3	0011	6	45	123	279	591	1215	2463	4959
4	0100	8	49	131	295	623	1279	2591	5215
5	0101	10	53	139	311	655	1343	2719	5471
6	0110	12	57	147	327	687	1407	2847	5727
7	0111	14	61	155	343	719	1471	2975	5983
8	1000	16	65	163	359	751	1535	3103	6239
9	1001	18	69	171	375	783	1599	3231	6495
10	1010	20	73	179	391	815	1663	3359	6751
11	1011	22	77	187	407	847	1727	3487	7007
12	1100	24	81	195	423	879	1791	3615	7263
13	1101	26	85	203	439	911	1855	3743	7519
14	1110	28	89	211	455	943	1919	3871	7775
15	1111	30	93	219	471	975	1983	3999	8031
STEP SIZE		2	4	8	16	32	64	128	256

μ-Law Normalized Tables

NORMALIZED ENCODE LEVEL (SIGN BIT EXCLUDED) $I_{C,S} = 2[2^C (S + 17) - 16.5]$

C = chord no. (0 through 7)
S = step no. (0 through 15)

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	1	35	103	239	511	1055	2143	4319
1	0001	3	39	111	255	543	1119	2271	4575
2	0010	5	43	119	271	575	1183	2399	4831
3	0011	7	47	127	287	607	1247	2527	5087
4	0100	9	51	135	303	639	1311	2655	5343
5	0101	11	55	143	319	671	1375	2783	5599
6	0110	13	59	151	335	703	1439	2911	5855
7	0111	15	63	159	351	735	1503	3039	6111
8	1000	17	67	167	367	767	1567	3167	6367
9	1001	19	71	175	383	799	1631	3295	6623
10	1010	21	75	183	399	831	1695	3423	6879
11	1011	23	79	191	415	863	1759	3551	7135
12	1100	25	83	199	431	895	1823	3679	7391
13	1101	27	87	207	447	927	1887	3807	7647
14	1110	29	91	215	463	959	1951	3935	7903
15	1111	31	95	223	479	991	2015	4063	8159
STEP SIZE		2	4	8	16	32	64	128	256

A-Law Normalized Tables

NORMALIZED DECODE OUTPUT (SIGN BIT EXCLUDED)

$I_{CS} = 2^{N-1} (33 + 2S)$ For $N > 0$
$I_{CS} = 2S + 1$ For $N = 0$

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	1	33	66	132	264	528	1056	2112
1	0001	3	35	70	140	280	560	1120	2240
2	0010	5	37	74	148	296	592	1184	2368
3	0011	7	39	78	156	312	624	1248	2496
4	0100	9	41	82	164	328	656	1312	2624
5	0101	11	43	86	172	344	688	1376	2752
6	0110	13	45	90	180	360	720	1440	2880
7	0111	15	47	94	188	376	752	1504	3008
8	1000	17	49	98	196	392	784	1568	3136
9	1001	19	51	102	204	408	816	1632	3264
10	1010	21	53	106	212	424	848	1696	3392
11	1011	23	55	110	220	440	880	1760	3520
12	1100	25	57	114	228	456	912	1824	3648
13	1101	27	59	118	236	472	944	1888	3776
14	1110	29	61	122	244	488	976	1952	3904
15	1111	31	63	126	252	504	1008	2016	4032
STEP SIZE		2	2	4	8	16	32	64	128

A-Law Normalized Table

NORMALIZED ENCODE DECISION LEVELS (SIGN BIT EXCLUDED)

$I_{CS} = 2^{N-1}(34 + 2S)$ For $N > 0$
$I_{CS} = 2S + 2$ For $S = 0$

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	2	34	68	136	272	544	1088	2176
1	0001	4	36	72	144	288	576	1152	2304
2	0010	6	38	76	152	304	608	1216	2432
3	0011	8	40	80	160	320	640	1280	2560
4	0100	10	42	84	168	336	672	1344	2688
5	0101	12	44	88	176	352	704	1408	2816
6	0110	14	46	92	184	368	736	1472	2944
7	0111	16	48	96	192	384	768	1536	3072
8	1000	18	50	100	200	400	800	1600	3200
9	1001	20	52	104	208	416	832	1664	3328
10	1010	22	54	108	216	432	864	1728	3456
11	1011	24	56	112	224	448	896	1792	3584
12	1100	26	58	116	232	464	928	1856	3712
13	1101	28	60	120	240	480	960	1920	3840
14	1110	30	62	124	248	496	992	1984	3968
15	1111	32	64	128	256	512	1024	2048	*4096
STEP SIZE		2	2	4	8	16	32	64	128

The numbers in these tables are directly proportional to the input reference current. However the exact relationship is somewhat complicated. A reference current of 528μA for the μ-law DAC will produce a step size of 0.5μA thus, for the μ-law device driven by a reference current of 528μA, it is only necessary to multiply all the numbers in the normalized tables by one-half step or 0.25μA to obtain the output in μA. The table tabulated below corresponds to a 528μA reference.

μ-Law Current Output Table

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS (SIGN BIT EXCLUDED)

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	8.25	24.75	57.75	123.75	255.75	519.75	1047.75
1	0001	0.5	9.25	26.75	61.75	131.75	271.75	551.75	1111.75
2	0010	1	10.25	28.75	65.75	139.75	287.75	583.75	1175.75
3	0011	1.5	11.25	30.75	69.75	147.75	303.75	615.75	1239.75
4	0100	2	12.25	32.75	73.75	155.75	319.75	647.75	1303.75
5	0101	2.5	13.25	34.75	77.75	163.75	335.75	679.75	1367.75
6	0110	3	14.25	36.75	81.75	171.75	351.75	711.75	1431.75
7	0111	3.5	15.25	38.75	85.75	179.75	367.75	743.75	1495.75
8	1000	4	16.25	40.75	89.75	187.75	383.75	775.75	1559.75
9	1001	4.5	17.25	42.75	93.75	195.75	399.75	807.75	1623.75
10	1010	5	18.25	44.75	97.75	203.75	415.75	839.75	1687.75
11	1011	5.5	19.25	46.75	101.75	211.75	431.75	871.75	1751.75
12	1100	6	20.25	48.75	105.75	219.75	447.75	903.75	1815.75
13	1101	6.5	21.25	50.75	109.75	227.75	463.75	935.75	1879.75
14	1110	7	22.25	52.75	113.75	235.75	479.75	967.75	1943.75
15	1111	7.5	23.25	54.75	117.75	243.75	495.75	999.75	2007.75
STEP SIZE		.50	1	2	4	8	16	32	64

*Virtual Decision Level

A similar exercise will yield a corresponding table for the A-law part. Multiplying all the numbers in the normalized A-law table, for instance, will produce a table of currents for a reference input of 512μA. A table based on 512μA reference current will have a step size of 1.0μA and is tabulated in the μ-law current output table.

A-Law Current Output Table

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS (SIGN BIT EXCLUDED)

STEP \ CHORD		0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0.5	16.5	33	66	132	264	528	1056
1	0001	1.5	17.5	35	70	140	280	560	1120
2	0010	2.5	18.5	37	74	148	286	592	1184
3	0011	3.5	19.5	39	78	156	312	624	1248
4	0100	4.5	20.5	41	82	164	328	656	1312
5	0101	5.5	21.5	43	86	172	344	688	1376
6	0110	6.5	22.5	45	90	180	360	720	1440
7	0111	7.5	23.5	47	94	188	376	752	1504
8	1000	8.5	24.5	49	98	196	392	784	1568
9	1001	9.5	25.5	51	102	204	408	816	1632
10	1010	10.5	26.5	53	106	212	424	848	1696
11	1011	11.5	27.5	55	110	220	440	880	1760
12	1100	12.5	28.5	57	114	228	456	912	1824
13	1101	13.5	29.5	59	118	236	472	944	1888
14	1110	14.5	30.5	61	122	244	488	976	1952
15	1111	15.5	31.5	63	126	252	504	1008	2016
STEP SIZE		1	1	2	4	8	16	32	64

Reviewing the companding DAC functional diagram Figure 8 demonstrates the relationship between step size and I_{REF}. For a μ-law device I_{C0} equals 16.5 chord zero steps and for an A-law device I_{C0} equals 16 chord zero steps. I_{C6} is always equal to I_{REF} in either system. I_{C6} is then equal to 64 times I_{C0} for a μ-law system, and 32 times I_{C0} for an A-law system. The step size can then be related to I_{REF} by the following equations:

$$\text{step size} = I_{REF}/64 \times 16.5 = I_{REF}/1056 \text{ (μ-law)}$$
$$\text{step size} = I_{REF}/32 \times 16 = I_{REF}/512 \text{ (A-law)}$$

Now for a reference current of 528μA the step size for a μ-law system is 528/1056 or 0.5μA. For a reference current of 512μA the step size for an A-law system is 512/512 or 1.0μA. These values concur with those used to generate the tables.

In the design of the PMI DAC-87 the biasing resistors were not scaled to exactly integer values. This was done deliberately to standardize somewhat on 528μA input reference current for both A-law and μ-law parts. The performance of the device is not affected, however the actual scaling is somewhat complicated and will not be discussed in this paper.

Finally if encode output tables were desired for current output they could be obtained by scaling to proper step size the normalized encode tables or adding one-half step to each value in the decode table, where the step size depends on the chord number.

DAC ACCURACY

Companding DACs must be manufactured to satisfy a unique set of parameters. The performance of a companded DAC used for telephony must satisfy the requirements of a communication system on an end-to-end basis. A voice channel is first encoded by one CODEC then decoded by a second CODEC such that the system performance can be measured on an audio-in-audio-out basis. The CODEC performance will be almost completely dominated by the Gain Tracking requirement.

GAIN TRACKING

Gain Tracking refers to the ability of a system to track its input power level. The test is normally made with a system such as that shown in Figure 12.

Gain Tracking is measured by monitoring the input and output levels in decibels. At an input level of −10Bm0 the output is recorded as the output reference level. For ideal Gain Tracking, any change (in dB) of the input level must be matched exactly by the same change in the output level.

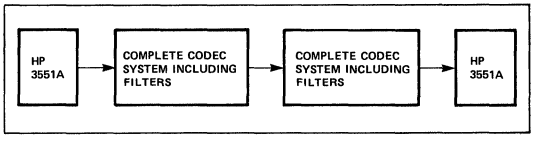


Figure 12. Gain Tracking or S/N Test

This condition is monitored over all input power levels of interest. The extent to which these power level changes differ (again in dB) is a measure of Gain Tracking, also referred to as gain deviation. The ATT/D3 Gain Tracking specification is show in Figure 13.

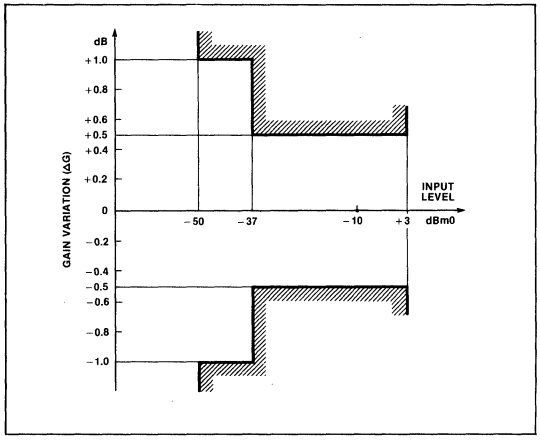


Figure 13. ATT/D3 Gain Tracking Specification

CCITT publishes two separate specifications for Gain Tracking. The apparatus used for making either of these tests is basically the same as that used in Figure 13 except that for the first part of the "method one" test the HP3551A would be replaced with a suitable white noise source at the input and an RMS reading voltmeter at the output. Gain Tracking masks equivalent to those found in CCITT publications are shown in Figure 14.

POWER LEVELS

For PCM channel performance measurements, power levels are characteristically expressed in dBm0. A reference level of 0dBm0 is established by referencing to a code in the **digital** transmission. The binary code pattern required to establish a reference level of 0dBm0 can be found in the CCITT publications. This pattern is reproduced in the PMI Telecommunications Handbook for the readers convenience. The constant repetition of these binary numbers at the normal sampling rate of 8kHz will produce a 1kHz sinusoid at a 0dBm0 reference level. Starting with this definition it can then be shown that a sinusoid whose peak value is just at the system saturation level (all "1s" PCM output) will have a power level of 3.14 and 3.17dBm0 for A-law and μ-law respectively.

SIGNAL-TO-DISTORTION MEASUREMENTS

Signal-to-Distortion is a measure of the total distortion a system will exhibit on an end-to-end basis. As with Gain Tracking this measurement is normally performed on an audio-to-audio basis. A typical setup for measuring Signal-to-Distortion is shown in Figure 15. A wideband (3kHz) filter may be substituted for the C-Message filter shown for some tests.

Figure 16 shows the ATT/D3 specification mask with the performance of a PMI demonstration COMDAC® based shared CODEC system superimposed. This method of measuring Signal-to-Distortion is applicable to either CCITT or ATT specifications.

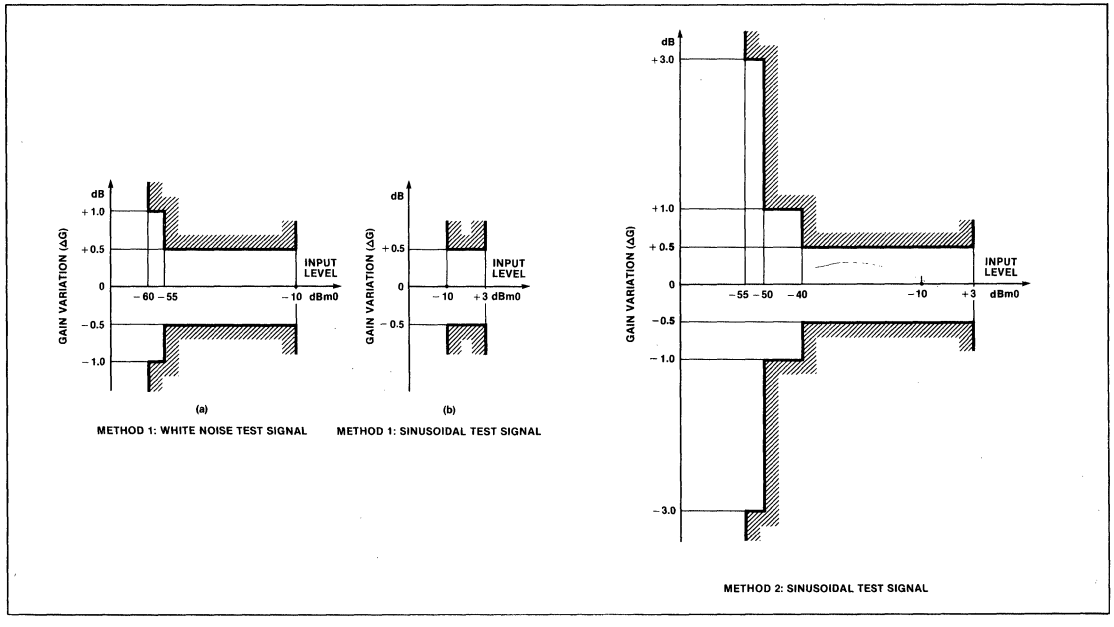
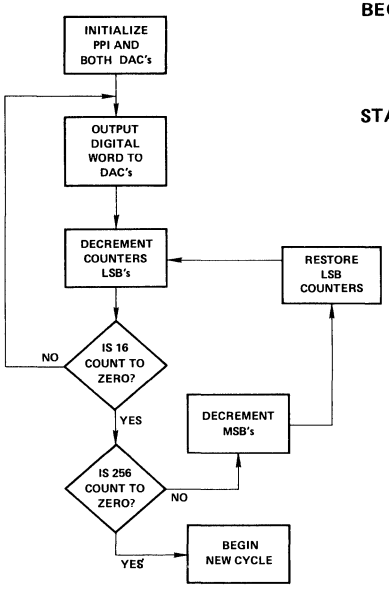


Figure 14. CCIT Gain Tracking Specification

Table 2. Initialize and Load Software for 12-Bit Output Interface




```
BEGIN   LXI   B, 0FFH     Load Ports A and C in counters B and C.
        LXI   D, 0FH      Loads Port B in counter D
        LXI   H, 8003H    Initialize PPI
        MVI   M, 7FH      Control Word sets PPI to output mode
START   MOV   A, B        Output MSB's to DAC #1
        STA   8000H
        MOV   A, D        Output LSB's to DAC #1 and #2
        STA   8001H
        MOV   A, C        Output MSB's to DAC #2
        STA   8002H

        SUI   11H         Decrement LSB's counter
        MOV   C, A
        JNZ   START       Count down from 16
        DCR   B           Decrement DAC #1 MSB counter
        DCR   D           Decrement DAC #2 MSB counter
        MVI   C, 0FFH     Restore LSB counter
        MOV   A, B
        JNZ   START       Count down from 256
        JMP   BEGIN       Start new cycle
```

P.P.I. PORT DESIGNATIONS FOR 12-BIT INTERFACE

PORT A	(PA0 thru PA7)	8 MSB's of DAC #1
PORT B	(PB0 thru PB7)	8 MSB's of DAC #2
PORT C	(PC0 thru PC7)	4 LSB's of DAC's 1 and 2

ADRF/ is the most significant address line and is used here to select the PPI via the $\overline{CS}$ pin.

Once the DAC interface program has initialized all software counters and the PPI counter data is placed on the data bus and latched into the PPI and DAC's. The third step in the software development is to decrement the C register and loop to START until the counter is at zero. The MSB registers (B and D) are then decremented. The C counter is counted down 16 times for each single count down in the B and D register (Table 2). Since the LSB counter starts with 16 and the (2) MSB counters begin with 256, the total count is therefore: 16 X 256 = 4096 (or 12 Bits). Each output ramps from 0 to +10 volts in approximately 170 μsec (at 2 MHz clockrate).

ADC 12-BIT INTERFACE

An ADC interface is vital for entering analog information into an 8080. Because of its popularity the Successive Approximation technique is discussed here. Successive Approximation Conversion (SAC) can be performed with either hardware or software. The software approach will be described later.

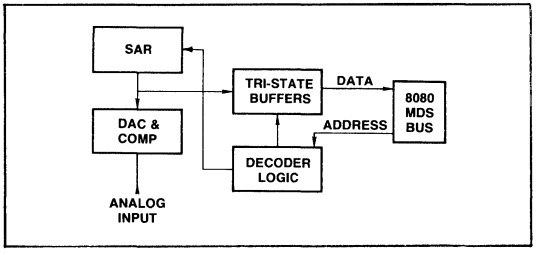


Figure 5. 12-Bit ADC Block Diagram

Although some microprocessors now have ADC's on the chip, a discrete Analog-to-Digital Function still out-performs on-board versions in almost every department. Accuracy and speed, the two crucial parameters in ADC design, lead designers to circuits such as that shown in Figure 5.

To start the conversion a negative going pulse is applied at the Successive Approximation Register (SAR) by the enable of the $\overline{SC}$ gate. A low on ADRF/ at the same time that the Memory Write (MWTC/) line goes low, resets a Flip-Flop (F/F) to start conversion. The F/F is synchronized by the system clock (refer to Figure 6 and Table 3a).

Since the ADC looks like memory to the μP it must be assigned memory locations.

8000H	→	Start Conversion (SC)
8001H	→	MSB Transfer
8002H	→	LSB Transfer
8004H	→	Conversion Complete (CC)

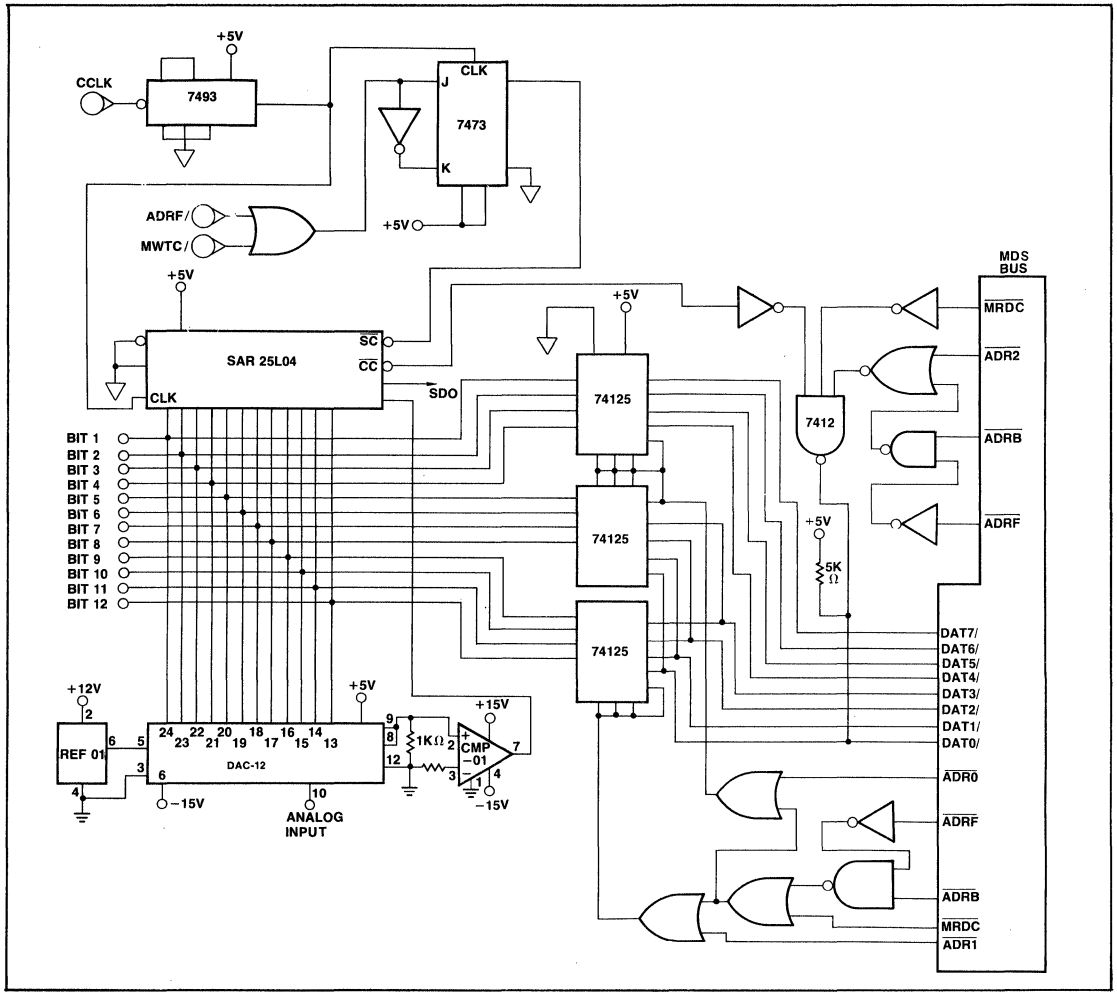
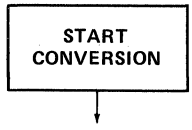


Figure 6. Complete 12-Bit Successive Approximation ADC Interface

Table 3A. Load Software for ADS Interface



SITCON	LXI	H, 8000H	Start Conversion
	MOV	M, A	Load Start Address

After "start conversion" the μP waits 20 μsec for a conversion complete CC signal. This delay is accomplished by a software loop seen in Table 3b.

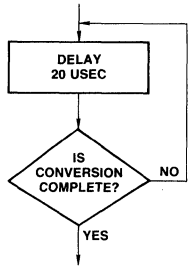
The software delay monitors the LSB data bus line which becomes active when $\overline{CC}$ goes low signifying end of conversion. The system clock period is about 1.6 μsec. Therefore, a 12-Bit conversion takes:

1.6 μsec X 12 = 19.2 μsec

The use of an interrupt would be more efficient because the μP would not have to "Poll" or "Wait" for the $\overline{CC}$ signal. However, interrupts can cause confusion and will not be described at this time. After conversion is complete, the digital result is stored in register pair B and C (Figure 7).

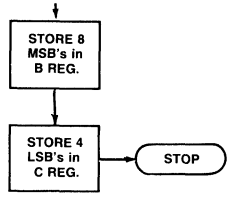
The ADC timing diagram (Figure 8) shows 12 clock cycles starting on the first positive edge after $\overline{SC}$ comes up. Notice

Table 3B. 20μsec Software Delay




```
DELAY   LXI   H, 8004H    Load address
        MOV   A, M         Check CC
        ANA   A            Set parity
        JPO   DELAY        Jump to delay if CC high
```

Table 3C. Storage of 12-Bit Input Data




```
LXI   H, 8001H    Load MSB Address
MOV   B, M        MSB to B Register
LXI   H, 8002H    Load LSB Address
MOV   C, M        LSB to C Register
HLT               Halt
```

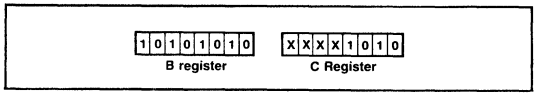


Figure 7. 12 Bits Stored in Two Registers

the SDO data out waveform is low for the five MSB's and high for the seven LSB's. This hex number 7F corresponds to an analog output of 310 mV.

DATA ACQUISITION 8-CHANNEL, 8-BIT INTERFACE

This discussion, so far, has progressed from a simple DAC building block, to a DAC in an ADC. Now the DAC will be described in a multi-input configuration. Since industrial applications, in many instances, require multiple sensing of analog signals, the need for the Data Acquisition System (DAS) becomes very important. The DAS can be broken into five elements. (Refer to Figure 9.)

Basically, the μP sends out four signals: (1) to select a channel in the Multiplexer, (2) select voltage range in the Amplifier, (3) a hold or sample command to the Sample/Hold, (4) and a start conversion command to the ADC.

A unique type of Analog-to-Digital Conversion, using a software SAR technique, is illustrated in Figure 10. Many applications do not require very fast conversion times and for that reason choosing software SAR, in place of a hardware SAR, reduces system cost. This design with DAC, MUX, S/H and SMP sells for less than $20 (excluding digital components).

TRACE 1 CLOCK

TRACE 2 $\overline{SC}$ START CONVERSION

TRACE 3 $\overline{CC}$ CONVERSION COMPLETE

TRACE 4 SDO SERIAL DATA OUT

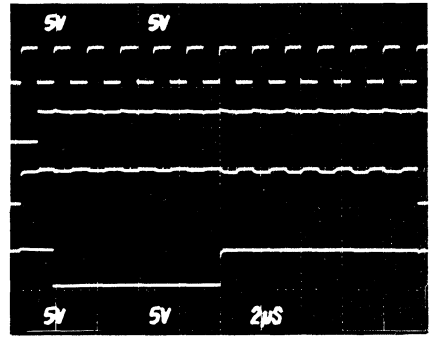


Figure 8. 12-Bit ADC Interface Timing Diagram

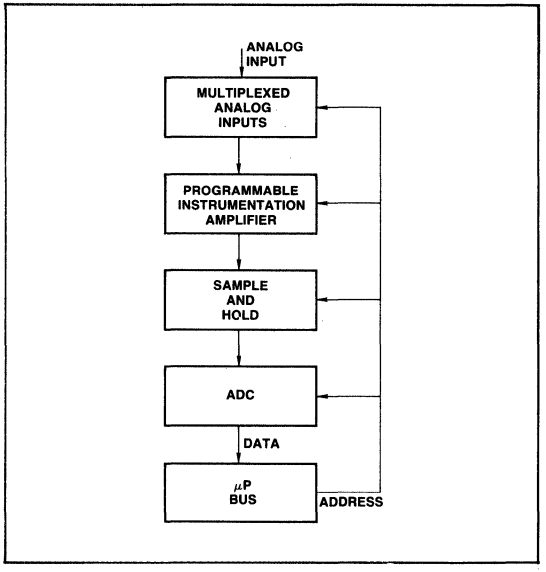


Figure 9. Block Diagram for Data Acquisition

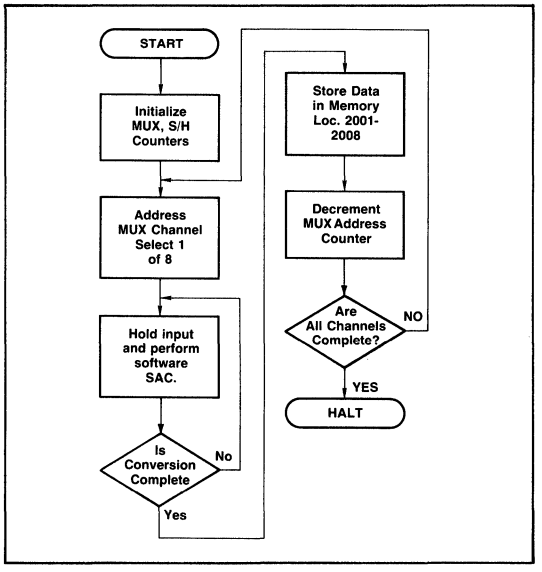


Figure 10. Flow Diagram for Software DAS

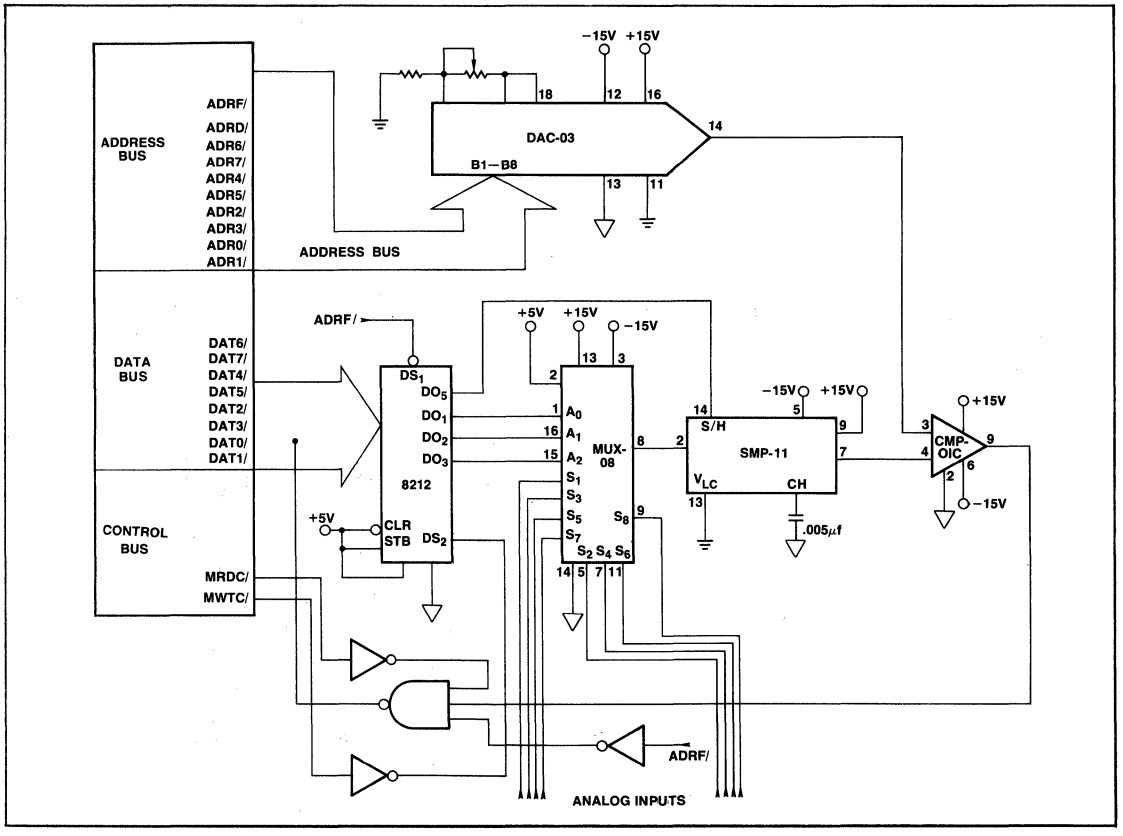


Figure 11. 8-Bit, 8-Channel Data Acquisition System with Software ADC

Throughput of a software DAS is approximately 2000 conversions per second (500 μsec per conversion).

System Description

Eight analog inputs ranging from 0 to 10 volts are connected to the Multiplexer (MUX). The MUX is selected by activating ADRF/. Once the Memory Write MWTC/ goes low, the MUX address in the μP accumulator is latched to the 8212 (Figure 11). The analog input selected is fed through the MUX and sampled by the Sample and Hold Amplifier (S/H). Notice the deletion of the Programmable Instrumentation Amplifier. If ranging is required, a simple resistance programmable amplifier can be used (Figure 12).

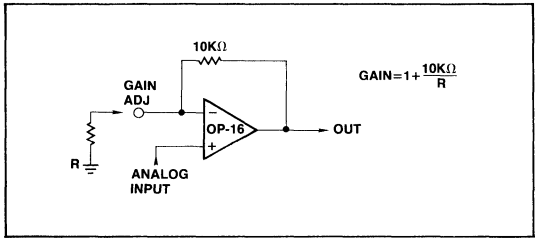


Figure 12. Programmable Gain Amp

A NOP instruction is inserted in the program after the MUX address selection to hold the processor for 2 μsec during the MUX settling time (refer to Table 4). Acquisition time of the S/H is 3.5 μsec and this delay is provided by the software during addressing. The analog signal is held while the program goes to ADCON (or the start of conversion). Registers B and C combine to act as a SAR during the software ADC portion of the program.**

Since the DAC-03's settling time is 1.5 μsec, the address bus must stay active (low) for this time. This circuit operates off the MDS Internal Acknowledge Signal. For faster throughputs a 2 μsec delay, once MRDC/ goes low, should be executed at the XACK/ (MDS Acknowledge) pin.

Register D stores the MUX address in the S/H Sample Mode, while the E register simply contains the Hold Command and MUX address. Both registers are decremented from eight to zero. Channel S7 is converted first and the Digital Data stored in Memory Location 2008. The program loops around eight times. Each time the JNZ START instruction tests the MUX counter for zero. After eight channels have been converted and stored, the program halts. This results in channels S8 through S1 being stored in Memory Locations 2008 through 2001 respectively.

HIGH SPEED 8-CHANNEL, 12-BIT DAS

Applications requiring fast throughputs such as a High-Speed Data Acquisition system, must resort to the hardware SAR in place of software SAR. Though throughputs as high as 50,000 channels per second are possible, 15,000 channels per second (to 12-Bit accuracy) is more realistic when processor time is included.

**For more information on software controlled ADC, please see Appendix II and contact Precision Monolithics for Application Note AN-22.

Table 4. 8-Channel Data Acquisition Program

```
Register   B = SAR TRIAL
           C = TEMPORARY SAR RESULT
           D = MUX ADDRESS COUNTER IN SAMPMODE
           E = MUX ADDRESS COUNTER IN HOLDMODE

BEGIN:  LXI   D,1808H     Load S/H MUX Counter.
START:  LXI   H,8000H     Set Memory Map.
        MOV   A,D         Ready MUX Address.
        MOV   M,A         Address MUX in Sample Mode.
        NOP               Wait for MUX to Settle.
        MOV   A,E         Address MUX in Hold Mode.
        MOV   M,A         Hold Input.
ADCON:  LXI   B,8000H   ┐
        MOV   A,B       │
        MOV   H,A       │
TEST:   ORA   C         │
        CMA             │
        MOV   L,A       │
        MOV   A,M       │
        CMA             │
        ANA   A         │ < ADC Conversion
        JPO   TOOHI     │
        MOV   A,B       │
        ORA   C         │
        MOV   C,A       │
TOOHI:  MOV   A,B       │
        RAR             │
        MOV   B,A       │
        JNC   TEST      ┘
        LXI   H,2000H     Initialize Data Storage
        MOV   L,E
        MOV   M,C
        DCR   D           Decrement Sample Counter.
        DCR   E           Decrement Hold Counter.
        MOV   A,E
        JNZ   START
        HLT
```

As in the previous DAS, this system (Figure 13) utilizes a precision MUX, S/H, DAC, comparator and digital components. For simplicity purposes, only an 8-channel system will be described. This system is expandable to 40 channels using five MUX-08's or to 64 channels using four MUX-16's. Further expansion is possible by inserting a 1 of 8 decoder between the latch and MUX as seen in Figure 14.

Since emphasis is on speed, consistent with 1 LSB accuracy and 1/2 LSB linearity, the software has only 21 instructions consuming 37 bytes of memory. It takes 83 μsec to complete initialization, single-channel conversion and data storage in memory (see Table 5).

SYSTEM SOFTWARE AND HARDWARE DESCRIPTION

Again, the MUX is addressed and an analog channel selected. The analog signal is held by the S/H and sent to a 12-Bit ADC for conversion. The label BEGIN starts initialization, setting the D/E register pair and the Stack Pointer (SP). START addresses the MUX and S/H. Start conversion (STCON) in software) begins with a low at $\overline{SC}$ then loops in DELAY waiting for conversion complete $\overline{CC}$. The instruction LHLD 8001 loads both H and L Registers with the 2-byte ADC word. This word is pushed onto the stack by the instruction PUSH H.

MUX counters D and E are then decremented and the program loops back to START for the next analog channel. Eight channels are stored in Memory at locations 2000 through 200F (see Figure 15).

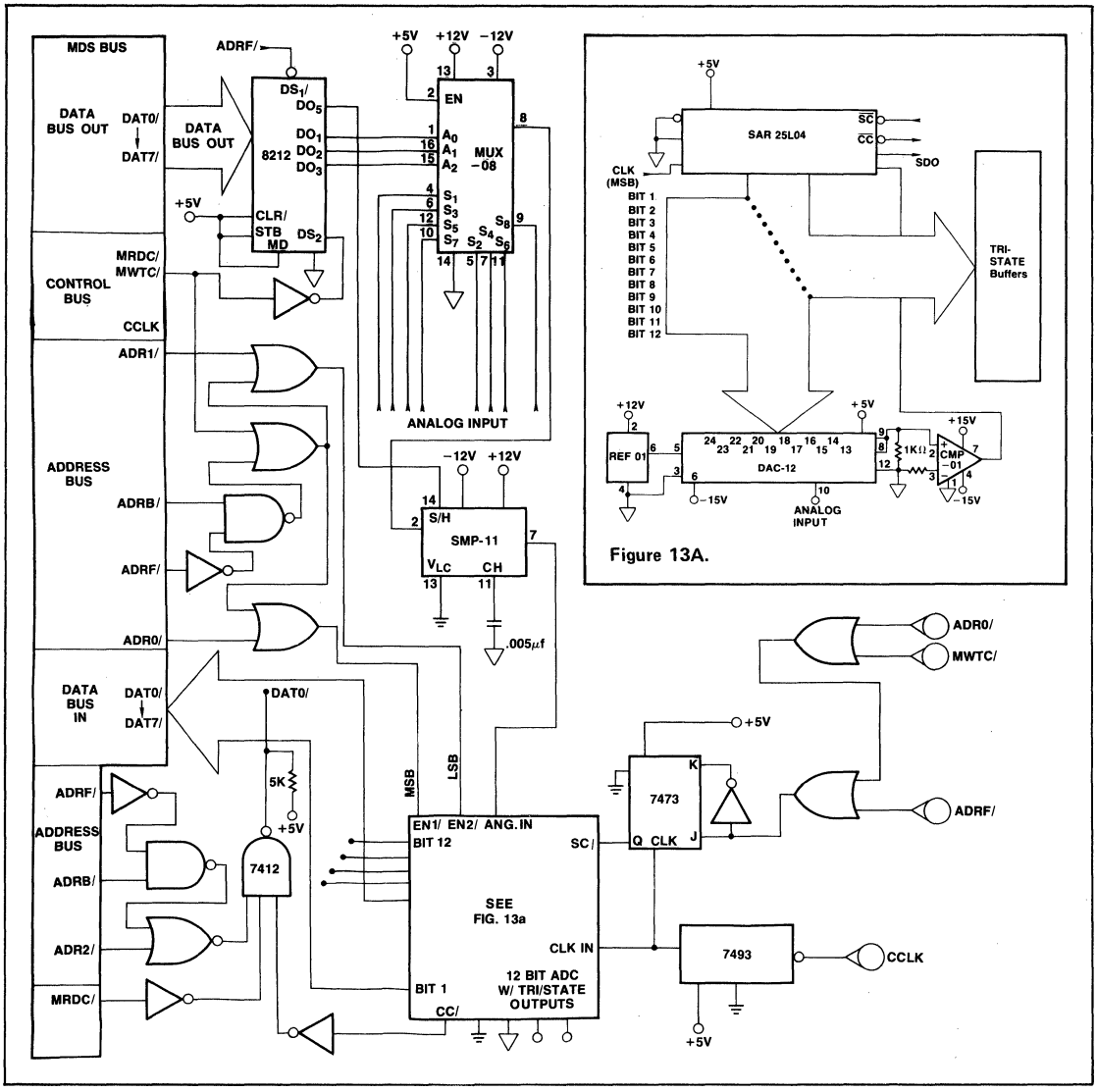


Figure 13A.

Figure 13. Complete, 12-Bit, 8-Channel High-Speed Data Acquisition System

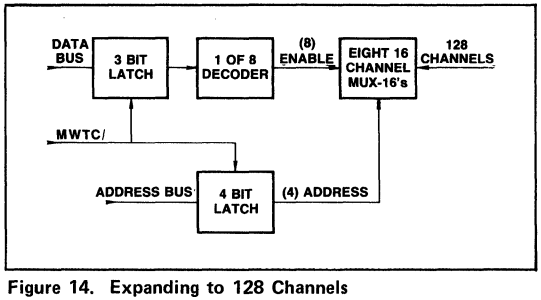


Figure 14. Expanding to 128 Channels

The MUX channel is latched until the S/H Amplifier has stored the input signal on a Hold Capacitor (see Figure 16). This diagram shows three channels with S8 and S6 at +5 volts and S7 at ground.

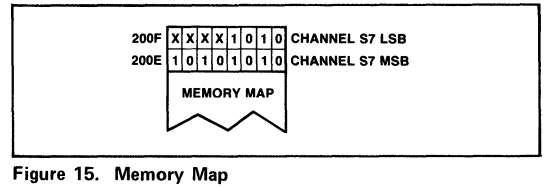


Figure 15. Memory Map

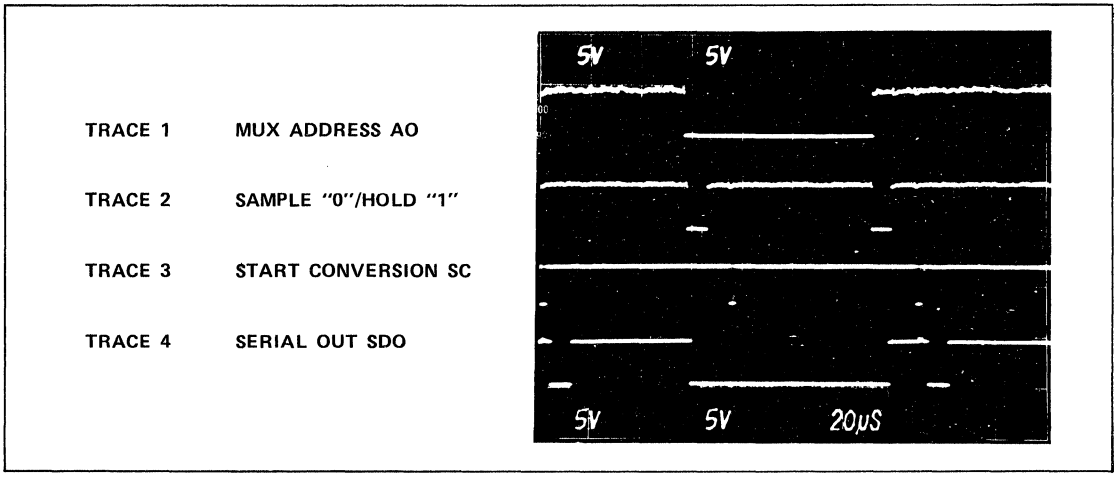


Figure 16. Timing Diagram for High-Speed 12-Bit DAS Showing Three Channels

Table 5. Program for 12-Bit, 8-Channel DAS

```
        ORG   1000H     ;
BEGIN:  LXI   D, 1808H  ; LOAD MUX COUNTERS
        LXI   SP,200FH  ; SET STACK POINTER
START:  LXI   H, 8000H  ; SET MEMORY MUX ENABLE
        MOV   A, D      ; READY MUX
        MOV   M, A      ; ADDRESS MUX AND SAMPLE
        NOP             ; WAIT FOR MUX TO SETTLE
        MOV   A, E      ; ADDRESS MUX AND HOLD
        MOV   M, A      ; HOLD ANALOG INPUT
STCON:  LXI   H, 8005H  ; ADDRESS START CONVERT
        MOV   M, A      ; START CONVERSION
DELAY:  LXI   H, 8004H  ; WAIT FOR CONV COMPLETE
        MOV   A, M      ; CHECK CC
        ANA   A         ; SET PARITY
        JPO   DELAY     ; CC?
        LHLD  8001H     ; TRANSFER 2 BYTE DATA
        PUSH  H         ; STORE DATA IN STACK
        DCR   D         ; COUNT DOWN SAMPLE COUNTER
        DCR   E         ; COUNT DOWN HOLD COUNTER
        MOV   A, E      ; TEST 8 CHANNELS
        JNZ   START     ; START NEXT CHANNEL
        HLT
```

CONCLUSION

The interface circuits discussed herein were designed around the 8080 Microbus and MDS (also Single Board Computer SBC 80/10) bus. Memory Mapping was used exclusively to increase software speed and add flexibility to I/O control operations.

Many designers are under the impression that in Data Converters speed is the sole figure of merit. But the Speed-versus-Cost Trade-Off must be considered. Speed is directly proportional to cost. The software SAR technique has speed advantages over Integrating, Voltage-to-Frequency and Tracking types of ADC, but prices are generally higher. The hardware versus software trade-off is critical because software development generally costs at least $10 per line of code. Of course, large production quantities can amortize software costs over a high volume of units.

On the other hand, DAC requirements do not have software trade-offs, but speed is again proportional to cost.

The DAS described here has shown only multiplexed techniques. However, dedicated ADC-per-channel types can also be implemented. Though the multiplexed DAS version is slower, it is also less expensive.

Both the ADC and the DAS, when interfaced to transducers, should be five to ten times more accurate than the sensor. Transducers generally range in accuracy from 0.05% to 5%. As an example, a 12 bit (0.012% or ½ LSB) converter should be selected for a transducer exhibiting 0.1% accuracy so as not to introduce further error in the system.

In conclusion, the D/A converters flexibility in microprocessor input and output applications was emphasized.

BIBLIOGRAPHY

1. "MCS-80 User's Manual", Intel Corporation, 10/77.

2. AN-22, "Software Controlled Analog to Digital Conversion Using DAC-08 and the 8080A Microprocessor" Precision Monolithics, Inc., 1/77.

3. "Intellec Microcomputer Development System, Hardware Reference Manual", Intel Corporation, 1976.

APPENDIX I

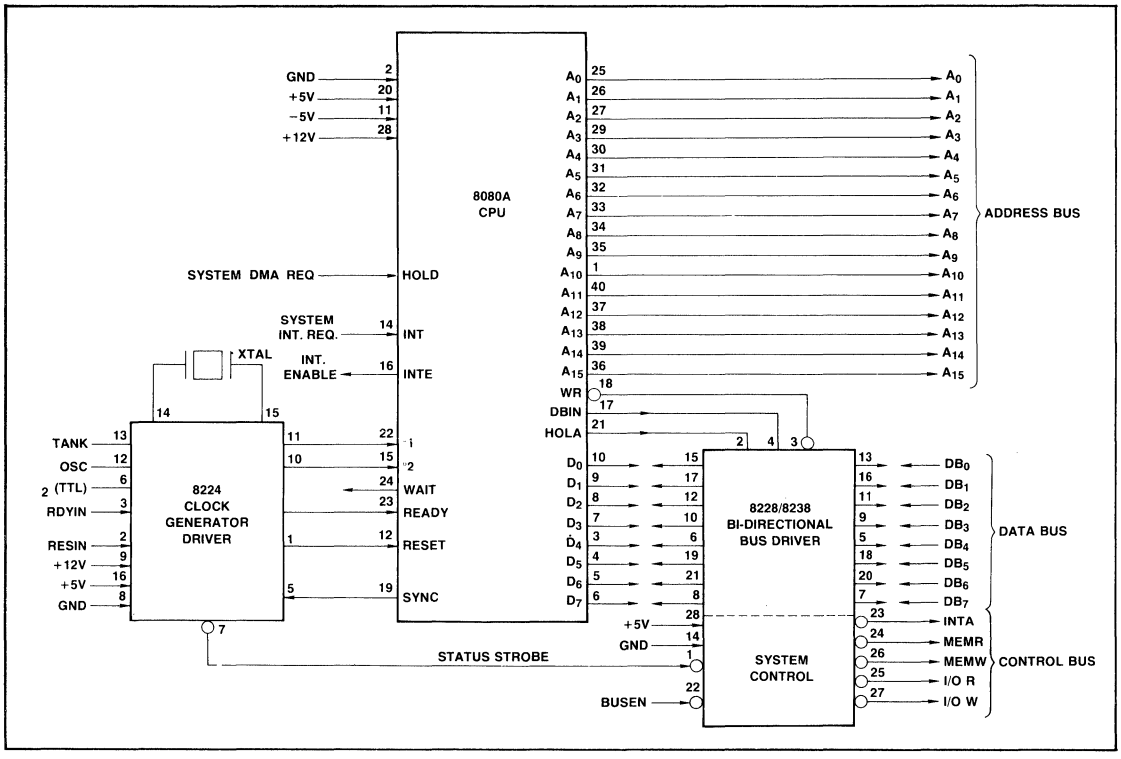
There are many bus structures in use today. In the interest of brevity and clarity only Intel's Microbus and Intellec MDS or SBC 80 (also called MULTIBUS) will be described here.

Both the Microbus and MULTIBUS structures are divided into address, data and control. The MULTIBUS, however, utilizes inverted buffers throughout for ease of interface. On the MULTIBUS, many extras are found in the control section to provide "Handshake" functions. Eight lines of priority interrupts are also added features that distinguish the MULTIBUS.

In reality the Microbus is internal to a MULTIBUS system. Conversely, the Microbus can be expanded to duplicate the MULTIBUS if required. The following table and figure further show these differences.

PIN ASSIGNMENT FOR SBC AND MDS INTELLEC BUS

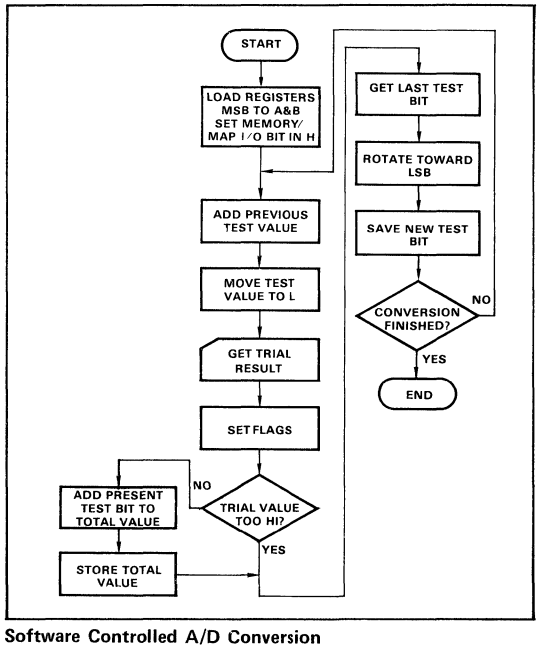
	PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
	1	GND	Signal GND	2	GND	Signal GND
	3	VCC	+5 VDC	4	VCC	+5 VDC
POWER	5	VCC	+5 VDC	6	VCC	+5 VDC
SUPPLIES	7	VDD	+12 VDC	8	VDD	+12 VDC
	9	VXI	Supply Spare 1	10	VXI	Supply Spare 1
	11	GND	Signal GND	12	GND	Signal GND
	13	BCLK/	Bus Clock	14	INIT/	Initialize
	15	BPRN/	Bus Pri. In	16	BPRO/	Bus Pri. Out
BUS	17	BUSY/	Bus Busy	18	BREQ/	Bus Request
CONTROLS	19	MRDC/	Mem Read Cmd	20	MWTC/	Mem Write Cmd
	21	IORC/	I/O Read Cmd	22	IOWC/	I/O Write Cmd
	23	XACK/	XFER Acknow	24	INH1/	Inhibit 1 disable RAM
				26	INH2/	Inhibit 2 disable PROM or ROM
	25	AACK/	Special	26		
	27			28		
SPARES	29			30		
	31	CCLK/	Constant Clock	32		
	33	INTR/	Direct Int	34		
	35	INT6/	Parallel	36	INT7/	Parallel
	37	INT4/	Interrupt	38	INT5/	Interrupt
INTERRUPTS	39	INT2/	Requests	40	INT3/	Requests
	41	INT0/		42	INT1/	
	43	ADRE/		44	ADRF/	
	45	ADRC/		46	ADRD/	
	47	ADRA/	Address	48	ADRB/	Address
ADDRESS	49	ADR8/	Bus	50	ADR9/	Bus
	51	ADR6/		52	ADR7/	
	53	ADR4/		54	ADR5/	
	55	ADR2/		56	ADR3/	
	57	ADR0/		58	ADR1/	
	59	DATE/		60	DATF/	
	61	DATC/		62	DATD/	
	63	DATA/	Data	64	DATB/	Data
DATA	65	DAT8/	Bus	66	DAT9/	Bus
	67	DAT6/		68	DAT7/	
	69	DAT4/		70	DAT5/	
	71	DAT2/		72	DAT3/	
	73	DAT0/		74	DAT1/	
	75	GND	Signal GND	76	GND	Signal GND
	77	VBB	−10 VDC	78	VBB	−10 VDC
POWER	79	VX2	−12 VDC	80	VX2	−12 VDC
SUPPLIES	81	VCC	+5 VDC	82	VCC	+5 VDC
	83	VCC	+5 VDC	84	VCC	+5 VDC
	85	GND	Signal GND	86	GND	Signal GND



Micro-Bus Pinout and Mnemonics

APPENDIX II

Software controlled Analog-to-Digital Conversion offers a medium-speed, low-cost way to convert analog signals with less hardware. This technique applies the Successive Approximation method, whereby the analog input is compared to an analog output of the D/A converter one bit at a time. The DAC is programmed by a microporcessor. This μP tests the comparators output each time the DAC's output changes. When the analog input and DAC output are equal, the digital count at the DAC is stored in memory. The resultant digital count is then the equivalent analog input (see the software ADC flow diagram).



Software Controlled A/D Conversion

APPLICATION NOTE 31

SUCCESSIVE APPROXIMATION REGISTER DESIGN FOR MULTI-CHANNEL CODEC'S

by Guido Pastorino

INTRODUCTION

This Application Note describes a low cost, high speed Successive Approximation Register (SAR) design for use with 24-channel or 32-channel encoders. It is implemented with standard MSI functions which are available in several processes: T^2L, Low Power Schottky, etc. The functions are also available in CMOS, although CMOS is only fast enough to encode 4 channels or less. The system is optimized for use with PMI COMDAC® DAC-86/87 D/A converter in conjunction with the CMP-01 precision voltage comparator and REF-01 voltage reference. This design of fers a low-cost alternative to the 2502 LSI SAR by sharing a common system timing circuit over all the encoders (usually 2 or 3) used in a 24 or 32 channel system.

First, the traditional encoding procedure using the 2502 LSI SAR is explained. Next, the improved method described here will be discussed and compared with the 2502 method.

TRADITIONAL ENCODING METHOD

An encoding sequence begins with the sign bit comparison and decision. During this time the comparator is a polarity detector only. The Encode/Decode (E/D) input is held at a logic "0". Therefore, no current flows into the encode outputs, and the comparator is effectively disconnected from the DAC. Once the input polarity has been determined, the E/D input is changed to a logic "1", allowing current to flow into $I_{OE}(+)$ or $I_{OE}(-)$ depending upon the sign bit answer.

For positive inputs, current flows into $I_{OE}(+)$ through R_1, and the comparator's output will be entered as the answer for each successive decision. For negative inputs current flows into $I_{OE}(-)$ through R_2, developing a negative voltage which is compared with the analog input. An exclusive-OR gate inverts the comparator output during negative trials to maintain the proper logic coding, all ones for full scale and all zeros for zero scale. However, the exclusive-OR gate must not invert the signal during the sign bit decision, hence the need for the second exclusive-OR gate and the additional D flip flop in the 2502 LSI SAR encoder.

The successive removal technique requires the first decision to be made at the code 01111111, sequentially turning off all bits until all decisions have been made.

Traditional encoding systems begin the encode cycle by setting the binary input at 01111111. This is because LSI SARs are not designed to accommodate a DAC that is implemented in a sign-magnitude configuration.

IMPROVED ENCODING METHOD

For the sign-magnitude configuration such as the COMDAC® DAC-86/87 system, the initial setting of 10111111 performed by the SAR described here allows the

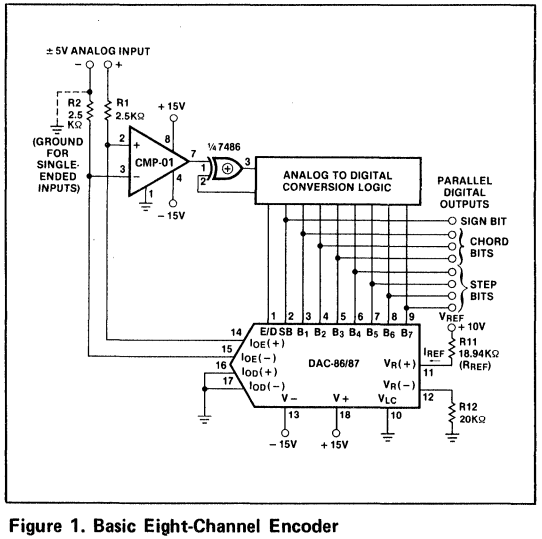


Figure 1. Basic Eight-Channel Encoder

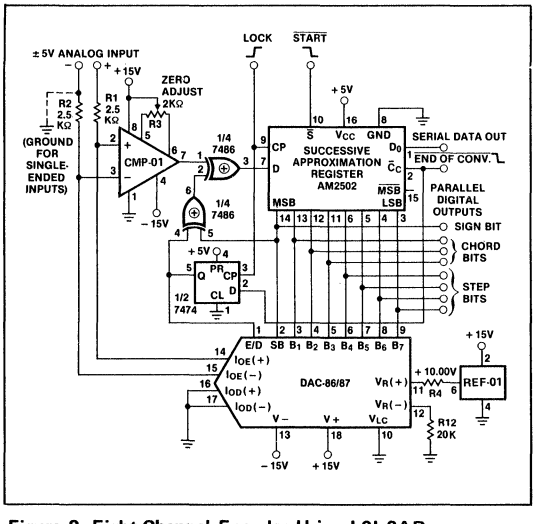


Figure 2. Eight-Channel Encoder Using LSI SAR

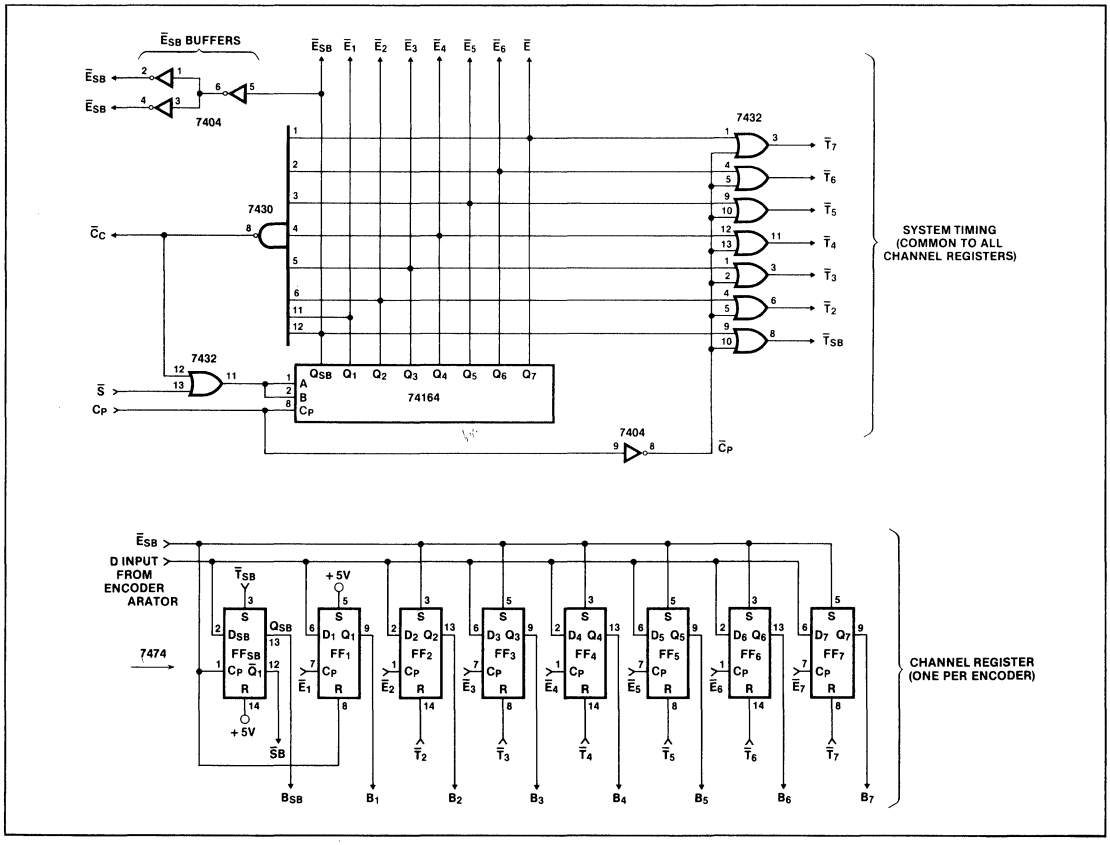


Figure 3. Successive Approximation Register

DAC to settle for one additional clock cycle and requires no logic circuitry to prevent the exclusive-OR gate from inverting during the sign bit trial. The theory of operation follows.

The start conversion pulse $\overline{S}$ occurs just before positive-going clock edge $C_{\overline{S}}$ as shown on the SAR waveforms. The 74164 shift register will have all Q outputs at the 1.0 level so long as the circuit has been operating for eight or more clock pulses. With $\overline{S}$ high the OR gate will continue to input a logic one into the shift register on every pulse. With all inputs at logic one the 7430 eight input NAND gate will have a zero output, thus the $\overline{S}$ signal going low will cause the next clock pulse $C_{\overline{S}}$ to clock a zero into the shift register output Q_{SB} which becomes the leading edge of negative-going pulse $\overline{E}_{SB}$. Now one input lead to the 7430 is a zero and the output of the NAND gate goes to logic one. The zero propagates down the shift register appearing on outputs Q_{SB} to Q_7 in succession, keeping the NAND gate output at logic one. Because of the OR gate this logic one is clocked repeatedly into the shift register outputs from Q_{SB} to Q_7. The cycle will not repeat if $\overline{S}$ is not held low for longer than 8 clock cycles; however, the actual duration of the $\overline{S}$ pulse is not important so long as it does not cause

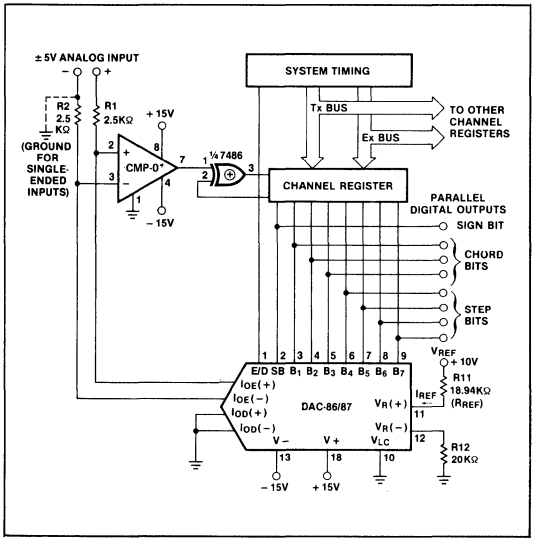


Figure 4. Eight-Channel Encoder with Improved Design SAR

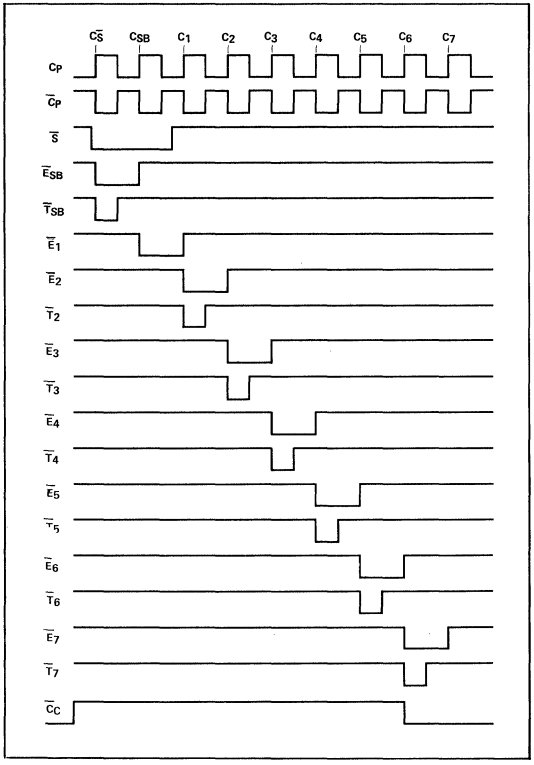


Figure 5. SAR Waveforms

the circuit to re-cycle. The $\overline{S}$ pulse need not be synchronized with the clock. $\overline{C}C$ stays high for 8 clock cycles.

As E_{SB} goes to zero it resets FF_1 and sets FF_2 through FF_7. When the circuit is used with the encoder circuit shown here, $\overline{E}_{SB}$ is used to keep the DAC in the decode mode for the duration of $\overline{E}_{SB}$. $\overline{T}_{SB}$, which is logically $\overline{E} + \overline{C}_P$, occurs at the leading edge of $\overline{E}_{SB}$ and sets FF_{SB} to SB = 1. Thus, on the first clock edge after $\overline{S}$ goes low the SAR is set to 10111111. The trailing edge of $\overline{E}_{SB}$ is used as a clock for FF_{SB} so that the comparator output, which represents the sign bit so long as the DAC is being held in the decode mode, is clocked into FF_{SB}. The $\overline{Q}$ output of FF_{SB} becomes the SB signal which drives the control input of the exclusive-OR gate.

By forcing this signal to a zero during the Sign Bit trial the exclusive-OR gate is in the proper non-invert mode while the sign bit is generated. $\overline{E}_1$ goes low just as $\overline{E}_{SB}$ goes high. No $\overline{T}_1$ signal is needed since FF_1 was set low during the initial setting. The rising edge of $\overline{E}_{SB}$ puts the DAC-86/87 back into the encode mode. The DAC internal circuit has been settling to the X0111111 magnitude output since the first clock after $\overline{S}$ went low, so the rising edge of $\overline{E}_1$ will clock the most significant bit of the quantized signal into FF_1. The remainder of the conversion proceeds as follows: $\overline{T}_2$ resets FF_2 and the rising edge of $\overline{E}_2$ clocks the second most significant bit into FF_2. $\overline{T}_3$ resets FF_3 and the rising edge of $\overline{E}_3$ clocks the second most significant bit into FF_3 and so on through $\overline{T}_7$ and $\overline{E}_7$.

E_{SB} BUFFERS

The implementation of this SAR requires a package count of 4 for the system timing which can then be shared over 3 channel registers, provided the $\overline{E}_{SB}$ buffers are properly used to prevent excessive fan-out on the $\overline{E}_{SB}$ line.

CONCLUSION

A low cost, alternative method of successive approximation register design has been shown which is optimized for use with multi-channel encoders for PCM systems.

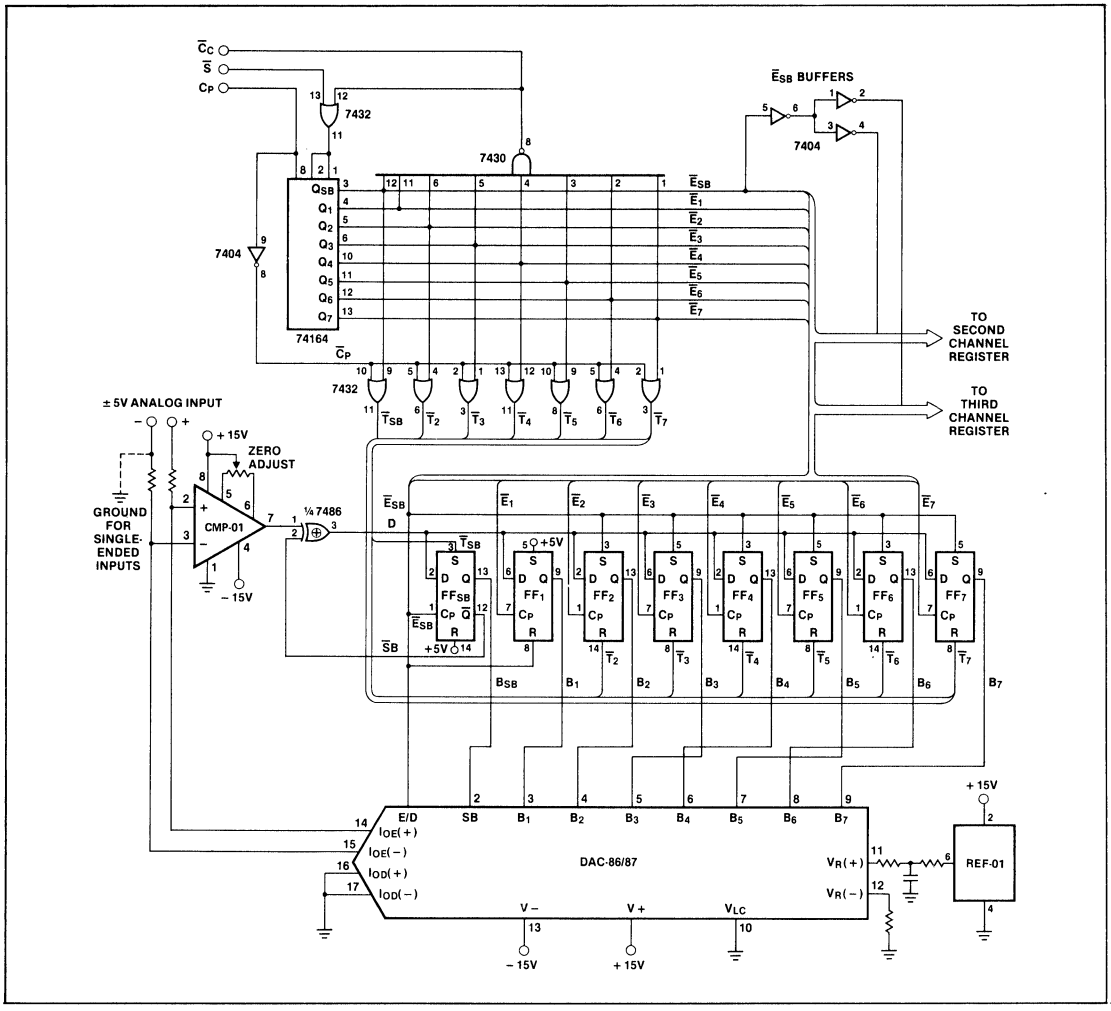


Figure 6. Improved Eight-Channel Encoder Complete Schematic

APPLICATION NOTE 32

SINGLE SUPPLY OPERATION OF PMI MULTIPLEXERS

by Shelby D. Givens

INTRODUCTION

In addition to normal operation (+/− supplies), the PMI family of BIFET multiplexers (MUX-08/88, MUX-24, MUX-16, and MUX-28) performs quite well in single supply systems. This Application Note explains single supply operation as it applies to BIFET and CMOS multiplexers. Common requirements are in battery-operated systems and in microprocessor-based, single supply data acquisition systems. BIFET and CMOS devices are compared for R_{ON} variation versus power supply voltage (V_S), then settling times.

CONNECTIONS FOR SINGLE SUPPLY OPERATION

Figure 1 shows single supply connections for the entire PMI BIFET multiplexer family. Each multiplexer handles 0 to +10V signals with a +15V supply. The signal range is conservatively rated to be (V_S−4V) as a maximum, and zero volts as a minimum. One important fact will be demonstrated in the performance photos to follow: THE MULTIPLEXERS OPERATE LINEARLY WITH SIGNALS LESS THAN ZERO VOLTS!

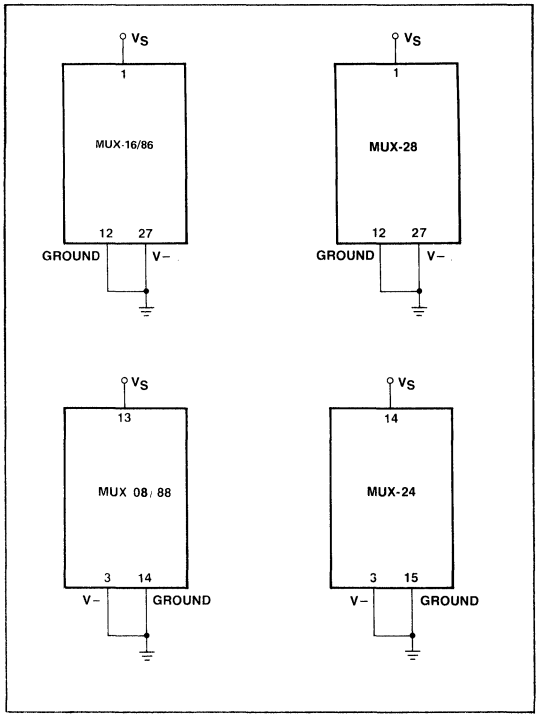


Figure 1. BIFET Multiplexer Single Suppy Connections

BIFET VARIATION OF R_{ON} WITH V_S (MUX-08)

Figure 2 shows the test circuit and defines the test conditions (MUX-08). Figure 3 shows the performance of a MUX-08 driving a 1KΩ load. The positive voltage should be 1.10V and the negative voltage should be −0.4V. The reason for the output voltages being less (magnitude) than the above is due to the R_{ON} of the multiplexer switches. Curves 1 and 2 show that R_{ON} does not vary as V_S varies from +5V to +15V.

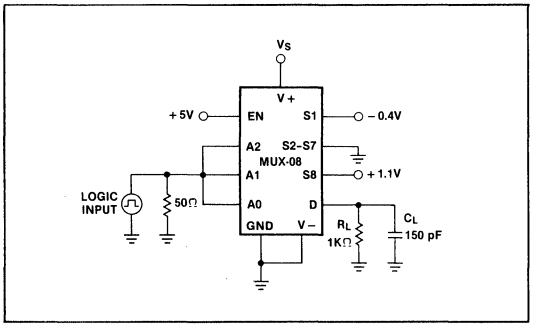


Figure 2. Test Circuit

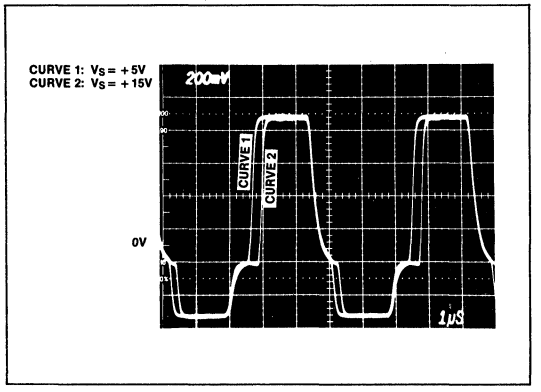


Figure 3. BIFET Variation of R_{ON} with V_S

CMOS VARIATION OF R_{ON} WITH V_S (508 pin-compatible device)

The CMOS multiplexer (connected as shown in Figure 4) DOES show a variation in R_{ON} as V_S is varied from + 6V to + 15V. This is evidenced by the curves shown in Figure 5. Note that while the positive peak voltages in Figure 3 are the same for both curves, the peaks differ in Figure 5.

One very important consideration when choosing a multiplexer is the non-linearity (or distortion) introduced by the switch when it is ON. What is important is the CHANGE in R_{ON} which occurs because of external variations such as power supplies. In particular, the variation in R_{ON} shown in Figure 3 is 148 ohms. The R_{ON} at V_S = + 6V is 1000 ohms,

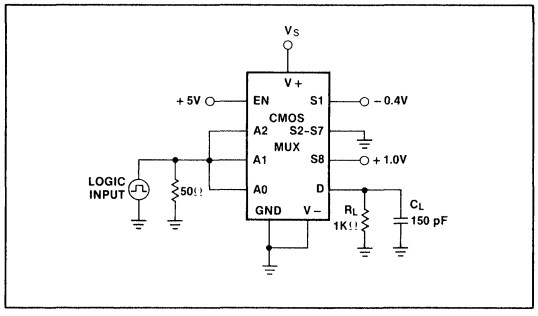


Figure 4. Test Circuit

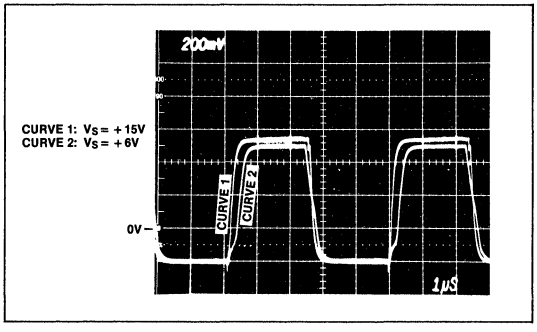


Figure 5. CMOS Variation of R_{ON} with V_S

while its value at V_S = + 15V is only 852 ohms. A change of 148 ohms represents a 1.48% error if the load resistor is 10,000 ohms. In battery-operated systems (which is what a lot of single supply applications are), distortion due to power supply variations is generally not acceptable.

CMOS VS. BIFET — EFFECT OF R_{ON} ON SETTLING TIME

Figure 6 defines the test conditions used for the BIFET and CMOS multiplexer curves shown in Figure 7. In this case,

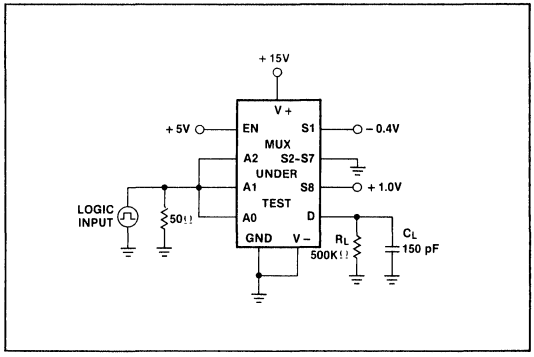


Figure 6. Test Circuit

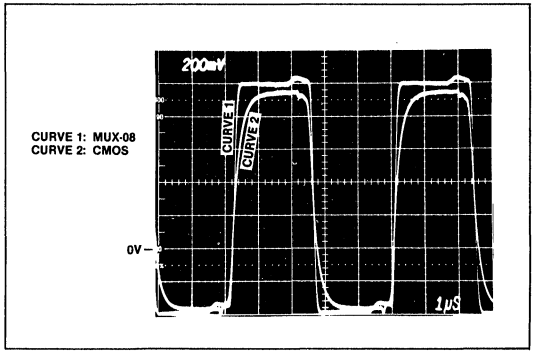


Figure 7. CMOS vs BIFET Settling Time (Unloaded Output Voltage)

R_L is large enough so that the output voltages will reach the input voltage levels. Note that MUX-08 does just that, while the CMOS multiplexer does not reach the final value.

The problem is settling time, and occurs because the R_{ON} of the CMOS device is considerably larger than the MUX-08 (852 ohms as opposed to 250 ohms). A final note concerns the fact that the multiplexers are switching signals at 400 mV *below ground* with no distortion.

CONCLUSION

The information presented has shown how BIFET multiplexers handle analog inputs in single supply systems, with R_{ON} independent of power supply variations, and with fast settling time.

APPLICATION NOTE 33

A GUIDE TO HYBRID INTEGRATED CIRCUIT DESIGN

by Mike Parsin

INTRODUCTION

This application note is a guide to the design and development of thin and thick film hybrid microcircuits. To aid the hybrid designer, emphasis is placed on assembly techniques and general design rules to avoid common design problems.

The importance of choosing the proper assembly method, for a particular application, is discussed. Assembly techniques include substrate and die attach methods, wire bond alternative, and sealing practices. Common design pitfalls associated with dice, films, conductors, and layout are also discussed.

ASSEMBLY PROCEDURE

Hybrid assembly is divided into four steps:

1. Substrate attachment to the package.
2. Die attachment to the package.
3. Wire bonding die to substrate.
4. Package sealing.

Correct selection of the methods used for the steps above is essential for cost effectiveness, and, in some cases, proper circuit operation. Although these operations may not seem important on the surface, methods must be chosen to provide the required quality and meet the specifications.

ATTACHMENT PROCEDURES

Eutectic Attach

Eutectic-alloy bond is the method used by PMI for standard IC products because it is more cost effective than epoxy. It is a metal attach which is accomplished by heating the substrate and die until a "wetting" action takes place. The die is then placed in contact with the substrate. This results in an excellent shear strength attachment. Gold backing is recommended for hybrid construction.

Both substrate to package and die to substrate attachment can be performed by the eutectic method. Although less expensive, this metal attach requires temperatures in excess of 300°C to wet the gold for proper attachment. Eutectic type of bonding is generally recommended for digital applications or low component count hybrid packaging.

Non-Conductive Epoxy Attachment

Epoxy is recommended for high precision applications because linear monolithic dice and film resistors can be affected by excessive temperatures. For substrate attach, a non-conductive, low out-gassing, film type epoxy, such as Ablefilm 517, is suggested. Film epoxies can also be used for die attach.

Conductive Epoxy

When attaching die to the substrate, conductive silver-filled epoxies are excellent choices for precision low drift circuit applications. PMI recommends Ablebond 36-2, Ablefilm ECF 550, EPO-TEK H31, or DuPont 5504 epoxies. Cure durations and temperatures are low, generally one hour at 125°C. Assembly temperatures are critical because Beta degradation and film resistivity change are directly proportional to heat and duration. Film changes can be expected when temperatures exceeding 300°C are approached (temperature at which films are heat treated). Heat treat is very important to film stabilization. Monolithic dice are susceptible to temperature, as previously mentioned. The degree of susceptibility is dependent on lot and the manufacturer's process. Common parameters affected because of temperatures are gain, input offset voltage, and input bias current.

WIRE BONDING ALTERNATIVES

There are four methods used in attaching die metalization to the substrate conductor or package beam:

1. Chip and Wire (most common)
2. Flip Chip Beam Tape
3. Beam Lead
4. Chip Carrier

Chip and Wire

Chip and wire is the most common method of bonding the die to an electrical conductor (see Figure 1). Types of wire bonders include thermocompression, thermosonic and ultrasonic. Thermocompression bonding is fast, and usually gold wire is used. Cutting through the oxide on the metalization is sometimes a problem though. Ultrasonic wire bonding solves the oxide problem by a scrubbing action that cuts through it. The disadvantage of ultrasonic bonding is that the angle of the machine's wedge to the bonding pad can cause problems in multi-die packaging. Ultrasonic, however, is ideal for monolithic IC manufacturers, where only one or possibly two die are in a package. The thermosonic method

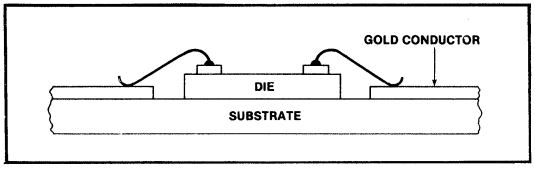


Figure 1. Chip and Wire Attach

is a combination of ultrasonic and thermocompression bond which uses heat, pressure, and scrubbing to give the best of both techniques.

Although PMI uses aluminum ultrasonic bonding on all of its products, hybrid manufacturers have generally found gold wire thermosonic to be more cost effective for hybrids.

Flip Chip Beam Tape

The flip chip on tape is another method of bonding die to a substrate (Figure 2).

"Bumps," constructed of copper or other conductive material, are deposited as part of the metalization. The die is then flipped over and eutectically attached to conductors on the tape. During hybrid assembly the tape is bonded to the substrate in a single operation.

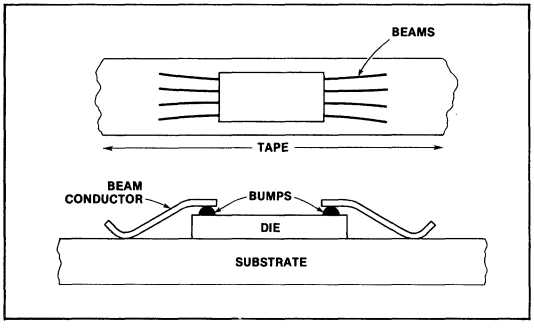


Figure 2. Flip Chip Beam Tape Attach

Beam Lead Bonding

The beam lead technique basically has the lead (which is approximately a 10-mil beam) connected to the metalization at wafer fabrication. A single attach operation combines both die and wire attach (Figure 3). This method is not used much in industry today.

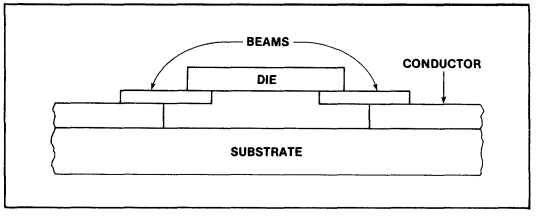


Figure 3. Beam Lead Attach

Chip Carrier

The chip carrier is a miniature, leadless package intended mainly to increase package density. This carrier contains the tested IC attached usually with chip and wire and eutectic or epoxy bond. The carrier can then be attached (or reflow soldered) to a Dual-in-Line motherboard or Hybrid.

PACKAGE SEALING

Epoxy

Film precut epoxies such as ABLEFILM 517A and 550 are commonly used for sealing hybrid packages. Although an epoxy seal can be hermetic, this type of seal has been known to leak after a period of time. PMI does not recommend epoxy for high reliability applications. Film epoxy is an excellent low temperature (165 °C cure) sealing method suggested for thin film commercial data conversion applications. Epoxy seals are usually used with Epoxy B and Ceramic packages.

Glass Seal

Used with ceramic and side-brazed packages, glass seal is a high temperature operation, in excess of 400 °C. As mentioned previously, heat treat for films occurs at this temperature, and film change is possible. In applications where absolute resistance is not nearly as critical as resistor tracking, the problem is not as severe, since resistors change together. PMI uses glass sealing and recommends it for high reliability applications.

Braze and Welding Sealing

Braze sealing is performed on a welding machine using a gold-tin or solder preform between the package and lid. Sealing temperatures are restricted to the sealing rim only. The pure weld seal (metal to metal) is another excellent seal but requires much higher sealing temperatures. However, as in brazing, the temperature is localized at the weld only. Brazing and welding are used with all-metal Kovar packages and are excellent for high reliability applications. Welding is ideal for space applications because a braze seal can possibly introduce contaminates into the package from the preform.

AVOIDING PROBLEMS IN HYBRID CIRCUIT DESIGN

This section deals with typical problems that arise because of improper design. Care must be taken in hybrid design because problems such as ground noise, ground loops, crosstalk, gain errors, and high temperature tracking errors can result. These problems can be substantially reduced with proper resistor placement, conductor or resistor line widths, layout, and film selection.

SUMMING AMPLIFIER DESIGN EXAMPLE

Consider the summing amplifier circuit in Figure 4 where R_A, R_B, and R_C must track the feedback resistor R_1. Layout is critical, so R_1 should be located as close as possible to R_A, R_B, and R_C for best TCR tracking and minimum gain error. The sum node is a high impedance point and is susceptible to crosstalk and noise pickup. This node should be isolated with a ground ring if possible. A low TCR thin film such as nickel-chromium or silicon-chrome is recommended to reduce tracking errors between the resistors. The ground should be an analog ground with no digital ground returns on it which would introduce noise.

16-BIT DAC DESIGN EXAMPLE

High resolution D/A converters are ideal for thin film hybrid designs. Figure 5 illustrates a 16-bit converter using four active ICs for current output and five dice for the voltage version.

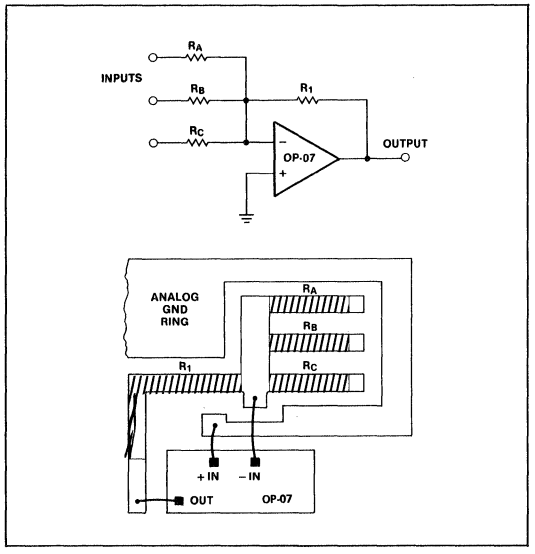


Figure 4. Summing Amplifier Layout

Resistor placement is again very important. Reference resistors R_A and R_{A1}, must be adjacent to R_B for proper tracking. Also, R_1, R_2, R_3, R_4 should be located close to R_{SPAN} for minimum gain TC error. Low TC films are used (see Table 1).

FILMS AND CONDUCTORS

The hybrid designer should be aware of pitfalls where film and conductors are concerned. The gold conductor, like the film resistor, can cause many problems and should be considered as a possible source of error.

Films can be either thick or thin, but there are many other characteristics that must be considered when selecting a film (see Table 1).

The substrate material can also determine TCR tracking. A smooth surface, such as silicon or glass, is excellent for resistor tracking. Silicon substrates dissipate power better than glass; however, stray capacitance is higher on the silicon surface. PMI uses silicon-chrome film sputtered on silicon.

Thick film is an excellent choice for general purpose applications. This film varies with paste and firing temperatures however. The thick film process applies the "Inked" resistance by silk-screening to a ceramic substrate. This technique is advantageous in high power and in most circuits where TC is not critical.

Gold conductors introduce 0.01 ohms per square (Ω/□) to as much as 0.1 Ω/□ resistivity. A long, narrow line width results in a high resistance. Gold bonding wires, one mil in diameter, can introduce 2 milliohm per milli-inch of resistance. Also, gold conductors typically have temperature coefficients of about +3000ppm/°C which should not be overlooked. It is recommended that the conductor be short and as wide as possible.

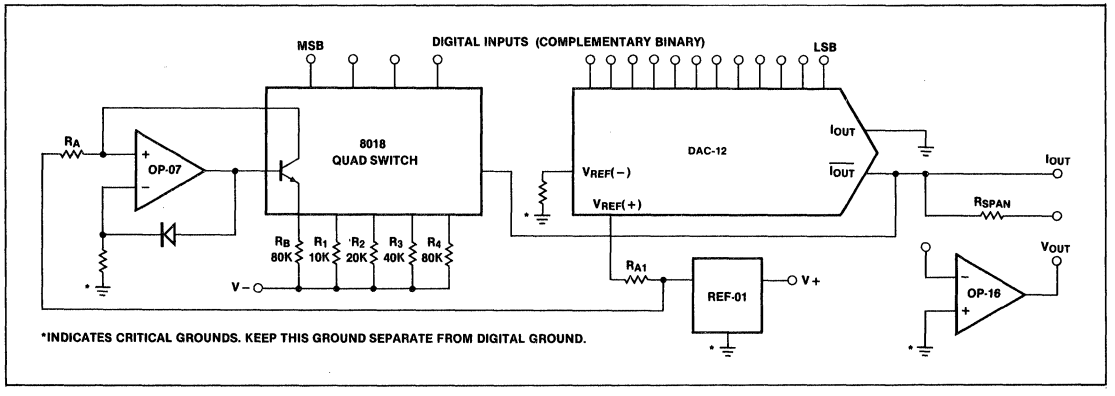


Figure 5. 16-Bit Digital-to-Analog Converter IC

Table 1. Film Types and Uses

TYPE	DENSITY (Ω/□)	TCR (ppm/°C)	TRACKING (ppm/°C)	APPLICATIONS
Nickel-Chromium	50 to 500	±50	±1	Excellent tracking. Precision data conversion.
Tantalum-Nitride	27 to 120	−150	±2	Precision circuits. Excellent long term stability.
Silicon-Chrome	2000	±100	±1	Precison/high density.
Cermet	2000	±250	±50	High density/commercial.
Thick	10 to 1 Meg	±100	±10 to ±50	General purpose/high power.

CAPACITANCE EFFECT

Conductors running parallel to each other can act as plates of a capacitor. This capacitance is shown in the expression:

$$C \propto \frac{L}{D} (k)$$

where C = Capacitance
$\propto$ = Proportional To
L = Conductor Length
D = Distance Between Conductors
k = Dielectric Constant
= a) Air is 1.0006
b) Glass is 6-10

The parallel conductor "capacitor effect" should be considered when designing high speed circuits (see Figure 6).

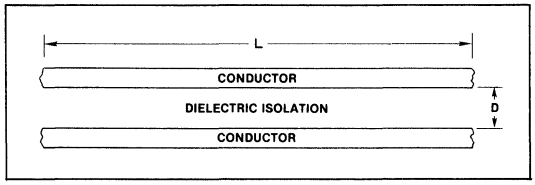


Figure 6. Conductor Capacitance

MONOLITHIC INTEGRATED CIRCUIT

The monolithic die can be damaged by excessive temperature or pressure. Temperature can cause Beta degradation, but also has some good effects. Low temperatures, around 125°C for long durations, can cause parameter shifts evidenced by a power burn-in operation. Power burn-in does stabilize active devices much in the same way as a temperature bake reduces film change.

Pressure or strain during die attachment or wire bond can also cause parameter change which is usually catastrophic. A punch-through problem is very common to thermocompression wire bonding. This problem occurs when the ball bond pierces or pushes the aluminum metalization down through the silicon or active portion of the die. Chips can also be strained when eutectic or epoxy die attach causes unbalanced stress effects.

CONCLUSION

This application note has described problems and solutions associated with assembly as well as physical design. Proper circuit operation at the breadboard level does not always guarantee hybrid operation. Layout, selection and design of film resistors, and design of conductors can be critical.

Wire bonding such as ultrasonic and thermosonic are reliable bonding methods because they scrub through metalization oxide. Epoxy die attach and package sealing are useful where low temperature assembly is required. Remember, temperatures in excess of 300°C can cause dice and film electrical changes.

In conclusion, the hybrid designer must be aware that hybrid operations and processes are not all the same. Selection of methods to be used is important.

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APPLICATION NOTE 34

BCD DACs SIMPLIFY INTELLIGENT INSTRUMENT DESIGN

TAKE ADVANTAGE OF BCD OUTPUTS TO MAKE A "SMART" DMM

by Gary Grandbois

Because the decimal system is easy to understand and use, many instruments and controls are designed to accept binary-coded-decimal (BCD) code at the user-to-equipment interface. In some cases, equipment designers also find that it is easier and less expensive to carry the BCD code through the system instead of converting to binary code and converting back.

The device that makes this possible is known as a BCD digital-to-analog converter. Its output current is a function of the BCD number at the input and the input reference current.

The use of BCD is especially popular in the design of instruments that provide a numerical display. Falling into this category are counters, calculators, temperature monitors, DMMs and a wide variety of dedicated instruments.

A typical example of the use of a BCD DAC to drive a 1mA analog meter is shown in Figure 1. The BCD DAC, a DAC-20,

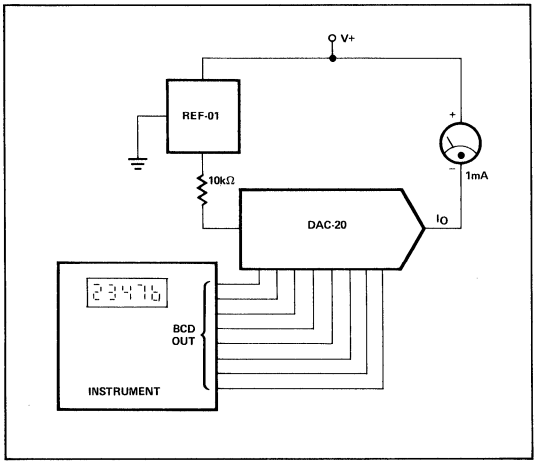


Figure 1. Analog Meter Driver

interfaces between the BCD output of an instrument and the meter input. The required reference voltage is delivered to the DAC-20 by a +10-volt precision voltage reference integrated circuit, the REF-01. A similar application in which the DAC-20 is used to drive a strip-recorder is shown in Figure 2.

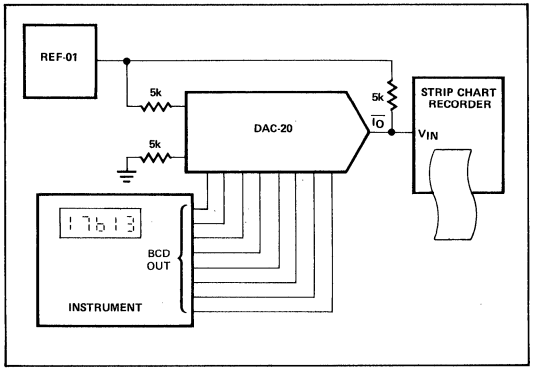


Figure 2. Time Analysis

The principal benefit provided by a system using the configuration shown in Figure 2 is the relative ease with which the information is grasped. Analog "hard copy" allows the reader to focus on particular aspects of a curve; trends that immediately stand out might be obscured in a numerical printout.

The use of a BCD DAC in process control is illustrated in Figure 3. The BCD outputs and the BCD DAC provide an analog feedback path to the control function.

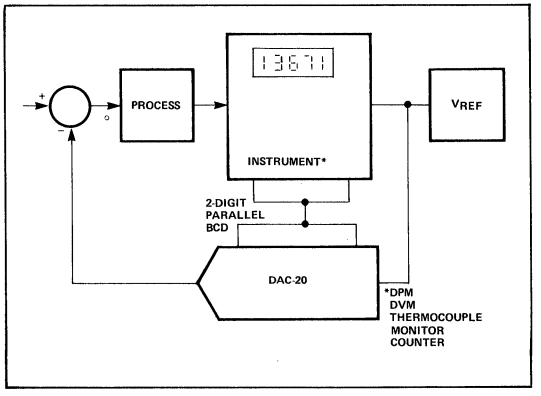


Figure 3. Process Control Loop

The reasons for using analog meters in digital instrumentation systems, while not immediately obvious, are very compelling. Digital meters provide precise readings without the ambiguity and subjective interpretation imposed by analog meters. Analog meters, however, are ideal for indicating the degree and direction of trends and for revealing rate of change. Contrast, for example, observing acceleration on an analog meter as opposed to a digital meter.

When viewing an analog meter, interpretation of larger or smaller merely involves needle position rather than number interpretation. A digital system that combines digital display precision with analog trend display provides the user with complete information presentation. The market acceptance of this concept is shown by the analog meter options offered in quality digital multimeters.

Many of the high-quality instruments available have a BCD output available in either a bit-parallel, digit-serial format (Multiplexed BCD) or in a fully-parallel format (usually provided for a printer interface). BCD DACs are readily used with instruments having either output and can be interfaced by direct connection or by opto-isolators which eliminate large common-mode voltages.

In instrument design, the BCD DAC is the tool that can turn the mere monitoring of a process into a controlling mechanism. By employing a BCD DAC, a thermocouple monitor can be transformed into an oven controller, a counter can be made into a speed controller, or a digital voltmeter can be converted into a process controller.

THE DAC-20

The 2-digit DAC-20 is one of a new breed of low-cost BCD interface converters. A bipolar multiplying DAC, with complimentary current outputs, the DAC-20 can be used with either positive true or negative true (complementary) logic. The unused output must be connected to ground or a voltage source capable of sourcing 1.65 times the reference current. Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source.

The capability of the DAC-20 to accept a variable reference allows it to "multiply" the analog reference with the digital BCD word. A circuit diagram depicting the elements on the DAC-20 chip is given in Figure 4.

One particularly useful application of a BCD DAC is that of adding greater functional capability and intelligence to an instrument which uses a 7-segment numeric display. In this type of instrument, BCD is the common coding format of the counters, A/D converters or thumbwheel switches used.

The two forms of BCD code mentioned earlier are found in these instruments. One is parallel BCD which is most often found in older instruments or in instruments not designed with LSI logic ICs; the other is multiplexed BCD which comes out in a 4-bit parallel (digit) fashion where successive digits are time multiplexed on a 4-bit bus and are identified by additional signal lines called digit strobes (or digit select lines).

The parallel output format allows easy interfacing to the input of the DAC-20; the multiplexed format, however, requires demultiplexing of the digits of interest into a parallel format. The circuit shown in Figure 5 performs this function

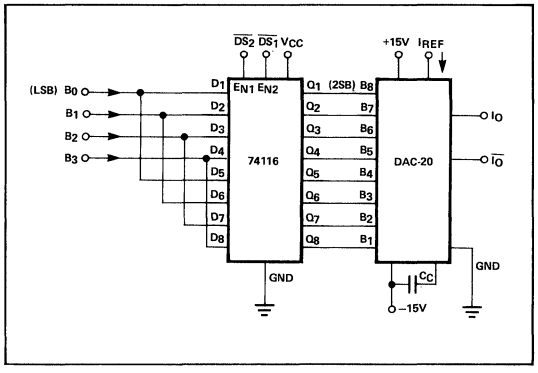


Figure 5. BCD De-Multiplexing and Converter

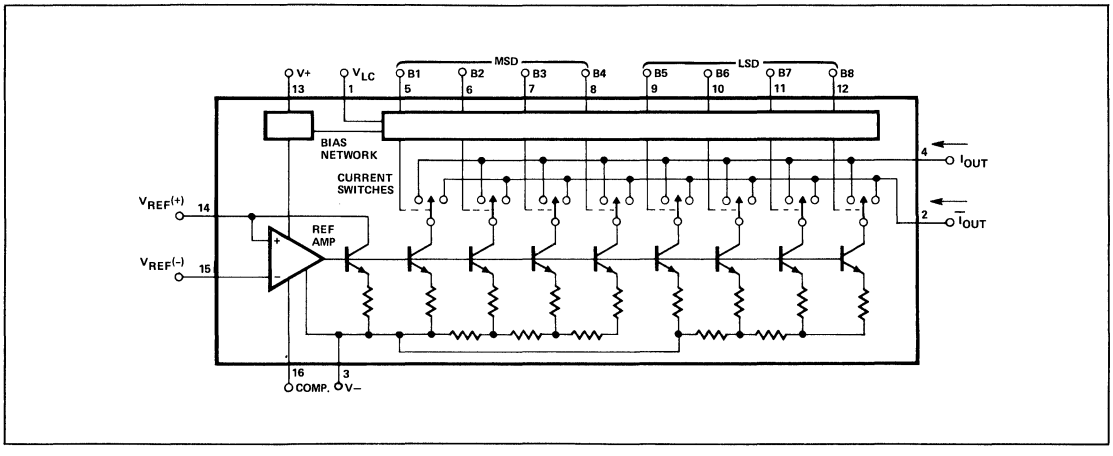


Figure 4. DAC-20 High-Speed Multiplying BCD D/A Converter

for systems which have inter-digit blanking (dead-time between digit selects) and active low digit strobes. The 4 bits of BCD data for each digit are loaded into the 4-bit latch each time the digit select goes low.

The latch/BCD DAC circuit shown in Figure 5 can be applied in a wide variety of applications. In this application note this circuit will be used to add "intelligence" to DPM-based instruments.

AUTO-NULL/AUTO-TARE APPLICATIONS

In the application shown in Figure 6 the BCD DAC is performing in a digital panel meter system in which zero offsetting negative feedback is used. If the transducer/DPM combination that should be reading zero is reading some number other than zero, that number can be loaded into the 8-bit

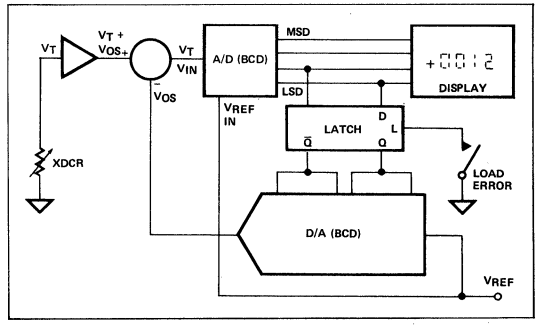


Figure 6. Auto-Nulling Diagram

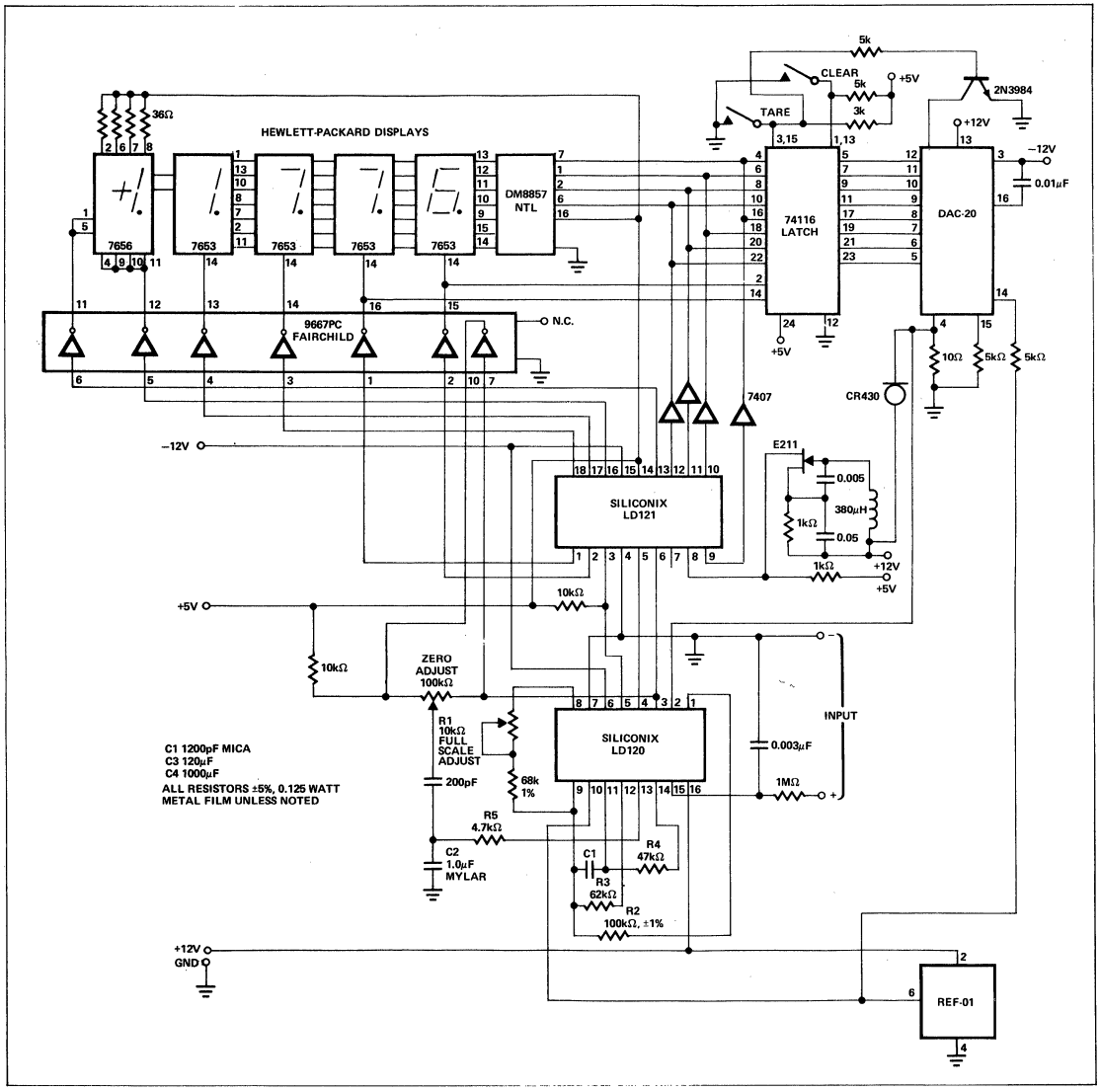


Figure 7. Automatic Nulling DPM

latch. The DAC will then supply a difference voltage to the DPM to return the zero input reading to zero.

Applications of this circuit are many and varied. They range from auto-tare digital scales where the tare button is pushed to subtract the weight of the empty container ("tare" weight) from subsequent weighings to push-button zeroing to cancel non-ideal transducer and signal conditioning offsets. The use of the circuit configuration depicted here allows the 2-digit DAC-20 to null a 4-1/2, 5-1/2, or 6-1/2 digit instrument since it operates on only the Least Significant Digits (LSDs).

The approach described in Figure 6 is implemented in the circuit of Figure 7 which presents a DPM with differential input capability to perform analog subtraction at the ADC. The DAC-20 adds null correction to the last two LSDs of the depicted 4-1/2 digit DPM. A latch stores the null "word" which is loaded during the push button nulling phase (the taring phase for scales). The DAC output, proportional to this word, is subtracted at the input of the DPM until the latch is either cleared or a new null word is entered. No pot adjustments are needed and the adjustment required is simply reduced to the pushing of a single button.

The nulling circuit is able to handle bipolar offsets by providing an initial zero offset of 1/2 of the DAC-20's range. This is achieved by biasing the current output of the DAC with a positive constant current from the current regulator diode CR430. Combined with the 10Ω resistor, the correction circuit can null offsets of up to ±5mV in 100μV steps.

In those applications where a sign-magnitude BCD code is required, an external switch can provide the sign-bit control of the current. This is shown in Figure 8.

ANALOG METER

The demultiplexing circuit described in Figure 5 can be applied in an analog meter driver as shown in Figure 9. The Most Significant Digits (MSDs) are latched to give a continuous digital input to the BCD DAC and a continuous analog output to the analog meter (0 to 1mA).

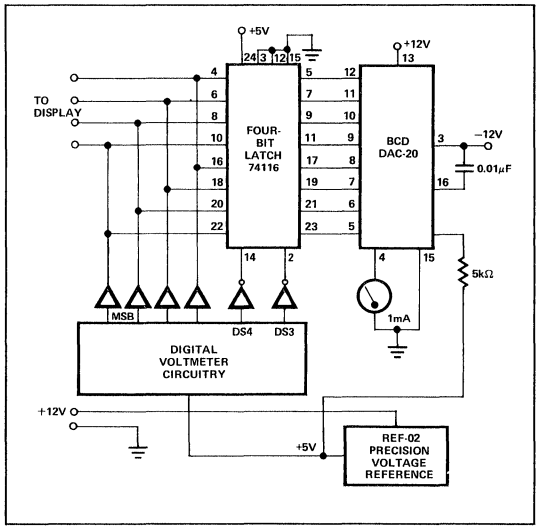


Figure 9. Drive Circuitry for 4-1/2 DPM with Analog Meter

The meter reads only magnitude, not sign. The sign of the digital display must be viewed for polarity determination.

Although the DPM is a 4-1/2 digit instrument (the 1/2 digit gives 100% overranging), the analog meter only reads to the 4-digit range and then returns to zero for an output of 10,000. Either the MSD can be read from the digital display, since it should be the most slowly changing digit, or the analog meter must be considered in error.

Basically the circuit shown in Figure 9 is the same circuit used for the auto-nulling circuit shown in Figure 7 except

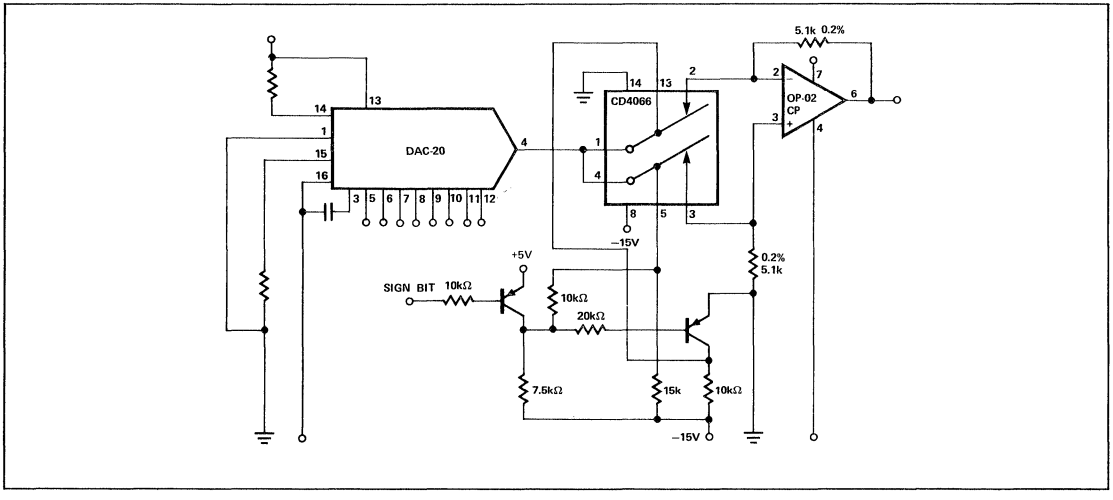


Figure 8. Sign-Magnitude BCD DAC

that the BCD DAC does not provide circuit feedback and the output current is continuously used to drive an analog meter.

The 8-bit latch is not used for data storage; rather its function is to demultiplex the multiplexed BCD. The high output compliance of the DAC-20 allows direct meter connection without the use of operational amplifiers.

The range of an analog meter and other devices employing BCD DACs can be extended by adding the circuitry shown in either Figure 10a or 10b which permits the addition of a third digit. In the circuit of 10a, the group of exclusive "ORs" sums the LSB of the 3rd digit into the second digit to give correct DAC outputs up to 159 (which can be loosely considered to be 2-1/2 digits). This circuit functions by noting the logic transfers needed in the second digit.

Thus, the LSB requires no change, $B_0 = B_0$; the second LSB is merely $= B_1 +$ MSB; the third bit $B_2 = B_2 + (B_1 \cdot \text{MSB})$; the fourth bit $B_3 = B_3 +$ MSB. Erroneous outputs will be produced for codes other than 0 to 159. An alternative method is to use a 4-bit adder, such as a 7483, to drive the MSD of the DAC. The presence of a "1" in the third digit should provide a 1010 code to the adder for proper operation. The circuit in Figure 10b shows how the complementary current output can be gated and used as an additional bit giving 2-1/2 digit voltage output for codes to 199.

AUTO CALIBRATION

Another useful feature for digital instrumentation is the capability to perform its own error correction (self-

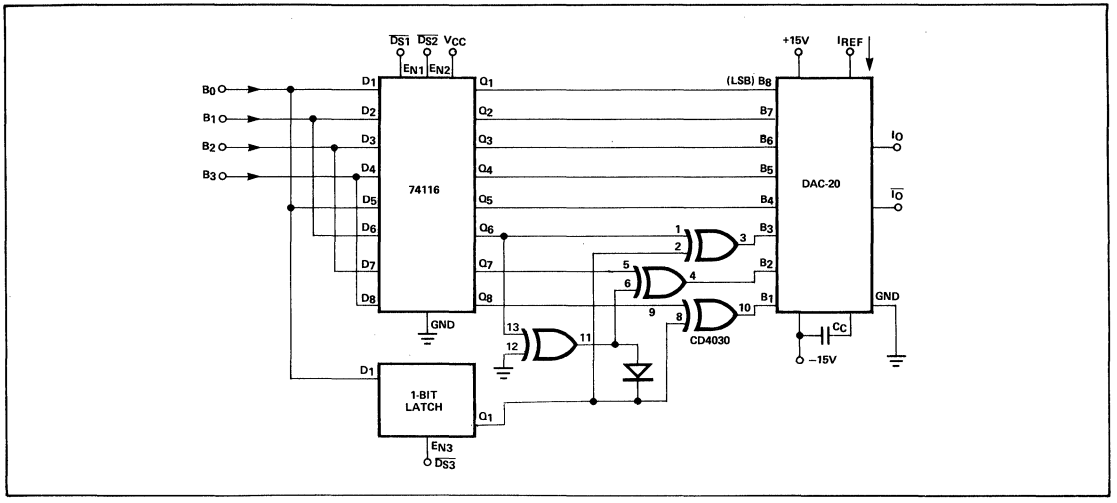


Figure 10a. "2-1/2" Digit Operation (159 Count)

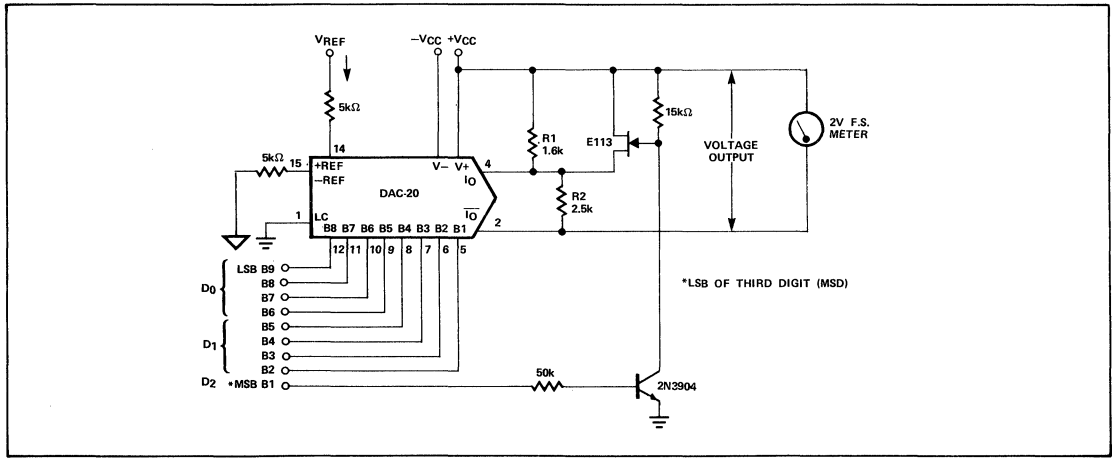


Figure 10b. "2-1/2" Digit Operation (199 Count)

in conjunction with a laboratory standard parameter (voltage, current, resistance, temperature, etc.).

Calibration is costly and time consuming; it requires expensive equipment and specialized personnel. Therefore simplified self-calibrating capability in instruments is extremely desirable.

A 2-digit BCD DAC, such as the DAC-20, can provide an instrument with self-calibration when used with non-volatile memory storage (CMOS with back-up power) of the digital error. A circuit which accomplishes this is shown in Figure 11.

Whatever the number of digits of the BCD DAC, the basic converter and reference voltage drift is assumed to be less than two full LSDs. Thus when a Lab Standard that gives an output of 1 X 10^n digits (10,000 for a 4 digit, or 4 plus a fractional digit ADC) is applied to the input, the error code can be loaded into the dual digit CMOS latches and will supply the proper correction voltage when the calibration button is released. The error (because this is a non-linear correction technique) is less than 1 LSB over the full 100 count range (the non-linearity is 1% of the error). This can be seen from the equation for the reference correction voltage ΔV_R.

$$\Delta V_R = \%\ \text{Error} \times V_R - \%\ \text{Error} \times \Delta V_R$$

By assuming that both the error and V_R corrections are small (1% error and 1% correction), the equation reduces to:

$$\Delta V_R = \%\ \text{Error} \times V_R$$

and the D/A converter can "multiply" the A/D reference voltage by the stored error term to provide the proper display correction voltage.

Since the D/A correction is for only the last two digits, its inherent drift is reduced by the ratio of the DAC and ADC codes (i.e. 100/10,000 = 1/100 for a 4-1/2 digit converter; 1/10 for a 3-1/2 digit system). The auto-calibration system shown in Figure 12 uses the lowest grade version of the DAC-20 (the DAC-20CQ) and yet only a maximum tempco of 0.8ppp/°C is contributed to a 4-1/2 digit ADC.

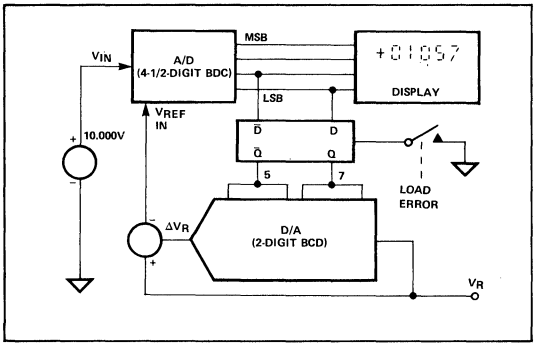


Figure 11. Auto-Calibrate Diagram

RESISTANCE MEASUREMENT

If the basic digital panel meter is expanded into a digital multimeter, additional opportunities arise for the use of BCD DACs. One such application is the adding of a current source output for resistive measurements.

The DAC-20 is especially attractive as a choice for the current source in a digital multimeter for several reasons including 0.25% bit matching, −10V to +18V output compliance, low temperature coefficient of 50 ppm/°C and low cost.

Even with discrete designs, the performance provided by the DAC-20 is not easily obtained.

An important feature provided by the DAC-20 in this application is that the current can be reduced by a factor of 10X

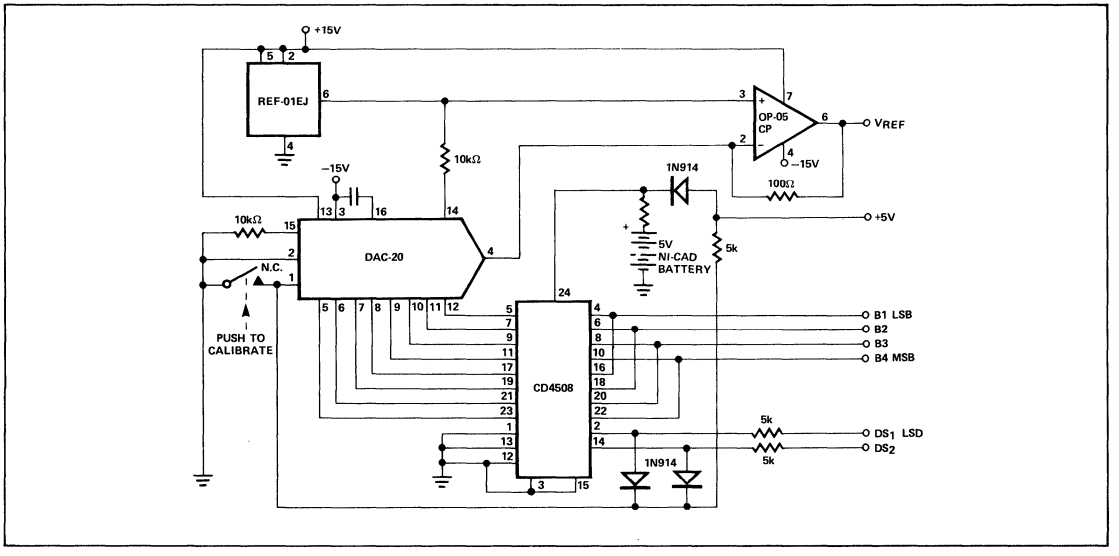


Figure 12. DVM Auto-Calibrate Circuit

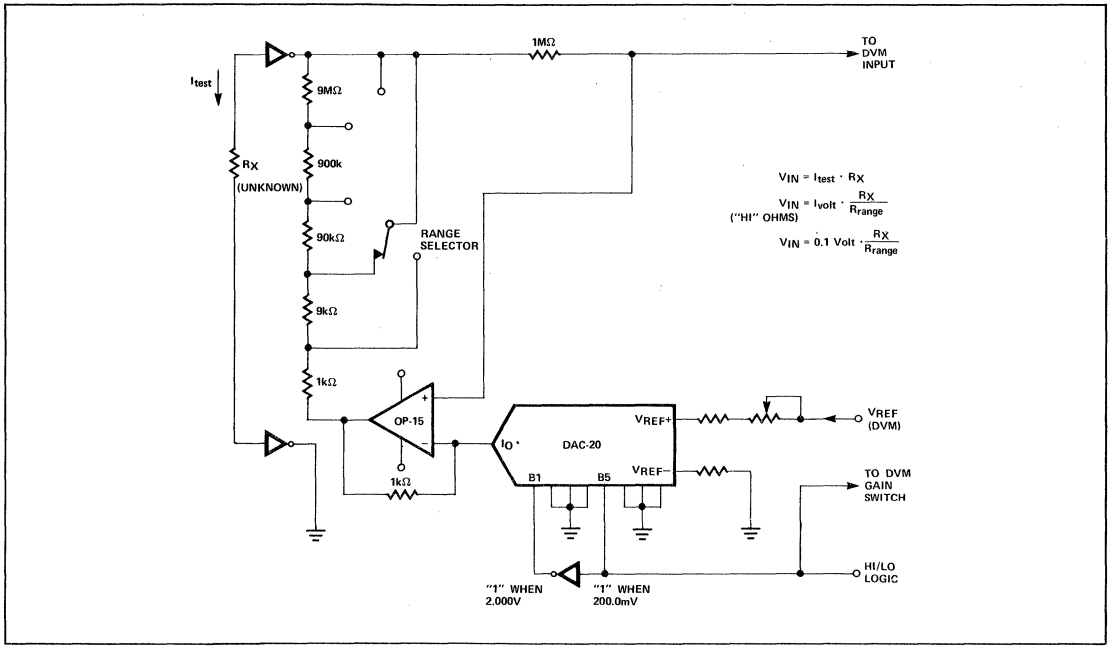


Figure 13. Hi-Lo Resistance-to-Voltage Converter

under logic control thereby allowing Hi-Lo resistance measurement by either gain switching the ADC (X10) to compensate for the current change or moving the decimal point. The Hi-Lo resistance measurement feature allows the user to measure resistance with and without forward biasing PN junctions (Hi and Lo ohms respectively).

The resistance measurement circuit shown in Figure 13 works with a basic DVM by providing resistance-to-voltage conversion with a programmable current source. This configuration uses the input range switching ladder network to program the current output (the output current = 1 Volt/ R_{range}).

AUTO-CALIBRATING RESISTANCE MEASUREMENT

A further refinement, possible for this or any DMM ohms measuring circuit using the floating current source configuration shown is to add a self-calibrating circuit with a BCD DAC. Basically this circuit would function in a manner similar to the DVM auto-calibration circuit previously discussed except that the sense of correction would be reversed (i.e. $\overline{I_O}$ instead of I_O used). This occurs because an increase in V_{REF} will decrease the DPM reading while an increase in the test current will increase the voltage across the unknown resistor thus increase the reading. As with the DVM auto-calibration circuits described in this note, calibration requires standard resistance that is a power of 10 (i.e. 1.0000k ohms) so that the stored correction term (error) is a decimally related error. As shown in Figure 14, the correction term is in a 100:1 ratio with the initial current setting source. Thus the tempco of the automatic resistance calibration circuit contributes only 0.50ppm/° C to the total system tempco. Unlike the reference auto-calibration circuit, this calibration circuit has no inherent non linearity.

PUTTING IT ALL TOGETHER

Combining the auto-calibrating voltage and resistance measuring circuits with the auto-nulling circuit leads to a powerful DVM that eliminates the need for normal calibration procedures. A reference standard can simply be sent to the instrument for calibration. In fact, a special "calibration standard" connector could be used to activate the auto-calibration features only when the "standard" is plugged into the instrument. This would eliminate the potential for calibration erasure. Figure 15 shows the complete intelligent DVM schematic including the full-range analog meter complement. The features of this instrument are:

1. Auto-nulling for ±50 LSBs.
2. Auto-calibration corrects for drifts up to ±50 LSBs in basic voltage ranges.
3. Hi-Lo resistance measurement with low drift.
4. Auto-calibration for resistance measurements up to ±50 LSBs.
5. Analog meter for trend display.

CONCLUSION

BCD DACs can provide convenience, flexibility and intelligence to BCD-based instruments such as Digital Multimeters without the added expense of software development.

As a decimally programmable current or voltage source, BCD DACs provide an important interface in bridging the gap between the use of digital instrumentation and the need for analog data, error correction and controls.

The use of the BCD DAC will grow in popularity in applications where binary-coded-decimal code is used at the man-machine interface and in systems where BCD is used

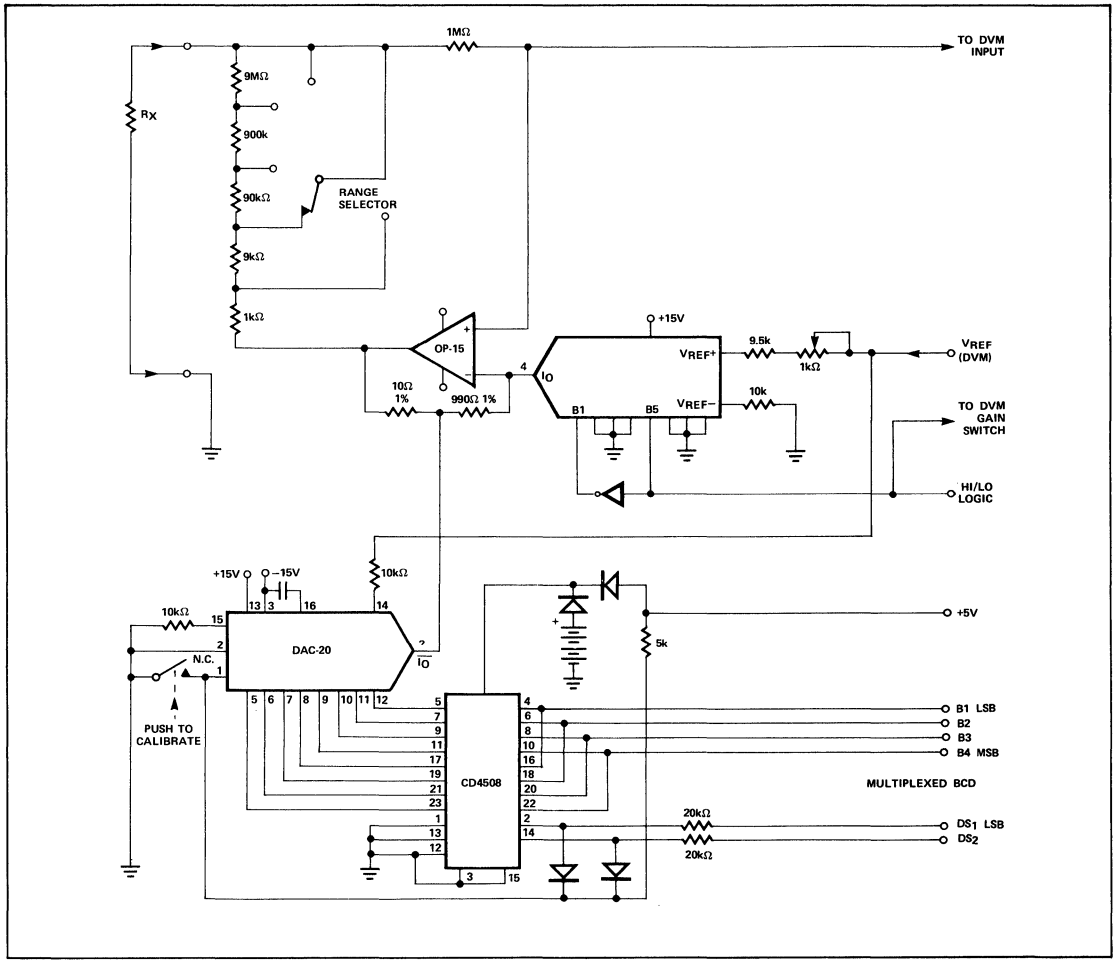


Figure 14. Auto-Calibrate Resistance Measurement

throughout. The convenience, flexibility and intelligence that BCD DACs provide BCD-based instruments such as digital multimeters will spread to other applications.

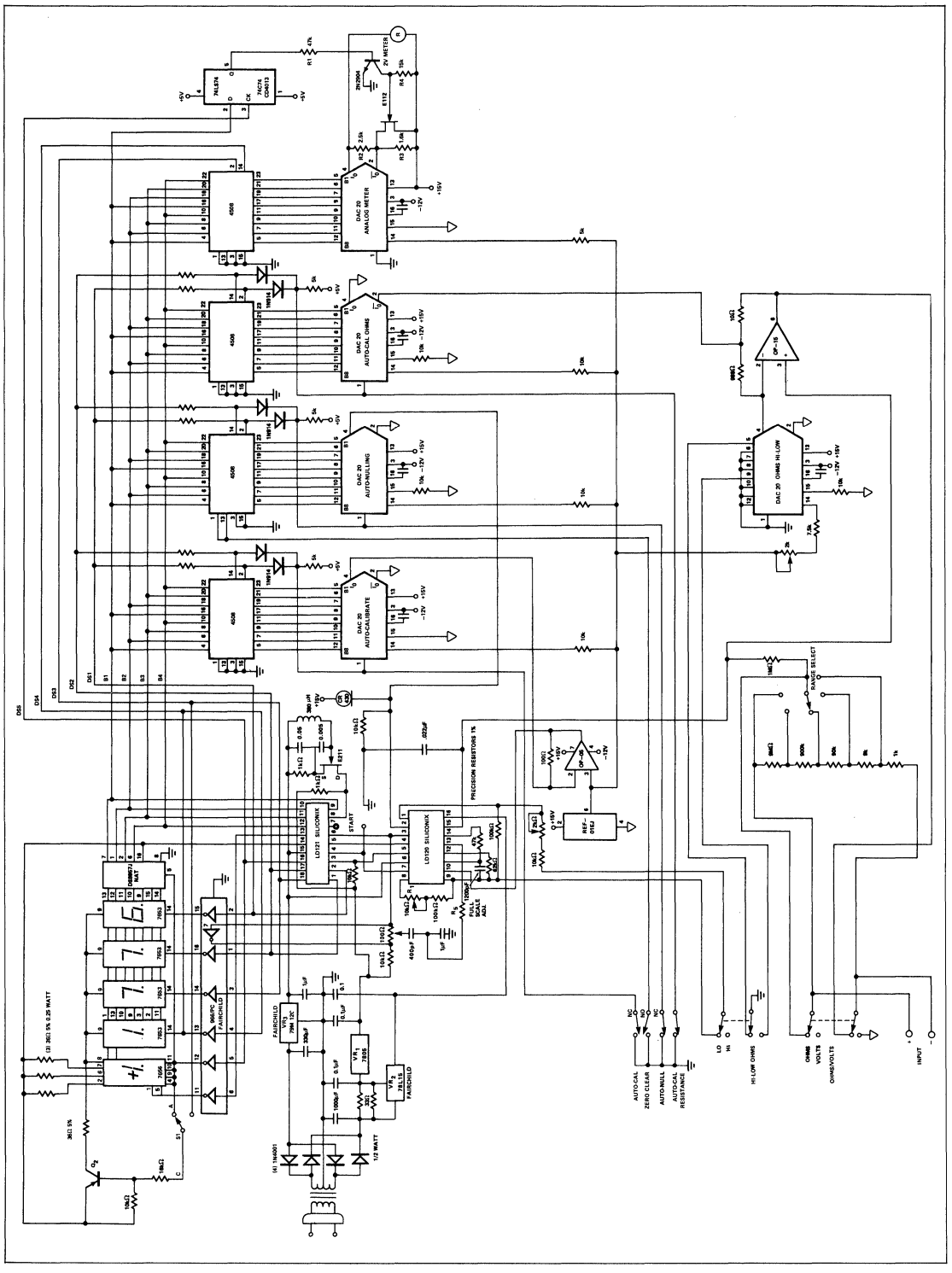


Figure 15. Complete Smart DMM

APPLICATION NOTE 35
UNDERSTANDING CROSSTALK IN ANALOG MULTIPLEXERS

by Shelby D. Givens

INTRODUCTION

One of the most troublesome errors in analog multiplexers is crosstalk. Various schemes have been devised to reduce its effects. One designer will terminate the multiplexer in a 10kΩ resistive impedance. Another will short the multiplexer node to ground between address changes with an analog switch. A third engineer will terminate the multiplexer node in 1MΩ because he doesn't want to live with the attenuation which comes about with any lower impedance. What is confounding about these three situations is that the solution is correct in each case. THE CORRECT SOLUTION IS DICTATED BY THE APPLICATION.

To understand why the solution is application dependent, it is necessary to dig rather deeply into what crosstalk really is. When this is done, crosstalk is found to have not one, but three components in a multiplexer. To differentiate the components one from the other, it is convenient to give them names:

1. Static crosstalk (CT)
2. Dynamic crosstalk (DCT)
3. Adjacent Channel crosstalk (ACCT)

This application note explains the three crosstalk components qualitatively and quantitatively. The qualitative discussion tells what component(s) should be considered in various applications. The quantitative discussion uses both theoretical and empirical information to arrive at conclusions about what performance should be expected.

STATIC CROSSTALK (CT)

To introduce the concept of crosstalk, Figure 1 will be helpful. A multiplexer is made up of several analog switches connected as shown in Figure 1c. The basic analog switch may be constructed of a FET (JFET or CMOS) and a suitable driver which switches it OFF and ON. This is shown in Figure 1a. The equivalent circuit of an analog switch is shown in Figure 1b. When the ideal switch (SW) is closed the switch has an ON resistance R_{ON}, and when SW is open, the OFF impedance is determined by C_{EQ}. The two channel multiplexer shown in Figure 1c shows how signals from one channel can be coupled into the other channel. Theoretically, V_{OUT} should consist of e_1 modified by the resistor divider formed by R_{ON1} and R_L (assumes reactance of C_L is $\gg R_L$). However the capacitance of switch number two (C_{EQ2}) does couple some portion of e_2 into V_{OUT}. This is the simplest example of crosstalk.

The model which explains static crosstalk is relatively simple and may be derived from the OFF isolation model. Figure 2a shows the OFF isolation model as capacitive coupling from the input to the output of an OFF switch. This condition may be duplicated in Figure 1c by opening SW_1 and setting $e_2 = 0$. Coupling from input to output is accomplished through C_{EQ},

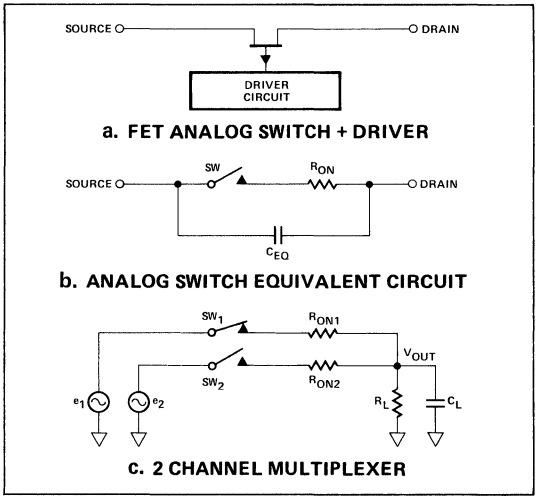


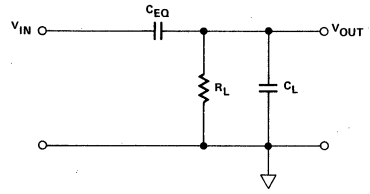
Figure 1. Essentials of an Analog Multiplexer

and this parameter may be computed from measurements of V_{IN}, V_{OUT}, and frequency. In the case of static crosstalk, C_{EQ} is shown coupling into a parallel combination of R_{ON} with R_L and C_L (Figure 2b). The two channel multiplexer shown in Figure 1c reduces to the circuit in Figure 2b, where $e_1 = 0$, $e_2 = V_{IN}$, and C_{EQ} is the coupling capacitance from e_2 to V_{OUT}.

Since R_L is generally 10kΩ or more, and typical analog switches are less than 1kΩ, static crosstalk is much smaller than OFF isolation. The crosstalk and OFF isolation numbers quoted on analog multiplexer data sheets are derived from the models shown in Figure 2. Unfortunately the one componet of crosstalk specified is the least troublesome of the three. However the crosstalk figures on data sheets will alert the designer to those devices which absolutely will not satisfy his requirements.

There are applications where the static crosstalk specification given on data sheets is adequate. When the multiplexer is being used as a one-of-many switch, and is not being cycled through all channels on an automatic basis, then the static crosstalk component will give accurate prediction of the actual performance. Examples of such applications are:

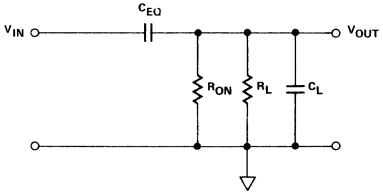
1. Audio/Video Selector Switch
2. Programmable Gain Amplifier
3. Programmable Power Supply



a. OFF ISOLATION EQUIVALENT CIRCUIT

"OFF" ISOLATION (ISO_{OFF})

The proportionate amount of a high frequency analog input signal which is coupled through the channel of an "OFF" device. This feedthrough is transmitted through $C_{DS(OFF)}$ to a load comprised of $C_{D(OFF)}$ in parallel with an external load. Isolation generally decreases by 6dB/octave with increasing frequency.



b. STATIC CROSSTALK EQUIVALENT CIRCUIT

CROSSTALK (CT)

The proportionate amount of cross-coupling from an "OFF" analog input channel to the output of another "ON" output channel.

Figure 2. Model for Static Crosstalk

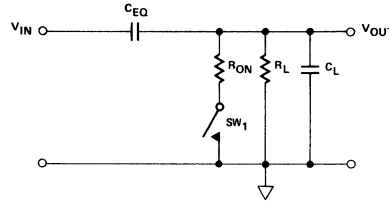
DYNAMIC CROSSTALK (DCT)

The dynamic crosstalk model can be derived from Figure 3. The switch SW_1 represents one condition on the multiplexer node (SW_1 is open). Actually SW_1 is continually switching between OFF and ON. This is represented in Figure 3b. In order to reduce crosstalk, multiplexers are designed to have break-before-make switching so that no two channels are addressed at the same time. The finite open time of SW_1 (shown in Figure 3b) represents the break-before-make action. There are two "open" conditions on the multiplexer node per cycle of the clock; thus the equivalent nodal resistance (R_{EQ}) may be computed as given in Figure 3b. Table I shows some typical values of static and dynamic crosstalk. Static crosstalk values are given in lines 1 and 12. There is a change in crosstalk as the clock frequency (f_{CLK}) is varied. Starting at line 4 notice the variation in crosstalk as R_L is varied from 10kΩ to 100kΩ while f_{CLK} remains constant at 100kHz. While Table I yields some theoretical values which give insight into the operation of dynamic crosstalk, a working multiplexer will have different values of f_{CLK} with respect to the maximum value of f_{SIG}. The real world situation will be analyzed in a later section of this paper.

Examples of multiplexer applications which are dynamic in nature are:

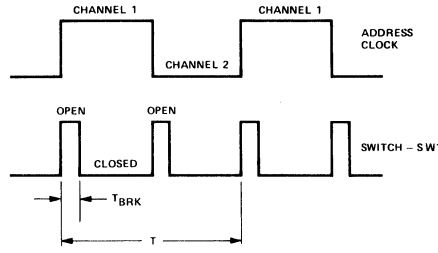
1. Industrial Process Control
2. Telephony
3. Data Acquisition Systems
4. Telemetry

Each one of the above applications are a form of Time Division Multiplexing. In other words, these are sampled-data



a. DYNAMIC CROSSTALK EQUIVALENT CIRCUIT

NOTE: SWI is a time dependent switch. Its characteristic is shown in Figure 3b.



b.

$T \equiv$ Period of address clock

$T_{BRK} \equiv$ Break-Before-Make Time

$$\text{If } R_L \gg R_{ON},\ R_{EQ} \cong \frac{R_{ON}(T - 2T_{BRK}) + 2R_L T_{BRK}}{T}$$

Figure 3. Model for Dynamic Crosstalk

Table 1. Computed Values of Static and Dynamic Crosstalk

LINE NO.	f_{SIG} Hz	f_{CLK} Hz	T μsec	T_{BRK} μsec	R_{ON} OHMS	R_L OHMS	R_{EQ} OHMS	C_{EQ} pF	CROSS-TALK dB
1	10K	0	—	0.80	300	10K	291	0.30	105
2	10K	20K	50	0.80	300	10K	602	0.30	99
3	10K	40K	25	0.80	300	10K	913	0.30	95
4	10K	100K	10	0.80	300	10K	1845	0.30	89
5	10K	100K	10	0.80	300	20K	3448	0.30	84
6	10K	100K	10	0.80	300	40K	6650	0.30	78
7	10K	100K	10	0.80	300	100K	16.25K	0.30	70
8	20K	50K	20	0.80	300	10K	1068	0.30	88
9	20K	50K	20	0.80	300	20K	1872	0.30	83
10	20K	50K	20	0.80	300	40K	3474	0.30	78
11	20K	50K	20	0.80	300	100K	8275	0.30	70
12	20K	0	—	0.80	300	100K	291	0.30	99

systems where each channel is being continuously sampled and the information for a given channel is contained in a given time slot. In these applications, the static crosstalk is almost meaningless, since the wrong choice of R_L (or f_{CLK}) can be disastrous.

ADJACENT CHANNEL CROSSTALK (ACCT)

Adjacent channel crosstalk is the most confusing component of crosstalk. In addition to its confusing nature, in some cases, it is the most dominant component. While both static and dynamic crosstalk are capacitive in nature, i.e., they vary with frequency at 6dB/octave, the adjacent channel crosstalk is **invariant with frequency**. In other words, it is possible to have crosstalk **when multiplexing DC signals** such as the outputs of thermocouples, pressure transducers, etc. The parameters which must be dealt with are R_L, C_L, R_{ON}, and f_{CLK}. In addition, the break-before-make time ($=T_{BRK}$) of the multiplexer is of importance. Before diving into the details of this component of crosstalk, it will be helpful to define what is meant by ACCT.

The term "adjacent" refers to time only. In other words, channel two is adjacent to channel one if channel two **immediately** follows channel one in time slots. Since the channel following is the "adjacent" channel, then channel one is not adjacent to channel two, but rather the other way around. Figure 4 illustrates the concept of adjacent channels. Assuming the multiplexer had, say, 1V on channel one, 2V on channel two, etc., then the output would look like the curve labeled "channel addressed." What is important about the waveforms in Figure 4 is the way the adjacent channel (in time) is shown. Note that while channel two is adjacent to channel one, channel one is itself adjacent to channel eight.

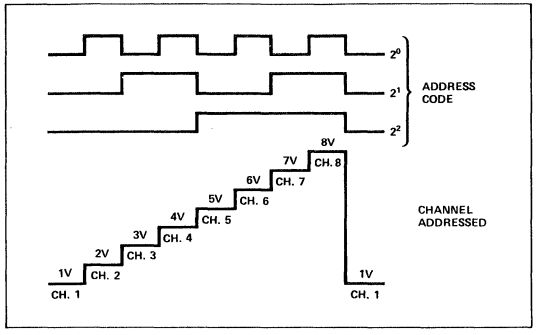


Figure 4. Adjacent Channel Concept

The fact that information is "carried forward" from one channel to the next (in time) suggests a storage mechanism as causing ACCT. Thus the multiplexer nodal capacitance becomes the prime suspect. Figure 5 illustrates how information is carried forward from one channel to the next as the addresses are changed. The address code is shown in Figure 5a, while Figure 5b shows the theoretical multiplexer output. Note that the even numbered channels have zero volts on them, while the odd channels have their channel number in volts. This arrangement best illustrates how the information is transferred to the adjacent channel (as

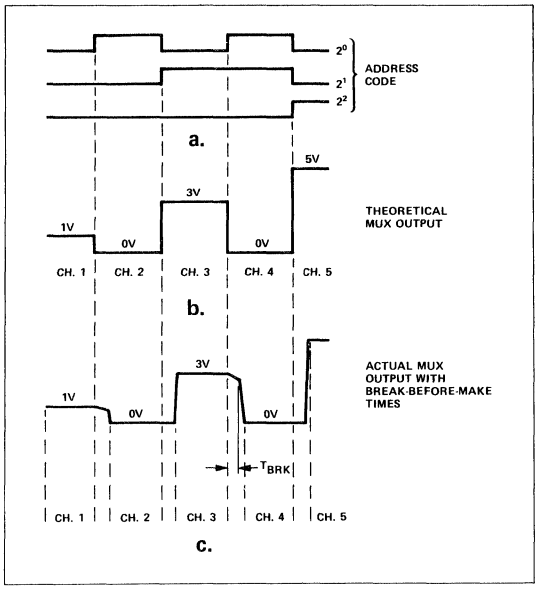


Figure 5. Adjacent Channel Crosstalk

shown in Figure 5c). While the theoretical MUX output switches from channel three (3 volts) to channel four (0 volts) at the moment of the address change, note the delay in the actual MUX output caused by T_{BRK}. During this time the MUX node discharges along an RC curve determined by the load capacitance (C_L), and the load resistance (R_L). When the break-before-make time (T_{BRK}) is over, channel four is turned ON and the RC product is suddenly reduced to $R_{ON}C_L$. A curve which details how this all takes place is shown in Figure 6. Before leaving Figure 5, the arrangement suggests a method of avoiding adjacent channel crosstalk. In other words, the alternate grounding of channels prevents channel one signals from reaching channel three... channel three from reaching channel five, etc.

The curve in Figure 6a shows a typical nodal discharge for a set of real world conditions. The curve is normalized and T_{BRK} is chosen to be 900nsec. An accepted method of measuring T_{BRK} is from the 50% point of the channel which has been turned OFF to the 50% point of the channel which is being turned ON. This concept is illustrated in Figure 6b. In this case (Figure 6a) T_{BRK} is measured from the moment of the address change. While this is not totally correct, the agreement between theoretical and actual results is good enough to justify the simpler model which is derived. Since most designers are interested in crosstalk which is less than the resolution of the discharge curve, the ACCT vs. time graph gives crosstalk down to 90dB. In other words, the ACCT is down 90dB in less than 1.25μsec.

Adjacent channel crosstalk is a problem in every application where dynamic crosstalk must be considered; however there are techniques to minimize its effects. A popular way to diminish adjacent channel crosstalk is to short the multiplexer node to ground between address changes. This requires an additional analog switch which should be fast

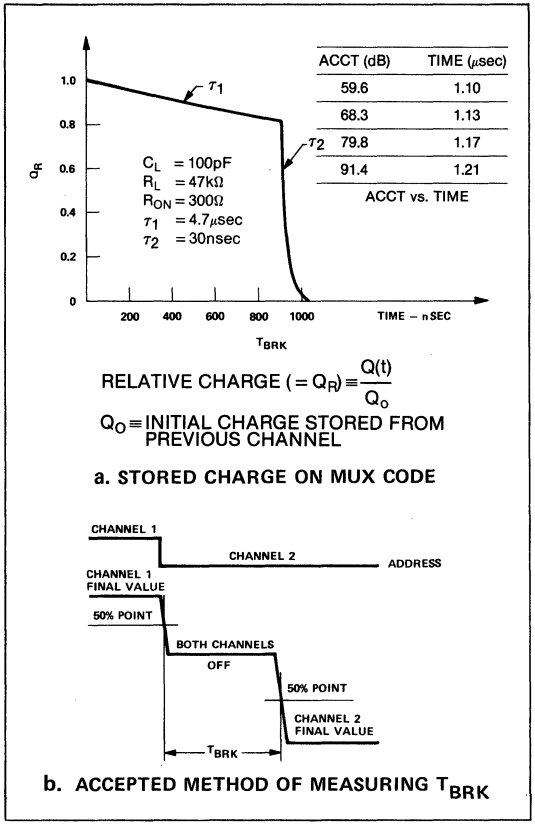


Figure 6. Stored Charge Decay and Definition of T_{BRK}

and have low R_{ON}. An alternative approach to reducing adjacent channel crosstalk is to ground every other channel in a multiplexer. This technique was illustrated in Figure 5.

MEASUREMENT OF STATIC CROSSTALK

Figures 7 and 8 give the element values for a typical PMI BIFET MUX-08 on channel three. In the case shown, the OFF isolation was first measured and found to be 75dB. With R_L and f_{SIG} known, then C_{EQ} was calculated. Once C_{EQ} is known, then R_{EQ} may be calculated from the static crosstalk measurement made in Figure 8. R_{EQ} is the parallel combination of R_L and R_{ON}; thus it is possible to compute R_{ON} and this value is also shown in Figure 8. The measurements thus far are relatively simple and only require a voltmeter which is capable of measuring signals which are 100dB below the reference signal. On the other hand, the measurement of dynamic crosstalk is a bit more involved, and requires a more complex system.

MEASUREMENT OF DYNAMIC CROSSTALK

The crosstalk measuring system shown in Figure 9 is to be used for measuring dynamic crosstalk. The signal from M_5 is fed into M_1 where it is multiplexed onto the OUT terminal.

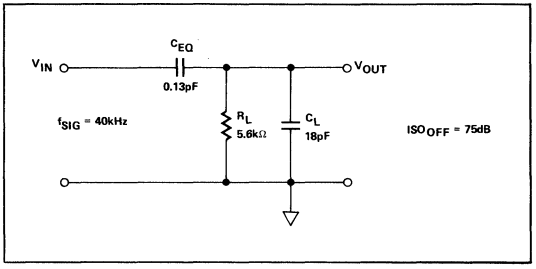


Figure 7. Typical OFF Isolation Element Values

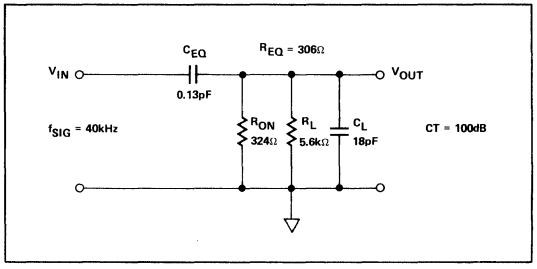


Figure 8. Typical Static Crosstalk Element Values

M_1 contains the multiplexer under test and a decoding circuit. The decoding circuit allows the selection of any two channels to be used as a two channel multiplexer. M_2 is a high-speed buffer used for driving the IN terminal of M_3. M_3 contains a multiplexer operated in a demultiplexer mode, along with decoding circuitry to allow several combinations of two channel demultiplexing. The signal which appears on S_{3A} is fed through M_4 (high-speed buffer) to M_8 for spectrum analysis. In short, if no errors are introduced by the multiplexer-demultiplexer system, the output should be the same as the input.

Since the system in Figure 9 is capable of measuring dynamic crosstalk, a good check of its performance is to repeat the static crosstalk measurements. M_3 is set to have IN connected to S_{3A} at all times. M_1 is set to have S_3 connected to OUT, and the signal thus measured is taken as the reference signal. Static crosstalk is measured by connecting S_1 (or S_8) to OUT, with V_{IN} still applied to S_3, and again measuring V_{OUT}. The relative signal levels represent static crosstalk. This measuring technique was used to verify the accuracy of the system.

The measurement of dynamic crosstalk leaves M_3 exactly as in the static case. With V_{IN} connected to S_3, M_1 is switched between S_1 and S_8. The signal frequency (f_{SIG}) was 40kHz and f_{CLK} was 100kHz (see Figure 10). From the crosstalk measured, the equivalent resistance (R_{EQ}) is computed to be 1150Ω (see Figure 10a). To verify the validity of this measurement, R_{EQ} was calculated using the formula in Figure 10c (T_{BRK} was measured separately). Since there is very good agreement between these two independently derived values, both the measurement technique and the dynamic crosstalk model are valid.

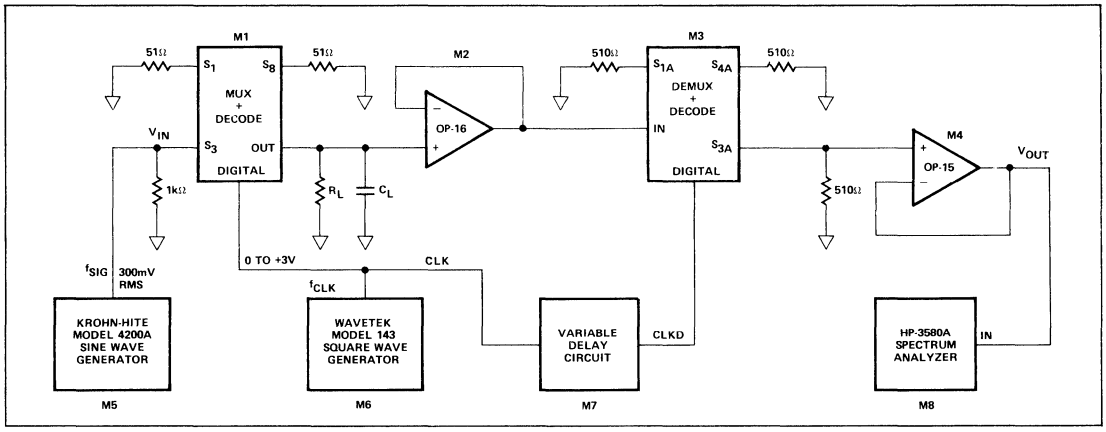
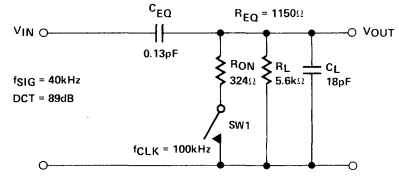


Figure 9. Dynamic Crosstalk Measuring System



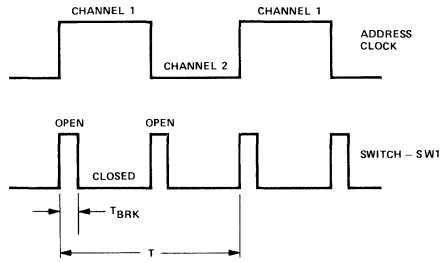
NOTE: SWI is a time dependent switch. Its characteristic is shown in Figure 10c.

a. TYPICAL DYNAMIC CROSSTALK ELEMENT VALUES

SYSTEM DYNAMIC CROSSTALK

f_{SIG}	f_{CLK}	R_L	R_{EQ}	DCT (C_{EQ} = 0.13pF)	DCT (C_{EQ} = 0.5pF)
Hz	HZ	Ω	Ω	dB	dB
10K	100K	10K	1718	97.1	85.4
10K	100K	22K	3463	91.0	79.3
10K	100K	33K	5059	87.7	76.0
10K	100K	47K	7090	84.7	73.0
10K	100K	100K	14.78K	78.4	66.7

b.



$T = 5\mu sec$

$T_{BRK} = 725nsec$

$R_{EQ} = 1089\Omega$

$T \equiv$ Period of Address Clock

$T_{BRK} \equiv$ Break-Before-Make Time

If $R_L \gg R_{ON}$, $R_{EQ} \cong \frac{R_{ON}(T - 2T_{BRK}(+ 2R_L T_{BRK})}{T}$

c.

Figure 10. Computed Dynamic Crosstalk for Actual Multiplexer

The numbers shown in Figure 10 apply to the measurement system, but are unlikely in a real multiplexer. To satisfy sampling theory limitations, f_{SIG} must be less than one-half the sampling frequency. Assuming $f_{CLK} = 200kHz$ then each channel in a multiplexer is addressed for 5μsec. This means that it takes 40μsec to sample all channels of an eight channel multiplexer. In other words, **each channel** is sampled at a 25kHz rate. Thus the maximum value of f_{SIG} would be 12.5kHz. Figure 10b gives values of dynamic crosstalk (DCT) which would be experienced if the values of R_{ON} and T_{BRK} shown in Figures 10a and 10b were used. The first DCT column lists the values for a C_{EQ} of 0.13pF (measured value of channel three). The second DCT column shows the performance for $C_{EQ} = 0.5pF$. The purpose for the second column is to point out how critical minimizing stray capacitance is to good crosstalk performance.

MEASUREMENT OF ADJACENT CHANNEL CROSSTALK

The system shown in Figure 11 was used to measure adjacent channel crosstalk (ACCT). M_1 drives the address lines of the MUX system and the gating input of M_4. By setting the period of M_4 (T_2) to 10μsec, the pulse rate out of M_4 is controlled by the pulse rate of M_1 (40μsec) coming into the gate input of M_4. The output of M_4 is in the complement mode

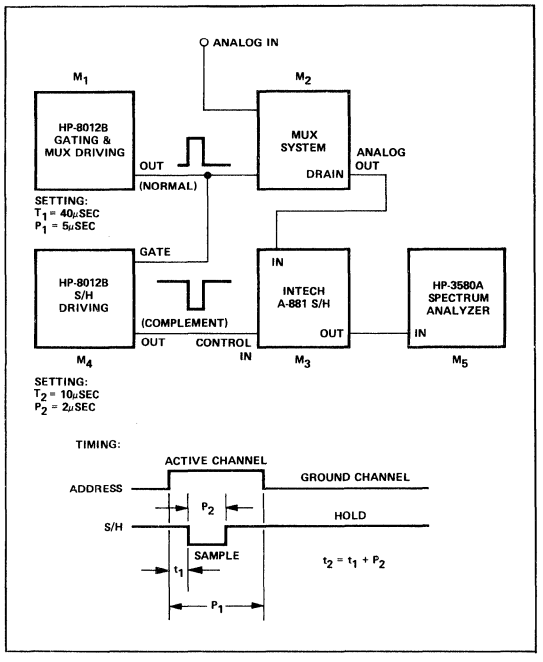
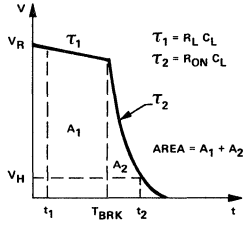


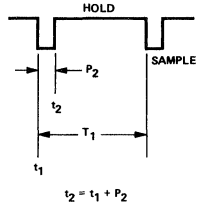
Figure 11. Adjacent Channel Crosstalk Measuring System

because the control input to M_3 causes the S/H to HOLD when the input is high (1). Thus the sample period occurs during the time P_2. M_4 also can delay its pulse relative to the pulse out of M_1, thereby allowing measurements of crosstalk versus t_1 (start of the sample time). This information is valuable because in many systems, a sample/hold is used with a successive approximation ADC to encode the analog output of the MUX. As will be shown, the ACCT can be made negligible if a sufficient time elapses before going to the HOLD mode for encoding the data. Since "time is money," the term "sufficient time" becomes important.

The nature of sample/holds and the nature of spectrum analyzers can cause some apparent discrepancies in the data observed by this measurement system. It is important to note the spectrum analyzer "sees" the average of **everything** that is presented to its input terminals. While it is true the sample/hold holds the last value it "saw," the spectrum analyzer also looks at the signal present during the sample/hold's sample time. Thus the equation which expresses the signal level present as a function of time must also account for the true averaging of the spectrum analyzer. Figure 12 shows the equations (12c) and the definitions of the terms used in the equations (12a and 12b). The term N_O is the **relative** signal level which the spectrum analyzer measures. If the model of the signal decay shown in Figure 12a is the correct one to explain the ACCT, then the computed value of N_O should correspond to the measured values. As will be shown in Figure 14, the agreement does in fact justify the model; however it was necessary to choose the measurement conditions **very carefully.**



a. VOLTAGE DECAY ON MUX OUTPUT



b. SAMPLE/HOLD

EQUATIONS:

1. $$\frac{V_O}{V_R} \equiv N_O = \frac{N_H(T_1 - P_2) + S_1 + S_2}{T_1}\text{; Where}$$

2. $$\frac{V_H}{V_R} \equiv N_H = EXP\left[\frac{-t}{\tau_1}\right],\ t \le T_{BRK}$$

$$= EXP\left[\frac{-T_{BRK}}{\tau_1}\right] EXP\left[\frac{T_{BRK} - t}{\tau_2}\right],\ t \ge T_{BRK}$$

3. $$\frac{A_1}{V_R} \equiv S_1 = \tau_1\left[EXP\left(\frac{-t_1}{\tau_1}\right) - EXP\left(\frac{-T_{BRK}}{\tau_1}\right)\right]$$

4. $$\frac{A_2}{V_R} \equiv S_2 = \tau_2\, EXP\left[\frac{-T_{BRK}}{\tau_1}\right]\left[1 - EXP\left(\frac{T_{BRK} - t_2}{\tau_2}\right)\right]$$

c.

Figure 12. Predicting the Measurement System Response

In order to get good correlation between lab data and theoretical predictions, it was necessary to use fairly long time constants ($R_L = 22k\Omega$ and $C_L = 1000pF$). With $R_L = 22k\Omega$ and $C_L = 50pF$ ($R_{ON} = 300\Omega$), the theoretical plot of ACCT (as measured on the spectrum analyzer) vs. t_1 is shown in Figure 13. Note that the data is plotted between 900nsec and 1025nsec. The curve shows that a **10nsec error in t_1 can cause a 6dB error** in reading on the spectrum analyzer. The results shown in Figure 14 confirm the necessity of using large capacitances to obtain predictable results. The theoretical curve tracks the actual data well in both cases; however the 1000pF curve is better than the 300pF curve. Notice that there is good agreement both at DC and at 4kHz.

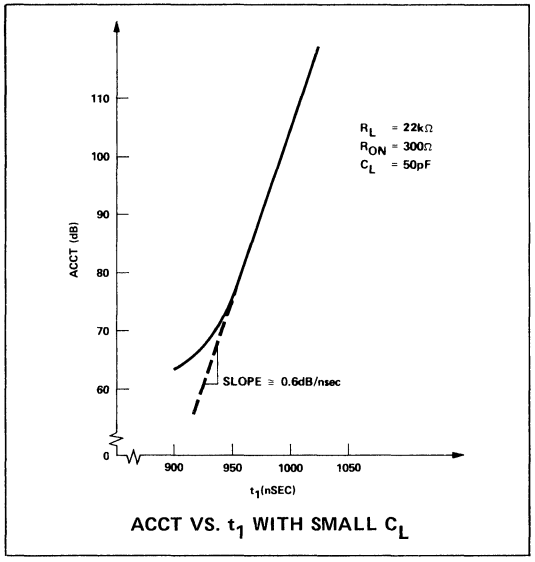


Figure 13. Measurement Errors Due To Small C_L

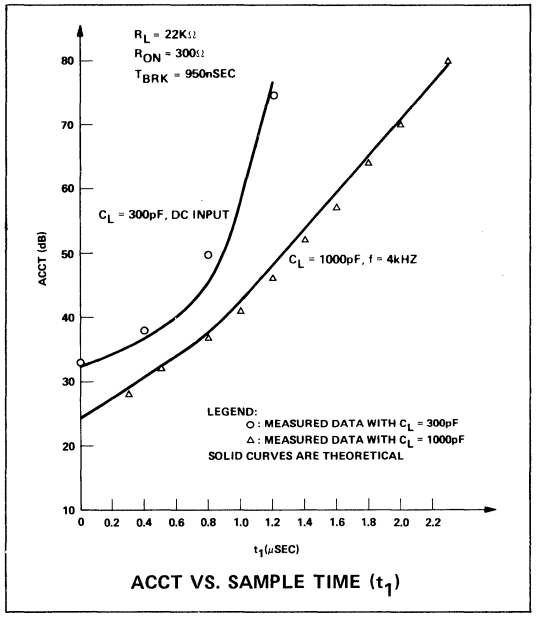


Figure 14. Agreement Between Measured and Computed ACCT

PREDICTING AND CONTROLLING ADJACENT CHANNEL CROSSTALK

The equations in Figure 12c can be used to predict how much adjacent channel crosstalk one might expect in an actual system. An all analog system will follow the MUX with a

A. Multiplexer-Demultiplexer System:

$N_H \equiv 0$ Therefore

1. $N_O = \frac{S_1 + S_2}{T_1}$, Where $T_1 = \frac{1}{f_{CLK}}$ x (No. of Channels)

2. $S_1 = \tau_1 \left[EXP\left(\frac{-t_1}{\tau_1}\right) - EXP\left(\frac{-T_{BRK}}{\tau_1}\right) \right]$

3. $S_2 = \tau_2 \ EXP\left[\frac{T_{BRK}}{\tau_1}\right]\left[1 - EXP\left(\frac{T_{BRK} - t_2}{\tau_2}\right)\right]$

Where $t_1 = T_D$ (Break-Before-Make Time of DEMUX)

$$t_2 = \frac{1}{f_{CLK}} - T_D$$

B. Multiplexer — Sample/Hold System

$S_1 = S_2 = P_2 \equiv 0$

4. $N_O = N_H = EXP\left[\frac{-t}{\tau_1}\right]$ $t \leq T_{BRK}$

$$= EXP\left[\frac{-T_{BRK}}{\tau_1}\right] EXP\left[\frac{T_{BRK} - t}{\tau_2}\right], \ t \geq T_{BRK}$$

Where: $t = t_H$ (Hold Command for Sample/Hold as measured from Address Change Time)

Figure 15. Predicting Adjacent Channel Crosstalk

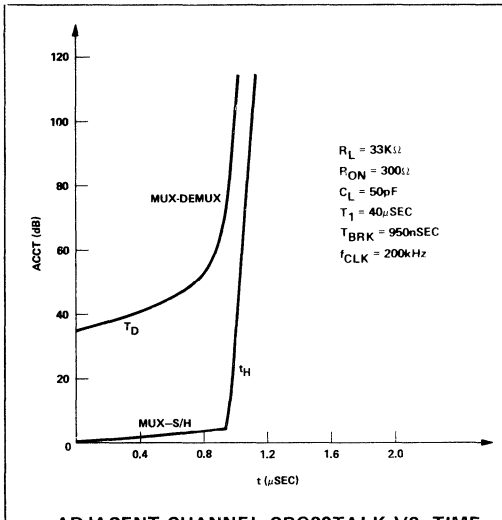


Figure 16. Computed ACCT vs Time for MUX-DEMUX and MUX-S/H Systems

demultiplexer, which will have its own break-before-make delay. An analog to digital system will have a sample/hold amplifier in front of the A/D converter. Since the equations which apply to these situations are different, they will be discussed separately. Figure 15 summarizes the conditions and the equations which apply to them.

Since there is no held voltage, then $N_H = 0$ in the multiplexer-demultiplexer system. This reduces N_O to the simple form shown in equation (1). S_1 and S_2 follow in equations (2) and (3). Since $t_1 = T_D$ (break-before-make time of the DEMUX), that time will have a significant effect on ACCT. The MUX-sample/hold system imposes the condition $S_1 = S_2 = P_2 = 0$; thus $N_O = N_H$. It will be instructive to compare the levels of ACCT in these two systems versus their appropriate times.

Figure 16 looks at a "typical" system which will give approximately one percent transmission error (33kΩ R_L and 300Ω R_{ON}), and has 50pF C_L. The value of C_L is somewhat on the high side (20pF being typical for MUX-08 connected to a buffer amp), but it does give a conservative value for analysis. What Figure 16 shows is rather startling. The adjacent channel crosstalk, while inherent in the multiplexer itself, can be eliminated in **both** systems by the proper timing. In the case of the sample/hold it is only necessary to delay the hold command for approximately 1.2μsec to have the ACCT vanish completely. This is no problem, since most sample/holds need at least 2μsec to accurately acquire the signal (this is particularly true of monolithic devices). The plot for the MUX-DEMUX system relates to T_D, which is **not adjustable** for a given DEMUX. What is possible is to add some delay to the address change for the DEMUX. In this way, the DEMUX will not "look" at the MUX output until the charge from the previous channel has had a chance to dissipate.

CONCLUSION

Table II summarizes the forms of crosstalk and lists ways of coping with them. Reduction of R_{ON} is helpful in all three cases. While T_{BRK} should be minimized as much as possible, it is important that no two channels are ON at the same time. In some cases, T_{BRK} is chosen such that even over temperature extremes, the break-before-make feature is maintained. Since all three components of crosstalk are present in a dynamic multiplexer, the "careful circuit board layout" is important even though it is not listed in the ACCT section.

Table 2. How to Handle Crosstalk

Crosstalk Component	Variation with f_{SIG}	Ways to Minimize Effects
Static	**6dB/octave**	• **Minimize R_{ON}** • **Reduce stray capacitance (C_{EQ}) by careful circuit board layout.**
Dynamic	**6dB/octave**	• **Minimize R_{ON}** • **Minimize f_{CLK}** • **Minimize T_{BRK}, but $T_{BRK} > 0$ is needed to prevent shorting channels together.** • **Minimize R_L** • **Reduce stray capacitance (C_{EQ}) by careful circuit board layout.**
Adjacent Channel	**NONE**	• **Minimize R_{ON}** • **Minimize f_{CLK}** • **Minimize T_{BRK}, but $T_{BRK} > 0$ is needed to prevent shorting channels together.** • **Minimize R_L and C_L** • **WAIT before allowing sample/hold or DEMUX to measure MUX output.**

This paper has pointed out the fact that static crosstalk (given on multiplexer data sheets) is only **one** of the **three** components of crosstalk. The models for static and dynamic crosstalk are relatively simple and were discussed to show how they are related. The most troublesome component of crosstalk (adjacent channel crosstalk) was shown not to be quite so straight-forward. For one thing, adjacent channel crosstalk (ACCT) is **not signal frequency dependent** as are CT and DCT. The mechanism which governs this form of crosstalk is stored charge on the MUX node. While CT and DCT must be minimized by careful layout and once present in the multiplexer cannot be reduced, such is not the case with ACCT. Even though ACCT is present in the multiplexer, the proper timing of demultiplexer or sample/hold commands can effectively eliminate ACCT from the total system.

APPLICATION NOTE 36

DAC-08 CONTROL OF 555 TIMERS

by Kishor Patel

INTRODUCTION

This application note describes a digitally or microprocessor controlled one-shot and an astable multivibrator using two of the industry's most widely used low cost building blocks, the PMI DAC-08 8 bit DAC and the 555 timer. Digital control ranges of 255 to 1 and 510 to 1 are shown for one-shot and astable applications allowing periods of 18μsec to 1.4 seconds and frequencies of 1 Hz to 60 KHz.

ONE-SHOT LINEAR MODE OPERATION

In the one-shot mode of operation, the time delay or the one-shot period is determined by a constant current source and a capacitor. A digitally programmable constant current source is made using the DAC-08 and two PNP transistors. The DAC-08 is a current sink; the two PNP transistors are used as a current mirror which reverses the direction of the DAC's sink current forming a current source. The current source charges the timing capacitor, causing the voltage across the capacitor to increase linearly at the rate of $\left\{\frac{I_{OUT}}{C}\right\}$ volts per second from approximately zero volts to $\frac{2}{3} V_{CC}$ of the 555 timer.

The one-shot's period, T, is basically an RC product with two other control factors. The R is fixed and represented by R_{REF} which sets up the correct I_{REF} current for the DAC. With the fixed R_{REF}, the one-shot period is directly proportional to the value of the timing capacitor C (see Table 1). The other two controlling factors are the DAC's digital inputs and the ratio of the timer's V_{CC} to the DAC's V_{REF}. The one-shot period is inversely proportional to the normalized digital input value and directly proportional to the V_{CC} to V_{REF} ratio as illustrated in Fig. 2. When operated in the linear mode, a 255 to 1 control range of the one-shot's period is achieved.

BASIC DESIGN

As shown in Fig. 1, this design involves a series of conversions from a digital input to an analog current to a threshold voltage and finally to a time delay or a frequency. A DAC-08 converts the digital input to an analog current

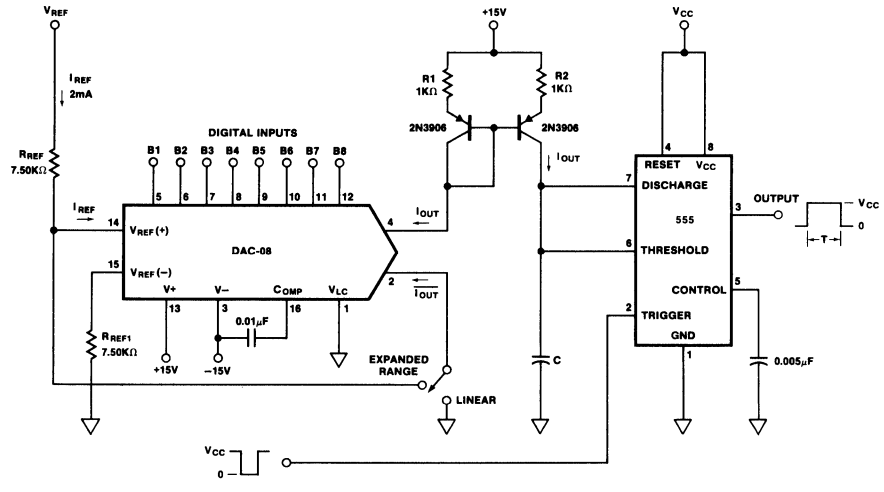


Figure 1. Digitally Controlled One-Shot

Table 1. One-Shot Linear Mode Timing Table

	ONE-SHOT PERIOD (msec)					
	V_{CC} = 15V V_{REF} = 15V			V_{CC} = 5V V_{REF} = 15V		
Input Digital Code	C = 1μF	C = 0.1μF	C = 0.01μF	C = 1μF	C = 0.1μF	C = 0.01μF
11 11 11 11	5.2	0.505	0.049	1.72	0.160	0.0176
00 00 00 01	1440	134	13.8	455	43	4.8

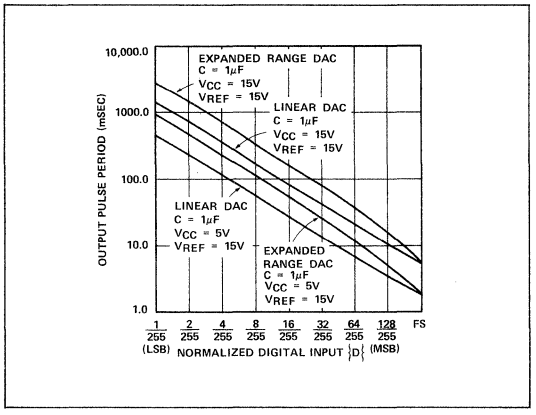


Figure 2. One-Shot Period vs Digital Input

which is then converted to a voltage by a two transistor current source and a capacitor. The voltage is then converted to a time delay or frequency by a timing capacitor and the 555 timer.

ONE-SHOT EXPANDED MODE OPERATION

Range is doubled to 510 to 1 by operating the DAC in the expanded range mode with the DAC's I_{OUT} fed forward from the reference input node of the DAC. Expanded range mode timing is shown in Table 2 and in the graph of Fig. 2.

ASTABLE MODE OPERATION

An astable multivibrator is made in a similar fashion in Fig. 3. A DAC-08 and two PNP's form a current source driving the timing capacitor (C) and a discharge resistor (R_B). The timing capacitor is charged linearly by the current source and discharged exponentially through R_B. Once again, the

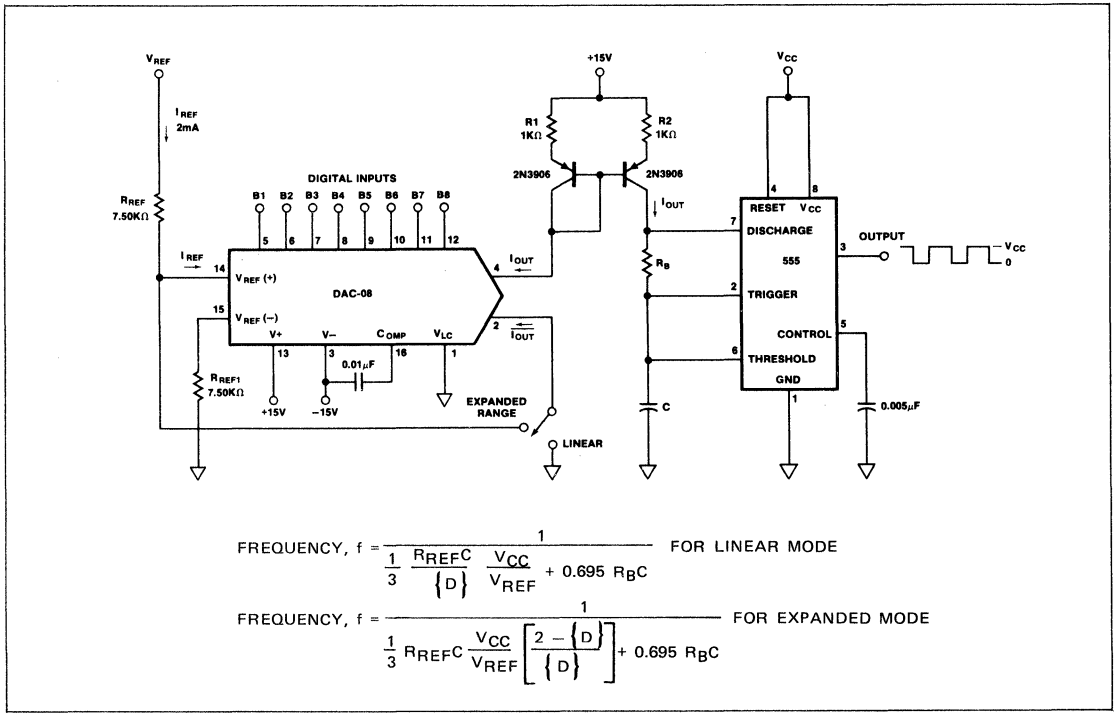


Figure 3. Digitally Controlled Astable Multivibrator

digital DAC input and the ratio of the timer V_{CC} to the DAC's V_{REF} provide additional control on the multivibrator's frequency. The digital input has directly proportional control while the V_{CC} to V_{REF} ratio has an inversely proportional control of frequency.

Frequency range is not fully 255 to 1 as expected but approximately 220 to 1, because the discharge time (output low) of a cycle is invariable for any digital input being determined by the product of R_B and C. Frequency is shown in Table 3 and in Fig. 4. Expanded range operation doubles frequency range as it did in the one-shot application. Frequency is shown in Table 4.

MICROPROCESSOR CONTROL

Both the one-shot and the astable multivibrator can be microprocessor controlled. Fig. 5 shows the implementation of a microprocessor controlled one-shot. The eight bit latch (74LS377) is used to interface between the data bus and the DAC. Stable data is latched in by a positive going edge of an address coincident pulse. After the data is latched, a buffered negative going address coincident pulse can be used to trigger the one-shot. The astable multivibrator is implimented similarly except for elimination of the buffer and the trigger pulses which are not required.

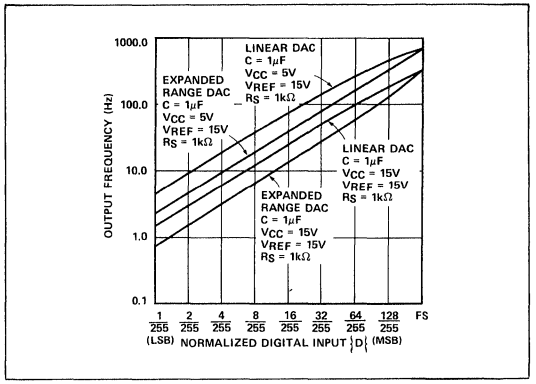


Figure 4. Multivibrator Frequency vs Digital Input

CONCLUSION

Digitally controlled one-shot and astable multivibrator with a wide range of outputs have been implemented. The one-shot has a 255 to 1 (8 Bit dynamic) time period range and the astable multivibrator a 220 to 1 frequency range. When the DAC is operated in the expanded modes, these ranges are doubled.

Table 2. One-Shot Expanded Mode Timing Table

	ONE-SHOT PERIOD (msec)					
	V_{CC} = 15V V_{REF} = 15V			V_{CC} = 5V V_{REF} = 15V		
Input Digital Code	C = 1μF	C = 0.1μF	C = 0.01μF	C = 1μF	C = 0.1μF	C = 0.01μF
11 11 11 11	5.2	0.495	0.049	1.72	0.160	0.0176
00 00 00 01	2900	280	26	970	87	8.4

Table 3. Astable Linear Mode Frequency Table

	ASTABLE MULTIVIBRATOR FREQUENCY (Hz)					
	R_B = 1kΩ; V_{CC} = 15V; V_{REF} = 15V			R_B = 1kΩ; V_{CC} = 5V; V_{REF} = 15V		
Input Digital Code	C = 1μF	C = 0.1μF	C = 0.01μF	C = 1μF	C = 0.1μF	C = 0.01μF
00 00 00 01	1.49	14.7	156	4.86	49.8	433
11 11 11 11	328	3,279	33,333	717	7,273	60,241

Table 4. Astable Expanded Mode Frequency Table

	ASTABLE MULTIVIBRATOR FREQUENCY (Hz)					
	R_B = 1kΩ; V_{CC} = 15V; V_{REF} = 15V			R_B = 1kΩ; V_{CC} = 5V; V_{REF} = 10V		
Input Digital Code	C = 1μF	C = 0.10μF	C = 0.01μF	C = 1μF	C = 0.1μF	C = 0.01μF
00 00 00 01	0.74	7.69	79.9	2.42	24.7	217
11 11 11 11	328	3,279	33,333	714	7,299	60,241

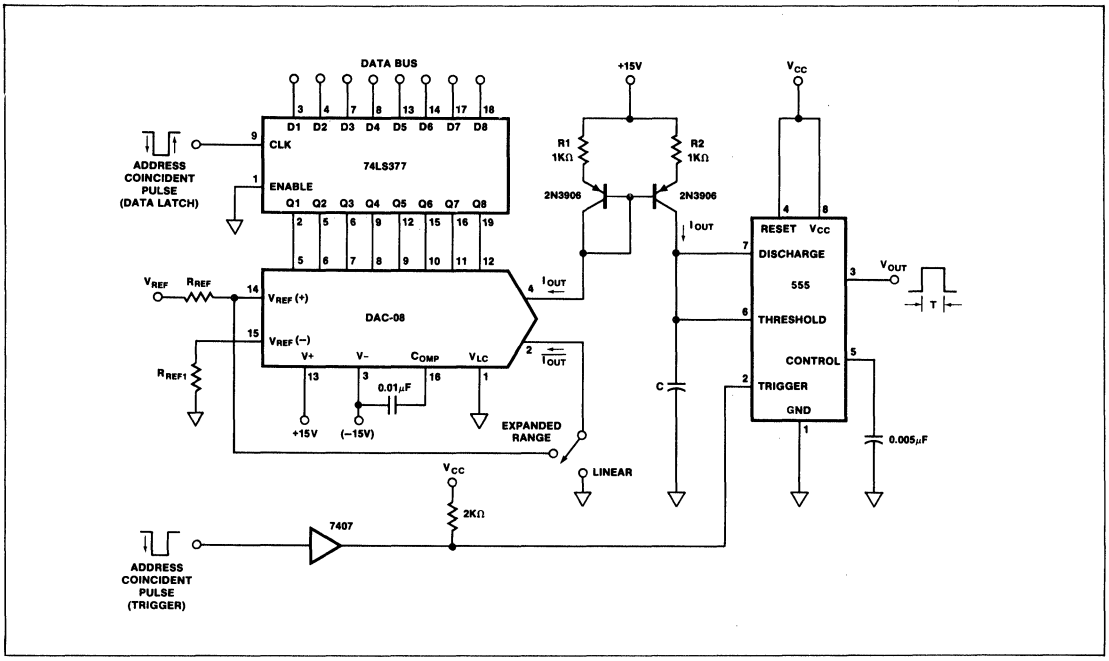


Figure 5. Microprocessor Controlled One-Shot

APPLICATION NOTE 37

EIGHT CHANNEL CODEC DEMONSTRATOR

by B. W. Berry

Precision Monolithics, Inc. has developed a CODEC demonstrator system in order to show the use of their line of telecom devices in a shared-channel system. These circuits provide a working digital transmission system incorporating eight analog input channels digitally interfacing to eight output channels. The circuit design was completed so that a single analog printed circuit board could be used either for encoding eight channels or decoding eight channels. A single digital timing and interface board is used to provide system clocks and the parallel digital data bus from transmitter to receiver. All board layouts and schematics are available from PMI. The design uses pluggable connections so that, if desired, the encoding portion or the decoding portion of the system can be tested separately. The user need only provide three voltage supplies (±15VDC, +5VDC), the appropriate filters and any applicable transmission test equipment.

HARDWARE

The entire eight-channel system consists of twenty-one integrated circuits mounted on three printed circuit boards. Two of the boards, as mentioned, are a common layout which is used for the analog functions of the system. The analog board used for the encoder (analog-to-digital conversion) requires the addition of a COMDAC® (DAC-86, 87), a MUX-88, a SMP-81, a CMP-01, and a REF-02. The other analog board is used for the decoder (digital-to-analog conversion) with the addition of a DAC-86, MUX-88, REF-02, and an OP-16. The general schematic and parts list for the analog boards is shown in Figures 1 and 2.

The control board is a T²L circuit of twelve devices designed to provide three basic functions, a) the successive approximation register with interface to the DAC-86, b) the clock for the encode portion of the demonstrator, and c) the digital

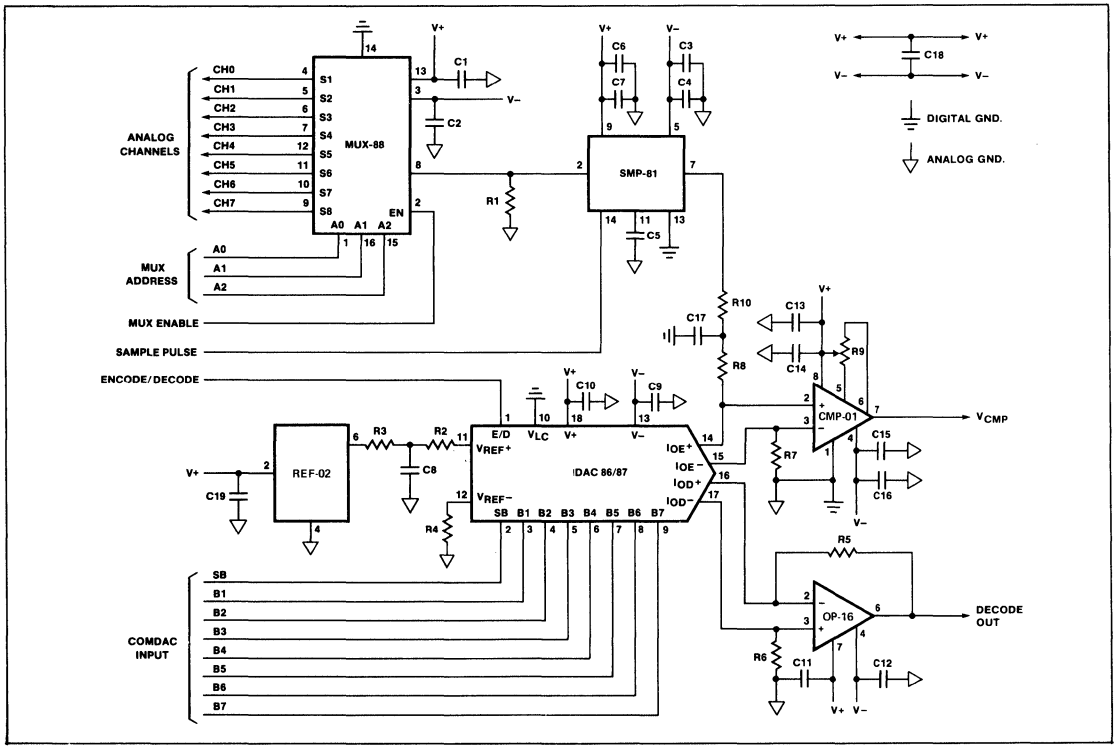


Figure 1. COMDAC* Encoder/Decoder Analog Circuit Board

*COMDAC IS A REGISTERED TRADEMARK.

TRANSMIT (Eight-Channel Encoder)	RECEIVE (Eight-Channel Decoder)
MUX-88	MUX-88
SMP-81FY	COMDAC®DAC-86EX (87)
COMDAC®DAC-86EX (87)	OP-16F
CMP-01EJ	REF-02
REF-02	

RESISTORS

R1 – 20K	R6 – 2.49K
R2 – 330	R7 – 2.49K
R3 – 9.1K	R8 – 1.5K
R4 – 10K	R9 – 2K (POT)
R5 – 2.49K	R10 – 1.0K

CAPACITORS

C1, C2, C4, C7, C8, C9, C10, C11, C12, C13, C15, C18, C19	0.1μf
C3, C6, C14, C16	10μf
C5	5000pf
C17	100pf

Figure 2. Parts List – Analog Board

interface between the encode and decode sections. The encoder clock design is a multiple frequency clock, the usefulness of which is treated in a later section, generated from a programmable read-only memory frequency divider. The PROM was used to provide flexibility in changing the clock waveforms if the user so wishes. The resultant clock waveforms are also described later; the circuit schematic is shown in Figures 3a and 3b. The PROM data is listed in Figure 4. The digital interface is provided by using a standard 8-bit, parallel-in, parallel-out latch updated as the successive approximation process is completed for each input channel. The remainder of the circuit consists of the SAR and the multiplexer address counters. A parts list for the circuit is shown in Figure 5. A complete circuit schematic for the digital board is shown in Appendix A.

The boards are interconnected by use of four mini-dip connectors and cables, a 16-pin and 14-pin from each analog board to the controller. The lead designations of the two connectors are shown in Figure 6. The input and output channels are accessible through "banana"-type plugs; this allows optional connections from the transmission line in order to try different types of filters and line interface circuits. The two analog boards require ±15VDC and "banana" plugs are provided to interface to the appropriate supplies. The control board requires +5VDC only. The entire system layout is shown in block diagram in Figure 7.

SYSTEM OPERATION AND DESIGN

To achieve a workable system configuration, the encoding and decoding operations were approached as two separate designs. The entire transmission link was then connected to complete the end-to-end tests.

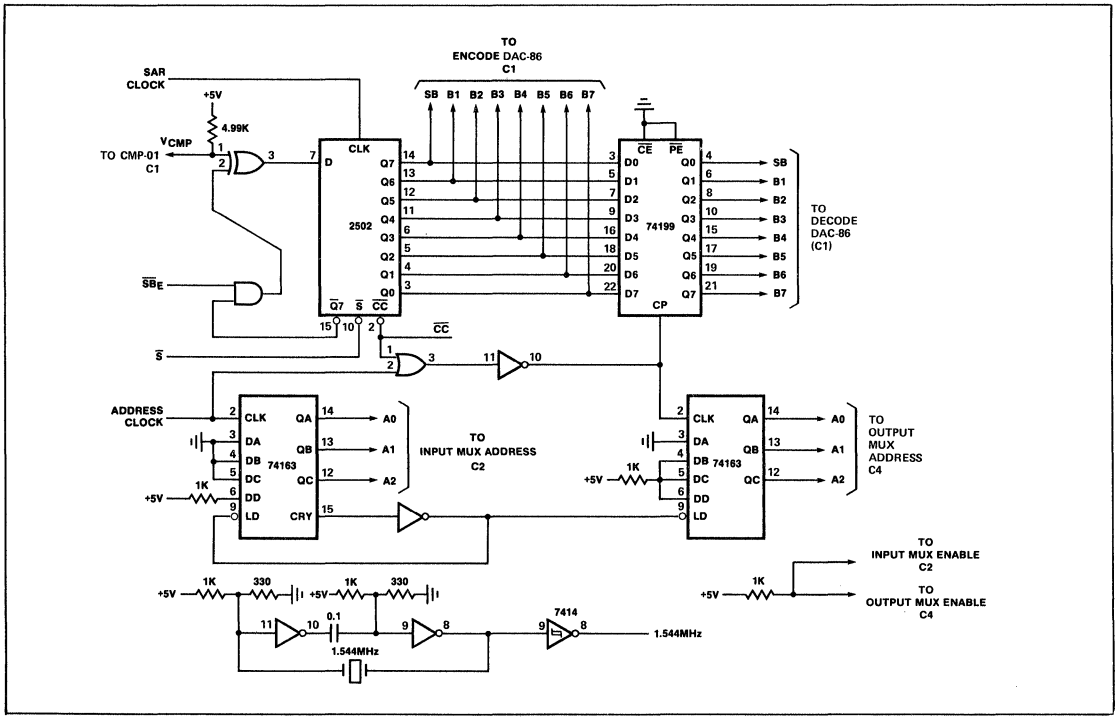


Figure 3A. Encoder/Decode Controller

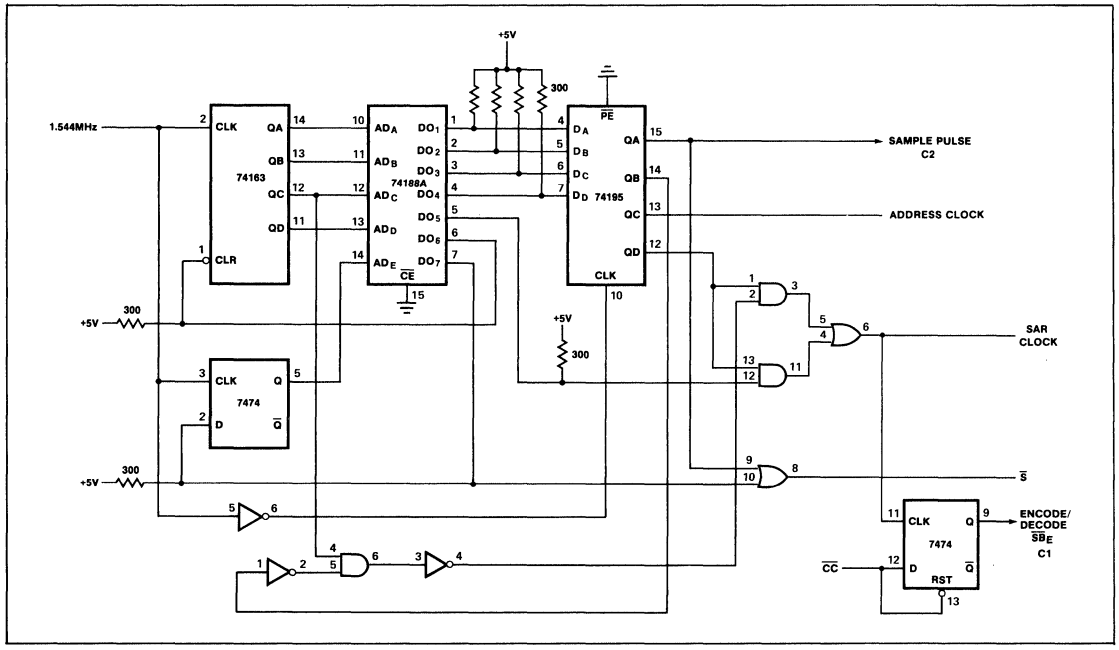


Figure 3B. Encode Clock

ADDRESS	DATA (MSB–LSB)	ADDRESS	DATA (MSB–LSB)
00	20	0C	27
01	28	0D	27
02	20	0E	2F
03	21	0F	6F
04	39	10	67
05	2B	11	67
06	23	12	6F
07	2B	13	6F
08	23	14	67
09	2B	15	67
0A	23	16	6E
0B	2F	17	0E

MSB = $D0_8$
LSB = $D0_1$
Address 18 – 1F – Unused.

Figure 4. PROM-Based Clock

PARTS		PARTS	
7404	2	74163	3
7408	1	74188A	1
7414	1	74195	1
7432	1	74199	1
7474	1	2502	1
7486	1	1.544MHz Crystal	

Figure 5. Parts List – Controller

CONNECTORS

PIN #	C1 (C3)	C2 (C4)
1	+5	+5 Gnd
2	+5	Sample Pulse
3	+5	MUX Enable
4	VC MP	A0 – Address
5	+5 Gnd	+5 Gnd
6	+5 Gnd	A2 – MUX Address
7	+5 Gnd	A1 – MUX Address
8	B7 – LSB	+5 Gnd
9	B6	+5 Gnd
10	B5	+5 Gnd
11	B4	+5 Gnd
12	B3	+5 Gnd
13	B2	+5 Gnd
14	B1	+5 Gnd
15	SB – MSB	+5 Gnd
16	Encode/Decode	+5 Gnd

*C2 is 14 Pin – C1 is 16 Pin

Figure 6. Pin Designations – System Connectors

The accuracy of the encoder, the analog-to-digital converter, is dependent upon several factors. The first, and most significant, is the speed (settling time) of the companding DAC in conjunction with the comparator. Other factors are switching time of the multiplexer, acquisition time of the sample-and-hold, hold-step settling time of the sample-and-hold, and output noise of the sample-and-hold and

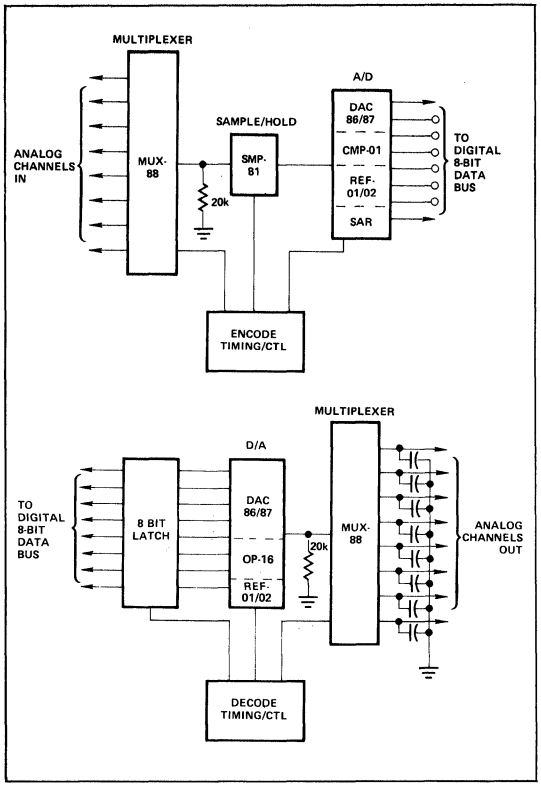


Figure 7. Eight-Channel System Layout

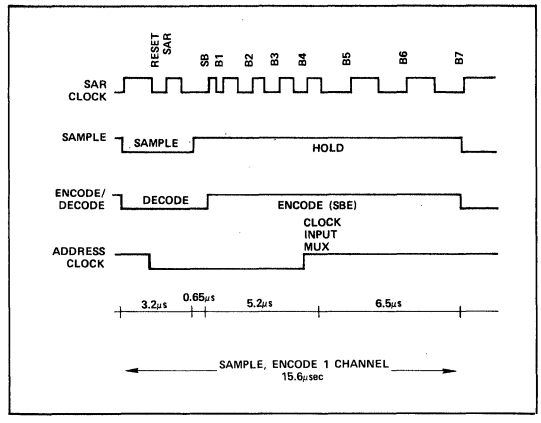


Figure 8. Encoder Timing Waveforms

multiplexer. All of these characteristics had to be considered while developing the encoder circuit.

In a companded A/D conversion, using a successive approximation method, different digital bits require different settling times. There is a constant increase in the settling time required as one goes from the sign bit to the chord bits and then to the step bits. This increase in settling time is partially caused by the scaled current sources used to design a companding D/A and is most affected by the magnitude of the voltage level being converted. So as the output currents of the DAC-86 become smaller (at smaller voltage levels), the comparator is less responsive. Also as the less significant bits are clocked in, the situation becomes more critical since progressively smaller current changes are provided to force the comparator to change output state. The encoder clock waveforms, shown in Figure 8, depict a system approach to accommodate these timing characteristics. The governing design criteria was that a limited amount of time is available to complete the successive approximation of the analog signal (for eight channels, with a sampling frequency of 8kHz, this means 15.6μs) and the optimum clock must fit within this period. All functions (including sampling, encoding, switching) must therefore be completed with an acceptable accuracy, within this time constraint. To achieve accurate data acquisition with the sample-and-hold, a sample pulse of 3.2μs was used. Once the pulse goes from sample to hold, there is a waiting time required to allow the sample-and-hold output to settle to the "held" value, 650ns is the time added. Since the sign bit is the fastest transition, the basic system clock (1.544MHz) is used for the first SAR clock period. The clock frequency is then halved to clock in the chord bits (B1, B2, B3), the next "slowest" transitions. Finally, the clock frequency is halved again to allow for the step bits (B4-B7), a frequency of 386kHz. The times required for the different bit conversions are shown in Figure 8. The SAR is reset during the sampling period and once the sample circuit has entered the hold mode, the input multiplexer's address is changed. This provides ample time for the MUX to switch to the next analog input with little effect on the adjacent waveforms. In addition, to further minimize interchannel crosstalk, a 20kΩ resistor to ground is added to the multiplexer output.

To provide sufficient noise immunity from the sample-and-hold to the comparator, a simple filtering circuit using a 100pF capacitor is added. A 4.9kΩ resistor to +5V from the comparator output aids in increasing the DAC-86 and comparator speed. In order to test the encoder without adding a decoder, a high-precision voltage source (DC levels) was used as an input to one or more channels of the A/D circuit. The data output (one byte every 15.6μs) was sampled and stored in a logic analyzer. By reviewing the samples for each channel, and comparing the data from all channels of the eight channel system, the effects of changes in the clock on the accuracy of the design could be observed. By inputting a steady-state value, the data out would not only demonstrate the "consistency" of the A/D conversion but also make obvious any adjacent channel effects that were produced.

The analyzer sampling also presents a method of initializing the system components. By grounding all inputs and digitally sampling the data bus output, the zero level can be set so as to produce an alternating series of data bytes equivalent to 0 volts (10000000 and 00000000).

A similar design approach was used in developing an eight-channel decoder. In this case, the response time of the DAC-86 and op amp offers little problem since an eight-channel decoder is relatively slow. However, the accuracy of the devices does become important. The design considerations become, therefore, the nonlinearity of the DAC-86 in

conjunction with the switching time and charge injection of the multiplexer. The DAC-86 is manufactured to strict linear specifications, which assures both excellent decoding linearity and absolute accuracy. The multiplexer is used both as a switch to demultiplex the output waveforms and as a holding circuit by adding capacitance to the output leads. One effect seen in the multiplexer is that as a channel is switched off, there is a charge injected onto the output. This charge is not normally obvious in a MUX design, however, when working into a high impedance (such as a filter) and with capacitors on the source leads (outputs), the charge can add an offset to the waveform. To minimize the effect, a large capacitor (0.1μF or greater) is added. Since the charge pulse is a short duration signal, the signal on the larger capacitor will be less affected by the charge than if a smaller component was used.

In terms of a system decoder design, this circuit could be used for more than eight channels. The op amp and DAC-86 are both capable of responding to more output channels. An eight-channel system was incorporated to remain compatible with the analog board that is used in the demonstrator. In order to decode more channels (>12), the output capacitance on the demultiplexer would need to be reduced. The other circuit components would remain the same.

The decoding circuitry can be tested separately by adding a series of data bytes and monitoring the output channels. The CCITT recommendation for testing PCM systems includes a method of testing a decoder by introducing a standard sequence of digital data words in order to produce a 1kHz sinusoid at a nominal level of 0dBm0.* This method proved useful in "debugging" the circuit design prior to attempting the end-to-end tests.

SYSTEM TESTS

Once the encoder and decoder were functioning separately, the entire system was connected with the appropriate interfacing to allow for full-system transmission tests. The measurements taken were the standard set of PCM specifications observed in the majority of data sheets for telecommunication oriented products. These tests included signal-to-total distortion, gain tracking, intelligible crosstalk, and idle channel noise.

There are two different methods of performing the tests. For the U.S. standards, a sinusoid signal is used as the channel input and the measurements are taken around the base (test) frequency. For the European tests, a pseudo-random or "white" noise source is preferred as the input signal. The test results discussed here were obtained with the U.S. testing procedures; similar test results have been achieved using European test methods.

The test set-up for signal-to-total distortion and gain tracking measurements is shown in Figure 9. The results are plotted in Figures 10 and 11. As is seen, each test was performed with both the C-Message Weighting and the 3kHz Flat response terminating configurations. The results using the μ-law parts (DAC-86) are represented. In terms of signal-to-total distortion, the system exceeds the recommended standard at all input levels by 2dB or greater. The system is also well within the recommended gain tracking limits for both terminations.

The crosstalk and idle channel noise measurements are given in Figure 12. One consideration of the system design, in terms of performance, was that the most difficult characteristic for a shared-channel system to minimize is the intelligible crosstalk specification. The design is directed

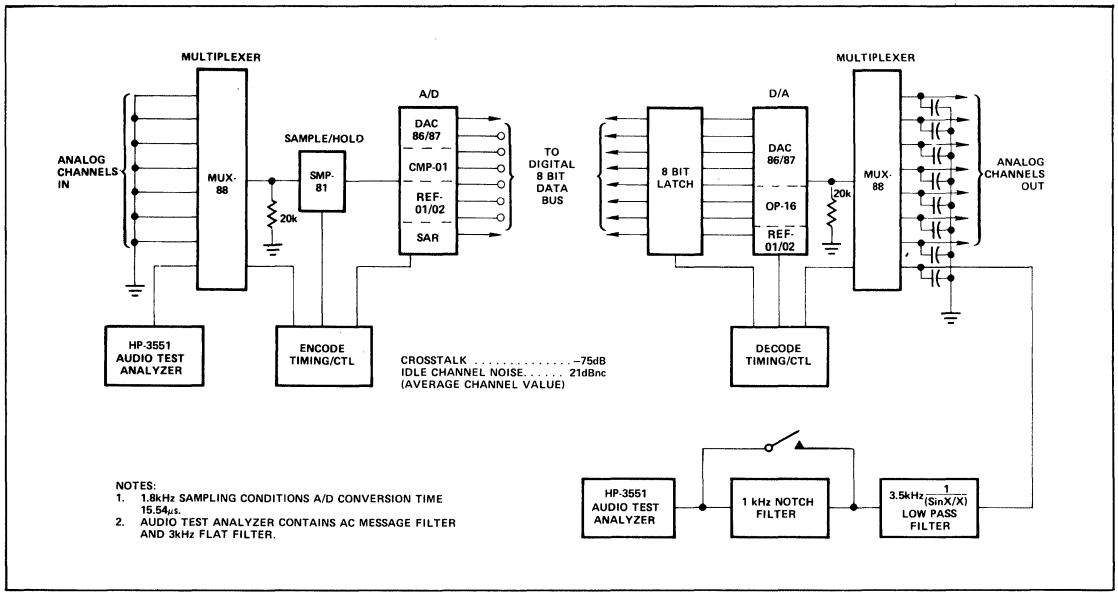


Figure 9. Eight-Channel Test Configuration

*Reference — CCITT Sixth Plenary Assembly (1976), Orange Book Vol. III-2

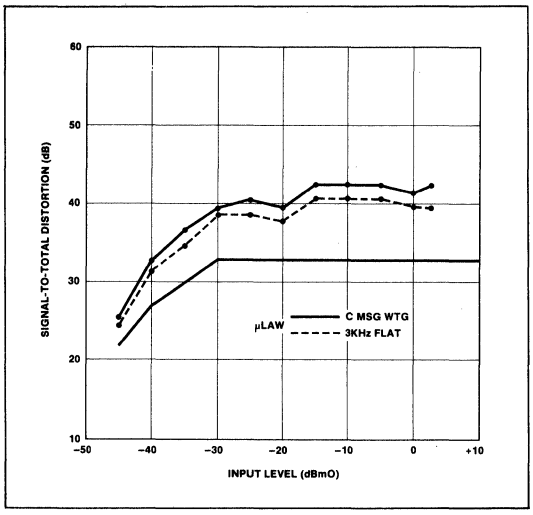


Figure 10. Signal-To-Quantizing Distortion vs. Input Level

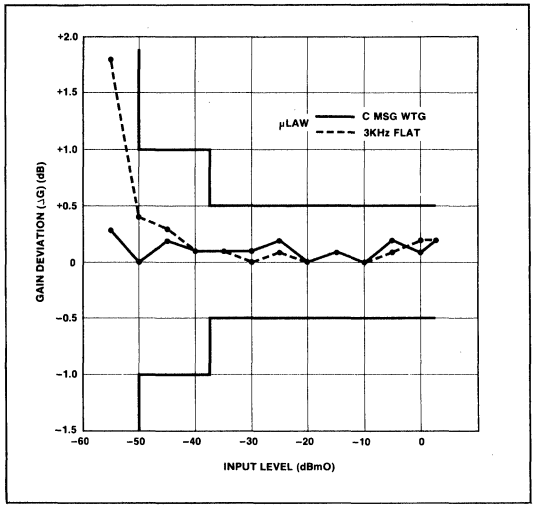


Figure 11. Gain Tracking

toward optimizing this measurement. The idle channel noise is at the system recommended level when measured without output filtering. It is further reduced by adding a PCM receive filter on the decoder multiplexer.

CONCLUSIONS

The circuitry just discussed is meant to represent one approach to designing an eight-channel, shared CODEC system. It is not meant to be the only design, but provides a working system upon which to base further engineering development. It should be noted that in terms of transmission testing, the demonstrator is an end-to-end system. The configuration presents the users with a complete circuit enabling them to observe the individual device characteristics significant in producing a shared-channel design.

The completed eight-channel CODEC demonstrator is shown in Figure 13, mounted in its carrying case.

IDLE CHANNEL NOISE

CHANNEL	NOISE (dBm0)	CHANNEL	NOISE (dBm0)
1	–66.9	5	–62.6
2	–67.6	6	–65.3
3	–67.0	7	–67.0
4	–67.2	8	–61.8

CROSSTALK

FREQUENCY	INTELLIGIBLE CROSSTALK
300 – 2900Hz	≤–78dBm0
2900 – 3400Hz	≤–70dBm0

Figure 12. Idle Channel Noise and Crosstalk

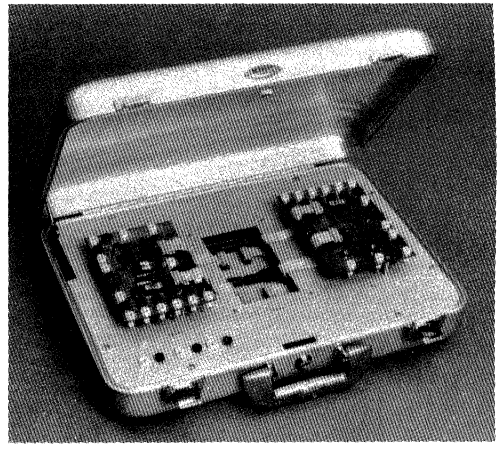


Figure 13. CODEC Eight-Channel Demonstrator

The demonstrator provides a starting point from which most characteristics important to both shared-channel and single-channel designs can be manipulated to allow for improvements in transmission quality. To be able to develop a realistic transmission design, the system engineer needs to consider more than just the coder/decoder devices. A complete multiple channel system, such as the PMI eight-channel demonstrator, allows the user to observe the complete system performance as it is affected by the individual system components.

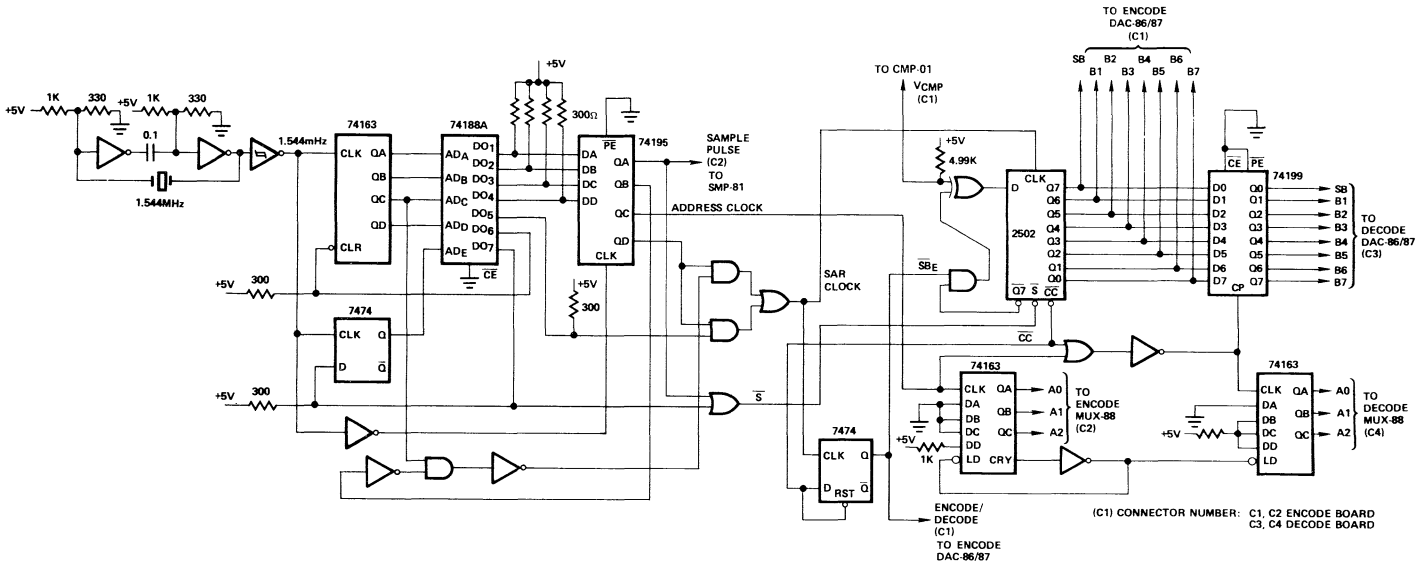


Figure A-1. Circuit Schematic

APPLICATION NOTE 38

FOUR-CHANNEL SHARED CODEC

by B.W. Berry

FOUR-CHANNEL SHARED CODEC

A four-channel CODEC assembled from LSI components is a cost-effective digital transmission system requiring a relatively small number of devices. The system makes use of a single COMDAC®* companded DAC-86 or DAC-87 digital-to-analog converter for both encoding and decoding (see Figure 1). The timing of the circuitry is compatible with ATT and CCITT system specifications.

Each channel is sampled at the standard 8kHz rate. With four channels this allows approximately 31.2μs to encode the sampled analog input and to decode the received digital signal for the same channel. To simplify the timing system requirements equal amounts of time were allowed for encoding and decoding, thus permitting 15.6μs for the more critical encode portion of the cycle. The encode/decode clocking scheme for this CODEC was incorporated directly from a successful eight-channel CODEC system which has been published as PMI Application Note 37. One original feature of the four-channel design was the use of dual eight-channel multiplexer ICs to switch the four channels. This results in a system whose interchannel crosstalk is practically negligible. Crosstalk figures of −85dB have been observed. This article describes the design procedure and reviews the transmission characteristics of the completed system.

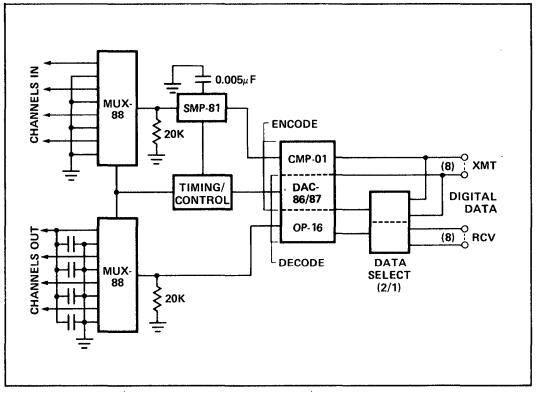


Figure 1. Four-Channel CODEC

CIRCUIT DESIGN

The analog circuitry required for a four-channel system is shown in Figure 2. The circuit uses the same printed circuit

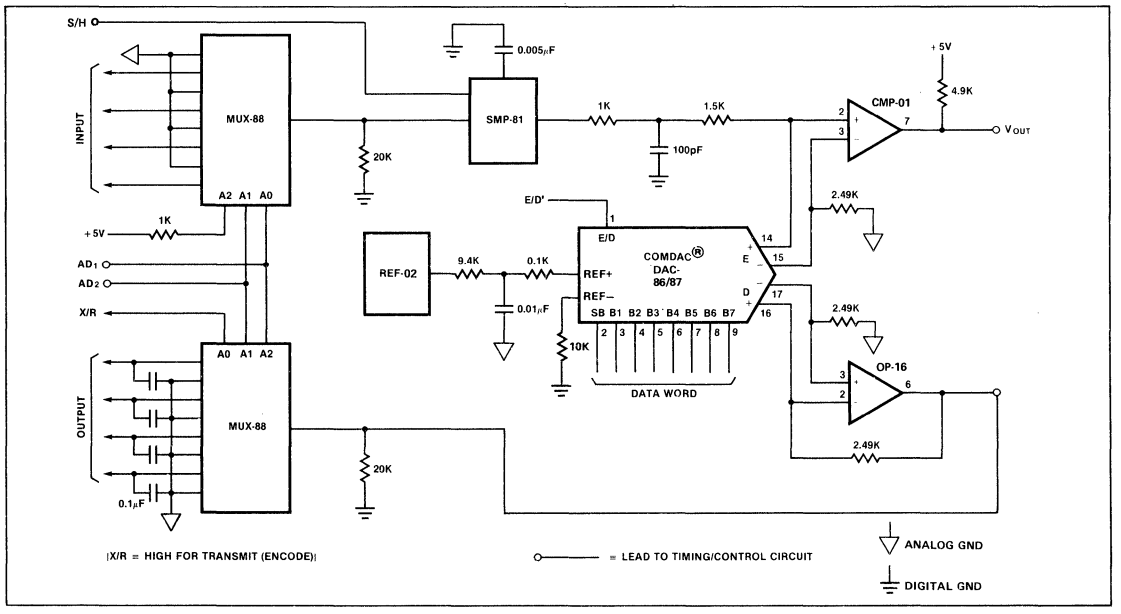


Figure 2. Four-Channel CODEC — Analog Board

*COMDAC® is a registered trademark of Precision Monolithics, Inc.

card as the transmit or receive sections of the eight-channel CODEC demonstrator (with the addition of a second multiplexer). The analog inputs all connect at the input multiplexer (MUX-88) using alternating inputs, the output (drain) of the MUX drives the SMP-81 sample-and-hold device. Once the input level is held, the COMDAC® (DAC-86 or 87), in conjunction with the comparator (CMP-01), begins the analog-to-digital conversion sequence. A successive approximation encode procedure is used; this generates, within the allotted conversion time (15.6μs), an eight-bit digital approximation of the analog level. The data byte is available at the successive approximation register output for the next 15.6μs time frame. During this time the CODEC decodes the incoming digital signals.

The decode cycle begins as soon as the encode cycle is completed. The DAC-86 is switched to the decode mode and an eight-bit data word is presented at its input leads, presumably from some distant analog-to digital converter through a switching matrix. As the DAC-86 is switched to decode, the operational amplifier (OP-16) converts the out put current of the DAC-86 into the appropriate voltage level. The output multiplexer is switched to the proper analog port as the decode procedure is initiated. On the output leads of the "de"-multiplexer, a hold capacitor is used to provide an output holding function. The "staircase" waveform is then available for filtering and the final subcriber interface.

As shown in the Figure 2, several circuit precautions were taken to reduce the internal noise levels. Foremost among these is the ample use of grounding throughout the analog circuit. All power supply inputs to the ICs are bypassed with capacitance (0.1μF) to ground. In addition, any spare land area of the board is filled with ground paths. The various voltage return paths are kept separate except for one common location on the board at the supply input leads. For further noise protection, a 20kΩ resistor to ground is connected to the drain leads (the common output or input) of both multiplexers. This reduces the multiplexer output noise and any crosstalk voltage feedthroughs. Also, in terms of the multiplexers, the output MUX is addressed to a grounded terminal (source connection) in between the active channels. This aids in minimizing the mutiplexer injection phenomena (discussed in detail in Application Note 37, describing the eight-channel CODEC design) and helps to further reduce the device crosstalk. The significance of using two multiplexers in this design is to allow unused channels of the output MUX to be connected to ground. The active channels are then alternated, in terms of addressing, with the grounded terminals. Addressing the multiplexers requires only two of the address leads to be controlled by a binary counter for data selection. The third address input is either held active (as in the input MUX), or can follow the system transmit and receive control signal (lead X/R, as in the output MUX). The address sequence for the input MUX is repeated through ports 4 to 7 (100 to 111), the most significant bit is held high and the two lower bits are counter outputs. This scheme allows maximum settling time for the MUX since the next channel to be encoded is selected more than 16μsecprior to the conversion. For the output MUX, the two **most** significant bits of the address are the counter output leads, the least significant bit is the transmit/receive lead (X/R). As is shown in Figure 3, the address sequence

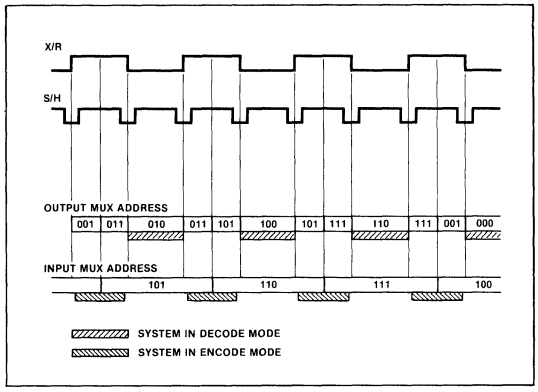


Figure 3. Four-Channel CODEC — Multiplexer Sequencing

alternates from active output port (even addresses) to grounded ports (odd addresses). The counter is changed while the MUX is selecting an unused (grounded) channel. This type of sequencing reduces the interchannel interference of the MUX and greatly adds to the system's measured performance.

To minimize sample-and-hold noise, a simple filter circuit is added to the output terminal of the device. A similar approach was used in the eight-channel design. Another feature in common with the eight-channel system is the use of a 4.9kΩ resistor pull-up from +5V to the output of the comparator; this decreases the switching time of the device for the encode procedure.

The timing waveforms generated for the four-channel system are based on the encoder clock used in the eight-channel CODEC. This clock circuit is shown in Figure 4. In a companded A/D conversion, using a successive approximation method, different digital bits require different settling times. There is a constant increase in the settling time required as one goes from the sign bit to the chord bits and then to the step bits. This increase in settling time is partially caused by the scaled current sources used to design a companding D/A and is most affected by the magnitude of the voltage level being converted. So that, as, the output currents of the DAC-86 become smaller (at smaller voltage levels), the comparator is less responsive. As the less significant bits are clocked in, the situation becomes more critical since progressively smaller current changes are provided to drive the comparator. A multi-frequency clock will take advantage of these timing variations; such a clocking scheme is shown in Figure 5. The governing design criteria is that a limited amount of time is available to complete the successive approximation of the analog signal and the optimum clock must fit within this period. All functions (including sampling, encoding, switching) must be completed, therefore, with an acceptable accuracy, within this time constraint. To achieve accurate data acquisition with the sample-and-hold, a sample pulse of 3.2μs was used. Once the pulse goes from sample to hold, there is a waiting time required to allow the sample-and-hold output to settle to the "held" value; 650ns is the time added. Since the sign bit is

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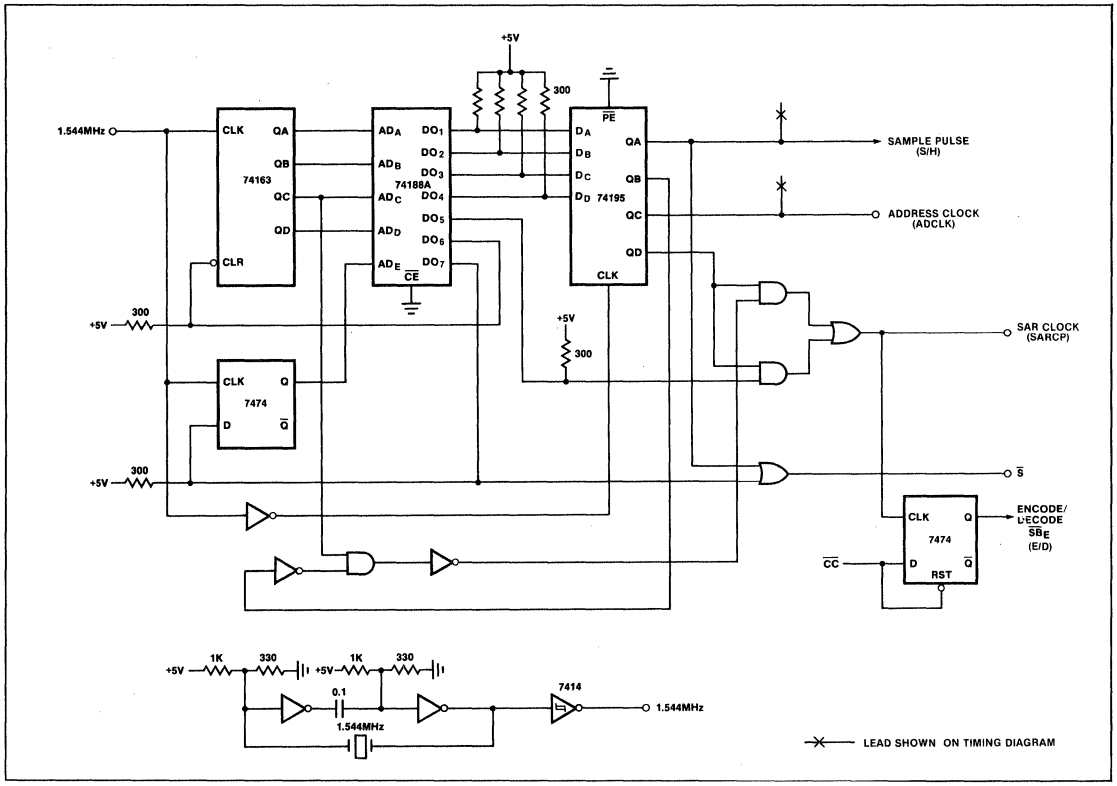


Figure 4. PROM Based System Clock

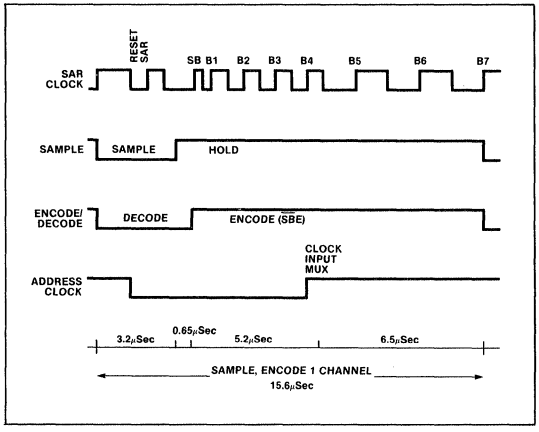


Figure 5. Four-Channel CODEC — Encoder Timing

the fastest transition, the basic system clock (1.544MHz) is used for the first SAR clock period. The clock frequency is then halved to clock in the chord bits (B1, B2, B3), the next "slowest" transitions. Finally, the clock frequency is halved again to allow for the step bits (B4-B7), a frequency of 386KHz. The SAR is reset during the sampling period and once the sample circuit has entered the hold mode, the input multiplexer's address is changed. This provides ample time for the MUX to switch to the next analog input with little effect on the adjacent waveforms.

Using this timing pattern as the starting point, the original eight-channel system was converted to a four-channel bidirectional design. The only additional control functions to be added were the timing signals needed to switch the DAC-86 between the encoding and decoding modes, to operate the output multiplexer, and to select the proper data inputs for the DAC-86. The DAC-86 mode select and the multiplexer address leads, as mentioned previously, are generated from a single system transmit/receive control (shown as X/R in Figure 6). The lead is the system monitor of the mode in which the CODEC is operating. When active (logic "1"), the DAC-86 and associated parts are in the encode mode. In the encode mode: the successive approximation register clock is enabled, the encode/decode lead to the DAC-86 (E/D) is enabled, the data input selector directs the SAR output back toward the DAC-86 for the feedback needed in successive approximation, and the output MUX connects the OP-16 to a grounded (unused) channel. The X/R lead remains at logic "1" until encoding is completed, then goes to ground (logic "0"), the decode state. To decode a

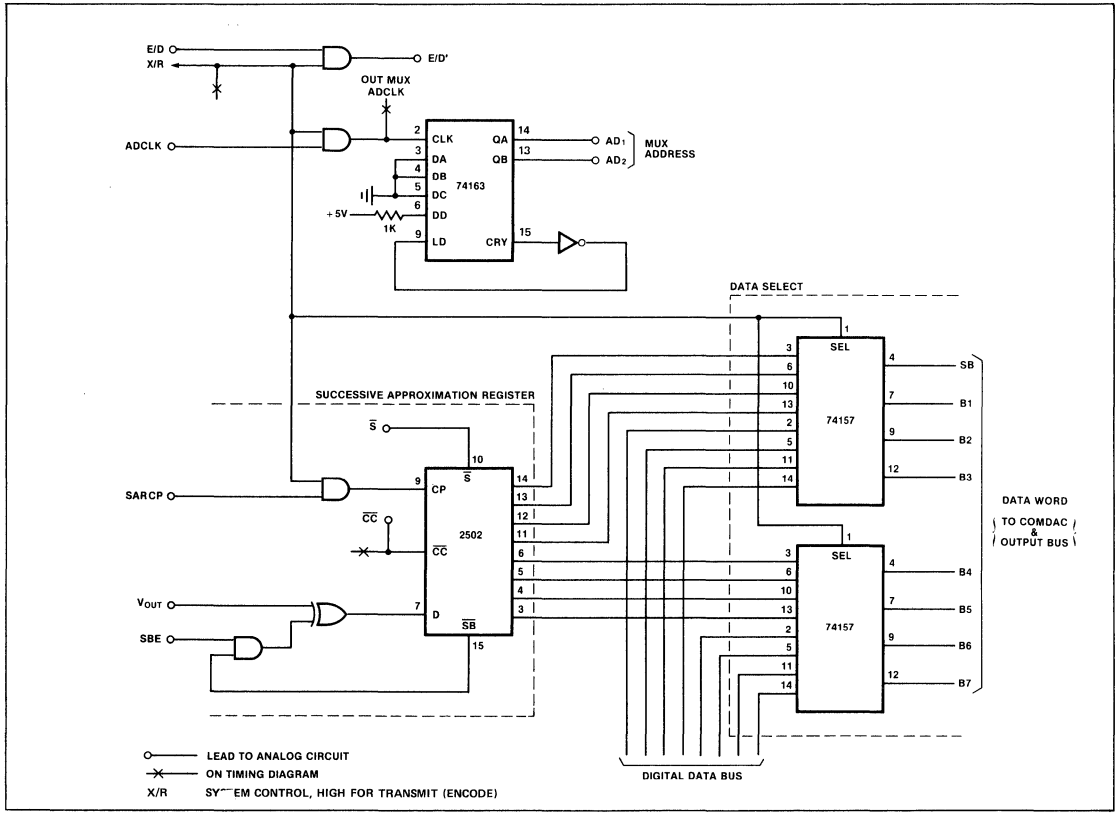


Figure 6. Four-Channel CODEC — Control Board

data byte, the DAC-86 is held in the decode mode (E/D is low), the output MUX is addressed to an active output port, and the SAR clock is disabled (this register will hold the last encoded data word throughout the decode cycle — it is not cleared until a new input signal is to be encoded). The data selector is directed to the digital system bus and the decoding of the byte on the bus begins. As described, the address leads of the multiplexers are programmed such that the input MUX will always be directed toward the next active channel, once the previous analog sample has been held. But the output MUX does not connect to an active channel until the decode cycle begins; during the encode cycle only unused (grounded) ports are addressed.

SYSTEM TESTS

The system as configured in the block diagram (Figure 7) is a complete four-channel CODEC. To perform the transmission tests, it was decided to use a single CODEC circuit and transmit data in a "loopback" configuration. As was mentioned earlier, the only signal required from an external controller is the X/R lead. This is generated for the test circuit by halving the inverted ADCLK lead from the prom-based clock. The system waveforms that result are shown in Figure 8. These clock patterns can be correlated to the encode clock waveforms in Figure 5 by comparing the ADCLK or the S/H leads. Since the successive approximation register is not cleared until after the decode cycle, an external register is not necessary to hold the data for the decoding process.

The transmission tests that were completed were the typical telephone network tests as described in the eight-

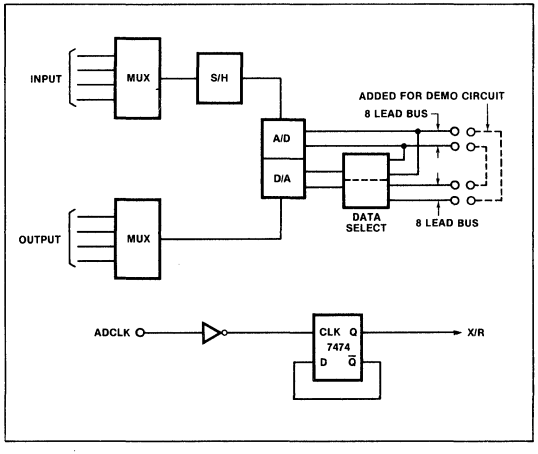


Figure 7. Four-Channel CODEC — Demonstrator Layout

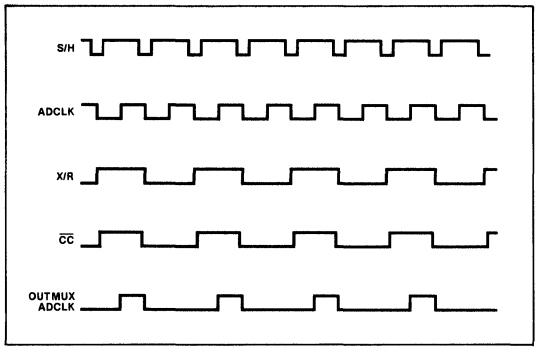


Figure 8. Four-Channel CODEC — Demonstrator Timing

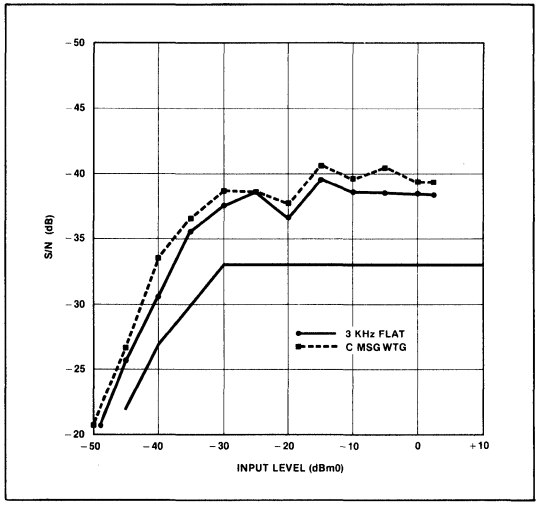


Figure 9. Signal-To-Total Distortion (Four-Channel)

channel application information. The tests include signal-to-total distortion, gain tracking, intelligible crosstalk and idle channel noise. Again the test method used for the first two tests was based on a sinusoidal input signal, as is common in the AT&T specifications, at a frequency between 400 and 3400Hz using a frequency-selective wave analyser. The results of all testing are shown in Figures 9 through 11.

It is of some interest to compare this data with the test results of the eight-channel CODEC design. In particular, the idle channel noise and the crosstalk measurements are improved. This can be partially explained by the different manipulations of the output multiplexer. This does however, tend to point to the fact that the output MUX can be a significant source of noise and cross channel interference. Further data is certainly necessary, but these results do point out an area of concentration for the system designer wanting to improve system performance.

In terms of signal-to-total distortion and gain tracking, the four-channel results compare favorably with the eight-

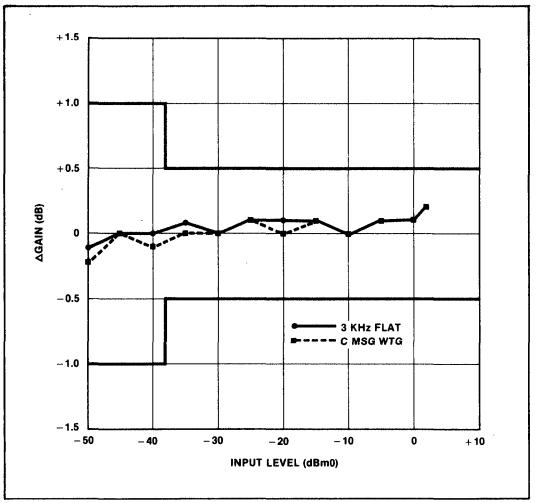


Figure 10. Gain Deviation (Four-Channel)

IDLE CHANNEL NOISE

Channel	
1	
2	no channel
3	had noise
4	level > 2dBrnc

INTELLIGIBLE CROSSTALK

f_{input}	Level
400-3400Hz	≤ −85dBmO

Figure 11. Transmission Measurements (Four-Channel)

channel data and both systems exceed the AT&T requirements. Overall, the transmission tests point out that using a single DAC-86 for four-channel transmitting and receiving is a realistic approach and can comply with all " system" standards.

CONCLUSIONS

The testing described in the preceeding pages demonstrates the feasibility of encoding and decoding four channels with a single DAC-86. The system has several advantages: 1) a smaller number of devices are required to complete the CODEC function than were necessary for the eight-channel design, 2) the clock circuitry (prom-based timing generator) is common to all encoders, so only a single such circuit is needed for multiple CODECs. Both of these factors contribute to reduced printed circuit board area for multiple transmission channels. The devices needed for a four-channel CODEC are listed in Figure 12. In terms of package sizes only one device is larger than sixteen pins (the DAC 86/87 is 18 pins) and three of the components are only eight pins. This should make system layout fairly simple and allow relatively dense component packing. If channel monitoring is incorporated, then a single supervision circuit could administer several circuit packs in a system line-

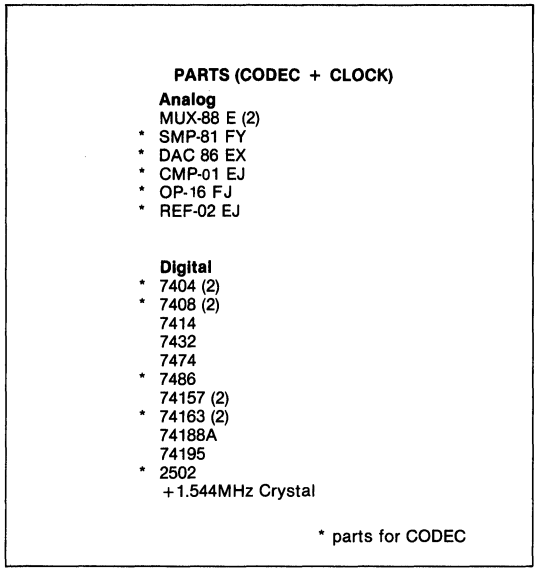


Figure 12. Four-Channel CODEC — Parts

up. The number of external leads is reduced in a four-channel CODEC and the design is easily added to a bus-structure data switching system.

The price per channel is still less than that being quoted by single-channel CODEC designers although slightly more than the eight-channel approach. (See pricing, Figure 13). The sacrifice made in price-per-channel is offset by the gains in system architecture and board layout offered by a four-channel shared CODEC. The shared channel CODEC approach is a viable solution to producing a digital transmission system. AN-37 shows designs at even lower per channel cost.

	ENCODE/DECODE	CLOCK
Digital	$ 3.82	$ 4.12
PMI	$19.90	
Total	$23.72	$ 4.12
per channel	$ 5.93	$ 1.03 ($0.17, when using clock for 24 channels)

NOTE: Pricing Based on 100,000 Parts

Figure 13. Four-Channel CODEC — Costs

APPLICATION NOTE 39

COMPANDING DIGITAL-TO-ANALOG CONVERTER

by Guido Pastorino

(FROM PMI DESIGN REVIEW NOTES – 1975)

INTRODUCTION

A companding digital-to-analog converter (DAC) is the key component in PCM CODEC systems. (CODEC is an acronym for coder-decoder.) A CODEC performs the coding functions which consist of an analog-to-digital conversion (ADC) of the input analog (voice) signal and decoding, which consists of a digital-to-analog conversion (DAC) of the received digital input.

The DAC is used for both encoding and decoding; it is in a feedback loop to generate the ADC functions. Voice signals in telephony require a system with a very large dynamic range. The dynamic range (DR) of a CODEC is defined as the ratio of the largest resolvable signal to the smallest signal which can be encoded. The dynamic range of the CODEC is the same as that of the DAC used in either the decode mode or in the feedback loop of the successive approximation type ADC. The dynamic range of a DAC is simply the ratio of its output for a linear input of one least significant bit (LSB) to that of the largest, all "1s," input. This ratio is usually expressed in decibels using the equation:

$$DR = 20 \log_{10} \frac{I_{MAX.}}{I_{LSB}}$$

where for a current output DAC I_{MAX} is the output current for all "1s" input and I_{LSB} is the output current for one LSB input. Using this equation a linear bit DAC can be shown to resolve a ratio of 2^n:1 therefore:

$$DR = 20 \log_{10} \frac{2^n}{1} \approx 6^n$$

The wide dynamic range requirements of a telephone system require the equivalent dynamic range of a 12-bit system or 72dB. However, this system would not be satisfactory for telephone voice transmission because of its excessive bandwidth requirements. With present day T1 type transmission systems a 64kbits/sec data rate is required to transmit each voice channel. The use of the linear system would increase this bit rate to 96kbits/sec. This would provide more accuracy than is needed at the expense of excessive bandwidth.

For voice systems the most important criterion is the signal-to-noise ratio. In a PCM system noise is due almost entirely to quantizing distortion. Thus, a non-linear DAC has a non-linear transfer characteristic to compress the analog signal into a digital word and a complementary transfer characteristic to expand the digital words into analog signals with a wide dynamic range. For a telephone system a CODEC requires a fairly uniform signal-to-distortion ratio over its entire dynamic range. Achieving this uniform signal-to-distortion ratio over a wide dynamic range requires the use of non-uniform coding. A non-uniform CODEC is a coder-decoder pair whose input amplitude range is divided into steps of unequal widths, such that the width of the quantizing steps increase in proportion to the amplitude of the signal. To achieve uniform signal to distortion performance a logarithmic transfer function is required. The word compand, (compand is an acronym for compress — expand) was borrowed from analog systems to describe this non-uniform coding system where quantizing and coding is such that step size depends on the input amplitude.

COMPANDING PRINCIPLES

Companding requirements differ for different signal distributions. As mentioned above, voice signals require constant S/D performance over a wide dynamic range. In order to accomplish this the distortion must be proportional to the signal level. This feat is best achieved by the use of a logarithmic compression law. However, a truly logarithmic assignment of code words is not physically possible since this implies an infinite number of codes. Two methods for generating practical implementations of logarithmic transfer functions have been derived which have become industry standards. These methods are generally known by their transfer functions which are called μ-law and A-law respectively. Both of these transfer functions are normally implemented with eight-bit non-linear DACs to achieve a 72dB dynamic range. This is the equivalent dynamic range of a twelve-bit linear DAC. The μ-law and the A-law transfer functions are described by the following equations:

$$\mu\text{-law} \quad Y = \frac{\ln(1+\mu|X|)}{\ln(1+\mu)} \quad \text{sgn } X \quad \text{for } -1 \le X \le +1$$

$$\text{A-law} \quad Y = \frac{1+\ln A|X|}{1+\ln A} \quad \text{sgn } X \quad \text{for } 1/A \le X \le 1$$

$$Y = \frac{A|X|}{1+\ln A} \quad \text{sgn } X \quad \text{for } 0 \le X \le 1/A$$

These laws have unique signal-to-distortion characteristics for each value of μ and A respectively. At present ATT has settled on a value of μ equal to 255 and CCITT specifications use a value of A equal to 87.6. Substituting these constants into the original equation above obtain:

$$\mu\text{-law} \quad Y = 0.18 \ln(1+\mu|X|) \quad \text{sgn } X \text{ for } -1 \le X \le 1$$

$$\text{A-law} \quad Y = 0.18 \ln(1+\ln|X|) \quad \text{sgn } X \text{ for } 1/A \le |X| \le 1$$

$$Y = 0.18\, A|X| \quad \text{sgn } X \text{ for } 0 \le |X| = 1/A$$

The wideband (unfiltered) signal-to-distortion ratio over the useable dynamic range of voice transmissions is shown in Figure 1. This plot does not represent actual system performance; it is instead, a measure of the distortion which would be caused by an ideal quantizer.

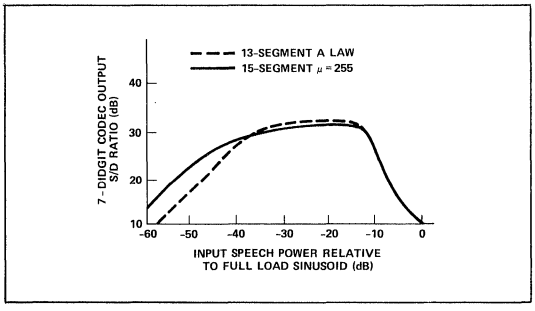


Figure 1. Input Speech Power Relative to Full Load Sinusoid (dB)

The practical implementation of the two transfer functions is accomplished by standardized piece-wise linear approximations. The transfer functions are implemented in chords or segments where the transfer function within any one chord is a linear staircase. Each chord has sixteen steps and the size of the step in each succeeding chord is double the size of the step in the preceeding chord. There are normally eight chords numbered zero through seven in both μ-law and A-law characteristics. For the A-law function the first two chords on either side of the origin have equal step sizes, whereas, for the μ-law function, the second chord after the origin has a step size which is double that of the first. For all remaining chords the steps double in size for each succeeding chord. This applies to both the μ-law and A-law functions. For the A-law function the four chords about the origin can be considered as a single segment so that the A-law characteristic is sometimes referred to as being a "13-segment" code. The A-law characteristic also differs from the μ-law characteristic in the manner in which the transfer function crosses the origin. The X-axis origin for the μ-law is at "mid-step" while the X-axis origin for the A-law is coincident with a "riser". This can be understood better from the "blow-ups" about the origin of Figures 2 and 3.

In order to obtain the best implementations of the transfer function, companded DACs are constructed such that encode and decode functions are offset by one-half step. With this technique the quantizing band for the encode DAC will be centered about the decode value. This can be seen in Figure 4, where the μ-law characteristics about the origin are shown. (The A-law characteristics would be identical except for the "mid-riser" phenomena at the origin.) As an example suppose that, for Figure 4, an analog input whose amplitude lies between levels 2 and 4 is being encoded. The best quantizing code to assign to this entire quantizing band is its mean value of 3. Thus the DAC used in the suc-

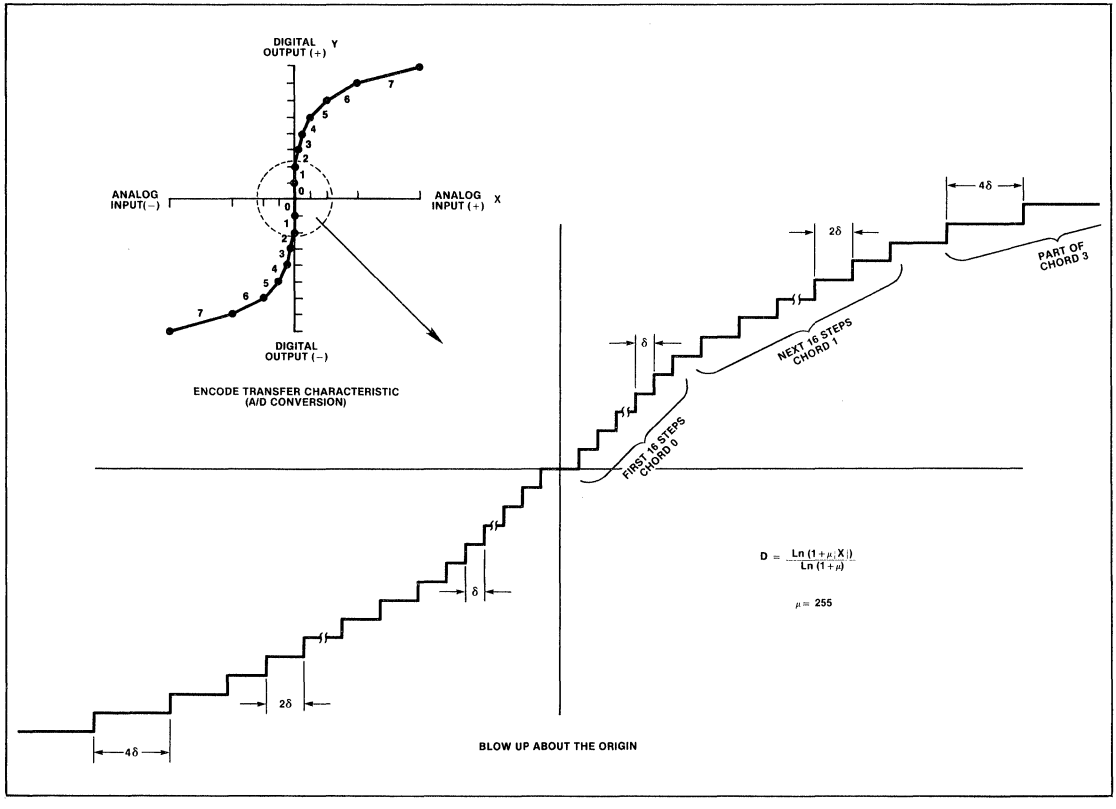


Figure 2. μ-Law Transfer Function

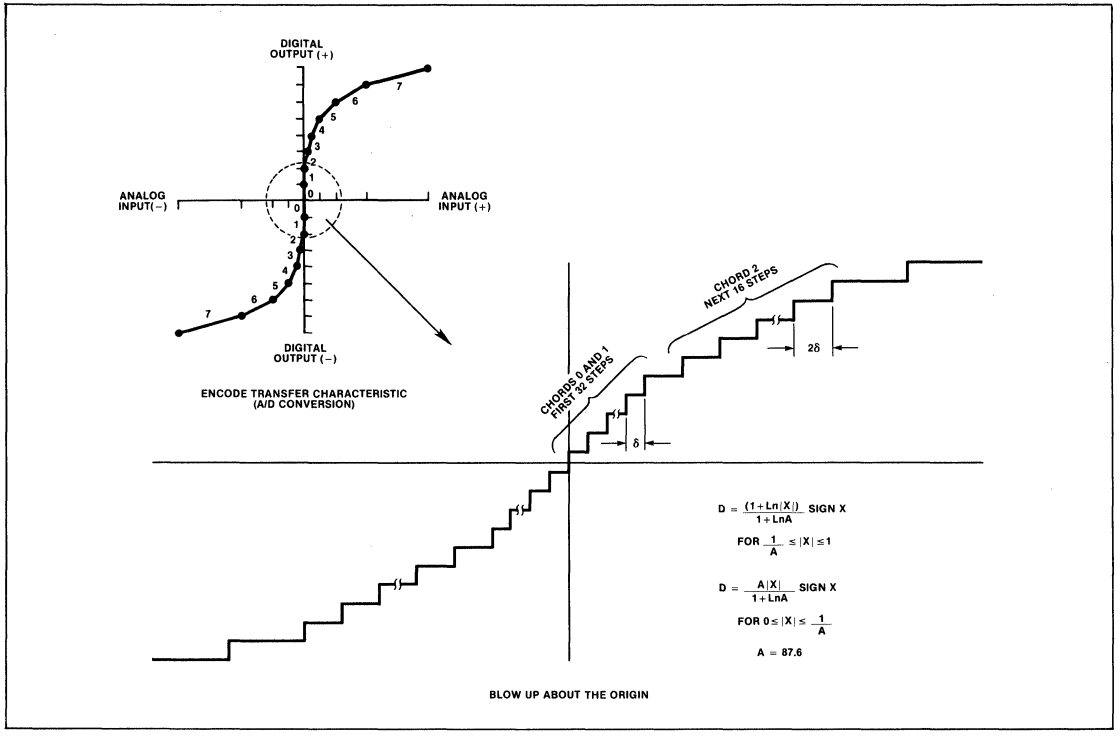


Figure 3. A-Law Transfer Function

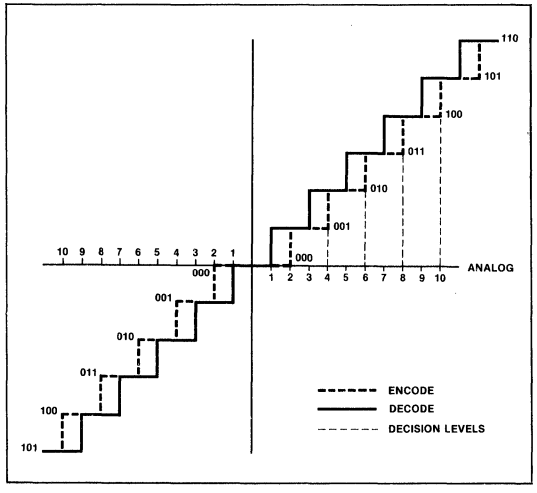


Figure 4. μ-Law Encode/Decode Characteristics About the Origin

cessive approximation feedback loop of the encode has output levels which represent the quantizing band edges. These can be referred to as decision levels. On the other hand the DAC for the decoder has output levels which represent the mean values of the quantizing bands which must, of necessity, be centered about the decoder output values. The end result is that a DAC used for decoding must be offset one-half step from the DAC used for encoding. This situation must exist over the entire range of the CODEC. A transmission system implemented with companding DACs is shown in Figure 5.

COMDAC® SYSTEM DESCRIPTION

A block diagram of PMI's companding DAC is shown in Figure 6. A single current output DAC is used to generate outputs for either the encode or decode mode of operation.

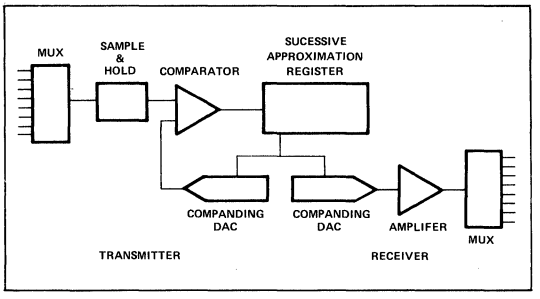


Figure 5. Transmission System Implemented with Companding DAC

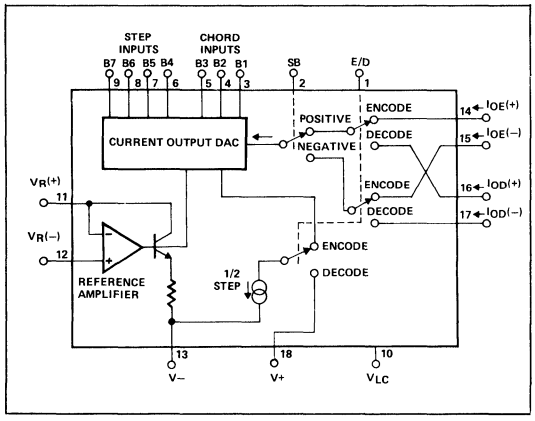


Figure 6. Equivalent Circuit and Pin Connection Diagram

Each companding DAC can be programmed to operate as either an encoder or a decoder by properly programming the E/D pin. The encode mode is offset one-half step from the decode mode by means of the current generator which is switched in during the encode mode. The reference amplifier establishes the current reference for the current output DAC. The sign bit pin (SB) controls the positive-negative switch which directs the output of the current output DAC.

This output will eventually end up at the positive (I_{OE+} or I_{OD+}) outputs or the negative (I_{OE-} or I_{OD-}) outputs depending on whether the SB pin is programmed to a binary "1" or a binary "0". The encode-decode switch E/D determines whether the DAC output shall be directed to the encode or decode terminations as shown in Figure 6. In addition, this same switch introduces the one-half step of offset current required during encode.

A better understanding of the COMDAC® circuitry is obtained by reviewing the previously discussed piece-wise linear approximation of the companding DAC transfer function to the desired μ-law or A-law transfer functions. Each chord or segment consists of 16 steps numbered from 0 to 15. The size of the steps double in size from one chord to the next as the number of the chord increases. The chords are numbered 0 to 7. In order to smooth out the characteristics during the transition from one chord to the next, the step current for step 0 of each chord is 1-1/2 times larger than the current of the highest step of the chord immediately preceding it. The succeeding 15 steps (steps 1 to 15) are then two times the size of the steps of this previous chord. These characteristics can be examined in Figure 7.

To implement the transfer function, the first chord (N = 0) uses 16 equal steps each of whose size, I_0 is 1/16 of chord current source I_{C0} for A-law, or 1/16.5 of current source I_{C0}

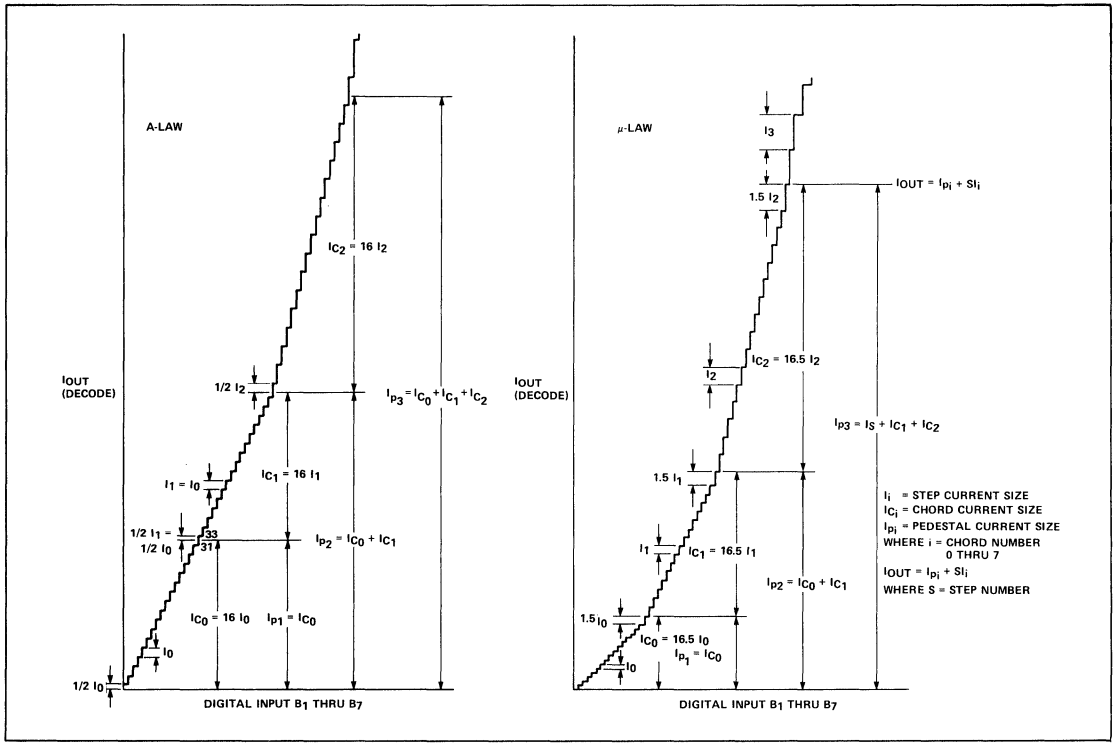


Figure 7. Construction of the Companding DAC Transfer Function

for μ-law. The next chord, N = 1, must begin at $I_{C0} + 1.5I_0$ for both A-law or μ-law. Another way of saying this is that chord N = 1 begins 16.5 steps from the origin. In order to accomplish this a pedestal current must be directed toward the output whose magnitude is equal to $I_{C0} + 1.5I_0$. Chord C2 begins at $I_{C0} + 1.5I_0 + I_{C1} + 1.5I_1$ and ends at $I_{C0} + 1.5I_0 + I_{C1} + 1.5I_1 + I_{C2} + 1.5I_2$ and so forth. This process continues with pedestal currents for each chord number N described by the equation:

$$I_{PN} = \sum_{i=0}^{N-1} (I_{Ci} + 1.5I_i) = 16.5 \sum_{i=0}^{N-1} I_i$$

note that $I_{PO} = 0$.

A functional diagram of a companding DAC which implements the proper transfer function discussed above is shown in Figure 8, which operates in the following manner: the reference amplifier sets the bias current for the chord generator by means of I_{C7} which is a current mirror whose output is equal to $2I_{REF}$. Next, due to the operation of an R–2R ladder which is described in a following paragraph, I_{C6} is made equal to one-half I_{C7} and is therefore equal to I_{REF}. I_{C5} is made equal to one-half I_{C6} and so forth. From I_{C3} down to I_{C0} a slave ladder is used rather than an R–2R ladder but the results are the same. The chord currents double in size progressing from I_{C0} to I_{C7} respectively (for A-law however $I_{C1} = I_{C0}$). The chord selector is programmed from the 1 of 8 decoder so that the chord identified by binary chord number N on leads B_1 to B_3 will switch I_{CN} to the step generator. All other chord currents are switched to the pedestal selector. The pedestal selector is programmed from the same 1 of 8 chord decoder such that chords I_0 to I_{N-1} are switched to the pedestal selector output in order to generate pedestal current I_{PN}. All other chord currents are switched to ground so that a pedestal current equal to the sum of the chord currents from I_{C0} to $I_{C(N-1)}$ will be directed to the output current switch matrix as I_{PN}. The I_{CN} flowing into the chord selector from the step generator is equal to 16.5 step currents (16.0 steps for A-law) where a step current is equal to the current step caused by changing the least significant bit in the chord of interest. Note that this satisfies the requirement of the equation for pedestal current I_{PN}. The step generator has the ability to sum current I_E into the output mode to provide the one-half step offset required when the system is operating in the encode mode. This one-half step offset current is controlled by the E/D pin. The system is in the encode mode when the E/D pin is biased to a binary "1".

DETAILED CIRCUIT DESCRIPTION

All of the single pole double throw switches in Figure 8 are constructed of bipolar emitter coupled transistors. One such switch is shown as an example in Figure 9. When the

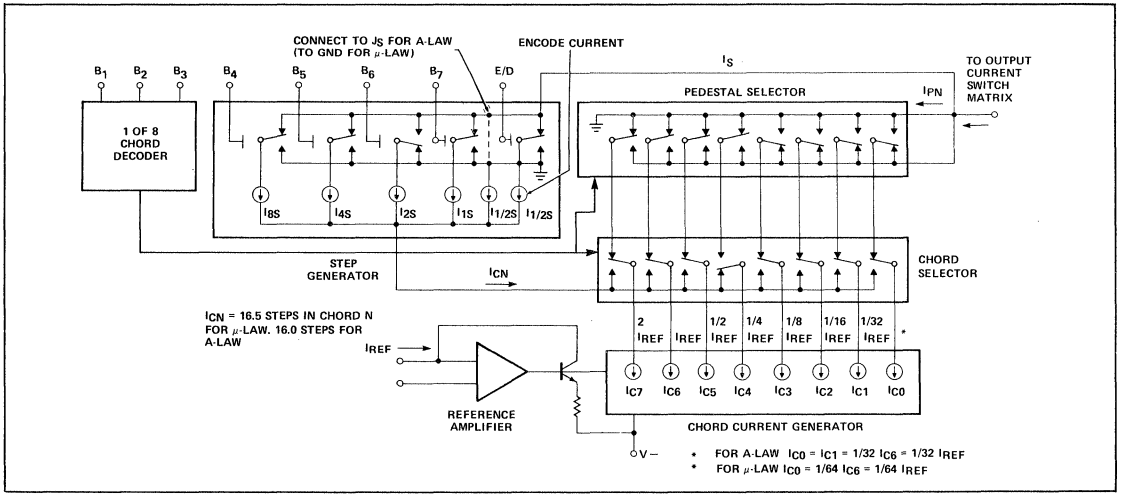


Figure 8. COMDAC® Companding DAC Functional Diagram

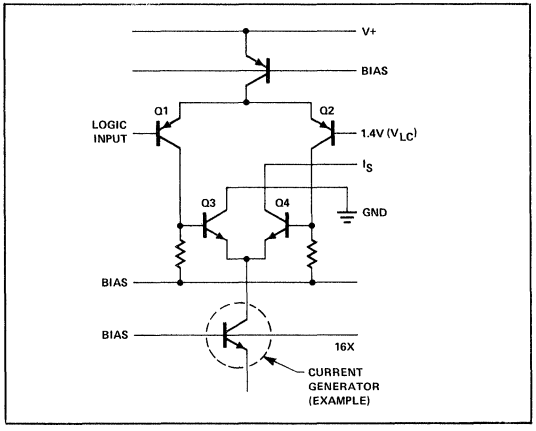


Figure 9. Double Pole Double Throw Switch Implemented with Emitter Coupled Transistors

logic input exceeds the logic level bias V_{LC} Q_1 is turned off and Q_2 is turned on. In turn Q_3 is turned off and Q_4 is turned on thus effectively switching the current generator, shown as an example, from the ground to I_S. Conversely, lowering the logic level input below V_{LC} will switch the current from I_S to ground. The V_{LC} Control permits the circuit to interface with a large range of logic levels.

The chord current generator circuit is shown in Figure 10. This circuit is the implementation of the chord current generator previously discussed. Q_0 is forced to operate at the reference input current I_{REF} and Q_1, with an emitter resistor one-half the size of the emitter resistor of Q_0, will then operate at $2I_{REF}$. Q_2 through Q_4 will operate at progressively smaller currents where each transistor operates at one-half the current of the transistor to its immediate left. To review this normal R−2R current-ladder function notice that Q_{4A} and Q_{4B} operate at equal currents and that the sum of their currents is equal to that of one transistor with an emitter resistor equal to R. When the series resistor R is added to the junction of the emitter resistors of Q_{4A} and Q_{4B} the current of Q_3 will be forced to equal the sum of the Q_{4A} and Q_{4B} currents. Thus Q_{4A} current equals one-half the Q_3 current. Now the current from Q_{4A}, Q_{4B} and Q_3 must all flow through the next series resistor R. This current is equal to twice that of Q_3; therefore it is easy to compute that the Q_2 current is twice that of the Q_3. The same reasoning may be used to proceed down the ladder to show that each transistor in the ladder sinks twice the current of the transistor on its immediate right. The slave ladder consisting of Q_5 through Q_{8A} and Q_{8B} continues to halve currents for each transistor proceeding to the right. However this part of the chord current generator uses scaled resistors instead of the R−2R ladder technique. Since Q_{4B} sinks constant current from the slave ladder, and since all the current must flow through the scaled emitter resistors, then the curent through each transistor must be inversely proportional to the size of its emitter resistor. By examination of the slave ladder it can be seen that each transistor proceeding to the right sinks one-half the current of the transistor to its immediate left. For the μ-law chord current generator Q_{8B} is simply diode connected such that the chord current for chord C_0 is roughly one-half the current of chord C_1. For the A-law chord current generator, however, the collectors of transistors Q_{8A} and Q_{8B} are tied together so that I_{C0} is exactly equal to I_{C1}. The currents flow to the chord current generator from an array of bipolar single pole double throw switches labeled "chord selector" in Figure 8. The actual switches are not shown in this paper.

The Step Current Generator is shown in Figure 11. Again the single pole double throw switches which connect the step generator to the output current matrix as shown in the companding DAC functional diagram are not represented. The step generator is connected to the chord selector which sinks I_{CN}. Ratioed emitters are used to divide the current. The largest emitter is 16 times the size of the smallest emitter and therefore sinks 16 times the current. The A-law step generator differs from the μ-law step generator in that each chord begins with a riser instead of a step. This also applies to the origin, therefore one-half step of current flows (decode mode) even when the binary input to the step generator is "0". Step switches controlled directly by the binary code connect the appropriate collectors of the step current generator transistors to the output current matrix. For both A-law and μ-law devices I_{CN} is one of the pedestal currents. The difference is that for the A-law device the pedestal current is equal to 16 steps whereas, for the μ-law, the pedestal current is equal to 16.5 steps.

NORMALIZED COMPANDING DAC OUTPUTS

It is convenient to generate tables of normalized values which correspond exactly to the CCITT (Consultive Committee for International Telephone and Telegraph) specifications. The following tables are normalized to the smallest DAC output which is equivalent to one-half step.

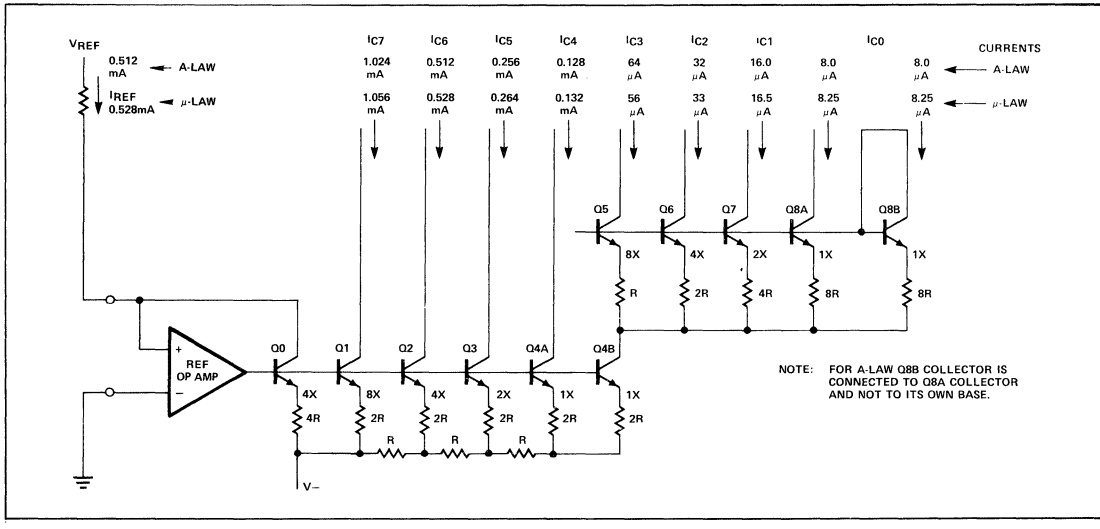


Figure 10. Chord Current Generator Diagram

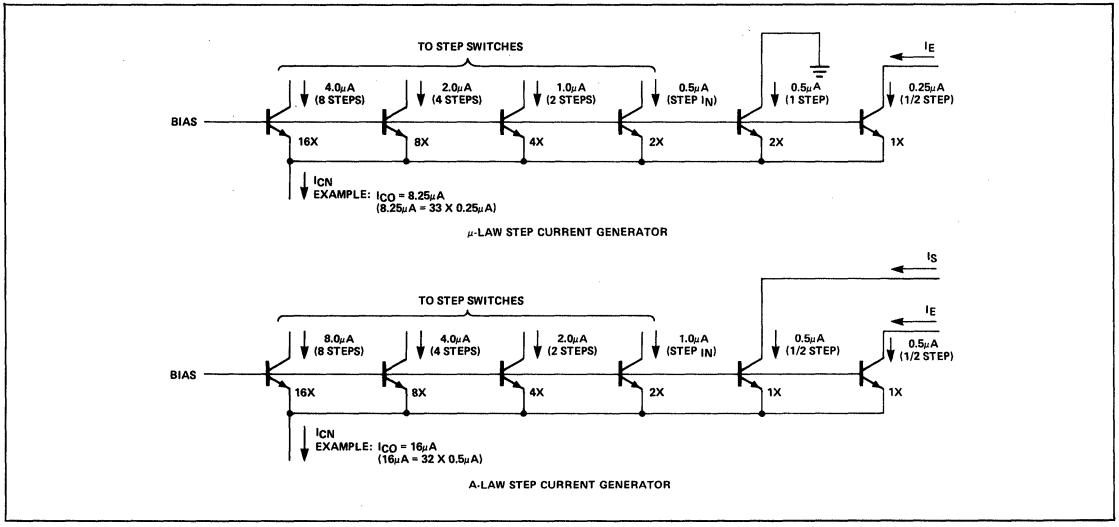


Figure 11. A-Law and μ-Law Step Current Generators

μ-Law Normalized Table

NORMALIZED DECODE OUTPUT (SIGN BIT EXCLUDED) $I_{C,S} = 2[2^C (S + 16.5) - 16.5]$

C = chord no. (0 through 7)
S = step no. (0 through 15)

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	33	99	231	495	1023	2079	4191
1	0001	2	37	107	247	527	1087	2207	4447
2	0010	4	41	115	263	559	1151	2335	4703
3	0011	6	45	123	279	591	1215	2463	4959
4	0100	8	49	131	295	623	1279	2591	5215
5	0101	10	53	139	311	655	1343	2719	5471
6	0110	12	57	147	327	687	1407	2847	5727
7	0111	14	61	155	343	719	1471	2975	5983
8	1000	16	65	163	359	751	1535	3103	6239
9	1001	18	69	171	375	783	1599	3231	6495
10	1010	20	73	179	391	815	1663	3359	6751
11	1011	22	77	187	407	847	1727	3487	7007
12	1100	24	81	195	423	879	1791	3615	7263
13	1101	26	85	203	439	911	1855	3743	7519
14	1110	28	89	211	455	943	1919	3871	7775
15	1111	30	93	219	471	975	1983	3999	8031
STEP SIZE		2	4	8	16	32	64	128	256

μ-Law Normalized Tables

NORMALIZED ENCODE LEVEL (SIGN BIT EXCLUDED) $I_{C,S} = 2[2^C (S + 17) - 16.5]$

C = chord no. (0 through 7)
S = step no. (0 through 15)

STEP \ CHORD		0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	1	35	103	239	511	1055	2143	4319
1	0001	3	39	111	255	543	1119	2271	4575
2	0010	5	43	119	271	575	1183	2399	4831
3	0011	7	47	127	287	607	1247	2527	5087
4	0100	9	51	135	303	639	1311	2655	5343
5	0101	11	55	143	319	671	1375	2783	5599
6	0110	13	59	151	335	703	1439	2911	5855
7	0111	15	63	159	351	735	1503	3039	6111
8	1000	17	67	167	367	767	1567	3167	6367
9	1001	19	71	175	383	799	1631	3295	6623
10	1010	21	75	183	399	831	1695	3423	6879
11	1011	23	79	191	415	863	1759	3551	7135
12	1100	25	83	199	431	895	1823	3679	7391
13	1101	27	87	207	447	927	1887	3807	7647
14	1110	29	91	215	463	959	1951	3935	7903
15	1111	31	95	223	479	991	2015	4063	8159
STEP SIZE		2	4	8	16	32	64	128	256

A-Law Normalized Tables

NORMALIZED DECODE OUTPUT (SIGN BIT EXCLUDED)

$I_{CS} = 2^{N-1} (33 + 2S)$ For $N > 0$
$I_{CS} = 2S + 1$ For $N = 0$

STEP \ CHORD		0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	1	33	66	132	264	528	1056	2112
1	0001	3	35	70	140	280	560	1120	2240
2	0010	5	37	74	148	296	592	1184	2368
3	0011	7	39	78	156	312	624	1248	2496
4	0100	9	41	82	164	328	656	1312	2624
5	0101	11	43	86	172	344	688	1376	2752
6	0110	13	45	90	180	360	720	1440	2880
7	0111	15	47	94	188	376	752	1504	3008
8	1000	17	49	98	196	392	784	1568	3136
9	1001	19	51	102	204	408	816	1632	3264
10	1010	21	53	106	212	424	848	1696	3392
11	1011	23	55	110	220	440	880	1760	3520
12	1100	25	57	114	228	456	912	1824	3648
13	1101	27	59	118	236	472	944	1888	3776
14	1110	29	61	122	244	488	976	1952	3904
15	1111	31	63	126	252	504	1008	2016	4032
STEP SIZE		2	2	4	8	16	32	64	128

A-Law Normalized Table

NORMALIZED ENCODE DECISION LEVELS (SIGN BIT EXCLUDED)

$I_{CS} = 2^{N-1}(34 + 2S)$ For $N > 0$
$I_{CS} = 2S + 2$ For $S = 0$

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	2	34	68	136	272	544	1088	2176
1	0001	4	36	72	144	288	576	1152	2304
2	0010	6	38	76	152	304	608	1216	2432
3	0011	8	40	80	160	320	640	1280	2560
4	0100	10	42	84	168	336	672	1344	2688
5	0101	12	44	88	176	352	704	1408	2816
6	0110	14	46	92	184	368	736	1472	2944
7	0111	16	48	96	192	384	768	1536	3072
8	1000	18	50	100	200	400	800	1600	3200
9	1001	20	52	104	208	416	832	1664	3328
10	1010	22	54	108	216	432	864	1728	3456
11	1011	24	56	112	224	448	896	1792	3584
12	1100	26	58	116	232	464	928	1856	3712
13	1101	28	60	120	240	480	960	1920	3840
14	1110	30	62	124	248	496	992	1984	3968
15	1111	32	64	128	256	512	1024	2048	*4096
STEP SIZE		2	2	4	8	16	32	64	128

The numbers in these tables are directly proportional to the input reference current. However the exact relationship is somewhat complicated. A reference current of 528μA for the μ-law DAC will produce a step size of 0.5μA thus, for the μ-law device driven by a reference current of 528μA, it is only necessary to multiply all the numbers in the normalized tables by one-half step or 0.25μA to obtain the output in μA. The table tabulated below corresponds to a 528μA reference.

μ-Law Current Output Table

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS (SIGN BIT EXCLUDED)

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	8.25	24.75	57.75	123.75	255.75	519.75	1047.75
1	0001	0.5	9.25	26.75	61.75	131.75	271.75	551.75	1111.75
2	0010	1	10.25	28.75	65.75	139.75	287.75	583.75	1175.75
3	0011	1.5	11.25	30.75	69.75	147.75	303.75	615.75	1239.75
4	0100	2	12.25	32.75	73.75	155.75	319.75	647.75	1303.75
5	0101	2.5	13.25	34.75	77.75	163.75	335.75	679.75	1367.75
6	0110	3	14.25	36.75	81.75	171.75	351.75	711.75	1431.75
7	0111	3.5	15.25	38.75	85.75	179.75	367.75	743.75	1495.75
8	1000	4	16.25	40.75	89.75	187.75	383.75	775.75	1559.75
9	1001	4.5	17.25	42.75	93.75	195.75	399.75	807.75	1623.75
10	1010	5	18.25	44.75	97.75	203.75	415.75	839.75	1687.75
11	1011	5.5	19.25	46.75	101.75	211.75	431.75	871.75	1751.75
12	1100	6	20.25	48.75	105.75	219.75	447.75	903.75	1815.75
13	1101	6.5	21.25	50.75	109.75	227.75	463.75	935.75	1879.75
14	1110	7	22.25	52.75	113.75	235.75	479.75	967.75	1943.75
15	1111	7.5	23.25	54.75	117.75	243.75	495.75	999.75	2007.75
STEP SIZE		.50	1	2	4	8	16	32	64

*Virtual Decision Level

A similar exercise will yield a corresponding table for the A-law part. Multiplying all the numbers in the normalized A-law table, for instance, will produce a table of currents for a reference input of 512μA. A table based on 512μA reference current will have a step size of 1.0μA and is tabulated in the μ-law current output table.

A-Law Current Output Table

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS (SIGN BIT EXCLUDED)

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0.5	16.5	33	66	132	264	528	1056
1	0001	1.5	17.5	35	70	140	280	560	1120
2	0010	2.5	18.5	37	74	148	286	592	1184
3	0011	3.5	19.5	39	78	156	312	624	1248
4	0100	4.5	20.5	41	82	164	328	656	1312
5	0101	5.5	21.5	43	86	172	344	688	1376
6	0110	6.5	22.5	45	90	180	360	720	1440
7	0111	7.5	23.5	47	94	188	376	752	1504
8	1000	8.5	24.5	49	98	196	392	784	1568
9	1001	9.5	25.5	51	102	204	408	816	1632
10	1010	10.5	26.5	53	106	212	424	848	1696
11	1011	11.5	27.5	55	110	220	440	880	1760
12	1100	12.5	28.5	57	114	228	456	912	1824
13	1101	13.5	29.5	59	118	236	472	944	1888
14	1110	14.5	30.5	61	122	244	488	976	1952
15	1111	15.5	31.5	63	126	252	504	1008	2016
STEP SIZE		1	1	2	4	8	16	32	64

Reviewing the companding DAC functional diagram Figure 8 demonstrates the relationship between step size and I_{REF}. For a μ-law device I_{C0} equals 16.5 chord zero steps and for an A-law device I_{C0} equals 16 chord zero steps. I_{C6} is always equal to I_{REF} in either system. I_{C6} is then equal to 64 times I_{C0} for a μ-law system, and 32 times I_{C0} for an A-law system. The step size can then be related to I_{REF} by the following equations:

$$\text{step size} = I_{REF}/64 \times 16.5 = I_{REF}/1056 \text{ (μ-law)}$$
$$\text{step size} = I_{REF}/32 \times 16 = I_{REF}/512 \text{ (A-law)}$$

Now for a reference current of 528μA the step size for a μ-law system is 528/1056 or 0.5μA. For a reference current of 512μA the step size for an A-law system is 512/512 or 1.0μA. These values concur with those used to generate the tables.

In the design of the PMI DAC-87 the biasing resistors were not scaled to exactly integer values. This was done deliberately to standardize somewhat on 528μA input reference current for both A-law and μ-law parts. The performance of the device is not affected, however the actual scaling is somewhat complicated and will not be discussed in this paper.

Finally if encode output tables were desired for current output they could be obtained by scaling to proper step size the normalized encode tables or adding one-half step to each value in the decode table, where the step size depends on the chord number.

DAC ACCURACY

Companding DACs must be manufactured to satisfy a unique set of parameters. The performance of a companded DAC used for telephony must satisfy the requirements of a communication system on an end-to-end basis. A voice channel is first encoded by one CODEC then decoded by a second CODEC such that the system performance can be measured on an audio-in-audio-out basis. The CODEC performance will be almost completely dominated by the Gain Tracking requirement.

GAIN TRACKING

Gain Tracking refers to the ability of a system to track its input power level. The test is normally made with a system such as that shown in Figure 12.

Gain Tracking is measured by monitoring the input and output levels in decibels. At an input level of −10Bm0 the output is recorded as the output reference level. For ideal Gain Tracking, any change (in dB) of the input level must be matched exactly by the same change in the output level.

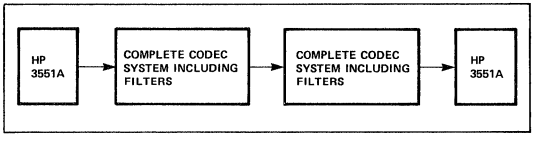


Figure 12. Gain Tracking or S/N Test

This condition is monitored over all input power levels of interest. The extent to which these power level changes differ (again in dB) is a measure of Gain Tracking, also referred to as gain deviation. The ATT/D3 Gain Tracking specification is show in Figure 13.

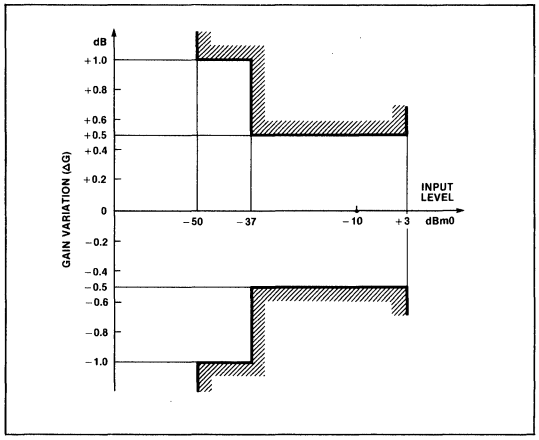


Figure 13. ATT/D3 Gain Tracking Specification

CCITT publishes two separate specifications for Gain Tracking. The apparatus used for making either of these tests is basically the same as that used in Figure 13 except that for the first part of the "method one" test the HP3551A would be replaced with a suitable white noise source at the input and an RMS reading voltmeter at the output. Gain Tracking masks equivalent to those found in CCITT publications are shown in Figure 14.

POWER LEVELS

For PCM channel performance measurements, power levels are characteristically expressed in dBm0. A reference level of 0dBm0 is established by referencing to a code in the **digital** transmission. The binary code pattern required to establish a reference level of 0dBm0 can be found in the CCITT publications. This pattern is reproduced in the PMI Telecommunications Handbook for the readers convenience. The constant repetition of these binary numbers at the normal sampling rate of 8kHz will produce a 1kHz sinusoid at a 0dBm0 reference level. Starting with this definition it can then be shown that a sinusoid whose peak value is just at the system saturation level (all "1s" PCM output) will have a power level of 3.14 and 3.17dBm0 for A-law and μ-law respectively.

SIGNAL-TO-DISTORTION MEASUREMENTS

Signal-to-Distortion is a measure of the total distortion a system will exhibit on an end-to-end basis. As with Gain Tracking this measurement is normally performed on an audio-to-audio basis. A typical setup for measuring Signal-to-Distortion is shown in Figure 15. A wideband (3kHz) filter may be substituted for the C-Message filter shown for some tests.

Figure 16 shows the ATT/D3 specification mask with the performance of a PMI demonstration COMDAC® based shared CODEC system superimposed. This method of measuring Signal-to-Distortion is applicable to either CCITT or ATT specifications.

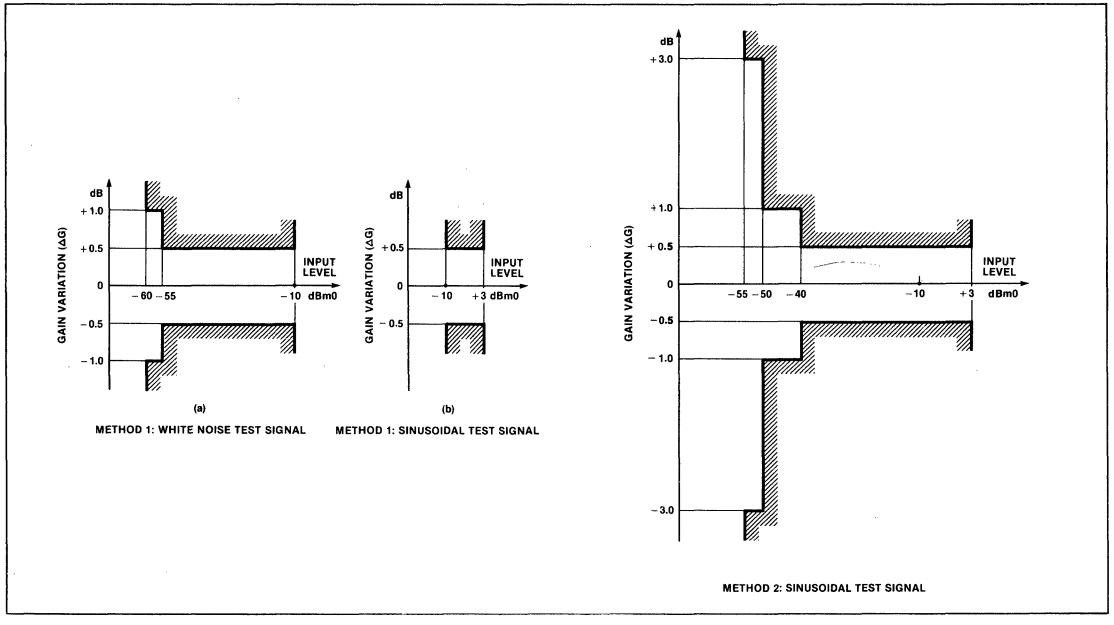


Figure 14. CCIT Gain Tracking Specification

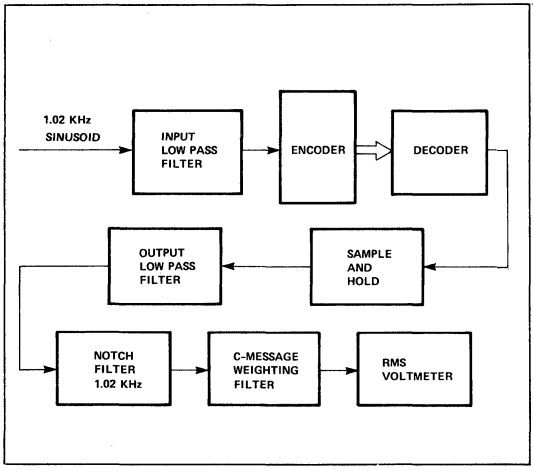


Figure 15. Signal-to-Distortion Test Setup

DAC ACCURACY VERSUS GAIN TRACKING AND SIGNAL-TO-DISTORTION RATIO

The analog portions of a PCM system usually make only a minor contribution to either Gain Tracking or Signal-to-Distortion errors. Thus, the major contribution to error is the inability of the companding DAC to accurately follow the encoding format. The process of quantizing and coding will cause some deviation from the ideal, however the errors made by the ideal CODEC system will be well within telephony specifications. To conform to the required Gain Tracking and Signal-to-Distortion specifications the DAC output currents must conform as closely as possible to the ideal transfer function as tabulated in the normalized tables. This corresponds to a specification of absolute error on the DAC output current with respect to its binary inputs. The DAC-86/87 companded DACs are guaranteed to plus or minus one-fourth step from ideal values in chord zero and to plus or minus one-half step elsewhere. This information can be transformed into tabular form by adding the allowable error to the DAC tables. Either the normalized tables or the current output tables can be used as a basis for this exercise.

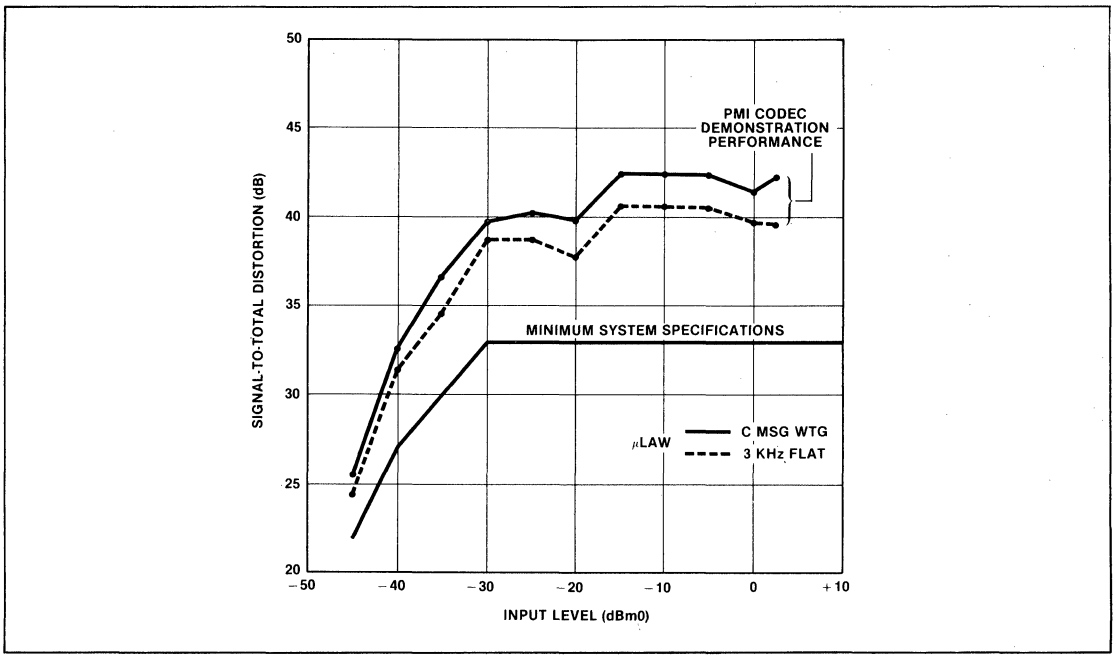


Figure 16. ATT/D3 Signal-to-Distortion Mask

APPLICATION NOTE 40

A BUFFER APPLICATIONS COLLECTION

by Shelby D. Givens

INTRODUCTION

This Application Note consists of a collection of circuits which apply buffers to the solutions of a variety of problems. As will be shown, buffers may be used to make filters, current sources, cable drivers, sample and holds, high speed instrumentation amplifiers, line drivers for multiplexers, current boosters for voltage references, and high speed voltage output DACs.

INDUCTORS AND FILTERS

The active inductor in Figure 1 is realized with an eight-lead IC, two carbon resistors, and a small capacitor. A commercial inductor of 50 henries may occupy up to five cubic inches.

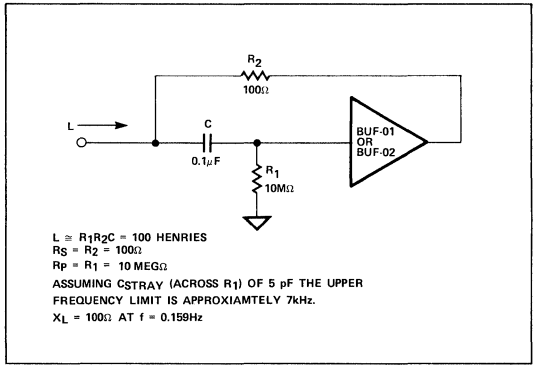


Figure 1. Active Inductor

The tuned circuit shown in Figure 2 uses the simulated inductor of Figure 1 (R_1, R_2, C_1) and C_2. Depending upon whether the circuit is driven at E_1 or E_2 the responses of Figures 3 or 4 result. The resonant response in both cases is

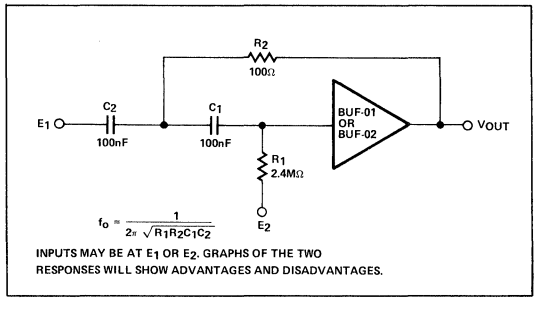


Figure 2. Tuned Circuit

+ 38dB at 103Hz. The Figure 3 response is + 2.5dB at 200Hz and − 10dB at 50Hz. On the other hand, the Figure 4 response is − 9dB at 200Hz and + 2.5dB at 50Hz.

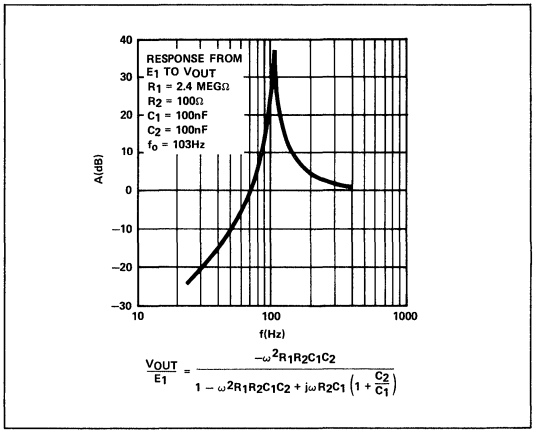


Figure 3. Response from E_1 to V_{out}

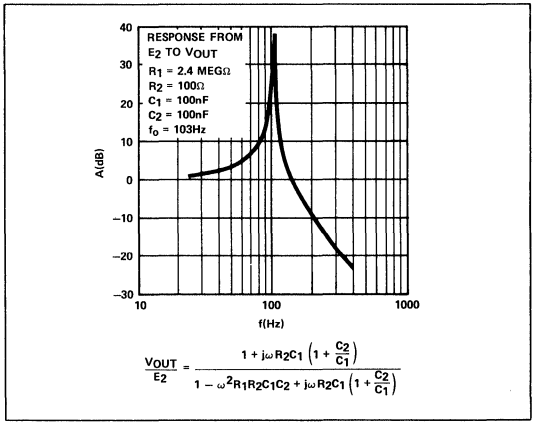


Figure 4. Response from E_2 to V_{out}

Figure 5 shows a low pass filter realized for f_o of 1MHz. What is remarkable about this filter is most ICs do not have the full power bandwidth to handle 1MHz signals in the 5 to 10 Volt range, while the BUF-03 has a greater than 4MHz full power bandwidth for a $20V_{p-p}$ sinewave. Similar comments apply to the filter in Figure 6. In other words, the extreme bandwidth of the BUF-03 extends the bandwidth capability of certain classes of active filters.

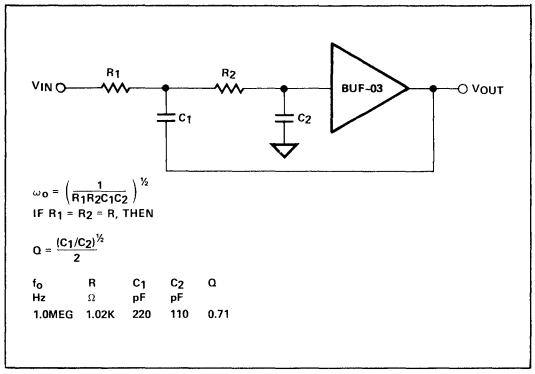
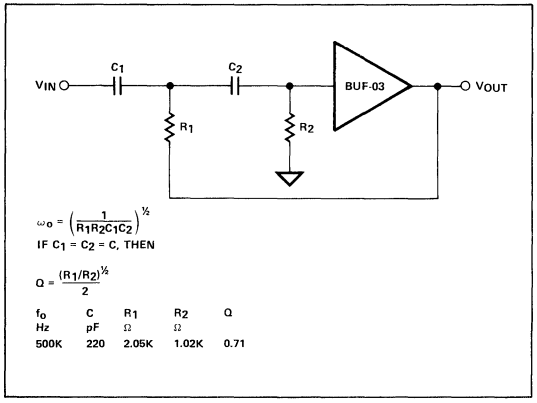


Figure 5. Low Pass Filter (High Frequency)



Figrue 6. High Pass Filter (High Frequency)

The BUF-03 can be used to make a 4.5MHz trap for use in TV. This circuit is shown in Figure 7, and the elements are chosen such that no capacitor is less than 100pF.

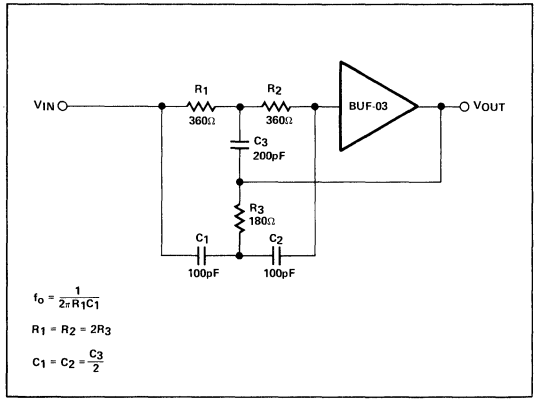


Figure 7. Notch Filter at 4.5MHz

HIGH SPEED CURRENT SOURCES

The BUF-03 in combination with an OP-16 produces a bipolar voltage-controlled current source. The circuits shown in Figures 8 and 9 were breadboarded and found to have rise times of approximately 1μsec. Since the waveforms had definite RC characteristics, layout was suspected as contributing primarily to the rise times observed. Figure 8 shows the inverting connection, while Figure 9 shows the noninverting connection.

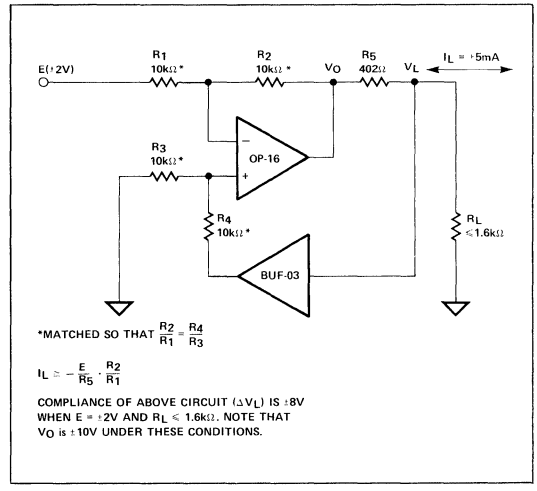


Figure 8. Inverting Bipolar Current Source (High Speed)

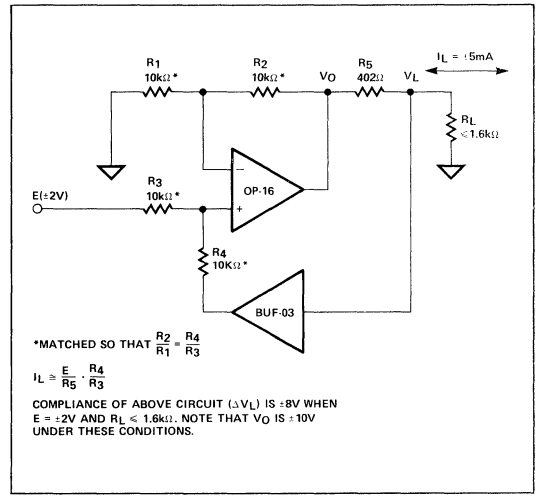


Figure 9. Noninverting Bipolar Current Source

DATA ACQUISITION SYSTEM APPLICATIONS

Because of the speed of these devices, the BUF-03 and OP-17 allow the fabrication of a high speed instrumentation amplifier as shown in Figure 10. The output of the in-

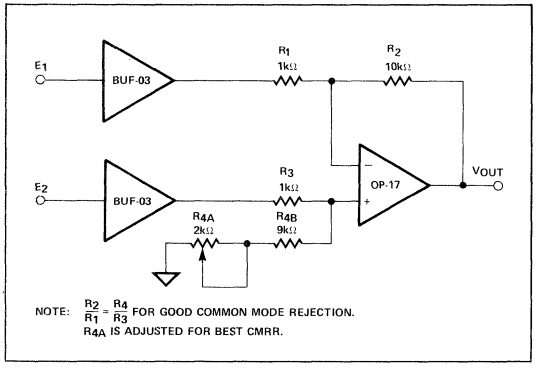


Figure 10. High Speed Instrumentation Amplifier

strumentation amplifier will likely be multiplexed onto a common data line. Here the BUF-02 or BUF-03 can be used as the data line drivers because of their speed and current capabilities. The connection for this application is shown in Figure 11. The realization of a high speed sample and hold is

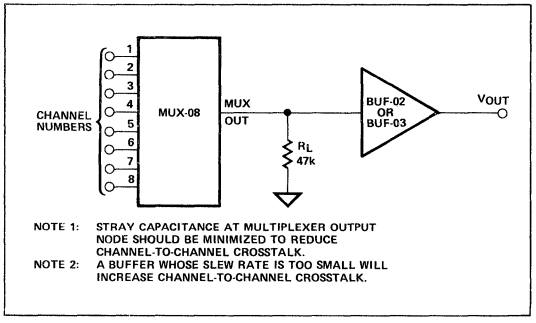


Figure 11. High Speed Line Driver for Multiplexers

possible using the BUF-03 and suitable analog switches. The circuit shown in Figure 12 provides the highest speed because there are no feedback loops to slow down the settling times. Typically the sample and hold is followed by a successive approximation analog-to-digital converter (ADC).

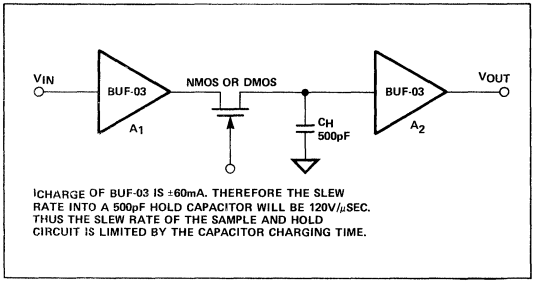


Figure 12. High Speed Sample and Hold

The BUF-01 is shown in Figure 13 as the input buffer for a 14-bit ADC. Because of its extreme accuracy, the BUF-01 can resolve ½LSB of a 10V, 14-bit system. The final applica-

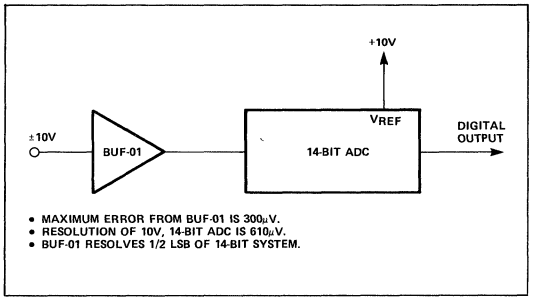


Figure 13. High Resolution ADC Input Buffer

tion involves the BUF-03 and the DAC-08 (digital-to-analog converter). Figure 14 shows how it is possible to develop both V_{out} and $\overline{V}_{out}$. The output capacitance of the DAC-08 is approximately 15pF, thus as R_0 increases in value, so does the settling time for V_{out} (and $\overline{V}_{out}$).

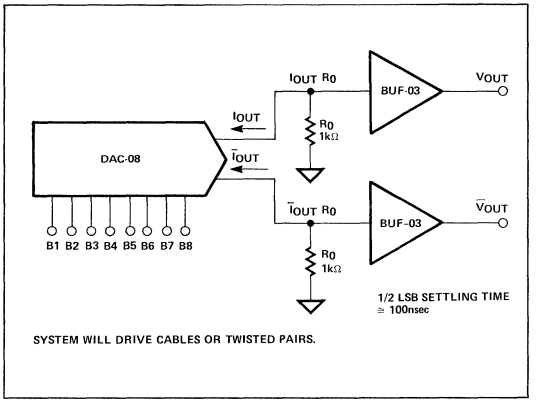


Figure 14. High Speed Voltage Output DAC

LINE DRIVER APPLICATIONS

If your BIFET "line driver" has the speed but not the stability or the current capability to drive coaxial cables, its output may be buffered with a BUF-03 as shown in Figure 15. Figure

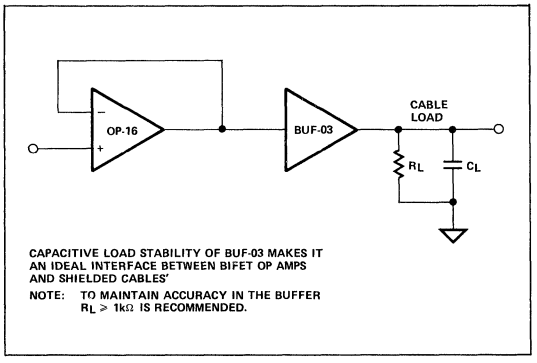


Figure 15. Convert BIFET Into Cable Driver

16 shows an alternative connection when better accuracy and more current capability is needed. Note that the limitation on R_L being greater than 1K does not apply in this case since the added error caused by lower impedances is imbedded inside the feedback loop of the op amp.

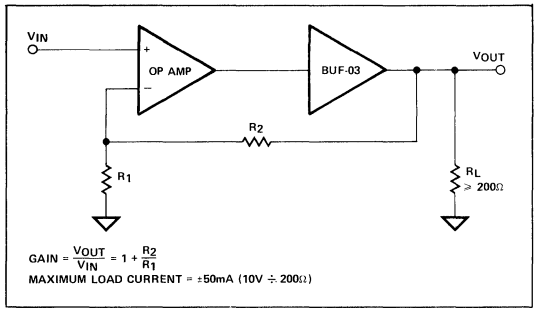


Figure 16. Current Booster

MISCELLANEOUS USES OF BUFFERS

An accurate buffer can be useful for isolating a reference zener from load fluctuations. In this way the same zener can be used in a variety of reference situations. The circuit shown in Figure 17 can supply up to 10mA (5mA for the BUF-02) to a load using a BUF-01. Single supply applications can be realized using either the BUF-02 or the BUF-03 as shown in Figure 18.

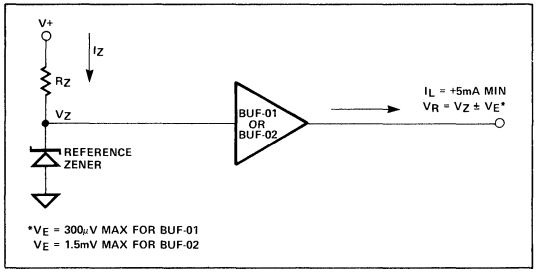


Figure 17. Buffered Voltage Reference

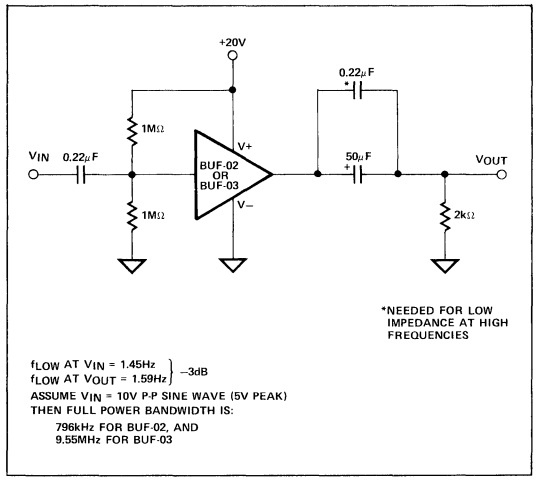


Figure 18. Single Supply AC Buffer (High Speed)

CONCLUSION

While the list is by no means all inclusive, this application note has attempted to point out some of the myriad of uses for the IC buffer. In particular, the BUF-03 makes possible a whole new class of high frequency filters and high speed current sources. Many problems in data acquisition systems can be solved by the use of buffers. In addition, the BUF-03 is useful in providing increased drive current, as well as the ability to drive long cables without instability. Finally, the versatility of the reference zener can be increased by using buffers, and for AC applications the buffer can be used on single power supplies.

APPLICATION NOTE 41

IMPROVED SHARED-CHANNEL CODEC DESIGN WITH PMI's NEW COMPANDING DACs

by B.W. Berry

DESIGNERS FACE CHOICE

Designers of telecommunications systems are faced with a fundamental design decision; they must base the design of digital voice transmission systems on either the use of a CODEC shared over several analog channels or on the use of one CODEC per channel.

Since 1976, users of PMI's shared-channel approach point to the economical advantages of a system that incorporates an encoder and a decoder capable of accommodating multiple voice channels. Proponents of single-CODEC-per-channel systems generally cite the straight-forward techniques involved in implementing this concept as the motivation for its selection.

The use of the shared-CODEC configuration is appealing because fewer integrated circuits per channel are required and less circuit board area per channel is needed. Because of its lower cost per channel and lower total system cost, the shared-channel CODEC concept looms as the logical choice for designers provided it can meet the performance needs of their systems.

Recently, new telecommunication components were introduced by Precision Monolithics Incorporated that improve the performance that can be obtained from a shared-CODEC system; the availability of these devices could influence future design decisions in favor of the shared CODEC concept over the single-CODEC approach. These newly developed devices, including the DAC-88 and the DAC-89 COMDAC® companding D/A converters, and the DMX-88 demultiplexer, not only provide performance which is superior to previously existing products, they are also easier to apply.

The degree of improvement offered by these devices and the present capabilities of a shared-CODEC system can be demonstrated using the circuit configuration shown in Figure 1. This configuration, an eight-channel digital transmission system, was designed and breadboarded by PMI as a vehicle for measuring the analog-input to analog-output transmission parameters commonly used to specify CODEC performance regardless of the particular system configuration.

Two of the components employed in the transmission system shown in Figure 1, the companding digital-to-analog converter and the analog multiplexer represent improved versions of previously existing products and are key contributors to the superior performance the system demonstrates over previous versions.

In the redesign of the companding DAC, it was felt that the best results would be achieved by improving the device's response within chord 0. Two design goals were set: to establish a reasonable settling time within chord 0 and to provide a guaranteed better than ±1/4 step linearity within that chord. Excellent results were obtained for both μ-law and A-law devices.

The new version of the companding DAC typically settles within 500ns, thus overcoming a restriction that had previously reduced the maximum number of channels for encoding. The IC's nominally settle to within ±1/8 step of the theoretical level in chord 0 and are 100% tested to be no worse than ±1/4 step.

Because of testing time restrictions, the settling time is given as a nominal specification. The guaranteed linearity specifi-

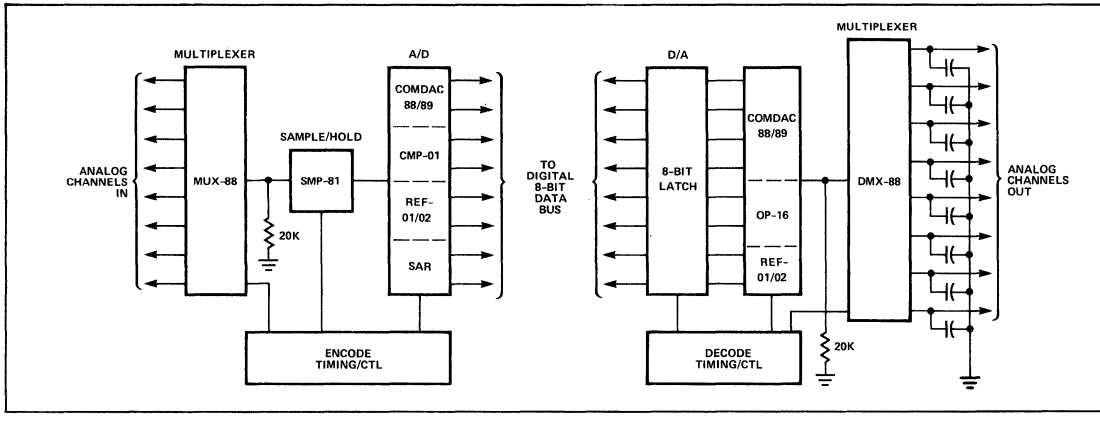


Figure 1. Eight-Channel Test Configuration.

cation, in conjunction with the nominal settling time data, can provide the designer with the data needed to determine if the performance needs of his system can be satisfied.

When the earlier version of the output multiplexer was used as a sample-and-hold and switch, it was found that certain characteristics of the device caused idle channel noise and transmission degradation. An analysis showed that reduction of the charge injected during the switch turn-off would enhance the performance of the device. The effect of the charge injection becomes important because of the capacitance added to the MUX output. This output drives a high-impedance load (the PCM filter) and without a discharge path, the charge adds to the analog output being switched through the multiplexer. Because of the use of an improved BiFET switch structure, the new multiplexer exhibits a discharged only 1/4 of 1/5 of the value for the previous device. Tests reveal that the idle channel noise is reduced by several dB when the DMX-88 is used as the output switch and sample-and-hold. In addition, the reduced amount of charge permits the use of a smaller value capacitor and thus increases the number of output channels that can be decoded.

DEMONSTRATOR MODIFICATIONS

The most obvious system improvement provided by the eight-channel system depicted in Figure 1, compared to an earlier demonstrator developed by PMI (described in the PMI application note AN-37), is a simplified encoder clocking scheme. In the original circuit, additional settling time was required because of the slower changing bits.

The new version of the clocking circuitry still employs a programmable read-only memory (PROM) for flexibility in performing future modifications and experimentation. However, the clock pattern is markedly changed. The new SAR clock timing diagram is shown in Figure 2. As can be seen, bit clocking is accomplished with a set 772 kHz clock. This

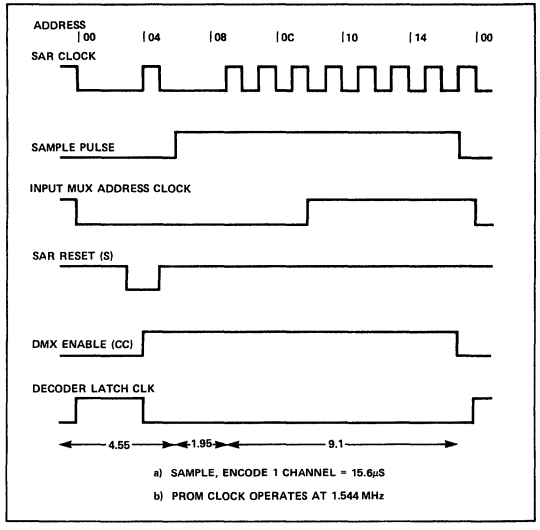


Figure 2. Encode Timing: DMX Control.

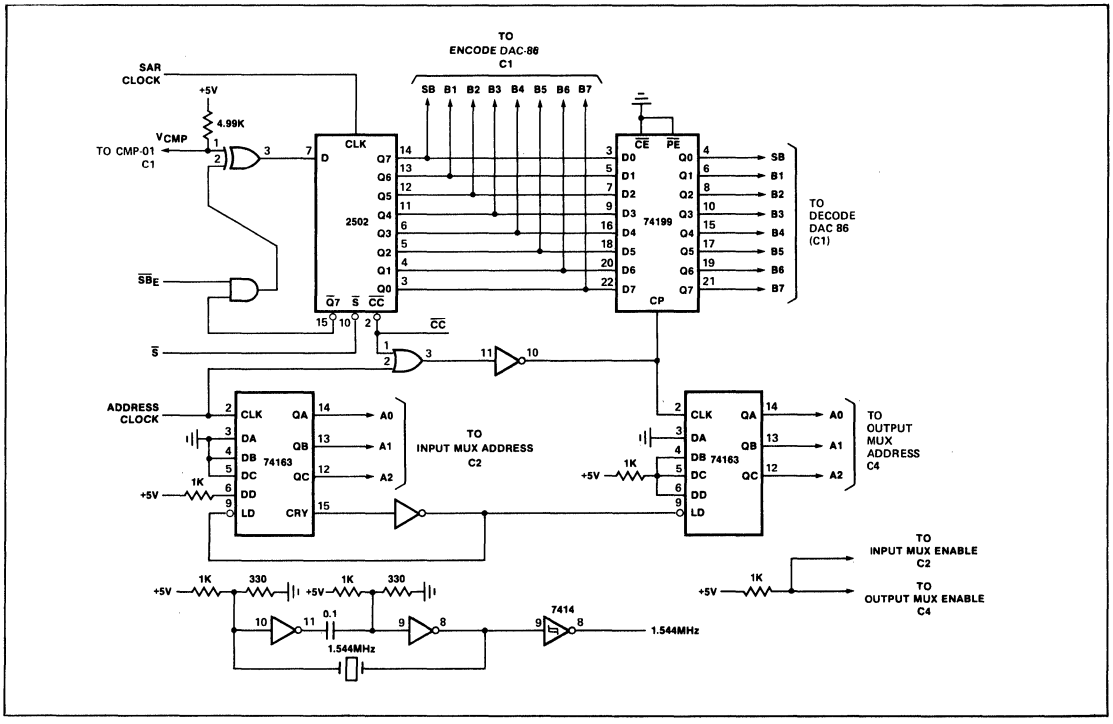


Figure 2A. Encode/Decode Controller

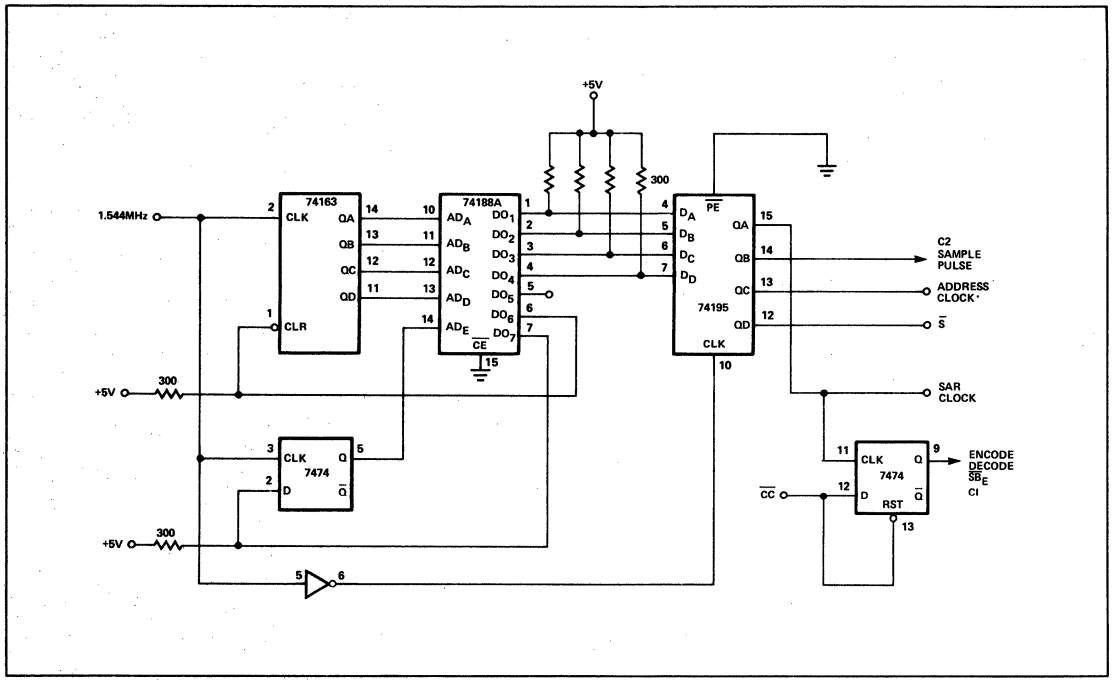


Figure 2B. Encode Clock.

allows 9.1 μs (eight-channel rate) for encoding; the remaining cycle time (6.5 μs) is used for sampling the analog signal and holding the level to be encoded. The remaining cycle time is divided as follows: sample period, 4.55 μs; transition time between the hold signal and the sign bit acquisition, 1.95 μs.

The sampling time for the new clocking scheme is longer than it was for the old design (4.5 μs as compared to 3.2 μs) and the hold settling time has increased from 0.65 to 1.95 μs. As a result, the values measured for gain tracking differential (linearity) at low input levels (-55 dBm0) provide an indication of the improved response.

Since the clocking pattern has been simplified, the number of TTL gates needed is less than had been required by the original configuration. An even simpler clocking scheme can be designed by replacing the PROM, address counter and data latch with a "D" flip-flop and some additional gates. The use of a programmable clock generator, however, was advantageous in demonstrating the effects of various circuit components on the overall transmission performance. For example, by increasing the sample time and thereby reducing the hold settling time (keeping the SAR clock the same frequency), the system tends to show different characteristics. The gain tracking stays within spec, but signal-to-total distortion increases at levels below -40dBm0. The crosstalk performance (adjacent channel) also deteriorates. Apparently both of these effects are results of the output settling of the sample-and-hold device. The point is that by designing with a system consisting of individual devices the user can more precisely determine those components that have the greatest effect on system characteristics. The design can then be adapted to maximize certain performance attributes in lieu of other, less-important characteristics. The system as finalized in these notes is a compromise system, one aimed at providing adequate performance in various applicaitons. The final design modifications are left up to the individuals responsible for the specific systems.

In terms of differences between using the older DAC-86/87 and the new designs (88/89), the requirements actually differ only slightly. Both new devices (88/89) now have idle currents present on the selected output leads; these currents are equal on both the positive and negative outputs and are normally around 10μA. However, since both leads have equal values, the effect on the output device is essentially zero change. The power dissipation is slightly higher for both parts, but less than 8mW per channel in a eight-channel design. The DAC-89EX is now specified at a lower reference current than the DAC-86/87 or DAC-88. The new reference is 16μA less than the original value. The tests described here were performed with constant reference current for both the DAC-88 and the DAC-89. The effect on the A-law measurements means the full-scale output is 2079μA instead of 2016μA. Although all steps are slightly expanded, for the purpose of the data collected here the reference current difference is negligible.

The normal testing configuration used was to provide a test signal input in one channel and monitor the output of that channel (or adjacent channels for crosstalk) with a PCM receive filter and the prescribed receiver. The test diagram is

shown in Figure 3. It becomes important to ground all unused encoder inputs to provide the proper termination. It also is very important when laying out system boards to generate sufficient ground planes and proper isolation between analog and digital ground areas. The common point of these ground areas should be as close to the power supply as possible. Also "daisy-chaining" of ground returns should be avoided. Careful consideration of grounding can help improve all system parameters.

The transmission test results collected with this system are shown in Figures 4 through 6. An example of results with a different clock pattern is also presented. The improvement in the redesigned DAC's becomes evident in Figures 7 and 8, which show the faster encoder clock driving the older DAC-86 and 87 components.

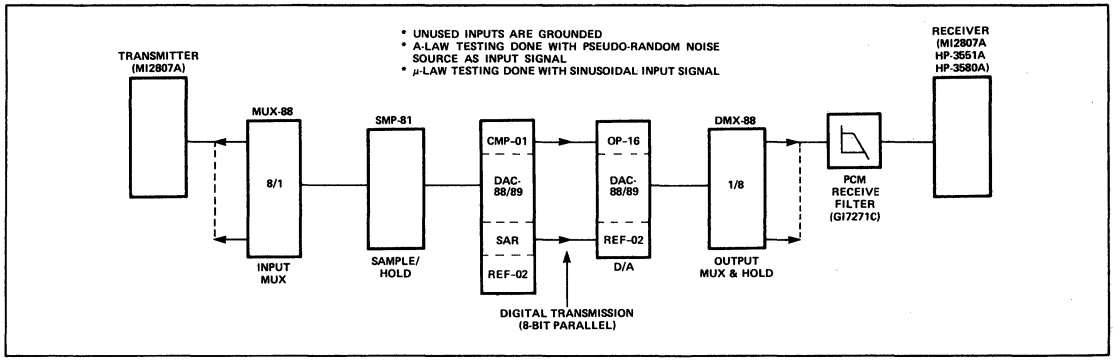


Figure 3. Test Configuration.

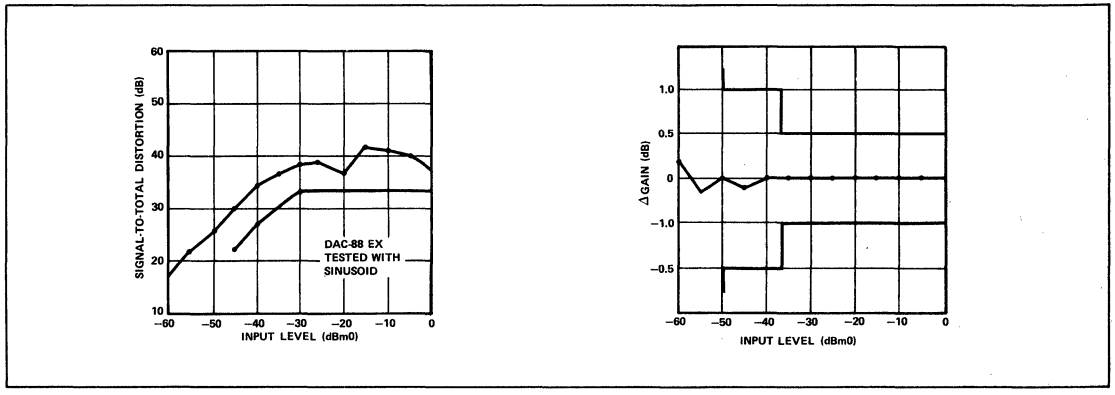


Figure 4. DAC-88EX Tested with Sinusoid.

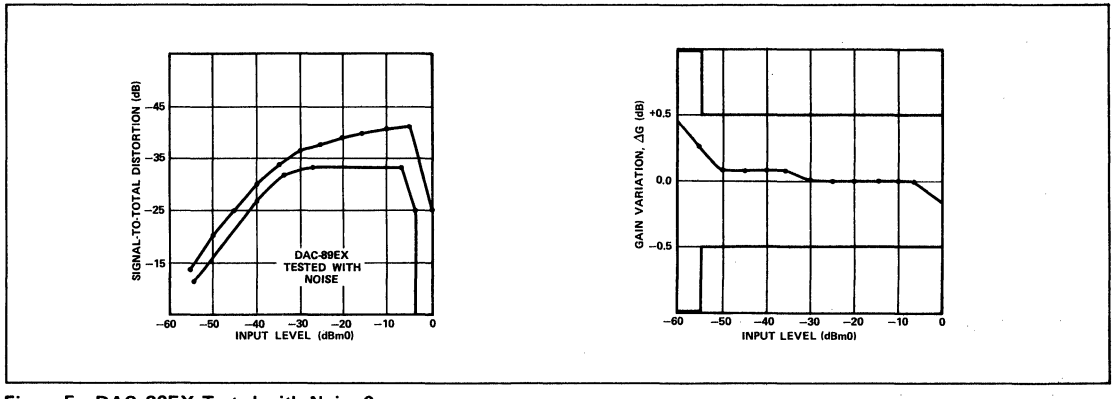


Figure 5. DAC-89EX Tested with Noise Source.

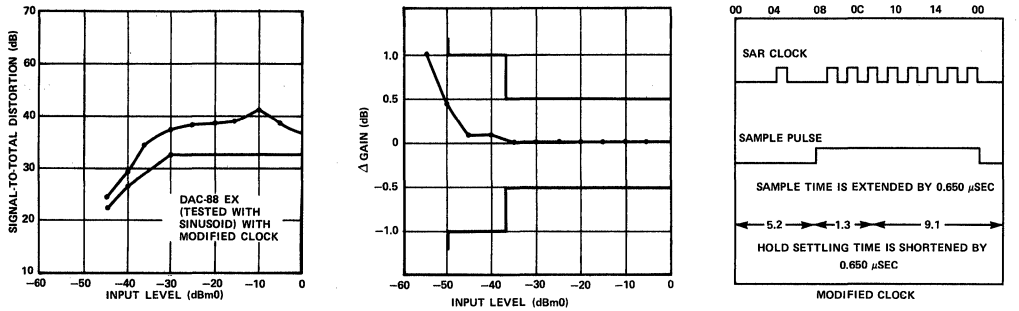


Figure 6. DAC-88EX with Altered Encode Clock (Reduced Hold Settling Time).

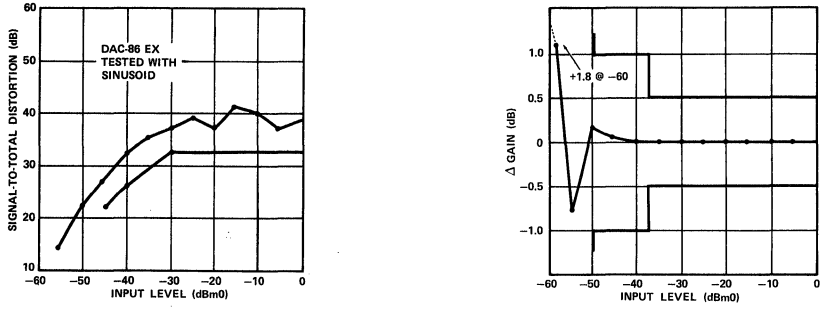


Figure 7. DAC-86EX Original μ-Law DAC with Faster Clock.

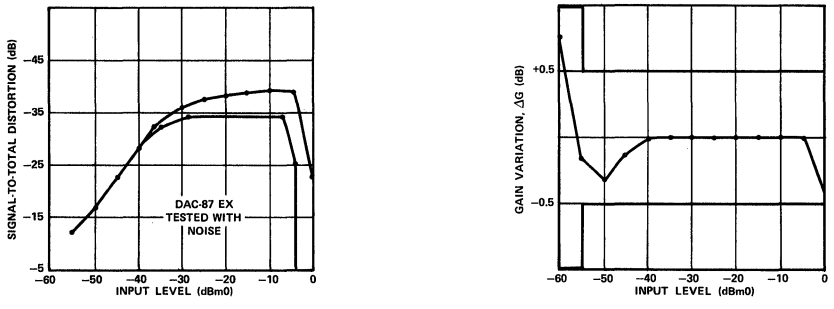


Figure 8. DAC-87EX Tested with Noise with Faster Clock.

Comparisons of idle channel noise measurements using the MUX-88 and the DMX-88 are shown in Figures 9 and 10. It is important to notice that these measurements were made at the input to the PCM output filter. Collecting data at the filter output is not feasable because the noise values are too low for the equipment being used. To show the difference between the new and old components, a measurement was made that yielded some data. However, for both devices the idle channel noise is well within the normal system guidelines. The test data shows the difference due to reduced device charge injection of the DMX. Using a 10,000pF hold capacitor produces at least a 10dB improvement for the DMX and when the hold capacitor is reduced, the improvement is even more obvious. The smaller hold capacitor allows the D/A circuit to drive more channels. Since the current capability of the multiplexer switch is limited, a smaller capacitor means less charge-up time is required and a faster settling time is possible. The "demultiplexer" allows the user the option of reducing the hold capacitance without affecting the idle channel noise performance.

	CHANNEL MEASURED	IDLE CHANNEL NOISE	HOLD CAP
MUX-88	1	-60.8	10000pf
	2	-61.1	10000pf
	3	-60.3	10000pf
	4	-61.1	10000pf
	5	-60.9	10000pf
	6	-61.3	10000pf
	7	-61.2	10000pf
	8	-60.0	10000pf
DMX-88	1	All Values <-70dB	10000pf
	2		10000pf
	3		10000pf
	4		10000pf
	5		10000pf
	6		10000pf
	7		10000pf
	8		10000pf

NOTE: VALUES MEASURED BEFORE PCM OUTPUT FILTER WITH HP-3551A (-70dB IS LOWEST MEASUREMENT)

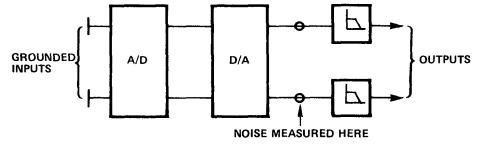


Figure 9. Idle Channel Noise.

Another demonstrator design change was added to show how additional reduction of crosstalk is possible through proper control of the output multiplexer. The first design did not make use of the enable function of the output switch. As a new digital word was latched to the decode circuit, the output MUX address was switched. The timing involved in these two sequences is such that some signal feedthrough is seen due to the data latch and D/A circuit (DAC-88/89 and OP-16) settling more quickly than the MUX switch can open. Performance is improved by the MUX being disabled prior to the analog channel being switched. This assures, by using lead CC, that the MUX is completely open while the new decoder

	CHANNEL MEASURED	IDLE CHANNEL NOISE	HOLD CAP
MUX-88	1	-57.2	1000pf
	2	-57.2	1000pf
	3	-57.2	1000pf
	4	-57.2	1000pf
	5	-57.2	1000pf
	6	-57.2	4300pf
	7	-57.2	4300pf
	8	-57.2	4300pf
DMX-88	1	-68.6	1000pf
	2	-68.6	1000pf
	3	-68.6	1000pf
	4	-68.6	1000pf
	5	-68.6	1000pf
	6	<-70	4300pf
	7	<-70	4300pf
	8	-69.9	4300pf

NOTE: MEASURED AS SHOWN IN PREVIOUS FIGURE.

Figure 10. Idle Channel Noise.

INPUT CHANNEL	MEASURED CHANNELS	CROSSTALK (1.02KHz)
1	4	-72
	3	-80
	2	-80
	8	-85
	7	-85
	6	-85
	5	-78
2	8	-72
	7	-80
	6	-85
	5	-85
	1	-85
	4	-84
	3	-85
3	2	-70
	8	-80
	7	-85
	6	-85
	1	-85
	4	-74
4	3	-72
	2	-78
	8	-82
	7	-85
	6	-85
	5	-80
	1	-75

- CHANNEL NUMBERS AS SHOWN ON ENCODER & DECODER BOARDS.
- INPUT LEVEL = 0dBm0
- MEASURED WITH HP3580A SPECTRUM ANALYSER.

Figure 11. Crosstalk.

output is settling. The MUX address is then switched and the MUX enabled. The timing of these signals is shown with the SAR clock in Figure 2. The crosstalk measurements are shown in Figure 11.

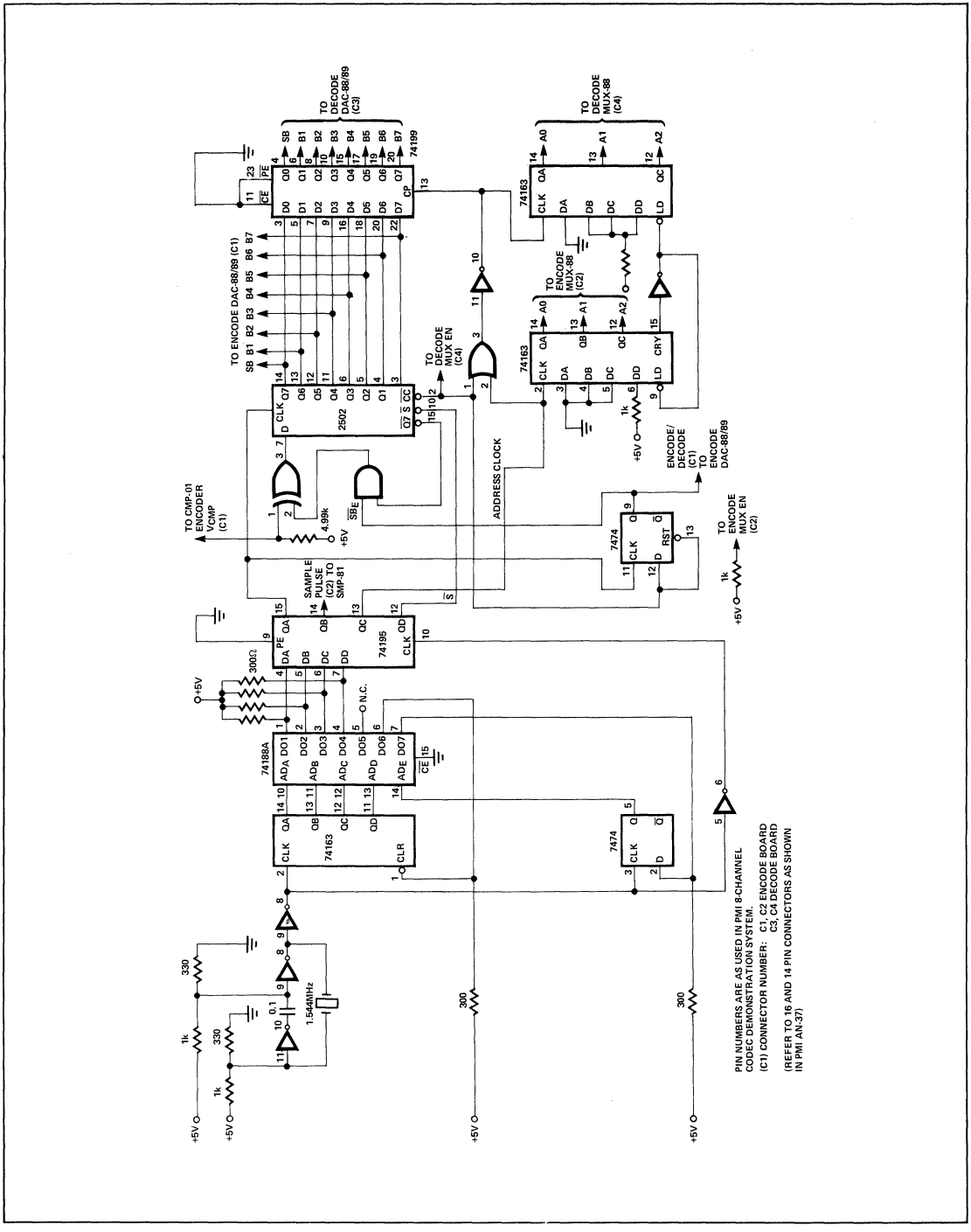


Figure 12A. CODEC Demonstration system Digital Control Board.

CONCLUSIONS

Thanks to the use of newly developed components, the PMI eight-channel CODEC demonstrator reveals the performance possible with a multiple channel digital transmission system. As illustrated by the test results, the transmission performance has been improved from that shown in AN-37. Moreover, the design is simpler and even more economical. Working with an eight-channel system allows the designer to investigate additional improvements in and advantages of the multiple-channel approach. Because of this, PMI makes a set of boards available (encoder, decoder, controller) to any customer interested in investigating the advantages to a shared-channel design.

The system is still the basic design presented in AN-37 and the work described in that note has aided in continuing improvement of PMI components. A complete demonstration system schematic is shown in Figure 12.

PMI is committed to providing telecommunication components capable of meeting and exceeding all requirements for digital switching and transmission systems. We feel the shared-channel approach provides economic and space advantages over the use of single-channel CODEC's in many designs. It has also been seen by several of our customers, that since our designs use individual components, by properly specifying these parts, the overall system performance can be guaranteed. This can provide savings in component and board-level testing costs. The system designer needs only to evaluate the PMI approach to become aware of the possibilities it holds in terms of digital transmission system design.

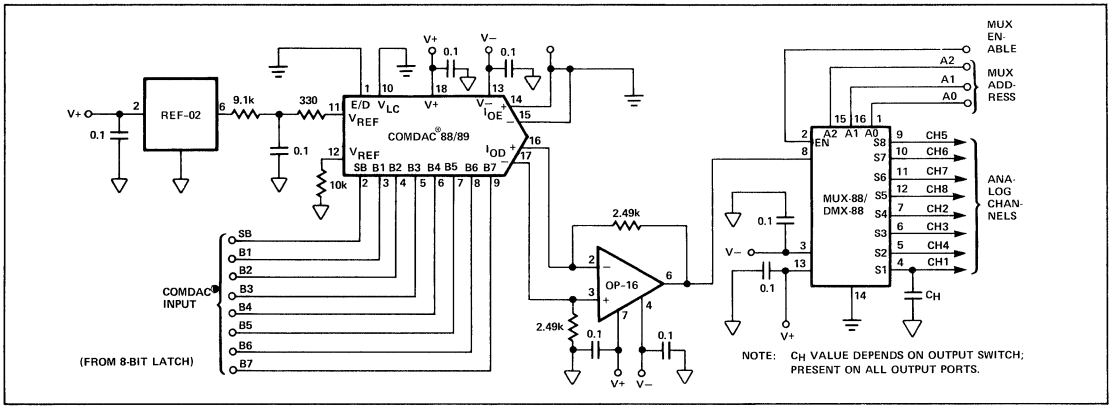


Figure 12B. Demo System Decode Board.

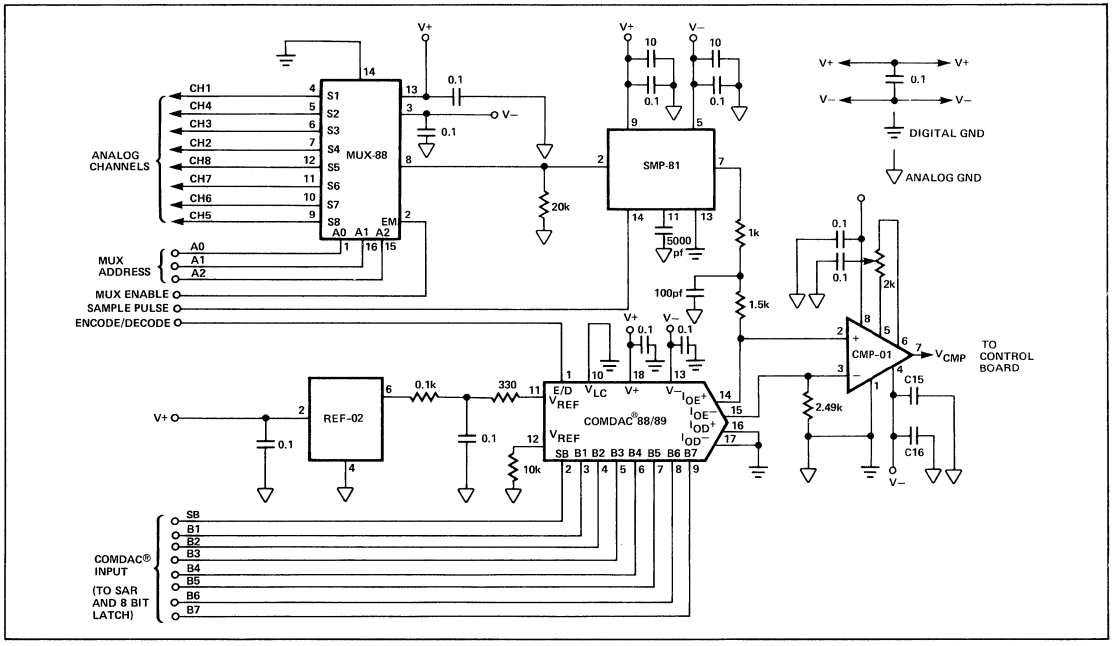


Figure 12C. Demo System Encode Board.

APPLICATION NOTE 42

A 1kHz, 0dBm0 Standard Signal Generator

by B.W. Berry

The CCITT standards concerning line transmission include a specification demonstrating the relationship between the encoding laws (A-law or μ-law) and a standard audio signal level. The relationship is such that when a specific periodic sequence of character signals are applied to the appropriate decoder, the output will be a sine-wave signal at 1kHz with a nominal level of 0dBm0. The prescribed digital characters are those represented in Tables 1 and 2.

While developing the multiple-channel CODEC systems, it became useful to test the encoder and decoder portions of the circuit separately. To complete such tests, a CCITT-standard signal generator was produced. The generator consists of five TTL packages and is driven by an 8kHz signal. The required digital sequence is simple to implement as four of the outputs are constant values. For the remaining active bits, a four bit-binary counter was used to produce an appropriate sequence. As is shown in the schematic (Figure 3), the counter clocks from 0101 to 1100 and then repeats. This sequence directly provides the output for bits 4 and 6 and the inverted bit 8. With additional logic, the remaining bit, bit 1, is also available.

The usefulness of such a generator is seen first of all in trouble shooting any preliminary CODEC designs. Secondly, for PMI, it provided a small, easily transportable signal source to be used in PMI's eight-channel CODEC demonstration unit. Using the digital signal generator in conjunction with a PMI DAC-88 or 89 and an OP-16 provides a analog driver capable of producing the CCITT standard transmission signal. The completed signal generator schematic is shown in Figure 4.

Table 1. A-Law

Character Signals								Transmitted Characters*							
B1	B2	B3	B4	B5	B6	B7	B8	B1	B2	B3	B4	B5	B6	B7	B8
0	0	1	1	0	1	0	0	0	1	1	0	0	0	0	1
0	0	1	0	0	0	0	1	0	1	1	1	0	1	0	0
0	0	1	0	0	0	0	1	0	1	1	1	0	1	0	0
0	0	1	1	0	1	0	0	0	1	1	0	0	0	0	1
1	0	1	1	0	1	0	0	1	1	1	0	0	0	0	1
1	0	1	0	0	0	0	1	1	1	1	1	0	1	0	0
1	0	1	0	0	0	0	1	1	1	1	1	0	1	0	0
1	0	1	1	0	1	0	0	1	1	1	0	0	0	0	1

*Transmitted Characters for A-LAW are obtained by inverting even bits of Character Signals.

Table 2. μ-Law

Character Signals								Transmitted Characters*							
B1	B2	B3	B4	B5	B6	B7	B8	B1	B2	B3	B4	B5	B6	B7	B8
0	0	0	1	1	1	1	0	1	1	1	0	0	0	0	1
0	0	0	0	1	0	1	1	1	1	1	1	0	1	0	0
0	0	0	0	1	0	1	1	1	1	1	1	0	1	0	0
0	0	0	1	1	1	1	0	1	1	1	0	0	0	0	1
1	0	0	1	1	1	1	0	0	1	1	0	0	0	0	1
1	0	0	0	1	0	1	1	0	1	1	1	0	1	0	0
1	0	0	0	1	0	1	1	0	1	1	1	0	1	0	0
1	0	0	1	1	1	1	0	0	1	1	0	0	0	0	1

*Transmitted Characters for μ-LAW, all bits are inverted.

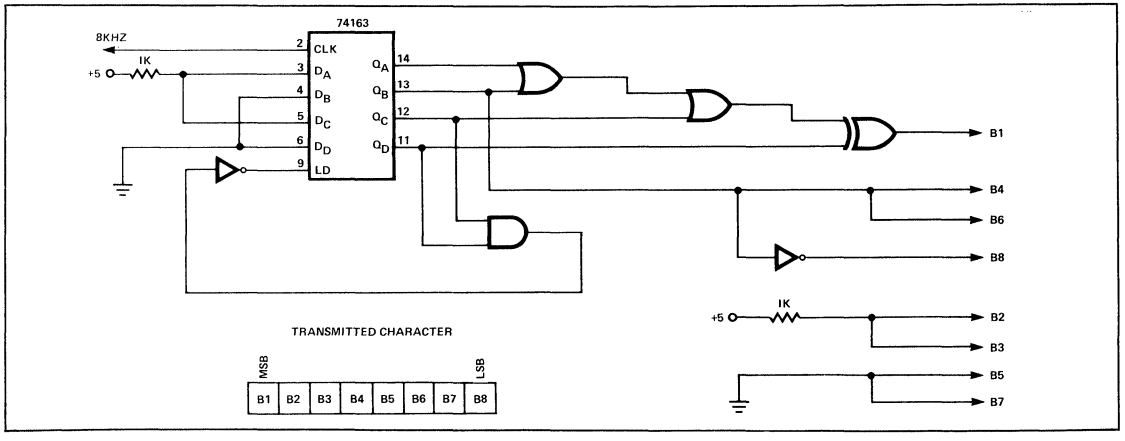


Figure 3. Charater Generator

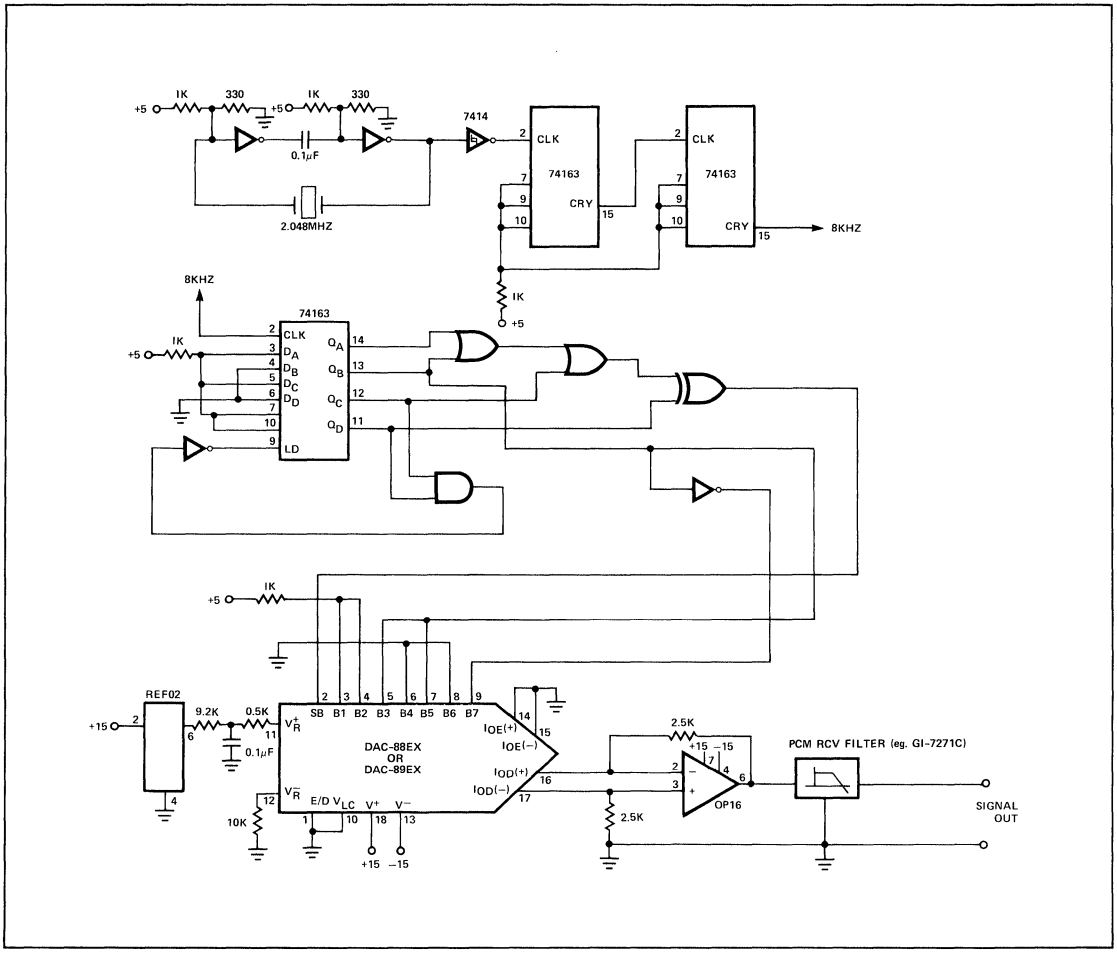


Figure 4. 1kHz, 0dBm0 Sine-Wave Generator

APPLICATION NOTE 43

THE DAC-76 IN CONTROL APPLICATIONS

by Mike Parsin

This note describes a companding D/A converter that is ideally suited for industrial control applications using 8-bit microprocessor bus structures. Features, such as 4-channel demultiplexing, a reference amplifier that accepts various levels of DC or AC for multiplying, and both encode or decode capabilities are on-board the COMDAC®. Twelve-bit accuracy can be obtained with a logrithmic 7-bit plus sign microprocessor compatible D/A converter.

The DAC-76 is at its best when measurement and control become critical as the signal approaches zero volts. Not all control systems that require precise control need the accuracy of a 12-bit digital-to-analog converter over their entire range of operation. In fact, the non-linearity of a 7-bit companding D/A converter can be quite an advantage.

COMDAC® CONVERTER CHARACTERISTICS

The term "companding" comes from compression/expansion which is used extensively in the telecommunication industry. Compression is performed in the encode or analog-to-digital conversion mode, and expansion occurs during decode or D/A conversion. The A/D transfer characteristic is seen in Figure 1. Eight points which are referred to as chords or segments are selected by a 3-bit binary code. Within each chord are 16 steps selected by a 4-bit binary code. Each chord segment is linear to 1/2LSB. Step size varies from 0.025% in chord 0 to 3.2% (of full scale) in chord 7 (see Table 1).

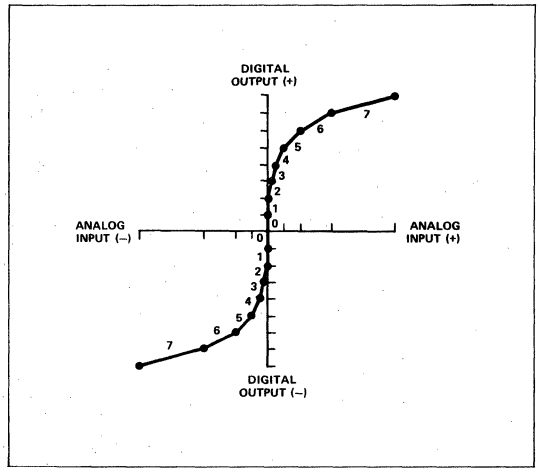


Figure 1. Transfer Characteristic

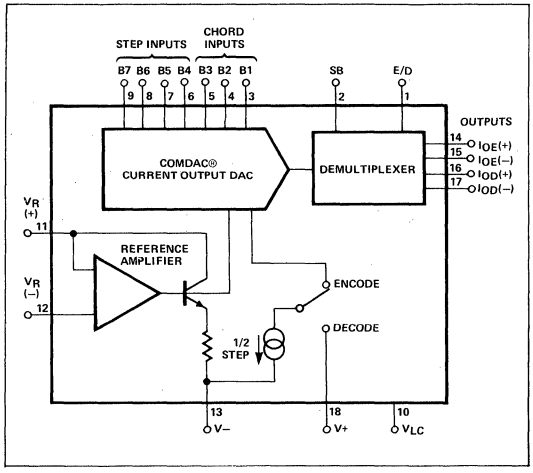


Figure 2. DAC-76 Equivalent Circuit

Table 1. Step Size Summary Table Decode Output (Sign Bit Excluded)

CHORD	STEP SIZE NORMALIZED TO FULL SCALE	STEP SIZE INμA WITH 2007.75μA F.S.	STEP SIZE AS A % OF FULL SCALE	STEP SIZE IN dB AT CHORD ENDPOINTS	STEP SIZE AS A % OF READING AT CHORD ENDPOINTS	RESOLUTION & ACCURACY OF EQUIVALENT BINARY DAC
0	2	0.5	0.025%	0.60	6.67%	SIGN + 12 BITS
1	4	1.0	0.05%	0.38	4.30%	SIGN + 11 BITS
2	8	2.0	0.1%	0.32	3.65%	SIGN + 10 BITS
3	16	4.0	0.2%	0.31	3.40%	SIGN + 9 BITS
4	32	8.0	0.4%	0.29	3.28%	SIGN + 8 BITS
5	64	16	0.8%	0.28	3.23%	SIGN + 7 BITS
6	128	32	1.6%	0.28	3.20%	SIGN + 6 BITS
7	256	64	3.2%	0.28	3.19%	SIGN + 5 BITS

COMDAC® DESCRIPTION

The DAC-76 contains a logrithmic current output D/A converter, a 4-channel demux, and a reference amplifier. The reference amplifier accepts bipolar inputs and sets the converter's full scale output range from 0 to 4.2ma. This output current can then be adjusted by the digital input code described earlier. Inputs B1 through B3 select the chord while B4 through B7 select the steps within the chord (see Figure 2). A unique switch is used in the demultiplexer section that can be programmed for encode/decode (E/D) select, or polarity of a bipolar signal selection with the sign bit (SB). The combination of both E/D and SB results in the 4-channel demultiplexing capabilities. The COMDAC® versatility becomes quite apparent in Figure 3.

Because the nature of D/A converters is to exhibit full scale minus 1 LSB when all bits are on, 1/2LSB is added in the encode mode to insure full scale accuracy. This corrects the error in encode operations but also means there is a 1/2LSB error between I_{OD} and I_{OE} (Figure 3a) in demultiplexer applications.

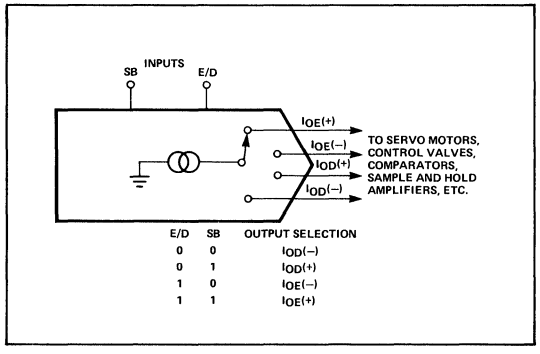


Figure 3a. Demultiplexing

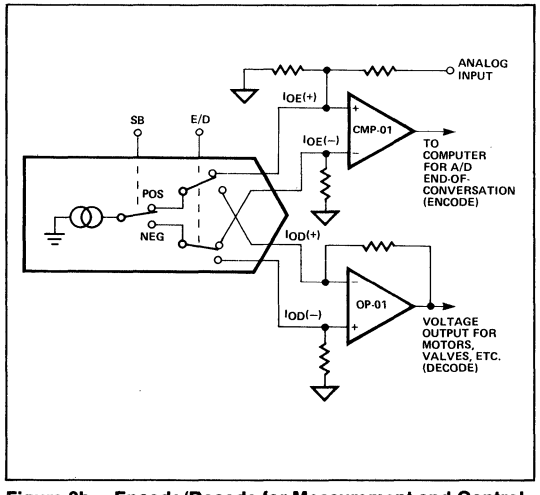


Figure 3b. Encode/Decode for Measurement and Control

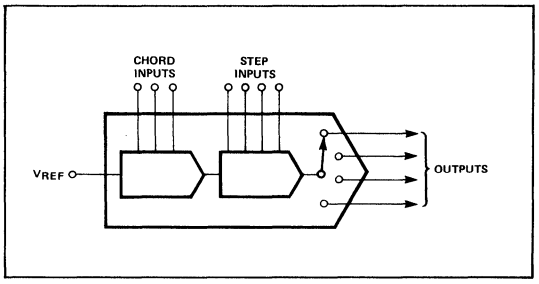


Figure 3c. Nonlinear Coding

MICROPROCESSOR COMPATIBILITY WITH 8-BIT μP's

Since the COMDAC® has 8 digital inputs, all data transfers can occur in 1 byte instead of 2 bytes required for 12-bit D/A converters. Another bit provided for encode/decode is a control function and does not affect data transfer speeds.

Figure 4 shows how simple it is to interface popular μP I/0 adapters with 8-bit ports. Another feature is the logic control pin (VLC) which can be used to enable the device (logic "0") or disable with a logic "1". The COMDAC® accepts all popular logic levels by applying the logic threshold voltage at this pin. The VLC is low for TTL applications.

Settling time of the DAC-76 is typically 1 microsecond. This is within the cycle time of most microprocessor's.

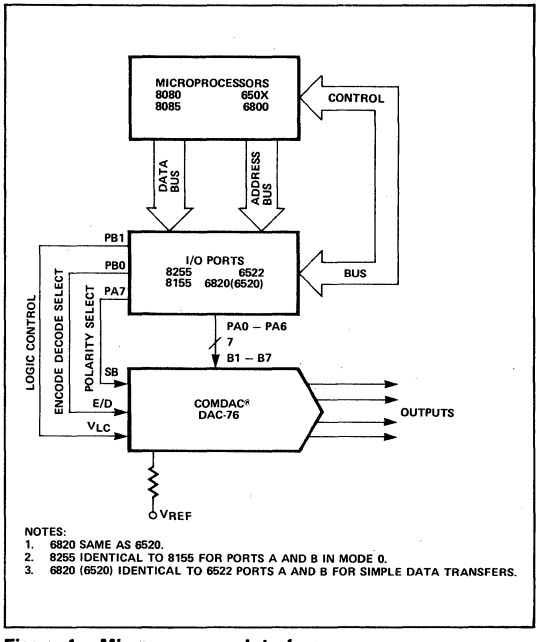


Figure 4. Microprocessor Interface

COMDAC® APPLICATIONS

When choosing between a linear or a logarithmic D/A converter, two factors should be considered. The first is that the error signal in control applications is far more important than the absolute value. The second is that low level signals are more critical than large signals, although a wide dynamic range is still a requirement.

This circuit is ideal when usually low signals are present at the sensor. For example, when measurement of a process is typically +100° C+/-10° C, but can range from 75° C to 1000° C. The alarm is set to trip at 500° C. In this case the COMDAC® accuracy should be greatest from 75° C to 110° C, a 35° C range. The DAC must have a dynamic range equivalent to 925 degrees, but only the 35 degree range need be accurate.

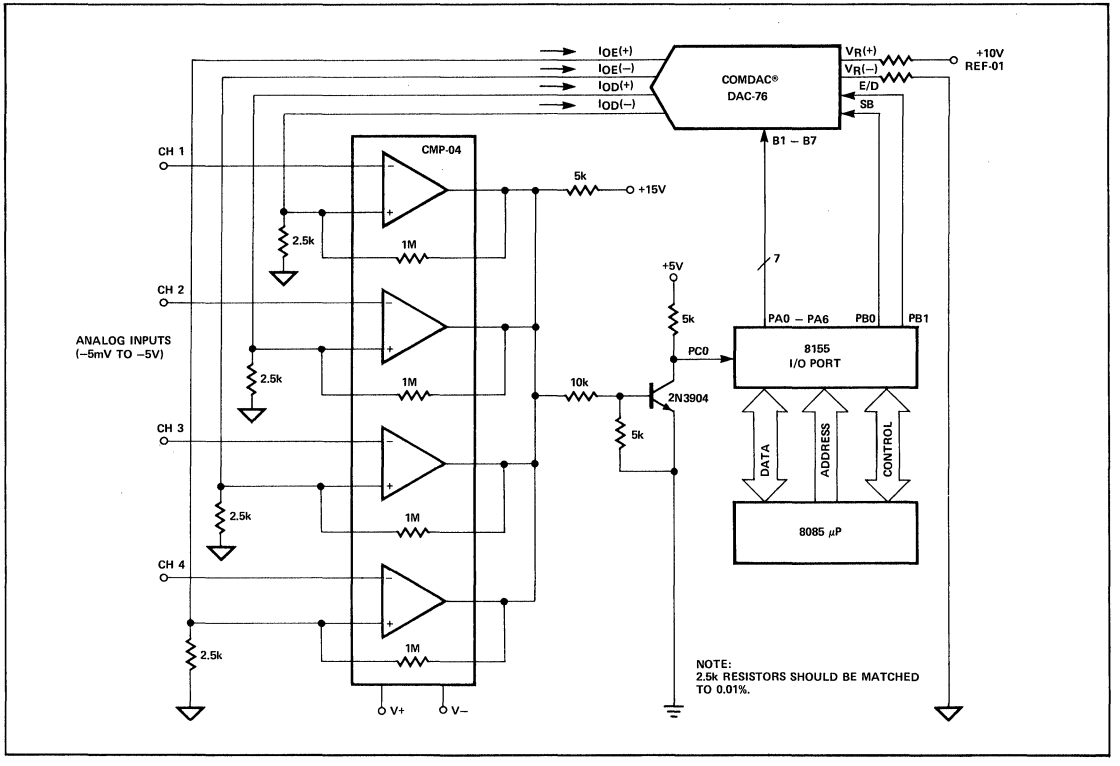


Figure 5. Four Channel Data Acquistion System

DATA ACQUISITION

A four-channel Data Acquisition System (DAS) is shown in Figure 5 which is unique because only two linear chips are needed. Initially, I/0 port PA is reset and port PB is addressed at PB0 and PB1 to select 1 of 4 input channels. The computer then counts up from zero at port PA until the COMDAC®'s output is equal to the analog input voltage at the selected comparator. Since the CMP-04 quad comparator has open collector outputs, these outputs are OR'ed together and an end-of-conversion is signaled when the selected comparator output goes low (Figure 5a). The count latched in port PA is then the digital equivalent of the analog input. All four channels can be selected this way with the resulting digital data stored in memory.

Analog inputs ranging from –5 millivolts to –5 volts can be measured. To guarantee that the CMP-04 output is normally high, at least 5 millivolts is required at all channels.

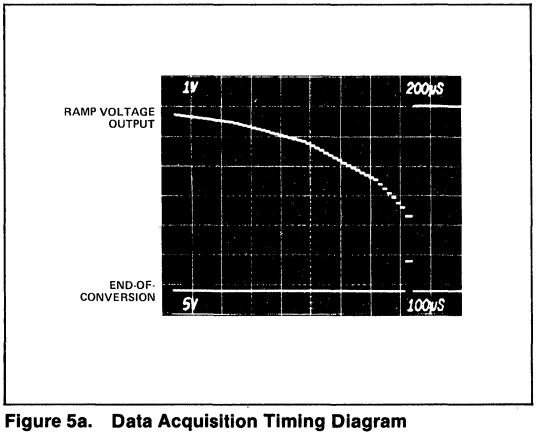


Figure 5a. Data Acquisition Timing Diagram

A logrithmic DAC will then trip the alarm at 500° C, measure to 1000° C, and give a very accurate reading from 75° C to 110° C. Keep in mind the dynamic range of the COMDAC® is 4000:1 or 72db (excluding the sign bit).

VALVE CONTROLLERS

A programmable controller (PC) is shown in Figure 6. To complete a "control loop", the data acquisition system just described and the PC are required. Today's distributed systems need mini or microcomputers at remote stations to operate the control loop. The system described here uses two DAC's to position the valve opening. A linear DAC-08 makes the gross setpoint adjustment while the COMDAC® makes the fine adjustment to 0.025%.

The operation of this circuit (Figure 6) is straight forward. When the process changes, it is detected by the microprocessor which is periodically monitoring the sensor's output through the DAS. The processor then determines the error between the setpoint and sensor. This "offset" is then sent to the COMDAC® for proper valve positioning. The offset current is "summed" with the DAC-08 at the amplifier.

A "reset time", which is the time between valve repositioning, is determined by the processor.

PROGRAMMABLE MOTOR CONTROL

Another popular application is the motor controller. Here a DC motor (Figure 7) is driven from the COMDAC® (requires a power amp). Speed is directly proportional to the voltage across the motor. The sign bit determines the direction of rotation and the 7 magnitude bits determine motor speeds. For servo applications a shaft encoder can be used to close the loop.

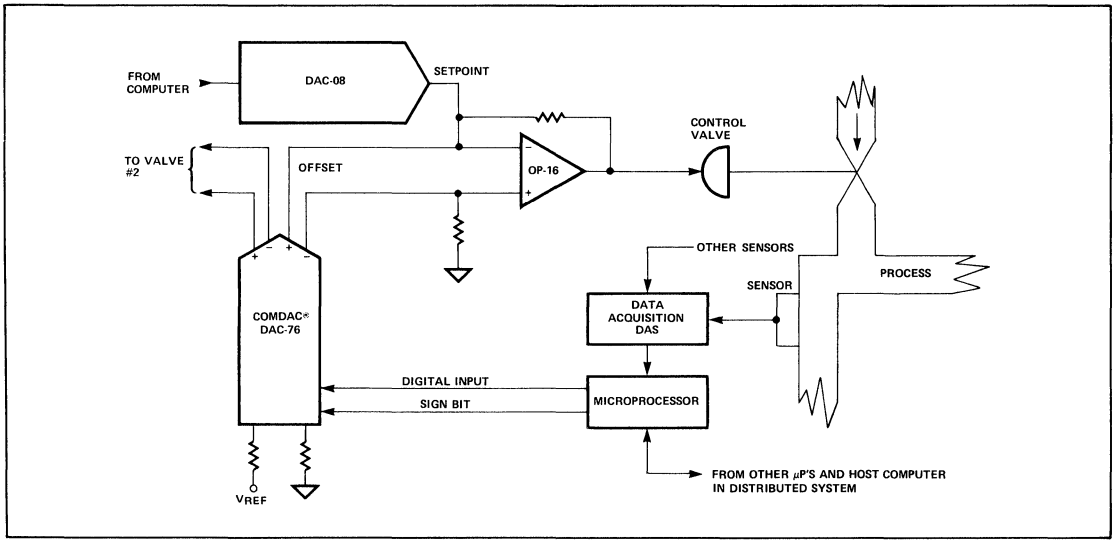


Figure 6. Programmable Controller in Distributed System

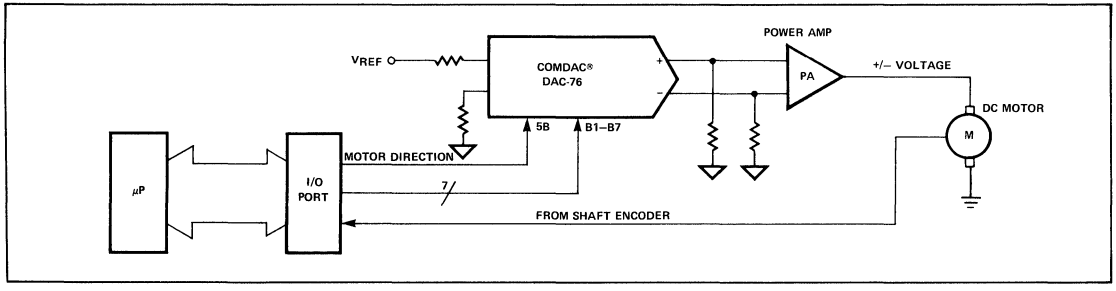


Figure 7. Programmable Servo Motor Controller

APPLICATION NOTE 44

COMPOSITE BUFFER PROVIDES SPEED, ACCURACY

by Scott Bernardi and George Erdi

INTRODUCTION

Suppose a particular operational amplifier integrated circuit satisfies all of the requirements for a voltage follower application except for speed. Instead of searching for a faster op amp, a design engineer may be able to obtain the desired speed by placing a fast buffer, such as the BUF-03, in the feedback loop of the op amp. The resulting composite amplifier maintains the op amp's accuracy while enhancing its speed.

The BUF-03, possessing a bandwidth of 63MHz, is well suited for this type of use. In Figure 1, it is shown in the feedback loop of an OP-07, an industry standard for applications requiring high DC accuracy but also a device with limited speed. The composite configuration is a fast and accurate noninverting unity-gain amplifier requiring only two external resistors.

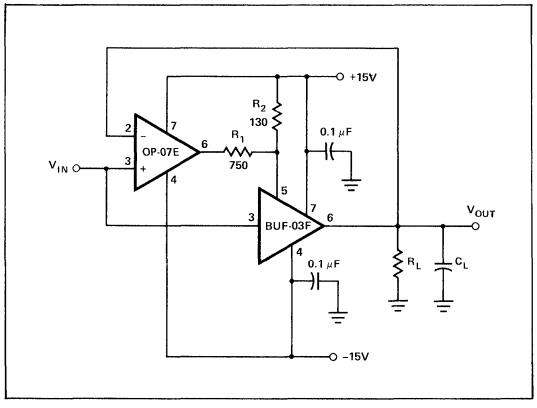


Figure 1. Use of the BUF-03 and the OP-07 as a Composite Amplifier in a Noninverting Unity-Gain Amplifier.

CIRCUIT OPERATION

In Figure 1, input signals of up to ±10V are applied to both the input of the BUF-03 and the non-inverting input of the OP-07. The OP-07 reduces the V_{IN} — V_{OUT} error of the BUF-03 by driving its **null** terminal, rather than the input of another op amp as is commonly done. Resistors R1 and R2 form a voltage divider which enables the output of the OP-07 to remain in its active region while modulating the BUF-03's null terminals (nominally at +14.3V).

The DC errors of the composite circuit, including input offset voltage (V_{OS}), change of offset voltage with temperature (TCV_{OS}), power supply rejection ratio (PSRR), and gain error (output regulation with load) are reduced to those of the OP-07. The circuit in Figure 1, using an OP-07E (prime grade, commercial-temperature version) and a BUF-03F (commercial grade, commercial-temperature version) boasts a V_{OS} at $V_{IN} = 0V$ of +30μV, and a gain error (V_{IN} — V_{OUT}) with a 1,000-ohm load of five parts per million (50μV) at ±10V.

The AC performance of the composite amplifier is that of the BUF-03. One of the main advantages provided by the circuit arrangement is that the BUF-03 remains stable with **any** capacitive load whereas the OP-07 requires a 50-ohm decoupling resistor with C_L greater than 500pF. Also, the BUF-03's 60-70mA driving current will slew large capacitances easily (1,000pF and 2k ohms at 60V/μs for a ±5V pulse). This is illustrated in the waveform shown in Figure 2. The slew rate of the system with $C_L = 10pF$ (probe capacitance) is 220V/μs as revealed in Figure 3.

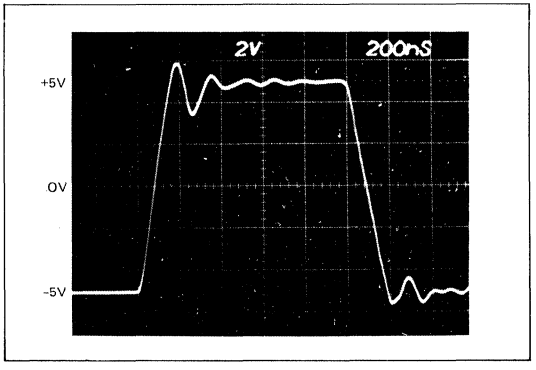


Figure 2. A Slew Rate of More Than 60V/μsec Is Obtained with an R_L of 2kΩ, a C_L of 1,000pF and 60mA of Driving Current.

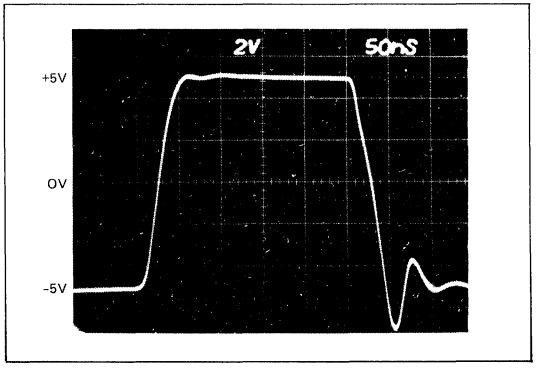


Figure 3. Very High Slew Rate Is Achieved with an R_L of 2kΩ and a C_L of 10pF.

In a composite amplifier arrangement, each of the devices dominates the characteristics at one of the two frequency extremes and a smooth transition of characteristics takes place in between.

If only low-frequency signals are to be processed, an OP-07 connected as a voltage follower might as well be used alone, unless of course, large capacitive load handling capability and large load currents are required. At higher frequencies, the OP-07 cannot respond fast enough to drive the BUF-03's null terminal correctly, resulting in improper gain error cancellation. However, even the BUF-03 alone has a typical gain error of only 0.5% for a ±10V input with 2k-ohm load (using the BUF-03F). The transition frequency occurs in the 2kHz to 10kHz region, depending on load conditions. There will be a point (up to the transition frequency) where the combined performance of both devices is better than either device individually.

CONCLUSION

The BUF-03 can be used as described with virtually any op amp in voltage follower applications to provide speed enhancement without sacrificing DC accuracy. This is true even where a high-speed op amp is already being employed, and still faster speed is desirable.

APPLICATION NOTE 45

TIME SHARING PERMITS DESIGN OF CONTROLLER WITH SINGLE DAC

by Mike Parsin

INTRODUCTION

The DAC-76 COMDAC® Companding D/A Converter is a monolithic IC containing a multiplying logarithmic D/A converter with a demultiplexed output for encode/decode switching.

This application note describes the use of a single DAC-76 in the design of a converter instead of the use of one IC for analog-to-digital conversion at the input and another IC for digital-to-analog conversion at the output (the conventional way of designing a controller).

In the controller to be described in the following paragraphs, the DAC-76 not only multiplexes between encode and decode, it also compresses 12-bit accuracy into a 7-bit format. Its seven bits plus sign make the DAC-76 an ideal interface for 8-bit microprocessors.

THE COMDAC® SYSTEM

The heart of a COMDAC® system is a DAC-76 companding D/A converter. Capable of being switched from "measurement" in the encode mode to "control" in the decode mode, the DAC-76 is completely bipolar in both modes because of the sign bit. All four outputs sink current.

The system depicted in Figure 2 uses six support chips. An 8085 microprocessor and an 8155 I/O port supply the digital data; an op amp, comparator, reference and sample-and-hold amplifier complete the analog function.

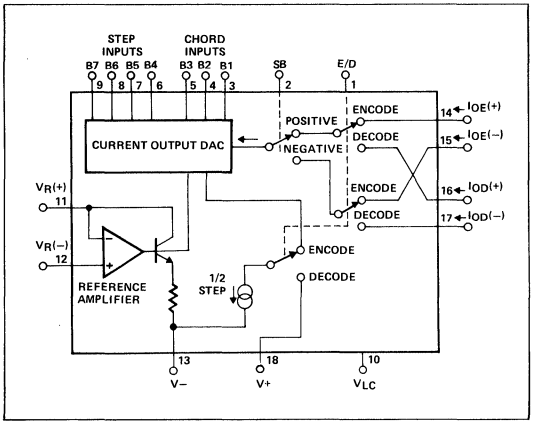


Figure 1. Equivalent Circuit

ENCODE MODE

The measuring mode starts when the Encode/Decode (E/D) line goes high. The microprocessor then sends a digital count to the DAC that starts a ramp. The encode waveform shown in Figure 3a reveals the timing and logarithmic ramp from the COMDAC® . This signal is fed to the comparator which in turn signals an end-of-conversion (EOC) when the

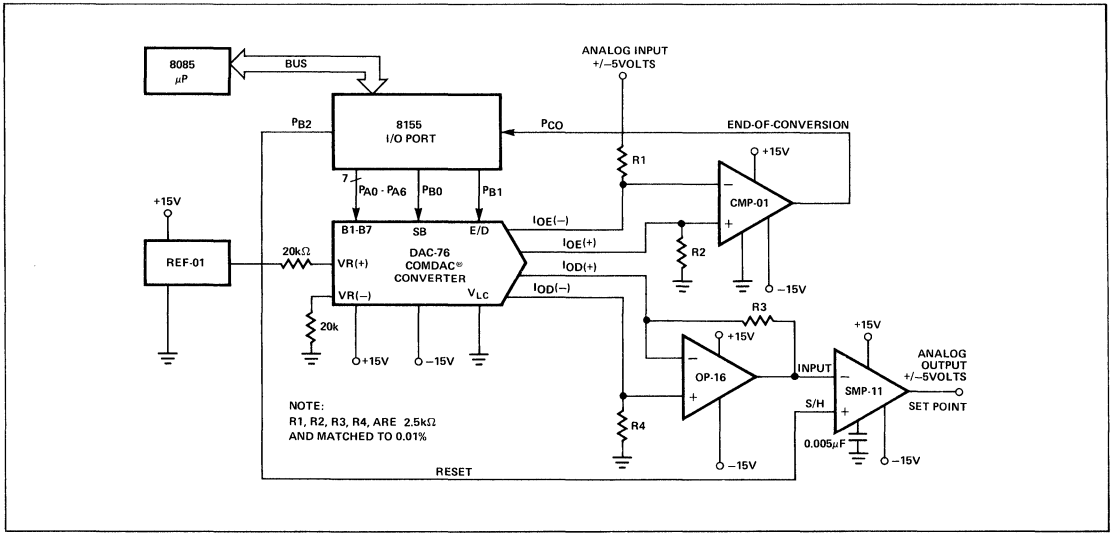


Figure 2. COMDAC® Controller Showing Analog Input/Output

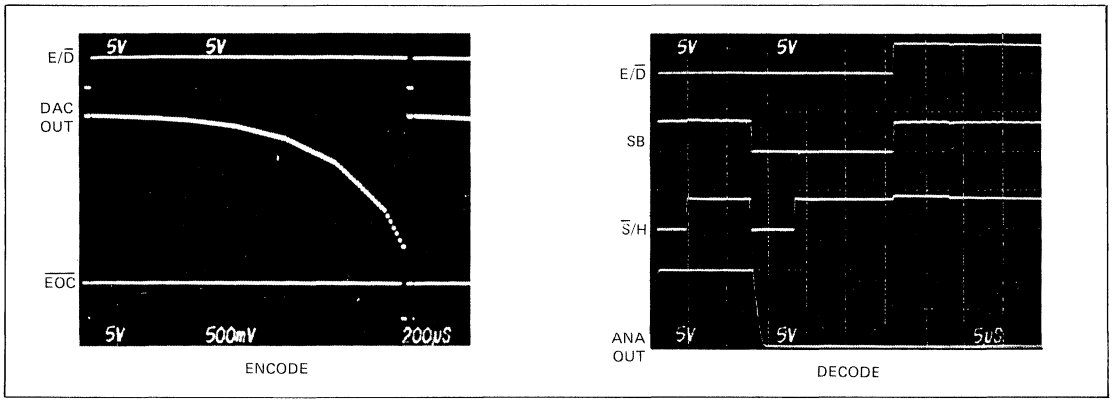


Figure 3. Timing Diagram

analog input equals the ramp voltage. The count stops and the binary result is stored in a one-byte memory location for further data processing. This data is the result of the transducer output.

The software for encoding is described in Table 1.

DECODE MODE

The data stored in the encode mode is now compared to the data in the previous setting. For example, if the setpoint was set for 100 degrees and the measured value was 110 degrees, this 10-degree error or "offset" would have to be corrected by the control device, in this case a valve. A look-up table determines the required change in valve position proportional to the offset voltage. Once the correction is determined by the microprocessor the data is sent to the DAC. A "low" at E/D sets the DAC to "decode" which steers current to the inverting input of a high-speed BIFET operational amplifier (OP-16) when the sign bit is "high."

The sample/hold amplifier samples during this time and "holds" the op amps output after it settles. This positive analog output of five volts goes to a negative 5-volt output when the sign bit is switched (see decode waveform in Figure 3b). The waveform shows that the analog output remains constant even when the COMDAC® system changes to the encode mode for another sample. The time between samples is referred to as "reset time." If the deviation or "offset" starts to increase more rapidly, the reset time is increased by the microprocessor. The program shown in Table 1 exhibits only control and measurement instructions. The sample/hold line can be considered a reset control. The output voltage is referred to as the "setpoint" and is used to control a linear device such as a control valve.

SINGLE LOOP CONTROLLER

Following the advent of the computer, most controllers became digitally controlled and were used in direct or distributed digital control systems.

The direct digital control system is defined as a single-host computer at the hub of a multitude of remote controllers. In contrast, the distributed digital control system is centralized by the host computer but has many remote micro or minicomputers that perform direct control of the loop or loops. The host computer is responsible for "supervisory" functions. In the case of a direct digital control system, the whole system "shuts down" if the host computer fails. The distributed system does not rely on any one component. Any of the remote computers or even the central computer can fail with only that particular remote station being affected. A bus structure referred to as "the data highway" interconnects the remote computers.

The controller shown in Figure 4 contains only a single control loop driven by a microprocessor; the controller, however, could be a part of the distributed system previously mentioned. The controller's sensor input voltage is amplified by an instrumentation amplifier converted to current by the V/I.

Current is used to transmit signals long distances because it is much less susceptible to noise than voltage transmission. The COMDAC® controller accepts the analog input, encodes the signal, compares the digitized signal to the setpoint, and finally establishes a new setpoint if an "error" has been introduced. The analog output is then converted to current for transmission to an electrically actuated control valve. This completes the control loop.

COMPANDING PRINCIPLE

"Companding" means compression/expansion. In the encode mode, the analog signal is compressed into a digital format illustrated by the transfer in Figure 5a. Expansion occurs during decode which expands the digitized signal back to analog. Figure 5b shows this transfer characteristic. These figures show eight points or segments which are referred to as "chords." Each chord is selected by a 3-bit binary code. Sixteen "steps" make up each chord which are selected by a 4-bit binary code. The chord segmentation is shown in Table 2. Note that the change in step size ranges from 0.025% in chord 0 to 3.2% (of full scale) in chord 7. The DAC-76 is monotonic over the full operating range and linear to ½ LSB within each chord. One of four outputs can be selected for bipolar operation in encode and decode modes (Table 3).

On-board the chip are a logarithmic current output D/A converter, an encode/decode demultiplexer, and a reference amplifier. Both positive and negative signals can be fed to the reference amplifier. These currents are then multiplied by the digital input. Inputs B1 through B3 select the chord while B4-B7 select the steps.

CONCLUSION

The single-loop controller described in this application note interfaces very nicely to an 8-bit microprocessor and totally eliminates an A/D converter. The COMDAC® converter or system becomes more accurate as the analog signal (in or out) approaches zero volts. Very broad changes can be accomplished by using the higher chords and fine adjustments are possible with the lower chords.

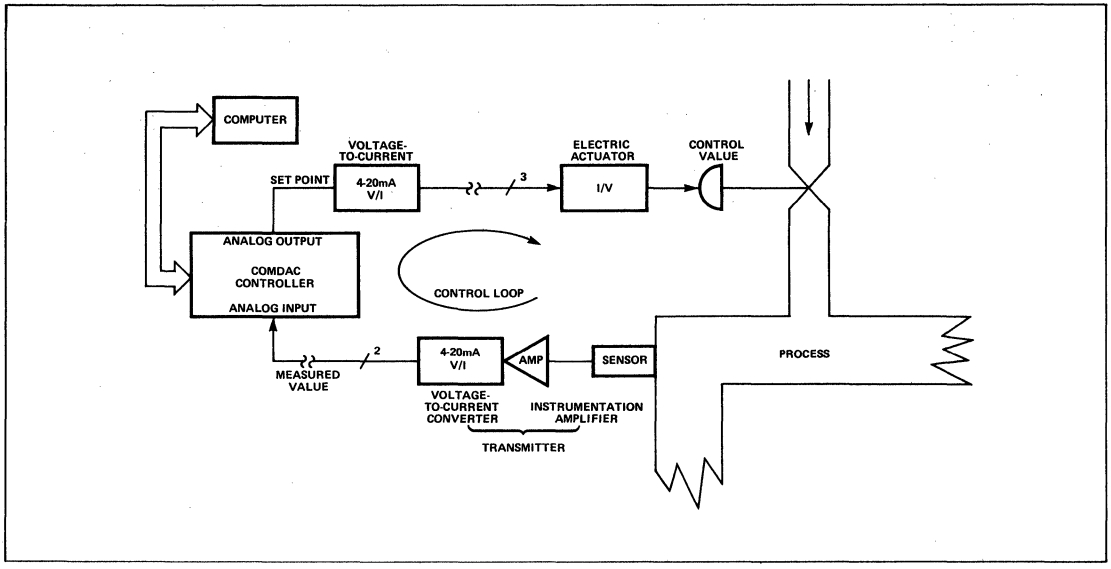


Figure 4. Controller in Single Loop Configuration

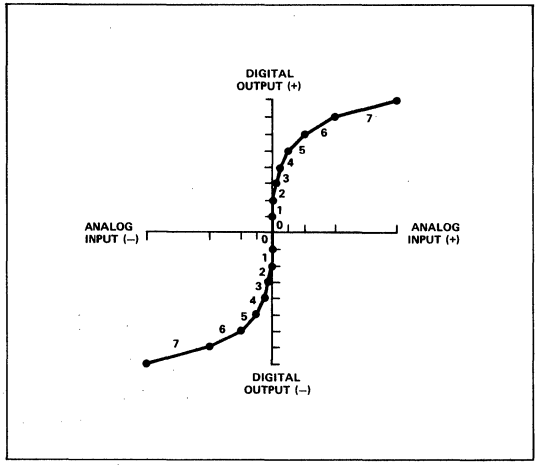


Figure 5a. Encode Transfer Characteristic (A/D Conversion)

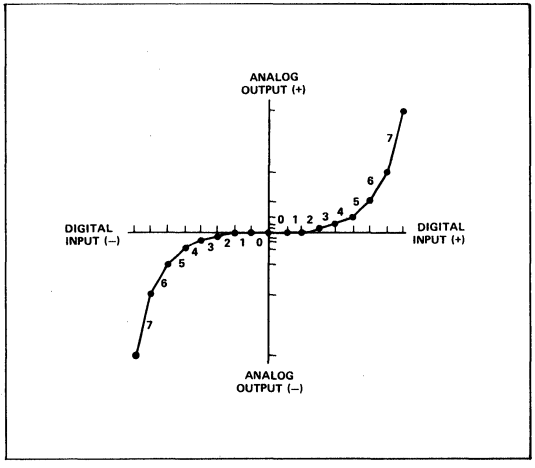


Figure 5b. Decode Transfer Characteristic (D/A Conversion)

Table 1. COMDAC® Software

```
                ;B REG = UP COUNTER
2000                    ORG     2000H
2000 31CC220    BEGIN:  LXI     SP,20C2H        ;INITIALIZE STACK POINTER
2003 3E03               MVI     A,03H   ;SET PT A&B TO OUT & PT C TO IN
2005 D320               OUT     20H     ;THIS SETS 8155 CSR
2007 3E07       ENCOD:  MVI     A,07H   ;START ENCODE
2009 00                 NOP
200A D322               OUT     22H     ;SET E/ TO ENCODE & S/B TO (-)
200C 04         LOOP:   INR     B       ;INCREMENT UP COUNTER
200D 00                 NOP
200E 78                 MOV     A,B     ;COUNT TO ACCUMULATOR
200F D321               OUT     21H     ;OUT COUNT TO COMDAC DIGITAL IN
2011 DB23               IN      23H     ;MONITOR END OF CONVERSION
2013 E601               ANI     01H     ;MASK PCO
2015 C20C20             JNZ     LOOP    ;LOOP WHEN EOC IS HIGH
2018 78                 MOV     A,B     ;MOVE RESULT TO ACCUMULATOR
2019 323C20             STA     203CH   ;STORE RESULT IN MEMORY 203C
201C 0600               MVI     B,00    ;CLEAR B REGISTER
201E 3E7F       DECOD:  MVI     A,7FH   ;START DECODE
2020 D321               OUT     21H     ;OUT TO DAC ALL 1's +5V
2022 3E01               MVI     A,01H   ;SET E/D TO DECODE & S/B TO (+)
2024 D322               OUT     22H     ;OUTPUT TO S/H & COMDAC
2026 3E05               MVI     A,05H   ;S/H TO HOLD ANALOG OUT TO +5V
2028 D322               OUT     22H     ;OUT TO S/H
202A 3E00               MVI     A,00H   ;ANALOG OUT TO NEGATIVE
202C 00                 NOP
202D 00                 NOP
202E D322               OUT     22H     ;OUT TO S/H & COMDAC
2030 3E04               MVI     A,04H   ;S/H TO HOLD ANALOG OUT TO -5V
2032 D322               OUT     22H     ;OUT TO S/H & DAC
2034 00                 NOP
2035 00                 NOP
2036 C30720             JMP     ENCOD   ;START ENCODE AGAIN
```

Table 2. Step Size Summary Table Decode Output (Sign Bit Excluded)

CHORD	STEP SIZE NORMALIZED TO FULL SCALE	STEP SIZE IN μA WITH 2007.75μA F.S.	STEP SIZE AS A % OF FULL SCALE	STEP SIZE IN dB AT CHORD ENDPOINTS	STEP SIZE AS A % OF READING AT CHORD ENDPOINTS	RESOLUTION & ACCURACY OF EQUIVALENT BINARY DAC
0	2	0.5	0.025%	0.60	6.67%	SIGN + 12 BITS
1	2	1.0	0.05%	0.38	4.30%	SIGN + 11 BITS
2	8	2.0	0.1%	0.32	3.65%	SIGN + 10 BITS
3	16	4.0	0.2%	0.31	3.40%	SIGN + 9 BITS
4	32	8.0	0.4%	0.29	3.28%	SIGN + 8 BITS
5	64	16	0.8%	0.28	3.23%	SIGN + 7 BITS
6	128	32	1.6%	0.28	3.20%	SIGN + 6 BITS
7	256	64	3.2%	0.28	3.19%	SIGN + 5 BITS

Table 3. Coding for Output Selection

E/D	SB	OUTPUT SELECTION
0	0	IOD(-)
0	1	IOD(+)
1	0	IOE(-)
1	1	IOE(+)

APPLICATION NOTE 47

BCD DAC MAKES PROGRAMMING OF FUNCTION GENERATOR SIMPLE

by Gary Grandbois and Wes Freeman

Providing analog instrumentation and signal processing systems with the capability to be digitally programmed is becoming increasingly important for two reasons. The first is compatibility with automated digital control systems using microprocessors or general-purpose interface Bus systems. The second reason, unrelated to automation, is the need to reduce errors that result from operator adjustments of equipment.

A conceptional view of analog control (using a potentiometer) and digital control (using a digital-to-analog IC) is depicted in Figure 1. Linear control of the analog function can be achieved through control of absolute voltage, differential voltage or current. Configurations for each of these control modes are shown in Figure 2. For maximum flexibility in applying digital control to a system, a current output DAC, such as the popular DAC-08, or the BCD DAC-20 should be used.

Use of a DAC in analog conditioning or signal processing systems can be a problem if the linear output of the DAC elicits a nonlinear response from the system. To add digital programmability to the system, the designer must begin with a linear system unless, of course, a log or other nonlinear response is desired.

An instrument that can be significantly enhanced by the inclusion of a BCD DAC in its circuitry is the ubiquitous function generator. A single-chip function generator, such as the 8038, can provide sine, triangle, and square-wave outputs at very low cost. The 8038 can operate over the 0.001Hz to over 100kHz range and through three outputs can deliver square, triangular and sine waveforms simultaneously.

In conjunction with a DAC-20 (a two-digit BCD DAC) and a few additional components, the 8038 can be used to design a function generator having 2% frequency linearity and providing both digitally programmable output and logarithmic sweep.

At first glance, the circuit shown in Figure 3 appears to provide the designer with digital control capability. In this circuit, the 8038 is programmed by the voltage differential between V_{CC} and V_{IN}. Unfortunately, the performance of the 8038 is not sufficiently linear to allow this simple interface arrangement to work. A linearization circuit must be added.

The linearization requirements of the 8038 can best be grasped by examining and understanding the way it functions. Initially, the 8038 generates a triangular wave which is then used in the derivation of the sine and square waveforms. The triangular wave is formed by two voltage-controlled current sources (VCCS), equal to I_1 and $2I_2$. One of the current sources (I_1) is always on; the other one ($2I_2$) is switched, so that an external capacitor is alternately charged and discharged.

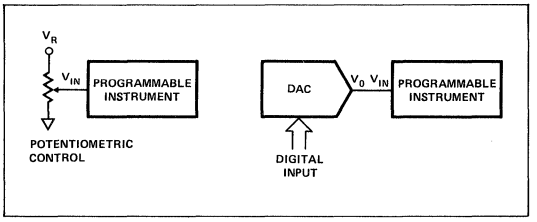


Figure 1. Simplified Representation of Analog and Digital Control: (a) Potentiometric Control; (b) Digital Control.

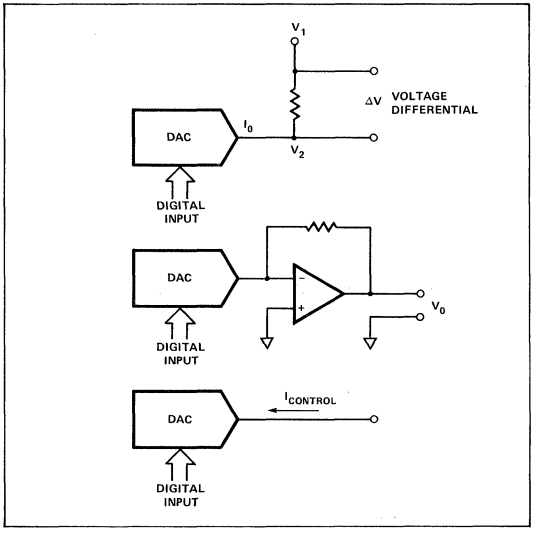


Figure 2. Control Configurations: (a) Differential Voltage Control; (b) Ground-Referenced Voltage Control; (c) Current Control.

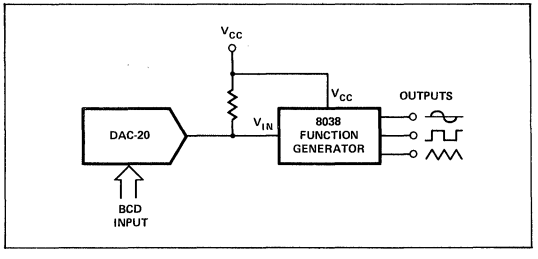


Figure 3. Basic Digital Control Configuration Using DAC-20 and 8038 Function Generator IC.

A simplified circuit diagram for the 8038 VCCS is shown in Figure 4. The VCCS output is given by:

$$I_1 = \frac{V_{IN} + V_{BEQ1} - V_{BEQ2}}{R_A} \quad (1)$$

This current source is not linear enough for the digital programming because V_{BEQ2} varies with I_1 while V_{BEQ1} does not. Adding a feedback amplifier to the VCCS, as shown in Figure 5, makes the output very linear by forcing the voltage at Pin 4 to equal V_{IN}, so that the VCCS output is simply:

$$I_1 = \frac{V_{IN}}{R_A} \quad (2)$$

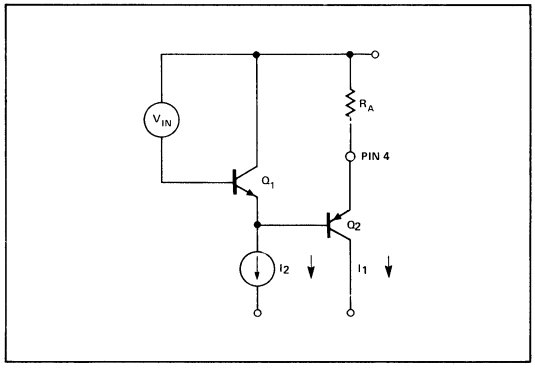


Figure 4. Simplified Circuit Diagram for the 8038's Voltage-Controlled Current Source.

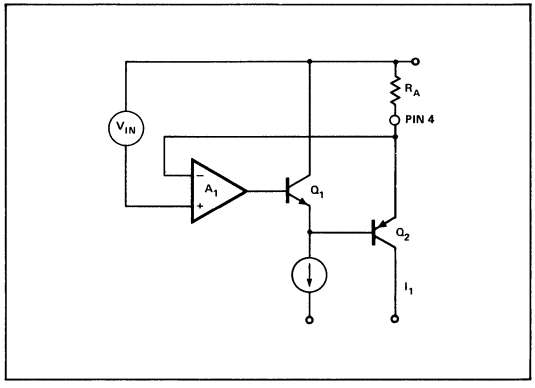


Figure 5. Improved VCCS with Added Feedback Amplifier.

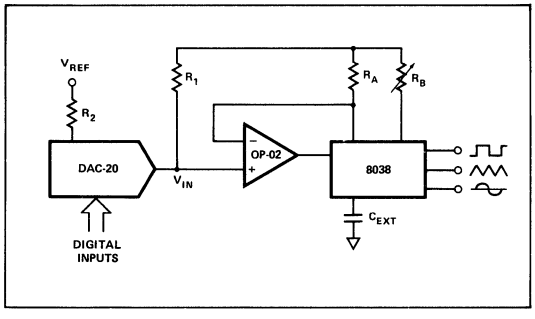


Figure 6. Digitally Controlled 8038.

The excellent linearity of the current source permits the output frequency (f_{out}) of the 8038 to be controlled by the DAC as shown in Figure 6. The digital inputs to the DAC set the voltage at point V_{IN}, and thereby control the output frequency of the 8038. R_A and C_{EXT} set the frequency range of the 8038 and R1 and R2 set the increment at which the frequency changes (although there are two current sources, the lowest sine wave distortion is obtained when $I_1 = I_2$; therefore, only R_A need be considered in calculating f_{out}).

The internal comparators of the 8038 limit the triangle wave amplitude to 1/3 V_{CC}. If $I_1 = I_2$ so that rise time = fall time, and $I_1 = V_{IN}/R_A$, then

$$f_{out} = \frac{-V_{IN}}{2/3\ V_{CC}\ R_A\ C_{EXT}} \quad (3)$$

The voltage at the output of the DAC-20 is given by:

$$V_{DAC} = V_{IN} = \frac{V_{REF}}{(R2)} \times \frac{N}{100 \times R1,} \quad (4)$$

where N is a two-digit BCD number. The most significant digit of the DAC-20 (comprised of four binary bits) can overrange to hexadecimal F (equivalent to decimal 15) so that N can range from 1 to 159.

The complete function generator schematic is shown in Figure 7. The component values listed will control the 8038 output from 100Hz to 15,900Hz, which covers almost all of the audio range. (Note that a 00 input should halt the generator; however, leakages and offsets keep the generator operating — in a bread-board version, the output was 19Hz.)

S_1 and S_2 are hexadecimal and decimal thumbwheel switches, respectively, for setting the desired frequency. Frequency linearity is excellent with f_{out} within 2% of programmed value over the entire frequency range. Sine wave distortion can be adjusted to less than 1%, and varies less than ±0.2% over the output range.

The Precision Monolithics REF-02 supplies a very stable reference voltage to R3, which sets the DAC-20 full scale current at 3.18mA. R1 converts the DAC output current to a voltage at the noninverting input of the OP-02, which then sets the f_{out} of the 8038. D1 and R6 protect the 8038 input from transients during power supply turn-on and C1-R5 roll off the op amp loop.

Since the DAC-20 has a high-compliance current source output, an external voltage source can be applied at V_{IN} if external control of f_{out} is desired. A modulating voltage can also be capacitively coupled into V_{IN} to provide a frequency-modulated output. Another way of modulating would be to apply the external signal to the DAC reference input to modulate the reference voltage.

Calibration of the generator is straightforward. Since the 8038 symmetry adjustments affect frequency, these are performed first. With a digital word of F9 (HEX) applied to the DAC, RB2 is adjusted for one 50% duty cycle square wave output and R13 and R14 adjusted for lowest distortion sine wave. Then, with a DAC input of 01, R11 is adjusted for a

50% duty cycle square wave and R7 for f_{out} = 100Hz. Finally, with a DAC input of A0, R2 is adjusted for f_{out} = 10kHz and the calibration is complete.

For audio testing, a generator with logarithmic sweep is very desirable. The addition of only 3 IC's provides log sweep as well as programmable counters on the input of the DAC-20. When S3 is open the oscillator will produce 16 cycles at each frequency step, producing a logarithmically related sweep. The log nature of the sweep is shown by the controlling equation for the counter.

$$\text{Count} = \int \frac{fo}{16}\, dt$$

but the frequency out, fo, is proportional to the count

$$fo = 100 \text{ count}$$

$$\frac{fo}{100} = \int \frac{fo}{16}\, dt \qquad \text{or} \qquad fo = \frac{16}{100}\frac{dfo}{dt}$$

When S3 is closed, the 74192 and 74193 counters act as transparent latches, so that thumbwheel switches S1 and S2 can be used to program f_{out}.

Microprocessor control of the generator is very simple since the DAC-20 is compatible with all logic families. Any CMOS, NMOS, or bipolar output device will drive the DAC-20, or a memory write pulse can be used to latch data into the counters (Figure 9). If the counters are used with µp control one bit of an I/O port or an external switch must be used to select swept or programmed output.

The "intelligence" added to this instrument by DAC control allows operation from µp or thumbwheel switches and permits easy interface to the IEEE 488 bus with the popular GPIB chips.

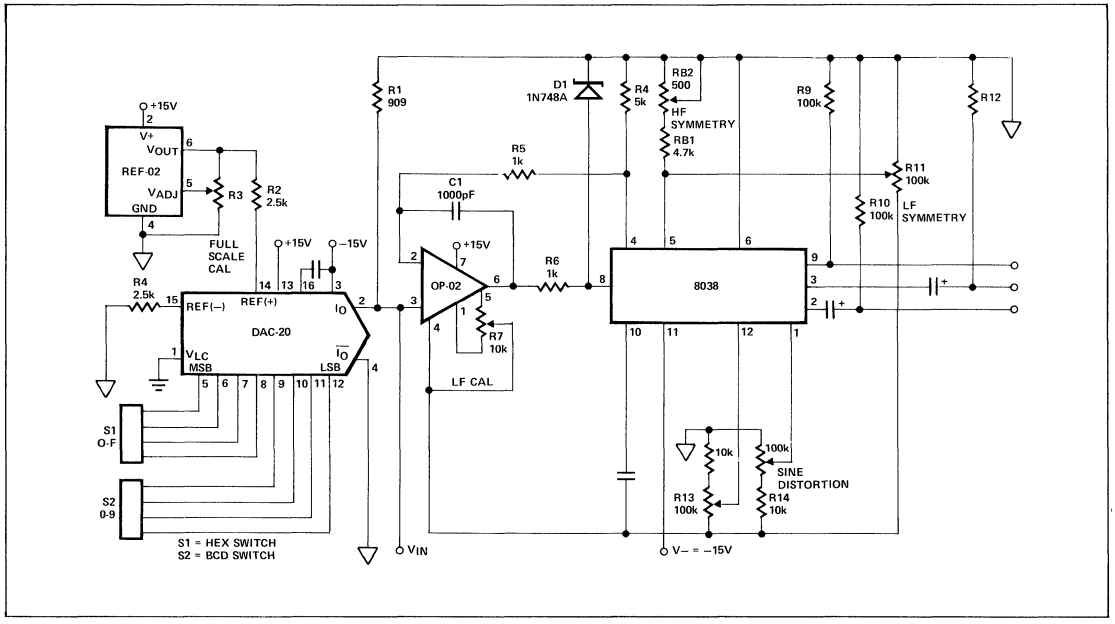


Figure 7. Complete Circuit Diagram for Programmed Function Generator.

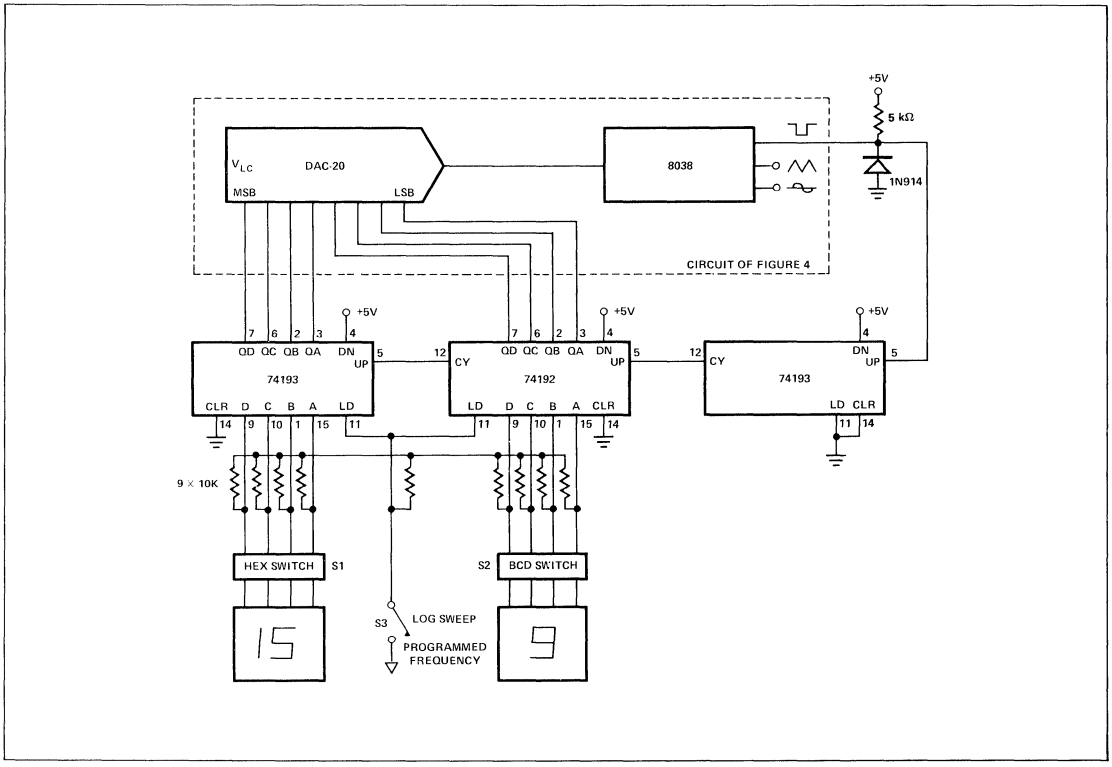


Figure 8. Log Sweep Modification of Programmable Function Generator.

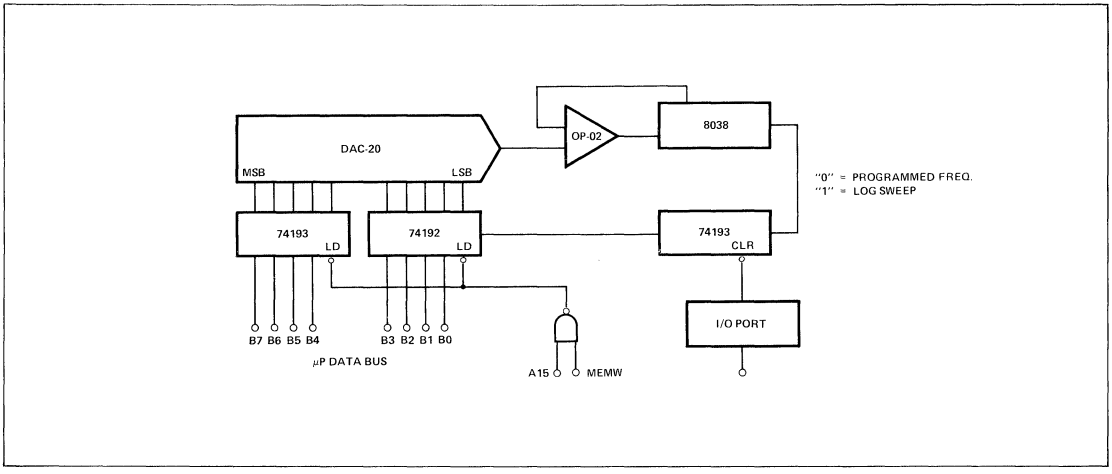


Figure 9. Microprocessor Interface to Function Generator with Software Selectable Sweep.

APPLICATION NOTE 48

DESIGNING DIGITAL REPEATERS WITH IC'S

by B.W. Berry

This note describes the use of the RPT-81 and the RPT-82, PCM carrier repeater integrated circuits, which perform all of the active functions required for a regenerative repeater operating at 1.544-2.048 Megabits per second (Mbps) data rates on PCM lines.

Most of the problems in digital voice transmission are caused by the transmission medium itself rather than by the transmit or receive hardware.

This is particularly true for the most commonly used medium, twisted-pair cable designed to carry analog voice-frequency signals in the 300- to 3700-Hz frequency range.

As more and more transmission routes are called upon to accommodate digital data, it becomes important, in terms of system cost and installation time, to use existing cable interchanges. As a result, audio-frequency-grade cable is called upon to transmit high-speed digital data. This was made possible through the development of digital regenerators.

A digital regenerator consists of two repeaters, one in each transmission direction. Repeaters receive digital data streams and retransmit them to the next receiver position. Current integrated-circuit repeaters eliminate the loading coils that were originally used to introduce a flat-band response over the voice band. A T1 repeater (the U.S. standard) can accept a degraded signal, regenerate it, retime the pulse stream, and transmit it over another 6000 feet of twisted-pair cable. The action taking place in the regenerative repeater stage is depicted within the dashed-line portion of Figure 1. When digital carrier repeater circuits are installed, the operating error rate for carrier systems with audio-grade cable pairs is well within the limits necessary for adequate voice communication.

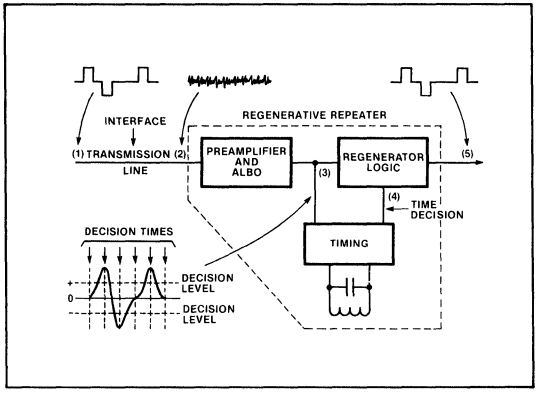


Figure 1: The functional elements of a regenerative repeater section are shown within the dashed line. The results being a re-shaping of the incoming pulses, which in turn enables a re-timed and regenerated data stream.

Several different integrated circuits are being used in the latest generation of repeater equipment. These circuits have cut the number of components required to build a digital regenerator while improving its capabilities and performance.

To grasp the concepts concerning use of the devices, it is helpful to first examine some of the basic theories relating to practical digital transmission.

The present T1 carrier uses bipolar or mark inversion digital format shown in Figure 2. There are several specific advantages provided by this coding system.

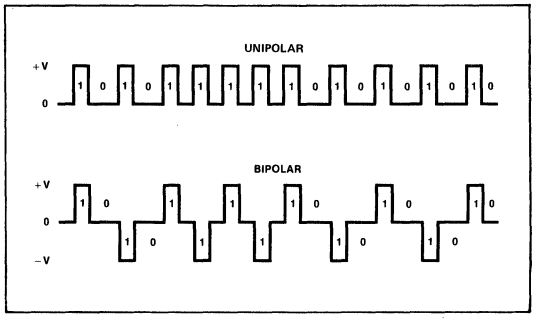


Figure 2: In the bipolar (alternate mark inversion) digital format, alternate 1 bits are inverted in polarity.

First, the maximum energy of the waveform is found at one-half of the bandwidth (data-transmission rate) of the system. For a binary code (see Figure 3), the most significant frequency is found at the zero level rather than the mid-frequency. This means that the energy spectrum encompasses double the bandwidth (3.088 MHz) of the transmission rate for the T1 rate. The bipolar scheme keeps the spectrum within the 1.544-MHz bandwidth of the transmission system.

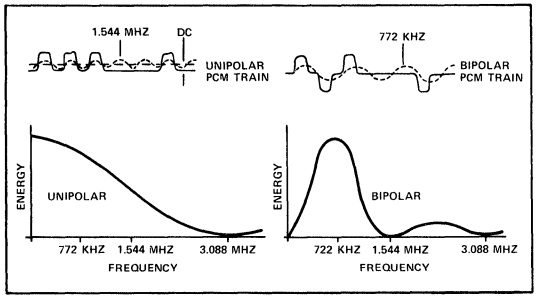


Figure 3: The (alternate mark inversion) bipolar digital format keeps the spectrum within the 1.544MHz bandwidth of the transmission system. The average dc component on the transmission pair is zero.

Another important characteristic of a bipolar code is that the average dc component on the transmission pair is zero. This is important in regenerator development because it allows the same channel to be used for data transmission and power supply. An advantage of this design approach is that extra pairs for powering a repeater location are not necessary with a simplex power arrangement.

Still another advantage provided by bipolar code is the capability to detect single-bit errors within the transmitted data. Since the sequence of pulses has alternating polarity, the absence of a pulse will be received as a bipolar violation. Though error bursts could produce incorrect error counts, it has been purported that the difference between the true error rate and measured error rate is negligible in high-error channels.

If the error rate is low enough to show differences for burst-error occurrences versus single-error counts, the channel will probably be performing well enough to make the difference unimportant.

There are also some problems associated with bipolar coding. For example, since retiming depends on the incoming pulse stream, a long series of zeroes will have a very low energy content. Some oscillator-resonant circuit designs may then damp out completely and fail to restart. This will depend on the Q of the circuit.

Some carrier designs have moved to different coding schemes to restrict the number of zeroes possible in a legal transmission. In European systems especially, the HDB3 code (high-density bipolar with no more than three zeroes in succession) has often been incorporated. In this discussion, however, the straight bipolar coding scheme will be considered when determining the relationship of the active components within the repeater.

The functional components of a repeater integrated circuit are illustrated in Figure 4. The repeater amplifies the incoming signal and equalizes the received signal to compensate for attenuation distortion and phase distortion. The analog amplifier also has a feedback loop that provides for a variable amplification dependent on the threshold detected for the incoming pulses (either positive or negative). Either of two methods can be used to obtain equalization: in the first approach, a fixed value of cable attenuation is provided; in the second approach, automatic equalization can be used with constant modification taking place to handle variable line lengths in that transmission section. The monolithic approach provides an equalization network and variable line matching circuitry.

The repeater must provide a timing-recovery circuit to extract the data transmission clock from the incoming pulse train. The recovery circuit will normally comprise a resonant circuit tuned to the peak energy level of the incoming signal. The resonant circuit is "energized" by the transitions at the received channel with the resonant frequency dependent on the Q of the circuit. A higher Q can allow the circuit to remain active through longer periods of zero signals levels. The recovered timing pattern is then used in the reproduction of the incoming series of pulses.

The repeater must be capable of differentiating between a data pulse and channel noise. The noise due to adjacent channel pairs or interference due to signals in adjacent time slots must not negate the reception of the proper incoming pulse sequence. Jitter due to timing variations from repeater section to repeater section can disrupt the signal detection

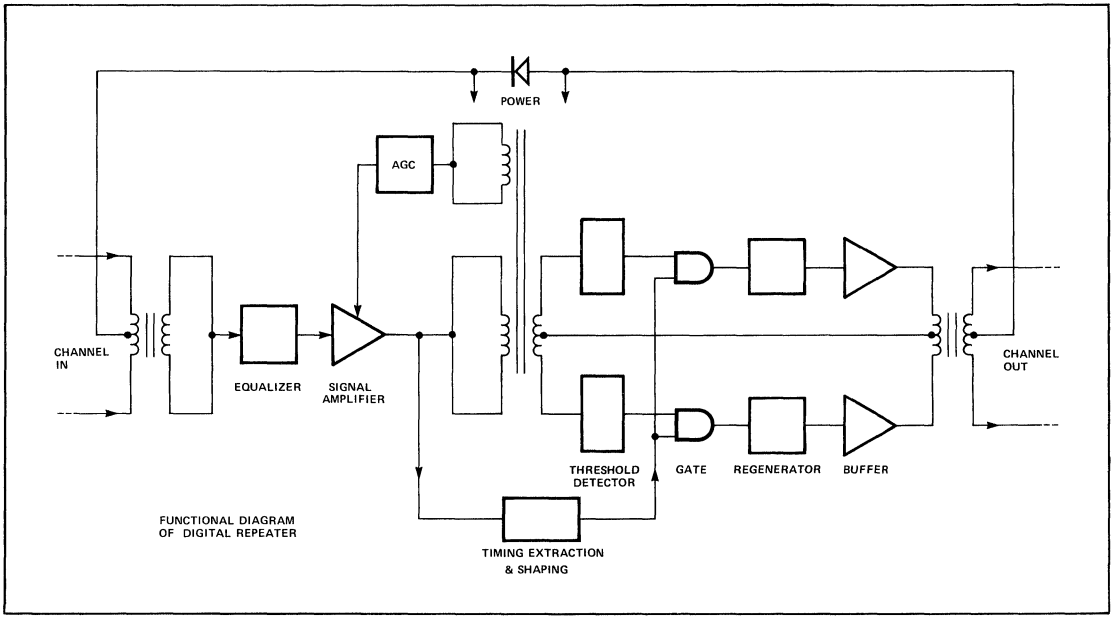


Figure 4: Functional diagram of a repeater integrated circuit shows the equalizer (to compensate for attenuation and phase distortion) and analog amplifier with feedback to provide variable amplification dependent on the detected threshold.

by causing pulse thresholds to be measured at the improper intervals. Pulse detection is accomplished by the detection of proper threshold levels and correct timing intervals. The repeater then will retime the detected levels to provide for a new pulse train. It is important when retiming the waveform that the input from the threshold detector precede the timing strobe. This ensures that the output pulse will follow the reconstructed timing, reducing the jitter components.

The final functional block necessary for the complete repeater function involves the regeneration of the output pulses. The buffer stages drive the output transformer to produce a posi-

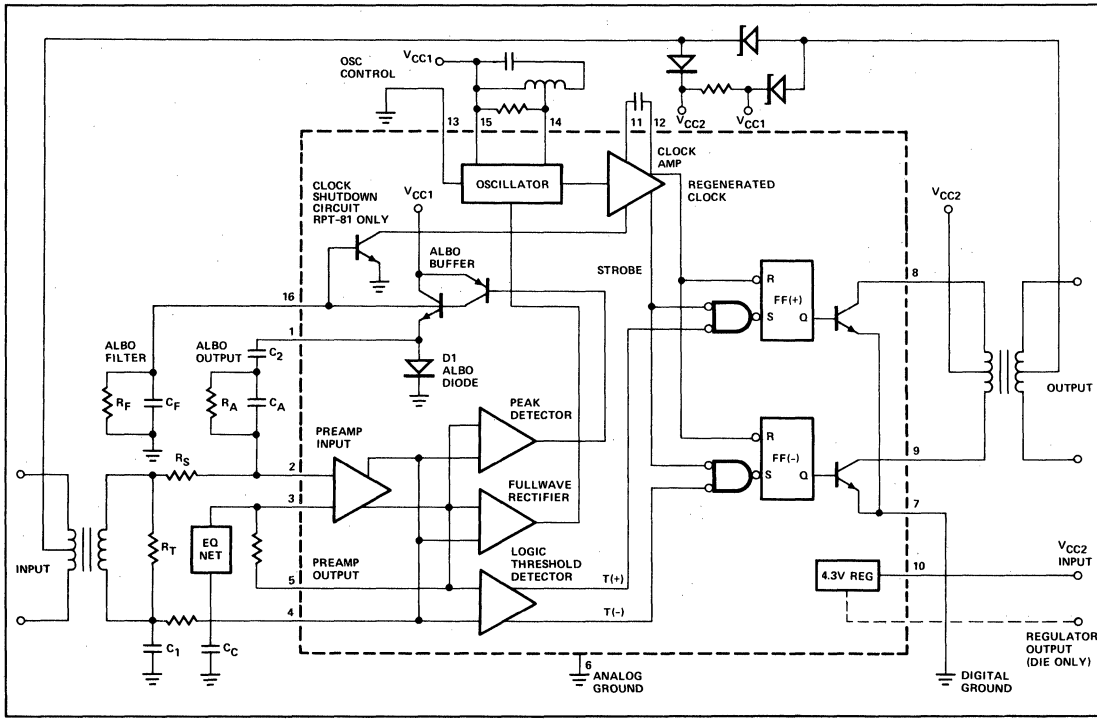


Figure 5: In PMI's RPT-81 and RPT-82, equalization and amplification of the incoming pulse train takes place through an amplifier with an external network controlled by feedback.

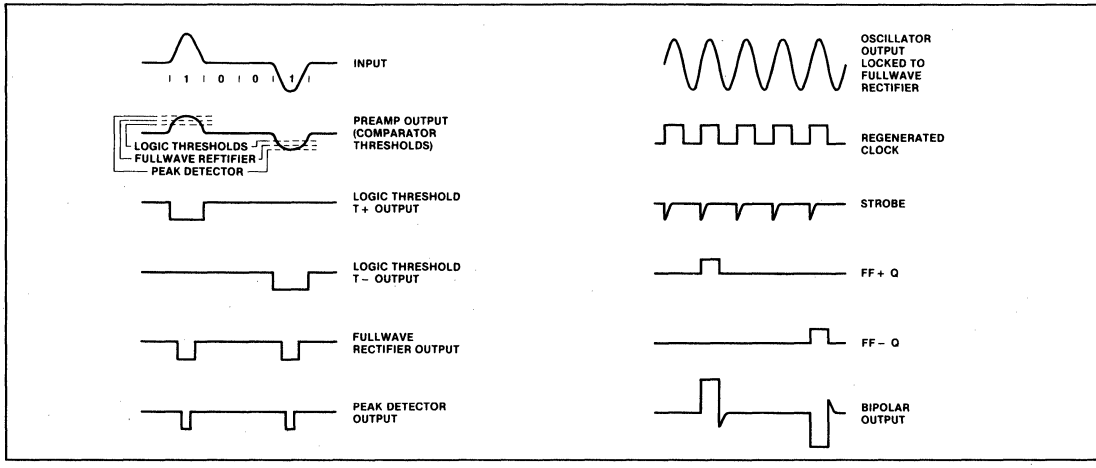


Figure 5A: Voltage waveforms at the outputs of the various functional blocks within the RPT-81 integrated circuit. The output pulses of the amplifier trip some combination of the level-detecting comparators.

tive or negative signal on the channel output pair. The design is such that, in most instances (U.S. and European), the generated signals are nominally square pulses. Different theories as to improving performance by band-limiting the output stage have been discussed and, in some instances, implemented. However, the majority opinion still seems to favor the square-wave components.

The repeater can be considered a combination of discrete yet interrelated functions. The overall function of the repeater is the shaping of incoming pulses, the retiming of these pulses, and the generation of an equivalent output stream.

IC APPROACH

In PMI's RPT-81 and RPT-82, the equalization and amplification of the incoming pulse train is achieved through a bipolar amplifier with an external equalization network controlled by feedback from the amplifier outputs (Figure 5). The result is that the pulses peak so the majority of the pulse amplitude is restricted to its own time slot.

The automatic attenuation of the pulses is done by an ALBO (automatic line build-out) circuit actuated through a buffer circuit on chip. The output pulses of the amplifier will trip one or all of the three level-detecting comparators. In terms of the ALBO feature, if the incoming pulses exceed a specified peak-reference value, the comparator generates current pulses that flow into the ALBO filter external to the chip and charge capacitor C_F.

The voltage at the ALBO filter is applied, in turn, to the base of the internal ALBO buffer transistor. The buffer will turn on when its base voltage exceeds approximately 1.7 volts. This 'on voltage' is also specified in the electrical characteristics of both the RPT-81 and RPT-82. The ALBO diode acts as a series impedance, normally much larger, and therefore the dominant factor, than the shunt impedance of the external network. As the current increases at the buffer, the diode impedance decreases and the shunt impedance becomes dominant.

The overall effect is to increase the ALBO attenuation as the filter voltage level increases. The result is that the feedback loop will adjust itself until the pulses out of the preamplifier are equal to the fixed reference. The references for the other level detector and rectifier are set at fixed ratios of this peak reference. Therefore, their thresholds are fixed with respect to the pulse shape and relative amplitude.

On the RPT-81 (not the RPT-82), a clock shutdown circuit, which is activated by the current levels from the ALBO buffer, is also provided. This shutdown circuit turns off the clock amplifier at low input levels, thus neither the regenerated clock nor the strobe outputs are enabled at the output buffer flip-flops. The circuit was incorporated to prevent random-noise pulses from being reproduced as valid output pulses. The problem, however, can be that at long line lengths the correct signals are too low in energy to activate the clock circuit. Presently, PMI has customers using both schemes in their repeater designs.

The timing of the circuit is based upon the pulsing of a resonant tank circuit. The full-wave-rectifier comparator output pulses the tank network. The pulses try to "force" the oscillator circuit to phase lock to the incoming pulse waveform, while the tank attempts to resonate at its preset (with external components) frequency. The result of the two factors is a clock circuit that runs at an average bit rate for the incoming waveforms.

Again, the value of Q for the tank circuit will help determine the oscillator accuracy. If the Q is high, the resonant frequency dominates and it is more difficult to phase-lock to the incoming pulse rate. A high Q circuit also changes considerably with the temperature and long-term component drift. A Q value that is too low will cause adverse affects on the oscillator circuit by the jitter present in the pulse stream. This means the jitter will then also be transferred to the output pulse train as well. For both the RPT-81 and RPT-82, Qs of greater than 75 are recommended.

The logic-threshold comparator provides the detection function for incoming pulses. For positive received pulses, a negative pulse is generated on the T+ line; for incoming negative pulses, a pulse is sent on the T− line. The clock amplifier "squares" the timing waveform from the oscillation circuit and produces a square clock signal and a negative strobe pulse. The strobe pulses are 'anded' with the logic outputs (T+ or T−) to set the output buffer flip-flops.

The strobe is coincident with the positive edge of the clock signal generated by the tank circuit. Once the appropriate flip-flop is set by the combination of the logic output and the strobe pulse, the output driver stage causes current to flow through the proper half of the output transformer, thus regenerating the received bipolar pulse. The falling (negative) edge of the internal clock signal serves to reset the output flip-flops and thereby terminate the output pulse. This is important to prevent the regenerated waveform from following the data threshold instead of the clocking circuit.

One option is made available to users of both the RPT-81 and the RPT-82. The internal clock oscillator can operate in either an injection-locked mode or a pulsed-tank mode. By grounding a pin on the device, the oscillator is free-running but is phase-locked to the full-wave rectified output. With the pin open, the oscillator will only operate when pulsed by an incoming signal. The circuit then "rings" until the next incoming pulse is received from the rectifier. In both cases, the overall effect is to phase-lock the resonant circuit to the average frequency of the pulse train.

The completed T1 repeater may look something like Figure 6 in a typical configuration. The input transformer provides a two-to-one step-up from the 100-ohm characteristic impedance of the line. The matching impedance, in this case, is doubled to approximately 400 ohms. A fixed attenuation is added to provide a fixed line build-out of approximately 6dB. The automatic build-out then provides a varying attenuation for line lengths up to 36dB.

The equalization network is added to give the preamplifier higher gains at higher frequencies. This compensates for the roll-off characteristics of the preamp and the transmission line.

The oscillator tank circuit provides the resonant frequency for the oscillator. It is controlled by current pulses generated as the incoming waveform is received.

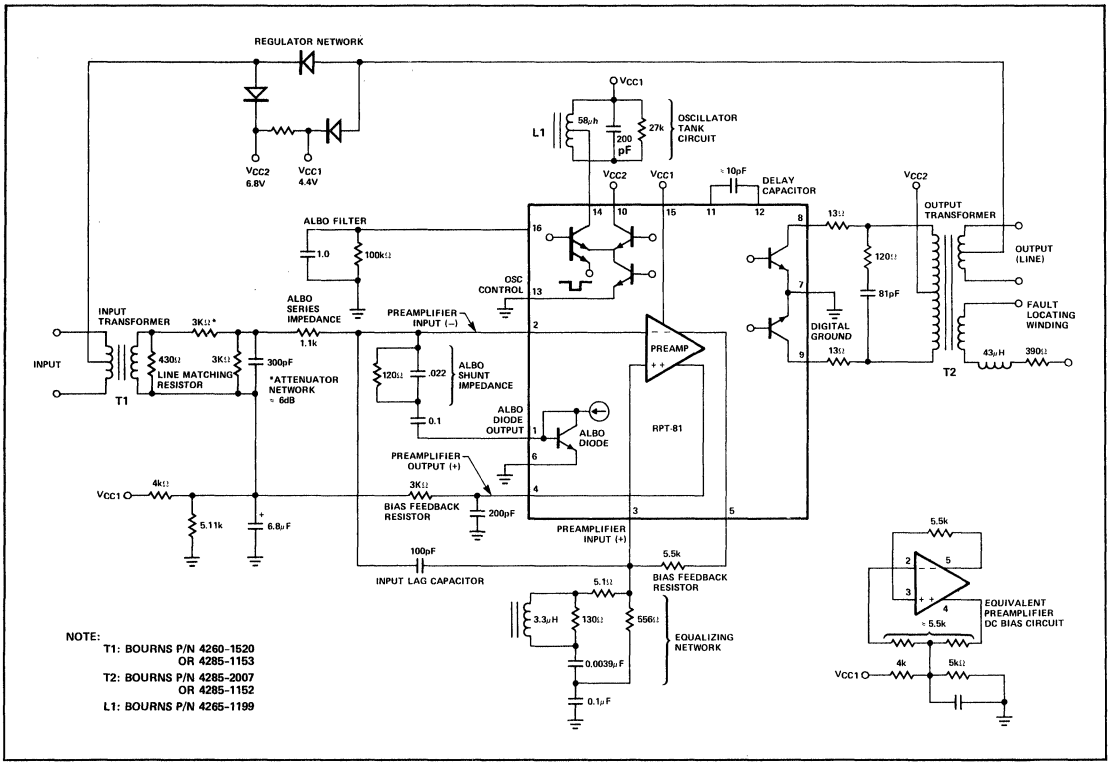


Figure 6: The complete T1 repeater system (1.544MHz) using the RPT-81 integrated circuit. The input transformer provides a 2:1 step-up from the 100ohm line impedance.

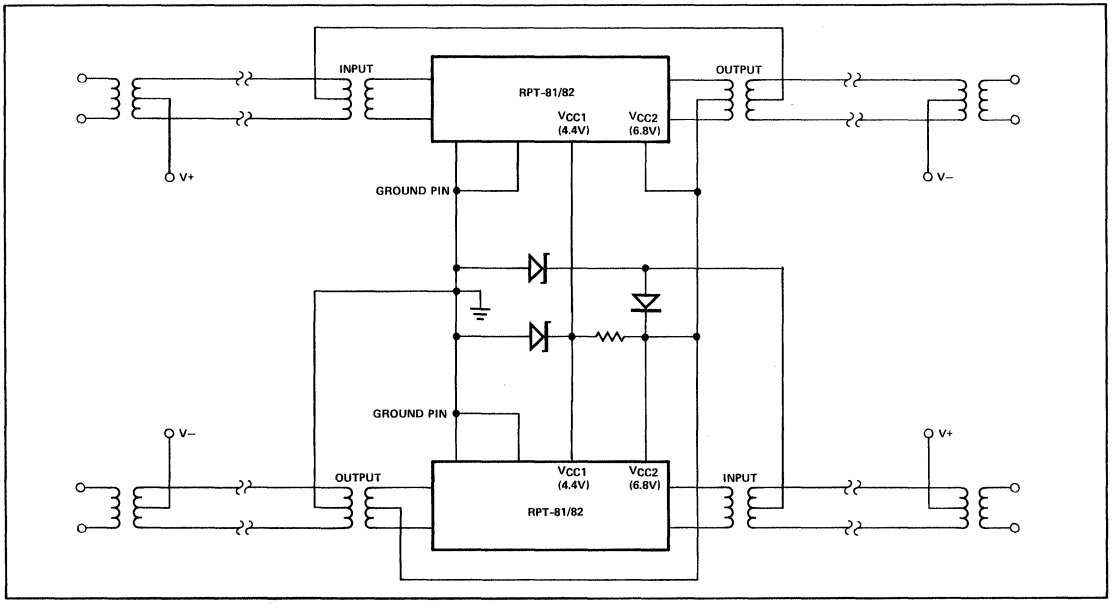


Figure 7: The simplex power supply design consists of two zener diodes and a diode float connected to the center taps of the line transformers. Nominal voltages are 4.4 and 6.8V.

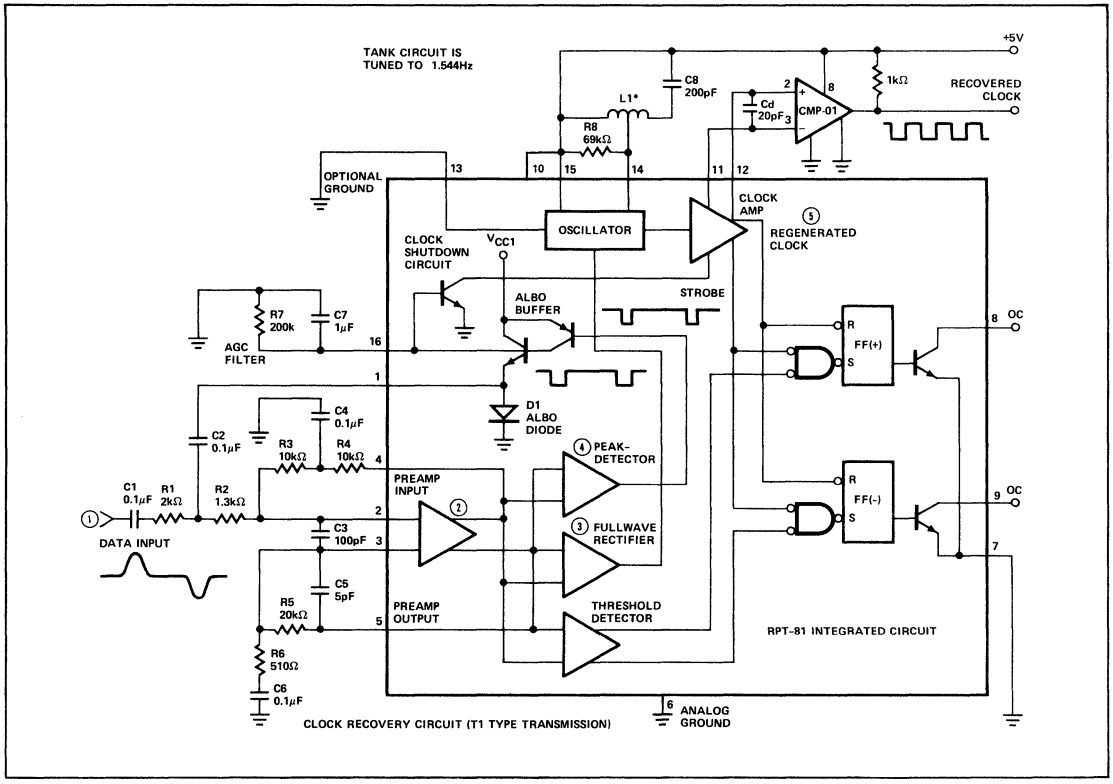


Figure 8: Integrated-circuit repeaters can also be used in clock-recovery circuits, as shown. This circuit can work from a single 5V supply.

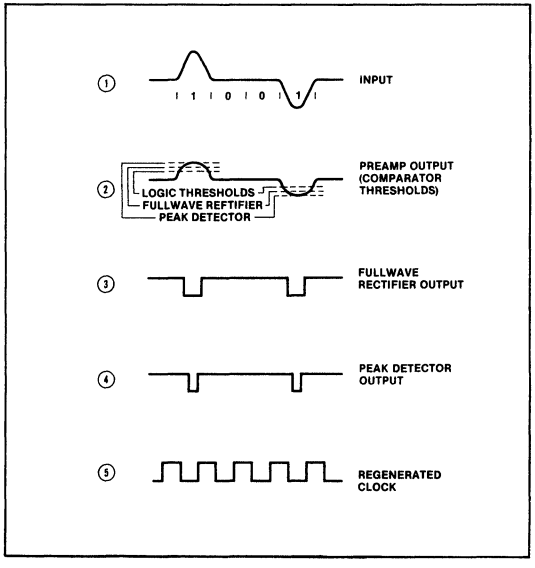


FIGURE 8A: Shows the voltage waveforms within the circuit.

The ALBO filter aids in integrating the pulse output of the detector. As the voltage increases, more current flows through the ALBO diode, and the line build-out is characteristic of longer line lengths.

The power-supply current is available over the signal pair. The simplex power design consists of two zener diodes and a diode float connected to the center taps of the line transformers (Figure 7). The nominal voltage values required are 4.4 and 6.8V.

This design meets the specifications called for in a T1 carrier repeater. The integrated circuit uses less than 13mA total current (both voltage supplies). This means the maximum output current for the total repeater circuit will be under 50mA at worst-case conditions (all ones output signal).

A final application of the integrated circuits is the use of the repeater device in a clock recovery circuit. Data transmission is becoming more important in areas other than long-distance digitized audio. In these instances, the capability of recovering clocking from the data stream can be advantageous. This can mean single-pair connections that can transfer data without additional wiring for timing and clock signals. Using the RPT-81 in conjunction with a precision comparator, such as the PMI CMP-01, will provide a recovery scheme capable of reproducing a clock waveform from input levels as low as 35mV peak-to-peak. Any system that requires clock retrieval from a data signal and synchronization to that signal can use a circuit similar to this design shown in Figure 8.

The test circuit was operated with an AMI incoming code at frequencies from 64kHz up to 1.544MHz. In the published design, the incoming data waveform is capacitively coupled to an input attenuator using fixed external components and the internal ALBO diode. Since the impedance at pin 1 of the device varies inversely with the amplitude of the input signal, the voltage at the preamplifier input (through resistor R2) will be held to less than 100mV peak-to-peak amplitude. This gives the design an input dynamics range of greater than 45dB while still producing a constant output waveform.

This circuit (Figure 8) can work from a single 5-Vdc supply, and the tests that have been completed show none of the external component values to have critical tolerances. The design can be used to recover clocking from an incoming data stream—again a capability that has proven advantageous for designers of data interfaces in many areas other than telecom carrier exchanges.

When considering new applications or new repeater designs, several possibilities have already been approached. Since the European line requirements are somewhat different from those in the U.S., a modification in the repeater design has been suggested. For example, providing a better line simulation and response over a longer line could require more than one ALBO network. A chip providing multiple ALBO connections could prove important. In addition, again due to the longer line lengths, the current requirements are even more critical, a device requiring only a 5-V supply voltage could be used in a lower current configuration.

In the U.S., work is presently being done with the use of a duobinary coding design. This would require some modifications to the present RPT-81 and RPT-82 to provide the accuracy necessary to reduce intersymbol interference.

In all design areas, higher data rates are being considered as well as the basic 1.544MHz (or 2.045MHz). In such designs, monolithic devices could also be valuable to improve transmission and data retrieval.

APPLICATION NOTE 49

DESIGNING A MULTIPLE-CHANNEL CODER/DECODER WITH BIPOLAR DEVICES

(PRESENTED AT ELECTRONIC DESIGN TELECOM CONFERENCE)

by B.W. Berry

Encoding analog to digital signals and decoding the digital words back to analog waveforms can be accomplished through the use of several different systems configurations. This note describes the building blocks needed to produce an economical shared-channel coder/decoder circuit capable of meeting all necessary system performance requirements while costing less, on a per channel basis, than a single-channel codec system.

A codec system in which coding and decoding is provided for every channel is shown in Figure 1. In theory, when the "digital transmission highway" reaches the individual phones, per-channel codecs become the necessary architecture. However, a shared-channel system, accomplished by multiplexing several analog channels and digitizing them via a shared coder, offers many advantages. Besides cost savings, these advantages include reduced circuit board area, reduced die area, easier incoming device inspection and better component reliability guarantees.

The first "commercial" use of digital transmission within the telephone network is normally attributed to the T1 Carrier, initially used in 1962. The T1 Carrier incorporated shared-channel coders and decoders implemented with discrete components and situated on several circuit boards. The codec portion of the T1 Carrier was actually a linear device, and compression or expansion of the analog signal was carried out through the use of a diode matrix. Later years served to provide various improvements in the initial design. In 1968, the D2 interface used the μ-law companding logarithm to replace the linear approximation involved in coding and decoding. This design continued to evolve until 1975, when, in the D3 interface, shared-channel coders and decoders were contained on 40-pin hybrid circuits. For every 24 channels, four of these hybrid circuits were needed to complete the analog-to-analog conversion. This design was used up to 1978 when the D4 system further reduced the conversion circuitry to two hybrids (in DIPs) per 24 channels, a 40 pin coder and a 32 pin decoder.

European designs followed a similar pattern of improvement; the basic system was somewhat different in that 32 channels using a higher frequency clocking scheme were employed. However, the most economical design approach seemed to designate sharing the coders and decoders among multiple channels.

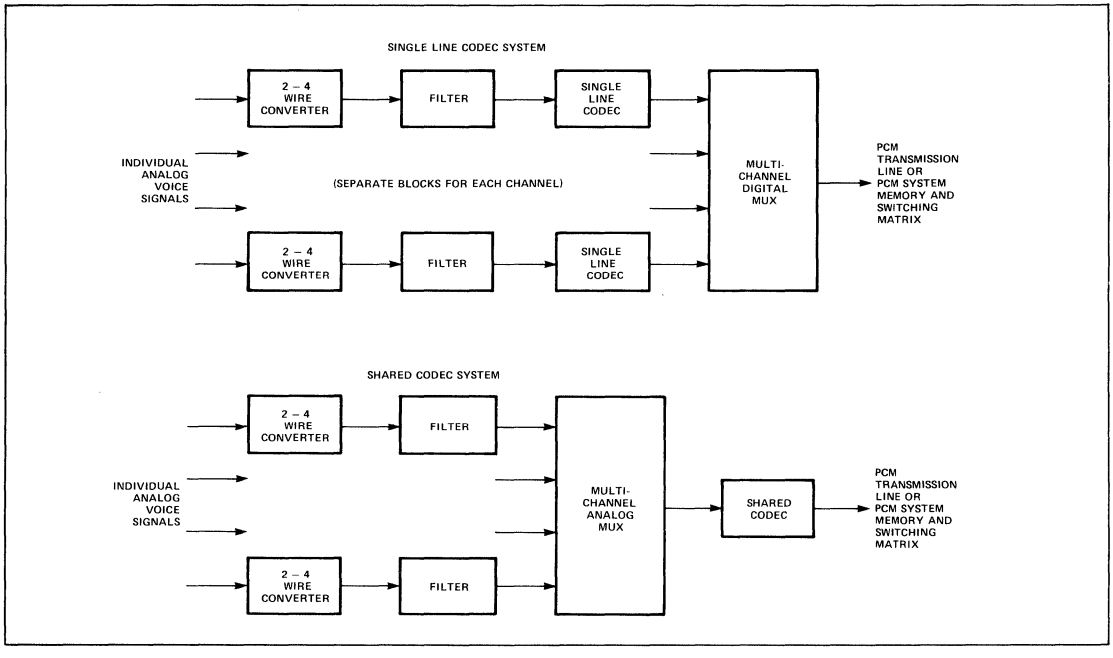


Figure 1: Block diagrams depict shared-channel and single (per-channel) codec configurations.

The "heart" of the shared-channel coder or decoder became the companding D/A converter. All of the other components needed are commonly used in digital-to-analog conversion designs throughout industry. The part unique to telecommunications designs (unique as initially envisioned) is one that supplies the non-linear transfer function DAC necessary to provide a wide dynamic range while minimizing bandwidth requirements. Generally, the function required is similar to that provided by linear converters (as shown in Figure 2). The difference lies in the current output DAC; in a companding system the step current must increase as multiples of the previous step size, not linearly. The step size is dependent upon the chord, or essentially the distance from the zero level. The reference amplifier sets the bias current for the chord current generator. The value of the chord current is selected by the digital, 1-out-of-8 selector and is fed to the step generator. The step generator current is a function of the chord pedestal current and the digital input value.

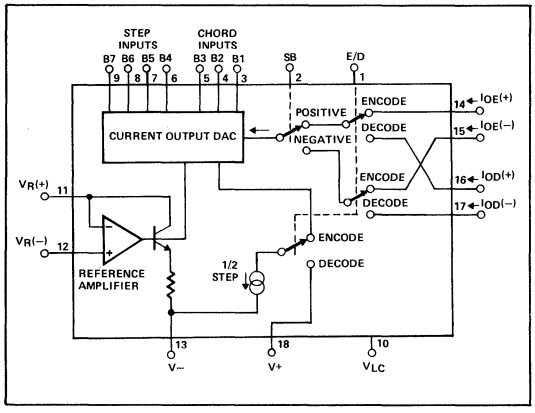


Figure 2: In a companding DAC, step current increases as multiples of the previous step size.

As can be seen, the device provides a select mechanism to allow either an encode or decode transfer. The difference is a 1/2 step to minimize quantization distortion between the encoding and decoding circuits.

The restrictions encountered in producing and designing such a part lie mainly in the speed and accuracy requirements. Bipolar technology allows the completed companding D/A converter to decode 24 or 32 channels (5.2 or 3.9 μsec per channel) and encode, with the successive approximation technique, up to 8 channels.

This is the basic premise of the shared-channel "codec" approach offered by PMI. Through the use of high-speed bipolar conversion, multiple analog channels are digitized using a single set of devices. The devices incorporated all have die areas less than 10,000 square mils and are readily manufacturable using PMI's bipolar processing techniques. The cost savings provided by multiple-channel systems are magnified as the systems incorporate more monolithic devices.

Additional advantages are obtained; since the devices are all relatively small, the required circuit board area is reduced on a per channel basis. The number of IC's required per channel is less than one, and all of the integrated circuits have 18 pins or less.

A SHARED EIGHT-CHANNEL DESIGN

One way to see the subtleties of a shared-channel design is to construct one. PMI has had an eight-channel system available for customer analysis for two years. In this time, more than twenty customers have evaluated its performance.

The encoder (shown in Figure 3) is comprised of the companding D/A converter (μ-law or A-law), an analog multiplexer, a monolithic sample-and-hold, a voltage comparator, and a voltage reference. To complete the successive approximation technique, a special digital register is added. The same analog components, with the substitution of a high slew-rate operational amplifier for the comparator and discarding the sample-and-hold, will produce a multiple channel decoder. In this case, a digital latch is added to interface from the digital data base to the digital-to-analog converter. Before looking at performance on an analog input to analog output basis, the individual A/D and D/A circuits will be discussed.

The encoder design is capable of generating an 8-bit digital word every 15.6 μsec. This means 8 analog input channels can be switched, sampled, and converted to digital representation by a single such circuit. To describe the encoder's

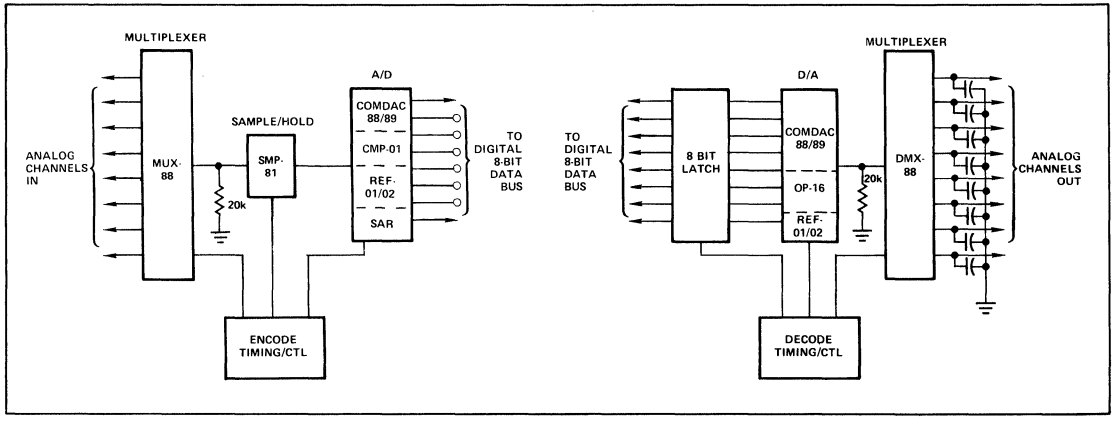


Figure 3: Components of encoders and decoders.

function, it is helpful to begin with the clocking waveforms used to time the successive approximation register, the multiplexer, and the sample-and-hold.

When allocating time to the individual components, the first area to be considered is the successive approximation sequence. Considerable time has been spent at PMI determining the most efficient method of minimizing the individual bit times while assuring adequate settling time as each step in the conversion sequence is reached. Initially, as shown in Figure 4, D/A converters in conjunction with the comparator had a combined settling time related to the bit being determined. As the approximation moved to lower order bits, the settling time required for the DAC and comparator increased. This was caused by delays in the internal switching of the DAC, and the fact that as lower order bits are selected, less current is switched to the output to drive the comparator. The result was that for the least significant bits to be determined consistently for small magnitude input signals, longer delay times between bits were necessary than for the higher-order bits. This led to the original 8-channel clocking scheme which provided increased 'bit' settling time as the approximation routine moved to the lower order bits. It was realized that by improving some of the internal characteristics of the DAC, this restriction could be relaxed, thus producing an easier system design. The results were the redesigned companding DAC's, the DAC-88 and DAC-89.

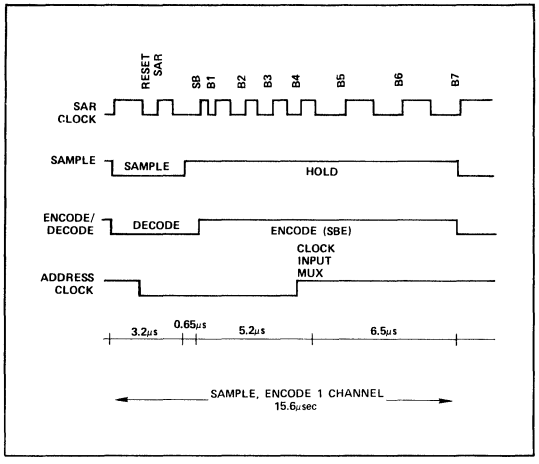


Figure 4: System clocks for original system.

With the present companding D/A converters, the system can allow a shorter time for the lower order bits (Figure 5). While still designing to an 8-channel time period, this means a single sub-multiple of the system clock can be used to directly drive the successive approximation register. Although admittedly designing a shared-channel system can seem to require more external circuitry, by careful consideration of the individual device characteristics, this extra design effort is actually minimal. In terms of the actual analog-to-digital conversion, the new PMI companding D/A converters (DAC-88 or DAC-89) are capable of completing the successive approximation sequence in just over 9μsec, this leaves more than 6μsec for the sampling of the analog signal prior to conversion.

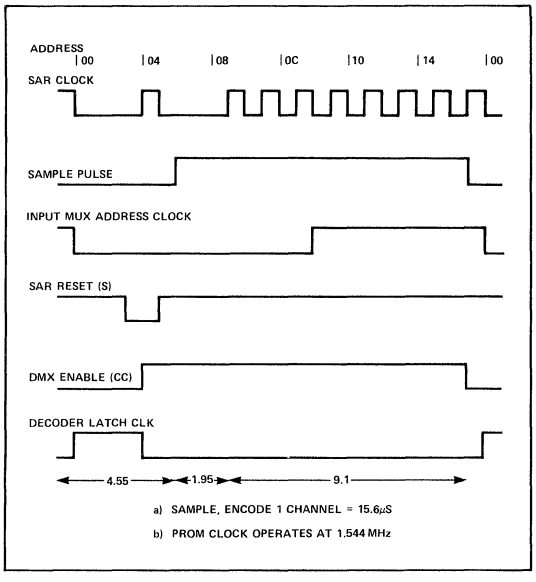


Figure 5: Improved performance provided by the use of DAC-88 and DAC-89.

The sample-and-hold time becomes the next most critical interval within the encoding period. Again, by testing the PMI developed shared-channel system, several interesting characteristics which might affect the system performance were observed. First of all, and, most obvious, is the required sample acquisition time. The typical time for the SMP-81 to acquire the input signal when varying between + and −5 volts is 3.5μsec. It is important to notice that the system timing also provides for nearly 2μsec of "idle" time between the sample-and-hold switching to the hold mode and the successive approximation register clocking in the sign bit (the first bit of the conversion sequence). This idle time, commonly referred to as hold settling time, assures that the sample-and-hold output has achieved the sampled input value. If there is any ringing effect due to the sample-and-hold switching from the tracking mode, by allowing some settling time, the accuracy of the digital conversion circuit will be improved. When clocking the sign bit in too soon after reaching the hold mode, for input signals less than −50dBm0, the sign bit is often in error, causing an enlarged zero crossing for the reproduced waveform. By assuring a sufficient hold settling interval, this zeroing effect is negated, and the performance of the encoder is improved.

CROSSTALK CONSIDERATIONS

Another major design consideration is the crosstalk in any analog system. In a multiple-channel converter (encoder and decoder) the crosstalk possibility is present due to the system use of analog multiplexing versus the digital multiplexing in per channel designs. However, crosstalk can be a factor in all systems. It is more a matter of when the problem is faced, and at what level of system architecture, rather than if it has to considered or not.

The major contributor to crosstalk within this shared-channel encoder design seems to be the input multiplexer and the

sample and hold circuit. Several precautions may be taken to aid to reduce the crosstalk levels of the system. The first consideration implemented was to allow ample switching time between incoming channels. The MUX-88 provides guaranteed break-before-make action when enabled. The switching time will consist typically of 200nsec to open, 400nsec separation interval between switch activations, and 200nsec for the next addressed switch to close. The address selector pointing to the next input analog signal then is not changed until the sample and hold has settled to its previously held value. This sequence assures no timing induced crosstalk due to active channels being selected simultaneously. Also, a 20kohm discharge resistor to ground is connected to the output port (common JFET drain) to provide an additional path for the multiplexer to discharge its old signal once the sample-and-hold is in the hold mode and the switch is changing addresses.

While testing several system configurations other than the 8-channel encoder, it became apparant that by alternating the signal inputs to the multiplexer with grounded inputs, crosstalk performance improved dramatically. In terms of a 4-channel encoder, this meant that after one active channel was sampled, the address leads were incremented to select an unused, grounded input. Then the multiplexer was clocked to switch the next analog signal into the system. Again, this leads to the conclusion that by using certain characteristics of the devices, increased performance levels are possible. So designers looking for additional crosstalk isolation can (by modifying the design and possibly adding an additional integrated circuit) produce the special performance levels. It is a matter of designing the system using individual components that allow each section of the design to be optimized.

The final part incorporated into the encoder is the voltage reference; the 5-volt (REF-02) or 10-volt (REF-01) references provide excellent output stability with little effect due to temperature variations. Although the demonstration unit shows separate references for the encoder and decoder, this was due more to circuit layout than design requirements. Each component has adequate load capability to provide the reference currents for several systems. Again this becomes a matter of system architecture, and the designer should select the appropriate reference distribution after considering economics and layout restrictions.

The encoder design was initially tested separately from the decoder. This was done by delivering a precision dc voltage level to one or more multiplexer ports. The parallel, 8-bit data output of the encoder was sampled using a digital logic analyzer. This set-up provided a method of continuously encoding a set voltage level and then measuring the consistency and accuracy of the digital approximation. The analyzer would also show any inter-channel interference caused by switching or device characteristics. Overall, this test method allows the user to vary devices individually and see the effect on the conversion process. It proved to be helpful in optimizing certain aspects of the circuit and defining the areas requiring special attention during the design phase.

The decoding circuit becomes a simpler design than the encoder, especially when considering that the system requirements are easier to fulfill. Even in a 32-channel system, the output channel rate allows for 3.9μsec settling time for each analog output level. The companding DAC's when used with a high slew-rate operational amplifier, such as the OP-16 have settling time more than adequate for their use in such designs. The important characteristics to consider are the accuracy requirements necessary to provide the proper analog signal reproduction at levels down to –60dBm0 and lower. It is in this regard, that some advantage is again apparent in the use of individual components, for PMI can provide a dc accuracy specification per companding DAC and test such performance for each production device. Both the μ-law and the A-law devices are guaranteed to $\pm$1/4 step in chord 0, the chord nearest to the origin. This specification aids in determining the total system performance in terms of tracking even at the lowest input levels. Considering production restrictions, this also provides a reasonable method for incoming testing of codec components, guarantees meeting component specifications, and still assures adequate system performance.

In a sampled data system, the normal design architecture is to provide an output hold circuit; this generates the common 'stair-step' type output signal. The 'stair-step' signal is then low-pass filtered and compensated for the sampling characteristics (sinx/x response characteristics) to provide the analog waveform. Since the multiple-channel decoder encompasses an output multiplexer to separate the analog channels, this component is also used to provide a simple yet adequate output hold device. By adding capacitance on the output port, the switch not only selects the appropriate output channel but also holds the analog value during the off time of the cycle. However, while testing different configurations, this design approach led to a realization for multiplexer improvement. While a normal analog multiplexer is sufficient when the outputs allow charge to be dissipated, the situation in a PCM decoder is one where the output is a high-impedance filter. When an analog multiplexer switches from a selected switch to the open state, the switch design normally generates a finite amount of charge that is coupled to the now-open switch output. Since the switch is open, and the output load is fairly high impedance (>100k in most cases), any charge introduced onto the capacitor is not dissipated but is evident as a voltage level.

This phenomena can be measured as an increase in idle channel noise for the output channels. In terms of physically observing the charge distribution, the "idle" channels with 0 input levels show a square wave output. The waveform oscillates from 0 volts (when the channel is selected) to a voltage dependent upon the charge and the hold capacitor on the output. The waveform at essentially 8kHz can affect the noise level of the supposedly quiet channel even within the audio frequency range.

One approach to reducing the output noise level is to increase the output hold capacitor value. By using a larger capacitor, the charge introduces a smaller voltage on the output, and the measured idle channel noise is decreased. This change, however, introduces another problem in that the larger the output capacitor, the longer it takes to generate the output waveform for each sample. Since the sample time is fixed (3.9 or 5.2μsec), this results in fewer channels per digital-to-analog conversion circuit. After investigating the charge induced effect, it was decided that a modification in the multiplexer design itself could also aid in reducing the

charge amount. The measurements showning the improvements in system response are given in Tables 1 and 2.

TABLE 1: Idle channel noise for the MUX-88 and the DMX-88.

	CHANNEL MEASURED	IDLE CHANNEL NOISE	HOLD CAP
MUX-88	1	-60.8	10000pf
	2	-61.1	10000pf
	3	-60.3	10000pf
	4	-61.1	10000pf
	5	-60.9	10000pf
	6	-61.3	10000pf
	7	-61.2	10000pf
	8	-60.0	10000pf
DMX-88	1	All Values <-70dB	10000pf
	2		10000pf
	3		10000pf
	4		10000pf
	5		10000pf
	6		10000pf
	7		10000pf
	8		10000pf

TABLE 2: Idle channel noise with reduced hold capacitance.

	CHANNEL MEASURED	IDLE CHANNEL NOISE	HOLD CAP
MUX-88	1	-57.2	1000pf
	2	-57.2	1000pf
	3	-57.2	1000pf
	4	-57.2	1000pf
	5	-57.2	1000pf
	6	-57.2	4300pf
	7	-57.2	4300pf
	8	-57.2	4300pf
DMX-88	1	-68.6	1000pf
	2	-68.6	1000pf
	3	-68.6	1000pf
	4	-68.6	1000pf
	5	-68.6	1000pf
	6	<-70	4300pf
	7	<-70	4300pf
	8	-69.9	4300pf

With a reduction in the charge value, the output voltage level is decreased without an increase of capacitor values. Therefore, the system is able to manage the data rates required. The redesigned device, designated the DMX-88, has achieved a reduction in the output charge injection of 1/4 to 1/5 the value measured in the earlier analog multiplexers. This is seen as an immediate reduction in the output voltage level for common capacitor values. And, more importantly, it enables the user to reduce the hold capacitor, still achieve the system required idle channel noise levels, and decode at a higher output rate.

Concerning crosstalk in the decoder, the most important consideration would seem to be controlling the output switch to assure sufficient open time between channels. In this design, the enable function of the analog de-multiplexer is used to disable the output switches prior to incrementing the address. The DAC, in conjunction with the op-amp, is fast enough in some transitions to reach the following channel output level prior to the previous switch being opened. By disabling all switches, changing the digital input mode and the address selector, and then enabling the switches, no inter-channel problems are displayed due to the output de-multiplexer. This slightly reduces the "on" time for each output channel, however, the DAC and op-amp are still more than fast enough to handle the required data rates.

TESTING

Final testing procedure is accomplished by comparing the performance of the shared-channel codec to the system requirements as put forward by Bell System and CCITT. The most common tests for digitizing systems are often a series of analog-to-analog measurements normally reserved for installed transmission or switching systems. The first such test is the signal-to-total distortion measurement, done by adding a set frequency tone (1020 or 1004Hz) to one channel and measuring the output of that channel after removing the tone by filtering.

It is in this test (Figure 6) that the response of the companding conversion laws versus the linear-transfer laws becomes obvious. The companding laws are designed to provide a flatter signal-to-noise ratio at the higher input levels, while approximating a higher order linear response curve at the lower input values. There are presently two methods of generating input signals that are used, dependent upon whose specifications are being met. The Bell System approach is to provide a straight sinusoidal input waveform at the prescribed frequency. The CCITT recommendations, however, also allow for a psuedo-random noise source to be used as the input signal.

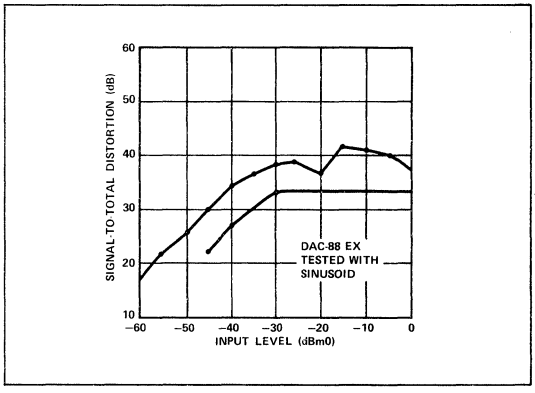


Figure 6: Signal-to-total distortion for the DAC-88EX.

Arguments are heard for both approaches; our measurements have been completed using both methods dependent upon which DAC (A-law or μ-law) is being evaluated. An interesting comparison can be made between the response of the present companding D/A converter (DAC-88/89) and

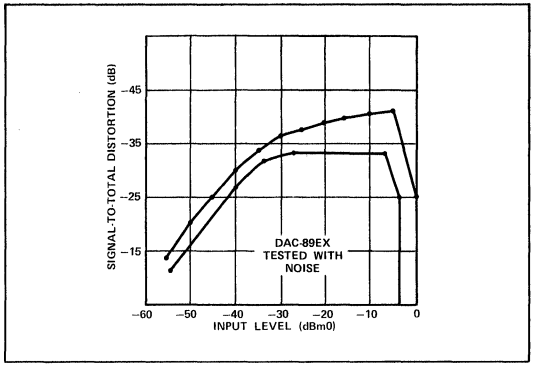


Figure 6A: Signal-to-total distortion for the DAC-89EX.

the original designs (DAC-86/87) by measuring the systems using constant bit clocking. As was mentioned earlier, the original designs of the converters required a slightly modified clocking scheme to achieve the required system performance. By running each device set at the higher frequency clock for the successive approximation sequence, the effect of the slower settling times and slightly worse chord 0 accuracy can be seen in terms of the system parameters. In Figure 7 it can be seen that the signal-to-distortion curves fall off more rapidly for the older devices at lower input levels.

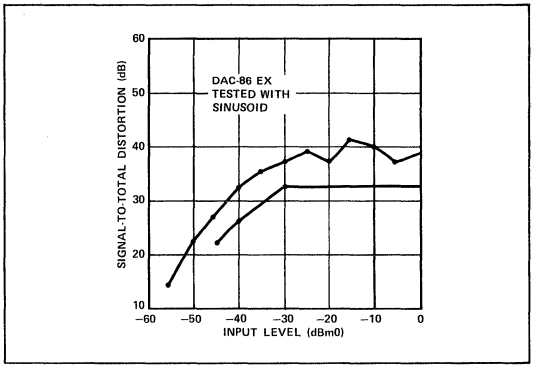


Figure 7: Signal-to-total distortion for the DAC-86EX.

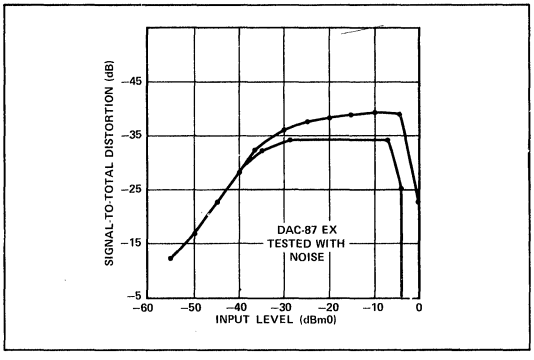


Figure 7A: Signal-to-total distortion for the DAC-87EX.

The next test results normally shown for "codec" performance are the gain linearity or tracking. As the input signal is reduced in magnitude, the output signal is measured to determine its loss in comparison. Again the CCITT and the Bell System standards differ in the type of input signal being used and the specifications for the measured output. The results in Figure 8 with the 8-channel system show compliance at all input levels. By comparing the older DAC design to the new version, another effect of the improved accuracy and settling time becomes evident. Expecially at the low input levels (–55 to –60dBm0), an obvious improvement is seen at the higher bit rate with the new DAC-89.

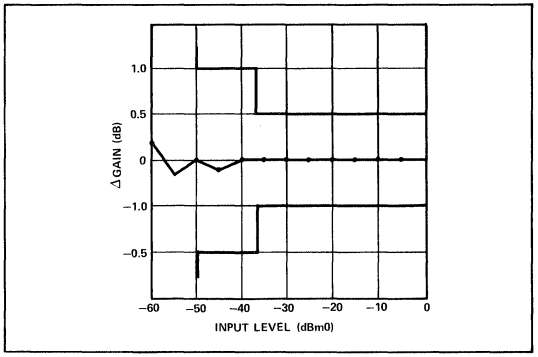


Figure 8: Gain tracking for the DAC-88EX.

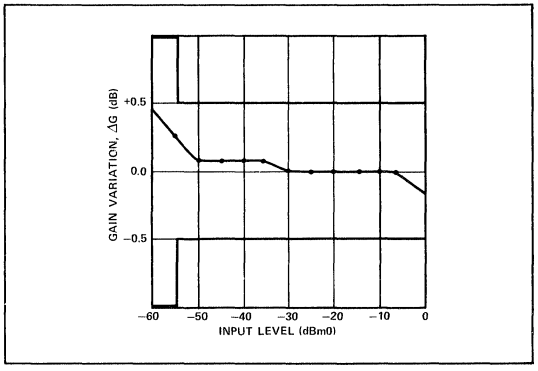


Figure 8A: Gain tracking for the DAC-89EX.

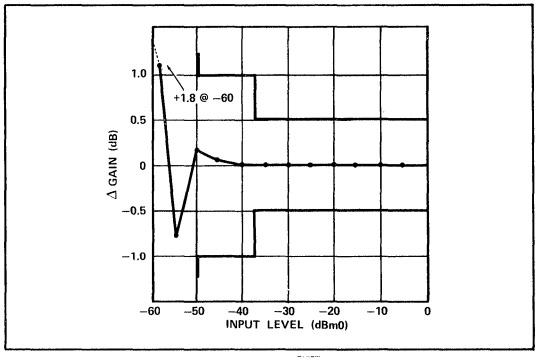


Figure 8B: Gain tracking for the DAC-86EX.

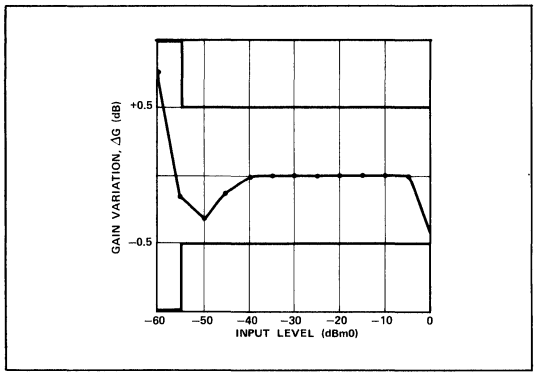


Figure 8C: Gain tracking for the DAC-87EX.

ADVANTAGES OF INDIVIDUAL COMPONENTS

It is important to note that a significant advantage in designing with the individual components is the flexibility it provides. By flexibility, it is meant that, if necessary, each system response characteristic can usually be traced back to the component (or components) affecting the measurement. This allows the designer the freedom of 'fine-tuning' the individual sections to achieve the overall system performance desired. For example, in terms of what was described as the hold settling time of the sample-and-hold circuit, since the timing of the overall design could be altered, the sample-and-hold clocking could be modified to reduce this characteristic. This provided improved system performance with only a minor adjustment in the total system design. Other examples of individual devices being adjusted for optimum performance include the re-design of the companding D/A converter and the de-multiplexer. In each case, it was a result of being able to control the separate design components that allowed either an improved device or an improvement in the system 'interface' to that device.

Another advantage to the use of individual components is the testing capability. With separate monolithic 'building blocks,' each device can be specified in the characteristics necessary for its proper functioning. By carefully selecting these requirements, the overall system response can also be predicted and guaranteed. PMI has held, and is still involved in, discussions with several of our customers to define those requirements per device to add confidence in the overall circuit designs. The customers can then set up an incoming device test apparatus to measure the significant specifications. All devices can realistically be tested in this manner, more so than expecting to measure system parameters in a large-scale production arrangement. So if the incoming inspection requirements become important to a production system, it could be useful to consider the advantages in testing individual device 'dc' parameters versus the system response.

The final advantage to be discussed is the cost per channel of the shared-channel design. It should be noted that shared-channel designs have been used in the past mainly because of cost savings over a per-channel arrangement. Even today as monolithic single-channel components become available, there is still a significant cost savings in the monolithic, shared-channel system. On a channel cost for 100 quantity pricing, the present costs show the figure to be under $5.00 per line (Table 3). In larger quantities, the savings obviously are even more. These figures are based on encoding eight channels with each decoding system. Also included in the data are figures showing the total 'chip' area and package sizes required. Reliability of components is based on size of die (silicon) circuitry in combination with the processing methods used. Bipolar is known as a high reliability process.

Table 3: Cost of devices used in codec systems.

Device	Cost at 100 pcs	Quantity Required	Total Cost	Chip Area (mil²)	Package Size	Total Chip Area	Total Pins
DAC88/89 COMDAC® Converter	$9.00	4	**$ 36.00**	9,996	18 DIP	39,984	72
SMP81 S/H Amplifier	9.50	3	**28.50**	6,966	14 DIP	20,898	42
CMP01 Comparator	4.50	3	**13.50**	2,730	8 TO 99	8,190	24
25L02 S.A.R.	3.30	3	**9.90**	9,135	16 DIP	27,405	48
OP16 Op Amp	4.50	1	**4.50**	2,880	8 TO 99	2,880	8
REF02 5 Volt Reference	5.00	1	**5.00**	2,520	8 TO 99	2,520	8
24-LINE TOTAL EXCLUDING MULTIPLEXERS		15	**$ 97.40**				
AVERAGE/LINE EXCLUDING MULTIPLEXERS		0.63/line	**4.05/Line**				
MUX88 8-Channel MUX	7.50	3	**22.50**	4,838	16 DIP	14,514	48
DMX88 8-Channel De-MUX	7.85	3	**23.55**	4,838	16 DIP	14,514	48
24-LINE TOTAL INCLUDING MULTIPLEXERS		21	**$143.45**			130,905	298
AVERAGE PER LINE						5,454	12.4
AVERAGE/LINE INCLUDING MULTIPLEXERS		0.88/line	**5.97**				

The pins per channel average gives a relative comparison of circuit board area required to produce the total system layout.

Realistically, there are certain designs that are easier to complete with the use of single-channel "codecs". It is not intended that all encoding or decoding designs must choose between per-channel or multiple-channel. The point that we hope is clear, is that in certain designs, a multiple-channel approach offers advantages in terms of costs, board area, testing and performance. These advantages make the designers work easier and more efficient. By making use of both multiple channel and single-channel designs where applicable, the transformation to digital transmission and switching becomes more cost effective and less difficult to implement.

A statement made earlier was that the companding DAC was originally envisioned as unique for telecommunications. However, several higher frequency systems, not specifically concerned with PCM transmission, have recently considered making use of companding D/A converters as well. These are mentioned to provide a look into possible future uses for faster conversion systems that still wish to conserve bandwidth. The immediate examples being discussed are music or program channels and transmitted TV audio signals. In both instances, more designs are turning to digitizing the analog signals prior to transmission for a variety of rea-

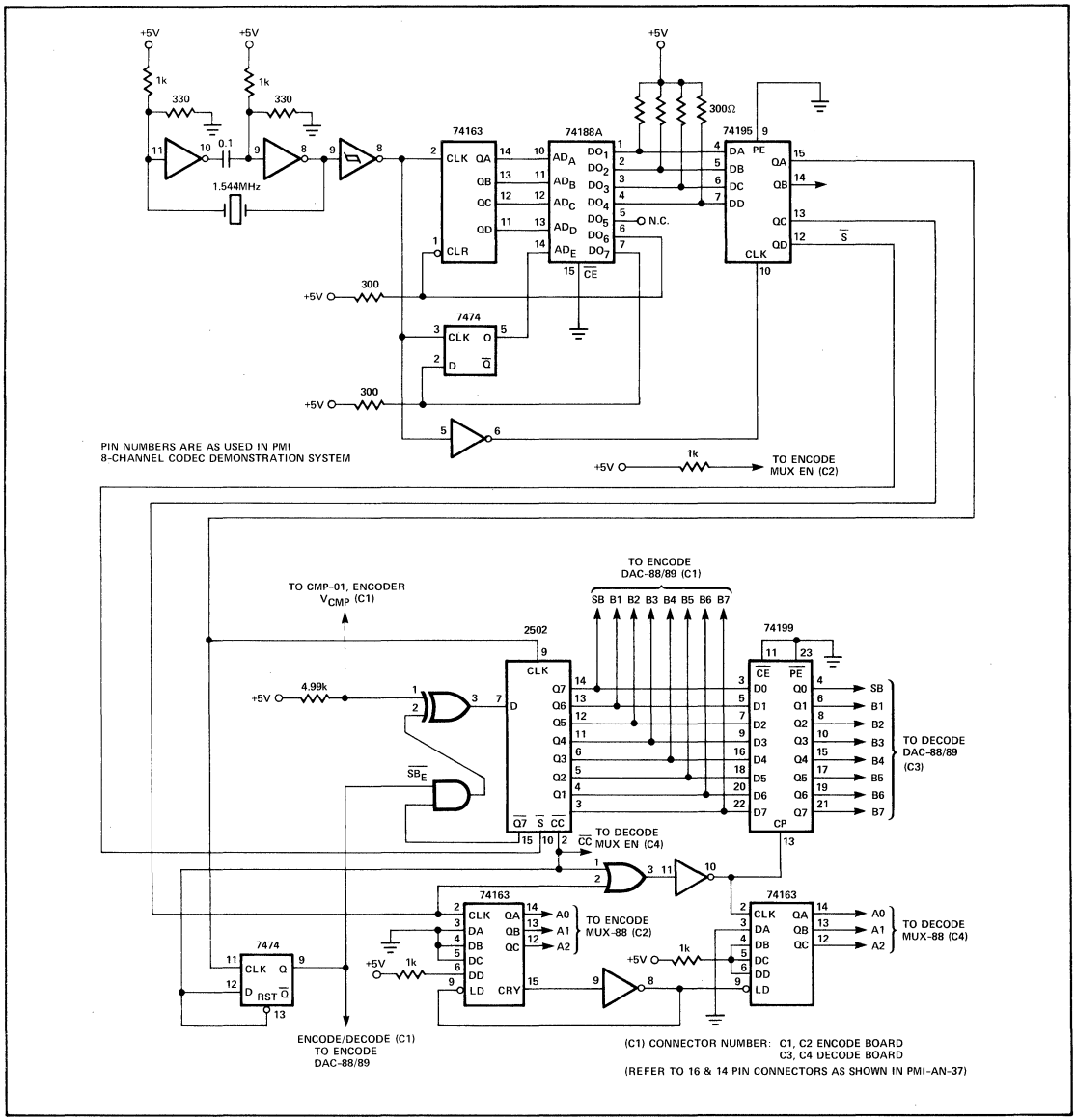


Figure 9 : Eight-channel demonstration system control/clock circuit.

sons. However, in this case, the audio response needs to include signals up to 15kHz, therefore requiring in most designs, 30kHz sampling. The advantages to companding converters are the same; minimum bandwidth with constant signal to distortion ratios while providing dynamic range equivalent to higher bit-rates. The problem has been operating most companding converters at 30kHz or greater. With the individual monolithic approach, this is no problem whatsoever, the 8-channel unit (see Figure 9 for control/clock circuit configuration) described is already converting at a 64kbps rate. The speed of the bipolar design provides ample conversion time for encoding and decoding these higher data rate samples.

The 30kHz sampling system is easily configured and the results, so far, have proven very acceptable. The companding approach has moved into areas where higher frequency response (i.e. higher sampling rates) are needed. The companding laws can therefore prove useful for many audio applications, not only PCM switching and carrier systems.

The monolithic shared-channel codec can produce a design alternative that provides economic and reliability advantages in a system design. The components needed are readily available today and are presently being used by several manufacturers.

In the future, shared-channel designs will continue to provide advantages. The expertise now exists to include all circuitry used in encoding "several" channels (8, for example) within a single monolithic device. The same is true for the decoding circuitry. This higher level of integration can provide continued cost savings on a per-channel basis while simplifying system design and layout. Both single-channel and shared-channel components will improve. Engineers designing digital transmission and switching systems must consider many factors in chosing a system configuration, the result hopefully being the most economical and efficient design possible.

APPLICATION NOTE 50

A VARIABLE-FREQUENCY, CLOCK RECOVERY CIRCUIT USING THE RPT-81 OR RPT-82

by B.W. Berry

This note describes a high-performance clock-recovery circuit, employing an RPT-81 repeater IC and a CMP-01 IC comparator, which helps derive a clock pulse from, and synchronizes it with, an incoming data signal. The circuit accepts a low-level bipolar pulse train (35mV peak-to-peak, minimum) while producing a usable recovered clock signal. Since the circuit also accepts high-level inputs (10V peak-to-peak, minimum), it can attain a 49-dB dynamic range.

The RPT-81 chip is conventionally connected, except that input and output transformers are not required and the (internal) output transistors are left as an open circuit (Figure 1). The recovered clock signal is picked off the RPT-81's clock amplifier (pins 11 and 12) by the CMP-01 comparator.

The comparator's output is basically a square wave at the data rate frequency (which, for this example, is the T1 transmission frequency of 1.544 Mbits/s).

Clock recovery can be best understood by referring to a more detailed diagram of the RPT-81's oscillator section and external tuned circuit (Figure 2). Grounding pin 13 creates a "locked oscillator" operating mode. Floating pin 13 creates a "pulsed tank" operating mode.

In the pulsed-tank mode, the external tuned circuit is stimulated each time the full-wave rectifier demands a current pulse. Between pulses, the tank circuit "rings" at its resonant frequency, damped only by R8 and the on-chip transistor collector resistor R.

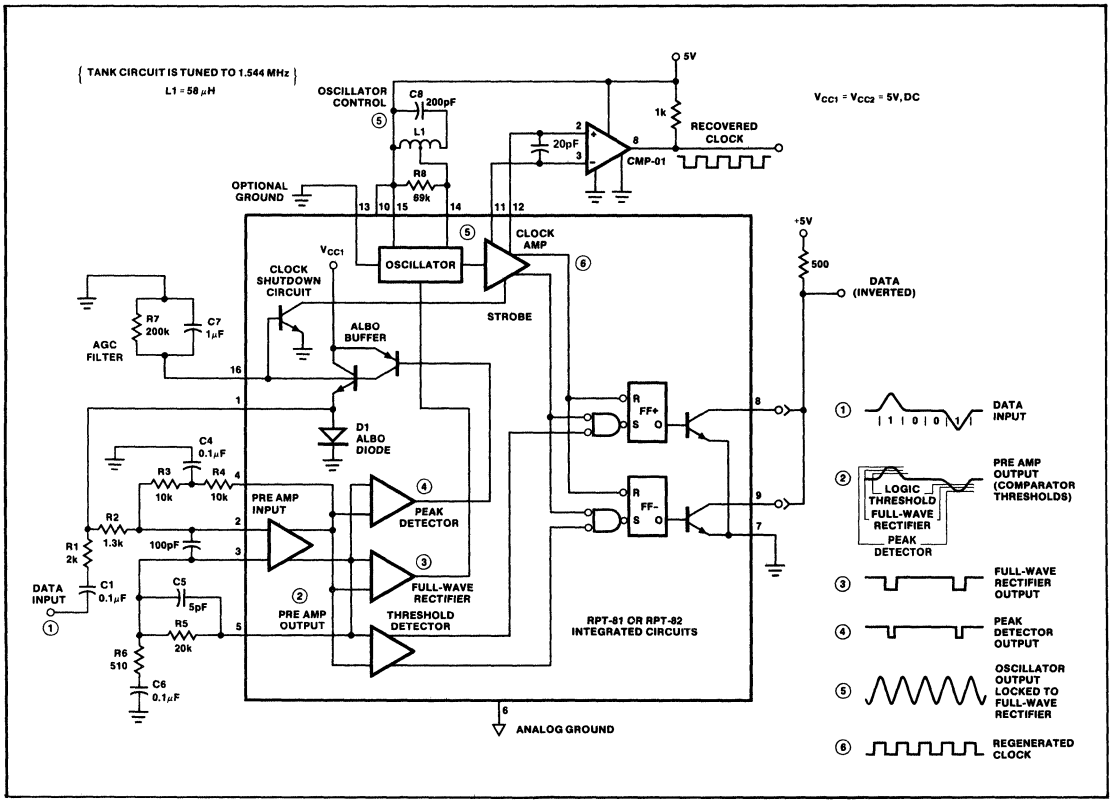


Figure 1: The clock-recovery circuit shown above will accept a 35mV peak-to-peak (minimum) bipolar pulse train and produce recovered clock pulses at the data rate frequency (1.544Mbits/s for this example). Key waveforms, shown in correct timing relationship, illustrate the circuit's operation. Comparator CMP-01 provides amplification and offset for a good TTL interface.

In the locked-oscillator mode, the oscillator runs continuously. It is injection-locked to the full-wave rectifier pulses by the second emitter of on-chip transistor Q. The oscillator circuit drives a buffer emitter follower, which in turn drives a clock amplifier. The clock amplifier has a differential output (pins 11 and 12) and squares the sinusoidal oscillations originating at pin 14.

Since the clock amplitude at pins 11 and 12 is only 1Vp-p around a common-mode dc level of 4.5V, the CMP-01 comparator provides a good interface to TTL or other logic. A small capacitor, C_4, may be connected across pins 11 and 12 to delay the clock relative to the data.

The circuit shown in Figure 1 does not make use of the data outputs of the repeater IC. However, if a data waveform is required in addition to the clocking pattern, the change in circuit configuration required is minor. By tieing the output leads of the two flip-flops together (pins 8 and 9) and adding a 500ohm pull-up resistor to +5V, an inverted data waveform is made available.

How "pulsed-tank" and "locked-oscillator" modes are selected is shown in Figure 2. Pickoff points for a regenerated clock signal (within the clock amplifier) are also evident in the diagram.

The circuit described in this note was designed and tested only with alternate-mark-inversion (AMI) codes. However, the system should work equally well with any return-to-zero code and would suit any of the many AMI-code variants. It can handle data rates up to 2.0 Mbits/s and uses only a single 5V supply.

Designs have been tested at frequencies from 64kHz up to 1.544MHz by simply modifying the tank circuit. In all cases, performance met desired expectations.

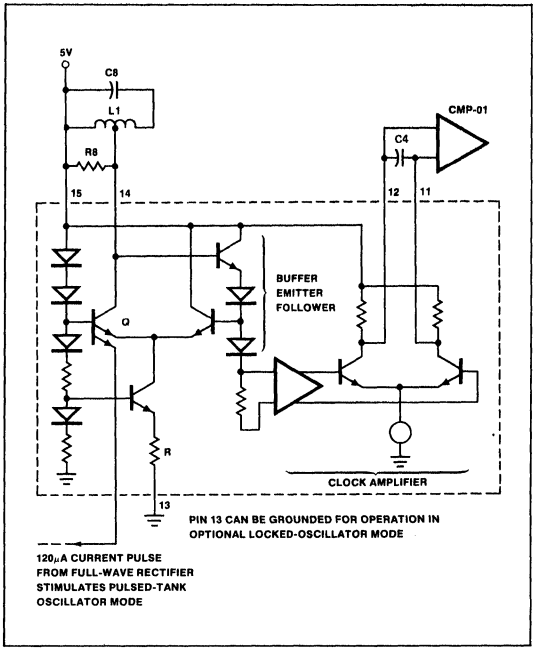


Figure 2: Detailed view of the RPT-81's oscillator and clock amplifier shows how "pulsed-tank" and "locked-oscillator" modes are selected. Pickoff points for a regenerated clock signal (within the clock amplifier) are also evident.

APPLICATION NOTE 53

SAMPLE/HOLD CIRCUIT MONITORS TWO INPUT SIGNALS AND TRACKS THE SMALLER OR LARGER SIGNAL

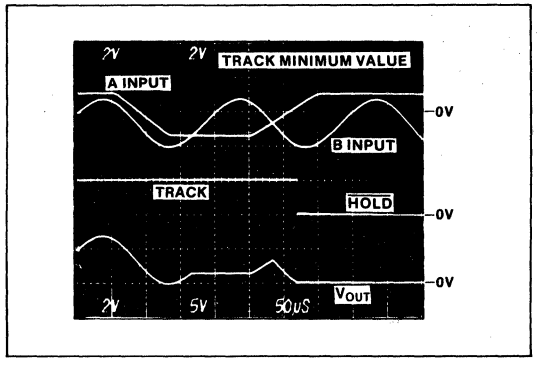
By Gary J. Grandbois
David Gillooly

INTRODUCTION

In control applications involving two sensors it may be necessary to select the smaller or larger of the two sensor signals for control purposes. Possible applications include electronic automobile antiskid control, depth measurement and temperature monitoring. Automatic selection of the signal of interest eliminates the wasteful and expensive hardware and software duplication needed to monitor, digitize and evaluate the two signals.

The circuit described provides a two channel sample and hold amplifier that automatically tracks the larger or smaller (user programmed) of two input signals. It is implemented with only one integrated circuit which can replace up to three IC packages that would be necessary (dual switch, comparator, quad op amp) in other implementations. This IC, the GAP-01, contains a comparator and two transconductance input amplifiers (A & B), whose outputs are switched by internal current mode switches into the voltage follower output buffer(C). Two digitally selectable signal paths through the device are possible via the Channel A, Channel B control signals.

Circuit operation is straight forward. In Figure 1, the signal paths through Channel A and Channel B are configured for gains of +1. The comparator monitors the input signals relative magnitudes. With the MIN/MAX control in the "Minimum Track" position (MAXIMUM/$\overline{\text{MINIMUM}}$ = "0"), and the system in "TRACK" (TRACK/$\overline{\text{HOLD}}$ = "1"). The minimum or smaller of the two input signals, A or B, is present at the GAP-01 output (Photograph 1). A "1" comparator output indicates input B is less than input A.



Photograph 1. Minimum Value Track/Hold.

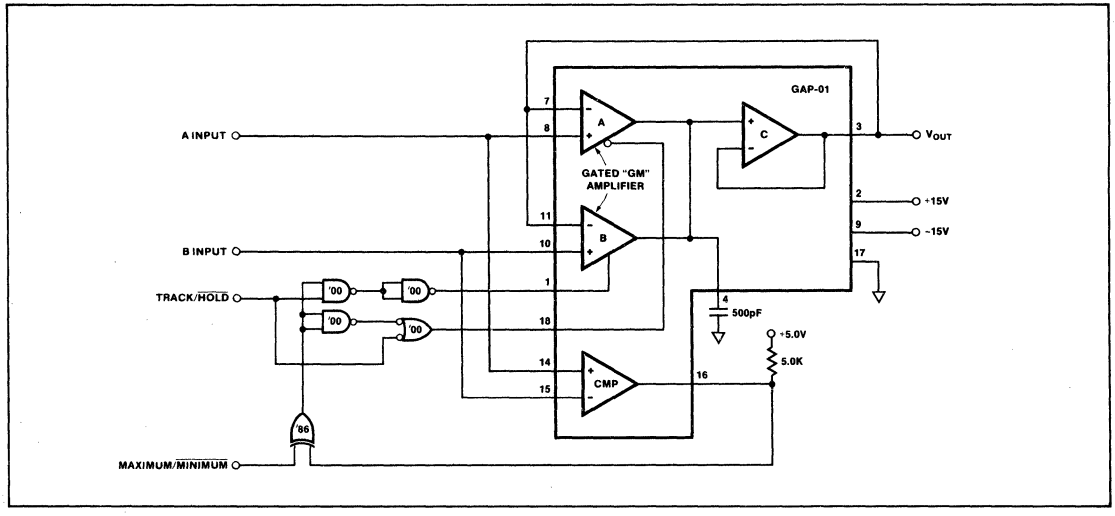
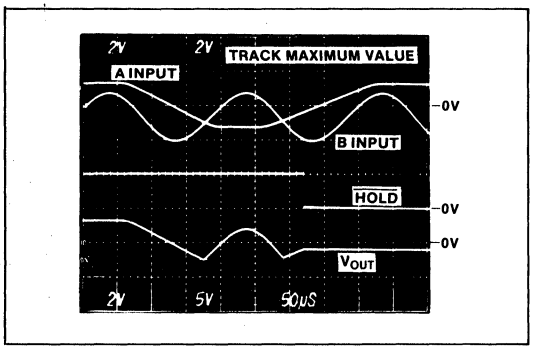


Figure 1. Minimum/Maximum Value Track/Hold.

By setting MAXIMUM/$\overline{\text{MINIMUM}}$ to "1" the larger of the two input signals is tracked (Photograph 2). The exclusive "OR" gate simply inverts the comparator output.



Photograph 2. Maximum Value Track/Hold.

Gains other than +1 are achievable by changing the GAP-01 feedback ratio as shown in Figure 2.

By setting the TRACK/$\overline{\text{HOLD}}$ control to "0" both the A and B amplifier outputs are disconnected from the output buffer amplifier input, thus putting the system into "hold and maintaining the last output stored on the external capacitor C_H. This capacitor serves both as a loop compensation and hold or storage capacitor. (Photographs 1 and 2) Droop rates of 0.2mV/msec are typical.

This powerful minimum/maximum track and hold system is easily constructed from a new general purpose integrated circuit.

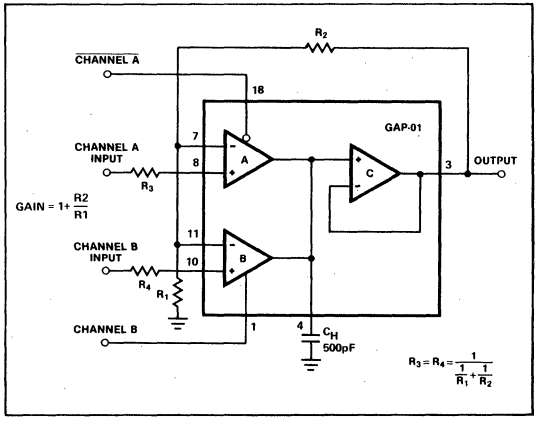


Figure 2. Alternate Gain Configuration.

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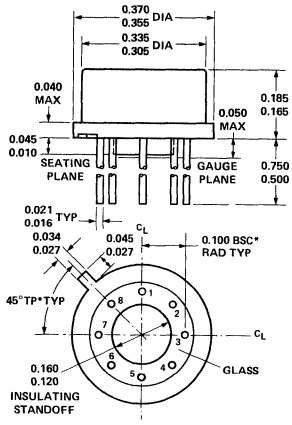
AVAILABLE PACKAGES

PACKAGE	DESCRIPTION
H	6-Pin TO-78
J	8-Pin TO-99
K	10-Pin TO-100
L	10-Pin Hermetic Flatpack
M	14-Pin Hermetic Flatpack
N	24-Pin Hermetic Flatpack
Y	14-Pin Hermetic DIP
Q	16-Pin Hermitic DIP
R	20-Pin Hermetic DIP
T	28-Pin Hermetic DIP
X	18-Pin Hermetic DIP
V	24-Pin Hermetic DIP
P	Epoxy B DIP (P is used for any plastic pkg.)
Z	8-Pin Hermetic DIP

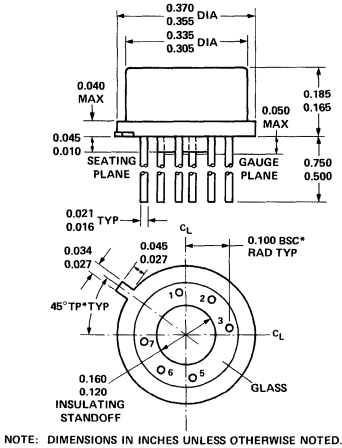
MECHANICAL DIMENSIONS — CANS

TO-99 (J)



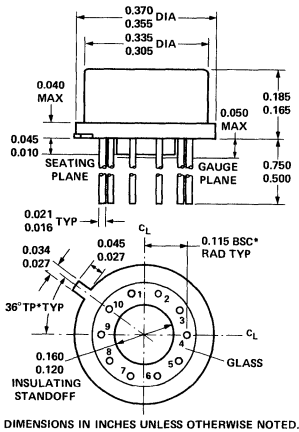
NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE.

TO-78 (H)



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE.

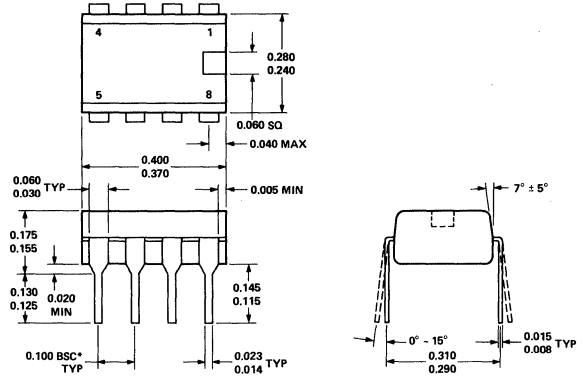
TO-100 (K)



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE.

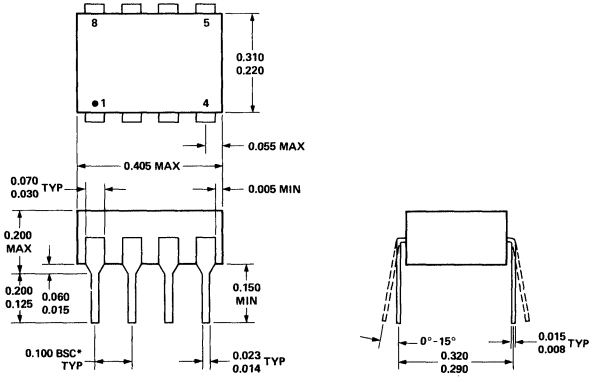
MECHANICAL DIMENSIONS — DIP'S

8-PIN EPOXY B MINI DIP



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE.

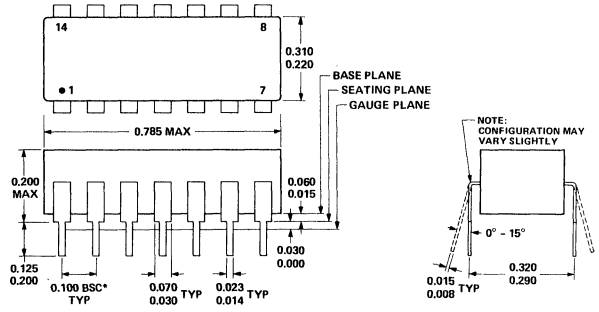
8-PIN HERMETIC DIP (Z)



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

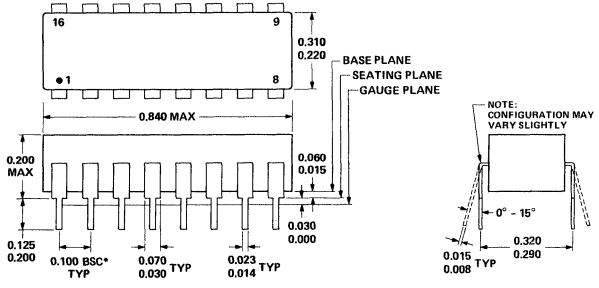
MECHANICAL DIMENSIONS — DIP'S

14-PIN HERMETIC DUAL-IN-LINE (Y)



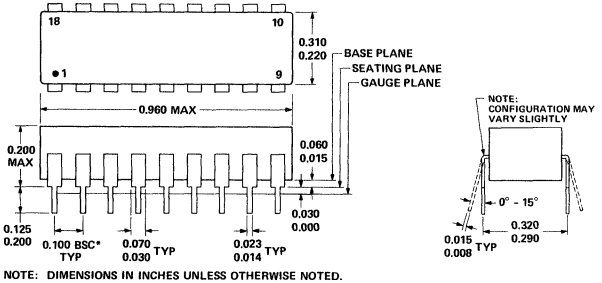
NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE.

16-PIN HERMETIC DUAL-IN-LINE (Q)



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE.

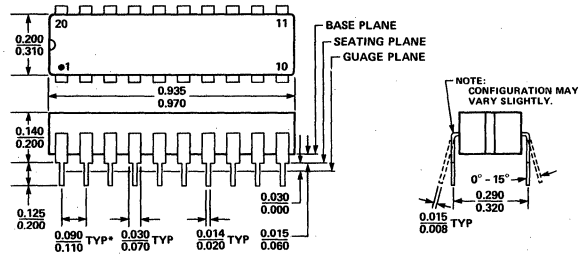
18-PIN HERMETIC DUAL-IN-LINE (X)



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE.

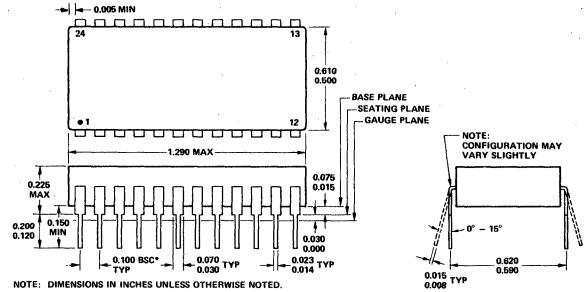
MECHANICAL DIMENSIONS — DIP'S

20-PIN HERMETIC DUAL-IN-LINE (R)



NOTE:
DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) GUAGE PLANE.

24-PIN HERMETIC DUAL-IN-LINE (V)



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
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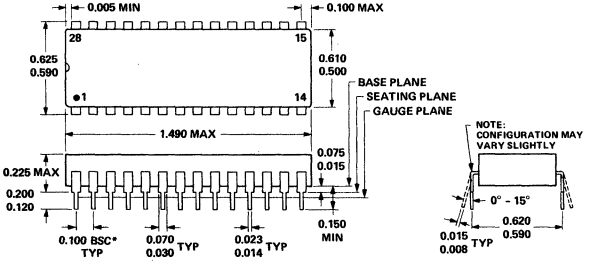
28-PIN HERMETIC DUAL-IN-LINE (T)



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
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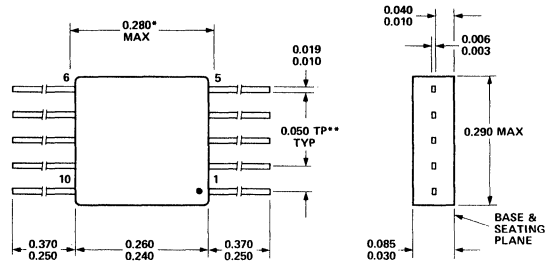
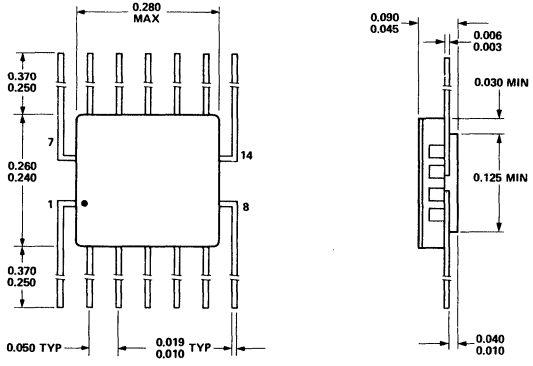
MECHANICAL DIMENSIONS — FLATPACKS

10-PIN HERMETIC FLATPACK (L)



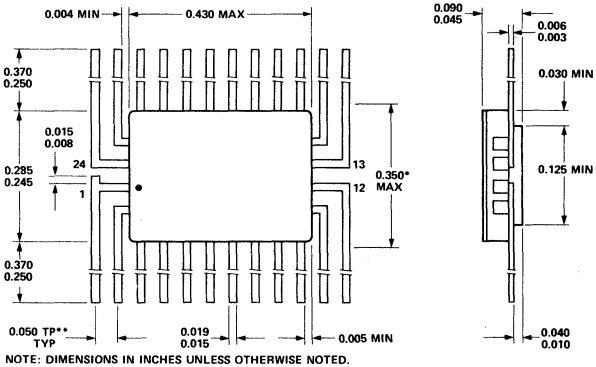
NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEAD AND BODY IRREGULARITIES PERMITTED IN THIS ZONE.
**LEADS WITHIN 0.005 RADIUS OF TRUE POSITION.

14-PIN HERMETIC FLATPACK (M)



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.

24-PIN HERMETIC FLATPACK (N)



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEAD AND BODY IRREGULARITIES PERMITTED IN THIS ZONE.
**LEADS WITHIN 0.005 RADIUS OF TRUE POSITION

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