Streams Processor U
Unified Memory S
Processor UMA U
Memory Streams P
r UMA Unified M
Streams Processor U
Unified Memory S
Processor UMA U
Memory Streams P
r UMA Unified M
Streams Processor U

Trio64UV+

Trio

MULTIMEDIA ACCELERATION
Cooperative Accelerator Architecture

Trio64UV+ UMA Graphics/Video Accelerator

March 1996

S3 Incorporated
2770 San Tomas Expressway
P.O. Box 58058
Santa Clara, CA 95052-8058

NOTATIONAL CONVENTIONS

The following notational conventions are used in this data book:

Signal names are shown in all uppercase letters. For example, XD.

A bar over a signal name indicates an active low signal. For example, $\overline{OE}$.

n-m indicates a bit field from bit n to bit m. For example, 7-0 specifies bits 7 through 0, inclusive.

n:m indicates a signal (pin) range from n to m. For example D[7:0] specifies data lines 7 through 0, inclusive

Use of a trailing letter H indicates a hexadecimal number. For example, 7AH is a hexadecimal number.

Use of a trailing letter b indicates a binary number. For example, 010b is a binary number.

When numerical modifiers such as K or M are used, they refer to binary rather than decimal form. Thus, for example, 1 KByte would be equivalent to 1024, not 1,000 bytes.

NOTICES

Additional information may be obtained from:

S3 Incorporated, Literature Department P.O. Box 58058, Santa Clara, CA 95052-8058.

Telephone: 408-980-5400, Fax: 408-980-5444

Table of Contents

List of Figures

List of Tables

Section 1: Introduction

High-Performance Integrated Graphics/Video Accelerator

- High-performance 64-bit graphics engine
- Integrated 24-bit RAMDAC with 135 MHz output pixel rate and programmable dual-clock synthesizer
- Unique S3 Streams Processor for hardware-assisted video playback
- S3 Scenic Highway for direct interface to live video and MPEG-1 peripherals

S3 Streams Processor Features

- Supports on-the-fly stretching and blending of primary RGB stream and RGB or YUV/YCbCr (video) secondary stream
- Each stream can have different color depths
- YUV data is color space converted on the fly

Advanced Playback Capabilities

- High-quality hardware-assisted video playback (up to 1024x768x8 bits/pixel)
- Support for Indeo, Cinepak, and software-accelerated MPEG-1 video playback

Game and Presentation Effects

- Hardware double-buffering support for high-quality tear-free playback
- 2-D scrolling and sprite plane support
- Color and chroma keying for overlaying of graphics onto video and video onto graphics
- Arithmetic blending of two pixel streams for fade-in/fade-out transition effects

Unified Memory Architecture (UMA)

- UMA shares system memory between the host CPU and the graphics/video subsystem
- System memory arbitration compatible with all major core logic vendors
- 64-bit DRAM memory interface
- 0.5-, 1-, 1.5 or 2-MByte configurable frame buffer
- Fast page and EDO mode memory support

Mixed Voltage Support

- 5V core, 5V or 3.3V memory bus operation
- Compatible with 5V or 3.3V memories
- Compatible with 5V or 3.3V UMA core logic

S3 Scenic Highway Interface

- Philips SAA7110/SAA7111 video digitizers
- S3 Scenic/MX2 MPEG-1 audio/video decoder

High Resolution Non-Interlaced Screen Support

- 1280x1024x256 colors
- 1024x768x256 colors
- 800x600x64K colors
- 640x480x16.7M colors

Glueless PCI 2.1 Bus Support

Multimedia Support Hooks

- 8-bit bidirectional feature connector
- S3 Scenic Highway
- I^2C bus

Full Software Support

- Drivers for Windows 3.11, Windows NT, Windows 95, OS/2 2.1 and 3.0 (Warp), SCO UNIX

Green PC/Monitor Plug and Play Support

- Full hardware and BIOS support for VESA Display Power Management Signaling (DPMS) monitor power savings modes
- Extensive static/dynamic power management
- DDC monitor communications support

Industry-Standard 208-pin PQFP package

1.1 OVERVIEW

The S3® Trio64UV+™ UMA graphics/video accelerator (hereinafter referred to as the Trio64UV+) is the newest member of the extremely successful Trio™ family of products. Based on the Trio64V+™ integrated graphics/video accelerator, Trio64UV+ adds Unified Memory Architecture (UMA) support allowing system memory to be shared between the host CPU and the graphics/video subsystem. UMA support provides a full-featured solution for motherboard designs that dramatically reduces the graphics subsystem cost and footprint. Trio64UV+ is targeted at entry-level Intel® Pentium™ systems and equivalents. It has been developed in conjunction with all major PC system core logic vendors and will be supported in many next generation Pentium/PCI core logic designs.

1.2 ADVANCED ARCHITECTURE/FEATURE SET

Trio64UV+ provides a 64-bit high performance graphics engine and a 64-bit DRAM interface. The full 64-bit memory data path is used in all frame buffer configurations, which range in size from 0.5 to 2 MBytes. Fast-page and EDO mode DRAMs are supported.

1.3 UNIFIED MEMORY ARCHITECTURE (UMA)

Trio64UV+ is the first product offered by S3 to support UMA operation. This architecture reserves a portion of main system memory as graphics memory, thus eliminating the need for a separate graphics frame buffer. This allows system manufacturers to dramatically reduce the graphics subsystem cost. Since the graphics memory is now an integral part of the host memory bus, CPU accesses to graphics memory are no longer constrained by PCI bandwidth limitations. This drastically reduces the software overhead of many common graphics operations.

1.4 STREAMS PROCESSOR SUPPORT

The S3 Streams Processor™ technology processes data from the graphics frame buffer, composes it and outputs the result to the internal DACs for generation of the analog RGB outputs to the monitor. Data is composed from up to 3 independent streams: (1) Primary Stream—RGB graphics data; (2) Secondary Stream—RGB or YUV/YCbCr (video) data from another region within the frame buffer; and (3) a 64x64x2 hardware cursor.

Arithmetic blending of a primary graphics stream and secondary graphics/video enables dramatic transition effects for game and multimedia applications. Color and chroma keying allow opaque or transparent overlays of one stream on the other.

Simultaneous display of graphics and video of different color depths is provided. For example, it is possible to display true color (24-bit) video data on top of an 8-bit graphics background. This can improve video quality and frame rates while reducing memory bandwidth and storage requirements.

1.5 MULTIMEDIA SUPPORT FEATURES

Trio64UV+ supports the S3 Scenic Highway™ local peripheral bus for direct connection to video input devices like the S3 Scenic/MX2™ Audio/Video MPEG decoder and the Philips® video digitizers. The Streams Processor and Scenic Highway are tightly coupled to provide optimal live video playback. The hardware automatically switches capture and display buffers without software intervention.

1.6 FEATURES ADDED TO Trio64V+

- Arbitration logic for UMA memory
- Support for system memory DRAMs [FP and EDO SIMMs]
- Support for 0.5- and 1.5-MByte frame buffers
- Optional disabling of DRAM refresh (core logic refreshes DRAM instead)
- Mixed voltage operation

1.7 FEATURES REMOVED FROM Trio64V+

- VL-Bus™ support
- Trio64™ -compatible mode
- Trio64-type VAFC feature connector support (multiplexed on PD lines)
- 16-bit VAFC feature connector on the LPB
- Video 8 In/Out LPB mode
- Video 16 LPB mode
- CL-480 support
- 4-MByte memory support
- 1-cycle EDO operation
- Relocation of Serial Port register to I/O port via power-on strapping

1.8 INTRODUCTION TO THIS DATA BOOKLET

This data booklet largely describes the areas in which Trio64UV+ differs from Trio64V+. It does contain complete pin descriptions and electrical and mechanical specification sections. Otherwise, the Trio64V+ data book must be used in conjunction with this data booklet.

Section 2: Pins

2.1 PINOUT DIAGRAMS

Trio64UV+ comes in a 208-pin PQFP package. The pinout is shown in Figure 2-1.

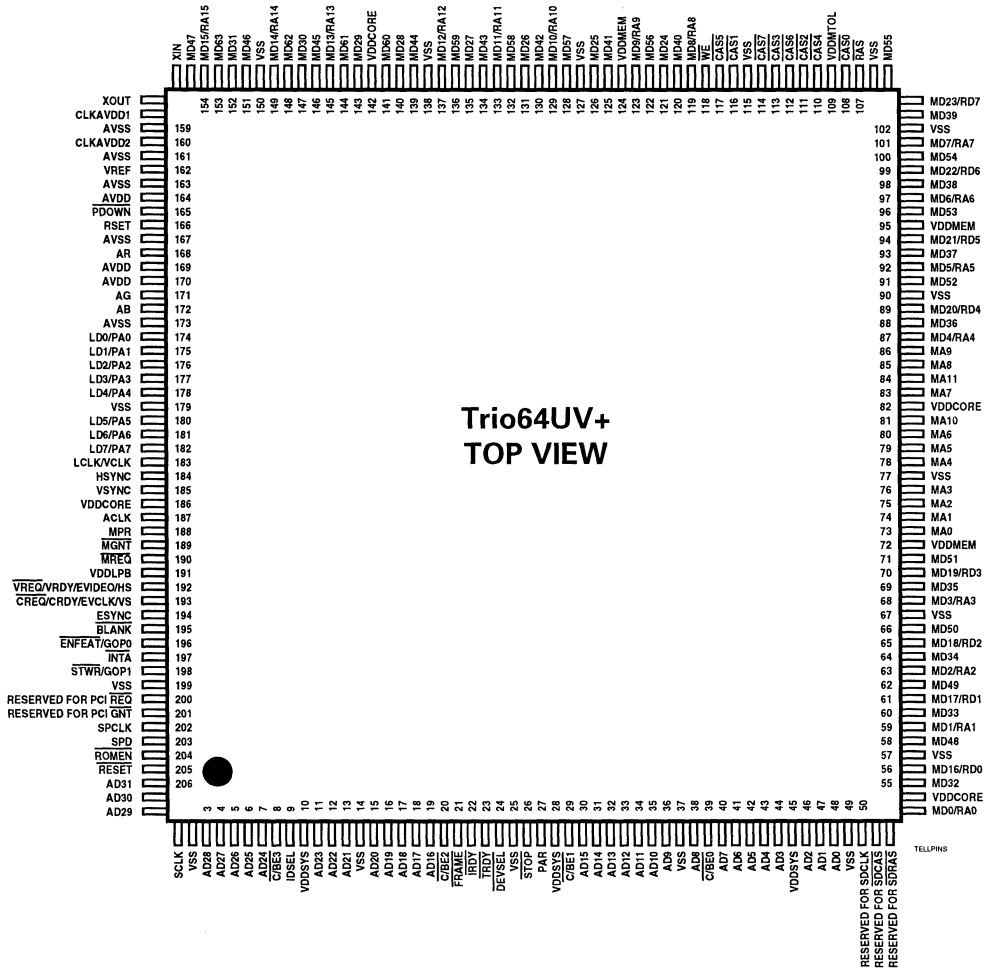


Figure 2-1. Pinout

2.2 PIN DESCRIPTIONS

The following table provides a brief description of each pin on Trio64UV+. The following abbreviations are used for pin types.

I - Input signal
O - Output signal
B - Bidirectional signal

Table 2-1. Pin Descriptions

Symbol	Type	Description
PCI BUS INTERFACE		
Address and Data		
AD[31:0]	B	Multiplexed Address/Data Bus. A bus transaction (cycle) consists of an address phase followed by one or more data phases.
$\overline{\text{C/BE[3:0]}}$	I	Bus Command/Data Byte Enables. These signals carry the bus command during the address phase and the byte enables during the data phase.
Bus Control		
SCLK	I	PCI System Clock.
$\overline{\text{INTA}}$	O	Interrupt Request.
$\overline{\text{IRDY}}$	I	Initiator Ready. A bus data phase is completed when both $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are asserted on the same cycle.
$\overline{\text{TRDY}}$	O	Target Ready. A bus data phase is completed when both $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are asserted on the same cycle.
$\overline{\text{DEVSEL}}$	O	Device Select. Trio64UV+ drives this signal active when it decodes its address as the target of the current access.
IDSEL	I	Initialization Device Select. This input is the chip select for PCI configuration register reads/writes.
$\overline{\text{RESET}}$	I	System Reset. Asserting this signal forces the registers and state machines to a known state.
$\overline{\text{FRAME}}$	I	Cycle Frame. This signal is asserted by the bus master to indicate the beginning of a bus transaction. It is deasserted during the final data phase of a bus transaction.
PAR	O	Parity. Trio64UV+ asserts this signal to verify even parity during reads.
$\overline{\text{STOP}}$	O	Stop. Trio64UV+ asserts this signal to indicate a target disconnect.

Table 2-1. Pin Descriptions (continued)

Symbol	Type	Description
CLOCK CONTROL		
XIN	I	Reference Frequency Input. If an external crystal is used, it is connected between XOUT and this pin. A stable external frequency source can also be input via this pin. If this is done, the input voltage must be the same as AVDD. If MD11 is strapped high at power-on, this becomes the DCLK (dot clock) input, bypassing the internal oscillator. This is normally only used for test purposes.
XOUT	O	Crystal Output. If an external 14.318 MHz crystal is used, it is connected between XIN and this pin. This pin drives the crystal via an internal oscillator.
DISPLAY MEMORY INTERFACE		
Address and Data		
MA[11:0]	O	Memory Address Bus. The memory row and column addresses are multiplexed on these lines.
MD[63:0]	B	Memory Data Bus Lines.
Memory Control		
$\overline{RAS}$	O	Row Address Strobe
$\overline{CAS}$[7:0]	O	Column Address Strobes.
$\overline{WE}$	O	Write Enable
Arbitration		
$\overline{MREQ}$	O	Memory Bus Request.
$\overline{MGNT}$	I	Memory Bus Grant.
MPR	O	Priority. Trio64UV+ asserts this signal to indicate a high priority bus request. This is not used with 2-pin arbitration schemes.
ACLK	I	Clock. This input is normally connected to the host CPU clock. It is used by Trio64UV+ to synchronize the memory bus arbitration with the host system. It may also be used as the system MCLK.
VIDEO INTERFACE		
$\overline{PDOWN}$	I	Power Down. Asserting this signal turns off the RGB analog output from the DACs.
VREF		Voltage Reference. This pin is tied to V_{SS} through a 0.1 µF capacitor.
RSET		Reference Resistor. This pin is tied to V_{SS} through an external resistor to control the full-scale current value.
AR	O	Analog Red. Analog red output to the monitor.
AG	O	Analog Green. Analog green output to the monitor.
AB	O	Analog Blue. Analog blue signal to the monitor.

Table 2-1. Pin Descriptions (continued)

Symbol	Type	Description
$\overline{\text{ENFEAT}}$	O	Enable Feature Connector. Setting SRD_0 to 1 drives this signal low when SR1C_1-0 are 00b. This also enables all feature connector operations.
$\overline{\text{BLANK}}$	B	Video Blank.
ESYNC	I	External SYNC. When ESYNC is driven low, HSYNC, VSYNC and $\overline{\text{BLANK}}$ become inputs. When ESYNC is high, HSYNC, VSYNC and $\overline{\text{BLANK}}$ become outputs.
EVIDEO	I	External Video. When this input is high, PA[7:0] are outputs to the feature connector.
EVCLK	I	External VCLK. When this input is asserted low, VCLK is an input to the internal RAMDAC. When this input is high, VCLK is output to the feature connector.
VCLK	B	Video/Pixel Clock. When EVCLK is high, this signal is an output to the feature connector. When EVCLK is low, this becomes an input used only for test purposes.
HSYNC	B	Horizontal Sync. When ESYNC is high, this is the horizontal sync output. When ESYNC is low, this is an input from the feature connector.
VSYNC	B	Vertical Sync. When ESYNC is high, this is the vertical sync output. When ESYNC is low, this is an input from the feature connector.
PA[7:0]	B	Pixel Address Lines [7:0]. The PA[7:0] function is enabled on the pins indicated for PCI configurations when LPB feature connector operation is enabled. When EVIDEO is high, PA signals are outputs to the feature connector.

Table 2-1. Pin Descriptions (Continued)

Symbol	Type	Description
MISCELLANEOUS FUNCTIONS		
General Data, I/O and Serial Ports		
RA[15:0]	O	ROM Address Bus. These signals provide the address for BIOS ROM reads. They are multiplexed with MD signals. Programmers must ensure that the memory bus is inactive when reading the ROM. This function is only used in test mode.
RD[7:0]	I	ROM Data Bus. These signals carry data for BIOS ROM reads. They are multiplexed with MD signals. Programmers must ensure that the memory bus is inactive when reading the ROM. This function is only used in test mode.
$\overline{\text{ROMEN}}$	O	ROM Enable. This signal provides the chip output enable input for BIOS ROM reads. This function is only used in test mode.
GOP[1:0]	O	General Output Port Bits 1-0. If SR1C_1 is set to 1, the value of CR5C_0 is output on pin 196 (GOP0) and the value of CR5C_1 is output on pin 198 (GOP1).
$\overline{\text{STWR}}$	O	Strobe Write. If SR1C_1 is cleared to 0, this signal is asserted whenever a write is made to CR5C. It is used to enable a General Output Port latch.
SPCLK	I/O	Serial Port Clock. This is the clock for serial data transfer, either for I^2C or DDC2 monitor data communications. As an output, it is programmed via MMFF20_0. As an input, its status is read via MMFF20_2. In either case the serial port must be enabled by setting MMFF20_4 to 1.
SPD	I/O	Serial Port Data. This is the data signal for serial data transfer, either for I^2C or DDC2 monitor data communications. As an output, it is programmed via MMFF20_1. As an input, its status is read via MMFF20_3. In either case the serial port must be enabled by setting MMFF20_4 to 1.
SCENIC HIGHWAY		
Scenic/MX2 Mode		
LD[7:0]	I/O	LPB Data. This is the Scenic Highway data bus and carries compressed data to Scenic/MX2 and video data from Scenic/MX2.
LCLK	I	LPB Clock. This clock controls transactions between Trio64UV+ and Scenic Highway peripherals
$\overline{\text{VREQ}}$/VRDY	O	Video Request/Ready. This signal is part of the the Scenic Highway data transfer protocol between Trio64UV+ and Scenic/MX2.
$\overline{\text{CREQ}}$/CRDY	I	Scenic/MX2 Request/Ready. This signal is part of the the Scenic Highway data transfer protocol between Trio64UV+ and Scenic/MX2.
$\overline{\text{ENFEAT}}$	O	Enable Feature Connector. This signal is connected to Scenic/MX2 chip enable input such that Scenic/MX2 is disabled when feature connector operation is enabled.
Video 8 Mode		
LD[7:0]	I	LPB Data Bus [7:0]. This is the Scenic Highway data bus and carries video data input.
HS	I	HSYNC. HSYNC input signaling the transition from one line to the next.
VS	I	VSYNC. VSYNC input signaling the transition from one frame to the next.

Table 2-1. Pin Descriptions (Continued)

Symbol	Type	Description
POWER AND GROUND		
VDDCORE	I	Core digital power supply
VDDLPB	I	LPB power supply
VDDMEM	I	Memory subsystem digital power supply (3.3V or 5V - see Section 3.4 for more information on mixed voltage operation)
VDDMTOL	I	3.3V or 5V tolerance for memory subsystem (see Section 3.4 for more information on mixed voltage operation)
VDDSYS	I	PCI Bus subsystem digital power supply
AVDD	I	Analog power supply (RAMDAC). This must be the same voltage as VDDCORE.
CLKAVDD[1:2]	I	Analog power supply (clock synthesizer, 1 = MCLK, 2 = DCLK). This must be the same voltage as VDDCORE.
VSS	I	Digital ground
AVSS	I	Analog ground

2.3 PIN LISTS

Table 2-2 lists all pins alphabetically. Table 2-3 lists all pins in numerical order.

Table 2-2. Alphabetical Pin Listing

	PIN(S)
Name	
AB	172
ACLK	187
AD[31:16]	206, 207, 208, 3, 4, 5, 6, 7, 11, 12, 13, 15,16, 17, 18, 19
AD[15:0]	30, 31, 32, 33, 34, 35, 36, 38, 40, 41, 42, 43, 44, 46, 47, 48
AG	171
AR	168
AVDD	164, 169, 170
AVSS	159, 161, 163, 167, 173
$\overline{\text{BLANK}}$	195
$\overline{\text{CAS}}$[7:0]	114, 112, 117, 110, 113, 111, 116, 108
$\overline{\text{C/BE}}$[3:0]	8, 20, 29, 39
CLKAVDD[1:2]	158, 160
$\overline{\text{CREQ}}$/CRDY	193
$\overline{\text{DEVSEL}}$	24
$\overline{\text{ENFEAT}}$	196
ESYNC	194
EVCLK	194
EVIDEO	192
$\overline{\text{FRAME}}$	21
RA[15:0]	154, 149, 145, 137, 133, 129, 123, 119, 101, 97, 92, 87, 68, 63, 59, 53
RD[7:0]	104, 99, 94, 89, 70, 65, 61, 56
GOP[1:0]	198, 196
HS	192
HSYNC	184
IDSEL	9
$\overline{\text{INTA}}$	197
$\overline{\text{IRDY}}$	22
LCLK	183
LD[7:0]	182, 181, 180, 178, 177, 176, 175, 174
MA[11:0]	84, 81, 86, 85, 83, 80, 79, 78, 76, 75, 74, 73
MD[63:48]	153, 148, 144, 141, 136, 132, 128, 122, 5, 100, 96, 91, 71, 66, 62, 58
MD[47:32]	155, 151, 146, 139, 134, 130, 125, 120, 103, 98, 93, 88, 69, 64, 60, 55
MD[31:16]	152, 147, 143, 140, 135, 131, 126, 121, 104, 99, 94, 89, 70, 65, 61, 56
MD[15:0]	154, 149, 145, 137, 133, 129, 123, 119, 101, 97, 92, 87, 68, 63, 59, 53

Table 2-2. Alphabetical Pin Listing (Continued)

Name	PIN(S)
$\overline{\text{MGNT}}$	189
MPR	188
$\overline{\text{MREQ}}$	190
PA[7:0]	182, 181, 180, 178, 177, 176, 175, 174
PAR	27
$\overline{\text{PDOWN}}$	165
$\overline{\text{RAS}}$	107
RESERVED	50, 51, 52, 200, 201
$\overline{\text{RESET}}$	205
$\overline{\text{ROMEN}}$	204
RSET	166
SCLK	1
SPCLK	202
SPD	203
$\overline{\text{STOP}}$	26
$\overline{\text{STWR}}$	198
TRDY	23
$\overline{\text{VCLK}}$	183
VDDCORE	54, 82, 142, 186
VDDLPB	191
VDDMEM	72, 95, 124
VDDMTOL	109
VDDSYS	10, 28, 45
$\overline{\text{VREQ}}$/VRDY	192
VREF	162
VS	193
VSS	2, 14, 25, 37, 49, 57, 67, 77, 90, 102, 106, 115, 127, 138, 150, 179, 199
VSYNC	185
$\overline{\text{WE}}$	118
XIN	156
XOUT	157

Table 2-3. Numerical Pin Listing

Number	Pin	Number	Pin
1	SCLK	43	AD4
2	**VSS**	44	AD3
3	AD28	45	**VDDSYS**
4	AD27	46	AD2
5	AD26	47	AD1
6	AD25	48	AD0
7	AD24	49	**VSS**
8	C/BE3	50	RESERVED
9	IDSEL	51	RESERVED
10	**VDDSYS**	52	RESERVED
11	AD23	53	MD0
12	AD22	54	**VDDCORE**
13	AD21	55	MD32
14	**VSS**	56	MD16
15	AD20	57	**VSS**
16	AD19	58	MD48
17	AD18	59	MD1
18	AD17	60	MD33
19	AD16	61	MD17
20	C/BE2	62	MD49
21	FRAME	63	MD2
22	IRDY	64	MD34
23	TRDY	65	MD18
24	DEVSEL	66	MD50
25	**VSS**	67	**VSS**
26	STOP	68	MD3
27	PAR	69	MD35
28	**VDDSYS**	70	MD19
29	C/BE1	71	MD51
30	AD15	72	**VDDMEM**
31	AD14	73	MA0
32	AD13	74	MA1
33	AD12	75	MA2
34	AD11	76	MA3
35	AD10	77	**VSS**
36	AD9	78	MA4
37	**VSS**	79	MA5
38	AD8	80	MA6
39	C/BE0	81	MA10
40	AD7	82	**VDDCORE**
41	AD6	83	MA7
42	AD5	84	MA11

Table 2-3. Numerical Pin Listing (Continued)

Number	Pin	Number	Pin
85	MA8	127	**VSS**
86	MA9	128	MD57
87	MD4	129	MD10
88	MD36	130	MD42
89	MD20	131	MD26
90	**VSS**	132	MD58
91	MD52	133	MD11
92	MD5	134	MD43
93	MD37	135	MD27
94	MD21	136	MD59
95	**VDDMEM**	137	MD27
96	MD53	138	**VSS**
97	MD6	139	MD44
98	MD38	140	MD28
99	MD22	141	MD60
100	MD54	142	**VDDCORE**
101	MD7	143	MD29
102	**VSS**	144	MD61
103	MD39	145	MD13
104	MD23	146	MD45
105	MD55	147	MD30
106	**VSS**	148	MD62
107	$\overline{\text{RAS}}$	149	MD14
108	$\overline{\text{CAS0}}$	150	**VSS**
109	**VDDMTOL**	151	MD46
110	$\overline{\text{CAS4}}$	152	MD31
111	$\overline{\text{CAS2}}$	153	MD63
112	$\overline{\text{CAS6}}$	154	MD15
113	$\overline{\text{CAS3}}$	155	MD47
114	$\overline{\text{CAS7}}$	156	XIN
115	**VSS**	157	XOUT
116	$\overline{\text{CAS1}}$	158	**CLKAVDD1**
117	$\overline{\text{CAS5}}$	159	**AVSS**
118	$\overline{\text{WE}}$	160	**CLKAVDD2**
119	MD8	161	**AVSS**
120	MD40	162	VREF
121	MD24	163	**AVSS**
122	MD56	164	**AVDD**
123	MD9	165	$\overline{\text{PDOWN}}$
124	**VDDMEM**	166	RSET
125	MD41	167	**AVSS**
126	MD25	168	AR

Table 2-3. Numerical Pin Listing (Continued)

Number	Pin
169	**AVDD**
170	**AVDD**
171	AG
172	AB
173	**AVSS**
174	LD0/PA0
175	LD1/PA1
176	LD2/PA2
177	LD3/PA3
178	LD4/PA4
179	**VSS**
180	LD5/PA5
181	LD6/PA6
182	LD7/PA7
183	LCLK/VCLK
184	HSYNC
185	VSYNC
186	**VDDCORE**
187	ACLK
188	MPR
189	$\overline{\text{MGNT}}$
190	$\overline{\text{MREQ}}$
191	**VDDLPB**
192	$\overline{\text{VREQ}}$/VRDY/HS/EVIDEO
193	$\overline{\text{CREQ}}$/CRDY/VS/EVCLK
194	ESYNC
195	$\overline{\text{BLANK}}$
196	$\overline{\text{ENFEAT}}$/GOP0
197	$\overline{\text{INTA}}$
198	$\overline{\text{STWR}}$/GOP1
199	**VSS**
200	RESERVED
201	RESERVED
202	SPCLK
203	SPD
204	$\overline{\text{ROMEN}}$
205	$\overline{\text{RESET}}$
206	AD31
207	AD30
208	AD29

Section 3: Functional Changes from Trio64V+

3.1 RESET/POWER-ON STRAPPING

The logic levels on PD[28:0] are latched in register bits for Trio64V+ and these pins are pulled up internally. However, only the logic value on MD11 is latched in a register bit (CR37_3) for Trio64UV+ and all MD pin pull-ups are removed. MD11 can only be strapped in a test configuration (to allow use of external MCLK and DCLK) and must never be strapped in an operational system.

The default values for some of the former (Trio64V+) power-on strapping bits have been changed so that Trio64UV+ will power up in a standard, operational configuration, e.g., in fast page memory mode using internal MCLK and DCLK.

3.2 MEMORY INTERFACE

Trio64UV+ system and memory interface is shown in Figure 3-1.

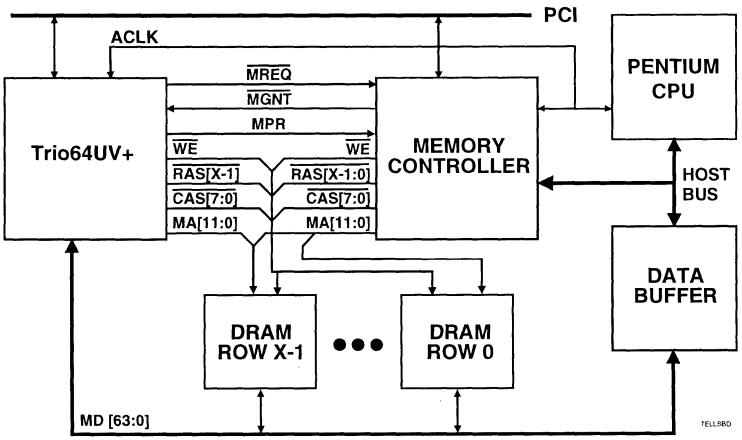


Figure 3-1. System and Memory Interface Block Diagram

Note to Figure 3-1

1. Trio64UV+ drives MA[11:0] only to DRAM row x-1. This is the first (physically) installed bank. The DRAM assigned to Trio64UV+ is then mapped by the core logic to the highest area of memory.

3.2.1 Memory Map

Trio64UV+ UMA frame buffer is located at the very top of physical memory. This is illustrated by Figure 3-2.

3.2.2 Address Translation

Address translation for MA[11:0] varies among core logic companies. Trio64UV+ supports a number of these variations as shown in Figure 3-3. The blank cells are for addresses above A20. These are always driven high by Trio64UV+ because it is always located at the top of the memory address space. The desired map is selected via CR81_6-4.

3.2.3 DRAM Types Supported

Trio64UV+ supports Fast Page and EDO memory in SIMM configuration, with EDO strongly preferred for its higher bandwidth. SDRAM pins are reserved for future use.

3.3 MEMORY ARBITRATION

3.3.1 Protocol Description

The arbitration scheme allows the core logic and Trio64UV+ to share memory resources effectively while minimizing performance degradation. The core logic is the memory owner; Trio64UV+ requests the memory when it needs access. In order to communicate the urgency of

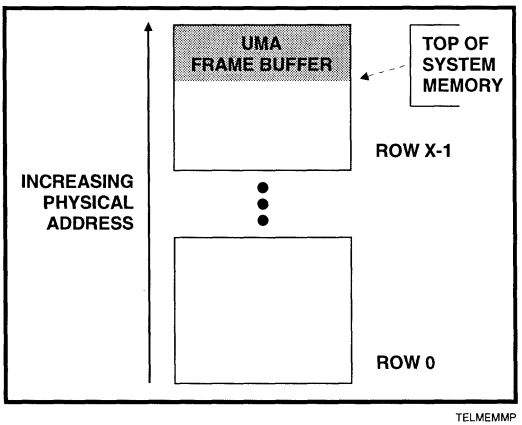


Figure 3-2. Memory Map

Notes to Figure 3-2

1. "Top of system memory" refers to top of memory as reported to the operating system. The UMA frame buffer is located above that (and could be mapped by the core logic to a higher, non-contiguous location).
2. The UMA frame buffer is not accessible to the Operating System as system memory, but device drivers could access this region through the core logic memory controller (MC). This region must be made non-cacheable as no bus snooping is done.
3. PCI masters can access the UMA frame buffer only through Trio64UV+. Therefore:
   A. The MC must ignore PCI master accesses with the UMA frame buffer as the target (the MC cannot claim the cycle)
   B. Trio64UV+ must implement a standard PCI base address for the UMA frame buffer.

VUMA standard (symmetric and asymmetric x9 and x10)

	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
Row				A20	A19	A18	A17	A16	A15	A14	A13	A12
Col				A11	A10	A9	A8	A7	A6	A5	A4	A3

VUMA (asymmetric x8)

	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
Row			A11	A20	A19	A18	A17	A16	A15	A14	A13	A12
Col					A10	A9	A8	A7	A6	A5	A4	A3

Alternate A (10x10, 11x10)

	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
Row				A20	A19	A18	A17	A16	A15	A14	A13	A12
Col			A11		A10	A9	A8	A7	A6	A5	A4	A3

Alternate B (11x11)

	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
Row				A20	A19	A18	A17	A16	A15	A14	A13	A12
Col		A11			A10	A9	A8	A7	A6	A5	A4	A3

Alternate C (12x8, 12x10)

	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
Row	A11			A20	A19	A18	A17	A16	A15	A14	A13	A12
Col					A10	A9	A8	A7	A6	A5	A4	A3

Figure 3-3. Address Translation

a given request, there are two types of requests: high priority and normal (i.e., low priority). A four pin interface controls this communication:

$\overline{\text{MREQ}}$ - *Memory Request* indicates to the core logic that Trio64UV+ wants control of the memory.

$\overline{\text{MGNT}}$ - *Memory Grant* indicates to the Trio64UV+ that access to the memory has been granted.

MPR - *Memory Priority* indicates the priority of a given request. A high state indicates a high priority request, while a low state indicates a normal request. This pin has no meaning when $\overline{\text{MREQ}}$ is not asserted. It also has no meaning when a 2-pin arbitration scheme is selected via CR81_1-0.

ACLK - *Arbitration Clock* provides timing for these arbitration signals, all of which are sampled on the rising edge. This is the same clock as the host clock.

3.3.2 Arbitration Timing Diagrams

Trio64UV+ supports several protocols for both normal and high priority memory arbitration. The timing diagrams for the VUMA protocols are presented in this section. The Intel SMBA proto-

col is also supported. Contact Intel for the specifications.

Figure 3-4 illustrates the basic (low priority) VUMA-style synchronous arbitration protocol for a 2-cycle EDO read. This protocol is selected when CR81_1-0 = 00b.

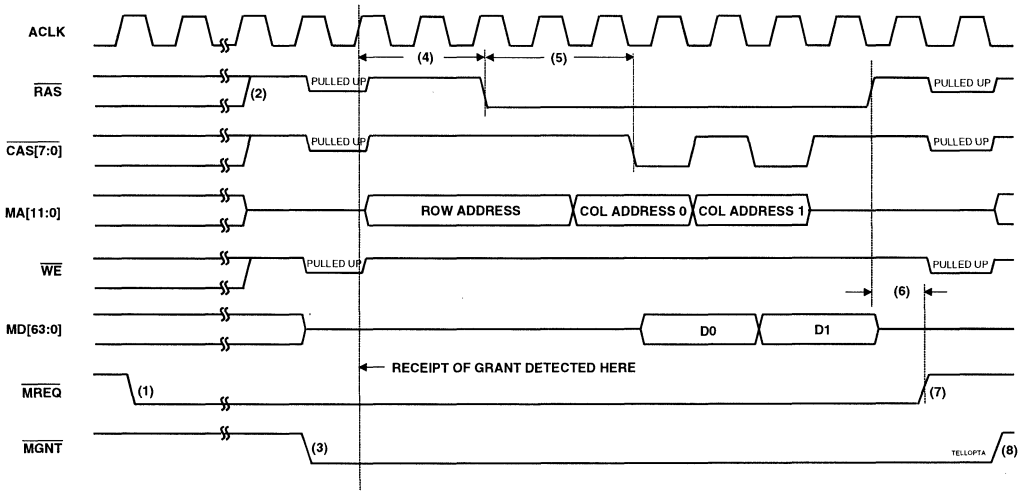


Figure 3-4. VUMA-Style Low Priority Arbitration

Notes to Figure 3-4

1. Trio64UV+ asserts $\overline{\text{MREQ}}$ to access memory when necessary, for example a graphics engine command or as the display FIFO begins to empty.
2. The core logic responds by driving $\overline{\text{RAS}}$, $\overline{\text{CAS}}$[7:0] and $\overline{\text{WE}}$ high for at least one clock.
3. The core logic alerts Trio64UV+ that it has granted the bus by asserting $\overline{\text{MGNT}}$. $\overline{\text{RAS}}$, $\overline{\text{CAS}}$[7:0], and $\overline{\text{WE}}$ float for one clock, after which Trio64UV+ takes over by driving the row address. Note that the floating signals are held high by internal or external pull-ups.
4. The time between recognition of the grant and assertion of $\overline{\text{RAS}}$ is programmable via CR83_3-2.
5. The $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ time is programmable (CR58_7 and CR83_4).
6. The time between $\overline{\text{RAS}}$ high and $\overline{\text{MREQ}}$ high is programmable via CR83_1-0. A value of 1 cycle is shown.
7. One clock after Trio64UV+ has finished its memory accesses, it deasserts $\overline{\text{MREQ}}$ and floats $\overline{\text{RAS}}$, $\overline{\text{CAS}}$[7:0] and $\overline{\text{WE}}$ for one clock. $\overline{\text{RAS}}$, $\overline{\text{CAS}}$[7:0] and $\overline{\text{WE}}$ must have been held high for one clock prior to this time. The MA and MD busses are both tri-stated.
8. The core logic responds by deasserting $\overline{\text{MGNT}}$ one cycle later.

Figure 3-5 shows the operation of a high priority request using the S3 3-pin arbitration (CR81_1-0 = 10b).

Figure 3-6 shows a high priority request using 2-pin arbitration (see CR81_1-0).

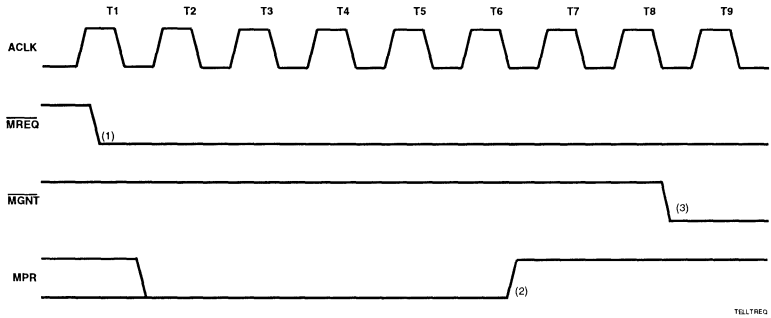


Figure 3-5. S3 3-Pin Arbitration

Notes to Figure 3-5

1. Trio64UV+ requests memory control.
2. If the core logic does not respond with $\overline{\text{MGNT}}$ soon enough, causing the display FIFO to hit its near-empty watermark, Trio64UV+ raises the priority of its request by asserting MPR, and keeping it asserted until memory is granted.
3. The core logic asserts $\overline{\text{MGNT}}$ soon thereafter in response to the high priority request. Note that the request could have been issued as high priority from its onset if necessary. The worst-case latency for the core logic to respond to a high priority request is defined as 35 ACLKs in the VUMA specification.

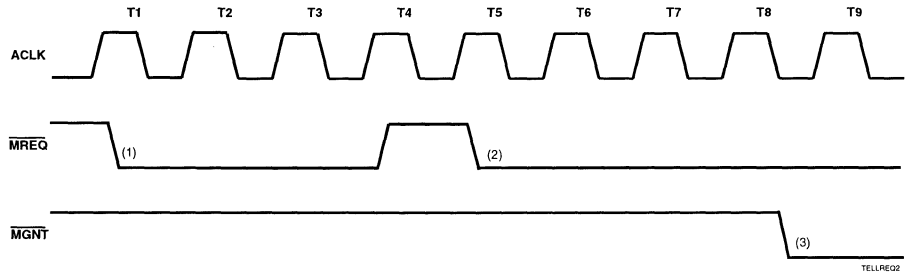


Figure 3-6. 2-Pin Arbitration

Notes to Figure 3-6

1. Trio64UV+ requests memory control. The request is low priority.
2. If the core logic does not respond with $\overline{\text{MGNT}}$ soon enough, causing the FIFO to hit its near-empty watermark, Trio64UV+ pulses the $\overline{\text{MREQ}}$ signal. This coverts the request to high priority.
3. The core logic asserts $\overline{\text{MGNT}}$ soon thereafter in response to the high priority request. The worst-case latency for the core logic to respond to a high priority request is defined as 35 ACLKs in

Figure 3-7 shows a situation where the core logic needs memory control back before Trio64UV+ is done.

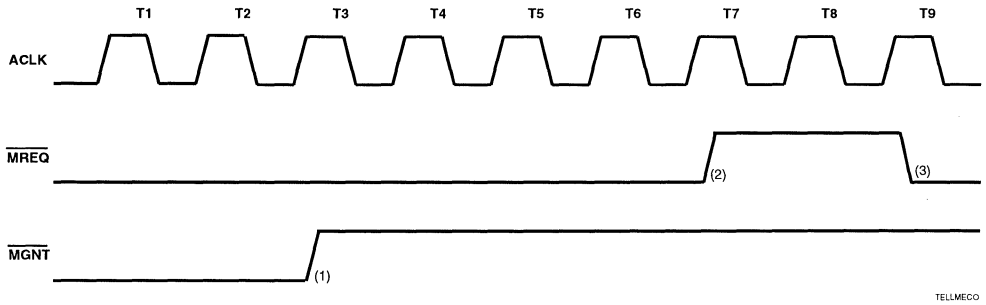


Figure 3-7. Early Withdrawal of the Bus Grant

Notes to Figure 3-7

1. This example begins with Trio64UV+ having memory control. The core logic deasserts $\overline{\text{MGNT}}$ when it needs memory control (e.g., for DRAM refresh) before Trio64UV+ is done.
2. Trio64UV+ must respond to this request as soon as possible by deasserting $\overline{\text{MREQ}}$. The worst-case latency for Trio64UV+ to respond is screen resolution dependent. The worst case is approximately 80 ACLKs, but this is not guaranteed.
3. After giving up memory control in this way, it is likely that Trio64UV+ will immediately start requesting again since it presumably has unfinished tasks which need access to memory. $\overline{\text{MREQ}}$ needs to be deasserted for at least two full clock cycles.

3.4 MIXED VOLTAGE SUPPORT

Trio64UV+ is designed as an OEM selectable 5V/3.3V voltage part in order to interface with forthcoming 3.3V memories and core logic. Trio64UV+ has two isolated digital power planes as described below.

1. All core functions in Trio64UV+ are still 5V, and are powered by VDDCORE. The LPB is also 5V and is powered by VDDLPB. The PCI subsystem is 5V and is powered by VDDSYS.
2. The memory interface unit is powered by VDDMEM. VDDMEM can be connected to a 5V or 3.3V source, and all output levels from this portion of Trio64UV+ will be driven to the VDDMEM source level. The affected signals are MD[63:0], MA[11:0], $\overline{\text{CAS}}$[7:0], $\overline{\text{RAS}}$ and $\overline{\text{WE}}$.

   If 5V memories are used with 3.3V core logic, VDDMEM for Trio64UV+ must be set to 3.3V and VDDMTOL must be set to 5V. If 3.3V memories are used with 3.3V core logic, both VDDMEM and VDDMTOL must be set to 3.3V. With 5V core logic and memories, both VDDMEM and VDDMTOL must be set to 5V.

A single digital ground plane is used.

3.5 OPERATING MODES

Trio64UV+ supports two operating modes as shown in Table 3-1.

Table 3-1. Operating Modes

UMA Arbitration	DRAM Refresh Owner	Operating Mode
Enabled	CPU	UMA mode (Note 1)
Disabled	Trio64UV+	Test (Note 2)

Notes

1. UMA Mode is the "normal" operational mode. This mode is selected when CR82_1-0 = 00b.
2. Test mode is used for validation when Trio64UV+ operates out of a private memory bank. In addition, UMA arbitration is turned off, giving Trio64UV+ unlimited access to memory. This mode also allows Trio64UV+ to operate as a standalone Trio64V+ with virtually complete functionality. This mode is selected when CR82_1-0 = 11b.

Section 4: Register Changes from Trio64V+

4.1 REGISTERS CHANGED

Register	Bit(s)	Description
SRA	6	Reserved (RAS1 eliminated)
SRD	1	0 = Reserved (Trio64-compatible VAFC feature connector eliminated)
SR1C	1-0	The VL-Bus selections are eliminated.
CR2E	7-0	New chip ID = 14H
CR2F	7-0	Revision ID = xxH
CR34	4	Reserved (CR3B not used)
CR36	1-0	Reserved - Hardwired to boot in PCI mode
CR36	3-2	MD pin values are not latched into these bits on reset. The default value is 11b (fast page mode DRAM operation). 1-cycle EDO operation is not supported.
CR36	4	Reserved (no VL-Bus)
CR36	7-5	000 = Reserved (4 MBytes not supported) 101 = 1.5 MBytes 111 = 0.5 MByte
CR37	0	Reserved (no VL-Bus)
CR37	2	Reserved (no VL-Bus)
CR37	3	An MD pin value is not latched into this bit on reset. The default value is 1 (use internal clocks).
CR37	4	Reserved (no VL-Bus)
CR3B	7-0	Reserved (Replaced by CR85_1-0)
CR40	4	Reserved (no VL-Bus)
CR53	4-3	No VL-Bus power-on default
CR58	1-0	11 = Reserved (no 4-MByte window). For a 0.5 MByte frame buffer, the linear addressing window size should be set to 1 MByte. For a 1.5 MByte frame buffer, the linear addressing window size should be set to 2 MBytes. In either case, software must not write beyond the size specified for the frame buffer.
CR58	3	Reserved (no VL-Bus)
CR59,CR5A	15-0	No VL-Bus power-on default. No 4-MByte window.
CR5D	6	Reserved (CR3B not used)

CR68	1-0	MD pin values are not latched into these bits on reset. The default value is 11b (no stretch).
CR68	2	An MD pin value is not latched into this bit on reset. The default value is 1 (3.5 MCLKs).
CR68	3	An MD pin value is not latched into this bit on reset. The default value is 1 (2.5 MCLKs).
CR68	7	Reserved
CR69	4	Reserved (2 MByte maximum memory)
CR6A	5	Reserved (2 MByte maximum memory)
CR6F	0	Reserved (hardwired to select LPB mode).
CR6F	2-1	Reserved (with no strapping, remapping the Serial Port register to an I/O port is not useful).
CR6F	4-3	MD pin values are not latched into these bits on reset. The default value is 11b (no delay).
MM81EC	2-0	Streams FIFO Sizes 000 = Primary Stream = 48 slots; Secondary Stream = 0 slots 001 = Reserved 010 = Primary Stream = 32 slots; Secondary Stream = 16 slots 011 = Primary Stream = 24 slots; Secondary Stream = 24 slots 100 = Primary Stream = 16 slots; Secondary Stream = 32 slots 101 = Reserved 110 = Reserved 111 = Primary Stream = 0 slots; Secondary Stream = 48 slots Each slot holds one quadword.
MM81EC	8-3	Secondary Stream Low Water Mark Value = Low watermark threshold (expressed in # of free FIFO slots) This value must be ≤ the secondary stream FIFO size specified by the Streams FIFO size bits and ≤ the secondary stream high watermark.
MM81EC	14-9	Primary Stream Low Watermark Value = Low watermark threshold (expressed in # of free FIFO slots) This value must be ≤ the primary stream FIFO size specified by the Streams FIFO size bits and ≤ the primary stream high watermark.
MM81EC	17-15	Unchanged from Trio64V+.
MM81EC	18	This bit must be set to 1 when LPB operation is enabled.
MM81EC	24-19	Secondary Stream High Watermark Value = High watermark threshold (expressed in # of free FIFO slots) This value must be ≤ the secondary stream FIFO size specified by the Streams FIFO size bits and ≥ the secondary stream low watermark.
MM81EC	30-25	Primary Stream High Watermark Value = High watermark threshold (expressed in # of free FIFO slots) This value must be ≤ the primary stream FIFO size specified by the Streams FIFO size bits and ≥ the primary stream low watermark.
MM81EC	31	Reserved

MMFF00	3-1	001 = Reserved (no video 16 mode) 011 = Reserved (no video 8 in/out mode)
MMFF00	31	Reserved (no CL-480 support)
PCI Index 02H	15-0	Device ID = 8814H
PCI Index 08H	7-0	Revision ID = xxH

4.2 NEW REGISTERS

UMA Control 1 Register (CR81)

Read/Write Address: 3?5H, Index 81H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	ADDRESS TRANS			R	R	ARB SELECT	

Bits 1-0 ARB SELECT - Arbitration Type Select
00 = VUMA 2-pin arbitration
01 = Intel 2-pin arbitration
10 = S3 3-pin arbitration
11 = Reserved

Bits 3-2 Reserved

Bits 6-4 ADDRESS TRANS - Memory Address Translation Scheme Select
000 = VUMA Standard (Row - MA[8:0], Col - MA[8:0])
001 = VUMA Asymmetrical x8 (Row - MA[9:0], Col - MA[7:0])
010 = Alternate A (Row - MA[8:0], Col - MA[9, 7:0])
011 = Alternate B (Row - MA[8:0], Col - MA[10, 7:0])
100 = Alternate C (Row - MA[11, 8:0], Col - MA[7:0])
101 = Reserved
110 = Reserved
111 = Reserved

Bit 7 Reserved

UMA Control 2 Register (CR82)

Read/Write Address: 3?5H, Index 82H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R=0	R=0	R	MCS	OP MODE	

Bits 1-0 OP MODE - Operating Mode
00 = UMA mode (standard operation)
01 = Reserved
10 = Reserved
11 = Test mode (used for validation when Trio64UV+ operates out of a private memory bank. In addition, UMA arbitration is turned off, giving Trio64UV+ unlimited access to memory. This mode also allows Trio64UV+ to operate as a standalone Trio64V+ with virtually complete functionality.)

Bit 2 MCS - Memory Clock Select
0 = Use internal MCLK
1 = Use external ACLK for MCLK

Bit 3 Reserved

Bits 5-4 Reserved = 00b

Bits 7-6 Reserved

UMA Control 3 Register (CR83)

Read/Write Address: 3?5H, Index 83H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	BH	RHI	R=0	IRHD		MREQ HOLD	

Bits 1-0 MREQHOLD
00 = Raise $\overline{\text{MREQ}}$ high (releasing the bus) 3 cycles after the rising edge of $\overline{\text{RAS}}$
01 = Raise $\overline{\text{MREQ}}$ high (releasing the bus) 2 cycles after the rising edge of $\overline{\text{RAS}}$
10 = Raise $\overline{\text{MREQ}}$ high (releasing the bus) 1 cycle after the rising edge of $\overline{\text{RAS}}$
11 = Raise $\overline{\text{MREQ}}$ high (releasing the bus) 0 cycles after the rising edge of $\overline{\text{RAS}}$

A value of 11b must not be used with VUMA-style arbitration. With VUMA-style arbitration, the memory signals are tri-stated on the same clock edge used to drive $\overline{\text{MREQ}}$ high.

Bits 3-2 IRHD - Initial $\overline{\text{RAS}}$ High Decrease
00 = Decrease $\overline{\text{RAS}}$ high by 0 clocks after $\overline{\text{MGNT}}$ asserted
01 = Decrease $\overline{\text{RAS}}$ high by 1 clock after $\overline{\text{MGNT}}$ asserted
10 = Decrease $\overline{\text{RAS}}$ high by 2 clocks after $\overline{\text{MGNT}}$ asserted
11 = Decrease $\overline{\text{RAS}}$ high by 3 clocks after $\overline{\text{MGNT}}$ asserted

This function is only valid for the first $\overline{\text{RAS}}$ cycle after the memory bus is granted to Tri064UV+. The reduction is from the $\overline{\text{RAS}}$ high time specified by CR58_7, CR68_3 and MM81EC_16. However, no matter what settings are programmed, the actual initial $\overline{\text{RAS}}$ high time will never be reduced to less than 2 clocks.

Bit 4 Reserved = 0

Bit 5 RHI - $\overline{\text{RAS}}$ Hold Increase
0 = Delay $\overline{\text{RAS}}$ high by one clock from the last $\overline{\text{CAS}}$ high
1 = $\overline{\text{RAS}}$ driven high on same clock edge as last $\overline{\text{CAS}}$ high

Bit 6 BH - Bus Hold
0 = Hold the bus (keep $\overline{\text{MREQ}}$ low) until the chipset preempts by raising $\overline{\text{MGNT}}$ high
1 = Release the bus (raise $\overline{\text{MREQ}}$) as soon as Trio64UV+ has completed its memory access activity

Bit 7 Reserved

UMA Control 4 Register (CR84)

Read/Write Address: 3?5H, Index 84H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	AHW	BGO	MCB	R	R = 0	RAA	R = 0

Bit 0 Reserved = 0

Bit 1 RAA - ROM Access Arbitration
0 = ROM access arbitration not used
1 = ROM access arbitration enabled

Setting this bit causes the memory control unit to check for no memory activity before performing the ROM access. This may delay the ROM access, but may also prevent screen flicker during soft resets. This function is only used in test mode.

Bit 2 Reserved = 0

Bit 3 Reserved

Bit 4 MBC - Memory Control Output Buffer Select
0 = Memory control (MA[11:0], $\overline{WE}$) output buffers are 24 mA
1 = Memory control (MA[11:0], $\overline{WE}$) output buffers are 16 mA

When using 3.3V memory interface operation, the drive values are 18 mA for a setting of 0 and 12 mA for a setting of 1.

Bit 5 BGO - Bus Giveup Override
0 = N value overrides high watermark in deciding when to give up the memory bus
1 = High watermark alone determines when to give up the memory bus

Bit 6 AHW - Above High Watermark Request
0 = Bus requests when the FIFO is above its high watermark are allowed
1 = Bus requests when the FIFO is above is high watermark are not made

Bit 7 Reserved

UMA Control 5 Register (CR85)

Read/Write Address: 3?5H, Index 85H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	DDPS	LPBP	SRDRA	

Bits 1-0 SRDRA - Screen Refresh Data Request Adjustment
00 = Streams FIFO filling request initiated at earliest time after start of blanking
01 = Streams FIFO filling request initiated 1 character clock later than the time specified by setting these bits to 00b
10 = Streams FIFO filling request initiated 2 character clocks later than the time specified by setting these bits to 00b
11 = Streams FIFO filling request initiated 3 character clocks later than the time specified by setting these bits to 00b

The default setting (00b) takes into consideration the worst case latency for obtaining the memory bus once it is requested. If the latency for a given system is less, these bits can be programmed to allow more time during blanking for other activities.

Bit 2 LPBP - LPB Priority
0 = An LPB memory access request is given a high priority
1 = An LPB memory access request is given a low priority

The default (0) setting provides the maximum assurance that all incoming video data is written to memory.

Bit 3 DDPS - Disable DAC Power Saving
0 = Enable DAC power saving
1 = Disable DAC power saving

The default (0) setting allows the DACs to be automatically powered down during the blanking period to reduce power consumption.

Bits 7-4 Reserved

UMA Control 6 Register (CR86)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 86H

This register is only effective if automatic DAC power saving is enabled (CR85_3 = 0).

7	6	5	4	3	2	1	0
R	DAC POWER UP TIME						

Bits 6-0 DAC POWER UP TIME

value = number of character clocks from the start of blanking at which the internal DACs are powered up

This value must be at least 1 less than the End Horizontal Blank value programmed in CR5D_3, CR5_7 and CR3_4-0. A value of 1 less starts DAC power up 1 character clock before the end of blanking. A value of 2 less starts DAC power up 2 character clocks before the end of blanking, etc. When the DACs power up, there is a voltage spike that affects the RGB outputs if they are active. Powering up the DACs earlier reduces the power savings but also reduces the chance that the power up voltage spike will affect the active display.

Bit 7 Reserved

Section 5: Programming Considerations

5.1 SYSTEM/VIDEO BIOS INITIALIZATION PROCESS

The flowchart for the BIOS initialization process is shown in Figure 5-1.

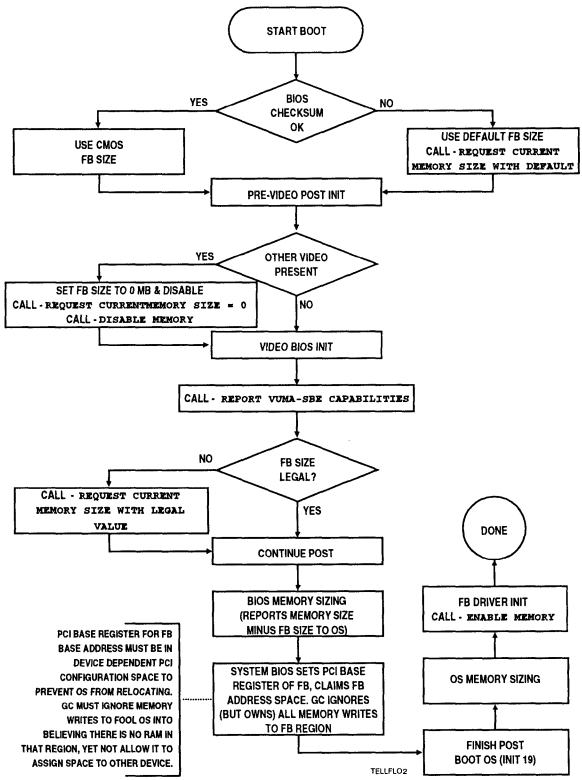


Figure 5-1. BIOS Initialization Process

5.2 MODE SETS

Software must ensure that a mode change is as transparent to the user as possible. This includes determination of when the UMA frame buffer size will change and subsequent automatic BIOS notification.This is illustrated by the flowchart in Figure 5-2.

Even though Windows 95™ will possibly support dynamic resolution changes without OS reboot, the Trio64UV+ architecture may require reboot for resolution/color changes that alter the UMA frame buffer size. Reboot is required for a growing UMA frame buffer, but optional for a shrinking one (though recovering 'extra' memory for OS use is highly recommended).

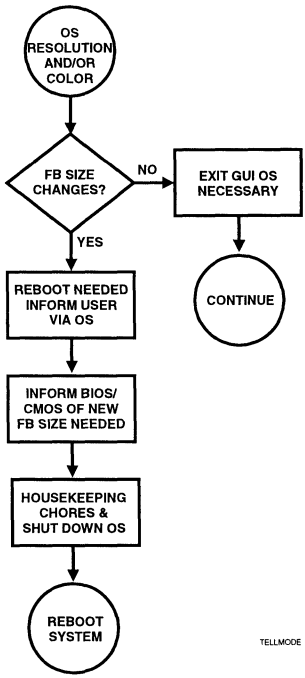


Figure 5-2. Mode Setting

Section 6: Electrical Data

6.1 MAXIMUM RATINGS

Table 6-1. Absolute Maximum Ratings

Ambient temperature	0° C to 70° C
Storage temperature	-40° C to 125° C
DC Supply Voltage	-0.5V to 7.0V
I/O Pin Voltage with respect to V_{SS}	-0.5V to V_{DD}+0.5V

6.2 DC SPECIFICATIONS

Note: In all cases below, digital VDD = 3.3 or 5V ± 5% and the operating temperature is 0° C to 70° C.

Table 6-2. RAMDAC/Clock Synthesizer DC Specifications

Symbol	Parameter	Min	Typical	Max	Unit
AVDD	DAC supply voltage	4.75	5	5.25	V
AVDD (CLOCK)	PLL supply voltage	4.75	5	5.25	V
VREF	Internal voltage reference	1.10	1.235	1.35	V

Table 6-3. RAMDAC Characteristics

	Min	Typical	Max	Unit
Resolution Each DAC		8		bits
LSB Size		66		µA
Integral Linearity Error			± 1	LSB
Differential Linearity Error			± 1	LSB
Output Full-Scale Current	15.4	17.6	19.8	mA
DAC to DAC Mismatch			5%	
Power Supply Rejection Ratio			0.5	%/ % AVDD
Output Compliance	0.0		1.5	V
Output Capacitance			30	pF
Glitch Impulse		75		pV-Sec

Table 6-4. Digital DC Specifications (VDD = 3.3V/5V ± 5%, Operating Temperature 0° C to 70° C)

Symbol	Parameter	Min (3.3V/5V)	Max (3.3V/5V)	Unit
V_{IL}	Input Low Voltage	-0.5	0.8/1.0	V
V_{IH}	Input High Voltage	2.0/1.65	V_{DD} +0.5	V
V_{OL}	Output Low Voltage		V_{SS} + 0.4	V
V_{OH}	Output High Voltage	2.4		V
I_{OL1}	Output Low Current	3/4 (Notes 1, 5)		mA
I_{OH1}	Output High Current	-1.5/-2		mA
I_{OL2}	Output Low Current	6/8 (Notes 2, 5)		mA
I_{OH2}	Output High Current	-3/-4		mA
I_{OL3}	Output Low Current	18/24 (Notes 3, 5)		mA
I_{OH3}	Output High Current	-9/-12		mA
I_{OL4}	Output Low Current	18/24 (Notes 4, 5)		mA
I_{OH4}	Output High Current	-9/-12		mA
I_{OZ}	Output Tri-state Current		1	µA
C_{IN}	Input Capacitance		5	pF
C_{OUT}	Output Capacitance		5	pF
I_{CC}	Power Supply Current		350 (Note 5)	mA

Notes for Table 6-4

1. I_{OL1}, I_{OH1} for pins LCLK, LD[7:0], MD[63:0]
2. I_{OL2}, I_{OH2} for pins $\overline{\text{ROMEN}}$, $\overline{\text{INTA}}$, $\overline{\text{STWR}}$, HSYNC, VSYNC, $\overline{\text{BLANK}}$, $\overline{\text{ENFEAT}}$, AD[31:0], $\overline{\text{VREQ}}$/VRDY, SPCLK, SPD, $\overline{\text{MREQ}}$, MPR, $\overline{\text{CAS}}$[7:0]
3. I_{OL3}, I_{OH3} for pins $\overline{\text{WE}}$, MA[11:0]. This assumes CR84_4 = 0 (default). If CR84_4 = 1, the drive levels for these pins are 12/16 mA.
4. I_{OL4}, I_{OH4} for pins PAR, $\overline{\text{STOP}}$, $\overline{\text{DEVSEL}}$, $\overline{\text{TRDY}}$, $\overline{\text{RAS}}$
5. I_{CC} measured for a resolution of 1024x768x8 with a 75 MHz DCLK and a 66 MHz MCLK at 25°C and 5V.
6. An output signal multiplexed on one of these pins has the same drive level.
7. Single value table entries are valid for both 3.3V and 5.V operation.

6.3 AC SPECIFICATIONS

Note: All AC timings are based on an 80 pF test load.

6.3.1 RAMDAC AC Specifications

Table 6-5. RAMDAC AC Specifications

Parameter	Typical	Max	Unit	Notes
DAC Output Delay	5		ns	1
DAC Output Rise/Fall Time	3		ns	2
DAC Output Settling Time	15		ns	
DAC-to-DAC Output Skew	2	5	ns	3

Notes for Table 6-5

1. Measured from the 50% point of VCLK to the 50% point of full scale transition
2. Measured from 10% to 90% full scale
3 With DAC outputs equally loaded

Table 6-6. RAMDAC Output Specifications

Description	I_{OUT} (mA)	V_{OUT} (V)	$\overline{BLANK}$	Input Data
White	17.6 typical	0.66 typical	1	FFH
Data	Data	Data	1	Data
Data (sync)	Data	Data	1	Data
Black	0	0	1	00H
Black (sync)	0	0	1	00H
$\overline{BLANK}$	0	0	0	Don't Care

Note

1.Condition for V_{OUT} is a 75 Ohm doubly terminated load, RSET = 147 Ohms and use of internal VREF.

6.3.2 Clock Timing

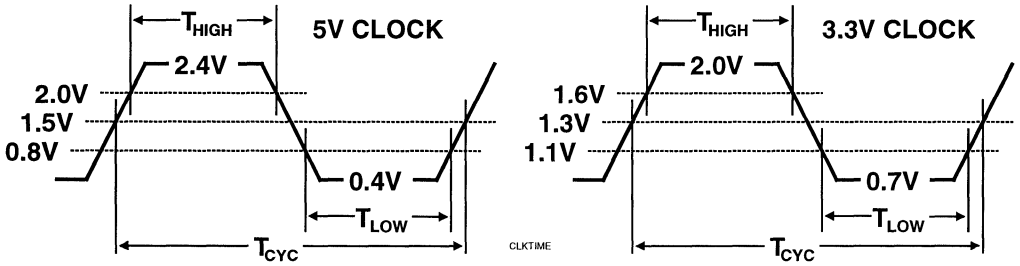


Figure 6-1. Clock Waveform Timing

Table 6-7. Clock Waveform Timing

Symbol	Parameter	Min	Max	Units	Notes
T_{CYC}	SCLK Cycle Time	30	125	ns	1
	LCLK Cycle Time	30	200	ns	
	MCLK Cycle Time	15	100	ns	
	ACLK Cycle Time	15	100	ns	
	DCLK Cycle Time (VGA Mode)	25	100	ns	1
	DCLK Cycle Time (Enhanced Mode)	12.5	100	ns	1, 2
T_{HIGH}	SCLK High Time	12	80	ns	
	LCLK High Time	12	160	ns	
	ACLK High Time	6	60	ns	
T_{LOW}	SCLK Low Time	12	80	ns	
	LCLK Low Time	12	160	ns	
	ACLK Low Time	6	60	ns	
	SCLK Slew Rate	1	4	V/ns	3
	LCLK Slew Rate	1	4	V/ns	3

Notes to Table 6-7

1. $f_{DCLK} \geq 1/2\ f_{SCLK}$ to ensure valid writes to the PLLs.
2. For DCLK rates above 80 MHz, clock doubling is used. The maximum DCLK rate with clock doubling is 67.5 MHz.
3. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to peak portion of the clock waveform.

6.3.3 Input/Output Timing

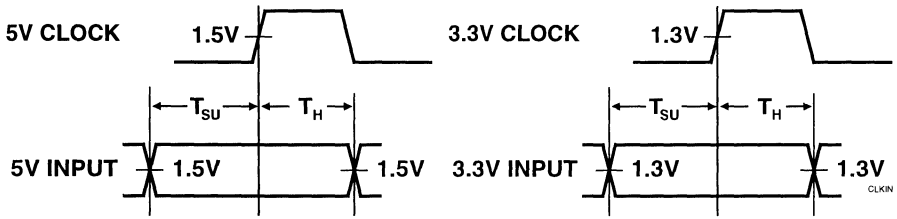


Figure 6-2. Input Timing

Table 6-8. SCLK-Referenced Input Timing

PCI Bus			
Symbol	**Parameter**	**Min**	**Units**
T_{SU}	AD[31:0], $\overline{C/BE[3:0]}$, $\overline{FRAME}$, $\overline{IRDY}$, IDSEL setup	7	ns
T_H	AD[31:0] hold	1	ns
T_H	$\overline{C/BE[3:0]}$, $\overline{FRAME}$, $\overline{IRDY}$, IDSEL hold	1	ns
T_{SU}	RD[7:0] setup	6	ns
T_H	RD[7:0] hold	1	ns

Table 6-9. LCLK-Referenced Input Timing

Scenic/MX2 Interface			
Symbol	**Parameter**	**Min**	**Units**
T_{SU}	LD[7:0] setup	10	ns
T_H	LD[7:0] hold	9	ns
T_{SU}	$\overline{CREQ}$/CRDY	6	ns
T_H	$\overline{CREQ}$/CRDY	8	ns
SAA7110 Interface			
Symbol	**Parameter**	**Min**	**Units**
T_{SU}	LD[7:0] setup	6	ns
T_H	LD[7:0] hold	8	ns
T_{SU}	HS setup	6	ns
T_H	HS hold	7	ns
T_{SU}	VS setup	6	ns
T_H	VS hold	7	ns

Table 6-10. MCLK-Referenced Input Timing

Symbol	Parameter	Min	Units
T_{SU}	MD[63:0] setup to MCLK high (2-cycle EDO)	0	ns
T_H	MD[63:0] hold from MCLK high (2-cycle EDO)	12.5	ns
T_{SU}	MD[63:0] setup to $\overline{CAS}$ high (fast page)	0	ns
T_H	MD[63:0] hold from $\overline{CAS}$ high (fast page)	15	ns

Note

1. The timing reference in each of the two cases above is to the event that causes the latching of the read data. The MCLK used to latch 2-cycle EDO data is an internal signal that cannot be directly observed. The $\overline{CAS}$ signals used to latch read data in fast page mode is derived from the internal MCLK. If the memory subsystem is driven with ACLK (CR82_2 = 1), the same timing relationships and values hold.

Table 6-11. ACLK-Referenced Input Timing

Symbol	Parameter	Min	Units
T_{SU}	$\overline{MGNT}$ setup	6	ns
T_H	$\overline{MGNT}$ hold	1	ns

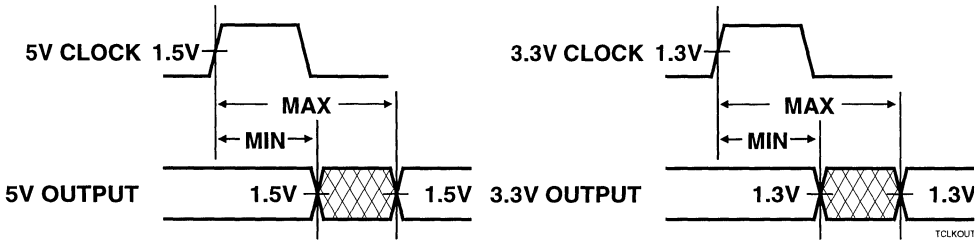


Figure 6-3. Output Timing

The minimum delay is the minimum time after the clock edge that the valid signal state from the previous cycle will begin transition to the next state (become invalid).

The maximum delay is the maximum time after the clock edge that the signal state is valid for the next cycle.

Table 6-12. SCLK-Referenced Output Timing

PCI Bus				
Parameter	**Min**	**Max**	**Units**	**Notes**
AD[31:0] valid delay	2	16	ns	1
$\overline{\text{DEVSEL}}$, PAR delay	2	11	ns	Medium $\overline{\text{DEVSEL}}$ timing used
$\overline{\text{STOP}}$ delay	2	11	ns	
$\overline{\text{TRDY}}$ delay	2	11	ns	
$\overline{\text{INTA}}$ delay	2	11	ns	
Miscellaneous				
$\overline{\text{ROMEN}}$ delay	4	10	ns	
RA[15:0] valid delay	5	30	ns	

Note

1. Due to the timing for $\overline{\text{TRDY}}$ for read cycles, data is not sampled on the clock edge immediately following its becoming valid. This guarantees the PCI 2.1 specification time of 11 ns.

Table 6-13. LCLK-Referenced Output Timing

Scenic/MX2 Interface				
Parameter	**Min**	**Max**	**Units**	**Notes**
$\overline{\text{VREQ}}$/VRDY active delay	2	11	ns	7 ns typ
LD[7:0] valid delay	2	15	ns	8 ns typ
LD[7:0] tri-state from LCLK	7	15	ns	

Table 6-14. MCLK-Referenced Output Timing

Parameter	Min	Max	Units	Notes
MD[63:0] valid delay	2	10	ns	1
MA[11:0] valid delay	1.5	8	ns	
$\overline{\text{CAS}}$[7:0] active delay	1	5.5	ns	
$\overline{\text{CAS}}$[7:0] inactive delay	1	5.5	ns	
$\overline{\text{RAS}}$ active delay	1	5	ns	
$\overline{\text{RAS}}$ inactive delay	1	6.5	ns	
$\overline{\text{WE}}$ active delay	1.5	4.5	ns	

Table 6-15. ACLK-Referenced Output Timing

Parameter	Min	Max	Units	Notes
$\overline{\text{MREQ}}$, MPR active delay	1.5	5	ns	

Table 6-16. Feature Connector Timing - Output from Trio64UV+ to Feature Connector

Symbol	Parameter	Min	Units	Notes
T_{SU}	PA[7:0], $\overline{\text{BLANK}}$ setup to VCLK rising	5	ns	
T_H	PA[7:0], $\overline{\text{BLANK}}$ hold from VCLK rising	5	ns	

Table 6-17. Feature Connector Timing - Output from Feature Connector to Trio64UV+

Symbol	Parameter	Min	Max	Units	Notes
T_{SU}	PA[7:0], $\overline{BLANK}$ setup to VCLK rising	6		ns	1
T_H	PA[7:0], $\overline{BLANK}$ hold from VCLK rising	6		ns	1
	VCLK	25	40	ns	1
	VCLK duty cycle	40	60	%	
	VCLK high time	10	25	ns	
	VCLK low time	10	25	ns	
	VCLK slew rate	1	4	V/ns	

Note

1. Pixel data is clocked into the internal RAMDAC using VCLK for the pass-through feature connector.

Section 7: Mechanical Data

7.1 THERMAL SPECIFICATIONS

Parameter	Min	Typ	Max	Unit
Thermal Resistance Θ_{JC}		5		°C/W
Thermal Resistance Θ_{JA} (Still Air)		24		°C/W
Junction Temperature			125	°C

7.2 MECHANICAL DIMENSIONS

Trio64UV+ comes in a 208-pin PQFP package. The mechanical dimensions are given in Figure 7-1.

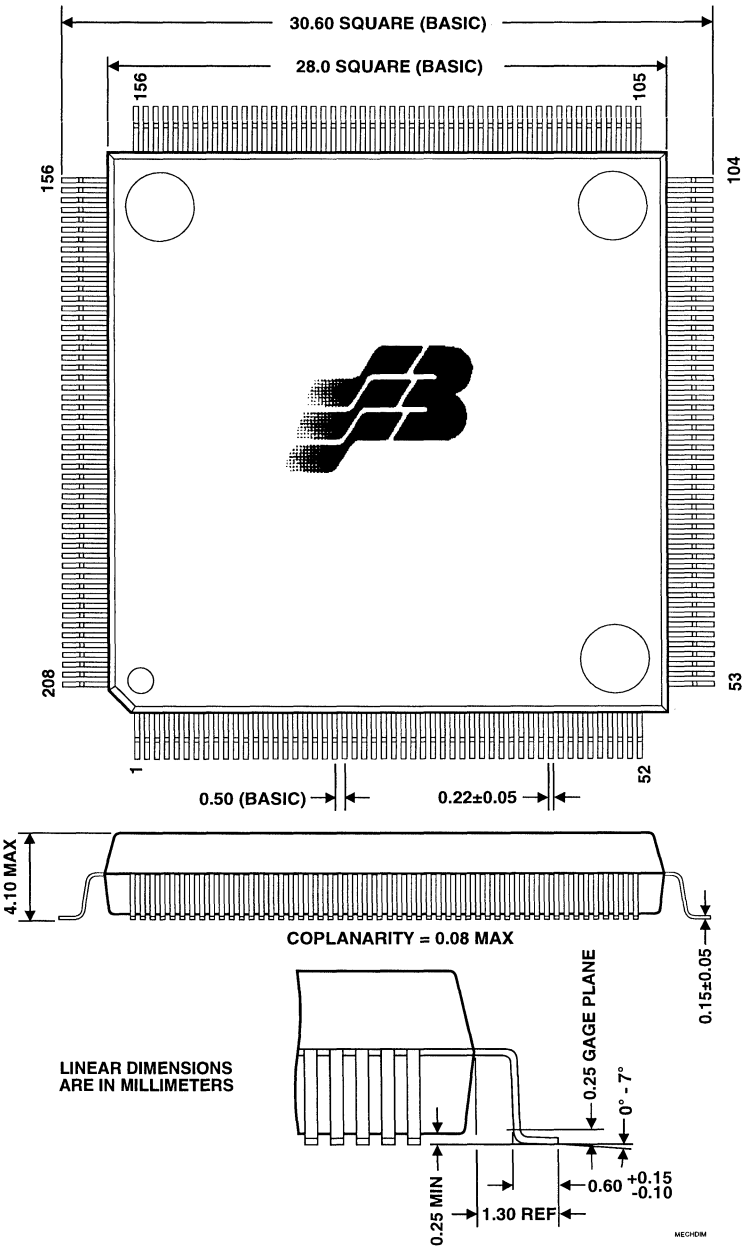


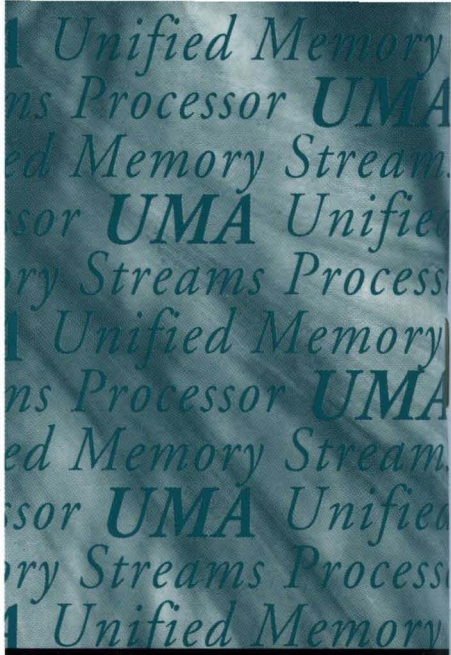
Figure 7-1. 208-pin PQFP Mechanical Dimensions

S3 Incorporated, P.O. Box 58058, Santa Clara, CA 95052-8058 Tel: 408-980-5400, Fax: 408-980-5444

S3 Trio64UV+ Data Book Update

1. (page 19-11 of the Trio64V+ data book) The combination of CR66_3 = 1 and CR66_7 = 0 is illegal and causes a system hang.
2. (page 6-8 of the Trio64UV+ data booklet) The maximum active delays for the -MREQ and MPR signals should be changed from 5 ns to 10 ns.
3. (page 4-6 of the Trio64UV+ data booklet) The setting of CR83_1-0 = 11 is illegal and causes on-screen noise.
4. (pages 20-17 and 20-18 of the Trio64V+ data book) The power-on default values for the BEE8H, Indices D and E are given in the data book as D000H and E000H respectively. These defaults should be given as "Undefined", with a note that these registers must be initialized appropriately by software before the Graphics Engine is used.

   Because writes to these registers are pipelined (see the explanation in the description of the BEE8H read only register), the "working" copy of each register does not get written until a Graphics Engine command is issued after a write. This is why the default states of the "working" registers are undefined immediately after power-up, i.e., no command has been issued to load the reset value. Software must use this two step method to initialize these registers, paying particular attention to bit 5 of BEE8H, Index E. If this is set incorrectly, the entire image could be clipped.



S3 Incorporated

P.O. Box 58058

2770 San Tomas Expwy.

Santa Clara, CA 95051-8058

Tel: (408) 980-5400

Fax: (408) 980-5444

Printed in U.S.A. on recycled paper
DB024-A