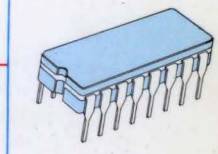
SAMSUNG

Data Book

Linear IC

VOL. 3, 1990



- Telephone
- Exchange
- Interface
- Driver

SAMSUNG
DATA BOOK LIST

I. Semiconductor Product Guide

II. Transistor Data Book

Vol. 1: Small Signal TR
Vol. 2: Bipolar Power TR
Vol. 3: TR Pellet

III. Linear IC Data Book

Vol. 1: Audio/CDP/Toy
Vol. 2: Video
Vol. 3: Telecom
Vol. 4: Industrial
Vol. 5: Data Converters

IV. CMOS Consumer IC Data Book

V. High Speed CMOS Logic Data Book

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QUALITY & RELIABILITY 1

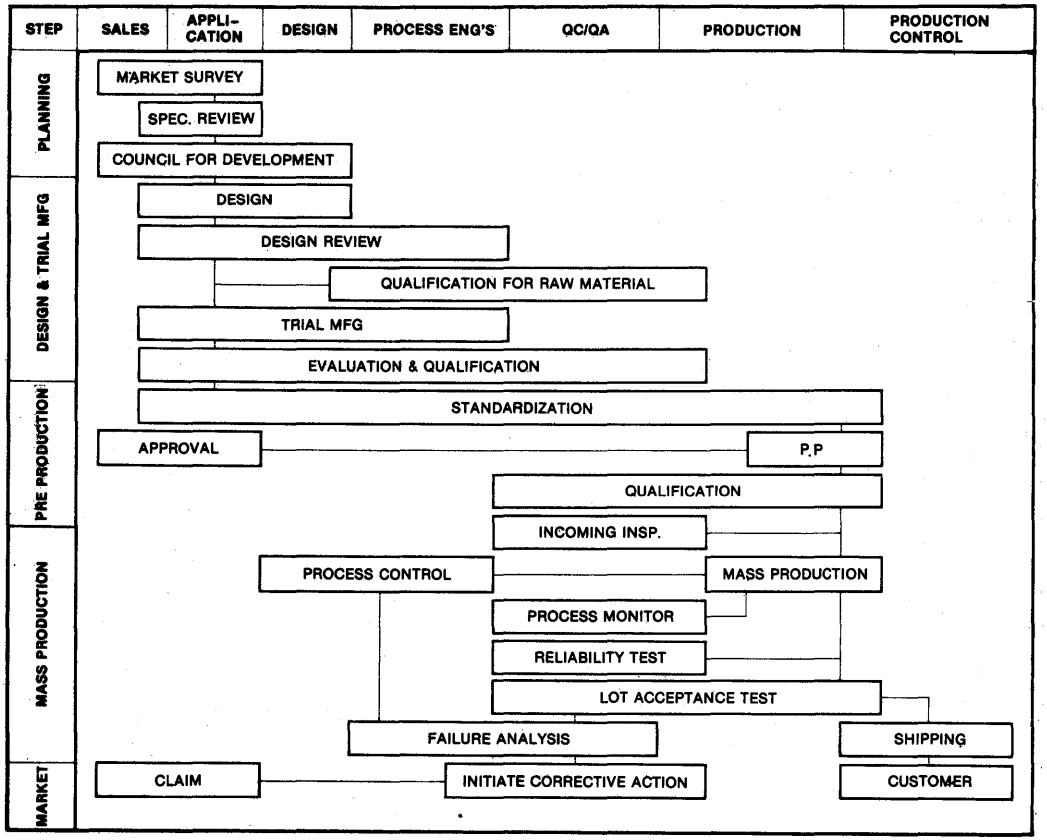
1. INTRODUCTION

SEC has been providing a wide variety of semiconductor products to the world since 1974. Since this time, extensive in-sights have been gained to create methods which most effectively result in reliable products. The worldwide customers of SEC have encouraged and helped develop the existing manufacturing and quality philosophy that is a way of life for SEC management and it's employees. This philosophy dictates the need for a zero defect environment through out SEC's processes leading ultimately to total customer satisfaction. By developing and using methods of Statistical Process Control and Statistical Quality Control, SEC has made great strides in improving product quality & reliability. The direct result of these improvements has been reduced product DPM (Defects Per Million) to levels below customer requirements. SEC's repeated ability to exceed requirements for customer's "Dock to Stock" programs and our commitment to all our customers needs, has made SEC the company to watch as we move ahead into the 1990's and beyond.

SEC's linear IC products are among the most reliable in the industry. SEC has always made a commitment to achieve the highest possible quality, reliability, and customer satisfaction with its products. Extensive qualification, monitor and outgoing programs are used to scrutinize product quality and reliability. Stringent controls are applied to every wafer fabrication and assembly lot to achieve reproducibility, and therefore maintain product reliability.

In this chapter, the quality and reliability programs established at SEC will be discussed. In addition, a description of reliability theory, reliability tests and various support efforts provides a broad framework from which to comprehend SEC quality and reliability.

To better understand the Quality Department's role in product development and manufacturing, a detailed diagram is listed below. As can be noted, Quality Engineering is involved in all phases, save that of initial product planning.

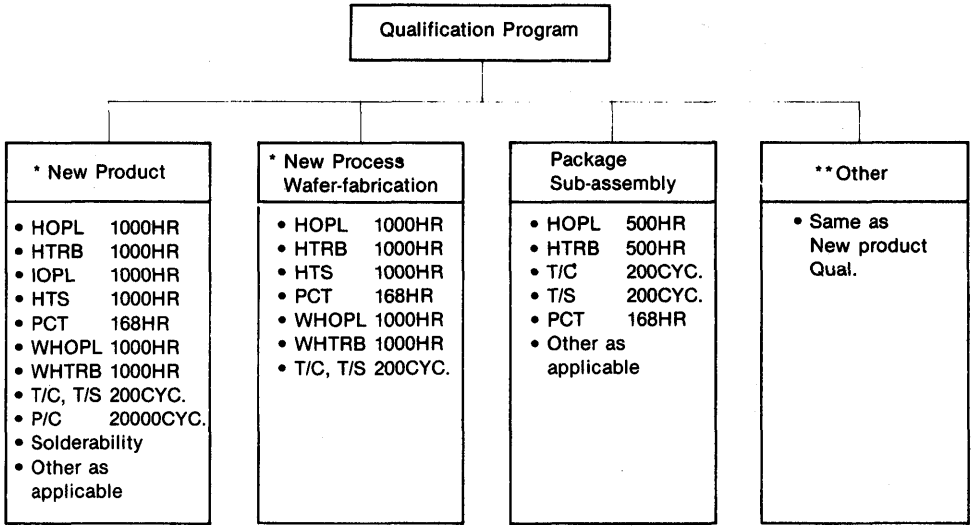


Quality Assurance During Development

2. QUALITY & RELIABILITY PROGRAM

2.1 QUALIFICATION

Procedures to qualify devices are listed below. There are both general and product-specific requirements. Procedures are detailed for new products, die-only qualifications, and package-only qualifications. The latter two are for products and/or packages already qualified, but where there is room for further product optimization.



*Testing time for each test items depends on the grade (group) of devices. (see the device group list 2.1 2))

** Design, Equipment, Material(s), etc....

1) PROCESS DEVELOPMENT QUALIFICATION

Purpose: To investigate the change of a process parameter and then apply it to a production process by reliability testing of a process which has been newly developed.

New Process, Wafer Fabrication Qualification

No	Test Item	Test Condition	Package	
			L-IC	Discrete
1	High Temperature Operating Life (HOPL)	$T_a = T_{opr}$(max) $V_{CC} = V_{CC}$(max) STATIC, DYNAMIC 1000HRS	YES	—
2	High Temperature Reverse Bias (HTRB)	$T_a = T_j$(max) $V_{CB} = 0.8 \times V_{CBO}$ 1000HRS	—	YES
3	High Temperature Storage (HTS)	$T_a = T_j$(max) 1000HRS	YES	YES
4	Pressure Cooker Test (PCT)	$T_a = 121°C \pm 2°C$ RH = 100% 15 PSIG 168HRS	YES	YES
5	Wet High Temperature Operating Life (WHOPL)	$T_a = 85°C$, RH = 85% $V_{CC} = V_{CC}$(min) 1000HRS	YES	—
6	Wet High Temperature Reverse Bias (WHTRB)	$T_a = 85°C$, RH = 85% $V_{CB} = 0.8 \times V_{CBO}$ 1000HRS	—	YES
7	Thermal Shock (T/S)	$-65°C \rightleftharpoons 150°C$ (Liquid) 5min, <10sec, 5min 200 cycles	YES	YES
8	Temperature Cycle (T/C)	$-65°C \rightleftharpoons 150°C$ (Air) 10min, 10min 200 Cycles	YES	YES

When the results of a reliability test are good, the process characteristics good and the yield level is satisfied, the process can be applied to production. If there are any problems found in a process after it has been applied to production, the problem will be investigated in detail and the process will be revised. Once the process has been revised and approved it will again be applied to production.

2) PRODUCT DEVELOPMENT QUALIFICATION

Purpose: To develop a stable and uniform product that satisfies the customer's requirements for quality by using the exact reliability test specification called out for the new product.

Products are grouped according to the importance of their application.

Group 1	Group 2	Group 3
1. A/D, D/A Converter 2. IC for LCD 3. IC for PC 4. ASIC Master 5. Codec 6. MPR 7. IC for Exchange 8. New Products	1. Transistor 2. Regulator/OP AMP 3. IC for Telephone 4. Comparator/Timer 5. MICOM 6. Audio/Video IC 7. General Mos IC	1. ASIC Opinion Product 2. Toy/Melody IC 3. MICOM family 4. Products Except Group 1, Group 2 Products

New Product Qualification Test Items

No.	Test Item	Test Condition	Part		Reference Method	Note
			L-IC	Discrete		
1	High Temperature Reverse Bias (HTRB)	Ta = T_j(max) V_{CB} = 0.8 × V_{CBO} 1000HRS	—	YES		
2	High Temperature Operating Life (HOPL)	Ta = T_{opr}(max) V_{CC} = V_{CC}(max) Static, Dynamic 1000HRS	YES	—	MIL-STD-883 1005	
3	High Temperature Storage (HTS)	Ta = T_{stg}(max) 1000HRS	YES	YES		
4	Operating Life (OPL)	Ta = 25°C P_C = P_C(max) 1000HRS	—	YES	MIL-STD-750 1026.3	For Small-Signal Device
5	Intermittent OPL (IOPL)	Ta = 25°C P_C = P_C(max) 2min/2min On/Off 1000HRS	—	YES	MIL-STD-750 1036.3	
6	Power Cycle (P/C)	ΔT_j = 125°C 120Sec/120Sec On/Off 10000CYC.	YES	YES		For PWR TR, PWR IC
7	Pressure Cooker Test (PCT)	Ta = 121°C ± 2°C RH = 100% 15PSIG 168HRS	YES	YES		
8	Wet High Temperature Reverse Bias (WHTRB)	Ta = 85°C, RH = 85% V_{CB} = 0.8 × V_{CBO} 1000HRS	—	YES		
9	Wet High Temperature Operating Life (WHOPL)	Ta = 85°C, RH = 85% V_{CC} = V_{CC}(min) Pdmin 1000HRS	YES	—		
10	Thermal Shock (T/S) (Liquid)	−65°C↔150°C 5min, <10Sec, 5min 200 Cycles	YES	YES	MIL-STD-883 1011	
11	Temperature Cycle (T/C) (Air)	−65°C↔150°C 10min, 10min 200 Cycles	YES	YES	MIL-STD-883 1011	
12	Solder Heat Resistance (S/H)	Ta = 260°C ± 5°C t = 10 ± 2Sec	YES	YES	MIL-STD-750 2031.1	
13	Solderability	Ta = 245°C ± 5°C t = 5 ± 0.5sec Reject is >10% uncovered surface	YES	YES	MIL-STD-883 2003	
14	Salt Atmosphere	Ta = 35°C, 5% NaCl 24HRS	YES	YES	MIL-STD-883 1009A	

New Products Qualification Test Item (Continued)

No.	Test Item	Test Condition	Part		Reference Method	Note
			L-IC	Discrete		
15	Mechanical Shock	1500G, 0.5ms 3 Times Each direction of X, Y and Z Axis	YES	YES	MIL-STD-750 2016	For Hermetic
16	Vibration	20G, 3 Axis f = 20 to 2000 cps for 4 min, 4 cycles	YES	YES	MIL-STD-883 2007	For Hermetic
17	Constant Acceleration	2000G X,Y,Z Axis 1min for each Axis	YES	YES	MIL-STD-883 2001	For Hermetic
18	ESD (Human Body Model)	R = 1.5kΩ C = 100pF 5 Discharge V ≥ ± 1000V	YES	YES	MIL-STD-883 3015	
19	Latch-up Test		YES	—	—	For CMOS
20	Fine Leak Gross Leak	Helium Fluoro Carbon	YES	YES	MIL-STD-883 1014	For Hermetic

Note) • SOT-23, TO-92S PKG: PCT-48HR

3) PACKAGE DEVELOPMENT QUALIFICATION

Purpose: Whenever a new package type is developed, it must meet the specifications for devices that have been qualified and have maintained certain specified quality levels before the new package type may be applied to production.

Flow	Contents	Remarks
	Beginning of PKG development	Select representative device for product group (proceed at least 2 lots)
	Ass'y Qual	• Push Test • MPT • Die Thick • Dimension • Bond Pull • X-Ray • Lead Torque • Solderability
	Reliability Qual	• HTRB (TR) • PCT • Vibration • HOPL (IC) • LTS • M/S • T/C • S/H • Const
	Approvement of Qual	• New PKG Development will be approved when Rel qual is good for 500HR.

Package Sub-Assembly Qualification Test Items

No.	Test Item	Test Condition	Package		Notes
			Plastic	Hermetic	
1	High Temperature Reverse Bias (HTRB)	$Ta = T_j(max)$ $V_{CB} = 0.8 \times V_{CBO}$ 500HRS	YES	YES	For Discrete
2	High Temperature Operating Life (HOPL)	$Ta = T_{opr}(max)$ $V_{CC} = V_{CC}(max)$ Static, Dynamic, 500HRS	YES	YES	For IC
3	Temperature Cycle (T/C)	$-65°C \rightleftharpoons 25°C \rightleftharpoons 150°C$ 10min, 5min, 10min 200 CYCLES	YES	YES	
4	Pressure Cooker Test (PCT)	$Ta = 121°C \pm 2°C$ RH = 100%, 15PSIG 168HRS	YES	—	
5	Thermal Shock (T/S)	$-65°C \rightleftharpoons 150°C$ (Liquid) 5min, < 10sec, 5min 200 CYCLES	YES	YES	
6	Solder Heat Resistance (S/H)	$260°C \pm 5°C$ 10 ± 1 sec Once without Flux	YES	YES	
7	Vibration (Variable-Frequency)	100 ~ 2000 ~ 100Hz 20G, 5min, 5Times, X, Y, Z	—	YES	For Discrete, others as applicable
8	Mechanical Shock (M/S)	1500G, 0.5ms 3 Times, X, Y, Z	—	YES	same as above
9	Constant Acceleration	20000G X, Y, Z Axis 1 min for each Axis	—	YES	same as above

4) CHANGE QUALIFICATIONS:

Purpose: To apply changes to production processes and designs by evaluating the quality levels for those processes and designs of devices in production.

Classification		Change
Design		Change of more than 1EA MASK for the product in production.
Process	Ass'y	• D/A • Coating • W/B • Mold
	Diffusion	• Diffusion/Photo/Etch, etc. • Metalization • Passivation

Procedure: Issuance of EIN for the change → Review of initial characteristics → Reliability test → Issuance of ECN (register of specification) → Application for production. Evaluation level: LTPD 10% (1/2)

2.2 MONITOR PROGRAM

1) ON GOING PROCESS CONTROL

All parameters of each process are controlled by SPC (Statistical Process Control). All resultant SPC data is gathered by computers and recorded automatically. Trends of each parameter are plotted on control charts by the computer and corrective actions are immediately taken whenever a parameter goes "out-of-control" beyond the control limits.
Whenever a parameter goes "out-of-control" in a process, engineers involved with that particular process have meetings to decide the disposition of those lots that were effected by the out-of-control process and corrective actions are implemented. In the case of critical defects, all lots are scrapped by MRB (Material Review Board).
As the key item of ongoing process control, Cp or Cpk value is controlled by computer for each process. The UCL and LCL for each process is then determined by the computer generated Cp or Cpk value. Cp or Cpk values are continually upgraded to insure the stabilization of process and a QIP (quality improvement plan) is made out to drive defects down to zero.
Process capabilities of each process are totaled and analyzed and those results of analysis are reflected on the QIP. The stabilization and maximization of process capabilities are driven by SPC.

2) PRODUCT RELIABILITY MONITOR

The reliability monitor program begins where the qualification program ends, at the start-up of limited production. Everything that is subject to qualification is considered subject to the monitor program. Generally, the product to be used for reliability monitors is gathered from each fab lot each month, where the product selected is representative of:

1) each fab process technology
2) each generic product type
3) each package technology
4) each subassembly plant

The product is shipped directly to the appropriate Q & R group, which puts the product through a series of electrical, mechanical, thermal, and environmental tests that usually are identical to those used initially for qualifying the product. Most tests are of short duration, but some may extend out to thousands of hours. Each month the test results are evaluated and problems, should they exist, identified.
Each monitor failure is analyzed. If a problem is detected where the failure rate is greater than that considered acceptable, or a reliability problem is suspected, a Material Review Board (MRB) is called. This meeting is attended by appropriate Q & R personnel, scheduling personnel, engineering, and any other affected group.
This group reviews the data, decides on disposition of the affected material, decides on appropriate corrective action, and basically controls the problem or issue until it is satisfactorily resolved.

3) FINAL QUALITY ASSURANCE PROGRAM

After the completion of the entire manufacturing process a sample of each lot is pulled and the data sheet verification test is repeated. This final verification objective is to ensure that test system to test system variations are not compromising the quality, and that inadvertent system or handling problems have not occurred.

4) ENVIRONMENT MONITOR

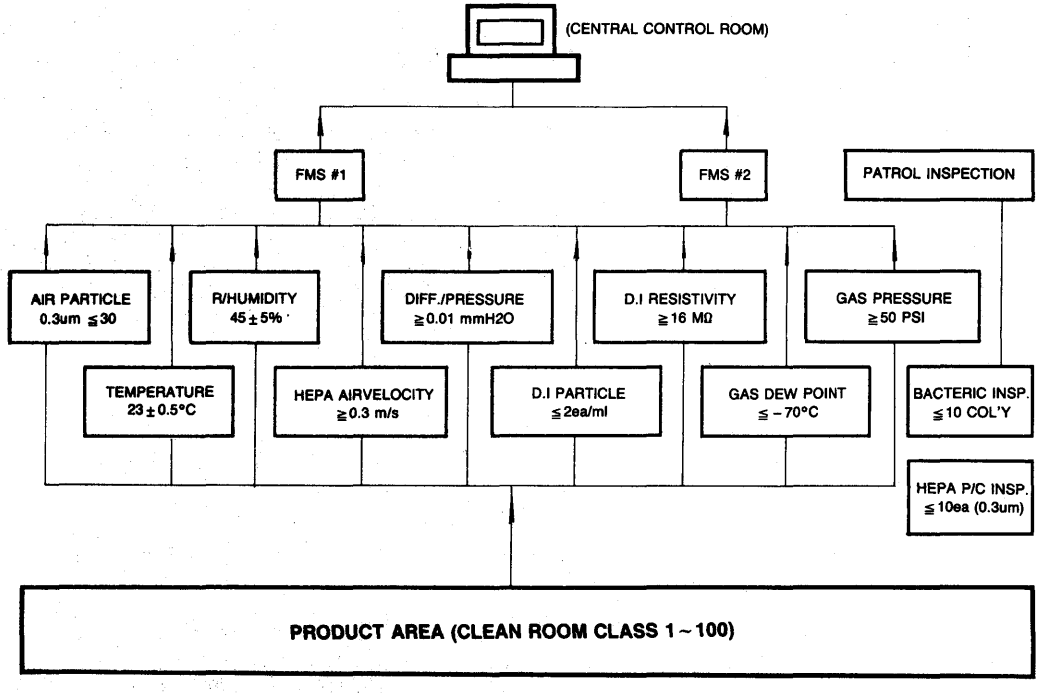
• **Instruments**

- F.M.S #1 (HIAC/ROYCO System 1 Set)
- F.M.S #2 (P.M.S System 1 Set)
- Control Particle Monitoring System (2 Set)

— On line monitoring system (Central control room)

- Portable Particle Counter, Sensors

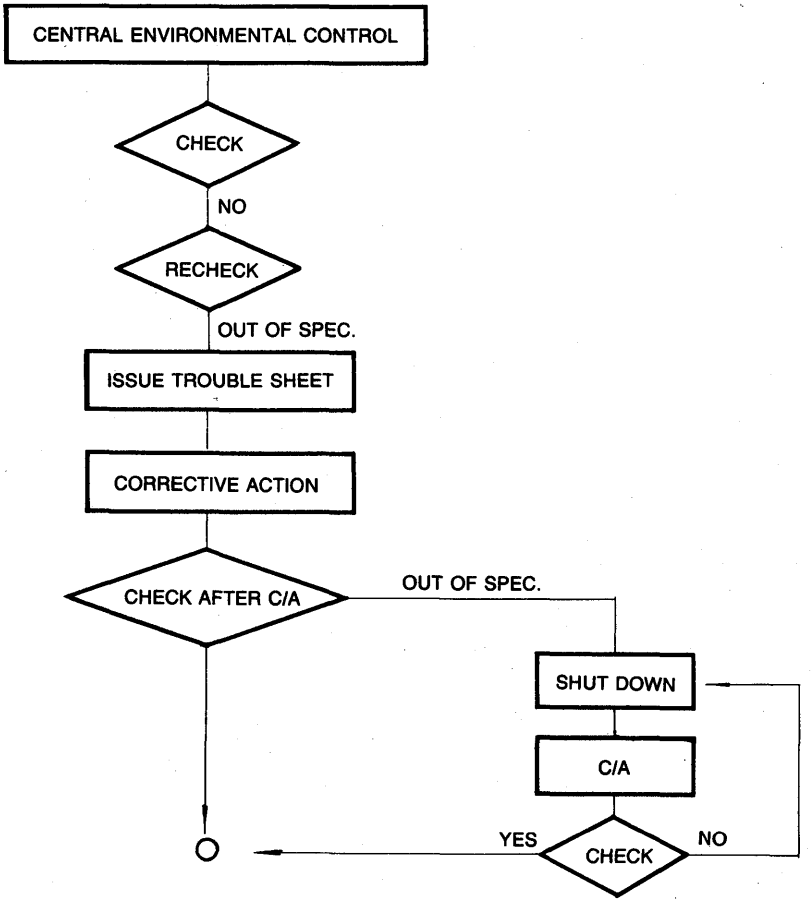
• **Block Diagram**



• **Environment Monitor**

Item	Frequency
1. Particle (Air, D-I Water)	5 min
2. Temperature, Relative Humidity	5 min
3. D.I Resistivity	5 min
4. Differential Pressure	5 min
5. HEPA Air Velocity	5 min
6. Gas (H_2, O_2, N_2, Air) Dew Point	5 min
7. Gas Pressure	5 min
8. HEPA Filter Particle	All HEPAs/1 room/Day
9. D-I Bacteria Main Lot	Weekly
10. D-I Bacteria Using Lot	Monthly

Corrective Action Requirement



2.3 QUALITY CONFORMANCE PROGRAM

1) DESCRIPTION

SEC has established a comprehensive reliability program to monitor and ensure the ongoing reliability of the Linear IC family. This program involves not only reliability data collection and analysis on existing parts, but also rigorous in-line quality controls for all products.
Listed below are details of tests performed to ensure that manufactured product continues to meet SEC's stringent quality standards. In line quality controls are reviewed extensively in later sections.
The tests run by the quality department are accelerated tests, serving to model "real world" applications through boosted temperature, voltage, and/or humidities. Accelerated conditions are used to derive device knowledge through means quicker than that of typical application situations. These accelerated conditions are then used to assess differing failure rate mechanisms that correlate directly with ambient conditions. Following are summaries of various stresses (and their conditions) run by SEC on Linear IC products.

2) HIGH TEMPERATURE OPERATING LIFE TEST (HOPL)

($T_j = 125°C$, $V_{CC} = V_{CC}$ max, static)

High temperature operating life test is performed to measure actual field reliability. Life tests of 1000HR to 2000HR durations are used to accelerate failure mechanisms by operating the device at an elevated ambient temperature (125°C). Data obtained from this test are used to predict product infant mortality, early life, and random failure rates. Data are translated to standard operating temperatures via failure analysis to determine the activation energy of each of the observed failures, using the Arrhenius relationship as previously discussed.

3) WET HIGH TEMPERATURE OPERATING LIFE TEST (WHOPL)

($Ta = 85°C$, R.H. = 85%, $V_{CC} = V_{CC}$ opt, static)

Wet high temperature operating life test is performed to evaluate the moisture resistance characteristics of plastic encapsulated components. Long time testing is performed under static bias conditions at 85°C/85 percent relative humidity with nominal voltages. To maximize metal corrosion, the biasing configuration utilizes low power levels.

4) INTERMITTENT OPERATING LIFE (IOPL)

(Pmax, 25°C, 2min on/2 min off)

This test is normally applied to scrutinize die bond thermal fatigue. A stressed device undergoes an "ON" cycle, where there is thermal heating due to power dissipation, and an "OFF " cycle, where there is thermal cooling due to lack of inputted power. Die attach (between die and package) and bond attach (between wire and die) are the critical areas of concern.

5) HIGH TEMPERATURE STORAGE TEST (HTS)

($Ta = 125°C$, UNBIASED)

High temperature storage is a test in which devices are subjected to elevated temperatures with no applied bias. The test is used to detect mechanical instabilities such as bond integrity, and process wearout mechanisms.

6) PRESSURE COOKER TEST (PCT)

(121°C, 15PSIG, 100% R.H., UNBIASED)

The pressure cooker test checks for resistance to moisture penetration. A highly pressurized vessel is used to force water (thereby promoting corrosion) into packaged devices located within the vessel.

7) TEMPERATURE CYCLING (T/C)

(−65°C to +150°C, AIR, UNBIASED)

This stess uses a chamber with alternating temperatures of −65°C and +150°C (air ambient) to thermally cycle devices within it. No bias is applied. The cycling checks for mechanical integrity of the packaged device, in particular bond wires and die attach, along with metal/polysilicon microcracks.

8) THERMAL SHOCK (T/S)

(−65°C to +150°C, LIQUID, UNBIASED)

This stress uses a chamber with alternating temperatures of −65°C to +150°C (liquid ambient) to thermally cycle devices within it. No bias is applied. The cycling is very rapid, and primarily checks for die/package compatibility.

9) RESISTANCE TO SOLDER HEAT

(UNBIASED, 260°C, 10 sec)

Solder Heat Resistance is performed to establish that devices can withstand the thermal effects of solder dip, soldering iron, or solder wave operations.

10) MECHANICAL SHOCK

(UNBIASED, 1500g, Pulse = 0.5msec)

This test determines the suitability of a device to be used in equipment where mechanical "shocks" may occur. Such shocks result from sudden or abrupt changes produced by rough (non-standard) handling, transportation, or field operations.

11) VARIABLE FREQUENCY VIBRATION

(UNBIASED, Range = 100 to 2000Hz)

Variable Frequency Vibration is done to model the effects of differential vibration in the specified range. Die attach and bonding integrity are particularly stressed, testing the mechanical soundness of device packaging.

12) CONSTANT ACCELERATION

(UNBIASED, 10kg to 20kg)

This is an accelerated test designed to indicate types or modes of structural and mechanical weaknesses not necessarily detectable in Mechanical Shock and Variable Frequency Vibration stressing.

13) RELATIVE STRESS COMPARISONS

Many stresses are run at SEC on many different devices. Through both theoretical and actual results, it was clearly determined which stresses were most effective. Also established were the stresses which weren't fully effective.

Comparisons have been made on the basis of defects able to be determined, efficiency in detection, and cost. For the reader's benefit, SEC provides the results of its conclusions on the following pages.

3. CUSTOMER SUPPORT SYSTEM

3.1 INTRODUCTION

Manufacturing companies have developed customer support systems for the purpose of uniting communications. Through these communications pass the information and knowledge required to satisfy the customers needs in areas such as quality and reliability, customer claims, customer training, field service technical issues, pricing or availability and above all, trust. Open lines of communication establishes thorough trust between the customer and vendor and are essential for such programs as dock-to-stock in order to achieve the ultimate in customer/vendor relations. SEC, in its commitment to customer satisfaction, has installed within its organization a support system that is designed to produce the open lines of communication between all facets of relations for both the customer and SEC.

3.2 POLICY

SEC has developed within its organization, a customer support system. SEC's policy requires that this system be manned with the proper personnel that are thoroughly trained in the areas that each represent and are dedicated to opening and maintaining lines of communication with the customer. Technical data used by SEC to support the customer must be up to date and always available for use by the customer (privileged or confidential information maybe excluded). Customer training is provided to the customer by only the most knowledgeable SEC personnel. SEC will provide customer field service in the form of periodic goodwill visits to customer sites or specialized problem solving services as required. Process change notification procedures as well as safety standards are also strictly adhered to.

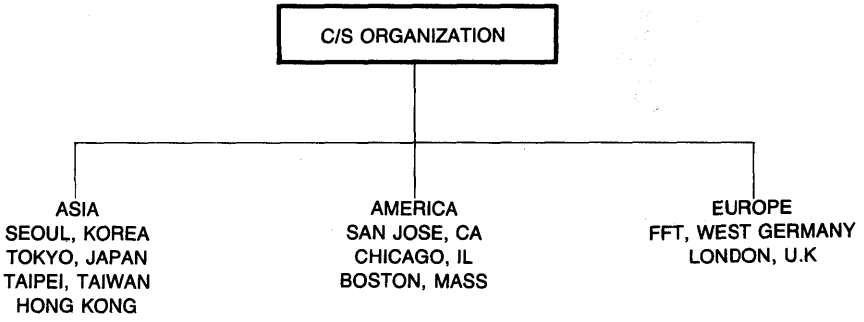
3.3 CUSTOMER SUPPORT SYSTEM

1) QUALITY ASSURANCE SERVICE

SEC has felt the need to reorganize its current Quality Assurance Sections in order to better service our customers. From this new organizational change, a new QA section was born. This new QA section, known as QA Section 3, was developed specifically for the customer. The customer service team in QA3, was organized to respond prombtly to customers quality requirements. The purpose of this team is to form a more responsive communication channel between plant R & D, the sales department and the customer. Customers will achieve satisfaction with our company's products by use of the newly organized customer service system. This service system is openly available to customers for comments concerning problems or opinions about SEC's devices. An 800 number is published on the inside of the handbooks cover.

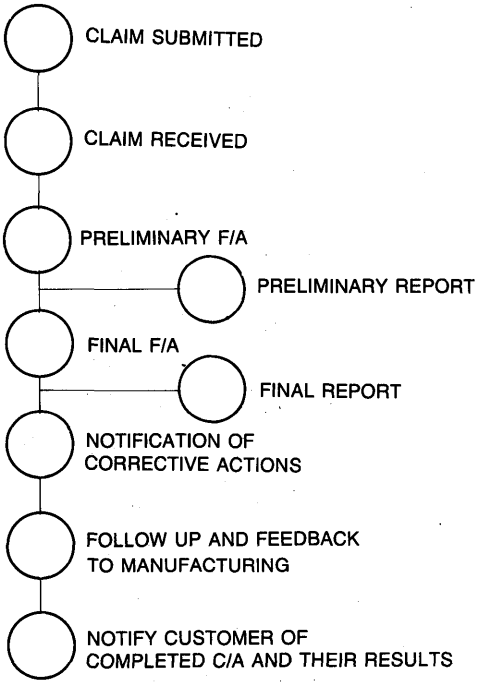
2) CUSTOMER SERVICE TEAM

The following organizational chart illustrates the world-wide base that the customer service team of SEC has established. Maintaining continuity between all of SEC's worldwide customer service teams is accomplished through the use of a newly installed computer network which allows constant communication between all teams.



3) CUSTOMER CLAIM SUPPORT SYSTEM

Information from the field concerning quality is an essential factor for the improvement of product quality. Equally important, is the investigation of field failures. Timely feedback of the results from the analysis is required to better service customers properly. This data also serves as a direct guide to the improvement of reliability and quality for both SEC and our customers.
The flowchart below demonstrates the process in which SEC currently follows for customer claims.



4) CUSTOMER TRAINING SYSTEM

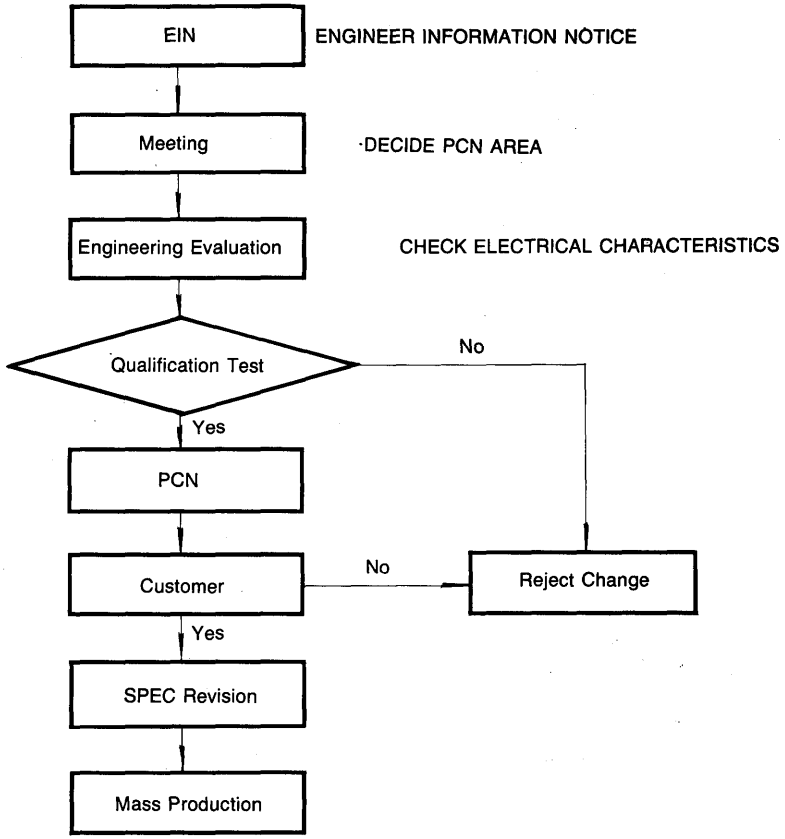
SEC has recently established a training team for the purpose of teaching SEC's customers the methods currently used by SEC to insure the product quality and reliability at the customers site. SEC offers this training in the form of group seminars or presentations and when requested or deemed necessary, individualized training is offered. In some cases, the training will take place at the customers site at the customers convenience while in other cases, SEC will extend on invitation to the customer to visit our manufacturing site.

5) CUSTOMER FIELD SERVICE

SEC has developed field service teams that are devoted to making customer contact when there aren't any problems. In other words, SEC is interested in making periodic goodwill visits. The visiting team would be comprised of those managers and engineers that are involved with the product types that the customer currently uses. The main goal of this team is to establish customer trust through communication.

3.4 PROCESS CHANGE NOTIFICATION SYSTEM (PCN)

Changes in a process are sometimes required to produce a higher quality product at a lower price. These changes can include new or different types of material, new or modified designs and new or different processes. SEC has developed a PCN procedure that is followed whenever a major or critical change is to be considered for any process. The idea behind the PCN is to allow change to a process by submitting the planned change for qualification by SEC engineering and then presenting the PCN to the customer for final approval. By following this procedure, the customer is assured that no major or critical change will occur to the process without the customers consent.



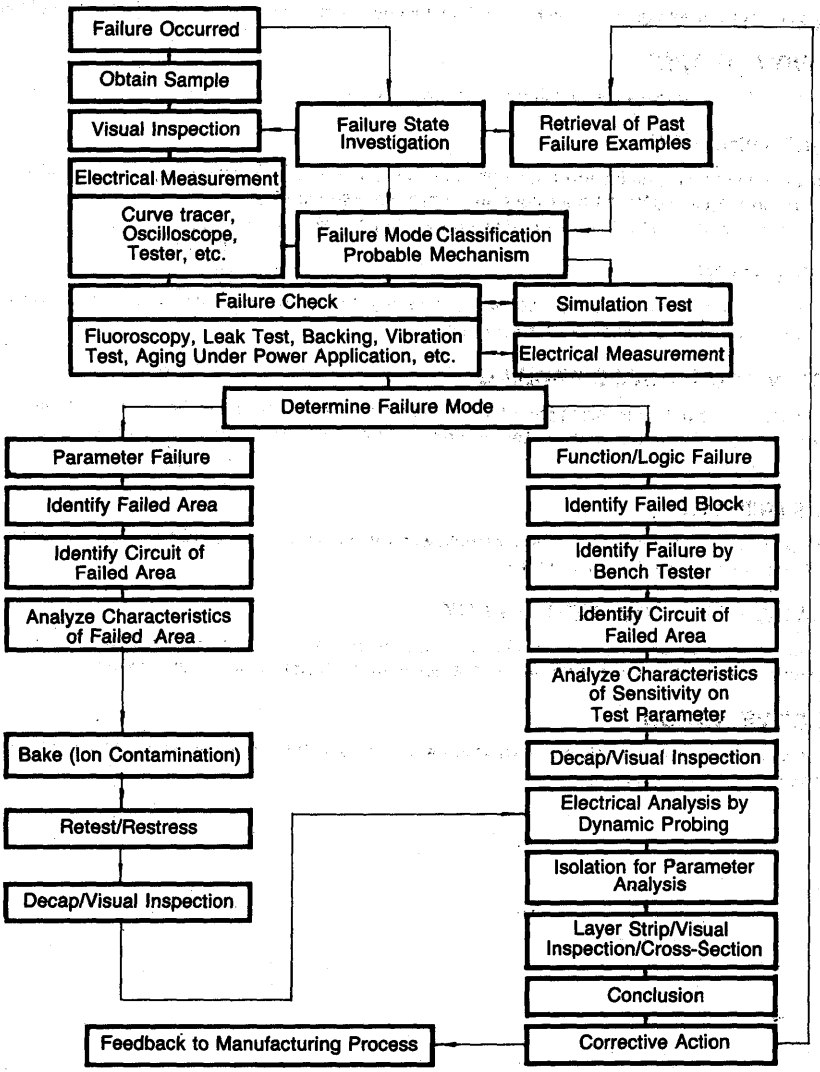
3.5 SAFETY STANDARDS

Most customers express the desire to use only products which have been manufactured with materials that meet the safety specifications of the Underwriters Laboratories. SEC has chosen to adhere to the specifications called out in the UL standard 94 by purchasing and using only those plastic materials that conform to this standard. UL 94 tests for a number of different flammability conditions that effect the plastic material used in semiconductor devices including horizontal burning, vertical burning and flame spread.

4. FAILURE ANALYSIS

4.1 PROCEDURE

A general failure analysis procedure is shown below. The method demonstrated in the flow chart applies to all rejects. However, each analysis is specific unto itself, so that a completely exhaustive analytical flow is impossible for the limits of this manual. Specific instances and examples of interest are provided later in the chapter. Also included in this section is a typical day-by-day accounting of a failure analysis in progress. A two-week turnaround is the objective, with greater than 90% of analysis lasting equal to or less than this duration. A sample analysis plan and report are attached at the conclusion of this section.



Failure Analysis Procedure Flow Chart

Applicable Comments for the above flow chart are made below.

1) DETERMINATION OF FAILURE MODE

The basic failure mode shall be determined with data from computer and bench testing. As a defect can represent various electrical failure modes, it is critical to determine the most basic failure mode. (For example, a V_{OL}/V_{OH} parameter failure may be also analyzed as a functional failure. However, it is very important to determine V_{OL}/V_{OH} as the basic failure mode.)

2) IDENTIFICATION AND ANALYSIS OF FAILED CIRCUIT AREA

Correlation shall be derived with general (macroscopic) failure phenomenon through circuit interpretation of the failed area.

3) SENSITIVITY OF TEST

Parametric value of failed sample shall be determined through adjusting DC and AC parameters, temperature range, etc.

4) ION CONTAMINATION

For a sample assumed to have an inversion phenomenon caused by ionic contamination, characteristics shall be identified by conducting a Ta = 150°C, 24 hour cure and repeating test/restress.
Contamination of a specific layer shall be determined by stripping each layer.

5) DECAPSULATION

There are 5 decap methods with respective merits and demerits. The appropriate method must be utilized on the basis of the characteristics and potential cause for each failure.

6) ISOLATION AND DYNAMIC PROBING

It is essential to isolate the probable failing part of the circuit for its electrical failure mode. Without isolation, exact detection of a failed part can not be accurately accomplished as an electrical failure mode has an influence on other parts of the circuit.

7) LAYER STRIPPING

Each layer strip should meet specification requirements with respect to time. It should never be the case that chemical attack is mistaken for causing the failure of a part.

8) GENERATION OF ACTIVATION ENERGY

Accelerated life testing requires generation of actual activation energies based upon establishing a definitive failure mode. This generation has a great effect in determining the acceleration factor of Arrehenius' model.

9) CORRECTIVE ACTION

Failure analysis is fully completed only by establishing a future plan and corrective action, which are taken to resolve a problem and prevent its recurrence.

4.2 Failure Modes and Mechanisms

1) Failure mechanisms for devices vary widely. They are caused by both front-end (wafer) and back-end (assembly) processing. To classify problems and their instigations, the table listed below is provided.

Items and Causes of Failure Modes

Item	Type of Failure	Failure Mode	Cause
Wire Bonding	Wire Disconnection	Open	Incomplete Manufacture or Misuse
	Wire Short	Short	
	Purple Plague	Open, High Resistance	
	Bond Detaching	Open, High Resistance	
	Misplaced Bonding, Loose Contact	Open, High Resistance Short	
	Improper Bond Shape Erroneous Bonding	Open, High Resistance Open, High Resistance	Incomplete Manufacture
Junction Region	Destruction by Surge	Low Breakdown Voltage, Short, Open	Incomplete Manufacture or Misuse
	Hot Spot		
Case	Lead Disconnection	Open, High Resistance	Same as above
	Lead Short	Short, High Leakage	
Seal	Incomplete Seal	Breakdown Voltage Deterioration, High Leakage	Same as above
	Enclosed High Humidity Gas		
	Contamination of Surface		
	Dust and Dirt	Short, Low Breakdown Voltage Large Leakage	
Metallization	High Current Density	Open, Short	Misuse
	Electromigration	Open, High Resistance	
	Scratch	Open, Short	Incomplete Manufacture
	Insufficient Thickness Excessive Etching	Open, High Resistance	
	Contamination, Dust and Dirt	Open, High Resistance	Incomplete Manufacture or Misuse
	Poor Wiring and Element Connection		
Chip Mounting	Chip Crack	Open, Short	Same as above
	Chip Detaching	Open, Short, High Thermal Resistance	
Oxidized Film	Pinhole, Crack	Low Breakdown Voltage, Short	Incomplete Manufacture
	Insufficiently Oxidized Film Thickness	Low Breakdown Voltage	
Surface Treatment	Channel Formation	Low Breakdown Voltage High Leakage	Same as above
	Contamination		
Mask	Insufficient Photoresist	Low Breakdown Voltage Short, Open, High Leakage	Same as above
	Mask Misalignment		
Material and Diffusion	Improper Impurity Density	Same as above	Same as above

2) Standard product reliability tests can naturally generate failures. Here, in this section, a table is given which lists tests and their associated rejects. Each test has a specific purpose, and if there exists a particular product weakness, a given test will expose it. In this manner, by knowing a test and it's function, a clear determination can be made as to the relevance of a failure for that particular test.

Reliability Tests and Associated Failure Modes

	Failure Cause	Diffusion	Oxide	Metalization	Wire Bonding	Package Environment	Package Seal	Lead Fatigue	Solderability	Mark	Die bonding
Item	Test Condition	•Contamination •Crystal Defect •Photoresist Reject	•Contamination •Pin Hole •Crack •Thickness Unstable	•Conpos. •Scratch •Void •Open	•Interface •Corrosion •Misbonding •Wire Open •Chemical Interface	•Conductive ions •Inadequate •Environments	•Sealing Reject	•Conpos.	•Marking	•Themal Reject	Resistance Reject •Crack •Chip Position Reject
T/C	-65°C→150°C 200 Cycles		0	0	0		0				0
T/S	-65°C→125°C 200 Cycles		0	0	0		0				0
Moisture Resistance	90-98%R.H./65°C3HRS 80-98%R.H./25°C8HRS 90-98%R.H./65°C3HRS 10 Cycles		0	0	0	0	0				
Vibration Fatigue	20G-3 Axis Orientation f=20 to 2000 cpe for 4 min. 4 cycles				0	0					0
Constant Acceleration	Pulse Duration: 0.1-1m sec Shock pulse: 0.5-3Kg				0						0
Mechanical Shock	1500g, 0.5ns Each Direction of X, Y and Z Axis				0						0
Lead Integrity	W=227g 90°C 3 times						0				
Marking	Isoprophylalcohol									0	
Solderability	Ta=230° 5 Sec. Once With Flux								0		
Salt Spray	Ta=35°C, 5% NaCl				0				0		
OPL	Individual Spec	0	0	0	0	0					0
IOPL	Individual Spec	0	0	0	0	0					0
HTRB	Individual Spec	0	0	0	0	0					0
HTS	Individual Spec		0		0	0			0		
WHTS	80°C, 90% RH 85°C, 85% RH		0	0			0	0	0		
WHTRB	85°C, 85% RH Bias	0	0	0	0	0	0	0	0		0

3) An anomalous manufacturing step can manifest itself in many ways with respect to product reliability. The chart below depicts process steps, the types of rejects they can generate, and the way to defect such failures. Of course, there are numerous QC and Production checks along all stages of the manufacturing process. However, a semiconductor product typically involves so many operations it's nearly impossible to detect all potential reliability hazards. Thus, there are final electrical and visual tests, reliability tests, and statistical analyses which are run prior to product releasal. The chart below speaks to the electrical, visual, and reliability tests.

Failure Mechanisms of Integrated Circuits

Process Step Affecting Reliability	Failure Mechanism	Failure Mode	Failure Detection Method
Wafer Fabrication	Dislocation and Stacking Fault	Degradation of Function Characteristics	Electrical Test Operation Life
	Non-Uniform Resistivity	Unpredictable Characteristic Values	Electrical Test
	Surface Abnormalities	Improper Electrical Characteristics, Short and Open	Electrical Test Operation Test
	Cracks, Chips, Scratches (Usually Caused During Handling)	Open and Short	Electrical Test Visual Inspection (Before Seal) Temperature Cycling
	Contamination	Degradation of Junction Characteristics	Visual Inspection (Before Seal), Temperature Cycling, High Temperature Storage, Reverse Bias
Passivation	Cracks and Pin Holes	Shorts, Low Breakdown Voltage	Temperature Cycling High Temperature Storage High-Voltage Test, Operation Life Visual Inspection (Before Seal)
	Non-Uniformity of Film Thickness	Low Breakdown Voltage Increase of Leakage Current in Oxide Film	Same as Above
Mask	Scratch, Crack, Scar of Photo Mask	Open, Short	Visual Inspection (Before Seal), Electrical Test
	Misalignment	Open, Short	Same as Above
	Abnormality of Photo-Resist Pattern (Line-Width, Space, Pin Hole)	Degradation of Characteristics Due to Parameter Drift Open, Short	Same as Above
Etching	Improper Elimination of Oxide Film	Open, Short, Intermittent Failure	Visual Inspection (Before Seal) Electrical Test Operation Life
	Under-Cut	Short or Open in Metallization	Visual Inspection (Before Seal) Electrical Test

Failure Mechanisms of Integrated Circuits (Continued)

Process Step Affecting Reliability	Failure Mechanism	Failure Mode	Failure Detection Method
Etching	Spotting (Smear) Inhomogeneous Etching	Latent Short	Visual Inspection (Before Seal) Temperature Cycle, High Temperature Storage Operation Life
	Contamination (Photo Resist, Residue of Chemical Substance)	Low Breakdown Voltage Increase of Leak Current	Same as Above Reverse Bias
Diffusion	Improper Control of Doping Profile	Performance Degradation Caused by Instability and Fault	High Temperature Storage Temperature Cycling Operation Life Electrical Test
Metallization	Scratched and Smeared Metallization (Caused During Handling)	Open and Short	Visual Inspection (Before Seal) Temperature Cycling Operation Life
	Thin Metallization Due to Insufficient Deposition or Oxide Film Step	Open or High Impedance Internal Connection	Electrical Test Operation Life Temperature Cycle
	Oxid Film Contamination Material Incompatibility	Open Metallization Caused by Poor Adhesion	High Temperature Storage Temperature Cycling Operation Life Test
	Corrosion (Residue of Chemical Substance)	Open Metallization	Visual Inspection (Before Seal), High Temperature Storage Temperature Cycle, Operation Life
	Displacement Contaminated Contact	High Contact Resistance, Open	Visual Inspection (Before Seal), Electrical Test, High Temperature Storage Temperature Cycle, Operation Life
	Improper Temperature and Period for Metallization	Peeled Metallization Poor Adhesion Short	Electrical Test High Temperature Storage Temperature Cycle Operation Life
Die Separation	Cracks and Chips Caused by Improper Dicing	Open	Visual Inspection (Before Seal) Temperature Cycling Thermal Shock Vibration Shock

Failure Mechanisms of Integrated Circuits (Continued)

Process Step Affecting Reliability	Failure Mechanism	Failure Mode	Failure Detection Method
Die Bonding	Void Between Header and Die	Degradation Due to Overheating	Radiography, Operation Life Constant Acceleration Shock, Vibration
	Over-Spreading of Eutectic Solder	Short, Intermittent Short	Visual Inspection (Before Seal), Radiography, Vibration Shock
	Poor Bonding of Die to Header	Die Crack and Lifting	Visual Inspection (Before Sealing), Constant Acceleration, Shock, Vibration
	Mismatching of Materials	Crack or Peeling of Die	Temperature Cycling High Temperature Storage Constant Acceleration
Wire Bonding	Poor Bonding Strength	Open Wire, Open, Lifting Vibration Shock	Constant Acceleration
	Mismatched Material and Contaminated Bonding Pad	Lead Bond Peeling	Temperature Cycling High Temperature Storage Constant Acceleration Shock, Vibration
	Formation of Intermetallic Plague	Open Bonding	High temperature storage, Temperature Cycling. Constant Acceleration Shock, Vibration
	Insufficient Bonding Area or Spacing	Open Bonding Short	Operation Life Test, Constant Acceleration, Shock Vibration, Visual Inspection (Before Seal)
	Improper Bonding Arrangement	Open, Short	Visual Inspection (Before Seal) Electrical Test
	Die Cracks or Chips	Open, Shock	Visual Inspection (Before Seal) High Temperature Storage Temperature Cycling Constant Acceleration, Shock Vibration
	Excessive Loop or Sag in Wire	Short to the Case, Substrate or other Parts of the Leads	Visual Inspection (Before Seal), Radiography, Constant Acceleration, Vibration
	Crack, Scratch, or Scar on Lead	Wire Disconnection Causing Open, Short	Visual Inspection (Before Seal), Constant Acceleration, Shock Vibration

Failure Mechanisms of Integrated Circuits (Continued)

Process Step Affecting Reliability	Failure Mechanism	Failure Mode	Failure Detection Method
	Insufficent Elimination of Tail Wire	Short, Intermittent Short	Same as Above Radiography
Sealing	Incomplete Hermetic Seal	Performance Degradation, Shorts and Opens Caused by Chemical Corrosion and Moisture	Fine Leak, Gross Leak
	Bad Atmosphere in Package	Performance Degradation Due to Inversion Layer Channeling	Operation Life Reverse Bias, High Temp. Storage, Temperature Cycling
	Bending or Breaking of the External Lead	Open	Visual Inspection, Lead Fatique
	Crack or Void in Seal Glass	Short or Open in Metallization Due to Leak	Seal, Electrical Test High Temperature Storage Temperature Cycling High Voltage Test
	Migration on Seal between Outer Lead and Metal Case	Intermittent Short	Low Voltage Test
	Electro-Conducting Particles Floating in Package	Same as Above	Constant Acceleration, Vibration Radiography
	Mismarking	Inoperable	Electrical Test

4) Equipment

A listing of important equipment used for failure analysis is shown below in tabular from, SEC's committment to comprehensive analysis of all relevant rejects necessarily implies a usefulness for key analytical instruments. Constant efforts are made to both use and modify equipment to meet specialized investigations. However, only standard equipment, not a listing of hybrids (for confidential development purposes), is listed below.

Equipment for failure analysis

Category	Item	Application
Visual	1. Stereo Microscope	Use for visual inspection
	2. SEM (Scanning Electron Microscope)	Use to inspect the surface or cross-section of a device at high magnification. Through voltage contrast techniques, it is possible to analyze voltage levels while the device is operating
	3. Infrared Microscope	Using the infrared radiation emitted by a functioning device, a thermal map can be produced.
	4. X-Ray	Use to inspect the bonding wire of encapsulated devices.
	5. Metallugical Microscope	Inspect interconnects, contacts, bonds
	6. Radiographic Scope	Inspect bond wires, die attach

Equipment for failure analysis (Continued)

Category	Item	Application
Elemental Analysis	1. Auger Electron Spectrometer (AES)	Used to detect and analyze contamination on the surface of a die
	2. EDX Spectrometer	Used with SEM to analyze elements present in a device. This is done by measuring the energy distribution of X-rays produced by the interaction of primary electrons and the sample.
	3. Differential Interference Microscope	Used for elemental analysis
	4. Electron Probe Micro Analyzer (EPMA)	Used for current analysis
	5. Ion Micro Mass Analyzer (IMMA)	Spectral analysis of chemical constituents
	6. Surface Eveness Micrometer	Measures planarity
	7. Differential Scanning Calorimeter (DSC)	Permits the analysis of glasses and polymers-especially encapsulation resins-through the measurement of reaction heat
	8. Thermo Gravimetric Analyser	Used to determine the thermal stability of polymers and glasses by measuring variations in mass with temperature.
	9. Plasma Etcher	Used to open devices encapsulated in epoxy resins, to remove silicon nitride, and to remove thin oxide films
	10. Transmission Electron Microscope (TEM)	Used for elemental analysis and high resolution surface on spectron
	11. Surface Tunneling Microscope (STM)	Used for elemental analysis
	12. Electron Spectrometry for Chemical Analysis (ESCA)	Used for elemental analysis
	13. Secondary Ion Mass Spectroscope	Used for elemental analysis
Decapsulation System	1. Grinding Machines 2. Angle Lapping 3. Evaporation 4. Diamond Cutter (Cross Section Cutter) 5. Molding System 6. Jet-Etching System 7. Etching Solution 8. Hot Plates 9. Ventilation Hoods	Used to decapsulate devices, to cut the cross section of die, to remove a surface layer.

Equipment for failure analysis (Continued)

Category	Item	Application
Electrical Test	1. Curve Tracer 2. TR, IC, MOS Tester 3. ESD Simulator 4. LCR Meter 5. DC-Analyzer 6. Noise Tester 7. Logic State Analyzer 8. Manipulator Probe Ssytem 9. Electron Beam Tester 10. Hot Electron Analyzer 11. I.R Scope	Used to measure electrical characteristic of devices, to establish the cause of failure.
Stress Test	1. Temperature Probe System 2. Constant Temperature Oven 3. Ovenn for Oper Life Test 4. Humidity Oven 5. Vibration System	Used to stress or cure the failed devices to identify a failure mechanism. This is a very important tool for analyzing degradation phenomena and intermittent failures.

Methods and Equipment for Failure Analysis

Item	Contents of Inspection	Equipment for Analysis
External Visual Check	• Condition of Lead, Plating, Soldering, Welding Area • Mark, Date Code • Package damage • Solderability • Sealing	Stereo-Optical-Scope x 40 Optical Microscope x 100 Helium Leak Detector Gross Leak Detector (Using Fluorocarbon)
Electrical Test	• DC Parameter, AC Parameter Test • Function Test • Margin Test of Voltage and Temp. • Diode Characteristics between Each Pin • Disconnection, Short Circuit and / or Electrical Characteristic detected by the above Inspection	IC Tester Curve Tracer (HP4145) Oscilloscope DC Power Supply Oscillator (Sine Wave Pulse) Heat-Gun, Cooling Gas Spray Thermo-Spot
Radiography	• Internal Structure of Device is Checked Non-Destructively	Soft X-Ray
Decapping	• Internal Structure is observed after decapping	Metal Cutting Scissors, Nippers Cap opener, plastic etcher, Hot plate, Drill, HNO_3
Internal Visual Check	• Detection of Defective Spot on the Chip Surface • Detection of Discrepancy of Internal Connection (Metallization, Wire Bond -ing, Etc.) • Electrical Characteristics are Checked by Mechanical Prober • Detection of Hot Spot • Existence of Foreign Material	Optical Microscope Micro-Prober SEM Laser Cutter Infrared Micro Scanner Thermal Plotter Infrared Microscope
Internal Structure Analysis	• Cross Sectional Analysis of Chips to Observe Diffusion Layer of Oxide Film • Analysis of Metallic Elements • Removing of Over-Coating Glass and Aluminum Metallization	Optical Microscope SEM, MAX, AES, SAM, IMA Spectrometer Micro-Prober
Simulation Test	• Operational Test on Actual Equipment	Actual Electronic Equipment

4.3 FAILURE MODE EFFECT ANALYSIS (FMEA)

Failure Mode Effect Analysis is a method used for checking if measures are taken against every possible failure in the design, the manufacturing process, the operating method, etc. For this analysis, factors such as design, manufacturing process, packaging, and operating method are divided into small units, and its functions are clearly defined. All possible failure modes are listed for each item, its effect on the product and the cause of each failure is examined. Each item is then evaluated to clarify the corrective actionto be taken.
Table shows an example of FMEA in the manufacturing process of plastic encapsulated MOS LSI. The incident column pertaining to the Evaluation Points show the failure rate; Effectiveness column shows the impact of the effect by the failure of the product, device, or system; and Detectability shows the rate of detection of the failure. These are individually graded on the basis of ten points. The result is then evaluated by multiplying the points. The larger value indicates the importance of the item. A counterplan for each item is then specified and action taken.

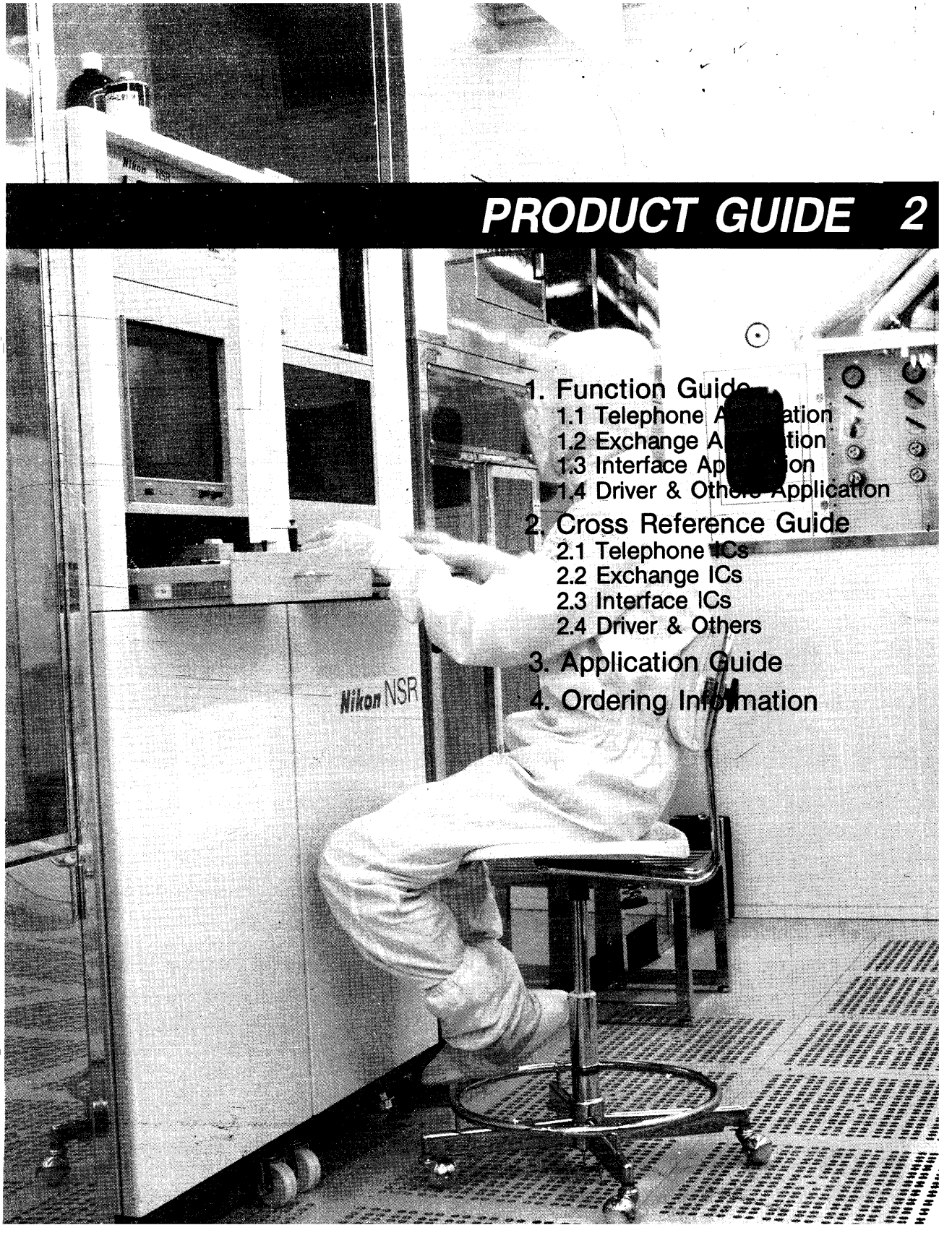
Manufacturing Process FMEA Example (Plastic Encapsulated Products)

Process Name (Process Function)	Failure Mode	Failure Effect	Failure Cause	Counterplan
Al metallization	Improper thickness Lack of Al wiring Breakage defect	Electromigration open circuit	Operator's mis-handling, dirt/foreign matter attachment, poor adjustment of equipment	Improvement and adjustment of written working process, dust control of clean room, SEM test in the process
Glassivation	Lack of glassivation film, failure film thickness	Increased leak current, improper operation	Dirt/foreign matter attachment, operator's mishandling	Dust control of clean room, improvement and adjustment of written working process
Visual Inspection	Scratch, die crack, dirt, spot, residual resist	Open circuit, increased junction leak current	Mishandling of wafer, Misclearning of water	Improvement and adjustment of written working process
Assembly Process Die Selection	Die crack	Increased junction leak current, improper operation	Poor adjustment of equipment, operator's mishandling	Corrective action to device control operator, improvement and adjustment of written working process
Die Bonding	Die crack Die floating	Open circuit, increased junction leak current, improper operation	Operator's mishandling temperature too low	Corrective action to device control operator, improvement and adjustment of written working process, visual inspection
Wire Bonding	Open bonding, improper bonding position, shorted bonding wire	Open circuit, short circuit	Poor bonding strength, operator's mishandling, poor adjustment of equipment, looped bonding wire, shape defact	Improvement and adjustment of written working process, corrective action to device control operator, visual inspection

Manufacturing Process FMEA Example (Plastic Encapsulated Products) (Continued)

Process Name (Process Function)	Failure Mode	Failure Effect	Failure Cause	Counterplan
Sealing (Resin)	Open bonding wire, shorted bonding wire, package crack, corrosion	Open circuit, short circuit, defective appearance	Poor adjustment of equipment, insufficient cure	Ditto
Lead Surface Treatment (plating)	Poor metal-plating thickness, dirt	Poor soldering, poor contact	Operator's mishandling poor adjustment of equipment, insufficient cleaning	Adjustment of written working process, corrective action to control operator
Lead Formation	Abnormal shape, broken lead	Failure inserting in the printed substrate poor operation	Operator's mishandling poor adjustment of equipment	Ditto
Marking	Marking error illegible marking	Operating destruction	Operator's mishandling insufficient cure	Improvement and adjustment of written working process

PRODUCT GUIDE 2



1. FUNCTION GUIDE

1.1 Telephone Application Function

Application	Type	Package	Circuit Function
Tone Ringer	KA2410 KA2411	8 DIP	Adjustable warbling and 2 frequency tone External triggering or ringer disable (KA2410) Adjustable supply initiating current (KA2411) Built-in hysteresis
Tone Ringer with Bridge Rectifier	KA2418/28	8 DIP	Protect against over voltage Low current consumption Allow the parallel operation of 4 devices Built-in hysteresis External component's are minimized High output voltage
DTMF Dialer	KS5808	16 DIP	Direct telephone line operation Standard 2 of 8 key board use Tone output: Bipolar output Mute output: N-CH open drain
	KS5809	16 DIP	Low power dissipation Single contact key board use Tone output: Bipolar output Mute output: N-CH open drain
	KS5810	16 DIP	Low power dissipation Single contact key board use 16 digit redial (Column 4 keys) Tone output: Bipolar output Mute output: N-CH open drain
	KS5811	16 DIP	Low power dissipation Standard 2 of 8 key board use 16 digit redial (# key) Tone output: Bipolar output Mute output: N-CH open drain
	KA2413	16 DIP	Wide operating line voltage and current range Short start up time External components are minimized Internal protection of all inputs
Pulse Dialer with Redial	KS5805A/B	18 DIP	KS5805A: Pin 2; V_{ref} KS5805B: Pin 2; Tone output RC oscillator used as frequency reference $\overline{DP}$ out, 17 digit redial
	KS58C/D05	18 DIP	KS58C05: Pin 2; V_{ref} KS58D05: Pin 2; Tone output RC oscillator used as frequency reference $\overline{DP}$ output, 32 digit redial

1.1 Telephone Application Function (Continued)

Application	Type	Package	Circuit Function
Pulse Dialer with Redial	KS58E05	16 DIP	$\overline{DP}$ output RC oscillator used as frequency reference 32 digit redial
	†KS5851/2	18 DIP	KS5851: Pin 2; V_{ref} KS5852: Pin 2; Tone output RC oscillator used as frequency reference $\overline{DP}$ output, 32 digit redial High quality Si-Gate CMOS process
	†KS5853	16 DIP	$\overline{DP}$ output RC oscillator used as frequency reference 32 digit redial High quality Si-Gate CMOS process
DTMF/Pulse Switchable Dialer	KS58A/B/C/D19 KS58A/B/C/D20	22 DIP/22 SDIP 18 DIP/20 SOP	Tone/pulse switchable dialing, touch key or slide switch 32 digit redialing & PABX auto-pause time Make/break ratio pin selectable
DTMF/Pulse Switchable with 10 No Memory	KS5822	22 DIP/22 SDIP	10 No x 16 digit memory including a redial memory Including PABX auto pause time 10 pps/20 pps pin selectable Make/Break pin selectable On/Off hook memory
	KS58A/B/C/D23	18 DIP/20 SOP	10 No x 16 digit memory including a redial memory Including PABX auto pause time Make/Break pin selectable
DTMF/Pulse Switchable with 20 No. Memory	†KS58531-42	28 DIP/28 SOP	20 Nox16digit memory including a 32 digit redial memory Including PABX auto pause time Make/break ratio pin selectable Repertory dialing is accessed by direct key or indirect key
Speech Network	KA2412A	14 DIP	Transmit/Receiver amplifier Side tone control On chip regulator
Low Voltage Speech Network with Dialer Interface	KA2425A/B	18 DIP	Low Voltage Operation (1.5V) Tx, Rx & side tone gain set by external resistor Loop length equalization for Tx, Rx & sidetone Provides regulated voltage for dialer DTMF level adjustable with a single resistor A: Mute active low B: Mute active high
Speech Network with Dialer Interface	†KA8500A/B †KA8501A/B ††KA8502A/B	16 DIP	Adjusts sending and receiving attenuation length Provides regulated voltage for dialer Linear interface for DTMF A: Mute active high B: Mute active low

† : New Product
†† : Under Development

1.1 Telephone Application Function (Continued)

Application	Type	Package	Circuit Function
Low Voltage Audio Amp	†KA8602	8 DIP 8 SOP 9 SIP	Wide supply voltage (2~16V) Easy gain control Medium output power P_O=250mW at V_{CC}=6V, R_L=32Ω, THD=10% Minimum external parts Load impedance range (8Ω~100Ω) Low distortion Mute function (I_{CC}=65μA: Typ)
DTMF Receiver	KT3170	18 DIP	Full DTMF Receiver Provides DTMF high and low group filtering Dial tone suppression Adjustable acquisition and release times Integrated bandsplit filter and digital decoder functions High quality and performance Single +5 Volt power supply
Cordlessphone Channel Select	††KS8800/1	18 DIP	15 channel/10 channel selector for cordlessphone 15 channel: KS8800 10 channel: KS8801 Include oscillation circuit with external X-tal (10.24MHz) 5KHz/4.4KHz output for guard tone Standby function for saving power
Tone Decoder	LM567C/L	8 DIP †8 SOP	Touch tone decoding Sequential tone decoding Communication paging High stable center frequency LM567L: Micropower (4mW at 5V) dissipation
FM IF Amplifier	MC3361	16 DIP †16 SOP	Small current dissipation (Typ. 3.5mA: V_{CC}=4.0V) Excellent input sensitivity Communication paging Used to cordless telephone parts required Work from 1.8V to 7.0V

† : New Product
†† : Under Development

1.2 Exchange Application Function

Application	Type	Package	Circuit Function
Codec	KT5116 †KT8520 ††KT8521	16 CERDIP 24 CERDIP 22 CERDIP	μ-Law: KT5116 μ-Law: KT8520 A-Law: KT8521 ±5V operation Low power consumption Synchronous or asynchronous operation
Codec Filter	KT3040/A	16 CERDIP	Exceeds all D3/D4 and CCITT spec. ±5V operation Low power consumption 20dB gain adjust range Sin X/X correction in receive filter TTL and CMOS compatible logic
Combo Codec	†KT8554 †KT8557 †KT8564 ††KT8567	16 CERDIP ††16 DIP 20 CERDIP ††20 DIP	Exceeds all D3/D4 and CCITT spec. Complete CODEC and filtering system including ±5V operation Low power consumption TTL and CMOS compatible logic Receive push-pull power amp (KT8564/7)
TSAC	KT8555	20 CERDIP	Controls up to 8 COMBO CODEC/Filters Low power consumption Single 5V operation Up to 32 time slots per frame
4×4 Crosspoint Switch	††KT8592	16 DIP	4×4 matrix-array with control memory Low on resistance $2V_{p\text{-}p}$ analog signal capability Less than 1% total distortion at 0dBm
12×8 Crosspoint Switch	††KT8593	40 DIP	12×8 matrix-array with control memory Low on resistance $2V_{p\text{-}p}$ analog signal capability Less than 1% total distortion at 0dBm

† : New Product
†† : Under Development

1.3 Interface Application Function

Application	Type	Package	Circuit Function
Line Driver	MC1488 ††KS5788	14 DIP 14 SOP	Conformance EIA standard No. RS-232C & V28 (CCITT) Quad line driver Interface between data terminal equipment (DTE) and data communication equipment (DCE) Current limited output: ± 10mA typ. Power-off source impedance 300 ohms min. Compatible with DTL and TTL, HCTLS families Flexible operating supply range KS5788: Low power CMOS version
Line Receiver	MC1489/A ††KS5789A	14 DIP 14 SOP	Conformance EIA standard No. RS-232C & V28 (CCITT) Quad line receiver Interface between data terminal equipment (DTE) and data communication equipment (DCE) input signal range: ± 30 volts Input threshold hysteresis built in Response control a) Logic threshold shifting b) Input noise filtering KS5789A: Low Power CMOS version
Line Transceiver	KA2654	8 DIP	Conformance EIA Standard No. RS-232C & V28 (CCITT) One Driver & One Receiver on chip Wide supply voltage (± 4.5V- ± 15V) Including reference regulator Response control provides TTL compatible

†† : Under Development

1.4 Driver and Other Application Function

Application	Type	Package	Circuit Function
Peripheral Driver Array	KA2655/6/7/8/9	16 DIP 16 SOP	Including 7 NPN darlington-connected transistors These arrays are well suited for driving lamps, relays, or printer hammers in a variety of industrial and consumer applications. High breakdown voltage and internal suppression diodes insure freedom from problems associated with inductive loads
Fluorescent Display Driver	KA2651	18 DIP	Consisting of 8 NPN darlington output stages and associated common-emitter input stages Digit or segment drivers Low input current, internal output pull-down resistor High output breakdown voltage Single or split supply operation
8-Channel Source Driver	KA2580A	18 DIP	TTL, CMOS, PMOS, NMOS compatible High output current ratings Internal transient suppression Efficient input/output pin structure Drive telephone relays, incandescent lamps, and LEDS
	KA2588A	20 DIP	KA2588A: Separated logic and driver supply line
Universal Asynchronous Receiver and Transmitter (UART)	KS5824 KS5812	24 DIP 40 DIP	The data formatting and control to interface serial asynchronous data communications between main system and subsystems. Low power, high speed CMOS process Serial/parallel conversion of data 8 and 9 bit transmission Programmable control register Optional ÷1, ÷16, and ÷64 clock modes Peripheral/modem control functions Double buffered Included 4 UART in one chip (KS5812)
8-Bit Latch & Driver	†KT8518	16 DIP	8-bit addressable latched driver

† New Product
†† Under Development

2. CROSS REFERENCE GUIDE

2.1 Telephone ICs

A. Dialer

Application	SAMSUNG	MOSTEK	AMI	UMC	SHARP	Others
Pulse Dialer	KS5805A KS5805B KS58C05 KS58D51 KS58E05 †KS5851 †KS5852 †KS5853	*MK50992 *MK50993 MK50981 MK50982 MK50991/2 MK50981 MK50982 MK50991/2	S2560A/B	*T40992 *T40993 UM9151 UM9151 UM9151-3 UM9151 UM9151 UM9151-3	*LR40992 *LR40993	
DTMF Dialer	KS5808 KS5809 KS5810 KS5811 KA2413	*MK5089 MK5087 MK5380	*S25089	*UM95089 UM95087 UM9559	*LR4089 LR4087	*SBA5089 SBA5091 SBA5099 *PBD3535
DTMF/Pulse Switchable with Redial	KS58A/B/C/D19 KS58A/B/C/D20	MK5370		*UM91230 *UM91210	LR48081 LR48082	*S7230A/B S7235 LC7360
DTMF/Pulse Switchable with 10 No. Memory	KS5822 KS5823	MK5375/6		*UM91261 *UM91260	LR4803	PCD3315 HM9110B/C
DTMF/Pulse Switchable with 20 No. Memory	†KS58531-42			UM91271 UM91270		S7241

B. Tone Ringer

Application	SAMSUNG	MOTOROLA	SGS	MITEL	CHERRY	Others
Tone Ringer	KA2410 KA2411			*ML8204 *ML8205	*CS8204 *CS8205	*TA31001 *TA31002
1 Chip Tone Ringer	KA2418 †KA2428	MC34012 MC34017	*LS1240 LS3240			Included Bridge Diode

C. Speech Network

Application	SAMSUNG	SGS	RIFA	ITT	ERSO	Others
Subset Amplifier	KA2412A	*LS285/A	PBL3726	TEA1045	*CIC9185	
Speech Network with Dialer Interface	KA2425A KA2425B †KA8500A/B †KA8501A/B ††KA8502A/B	*LS156 *LS256 *LS356	PBL3781			U4053/7 U4055/6 TP5700
Audio Amp	†KA8602					MC34119

† : New Product
†† : Under Development
* : Direct Replacement

D. Cordlessphone Channel Select

Application	SAMSUNG	MOTOROLA	SANYO	Others
Channel Select	††KS8800/1	MC145166/8	LC7150/1	

E. Tone Decoder

Application	SAMSUNG	NATIONAL	SHARP	SIGNETICS	Others
Tone Decoder	LM567C	*LM567	*IR3N05	*NE567	*XR567 (EXAR)
	LM567L				*XRL567 (EXAR)

F. FM IF Amplifier

Application	SAMSUNG	MOTOROLA	SHARP	SPRAGUE	Others
FM IF Amplifier	MC3361	*MC3361	IR3N06	ULN3859	*LM3361

G. DTMF Receiver

Application	SAMSUNG	MITEL	GTE	Others
DTMF Receiver	KT3170	*MT8870	*G8870	

2.2 Exchange ICs

Application	SAMSUNG	N.S	FAIRCHILD	SGS	INTEL	MOTOROLA	THOMSON
μ-Law CODEC	KT5116	*TP5116	*μA5116	*M5116	2910		
CODEC FILTER	KT3040	*TP3040	*μA5912	*M5912	*2912		*ETC5040
μ-Law COMBO CODEC	†KT8564	*TP3064			2913	MC14400-5	*ETC5064
μ-Law COMBO CODEC	†KT8554	*TP3054	*μA3054		*2916		*ETC5054
A-Law COMBO CODEC	††KT8567	*TP3067					*ETC5067
A-Law COMBO CODEC	†KT8557	*TP3057	*μA3057		*2917		*ETC5057
μ-Law CODEC	†KT8520	*TP3020	μA5151		*2910		
A-Law CODEC	††KT8521	*TP3021			*2911		
TSAC	KT8555	*TP3155					
4×4 Crosspoint Switch	††KT8592					*MC142100	*CD22100
12×8 Crosspoint Switch	††KT8593			*M093			

† : New Product
†† : Under Development
* : Direct Replacement

2.3 Interface ICs

Application		SAMSUNG	MOTOROLA	TI	N/S	FAIRCHILD	SIGNETICS
RS-232C	Line Driver	††KS5788			*DS14C88		
		MC1488	*MC1488	*SN75188	*DS1488	*μA1488	*MC1488
	Line Receiver	MC1489	*MC1489	*SN75189	*DS1489	*μA1489	*MC1489
		MC1489A	*MC1489A	*SN75189A	*DS1489A	*μA1489A	*MC1489A
		††KS5789A			*DS14C89A		
	Transceiver	KA2654		*SN751701			

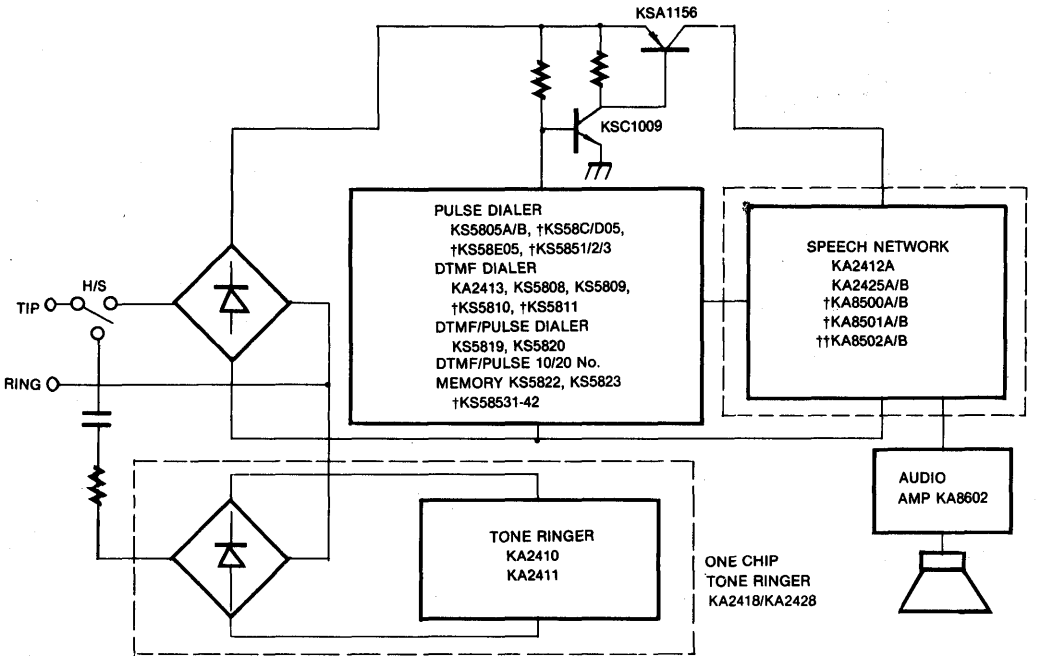
2.4 Driver & Others

Application	SAMSUNG	SPRAGUE	EXAR	MOTOROLA	TI	Others
8ch Source Driver	KA2580A	*UDN2580A				
	KA2588A	*UDN2588A				
Flouscent Display Driver	KA2651	*UDN6118	*XR6118			
Peripheral Driver Array	KA2655	*ULN2001		*MC1411	SN75476	
	KA2656	*ULN2002		*MC1412	SN75477	
	KA2657	*ULN2003		*MC1413	SN75478	
	KA2658	*ULN2004		*MC1416		
	KA2659	*ULN2005				
Single UART	KS5824			*MC6850		*HD6350
Quad UART	KS5812					
8-Bit Latch & Driver	†KT8518					

† New Product
†† Under Development
* Direct Replacement

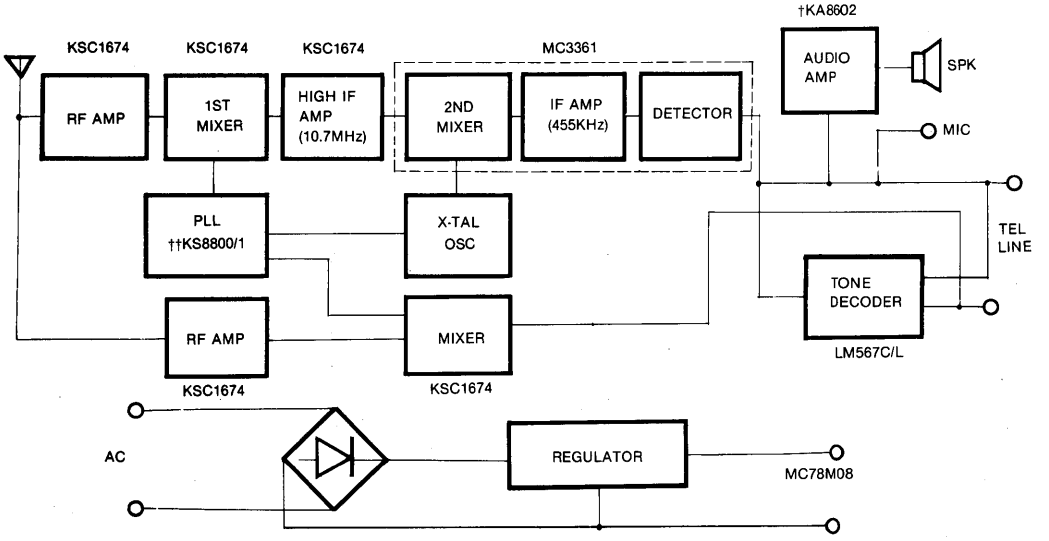
3. APPLICATION GUIDE

3.1 Telephone

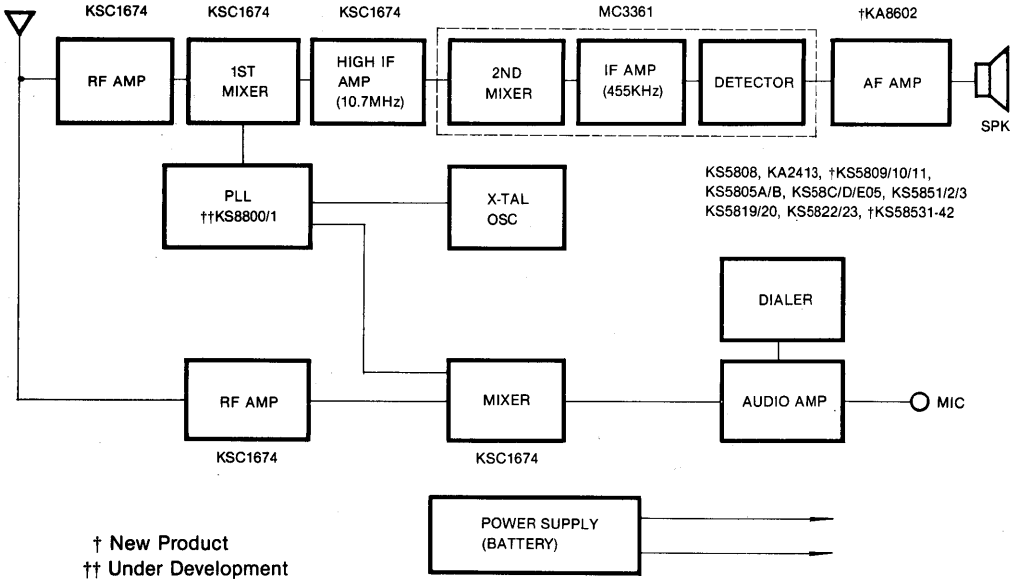


† New Product
†† Under Development

3.2-1 Cordless Phone (Base Unit)

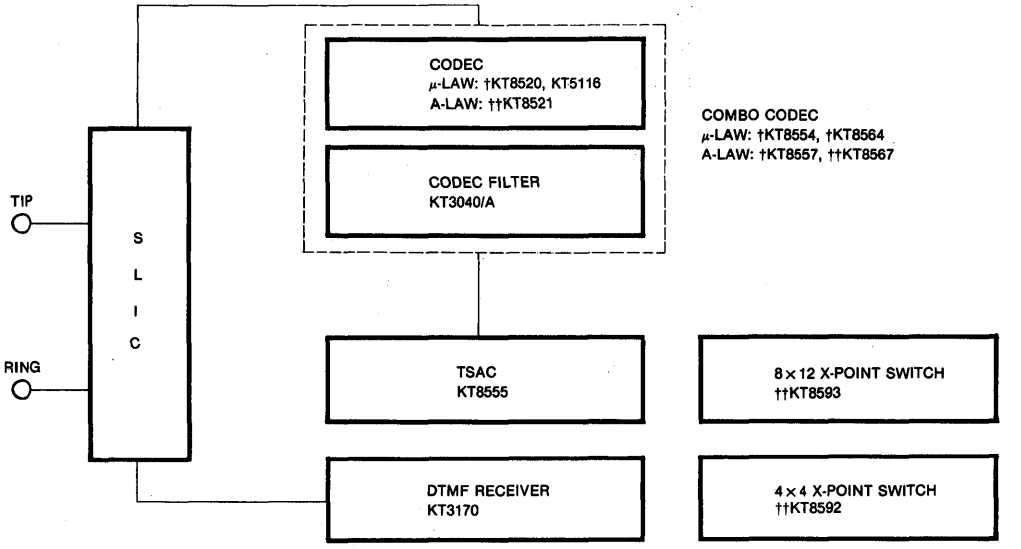


3.2-2 Cordless Phone (Handset Unit)

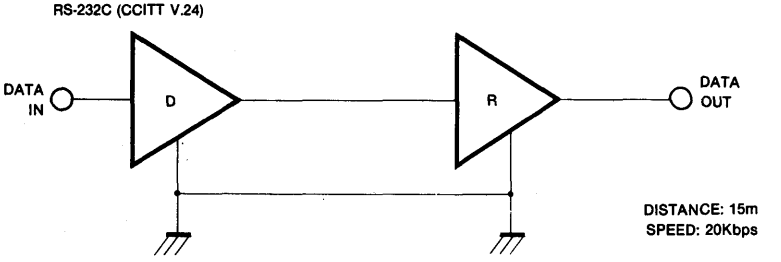


† New Product
†† Under Development

3.3 Exchange



3.4 Interface



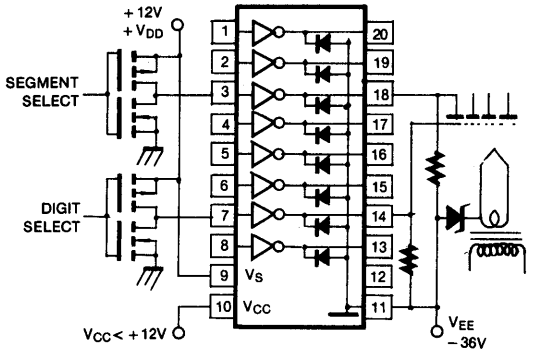
Drivers	Receivers	Transceivers
Quad	Quad	Single
MC1488 ††KS5788	MC1489 MC1489A ††KS5789A	KA2654

† New Product
†† Under Development

3.5 Driver

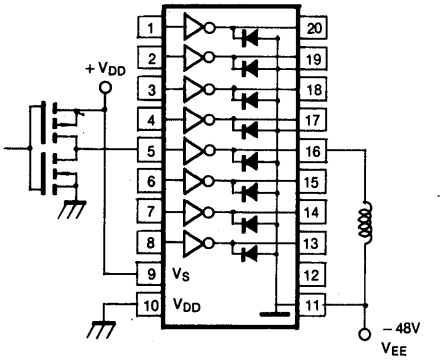
Typical Applications

KA2588A



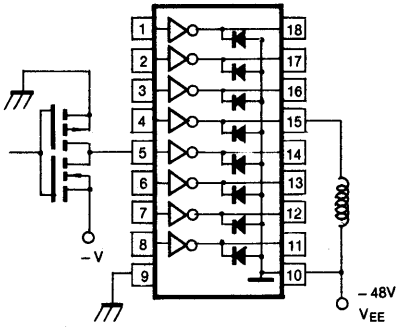
VACUUM FLUORESCENT DISPLAY DRIVER (SPLIT SUPPLY)

KA2588A



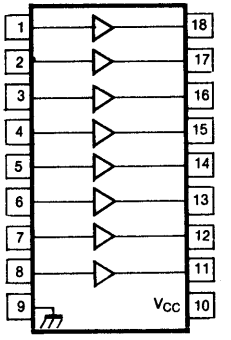
TELECOMMUNICATION RELAY DRIVER (POSITIVE LOGIC)

KA2580A

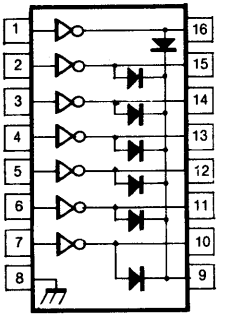


TELECOMMUNICATION RELAY DRIVER (NEGATIVE LOGIC)

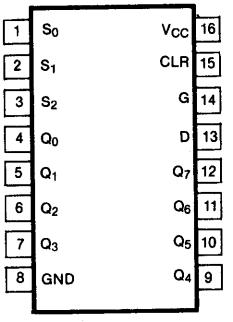
K2651



KA2655/6/7/8/9

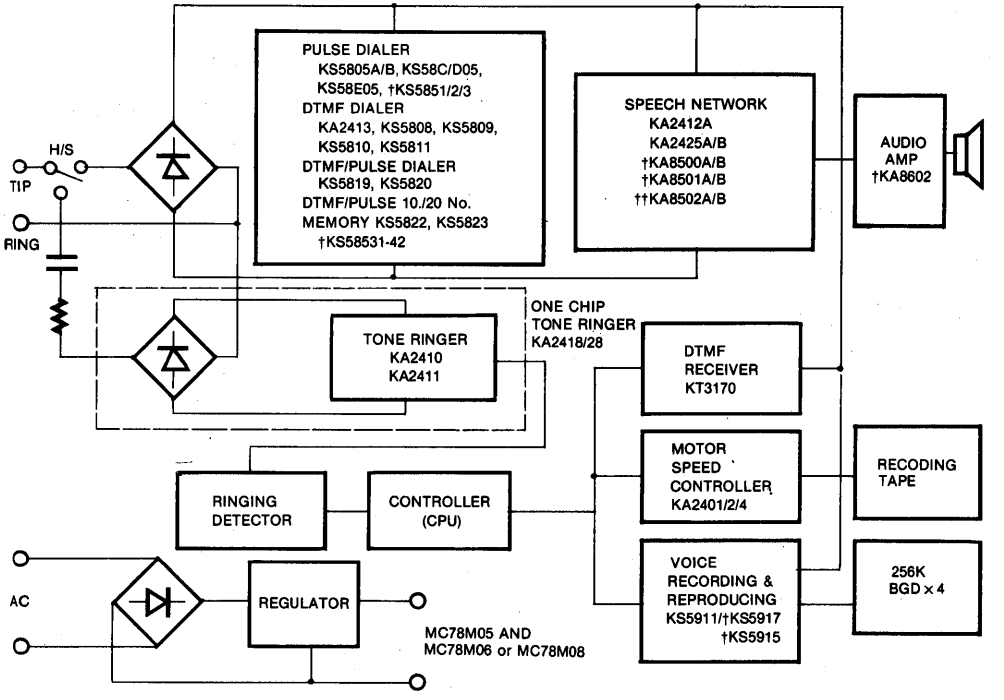


†KT8518



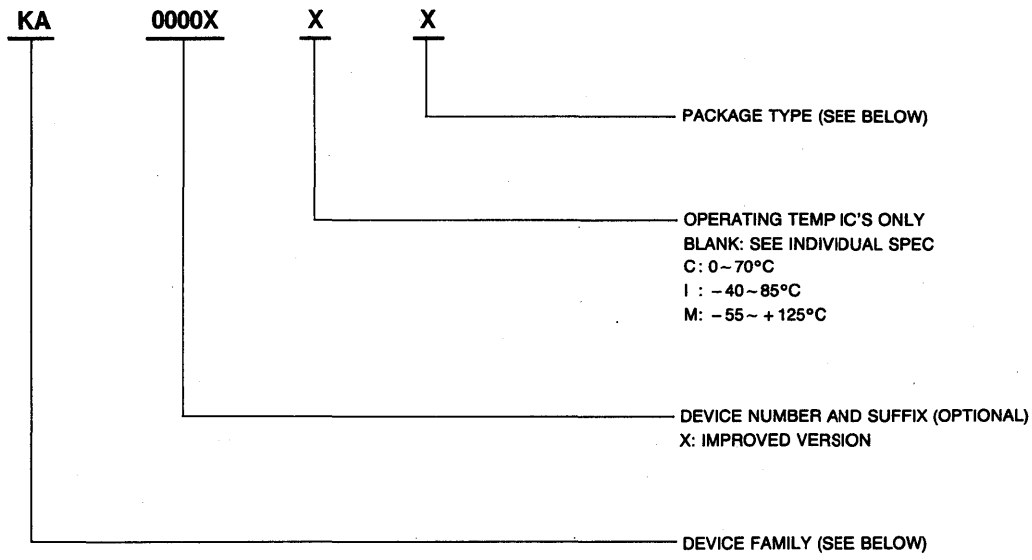
Select Inputs			Latch Addressed
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

3.6 Answering Machine



† : New Product
†† : Under Development

4. ORDERING INFORMATION



DEVICE FAMILY

TRANSISTOR / FET

DKS	DALINGTON TR
• IRF	MOS POWER
• IRFA	MOS POWER, TO-126
• IRFP	MOS POWER, TO-3P
• KSA	PNP TR
KSB	PNP TR
KSC	NPN TR
KSD	NPN TR
• MMBT	TR, SOT-23
• MMBTA	TR, SOT-23
• MMBTH	TR, SOT-23
• MPS	TR, SOT-23
• MPSA	TR, TO-92
• MPSH	TR, TO-92
• PN	TR, TO-92
SSH	MOS POWER, TO-3P
SSM	MOS POWER, TO-3
SSP	MOS POWER, TO-220
• TIP	BIPOLAR TR
• 2N	TR

INTEGRATED CIRCUIT

KA	LINEAR IC
KF	J-FET OP AMP
KG	GATE ARRAY
KS	CMOS IC
KT	TELECOM
• LM	NATIONAL
• MC	MOTOROLA
• NE	SIGNETICS
SA	LINEAR ARRAY
SD	H.D AND LINEAR ARRAY
KSV	A/D-D/A CONVERTER
KAD	A/D CONVERTER
KDA	D/A CONVERTER

PACKAGE TYPE

IC'S ONLY

D	SOP
DT	D-PACK
J	CERAMIC
K	TO-3P
L	LCCC
N	PLASTIC
PL	PLCC
R	TO-126
T	TO-220
Z	TO-92
V	TO-92L
W	ZIP
S	SIP
G	BARE CHIP
E	SSM

• NOTE: Direct-Replacement parts for products initiated by other manufacturers.

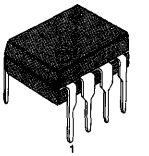
NOTES

TELEPHONE ICs 3

TONE RINGER

The KA2410/KA2411 is a bipolar integrated circuit designed for telephone bell replacement.

8 DIP



FUNCTIONS

- Two oscillators
- Output amplifier
- Power supply control circuit

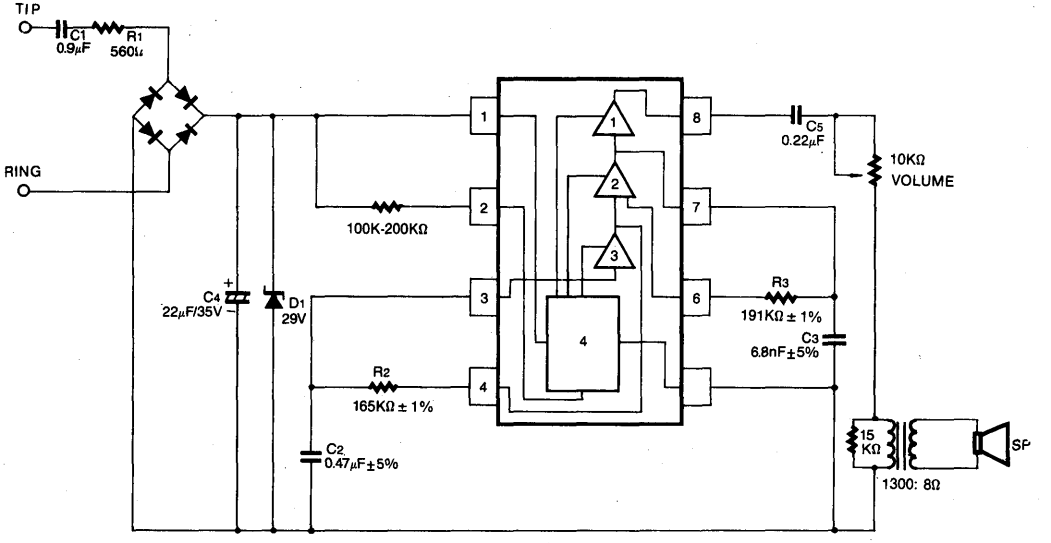
FEATURES

- **Designed for telephone bell replacement**
- **Low current drain.**
- **Small size 'MINIDIP' package.**
- **Adjustable 2-frequency tone.**
- **Adjustable warbling rate.**
- **Built-in hysteresis prevents false triggering and rotary dial 'CHIRPS'**
- **Extension tone ringer modules**
- **Alarms or other alerting devices.**
- **External triggering or ringer disable (KA2410).**
- **Adjustable for reduced initial supply current (KA2411)**

ORDERING INFORMATION

Device	Operating Temperature
KA2410N	−45 ~ +65°C
KA2411N	

APPLICATION CIRCUIT 1 (KA2410)



Note: 1. Output amplifier
2. High frequency oscillator
3. Low frequency oscillator
4. Hysteresis regulator

Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	30	V
Power Dissipation	P_D	400	mW
Operating Temperature	T_{opr}	−45 to 65	°C
Storage Temperature	T_{stg}	−65 to 150	°C

ELECTRICAL CHARACTERISTICS (T_a =25°C)

(All voltage referenced to GND unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage	V_{CC}				29.0	V
Initiation Supply Voltage[1]	V_{SI}	See Fig. 2	17	19	21	V
Initiation Supply Current[1]	I_{SI}	KA2411-6.8K-Pin 2 to GND	1.4	2.5	4.2	mA
Sustaining Voltage[2]	V_{SUS}	See Fig. 2	9.7	11.0	12.0	V
Sustaining Current[2]	I_{SUS}	No Load V_{CC}=V_{SUS}, See Fig. 2	0.7	1.4	2.5	mA
Trigger Voltage[3]	V_{TR}	KA2410 Only V_{CC}=15V	9.0	10.5	12.0	V
Trigger Current[3]	I_{TR}	KA2410 Only	10.0	20.0	1000[5]	μA
Disable Voltage[4]	V_{DIS}	KA2410 Only			0.8	V
Disable Current[4]	I_{DIS}	KA2410 Only	−40	−50		μA
Output Voltage High	V_{OH}	V_{CC}=21V, I_s=−15mA Pin 6=6V, Pin 7=GND	17.0	19.0	21.0	V
Output Voltage Low	V_{O1}	V_{CC}=21V, I_s=15mA Pin 6=GND, Pin 7=6V			1.6	V
I_{IN} (Pin 3) I_{IN} (Pin 7)		Pin 3=6V, Pin 4=GND Pin 7=6V, Pin 6=GND	— —	— —	500 500	nA nA
High Frequency 1 High Frequency 2 Low Frequency	f_{H1} f_{H2} f_L	R_3=191K, C_3=6800pF R_3=191K, C_3=6800pF R_2=165K, C_2=0.47μF	461 576 9.0	512 640 10	563 704 11.0	Hz Hz Hz

• NOTE (see electrical characteristics sheet)

1. Initial supply voltage (V_{SI}) is the supply voltage required to start the tone ringer oscillating.
2. Sustaining voltage (Vsus) is the supply voltage required to maintain oscillation.
3. V_{TR} and I_{TR} are the conditiohs applied to trigger in to start oscillation for $V_{SUS} \leqq V_{CC} \leqq V_{SI}$
4. V_{DIS} and I_{DIS} are the conditions applied to trigger in to inhibit oscillation for $V_{SI} \leqq V_{CC}$
5. Trigger current must be limited to this value externally.

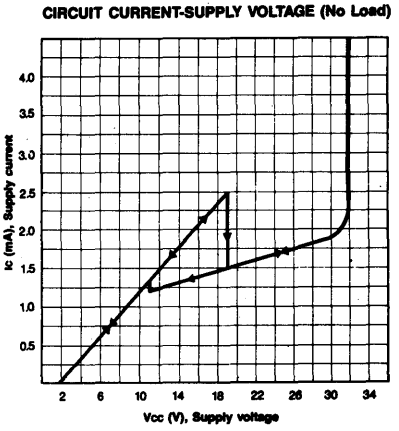


Fig. 2

APPLICATION NOTE

The application circuit illustrates the use of the KA2410/KA2411 devices in typical telephone or extension tone ringer applications.

The AC ringer signal voltage appears across the TIP and RING inputs of the circuit and is attenuated by capacitor C_1 and resistor R_1.

C_1 also provides isolation from DC voltages (48V) on the exchange line.

After full wave rectification by the bridge diode, the waveform is filtered by capacitor C_4 to provide a DC supply for the tone ringer chip.

When this voltage exceeds the initiation voltage (V_{SI}), oscillation starts.

With the components shown, the output frequency chops between 512 (f_{h1}) and 640Hz (f_{h2}) at a 10Hz (f_L) rate.

The loudspeaker load is coupled through a 1300Ω to 8Ω transformer.

The output coupling capacitor C_5 is required with transformer coupled loads.

When driving a piezo-ceramic transducer type load, the coupling C_5 and transformer (1300Ω: 8Ω) are not required. However, a current limiting resistor is required.

The low frequency oscillator oscillates at a rate (f_L) controlled by an external resistor (R_2) and capacitor (C_2).

The frequency can be determined using the relation $f_L = 1/1.289\ R_2.\ C_2$. The high frequency oscillates at a f_{H1}, f_{H2} controlled by an external resistor (R_3) and capacitor (C_3). The frequency can be determined using the relation $f_{HI} = 1/1.504\ R_3.\ C_3$. $f_{H2} = 1/1.203\ R_3,\ C_3$.

Pin 2 of the KA2411 allows connection of an external resistor R_{SL}, which is used to program the slope of the supply current vs supply voltage characteristics (see Fig 4), and hence the supply current up to the initial voltage (V_{SI}). This initial voltage remains constant independent of R_{SL}.

The supply current drawn prior to triggering varies inversely with R_{SL}, decreasing for an increasing value of resistance. Thus, increasing the value of R_{SL}, will decrease the amount of AC ringing current required to trigger the device. As such longer subscriber loops are possible since less voltage is dropped per unit length of loop wire due to the lower current level. R_{SL} can also be used to compensate for smaller AC coupling capacitors (C_5 on Fig 3) (higher impedance) to the line which is used to alter the ringer equivalence number of a tone ringer circuit.

The graph in Fig. 4 illustrates the variation of supply current with supply voltage of the KA2411. Three curves are drawn to show the variation of initiation current with R_{SL}. Curve B ($R_{SL} = 6.8K\Omega$) shows the I-V characteristic for the KA2411 tone ringer. Curve A is a piot with $R_{SL} < 6.8K\Omega$ and shows an increase in the current drawn up to the initiation voltage V_{SI}. The I-V characteristic after initiation remains unchanged. Curve C illustrates the effect of increasing R_{SL} above 6.8KΩ initiation current decreases but is unchanged again after triggering.

APPLICATION CIRCUIT 2 (KA2411)

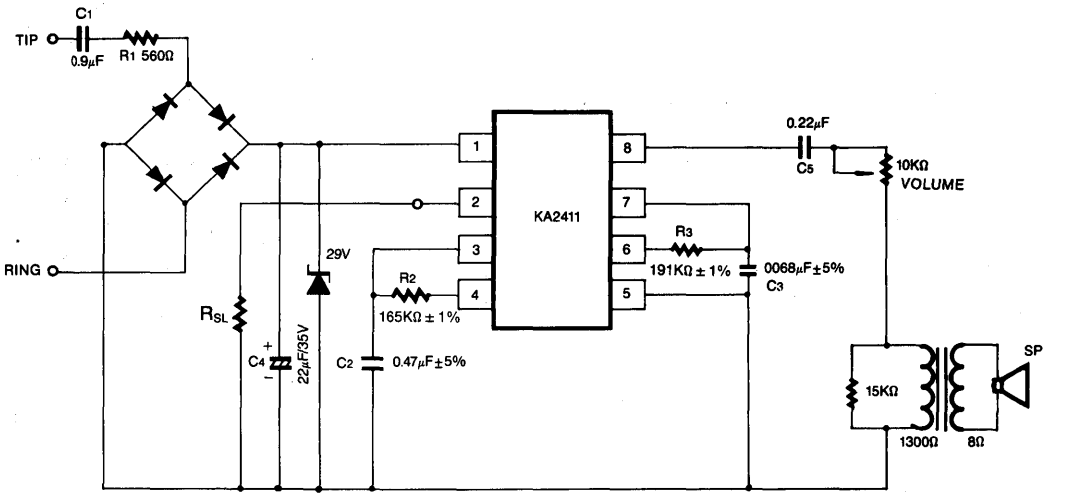


Fig. 3

LINEAR INTEGRATED CIRCUIT

KA2411 Supply Current (No Load) Vs. Supply Voltage

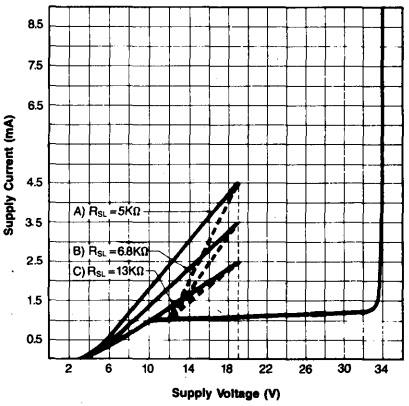


Fig. 4

EQUIVALENT CIRCUIT (Pin 2 Input)

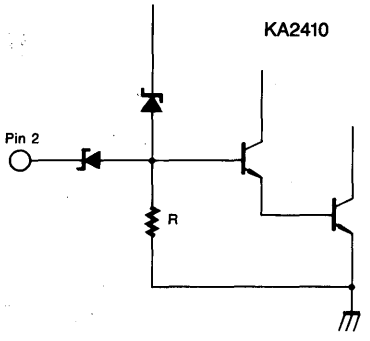


Fig. 5

INHIBITING OSCILLATION

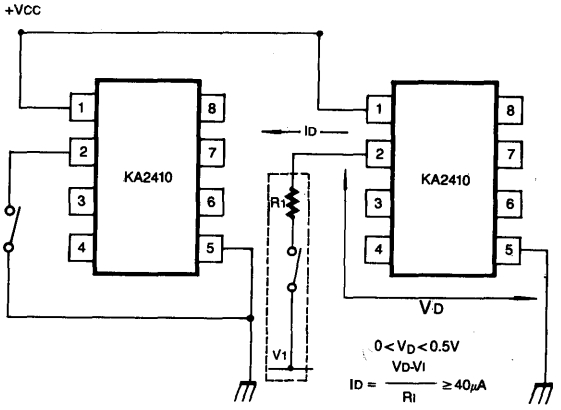


Fig. 6

PROGRAMMING THE KA2410 INITIATION SUPPLY VOLTAGE

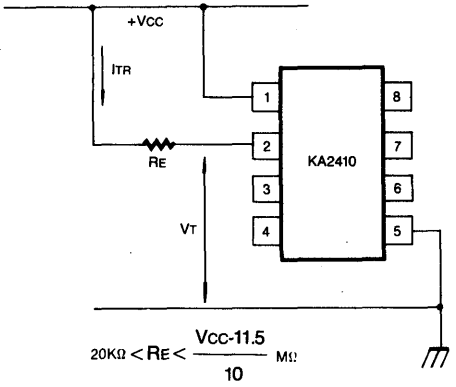


Fig. 7

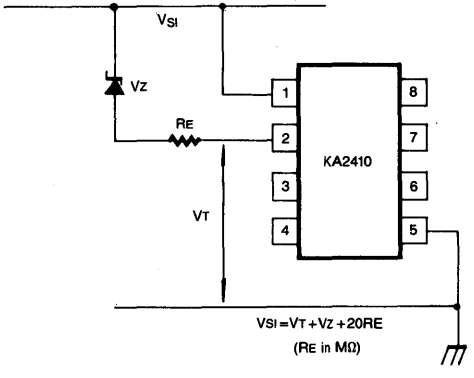


Fig. 8

TRIGGERING THE KA2410 FROM CMOS OR TTL LOGIC

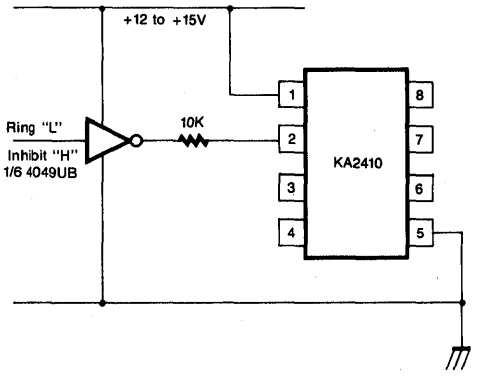


Fig. 9

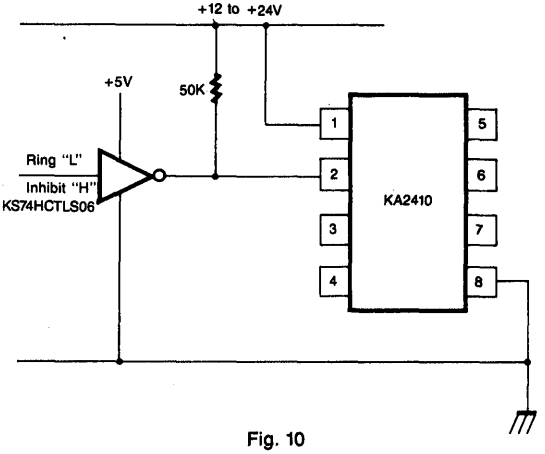
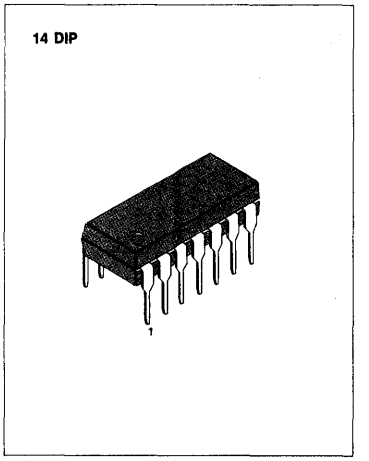


Fig. 10

TELEPHONE SPEECH CIRCUITS

The KA2412A is designed for replacement of the hybrid circuit (2 ~ 4 wire interface) in conventional telephones.



FEATURES

- **Adjustable sending and receiving gain to compensate for line attenuation by sensing the line current.**
- **The same type of transducer can be used for both transmitter and receiver, usually a 350Ω dynamic type.**
- **Output impedance can be matched to the line, independent of transducer impedance.**
- **Minimum number of external parts required**

BLOCK DIAGRAM

ORDERING INFORMATION

Device	Operating Temperature
KA2412AN	– 20 ~ + 70°C

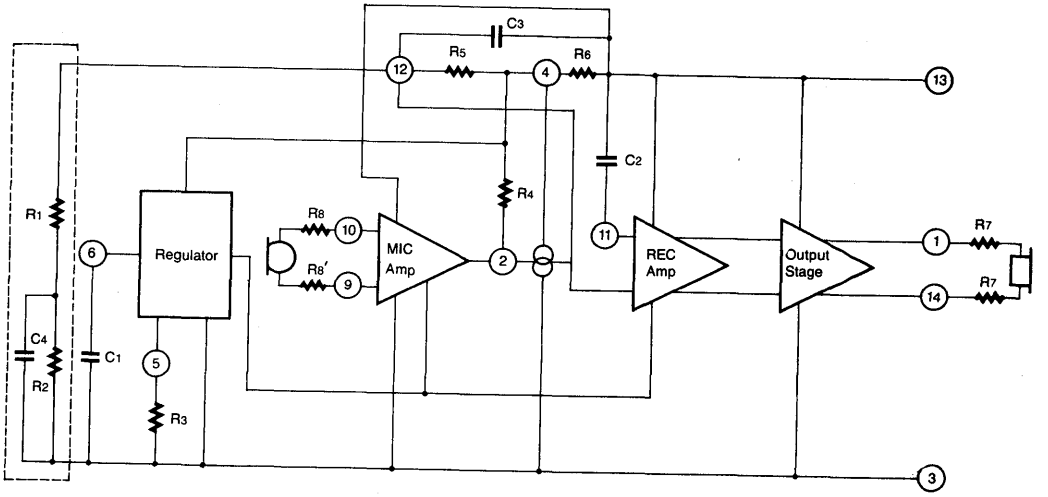


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Line Voltage (3 msec pulse duration)	V_L	22	V
Forword Line Current	I_{LF}	120	mA
Reverse Line Current	I_{LR}	−150	mA
Power Dissipation	P_D	1.0	W
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(T_a = −15°C ~ +45°C, f=300Hz ~ 3400Hz unless otherwise specified. Refer to the test circuit.)

Characteristic	Symbol	Test Circuit	Test Conditions	Min	Typ	Max	Unit
Line Voltage	V_L	Fig 2	I_L = 80mA I_L = 20mA I_L = 10mA	10.0 5.0 3.8		11.5 5.8 4.6	V
Sending Gain	G_S	Fig 3	T_a = 25°C, f = 1KHz I_L = 15mA I_L = 30mA I_L = 60mA I_L = 80mA	 46.5 45.5 40.5 40.5		 50.5 49.5 44.5 44.5	dB
Sending Gain Variation vs temp	ΔG_{ST}	Fig 3	−15°C < T_a < +45°C		±0.8		dB
Sending Gain Flatness	ΔG_{SF}	Fig 3	G_S = 0dB at f=1KHz I_L = 10 ~ 80mA			±0.5	dB
Sending Distortion	THD_S	Fig 3	I_L = 20mA V_{SO} = 1V_{P-P} I_L = 80mA V_{SO} = 400mVrms			2.0 2.0	% %
Sending Noise	V_{NS}		V_{MI} = 0, I_L = 60mA			130	μV
Maximum Sending Output	V_S (max)	Fig 3	I_L = 10 V_{MI} = 707mVrms			6.0	V_{P-P}
Receiving Gain	G_R	Fig 4	T_a = 25°C, f = 1KHz I_L = 15mA I_L = 30mA I_L = 60mA I_L = 80mA	 −12.6 −12.6 −19.9 −20.1		 −9.0 −9.0 −16.3 −17.9	dB
Receiving Gain variation vs temp	ΔG_{RT}	Fig 4	−15°C < T_a < 45°C		±0.8		dB
Receiving Gain Flatness	ΔG_{RF}	Fig 4	G_R = 0dB at f=1KHz I_L = 10 ~ 80mA			±0.5	dB

ELECTRICAL CHARACTERISTICS (Continued)

(T_a = −15°C ~ +45°C, f=300Hz ~ 3400Hz, unless otherwise specified refer to the test circuit)

Characteristic	Symbol	Test Circuit	Test Conditions	Min	Typ	Max	Unit
Receiving Distortion	THD_R	Fig 4	I_L=20mA ~ 80mA V_{RO}=200mVrms			2.0	%
Receiving Noise	V_{NR}	Fig 4	V_{RI}=OV, I_L=60mA Posphometric			75	μV
Max Receiving Output Current		I_{om}	I_L=10mA V_{RI}=707mVrms			2.0	mA
Side Tone	ST	Fig 5	f=1KHz, T_a=25°C I_L=20mA I_L=60mA		7.0 0.0		dB
Return Loss	R_L	Fig 6	S2 in a S2 in b		14 14		dB

PIN DESCRIPTION

1. Pin 1, Pin 14 : Receiver output
2. Pin 2 : Line impedance adjust
3. Pin 3 : Ground
4. Pin 4 : DC regulator
5. Pin 5 : Bias
6. Pin 6 : AC loop opening
7. Pin 7 : No connection
8. Pin 8 : No connection
9. Pin 9, Pin 10 : Mic input
10. Pin 11 : Input receive Amp (−)
11. Pin 12 : Input receive Amp (+)
12. Pin 13 : V_{CC}

TEST CIRCUIT

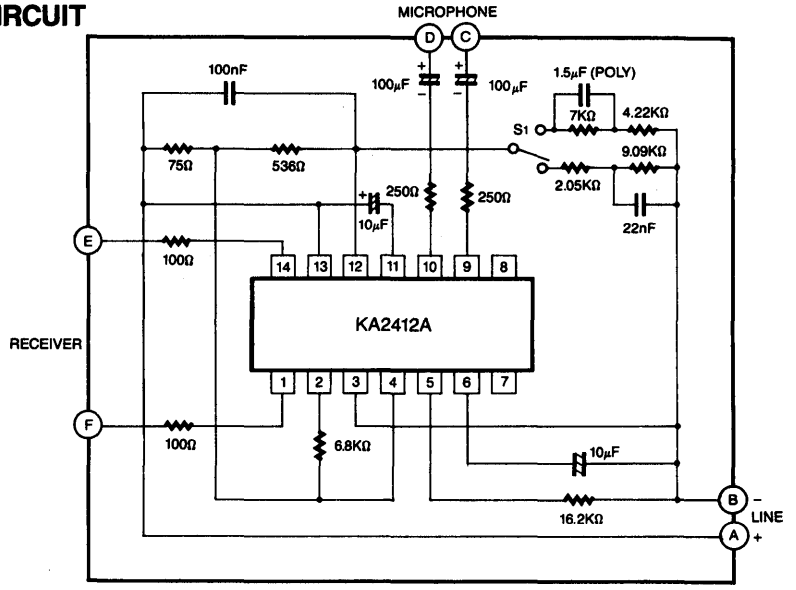


Fig. 2

Sending Gain

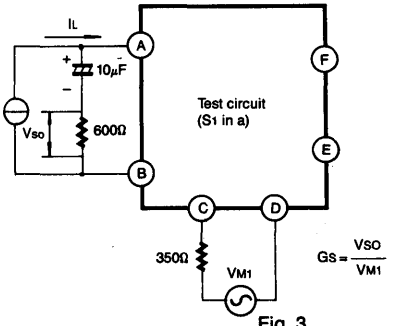


Fig. 3

Receiving Gain

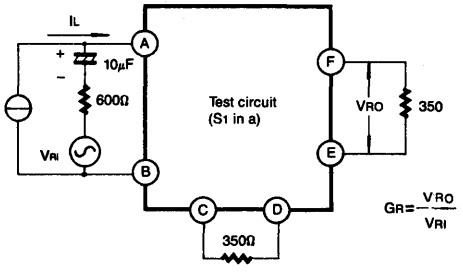


Fig. 4

Side Tone

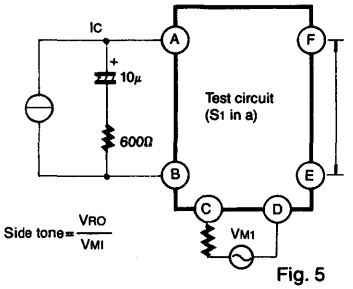


Fig. 5

Return Loss

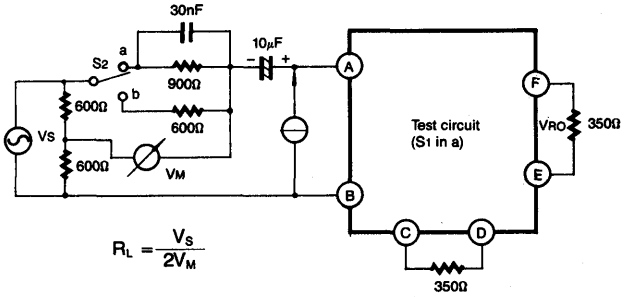


Fig. 6

APPLICATION INFOMRATION

The following table is recommended for Fig. 1. Different values can be used and notes are added in order to help designer.

Component	Recommended Value	Purpose	Note
R_1	2.05K	Balance network	In order to optimize the sidetone it is possible to change R_1 and R_2 values. In any case: $\frac{Z_B}{Z_L} = \frac{R_5}{R_6}$ where $Z_B = R_1 + R_2 // C_4$
R_2	9.09K		
R_3	16.2K	Bias resistor	By changing R_3 value, it is possible to shift the gain characteristics. The value can be chosen from 15K to 20K. The recommended value assures the maximum swing
R_5	536	Bridge resistors	The ratio R_5/R_6 fixes the amount of the signal delivered to the line.
R_6	75		
R_7, R_7'	100	Receiver impedance matching	R_7 and R_7' must be equal; 100Ω is a typical value for dynamic capsules
R_8, R_8'	250	Microphone impedance matching	R_8 and R_8' must be equal; 250Ω is a typical value for dynamic capsules. Furthermore, they determine the sending gain variation according to; $G_S = 20 \log \frac{R_X}{850}$ where $R_X = R_8 + R_8' + R_{MIC}$
C_1	10uF	AC loop opening	Ensures a high regulator impedance for AC signals (=20KΩ). This capacitor should not be higher than 10uF in order to have a short response time of the system.
C_2	1uF	DC decoupling for receiving input	
C_3	82nF	High frequency roll-off	C_3 determines the high frequency response of the circuit. It also acts as RF by pass.
C_4	22nF	Balance network	See note for R_1 and R_2

DESCRIPTION

1. Circuit Description:

The KA2412A is based on a bridge configuration. The KA2412A contains a regulator block, a sending amplifier and a receiving amplifier. The regulator monitors the line current and adjusts the amplifier gain to compensate for the line length.

The transmit/receiver amplifiers are connected to the line via an external bridge to provide side tone attenuation. When the subscriber is talking, A controlled amount of the sending signal is allowed to reach the receiver to give a feedback to the subscriber. The phenomenon is caused by mismatching of the wheastone bridge and is called the side tone signal.

The line current compensation ensures that when the subscriber is talking, the signal delivered to the line is increased in according to the line length. When he is hearing, the signal level on the receiver capsule is constant.

Gain variation over the operating temperature range is less than ±1dB. The impedance to the line can be adjusted; without any change in circuit parameters; by changing an external resistor (6.8KΩ at Pin 2).

The KA2412A works with the same type of transducers for both transmitter and receiver (typically 350Ω Dynamic units).

2. Two to four wires conversion

1) In the case of the traditional telephone set:

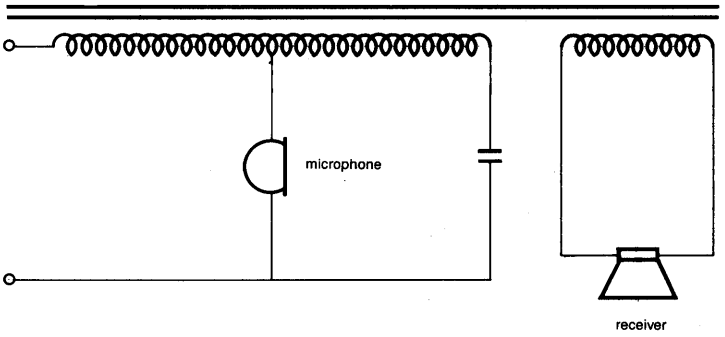


Fig. 10

A traditional speech circuit is equivalently equal to the circuit as described in Fig. 7. The microphone is composed of carbon powder. It converts the sound pressure into the variation of resistance and so a AC signal is generated when the bias current flows through the microphone and a subscriber is talking. The current actuated by the microphone does not affect the receiver because it is compensated by the coil polarity.

But the incoming signal is transferied to the receiver, so and this circuit is called 2—4 wires conversion, which is incoming 2 wires and Mic. Receivers 4 wires.

2) In the case of the KA2412 A

KA2412A performs the two wires (Telephone line) to four wires (Microphone, Receiver) conversion by means of a wheastone bridge configuration so obtaining the proper decoupling between sending and receiving signals (see Fig. 8)

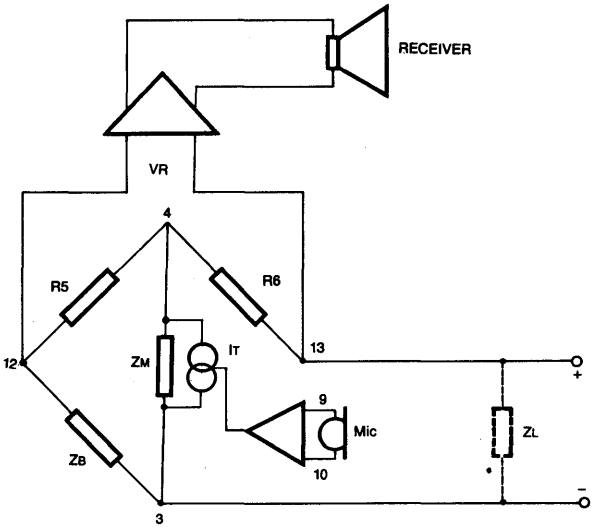


Fig. 8

For a perfect balancing of the bridge $\frac{Z_B}{Z_L} = \frac{R5}{R6}$

* In sending mode;

The AC signal from the microphone is sent to one diagonal of the bridge (pin 3 and pin 4). A small percentage of the signal power is lost on Z_B (being $Z_B >> Z_L$); the main part is sent to the line Via R6.

The impedance A_M is defined as $\frac{V_{4\text{-}3}}{I_{4\text{-}3}}$

$$V_R = \frac{(R6+Z_B)//(R5+Z_L)}{Z_M+(R6+Z_B)//(R5+Z_L)} \left(\frac{Z_L}{R6+Z_L} - \frac{Z_B}{R5+Z_B}\right) Z_M I_T$$

To reduce the receiving input signal,

$$\frac{Z_L}{R6+Z_L} = \frac{Z_B}{R5+Z_B} \rightarrow \frac{R6}{Z_L} = \frac{R5}{Z_B}$$

also, in order to reduce power loss in R5 & Z_B and to transfer the maximum power to the line via R6.

$R5+Z_B >> R6+Z_L$

$R6+Z_M = Z_L$

Then the line impedance Z_L grows from 600 ohm to 900 ohm when the line length increases.
The voltage driven to the line is

$$V_L = \frac{Z_L}{R6+Z_M+Z_L} \times Z_{MIT}$$

In order to maximize sending Gain
$Z_L >> R6$

Therefore, in the case of the KA2412 test circuit:
$R6=75$, $Z_M=6.8K/11$, $Z_L=600$

$$V_L = \frac{Z_L}{Z_M+R6+Z_L} \times Z_M I_T = 286.82 I_T$$

* In receiving mode:
The AC signal coming from the line is sensed across the second diagonal of the wheastone bridge (pin 11 and pin 13). After amplification it is applied to the receiver.

$$V_R = \frac{V_I}{Z_L+R_6+(R_5+Z_B)//Z_M} (R_6+R_5+Z_B)//Z_M \left(1-\frac{Z_B}{Z_B+R_5}\right)$$

$$= \frac{V_I}{Z_L+R_6+(R_5+Z_B)//Z_M} \left(R_6+\frac{Z_M R_5}{Z_M+R_5+R_6}\right)$$

To avoid the reflection
$Z_L=R_6+Z_M$, $10 Z_M=R_5+Z_B$

Therefore

$$V_R = \frac{V_I}{2R_6+1.91 Z_M}\left(R_6+\frac{Z_B}{11}\right)$$

In the case of the KA2412A test circuit
$Z_L=600\Omega$, $R_6=75\Omega$, $Z_M=6.8K\Omega/11=6.8\Omega$
$R_5=536\Omega$, $Z_B=6.076K\Omega$ ($f_{REF}=1KHz$)

$$\frac{V_R}{V_I}=0.093$$

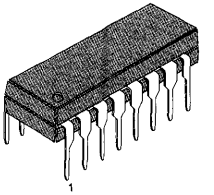
3. Automatic Gain Control.

The KA2412A automatically adjusts the gain of the sending and receiving amplifiers to compensate for line attenuation. The maximum gain is reached for a line current range of 10—20 mA and minimum gain can also be reached for a line current range of 60—100 mA.

DUAL TONE MULTI FREQUENCY GENERATOR

The KA2413 is a monolithic integrated DTMF generator designed for use in a telephone set in parallel with an electronic speech circuit. The DC characteristic to the line is set by the speech circuit.

16 DIP



FEATURES

- **Wide operating line voltage and current range**
- **Operates with a standard crystal at 3.58MHz**
- **Operates with a single contact or matrix key-board**
- **Levels from the high and low frequency group can be adjusted separately.**
- **No individual level adjustment is necessary for every circuit**
- **The signal levels are stabilized against variations in temperature and line voltage.**
- **Short start-up time**
- **All tones can be generated separately for testing.**
- **Easy PCB layout; all keyboard connections on one side of the chip**
- **Internal protection of all inputs**
- **Minimum number of external parts required.**

ORDERING INFORMATION

Device	Operating Temperature
KA2413N	−20 ~ +70°C

BLOCK DIAGRAM

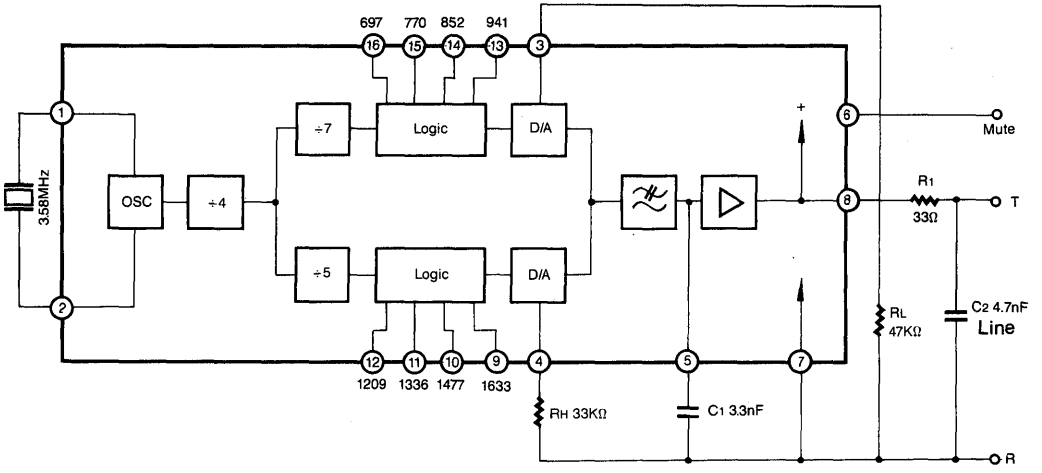


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Line Voltage (Peak) t_P =2 sec	V_L (peak)	20	V
Line Voltage (Peak) t_P =20m sec	V_L (peak)	22	V
Line Voltage (Conditions)	V_L (cont)	15	V
Power Dissipation	P_D	400	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−55 ~ +150	°C

ELECTRICAL CHARACTERISTICS (T_a =25°C)

(V_L =4.3 ~ 9V, unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Line Voltage		V_L (opr)	Tone Generation 1.3 V_P Signal	4.3		9.0	V
Standby Line Voltage		V_L (std)	Stand-By 2.0 V_P Signal	4.3		9.0	V
Operating Line Current		I_L (opr)	V_L =4.3V			10.0	mA
Standby Line Current		I_L (std)	No Key Pressed V_L =4.3V			250	μA
Mute Current		I_M	One or More Keys Pressed	125.0			μA
Key Resistance		R_K	Key Circuit Closed			1.0	kΩ
Tone Output Frequency							
Low (Row)	f_1 = 697 Hz	Δf	f_{OSC} =3.5795 MHz	−1.0	−0.32	+1.0	%
	f_2 =770 Hz			−1.0	+0.02	+1.0	%
	f_3 =852 Hz			−1.0	+0.03	+1.0	%
	f_4 =941 Hz			−1.0	−0.11	+1.0	%
High (Column)	f_5 =1209 Hz			−1.0	−0.03	+1.0	%
	f_6 =1336 Hz			−1.0	−0.03	+1.0	%
	f_7 =1477 Hz			−1.0	−0.68	+1.0	%
	f_8 =1633 Hz			−1.0	−0.36	+1.0	%

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Signal level	High	V_H	R_H=46.4KΩ R_L=69.8KΩ		-9.0		dBm
	Low	V_L			-11.0		
	High	V_H	R_H=33.0KΩ R_L=47.0KΩ	-8.0	-6.0	-4.0	dBm
	Low	V_L		-10.0	-8.0	-6.0	
	High	V_H	R_H=26.1KΩ R_L=39.2KΩ		-4.0		dBm
	Low	V_L			-6.0		
Ratio Signal Level		V_H/V_L		1.0	2.0	3.0	dB
Impedance to Line		Z_L	Tone Generation Stand-By	6.0 50.0			KΩ
Total Harmonic Distortion		THD	Tone Generation			-31.0	dBm
Output Noise		V_{NO}	Stand-By			-80.0	dBm
Harmonics			300 — 3400Hz			-33.0	dBm
			3.4 — 50KHz			-33.0	dBm
			≥50KHz			-80.0	dBm
Start-up Time		t_S	Output level within 1dB from final level		3	5	mS

TEST CIRCUIT

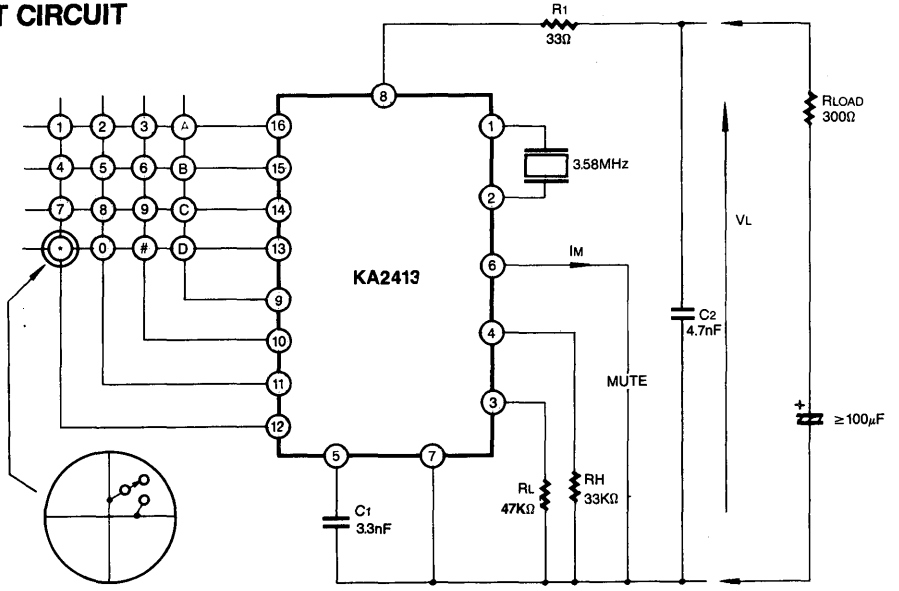


Fig. 2

• KA2413 can also be controlled by a microprocessor (see Fig 5). The negative branch of the microprocessor voltage supply is connected to pin 7 of the KA2413 and the inputs (8) are connected with resistors.

For tone-generating, one input of the low group (Pins 13—16) is connected to the positive voltage and one input of the high group (Pins 9—12) is connected to the negative voltage, then the KA2413 is activated and activated and the mute output is put in High state.

Microcomputer interface

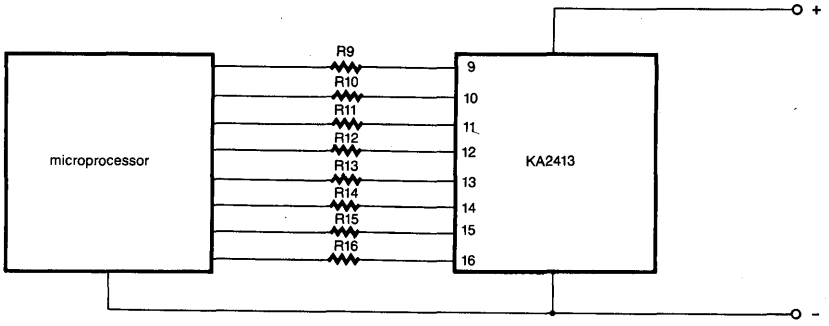


Fig. 5

1) R9, R10, R11, R12 (60K — 80K)
The two functions of the resistors are:
— To raise the OFF/ON voltage
— To limit the current when the input levels are high. Too high current will interfere with the functions of the other three inputs (the resistors can be exchanged with diodes directly away from the KA2413)

High-frequency group resistors to microcomputer

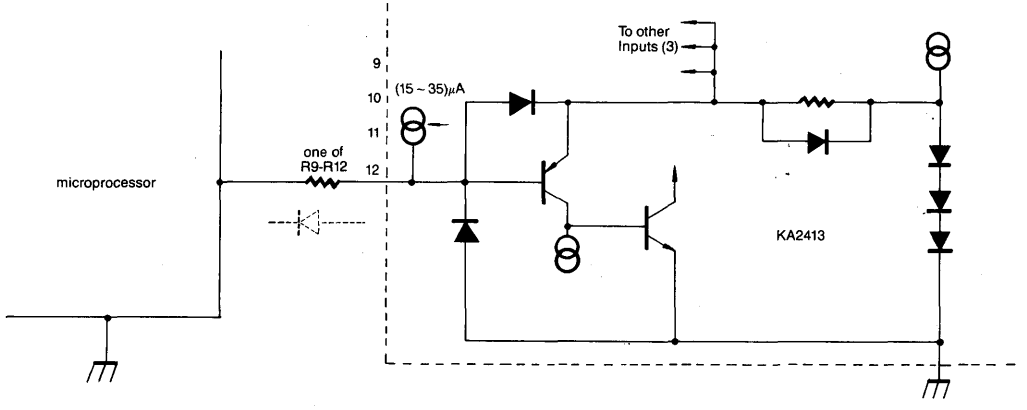


Fig. 6

2) R13, R14, R15, R16 (20K — 30K)
The two functions of the resistors are:
— To raise the OFF/ON voltage
— To limit the current when the input levels are high.

Low-frequency group resistors for microcomputer

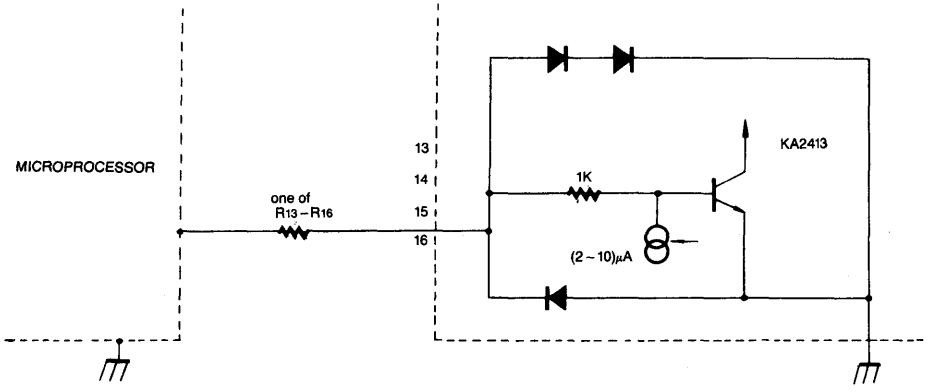
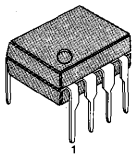


Fig. 7

TELEPHONE TONE RINGER WITH BRIDGE DIODE

The KA2418/28 is a monolithic integrated circuit telephone tone ringer with bridge diode, when coupled with an appropriate transducer, it replaces the electromechanical beil. This device is designed for use with either a piezo transducer or an inexpensive transformer coupled speaker to produce a pleasing tone composed of a high frequency (f_R) alternating with a low frequency (f_L) resulting in a warble frequency. The supply voltage is obtained from the AC ring signal and the circuit is designed so that noise on the line or variation of the ringing signal can not affect correct operation of the device.

8 DIP



FEATURES

- **On chip high voltage full wave diode bridge rectifier**
- **Low current consumption, in order to allow the parallel operation of the 4 devices**
- **Low external component count**
- **Tone and switching frequencies adjustable by external components**
- **High noise immunity due to built-in voltage-current hysteresis**
- **Activation voltage adjustable**
- **Internal zener diodes to protect against over voltages**
- **Ringer impedance adjustable with external components.**

ORDERING INFORMATION

Device	Operating Temperature
KA2418N	−20 ~ +70°C
KA2428N	

APPLICATIONS

- Electronic telephone ringers
- Extension ringers

BLOCK DIAGRAM

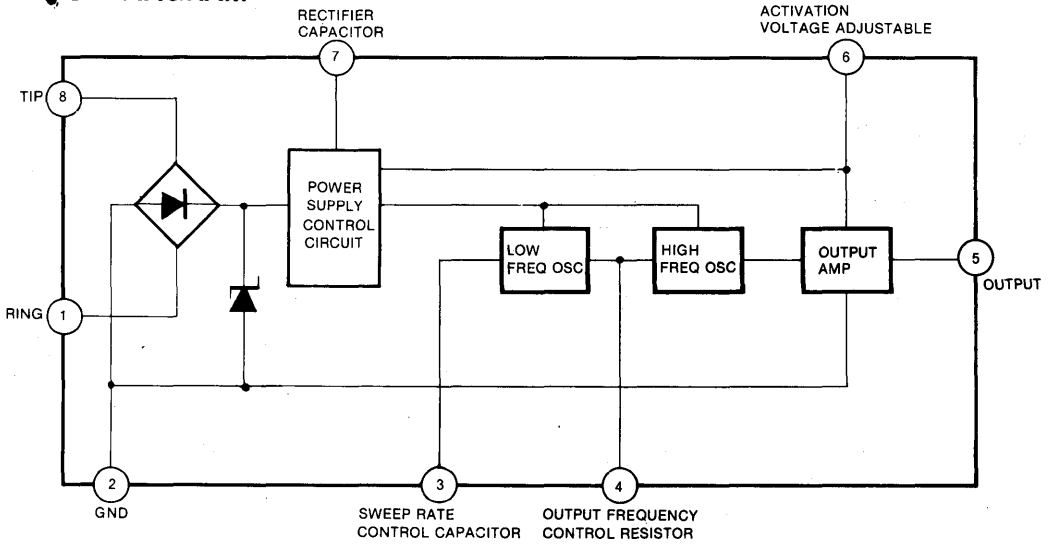


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Calling Voltage (f=50Hz) Continuous	V_{TP}	120	Vrms
Calling Voltage (f=50Hz) 5 Sec ON/10 Sec OFF	V_{TP}	200	Vrms
Supply Current	I_{CC}	22	mA
Operating Temperature	T_{OP}	−20 ~ +70	°C
Storage and Junction Temperature	T_{stg}	−65 ~ +150	°C

Absolute maximum ratings are those values beyond which peramanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS

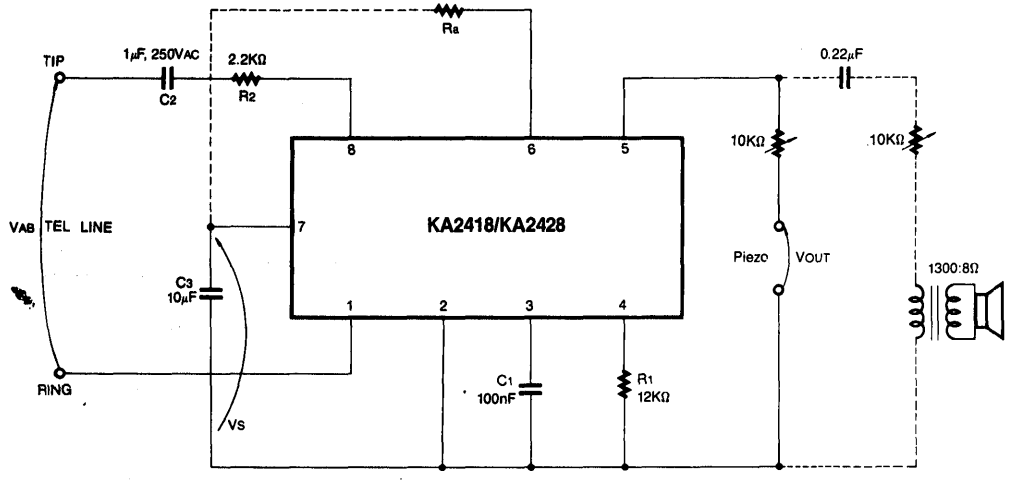
(T_a = 25°C unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{CC}				26	V
Current Consumption without Load	I_{CC}	V_S = 8.8 to 26V		1.5	1.8	mA
Activiation Voltage	V_{ON}		12.2		13	V
Activiation Voltage Range	V_{ONR}	R_A = 1kΩ	8		10	V
Sustaining Voltage	V_{SUS}		8		8.8	V
Differential Resistance in Off Condition	R_D		6.4			kΩ
Output Voltage Swing	V_{OUT}			V_{CC} −3		V
Short Circuit Current	I_{OUT}	V_S = 26V		35		mA

AC OPERATION

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Frequencies (KA2418)		V_{CC} = 26V, R_1 = 14KΩ				
f_{H1}	f_{H1}	V_{CC} = 0V		2300		Hz
f_{H2}	f_{H2}	V_{CC} = 6V		1700		Hz
Output Frequencies (KA2428)		V_{CC} = 26V, R_1 = 14KΩ				
f_{H1}	f_{H1}	V_{CC} = 0V		1900		Hz
f_{H2}	f_{H2}	V_{CC} = 6V		1300		Hz
f_{H1} Range		R_i = 27KΩ to 1.7KΩ	0.1		15	KHz
Sweep Frequency	f_L	R_1 = 14KΩ, C_1 = 100nF		10		Hz

TEST AND APPLICATION CIRCUIT



$$f_1 = \frac{3.22 \cdot 10^4}{R_1\,(K\Omega)}\ (KA2418),\quad f_1 = \frac{2.66 \cdot 10^4}{R_1\,(K\Omega)}\ (KA2428),\quad f_2 = \frac{5}{7} f_1 \qquad f_{sweep} = \frac{1000}{C_1\,(nF)}$$

Fig. 2

DESCRIPTION

The KA2418/28 tone ringer derives its power supply by rectifying the AC ringing signal. It uses this power to activate two tone generators. The two tone frequencies generated are switched by an internal oscillator in a fast sequence and made audible across an output amplifier in the loudspeaker; both tone frequencies and the switching frequency can be externally adjusted.

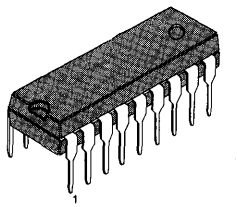
The device can drive either directly a piezo ceramic converter (buzzer) or small loudspeaker. In case of using a loudspeaker, a transformer is needed.

An internal shunt voltage regulator provides DC voltage to the output stage, low frequency oscillator, and high frequency oscillator. To protect the IC from telephone line transients, a zener Diode is included.

SPEECH NETWORK WITH DIALER INTERFACE

The KA2425A/B is a telephone speech network integrated circuit which includes transmit amp, receive amp, sidetone amp, DC loop interface function, DTMF input, voltage regulator for speech, a regulated output voltage for a dialer, and equalization circuit.

18 DIP



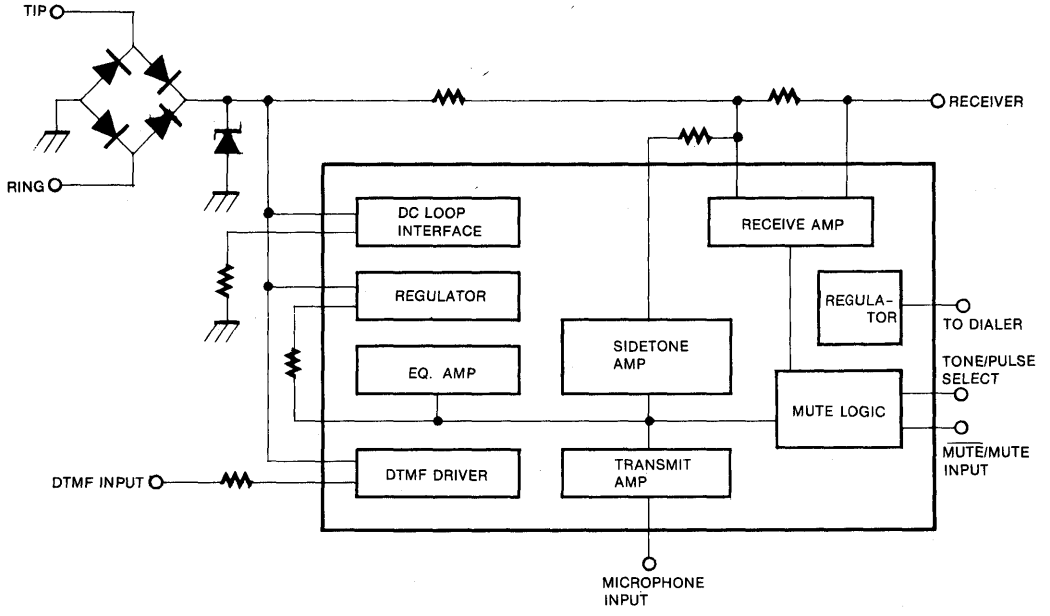
FEATURES

- **Low voltage operation (1.5V: speech)**
- **Transmit, receive, side tone and DTMF level are controlled by external resistors**
- **Regulated voltage for dialer**
- **Loop length equalization**
- **$\overline{\text{MUTE}}$: KA2425A MUTE: KA2425B**
- **Linear interface for DTMF**

ORDERING INFORMATION

Device	Package	Function	Operating Temperature
KA2425AN	18 DIP	$\overline{\text{MUTE}}$	−20 ~ +60°C
KA2425BN	18 DIP	MUTE	

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Value	Unit
V_+ Voltage	−1.0 ~ +18	V
$\overline{V_{DD}}$ ($V_+ = 0$)	−1.0 ~ +6	V
$\overline{MT}$, MT, MS Inputs	−1.0 ~ V_{DD} + 1	V
V_{LR}	−1.0 ~ V_+ − 3.0	V
Storage Temperature	−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Value	Unit
I_{TXO} (Instantaneous)	0 ~ 10	mA
V_+ Voltage: Speech Mode	+1.5 ~ +15	V
Tone Dialing Mode	+3.3 ~ +15	V
Operating Temperature	−20 ~ +60	°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C, Refer to Fig. 1)

Characteristic	Test Conditions	Min	Typ	Max	Unit
SYSTEM SPECIFICATIONS (Refer to Fig. 1	**Fig. 4)**				
Tip-Ring Voltage (including polarity guard bridge drop of 1.4V) (Speech Mode)	I_L = 5.0mA	—	2.4	—	V_{dc}
	I_L = 10mA	—	3.9	—	
	I_L = 20mA	—	4.6	—	
	I_L = 40mA	—	5.6	—	
	I_L = 60mA	—	6.6	—	
Transmit					
Gain from V_S to V+	Figure 3 (I_L = 20mA)	28	29.5	31	dB
Gain Change	I_L = 60mA	−6.0	−4.5	−3.6	dB
Distortion		—	2.0	—	%
Output Noise		—	11	—	dBmc
Receive					
V_{RXO}/V_S	f = 1.0KHz, I_L = 20mA	−16	−15	−13	dB
Receive Gain Change	(See Figure 4) I_L = 60mA	−5.0	−3.0	−2.0	dB
Distortion		—	2.0	—	%
Sidetone Level					dB
$V_{RXO}/V+$ (Figure 3)	I_L = 20mA	—	−36	—	
	I_L = 60mA	—	−21	—	
Sidetone Cancellation $\{\frac{V_{RXO}}{V+}$(Figure 4)$\}$dB − $\{\frac{V_{RXO}}{V+}$(Figure 3)$\}$dB	I_L = 20mA	20	26	—	dB
DTMF Driver		3.2	4.8	6.2	dB
$V+ V_{IN}$ (Figure 2)	I_L = 20mA				
AC Impedance					Ω
Speech mode (incl. C_6, See Figure 4)	I_L = 20mA	—	750	—	
$Z_{ac} = (600)V+/(V_S - V+)$	I_L = 60mA	—	300	—	
Tone Mode (including C_6)	20mA < I_L < 60mA	—	1650	—	

Note: Typicals are not tested or guaranteed.

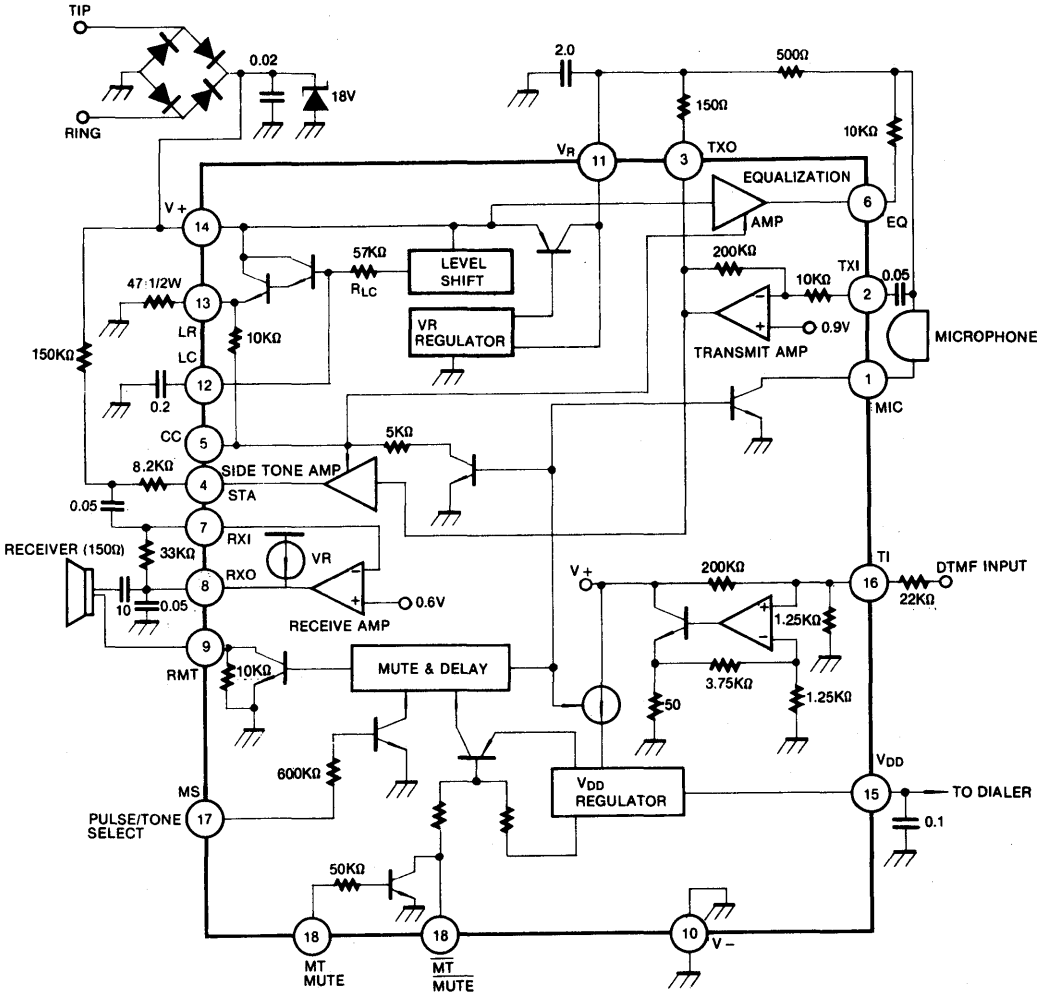
ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
SPEECH AMPLIFIERS						
Transmit Amplifier						
Gain	A_{TXO}	TXI to TXO	22	24	26	dB
TXO Bias Voltage	V_{TXOSP}	Speech/Pulse Mode	0.45	0.52	0.60	$\times V_R$
TXO Bias Voltage	V_{TXCOL}	Tone Mode	VR – 25	VR – 5.0	—	mV
TXO High Voltage	V_{TXCH}	Speech/Pulse Mode	VR – 25	VR – 5.0	—	mV
TXO Low Voltage	V_{TXCL}	Speech/Pulse Mode	—	125	250	mV
TXI Input Resistance	R_{TXI}		—	10	—	KΩ
Receive Amplifier						
RXO Bias Voltage	V_{RXO}	All Mode	0.45	0.52	0.60	$\times V_R$
RXO Source Current	I_{RXOSP}	Speech Mode	1.5	2.0	—	mA
RXO Source Current	I_{RXOCL}	Pulse/Tone Mode	200	400	—	μA
RXO High Voltage	V_{RXCH}	All Mode	VR – 100	VR – 50	—	mV
RXO Low Voltage	V_{RXOL}	All Mode	—	50	150	mV
SIDETONE AMPLIFIER						
Gain (TXO to STA)	A_{STA}					dB
Speech Mode		$@V_{LR} = 0.5V$	—	– 15	—	
Speech Mode		$@V_{LR} = 2.5V$	—	– 21	—	
Pulse Mode		$@V_{LR} = 0.2V$	—	– 15	—	
Pulse Mode		$@V_{LR} = 1.0V$	—	– 21	—	
STA Bias Voltage	V_{STA}	All Modes	0.65	0.8	0.9	$\times V_R$
MICROPHONE, RECEIVER CONTROLS						
MIC Saturation Voltage	V_{OLMIC}	Speech Mode, I = 500μA	—	50	125	mV
MIC Leakage Current	I_{MICLK}	Dialing Mode, Pin 1 = 3.0V	—	0	5.0	μA
RMT Resistance	R_{RMTSP}	Speech Mode	—	8.0	15	Ω
	R_{RMTDL}	Dialing Mode	5.0	10	18	KΩ
RMT Delay	t_{RMT}	Dialing to Speech	2.0	4.0	20	ms
EQUALIZATION AMPLIFIER						
Gain (V + to EQ)	A_{EQ}					dB
Speech Mode		$@V_{LR} = 0.5V$	—	– 12	—	
Speech Mode		$@V_{LR} = 2.5V$	—	– 2.5	—	
Pulse Mode		$@V_{LR} = 0.2V$	—	– 12	—	
Pulse Mode		$@V_{LR} = 1.0V$	—	– 2.5	—	
EQ Bias Voltage	V_{EQ}					V_{dc}
Speech Mode		$@V_{LR} = 0.5V$	—	0.66	—	
Pulse Mode		$@V_{LR} = 0.5V$	—	1.3	—	
Speech, Pulse Mode		$@V_{LR} = 2.5V$	—	3.3	—	

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
DIALING INTERFACE						
$\overline{MT}$ Input Resistance	H_{MT}		50	100		KΩ
MT Input Resistance			—	50	—	KΩ
$\overline{MT}$, MT Input High Voltage	V_{IHMI}		$V_{DD}-0.3$	—		V_{dc}
$\overline{MT}$, MT Input Low Voltage	V_{ILMT}		—	—	1.0	V_{dc}
MS Input Resistance	R_{MS}		280	600		KΩ
MS Input High Voltage	V_{IHMS}		2.0	—	—	V_{dc}
MS Input Low Voltage	V_{ILMS}		—		0.3	V_{dc}
TI Input Resistance	R_{TI}		—	1.25	—	KΩ
DTMF Gain	A_{DTMF}	See Figure 2 ($V+/V_{IN}$)	3.2	4.8	6.2	dB
LINE INTERFACE						
V+Current (Pin 12 Grounded)	I+					mA
Speech Mode		V+ = 1.7V	4.5	7.1	9.0	
Speech/Pulse Modes		V+ = 12V	5.5	8.4	12.5	
Tone Mode		V+ = 12V	6.0	8.8	14.0	
V+Voltage	V+					V_{dc}
Speech/Pulse Mode		I_L = 20mA	2.6	3.2	3.8	
Speech/Pulse Mode		I_L = 30mA	3.0	3.7	4.4	
Speech/Pulse Mode		I_L = 120mA	7.0	8.2	9.5	
Tone Mode		I_L = 20mA	4.1	4.9	5.7	
Tone Mode		I_L = 30mA	4.5	6.4	6.2	
LR Level Shift	$\triangle V_{LR}$					V_{dc}
Speech/Pulse Mode		V+ − V_{LR}	—	2.7	—	
Tone Mode			—	4.3	—	
LC Terminal Resistance	R_{LC}		36	57	94	KΩ
VOLTAGE REGULATORS						
VR Voltage	V_R	(V+ = 1.7V)	1.1	1.2	1.3	V_{dc}
Load Regulation	$\triangle V_{RLD}$	0mA<I_R<6.0mA	—	20	—	mV
Line Regulation	$\triangle V_{RLE}$	2.0V<V+<6.5V	—	25	—	mV
V_{DD} Voltage	V_{DD}	(V+ = 4.5V)	3.0	3.3	3.8	V_{dd}
Load Regulation (Dialing Mode)	$\triangle V_{DDLD}$	0<I_{DD}<1.6mA	—	0.25	—	V_{dd}
Line Regulation (All Modes)	$\triangle V_{DDLM}$	4.0V<V+<9.0V	—	50	—	mV
Max. Output Current	I_{DDSM}	Speech Mode	375	550	1000	μA
Max Output Current	I_{DDOL}	Dialing Mode	1.6	2.0	3.6	mA
V_{DD} Leakage Current	I_{DDLK}	V+ = 0, V_{DD} = 3.0V		—	1.5	μA

Fig. 1 Test Circuit



PIN DESCRIPTION (See Fig. 1)

No.	Name	Description
1	MIC	Microphone negative supply pin
2	TXI	Transmit amplifier input. Input impedance is 10KΩ
3	TXO	Transmit amplifier output. The AC signal current from this output flows through the V_R series pass transistor via R_9 to drive the line at V+. Increasing R_9 will decrease the signal at V+.
4	STA	Sidetone amplifier output. The signal level at STA increases with loop length.
5	CC	Compensation capacitor. In most applications, CC remains open. A capacitor from CC to GND will compensate the loop length equalization circuit when additional stability is required.
6	EQ	Equalization amplifier output. A portion of the V+ signal is present on this pin to provide negative feedback around the transmit amplifier. The feedback decreases with increasing loop length, causing the AC impedance of the circuit to increase.
7	RXI	Receive amplifier input. Input impedance is>100KΩ.
8	RXO	Receive amplifier output.
9	RMT	Receiver mute.
10	V−	Negative supply.
11	VR	Regulated voltage output. The VR voltage is regulated at 1.2V.
12	LC	AC load capacitor.
13	LR	DC load resistor. This resistor determines the DC resistance of the telephone, and removes power dissipation from the chip.
14	V+	Positive supply.
15	V_{DD}	V_{DD} regulator. V_{DD} is the output of a shunt type regulator with a nomina voltage of 3.3V.
16	TI	DTMF input. Increasing R_7 will reduce the DTMF output levels.
17	MS	Mode select. A logic "I" (>2.0V) selects the pulse dialing mode. A logic "O" (<1.0V) selects the tone dialing mode.
18	$\overline{MT}$	Mute input for KA2425A. $\overline{MT}$ is connected through an internal 100KΩ resistor to the base of an NPN transistor, with the emitter at V_{DD}. A logic "O" (<1.0V) will mute the network for dialing. A logic "I" ($>V_{DD}-0.3V$) puts the KA2425A into the speech mode.
	MT	Mute input for KA2425B. MT is connected through an internal 50KΩ to the base of a NPN transistor, with the collector to the base of a PNP transistor. A logic "I" ($>V_{DD}-0.3V$) will mute the network for dialing. A logic "O" (<1.0V) puts the KA2425B into the speech mode.

Fig. 2 DTMF Driver Test

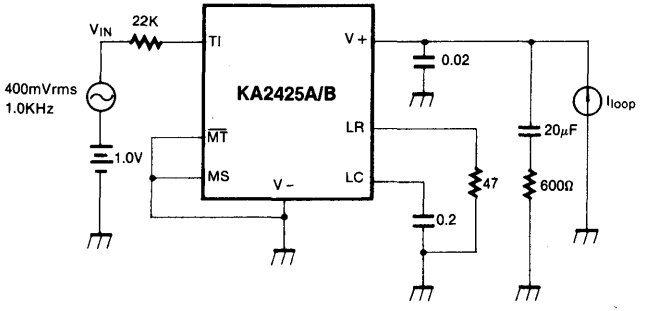


Fig. 3 Transmit and Sidetone Level Test

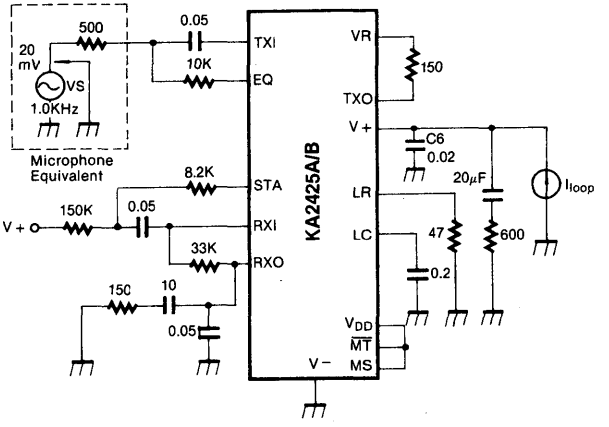
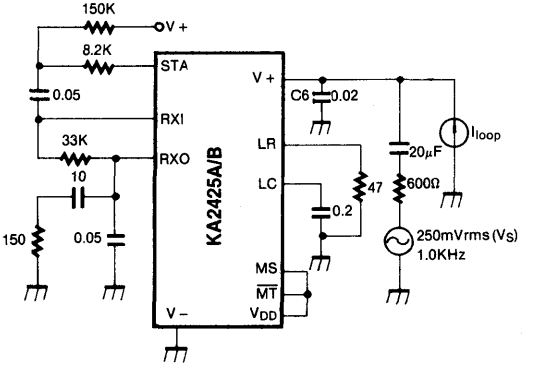


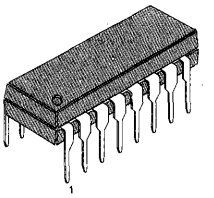
Fig. 4 AC Impedance, Receive and Sidetone Cancellation Test



SPEECH NETWORK WITH DIALER INTERFACE

The KA8500A/B is a telephone speech network integrated circuit which includes transmit amp, receive amp, DTMF amp, voltage regulator, line equalizer, voltage comparator. It handles the voice signal, performing the 2/4 wires interface and changing the gain on both sending and receiving amplifiers to compansate for line attenuation by sensing the line length through the line current.

16 DIP



FEATURES

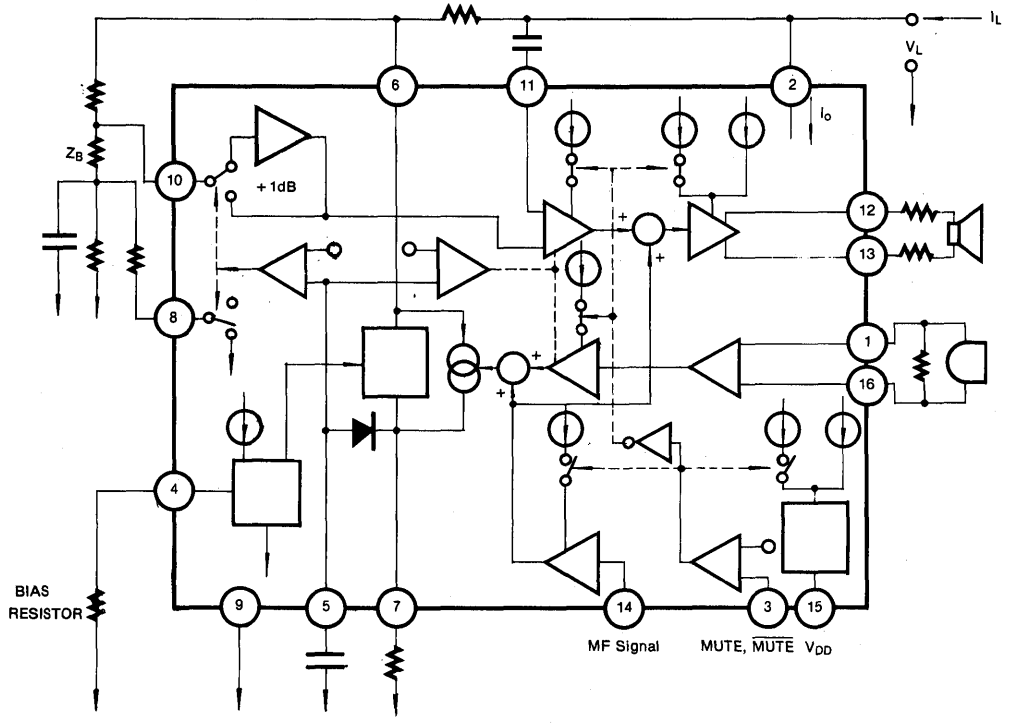
- **Adjusts sending and receiving attenuation length**
- **Regulated voltage for dialer**
- **Linear interface for DTMF**
- **Suitable for ceramic tranducers**
- **Mute function**

ORDERING INFORMATION

Device	Function	Package	Operating Temperature
KA8500AN	MUTE	16 DIP	−45 ~ +70°C
*KA8500BN	$\overline{\text{MUTE}}$		

* Under development

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Line Voltage (3msec max)	V_L	22	V
Forward Line Current	I_{LF}	150	mA
Reverse Line Current	I_{LR}	−150	mA
Power Dissipation (Ta = 70°C)	P_D	1	W
Operating Temperature	T_{opr}	−45 ~ +70	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

3

ELECTRICAL CHARACTERISTICS

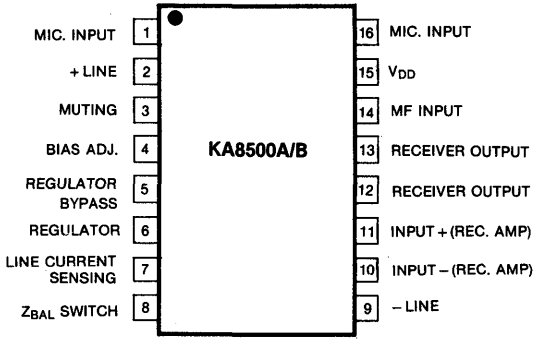
(Refer to the test circuits, S1 and S2 in(a) f = 200 ~ 3400Hz, Ta = −20 ~ +70°C, unless otherwise specified.)

Characteristic	Symbol	Test Condition		Test Fig.	KA8500A/B Min	KA8500A/B Typ	KA8500A/B Max	Unit
Line Voltage	V_L	Ta = 25°C	I_L = 12mA		3.9		4.7	V
			I_L = 20mA				5.5	
			I_L = 80mA				12.2	
Common Mode Rejection Ratio	CMRR	f = 1KHz I_L = 12 ~ 80mA		1	50			dB
Line Matching Impedance	Z_L	V_{RI} = 0.3V, I_L = 12 ~ 80mA f = 1KHz		3	500	600	700	Ω
Sending Gain	G_S	Ta = 25°C f = 1KHz V_{MI} = 2mV	I_L = 25mA	2	48	49	50	dB
			I_L = 52mA		44	45	46	
Sending Gain Flatness	G_{SF}	V_{MI} = 2mV f_{ref} = 1KHz I_L = 12 ~ 80mA		2			±1	dB
Sending Distortion	THD_S	f = 1KHz	V_{SO} = 1V	2			2	%
		I_L = 16 ~ 80mA	V_{SO} = 1.3V				10	
Sending Noise	N_S	V_{MI} = 0V, I_L = 40mA		2			−70	dBmp
Side Tone	ST	Ta = 25°C, f = 1KHz I_L = 25 ~ 52mA, S_1 = b		2			36	dB
Micphone Input Impedence	Z_{IM}	V_{MI} = 2mV, I_L = 12 ~ 80mA			40			KΩ
Sending Loss in MF Operation	SL	V_{MI} = 2mV KA8500A; S2 = b KA8500B; S2 = a	I_L = 25mA	2	−30			dB
			I_L = 52mA		−30			
Receiving Gain	G_R	Ta = 25°C V_{RI} = 0.3V, f = 1KHz	I_L = 25mA	3	7	8	9	dB
			I_L = 52mA		3	4	5	

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic		Symbol	Test Condition			Test Fig.	KA8500A/B Min	KA8500A/B Typ	KA8500A/B Max	Unit
Receiving Gain Flatness		G_{RF}	$V_{RI}=0.3V$, $f_{ref}=1KHz$ $I_L=12\sim80mA$			3			±1	dB
Receiving Distortion		THD_R	f = 1KHz	I_L = 12mA	$V_{RO}=1.6V$	3			2	%
					$V_{RO}=1.9V$				10	
				I_L = 50mA	$V_{RO}=1.8V$				2	
					$V_{RO}=2.1V$				10	
Receiving Noise		N_R	$V_{RI}=0V$, $I_L=12\sim80mA$			3		150		μV
Receiver Output Impedance		R_O	$V_{RO}=50mV$, $I_L=40mA$						100	Ω
MF Supply Voltage		V_{DD}	$I_L=12\sim80mA$				2.4	2.5		V
MF Supply Current	Stand by	I_{DD}	$I_L=12\sim80mA$ KA8500A; S2 = b KA8500B; S2 = a				0.5			mA
	Operation						2			
MF Amplifier Gain		G_{MF}	$I_L=12\sim80mA$ $f_{MF}=1KHz$ $V_{MF}=80mV$			4	15		17	dB
DC Input Voltage Level (pin 14)		V_{IMF}	$V_{MF}=80mV$					$0.3V_{DD}$		V
Input Impedance (pin 14)		Z_{MF}	$V_{MF}=80mV$				60			KΩ
Distortion		THD_{MF}	$V_{MF}=110mV$ $I_L=12\sim80mA$			4			2	%
Starting Delay Time		t_d	$I_L=12\sim80mA$						5	mS
Muting Threshold Voltage (pin 3)		V_{TH}							1	V
							1.6			
Muting Current	Stand by	I_M	$I_L=12\sim80mA$						−10	μA
	Operation		$I_L=12\sim80mA$ KA8500A; S2 = b KA8500B; S2 = a						+10	

CONNECTION DIAGRAM



TEST CIRCUIT

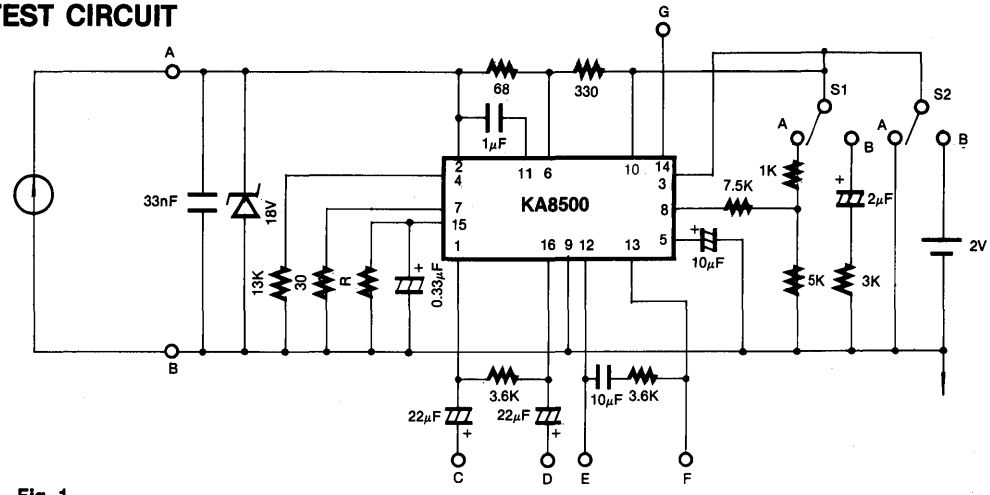
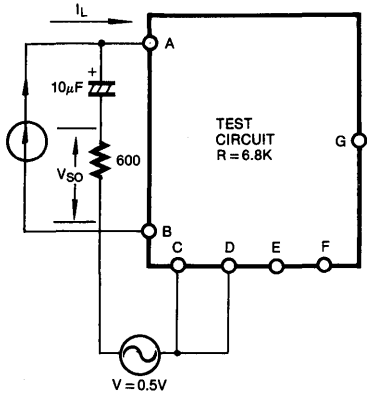


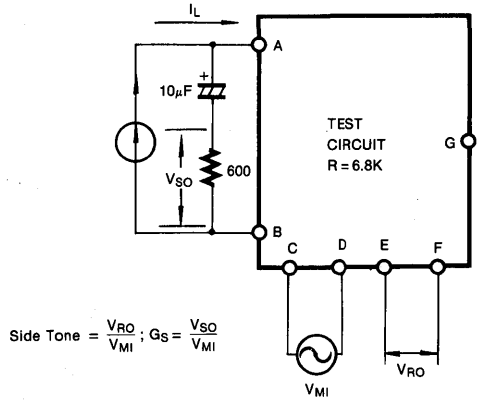
Fig. 1

Fig. 2



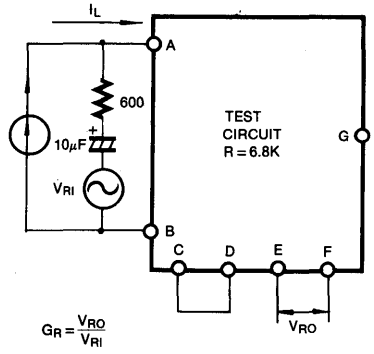
V = 0.5V; CMRR

Fig. 3

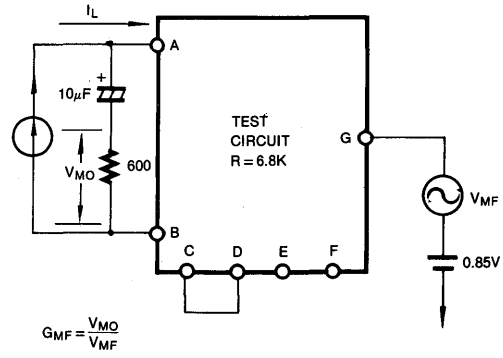


Side Tone = $\frac{V_{RO}}{V_{MI}}$; $G_S = \frac{V_{SO}}{V_{MI}}$

fig. 4



$G_R = \frac{V_{RO}}{V_{RI}}$

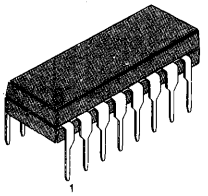


$G_{MF} = \frac{V_{MO}}{V_{MF}}$

SPEECH NETWORK WITH DIALER INTERFACE

The KA8501A/B is a telephone speech network integrated circuit which includes transmit amp, receive amp, DTMF amp, voltage regulator, line equalizer, voltage comparator. It handles the voice signal, performing the 2/4 wires interface and changing the gain on both sending and receiving amplifiers to compansate the line current. The KA8501A/B can work in fixed gain mode.

16 DIP



FEATURES

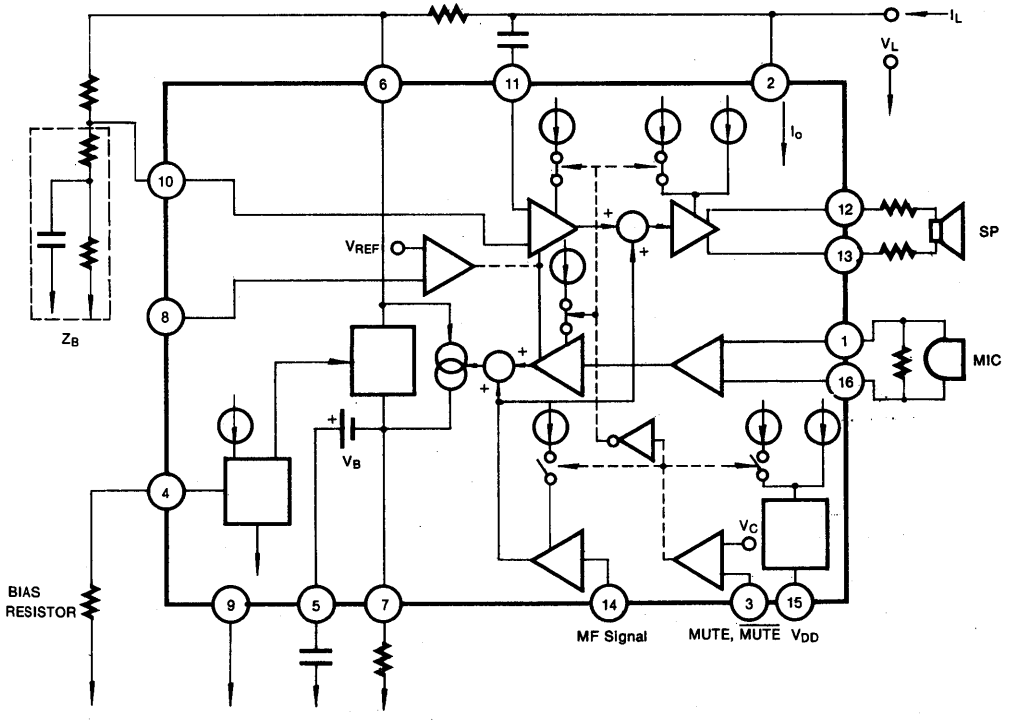
- **Adjusts sending and receiving attenuation length**
- **Regulated voltage for dialer**
- **Linear interface for DTMF**
- **Suitable for ceramic tranducers**
- **Mute function**

ORDERING INFORMATION

Device	Function	Package	Operating Temperature
KA8501AN	MUTE	16 DIP	−45 ~ +70°C
*KA8501BN	$\overline{\text{MUTE}}$		

* Under development

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Line Voltage (3msec max)	V_L	22	V
Forward Line Current	I_{LF}	150	mA
Reverse Line Current	I_{LR}	−150	mA
Power Dissipation (Ta = 70°C)	P_D	1	W
Operating Temperature	T_{opr}	−45 ~ +70	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

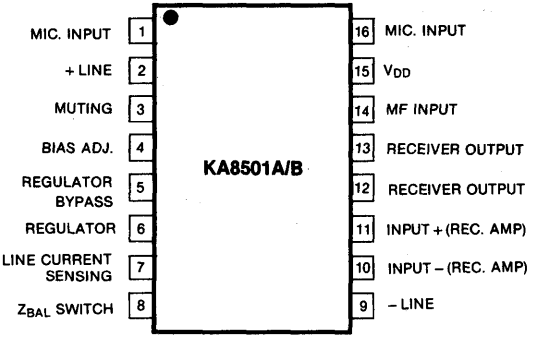
(Refer to the test circuits, S1 and S2 in(a) f = 200 ~ 3400Hz, Ta = −20 ~ +70°C, unless otherwise specified.)

Characteristic	Symbol	Test Condition		Test Fig.	KA8501A/B Min	KA8501A/B Typ	KA8501A/B Max	Unit
Line Voltage	V_L	Ta = 25°C	I_L = 12mA		3.9		4.7	V
			I_L = 20mA				5.5	
			I_L = 80mA				12.2	
Common Mode Rejection Ratio	CMRR	f = 1KHz I_L = 12 ~ 80mA		1	50			dB
Line Matching Impedance	Z_L	V_{RI} = 0.3V, I_L = 12 ~ 80mA f = 1KHz		3	500	600	700	Ω
Sending Gain	G_S	Ta = 25°C f = 1KHz V_{MI} = 2mV	I_L = 25mA	2	48	49	50	dB
			I_L = 52mA		44	45	46	
		S3 in(B) I_L = 25 ~ 52mA			48	49	50	
Sending Gain Flatness	G_{SF}	V_{MI} = 2mV f_{ref} = 1KHz I_L = 12 ~ 80mA		2			±1	dB
Sending Distortion	THD_S	f = 1KHz	V_{SO} = 1V	2			2	%
		I_L = 16 ~ 80mA	V_{SO} = 1.3V				10	
Sending Noise	N_S	V_{MI} = 0V, I_L = 40mA					−70	dBmp
Side Tone	ST	Ta = 25°C, f = 1KHz I_L = 25 ~ 52mA, S_1 = b		2			36	dB
Micphone Input Impedence	Z_{IM}	V_{MI} = 2mV, I_L = 12 ~ 80mA			40			KΩ
Sending Loss in MF Operation	SL	V_{MI} = 2mV KA8501A; S2 = b KA8501B; S2 = a	I_L = 25mA	2	−30			dB
			I_L = 52mA		−30			
Receiving Gain	G_R	Ta = 25°C V_{RI} = 0.3V, f = 1KHz	I_L = 25mA	3	7	8	9	dB
			I_L = 52mA		2.5	3.5	4.5	
		S3 in(B) I_L = 25 ~ 52mA			7	8	9	

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic		Symbol	Test Condition			Test Fig.	KA8501A/B Min	KA8501A/B Typ	KA8501A/B Max	Unit
Receiving Gain Flatness		G_{RF}	$V_{RI}=0.3V$, $f_{ref}=1KHz$ $I_L=12\sim80mA$			3			±1	dB
Receiving Distortion		THD_R	$f=$ 1KHz	$I_L=$ 12mA	$V_{RO}=1.6V$	3			2	%
					$V_{RO}=1.9V$				10	
				$I_L=$ 50mA	$V_{RO}=1.8V$				2	
					$V_{RO}=2.1V$				10	
Receiving Noise		N_R	$V_{RI}=0V$, $I_L=12\sim80mA$			3			100	μV
Receiver Output Impedance		R_O	$V_{RO}=50mV$, $I_L=40mA$						100	Ω
MF Supply Voltage		V_{DD}	$I_L=12\sim80mA$				2.4	2.5		V
MF Supply Current	Stand by	I_{DD}	$I_L=12\sim80mA$ KA8501A; S2 = b KA8501B; S2 = a				0.5			mA
	Operation						2			
MF Amplifier Gain		G_{MF}	$I_L=12\sim80mA$ $f_{MF}=1KHz$ $V_{MF}=80mV$			4	15		17	dB
DC Input Voltage Level (pin 14)		V_{IMF}	$V_{MF}=80mV$					$0.3V_{DD}$		V
Input Impedance (pin 14)		Z_{MF}	$V_{MF}=80mV$				40			KΩ
Distortion		THD_{MF}	$V_{MF}=110mV$ $I_L=12\sim80mA$			4			2	%
Starting Delay Time		t_d	$I_L=12\sim80mA$						5	mS
Muting Threshold Voltage (pin 3)		V_{TH}							1	V
							1.6			
Muting Current	Stand by	I_M	$I_L=12\sim80mA$						−10	μA
	Operation		$I_L=12\sim80mA$ KA8501A; S2 = b KA8501B; S2 = a						+10	

CONNECTION DIAGRAM



TEST CIRCUIT

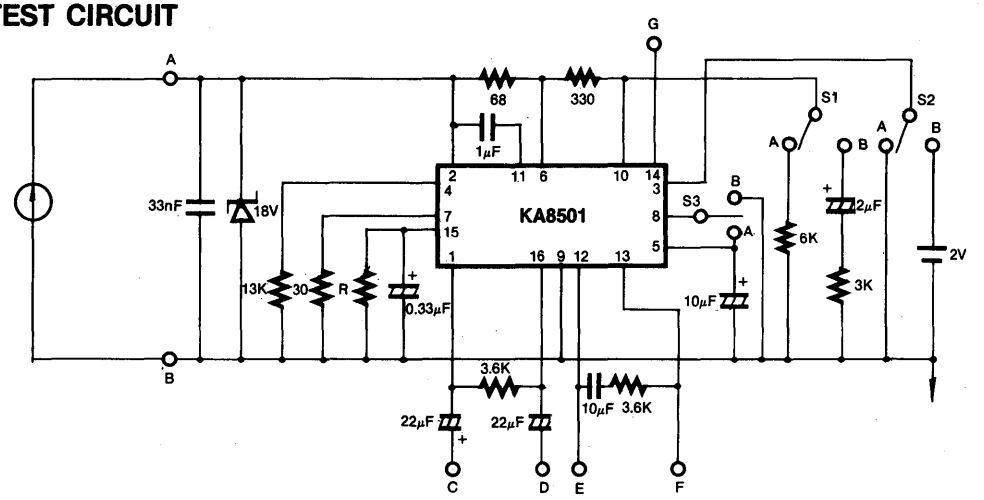


Fig. 1

Fig. 2

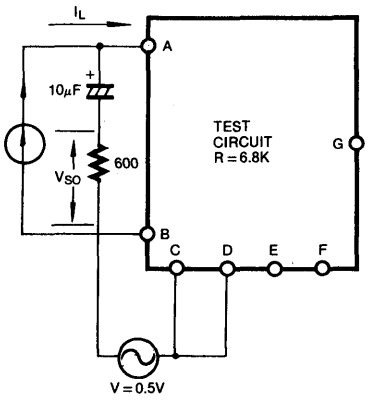


Fig. 3

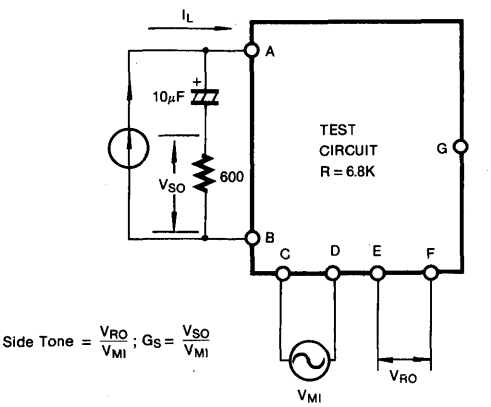
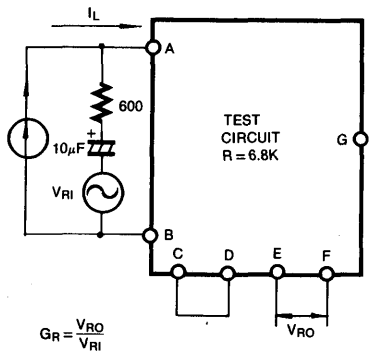
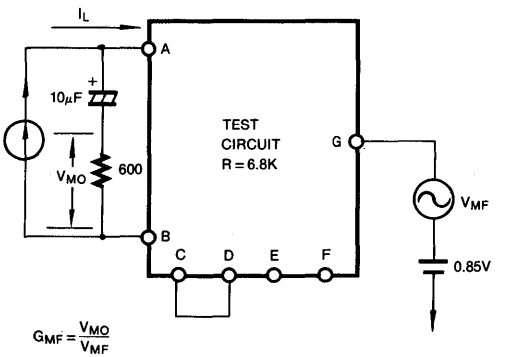


fig. 4

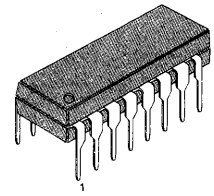




SPEECH NETWORK WITH DIALER INTERFACE

The KA8502A/B is a telephone speech network integrated circuit which includes transmit amp, receive amp, DTMF amp, voltage regulator, line equalizer, voltage comparator. It handles the voice signal, performing the 2/4 wires interface and changing the gain on both sending and receiving amplifiers to compansate for line attenuation by sensing the line length through the line current. The KA8502A/B can work in fixed gain mode.

16 DIP



FEATURES

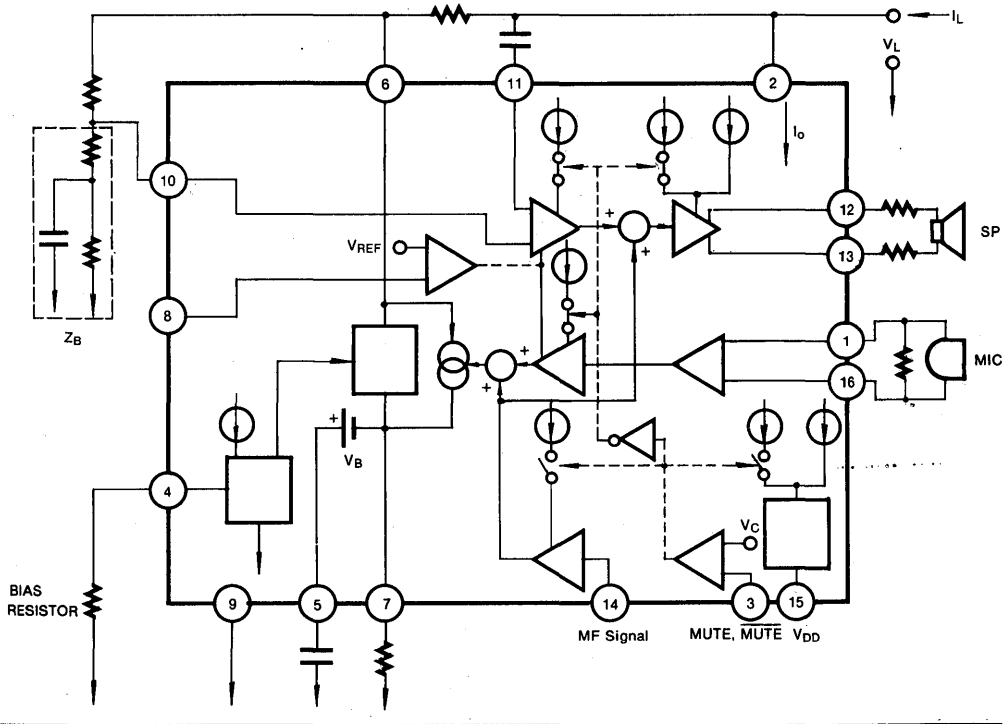
- **Adjusts sending and receiving attenuation length**
- **Regulated voltage for dialer**
- **Linear interface for DTMF**
- **Suitable for ceramic tranducers**
- **Mute function**

ORDERING INFORMATION

Device	Function	Package	Operating Temperature
*KA8502AN	MUTE	16 DIP	−45~ +70°C
*KA8502BN	$\overline{\text{MUTE}}$		

* Under Development

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Line Voltage (3msec max)	V_L	22	V
Forward Line Current	I_{LF}	150	mA
Reverse Line Current	I_{LR}	−150	mA
Power Dissipation (Ta=70°C)	P_D	1	W
Operating Temperature	T_{opr}	−45~+70	°C
Storage Temperature	T_{stg}	−65~+150	°C

ELECTRICAL CHARACTERISTICS

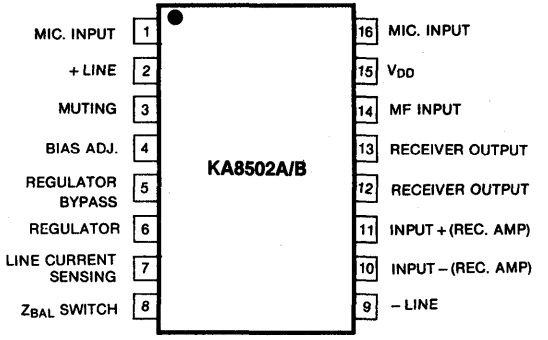
(Refer to the test circuits, S1 and S2 in(a) V_G=1~2V, I_L=12~80mA, f=200~3400Hz, Ta=−20~+70°C, unless otherwise specified.)

Characteristic	Symbol	Test Condition		Test Fig.	KA8502A/B Min	KA8502A/B Typ	KA8502A/B Max	Unit
Line Voltage	V_L	Ta=25°C	I_L=12mA		3.65		4.5	V
			I_L=20mA				5.0	
			I_L=80mA				10.0	
Common Mode Rejection Ratio	CMRR	f=1KHz I_L=12~80mA		1	50			dB
Line Matching Impedance	Z_L	V_{RI}=0.3V, I_L=12~80mA f=1KHz		3	500	600	700	Ω
Sending Gain	G_S	Ta=25°C f=1KHz V_{MI}=2mV	V_G=2V	2	44.5	45.5	46.5	dB
			V_G=1V		48.5	49.5	50.5	
Sending Gain Flatness	G_{SF}	V_{MI}=2mV f_{ref}=1KHz I_L=12~80mA		2			±1	dB
Sending Distortion	THD_S	f=1KHz	V_{SO}=775mV	2			2	%
		I_L=16	V_{SO}=900mV				10	
Sending Noise	N_S	V_{MI}=0V, V_G=1V		2		−71	−69	dBmp
Side Tone	ST	Ta=25°C, f=1KHz S_1=b		2			36	dB
Micphone Input Impedence	Z_{IM}	V_{MI}=2mV,			40			KΩ
Receiving Gain	G_R	Ta=25°C V_{RI}=0.3V, f=1KHz	V_G=2V	3	−5		−3	dB
			V_G=1V		−0.5		1.5	

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic		Symbol	Test Condition		Test Fig.	KA8502A/B Min	KA8502A/B Typ	KA8502A/B Max	Unit
Receiving Gain Flatness		G_{RF}	$V_{RI}=0.3V$, $f_{ref}=1KHz$ $I_L=12\sim80mA$		3			±1	dB
Receiving Distortion		THD_R	$f=1KHz$	$V_{RO}=400mV$	3			2	%
				$V_{RO}=450mV$				5	
Receiving Noise		N_R	$V_{RI}=0V$, $I_L=12\sim80mA$		3		100	200	μV
Receiver Output Impedance			$V_{RO}=50mV$,				30		Ω
MF Supply Voltage		V_{DD}	$I_L=12\sim80mA$			2.4	2.5	2.7	V
MF Supply Current	Stand by	I_{DD}	$I_L=12\sim80mA$ KA8502A; S2 = b KA8502B; S2 = a			0.5			mA
	Operation					2			
MF Amplifier Gain		G_{MF}	$I_L=12\sim80mA$ $f_{MF}=1KHz$ $V_{MF}=80mV$		4	15		17	dB
DC Input Voltage Level (pin 14)		V_{IMF}	$V_{MF}=80mV$				$0.3V_{DD}$		V
Input Impedance (pin 14)		Z_{MF}	$V_{MF}=80mV$			60			KΩ
Distortion		THD_{MF}	$V_{MF}=110mV$ $I_L=12\sim80mA$		4			2	%
Starting Delay Time		t_d	$I_L=12\sim80mA$					5	mS
Muting Threshold Voltage (pin 3)		V_{TH}						1	V
						1.6			
Muting Current	Stand by	I_M	$I_L=12\sim80mA$					−10	μA
	Operation		$I_L=12\sim80mA$ KA8502A; S2 = b KA8502B; S2 = a					+10	
Input Current (pin 8)		I_8						−10	μA

CONNECTION DIAGRAM



TEST CIRCUIT

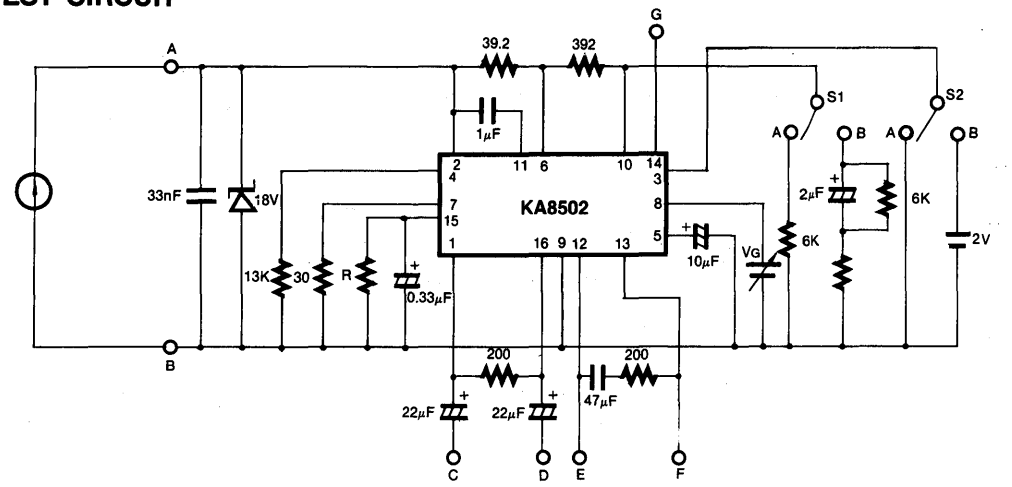


Fig. 1

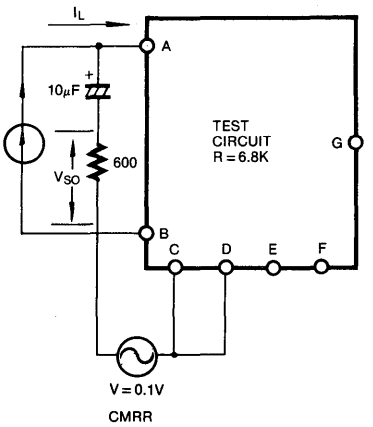
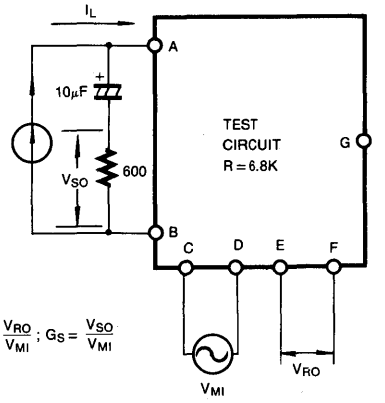


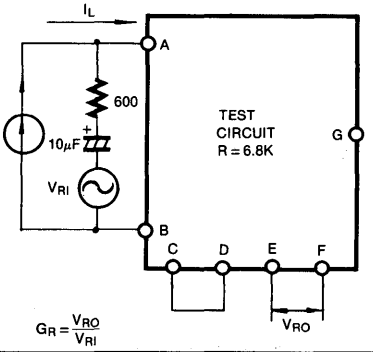
Fig. 3

Fig. 2

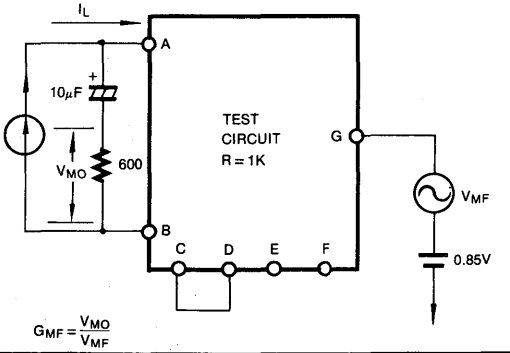


Side Tone = $\frac{V_{RO}}{V_{MI}}$; $G_S = \frac{V_{SO}}{V_{MI}}$

fig. 4



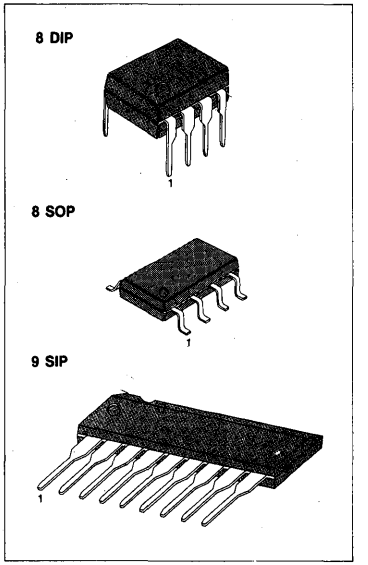
$G_R = \frac{V_{RO}}{V_{RI}}$



$G_{MF} = \frac{V_{MO}}{V_{MF}}$

LOW VOLTAGE AUDIO AMPLIFIER

The KA8602 is the audio power amplifier available for low voltages. This supplies differential outputs for maximizing output swing at low voltages. KA8602 doesn't need coupling capacitors to the speaker. The gain of this amp is controlled easily by two external resistors.



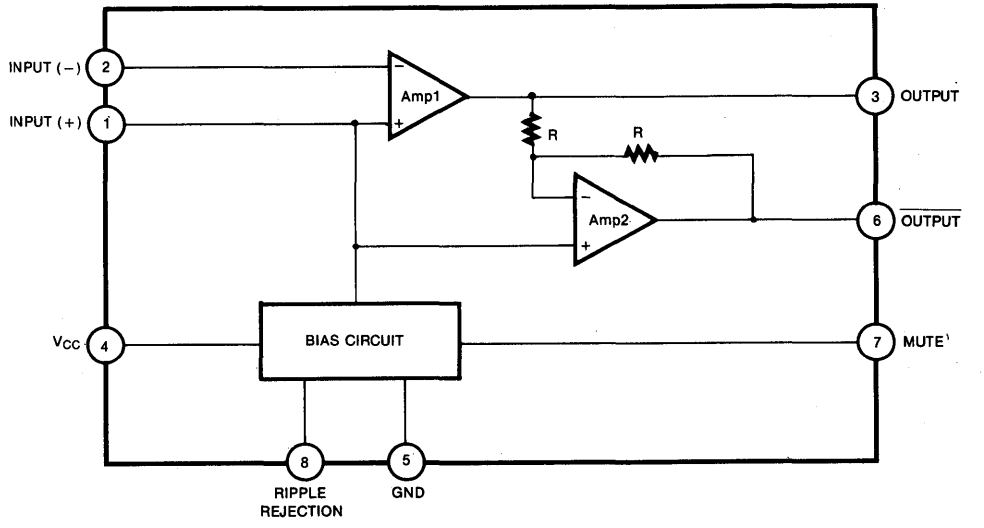
FEATURES

- **Wide Supply Voltage (2~16V)**
- **Low Quiescent Supply Current (I_{CC} = 2.7mA: Typ)**
- **Easy Gain Control**
- **Medium Output Power**
  P_O = 250mW at V_{CC} = 6V, R_L = 32Ω, THD = 10%
- **Minimum External Parts**
- **Load Impedance Range (8Ω~100Ω)**
- **Low Distortion**
- **Mute Function (I_{CC} = 65μA: Typ)**

ORDERING INFORMATION

Device	Package	Operating Temperature
*KA8602N	8DIP	−20~+70°C
*KA8602D	8SOP	
*KA8602S	9SIP	

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{CC}	−1.0 ~ +18	V
Output Current (output pin)	I_O	±250	mA
Maximum Voltage (input, RR, Mute pin)	V_{IR}	−1.0 ~ V_{CC} +1.0	V
Applied Output Voltage (output pin) when disabled	V_{OR}	−1.0 ~ V_{CC} +1.0	V
Junction Temperature	T_j	−55 ~ +140	°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	+2.0		+16	V
Load Impedance	R_L	8		100	Ω
Peak Load Current	I_{LP}			±200	mA
Differential Gain (5KHz Bandwidth)	A_{VD}	0		46	dB
Voltage at Mute (Pin 7)	V_M	0		V_{CC}	V
Ambient Temperature	T_a	−20		+70	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 6V, Ta = 25°C, unless otherwise noted)

Characteristics		Symbol	Test Condition		Min	Typ	Max	Unit
DC ELECTRICAL CHARACTERISTICS								
Power Supply Current ($R_L = \infty$)		I_{CC}	V_{CC} = 3.0V, Mute = 0.8V V_{CC} = 16V, Mute = 0.8V			2.7 3.3	4.0 5.0	mA
			V_{CC} = 3.0V, Mute = 2.0V			65	100	μA
Output Voltage (output pin)		V_O	R_L = 16Ω R_f = 75KΩ	V_{CC} = 3.0V V_{CC} = 6.0V V_{CC} = 12.0V	1.0	1.15 2.65 5.65	1.25	V
Output Offset Voltage		$\triangle V_O$	V_{CC} = 6.0V, R_f = 75KΩ, R_L = 32Ω		−30	0	+30	mV
Output High Level		V_{OH}	2.0V ≤ V_{CC} ≤ 16V, I_{out} = −75mA			V_{CC} − 1.0		V
Output Low Level		V_{OL}	2.0V ≤ V_{CC} ≤ 16V, I_{out} = 75mA			0.16		V
Input Bias Current (pin 2)		I_{IB}				−100	−200	nA
Equivalent Resistance		R_E	pin 1 pin 8		100 18	150 25	220 40	KΩ
Mute	Input Low Voltage	V_{IL}					0.8	V
	Input High Voltage	V_{IH}			2.0			V
	Input Resistance	R_I	V_{CC} = Mute = 16V		50	90	175	KΩ

ELECTRICAL CHARACTERISTICS

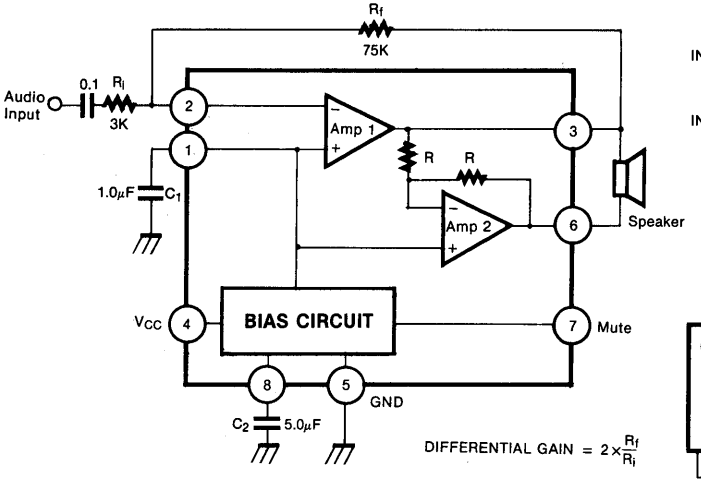
(V_{CC} = 6V, Ta = 25°C, unless otherwise noted)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
AC ELECTRICAL CHARACTERISTICS						
Open Loop Gain (Amp 1)	A_{OL}		80			dB
Closed Loop Gain (Amp 2)	A_{CL}	f = 1.0KHz, R_L = 32Ω	−0.35	0	+0.35	dB
Output Power	P_O	V_{CC} = 3.0V, R_L = 16Ω, THD≤10% V_{CC} = 6.0V, R_L = 32Ω, THD≤10% V_{CC} = 12V, R_L = 100Ω, THD≤10%	55 250 400			mW
Total Harmonic Distortion (f = 1.0KHz)	THD	V_{CC} = 6.0V, R_L = 32Ω, P_O = 125mW V_{CC}≥3.0V, R_L = 8Ω, P_O = 20mW V_{CC}≥12V, R_L = 32Ω, P_O = 200mW		0.5 0.5 0.6	1.0	%
Gain Bandwidth Product	GBP			1.5		MHz
Power Supply Rejection (V_{CC} = 6.0V, △V_{CC} = 3.0V)	PSRR	C_1 = ∞, C_2 = 0.01μF C_1 = 0.1μF, C_2 = 0, f = 1.0KHz C_1 = 1.0μF, C_2 = 5.0μF, f = 1.0KHz	50	 12 52		dB
Muting	GMT	Mute = 2.0V, 1.0KHz≤f≤20KHz		>70		dB

PIN DESCRIPTION

Pin No.	Name	Function
1	Input (+)	Analog Ground for the amplifiers. A 1.0μF capacitor at this pin (with a 5.0μF capacitor at pin 8) provides 52dB (Typ) of power supply rejection. Turn-on time of the circuit is affected by the capacitor on this pin. This pin can be used as an alternate input.
2	Input (−)	Amplifier input. The input capacitor and resistor set low frequency rolloff and input impedance. The feedback resistor is connected to this pin and output.
3	Output	Amplifier 1's output. The DC Level is≈ (V_{CC} − 0.7V)/2
4	V_{CC}	DC supply voltage (+2.0 ~ +16V) is applied to this pin.
5	GND	Ground pin.
6	$\overline{\text{Output}}$	Amplifier 2's output. This signal is equal in amplitude, but 180° out of phase with that at output pin. The DC level is ≈(V_{CC} − 0.7V)/2.
7	Mute	This pin can be used to power down the IC to conserve power, or for muting, or both. When at a logic "Low" (0 to 0.8 volts), the KA8602 is enabled for normal operation. When at a logic "High" (2.0 to V_{CC} volts), the IC is disabled. If Mute is open, that is equivalent to a logic "Low".
8	Ripple Rejection	A capacitor at this pin increases power supply rejection, and affects turn-on time. This pin can be left open if the capacitor at pin 1 is sufficient.

TYPICAL APPLICATION CIRCUIT



PIN CONFIGURATION

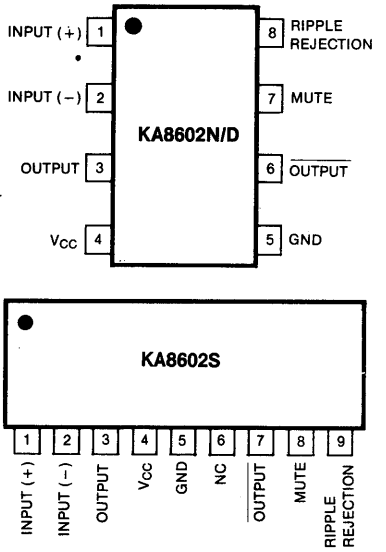


Fig. 1 AUDIO AMPLIFIER (HIGH INPUT IMPEDANCE)

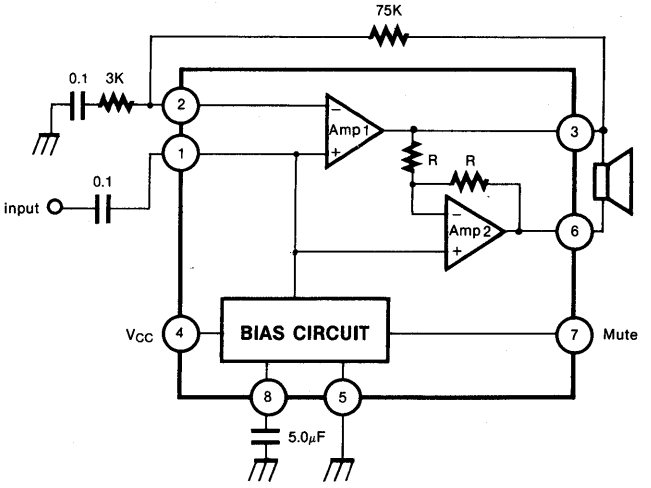


Fig. 2 DUAL SUPPLY OPERATION

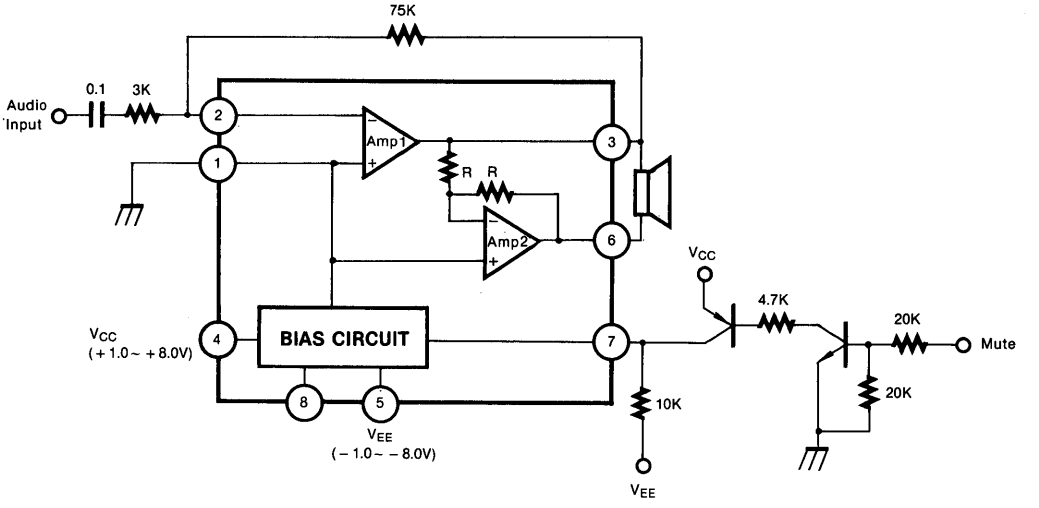


Fig. 3 AUDIO AMPLIFIER (BASS SUPPRESSION)

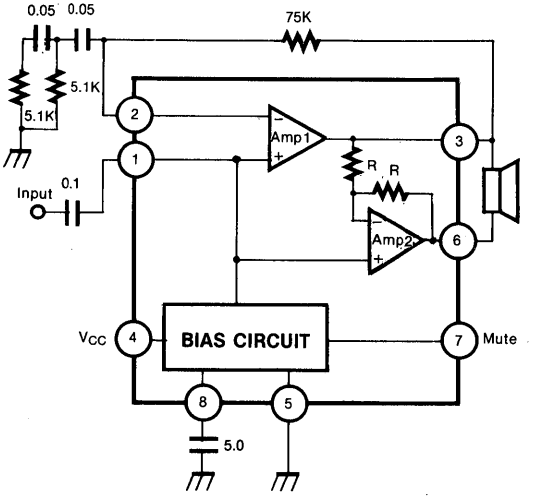


Fig. 4 AUDIO AMPLIFIER (BANDPASS)

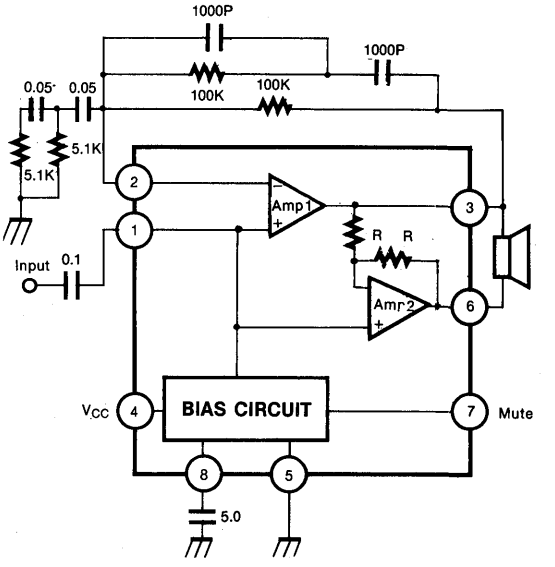


Fig. 5 FREQUENCY RESPONSE OF Fig. 3

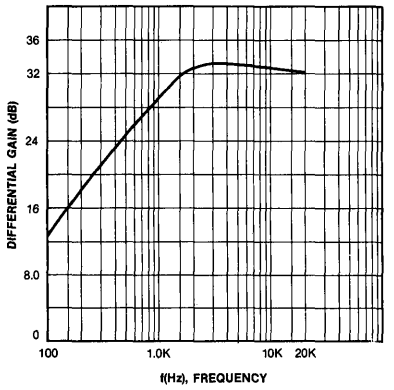


Fig. 6 FREQUENCY RESPONSE OF Fig. 4

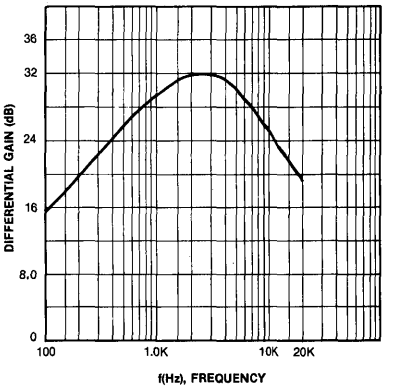


Fig. 7 OPEN LOOP GAIN & PHASE (AMP 1)

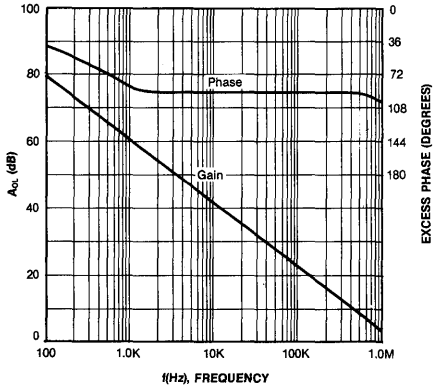


Fig. 8 DIFFERENTIAL GAIN vs FREQUENCY

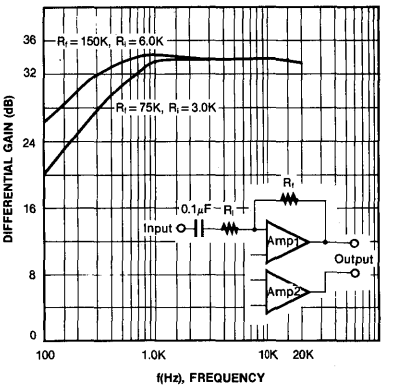


Fig. 9 POWER SUPPLY CURRENT

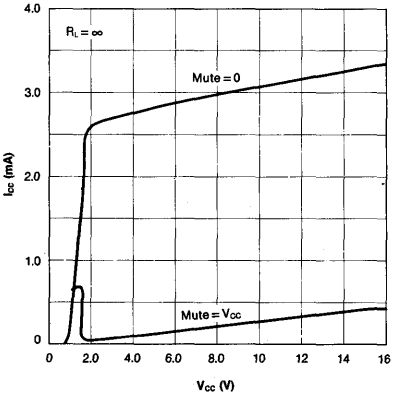


Fig. 10 MAXIMUM ALLOWABLE LOAD POWER

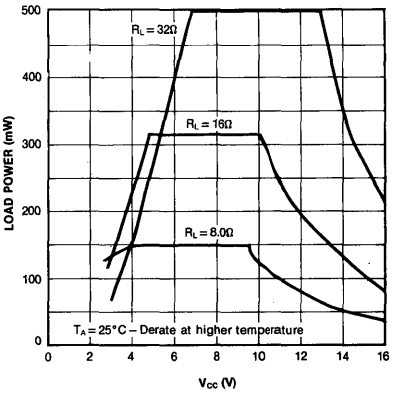


Fig. 11 PSRR vs FREQUENCY ($C_2 = 10\mu F$)

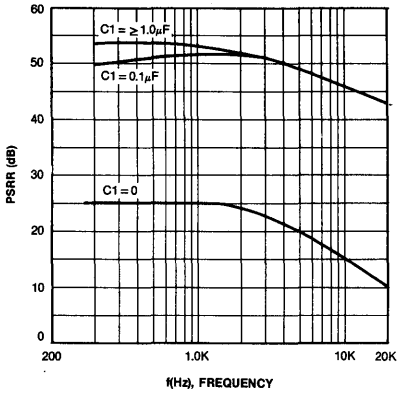


Fig. 12 PSRR vs FREQUENCY ($C_2 = 5.0\mu F$)

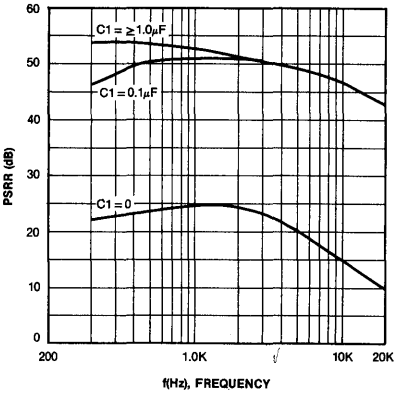


Fig. 13 PSRR vs FREQUENCY ($C_2 = 1.0\mu F$)

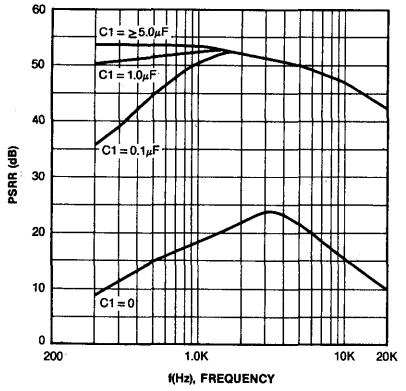


Fig. 14 PSRR vs FREQUENCY ($C_2 = 0$)

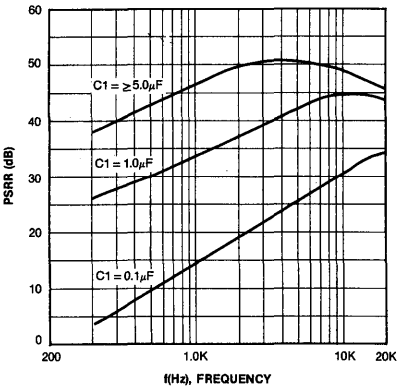


Fig. 15 V_{CC}-V_{OH} vs LOAD CURRENT

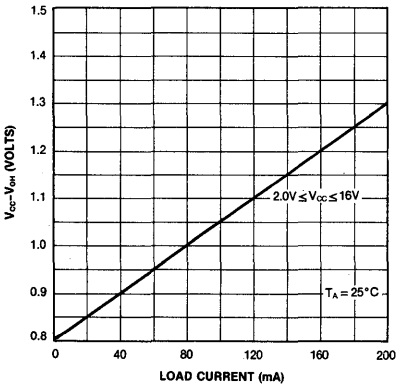


Fig. 16 V_{OL} vs LOAD CURRENT

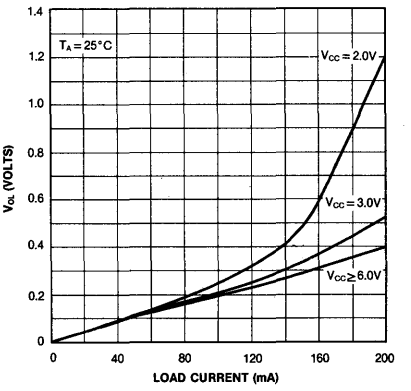


Fig. 17 POWER DISSIPATION (8Ω LOAD)

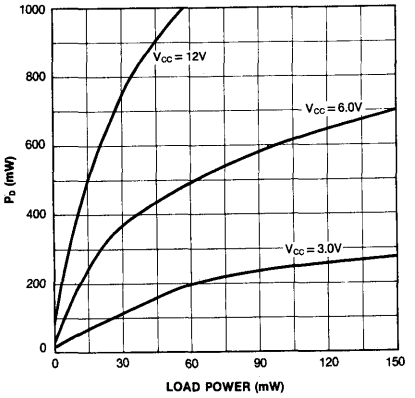


Fig. 18 POWER DISSIPATION (16Ω LOAD)

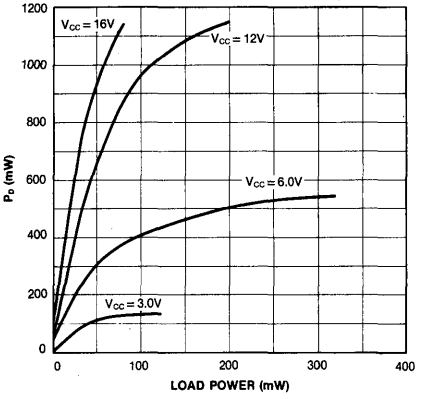


Fig. 19 POWER DISSIPATION (32Ω LOAD)

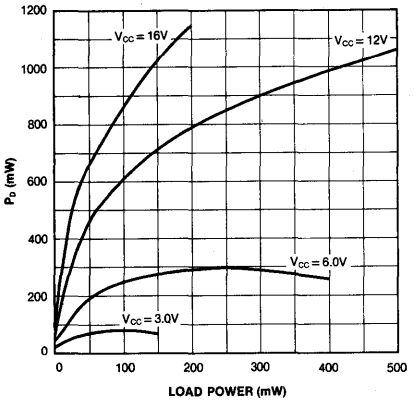


Fig. 20 DISTORTION vs POWER
(f = 1KHz, A_{VD} = 34dB)

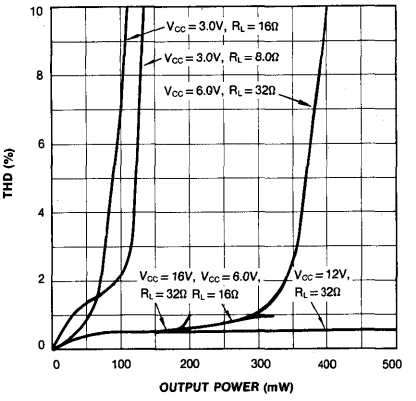


Fig. 21 DISTORTION vs POWER
(f = 3KHz, A_{VD} = 34dB)

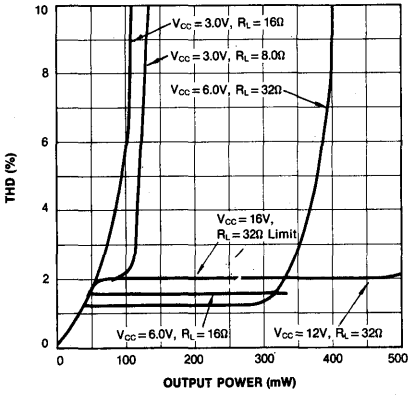
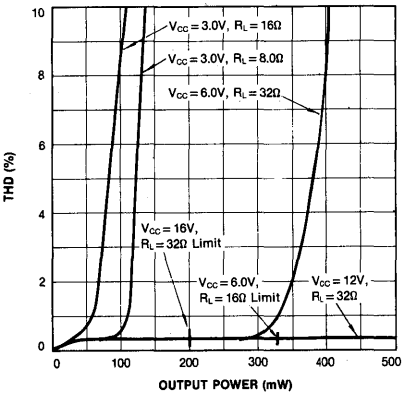
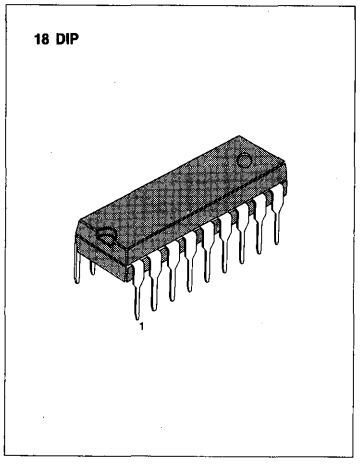


Fig. 22 DISTORTION vs POWER
(f = 1,3KHz, A_{VD} = 12dB)



TELEPHONE PULSE DIALER WITH REDIAL

The KS5805A/B is a monolithic CMOS integrated circuit and provides all the features required for implementing a pulse dialer with redial.



FUNCTIONS

- $\overline{\text{Mute}}$ output logic "0"
- $\overline{\text{Pulse}}$ output logic "0"
- RC oscillation for reference frequency
- Designed to operate directly from the telephone line
- Used CMOS technology for low voltage, low power operation
- Power up clear circuitry
- KS5805A pin 2: V_{REF}
- KS5805B pin 2: Tone out

FEATURES

- **Uses either a standard 2 of 7 matrix keyboard with negative true common or the inexpensive form A-type keyboard**
- **Make/Break ratio can be selected**
- **Redial with * or #**
- **Continuous $\overline{\text{MUTE}}$**
- **Tone signal output or on-chip reference voltage by bonding option on chip**
- **10 pps/20 pps can be selected**

ORDERING INFORMATION

Device	Package	Function	Operating Temperature
KS5805AN	18 DIP	Pin 2 = V_{ref}	−30 ~ +60°C
KS5805BN	18 DIP	Pin 2 = Tone Out	

TEST CIRCUIT

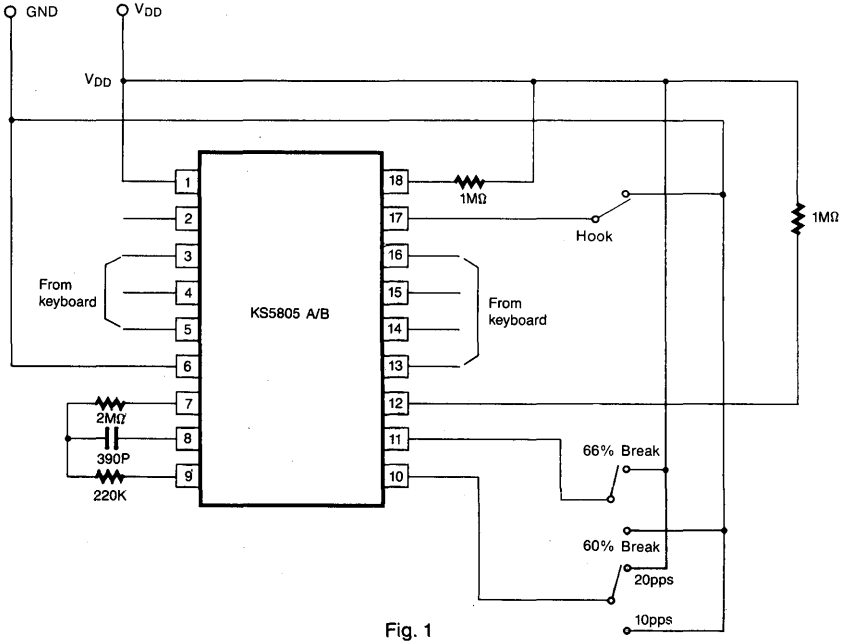


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	6.2	V
Voltage on Any Pin	V_{IN}	V_{DD} +0.3, Gnd−0.3	V
Power Dissipation	P_D	500.0	mW
Operating Temperature	Topr	−30 ~ +60	°C
Storage Temperature	Tstg	−65 ~ +150	°C

DC ELECTRICAL CHARACTERISTICS

(T_a = 25°C unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{DD}		2.5		6.0	V	
Key Contract Resistance	R_{KI}				1	KΩ	1
Keyboard Capacitance	C_{KI}				30	pF	
Key Input Voltage	K_{IH}	2 of 7 input mode	0.8V_{DD}		V_{DD}	V	1
	K_{IL}		Gnd		0.2V_{DD}		
Key Pull-Up Resistance	K_{IRU}	V_{DD} = 6.0V		100		KΩ	
Key Pull-Down Resistance	K_{IRD}	V_{IN} = 4.8V		4.0		KΩ	
Mute Sink Current	I_M	V_{DD} = 2.5V V_O = 0.5V	500			μA	2
Pulse Output Sink Current	I_P	V_{DD} = 2.5V V_O = 0.5V	1.0			mA	3
Tone Output Sink Current	I_{TL}	V_{DD} = 2.5V V_O = 0.5V	250			μA	4
Tone Output Source Current	I_{TH}	V_{DD} = 2.5V V_O = 0.5V	250			μA	4
Memory Retention Current	I_{MR}	All outputs under no load		0.7		μA	6
Operating Current	I_{OD}	All outputs under no load		100	150	μA	
Mute or Pulse Off Leakage	I_{LKG}	V_{DD} = 6.0V V_O = 6.0V		0.001	1.0	μA	2.3
V_{REF} Output Source Current	I_{REF}	$V_{DD} - V_{REF}$ = 6.0V	1.0	7.0		mA	5

Note 1) Applies to key input pin. (R_1-R_4, C_1-C_3)
2) Applies to MUTE output in.
3) Applies to PULSE output pin.
4) Applies to TONE pin (KS5805B)
5) Applies to V_{REF} pin (KS5805A)
6) Current necessary for memory to be maintained. All outputs unloaded.

* Typical values are to be used as a design aid and are not subject to production testing.

AC ELECTRICAL CHARACTERISTICS (T_a =25°C)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
Oscilator Frequency	F_{OSC}		4		KHz	1
Key Input Debounce Time	T_{DB}		10		ms	3,4
Key Down Time for Valid Entry	T_{KD}	40			ms	4,5
Key Down Time During Two-Key Roll Over	t_{KR}	5			ms	4
Oscillator Stat-Up Time (V_{DD} = 2.5V)	t_{os}		1		ms	
Mute Valid After Last Outpulse	t_{MO}		5		ms	3,4
Pulse Output Pulse Rate	P_R		10		PPS	2
On-Hook Time Required to Clear Memory	t_{OH}	300			ms	4
Pre-Digital Pause	T_{PDP}		800		ms	3,4
Inter-Digital Pause	T_{IDP}		800		ms	3,4
Frequency Stability V_{DD} = 2.5 ~ 3.5V	Δf		±4		%	
Frequency Stability V_{DD} = 3.5 ~ 6.0V	Δf		±4		%	
Tone Output Frequency	F_{TONE}		1		KHz	4,6

Note: 1) R_S =2MΩ, R=220KΩ, C=390pF.
2) If pin 10 is tied to V_{CC}, the output pulse rate will be 20pps.
3) If the 20pps option is selected, the time will be 1/2 these shown.
4) These times are directly proportional to the oscillator frequency.
5) Debounce plus oscillator start-up time ≤ 40ms.
6) If the 20pps option is selected, the tone output frequency will be 2KHz. (KS5805B ONLY)

PIN CONNECTIONS

Pin 1: V_{DD}
Pin 2: V_{ref} (KS5805A)/Pacifier tone (KS5805B)
Pin 3: $\overline{\text{Column 1}}$
Pin 4: $\overline{\text{Column 2}}$
Pin 5: $\overline{\text{Column 3}}$
Pin 6: GND
Pin 7: RC Oscillator
Pin 8: RC Oscillator
Pin 9: RC Oscillator
Pin 10: 10/20pps Select
Pin 11: $\overline{\text{Make}}$/Break Select
Pin 12: $\overline{\text{Mute}}$ Output
Pin 13: $\overline{\text{ROW 4}}$
Pin 14: $\overline{\text{ROW 3}}$
Pin 15: $\overline{\text{ROW 2}}$
Pin 16: $\overline{\text{ROW 1}}$
Pin 17: On-$\overline{\text{Hook}}$/Test
Pin 18: $\overline{\text{Pulse}}$ Output

TIMING CHARACTERISTICS

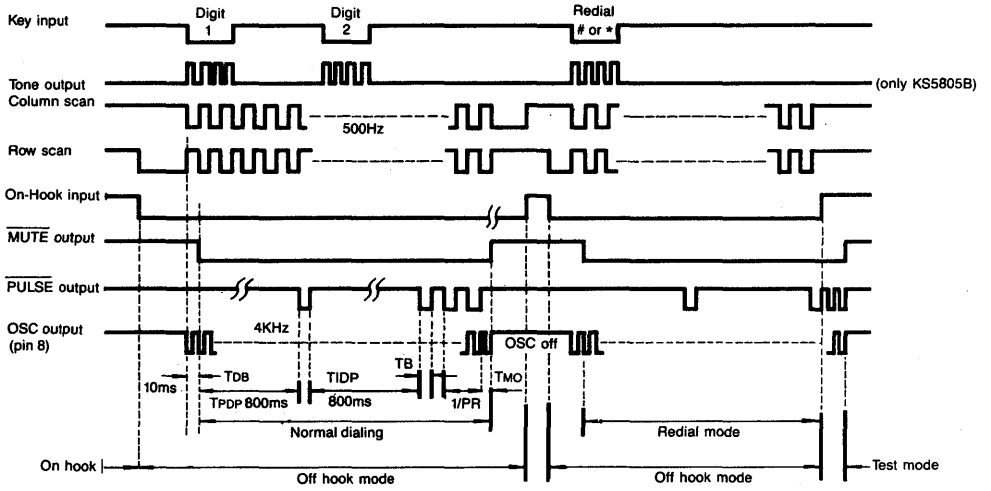


Fig. 2

PIN DESCRIPTIONS

1. V_{DD} (Pin 1)

This is the positive supply pin. The voltage on this pin is measured relative to Pin 6 and is supplied from a 150μA current source. This voltage should be regulated to less than 6.0 volts using on external form or regulation.

2. Tone signal output/V_{REF} (Pin 2)

The tone signal out pin is CMOS comperementaly output and drives external bipolar transistor. This pin generates a tone signal when a key is depressed. Tone signal frequency is 1KHz when 10pps pulse rate is selected. (the frequency is 2KHz when 20pps pulse rate is selected). Only the pin 2 of KS5805A is V_{REF} (on-chip reference voltage).

TYPICAL I-V CHARACTERISTICS

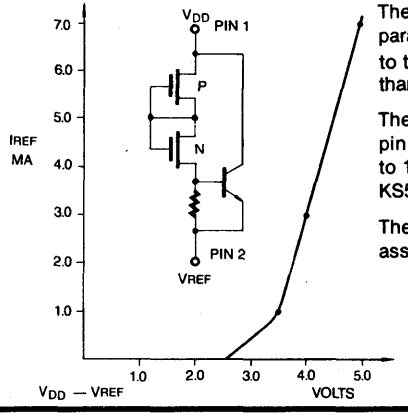


Fig. 3

The V_{REF} output provides a reference voltage that tracks internal parameters of the KS5805A. V_{REF} provides a negative voltage reference to the V_{DD} supply. Its magnitude will be approximately 0.6 volts higher than the minimum operating voltage of a particular KS5805A.

The typical application would be to connect the V_{REF} pin to the GND pin (Pin 6). The supply to the V_{DD} pin (Pin 1) should then be regulated to 150μA (I_{OP} max). With this amount of supply current, operation of the KS5805A is guaranteed.

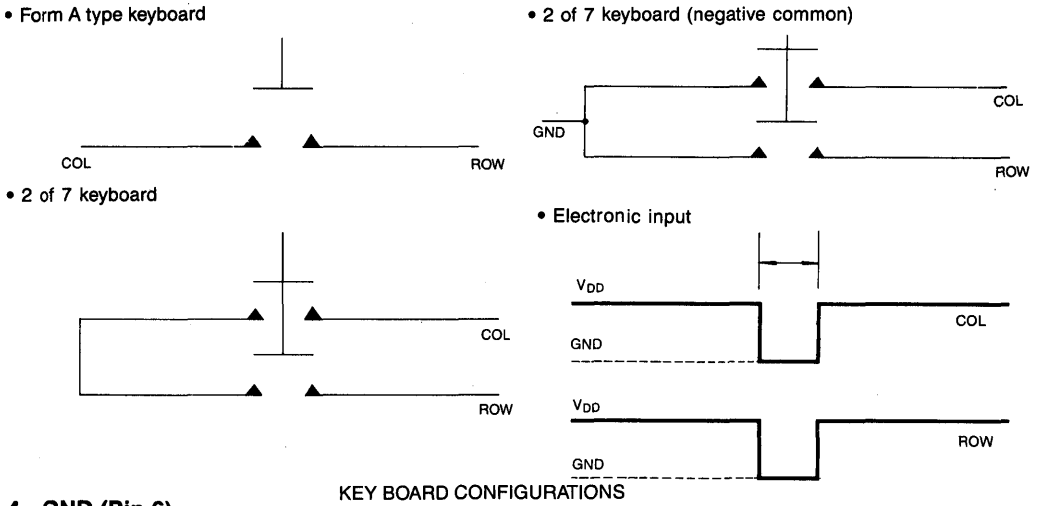
The internal circuit of the V_{REF} function is shown in Figure 3 with its associated I-V characteristic.

3. Keyboard inputs (Pin 3, 4, 5, 13, 14, 15, 16,)

The KS5805A/B incorporates an innovative keyboard scheme that allows either the standard 2-of-7 keyboard with negative common or the inexpensive single contact (form A) keyboard to be used.

A valid key entry is defined by either a single row being connected to a single column or GND being simultaneously presented to both a single row and column. When in the on-hook mode, the row and column inputs are held high and no keyboard inputs are accepted.

When off-hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled and the rows and columns are scanned alternately (pulled high, then low) to verify the varied input. The input must remain valid for 10msec of debounce time to be accepted.



KEY BOARD CONFIGURATIONS

4. GND (Pin 6)

This is the negative supply pin and is connected to the common part in general applications.

5. OSCILLATOR (Pins 7, 8, 9)

The KS5805A/B contains on-chip inverters to provide oscillator which will operate with a minimum external components.

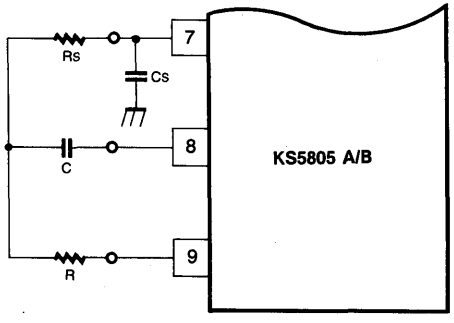
Following figure shows the on-chip configuration with the necessary external components. Optimum stability occurs with the ratio $K=R_S/R$ equal to 10.

The oscillator period is given by:

$$T = RC\ (1.386 + (3.5KC_S)/C\text{-}(2K/(K+1))\ \text{in}\ (K/(1.5K+0.5))$$

Where C_S is the stray capacitance on Pin 7.

Accuracy and stability will be enhanced with this capacitance minimized.



6. 20/10 pps (Pin 10)

Connecting this pin to GND (pin 6) will select an output pulse rate of 10pps.
Connecting the pin V_{DD} (pin 1) will select an output pulse rate of 20pps.

7. MAKE/BREAK (Pin 11)

The MAKE/BREAK pin controls the MAKE/BREAK ratio of the pulse output. The MAKE/BREAK ratio is controlled by connection V_{DD} or GND to this pin as shown in the following table.

Input	Make	Break
V_{DD} (Pin 1)	34%	66%
GND (Pin 6)	40%	60%

8. $\overline{\text{MUTE}}$ OUTPUT (Pin 12)

The $\overline{\text{mute}}$ output is an open-drain N-channel transistor designed to drive external bipolar transistor.
This circuitry is usually used to $\overline{\text{mute}}$ the receiver during outpulsing. As shown in Fig. 2 the KS5805 $\overline{\text{mute}}$ output turns on (pulls to the V_{GND}-supply) at the beginning of the predigital pause and turns off (goes to an open circuit) following the last break.
The delay from the end of the last break until the $\overline{\text{mute}}$ output turns off is $\overline{\text{mute}}$ overlap and is specified as t_{MO}.

9. ON-HOOK/TEST (Pin 17)

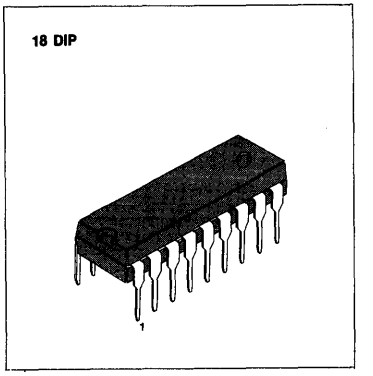
The "ON-HOOK" or "Test" input of the KS5805A/B has a 100KΩ pull-up to the positive supply. A V_{CC} input or allowing the pin to float sets the circuit in its on-hook or test mode while a V_{GND} input sets it in the off-hook or normal mode. When off-hook the KS5805A/B will accept key inputs and outputs the digits in normal fashion. Upon completion of the last digit, the oscillator is disabled and the circuit stands by for additional inputs.
Switching the KS5805A/B to on-hook while it is outpulsing causes the remaining digits to be outpulsed at 100x the normal rate (M/B ratio is then 50/50).
This feature provides a means of rapidly testing the device and is also on efficient method by which the circuitry is reset. When the outpulsing in this mode, which can be up to 300msec, is completed, the circuit is deactivated and will require current only necessary to sustain the memory and power-up-clear detect circuity (refer to the electrical specifications).
Upon retuning off-hook, a negative transistion on the mute output will insure the speech network is connected to the line. If the first key entry is eithr a * or #, the number sequence stored on-chip will be outpulsed. Any other valid key entries will clear the memory and outpulse the new number sequence.

10. $\overline{\text{PULSE}}$ OUTPUT (Pin 18)

The $\overline{\text{pulse}}$ output is an open drain N-channel transistor designed to drive external bipolar transistor. These transistor would normally be used to $\overline{\text{pulse}}$ the telephone line by disconnecting and connecting the network. The KS58A/B05 pulse output is an open circuit during make and pulls to the GND supply during break.

PULSE DIALER WITH REDIAL

The KS58C/D05 is a monolithic CMOS integrated circuit which uses an inexpensive RC oscillator for its frequency reference and provides all the features required for implementing a pulse dialer with 32 digit redial.



FUNCTIONS

- Mute output logic "0"
- Pulse output logic "0"
- RC oscillation for reference frequency
- Designed to operate directly from the telephone line
- Used CMOS technology for low voltage, low power operation

FEATURES

- **Wide operating voltage range (2.0 ~ 6.0V)**
- **Low power dissipation**
- **Use either a standard 2 of 7 matrix keyboard with negative true common or the inexpensive form A-type keyboard**
- **Make/Break ratio can be selected**
- **Redial with * or #**
- **Continuous $\overline{\text{MUTE}}$**
- **Power up clear circuitry on chip**
- **KS58C05 pin 2: V_{ref}, KS58D05 pin 2: Tone output**
- **10 pps/20 pps can be selected**

ORDERING INFORMATION

Device	Package	Function	Operating Temperature
KS58C05N	18 DIP	Pin 2 = V_{ref}	−20 ~ +70°C
KS58D05N	18 DIP	Pin 2 = Tone Out	

TEST CIRCUIT

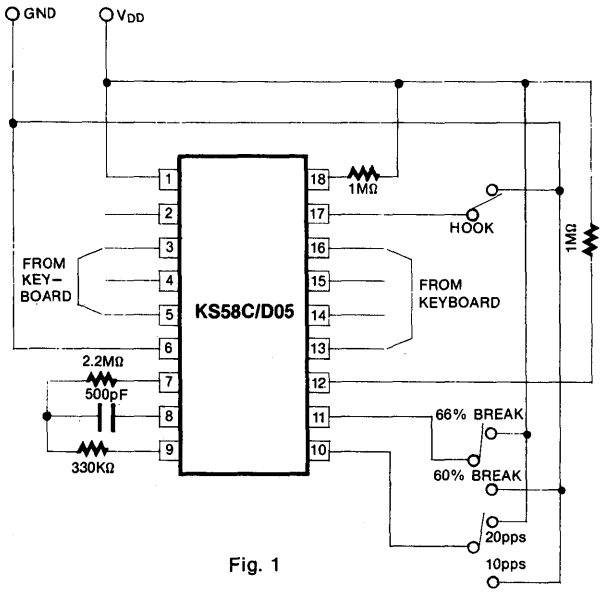


Fig. 1

PIN CONNECTIONS

Pin 1: V_{DD}
Pin 2: V_{ref} (KS58C05)/Pacifier tone (KS58D05)
Pin 3: $\overline{\text{Column 1}}$
Pin 4: $\overline{\text{Column 2}}$
Pin 5: $\overline{\text{Column 3}}$
Pin 6: GND
Pin 7: RC Oscillator
Pin 8: RC Oscillator
Pin 9: RC Oscillator
Pin 10: 10/20pps Select
Pin 11: Make/Break Select
Pin 12: $\overline{\text{Mute}}$ Output
Pin 13: $\overline{\text{ROW 4}}$
Pin 14: $\overline{\text{ROW 3}}$
Pin 15: $\overline{\text{ROW 2}}$
Pin 16: $\overline{\text{ROW 1}}$
Pin 17: On-Hook/Test
Pin 18: $\overline{\text{Pulse}}$ Output

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	6.2	V
Input Voltage	V_{IN}	Gnd – 0.3, V_{DD} + 0.3	V
Output Voltage	V_{OUT}	Gnd – 0.3, V_{DD} + 0.3	V
Power Dissipation	P_D	500	mW
Operating Temperature	T_a	– 20 ~ + 70	°C
Storage Temperature	T_{stg}	– 40 ~ + 125	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.5V, f_{OSC} = 2.4KHz, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.0		6.0	V
Memory Retention Voltage	V_{DR}		1.0			V
Input High Voltage	V_{IH}	$\overline{R_1} \sim \overline{R_4}$, $\overline{C_1} \sim \overline{C_4}$, $\overline{HS}$, DRS, M/B	0.8V_{DD}		V_{DD}	V
Input Low Voltage	V_{IL}		Gnd		0.2V_{DD}	V
Operating Current	I_{DD}	All output under no load		100	150	μA
Output Leakage Current	I_{OL}	V_{CC} = 6.0V, $\overline{MUTE}$, $\overline{PULSE}$ = 6.0V		0.001	1	μA
Output Current ($\overline{MUTE}$, $\overline{PULSE}$)	I_{O1}	V_O = 0.4V, V_{DD} = 2.5V	0.5	1.5		mA
	I_{O2}	V_O = 0.4V, V_{DD} = 3.5V	1.7	5.0		mA
Oscillator Frequency	f_{OSC}			2.4		KHz
Valid Key Entry Time	T_{KD}		14		20	mS
On Hook Time Required to Clear Memory	T_{OH}		300			mS
Inter Digital Pause	T_{IDP}			800		mS
Frequency Stability	△f	V_{DD} = 2.0 ~ 6.0V		± 10		%
Tone Output Frequency	f_{TONE}			1.2		KHz

FUNCTION DESCRIPTION

1. "ON-HOOK" MODE

When "ON-HOOK," key inputs will not be recognized because the oscillator is disabled, which prevents the circuit from drawing excessive current.

2. "DIAL" MODE

When "OFF-HOOK," the device senses the key down condition by detecting one key input and enters the key's code into at on-chip memory.

The memory can store up to 32 digits, and it allows key strobes to be entered at rates comparable to a tone dialing telephone. Output pulsing will continue until all entered digits have been dialed. To implement the pulse dialer function, two outputs are provided, one to pulse the telephone line and one to mute the receiver.

3. "REDIAL" MODE

The first 32 digits entered will be stored in the on-chip redial memory and can be redialed by pressing either * or #, provided that the receiver is "ON-HOOK" for minimum T_{OH} (on hook time required to clear memory).

4. POWER UP CLEAR

The on-chip "POWER UP CLEAR" circuit reliable operation of the device. If the supply to the circuit is not sufficient to retain data in the memory, a "POWER UP CLEAR" will help regaining a proper supply level. This function will prevent the "Redial" or spontaneous outputing of incorrect data.

TIMING CHARACTERISTICS

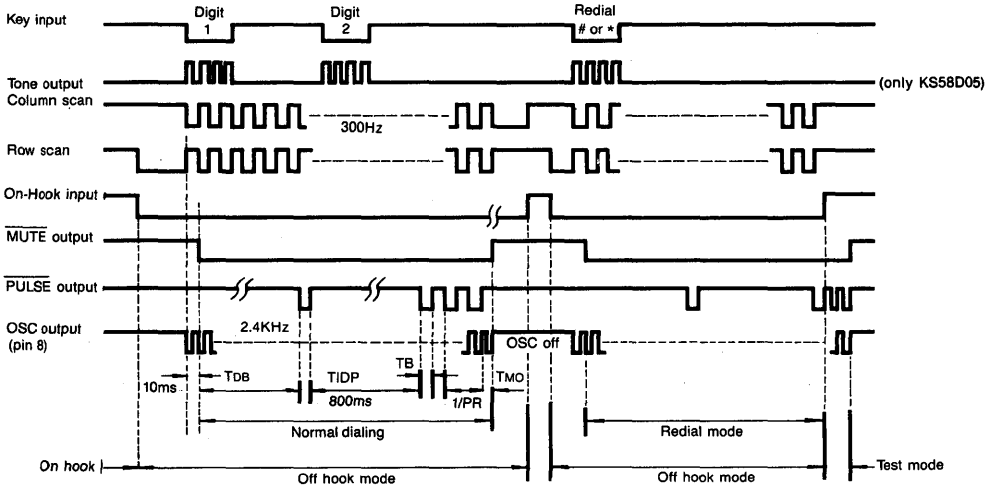


Fig. 2

PIN DESCRIPTIONS

1. V_{DD} (Pin 1)

This is the positive supply pin. The voltage on this pin is measured relative to Pin 6 and is supplied from a 150 μA current source. This voltage should be regulated to less than 6.0 volts using on external form or regulation.

2. Tone signal output/V_{REF} (Pin 2)

The tone signal out pin is CMOS comperementaly output and drives external bipolar transistor. This pin generates a tone signal when a key is depressed. The tone signal frequency is 1.2 KHz when 10 pps pulse rate is selected.

TYPICAL I-V CHARACTERISTICS

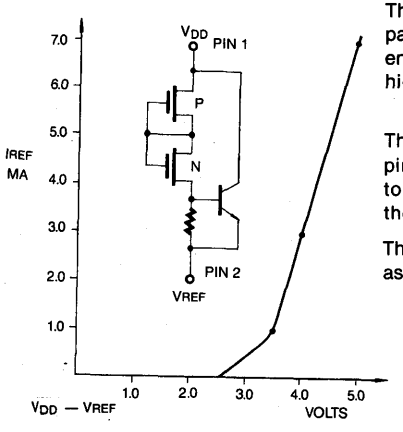


Fig. 3

The V_{REF} output provides a reference voltage that tracks internal parameters of the KS58C05. The V_{REF} provides a negative voltage reference to the V_{DD} supply. Its magnitude will be approximately 0.6 volts higher than the minimum operating voltage of a particular KS58C05.

The typical application would be to connect the V_{REF} pin to the GND pin (Pin 6). The supply to the V_{DD} pin (Pin 1) should then be regulated to 150μA (I_{OP} max). With this amount of supply current, operation of the KS58C05 is guaranteed.

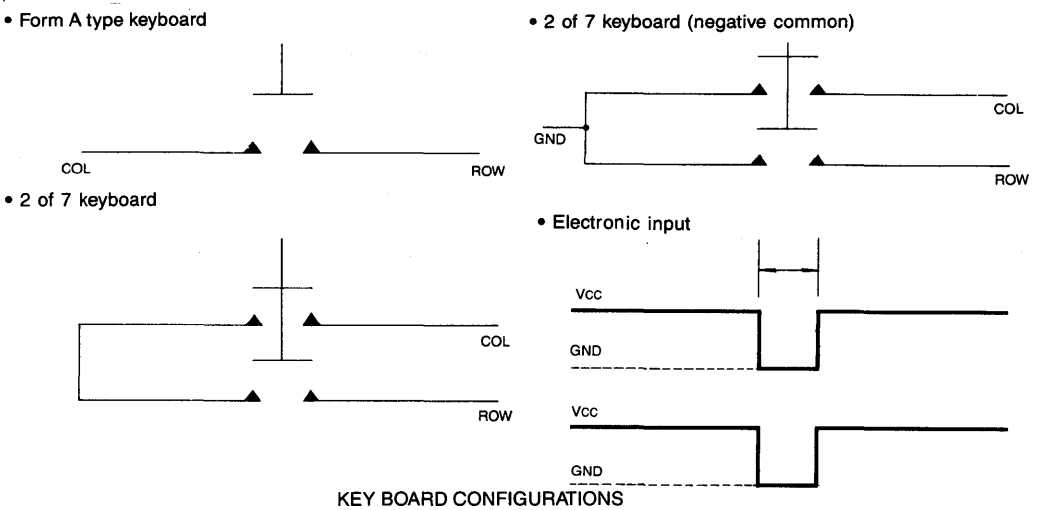
The internal circuit of the V_{REF} function is shown in Figure 3 with its associated I-V characteristic.

3. Keyboard inputs (Pin 3, 4, 5, 13, 14, 15, 16)

The KS58C/D05 incorporates an innovative keyboard scheme that allows either the standard 2-of-7 keyboard with negative common or the inexpensive single contact (form A) keyboard to be used.

A valid key entry is defined by either a single row being connected to a single column or GND being simutanecusly presented to both a single row and column. When in the on-hook mode, the row and column inputs are held high are no keyboard inputs are accepted.

When off-hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled and the rows and columns are scanned alternately (pulled high, then low) to verify the varied input. The input must remain valid for 14-20 msec of debounce time to be accepted.



KEY BOARD CONFIGURATIONS

4. GND (Pin 6)

This is the negative supply pin and is connected to the common part in general applications.

5. OSCILLATOR (Pin 7, 8, 9)

The KS58C/D05 contains on-chip inverters to provide oscillator which will operate with a minimum external components.

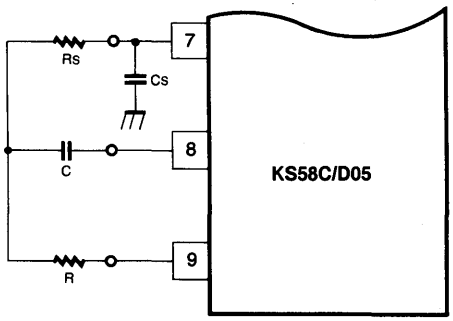
Following figure shows the on-chip configuration with the necessary external components. Optimum stability occurs with the ratio $K = R_S/R$ equal to 6.67.

The oscillator period is given by:

$$T = RC\ \{1.386 + (3.5K_{CS})/C\text{-}(2K/CK + 1)\ \text{In}\ CK/(1.5K + 0.5)\}$$

Where C_S is the stray capacitance on Pin 7.

Accuracy and stability will be enhanced with this capacitance minimized.



6. 20/10 pps (Pin 10)

Connecting this pin to GND (pin 6) will select an output pulse rate of 10pps.
Connecting the pin V_{DD} (pin 1) will select an output pulse rate of 20pps.

7. MAKE/BREAK (Pin 11)

The MAKE/BREAK pin controls the MAKE/BREAK ratio of the pulse output. The MAKE/BREAK ratio is controlled by connection V_{DD} or GND to this pin as shown in the following table.

Input	Make	Break
V_{DD} (Pin 1)	33.4%	66.6%
GND (Pin 6)	40%	60%

8. $\overline{\text{MUTE}}$ OUTPUT (Pin 12)

The mute output is an open-drain N-channel transistor designed to drive external bipolar transistor.
This circuitry is usually used to mute the receiver during outpulsing. As shown in Fig. 2 the KS58C/D05 $\overline{\text{mute}}$ output turns on (pulls to the V_{GND}-supply) at the beginning of the predigital pause and turns off (goes to an open circuit) following the last break.
The delay from the end of the last break until the $\overline{\text{mute}}$ output turns off is $\overline{\text{mute}}$ overlap and is specified as t_{MO}.

9. ON-HOOK/TEST (Pin 17)

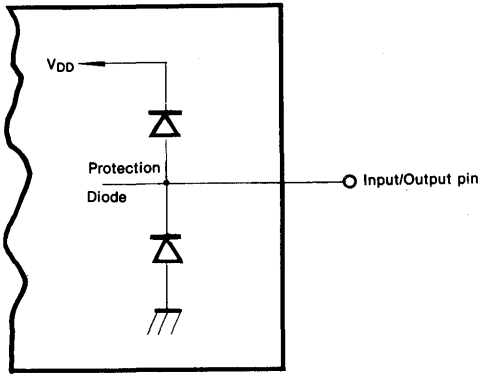
This pin detects the state of the hook switch contact "OFF HOOK" corresponds to V_{SS} condition. "ON HOOK" corresponds to V_{DD} condition. When outpulsing in this mode, which can be up to 300msec, is completed, the circuit is deactivated and will require current only necessary to sustain the memory and power-up-clear detect circuitry (refer to the electrical specifications).
Upon retuning off-hook, a negative transistion on the mute output will insure the speech network is connected to the line. If the first key entry is either a * or #, the number sequence stored on-chip will be outpulsed. Any other valid key entries will clear the memory and outpulse the new number sequence.

10. $\overline{\text{PULSE}}$ OUTPUT (Pin 18)

The $\overline{\text{pulse}}$ output is an open drain N-channel transistor designed to drive external bipolar transistor. These transistor would normally be used to pulse the telephone line by disconnecting and connecting the network. The KS58C/D05 $\overline{\text{pulse}}$ output is an open circuit during make and pulls to the GND supply during break.

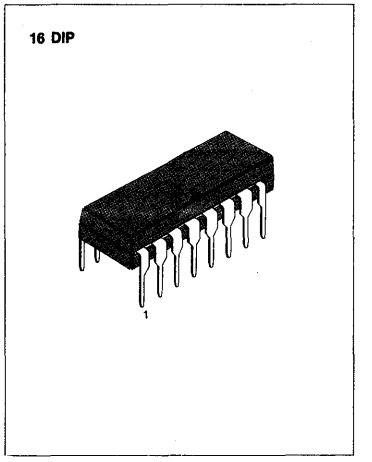
11. ESD PROTECTION

All Input/Output pins are protected ESD.



PULSE DIALER WITH REDIAL

The KS58E05 is a monolithic CMOS integrated circuit which uses an inexpensive RC oscillator for its frequency reference and provides all the features required for implementing a pulse dialer with 32 digit redial.



FUNCTIONS

- $\overline{\text{Mute}}$ output logic "0"
- $\overline{\text{Pulse}}$ output logic "0"
- RC oscillation for reference frequency
- Designed to operate directly from the telephone line
- Used CMOS technology for low voltage, low power operation

FEATURES

- **Wide operating voltage range (2.0 ~ 6.0V)**
- **Low power dissipation**
- **Use either a standard 2 of 7 matrix keyboard with negative true common or the inexpensive form A-type keyboard**
- **Make/Break ratio can be selected**
- **Redial with * or #**
- **Continuous MUTE**
- **Power up clear circuitry on chip**
- **10 pps only.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KS58E05N	16 DIP	−20 ~ +70°C

TEST CIRCUIT

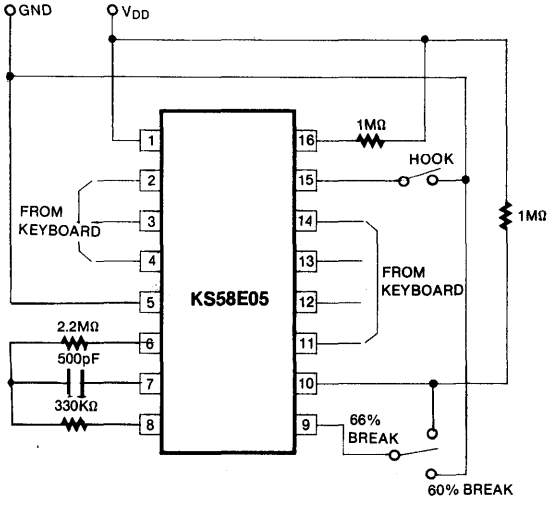


Fig. 1

PIN CONNECTIONS

Pin 1: V_{DD}
Pin 2: $\overline{\text{Column 1}}$
Pin 3: $\overline{\text{Column 2}}$
Pin 4: $\overline{\text{Column 3}}$
Pin 5: GND
Pin 6: RC Oscillator
Pin 7: RC Oscillator
Pin 8: RC Oscillator
Pin 9: Make/Break Select
Pin 10: $\overline{\text{Mute}}$ Output
Pin 11: $\overline{\text{ROW 4}}$
Pin 12: $\overline{\text{ROW 3}}$
Pin 13: $\overline{\text{ROW 2}}$
Pin 14: $\overline{\text{ROW 1}}$
Pin 15: On-Hook/Test
Pin 16: $\overline{\text{Pulse}}$ Output

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	6.2	V
Input Voltage	V_{IN}	GND − 0.3, V_{DD} + 0.3	V
Output Voltage	V_{OUT}	GND − 0.3, V_{DD} + 0.3	V
Power Dissipation	P_D	500	mW
Operating Temperature	T_a	− 20 ~ + 70	°C
Storage Temperature	T_{stg}	− 40 ~ + 125	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.5V, f_{OSC} = 2.4KHz, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.0		6.0	V
Memory Retention Voltage	V_{DR}		1.0			V
Input High Voltage	V_{IH}	$\overline{R_1} \sim \overline{R_4}$, $\overline{C_1} \sim \overline{C_4}$, $\overline{HS}$, M/B	0.8V_{DD}		V_{DD}	V
Input Low Voltage	V_{IL}		GND		0.2V_{DD}	V
Operating Current	I_{OD}	All output under no load		100	150	μA
Output Leakage Current	I_{OL}	V_{CC} = 6.0V, $\overline{MUTE}$, $\overline{PULSE}$ = 6.0V		0.001	1	μA
Output Current ($\overline{MUTE}$, $\overline{PULSE}$)	I_{OL1}	V_O = 0.4V, V_{DD} = 2.5V	0.5	1.5		mA
	I_{OL2}	V_O = 0.4V, V_{DD} = 3.5V	1.7	5.0		mA
Oscillator Frequency	f_{OSC}			2.4		KHz
Valid Key Entry Time	T_{KD}		14		20	mS
On Hook Time Required to Clear Memory	T_{OH}		300			mS
Inter Digital Pause	T_{IDP}			800		mS
Frequency Stability	△f	V_{DD} = 2.0 ~ 6.0V		± 10		%

FUNCTION DESCRIPTION

1. "ON-HOOK" MODE

When "ON-HOOK," key inputs will not be recognized because the oscillator is disabled which prevents the circuit from drawing excessive current.

2. "DIAL" MODE

When "OFF-HOOK," the device senses key down condition by detecting one key input and enters the key's code into an on-chip memory.

The memory can be store up to 32 digits, and it allows key strobes to be entered at rates comparable to a tone dialing telephone. Output pulsing will continue until all entered digits have been dialed. To implement the pulse dialer function, two outputs are provided, one to pulse the telephone line and one to mute the receiver.

3. "REDIAL" MODE

The first 32 digits entered will be stored in the on-chip redial memory and can be redialed by pressing either * or #, provided that the receiver is "ON-HOOK" for minimum ton (on hook time required to clear memory).

4. POWER UP CLEAR

The on-chip "POWER UP CLEAR" circuit reliable operation of the device. If the supply to the circuit is not sufficient to retain data in the memory, a "POWER UP CLEAR" will help regaining a proper supply level.

This function will prevent the "Redial" or sportaneous outputing of incorrect data.

TIMING CHARACTERISTICS

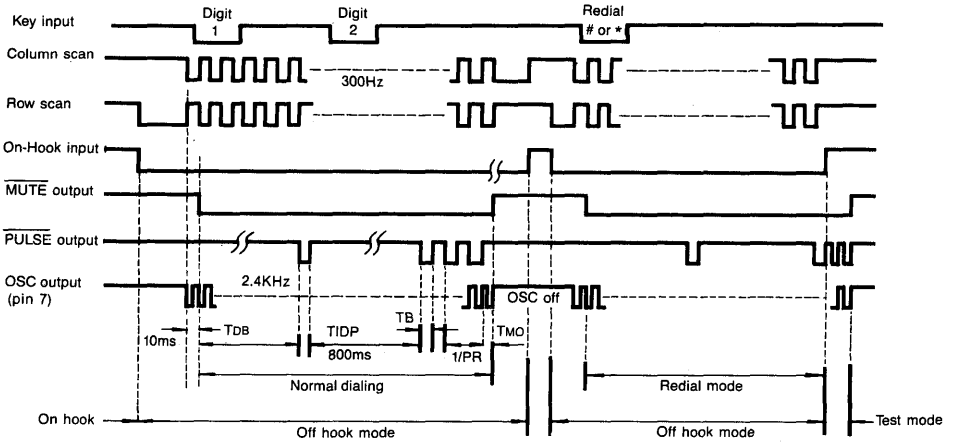


Fig. 2

1. V_{DD} (Pin 1)

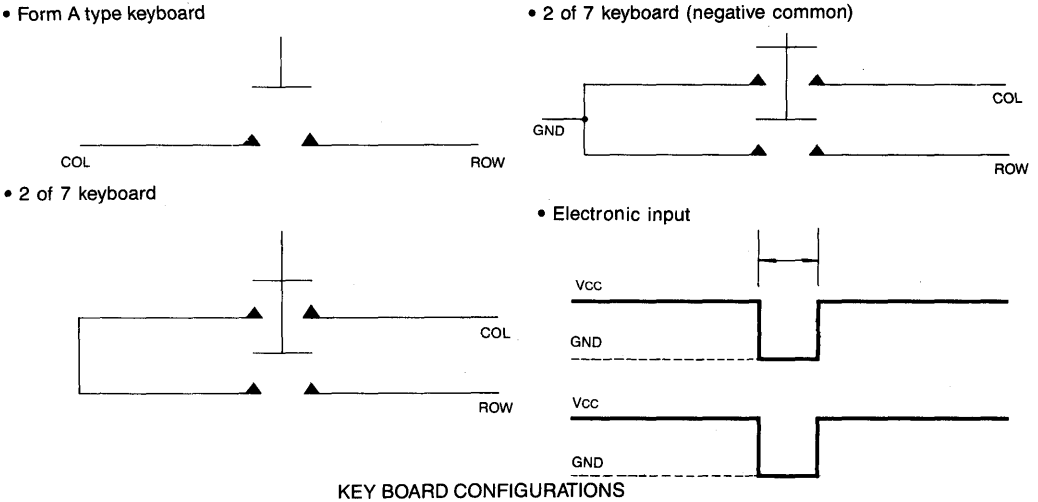
This is the positive supply pin. The voltage on this pin is measured relative to Pin 6 and is supplied from a 150 μA current source. This voltage should be regulated to less than 6.0 volts using on external form or regulation.

2. Keyboard inputs (Pin 2, 3, 4, 11, 12, 13, 14)

The KS58E05 incorporates an innovative keyboard scheme that allows either the standard 2-of-7 keyboard with negative common or the inexpensive single contact (form A) keyboard to be used.

A valid key entry is defined by either a single row being connected to a single column or GND being simultaneously presented to both a single row and column. When in the on-hook mode, the row and column inputs are held high and no keyboard inputs are accepted.

When off-hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled and the rows and columns are alternately scanned (pulled high, then low) to verify the input is varied. The input must remain valid continuously for 14-20 msec of debounce time to be accepted.



KEY BOARD CONFIGURATIONS

3. GND (Pin 5)

This is the negative supply pin and is connected to the common part in general applications.

4. OSCILLATOR (Pin 6, 7, 8)

The KS58E05 contains on-chip inverters to provide oscillator which will operate with a minimum external components.

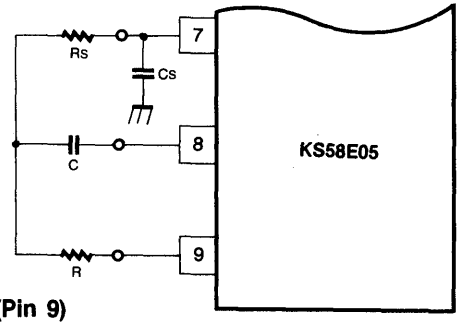
Following figure shows the on-chip configuration with the necessary external components. Optimum stability occurs with the ratio $K = R_S/R$ equal to 6.67.

The oscillator period is given by:

$T = RC \{1.386 + (3.5K_{CS})/C\text{-}(2K/CK + 1) \ln CK/(1.5K + 0.5)\}$

Where C_S is the stray capacitance on Pin 6.

Accuracy and stability will be enhanced with this capacitance minimized.



5. MAKE/BREAK (Pin 9)

The MAKE/BREAK pin controls the MAKE/BREAK ratio of the pulse output. The MAKE/BREAK ratio is controlled by connection V_{DD} or GND to this pin as shown in the following table.

Input	Make	Break
V_{DD} (Pin 1)	33.4%	66.6%
GND (Pin 5)	40%	60%

6. $\overline{\text{MUTE}}$ OUTPUT (Pin 10)

The mute output is an open-drain N-channel transistor designed to drive external bipolar transistor.

This circuitry is usually used to mute the receiver during outpulsing. As shown in Fig. 2 the KS58E05 mute output turns on (pulls to the V_{GND}-supply) at the beginning of the predigital pause and turns off (goes to an open circuit) following the last break.

The delay from the end of the last break until the mute output turns off is mute overlap and is specified as t_{MO}.

7. ON-HOOK/TEST (Pin 15)

This pin detects the state of the hook switch contact "OFF HOOK" corresponds to V_{SS} condition. "ON HOOK" corresponds to V_{DD} condition. When outpulsing in this mode, which can be up to 300msec, is completed, the circuit is deactivated and will require current only necessary to sustain the memory and power-up-clear detect circuitry (refer to the electrical specifications).

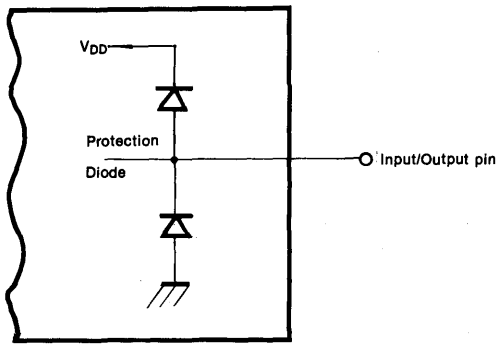
Upon retuning off-hook, a negative transistion on the mute output will insure the speech network is connected to the line. If the first key entry is either a * or #, the number sequence stored on-chip will be outpulsed. Any other valid key entries will clear the memory and outpulse the new number sequence.

8. $\overline{\text{PULSE}}$ OUTPUT (Pin 16)

The pulse output is an open drain N-channel transistor designed to drive external bipolar transistor. These transistor would normally be used to pulse the telephone line by disconnecting and connecting the network. The KS58E05 pulse output is an open circuit during make and pulls to the GND supply during break.

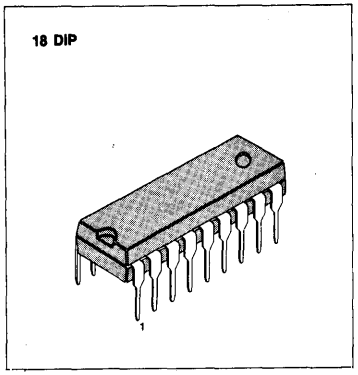
9. ESD PROTECTION

All Input/Output pins are protected ESD



PULSE DIALER WITH REDIAL

The KS5851/52 is a monolithic CMOS integrated circuit which uses an inexpensive RC oscillator for its frequency reference and provides all the features required for implementing a pulse dialer with 32 digit redial.



FUNCTIONS

- Mute output logic "0"
- Pulse output logic "0"
- RC oscillation for reference frequency
- Designed to operate directly from the telephone line
- Used CMOS technology for low voltage, low power operation

FEATURES

- **Wide operating voltage range (2.0 ~ 6.0V)**
- **Low power dissipation**
- **Use either a standard 2 of 7 matrix keyboard with negative true common or the inexpensive form A-type keyboard**
- **Make/Break ratio can be selected**
- **Redial with * or #**
- **Continuous $\overline{\text{MUTE}}$**
- **Power up clear circuitry on chip**
- **KS5851 pin 2: V_{ref}, KS5852 pin 2: Tone output**
- **10 pps/20 pps can be selected**

ORDERING INFORMATION

Device	Package	Function	Operating Temperature
KS5851N	18 DIP	Pin 2 = V_{ref}	− 20 ~ + 70°C
KS5852N	18 DIP	Pin 2 = Tone Out	

TEST CIRCUIT

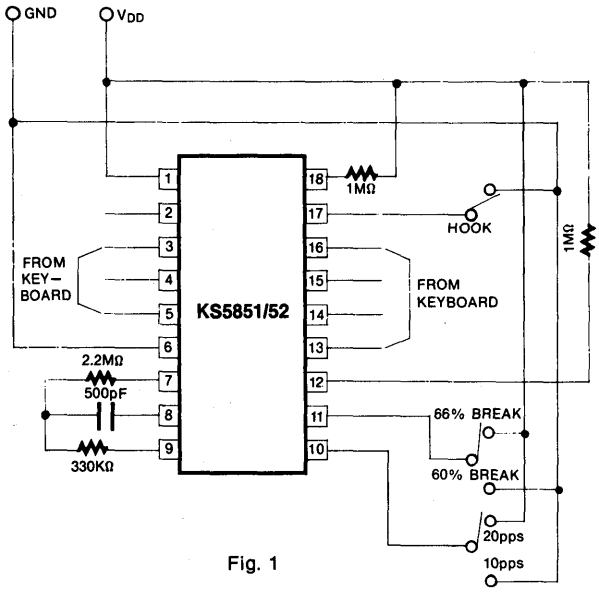


Fig. 1

PIN CONNECTIONS

Pin 1: V_{DD}
Pin 2: V_{ref} (KS5851)/Pacifier tone (KS5852)
Pin 3: $\overline{\text{Column 1}}$
Pin 4: $\overline{\text{Column 2}}$
Pin 5: $\overline{\text{Column 3}}$
Pin 6: GND
Pin 7: RC Oscillator
Pin 8: RC Oscillator
Pin 9: RC Oscillator
Pin 10: 10/20pps Select
Pin 11: Make/Break Select
Pin 12: $\overline{\text{Mute}}$ Output
Pin 13: $\overline{\text{ROW 4}}$
Pin 14: $\overline{\text{ROW 3}}$
Pin 15: $\overline{\text{ROW 2}}$
Pin 16: $\overline{\text{ROW 1}}$
Pin 17: On-Hook/Test
Pin 18: $\overline{\text{Pulse}}$ Output

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	6.2	V
Input Voltage	V_{IN}	Gnd – 0.3, V_{DD} + 0.3	V
Output Voltage	V_{OUT}	Gnd – 0.3, V_{DD} + 0.3	V
Power Dissipation	P_D	500	mW
Operating Temperature	T_a	– 20 ~ + 70	°C
Storage Temperature	T_{stg}	– 40 ~ + 125	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.5V, f_{OSC} = 2.4KHz, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.0		6.0	V
Memory Retention Voltage	V_{DR}		1.0			V
Input High Voltage	V_{IH}	$\overline{R_1} \sim \overline{R_4}$, $\overline{C_1} \sim \overline{C_4}$, $\overline{HS}$, DRS, M/B	0.8V_{DD}		V_{DD}	V
Input Low Voltage	V_{IL}		Gnd		0.2V_{DD}	V
Operating Current	I_{OD}	All output under no load		100	150	μA
Output Leakage Current	I_{OL}	V_{CC} = 6.0V, $\overline{MUTE}$, $\overline{PULSE}$ = 6.0V		0.001	1	μA
Output Current ($\overline{MUTE}$, $\overline{PULSE}$)	I_{OL1}	V_O = 0.4V, V_{DD} = 2.5V	0.5	1.5		mA
	I_{OL2}	V_O = 0.4V, V_{DD} = 3.5V	1.7	5.0		mA
Oscillator Frequency	f_{OSC}			2.4		KHz
Valid Key Entry Time	T_{KD}		14		20	mS
On Hook Time Required to Clear Memory	T_{OH}		300			mS
Inter Digital Pause	T_{IDP}			800		mS
Frequency Stability	$\triangle f$	V_{DD} = 2.0 ~ 6.0V		± 10		%
Tone Output Frequency	f_{TONE}			1.2		KHz

FUNCTION DESCRIPTION

1. "ON-HOOK" MODE

When "ON-HOOK," key inputs will not be recognized because the oscillator is disabled which prevents the circuit from drawing excessive current.

2. "DIAL" MODE

When "OFF-HOOK," the device senses key down condition by detecting one key input and enters the key's code into an on-chip memory.

The memory can be store up to 32 digits, and it allows key strobes to be entered at rates comparable to tone dialing telephone. Output pulsing will continue until all entered digits have been dialed. To implement the pulse dialer function, two outputs, one to pulse the telephone line and one to mute the receiver, are provided.

3. "REDIAL" MODE

The first 32 digits entered will be stored in the on-chip redial memory and can be redialed by pressing either * or #, provided that the receiver is "ON-HOOK" for minimum T_{OH} (on hook time required to clear memory).

4. POWER UP CLEAR

The on-chip "POWER UP CLEAR" circuit reliable operation of the device. If the supply to the circuit is not sufficient to retain data in the memory, a "POWER UP CLEAR" will help regaining a proper supply level.

This function will prevent the "Redial" or spontaneous outputing of incorrect data.

TIMING CHARACTERISTICS

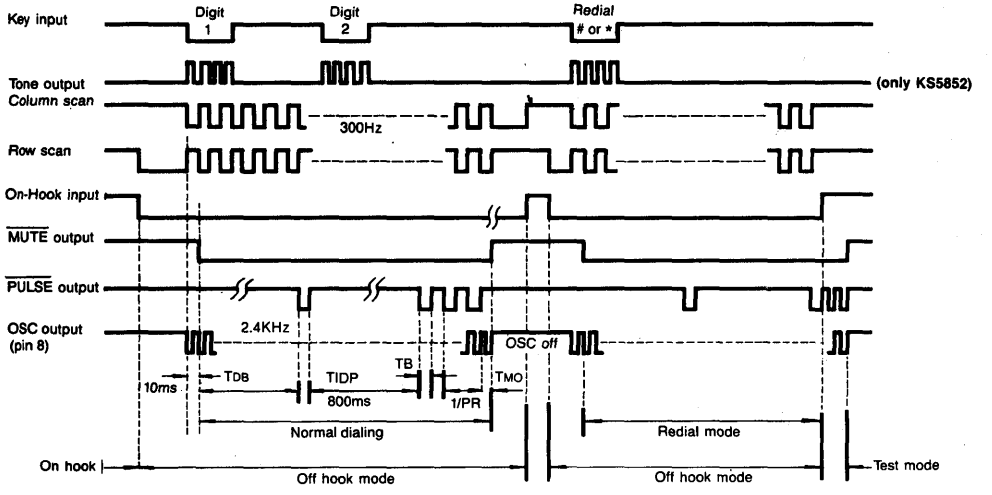


Fig. 2

PIN DESCRIPTIONS

1. V_{DD} (Pin 1)

This is positive supply pin. The voltage on this pin is measured relative to Pin 6 and is supplied from a 150μA current source. This voltage should be regulated to less than 6.0 volts using on external form or regulation.

2. Tone signal output/V_{REF} (Pin 2)

Tone signal out pin is CMOS complementally output and drives external bipolar transistor. This pin generates a tone signal when a key is depressed. Tone signal frequency is 1.2KHz when 10pps pulse rate is selected.

TYPICAL I-V CHARACTERISTICS

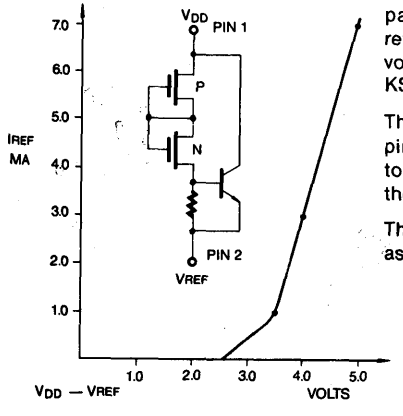


Fig. 3

The V_{REF} output provides a reference voltage that tracks internal parameters of the KS5851. V_{REF} provides a negative voltage reference to the V_{DD} supply. Its magnitude will be approximately 0.6 volt higher than the minimum operating voltage of each particular KS5851.

The typical application would be to connect the V_{REF} pin to the GND pin (Pin 6). The supply to the V_{DD} pin (Pin 1) should then be regulated to 150μA (I_{OP} max). With this amount of supply current, operation of the KS5851 is guaranteed.

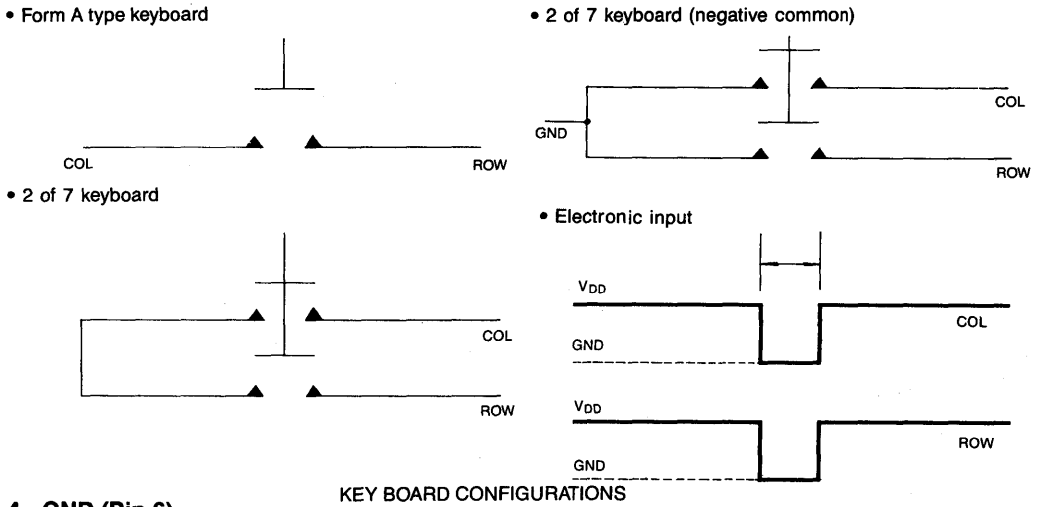
The internal circuit of the V_{REF} function is shown in Figure 3 with its associated I-V characteristic.

3. Keyboard inputs (Pin 3, 4, 5, 13, 14, 15, 16,)

The KS5851/52 incorporates an innovative keyboard scheme that allows either the standard 2-of-7 keyboard with negative common or the inexpensive single contact (form A) keyboard to be used.

A valid key entry is defined by either a single row being connected to a single column or GND being simultaneously presented to both a single row and column. When in the on-hook mode, the row and column inputs are held high and no keyboard inputs are accepted.

When off-hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled and the rows and columns are scanned alternately (pulled high, then low) to verify the varied input. The input must remain valid for 10msec of debounce time to be accepted.



KEY BOARD CONFIGURATIONS

4. GND (Pin 6)

This is the negative supply pin and is connected to the common part in general applications.

5. OSCILLATOR (Pins 7, 8, 9)

The KS5851/52 contains on-chip inverters to provide oscillator which will operate with a minimum external components.

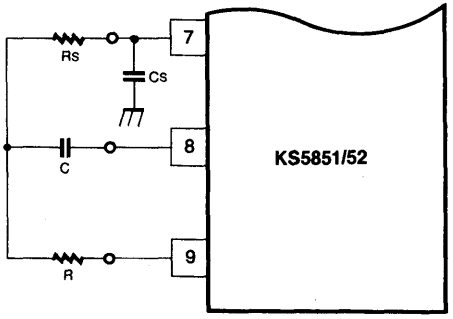
Following figure shows the on-chip configuration with the necessary external components. Optimum stability occurs with the ratio $K=R_S/R$ equal to 10.

The oscillator period is given by:

$$T = RC\ (1.386 + (3.5KC_S)/C\text{-}(2K/(K+1))\ \text{in}\ (K/(1.5K+0.5))$$

Where C_S is the stray capacitance on Pin 7.

Accuracy and stability will be enhanced with this capacitance minimized.



6. 20/10 pps (Pin 10)

Connecting this pin to GND (pin 6) will select an output pulse rate of 10pps.
Connecting the pin V_{DD} (pin 1) will select an output pulse rate of 20pps.

7. MAKE/BREAK (Pin 11)

The MAKE/BREAK pin controls the MAKE/BREAK ratio of the pulse output. The MAKE/BREAK ratio is controlled by connection V_{DD} or GND to this pin as shown in the following table.

Input	Make	Break
V_{DD} (Pin 1)	33.4%	66.6%
GND (Pin 6)	40%	60%

8. $\overline{\text{MUTE}}$ OUTPUT (Pin 12)

The mute output is an open-drain N-channel transistor designed to drive external bipolar transistor.
This circuitry is usually used to mute the receiver during outpulsing. As shown in Fig. 2 the KS5851/52 $\overline{\text{mute}}$ output turns on (pulls to the V_{GND}-supply) at the beginning of the predigital pause and turns off (goes to an open circuit) following the last break.
The delay from the end of the last break until the $\overline{\text{mute}}$ output turns off is $\overline{\text{mute}}$ overlap and is specified as t_{MO}.

9. ON-HOOK/TEST (Pin 17)

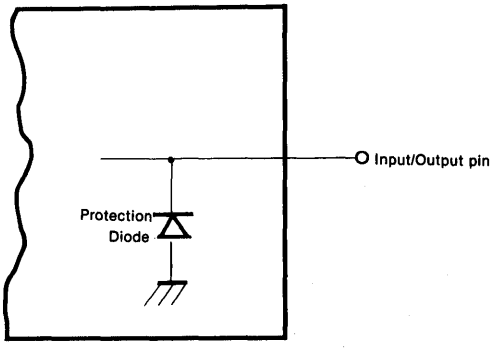
This pin detects the state of the hook switch contact "OFF HOOK" corresponds to V_{SS} condition. "ON HOOK" corresponds to V_{DD} condition. When outpulsing in this mode, which can be up to 300msec, is completed, the circuit is deactivated and will require current only necessary to sustain the memory and power-up-clear detect circuitry (refer to the electrical specifications).
Upon retuning off-hook, a negative transistion on the mute output will insure the speech network is connected to the line. If the first key entry is either a * or #, the number sequence stored on-chip will be outpulsed. Any other valid key entries will clear the memory and outpulse the new number sequence.

10. $\overline{\text{PULSE}}$ OUTPUT (Pin 18)

The $\overline{\text{pulse}}$ output is an open drain N-channel transistor designed to drive external bipolar transistor. These transistor would normally be used to pulse the telephone line by disconnec ting and connecting the network. The KS5851/52 $\overline{\text{pulse}}$ output is an open circuit during make and pulls to the GND supply during break.

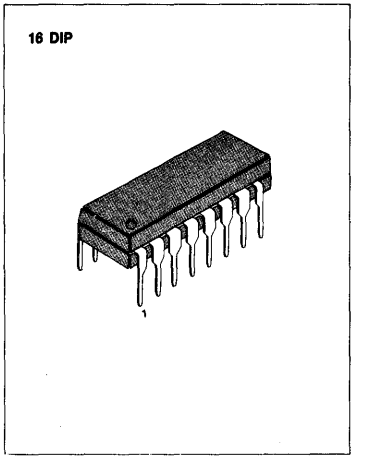
11. ESD PROTECTION

All Input/Output are protected ESD.



PULSE DIALER WITH REDIAL

The KS5853 is a monolithic CMOS integrated circuit which uses an inexpensive RC oscillator for its frequency reference and provides all the features required for implementing a pulse dialer with 32 digit redial.



FUNCTIONS

- $\overline{\text{Mute}}$ output logic "0"
- $\overline{\text{Pulse}}$ output logic "0"
- RC oscillation for reference frequency
- Designed to operate directly from the telephone line
- Used CMOS technology for low voltage, low power operation

FEATURES

- **Wide operating voltage range (2.0 ~ 6.0V)**
- **Low power dissipation**
- **Use either a standard 2 of 7 matrix keyboard with negative true common or the inexpensive form A-type keyboard**
- **Make/Break ratio can be selected**
- **Redial with * or #**
- **Continuous $\overline{\text{MUTE}}$**
- **Power up clear circuitry on chip**
- **10 pps only.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KS5853N	16 DIP	− 20 ~ + 70°C

TEST CIRCUIT

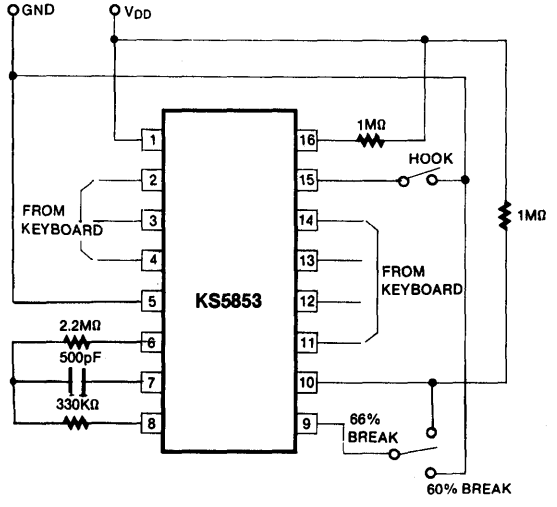


Fig. 1

PIN CONNECTIONS

Pin 1: V_{DD}
Pin 2: $\overline{\text{Column 1}}$
Pin 3: $\overline{\text{Column 2}}$
Pin 4: Column 3
Pin 5: GND
Pin 6: RC Oscillator
Pin 7: RC Oscillator
Pin 8: RC Oscillator
Pin 9: Make/Break Select
Pin 10: $\overline{\text{Mute}}$ Output
Pin 11: $\overline{\text{ROW 4}}$
Pin 12: $\overline{\text{ROW 3}}$
Pin 13: $\overline{\text{ROW 2}}$
Pin 14: $\overline{\text{ROW 1}}$
Pin 15: On-Hook/Test
Pin 16: $\overline{\text{Pulse}}$ Output

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	6.2	V
Input Voltage	V_{IN}	GND − 0.3, V_{DD} + 0.3	V
Output Voltage	V_{OUT}	GND − 0.3, V_{DD} + 0.3	V
Power Dissipation	P_D	500	mW
Operating Temperature	T_a	− 20 ~ + 70	°C
Storage Temperature	T_{stg}	− 40 ~ + 125	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.5V, f_{OSC} = 2.4KHz, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.0		6.0	V
Memory Retention Voltage	V_{DR}		1.0			V
Input High Voltage	V_{IH}	$\overline{R_1} \sim \overline{R_4}$, $\overline{C_1} \sim \overline{C_4}$, $\overline{HS}$, M/B	0.8V_{DD}		V_{DD}	V
Input Low Voltage	V_{IL}		GND		0.2V_{DD}	V
Operating Current	I_{OD}	All output under no load		100	150	μA
Output Leakage Current	I_{OL}	V_{CC} = 6.0V, $\overline{MUTE}$, $\overline{PULSE}$ = 6.0V		0.001	1	μA
Output Current ($\overline{MUTE}$, $\overline{PULSE}$)	I_{OL1}	V_O = 0.4V, V_{DD} = 2.5V	0.5	1.5		mA
	I_{OL2}	V_O = 0.4V, V_{DD} = 3.5V	1.7	5.0		mA
Oscillator Frequency	f_{OSC}			2.4		KHz
Valid Key Entry Time	T_{KD}		14		20	mS
On Hook Time Required to Clear Memory	T_{OH}		300			mS
Inter Digital Pause	T_{IDP}			800		mS
Frequency Stability	△f	V_{DD} = 2.0 ~ 6.0V		± 10		%

FUNCTION DESCRIPTION

1. "ON-HOOK" MODE

When "ON-HOOK," key inputs will not be recognized because the oscillator is disabled which prevents the circuit from drawing excessive current.

2. "DIAL" MODE

When "OFF-HOOK," the device senses key down condition by detecting one key input and enters the key's code into at on-chip memory.

The memory can be store up to 32 digits, and it allows key strobes to be entered at rates comparable to tone dialing telephone. Output pulsing will continue until all entered digits have been dialed. To implement the pulse dialer function, two outputs, one to pulse the telephone line and one to mute the receiver, are provided.

3. "REDIAL" MODE

The first 32 digits entered will be stored in the on-chip redial memory and can be redialed by pressing either * or #, provided that the receiver is "ON-HOOK" for minimum ton (on hook time required to clear memory).

4. POWER UP CLEAR

The on-chip "POWER UP CLEAR" circuit reliable operation of the device. If the supply to the circuit is not sufficient to retain data in the memory, a "POWER UP CLEAR" will help regaining a proper supply level.

This function will prevent the "Redial" or sportaneous outputing of incorrect data.

TIMING CHARACTERISTICS

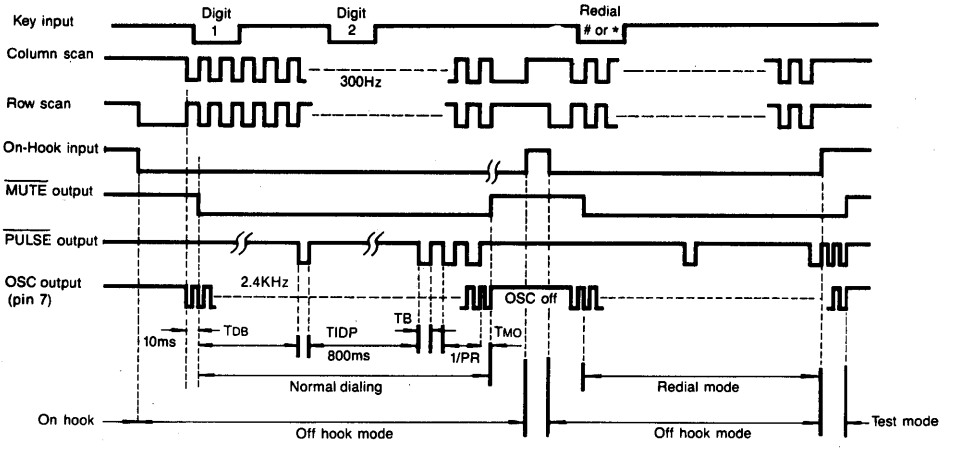


Fig. 2

1. V_{DD} (Pin 1)

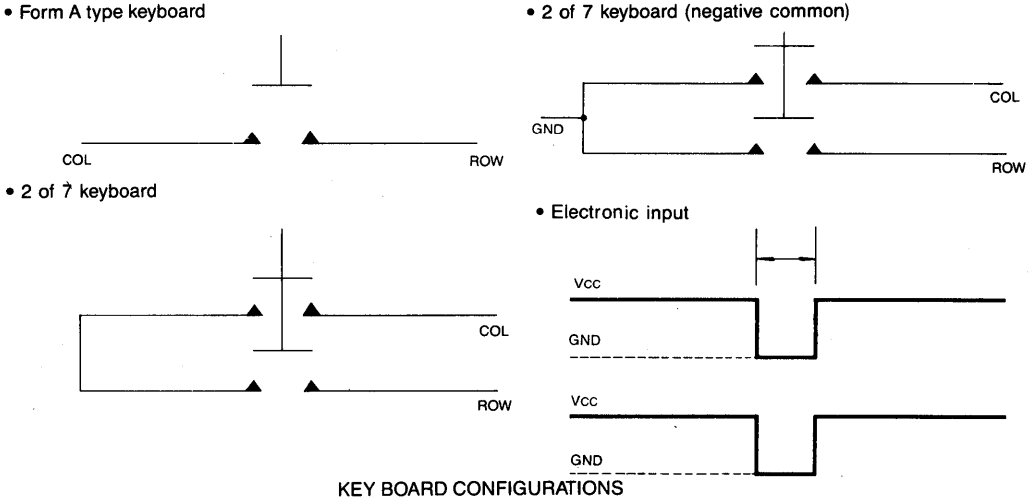
This is positive supply pin. The voltage on this pin is measured relative to Pin 6 and is supplied from a 150μA current source. This voltage should be regulated to less than 6.0 volts using on external form or regulation.

2. Keyboard inputs (Pin 2, 3, 4, 11, 12, 13, 14)

The KS5853 incorporates an innovative keyboard scheme that allows either the standard 2-of-7 keyboard with negative common or the inexpensive single contact (form A) keyboard to be used.

A valied key entry is defined by either a single row being connected to a single column or GND being simultaneously presented to both a single row and column. When in the on-hook mode, the row and column inputs are held high and no keyboard inputs are accepted.

When off-hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled and the rows and columns are alternately scanned (pulled high, then low) to verify the input is varied. The input must remain valid continuously for 14-20 msec of debounce time to be accepted.



KEY BOARD CONFIGURATIONS

3. GND (Pin 5)

This is the negative supply pin and is connected to the common part in the general applications.

4. OSCILLATOR (Pin 6, 7, 8)

The KS5853 contains on-chip inverters to provide oscillator which will operate with a minimum external components.

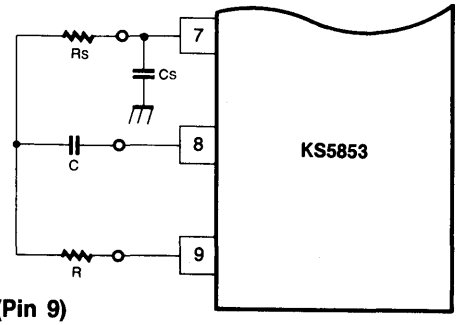
Following figure shows the on-chip configuration with the necessary external components. Optimum stability occurs with the ratio $K = R_S/R$ equal to 6.67.

The oscillator period is given by:

$$T = RC\ \{1.386 + (3.5K_{CS})/C\text{-}(2K/CK + 1)\ \text{In}\ CK/(1.5K + 0.5)\}$$

Where C_S is the stray capacitance on Pin 6.

Accuracy and stability will be enhanced with this capacitance minimized.



5. MAKE/BREAK (Pin 9)

The MAKE/BREAK pin controls the MAKE/BREAK ratio of the pulse output. The MAKE/BREAK ratio is controlled by connection V_{DD} or GND to this pin as shown in the following table.

Input	Make	Break
V_{DD} (Pin 1)	33.4%	66.6%
GND (Pin 5)	40%	60%

6. $\overline{\text{MUTE}}$ OUTPUT (Pin 10)

The mute output is an open-drain N-channel transistor designed to drive external bipolar transistor.

This circuitry is usually used to mute the receiver during outpulsing. As shown in Fig. 2 the KS5853 mute output turns on (pulls to the V_{GND}-supply) at the beginning of the predigital pause and turns off (goes to an open circuit) following the last break.

The delay from the end of the last break until the mute output turns off is mute overlap and is specified as t_{MO}.

7. ON-HOOK/TEST (Pin 15)

This pin detects the state of the hook switch contact "OFF HOOK" corresponds to V_{SS} condition. "ON HOOK" corresponds to V_{DD} condition. When outpulsing in this mode, which can be up to 300msec, is completed, the circuit is deactivated and will require current only necessary to sustain the memory and power-up-clear detect circuitry (refer to the electrical specifications).

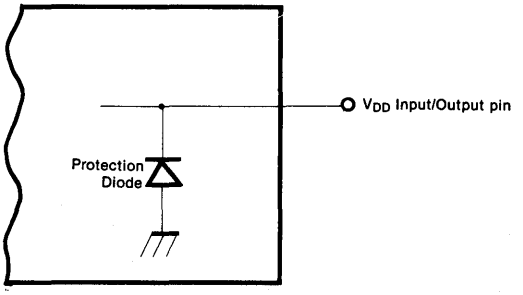
Upon retuning off-hook, a negative transistion on the mute output will insure the speech network is connected to the line. If the first key entry is either a * or #, the number sequence stored on-chip will be outpulsed. Any other valid key entries will clear the memory and outpulse the new number sequence.

8. $\overline{\text{PULSE}}$ OUTPUT (Pin 16)

The pulse output is an open drain N-channel transistor designed to drive external bipolar transistor. These transistor would normally be used to pulse the telephone line by disconnecting and connecting the network. The KS5853 pulse output is an open circuit during make and pulls to the GND supply during break.

9. ESD PROTECTION

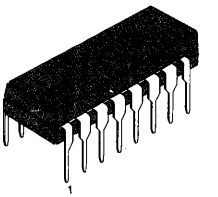
All Input/Output pins are protected ESD.



DUAL TONE MULTI FREQUENCY DIALER

The KS5808 is a monolithic integrated circuit fabricated using CMOS process and is designed specifically for integrated tone dialer applications.

16 DIP



FUNCTIONS

- Fixed supply operation
- Negative-true keyboard input
- Tone disable input
- Stable-output level

FEATURES

- **Minimum number of external parts required.**
- **High accuracy tones.**
- **Digital divider logic, resistive ladder network and CMOS operational amplifier on single chip.**
- **Uses inexpensive 3.579545 MHz television color burst crystal.**
- **Invalid key entry can result in either single tone or no tone.**
- **Tone disable allows any key down output to function from keyboard input without generating tones.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KS5808N	16 DIP	−30 ~ +60°C

BLOCK DIAGRAM

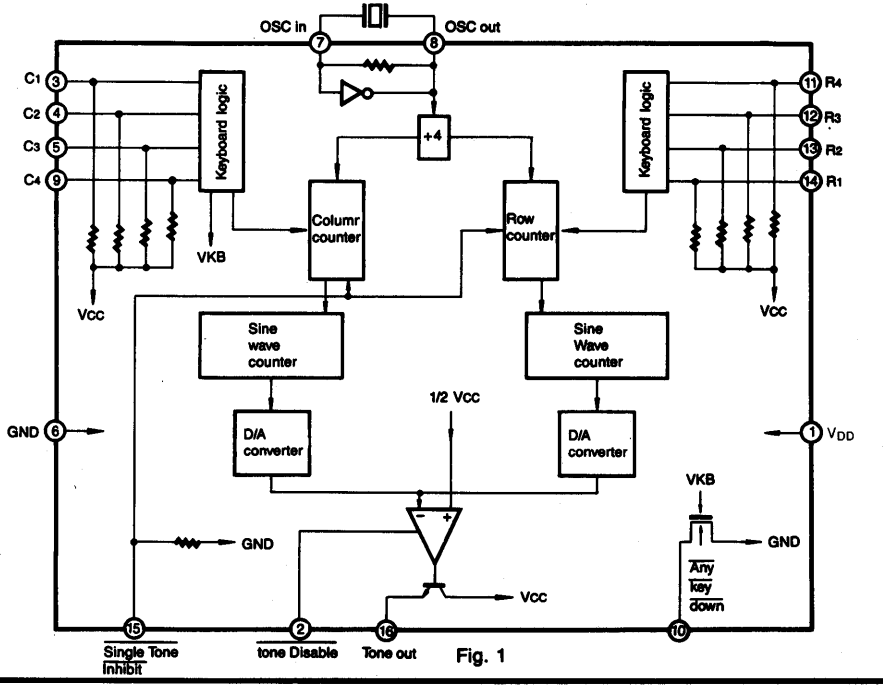


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	10.5	V
Any Input Relative to V_{DD} (Except Pin 10)	V_N	0.3	V
Any Input Relative to GND (Except Pin 10)	V_N	−0.3	V
Power Dissipation	P_D	500	mW
Operating Temperature	Topr	−30 ~ +60	°C
Storage Temperature	Tstg	−65 ~ +150	°C

3

ELECTRICAL CHARACTERISTICS

(−30°C<T_a<60°C unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		3		10	V
Input "0"	V_{IL}		0		0.3V_{CC}	V
Input "1"	V_{IH}		0.7V_{CC}		V_{CC}	V
Input Pull-Up Resistor	R_I		20		100	KΩ
$\overline{\text{Tone Disable}}$	$\overline{TD}$	Note 4	0		0.3V_{CC}	V
Tone Output	V_{OUT}	Note 1	−10		−7	dBm
Preemphasis, High Band			2.4	2.7	3	dB
Output Distortion, Measured in Terms of Total Out-of-Band Power Relative to RMS sum of Row and Column fundamental Power		Note 2			−20	dB
Rise Time	T_{RISE}	Note 3		2.8	5	mS
$\overline{\text{Any Key Down}}$ Sink Current to GND	I_{AKD}	At V_{OUT}=0.5V	500			uA
$\overline{\text{ADK}}$ Off Leakage Current	I_{AKDO}	At V_{OUT}=5V			2	uA
Supply Current Operating	I_{OD}	At V_{DD}=3.5V Note 6			2	mA
Supply Current Standby	I_{DD}	At V_{DD}=10V Note 5			200	uA
Tone Output-No Key Down	NKD				−80	dBm

Note: 1. Single-tone, low-group. Any V_{DD} between 3.4V and 3.6V, odBm=0.775V, R_{LOAD}=10K see test circuit Fig 2.
2. Any dual-tone. Any V_{DD} between 3.4V to 10.0V.
3. Time from a valid keystroke with no bounce to allow the waveform to go from min to 90% of the final magnitude of either frequency. Crystal parameters defined as R_S=100Ω L=96mH, C=0.02pF, and C_h=5pF, V_{DD} ≧3.4V, f=3.57954MHz±0.02%.
4. Only tones will be disabled when $\overline{TD}$ is taken to logical "0". Other chip functions may activate. Pull-up resistor on $\overline{TD}$ input will meet same spec as other inputs. Logic 0=GND
5. Stand-by condition is defined as no keys activated, $\overline{TD}$=Logical 1, $\overline{\text{Single Tone Inhibit}}$=Logical 0.
6. One key depressed only. Outputs unloaded.

PIN CONNECTIONS

PIN 1: Supply Voltage V_{DD}
PIN 2: $\overline{\text{Tone Disable}}$ Input
PIN 3: $\overline{\text{Column Input}}$ C_1
PIN 4: $\overline{\text{Column Input}}$ C_2
PIN 5: $\overline{\text{Column Input}}$ C_3
PIN 6: GND
PIN 7: OSC IN
PIN 8: OSC OUT
PIN 9: $\overline{\text{Column Input}}$ C_4
PIN 10: $\overline{\text{Any Key Down}}$
PIN 11: $\overline{\text{Row Input}}$ R_4
PIN 12: $\overline{\text{Row Input}}$ R_3
PIN 13: $\overline{\text{Row Input}}$ R_2
PIN 14: $\overline{\text{Row Input}}$ R_1
PIN 15: $\overline{\text{Single Tone Inhibit}}$
PIN 16: Tone Output

Tone Output Test Circuit

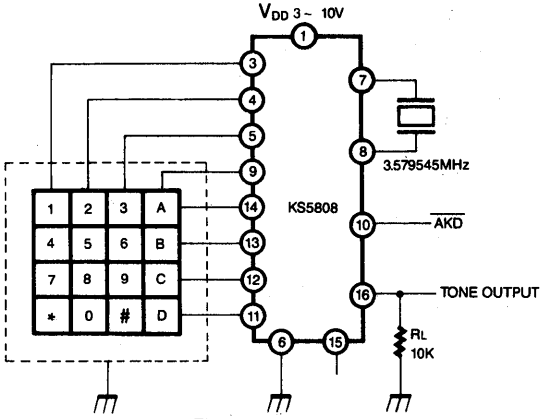


Fig. 2

FUNCTION DESCRIPTION

1. Oscillator

The network contains an on-board inverter with sufficient loop gain to provide oscillation when used with a low cost television color-burst crystal. The inverter's input is osc in (pin 7) and output is osc out (pin 8). The circuit is designed to work with a crystal cut to 3.579545MHz to give the frequencies in table 1. The oscillator is disabled whenever a keyboard input is not sensed.

Table 1: Standard DTMF and output frequencies of the KS5808

Item / Key	f	Standard DTMF Hz	Tone Output Frequency using 3.57954MHz Crystal Hz	Deviation from Standard %
ROW	f1	697	701.3	+0.62
	f2	770	771.4	+0.19
	f3	852	857.2	+0.61
	f4	941	935.1	−0.63
COL	f5	1209	1215.9	+0.57
	f6	1336	1331.7	−0.32
	f7	1477	1471.9	−0.35
	f8	1633	1645.0	+0.73

Most crystals don't vary more than 0.02%. Any crystal frequency deviation from 3.5795MHz will be reflected in the tone output frequency.

2. Output Waveform

The row and column output waveforms are shown in Figure 3. These waveforms are digitally synthesized using on-chip D/A converters. Distortion measurement of these unfiltered waveforms will show a typical distortion of 7% or less. The on-chip operational amplifier of the KS5808 mixes the row and column tones together to result in a dual-tone waveform.

Spectral analysis of this waveform will show that typically all harmonic and intermodulation distortion components will be −30dB down when referenced to the strongest fundamental (column tone). Figures 6 and 7 show a typical dual tone waveform and its spectral analysis.

Typical Sinewave Output

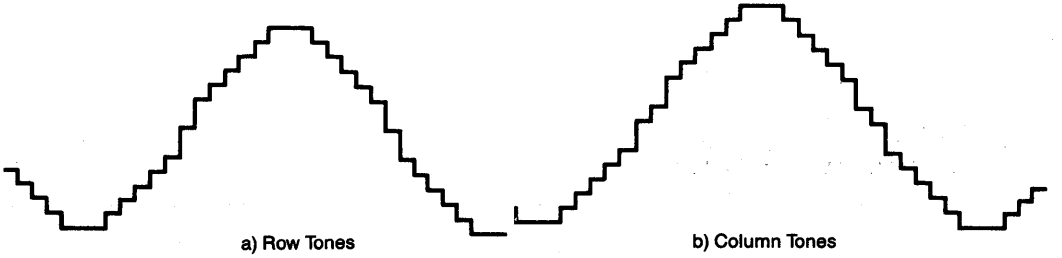


Fig. 3

3. Output Tone Level

The output tone level of the KS5808 is proportional to the applied DC supply voltage. Operation will normally be with a requlated supply. This results in enhanced temperature stability, since the supply voltage may be made temperature stable.

4. Keyboard Configuration

Each keyboard input is standard CMOS with a pull-up resistor to V_{CC}. These inputs may be controlled by a keyboard or electronic means. Open collector TTL or standard CMOS (operated off same supply as the KS5808) may be used for electronic control.

The switch contacts used in the keyboards may be void of precious metals, due to the CMOS network's ability to recognize resistance up to 1KΩ as a valid key closure.

2 of 8 DTMF keyboard

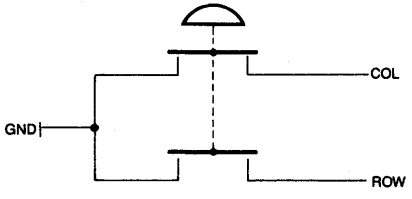


Fig. 4

Electronic Input Pulses

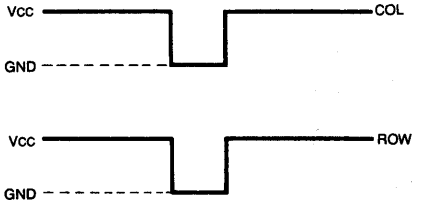


Fig. 5

TYPICAL DUAL TONE WAVEFORM

(ROW 1, Column 1)

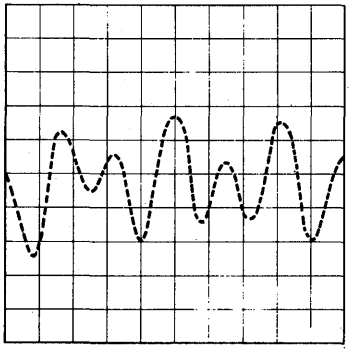


Fig. 6

SPECTRAL ANALYSIS OF WAVEFORM

(Vert: 10dB/Div, Hori: 1KHz/Div)

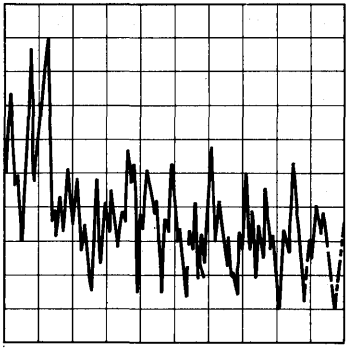


Fig. 7

POWER DISSIPATION VERSUS TEMPERATURE

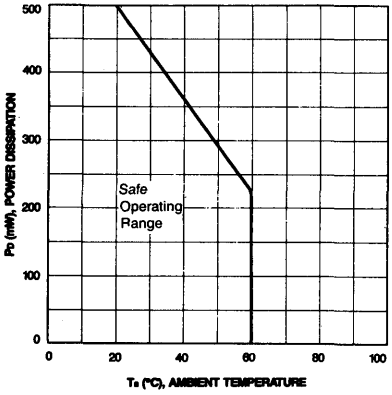


Fig. 8

PIN DESCRIPTIONS

1. Row and Column Input (Pin 3, 4, 5, 9, 11, 12, 13, 14)

With Single Tone Inhibit at V_{CC}, connection of GND to a single column will cause the generation of that column tone. Connection of GND to more than one column will result in no tones being generated. The application of GND to only a row pin or pins has no effect on the circuit. There must always be at least one column connected to GND for row tones to be generated. If a single row tone is desired, it may be generated by tying any two column pins and the desired row pin to GND. Dual tones will be generated if a single row pin and a single column pin are connected to GND.

2. Any Key Down Output (Pin10)

The any key down output is used for electronic control of receiver and/or transmitter switching and other desired functions. It switches to GND when a keyboard button is pushed and is open circuited when not. The AKD output switches regardless of the tone disable and single tone inhibit inputs.

3. Tone Disable Input (Pin 2)

The Tone Disable input is used to defeat tone generation when the keyboard is used for other functions besides DTMF signaling. It has a pull-up to V_{DD} and when tied to GND tones are inhibited. All other chip functions operate normally.

4. Single Tone Inhibit Input (Pin 15)

The Single Tone Inhibit input is used to inhibit the generation of other than dual tones. It has a pull-down to GND and when floating or tied to GND, any input situation that would normally result in a single tone will now result in no tone, with all other chip functions operating normally.

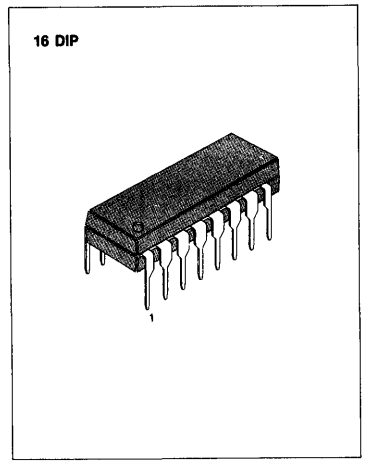
When forced to V_{DD} single or dual tones may be generated as described in the paragraph under row and column inputs.

5. Tone Output (Pin 16)

The tone output pin is connected internally in the KS5808 to the emitter of an NPN transistor whose collector is tied to V_{DD}. The input to this transistor is the on-chip operational ampifier which mixes the row and column tones together and provides output level regulation.

DTMF DIALER WITH REDIAL

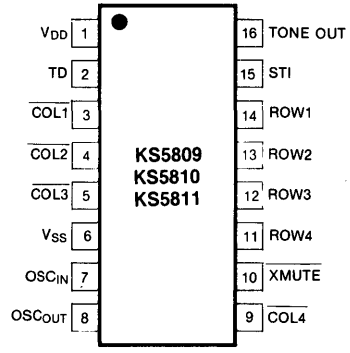
The KS5809/KS5810/KS5811 are monolithic CMOS Integrated circuit which use an 3.579545MHz oscillator for its frequency reference and provides all the features required for implementing a tone dialer.
The required sinusoidal wave form for each individual tone is digitally synthesized on the chip. The wave form so generated has very low total harmonic distortion (7 % Max). A voltage reference is generated on the chip.



FEATURES

- **Wide supply voltage range (2.0~5.5V)**
- **Low power dissipation**
- **Use inexpensive TV crystal (3.579545MHz)**
- **Tone disable input**
- **Low standby current**
- **Continuous mute**
- **Uses either the inexpensive Form A type keyboard or the standard 2 of 7 matrix keyboard with negative common**

PIN CONFIGURATION



ORDERING INFORMATION

Device	Redial Function	Operating Temperature
KS5809N	No Redial	−20 ~ +70°C
KS5810N	Column 4 Key (A, B, C, D) Redial	
KS5811N	# Key Redial	

ARRANGEMENT OF KEYBOARD

1	2	3	A
4	5	6	B
7	8	9	C
*	0	#	D

DTMF FREQUENCIES

Input	Specified	Actual	% Error
R_1	697	699.1	+0.31
R_2	770	766.2	−0.49
R_3	852	847.4	−0.54
R_4	941	948.0	+0.74
C_1	1209	1215.7	+0.57
C_2	1336	1331.7	−0.32
C_3	1477	1471.9	−0.35
C_4	1633	1645.0	+0.73

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	6.0	V
Input Voltage	V_{IN}	$V_{SS}-0.3$, $V_{DD}+0.3$	V
Output Voltage	V_{OUT}	$V_{SS}-0.3$, $V_{DD}+0.3$	V
Operating Temperature	T_a	$-20 \sim +70$	°C
Storage Temperature	T_{stg}	$-40 \sim +125$	°C
Power Dissipation	P_D	500	mW

ELECTRICAL CHARACTERISTICS

($V_{DD}=3.5V$, $V_{SS}=0V$, $f_{osc}=3.579545MHz$, $Ta=25°C$, unless otherwise specified)

Characteristic	Symbol	Test Condition		Min	Typ	Max	Unit
Supply Voltage	V_{DD}			2.0		5.5	V
Memory Retention Voltage	V_{DR}			1.0			V
Key Input High Voltage	V_{IH}	$R_1 \sim R_4$, $C_1 \sim C_4$		0.8 V_{DD}		V_{DD}	V
Key Input Low Voltage	V_{IL}			V_{SS}		0.2 V_{DD}	V
Operating Current	I_{DD}	All outputs unloaded.			1.0	2.0	mA
Output Leakage Current	I_{OL}	$V_{DD}=5.5V$				1.0	μA
Oscillator Frequency	f_{osc}				3.57954		MHz
Valid Key Entry Time	T_{KD}			23		25.3	mS
Tone Output	V_{or}	ROW TONE ONLY	$V_{DD}=2.5V$, $R_L=5K$	−16.0		−12.0	dBV
			$V_{DD}=3.5V$, $R_L=5K$	−14.0		−11.0	dBV
Ratio of Column to Row Tone	dB_{cr}			1.0	2.0	3.0	dB
Distortion	% DIS				1.2	7	%

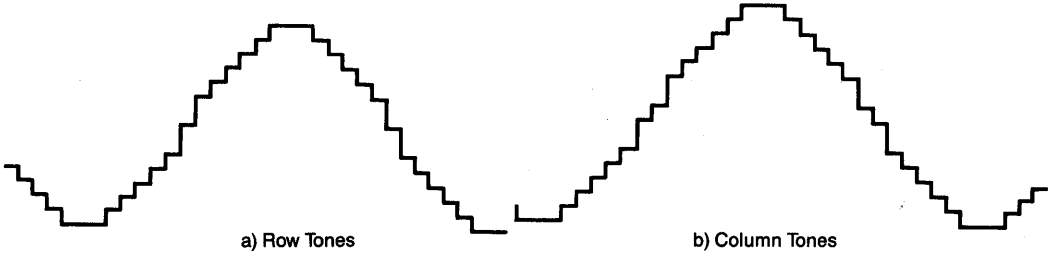
FUNCTION DESCRIPTION

1. Oscillator

When Tone Disable is connected V_{SS} oscillator is disable. This oscillator inhibit prevents the circuit from drawing excessive current. The circuit is designed to work with a crystal out to 3.579545MHz to tone frequency.

2. Output Waveform

The Row and Column output waveforms are shown in Fig. 1. These waveforms are digitally synthesized using a on-chip D/A converter. Distortion measurement of these unfiltered wavefforms will show a typical distortion of 7% or less. The on-chip OP AMP of the KS5809/5810/5811 mix the Row and Column tones together to result in a dual tone waveform.



a) Row Tones b) Column Tones

Fig. 1

PIN DESCRIPTION

1. V_{DD} (Pin 1)

This is the positive supply Pin.
The voltage on this Pin is measured relative to V_{SS} (Pin 6).

2. Tone Disable (Pin 2)

When tone disable input is connected to V_{SS}, key input and oscillator are disabled. When this pin is connected to V_{DD}, key input is sensed.

3. Keyboard Inputs (Pin 3, 4, 5, 9, 11, 12, 13, 14)

The KS5809/5810 can use inexpensive Form A keyboard, standard 2-of-7 keyboard or standard 2-of-7 keyboard with negative common. The KS5811 can use standard 2-of-8 keyboard or standard 2-of-8 keyboard with negative common (refer to Fig. 2, Fig. 3, Fig. 4). A valid key entry is defined by either a single Row being connected to a single column or V_{SS} being simulateneously presented to both a single Row and Column. When tone disable $-V_{SS}$, the Row and Column inputs are held high and no keyboard inputs are accepted.
When tone disable $-V_{DD}$ the keyboard is completely static until the initial valid key input is sensed.
The oscillator is then enabled and the Rows and Columns are alternately scanned to verify the input is varied (refer to Fig. 5).

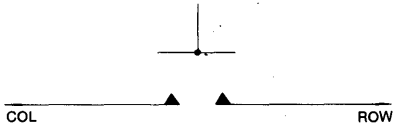


Fig. 2 Form A Keyboard

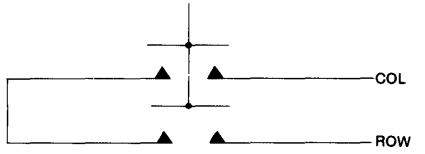


Fig. 3 2 of 7 (2 of 8) Keyboard

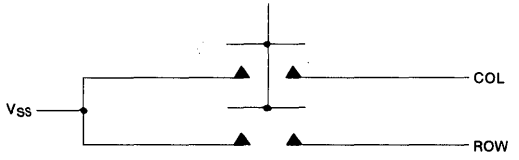


Fig. 4 2 of 7 (2 of 8) Keyboard Negative Common

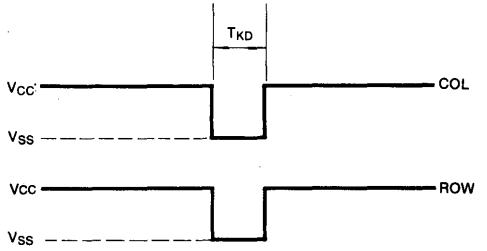


Fig. 5 Electronic Input

4. V_{SS} (Pin 6)

This is the negative supply pin and is connected to a common part in a general application.

5. Oscillator In (Pin 7), Oscillator Out (Pin 8)

The network contains an on-board inverter with sufficient loop gain to provide oscillation. The inverter input is Oscillator In, output is Oscillator Out.

6. $\overline{\text{XMUTE}}$ (Pin 10)

The XMUTE output is a N-channel open drain.

Key-in \ $\overline{\text{Tone-Dis}}$	Connected to V_{SS}	Connected to V_{DD}
Key is sensed	ON	ON
Key is no sensed	ON	OPEN

ON: $\overline{\text{XMUTE}}$ is connected to V_{SS}
OPEN: $\overline{\text{XMUTE}}$ is opened

7. Single Tone Enable (Pin 15)

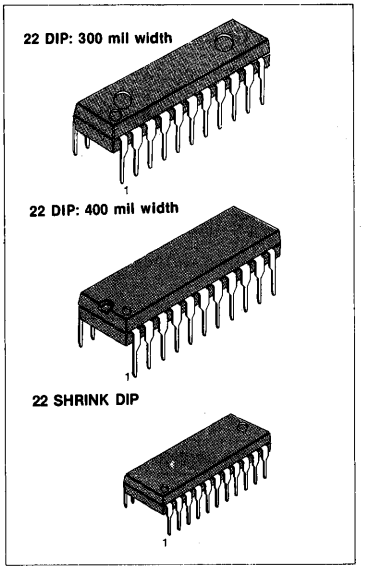
The single tone enable input is used to generate a single tone for test. It has pull down to V_{SS} and when floating or tied to V_{SS}, single tone is inhibited. When tied to V_{DD}, single tone is enabled.

8. Tone Output (Pin 16)

The tone out is connected internally in the KS5809/5810/5811 to the emitter of an NPN transistor whose collector is tied to V_{DD}. The input to this transistor is the on-chip OP AMP which mixes the Row and Column tones together and provides output level regulation.

TONE/PULSE DIALER WITH REDIAL

The KS5819 is a DTMF/PULSE switchable dialer with a 32-digit redial memory. Through pin selection, switching from pulse to DTMF mode can be done using a slide switch or by depressing [T] key. All necessary dual-tone frequencies are derived from a 3.579545MHz TV crystal, providing very high accuracy and stability. The required sinusoidal wave form for each individual tone is digitally synthesized on the chip. The wave form so generated has very low total harmonic distortion (7% max). A voltage reference is generated on the chip which is stable over the operating voltage and temperature range and regulates the signal levels of the dual tones to meet telephone industry specifications. CMOS technology is applied to this device, for very low power requirements, high noise immunity, and easy interface to a variety of telephones requiring few external components.



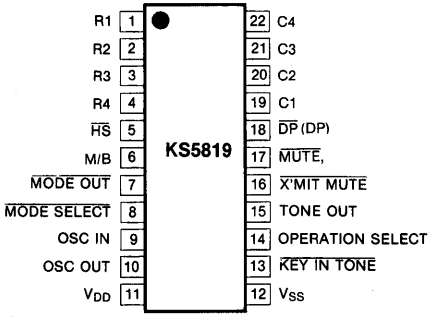
FEATURES

- **Tone/Pulse switchable (touch key or slide switch).**
- **32 digit capacity for redial**
- **Automatic mix redialing (last number dial) of PULSE→DTMF with multiple auto access pause (3.5 sec)**
- **Key-in-tone output for valid key entry in pulse mode (Fkf = 1.75KHz, Tkf = 23mS).**
- **Low power CMOS process (2.0 to 5.5V)**
- **Numbers dialed manually after redial are cascadable and stored as additional numbers for next redialing**
- **Uses inexpensive TV crystal (3.579545MHz)**
- **Make/Break ratio (33 1/3~66 2/3 or 40/60) pin selectable**
- **Touch key hooking (604ms)**
- **Low standby current**
- **4 x 4 or (2 of 8) keyboard available**

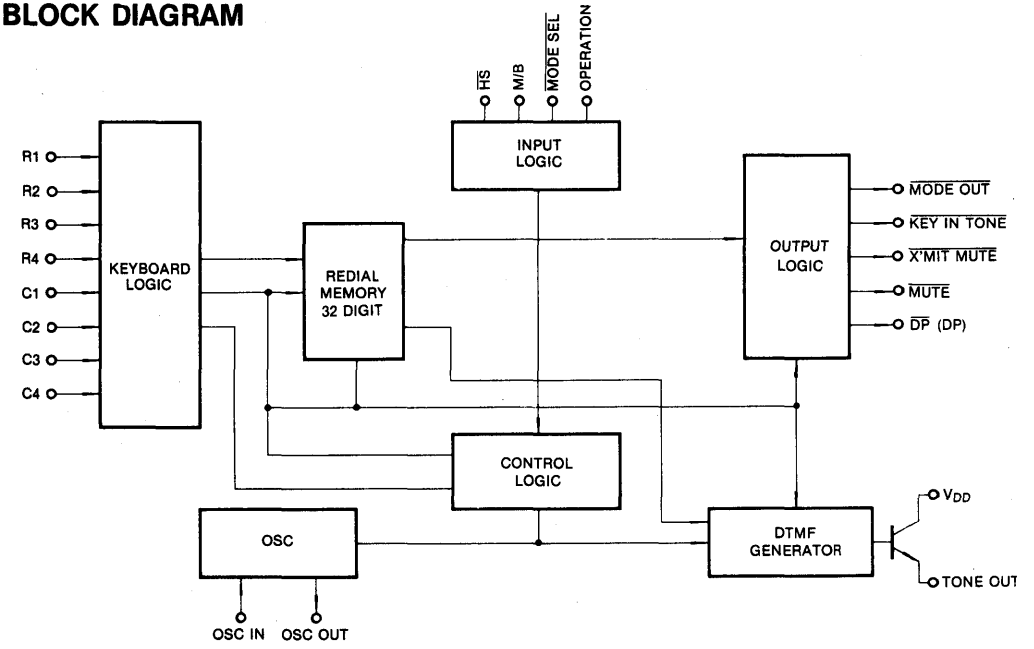
ORDERING INFORMATION

Device	Package	Dial Pulse	PPS
KS58A19N	300mil	DP	10
KS58B19N	Width	DP	20
KS58C19N	Size	$\overline{DP}$	10
KS58D19N		$\overline{DP}$	20
KS58A19E	400mil	DP	10
KS58B19E	Width	DP	20
KS58C19E	Size	$\overline{DP}$	10
KS58D19E		$\overline{DP}$	20
KS58A19P	Shrink	DP	10
KS58B19P	Package	DP	20
KS58C19P	Type	$\overline{DP}$	10
KS58D19P		$\overline{DP}$	20

PIN CONFIGURATION



BLOCK DIAGRAM



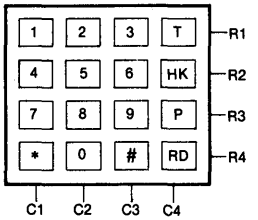
TONE DURATION & PAUSE IN REDIAL

Characteristic	Symbol	Typ	Unit
Tone Duration	T_D	110	mS
Minimum Pause	ITP	110	mS
Cycle Time	T_C	220	mS

TONE FREQUENCIES

Input	Specified	Actual	% Error
R1	697	699.1	+0.31
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.7	+0.57
C2	1336	1331.7	−0.32
C3	1477	1471.9	−0.35

ARRANGMENT OF KEYBOARD



T : PULSE-DTMF SWITCHING
HK : HOOKING (604ms)
P : PAUSE (3.5 second)
RD : REDIAL

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{DD}	6.0	V
Input Voltage	V_{IN}	$V_{SS}-0.3$, $V_{DD}+0.3$	V
Output Voltage	V_{OUT}	$V_{SS}-0.3$, $V_{DD}+0.3$	V
Output Voltage	V_{OUT}	$\leqq V_{DD}$ ($\overline{DP}$, $\overline{MUTE}$, $\overline{XMUTE}$)	V
Tone Output Current	I_{TONE}	50	mA
Power Dissipation	P_D	500	mW
Operating Temperature	T_{opr}	$-20 \sim +70$	°C
Storage Temperature	T_{stg}	$-40 \sim +125$	°C

ELECTRICAL CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 3.5V, fx'tal = 3.579545MHz, Ta = 25°C, unless otherwise noted)

Characteristic	Symbol	Test Conditions			Min	Typ	Max	Unit
Operating Voltage Range	V_{DDP}	Pulse Mode	All inputs connected to V_{DD} or V_{SS}		2.0		5.5	V
	V_{DDT}	Tone Mode			2.0		5.5	
Memory Retention Voltage	V_{DR}				1.0			V
Operating Supply Current	I_{DDP}	$\overline{MODE} = V_{DD}$	One key selected $\overline{HS} = V_{SS}$. All outputs unloaded			0.3	0.5	mA
	I_{DDT}	$\overline{MODE} = V_{SS}$				0.5	1.0	
Standby Current	I_{SD1}	$\overline{HS} = V_{DD} = 1.5V$	No key selected. All outputs unloaded				0.05	μA
	I_{SD2}	$\overline{HS} = V_{SS}$					50	
Output Current	I_{OL1}	$\overline{DP}$, $\overline{MUTE}$ $\overline{XMUTE}$	$V_{OL} = 0.4V$	$V_{DD} = 3.5V$	1.7	5.0		mA
	I_{OL2}			$V_{DD} = 2.5V$	0.5	1.5		
Output Leakage Current	I_{OFF}	$\overline{MODE\ OUT}$, $\overline{KT}$	$V_{OUT} = 2.5V$				1.0	μA
Input Voltage	V_{IH}	R1-R4, C1-C3, $\overline{HS}$, M/B			$0.8V_{DD}$		V_{DD}	V
	V_{IL}	OPERATION SELECT, $\overline{MODE\ SELECT}$			V_{SS}		$0.2V_{DD}$	
Input Current	I_{IN1}	$V_{DD} = 3.5V$ $V_{IN} = 0V$	R1-R4				116	μA
	I_{IN2}	$V_{DD} = 2.5V$ $V_{IN} = 0V$					50	
Valid Key Entry Time	T_{kd}				23		25.3	mS
Column and Row Scanning Frequency	F_{cr}					437		Hz
Key-In Tone Output Duration	T_{kt}					23		mS
Key-In Tone Frequency	F_{kt}					1.75		KHz
Auto Access Pause Time	T_{ap}					3.5		sec
Tone Output	V_{or}	$V_{DD} = 2.5V$, $R_L = 5K$	ROW TONE ONLY		−16.0		−12.0	dBV
		$V_{DD} = 3.5V$ $R_L = 5K$			−14.0		−11.0	
Ratio of Column to Row Tone	dB_{cr}	$V_{DD} = 3.5V$			1.0	2.0	3.0	dB
Distortion	%DIS	$V_{DD} = 3.5V$					7	%
Tone Output Delay Time	T_{psd}					1.5		mS

PIN DESCRIPTION

<table>
<tr><th>Pin</th><th>Name</th><th>Description</th></tr>
<tr><td>1-4
15-22</td><td>R1-R4
C1-C4</td><td>Keyboard (R1, R2, R3, R4, C1, C2, C3, C4)
These inputs can be interfaced to an XY matrix keyboard. $C_1 \sim C_4$ & $R_1 \sim R_4$ are set to low at On Hook ($\overline{HS}$ = high). $C_1 \sim C_4$ key inputs are set to low and R1-R4 are set to high at OFF HOOK ($\overline{HS}$ = low) which enables the key-input operation. Oscillator starts running when a key press is detected.
Scanning signals are presented at both column and row inputs (TYP: 437Hz) until the input key is released. Key inputs are compatible with standard 2-of-8 form or single-contact keyboard. Debouncing is provided to avoid false entry (TYP: 25mS).</td></tr>
<tr><td>5</td><td>$\overline{HS}$</td><td>Hook Switch
This input detects the state of the hook switch contact.
"Off Hook" corresponds to V_{SS} condition.
"On Hook" corresponds to V_{DD} condition.</td></tr>
<tr><td>6</td><td>M/B</td><td>Make/Break Ratio
This input provides the selection of the Make/Break ratio (33.3: 66.6/40:60) when M/B is connected to V_{DD}/V_{SS}.</td></tr>
<tr><td>7</td><td>$\overline{\text{MODE OUT}}$</td><td>Mode Output
This output indicates whether the chip is operating in pulse or tone mode. Pulse/Tone mode corresponds to OFF/ON state (N channel open drain). Mode state is controlled with Operation Select, $\overline{\text{Mode Select}}$ and [T] key inputs.</td></tr>
<tr><td>8</td><td>$\overline{\text{MODE SELECT}}$</td><td>Mode Select Input
Pulse/DTMF mode is selected as shown in the following table.
Initial Mode means the state after going Off Hook ($\overline{HS} \rightarrow$"$V_{SS}$")
<table>
<tr><th>OPERATION SELECT</th><th>$\overline{\text{MODE SELECT}}$</th><th>INITIAL MODE</th><th>SWITCHING ENTRY MODE</th><th>NOTES</th></tr>
<tr><td rowspan="2">V_{DD}</td><td>V_{DD}</td><td>Pulse</td><td>[T] Key-In</td><td rowspan="2">$\overline{\text{MODE SELECT}}$ defines only initial mode after going Off Hook and is latched at first key entry.</td></tr>
<tr><td>V_{SS}</td><td>Tone</td><td>N/A</td></tr>
<tr><td rowspan="2">V_{SS}</td><td>V_{DD}</td><td>Pulse</td><td>$\overline{\text{MODE SELECT}}$ input = V_{SS}</td><td rowspan="2">[T] key is disabled under this condition.</td></tr>
<tr><td>V_{SS}</td><td>Tone</td><td>N/A</td></tr>
</table>
If choice of switching method is desired (either [T] key or $\overline{\text{MODE SELECT}}$). Operation select should be connected to $\overline{\text{MODE SELECT}}$ in order to avoid false operation.</td></tr>
<tr><td>9
10</td><td>OSC IN
OSC OUT</td><td>Oscillator Input/Output
These pins are provided to connect an external 3.58MHz crystal. Oscillator starts (at Off Hook) and is sustained until pulse or DTMF signal are finished.</td></tr>
<tr><td>11
12</td><td>V_{DD}
V_{SS}</td><td>Power
These are the power supply inputs. The device is designed to be operated on 2.0V to 5.5V.</td></tr>
</table>

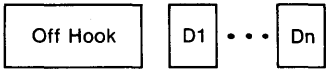
PIN DESCRIPTION (Continued)

<table>
<tr><th>Pin</th><th>Name</th><th>Description</th></tr>
<tr><td>13</td><td>$\overline{\text{KEY IN TONE}}$</td><td>Key In Tone Output
Key in tone signal is provided only in pulse mode for all Key-ins except [T] key-in. No $\overline{\text{KEY IN TONE}}$ is generated in DTMF mode. Fkt: 1.75KHz, Tkt: 23mS.
(N channel open drain)</td></tr>
<tr><td>14</td><td>OPERATION SELECT</td><td>Operation Select Input
Mode switching (from Pulse to DTMF) entry is selectable with this input, i.e. whether [T] key entry or $\overline{\text{MODE SELECT}}$ input entry is selectable.</td></tr>
<tr><td>15</td><td>TONE OUT</td><td>DTMF Signal Output
When a valid keypress is detected in DTMF mode appropriate low and high group frequencies are generated which hybrided the Dual Tone Output.
Tone out is Off State in pulse mode.</td></tr>
<tr><td>16</td><td>$\overline{\text{X'MIT MUTE}}$</td><td>$\overline{\text{X'mit Mute Output}}$
<table><tr><th>$\overline{\text{HS}}$</th><th>$\overline{\text{X'mit Mute Output}}$</th></tr><tr><td>$V_{DD}$</td><td>"ON"</td></tr><tr><td>V_{SS}</td><td>Normally "OFF"
"ON" during pulse and DTMF dialing</td></tr></table>(N channel open drain)</td></tr>
<tr><td>17</td><td>$\overline{\text{MUTE}}$</td><td>$\overline{\text{Mute Output}}$
<table><tr><th>$\overline{\text{HS}}$</th><th>$\overline{\text{MUTE OUTPUT}}$</th></tr><tr><td>$V_{DD}$</td><td>"ON"</td></tr><tr><td>V_{SS}</td><td>Normally "OFF" in DTMF mode.
"ON" during pulse dialing</td></tr></table>(N channel open drain)</td></tr>
<tr><td>18</td><td>$\overline{\text{DP}}$, DP</td><td>Dial Pulse Out. $\overline{\text{DP}}$: C/D, DP: A/B
DP: The normal output will be "OFF" during break and "ON" during make at "OFF HOOK."
The output will be "ON" at "ON HOOK,"
$\overline{\text{DP}}$: The normal output will be "ON" during break and "OFF" during make at "OFF HOOK."
The output will be "OFF" at "ON HOOK."</td></tr>
</table>

KEYBOARD OPERATION

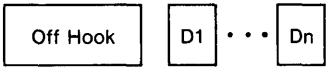
1. SINGLE MODE OPERATION

- **Pulse Mode Operation**

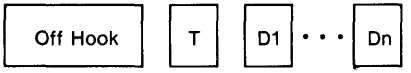


Pulse mode is defined by the initial mode after going Off Hook and latched at [D1] key entry. This is the condition under $\overline{\text{Mode Select}} = V_{DD}$.

- **Tone Mode Operation**

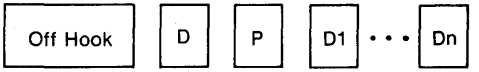


Tone mode is defined by the initial mode after going Off Hook and latched at [D1] key entry. This condition is under $\overline{\text{Mode Select}} = V_{SS}$.



If initial mode is at pulse mode after going Off Hook and $\overline{\text{Mode Select}} = V_{DD}$, Operation Select = V_{DD}. Switching mode from pulse to tone can be done by [T] key entry and latched at [D1] key entry.

- **Manual Dialing with Automatic Access Pause**

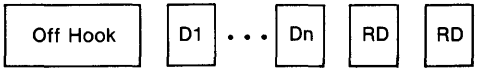


Multiple Pause key entries can be accepted and stored in the redial memory, each as a digit. Each [P] key provides 3.5 seconds pause time, but the [P] key entry as the first digit after going Off Hook is ignored. The [*] key can also be used as a pause key in the pulse mode. Pause (s) can be the cancelled with the [P] or [RD] key during pause time in redialing.

- **Redialing**

Up to 32 digits can be dialed with the [RD] key. The [RD] key is disabled while pulse or DTMF signals are transmitted. When more then 32 digits are stored, redial is also inhibited.
The [#] key can be used as the [RD] key in the pulse mode.

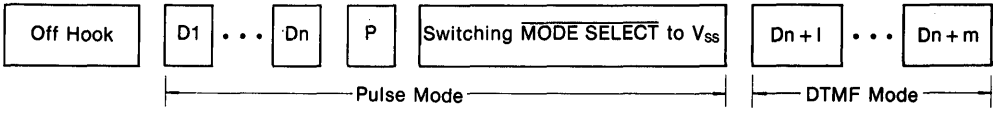
- **Inhibiting Redial**



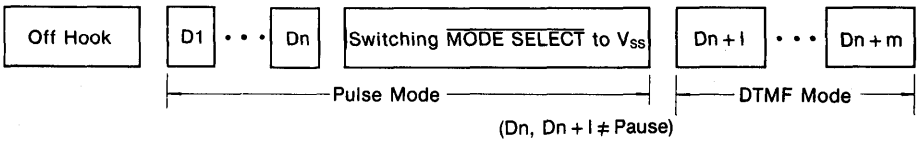
Redial can be inhibited by depressing the [RD] key twice after DTMF or pulse signals are transmitted.

2. PULSE/TONE SWITCHABLE OPERATION

• **Mode Switching by $\overline{\text{MODE SELECT}}$ Input (OPERATION SELECT = V_{SS})**

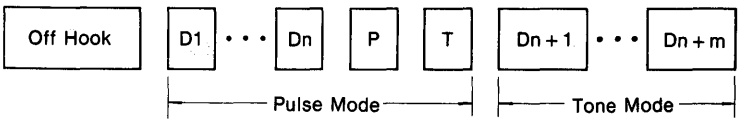


The pulse mode is initially defined $\overline{\text{MODE SELECT}} = V_{DD}$. Mode switching to the DTMF mode can be accepted by $\overline{\text{MODE SELECT}} = V_{SS}$. The DTMF mode will be set up after the pulse mode is finished. In this mode, digits [Dn+1] ... [Dn+m] are transmitted from Tone Out as DTMF signals by depressing the corresponding keys.
If no P key is contained serially before or after mode switching, the following condition is obtained.

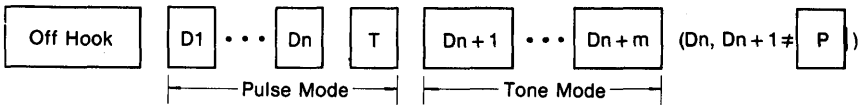


If digit [Dn+1] is depressed after the pulse mode is finished, the DTMF mode will be set up after the last pulse signal ([Dn]) is generated. In this mode, digits [Dn+1] ... [Dn+m] are transmitted from Tone Out as DTMF signals by depressing the corresponding keys. If digit [Dn+1] is depressed during dialing pulse signals, DTMF mode, in the Hold State, will be set after the last pulse signal [Dn] is finished. MODE OUT will flash to indicate this Hold State [Dn+1] ... [Dn+m] is stored in the redial memory as DTMF data and not transmitted from Tone Out. When it is ready to transmit the DTMF data in redial memory, the [T], [RD] or [P] key is depressed to reset this Hold State and [Dn+1] ... [Dn+m] data are serially transmitted.

• Mode Switching by [T] key (OPERATION SELECT = V_{DD})



The pulse mode is initially defined with $\overline{\text{MODE SELECT}} = V_{DD}$. Mode switching to the DTMF mode can be accepted by the [T] key. In the DTMF mode, digits [Dn+1] ... [Dn+m] are transmitted from Tone Out as DTMF signals by depressing the corresponding key. If no [P] key is contained serially before or after the [T] key, the following condition is obtained.



It results in the next condition:
If digit [Dn+1] is depressed after the pulse mode is finished, the DTMF mode will be set after the last pulse signal Dn is out. In this mode, digits [Dn+1] ... [Dn+m] are transmitted from TONE OUT as DTMF signals by depressing, the corresponding key.

If digit [Dn+1] is depressed during dialing pulse signal, the Hold State will be set after the last pulse signal [Dn] is finished. When DTMF MODE is set. MODE OUT will flash to indicate this Hold State.
Digits [Dn+1] ... [Dn+m] are stored in the redial memory as DTMF data and not transmitted from Tone Out.
When it is ready to transmit DTMF data in the redial memory, the [T], [RD] or [P] key is depressed to reset this Hold State and [Dn+1] ... [Dn+m] data are serially transmitted.

- Redial with Hold State Cancell

[Off Hook] [RD] [T] (or [P], [RD] key)

A pause can be cancelled with the [P], [T] or [RD] key in redialing. Any pause in series corresponding with a pause is also cancelled. When no pause is stored before or after mode switching, the chip will go into the Hold State when the DTMF mode is set up. MODE OUT will flash to indicate this Hold State. The DTMF data are stored in the redial memory and not transmitted from tone out.
The [T], [RD] or [P] key is depressed to reset this Hold State and the DTMF data are serially transmitted.

Single Tone Operation in DTMF Mode (Test mode)

1. The M/B pin is used to trigger the chip into the test mode by applying a positive or negative pulse after "Off Hook." The test mode is sustained until On Hook. The single tone is shown in the following table which contrast with the normal mode.

Normal mode

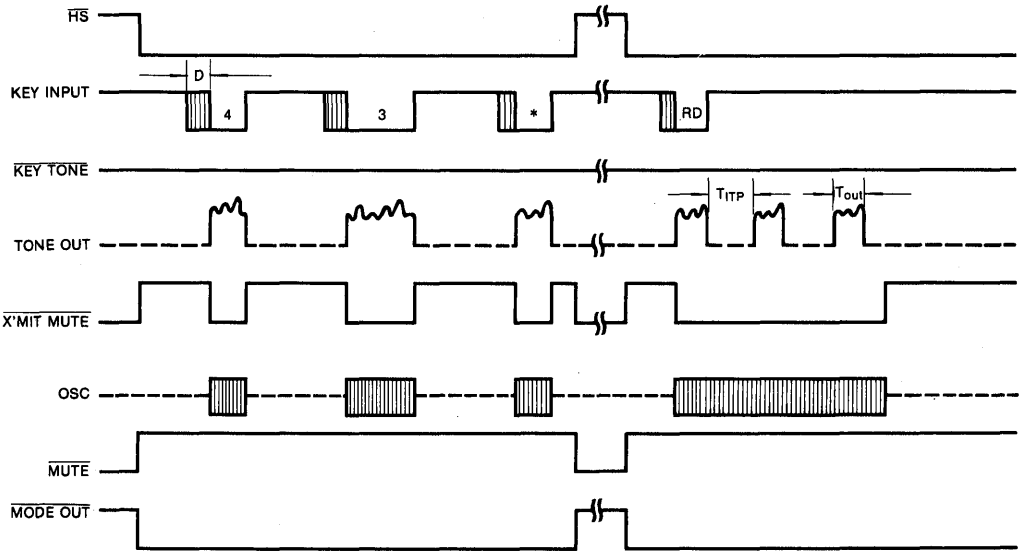
	C1	C2	C3
R1	1	2	3
R2	4	5	6
R3	7	8	9
R4	*	0	#

Single tone mode

	C1	C2	C3
R1	R1	C2	C3
R2	C1	C2	R2
R3	R3	C2	C3
R4	C1	R4	C3

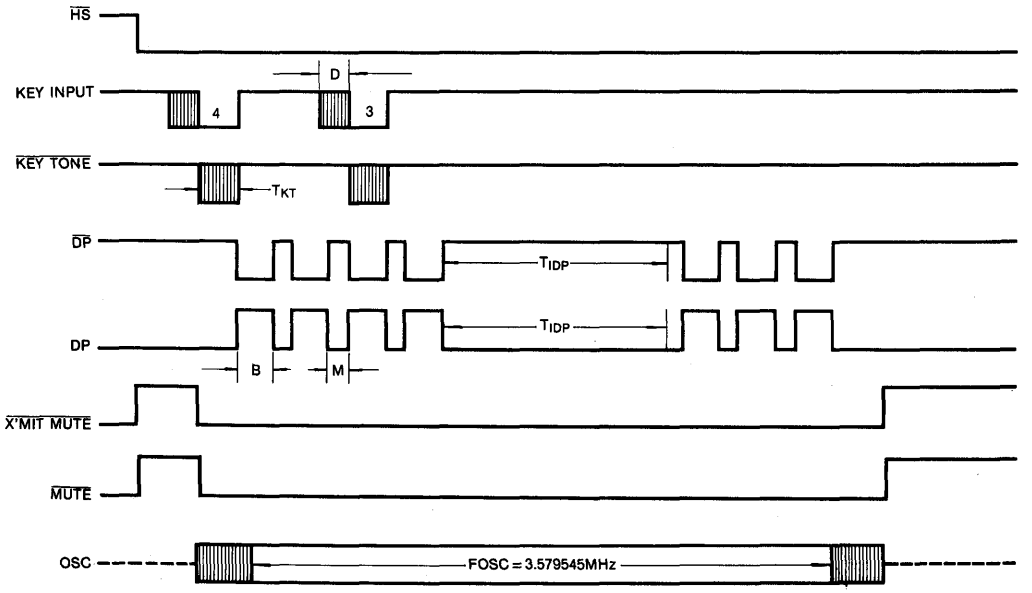
2. The single tone can be generated by simultaneously depressing two digit keys in the appropriate Row and Column. If tthe wo digit keys are not in the same Row or Column, the dual tone is disabled and no output is provided.

TONE MODE TIMING (MODE SELECT = V_{SS})



D: Debouncing time: 25mS
T_{ITP}: 110mS T_{out}: 110mS

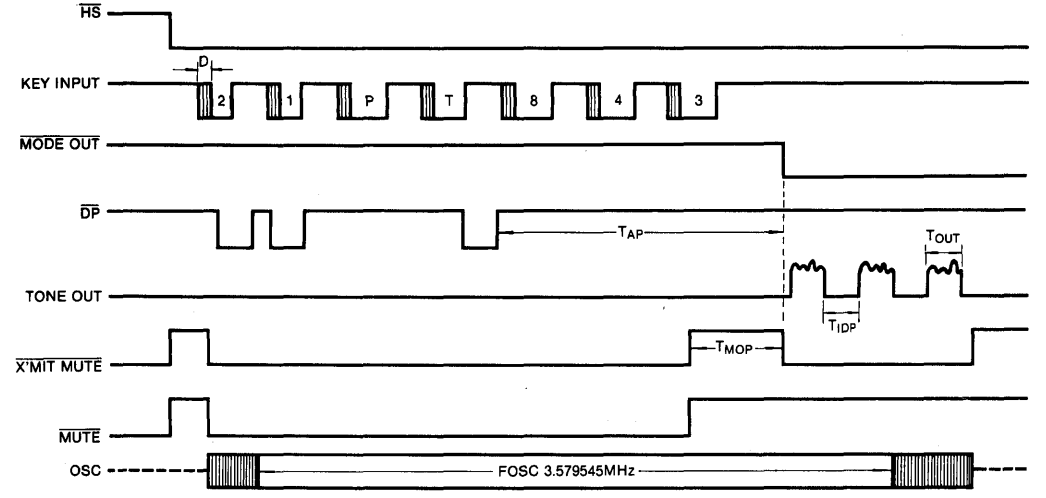
PULSE MODE TIMING ($\overline{\text{MODE SELECT}}$ = V_{DD})



D (Debouncing Time): 25mS T_{KT}: 23mS
T_{IDP}: 879mS f_{KT}: 1.75KHz

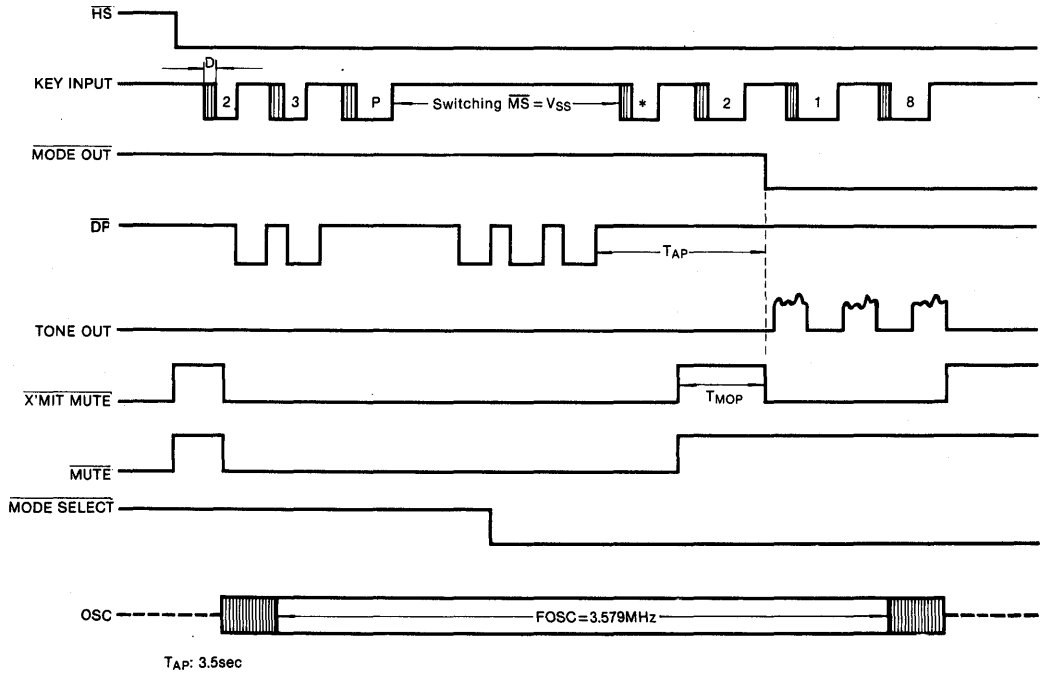
TIMING DIAGRAM

(for Switching Mode Operation by [T] key) (OPERATION SELECT, $\overline{\text{MODE SELECT}}$ = = V_{DD})



TIMING DIAGRAM

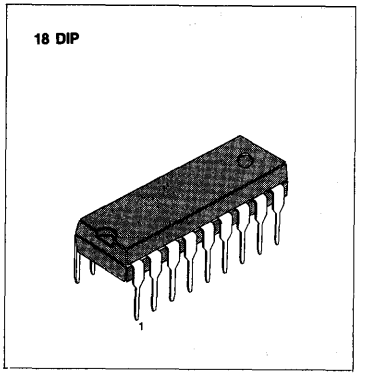
(for Switching Mode Operation by $\overline{\text{MODE SELECT}}$ Input) (OPERATION SELECT = V_{SS})



T_{AP}: 3.5sec

TONE/PULSE DIALER WITH REDIAL

The KS5820 is a DTMF/PULSE switchable dialer with a 32-digit redial memory. Through pin selection, switching from pulse to DTMF mode can be done using a slide switch. All necessary dual-tone frequencies are derived from a 3.579545MHz TV crystal, providing very high accuracy and stability. The required sinusoidal wave form for each individual tone is digitally synthesized on the chip. The wave form so generated has very low total harmonic distortion (7% Max). A voltage reference is generated on the chip which is stable over the operating voltage and temperature range and regulates the single levels of the dual tone to meet telephone industry specifications. CMOS technology is applied to this device, for very low power requirements high noise immunity, and easy interface to a variety of telephones requiring external components.



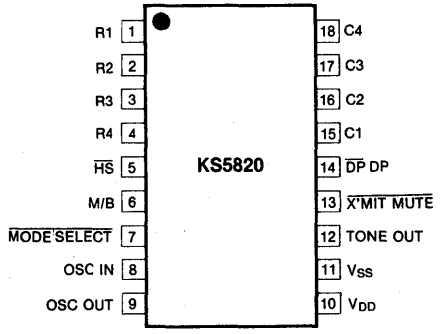
FEATURES

- **Tone/Pulse switchable (slide switch).**
- **32 digit capacity for redial**
- **Automatic mix redialing (last number dial) of PULSE→DTMF with multiple auto access pause**
- **PABX auto-pause for 3.5 sec.**
- **4 x 4 or (2 of 8) keyboard available**
- **Low power CMOS process (2.0 to 5.5V)**
- **Numbers dialed manually after redial are cascadable and stored as additional numbers for next redialing**
- **Uses inexpensive TV crystal (3.579545MHz)**
- **Make/Break ratio (33 1/3 ~ 66 2/3 or 40/60) pin selectable**
- **Touch key hooking (604ms)**
- **Low standby current**

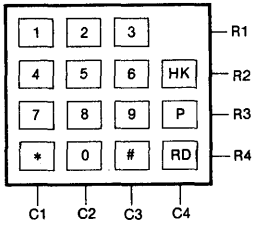
ORDERING INFORMATION

Device	Dial Pulse	PPS	Make/Break Ratio
KS58A20N	DP	10	V_{DD}: 33.3/66.6
			V_{SS}: 40/60
KS58B20N	DP	20	V_{DD}: 33.3/66.6
			V_{SS}: 40/60
KS58C20N	$\overline{DP}$	10	V_{DD}: 33.3/16.6
			V_{SS}: 40/60
KS58D20N	$\overline{DP}$	20	V_{DD}: 33.3/66.6
			V_{SS}: 40/60

PIN CONFIGURATION

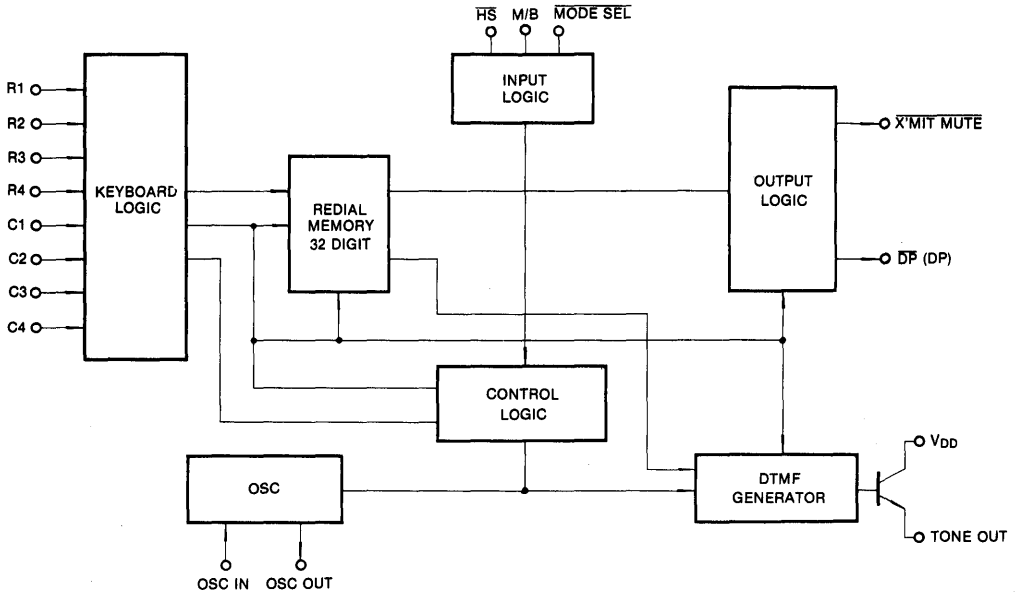


ARRANGEMENT OF KEYBOARD



HK : HOOKING (604ms)
P : PAUSE (3.5 second)
RD : REDIAL

BLOCK DIAGRAM



TONE DURATION & PAUSE IN REDIAL

Characteristic	Symbol	Typ	Unit
Tone Duration	T_D	110	mS
Minimum Pause	ITP	110	mS
Cycle Time	T_C	220	mS

TONE FREQUENCIES

Input	Specified	Actual	% Error
R1	697	699.1	+0.31
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.7	+0.57
C2	1336	1331.7	−0.32
C3	1477	1471.9	−0.35

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{DD}	6.0	V
Input Voltage	V_{IN}	$V_{SS}-0.3$, $V_{DD}+0.3$	V
Output Voltage	V_{OUT}	$V_{SS}-0.3$, $V_{DD}+0.3$	
Output Voltage	V_{OUT}	$\leqq V_{DD}$, ($\overline{DP}$, $\overline{X'MITMUTE}$)	V
Tone Output Current	I_{TONE}	50	mA
Power Dissipation	P_D	500	mW
Operating Temperature	T_{opr}	$-20 \sim +70$	°C
Storage Temperature	T_{stg}	$-40 \sim +125$	

ELECTRICAL CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 3.5V, fx'tal = 3.579545MHz, Ta = 25°C, unless otherwise noted)

Characteristic	Symbol	Test Conditions			Min	Typ	Max	Unit
Operating Voltage Range	V_{DDP}	Pulse Mode	All inputs connected to V_{DD} or V_{SS}		2.0		5.5	V
	V_{DDT}	Tone Mode			2.0		5.5	
Memory Retention Voltage	V_{DR}				1.0			
Operating Supply Current	I_{DDP}	$\overline{MODE} = V_{DD}$	One key selected $\overline{HS} = V_{SS}$. All outputs unloaded			0.3	0.5	mA
	I_{DDT}	$\overline{MODE} = V_{SS}$				0.5	1.0	
Standby Current	I_{SD1}	$\overline{HS} = V_{DD} = 1.5V$	No key selected. All outputs unloaded				0.05	μA
	I_{SD2}	$\overline{HS} = V_{SS}$					50	
Output Current	I_{OD1}	$\overline{DP}$	$V_{OL} = 0.4V$	$V_{DD} = 3.5V$	1.7	5.0		mA
	I_{OD2}	$\overline{X'MIT\ MUTE}$		$V_{DD} = 2.5V$	0.5	1.5		
Input Voltage	V_{IH}	R1-R4. C1-C3. $\overline{HS}$. M/B $\overline{MODE\ SELECT}$			$0.8V_{DD}$		V_{DD}	V
	V_{IL}				V_{SS}		$0.2V_{DD}$	
Input Current	I_{IN1}	$V_{DD} = 3.5V$ $V_{IN} = 0V$	R1-R4				116	μA
	I_{IN2}	$V_{DD} = 2.5V$ $V_{IN} = 0V$					50	
Valid Key Entry Time	T_{kd}				23		25.3	mS
Column and Row Scanning Frequency	F_{cr}					437		Hz
Auto Access Pause Time	T_{ap}					3.5		sec
Tone Output	V_{or}	ROW TONE ONLY	$V_{DD} = 2.5V$ $R_L = 5K$		−16.0		−12.0	dBV
			$V_{DD} = 3.5V$ $R_L = 5K$		−14.0		−11.0	
Ratio of Column to Row Tone	dB_{cr}	$V_{DD} = 3.5V$			1.0	2.0	3.0	dB
Distortion	%DIS	$V_{DD} = 3.5V$					7	%
Tone Output Delay Time	T_{psd}					1.5		mS

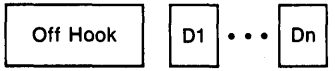
PIN DESCRIPTION

<table>
<tr><th>Pin</th><th>Name</th><th>Description</th></tr>
<tr><td>1-4
15-18</td><td>R1-R4
C1-C4</td><td>Keyboard (R1, R2, R3, R4, C1, C2, C3, C4)
These inputs can be interfaced to an XY matrix keyboard.
C1-C4 & R1-R4 are set to low at On Hook ($\overline{HS}$ = high). C1-C4 key inputs are set to low and R1-R4 are set to high at OFF HOOK ($\overline{HS}$ = low) which enables the key-Input operation. The oscillator starts running when a keypress is detected. Scanning signals are presented at both column and row inputs (TYP: 437Hz) until the input key is released. Key inputs are compatible with standard 2-of-8 form or single-contact keyboard. Debouncing is provided to avoid false entry (TYP: 25mS).</td></tr>
<tr><td>5</td><td>$\overline{HS}$</td><td>Hook Switch
This input detects the state of the hook switch contact. "Off Hook" corresponds to V_{SS} condition. "On Hook" corresponds to V_{DD} condition.</td></tr>
<tr><td>6</td><td>M/B</td><td>Make/Break Ratio
This input provides the selection of the Make/Break ratio (33.3: 66.6/40:60) when M/B is connected to V_{DD}/V_{SS}.</td></tr>
<tr><td>7</td><td>$\overline{\text{MODE SELECT}}$</td><td>Mode Select Input
Pulse/DTMF mode is selected as shown in the following table.
Initial Mode means the state after going Off Hook ($\overline{HS} \rightarrow$ "V_{SS}")
<table>
<tr><th>$\overline{\text{MODE SELECT}}$</th><th>INITIAL MODE</th><th>SWITCHING ENTRY MODE</th></tr>
<tr><td>V_{DD}</td><td>Pulse</td><td>$\overline{\text{MODE SELECT}}$ Input = V_{SS}</td></tr>
<tr><td>V_{SS}</td><td>Tone</td><td>N/A</td></tr>
</table></td></tr>
<tr><td>8-9</td><td>OSC IN
OSC OUT</td><td>Oscillator Input/Output
These pins are provided to connect an external 3.58MHz crystal. Oscillator starts (at Off Hook) and is sustained until pulse or DTMF signals are finished.</td></tr>
<tr><td>10-11</td><td>V_{DD}, V_{SS}</td><td>Power
These are the power supply inputs. The device is designed to be operated on 2.0V to 5.5V.</td></tr>
<tr><td>12</td><td>TONE OUT</td><td>DTMF Signal Output
When a valid keypress is detected in DTMF mode appropriate low and high group frequencies are generated which hybrid the Dual Tone Output.
Tone out is Off State in pulse mode.</td></tr>
<tr><td>13</td><td>$\overline{\text{X'MIT MUTE}}$</td><td>X'mit Mute Output
<table>
<tr><th>$\overline{HS}$</th><th>$\overline{\text{X'mit Mute Output}}$</th></tr>
<tr><td>V_{DD}</td><td>"ON"</td></tr>
<tr><td>V_{SS}</td><td>Normally "OFF"
"ON" during pulse and DTMF dialing</td></tr>
</table>
(N channel open drain)</td></tr>
<tr><td>14</td><td>$\overline{DP}$, DP</td><td>Dial Pulse Out
DP: The normal output will be "OFF" during break and "ON" during make at "OFF HOOK." The output will be "ON" at "ON HOOK,"
$\overline{DP}$: The normal output will be "ON" during break and "OFF" during make at "OFF HOOK." The output will be "OFF" at "ON HOOK."</td></tr>
</table>

KEYBOARD OPERATION

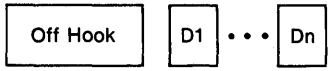
1. SINGLE MODE OPERATION

- **Pulse Mode Operation**



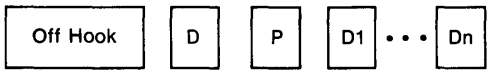
Pulse mode is defined by the initial mode after going Off Hook and latched at [D1] key entry. This is the condition under $\overline{\text{Mode Select}} = V_{DD}$.

- **Tone Mode Operation**



Tone mode is defined by the initial mode after going Off Hook and latched at [D1] key entry. This condition is under $\overline{\text{Mode Select}} = V_{SS}$.

- **Manual Dialing with Automatic Access Pause**

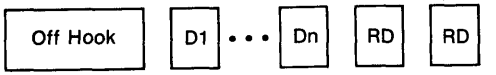


Multiple Pause key entries can be accepted and stored in the redial memory, each as a digit. Each [P] key provides 3.5 seconds pause time, but the [P] key entry as the first digit after going Off Hook is ignored. The [*] key can also be used as a pause key in the pulse mode. Pause (s) can be the cancelled with the [P] or [RD] key during pause time in redialing.
[D] = Any numeric key.

- **Redialing**

Up to 32 digits can be dialed with the [RD] key. The [RD] key is disabled while pulse or DTMF signals are transmitted. When more then 32 digits are stored, redial is also inhibited.
The [#] key can be used as the [RD] key in the pulse mode.

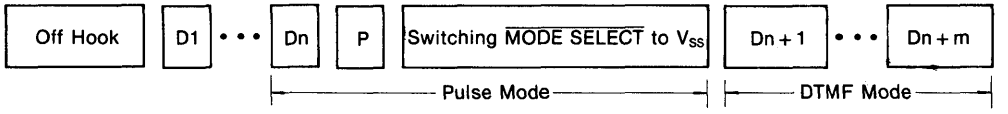
- **Inhibiting Redial**



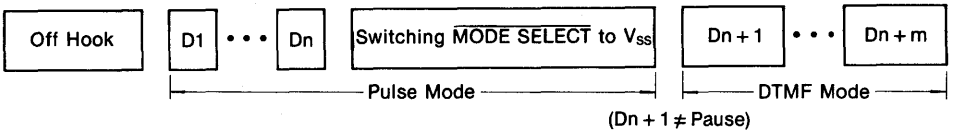
Redial can be inhibited by depressing the [RD] key twice after DTMF or pulse signals are transmitted.

2. PULSE/TONE SWITCHABLE OPERATION

• **Mode Switching by $\overline{\text{MODE SELECT}}$ Input**



The pulse mode is initially defined $\overline{\text{MODE SELECT}} = V_{DD}$. Mode switching to the DTMF mode can be accepted by $\overline{\text{MODE SELECT}} = V_{SS}$, the DTMF mode will be set up after the pulse mode is finished. In this mode, digits [Dn + 1] ... [Dn + m] are transmitted from Tone Out as DTMF signals by depressing the corresponding keys.
If no [P] key is contained serially before or after mode switching, the following condition is obtained.



If digit [Dn + 1] is depressed after the pulse mode is finished, the DTMF mode will be set up after the last pulse signal ([Dn]) is generated. In this mode, digits [Dn + 1] ... [Dn + m] are transmitted from Tone Out as DTMF signals by depressing the corresponding keys. If digit [Dn + 1] is depressed during dialing pulse signals, DTMF mode, in the Hold State, will be set after the last pulse signal [Dn] is finished. MODE OUT will flash to indicate this Hold State [Dn + 1] ... [Dn + m] is stored in the redial memory as DTMF data and not transmitted from Tone Out. When it is ready to transmit the DTMF data in redial memory, the [T], [RD] or [P] key is depressed to reset this Hold State and [Dn + 1] ... [Dn + m] data are serially transmitted.

Single Tone Operation in DTMF Mode (Test mode)

1. The M/B pin is used to trigger the chip into the test mode by applying a positive or negative pulse after "Off Hook." The test mode is sustained until On Hook. The single tone is shown in the following table which contrast with the normal mode.

Normal mode

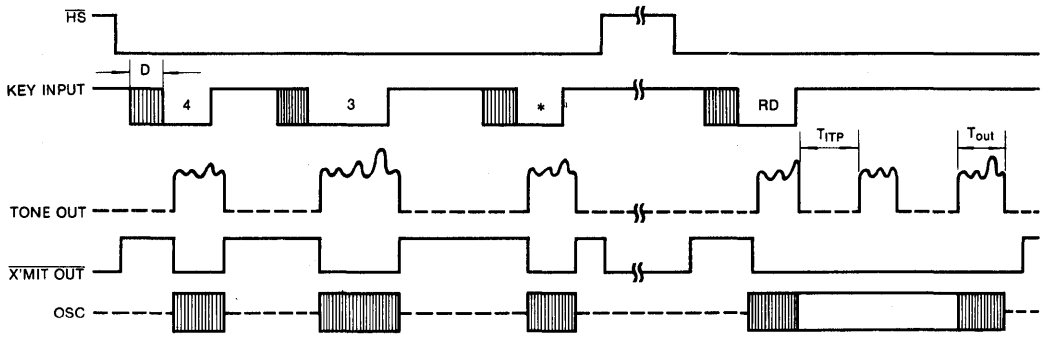
	C1	C2	C3
R1	1	2	3
R2	4	5	6
R3	7	8	9
R4	*	0	#

Single tone mode

	C1	C2	C3
R1	R1	C2	C3
R2	C1	C2	R2
R3	R3	C2	C3
R4	C1	R4	C3

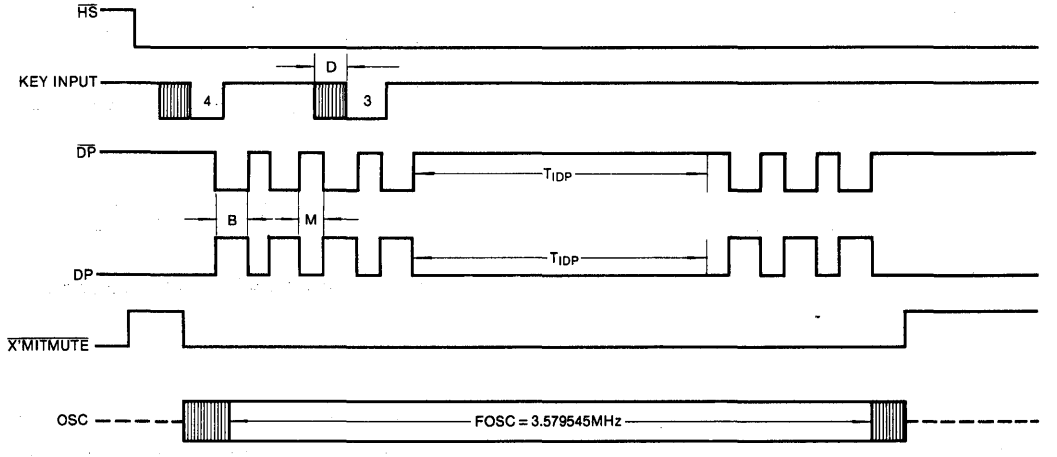
2. The single tone can be generated by simultaneously depressing two digit keys in the appropriate Row and Column. If tthe wo digit keys are not in the same Row or Column, the dual tone is disabled and no output is provided.

TONE MODE TIMING ($\overline{\text{MODE SELECT}} = V_{SS}$)



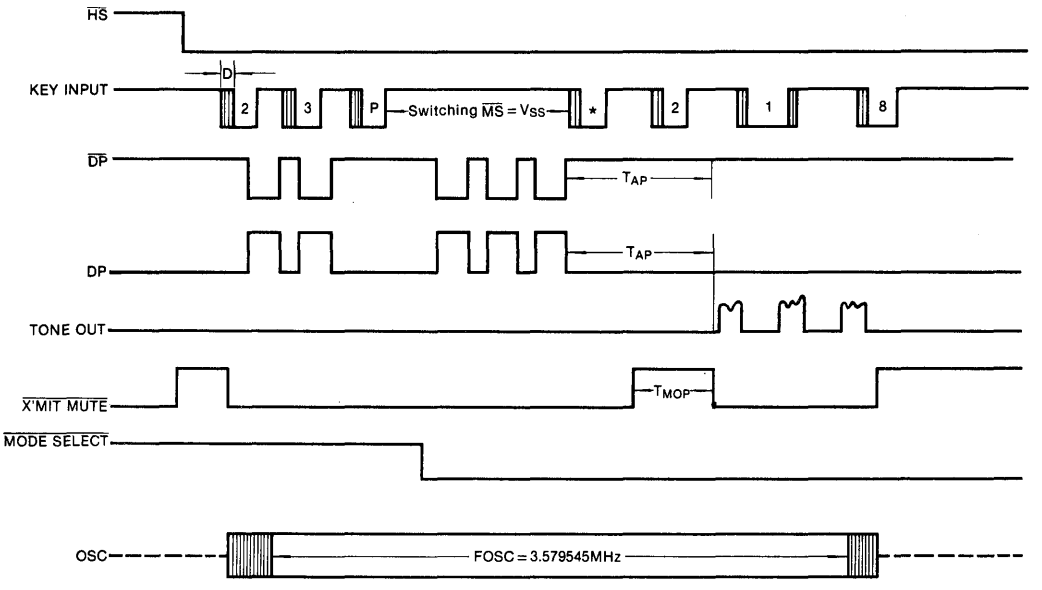
D: Debouncing Time: 25mS T_{out}: 110mS
T_{ITP}: 110mS

PULSE MODE TIMING ($\overline{\text{MODE SELECT}} = V_{DD}$)



D: Debouncing Time: 25mS
T_{IDP}: Inter Digit Pause: 879mS

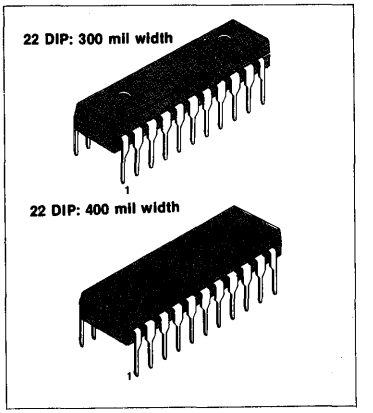
TIMING DIAGRAM (for Switching Mode Operation by $\overline{\text{MODE SELECT}}$ Input)



T_{AP}: Auto Pause Time 3.5sec

10 MEMORY TONE/ PULSE REPERTORY DIALER

The KS5822, a CMOS digital LSI, is a 10 number by 16 digit tone/pulse switchable dialer, with 32 digit redial memory. Through pin selection, switching from pulse to tone mode, 10 or 20pps and make/break ratio can be done.



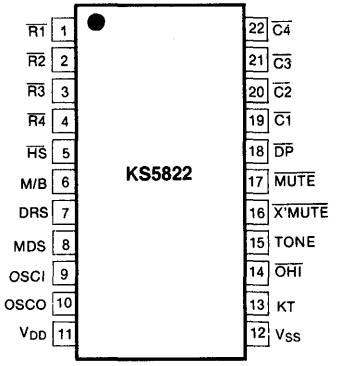
FEATURES

- 32 digit redial memory with buffer
- 10 No x 16 digit repertory memory
- Tone/Pulse switchable via slide switch with multiple auto access pause (3.5 sec)
- Uses inexpensive TV crystal (3.579545MHz)
- Make/Break ratio pin selectable (1/2, 2/3)
- Dialing pulse rate pin selectable 10pps/20pps
- Two key single tone operation
- Redial memory cascadable with normal dialing
- Fully debounced 4 x 4 keyboard
- Low voltage operating: 2.0 ~ 5.5V
- Low standby current
- Includes power on reset function
- Minimum tone duration: 110mS
- Minimum interdigit tone pause time: 110mS

ORDERING INFORMATION

Device	Package	Operating Temperature
KS5822N	300 mil Width	−20 ~ +70°C
KS5822E	400 mil Width	

PIN CONFIGURATION



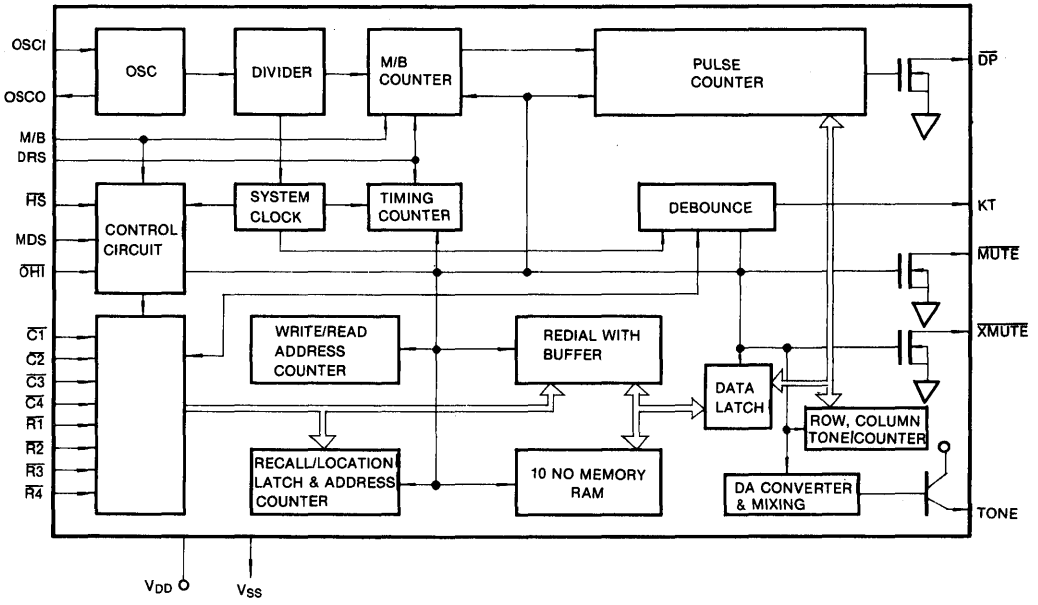
ARRANGEMENT OF KEYBOARD

1	2	3	ST	ST : Store
4	5	6	R/L	R/L : Recall/Location
7	8	9	P	P : Pause
*	0	#	RD	RD : Redial

PIN DESCRIPTION

Pin	Name	Description
1-4 19-22	$\overline{R1}$-$\overline{R4}$ $\overline{C1}$-$\overline{C4}$	Keyboard Input These inputs can be interfaced to an XY matrix keyboard.
5	$\overline{HS}$	Hook Switch Input. V_{DD} = On Hook, V_{SS} = Off Hook
6	M/B	Make/Break Ratio Select. V_{DD} = 1:2 (M/B), V_{SS} = 2:3 (M/B)
7	DRS	Dial Pulse Ratio Select V_{DD} = 20pps, V_{SS} = 10pps
8	MDS	Mode Select. V_{DD} = Pulse mode, V_{SS} = Tone mode
9	OSC IN	Oscillator Input/Output
10	OSC OUT	
11	V_{DD}	Power. This device is designed to operate on 2.0V to 5.5V
12	V_{SS}	
13	KT	Key In Tone Output. (In Pulse & Tone Mode) f_{KT} = 1.785KHz, t_{KT} = 36.6mS
14	$\overline{OHI}$	On Hook Store Inhibitive Input. V_{DD} = Store available, V_{SS} = Inhibitive store function
15	TONE	DTMF Signal Output
16	$\overline{XMUTE}$	$\overline{XMUTE}$ Output. This is a N-channel open drain output. Operating pulse and tone mode.
17	$\overline{MUTE}$	$\overline{MUTE}$ Output. Operating only pulse mode.
18	$\overline{DP}$	Dial Pulse Output. (N-channel open drain)

BLOCK DIAGRAM



TONE DURATION & PAUSE

Characteristic	Symbol	Typ	Unit
Tone Duration	T_D	110	mS
Minimum Pause	I_{TP}	110	mS

TONE FREQUENCIES

Input	Specified	Actual	% Error
R1	697	699.1	+0.31
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1,209	1,215.9	+0.57
C2	1,336	1,331.7	+0.32
C3	1,477	1,471.8	−0.35

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 ~ 6.0	V
Input Voltage	V_{IN}	−0.3 ~ V_{DD} + 0.3	V
Output Voltage	V_{OUT}	−0.3 ~ V_{DD} + 0.3	V
Operating Temperature	T_a	−20 ~ +70	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C
Power Dissipation	P_D	500	mW

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.5V, V_{SS} = 0V, f_{OSC} = 3.579545MHz, Ta = 25°C, unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}		2.0		5.5	V
Memory Retention Voltage	V_r		1.0			V
Operating Supply Current	I_{ODP}	Pulse Mode, all outputs unloaded			0.5	mA
	I_{ODT}	Tone Mode, all outputs unloaded			1.0	mA
Standby Current	I_{DD1}	$\overline{HS}$ = V_{DD} = 1.0V, all outputs unloaded		0.03	0.05	μA
	I_{DD2}	$\overline{HS}$ = V_{SS}, all outputs unloaded		30	50	μA
Output Sink Current ($\overline{DP}$, $\overline{XMUTE}$, $\overline{MUTE}$)	I_{OL1}	V_{OL} = 0.4V	1.7	5.0		mA
	I_{OL2}	V_{OL} = 0.4V, V_{DD} = 2.5V	0.5	1.5		mA
Key In Tone Current	I_{OHK}	V_{OH} = 0.4V	1.7	5.0		mA
	I_{OHL}	V_{OL} = 3.0V	1.8	5.2		mA
Input Voltage ($\overline{R1}$-$\overline{R4}$, $\overline{C1}$-$\overline{C4}$, $\overline{HS}$, MDS, M/B, DRS)	V_{IH}		0.8V_{DD}		V_{DD}	V
	V_{IL}		V_{SS}		0.2V_{DD}	V
Input Current (R1-R4, C1-C4)	I_{IH}	V_{IN} = V_{SS}			116	μA
	I_{IL}	V_{IN} = V_{SS}, V_{DD} = 2.5V			50	μA
Row Tone Level	V_{TH}	V_{DD} = 3.5V, R_L = 5KΩ	−14		−11	dBV
	V_{TL}	V_{DD} = 2.5V, R_L = 5KΩ	−16		−12	
Ratio of Column to Row Tone	dB_{cr}		1	2	3	dB
Distortion	THD				7	%
Valid Key Entry Time	T_{KD}			9.1	19.1	mS
Pause Time	t_{ap}			3.51		sec

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Pulse Interdigit Pause Time	t_{IDP1}	DRS = V_{SS}, 10pps		805.6		mS
	t_{IDP2}	DRS = V_{DD}, 20pps		402.8		
Tone Interdigit Pause Time	t_{IDT}			109.8		mS
Minimum Tone Duration	t_{TD}			109.8		mS
Minimum Key In Tone Duration	t_{KT}			36.6		mS
Key In Tone Frequency	f_{KT}			1.785		KHz
Make/Break Time	$t_{M/B}$	DRS = V_{SS}, M/B = V_{DD}, 10pps		34.33 68.66		mS
		DRS = V_{SS}, M/B = V_{SS}, 10pps		41.19 61.79		mS
Make/Break Time	$t_{M/B}$	DRS = V_{DD}, M/B = V_{DD}, 20pps		17.17 34.33		mS
		DRS = V_{DD}, M/B = V_{SS}, 20pps		20.60 30.90		mS

KEY DESCRIPTION

- **1, 2, 3, 4, 5, 6, 7, 8, 9, 0 KEYS**

  These are Tone/Pulse dialing signal keys in normal state but their entry right after store mode or recall mode provides store memory location.

- ***, # KEYS**

  These are served as a dialing signal during the tone mode. But during the pulse mode the * key modulates pause and the # key redials.

- **PAUSE KEY**

  The pause key is stored in the RAM as a digit and while this digit is processed no dialing can be operated. During the pause time (3.51 sec) no output is generated.

- **REDIAL KEY**

  The redial key is valid only when it is pressed as the 1st key after OFF-HOOK operation.

- **RECALL/LOCATION KEY**

  Location or recall number selection is enabled by detecting R/L key input.

- **STORE KEY**

  If the ST key is allowed when the dialer is set to the corresponding condition, pressing the ST key will change the dialer into the ST mode.
  The ST mode is released after the memory transfer operation is executed. This pin is a master control key. The dialing sequence will be interrupted when the key is activated.

OPERATION OF TONE/PULSE

• SYMBOL DEFINITION

T/p = Tone Mode t/P = Pulse Mode
Dp = Pulse Data: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0 Keys
Dt = Tone Data: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, *, #
Dm = Memory Location
R// = R/L Key for Recalling
r/L = R/L Key for Location
RD = Redial Key
P = Pause Key
ST = Store Key
Conv = Conversation Mode

• NORMAL DIALING IN PULSE MODE

Off Hook, t/P; Dp_1, Dp_2, ... Dpn; Conv; On Hook

• NORMAL DIALING IN TONE MODE

Off Hook, T/p; Dt_1, Dt_2, ... Dtn; Conv; On Hook

• NORMAL DIALING IN PULSE TO TONE MODE

Off Hook, t/P; Dp_1, Dp_2, ... Dpn; T/p; Dt_1, Dt_2, ... Dtn; Conv; On Hook

• REDIALING

Off Hook; RD; Conv; On Hook
Note: More than 33 digits in the redial memory inhibit the redial function and the RD input after Off Hook is ignored.

• STORING A NUMBER FOR PULSE MODE

1) $\overline{OHI}$ = Low
Off Hook, t/P; ST; Dp_1, Dp_2, ... Dpn; r/L; Dm; On Hook
(Return to Normal Mode)

2) $\overline{OHI}$ = High
On Hook, t/P; ST; Dp_1, Dp_2, ... Dpn; r/L; Dm;
(Return to Normal Mode)

• STORING A NUMBER FOR PULSE-TO-TONE MIXED DIALING

On (Off) Hook (By Condition), t/P; ST; Dp_1, Dp_2, ... Dpn; T/p; Dt_1, Dt_2, ... Dtn; r/L; Dm; On Hook
(Return to Normal Mode)

• STORING A NUMBER FOR TONE MODE

On (Off) Hook (By Condition), T/p; ST; Dt_1, Dt_2, ... Dtn; r/L; Dm; On Hook (Return to Normal Mode)
Note: The tone data is a one digit in tone mode and the device provides a 31 digit redial memory and a 15 digit storing memory in the tone mode.

• A NUMBER REPERTORY DIALING

Off Hook; R//; Dm; Conv; On Hook

• REPERTORY DIALING FOR CASCADED MEMORIES

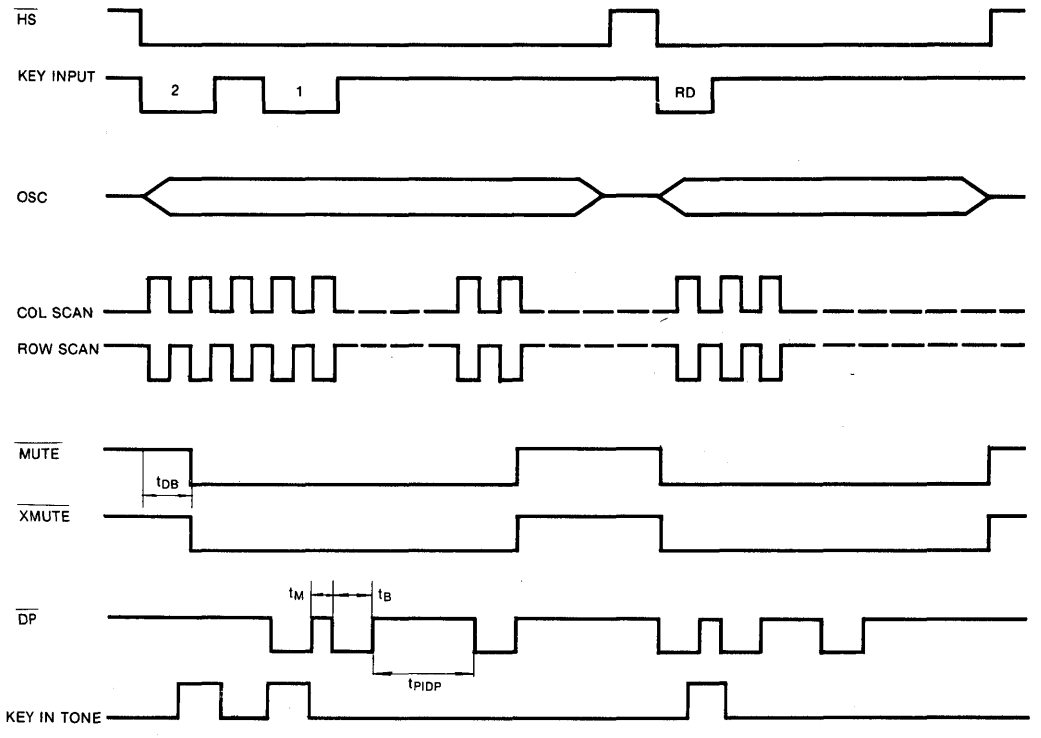
Off Hook; R//; Dm; ..... ; R//, Dm; Conv; On Hook
Note: If cascade number exceeds 32 digits, the next digit is ignored. The number cannot be redialed by being truncated.

TONE GENERATOR

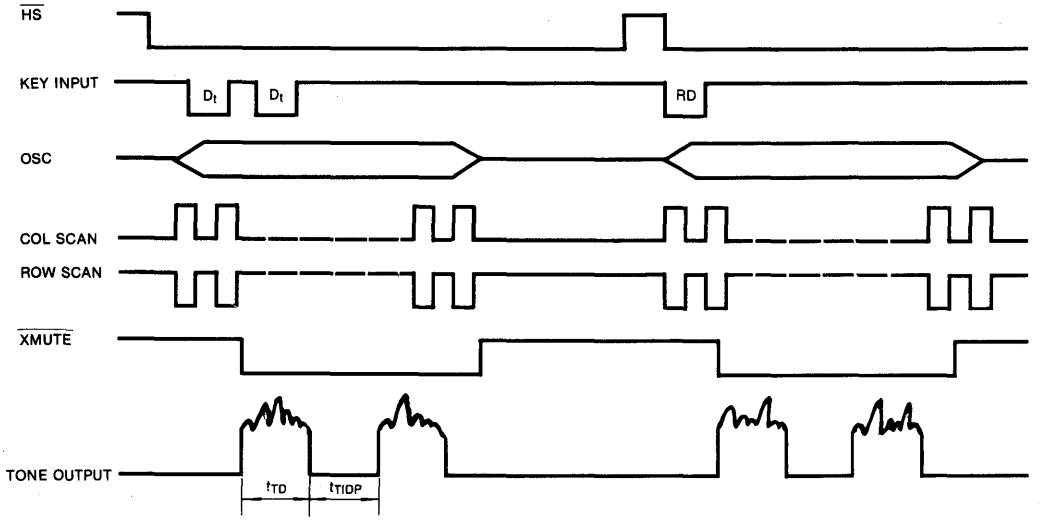
A single tone generated consists of 14 level and 28 segments. It's column tone output is 2 dB preemphasized than row tone output.

TIMING DIAGRAM

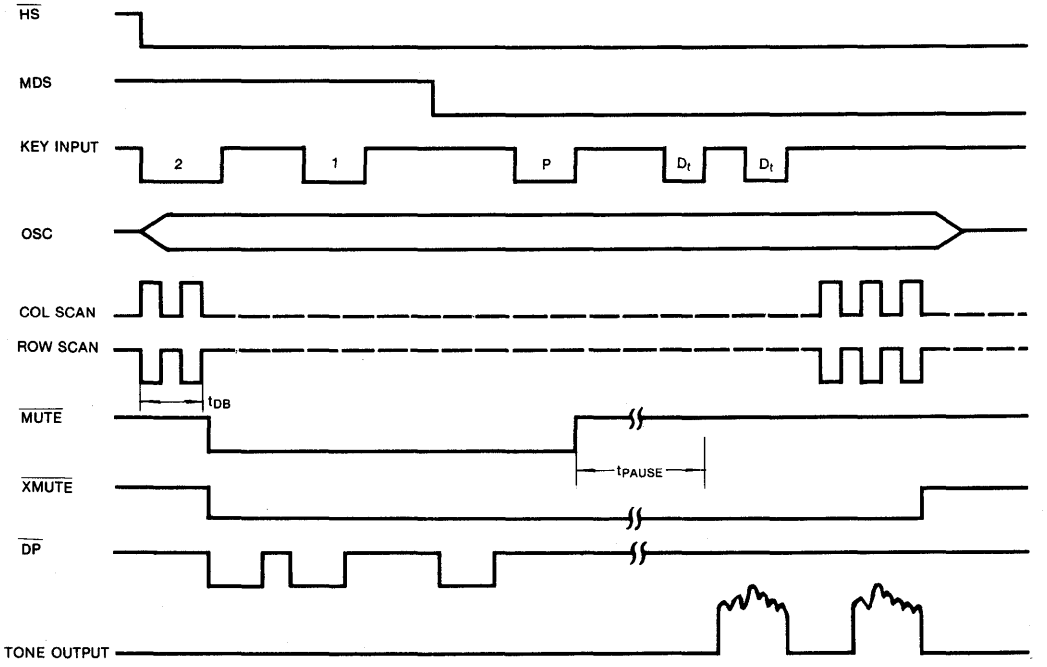
PULSE MODE



TONE MODE

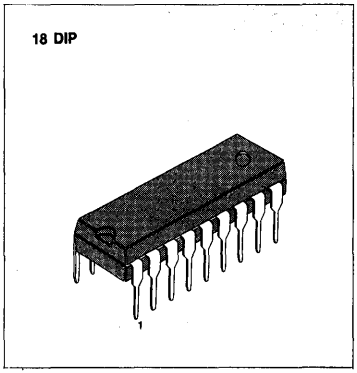


PULSE TO TONE DIALING



10 MEMORY TONE/ PULSE REPERTORY DIALER

The KS5823 series, a CMOS digital LSI, is a 10 number by 16 digit tone/pulse switchable dialer, with 32 digit redial memory. Through pin selection, switching from pulse to tone mode and make/break ratio can be done.



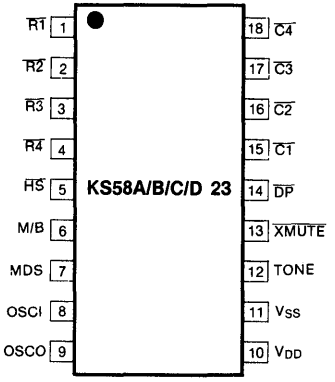
FEATURES

- **32 digit redial memory with buffer**
- **10 No x 16 digit repertory memory**
- **Tone/Pulse switchable via slide switch with multiple auto access pause (3.5 sec)**
- **Uses inexpensive TV crystal (3.579545MHz)**
- **Make/Break ratio pin selectable (1/2, 2/3)**
- **Two key single tone operation**
- **Redial memory cascadable with normal dialing**
- **Fully debounced 4 x 4 keyboard**
- **Low voltage operating: 2.0~5.5V**
- **Low standby current**
- **Includes power on reset function**
- **Minimum tone duration: 110mS**
- **Minimum interdigit tone pause time: 110mS**

ORDERING INFORMATION

Device	PPS	Storage Mode	Operating Temperature
KS58A23N	10pps	Off Hook Only	−20 ~ +70°C
KS58B23N	20pps	On/Off Hook	
KS58C23N	10pps	On/Off Hook	
KS58D23N	20pps	Off Hook Only	

PIN CONFIGURATION



ARRANGEMENT OF KEYBOARD

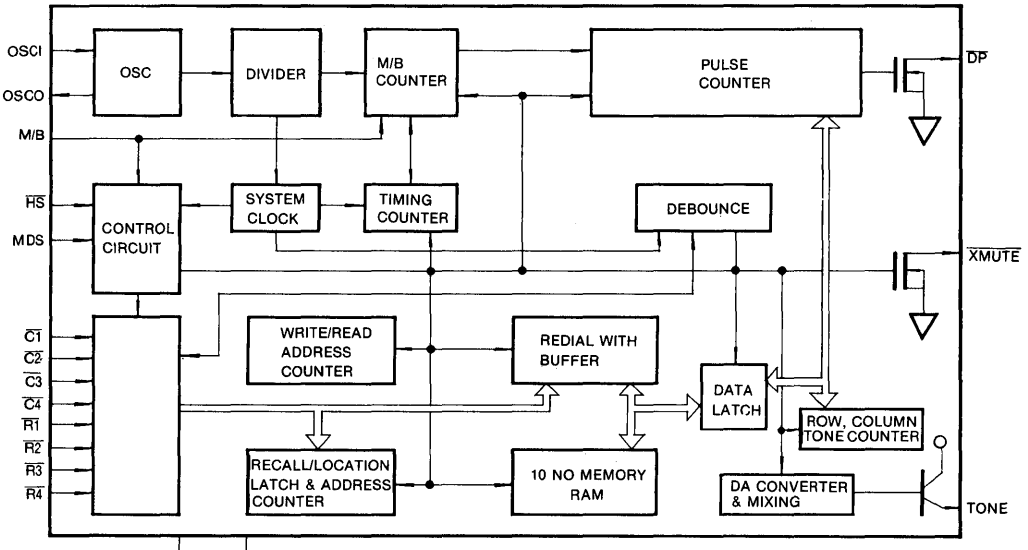
1	2	3	ST
4	5	6	R/L
7	8	9	P
*	0	#	RD

ST : Store
R/L : Recall/Location
P : Pause
RD : Redial

PIN DESCRIPTION

Pin	Name	Description
1-4	$\overline{R1}$-$\overline{R4}$	Keyboard Input These inputs can be interfaced to an XY matrix keyboard.
15-18	$\overline{C1}$-$\overline{C4}$	
5	$\overline{HS}$	Hook Switch Input. V_{DD} = On Hook, V_{SS} = Off Hook
6	M/B	Make/Break Ratio Select. V_{DD} = 1:2 (M/B), V_{SS} = 2:3 (M/B)
7	MDS	Mode Select. V_{DD} = Pulse mode, V_{SS} = Tone mode
8	OSC IN	Oscillator Input/Output
9	OSC OUT	
10	V_{DD}	Power. This device is designed to operate on 2.0V to 5.5V
11	V_{SS}	
12	TONE	DTMF Signal Output.
13	$\overline{XMUTE}$	XMUTE Output. This is a N-channel open drain output.
14	$\overline{DP}$	Dial Pulse Output. (N-chnanel open drain)

BLOCK DIAGRAM



Note: KS58A/C23 DRS = V_{SS}
KS58B/D23 DRS = V_{DD}
KS58A/D23 OHI = V_{SS}
KS58B/C23 OHI = V_{DD}

TONE DURATION & PAUSE

Characteristic	Symbol	Typ	Unit
Tone Duration	T_D	110	mS
Minimum Pause	I_{TP}	110	mS

TONE FREQUENCIES

Input	Specified	Actual	% Error
$\overline{R1}$	697	699.1	+0.31
$\overline{R2}$	770	766.2	−0.49
$\overline{R3}$	852	847.4	−0.54
$\overline{R4}$	941	948.0	+0.74
$\overline{C1}$	1,209	1,215.9	+0.57
$\overline{C2}$	1,336	1,331.7	+0.32
$\overline{C3}$	1,477	1,471.8	−0.35

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{DD}	$-0.3 \sim 6.0$	V
Input Voltage	V_{IN}	$-0.3 \sim V_{DD}+0.3$	V
Output Voltage	V_{OUT}	$-0.3 \sim V_{DD}+0.3$	V
Operating Temperature	T_a	$-20 \sim +70$	°C
Storage Temperature	T_{stg}	$-55 \sim +150$	°C
Power Dissipation	P_D	500	mW

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.5V, V_{SS} = 0V, f_{OSC} = 3.579545MHz, Ta = 25°C, unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}		2.0		5.5	V
Memory Retention Voltage	V_r		1.0			V
Operating Supply Current	I_{ODP}	Pulse Mode, all outputs unloaded			0.5	mA
	I_{ODT}	Tone Mode, all outputs unloaded			1.0	mA
Standby Current	I_{DD1}	$\overline{HS} = V_{DD} = 1.0V$, all outputs unloaded		0.03	0.05	μA
	I_{DD2}	$\overline{HS} = V_{SS}$, all outputs unloaded		30	50	μA
Output Sink Current ($\overline{DP}$, $\overline{XMUTE}$)	I_{OL1}	$V_{OL} = 0.4V$	1.7	5.0		mA
	I_{OL2}	$V_{OL} = 0.4V$, $V_{DD} = 2.5V$	0.5	1.5		mA
Input Voltage ($\overline{R1}$-$\overline{R4}$, $\overline{C1}$-$\overline{C4}$, $\overline{HS}$, MDS, M/B)	V_{IH}		$0.8V_{DD}$		V_{DD}	V
	V_{IL}		V_{SS}		$0.2V_{DD}$	V
Input Current (R1-R4, C1-C4)	I_{IH}	$V_{IN} = V_{SS}$			116	μA
	I_{IL}	$V_{IN} = V_{SS}$, $V_{DD} = 2.5V$			50	μA
Row Tone Level	V_{TH}	$V_{DD} = 3.5V$, $R_L = 5K\Omega$	−14		−11	dBV
	V_{TL}	$V_{DD} = 2.5V$, $R_L = 5K\Omega$	−16		−12	
Ratio of Column to Row Tone	dB_{cr}		1	2	3	dB
Distortion	THD				7	%
Valid Key Entry Time	T_{KD}			9.1	19.1	mS
Pause Time	t_{ap}			3.51		sec

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Pulse Interdigit Pause Time	t_{IDP1}	(KS58A/C23)		805.6		mS
	t_{IDP2}	(KS58B/D23)		402.8		
Tone Interdigit Pause Time	t_{IDT}			109.8		mS
Minimum Tone Duration	t_{TD}			109.8		mS
Make/Break Time	$t_{M/B}$	M/B = V_{DD}, KS58A/C23		34.33 68.66		mS
		M/B = V_{SS}, KS58A/C23		41.19 61.79		mS
Make/Break Time	$t_{M/B}$	M/B = V_{DD}, KS58B/D23		17.17 34.33		mS
		M/B = V_{SS}, KS58B/D23		20.60 30.90		mS

KEY DESCRIPTION

- **1, 2, 3, 4, 5, 6, 7, 8, 9, 0 KEYS**
  These are Tone/Pulse dialing signal keys in normal state but their entry right after the store mode or recall mode provides a store memory location.
- ***, # KEYS**

  These keys serve as a dialing signal during the tone mode. But during the pulse mode the * key modulates pause and the # key redials.
- **PAUSE KEY**

  The pause key is stored in the RAM as a digit and while this digit is processed no dialing can be operated. During the pause time (3.51 sec) no output is generated.
- **REDIAL KEY**
  The redial key is valid only when it is pressed as the 1st key after OFF-HOOK operation.
- **RECALL/LOCATION KEY**
  Location or recall number selection is enabled by detecting R/L key input.
- **STORE KEY**
  If the ST key is allowed when the dialer is set to the corresponding condition, pressing the ST key will change the dialer into the ST mode.
  The ST mode is released after the memory transfer operation is executed. This pin is a master control key. The dialing sequence will be interrupted when the key is activated.

OPERATION OF TONE/PULSE

- **SYMBOL DEFINITION**

T/p = Tone Mode t/P = Pulse Mode
Dp = Pulse Data: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0 Keys
Dt = Tone Data: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, *, #
Dm = Memory Location
R// = R/L Key for Recalling
r/L = R/L Key for Location
RD = Redial Key
P = Pause Key
ST = Store Key
Conv = Conversation Mode

- **NORMAL DIALING IN PULSE MODE**

  Off Hook, t/P; Dp_1, Dp_2, ... Dpn; Conv; On Hook

- **NORMAL DIALING IN TONE MODE**

  Off Hook, T/p; Dt_1, Dt_2, ... Dtn; Conv; On Hook

- **NORMAL DIALING IN PULSE TO TONE MODE**

  Off Hook, t/P; Dp_1, Dp_2, ... Dpn; T/p; Dt_1, Dt_2, ... Dtn; Conv; On Hook

- **REDIALING**

  Off Hook; RD; Conv; On Hook
  Note: More than 33 digits in the redial memory inhibits the redial function and RD input after Off Hook is ignored.

- **STORING A NUMBER FOR PULSE MODE**

  1) $\overline{OHI}$ = Low (KS58A/D23)
  Off Hook, t/P; ST; Dp_1, Dp_2, ... Dpn; r/L; Dm; On Hook
  (Return to Normal Mode)

  2) $\overline{OHI}$ = High (KS58B/C23)
  On Hook, t/P; ST; Dp_1, Dp_2, ... Dpn; r/L; Dm;
  (Return to Normal Mode)

- **STORING A NUMBER FOR PULSE-TO-TONE MIXED DIALING**

  On (Off) Hook (By Condition), t/P; ST; Dp_1, Dp_2, ... Dpn; T/p; Dt_1, Dt_2, ... Dtn; r/L; Dm; On Hook
  (Return to Normal Mode)

- **STORING A NUMBER FOR TONE MODE**

  On (Off) Hook (By Condition), T/p; ST; Dt_1, Dt_2, ... Dtn; r/L; Dm; On Hook (Return to Normal Mode)
  Note: The tone data is a one digit in tone mode and the device provides a 31 digit redial memory and a 15 digit storing memory in the tone mode.

- **A NUMBER REPERTORY DIALING**

  Off Hook; R/I; Dm; Conv; On Hook

- **REPERTORY DIALING FOR CASCADED MEMORIES**

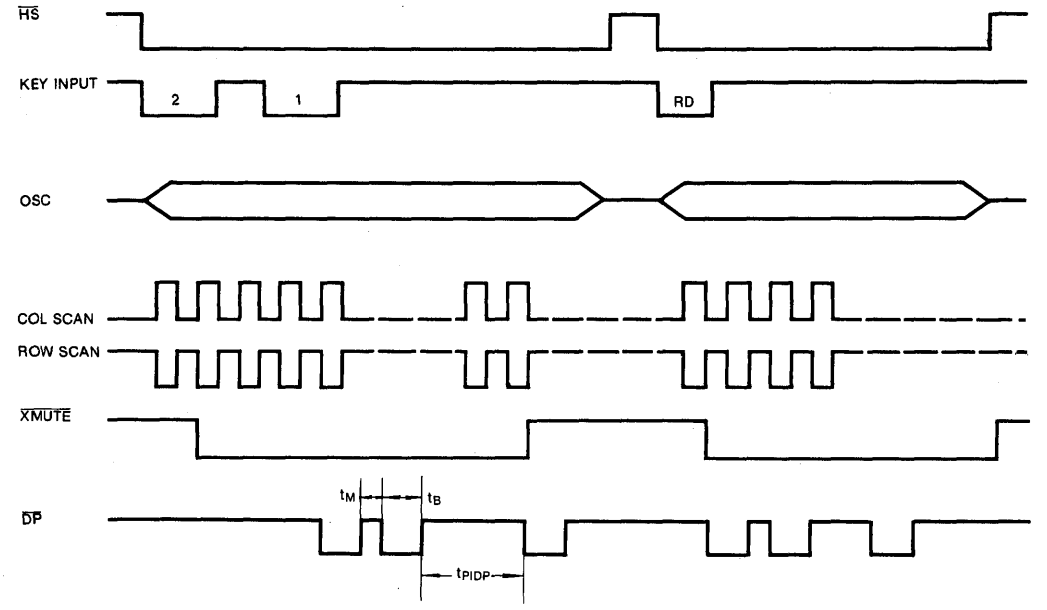
  Off Hook; R/I; Dm; ..... ; R/I, Dm; Conv; On Hook
  Note: If cascade number exceeds 32 digits, the next digit is ignored. The number cannot be redialed by being truncated.

TONE GENERATOR

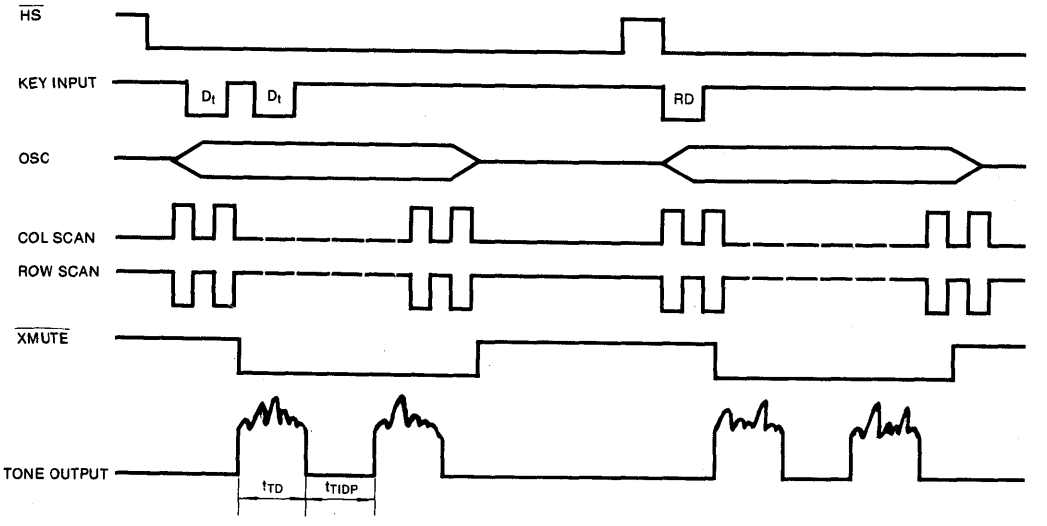
A single tone generated consists of 14 level and 28 segments. It's column tone output is 2 dB preemphasized than row tone output.

TIMING DIAGRAM

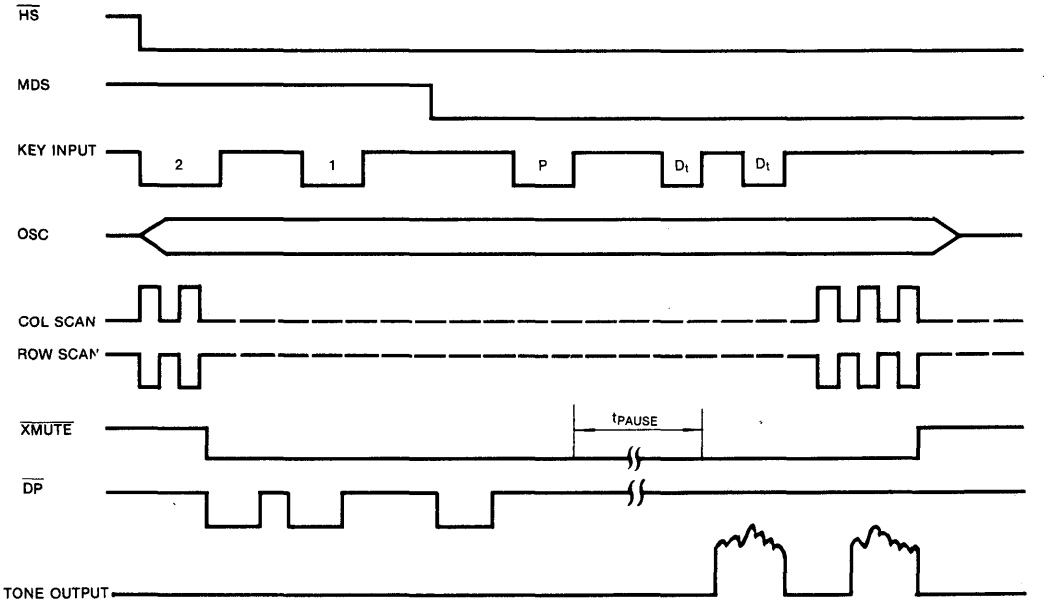
PULSE MODE



TONE MODE

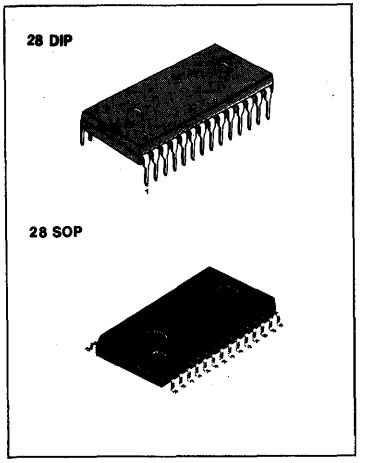


PULSE TO TONE DIALING



20 MEMORY TONE/PULSE REPERTORY DIALER

The KS58531 ~ KS58542 a CMOS digital LSI, is a 20 number by 16 digit repertory memory dialer with 32 digit redial memory. Through pin selection, switching from pulse to tone mode, on hook store or off hook store and make/break ratio can be done.

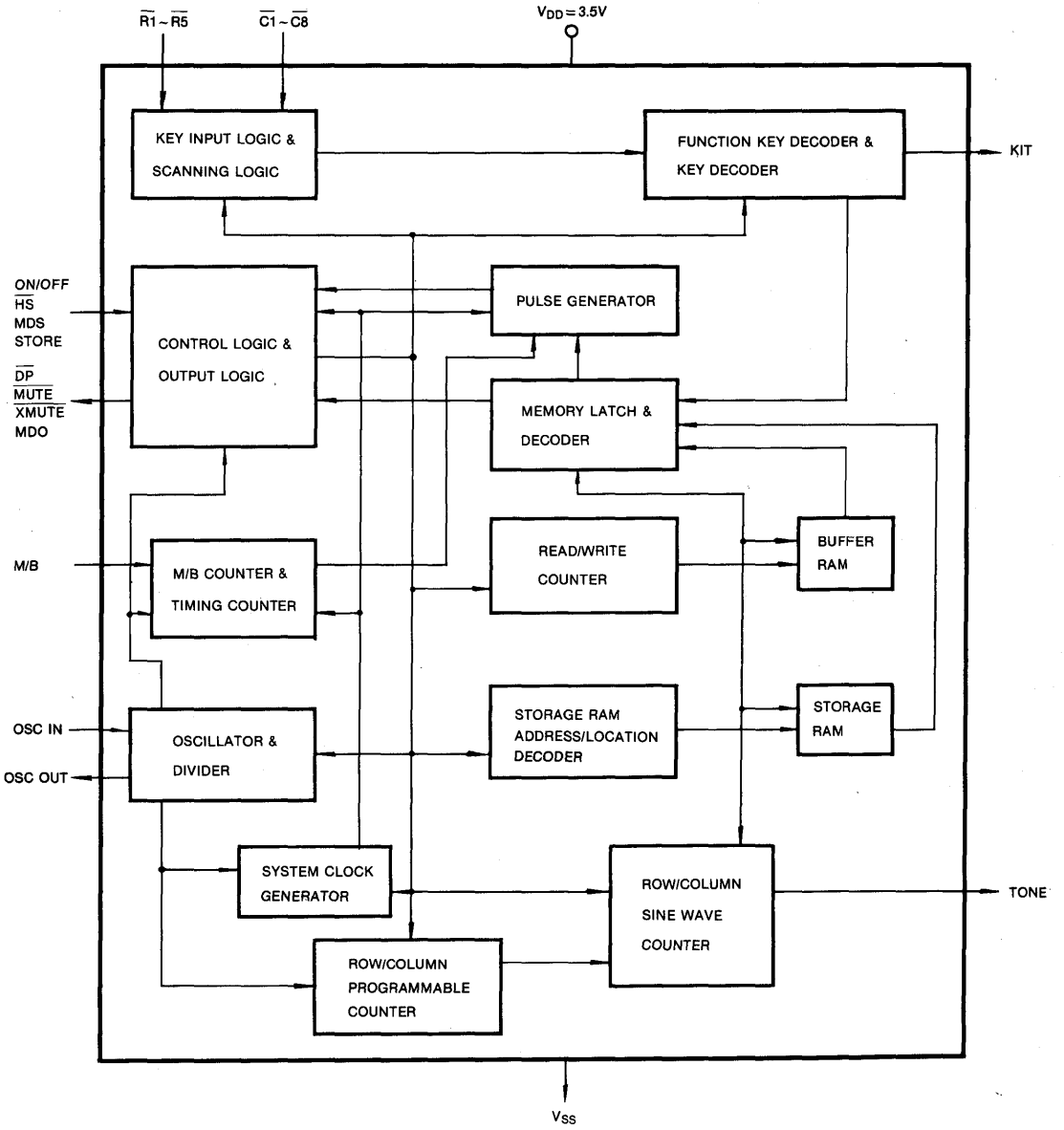


- **32 digit redial memory with buffer**
- **20 No x 16 digit repertory memory**
- **Pulse to DTMF dialing mode is selected by touch key or slide switch**
- **Uses inexpensive 3.579545MHz crystal or resonator.**
- **Manually dialing numbers after redialing are stored and cascaded in redial memory as additional numbers for next redialing**
- **Make/Break ratio (1/2, 2/3) pin selectable**
- **Two key single tone operation in test mode**
- **Repertory dialing is accessed by direct key or indirect key**
- **Flash function can be stored in memory**
- **Low operating current: 500μA (max) at V_{DD} = 3.5V pulse mode**
  1.0mA (max) at V_{DD} = 3.5V DTMF mode
- **Low memory retention voltage: 1.0V (min)**
- **Low memory retention current: 0.7μA (typ)**

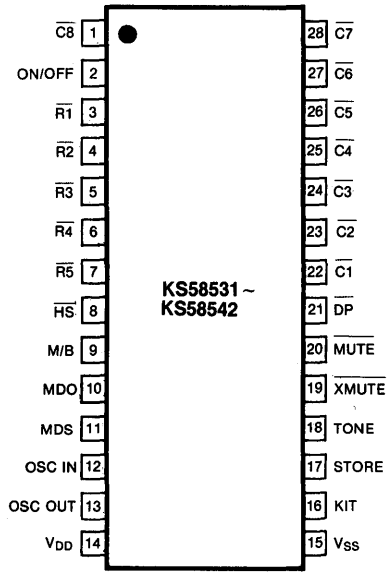
ORDERING INFORMATION

Device	Flash Time			Pause		PPS		Package	Operating Temperature
	0.1S	0.3S	0.6S	2S	3.6S	10	20		
KS58531N/D	O			O		O		28 DIP/SOP	−20 ~ +70°C
KS58532N/D	O				O	O			
KS58533N/D		O		O		O			
KS58534N/D		O			O	O			
KS58535N/D			O	O		O			
KS58536N/D			O		O	O			
KS58537N/D	O			O			O		
KS58538N/D	O				O		O		
KS58539N/D		O		O			O		
KS58540N/D		O			O		O		
KS58541N/D			O	O			O		
KS58542N/D			O		O		O		

BLOCK DIAGRAM



PIN CONFIGURATION



ARRANGEMENT OF KEYBOARD

t1	ST	t2	DTMF	M1	M6	M11	M16	— R1
1	2	3	F	M2	M7	M12	M17	— R2
4	5	6	REC	M3	M8	M13	M18	— R3
7	8	9	CL	M4	M9	M14	M19	— R4
*	0	#	RD/P	M5	M10	M15	M20	— R5
C1	C2	C3	C4	C5	C6	C7	C8	

PIN DESCRIPTION

Pin	Name	Description
3-7 22-28, 1	$\overline{R1}$-$\overline{R5}$ $\overline{C1}$-$\overline{C8}$	Keyboard Input Pins. As $\overline{HK}$ pin is high (ON HOOK), all these pins become TRI-STATE. When $\overline{HK}$ pin goes low and one key is pressed, the corresponding ROW and COLUMN will be low.
2	ON/OFF	ON HOOK/OFF HOOK Store Enable —ON HOOK store can be done if this pin is high. —OFF HOOK store can be done if this pin is low.
8	$\overline{HS}$	HOOK Switch Input V_{DD} = ON HOOK, V_{SS} = OFF HOOK
9	M/B	Make/Break Ratio Select V_{DD} = 1:2 (M/B), V_{SS} = 2:3 (M/B)
10	MDO	Tone/Pulse Mode Indicator This pin is high in pulse mode and goes low in tone mode.
11	MDS	Tone/Pulse Mode Select Pin V_{DD} = Pulse mode, V_{SS} = Tone mode
12, 13	OSC_{IN} OSC_{OUT}	Oscillator Input/Output
14, 15	V_{DD} V_{SS}	Power
16	KIT	Key In Tone Key in tone output for any valid key data in pulse mode and function key data in tone mode.
17	STORE	Store Switch Input V_{DD} = Store mode, V_{SS} = Normal mode
18	TONE	DTMF Tone Output
19	$\overline{XMUTE}$	$\overline{XMUTE}$ Output Pin This is a CMOS output and is switching on digit dialing and flash dialing in both mode.
20	$\overline{MUTE}$	$\overline{MUTE}$ Output Pin This is a CMOS output and is switching on digit dialing and flash dialing in pulse mode.
21	$\overline{DP}$	Dial pulse output (CMOS output)

TONE DURATION & PAUSE

Characteristic	Symbol	Typ	Unit
Tone Duration	T_D	98	mS
Minimum Pause	I_{TP}	104	mS

TONE FREQUENCIES

Input	Specified	Actual	% Error
$\overline{R2}$	697	699.1	+0.31
$\overline{R3}$	770	766.2	−0.49
$\overline{R4}$	852	847.4	−0.54
$\overline{R5}$	941	948.0	+0.74
$\overline{C1}$	1,209	1,215.9	+0.57
$\overline{C2}$	1,336	1,331.7	+0.32
$\overline{C3}$	1,477	1,471.8	−0.35

KEYBOARD DESCRIPTION

- 1, 2, 3, 4, 5, 6, 7, 8, 9, 0
  Dialing signal keys

- *, #
  Dialing signal keys at tone mode only

- M1, M2, ..., M20
  1) In normal dialing or repertory dialing mode, pressing MX (X = 1, ..., 20) key, the first two cascaded memories will cascade the corresponding repertory memory to redial buffer immediately. However, when cascaded memories exceed three, the exceeded cascaded memories should enter after all the digits in buffer has dialed out otherwise they will be ignored.
  2) In store mode, pressing MX (X = 1, ..., 20) key will cause the 16 digits of redial buffer storing to corresponding repertory memory.

- DTMF
  1) In pulse mode, pressing this key will cause the T code is written to redial buffer and it will remain auto-access pause time in redialing or repertory dialing. If this key is pressed several times, only the first key-in is effective.
  2) In redialing or repertory dialing, pressing this key will cause cancel of pause and auto-access pause time.

- F
  A flash code will store to redial buffer and storage RAM if this key is pressed. During the execution of flash code, $\overline{DP}$, $\overline{XMUTE}$ and $\overline{MUTE}$ will be forced to low for t_f (flash time) and then, pause for t_{fp} (flash pause time) before the next dialing digit.

- RD/P
  This key will be allowed as redial key if it is the first key-in after off hook. Otherwise, it will be allowed as a pause key.

- STORE
  This key is effective when the dialing sequence has completed and it is the first key-in after off hook. Pressing this key once will enter the store mode. The store mode will be released by pressing this key again or on-hook once.

- REC
  Repertory dialing can carry out indirectly by using this key. The indirect memory location is same as the direct memory location (Pressing REC 0 1 is equal to pressing M1)

- t1, t2
  Test 1 and Test 2 are used the testing. User is not recommended to use these keys.

- CL
  In store mode, pressing this key will cause the memory clear and the memory revision.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 ~ 6.0	V
Input Voltage	V_{IN}	−0.3 ~ V_{DD} + 0.3	V
Output Voltage	V_{OUT}	−0.3 ~ V_{DD} + 0.3	V
Operating Temperature	T_a	−20 ~ +70	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C
Power Dissipation	P_D	500	mW

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.5V, V_{SS} = 0V, f_{OSC} = 3.579545MHz, Ta = 25°C, unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}		2.0		5.5	V
Memory Retention Voltage	V_R		1.0			V
Memory Retention Current	I_R			0.7		μA
Operating Supply Current	I_{ODP}	Pulse Mode, all outputs unloaded			0.5	mA
	I_{ODT}	Tone Mode, all outputs unloaded			1.0	mA
Standby Current	I_{DD1}	$\overline{HS}$ = V_{DD} = 1.0V, all outputs unloaded		0.03	0.05	μA
	I_{DD2}	$\overline{HS}$ = V_{SS}, all outputs unloaded		30	50	μA
Output Sink Current ($\overline{DP}$, $\overline{XMUTE}$, $\overline{MUTE}$)	I_{OL}	V_{OL} = 0.4V	1.7	5.0		mA
	I_{OH}	V_{OH} = 3.0V	1.8	5.2		mA
Key In Tone Current	I_{OLK}	V_{OL} = 0.4V	1.7	5.0		mA
Input Voltage	V_{IH}		0.8V_{DD}		V_{DD}	V
	V_{IL}		V_{SS}		0.2V_{DD}	V
Input Current (R1-R5, C1-C8)	I_{IH}	V_{IN} = V_{SS}			116	μA
	I_{IL}	V_{IN} = V_{SS}, V_{DD} = 2.5V			50	μA
Row Tone Level	V_{TH}	V_{DD} = 3.5V, R_L = 5KΩ	−14		−11	dBV
	V_{TL}	V_{DD} = 2.5V, R_L = 5KΩ	−16		−12	
Ratio of Column to Row Tone	dB_{cr}		1	2	3	dB
Distortion	THD				7	%
Valid Key Entry Time	T_{KD}		33.5			mS
Key Tone Duration	T_{KT}			33.1		mS
Key Tone Frequency	f_{KT}			1.2		KHz

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Pause Time	t_P	2 sec	MDS = H		2.04		sec
			MDS = L		2.12		
		3.6 sec	MDS = H		3.64		
			MDS = L		3.72		
Auto-Access Pause Time	t_{AP}				1.009		sec
Pulse Interdigit Pause Time	t_{PIDP}	20pps	M/B = H		419.0		mS
			M/B = L		422.4		
		10pps	M/B = H		838.1		
			M/B = L		844.9		
Tone Interdigit Pause Time	t_{TIDP}				103.5		mS
Tone Minimum Duration	t_{TD}				97.64		mS
Flash Time	t_F			600.3		612.9	mS
Flash Pause Time	t_{FP}			1.002		1.046	sec
Make/Break Time	$t_{M/B}$	10pps	M/B = H		33.5 67.0		mS
			M/B = L		40.2 60.3		
		20pps	M/B = H		16.7 33.5		
			M/B = L		20.1 30.2		

KEYBOARD AND SWITCHES OPERATION MANUAL

- SYMBOL DEFINITION
  Dp = Pulse Data: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, F, Pause
  Dt = Tone Data: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, *, #, F, Pause
  Mx = REPERTORY MEMORY: M1, M2, ..., M20
  LOC = 01, 02, ..., 20
  ZiZiZi = Conversation Mode
  OFF = OFF HOOK
  ON = ON HOOK
  ⎍ = Input level from low to high
  ⎏ = Input level from high to low
  Dg = Storing data

- NORMAL DIALING IN PULSE MODE
  OFF; Dp, ..., Dp; ZiZiZi; ON;

- NORMAL DIALING IN TONE MODE
  OFF; Dt, ..., Dt; ZiZiZi; ON;

- NORMAL DIALING FROM PULSE TO TONE VIA DTMF KEY
  OFF; Dp, ..., Dp, DTMF, Dt, ..., Dt; ZiZiZi; ON;

- NORMAL DIALING FROM PULSE TO TONE VIA MDS PIN
  OFF; Dp, ..., Dp, MDS ⎏, Dt, ..., Dt; ZiZiZi; ON;

- REDIAL
  OFF; RD/P; ZiZiZi; ON;

  Note: 1) In normal dialing mode, the dialing digit is unlimited. However, if the dialing digits exceed 32 digit, the redialing operation will be inhibited.
  2) All key input will be ignored during the redialing and repertory dialing but pressing the DTMF key during the time of pause and auto-access pause operation, the pause and auto-access pause time are canceled and next data will send out.

- REPERTORY DIAL FOR ONE MEMORY
  OFF; Mx (x = 1, 2, ..., 20); ZiZiZi; ON; or
  OFF; REC, LOCx (x = 01, 02, ..., 20); ZiZiZi; ON;

- REPERTORY DIAL FOR CASCADED MEMORIES
  1) Cascaded memories are two memories.
  OFF; Mi, Mj (i, j = 1, ..., 20); ZiZiZi; ON; or
  OFF; REC, LOCi, REC, LOCj (i, j = 01, ..., 20); ZiZiZi; ON;
  2) Cascaded memories are exceed two memories.
  OFF; Mi, Mj; All the digits have dialed out; Mk;
  All the digits have dialed out; Ml (i, j, k, l = 1, ..., 20); ZiZiZi; ON; or
  OFF; REC, LOCi, REC, LOCj; All the digits have dialed
  out; REC, LOCk, All the digits have dialed out; REC, LOCl (i, j, k, l = 01, ..., 20); ZiZiZi; ON;

- STORING REPERTORY MEMORIES VIA STORE KEY
  OFF: ST, Dg, ..., Dg; Mi (i = 1, ..., 20) or REC LOCi (i = 01, ..., 20); Dg, ..., Dg; Mj (j = 1, ..., 20) or REC LOCj (j = 01, ..., 20) store mode will be released by pressing store key again or ON HOOK once.

- STORING REPERTORY MEMORIES VIA STORE PIN
  OFF: Store Pin ⎍⎺; Dg, ..., Dg; Mi (i = 1, ..., 20) or REC LOCi (i = 01, ..., 20); Dg, ..., Dg; Mj (j = 1, ..., 20) or REC LOCj (j = 01, ..., 20); store pin ⎺⎍; (Return to normal mode)

- MEMORY CLEAR FUNCTION VIA CLEAR KEY
  OFF: ST; CL; Mx (x = 1, ..., 20) or REC LOCx (x = 01, ..., 20); ON;

- MEMORY DATA CHANGE VIA CLEAR KEY
  OFF: ST; Dg, ..., Dg, CL, Dg, ..., Dg; Mx (x = 1, ..., 20) or REC LOCx (x = 01, ..., 20)
  (The Digits after CL are memorized at Mx or LOCx)

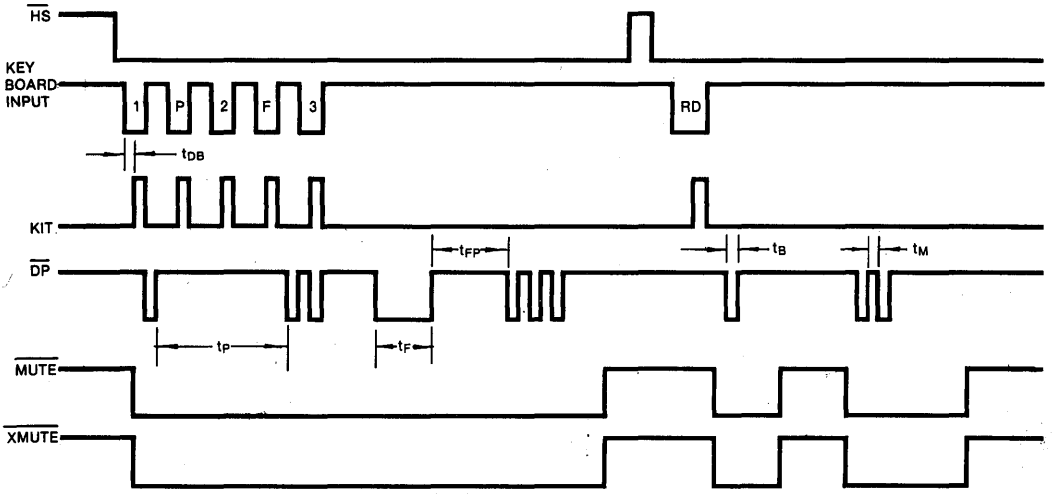
- F KEY FUNCTION
  1) Repertory Dialing
     —In store mode, pressing F, 1, 2, 3, 4, 5, 6 and then pressing Mx or REC LOCx; In normal mode pressing Mx or REC LOCx, the output data is F, 1, 2, 3, 4, 5, 6.
     —In store mode, pressing 1, 2, 3, F, 4, 5, 6 and then pressing Mx or REC LOCx; In normal mode pressing Mx or REC LOCx, the output data is 1, 2, 3, 4, 5, 6. In store mode, the F key is effective only when it is the first key.
  2) Normal Dialing and Redialing
     —The input digits are 1, 2, 3, F, 4, 5, 6 in normal dialing, and then ON HOOK; OFF HOOK; RD/P; the output data is 1, 2, 3.
     —The input digits are 1, 2, 3, 4, 5, 6 in normal dialing and then ON HOOK; OFF HOOK; pressing F, 7, 8, 9; ON HOOK; OFF HOOK; RD/P; the output data is 1, 2, 3, 4, 5, 6.
     —In other word, the flash data and the following digits will be discarded.

TONE GENERATION

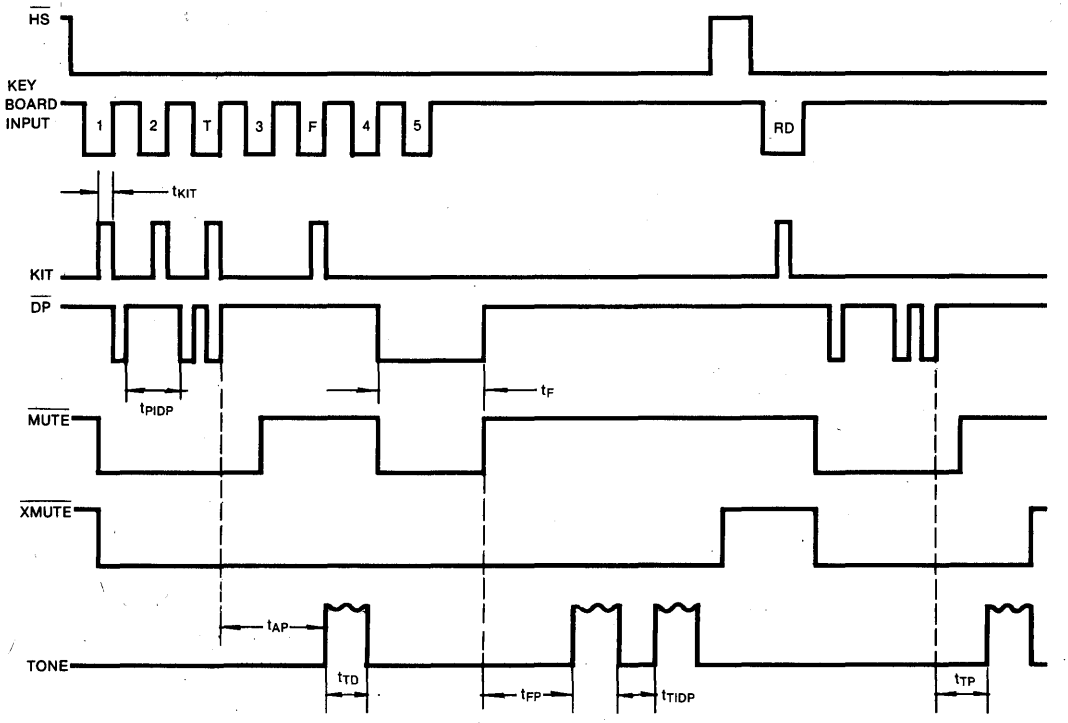
This device is well designed with 14-level, 28 segment. The COLOMN TONE is pre-emphasized 2dB than the ROW TONE. In order to single tone generation, push the same COLUMN or ROW keys more than 2 keys at same time.

TIMING DIAGRAM

1) PULSE MODE

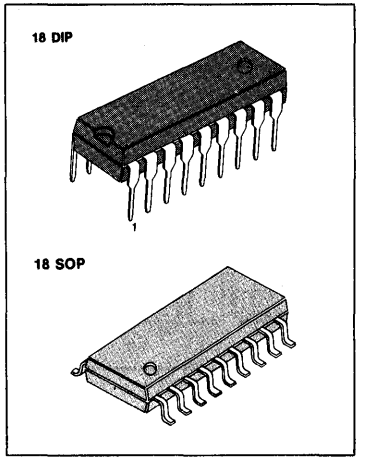


2) PULSE ⟶ TONE MODE



15CH/10CH SELECTOR FOR CORDLESSPHONE

The KS8800/KS8801 is designed to select 15/10 channels for cordless-phone of which frequency band is 46/49 MHz.
The device has reference frequency generator, programmable divider for transmit and receive section and phase detector.



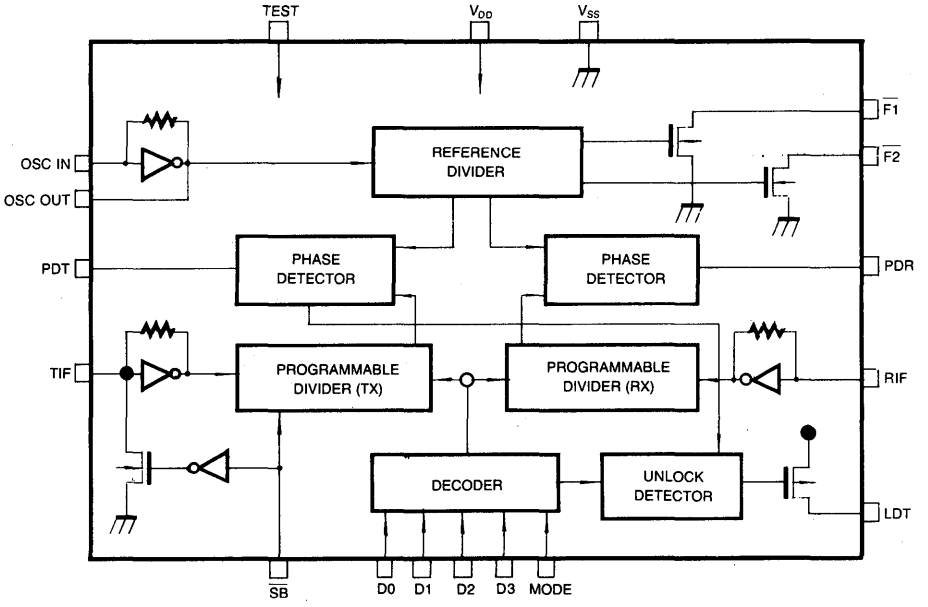
FEATURES

- **15 channels selectable (both transmit/receive): KS8800**
- **10 channels selectable (both transmit/receive): KS8801**
- **Include oscillation circuit with external X-TAL (10.24MHz)**
- **5KHz/4.4KHz output for guard tone**
- **Standby function for saving power**

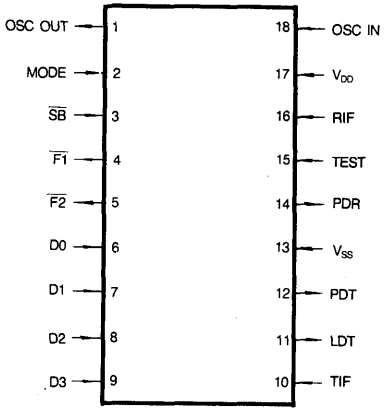
ORDERING INFORMATION

Device	Package	Operating Temperature
KS8800N	18 DIP	−30~75°C
KS8801N	18 DIP	
KS8800D	18 SOP	
KS8801D	18 SOP	

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Name	I/O	Description	Remarks
1	OSC OUT	Out	– This output generates reference frequency when it is connected to pin 18 with external OSC of which frequency is 10.24MHz	
2	Mode	In	– Base/remote unit selection pin "High": Base unit "Low" : Remote unit	
3	$\overline{SB}$	In	– Stand-by pin – This input controls the T_X PLL for reducing the power dissipation "High": Normal operation "Low" : Stand-by	
4	$\overline{F1}$	Out	– 5kHz output – N-channel open drain, normally connect to V_{SS}	
5	$\overline{F2}$	Out	– 4.4kHz output – N-channel open drain, normally connect to V_{SS}	
6 7 8 9	D0 D1 D2 D3	In	– Channel selection pins – The combinations of these inputs select one channel among the 15/10 channels	See Table 1 Table 2

PIN DESCRIPTION (Continued)

Pin No.	Name	I/O	Description	Remarks
10	TIF	In	– Input of programmable divider for T_X – AC coupling with V_{CO} – In case of large signal, it needs DC-coupling – Min.input voltage is $0.15V_{rms}$	
11	LDT	Out	– Unlocked signal out pin (See output characteristics)	
12	PDT	Out	– Phase detector output for T_X – PDT detects the phase error from T_X PLL and its output is connected to external low pass filter	
13	V_{SS}	Power	– This is negative supply of the IC – It usually grounded	
14	PDR	Out	– Phase detector output for R_X – PDR detects the phase error from R_X PLL and its output is connected to external low pass filter	
15	Test	In	– Input terminal of LSI for testing – Normally grounded	
16	RIF	In	– Input of programmable divider for R_X. – AC coupling with V_{CO} – In case of large signal (standard CMOS logic), it needs DC coupling – Min. input voltage is $0.15V_{rms}$	
17	V_{DD}	Power	– This pin is positive supply of the IC – Its reference is V_{SS}, and normally +3.0 ~ +5.5V more positive than V_{SS}	
18	OSC IN	In	– X-TAL OSC connection pin – This input generates the reference frequency when it is connected to pin 1 with external OSC	

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristics	Symbol	Value	Unit	Remark
Max. Power Supply Voltage	V_{DD} max	−0.5 ~ 6.0	V	
Max. Input Voltage	V_I max	−0.3 ~ V_{DD} + 0.5	V	All Inputs
Max. Output Current	I out	0 ~ 3.0	mA	$\overline{F1}$, $\overline{F2}$, LDT
Power Dissipation	P_d max	350	mW	Ta ≦ 75°C
Operating Temperature Range	T_{opr}	−30 ~ +75	°C	
Storage Temperature Range	T_{stg}	−40 ~ +125	°C	

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ELECTRICAL CHARACTERISTICS (Ta = 25°C)

Description	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}		3		5.5	V
Input Voltage	$V_{IH}1$	D0 ~ D3, $\overline{SB}$	$0.7V_{DD}$		V_{DD}	V
	$V_{IL}1$	D0 ~ D3, $\overline{SB}$	0		$0.3V_{DD}$	V
	$V_{IH}2$	Mode	$0.9V_{DD}$		V_{DD}	V
	$V_{IL}2$	Mode	0		$0.1V_{DD}$	V
Input Frequency	$F_{IN}1$	$V_{TIF} = 0.15V_{rms}$	10		27	MHz
	$F_{IN}2$	$V_{RIF} = 0.15V_{rms}$	30		42	MHz
	$F_{IN}3$	$OSC_{in} = 0.3V_{rms}$	5	10.24	11	MHz
Input Amplitude	$V_{IN}1$	F_{TIF} = 27 HMz	0.15		$0.3V_{DD}$	V_{rms}
	$V_{IN}1$	F_{RIF} = 42 MHz	0.15		$0.3V_{DD}$	V_{rms}
	$V_{IN}3$	OSC_{in} = 11 MHz	0.3		$0.3V_{DD}$	V_{rms}
Input Current	$I_{IH}1$	$OSC_{in} = V_{DD}$			20	uA
	$I_{IL}1$	$OSC_{in} = V_{SS}$			20	uA
	$I_{IH}2$	TIF, RIF: V_{DD}			40	uA
	$I_{IL}2$	TIF, RIF: V_{SS}			40	uA
	$I_{IH}3$	$\overline{SB}$, Mode, D0 ~ D3: V_{DD}			10	uA
	$I_{IL}3$	$\overline{SB}$, Mode, D0 ~ D3: V_{SS}			10	uA

ELECTRICAL CHARACTERISTICS (Continued)

Description	Symbol	Condition	Min.	Typ.	Max.	Unit
Output Voltage	$V_{OH}1$	PDT, PDR; Io = 0.5mA	V_{DD}-1.0			V
	$V_{OL}1$	PDT, PDR; Io = 0.5mA			0.4	V
Output OFF Leakage Current	$I_{LKG}1$	PDT, PDR; Vo = V_{DD}/V_{SS}		0.01	1.0	uA
Output Voltage	$V_{OH}2$	LDT; Io = 1mA	V_{DD}-1.0			V
Output OFF Leakage Current	$I_{LKG}2$	LDT; Vo = V_{SS}			5.0	uA
Output Voltage	$V_{OL}2$	$\overline{F1}$, $\overline{F2}$; Io = 1mA			0.4	V
Output OFF Leakage Current	$I_{LKG}3$	$\overline{F1}$, $\overline{F2}$; Vo = V_{DD}			5.0	uA
Stand-By Current	$I_{STD}1$	V_{DD} = 3V (Note 2)			3.0	mA
	$I_{STD}2$	V_{DD} = 4.5V (Note 2)			5.0	mA
	$I_{STD}3$	V_{DD} = 5.5V (Note 2)			10	mA
Operating Current KS8800/KS8801	$I_{DD}1$	V_{DD} = 3V (Note 1)			5.0/4.0	mA
	$I_{DD}2$	V_{DD} = 4.5V (Note 1)			10.0/7.0	mA
	$I_{DD}3$	V_{DD} = 5.5V (Note 1)			15.0/13.0	mA

* Note 1) OSC_{in} : 10.24 MHz X-tal Connection
TIF : 27 MHz 150 mV_{rms}
RIF : 42 MHz 150 mV_{rms}
Mode : V_{DD}, $\overline{SB}$ = V_{DD}, Others are Opened

* Note 2) OSC_{in} : 10.24 MHz X-tal Connection
TIF : 27 MHz 150 mV_{rms}
RIF : 42 MHz 150 mV_{rms}
Mode : V_{DD}, $\overline{SB}$ = V_{SS}, Others are Opened

Capacitor more than 2000 pF should be connected between V_{DD} & V_{SS}

BASE (MODE = 1)

Input				CH	R_x (Fref = 5KHz)			T_x (Fref = 2.5KHz)		
D0	D1	D2	D3		FR_X (MHz)	F_{VCO} (MHz)	N	FT_X (MHz)	F_{vco} (MHz)	N
0	0	0	1	1	49.695	39.000	7800	46.510	23.255	9302
0	0	1	0	2	49.710	39.015	7803	46.530	23.265	9306
0	0	1	1	3	49.725	39.030	7806	46.550	23.275	9310
0	1	0	0	4	49.740	39.045	7809	46.570	23.285	9314
0	1	0	1	5	49.755	39.060	7812	46.590	23.295	9318
0	1	1	0	6	49.670	38.975	7795	46.610	23.305	9322
0	1	1	1	7	49.845	39.150	7830	46.630	23.315	9326
1	0	0	0	8	49.860	39.165	7833	46.670	23.335	9334
1	0	0	1	9	49.770	39.075	7815	46.710	23.355	9342
1	0	1	0	10	49.875	39.180	7836	46.730	23.365	9346
1	0	1	1	11	49.830	39.135	7827	46.770	23.385	9354
1	1	0	0	12	49.890	39.195	7839	46.830	23.415	9366
1	1	0	1	13	49.930	39.235	7847	46.870	23.435	9374
1	1	1	0	14	49.990	39.295	7859	46.930	23.465	9386
1	1	1	1	15	49.970	39.275	7855	46.970	23.485	9394
0	0	0	0	15	49.970	39.275	7855	46.970	23.485	9394

REMOTE (MODE = 0)

Input				CH	R_x (Fref = 5KHz)			T_x (Fref = 2.5KHz)		
D0	D1	D2	D3		FR_X (MHz)	F_{VCO} (MHz)	N	FT_X (MHz)	F_{vco} (MHz)	N
0	0	0	1	1	46.510	35.815	7163	49.695	24.8475	9939
0	0	1	0	2	46.530	35.835	7167	49.710	24.8550	9942
0	0	1	1	3	46.550	35.855	7171	49.725	24.8625	9945
0	1	0	0	4	46.570	35.875	7175	49.740	24.8700	9948
0	1	0	1	5	46.590	35.895	7179	49.755	24.8775	9951
0	1	1	0	6	46.610	35.915	7183	49.670	24.8350	9934
0	1	1	1	7	46.630	35.935	7187	49.845	24.9225	9969
1	0	0	0	8	46.670	35.975	7195	49.860	24.9300	9972
1	0	0	1	9	46.710	36.015	7203	49.770	24.8850	9954
1	0	1	0	10	46.730	36.035	7207	49.875	24.9375	9975
1	0	1	1	11	46.770	36.075	7215	49.830	24.9150	9966
1	1	0	0	12	46.830	36.135	7227	49.890	24.9450	9978
1	1	0	1	13	46.870	36.175	7235	49.930	24.9650	9986
1	1	1	0	14	46.930	36.235	7247	49.990	24.9950	9998
1	1	1	1	15	46.970	36.275	7255	49.970	24.9850	9994
0	0	0	0	15	46.970	36.275	7255	49.970	24.9850	9994

Table 1. Channel & frequency table to base/remote input data for KS8800 (15 channels)

BASE (MODE = 1)

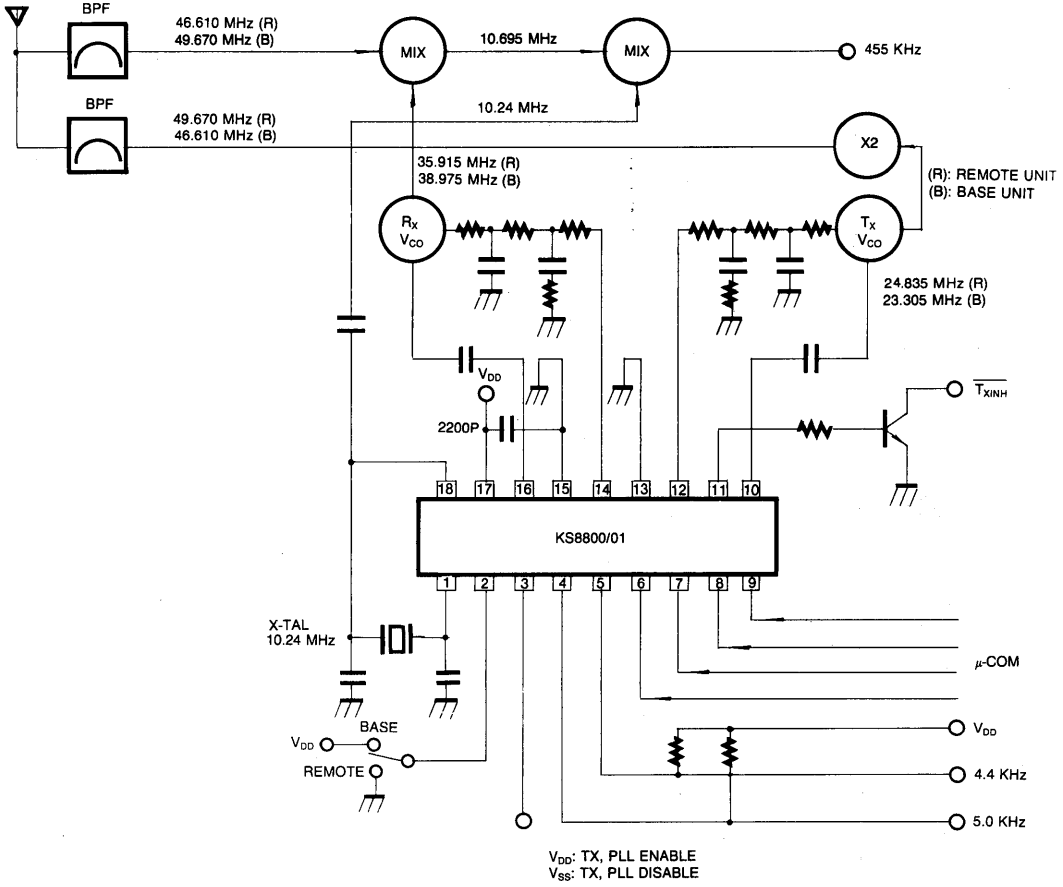
Input				CH	R_x (Fref = 5KHz)			T_x (Fref = 2.5KHz)		
D0	D1	D2	D3		FR_X (MHz)	F_{VCO} (MHz)	N	FT_X (MHz)	F_{veo} (MHz)	N
1	0	0	0	1	49.670	38.975	7795	46.610	23.305	9322
0	1	0	0	2	49.845	39.150	7830	46.630	23.315	9326
1	1	0	0	3	49.860	39.165	7833	46.670	23.335	9334
0	0	1	0	4	49.770	39.075	7815	46.710	23.355	9342
1	0	1	0	5	49.875	39.180	7836	46.730	23.365	9346
0	1	1	0	6	49.830	39.135	7827	46.770	23.385	9354
1	1	1	0	7	49.890	39.195	7839	46.830	23.415	9366
0	0	0	1	8	49.930	39.235	7847	46.870	23.435	9374
1	0	0	1	9	49.990	39.295	7859	46.930	23.465	9386
0	1	0	1	10	49.970	39.275	7855	46.970	23.485	9394
1	1	0	1	10	49.970	39.275	7855	46.970	23.485	9394
0	0	1	1	10	49.970	39.275	7855	46.970	23.485	9394
1	0	1	1	10	49.970	39.275	7855	46.970	23.485	9394
0	1	1	1	10	49.970	39.275	7855	46.970	23.485	9394
1	1	1	1	10	49.970	39.275	7855	46.970	23.485	9394
0	0	0	0	10	49.970	39.275	7855	46.970	23.485	9394

REMOTE (MODE = 0)

Input				CH	R_x (Fref = 5KHz)			T_x (Fref = 2.5KHz)		
D0	D1	D2	D3		FR_X (MHz)	F_{VCO} (MHz)	N	FT_X (MHz)	F_{vco} (MHz)	N
1	0	0	0	1	46.610	35.915	7183	49.670	24.8350	9934
0	1	0	0	2	46.635	35.935	7187	49.845	24.9225	9969
1	1	0	0	3	46.670	35.975	7195	49.860	24.9330	9972
0	0	1	0	4	46.710	36.015	7203	49.770	24.8850	9954
1	0	1	0	5	46.735	36.035	7207	49.875	24.9375	9975
0	1	1	0	6	46.770	36.075	7215	49.830	24.9150	9966
1	1	1	0	7	46.830	36.135	7227	49.890	24.9450	9978
0	0	0	1	8	46.870	36.175	7235	49.930	24.9650	9986
1	0	0	1	9	46.930	36.235	7247	49.990	24.9950	9998
0	1	0	1	10	46.970	36.275	7255	49.970	24.9850	9994
1	1	0	1	10	46.970	36.275	7255	49.970	24.9850	9994
0	0	1	1	10	46.970	36.275	7255	49.970	24.9850	9994
1	0	1	1	10	46.970	36.275	7255	49.970	24.9850	9994
0	1	1	1	10	46.970	36.275	7255	49.970	24.9850	9994
1	1	1	1	10	46.970	36.275	7255	49.970	24.9850	9994
0	0	0	0	10	46.970	36.275	7255	49.970	24.9850	9994

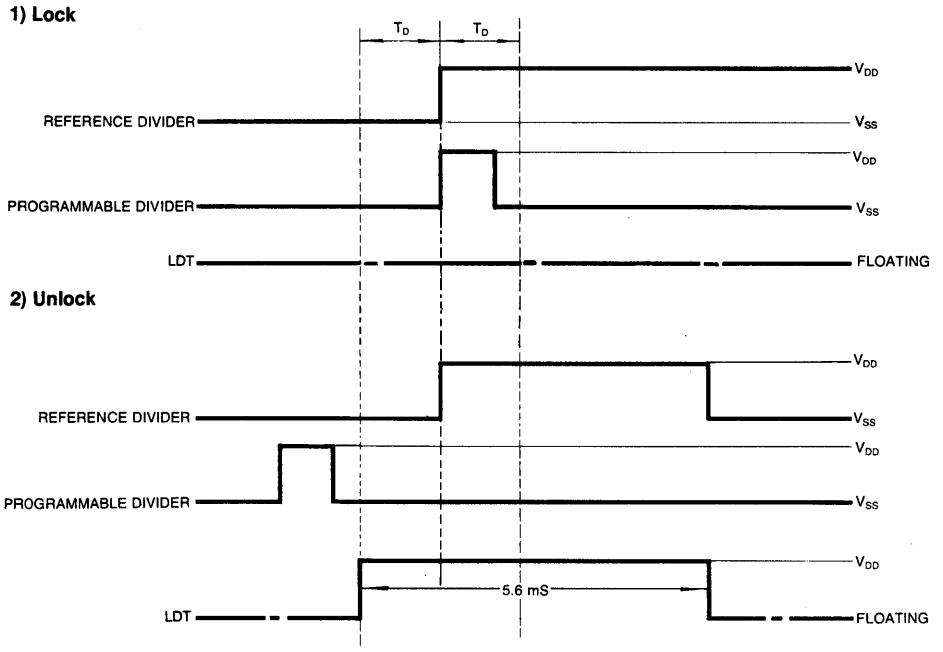
Table 2. Channel & frequency table to base/remote input data for KS8801 (10 channels)

TYPICAL APPLICATION



LDT OUTPUT CHARACTERISTICS

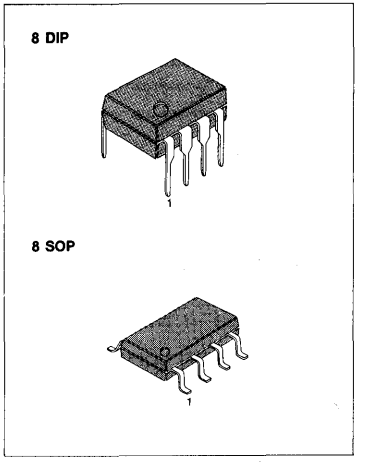
Phase Difference $T_D = 6.25\mu S$



Note) When the phase difference of programmable devider & reference divider exceeds T_D than LDT output is high.

TONE DECODER

The LM567C is a monolithic phase locked loop system designed to provide a saturated transistor switch to GND, when an input signal is present within the passband. External components are used to independently set center frequency bandwidth and output delay.



FEATURES

- **Wide frequency range (0.01Hz — 500kHz).**
- **Bandwidth adjustable from 0 to 14%**
- **Logic compatible output with 100mA current sinking capability.**
- **Inherent immunity to false signals.**
- **High rejection of out-of-band signals and noise.**
- **Frequency range adjustable over 20:1 range by an external resistor.**

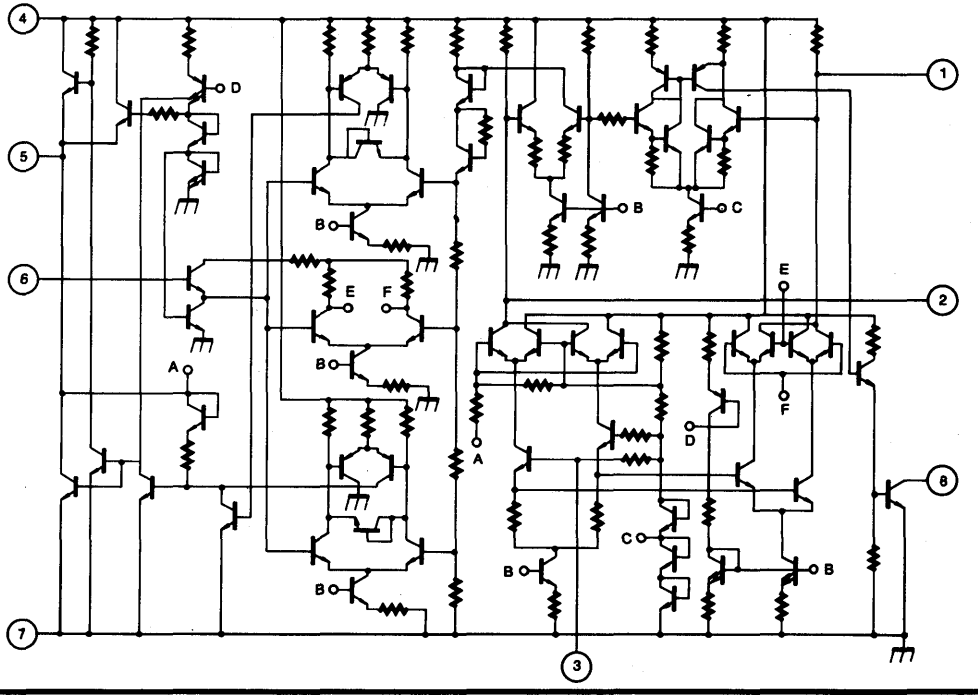
APPLICATIONS

- Touch Tone Decoder
- Wireless Intercom.
- Communications paging decoders
- Frequency monitoring and control.
- Ultrasonic controls (remote TV etc.)
- Carrier current remote controls.
- Precision oscillator.

ORDERING INFORMATION

Device	Package	Operating Temperature
LM567CN	8 DIP	0 ~ + 70°C
LM567CD	8 SOP	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{CC}	10	V
Input Voltage	V_{IN}	−10 ~ V_{CC} +0.5	V
Output Voltage	V_O	15	V
Power Dissipation	Pd	300	mW
Operating Temperature	Topr	0 ~ +70	°C
Storage Temperature	Tstg	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, T_a = 25°C unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage Range	V_{CC}		4.75	5.0	9.0	V
Supply Current Quiescent	I_{CC}-1	R_L=20K		7	10	mA
Supply Current Activated	I_{CC}-2	R_L=20K		12	15	mA
Quiescent Power Dissipation	P_{QD}	R_L=20K		35		mW
Highest Center Frequency	H_{FO}	R_L=20K	100	500		KHz
Center Frequency Stability	F_{SE}	0°C to 70°C		±60		ppm/°C
Center Frequency Shift With Supply Voltage	F_{CS}			0.7	2	%/V
Largest Detection Bandwidth	B.W		10	14	18	% of fo
Largest Detection B.W Skew	B.Ws			2	3	% of fo
Largest Detection Bandwidth Variation With Supply Voltage	B.Wv			±2	±5	%/V
Largest Detection Bandwidth Variation With Temperature	B.Wt			±0.1		%/°C
Input Resistance	R_{IN}			20		Kohm
Smallest Detectable Input Voltage	V_{IN}-1	I_L=100mA, fi=fo		20	25	mVrms
Largest No Output Input Voltage	V_{IN}-2		10	15		mVrms
Greatest Simultaneous Outband Signal To Inband Signal Ratio	S1/Sd	R_L = 20k V_{IN} = 300mV_{RMS} fi=fo=100KHz		+6		dB
Minimum Input Signal to Wideband Noise Ratio	S2/Sd	fi_1 =140KHz fi_2 =60KHz		−6		dB
Fastest On-Off Cycling Rate	F_{OUT}	R_L=20K		fo/20		
Output Leakage Current	I_{CO}	V_{IN}=25mV_{RMS}		0.01	25	μA
Output Saturaton Voltage	V_{SAT}-1	I_L=30mA, V_{IN}=25mVrms		0.2	0.4	V
	V_{SAT}-2	I_L=100mA, V_{IN}=25mVrms		0.6	1.0	V
Output Fall Time	T_F	R_L=50		30		nS
Output Rise Time	T_R	R_L=50		150		nS

CIRCUIT DESCRIPTION

The LM567C monolithic tone decoder consists of a phase detector, low pass filter, and current controlled oscillator which comprise the basic phase-locked loop, plus an additional low pass filter and quadrature detector enabling detection on in-band signals. The device has a normally high open collector output capable of sinking 100 mA.

The input signal is applied to Pin 3 (20 kΩ nominal input resistance). Free running frequency is controlled by an RC network at Pins 5 and 6 and can typically reach 500 kHz. A capacitor on Pin 1 serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 2; bandwidth and skew are also dependant upon the circuitry here. Bandwidth is adjustable from 0% to 14% of the center frequency. Pin 4 is $+V_{CC}$ (4.75 to 9V nominal, 10V maximum); Pin 7 is ground; and Pin 8 is a open collector output, pulling low when an in-band signal triggers the device.

BLOCK DIAGRAM

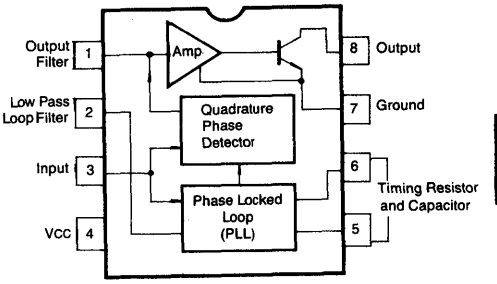


Fig. 1

DEFINITION OF LM567C PARAMETERS

CENTER FREQUENCY f_O

f_O is the free-running frequency of the C_L controlled oscillator with no input signal. It is determined by resistor R_1 between pins 5 and 6, and capacitor C_1 from pin 6 to ground f_O can be approximated by

$$f_O \approx \frac{1}{R_1 C_1}$$

where R_1 is in ohms and C_1 is in farads.

LARGEST DETECTION BANDWIDTH

The largest detection bandwidth is the largest frequency range within which an input signal above the threshold voltage will cause a logical zero state at the output. The maximum detection bandwidth corresponds to the lock range of the PLL.

DETECTION BANDWIDTH (BW)

The detection bandwidth is the frequency range centered about f_O, within which an input signal larger than the threshold voltage (typically 20mVrms) will cause a logic zero state at the output. The detection bandwidth corresponds to the capture range of the PLL and is determined by the low-pass bandwidth filter. The bandwidth of the filter, as a percent of f_O, can be determined by the approximation

$$BW = 1070 \sqrt{\frac{V_i}{f_O C_2}}$$

where V_i is the input signal in volts, rms, and C_2 is the capacitance at pin 2 in μF.

DETECTION BAND SKEW

The detection band skew is a measure of how accurately the largest detection band is centered about the center frequency, f_O. It is defined as $(f_{max} + f_{min} - 2f_O)/f_O$, where f_{max} and f_{min} are the frequencies corresponding to the edges of the detection band. If necessary, the detection band skew can be reduced to zero by an optional centering adjustment.

PIN DESCRIPTION

OUTPUT FILTER — C_3 (Pin 1)

Capacitor C_3 connected from pin 1 to ground forms a simple low-pass post detection filter to eliminate spurious outputs due to out-of-band signals. The time constant of the filter can be expressed as $T_3 = R_3C_3$, where R_3 (4.7kΩ) is the internal impedance at pin 1.

The precise value of C_3 is not entical for most applications. To eliminate the possibility of false triggering by spurious signals, it is recommended that C_3 be $\geq 2\ C_2$, where C_2 is the loop filter capacitance at pin 2.

If the value of C_3 becomes too large, the turn-on or turn-off time of the output stage will be delayed until the voltage change across C_3 reaches the threshold voltage. In certain applications, the delay may be desirable as a means of suppressing spurious outputs. Conversely, if the value of C_3 is too small, the beat rate at the output of the quadrature detector may cause a false logic level change at the output. (Pin 8)

The average voltage (during lock) at pin 1 is a function of the inband input amplitude in accordance with the given transfer characteristic.

LOOP FILTER — C_2 (Pin 2)

Capacitor C_2 connected from pin 2 to ground serves as a single pole, low-pass filter for the PLL portion of the LM567C. The filter time constant is given by $T_2 = R_2C_2$, where R_2 (10 kΩ) is the impedance at pin 2.

The selection of C_2 is determined by the detection bandwidth requirements. For additional information see the section on "Definition of LM567C Parameters."

The voltage at pin 2, the phase detector output, is a linear function of frequency over the range of 0.95 to 1.05 f_O, with a slope of approximately 20 mV/% frequency deviation.

INPUT (Pin 3)

The input signal is applied to pin 3 through a coupling capacitor. This terminal is internally biased at a dc level 2 volts above ground, and has an input impedance level of approximately 20 kΩ

TIMING RESISTOR R_1 AND CAPACITOR C_1 (Pins 5 and 6)

The center frequency of the decoder is set by resistor R_1 between pins 5 and 6, and capacitor C_1 from pin 6 to ground, as shown in Figure 3.

Pin 5 is the oscillator squarewave output which has a magnitude of approximately V_{CC} — 1.4V and an average dc level of $V_{CC}/2$. A 1 kΩ load may be driven from this point. The voltage at pin 6 is an exponential triangle waveform with a peak-to-peak amplitude of 1 volt and an average dc level of $V_{CC}/2$. Only high impedance loads should be connected to pin 6 to avoid disturbing the temperature stability or duty cycle of the oscillator.

LOGIC OUTPUT (Pin 8)

Terminal 8 provides a binary logic output when an input signal is present within the pass-band of the decoder. The logic output is an uncommitted, "base-collector" power transistor capable of switching high current loads. The current level at the output is determined by an external load resistor R_L, connected from pin 8 to the positive supply.

When an in-band signal is present, the output transistor at pin 8 saturates with a collector voltage less than 1 volt (typically 0.6V) at full rated current of 100 mA. If large output voltage swings are needed, R_L can be connected to a supply voltage, V+, higher than the V_{CC} supply. For safe operation, V+ $\leq$ 20 volts.

OPERATING INSTRUCTIONS

SELECTION OF EXTERNAL COMPONENTS

A typical connection diagram for the LM567C is shown in Figure 3. For most applications, the following procedure will be sufficient for determination of the external components R_1, C_1, C_2, and C_3.

1. R_1 and C_1 should be selected for the desired center frequency by the expression $f_O = 1/R_1C_1$. For optimum temperature stability, R_1 should be selected such that 2kΩ, and the R_1C_1 product should have sufficient stability over the projected operating temperature range.
2. Low-pass capacitor, C_2, can be determined from the Bandwidth versus Input Signal Amplitude graph of Figure 7. One approach is to select an area of operation from the graph, and then adjust the input level and value of C_2 accordingly. Or, if the input amplitude variation is known, the required f_OC_2 product can be found to give the desired bandwidth. Capacitor C_2 connected from pin 2 to ground serves as a single pole, low-pass filter for the PLL portion of the LM567C. solely by the f_OC_2 product.
3. Capacitor C_3 sets the band edge of the low-pass filter which attenuates frequencies outside of the detection band and thereby eliminates spurious outputs. If C_3 is too small, frequencies adjacent to the detection band may switch the output stage off and on at the beat frequency, or the output may pulse off and on during the turn-on transient, a typical minimum value of C_3 is 2 C_2.

Conversely, if C_3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage across C_3 passes the threshold value.

PRINCIPLE OF OPERATION

The LM567C is a frequency selective tone decoder system based on the phase-locked loop (PLL) principle. the system is comprised of a phase-locked loop, a quadrature AM detector, a voltage comparator, and an output logic driver. The four sections are internally interconnected as shown in Figure 1.

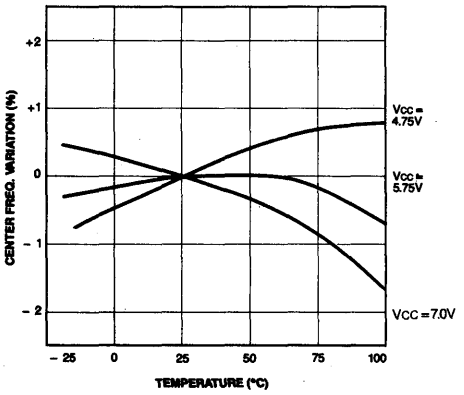
When an input tone is present within the pass-band of the circuit, the PLL synchronizes or "locks" on the input signal. The quadrature detector serves as a lock indicator: when the PLL is locked on an input signal, the dc voltage at the output of the detector is shifted. This dc level shift is then converted to an output logic pulse by the amplifier and logic driver. The logic driver is a "bare collector" transistor stage capable of switching 100 mA loads.

The logic output at pin 8 is normally in a "high" state, until a tone that is within the capture range of the decoder is present at the input. When the decoder is locked on an input signal, the logic output at pin 8 goes to a "low" state.

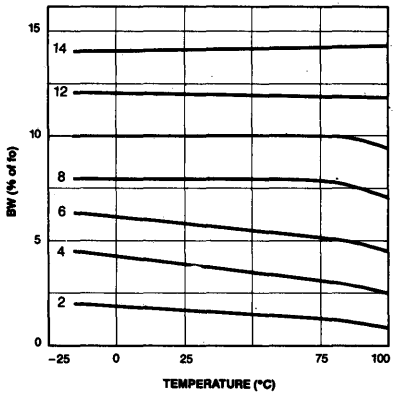
The center frequency of the detector is set by the free-running frequency of the current-controlled oscillator in the PLL. This free-running frequency, f_O, is determined by the selection of R_1 and C_1 connected to pins 5 and 6, as shown in Figure 3. The detection bandwidth is determined by the size of the PLL filter capacitor, C_2; and the output response speed is controlled by the output filter capacitor, C_3

TYPICAL CHARACTERISTICS

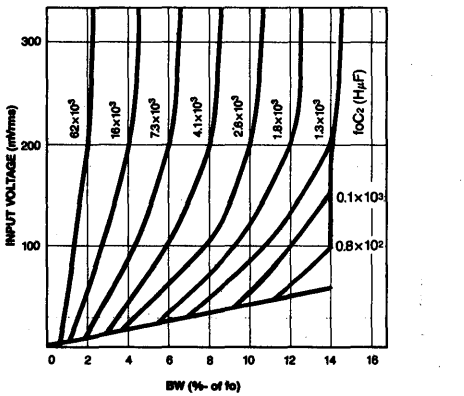
CENTER FREQ. VS TEMPERATURE



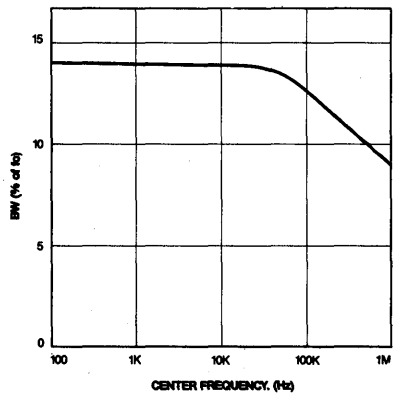
TYP. BW VS TEMPERATURE



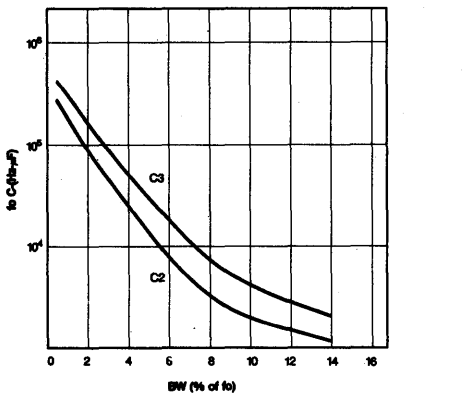
BW VS INPUT VOLTAGE.



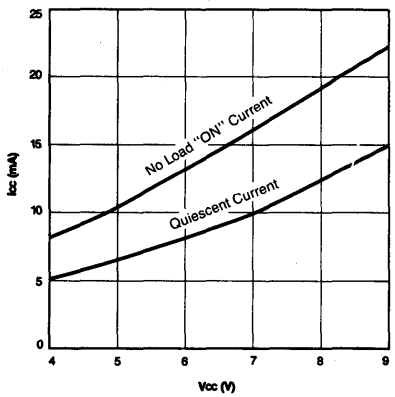
BW VS CENTER FREQUENCY

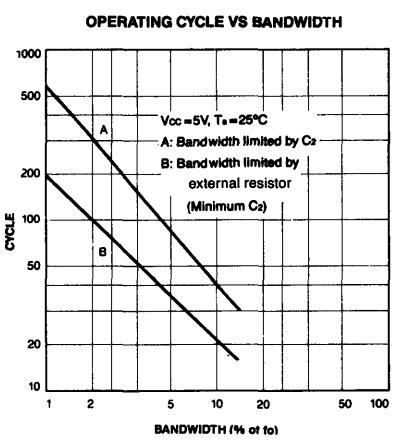


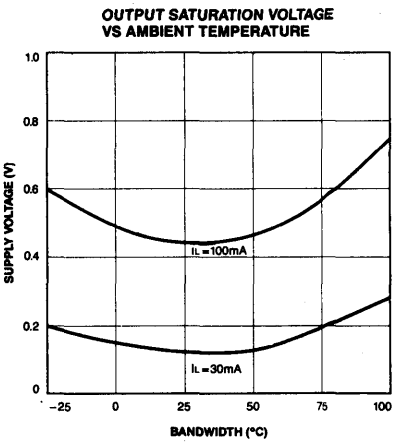
BW (C2, C3 CHARCT.)



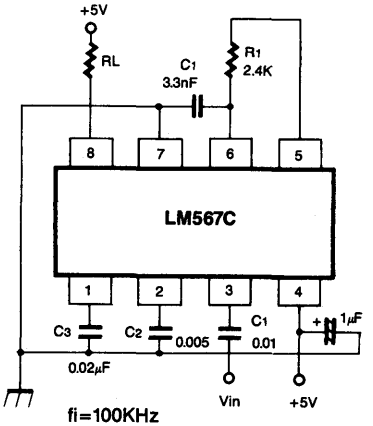
CURRENT DRAIN VS. VCC







AC TEST CIRCUIT

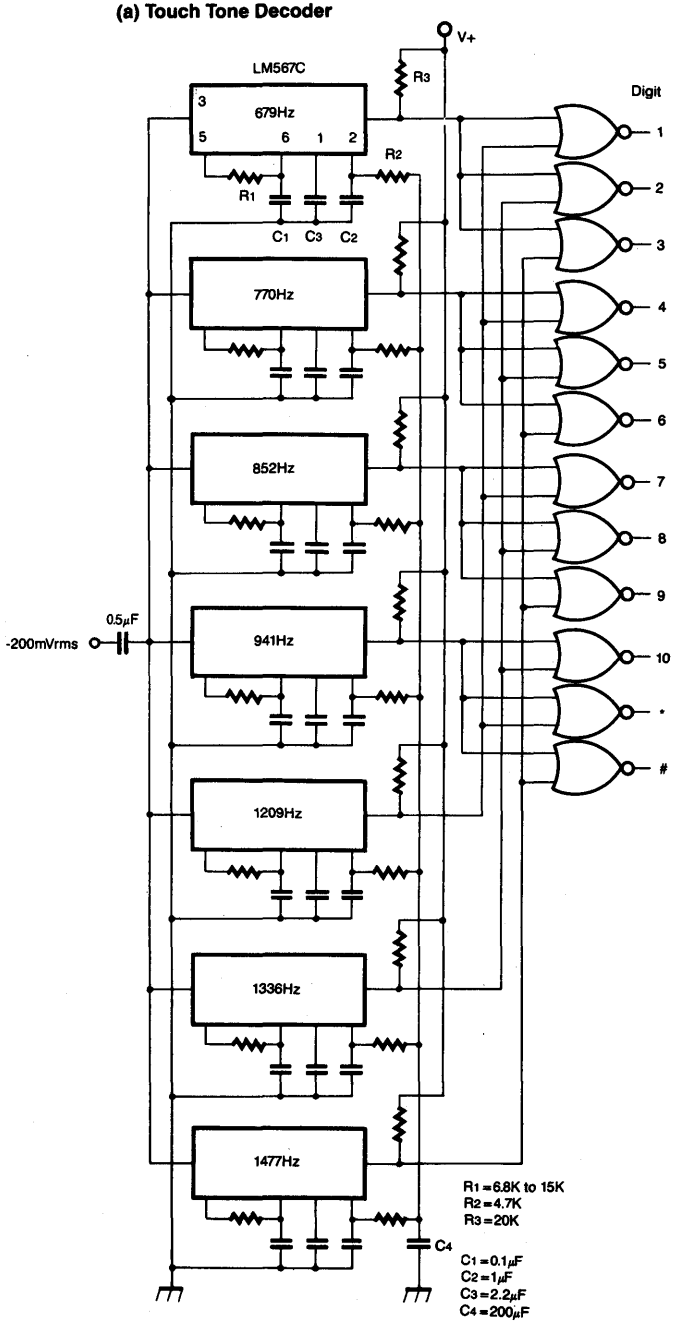


fi=100KHz
Note: Adjust for fo=100KHz

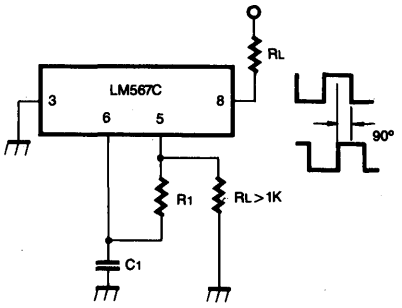
Fig. 2

APPLICATION CIRCUIT

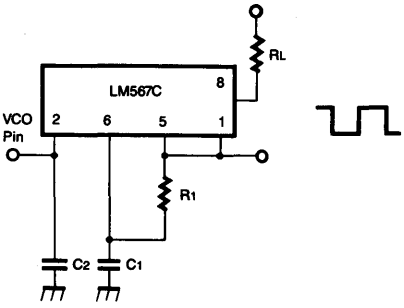
(a) Touch Tone Decoder



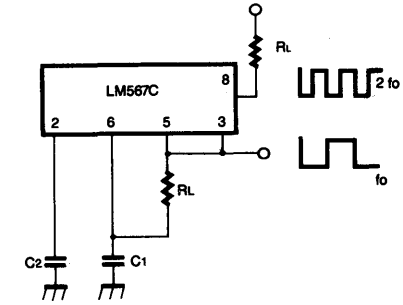
(b) 2-Phase Oscillator



(c) Variable Oscillator

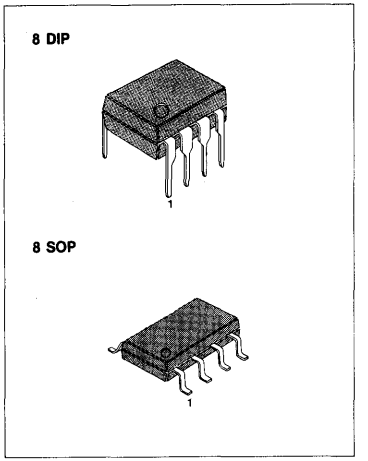


(d) Frequency Doubler



MICROPOWER TONE DECODER

The LM567L is a micropower phase-locked loop (PLL) circuit designed for general purpose tone and frequency decoding. In applications requiring very low power dissipation, the LM567L can replace the popular 567 type decoder with only minor component value changes. The LM567L offers approximately 1/10th the power dissipation of the conventional 567 type tone decoder, without sacrificing its key features such as the oscillator stability, frequency selectivity, and detection threshold. Typical quiescent power dissipation is less than 4mW at 5 volts.



FEATURES

- **Very low power dissipation (4mW at 5V)**
- **Bandwidth adjustable from 0 to 14% of f_o**
- **Logic compatible output with 10mA current sinking capability.**
- **Highly stable center frequency.**
- **Center frequency adjustable from 0.01Hz to 60KHz.**
- **Inherent immunity to false signals.**
- **High rejection of out-of-band signals and noise.**
- **Frequency range adjustable over 20:1 range by external resistor.**

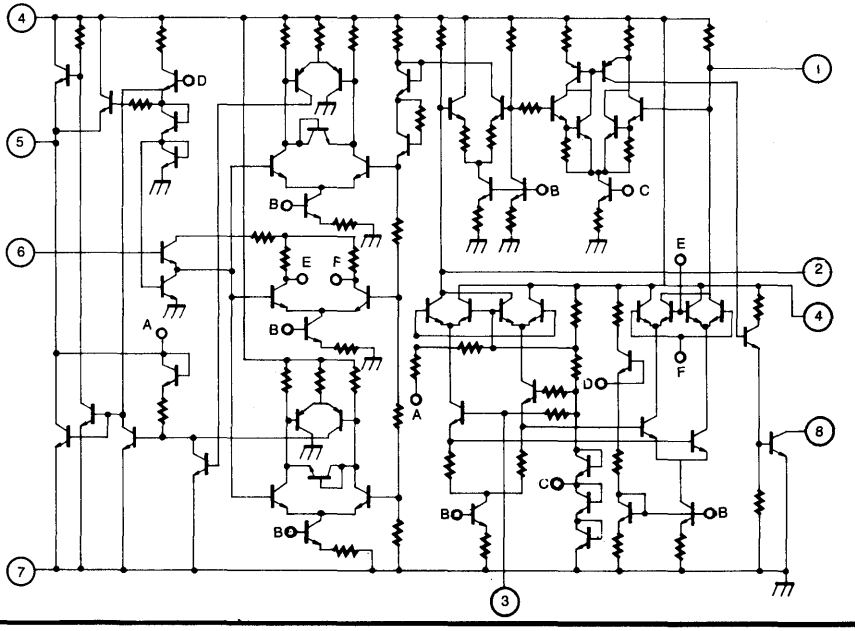
APPLICATIONS

- **Battery-operated tone detection**
- **Touch-tone decoding**
- **Sequential tone decoding**
- **Communications paging**
- **Ultrasonic remote-control**
- **Telemetric decoding**

ORDERING INFORMATION

Device	Package	Operating Temperature
LM567LN	8 DIP	0 ~ +70°C
LM567LD	8 SOP	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

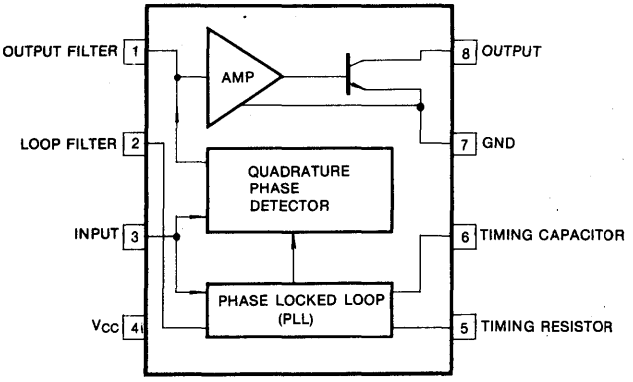
Characteristic	Symbol	Value	Unit
Power Supply	V_{CC}	10	V
Power Dissipation			
Plastic Package	P_d	300	mW
Derate Above +25°C		2.5	mW/°C
Operating Temperature	Topr	0 ~ +70	°C
Storage Temperature	Tstg	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, T_a = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Range	V_{CC}		4.75		8.0	V
Supply Current/Quiescent Supply Current/Activated	I_{CC-1} I_{CC-2}	R_L = 20KΩ, R_L = 20KΩ, V_{IN} = 300mV_{rms}, $f_i = f_o$		0.6 0.8	1.0 1.4	mA mA
Highest Center Frequency	H_{fo}	R1 = 3KΩ ~ 5KΩ	10	60		KHz
Center Frequency Drift Temperature 0<T_a<70°C Supply Voltage		 See Figures 15 and 16 f_O = 10KHz, V_{CC} = 4.75 ~ 5.75V		 − 150 0.5	 3.0	 ppm/°C %/V
Largest Detection Bandwidth	B.W	f_o = 10KHz, V_{IN} = 300mV_{rms} R_L = 20KΩ	10	14	18	% of f_o
Largest Detection Bandwidth Skew	B.Ws	See Figure 4 for Definition		2	3	% of f_o
Largest Detection Bandwidth Variation With Temperature	B.Wt	V_{IN} = 300mV_{rms}, R_L = 20KΩ		± 0.1		%/°C
Largest Detection Bandwidth Variation With Spply Voltage	B.Wv	V_{IN} = 300mV_{rms}, R_L = 20KΩ		± 2		%/V
Input Resistance	R_{IN}			100		KΩ
Smallest Detectable Input Voltage	V_{IN-1}	I_L = 10mA, $f_i = f_o$ = 10KHz		20	25	mV_{rms}
Largest No-Output Input Voltage	V_{IN-2}	I_L = 10mA, $f_i = f_o$ = 10KHz	10	15		mV_{rms}
Greatest Simultaneous Outband Signal to Inband Signal Ratio	S_1/S_d	V_{IN} = 300mV_{rms}, f_i'1 = 6KHz $f_i = f_o$ = 10KHz		+ 6		dB
Minimum Input Signal to Wideband Noise Ratio	S_2/S_d	V_{IN} = 300mV_{rms}, f_i'2 = 14KHz $f_i = f_o$ = 10KHz		− 6		dB
Output Saturation Voltage	V_{SAT-1}	I_L = 2mA, V_{IN} = 25mV_{rms}		0.2	0.4	V
	V_{SAT-2}	I_L = 10mA, V_{IN} = 25mV_{rms}		0.3	0.6	V
Output Leakage Current	I_{CO}			0.01	25	μA
Fastest On/Off Cycling Rate	F_{OUT}	$f_i = f_o$ = 10KHz	f_o/20			
Output Rise Time	T_r	R_L = 1KΩ		150		nS
Output Fall Time	T_f	R_L = 1KΩ		30		nS

BLOCK DIAGRAM



TEST CIRCUIT

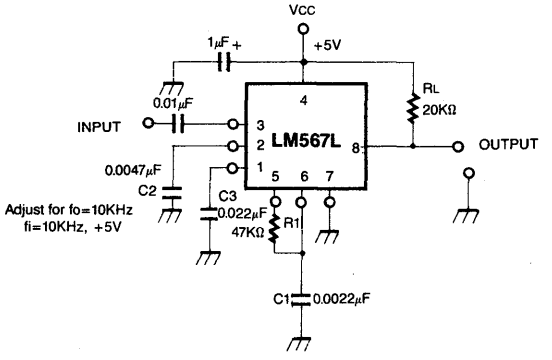


Fig. 1

TYPICAL APPLICATION CIRCUIT

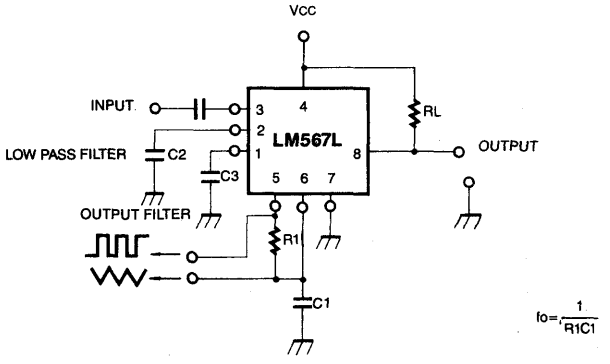


Fig. 2

CIRCUIT DESCRIPTION

The LM567L monolithic circuit consists of a phase detector, low pass filter, and current controlled oscillator which comprise the basic phase-locked loop, plus an additional low pass filter and quadrature detector enabling detection of in-band signals. The device has a normally high open collector output.

The input signal is applied to Pin 3 (100KΩ nominal input resistance). Free running frequency is controlled by an RC network at pins 5 and 6. A capacitor on pin 1 serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 2; band-width and skew are also dependent upon the circuitry here. Pin 4 is $+V_{CC}$ (4.75 to 8V nominal, 10V maximum); Pin 7 is ground; and Pin 8 is the open collector output, pulling low when an in-band signal triggers the device.

The LM567L is pin-for-pin compatible with the standard LM567-type decoder. Internal resistors have been scaled up by a factor of ten, thereby reducing power dissipation and allowing use of smaller capacitors for the same applications compared to the standard part. This scaling also lowers maximum device center frequency and load current sinking capabilities.

PRINCIPLES OF OPERATION

The LM567L is a frequency selective tone decoder system based on the phase-locked loop (PLL) principle. The system is comprised of a phase-locked loop, a quadrature detector, a voltage comparator, and an output logic driver.

When an input tone is present within the pass-band of the circuit, the PLL synchronizes or "locks" on the input signal. The quadrature detector serves as a lock indicator: when the PLL is locked on an input signal, the DC voltage at the output of the detector is shifted. This DC level shift is then converted to an output logic pulse by the amplifier and logic driver. The logic output at Pin 8 is an "open-collector" NPN transistor stage capable of switching 10mA current loads.

The logic output at Pin 8 is normally in a "high" state, until a tone that is within the capture range of the decoder is present at the input. When the decoder is locked on an input signal, the logic output at Pin 8 goes to a "low" state.

Fig 3 shows the typical output response of the circuit for a tone-burst applied to the input, within the detection band.

The center frequency of the detector is set by the free-running frequency of the current-controlled oscillator in the PLL. This free-running frequency, f_o, is determined by the selection of R1 and C1 connected to Pins 5 and 6, as shown in Fig 2. The detection bandwidth is determined by the size of the PLL filter capacitor, C2 (see Fig 10); and the output response speed is controlled by the output filter capacitor, C3.

DEFINITION OF DEVICE PARAMETERS

CENTER FREQUENCY f_O

f_O is the free-running frequency of the current-controlled oscillator with no input signal. It is determined by resistor R1 between Pins 5 and 6, and capacitor C1 from Pin 6 to ground, f_O can be approximated by

$$f_O = \frac{1}{R1C1}\ \text{Hz}$$ where R1 is in ohms and C1 is in farads.

DETECTION BANDWIDTH (BW)

The largest detection bandwidth is the frequency range centered about f_O, within which an input signal larger than the threshold voltage (typically $20mV_{rms}$) will cause a logic zero state at the output. The detection bandwidth corresponds to the capture range of the PLL and is determined by the low-pass loop filter at Pin 2. Typical dependence of detection bandwidth on the filter capacitance and the input signal amplitude is shown in Figs 10 and 11, or may be calculated by the approximation.

$$B\cdot W\ (\%) = 338\sqrt{\frac{V_i\ (\text{RMS})}{f_O\ (\text{Hz})\cdot C_2\ (\mu\text{F})}}$$

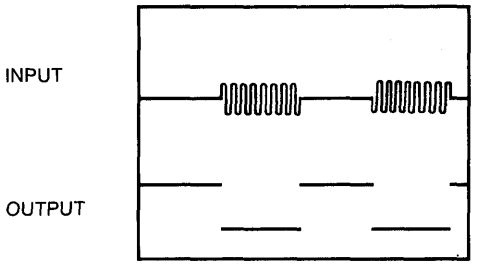
LARGEST DETECTION BANDWIDTH

The largest detection bandwidth is the largest frequency range within which an input signal above the threshold voltage will cause a logical zero state at the output. The maximum detection bandwidth corresponds to the lock range of the PLL.

DETECTION BANDWIDTH SKEW

The detection bandwidth skew is a measure of how accurately the largest detection band is centered about the center frequency f_o. This parameter is graphically illustrated in Fig 4. In the figure, f_{min} and f_{max} correspond to the lower and the upper ends of the largest detection band, and f1 corresponds to the apparent center of the detection band, and is defined as the arithmetic average of fmin and fmax and f_O is the free running frequency of the LM567L oscillator section. The bandwidth skew Δf_X is the difference between these frequencies. Normalized to f_o, this bandwidth skew can be expressed as:

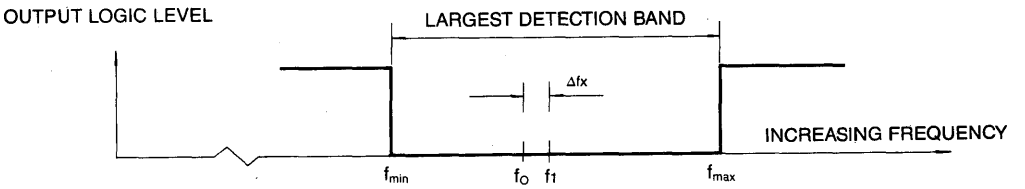
$$\text{Bandwidth Skew} = \frac{\Delta fx}{f_O} = \frac{(fmax + fmin - 2\,f_O)}{2\,f_O}$$



Response to $100mV_{rms}$ tone burst. $R_L = 1K\Omega$

Fig. 3. Typical Output Response to 100mV Input Tone-Burst

If necessary, the detection bandwidth skew can be reduced to zero by an optional centering adjustment. (see optional controls.)



f_O = PLL free-running frequency
f1 = Center freq of detection band = $(f_{max} + f_{min})/2$

Fig. 4. Definition of Bandwidth Skew

PIN DESCRIPTION AND EXTERNAL COMPONENTS

PIN 3: INPUT

The input signal is applied to Pin 3 through a coupling capacitor. This terminal is internally biased at a DC level 2 volts above ground, and has an input impedance level of approximately 100KΩ.

PIN 5 and 6: TIMING RESISTOR R1 and CAPACITOR C1

The center frequency of the decoder is set by resistor R1 between Pins 5 and 6, and capacitor C1 from Pin 6 to ground, as shown in Fig 2.

Pin 5 is the oscillator squarewave output which has a magnitude of approximately V_{CC}-1.4V and an average DC level of $V_{CC}/2$.A 5KΩ load may be driven from this point. The voltage at pin 6 is an exponential triangle waveform with a peak-to-peak amplitude of=$(V_{CC}$-1.3)/3.5 volts and an average DC level of $V_{CC}/2$. Only high impedance loads should be connected to Pin 6 to avoid disturbing the temperature stability or duty cycle of the oscillator.

PIN 2: LOOP FILTER-C2

Capacitor C2 connected from Pin 2 to ground serves as a single pole, low-pass filter for the PLL portion of the LM567L. The filter time constant is given by T2=R2C2, where R2 (100KΩ) is the impedance at Pin 2.

The selection of C2 is determined by the detection bandwidth requirements, as shown in Fig 10. For additional information see section on "Definition of Device Parameters."

The voltage at Pin 2, the phase detector output, is a linear function of frequency over the range of 0.95 f_O to 1.05 f_O, with a slope of approximately 20mV/% frequency deviation.

PIN 1: OUTPUT FILTER-C3

Capacitor C3 connected from Pin 1 to ground forms a simple low-pass post detection filter to eliminate spurious outputs due to out-of-band signals. The time constant of the filter can be expressed as T3=R3C3, where R3 (47KΩ) is the internal impedance at Pin 1.

If the value of C3 becomes too large, the turn-on or turn-off time of the output stage will be delayed until the voltage change across C3 reaches the threshold voltage. In certain applications, the delay may be desirable as a means of suppressing spurious outputs. Conversely, if the value of C3 is too small, the beat rate at the output of the quadrature detector may cause a false logic level change at the output (Pin 8).

The average voltage (during lock) at Pin 1 is a function of the in-band input amplitude in accordance with the given transfer characteristic.

PIN 8: LOGIC OUTPUT

Terminal 8 provides a binary logic output when an input signal is present within the pass-band of the decoder. The logic output is an uncommitted, open-collector power transistor capable of switching high current loads. The current level at the output is determined by an external load resistor, RL, connected from Pin 8 to the positive supply.

When an in-band signal is present the output transistor at Pin 8 saturates with a collector voltage of less than 0.6V at full rated output current of 10mA. If large output voltage swings are needed, RL can be connected to a supply voltage, V+, higher than the V_{CC} supply. For safe operation, V+ ≤15 volts.

OPERATING INSTRUCTIONS

SELECTION OF EXTERNAL COMPONENTS

A typical connection diagram for the LM567L is shown in Fig 2. For most applications, the following procedure will be sufficient for determination of the external components R1, C1, C2, and C3.

1. R1 and C1 should be selected for the desired center frequency by the expression $f_O \approx 1/R1C2$. For optimum temperature stability, R1 should be selected such that 20KΩ ≤ R1 ≤200KΩ, and the R1C1 product should have sufficient stability over the projected operating temperature range.
2. Low-pass capacitor, C2, can be determined from the bandwidth versus input signal amplitude graph of Fig 10. One approach is to select an area of operation from the graph, and then adjust the input level and value of C2 accordingly. Or if the input amplitude variation is known, the required f_O C2 product can be found to give the desired bandwidth. Constant bandwidth operation requires $V_i > 200mV_{rms}$. Then, as noted on the graph, bandwidth will be controlled solely by the f_O C2 product.
3. Capacitor C3 sets the band edge of the low-pass filter which attenuates frequencies outside of the detection band and thereby eliminates spurious outputs. If C3 is too small, frequencies adjacent to the detection band may switch the output stage off and on at the beat frequency, or the output may pulse off and on during the turn-on transient. A typical minimum value for C3 is 2 C2.

   Conversely, if C3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage across C3 passes the threshold value.

PRECAUTIONS

1. The LM567L will lock on signals near (2n+1) f_O and produce an output for signals near (4n+1) f_O, for n=0, 1, 2 etc. Signals at 5 f_O and 9 f_O can cause an unwanted output and should, therefore, be attenuated before reaching the input of the circuit.
2. Operating the LM567L in a reduced bandwidth mode of operation at input levels less than $200mV_{rms}$ results in maximum immunity to noise and out-band signals. Decreased loop damping, however, causes the worst-case lock-up time to increase, as shown by the graph of Fig 13.

3. Bandwidth variations due to changes in the in-band signal amplitude can be eliminated by operating the LM567L in the high input level mode, above 200mV$_{rms}$. The input stage is then limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in-band signal is suppressed. In addition, the limited input stage will create in-band components from subharmonic signals so that the circuit becomes sensitive to signals at $f_o/3$, $f_o/5$ etc.
4. Care should be exercised in lead routing and lead lengths should be kept as short as possible. Power supply leads should be properly bypassed close to the integrated circuit and grounding paths should be carefully determined to avoid ground loops and undesirable voltage variations. In addition, circuits requiring heavy load currents should be provided by a separate power supply, or filter capacitors increased to minimize supply voltage variations.

OPTIONAL CONTROLS

PROGRAMMING

Varying the value of resistor R1 and/or capacitor C1 will change the center frequency. The value of R1 can be changed either mechanically or by solid state switches. Additional C1 capacitors can be added by grounding them through saturated npn transistors.

SPEED OF RESPONSE

The minimum lock-up time is inversely related to the loop frequency. As the natural loop frequency is lowered, the turn-on transients becomes greater. Thus maximum operating speed is obtained when the value of capacitor C2 is minimum. At the instant an input signal is applied, its phase may drive the oscillator away from the incoming frequency rather than toward it. Under this condition, the lock-up transient is in a worst case situation, and the minimum theoretical lock-up time will not be achievable.

The following expressions yield the values of C2 and C3, in microfarads, which allow the maximum operating speeds for various center frequencies where f_o is Hz.

$$C2 = \frac{13}{f_o}, \quad C3 = \frac{26}{f_o} \ \mu F$$

The minimum rate that digital information may be detected without losing information due to turn-on transient or output chatter is about 10 cycles/bit, which corresponds to an information transfer rate of $f_o/10$ baud. In situations where minimum turn-off is of less importance than fast turn-on, the optional sensitivity adjustment circuit of Fig 5 can be used to bring the quiescent C3 voltage closer to the threshold voltage. Sensitivity to beat frequencies, noise, and extraneous signals, however, will be increased.

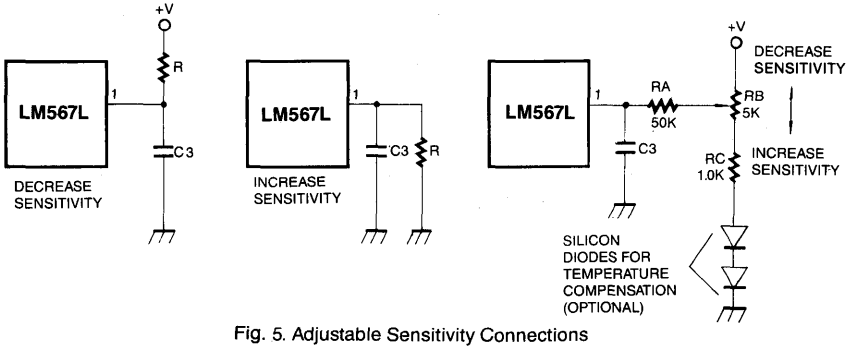


Fig. 5. Adjustable Sensitivity Connections

CHATTER

When the value of C3 is small, the lock transient and ac components at the lock detector output may cause the output stage to move through its threshold more than once, resulting in output chatter.

Although some loads, such as lamps and relays will not respond to chatter, logic may interpret chatter as a series of output signals. Chatter can be eliminated by feeding a portion of the output back to the input (Pin 1) or, by increasing the size of capacitor C3. Generally, the feedback method is preferred since keeping C_3 small will enable faster operation. Three alternate schemes for chatter prevention are shown in Fig 6. Generally, it is only necessary to assure that the feedback time constant does not get so large that it prevents operation at the highest anticipated speed.

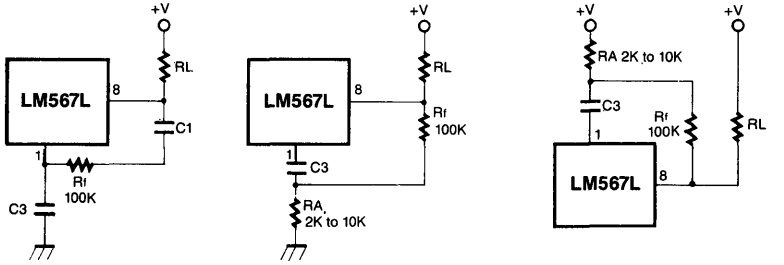


Fig. 6. Methods of Reducing Chatter

SKEW ADJUSTMENT

The circuits shown in Fig 7 can be used to change the position of the detection band (capture range) within the largest detection band (lock range). By moving the detection band to either edge of the lock range, input signal variations will expand the detection band in one direction only, since R_3 also has a slight effect on the duty cycle, this approach may be useful in obtaining a precise duty cycle when the circuit is used as an oscillator.

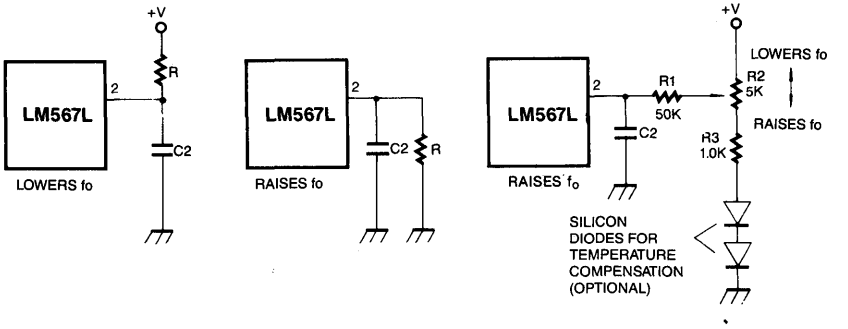


Fig. 7. Detection Band Skew Adjustment

TYPICAL PERFORMANCE CHARACTERISTICS

FIG 8. SUPPLY CURRENT
V_S SUPPLY VOLTAGE

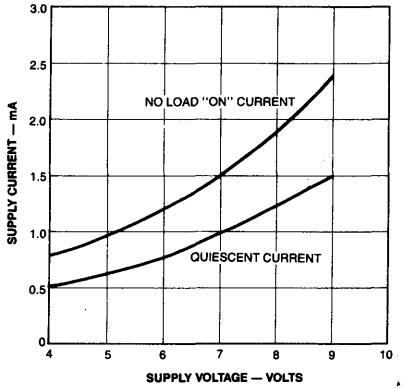


FIG 9. LARGEST DETECTION BANDWIDTH
V_S OPERATING FREQUENCY

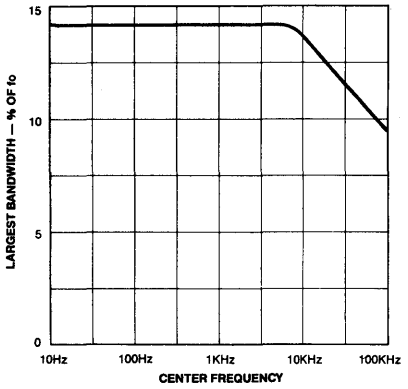


FIG 10. DETECTION BANDWIDTH
V_S A FUNCTION OF C2 AND C3

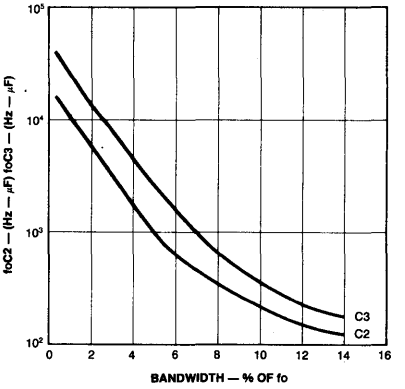


FIG 11. BANDWIDTH V_S INPUT SIGNAL
AMPLITUDE (C2 IN μF)

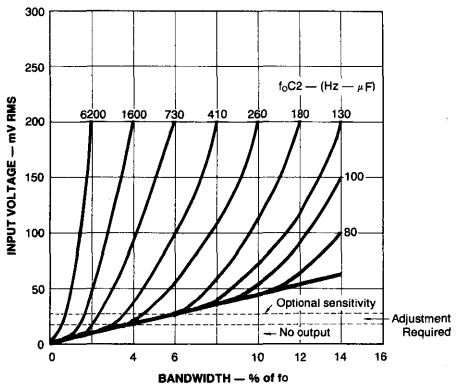


FIG 12. BANDWIDTH VARIATION
WITH TEMPERATURE

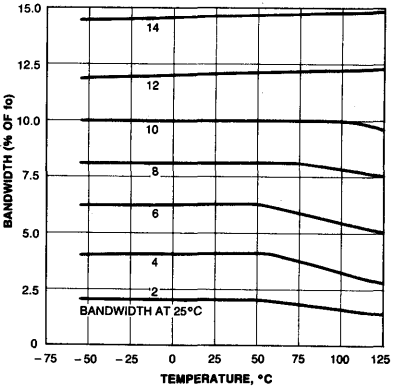


FIG 13. GREATEST NUMBER OF
CYCLES BEFORE OUTPUT

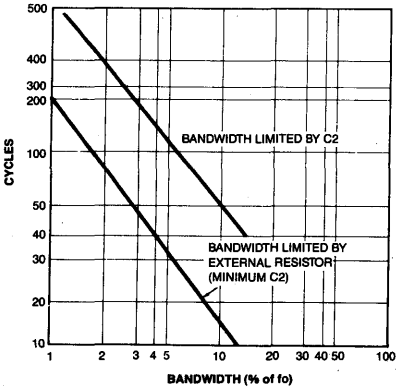


FIG 14. POWER SUPPLY DEPENDENCE OF CENTER FREQUENCY

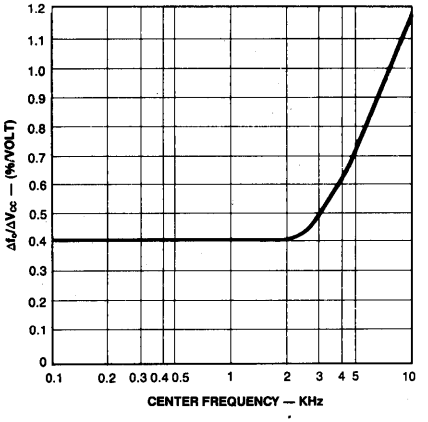


FIG 15. TYPICAL CENTER FREQUENCY DRIFT WITH TEMPERATURE(V_{CC} = 5V, R1 = 80kΩ, fo = 1KHz)

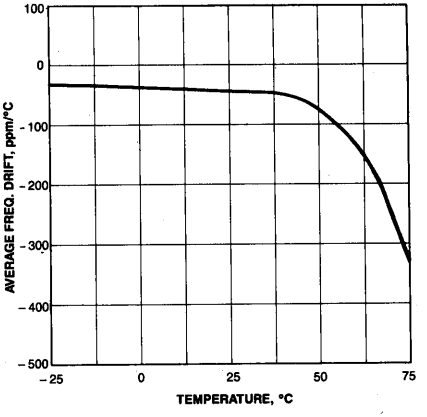
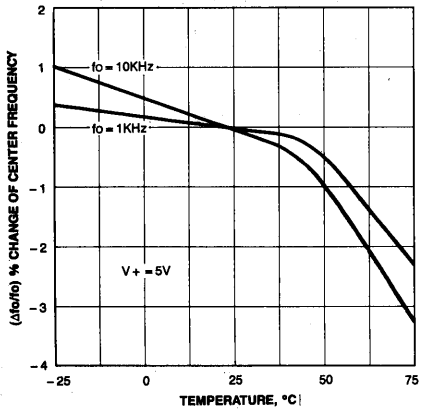
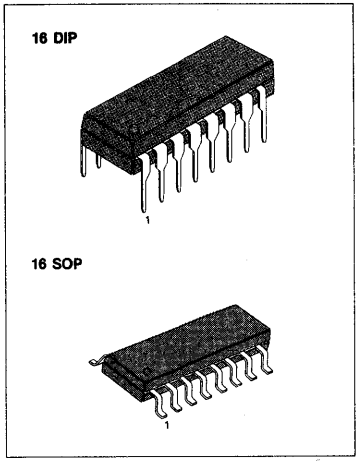


FIG 16. TYPICAL FREQUENCY DRIFT AS A FUNCTION OF TEMPERATURE



LOW VOLTAGE/POWER NARROW BAND FM IF

The MC3361 is designed for use in FM dual conversion communication. It contains a complete narrow band FM demodulation system operable to less than 2.5V supply voltage. This low-power narrow-band FM IF system provides the second converter, second IF, demodulator. Filter Amp and squelch circuitry for communications and scanning receivers.



FEATURES

- **Stable operation with wide supply voltage (2.5V to 7.0V)**
- **Low power consumption (4.0mA typ. at V_{CC} = 4.0V)**
- **Excellent input sensitivity (−3dB limiting, 2.0μV_{rms} typ)**
- **Minimum number of external components required.**

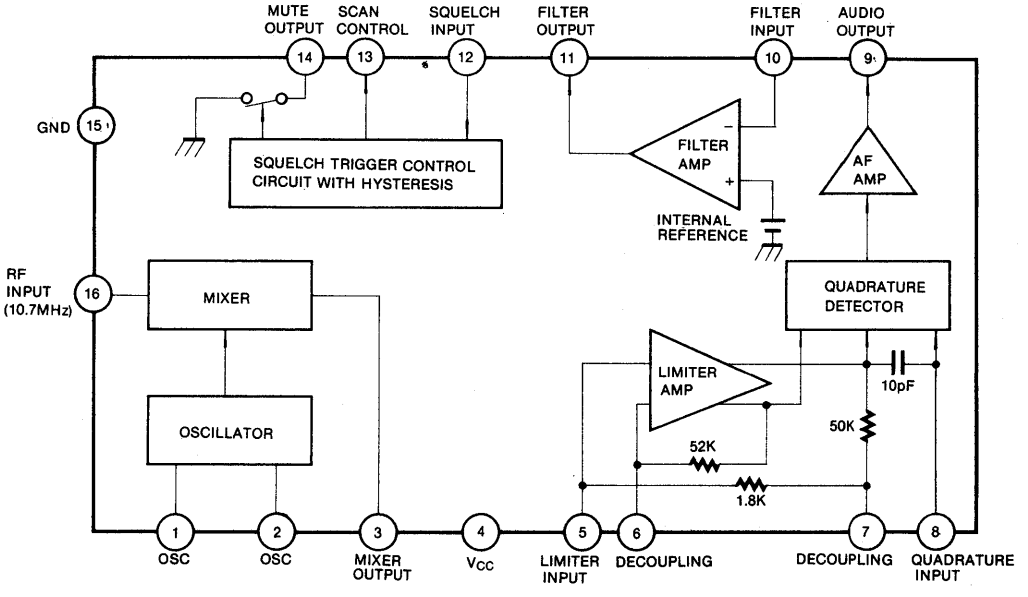
APPLICATION

- Cordless phone (for home use)
- FM dual conversion communications equipment

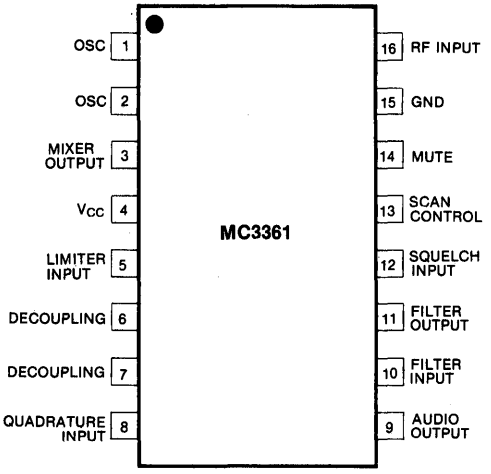
ORDERING INFORMATION

Device	Package	Operating Temperature
MC3361N	16DIP	−20 ~ +70°C
MC3361D	16 SOP	

BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC} (max)	10	V
Operating Voltage Range	V_{CC}	2.5 to 7.0	V
Detector Input Voltage	V_8	1.0	$V_{p\text{-}p}$
RF Input Voltage ($V_{CC} \geq 4.0V$)	V_{16}	1.0	V_{rms}
Mute Function	V_{14}	−0.5 ~ +5.0	V_{peak}
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

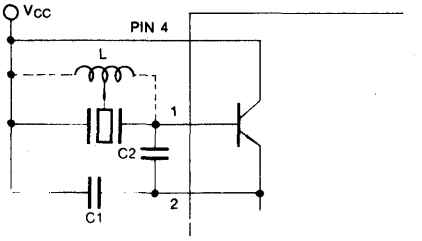
Absolute maximum ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.0V, fo = 10.7MHz, $\triangle f = \pm 3$KHz, f_{MOD} = 1KHz, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	I_{CC}	Squelch off (V_{12} = 2V) Squelch on (V_{12} = GND)		4.0 6.0		mA mA
Input Limiting Voltage	V_{INL}	−3.0dB limiting		2.0		μV
Detector Output Voltage	V_9			2.0		V_{dc}
Detector Output Impedance	Z_{OD}			400		Ω
Audio Output Voltage	V_O	V_{in} = 10mV	100	160		mV_{rms}
Filter Gain	A_{VF}	f = 10KHz, V_{in} = 5mV	40	48		dB
Filter Output DC Voltage	V_{OF}			1.5		V_{dc}
Trigger Hysteresis of Filter	V_{TH}			50		mV
Mute Switch-on Resistance	R_{ON}	Mute "Low"		10		Ω
Mute Switch-off Resistance	R_{OFF}	Mute "High"		10		MΩ
Scan Control "Low" Output	V_{13L}	Mute off (V_{12} = 2V)			0.5	V_{dc}
Scan Control "High" Output	V_{13H}	Mute on (V_{12} = GND)	3.0			V_{dc}
Mixer Conversion Gain	A_{VM}			24		dB
Mixer Input Resistance	R_{IM}			3.3		KΩ
Mixer Input Capacitance	C_{IM}			2.2		pF

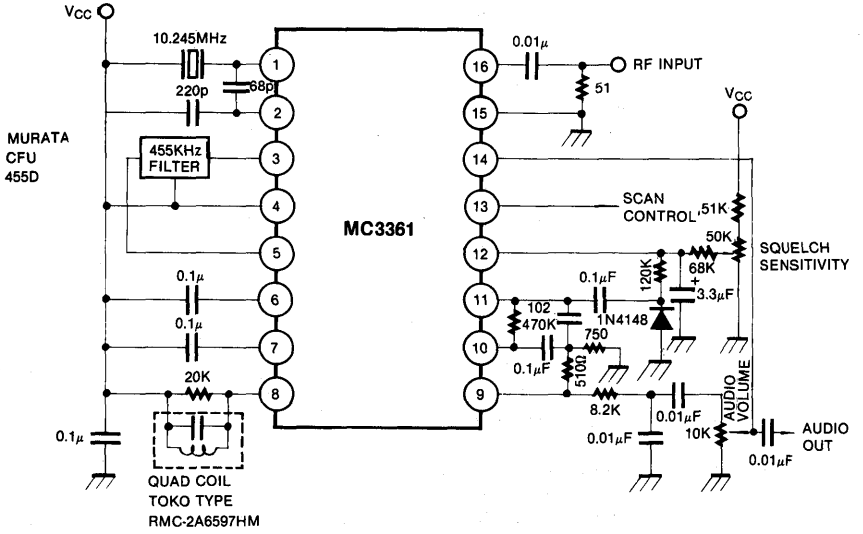
PIN DESCRIPTION

Pin No.	Name	Function
1, 2	OSC	The crystal oscillator terminals for mixer conversion. The colpitts oscillator is internally biased with a regulated current source which assures proper operation over a wide supply range. The collector, base and emitter terminals are at pins 4, 1, and 2 respectively. The crystal which is used in the parallel resonant mode, may be replaced with an appropriate inductor if the application does not require the stability of a crystal oscillator. 
3, 16	Mixer Input, (RF Input) Mixer Output	The mixer input/output terminals. The mixer converts the input frequency (10.7MHz) down to 455KHz. The mixer is double balanced to reduce spurious response. The mixer output impedance will properly match the input impedance of a ceramic filter which is used as a bandpass filter coupling the mixer output to the IF limiting amplifier. Following the mixer, a ceramic bandpass filter is recommended. The 455KHz types come in bandwidth from ±2KHz to ±15KHz.
4	V_{CC}	Power supply pin.
5, 6, 7	Limiter Amp Input, Decoupling	Limiter Amp inputs and decoupling terminals. The IF limiter amplifier consists of five differential gain stages, with the input impedance set by 1.8KΩ resistor to properly terminate the ceramic filter driving the IF. The IF output is connected to the external quad coil at pin 8 via an internal 10pF capacitor. The frequency limitation is due to the high resistance values in the IF, which were necessary to meet the low power requirement. The output of the limiter is internally connected to the quadrature detector.
8, 9	Quadrature Input, Audio Output	Quadrature detector input and output terminals. A conventional quadrature detector is used to demodulate the FM signal. The Q of the quad coil, which is determined by the external resistor placed across it, has multiple affects on the audio output. ($Q \propto R$) Increasing the Q increases audio output level but because of non-linearities in the tank phase characteristic, also increases distortion. For proper operation, the voltage swing on pin 9 should be adequate to prevent distortion (160mV_{ms} typ). The detector output is amplified and buffered to the audio output pin 9, which has an output impedance of approximately 400Ω.

PIN DESCRIPTION (Continued)

Pin No.	Name	Function
10, 11	Filter Input/ Output	Filter Amp input/output terminals. The inverting OP Amp is provided with an output at pin 11 providing dc bias (externally) to the input at pin 10 which is referred internally to 0.7V. The OP Amp is normally utilized as either a bandpass filter to extract a specific frequency from the audio output, such as a ring or dial tone, or as a high pass filter to detect noise due to no input at the mixer.
12, 13, 14	Squelch In, Scan Control, Mute Output	Squelch control input, scan control output, mute output terminals. A low bias to pin 12 sets up the squelch trigger circuit such that pin 13 is high, and the audio mute (pin 14) is internally short circuited to ground (typically 10Ω to GND). If pin 12 is raised above mute threshold (0.7V) by the noise or tone detector, pin 13 (scan control output) will become low level output and the audio mute will be an open circuit. There is 50mV of hysteresis at pin 12 which effectively prevents jitter.
15	GND	GND pin.

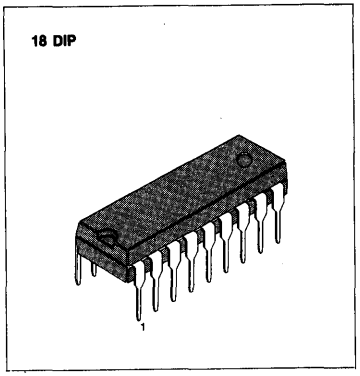
TYPICAL APPLICATION CIRCUIT



In the above typical application, the audio signal is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch trigger circuit indicates the presence of noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated which can be used to mute the audio.

LOW POWER DTMF RECEIVER

The KT3170 is a complete Dual Tone Multiple Frequency (DTMF) receiver that is fabricated by low power CMOS and the Switched-Capacitor Filter technology. This LSI consists of band split filters, which separates the high and low group tones, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus. It decodes all 16 DTMF tone pairs into a 4bits digital code.
The externally required components are minimized by on chip provision of a differential input AMP, clock oscillator and latched three state interface. The on chip clock generator requires only a low cost TV crystal as an external component.



FEATURES

- **Detects all 16 standard tones.**
- **Low power consumption: 15mW (Typ)**
- **Single power supply: 5V**
- **Uses inexpensive 3.58MHz crystal**
- **Three state outputs for microprocessor interface**
- **Good quality and performance for using in exchange system**
- **Package options include standard plastic and ceramic 300 mil DIPs**
- **Power down mode/input inhibit**

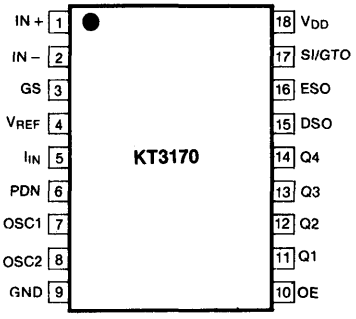
APPLICATIONS

- PABX
- Central Office
- Paging Systems
- Remote Control
- Credit Card Systems
- Key Phone System
- Answering Phone
- Home Automation System
- Mobile Radio
- Remote Data Entry

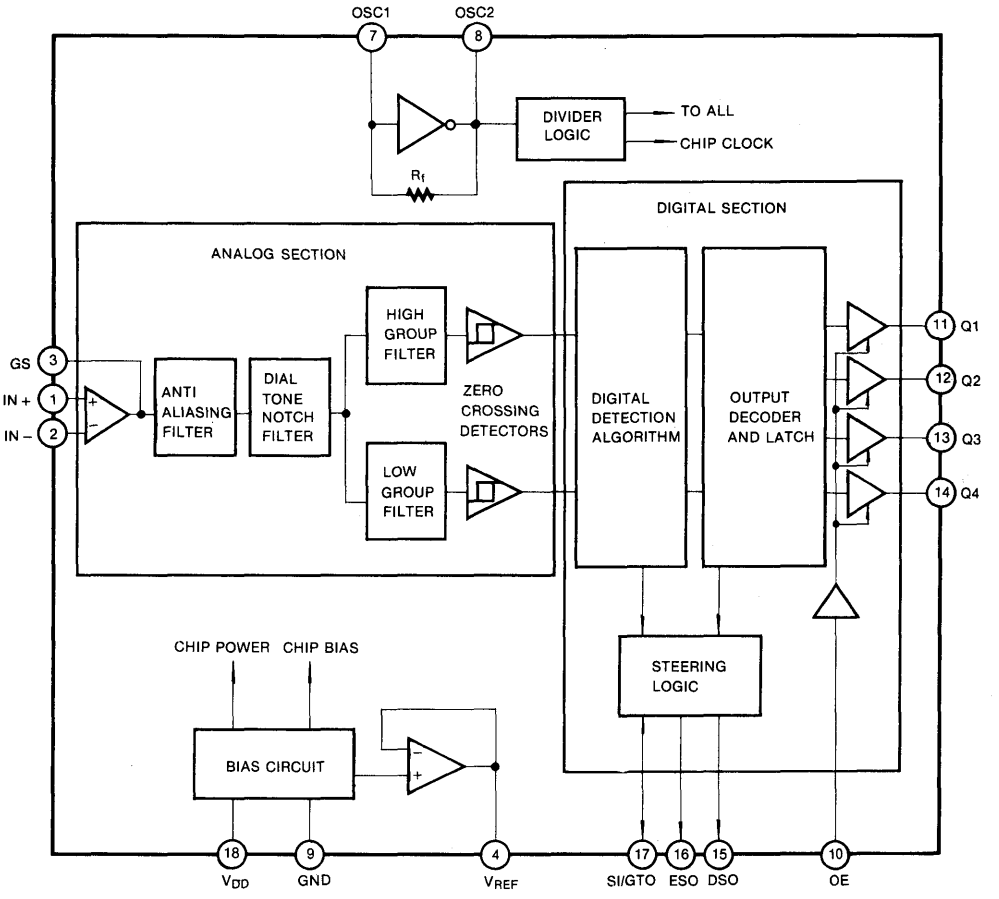
ORDERING INFORMATION

Device	Package	Operating Temperature
KT3170N	Plastic	−40 ~ +85°C
KT3170J	Ceramic	

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	6	V
Analog Input Voltage Range	V_{INA}	$-0.3 \sim V_{DD}+0.3$	V
Digital Input Voltage Range	V_{IND}	$-0.3 \sim V_{DD}+0.3$	V
Output Voltage Range	V_O	$-0.3 \sim V_{DD}+0.3$	V
Current On Any Pin	I_{IN}	10	mA
Operating Temperature	T_a	$-40 \sim +85$	°C
Storage Temperature	T_{stg}	$-60 \sim +150$	°C

* Absolute Maximum Ratings are these values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{DD} = 5V, Ta = 25°C, unless otherwise noted)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage	V_{DD}		4.75		5.25	V
Operating Supply Current	I_{DD}			3.0	9.0	mA
Power Dissipation	P_D			15	45	mW
Input Voltage Low	V_{IL}				1.5	V
Input Voltage High	V_{IH}		3.5			V
Input Leakage Current	I_{IH}/I_{IL}	V_{IN} = GND or V_{DD}		0.1		μA
Pull Up Current On OE Pin	I_{PU}	OE = GND		7.5	15	μA
Analog Input Impedance	R_{IN}	f_{IN} = 1KHz	8	10		MΩ
Steering Input Threshold Voltage	V_{TS}		2.2		2.5	V
Output Voltage Low	V_{OL}	No Load			0.03	V
Output Voltage High	V_{OH}	No Load	4.97			V
Output Current	I_{sink}	V_{OL} = 0.4V	1	2.5		mA
Output Current	I_{source}	V_{OH} = 4.6V	0.4	0.8		mA
V_{ref} Output Voltage	V_{ref}		2.4		2.8	V
V_{ref} Output Resistance	R_{ref}			10		KΩ
Analog Input Offset Voltage	V_{OS}			25		mW
Power Supply Rejection Ratio	PSRR	Gain Setting Amp at 1KHz		60		dB
Common Mode Rejection Ratio	CMRR	$-3.0V < V_{IN} < 3.0V$		60		dB
Open Loop Voltage Gain	A_V	Gain Setting Amp at 1KHz		65		dB
Open Loop Unit Gain Bandwidth	BW			1.5		MHz
Analog Output Voltage Swing	V_{AO}	R_L = 100K		4.5		V_{p-p}
Acceptable Capacitive Load	C_L	GS		100		pF
Acceptable Resistive Load	R_L	GS		50		KΩ
Analog Input Common Mode Voltage Range	V_{CM}	No Load		3.0		V_{p-p}

AC ELECTRICAL CHARACTERISTICS (V_{DD} = 5V, Ta = 25°C, f_C = 3.579545MHz)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Valid Input Signal Range (each tone of composite signal)	V_{INA}		−29		1.0	dBm
Dual Tone Twist Accept	TW			±10		dB
Acceptable Frequency Deviation	FDA				±1.5% ±2Hz	
Frequency Deviation Reject	FDR		±3.5%			
Third Tone Tolerance	T3		−25	−16		dB
Noise Tolerance	NT			−12		dB
Dial Tone Tolerance	DT		18	22		dB
Crystal Clock Frequency	f_c		3.5759	3.5795	3.5831	MHz
Maximum Clock Input Rise Time	t_r	External Clock			110	nS
Maximum Clock Input Fall Time	t_f	External Clock			110	nS
Acceptable Clock Input Duty Cycle	DC	External Clock	40	50	60	%
Acceptable Capacitive Load	CLO	OSC2 PIN			30	pF
Tone Present Detect Time	TDP		5	11	14	mS
Tone Absent Detect Time	TDA		0.5	4	8.5	mS
Minimum Tone Duration Accept	TUA	User Adjustable			40	mS
Maximum Tone Duration Reject	TUR	User Adjustable	20			mS
Acceptable Interdigit Pause	TAID	User Adjustable			40	mS
Rejectable Interdigit Pause	TRID	User Adjustable	20			mS
Propagation Delay Time SI to Q	TPSQ	OE = High		8	11	μS
Propagation Delay Time SI to DSO	T_{psds}	OE = High		12		μS
Output Data Setup Q to DSO	TSU	OE = High		3.4		μS
Propagation Delay Time OE to Q (Enable)	TPEQ	R_L = 10K, C_L = 50pF		50	60	nS
Propagation Delay Time OE to Q (Disable)	TPDQ	R_L = 10K, C_L = 50pF		300		nS

Notes:
1. Digit sequence consists of all 16 DTMF tones.
2. Tone duration = 40mS, Tone pause = 40mS.
3. Nominal DTMF frequencies are used.
4. Both tones in the composite signal have an equal amplitude.
5. Tone pair is deviated by ±1.5% ±2Hz.
6. Bandwidth limited (3KHz) Gaussian Noise.
7. The precise dial tone frequencies are (350Hz and 440Hz) ±2%.
8. For an error rate of better than 1 in 10000.
9. Referenced to lowest level frequency component in DTMF signal.
10. Minimum signal acceptance level is measured with specified maximum frequency deviation.
11. This item also applies to a third tone injected onto the power supply.
12. Referenced to Fig. 1 Input DTMF tone level at −28dBm.

PIN DESCRIPTION

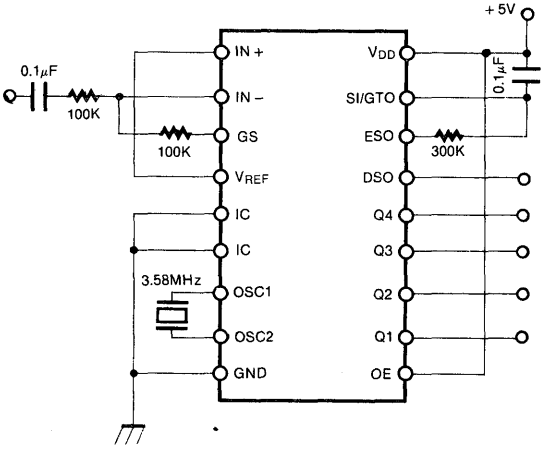
Pin	Name	Description
1	IN +	Non inverting Input of the op amp.
2	IN –	Inverting Input of the op amp.
3	GS	Gain Select. The output used for gain adjustment of analog input signal with a feedback resistor.
4	V_{ref}	Reference Voltage output (V_{DD}/2, Typ) can be used to bias the op amp input of V_{DD}/2.
5	I_{IN}	Input inhibit. High input states inhibits the detection of tones. This pin is pulled down internally.
6	P_{DN}	Control input for the stand-by power down mode. Power down occurs when the signal on this input is in high states. This pin is pulled down internally.
7, 8	OSC1 OSC2	Clock input/output. A inexpensive 3.579545MHz crystal connected between these pins completes internal oscillator. Also, external clock can be used.
9	GND	Ground pin.
10	OE	Output Enable input. Outputs Q1-Q4 are CMOS push pull when OE is High and open circuited (High impedence) when disabled by pulling OE low. Internal pull up resistor built in.
11-14	Q1-Q4	Three state data output. When enabled by OE, these digital outputs provide the hexadecimal code corresponding to the last valid tone pair received.
15	DSO	Delayed Steering Output. Indicates that valid frequencies have been present for the required guard time, thus constituting a valid signal. Presents a logic high when a received tone pair has been registered and the output latch is updated. Returns to logic low when the voltage on SI/GTO falls below V_{TS}.
16	ESO	Early Steering Outputs. Indicates detection of valid tone outputs a logic high immediately when the digital algorithm detects a recognizable tone pair. Any momentary loss of signal condition will cause ESO to return to low.
17	SI/GTO	Steering Input/Guard Time Output. A voltage greater than V_{TS} detected at SI causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TS} frees the device to accept a new tone pair. The GTO output acts to reset the external steering time constant, and its state is a function of ESO and the voltage on SI.
18	V_{DD}	Power Supply (+5V, Typ)

APPLICATION INFORMATION

The KT3170 is complete Touch-Tone detection system. It combines high precision active filter with analog circuits and digital control logic on a monolithic CMOS chip. This application information describes device operation of each block, performance and typically application circuit.

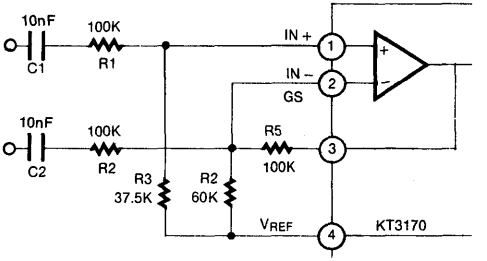
ANALOG INPUT CONFIGURATION

The KT3170 is designed to accept sinusoidal input waveforms but will operate satisfactorily with any input that has the correct fundamental frequency. The input arrangement provides a differential input op amp, bias source (reference voltage V_{REF}) which is used to bias the inputs at mid-rail. Connection of a feedback resistor to the op amp output (GS) makes gain of op amp adjust. The signal level at the input must be operated in power supply range on the data sheet. In a single ended configuration, the input pins are connected as shown in application circuit with unity gain and V_{REF} biasing. In a differential ended configuration the input pins are connected as shown in Fig. 2 with voltage gain (R5/R1).



All resistors are 1% tolerance
All capacitors are 5% tolerance

Fig. 1 Single Ended Input Configuration



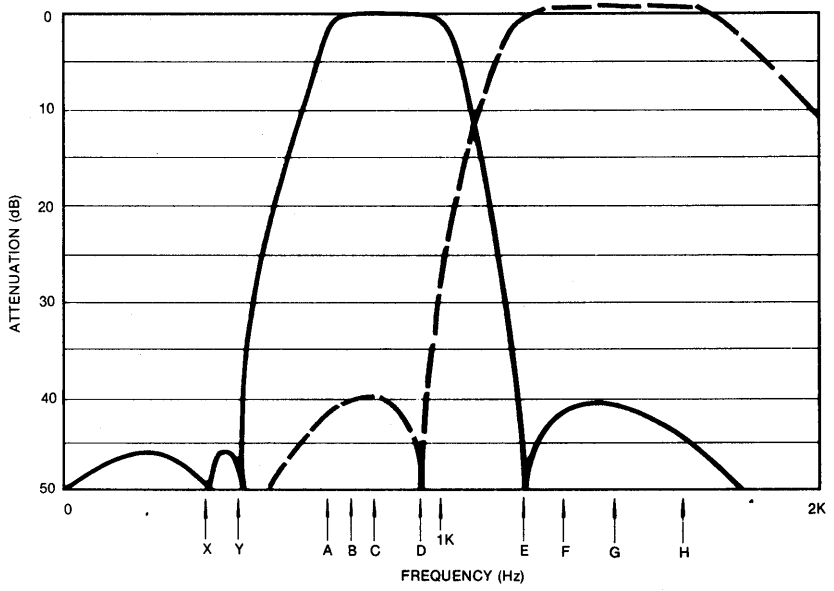
R3 = R2R5/(R2 + R5), VOLTAGE GAIN = R5/R1
INPUT IMPEDANCE: $2\sqrt{R_1^2 + (1/wC)^2}$

All resistors are 1% tolerance
All capacitors are 5% tolerance

Fig. 2 Differential Ended Input Configuration

FILTER SECTION

After analog signal is passed op amp, separation of the low group and high group tones is achieved by applying the DTMF signal to the inputs of two 9th-order switched capacitor band pass filter, the bandwidths of which correspond to the low and high group frequencies. The band split filters are actually rejecting all frequencies except the 16 DTMF tone pairs. The filter section also incorporates notches at 350 and 440Hz for exceptional dial tone rejection as shown below. Each filter output is followed by a single order switched capacitor section which smoothes the signals prior to limiting. Limiting is performed by high-gain comparator which are provided with hysteresis to prevent detection of unwanted low level signals. The outputs of the comparators provide full-rail logic swing at the frequencies of the incoming DTMF signals.



PRECISE DIAL TONES
X = 350Hz
Y = 440Hz

DTMF TONES

A = 697Hz	E = 1209Hz
B = 770Hz	F = 1336Hz
C = 852Hz	G = 1477Hz
D = 941Hz	H = 1633Hz

Fig. 3 Typical Filter Characteristics

DECODER SECTION

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations.

The averaging algorithm has been developed to ensure an optimum combination of immunity to "talk-off" and tolerance to the presence of interferring nsignals (third tones) and noise. When the detector recognizes the simultaneous presence of two valid tones (known as "signal condition"), it raises the "Early Steering" flag (ESO). Any loss of signal condition will cause the ESO to fall.

OSCILLATOR SECTION

The KT3170 contains an on chip inverter with sufficient gain a feedback resistor Rf to provide oscillation when connected to a low cost television "color-burst" crystal. The oscillator circuit is connected as shown in application circuit. It is possible to operate several KT3170 devices employing only a single crystal oscillator. The oscillator output of the first devices in the chain is coupled through a 30pF capacitor to the oscillator input (OSC1) of the next device; subsequent devices are connected in a similar fashion as shown Fig. 4. The problems for unbalanced loading are not a concern with the arrangement shown, i.e., balancing capacitors are not required.

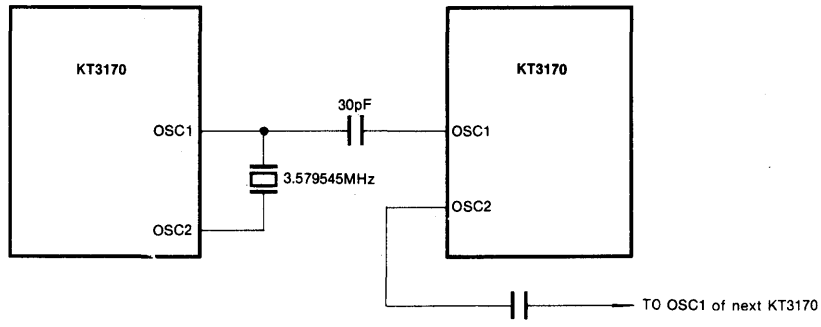


Fig. 4 Oscillator Connection

STEERING CIRCUIT

Before registration of a decoded tone pair, the receiver checks for a valid signal duration. This check is performed by an external RC time constant driven by the ESO. A logic high on the ESO causes V_C (see Fig. 5) to rise as the capacitor discharges. Providing signal condition is maintained (ESO remains high) for the validation period (t_{GTP}), V_C reaches the threshold (V_{TST}) of the steering logic to register the tone pair, thus latching its corresponding 4 bits code (see Table 1) into the output latch. At this point, the GTO output is activated and drives V_C to V_{DD}. GTO continues to drive high as long as the ESO remains high, finally after a short delay to allow the output latch to settle, the "delayed steering" output flag (STO) goes high, signalling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three-state control input (OE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruption (drop outs) too short to be considered a valid pause. This capability, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

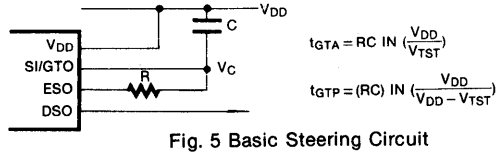


Fig. 5 Basic Steering Circuit

DIGITAL OUTPUT

Outputs Q1-Q4 are CMOS push pull when enabled (EO = High) and open circuited (high impedance) when disabled by pulling EO = Low. These digital outputs provide the hexadecimal code corresponding to the DTMF signals. The table below describes the hexadecimal.

NO	LOW FREQUENCY	HIGH FREQUENCY	OE	Q4	Q3	Q2	Q1
1	697	1209	H	0	0	0	1
2	697	1336	H	0	0	1	0
3	697	1477	H	0	0	1	1
4	770	1209	H	0	1	0	0
5	770	1336	H	0	1	0	1
6	770	1477	H	0	1	1	0
7	852	1209	H	0	1	1	1
8	852	1336	H	1	0	0	0
9	852	1477	H	1	0	0	1
0	941	1336	H	1	0	1	0
*	941	1209	H	1	0	1	1
#	941	1477	H	1	1	0	0
A	697	1633	H	1	1	0	1
B	770	1633	H	1	1	1	0
C	852	1633	H	1	1	1	1
D	941	1633	H	0	0	0	0
ANY	—	—	L	Z	Z	Z	Z

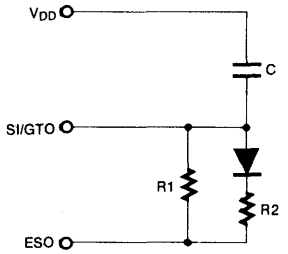
Z: High Impedance
H: High Logic Level
L: Low Logic Level

GUARD TIME ADJUSTMENT

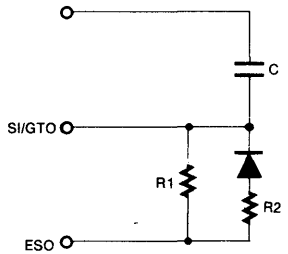
In a situations which do not require independent selection of receive and pause, the simple steering of Fig. 5 is applicable. Component values are chosen according to the following formula:

$t_{REC} = t_{DP} + t_{GTP}$, $t_{GTP} = 0.63RC$

The value of t_{DP} is a parameter of the device and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1μF is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a t_{REC} of 40 miliseconds would be 300K. A typical circuit using this steering configuration is shown in Figure 1. The timing requirements for most telecommunication applications are satisfied with this circuits. Different steering arrangements may be used to select independently the guard times for tone-present (t_{GTP}) and tone-absent (t_{GTA}). This may be necessary to meet system specifications which place both tone duration and interdigit pause. Guard time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition for long enough to be registered. On the other hand, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop-outs would be requirements. Design information for guard time adjustments is shown in Figure 6.



$t_{GTP} = (R1C)\ln(V_{DD}/V_{DD} - V_{TST})$
$t_{GTA} = (RpC)\ln(V_{DD}/V_{TST})$
$Rp = R1R2/(R1 + R2)$
(a) Decreasing t_{GTA}($t_{GTP} > t_{GTA}$)

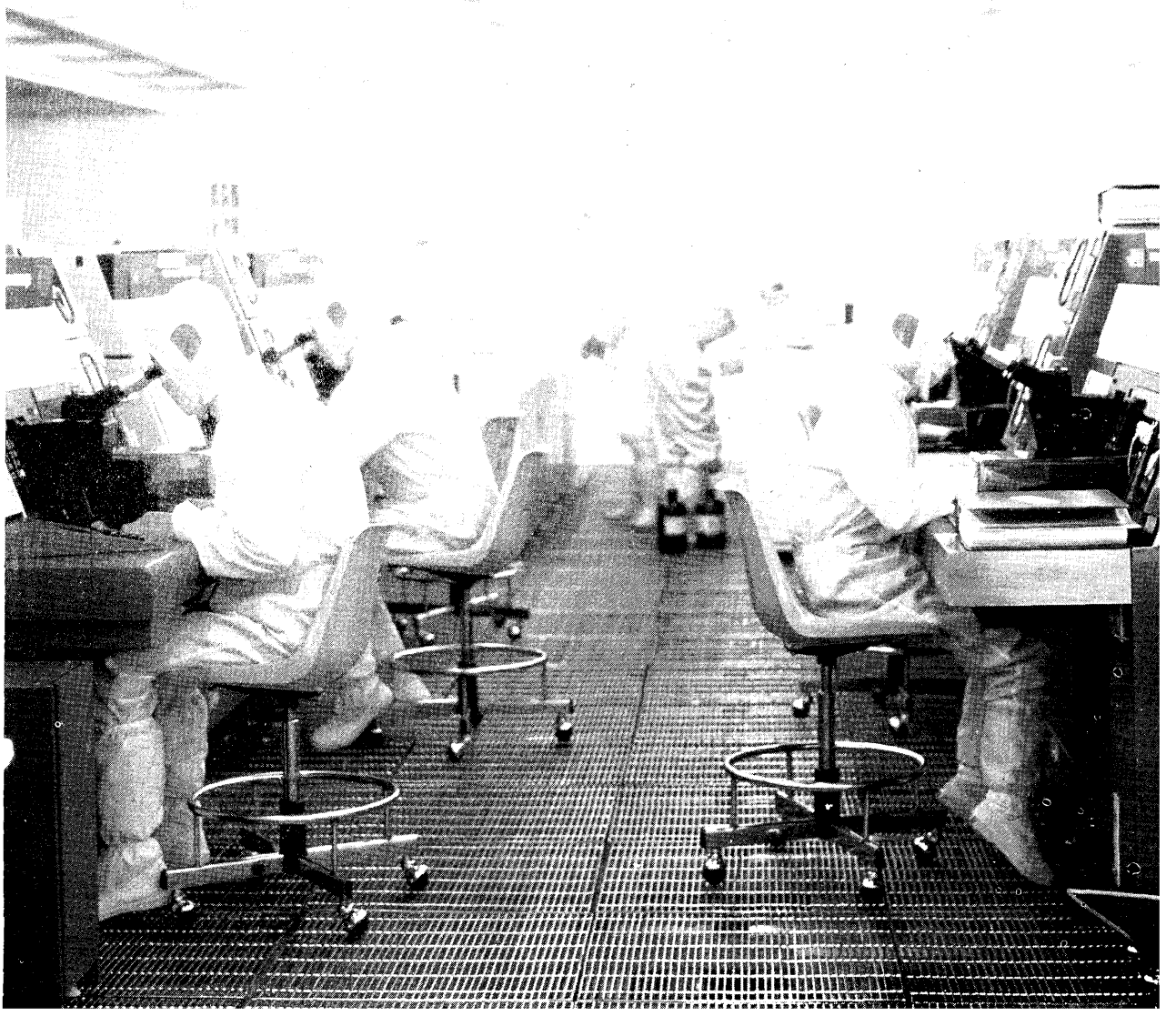


$t_{GTP} = (RpC)\ln(V_{DD}/V_{DD} - V_{TST})$
$t_{GTA} = (R1C)\ln(V_{DD}/V_{TST})$
$Rp = R1R2/(R1 + R2)$
(a) Decreasing t_{GTP}($t_{GTP} < t_{GTA}$)

Figure 6. Guard Time Adjustment

NOTES

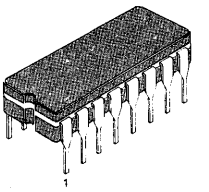
EXCHANGE ICs 4



PCM TRANSMIT/RECEIVE FILTER

The KT3040 PCM CODEC Filter is a monolithic circuit that provides the transmit and receive filtering necessary to interface a voice telephone circuit to a time division multiplexed application in 8KHz sampling system. The device consists of two switched capacitor filters, transmit and receive, and power amplifiers which may be used to drive a transformer hybrid (2 to 4 wire converter) or an electronic hybrid (SLIC). If an electronic hybrid is used, the power amplifiers are not needed and may be deactivated to minimize power dissipation. The transmit filter is a fifth order low pass filter in series with a fourth order high pass filter. It provides a flat band pass filter which will pass frequencies between 200Hz and 3400Hz and provides rejection of the 50/60Hz power line frequency as well as the anti aliasing needed in an 8KHz sampling system. The receive filter is a low pass filter which smooths the voltage steps present in the CODEC output waveform and provides the sin x/x correction necessary to give unity gain in the passband for the CODEC-decoder-and-receive-filter pair.

16 CERDIP



FEATURES

- **Exceeds all D3/D4 and CCITT specifications**
- **Low power consumption: 45 mW (0 dBm0 into 600Ω)**
  30 mW (power amps disabled)
- **Power down mode: 0.5 mW**
- **External gain adjustment, both transmit and receive filters.**
- **Transmit filter includes 50/60Hz rejection**
- **Receive filter includes sin x/x compensation**
- **Direct interface with transformer or electronic telephone hybrids**
- **TTL and CMOS compatible logic**
- **Power supplies: +5V, −5V**
- **All inputs protected against static discharge due to handling**
- **300 mil ceramic package available**

ORDERING INFORMATION

Device	Package	Operating Temperature
†KT3040N	Plastic	−25~+125°C
†KT3040AN	Plastic	
KT3040J	Ceramic	
KT3040AJ	Ceramic	

† Under Development

BLOCK DIAGRAM

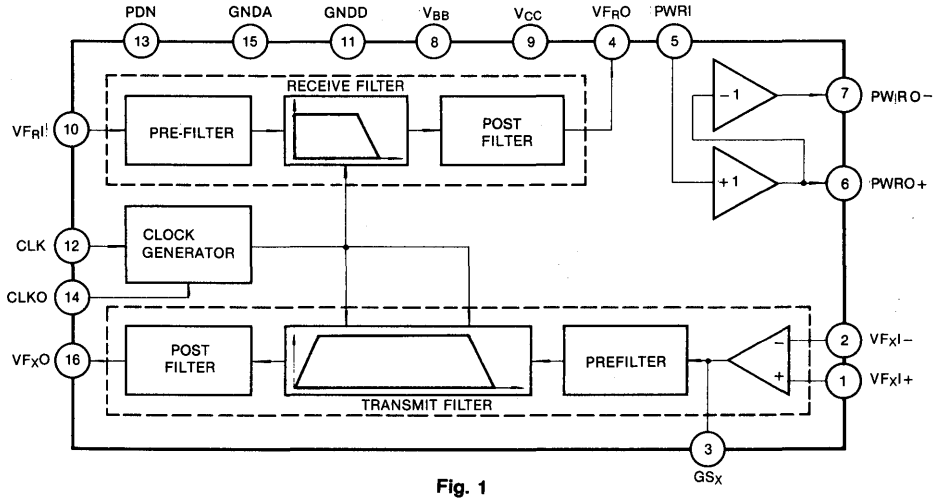
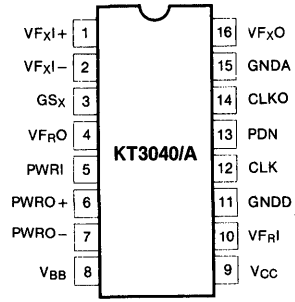


Fig. 1

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltages	V_{CC}, V_{BB}	±7	V
Power Dissipation	P_D	1	W/PKG
Input Voltage	V_{IN}	±7	V
Output Short-Circuit Duration	$T_{S.C\ OUT}$	Continuous	sec
Operating Temperature Range	Ta	−25 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Lead Temperature (Soldering 10 seconds)	T_L	300	°C

DC ELECTRICAL CHARACTERISTICS

(Ta = 0°C to 70°C, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, f_C = 2.048MHz, GNDA = 0V, GNDD = 0V; unless otherwise specified)

Characteristic	Symbol	Test Conditions	KT3040			KT3040A			Unit
			Min	Typ	Max	Min	Typ	Max	
POWER CONSUMPTION									
V_{CC} Standby Current	I_{CC}	PDN = High		50	400		50	100	μA
V_{BB} Standby Current	I_{BB}	PDN = High		50	400		50	100	μA
V_{CC} Operating Current	I_{CC1}	PWRI = V_{BB}, Power amp inactive		3	4		3	4	mA
V_{BB} Operating Current	I_{BB1}	PWRI = V_{BB}, Power amp inactive		3	4		3	4	mA
V_{CC} Operating Current	I_{CC2}	R_L = 600Ω connected between PWRO+ and PWRO−, Input Level = 0 dBm0 (Note 1)		4.6	6.4		4.6	6.4	mA
V_{BB} Operating Current	I_{BB2}	(Note 1)		4.6	6.4		4.6	6.4	mA
DIGITAL INTERFACE									
CLK Input Current	I_{INC}	$V_{BB} \leq V_{IN} \leq V_{CC}$	−10		10	−10		10	μA
PDN Input Current	I_{INP}	$V_{BB} \leq V_{IN} \leq V_{CC}$	−100			−100			μA
CLKO Input Current	I_{INO}	$V_{BB} \leq V_{IN} \leq V_{CC} - 0.5$	−10		0.1	−10		0.1	μA
High Level Input Voltage	V_{IH}	Except CLKO	2.2		V_{CC}	2.2		V_{CC}	V
Low Level Input Voltage	V_{IL}	Except CLKO	0		0.8	0		0.8	V
High Level Input Voltage	V_{IHO}	CLKO Pin	$V_{CC} - 0.5$		V_{CC}	$V_{CC} - 0.5$		V_{CC}	V
Low Level Input Voltage	V_{ILO}	CLKO Pin	V_{BB}		$V_{BB} + 0.5$	V_{BB}		$V_{BB} + 0.5$	V
Input Intermediate Voltage	V_{IIO}	CLKO Pin	−0.8		0.8	−0.8		0.8	V

4

DC ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	KT3040			KT3040A			Unit
			Min	Typ	Max	Min	Typ	Max	
TRANSMIT FILTER GAIN SETTING AMPLIFIER									
V_{FXI} Input Leakage Current	IB_XI	$V_{BB} \leq V_{FXI} \leq V_{CC}$	−100		100	−100		100	nA
V_{FXI} Input Resistance	RI_XI	$V_{BB} \leq V_{FXI} \leq V_{CC}$	10			10			MΩ
V_{FXI} Input Offset Voltage	VOS_XI	$-2.5V \leq V_{IN} \leq +2.5V$	−20		20	−20		20	mV
V_{FXI} Common Mode Range	V_{CM}		−2.5		2.5	−2.5		2.5	V
Common Mode Rejection Ratio	CMRR	$-2.5V \leq V_{IN} \leq 2.5V$	60			60			dB
Power Supply Rejection Ratio of V_{CC} or V_{BB}	PSRR		60			60			dB
Open Loop Output Resistance of GS_X	R_{OL}			1			1		KΩ
Minimum Load Resistance of GS_X	R_{LXI}		10			10			KΩ
Maximum Load Capacitance of GS_X	C_{OL}				100			100	pF
Output Voltage Swing of GS_X	V_{OXI}	$R_L \geq 10K\Omega$	±2.5			±2.5			V
Open Loop Voltage Gain of GS_X	A_{VOL}	$R_L \geq 10K\Omega$	5,000			5,000			V/V
Open Loop Unity Gain Bandwidth of GS_X	f_C			2			2		MHz

AC ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Ta = 25°C. All parameters are specified for a signal level of 0dBm0 at 1KHz. The 0dBm0 level is assumed to be $1.54V_{rms}$ measured at the output of the transmit or receive filter)

Characteristic	Symbol	Test Conditions	KT3040			KT3040A			Unit
			Min	Typ	Max	Min	Typ	Max	
TRANSMIT FILTER (Transmit filter input OP amp set to the non-inverting unity gain mode, with $V_{FXI} = 1.09V_{rms}$ unless otherwise noted)									
Minimum Load Resistance of V_{FXO}	RL_X	$-2.5V < V_{OUT} < 2.5V$ $-3.2V < V_{OUT} < 3.2V$	3 10			3 10			KΩ KΩ
Load Capacitance V_{FXO}	CL_X				100			100	pF
Power Supply Rejection Ratio, V_{FXO}	PSRR1	f = 1KHz, $V_{FXI} = 0V_{rms}$, V_{CC} Pin	30			30			dB
Power Supply Rejection Ratio, V_{FXO}	PSRR2	f = 1KHz, $V_{FXI} = 0V_{rms}$, V_{BB} Pin	35			35			dB
Absolute Gain	G_{AX}	f = 1KHz	2.875	3.0	3.125	2.9	3.0	3.1	dB
Gain Relative to G_{AX}	G_{RX}	Below 50Hz			-35			-35	dB
		50Hz		-41	-35		-41	-35	dB
		60Hz		-35	-30		-35	-30	dB
		200Hz	-1.5		0.05	-1.5		0	dB
		300Hz to 3KHz	-0.15		0.15	-0.125		0.125	dB
		3.3KHz	-0.35		0.03	-0.35		0.03	dB
		3.4KHz	-0.7		-0.1	-0.7		-0.1	dB
		4.0KHz		-15	-14		-15	-14	dB
		4.6KHz and above			-32			-32	dB
Absolute Delay at 1KHz	D_{AX}				230			230	μS
Differential Envelope Delay from 1KHz to 2.6KHz	D_{DX}				60			60	μS
Single Frequency Distortion Products	D_{PX1}				-48			-48	dB
Distortion at Maximum Signal Level	D_{PX2}	Gain = 20dB, R_L = 10K $0.16V_{rms}$, 1KHz Signal Applied to V_{FXI}			-45			-45	dB
Total C Message Noise at V_{FXO}	N_{CX2}	Gain setting OP amp at 20dB Gain		3	6		2	5	dB_{rnco}
Total C Message Noise at V_{FXO}	N_{CX2}	Gain setting OP amp at 20dB Gain		3	6		3	6	dB_{rnco}
Temperature Coefficient of 1KHz Gain	G_{AXT}			0.0004			0.0004		dB/°C
Supply Voltage Coefficient of 1KHz Gain	G_{AXS}	$V_{CC} = 5.0V \pm 5\%$ $V_{BB} = -5.0V \pm 5\%$		0.01			0.01		dB/V

AC ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	KT3040			KT3040A			Unit
			Min	Typ	Max	Min	Typ	Max	
Crosstalk, Rx to Tx $20 \log \frac{V_{FXO}}{V_{FRO}}$	CT_{RX}	Rx filter output = $2.2V_{rms}$ $V_{FXI} = 0V_{rms}$, f = 0.2KHz to 3.4KHz measure V_{FXO}			−70			−70	dB
Gain Tracking Relative to G_{AX}	G_{RXL}	Output Level = +3dBm0 +2dBm0 to −40dBm0 −40dBm0 to −55dBm0	−0.1 −0.05 −0.1		0.1 0.05 0.1	−0.1 −0.05 −0.1		0.1 0.05 0.1	dB dB dB
RECEIVE FILTER (Unless otherwise noted, the receive filter is preceded by a sinx/x filter with an input signal level of $1.54V_{rms}$)									
Input Leakage Current, V_{FRI}	I_{BR}	$-3.2V \leq V_{IN} \leq 3.2V$	−100		100	−100		100	nA
Input Resistance, V_{FRI}	R_{IR}		10			10			MΩ
Output Resistance, V_{FRO}	R_{OR}			1	3		1	3	Ω
Load Capacitance, V_{FRO}	C_{LR}				100			100	pF
Load Resistance, V_{FRO}	R_{LR}		10			10			KΩ
Power Supply Rejection of V_{CC} or V_{BB}, V_{FRO}	PSRR3	V_{FRI} connected to GNDA, f = 1KHz	35			35			dB
Output DC Offset, V_{FRO}	V_{OS}	V_{FRI} connected to GNDA	−200		200	−200		200	mV
Absolute Gain	G_{AR}	f = 1KHz	−0.125		0.125	−0.1		0.1	dB
Gain Relative to Gain at 1KHz	G_{RR}	Below 300Hz 300Hz to 3.0KHz 3.3KHz 3.4KHz 4.0KHz 4.6KHz and above	 −0.15 0.35 −0.7		0.125 0.15 0.03 −0.1 −14 −32	 −0.125 0.35 −0.7		0.125 0.125 0.03 −0.1 −14 −32	dB dB dB dB dB dB
Absolute Delay at 1KHz	D_{AR}				100			100	μS
Differential Envelope Delay 1KHz to 2.6KHz	D_{DR}				100			100	μS
Single Frequency Distortion Products	D_{PR1}	f = 1KHz			−48			−48	dB
Distortion at Maximum Signal Level	D_{PR2}	$2.2V_{rms}$ Input sinx/x filter, f = 1KHz, R_L = 10K			−45			−45	dB
Total C Message Noise at V_{FRO}	N_{CR}			3	5		3	5	dB_{rnco}
Temperature Coefficient of 1KHz Gain	G_{ART}			0.0004			0.0004		dB/°C
Supply Voltage Coefficient of 1KHz Gain	G_{ARS}			0.01			0.01		dB/V

AC ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	KT3040			KT3040A			Unit
			Min	Typ	Max	Min	Typ	Max	
Crosstalk, Transmit to Receive $20 \log \frac{V_{FRO}}{V_{FXO}}$	CT_{XR}	Transmit filter output $= 2.2V_{rms}$, $V_{FRI} = 0V_{rms}$, f = 0.3KHz to 3.4KHz measure V_{FRO}			−70			−70	dB
Gain Tracking Relative to G_{AR}	G_{RRL}	Output level = +3dBmO +2dBmO to −40dBmO −40dBmO to −55dBmO (Note 5)	−0.1 −0.05 −0.1		0.1 0.05 0.1	−0.1 −0.05 −0.1		0.1 0.05 0.1	dB dB dB
RECEIVE OUTPUT POWER AMPLIFIER									
Input Leakage Current, PWRI	I_{BP}	$-3.2V \leq V_{IN} \leq 3.2V$	0.1		3	0.1		3	μA
Input Resistance, PWRI	R_{IP}		10			10			MΩ
Output Resistance, PWRO+, PWRO−	R_{OP1}	Amplifier Active		1			1		Ω
Load Capacitance, PWRO+, PWRO−	C_{LP}				500			500	pF
Gain, PWRI to PWRO+ Gain, PWRI to PWRO−	G_{AP+} G_{AP-}	$R_L = 600\Omega$ connected between PWRO+ and PWRO−, input Level = 0dBm0 (Note 4)		1 −1			1 −1		V/V V/V
Gain Tracking Relative to 0dBm0 Output Level. Including Receive Filter	G_{RPL}	$V = 2.05V_{rms}$, $R_L = 600\Omega$ (Note 4, 5) $V = 1.75V_{rms}$, $R_L = 300\Omega$	−0.1 −0.1		0.1 0.1	−0.1 −0.1		0.1 0.1	dB
Signal/Distortion	S/D_P	$V = 2.05V_{rms}$, $R_L = 600\Omega$ $V = 1.75V_{rms}$, $R_L = 300\Omega$ (Note 4, 5)			−45 −45			−45 −45	dB dB
Output DC Offset PWRO+, PWRO−	V_{OSP}	PWRI connected to GNDA	−50		50	−50		50	mV
Power Supply Rejection Ratio of V_{CC} or V_{BB}	PSRR5	PWRI connected to GNDA	45			45			dB

Note 1: Maximum power consumption will depend on the load impedance connected to the power Amplifier. This specification listed assumes $0dB_m$ is delivered to 600Ω connected from PWRO+ to PWRO−.

Note 2: Voltage input to receive filter at 0V. V_{FRO} connected to PWRI, 600Ω from PWRO+ to PWRO−. Output measured from PWRO+ to PWRO−.

Note 3: The 0dBm0 level for the filter is assumed to be $1.54V_{rms}$ measured at the output of the XMT or RCV filter.

Note 4: The 0dBm0 level for the power amplifiers is load dependent. For $R_L = 600\Omega$ to GNDA, the 0dBm0 level is $1.43V_{rms}$ measured at the amplifier output for $R_L = 300\Omega$ the 0dBm0 level is $1.22V_{rms}$.

Note 5: V_{FRO} connected to PWRI, input signal applied to V_{FRI}.

PIN DESCRIPTION

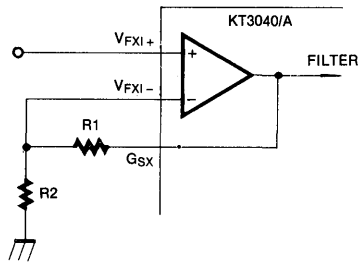
Pin No.	Designation	Function
1	V_{FXI+}	The non-inverting input of the gain adjustment OP amp in the transmit filter. The signal applied to this pin typically comes from the 2 to 4 wire hybrid in the case of a 2 wire line and goes through the frequency rejection and antialiasing filters before being sent to the CODEC for encoding.
2	V_{FXI-}	Inverting input of the gain adjustment operational amplifier on the transmit filter.
3	G_{SX}	Output of the gain adjustment operational amplifier on the transmit filter. Used for gain setting of the transmit filter.
4	V_{FRO}	Analog output of the receive filter. This output is capable of driving high impedance electronic hybrids. The gain of the receive signal may be attenuated by using a resister divider. For a transformer hybrid application, V_{FRO} is tied to PWRI and a dual balanced output is provided on pins PWRO+ and PWRO−.
5	PWRI	Input to the power driver amplifiers on the receive side for interface to transformer hybrids. High impedance input. When tied to V_{BB}, the power amplifiers are powered down.
6	PWRO+	Non-inverting side of the power amplifiers. Power driver output capable of directly driving transformer hybrids.
7	PWRO−	Inverting side of the power amplifiers. Power driver output capable of directly driving transformer hybrids.
8	V_{BB}	The negative power supply pin. The recommended input is −5V.
9	V_{CC}	The positive power supply pin. The recommended input is 5V.
10	V_{FRI}	Analog input of the receive filter, interface to the CODEC analog output for PCM applications. The receive filter provides the sinx/x correction needed for sample and hold types CODEC outputs to give unity gain.
11	GNDD	Digital ground return for internal clock generator.
12	CLK	The master clock input. Three clock frequencies can be used: 1.536MHz, 1.544MHz or 2.048MHz. For proper operation this clock should be tied to the receive clock of the CODEC.
13	PDN	Control input for the stand-by power down mode. Power down occurs when the signal on this input is pulled high. An internal pull up to the positive supply is provided.
14	CLK0	Master clock (pin 12, CLK) frequency selection. If tied to V_{BB}, CLK should be 1.536MHz. If tied to GNDD, CLK should be 1.544MHz. If tied to V_{SS}, CLK should be 2.048MHz. An internal pull up is provided.
15	GNDA	Analog return common to the transmit and receive analog circuits. Not internally connected to GNDD.
16	V_{FXO}	The analog output of the transmit filter. The output voltage range is ±3.2V.

FUNCTIONAL DESCRIPTION

The KT3040/A provides the transmit and receive filters found on the analog termination of a PCM line or trunk. The transmit filter performs the anti-aliasing function needed for an 8KHz sampling system, and the 50/60Hz rejection. The receive filter has a low pass transfer characteristic and also provides the sinx/x correction necessary to interface μ-Law and A-Law CODECs which have a non-return-to zero output of the digital to analog conversion. Gain adjustment is provided in the receive and transmit directions. The KT3040/A can interface directly with a transformer hybrid (2 to 4 wire conversion) or with electronic hybrids.

Transmit Filter

The input stage provides gain adjustment in the passband. The CMOS operational amplifier has a common mode range of ±2.5V, a DC offset of less than ±20mV, a voltage gain greater than 5,000 and a unity gain bandwidth of 2MHz. The load impedance connected to the amplifier output (G_{SX}) must be greater than 10KΩ in parallel with 25pF. The input operational amplifier can also be used in the inverting mode of differential amplifier mode. It can be connected to provide a gain of 20dB without degrading the overall filter performance.



$R1 + R2 \geq 10K\Omega$

$$\text{Input OP Amp Gain} = \frac{R1 + R2}{R2}$$

$$\text{Tx Voltage Gain} = \frac{R1 + R2}{R2} \times \sqrt{2}$$

(The Tx filter itself introduces, a 3dB gain)

The Tx input stage is followed by a prefilter which is a two-pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched capacitor band pass filter. A band pass filter provides rejection of 200Hz or lower noise which may exist in the signal path, and stopband attenuation which exceeds the D3 and D4 specifications as well as the CCITT G712 recommendations.

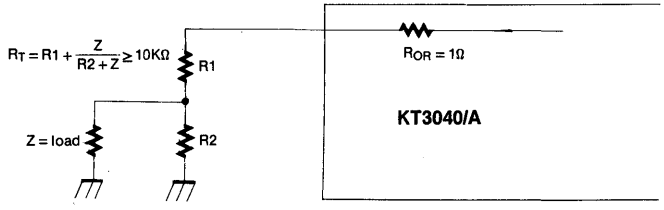
The output stage of the transmit filter, the post filter is also a two pole RC active low pass filter which attenuate clock frequency noise by at least 40dB. The output of the transmit filter is capable of driving a $\pm 3.2V_{p\text{-}p}$ signal into a 10KΩ load in parallel with up to 25pF.

Receive Filter

The Rx input stage is a prefilter which is similar to the Tx prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter provides stopband rejection, sinx/x gain correction and passband flatness.

The receive filter output V_{FRO} lead is capable of driving high impedance electronic hybrids. The gain of the receive section from V_{FRI} to V_{FRO} is $(\pi f/8000)/\text{Sin}(\pi f/8000)$.

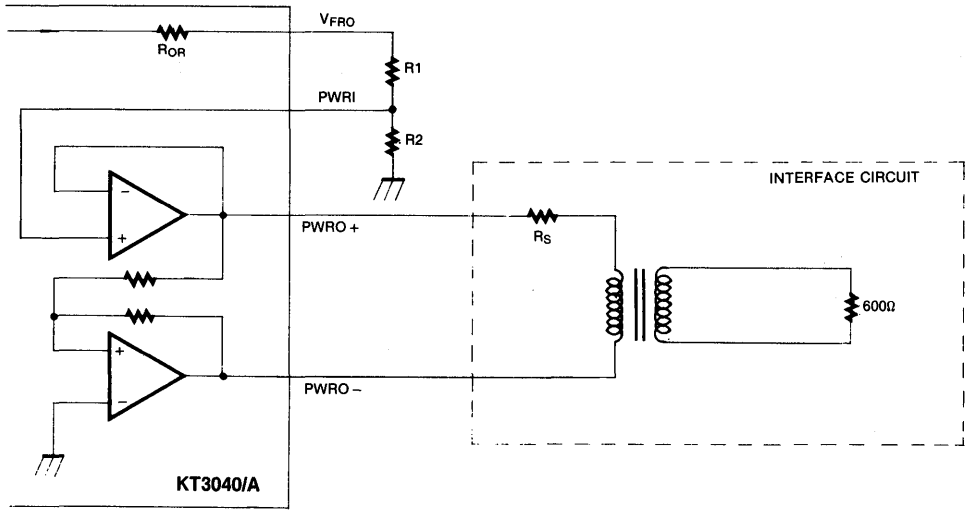
The filter gain can be adjusted downward by a resistor voltage divider as shown below. The total load impedance R_T connected to the filter output (V_{FRO}) must be greater than 10KΩ.



Receive Filter Output Gain Adjustment

Receive Filter Power Amplifier

A balanced power amplifier is provided in order to transformer coupled line circuits. The receive filter output V_{FRO} is connected through gain setting resistors R1 and R2 to the amplifier input PWRI. The input voltage range on PWRI is ± 3.2V. The series combination of R_S and the hybrid transformer must present a minimum AC load resistance of 600Ω to the amplifier in the bridge configuration. A typical connection of the output driver amplifier is shown below.



Typical Connection of Output Driver Amp

The power amps can be deactivated, when not required, by connecting the power amplifier input (pin 5) to the negative power supply V_{BB}. This reduces the total filter power consumption by approximately 10mW-20mW depending on output signal amplitude.

Power Down Mode

Pin 13 (PDN) provides the power down control. When the level on this pin is high, the KT3040/A goes into standby, power down mode. The total filter power consumption will reduce to less than 1mW. This feature allows multiple KT3040/A to drive the same analog bus on a time shared basis. Connect PDN to GNDD for normal operation.

APPLICATION INFORMATION

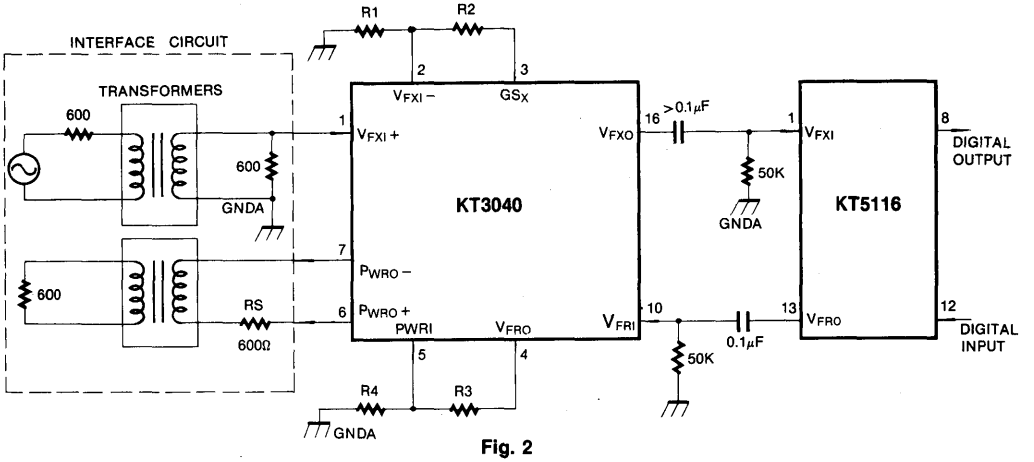


Fig. 2

Note 1: Transmit voltage gain $= \frac{R_1 + R_2}{R_2} \times \sqrt{2}$ (The filter itself introduces a 3dB gain), $(R_1 + R_2 \geq 10K)$

Note 2: Receive Gain $= \frac{R_4}{R_3 + R_4}$ $(R_3 + R_4 \geq 10K)$

Note 3: In the configuration shown, the receive filter amplifiers will drive a 600Ω T to R termination to a maximum signal level of 8.5dBm. An alternative arrangement, using a transformer winding ratio equivalent to 1.414:1 and 300Ω lesistor, R_S, will provide a maximum signal level of 10.1dBm across a 600Ω termination impedance.

Gain Adjust

Fig. 2 shows the signal path interconnections between the KT3040 and KT5116 single-channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

Optimum noise and distortion performance will be obtained from the KT3040 filter when operated with system peak overload voltages of ±2.5 to ±3.2V at V_{FXO} and V_{FRO}. When interfacing to a PCM CODEC with a peak overload voltage outside this range, further gain or attenuation may be required.

For example, the KT3040 filter can be used with the KT3000 series CODEC which has a 5.5V peak overload voltage. A gain stage following the transmit filter output and an attenuation stage following the CODEC output are required.

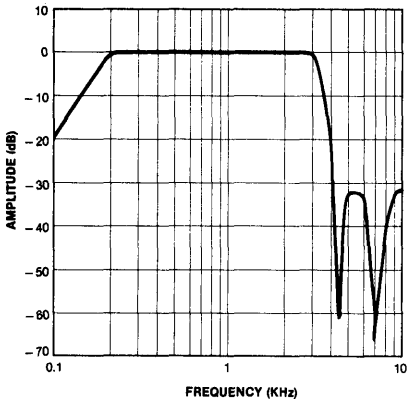
Decoupling Recommendations

PC board decoupling should be sufficient to prevent power supply transients from exceeding the absolute maximum rating of the device. A minimum of 1μF is recommended for each power supply.

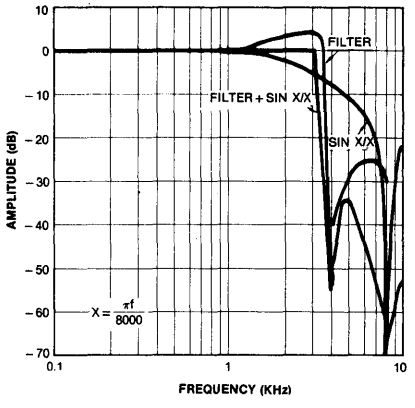
A 0.05μF bypassing capacitor should also be connected from each power supply to GNDA. However, this decoupling may be reduced depending on board design and performance. Ground loops should be avoided.

TYPICAL PERFORMANCE CURVE

TRANSMIT FILTER STAGE



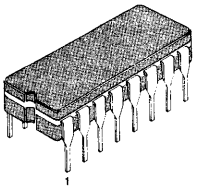
RECEIVE FILTER STAGE



μ-LAW COMPANDING CODEC

The KT5116 is a monolithic CMOS companding CODEC which contains two parts: (1) an analog-to-digital converter (2) a digital to-analog converter which have transfer characteristics conforming to the μ-Law companding code.
These two parts form a coder-decoder function designed to meet the needs of the telecommunications industry for per-channel voice-frequency codes used in telephone digital switching and transmission systems.
Digital input and output are in serial format using sign-plus-amplitude coding.
A sync pulse input is provided for reception of multichannel information being multiplexed and synchronizing transmission over a single transmission line.
Practical transmission and reception of 8bit data words which contain the analog information is done from 64Kb/s to 2.1Mb/s rate with analog signal sampling occuring at an 8KHz rate.

16 CERDIP



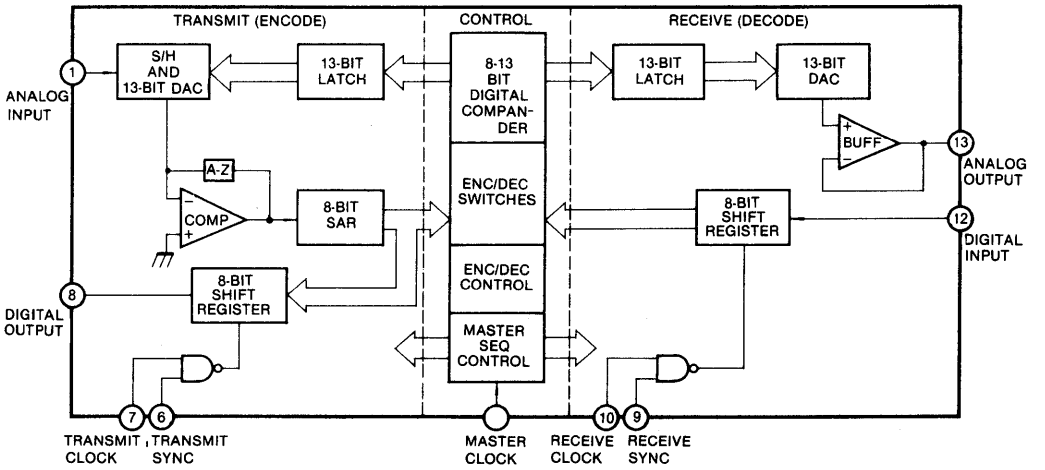
FEATURES

- **The simple ±5V power supply operation**
- **Typically 30mW low power dissipation**
- **Follows the μ-255 companding law**
- **Synchronous and asynchronous operation**
- **On-chip offset null circuit eliminates long term drift, drift error and need for trimming**
- **Minimum external circuitry required**
- **Separate analog and digital grounding pins reduce system noise problems**
- **On-chip sample and hold.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KT5116J	Ceramic	0~70°C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
DC Power Supply	V+ (V−)	+6 (−6)	V
Ambient Operating Temperature	T_a	0 to 70	°C
Storage Temperature	T_s	−55 to 125	°C
Package Dissipation at 25°C	P_D	500	mW
Digital Input Voltage	V_{DI}	−0.5 to 6	V
Analog Input Voltage	V_{AI}	−6 to 6	V
Positive Reference Voltage	V_{ref+}	−0.5 to 6	V
Negative Reference Voltage	V_{ref-}	−6 to 0.5	V

DIGITAL OUTPUT CODE μ-LAW

No	Chord Code	Chord Value	Step Value
1	0 0 0	0.0mV	0.613mV
2	0 0 1	10.11mV	1.226mV
3	0 1 0	30.3mV	2.45mV
4	0 1 1	70.8mV	4.90mV
5	1 0 0	151.7mV	9.81mV
6	1 0 1	313mV	19.61mV
7	1 1 0	637mV	39.2mV
8	1 1 1	1284mV	78.4mV

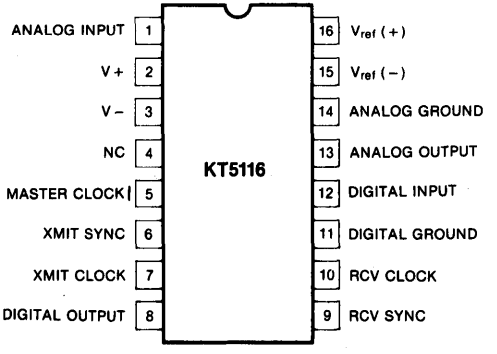
EXAMPLE;

1 011 0010 = +70.8mV+ (2×4.90mV)

sign bit chord step bit = 80.6mV

If the sign bit were a zero, then both plus signs would be changed to minus signs

PIN CONFIGURATION



DC CHARACTERISTICS

(Condition; $V^+ = 5V$, $V^- = -5V$, $V_{ref+} = 2.5V$, $V_{ref-} = -2.5V$)

Parameter	Symbol	Min	Typ	Max	Unit
Analog Input Resistance During Sampling	R_{INAS}		2		KΩ
Analog Input Resistance Non-Sampling	R_{INANS}		100		MΩ
Analog Input Capacitance	C_{INA}		150	250	pF
Analog Input Offset Voltage	V_{offINA}		±1	±8	mV
Analog Output Resistance	R_{OUTA}		1	10	Ω
Analog Output Current	$I_{out/A}$	0.25	0.5		mA
Analog Output Offset Voltage	$V_{off/O}$		±20	±850	mV
Logic Input Low Current ($V_{IN} = 0.8V$) Digital Input, Clock Input, SYNC Input	I_{IL}		±0.1	±10	μA
Logic Input High Current ($V_{IN} = 2.4V$)	I_{IH}		−0.25	−0.8	mA
Digital Output Capacitance	$C_{D/O}$		8	12	pF
Digital Output Leakage Current	I_{DOL}		±0.1	±10	μA
Digital Output Low Voltage	V_{OL}			0.4	V
Digital Output High Voltage	V_{OH}	3.9			V
Positive Supply Current	I^+		4	10	mA
Negative Supply Current	I^-		2	6	mA
Positive Reference Current	I_{ref+}		4	20	μA
Negative Reference Current	I_{ref-}		4	20	μA

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AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Master Clock Frequency	f_m	1.5	1.544	2.1	MHz
RCV, XMIT Clock Frequency	f_r, f_x	0.064	1.544	2.1	MHz
Clock Pulse Width (MASTER, XMIT, RCV)	PW_{CLK}	200			ns
Clock Rise, Fall Time (MASTER, XMIT, RCV)	t_{rc}, t_{fc}			25% of PW_{CLK}	ns
SYNC Rise, Fall Time (XMIT, RCV)	t_{rs}, t_{fs}			25% of PW_{CLK}	ns
SYNC Pulse Width (XMIT, RCV)			$\frac{8}{fx\ (fr)}$		μs
Data Input Rise, Fall Time	t_{DIR}, t_{DIF}			25% of PW_{CLK}	ns
SYNC Pulse Period (XMIT, RCV)	t_{ps}		125		μs
XMIT Clock-to-XMIT SYNC Delay	t_{xcs}	50% of t_{fc} (t_{rs})			ns
XMIT Clock-to-XMIT SYNC (Negative Edge) Delay	t_{xcsn}	200			ns
XMIT SYNC Set-Up Time	t_{xss}	200			ns
XMIT Data Delay	t_{xdd}	0		200	ns
XMIT Data Present	t_{xdp}	0		200	ns
XMIT Data Three State	t_{xdt}			150	ns
Digital Output Fall Time	t_{dof}		50	100	ns
Digital Output Rise Time	t_{dor}		50	100	ns
RCV SYNC-to-RCV Clock Delay	t_{src}	50% t_{rc} (t_{fs})			ns
RCV Data Set-Up Time	t_{rds}	50			ns
RCV Data Hold Time	t_{rdh}	200			ns
RCV Clock-to-RCV SYNC Delay	t_{rcs}	200			ns
RCV SYNC Set-Up Time	t_{rss}	200			ns
RCV SYNC-to-Analog Output Delay	t_{sao}		7		μs
Analog Output Positive Slew Rate	Slew $^+$		1		V/μs
Analog Output Negative Slew Rate	Slew $^-$		1		V/μs
Analog Output Drop Rate	Droop		25		μV/μs

POWER SUPPLY REQUIREMENTS

Parameter	Symbol	Min	Typ	Max	Unit
Positive Supply Voltage	V^+	4.75	5.0	5.25	V
Negative Supply Voltage	V^-	−5.25	−5.0	−4.75	V
Positive Reference Voltage	V_{ref}^+	2.375	2.5	2.625	V
Negative Reference Voltage	V_{ref}^-	−2.625	−2.5	−2.375	V

SYSTEM CHARACTERISTICS

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Signal-to-Distortion	Analog Input: 0 ~ −30dBm0 Analog Input: −40dBm0 Analog Input: −45dBm0	S/D	35 29 24	39 34 29		dB dB dB
Gain Tracking	Analog Input: +3 ~ −37dBm0 Analog Input: −37 ~ −50dBm0 Analog Input: −50 ~ −55dBm0	GT		±0.1 ±0.1 ±0.2	±0.4 ±0.8 ±2.5	dB dB dB
Idle Channel Noise	Analog Input = 0V	N_{IC}		10	18	dBrnc0
Transmission Level Point	600Ω	T_{LP}		+4		dB

PIN DESCRIPTION

1. Analog Input (Pin 1)

At this pin, employs voice-frequency analog signals which are bandwidth-limited to 4KHz. Then, they are sampled at an 8KHz rate. The Analog Input must remain between V_{ref} (+) and V_{ref} (−) for accurate conversion.

2. Positive Supply Voltage and Negative Supply Voltage (Pin 2, 3)

Pin 2, 3 is a pin which employs supply voltage. Typically, the voltages of these pins are ±5V.

3. NC (Pin 4)

This is a non-connection pin.

4. Master Clock (Pin 5)

This signal provides the basic timing and control signals required for all internal conversions. It is not necessary for synchronizing with RCV SYNC, RCV Clock, XMIT SYNC or XMIT Clock. It is not internally related to them.

5. XMIT SYNC (Pin 6)

This input is synchronized with XMIT Clock. If XMIT SYNC goes High, the Digital Output is activated and the A/D conversion begins on the next positive edge of Master Clock. Otherwise, if XMIT SYNC goes Low, the Digital Output become 3 state. XMIT SYNC must go Low for at least 1 Master Clock prior to the transmission of the next digital word.

6. XMIT Clock (Pin 7)

The on-chip 8-bit output shift register of the KT5116 is unloaded at the clock rate present on this pin. Clock rates of 64KHz to 2.1MHz can be used for XMIT Clock. When the positive edge of XMIT SYNC occurs after the positive edge of XMIT Clock, XMIT SYNC will determine when the first positive edge of the internal clock will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

7. Digital Output (Pin 8)

The Digital Output is composed of a sign bit, 3 chord bits and 4 step bits. The sign bit indicates the polarity of the Analog Input while the chord and step bits indicate the magnitude. The KT5116 output register stores the 8 bit encoded sample of the Analog Input. The 8 bit-word is shifted out under control of XMIT SYNC and XMIT CLOCK. If XMIT SYNC is Low, the Digital Output is an open circuit, otherwise when XMIT SYNC is High, the state of the Digital Output is determined by the value of the output bit in the serial shift register.

8. RCV SYNC (Pin 9): Refer to Figure 3

This input is synchronized with RCV CLOCK, and serial data is clocked in by RCV CLOCK. Duration of the RCV pulse is approximately eight RCV Clock periods. The conversion from digital to analog starts after the negative edge of RCV SYNC pulse (see Fig. 6). The negative edge of RCV SYNC should occur before the 9th positive clock edge to insure that only eight bits are clocked in. RCV SYNC must stay low for 17 Master Clocks (minimum) before the digital word is to be received (see Fig. 11).

9. RCV Clock (Pin 10): Refer to Figure 3

Valid data should be applied to the digital input before the positive edge of the internal clock. (refer to Fig. 3) This SYNC pulse is approximately eight RCV CLOCK periods. The conversion from digital to analog starts after the negative the internal clock transfers the data to the slave of the master-slave flip-flop. A hold time, t_{rdh}, is required to complete this transfer. If the rising edge of RCV SYNC occurs after the first rising edge of RCV occurs after the first rising edge of RCV CLOCK, RCV SYNC will determine when the first positive edge of internal clock will occur. In this event, the set-up and hold times for the first clock pulse should be measured from the positive edge of RCV SYNC.

10. Digital Ground (Pin 11)

11. Digital Input (Pin 12)

The KT5116 input register accepts the 8-bit sample of an analog value and loads it under control of RCV SYNC and RCV CLOCK (refer to Figure 3). When RCV SYNC goes High, the KT5116 uses RCV CLOCK to clock to clock the serial data into its input register RCV SYNC goes Low to indicate the end of serial input data. The eight bits of the input data have the same functions described for the Digital Output.

12. Analog Output (Pin 13)

The Analog Output is in the form of voltage steps (100% duty cycle) having amplitude equal to the analog sample which was encoded. This wave form is then filtered with an external low-pass filter with sin x/x correction to recreate the sample voice signal.

13. Analog Ground (Pin 14)

14. Positive and Negative Reference Voltages, (Pin 15, 16) V_{ref} (−), V_{ref} (+)

These inputs provide the conversion reference for the digital-to-analog converter in the KT5116. V_{ref} (+) and V_{ref} (−) must maintain 100ppm/°C regulation over the operating temperature. Variation of the reference directly affects system again.

RECOMMENDED ANALOG INPUT CIRCUIT

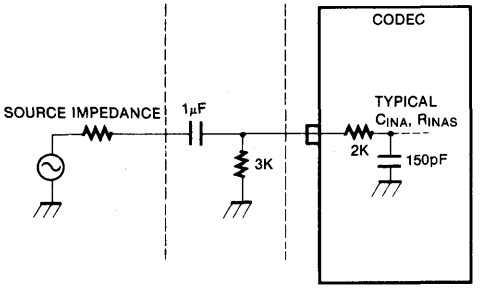


Fig. 1

TRANSMITTER SECTION TIMING

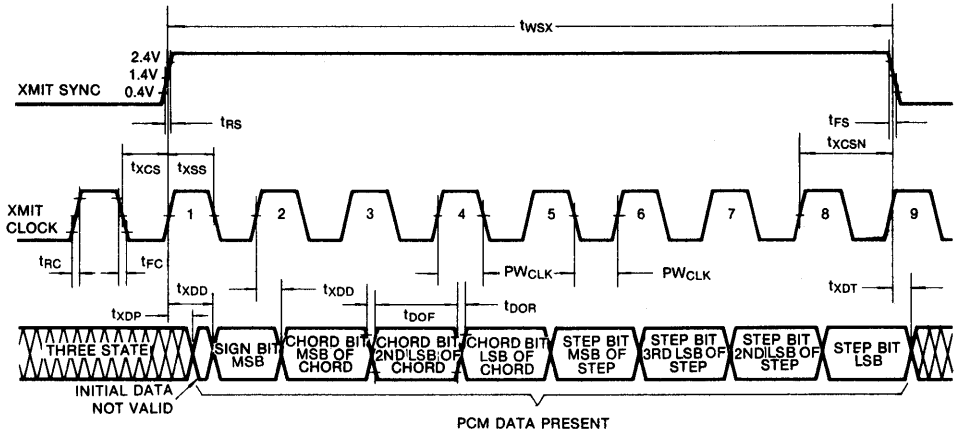


Fig. 2

RECEIVER SECTION TIMING

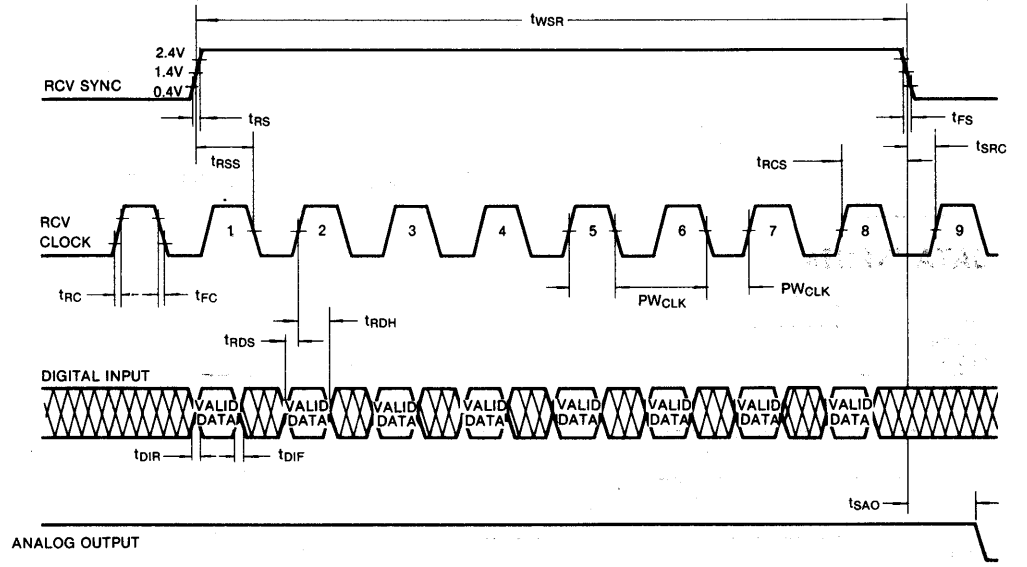


Fig. 3

Note: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

Fig. 4 S/D RATIO VS INPUT LEVEL

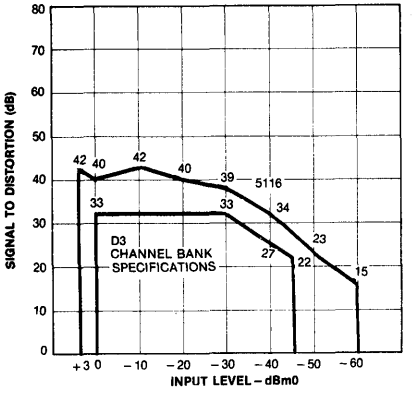
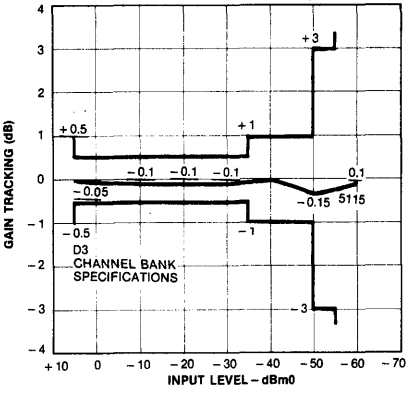


Fig. 5 GAIN TRACKING PERFORMANCE



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A/D, D/A CONVERSION TIMING

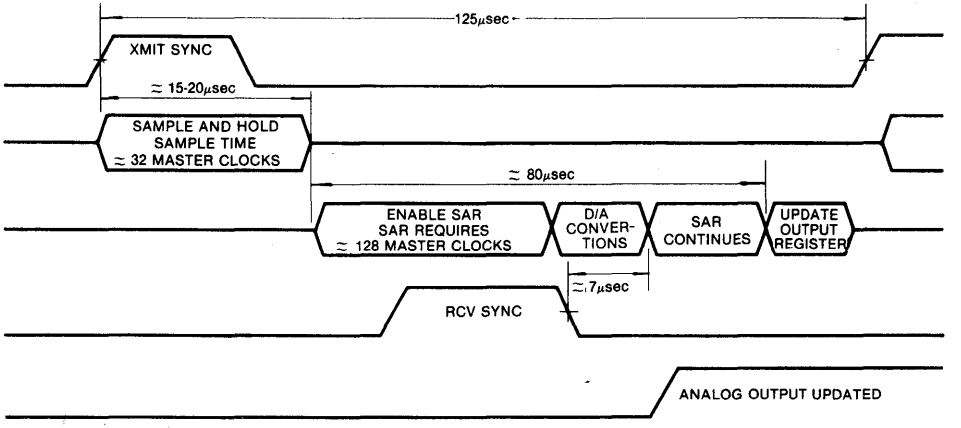
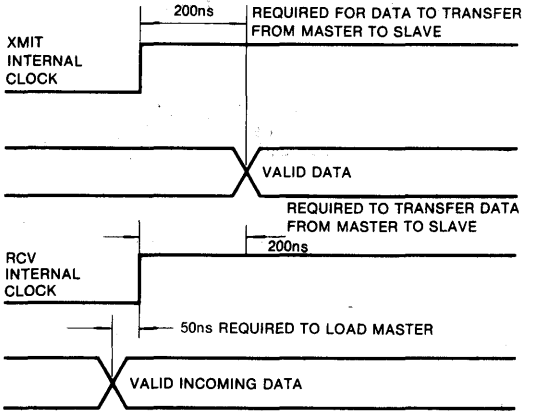


Fig. 6

DATA INPUT/OUTPUT TIMING



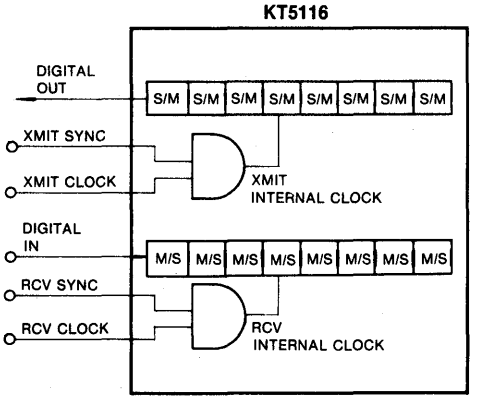


Fig. 7

A/D CONVERTER (μ-Law Encoder) TRANSFER CHARACTERISTIC

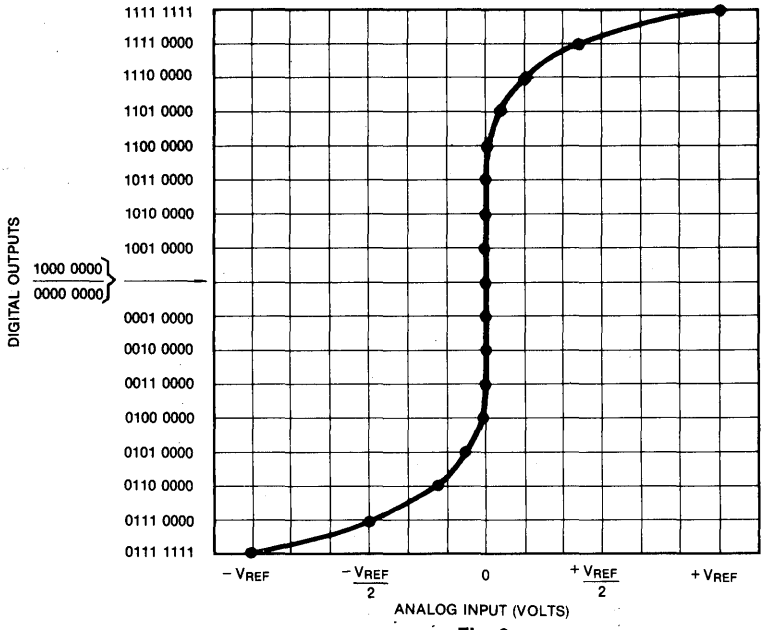


Fig. 8

D/A CONVERTER (μ-Law Decoder) TRANSFER CHARACTERISTIC

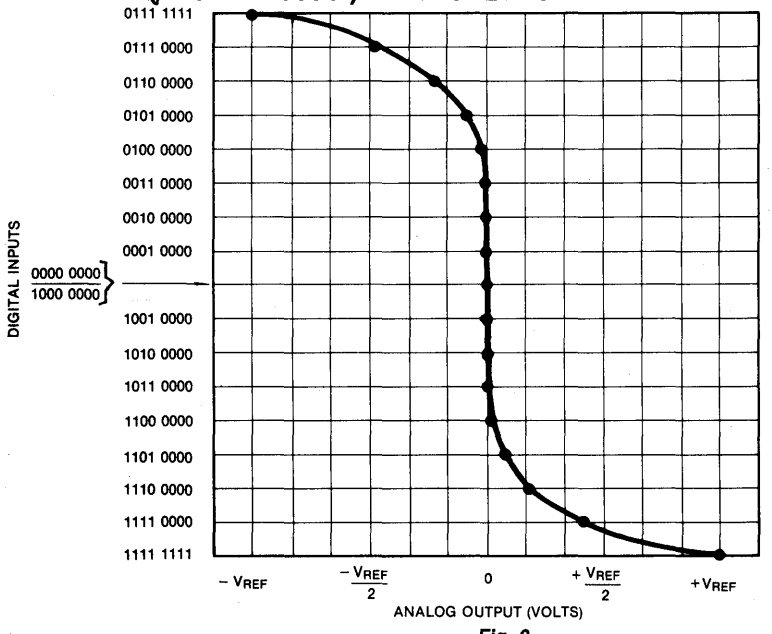


Fig. 9

64KHz OPERATION, TRANSMITTER SECTION TIMING

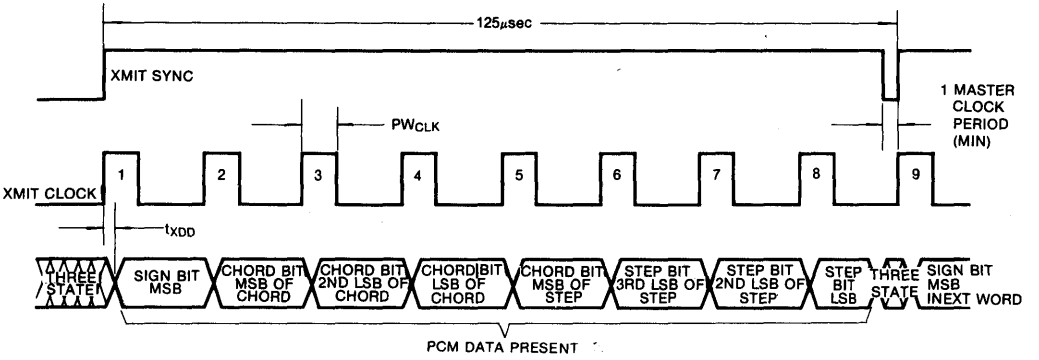


Fig. 10

Note: All rise and fail times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

64KHz OPERATION, RECEIVER SECTION TIMING

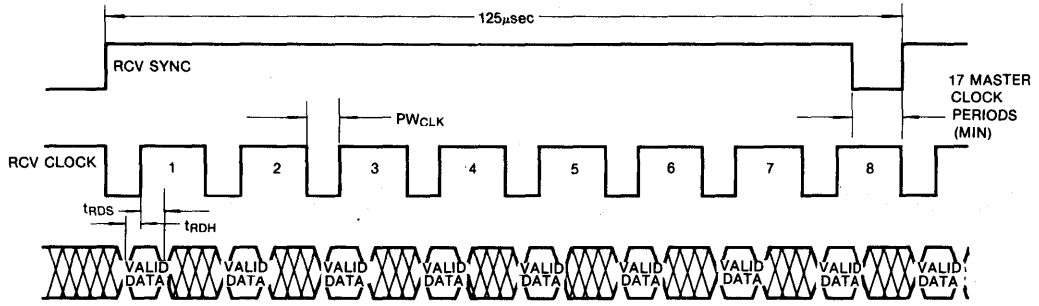
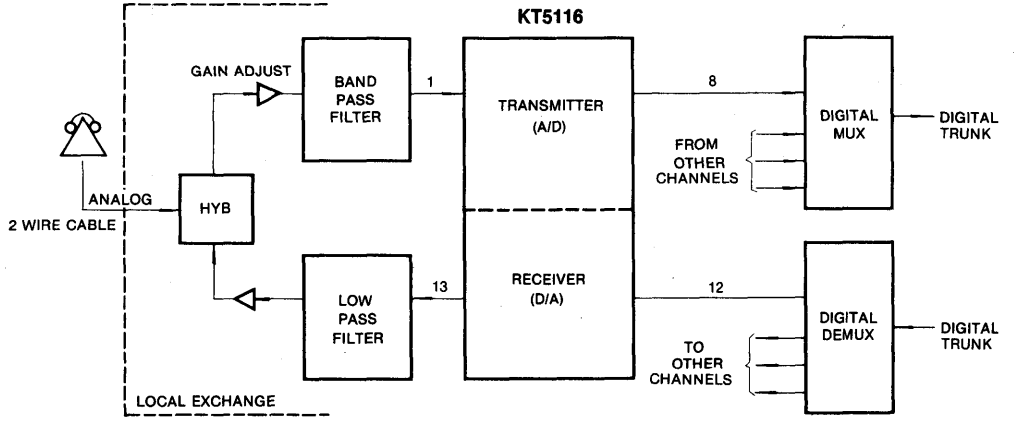


Fig. 11

Note: All rise and fail times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

PCM SYSTEM BLOCK DIAGRAM



SYSTEM CHARACTERISTICS TEST CONFIGURATION

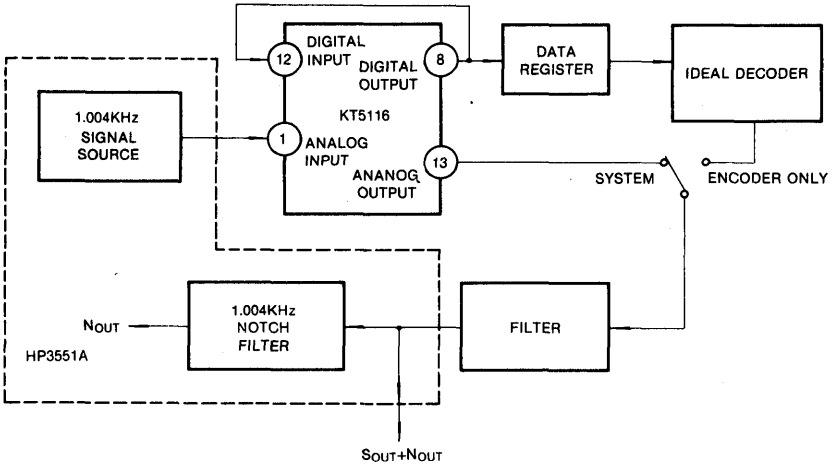


Fig. 12

Note: The ideal decoder consists of a digital decomponder and a 13-bit precision DAC.

PERFORMANCE EVALUATION

The equipment connections shown in Figure 12 can be used to evaluate the performance of the KT5116. An analog signal provided by the HP3551 a transmission test set is connected to the Analog Input (Pin 1) of the KT5116. The Digital Output of the CODEC is tied back to the Digital Input and the Analog Output is fed through a low-pass filter to the HP3551A.

Remaining pins of the KT5116 are connected as follows:

1. RCV SYNC is tied to XMIT SYNC.
2. XMIT CLOCK is tied to Master CLOCK. The signal is inverted and tied to RCV clock.

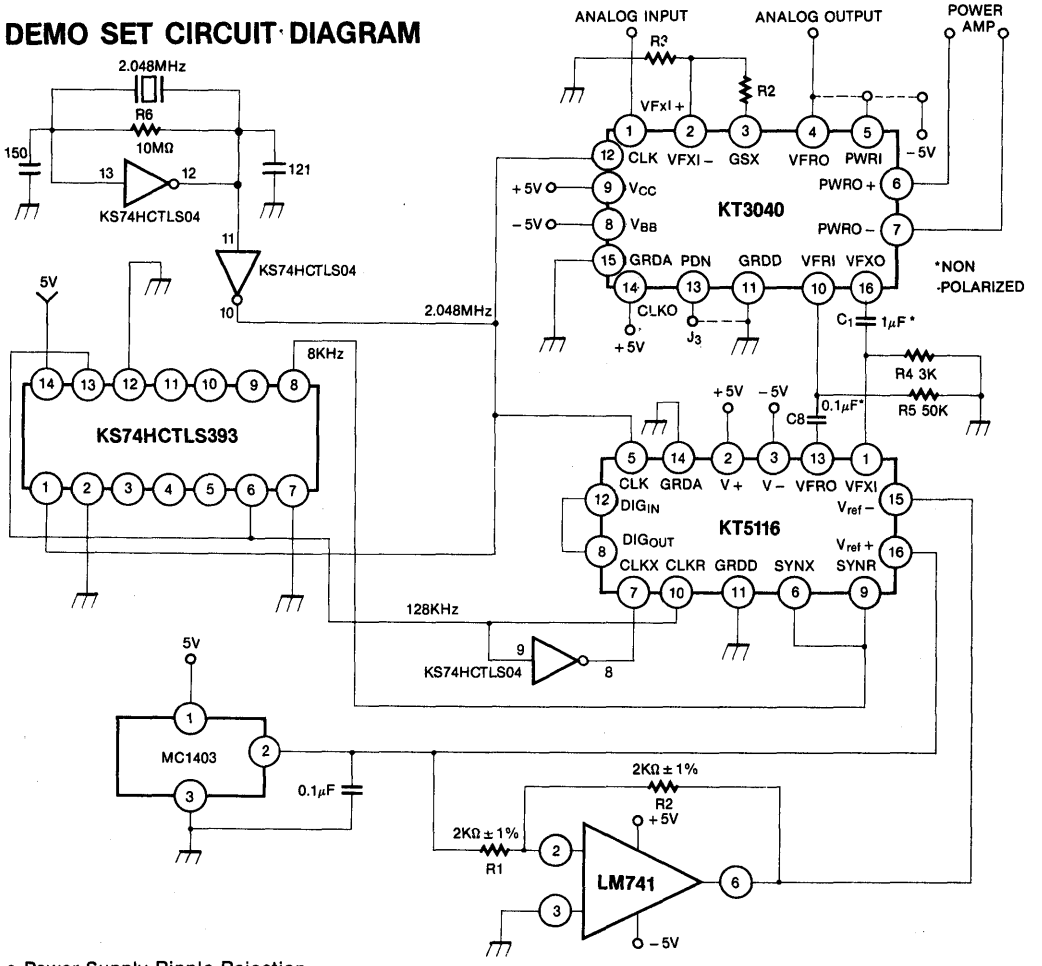
The following timing signals are required:

1. Master CLOCK=2.048MHz
2. XMIT SYNC repetition rate=8KHz
3. XMIT SYNC width=8 XMIT CLOCK periods.

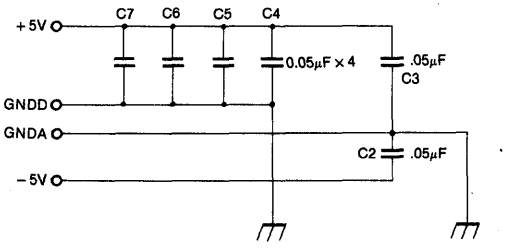
when all the above requirements are met, the set-up of Figure 12 permits the measurement of synchronous system performance over a wide range of Analog Inputs.

The data register and ideal decoder provide a means of checking the encoder portion of the KT5116 independently of the decoder section. To test the system in the asynchronous mode, Master CLOCK should be separated from RCV CLOCK. XMIT CLOCK and RCV CLOCK are separated also.

DEMO SET CIRCUIT DIAGRAM



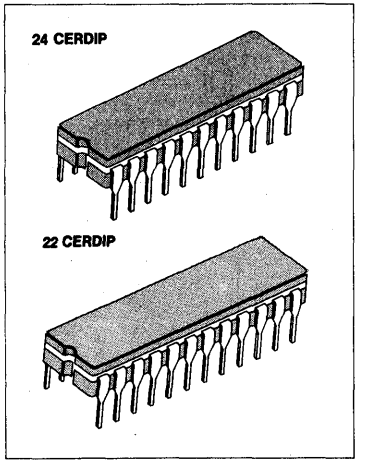
• Power Supply Ripple Rejection



NOTE: All unused input connected to GNDD or V_{CC}, only in HCT series.

MONOLITHIC CODECS

The devices are monolithic PCM CODECs implemented with high reliability CMOS technology. The KT8520 is intended for μ-law applications and the KT8521 is intended for A-law applications.
Integrated into the CODECs are circuits for signaling interface, PCM time-slot control logic, analog-to-digital (A/D) conversion, and digital-to-analog (D/A) conversion. The devices are intended to be used with the KT3040 monolithic PCM filter which provides the input anti-aliasing function for the encoder and smoothes the output of the decoder and corrects for the sinx/x distortion introduced by the decoder sample and hold output.



FEATURES

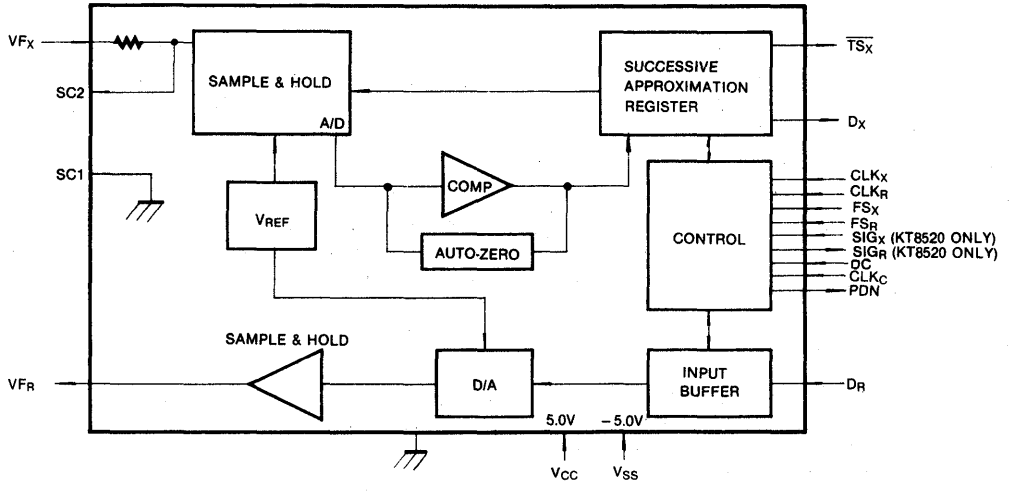
- **Low power consumption: 45 mW (operation)**
  1 mW (standby)
- **$\pm$5V power supplies.**
- **TTL compatible digital inputs and outputs**
- **Optional programmable time slot selection**
- **Internal sample and hold capacitors, auto zero circuit**
- **KT8520: μ-law, 24 DIP**
- **KT8521: A-law, 22 DIP**
- **Synchronous or asynchronous operation**

ORDERING INFORMATION

Device	Package	Operating Temperature
†KT8520N	Plastic	−25~ +125°C
†KT8521N	Plastic	
KT8520J	Ceramic	
†KT8521J	Ceramic	

† Under Development

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
V_{CC}	V_{CC}	7	V
V_{BB}	V_{BB}	−7	V
Any Analog Input or Output	Analog I/O	V_{BB} − 0.3 to V_{CC} + 0.3	V
Any Digital Input or Output	Digital I/O	GND − 0.3 to V_{CC} + 0.3	V
Operating Temperature Range	Ta	−25 ~ +125	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C
Lead Temperature (Soldering, 10 secs)	T_L	300	°C

4

DC ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V_{CC} = 5.0V ± 5%, V_{BB} = −5.0V ± 5%, Ta = 0°C to 70°C, typical characteristics specified at V_{CC} = 5.0V, V_{BB} = −5.0V, Ta = 25°C. All signals referenced to GND.)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
POWER DISSIPATION						
Operating Current, V_{CC}	I_{CC1}			4.5	8.0	mA
Operating Current, V_{BB}	I_{BB1}			4.5	8.0	mA
Standby Current, V_{CC}	I_{CCO}			0.1	0.4	mA
Standby Current, V_{BB}	I_{BBO}			0.03	0.1	mA
DIGITAL INTERFACE						
Input Current	I_I	$0 < V_{IN} < V_{CC}$	−10		10	μA
Input Low Voltage	V_{IL}				0.6	V
Input High Voltage	V_{IH}		2.2			V
Output Low Voltage	V_{OL}	D_X, I_{OL} = 4.0mA SIG_R, I_{OL} = 0.5mA $\overline{TS}_X$, I_{OL} = 3.2mA, Open Drain PDN, I_{OL} = 1.6mA			0.4 0.4 0.4 0.4	V V V V
Output High Voltage	V_{OH}	D_X, I_{OH} = 6.0mA SIG_R, I_{OH} = 0.6mA	2.4 2.4			V V
ANALOG INTERFACE						
VFX Input Impedance when Sampling	Z_I	Resistance in series with 70pF	2.0			KΩ
Output Impedance at VFR	Z_O	−3.1V < VFR < 3.1V		10	20	Ω
Output Offset Voltage at VFR	V_{OS}	DR = PCM Zero Code (KT8520) or Alternating ± 1 Code (KT8521)	−25		25	mV
Analog Input Bias Current	I_{IN}	V_{IN} = 0V	−0.1		0.1	μA
DC Blocking Time Constant	R1·C1		4.0			mS
Input Bias Resistor	R1				160	KΩ
DC Blocking Capacitor	C1		0.1			μF

AC ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, the analog input is a 0dBm0, 1.02KHz sine wave. $V_{CC} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$, $Ta = 0°C$ to $70°C$, typical characteristics specified at $V_{CC} = 5.0V$, $V_{BB} = -5.0V$, $Ta = 25°C$. All signals referenced to GND.)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Absolute Transmit Gain	G_{XA}	$V_{CC} = 5V$, $V_{BB} = -5V$, $T = 25°C$	−0.375		−0.025	dB
Absolute Transmit Gain Variation with Temperature	G_{XAT}	$T = 0°C$ to $70°C$	−0.05		0.05	dB
Absolute Transmit Gain Variation with Supply Voltage	G_{XAV}	$V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$	−0.07		0.07	dB
Absolute Receive Gain	G_{RA}	$V_{CC} = 5V$, $V_{BB} = -5V$, $T = 25°C$	−0.175		0.175	dB
Absolute Receive Gain Variation with Temperature	G_{RAT}	$T = 0°C$ to $70°C$	−0.05		0.05	dB
Absolute Receive Gain Variation with Supply Voltage	G_{RAV}	$V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$	−0.07		0.07	dB
Absolute Receive & Transmit Gain Variation with Level	G_{RAL} G_{XAL}	CCITT Method 2 Relative to −10dBm0 0dBm0 to 3dBm0 −40dBm0 to 0dBm0 −50dBm0 to −40dBm0 −55dBm0 to −50dBm0	 −0.3 −0.2 −0.4 −1.0		 0.3 0.2 0.4 1.0	 dB dB dB dB
Receive & Transmit Signal to Distortion Ratio	S/D_R S/D_X	Sinusoidal Test Method Input Level −30dBm0 to 0dBm0 −40dBm0 −45dBm0	 35 29 25			 dBc dBc dBc
Idle Channel Noise, Receive	N_R	DR = Steady State PCM Code			6	$dB_{mc}0$
Idle Channel Noise, Transmit	N_X	No Signaling (KT8520) Note 1 (KT8521)			13 −66*	$dB_{mc}0$ dBnOp
Receive & Transmit Harmonic Distortion	HD_R HD_X	2nd or 3rd Harmonic			−47	dB
Transmit Positive Power Supply Rejection	$PPSR_X$	Input Level = 0V, $V_{CC} = 5.0V_{dc}$ + $300mV_{rms}$, f = 1.02KHz	50			dB
Receive Positive Power Supply Rejection	$PPSR_R$	D_R = Steady PCM Code $V_{CC} = 5.0V_{dc} + 300mV_{rms}$, f = 1.02KHz	40			dB
Transmit Negative Power Supply Rejection	$NPSR_X$	Input Level = 0V, $V_{BB} = -5.0V_{dc}$ + $300mV_{rms}$, f = 1.02KHz	50			dB

AC ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Receive Negative Power Supply	$NPSR_R$	D_R = Steady PCM Code $V_{BB} = -5.0V_{dc} + 300mV_{rms}$ f = 1.02KHz	45			dB
Transmit to Receive Crosstalk	CT_{XR}	D_R = Steady PCM Code			−75	dB
Receive to Transmit Crosstalk	CTR_X	Transmit Input Level = 0V KT8520 KT8521 (Note 2)			 −70 −65	 dB dB

Note 1: Measured by extrapolation from the distortion test result at −50dBm0 level.
Note 2: Theoretical worst-case for a perfectly zeroed encoder with alternating sign bit, due to the decoding law.

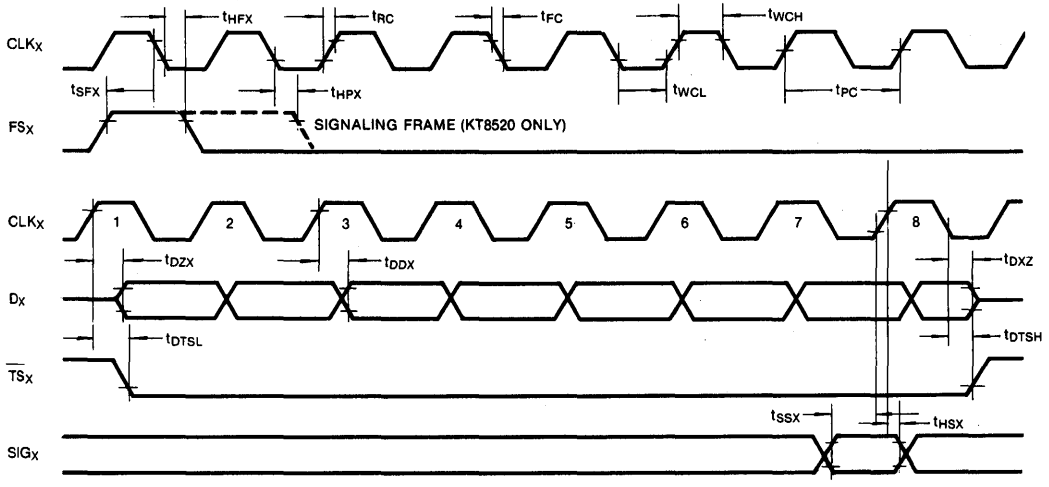
TIMING CHARACTERISTICS

(Unless otherwise noted, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, Ta = 0°C to 70°C, typical characteristics specified at $V_{CC} = 5.0V$, $V_{BB} = -5.0V$, Ta = 25°C. All signals referenced to GND. All timing parameters are measured at $V_{OH} = 2.0V$, $V_{OL} = 0.7V$.)

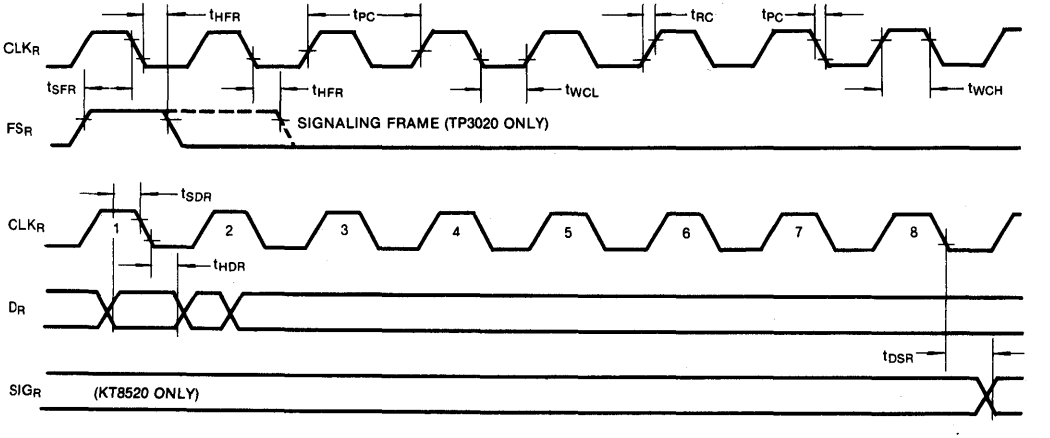
Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Clock Period	t_{PC}	CLK_C, CLK_R, CLK_X	485			nS
Clock Rise and Fall Time	t_{RC}, t_{FC}	CLK_C, CLK_R, CLK_X			30	nS
Clock Pulse Width (High, Low)	$t_{WCH/L}$	CLK_C, CLK_R, CLK_X	165			nS
A/D Conversion Time	$t_{A/D}$	From end of encoder time Slot to completion of conversion			16	Time Slots
D/A Conversion Time	$t_{D/A}$	From end of decoder time Slot to transition of VF_R			2	Time Slots
D_C to CLK_C Set-Up Time	t_{SDC}		100			nS
CLK_C to D_C Hold Time	t_{HDC}		100			nS
FS_X to CLK_X Set-Up Time	t_{SFX}		100			nS
CLK_X to FS_X Hold Time	t_{HFX}		100			nS
Delay Time to Enable D_X on TS Entry	t_{DZX}	$C_L = 150pF$	25		125	nS
Delay Time, CLK_X to D_X	t_{DDX}	$C_L = 150pF$			125	nS
Delay Time, D_X to High Impedance State on TS Exit	t_{DXZ}	$C_L = 0pF$	50		165	nS
Delay to $\overline{TS}_X$ Low	t_{DTSL}	$0 \leq C_L \leq 150pF$	30		185	nS
Delay to $\overline{TS}_X$ Off	t_{DTSH}	$C_L = 0pF$	30		185	nS
Delay Time, CLK_R to SIG_R	t_{DSR}	$C_L = 100pF$			300	nS
SIG_X to CLK_X Set-Up Time	t_{SSX}		100			nS
CLK_X to SIG_X Hold Time	t_{HSX}		100			nS
FS_R to CLK_R Set-Up Time	t_{SFR}		100			nS
CLK_R to FS_R Hold Time	t_{HFR}		100			nS
D_R to CLK_R Set-Up Time	t_{SDR}		40			nS
CLK_R to D_R Hold Time	t_{HDR}		30			nS

TIMING DIAGRAM

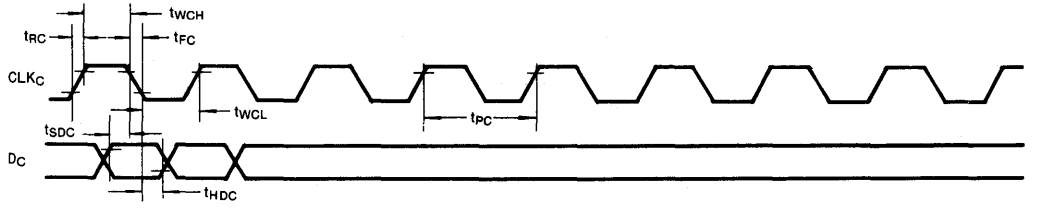
TRANSMIT TIMING



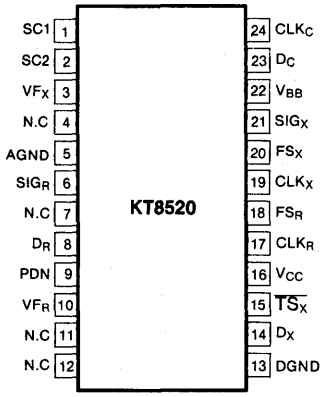
RECEIVE TIMING

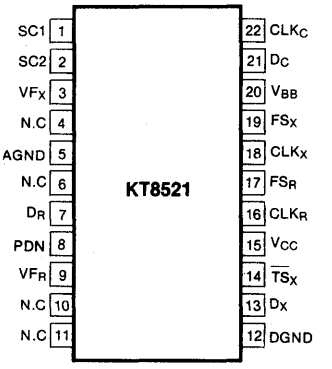


CONTROL TIMING



PIN CONFIGURATION





PIN DESCRIPTION

Name	Function
SC1	Internally connected to GNDA.
SC2	Connects VF_X to an external sample/hold capacitor if fitted for use with pin-compatible NMOS CODECs. Ensures gain compatibility.
VF_X	Analog input to be encoded into a PCM word. The signal in this pin is sampled at the end of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
NC	No connect. Recommended practice is to strap the NC pin to GND.
A/D GND	Analog & Digital ground. All analog & digital signals are referenced to this pin.
SIG_R	Receive signaling bit output. During receive signaling frames the LSB (Least Significant Bit) shifted into D_R is internally latched and appears at this output-SIG_R will then remain valid until changed during a subsequent receive signaling frame or reset by a power-down command.
D_R	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into D_R, MSB (most significant bit) first, on the falling edge of CLK_R.
PDN	Power down output is active high when the CODEC is in the power down state. The open drain output is capable of sinking one TTL load.
VF_R	Analog output.
D_X	Serial PCM output from the encoder (Three-state output). During the encoder time slot, the PCM code for the previous sample of VF_X is shifted out, MSB first, on the rising edge of CLK_X.
$\overline{TS_X}$	Time slot output. (TTL compatible open drain). This output pulses low during the encoder time slot.
V_{CC}	+5V ± 5%, referenced to GND.
CLK_R	Master decoder clock input. This input used to shift in the PCM data on D_R and to operate the decoder sequencer. Operating at 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with CLK_X or CLK_C.

PIN DESCRIPTION (Continued)

Name	Function
FS_R	Decoder frame synchronous pulse. Normally occurring at an 8KHz rate, this pulse is nominally one CLK_R cycle wide. Extending the width of FS_R to two or more cycles of CLK_R signifies a receive signaling frame.
CLK_X	Master encoder clock input. This input used to shift out the PCM data on D_X and to operate the encoder sequencer. Operating at 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with CLK_R or CLK_C.
FS_X	Encoder frame synchronous pulse. Normally occurring at an 8KHz rate, this pulse is nominally one CLK_X cycle wide. Extending the width of FS_R to two or more cycles of CLK_X signifies a transmit signaling frame.
SIG_X	Transmit signaling input. During a transmit signaling frame, the signal at SIG_X is shifted out of D_X in place of the last bit of PCM data.
V_{BB}	$-5V \pm 5\%$, referenced to GND.
DC	Serial control data input. Serial data on D_C is shifted into the CODEC on the falling edge of CLK_C. In the fixed time slot mode, D_C doubles as a power down input.
CLK_C	Control clock input used to shift serial control data into D_C. CLK_C must pulse 8 times during a period of time less than or equal to one frame time, although the 8 pulses may overlap a frame boundary. CLK_C need not be synchronous with CLK_X or CLK_R. Connecting this pin continuously high, the CODEC, into the fixed time slot mode.

FUNCTIONAL DESCRIPTION

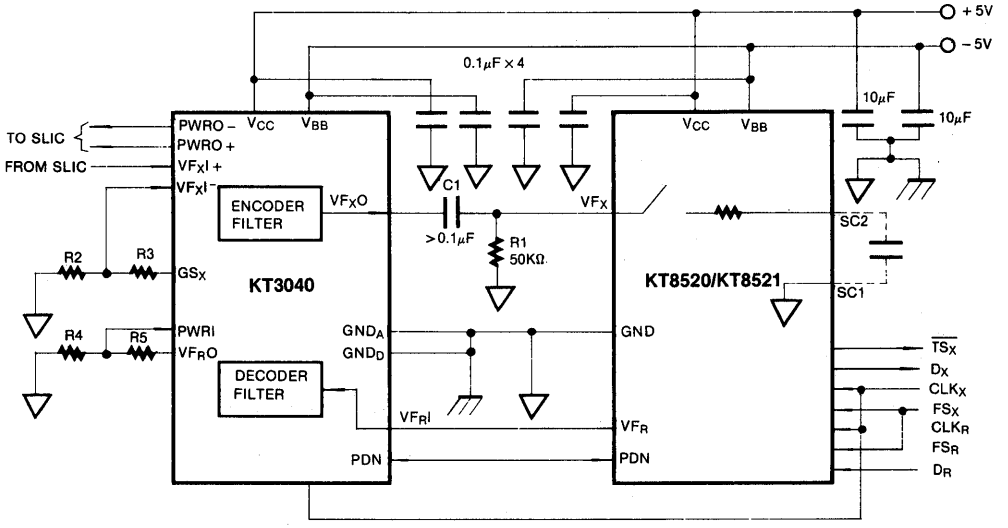
The CODECs are capable of operating as transmitters and receivers in any of the 64 channels of a PCM system. The receive and transmit sections can be assigned to the same channel (time slot) or to different channels, and assignments can be changed under microcomputer control to meet changing system needs. Table 1 shows the control options.

<table>
<tr><th>Control
CLK_C</th><th>Signals
DC</th><th>Operation</th></tr>
<tr><td>L</td><td>X</td><td>Undefined operation</td></tr>
<tr><td>V_{CC}</td><td>H</td><td>Power-down or standby operational status</td></tr>
<tr><td>V_{CC}</td><td>L</td><td>Direct-control operation. Receive and transmit in the first time slot.</td></tr>
<tr><td>↓</td><td>X</td><td>Microcomputer-control operation. Clock in one of 8 bits of the control word at the D_C input.
<table>
<tr><th>B1</th><th>B2</th><th colspan="5">Action</th></tr>
<tr><td>0</td><td>0</td><td colspan="5">Assign time slot to encoder & decoder</td></tr>
<tr><td>0</td><td>1</td><td colspan="5">Assign time slot to encoder</td></tr>
<tr><td>1</td><td>0</td><td colspan="5">Assign time slot to decoder</td></tr>
<tr><td>1</td><td>1</td><td colspan="5">Power-down CODEC</td></tr>
<tr><th>B3</th><th>B4</th><th>B5</th><th>B6</th><th>B7</th><th>B8</th><th>Time Slot</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>3</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>4</td></tr>
<tr><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td></tr>
<tr><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td></tr>
<tr><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>63</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>64</td></tr>
</table>
Bits 3 through 8 for time-slot assignments 1 through 64. The time-slot numbers equal one more than the decimal equivalent represented by bits 3 (MSB) through 8 (LSB) using positive logic.</td></tr>
</table>

Note: H = High Level, L = Low Level, X = Irrelevant, ↓ = From V_{CC} to Low Transition

TABLE 1. OPERATION CONTROL CONFIGURATIONS

APPLICATION CIRCUIT (TYPICAL)



Analog Ground

Digital Ground

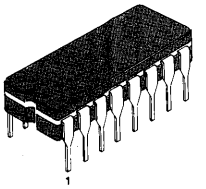
$$\text{Transmit Gain} = 20 \times \log\left(\frac{R3 + R2}{R2}\right) + 3\text{dB}$$

$$\text{Receive Gain} = 20 \times \log\left(\frac{R4}{R2 + R5}\right) \text{ for each power amp}$$

COMBO CODECS

The KT8554 and KT8557 are single-chip PCM encoders and decoders (PCM CODECs) and PCM line filters. These devices provide all the functions required to interface a full-duplex voice telephone circuit with a time-division-multiplexed (TDM) system.
These devices are designed to perform the transmit encoding and receive decoding as well as the transmit and receive filtering functions in PCM system. They are intended to be used at the analog termination of a PCM line or trunk.
These devices provide the bandpass filtering of the analog signals prior to encoding and after decoding. These combination devices perform the encoding and decoding of voice and call progress tones as well as the signaling and supervision information.

16 CERDIP



FEATURES

- **Complete CODEC and filtering system**
- **Meets or exceeds AT&T D3/D4 and CCITT specifications**
  μ-Law: KT8554, A-Law: KT8557
- **On-chip auto zero, sample and hold, and precision voltage references**
- **Low power dissipation: 60mW (operating)**
  3mW (standby)
- **$\pm$5V operation**
- **TTL or CMOS compatible**
- **Automatic power down**

ORDERING INFORMATION

Device	Package	Operating Temperature
†KT8554N	Plastic	−25~+125°C
†KT8557N	Plastic	
KT8554J	Ceramic	
KT8557J	Ceramic	

† Under Development

BLOCK DIAGRAMS

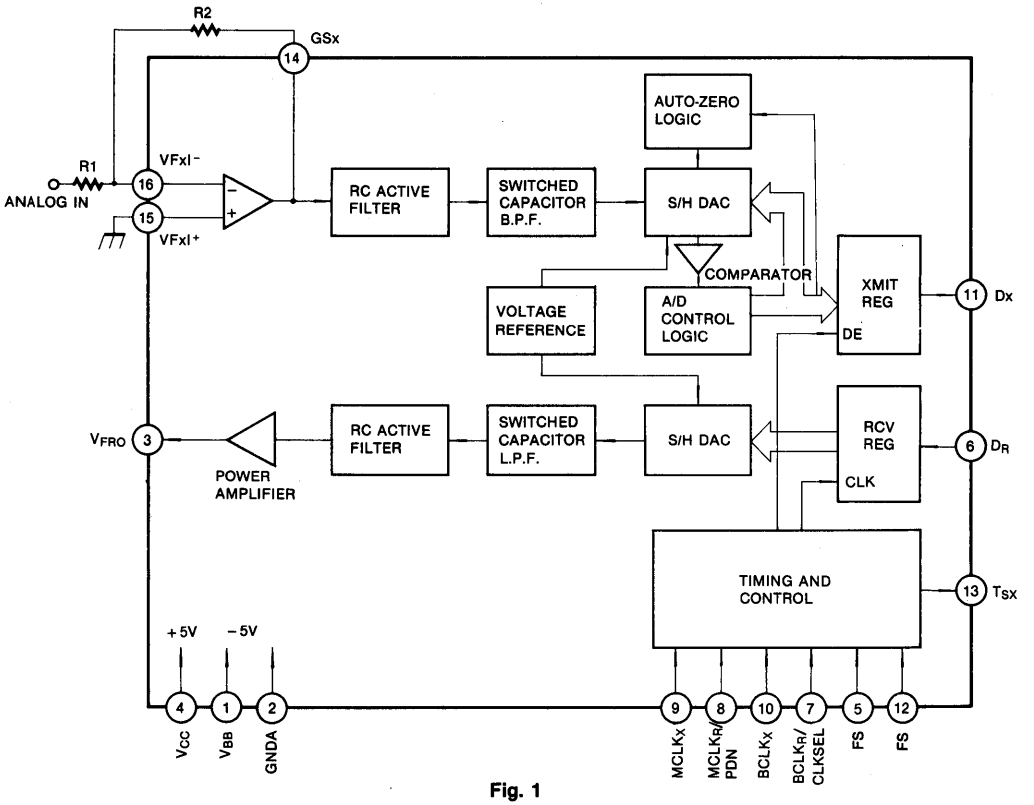


Fig. 1

ABSOLUTE MAXIMUM RATINGS

Characteristic.	Symbol	Value	Unit
V_{CC} to GNDA	V_{CC}	7	V
V_{BB} to GNDA	V_{BB}	−7	V
Voltage at Any Analog Input or Output	AI/O	$V_{CC}+0.3$ to $V_{BB}-0.3$	V
Voltage at Any Digital Input or Output	DI/O	$V_{CC}+0.3$ to GNDA − 0.3	V
Operating Temperature Range	Ta	−25 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Lead Temperature (Soldering, 10 secs)	T_L	300	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, $V_{CC} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$, GNDA = 0V, Ta = 0°C to 70°C; typical characteristics specified at $V_{CC} = 5.0V$, $V_{BB} = -5.0V$, Ta = 25°C; all signals referenced to GNDA.)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Power Dissipation						
Power-Down Current	$I_{CC}0$	No Load		0.5	1.5	mA
Power-Down Current	$I_{BB}0$	No Load		0.05	0.3	mA
Active Current	$I_{CC}1$	No Load		6.0	9.0	mA
Active Current	$I_{BB}1$	No Load		6.0	9.0	mA
Digital Interface						
Input Low Voltage	V_{IL}				0.6	V
Input High Voltage	V_{IH}		2.2			V
Input Low Current	I_{IL}	$GNDA \leq V_{IN} \leq V_{IL}$, all digital inputs	−10		10	μA
Input High Current	I_{IH}	$V_{IH} \leq V_{IN} \leq V_{CC}$	−10		10	μA
Output Low Voltage	V_{OL}	D_X, $I_L = 3.2mA$ SIG_R, $I_L = 1.0mA$ $\overline{TS}_X$, $I_L = 3.2mA$, open drain			0.4 0.4 0.4	V V V
Output High Voltage	V_{OH}	D_X, $I_H = -3.2mA$ SIG_R, $I_H = -1.0mA$	2.4 2.4			V V
Output Current in High Impedance State (TRI-STATE)	I_{OZ}	D_X, $GNDA \leq V_O \leq V_{CC}$	−10		10	μA
Analog Interface with Receive Filter						
Output Resistance	R_ORF	Pin VF_RO		1	3	Ω
Load Resistance	R_LRF	$VF_RO = \pm 2.5V$	600			Ω
Load Capacitance	C_LRF				500	pF
Output DC Offset Voltage	VOS_RO		−200		200	mV
Analog Interface with Transmit Input Amplifier						
Input Leakage Current	I_IXA	$-2.5V \leq V \leq +2.5V$, VF_XI+ or VF_XI-	−200		200	nA
Input Resistance	R_IXA	$-2.5V \leq V \leq +2.5V$, VF_XI+ or VF_XI-	10			MΩ
Output Resistance	R_OXA	Closed loop, unity gain		1	3	Ω
Load Resistance	R_LXA	GS_X	10			KΩ
Load Capacitance	C_LXA	GS_X			50	pF
Output Dynamic Range	V_OXA	GS_X, $R_L \leq 10K\Omega$	±2.8			V
Voltage Gain	A_VXA	VF_XI+ to GS_X	5,000			V/V
Unity Gain Bandwidth	F_UXA		1	2		MHz
Offset Voltage	V_{OS}XA		−20		20	mV
Common-Mode Voltage	V_{CM}XA	CMRRXA > 60dB	−2.5		2.5	V
Common-Mode Rejection Ratio	CMRRXA	DC Test	60			dB
Power Supply Rejection Ratio	PSRRXA	DC Test	60			dB

TIMING CHARACTERISTICS

(Unless otherwise noted, $V_{CC} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$, GNDA = 0V, Ta = 0°C to 70°C; typical characteristics specified at $V_{CC} = 5.0V$, $V_{BB} = -5.0V$, Ta = 25°C; all signals referenced to GNDA.)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency of Master Clocks	$1/t_{PM}$	Depends on the device used and the $BCLK_R$/CLKSEL Pin. $MCLK_X$ and $MCLK_R$		1.536 1.544 2.048		MHz MHz MHz
Rise Time of Bit Clock	t_{RB}	$t_{PB} = 488ns$			50	ns
Fall Time of Bit Clock	t_{FB}	$t_{PB} = 488ns$			50	ns
Holding Time from Bit Clock Low to Frame Sync	t_{HBFL}	Long frame only	0			ns
Holding Time from Bit Clock High to Frame Sync	t_{HOLD}	Short frame only	0			ns
Set-Up Time from Frame Sync to Bit Clock Low	t_{SFB}	Long frame only	80			ns
Delay Time from $BCLK_X$ High to Data Valid	t_{DBD}	Load = 150pF plus 2 LSTTL loads	0		180	ns
Delay Time to $\overline{TS_X}$ Low	t_{XDP}	Load = 150pF plus 2 LSTTL loads			140	ns
Delay Time from $BCLK_X$ Low to Data Output Disabled	t_{DZC}		50		165	ns
Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Comes Later	t_{DZF}	$C_L = 0pF$ to 150pF	20		165	ns
Set-Up Time from D_R Valid to $BCLK_{R/X}$ Low	t_{SDB}		50			ns
Hold Time from $BCLK_{R/X}$ Low to D_R Invalid	t_{HBD}		50			ns
Delay Time from $BCLK_{R/X}$ Low to SIG_R Valid	t_{DFSSG}	Load = 50pF plus 2 LSTTL loads			300	ns
Set-Up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low	t_{SF}	Short frame sync pulse (1 or 2 bit clock periods long) (Note 1)	50			ns
Width of Master Clock High	t_{WMH}	$MCLK_X$ and $MCLK_R$	160			ns
Width of Master Clock Low	t_{WML}	$MCLK_X$ and $MCLK_R$	160			ns
Rise Time of Master Clock	t_{RM}	$MCLK_X$ and $MCLK_R$			50	ns
Fall Time of Master Clock	t_{FM}	$MCLK_X$ and $MCLK_R$			50	ns
Set-Up Time from $BCLK_X$ High (and FS_X In Long Frame Sync Mode) to $MCLK_X$ Falling Edge	t_{SBFM}	First bit clock after the leading edge of FS_X				
Period of Bit Clock	t_{PB}		485	488	15,725	ns
Width of Bit Clock High	t_{WBH}	$V_{IH} = 2.2V$	160			ns
Width of Bit Clock Low	t_{WBL}	$V_{IL} = 0.6V$	160			ns

TIMING CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	t_{HF}	Short frame sync pulse (1 or 2 bit clock periods long) (Note 1)	100			ns
Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R)	t_{HBFI}	Long frame sync pulse (from 3 to 8 bit clock periods long)	100			ns
Minimum Width of the Frame Sync Pulse (Low Level)	t_{WFL}	64K bit/s operating mode	160			ns

Note 1: For short frame sync timing, FS_X and FS_R must go high while their respective bit clocks are high.

4

TIMING DIAGRAM

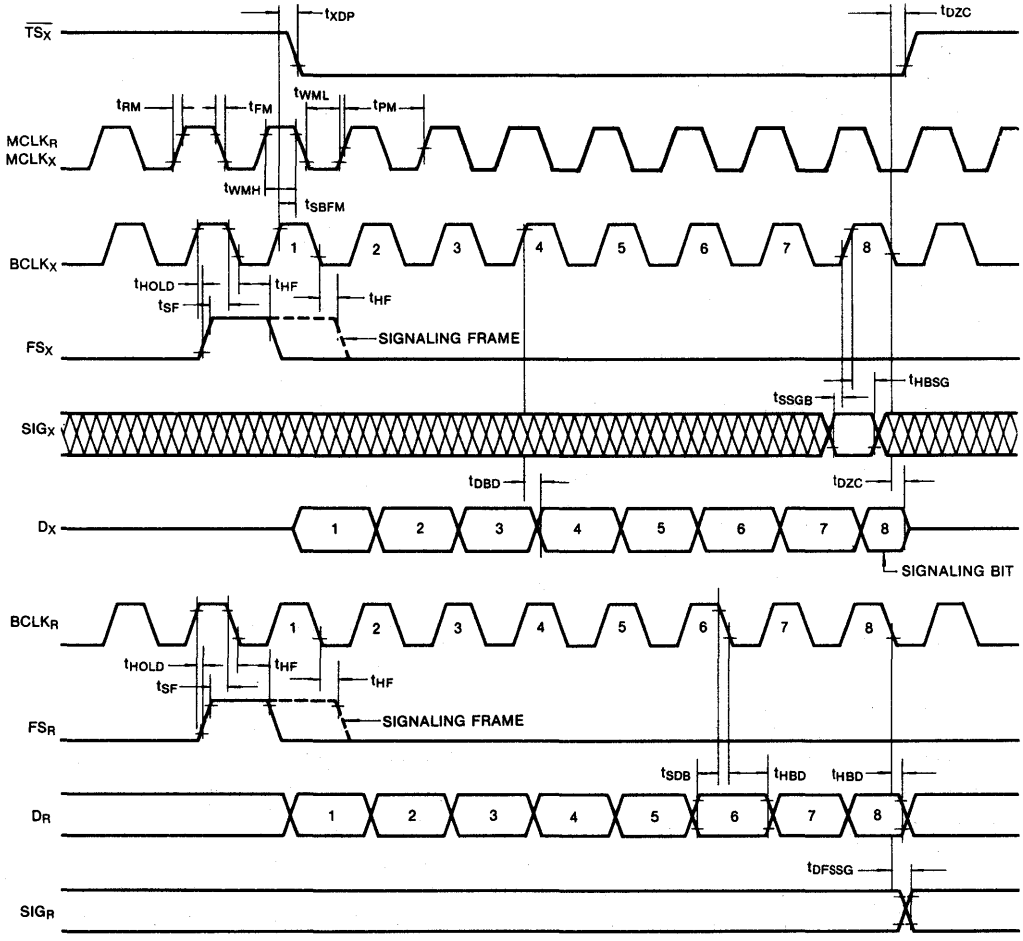


Fig. 2. Short Frame Sync Timing

TIMING DIAGRAM (Continued)

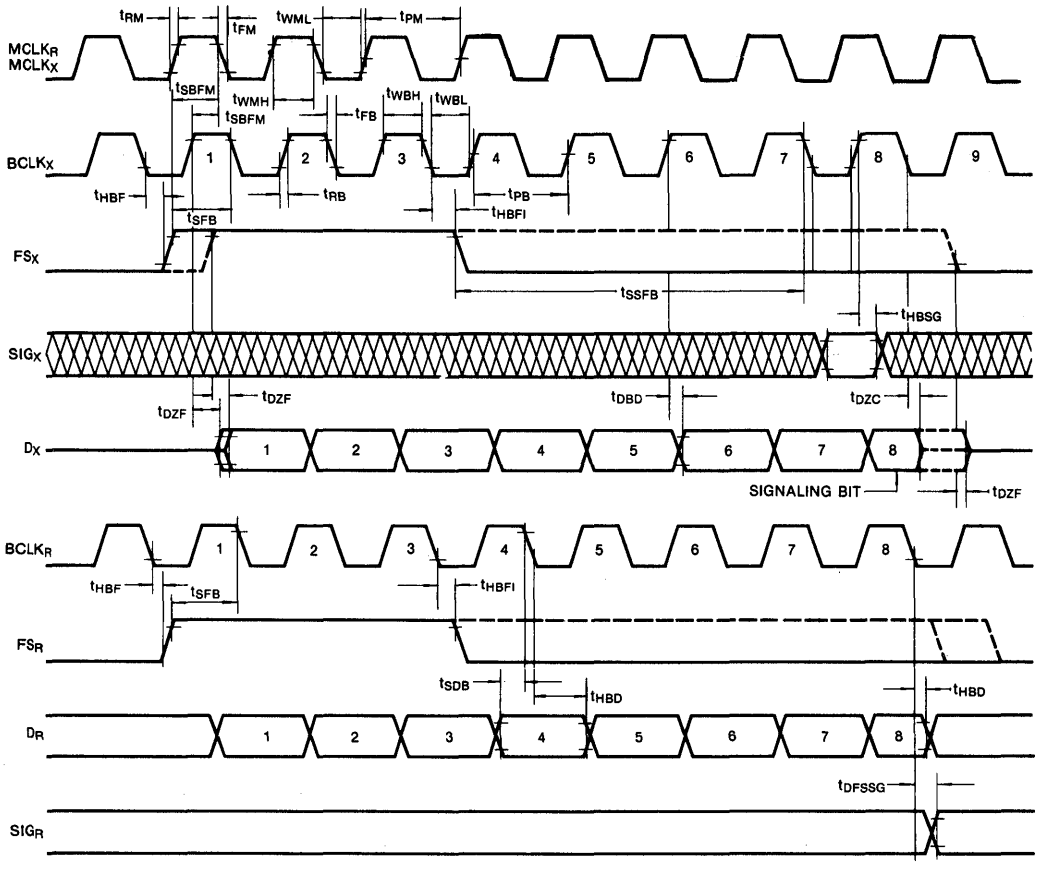


Fig. 3 Long Frame Sync Timing

TRANSMISSION CHARACTERISTICS

(Unless otherwise specified: Ta = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, GNDA = 0V, f = 1.02KHz, V_{IN} = 0dBm0, transmit input amplifier connected for unity-gain non-inverting.)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Amplitude Response						
Receive Gain, Absolute	G_{RA}	Ta = 25°C, V_{CC} = 5V, V_{BB} = −5V Input = Digital code sequence for 0dBm0 signal at 1020Hz	−0.15		0.15	dB
Receive Gain, Relative to G_{RA}	G_{RR}	f = 0Hz to 3000Hz f = 3300Hz f = 3400Hz f = 4000Hz	−0.15 −0.35 −0.7		0.15 0.05 0 −14	dB dB dB dB
Absolute Receive Gain Variation with Temperature	G_{RAT}	Ta = 0°C to 70°C			±0.1	dB
Absolute Receive Gain Variation with Supply Voltage	G_{RAV}	V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%			±0.05	dB
Receive Gain Variations with Level	G_{RRL}	Sinusoidal test method; reference input PCM code corresponds to an Ideally encoded −10dBm0 signal PCM level = −40dBm0 to +3dBm0 PCM level = −50dBm0 to −40dBm0 PCM level = −55dBm0 to −50dBm0	 −0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB
Receive Output Drive Level	V_{RO}	R_L = 600Ω	−2.5		2.5	V
Absolute Levels	A_L	Nominal 0dBm0 level is 4dBm (600Ω) 0dBm0		1.2276		V_{rms}
Max Overload Level	t_{MAX}	Max overload level (3.17dBm0): KT8554 Max overload level (3.14dBm0): KT8557		2.501		V_{PK}
Transmit Gain, Absolute	G_{XA}	Ta = 25°C, V_{CC} = 5V, V_{BB} = −5V Input at GS_X = 0dBm0 at 1020Hz	−0.15		0.15	dB
Transmit Gain, Relative to G_{XA}	G_{XR}	f = 16Hz f = 50Hz f = 60Hz f = 200Hz f = 300Hz − 3000Hz f = 3300Hz f = 3400Hz f = 4000Hz f = 4600Hz and up, measure response from 0Hz to 4000Hz	 −1.8 −0.15 −0.35 −0.7		−40 −30 −26 −0.1 0.15 0.05 0 −14 −32	dB dB dB dB dB dB dB dB dB
Absolute Transmit Gain Variation with Temperature	G_{XAT}	Ta = 0°C to 70°C			±0.1	dB
Absolute Transmit Gain Variation with Supply Voltage	G_{XAV}	V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%			±0.05	dB
Transmit Gain Variations with Level	G_{XRL}	Sinusoidal test method Reference level = −10dBm0 VF_XI+ = −40dBm0 to +3dBm0 VF_XI+ = −50dBm0 to −40dBm0 VF_XI+ = −55dBm0 to −50dBm0	 −0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB

4

TRANSMISSION CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Envelope Delay Distortion with Frequency						
Receive Delay, Absolute	D_{RA}	f = 1600Hz		180	200	μs
Receive Delay, Relative to D_{RA}	D_{RR}	f = 500Hz – 1000Hz	– 40	– 25		μs
		f = 1000Hz – 1600Hz	– 30	– 20		μs
		f = 1600Hz – 2600Hz		70	90	μs
		f = 2600Hz – 2800Hz		100	125	μs
		f = 2800Hz – 3000Hz		145	175	μs
Transmit Delay, Absolute	D_{XA}	f = 1600Hz		290	315	μs
Transmit Delay, Relative to D_{XA}	D_{XR}	f = 500Hz – 600Hz		195	220	μs
		f = 600Hz – 800Hz		120	145	μs
		f = 800Hz – 1000Hz		50	75	μs
		f = 1000Hz – 1600Hz		20	40	μs
		f = 1600Hz – 2600Hz		55	75	μs
		f = 2600Hz – 2800Hz		80	105	μs
		f = 2800Hz – 3000Hz		130	155	μs
Noise						
Receive Noise, C Message Weighted	N_{RC}	PCM code equals alternating positive and negative zero, KT8554		8	11	dBrncO
Receive Noise, P Message Weighted	N_{PP}	PCM code equals, positive zero, KT8557		– 82	– 79	dBmOp
Transmit Noise, C Message Weighted	N_{XC}	KT8554		12	15	dBrncO
Transmit Noise, P Message Weighted	N_{XP}	KT8557		– 74	– 67	dBmOp
Noise, Single Frequency	N_{RS}	f = 0KHz to 100KHz, loop around measurement, $VF_XI+ = 0V_{rms}$			– 53	dBmO
Positive Power Supply Rejection, Transmit	$PPSR_X$	$VF_XI+ = 0V_{rms}$, $V_{CC} = 5.0V_{DC} + 100mV_{rms}$ f = 0KHz – 50KHz	30	35		dBC
Negative Power Supply Rejection, Transmit	$NPSR_X$	$VF_XI+ = 0V_{rms}$, $V_{BB} = -5.0V_{DC} + 100mV_{rms}$ f = 0KHz – 50KHz	40	45		dBC
Positive Power Supply Rejection, Receive	$PPSR_R$	PCM code equals positive zero $V_{CC} = 5.0V_{DC} + 100mV_{rms}$				
		f = 0Hz – 4000Hz	35			dBC
		f = 4KHz – 25KHz	35			dB
		f = 25KHz – 50KHz	35			dB
Negative Power Supply Rejection, Receive	$NPSR_R$	PCM code equals positive zero $V_{BB} = -5.0V_{DC} + 100mV_{rms}$				
		f = 0Hz – 4000Hz	40			dBC
		f = 4KHz – 25KHz	40			dB
		f = 25KHz – 50KHz	36			dB

TRANSMISSION CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious Out-of-Band Signals at the Channel Output	SOS	Loop around measurement, 0dBm0, 300Hz – 3400Hz input applied to VF_XI+, Measure individual image signals at VF_RO 4600Hz – 7600Hz 7600Hz – 8400Hz 8400Hz – 100,000Hz			 – 32 – 40 – 32	 dB dB dB
Distortion						
Signal to Total Distortion	STD_X	Sinusoidal test method				
Transmit or Receive Half-Channel	STD_R	Level = 3.0dBm0 = 0dBm0 to 30dBm0 = – 40dBm0 XMT RCV = – 55dBm0 XMT RCV	33 36 29 30 14 15			dBC dBC dBC dBC dBC dBC
Single Frequency Distortion, Transmit	SFD_X				– 46	dB
Single Frequency Distortion, Receive	SFD_R				– 46	dB
Intermodulation Distortion	IMD	Loop around measurement, VF_X+ = – 4dBm0 to – 21dBm0, two frequencies in the range 300Hz – 3400Hz			– 41	dB
Crosstalk						
Transmit to Receive Crosstalk, 0dBm0 Transmit Level	CT_{X-R}	f = 300Hz – 3400Hz D_R = Steady PCM code		– 90	– 75	dB
Receive to Transmit Crosstalk, 0dBm0 Receive Level	CT_{R-X}	f = 300Hz – 3400Hz, VF_XI = 0V		– 90	– 70 (Note 1)	dB

Note 1. CT_{R-X} is measured with a – 40dBm0 activating signal applied at VF_XI+

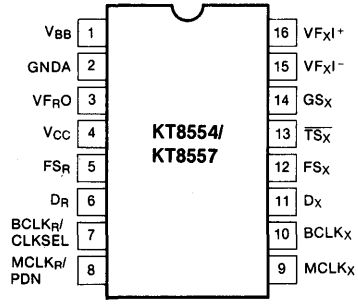
ENCODING FORMAT AT Dx OUTPUT

	μ-Law KT8554	A-Law KT8557
V_{IN} (at GS_X) = + Full – Scale	1 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0
V_{IN} (at GS_X) = 0V	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
V_{IN} (at GS_X) = – Full – Scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0

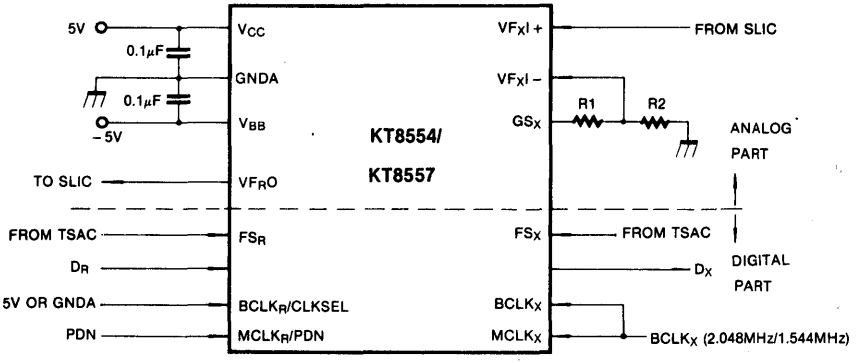
PIN DESCRIPTION

Pin No.	Symbol	Description
1	V_{BB}	Negative power supply. $V_{BB} = -5V \pm 5\%$.
2	GNDA	Analog ground. All signals are referenced to this pin.
3	VF_RO	Analog output of the receive filter.
4	V_{CC}	Positive power supply. $V_{CC} = +5V \pm 5\%$.
5	FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8KHz pulse train.
6	D_R	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
7	$BCLK_R$/ CLKSEL	The bit clock which shifts data into D_R after the FS_R leading edge. Many vary from 64KHz to 2.048MHz. Alternatively, may be a logic input which selects either 1.536MHz/1.544MHz or 2.048MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions.
8	$MCLK_R$/ PDN	Receive master clock. Must be 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continously low, $MCLK_R$ is selected for all internal timing. When $MCLK_R$ is connected continuously high the device is powered down.
9	$MCLK_X$	Transmit master clock. Must be 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with $MCLK_R$.
10	$BCLK_X$	The bit clock which shifts out the PCM data on D_X. May vary from 64KHz to 2.048MHz, but must be synchronous with $MCLK_X$.
11	D_X	The TRI-STATE PCM data output which is enabled by FS_X.
12	FS_X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8KHz pulse train.
13	$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
14	GS_X	Analog output of the transmit input amplifier. Used to externally set again.
15	$V_{FXI}-$	Inverting input of the transmit input amplifier.
16	$V_{FXI}+$	Non-inverting input of the transmit input amplifier.

PIN CONNECTION



APPLICATION CIRCUITS

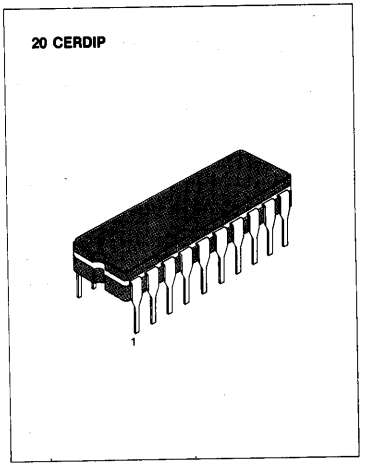


Note: XMIT gain $= 20 \times \log(\frac{R1+R2}{R2})$, $(R1+R2) > 10K\Omega$.

Fig. 4

TIME SLOT ASSIGNMENT CIRCUIT (TSAC)

The KT8555 is a per channel Time Slot Assignment Circuit (TSAC) that produces 8-bit receive and transmit time slots for 4 COMBO CODEC/Filters.
Each frame synchronization pulse may be independently assigned to a time slot in a frame of up to 64 time slots.



FEATURES

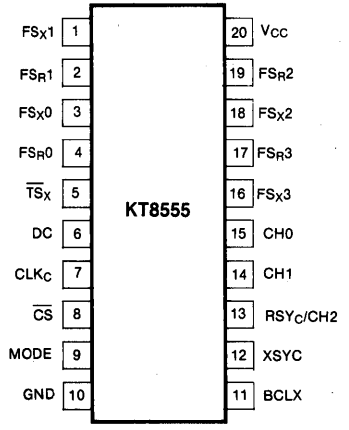
- **Single, 5V operation**
- **Low power consumption: 5mW**
- **Controls 4 COMBO CODEC/Filters**
- **Independent transmit and receive frame syncs and enables**
- **8 channel unidirectional mode**
- **Up to 64 time slots per frame**
- **Compatible with KT8554/7, KT8564/7, KT8520/1 CODECs**
- **TTL and CMOS compatible**

ORDERING INFORMATION

Device	Package	Operating Temperature
†KT8555N	20 Plastic DIP	−20~+125°C
KT8555J	20 Ceramic DIP	

† Under Development

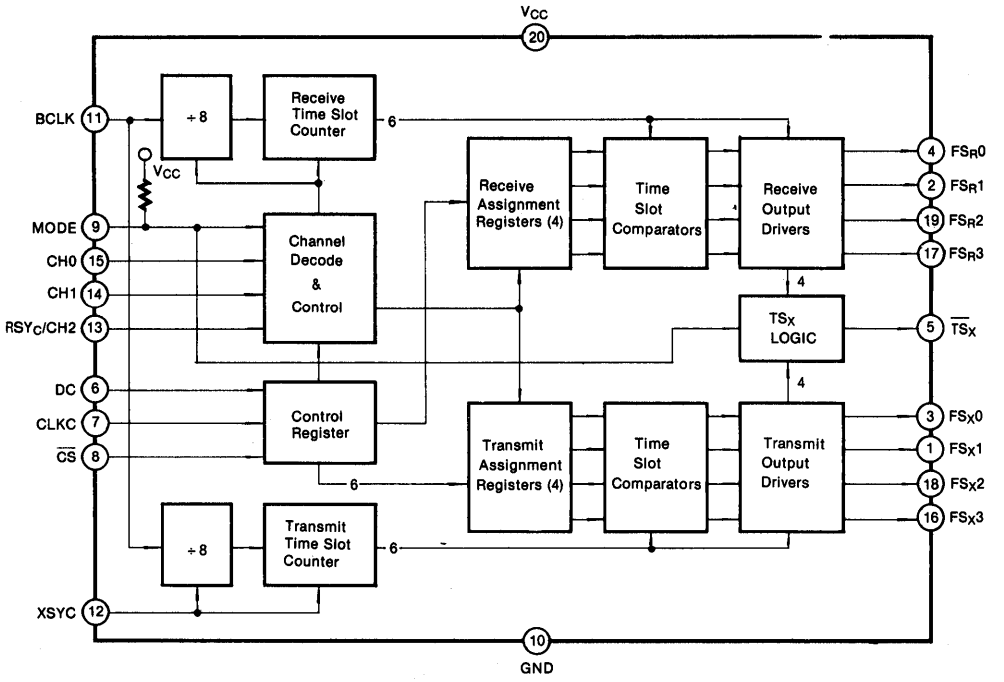
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Function
3 1 18 16	FS_X0 FS_X1 FS_X2 FS_X3	A frame sync output which is normally low, and goes active-high for 8 cycles of BCLK when a valid transmit time slot assignment is made.
4 2 19 17	FS_R0 FS_R1 FS_R2 FS_R3	A frame sync output which is normally low, and goes active-high for 8 cycles of BCLK when a valid receive time slot assignment is made.
5	$\overline{TS_X}$	This pin pulls low during any active transmit time slot. (N-channel open drain)
6	D_C	The input for an 8 bit serial control word. $\overline{X}$ is the first bit clocked in.
7	CLK_C	The clock input for the control interface.
8	$\overline{CS}$	The active-low chip select for the control interface.
9	MODE	Mode 1 = Open or V_{CC} Mode 2 = Gnd
10	GND	Ground
11	BCLK	The bit clock input
12	XSYC	The transmit TSO sync pulse input. Must be synchronous with BCLK.
13	RSY_C/CH2	This input function is determined by the MODE input (Pin 9). In mode 1 this input is the receive TSO sync pulse, RSY_C, which must be synchronous with BCLK. In mode 2 this is the CH2 input for the MSB of the channel select word.
14	CH1	The input for the NSB (next significant bit) of the channel select word.
15	CH0	The input for the LSB (last significant bit) of the channel select word, which defines the frame sync output affected by the following control word.
20	V_{CC}	Power supply pin. 5V ± 5%

BLOCK DIAGRAM



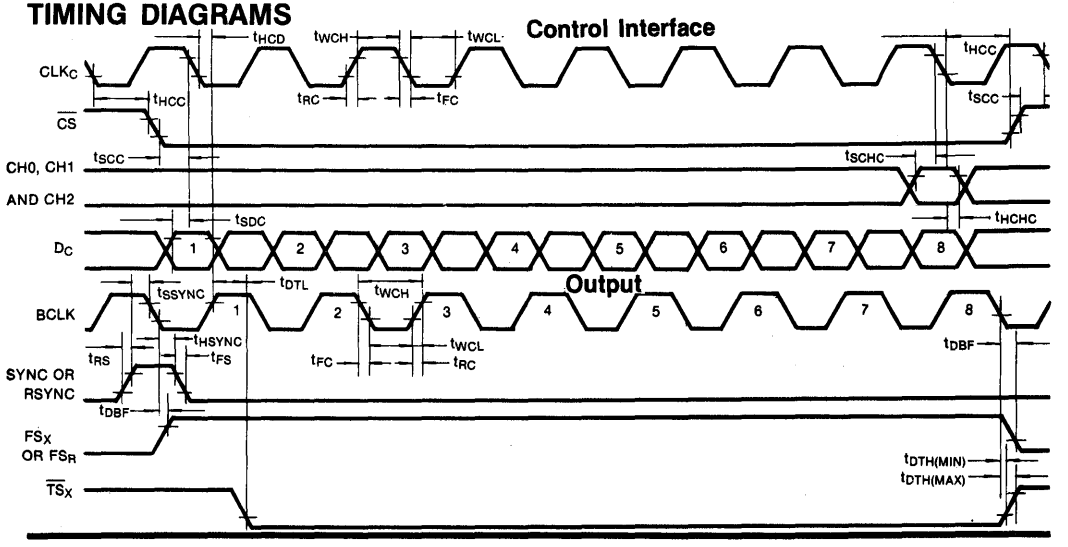
ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
V_{CC} to GND	V_{CC}	7.0	V
Any Input Voltage	V_I	$V_{CC}+0.3 \sim -0.3$	V
Any Output Voltage	V_O	$V_{CC}+0.3 \sim -0.3$	V
Operating Temperature Range	Ta	$-25 \sim 125$	°C
Storage Temperature Range	T_{stg}	$-65 \sim 150$	°C
Lead Temperature (Soldering, 10 secs)	T_L	300	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted; V_{CC} = 5.0V ± 5%, Ta = 0°C ~ 70°C)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Current	I_{CC}	BCLK = 4.096MHz, All outputs open		1	1.5	mA
Input Voltage High	V_{IH}		2.0			V
Input Voltage Low	V_{IL}				0.7	V
Input Current 1	I_{I1}	All Inputs Except Mode, $V_{IL} < V_{IN} < V_{IH}$	−1		1	μA
Input Current 2	I_{I2}	Mode, V_{IN} = 0V	−100			μA
Output Voltage High	V_{OH}	FS_X and FS_R Ouputs, I_{OH} = 3mA	2.4			V
Output Voltage Low	V_{OL}	FS_X and FS_R Outputs, I_{OL} = 3mA			0.4	V
		TS_X output, I_{OL} = 3mA			0.4	V
Rise and Fall Time of Clock	t_{RC}, t_{FC}	BCLK, CLKC			50	nS
Delay to $\overline{T_{SX}}$ Low	t_{DTL}	C_L = 50pF			140	nS
Delay to $\overline{T_{SX}}$ High	t_{DTH}	R_L = 1KΩ to V_{CC}	30		100	nS
Hold Time from BCLK to Frame Sync	t_{HS}		50			nS
Set-Up Time from Frame Sync to BLCK	t_{SS}		30			nS
Delay Time from BLCK Low to $S_{X/R}$ 0-3 High or Low	t_{DBF}	C_L = 50pF			50	nS
Hold Time from Channel Select to CLKC	t_{HCH}		50			nS
Set-Up Time from Channel Select to CLKC	t_{SCH}		30			nS
Period of Clock	t_{PC}	BCLK, CLKC	240			nS
Width of Clock High	t_{WCH}	BCLK, CLKC	50			nS
Width of Clock Low	t_{WCL}	BCLK, CLKC	50			nS
Set-Up Time from D_C to CLKC	t_{SDC}		30			nS
Hold Time from CLKC to D_C	t_{HCD}		50			nS
Set-Up Time from CS to CLKC	t_{SCC}		30			nS
Hold Time from CLKC to CS	t_{HCC}		100			nS

TIMING DIAGRAMS



FUNCTION DESCRIPTION

Operating Modes

The KT8555 is a control interface which requires an 8 bit serial control word. The device is compatible with KT8520/KT8521 CODECs. Either one of the frame sync output group, FS_X0 to FS_X3 or FS_R0 to FS_R3, affected by the control word is defined by the two bits, $\overline{X}$ and $\overline{R}$. Time slot selected from 0 to 63 is specified. A frame sync output is highly active for one time slot which is equivalent to 8 cycles of BLCK. Up to 64 time slots are allowed to form a frame. There are two operational mode. In mode 1, each channel of transmit and receive direction has different time slot assigned. This mode can be selected by either leaving pin 9 (MODE) opened or connecting it with V_{CC}. In such a case, pin 13 is RSYNC input defining the start of each receive frame while four outputs, FS_R0 to FS_R3, are assigned with respect to RSYNC. On the other hand, start of each transmit frame is defined by XSYNC input by which output FS_X0 to FS_X3, are assigned. XSYNC and RSYNC can be phase related. Channels from 0-3 are selected by the input CH0 and CH1 (refer to the table 1). In mode 2, all 8 frame sync outputs can be assigned with respect to XSYNC input. The mode 2, selected by connecting pin 9 (MODE) to GND, enables the KT8555 TSAC suitable for an 8-channel undirectional controller and for a system where both transmit and receive direction of each channel have same time slot assigned. For instance, FS_X and FS_R input of COMBO CODEC/FILTER are hard wired together. The channel assigned has its channel selected by CH0, CH1 and CH2 (refer to table 2).

$\overline{X}$	$\overline{R}$	T5	T4	T3	T2	T1	T0

$\overline{X}$ is the first bit clocked into DC input

CONTROL DATA FORMAT

T5	T4	T3	T2	T1	T0	Time Slot
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
						.
						.
						.
0	1	1	1	1	0	30
0	1	1	1	1	1	31
1	0	0	0	0	0	32
1	0	0	0	0	1	33
						.
						.
						.
1	1	1	1	1	1	63

CH1	CH0	Channel Selected
0	0	Assign to FS_X0 and/or FS_R0
0	1	Assign to FS_X1 and/or FS_R1
1	0	Assign to FS_X2 and/or FS_R2
1	1	Assign to FS_X3 and/or FS_R3

$\overline{X}$	$\overline{R}$	Action
0	0	Assign time slot to both selected FS_X and FS_R
0	1	Assign time slot to seleced FS_X only
1	0	Assign time slot to selected FS_R only
1	1	Disable both selected FS_X and FS_R

TABLE 1. CONTROL MODE 1

CH2	CH1	CH0	Channel Selected
0	0	0	Assign to FS_X0
0	0	1	Assign to FS_X1
0	1	0	Assign to FS_X2
0	1	1	Assign to FS_X3
1	0	0	Assign to FS_R0
1	0	1	Assign to FS_R1
1	1	0	Assign to FS_R2
1	1	1	Assign to FS_R3

$\overline{X}$	$\overline{R}$	Action
0	0	Assign time slot to selected output
0	1	Assign time slot to selected output
1	0	Assign time slot to selected output
1	1	Disable selected output

TABLE 2. CONTROL MODE 2

4

Loading Control Data

While control data is loaded, the binary cord for the selected channel should be set on inputs CH0 and CH1 (and CH2 in mode 2). Please refer to Tables 1 and 2.
Control data is clocked into the DC input on the falling edges of CLKC with low $\overline{CS}$. A newly assigned time slot is transferred to the assignment register, selected on the high going of $\overline{CS}$, and it is re-synchronized to the system clock. As a result the newly generated FS output pulse will start at the next complete valid time slot after the rising edge of $\overline{CS}$.

Power Up Initialization

All frame sync outputs, FS_X0-FS_X3 and FS_R0-FS_R3, are inhibited and held low during power-up period. Therefore no output is active until a valid time slot is assigned.

Time Slot Counter Operation

As TSO of each transmit frame starts, defined by the first falling edge of BCLK after XSYNC goes high, the transmit time slot counter is reset to 000000. Then it starts increasing once every 8 cycles of BLCK. When a match is found by comparing each count with the 4 transmit assignment register, a frame sync pulse is generated at the FS_X output.
Like wise the start of the receive TSO is defined by the falling edge of BCLK after RSYNC goes high. The output, FS_R0-FS_R3, are generated with respect to TSO when the receive time counter is matched with an appropriate receive assignment register.

$\overline{TS}_X$ Output

In mode 1, where there are separate transmit and receive assignments, the output is pulled low of FS_X output pulse is detected. During the mode 2, the output is pulled low if either of FS_X or FS_R is generated. Other than such cases, it is an open circuit allowing $\overline{TS}_X$ outputs of TSACs to be wire-ANDed together with a common pull-up resistor. The output can control the TRI-STATE enable input of a line driver to buffer the transmit PCM bus provided from the CODEC/Filter to the backplane.

APPLICATION CIRCUIT

The KT8555 TSAC combined with any kind of COMBO from KT8554/7 or KT8564/7 series can obtain data timing as illustrated in Fig. 1. Even though FS_X output goes high before BCLK gets high, the D_X output of the combo remains in the TRI-STATE mode until both outputs are high. The eight bit period is shortened to avoid a bus clash as on the KT8520/1 CODECs.
Alternatively, full 8 bits can be obtained by inverting the BCLK to the combo devices, thereby rising edges of BLCK and $FS_{X/R}$ are aligned.
Fig. 2 is typical timing of the control data interface.
Fig. 3 is the digital interconnections of a typical line card application.

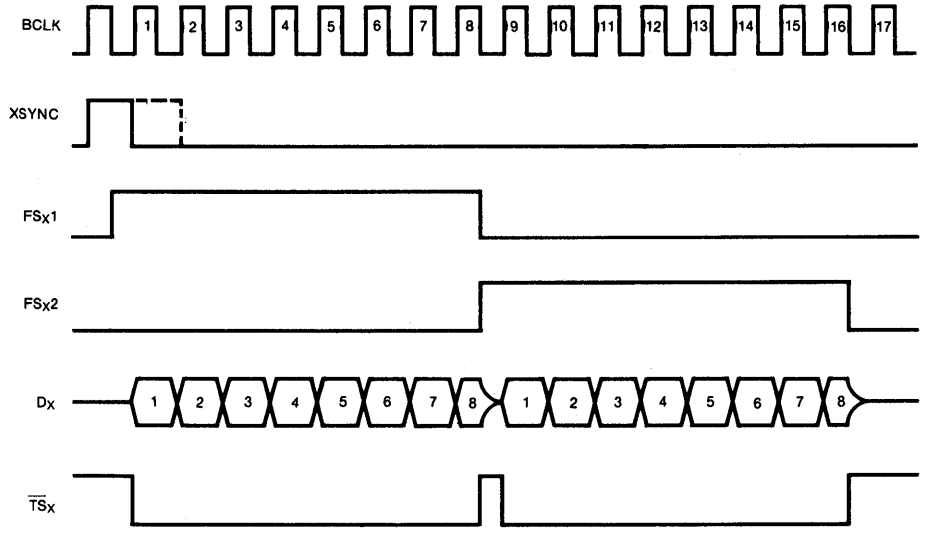


Fig. 1 Transmit Data Timing

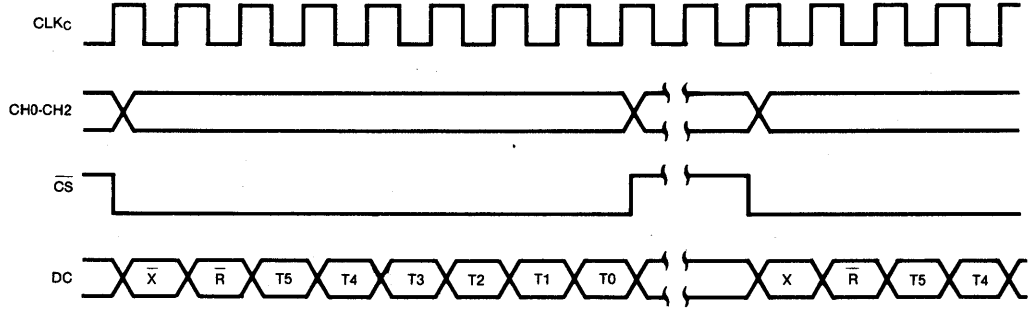


Fig. 2 Control Data Timing

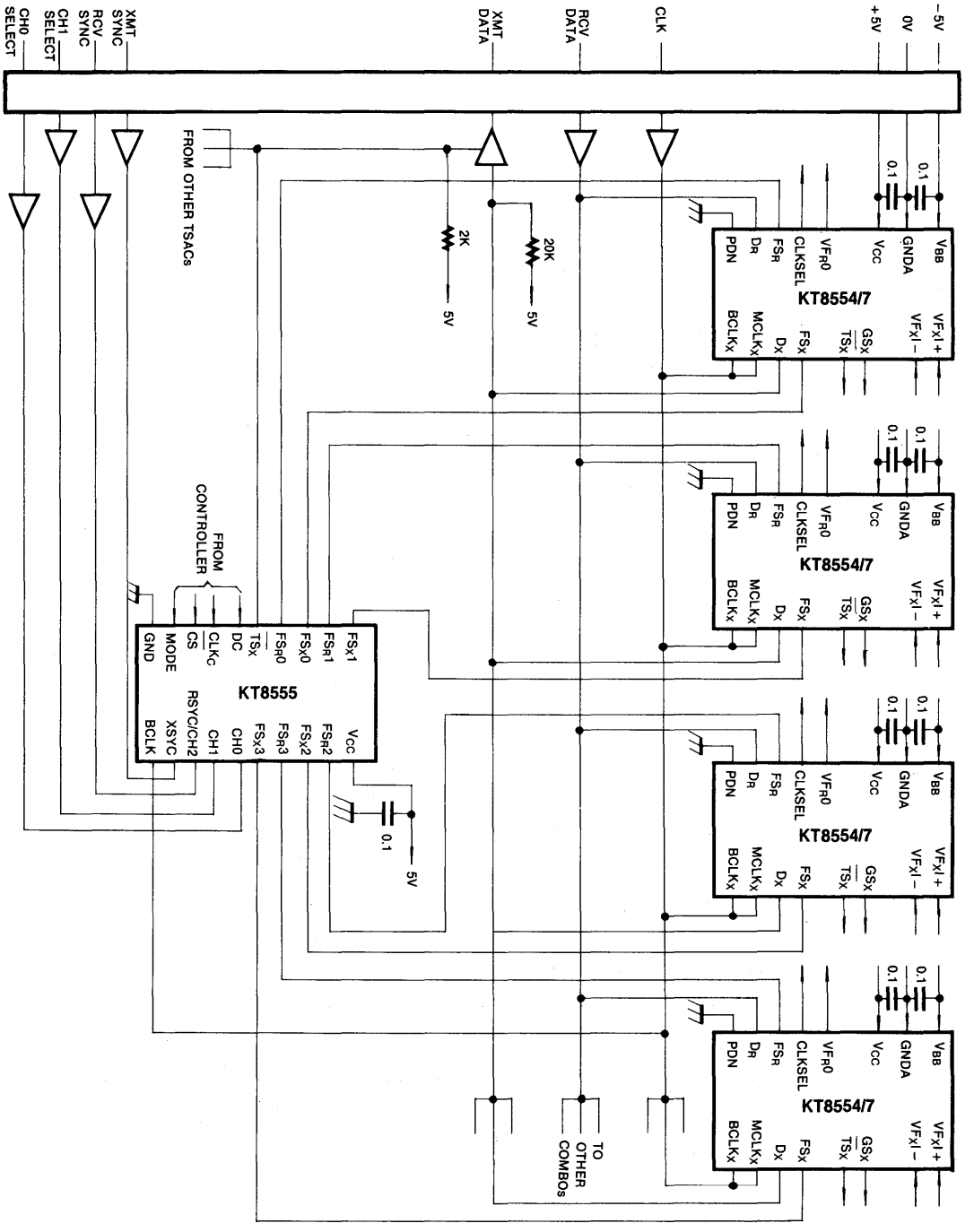
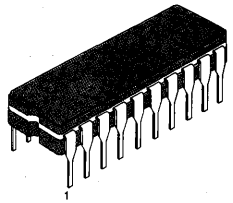


Fig. 3 Digital Interconnections on a Typical Synchronous Line Board

COMBO CODECS

The KT8564 and KT8567 are single-chip PCM encoders and decoders (PCM CODECs), PCM line filter and receive power amp.
These devices provide all the functions required to interface a full-duplex voice telephone circuit with a time-division-multiplexed (TDM) system.
These devices are designed to perform the transmit encoding and decoding as well as the transmit and receive filtering functions in PCM system.
They are intended to be used at the analog termination of a PCM line or trunk.
These devices provide the bandpass filtering of the analog signals prior to encoding and after decoding. These combination devices perform the encoding and decoding of voice and call progress tones as well as the signalling and supervision information.

20 CERDIP



FEATURES

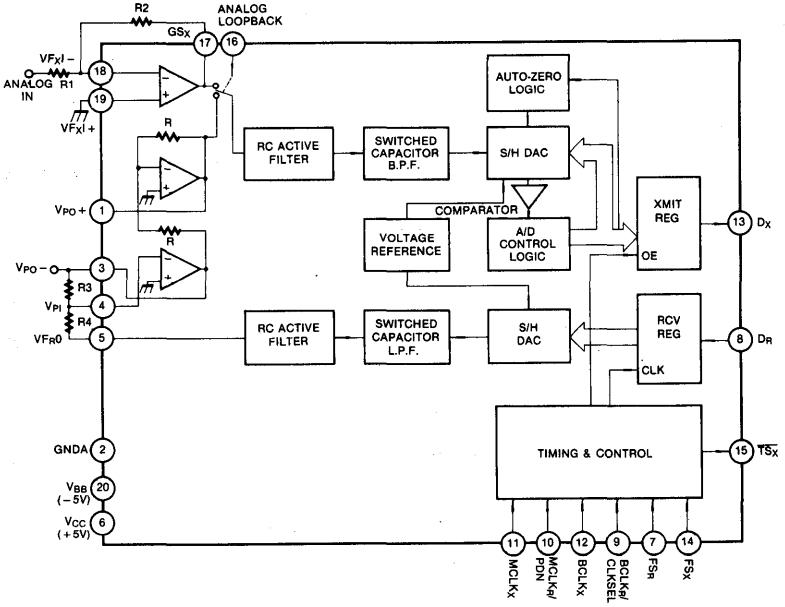
- **Complete CODEC and filtering system**
- **Meets or exceeds D3/D4 and CCITT specifications. μ-Law: KT8564 A-Law: KT8567**
- **On-chip auto zero, sample and hold and precision voltage references.**
- **Receive push-pull power amplifiers**
- **Low power dissipation: 70mW (operating) 3mW (standby)**
- **$\pm$5V operation**
- **TTL or CMOS compatible**
- **Automatic power down**

ORDERING INFORMATION

Device	Package	Operating Temperature
†KT8564N	Plastic	$-25\sim+125°C$
†KT8567N	Plastic	
KT8564J	Ceramic	
†KT8567J	Ceramic	

† Under Development

TYPICAL I-V CHARACTERISTICS



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
V_{CC} to GNDA	V_{CC}	7	V
V_{BB} to GNDA	V_{BB}	−7	V
Voltage at Any Analog Input or Output	I/O	$V_{CC}+0.3$ to $V_{BB}-0.3$	V
Voltage at Any Digital Input or Output	I/O	$V_{CC}+0.3$ to GNDA − 0.3	V
Operating Temperature Range	T_a	−25 ~ +125	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C
Lead Temperature (Soldering, 10 secs)	T_L	300	°C

4

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted: $V_{CC}=5.0V\pm5\%$, $V_{BB}=-5V\pm5\%$, GNDA = 0V, Ta = 0°C to 70°C; typical characteristics specified at $V_{CC}=5.0V$, Ta = 25°C; all signals are referenced to GNDA)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Power Dissipation						
Active Current	$I_{CC}1$	Power amplifiers active, VPI = 0V		7.0	10.0	mA
Active Current	$I_{BB}1$	Power amplifiers active, VPI = 0V		7.0	10.0	mA
Power-Down Current	I_{CCO}			0.5	1.5	mA
Power-Down Current	I_{BBO}			0.05	0.3	mA
Digital Interface						
Input Low Current	I_{IL}	$GNDA\leq V_{IN}\leq V_{IL}$, All digital inputs	−10		10	μA
Input High Current	I_{IH}	$V_{IH}\leq V_{IN}\leq V_{CC}$	−10		10	μA
Output Current in High Impedance State (TRI-STATE)	I_{OZ}	D_X, $GNDA\leq V_O\leq V_{CC}$	−10		10	μA
Input Low Voltage	V_{IL}				0.6	V
Input High Voltage	V_{IH}		2.2			V
Output Low Voltage	V_{OL}	D_X, $I_L=3.2mA$ SIG_R, $I_L=1.0mA$ $\overline{TS_X}$, $I_L=3.2mA$, Open Drain			0.4 0.4 0.4	V
Output High Voltage	V_{OH}	D_X, $I_H=-3.2mA$ SIG_R, $I_H=-1.0mA$	2.4 2.4			V
Analog Interface with Transmit Input Amplifier						
Input Leakage Current	I_IXA	$-2.5V\leq V\leq+2.5V$, VF_XI+ or VF_XI-	−200		200	nA
Input Resistance	R_IXA	$-2.5V\leq V\leq+2.5V$, VF_XI+ or VF_XI-	10			MΩ
Output Resistance	R_OXA	Closed loop, unity gain		1	3	Ω
Load Resistance	R_LXA	GS_X	10			KΩ
Load Capacitance	C_LXA	GS_X			50	pF
Output Dynamic Range	V_OXA	GS_X, $R_L\geq10K\Omega$	−2.8		+2.8	V

ELECTRICAL CHARACTERISTICS (Continued)

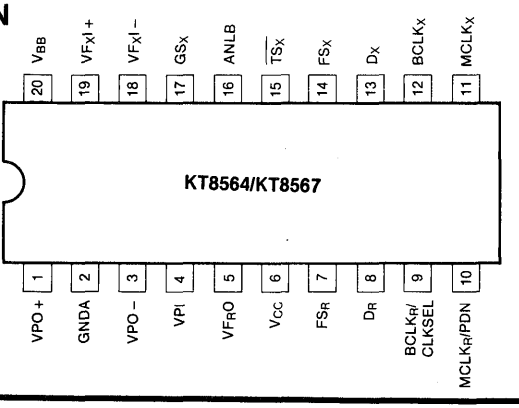
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Voltage Gain	A_VXA	VF_XI+ to GS_X	5000			V/V
Unity-Gain Bandwidth	F_UXA		1	2		MHz
Offset Voltage	$V_{OS}XA$		−20		20	mV
Common-Mode Voltage	$V_{CM}XA$	CMRRXA>60dB	−2.5		2.5	V
Common-Mode Rejection Ratio	CMRRXA	DC Test	60			dB
Power Supply Rejection Ratio	PSRRXA	DC Test	60			dB
Analog Interface with Receive Filter						
Output Resistance	R_ORF	Pin VF_RO		1	3	Ω
Output DC Offset Voltage	VOS_RO	Measure from VF_RO to GND A	−200		200	mV
Load Resistance	R_LRF	$VF_RO = \pm 2.5V$	10			KΩ
Load Capacitance	C_LRF	Connect from VF_RO to GND A			25	pF
Analog Interface with Power Amplifiers						
Input Leakage Current	IPI	$-1.0V \leq VPI \leq 1.0V \leq VPI \leq 1.0V$	−100		100	nA
Input Resistance	RIPI	$-1.0V \leq VPI \leq 1.0V$	10			MΩ
Input Offset Voltage	VI_{OS}		−25		25	mV
Output Resistance	ROP	Inverting unity gain at VPO+ or VPO−		1		Ω
Unity-Gain Bandwidth	F_C	Open loop (VPO−)		400		KHz
Load Capacitance	C_{LP}	$R_L \geq 1500\Omega$ VPO+ or $R_L = 600\Omega$ VPO− to $R_L = 300\Omega$ GNDA			100 500 1000	pF pF pF
Gain from VPO− to VPO+	GA_P+	$R_L = 300\Omega$ VPO+ to GNDA level at VPO− = −1.77Vrms (+3dBmo)		−1		V/V
Power Supply Rejection of V_{CC} or V_{BB}	$PSRR_P$	VPO− connected to VPI 0KHz−4KHz 0KHz−50KHz	 60 36			 dB dB
Frequency of Master Clock	$1/t_{PM}$	Depends on the device used and the $BCLK_R$/CLKSEL Pin $MCLK_X$ and $MCLK_R$		1.536 1.544 2.048		MHz MHz MHz
Width of Master Clock High	t_{WMH}	$MCLK_X$ and $MCLK_R$	160			ns
Width of Master Clock Low	t_{WML}	$MCLK_X$ and $MCLK_R$	160			ns
Rise Time of Master Clock	t_{RM}	$MCLK_X$ and $MCLK_R$			50	ns
Fall Time of Master Clock	t_{FM}	$MCLK_X$ and $MCLK_R$			50	ns
Set-Up Time from $BCLK_X$ High (and FS_X in Long Frame Sync Mode) to $MCLK_X$ Falling Edge	t_{SBFM}	First bit clock after the leading edge of FS_X	100			ns
Period of Bit Clock	t_{PB}		485	488	15,725	ns
Width of Bit Clock High	t_{WBH}	$V_{IH} = 2.2V$	160			ns
Width of Bit Clock Low	t_{WBL}	$V_{IL} = 0.6V$	160			ns
Rise Time of Bit Clock	t_{RB}	$t_{PB} = 480ns$			50	ns
Fall Time of Bit Clock	t_{FB}	$t_{PB} = 488ns$			50	ns

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Holding Time from Bit Clock Low to Frame Sync	t_{HBF}	Long frame only	0			ns
Holding Time from Bit Clock High to Frame Sync	t_{HOLD}	Short frame only	0			ns
Set-Up Time for Frame Sync to Bit Clock Low	t_{SFB}	Long Frame Only	80			ns
Delay Time from $BCLK_X$ High to Data Valid	t_{DBD}	Load = 150pF plus 2 LSTTL loads	0		180	ns
Delay Time to $\overline{TS_X}$ Low	t_{XDP}	Load = 150pF plus 2 LSTTL loads			140	ns
Delay Time from $BCLK_X$ Low to Data Output Disabled	t_{DEC}		50		165	ns
Delay Time to Valid Data from FS_X or $BCLK_X$, whichever Comes Later	t_{DZF}	C_L = 0pF to 150pF	20		165	ns
Set-Up Time from D_R Valid to $BCLK_{R/X}$ Low	t_{SDB}		50			ns
Hold Time from $BCLK_{R/X}$ Low to D_R Invalid	t_{HBD}		50			ns
Delay Time from $BCLK_{R/X}$ Low to SIG_R Valid	t_{DFSSF}	Load = 50pF plus 2 LSTTL loads			300	ns
Set-Up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low	t_{SF}	Short frame sync pulse (1 or 2 bit clock periods long)(Note 1)	50			ns
Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	t_{HF}	Short frame sync pulse (1 or 2 bit clock periods long)(Note 1)	100			ns
Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X of FS_R)	t_{HBFI}	Long frame sync pulse (from 3 to 8 bit clock periods long)	100			ns
Minimum Width of the Frame Sync Pulse (Low Level)	t_{WFL}	64K bit/s operating mode	160			ns

Note 1: For short frame sync timing, FS_X and FS_R must go high while their respective bit clocks are high.

PIN CONFIGURATION



TIMING DIAGRAM

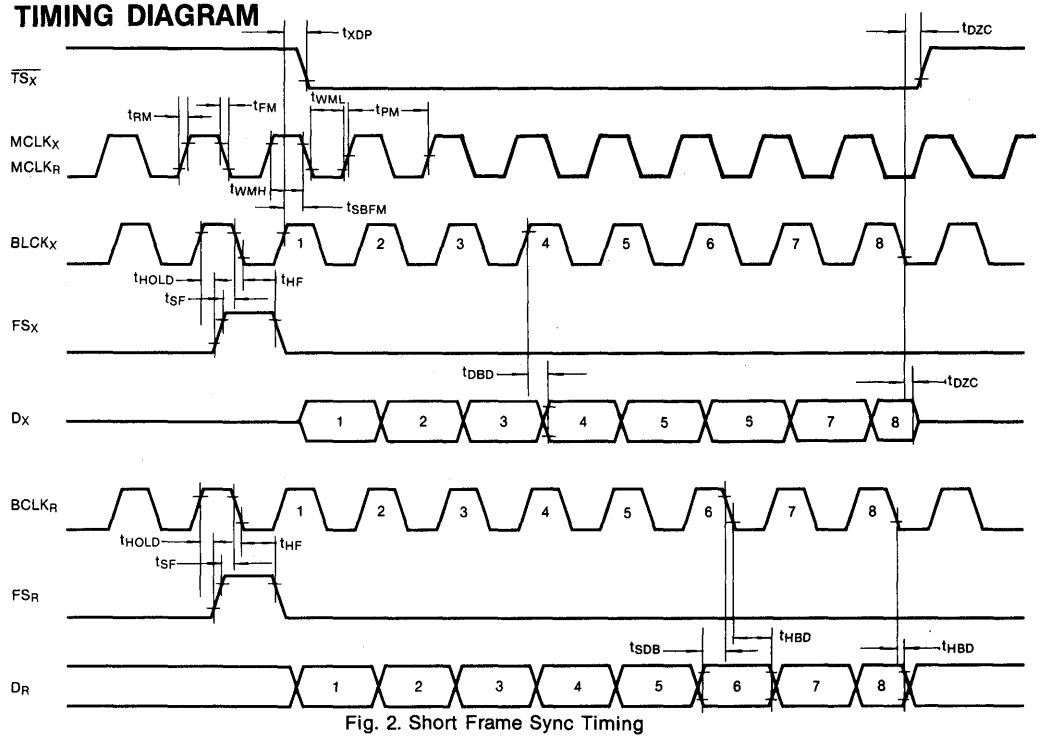


Fig. 2. Short Frame Sync Timing

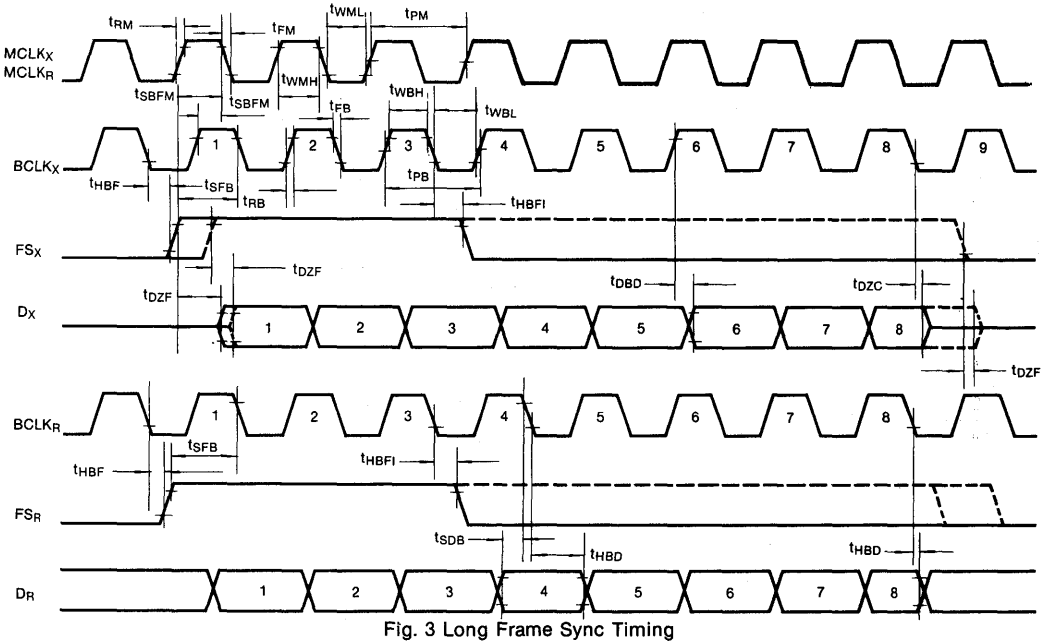


Fig. 3 Long Frame Sync Timing

PIN DESCRIPTION

Pin	Name	Function
1	VPO^+	The non-inverted output of the receive power amplifier.
2	GNDA	Analog ground. All signals are referenced to this pin.
3	VPO^-	The inverted output of the receive power amplifier.
4	VPI	Inverting input to the receive power amplifier. Also powers down both amplifiers when connected to V_{BB}.
5	VF_RO	Analog output of the receive filter.
6	V_{CC}	Positive power supply pin $V_{CC} = +5V \pm 5\%$.
7	FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R, FS_R is an 8KHz pulse train. (refer to Fig 2 and 3 for timing details)
8	D_R	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
9	$BCLK_R$/ CLKSEL	The bit clock which shifts data into D_R after the FS_R leading edge. May vary from 64KHz to 2.048MHz. Alternatively, may be a logic input which selects either 1.536MHz/1.544MHz or 2.048MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions. (see Table 1)
10	$MCLK_R$/ PDN	Receive master clock. Must be 1.536MHz or 2.048MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
11	$MCLK_X$	Transmit master clock. Must be 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with $MCLK_R$.
12	$BCLK_X$	The bit clock which shifts out the PCM data on D_X. May vary from 64KHz to 2.048MHz, but must be synchronous with $MCLK_X$.
13	D_X	The TRI-STATE PCM data output which is enabled by FS_X.
14	FS_X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data a on D_X, FS_X is an 8KHz pulse train. (refer to Fig 2, 3)
15	$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
16	ANLB	Analog loopback control input. Must be set to logic '0' for normal operation. When pulled to logic '1', the transmit filter input is dis connected from the output of the preamplifier and connected to the VPO^+ output of the receive power, amplifier.
17	GS_X	Analog output of the transmit input amplifier. Used to externally set again.
18	VF_XI^-	Inverting input of the transmit input amplifier.
19	VF_XI^+	Non-inverting input of the transmit input amplifier.
20	V_{BB}	Negative power supply pin $V_{BB} = -5V \pm 5\%$.

TRANSMISSION CHARACTERISTICS

(Unless otherwise specified: Ta = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, GNDA = 0V, f = 1.02KHz, V_{IN} = 0dBm0, transmit input amplifier connected for unity-gain non-inverting.)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
AMPLITUDE RESPONSE						
Receive Gain, Absolute	G_{RA}	Ta = 25°C, V_{CC} = 5V, V_{BB} = −5V Input = Digital code sequence for 0dBm0 signal at 1020Hz	−0.15		0.15	dB
Receive Gain, Relative to G_{RA}	G_{RR}	f = 0Hz to 3000Hz f = 3300Hz f = 3400Hz f = 4000Hz	−0.15 −0.35 −0.7		0.15 0.05 0 −14	dB dB dB dB
Absolute Receive Gain Variation with Temperature	G_{RAT}	Ta = 0°C to 70°C			±0.1	dB
Absolute Receive Gain Variation with Supply Voltage	G_{RAV}	V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%			±0.05	dB
Receive Gain Variations with Level	G_{RRL}	Sinusoidal test method; reference input PCM code corresponds to an Ideally encoded −10dBm0 signal PCM level = −40dBm0 to +3dBm0 PCM level = −50dBm0 to −40dBm0 PCM level = −55dBm0 to −50dBm0	 −0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB
Receive Filter Output at VF_RO	V_{RO}	R_L = 10Ω	−2.5		2.5	V
Absolute Levels	A_L	Nominal 0dBm0 level is 4dBm (600Ω) 0dBm0		1.2276		V_{rms}
Max Transmit Overload Level	t_{MAX}	Max transmit overload level KT8564(3.17dBm0), KT8567(3.14dBm0)		2.501 2.492		V_{PK}
Transmit Gain, Absolute	G_{XA}	Ta = 25°C, V_{CC} = 5V, V_{BB} = −5V Input at GS_X = 0dBm0 at 1020Hz	−0.15		0.15	dB
Transmit Gain, Relative to G_{XA}	G_{XR}	f = 16Hz f = 50Hz f = 60Hz f = 200Hz f = 300Hz − 3000Hz f = 3300Hz f = 3400Hz f = 4000Hz f = 4600Hz and up, measure Response from 0Hz to 4000Hz	 −1.8 −0.15 −0.35 −0.7		−40 −30 −26 −0.1 0.15 0.05 0 −14 −32	dB dB dB dB dB dB dB dB dB
Absolute Transmit Gain Variation with Temperature	G_{XAT}	Ta = 0°C to 70°C			±0.1	dB
Absolute Transmit Gain Variation with Supply Voltage	G_{XAV}	V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%			±0.05	dB
Transmit Gain Variations with Level	G_{XRL}	Sinusoldal test method Reference level = −10dBm0 VF_XI+ = −40dBm0 to +3dBm0 VF_XI+ = −50dBm0 to −40dBm0 VF_XI+ = −55dBm0 to −50dBm0	 −0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB

TRANSMISSION CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
Transmit Delay, Absolute	D_{XA}	f = 1600Hz		290	315	μs
Transmit Delay, Relative to D_{XA}	D_{XR}	f = 500Hz – 600Hz f = 600Hz – 800Hz f = 800Hz – 1000Hz f = 1000Hz – 1600Hz f = 1600Hz – 2600Hz f = 2600Hz – 2800Hz f = 2800Hz – 3000Hz		195 120 50 20 55 80 130	220 145 75 40 75 105 155	μs μs μs μs μs μs μs
Receive Delay, Absolute	D_{RA}	f = 1600Hz		180	200	μs
Receive Delay, Relative to D_{RA}	D_{RR}	f = 500Hz – 1000Hz f = 1000Hz – 1600Hz f = 1600Hz – 2600Hz f = 2600Hz – 2800Hz f = 2800Hz – 3000Hz	– 40 – 30	– 25 – 20 70 100 145	 90 125 175	μs μs μs μs μs
NOISE						
Transmit Noise, C Message Weighted	N_{XC}	$VF_XI+ = 0V$, KT8564		12	15	dBrnc0
Transmit Noise, P Message Weighted	N_{XP}	$VF_XI+ = 0V$, KT8567		– 74	– 67	dBm0p
Receive Noise, C Message Weighted	N_{RC}	PCM code equals alternating positive and negative zero, KT8564		8	11	dBrnc0
Receive Noise, P Message Weighted	N_{RP}	PCM code equals positive zero, KT8567		– 82	– 79	dBm0p
Noise, Single Frequency	N_{RS}	f = 0KHz to 100KHz, loop around measurement, $VF_XI+ = 0V_{rms}$			– 53	dBm0
Positive Power Supply Rejection, Transmit	$PPSR_X$	$VF_XI+ = 0V_{rms}$, $V_{CC} = 5.0V_{DC} + 100mV_{rms}$ f = 0KHz – 50KHz	30	35		dBC
Negative Power Supply Rejection, Transmit	$NPSR_X$	$VF_XI+ = 0V_{rms}$, $V_{BB} = -5.0V_{DC} + 100mV_{rms}$ f = 0KHz – 50KHz	40	45		dBC
Positive Power Supply Rejection, Receive	$PPSR_R$	PCM code equals positive zero $V_{CC} = 5.0V_{DC} + 100mV_{rms}$ f = 0Hz – 4000Hz f = 4KHz – 25KHz f = 25KHz – 50KHz	 35 35 35			 dBC dB dB
Negative Power Supply Rejection, Receive	$NPSR_R$	PCM code equals positive zero $V_{BB} = -5.0V_{DC} + 100mV_{rms}$ f = 0Hz – 4000Hz f = 4KHz – 25KHz f = 25KHz – 50KHz	 40 40 36			 dBC dB dB

TRANSMISSION CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious Out-of-Band Signals at the Channel Output	SOS	Loop around measurement, 0dBm0, 300Hz – 3400Hz input applied to VF_XI+, measure individual image signals at VF_RO 4600Hz – 7600Hz 7600Hz – 8400Hz 8400Hz – 100,000Hz			 – 32 – 40 – 32	 dB dB dB
Distortion						
Signal to Total Distortion	STD_X	Sinusoidal test method				
Transmit or Receive Half-Channel	STD_R	Level = 3.0dBm0 = 0dBm0 to 30dBm0 = – 40dBm0 XMT RCV = – 55dBm0 XMT RCV	33 36 29 30 14 15			dBC dBC dBC dBC dBC dBC
Single Frequency Distortion, Transmit	SFD_X				– 46	dB
Single Frequency Distortion, Receive	SFD_R				– 46	dB
Intermodulation Distortion	IMD	Loop around measurement, VF_X+ = – 4dBm0 to – 21dBm0, two frequencies in the range 300Hz – 3400Hz			– 41	dB
Crosstalk						
Transmit to Receive Crosstalk	CT_{X-R}	f = 300Hz – 3400Hz D_R = Steady PCM code		– 90	– 75	dB
Receive to Transmit Crosstalk	CT_{R-X}	f = 300Hz – 3000Hz, VF_XI = 0V		– 90	– 70 (Note 1)	dB
Power Amplifiers						
Maximum 0dBm0 Level for Better than ±0.1dB Linearity Over the Range – 10dBm0 to + 3dBm0	V_{OL}	Balanced load, R_L connected between VPO+ and VPO– R_L = 600Ω R_L = 1200Ω R_L = 30KΩ	 3.3 3.5 4.0			 Vrms Vrms Vrms
Signal/Distortion	S/Dp	R_L = 600Ω, 0dBm0	50			dB

Note 1. CT_{R-X} is measured with a – 50dBm0 activating signal applied at VF_XI+.

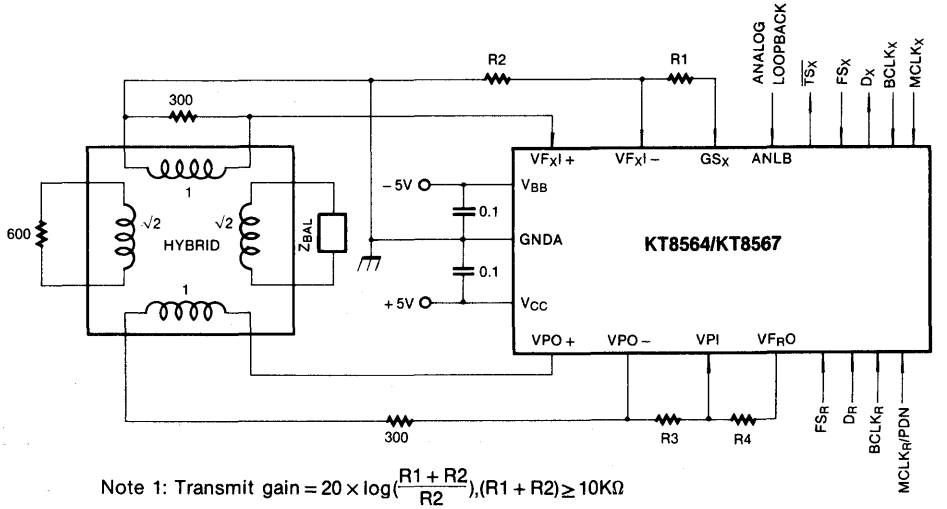
SELECTION OF MASTER CLOCK FREQUENCIES

$BCLK_R$/CLKSEL	MASTER CLOCK FREQUENCY SELECTED	
	KT8564	KT8567
Clocked	1.536MHz or 1.544MHz	2.048MHz
0	2.048MHz	1.536MHz or 1.544MHz
1 (or open circuit)	1.544MHz	2.048MHz

ENCODING FORMAT AT Dx OUTPUT

	KT8564 (μ-Law)	KT8567 (A-Law, Includes Even Bit Inversion)
V_{IN} = + Full Scale	1 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0
V_{IN} = 0V	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
V_{IN} = – Full Scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0

APPLICATION CIRCUIT



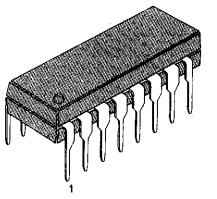
Note 1: Transmit gain $= 20 \times \log(\frac{R1+R2}{R2}), (R1+R2) \geq 10K\Omega$

Note 2: Receive gain $= 20 \times \log(\frac{2 \times R3}{R4}), R4 \geq 10K\Omega$

4 x 4 CROSSPOINT SWITCH WITH CONTROL MEMORY

The KT8592 contains 4 x 4 matrix-array with 16 latches. Any one of 16 switches can be selected by applying its address to the device and a pulse to the strobe input pin. The selected switch can be turned on or off by applying a logical one or zero to the data in and the strobe input at logical one.

16 DIP



FEATURES

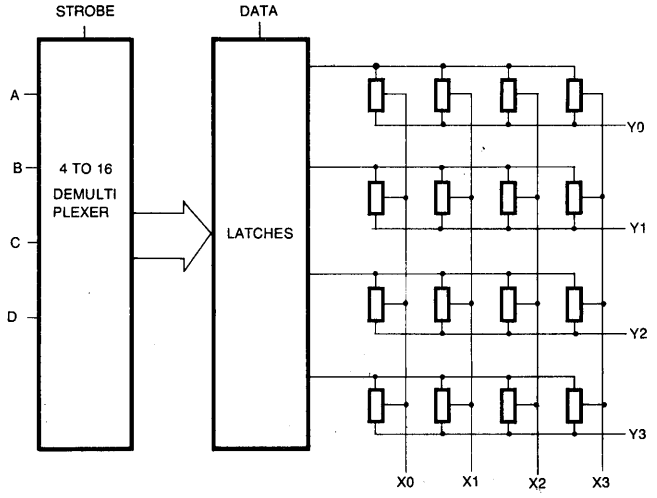
- **Low on resistance (Typ: 75Ω at V_{DD} = 12V)**
- **Internal control latches**
- **$2V_{PP}$ analog signal capability**
- **High linearity: 0.5% distortion (Typ) at f = 1KHz, $V_{IN} = 5V_{P-P}$, V_{DD} = 10V, R_L = 1KΩ**

ORDERING INFORMATION

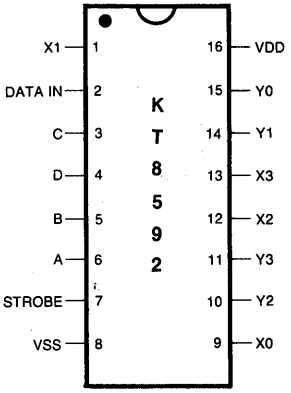
Device	Package	Operating Temperature
†KT8592N	16DIP	−40 ~ +85°C

† Under Development

BLOCK DIAGRAM



PIN CONFIGURATION



INPUT/OUTPUT DESCRIPTION

I/O	Lavel	Pin No.	
POWER			
I	V_{DD}	16	Positive power supply
I	V_{SS}	8	Negative power supply
ADDRESS			
I	A, B	6, 5	X Address lines. These 2 pins are used to select one of the 4 rows of switches. Refer to the thruth table.
I	C, D	3, 4	Y Address lines. These 2 pins are used to select one of the 4 columns of switchs. Refer to the thruth table.
CONTROL			
I	Data	2	This input determines if the selected switch will be turned On (closed) or Off (opened). If the pin is held high. The selected switch will be closed. If the pin is held low, the switch will be opened.
I	Strobe	7	This pin enables whatever action is selected by the address and data in pins. When the strobe pin is held low, no switch openings or closings take place. When the strobe pin is holding high. The switch addressed by the selected lines will be opened or closed. (Depending upon the state of the data in pin)
DATA			
I/O	X0-X3	9,1,12,13	Analog input/outputs. These pins are connected to the rows of the switch matrix.
I/O	Y0-Y3	15,14,10,11	Analog input/outputs. These pins are connected to the columns of the switch matrix.

TRUTH TABLE

ADDRESS				CONNECTIONS
A	B	C	D	
0	0	0	0	X0 – Y0
1	0	0	0	X1 – Y0
0	1	0	0	X2 – Y0
1	1	0	0	X3 – Y0
0	0	1	0	X0 – Y1
1	0	1	0	X1 – Y1
0	1	1	0	X2 – Y1
1	1	1	0	X3 – Y1
0	0	0	1	X0 – Y2
1	0	0	1	X1 – Y2
0	1	0	1	X2 – Y2
1	1	0	1	X3 – Y2
0	0	1	1	X0 – Y3
1	0	1	1	X1 – Y3
0	1	1	1	X2 – Y3
1	1	1	1	X3 – Y3

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.5 ~ +20	V
Input Voltage, All Inputs	V_{IN}	−0.5 ~ V_{DD} + 0.5	V
Input Current (Analog Inputs)	I_{IN}	±10	mA
Power Dissipation	P_D	500	mW
Operating Temperature Range	Ta	−40 ~ +85	°C
Storage Temperature Range	Tstg	−65 ~ +150	°C

DC ELECTRICAL CHARACTERISTICS

Characteristic	Test Conditions	V_{IN} (V)	V_{DD} (V)	Values −40°C	Values 85°C	Values 25°C Min	Values 25°C Typ	Values 25°C Max	Unit
CROSSPOINTS									
I_{DD}, Quiescent Current			5 10 15	5 10 20	150 300 600		0.04 0.04 0.04	5 10 20	uA
Ron, ON Resistance	Any Switch Vis = 0 to V_{DD}		5 10 12 15	1000 145 110 75	1440 205 155 110		225 85 75 65	1250 180 135 95	Ω
△Ron, △ON Resistance	Between Any Two Switches		5 10 12 15				35 20 18 15		Ω
I_L, OFF Switch Leakage Current	All Switches OFF	0/18	18	±100	±1000		±1	±100	nA
CONTROLS									
V_{IL}, Input Low Voltage	OFF Switch I_L < 0.2 uA		5 10 15	1.5 3 4				1.5 3 4	V
V_{IH}, Input High Voltage	ON Switch see Ron Charac.		5 10 15	3.5 7 11		3.5 7 11			V
I_{IN}, Input Current	Any Control	0/18	18	±0.1	±1		$\pm 10^{-5}$	±0.1	uA

AC ELECTRICAL CHARACTERISTICS (Ta = 25°C)

Characteristic	Test Conditions	f_I (KHz)	R_L (KΩ)	V_{IS} (V)	V_{DD} (V)	Values Min	Values Typ	Values Max	Unit
CROSSPOINTS									
t_{PHL}, t_{PLH}, Propagation Delay Time (Switch ON) Signal Input to Output	C_L = 50pF t_r, t_f = 20ns Fig. 2		10	5 10 15	5 10 15		30 15 10	60 30 20	ns
Frequency Response (Any Switch ON) 20 log (V_{OS}/V_{IS}) = −3dB	Sine Wave Input	1	1	5	10		40		MHz
Sine Wave Distortion		1	1	5	10		0.5		%
Feedthrough (All Switches OFF)	Sine Wave Input Fig. 3	1.6	1	5	10		−80		dB
Frequency for Signal Crosstalk Attenuation of 40dB Attenuation of 110dB	Sine Wave Input		1	10	10		 1.5 0.1		 MHz KHz
C, Capacitance Xn to Ground Yn to Ground Feedthrough					 5 ~ 15 5 ~ 15		 18 30 0.4		pF
CONTROLS				See Fig.					
Propagation Delay Time t_{PHZ} Strobe to Output (Switch Turn on to High Level)	R_L = 1KΩ C_L = 50pF t_r, t_f = 20ns			5	5 10 15		300 125 80	600 250 160	ns
t_{PZH} Data in to Output (Turn on to High Level)				6	5 10 15		110 40 25	220 80 50	
t_{PZH} Address to Output (Turn on to High Level)				7	5 10 15		350 135 90	700 270 180	
Propagation Delay Time t_{PHZ} Strobe to Output (Switch Turn OFF)				5	5 10 15		165 85 70	330 170 140	
t_{PHL} Data in to Output (Turn on to Low Level)				6	5 10 15		210 110 100	420 220 200	ns
t_{PHZ} Address to Output (Turn OFF)				7	5 10 15		435 210 160	870 420 320	

AC ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Test Conditions	R_L (KΩ)	V_{IS} (V)	See Fig.	V_{DD} (V)	Values Min	Values Typ	Values Max	Unit
t_{SU}, Setup Time Data in to Strobe, Address	$R_L = 1K\Omega$, $C_L = 50pF$ t_r, $t_f = 20ns$				5		95	190	ns
				5	10		25	50	
				7	15		15	30	
t_H, Hold Time Data in to Strobe, Address					5		180	360	
				5	10		110	220	
				7	15		35	70	
f_0, Switching Frequency					5	0.6	1.2		MHz
					10	1.6	3.2		
					15	2.5	5		
t_W, Strobe Pulse Width					5		300	600	ns
					10		120	240	
					15		90	180	
Control Crosstalk Data In, Address or Strobe to Output	Square Wave Input t_r, $t_f = 20ns$	10	10		10		75		mV (Peak)
C_{IN}, Input Capacitance	Any Control Input						5	7.5	pF

TEST CIRCUIT

FIG. 1 Ron MEASUREMENT

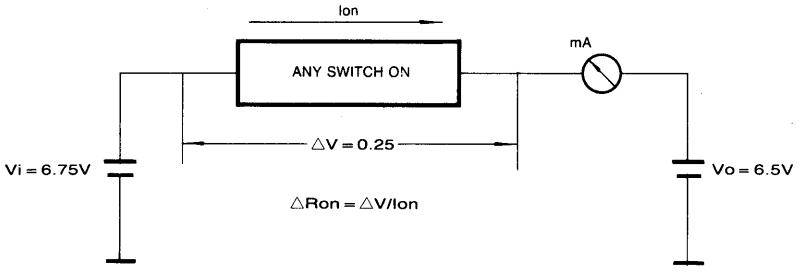
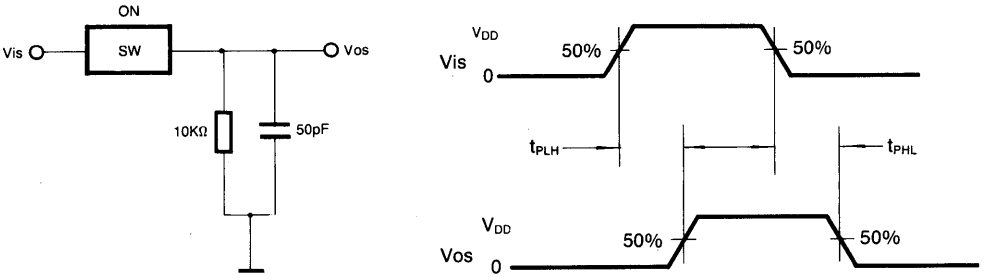


FIG. 2 PROPAGATION DELAY TIME & WAVEFORMS (SIGNAL INPUT TO SIGNAL OUTPUT, SWITCH ON)



SW = ANY CROSSPOINT
STROBE = DATA IN = V_{DD}

FIG. 3 OFF ISOLATION MEASUREMENT (FEEDTHROUGH)

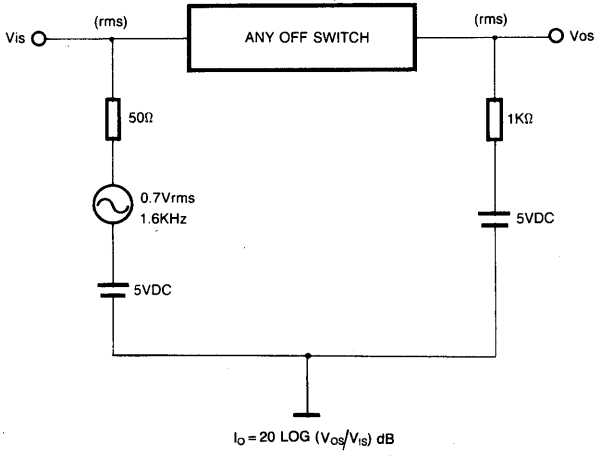


FIG. 4 CROSSTALK MEASUREMENT

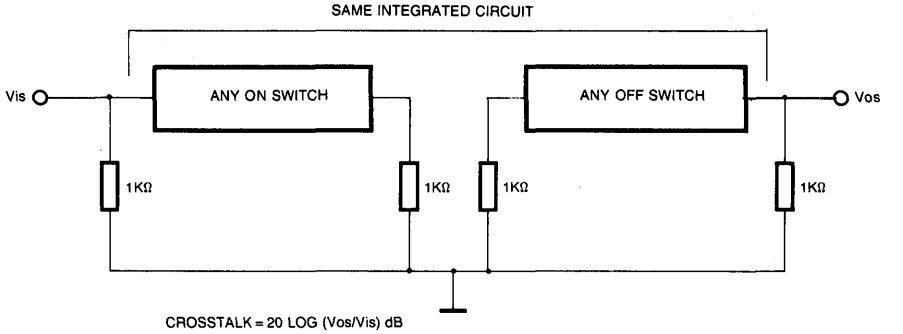


FIG. 5 PROPAGATION DELAY TIME & WAVEFORMS (STROBE TO SIGNAL OUTPUT, SWITCH TURN ON OR TURN OFF)

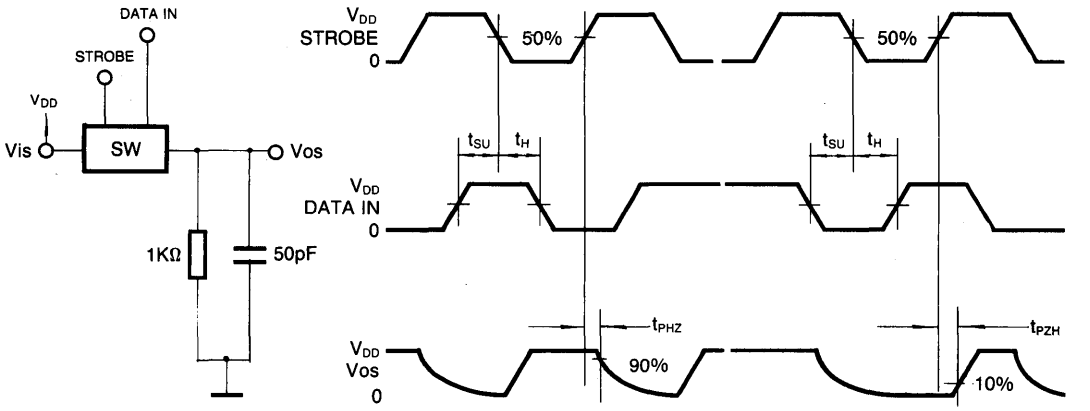
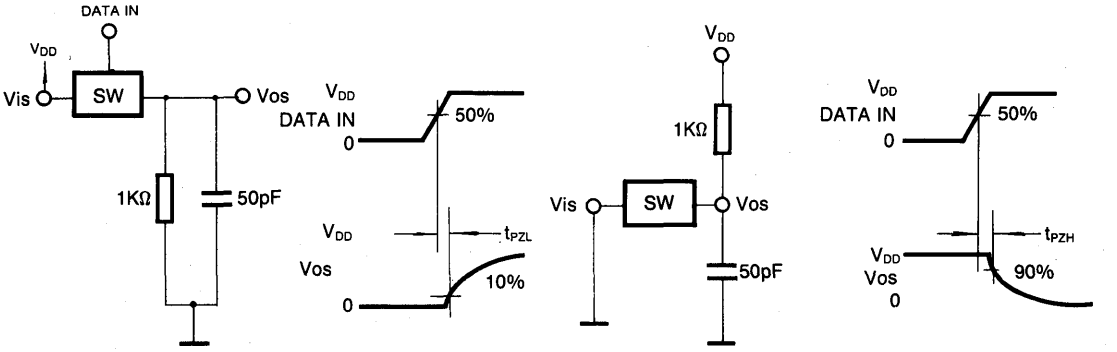


FIG. 6 PROPAGATION DELAY TIME & WAVEFORMS (STROBE TO SIGNAL OUTPUT, SWITCH TURN ON TO HIGH or LOW LEVEL)



SW = ANY CROSSPOINT
STROBE = V_{DD}

FIG. 7 PROPAGATION DELAY TIME & WAVEFORMS (ADDRESS TO SIGNAL OUTPUT, SWITCH TURN ON or TURN OFF)

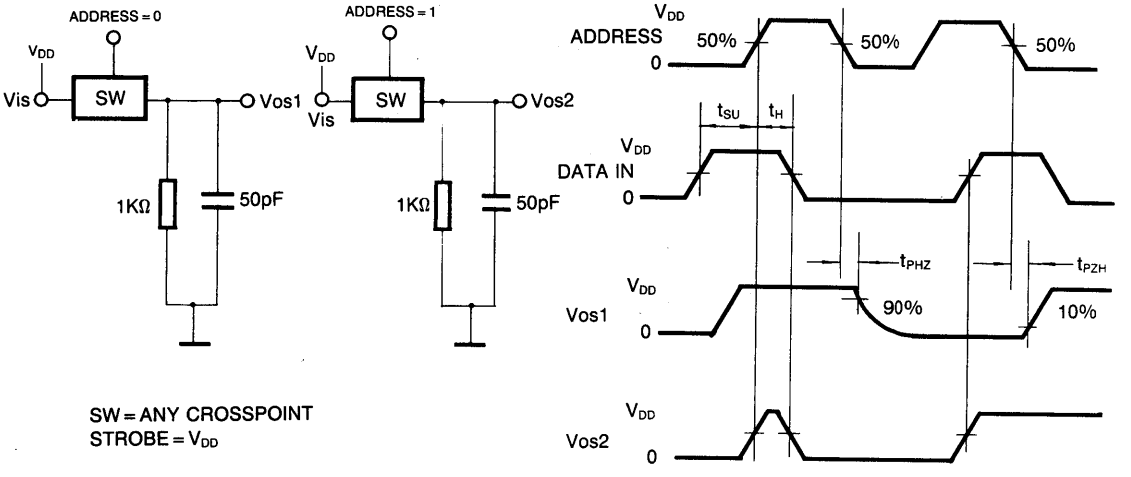
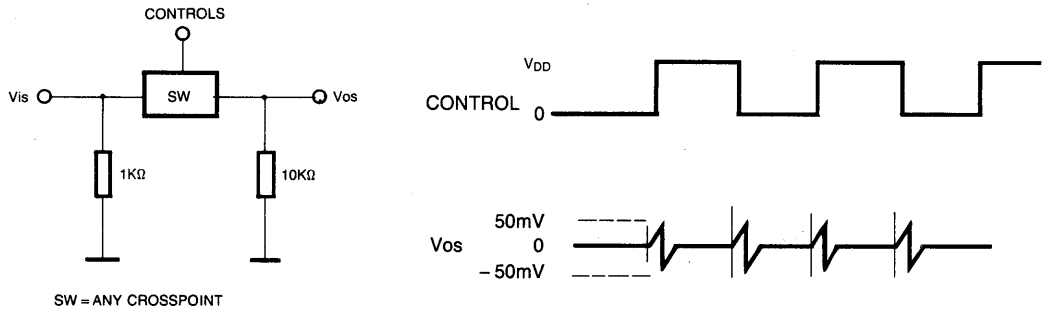
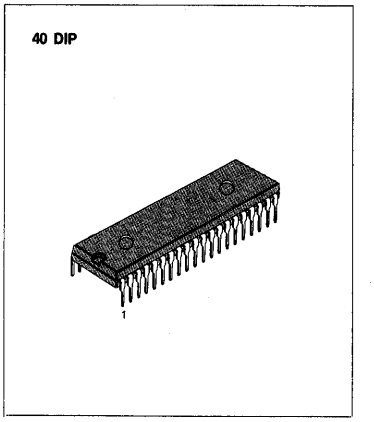


FIG. 8 WAVEFORMS FOR CROSSTALK (CONTROL INPUT TO SIGNAL OUTPUT)



12 x 8 CROSSPOINT SWITCH WITH CONTROL MEMORY

The KT8593 contains a 12 x 8 array of crosspoint switch with a 7 to 96 line decoder and latch circuits. Anyone of 96 switches can be selected by applying the appropriate 7 input bits. The selected switch can be turned on or off by applying a logical one or zero to the data in and the strobe input at logical one. A reset signal can be used to turn off all the switches together when is switched at logical one. Logic inputs are TTL compatible.



FEATURES

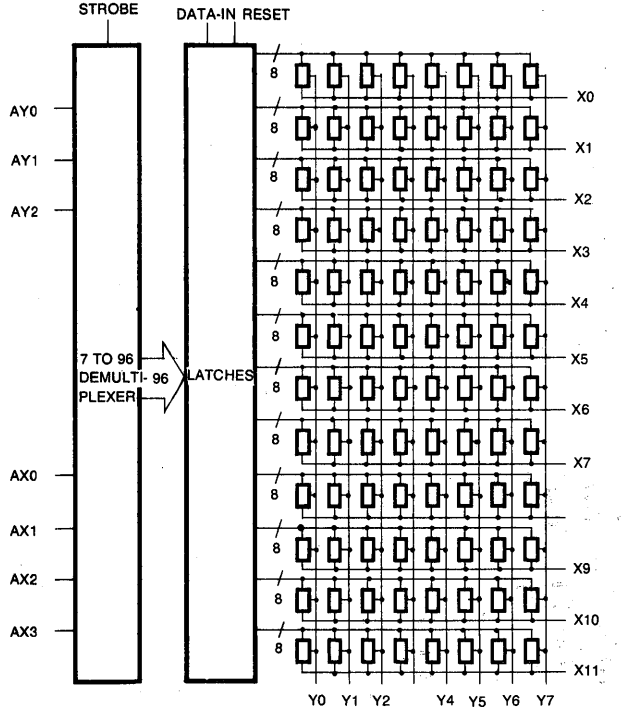
- **Low on Resistance (Typ: 35Ω at V_{DD} = 14V)**
- **Internal Control Latches**
- **2 V_{PP} Analog Signal Capability**
- **Less than 1% Total Distortion at 0 dBm**

ORDERING INFORMATION

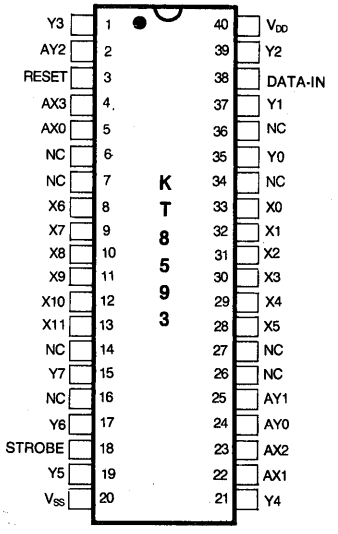
Device	Package	Operating Temperature
†KT8593N	40DIP	0~70°C

† Under Development

BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	$-0.5 \sim 18$	V
Input Voltage Range	V_{IN}	$-0.5 \sim V_{DD}+0.5$	V
Input Current (Analog Input)	I_{IN}	± 12	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_a	$0 \sim 70$	°C
Storage Temperature Range	T_{stg}	$-50 \sim 125$	°C

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RECOMMENDED OPERATING CONDITION

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	$10 \sim 16$	V
Operating Temperature	T_a	$0 \sim 70$	°C
Input Logic Level	V_{IN}	$0 \sim V_{DD}$	V

DC ELECTRICAL CHARACTERISTICS ($Ta = 0$ to 70°C, $V_{DD} = 14V$)

Characteristic	Test Condition	Min	Typ	Max	Unit
CROSSPOINT					
Operating Current	$f_O = 100$ KHz			35	mA
ON Resistance	$V_{IDC} = 6.75V$ $V_{ODC} = 6.5V$ (Fig. 1)		35	75	Ω
△R on Between any 2 Switch			6	10	Ω
OFF Leakage	All Switches OFF $V_{os} = V_{is} = 0$ to V_{DD}		1	±500	nA
CONTROLS					
V_{IL}				0.8	V
V_{IH}		2.4			V
Input Leakage			0.1	±3	nA

AC ELECTRICAL CHARACTERISTICS ($T_a = 25°C$, $C_L = 50pF$, t_r, $t_f = 20nS$, $V_{DD} = 14V$)

Characteristic		Test Conditions					Values			Unit
		fi (KHz)	R_L (KΩ)	V_{is} (V_{PP})	V_{DC} (V)	Note	Min	Typ	Max	
CROSSPOINTS										
t_{PHL}, t_{PLH}	Propagation delay time (Switch ON) signal input to output		1	2	5	Fig. 2		10	40	nS
	Frequency response (Any switch ON) 20 log (V_{os}/V_{is}) = − 3dB		0.091	2	5	C_L = 3pF		50		MHz
	Sine wave distortion	1000	0.091	2	5				1	%
	Feedthrough (All switches OFF)	10	1	2	5	Fig. 3	− 90			dB
	Frequency for signal crosstalk Attenuation of 40dB Attenuation of 110dB		1	2	5	Fig. 4	1 5			MHz KHz
C	Capacitance X_n to ground							15		
	Y_n to ground	1000		0.1	5			15		pF
	Feedthrough							0.4		
C	Capacitance Logic input to ground	1000		0.1	5			5		pF

Characteristic		Test Conditions			Values			Unit
			See Fig.	V_{DD} (V)	Min	Typ	Max	
CONTROLS								
t_{PSN}	Propagation delay time Strobe to output (Switch Turn-ON)	R_L = 1KΩ, C_L = 50pF t_r, t_f = 20nS	5	14		150	200	nS
t_{PZH}	Data-In to Output (Turn-ON to High Level)		6	14		100	150	nS
t_{PAN}	Address to Output (Turn-ON to High Level)		7	14		150	200	nS
T_{PSF}	Propagation delay time Strobe to Output (Switch Turn-OFF)		5	14		150	200	nS
t_{PZL}	Data-In to Output (Turn-ON to Low Level)		6	14		100	150	nS

AC ELECTRICAL CHARACTERISTICS (Continued)

Characteristic		Test Conditions	See Fig.	V_{DD} (V)	Values Min	Values Typ	Values Max	Unit
t_{PAF}	Address to Output (Turn-OFF)	$R_L = 1K\Omega$, $C_L = 50pF$ $t_r, t_f = 20nS$	7	14		150	200	nS
t_{ss}	Set-Up time Data-In to Strobe		5	14	20			nS
t_{SH}	Hold time Data-In to Strobe		5	14	20			nS
t_{AS}	Set-Up time Data-In to Address		7	14	20			nS
t_{AH}	Hold time Data-In to Address		7	14	20			nS
f_S	Switching Frequency			14		1		MHz
t_W	Strobe Pulse Width			14	40			nS
	Control Crosstalk Data-In, Address, or Strobe to Output	Square wave input $V_{IN} = 3V$, $R_L = 10K\Omega$ $t_r, t_f = 20nS$	8	14		75		mV
t_W	Reset Pulse Width	$R_L = 1K\Omega$, $C_L = 50pF$ $t_r, t_f = 20nS$	9	14	40			nS
t_{PHZ}	Reset Turn-OFF Delay		9	14		150	200	nS

4

TEST CIRCUITS

FIG. 1. RON MEASUREMENT

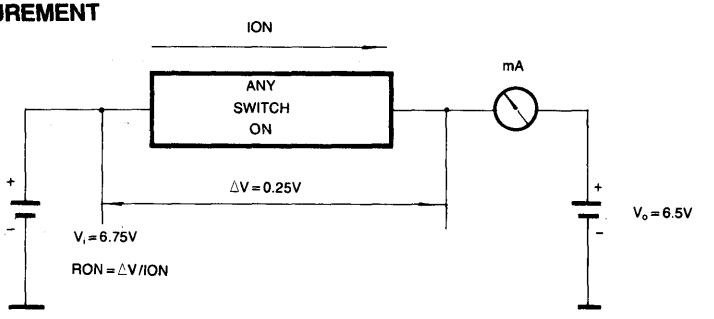
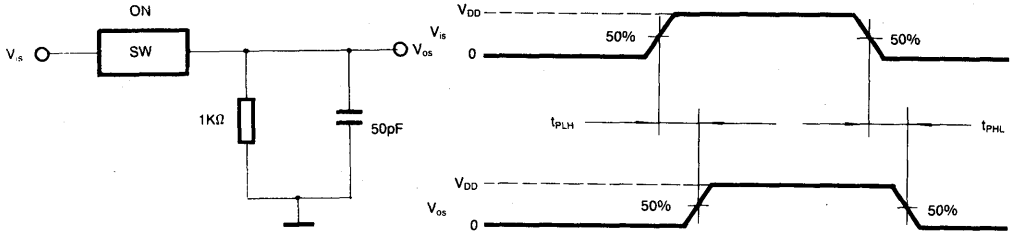
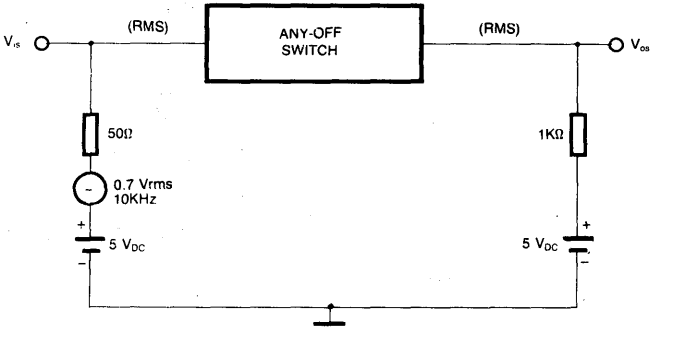


FIG. 2. PROPAGATION DELAY TIME & WAVEFORMS (SIGNAL INPUT TO SIGNAL OUTPUT, SWITCH ON)



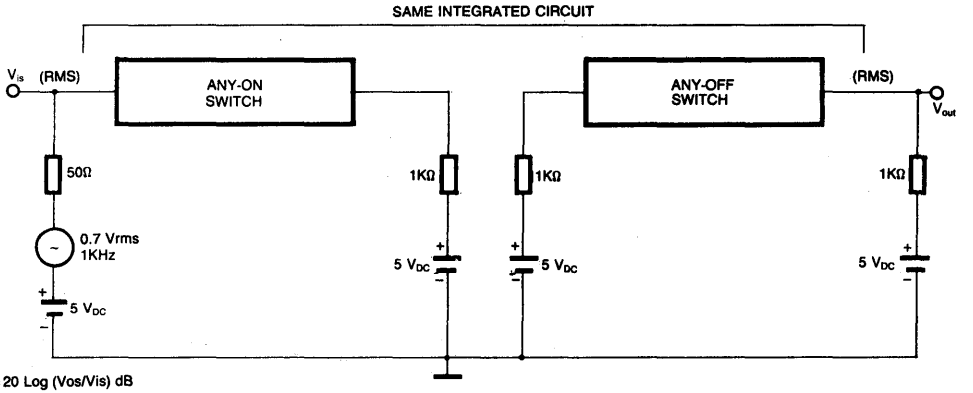
SW = ANY CROSSPOINT
STROBE = DATA-IN = V_{DD}

FIG. 3. OFF ISOLATION MEASUREMENT (FEED THROUGH)



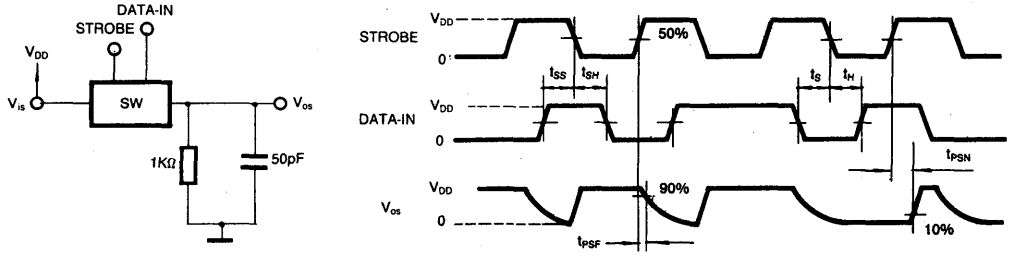
I_O = 20 Log(Vos/Vis) dB

FIG. 4. CROSSTALK MEASUREMENT



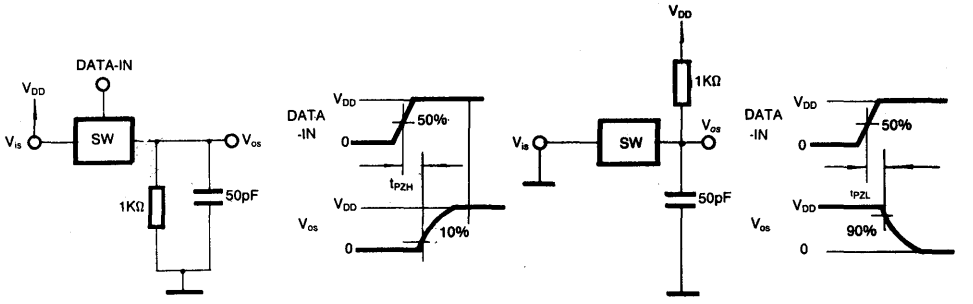
CT = 20 Log (Vos/Vis) dB

FIG. 5. PROPAGATION DELAY TIME & WAVE FORMS (STROBE TO SIGNAL OUTPUT, SWITCH TURN-ON OR TURN-OFF)



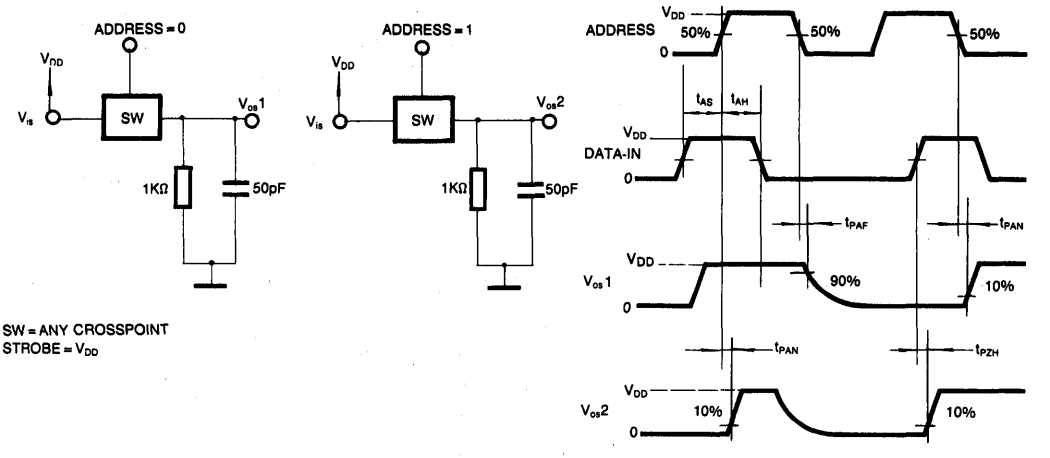
SW = ANY CROSSPOINT

FIG. 6. PROPAGATION DELAY TIME & WAVE FORMS (DATA-IN SIGNAL OUTPUT, SWITCH TURN ON TO HIGH OR LOW LEVEL)



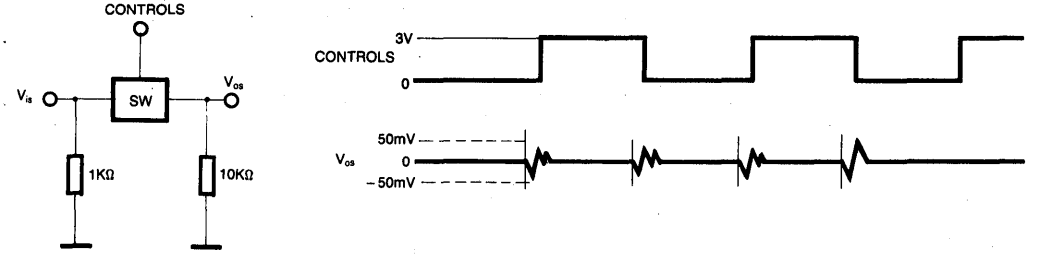
SW = ANY CROSSPOINT
STROBE-V_{DD}

FIG. 7. PROPAGATION DELAY TIME & WAVE FORMS (ADDRESS TO SIGNAL OUTPUT, SWITCH TURN-ON OR TURN-OFF)



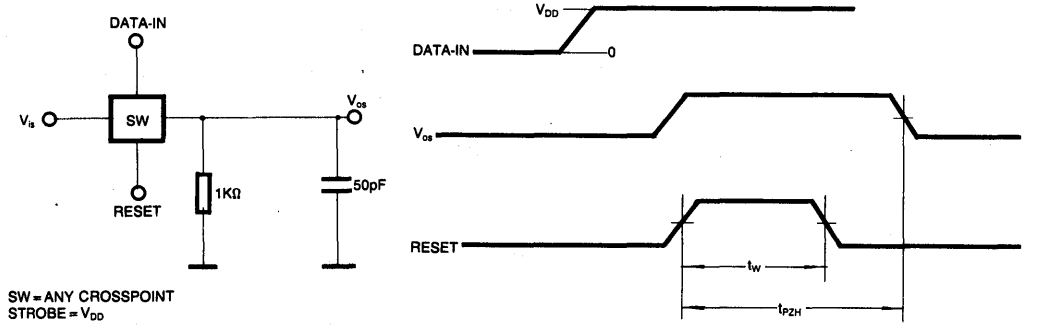
SW = ANY CROSSPOINT
STROBE = V_{DD}

FIG. 8. WAVE FORMS FOR CROSSTALK (CONTROL INPUT TO SIGNAL OUTPUT)



SW = ANY CROSSPOINT

FIG. 9. PROPAGATION DELAY TIME & WAVE FORM (RESET TO OUTPUT SIGNAL)



SW = ANY CROSSPOINT
STROBE = V_{DD}

TRUTH TABLE

Address							Connections
AX0	AX1	AX2	AX3	AY0	AY1	AY2	
0	0	0	0	0	0	0	X0 – Y0
1	0	0	0	0	0	0	X1 – Y0
0	1	0	0	0	0	0	X2 – Y0
1	1	0	0	0	0	0	X3 – Y0
0	0	1	0	0	0	0	X4 – Y0
1	0	1	0	0	0	0	X5 – Y0
0	1	1	0	0	0	0	No Connection
1	1	1	0	0	0	0	No Connection
0	0	0	1	0	0	0	X6 – Y0
1	0	0	1	0	0	0	X7 – Y0
0	1	0	1	0	0	0	X8 – Y0
1	1	0	1	0	0	0	X9 – Y0
0	0	1	1	0	0	0	X10 – Y0
1	0	1	1	0	0	0	X11 – Y0
0	1	1	1	0	0	0	No Connection
1	1	1	1	0	0	0	No Connection
0	0	0	0	1	0	0	X0 – Y1
↓	↓	↓	↓	↓	↓	↓	↓
1	0	1	1	1	0	0	X11 – Y1
0	0	0	0	0	1	0	X0 – Y2
↓	↓	↓	↓	↓	↓	↓	↓
1	0	1	1	0	1	0	X11 – Y2
0	0	0	0	1	1	0	X0 – Y3
↓	↓	↓	↓	↓	↓	↓	↓
1	0	1	1	1	1	0	X11 – Y3
0	0	0	0	0	0	1	X0 – Y4
↓	↓	↓	↓	↓	↓	↓	↓
1	0	1	1	0	0	1	X11 – Y4
0	0	0	0	1	0	1	X0 – Y5
↓	↓	↓	↓	↓	↓	↓	↓
1	0	1	1	1	0	1	X11 – Y5
0	0	0	0	0	1	1	X0 – Y6
↓	↓	↓	↓	↓	↓	↓	↓
1	0	1	1	0	1	1	X11 – Y6
0	0	0	0	1	1	1	X0 – Y7
↓	↓	↓	↓	↓	↓	↓	↓
1	0	1	1	1	1	1	X11 – Y7

Address Not Allowed

INPUT/OUTPUT DESCRIPTION

I/O	Label	Pin No.	Description
POWER			
I	V_{DD}	40	Positive power supply
I	V_{SS}	20	Negative power supply
ADDRESS			
I	AX0 – AX3	4, 5, 22, 23	X address lines. These 4 pins are used to select one of the 12 rows of switches. Refer to the truth table
I	AY0 – AY2	2, 24, 25	Y address lines. These 3 pins are used to select one of the 8 columns of switches. Refer to the truth table
CONTROL			
I	Data In	38	This input determines if the selected switch will be turned ON (closed) or OFF (opened). If the pin is held high, the selected switch will be closed. If the pin is held low, the switch will be opened.
I	Strobe	18	This pin enables whatever action is selected by the address and data pins. When the strobe pin is held low, no switch openings or closings take place. When the strobe pin is helding high, the switch addressed by the select lines will be opened or closed (depending upon the state of the data-in pin)
I	Reset	3	Master reset. This pin turns OFF (opens) all 96 switches. The states of the above control lines are irrelevent this pin is active high.
DATA			
I/O	X0 – X11	8 – 13, 28 – 33	Analog input/outputs. These pins are connected to the rows of the switch matrix.
I/O	Y0 – Y7	1, 15, 17, 19, 21, 35, 37, 39	Analog input/outputs. These pins are connected to the columns of the switch matrix.

TYPICAL APPLICATIONS

Although the KT8593 allows switching 96 possible signal paths, it is not limited to applications of only an 8 x 12 x 1 configuration. Figure 1 shows a method of addressing 4 separate KT8593's. In this example, the RESET, DATA-IN, and ADDRESS lines are connected in parallel for the four devices. The logic for lines A, B and STROBE go to a 2-line to 4-line decoder with the STROBE used to both enable and clock the data. This decode (or a wider one) could be easily implemented with a single programmable logic device.

Figure 2 shows a case where both the X and Y lines have been expanded. This may be useful for applications where several different source/destination paths need to be controlled by a single controller. The A and B lines are decoded to select the desired device.

In Figure 3, the Y-lines of all devices are connected in parallel to allow an 8 x 48 x 1 switch configuration. The A and B inputs become in effect an extension of the X-address line. This could also be used to make a 32 x 12 x 1 matrix by trying the X-lines in parallel with the A and B inputs used as Y-address lines.

Figure 4 shows an application where switches in 2 devices are connected at the same time. This would be useful in applications requiring the switching of differential signals.

Figure 1.

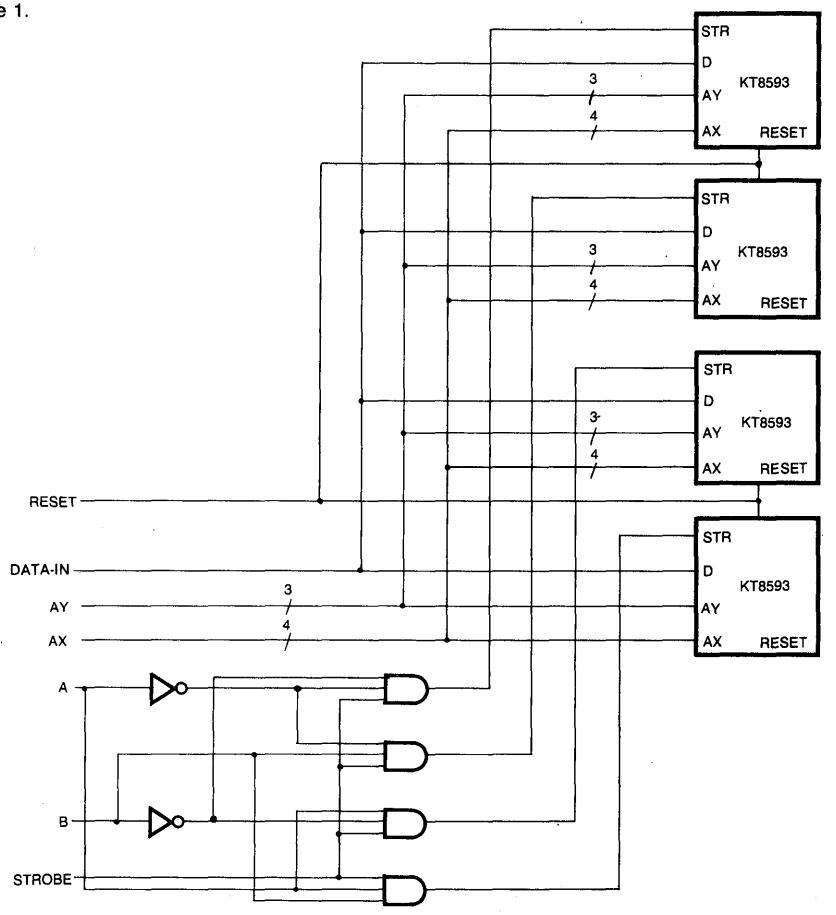


Figure 2.

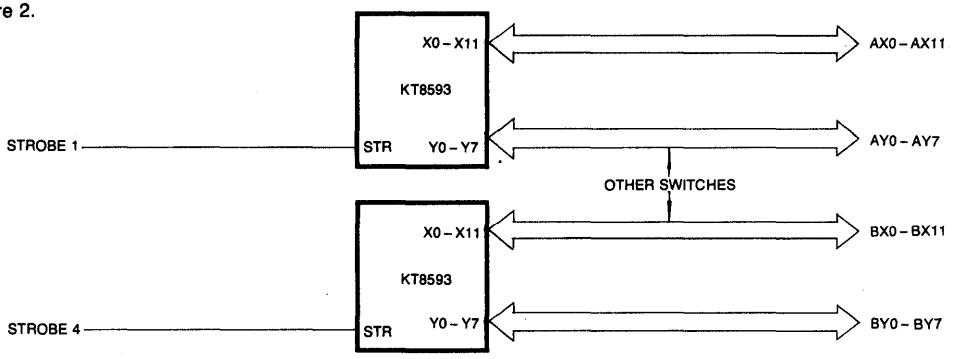


Figure 3.

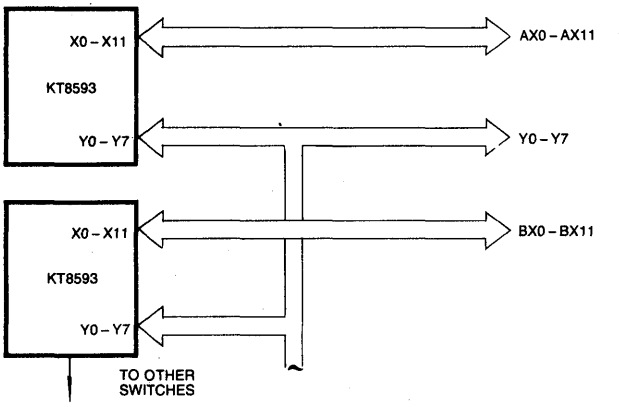
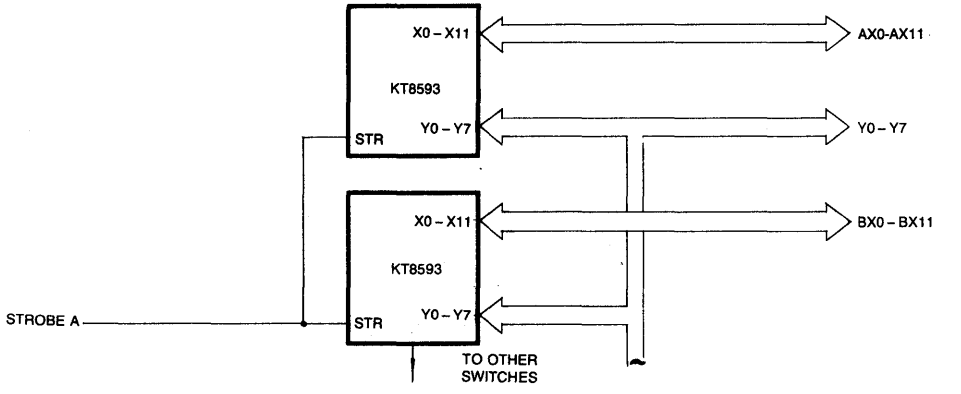
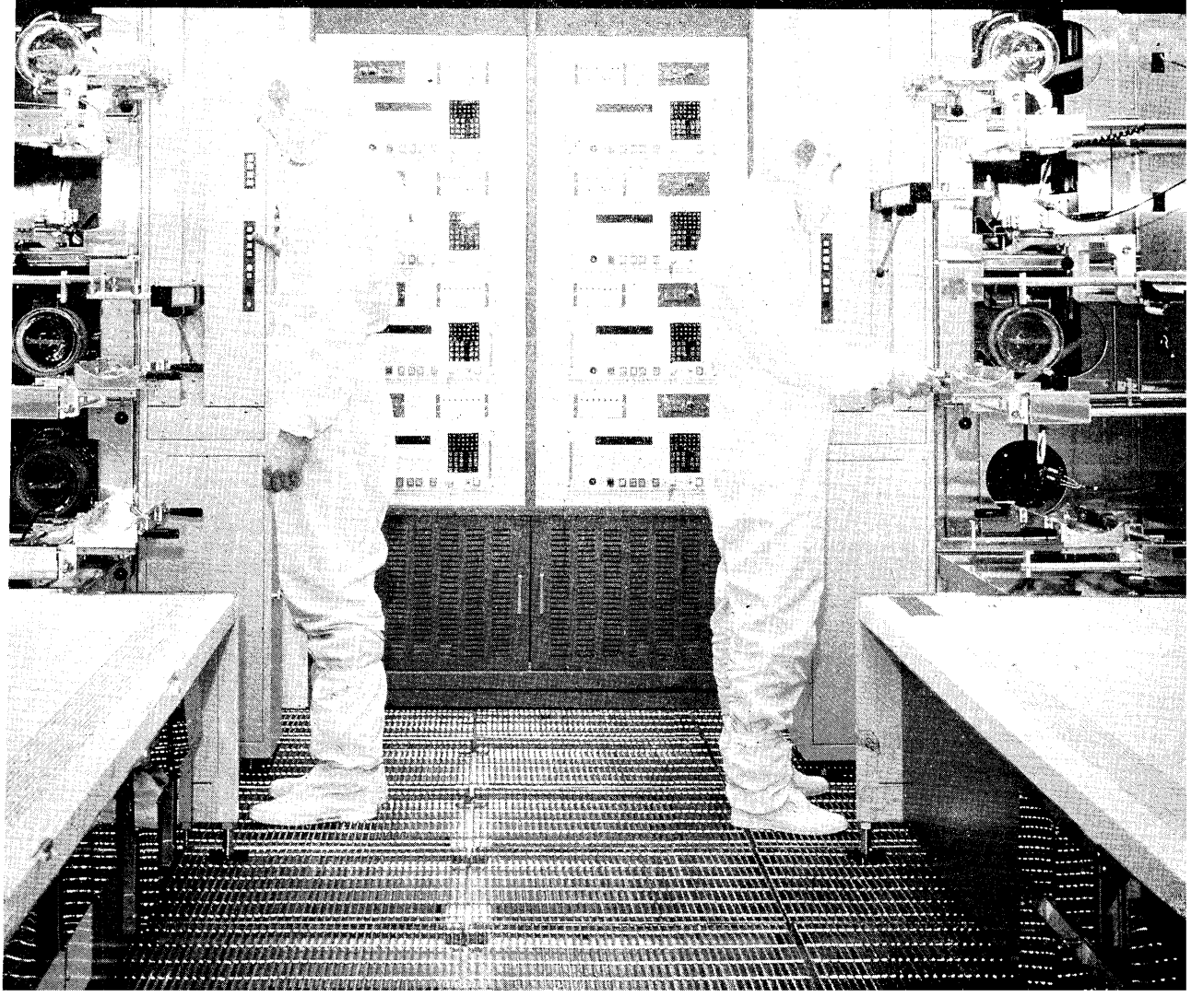


Figure 4.



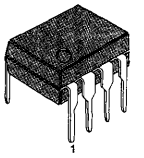
INTERFACE ICs 5



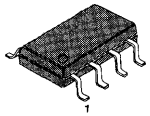
LINE DRIVER AND RECEIVER

The KA2654 is a monolithic one line driver and one line receiver designed to interface DTE (Data Terminal Equipment) with DCE (Data Communication Equipment) in conformance with the specifications of EIA standard No.RS-232C.
The driver is similar to the MC1488. The receiver is similar to the MC1489 and that a separate response control terminal is provided for.
A resistor or a resistor and bias voltage can be connected between this terminal and ground to shift the input threshold voltage level. An external capacitor can be connected from terminal to ground to provide input noise filtering.

8 DIP



8 SOP



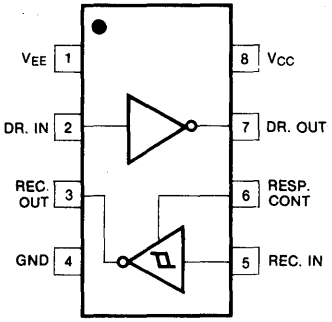
FEATURES

- **Meet specifications of EIA RS-232C**
- **Current limited output: 12mA (Typ)**
- **Wide supply voltage: ±4.5 ~ ±15V**
- **Low power consumption: 117mW**
- **Power off source impedance: 300 ohms**
- **Response Control Provides**
- **Receiver output compatible with TTL**

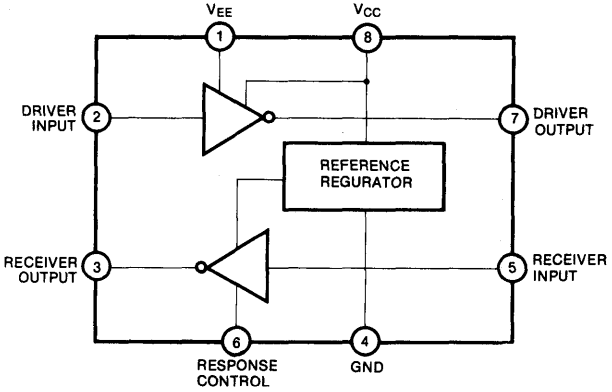
ORDERING INFORMATION

Device	Package	Operating Temperature
KA2654N	8 DIP	−20 ~ +85°C
KA2654D	8 SOP	−20 ~ +70°C

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C, unless otherwise noted)

Characteristic		Symbol	Value	Unit
Positive Supply Voltage		V_{CC}	−0.4 ~ +18	V
Negative Supply Voltage		V_{EE}	0.4 ~ −18	V
Input Voltage Range of Driver		V_{ird}	−5 ~ 18	V
Input Voltage Range of Receiver		V_{irr}	−30 ~ 30	V
Output Voltage Range of Driver		V_{ord}	−25 ~ 25	V
Output Voltage Range of Receiver		V_{orr}	−0.4 ~ 7	V
Output Current of Driver		I_{cd}	50	mA
Response Control Current		I_{res}	−10 ~ 10	mA
Power Dissipation	DIP	P_d	762	mW
	SOP	P_d	543	mW
Operating Temperature Range	DIP	T_a	−20 ~ 85	°C
	SOP	T_a	−20 ~ 70	°C
Storage Temperature Range		T_{stg}	−65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit
Positive Supply Voltage	V_{CC}	4.5 ~ 15	V
Negative Supply Voltage	V_{EE}	−4.5 ~ −15	V
Response Control Current	I_{RES}	−5.5 ~ 5.5	mA
Input Voltage of Driver	V_{ID}	15	V
Input Voltage of Receiver	V_{IR}	−25 ~ 25	V
Output Current of Receiver	I_{OR}	24	mA

ELECTRICAL CHARACTERISTICS

(V_{CC} = 12V, V_{EE} = −12V, Ta = −20°C ~ 85°C, unless otherwise noted)

Characteristic		Symbol	Test Condition	Min	Typ	Max	Unit
Positive Supply Current	V_{CC} = 5V	I_{CC1}	V_{ID} = 2.0V		6.3	8.1	mA
	V_{CC} = 9V		V_{IR} = 2.3V		9.1	11.9	
	V_{CC} = 12V		No Load		10.4	14.0	
	V_{CC} = 5V	I_{CC2}	V_{ID} = 0.8V		2.5	3.4	
	V_{CC} = 9V		V_{IR} = 0.6V		3.7	5.1	
	V_{CC} = 12V		No Load		4.1	5.6	
Negative Supply Current	V_{EE} = −5V	I_{EE1}	V_{ID} = 2.0V		−2.4	−3.1	
	V_{EE} = −9V		V_{IR} = 2.3V		−3.9	−4.9	
	V_{EE} = −12V		No Load		−4.8	−6.1	
	V_{EE} = −5V	I_{EE2}	V_{ID} = 0.8V		−0.20	−0.35	
	V_{EE} = −9V		V_{IR} = 0.6V		−0.25	−0.40	
	V_{EE} = −12V		No Load		−0.27	−0.45	
Positive Supply Current	V_{CC} = 5V	I_{CC3}	V_{ID} = 0V, V_{IR} = 2.3V		4.8	6.4	
	V_{CC} = 12V		V_{EE} = 0V, No Load		6.7	9.1	

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic		Symbol	Test Condition	Min	Typ	Max	Unit
DRIVER							
Input Voltage High		V_{IH}		2.0			V
Input Voltage Low		V_{IL}				0.8	
Output Voltage High	$V_{CC}=5V$, $V_{EE}=-5V$	V_{OH}	$V_{ID}=0.8V$, $R_L=3K\Omega$	3.2	3.7		V
	$V_{CC}=9V$, $V_{EE}=-9V$			6.5	7.1		
	$V_{CC}=12V$, $V_{EE}=-12V$			8.9	9.8		
Output Voltage Low	$V_{CC}=5V$, $V_{EE}=-5V$	V_{OL}	$V_{ID}=2.0V$, $R_L=3K\Omega$		-3.6	-3.2	V
	$V_{CC}=9V$, $V_{EE}=-9V$				-7.1	-6.4	
	$V_{CC}=12V$, $V_{EE}=-12V$				-9.7	-8.8	
Input Current High		I_{IH}	$V_{ID}=7.0V$			5	μA
Input Current Low		I_{IL}	$V_{ID}=0.0V$		-0.73	-1.2	mA
Output Short Circuit Current (Positive)		I_{OSH}	$V_{ID}=0.8V$, $V_O=0.0V$	-7.0	-12.0	-14.5	mA
Output Short Circuit Current (Negative)		I_{OSL}	$V_{ID}=2.0V$, $V_O=0.0V$	6.5	11.5	14.0	mA
Output Impedance		R_O	$V_{CC}=V_{EE}=0V$, $V_O=\pm 2V$	300			Ω
RECEIVER							
Input Threshold Voltage (Positive)		V_{T+}		1.2	1.9	2.3	V
Input Threshold Voltage (Negative)		V_{T-}		0.6	0.95	1.2	
Input Hysteresis		V_{HYS}		0.6			V
Output Voltage High	$V_{CC}=5V$, $V_{EE}=-5V$	V_{OH}	$V_{IR}=0.6V$, $I_{OH}=-10\mu A$	3.7	4.1	4.5	V
	$V_{CC}=12V$, $V_{EE}=-12V$			4.4	4.7	5.2	
	$V_{CC}=5V$, $V_{EE}=-5V$	V_{OH}	$V_{IR}=0.6V$, $I_{OH}=0.4mA$	3.1	3.4	3.8	
	$V_{CC}=12V$, $V_{EE}=-12V$			3.6	4.0	4.5	
Output Voltage Low		V_{OL}	$V_{IR}=2.3V$, $I_{OL}=24mA$		0.2	0.3	V
Input Current High		I_{IH}	$V_{IR}=25V$	3.6	6.7	8.3	mA
			$V_{IR}=3V$	0.43	0.67	1.0	
Input Current Low		I_{IL}	$V_{IR}=-25V$	-3.6	-6.7	-8.3	mA
			$V_{IR}=-3V$	-0.43	-0.74	-1.0	
Output Short Circuit Current		I_{OS}	$V_{IR}=0.6V$		-2.8	-3.7	mA

Note) 1. All characteristics are measured with the response control terminal open.

SWITCHING CHARACTERISTICS

(V_{CC} = 12V, V_{EE} = − 12V, Ta = − 25°C, unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
DRIVER						
Propagation Delay Time Low to High	t_{PLH}	R_L = 3KΩ, C_L = 50pF		340	480	ns
Propagation Delay Time High to Low	t_{PHL}			100	150	ns
Transition Time Low to High	t_{TLH}			120	180	ns
Transition Time High to Low	t_{THL}			105	160	ns
Transition Time Low to High	t_{TLH}	R_L = 3KΩ~7KΩ(Fig. 1), C_L = 2500pF, (Note 2)		2.1	3.0	μs
Transition Time High to Low	t_{THL}			2.1	3.0	μs
RECEIVER						
Propagation Delay Time Low to High	t_{PLH}	R_L = 400Ω, C_L = 50pF		150	240	ns
Propagation Delay time High to Low	t_{PHL}			50	100	ns
Transition Time Low to High	t_{TLH}			250	360	ns
Transition Time High to Low	t_{THL}			18	35	ns

Note) 2. Measured between +3V and −3V points on the output waveform.

TEST CIRCUIT

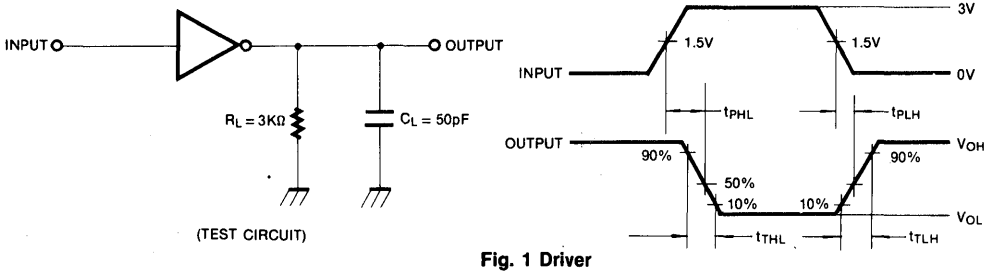
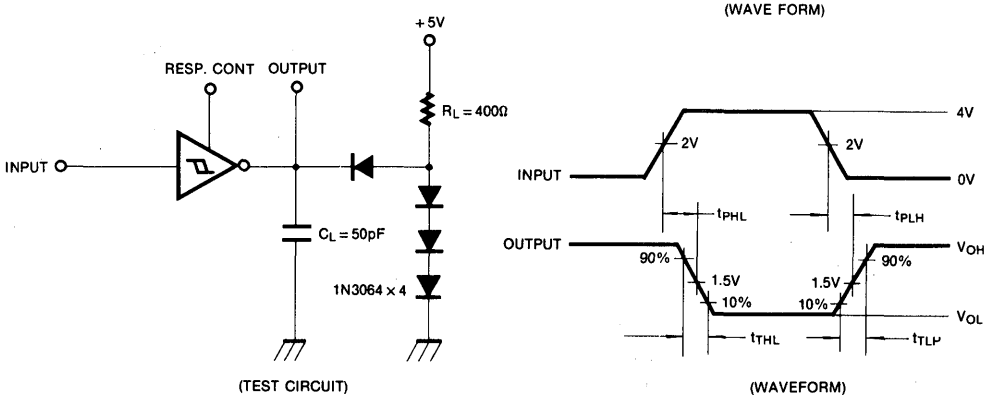


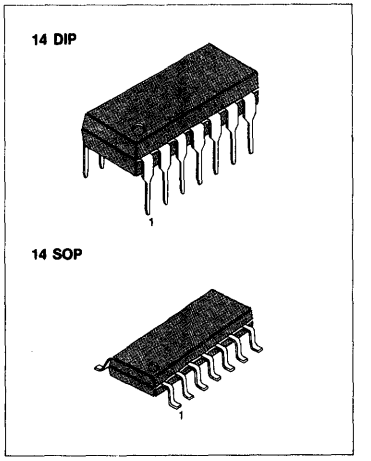
Fig. 1 Driver



Note) 3. The pulse generator has the following characteristics: Z_{OUT} = 50Ω, tw = 500ns, tr = tf ≧ 5ns

QUAD CMOS LINE DRIVER

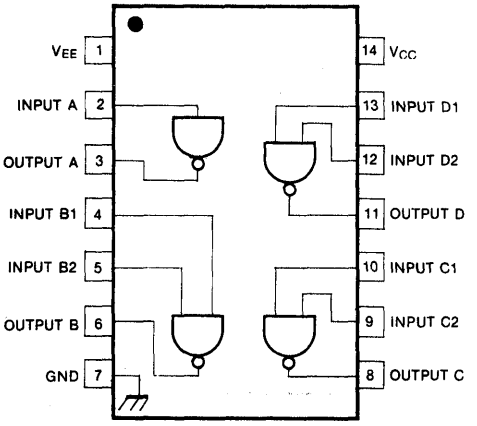
The KS5788 is designed to interface data terminal equipment (DTE) with data communications equipment (DCE) in conformance with the specifications of EIA RS-232-C, CCITT V.24 standards. The KS5788 is a direct replacement for the bipolar device (MC1488).



FEATURES

- **Low power consumption & low delay slew**
- **Pin for pin equivalent to MC1488**
- **Power-off source impedance: 300Ω (min)**
- **Compatible with TTL and HCTLS families**
- **Flexible operating supply range: 4.5~12.6V**

PIN CONFIGURATION



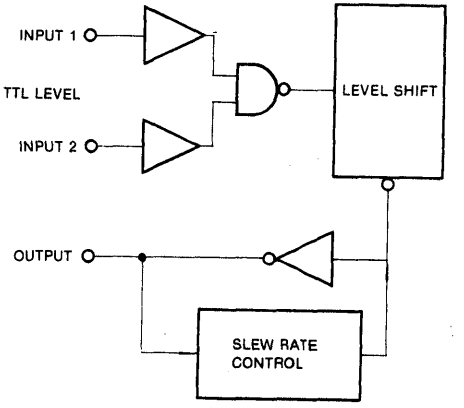
ORDERING INFORMATION

Device	Package	Operating Temperature
†KS5788N	14 DIP	−40~+85°C
†KS5788D	14 SOP	

† Under Development

BLOCK DIAGRAM

(1/4 OF CIRCUIT SHOWN)



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C, unless otherwise noted)

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	−0.5 ~ 13.5 0.5 ~ −13.5	V_{dc}
Input Voltage (Any Input Pin)	V_{IN}	−0.3 ~ V_{CC} + 0.3	V_{dc}
Output Voltage (Any Output Pin)	V_{OUT}	−25 ~ 25	V_{dc}
Power Dissipation	P_D	1.0	W
Operating Temperature	T_a	−40 ~ 85	°C
Storage Temperature	T_{stg}	−65 ~ 150	°C

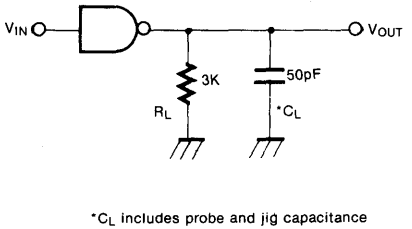
ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5 to 12V, V_{EE} = −4.5 to −12V, GND = 0V, Ta = −40° to 85°C, unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
RECOMMENDED OPERATING CONDITIONS						
Power Supply Voltage V_{CC} V_{EE}	V_{CC} V_{EE}		4.5 −4.5		12.6 −12.6	V_{dc}
DC ELECTRICAL CHARACTERISTICS						
Input Current 1	I_{IL}	V_{IN} = GND	−10		10	μA
Input Current 2	I_{IH}	V_{IN} = V_{CC}	−10		10	μA
Positive Supply Current 1 (V_{IN} = V_{IL}, R_L = ∞, per package)	I_{CC1}	V_{CC} = 4.5V, V_{EE} = −4.5V V_{CC} = 9.0V, V_{EE} = −9.0V V_{CC} = 12.0V, V_{EE} = −12.0V			10 30 60	μA μA μA
Positive Supply Current 2 (V_{IN} = V_{IH}, R_L = ∞, per package)	I_{CC2}	V_{CC} = 4.5V, V_{EE} = −4.5V V_{CC} = 9.0V, V_{EE} = −9.0V V_{CC} = 12.0V, V_{EE} = −12.0V			30 190 425	μA μA μA
Negative Supply Current 1 (V_{IN} = V_{IL}, R_L = ∞, per package)	I_{EE1}	V_{CC} = 4.5V, V_{EE} = −4.5V V_{CC} = 9.0V, V_{EE} = −9.0V V_{CC} = 12.0V, V_{EE} = −12.0V			−10 −10 −10	μA μA μA
Negative Supply Current 2 (V_{IN} = V_{IH}, R_L = ∞, per package)	I_{EE2}	V_{CC} = 4.5V, V_{EE} = −4.5V V_{CC} = 9.0V, V_{EE} = −9.0V V_{CC} = 12.0V, V_{EE} = −12.0V			−30 −30 −60	μA μA μA
Input Voltage High	V_{IH}		2.0		V_{DD}	V_{dc}
Input Voltage Low	V_{IL}	$V_{CC} \geqq 7V$, $V_{EE} \leqq -7V$ $V_{CC} \leqq 7V$, $V_{EE} \geqq -7V$	GND GND		0.8 0.6	V_{dc}

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic		Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage High ($V_{IN}=V_{IL}$, $R_L=3K\Omega\sim7K\Omega$)		V_{OH}	$V_{CC}=4.5V$, $V_{EE}=-4.5V$ $V_{CC}=9.0V$, $V_{EE}=-9.0V$ $V_{CC}=12V$, $V_{EE}=-12V$	3.0 6.5 9.0			V_{dc}
Output Voltage Low ($V_{IN}=V_{IH}$, $R_L=3K\Omega\sim7K\Omega$)		V_{OL}	$V_{CC}=4.5V$, $V_{EE}=-4.5V$ $V_{CC}=9.0V$, $V_{EE}=-9.0V$ $V_{CC}=12V$, $V_{EE}=-12V$			-3.0 -6.5 -9.0	V_{dc}
Output Short Circuit Current	$V_{IN}=V_{IL}$	I_{OS}	$V_O=GND$			45	mA
	$V_{IN}=V_{IH}$		$V_{CC}=12V$, $V_{EE}=-12V$			-45	
Power Off Output Resistance		R_O	$V_{CC}=V_{EE}=0V$, $V_{OUT}=\pm2V$	300			Ω
SWITCHING CHARACTERISTICS ($V_{CC}=4.5V$ to $12V$, $V_{EE}=-4.5V$ to $-12V$, $Ta=-40°C\sim85°C$, Fig. 1)							
Propagation Delay		t_{pd}	$V_{CC}=4.5V$, $V_{EE}=-4.5V$ $V_{CC}=9.0V$, $V_{EE}=-9.0V$ $V_{CC}=12V$, $V_{EE}=-12V$			6.0 5.0 4.0	μS
Output Rise Time		t_r	V_{OUT} = from $-3V$ to $3V$	0.2			μS
Output Fall Time		t_f	V_{OUT} = from $3V$ to $-3V$	0.2			μS
Output Slew Rate		S_R	$R_L=3K\Omega$ to $7K\Omega$ $15pF>C_L>2.5nF$			30	V/μS
Typical Propagation Delay Skew		t_{SK}	$V_{CC}=12V$, $V_{EE}=-12V$		400		nS



*C_L includes probe and jig capacitance

Fig. 1 AC Test Circuit

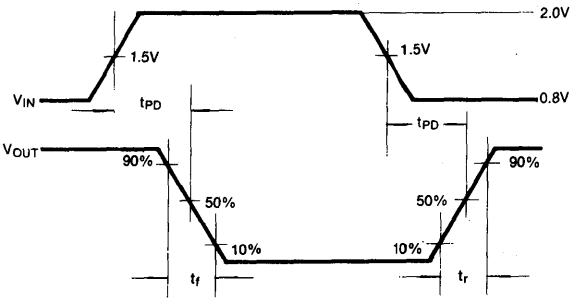
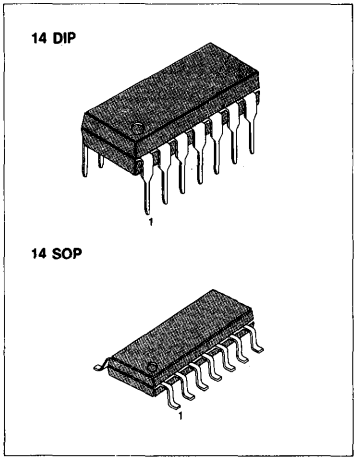


Fig. 2 Switching Waveforms

QUAD CMOS LINE RECEIVER

The KS5789A is designed to interface data terminal equipment (DTE) with data communications equipment (DCE) in conformance with the specifications of EIA RS-232-C, CCITT V.24 standards. The KS5789A is a direct replacement for the bipolar device (MC1489/A).



FEATURES

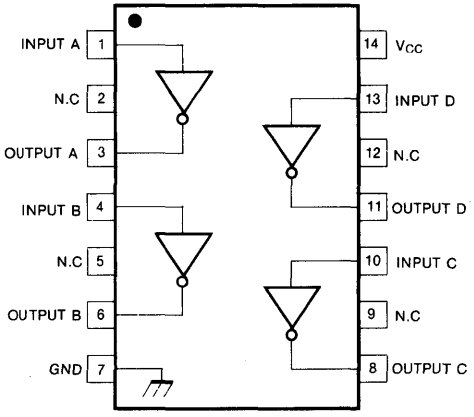
- **Low power consumption & low delay slew**
- **Pin for pin equivalent to MC1489/A**
- **Inputs withstand ± 30V**
- **Fail-safe operating mode**
- **Internal noise filter**
- **Internal input threshold with hysteresis**

ORDERING INFORMATION

Device	Package	Operating Temperature
†KS5789AN	14 DIP	−40 ~ +85°C
†KS5789AD	14 SOP	

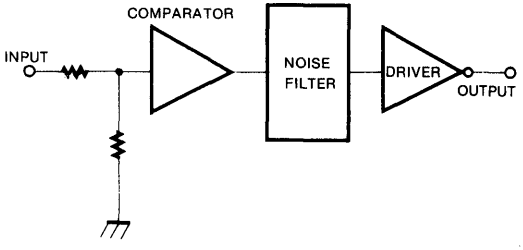
† Under Development

PIN CONFIGURATION



BLOCK DIAGRAM

(1/4 OF CIRCUIT SHOWN)



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C, unless otherwise noted)

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 ~ 7.0	V_{dc}
Input Voltage	V_{IN}	−30 ~ 30	V_{dc}
Output Voltage	V_{OUT}	−0.3 ~ V_{CC} + 0.3	V_{dc}
Power Dissipation (85°C)	P_D	500	mW
Operating Temperature	T_a	−40 ~ 85	°C
Storage Temperature	T_{stg}	−65 ~ 150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 0.5V, Ta = −40° to 85°C, unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
DC ELECTRICAL CHARACTERISTICS						
Input Voltage High	V_{IH}		1.3		2.5	V_{dc}
Input Voltage Low	V_{IL}		0.5		1.7	V_{dc}
Input Hysteresis Voltage	V_H	$V_{IH} - V_{IL}$		1.0		V_{dc}
Input Current	I_{IN}	V_{IN} = 3V V_{IN} = −3V V_{IN} = 25V V_{IN} = −25V	0.43 −0.43 3.6 −3.6		1.0 −1.0 8.3 −8.3	mA
Output Voltage High	V_{OH}	$V_{IN} = V_{IL(min)}$, I_{OUT} = −3.2mA	2.8			V_{dc}
Output Voltage Low	V_{OL}	$V_{IN} = V_{IH(max)}$, I_{OUT} = 3.2mA			0.4	V_{dc}
Supply Current	I_{CC}	$R_L = \infty$, $V_{IN} = V_{IL(min)}$ to $V_{IH(max)}$			600	μA
SWITCHING CHARACTERISTICS (V_{CC} = 4.5V to 5.5V, Ta = −40° ~ 85°C, C_L = 50pF, Note 1)						
Propagation Delay	t_p	Input pulse width ≧ 10μS			6.5	μS
Output Rise Time	t_r				300	nS
Output Fall Time	t_f				300	nS
Pulse Width Assumed to be Noise	t_{nw}				1.0	μS
Propagration Delay Skew	t_{sk}			400		nS

Note 1: Test waveform $t_r = t_f$ = 200ns, V_{IH} = +3V, V_{IL} = −3V, f = 20KHz

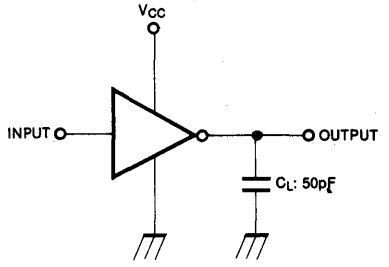


Fig. 1 AC Test Circuit

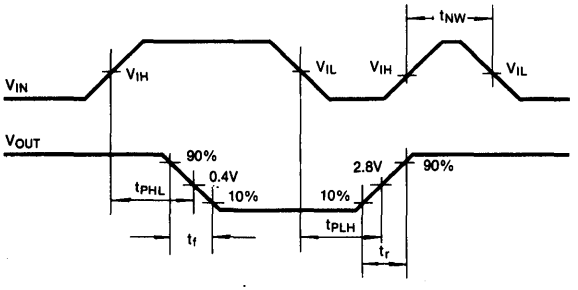
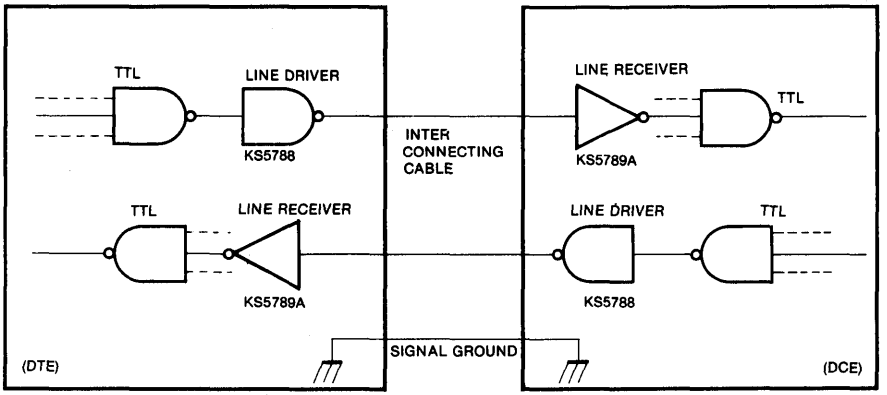


Fig. 2 Switching Waveforms

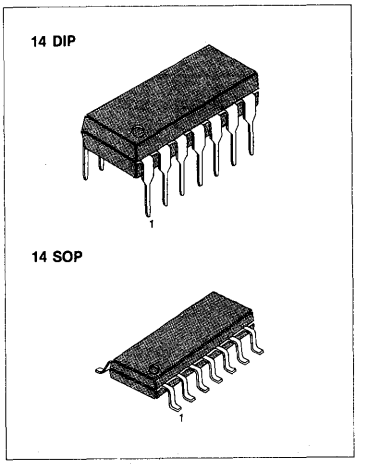
TYPICAL APPLICATION



RS-232-C Data Transmission

QUAD LINE DRIVER

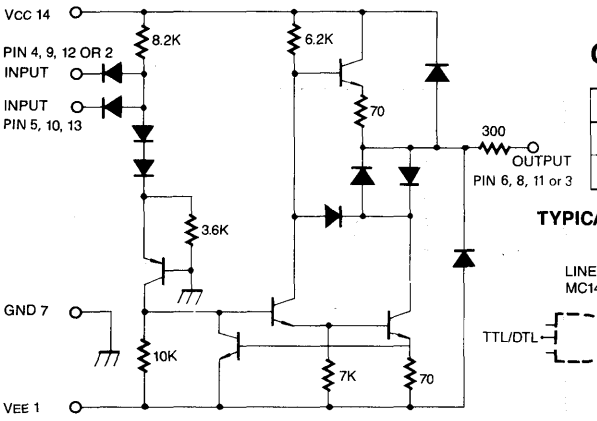
The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.



FEATURES

- **Current Limited Output: ± 10mA typ**
- **Power-Off Source Impedance: 300 Ohms (min)**
- **Simple Slew Rate Control with External Capacitor**
- **Flexible Operating Supply Range**
- **Compatible with DTL and TTL, HCTLS Families**

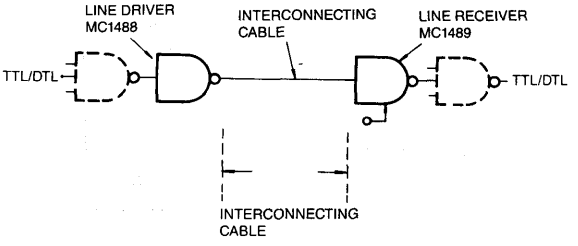
SCHEMATIC DIAGRAM (1/4 of Circuit Shown)



ORDERING INFORMATION

Device	Package	Operating Temperature
MC1488N	14 DIP	0 ~ +70°C
MC1488D	14 SOP	

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS (T_a = 25°C unless otherwise noted)

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+15 −15	V_{DC}
Input Voltage Range	V_{IR}	$-15 \leq V_{IR} \leq 7.0$	V_{DC}
Output Signal Voltage	V_D	±15	V_{DC}
Power Dissipation	P_D	1000	mW
Derate Above T_a = +25°C	$1/R\theta_{JA}$	6.7	mW/°C
Operating Temperature Range	T_a	0 ~ +70	°C
Storage Temperature Range	Tstg	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 9.0±1%V, V_{EE} = −9.0 ± 1%V, T_a = 0 ~ 70°C unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Fig
Input Current 1	I_{IL}	Low Logic State (V_{IL} = 0)		1.0	1.6	mA	1
Input Current 2	I_{IH}	High Logic State (V_{IH} = 5.0V)			10	μA	1
Output Voltage-High Logic State	V_{OH}	V_{IL} = 0.8V, R_L = 3.0KΩ, V_{CC} = 9.0V, V_{EE} = −9.0V	6	7		V	2
		V_{IL} = 0.8V, R_L = 3.0KΩ, V_{CC} = 13.2V, V_{EE} = −13.2V	9	10.5			
Output Voltage-Low Logic State	V_{OL}	V_{IH} = 1.9V, R_L = 3.0KΩ, V_{CC} = 9.0V, V_{EE} = −9.0V	−6	−7		V	2
		V_{IH} = 1.9V, R_L = 3.0KΩ, V_{CC} = 13.2V, V_{EE} = −13.2V	−9	−10.5			
Output Short Circuit Current	I_{OS+}	Positive	−6	−10	−12	mA	3
Output Short Circuit Current	I_{OS-}	Negative	6	10	12	mA	3
Output Resistance	R_O	V_{CC} = V_{EE} = 0, V_O = ±2.0V	300			Ω	
Positive Supply Current (RL=∞)	I_{CC}	V_{IH} = 1.9V, V_{CC} = +9.0V		15	20	mA	5
		V_{IL} = 0.8V, V_{CC} = +9.0V		4.5	6		
		V_{IH} = 1.9V, V_{CC} = +12V		19	25		
		V_{IL} = 0.8V, V_{CC} = +12V		5.5	7		
		V_{IH} = 1.9V, V_{CC} = +15V			34		
		V_{IL} = 0.8V, V_{CC} = +15V			12		
Negative Supply Current (RL=∞)	I_{EE}	V_{IH} = 1.9V, V_{EE} = −9.0V		−13	−17	mA	5
		V_{IL} = 0.8V, V_{EE} = −9.0V			−15	μA	
		V_{IH} = 1.9V, V_{EE} = −12V		−18	−23	mA	
		V_{IL} = 0.8V, V_{EE} = −12V			−15	μA	
		V_{IH} = 1.9V, V_{EE} = −15V			−34	mA	
		V_{IL} = 0.8V, V_{EE} = −15V			−2.5	mA	
Power Consumption	P_C	V_{CC} = 9.0V, V_{EE} = −9.0V			333	mW	
		V_{CC} = 12V, V_{EE} = −12V			576		

* Maximum package power dissipation may be exceeded if all outputs are shorted simultaneously.

SWITCHING CHARACTERISTICS

(V_{CC} = 9.0 ± 1%V, V_{EE} = −9.0 ± 1%V, T_a = 0 ~ 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Fig
Propagation Delay Time	t_{PLH}	Z_L = 3.0K and 15pF		275	350	nS	6
Fall Time	t_{THL}	Z_L = 3.0K and 15pF		45	75	nS	6
Rise Time	t_{TLH}	Z_L = 3.0K and 15pF		55	100	nS	6
Propagation Delay Time	t_{PHL}	Z_L = 3.0K and 15pF		110	175	nS	6

DC TEST CIRCUIT

FIGURE 1 INPUT CURRENT

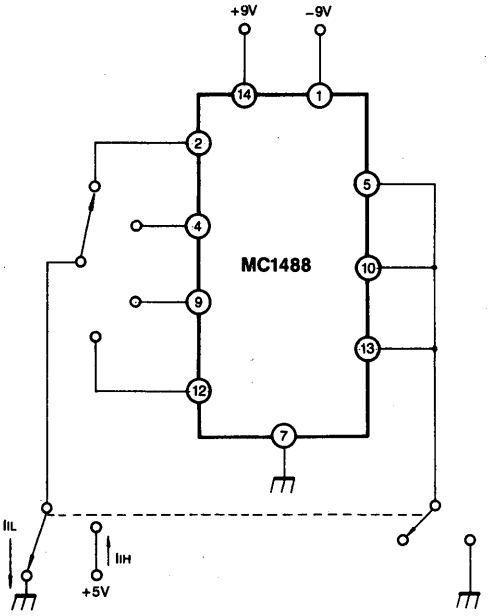


FIGURE 2 OUTPUT VOLTAGE

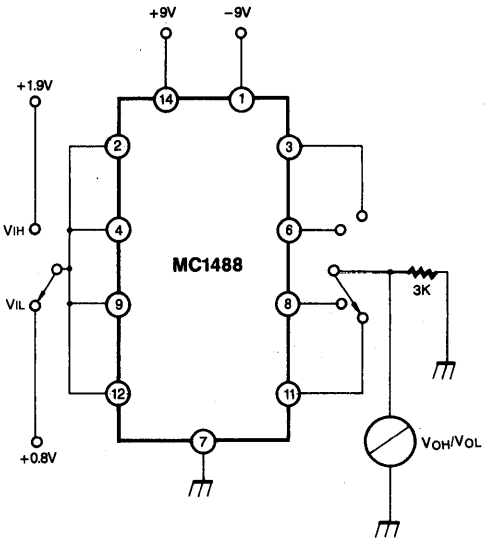


FIGURE 3 OUTPUT SHORT CIRCUIT CURRENT

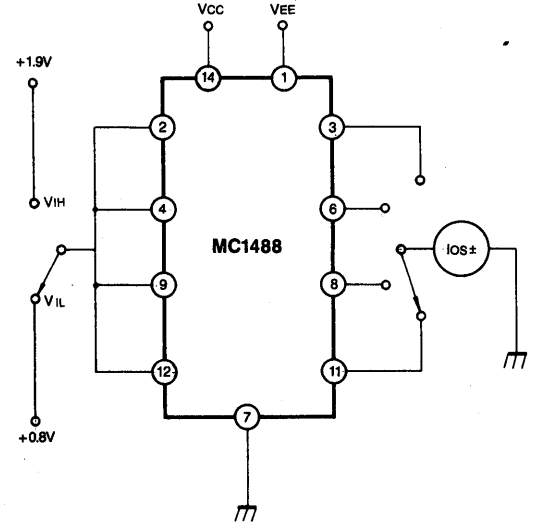


FIGURE 4 OUTPUT RESISTANCE (POWER OFF)

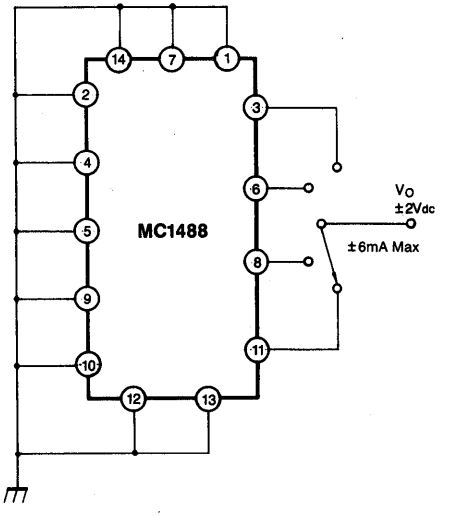


FIGURE 5 POWER SUPPLY CURRENTS

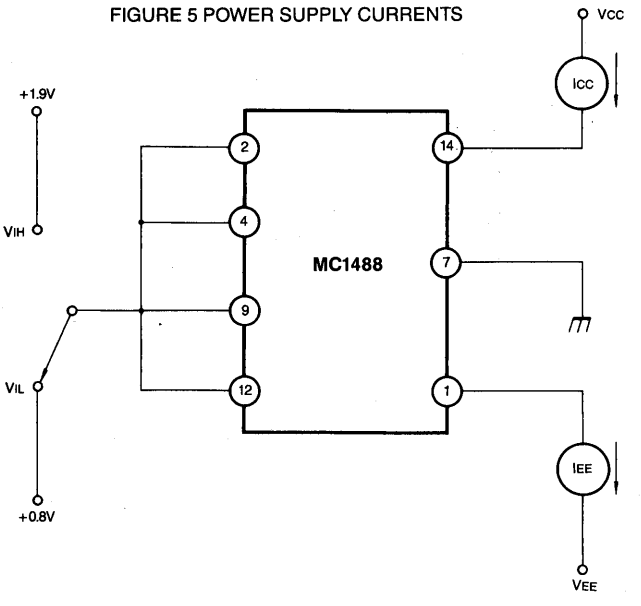
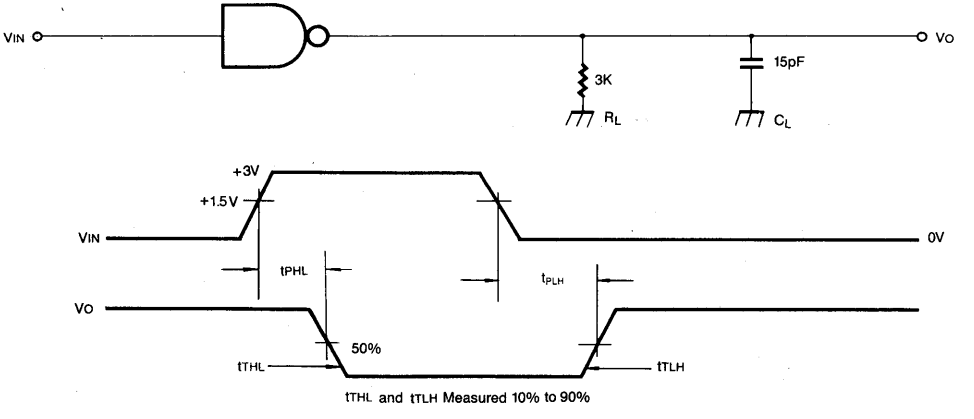


FIGURE 6 SWITCHING RESPONSE



TYPICAL PERFORMANCE CHARACTERISTICS

FIGURE 7 — TRANSFER CHARACTERISTICS V_S POWER-SUPPLY VOLTAGE

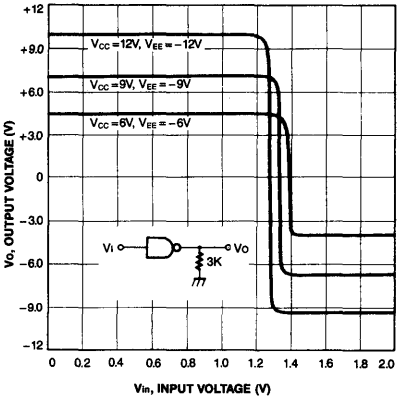


FIGURE 8 — SHORT CIRCUIT OUTPUT CURRENT V_S TEMPERATURE

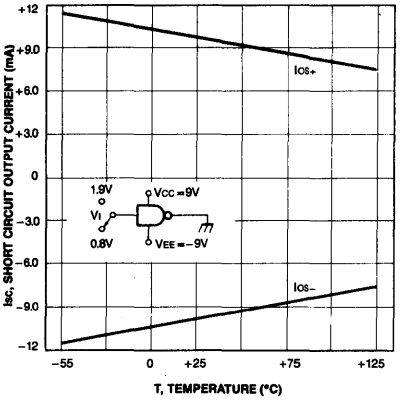


FIGURE 9 — OUTPUT SLEW RATE V_S LOAD CAPACITANCE

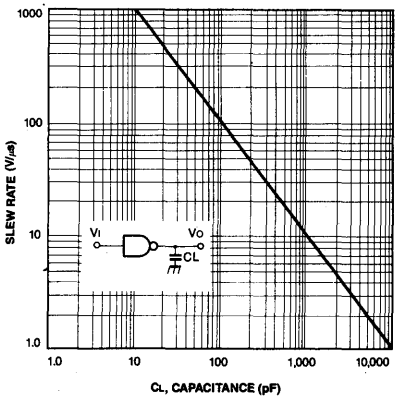


FIGURE 10 — OUTPUT VOLTAGE AND CURRENT LIMITING CHARACTERISTICS

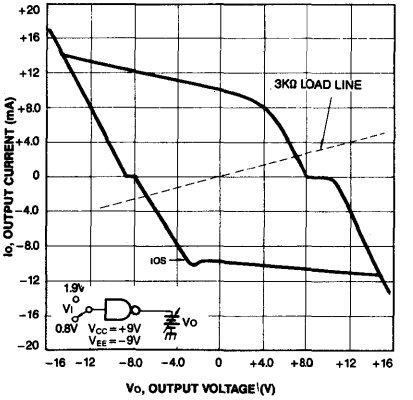
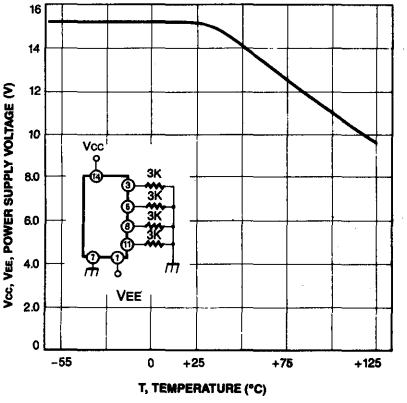
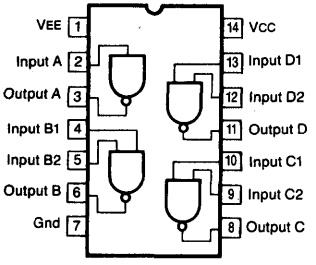


FIGURE 11 — MAXIMUM OPEATING TEMPERATURE V_S POWER SUPPLY VOLTAGE

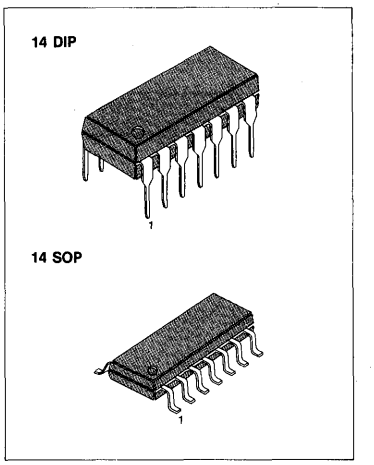


PIN CONNECTIONS



QUAD LINE RECEIVER

The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

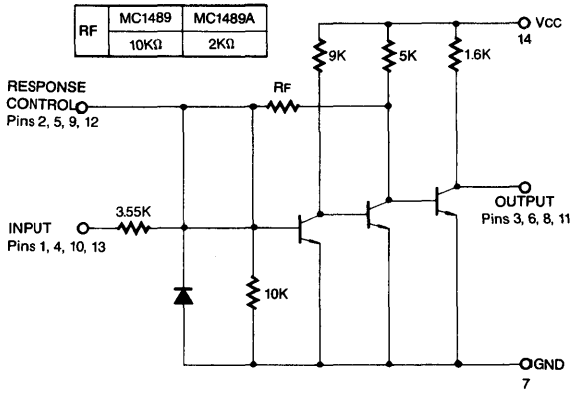


FEATURES

- **Input Resistance: 3.0KΩ to 7.0KΩ**
- **Input Signal Range: ±30 Volts**
- **Response Control**
  - **a) Logic Threshold Shifting**
  - **b) Input Noise Filtering**
- **Input Threshold Hysteresis Built in**

SCHEMATIC DIAGRAM

(1/4 OF CIRCUIT SHOWN)



ORDERING INFORMATION

Device	Package	Operating Temperature
MC1489N	14 DIP	0 ~ +70°C
MC1489AN		
MC1489D	14 SOP	
MC1489AD		

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10	V_{DC}
Input Voltage Range	V_{IR}	±30	V_{DC}
Output Load Current	I_L	20	mA
Power Dissipation Derate Above T_a = +25°C	P_D $1/\theta_{JA}$	1000 6.7	mW mW/°C
Operating Temperature	T_a	0 to +70	°C
Storage Temperature	Tstg	−65 to +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_a = 0 ~ 70°C unless otherwise noted)

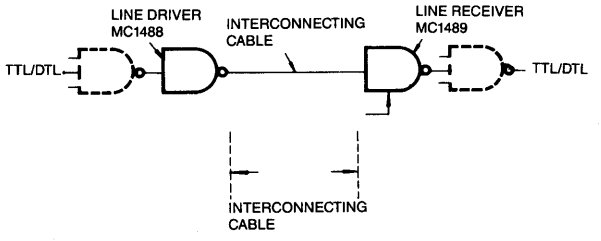
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Positive Input Current	I_{IH}	V_{IH} = 25Vdc	3.6		8.3	mA
		V_{IH} = 3.0Vdc	0.43			
Negative Input Current	I_{IL}	V_{IL} = −25Vdc	−3.6		−8.3	mA
		V_{IL} = −3.0Vdc	−0.43			
Input Turn-On Thereshold Voltage MC1489 MC1489A	V_{IH}	T_a = 25°C, $V_{OL} \leq$ 0.45V I_L = 10mA	 1.0 1.75	 1.95	 1.5 2.25	Vdc
Input Turn-Off Threshold Voltage	V_{IL}	T_a = 25°C, $V_{OH} \geq$ 2.5V, I_L = −0.5mA	0.75		1.25	Vdc
Output Voltage High	V_{OH}	V_{IN} = 0.75V, I_L = −0.5mA	2.6	4.0	5.0	Vdc
		Input Open, I_L = −0.5mA	2.6	4.0	5.0	
Output Voltage Low	V_{OL}	V_{IN} = 3.0V, I_L = 10mA		0.2	0.45	Vdc
Output Short Circuit Current	I_{OS}	V_{IN} = 0.75V		−3.0	−4.0	mA
Power Supply Current	I_{CC}	All gates "on", I_{OUT} = 0mA, V_{IH} = 5.0V		16	26	mA
Power Consumption	P_C	V_{IH} = 5.0V		80	130	mW

SWITCHING CHARACTERISTICS

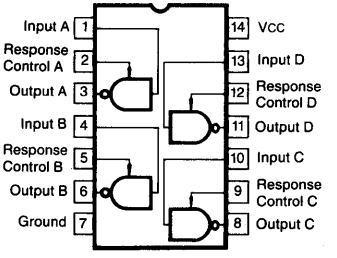
(V_{CC} = 5.0V ± 1%, T_a = 25°C, See Fig. 1)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time	t_{PLH}	R_L = 3.9KΩ		25	85	nS
Rise Time	t_{TLH}	R_L = 3.9KΩ		120	175	nS
Propagation Delay Time	t_{PHL}	R_L = 390Ω		25	50	nS
Fall Time	t_{THL}	R_L = 390Ω		10	20	nS

TYPICAL APPLICATION

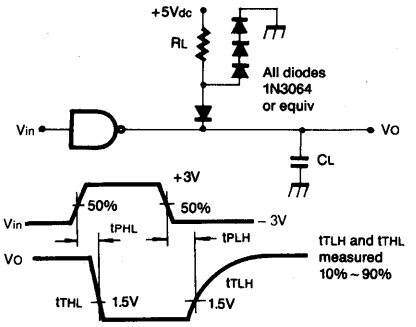


PIN CONNECTIONS



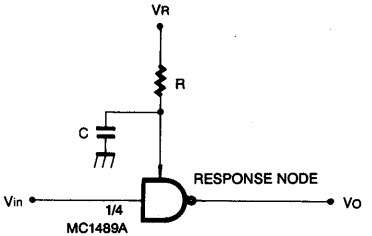
TEST CIRCUIT

Fig 1 — SWITCHING RESPONSE



CL = 15pF = total parasitic capacitance, which includes probe and wiring capacitances

Fig 2 — RESPONSE CONTROL NODE



C, capacitor is for noise filtering
R. resistor is for threshold shifting

TYPICAL PERFORMANCE CHARACTERISTICS

(V_{CC} = 5.0 V_{dc}, T_a = +25°C unless otherwise noted)

Fig. 3 — TYPICAL TURN-ON THRESHOLD V_s CAPACITANCE FROM RESPONSE CONTROL PIN TO GND

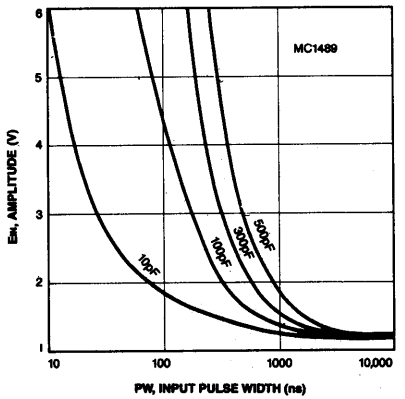


Fig. 4 — TYPICAL TURN-ON THRESHOLD V_s CAPACITANCE FROM RESPONSE CONTROL PIN TO GND

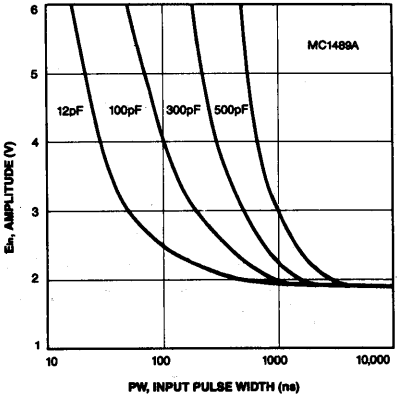


Fig. 5 — INPUT CURRENT

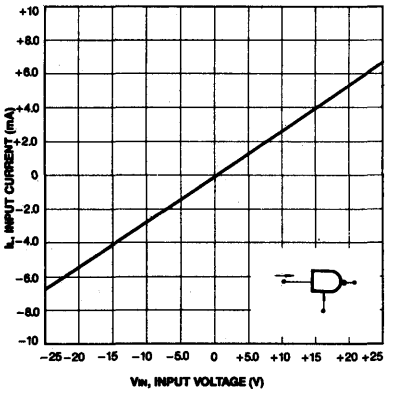


Fig. 6 — MC1489 INPUT THRESHOLD VOLTAGE ADJUSTMENT

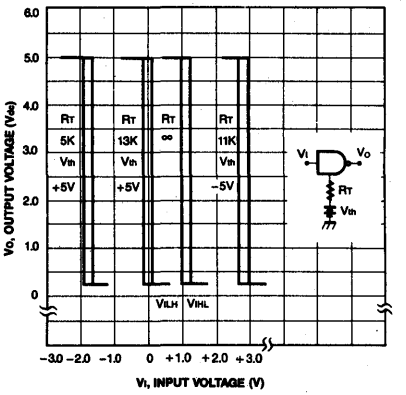


Fig. 7 — MC1489A INPUT THRESHOLD VOLTAGE ADJUSTMENT

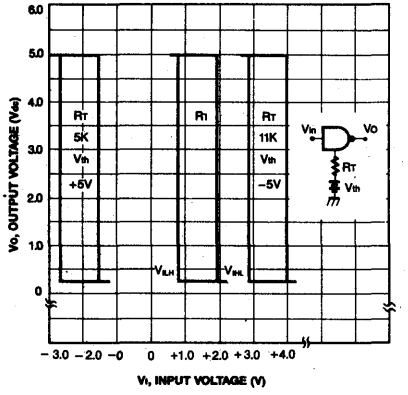


Fig. 8 — INPUT THRESHOLD VOLTAGE Vs. TEMPERATURE

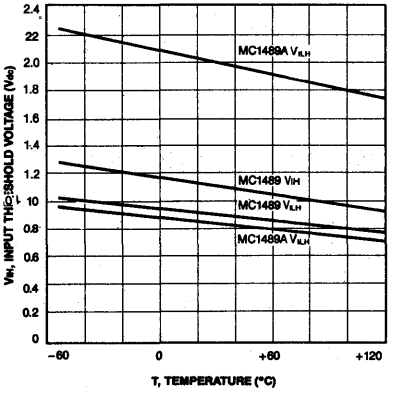
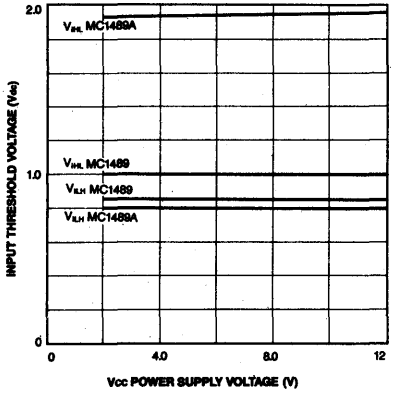


Fig. 9 — INPUT THRESHOLD Vs. POWER SUPPLY VOLTAGE



NOTES

DRIVER & OTHER ICs 6

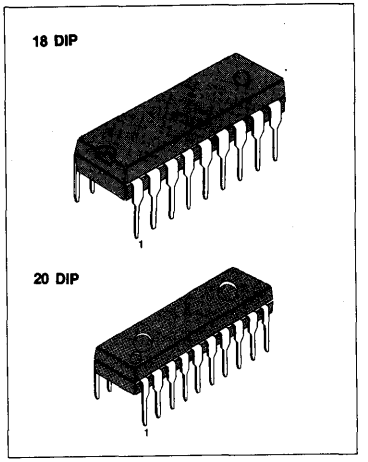
8-CHANNEL SOURCE DRIVERS

These integrated circuits, rated for operation with output voltages of up to 50V and designed to link NMOS logic with high-current inductive loads, will work with many combinations of logic-and load-voltage levels, meeting interface requirements beyond the capabilities of standard logic buffers.

KA2580A is a high current source driver used to switch the ground ends of loads that are directly connected to a negative supply. Typical loads are telephone relays, PIN diodes, and LEDs.

KA2588A is a high-current source driver similar to KA2580A, has separated logic and driver supply lines. Its eight drivers can serve as an interface between positive logic (TTL, CMOS, PMOS) or negative logic (NMOS) and either negative or split-load supplies.

KA2580A is furnished in 18-pin dual in-line plastic package; KA2588A is supplied in a 20-pin dual in-line plastic package. All input connections are on one side of the packages, output pins on the other, to simplify printed wiring board layout.



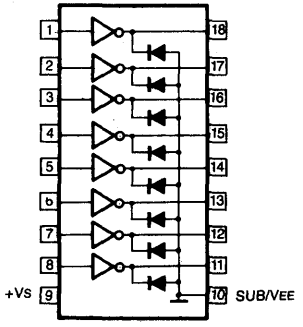
FEATURES

- **TTL, CMOS, PMOS, NMOS Compatible**
- **High Output Current Ratings**
- **Internal Transient Suppression**
- **Efficient Input/Output Pin Structure**

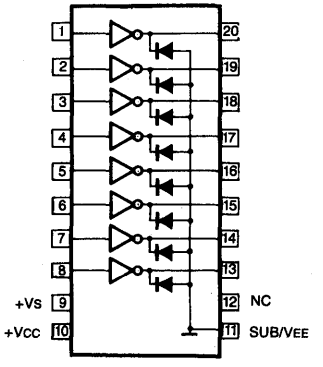
ORDERING INFORMATION

Device	Package	Operating Temperature
KA2580AN	18 DIP	−20 ~ +85°C
KA2588AN	20 DIP	

SCHEMATIC DIAGRAM



KA2580A



KA2588A

ABSOLUTE MAXIMUM RATINGS

(T_a=25°C, for Any One Driver unless otherwise noted)

Characteristic	Symbol	Value	Unit
Output Voltage	V_{CE}	50	V
Supply Voltage (ref, sub)	V_S	50	V
Supply Voltage (ref, sub, KA2588A)	V_{CC}	50	V
Input Voltage (ref, Vs)	V_{IN}	−30	V
Total Current	$I_{CC}+I_S$	−500	mA
Substrate Current	I_{SUB}	3.0	A
Power Dissipation (single output)	Pd	1.0	W
(total Package)*		2.2	W
Operating Temperature	T_a	−20 ~ +85	°C
Storage Temperature	Tstg	−65 ~ +150	°C

* Derate at the rate of 18mW/°C above 25°C

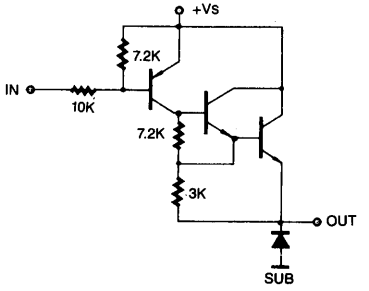
TYPICAL OPERATING VOLTAGE

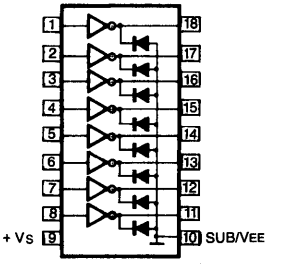
V_S	V_{IN} (on)	V_{IN} (off)	V_{CC}	V_{EE}(max)	DVC Type
0V	−15V ~ −3.6V	−0.5V ~ 0V	NA	−50V	KA2580A
+5V	0V ~ +1.4V	+4.5V ~ +5V	NA	−45V	KA2580A
			≤5V	−45V	KA2588A
+12V	0V ~ +8.4V	+11.5V ~ +12V	NA	−38V	KA2580A
			≤12V	−38V	KA2588A
+15V	0V ~ +11.4V	+14.5V ~ +15V	NA	−35V	KA2580A
			≤15V	−35V	KA2588A

Notes

1) For simplication, these devices are characterized to the above with specific voltages for inputs, logic supply (V_s), load supply (V_{EE}), and collector supply (V_{CC}).
2) Typical use of the KA2580A is with negative referenced logic. The more common application of the KA2588A is with positive referenced logic supplies.
3) In application, the devices are capable of operation over a wide range of logic and supply voltage levels.
4) The substrate must be tied to the most negative point in the external circuit to maintain isolation drivers and to provide for normal circuit operation.

PARTIAL SCHEMATIC (KA2580A)





ELECTRICAL CHARACTERISTICS (KA2580A)

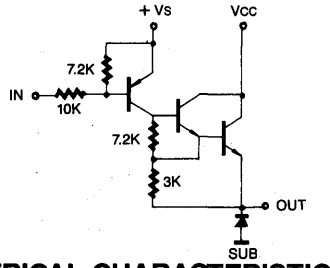
(T_a=25°C, V_S=0V, V_{EE}=−45V unless otherwise noted)

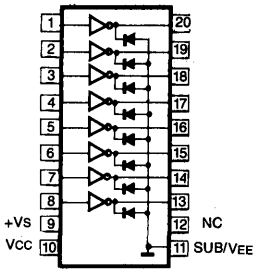
Characteristic	Symbol	Test Conditions	Min	Max	Unit
Output Leakage Current	I_{CEX}	V_{in}=−0.5V, V_{OUT}=V_{EE}=−50V		50	μA
		V_{IN}= −0.4V, V_{OUT}=V_{EE}= −50V, T_a=70°C		100	μA
Output Sustaining Voltage (Note 1, 2)	V_{CE} (sus)	V_{IN}=−0.4V, I_{OUT}=−25mA	35		V
Output Saturation Voltage	V_{CE} (sat)	V_{IN}=−2.4V, I_{OUT}=−100mA		1.8	V
		V_{IN}=−3.0V, I_{OUT}=−225mA		1.9	V
		V_{IN}=−3.6V, I_{OUT}=−350mA		2.0	V
Input Current	I_{IN} (on)	V_{IN}=−3.6V, I_{OUT}=−350mA		−500	μA
		V_{IN}=−15V, I_{OUT}=−350mA		−2.1	mA
	I_{IN} (off)	I_{OUT}= −500μA, T_a=70°C (Note 3)	−50		μA
Input Voltage (Note 4)	V_{IN} (on)	I_{OUT}=−100mA, V_{CE}≤1.8V		−2.4	V
		I_{OUT}=−225mA, V_{CE}≤1.9V		−3.0	V
		I_{OUT}=−350mA, V_{CE}≤2.0V		−3.6	V
	V_{IN} (off)	I_{OUT}=−500μA, T_a=70°C	−0.2		V
Clamp Diode Leakage Current	I_R	V_R=50V, T_a=70°C		50	μA
Clamp Diode Forward Voltage	Vf	If=350mA		2.0	V
Input Capacitance	C_{IN}			25	pF
Turn-On Delay	t_{PHL}	0.5 V_{IN} to 0.5 V_{OUT}		5.0	μS
Turn-Off Delay	t_{PLH}	0.5 V_{IN} to 0.5 V_{OUT}		5.0	μS

Notes

1) Pulsed test, tp≤300uS, duty cycle≤2%.
2) Negative current is defined as coming out of specified device pin.
3) The Iin (off) current limit guarantees against partial turn-on of the output.
4) The Vin (on) voltage limit guarantees a minimum output source per the specified conditions.
5) The substrate must always be tied to the most negative point and must be at least 4.0V below V_s.

PARTIAL SCHEMATIC (KA2588A)





ELECTRICAL CHARACTERISTICS (KA2588A)

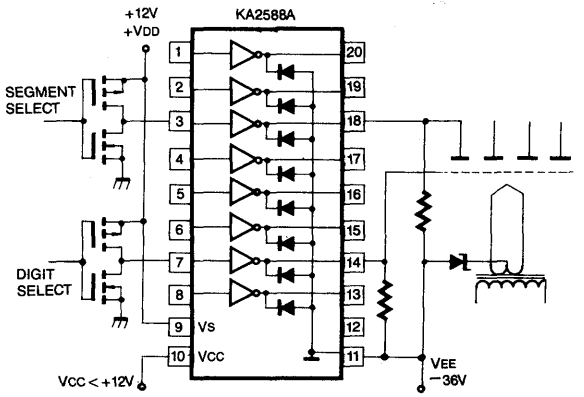
(T_a=25°C, V_S=V_{CC}=5.0V, V_{EE}=−40V unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Max	Unit
Output Leakage Current	I_{CEX}	V_{IN}≥4.5V, V_{OUT}=V_{EE}=−45V		50	μA
		V_{IN}≥4.6V, V_{OUT}=V_{EE}=−45V T_a=70°C		100	μA
Output Sustaining Voltage (Note 1, 2)	V_{CE} (sus)	V_{IN}≥4.6V, I_{OUT}=−25mA	35		V
Output Saturation Voltage	V_{CE} (sat)	V_{IN}=2.6V, I_{OUT}=−100mA Ref. V_{CC}		1.8	V
		V_{IN}=2.0V, I_{OUT}=−225mA Ref. V_{CC}		1.9	V
		V_{IN}=1.4V, I_{OUT}=−350mA Ref. V_{CC}		2.0	V
Input Current	I_{IN} (on)	V_{IN}=1.4V, I_{OUT}=−350mA		−500	μA
		V_S=15V, V_{EE}=−30V, V_{IN}=0V, I_{OUT}=−350mA		−2.1	mA
	I_{IN} (off)	I_{OUT}=−500μA, T_a=70°C (Note 3)	−50		μA
Input Voltage (Note 4)	V_{IN} (on)	I_{OUT}=−100mA, V_{CE}≤1.8V		2.6	V
		I_{OUT}=−225mA, V_{CE}≤1.9V		2.0	V
		I_{OUT}=−350mA, V_{CE}≤2.0V		1.4	V
	V_{IN} (off)	I_{OUT}=−500μA, T_A=70°C	4.8		V
Clamp Diode Leakage Current	I_R	V_R=50V, T_a=70°C		50	μA
Clamp Diode Forward Voltage	Vf	If=350mA		2.0	V
Input Capacitance	C_{IN}			25	pF
Turn-On Delay	t_{PHL}	0.5 V_{IN} to 0.5 Vout		5.0	μS
Turn-Off Delay	t_{PLH}	0.5 V_{IN} to 0.5 Vout		5.0	μS

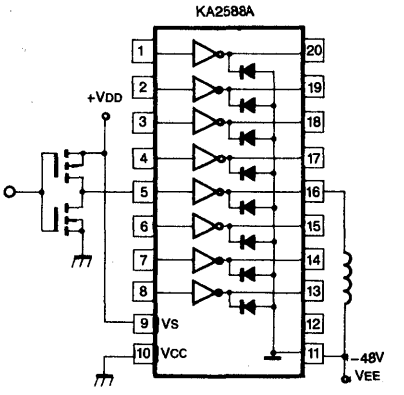
Notes

1) Pulsed test, tp≤300uS, duty cycle≤2%.
2) Negative current is defined as coming out of specified device pin.
3) The Iin (off) current limit guarantees against partial turn-on of the output.
4) The Vin (on) voltage limit guarantees a minimum output source per the specified conditions.
5) The substrate must always be tied to the most negative point and must be at least 4.0V below V_s.
6) V_{CC} must never be more positive than V_S.

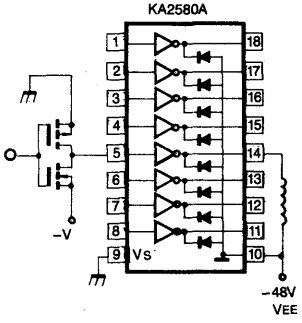
TYPICAL APPLICATIONS



Vacuum Fluorescent Display Driver (Split Supply)



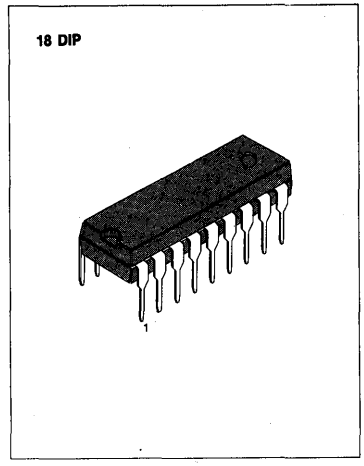
Telecommunicaiton Relay Driver (Positive Logic)



Telecommunication Relay Driver (Negative Logic)

FLUORESCENT DISPLAY DRIVERS

Consisting of eight NPN Darlington output stages and the associated common-emitter input stages, these drivers are designed to interface between low-level digital logic and vacuum fluorescent displays. KA2651 is capable of driving the digits and/or segments of these displays and is designed to permit all outputs to be activated simultaneously. Pull-down resistors are incorporated into each output and no external components are required for most fluorescent display applications.



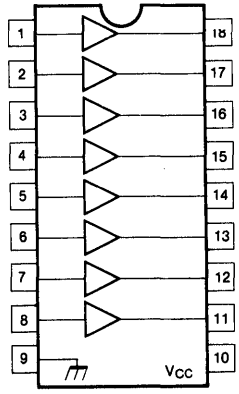
FEATURES

- **Digit or Segment Drivers**
- **Low Input Current**
- **Internal Output Pull-Down Resistors**
- **High Output Breakdown Voltage**
- **Single or Split Supply Operation**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2651N	18 DIP	−20 ~ +85°C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C, Voltages are with reference to ground unless otherwise noted)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	65	V
Input Voltage	V_{IN}	20	V
Output Current	I_{Out}	−40	mA
Operating Temperature	T_{opr}	−20 ~ +85	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	5.0 ~ 50	V
Input ON Voltage	V_{IN}	2.4 ~ 15	V
Output ON Current*	I_{outON}	−25	mA

* Positive (negative) current is defined as going into (coming out of) the specified device pin.

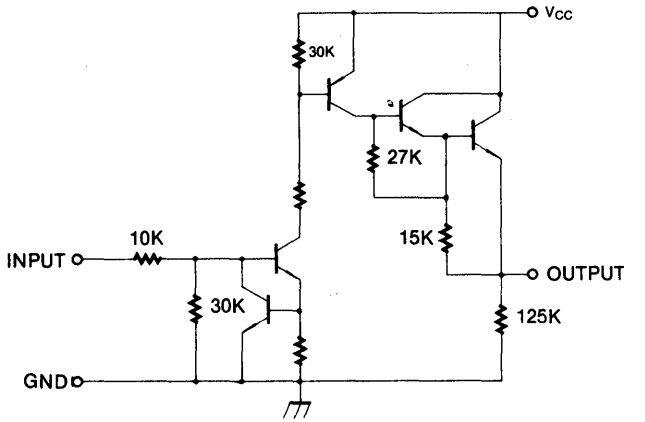
ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 60V, unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Leakage Current	I_{OUTLK}	V_{IN} = 0.4V			15	μA
Output OFF Voltage	V_{OUTOFF}	V_{IN} = 0.4V			1.0	V
Output Pull-Down Current	I_{OUTPD}	Input Open, $V_{OUT} = V_{CC}$	350	550	775	μA
Output ON Voltage	V_{OUTON}	V_{IN} = 2.4V I_{OUT} = −25mA	57	58		V
Input ON Current	I_{IN}	V_{IN} = 2.4V		120	225	μA
		V_{IN} = 5.0V		450	650	μA
Supply Current	I_{CC}	All Inputs Open		10	100	μA
		All Inputs = 2.4V		5.5	8.0	mA

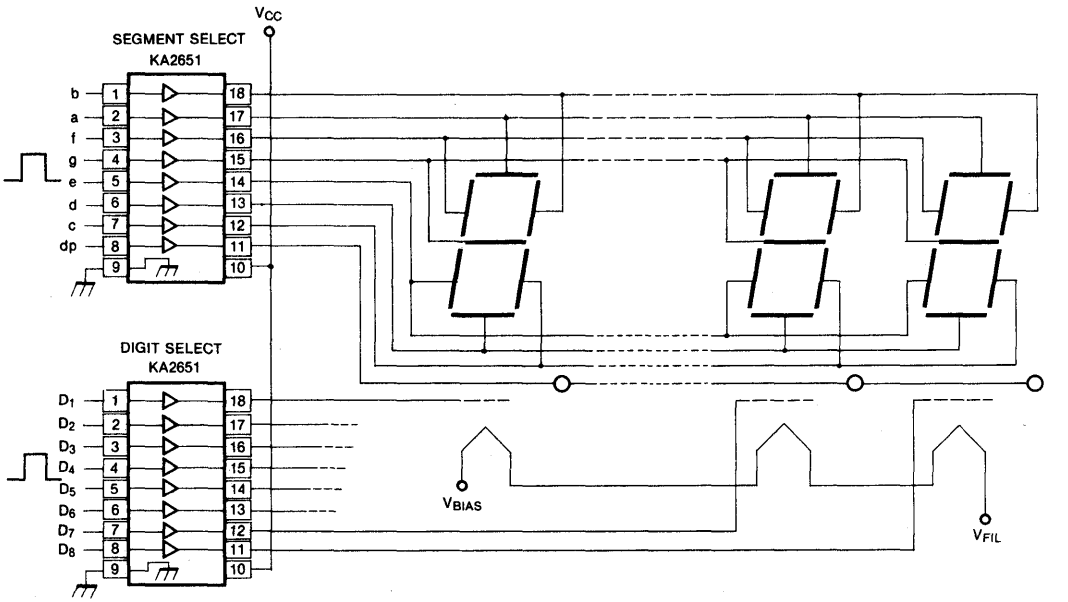
6

PARTIAL SCHEMATIC



(One Driver)

TYPICAL MULTIPLEXED FLUORESCENT DISPLAY



HIGH VOLTAGE, HIGH CURRENT DARLINGTON ARRAYS

The KA2655, KA2656, KA2657, KA2658 and KA2659 are comprised of seven high voltage, high current NPN darlington transistors arrays with common emitter, open collector outputs. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout. Peak inrush currents to 600mA permit them to drive incandescent lamps.

The KA2655 is a general purpose array for use with DTL, TTL, PMOS or CMOS logic directly.

The KA2656 version does away with the need for any external discrete resistors, since each unit has a resistor and a zener diode in series with the input. The KA2656 is designed for use with 14 to 25V PMOS devices. The zener diode also gives these devices excellent noise immunity.

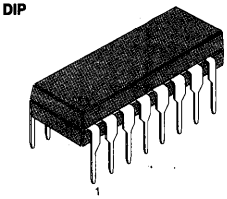
The KA2657 has a series base resistor to each darlington pair, and thus allows operation directly with TTL or CMOS operating at supply voltages of 5V. The KA2657 will handle numerous interfaces needs-particularly those beyond the capabilities of standard logic buffers.

The KA2658 has an appropriate input resistor to allow direct operation from CMOS or PMOS outputs operating supply voltages of 6 to 15V.

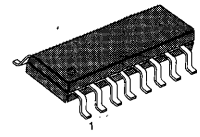
The KA2659 is designed for use with standard TTL and Schottky TTL, with which higher output currents are required and loading of the logic output is not a concern. These devices will sink a minimum of 350mA when driven from a "totempole" logic output.

These versatile devices are useful for driving a wide range of loads including Solenoids, Relays, DC motors, LED displays, Filament lamps, thermal printheads and high power buffer. Applications requiring sink currents beyonds the capability of a single output may be accomodated by paralleling the outputs.

16 DIP



16 SOP



ORDERING INFORMATION

Device	Package	Input Level	Operating Temperature
KA2655N	16 DIP	DTL, TTL, PMOS, CMOS	−20 ~ +85°C
KA2655D	16 SOP		
KA2656N	16 DIP	PMOS	
KA2656D	16 SOP		
KA2657N	16 DIP	TTL, CMOS	
KA2657D	16 SOP		
KA2658N	16 DIP	CMOS, PMOS	
KA2658D	16 SOP		
KA2659N	16 DIP	TTL	
KA2659D	16 SOP		

APPLICATIONS

- Relay driver
- DC motor driver
- Solenoids driver
- LED display driver
- Filament lamp driver
- High power buffer
- Thermal print head driver

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Output Voltage	V_O	50	V
Input Voltage (KA2656/7/8)	V_{IN}	30	V
(KA2659)		15	
Continuous Collector Current	I_C	500	mA
Continuous Input Current	I_{IN}	25	mA
Power Dissipation	P_D	1.0	W
Operating Temperature	T_{opr}	−20 ~ +85	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, unless otherwise noted)

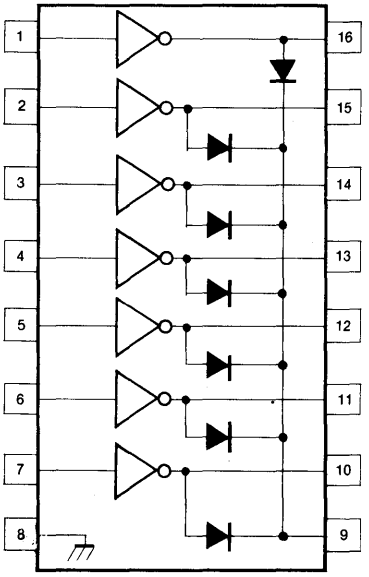
Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Output Leakage Current	I_{LK}	V_{CE} = 50V, Ta = 25°C V_{IN} = open			50	μA
		V_{CE} = 50V, Ta = 70°C V_{IN} = open			100	
		V_{CE} = 50V, Ta = 70°C V_{IN} = 6.0V (KA2656)			500	
		V_{CE} = 50V, Ta = 70°C V_{IN} = 1.0V (KA2658)			500	
Output Saturation Voltage	V_{sat}	I_C = 100mA, I_{IN} = 250μA		0.9	1.1	V
		I_C = 200mA, I_{IN} = 350μA		1.1	1.3	
		I_C = 350mA, I_{IN} = 500μA		1.25	1.6	
Input Current 1 (Off Condition)	$I_{IN}1$	I_C = 500μA, Ta = 70°C	50	65		μA
Input Current 2 (On Condition)	$I_{IN}2$	V_{IN} = 17V (KA2656), V_O = open		0.85	1.3	mA
		V_{IN} = 3.85V (KA2657), V_O = open		0.93	1.35	
		V_{IN} = 5V (KA2658), V_O = open		0.35	0.5	
		V_{IN} = 12V (KA2658), V_O = open		1.0	1.45	
		V_{IN} = 3.0V (KA2659), V_O = open		1.5	2.4	
Input Voltage	V_{IN}	V_{CE} = 2.0V, I_C = 300mA (KA2656)			13	V
		V_{CE} = 2.0V, I_C = 200mA (KA2657)			2.4	
		V_{CE} = 2.0V, I_C = 250mA (KA2657)			2.7	
		V_{CE} = 2.0V, I_C = 300mA (KA2657)			3.0	
		V_{CE} = 2.0V, I_C = 125mA (KA2658)			5.0	
		V_{CE} = 2.0V, I_C = 200mA (KA2658)			6.0	
		V_{CE} = 2.0V, I_C = 275mA (KA2658)			7.0	
		V_{CE} = 2.0V, I_C = 350mA (KA2658)			8.0	
		V_{CE} = 2.0V, I_C = 350mA (KA2659)			2.4	

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, unless otherwise noted)

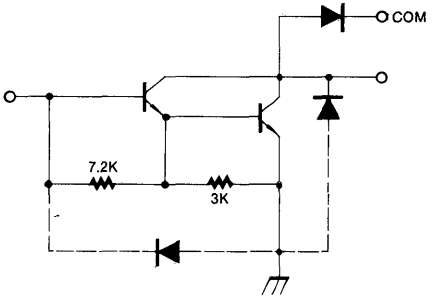
Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
DC Current Gain	h_{FE}	V_{CE} = 2.0V, I_C = 350mA (KA2655)	1000			
Input Capacitance	C_{IN}			15	30	pF
Propagation Delay Time	t_{ON}	0.5 V_{IN} to 0.5 V_O		0.25	1.0	μs
	t_{OFF}	0.5 V_{IN} to 0.5 V_O		0.25	1.0	μs
Clamp Diode Leakage Current	I_R	V_{IN} = open, V_O = GND, V_R = 50V, Ta = 25°C			50	μA
		V_{IN} = open, V_O = GND, V_R = 50V, Ta = 70°C			100	μA
Clamp Diode Forward Voltage	V_F	I_F = 350mA		1.7	2.0	V

PIN CONFIGURATION



SCHEMATIC DIAGRAMS

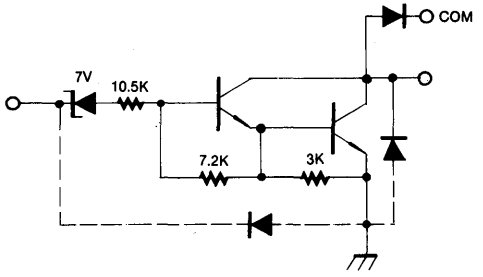
KA2655 (each driver)



6

SCHEMATIC DIAGRAMS

KA2656 (each driver)



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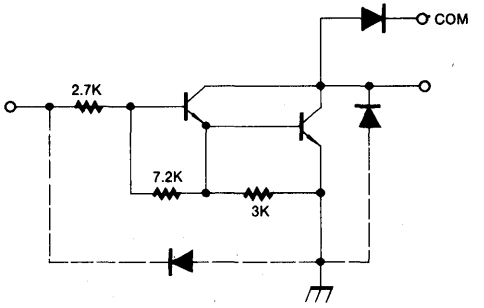

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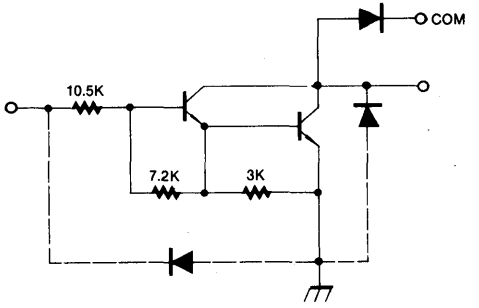
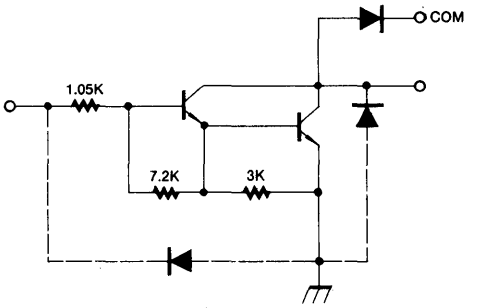


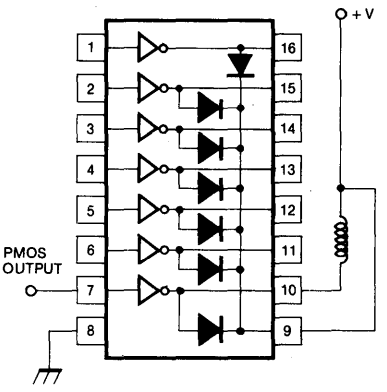
KA2659 (each driver)



TYPICAL APPLICATIONS

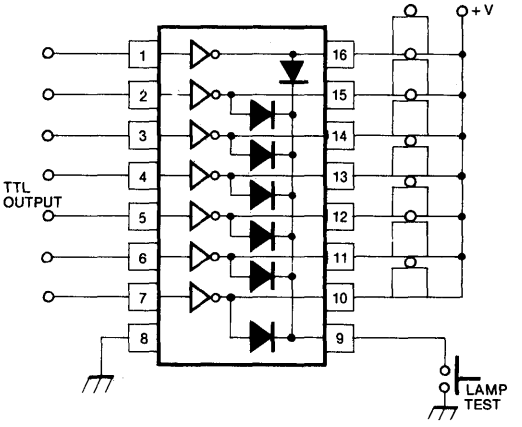
PMOS TO LOAD

KA2656



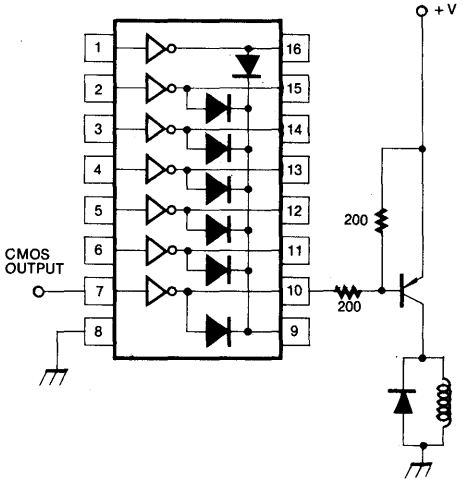
TTL TO LOAD

KA2657/9



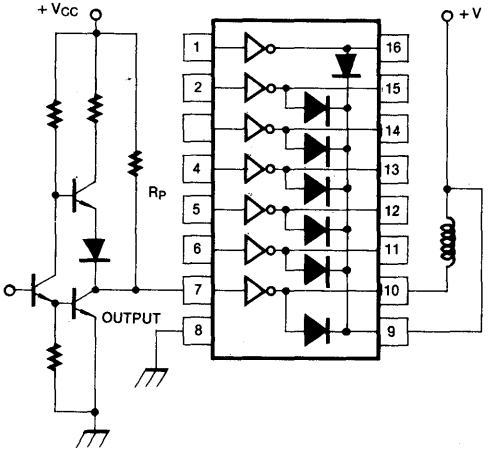
BUFFER FOR HIGH-CURRENT LOAD

KA2658



USE OF PULL-UP RESISTORS TO INCREASE DRIVE CURRENT

KA2657

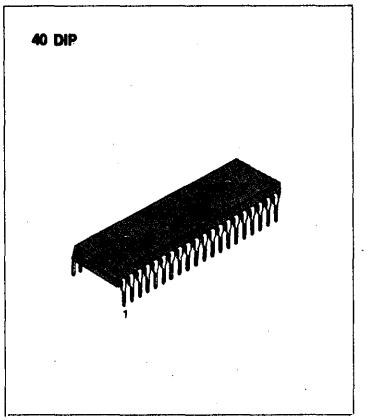


6

QUAD UNIVERSIAL ASYNCHRONOUS RECEIVER AND TRANSMITTER

The KS5812, QUAD-UART, is a Si-Gate CMOS IC which provides the data formatting and control to interface serial asynchronous data communications between main system and subsystems.

The parallel data of the bus system is serially transmitted and by the asynchronous data interface with proper formatting and error checking. The KS5812 includes Transmit part, Receive part, Programmable control part, Status check part, and Select part. The control register that is programmed via the data bus during system initialization, provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control.



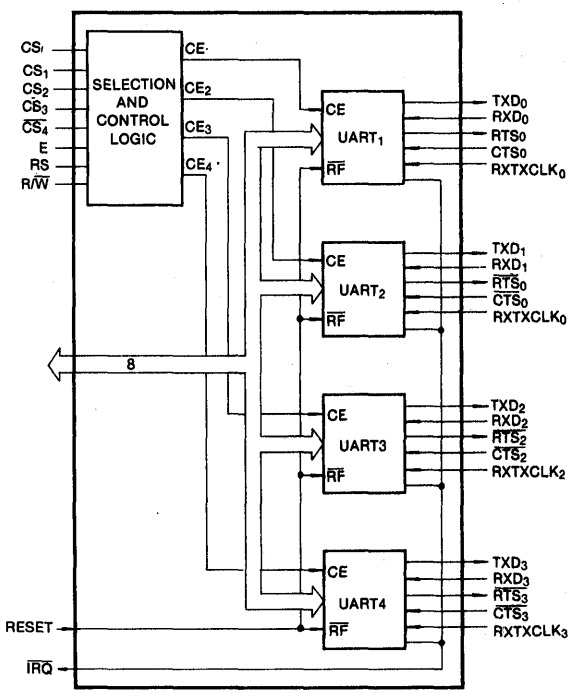
FEATURES

- **Low power, High speed CMOS process.**
- **Serial/Parallel conversion of Data**
- **8-and 9-bit Transmission**
- **Optional Even and Odd Parity**
- **Parity, Overrun and Framing Error Checking**
- **Programmable Control Register**
- **Optional +1, +16, and +64 Clock Modes**
- **Peripheral/Modem Control Functions**
- ***Double Buffered***
- **One-or Two-Stop Bit Operation**

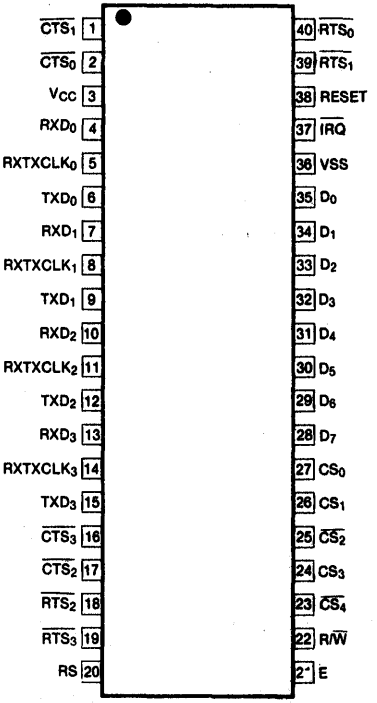
ORDERING INFORMATION

Device	Package	Operating Temperature
KS5812N	40 DIP	−20 ~ +75°C

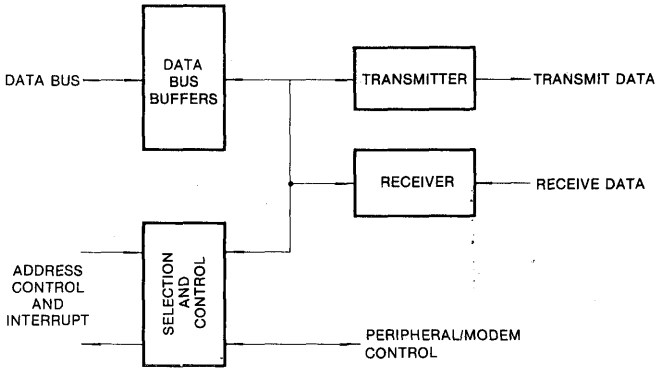
BLOCK DIAGRAM



PIN CONFIGURATION



UART BLOCK DIAGRAM



6

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage*	V_{CC}*	−0.3 to +7.0	V
Input Voltage*	V_{in}*	−0.3 to +7.0	V
Maximum Output Current**	I_C**	10	mA
Operating Temperature	T_{opr}	−20 to +75	°C
Storage Temperature	T_{stg}	−55 to +150	°C

*With respect to V_{SS} (System GND)

**Maximum output current is the maximum current which can flow out from one output terminal or I/O common terminal ($D_0 \sim D_7$, $\overline{RTS}$, Tx Data, $\overline{IRQ}$)

(Note) Permanent IC damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If they are exceeded, it could affect the reliability of the IC.

RECOMMENDED OPERATING CONDITIONS

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{CC}*	4.5	5.0	5.5	V
Input "Low" Voltage		V_{IL}*	0	—	0.8	V
Input "High" Voltage	$D_0 \sim D_7$, RS, $\overline{CTS_i}$, RxD_i	V_{IH}*	2.0	—	V_{CC}	V
	CS_0, CS_2, CS_1 R/$\overline{W}$, E, CS_3, $\overline{CS_4}$, $RXTXCLK_i$		2.2	—	V_{CC}	
Operating Temperature		T_{opr}	−20	25	75	°C

* With respect to V_{SS} (System GND)

DC CHARACTERISTICS ($V_{CC} = +5V \pm 5\%$, $V_{SS} = 0V$, $Ta = -20 \sim +75°C$, unless otherwise noted.)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Input "High" Voltage	$D_0 \sim D_7$, RS, CTSi,	V_{IH}		2.0	—	V_{CC}	V
	CS_0, CS_2, CS_1, R/$\overline{W}$, E, CS_3, $\overline{CS_4}$ RXTXCLKi			2.2	—	V_{CC}	
Input "Low" Voltage	All inputs	V_{IL}		−0.3	—	0.8	V
Input Leakage Current	R/$\overline{W}$, CS_0, CS_1, CS_2, E, CS_3, $\overline{CS_4}$	I_{IN}	$V_{IN} = 0 \sim V_{CC}$	−2.5	—	2.5	μA
Three-State (Off State) Input Current	$D_0 \sim D_7$	I_{TSI}	$V_{IN} = 0.4 \sim V_{CC}$	−10	—	10	μA
Output "High" Voltage	$D_0 \sim D_7$	V_{OH}	$I_{OH} = -400\mu A$	4.1	—	—	V
			$I_{OH} \leq -10\mu A$	V_{CC}-0.1	—	—	
	TXDi, $\overline{RTSi}$		$I_{OH} = -400$	4.1	—	—	
			$I_{OH} \leq -10\mu A$	V_{CC}-0.1	—	—	
Output "Low" Voltage	All outputs	V_{OL}	$I_{OH} = 1.6mA$	—	—	0.4	V
Output Leakage Current (off state)	$\overline{IRQ}$	I_{LOH}	$V_{OH} = V_{CC}$	—	—	10	μA
Input Capacitance	$D_0 \sim D_7$	C_{IN}	$V_{IN} = 0V$, $Ta = 25°C$, $f = 1.0$ MHz	—	—	12.5	pF
	E, RXTXCLKi, R/$\overline{W}$, RS, RXDi, CS_0, CS_1, CS_2, CTS, CS_3, $\overline{CS_4}$			—	—	7.5	
Output Capacitance	$\overline{RTS}$, TXDi	C_{out}	$V_{IN} = 0V$, $Ta = 25°C$, $f = 1.0$ MHz	—	—	10	pF
	$\overline{IRQ}$			—	—	5.0	
Supply Current	• Under transmitting and Receiving operation • 500 kbps • Data bus in R/$\overline{W}$ operation	I_{CC}	E = 1.0 MHz	—	—	3	mA
			E = 1.5 MHz	—	—	4	
			E = 2.0 MHz	—	—	5	
	• Chip is not selected • 500 kbps • Under non transmitting and receiving operation • Input level (Except E) V_{IH} min = $V_{CC} - 0.8V$ V_{IL} max = 0.8V		E = 1.0 MHz	—	—	200	μA
			E = 1.5 MHz	—	—	250	
			E = 2.0 MHz	—	—	300	

AC CHARACTERISTICS (V_{CC} = 5.0V ± 5%, V_{SS} = 0V, Ta = −20 ~ +75°C, unless otherwise noted.)

1. TIMING OF DATA TRANSMISSION

Characteristic		Symbol	Test Conditions	KS5812 Min	KS5812 Max	Unit
Minimum Clock Pulse Width	÷1 Mode	PW_{CL}	Fig. 1	900	—	ns
	÷16, ÷64 Modes			600	—	ns
	÷1 Mode	PW_{CH}	Fig. 2	900	—	ns
	÷16, ÷64 Modes			600	—	ns
Clock Frequency	÷1 Mode	f_C		—	500	KHz
	÷16, ÷64 Modes			—	800	KHz
Clock-to-Data Delay for Transmitter		t_{TDD}	Fig. 3	—	600	ns
Receive Data Setup Time	÷1 Mode	t_{RDSU}	Fig. 4	250	—	ns
Receive Data Hold Time	÷1 Mode	t_{RDH}	Fig. 5	250	—	ns
$\overline{IRQ}$ Release Time		t_{IR}	Fig. 6	—	1200	ns
$\overline{RTS}$ Delay Time		t_{RTS}	Fig. 6	—	560	ns
Rise Time and Fall Time	Except E	t_r, t_f		—	1000*	ns

* 1.0μs or 10% of the pulse width, whichever is smaller.

2. BUS TIMING CHARACTERISTICS

1) READ

Characteristic	Symbol	Test Conditions	KS5812 Min	KS5812 Max	Unit
Enable Cycle Time	$t_{cyc}E$	Fig. 7	1000	—	ns
Enable "High" Pulse Width	PW_{EH}	Fig. 7	450	—	ns
Enable "Low" Pulse Width	PW_{EL}	Fig. 7	430	—	ns
Setup Time, Address and R/$\overline{W}$ Valid to Enable Positive Transition	t_{AS}	Fig. 7	80	—	ns
Data Delay Time	t_{DDR}	Fig. 7	—	290	ns
Data Hold Time	t_H	Fig. 7	20	100	ns
Address Hold Time	t_{AH}	Fig. 7	10	—	ns
Rise and Fall Time for Enable Input	t_{Er}, t_{Ef}	Fig. 7	—	25	ns

2) WRITE

Characteristic	Symbol	Test Conditions	KS5812		Unit
			Min	Max	
Enable Cycle Time	$t_{cyc}E$	Fig. 8	1000	—	ns
Enable "High" Pulse Width	PW_{EH}	Fig. 8	450	—	ns
Enable "Low" Pulse Width	PW_{EL}	Fig. 8	430	—	ns
Setup Time, Address and R/$\overline{W}$ Valid to Enable Positive Transition	t_{AS}	Fig. 8	80	—	ns
Data Setup Time	t_{DSW}	Fig. 8	165	—	ns
Data Hold Time	t_H	Fig. 8	10	—	ns
Address Hold Time	t_{AH}	Fig. 8	10	—	ns
Rise and Fall Time for Enable Input	t_{Er}, t_{Ef}	Fig. 8	—	25	ns

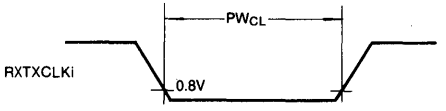


Fig. 1 Clock Pulse Width, "Low" State

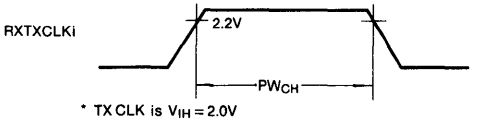


Fig. 2 Clock Pulse Width, "High" State

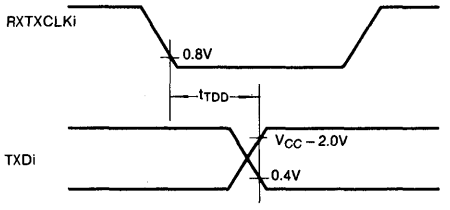


Fig. 3 Transmit Data Output Delay

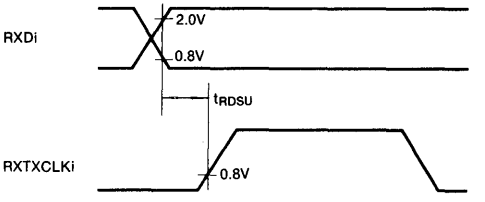


Fig. 4 Receive Data Setup Time (÷1 Mode)

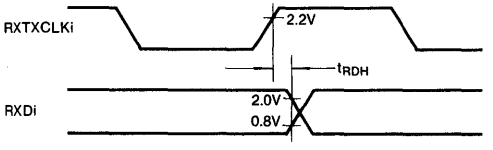
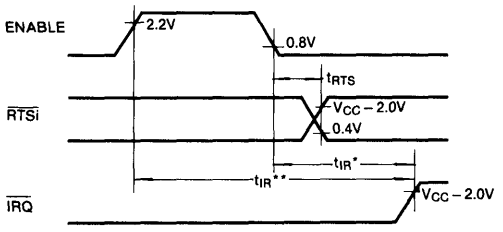


Fig. 5 Receive Data Hold Time (÷1 Mode)



* (1) $\overline{IRQ}$ Release Time applied to R_xDi Register read operation
(2) $\overline{IRQ}$ Release Time applied to T_xDi Register write operation
(3) $\overline{IRQ}$ Release Time applied to control Register write TIE = 0, RIE = 0 operation.

** $\overline{IRQ}$ Release Time applied to R_X Data Register read operation right after read status register, when $\overline{IRQ}$ is asserted by DCD rising edge.

Note: Note that the following takes place when $\overline{IRQ}$ is asserted by the detection of transmit data register empty status. $\overline{IRQ}$ is released to "High" asynchronously with E signal when $\overline{CTSi}$ goes "High". (Refer to Figure 14)

Fig. 6 $\overline{RTSi}$ Delay and $\overline{IRQ}$ Release Time

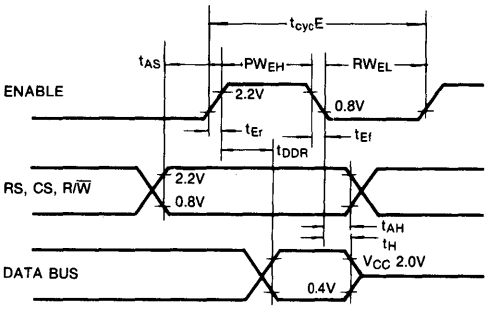


Fig. 7 Bus Read Timing Characteristics (Read information from UART)

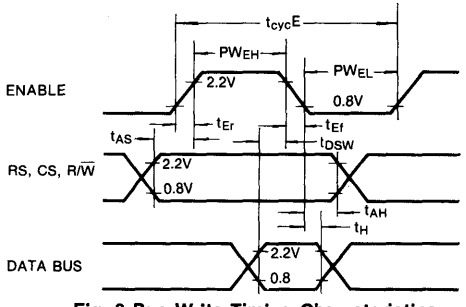


Fig. 8 Bus Write Timing Characteristics (Write information into UART)

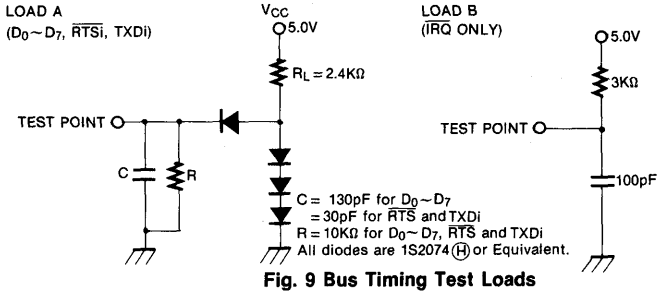


Fig. 9 Bus Timing Test Loads

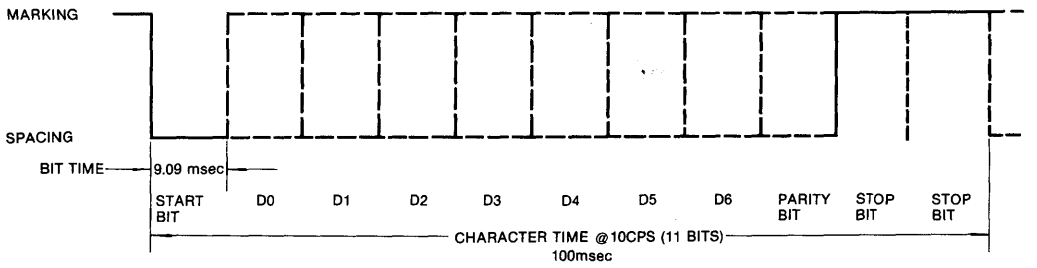


Fig. 10 110 Baud Serial ASCII Data Timing

DEVICE OPERATION

At the bus interface, the UARTi appears as two addressable memory locations. Internally, there are four registers: two read-only and two write-only registers. The read-only registers are Status and Receive Data; the write-only registers are Control and Transmit Data. The serial interface consists of serial input and output lines with independent clocks, and three peripheral/modem control lines.

POWER ON/MASTER RESET

The master reset (CR0, CR1) should be set during system initialization to insure the reset condition and prepare for programming the UARTi functional configuration when the communications channel is required. During the first master reset, the $\overline{IRQ}$ and $\overline{RTSi}$ outputs are held at level 1. On all other master resets, the $\overline{RTSi}$ output can be programmed high or low with the $\overline{IRQ}$ output held high. Control bits CR5 and CR6 should also be programmed to define the state of $\overline{RTSi}$ whenever master reset is utilized. The UARTi also contains internal power-on reset logic to detect the power line turn-on transition and hold the chip in a reset state to prevent erroneous output transitions prior to initialization. This circuitry depends on clean power turn-on transitions. The power-on reset is released by means of the bus-programmed master reset which must be applied prior to operating the UARTi. After master resetting the UARTi, the programmable Control Register can be set for a number of options such as variable clock divider ratios, variable word length, one or two stop bits, parity (even, odd, or none), etc.

TRANSMIT

A typical transmitting sequence consists of reading the UARTi. Status Register either as a result of an interrupt or in the UARTi's turn in a polling sequence. A character may be written into the Transmit Data Register if the status read operation has indicated that the Transmit Data Register is empty. This character is transferred to Shift Register where it is serialized and transmitted from the Transmit Data output preceded by a start bit and followed by one or two stop bits. Internal parity (odd or even) can be optionally added to the character and will occur between the last data bit and the first stop bit. After the first character is written in the Data Register, the Status Register can be read again to check for a Transmit Data Register Empty condition and current peripheral status. If the Register is empty, another character can be loaded for transmission even though the first character is in the process of being transmitted (because of double buffering). The second character will be automatically transferred into the Shift Register when the first character transmission is completed. This sequence continues until all the characters have been transmitted.

RECEIVE

Data is received from a peripheral by means of the Receive Data input. A divide-by-one clock ratio is provided for an externally synchronized clock (to its data) while the divide by-16 and 64 ratios are provided for internal synchronization. Bit synchronization in the divide-by-16 and 64 modes is initiated by the detection of 8 or 32 low samples on the receive line in the divide-by-16 and 64 modes respectively. False start bit deletion capability insures that a full half bit of a start bit has been received before the internal clock is synchronized to the bit time. As a character is being received, parity (odd or even) will be checked and the error indication will be available in the Status Register along with framing error, overrun error, and Receive Data Register full. In a typical receiving sequence, the Status Register is read to determine if a character has been received from a peripheral. If the Receiver Data Register is full, the character is placed on the 8-bit UARTi bus when a Read Data command is received from the MPU. When parity has been selected for a 7-bit word (7 bits plus parity), the receiver strips the parity bit (D7 = 0) so that data alone is transferred to the MPU. This feature reduces MPU programming. The Status Register can continue to be read to determine when another character is available in the Receive Data Register. The receiver is also double buffered so that a character can be read from the data register as another character is being received in the shift register. The above sequence continues until all characters have been received.

INPUT/OUTPUT FUNCTIONS

UART INTERFACE SIGNALS FOR MPU

The KS5812 interfaces to the MPU with an 8-bit bidirectional data bus, five chip select lines, a register select line, an interrupt request line, read/write line, and enable line. These signals permit the MPU to have complete control over the KS5812.

UART Bidirectional Data (D0-D7) — The bidirectional data lines (D0-D7) allow for data transfer between the KS5812 and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an UARTi read operation.

UART Enable (E) — The Enable signal, E, is a high-impedance TTL-compatible input that enables the bus

input/output data buffers and clocks data to and from the KS5812.

Read/Write (R/$\overline{W}$) — The Read/Write line is a high-impedance input that is TTL compatible and is used to control the direction of data flow through the UARTi's input/output data bus interface. When Read/Write is high (MPU Read cycle), KS5812 output drivers are turned on and a selected register is read. When it is low, the KS5812 output drivers are turned off and the MPU writes into a selected register. Therefore, the Read/Write signal is used to select read-only or write-only registers within the KS5812.

Chip Select (CS0, CS1, CS2, CS3, $\overline{CS4}$) — These five high-impedance TTL-compatible input lines are to select and address the KS5812. Each UART can be enabled when CS2 and CS3 are high and $\overline{CS4}$ is low. CS0 and CS1 are used to select individual UART.

CS0	CS1	CS2	CS3	CS4	UARTi
0	0	1	1	0	UART1
0	1	1	1	0	UART2
1	0	1	1	0	UART3
1	1	1	1	0	UART4

Register Select (RS) — The Register Select line is a high-impedance input that is TTL compatible. A high level is used to select the Transmit/Receive Data Registers and a low level the Control/Status Registers. The Read/Write signal line is used in conjunction with Register Select to select the read-only or write-only register in each register pair.

Interrupt Request ($\overline{IRQ}$) — Interrupt Request is a TTL-compatible, open-drain (no internal pullup), active low output that is used to interrupt the MPU. The $\overline{IRQ}$ output remains low as long as the cause of the interrupt is present and the appropriate interrupt enable within the KS5812 is set. The $\overline{IRQ}$ status bit, when high, indicates the $\overline{IRQ}$ output is in the active state.

Interrupts result from conditions in both the transmitter and receiver sections of the UARTi. The transmitter section causes an interrupt when the Transmitter Interrupt Enabled condition is selected (CR5•$\overline{CR6}$), and the Transmit Data Register Empty (TDRE) status bit is high. The TDRE status bit indicates the current status of the Transmitter Data Register except when inhibited by Clear-to-Send ($\overline{CTSi}$) being high or the UARTi being maintained in the Reset condition. The interrupt is cleared by writing data into the Transmit Data Register. The interrupt is masked by disabling the Transmitter Interrupt via CR5 or CR6 or by the loss of $\overline{CTSi}$ which inhibits the TDRE status bit. The Receiver section causes an interrupt when the Receiver Interrupt Enable is set and the Receive Data Register Full (RDRF) status bit is high, an Overrun has occurred. An interrupt resulting from the RDRF status bit can be cleared by reading data or resetting the UARTi. Interrupts caused by Overrun are cleared by reading the status register after the error condition has occurred and then reading the Receive Data Register or resetting the UARTi. The receiver interrupt is masked by resetting the Receiver Interrupt Enable.

CLOCK INPUTS

High-impedance TTL-compatible inputs are provided for clocking of transmitted and received data. Clock frequencies of 1, 16, or 64 times the data rate may be selected.

RECEIVE AND TRANSMITTER CLOCK (RXTXCLKi)

—The RXTXCLKi input are both used for the clocking of transmitted data and for synchronization of received data. (In the /1 mode, the clock and data must be synchronized externally.) The transmitter initiates data on the negative transition of the clock and the receiver samples the data on the positive transition of the clock.

SERIAL INPUT/OUTPUT LINES

Receive Data (RXDi) — The Receive Data line is a high-impedance TTL-compatible input through which data is received in a serial format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used.

Transmit Data (TXDi) — The Transmit Data output line transfers serial data to a modem or other peripheral.

PERIPHERAL/MODEM CONTROL

The UARTi includes several functions that permit limited control of a peripheral or modem. The functions included are Clear-to-Send, Request-to-Send and Data Carrier Detect.

Clear-to-Send ($\overline{CTSi}$) — This high-impedance TTL-compatible input provides automatic control of the transmitting end of a communications link via the modem Clear-to-Send active low output by inhibiting the Transmit Data Register Empty (TDRE) status bit.

Request-to-Send ($\overline{RTSi}$) — The Request-to-Send output enables the MPU to control a peripheral or modem via the data bus. The $\overline{RTSi}$ output corresponds to the state of the Control Register bits CR5 and CR6. When CR6 = 0 or both CR5 and CR6 = 1, the $\overline{RTSi}$ output is low (the active state). This output can also be used for Data Terminal Ready (DTR).

TRANSMIT DATA REGISTER (TDR)

Data is written in the Transmit Data Register during the negative transition of the enable (E) when the UARTi has been addressed with RS high and R/$\overline{W}$ low. Writing data into the register causes the Transmit Data Register Empty bit in the Status Register to go low. Data can then be transmitted. If the transmitter is idling and no character is being transmitted, then the transfer will take place within 1-bit time of the trailing edge of the Write command. If a character is being transmitted, the new data character will commence as soon as the previous character is complete. The transfer of data causes the Transmit Data Register Empty (TDRE) bit to indicate empty.

RECEIVE DATA REGISTER (RDR)

Data is automatically transferred to the empty Receive Data Register (RDR) from the receiver deserializer (a shift register) upon receiving a complete character. This event causes the Receive Data Register Full bit (RDRF) in the status buffer to go high (full). Data may then be read through the bus by addressing the UARTi and selecting the Receive Data Register with RS and R/$\overline{W}$ high when the UARTi is enabled. The non-destructive read cycle causes the RDRF bit to be cleared to empty although the data is retained in the RDR. The status is maintained by RDRF as to whether or not the data is current. When the Receive Data Register is full, the automatic transfer of data from the Receiver Shift Register to the Data Register is inhibited and the RDR contents remain valid with its current status stored in the Status Register.

CONTROL REGISTER

The UARTi Control Register consists of eight bits of write-only buffer that are selected when RS and R/$\overline{W}$ are low. This register controls the function of the receiver, transmitter, interrupt enables, and the Request-to-Send peripheral/modem control output.

Counter Divide Select Bits (CR0 and CR1) — The Counter Divide Select Bits (CR0 and CR1) determine the divide ratios utilized in both the transmitter and receiver sections of the UARTi. Additionally, these bits are used to provide a master reset for the UARTi which clears the Status Register (except for external conditions on $\overline{CTSi}$ and $\overline{DCD}$) and initializes both the receiver and transmitter. Master reset does not affect other Control Register bits. Note that after power-on or a power fail/restart, these bits must be set high to reset the UARTi. After resetting, the clock divide ratio may be selected. These counter select bits provide for the following clock divide ratios:

CR1	CR0	Function
0	0	÷ 1
0	1	÷ 16
1	0	÷ 64
1	1	Master Reset

Word Select Bits (CR2, CR3, and CR4) — The Word Select bits are used to select word length, parity, and the number of stop bits. The encoding format is as follows;

CR4	CR3	CR2	Function
0	0	0	7 Bits + Even Parity + 2 Stop Bits
0	0	1	7 Bits + Odd Parity + 2 Stop Bits
0	1	0	7 Bits + Even Parity + 1 Stop Bit
0	1	1	7 Bits + Odd Parity + 1 Stop Bit
1	0	0	8 Bits + 2 Stop Bits
1	0	1	8 Bits + 1 Stop Bit
1	1	0	8 Bits + Even Parity + 1 Stop Bit
1	1	1	8 Bits + Odd Parity + 1 Stop Bit

Word length, Parity Select, and Stop Bit changes are not buffered and therefore become effective immediately.

Transmitter Control Bits (CR5 and CR6) — Two Transmitter Control bits provide for the control of the interrupt from the Transmit Data Register Empty condition, the Request-to-Send ($\overline{RTSi}$) output, and the transmission of a Break level (space). The following encoding format is used:

CR6	CR5	Function
0	0	$\overline{RTSi}$ = low, Transmitting Interrupt Disabled.
0	1	$\overline{RTSi}$ = low, Transmitting Interrupt Enabled.
1	0	$\overline{RTSi}$ = high, Transmitting Interrupt Disabled.
1	1	RTS = low, Transmits a Break level on the Transmit Data Output. Transmitting Interrupt Disabled.

Receive Interrupt Enable Bit (CR7) — The following interrupts will be enabled by a high level in bit position 7 of the Control Register (CR7). Receive Data Register Full Overrun.

STATUS REGISTER

Information on the status of the UARTi is available to the MPU by reading the UARTi Status Register. This read only register is selected when RS is low and R/$\overline{W}$ is high. Information stored in this register indicates the

status of the Transmit Data Register, the Receive Data Register and error logic, and the peripheral/modem status inputs of the UARTi

Receive Data Register Full (RDRF), Bit 0 — Receive Data Register Full indicates that received data has been transferred to the Receive Data Register. RDRF is cleared after an MPU read of the Receive Data Register or by a master reset. The cleared or empty state indicates that the contents of the Receive Data Register are not current. Data Carrier Detect being high also causes RDRF to indicate empty.

Transmit Data Register Empty (TDRE), Bit 1 — The Transmit Data Register Empty bit being set high indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The low state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

Clear-to-Send ($\overline{CTS}$), Bit 3 — The Clear-to-Send bit indicates the state of the Clear-to-Send input from a modem. A low $\overline{CTS}$ indicates that there is a Clear-to-Send from the modem. In the high state, the Transmit Data Register Empty bit is inhibited and the Clear-to-Send status bit will be high. Master reset does not affect the Clear-to-Send status bit.

Framing Error (FE), Bit 4 — Framing error indicates that the received character is improperly framed by a start and a stop bit and is detected by the absence of the first stop bit. This error indicates a synchronization error, faulty transmission, or a break condition. The framing error flag is set or reset during the receive data transfer time. Therefore, this error indicator is present throughout the time that the associated character is available.

Receiver Overrun (OVRN), Bit 5 — Overrun is an error flag the indicates that one or more characters in the data stream were lost. That is, a character or a number of characters were received but not read from the Receive Data Register (RDR) prior to subsequent characters being received. The overrun condition begins at the midpoint of the last bit of the second character received in succession without a read of the HDR having occurred. The Overrun does not occur in the Status Register until the valid character prior to Overrun has been read. The RDRF bit remains set until the Overrun is reset. Character synchronization is maintained during the Overrun condition. The Overrun indication is reset after the reading of data from the Receive Data Register or by a Master Reset.

Parity Error (PE), Bit 6 — The parity error flag indicates that the number of highs (ones) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication will be present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver parity check results are inhibited.

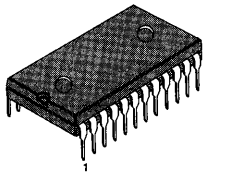
Interrupt Request ($\overline{IRQ}$), Bit 7 — The $\overline{IRQ}$ bit indicates the state of the $\overline{IRQ}$ output. Any interrupt condition with its applicable enable will be indicated in this status bit. Anytime the $\overline{IRQ}$ output is low the $\overline{IRQ}$ bit will be high to indicate the interrupt or service request status. $\overline{IRQ}$ is cleared by a read operation to the Receive Data Register or a write operation to the Transmit Data Register.

UNIVERSAL ASYNCHRONOUS RECEIVER AND TRANSMITTER

The KS5824 UART, is a Si-gate CMOS IC which provides the data formatting and control to interface serial asynchronous data communications between main systems and subsystems.

The bus interface of the KS5824 includes select, enable, read/write, interrupt and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially, transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the UART is programmed via the data bus during system initialization. A programmable control register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control. For peripheral or modem operation, three control lines are provided. Exceeding Low Power dissipation is realized due to adopting CMOS process.

24 DIP



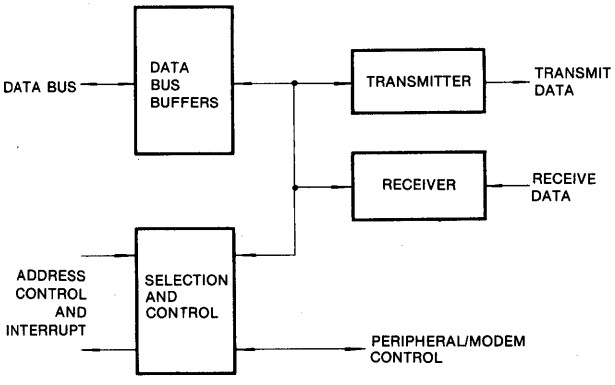
FEATURES

- **Low-power, high-speed, CMOS process**
- **Serial/parallel conversion of data**
- **8-and 9-bit transmission**
- **Optional even and odd parity**
- **Parity, overrun and framing error checking**
- **Programmable control register**
- **Optional ÷1, ÷16, and ÷64 clock modes**
- **Peripheral/modem control functions**
- **Double buffered**
- **One-or two-stop bit operation**

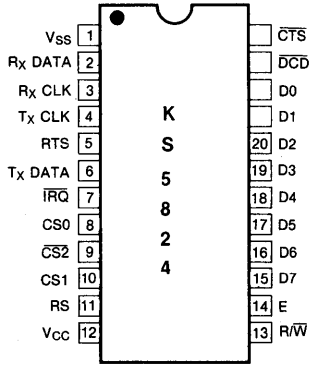
ORDERING INFORMATION

Device	Package	Operating Temperature
KS5824N	24 DIP	−20 ~ +75°C

BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}*	−0.3 to +7.0	V
Input Voltage	V_{IN}*	−0.3 to +7.0	V
Maximum Output Current	I_O**	10	mA
Operating Temperature	T_{opr}	−20 to +75	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* With respect to V_{SS} (SYSTEM GND)

** Maximum output current is the maximum current which can flow out from one output terminal or I/O common terminal (D_0~D_7, $\overline{RTS}$, T_X Data, $\overline{IRQ}$).

Note: Permanent IC damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions are exceeded, it could affect reliability of IC.

RECOMMENDED OPERATING CONDITIONS

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{CC}*	4.5	5.0	5.5	V
Input "Low" Voltage		V_{IL}*	0	—	0.8	V
Input "High" Voltage	D_0~D_7, RS, T_X CLK, $\overline{DCD}$, $\overline{CTS}$, R_X Data	V_{IH}*	2.0	—	V_{CC}	V
	CS_0, $\overline{CS_2}$, CS_1, R/$\overline{W}$, E, R_X CLK		2.2	—	V_{CC}	
Operating Temperature		T_{opr}	−20	25	75	°C

* With respect to V_{SS} (SYSTEM GND)

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (V_{CC} = 5V ± 5%, V_{SS} = 0V, Ta = −20 ~ +75°C, unless otherwise noted.)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Input "High" Voltage	D_0 ~ D_7, RS, T_X CLK, $\overline{DCD}$, $\overline{CTS}$, R_X Data	V_{IH}		2.0		V_{CC}	V
	CS_0, $\overline{CS_2}$, CS_1, R/$\overline{W}$, E, R_X CLK			2.2		V_{CC}	
Input "Low" Voltage	All inputs	V_{IL}		−0.3		0.8	V
Input Leakage Current	R/$\overline{W}$, CS_0, CS_1, $\overline{CS_2}$, E	I_{IN}	V_{IN} = 0 ~ V_{CC}	−2.5		2.5	μA
Three-State (Off State) Input Current	D_0 ~ D_7	I_{TSI}	V_{IN} = 0.4 ~ V_{CC}	−10		10	μA
Output "High" Voltage	D_0 ~ D_7	V_{OH}	I_{OH} = −205μA	2.4			V
	T_X data, $\overline{RTS}$		I_{OH} = −100μA	2.4			
Output "Low" Voltage	All outputs	V_{OL}	I_{OH} = 1.6mA			0.4	V

DC CHARACTERISTICS (Continued)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Output Leakage Current (Off State)	$\overline{IRQ}$	I_{LOH}	$V_{OH} = V_{CC}$	—	—	10	μA
Input Capacitance	$D_0 \sim D_7$	C_{IN}	$V_{IN} = 0V$, $Ta = 25°C$, $f = 1.0MHz$	—	—	12.5	pF
	E, T_X CLK, R_X CLK, R/$\overline{W}$, RS, R_X Data, CS_0, CS_1, $\overline{CS_2}$, $\overline{CTS}$, $\overline{DCD}$			—	—	7.5	
Output Capacitance	$\overline{RTS}$, T_X Data	C_{OUT}	$V_{IN} = 0V$, $Ta = 25°C$ $f = 1.0MHz$	—	—	10	pF
	$\overline{IRQ}$			—	—	5.0	
Supply Current	• Under transmitting and receiving operation • 500 kbps • Data bus in R/$\overline{W}$ operation	I_{CC}	E = 1.0MHz	—	—	3	mA
			E = 1.5MHz	—	—	4	
			E = 2.0MHz	—	—	5	
	• Chip is not selected • 500 kbps • Under non transmitting and receiving operation • Input level (Except E) V_{IH} min = $V_{CC} - 0.8V$ V_{IL} max = 0.8V		E = 1.0MHz	—	—	200	μA
			E = 1.5MHz	—	—	250	
			E = 2.0MHz	—	—	300	

AC CHARACTERISTICS ($V_{CC} = 5.0V \pm 5\%$, $V_{SS} = 0V$, $Ta = -20 \sim +75°C$, unless otherwise noted.)

1. TIMING OF DATA TRANSMISSION

Characteristic		Symbol	Test Conditions	Min	Max	Unit
Minimum Clock Pulse Width	÷1 Mode	PW_{CL}	Fig. 1	900	—	ns
	÷16, ÷64 Modes			600	—	ns
	÷1 Mode	PW_{CH}	Fig. 2	900	—	ns
	÷16, ÷64 Modes			600	—	ns
Clock Frequency	÷1 Mode	f_C		—	500	KHz
	÷16, ÷64 Modes			—	800	KHz
Clock-to-Data Delay for Transmitter		t_{TDD}	Fig. 3	—	600	ns
Receive Data Setup Time	÷1 Mode	t_{RDSU}	Fig. 4	250	—	ns
Receive Data Hold Time	÷1 Mode	t_{RDH}	Fig. 5	250	—	ns
$\overline{IRQ}$ Release Time		t_{IR}	Fig. 6	—	1200	ns
$\overline{RTS}$ Delay Time		t_{RTS}	Fig. 6	—	560	ns
Rise Time and Fall Time	Except E	t_r, t_f		—	1000*	ns

* 1.0μs or 10% of the pulse width, whichever is smaller.

2. BUS TIMING CHARACTERISTICS

1) READ

Characteristic	Symbol	Test Conditions	Min	Max	Unit
Enable Cycle Time	$t_{cyc}E$	Fig. 7	1000	—	ns
Enable "High" Pulse Width	PW_{EH}	Fig. 7	450	—	ns
Enable "Low" Pulse Width	PW_{EL}	Fig. 7	430	—	ns
Setup Time, Address and R/$\overline{W}$ Valid to Enable Positive Transition	t_{AS}	Fig. 7	80	—	ns
Data Delay Time	t_{DDR}	Fig. 7	—	290	ns
Data Hold Time	t_H	Fig. 7	20	100	ns
Address Hold Time	t_{AH}	Fig. 7	10	—	ns
Rise and Fall Time for Enable Input	t_{Er}, t_{Ef}	Fig. 7	—	25	ns

2) WRITE

Characteristic	Symbol	Test Conditions	Min	Max	Unit
Enable Cycle Time	$t_{cyc}E$	Fig. 8	1000	—	ns
Enable "High" Pulse Width	PW_{EH}	Fig. 8	450	—	ns
Enable "Low" Pulse Width	PW_{EL}	Fig. 8	430	—	ns
Setup Time, Address and R/$\overline{W}$ Valid to Enable Positive Transition	t_{AS}	Fig. 8	80	—	ns
Data Setup Time	t_{DSW}	Fig. 8	165	—	ns
Data Hold Time	t_H	Fig. 8	10	—	ns
Address Hold Time	t_{AH}	Fig. 8	10	—	ns
Rise and Fall Time for Enable Input	t_{Er}, t_{Ef}	Fig. 8	—	25	ns

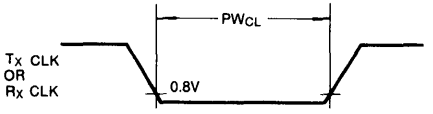
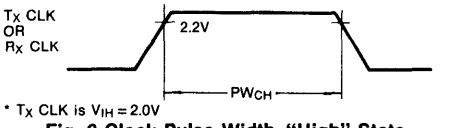


Fig. 1 Clock Pulse Width, "Low" State



* T_X CLK is $V_{IH} = 2.0V$

Fig. 2 Clock Pulse Width, "High" State

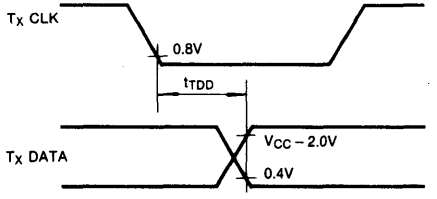


Fig. 3 Transmit Data Output Delay

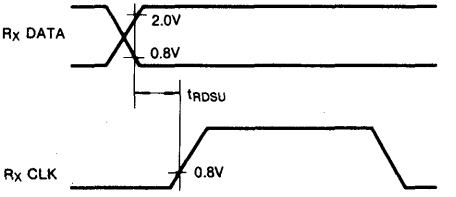


Fig. 4 Receive Data Setup Time (÷1 Mode)

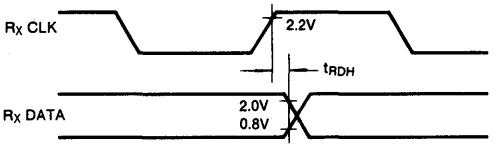


Fig. 5 Receive Data Hold Time (÷1 Mode)

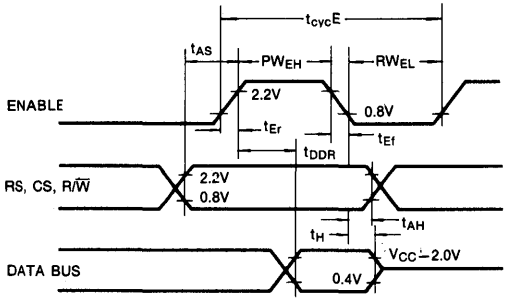
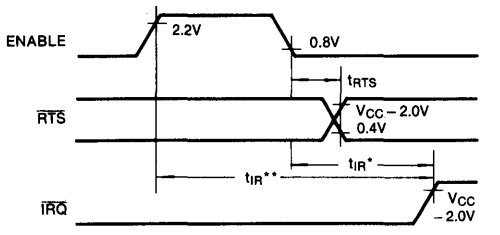


Fig. 7 Bus Read Timing Characteristics (Read information from UART)



* (1) $\overline{IRQ}$ Release Time applied to R_X Data Register read operation.
(2) $\overline{IRQ}$ Release Time applied to T_X Data Register write operation
(3) $\overline{IRQ}$ Release Time applied to control Register write TIE = 0, RIE = 0 operation.

** $\overline{IRQ}$ Release Time applied to R_X Data Register read operation right after read status register, when $\overline{IRQ}$ is asserted by $\overline{DCD}$ rising edge.

Note: Note that following take place when $\overline{IRQ}$ is asserted by the detection of transmit data register empty status. $\overline{IRQ}$ is released to "High" asynchronously with E signal when $\overline{CTS}$ goes "High". (Refer to Figure 14)

Fig. 6 $\overline{RTS}$ Delay and $\overline{IRQ}$ Release Time

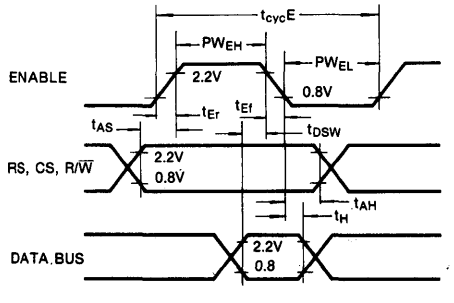


Fig. 8 Bus Write Timing Characteristics (Write information into UART)

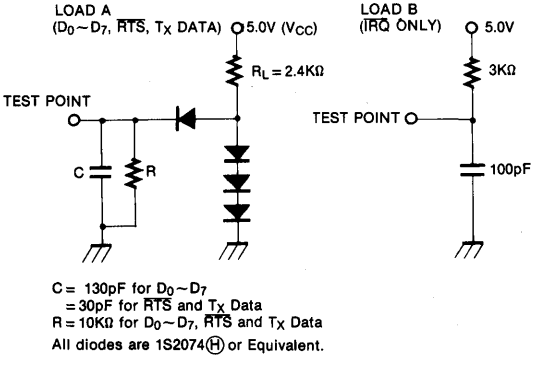


Fig. 9 Bus Timing Test Loads

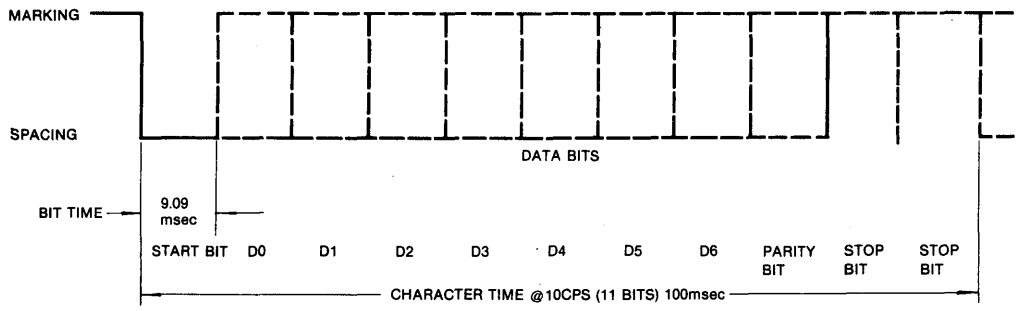


Fig. 10 110 Baud Serial ASCII Data Timing

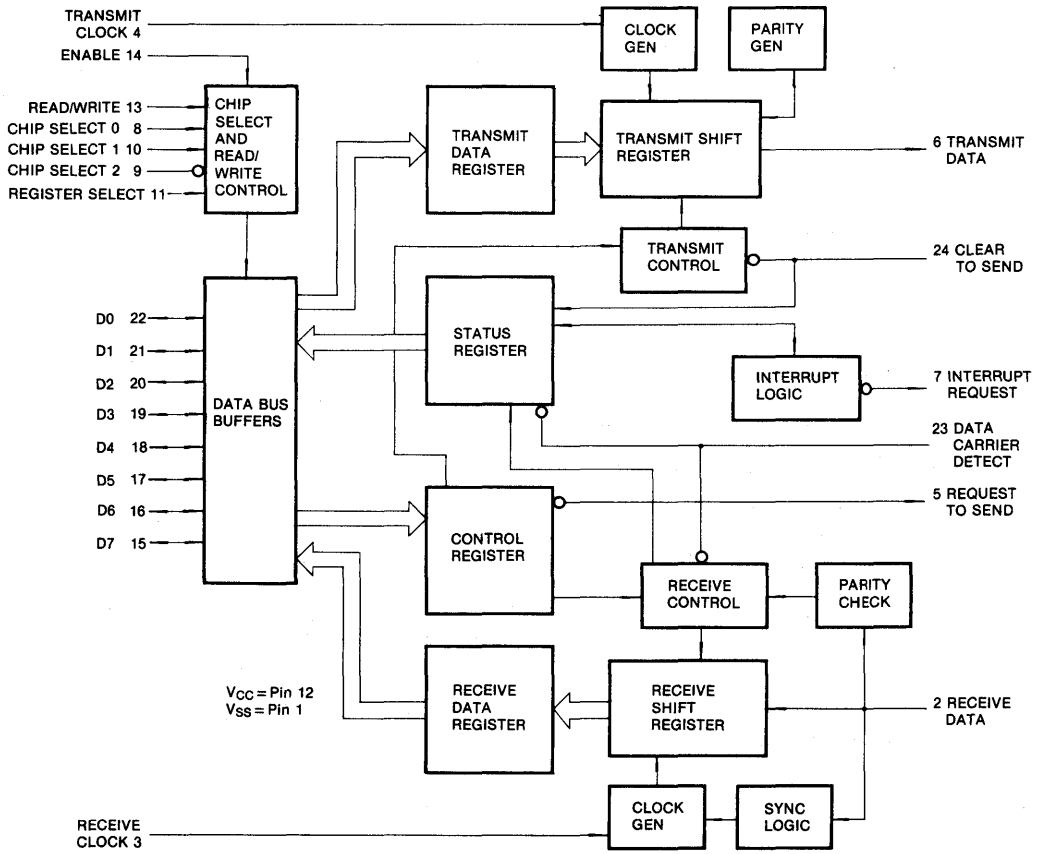


Fig. 11 Expanded Block Diagram

DEVICE OPERATION

At the bus interface, the UART appears as two addressable memory locations. Internally, there are four registers: two read-only and two write-only registers. The read-only registers are Status and Receive Data; the write-only registers are Control and Transmit Data. The serial interface consists of serial input and output lines with independent clocks, and three peripheral/modem control lines.

POWER ON/MASTER RESET

The master reset (CR0, CR1) should be set during system initialization to insure the reset condition and prepare for programming the UART functional configuration when the communications channel is required. During the first master reset, the $\overline{IRQ}$ and $\overline{RTS}$ outputs are held at level 1. On all other master resets, the $\overline{RTS}$ output can be programmed high or low with the $\overline{IRQ}$ output held high. Control bits CR5 and CR6 should also be programmed to define the state of $\overline{RTS}$ whenever master reset is utilized. The UART also contains internal power-on reset logic to detect the power line turn-on transition and hold the chip in a reset state to prevent erroneous output transitions prior to initialization. This circuitry depends on clean power turn-on transitions. The power-on reset is released by means of the bus-programmed master reset which must be applied prior to operating the UART. After master resetting the UART, the programmable Control Register can be set for a number of options such as variable clock divider ratios, variable word length, one or two stop bits, parity (even, odd, or none), etc.

TRANSMIT

A typical transmitting sequence consists of reading the UART. Status Register either as a result of an interrupt or in the UART's turn in a polling sequence. A character may be written into the Transmit Data Register if the status read operation has indicated that the Transmit Data Register is empty. This character is transferred to a Shift Register where it is serialized and transmitted from the Transmit Data output preceded by a start bit and followed by one or two stop bits. Internal parity (odd or even) can be optionally added to the character and will occur between the last data bit and the first stop bit. After the first character is written in the Data Register, the Status Register can be read again to check for a Transmit Data Register Empty condition and current peripheral status. If the register is empty, another character can be loaded for transmission even though the first character is in the process of being transmitted (because of double buffering). The second character will be automatically transferred into the Shift Register when the first character transmission is completed. This sequence continues until all the characters have been transmitted.

RECEIVE

Data is received from a peripheral by means of the Receive Data input. A divide-by-one clock ratio is provided for an externally synchronized clock (to its data) while the divide-by-16 and 64 ratios are provided for internal synchronization. Bit synchronization in the divide-by-16 and 64 modes is initiated by the detection of 8 or 32 low samples on the receive line in the divide-by-16 and 64 modes respectively. False start bit deletion capability insures that a full half bit of a start bit has been received before the internal clock is synchronized to the bit time. As a character is being received, parity (odd or even) will be checked and the error indication will be available in the Status Register along with framing error, overrun error, and Receive Data Register full. In a typical receiving sequence, the Status Register is read to determine if a character has been received from a peripheral. If the Receiver Data Register is full, the character is placed on the 8-bit UART bus when a Read Data command is received from the MPU. When parity has been selected for a 7-bit word (7 bits plus parity), the receiver strips the parity bit (D7 = 0) so that data alone is transferred to the MPU. This feature reduces MPU programming. The Status Register can continue to be read to determine when another character is available in the Receive Data Register. The receiver is also double buffered so that a character can be read from the data register as another character is being received in the shift register. The above sequence continues until all characters have been received.

INPUT/OUTPUT FUNCTIONS

UART INTERFACE SIGNALS FOR MPU

The KS5824 interfaces to the MPU with an 8-bit bidirectional data bus, three chip select lines, a register select line, an interrupt request line, read/write line, and enable line. These signals permit the MPU to have complete control over the KS5824.

UART Bidirectional Data (D0-D7) — The bidirectional data lines (D0-D7) allow for data transfer between the KS5824 and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an UART read operation.

UART Enable (E) — The Enable signal, E, is a high-impedance TTL-compatible input that enables the bus input/output data buffers and clocks data to and from the KS5824.

Read/Write (R/$\overline{W}$) — The Read/Write line is a high-impedance input that is TTL compatible and is used to control the direction of data flow through the UART's input/output data bus interface. When Read/Write is high (MPU Read cycle), KS5824 output drivers are turned on and a selected register is read. When it is low, the KS5824 output drivers are turned off and the MPU writes into a selected register. Therefore, the Read/Write signal is used to select read-only or write-only registers within the KS5824.

Chip Select (CS0, CS1, $\overline{CS2}$) — These three high-impedance TTL-compatible input lines are used to address the KS5824. The KS5824 is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. Transfers of data to and from the KS5824, are then performed under the control of the Enable Signal, Read/Write, and Register Select.

Register Select (RS) — The Register Select line is a high-impedance input that is TTL compatible. A high level is used to select the Transmit/Receive Data Registers and a low level the Control/Status Registers. The Read/Write signal line is used in conjunction with Register Select to select the read-only or write-only register in each register pair.

Interrupt Request ($\overline{IRQ}$) — Interrupt Request is a TTL-compatible, open-drain (no internal pullup), active low output that is used to interrupt the MPU. The $\overline{IRQ}$ output remains low as long as the cause of the interrupt is present and the appropriate interrupt enable within the UART is set. The $\overline{IRQ}$ status bit, when high, indicates the $\overline{IRQ}$ output is in the active state.

Interrupts result from conditions in both the transmitter and receiver sections of the UART. The transmitter section causes an interrupt when the Transmitter Interrupt Enabled condition is selected (CR5•CR6), and the Transmit Data Register Empty (TDRE) status bit is high. The TDRE status bit indicates the current status of the Transmitter Data Register except when inhibited by Clear-to-Send ($\overline{CTS}$) being high or the UART being maintained in the Reset condition. The interrupt is cleared by writing data into the Transmit Data Register. The interrupt is masked by disabling the Transmitter Interrupt via CR5 or CR6 or by the loss of $\overline{CTS}$ which inhibits the TDRE status bit. The Receiver section causes an interrupt when the Receiver Interrupt Enable is set and the Receive Data Register Full (RDRF) status bit is high, an Overrun has occurred, or Data Carrier Detect ($\overline{DCD}$) has gone high. An interrupt resulting from the RDRF status bit can be cleared by reading data or resetting the UART. Interrupts caused by Overrun or loss of $\overline{DCD}$ are cleared by reading the status register after the error condition has occurred and then reading the Receive Data Register or resetting the UART. The receiver interrupt is masked by resetting the Receiver Interrupt Enable.

CLOCK INPUTS

Separate high-impedance TTL-compatible inputs are provided for clocking of transmitted and received data. Clock frequencies of 1, 16, or 64 times the data rate may be selected.

Transmit Clock (T_X CLK) —The Transmit Clock input is used for the clocking of transmitted data. The transmitter initiates data on the negative transition of the clock.

Receive Clock (R_X CLK) — The Receive Clock input is used for synchronization of received data. (In the ÷1 mode, the clock and data must be synchronized externally.) The receiver samples the data on the positive transition of the clock.

SERIAL INPUT/OUTPUT LINES

Receive Data (R_X Data) — The Receive Data line is a high-impedance TTL-compatible input through which data is received in a serial format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used.

Transmit Data (T_X Data) — The Transmit Data output line transfers serial data to a modem or other peripheral.

PERIPHERAL/MODEM CONTROL

The UART includes several functions that permit limited control of a peripheral or modem. The functions included are Clear-to-Send, Request-to-Send and Data Carrier Detect.

Clear-to-Send ($\overline{CTS}$) — This high-impedance TTL-compatible input provides automatic control of the transmitting end of a communications link via the modem Clear-to-Send active low output by inhibiting the Transmit Data Register Empty (TDRE) status bit.

Request-to-Send ($\overline{RTS}$) — The Request-to-Send output enables the MPU to control a peripheral or modem via the data bus. The $\overline{RTS}$; output corresponds to the state of the Control Register bits CR5 and CR6. When CR6 = 0 or both CR5 and CR6 = 1, the $\overline{RTS}$ output is low (the active state). This output can also be used for Data Terminal Ready (DTR).

Data Carrier Detect ($\overline{DCD}$) — This high-impedance TTL-compatible input provides automatic control, such as in the receiving end of a communications link by means of a modem Data Carrier Detect output. The $\overline{DCD}$ input inhibits and initializes the receiver section of the UART when high. A low-to-high transition of the Data Carrier Detect initiates an interrupt to the MPU to indicate the occurrence of a loss of carrier when the Receive Interrupt Enable bit is set. The Rx CLK must be running for proper $\overline{DCD}$ operation.

UART REGISTERS

The expanded block diagram for the UART indicates the internal registers on the chip that are used for the status, control, receiving, and transmitting of data. The content of each of the registers is summarized in Table 1.

TRANSMIT DATA REGISTER (TDR)

Data is written in the Transmit Data Register during the negative transition of the enable (E) when the UART has been addressed with RS high and R/$\overline{W}$ low. Writing data into the register causes the Transmit Data Register Empty bit in the Status Register to go low. Data can then be transmitted. If the transmitter is idling and no character is being transmitted, then the transfer will take place within 1-bit time of the training edge of the Write command. If a character is being transmitted, the new data character will commence as soon as the previous character is complete. The transfer of data causes the Transmit Data Register Empty (TDRE) bit to indicate empty.

RECEIVE DATA REGISTER (RDR)

Data is automatically transferred to the empty Receive Data Register (RDR) from the receiver deserializer (a shift register) upon receiving a complete character. This event causes the Receive Data Register Full bit (RDRF) in the status buffer to go high (full). Data may then be read through the bus by addressing the UART and selecting the Receive Data Register with RS and R/$\overline{W}$ high when the UART is enabled. The non-destructive read cycle causes the RDRF bit to be cleared to empty although the data is retained in the RDR. The status is maintained by RDRF as to whether or not the data is current. When the Receive Data Register is full, the automatic transfer of data from the Receiver Shift Register to the Data Register is inhibited and the RDR contents remain valid with its current status stored in the Status Register.

DEFINITION OF UART REGISTER CONTENTS

Data Bus Line Number	Buffer Address			
	RS • R/$\overline{W}$ Transmit Data Register (Write Only)	RS • R/$\overline{W}$ Receive Data Register (Read Only)	$\overline{RS}$ • R/$\overline{W}$ Control Register (Write Only)	$\overline{RS}$ • R/$\overline{W}$ Status Register (Read Only)
0	Data Bit 0*	Data Bit 0	Counter Divide Select 1 (CR0)	Receive Data Register Full (RDRF)
1	Data Bit 1	Data Bit 1	Counter Divide Select 2 (CR1)	Transmit Data Register Empty (TDRE)
2	Data Bit 2	Data Bit 2	Word Select 1 (CR2)	Data Carrier Detect ($\overline{DCD}$)
3	Data Bit 3	Data Bit 3	Word Select 2 (CR3)	Clear-to-Send ($\overline{CTS}$)
4	Data Bit 4	Data Bit 4	Word Select 3 (CR4)	Framing Error (FE)
5	Data Bit 5	Data Bit 5	Transmit Control 1 (CR5)	Receiver Overrun (OVRN)
6	Data Bit 6	Data Bit 6	Transmit Control 2 (CR6)	Parity Error (PE)
7	Data Bit 7***	Data Bit 7**	Receive Interrupt Enable (CR7)	Interrupt Request ($\overline{IRQ}$)

* Leading bit = LSB = Bit 0
** Data bit will be zero in 7 bit plus parity modes
*** Data bit is "don't care" in 7 bit plus parity modes.

CONTROL REGISTER

The UART Control Register consists of eight bits of write-only buffer that are selected when RS and R/$\overline{W}$ are low. This register controls the function of the receiver, transmitter, interrupt enables, and the Request-to-Send peripheral/modem control output.

Counter Divide Select Bits (CR0 and CR1) — The Counter Divide Select Bits (CR0 and CR1) determine the divide ratios utilized in both the transmitter and receiver sections of the UART. Additionally, these bits are used to provide a master reset for the UART which clears the Status Register (except for external conditions on $\overline{CTS}$ and $\overline{DCD}$) and initializes both the receiver and transmitter. Master reset does not affect other Control Register bits. Note that after power-on or a power fail/restart, these bits must be set high to reset the UART. After resetting, the clock divide ratio may be selected. These counter select bits provide for the following clock divide ratios:

CR1	CR0	Function
0	0	÷1
0	1	÷16
1	0	÷64
1	1	Master Reset

Word Select Bits (CR2, CR3, and CR4) — The Word Select bits are used to select word length, parity, and the number of stop bits. The encoding format is as follows;

CR4	CR3	CR2	Function
0	0	0	7 Bits + Even Parity + 2 Stop Bits
0	0	1	7 Bits + Odd Parity + 2 Stop Bits
0	1	0	7 Bits + Even Parity + 1 Stop Bit
0	1	1	7 Bits + Odd Parity + 1 Stop Bit
1	0	0	8 Bits + 2 Stop Bits
1	0	1	8 Bits + 1 Stop Bit
1	1	0	8 Bits + Even Parity + 1 Stop Bit
1	1	1	8 Bits + Odd Parity + 1 Stop Bit

Word length, Parity Select, and Stop Bit changes are not buffered and therefore become effective immediately.

Transmitter Control Bits (CR5 and CR6) — Two Transmitter Control bits provide for the control of the interrupt from the Transmit Data Register Empty condition, the Request-to-Send ($\overline{RTS}$) output, and the transmission of a Break level (space). The following encoding format is used:

CR6	CR5	Function
0	0	$\overline{RTS}$ = low, Transmitting Interrupt Disabled.
0	1	$\overline{RTS}$ = low, Transmitting Interrupt Enabled.
1	0	$\overline{RTS}$ = high, Transmitting Interrupt Disabled.
1	1	RTSi: low. Transmits a Break level on the Transmit Data Output. Transmitting Interrupt Disabled.

Receive Interrupt Enable Bit (CR7) — The following interrupts will be enabled by a high level in bit position 7 of the Control Register (CR7): Receive Data Register Full Overrun or a low-to-high transition on the Data Carrier Detect ($\overline{DCD}$) signal line.

STATUS REGISTER

Information on the status of the UART is available to the MPU by reading the UART Status Register. This read-only register is selected when RS is low and R/$\overline{W}$ is high. Information stored in this register indicates the status of the Transmit Data Register, the Receive Data Register and error logic, and the peripheral/modem status inputs of the UART.

Receive Data Register Full (RDRF), Bit 0 — Receive Data Register Full indicates that received data has been transferred to the Receive Data Register. RDRF is cleared after an MPU read of the Receive Data Register or by a master reset. The cleared or empty state indicates that the contents of the Receive Data Register are not current. Data Carrier Detect being high also causes RDRF to indicate empty.

Transmit Data Register Empty (TDRE), Bit 1 — The Transmit Data Register Empty bit being set high indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The low state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

Data Carrier Detect ($\overline{DCD}$), Bit 2 — The Data Carrier Detect bit will be high when the $\overline{DCD}$ input from a modem has gone high to indicate that a carrier is not present. This bit going high causes and Interrupt Request to be generated when the Reoeive Interrupt Enable is set. It remains high after the $\overline{DCD}$ input is returned low until cleared by first reading the Status Register and then the Data Register or until a master reset occurs. If the $\overline{DCD}$ input remains high after read

status and read data or master reset has occurred, the interrupt is cleared, the $\overline{DCD}$ status bit remains high and will follow the $\overline{DCD}$ input.

Clear-to-Send ($\overline{CTS}$), Bit 3 — The Clear-to-Send bit indicates the state of the Clear-to-Send input from a modem. A low $\overline{CTS}$ indicates that there is a Clear-to-Send from the modem. In the high state, the Transmit Data Register Empty bit is inhibited and the Clear-to-Send status bit will be high. Master reset does not affect the Clear-to-Send status bit.

Framing Error (FE), Bit 4 — Framing error indicates that the received character is improperly framed by a start and a stop bit and is detected by the absence of the first stop bit. This error indicates a synchronization error, faulty transmission, or a break condition. The framing error flag is set or reset during the receive data transfer time. Therefore, this error indicator is present throughout the time that the associated character is available.

Receiver Overrun (OVRN), Bit 5 — Overrun is an error flag the indicates that one or more characters in the data stream were lost. That is, a character or a number of characters were received but not read from the Receive Data Register (RDR) prior to subsequent characters being received. The overrun condition begins at the midpoint of the last bit of the second character received in succession without a read of the RDR having occurred. The Overrun does not occur in the Status Register until the valid character prior to Overrun has been read. The RDRF bit remains set until the Overrun is reset. Character synchronization is maintained during the Overrun condition. The Overrun indication is reset after the reading of data from the Receive Data Register or by a Master Reset.

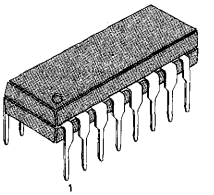
Parity Error (PE), Bit 6 — The parity error flag indicates that the number of highs (ones) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication will be present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver parity check results are inhibited.

Interrupt Request ($\overline{IRQ}$), Bit 7 — The $\overline{IRQ}$ bit indicates the state of the $\overline{IRQ}$ output. Any interrupt condition with its applicable enable will be indicated in this status bit. Anytime the $\overline{IRQ}$ output is low the $\overline{IRQ}$ bit will be high to indicate the interrupt or service request status. $\overline{IRQ}$ is cleared by a read operation to the Receive Data Register or a write operation to the Transmit Data Register.

8-BIT ADDRESSABLE LATCHED DRIVER

The KT8518 is an 8-Bit addressable latched driver with three address inputs (A0, A1, A2), a data input (D), an active low enable input (EN), an active low clear input (CLR) and eight high current parallel latch outputs (Q0 ~ Q7) which sink current to ground.
When the enable (EN) is high and the clear (CLR) is low all outputs (Q0 ~ Q7) are high (OFF). Eight-channel demultiplexing or active low 1-of-8 decoding with output enable operation occurs when the clear (CLR) and the enable (EN) inputs are low.
When the clear (CLR) input is high and the enable (EN) input is low the selected output (Q0 ~ Q7), determined by the address inputs (A0, A1, A2), follows the data (D) input (D = 0 turns "OFF" and D = 1 turns "ON" the addressed high current output).
When the enable (EN) input goes high, the contents of the latch are stored.

16 DIP



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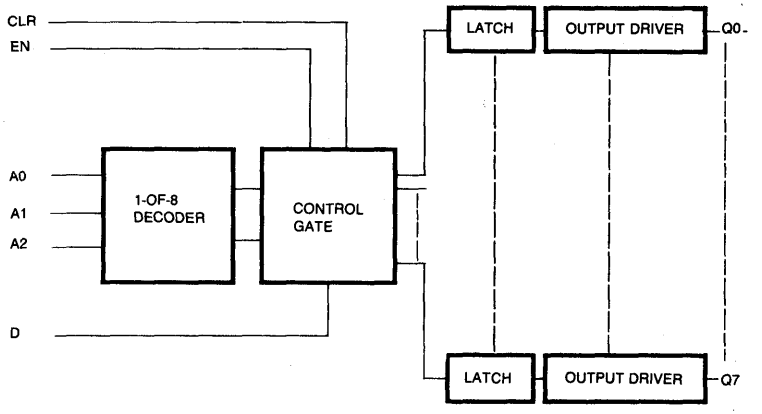
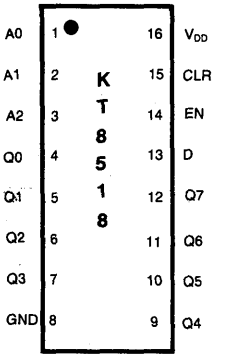
ORDERING INFORMATION

Device	Package	Operating Temperature
KT8518N	16DIP	0° ~ 70°C

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin	Symbol	Description
1, 2, 3	A0, A1, A2	address inputs
4, 5, 6, 7, 9, 10, 11, 12*	Q0 - Q7	high current parallel latch output
13	D	data input
14	EN	enable (active low)
15	CLR	clear input (active low)
8	GND	Power
16	VDD	

MODE SELECTION

EN	CLR	Mode
L	H	Addressable Latch
H	H	Latch
L	L	1-of-8 Decoding
H	L	All Outputs OFF

TRUTH TABLE

INPUTS						OUTPUTS								MODE
CLR	EN	D	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	
L	H	X	X	X	X	H	H	H	H	H	H	H	H	ALL OUTPUT OFF
L	L	L	L	L	L	H	H	H	H	H	H	H	H	
L	L	H	L	L	L	L	H	H	H	H	H	H	H	
L	L	L	H	L	L	H	H	H	H	H	H	H	H	
L	L	H	H	L	L	H	L	H	H	H	H	H	H	1-OF-8 DECODING
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L	L	L	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	L	
H	H	X	X	X	X	Qn-1	-	-	-	-	-	-	-	LATCH
H	L	L	L	L	L	H	Qn-1	-	-	-	-	-	-	
H	L	H	L	L	L	L	Qn-1	-	-	-	-	-	-	
H	L	L	H	L	L	Qn-1	H	Qn-1	-	-	-	-	-	ADDRESSABLE LATCH
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H	H	X	X	X	X	Qn-1	-	-	-	-	-	-	H	
H	H	X	X	X	X	Qn-1	-	-	-	-	-	-	L	

ABSOLUTE MAXIMUM RATING

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.5 ~ 7.0	V
Input Voltage Range	V_{IN}	−0.5 ~ 7.0	V
Output Voltage	V_{OUT}	0 ~ 7.0	V
Continuous Output Current (Each Driver)	I_{OUT}	100	mA
Operating Temperature Range	Ta	0 ~ 70	°C
Storage Temperature Range	Tstg	−25 ~ 150	°C

ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = 0°C ~ 70°C)

Characteristic		Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage		V_{IH}		2.0			V
		V_{IL}				0.8	
Input Damp Diode Voltage		V_{IK}	V_{CC} = min I_{IN} = −18mA		−0.65	−1.5	V
Input Current		I_{IH}	$V_{IN} = V_{DD}$			1	μA
		I_{IL}	V_{IN} = GND			−1	
Output Voltage 1		V_{OL1}	I_{OL} = 80mA Each Driver			0.5	V
Output Voltage 2		V_{OL2}	I_{OL} = 40mA All Outputs Low			0.4	V
Supply Current	All Outputs Low	I_{DDL}	No Output Load			10	μA
	All Outputs High	I_{DDH}				10	
Clamp Diode Leakage Current		I_r				100	μA
Clamp Diode Forward Voltage		V_f				1.5	V

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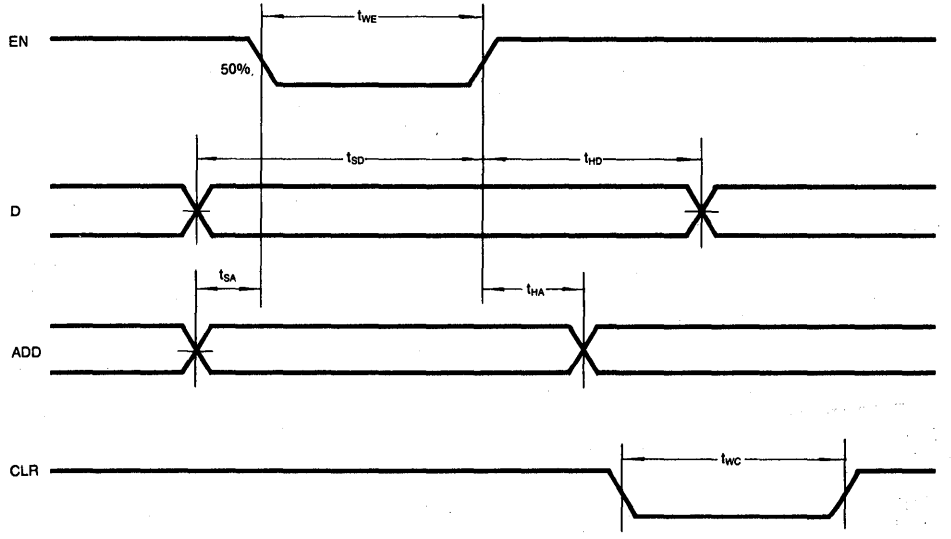
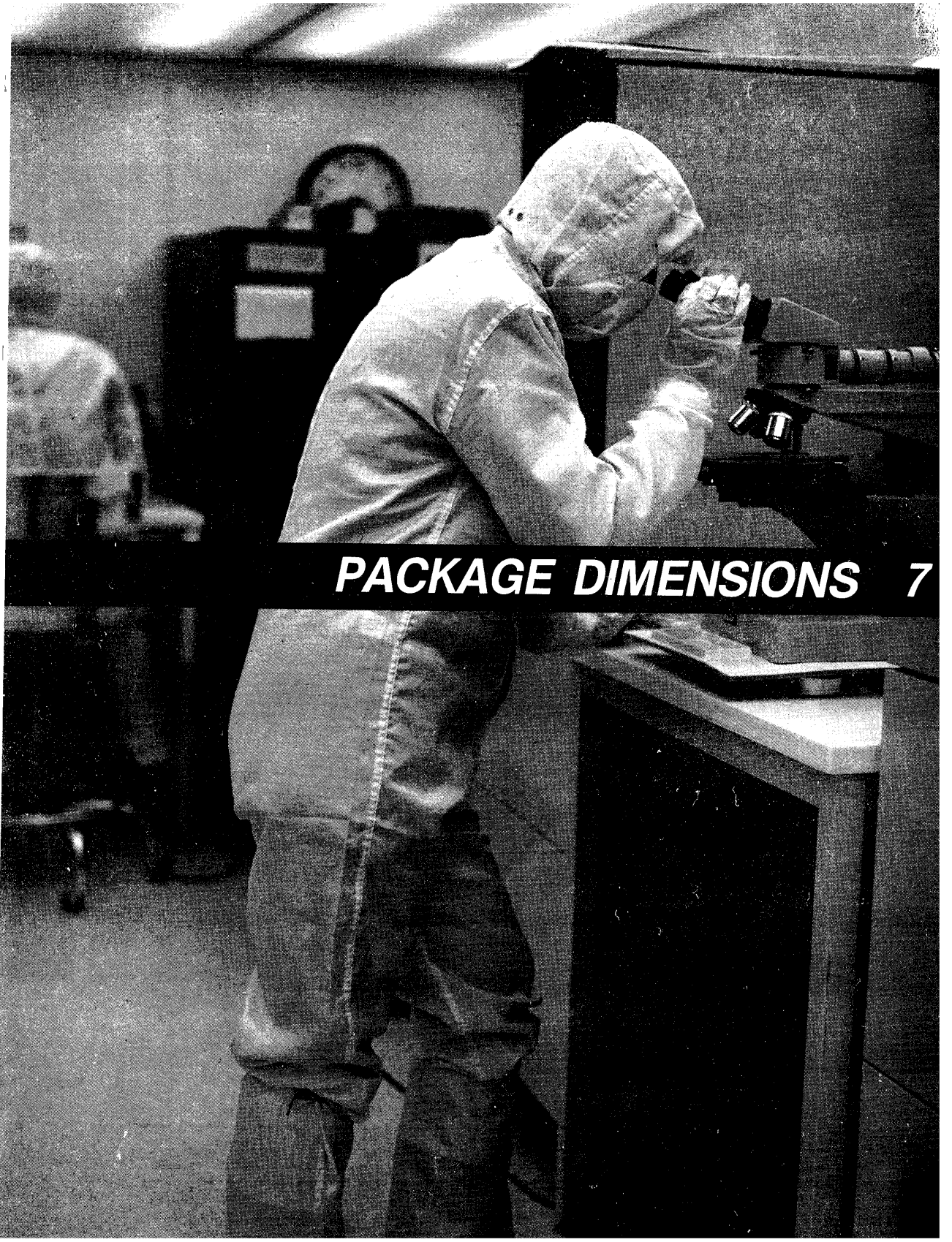
AC ELECTRICAL CHARACTERISTICS (V_{DD} = 5V, Ta = 25°C, C_L = 45pF, R_L = 330Ω)

Characteristic		Symbol	Min	Typ	Max	Unit
PROPAGATION DELAY TIME						nS
	Any Input to Output	t_{PLH}		45	90	
		t_{PHL}		25	50	
	EN Pulse Width	t_{WE}	15			
	CLR Pulse Width	t_{WC}	15			
	Set Up Time (D to EN)	t_{SD}	10			
	Hold Time (D to EN)	t_{HD}	0			
	Set Up Time (ADD to EN)	t_{SA}	10			
	Hold Time (ADD to EN)	t_{HA}	0			

TIMING DIAGRAM

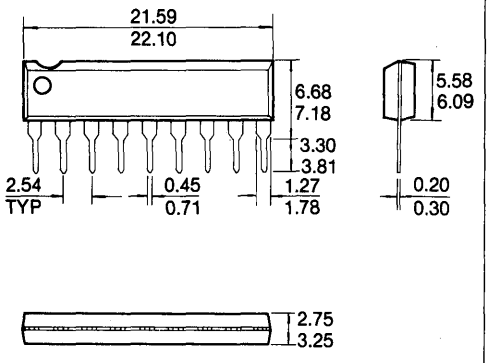




PACKAGE DIMENSIONS 7

9 SIP

Unit: mm



8 DIP

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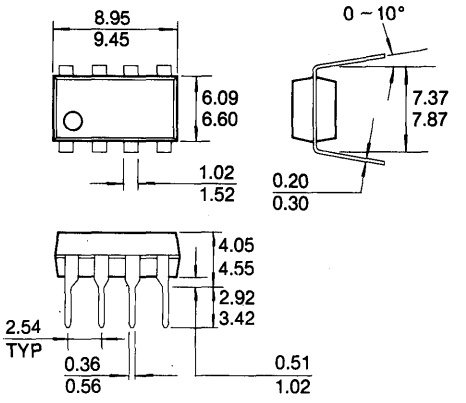
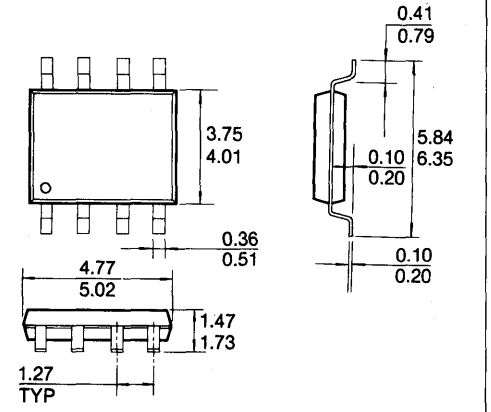


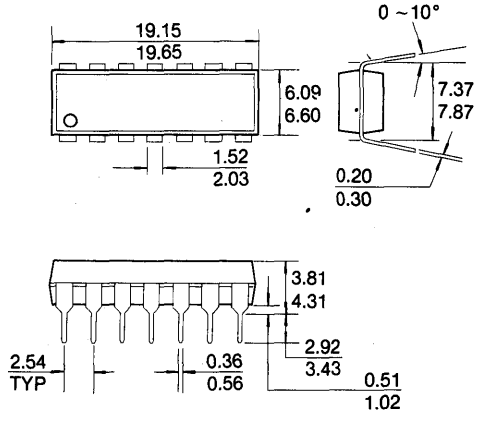
8 SOP

Unit: mm



14 DIP

Unit: mm



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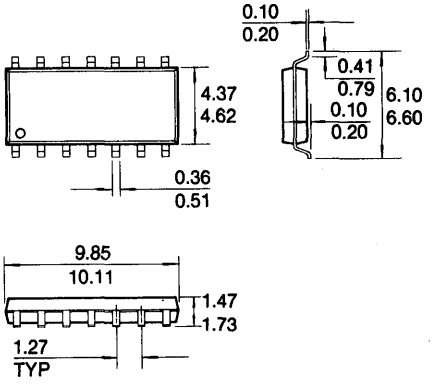
PACKAGE DIMENSIONS

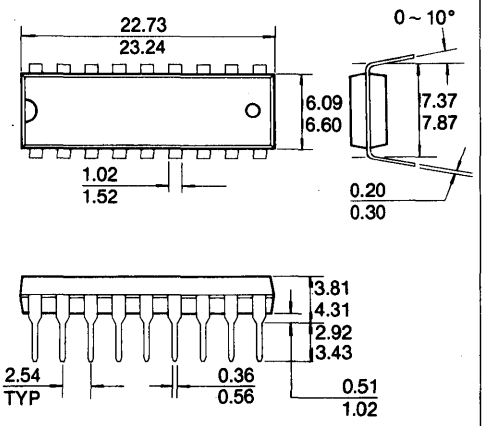
14 SOP

Unit: mm



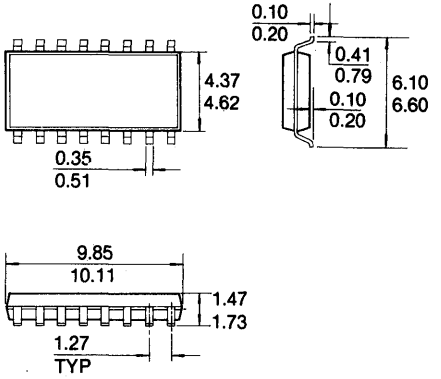
18 DIP

Unit: mm



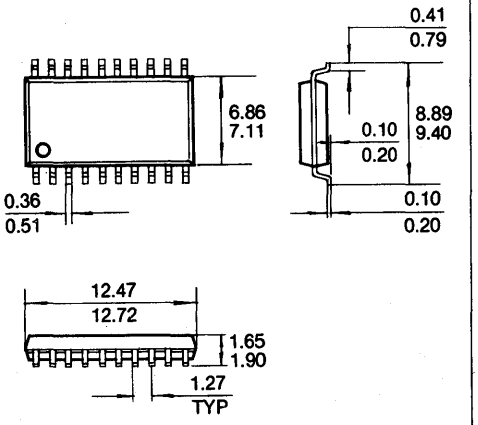
16 SOP

Unit: mm



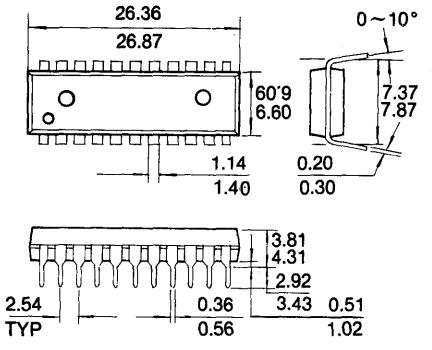
20 SOP

Unit: mm



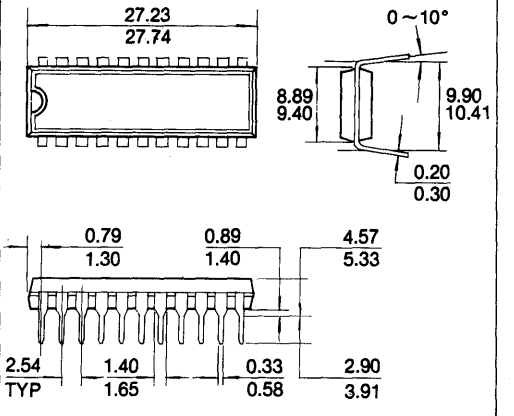
22 DIP (300)

Unit: mm



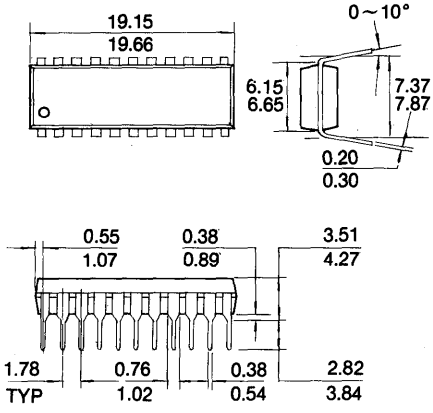
22 DIP (400)

Unit: mm



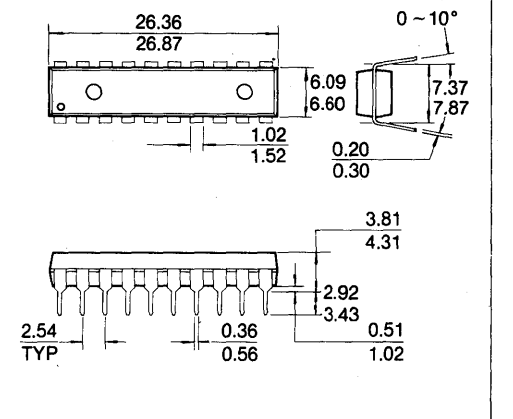
22 DIP (Shrink)

Unit: mm



20 DIP

Unit: mm



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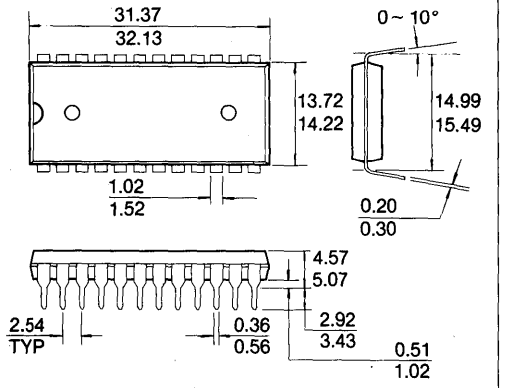
PACKAGE DIMENSIONS

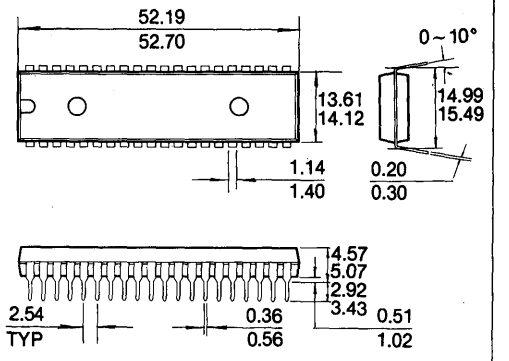
24 DIP

Unit: mm



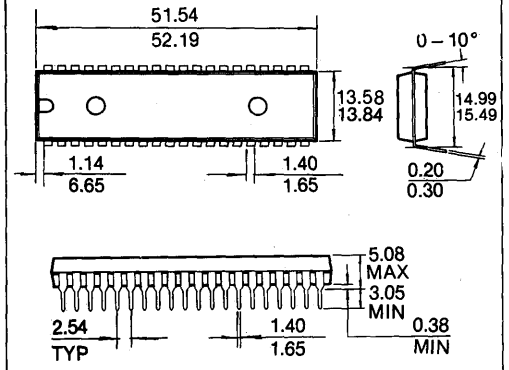
40 DIP-N (1)

Unit: mm



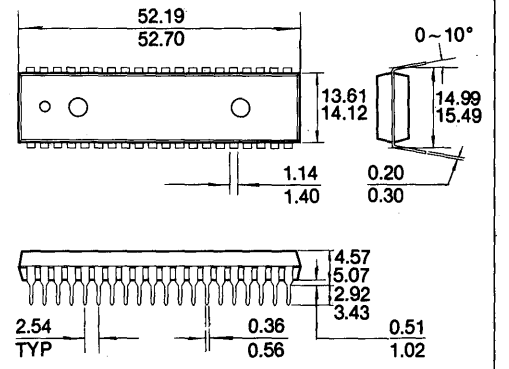
40DIP-N(2)

Unit: mm



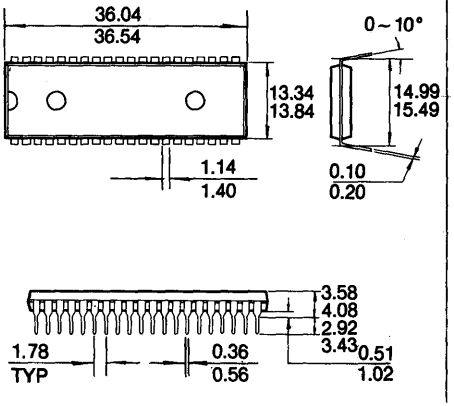
40 DIP-N (3)

Unit: mm



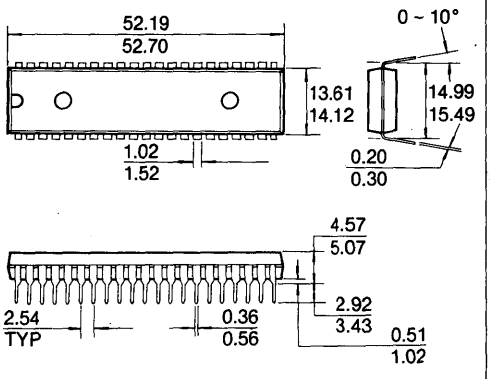
40 SDIP

Unit: mm



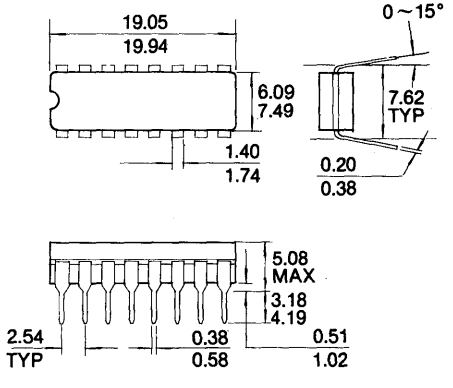
42 DIP

Unit: mm



16 CERDIP

Unit: mm



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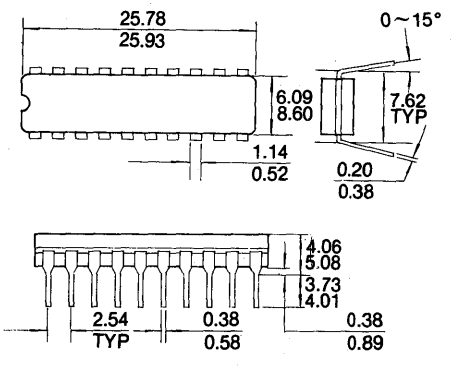
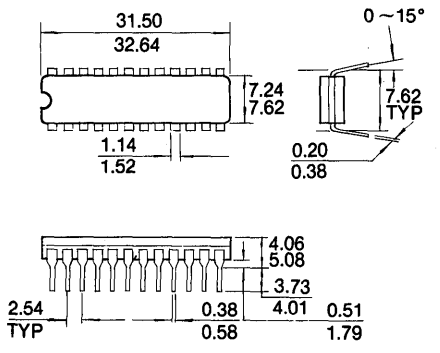
Unit: mm



7

PACKAGE DIMENSIONS

24 CERDIP **Unit: mm**



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