DATABOOK

MOS MEMORY PRODUCTS
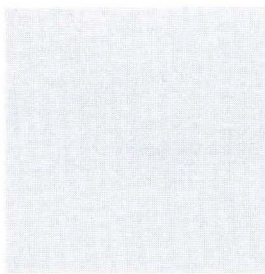
2nd EDITION

SGS Technology and Service
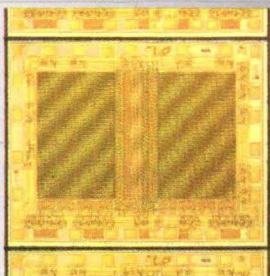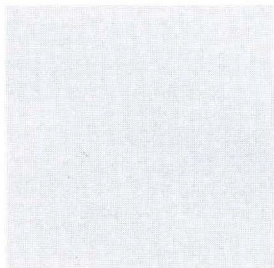
MOS MEMORY
PRODUCTS

2nd EDITION
FEBRUARY 1986
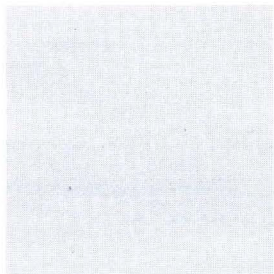
The M2716-16K EPROM
memory designed and
produced by SGS.

The 256K EPROM designed and
produced by SGS.

Highly automated wafer
processing increases yields
and throughput to give SGS
high production capability.

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TABLE OF CONTENTS

IDENTITY

Late in 1957, SGS was founded around a team of researchers who were already carrying out pioneer work in the field of semiconductors. From that small nucleus, the company has evolved into a Group of Companies, operating on a worldwide basis as a broad range semiconductor producer, with billings well over a quarter billion dollars and employing over 10000 people.

The SGS Group of Companies has now reached a total of 12 subsidiaries, located in Brazil, France, Germany, Italy, Malta, Malaysia, Singapore, Spain, Sweden, Switzerland, United Kingdom and the USA.

To go with its logo, the company takes the motto "Technology and Service", underlining the accent given to the development of state-of-the-art technologies and the corporate commitment to offer customers the best quality and service in the industry.

SGS LOCATIONS - EUROPE
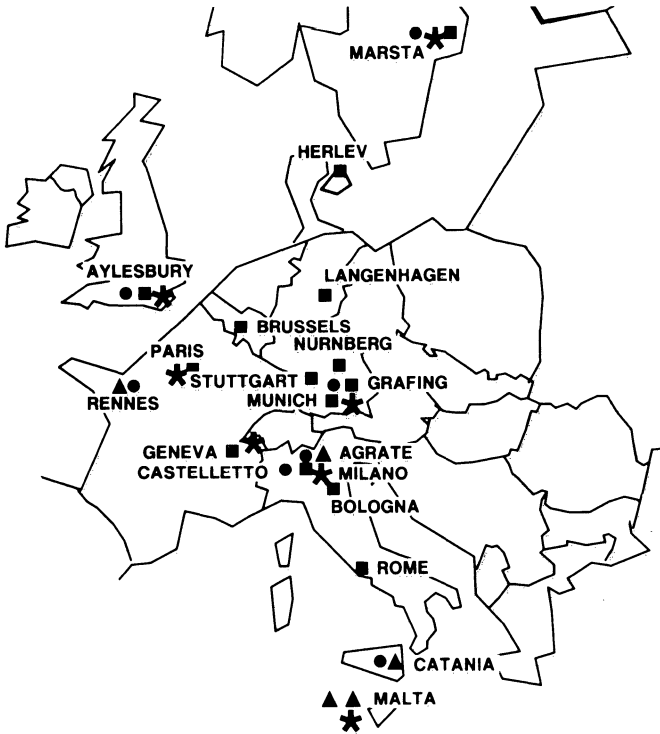
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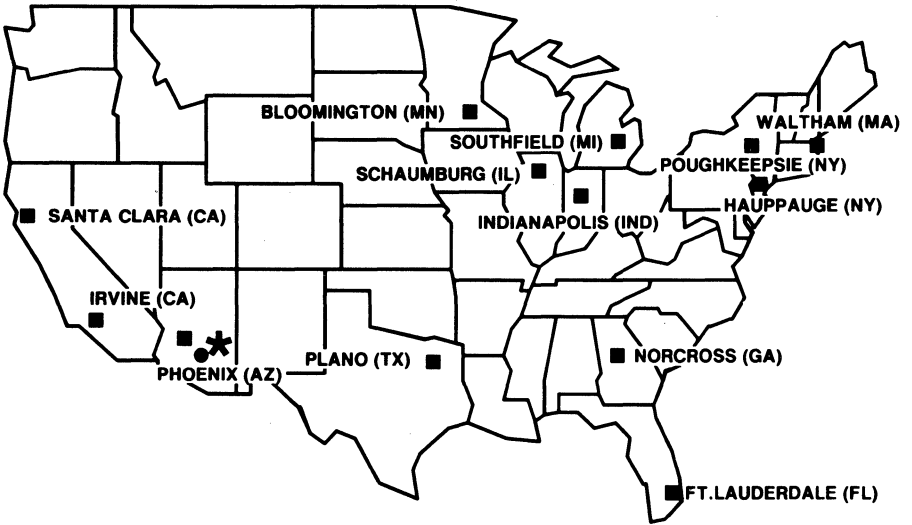
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ALPHANUMERICAL INDEX

PRODUCT GUIDE

SALES TYPE IDENTIFICATION

example: | M | 27128A | 20 | F | 1

Memory Prefix _____

Identification Number _____

Speed Range _____

		EPROMs		ROMs	
V_{CC} 5V ± 5%	V_{CC} 5V ± 10%	M2716 M2716P (ns)	M2732A-M2764 M2764A-27128A M27256-M27512 (ns)	M2316H (ns)	M2332-M2333 M2364-M2365 M23256-M23256A (ns)
Notyng	25	450	250	300	250
1		350			
2	20		200		
3	30		300		
4	45		450		

Package _____
B   Plastic
D   Ceramic Multi Layer
F   Ceramic Frit-Seal
M   SO-8 Plastic

Temperature Range _____
1   0 to + 70°C
6   −40 to + 85°C
2   −55 to +125°C

PROCESSES DESCRIPTION

ERASABLE PROGRAMMABLE READ ONLY MEMORY

Capacity	Device	Organization	Process	Access Time (Max.)	Page
16K	M2716	2K × 8 bit	NMOS E	350/450 ns	37
32K	M2732A	4K × 8 bit	NMOS E1	200/250/300/450 ns	45
64K	M2764	8K × 8 bit	NMOS E2	200/250/300/450 ns	53
64K	M2764A	8K × 8 bit	NMOS E3	200/250/300/450 ns	61
128K	M27128A	16K × 8 bit	NMOS E3	200/250/300/450 ns	71
256K	M27256	32K × 8 bit	NMOS E3	200/250/300/450 ns	81
512K	M27512	64K × 8 bit	NMOS E3	250/300 ns	91

MASK READ ONLY MEMORY

Capacity	Device	Organization	Process	Access Time (Max.)	Page
16K	M2316H	2K × 8 bit	NMOS H1	300 ns	111
32K	M2332	4K × 8 bit	NMOS H1	250 ns	115
32K	M2333	4K × 8 bit	NMOS H1	250 ns	115
64K	M2364	8K × 8 bit	NMOS H2	250 ns	119
64K	M2365	8K × 8 bit	NMOS H2	250 ns	123
256K	M23256	32K × 8 bit	NMOS H2	250 ns	127
256K	M23256A	32K × 8 bit	NMOS H2	250 ns	127

ELECTRICALLY ERASABLE PROGRAMMBLE READ ONLY MEMORY

Capacity	Device	Organization	Process	Max. Clock Frequency	Page
1K	M8571	see data sheet	NMOS F1	125 KHz	133
256	M9306	16 × 16 bit	NMOS F1	250 KHz	143
1024	M9346	64 × 16 bit	NMOS F1	250 KHz	147

| PROCESS	CHARACTERISTICS	PRODUCTS
NMOS E	PH DOPING CHANNEL LENGTH 4 μm GATE OXIDE THICKNESS 1100Å VCC = 5V VPP = 25V	EPROM (M2716) (M2716P)
NMOS E1	AS DOPING CHANNEL LENGTH 3 μm GATE OXIDE THICKNESS 700Å VCC = 5V VPP = 21V	EPROM (M2732A) (M2732AP)
NMOS E2	AS DOPING CHANNEL LENGTH 2 μm GATE OXIDE THICKNESS 700Å VCC = 5V VPP = 21V	EPROM (M2764) (M2764P)
NMOS E3	AS DOPING CHANNEL LENGTH 1.5 μm GATE OXIDE THICKNESS 350Å VCC = 5V VPP = 12.5V	EPROM (M2764A) (M2764AP) (M27128A) (M27256)
NMOS F1	AS DOPING CHANNEL LENGTH 3.5 μm GATE OXIDE THICKNESS 800Å VCC = 5V	EEPROM (M8571) (M9306) (M9346)
NMOS H1	AS DOPING CHANNEL LENGTH 3/4 μm GATE OXIDE THICKNESS 500Å VCC = 5V	ROM
NMOS H2	AS DOPING CHANNEL LENGTH 2.5 μm GATE OXIDE THICKNESS 350Å VCC = 5V	ROM

TECHNICAL INFORMATION

HOW DOES AN EPROM WORK

The EPROM cell transistor is just like a standard MOS transistor with the exception that a floating gate is added as shown in figure 1. The vertical stacking allows the functions of storage and reading, which normally require separate devices, to be within the space a single field effect transistor occupies. The EPROM cell is programmed by charging the floating gate with the injection of "hot electrons" from the drain's pinch off region. Erasing is obtained by internal photoemission from the floating gate to the top gate and substrate. The ultraviolet light give to the electrons enough energy to pass the energy barrier between the floating gate and the oxide surrounding it.

When the EPROM cell is programmed, the negative charge on the floating gate causes the floating gate to source voltage to be negative. This turns the cell off, even with a positive reading voltage applied to the select gate. Since the floating gate is not tied to a power supply, its voltage is determined by its charge and by capacitive coupling to the voltages of the select gate, the drain, the channel, and the source. The difference between the floating gate voltage and the voltages of these other areas can be used to determine the electric fields in the various oxide regions of the device. Although the voltage applied to the chip during programming is high 25; 21 or 12.5V) the fields across the gate oxide directly above the channel are relatively small, about 1.5MV/cm. During all other operations, even when the floating gate is fully charged, this field is less than 0.7MV/cm.
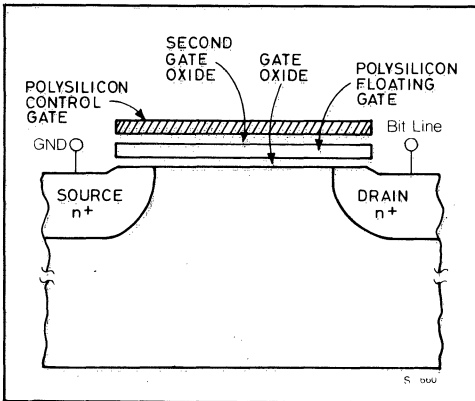
During programming (see fig. 2) the hot electrons get their energy from the voltage applied to the drain of the EPROM cell. They are accelerated along the channel into the even higher fields surrounding the drain depletion region. While traversing the channel, the electrons enter a region where the electric field in the substrate is about 10^5V/cm or greater. At this point the rate of energy gained from the electric field can no longer be described by the temperature of the silicon; hence the term "hot". Once these electrons gain sufficient energy they can surmount the energy barrier of about 3.2 eV between the silicon substrate and the silicon dioxide insulator.

Because energy loss due to phonon emission increase at higher lattice temperature, it is actually easier to obtain hot electrons at lower operating temperatures. In addition to phonon emission, hot electrons with energies above about 1.8 eV may give up some of this energy in another way: through electron hole pair creation resulting from impact ionization. This phenomenon is observed in ordinary MOS transistors as the cause of the onset of the substrate current at high drain voltages. However, in the case of the EPROM, significant current multiplication produces substantial substrate current even before a large enough drain voltage is reached to produce hot electron injection into the oxide.

With positive drain and channel voltages, electrons injected into the oxide of an n-channel EPROM return to the substrate unless a high positive select gate voltage is applied to pull the electrons toward the floating gate. Not only does the floating gate have to be positively biased with respect to the source, it must also be positive with respect to the point along the channel where hot electron injection occurs.

Fig. 1

Fig. 2
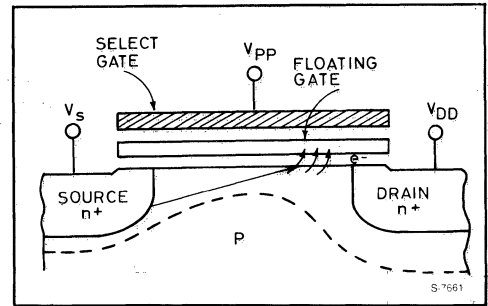
Near the beginning of the injection process the inversion layer extends almost all the way to the drain, and the field in the oxide is attractive except for a small portion very near the drain. Current begins to flow through the oxide at the point where the electrons are their hottest and where the oxide field is most favorable. As the floating gate charges up, the floating gate to source voltage drops and the drain's pinch off region moves towards the source. The surface field near the drain intensifies and more hot electrons are produced in the substrate. However in the region where the electron are their hottest, the oxide field is least favorable for injection and so the injected electron injection process is self limiting. The charging of the floating gate reduces the number of electrons that can be accelerated in the high field region. As the floating gate becomes fully charged, to oxide current is reduced almost to zero because the oxide field is now repulsive to the electrons injected into the high field is now repulsive to the electrons injected into the high field region.

Since the reducing electric field between the floating gate and the channel is responsible for shutting off the oxide current, the saturated threshold voltage shift off the floating gate tracks the selected gate voltage during programming on a volt per volt basis. The floating gate charges to the same value relative as the source and channel. An increase in the selected gate voltage during programming merely increases the charge of the floating gate necessary to abort the injection of hot electrons. The drain voltage boes not in general have a major effect on the final programmed voltage of the floating gate. However it does effect the speed at which the device is programmed, since injection exhibits an exponential dependence on the electric field in the channel.

EPROMs needs to be completely erased before they are reprogrammed. Erasure is accomplished by exposing the devices to UV light. Typical erasure sources are quartz jacketed mercury arc lamps and mercury vapor lamps, which emit strong radiation at a wavelength of 2537 Å. The photons emitted by the lamps are absorbed by electrons in the conduction and valence bands of the floating gate; at this wavelength, most of them are absorbed within 50 Å of the oxide interface (see fig. 3).
The excited electrons leave the floating gate, enter the oxide, and are swept away to the select gate or substrate by local field. During erasure, the select gate, source, drain, and substrate are all near ground potential. With an N-type floating gate, electrons can be excited from either the conduction band or the valence band into the oxide. Ultraviolet rays are so strongly absorbed that they don't get past the top select gate and the photons

can only make their way to the floating gate from the side. In self aligned structure, the edge of the floating gate is directly exposed to the radiation. But in earlier N-channel structures in which the floating gate is completely covered by the select gate, erasure is accomplished as the photons travel through the field oxide, under the select gate, and to the floating gate where they are absorbed. This wave-guiding effect is efficent beacuse the reflectivity of silicon to 2500 Å light is roughly 65%₀.

During reading, the EPROM cell operates like an ordinary transistor except that the normal gate capacitance is replaced by the series capacitance of the floating gate structure. The most important characteristic of a non volatile memory is how well they retain their data. For EPROMs the answer hinges on how well the charge on the floating gate stays put over the lifetime of the part. The advantage of floating gate memories is that the gates are surrounded by high integrity silicon dioxide. This oxide is a nearly ideal insulator because it has a wide bandgap, a very high barrier with reference to silicon and aluminium, a relatively low surface state density on silicon, low bulk trapping levels, and no structural polarization. For ordinary electric fields from the floating gate to the select gate and substrate encountered during reading and storage, electron emission is negligible.

Fig. 3

15
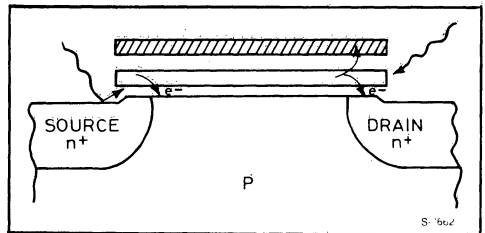
EPROMS TECHNOLOGY EVOLUTION

From the introduction of the M2716, SGS has been developing and evolving EPROM technologies in order to increase storage capacity and quality characteristics.
Starting from 1978 with the M2716, manufactured using the NMOS E0 process, four distinct advances have been made reducing cell area from $340 \mu m^2$ down to the present $36 \mu m^2$ with the NMOS E3 process. The evolution can be clearly seen in figs. 1 to 4.
Figure 1 shows the matrix area of a M2716. Figures 2, 3 and 4 then show respectively the M2732A, M2764 and M27256, respectively manufactured using NMOS E1, E2 and E3 processes. The table shown below gives some characteristics of the four processes.

PROCESS NMOS		E0	E1	E2	E3
CELL AREA	(μm^2)	340	162.5	100	36
GATE OXIDE1 THICKNESS	(Å)	1100	700	700	350
GATE OXIDE2 THICKNESS	(Å)	1200	800	800	400
PROGRAMMING VOLTAGE	(V)	25	21	21	12.5
CELL TRANS. LENGTH	(μm)	4.00	3.00	2.25	1.50

CELL EVOLUTION

CELL EVOLUTION

2716 CELL

M2732A CELL
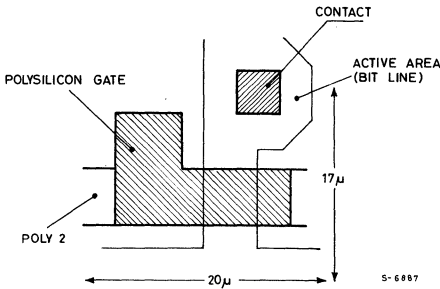
M27256 CELL
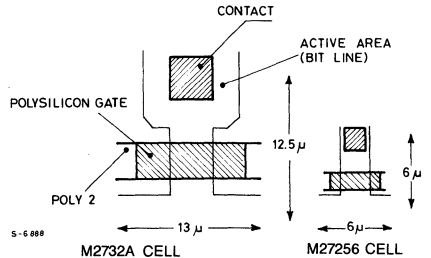
EPROM CELL SYMBOL
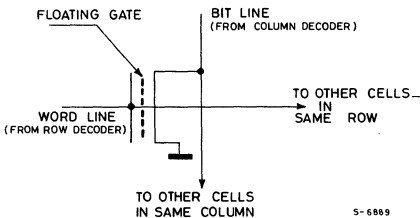
FLOATING GATE IN EPROMs CELLS
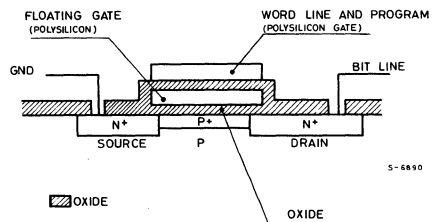
FIG. 1 - M2716 MATRIX AREA 1 cm = 4 μm
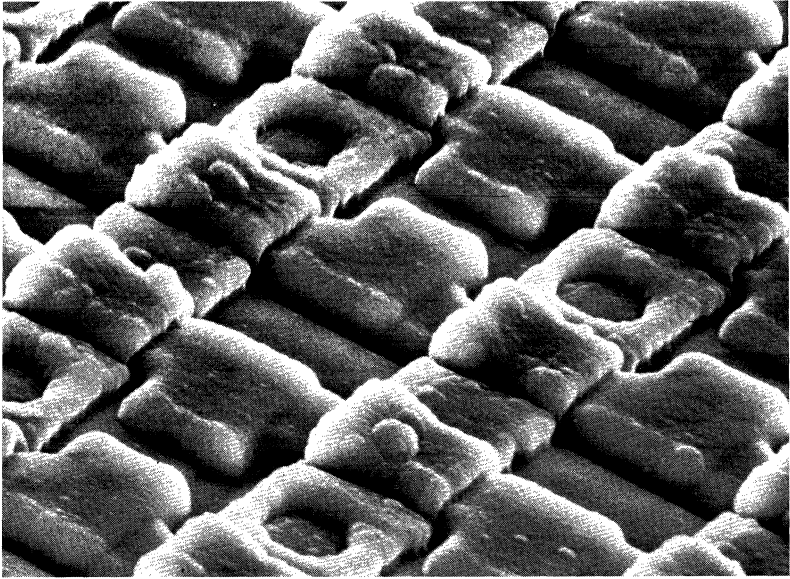
FIG. 2 - M2732A MATRIX AREA 1 cm = 4 μm
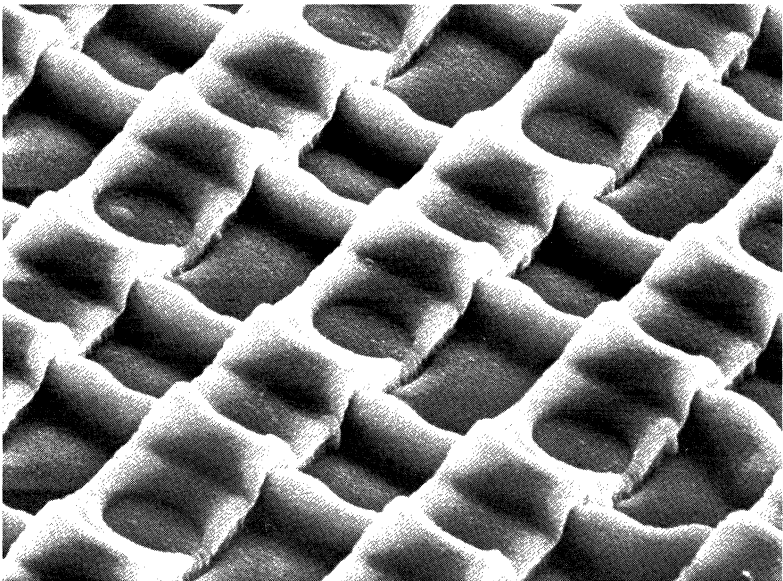
FIG. 3 - M2764 MATRIX AREA 1 cm = 4 μm
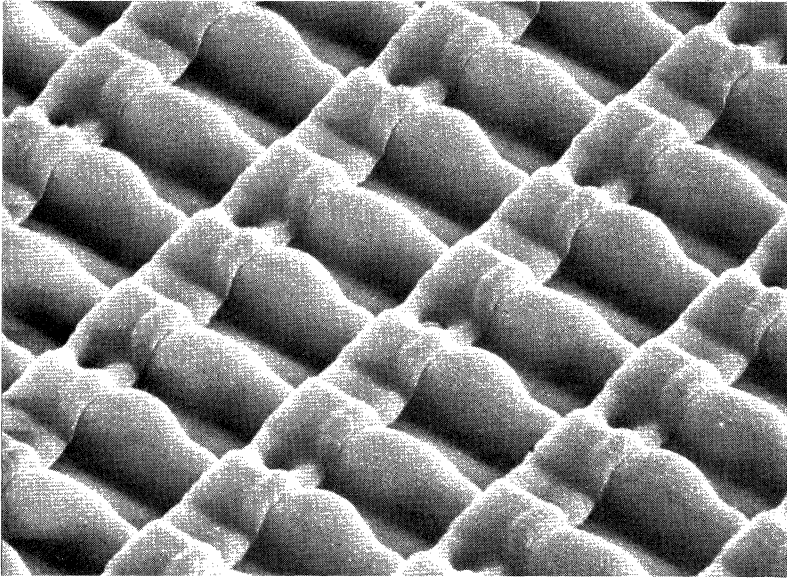
FIG. 4 - M27256 MATRIX AREA 1 cm = 1 μm
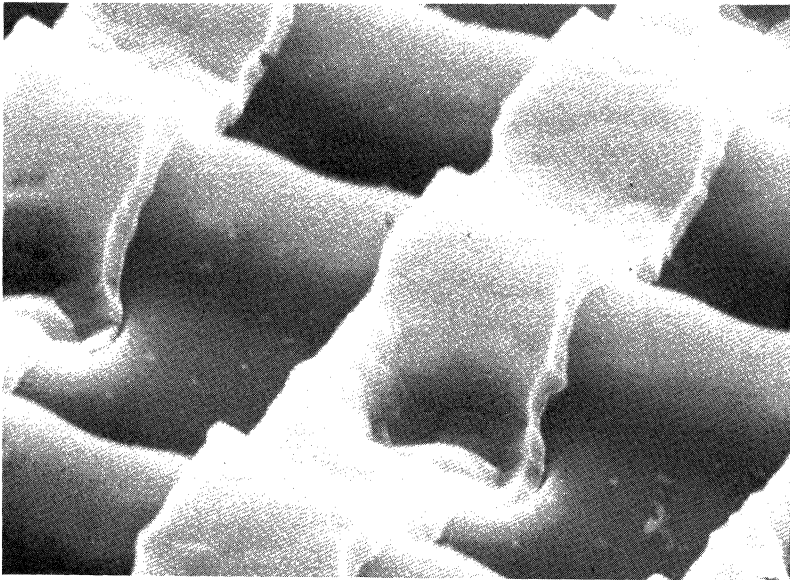
FIG. 5 - NMOS E3 CELL SECTION
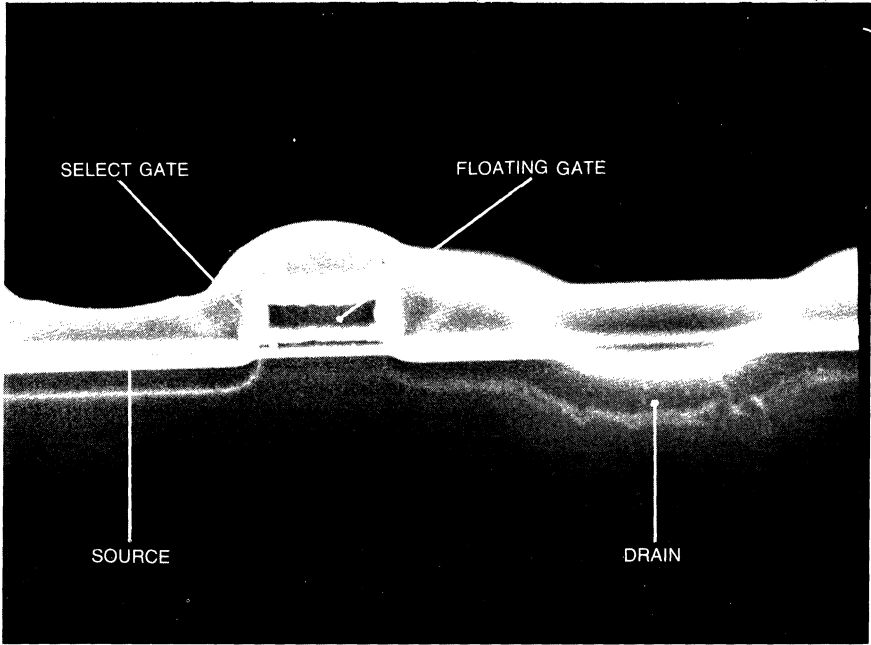
EPROMS PROGRAMMING

This document concerns programming characteristics of the M2764A and M27256, concentrating on those factors which will be new to the EPROM memory designer.

Figure 1 shows the evolution of SGS's EPROM family. The new generation M27256 brings with it improved performance and state-of-the-art reliability.

The lower programming voltage (12.5V) and the replacement of PGM by A14 highlight the additions accompanying the M27256. Advanced technology from the M27256 will soon bring enhanced performance to lower density EPROMs, specifically the M2764A and M27128A.

Fig. 1 - SGS EPROMs EVOLUTION

27256	27128A	2764A	2732A	2716			2716	2732A	2764A	27128A	27256
V_{PP}	V_{PP}	V_{PP}							V_{CC}	V_{CC}	V_{CC}
A12	A12	A12							$\overline{PGM}$	$\overline{PGM}$	A14
A7	A7	A7	A7	A7			V_{CC}	V_{CC}	N.C.	A13	A13
A6	A6	A6	A6	A6			A8	A8	A8	A8	A8
A5	A5	A5	A5	A5			A9	A9	A9	A9	A9
A4	A4	A4	A4	A4			VPP	A11	A11	A11	A11
A3	A3	A3	A3	A3			$\overline{OE}$	$\overline{OE}$/VPP	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A2	A2	A2	A2	A2			A10	A10	A10	A10	A10
A1	A1	A1	A1	A1			$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
A0	A0	A0	A0	A0			O7	O7	O7	O7	O7
O0	O0	O0	O0	O0			O6	O6	O6	O6	O6
O1	O1	O1	O1	O1			O5	O5	O5	O5	O5
O2	O2	O2	O2	O2			O4	O4	O4	O4	O4
GND	GND	GND	GND	GND			O3	O3	O3	O3	O3

THE FAST PROGRAMMING ALGORITHM

The Fast Programming Algorithm was developed as an improved alternative to the 50 msec per byte programming techniques for SGS's M2764 EPROM. By taking advantage of the variable programming times required by the cells in an EPROM array, programming speed increase of 5 or 6 times have been achieved (see table 1). The success of this algorithm, coupled with the long programming times which would be inherent in programming the M27256 with a 50 msec per byte algorithm, has prompted SGS to develop a new M27256 Fast Programming Algorithm specifically tailored to user requirements.

TABLE 1 - EPROM PROGRAMMING-TIME EVOLUTION

DEVICE	BYTES	PROGRAMMING TIME (MIN)
2716	2048	1.75
2732A	4096	3.5
2764	8192	7.0
2764 *	8192	1.25
2764A *	8192	1.25
27128A *	16384	2.5
27256 *	32768	5

* Using Fast Programming Algorithm

The programming speed improvement (Fast Programming Algorithm) is an interactive closed loop technique of margin checking.

It ensure that the programmed bit won't change status once V_{CC} is in the normal operating range. For the M2764 the algorithm begins by setting V_{CC} to 6V (higher than required for normal operation but necessary to provide programming margin), setting the programming voltage V_{PP} to 21V and then iteratively supplying 1-msec LOW-going programming pulses to the EPROM's programm-disable pin PGM. After each pulse, the algorithm checks the EPROM's output for the desired programmed value. If the output is incorrect, the algorithm repeats the pulse-and-check operation; incorrect output after 15 pulses causes rejection of the EPROM device.

If the EPROM is fully functional, however, one of the pulses results in proper EPROM output. At that point, the algorithm supplies still another programming pulse—this one four times longer than the combined length of the previously applied 1-msec pulses. This longer pulse helps ensure that the EPROM cell has adequate programming margin for reliable operation.

Although the pulse can be as long as 60 msec, very few EPROM bytes require this much programming time. In fact, most EPROM bytes program with only one or two 1-msec pulses, so a typical total programming time per byte is 5 to 10 msec.

For reference see fig. 2

FIG. 2 - M2764 FAST PROGRAMMING FLOWCHART
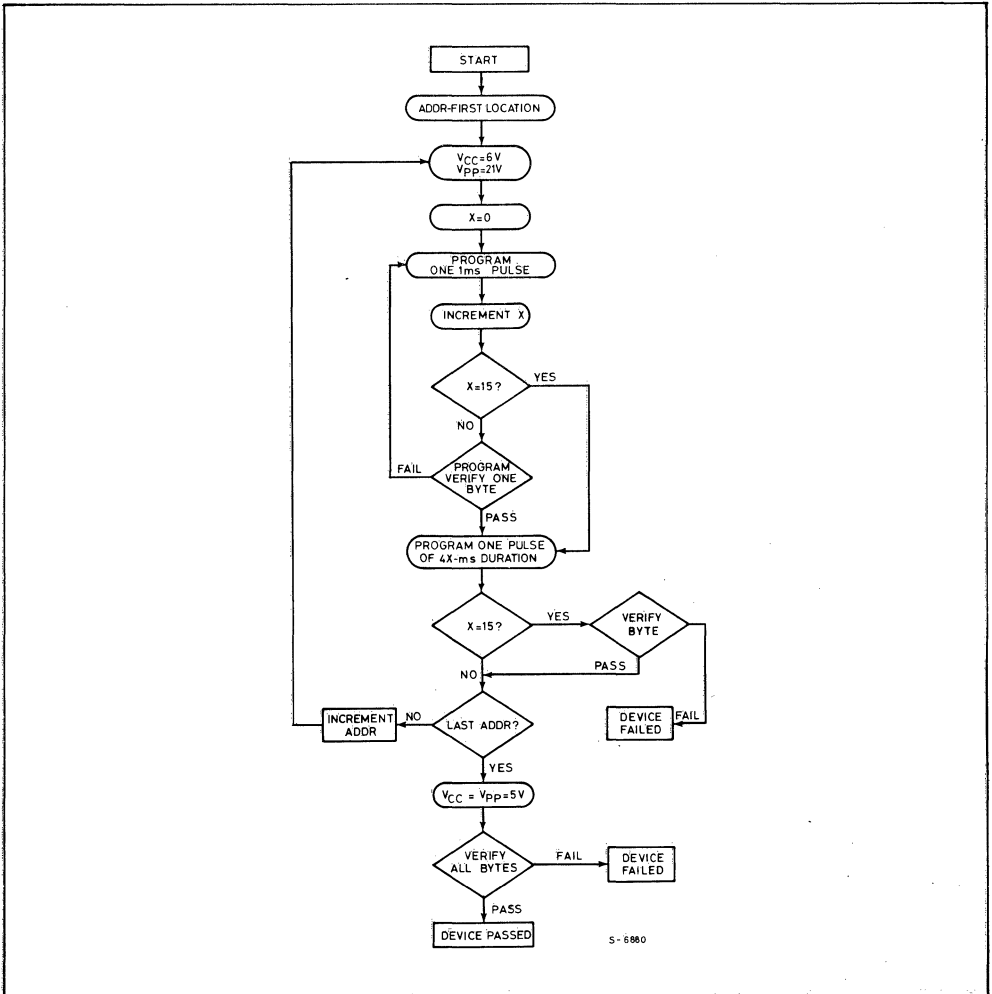
The M27256 programming algorithm is similar to the Fast Programming Algorithms used for SGS's M2764 and M27128 EPROMs. It is now available as a standard feature in many PROM programmers. This new programming algorithm guarantees that each cell has been programmed reliably.

The M27256 Fast Programming Algorithm shown in figure 3 is a feedback control loop. In examining this flowchart three distinct characteristics can be seen. First, the programming voltage has been reduced form 21 ± 0.5 volts, as was required on earlier generation M2764 EPROM, to 12.5 ± 0.5 volts. In all cases the V_{PP} voltage shoud never exceed 14 volts, and a 0.1 μF capacitor shoud be placed between V_{PP} and ground to insure proper decoupling. The technology advances implemented in the M27256 allow the programming voltage to be reduced while taking advantage of the performance of the programmed cell. The second characteristic that should be noted is the maximum number of 1ms pulses which are applied throughout the closed loop programming algorithm. As shown, 25 iterations of the loop is the maximum number allowed. The last characteristic which should be mentioned is the insertion of a byte verify after the iteration count has been maximized. This will save time by failing any device which may not verify correctly after 25 one msec pulses.

This Programming Algorithm shoud be used as well for M2764A and M27128A manufactured with the same NMOS-E3 Process (see page 16)

FIG 3 - M27256 FAST PROGRAMMING FLOWCHART
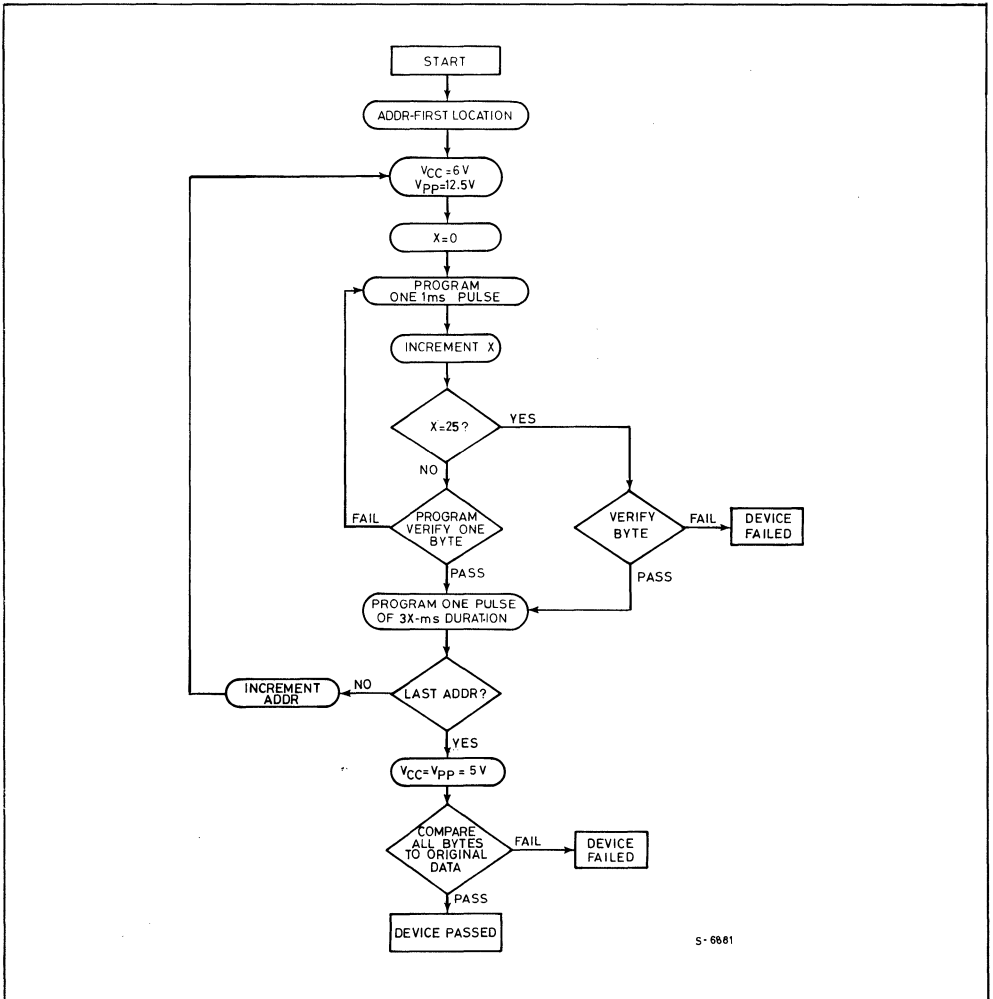
S - 6861

FIG. 4 - M27256 FAST PROGRAMMING WAVEFORMS
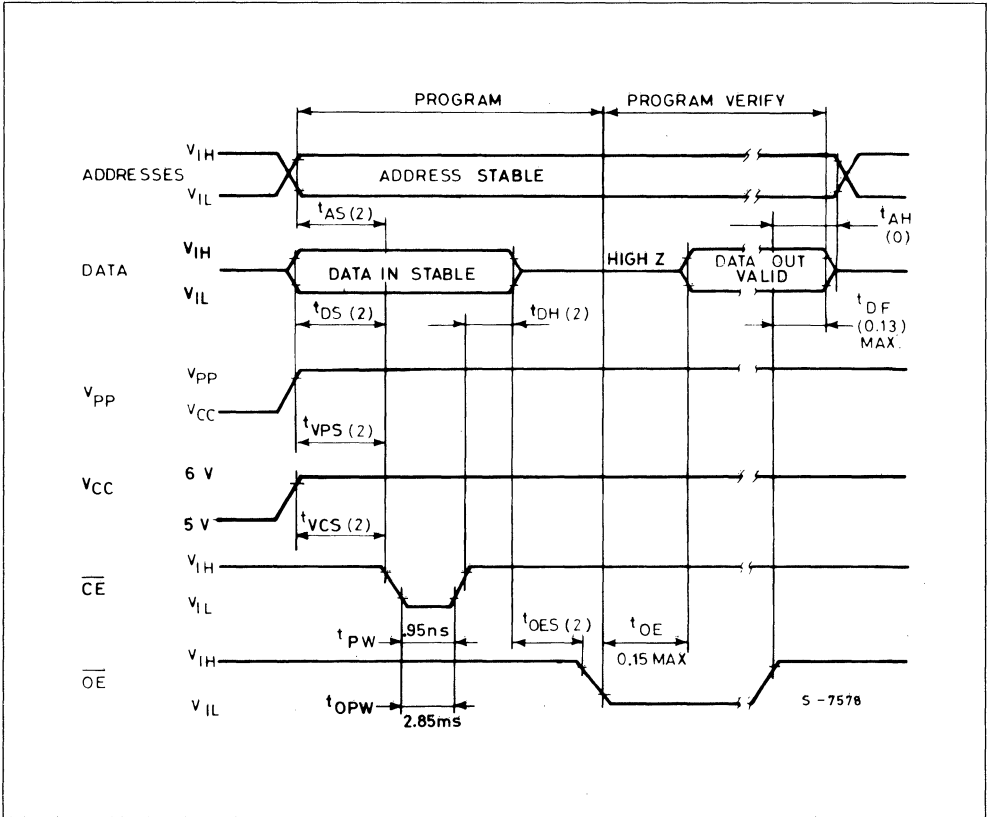
Notes:

1. All times shown in ( ) are minimum and in usec unless otherwise specified.
2. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
3. t_{OE} and t_{DFP} are characteristics of the device but must be accomodated by the programmer.
4. When the programming the M27256 a 0.1μF capacitor is required across V_{PP} and GROUND to suppress spurious voltage transients which can damage the device.

ELECTRONIC SIGNATURE

The Electronic Signature mode allow the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for uses by programming equipment for the purpose of automatically matching the device to be programmed with its correspongind programming algorithm. This mode is functional in the $25°C \pm 5°C$ ambient temperature range that is requiered when programming the EPROM. For M27256 to activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the EPROM. Two identifier bytes may than be sequenced form the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. For the SGS M27256, these two identifier bytes are given below. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (07) defined as the parity bit.

This feature has been implemented also an M2764A, M27128A and M27512.

In Fig. 5 you can see the Electronic Signature Mode for the complete EPROM family.

FIG. 5 - ELECTRONIC SIGNATURE MODE

IDENTIFIER		PINS	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
M2764A	Manufacturer code	V_{IL}	0	0	1	0	0	0	0	0	20
	Device code	V_{IH}	0	0	0	0	1	0	0	0	08
M27128A	Manufacturer code	V_{IL}	0	0	1	0	0	0	0	0	20
	Device code	V_{IH}	1	0	0	0	1	0	0	0	89
M27256	Manufacturer code	V_{IL}	0	0	1	0	0	0	0	0	20
	Device code	V_{IH}	0	0	0	0	0	1	0	0	04
M27512	Manufacturer code	V_{IL}	0	0	1	0	0	0	0	0	20
	Device code	V_{IH}	0	0	0	0	1	1	0	1	0D

Note: For M27512 only $A9 = 12V \pm 0.5V$; A1-A8, A10-A13, $\overline{CE}$, $\overline{OE}/V_{PP} = V_{IL}$; A14, A15 = V_{IH}

EEPROM M9306 PRODUCT DESCRIPTION

New components being used in computer systems are necessary for computer evolution. One of these is the Electrically Erasable Programmable Read Only Memory (EEPROM), that can be elettrically erased and written one byte at a time.
EEPROM is particularly attractive in applications requiring field update of program store memory or non volatile data captime, and has the data retention requirements of eaulier generations of PROMs, but also must maintain its field programmable characteristics over its device life. In this paper we will present the SGS M9306 serial EEPROM in all his characteristics.

PRODUCT DESIGN

DESIGN CHARACTERISTICS

Device Name	9306
Device Desctiption	256 bit serial EEPROM
Stepping (Revision)	1
Process Name	NMOS-F1
Array Organization:	16×16
Number of Rows	8
Number of Columns/Output	32
Number of Sense Amps/Output	1
Memory Cell Area	
Active	$3.5 \times 4\mu$
Total	$21 \times 30\mu$
Min Row Pitch	12μ
Column Pitch	21μ
Die Size	64×65 mils

MEMORY MATRIX CONFIGURATION

25
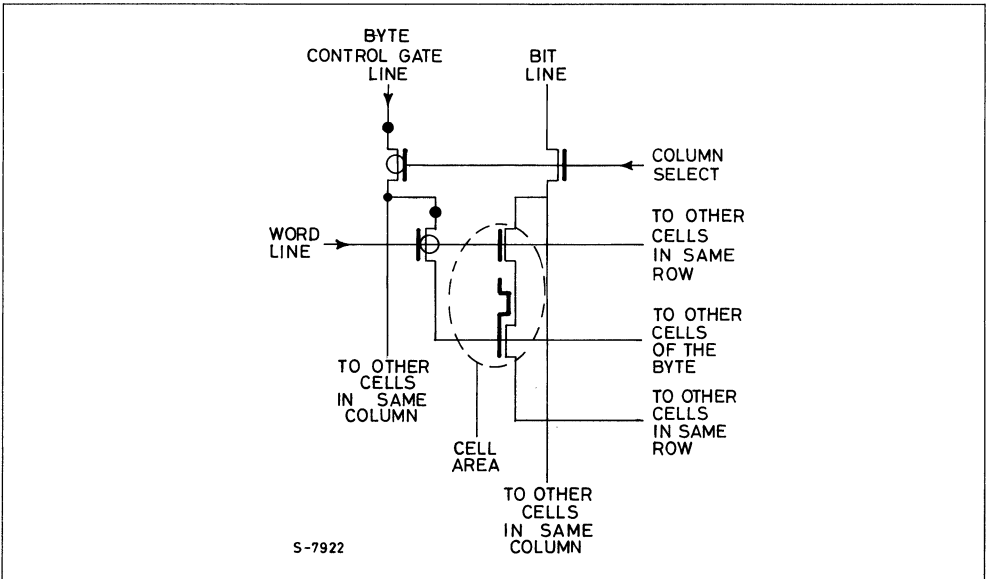
PRODUCT TECHNOLOGY

PROCESS DEFINITION

— The NMOS-F1 is a n-channel MOS process with a minimum transitstor length of $4\mu m$.
— The process has been optimized for a 21 Volt programming voltage.
— Active elements are obtained by means at ion implantation.
— NMOS-F1 is a two polysilicon level process; Source and Drain doping is As from As-doped polysilicon.
   A pictorial view of process is shown in Fig. 1.

MASK SEQUENCE

PLANOX	100
N + IMPLANT (FLOTOX)	150
DEPLETION	360
THINNER OXIDE	150
1st POLY	600
ENH. IMPLANT (LVS)	300
BURIED CONTACTS	380
2nd POLY (Logic)	401
DRAIN EXT.	451
CONTACTS	741
METAL	800
GLASS PASSIVATION	900
NITRIDE PASSIVATION	950

In the standard layout of the memory cell the mask 150 is used twice during the process:
first time to define the area to be implanted N + and a second time to define the area where the thin oxide will be grown.

MEMORY CELL

The memory cell is a transistor with a floating gate in first polysilicon level and a control gate in second polysilicon level.
The voltage of the floating gate is determined by capacitive coupling to the control gate and to the tunneling oxide, drain and field oxide areas.
The electric field during programming and the current in the channel of the transistor during reading depend on the voltage V_F, so it is clear that for good operation of the memory cell it is very important that the values of the capacitive couplings are not changed.
The layout of the memory cell is shown in Fig. 2. A section view of the cell structure is shown in Fig. 3.

Fig. 1
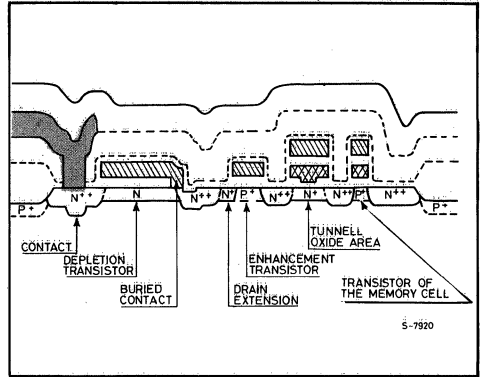
Fig. 2
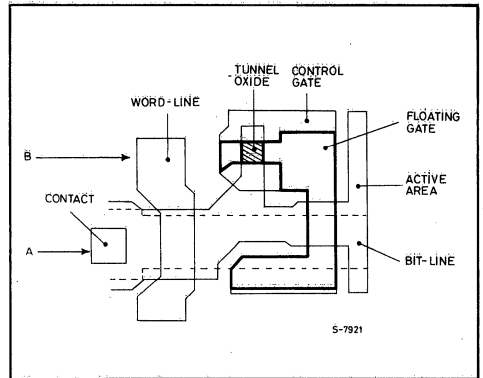
Fig. 3
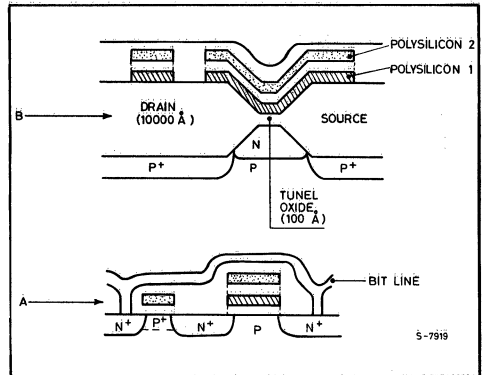
PROCESS CHARACTERISTICS

Device Name	9306
Device Description	256 bits serial EEPROM
Process Name	NMOS-F1
Wafer Size	4"
Min. Channel Length (left)	3.5μ
Number Poly Layer	2
Min. Number of Mask	13
Min. Number of Implants	5*
Lateral Diffusion	0.4μ
Oxide Thickness	
Poly 1 Gate	700 Å
Poly 2 Gate	800 Å
Thinner Oxide	100 Å
Poly 1 Thickness	1800 Å
Poly 2 Thickness	4500 Å
Metal Thickness	1.1μ
Min. Diffusion Width	4μ
Min. Poly 2 Width	3μ
Min. Poly 2 Spacing	4μ
Min. Metal Width	6μ
Min. Metal Spacing	6μ
Source-Drain Length	4μ
Contact to Poly 2 Spacing	4μ
Min. Contact Size	$4 \times 4\mu$
Thinner Oxide Area	$\sim 5\mu^2$
Stanting Resistivity	$30 \div 50$ Ohm/cm
Type of Dopomt	Arsenicum
Gate Material	Polysilicon
Word Line Material	Polysilicon
Bit Line Material	Metal
Metallization	Alluminum
Poly-Metal Isolation Material	P-VAPOX
Poly-Metal Isolation Thickness	1.1μ
Passivation Material	$VAPOX + Si_3N_4$
Passivation Thickness (Vapox)	7000 Å
Passivation Thickness (Nitride)	6000 Å

* Field, N + I.I., Depletion Load, Enhancement, Drain Extention

ELECTRICAL CHARACTERIZATION

TESTING FLOW-CHART
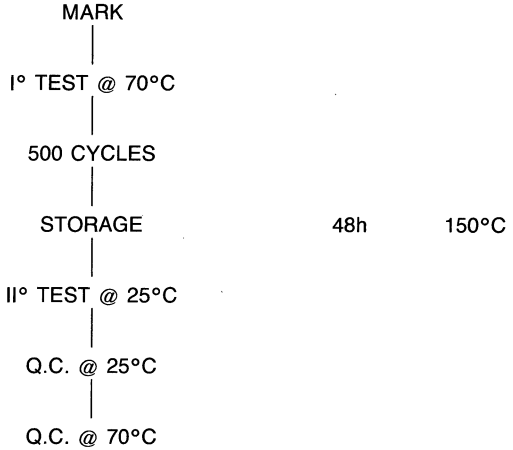
MARK

|

I° TEST @ 70°C

|

500 CYCLES

|

STORAGE   48h   150°C

|

II° TEST @ 25°C

|

Q.C. @ 25°C

|

Q.C. @ 70°C

```
            TWO AXIS SHMOO PLOT                          XINCOM

  PART NUMBER:    M225           BATCH:            LOG DATE:  10/15/85
  DEVICE TYPE:                   STAGE:            LOG TIME:  16:31:26
  TEST PROGRAM:   XNCAR225.TP    GROUP:   AUTO1    PRT DATE:  10/15/85
  ADAPTER NO.:                   HEAD:    01       PRT TIME:  16:38:02
  ---------------------------------------------------------------------
                         TEST CONDITIONS

  COMNT    DUTY CYCLE = 25 %
  ---------------------------------------------------------------------

  PRD   (NS)

  1000.0   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
  1200.0   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
  1400.0   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
  1600.0   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX............
  1800.0   XXXXXXXXXXXXXXXXX................................
  2000.0   XXXXXXXXXXXXX...................................
  2200.0   XXXXXXXXXX.....................................
  2400.0   XXXXXXXX.......................................
  2600.0   XXXXXXX........................................
  2800.0   XXXXXXX........................................
  3000.0   XXXXXX.........................................
  3200.0   XXXXX..........................................
  3400.0   XXXXX..........................................
  3600.0   XXXXX..........................................
  3800.0   XXXXX..........................................
  4000.0   XXXXX.........................................
  4200.0   XXXXX.........░░░░░░.........................
  4400.0   XXXXX.........░░░░░░.........................
  4600.0   XXXXX.........░░░░░░.........................
  4800.0   XXXXX.........░░░░░░.........................
  5000.0   XXXXX.........░░░░░░.........................
           ↑.........↑.....↑.......↑.........↑.........↑.
           3.00      4.00   5.00    6.00     7.00      8.00
                            VCC1  ( V)
```

SPECIFICATION WORK AREA

```
            TWO AXIS SHMOO PLOT                        XINCOM

PART NUMBER:    M225              BATCH:           LOG DATE:  10/15/85
DEVICE TYPE:                      STAGE:           LOG TIME:  16:37:43
TEST PROGRAM:   XNCAR225.TP       GROUP:   AUTO1   PRT DATE:  10/15/85
ADAPTER NO.:                      HEAD:    01      PRT TIME:  16:38:32
-----------------------------------------------------------------------
                          TEST CONDITIONS

COMNT    WRITE TIME
-----------------------------------------------------------------------

TW    (MS)

  0.25   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
  0.50   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
  0.75   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
  1.00   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
  1.25   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX............
  1.50   XXXXXX............................................
  1.75   XXXXXX............................................
  2.00   XXXXXX............................................
  2.25   XXXXXX............................................
  2.50   XXXXXX............................................
  2.75   XXXXXX............................................
  3.00   XXXXXX............................................
  3.25   XXXXXX............................................
  3.50   XXXXXX............................................
  3.75   XXXXXX............................................
  4.00   XXXXXX............................................
         ↑.........↑.........↑.........↑.........↑.........↑.
         3.00      4.00      5.00      6.00      7.00      8.00
                              VCC1   ( V)
```

```
            TWO AXIS SHMOO PLOT                        XINCOM

PART NUMBER:    M225              BATCH:           LOG DATE:  10/15/85
DEVICE TYPE:                      STAGE:           LOG TIME:  16:34:44
TEST PROGRAM:   XNCAR225.TP       GROUP:   AUTO1   PRT DATE:  10/15/85
ADAPTER NO.:                      HEAD:    01      PRT TIME:  16:38:18
-----------------------------------------------------------------------
                          TEST CONDITIONS

COMNT    ERASE TIME
-----------------------------------------------------------------------

TE    (MS)

  0.25   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
  0.50   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
  0.75   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
  1.00   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
  1.25   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
  1.50   XXXXXXXXXXXXXXXXXXXXXXXXX..........................
  1.75   XXXXXX............................................
  2.00   XXXXXX............................................
  2.25   XXXXXX............................................
  2.50   XXXXXX............................................
  2.75   XXXXXX............................................
  3.00   XXXXXX............................................
  3.25   XXXXXX............................................
  3.50   XXXXXX............................................
  3.75   XXXXXX............................................
  4.00   XXXXXX............................................
         ↑.........↑.........↑.........↑.........↑.........↑.
         3.00      4.00      5.00      6.00      7.00      8.00
                              VCC1   ( V)
```
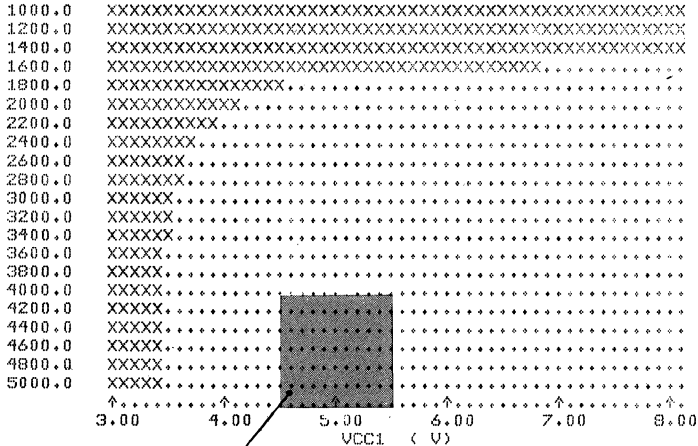
CHARACTERIZZATION RESULTS

Parameter	Value	Measurements			Limit	Unit
		0°C	25°C	70°C		
I_{CC1}	min	1.1	1.2	1.1		
	typ.	1.53	1.53	1.47	< 5 mA	mA
	max	2.0	2.0	1.9		
I_{CC2}	min	1.1	1.1	1.1		
	typ.	1.48	1.45	1.39	< 3 mA	mA
	max	2.0	2.0	1.8		
I_{CC3}	min	2.0	2.0	1.9		
	typ.	2.76	2.58	2.38	< 6 mA	mA
	max	3.5	3.4	3.0		
V_{OH}	min	2.83	2.84	2.84		
	typ.	2.89	2.90	2.91	> 2.4 V	V
	max	3.00	3.03	3.03		
V_{OL}	min	0.063	0.065	0.069		
	typ.	0.066	0.071	0.077	< 0.4 V	V
	max	0.070	0.077	0.082		
$V_{CC\ MIN}$	min		3.50	3.40		
	typ.		3.65	3.63	> 4.5 V	V
	max		3.90	3.90		
PW CK MIN.	min		450	500		
	typ.		657	682	> 1.000 ns	ns
	max		850	850		
T-ERA MIN.	min		1.75	2.00		
	typ.		2.01	2.28	$5 \div 30$ ms	ms
	max		2.50	2.75		
T-WRI MIN.	min		1.50	1.75		
	typ.		1.80	2.03	$5 \div 30$ ms	ms
	max		2.25	2.50		
$V_{CC\ MAX}$			> 8 V	> 8 V	< 5.5 V	V

BUILD ASSEMBLY INFORMATION
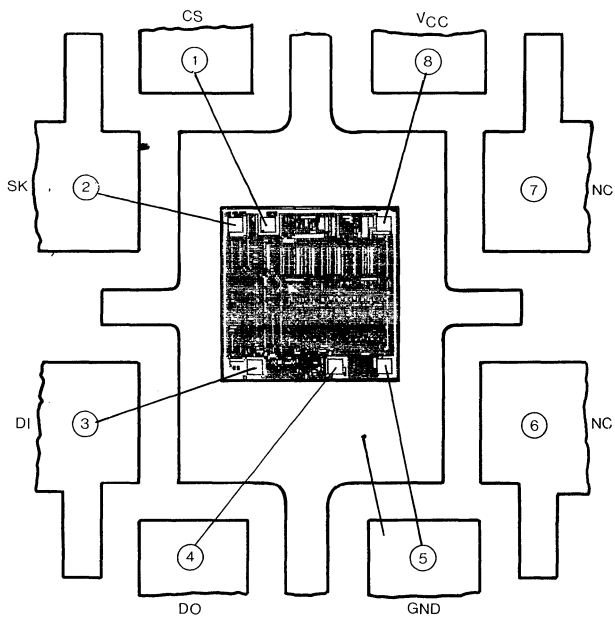
S-8645

DOUBLE LAYER P-VAPOX AND Si$_3$N$_4$ GLASS PASSIVATION

A. Panchieri Q.A. MOS DIVISION

Newly developed passivation process for NMOS/HS-CMOS devices gives improved protection to die encapsulated in plastic packages.

PROCESS DESCRIPTION

The process consists of a two layer film of P-Vapox (phosphorus doped silicon oxide) and Si$_3$ N$_4$ (silicon nitride), obtained by two different masking and etching steps to avoid defects caused by lack of dieletric integrity.

The process gives good metal step coverage together with PECVD (Plasma Enhanced Chemical Vapox Deposition) to avoid cracking near metal edge and possible hillocks defects.

The double layer enables us, by means of an appropriate oversize either at the boundaries of the die side or at the bonding pad side, to ensure full sealing of the underlying P-Vapox layer.

This prevents the layer from being exposed to moisture coming from the package. Thus the probability of metal corrosion on the bonding pad due to phosphoric acid is drastically reduced.

As a result the die is provided with a very good humidity immunity.

PROCESS FLOW

(After metal mask)

P-Vapox deposition of 4% phosphorus concentration

↓

P-Vapox mask and plasma etch

↓

Silicon nitride deposition

↓

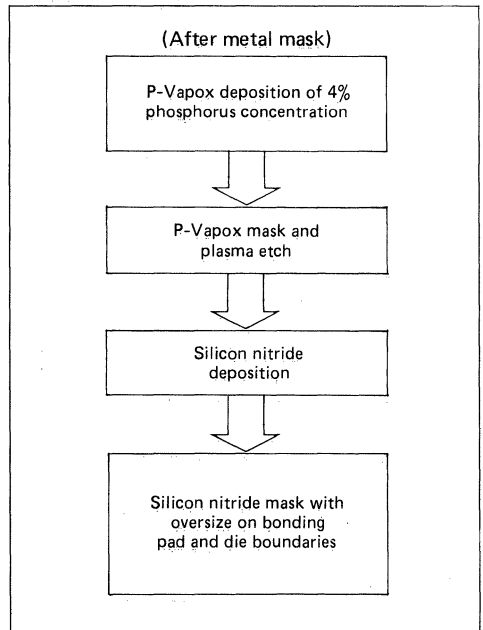Silicon nitride mask with oversize on bonding pad and die boundaries

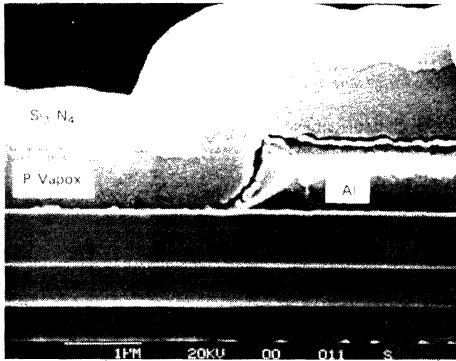FIG. 1 - TYPICAL MICROSECTION OF DEVICE WITH NITRIDE PASSIVATION.
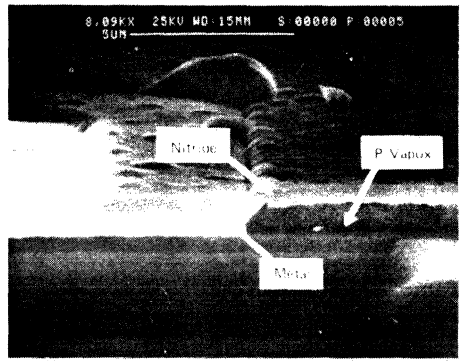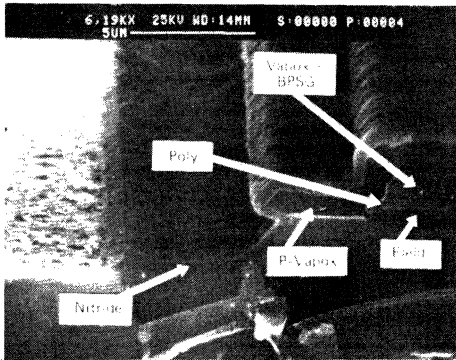

FIG. 3 - SECTION ALONG THE PAD

FIG. 2 - SECTION ALONG THE SCRIBING LINE.

RELIABILITY RESULTS

The reliability performance in moist ambient was evalued using both 85°C/85% RH/BIAS and 121°C Pressure Pot test.

Different products in different plastic packages were tested.

To give an idea of reliability performances obtained on products with the new passivation process, we have set out the process qualification test results in the following table:

|	HS-CMOS LOGICS			µPROCESSORS		MEMORIES	
	HOURS	SAMPLE	FAIL	SAMPLE	FAIL	SAMPLE	FAIL
STATIC/DYNAMIC LIFE TEST $T_{amb}=125°C$ $V_{CC}=STD$	1000	1355	0	385	0	270	0
	2000	915	0	385	0	270	0
	3000	600	0	—	—	—	—
	4000	600	0	—	—	—	—
TEMP HUMIDITY BIAS (85°C/85% RH) $V_{CC}=STD$	1000	740	0	240	0	360	0
	2000	510	0	240	0	360	0
	3000	260	1 funct.	—	—	—	—
	4000	259	0	—	—	—	—
PRESSURE POT $T_{amb}=121°C$-2 atm	96	965	0	540	0	250	0
	144	775	1 funct.	540	0	250	0
	192	320	0	300	0	120	0
	288	320	0	300	1 funct.	120	0

ERASABLE PROGRAMMABLE
READ ONLY MEMORY

M2716

16K (2K × 8) UV ERASABLE PROM

- FAST ACCESS TIME:
  350ns MAX M2716-1
  450ns MAX M2716

- SINGLE +5V POWER SUPPLY

- LOW POWER DISSIPATION:
  525 mW MAX. ACTIVE POWER
  132 mW MAX. STANDBY POWER

- SIMPLE PROGRAMMING REQUIREMENTS
  — SINGLE LOCATION PROGRAMMING
  — PROGRAMS WITH ONE 50 ms PULSE

- INPUTS AND OUTPUTS TTL COMPATIBLE
  DURING READ PROGRAM

- COMPLETELY STATIC

- EXTENDED TEMPERATURE RANGE
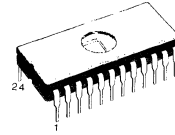
F
Ceramic Package
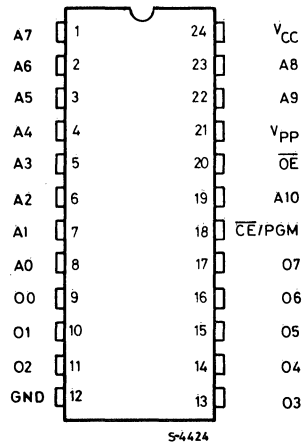ORDERING NUMBERS: M2716F1
M2716-1F1
M2716F6
M2716-1F6

DESCRIPTION

The M2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The M2716 operates from a single − 5V power supply, has a static standby mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical. The M2716, with its single 5-volt supply and with an access time up to 350ns, is ideal for use with the newer high performance +5V microprocessor such as the Z8®, Z80® and Z8000™. The M2716P is also the first EPROM with a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The M2716 has the simplest and fastest method yet devised for programming EPROMs — single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Program any location at any time-either individually, sequentially or at random, with the M2716's single address location programming. Total programming time for all 16.384 bits is only 100 seconds:

The M2716 is available in 24-lead dual in-line ceramic package glass lens (frit-seal)

PIN CONNECTIONS

A7	1	24	V_{CC}
A6	2	23	A8
A5	3	22	A9
A4	4	21	V_{PP}
A3	5	20	$\overline{OE}$
A2	6	19	A10
A1	7	18	$\overline{CE}$/PGM
A0	8	17	O7
O0	9	16	O6
O1	10	15	O5
O2	11	14	O4
GND	12	13	O3

S-4424
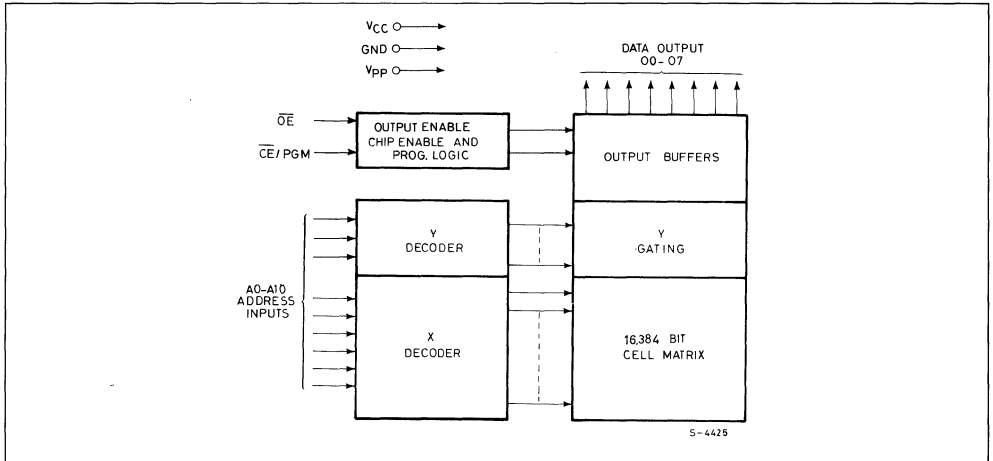
PIN NAMES

A0-A10	ADDRESSES
$\overline{CE}$/PGM	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
O0-O7	OUTPUTS

BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	All Input or Output voltages with respect to ground	+ 6 to − 0.3	V
V_{PP}	Supply voltage with respect to ground during program	+ 26.5 to − 0.3	V
T_{amb}	Ambient temperature under bias: standard extended	0 to + 70 − 40 to + 85	°C
T_{stg}	Storage temperature range	− 65 to + 125	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE \ PINS	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
READ	V_{IL}	V_{IL}	+ 5	+ 5	D_{OUT}
STANDBY	V_{IH}	Don't Care	+ 5	+ 5	HIGH Z
PROGRAM	Pulse V_{IL} to V_{IH}	V_{IH}	+ 25	+ 5	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	+ 25	+ 5	D_{OUT}
PROGRAM INHIBIT	V_{IL}	V_{IH}	+ 25	+ 5	HIGH Z

Note: The five modes of operation of the M2716P are listed in this table. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are a + 5V V_{CC} and a V_{PP} power supply must be at 25V during the three programming modes, and must be at 5V in the other two modes.

READ OPERATION
DC AND AC OPERATING CONDITIONS

	M2716F1	M2716-1F1	M2716F6	M2716-1F6
Operating Temperature Range	0 to 70°C	0 to 70°C	−40 to 85°C	−40 to 85°C
V_{CC} Power Supply [1,2]	5V ±5%	5V ±10%	5V ±5%	5V ±10%
V_{PP} Power Supply [2]	$V_{CC} ± 0.6$	$V_{CC} ± 0.6$	$V_{CC} ± 0.6$	$V_{CC} ± 0.6$

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ. (3)	Max.	
I_{LI}	Input Load Current	$V_I = 5.25V$			10	μA
I_{LO}	Output Leakage Current	$V_O = 5.25V$			10	μA
$I_{PP1(2)}$	$V_{PP} = 5.25V$				5	mA
$I_{CC1(2)}$	V_{CC} Supply Current (Standby)	$\overline{CE} = V_{IH}$ $\overline{OE} = V_{IL}$		10	25	mA
$I_{CC2(2)}$	V_{CC} Supply Current (Active)	$\overline{OE} = \overline{CE} = V_{IL}$		57	100	mA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400 \mu$A	2.4			V

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	M2716		M2716-1		Unit
			Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		450		350	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		450		350	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		120		120	ns
$t_{DF(4)}$	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	100	0	100	ns
t_{OH}	Output Hold from Address $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		ns

CAPACITANCE[4] ($T_{amb} = 25°C$, f = 1 MHz)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_I = 0V$		4	6	pF
C_{OUT}	Output Capacitance	$V_O = 0V$		8	12	pF

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_{amb} = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and not 100% tested.
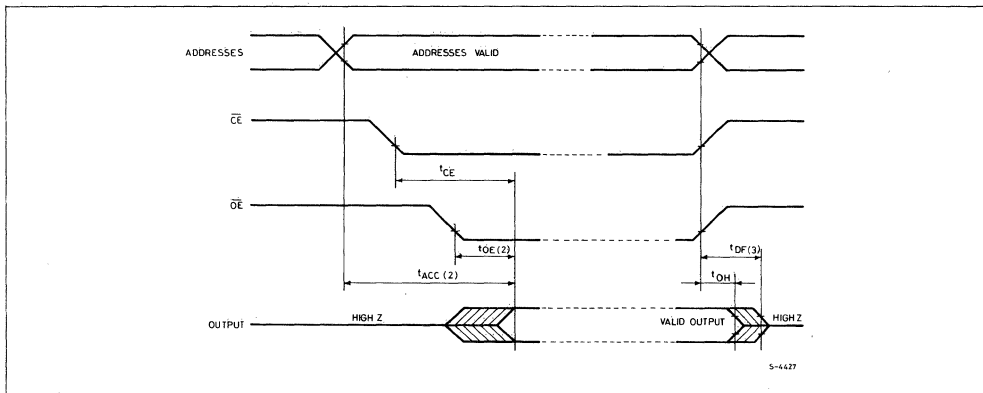
AC TEST CONDITIONS
Output Load: 100pF + 1TTL Gate
Input Rise and Fall Times: $\leqslant$ = 20ns
Input Pulse Levels: 0.8 to 2.2V
Timing Measurement Reference Levels: Inputs 1 and 2V
Outputs 0.8 and 2V

AC WAVEFORMS

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

READ MODE
The M2716 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs 120 ns (t_{OE}) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE
The M2716 has a standby mode which reduces the active power dissipation by 75%, from 525mW to 132mW. The M2716 is placed in the standby mode by applying a TTL high signal to $\overline{CE}$ input. When in standby mode, the output are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TIEING
Because M2716's are usually used in larger memory arrays, the product has 2 line control function that accommodates this use of multiple memory connection. The two line control function allows for:

a) the lowest possible memory power dissipation

b) complete assurance that output bus contention will not oucur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and the output pins are only active when data is desired from a particular memory device.

PROGRAMMING OPERATION [1] ($T_{amb} = 25°C \pm 5\%$, V_{CC}[2] $= 5V \pm 5\%$, V_{PP}[2,3] $= 25V \pm 1V$)

DC AND OPERATING CHARACTERISTIC:

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current (for Any Input)	$V_I = 5.25V/0.45$			10	μA
V_{IL}	Input Low Level		-0.1		0.8	V
V_{IH}	Input High Level		2.0		$V_{CC} + 1$	V
I_{CC}	V_{CC} Supply Current				100	mA
I_{PP1}	V_{PP} Supply Current	$\overline{CE}$/PGM $= V_{IL}$			5	mA
I_{PP2}	V_{PP} Supply Current During Programming Pulse	$\overline{CE}$/PGM $= V_{IH}$			30	mA

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Setup Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{AH}	Address Hold Time		2			μs
t_{OEH}	$\overline{OE}$ Hold Time		2			μs
t_{DH}	Data Hold Time		2			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{OE}$/PGM $= V_{IL}$	0		120	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE}$/PGM $= V_{IL}$			120	νs
t_{PW}	Program Pulse Width		45	50	55	ms
t_{PRT}	Program Pulse Rise Time		5			ns
t_{PFT}	Program Pulse Fall Time		5			νs

CAUTION: The V_{CC} and V_{PP} supplied must be sequenced on and off such that V_{CC} is applied simultaneosly or before V_{PP} and removed simultaneosly or after V_{PP} to prevent damage to the M2716. The maximum allowable voltage during programming which may be applied to the V_{PP} with respect to ground is $+26V$. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding the 26-volt maximum specification. For convenience in programming, the M2716 may be verified with the V_{PP} supply at $25V \pm 1V$. During normal read operation, however, V_{PP} must be at V_{CC}.

Notes:
1. SGS guarantees the product only if it is programmed to specifications described herein.
2. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The M2716 must not be inserted into or removed from a board with V_{PP} at $25 \pm 1V$ to prevent damage to the device.
3. The maximum allowable voltage which may be applied to the V_{PP} pin during programming is $+ 26V$. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 26V maximum specification.
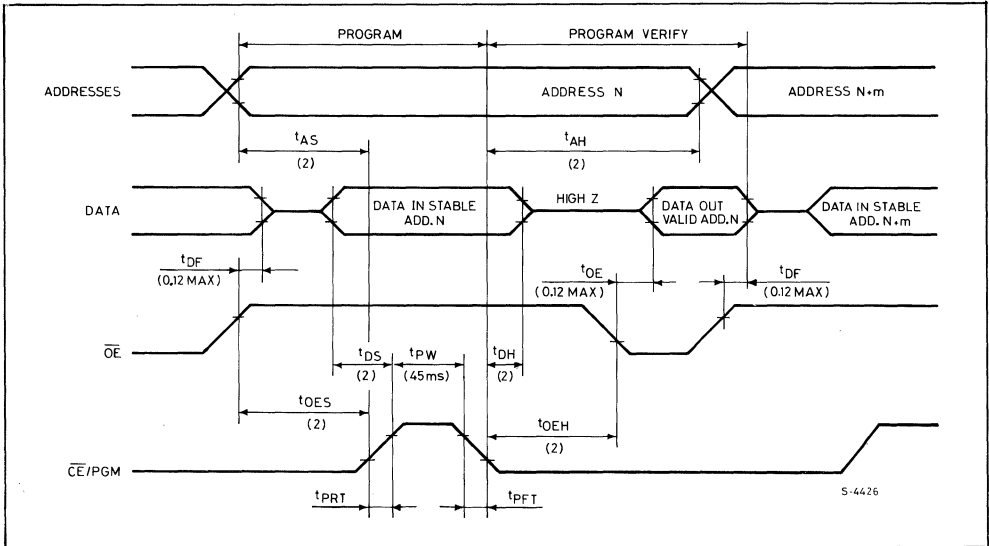
M2716

PROGRAMMING WAVEFORMS
($V_{PP} = 25V \pm 1V$, $V_{CC} = 5V \pm 5\%$)

Note: All times shown in parentheses are minimum times and are μsec unless otherwise noted.

PROGRAMMING

Initially, and after each erasure, all bits of the M2716 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure. The M2716 is in the programming mode when the V_{PP} power supply is at 25V and $\overline{OE}$ is at V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. When the address and data are stable, a 50 msec, active high, TTL program pulse is applied to the $\overline{CE}$/PGM input. A program pulse must be applied at each address location to be programmed. You can program any location at any time — either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec. The M2716 must not be programmed with a DC signal applied to the $\overline{CE}$/PGM input.

Programming of multiple M2716s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled M2716s may be connected together when they are programmed with the same data. A high level TTL pulse applied to the $\overline{CE}$/PGM input-programs the parallel M2716s.

PROGRAM INHIBIT

Programming of multiple M2716s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel M2716s may be common. A TTL level program pulse applied to a M2716's $\overline{CE}$/PGM input with V_{PP} at 25V will program that M2716. A low level $\overline{CE}$/PGM input inhibits the other M2716 from beign programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at 5V.

ERASURE OPERATION

The erasure characteristics of the M2716 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (A). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 A range. Data show that constant exposure to room level fluorescent lighting could erase the typical M2716 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M2716 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested to put opaque labels over the M2716 window to prevent unintentional erasure.

The recommended erasure procedure for the M2716 is exposure to shortware ultraviolet light which has a wavelength of 2537 Angstroms (A). The integrated dose (i.e. UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μ W/cm^2 power rating. The M2716 should be placed within 2.5 cm of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.
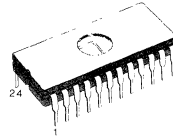
M2732A

32K (4K × 8) UV ERASABLE PROM

- FAST ACCESS TIME:
  200ns MAX M2732A-2F1
  250ns MAX M2732AF1/M2732AF6
  300ns MAX M2732A/-3F1
  450ns MAX M2732A-4F1/M2732A-4F6

- SINGLE +5V POWER SUPPLY

- LOW STANDBY CURRENT 35mA MAX

- INPUTS AND OUTPUTS TTL COMPATIBLE
  DURING READ AND PROGRAM

- COMPLETELY STATIC

F
Ceramic Package
ORDERING NUMBERS: M2732AF1
M2732A-2F1
M2732A-3F1
M2732A-4F1

M2732AF6
M2732A-4F6

DESCRIPTION

The M2732A is a 32,768-bits ultraviolet erasable and electrically programmable read-only memory (EPROM). It is organized as 4,096 words by 8 bits and manufactured using SGS' N-channel Si-Gate MOS process. The M2732A with its single +5V power supply and with an access time of 200ns, is ideal for use with the high performance +5V microprocessors such as the Z8®, Z80® and Z8000™. The M2732A has an important feature which is the separate output control, Output Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control elimitates bus contention in multiple bus microprocessor systems.

The M2732A also features a standby mode which reduces the power dissipation without increasing access time. The active current is 125 mA while the maximum standby current is only 35 mA a 70% saving. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input.

The M2732A is available in a 24-lead dual in-line ceramic package glass lens (frit-seal).

PIN CONNECTIONS

S – 6705
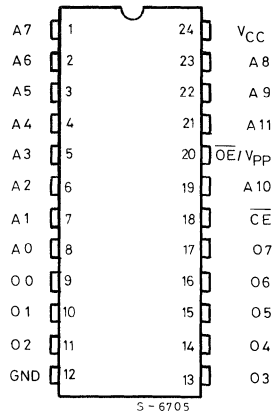
PIN NAMES

A0-A11	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE INPUT
O0-O7	DATA INPUT/OUTPUT

M2732A

BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

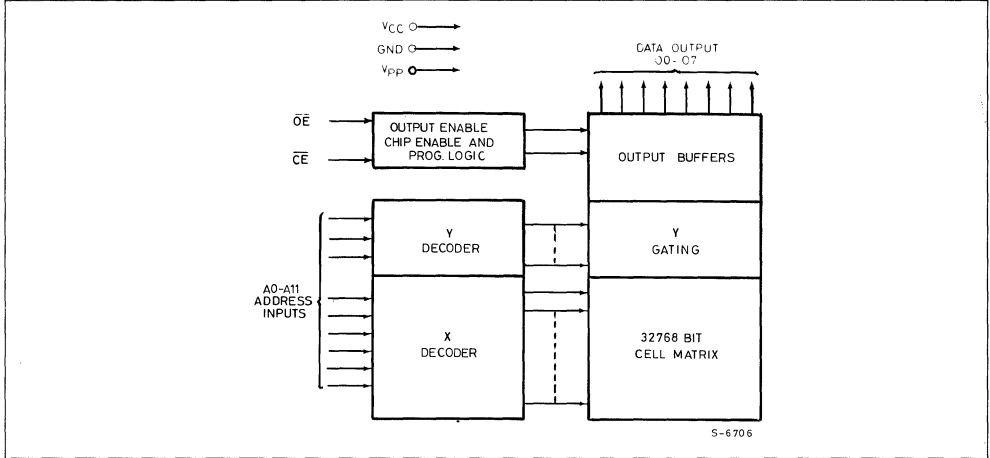| Symbol	Parameter	Value	Unit
V_I	All Input or Output voltages with respect to ground	+ 6 to − 0.6	V
V_{PP}	Supply voltage with respect to ground during program	+ 22 to − 0.6	V
T_{amb}	Ambient temperature under bias F1/-2F1/-3F1/-4F1	− 10 to + 80	°C
	F6/4F6	− 50 to + 95	°C
T_{stg}	Storage temperature range	− 65 to + 125	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

PINS MODE	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
READ	V_{IL}	V_{IL}	+ 5	D_{OUT}
STANDBY	V_{IH}	Don't Care	+ 5	High Z
PROGRAM	V_{IL}	V_{PP}	+ 5	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	+ 5	D_{OUT}
PROGRAM INHIBIT	V_{IH}	V_{PP}	+ 5	High Z

READ OPERATION
DC AND AC CONDITIONS

	F1/ – 2F1 – 3F1/ – 4F1	F6/ – 4F6
Operating Temperature Range	0 to 70°C	– 40 to 85°C
V_{CC} Power Supply [1,2]	5V ±5%	5V ±5%
V_{PP} Voltage [2]	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.[3]	Max.	
I_{LI}	Input Load Current	$V_{IN} = 5.5V$			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$			10	μA
I_{CC1}[2]	V_{CC} Current Standby	$\overline{CE} = V_{IH}$ $\overline{OE} = V_{IL}$			35	mA
I_{CC2}[2]	V_{CC} Current Active	$\overline{CE} = \overline{OE} = V_{IL}$		70	125	mA
V_{IL}	Input Low Voltage		– 0.1		+ 0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400 \mu$A	2.4			V

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	M2732A-2		M2732A		M2732A-3		M2732A-4		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		200		250		300		450	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		200		250		300		450	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		100		100		150		150	ns
t_{DF}[4]	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	60	0	60	0	130	0	130	ns
t_{OH}	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

CAPACITANCE [4] ($T_{amb} = 25°C$, f = 1MHz)

Parameter	Test conditions	Values			Unit
		Min.	Typ.	Max.	
$C_{IN\,1}$ Input Capacitance excepet $\overline{OE}/V_{PP}$	$V_{IN} = 0$		4	6	pF
$C_{IN\,2}$ $\overline{OE}/V_{PP}$ Input capacitance	$V_{IN} = 0$			20	pF
Output capacitance	$V_{OUT} = 0$		8	12	pF

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_{amb} = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested
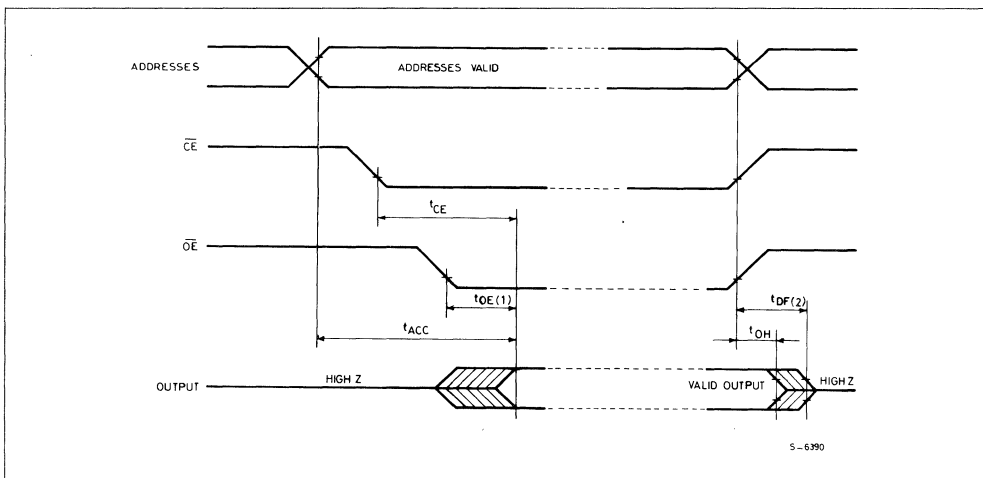
AC TEST CONDITIONS
Output Load: 100pF + 1TTL Gate
Input Rise and Fall Times: $\leqslant = 20$ns
Input Pulse Levels: 0.45 to 2.4V
Timing Measurement Reference Levels: Inputs   0.8 and 2V
                                         Outputs 0.8 and 2V

AC WAVEFORMS

Notes:
1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

READ MODE
The M2732A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to delay from $\overline{CE}$ to output ($t\overline{CE}$). Data is available at the outputs after the falling edge of OE, assuming that CE has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE
The M2732A has a standby mode which reduces the active power current by 70%, from 125mA to 35mA. The M2732A is placed in the standby mode by applying a TTL high signal to $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TIEING
Because M2732A's are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a) the lowest possible memory power dissipation

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

PROGRAMMING OPERATION [1]($T_{amb} = 25°C \pm 5°C$, V_{CC}[2]$= 5V \pm 5\%$, V_{PP}[2,3]$= 21V \pm 0.5V$)

DC AND OPERATING CHARACTERISTIC.

Symbol	Parameter	Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}			10	μA
V_{IL}	Input Low Level		-0.1		0.8	V
V_{IH}	Input High Level		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage During Verify	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage During Verify	$I_{OH} = -400 \mu A$	2.4			V
I_{CC2}	V_{CC} Supply Current (Active)			70	125	mA
I_{PP}	V_{PP} Supply Current	$\overline{CE} = V_{IL}, \overline{OE} = V_{PP}$			30	mA

AC CHARACTERISTICS

Symbol	Parameter	Test conditions	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Set Up Time		2			μs
t_{OES}	$\overline{OE}$ Set Up Time		2			μs
t_{DS}	Data Set Up Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Old Time		2			μs
t_{DF}	Chip Enable to Output Float Delay		0		130	ns
t_{DV}	Data valid from $\overline{CE}$	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$			1	μs
t_{PW}	$\overline{CE}$ Pulse Width During Programming		45	50	55	ms
t_{PRT}	$\overline{OE}$ Pulse rise time During Programming		50			ns
t_{VR}	V_{PP} recovery time		2			μs

Notes:
1. SGS guarantees the product only if it is programmed to specifications described herein.
2. V_{CC} must be applied simultaneusly with or before V_{PP} and removed simultaneously with or after V_{PP}. The M2732A must not be inserted into or removed from a board with V_{PP} at $21 \pm 0.5V$ or damage may occur to the device.
3. The maximum allowable voltage which may be applied to the V_{PP} pin during programming is $+22V$. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 22V maximum specification.

PROGRAMMING WAVEFORMS
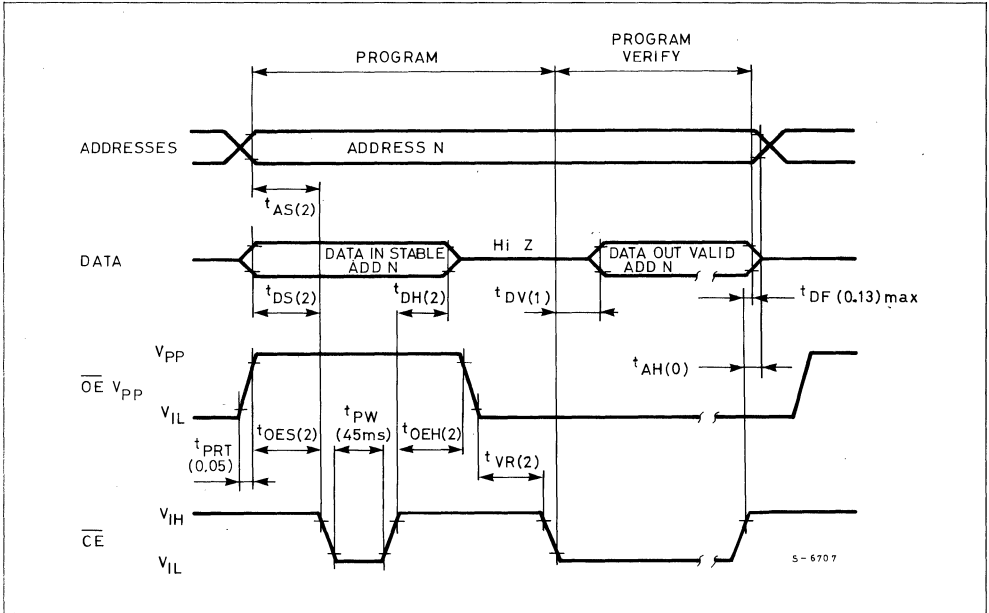
1. All times shown in ( ) are minimum and in μsec unless otherwise specified.
2. The input timing reference level is 1V for V_{IL} and 2V for V_{IH}.
3. t_{OE} and t_{OF} are characteristics of the device but must be accomodated by the programmer.

PROGRAMMING

Caution: Exceeding 22V on pin (V_{PP}) will damage the M2732A.

When delivered, and after each erasure, all bits of the M2732A are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.
The M2732A is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 21V. It is required that a 0.1 μF capacitor be placed across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.
When the address and data are stable, a 50 msec, active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time — either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec. The 2732A must not be programmed with a DC signal applied to the $\overline{CE}$ input.
Programming of multiple 2732As in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled M2732As may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled 2732As.

PROGRAM INHIBIT

Programming of multiple 2732As in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel

2732As may be common. A TTL level program pulse applied to a 2732A's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 21V will program that 2732A. A high level $\overline{CE}$ input inhibits the other 2732As from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}.

ERASURE OPERATION

The erasure characteristics of the M2732A are such that erasure begins when the cels are exposed to light with wavelengths shorter than approximately 4000 Angstroms (A). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 A range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M2732A in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to the direct sunlight. If the M2732A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels to put over the M2732A window to prevent unintentional erasure.

The recommended erasure procedure for the M2732A is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (A). The integrated dose (i.e. UV intensity × exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 μW/cm^2 power rating. The M2732A should be placed within 2.5 cm of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.
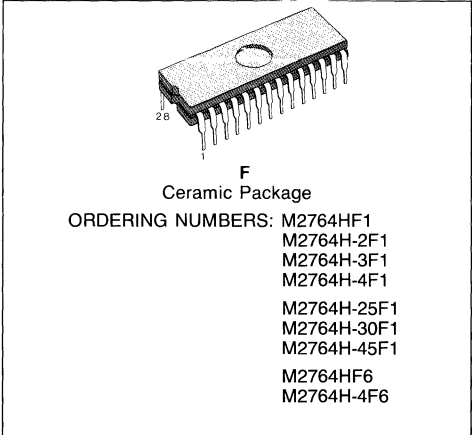
M2764

64K (8K × 8) UV ERASABLE PROM

- FAST ACCESS TIME:
  200ns MAX M2764-2F1
  250ns MAX M2764F1/-25F1/F6
  300ns MAX M2764-3F1/-30F1
  450ns MAX M2764-4F1/-45F1/-4F6

- SINGLE +5V POWER SUPPLY

- LOW STANDBY CURRENT 40mA MAX

- INPUTS AND OUTPUTS TTL COMPATIBLE
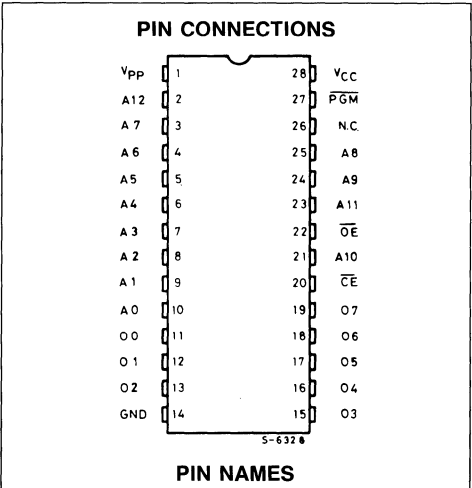 DURING READ AND PROGRAM

- COMPLETELY STATIC

F
Ceramic Package

ORDERING NUMBERS: M2764HF1
M2764H-2F1
M2764H-3F1
M2764H-4F1

M2764H-25F1
M2764H-30F1
M2764H-45F1

M2764HF6
M2764H-4F6

DESCRIPTION
The M2764 is a 65,536-bits ultraviolet erasable and electrically programmable read-only memory (EPROM). It is organized as 8,192 words by 8 bits and manufactured using SGS' N-channel Si-Gate MOS process.

The M2764 with its single +5V power supply and with an access time of 200ns, is ideal for use with the high performance +5V microprocessor such as Z8®, Z80® and Z8000™. The M2764 has an important feature which is the separate the output control, Ouptut Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems.

The M2764 also features a standby mode which reduces the power dissipation without increasing access time. The active current is 100mA while the maximum standby current is only 40mA, a 60% saving. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input.
The M2764 is available in a 28-lead dual in-line ceramic package glass lens. (frit-seal)

PIN CONNECTIONS

V_{PP}	1	28	V_{CC}
A12	2	27	$\overline{PGM}$
A7	3	26	N.C.
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	$\overline{OE}$
A2	8	21	A10
A1	9	20	$\overline{CE}$
A0	10	19	O7
O0	11	18	O6
O1	12	17	O5
O2	13	16	O4
GND	14	15	O3

S-6328

PIN NAMES

A0-A12	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE INPUT
$\overline{PGM}$	PROGRAM
N.C.	NO CONNECTION
O0-O7	DATA INPUT/OUTPUT

BLOCK DIAGRAM
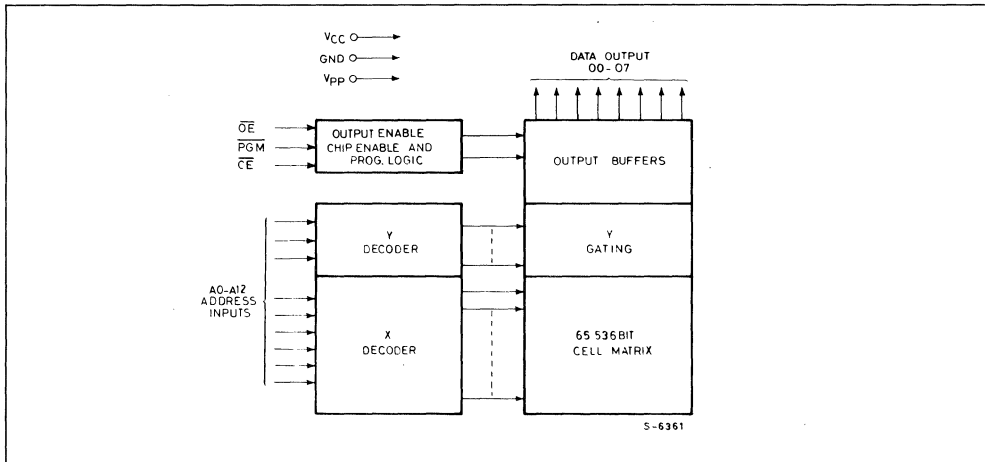
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	All Input or Output voltages with respect to ground	$+ 7$ to $- 0.6$	V
V_{PP}	Supply voltage with respect to ground during program	$+22$ to $- 0.6$	V
T_{amb}	Ambient temperature under bias /F1/-2F1/-3F1/-4F1/ /-25F1/-30F1/-45F1 /F6-4F6	$- 10$ to $+ 80$	°C
T_{stg}	Storage temperature range	$- 65$ to $+ 125$	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	OUTPUTS
READ	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
STANDBY	V_{IH}	X	X	V_{CC}	V_{CC}	HIGH Z
PROGRAM	V_{IL}	X	V_{IL}	V_{PP}	V_{CC}	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
PROGRAM INHIBIT	V_{IH}	X	X	V_{PP}	V_{CC}	HIGH Z

X = Don't care

READ OPERATION
DC AND AC CONDITIONS

	F1/ − 2F1 − 3F1/ − 4F1	− 25F1/ − 30F1/ − 45F1	F6/ − 4F6
Operating Temperature Range	0 to 70°C	0 to 70°C	− 40 to 85°C
V_{CC} Power Supply (1,2)	5V ±5%	5V ±10%	5V ±5%
V_{PP} Voltage (2)	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.(3)	Max.	
I_{LI}	Input Load Current	$V_{IN} = 5.5V$			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$			10	μA
$I_{PP1(2)}$	V_{PP} Current Read	$V_{PP} = 5.5V$		2	5	mA
$I_{CC1(2)}$	V_{CC} Current Standby	$\overline{CE} = V_{IN}$			40	mA
$I_{CC2(2)}$	V_{CC} Current Active	$\overline{CE} = \overline{OE} = V_{IL}$		50	100	mA
V_{IL}	Input Low Voltage		− 0.1		+ 0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = − 400 \mu A$	2.4			V

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	2764-2		2764 2764-25		2764-3 2764-30		2764-4 2764-45		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		200		250		300		450	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		200		250		300		450	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		75		100		120		150	ns
$t_{DF(4)}$	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	60	0	85	0	105	0	130	ns
t_{OH}	Output Hold from Address $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

CAPACITANCE[5] ($T_{amb} = 25°C$, f = 1 MHz)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_{amb} = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and not 100% tested. Output Float is defined as the point where data is no longer driven-see timing diagram.
5. This parameter is only sampled and not 100% tested.

M2764

AC TEST CONDITIONS
Output Load: 100pF + 1TTL Gate
Input Rise and Fall Times: $\leqslant$ = 20ns
Input Pulse Levels: 0.45 to 2.4V
Timing Measurement Reference Levels: Inputs   0.8 and 2V
Outputs 0.8 and 2V

AC TESTING INPUT/OUTPUT WAVEFORM
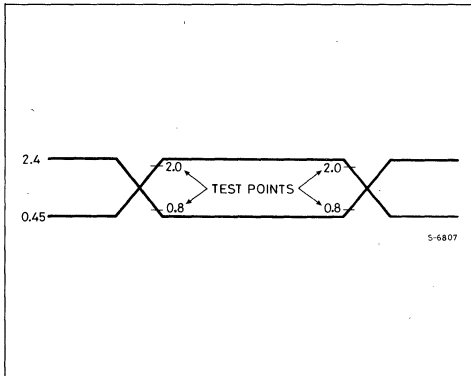
AC TESTING LOAD CIRCUIT
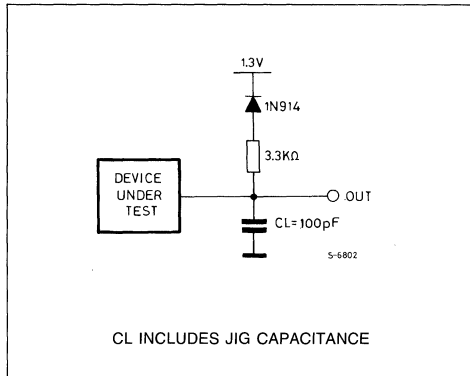
CL INCLUDES JIG CAPACITANCE

AC WAVEFORMS
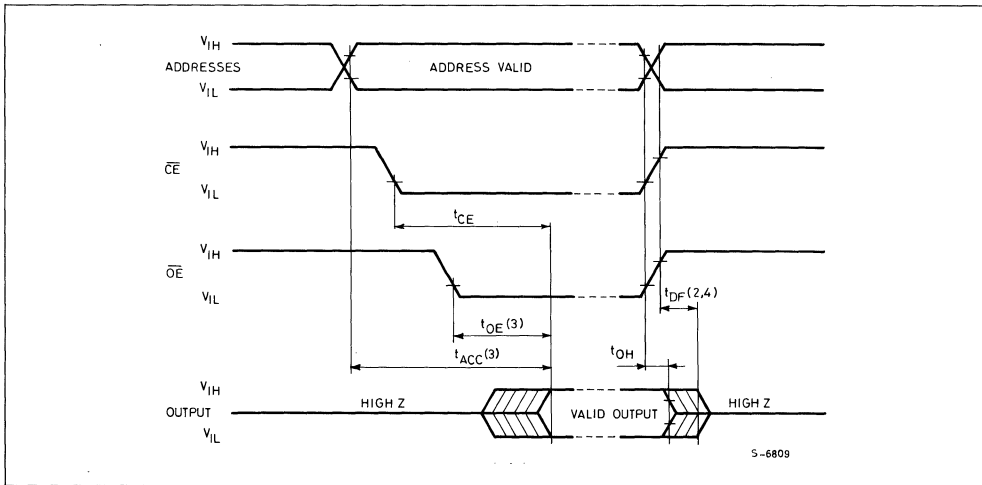
Notes:
1. Typical values are for T_{amb} = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

READ MODE

The M2764 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M2764 has a standby mode which reduces the active power current by 60%, form 100mA to 40 mA. The M2764 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TIEING

Because M2764's are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:
a) the lowest possible memory power dissipation
b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

PROGRAMMING

Caution: exceeding 22V on pin (V_{PP}) will damage the M2764.

When delivered, and after each erasure, all bits of the M2764 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure. The M2764 is in the programming mode when V_{PP} input is at 21V and $\overline{CE}$ is at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

For programming, $\overline{CE}$ should be kept TTL-low at all times while V_{PP} is kept at 21V. When the addresses are stable, a 50ms, active-low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time either individually, sequentially, or at random. The program pulse has a maximum width of 55ms.

FAST PROGRAMMING ALGORITHM

Fast Programming Algorithm rapidly programs M2764 EPROMs using an efficient and reliable method particularly suited to the production programming enviroment. Typical programming times for individual devices are on the order of 1.25 minutes. Programming reliability is also ensured as the incremental program margin of each bytes is continually monitored to determine when it has been successfully programmed. A flowchart of the Fast Programming Algorithm is shown in last page.

The Fast Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial $\overline{CE}$ pulse (s) is one millisecond, which will then be followed by a longer overprogram pulse of length 4X msec (X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular M2764 location), before a correct verify occurs. Up to 15 one-millisecond pulses per byte are provided for before the over program pulse is applied. The entire sequence of program pulses and byte verifications is performed at $V_{CC} = 6.0V$ and $V_{PP} = 21.0V$. When the Fast Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5.0V$.

PROGRAM INHIBIT

Programming of multiple M2764s in parallel with different data is also easily accomplished. Except for $\overline{CE}$ (or $\overline{PGM}$), all like inputs (including $\overline{OE}$) of the parallel M2764s may be common. A TTL low pulse applied to a M2764 $\overline{CE}$ and $\overline{PGM}$ input, with V_{PP} at 21V will program that M2764. A high level $\overline{CE}$ input inhibits the other M2764s from being programmed.
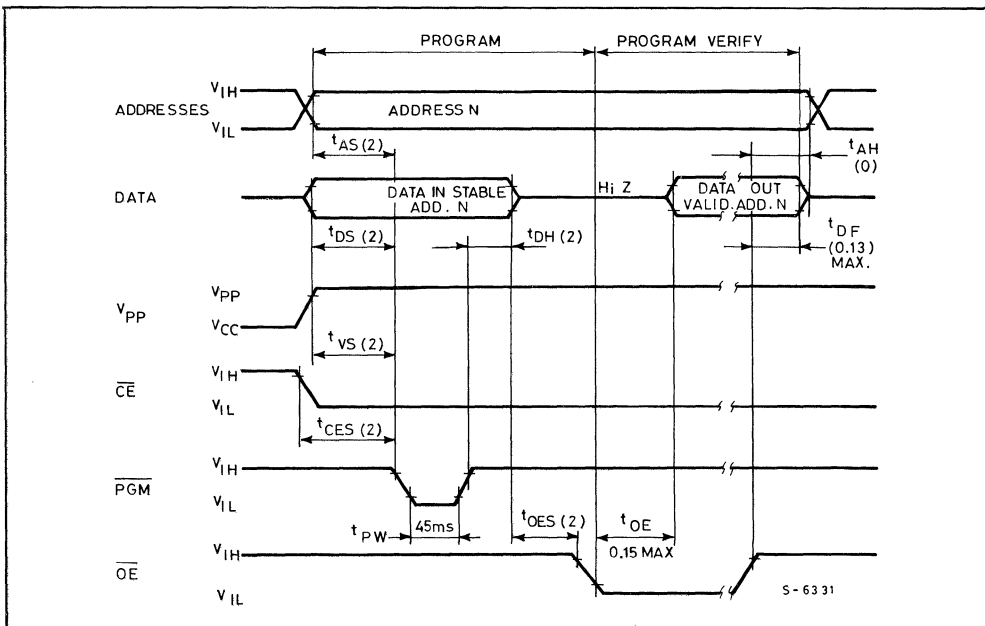
PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{CE}$ and $\overline{OE}$ at V_{IL}. However, $\overline{PGM}$ is at V_{IH}.

ERASURE OPERATION

The erasure characteristic of the M2764 are such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M2764 in approximately 3 years, while it would take approximately 1 week to cause erasure when expose to the direct sunlight. If the M2764 is to be exposed to these type of lighting conditions for extended periods of time, it is suggested that opaque labels to put over the M2764 window to prevent unintentional erasure. The recommended erasure procedure for the M2764 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 μW/cm2 power rating. The M2764 should be placed within 2.5 cm of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

PROGRAMMING WAVEFORMS

PROGRAMMING OPERATION [1]($T_{amb} = 25°C \pm 5°C$, V_{CC}[2] $= 5V \pm 5\%$, V_{PP}[2,3] $= 21V \pm 0.5V$)

DC AND OPERATING CHARACTERISTIC:

Symbol	Parameter	Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}			10	μA
V_{IL}	Input Low Level		-0.1		0.8	V
V_{IH}	Input High Level		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage During Verify	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage During Verify	$I_{OH} = -400 \mu$A	2.4			V
I_{CC2}	V_{CC} Supply Current (Active)				100	mA
I_{PP}	V_{PP} Supply Current	$\overline{CE} = \overline{PGM} = V_{IL}$			30	mA

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions (See note 2)	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Setup Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
$t_{DFP(6)}$	Output Enable Output Float Delay		0		130	ns
t_{VPS}	V_{PP} Setup Time		2			μs
t_{VCS}	V_{CC} Setup Time		2			μs
t_{PW}	Initial Program Pulse Width	(see Note 4)	0.95	1.0	1.05	ms
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width	(see note 5)	3.8		63	ms
t_{OE}	Data Valid from $\overline{OE}$				150	ns

Notes:
1. SGS guarantees the product only if it is programmed to specifications described herein.
2. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The M2764 must not be inserted into or removed from a board with V_{PP} at $21 \pm 0.5V$ or damage may occur to the device.
3. The maximum allowable voltage which may be applied to the V_{PP} pin during progamming is $+22V$. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 22V maximum specification.
4. Initial Program Pulse width tolerance is 1msec $\pm 5\%$.
5. The length of the overprogram pulse may vary from 3.8 msec to 63 msec as a function of the iteration counter value X.
6. This parameter is only sampled and is not 100% tested.
   Output Float is defined as the point where data is no longer driven (see timing diagram).

FAST PROGRAMMING FLOWCHART

START

ADDR-FIRST LOCATION

$V_{CC} = 6V$
$V_{PP} = 21V$

X = 0

PROGRAM ONE 1ms PULSE

INCREMENT X

X = 15? YES

NO

PROGRAM VERIFY ONE BYTE FAIL

PASS

PROGRAM ONE PULSE OF 4X-ms DURATION

X = 15? YES VERIFY BYTE

PASS

NO

INCREMENT ADDR NO LAST ADDR?

DEVICE FAILED FAIL

YES

$V_{CC} = V_{PP} = 5V$

VERIFY ALL BYTES FAIL DEVICE FAILED

PASS

DEVICE PASSED

S- 6880

SGS
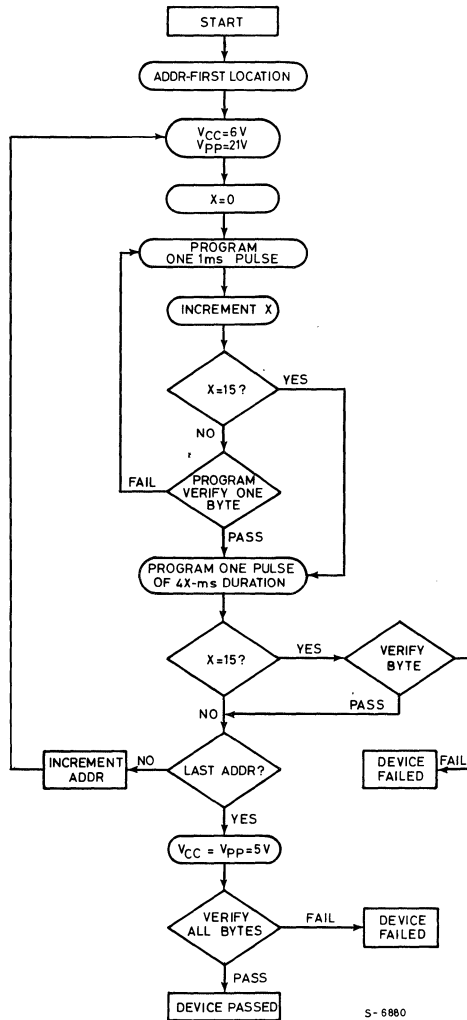
M2764A

64K (8K × 8) UV ERASABLE PROM

- **FAST ACCESS TIME:**
  200ns MAX M2764A-2F1/M2764A-20F1
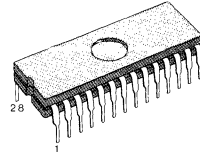 250ns MAX M2764AF1/M2764AF6/M2764A-25F1
  300ns MAX M2764A-3F1/M2764A-30F1
  450ns MAX M2764A-4F1/M2764A-4F6/M2764A-45F1

- 0 to 70°C STANDARD TEMPERATURE RANGE

- −40 to +85°C EXTENDED TEMPERATURE RANGE

- SINGLE +5V POWER SUPPLY

- LOW STANDBY CURRENT (35mA MAX)

- TTL COMPATIBLE

- FAST PROGRAMMING ALGORITHM

- ELECTRONIC SIGNATURE

- ±10% V_{CC} TOLLERANCE AVAILABLE

F
Ceramic Package

ORDERING NUMBERS: M2764A-2F1
M2764AF1
M2764A-3F1
M2764A-4F1

M2764A-20F1
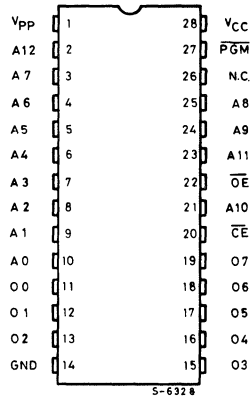M2764A-25F1
M2764A-30F1
M2764A-45F1

M2764AF6
M2764A-4F6

DESCRIPTION

The M2764A is a 65,536-bit ultraviolet erasable and electrically programmable read only memory (EPROM). It is organized as 8,192 words by 8 bits and manufactured using SGS' NMOS-E3 process.

The M2764A with its single +5V power supply and with an access time of 200ns, is ideal for use with high performance +5V microprocessor such as Z8®, Z80® and Z8000™. The M2764A has an important feature which is to separate the output control, Ouput Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminate bus contention in multiple bus microprocessor systems.

The M2764A also features a standby mode which reduces the power dissipation without increasing access time. The active current is 75mA while the maximum standby current is only 35 mA, a 53% saving. The standby mode is achieved by applyng a TTL-high signal to the $\overline{CE}$ input. The M2764A has an "Electronic Signature" that allows programmers to automatically identify device type and pinout. The M2764A is available in a 28-lead dual in-line ceramic package (frit-seal) glass lens.

PIN CONNECTIONS

VPP	1	28	VCC
A12	2	27	$\overline{PGM}$
A7	3	26	N.C.
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	$\overline{OE}$
A2	8	21	A10
A1	9	20	$\overline{CE}$
A0	10	19	O7
O0	11	18	O6
O1	12	17	O5
O2	13	16	O4
GND	14	15	O3

S-6328

PIN NAMES

A0-A12	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE INPUT
$\overline{PGM}$	PROGRAM
N.C.	NO CONNECTION
O0-O7	DATA INPUT/OUTPUT

M2764A

BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Values	Unit
V_I	All Input or Output voltages with respect to ground	+6.5 to −0.6	V
V_{PP}	Supply voltage with respect to ground	+14 to −0,6	V
T_{amb}	Ambient temperature under bias /F1	−10 to +80	°C
	/F6	−50 to +95	°C
T_{stg}	Storage temperature range	−65 to +125	°C
	Voltage on pin 24 with respect to ground	+13.5 to −0.6	V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11-13, 15-19)
READ	V_{IL}	V_{IL}	X	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	X	V_{IH}	V_{CC}	V_{CC}	HIGH Z
STANDBY	V_{IH}	X	X	X	V_{CC}	V_{CC}	HIGH Z
FAST PROGRAMMING	V_{IL}	V_{IH}	X	V_{IL}	V_{PP}	V_{CC}	D_{IN}
VERIFY	V_{IL}	V_{IL}	X	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
PROGRAM INHIBIT	V_{IH}	X	X	X	V_{PP}	V_{CC}	HIGH Z
ELECTRONIC SIGNATURE	V_{IL}	V_{IL}	V_H	V_{IH}	V_{CC}	V_{CC}	CODES

NOTE: X can be V_{IH} or V_{IL} $V_H = 12V \pm 0.5V$

READ OPERATION
DC AND AC CONDITIONS

	F1/ − 2F1 − 3F1/ − 4F1	− 20F1/ − 25F1 − 30F1/ − 45F1	F6/ − 4F6
Operating Temperature Range	0 to 70°C	0 to 70°C	− 40 to 85°C
V_{CC} Power Supply [1,2]	5V ±5%	5V ±10%	5V ±5%
V_{PP} Voltage [2]	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Load Current	$V_{IN} = 5.5V$			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$			10	μA
$I_{PP1(2)}$	V_{PP} Current Read	$V_{PP} = 5.5V$			5	mA
$I_{CC1(2)}$	V_{CC} Current Standby	$\overline{CE} = V_{IH}$			20/35[6]	mA
$I_{CC2(2)}$	V_{CC} Current Active	$\overline{CE} = \overline{OE} = V_{IL}$			60/75[6]	mA
V_{IL}	Input Low Voltage		− 0.1		+ 0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = − 400 \mu A$	2.4			V
$V_{PP(2)}$	V_{PP} Read Voltage	$V_{CC} = 5V ± 0.25V$	3.8		V_{CC}	V

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	2764A-2 2764A-20		2764A-25 / 2764A		2764A-30 / 2764A-3		2764A-45 / 2764A-4		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		200		250		300		450	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		200		250		300		450	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		75		100		120		150	ns
$t_{DF(4)}$	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	55	0	60	0	105	0	130	ns
t_{OH}	Output Hold from Address $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

CAPACITANCE[5] ($T_{amb} = 25°C$, f = 1 MHz)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming.
   The supply current would than be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_{amb} = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and not 100% tested. Output Float is defined as the point where data is no longer driven-see timing diagram.
5. This parameter is only sampled and is not 100% tested.
6. Max: I_{CC} rating differs with access time. Rating of 60mA active and 20mA standby are for M2764A at 200 ns access time only.

AC TEST CONDITIONS
Output Load: 100pF + 1TTL Gate
Input Rise and Fall Times: $\leqslant$ = 20ns
Input Pulse Levels: 0.45 to 2.4V
Timing Measurement Reference Levels: Inputs 0.8 and 2V
Outputs 0.8 and 2V

AC TESTING INPUT/OUTPUT WAVEFORM

AC TESTING LOAD CIRCUIT

CL INCLUDES JIG CAPACITANCE

AC WAVEFORMS

Notes:
1. Typical values are for T_{amb} = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION
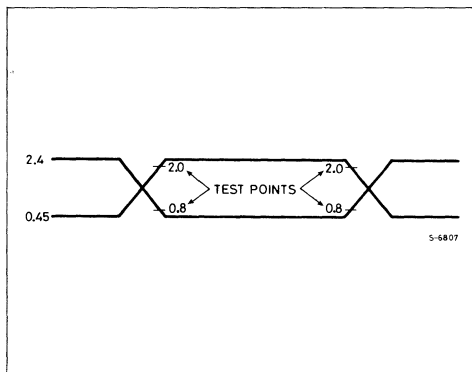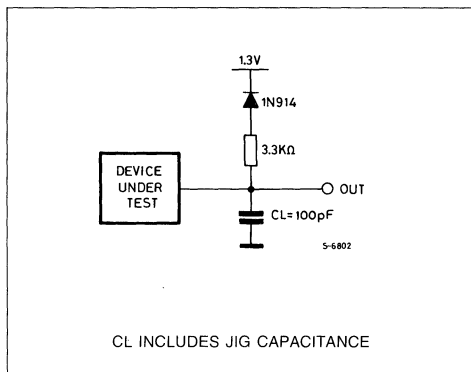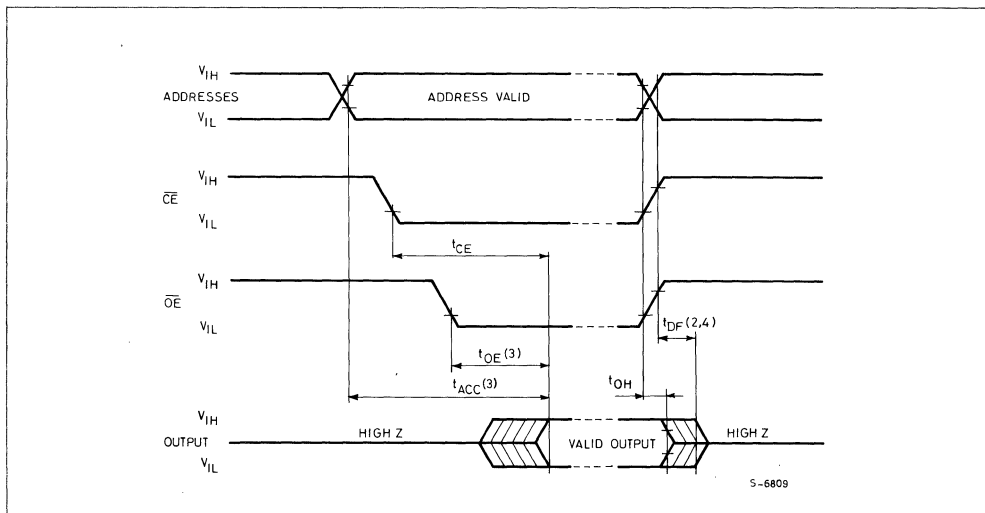
The seven modes of operations of the M2764A are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

READ MODE

The M2764A has two control function, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M2764A has a standby mode which reduces the maximum active power current from 75 mA to 35 mA. The M2764A is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TIEING

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:
a) the lowest possible memory power dissipation
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of NMOS-E3 EPROMs require careful decoupling of the devices the supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of this transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitors should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution: exceeding 14V on pin 1 (V_{PP}) will damage the M2764A.

When delivered, and after each erasure, all bits of the M2764A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure. The M2764A is in the programming mode when V_{PP} input is at 12.5V and $\overline{CE}$ and $\overline{PGM}$ are at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

FAST PROGRAMMING ALGORITHM

Fast Programming Algorithm rapidly programs M2764A EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the

M2764A Fast Programming Algorithm is shown on the last page. The Fast Programming Algorithm utilizes two different pulse types: initial and over-program.

The duration of the initial $\overline{PGM}$ pulse (s) is one millisecond, which will than be followed by a longer overprogram pulse of length 3Xmsec. (X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular M2764A location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are' provided for before the over program pulse is applied. The entire sequence of program pulses and byte verifications is performed at $V_{CC} = 6V$ and $V_{PP} = 12.5V$. When the Fast Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5V$.

PROGRAM INHIBIT

Programming of multiple M2764As in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel M2764A may be common. A TTL low pulse applied to a M2764A's $\overline{CE}$ input, with V_{PP} at 12.5V, will program that M2764A. A high level $\overline{CE}$ input inhibits the other M2764A from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} at 12.5V.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the M2764A. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the M2764A. Two identifier bytes may than be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the SGS M2764A, these two identifier bytes are given below. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (07) defined as the parity bit.

ERASURE OPERATION

The erasure characteristic of the M2764A is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom $\mathring{A}$. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 A range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M2764A in about 3 years, while it would take approximately 1 week to cause erasure when expose to direct sunlight. If the M2764A is to be exposed to these type of lighting conditions for extended periods of time, it is suggested that opaque labels to put over the M2764A window to prevent unintentional erasure. The recommended erasure procedure for the M2764A is exposure to short wave ultraviolet light which has wavelength 2537 $\mathring{A}$. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm2 power rating. The M2764A should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

IDENTIFIER \ PINS	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
Manufacturer code	V_{IL}	0	0	1	0	0	0	0	0	20
Device code	V_{IH}	0	0	0	0	1	0	0	0	08

PROGRAMMING OPERATION ($T_{amb} = 25°C \pm 5°C$, $V_{CC}^{(1)} = 6V \pm 0.25V$, $V_{PP}^{(1)} = 12.5V \pm 0.3V$)

DC AND OPERATING CHARACTERISTIC

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}			10	μA
V_{IL}	Input Low Level (All Inputs)		- 0.1		0.8	V
V_{IH}	Input High Level		2.0		V_{CC}	V
V_{OL}	Output Low Voltage During Verify	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage During Verify	$I_{OH} = - 400 \mu A$	2.4			V
I_{CC2}	V_{CC} Supply Current (Program & Verify)				75	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$			50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5		12.5	V

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Setup Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hodl Time		2			μs
$t_{DFP(4)}$	Output Enable Output Float Delay		0		130	ns
t_{VPS}	V_{PP} Setup Time		2			μs
t_{VCS}	V_{CC} Setup Time		2			μs
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	(see Note 3)	0.95	1.0	1.05	ms
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	(see Note 2)	2.85		78.75	ms
t_{OE}	Data Valid from $\overline{OE}$				150	ns

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of the iteration counter value X.
3. Initial Program Pulse width tolerance is 1msec $\pm 5\%$.
4. This parameter is only sampled and not 100% tested.
   Output Float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING WAFEFORMS

Notes:
1. All times shown in ( ) are minimum and in usec unless otherwise specified.
2. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
3. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
4. When programming the M2764A a 0.1μF capacitor is required across V_{PP} and GROUND to suppress spurious voltage transients which can damage the device.

FAST PROGRAMMING FLOWCHART

START

ADDR-FIRST LOCATION

$V_{CC} = 6 V$
$V_{PP} = 12.5V$

$X = 0$

PROGRAM ONE 1ms PULSE

INCREMENT X

$X = 25$? — YES →

NO ↓

PROGRAM VERIFY ONE BYTE — FAIL

PASS ↓

VERIFY BYTE — FAIL → DEVICE FAILED

PASS ↓

PROGRAM ONE PULSE OF 3X-ms DURATION

LAST ADDR? — NO → INCREMENT ADDR

YES ↓

$V_{CC} = V_{PP} = 5 V$

COMPARE ALL BYTES TO ORIGINAL DATA — FAIL → DEVICE FAILED

PASS ↓

DEVICE PASSED

S-6881

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SGS

M27128A

128K (16K × 8) UV ERASABLE PROM

- FAST ACCESS TIME:
  200ns MAX M27128A-2F1
  250ns MAX M27128AF1/M27128AF6/M27128A-25F1
  300ns MAX M27128A-3F1/M27128A-30F1
  450ns MAX M27128A-4F1/M27128A-4F6/M27128A-45F1

- 0 to 70°C STANDARD TEMPERATURE RANGE

- − 40 to + 85°C EXTENDED TEMPERATURE RANGE

- SINGLE + 5V POWER SUPPLY

- LOW STANDBY CURRENT (40mA MAX)

- TTL COMPATIBLE

- FAST PROGRAMMING ALGORITHM

- ELECTRONIC SIGNATURE

- ± 10% V_{CC} TOLLERANCE AVAILABLE

F
Ceramic Package
ORDERING NUMBERS: M27128A-2F1
M27128AF1
M27128A-3F1
M27128A-4F1

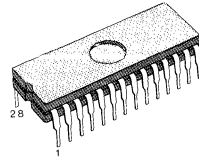M27128A-25F1
M27128A-30F1
M27128A-45F1

M27128AF6
M27128A-4F6

DESCRIPTION

The M27128A is a 131,072-bit ultraviolet erasable and electrically programmable read only memory (EPROM). It is organized as 16,384 words by 8 bits and manufactured using SGS' NMOS-E3 process.

The M27128A with its single + 5V power supply and with an access time of 200ns, is ideal for use with high performance + 5V microprocessor such as Z8®, Z80® and Z8000™. The M27128A has an important feature which is to separate the output control, Output Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminate bus contention in multiple bus microprocessor systems.

The M27128A also features a standby mode which reduces the power dissipation without increasing access time. The active current is 85mA while the maximum standby current is only 40 mA, a 53% saving. The standby mode is achieved by appling a TTL-high signal to the $\overline{CE}$ input. The M27128A has an "Electronic Signature" that allows programmers to automatically identify device type and pinout.

The M27128A is available in a 28-lead dual in-line ceramic package (frit-seal) glass lens.

PIN CONNECTIONS

S-7663

PIN NAMES

A0-A13	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE INPUT
PGM	PROGRAM
O0-O7	DATA INPUT/OUTPUT

BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Values	Unit
V_I	All Input or Output voltages with respect to ground	+ 6.25 to − 0.6	V
V_{PP}	Supply voltage with respect to ground	+ 14 to − 0,6	V
T_{amb}	Ambient temperature under bias /F1	− 10 to + 80	°C
	/F6	− 50 to + 95	°C
T_{stg}	Storage temperature range	− 65 to + 125	°C
	Voltage on pin 24 with respect to ground	+ 13.5 to − 0.6	V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11-13, 15-19)
READ	V_{IL}	V_{IL}	X	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	X	V_{IH}	V_{CC}	V_{CC}	HIGH Z
STANDBY	V_{IH}	X	X	X	V_{CC}	V_{CC}	HIGH Z
FAST PROGRAMMING	V_{IL}	V_{IH}	X	V_{IL}	V_{PP}	V_{CC}	D_{IN}
VERIFY	V_{IL}	V_{IL}	X	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
PROGRAM INHIBIT	V_{IH}	X	X	X	V_{PP}	V_{CC}	HIGH Z
ELECTRONIC SIGNATURE	V_{IL}	V_{IL}	V_H	V_{IH}	V_{CC}	V_{CC}	CODES

NOTE: X can be V_{IH} or V_{IL} $V_H = 12V \pm 0.5V$

READ OPERATION
DC AND AC CONDITIONS

	F1/ - 2F1/ - 3F1/ - 4F1	- 25F1/ - 30F1/ - 45F1	F6/ - 4F6
Operating Temperature Range	0 to 70°C	0 to 70°C	- 40 to 85°C
V_{CC} Power Supply [1,2]	5V ±5%	5V ±10%	5V ±5%
V_{PP} Voltage [2]	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ. [3]	Max.	
I_{LI}	Input Load Current	$V_{IN} = 5.5V$			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$			10	μA
$I_{PP1(2)}$	V_{PP} Current Read Standby	$V_{PP} = 5.5V$			5	mA
$I_{CC1(2)}$	V_{CC} Current Standby	$\overline{CE} = V_{IH}$			40	mA
$I_{CC2(2)}$	V_{CC} Current Active	$\overline{CE} = \overline{OE} = V_{IL}$ $V_{PP} = V_{CC}$			85	mA
V_{IL}	Input Low Voltage		- 0.1		+ 0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = - 400 \mu A$	2.4			V
$V_{PP(2)}$	V_{PP} Read Voltage	$V_{CC} = 5V \pm 0.25V$	3.8		V_{CC}	V

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	27128A-2		27128A-25 / 27128		27128A-30 / 27128A-3		27128A-45 / 27128A-4		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		200		250		300		450	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		200		250		300		450	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		75		100		120		150	ns
$t_{DF(4)}$	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	55	0	60	0	105	0	130	ns
t_{OH}	Output Hold from Address CE or OE Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

CAPACITANCE[5] ($T_{amb} = 25°C$, f = 1 MHz)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would than be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_{amb} = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and not 100% tested. Output Float is defined as the point where data is no longer driven. (See timing diagram).
5. This parameter is only sampled and is not 100% tested.

AC TEST CONDITIONS
Output Load: 100pF + 1TTL Gate
Input Rise and Fall Times: $\leqslant$ = 20ns
Input Pulse Levels: 0.45 to 2.4V
Timing Measurement Reference Levels: Inputs   0.8 and 2V
Outputs 0.8 and 2V

AC TESTING INPUT/OUTPUT WAVEFORM

AC TESTING LOAD CIRCUIT

CL INCLUDES JIG CAPACITANCE

AC WAVEFORMS

Notes:
1. Typical values are for T_{amb} = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The seven modes of operations of the M27128A are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

READ MODE

The M27128A has two control function, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M27128A has a standby mode which reduces the maximum active power current from 85 mA to 40 mA. The M27128A is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TIEING

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:
a) the lowest possible memory power dissipation
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of NMOS-E3 EPROMs require careful decoupling of the devices the supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of this transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitors should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution: exceeding 13V on pin 1 (V_{PP}) will damage the M27128A.

When delivered, and after each erasure, all bits of the M27128A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure. The M27128A is in the programming mode when V_{PP} input is at 12.5V and $\overline{CE}$ and $\overline{PGM}$ are at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

FAST PROGRAMMING ALGORITHM

Fast Programming Algorithm rapidly programs M27128A EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each bytes is continually monitored to determine when it has been successfully programmed. A flowchart of the

M27128A

M27128A Fast Programming Algorithm is shown on the last page. The Fast Programming Algorithm utilizes two different pulse types: initial and over-program.

The duration of the initial $\overline{PGM}$ pulse (s) is one millisecond, which will than be followed by a longer overprogram pulse of length 3Xmsec. (X is an itera-tion counter and is equal to the number of the in-itial one millisecond pulses applied to a particular M27128A location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are pro-vided for before the over program pulse is applied. The entire sequence of program pulses and byte verifications is performed at $V_{CC} = 6V$ and $V_{PP} = 12.5V$. When the Fast Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5V$.

PROGRAM INHIBIT
Programming of multiple M27128As in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel M27128A may be common. A TTL low pulse ap-plied to a M27128A's $\overline{CE}$ input, with V_{PP} at 12.5V, will program that M27128A. A high level $\overline{CE}$ input inhibits the other M27128A from being pro-grammed.

PROGRAM VERIFY
A verify should be performed on the programmed bits to determine that they were correctly pro-grammed. The verify is accomplished with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} at 12.5V.

ELECTRONIC SIGNATURE
The Electronic Signature mode allows the reading out of a binary code from an EPROM that will iden-tify its manufacturer and type. This mode is intend-ed for use by programming equipment for the pur-pose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the M27128A. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the M27128A. Two identifier bytes may than be se-quenced from the device outputs by toggling ad-dress line A0 (pin 10) from V_{IL} to V_{IH}. All other ad-dress lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the SGS M27128A, these two identifier bytes are given below. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (07) defined as the parity bit.

ERASURE OPERATION
The erasure characteristic of the M27128A is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom $\overset{\circ}{A}$. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 A range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M27128A in about 3 years, while it would take approximately 1 week to cause erasure when expose to direct sunlight. If the M27128A is to be exposed to these type of lighting conditions for extended periods of time, it is suggested that opaque labels to put over the M27128A window to prevent unintentional erasure. The recommended erasure procedure for the M27128A is exposure to short wave ultraviolet light which has wavelength 2537 $\overset{\circ}{A}$. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm2 power rating. The M27128A should be placed within 2.5 cm (1 inch) of the lamp tubes dur-ing the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

IDENTIFIER	PINS A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
Manufacturer code	V_{IL}	0	0	1	0	0	0	0	0	20
Device code	V_{IH}	1	0	0	0	1	0	0	0	89

PROGRAMMING OPERATION $(T_{amb} = 25°C \pm 5°C, V_{CC}^{(1)} = 6V \pm 0.25V, V_{PP}^{(1)} = 12.5V \pm 0.3V)$

DC AND OPERATING CHARACTERISTIC

Symbol	Parameter	Test Conditions (See note 1)	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}			10	μA
V_{IL}	Input Low Level (All Inputs)		-0.1		0.8	V
V_{IH}	Input High Level		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage During Verify	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage During Verify	$I_{OH} = -400 \mu A$	2.4			V
I_{CC2}	V_{CC} Supply Current (Program & Verify)				100	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$			50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5		12.5	V

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions (See note 1)	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Setup Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
$t_{DFP(4)}$	Output Enable Output Float Delay		0		130	ns
t_{VPS}	V_{PP} Setup Time		2			μs
t_{VCS}	V_{CC} Setup Time		2			μs
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	(see Note 3)	0.95	1.0	1.05	ms
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	(see Note 2)	2.85		78.75	ms
t_{OE}	Data Valid from $\overline{OE}$				150	ns

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of the iteration counter value X.
3. Initial Program Pulse width tolerance is 1msec $\pm 5\%$.
4. This parameter is only sampled and not 100% tested.
   Output Float is defined as the point where data is no longer driven (see timing diagram).

M27128A

PROGRAMMING WAFEFORMS
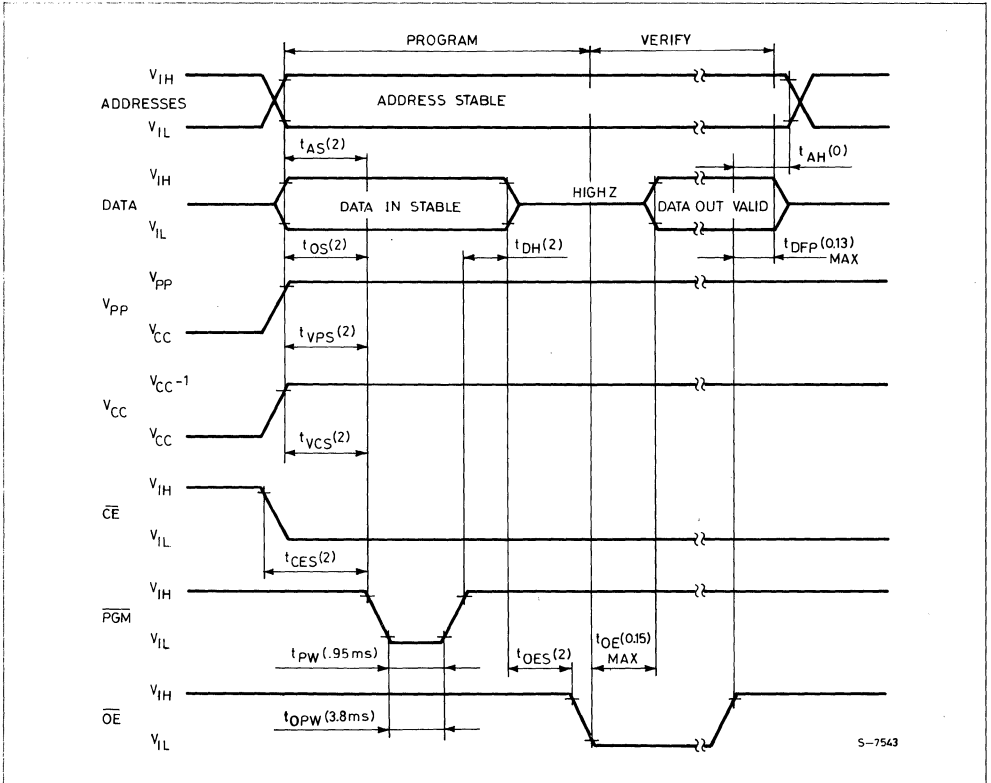
Notes:
1. All times shown in ( ) are minimum and in usec unless otherwise specified.
2. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
3. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
4. When programming the M27128A a 0.1μF capacitor is required across V_{PP} and GROUND to suppress spurious voltage transients which can damage the device.

FAST PROGRAMMING FLOWCHART

START

ADDR-FIRST LOCATION

$V_{CC} = 6 V$
$V_{PP} = 12.5 V$

$X = 0$

PROGRAM
ONE 1ms PULSE

INCREMENT X

$X = 25$?

YES

NO

PROGRAM
VERIFY ONE
BYTE

FAIL

VERIFY
BYTE

FAIL

DEVICE
FAILED

PASS

PASS

PROGRAM ONE PULSE
OF 3X-ms DURATION

INCREMENT
ADDR

NO

LAST ADDR?

YES

$V_{CC} = V_{PP} = 5 V$

COMPARE
ALL BYTES
TO ORIGINAL
DATA

FAIL

DEVICE
FAILED

PASS

DEVICE PASSED

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79
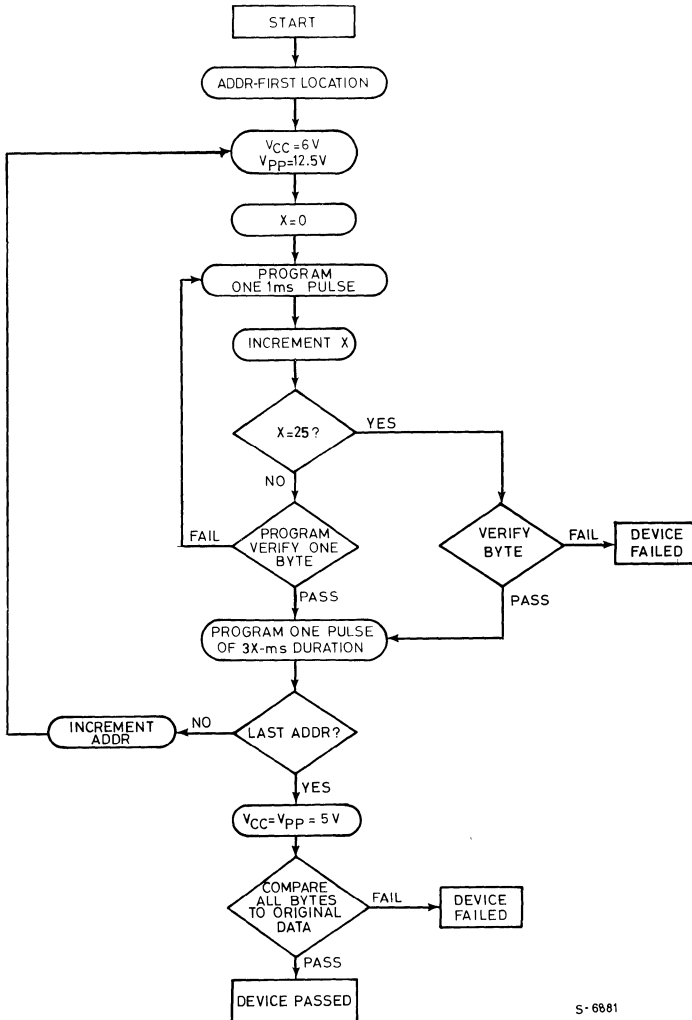
M27256

256K (32K × 8) UV ERASABLE PROM

- FAST ACCESS TIME:
  200ns MAX M27256-2F1
  250ns MAX M27256F1/M27256F6/M27256-25F1
  300ns MAX M27256-3F1/M27256-30F1
  450ns MAX M27256-4F1/M27256-4F6/M27256-45F1
- 0 to 70°C STANDARD TEMPERATURE RANGE
- − 40 to +85°C EXTENDED TEMPERATURE RANGE
- SINGLE +5V POWER SUPPLY
- LOW STANDBY CURRENT (40mA MAX)
- TTL COMPATIBLE
- ±10% V_{CC} TOLERANCE AVAILABLE

F
Ceramic Package
ORDERING NUMBERS: M27256-2F1
M27256F1
M27256-3F1
M27256-4F1

M27256-25F1
M27256-30F1
M27256-45F1

M27256F6
M27256-4F6

DESCRIPTION

The M27256 is a 262,144-bit ultraviolet erasable and electrically programmable read only memory (EPROM). It is organized as 32.768 words by 8 bits and manufactured using SGS' NMOS-E3 process. The M27256 with its single +5V power supply and with an access time of 200ns, is ideal for use with high performance +5V microprocessor such as Z8®, Z80® and Z8000™. The M27256 has an important feature which is to separate the output control, Ouptut Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminate bus contention in multiple bus microprocessor systems.

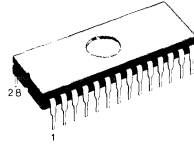The M27256 also features a standby mode which reduces the power dissipation without increasing access time. The active current is 100mA while the maximum standby current is only 40 mA, a 60% saving. The standby mode is achieved by appling a TTL-high signal to the $\overline{CE}$ input. The M27256 enables implementation of new, advanced systems with firmware intensive architectures.

The combination of the M27256's high density, and new advanced microprocessors having megabit addressing capability provides designers with opportunities to engineer user-friendly, high reliability, high-performance systems. The M27256 large storage capability enables it to function as a high density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a M27256 directly on a system's memory bus. This permits immediate microprocessor access and execution of software and eliminates the need for time consuming disk accesses and downloads. The M27256 has an "Electronic Signature" that allows programmers to automatically identify device type and pinout.

PIN CONNECTIONS

V_{PP}	1	28	V_{CC}
A12	2	27	A14
A7	3	26	A13
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	$\overline{OE}$
A2	8	21	A10
A1	9	20	$\overline{CE}$
A0	10	19	O7
O0	11	18	O6
O1	12	17	O5
O2	13	16	O4
GND	14	15	O3

S - 7576

PIN NAMES

A0-A14	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE INPUT
O0-O7	DATA INPUT/OUTPUT

BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	All Input or Output voltages with respect to ground	+ 6.25 to − 0.6	V
V_{PP}	Supply voltage with respect to ground	+ 14 to − 0,6	V
T_{amb}	Ambient temperature under bias /F1	− 10 to + 80	°C
	/F6	− 50 to + 95	°C
T_{stg}	Storage temperature range	− 65 to + 125	°C
	Voltage on pin 24 with respect to ground	+ 13.5 to − 0.6	V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE / PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	A0 (10)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11-13, 15-19)
READ	V_{IL}	V_{IL}	X	X	V_{CC}	V_{CC}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	X	X	V_{CC}	V_{CC}	HIGH Z
STANDBY	V_{IH}	X	X	X	V_{CC}	V_{CC}	HIGH Z
PROGRAM	V_{IL}	V_{IH}	X	X	V_{PP}	V_{CC}	D_{IN}
VERIFY	V_{IH}	V_{IL}	X	X	V_{PP}	V_{CC}	D_{OUT}
OPTIONAL VERIFY	V_{IL}	V_{IL}	X	X	V_{PP}	V_{CC}	D_{OUT}
PROGRAM INHIBIT	V_{IH}	V_{IH}	X	X	V_{PP}	V_{CC}	HIGH Z
ELECTRONIC SIGNATURE	V_{IL}	V_{IL}	V_H	V_{IL}	V_{CC}	V_{CC}	MAN.CODES
	V_{IL}	V_{IL}	V_H	V_{IH}	V_{CC}	V_{CC}	DEV.CODE

NOTE: X can be V_{IH} or V_{IL} $V_H = 12V \pm 0.5V$

READ OPERATION
DC AND AC CONDITIONS

	F1/ – 2F1 – 3F1/ – 4F1	– 25F1/ – 30F1/ – 45F1	F6/ – 4F6
Operating Temperature Range	0 to 70°C	0 to 70°C	– 40 to 85°C
V_{CC} Power Supply [1,2]	5V ±5%	5V ±10%	5V ±5%
V_{PP} Voltage [2]	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ. [3]	Max.	
I_{LI}	Input Load Current	$V_{IN} = 5.5V$			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$			10	μA
$I_{PP1(2)}$	V_{PP} Current Read Standby	$V_{PP} = 5.5V$			5	mA
$I_{CC1(2)}$	V_{CC} Current Standby	$\overline{CE} = V_{IH}$		20	40	mA
$I_{CC2(2)}$	V_{CC} Current Active	$\overline{CE} = \overline{OE} = V_{IL}$ $V_{PP} = V_{CC}$		45	100	mA
V_{IL}	Input Low Voltage		– 0.1		+ 0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = – 400$ μA	2.4			V
$V_{PP(2)}$	V_{PP} Read Voltage	$V_{CC} = 5V ± 0.25V$	3.8		V_{CC}	V

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	27256-2		27256-25 / 27256		27256-30 / 27256-3		27256-45 / 27256-4		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		200		250		300		450	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		200		250		300		450	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		75		100		120		150	ns
$t_{DF(4)}$	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	55	0	60	0	105	0	130	ns
t_{OH}	Output Hold from Address $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

CAPACITANCE[5] ($T_{amb} = 25°C$, f = 1 MHz)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would than be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_{amb} = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and not 100% tested. Output Float is defined as the point where data is no longer driven-see timing diagram.
5. This parameter is only sampled and not 100% tested.

AC TEST CONDITIONS
Output Load: 100pF + 1TTL Gate
Input Rise and Fall Times: $\leqslant$ = 20ns
Input Pulse Levels: 0.45 to 2.4V
Timing Measurement Reference Levels: Inputs   0.8 and 2V
                                      Outputs 0.8 and 2V

AC TESTING INPUT/OUTPUT WAVEFORM

2.4
2.0   2.0
TEST POINTS
0.8   0.8
0.45

S-6807

AC TESTING LOAD CIRCUIT

1.3V

1N914

3.3KΩ

DEVICE
UNDER   O OUT
TEST
CL = 100pF

S-6802

CL INCLUDES JIG CAPACITANCE

AC WAVEFORMS

V_{IH}
ADDRESSES   ADDRESS VALID
V_{IL}

V_{IH}
$\overline{CE}$
V_{IL}
t_{CE}

V_{IH}
$\overline{OE}$
V_{IL}
$t_{DF}(2,4)$

$t_{OE}(3)$
$t_{ACC}(3)$ t_{OH}

V_{IH}
OUTPUT   HIGH Z   VALID OUTPUT   HIGH Z
V_{IL}

S-6809

Notes:
1. Typical values are for T_{amb} = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The eight modes of operations of the M27256 are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

READ MODE

The M27256 has two control function, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

STANDBY MODE

The M27256 has a standby mode which reduces the maximum active power current from 100 mA to 40 mA. The M27256 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:
a) the lowest possible memory power dissipation
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of NMOS-E3 EPROMs require careful decoupling of the devices the supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of this transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitors should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution: exceeding 13V on pin 1 (V_{PP}) will damage the M27256.

When delivered, and after each erasure, all bits of the M27256 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure. The M27256 is in the programming mode when V_{PP} input is at 12.5V and $\overline{CE}$ and is at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

FAST PROGRAMMING ALGORITHM

Fast Programming Algorithm rapidly programs M27256 EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each bytes is continually monitored to determine when it has been successfully programmed. A flowchart of the M27256 Fast Programming Algorithm is shown on the last page. The Fast Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial $\overline{CE}$ pulse (s) is one millisecond, which will than be followed by a

longer overprogram pulse of length 3Xmsec. (X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular M27256 location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied. The entire sequence of program pulses and byte verifications is performed at $V_{CC} = 6V$ and $V_{PP} = 12.5V$. When the Fast Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5V$.

PROGRAM INHIBIT

Programming of multiple M27256s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel M27256 may be common. A TTL low pulse applied to a M27256's $\overline{CE}$ input, with V_{PP} at 12.5V, will program that M27256. A high level $\overline{CE}$ input inhibits the other M27256s from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IH} and V_{PP} at 12.5V.

OPTIONAL VERIFY

The optional verify may be performed instead of the verify mode. It is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL} (as opposed to the standard verify which has $\overline{CE}$ at V_{IH}), and V_{PP} at 12.5V. The outputs will three-state according to the signal presented to $\overline{OE}$. Therefore, all devices with $V_{PP} = 12.5V$ and $\overline{OE} = V_{IL}$ will present data on the bus independent of the $\overline{CE}$ state. When parallel programming several devices which share the common bus, V_{PP} should be lowered to V_{CC} (= 6V) and the normal read mode used to execute a program verify.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the pur-

pose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27256. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the M27256. Two identifier bytes may than be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the SGS M27256, these two identifier bytes are given below. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (07) defined as the parity bit.

ERASURE OPERATION

The erasure characteristic of the M27256 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 A range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M27256 in about 3 years, while it would take approximately 1 week to cause erasure when expose to direct sunlight. If the M27256 is to be exposed to these type of lighting conditions for extended periods of time, it is suggested that opaque labels to put over the M27256 window to prevent unintentional erasure. The recommended erasure procedure for the M27256 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 μW/cm² power rating. The M27256 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

PINS / IDENTIFIER	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
Manufacturer code	V_{IL}	0	0	1	0	0	0	0	0	20
Device code	V_{IH}	0	0	0	0	0	1	0	0	04

PROGRAMMING OPERATION ($T_{amb} = 25°C \pm 5°C$, $V_{CC}^{(1)} = 6V \pm 0.25V$, $V_{PP}^{(1)} = 12.5V \pm 0.3V$

DC AND OPERATING CHARACTERISTIC:

Symbol	Parameter	Test Conditions (See note 1)	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}			10	μA
V_{IL}	Input Low Level (All Inputs)		-0.1		0.8	V
V_{IH}	Input High Level		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage During Verify	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage During Verify	$I_{OH} = -400 \mu A$	2.4			V
I_{CC2}	V_{CC} Supply Current (Program & Verify)				100	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$			50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5		12.5	V

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions (See note 1)	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Setup Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hodl Time		2			μs
$t_{DFP(4)}$	Output Enable Output Float Delay		0		130	ns
t_{VPS}	V_{PP} Setup Time		2			μs
t_{VCS}	V_{CC} Setup Time		2			μs
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	(see Note 3)	0.95	1.0	1.05	ms
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width	(see Note 2)	2.85		78.75	ms
t_{OE}	Data Valid from $\overline{OE}$				150	ns

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of the iteration counter value X.
3. Initial Program Pulse width tolerance is 1msec $\pm 5\%$.
4. This parameter is only sampled and not 100% tested.
   Output Float is defined as the point where data is no longer driven (see timing diagram).

M27256

PROGRAMMING WAFEFORMS
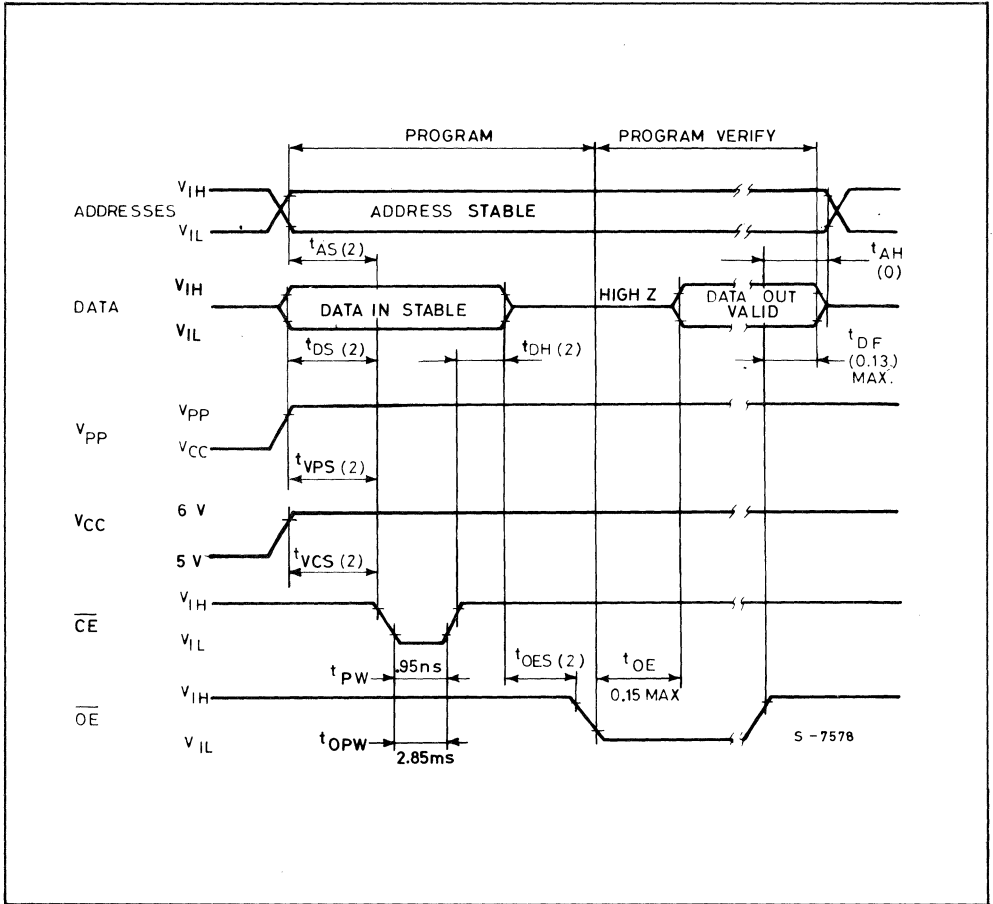
Notes:
1. All times shown in ( ) are minimum and in usec unless otherwise specified
2. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}
3. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
4. When programming the M27256 a $0.1 \mu F$ capacitor is required across V_{PP} and GROUND to suppress spurious voltage transients which can damage the device.

FAST PROGRAMMING FLOWCHART

```
                    ┌──────────┐
                    │  START   │
                    └──────────┘
                         │
                  ╭──────────────╮
                  │ ADDR-FIRST LOCATION │
                  ╰──────────────╯
                         │
                  ╭──────────────╮
                  │  VCC = 6 V   │
                  │  VPP=12.5V   │
                  ╰──────────────╯
                         │
                  ╭──────────────╮
                  │   X = 0      │
                  ╰──────────────╯
                         │
                  ╭──────────────╮
                  │  PROGRAM     │
                  │ ONE 1ms PULSE│
                  ╰──────────────╯
                         │
                  ╭──────────────╮
                  │ INCREMENT X  │
                  ╰──────────────╯
                         │
                      ◇ X=25? ◇ ──YES──┐
                         │ NO           │
                  ╭──────────────╮      │
       FAIL ──────│  PROGRAM     │   ◇ VERIFY ◇ ──FAIL── ┌──────────┐
                  │ VERIFY ONE   │     BYTE               │ DEVICE   │
                  │   BYTE       │      │                 │ FAILED   │
                  ╰──────────────╯     PASS               └──────────┘
                         │ PASS         │
                  ╭──────────────╮      │
                  │ PROGRAM ONE PULSE │ │
                  │ OF 3X-ms DURATION │─┘
                  ╰──────────────╯
                         │
   ╭──────────╮  NO   ◇ LAST ADDR? ◇
   │ INCREMENT │◄─────
   │   ADDR    │        │ YES
   ╰──────────╯   ╭──────────────╮
                  │ VCC=VPP = 5 V│
                  ╰──────────────╯
                         │
                      ◇ COMPARE
                       ALL BYTES ◇ ──FAIL── ┌──────────┐
                      TO ORIGINAL           │ DEVICE   │
                        DATA                │ FAILED   │
                         │ PASS             └──────────┘
                  ┌──────────────┐
                  │ DEVICE PASSED│        S-6881
                  └──────────────┘
```
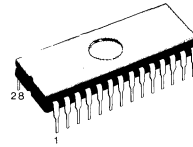
89

M27512

512K (64K × 8) UV ERASABLE EPROM

- FAST ACCESS TIME:
  250ns MAX M27512F1
- 0 TO 70°C STANDARD TEMPERATURE RANGE
- SINGLE +5V POWER SUPPLY
- LOW STANDBY CURRENT (40mA MAX)
- TTL COMPATIBLE
- FAST PROGRAMMING
- ELECTRONIC SIGNATURE

F
Ceramic Package
ORDERING NUMBERS: M27512F1
M27512-3F1
M27512-25F1
M27512-30F1

DESCRIPTION

The M27512 is a 524,288-bit ultraviolet erasable and electrically programmable read only memory (EPROM). It is organized as 65,536 words by 8 bits and manufactured using SGS' NMOS-E3 process. The M27512 with its single +5V power supply and with an access time of 250ns, is ideal for use with high performance +5V microprocessor allowing full speed operation without the addition of performance-degrading WAIT states. The M27512 has an important feature which is to separate the output control, Output Enable ($\overline{OE}/V_{PP}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}/V_{PP}$ control eliminate bus contention in multiple bus microprocessor systems. The M27512 also features a standby mode which reduces the power dissipation without increasing access time. The active current is 125mA while the maximum standby current is only 40 mA, a 70% saving. The standby mode is achieved by applyng a TTL-high signal to the $\overline{CE}$ input. The M27512 enables implementation of new, advanced systems with firmware intensive architectures.
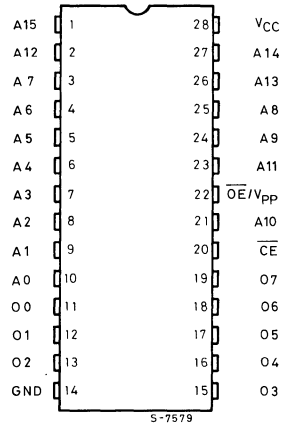
The combination of the M27512s high density, and new advanced microprocessors having megabit addressing capability provides designers with opportunities to engineer user-friendly, high reliability, high-performance systems. The M27512 large storage capability enables it to function as a high density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a M27512 directly on a system's memory bus. This permits immediate microprocessor access and execution of software and eliminates the need for time consuming disk accesses and downloads. The M27512 has an "Electronic Signature" that allows programmers to automatically identify device type and pinout. The M27512 is available in a 28-lead dual in-line ceramic package glass lens (frit seal).

PIN CONNECTIONS

A15	1		28	V_{CC}
A12	2		27	A14
A7	3		26	A13
A6	4		25	A8
A5	5		24	A9
A4	6		23	A11
A3	7		22	$\overline{OE}/V_{PP}$
A2	8		21	A10
A1	9		20	$\overline{CE}$
A0	10		19	O7
O0	11		18	O6
O1	12		17	O5
O2	13		16	O4
GND	14		15	O3

S-7579

PIN NAMES

A0-A15	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}/V_{PP}$	OUTPUT ENABLE/V_{PP} INPUT
O0-O7	DATA INPUT/OUTPUT

BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	All Input or Output voltages with respect to ground	+ 6.5 to − 0.6	V
V_{PP}	Supply voltage with respect to ground	+14 to − 0.6	V
T_{amb}	Ambient temperature under bias	−10 to + 80	°C
T_{stg}	Storage temperature range	− 65 to +125	°C
	Voltage on pin 24 with respect to ground	+ 13.5 to −0.6	V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	A9 (24)	A0 (10)	V_{CC} (28)	OUTPUTS (11-13, 15-19)
READ	V_{IL}	V_{IL}	X	X	V_{CC}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	X	X	V_{CC}	HIGH Z
STANDBY	V_{IH}	X	X	X	V_{CC}	HIGH Z
PROGRAM	V_{IL}	V_{PP}	X	X	V_{CC}	D_{IN}
PROGRAM INHIBIT	V_{IH}	V_{PP}	X	X	V_{CC}	HIGH Z
ELECTRONIC SIGNATURE	V_{IL}	V_{IL}	V_H	V_{IL}	V_{CC}	MAN.CODE
	V_{IL}	V_{IL}	V_H	V_{IH}	V_{CC}	DEV.CODE

NOTE: X can be V_{IH} or V_{IL} $V_H = 12V \pm 0.5V$

READ OPERATION
DC AND AC OPERATING CONDITIONS

	F1/-3F1	– 25F1/ – 30F1
Operating Temperature Range	0 to 70°C	0 to 70°C
V_{CC} Power Supply [1]	5V ± 5%	5V ± 10%

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ. [2]	Max.	
I_{LI}	Input Load Current	$V_{IN} = 5.5V$			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$			10	μA
I_{CC1}	V_{CC} Current Standby	$\overline{CE} = V_{IH}$		20	40	mA
I_{CC2}	V_{CC} Current Active	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$		90	125	mA
V_{IL}	Input Low Voltage		– 0.1		+ 0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = - 400 \mu A$	2.4			V

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	27512-25/ 27512		27512-30/ 27512-3		Unit
			Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}/V_{PP} = V_{IL}$		250		300	ns
t_{OE}	$\overline{OE}/V_{PP}$ to Output Delay	$\overline{CE} = V_{IL}$		100		120	ns
$t_{DF(3)}$	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	60	0	105	ns
t_{OH}	Output Hold from Address $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$	0		0		ns

CAPACITANCE[4] ($T_{amb} = 25°C$, f = 1 MHz)

Symbol	Parameter	Test Conditions	Min.	Typ. [2]	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

Notes:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. Typical values are for $T_{amb} = 25°C$ and nominal supply voltages.
3. This parameter is only sampled and not 100% tested. Output Float is defined as the point where data is no longer driven-see timing diagram.
4. This parameter is only sampled and not 100% tested.
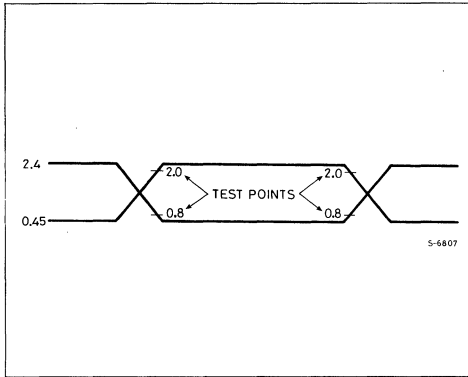
M27512

AC TEST CONDITIONS
Output Load: 100pF + 1TTL Gate
Input Rise and Fall Times: $\leqslant$ = 20ns
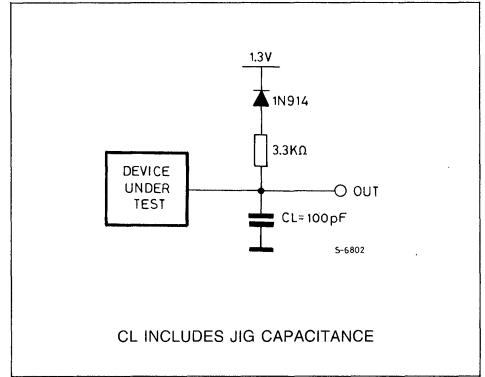Input Pulse Levels: 0.45 to 2.4V
Timing Measurement Reference Levels: Inputs   0.8 and 2V
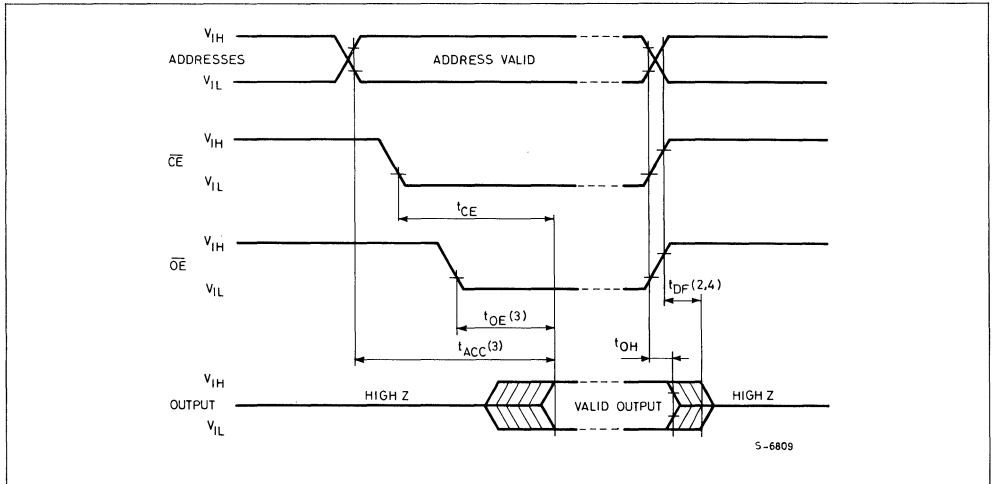   Outputs 0.8 and 2V

AC TESTING INPUT/OUTPUT WAVEFORM

AC TESTING LOAD CIRCUIT

CL INCLUDES JIG CAPACITANCE

AC WAVEFORMS

Notes: 1. Typical values are for T_{amb} = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}/V_{PP}$ may be delayed up to t_{CE} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}/V_{PP}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The six modes of operations of the M27512 are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ and 12V on A9 for Electronic Signature.

READ MODE

The M27512 has two control function, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}/V_{PP}$) is the output control and should be used to gate data from to the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after delay at t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M27512 has a standby mode which reduces the maximum active power current from 125 mA to 40 mA. The M27512 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}/V_{PP}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:
a) the lowest possible memory power dissipation
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}/V_{PP}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of NMOS-E3 EPROMs require careful decoupling of the devices the supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of this transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitors should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution: exceeding 14V on pin 22 ($\overline{OE}/V_{PP}$) will permanently damage the M27512.

When delivered, and after each erasure, all bits of the M27512 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure. The M27512 is in the programming mode when $\overline{OE}/V_{PP}$ input is at 12.5V and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

FAST PROGRAMMING ALGORITHM

Fast Programming Algorithm rapidly programs M27512 EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each bytes is continually monitored to determine when it has been successfully programmed. A flowchart of the

M27512 Fast Programming Algorithm is shown on last page. The Fast Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial $\overline{CE}$ pulse (s) is one millisecond, which will than be followed by a longer overprogram pulse of length 3X msec. (X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular M27512 location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied. The entire sequence of program pulses and byte verifications is performed at $V_{CC} = 6V$ and $\overline{OE}/V_{PP} = 12.5V$. When the Fast Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = 5V$.

PROGRAM INHIBIT
Programming of multiple M27512s in parallel with different data is also easily accomplished. Except for $\overline{CE}$ and $\overline{OE}/V_{PP}$ all inputs of the parallel M27512 may be common. A TTL low level pulse applied to a M27512's $\overline{CE}$ input, with $\overline{OE}/V_{PP}$ at 12.5V, will program that M27512. A high level $\overline{CE}$ input inhibits the other M27512s from being programmed.

PROGRAM VERIFY
A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

ELECTRONIC SIGNATURE
The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming

algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27512. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the M27512. Two identifier bytes may than be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode, except for A14 and A15 which should be held high. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the SGS M27512, these two identifier bytes are given here below. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (07) defined as the parity bit.

ERASURE OPERATION
The erasure characteristic of the M27512 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 A range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M27512 in about 3 years, while it would take approximately 1 week to cause erasure when expose to direct sunlight. If the M27512 is to be exposed to these type of lighting conditions for extended periods of time, it is suggested that opaque labels to put over the M27512 window to prevent unintentional erasure. The recommended erasure procedure for the M27512 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm² power rating. The M27512 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

PINS / IDENTIFIER	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
Manufacturer code	V_{IL}	0	0	1	0	0	0	0	0	20
Device code	V_{IH}	0	0	0	0	1	1	0	1	0D

Note: A9 = 12V ± 0.5V; A1-A8, A10-A13, $\overline{CE}$, $\overline{OE}/V_{PP} = V_{IL}$; A14, A15 = V_{IH}

PROGRAMMING OPERATION ($T_{amb} = 25°C \pm 5°C$, $V_{CC}^{(1)} = 6V \pm 0.25V$, $\overline{OE}/V_{PP}^{(1)} = 12.5V \pm 0.5V$)

DC AND OPERATING CHARACTERISTIC:

Symbol	Parameter	Test Conditions (See note 1)	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}			10	μA
V_{IL}	Input Low Level (All Inputs)		-0.1		0.8	V
V_{IH}	Input High Level		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage During Verify	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage During Verify	$I_{OH} = -400 \mu A$	2.4			V
I_{CC2}	V_{CC} Supply Current				150	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$			50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5		12.5	V

AC CHARACTERISTICS

| Symbol	Parameter	Test Conditions (See note 1)	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Setup Time		2			μs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time		2			μs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
$t_{DFP(4)}$	Output Enable Output Float Delay		0		130	ns
t_{VCS}	V_{CC} Setup Time		0			μs
$t_{PW(3)}$	$\overline{CE}$ Initial Program Pulse Width		0.95	1.0	1.05	ms
$t_{OPW(2)}$	$\overline{CE}$ Overprogram Pulse Width		2.85		78.75	ms
t_{DV}	Data Valid from $\overline{CE}$				1	ns
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2			μs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50			ns

Notes:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of the iteration counter value X.
3. Initial Program Pulse width tolerance is 1msec $\pm 5\%$.
4. This parameter is only sampled and not 100% tested.
   Output Float is defined as the point where data is no longer driven (see timing diagram).
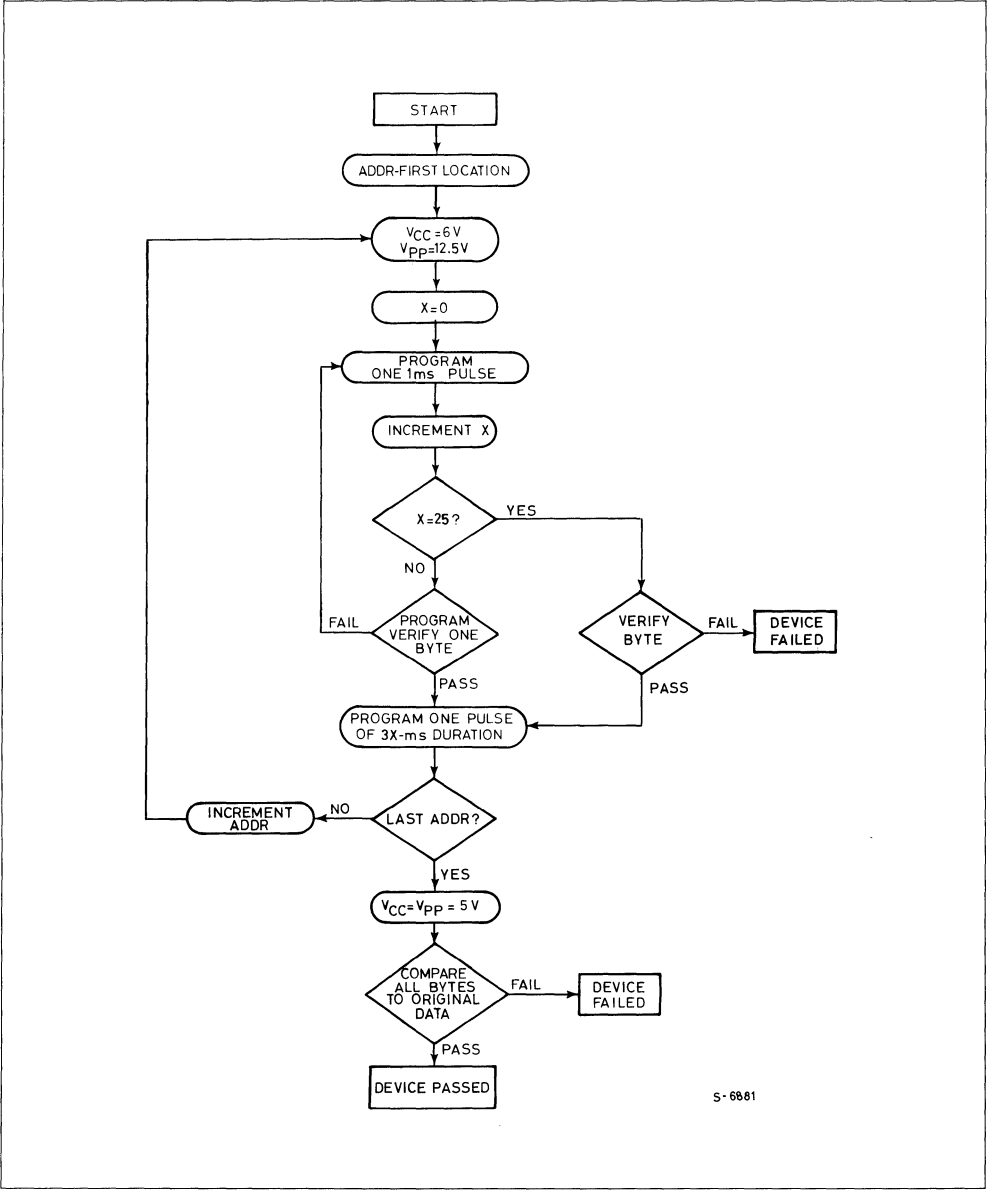
M27512

PROGRAMMING WAVEFORMS
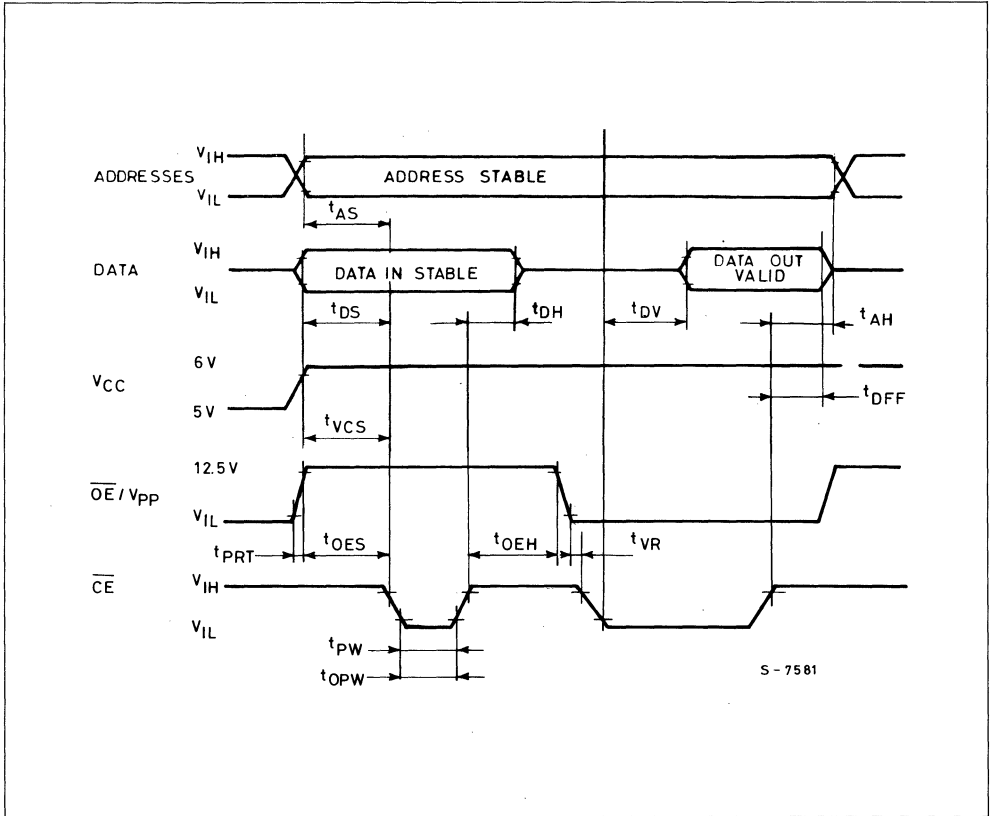
Notes: 1. The input timing reference level is 0.8V for a V_{IL} and 2V for V_{IH}.

2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

FAST PROGRAMMING FLOWCHART

```
                    ┌──────────┐
                    │  START   │
                    └────┬─────┘
            ┌────────────────────────┐
            │   ADDR-FIRST LOCATION  │
            └────────────┬───────────┘
                 ┌───────────────┐
                 │  VCC = 6 V    │
                 │  VPP = 12.5 V │
                 └──────┬────────┘
                   ┌──────────┐
                   │   X = 0  │
                   └────┬─────┘
                ┌────────────────┐
                │    PROGRAM     │
                │ ONE 1ms PULSE  │
                └───────┬────────┘
                 ┌──────────────┐
                 │ INCREMENT X  │
                 └──────┬───────┘
                    ◇ X=25? ◇──YES──┐
                      │NO           │
              ┌─────────────┐   ◇ VERIFY ◇──FAIL──┌──────────┐
        FAIL──│  PROGRAM    │     │ BYTE           │ DEVICE   │
              │ VERIFY ONE  │     │PASS            │ FAILED   │
              │    BYTE     │     │                └──────────┘
              └──────┬──────┘     │
                  │PASS           │
          ┌────────────────────────┐
          │  PROGRAM ONE PULSE     │
          │  OF 3X-ms DURATION     │
          └───────────┬────────────┘
    ┌──────────┐   ◇ LAST ADDR? ◇
    │INCREMENT │──NO──┤
    │  ADDR    │      │YES
    └──────────┘  ┌──────────────┐
                  │ VCC=VPP = 5 V│
                  └──────┬───────┘
                    ◇ COMPARE    ◇──FAIL──┌──────────┐
                    │ ALL BYTES  │        │ DEVICE   │
                    │TO ORIGINAL │        │ FAILED   │
                    │   DATA     │        └──────────┘
                    │PASS
              ┌───────────────┐
              │ DEVICE PASSED │    S-6881
              └───────────────┘
```
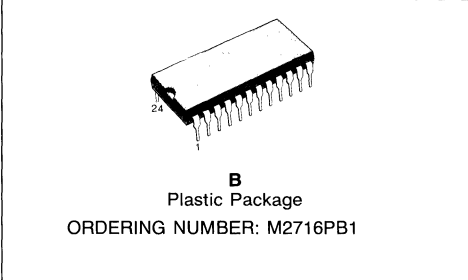
ONE TIME PROGRAMMABLE EPROM

SGS

M2716P

16K (2K × 8) OTP EPROM

- FAST ACCESS TIME:
  450ns MAX M2716P

- SINGLE +5V POWER SUPPLY

- LOW POWER DISSIPATION:
  525 mW MAX. ACTIVE POWER
  132 mW MAX. STANDBY POWER

- SIMPLE PROGRAMMING REQUIREMENTS
  — SINGLE LOCATION PROGRAMMING
  — PROGRAMS WITH ONE 50 ms PULSE

- INPUTS AND OUTPUTS TTL COMPATIBLE
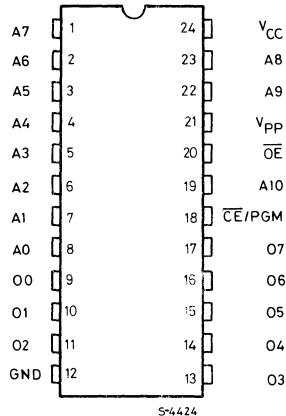 DURING READ AND PROGRAM

- COMPLETELY STATIC

B
Plastic Package
ORDERING NUMBER: M2716PB1

DESCRIPTION

The M2716P is a 16,384-bit One Time Programmable EPROM. It is organized as 2,048 words by 8 bits and manufactured using SGS NMOS-E process. The M2716P has been made for high volume environments where a programmable memory is required for flexibility. The M2716P with its single +5V power supply and with an access time of 450ns, is ideal for use with high performance +5V microprocessor such as $Z8^®$, $Z80^®$ and $Z8000^{TM}$. The M2716P has an important feature which is to separate the output control, Output Enable ($\overline{OE}$) from the Chip Enable Control ($\overline{CE}$). The $\overline{OE}$ control eliminate bus contention in multiple bus microprocessor systems. The M2716P is ideal for volume production environments where inventory and lead time risks occur for program codes. Inventoried in the unprogrammed state, the M2716P is programmed with single 50ms TTL pulse.

Costs incurred for new ROM masks or obsoleted ROM inventories are avoided. The tight package dimensional controls, inherent non-erasability, and legible marking of the M2716P make it the ideal component for these production applications. The M2716P also features a standby mode which reduces the power dissipation without increasing access time. The active current is 100mA while the maximum standby current is only 25 mA, a 75% saving. The standby mode is achieved by appling a TTL-high signal to the $\overline{CE}$ input. The M2716P is available in a 24-lead dual in-line plastic package.
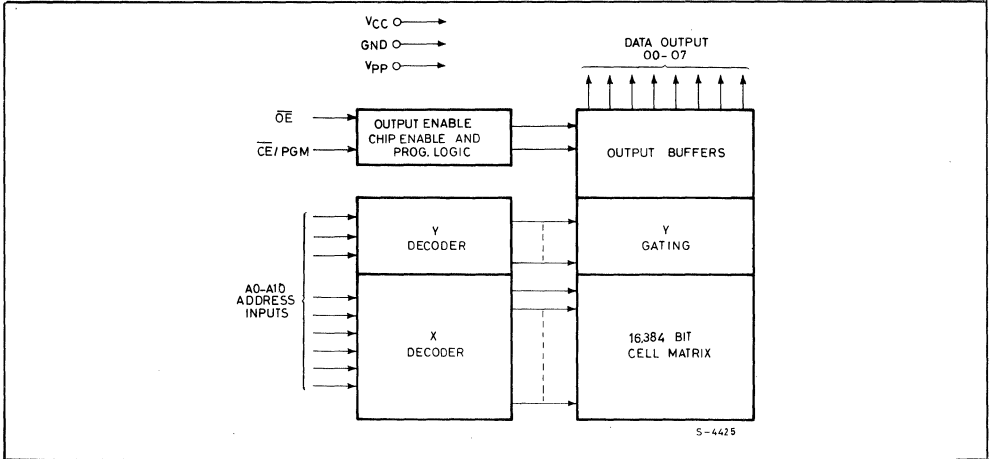
PIN CONNECTIONS

A7	1	24	V_{CC}
A6	2	23	A8
A5	3	22	A9
A4	4	21	V_{PP}
A3	5	20	$\overline{OE}$
A2	6	19	A10
A1	7	18	$\overline{CE}$/PGM
A0	8	17	O7
O0	9	16	O6
O1	10	15	O5
O2	11	14	O4
GND	12	13	O3

S-4424

PIN NAMES

A0-A10	ADDRESSES
$\overline{CE}$/PGM	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
O0-O7	OUTPUTS

M2716P

BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	All Input or Output voltages with respect to ground	+ 6 to − 0.6	V
V_{PP}	Supply voltage with respect to ground during program	+ 26.5 to − 0.3	V
T_{amb}	Ambient temperature under bias	− 10 to + 80	°C
T_{stg}	Storage temperature range	− 65 to + 125	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE \ PINS	CE/PGM (18)	OE (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
READ	V_{IL}	V_{IL}	+ 5	+5	D_{OUT}
STANDBY	V_{IH}	Don't Care	+ 5	+5	HIGH Z
PROGRAM	Pulse V_{IL} to V_{IH}	V_{IH}	+ 25	+5	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	+ 25	+5	D_{OUT}
PROGRAM INHIBIT	V_{IL}	V_{IH}	+ 25	+5	HIGH Z

Note: The five modes of operation of the M2716P are listed in this table. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are a + 5V V_{CC} and a V_{PP} power supply must be at 25V during the three programming modes, and must be at 5V in the other two modes.

READ OPERATION
DC AND AC OPERATING CONDITIONS

	M2716P
Operating Temperature Range	0 to 70°C
V_{CC} Power Supply [1,2]	5V ± 5%
V_{PP} Power Supply [2]	$V_{CC} \pm 0.6$

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ. [3]	Max.	
I_{LI}	Input Load Current	$V_{IN} = 5.25V$			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.25V$			10	μA
$I_{PP1(2)}$	V_{PP} Supply Current	$V_{PP} = 5.25V$	5 mA			
$I_{CC1(2)}$	V_{CC} Supply Current (Standby)	$\overline{CE} = V_{IH}$ $\overline{OE} = V_{IL}$		10	25	mA
$I_{CC2(2)}$	V_{CC} Supply Current (Active)	$\overline{OE} = \overline{CE} = V_{IL}$		57	100	mA
V_{IL}	Input Low Voltage		-0.1		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400 \mu A$	2.4			V

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	M2716P		Unit
			Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		450	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		450	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		120	ns
$t_{DF(4)}$	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	100	ns
t_{OH}	Output Hold from Address $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		ns

CAPACITANCE[4] ($T_{amb} = 25°C$, $f = 1$ MHz)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming.
   The supply current would than be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_{amb} = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested.
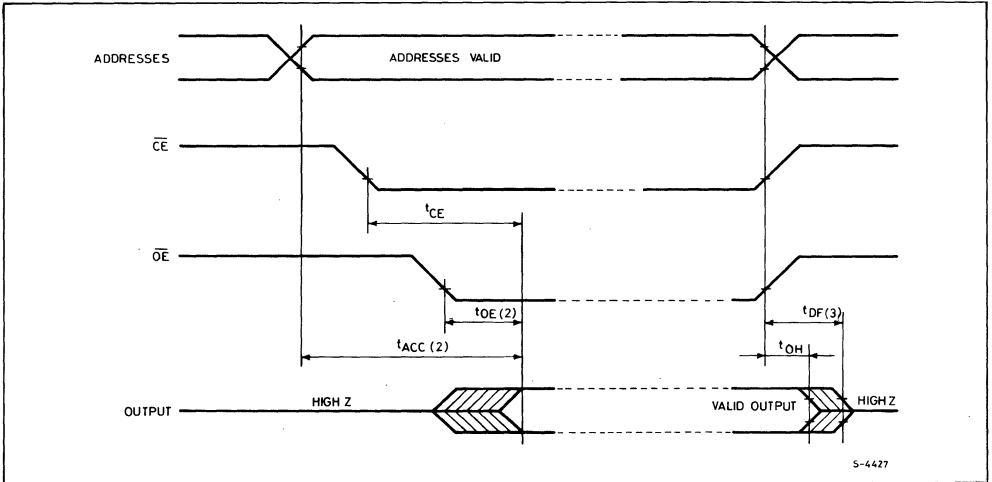
M2716P

AC TEST CONDITIONS
Output Load: 100pF + 1TTL Gate
Input Rise and Fall Times: ≤ = 20ns
Input Pulse Levels: 0.45 to 2.4V
Timing Measurement Reference Levels: Inputs   0.8 and 2V
                                       Outputs 0.8 and 2V

AC WAVEFORMS

S-4427

Notes: 1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

READ MODE
The M2716P has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs 120 ns (t_{OE}) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

STANDBY MODE
The M2716P has a standby mode which reduces the active power dissipation by 75%, from 525mW to 132mW. The M2716P is placed in the standby mode by applying a TTL high signal to $\overline{CE}$ input. When in standby mode, the output are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TIEING
Because M2716P's are usually used in larger memory arrays, the product has 2 line control function that accommodates this use of multiple memory connection. The two line control function allows for:
a) the lowest possible memory power dissipation
   and
b) complete assurance that output bus contention will not ooucur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

M2716P

PROGRAMMING OPERATION [1] ($T_{amb} = 25°C \pm 5°C$, V_{CC}[2] $= 5V \pm 5\%$, V_{PP}[2,3] $= 21V \pm 1V$)∗

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current (for Any Input)	$V_{IN} = 5.25V/0.45$			10	μA
V_{IL}	Input Low Level		-0.1		0.8	V
V_{IH}	Input High Level		2.0		$V_{CC} + 1$	V
I_{CC}	V_{CC} Supply Current				100	mA
I_{PP1}	V_{PP} Supply Current	$\overline{CE}/PGM = V_{IL}$			5	mA
I_{PP2}	V_{PP} Supply Current During Programming Pulse	$\overline{CE}/PGM = V_{IH}$			30	mA

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Set Up Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{AH}	Address Hold Time		2			μs
t_{OEH}	$\overline{OE}$ Hold Time		2			μs
t_{DH}	Data Old Time		2			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}/PGM = V_{IL}$	0		120	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE}/PGM = V_{IL}$			120	ns
t_{PW}	Program Pulse Width		45	50	55	ms
t_{PRT}	Program Pulse Rise Time		5			ns
t_{PFT}	Program Pulse Fall Time		5			ns

CAUTION: The V_{CC} and V_{PP} supplied must be sequenced on and off such that V_{CC} is applied simultaneosly or before V_{PP} and removed simultaneosly or after V_{PP} to prevent damage to the M2716P. The maximum allowable voltage during programming which may be applied to the V_{PP} with respect to ground is $+26V$. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding the 26-volt maximum specification. For convenience in programming, the M2716P may be verified with the V_{PP} supply at 25V $\pm 1V$. During normal read operation, however, V_{PP} must be at V_{CC}.

Notes:
1. SGS guarantees the product only if it is programmed to specifications described herein.
2. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously with or after V_{PP}. The M2716P must not be inserted into or removed from a board with V_{PP} at 25 $\pm 1V$ or damage may occur to the device.
3. The maximum allowable voltage which may be applied to the V_{PP} pin during programming is $+26V$. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 26V maximum specification.

M2716P

AC TEST CONDITIONS

$V_{CC} = 5V \pm 5\%$
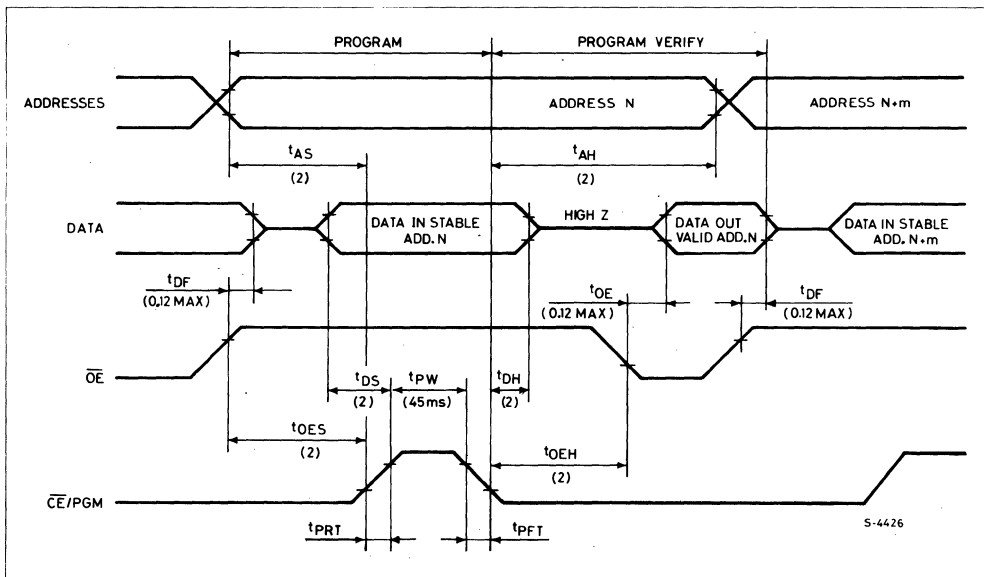
$V_{PP} = 25V \pm 1V$

Input Rise and Fall Times (10% to 90%) = 20 ns

Input Pulse Levels = 0.8V to 2.2V

Input Timing Reference Level = 1V and 2V

Output Timing Reference Level = 0.8V and 2V

PROGRAMMING WAVEFORMS ($V_{PP} = 25V \pm 1V$, $V_{CC} = 5V \pm 5\%$)

Note: All times shown in parantheses are minimum times and are μsec unless otherwise noted.

PROGRAMMING

Initially all bits of the M2716P are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The M2716P is in the programming mode when the V_{PP} power supply is at 25V and $\overline{OE}$ is at V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 msec, active high, TTL program pulse is applied to the CE/PGM input. A program pulse must be applied at each address location to be programmed. You can program any location at any time — either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec. The M2716P must not be programmed with a DC signal applied to the CE/PGM input.

Programming of multiple M2716Ps in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled M2716Ps may be connected together when they are programmed with the same data. A high level TTL pulse applied to the CE/PGM input programs the parallel M2716P.

PROGRAM INHIBIT

Programming of multiple M2716P in parallel with different data is also easily accomplished. Except for CE/PGM, all like inputs (including $\overline{OE}$) of the parallel M2716P may be common. A TTL level program pulse applied to a M2716P CE/PGM input with V_{PP} at 25V will program that M2716P. A low level CE/PGM input inhibits the other M2716P from beign programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at 5V.

MASK READ ONLY MEMORY
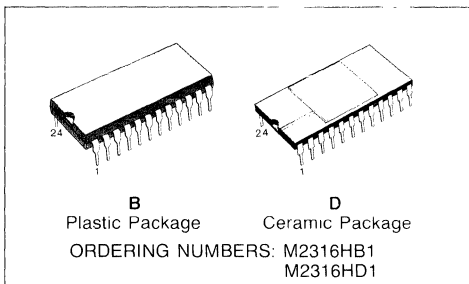
M2316H

16K-BIT READ ONLY MEMORY

- SINGLE +5 ±10% POWER SUPPLY
- ACCESS TIME 300 ns (MAX)
- COMPLETELY STATIC OPERATION
- INPUTS AND OUTPUTS TTL COMPATIBLE
- THERE PROGRAMMABLE CHIP SELECTS FOR SIMPLE MEMORY EXPANSION AND SYSTEM INTERFACE
- THREE STATE OUTPUTS FOR DIRECT BUS INTERFACE
- EPROMs ACCEPTED AS PROGRAM DATA INPUTS
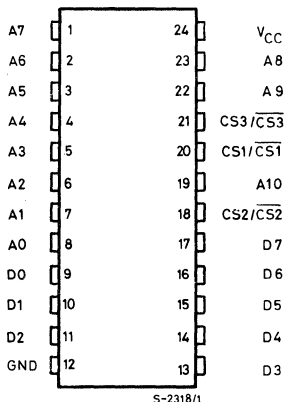- LATE MASK PROGRAMMING FOR FAST TURNAROUND TIME

DESCRIPTION

The M2316H is a 16,384-bit static Read Only Memory organized as 2,048 by 8 bits.
It is manufactured using SGS' high density N-channel Si-Gate MOS process and is ideal for non volatile data storage applications such as program storage. The three-state outputs and TTL input/output levels allow for direct interface with common system bus structures.
The M2316H is available in 24-lead dual in line plastic or ceramic packages.

B
Plastic Package

D
Ceramic Package

ORDERING NUMBERS: M2316HB1
M2316HD1

PIN CONNECTIONS

A7	1	24	V_{CC}
A6	2	23	A8
A5	3	22	A9
A4	4	21	CS3/$\overline{CS3}$
A3	5	20	CS1/$\overline{CS1}$
A2	6	19	A10
A1	7	18	CS2/$\overline{CS2}$
A0	8	17	D7
D0	9	16	D6
D1	10	15	D5
D2	11	14	D4
GND	12	13	D3

S-2318/1

PIN NAMES

A0-A10	ADDRESS INPUTS
D0-D7	DATA OUTPUTS
CS1-CS3	CHIP SELECT INPUTS

M2316H

BLOCK DIAGRAM

S-2319

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any pin with respect to ground	-0.5 to $+7$	V
P_{tot}	Total power dissipation	1	W
T_{stg}	Storage temperature: ceramic package	-65 to $+150$	°C
	plastic package	-55 to $+125$	°C
T_{op}	Operating temperature	0 to $+70$	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

WAVEFORMS

S-4895

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STATIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
V_{OH}	Output High Voltage	$V_{CC} = 4.5V$, $I_{OH} = -400 \mu A$	2.4		V_{CC}	V
I_{LO}	Output Leakage Current	Chip deselected $V_{OUT} = 0V$ to V_{CC}			. 10	μA
V_{IL}	Input Low Voltage	See Note 1	0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{OL}	Output Low Voltage	$V_{CC} = 4.5V$ $I_{OL} = 2.1$ mA			0.4	V
I_{LI}	Input Load Current	$V_{CC} = 5.5V$, $0V \leqslant V_{IN} \leqslant 5.5V$			10	V
I_{CC}	Power Supply Current	Output unloaded, Chip enabled $V_{CC} = 5.5V$, $V_{IN} = V_{CC}$		40	70	mA

Note 1: Input levels that swing more negative than   0.5V will be clamped and may cause damage to the device.

DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min	Typ.	Max	
t_{ACC}	Address Access Time	Output load: 1 TTL load and 100 pf			300	ns
t_{CO}	Chip Select Delay				100	ns
t_{DF}	Chip Deselect Delay	Input transition time: 20 ns			100	ns
t_{OH}	Previous Data Valid After Address Change Delay	Timing reference levels: Input: 1.5V Output: 0.8V and 2.0V	10			ns

CAPACITANCE ($T_{amb} = 25°C$, $f = 1$ MHz, see Note 2)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	All pins except pin under test tied to AC ground			7	pF
C_{OUT}	Output Capacitance				10	pF

Note 2: This parameter is sampled periodically and is not 100% tested

SGS

32K-BIT READ ONLY MEMORY

- M2332-2532 EPROM PIN COMPATIBLE
- M2333-2732 EPROM PIN COMPATIBLE
- SINGLE +5V ±10% POWER SUPPLY
- ACCESS TIME 300 ns (MAX)
- COMPLETELY STATIC OPERATION
- INPUTS AND OUTPUTS TTL COMPATIBLE
- TWO PROGRAMMABLE CHIP SELECTS FOR SIMPLE MEMORY EXPANSION AND SYSTEM INTERFACE
- 2716/2532/2732 EPROMs ACCEPTED AS PROGRAM DATA INPUTS.
- THREE-STATE OUTPUTS FOR DIRECT BUS INTERFACE

B Plastic Package	**F** · Ceramic Package

ORDERING NUMBERS: M2332B1
M2332F1
M2333B1
M2333F1
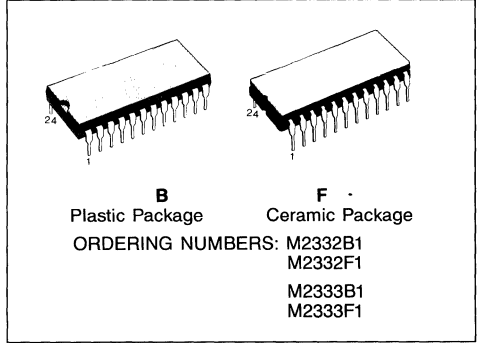
DESCRIPTION

The M2332 and M2333 are 32,768-bit static Read Only Memories organized as 4,096 by 8 bits. They are manufactured using our high density N-channel Si-Gate MOS process and are ideal for large, non-volatile data storage applications such as program storage. The three-state outputs and TTL input/output levels allow for direct interface with common system bus structures.

The M2332 and M2333 are available in 24-lead dual-in-line plastic or ceramic packages.

PIN CONNECTIONS

M2332

Pin		Pin	
A7	1	24	V_{CC}
A6	2	23	A8
A5	3	22	A9
A4	4	21	CS2/$\overline{CS2}$/D.C.
A3	5	20	CS1/$\overline{CS1}$/D.C.
A2	6	19	A10
A1	7	18	A11
A0	8	17	O7
O0	9	16	O6
O1	10	15	O5
O2	11	14	O4
GND	12	13	O3

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M2333

Pin		Pin	
A7	1	24	V_{CC}
A6	2	23	A8
A5	3	22	A9
A4	4	21	A11
A3	5	20	CS1/$\overline{CS1}$/D.C.
A2	6	19	A10
A1	7	18	CS2/$\overline{CS2}$/D.C.
A0	8	17	O7
O0	9	16	O6
O1	10	15	O5
O2	11	14	O4
GND	12	13	O3

S-4893/1

PIN NAMES

A0-A11	ADDRESS INPUT
O0-O7	DATA OUTPUT
CS	CHIP SELECT INPUT
V_{CC}	POWER SUPPLY
GND	GROUND
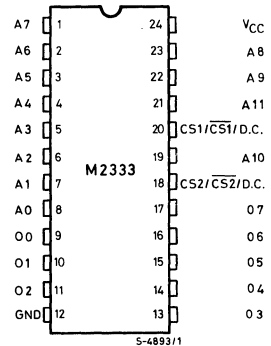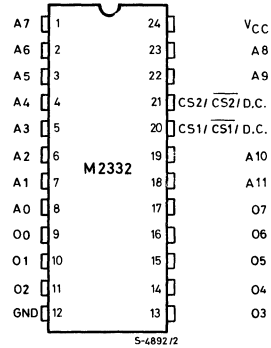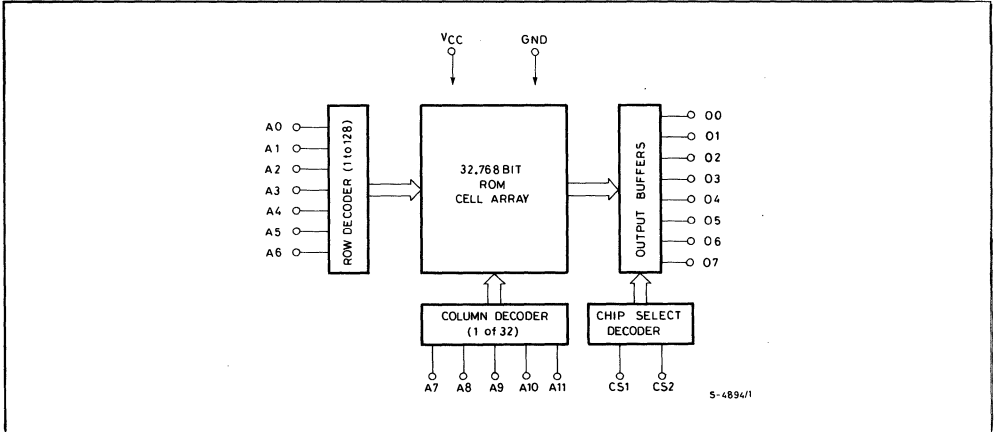
M2332
M2333

BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltages on any pin with respect to ground	-0.5 to $+7$	V
P_{tot}	Total power dissipation	1	W
T_{stg}	Storage temperature: for ceramic package	-65 to $+150$	°C
	for plastic package	-55 to $+125$	°C
T_{op}	Operating temperature	0 to $+70$	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

WAVEFORMS

DC AND OPERATING CHARACTERISTICS ($T_{amb} = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Load Current	$V_{CC} = 5.5V$, $0V \leqslant V_{IN} \leqslant 5.5V$			10	μA
I_{LO}	Output Leakage Current	Chip deselected $V_{OUT} = +0.4V$ to V_{CC}			10	μA
I_{CC}	Power Supply Current	Output unloaded, Chip enabled $V_{CC} = 5.5V$, $V_{IN} = V_{CC}$			70	mA
V_{IL}	Input Low Voltage	See Note 1	-0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{OL}	Output Low Voltage	$V_{CC} = 4.5V$ $I_{OL} = 2.1$ mA			0.4	V
V_{OH}	Output High Voltage	$V_{CC} = 4.5V$ $I_{OH} = -400$ μA	2.4		V_{CC}	V

Note 1: Input levels that swing more negative than $-0.5V$ will be clamped and may cause damage to the device.

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	M2332-33/B1 M2332-33/D1		Unit
			Min	Max	
t_{ACC}	Address Access Time	Output load: 1 TTL Load and 100 pF		250	ns
t_{CO}	Chip Selected Delay			100	ns
t_{DF}	Chip Deselected Delay	Input transition time: 20 ns		100	ns
t_{OH}	Previous Data Valid After Address Change Delay	Timing reference levels: Input: 1.5V Output: 0.8V and 2.0V	20		ns

CAPACITANCE ($T_{amb} = 25°C$, $f = 1$ MHz, see Note 2)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	All pins except pin under test tied to AC ground			7	pF
C_{OUT}	Output Capacitance				10	pF

Note 2: This parameter is sampled periodically and is not 100% tested.

SGS

64K-BIT READ ONLY MEMORY

- ACCESS TIME 250 ns (MAX)
- COMPLETELY STATIC OPERATION
- SINGLE + 5V ±10% POWER SUPPLY
- 8192 × 8 BIT ORGANISATION
- INPUTS AND OUTPUTS TTL COMPATIBLE
- PROGRAMMABLE CHIP SELECT
- THREE-STATE OUTPUTS FOR DIRECT BUS INTERFACE
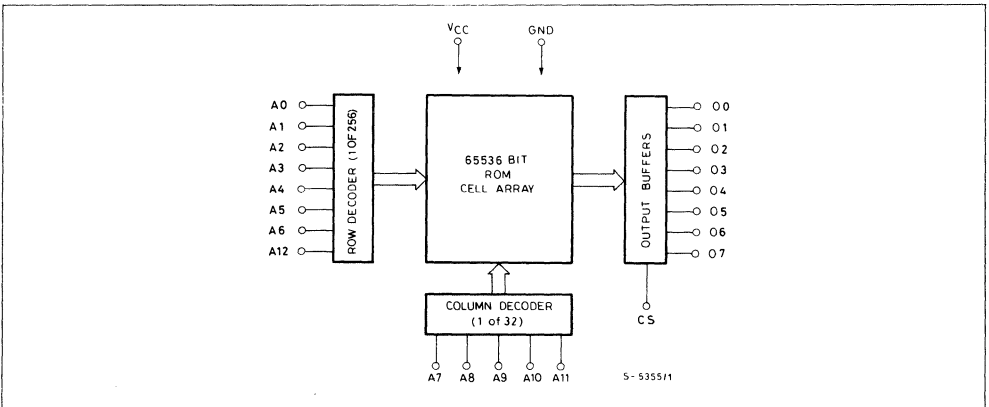- EPROMs ACCEPTED AS PROGRAM DATA INPUTS

B	F
Plastic Package	Ceramic Package

ORDERING NUMBERS: M2364B1
M2364F1
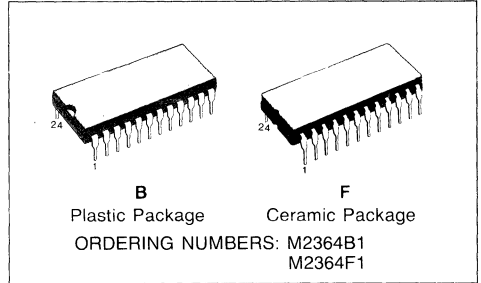
DESCRIPTION

The M2364 is a 65,536-bit static Read Only Memory organized as 8,192 by 8 bits.

It is manufactured using our high density N-channel Si-gate MOS process and is ideal for non-volatile data storage applications where high performance, large bit storage and simple interfacing are important design considerations.

The M2364 is available in 24-lead dual in-line plastic or ceramic package.

PIN CONNECTIONS

A7 ☐ 1	24 ☐ V_{CC}
A6 ☐ 2	23 ☐ A8
A5 ☐ 3	22 ☐ A9
A4 ☐ 4	21 ☐ A12
A3 ☐ 5	20 ☐ CS/$\overline{CS}$/DC.
A2 ☐ 6	19 ☐ A10
A1 ☐ 7	18 ☐ A11
A0 ☐ 8	17 ☐ O7
O0 ☐ 9	16 ☐ O6
O1 ☐ 10	15 ☐ O5
O2 ☐ 11	14 ☐ O4
GND ☐ 12	13 ☐ O3

S-5354/2
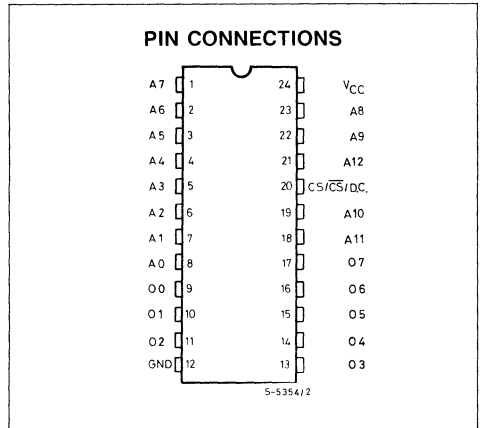
BLOCK DIAGRAM

M2364

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltages on any pin with respect to Ground	+ 0.5 to − 7	V
P_{tot}	Total power dissipation	1	W
T_{stg}	Storage temperature: ceramic package	− 65 to + 150	°C
	plastic package	− 55 to + 125	°C
T_{op}	Operating temperature	0 to + 70	°C

Stresses above those listed under ''Absolute Maximum Ratings'' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC AND OPERATING CHARACTERISTICS ($T_{amb} = 0°C$ to $+ 70°C$, $V_{CC} = 5V \pm 10\%$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Load Current	$V_{CC} = 5.5V$, $0V \leqslant V_{IN} \leqslant 5.5V$			10	μA
I_{LO}	Output Leakage Current	Chip deselected $V_{OUT} = 0V$ to V_{CC}			10	μA
V_{IL}	Input Low Voltage	See note 1	− 0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA $V_{CC} = 4.5V$			0.4	V
V_{OH}	Output High Voltage	$I_{OH} = - 400 \mu A$ $V_{CC} = 4.5V$	2.4		V_{CC}	V
I_{CC}	Power Supply Current	Output unloaded, Chip enabled $V_{CC} = 5.5V$, $V_{IN} = V_{CC}$			80	mA

Note 1: Input levels that swing more negative than − 0.5V will be clamped and may cause damage to the device.

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	M2364		Unit
			Min	Max	
t_{ACC}	Address Access Time	Output load: 1 TTL load and 100 pF		250	ns
t_{CO}	Chip Select Delay			100	ns
t_{DF}	Chip Deselect Delay	Input transition time: 20 ns		100	ns
t_{OH}	Previous Data Valid After Address Change Delay	Timing reference levels: Input: 1.5 V Output: 0.8V and 2.0V	10		ns

CAPACITANCE ($T_{amb} = 25°C$, $f = 1$ MHz, see Note 2))

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	All pins except pin under test tied to AC ground			7	pF
C_{OUT}	Output Capacitance				10	pF

Note 2: This parameter is sampled periodically and is not 100%, tested.

WAVEFORMS

64K-BIT READ ONLY MEMORY

- PIN COMPATIBLE WITH M2764
- ACCESS TIME 250 ns (MAX)
- COMPLETELY STATIC OPERATION
- SINGLE +5V ±10% POWER SUPPLY
- 8192×8 BIT ORGANISATION
- INPUTS AND OUTPUTS TTL COMPATIBLE
- PROGRAMMABLE CHIP SELECT
- THREE-STATE OUTPUTS FOR DIRECT BUS INTERFACE
- EPROMs ACCEPTED AS PROGRAM DATA INPUTS

B
Plastic Package

F
Ceramic Package

ORDERING NUMBERS: M2365B1
M2365F1

DESCRIPTION

The M2365 is a 65,536-bit static Read Only Memory organized as 8,192 by 8 bits. It is manufactured using our high density N-channel Si-gate MOS process and is ideal for non-volatile data storage applications where high performance, large bit storage and simple interfacing are important design considerations.

The M2365 available in 28-lead dual in-line plastic or ceramic package.

PIN CONNECTIONS

Pin		Pin	
NC	1	28	V_{CC}
A12	2	27	CS1/$\overline{CS1}$/NC
A7	3	26	CS2/$\overline{CS2}$/NC
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	CS3/$\overline{CS3}$/NC
A2	8	21	A10
A1	9	20	CS4/$\overline{CS4}$/NC
A0	10	19	O7
O0	11	18	O6
O1	12	17	O5
O2	13	16	O4
GND	14	15	O3

S-6793
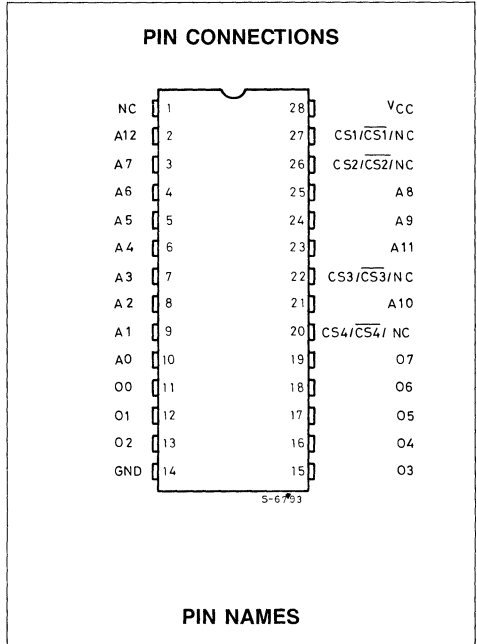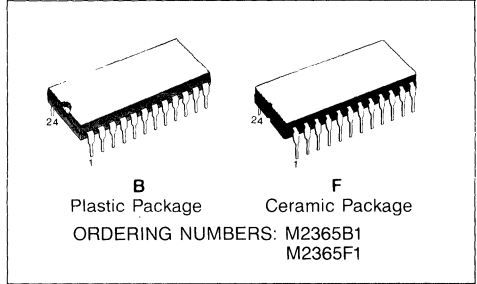
PIN NAMES

A0-A12	ADDRESS INPUT
CS/$\overline{CS}$	CHIP SELECT INPUT
NC	NO CONNECTION
O0-O7	DATA OUTPUT
V_{CC}	POWER SUPPLY
GND	GROUND

BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltages on any pin with respect to ground	$-$ 0.5 to $+$ 7	V
P_{tot}	Total power dissipation	1	W
T_{stg}	Storage temperature: ceramic package	-65 to $+150$	°C
	plastic package	-55 to $+125$	°C
T_{op}	Operating temperature	0 to $+$ 70	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

WAVEFORMS

DC AND OPERATING CHARACTERISTICS ($T_{amb} = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Load Current	$V_{CC} = 5.5V$, $0V \leqslant V_{IN} \leqslant 5.5V$			10	μA
I_{LO}	Output Leakage Current	Chip deselected $V_{OUT} = 0V$ to V_{CC}			10	μA
I_{CC}	Power Supply Current	Output unloaded, Chip enabled $V_{CC} = 5.5V$, $V_{IN} = V_{CC}$			70	mA
V_{IL}	Input Low Voltage	See Note 1	-0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{OL}	Output Low Voltage	$V_{CC} = 4.5V$ $I_{OL} = 2.1$ mA			0.4	V
V_{OH}	Output High Voltage	$V_{CC} = 4.5V$ $I_{OH} = -400 \mu A$	2.4		V_{CC}	V

Note 1: Input levels that swing more negative than $-0.5V$ will be clamped and may cause damage to the device.

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	M2365			Unit
			Min	Typ.	Max	
t_{ACC}	Address Access Time	Output load: 1 TTL load and 100 pf			250	ns
t_{CO}	Chip Select Delay				100	ns
t_{DF}	Chip Deselect Delay	Input transition time: 20 ns			100	ns
t_{OH}	Previous Data Valid After Address Change Delay	Timing reference levels: Input: 1.5V Output: 0.8V and 2.0V	10			ns

CAPACITANCE ($T_{amb} = 25°C$, $f = 1$ MHz, see Note 2)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	All pins except pin under test tied to AC ground			7	pF
C_{OUT}	Output Capacitance				10	pF

Note 2: This parameter is sampled periodically and is not 100% tested.

SGS®

M23256
M23256A

PRELIMINARY DATA

256K-BIT READ ONLY MEMORIES

- ACCESS TIME 250 ns (MAX)
- COMPLETELY STATIC OPERATION
- SINGLE +5V ±10% POWER SUPPLY
- 32 768 × 8 BIT ORGANIZATION
- INPUTS AND OUTPUTS TTL COMPATIBLE
- THREE STATE OUTPUTS FOR DIRECT BUS INTERFACE
- M23256A - AUTOMATIC POWER DOWN ($\overline{CE}$) TWO PROGRAMMABLE CHIP SELECTS
- M23256 - NO POWER DOWN VERSION THREE PROGRAMMABLE CHIP SELECTS
- 28 PIN JEDEC APPROVED PINOUT
- EPROMs ACCEPTED AS PROGRAM DATA INPUTS

B — Plastic Package   **F** — Ceramic Package

ORDERING NUMBERS: M23256B1
M23256F1
M23256AB1
M23256AF1

PIN CONNECTIONS

M23256

CS1/$\overline{CS1}$/ D.C. 1	28 V$_{CC}$
A12 2	27 A14
A7 3	26 A13
A6 4	25 A8
A5 5	24 A9
A4 6	23 A11
A3 7	22 CS2/$\overline{CS2}$/ D.C.
A2 8	21 A10
A1 9	20 CS3/$\overline{CS3}$/ D.C.
A0 10	19 O7
O0 11	18 O6
O1 12	17 O5
O2 13	16 O4
GND 14	15 O3

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M23256A

CS1/$\overline{CS1}$/ D.C. 1	28 V$_{CC}$
A12 2	27 A14
A7 3	26 A13
A6 4	25 A8
A5 5	24 A9
A4 6	23 A11
A3 7	22 CS2/$\overline{CS2}$/ D.C.
A2 8	21 A10
A1 9	20 $\overline{CE}$
A0 10	19 O7
O0 11	18 O6
O1 12	17 O5
O2 13	16 O4
GND 14	15 O3

S-6356/2

DESCRIPTION

The M23256 and M23256A are 26,2144-bit static Read Only Memories organized as 32,768 by 8 bits. They are manufactured using our high density N-channel Si-gate MOS process and are ideal for non-volatile data storage applications where high performance, large bit storage and simple interfacing are important design considerations. The M23256A offers two programmable chip selects and an automatic power down feature.

When $\overline{CE}$ remains high. The M23256 offers three programmable chip selects with no power down feature. Chip select logic levels for the memories are fixed during the masking sequence.

The M23256 and M23256A are available in 28-lead dual in-line plastic or ceramic packages.

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BLOCK DIAGRAM (M23256)
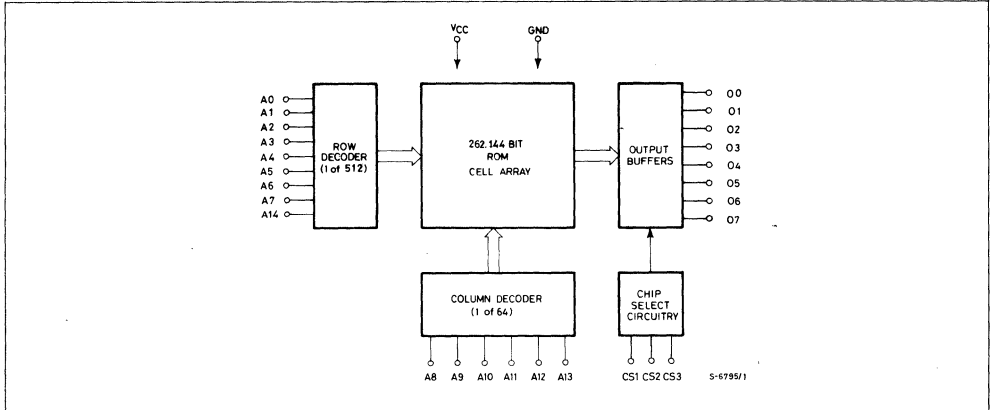
BLOCK DIAGRAM (M23256A)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any pin with respect to ground	− 0.5 to + 7	V
P_{tot}	Total power dissipation	1	W
T_{stg}	Storage temperature: ceramic package	− 65 to + 150	°C
	plastic package	− 55 to + 125	°C
T_{op}	Operating temperature	0 to + 70	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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DC AND OPERATING CHARACTERISTICS ($T_{amb} = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Load Current	$V_{CC} = 5.5V$, $0V \leqslant V_{IN} \leqslant 5.5V$			10	μA
I_{LO}	Output Leakage Current	Chip deselected $V_{OUT} = 0V$ to V_{CC}			10	μA
I_{CC}	Power Supply Current	Output unloaded, Chip enabled $V_{CC} = 5.5V$, $V_{IN} = V_{CC}$			100	mA
V_{IL}	Input Low Voltage	See Note 1	-0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{OL}	Output Low Voltage	$V_{CC} = 4.5V$ $I_{OL} = 2.1$ mA			0.4	V
V_{OH}	Output High Voltage	$V_{CC} = 4.5V$ $I_{OH} = -400\ \mu A$	2.4		V_{CC}	V
I_{SD}	Standby Supply Current (M23256A only)	Outputs unloaded $V_{CC} = 5.5V$, $\overline{CE} = 2.0V$			20	mA

Note 1: Input levels that swing more negative than — 0.5V will be clamped and may cause damage to the device.

AC CHARACTERISTICS

Symbol	Parameter	Test conditions (see Note 2)	M23256 — M23256A		Unit
			Min	Max	
t_{ACC}	Address Access Time			250	ns
t_{ACE}	Chip Enable Access Time	(M23256A only)		250	ns
t_{ACS}	Chip Select Access Time			100	ns
t_{DF1}	Chip Deselect Delay			100	ns
t_{DF2}	Chip Disenable Delay	(M23256A only)		100	ns
t_{OH}	Output Hold After Address Change		10		ns
t_{PU}	Power Up Time	(M23256A only)	0		ns
t_{PD}	Power Down Time	(M23256A only)		100	ns

Note 2: Output load: 1 TTL load and 100 pF. — Input transition time: 20 ns. — Timing reference levels: Input 1.5V, Output 0.8V and 2.0V.

CAPACITANCE ($T_{amb} = 25°C$, f = 1 MHz, see Note 3)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input capacitance	All pins except pin under test tied to AC ground			7	pF
C_{OUT}	Output capacitance				10	pF

Note 3: This parameter is sampled periodically and is not 100% tested.

WAVEFORMS
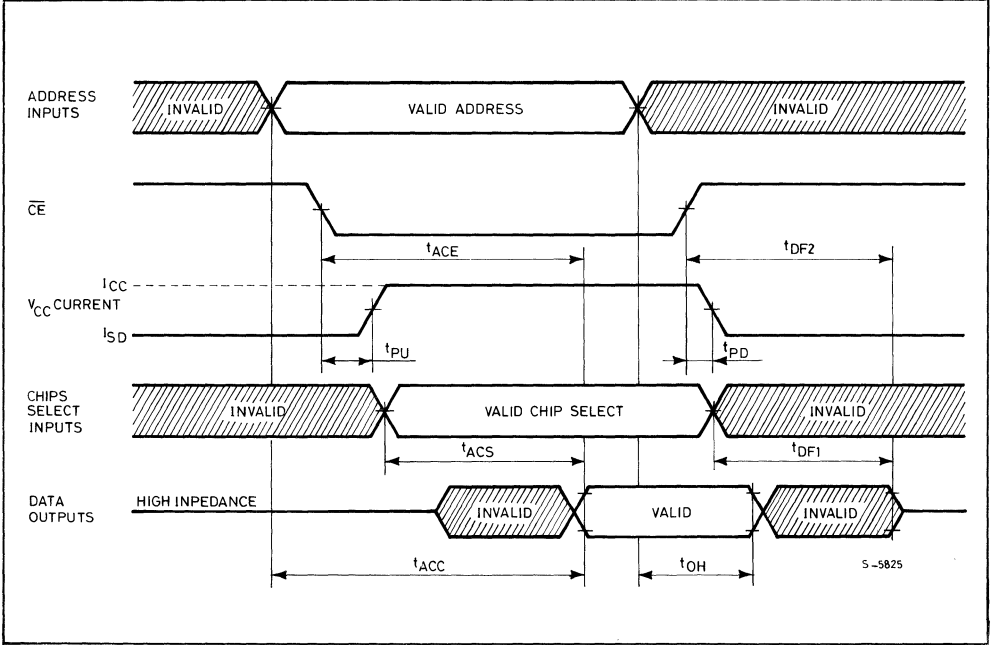
ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY

M8571

1024. BIT SERIAL EEPROM

- 10 YEAR DATA RETENTION
- SINGLE + 5V POWER SUPPLY
- AUTOMATIC POWER DOWN
- INTERNAL HIGH VOLTAGE AND SHAPING GENERATOR
- SELF TIMED E/W OPERATION
- AUTOMATIC ERASE-BEFORE WRITE
- 3-WIRES S-BUS (I2C BUS COMPATIBLE)
- 2 CHIP SELECT FOR SIMPLE MEMORY EXTENSION
- SELF INCREMENTING ADDRESS REGISTER
- MULTI-MODE ADDRESSING (WHEN MS = V_{IH} ALLOWING:
  - PARTITIONING OF THE 1024BITS INTO:
    - 128 × 8bit
    - 64 × 16bit
    - 32 × 32bit
  - OPCODE-LIKE ADDRESSES FOR:
    - halting of a modify operation
    - reading of the device "busy" status
    - "block erase" operation
    - reloading of the address register with the pre-increment value

The M8571 is a 1024-bit Electrically Erasable Programmable Read Only Memory (EEPROM). It allows partitioning of the 1024-bit into: 128 × 8-bit (bytes); 64 × 16-bit (words); 32 × 32-bit (pages). The M8571 is manufactured with SGS's reliable floating gate technology. Addresses and data are transferred serially via a three-line bidirectional bus (S-BUS). When the MS pin is at V_{IL} the device works like the PCD 8571 CMOS RAM. The built-in address register is incremented automatically after writing or reading of each address partition.
The M8571 is available in 8-pin dual in-line plastic and ceramic packages.

B Plastic Package   **F** Ceramic Package

ORDERING NUMBERS: M8571B1
M8571F1

PIN CONNECTIONS

Pin		Pin
CS 1	1	8 V_{CC}
CS 2	2	7 MS
SEN	3	6 SCL
GND	4	5 SDA

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PIN DESCRIPTION

- V_{CC}; GND: Power supplies.
- SCL: Clock line for the S-BUS system.
- SEN: Start/Stop line for the S-BUS system.
- SDA: Data line for the S-BUS system (open drain).
- CS1/CS2: Chip Select inputs. In order to select a device the 2 bits (7th and 6th) in the first byte of the interface protocol, must match the CS values.
- MS: Mode Select input to determine the operating mode of the M8571 (this pin can recognize a non standard level, $V_{IN} \geqslant 7.5V$, to enable "Block Erase" operations).
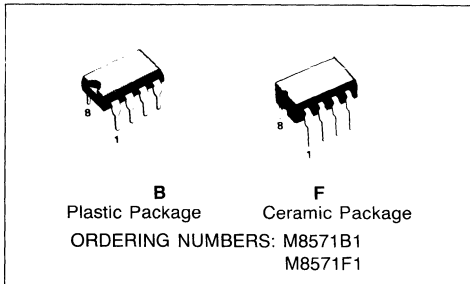
PIN NAMES

CS	CHIP SELECT INPUTS
SEN	START/STOP INPUT
SCL	CLOCK INPUT
SDA	DATA INPUT/OUTPUT
V_{CC}	POWER SUPPLY
GND	GROUND
MS	MODE SELECT INPUT

Fig. 1 - Block Diagram
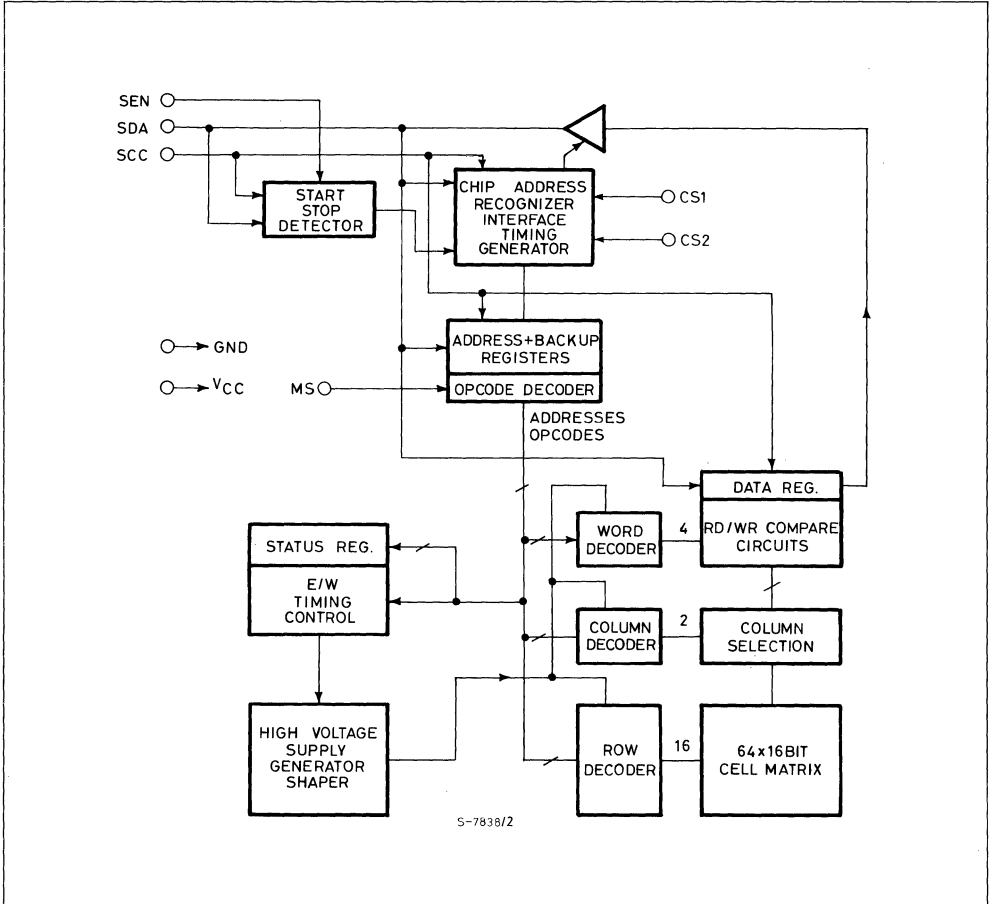
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	All Input or Output voltages with respect to ground	+ 6 to − 0.6	V
T_{amb}	Ambient temperature under bias	− 10 to + 80	°C
T_{stg}	Storage temperature range	− 65 to + 125	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC AND AC OPERATING CONDITIONS

Operating Temperature Range	0 to 70°C
V_{CC} Power Supply	5V ±5%

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Load Current	$V_{IN} = 5.5V$			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$			10	μA
I_{CC1}	V_{CC} Current Standby			2	8	mA
I_{CC2}	V_{CC} Current Active			4	20	mA
V_{IL}	Input Low Voltage		−0.1		1.5	V
V_{IH}	Input High Voltage		3.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Max	Unit
f_{SCL}	Clock frequency		0	125	KHz
t_{SW}	Tolerable spike width on bus			100	ns
t_{DH}	DAT Data hold time		0		μs
t_{SU}	DAT Data set-up time		250		ns
t_r	Signal Rise time			700	ns
t_f	Signal Fall time			300	ns

CAPACITANCE

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
C_{IN}	Input Capacitance	$V_{IN} = 0V$		4	6	pF

M8571

S-BUS DESCRIPTION

The S-BUS is a three-wire bidirectional data-bus with functional features similar to the I²C bus. In fact the S-BUS includes decoding of START/STOP conditions and the arbitration procedure in case of multimaster system configuration. Both different transmission modes are shown in figures 2a and 2b. As it can be seen, the SDA line, in the I²C bus, represents the AND combination of SDA and SEN lines in the S-BUS.

If the SDA and the SEN lines of the S-BUS one short-circuit connected, they appear as the SDA line of I²C bus.

The START/STOP conditions (respectively points 1 and 6) are detected (by the peripherals designed to work with S-BUS) by a transition of the SEN line $(1 - - > 0/0 - - > 1)$ while the SCL line is at the high level.

The SDA line is only allowed to change during the time the SCL line is low (points 2, 3, 4, 5). After the START information (point 1) the SEN line returns to the high level and remains unchanged for all the time the transmission is performed. When the transmission is completed (point 5) the SDA line is set to high level and, at the same time, the SEN line returns to the low level in order to supply the STOP information with a low to high transition; while the SCL line is at high level.

On the S-BUS, as on the I²C bus, each byte of eight bits is followed by one acknowledge bit which is a high level put on the SDA line by transmitter.

A peripheral that acknowledges has to pull down the SDA line during the acknowledge clock pulse as shown in Figure 3.

FIG. 2a - S-BUS CONFIGURATION
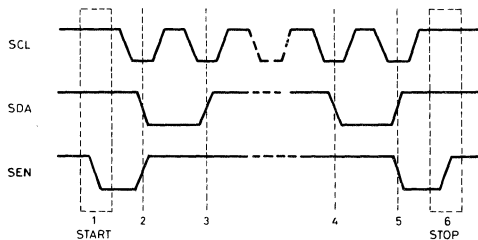
S-7924/1

FIG. 2b - I²C BUS CONFIGURATION
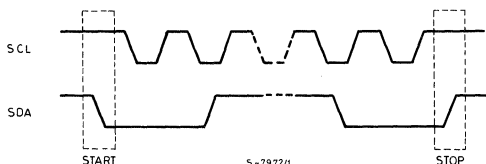
S-7972/1

FIG. 3 - ACKNOWLEDGE
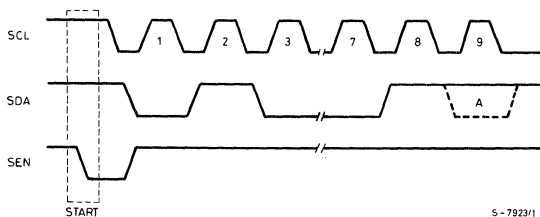
S-7923/1

An addresses receiver has to generate an aknowledge after the reception of each byte; otherwise the SDA line remains at the high level during the ninth clock pulse time.
In this case the master transmitter can generate the STOP information, via the SEN line, in order to abort the transfer.

Compability S-BUS/I²C bus. Using the S-BUS protocol it's possible to implement "mixed" system including S-BUS/I²C bus peripherals.
In order to have the compability with the I²C bus peripherals, the devices including the S-BUS interface must have their SDA and SEN pins have to be connected together as shown in figure 5 and 5b.
It is also possible to use mixed S-BUS/I²C bus protocols as showed in figure 5c. S-BUS peripherals will only react to S-BUS protocol signals, while I²C bus peripheral will only react to I²C bus signals.

FIG. 4 - SYSTEM WITH S-BUS PERIPHERALS
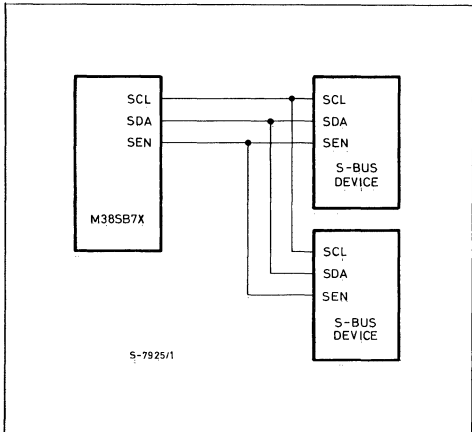
FIG. 5 - SYSTEM WITH "MIXED" S-BUS/I²C BUS PERIPHERAL

M8571
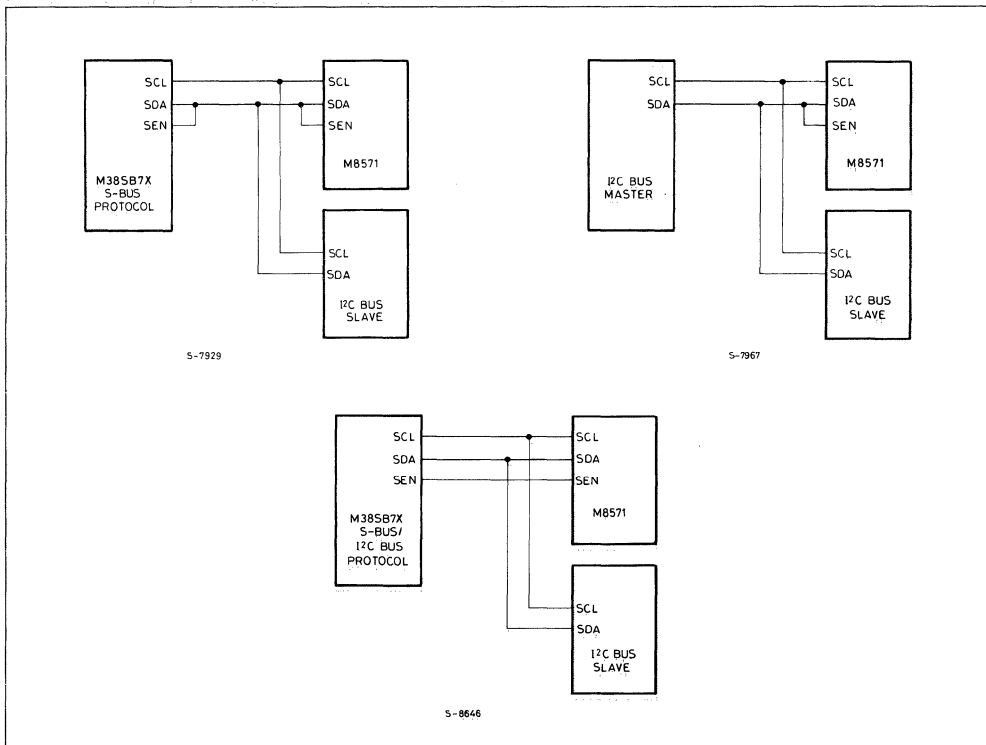
S-BUS DESCRIPTION (Continued)

Multimaster System. The S-BUS allows the implementation of the multimaster configuration (two or more master stations and slave peripherals). In such a system if two or more transmitter, through the SEN line (SEN 1 − − >0 while SCL = 1), require the bus at the same time, the arbitration procedure is performed as in the I²C bus.

FIG. 6 - MULTIMASTER SYSTEM

M8571
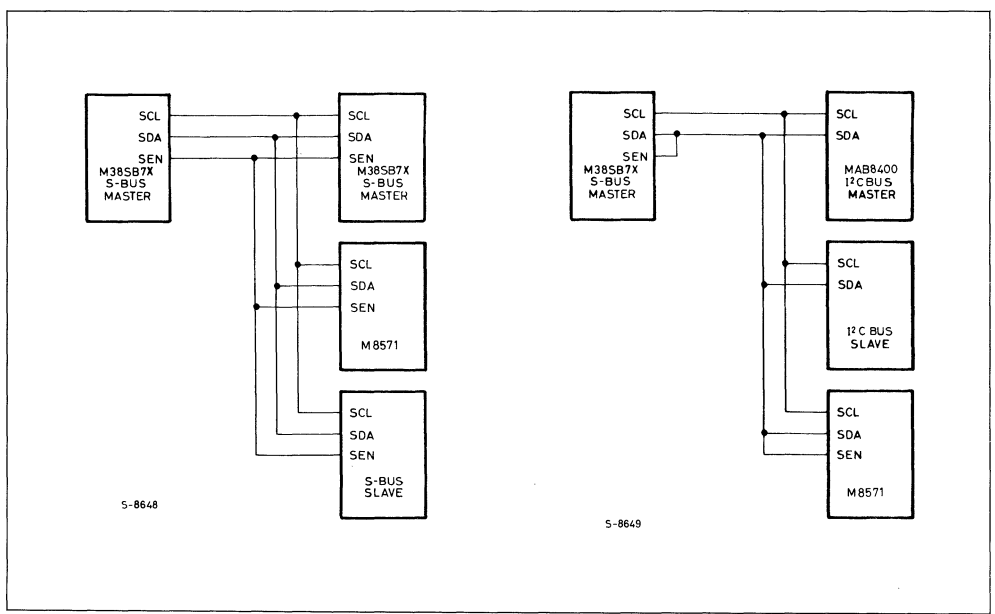
S-BUS INTERFACE

The serial, 3-wire, interface (SDA, SCL and SEN wires are open drain to allow "wired-and" operation) connects several devices which can be divided into "masters" and "slaves". A master is a device that can manage a data transfer; as such, it drives the Start and Stop (SEN), the clock (SCL) and the data (SDA) lines. The bus is "multimaster" in that more master devices can access it; arbitration procedures are provided in the bus management. Obviously, at least one master must be present on the bus. The M8571 is a hardware slave device. It can only answer the requests of the masters on the bus; therefore SDA is an I/O, while SCL and SEN are inputs. The S-BUS allows two operating speed: high (125KHz) and low (2KHz). The M8571 can work at both high and low speed.

START/STOP ACKNOWLEDGE

The timing specs of the S-BUS protocol require that data on the SDA and SEN lines be stable during the "high" time of SCL. Two exceptions to this rule are foreseen and they are used to signal the start and stop condition of a data transfer.
A "high to low" transition on the SEN line, with SCL "high", is a start (STA).
A "low to high" transition on the SEN line, with SCL "high", is a stop.
Data are transmitted in 8-bit groups; after each group, a ninth bit is interposed, with the purpose of acknowledging the transmitting sequence (the transmitter device place a "1" on the bus, the acknowledging receiver a "0").

INTERFACE PROTOCOL

The following description deals with 8-bits data transfers, so that it fully fits when the memory is "seen" as 128 × 8 array. Although the basic structure of the protocol remains the same the behaviour of the M8571 in 16 or 32 bit data transfers is somewhat different. The differencies are descibed later on.

The interface protocol comprises:
- A start condition (STA)
- A "chip address" byte, trasmitted by the master, containing two different informations.

   a) the code identifying the device the master wants to address (this information is present in the first seven bits); 4bits indicates the type of the device (i.e. memory, tuning, A/D, etc.; the code for memories is 1010); then

there is a bit at low level and 2bits that are the Chip Select configuration that must match the hardware present on the 2 CS pins (this is the case of a device with 2 Chip Select like the M8571, for M8571 CS1 and CS2 must match respectively the 7th and the 6th bit of the byte).

   b) the direction of transmission on the bus (this information is given in the 8th bit of the byte); "0" means "Write", that is from the master to the slave, while "1" means "Read". The addressed slave must always acknowledge.

The sequence, from now on, is different according to the value of the R/W bit.

1) $R/\overline{W}$ = "0" (WRITE)

   In all the following bytes the master acts as transmitter; the sequence follows with:
   a) a "word address" byte containing the address of the selected memory word and/or opcode (see word address/opcode section).
   b) a "data" byte which will be written at the address given in the previous byte.
   c) further data bytes which, due to the self incrementing address register, will be written in the "next" memory locations. At the end of each byte the M8571 acknowledges.
   d) a stop condition (STO)

After receiving and acknowledging a data byte or a set of data bytes to be written, the M8571 automatically erases the addressed memory locations and rewrites them with the received data. Since the E/W time for an EEPROM is in the order of 10-20 ms, the next operation can take place only after $t_{E/W}$ (what the master can and must do is described in the E/W TIME SPECS section).
An example of a write sequence is given bellow:
0. STA
1. 10100ss0 A (M8571 acknowledges only if "ss" matches its CS code)
2. xyyyyyyy A
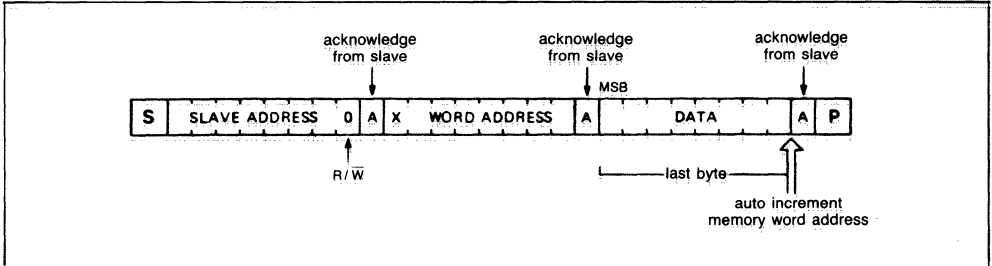3. zzzzzzzz A (at this moment the M8571 starts writing zzzzzzzz at the address yyyyyyy)
than after $t_{E/W}$:
4. tttttttt A (now the M8571 write data tttttttt at address yyyyyyy + 1)

The write sequence can be composed by an unlimited number of data bytes.

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Master transmits to slave receiver (WRITE mode)

```
                    acknowledge        acknowledge        acknowledge
                    from slave         from slave         from slave
                         │                  │ MSB              │
                         ▼                  ▼                  ▼
 S  SLAVE ADDRESS  0  A  X  WORD ADDRESS  A       DATA       A  P
                      ▲                                   ▲
                     R/W̄                   └──last byte──┘
                                                auto increment
                                                memory word address
```

2) R/W̄ = "1" (READ)

In this case the slave acts as transmitter and, therefore, the transmission changes direction. The second byte of the sequence will be sent by the M8571 and it will contain the data present in the memory present at the address pointed by the "current" value of the address register. Following bytes will be the data present at the "next" addresses. At the end of each byte, the M8571 places a "1" on the bus during acknowledge time and waits for the master to send a "0" (meaning "acknowledge"). When the master want to stop the transfer, it gives a "1" (not "acknowledged"): as a consequence, the M8571 leaves the bus high so that the master can give the stop condition. An example is given below:

0. STA
1. 10100ss1 A
2. xxxxxxxx H (xxxxxxxx is the data present in the currently addressed memory location; H is the high level placed on the bus by M8571)

3) MIXED SEQUENCE

When the master wants to read a memory location different from the one currently addressed, a longer sequence is needed, which includes the writing of the address register. The sequence is as follows:

0. STA
1. 10100ss0 A
2. xyyyyyyy A
3. STA
4. 10100ss1 A
5. xxxxxxxx H

Where xxxxxxxx is the data present in the yyyyyyy memory location
As appears from the example, a start condition can be given without a previous stop condition.

Master reads slave immediately after first byte (READ mode)

```
                    acknowledge        acknowledge        acknowledge
                    from slave         from master        from master
                         │                  │ MSB              │
                         ▼                  ▼                  ▼
 S  SLAVE ADDRESS  1  A       DATA        A                  1  P
                      ▲                  ▲
                     R/W̄  └─ n bytes ─┘  └── n bytes ──┘
                                 auto increment
                                 word address
```
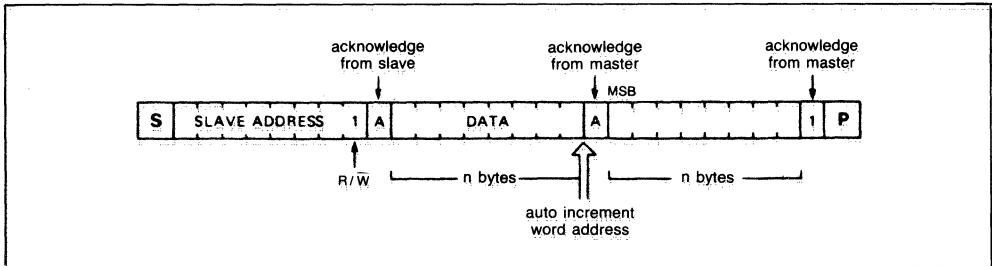
Master reads after setting word address (WRITE word address; READ data)
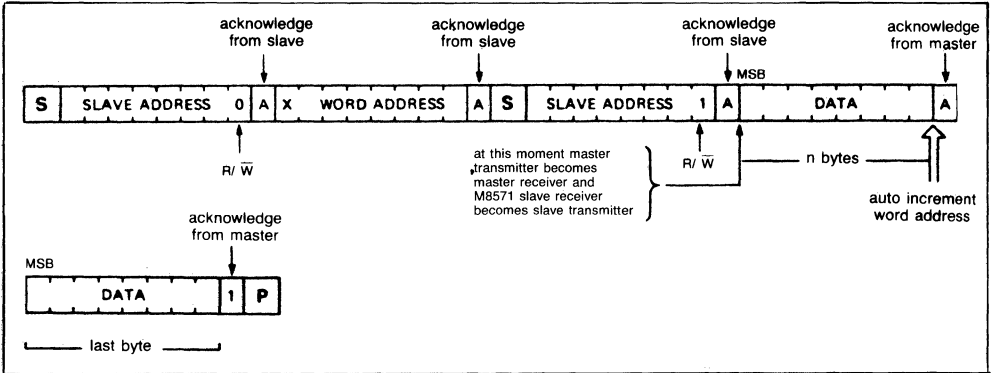
4) E/W TIME SPECS

After the beginning of an E/W operation at a certain location the M8571 is "busy" until the operation is finished. To show this busy state, the M8571 refuses acknowledge of the next data bytes until $t_{E/W}$ is over. The master device that wants to use the self-increment feature must therefore keep sending the next data byte and monitoring the acknowledge bit until it becomes active.

The communication sequence on the bus becomes, therefore.

0. STA
1. 1 0 1 0 0 s s 0 A
2. x y y y y y y y A
3. z z z z z z z z A
4a. t t t t t t t t H (not acknowledged when $t < t_{E/W}$)
4b. t t t t t t t t A (acknowledged after $t_{E/W}$)

Now the M8571 will write data ttttttt at address yyyyyyy+1
This usage mode keeps the bus unavailable for other tasks during the $t_{E/W}$ time. It is possible to free the bus by giving a stop condition (this condition stops only the bus sequence, not the E/W operation). After a stop condition the access sequence must be started again from the beginning (start).
The E/W circuitry in the M8571 performs automatically the "Erase before Write" sequence required by the technology. Furthermore, both erase and write last all (and only) the time needed for the required modification to happen (this is ac-

complished by an intelligent "compare and retry" circuitry). This optimizes E/W time but may have the drawback of "locking" the circuitry in case a memory location "breaks down" and can not be modified (in which case $t_{E/W}$ becomes infinite).
To overcome this drawback, it has been made possible to force the circuit out of the E/W status, that is to halt a modify operation. Two different modes are provided, depending on the value of the MS control pin:

$$MS \leqslant V_{IL}$$

The E/W operation is unconditionally stopped by a following valid chip address byte.

$$MS \geqslant V_{IH}$$

An opcode is provided to halt the operation (see "EEPROM mode" section).

5) WORD ADDRESS/OPCODE

The second byte transmitted in a write sequence can assume several meaning according to the value of the MS pin. In any case, it carries all the informations the M8571 needs to perform the desired operation.
MS can assume three different values:

- V_{IL} ($V_{IN} \leq 1.5V$)
- V_{IH} ($3.0V \leq V_{IN} < V_{CC} + 1$)
- V_H ($9.0V \leq V_{IN} \leq 12V$)

M8571

With regards to the value of MS, the possible behaviours are:

a) MS = V_{IL} ("RAM mode")

In this mode the M8571 is compatible with the PCD 8571 RAM (128 × 8bit). The second byte of the sequence gives the address of the word to be selected, both for write and for read:

1. x y y y y y y y A

y y y y y y y is the word address; the first bit is "don't care; the main feature of this mode are the following:
  . the memory appears as an 128 × 8 array
  . only "byte operations are allowed;
  . E/W operations are stopped by the following accesses.

b) MS = V_{IH} (EEPROM mode)

The word address-byte now must be regarded as mixed address-opcode byte; more precisely, the first three bits indicate the meaning to be attributed to the remainder of the byte. The possible combinations are:

0 y y y y y y y	byte-mode (8 bits) RD or E/W at address y y y y y y y
1 0 y y y y y y	word-mode (16 bits) RD or E/W at address y y y y y y
1 1 0 y y y y y	page-mode (32 bits) RD or E/W at address y y y y y
1 1 1 1 1 1 1 1	E/W cycle stop
1 1 1 0 0 0 0 0	Read busy bit
1 1 1 0 0 1 0 0	Block Erase (see also BLOCK mode)
1 1 1 1 0 0 0 1	Reload Address Register with pre-increment data

In this mode, as well as in RAM mode, the "busy" information is transmitted from the M8571 to the master using the "no acknowledge" format. Furthermore, "Read busy bit" instruction, which is always answered by the M8571 no matter what it is doing, allows the master to know wheter the "no acknowledge" condition comes from a "busy" status or from a malfunction; the "busy" status is signalled by the byte 11100101; the "no busy" by 00011010.

Also in this mode the self-incrementing address register is available, both for read and for write, for each word length.

The M8571 is provided with a double register for storing the address that is sent during the second byte of a write sequence.

When athe self-incrementing is used, this address becomes the "starting address" of the modified string of bytes. The "reload" instruction allows the master to recover this address if it wants to read the modified string from the beginning, without the need for external storage of the "starting address".

c) MS = V_H (BLOCK mode)

The only instruction that can be executed in this mode is "Block Erase", which is useful to erase the whole array in a single shot. This can occur either during testing or at the set-up of a new system, when all the memory must be written anew. When this instruction is given, the self-timing circuitry is disabled, so that an E/W cycle stop instruction must be given after the proper E/W time, to stop the operation. The "enable" feature obtained with the non standard level on MS was added to avoid unintentional clearing of the whole memory, whenever the "Block Erase" code was erroneously sent.

6) 16-bit or 32-bit OPERATIONS

The obvious advantage of an operation on 16 bits (a word) or on 32 bits (a page) is that the E/W time is 10 to 20 ms for the whole word or page. When a word or page mode operation is required, the device behaviour undergoes some slight modifications:
- The M8571 waits for receiving all the bytes that compose the word or the page before starting an E/W operation;
- The self-incrementing address register keeps into account the word or page lenght so that, at the end of a word or page mode operation, it points to the next word or page.
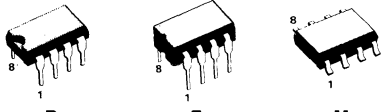
256 BIT (16 x 16) SERIAL EEPROM

- LOW COST
- SINGLE SUPPLY (5V ± 10%)
- TTL COMPATIBLE
- 16 x 16 READ/WRITE MEMORY
- LOW STANDBY POWER
- NON-VOLATILE
- RELIABLE FLOTOX PROCESS
- EXTENDED TEMPERATURE RANGE

The M9306 is a 256 bit non-volatile sequential access memory manufactured using SGS FLOATING GATE process. It is a peripheral memory designed for data storage and/or timing and is accessed via a simple serial interface. The device contains 256 bits organized as 16 x 16. The M9306 has been designed to meet application requiring up to 10000 E/W cycles per word. Written information has at least 10 year data retention. A power down mode allows consumption to be decreased.

B	F	M
Plastic Package	Ceramic Package	Plastic Micropackage

ORDERING NUMBERS: M9306B1-B6
M9306F1-F6
M9306M1-M6
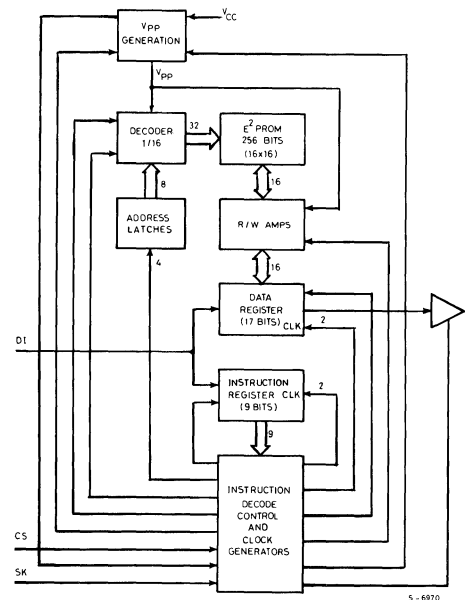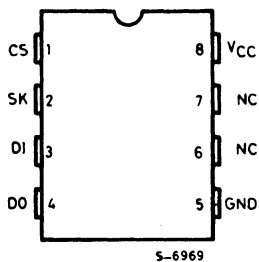
PIN CONNECTIONS

S-6969

BLOCK DIAGRAM

PIN NAMES

CS	CHIP SELECT
SK	SERIAL DATA CLOCK
DI	SERIAL DATA INPUT
DO	SERIAL DATA OUTPUT
V_{CC}	POWER SUPPLY
GND	GROUND

FUNCTIONAL DESCRIPTION

The input and output pins are controlled by separate serial formats. Seveb 9-bit instruction can be executed. The instruction format as a logical "1" has a start bit, four bits as an op code, and four bits of address. The on-chip programming voltage generator allows the user to use a single power supply (V_{CC}). The serial output (DO) pin is valid only during the read mode. During all other modes the DO pin is in high impedance state, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16 bit serial out shift register. A dummy bit (logical "0") precedes the 16 bit data output string. The output data changes during the high state of the system clock.

ERASE/WRITE ENABLE AND DISABLE

Programming must be preceded once by programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction in executed. The programming disable instruction is provided to protect against accidental data disturbance.

Execution of a READ instruction is independent of both EWEN and EWDS instructions.

ERASE

Like most EEPROMs, the register must first be erased (all bits set to 1s) before the register can

be written (certain bits set to 0s). After an ERASE instruction is input, CS is dropped low. This falling edge of CS determines the start of programming. The register at the address specified in the instruction is then set entirely to 1s. When the erase/write programming time ($t_{E/W}$) constraint has been satisfied, CS is brought up for at least one SK period. A new instruction may then be input, or a low power standby state may be achieved by dropping CS low.

WRITE

The WRITE instruction is followed by 16 bits of data which are written into the specified address. This register must have been previously erased. Like any programming mode, erase/write time is determined by the low state of CS following the instruction. The on chip high voltage section only generates high voltage during this programming mode, which prevents spurious programming during other modes. When CS rises to V_{IH}, the programming cycles ends. All programming mode should be ended with CS high for one SK period, or followed by another instruction.

CHIP WRITE

Entire chip can be written for ease of testing. Writing the chip means that all registers in the memory array have each bytes set as the byte sent with the instruction.

CHIP ERASE

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a 1. Each register is then ready for a WRITE instruction.

INSTRUCTION SET

Instruction	SB	Op Code	Address	Data	Comments
READ	1	1000	A3A2A1A0		Read register A3A2A1A0
WRITE	1	0100	A3A2A1A0	D15-D0	Write register A3A2A1A0
ERASE	1	1100	A3A2A1A0		Erase register A3A2A1A0
EWEN	1	0011	0 0 0 0		Erase/write enable
EWDS	1	0000	0 0 0 0		Erase/write disable
ERAL	1	0010	0 0 0 0		Erase all registers
WRAL	1	0001	0 0 0 0	D15-D0	Write all registers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Values	Unit
V_I	Voltage Relative to GND	+ 6V to − 0.3	V
T_{amb}	Ambient Operating Temperature: standard	0 to + 70	°C
	extended	− 40 to + 85	°C
T_{stg}	Ambient Storage Temperature	− 65 to + 125	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (0°C to + 70°C, for standard Temperature/ − 40°C to + 85°C for extended Temperature, $V_{CC} = 5V \pm 10\%$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating Voltage		4.5		5.5	V
I_{CC1}	Operating Current	$V_{CC} = 5.5V$, CS = 1		1.5	5	mA
I_{CC2}	Standby Current	$V_{CC} = 5.5V$, CS = 0		1.2	3	mA
I_{CC3}	E/W Operating Current	$V_{CC} = 5.5V$		2.5	6	mA
V_{IL}	Input Voltage Levels		− 0.1		0.8	V
V_{IH}			2.0		$V_{CC} + 1$	
V_{OL}	Output Voltage Levels	$I_{OL} = 2.1$ mA			0.4	V
V_{OH}		$I_{OH} = - 400 \mu A$	2.4			
I_{LI}	Input Leakage Current	$V_{IN} = 5.5V$			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$, CS = 0			10	μA
	SK Frequency				250*	kHz
	SK Duty Cycle		25		75	%
	Input Set-Up and Hold Times					
t_{CSS}	CS		0.2			
t_{CSH}			0			μs
t_{DIS}	D I		0.2			
t_{DIH}			0.2			
t_{PD1}	Output Delay	$CL = 100$ pF			0.5	
t_{PD0}	DO	$V_{OL} = 0.8V$,			0.5	μs
		$V_{OH} = 2.0V$				
$t_{E/W}$	Erase/Write Pulse Width		5		30	ms

* The maximum SK Frequency is 500 KHz when SK Duty Cycle is as 50%

M9306

TIMING DIAGRAMS
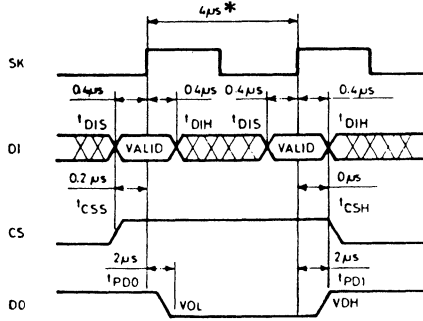
* THIS IS THE MAXIMUM SK FREQUENCY   S-6971

S-8280
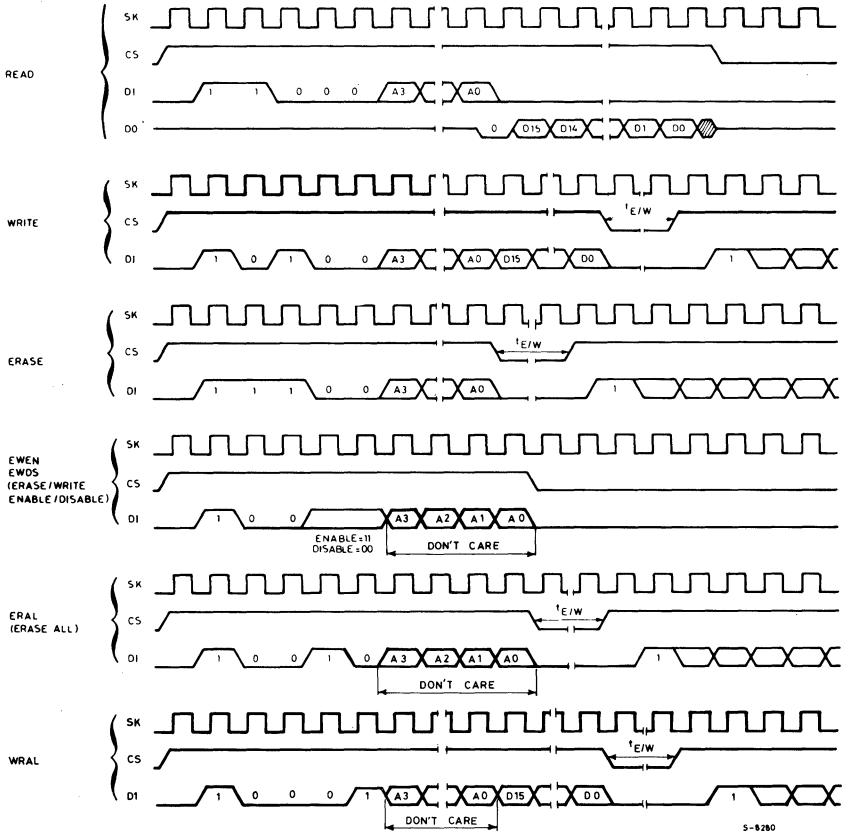
M9346

1024 BIT (64 × 16) SERIAL EEPROM

- LOW COST
- SINGLE SUPPLY READ/WRITE/ERASE OPERATIONS (5V ± 10%)
- TTL COMPATIBLE
- 64 × 16 READ/WRITE MEMORY
- LOW STANDBY POWER
- NON-VOLATILE ERASE AND WRITE
- RELIABLE FLOTOX PROCESS
- SELF-TIMED PROGRAMMING CYCLE
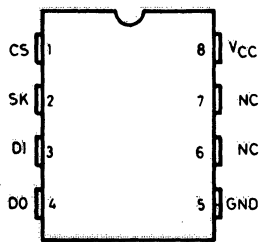- DEVICE STATUS SIGNAL DURING PROGRAMMING

The M9346 is a 1024 bit non-volatile sequential access memory manufactured using SGS FLOATING GATE process. It is a peripheral memory designed for data storage and/or timing and is accessed via a simple serial interface. The device contains 1024 bits organized as 64x16. Written information is stored in a floating gate cell untill updated by an erase and write cycle. The M9346 has been designed for applications requiring up to 10^4 erase/write cycles per register. A power down mode allows a consumption decrease by 75%.

B	**F**	**M**
Plastic Package	Ceramic Package	Plastic Micropackage
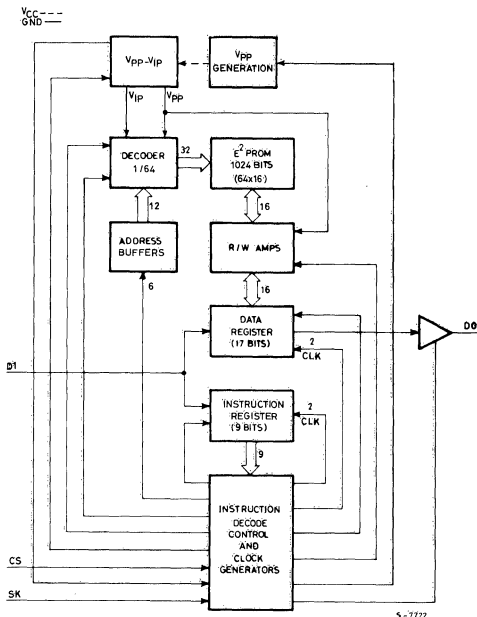
ORDERING NUMBERS: M9346B1-B6
M9346F1-F6
M9346M1-M6

PIN CONNECTIONS

CS	1	8	V_{CC}
SK	2	7	NC
DI	3	6	NC
DO	4	5	GND

S-6969

BLOCK DIAGRAM

S-7722

PIN NAMES

CS	CHIP SELECT
SK	SERIAL DATA CLOCK
DI	SERIAL DATA INPUT
DO	SERIAL DATA OUTPUT
V_{CC}	POWER SUPPLY
GND	GROUND

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M9346

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Values	Unit
V_I	Voltage Relative to GND	+ 6V to − 0.3	V
T_{amb}	Ambient Operating Temperature: standard	0 to + 70	°C
	extended	− 40 to + 85	
T_{stg}	Ambient Storage temperature	− 65 to + 125	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (0° to + 70°C, for standard Temperarure/ − 40° to + 85°C for extended Temperarure, $V_{CC} = 5V \pm 10\%$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating Voltage		4.5		5.5	V
I_{CC1}	Operating Current Erase/	$V_{CC} = 5.5V$, $CS = 1$,			12	mA
	Write Operating Current	$SK = 1$, $V_{CC} = 5.5V$			12	mA
I_{CC2}	Standby Current	$V_{CC} = 5.5V$, $CS = 0$			3	mA
V_{IL}	Input Voltage Levels		− 0.1		0.8	V
V_{IH}			2.0		$V_{CC} + 1$	
V_{OL}	Output Voltage Levels	$I_{OL} = 2.1$ mA			0.4	V
V_{OH}		$I_{OH} = - 400 \mu A$	2.4			
I_{LI}	Input Leakage Current	$V_{IN} = 5.5V$			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$, $CS = 0$			10	μA
	SK Frequency		0		250	kHz
	SK Duty Cycle		25		75	%
t_{CSS}	Input Times		0.2			μs
t_{CSH}	CS		0			
t_{DIS}	D I		0.4			
t_{DIH}			0.4			
t_{PD1}	Output DO	$CL = 100$ pF $V_{OL} = 0.8V$, $V_{OH} = 2V$			2	μs
t_{PD0}		$V_{IL} = 0.45V$, $V_{IH} = 2.40V$			2	
$t_{E/W}$	Self-Timed Program Cycle				10	ms
t_{CS}	Min CS Low Time		1			μs
t_{SV}	Rising Edge of CS to Status Valid	$C_L = 100$ pF			1	μs
t_{0H}, t_{1H}	Falling Edge of CS to DO tri-state				0.4	μs
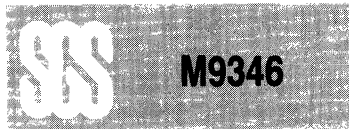
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FUNCTIONAL DESCRIPTION

The input and output pins are controlled by separate serial formats. Seven 9-bit instructions can be executed. The instruction format as a logical "1" has a start bit, four bits has an op code, and six bits of address. The on-chip programming voltage generator allows the user to use a single power supply (V_{CC}). It only generates high voltage during the programming modes (write, erase, chip-erase, chip-write) to prevent spurious programming during other modes. The programming cycle is self timed, with the data out (DO) pin indicating the ready/busy state of the chip. The serial output (DO) pin is valid as data out during the read mode, and if initiated, as a ready/busy status indicator during a programming cycle. During all other modes the DO pin is in high impedance state eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16 bit serial out shift register. A dummy bit (logical "0") precedes the 16 bit data output string. The output data changes during the high state of the system clock.

ERASE/WRITE ENABLE AND DISABLE

When V_{CC} is applied to the part it powers up in the programming disable (EWDS) state, programming must be preceded by programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed or V_{CC} is removed from the part. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both EWEN and EWDS instructions.

ERASE

Like most EEPROMs, the register must first be erased (all bits set to logical '1') before the register can be written (certain bits set to logical '0'). After an ERASE instruction is input, CS is dropped low.

This falling edge of CS determines the start of the self-timed programming cycle. If CS is brought high subsequently (after observing the t_{CS} specification), the DO pin will indicate the ready/busy status of the chip. The DO pin will go low if the chip is still programming. The DO pin will go high when all bits of the register at the address specified in the instruction have been set to a logical '1'. The part is now ready for the next instruction sequence.

WRITE

The WRITE instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data (DO) is put on the data in (DI) pin CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. Like all programming modes, DO indicates the ready/busy status of the chip if CS is brought high after a minimum of 1 μs (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register at the address specifed in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction. The register to be written into must have been previously erased.

CHIP ERASE

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a logical '1'. Each register is then ready for a WRITE instruction. The chip erase cycle is identical to the erase cycle except for the different op code.

CHIP WRITE

All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

Note 1: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Note 2: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. If can remain deactivated during the self-timed programming cycle and status check.
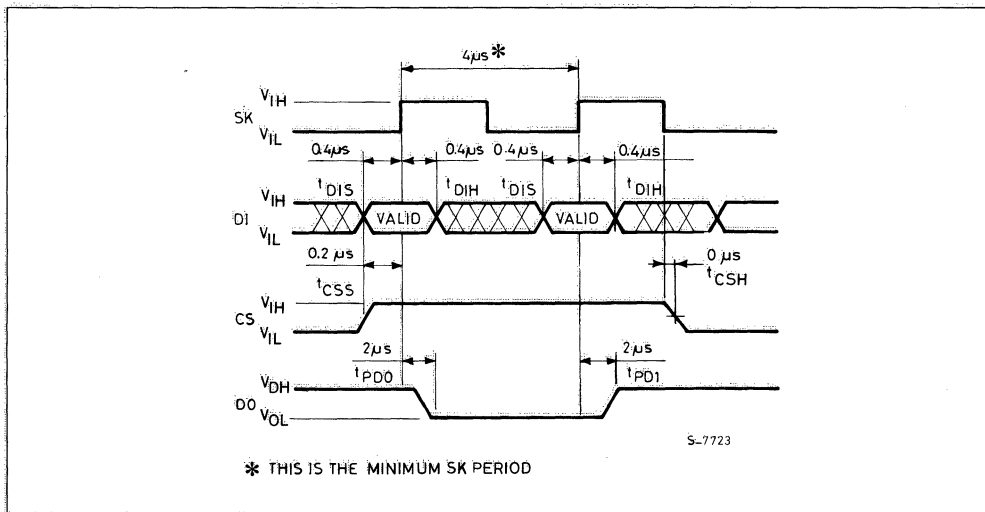
INSTRUCTION SET

| Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5A4A3A2A1A0		Read register A5A4A3A2A1A0
WRITE	1	01	A5A4A3A2A1A0	D15-D0	Write register A5A4A3A2A1A0
ERASE	1	11	A5A4A3A2A1A0		Erase register A5A4A3A2A1A0
EWEN	1	00	11 x x x x		Erase/write enable
EWDS	1	00	00 x x x x		Erase/write disable
ERAL	1	00	10 x x x x		Erase all registers
WRAL	1	00	01 x x x x	D15-D0	Write all registers

M9346 has 7 instructions as shown. Note that the MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 6-bit address for 1 of 64, 16-bit registers.

TIMING DIAGRAMS
SYNCHRONOUS DATA TIMING

S-7723

✳ THIS IS THE MINIMUM SK PERIOD

150

TIMING DIAGRAMS

INSTRUCTION TIMING
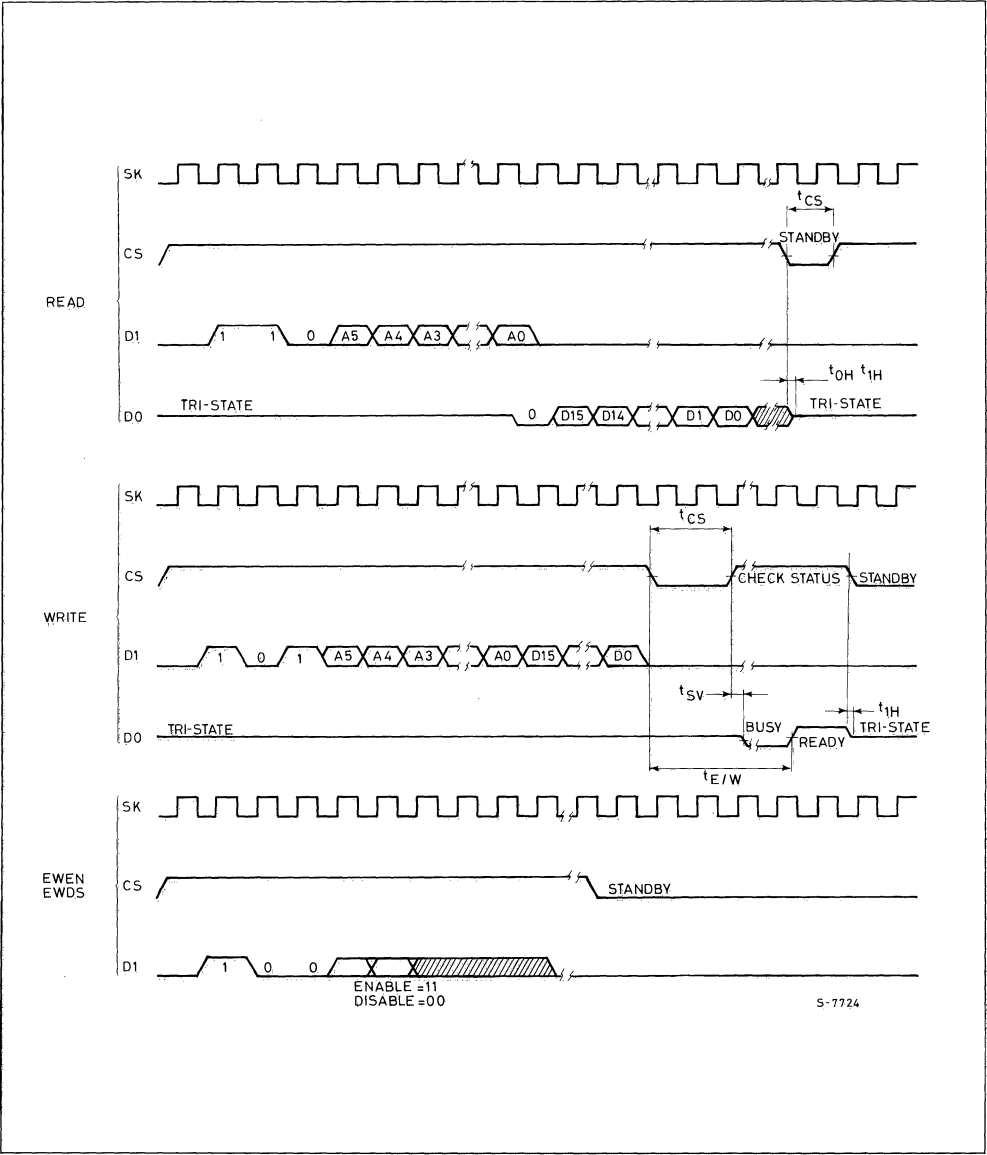
S-7724

TIMING DIAGRAMS (Continued)
INSTRUCTION TIMING
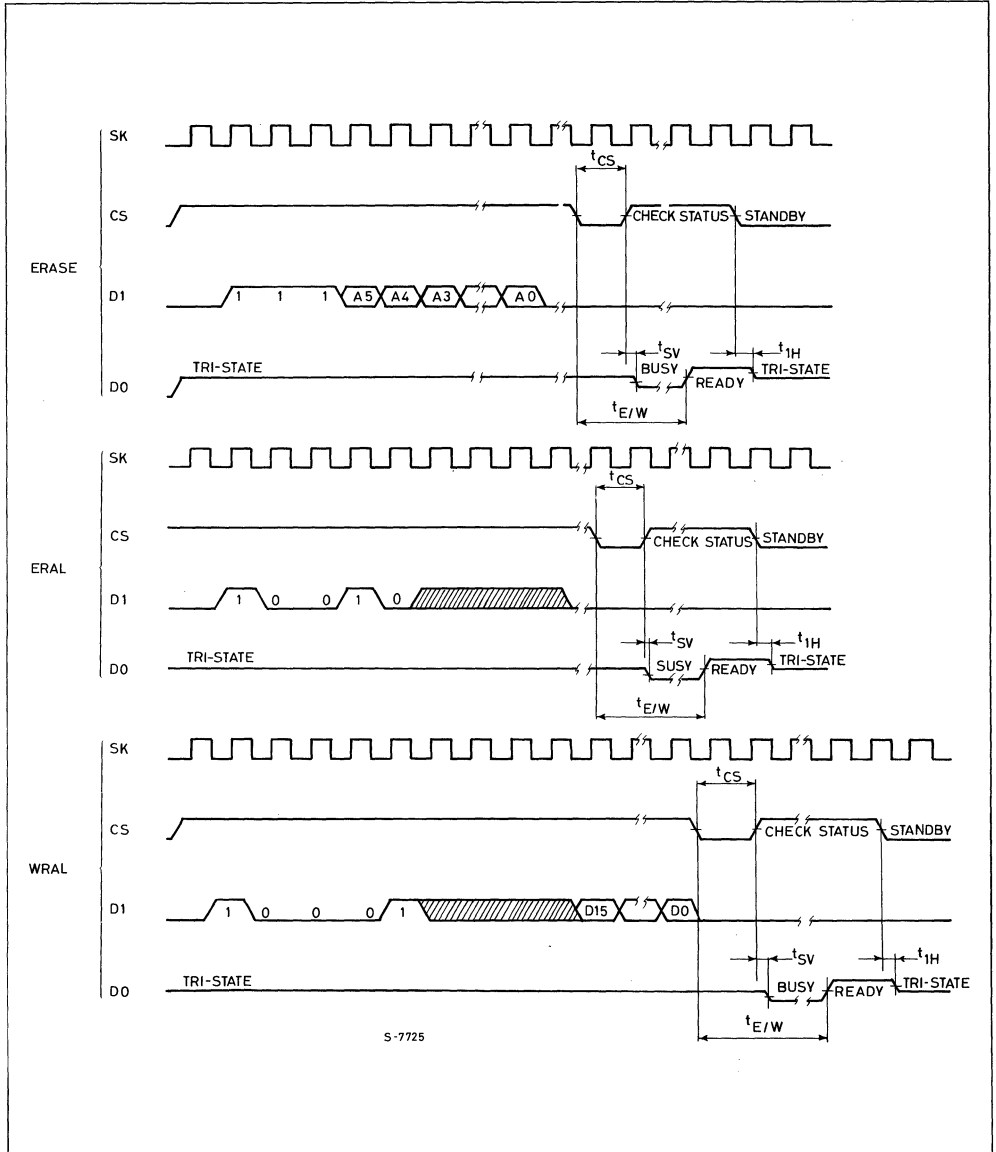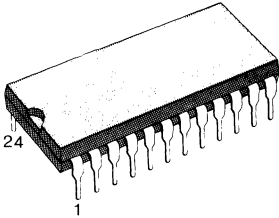

S-7725

PACKAGES

Packages

8-LEAD PLASTIC DIP
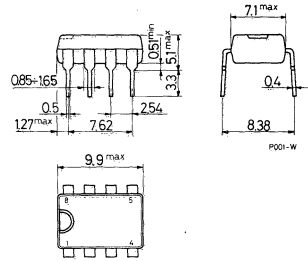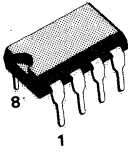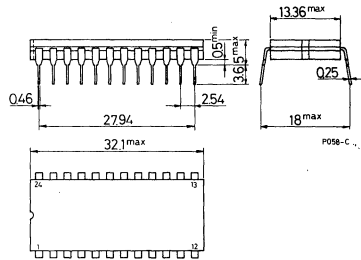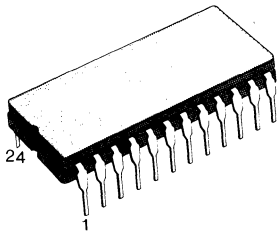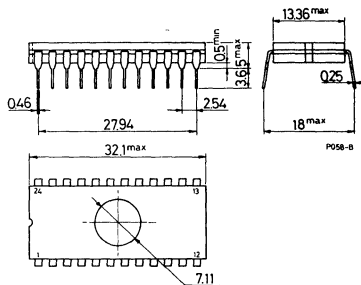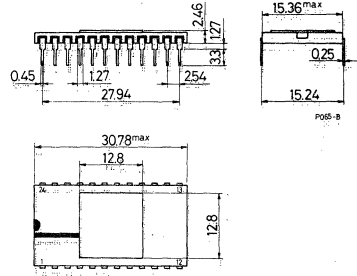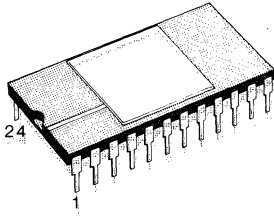

8-LEAD CERAMIC DIP (Frit-seal)
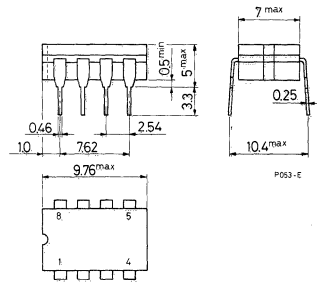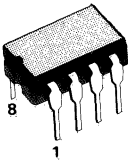
SO-8 PLASTIC
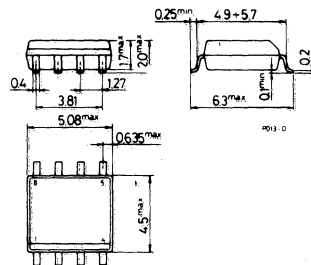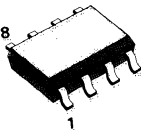
Packages

24-LEAD PLASTIC DIP

14.10 max
0.63
3.34-4.45
0.25
1.27 0.45 2.54
27.94
15.20÷16.68
32.2 max
P043 - A

24

13

1

12

24

1

24-LEAD CERAMIC DIP (Frit-seal)

13.36 max
0.5 min
3.65 max
0.25
0.46 2.54
27.94 18 max
32.1 max
P058-C

24

13

1

12

24

1

24-LEAD CERAMIC DIP (Glass lens)

13.36 max
0.5 min
3.65 max
0.25
0.46 2.54
27.94 18 max
32.1 max
P058-B

24

13

1

12

7.11

24

1
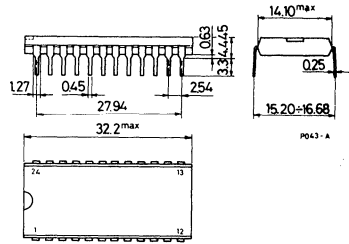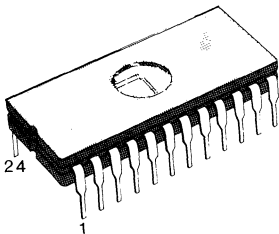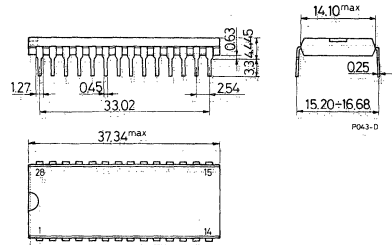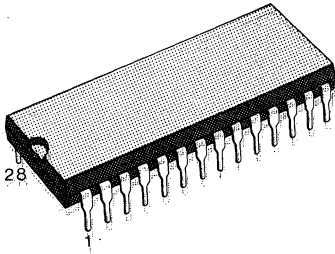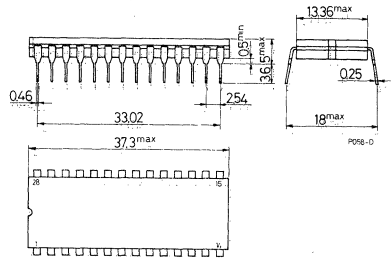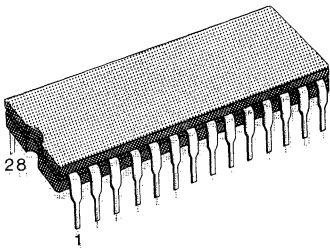
Packages

24-LEAD CERAMIC DIP

28-LEAD PLASTIC DIP
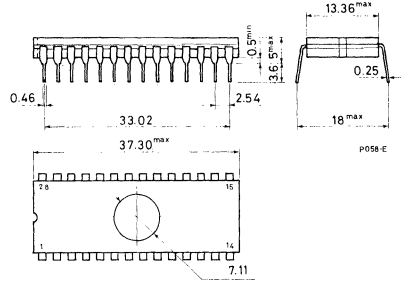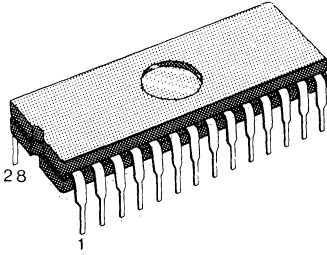

28-LEAD CERAMIC DIP (Frit-seal)

156

Packages

28-LEAD CERAMIC DIP (Glass lens)

157

RELIABILITY TEST RESULTS ON M2764

TEST	TEST CONDITION	SAMPLE	FAILURE	NOTE
SOLDERABILITY MIL-STD 883-2003	T_{amb} =240°C	425	1	uncovered area >10%
STATIC LIFE TEST MIL-STD 883-1005	V_{CC} =5V T_{amb} =125°C 　　　1000 HRS 　　　2000 HRS	 240 100	 0 0	
DYNAMIC LIFE TEST MIL-STD 883-1005	V_{CC} =5V f=500KHz T_{amb} =125°C 　　　1000 HRS 　　　2000 HRS	 475 205	 1	 single bit charge loss
LOW TEMPERATURE DYNAMIC LIFE TEST MIL-STD 883-1005	V_{CC} =5V f=500KHz T_{amb} = −10°C 　　　1000 HRS	 240	 1	 leakage
LOW TEMPERATURE ON-OFF STATIC LIFE TEST	V_{CC} =5V T_{amb} =0°C t_{ON} =15' t_{OFF} =15' 　　　2000 HRS	32	0	
RETENTION BAKE	1000 HRS　　　　T_{amb} =200°C 2000 HRS　　*T_{amb} =250°C 2000 HRS　　　　T_{amb} =200°C	510 190 100	1 0 0	single bit charge loss
TEMPERATURE CYCLING MIL-STD 883-1010	T_{amb} = −65°C to 150°C 　　　100 CYCLES 　　　500 CYCLES 　　　1000 CYCLES	 975 150 50	 0 0 0	
ELECTROSTATIC DISCARGE SENSITIVITY MIL-STD 883-3015	R=1.5 KΩ C=100 pF V=600	80	0	
WRITE ERASE CYCLING	100 CYCLES	155	0	
THERMAL SHOCKS MIL-STD 883-1011	T_{amb} − 55° to 125°C 　　　200 CYCLES	260	0	
THERMAL SHOCKS MIL-STD 883-1011 TEMPERATURE CYCLING MIL-STD 883-1010 MOISTURE RESISTANCE MIL-STD 883-1004 SEAL: FINE 　　　GROSS MIL-STD 883-1014	T_{amb} − 55° to 125°C 　　　15 CYCLES T_{amb} = −65°C TO 150°C 　　　100 CYCLES 10 CYCLES of 24 HRS T_{amb} = −10° to 65°C 　　　RH=90% TEST COND. A1 TEST COND. C	 190	 0	
MECHANICAL SHOCK MIL-STD 883-2002 VIBRATION VARIABLE FREQUENCY MIL-STD 883-2007 CONSTANT ACCELLERATION MIL-STD 883-2001 SEAL: FINE 　　　GROSS MIL-STD 883-1014	TEST. COND. B TEST. COND. A TEST. COND. D TEST COND. A1 (5.10^{-8}) TEST. COND. C (FC43 at 125°C)	 175	 0	

* WITH MULTI-LAYER PACKAGE
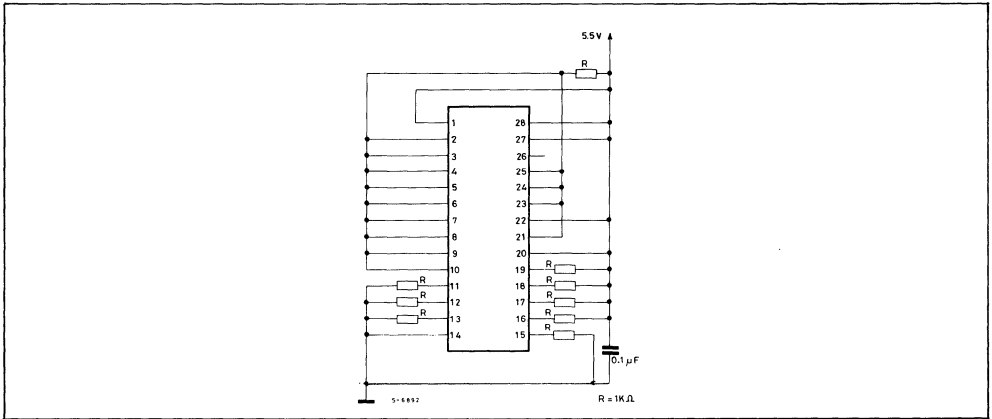
FAILURE RATE ESTIMATION

CUMULATIVE DATA M2764

LIFE TEST

ACTUAL DEVICE HRS $T_{amb} = 125°C$	LIFE TEST FAILURES	FAILURE RATE 60% C.L. %/1000 HRS $E_a = 0.6$ eV	
		$T_{amb} = 55°C$	$T_{amb} = 70°C$
1.02×10^6	1	0.0047	0.012

M2764 - BIAS LIFE TEST

M2764 - DYNAMIC LIFE TEST

Note: A0 frequency = 500 KHz
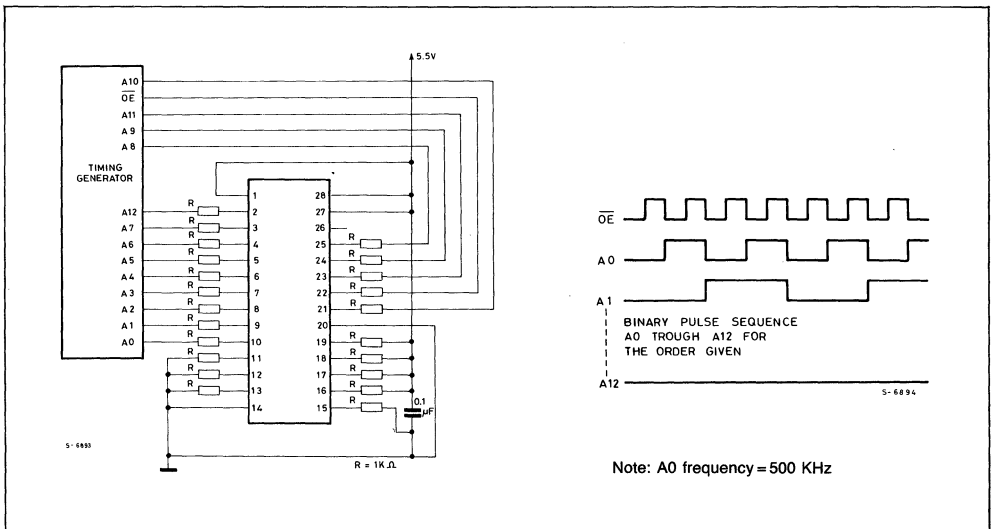
RELIABILITY TEST RESULTS ON M9306

TEST	TEST CONDITION	SAMPLE SIZE	FAILURE	NOTE
STATIC LIFE TEST MIL-STD 883-1005	$V_{CC}=5V$ $T_{amb}=125°C$			
	168 HRS	260	0	
	500 HRS	260	0	
	1000 HRS	260	0	
	2000 HRS	180	0	
DYNAMIC LIFE TEST MIL-STD 883-1005	$V_{CC}=5V$ f=250KHz $T_{amb}=125°C$			
	168 HRS	220	0	
	500 HRS	220	0	
	1000 HRS	220	0	
	2000 HRS	180	0	
PRESSURE POT	121°C − 2 ATM			
	96 HRS	200	0	
	168 HRS	200	0	
	288 HRS	200	0	
WRITE/ERASE CYCLING	$V_{CC}=5V$ $T_{amb}=80°C$ f=250 KHz			
	10000 cycle	255	0	
	100000 cylce	150	0	
RETENTION BAKE	$T_{amb}=150°C$			
	2000 HRS	290	0	
HUMIDITY TEST BS C.E.C.C. 90.000	85°C/85% RH WITH BIAS $V_{CC}=5V$			
	168 HRS	120	0	
	500 HRS	120	0	
	1000 HRS	120	0	
TEMPERATURE CYCLING MIL-STD 883-1010	$T_{amb}=-65°C$ to 150°C			
	100 CYCLES	75	0	
	1000 CYCLES	75	0	
THERMAL SHOCK MIL-STD 883-1011	$T_{amb}-55°$ to 125°C			
	200 CYCLES	50	0	
	1000 CYCLES	50	0	

M9306 - STATIC LIFE TEST

M9306 - DYNAMIC LIFE TEST

OUTPUT CONNECT to V_{CC} S-8657
$f_{CK} = 250$KHz

OUTPUT CONNECT to GND

S-8658
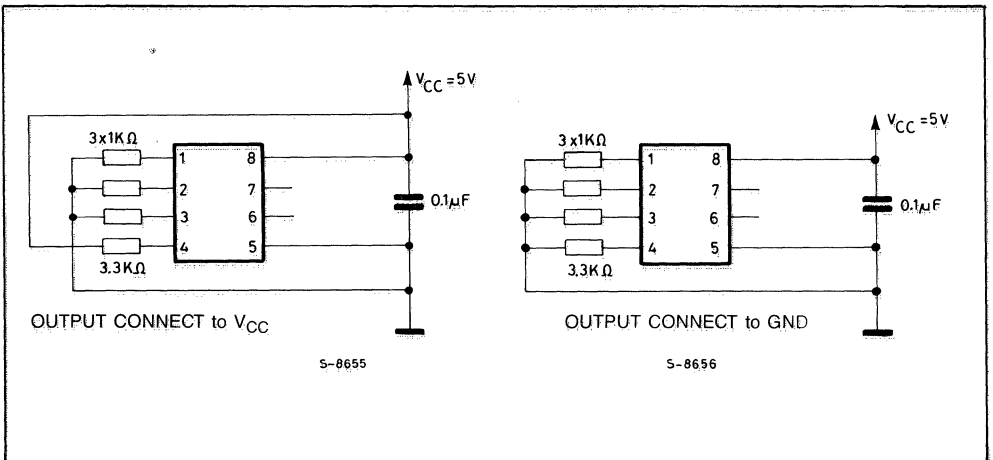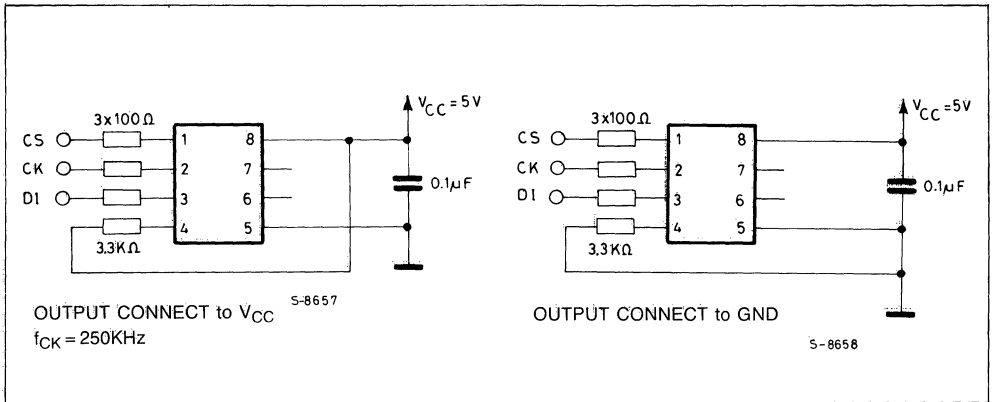
M9306 - WRITE-ERASE CYCLES TEST

$f_{CK} = 250$KHz   S-8659
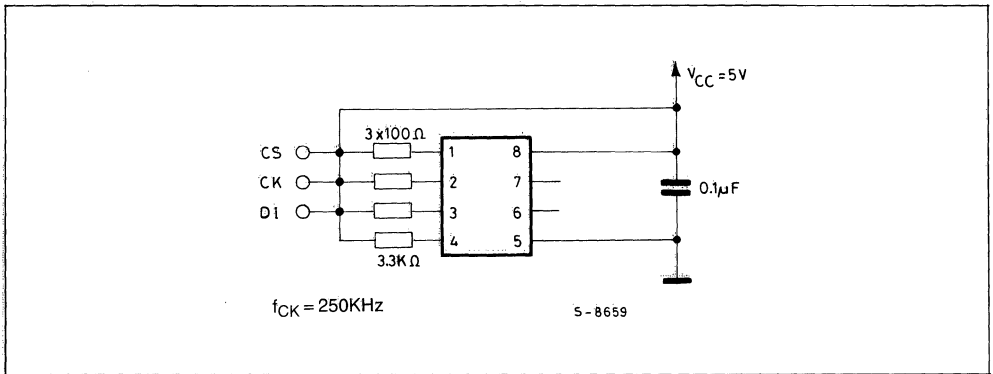
QUALITY ASSURANCE ORGANIZATION CHART

```
                           ┌─────────────────┐
                           │   Q.A. Manager  │
                           └─────────────────┘
```

Quality Control	Quality Control	Reliability	Customers Management	Off-shore Plants

- purchased goods
- supplies
- diffusion
- assembly

- finished products
- customer returns management
- qual. parts delivery
- PPM management

- test operation
- failure analysis
- engineering
- new products quality
- new processes quality

- procurement specs management
- special products
- quality management

- audit
- quality improvement
- resident engineers

FAILURE ANALYSIS PROCEDURE

The particular analytical technique used at a particular time depends on the failure mechanism and the sequence that has been followed in the failure analysis. The proper sequence is of extreme importance in order to not destroy evidence. A recommended sequence of individual steps is a follows:

1) EXTERNAL VISUAL EXAMINATION
2) ELECTRICAL TESTS (Complete and pin-to-pin tests)
3) X-RAY (For assy problems)
4) HERMETICITY TESTS (Fine and gross)
5) ULTRAVIOLET OR X-RAY (To point out package leak)
6) DECAPSULATION
7) DIE PHOTO
8) VISUAL INSPECTION
9) PASSIVATION OXIDE REMOVAL
10) ELECTRICAL PROBING
11) WIRE PULL TESTS
12) ELECTRON MICROPROBE
13) AUGER ELECTRON AND X-RAY SPECTROSCOPY
14) SELECTIVE REMOVAL OF METAL
15) S.E.M. INSPECTION
16) DECORATION TECNIQUE
17) OXIDE THICKNESS MEASUREMENTS
18) ETCHING SiO 2
19) BEVEL/STAIN
20) SIRTL ETCH
21) CROSS-SECTION
22) STORE SAMPLE
23) RECORD DATA

The preliminary steps in the failure analysis are perhaps the most important since important evidence is most likely to be lost or overlooked. Some of the more important aspects of these steps will therefore be reviewed in some detail.
As much information as possible on the failed device and the circumstances surrounding its failure, should be obtained and documented. The failed deviced should be positively identified and placed in its own receptable.
The failure most be verified. A significant number of reported failures prove to be good devices. The circuit must be tested to determine how it fails to meet data sheet specifications. In some cases tests at temperature extremes are required. Additional tests include continuity tests on each pin to determine if the wire bonds are in place and tests between pins to detect shorts or leakage paths.
External examination often reveals the problem area. The examination should be made with the un aided eye and a magnification of 30×.
Such obvious causes of failure as the following should be included in the external package examination:

1. Leads-broken, missing, or shorted
2. Glass to metal seals-corrosion at or near the seal interface, or cracked
3. Plating - peeled, incomplete, corroded.
4. Package markings - incorrect orientation would result in placing incorrect potentials or polarities on different terminals. Mistakes in type designation can also lead to devices being used for incorrect applications and inducing failures.
5. Package seal or closure interface.

At the appropriate time, the package should be decapsulated and an optical examination of the chip made.

MOS /CMOS STD PROCESS FLOW-CHART

KEY:

○ 100% OPERATION /SCREENING

□ AUDIT / MONITOR

□ GATE INSPECTION (SAMPLE)

1 - MATERIAL ACCEPTANCE

2 - WAFER / MASK FABRICATION

2A- MASK ACCEPTANCE

3 - INPROCESS EQUIPMENT ENVIRONMENT INSPECTION (AUDIT)

4 - ELECTRICAL WAFER SORT

5 - FINISHED WAFER VISUAL ACCEPTANCE

6 - DIE FABRICATION AND VISUAL SCREENING (*)

7 - DIE VISUAL ACCEPTANCE

CERAMIC PACKAGE

8 - DIF ATTACH / WIRE BOND

9 - VISUAL AND MECHANICAL CONTROL (MONITOR)
    ASSEMBLY AREA ENVIRONMENT & EQUIPMENT (AUDIT)

10 - VISUAL SCREENING (*)

11 - PRE-CAP VISUAL ACCEPTANCE

12 - SEALING / MOLDING

13 - SEALING ATMOSPHERE, SEAL ⎱
     AND LID TORQUE CONTROL ⎰   (MONITOR)
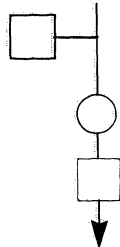
14 - CROPPING / BENDING

PLASTIC PACKAGE

PLASTIC PACKAGE

MOS /CMOS STD PROCESS FLOW-CHART (Continued)

CERAMIC
PACKAGE

PLASTIC PACKAGE
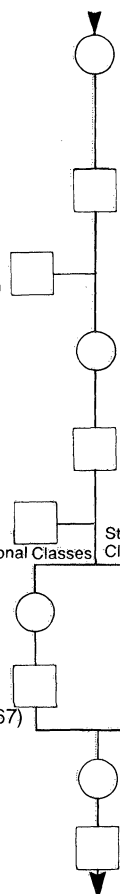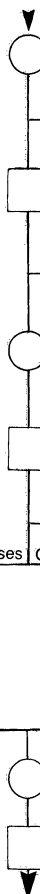
15 - VISUAL CONTROL

16 - TINNING (EXCEPT SIDE BRAZED)

17 - TINNING ACCEPTANCE

(*) Omitted when intrinsic quality meets the specified quality level.

MOS/CMOS STD & OPTIONAL PROCESS FLOW-CHART

CERAMIC
PACKAGE

PLASTIC PACKAGE

18 - LEAD TRIMMING

19 - INTERNAL WATER-VAPOR CONTENT (MONITOR)

20 - RAW-LINE ACCEPTANCE

21 - RELIABILITY TESTS STD CLASS
(REAL TIME & GROUP B C D TESTS) (MONITOR-AUDIT)

22 - ELECTRICAL TESTING AND MARKING
(SEE PAGE 167 FOR EPROM FAMILY)

23 - VISUAL AND ELECTRICAL FINAL
ACCEPTANCE (SEE PAGE 167)

23A- MECHANICAL (MONITOR) (SEE PAGE 167)

Std
Classes | Optional Classes

Optional Classes | Std Classes

24 - SCREENING OPTIONS
(TO BE AGREED WITH CUSTOMER)

25 - VISUAL, ELECTRICAL AND RELIABILITY TESTS
FINAL ACCEPTANCE (OPTIONAL CLASSES) (SEE PAGE 167)
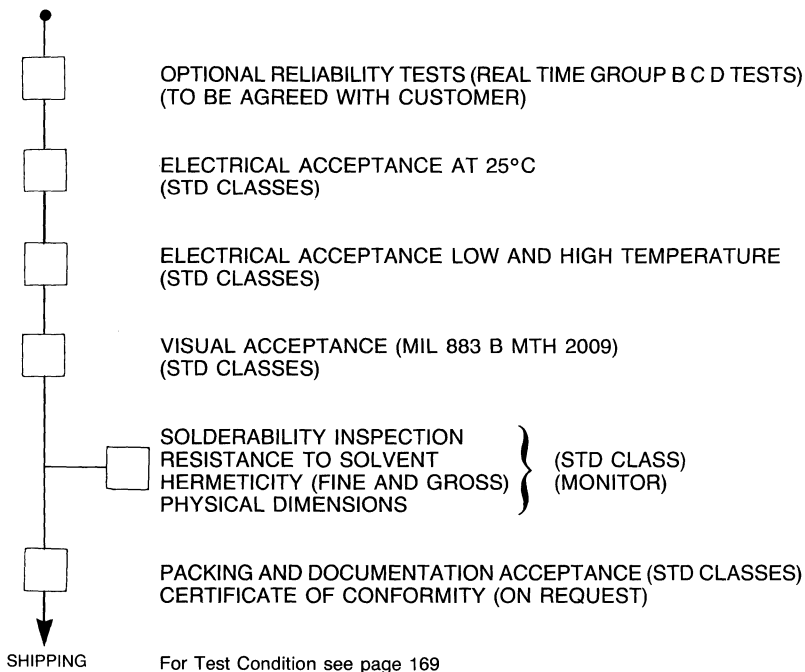
26 - PACKING

27 - PACKING AND DOCUMENTATION ACCEPTANCE
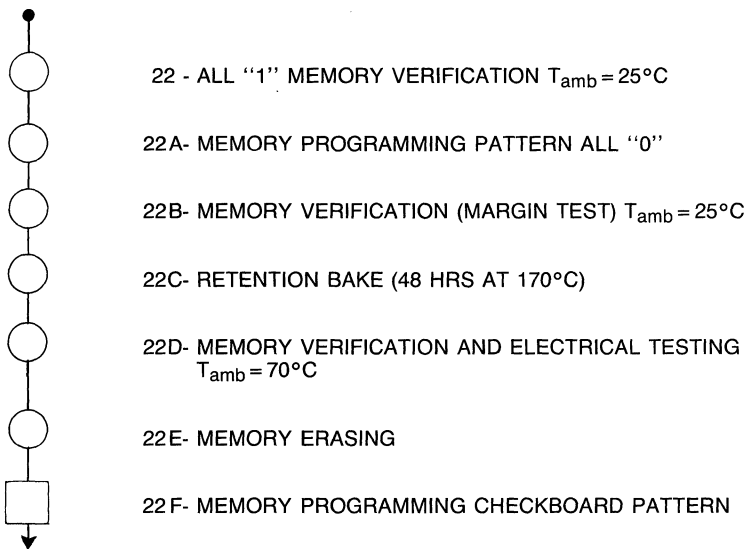
For Test Conditions see page 169

SHIPPING

SHIPPING

MOS/CMOS VISUAL AND ELECTRICAL FINAL ACCEPTANCE

OPTIONAL RELIABILITY TESTS (REAL TIME GROUP B C D TESTS)
(TO BE AGREED WITH CUSTOMER)

ELECTRICAL ACCEPTANCE AT 25°C
(STD CLASSES)

ELECTRICAL ACCEPTANCE LOW AND HIGH TEMPERATURE
(STD CLASSES)

VISUAL ACCEPTANCE (MIL 883 B MTH 2009)
(STD CLASSES)

SOLDERABILITY INSPECTION
RESISTANCE TO SOLVENT   (STD CLASS)
HERMETICITY (FINE AND GROSS)   (MONITOR)
PHYSICAL DIMENSIONS

PACKING AND DOCUMENTATION ACCEPTANCE (STD CLASSES)
CERTIFICATE OF CONFORMITY (ON REQUEST)

SHIPPING

For Test Condition see page 169

TEST FLOW FOR EPROM FAMILY

22 - ALL "1" MEMORY VERIFICATION $T_{amb} = 25°C$

22A- MEMORY PROGRAMMING PATTERN ALL "0"

22B- MEMORY VERIFICATION (MARGIN TEST) $T_{amb} = 25°C$

22C- RETENTION BAKE (48 HRS AT 170°C)

22D- MEMORY VERIFICATION AND ELECTRICAL TESTING
      $T_{amb} = 70°C$

22E- MEMORY ERASING

22F- MEMORY PROGRAMMING CHECKBOARD PATTERN

TEST FLOW FOR EPROM FAMILY (Continued)

22G- MEMORY VERIFICATION AND ELECTRICAL TESTING
$T_{amb} = 70°C$

22H- MEMORY ERASING

22 I - MARKING

22 L- PATTERN ALL "1" MEMORY VERIFICATION

23 - VISUAL AND ELECTRICAL FINAL ACCEPTANCE

PRODUCTION QUALITY TESTS DESCRIPTION AND SCREENINGS

PROCESS STEPS	TESTS	DESCRIPTIONS
1	MATERIAL ACCEPTANCE	WAFER - MASKS - WIRES - FRAMES - PHOTORESIST - CHEMICALS - PREFORMS - RESIN - BONDING TOOLS - PLASTIC TUBES - GLAZED CERAMIC PARTS MULTILAYER CERAMIC PACK - GOLD PLATED CAPS
2 A	MASK ACCEPTANCE	VISUAL DIMENSIONS
3	WAFER FABRICATION INSPECTION	
	INPROCESS	PHOSPHORUS CONTENT IN P. VAPOX
		GLASSIVATION INTEGRITY (MIL-STD 883C MTH 2021)
		S.E.M. INSPECTION (MIL-STD 883C MTH 2018)
		VISUAL AND DIMENSIONAL INSPECTION (MIL-STD 883C MTH 2010 COND. B)
	EQUIPMENT	CONTAMINATION
		D.I. WATER RESISTIVITY
		BACTERIOLOGICAL ANALYSIS OF THE D.I. WATER
	ENVIRONMENT	DUST COUNT HUMIDITY TEMPERATURE
5	FINISHED WAFERS VISUAL ACCEPTANCE	MIL-STD 883C MTH 2010 COND. B
7	DIE VISUAL ACCEPTANCE	MIL-STD 883C MTH 2010 COND. B
9	DIE ATTACH CONTROL	MIL-STD 883C MTH 2010 COND. B (INTERNAL VISUAL) AND MTH 2019 (DIE SHEAR STRENGHT)
	BONDING CONTROL	MIL-STD 883C MTH 2010 COND. B (INTERNAL VISUAL) AND MTH 2011 COND. D (BOND STRENGTH)
	ASSEMBLY AREA ENVIRONMENT CONTROL	DUST COUNT HUMIDITY TEMPERATURE
	EQUIPMENT	D.I. WATER RESISTIVITY
11	PRECAP ACCEPTANCE	MIL-STD 883C MTH 2010 COND B (INTERNAL VISUAL)
12	SEALING	VACUUM PREBAKE: 2 HRS AT 220°C HIGH TEMP. FINAL SEAL: 8 MINUTES ABOUT AT 450°C
	MOLDING AND STABILIZATION BAKE	STABILIZATION BAKE: 8 HRS AT 175°C
13	SEALING ATMOSPHERE CONTROL	MOISTURE CONTENT: < 200 PPM
	SEAL CONTROL	FINE LEAK MIL-STD 883C MTH 1014 COND. A1 HELIUM LEAK DETECTOR AFTER PRESSURIZATION IN HE FOR 2 HRS AT 4 ATM LIMIT: 5×10^{-8} CC/S FOR ICV * < 0.4 CC 2×10^{-7} CC/S FOR ICV > 0.4 CC * (ICV = INTERNAL CAVITY VOLUME)

PROCESS STEPS	TESTS	DESCRIPTIONS
13		GROSS LEAK MIL-STD 883C MTH 1014 COND. C (FLUOROCARBON GROSS LEAK) 5 TORR VACUUM FOR 1 hr EXCEPT FOR ICV > 0.1 CC FOLLOWED BY PRESSURIZATION IN MINERAL OIL AT: 4 ATM FOR 2 HRS FOR ICV < 0.1 CC OR 4 ATM FOR 10 HRS FOR ICV > 0.1 CC AND SUBSEQUENT IMMERSION IN MINERAL OIL AT $T_{amb} = 125°C$
	LID TORQUE CONTROL	CERAMIC PACKAGES ONLY MIL-STD 883C MTH 2024
15	CROPPING / BENDING CONTROL	MIL-STD 883C MTH 2009
17	TIMING ACCEPTANCE	SOLDERABILITY MIL-STD 883C MTH 2003 T_{amb} = 245 + 5°C FOR 5 + 0.5 SEC. WITH PRECONDITIONING FOR 1 hr ABOVE BOILING DIST. WATER (I.E.C. MTH AVAIL. ON REQUEST) EXTERNAL VISUAL MIL-STD 883C MTH 2009
19	INTERNAL WATER VAPOR CONTENT CONTROL	DEW POINT MTH MIL-STD 883C MTH 1018 PROCEDURE 3-5000 PPM MAX (DEW POINT TEMPER. LESS THAN − 15°C)
20	RAW LINE ACCEPTANCE	EXTERNAL VISUAL MIL-STD 883C MTH 2009 LID TORQUE TEST: AS PER STEP 13 CONSTANT ACCELERATION MIL-STD 883C MTH 2001 COND. E (30,0006) Y1 ORIENTATION ONLY * SEAL CONTROL: AS PER STEP 13
21	RELIABILITY TEST (REAL TIME AND GROUP B C D TESTS)	MONITOR ON STD CLASSES, GATE ON REQUEST (TEST AND SAMPLE SIZE TO BE AGREED WITH CUSTOMER) AUDIT ON ALL FACTORIES
23	VISUAL AND ELECTRICAL FINAL ACCEPTANCE STD CLASS	VISUAL AND MECHANICAL INSPECTION CUMULATIVE ELECTRICAL AND INOPERATIVE MECHANICAL FAILURES
23 A	MECHANICAL	SOLDERABILITY INSPECTION RESISTANCE TO SOLVENT HERMETICITY (FINE AND GROSS) PHYSICAL DIMENSIONS
27	PACKING AND DOCUMENTATION ACCEP.	VISUAL

* 20,000 G FOR PACKAGES WITH CAVITY PERIMETER OF 5 CM OF MORE AND/OR WITH A MASS OF 5 GRAMS OR MORE

NOTES

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